PSD3XX
Programmable Microcontroller Peripherals

Philips Semiconductors

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Preface

PSD3XX
Programmable Microcontroller Peripherals

PSDX3XX Programmable Microcontroller Peripherals from Philips Semiconductors

Philips Semiconductors supplies a wide range of microcontrollers peripherals for use with all of the popular microcontroller architectures. By offering a wide range of peripheral products, we can meet a broad range of specific or unique application requirements. In addition, Philips Semiconductors supplies a full line of microcontrollers based on the 80C49 and 80C51 architectures. With over 50 derivatives of the 80C51 microcontroller available, Philips Semiconductors has the broadest offering on the market.

This data handbook covers the PSD3XX products. These programmable microcontroller peripherals contain 32K to 128K bytes of EPROM (UV erasable or One Time Programmable) external program memory, 2K bytes of SRAM external data memory, and memory paging and port reconstruction logic. Philips Semiconductors' PSD3XX products interface directly to our 80C51 microcontrollers without need of any other parts. This allows the memory of the microcontroller to be increased with the addition of only one part and without the loss of the functionality of the microcontroller ports used in the interface.

Philips Semiconductors supplies a wide range of microcontrollers based on mainstream architectures, spanning 8-, 16-, and 32-bit product lines. All of our microcontrollers are based on mainstream architectures to allow our customers to take advantage of existing software and a vast array of third-party support.

Philips Semiconductors' 8-bit microcontrollers are based on the popular 80C51 and 80C49 architectures. We offer most of the Industry Standard products as well as a large selection of powerful derivatives. Many of the derivatives have an I^2C serial interface that allows them to be easily connected to over 70 other parts: this increases their capabilities even further. The 80C51 products are covered in the *80C51-Based 8-Bit Microcontrollers* data handbook (IC20) and the I^2C parts that are most commonly used with microcontrollers are covered in the *I^2C Peripherals for Microcontrollers* data handbook. Philips Semiconductors offers the most 80C51 derivatives in the world.

Philips Semiconductors' 16-bit microcontroller family is based on the powerful 68000 architecture. While these are called 16-bit microcontrollers, the 68000 CPU core architecture is 32-bit. This offers the user a great deal more processing power, when the need arises in a design to move from an 8-bit to a 16-bit microcontroller. Philips Semiconductors' 16-bit microcontrollers are software compatible with existing 68000 code. As with our popular 8-bit microcontrollers, EPROM and OTP versions of our 16-bit products are available. The 16-bit microcontrollers are covered in a separate data handbook, the IC21, *68000-Based 16-bit Microcontrollers*.

Philips Semiconductors is developing a family of 32-bit microcontrollers based on the SPARC RISC architecture. This family of microcontrollers will offer the ultimate in processing power for those applications that are computation-intensive in a embedded control environment.

Philips Semiconductors offers uncompromising quality, service, and support with all of our microcontroller and microcontroller peripheral products. For a complete family and the best in microcontroller products, look to Philips Semiconductors.

Philips Semiconductors – Microcontroller Products

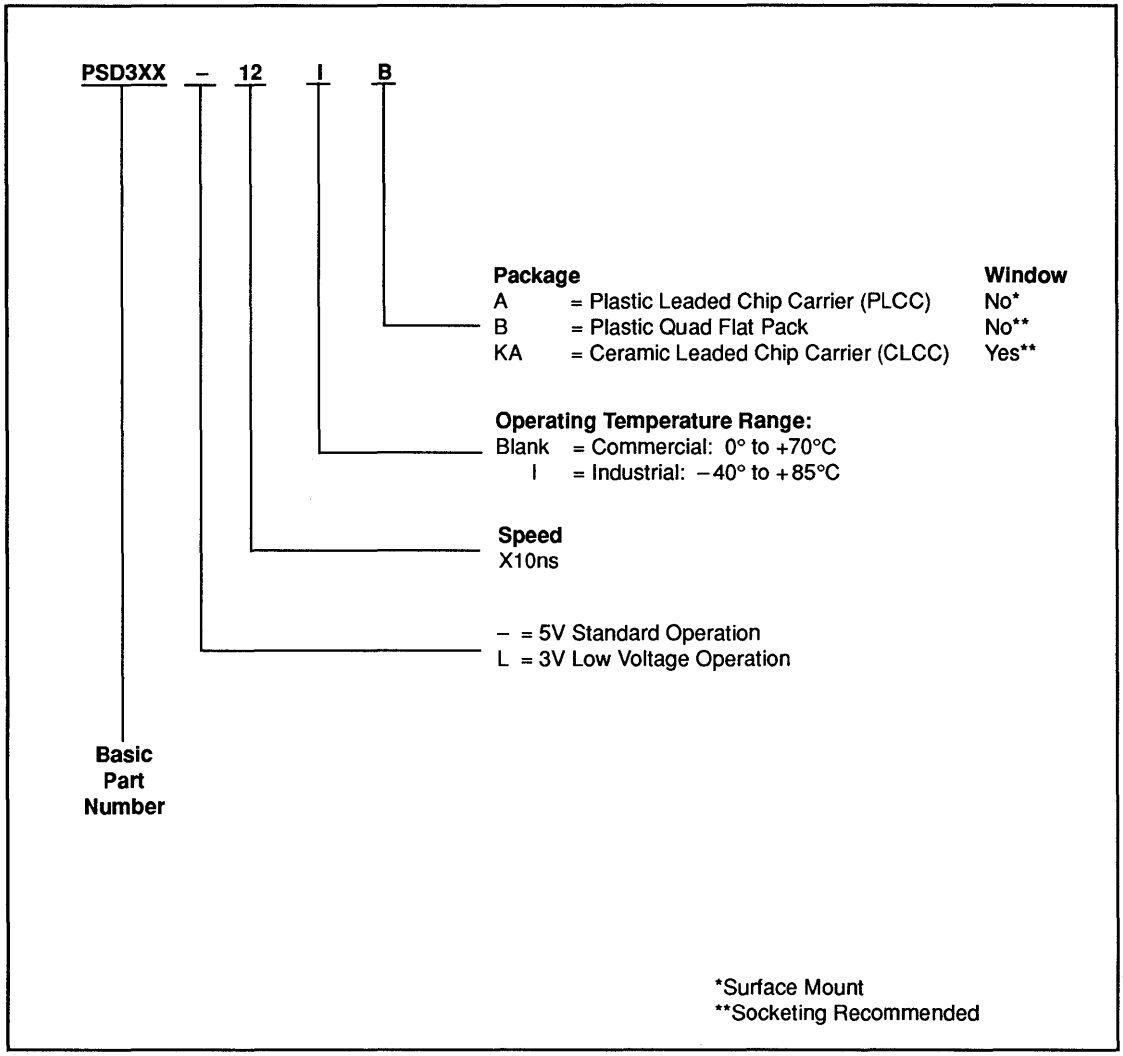
Product Status

PSD3XX
Programmable Microcontroller Peripherals

DEFINITIONS		
Data Sheet Identification	**Product Status**	**Definition**
Objective Specification	**Formative or in Design**	This data sheet contains the design target or goal specifications for product development. Specifications may change in any manner without notice.
Preliminary Specification	**Preproduction Product**	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product Specification	**Full Production**	This data sheet contains Final Specifications. Philips Semiconductors reserves the right to make changes at any time without notice, in order to improve design and supply the best possible product.

Ordering Information

PART NUMBER EXPLANATION



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Field-programmable microcontroller peripherals — PSD3XX Family

Key Features

- ❑ Single Chip Programmable Peripheral for Microcontroller-based Applications
- ❑ 19 Individually Configurable I/O pins that can be used as
  - — Microcontroller I/O port expansion
  - — Programmable Address Decoder (PAD) I/O
  - — Latched address output
  - — Open drain or CMOS
- ❑ Two Programmable Arrays (PAD A and PAD B)
  - — Total of 40 Product Terms and up to 16 Inputs and 24 Outputs
  - — Address Decoding up to 1 MB
  - — Logic replacement
- ❑ "No Glue" Microcontroller Chip-Set
  - — Built-in address latches for multiplexed address/data bus
  - — Non-multiplexed address/data bus mode
  - — ALE and Reset polarity programmable
  - — Selectable modes for read and write control bus as $\overline{RD}/\overline{WR}$ or R/$\overline{W}$/E
- ❑ 256 Kbits of UV EPROM
  - — Configurable as 32K x 8 or as 16K x 16
  - — Divides into 8 equal mappable blocks for optimized mapping
  - — Block resolution is 4K x 8 or 2K x 16
  - — 120 ns EPROM access time, including input latches and PAD address decoding.
- ❑ 16 Kbit Static RAM
  - — Configurable as 2K x 8 or as 1K x 16
  - — 120 ns SRAM access time, including input latches and PAD address decoding
- ❑ Address/Data Track Mode
  - — Enables easy Interface to Shared Resources (Mail Box SRAM) with other Microcontrollers or a Host Processor
- ❑ Built-In Security
  - — Locks the PSD3XX Configuration and PAD Decoding
- ❑ Available in a Variety of Packaging
  - — 44 Pin PLDCC and CLDCC
- ❑ Simple Menu-Driven Software: Configure the PSD3XX on an IBM PC

PSD3XX Family Feature Summary

Part	PLD Inputs/ Product Terms	Ports	EPROM Size	SRAM Size	Configuration	Memory Paging	C-Miser Bit	Security Bit
PSD301®	14/40	19	256 Kb	16 Kb	x8 or x16		X	X
PSD311	14/40	19	256 Kb	16 Kb	x8		X	X
PSD302	18/40	19	512 Kb	16 Kb	x8 or x16	X	X	X
PSD312	18/40	19	512 Kb	16 Kb	x8	X	X	X
PSD303	18/40	19	1 Mb	16 Kb	x8 or x16	X	X	X
PSD313	18/40	19	1 Mb	16 Kb	x8	X	X	X

Partial Listing of Microcontrollers Supported

- **Motorola family:**
  M6805, M68HC11, M68HC16, M68000/10/20, M60008, M683XX
- **Intel family:**
  8031/8051, 8096/8098, 80186/88, 80196/98
- **Signetics:**
  SC80C451, SC80552
- **TI:**
  SC80C451, TMS320C14
- **Zilog:**
  Z8, Z80, Z180
- **National:**
  HPC16000, HPC46400

Applications

- Computers (Notebook and Portable PCs)
  - Fixed Disk Control, Modem, Imaging, Laser Printer Control
- Telecommunications
  - Modem, Cellular Phone, Digital PBX, Digital Speech, FAX, Digital Signal Processing
- Portable Industrial Equipment
  - Measurement Meters, Data Recorders
- Medical Instrumentation
  - Hearing Aids, Monitoring Equipment, Diagnostic Tools

Introduction

The PSD3XX Series are members of the rapidly growing family of PSD devices. They are the market's first low-voltage single-chip solution for microcontroller-based applications where consistent specifications for design, fast time-to-market, small form factor, and low power consumptions are essential. When combined in an 8- or 16-bit system, virtually any microcontroller (68HC11, 8051, 80186, etc.) and the PSD3XX device work together to create a very powerful chip-set solution. This implementation eliminates mixing and matching low voltage specifications for various discrete components. It also provides all the required control and peripheral elements needed in a microcontroller-based system with no external discrete "glue" logic required.

The solution comes complete with simple system software development tools for integrating the PSD3XX with the microcontroller. Hosted on IBM PC platforms or compatibles, the easy to use software enables the designer to quickly configure the device and use it immediately.

Product Description

The PSD3XX family integrates high performance user-configurable blocks of EPROM, SRAM, and programmable logic. The major functional blocks include two programmable logic arrays, PAD A and PAD B, 256K to 1Mbit of EPROM, 16K bits of SRAM, input latches, and output ports. The PSD3XX family is ideal for applications requiring low power and very small form factors. These include hard disk control, modems, cellular telephones, instrumentation, computer peripherals, military and similar applications.

The PSD3XX family offers a unique single-chip solution for microcontrollers that need:

- I/O reconstruction (microcontrollers lose at least two I/O ports when accessing external resources).
- More EPROM and SRAM than the microcontroller's internal memory.
- Chip-select, control, or latched address lines that are otherwise implemented discretely.
- An interface to shared external resources.
- Expanded microcontroller address space.

The PSD3XX Family Architecture (Figure 1) can efficiently interface with, and enhance, any low-voltage 8- or 16-bit microcontroller system. This is the first solution that provides microcontrollers with port expansion, latched addresses, page logic, two programmable logic arrays (PAD A and PAD B), an interface to shared resources, 256K, 512K or 1M bit EPROM, and 16K bit SRAM on a single chip. The PSD3XX family does not require any glue logic for interfacing to any 8- or 16-bit microcontroller.

The 8051 microcontroller family can take full advantage of the PSD3XX's separate program and data address spaces. Users of the 68HCXX microcontroller family can change the functionality of the control signals and directly connect the R/$\overline{W}$ and E, or the R/$\overline{W}$ and DS signals. (Users of 16-bit microcontrollers, including the 80186, 8096, 80196 and 16XXX, can use the PSD301/302/303 in a 16-bit configuration). Address and data buses can be configured as separate or multiplexed, whichever is required by the host processor.

The flexibility of the PSD3XX I/O ports permits interfacing to shared resources. The arbitration can be controlled internally by PAD A outputs. The user can assign the following functions to these ports: standard I/O pins, chip-select outputs from PAD A and PAD B, or latched address or multiplexed low-order address/data byte. This enables users to design add-on systems such as disk drives, modems, etc., that easily interface to the host bus (e.g., IBM PC, SCSI).

The page register extends the accessible address space of certain microcontrollers from 64 K to 1 M. There are 16 pages that can serve as base address inputs to the PAD, thereby enlarging the address space of 16 address line microcontrollers by a factor of 16.

Figure 1. PSD3XX Family Architecture

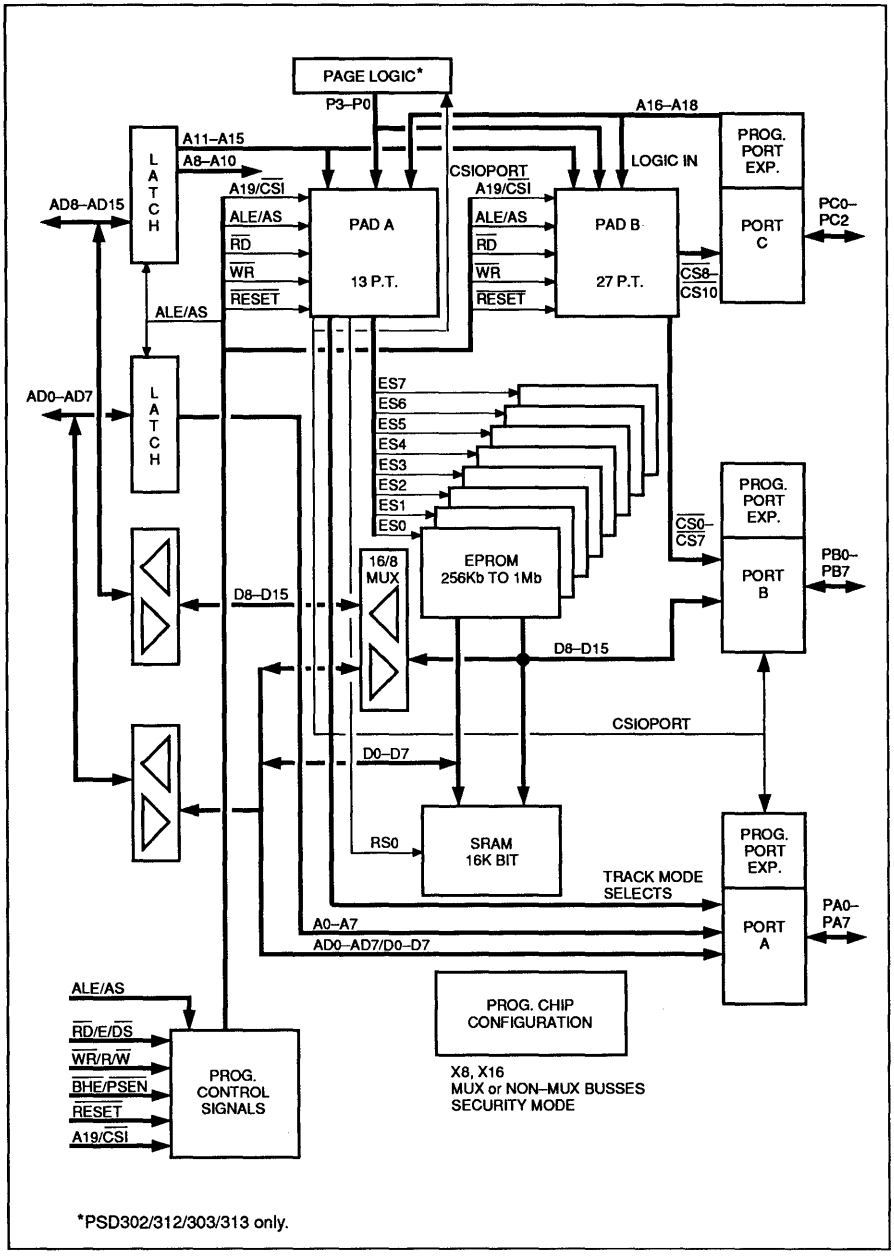


Table 1. PSD3XX Pin Descriptions

Name	Type	Description
$\overline{BHE}/\overline{PSEN}$ (PSD30X Devices)	I	When the data bus width is 8 bits (CDATA = 0), this pin is $\overline{PSEN}$. In this mode, $\overline{PSEN}$ is the active low EPROM read pulse. The SRAM and I/O ports read signal is generated according to the description of the $\overline{WR}/V_{PP}$ or R/$\overline{W}$ and $\overline{RD}/\overline{E}/\overline{DS}$ pins. If the host processor is a member of the 8031 family, $\overline{PSEN}$ must be connected to the corresponding host pin. In other 8-bit host processors that do not have a special EPROM-only read strobe, PSEN should be tied to V_{CC}. In this case, $\overline{RD}$ or E and R/$\overline{W}$ provide the read strobe for the SRAM, I/O ports, and EPROM. When the data bus width is configured as 16 (CDATA = 1), this pin is $\overline{BHE}$. When $\overline{BHE}$ is low, data bus bits D8–D15 are read from, or written into, the PSD3XX, depending on the operation being read or write, respectively. In programming mode, this pin is pulsed between V_{PP} and 0.
or		
$\overline{PSEN}$ (PSD31X Devices Only)	I	The $\overline{PSEN}$ is the active low EPROM read pulse. The SRAM and I/O ports read signal is generated according to the description of the $\overline{WR}/V_{PP}$ or R/$\overline{W}$, and $\overline{RD}$/E pins. If the host processor is a member of the 8031 family, $\overline{PSEN}$ must be connected to the correspondinbg host pin. In other 8-bit host processors that do not have a special EPROM-only read strobe, $\overline{PSEN}$ should be tied to V_{CC}. In this case, $\overline{RD}$ or E and R/$\overline{W}$ provide the read strobe for the SRAM, I/O ports, and EPROM.
$\overline{WR}/V_{PP}$ or R/$\overline{W}/V_{PP}$	I	In the operating mode this pin's function is $\overline{WR}$ (CRRWR = 0) or R/$\overline{W}$ (CRRWR = 1) when configured as R/$\overline{W}$. The following tables summarize the read and write operations (CRRWR = 1): CEDS = 0 R/$\overline{W}$ | E | X | 0 | NOP 0 | 1 | write 1 | 1 | read CEDS = 1 R/$\overline{W}$ | $\overline{DS}$ | X | 1 | NOP 0 | 0 | write 1 | 0 | read When configured as $\overline{WR}$, a write operation is executed during an active low pulse. When configured as R/$\overline{W}$, with R/$\overline{W}$ = 1 and E = 1, a read operation is executed; if R/$\overline{W}$ = 0 and E = 1, a write operation is executed. In programming mode, this pin must be tied to V_{PP} voltage.
$\overline{RD}/\overline{E}/\overline{DS}$ (Note 2)	I	The pin function depends on the CRRWR and CEDS configuration bits. If CRRWR = 0, $\overline{RD}$ is an active low read pulse. When CRRWR = 1, this pin and the R/$\overline{W}$ pin define the following cycle type: If CEDS = 0, E is an active high strobe. If CEDS = 1, $\overline{DS}$ is an active low strobe.
or		
$\overline{RD}$/E (Note 3)	I	When configured as $\overline{RD}$ (CRRWR = 0), this pin provides an active low $\overline{RD}$ strobe. When configured as E (CRRWR = 1), this pin becomes an active high pulse, which, together with R/$\overline{W}$ defines the cycle type. Then, if R/$\overline{W}$ = 1 and E = 1, a read operation is executed. If R/$\overline{W}$ = 0 and E = 1, a write operation is executed.

Legend: The I/O column abbreviations are: I = input; I/O = input/output; P = power.

NOTE: 1. All the configuration bits mentioned in Table 1 appear in parentheses and are explained in the Configuration Register section.
2. PSD302/312/303/313 only.
3. PSD301/311 only.

Table 1. PSD3XX Pin Descriptions (Cont.)

Name	Type	Description
$\overline{CSI}$/A19	I	This pin has two configurations. When it is $\overline{CSI}$ (CA19/$\overline{CSI}$ = 0) and the pin is asserted high, the device is deselected and powered down. (See Tables 12 and 13 for the chip state during power-down mode.) If the pin is asserted low, the chip is in normal operational mode. When it is configured as A19, (CA19/$\overline{CSI}$ = 1), this pin can be used as an additional input to the PAD. CADLOG3 = 1 defines the pin as an address; CADLOG3 = 0 defines it as a logic input. If it is an address, A19 can be latched with ALE (CADDHLT = 1) or be a transparent logic input (CADDHLT = 0). In this mode, there is no power-down capability.
RESET	I	The user-programmable pin can be configured to reset on high level (CRESET = 1) or on low level (CRESET = 0). It should remain active for at least 100 ns. See Tables 10a, 10b and 11 for the chip state after reset.
ALE or AS	I	In the multiplexed modes, the ALE pin functions as an Address Latch Enable or as an Address strobe and can be configured as an active high or active low signal. The ALE or AS trailing edge latches lines AD15/A15–AD0/A0 and A16–A19 in 16-bit mode (AD7/A7–AD0/A0 and A16–A19 in 8-bit mode) and $\overline{BHE}$, depending on the PSD3XX configuration. See Table 8. In the non-multiplexed modes, it can be used as a general-purpose logic input to the PAD.
PA7 PA6 PA5 PA4 PA3 PA2 PA1 PA0	I/O	PA7–PA0 is an 8-bit port that can be configured to track AD7/A7–AD0/A0 from the input (CPAF2 = 1). Otherwise (CPAF2 = 0), each bit can be configured separately as an I/O or lower-order latched address line. When configured as an I/O (CPAF1 = 0), the direction of the pin is defined by its direction bit, which resides in the direction register. If a pin is an I/O output, its data bit (which resides in the data register) comes out. When it is configured as a low-order address line (CPAF1 =1), A7–A0 can be made the corresponding output through this port (e.g., PA6 can be configured to be the A6 address line). Each port bit can be a CMOS output (CPACOD = 0) or an open drain output (CPACOD = 1). When the chip is in non-multiplexed mode (CADDRAT = 0), the port becomes the data bus lines (D0–D7). See Figure 4.
PB7 PB6 PB5 PB4 PB3 PB2 PB1 PB0	I/O	PB7–PB0 is an 8-bit port for which each bit can be configured as an I/O (CPBF = 1) or chip-select output (CPBF = 0). Each port bit can be a CMOS output (CPBCOD = 0) or an open drain output (CPBCOD = 1). When configured as an I/O, the direction of the pin is defined by its direction bit, which resides in the direction register. If a pin is an I/O output, its data (which resides in the data register) comes out. When configured as a chip-select output, $\overline{CS0}$–$\overline{CS3}$ are a function of up to four product terms of the inputs to the PAD B; $\overline{CS4}$,–$\overline{CS7}$ then are each a function of up to two product terms. On the PSD301L/302L/303L, when the chip is in non-multiplexed mode (CADDRAT = 0) and the data bus width is 16 (CDATA = 1), the port becomes the data bus (D8–D15). See Figure 6.

Table 1. PSD3XX Pin Descriptions (Cont.)

Name	Type	Description
PC0 PC1 PC2	I/O	This is a 3-bit port for which each bit is configurable as a PAD A and B input or output. When configured as an input (CPCF = 0), a bit individually becomes an address (CADLOG = 1) or a logic input (CADLOG = 0). The addresses can be latched with ALE (CADDHLT = 1) or be transparent inputs to the PADs (CADDHLT = 0). When a pin is configured as an output (CPCF = 1), it is a function of one product term of all PAD inputs. See Figure 7.
AD0/A0 AD1/A1 AD2/A2 AD3/A3 AD4/A4 AD5/A5 AD6/A6 AD7/A7	I/O	In multiplexed mode, these pins are the multiplexed low-order address/data byte. After ALE latches the addresses, these pins input or output data, depending on the settings of the $\overline{RD}$/E ($\overline{RD}$/E/$\overline{DS}$ on the PSD302/303), $\overline{WR}$/V_{PP} or R/$\overline{W}$, and $\overline{BHE}$/$\overline{PSEN}$ pins. In non-multiplexed mode, these pins are the low-order address input.
AD8/A8 AD9/A9 AD10/A10 AD11/A11 AD12/A12 AD13/A13 AD14/A14 AD15/A15	I/O	In 16-bit multiplexed mode, these pins are the multiplexed high-order address/data byte. After ALE latches the addresses, these pins input or output data, depending on the settings of the $\overline{RD}$/E or $\overline{RD}$/E/$\overline{DS}$, $\overline{WR}$/V_{PP} or R/$\overline{W}$, and $\overline{BHE}$/$\overline{PSEN}$ pins. In all other modes, these pins are the high-order address input.
GND	P	V_{SS} (ground) pin.
V_{CC}	P	Supply voltage input.

Operating Modes

The PSD3XX's four operating modes enable it to interface directly to 8- and 16-bit microcontrollers with multiplexed and non-multiplexed address/data buses. These operating modes are:

- Multiplexed 8-bit address/data bus
- Multiplexed 16-bit address/data bus (PSD30X)
- Non-multiplexed address/data, 8-bit data bus
- Non-multiplexed 16-bit address/data bus (PSD30X)

Multiplexed 8-bit Address/Data Bus

This mode is used to interface to microcontrollers with an 8-bit data bus and a 16-bit or larger address bus. The address/data bus (AD0/A0–AD7/A7) is bi-directional and permits the latching of the address when the ALE signal is active. On the same pins, the data is read from or written to the device; this depends on the state of the $\overline{RD}$/E or $\overline{RD}$/E/$\overline{DS}$ pin, $\overline{BHE}$/$\overline{PSEN}$ or $\overline{PSEN}$ pin and $\overline{WR}$/V_{PP} or R/$\overline{W}$ pins. The high-order address/data bus (AD8/A8–AD15/A15) contains the high-order address bus byte. Ports A and B can be configured as in Table 2.

Multiplexed 16-bit Address/Data Bus

This mode is used to interface to microcontrollers with a 16-bit data bus and a 16-bit or larger address bus. The low-order address/data bus (AD0/A0–AD7/A7) is bi-directional and permits the latching of the address when the ALE signal is active. On the same pins, the data is read from or written to the device; this depends on the state of the $\overline{RD}$/E/$\overline{DS}$, $\overline{BHE}$/$\overline{PSEN}$, and $\overline{WR}$/V_{PP} or R/$\overline{W}$ pins. The high-order address/data bus (AD8/A8–AD15/A15) is bi-directional and permits latching of the high-order address when the ALE signal is active on the same pins. The high-order data bus is read from or written to the device, depending on the state of the $\overline{RD}$/E/$\overline{DS}$, $\overline{BHE}$/$\overline{PSEN}$, and $\overline{WR}$/V_{PP} or R/$\overline{W}$ pins. Ports A and B can be configured as in Table 2.

Non-Multiplexed Address/Data, 8-bit Data Bus

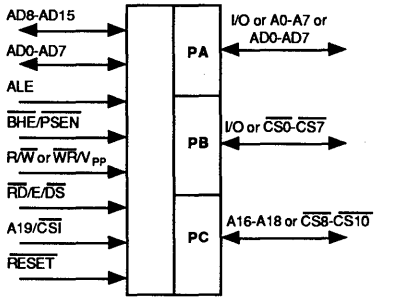
This mode is used to interface to non-multiplexed 8-bit microcontrollers with an 8-bit data bus and a 16-bit or larger address bus. The low-order address/data bus (AD0/A0–AD7/A7) is the low-order address input bus. The high-order address/data bus (AD8/A8–AD15/A15) (A8–A15 on the PSD31X) is the high-order address bus byte. Port A is the low-order data bus. Port B can be configured as shown in Table 2.

Non-Multiplexed Address/Data, 16-bit Data Bus

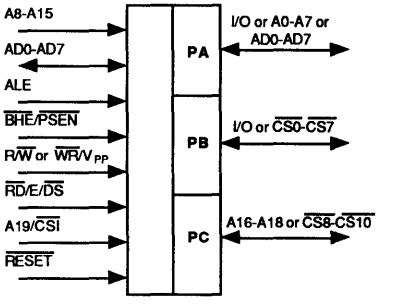
This mode is used to interface to non-multiplexed 16-bit microcontrollers with a 16-bit data bus and a 16-bit or larger address bus. The low-order address/data bus (AD0/A0–AD7/A7) is the low-order address input bus. The high-order address/data bus (AD8/A8–AD15/A15) is the high-order address bus byte. Port A is the low-order data bus. Port B is the high-order data bus.

Table 2 summarizes the effect of the different operating modes on ports A, B, and the address/data pins. The configuration of Port C is independent of the four operating modes.

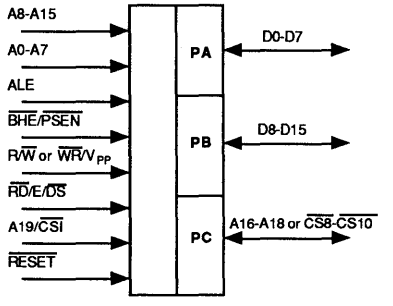
Figure 2a. PSD3XX Port Configurations (x8/x16)



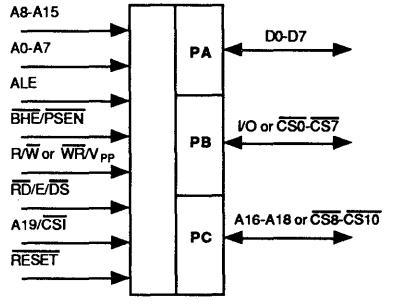
1. Configured for multiplexed 16-bit address/data bus.



2. Configured for multiplexed 8-bit address/data bus.

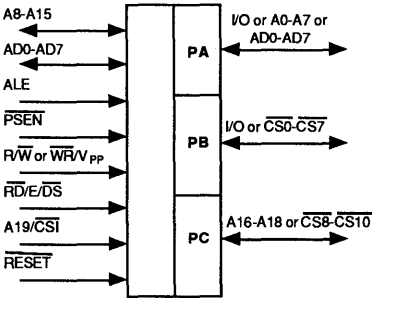


3. Configured for non-multiplexed 16-bit address/data bus.

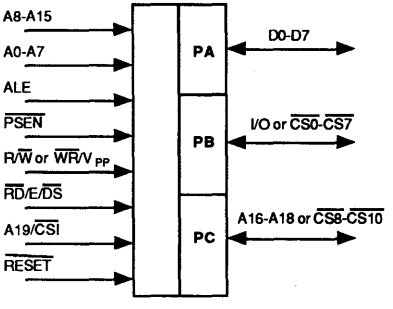


4. Configured for non-multiplexed address/data, 8-bit bus.

Figure 2b. PSD3XX Port Configurations (x8 Only)



1. Configured for multiplexed 8-bit address/data bus.



2. Configured for non-multiplexed address/data, 8-bit bus.

Legend: AD8–AD15 = Addresses A8–A15 multiplexed with data lines D8–D15.
AD0–AD7 = Addresses A0–A7 multiplexed with data lines D0–D7.

Table 2. PSD30X Bus and Port Configuration Options

	Multiplexed Address/Data	Non-Multiplexed Address/Data
8-bit Data Bus		
Port A	I/O or low-order address lines or Low-order multiplexed address/data byte	D0–D7 data bus byte
Port B	I/O or $\overline{CS0}$–$\overline{CS7}$	I/O and/or $\overline{CS0}$–$\overline{CS7}$
AD0/A0–AD7/A7	Low-order multiplexed address/data byte	Low-order address bus byte
AD8/A8–AD15/A15	High-order multiplexed address data byte	High-order address bus byte
16-bit Data Bus		
Port A	I/O or low-order address lines or Low-order multiplexed address/data byte	Low-order data bus byte
Port B	I/O or $\overline{CS0}$–$\overline{CS7}$	High-order data bus byte
AD0/A0–AD7/A7	Low-order multiplexed address/data byte	Low-order address bus byte
AD8/A8–AD15/A15	High-order multiplexed address/data byte	High-order address bus byte

Table 2a. PSD31X Bus and Port Configuration Options

	Multiplexed Address/Data	Non-Multiplexed Address/Data
8-bit Data Bus		
Port A	I/O or low-order address lines or Low-order multiplexed address/data byte	D0–D7 data bus byte
Port B	I/O or $\overline{CS0}$–$\overline{CS7}$	I/O and/or $\overline{CS0}$–$\overline{CS7}$
AD0/A0–AD7/A7	Low-order multiplexed address/data byte	Low-order address bus byte
A8–A15	High-order address bus byte	High-order address bus byte

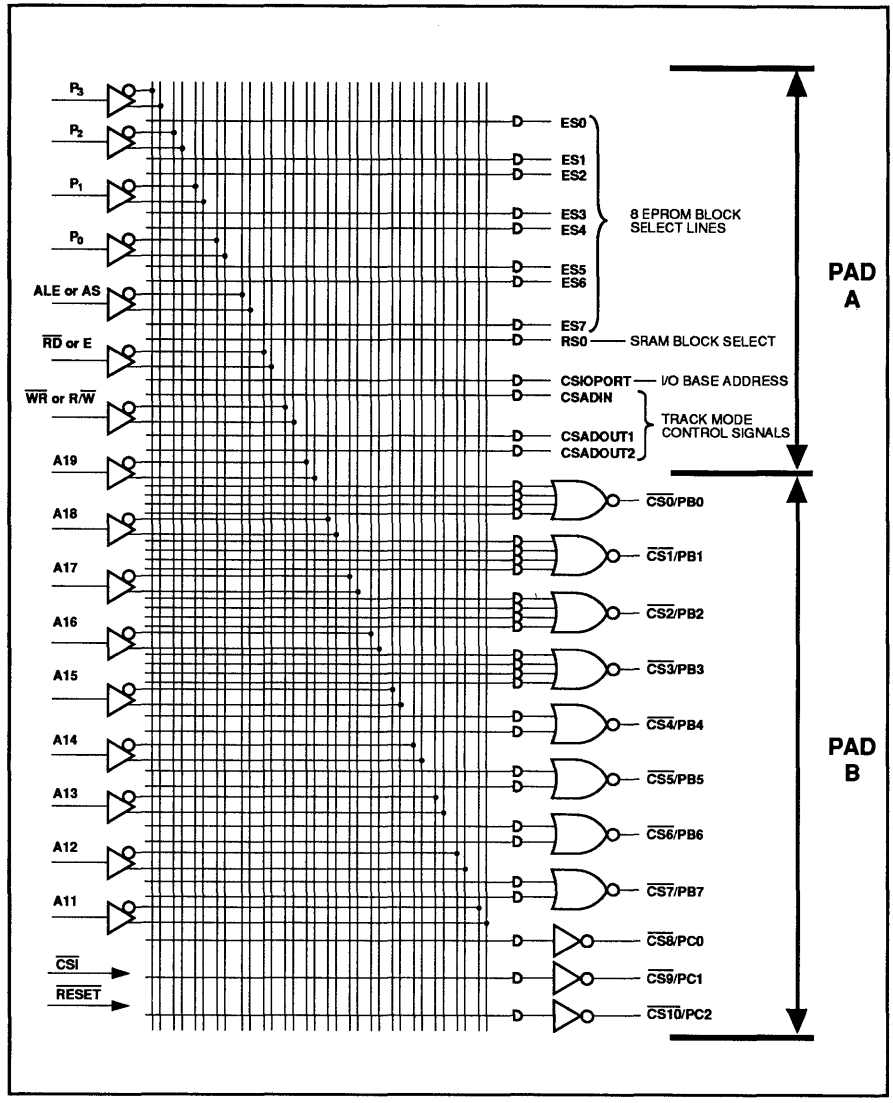
Programmable Address Decoder (PAD)

The PSD3XX consists of two programmable arrays referred to as PAD A and PAD B (Figure 3). PAD A is used to generate chip select signals derived from the input address to the internal EPROM blocks, SRAM, I/O ports, and Track Mode signals. All its I/O functions are listed in Table 3 and shown in Figure 3. PAD B outputs to Ports B and C for off-chip usage.

PAD B can also be used to extend the decoding to select external devices or as a random logic replacement. The input bus to both PAD A and PAD B is the same.

Using MAPLE software, each programmable bit in the PAD's array can have one of three logic states of 0, 1, and don't care (X). In a user's logic design, both PADs can share the same inputs using the X for input signals that are not supposed to affect other functions. The PADs use reprogrammable CMOS EPROM technology and can be programmed and erased by the user.

Figure 3. PAD Description



NOTES: 4. $\overline{CSI}$ is a power-down signal. When high, the PAD is in stand-by mode and all its outputs become non-active. See Tables 12 and 13.

5. RESET deselects all PAD output signals. See Tables 10 and 11.
6. A18, A17, and A16 are internally multiplexed with $\overline{CS10}$, $\overline{CS9}$, and $\overline{CS8}$, respectively. Either A18 or $\overline{CS10}$, A17 or $\overline{CS9}$, and A16 or $\overline{CS8}$ can be routed to the external pins of Port C. Port C can be configured as either input or output.
7. P_0–P_3 are not included on PSD3X1 devices.

Table 3. PSD3XX PAD A and PAD B Functions

	Function
PAD A and PAD B Inputs	
A19/$\overline{CSI}$	In $\overline{CSI}$ mode (when high), PAD deselects all of its outputs and enters a power-down mode (see Tables 12 and 13). In A19 mode, it is another input to the PAD.
A16–A18	These are general purpose inputs from Port C. See Figure 3, Note 4.
A11–A15	These are address inputs.
P0–P3	These are page number inputs (for the PSD302/312/303/313 only).
$\overline{RD}$ or E	This is the read pulse or enable strobe input.
$\overline{WR}$ or R/$\overline{W}$	This is the write pulse or R/$\overline{W}$ select signal.
ALE	This is the ALE input to the chip.
RESET	This deselects all outputs from the PAD; it can not be used in product term equations. See Tables 10 and 11.
PAD A Outputs	
ES0–ES7	These are internal chip-selects to the 8 EPROM banks. Each bank can be located on any boundary that is a function of one product term of the PAD address inputs.
RS0	This is an internal chip-select to the SRAM. Its base address location is a function of one term of the PAD address inputs.
CSIOPORT	This internal chip-select selects the I/O ports. It can be placed on any boundary that is a function of one product term of the PAD inputs. See Tables 6 and 7.
CSADIN	This internal chip-select, when Port A is configured as a low-order address/data bus in the track mode (CPAF2 = 1), controls the input direction of Port A. CSADIN is gated externally to the PAD by the internal read signal. When CSADIN and a read operation are active, data presented on Port A flows out of AD0/A0–AD7/A7. This chip-select can be placed on any boundary that is a function of one product term of the PAD inputs. See Figure 5.
CSADOUT1	This internal chip-select, when Port A is configured as a low-order address/data bus in track mode (CPAF2 = 1), controls the output direction of Port A. CSADOUT1 is gated externally to the PAD by the ALE signal. When CSADOUT1 and the ALE signal are active, the address presented on AD0/A0–AD7/A7 flows out of Port A. This chip-select can be placed on any boundary that is a function of one product term of the PAD inputs. See Figure 5.
CSADOUT2	This internal chip-select, when Port A is configured as a low-order address/data bus in the track mode (CPAF2 = 1), controls the output direction of Port A. CSADOUT2 must include the write-cycle control signals as part of its product term. When CSADOUT2 is active, the data presented on AD0/A0–AD7/A7 flows out of Port A. This chip-select can be placed on any boundary that is a function of one product term of the PAD inputs. See Figure 5.
PAD B Outputs	
$\overline{CS0}$–$\overline{CS3}$	These chip-select outputs can be routed through Port B. Each of them is a function of up to four product terms of the PAD inputs.
$\overline{CS4}$–$\overline{CS7}$	These chip-select outputs can be routed through Port B. Each of them is a function of up to two product terms of the PAD inputs.
$\overline{CS8}$–$\overline{CS10}$	These chip-select outputs can be routed through Port C. See Figure 3, Note 4. Each of them is a function of one product term of the PAD inputs.

Configuration Bits

The configuration bits shown in Table 4 are non-volatile cells that let the user set the device, I/O, and control functions to the proper operational mode. Table 5 lists all configuration bits. The configuration bits are programmed and verified during the programming phase. In operational mode, they are not accessible. To simplify implementing a specific mode, use the PSD3XX MAPLE software to set the bits.

Table 4. PSD3XX Non-Volatile Configuration Bits

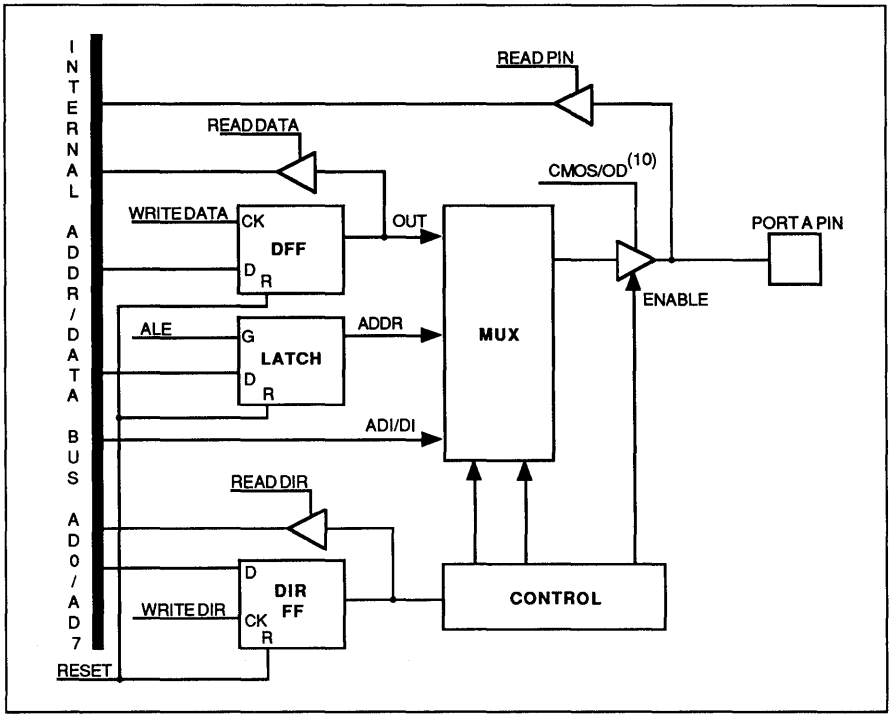
Use This Bit	To
CDATA	Set the data bus width to 8 or 16 bits (PSD30X only).
CADDRDAT	Set the address/data buses to multiplexed or non-multiplexed mode.
CEDS	Determine the polarity and functionality of read and write. (Note 9)
CA19/$\overline{CSI}$	Set A19/$\overline{CSI}$ to $\overline{CSI}$ (power-down) or A19 input.
CALE	Set the ALE polarity.
CPAF2	Set Port A either to track the low-order byte of the address/data multiplexed bus or to select the I/O or address option.
CSECURITY	Set the security on or off (a secured part can not be duplicated).
CRESET	Set the RESET polarity.
$\overline{COMB}$/SEP	Set $\overline{PSEN}$ and $\overline{RD}$ for combined or separate address spaces (see Figures 9 and 10).
CPAF1 (8 Bits)	Configure each pin of Port A in multiplexed mode to be an I/O or address out.
CPACOD (8 Bits)	Configure each pin of Port A as an open drain or active CMOS pull-up output.
CPBF (8 Bits)	Configure each pin of Port B as an I/O or a chip-select output.
CPBCOD (8 Bits)	Configure each pin of Port B as an open drain or active CMOS pull-up output.
CPCF (3 Bits)	Configure each pin of Port C as an address input or a chip-select output.
CADDHLT	Configure pins A16 – A19 to go through a latch or to have their latch transparent.
CADLOG (4 Bits)	Configure A16 – A19 individually as logic or address inputs. (Note 9)
CATD	Configure pins A16–A19 as PAD logic inputs or high-order address inputs (Note 8).
CLOT	Determine in non-multiplexed mode if address inputs are transparent or latched (Note 9).
CRRWR	Set the $\overline{RD}$/E and $\overline{WR}$/V_{PP} or R/$\overline{W}$ pins to $\overline{RD}$ and $\overline{WR}$ pulse, or to E strobe and R/W status (Note 8).
CRRWR	Configure the polarity and control methods of read and write cycles. (Note 9)
CMISER	Controls the lower-power mode.

NOTES: 8. PSD31X only. 9. PSD302/312/303/313 only.

Port Functions

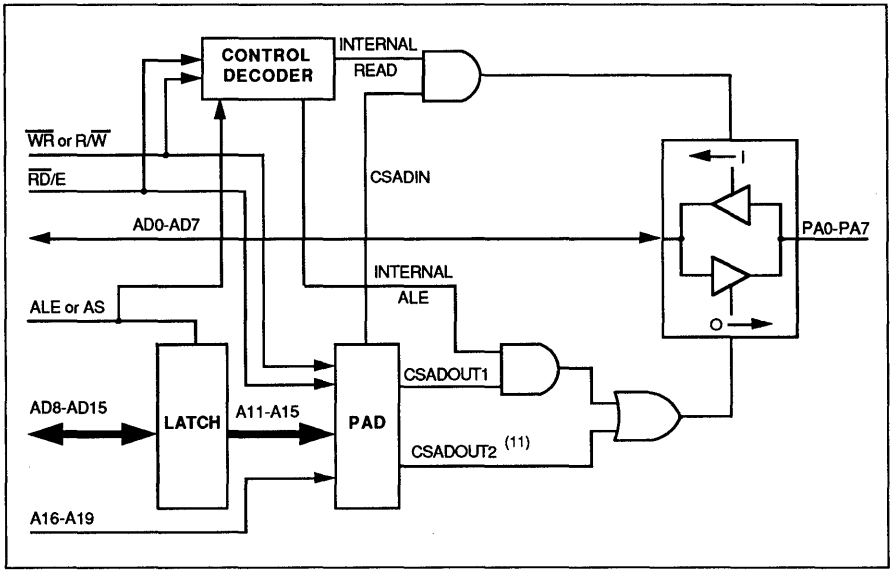
The PSD3XX has three I/O ports (Ports A, B, and C) that are configurable at the bit level. This permits great flexibility and a high degree of customization for specific applications. The following is a description of each port. Figure 4 shows the pin structure of Port A.

Figure 4. Port A Pin Structure



NOTE: 10. CMOS/OD determines whether the output is open drain or CMOS.

Figure 5. Port A Track Mode



NOTE: 11. The expression for CSADOUT2 must include the following write operation cycle signals:
For CRRWR = 0, CSADOUT2 must include $\overline{WR}$ = 0.
For CRRWR = 1, CSADOUT2 must include E = 1 and R/$\overline{W}$ = 0.

Table 5. PSD3XX Configuration Bits[12,13]

Configuration Bits	No. of Bits	Function
CDATA (Note 14)	1	8-bit or 16-bit Data Bus Width CDATA = 0 eight bits CDATA = 1 sixteen bits
CADDRDAT	1	ADDRESS/DATA Multiplexed (separate buses) CADDRDAT = 0, non-multiplexed CADDRDAT = 1, multiplexed
CA19/$\overline{CSI}$	1	A19 or $\overline{CSI}$ CA19/$\overline{CSI}$ = 0, enable power-down CA19/$\overline{CSI}$ = 1, enable A19 input to PAD
CALE	1	Active HIGH or Active LOW CALE = 0, Active high CALE = 1, Active low
CRESET	1	Active high or active low CRESET = 0, active low reset signal CRESET = 1, active high reset signal
$\overline{COMB}$/SEP	1	Combined or Separate Address Space for SRAM and EPROM 0 = Combined, 1 = Separate
CPAF1	8	Port A I/Os or A0–A7 CPAF1 = 0, Port A pin = I/O CPAF1 = 1, Port A pin = A0 – A7
CPAF2	1	Port A AD0–AD7 (address/data multiplexed bus) CPAF2 = 0, address or I/O on Port A (according to CPAF1) CPAF2 = 1, address/data multiplexed on Port A (track mode)
CATD (Note 16)	1	A16–A19 address or logic inputs CATD = 0, logic inputs CATD = 1, address inputs
CADDHLT	1	A16–A19 Transparent or Latched CADDHLT = 0, Address latch transparent CADDHLT = 1, Address latched (ALE dependent)
CSECURITY	1	SECURITY On/Off CSECURITY = 0, off CSECURITY = 1, on
CLOT (Note 15)	1	A0–A15 Address Inputs are transparent or ALE-dependent in non-multiplexed modes CLOT = 0, transparent CLOT = 1, ALE-dependent
CRRWR CEDS (Note 15)	2	Determine the polarity and control methods of read and write cycles. CEDS CRRWR 0 0 $\overline{RD}$ and $\overline{WR}$ active low pulses 0 1 R/$\overline{W}$ status and high E pulse 1 1 R/$\overline{W}$ status and low $\overline{DS}$ pulse
CRRWR (Note 16)	1	CRRWR = 0, $\overline{RD}$ and $\overline{WR}$ active low strobes CRRWR = 1, R/$\overline{W}$ status and E active high pulse
CPACOD	8	Port A CMOS or Open Drain Output CPACOD = 0, CMOS output CPACOD = 1, open-drain output

Table 5. PSD3XX Configuration Bits (Cont.)

Configuration Bits	No. of Bits	Function
CPBF	8	Port B is I/O or $\overline{CS0}$– $\overline{CS7}$ CPBF = 0, Port B pin is CS0 – $\overline{CS7}$ CPBF = 1, Port B pin is I/O
CPBCOD	8	Port B CMOS or Open Drain CPBCOD = 0, CMOS output CPBCOD = 1, open-drain output
CPCF	3	Port C A16–A18 or $\overline{CS8}$–$\overline{CS10}$ CPCF = 0, Port C pin is A16–A18 CPCF = 1, Port C pin is $\overline{CS8}$–$\overline{CS10}$
CADLOG (Note 15)	4	Port C: A16–A19 Address or Logic Input CADLOG = 0, Port C pin or A19/$\overline{CSI}$ is logic input CADLOG = 1, Port C pin or A19/$\overline{CSI}$ is address input
CMISER	1	Default: CMISER = 0 CMISER = 1, lower-power mode

NOTES: 12. The Maple software will guide the user to the proper configuration choice.
13. In an unprogrammed or erased part, all configuration bits are 0.
14. PSD30X only.
15. PSD3X2/3X3 only.
16. PSD3X1 only.

Port Functions (Cont.)

Port A in Multiplexed Address/Data Mode

The default configuration of Port A is I/O. In this mode, every pin can be set as an input or output by writing into the respective pin's direction flip flop (DIR FF, in Figure 4). As an output, the pin level can be controlled by writing into the respective pin's data flip flop (DFF, in Figure 4). When DIR FF = 1, the pin is configured as an output. When DIR FF = 0, the pin is configured as an input. The controller can read the DIR FF bits by accessing the READ DIR register; it can read the DFF bits by accessing the READ DATA register. Port A pin levels can be read by accessing the READ PIN register. Individual pins can be configured as CMOS or open drain outputs. Open drain pins require external pull-up resistors. For addressing information, refer to Tables 6 and 7.

Alternatively, each bit of Port A can be configured as a low-order latched address bus bit. The address is provided by the port address latch, which latches the address on the trailing edge of ALE. PA0–PA7 can become A0–A7, respectively. This feature enables the user generate low-order address bits to access external peripherals or memory that require several low-order address lines.

Another mode of Port A (CPAF2 = 1) sets the entire port to track the inputs AD0/A0–AD7/A7, depending on specific address ranges defined by the PAD's CSADIN, CSADOUT1, and CSADOUT2 signals. This feature lets the user interface the microcontroller to shared external resources without requiring external buffers and decoders. In this mode, the port is effectively a bi-directional buffer. The direction is controlled by using the input signals ALE, $\overline{RD}$/E or $\overline{RD}$/E/$\overline{DS}$, $\overline{WR}$/V_{PP} or R/$\overline{W}$, and the internal PAD outputs $\overline{CS}$ADOUT1, $\overline{CS}$ADOUT2 and CSADIN (see Figure 5). When CSADOUT1 and ALE are true, the address on the input AD0/A0–AD7/A7 pins is output through Port A. (Carefully check the generation of CSADOUT1, and ensure that it is stable during the ALE pulse. When CSADOUT2 is active, a write operation is performed (see note to Figure 5). The data on the input AD0/A0–AD7/A7 pins flows out through Port A. When CSADIN and a read operation is performed (depending on the mode of the $\overline{RD}$/E or $\overline{RD}$/E/$\overline{DS}$, and $\overline{WR}$/V_{PP} or R/$\overline{W}$ pins), the data on Port A flows out through the AD0/A0–AD7/A7 pins. In this operational mode, Port A is tri-stated when none of the above-mentioned three conditions exist.

Port Functions (Cont.)

Port A in Non-Multiplexed Address/Data Mode

In this mode, Port A becomes the low order data bus byte of the chip. When reading an internal location, data is presented on Port A pins. When writing to an internal location, data present on Port A pins is written to that location.

Port B in Multiplexed Address/Data and in 8-Bit Non-Multiplexed Modes

The default configuration of Port B is I/O. In this mode, every pin can be set as an input or output by writing into the respective pin's direction flip flop (DIR FF, in Figure 6). As an output, the pin level can be controlled by writing into the respective pin's data flip flop (DFF, in Figure 6). When DIR FF = 1, the pin is configured as an output. When DIR FF = 0, the pin is configured as an input. The controller can read the DIR FF bits by accessing the READ DIR register; it can read the DFF bits by accessing the READ DATA register. Port B pin levels can be read by accessing the READ PIN register. Individual pins can be configured as CMOS or open drain outputs. Open drain pins require external pull-up resistors. For addressing information, refer to Tables 6 and 7.

Alternately, each bit of Port B can be configured to provide a chip-select output signal from PAD B. PB0–PB7 can provide $\overline{CS0}$–$\overline{CS7}$, respectively. Each of the signals $\overline{CS0}$–$\overline{CS3}$ is comprised of four product terms.Thus, up to four ANDed expressions can be ORed while deriving any of these signals. Each of the signals $\overline{CS4}$–$\overline{CS7}$ is comprised of two product terms. Thus, up to two ANDed expressions can be ORed while deriving any of these signals.

Port B in 16-Bit Non-Multiplexed Address/Data Mode (PSD30X)

In this mode, Port B becomes the high-order data bus byte of the chip. When reading an internal high-order data bus byte location, the data is presented on Port B pins. When writing to an internal high-order data bus byte location, data present on Port B is written to that location. See Table 9.

Accessing the I/O Port Registers

Tables 6 and 7 show the offset values with the respect to the base address defined by the CSIOPORT. They let the user access the corresponding registers.

Port C in All Modes

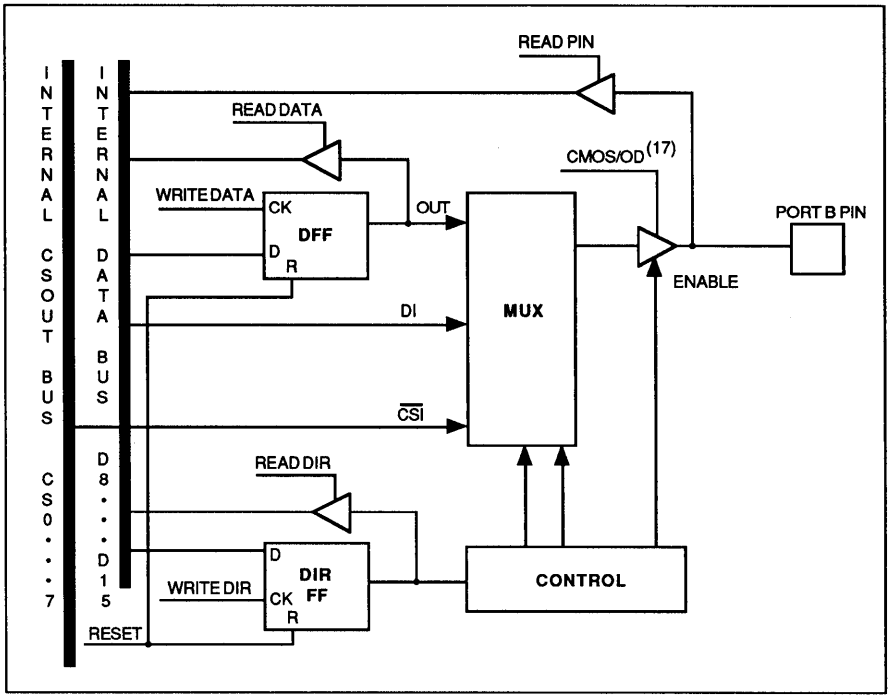
Each pin of Port C (shown in Figure 7) can be configured as an input to PAD A and PAD B or output from PAD B. As inputs, the pins are named A16–A18. Although the pins are given names of the high-order address bus, they can be used for any other address lines or logic inputs to PAD A and PAD B. For example, A8–A10 can also be connected to those pins, improving the boundaries of $\overline{CS0}$–$\overline{CS7}$ resolution to 256 bytes. As inputs, they can be individually configured to be logic or address inputs. A logic input uses the PAD only for Boolean equations that are implemented in any or all of the $\overline{CS0}$–$\overline{CS10}$ PAD B outputs. Port C addresses can be programmed to latch the inputs by the trailing edge ALE or to be transparent.

Alternately, PC0–PC2 can become $\overline{CS8}$–$\overline{CS10}$ outputs, respectively, providing the user with more external chip-select PAD outputs. Each of the signals $\overline{CS8}$–$\overline{CS10}$ is comprised of one product term.

ALE/AS and AD0/A0–AD15/A15 in Non-Multiplexed Modes

In non-multiplexed modes, AD0/A0–AD15/A15 are address inputs only and can become transparent (CLOT = 0) or ALE dependent (CLOT = 1). In transparent mode, the ALE/AS pin can be used as an additional logic input to the PADs. The non-multiplexed ALE dependent mode is useful in applications for which the host processor has a multiplex address/data bus and AD0/A0–AD7/A7 are not multiplexed with A0–A7 but rather are multiplexed with other address lines. In these applications, Port A serves as a data bus and each of its pins can be directly connected to the corresponding host's multiplexed pin, where that data bit is expected.
(See Table 8.)

Figure 6. Port B Pin Structure



NOTE: 17. CMOS/OD determines whether the output is open drain or CMOS.

Table 6. I/O Port Addresses in an 8-bit Data Bus Mode

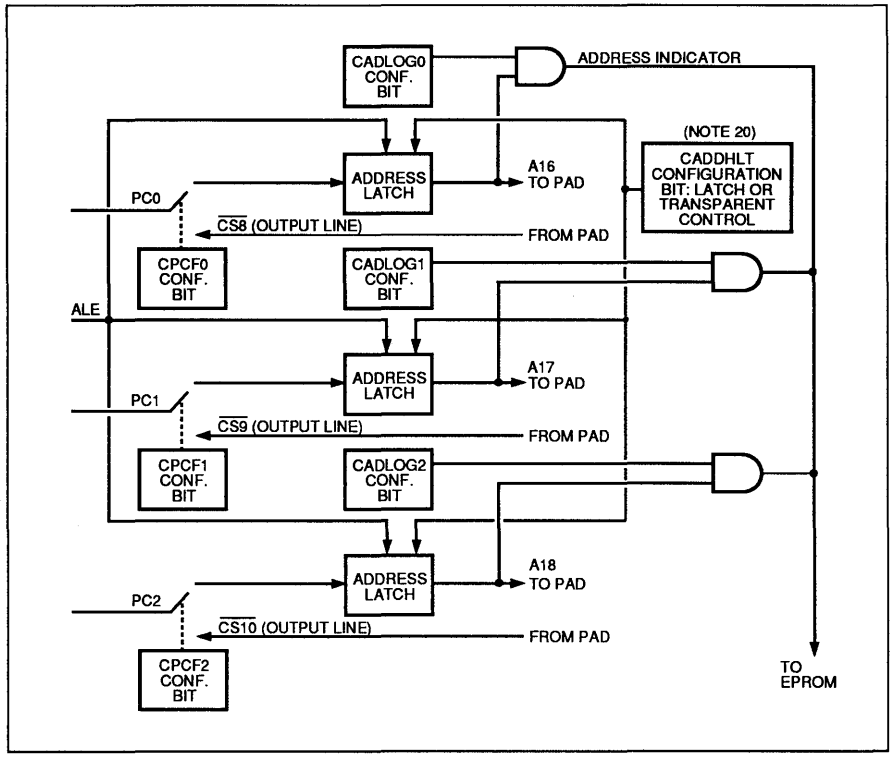
Register Name	Byte Size Access of the I/O Port Registers Offset from the CSIOPORT
Pin Register of Port A	+ 2 (accessible during read operation only)
Direction Register of Port A	+ 4
Data Register of Port A	+ 6
Pin Register of Port B	+ 3 (accessible during read operation only)
Direction Register of Port B	+ 5
Data Register of Port B	+ 7
Page Register	+18

Table 7. I/O Port Addresses in a 16-bit Data Bus Mode[18,19] (PSD30X)

Register Name	Word Size Access of the I/O Port Registers Offset from the CSIOPORT
Pin Register of Ports B and A	+ 2 (accessible during read operation only)
Direction Register of Ports B and A	+ 4
Data Register of Ports B and A	+ 6

NOTES: 18. When the data bus width is 16, Port B registers can only be accessed if the $\overline{BHE}$ signal is low.
19. I/O Ports A and B are still byte-addressable, as shown in Table 6. For I/O Port B register access, $\overline{BHE}$ must be low.

Figure 7. Port C Structure



NOTES: 20. The CADDHLT configuration bit determines if A18–A16 are transparent via the latch, or if they must be latched by the trailing edge of the ALE strobe.

21. PSD3X2/3X3: Individual pins can be configured independently as address or logic inputs (CADLOG, bits 0–2).
PSD3X1: All Port C pins are either address or logic inputs (CATD).

Port Functions (Cont.)

ALE/AS and AD0/A0–AD15/A15 in Non-Multiplexed Modes (PSD3X2/3X3)

In non-multiplexed modes, AD0/A0–AD15/A15 are address inputs only and can become transparent (CLOT = 0) or ALE dependent (CLOT = 1). In transparent mode, the ALE/AS pin can be used as an additional logic input to the PADs. The non-multiplexed ALE dependent mode is useful in applications for which the host processor has a multiplex address/data bus and AD0/A0–AD7/A7 are not multiplexed with A0–A7 but rather are multiplexed with other address lines. In these applications, Port A serves as a data bus and each of its pins can be directly connected to the corresponding host's multiplexed pin, where that data bit is expected. (See Table 8.)

ALE/AS and AD0/A0–AD7/A7 in Non-Multiplexed Modes (PSD31X)

In non-multiplexed modes, A0–A15 are address inputs only and can become transparent (CLOT = 0) or ALE dependent (CLOT = 1). In transparent mode, the ALE/AS pin can be used as an additional logic input to the PADs. The non-multiplexed ALE dependent mode is useful in applications for which the host processor has a multiplex address/data bus and AD0/A0–AD7/A7 are not multiplexed with A0–A7 but rather are multiplexed with other address lines. In these applications, Port A serves as a data bus and each of its pins can be directly connected to the corresponding host's multiplexed pin, where that data bit is expected. (See Table 8.)

A16–A19 Inputs

If one or more of the pins PC0, PC1 PC2 and $\overline{CSI}$/A19 are configured as inputs, the configuration bits CADDHLT and CATD define their functionality inside the part. CADDHLT determines if these inputs are to be latched by the trailing edge of the ALE or AS signal (CADDHLT = 1), or enabled into the PSD3XX at all times (CADDHLT = 0, transparent mode). CATD determines whether these lines are high-order address lines, that take part in the derivation of memory and I/O select signals inside the chip (CATD = 1), or logic input lines that have no impact on memory or I/O selections (CATD = 0). Logic input lines typically participate in the Boolean expressions implemented in the PAD.

EPROM

The EPROM has 8 banks of memory. Each bank can be placed in any address location by programming the PAD. Bank0–Bank7 is selected by PAD outputs ES0–ES7, respectively.

Device	EPROM Size	EPROM Architecture		EPROM Bank Architecture (8 ea)	
		x8	x16	x8	x16
PSD301	256Kb	32K x 8	16K x 16	4K x 8	2K x 16
PSD311	256Kb	32K x 8	–	4K x 8	–
PSD302	512Kb	64K x 8	32K x 16	8K x 8	4K x 16
PSD312	512Kb	64K x 8	–	8K x 8	–
PSD303	1Mb	128K x 8	64K x 16	16K x 8	8K x 16
PSD313	1Mb	128K x 8	–	16K x 8	–

SRAM

Each PSD3XX device has 16K bits of SRAM. Depending on the configuration of the data bus, the SRAM organization can be 2K x 8 (8-bit data bus) or 1K x 16 (16-bit data bus). The SRAM is selected by the RS0 output of the PAD.

Memory Paging (PSD3X2/3X3)

The page register consists of four flip-flops, which can be read from, or written to, through the I/O address space (CSIOPORT). The page register is connected to the D3–D0 lines. The Page Register address is CSIOPORT + 18H. The page register outputs are P3–P0, which are fed into the PAD. This enables the host microcontroller to enlarge its address space by a factor of 16 (there can be a maximum of 16 pages). See Figure 8.

Figure 8. Page Register (PSD3X2/3X3)

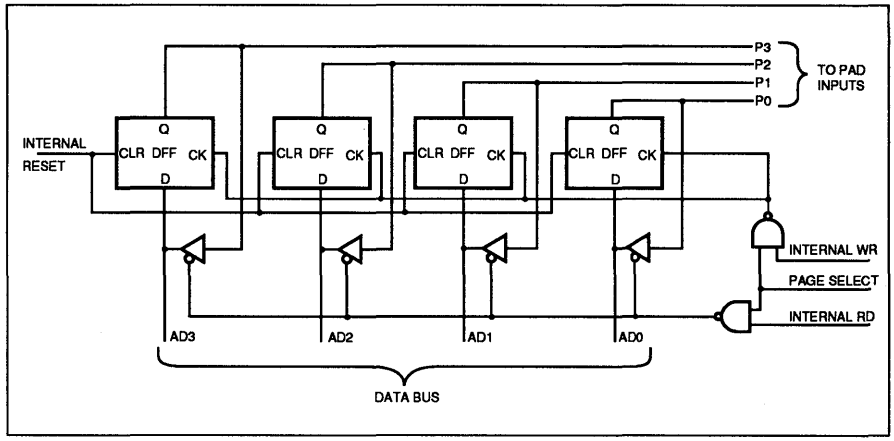


Table 8. Signal Latch Status in All Operating Modes

Signal Name	Configuration Bits	Configuration Mode	Signal Latch Status
AD8/A8–AD15/A15	CDATA , CADDRDAT, CLOT = 0	8-bit data, non-multiplexed	Transparent
	CDATA, CADDRDAT = 0, CLOT = 1		ALE Dependent
	CDATA = 1, CADDRDAT, CLOT = 0	16-bit data, non-multiplexed	Transparent
	CDATA = 1, CADDRDAT = 0, CLOT = 1		ALE Dependent
	CDATA = 0, CADDRDAT = 1	8-bit data, multiplexed	Transparent
	CDATA = 1, CADDRDAT = 1	16-bit data, multiplexed	ALE Dependent
AD0/A0-AD7/A7	CADDRDAT = 0, CLOT = 0	non-multiplexed modes	Transparent
	CADDRDAT = 0, CLOT = 1		ALE Dependent
	CADDRDAT = 1	multiplexed modes	ALE Dependent
$\overline{BHE}$/PSEN	CDATA = 0	8-bit data, $\overline{PSEN}$ is active	Transparent
	CDATA = 1, CADDRDAT = 0	16-bit data, non-multiplexed mode, $\overline{BHE}$ is active	Transparent
A19 and PC2–PC0	CDATA = 1, CADDRDAT = 1	16-bit data, multiplexed mode, $\overline{BHE}$ is active	ALE Dependent
	CADDHLT = 0	A16–A19 can become logic inputs	Transparent
	CADDHLT = 1	A16–A19 can become multiplexed address lines	ALE Dependent

Control Signals

The PSD3XX control signals are $\overline{WR}/V_{PP}$ or R/$\overline{W}$, $\overline{RD}$/E or $\overline{RD}$/E/$\overline{DS}$, ALE, $\overline{BHE}$/$\overline{PSEN}$ or $\overline{PSEN}$, $\overline{RESET}$, and A19/$\overline{CSI}$. Each of these signals can be configured to meet the output control signal requirements of various microcontrollers.

$\overline{WR}/V_{PP}$ or R/$\overline{W}$

In operational mode, this signal can be configured as $\overline{WR}$ or R/$\overline{W}$. As $\overline{WR}$, all write operations are activated by an active low signal on this pin. As R/$\overline{W}$, the pin operates with the E strobe of the $\overline{RD}$/E/$\overline{DS}$ or $\overline{RD}$/E pin. When R/$\overline{W}$ is high, an active high signal on the $\overline{RD}$/E/$\overline{DS}$ or $\overline{RD}$/E pin performs a read operation. When R/$\overline{W}$ is low, an active high signal on the $\overline{RD}$/E/$\overline{DS}$ or $\overline{RD}$/E pin performs a write operation.

$\overline{RD}$/E/$\overline{DS}$ (or $\overline{RD}$/E on PSD3X1)

In operational mode, this signal can be configured as $\overline{RD}$, E, or $\overline{DS}$. As $\overline{RD}$, all read operations are activated by an active low signal on this pin. As E, the pin operates with the R/$\overline{W}$ signal of the $\overline{WR}/V_{PP}$ or R/$\overline{W}$ pin. When R/$\overline{W}$ is high, an active high signal on the $\overline{RD}$/E/$\overline{DS}$ pin performs a read operation. When R/$\overline{W}$ is low, an active high signal on the $\overline{RD}$/E/$\overline{DS}$ pin performs a write operation.

As $\overline{DS}$, the pin functions with the R/$\overline{W}$ signal as an active low data strobe signal. As $\overline{DS}$, the R/$\overline{W}$ defines the mode of operation (Read or Write).

ALE or AS

ALE polarity is programmable. When programmed to be active high, a high on the pin causes the input address latches, Port A address latches, Port C, and A19 address latches to be transparent. The falling edge of ALE locks the information into the latches. When ALE is programmed to be active low, a low on the pin causes the input address latches, Port A address latches, Port C, and A19 address latches to be transparent. The rising edge of ALE locks the appropriate information into the latches.

$\overline{BHE}$/$\overline{PSEN}$

This pin's function depends on the PSD3XX data bus width. If it is 8 bits, the pin is $\overline{PSEN}$; if it is 16 bits, the pin is $\overline{BHE}$. In 8-bit mode, the $\overline{PSEN}$ function enables the user to work with two address spaces: program memory and data memory (if COMB/SEP = 1). In this mode, an active low signal on the PSEN pin causes the EPROM to be read if selected. The SRAM and I/O ports read operation are done by $\overline{RD}$ low (CRRWR = 0), or by E high and R/$\overline{W}$ high (CRRWR = 1, CEDS = 0) or by $\overline{DS}$ low and R/$\overline{W}$ high (CRRWR, CEDS = 1).

Whenever a member of the 8031 family (or any other similar microcontroller) is used, the $\overline{PSEN}$ pin must be connected to the $\overline{PSEN}$ pin of the microcontroller.

If COMB/SEP = 0, the address spaces of the program and the data are combined. In this configuration (except for the 8031-type case mentioned above), the $\overline{PSEN}$ pin must be tied high to V_{CC}, and the EPROM, SRAM, and I/O ports are read by $\overline{RD}$ low (CRRWR = 0), or by E high and R/$\overline{W}$ high (CRRWR = 1, CEDS = 0) or by $\overline{DS}$ low and R/$\overline{W}$ high (CRRWR, CEDS = 1). See Figures 9 and 10.

In $\overline{BHE}$ mode, this pin enables accessing of the upper-half byte of the data bus. A low on this pin enables a write or read operation to be performed on the upper half of the data bus (see Table 9).

RESET

This is an asynchronous input pin that clears and initializes the PSD3XX. Reset polarity is programmable (active low or active high). Whenever the PSD3XX reset input is driven active for at least 100 ns, the chip is reset. The PSD3XX must be reset before it can be used. Tables 10a, 10b and 11 indicate the state of the part during and after reset.

Control Signals (Cont.)

A19/$\overline{CSI}$

When configured as $\overline{CSI}$, a high on this pin deselects, and powers down, the chip. A low on this pin puts the chip in normal operational mode. For PSD3XX states during the power-down mode, see Tables 12 and 13, and Figure 11.

In A19 mode, the pin is an additional input to the PAD. It can be used as an address line (CADLOG3 = 1) or as a general-purpose logic input (CADLOG3 = 0). A19 can be configured as ALE dependent or as transparent input (see Table 8). In this mode, the chip is always enabled.

Figure 9. Combined Address Space

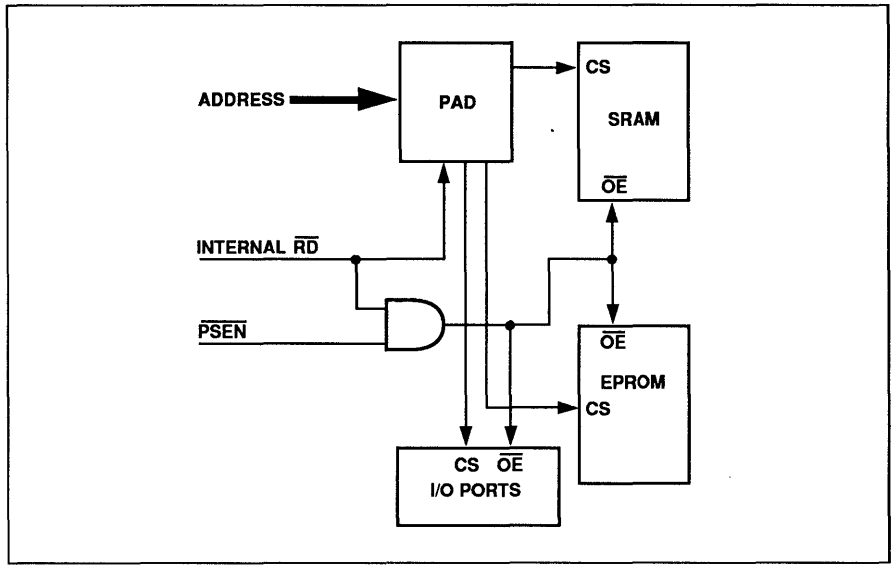


Table 9. High/Low Byte Selection Truth Table (in 16-Bit Configuration Only)

$\overline{BHE}$	A_0	Operation
0	0	Whole Word
0	1	Upper Byte From/To Odd Address
1	0	Lower Byte From/To Even Address
1	1	None

Figure 10. 8031-Type Separate Code and Data Address Spaces

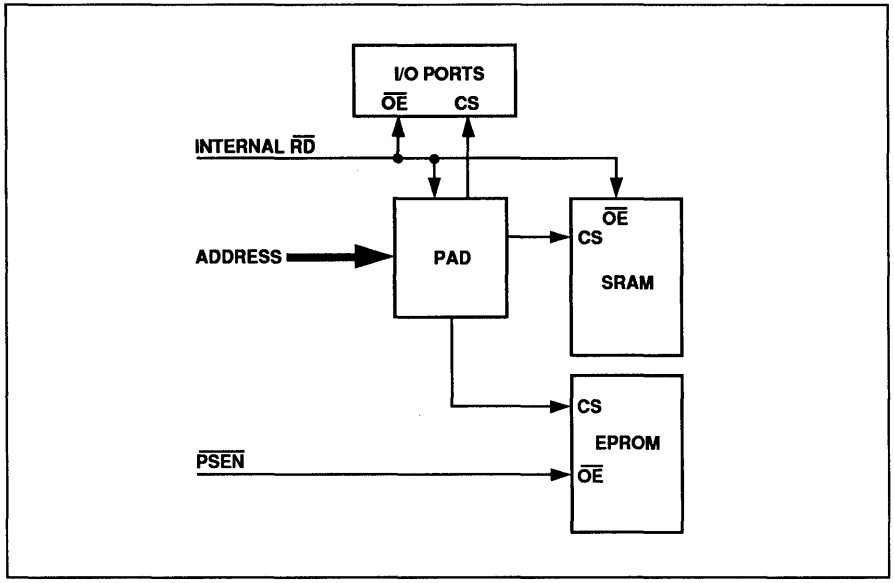


Table 10a. Signal States During Reset Cycle (RESET)

Signal	Condition
AD0/A0–AD15/A15	Input
PA0–PA7 (Port A)	Input
PB0–PB7 (Port B)	Input
PC0–PC2 (Port C)	Input

Table 10b. Signal States After Reset Cycle (RESET)

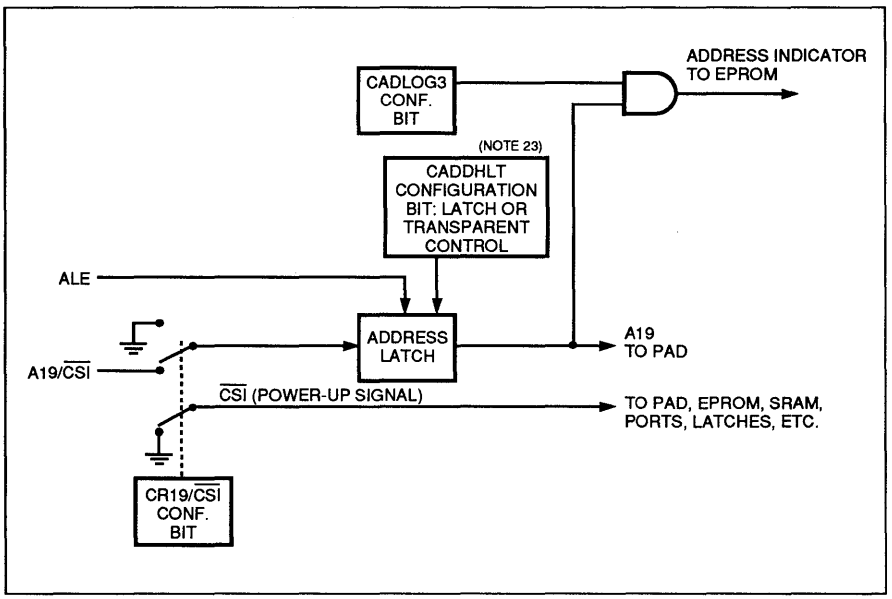
Signal	Configuration Mode	Condition
AD0/A0–AD7/A7	All	Input
A8–A15	All	Input
PA0–PA7) (Port A	I/O Tracking AD0/A0–AD7 Address outputs A0–A7	Input Input Low
PB0–PB7 (Port B)	I/O $\overline{CS7}$–$\overline{CS0}$ CMOS outputs $\overline{CS7}$–$\overline{CS0}$ open drain outputs	Input High Tri-stated
PC0–PC2 (Port C)	Address inputs A16–A18 $\overline{CS8}$–$\overline{CS10}$ CMOS outputs	Input High

Table 11. Internal States During and After Reset Cycle

Component	Signals	Contents
PAD	$\overline{CS0}$–$\overline{CS10}$	All = 1 (Note 22)
	CSADIN, CSADOUT1, CSADOUT2, CSIOPORT, RS0, ES0 – ES7	All = 0 (Note 22)
Data register A	n/a	0
Direction register A	n/a	0
Data register B	n/a	0
Direction register B	n/a	0

NOTE: 22. All PAD outputs are in a non-active state.

Figure 11. A19/$\overline{CSI}$ Cell Structure



NOTES: 23. The CADDHLT configuration bit determines if A19–A16 are transparent via the latch, or if they must be latched by the trailing edge of the ALE strobe.

Table 12a. Signal States During Power-Down Mode (PSD30X)

Signal	Configuration Mode	Condition
AD0/A0–AD15/A15	All	Input
PA0–PA7	I/O Tracking AD0/A0–AD7/A7 Address outputs A0–A7	Unchanged Input All 1's
PB0–PB7	I/O $\overline{CS0}$–$\overline{CS7}$ CMOS outputs $\overline{CS0}$–$\overline{CS7}$ open drain outputs	Unchanged All 1's Tri-stated
PC0–PC2	Address inputs A18–A16 $\overline{CS8}$–$\overline{CS10}$ CMOS outputs	Input All 1's

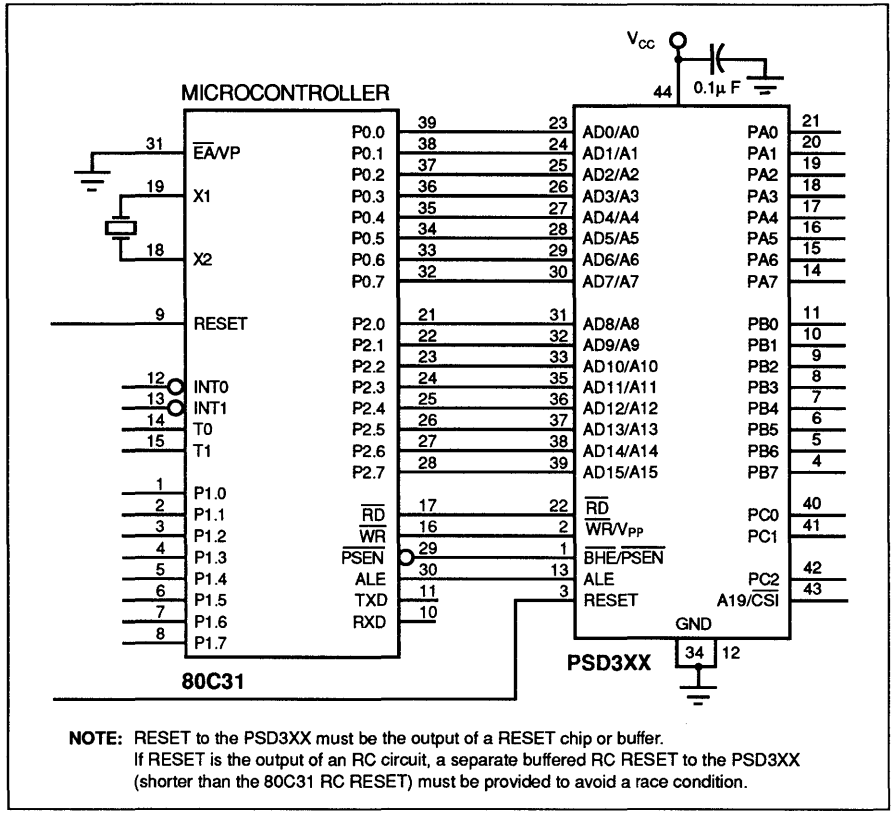
Table 12b. Signal States During Power-Down Mode (PSD31X)

Signal	Configuration Mode	Condition
AD0/A0–AD7/A7	All	Input
A8–A15	All	Input
PA0–PA7	I/O Tracking AD0/A0–AD7/A7 Address outputs A0–A7	Unchanged Input All 1's
PB0–PB7	I/O $\overline{CS0}$–$\overline{CS7}$ CMOS outputs CS0–CS7 open drain outputs	Unchanged All 1's Tri-stated
PC0–PC2	Address inputs A18–A16 $\overline{CS8}$–$\overline{CS10}$ CMOS outputs	Input All 1's

Table 13. Internal States During Power-Down

Component	Signals	Contents
PAD	$\overline{CS0}$–$\overline{CS10}$	All 1's (deselected)
	CSADIN, CSADOUT1, CSADOUT2, CSIOPORT, RS0, ES0–ES7	All 0's (deselected)
Data register A Direction register A Data register B Direction register B	n/a n/a n/a n/a	All unchanged

Figure 12. PSD3XX Interface With Intel's 80C31



NOTE: RESET to the PSD3XX must be the output of a RESET chip or buffer. If RESET is the output of an RC circuit, a separate buffered RC RESET to the PSD3XX (shorter than the 80C31 RC RESET) must be provided to avoid a race condition.

The configuration bits for Figure 12 are:

CALE	0	COMB/SEP	0 or 1 (both valid)
CDATA	0	CRRWR	0
CADDRDAT	1	CEDS	0
CRESET	1		

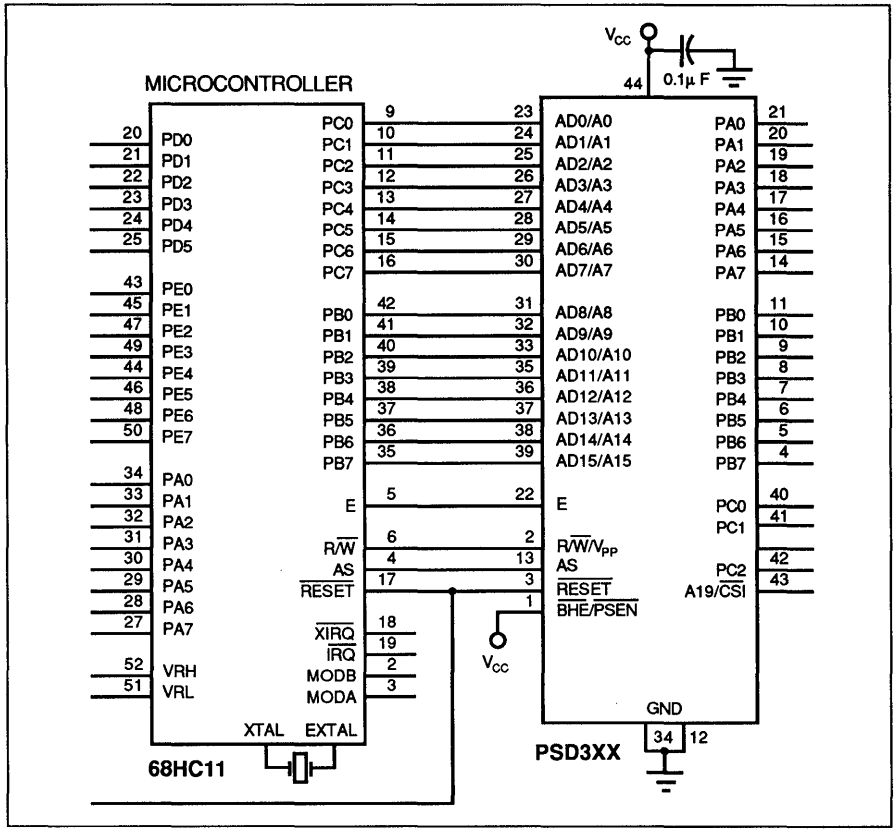
All other configuration bits may vary according to the application requirements.

System Applications

In Figure 12, the PSD3XX is configured to interface with Intel's 80C31, which is a 16-bit address/8-bit data bus microcontroller. Its data bus is multiplexed with the low-order address byte. The 80C31 uses signals $\overline{RD}$ to read from data memory and $\overline{PSEN}$ to read from code memory. It uses $\overline{WR}$ to write into the data memory. It also uses active high reset and ALE signals. The rest of the configuration bits as well as the unconnected signals (not shown) are application specific and, thus, user dependent.

In Figure 13, the PSD3XX is configured to interface with Motorola's 68HC11, which is a 16-bit address/8-bit data bus microcontroller. Its data bus is multiplexed with the low-order address byte. The 68HC11 uses E and R/W signals to derive the read and write strobes. It uses the term AS (address strobe) for the address latch pulse. RESET is an active low signal. The rest of the configuration bits as well as the unconnected signals (not shown) are specific and, thus, user dependent.

Figure 13. PSD3XX Interface With Motorola's 68HC11



The configuration bits for Figure 13 are:

CALE	0	COMB/SEP	0
CDATA	0	CRRWR	1
CADDRDAT	1	CEDS	0
CRESET	0		

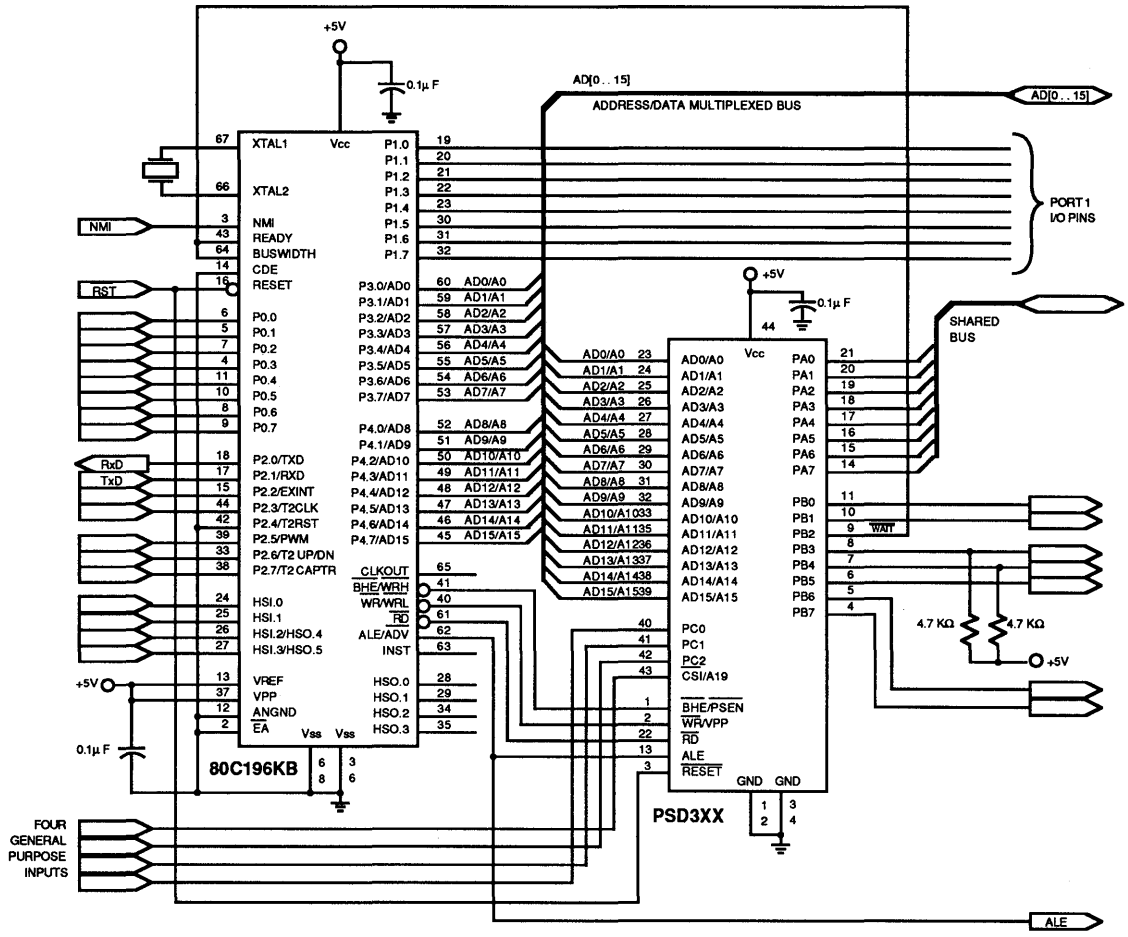
All other configuration bits may vary according to the application requirements.

System Applications (Cont.)

In Figure 14, the PSD3XX is configured to work directly with Intel's 80C196KB microcontroller, which is a 16-bit address/16-bit data bus processor. Address and data lines multiplexed. In the example shown, all configuration bits are set. The PSD3XX is configured to use PC0, PC1, PC2, and $\overline{CSI}$/A19 as A16, A17, A18, and A19 inputs, respectively. These signals are independent of the ALE pulse (latch-transparent). They are used as four general-purpose logic inputs that take part in the PAD equations implementation.

Port A is configured to work in the special track mode, in which (for certain conditions) PA0–PA7 tracks lines AD0/A0–AD7/A7. Port B is configured to generate $\overline{CS0}$–$\overline{CS7}$. In this example, PB2 serves as a $\overline{WAIT}$ signal that slows down the 80C196KB during the access of external peripherals. These 8-bit wide peripherals are connected to the shared bus of Port A. The $\overline{WAIT}$ signal also drives the buswidth input of the microcontroller, so that every external peripheral cycle becomes an 8-bit data bus cycle. PB3 and PB4 are open-drain output signals; thus, they are pulled up externally.

Figure 14.
PSD3XX Interface With Intel's 80C196KB.



The configuration bits for Figure 14 are:

CALE	0	CSECURITY	Don't care
CDATA	1	CPCF2, CPCF1, CPCF0	0, 0, 0
CADDRDAT	1	CPACOD7–CPACOD0	00H
CPAF1	Don't care	CPBF7–CPBF0	00H
CPAF2	1	CPBCOD7–CPBCOD0	18H
CA19/$\overline{CSI}$	1	CEDS	0
CRRWR	0	CADLOG3—CADLOG0	0H
COMB/SEP	0		
CADDHLT	0		
CRESET	0		

Field-programmable microcontroller peripheral — PSD301

Key Features

- Single Chip Programmable Peripheral for Microcontroller-based Applications

- 19 Individually Configurable I/O pins that can be used as:
  - Microcontroller I/O port expansion
  - Programmable Address Decoder (PAD) I/O
  - Latched address output
  - Open drain or CMOS

- Two Programmable Arrays (PAD A and PAD B)
  - Total of 40 Product Terms and up to 16 Inputs and 24 Outputs
  - Address Decoding up to 1 MB
  - Logic replacement

- "No Glue" Microcontroller Chip-Set
  - Built-in address latches for multiplexed address/data bus
  - Non-multiplexed address/data bus mode
  - Selectable 8 or 16 bit data bus width
  - ALE and Reset polarity programmable
  - Selectable modes for read and write control bus as $\overline{RD}/\overline{WR}$ or R/$\overline{W}$/E
  - $\overline{BHE}$ pin for byte select in 16-bit mode
  - $\overline{PSEN}$ pin for 8051 users

- 256 Kbits of UV EPROM
  - Configurable as 32K x 8 or as 16K x 16
  - Divides into 8 equal mappable blocks for optimized mapping
  - Block resolution is 4K x 8 or 2K x 16
  - 120 ns EPROM access time, including input latches and PAD address decoding.

- 16 Kbit Static RAM
  - Configurable as 2K x 8 or as 1K x 16
  - 120 ns SRAM access time, including input latches and PAD address decoding

- Address/Data Track Mode
  - Enables easy Interface to Shared Resources (e.g., Mail Box SRAM) with other Microcontrollers or a Host Processor

- Built-In Security
  - Locks the PSD301 and PAD Decoding Configuration

- Available in a Choice of Packages
  - 44 Pin PLCC and CLCC
  - 52 Pin PQFP

- Simple Menu-Driven Software: Configure the PSD301 on an IBM PC

- Pin Compatible with the PSD3XX and PSD3XXL Family

Security Mode

Security Mode in the PSD3XX locks the contents of the PAD A , PAD B and all the configuration bits. The EPROM, SRAM, and I/O contents can be accessed only through the PAD. The Security Mode can be set by the MAPLE or Programming software. In window packages, the mode is erasable through UV full part erasure. In the security mode, the PSD3XX contents cannot be copied on a programmer.

CMiser-Bit

The CMiser-Bit provides a programmable option for power-sensitive applications that require further reduction in power consumption. The CMiser-Bit (CMiser = 1) in the Maple portion of the PSD3XX sytem development software can be used to reduce power consumption. The CMiser-Bit turns off the EPROM blocks in the PSD3XX whenever the EPROM is not accessed, thereby reducing the active current consumed by the PSD3XX.

In the default mode, or if the PSD3XX is configured without programming the CMiser-Bit (CMiser = 0), the device operates at specified speed and power rating as specified in the A.C. and D.C. Characteristics.

However, if the CMiser-Bit is programmed (CMiser = 1), the device consumes even lower current, and is reflected in the data sheet. This mode has an adder in propagation delay in T5, T6, and T7 parameters in the A.C. Characteristics, and should be added to compute worst-case timing requirements in the application.

Absolute Maximum Ratings[1]

Symbol	Parameter	Condition	Min	Max	Unit
T_{STG}	Storage Temperature	CERDIP	– 65	+ 150	°C
		PLASTIC	– 65	+ 125	°C
	Voltage on any Pin	With Respect to GND	– 0.6	+ 7	V
V_{PP}	Programming Supply Voltage	With Respect to GND	– 0.6	+ 14	V
V_{CC}	Supply Voltage	With Respect to GND	– 0.6	+ 7	V
	ESD Protection			>2000	V

NOTE: 1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at theses or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods of time may affect device reliability.

Operating Range

Range	Temperature	V_{CC}	V_{CC} Tolerance		
			-12	-15	-20
Commercial	0° C to +70°C	+ 5 V	± 10%	± 10%	± 10%
Industrial	–40° C to +80°C	+ 5 V		± 10%	± 10%
Military	–55° C to +125°C	+ 5 V			± 10%

Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	Supply Voltage	All Speeds	4.5	5	5.5	V
V_{IH}	High-level Input Voltage	V_{CC} = 4.5 V to 5.5 V	2			V
V_{IL}	Low-level Input Voltage	V_{CC} = 4.5 V to 5.5 V	0		0.8	V

DC Characteristics

Symbol	Parameter	Conditions				CMiser = 1 Subtract:			Unit
			Min	Typ	Max	Min	Typ	Max	
V_{OL}	Output Low Voltage	I_{OL} = 20 µA V_{CC} = 4.5 V		0.01	0.1				V
		I_{OL} = 8 mA V_{CC} = 4.5 V		0.15	0.45				V
V_{OH}	Output High Voltage	I_{OH} = –20 µA V_{CC} = 4.5 V	4.4	4.49					V
		I_{OH} = –2 mA V_{CC} = 4.5 V	2.4	3.9					V
I_{SB1}	V_{CC} Standby Current (CMOS) (Notes 2 and 4)	Comm'l		50	100				µA
		Ind/Mil		75	150				µA
I_{CC1}	Active Current (CMOS) (No Internal Memory Block Selected) (Notes 2 and 5)	Comm'l (Note 6)		16	35		7	10	mA
		Comm'l (Note 7)		28	50		7	10	mA
		Ind/Mil (Note 6)		16	45		7	10	mA
		Ind/Mil (Note 7)		28	60		7	10	mA
I_{CC2}	Active Current (CMOS) (EPROM Block Selected) (Notes 2 and 5)	Comm'l (Note 6)		16	35		0	0	mA
		Comm'l (Note 7)		28	50		0	0	mA
		Ind/Mil (Note 6)		16	45		0	0	mA
		Ind/Mil (Note 7)		28	60		0	0	mA
I_{CC3}	Active Current (CMOS) (SRAM Block Selected (Notes 2 and 5)	Comm'l (Note 6)		47	80		7	10	mA
		Comm'l (Note 7)		59	95		7	10	mA
		Ind/Mil (Note 6)		47	100		7	10	mA
		Ind/Mil (Note 7)		59	115		7	10	mA
I_{LI}	Input Leakage Current	V_{IN} = 5.5 V or GND	–1	±0.1	1				µA
I_{LO}	Output Leakage Current	V_{OUT} = 5.5 V or GND	–10	±5	10				µA

NOTES: 2. CMOS inputs: GND ± 0.3 V or V_{CC} ± 0.3V.
3. TTL inputs: $V_{IL} \leq 0.8$ V, $V_{IH} \geq 2.0$ V.
4. $\overline{CSI}$/A19 is high and the part is in a power-down configuration mode.
5. Add 3.0 mA/MHz for AC power component (power = AC + DC).
6. Ten (10) PAD product terms active. (Add 380 µA per product term, typical, or 480 µA per product term maximum
7. Forty-one (41) PAD product terms active.

AC Characteristics

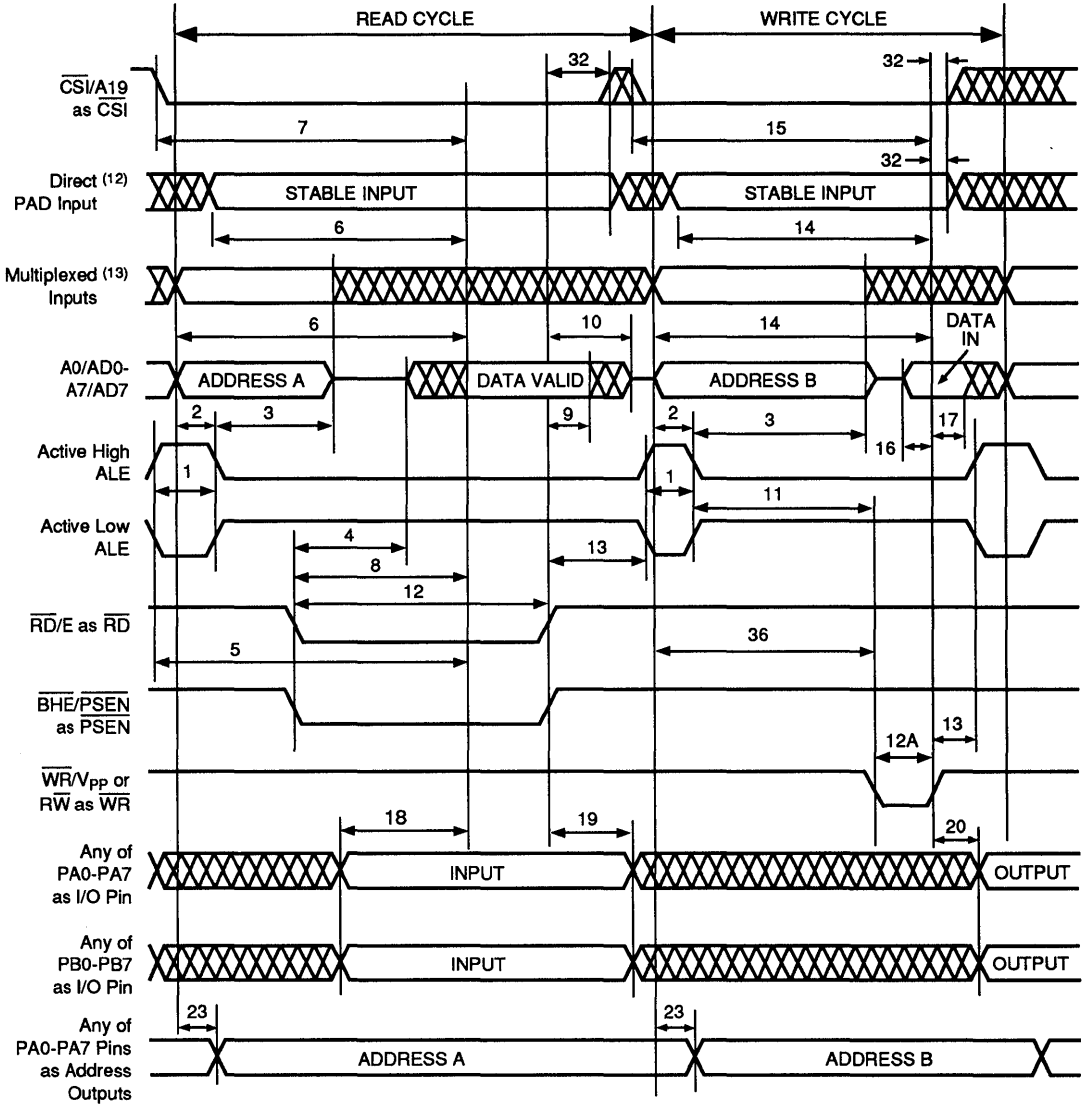
Symbol	Parameter	-90		-12		-15		-20		CMiser = 1 Add:	Unit
		Min	Max	Min	Max	Min	Max	Min	Max		
T1	ALE or AS Pulse Width	20		30		40		50		0	ns
T2	Address Set-up Time	5		9		12		15		0	ns
T3	Address Hold Time	8		13		15		25		0	ns
T4	Leading Edge of Read to Data Active	0		0		0		0		0	ns
T5	ALE Valid to Data Valid		100		140		170		200	10	ns
T6	Address Valid to Data Valid		90		120		150		200	10	ns
T7	$\overline{CSI}$ Active to Data Valid		100		150		160		200	15	ns
T8	Leading Edge of Read to Data Valid		32		38		55		60	0	ns
T9	Read Data Hold Time	0		0		0		0		0	ns
T10	Trailing Edge of Read to Data High-Z		35		35		40		45	0	ns
T11	Trailing Edge of ALE or AS to Leading Edge of Write	0		0		0		0		0	ns
T12	$\overline{RD}$, E, $\overline{PSEN}$, or $\overline{DS}$ Pulse Width	40		45		60		75		0	ns
T12A	$\overline{WR}$ Pulse Width	20		25		35		45		0	ns
T13	Trailing Edge of Write or Read to Leading Edge of ALE or AS	0		0		0		0		0	ns
T14	Address Valid to Trailing Edge of Write	90		120		150		200		0	ns
T15	$\overline{CSI}$ Active to Trailing Edge of Write	100		130		160		200		0	ns
T16	Write Data Set-up Time	20		25		30		40		0	ns
T17	Write Data Hold Time	5		5		10		15		0	ns
T18	Port to Data Out Valid Propagation Delay		30		30		35		45	0	ns
T19	Port Input Hold Time	0		0		0		0		0	ns
T20	Trailing Edge of Write to Port Output Valid	40		40		50		60		0	ns
T21	ADi or Control to $\overline{CSOi}$ Valid	6	25	6	30	6	35	5	45	0	ns
T22	ADi or Control to $\overline{CSOi}$ Invalid	5	25	5	30	4	35	4	45	0	ns

AC Characteristics (Cont.)

Symbol	Parameter	-90		-12		-15		-20		CMiser = 1 Add:	Unit
		Min	Max	Min	Max	Min	Max	Min	Max		
T23	Track Mode Address Propagation Delay: CSADOUT1 Already True		22		22		22		28	0	ns
T23A	Track Mode Address Propagation Delay: CSADOUT1 Becomes True During ALE or AS		33		33		40		50	0	ns
T24	Track Mode Trailing Edge of ALE or AS to Address High-Z		32		32		35		40	0	ns
T25	Track Mode Read Propagation Delay		29		29		29		35	0	ns
T26	Track Mode Read Hold Time	11	29	11	29	10	29	10	35	0	ns
T27	Track Mode Write Cycle, Data Propagation Delay		20		20		20		30	0	ns
T28	Track Mode Write Cycle, Write to Data Propagation Delay	8	30	8	30	7	40	7	55	0	ns
T29	Hold Time of Port A Valid During Write $\overline{CSOi}$ Trailing Edge	2		2		2		2		0	ns
T30	$\overline{CSI}$ Active to $\overline{CSOi}$ Active	9	40	9	45	9	45	8	60	0	ns
T31	$\overline{CSI}$ Inactive to $\overline{CSOi}$ Inactive	9	40	9	45	9	45	8	60	0	ns
T32	Direct PAD Input as Hold Time	10		10		12		15		0	ns
T33	R/$\overline{W}$ Active to E High	20		20		30		40		0	ns
T34	E End to R/$\overline{W}$	20		20		30		40		0	ns
T35	AS Inactive to E high	0		0		0		0		0	ns
T36	Address to Leading Edge of Write	20		20		25		30		0	ns

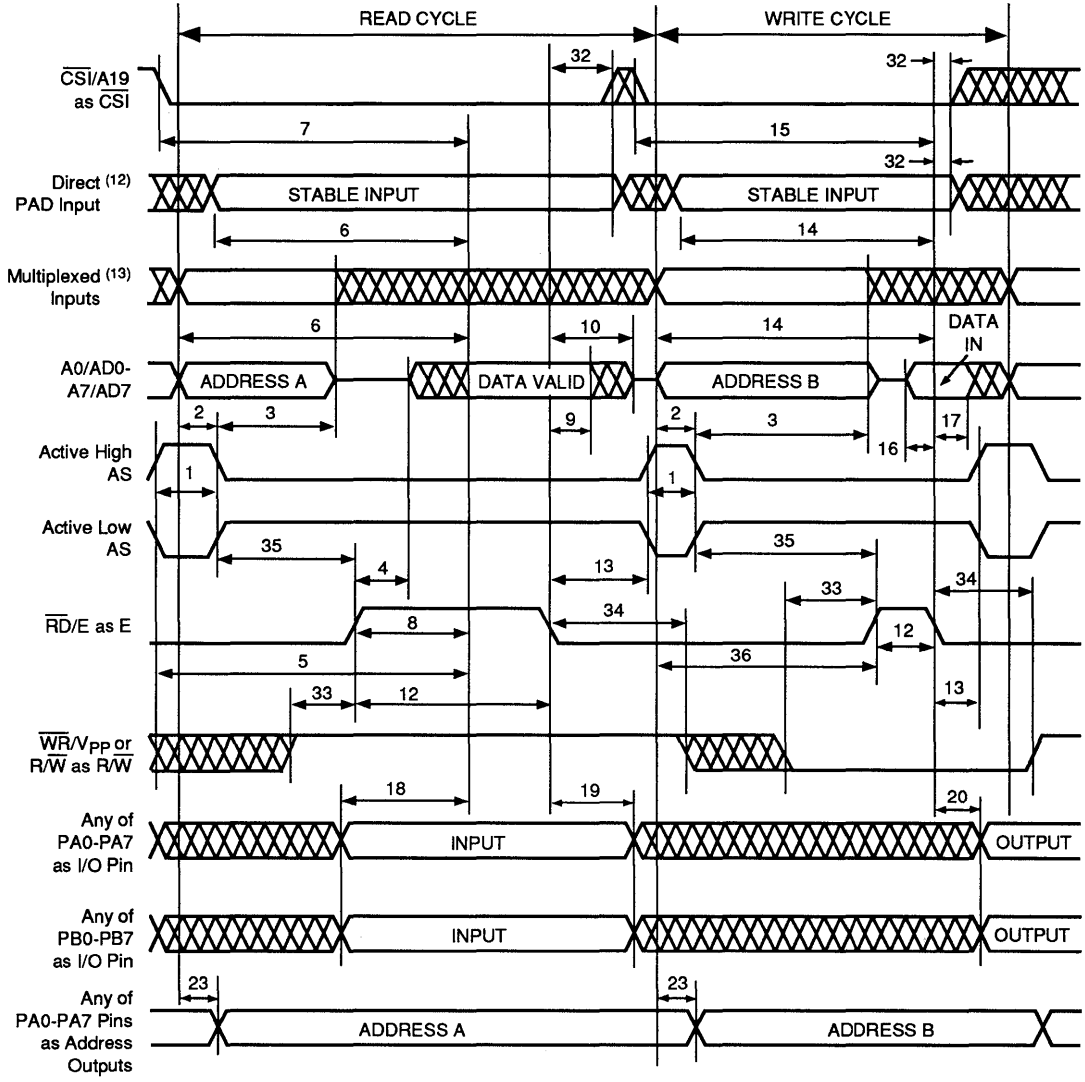
NOTES: 8. ADi = any address line.
9. $\overline{CSOi}$ = any of the chip-select output signals coming through Port B ($\overline{CS0}$–$\overline{CS7}$) or through Port C ($\overline{CS8}$–$\overline{CS10}$).
10. Direct PAD input = any of the following direct PAD input lines: $\overline{CSI}$/A19 as transparent A19, $\overline{RD}$/E/$\overline{DS}$, $\overline{WR}$ or R/$\overline{W}$, transparent PC0–PC2, ALE (or AS).
11. Control signals $\overline{RD}$/E/$\overline{DS}$ or $\overline{WR}$ or R/$\overline{W}$.

Figure 1. Timing of 8-Bit Multiplexed Address/DataBus, CRRWR = 0



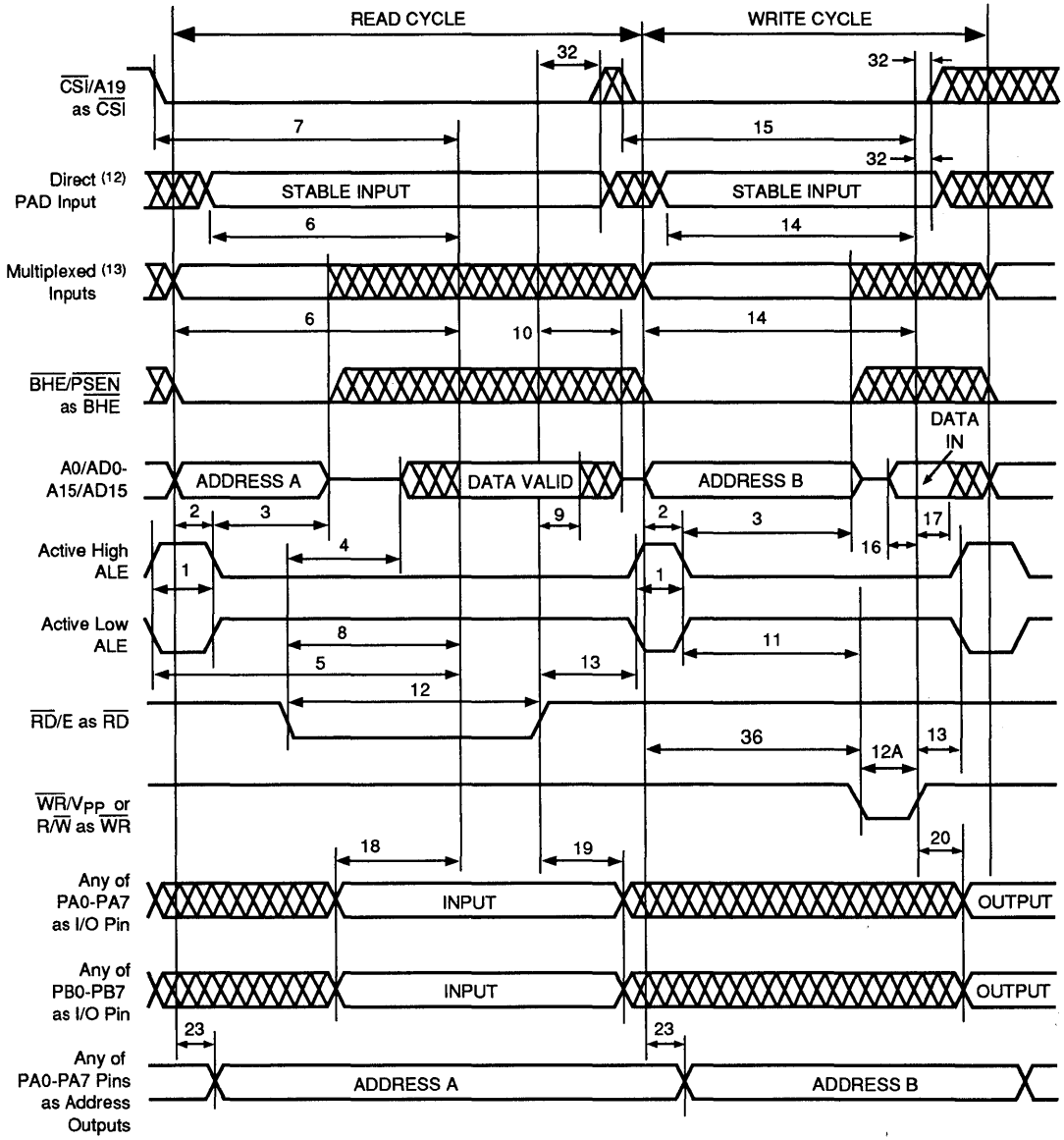
See referenced notes on page 48.

Figure 2. Timing of 8-Bit Multiplexed Address/DataBus, CRRWR = 1



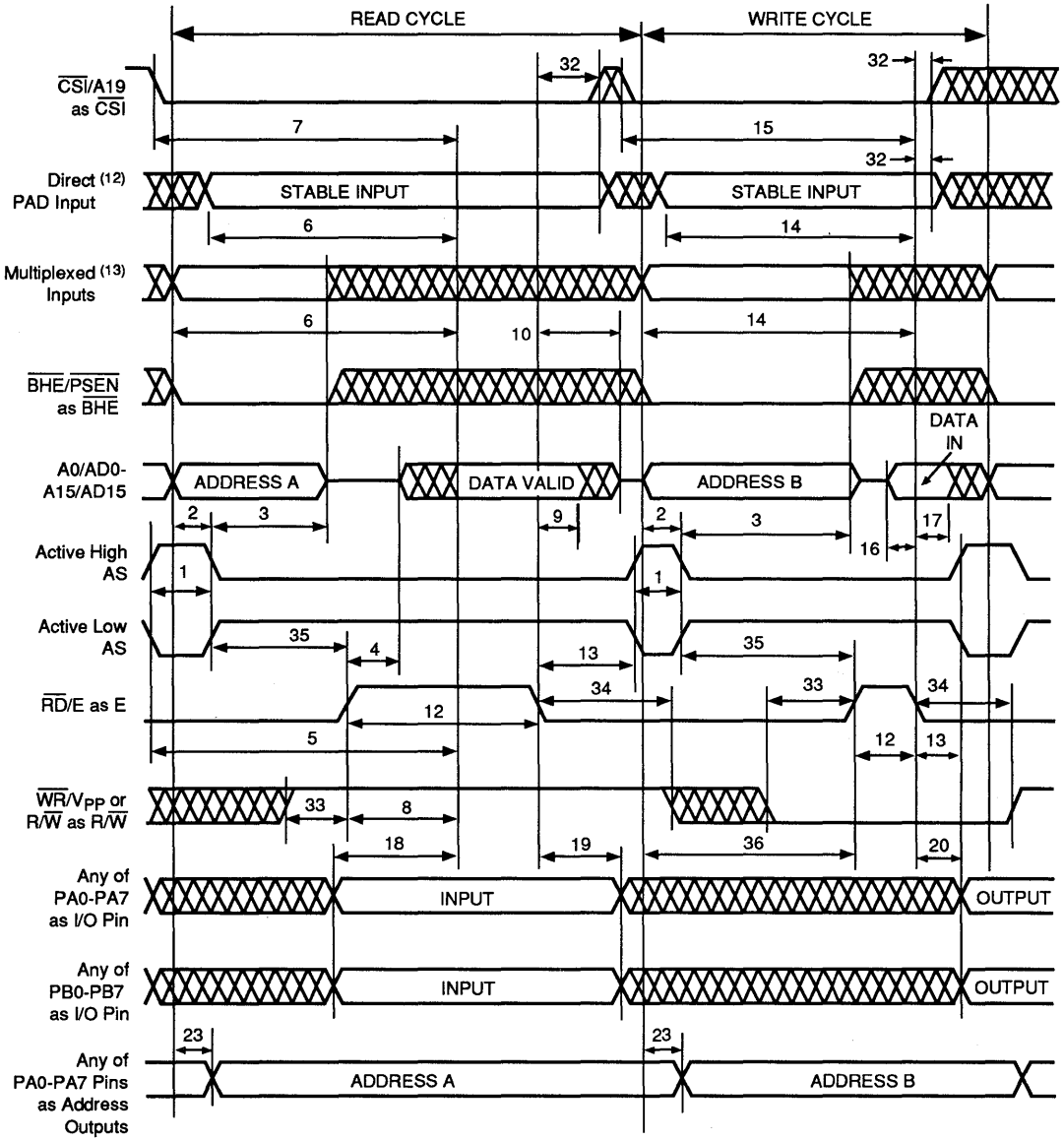
See referenced notes on page 48.

Figure 3. Timing of 16-Bit Multiplexed Address/DataBus, CRRWR = 0



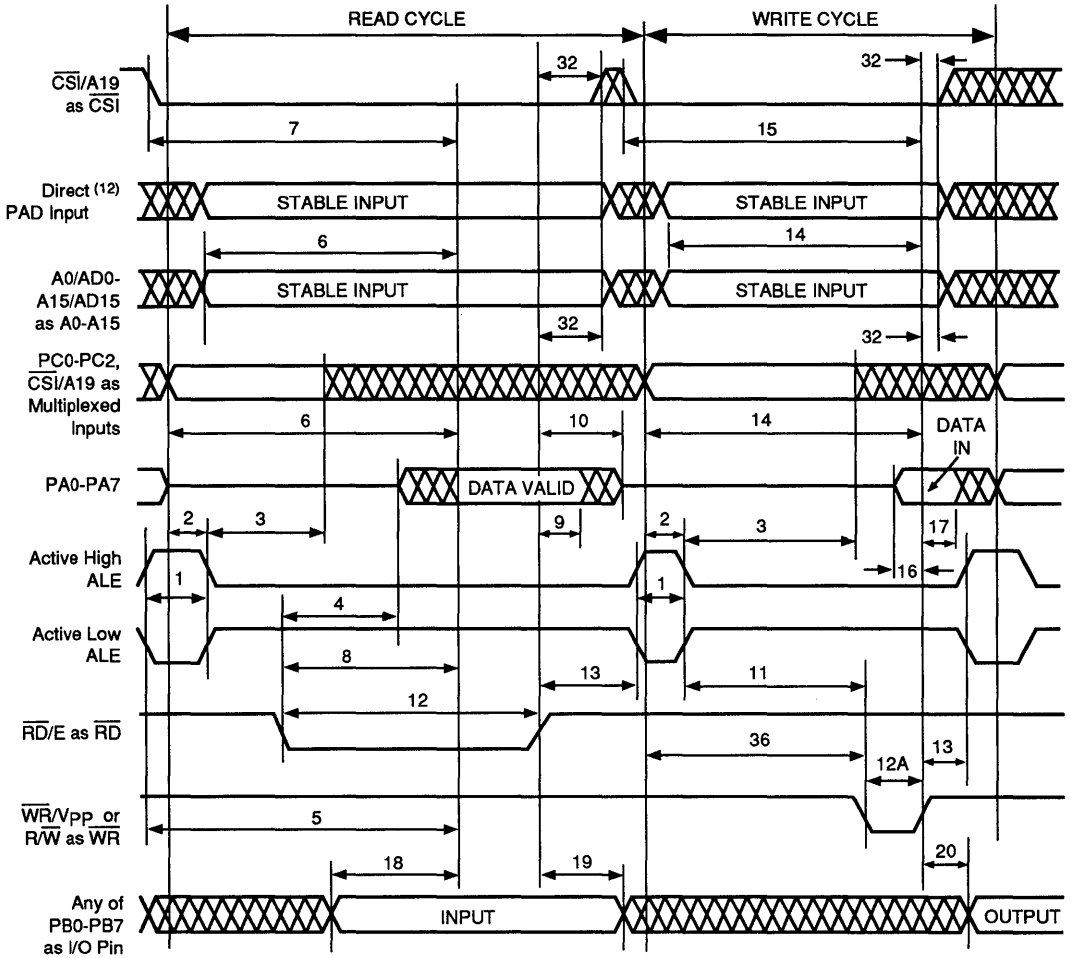
See referenced notes on page 48.

Figure 4. Timing of 16-Bit Multiplexed Address/DataBus, CRRWR = 1



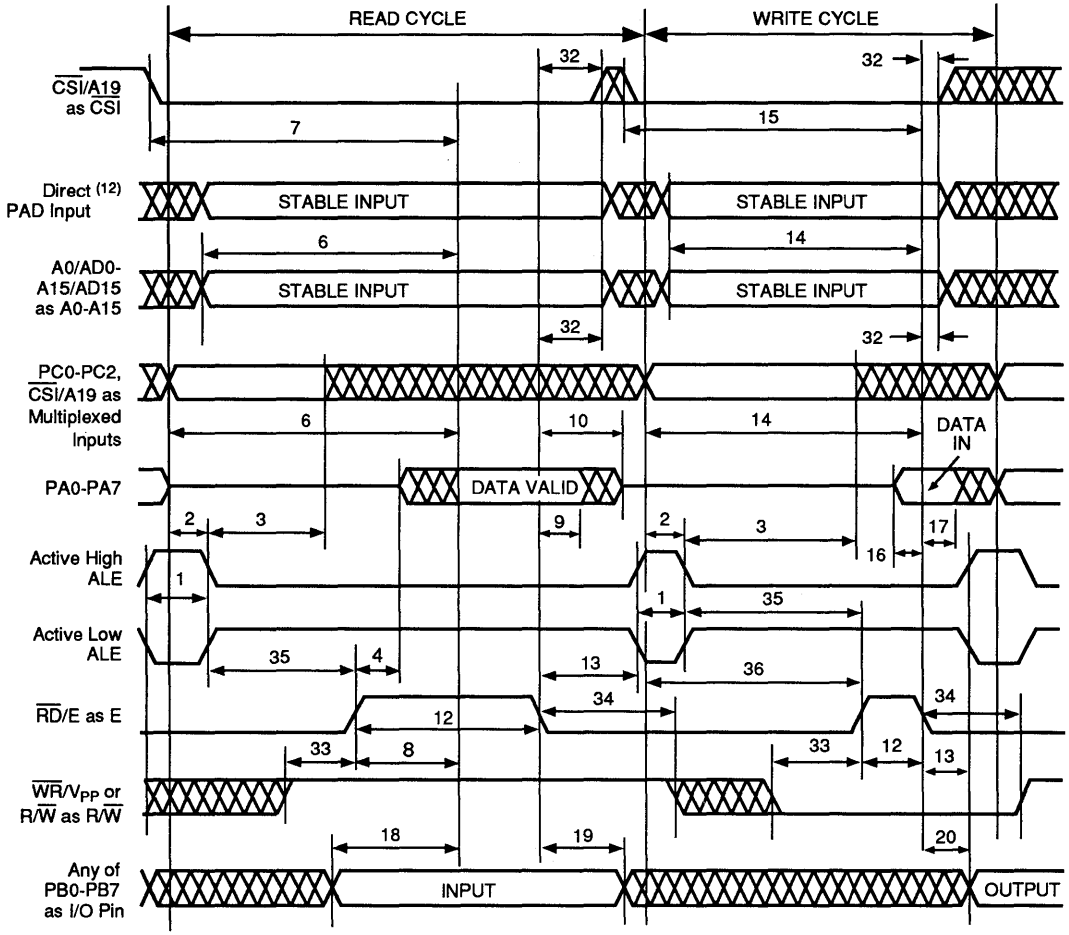
See referenced notes on page 48.

Figure 5. Timing of 8-Bit Data, Non-Multiplexed Address/DataBus, CRRWR = 0



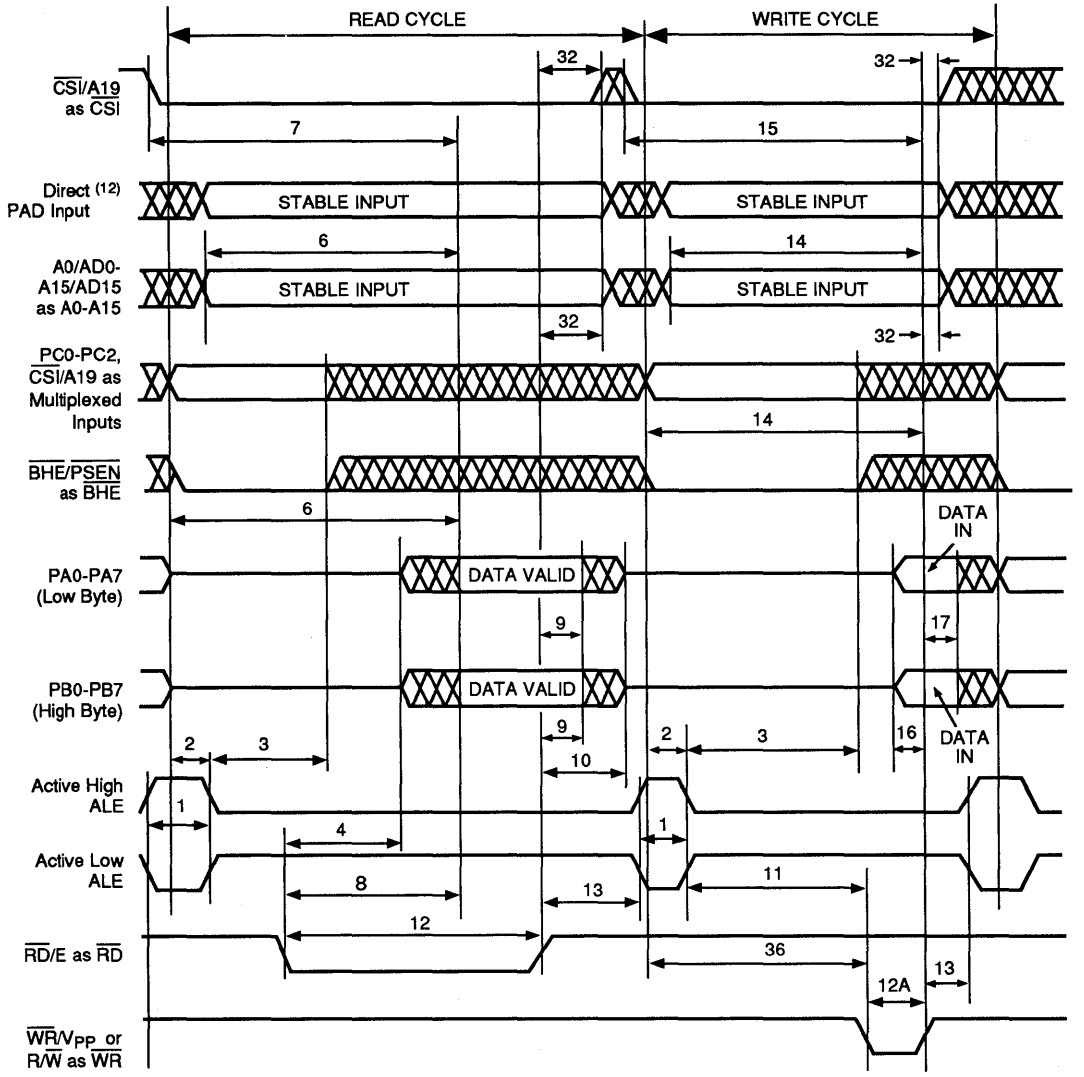
See referenced notes on page 48.

Figure 6. Timing of 8-Bit Data, Non-Multiplexed Address/DataBus, CRRWR = 1



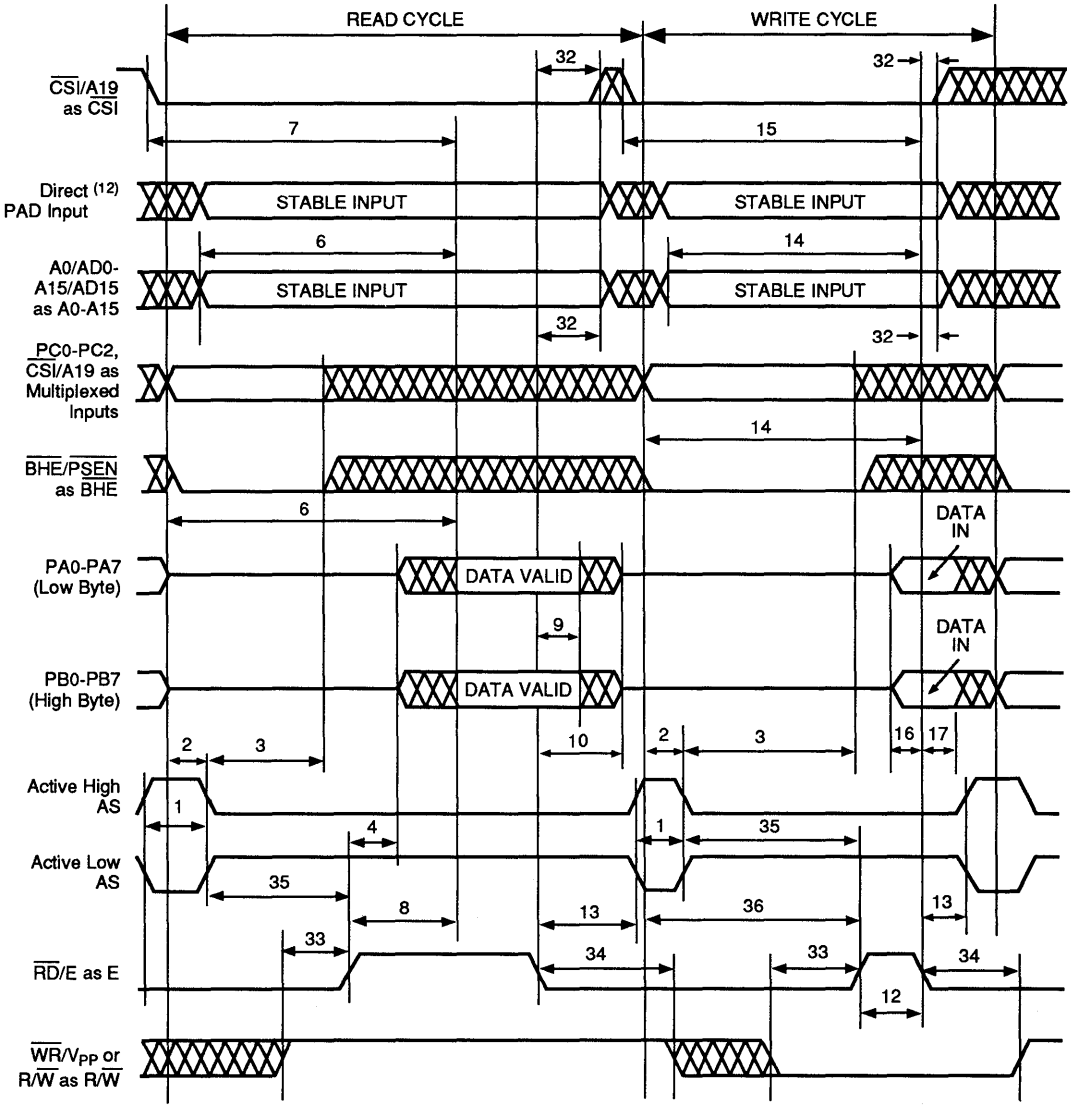
See referenced notes on page 48.

Figure 7. Timing of 16-Bit Non-Multiplexed Address/DataBus, CRRWR = 0



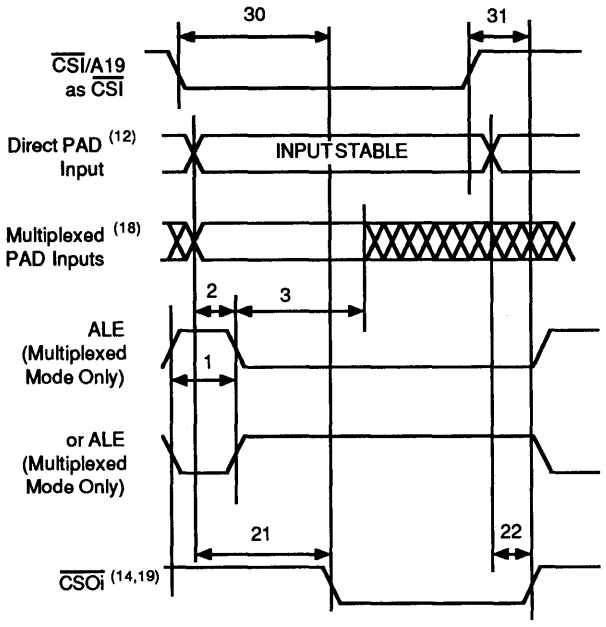
See referenced notes on page 48.

Figure 8. Timing of 16-Bit Non-Multiplexed Address/DataBus, CRRWR = 1



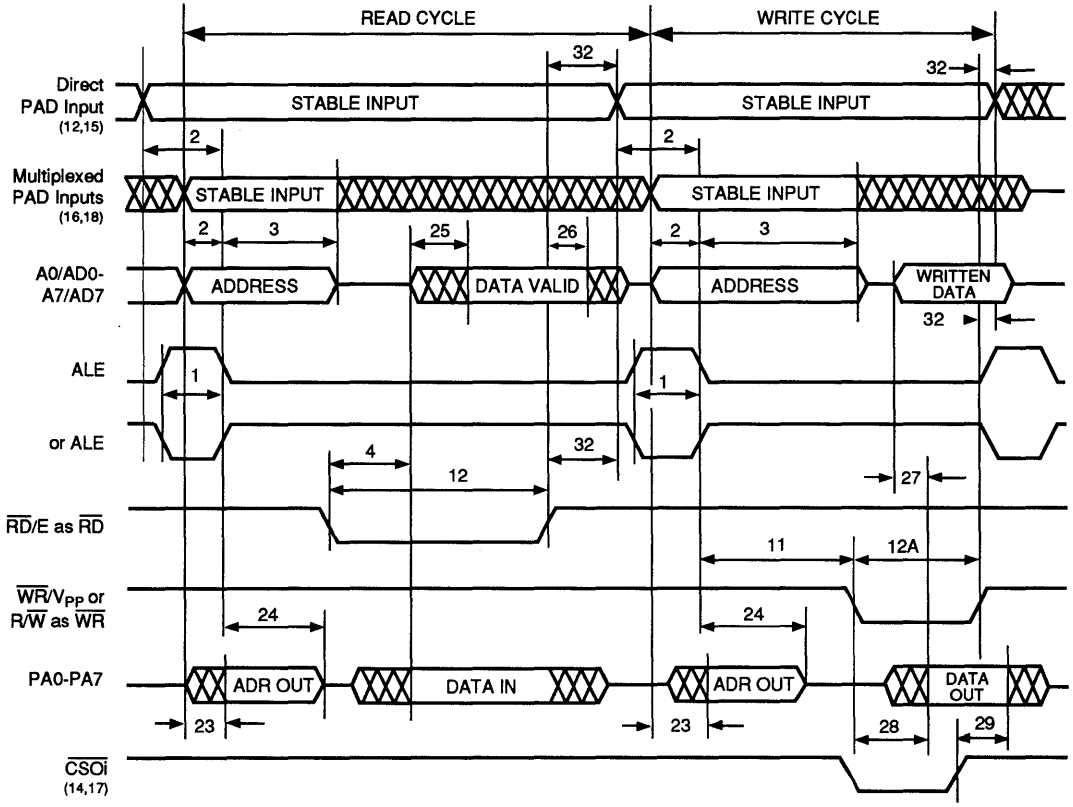
See referenced notes on page 48.

Figure 9. Chip-Select Output Timing



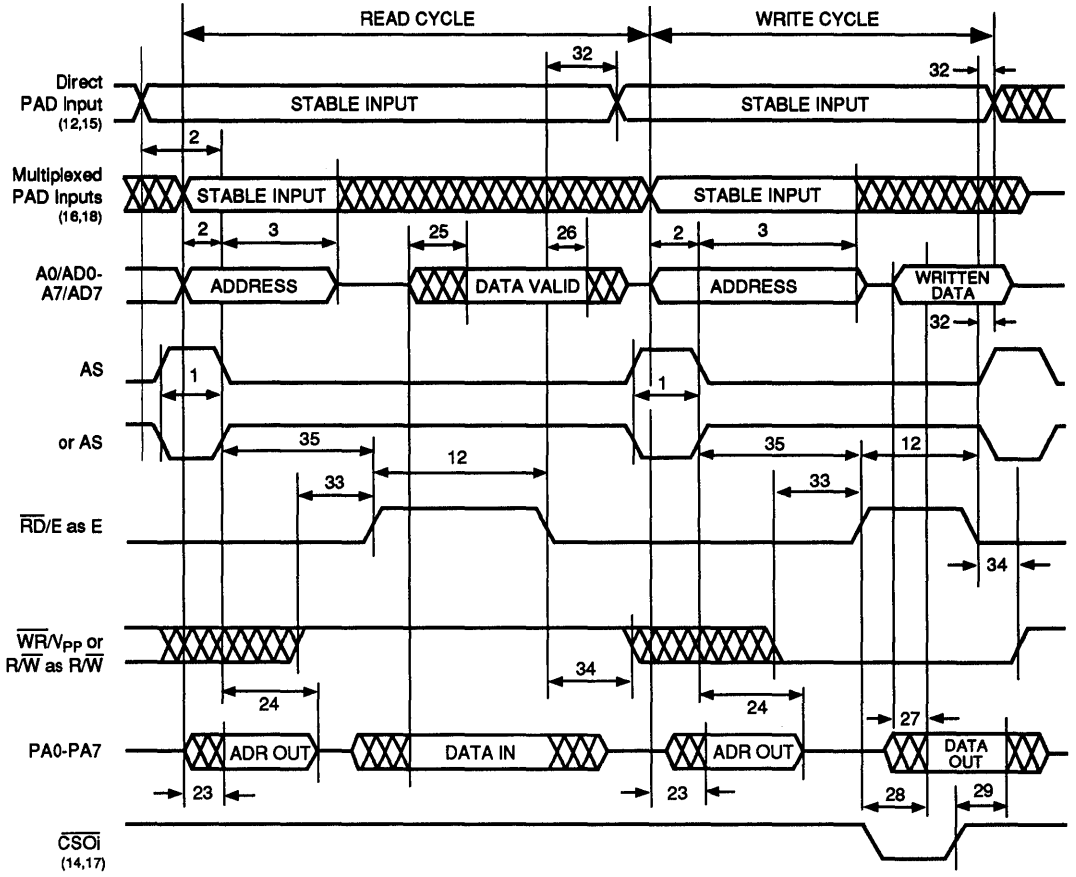
See referenced notes on page 48.

Figure 10. Port A as AD0–AD7 Timing (Track Mode), CRRWR = 0



See referenced notes on page 48.

Figure 11. Port A as AD0–AD7 Timing (Track Mode), CRRWR = 1



Notes for Timing Diagrams

12. Direct PAD input = any of the following direct PAD input lines: CSI/A19 as transparent A19, RD/E, WR or R/W, transparent PC0–PC2, ALE and A11/AD11–A15/AD15 in non-multiplexed modes.
13. Multiplexed inputs: any of the following inputs that are latched by the ALE (or AS): A0/AD0–A15/AD15, CSI/A19 as ALE dependent A19, ALE dependent PC0–PC2.
14. CSOi = any of the chip-select output signals coming through Port B (CS0–CS7) or through Port C (CS8–CS10).
15. CSADOUT1, which internally enables the address transfer to Port A, should be derived only from direct PAD input signals, otherwise the address propagation delay is slowed down.
16. CSADIN and CSADOUT2, which internally enable the data-in or data-out transfers, respectively, can be derived from any combination of direct PAD inputs and multiplexed PAD inputs.
17. The write operation signals are included in the CSOi expression.
18. Multiplexed PAD inputs: any of the following PAD inputs that are latched by the ALE (or AS) in the multiplexed modes: A11/AD11–A15/AD15, CSI/A19 as ALE dependent A19, ALE dependent PC0–PC2.
19. CSOi product terms can include any of the PAD input signals except for reset and CSI.

Pin Capacitance[20]

Symbol	Parameter	Conditions	Typical[21]	Max	Unit
C_{IN}	Capacitance (for input pins only)	V_{IN} = 0 V	4	6	pF
C_{OUT}	Capacitance (for input/output pins)	V_{OUT} = 0 V	8	12	pF
C_{VPP}	Capacitance (for WR/V_{PP} or R/W/V_{PP})	V_{PP} = 0 V	18	25	pF

NOTES: 20. This paramter is only sampled and is not 100% tested.
21. Typical values are for T_A = 25°C and nominal supply voltages.

Figure 12. AC Testing Input/Output Waveform

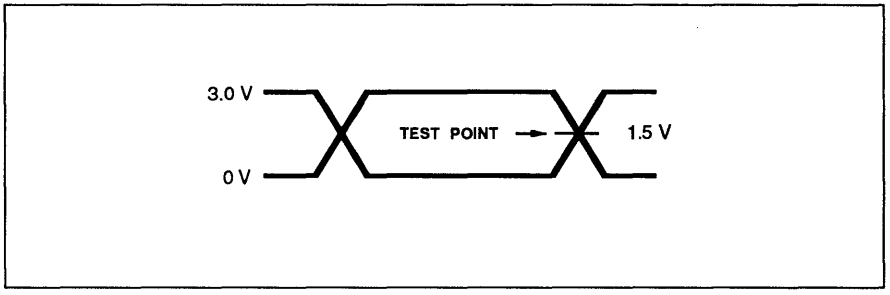
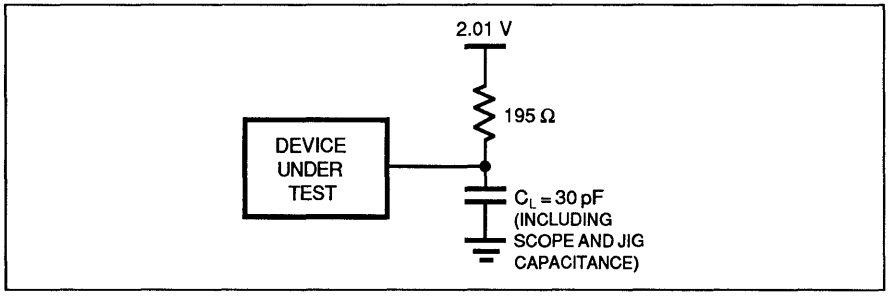


Figure 13. AC Testing Load Circuit



Erasure and Programming

To clear all locations of their programmed contents, expose the device to ultra-violet light source. A dosage of 15 W second/cm^2 is required. This dosage can be obtained with exposure to a wavelength of 2537 Å and intensity of 12000 µW/cm^2 for 15 to 20 minutes. The device should be about 1 inch from the source, and all filters should be removed from the UV light source prior to erasure.

The PSD3XX and similar devices will erase with light sources having wavelengths shorter than 4000 Å. Although the erasure times will be much longer than with UV sources at 2537 Å, exposure to fluorescent light and sunlight eventually erases the device. For maximum system reliability, these sources should be avoided. If used in such an environment, the package windows should be covered by an opaque substance.

Upon delivery, or after each erasure, the PSD3XX device has all bits in the PAD and EPROM in the "1" or high state. The configuration bits are in the "0" or low state. The code, configuration, and PAD MAP data are loaded through the procedure of programming

Pin Assignments

Pin Name	44-Pin PLCC/CLCC Package	52-Pin PQFP Package
$\overline{BHE}/\overline{PSEN}$	1	46
$\overline{WR}/V_{PP}$ or $R/\overline{W}$	2	47
RESET	3	48
PB7	4	49
PB6	5	50
PB5	6	51
PB4	7	2
PB3	8	3
PB2	9	4
PB1	10	5
PB0	11	6
GND	12	7
ALE or AS	13	8
PA7	14	9
PA6	15	10
PA5	16	11
PA4	17	12
PA3	18	15
PA2	19	16
PA1	20	17
PA0	21	18
$\overline{RD}/E$	22	19
AD0/A0	23	20
AD1/A1	24	21
AD2/A2	25	22
AD3/A3	26	23
AD4/A4	27	24
AD5/A5	28	25
AD6/A6	29	28
AD7/A7	30	29
AD8/A8	31	30
AD9/A9	32	31
AD10/A10	33	32
GND	34	33
AD11/A11	35	34
AD12/A12	36	35
AD13/A13	37	36
AD14/A14	38	37
AD15/A15	39	38
PC0	40	41
PC1	41	42
PC2	42	43
A19/$\overline{CSI}$	43	44
V_{CC}	44	45

NOTE: 36. Pins 1, 13, 14, 26, 27, 39, 40, and 52 are No Connect.

Package Information

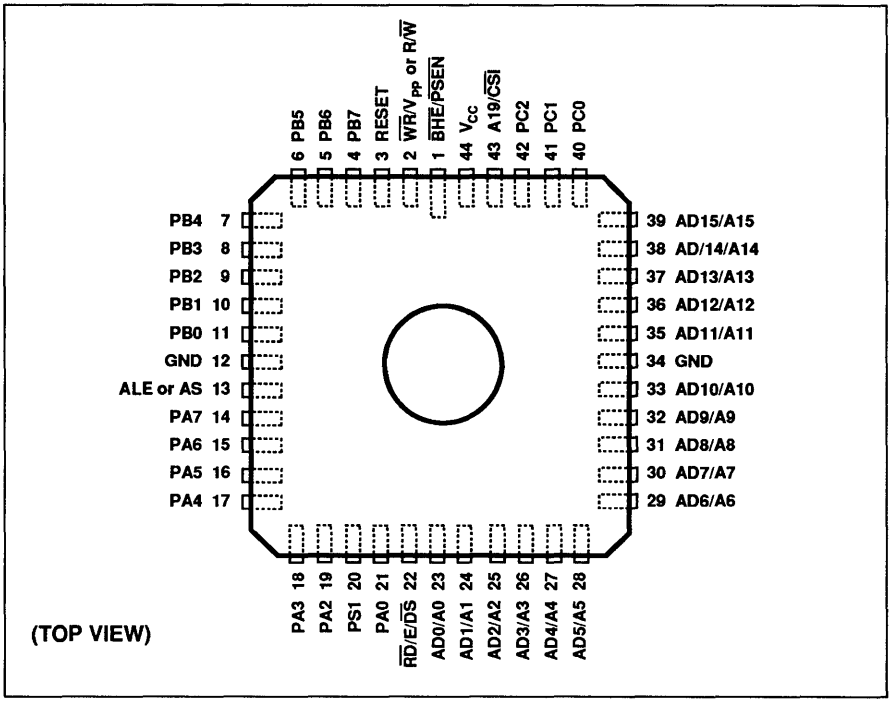


Figure 14. Drawing L4 – 44 Pin Ceramic Leaded Chip Carrier (CLCC) with Window (Package Type L)

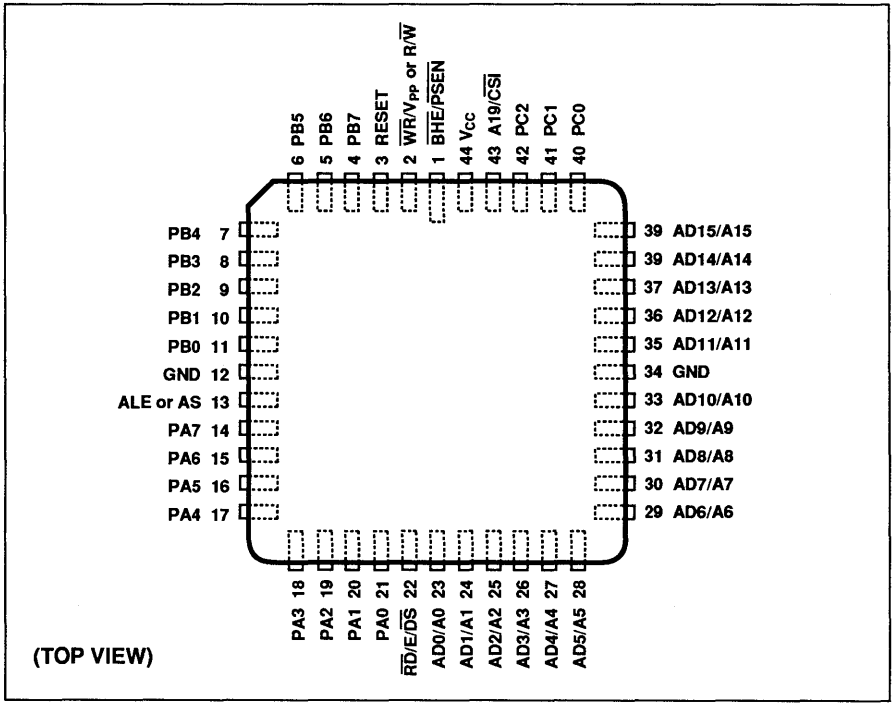
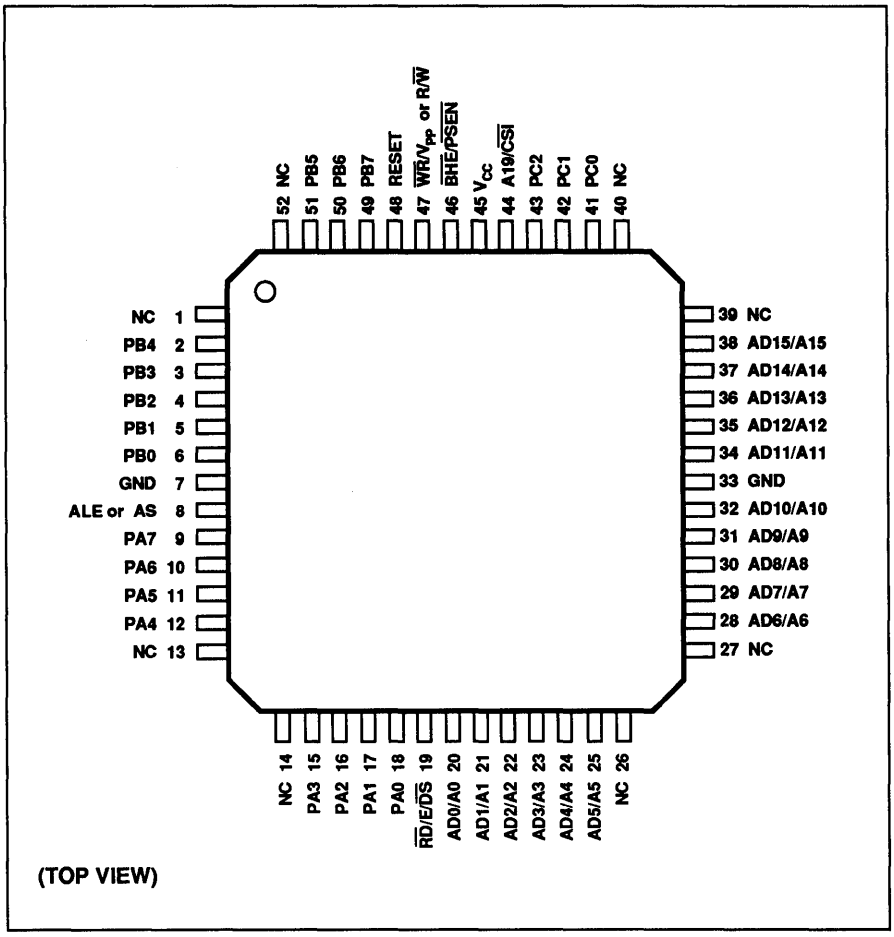


Figure 15. Drawing J2 – 44 Pin Plastic Leaded Chip Carrier (PLCC) (Package Type J)

Figure 16. Drawing Q2 – 52 Pin PQFP (Package Type Q)



Ordering Information

Part Number	Spd. (ns)	Package Type	Package Drawing	Operating Temperature Range	Manufacturing Procedure
PSD301-90 A	90	44-pin PLCC	J2	Commercial	Standard
PSD301-90 KA	90	44-pin CLCC	L4	Commercial	Standard
PSD301-12 A	120	44-pin PLCC	J2	Commercial	Standard
PSD301-12 KA	120	44-pin CLCC	L4	Commercial	Standard
PSD301-12 B	120	52-pin PQFP	Q2	Commercial	Standard
PSD301-15 A	150	44-pin PLCC	J2	Commercial	Standard
PSD301-15I A	150	44-pin PLCC	J2	Industrial	Standard
PSD301-15 KA	150	44-pin CLCC	L4	Commercial	Standard
PSD301-15I KA	150	44-pin CLCC	L4	Industrial	Standard
PSD301-15 B	150	52-pin PQFP	Q2	Commercial	Standard
PSD301-15I B	150	52-pin PQFP	Q2	Industrial	Standard
PSD301-20 A	200	44-pin PLCC	J2	Commercial	Standard
PSD301-20I A	200	44-pin PLCC	J2	Industrial	Standard
PSD301-20 KA	200	44-pin CLCC	L4	Commercial	Standard
PSD301-20I KA	200	44-pin CLCC	L4	Industrial	Standard
PSD301-20 B	200	52-pin PQFP	Q2	Commercial	Standard
PSD301-20I B	200	52-pin PQFP	Q2	Industrial	Standard

Field-programmable microcontroller peripheral — PSD311

Key Features

- Single Chip Programmable Peripheral for Microcontroller-based Applications
- 19 Individually Configurable I/O pins that can be used as:
  - Microcontroller I/O port expansion
  - Programmable Address Decoder (PAD) I/O
  - Latched address output
  - Open drain or CMOS
- Two Programmable Arrays (PAD A and PAD B)
  - Total of 40 Product Terms and up to 16 Inputs and 24 Outputs
  - Address Decoding up to 1 MB
  - Logic replacement
- "No Glue" Microcontroller Chip-Set
  - Built-in address latches for multiplexed address/data bus
  - Non-multiplexed address/data bus mode
  - 8-bit data bus width
  - ALE and Reset polarity programmable
  - Selectable modes for read and write control bus as $\overline{RD}/\overline{WR}$ or R/$\overline{W}$/E
  - $\overline{PSEN}$ pin for 8051 users
- 256 Kbits of UV EPROM
  - Configurable as 32K x 8
  - Divides into 8 equal mappable blocks for optimized mapping
  - Block resolution is 4K x 8
  - 120 ns EPROM access time, including input latches and PAD address decoding.
- 16 Kbit Static RAM
  - Configurable as 2K x 8
  - 120 ns SRAM access time, including input latches and PAD address decoding
- Address/Data Track Mode
  - Enables easy Interface to Shared Resources (e.g., Mail Box SRAM) with other Microcontrollers or a Host Processor
- Built-In Security
  - Locks the PSD311 and PAD Decoding Configuration
- Available in a Choice of Packages
  - 44 Pin PLCC and CLCC
  - 52 Pin PQFP
  - 44 Pin CPGA
- Simple Menu-Driven Software: Configure the PSD311 on an IBM PC

Security Mode

Security Mode in the PSD3XX locks the contents of the PAD A , PAD B and all the configuration bits. The EPROM, SRAM, and I/O contents can be accessed only through the PAD. The Security Mode can be set by the MAPLE or Programming software. In window packages, the mode is erasable through UV full part erasure. In the security mode, the PSD3XX contents cannot be copied on a programmer.

CMiser-Bit

The CMiser-Bit provides a programmable option for power-sensitive applications that require further reduction in power consumption. The CMiser-Bit (CMiser = 1) in the Maple portion of the PSD3XX sytem development software can be used to reduce power consumption. The CMiser-Bit turns off the EPROM blocks in the PSD3XX whenever the EPROM is not accessed, thereby reducing the active current consumed by the PSD3XX.

In the default mode, or if the PSD3XX is configured without programming the CMiser-Bit (CMiser = 0), the device operates at specified speed and power rating as specified in the A.C. and D.C. Characteristics.

However, if the CMiser-Bit is programmed (CMiser = 1), the device consumes even lower current, and is reflected in the data sheet. This mode has an adder in propagation delay in T5, T6, and T7 parameters in the A.C. Characteristics, and should be added to compute worst-case timing requirements in the application.

Absolute Maximum Ratings[1]

Symbol	Parameter	Condition	Min	Max	Unit
T_{STG}	Storage Temperature	CERDIP	– 65	+ 150	°C
		PLASTIC	– 65	+ 125	°C
	Voltage on any Pin	With Respect to GND	– 0.6	+ 7	V
V_{PP}	Programming Supply Voltage	With Respect to GND	– 0.6	+ 14	V
V_{CC}	Supply Voltage	With Respect to GND	– 0.6	+ 7	V
	ESD Protection			>2000	V

NOTE: 1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at theses or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods of time may affect device reliability.

Operating Range

Range	Temperature	V_{CC}	V_{CC} Tolerance		
			-12	-15	-20
Commercial	0° C to +70°C	+ 5 V	± 10%	± 10%	± 10%
Industrial	–40° C to +80°C	+ 5 V		± 10%	± 10%
Military	–55° C to +125°C	+ 5 V			± 10%

Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	Supply Voltage	All Speeds	4.5	5	5.5	V
V_{IH}	High-level Input Voltage	V_{CC} = 4.5 V to 5.5 V	2			V
V_{IL}	Low-level Input Voltage	V_{CC} = 4.5 V to 5.5 V	0		0.8	V

DC Characteristics

Symbol	Parameter	Conditions				CMiser = 1 Subtract:			Unit
			Min	Typ	Max	Min	Typ	Max	
V_{OL}	Output Low Voltage	I_{OL} = 20 µA V_{CC} = 4.5 V		0.01	0.1				V
		I_{OL} = 8 mA V_{CC} = 4.5 V		0.15	0.45				V
V_{OH}	Output High Voltage	I_{OH} = –20 µA V_{CC} = 4.5 V	4.4	4.49					V
		I_{OH} = –2 mA V_{CC} = 4.5 V	2.4	3.9					V
I_{SB1}	V_{CC} Standby Current (CMOS) (Notes 2 and 4)	Comm'l		50	100				µA
		Ind/Mil		75	150				µA
I_{CC1}	Active Current (CMOS) (No Internal Memory Block Selected) (Notes 2 and 5)	Comm'l (Note 6)		16	35		7	10	mA
		Comm'l (Note 7)		28	50		7	10	mA
		Ind/Mil (Note 6)		16	45		7	10	mA
		Ind/Mil (Note 7)		28	60		7	10	mA
I_{CC2}	Active Current (CMOS) (EPROM Block Selected) (Notes 2 and 5)	Comm'l (Note 6)		16	35		0	0	mA
		Comm'l (Note 7)		28	50		0	0	mA
		Ind/Mil (Note 6)		16	45		0	0	mA
		Ind/Mil (Note 7)		28	60		0	0	mA
I_{CC3}	Active Current (CMOS) (SRAM Block Selected (Notes 2 and 5)	Comm'l (Note 6)		47	80		7	10	mA
		Comm'l (Note 7)		59	95		7	10	mA
		Ind/Mil (Note 6)		47	100		7	10	mA
		Ind/Mil (Note 7)		59	115		7	10	mA
I_{LI}	Input Leakage Current	V_{IN} = 5.5 V or GND	–1	±0.1	1				µA
I_{LO}	Output Leakage Current	V_{OUT} = 5.5 V or GND	–10	±5	10				µA

NOTES: 2. CMOS inputs: GND ± 0.3 V or V_{CC} ± 0.3V.
3. TTL inputs: $V_{IL} \leq 0.8$ V, $V_{IH} \geq 2.0$ V.
4. CSI/A19 is high and the part is in a power-down configuration mode.
5. Add 3.0 mA/MHz for AC power component (power = AC + DC).
6. Ten (10) PAD product terms active. (Add 380 µA per product term, typical, or 480 µA per product term maximum
7. Forty-one (41) PAD product terms active.

AC Characteristics

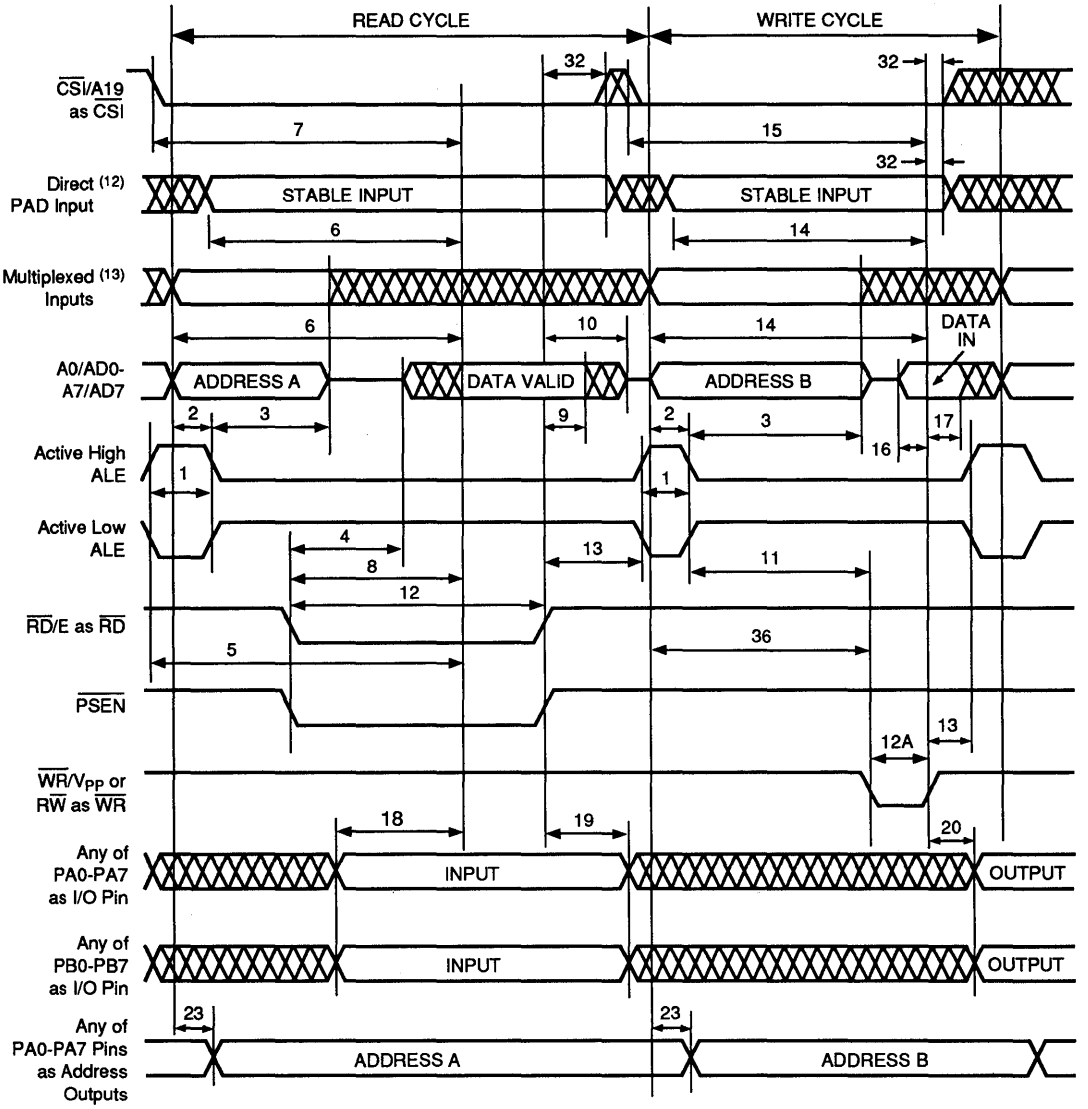
Symbol	Parameter	-90		-12		-15		-20		CMiser = 1 Add:	Unit
		Min	Max	Min	Max	Min	Max	Min	Max		
T1	ALE or AS Pulse Width	20		30		40		50		0	ns
T2	Address Set-up Time	5		9		12		15		0	ns
T3	Address Hold Time	8		13		15		25		0	ns
T4	Leading Edge of Read to Data Active	0		0		0		0		0	ns
T5	ALE Valid to Data Valid		100		140		170		200	10	ns
T6	Address Valid to Data Valid		90		120		150		200	10	ns
T7	$\overline{CSI}$ Active to Data Valid		100		150		160		200	15	ns
T8	Leading Edge of Read to Data Valid		32		38		55		60	0	ns
T9	Read Data Hold Time	0		0		0		0		0	ns
T10	Trailing Edge of Read to Data High-Z		35		35		40		45	0	ns
T11	Trailing Edge of ALE or AS to Leading Edge of Write	0		0		0		0		0	ns
T12	$\overline{RD}$, E, $\overline{PSEN}$, or $\overline{DS}$ Pulse Width	40		45		60		75		0	ns
T12A	$\overline{WR}$ Pulse Width	20		25		35		45		0	ns
T13	Trailing Edge of Write or Read to Leading Edge of ALE or AS	0		0		0		0		0	ns
T14	Address Valid to Trailing Edge of Write	90		120		150		200		0	ns
T15	$\overline{CSI}$ Active to Trailing Edge of Write	100		130		160		200		0	ns
T16	Write Data Set-up Time	20		25		30		40		0	ns
T17	Write Data Hold Time	5		5		10		15		0	ns
T18	Port to Data Out Valid Propagation Delay		30		30		35		45	0	ns
T19	Port Input Hold Time	0		0		0		0		0	ns
T20	Trailing Edge of Write to Port Output Valid	40		40		50		60		0	ns
T21	ADi or Control to $\overline{CSOi}$ Valid	6	25	6	30	6	35	5	45	0	ns
T22	ADi or Control to $\overline{CSOi}$ Invalid	5	25	5	30	4	35	4	45	0	ns

AC Characteristics (Cont.)

Symbol	Parameter	-90		-12		-15		-20		CMiser = 1 Add:*	Unit
		Min	Max	Min	Max	Min	Max	Min	Max		
T23	Track Mode Address Propagation Delay: CSADOUT1 Already True		22		22		22		28	0	ns
T23A	Track Mode Address Propagation Delay: CSADOUT1 Becomes True During ALE or AS		33		33		40		50	0	ns
T24	Track Mode Trailing Edge of ALE or AS to Address High-Z		32		32		35		40	0	ns
T25	Track Mode Read Propagation Delay		29		29		29		35	0	ns
T26	Track Mode Read Hold Time	11	29	11	29	10	29	10	35	0	ns
T27	Track Mode Write Cycle, Data Propagation Delay		20		20		20		30	0	ns
T28	Track Mode Write Cycle, Write to Data Propagation Delay	8	30	8	30	7	40	7	55	0	ns
T29	Hold Time of Port A Valid During Write $\overline{CSOi}$ Trailing Edge	2		2		2		2		0	ns
T30	$\overline{CSI}$ Active to $\overline{CSOi}$ Active	9	40	9	45	9	45	8	60	0	ns
T31	$\overline{CSI}$ Inactive to $\overline{CSOi}$ Inactive	9	40	9	45	9	45	8	60	0	ns
T32	Direct PAD Input as Hold Time	10		10		12		15		0	ns
T33	R/$\overline{W}$ Active to E High	20		20		30		40		0	ns
T34	E End to R/$\overline{W}$	20		20		30		40		0	ns
T35	AS Inactive to E high	0		0		0		0		0	ns
T36	Address to Leading Edge of Write	20		20		25		30		0	ns

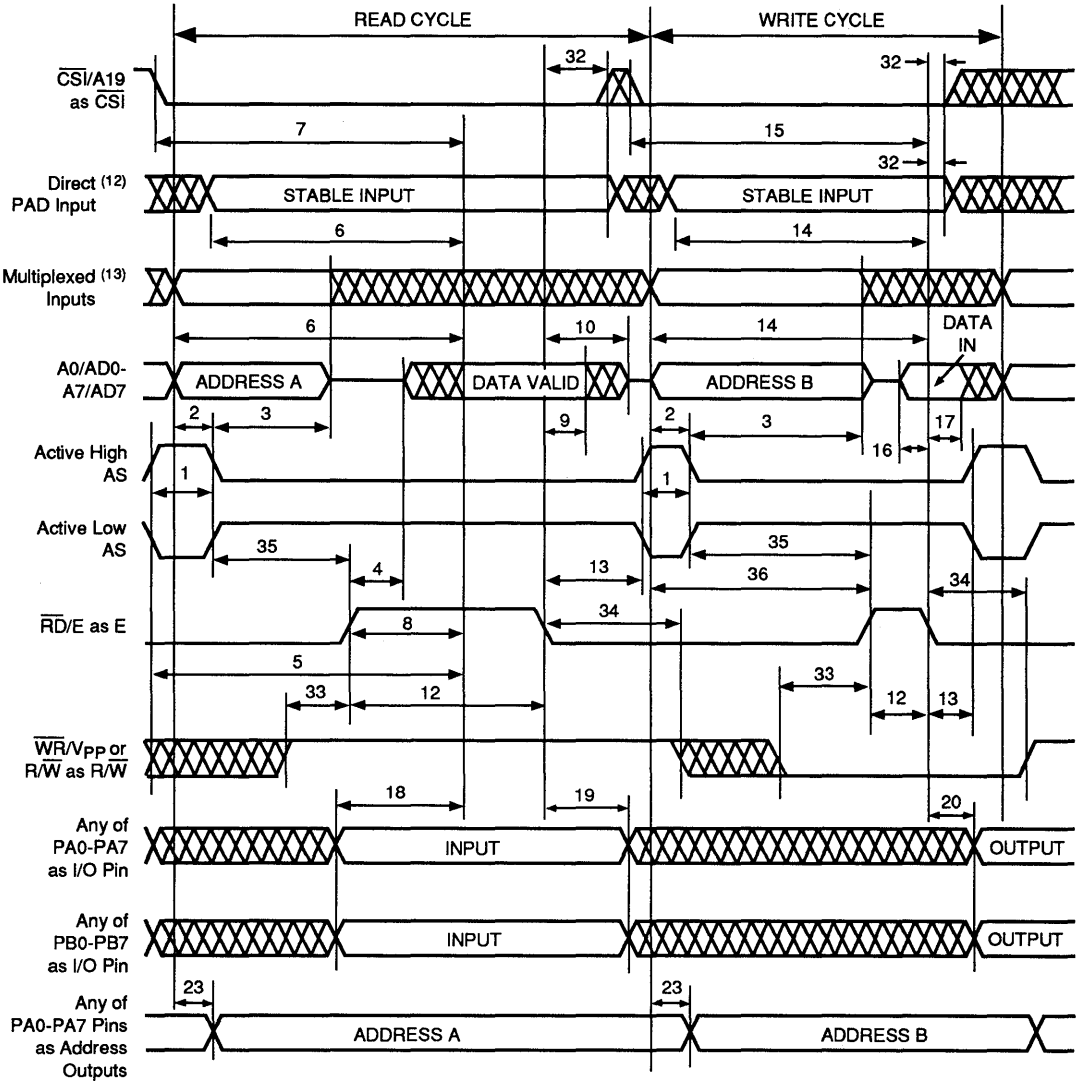
NOTES: 8. ADi = any address line.
9. $\overline{CSOi}$ = any of the chip-select output signals coming through Port B ($\overline{CS0}$–$\overline{CS7}$) or through Port C ($\overline{CS8}$–$\overline{CS10}$).
10. Direct PAD input = any of the following direct PAD input lines: $\overline{CSI}$/A19 as transparent A19, $\overline{RD}$/E/$\overline{DS}$, $\overline{WR}$ or R/$\overline{W}$, transparent PC0–PC2, ALE (or AS).
11. Control signals $\overline{RD}$/E/$\overline{DS}$ or $\overline{WR}$ or R/$\overline{W}$.

Figure 1. Timing of 8-Bit Multiplexed Address/DataBus, CRRWR = 0



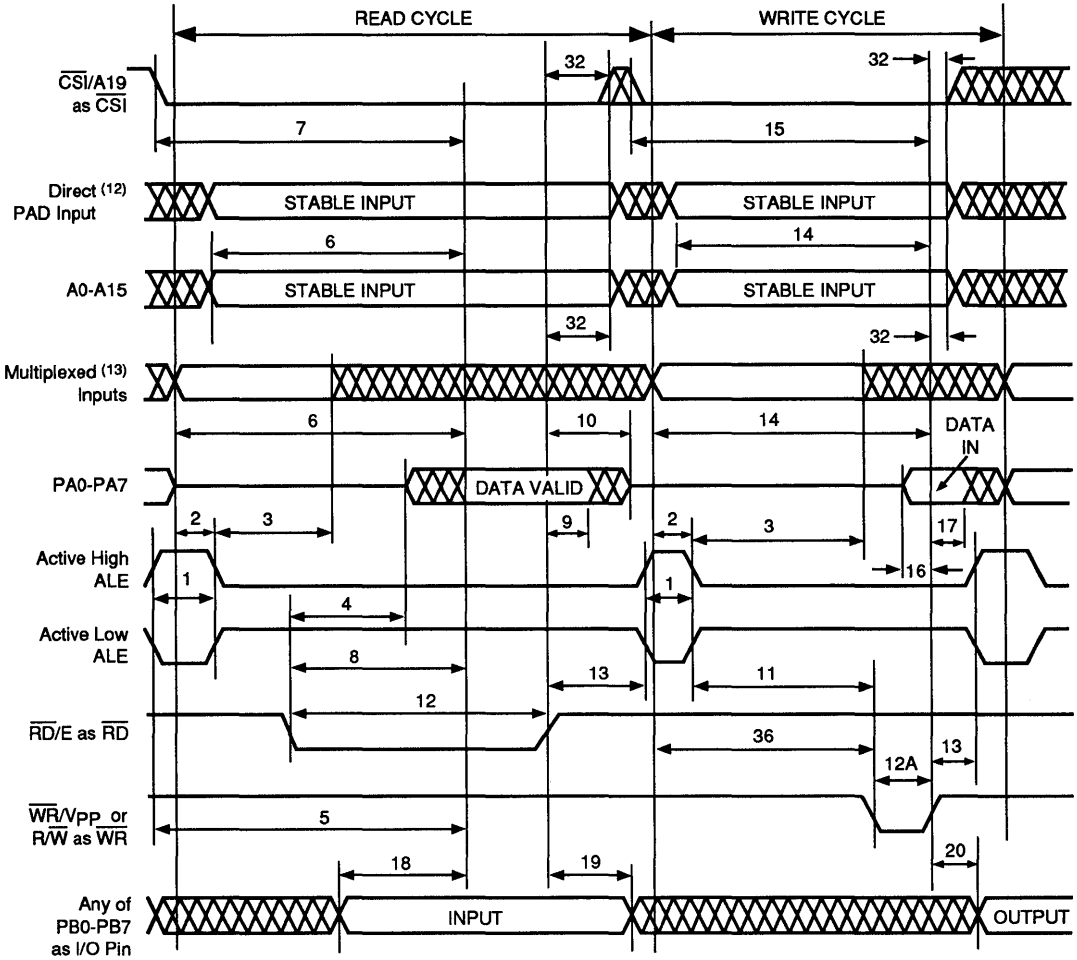
See referenced notes on page 66.

Figure 2. Timing of 8-Bit Multiplexed Address/DataBus, CRRWR = 1



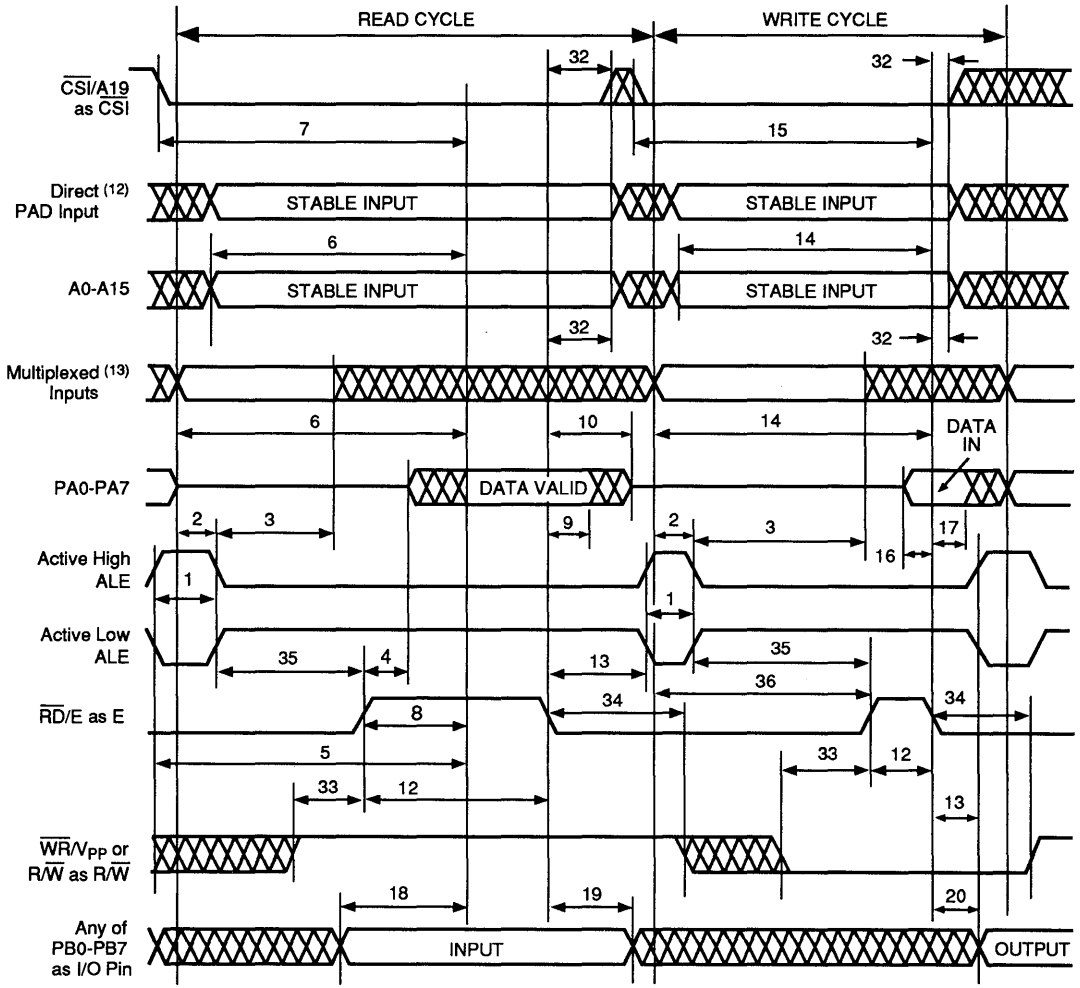
See referenced notes on page 66.

Figure 3. Timing of 8-Bit Data, Non-Multiplexed Address/DataBus, CRRWR = 0



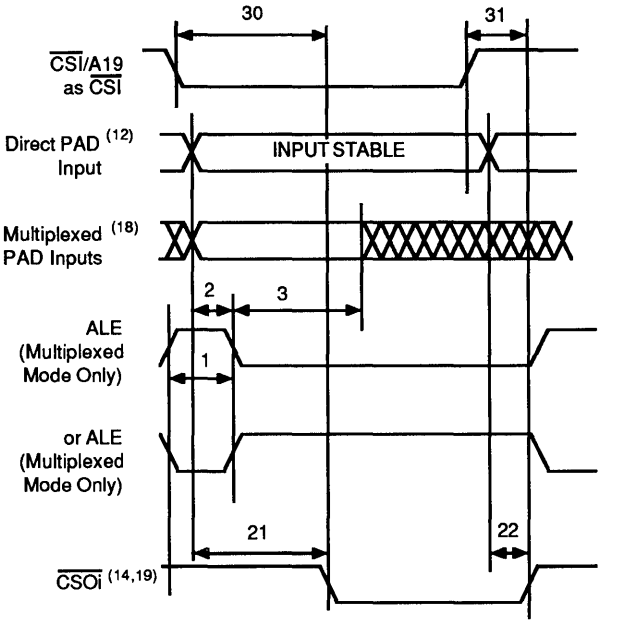
See referenced notes on page 66.

Figure 4. Timing of 8-Bit Data, Non-Multiplexed Address/DataBus, CRRWR = 1



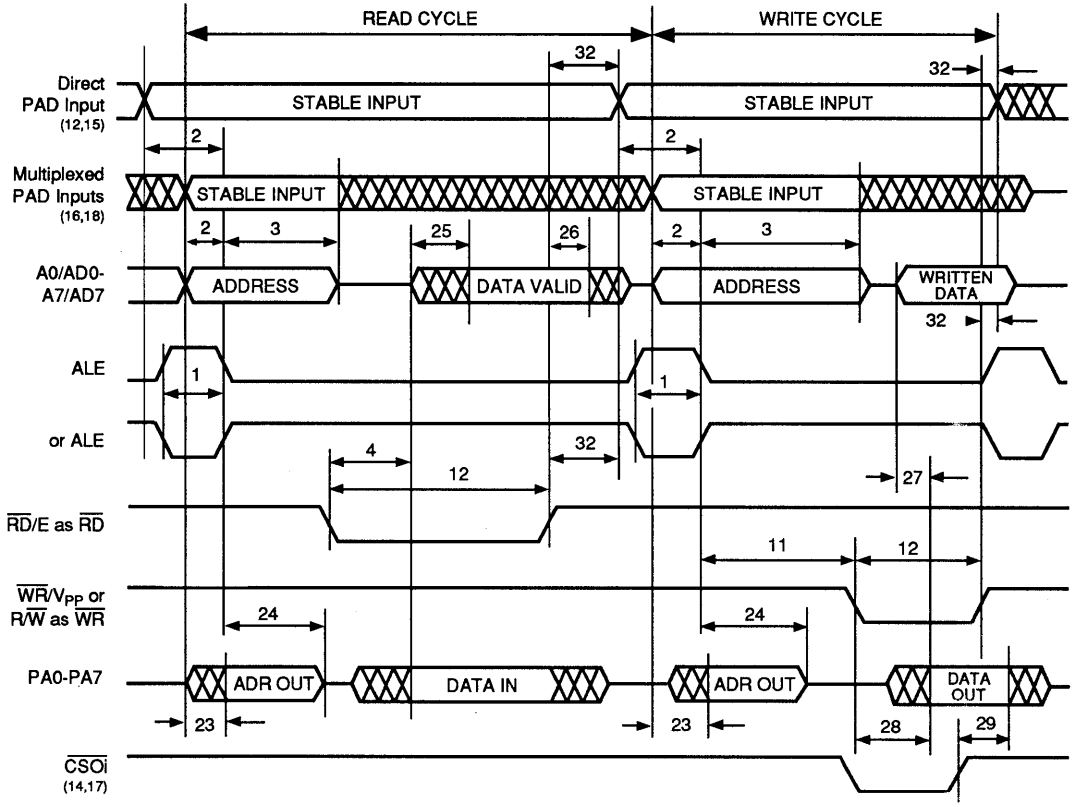
See referenced notes on page 66.

Figure 5. Chip-Select Output Timing



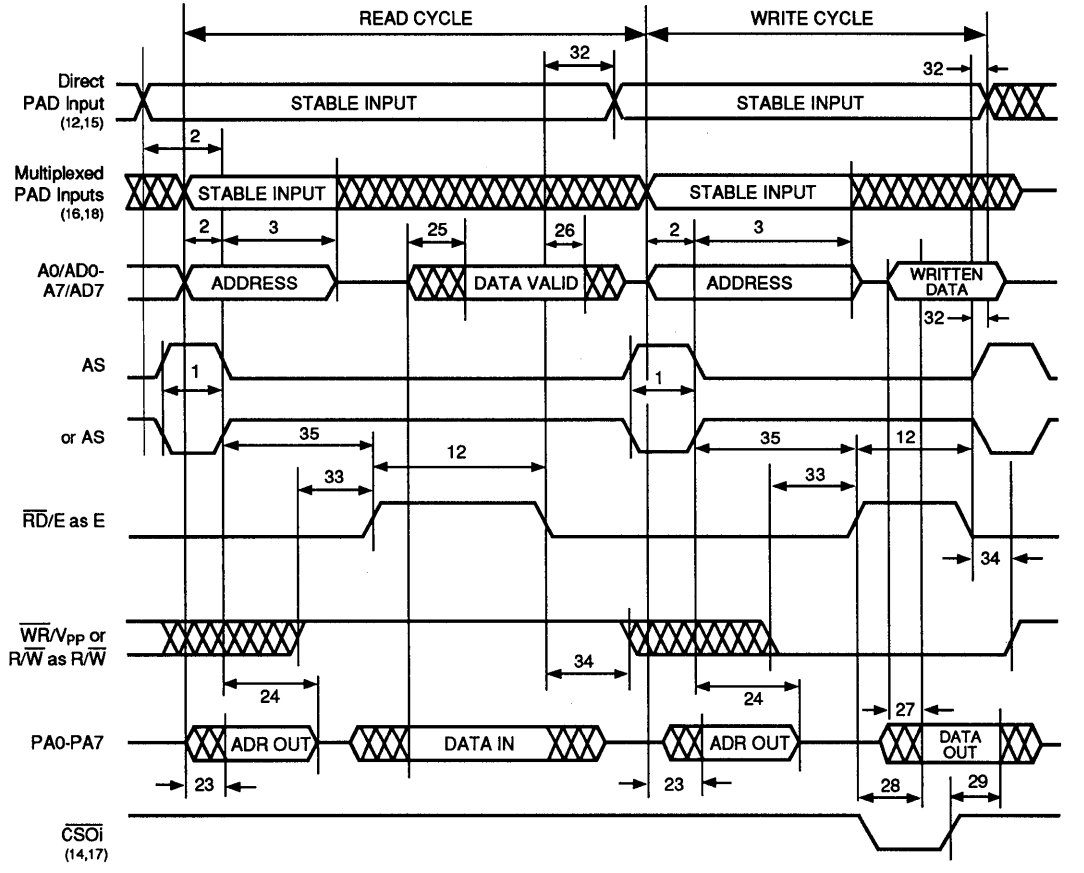
See referenced notes on page 66.

Figure 6. Port A as AD0–AD7 Timing (Track Mode), CRRWR = 0



See referenced notes on page 66.

Figure 7. Port A as AD0–AD7 Timing (Track Mode), CRRWR = 1



Notes for Timing Diagrams

12. Direct PAD input = any of the following direct PAD input lines: $\overline{CSI}$/A19 as transparent A19, $\overline{RD}$/E, $\overline{WR}$ or R/$\overline{W}$, transparent PC0–PC2, ALE in non-multiplexed modes.
13. Multiplexed inputs: any of the following inputs that are latched by the ALE (or AS): A0/AD0–A15/AD15, $\overline{CSI}$/A19 as ALE dependent A19, ALE dependent PC0–PC2.
14. $\overline{CSOi}$ = any of the chip-select output signals coming through Port B ($\overline{CS0}$–$\overline{CS7}$) or through Port C ($\overline{CS8}$–$\overline{CS10}$).
15. CSADOUT1, which internally enables the address transfer to Port A, should be derived only from direct PAD input signals, otherwise the address propagation delay is slowed down.
16. CSADIN and CSADOUT2, which internally enable the data-in or data-out transfers, respectively, can be derived from any combination of direct PAD inputs and multiplexed PAD inputs.
17. The write operation signals are included in the $\overline{CSOi}$ expression.
18. Multiplexed PAD inputs: any of the following PAD inputs that are latched by the ALE (or AS) in the multiplexed modes: A11/AD11–A15/AD15, $\overline{CSI}$/A19 as ALE dependent A19, ALE dependent PC0–PC2.
19. $\overline{CSOi}$ product terms can include any of the PAD input signals except for reset and $\overline{CSI}$.

Pin Capacitance[20]

Symbol	Parameter	Conditions	Typical[21]	Max	Unit
C_{IN}	Capacitance (for input pins only)	V_{IN} = 0 V	4	6	pF
C_{OUT}	Capacitance (for input/output pins)	V_{OUT} = 0 V	8	12	pF
C_{VPP}	Capacitance (for WR/V_{PP} or R/W/V_{PP})	V_{PP} = 0 V	18	25	pF

NOTES: 20. This paramter is only sampled and is not 100% tested.
21. Typical values are for T_A = 25°C and nominal supply voltages.

Figure 8. AC Testing Input/Output Waveform

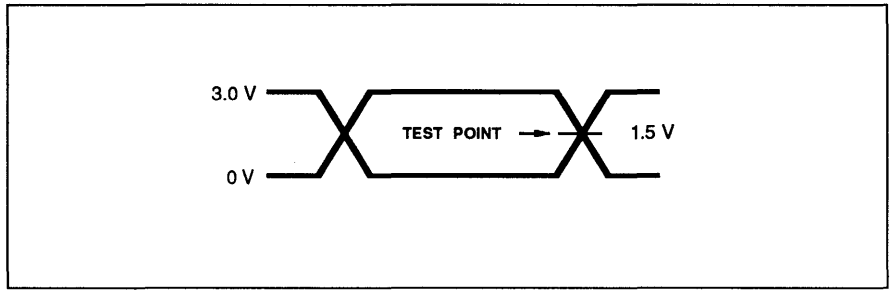
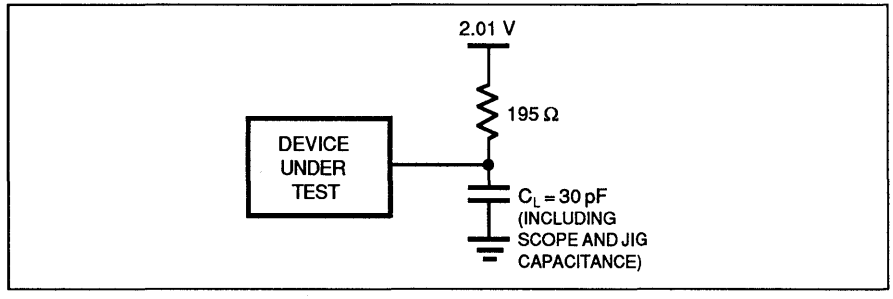


Figure 9. AC Testing Load Circuit



Erasure and Programming

To clear all locations of their programmed contents, expose the device to ultra-violet light source. A dosage of 15 W second/cm^2 is required. This dosage can be obtained with exposure to a wavelength of 2537 Å and intensity of 12000 µW/cm^2 for 15 to 20 minutes. The device should be about 1 inch from the source, and all filters should be removed from the UV light source prior to erasure.

The PSD3XX and similar devices will erase with light sources having wavelengths shorter than 4000 Å. Although the erasure times will be much longer than with UV sources at 2537 Å, exposure to fluorescent light and sunlight eventually erases the device. For maximum system reliability, these sources should be avoided. If used in such an environment, the package windows should be covered by an opaque substance.

Upon delivery, or after each erasure, the PSD3XX device has all bits in the PAD and EPROM in the "1" or high state. The configuration bits are in the "0" or low state. The code, configuration, and PAD MAP data are loaded through the procedure of programming

Pin Assignments

Pin Name	44-Pin PLCC/CLCC Package	52-Pin PQFP Package
$\overline{PSEN}$	1	46
$\overline{WR}/V_{PP}$ or R/$\overline{W}$	2	47
RESET	3	48
PB7	4	49
PB6	5	50
PB5	6	51
PB4	7	2
PB3	8	3
PB2	9	4
PB1	10	5
PB0	11	6
GND	12	7
ALE or AS	13	8
PA7	14	9
PA6	15	10
PA5	16	11
PA4	17	12
PA3	18	15
PA2	19	16
PA1	20	17
PA0	21	18
$\overline{RD}$/E	22	19
AD0/A0	23	20
AD1/A1	24	21
AD2/A2	25	22
AD3/A3	26	23
AD4/A4	27	24
AD5/A5	28	25
AD6/A6	29	28
AD7/A7	30	29
A8	31	30
A9	32	31
A10	33	32
GND	34	33
A11	35	34
A12	36	35
A13	37	36
A14	38	37
A15	39	38
PC0	40	41
PC1	41	42
PC2	42	43
A19/$\overline{CSI}$	43	44
V_{CC}	44	45

NOTE: 36. Pins 1, 13, 14, 26, 27, 39, 40, and 52 are No Connect.

Package Information

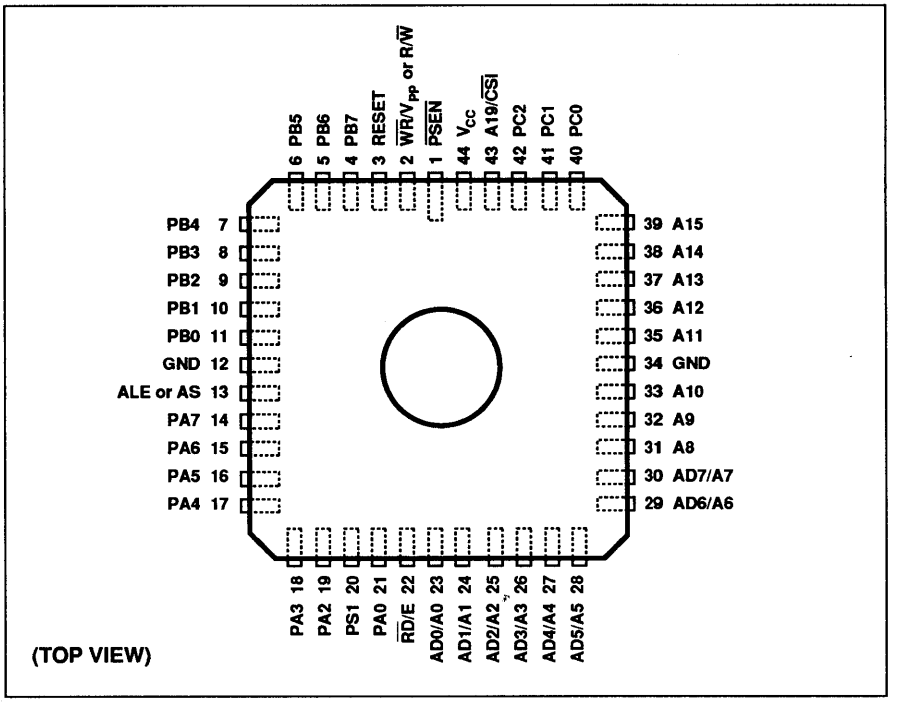


Figure 10. Drawing L4 – 44 Pin Ceramic Leaded Chip Carrier (CLCC) with Window (Package Type L)

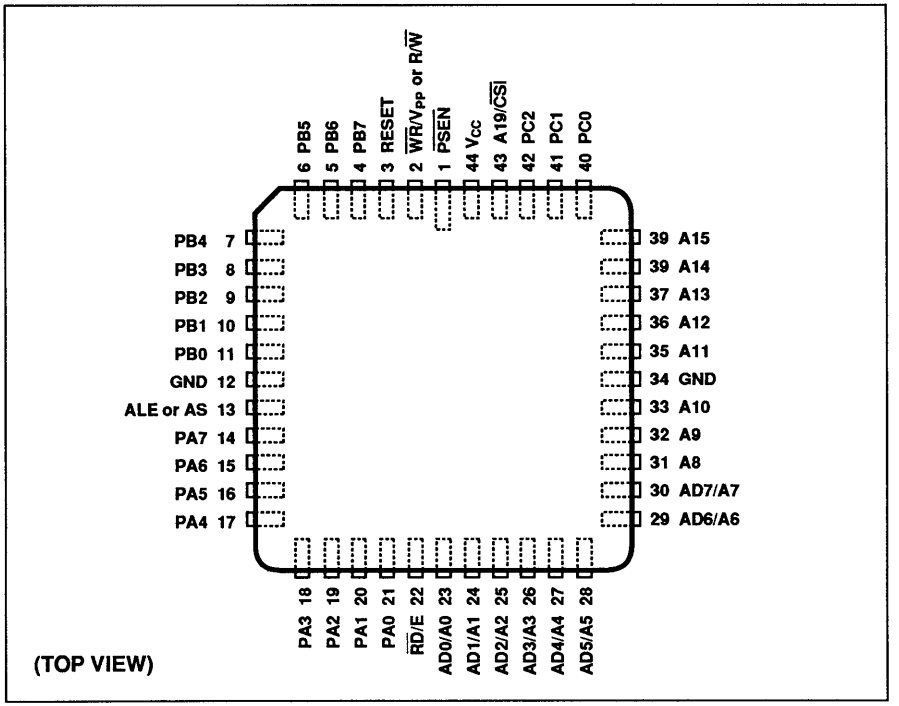
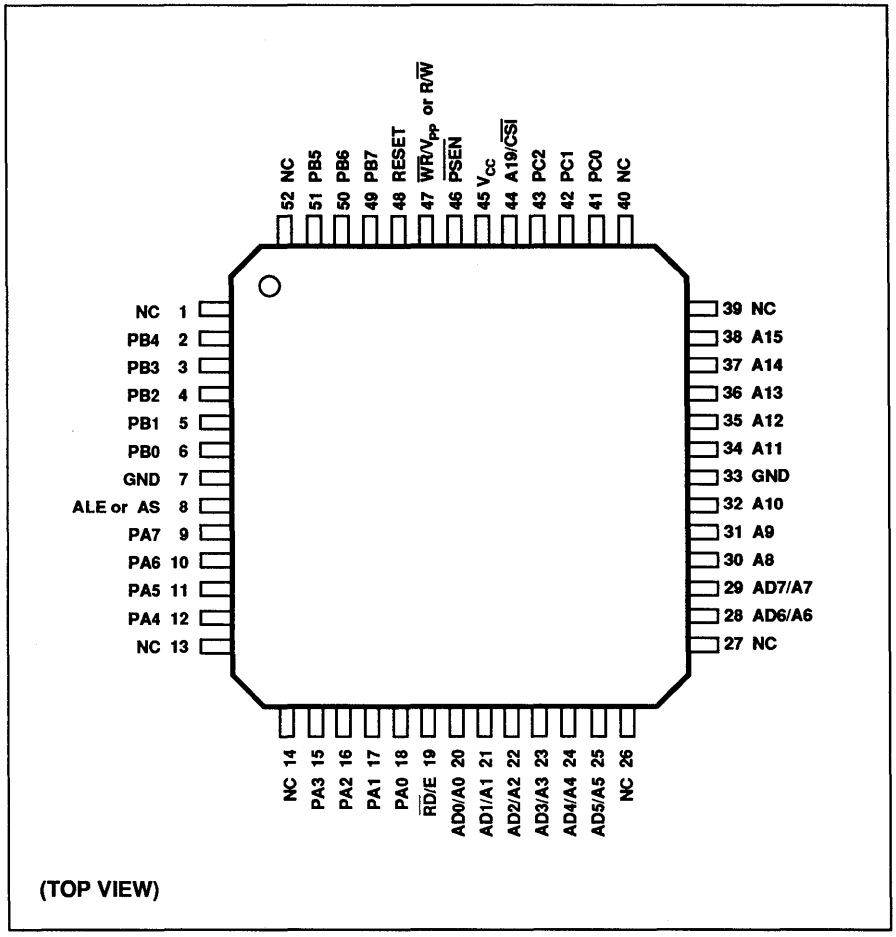


Figure 11. Drawing J2 – 44 Pin Plastic Leaded Chip Carrier (PLCC) (Package Type J)

Figure 12. Drawing Q2 – 52 Pin PQFP (Package Type Q)



Ordering Information

Part Number	Spd. (ns)	Package Type	Package Drawing	Operating Temperature Range	Manufacturing Procedure
PSD311-90 A	90	44-pin PLCC	J2	Commercial	Standard
PSD311-90 KA	90	44-pin CLCC	L4	Commercial	Standard
PSD311-12 A	120	44-pin PLCC	J2	Commercial	Standard
PSD311-12 KA	120	44-pin CLCC	L4	Commercial	Standard
PSD311-12 B	120	52-pin PQFP	Q2	Commercial	Standard
PSD311-15 A	150	44-pin PLCC	J2	Commercial	Standard
PSD311-15I A	150	44-pin PLCC	J2	Industrial	Standard
PSD311-15 KA	150	44-pin CLCC	L4	Commercial	Standard
PSD311-15I KA	150	44-pin CLCC	L4	Industrial	Standard
PSD311-15 B	150	52-pin PQFP	Q2	Commercial	Standard
PSD311-15I B	150	52-pin PQFP	Q2	Industrial	Standard
PSD311-20 A	200	44-pin PLCC	J2	Commercial	Standard
PSD311-20I A	200	44-pin PLCC	J2	Industrial	Standard
PSD311-20 KA	200	44-pin CLCC	L4	Commercial	Standard
PSD311-20I KA	200	44-pin CLCC	L4	Industrial	Standard
PSD311-20 B	200	52-pin PQFP	Q2	Commercial	Standard
PSD311-20I B	200	52-pin PQFP	Q2	Industrial	Standard

Field-programmable microcontroller peripheral — PSD302

Key Features

- Single Chip Programmable Peripheral for Microcontroller-based Applications
- 19 Individually Configurable I/O pins that can be used as:
  - Microcontroller I/O port expansion
  - Programmable Address Decoder (PAD) I/O
  - Latched address output
  - Open drain or CMOS
- Two Programmable Arrays (PAD A & PAD B)
  - Total of 40 Product Terms and up to 16 Inputs and 24 Outputs
  - Direct Address Decoding up to 1 Meg address space and up to 16 Meg with paging
  - Logic replacement
- "No Glue" Microcontroller Chip-Set
  - Built-in address latches for multiplexed address/data bus
  - Non-multiplexed address/data bus mode
  - Selectable 8 or 16 bit data bus width
  - ALE and Reset polarity programmable
  - Selectable modes for read and write control bus as $\overline{RD}/\overline{WR}$, $R/\overline{W}/E$, or $R/\overline{W}/\overline{DS}$
  - $\overline{BHE}$ pin for byte select in 16-bit mode
  - $\overline{PSEN}$ pin for 8051 users
- Built-In Page Logic
  - To Expand the Address Space of Microcontrollers with Limited Address Space Capabilities
  - Up to 16 pages
- 512 Kbits of UV EPROM
  - Configurable as 64K x 8 or as 32K x 16
  - Divides into 8 equal mappable blocks for optimized mapping
  - Block resolution is 8K x 8 or 4K x 16
  - 120 ns EPROM access time, including input latches and PAD address decoding.
- 16 Kbit Static RAM
  - Configurable as 2K x 8 or as 1K x 16
  - 120 ns SRAM access time, including input latches and PAD address decoding
- Address/Data Track Mode
  - Enables easy Interface to Shared Resources (e.g., Mail Box SRAM) with other Microcontrollers or a Host Processor
- CMiser-Bit
  - Programmable option to further reduce power consumption
- Built-In Security
  - Locks the PSD302 and PAD Decoding Configuration
- Available in a Choice of Packages
  - 44 Pin PLCC and CLCC
  - 52 Pin PQFP
- Simple Menu-Driven Software: Configure the PSD302 on an IBM PC
- Pin and Function Compatible with the PSD301

Security Mode

Security Mode in the PSD3XX locks the contents of the PAD A , PAD B and all the configuration bits. The EPROM, SRAM, and I/O contents can be accessed only through the PAD. The Security Mode can be set by the MAPLE or Programming software. In window packages, the mode is erasable through UV full part erasure. In the security mode, the PSD3XX contents cannot be copied on a programmer.

CMiser-Bit

The CMiser-Bit provides a programmable option for power-sensitive applications that require further reduction in power consumption. The CMiser-Bit (CMiser = 1) in the Maple portion of the PSD3XX sytem development software can be used to reduce power consumption. The CMiser-Bit turns off the EPROM blocks in the PSD3XX whenever the EPROM is not accessed, thereby reducing the active current consumed by the PSD3XX.

In the default mode, or if the PSD3XX is configured without programming the CMiser-Bit (CMiser = 0), the device operates at specified speed and power rating as specified in the A.C. and D.C. Characteristics.

However, if the CMiser-Bit is programmed (CMiser = 1), the device consumes even lower current, and is reflected in the data sheet. This mode has an adder in propagation delay in T5, T6, and T7 parameters in the A.C. Characteristics, and should be added to compute worst-case timing requirements in the application.

Absolute Maximum Ratings[1]

Symbol	Parameter	Condition	Min	Max	Unit
T_{STG}	Storage Temperature	CERDIP	– 65	+ 150	°C
		PLASTIC	– 65	+ 125	°C
	Voltage on any Pin	With Respect to GND	– 0.6	+ 7	V
V_{PP}	Programming Supply Voltage	With Respect to GND	– 0.6	+ 14	V
V_{CC}	Supply Voltage	With Respect to GND	– 0.6	+ 7	V
	ESD Protection			>2000	V

NOTE: 1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at theses or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods of time may affect device reliability.

Operating Range

Range	Temperature	V_{CC}	V_{CC} Tolerance		
			-12	-15	-20
Commercial	0° C to +70°C	+ 5 V	± 10%	± 10%	± 10%
Industrial	–40° C to +80°C	+ 5 V		± 10%	± 10%
Military	–55° C to +125°C	+ 5 V			± 10%

Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	Supply Voltage	All Speeds	4.5	5	5.5	V
V_{IH}	High-level Input Voltage	V_{CC} = 4.5 V to 5.5 V	2			V
V_{IL}	Low-level Input Voltage	V_{CC} = 4.5 V to 5.5 V	0		0.8	V

DC Characteristics

Symbol	Parameter	Conditions				CMiser = 1 Subtract:			Unit
			Min	Typ	Max	Min	Typ	Max	
V_{OL}	Output Low Voltage	I_{OL} = 20 µA V_{CC} = 4.5 V		0.01	0.1				V
		I_{OL} = 8 mA V_{CC} = 4.5 V		0.15	0.45				V
V_{OH}	Output High Voltage	I_{OH} = –20 µA V_{CC} = 4.5 V	4.4	4.49					V
		I_{OH} = –2 mA V_{CC} = 4.5 V	2.4	3.9					V
I_{SB1}	V_{CC} Standby Current (CMOS) (Notes 2 and 4)	Comm'l		50	100				µA
		Ind/Mil		75	150				µA
I_{CC1}	Active Current (CMOS) (No Internal Memory Block Selected) (Notes 2 and 5)	Comm'l (Note 6)		16	35		7	10	mA
		Comm'l (Note 7)		28	50		7	10	mA
		Ind/Mil (Note 6)		16	45		7	10	mA
		Ind/Mil (Note 7)		28	60		7	10	mA
I_{CC2}	Active Current (CMOS) (EPROM Block Selected) (Notes 2 and 5)	Comm'l (Note 6)		16	35		0	0	mA
		Comm'l (Note 7)		28	50		0	0	mA
		Ind/Mil (Note 6)		16	45		0	0	mA
		Ind/Mil (Note 7)		28	60		0	0	mA
I_{CC3}	Active Current (CMOS) (SRAM Block Selected (Notes 2 and 5)	Comm'l (Note 6)		47	80		7	10	mA
		Comm'l (Note 7)		59	95		7	10	mA
		Ind/Mil (Note 6)		47	100		7	10	mA
		Ind/Mil (Note 7)		59	115		7	10	mA
I_{LI}	Input Leakage Current	V_{IN} = 5.5 V or GND	–1	±0.1	1				µA
I_{LO}	Output Leakage Current	V_{OUT} = 5.5 V or GND	–10	±5	10				µA

NOTES: 2. CMOS inputs: GND ± 0.3 V or V_{CC} ± 0.3V.
3. TTL inputs: $V_{IL} \leq 0.8$ V, $V_{IH} \geq 2.0$ V.
4. $\overline{CSI}$/A19 is high and the part is in a power-down configuration mode.
5. Add 3.0 mA/MHz for AC power component (power = AC + DC).
6. Ten (10) PAD product terms active. (Add 380 µA per product term, typical, or 480 µA per product term maximum
7. Forty-one (41) PAD product terms active.

AC Characteristics

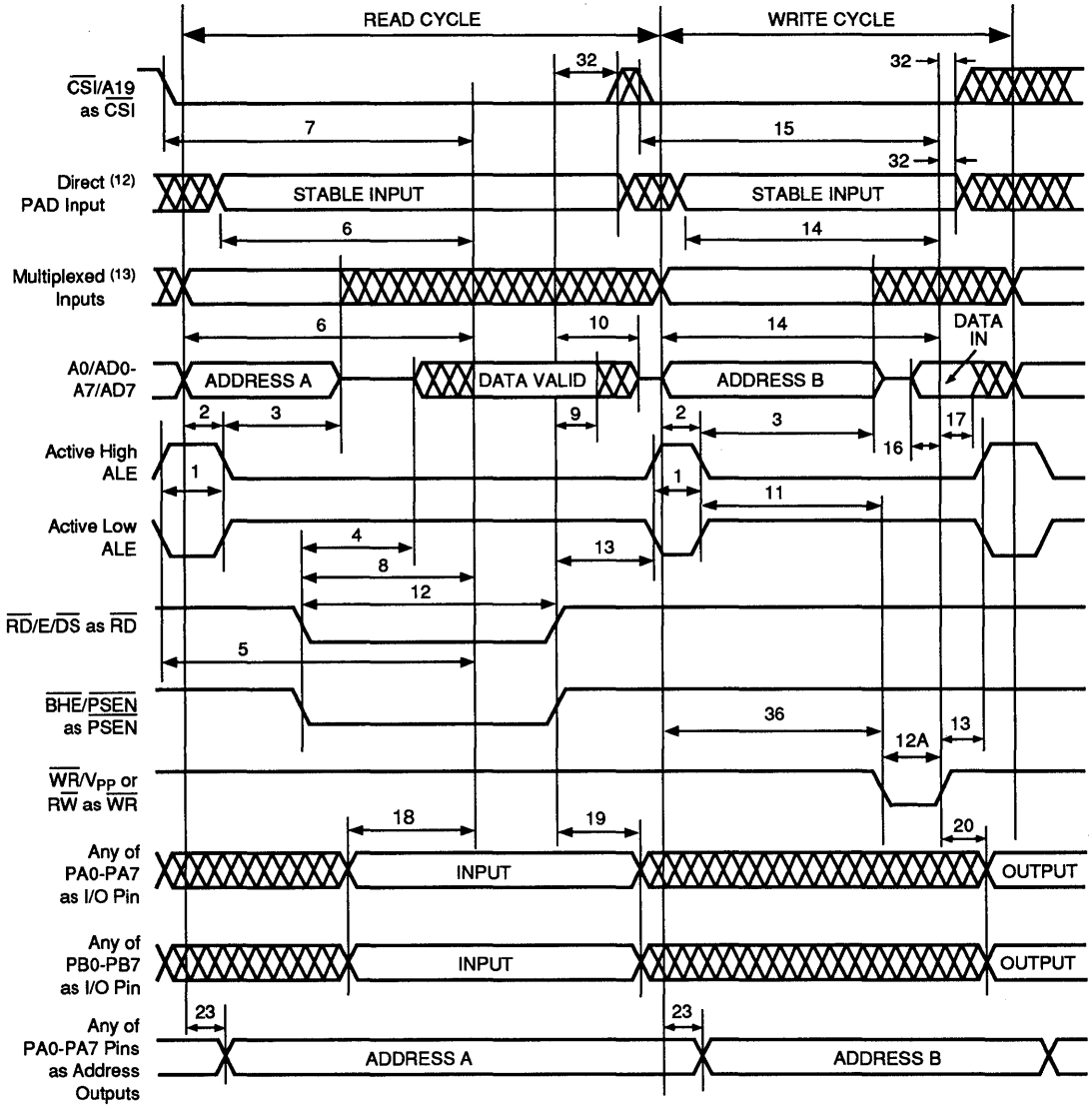
Symbol	Parameter	-90		-12		-15		-20		CMiser = 1 Add:	Unit
		Min	Max	Min	Max	Min	Max	Min	Max		
T1	ALE or AS Pulse Width	20		30		40		50		0	ns
T2	Address Set-up Time	5		9		12		15		0	ns
T3	Address Hold Time	8		9		12		15		0	ns
T4	Leading Edge of Read to Data Active	0		0		0		0		0	ns
T5	ALE Valid to Data Valid		100		130		160		200	10	ns
T6	Address Valid to Data Valid		90		120		150		200	10	ns
T7	$\overline{CSI}$ Active to Data Valid		100		130		160		200	15	ns
T8	Leading Edge of Read to Data Valid		32		38		55		60	0	ns
T9	Read Data Hold Time	0		0		0		0		0	ns
T10	Trailing Edge of Read to Data High-Z		32		32		35		40	0	ns
T11	Trailing Edge of ALE or AS to Leading Edge of Write	0		0		0		0		0	ns
T12	$\overline{RD}$, E, $\overline{PSEN}$, or $\overline{DS}$ Pulse Width	40		45		60		75		0	ns
T12A	$\overline{WR}$ Pulse Width	20		25		35		45		0	ns
T13	Trailing Edge of Write or Read to Leading Edge of ALE or AS	0		0		0		0		0	ns
T14	Address Valid to Trailing Edge of Write	90		120		150		200		0	ns
T15	$\overline{CSI}$ Active to Trailing Edge of Write	100		130		160		200		0	ns
T16	Write Data Set-up Time	20		25		30		40		0	ns
T17	Write Data Hold Time	5		5		10		15		0	ns
T18	Port to Data Out Valid Propagation Delay		30		30		35		45	0	ns
T19	Port Input Hold Time	0		0		0		0		0	ns
T20	Trailing Edge of Write to Port Output Valid	40		40		50		60		0	ns
T21	ADi or Control to $\overline{CSOi}$ Valid	6	25	6	30	6	35	5	45	0	ns
T22	ADi or Control to $\overline{CSOi}$ Invalid	5	25	5	30	4	35	4	45	0	ns

AC Characteristics (Cont.)

Symbol	Parameter	-90		-12		-15		-20		CMiser = 1 Add:*	Unit
		Min	Max	Min	Max	Min	Max	Min	Max		
T23	Track Mode Address Propagation Delay: CSADOUT1 Already True		22		22		28		28	0	ns
T23A	Track Mode Address Propagation Delay: CSADOUT1 Becomes True During ALE or AS		33		33		50		50	0	ns
T24	Track Mode Trailing Edge of ALE or AS to Address High-Z		32		32		35		40	0	ns
T25	Track Mode Read Propagation Delay		29		29		35		35	0	ns
T26	Track Mode Read Hold Time	11	29	11	29	10	29	10	35	0	ns
T27	Track Mode Write Cycle, Data Propagation Delay		20		20		30		30	0	ns
T28	Track Mode Write Cycle, Write to Data Propagation Delay	8	30	8	30	7	40	7	55	0	ns
T29	Hold Time of Port A Valid During Write $\overline{CSOi}$ Trailing Edge	2		2		2		2		0	ns
T30	$\overline{CSI}$ Active to $\overline{CSOi}$ Active	9	40	9	45	9	50	8	60	0	ns
T31	$\overline{CSI}$ Inactive to $\overline{CSOi}$ Inactive	9	40	9	45	9	50	8	60	0	ns
T32	Direct PAD Input as Hold Time	10		10		12		15		0	ns
T33	R/$\overline{W}$ Active to E or $\overline{DS}$ Start	20		20		30		40		0	ns
T34	E or $\overline{DS}$ End to R/$\overline{W}$	20		20		30		40		0	ns
T35	AS Inactive to E high	0		0		0		0		0	ns
T36	Address to Leading Edge of Write	20		20		25		30		0	ns

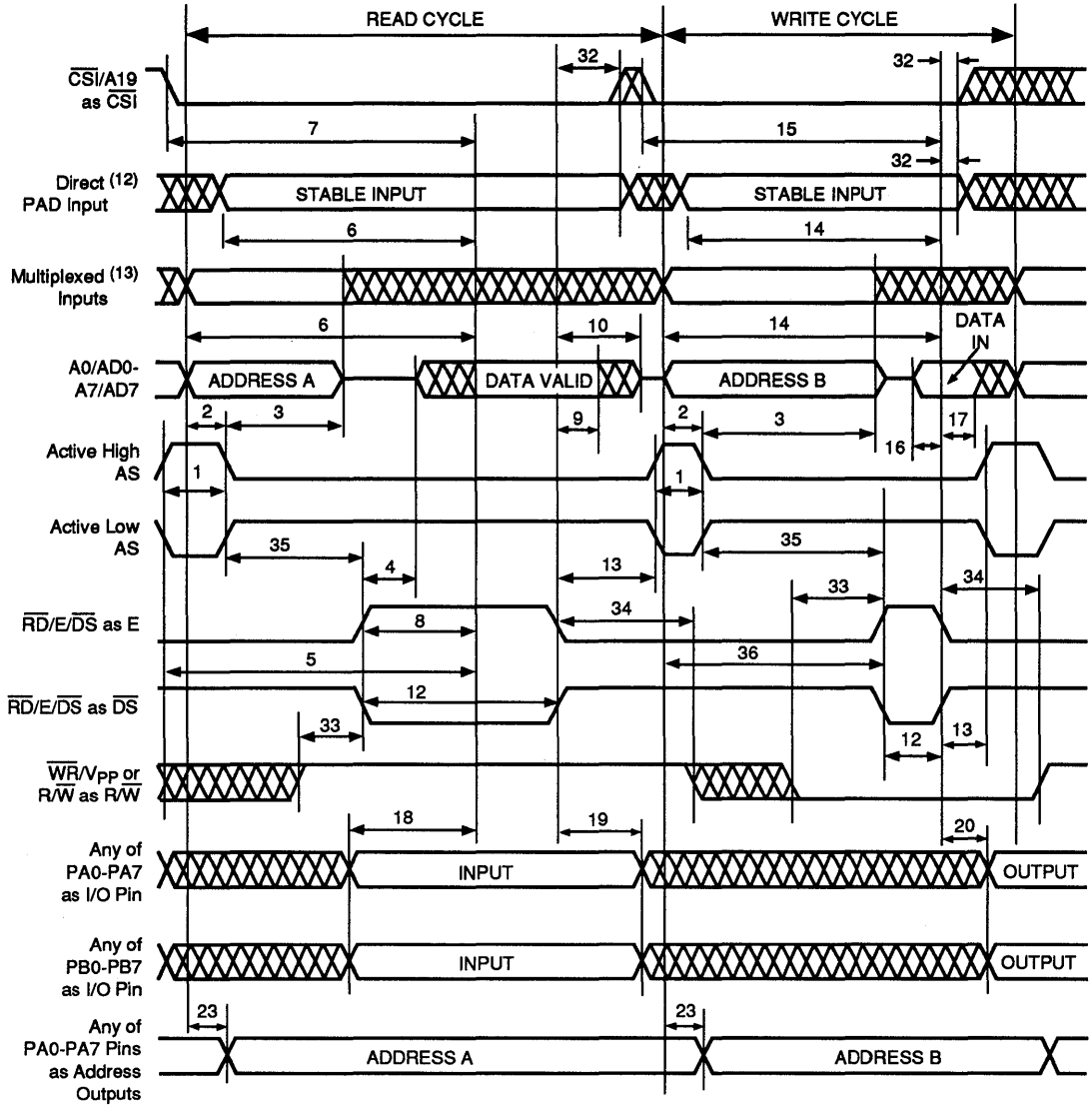
NOTES: 8. ADi = any address line.
9. $\overline{CSOi}$ = any of the chip-select output signals coming through Port B ($\overline{CS0}$–$\overline{CS7}$) or through Port C ($\overline{CS8}$–$\overline{CS10}$).
10. Direct PAD input = any of the following direct PAD input lines: $\overline{CSI}$/A19 as transparent A19, $\overline{RD}$/E/$\overline{DS}$, $\overline{WR}$ or R/$\overline{W}$, transparent PC0–PC2, ALE (or AS).
11. Control signals $\overline{RD}$/E/$\overline{DS}$ or $\overline{WR}$ or R/$\overline{W}$.

Figure 1. Timing of 8-Bit Multiplexed Address/DataBus, CRRWR = 0



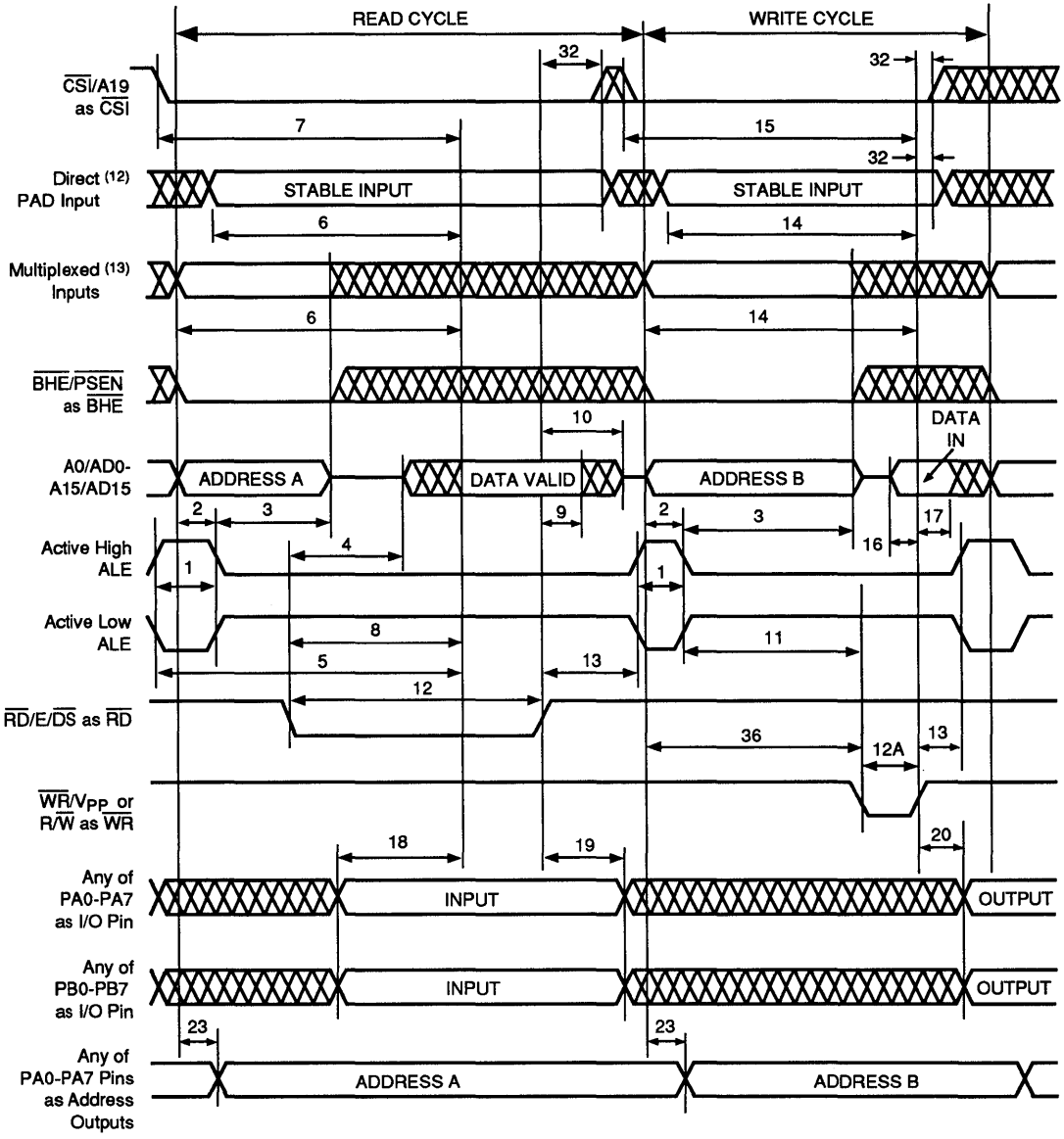
See referenced notes on page 88.

Figure 2. Timing of 8-Bit Multiplexed Address/DataBus, CRRWR = 1



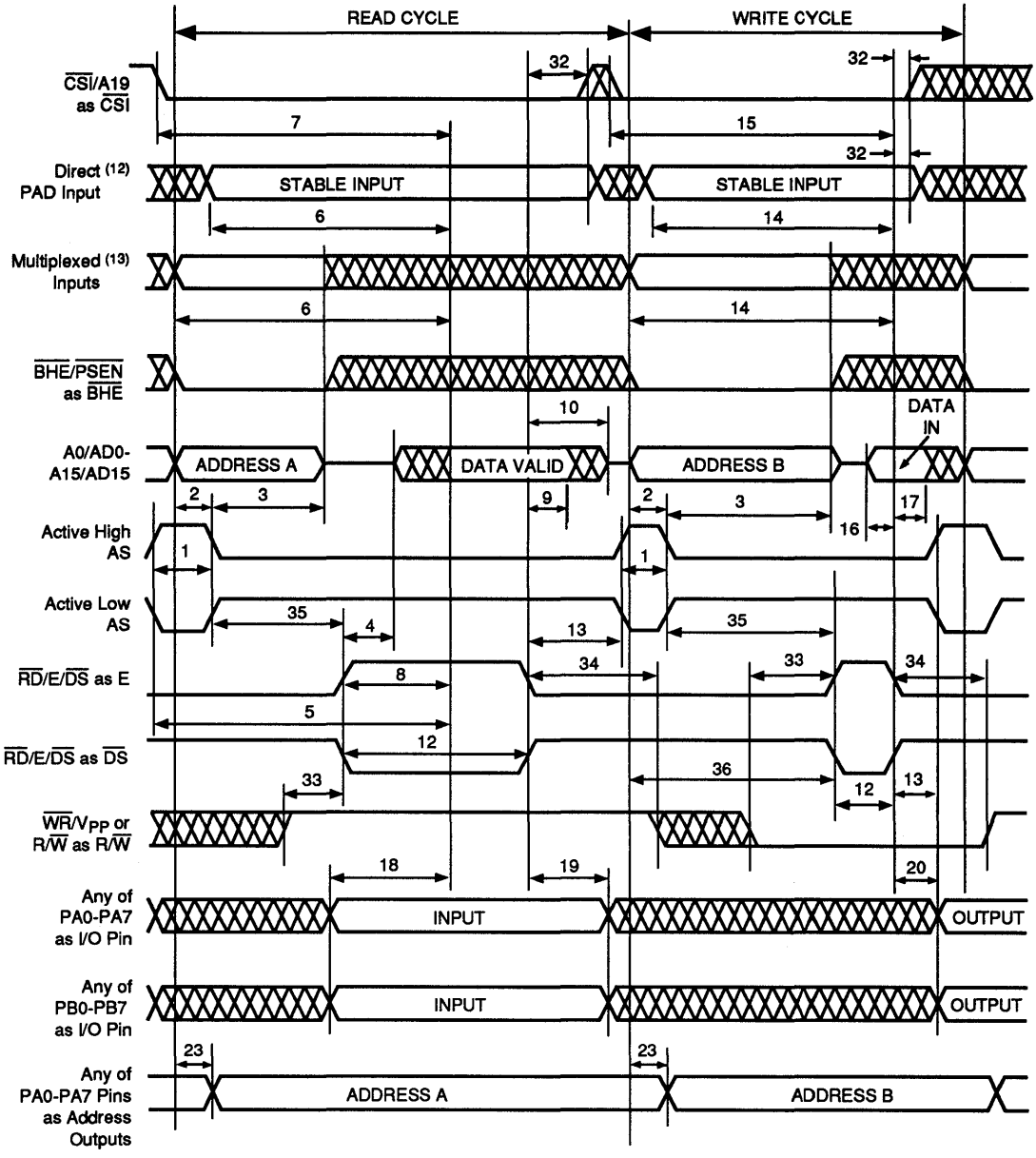
See referenced notes on page 88.

Figure 3. Timing of 16-Bit Multiplexed Address/DataBus, CRRWR = 0



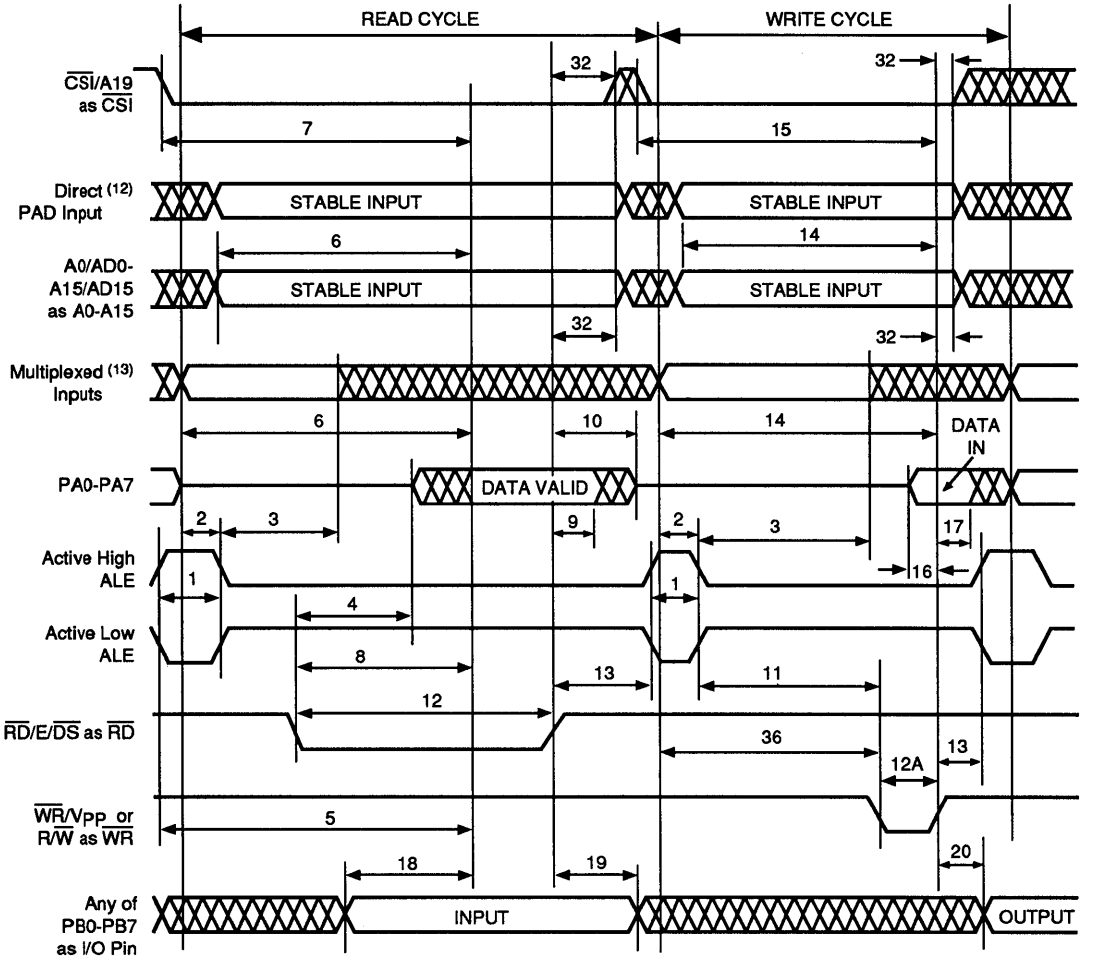
See referenced notes on page 88.

Figure 4. Timing of 16-Bit Multiplexed Address/DataBus, CRRWR = 1



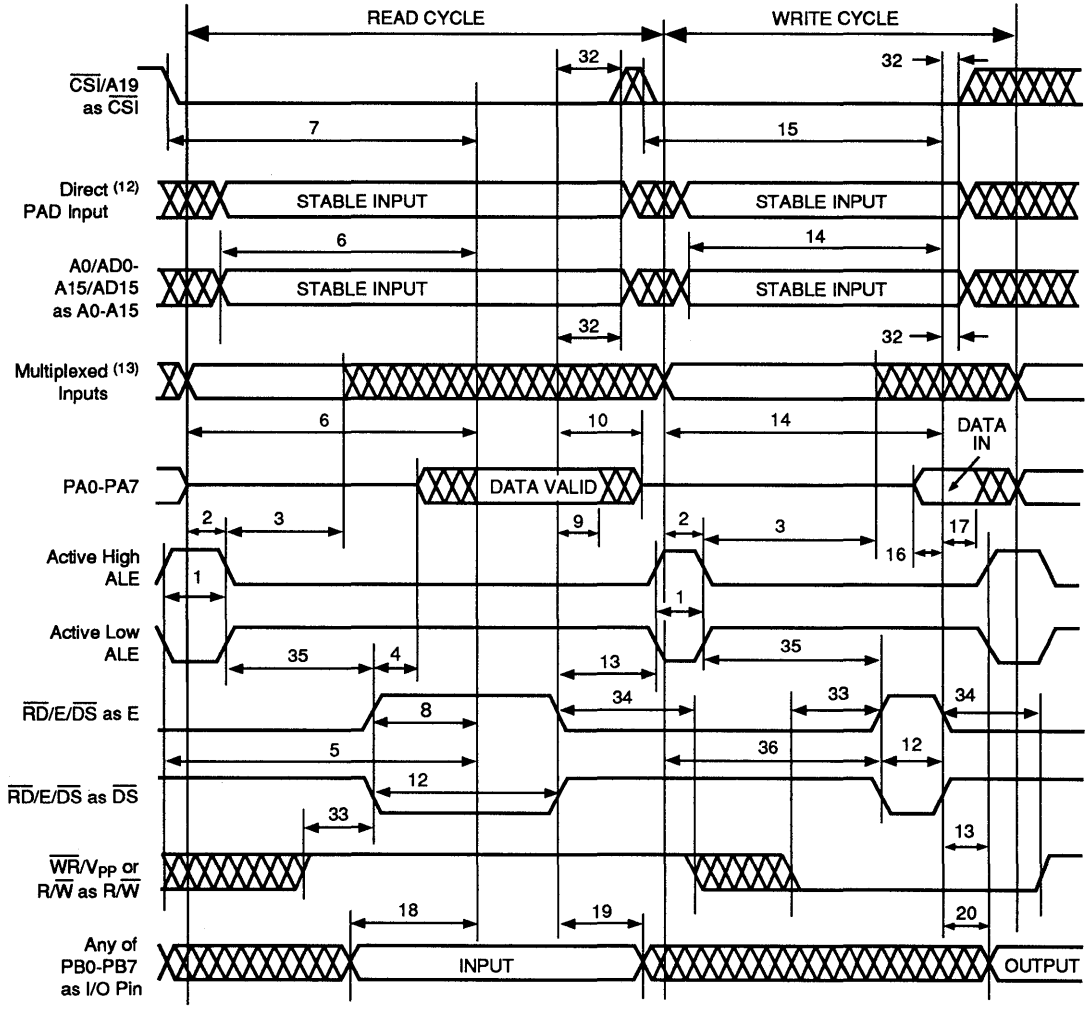
See referenced notes on page 88.

Figure 5. Timing of 8-Bit Data, Non-Multiplexed Address/DataBus, CRRWR = 0



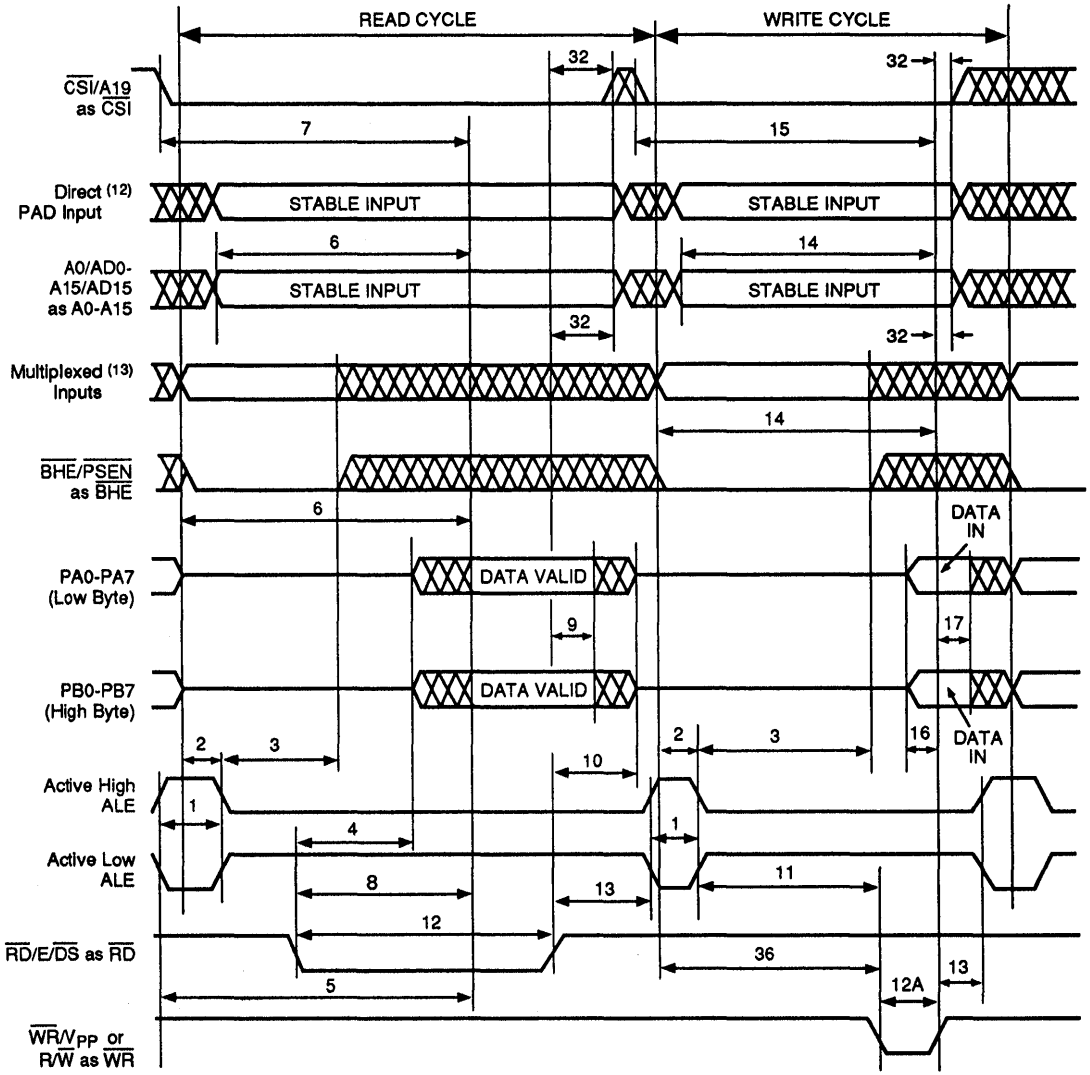
See referenced notes on page 88.

Figure 6. Timing of 8-Bit Data, Non-Multiplexed Address/DataBus, CRRWR = 1



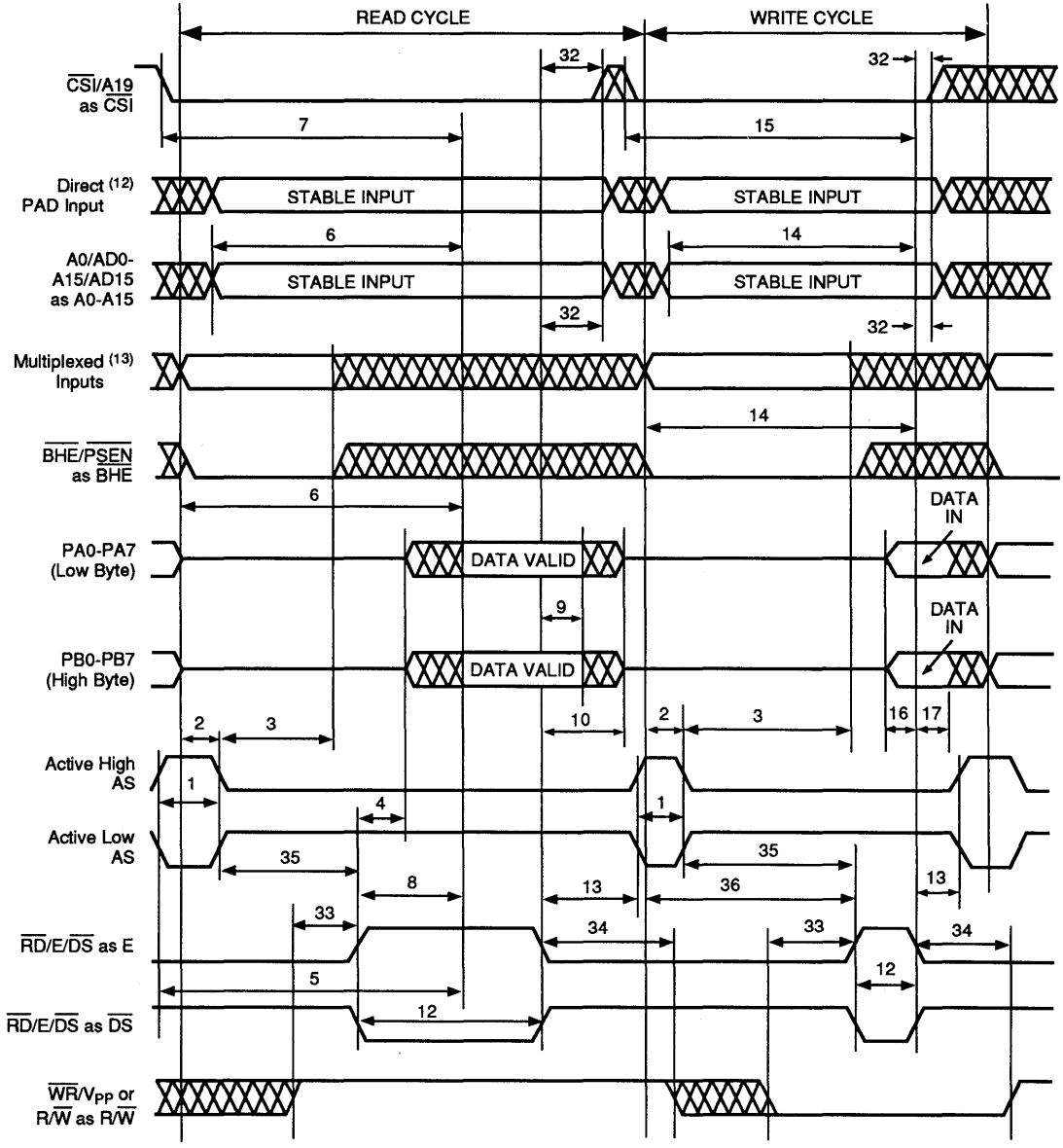
See referenced notes on page 88.

Figure 7. Timing of 16-Bit Non-Multiplexed Address/DataBus, CRRWR = 0



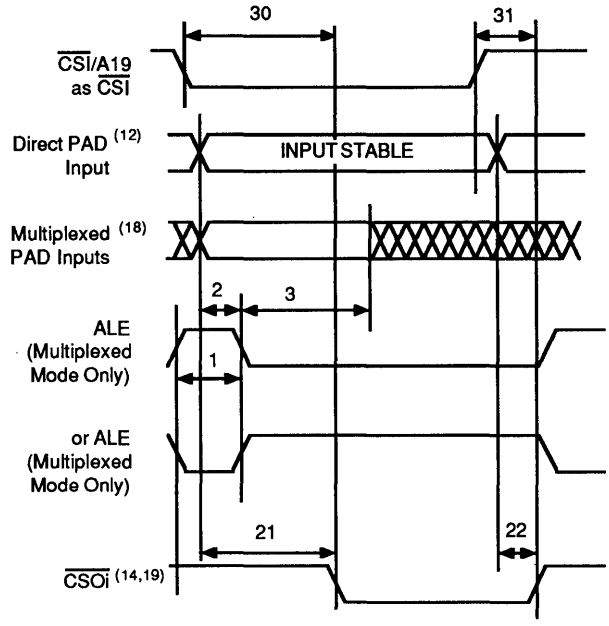
See referenced notes on page 88.

Figure 8. Timing of 16-Bit Non-Multiplexed Address/DataBus, CRRWR = 1



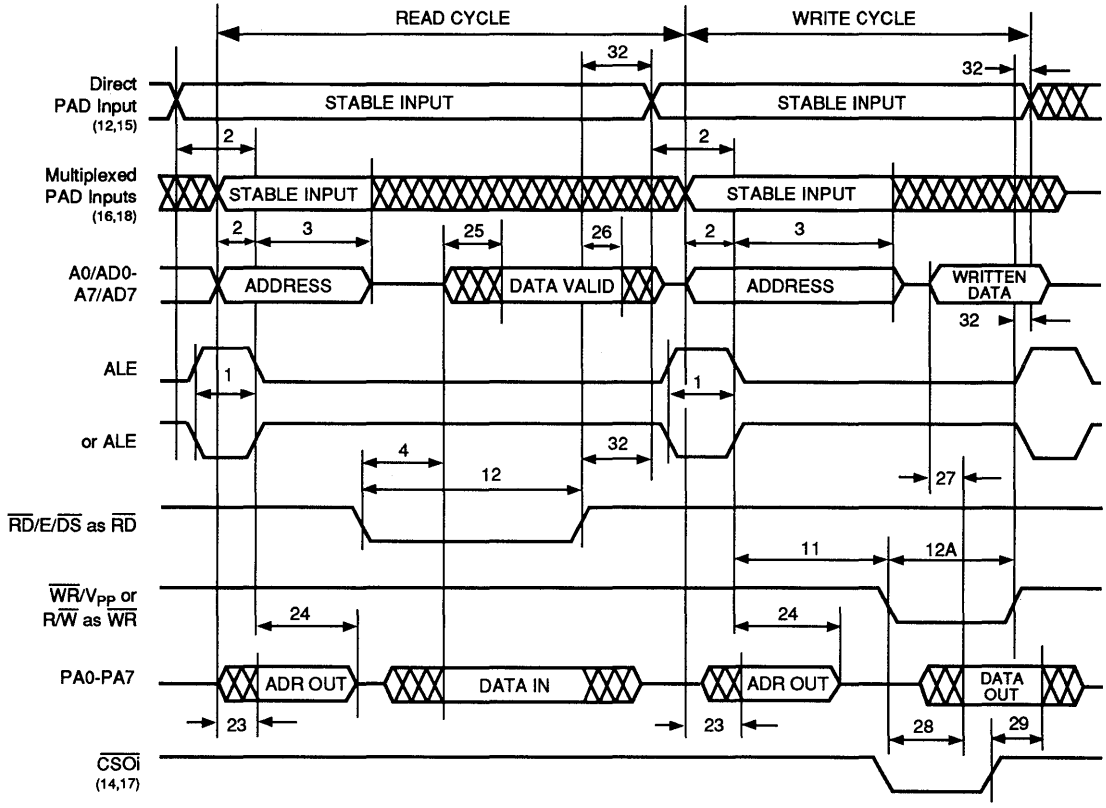
See referenced notes on page 88.

Figure 9. Chip-Select Output Timing



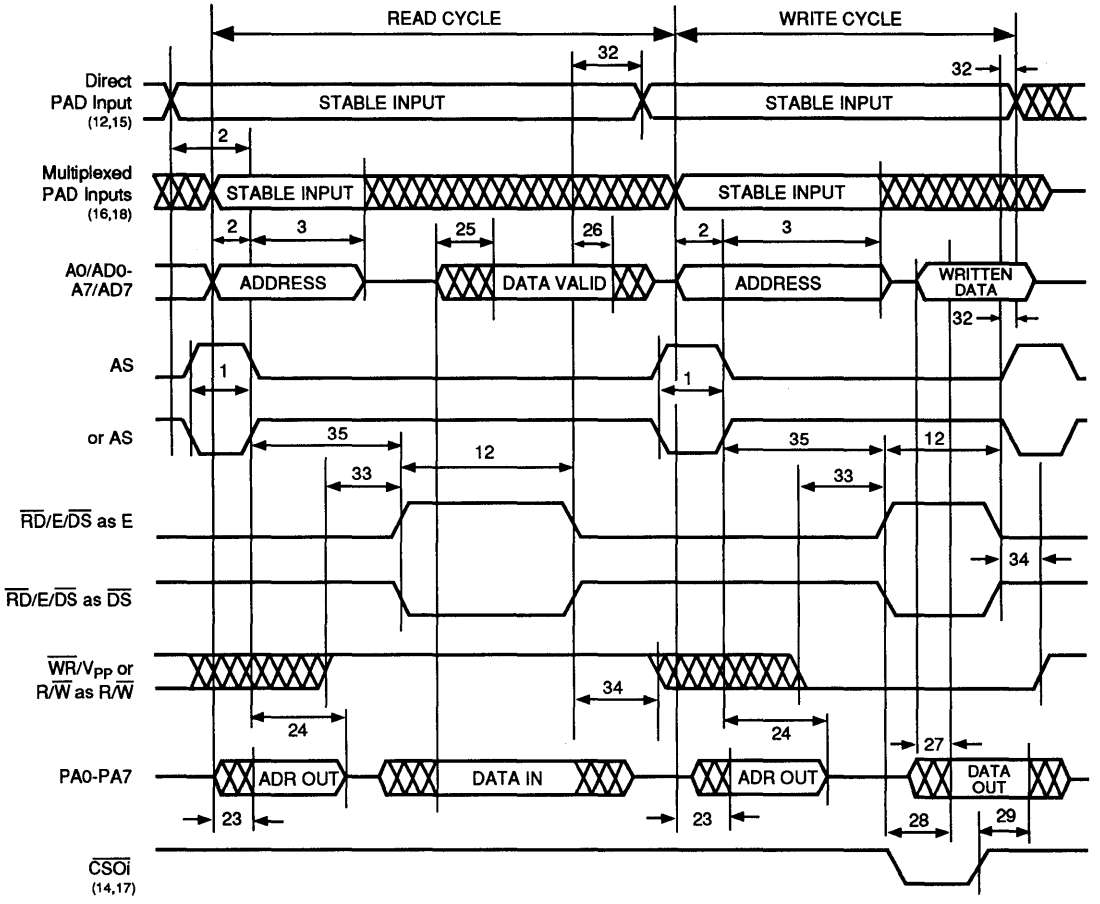
See referenced notes on page 88.

Figure 10. Port A as AD0–AD7 Timing (Track Mode), CRRWR = 0



See referenced notes on page 88.

Figure 11. Port A as AD0–AD7 Timing (Track Mode), CRRWR = 1



Notes for Timing Diagrams

12. Direct PAD input = any of the following direct PAD input lines: $\overline{CSI}$/A19 as transparent A19, $\overline{RD}$/E, $\overline{WR}$ or R/$\overline{W}$, transparent PC0–PC2, ALE in non-multiplexed modes.
13. Multiplexed inputs: any of the following inputs that are latched by the ALE (or AS): A0/AD0–A15/AD15, $\overline{CSI}$/A19 as ALE dependent A19, ALE dependent PC0–PC2.
14. $\overline{CSOi}$ = any of the chip-select output signals coming through Port B ($\overline{CS0}$–$\overline{CS7}$) or through Port C ($\overline{CS8}$–$\overline{CS10}$).
15. CSADOUT1, which internally enables the address transfer to Port A, should be derived only from direct PAD input signals, otherwise the address propagation delay is slowed down.
16. CSADIN and CSADOUT2, which internally enable the data-in or data-out transfers, respectively, can be derived from any combination of direct PAD inputs and multiplexed PAD inputs.
17. The write operation signals are included in the $\overline{CSOi}$ expression.
18. Multiplexed PAD inputs: any of the following PAD inputs that are latched by the ALE (or AS) in the multiplexed modes: A11/AD11–A15/AD15, $\overline{CSI}$/A19 as ALE dependent A19, ALE dependent PC0–PC2.
19. $\overline{CSOi}$ product terms can include any of the PAD input signals except for reset and $\overline{CSI}$.

Pin Capacitance[20]

Symbol	Parameter	Conditions	Typical[21]	Max	Unit
C_{IN}	Capacitance (for input pins only)	V_{IN} = 0 V	4	6	pF
C_{OUT}	Capacitance (for input/output pins)	V_{OUT} = 0 V	8	12	pF
C_{VPP}	Capacitance (for WR/V_{PP} or R/W/V_{PP})	V_{PP} = 0 V	18	25	pF

NOTES: 20. This paramter is only sampled and is not 100% tested.
21. Typical values are for T_A = 25°C and nominal supply voltages.

Figure 12. AC Testing Input/Output Waveform

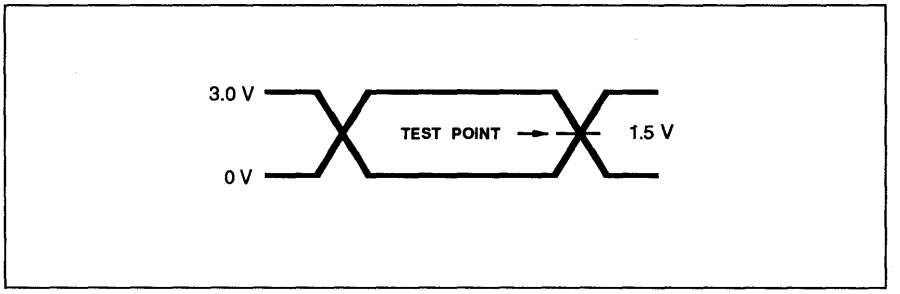
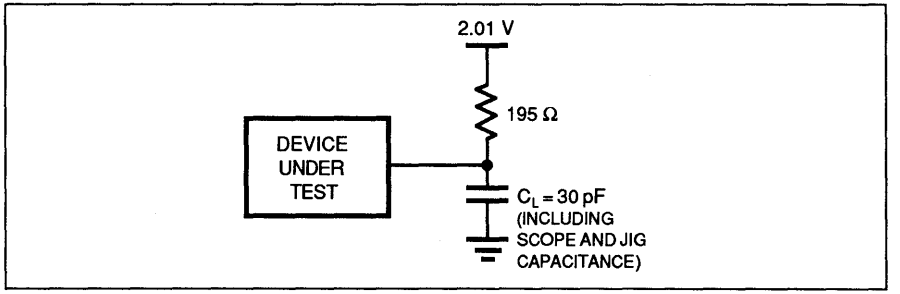


Figure 13. AC Testing Load Circuit



Erasure and Programming

To clear all locations of their programmed contents, expose the device to ultra-violet light source. A dosage of 15 W second/cm^2 is required. This dosage can be obtained with exposure to a wavelength of 2537 Å and intensity of 12000 µW/cm^2 for 15 to 20 minutes. The device should be about 1 inch from the source, and all filters should be removed from the UV light source prior to erasure.

The PSD3XX and similar devices will erase with light sources having wavelengths shorter than 4000 Å. Although the erasure times will be much longer than with UV sources at 2537 Å, exposure to fluorescent light and sunlight eventually erases the device. For maximum system reliability, these sources should be avoided. If used in such an environment, the package windows should be covered by an opaque substance.

Upon delivery, or after each erasure, the PSD3XX device has all bits in the PAD and EPROM in the "1" or high state. The configuration bits are in the "0" or low state. The code, configuration, and PAD MAP data are loaded through the procedure of programming

Pin Assignments

Pin Name	44-Pin PLCC/CLCC Package	52-Pin PQFP Package
$\overline{BHE}/\overline{PSEN}$	1	46
$\overline{WR}/V_{PP}$ or R/$\overline{W}$	2	47
RESET	3	48
PB7	4	49
PB6	5	50
PB5	6	51
PB4	7	2
PB3	8	3
PB2	9	4
PB1	10	5
PB0	11	6
GND	12	7
ALE or AS	13	8
PA7	14	9
PA6	15	10
PA5	16	11
PA4	17	12
PA3	18	15
PA2	19	16
PA1	20	17
PA0	21	18
$\overline{RD}$/E/$\overline{DS}$	22	19
AD0/A0	23	20
AD1/A1	24	21
AD2/A2	25	22
AD3/A3	26	23
AD4/A4	27	24
AD5/A5	28	25
AD6/A6	29	28
AD7/A7	30	29
AD8/A8	31	30
AD9/A9	32	31
AD10/A10	33	32
GND	34	33
AD11/A11	35	34
AD12/A12	36	35
AD13/A13	37	36
AD14/A14	38	37
AD15/A15	39	38
PC0	40	41
PC1	41	42
PC2	42	43
A19/$\overline{CSI}$	43	44
V_{CC}	44	45

NOTE: 36. Pins 1, 13, 14, 26, 27, 39, 40, and 52 are No Connect.

Package Information

Figure 14. Drawing L4 — 44 Pin Ceramic Leaded Chip Carrier (CLCC) with Window (Package Type L)

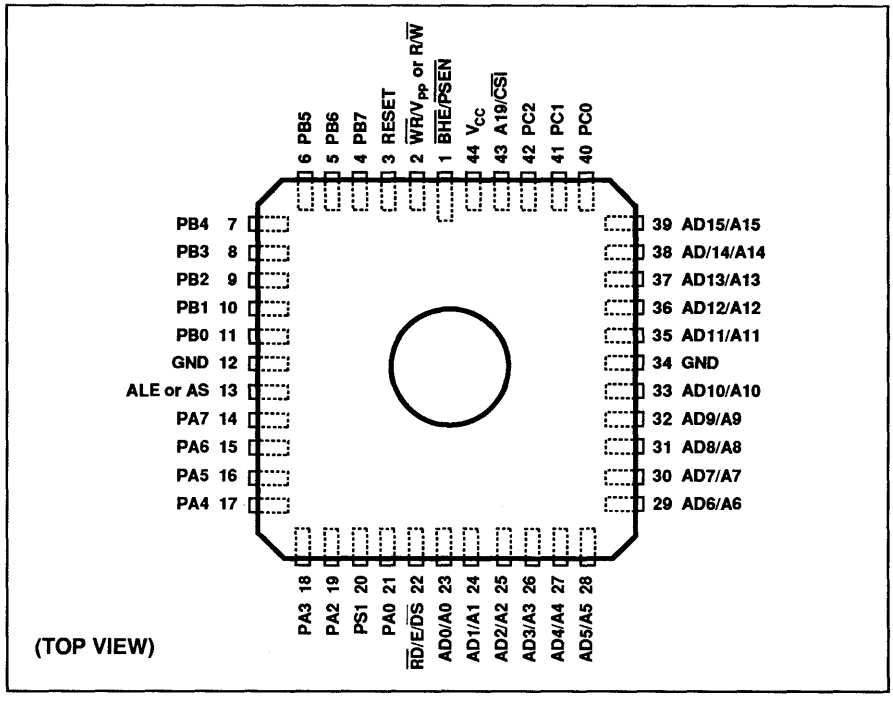


Figure 15. Drawing J2 — 44 Pin Plastic Leaded Chip Carrier (PLCC) with Window (Package Type J)

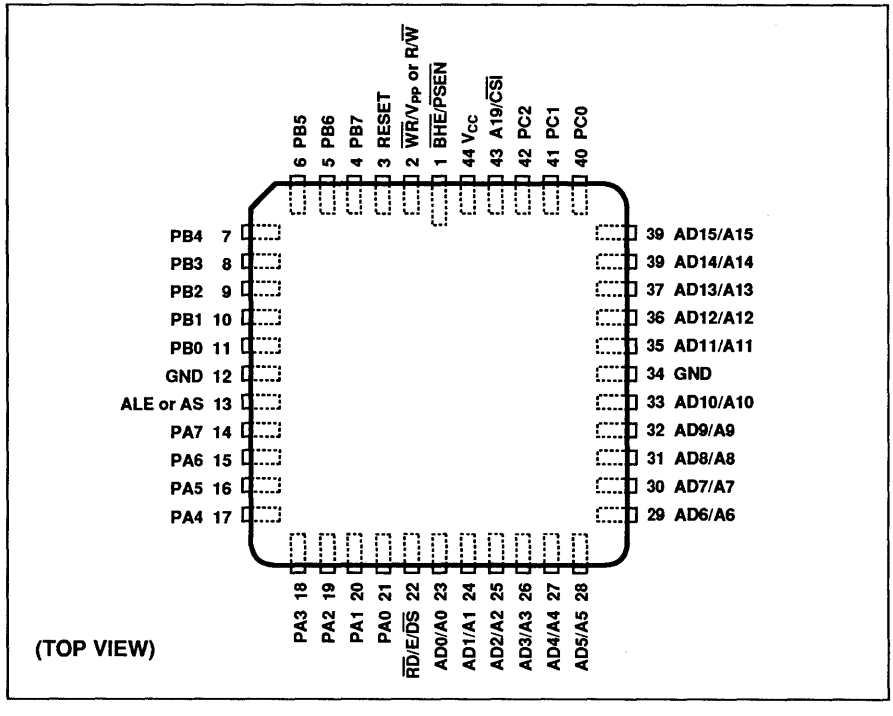
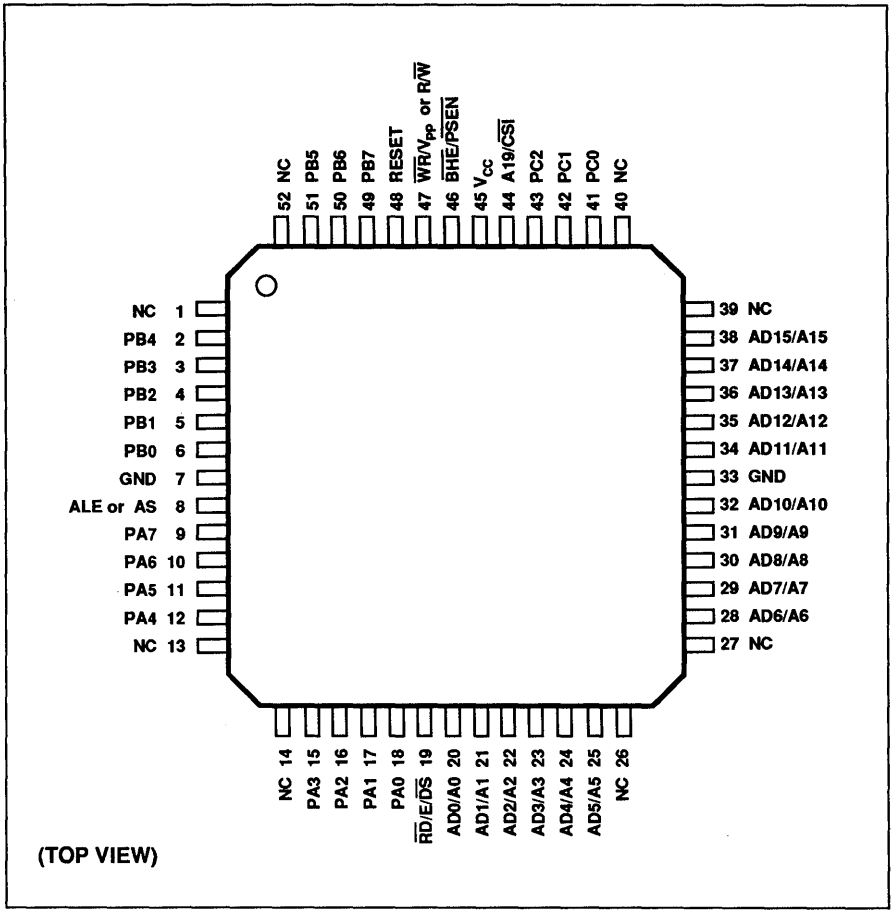


Figure 16. Drawing Q2 – 52 Pin PQFP (Package Type Q)



Ordering Information

Part Number	Spd. (ns)	Package Type	Package Drawing	Operating Temperature Range	WSI Manufacturing Procedure
PSD302-90 A	90	44-pin PLCC	J2	Commercial	Standard
PSD302-90 KA	90	44-pin CLCC	L4	Commercial	Standard
PSD302-12 A	120	44-pin PLCC	J2	Commercial	Standard
PSD302-12 KA	120	44-pin CLCC	L4	Commercial	Standard
PSD302-12 B	120	52-pin PQFP	Q2	Commercial	Standard
PSD302-15 A	150	44-pin PLCC	J2	Commercial	Standard
PSD302-15I A	150	44-pin PLCC	J2	Industrial	Standard
PSD302-15 KA	150	44-pin CLCC	L4	Commercial	Standard
PSD302-15I KA	150	44-pin CLCC	L4	Industrial	Standard
PSD302-15 B	150	52-pin PQFP	Q2	Commercial	Standard
PSD302-15I B	150	52-pin PQFP	Q2	Industrial	Standard
PSD302-20 A	200	44-pin PLCC	J2	Commercial	Standard
PSD302-20I A	200	44-pin PLCC	J2	Industrial	Standard
PSD302-20 KA	200	44-pin CLCC	L4	Commercial	Standard
PSD302-20I KA	200	44-pin CLCC	L4	Industrial	Standard
PSD302-20 B	200	52-pin PQFP	Q2	Commercial	Standard
PSD302-20I B	200	52-pin PQFP	Q2	Industrial	Standard

Field-programmable microcontroller peripheral — PSD312

Key Features

- ❑ Single Chip Programmable Peripheral for Microcontroller-based Applications
- ❑ 19 Individually Configurable I/O pins that can be used as:
  - — Microcontroller I/O port expansion
  - — Programmable Address Decoder (PAD) I/O
  - — Latched address output
  - — Open drain or CMOS
- ❑ Two Programmable Arrays (PAD A & PAD B)
  - — Total of 40 Product Terms and up to 16 Inputs and 24 Outputs
  - — Direct Address Decoding up to 1 Meg address space and up to 16 Meg with paging
  - — Logic replacement
- ❑ "No Glue" Microcontroller Chip-Set
  - — Built-in address latches for multiplexed address/data bus
  - — Non-multiplexed address/data bus mode
  - — 8-bit data bus width
  - — ALE and Reset polarity programmable
  - — Selectable modes for read and write control bus as $\overline{RD}/\overline{WR}$, R/$\overline{W}$/E, or R/$\overline{W}$/$\overline{DS}$
  - — $\overline{PSEN}$ pin for 8051 users
- ❑ Built-In Page Logic
  - — To Expand the Address Space of Microcontrollers with Limited Address Space Capabilities
  - — Up to 16 pages
- ❑ 512 Kbits of UV EPROM
  - — Configurable as 64K x 8
  - — Divides into 8 equal mappable blocks for optimized mapping
  - — Block resolution is 8K x 8
  - — 120 ns EPROM access time, including input latches and PAD address decoding.
- ❑ 16 Kbit Static RAM
  - — Configurable as 2K x 8
  - — 120 ns SRAM access time, including input latches and PAD address decoding
- ❑ Address/Data Track Mode
  - — Enables easy Interface to Shared Resources (e.g., Mail Box SRAM) with other Microcontrollers or a Host Processor
- ❑ CMiser-Bit
  - — Programmable option to further reduce power consumption
- ❑ Built-In Security
  - — Locks the PSD312 and PAD Decoding Configuration
- ❑ Available in a Choice of Packages
  - — 44 Pin PLCC and CLCC
  - — 52 Pin PQFP
- ❑ Simple Menu-Driven Software: Configure the PSD312 on an IBM PC
- ❑ Pin and Function Compatible with the PSD31X

Security Mode

Security Mode in the PSD3XX locks the contents of the PAD A , PAD B and all the configuration bits. The EPROM, SRAM, and I/O contents can be accessed only through the PAD. The Security Mode can be set by the MAPLE or Programming software. In window packages, the mode is erasable through UV full part erasure. In the security mode, the PSD3XX contents cannot be copied on a programmer.

CMiser-Bit

The CMiser-Bit provides a programmable option for power-sensitive applications that require further reduction in power consumption. The CMiser-Bit (CMiser = 1) in the Maple portion of the PSD3XX sytem development software can be used to reduce power consumption. The CMiser-Bit turns off the EPROM blocks in the PSD3XX whenever the EPROM is not accessed, thereby reducing the active current consumed by the PSD3XX.

In the default mode, or if the PSD3XX is configured without programming the CMiser-Bit (CMiser = 0), the device operates at specified speed and power rating as specified in the A.C. and D.C. Characteristics.

However, if the CMiser-Bit is programmed (CMiser = 1), the device consumes even lower current, and is reflected in the data sheet. This mode has an adder in propagation delay in T5, T6, and T7 parameters in the A.C. Characteristics, and should be added to compute worst-case timing requirements in the application.

Absolute Maximum Ratings[1]

Symbol	Parameter	Condition	Min	Max	Unit
T_{STG}	Storage Temperature	CERDIP	– 65	+ 150	°C
		PLASTIC	– 65	+ 125	°C
	Voltage on any Pin	With Respect to GND	– 0.6	+ 7	V
V_{PP}	Programming Supply Voltage	With Respect to GND	– 0.6	+ 14	V
V_{CC}	Supply Voltage	With Respect to GND	– 0.6	+ 7	V
	ESD Protection			>2000	V

NOTE: 1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at theses or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods of time may affect device reliability.

Operating Range

Range	Temperature	V_{CC}	V_{CC} Tolerance		
			-12	-15	-20
Commercial	0° C to +70°C	+ 5 V	± 10%	± 10%	± 10%
Industrial	–40° C to +80°C	+ 5 V		± 10%	± 10%
Military	–55° C to +125°C	+ 5 V			± 10%

Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	Supply Voltage	All Speeds	4.5	5	5.5	V
V_{IH}	High-level Input Voltage	V_{CC} = 4.5 V to 5.5 V	2			V
V_{IL}	Low-level Input Voltage	V_{CC} = 4.5 V to 5.5 V	0		0.8	V

DC Characteristics

Symbol	Parameter	Conditions				CMiser = 1 Subtract:			Unit
			Min	Typ	Max	Min	Typ	Max	
V_{OL}	Output Low Voltage	I_{OL} = 20 µA V_{CC} = 4.5 V		0.01	0.1				V
		I_{OL} = 8 mA V_{CC} = 4.5 V		0.15	0.45				V
V_{OH}	Output High Voltage	I_{OH} = –20 µA V_{CC} = 4.5 V	4.4	4.49					V
		I_{OH} = –2 mA V_{CC} = 4.5 V	2.4	3.9					V
I_{SB1}	V_{CC} Standby Current (CMOS) (Notes 2 and 4)	Comm'l		50	100				µA
		Ind/Mil		75	150				µA
I_{CC1}	Active Current (CMOS) (No Internal Memory Block Selected) (Notes 2 and 5)	Comm'l (Note 6)		16	35		7	10	mA
		Comm'l (Note 7)		28	50		7	10	mA
		Ind/Mil (Note 6)		16	45		7	10	mA
		Ind/Mil (Note 7)		28	60		7	10	mA
I_{CC2}	Active Current (CMOS) (EPROM Block Selected) (Notes 2 and 5)	Comm'l (Note 6)		16	35		0	0	mA
		Comm'l (Note 7)		28	50		0	0	mA
		Ind/Mil (Note 6)		16	45		0	0	mA
		Ind/Mil (Note 7)		28	60		0	0	mA
I_{CC3}	Active Current (CMOS) (SRAM Block Selected (Notes 2 and 5)	Comm'l (Note 6)		47	80		7	10	mA
		Comm'l (Note 7)		59	95		7	10	mA
		Ind/Mil (Note 6)		47	100		7	10	mA
		Ind/Mil (Note 7)		59	115		7	10	mA
I_{LI}	Input Leakage Current	V_{IN} = 5.5 V or GND	–1	±0.1	1				µA
I_{LO}	Output Leakage Current	V_{OUT} = 5.5 V or GND	–10	±5	10				µA

NOTES: 2. CMOS inputs: GND ± 0.3 V or V_{CC} ± 0.3V.
3. TTL inputs: $V_{IL} \leq 0.8$ V, $V_{IH} \geq 2.0$ V.
4. $\overline{CSI}$/A19 is high and the part is in a power-down configuration mode.
5. Add 3.0 mA/MHz for AC power component (power = AC + DC).
6. Ten (10) PAD product terms active. (Add 380 µA per product term, typical, or 480 µA per product term maximum
7. Forty-one (41) PAD product terms active.

AC Characteristics

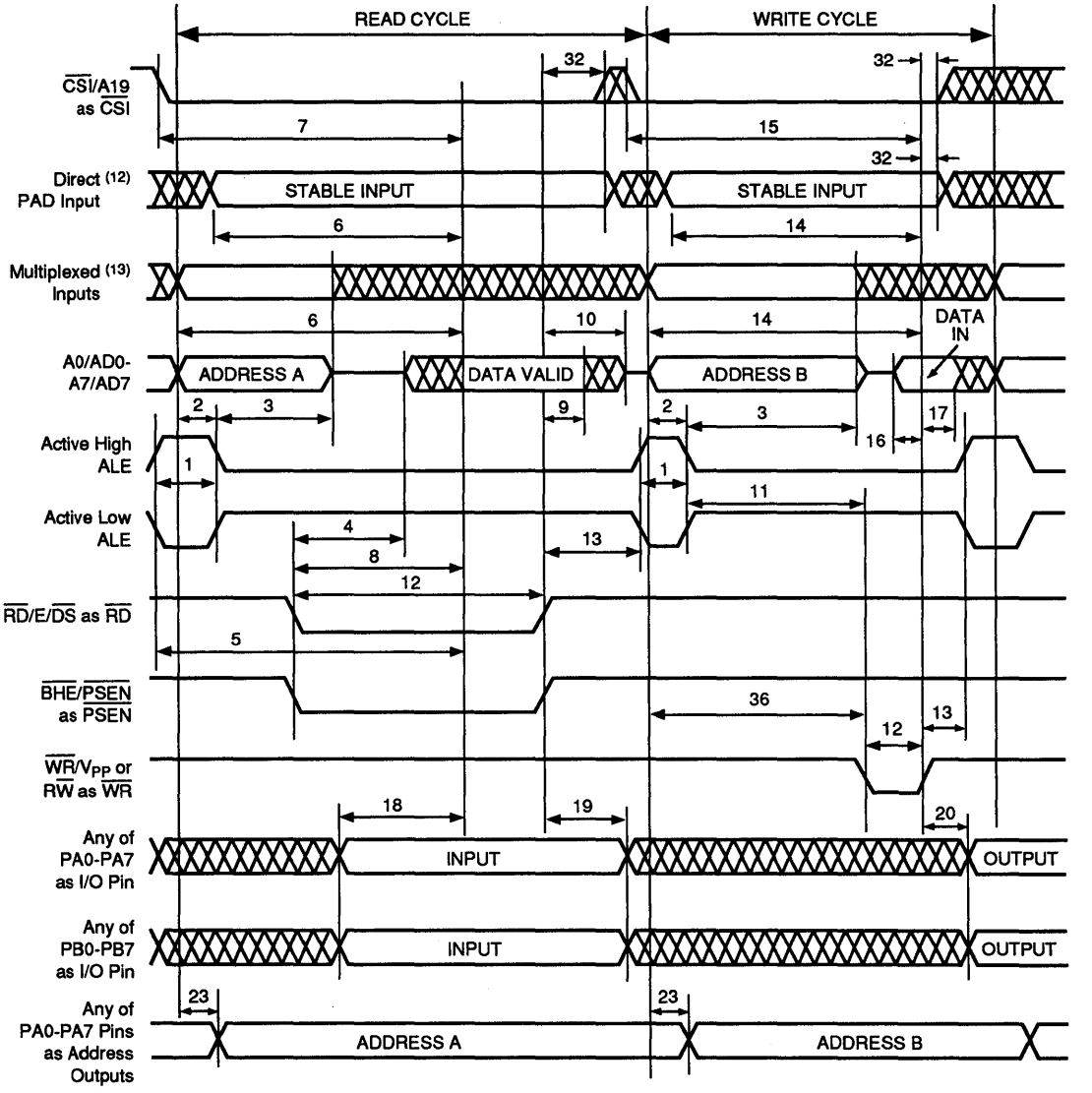
Symbol	Parameter	-90		-12		-15		-20		CMiser = 1 Add:	Unit
		Min	Max	Min	Max	Min	Max	Min	Max		
T1	ALE or AS Pulse Width	20		30		40		50		0	ns
T2	Address Set-up Time	5		9		12		15		0	ns
T3	Address Hold Time	8		9		12		15		0	ns
T4	Leading Edge of Read to Data Active	0		0		0		0		0	ns
T5	ALE Valid to Data Valid		100		130		160		200	10	ns
T6	Address Valid to Data Valid		90		120		150		200	10	ns
T7	$\overline{CSI}$ Active to Data Valid		100		130		160		200	15	ns
T8	Leading Edge of Read to Data Valid		32		38		55		60	0	ns
T9	Read Data Hold Time	0		0		0		0		0	ns
T10	Trailing Edge of Read to Data High-Z		32		32		35		40	0	ns
T11	Trailing Edge of ALE or AS to Leading Edge of Write	0		0		0		0		0	ns
T12	$\overline{RD}$, E, $\overline{PSEN}$, or $\overline{DS}$ Pulse Width	40		45		60		75		0	ns
T12A	$\overline{WR}$ Pulse Width	20		25		35		45		0	ns
T13	Trailing Edge of Write or Read to Leading Edge of ALE or AS	0		0		0		0		0	ns
T14	Address Valid to Trailing Edge of Write	90		120		150		200		0	ns
T15	$\overline{CSI}$ Active to Trailing Edge of Write	100		130		160		200		0	ns
T16	Write Data Set-up Time	20		25		30		40		0	ns
T17	Write Data Hold Time	5		5		10		15		0	ns
T18	Port to Data Out Valid Propagation Delay		30		30		35		45	0	ns
T19	Port Input Hold Time	0		0		0		0		0	ns
T20	Trailing Edge of Write to Port Output Valid	40		40		50		60		0	ns
T21	ADi or Control to $\overline{CSOi}$ Valid	6	25	6	30	6	35	5	45	0	ns
T22	ADi or Control to $\overline{CSOi}$ Invalid	5	25	5	30	4	35	4	45	0	ns

AC Characteristics (Cont.)

Symbol	Parameter	-90		-12		-15		-20		CMiser = 1 Add:	Unit
		Min	Max	Min	Max	Min	Max	Min	Max		
T23	Track Mode Address Propagation Delay: CSADOUT1 Already True		22		22		28		28	0	ns
T23A	Track Mode Address Propagation Delay: CSADOUT1 Becomes True During ALE or AS		33		33		50		50	0	ns
T24	Track Mode Trailing Edge of ALE or AS to Address High-Z		32		32		35		40	0	ns
T25	Track Mode Read Propagation Delay		29		29		35		35	0	ns
T26	Track Mode Read Hold Time	11	29	11	29	10	29	10	35	0	ns
T27	Track Mode Write Cycle, Data Propagation Delay		20		20		30		30	0	ns
T28	Track Mode Write Cycle, Write to Data Propagation Delay	8	30	8	30	7	40	7	55	0	ns
T29	Hold Time of Port A Valid During Write $\overline{CSOi}$ Trailing Edge	2		2		2		2		0	ns
T30	$\overline{CSI}$ Active to $\overline{CSOi}$ Active	9	40	9	45	9	50	8	60	0	ns
T31	$\overline{CSI}$ Inactive to $\overline{CSOi}$ Inactive	9	40	9	45	9	50	8	60	0	ns
T32	Direct PAD Input as Hold Time	10		10		12		15		0	ns
T33	R/$\overline{W}$ Active to E or $\overline{DS}$ Start	20		20		30		40		0	ns
T34	E or $\overline{DS}$ End to R/$\overline{W}$	20		20		30		40		0	ns
T35	AS Inactive to E high	0		0		0		0		0	ns
T36	Address to Leading Edge of Write	20		20		25		30		0	ns

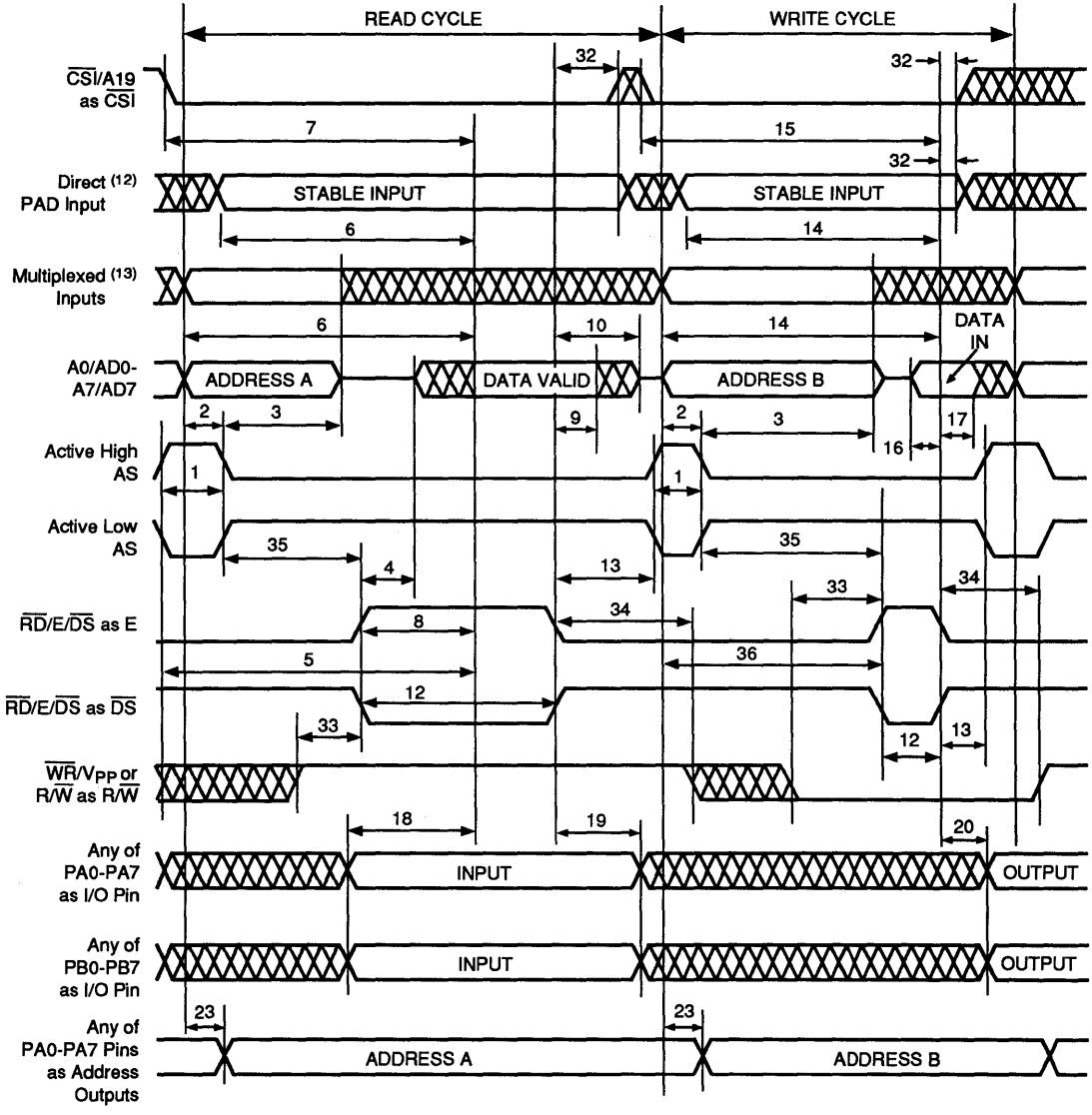
NOTES: 8. ADi = any address line.
9. $\overline{CSOi}$ = any of the chip-select output signals coming through Port B ($\overline{CS0}$–$\overline{CS7}$) or through Port C ($\overline{CS8}$–$\overline{CS10}$).
10. Direct PAD input = any of the following direct PAD input lines: $\overline{CSI}$/A19 as transparent A19, $\overline{RD}$/E/$\overline{DS}$, $\overline{WR}$ or R/$\overline{W}$, transparent PC0–PC2, ALE (or AS).
11. Control signals $\overline{RD}$/E/$\overline{DS}$ or $\overline{WR}$ or R/$\overline{W}$.

Figure 1. Timing of 8-Bit Multiplexed Address/DataBus, CRRWR = 0



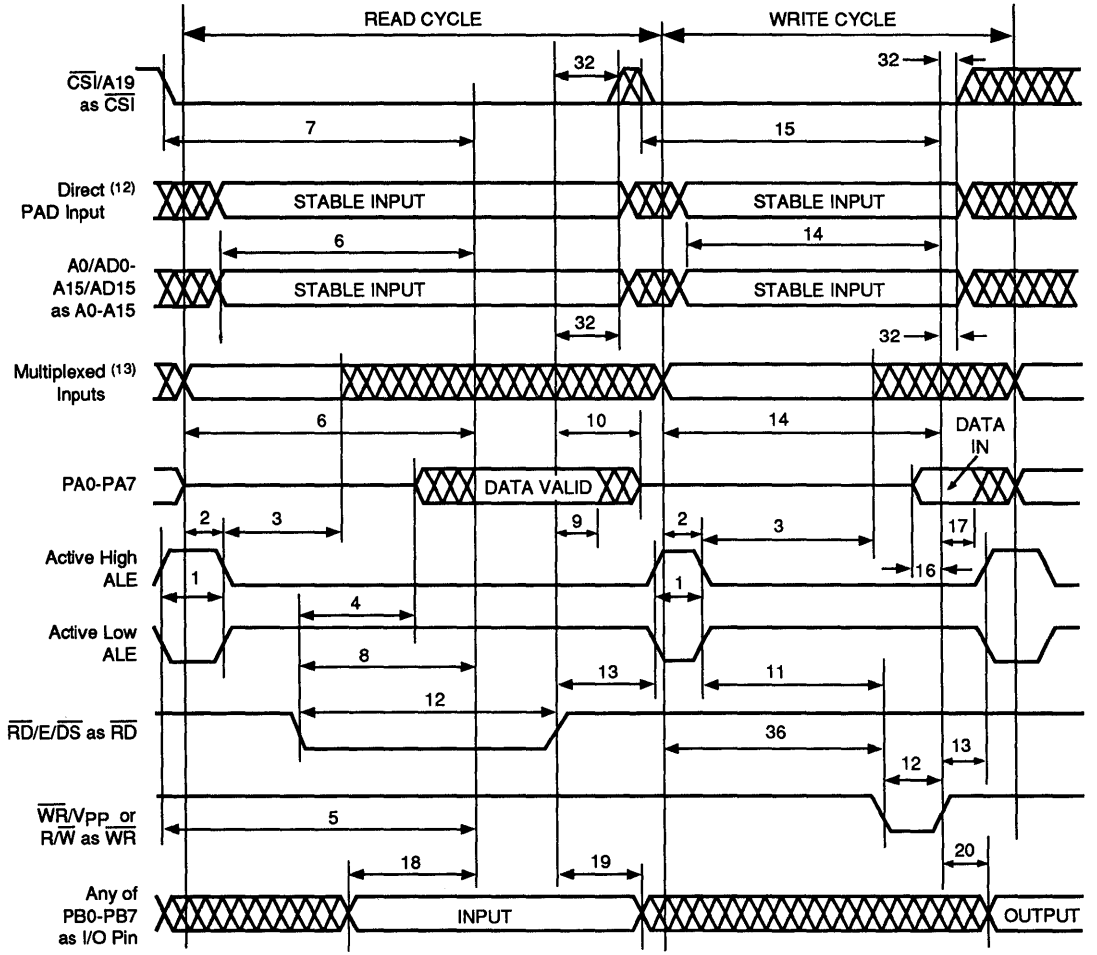
See referenced notes on page 106.

Figure 2. Timing of 8-Bit Multiplexed Address/DataBus, CRRWR = 1



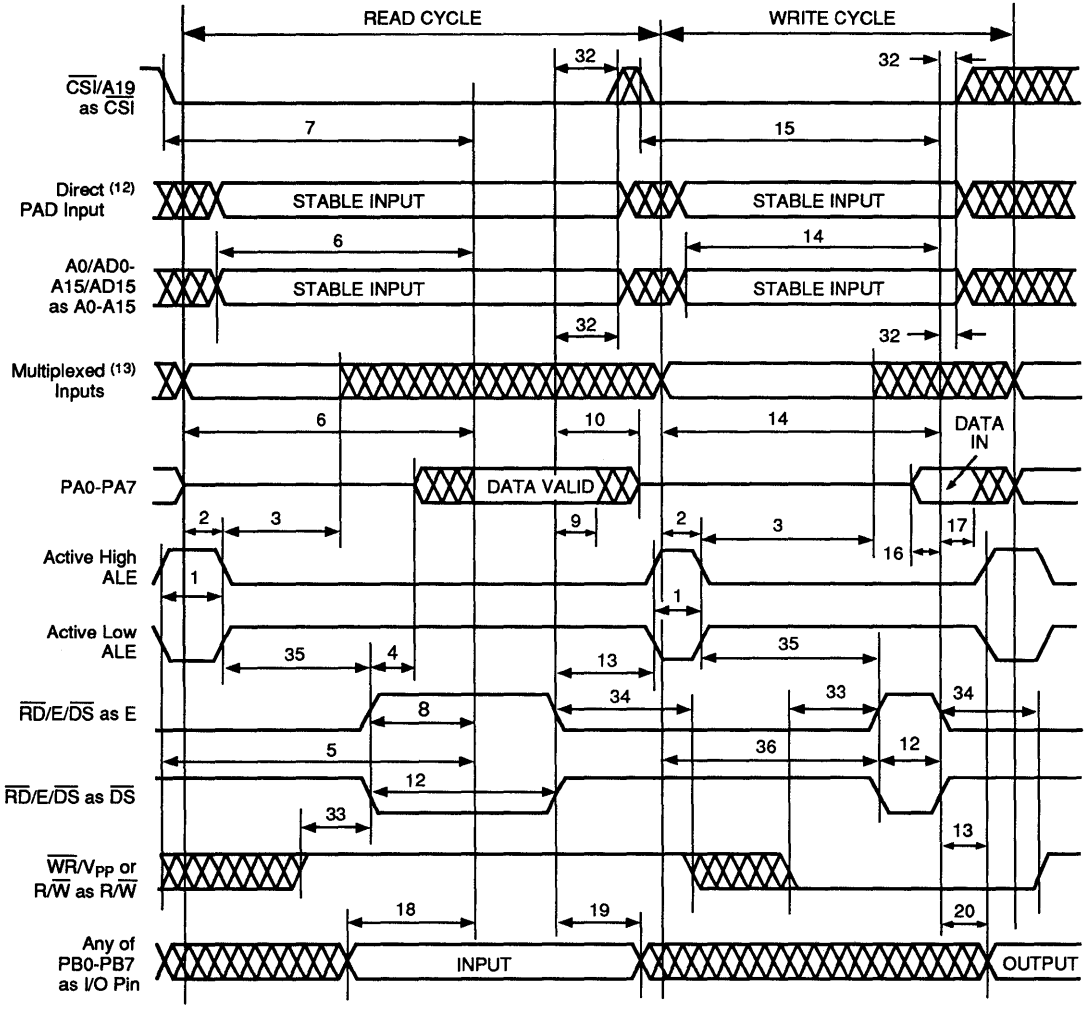
See referenced notes on page 106.

Figure 3. Timing of 8-Bit Data, Non-Multiplexed Address/DataBus, CRRWR = 0



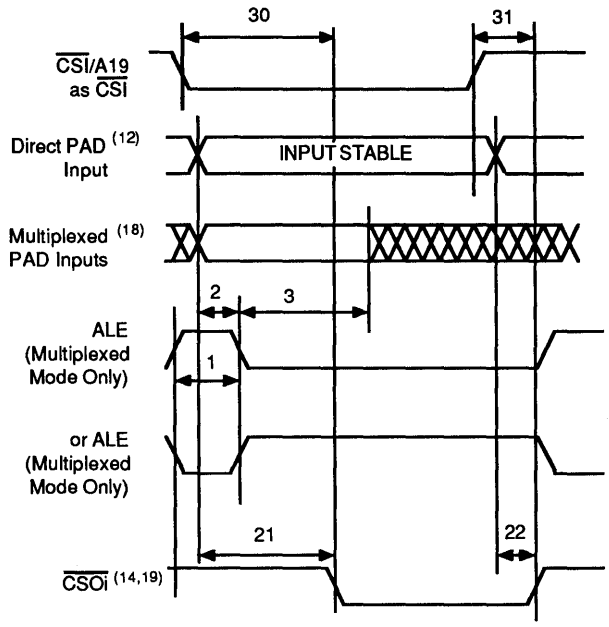
See referenced notes on page 106.

Figure 4. Timing of 8-Bit Data, Non-Multiplexed Address/DataBus, CRRWR = 1



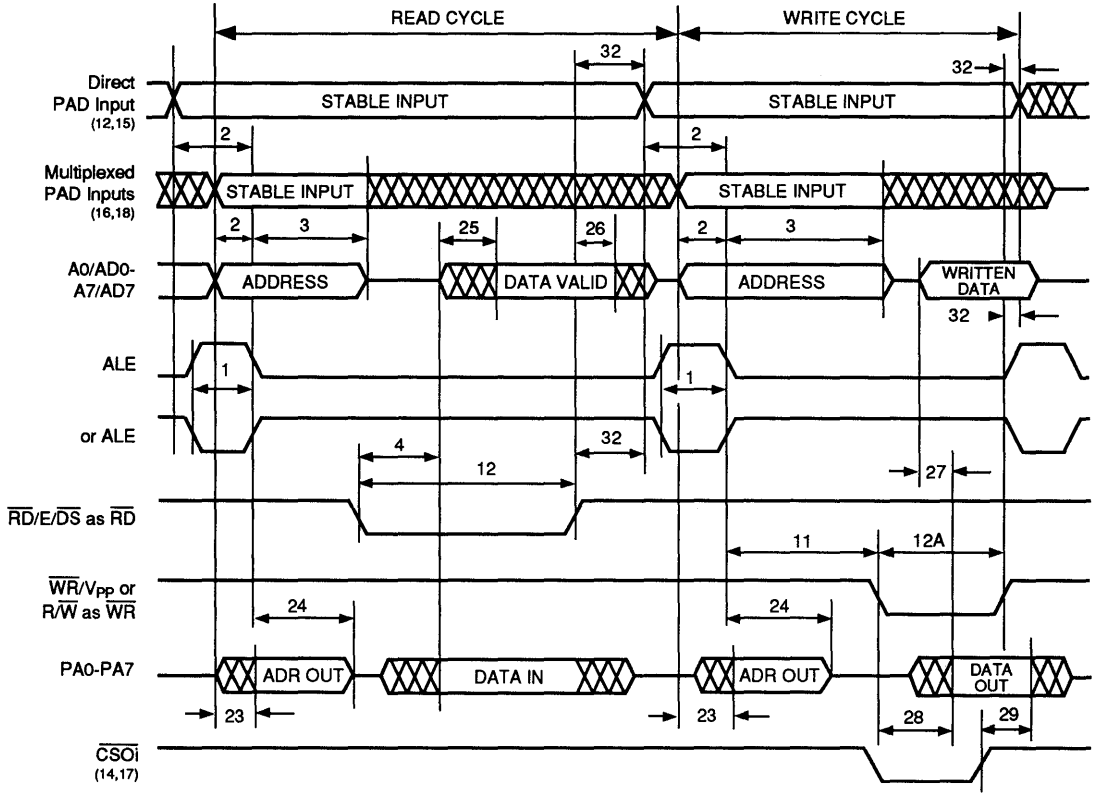
See referenced notes on page 106.

Figure 5. Chip-Select Output Timing



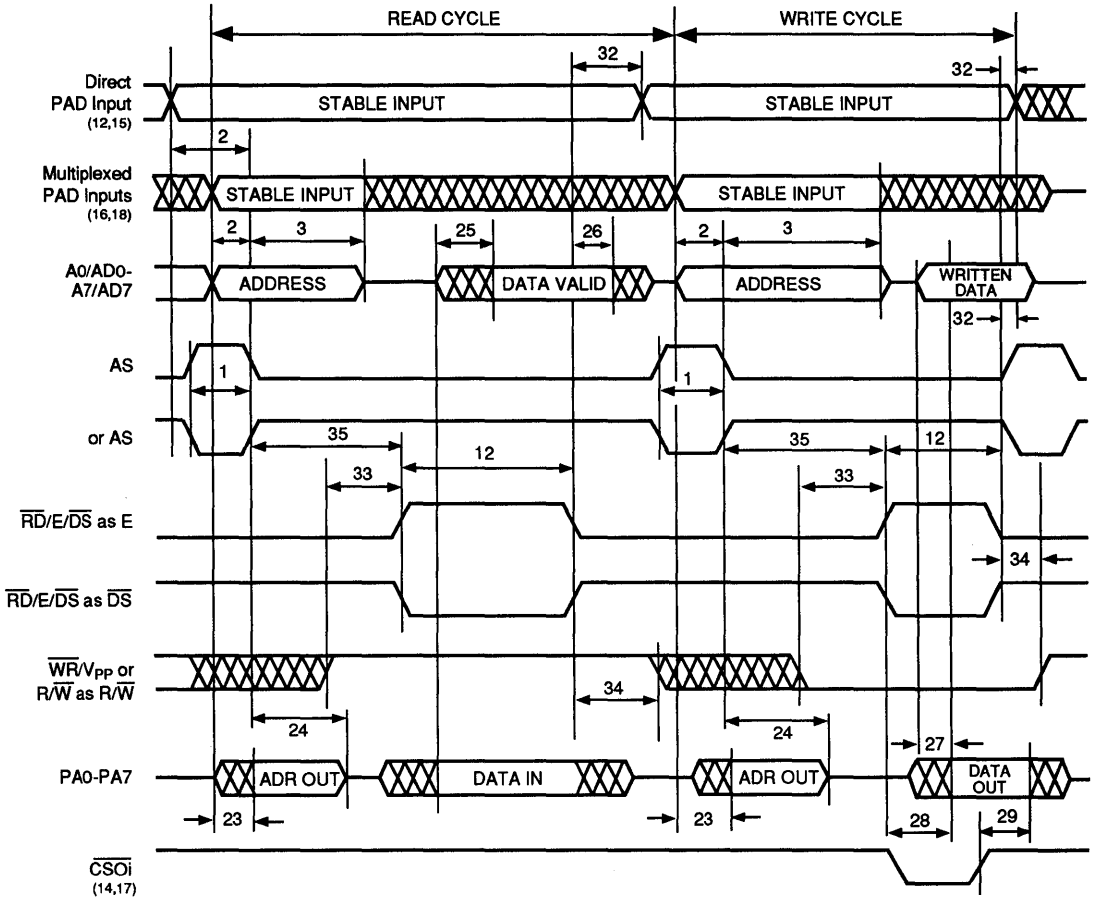
See referenced notes on page 106.

Figure 6. Port A as AD0–AD7 Timing (Track Mode), CRRWR = 0



See referenced notes on page 106.

Figure 11. Port A as AD0–AD7 Timing (Track Mode), CRRWR = 1



Notes for Timing Diagrams

12. Direct PAD input = any of the following direct PAD input lines: $\overline{CSI}$/A19 as transparent A19, $\overline{RD}$/E, $\overline{WR}$ or R/$\overline{W}$, transparent PC0–PC2, ALE in non-multiplexed modes.
13. Multiplexed inputs: any of the following inputs that are latched by the ALE (or AS): A0/AD0–A15/AD15, $\overline{CSI}$/A19 as ALE dependent A19, ALE dependent PC0–PC2.
14. $\overline{CSOi}$ = any of the chip-select output signals coming through Port B ($\overline{CS0}$–$\overline{CS7}$) or through Port C ($\overline{CS8}$–$\overline{CS10}$).
15. CSADOUT1, which internally enables the address transfer to Port A, should be derived only from direct PAD input signals, otherwise the address propagation delay is slowed down.
16. CSADIN and CSADOUT2, which internally enable the data-in or data-out transfers, respectively, can be derived from any combination of direct PAD inputs and multiplexed PAD inputs.
17. The write operation signals are included in the $\overline{CSOi}$ expression.
18. Multiplexed PAD inputs: any of the following PAD inputs that are latched by the ALE (or AS) in the multiplexed modes: A11/AD11–A15/AD15, $\overline{CSI}$/A19 as ALE dependent A19, ALE dependent PC0–PC2.
19. $\overline{CSOi}$ product terms can include any of the PAD input signals except for reset and $\overline{CSI}$.

Pin Capacitance[20]

Symbol	Parameter	Conditions	Typical[21]	Max	Unit
C_{IN}	Capacitance (for input pins only)	V_{IN} = 0 V	4	6	pF
C_{OUT}	Capacitance (for input/output pins)	V_{OUT} = 0 V	8	12	pF
C_{VPP}	Capacitance (for WR/V_{PP} or R/W/V_{PP})	V_{PP} = 0 V	18	25	pF

NOTES: 20. This paramter is only sampled and is not 100% tested.
21. Typical values are for T_A = 25°C and nominal supply voltages.

Figure 8. AC Testing Input/Output Waveform

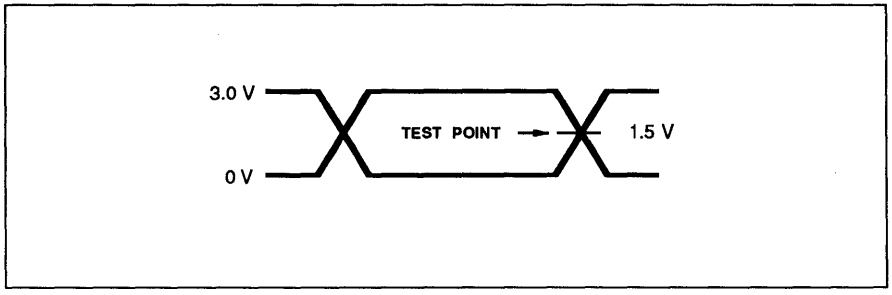
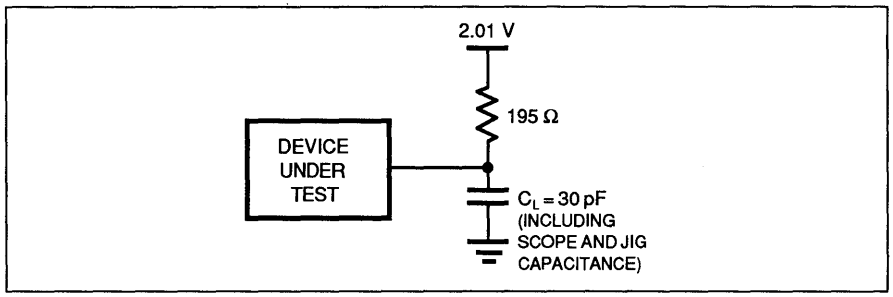


Figure 9. AC Testing Load Circuit



Erasure and Programming

To clear all locations of their programmed contents, expose the device to ultra-violet light source. A dosage of 15 W second/cm^2 is required. This dosage can be obtained with exposure to a wavelength of 2537 Å and intensity of 12000 µW/cm^2 for 15 to 20 minutes. The device should be about 1 inch from the source, and all filters should be removed from the UV light source prior to erasure.

The PSD3XX and similar devices will erase with light sources having wavelengths shorter than 4000 Å. Although the erasure times will be much longer than with UV sources at 2537 Å, exposure to fluorescent light and sunlight eventually erases the device. For maximum system reliability, these sources should be avoided. If used in such an environment, the package windows should be covered by an opaque substance.

Upon delivery, or after each erasure, the PSD3XX device has all bits in the PAD and EPROM in the "1" or high state. The configuration bits are in the "0" or low state. The code, configuration, and PAD MAP data are loaded through the procedure of programming.

Pin Assignments

Pin Name	44-Pin PLCC/CLCC Package	52-Pin PQFP Package
$\overline{PSEN}$	1	46
$\overline{WR}/V_{PP}$ or R/$\overline{W}$	2	47
RESET	3	48
PB7	4	49
PB6	5	50
PB5	6	51
PB4	7	2
PB3	8	3
PB2	9	4
PB1	10	5
PB0	11	6
GND	12	7
ALE or AS	13	8
PA7	14	9
PA6	15	10
PA5	16	11
PA4	17	12
PA3	18	15
PA2	19	16
PA1	20	17
PA0	21	18
$\overline{RD}$/E/$\overline{DS}$	22	19
AD0/A0	23	20
AD1/A1	24	21
AD2/A2	25	22
AD3/A3	26	23
AD4/A4	27	24
AD5/A5	28	25
AD6/A6	29	28
AD7/A7	30	29
A8	31	30
A9	32	31
A10	33	32
GND	34	33
A11	35	34
A12	36	35
A13	37	36
A14	38	37
A15	39	38
PC0	40	41
PC1	41	42
PC2	42	43
A19/$\overline{CSI}$	43	44
V_{CC}	44	45

NOTE: 36. Pins 1, 13, 14, 26, 27, 39, 40, and 52 are No Connect.

Package Information

Figure 10. Drawing L4 — 44 Pin Ceramic Leaded Chip Carrier (CLCC) with Window (Package Type L)

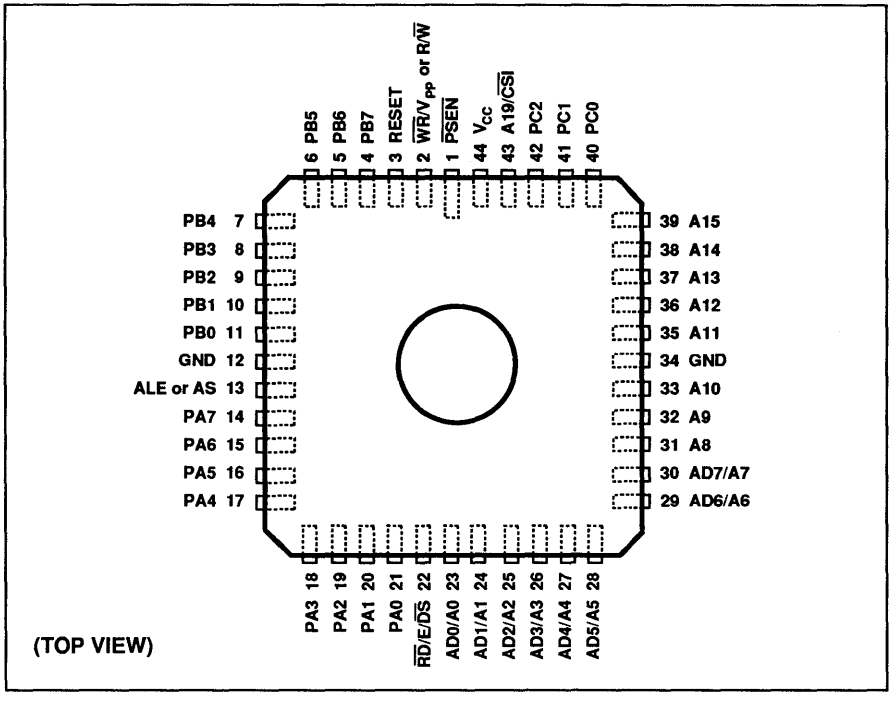


Figure 11. Drawing J2 — 44 Pin Plastic Leaded Chip Carrier (PLCC) with Window (Package Type J)

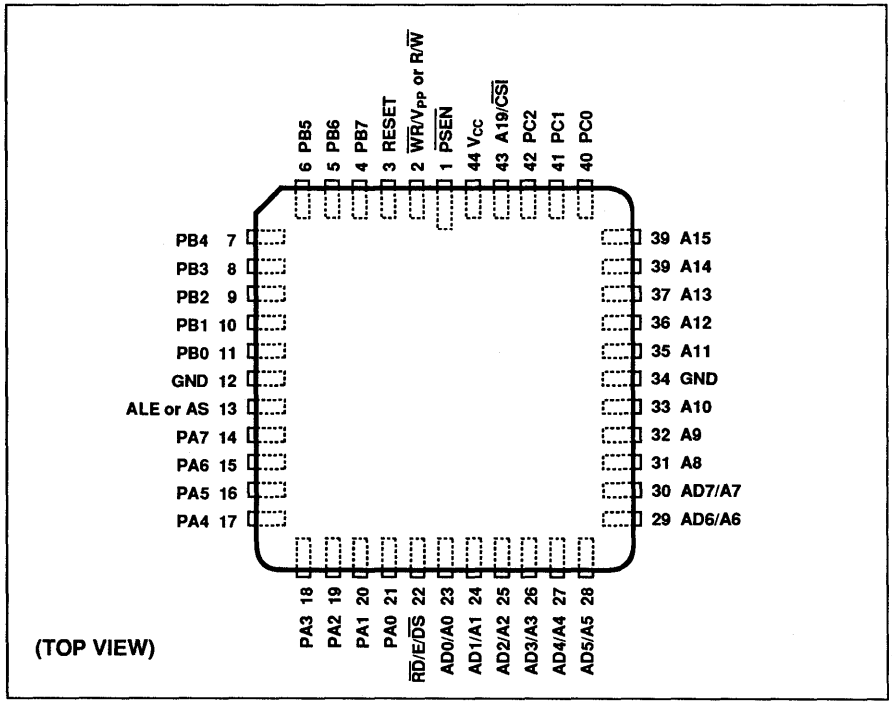
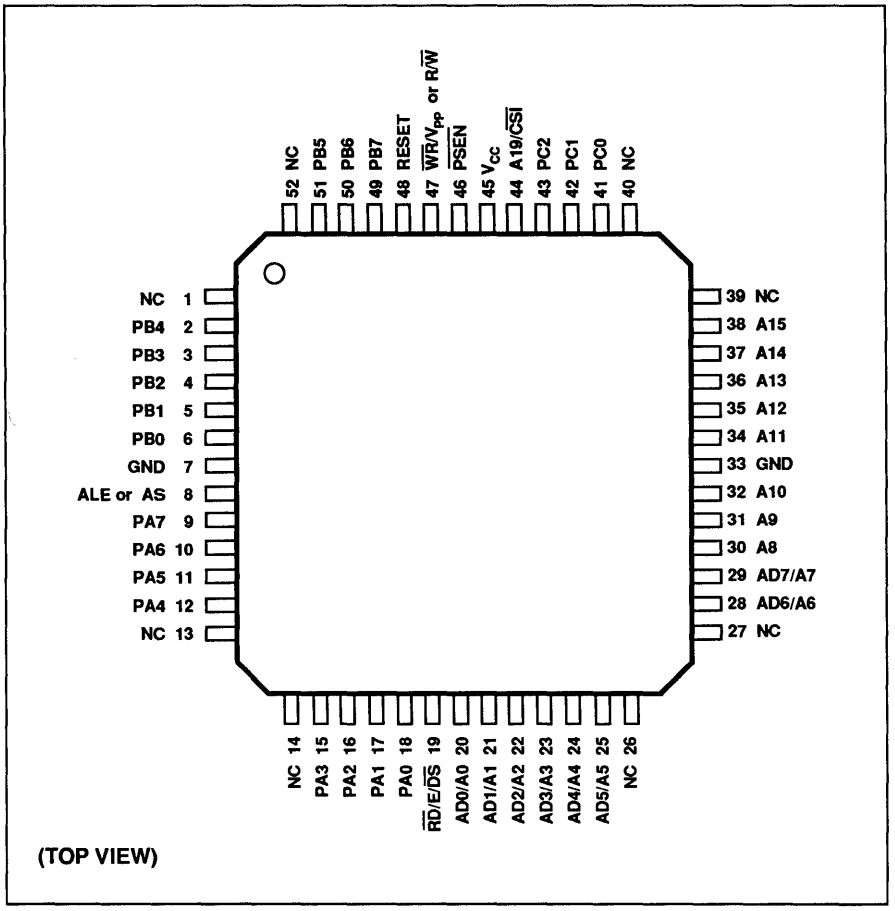


Figure 12. Drawing Q2 – 52 Pin PQFP (Package Type Q)



Ordering Information

Part Number	Spd. (ns)	Package Type	Package Drawing	Operating Temperature Range	Manufacturing Procedure
PSD312-90 A	90	44-pin PLCC	J2	Commercial	Standard
PSD312-90 KA	90	44-pin CLCC	L4	Commercial	Standard
PSD312-12 A	120	44-pin PLCC	J2	Commercial	Standard
PSD312-12 KA	120	44-pin CLCC	L4	Commercial	Standard
PSD312-12 B	120	52-pin PQFP	Q2	Commercial	Standard
PSD312-15 A	150	44-pin PLCC	J2	Commercial	Standard
PSD312-15I A	150	44-pin PLCC	J2	Industrial	Standard
PSD312-15 KA	150	44-pin CLCC	L4	Commercial	Standard
PSD312-15I KA	150	44-pin CLCC	L4	Industrial	Standard
PSD312-15 B	150	52-pin PQFP	Q2	Commercial	Standard
PSD312-15I B	150	52-pin PQFP	Q2	Industrial	Standard
PSD312-20 A	200	44-pin PLCC	J2	Commercial	Standard
PSD312-20I A	200	44-pin PLCC	J2	Industrial	Standard
PSD312-20 KA	200	44-pin CLCC	L4	Commercial	Standard
PSD312-20I KA	200	44-pin CLCC	L4	Industrial	Standard
PSD312-20 B	200	52-pin PQFP	Q2	Commercial	Standard
PSD312-20I B	200	52-pin PQFP	Q2	Industrial	Standard

Field-programmable microcontroller peripheral — PSD303

Key Features

- ❑ Single Chip Programmable Peripheral for Microcontroller-based Applications
- ❑ 19 Individually Configurable I/O pins that can be used as:
  - — Microcontroller I/O port expansion
  - — Programmable Address Decoder (PAD) I/O
  - — Latched address output
  - — Open drain or CMOS
- ❑ Two Programmable Arrays (PAD A & PAD B)
  - — Total of 40 Product Terms and up to 16 Inputs and 24 Outputs
  - — Direct Address Decoding up to 1 Meg address space and up to 16 Meg with paging
  - — Logic replacement
- ❑ "No Glue" Microcontroller Chip-Set
  - — Built-in address latches for multiplexed address/data bus
  - — Non-multiplexed address/data bus mode
  - — Selectable 8 or 16 bit data bus width
  - — ALE and Reset polarity programmable
  - — Selectable modes for read and write control bus as $\overline{RD}/\overline{WR}$, R/$\overline{W}$/E, or R/$\overline{W}$/$\overline{DS}$
  - — $\overline{BHE}$ pin for byte select in 16-bit mode
  - — $\overline{PSEN}$ pin for 8051 users
- ❑ Built-In Page Logic
  - — To Expand the Address Space of Microcontrollers with Limited Address Space Capabilities
  - — Up to 16 pages
- ❑ 1 M bit of UV EPROM
  - — Configurable as 128K x 8 or as 64K x 16
  - — Divides into 8 equal mappable blocks for optimized mapping
  - — Block resolution is 16K x 8 or 8K x 16
  - — 120 ns EPROM access time, including input latches and PAD address decoding.
- ❑ 16 Kbit Static RAM
  - — Configurable as 2K x 8 or as 1K x 16
  - — 120 ns SRAM access time, including input latches and PAD address decoding
- ❑ Address/Data Track Mode
  - — Enables easy Interface to Shared Resources (e.g., Mail Box SRAM) with other Microcontrollers or a Host Processor
- ❑ Built-In Security
  - — Locks the PSD303 and PAD Decoding Configuration
- ❑ Available in a Choice of Packages
  - — 44 Pin PLCC and CLCC
- ❑ Simple Menu-Driven Software: Configure the PSD303 on an IBM PC
- ❑ Pin and Function Compatible with the PSD301 and PSD302

Security Mode

Security Mode in the PSD3XX locks the contents of the PAD A , PAD B and all the configuration bits. The EPROM, SRAM, and I/O contents can be accessed only through the PAD. The Security Mode can be set by the MAPLE or Programming software. In window packages, the mode is erasable through UV full part erasure. In the security mode, the PSD3XX contents cannot be copied on a programmer.

CMiser-Bit

The CMiser-Bit provides a programmable option for power-sensitive applications that require further reduction in power consumption. The CMiser-Bit (CMiser = 1) in the Maple portion of the PSD3XX sytem development software can be used to reduce power consumption. The CMiser-Bit turns off the EPROM blocks in the PSD3XX whenever the EPROM is not accessed, thereby reducing the active current consumed by the PSD3XX.

In the default mode, or if the PSD3XX is configured without programming the CMiser-Bit (CMiser = 0), the device operates at specified speed and power rating as specified in the A.C. and D.C. Characteristics.

However, if the CMiser-Bit is programmed (CMiser = 1), the device consumes even lower current, and is reflected in the data sheet. This mode has an adder in propagation delay in T5, T6, and T7 parameters in the A.C. Characteristics, and should be added to compute worst-case timing requirements in the application.

Absolute Maximum Ratings[1]

Symbol	Parameter	Condition	Min	Max	Unit
T_{STG}	Storage Temperature	CERDIP	– 65	+ 150	°C
		PLASTIC	– 65	+ 125	°C
	Voltage on any Pin	With Respect to GND	– 0.6	+ 7	V
V_{PP}	Programming Supply Voltage	With Respect to GND	– 0.6	+ 14	V
V_{CC}	Supply Voltage	With Respect to GND	– 0.6	+ 7	V
	ESD Protection			>2000	V

NOTE: 1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at theses or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods of time may affect device reliability.

Operating Range

Range	Temperature	V_{CC}	V_{CC} Tolerance		
			-12	-15	-20
Commercial	0° C to +70°C	+ 5 V	± 10%	± 10%	± 10%
Industrial	–40° C to +80°C	+ 5 V		± 10%	± 10%
Military	–55° C to +125°C	+ 5 V			± 10%

Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	Supply Voltage	All Speeds	4.5	5	5.5	V
V_{IH}	High-level Input Voltage	V_{CC} = 4.5 V to 5.5 V	2			V
V_{IL}	Low-level Input Voltage	V_{CC} = 4.5 V to 5.5 V	0		0.8	V

DC Characteristics

Symbol	Parameter	Conditions				CMiser = 1 Subtract:			Unit
			Min	Typ	Max	Min	Typ	Max	
V_{OL}	Output Low Voltage	I_{OL} = 20 µA V_{CC} = 4.5 V		0.01	0.1				V
		I_{OL} = 8 mA V_{CC} = 4.5 V		0.15	0.45				V
V_{OH}	Output High Voltage	I_{OH} = –20 µA V_{CC} = 4.5 V	4.4	4.49					V
		I_{OH} = –2 mA V_{CC} = 4.5 V	2.4	3.9					V
I_{SB1}	V_{CC} Standby Current (CMOS) (Notes 2 and 4)	Comm'l		50	100				µA
		Ind/Mil		75	150				µA
I_{CC1}	Active Current (CMOS) (No Internal Memory Block Selected) (Notes 2 and 5)	Comm'l (Note 6)		16	35		7	10	mA
		Comm'l (Note 7)		28	50		7	10	mA
		Ind/Mil (Note 6)		16	45		7	10	mA
		Ind/Mil (Note 7)		28	60		7	10	mA
I_{CC2}	Active Current (CMOS) (EPROM Block Selected) (Notes 2 and 5)	Comm'l (Note 6)		16	35		0	0	mA
		Comm'l (Note 7)		28	50		0	0	mA
		Ind/Mil (Note 6)		16	45		0	0	mA
		Ind/Mil (Note 7)		28	60		0	0	mA
I_{CC3}	Active Current (CMOS) (SRAM Block Selected (Notes 2 and 5)	Comm'l (Note 6)		47	80		7	10	mA
		Comm'l (Note 7)		59	95		7	10	mA
		Ind/Mil (Note 6)		47	100		7	10	mA
		Ind/Mil (Note 7)		59	115		7	10	mA
I_{LI}	Input Leakage Current	V_{IN} = 5.5 V or GND	–1	±0.1	1				µA
I_{LO}	Output Leakage Current	V_{OUT} = 5.5 V or GND	–10	±5	10				µA

NOTES: 2. CMOS inputs: GND ± 0.3 V or V_{CC} ± 0.3V.
3. TTL inputs: $V_{IL} \leq 0.8$ V, $V_{IH} \geq 2.0$ V.
4. $\overline{CSI}$/A19 is high and the part is in a power-down configuration mode.
5. Add 3.0 mA/MHz for AC power component (power = AC + DC).
6. Ten (10) PAD product terms active. (Add 380 µA per product term, typical, or 480 µA per product term maximum
7. Forty-one (41) PAD product terms active.

AC Characteristics

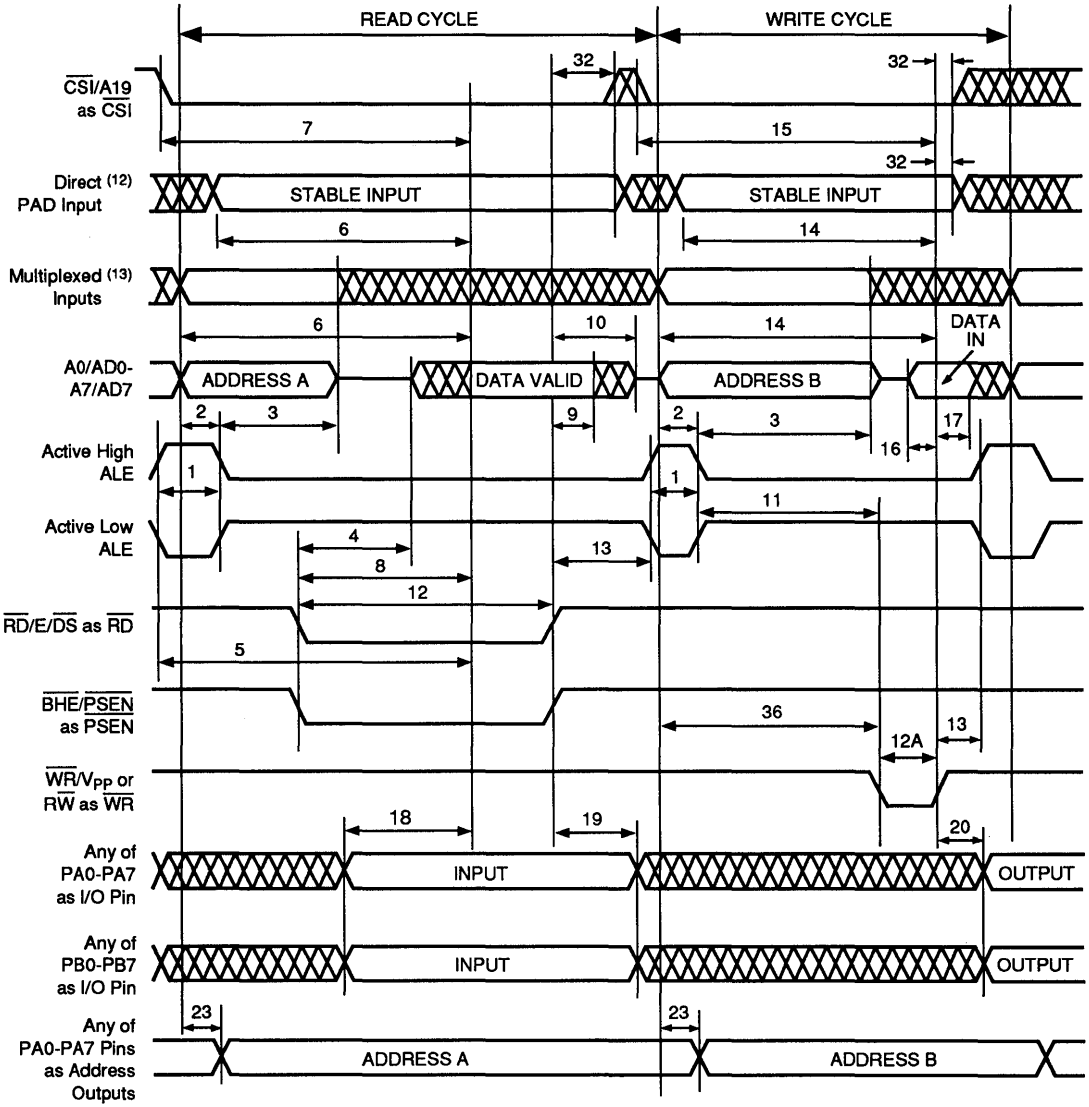
Symbol	Parameter	-90		-12		-15		-20		CMiser = 1 Add:	Unit
		Min	Max	Min	Max	Min	Max	Min	Max		
T1	ALE or AS Pulse Width	20		30		40		50		0	ns
T2	Address Set-up Time	5		9		12		15		0	ns
T3	Address Hold Time	8		9		12		15		0	ns
T4	Leading Edge of Read to Data Active	0		0		0		0		0	ns
T5	ALE Valid to Data Valid		100		130		160		200	10	ns
T6	Address Valid to Data Valid		90		120		150		200	10	ns
T7	$\overline{CSI}$ Active to Data Valid		100		130		160		200	15	ns
T8	Leading Edge of Read to Data Valid		32		38		55		60	0	ns
T9	Read Data Hold Time	0		0		0		0		0	ns
T10	Trailing Edge of Read to Data High-Z		32		32		35		40	0	ns
T11	Trailing Edge of ALE or AS to Leading Edge of Write	0		0		0		0		0	ns
T12	$\overline{RD}$, E, $\overline{PSEN}$, or $\overline{DS}$ Pulse Width	40		45		60		75		0	ns
T12A	$\overline{WR}$ Pulse Width	20		25		35		45		0	ns
T13	Trailing Edge of Write or Read to Leading Edge of ALE or AS	0		0		0		0		0	ns
T14	Address Valid to Trailing Edge of Write	90		120		150		200		0	ns
T15	$\overline{CSI}$ Active to Trailing Edge of Write	100		130		160		200		0	ns
T16	Write Data Set-up Time	20		25		30		40		0	ns
T17	Write Data Hold Time	5		5		10		15		0	ns
T18	Port to Data Out Valid Propagation Delay		30		30		35		45	0	ns
T19	Port Input Hold Time	0		0		0		0		0	ns
T20	Trailing Edge of Write to Port Output Valid	40		40		50		60		0	ns
T21	ADi or Control to $\overline{CSOi}$ Valid	6	25	6	30	6	35	5	45	0	ns
T22	ADi or Control to $\overline{CSOi}$ Invalid	5	25	5	30	4	35	4	45	0	ns

AC Characteristics (Cont.)

Symbol	Parameter	-90		-12		-15		-20		CMiser = 1 Add:	Unit
		Min	Max	Min	Max	Min	Max	Min	Max		
T23	Track Mode Address Propagation Delay: CSADOUT1 Already True		22		22		28		28	0	ns
T23A	Track Mode Address Propagation Delay: CSADOUT1 Becomes True During ALE or AS		33		33		50		50	0	ns
T24	Track Mode Trailing Edge of ALE or AS to Address High-Z		32		32		35		40	0	ns
T25	Track Mode Read Propagation Delay		29		29		35		35	0	ns
T26	Track Mode Read Hold Time	11	29	11	29	10	29	10	35	0	ns
T27	Track Mode Write Cycle, Data Propagation Delay		20		20		30		30	0	ns
T28	Track Mode Write Cycle, Write to Data Propagation Delay	8	30	8	30	7	40	7	55	0	ns
T29	Hold Time of Port A Valid During Write $\overline{CSOi}$ Trailing Edge	2		2		2		2		0	ns
T30	$\overline{CSI}$ Active to $\overline{CSOi}$ Active	9	40	9	45	9	50	8	60	0	ns
T31	$\overline{CSI}$ Inactive to $\overline{CSOi}$ Inactive	9	40	9	45	9	50	8	60	0	ns
T32	Direct PAD Input as Hold Time	10		10		12		15		0	ns
T33	R/$\overline{W}$ Active to E or $\overline{DS}$ Start	20		20		30		40		0	ns
T34	E or $\overline{DS}$ End to R/$\overline{W}$	20		20		30		40		0	ns
T35	AS Inactive to E high	0		0		0		0		0	ns
T36	Address to Leading Edge of Write	20		20		25		30		0	ns

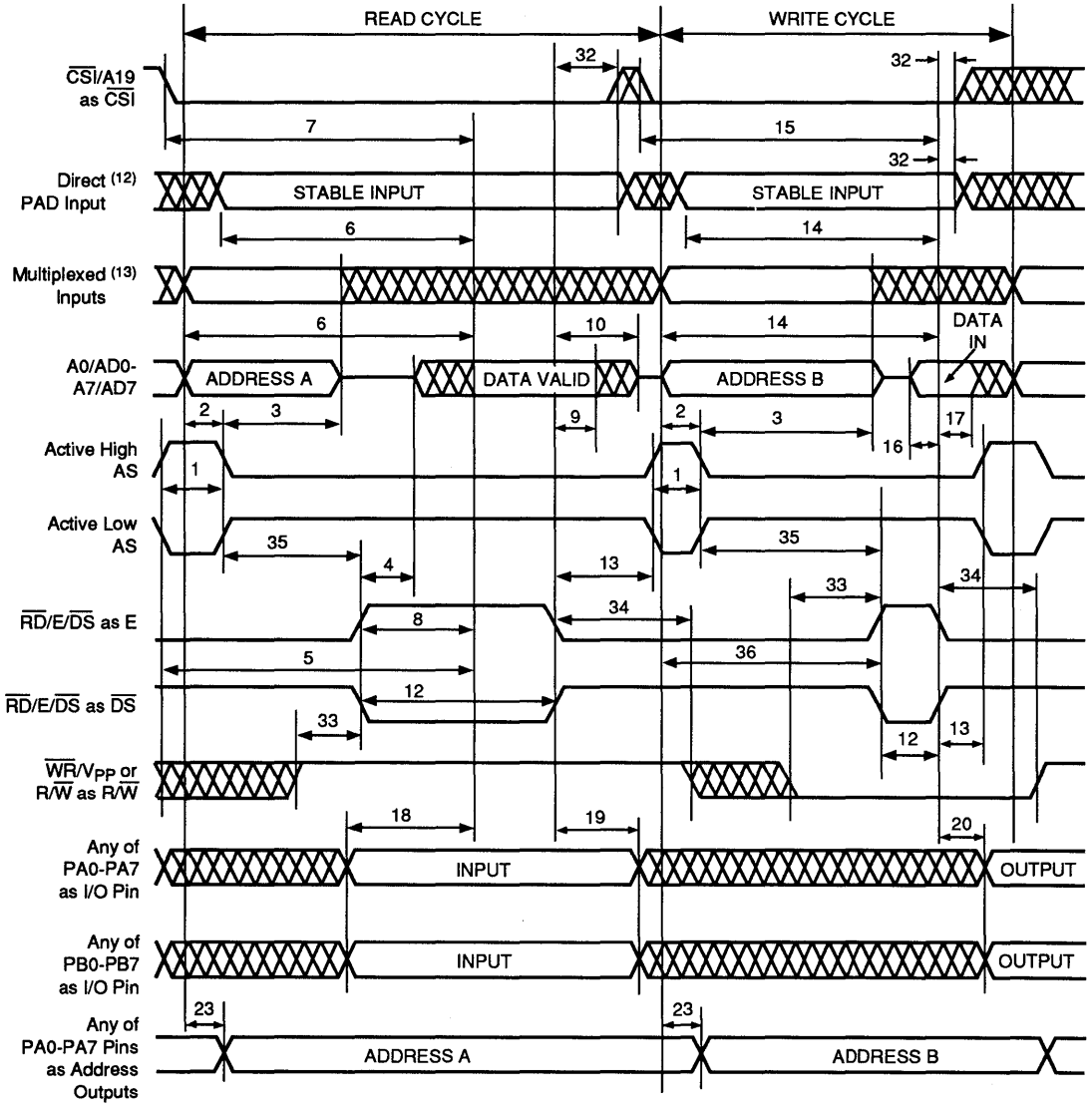
NOTES: 8. ADi = any address line.
9. $\overline{CSOi}$ = any of the chip-select output signals coming through Port B ($\overline{CS0}$–$\overline{CS7}$) or through Port C ($\overline{CS8}$–$\overline{CS10}$).
10. Direct PAD input = any of the following direct PAD input lines: $\overline{CSI}$/A19 as transparent A19, $\overline{RD}$/E/$\overline{DS}$, $\overline{WR}$ or R/$\overline{W}$, transparent PC0–PC2, ALE (or AS).
11. Control signals $\overline{RD}$/E/$\overline{DS}$ or $\overline{WR}$ or R/$\overline{W}$.

Figure 1. Timing of 8-Bit Multiplexed Address/DataBus, CRRWR = 0



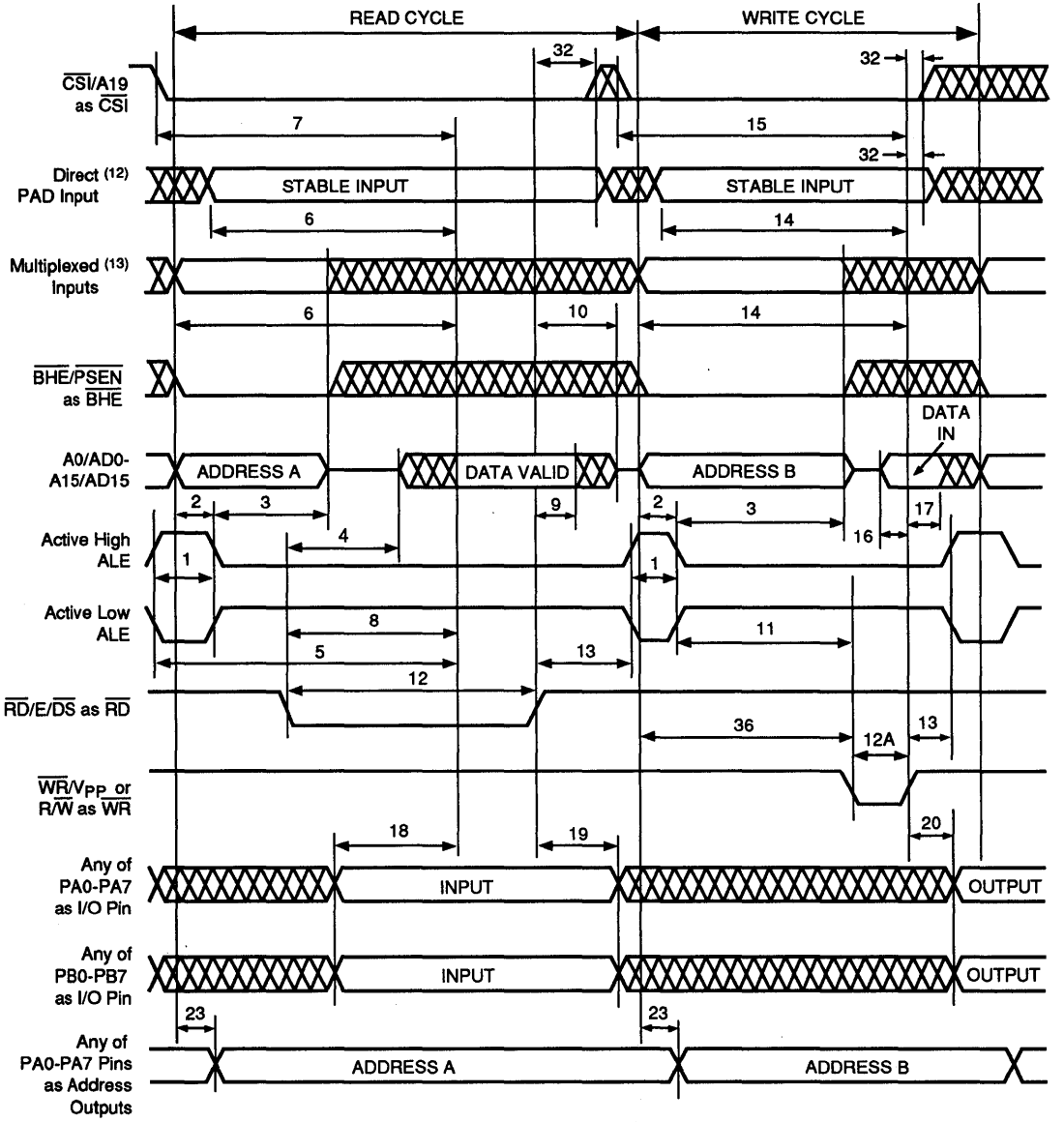
See referenced notes on page 128.

Figure 2. Timing of 8-Bit Multiplexed Address/DataBus, CRRWR = 1



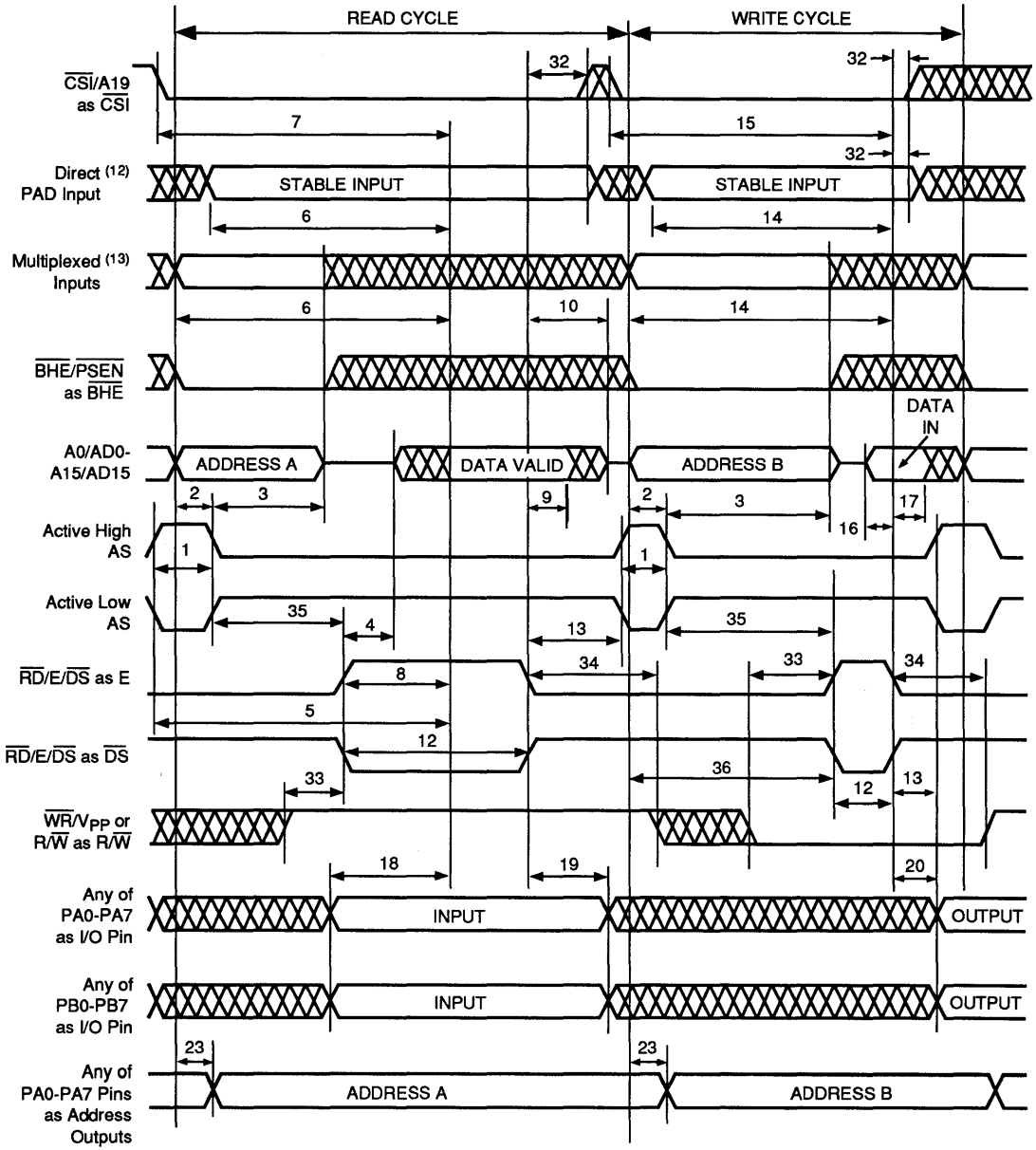
See referenced notes on page 128.

Figure 3. Timing of 16-Bit Multiplexed Address/DataBus, CRRWR = 0



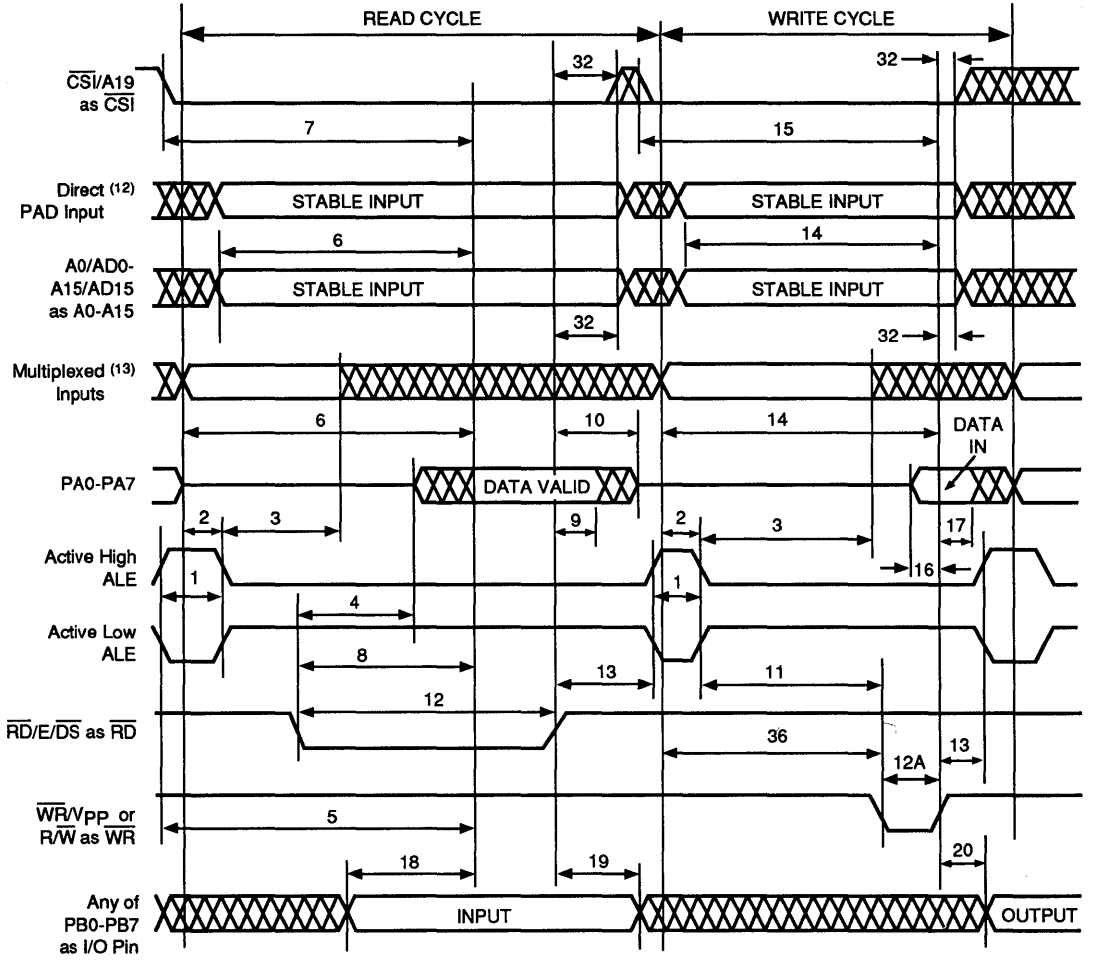
See referenced notes on page 128.

Figure 4. Timing of 16-Bit Multiplexed Address/DataBus, CRRWR = 1



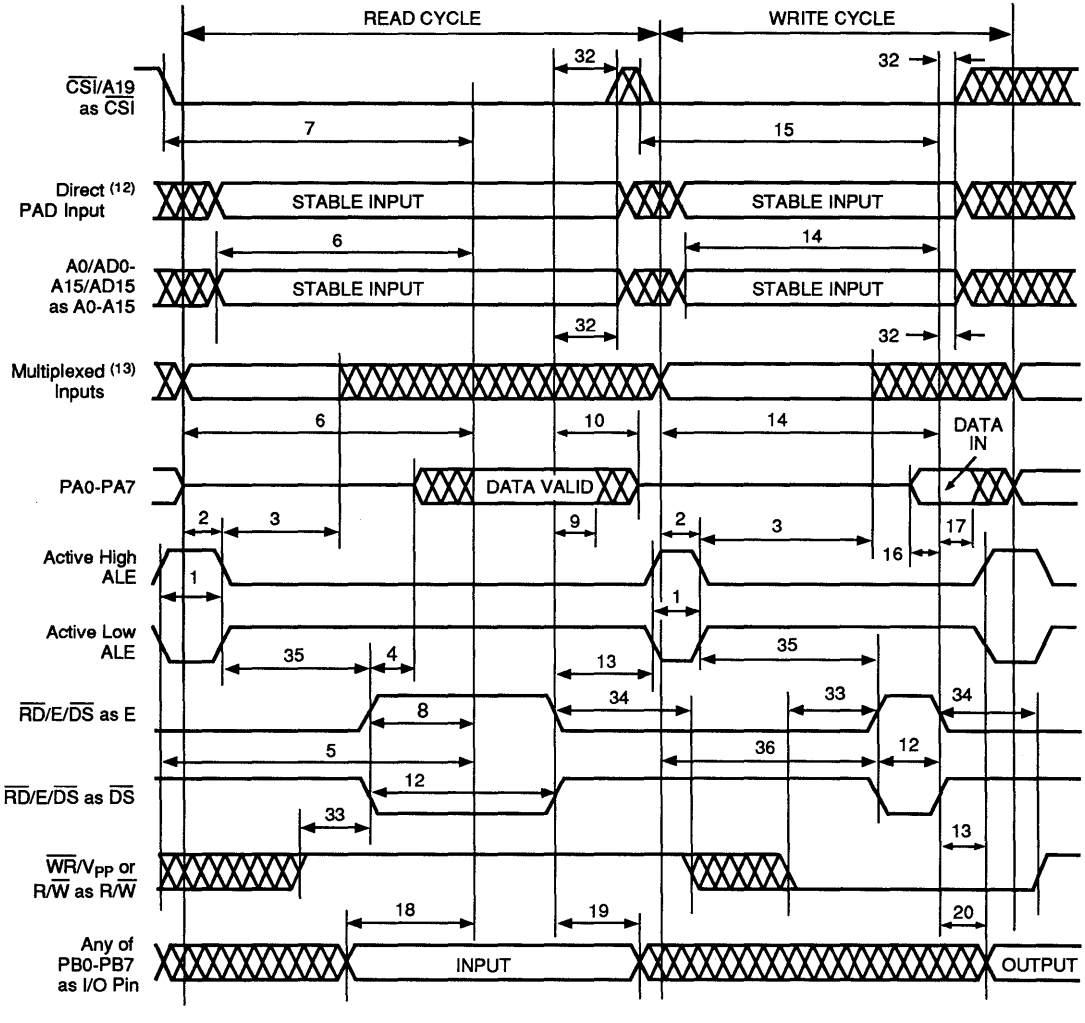
See referenced notes on page 128.

Figure 5. Timing of 8-Bit Data, Non-Multiplexed Address/DataBus, CRRWR = 0



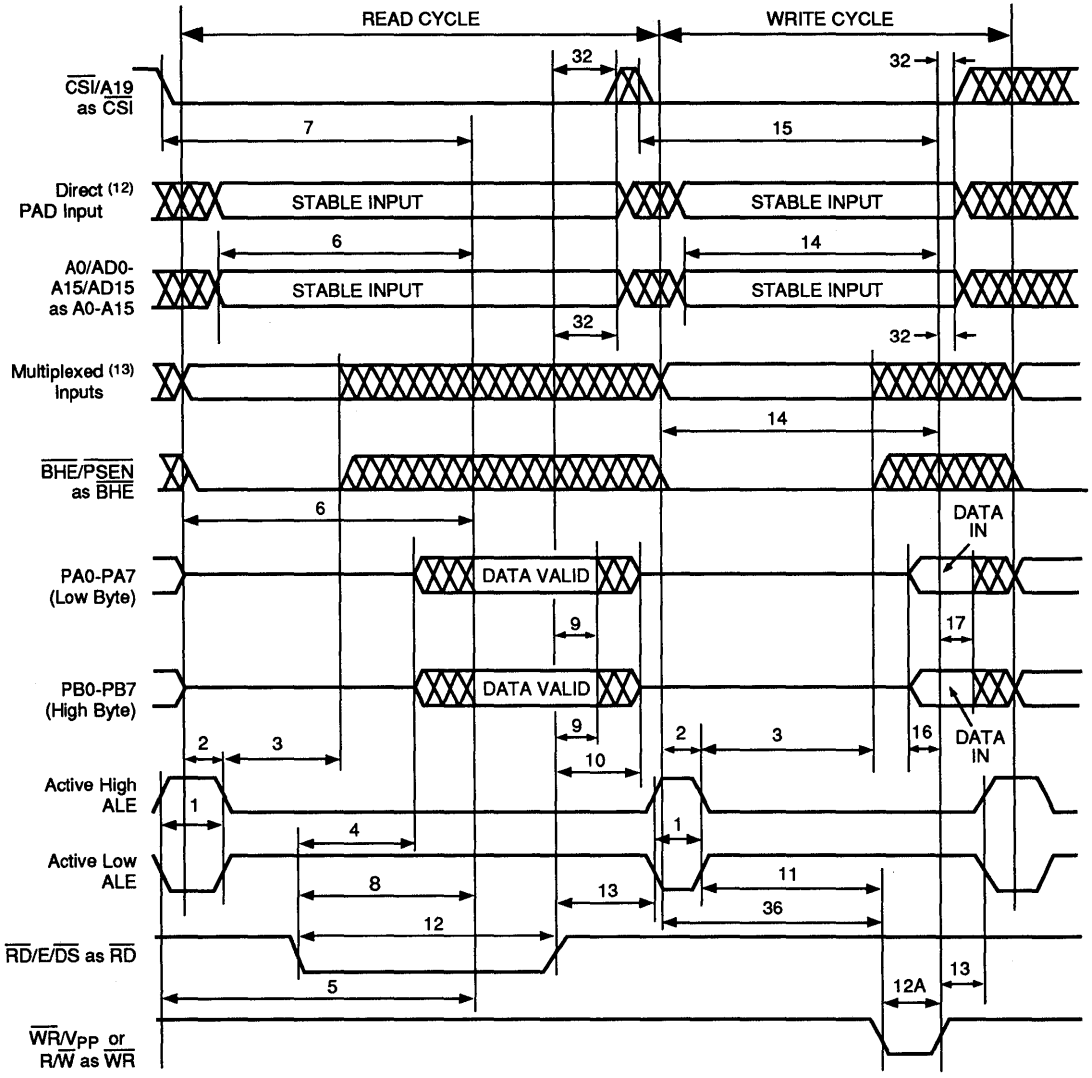
See referenced notes on page 128.

Figure 6. Timing of 8-Bit Data, Non-Multiplexed Address/DataBus, CRRWR = 1



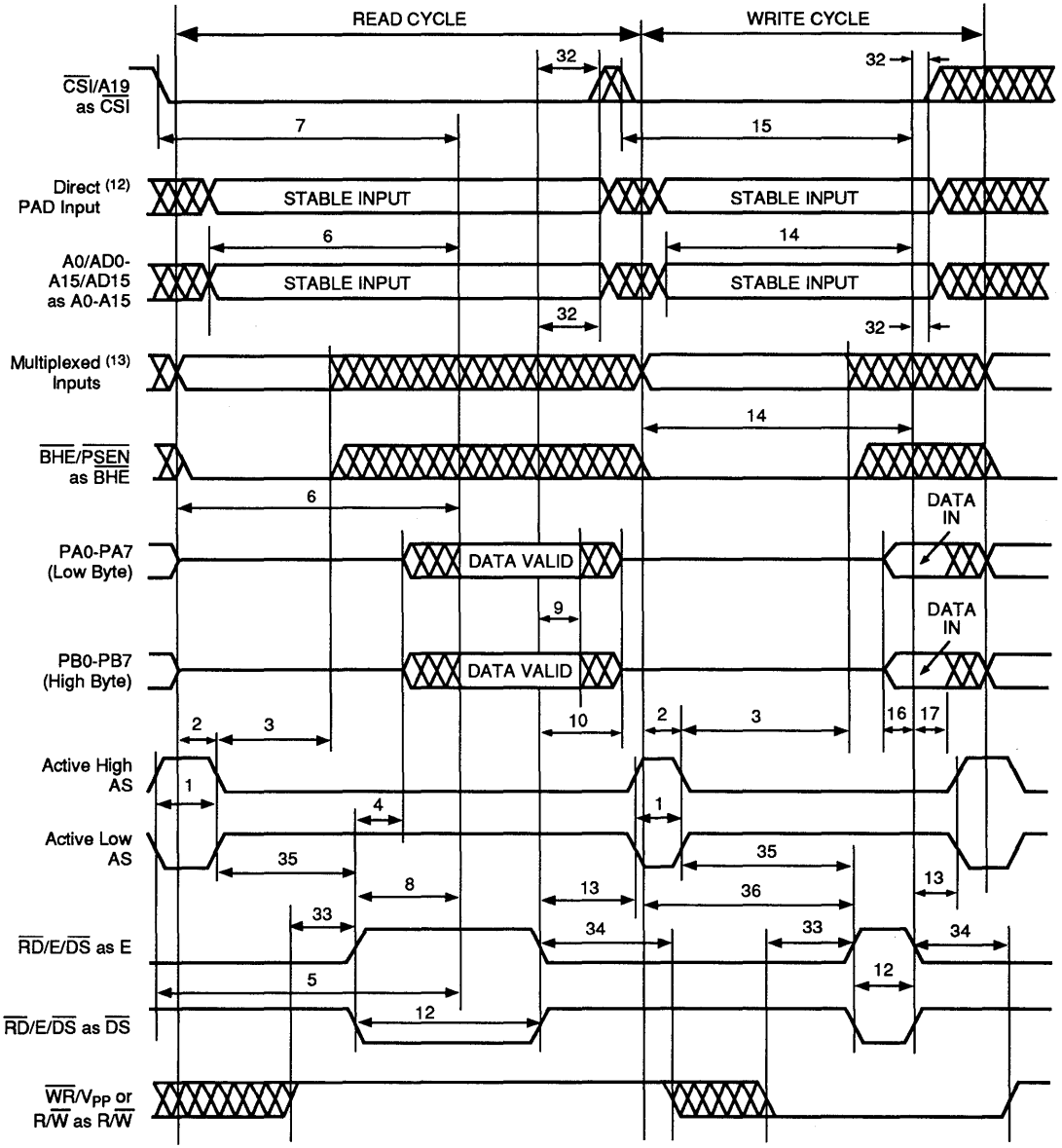
See referenced notes on page 128.

Figure 7. Timing of 16-Bit Non-Multiplexed Address/DataBus, CRRWR = 0



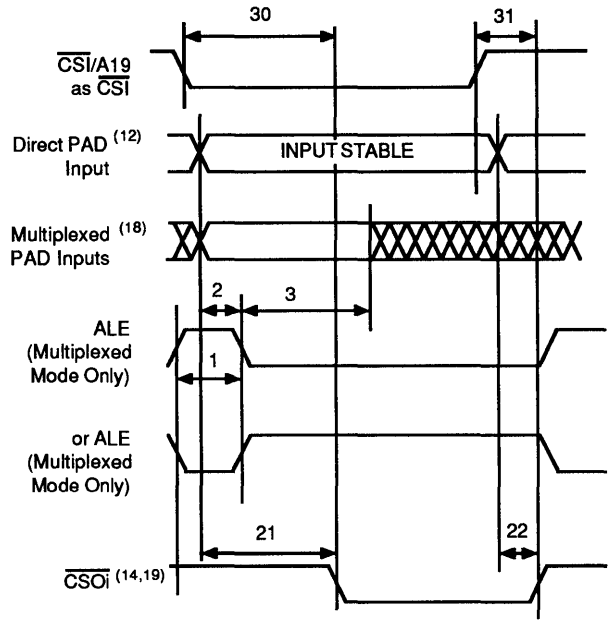
See referenced notes on page 128.

Figure 8. Timing of 16-Bit Non-Multiplexed Address/DataBus, CRRWR = 1



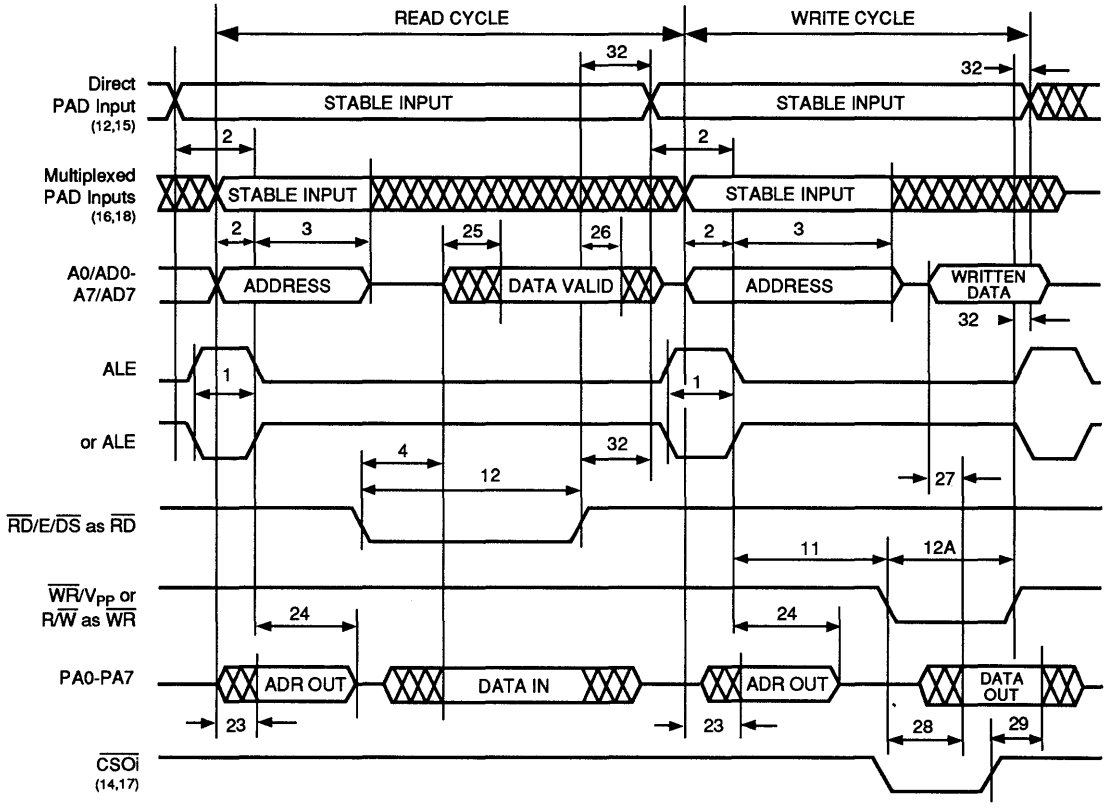
See referenced notes on page 128.

Figure 9. Chip-Select Output Timing



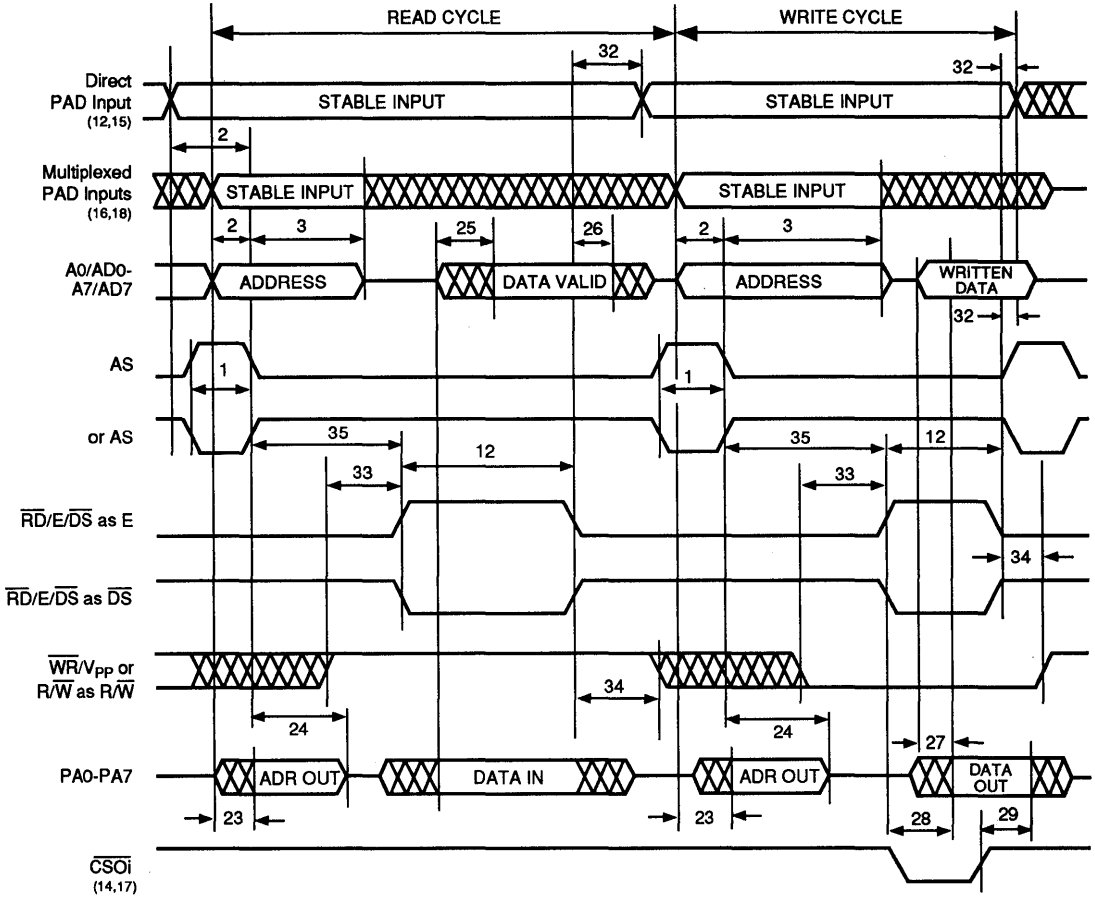
See referenced notes on page 128.

Figure 10. Port A as AD0–AD7 Timing (Track Mode), CRRWR = 0



See referenced notes on page 128.

Figure 11. Port A as AD0–AD7 Timing (Track Mode), CRRWR = 1



Notes for Timing Diagrams

12. Direct PAD input = any of the following direct PAD input lines: $\overline{CSI}$/A19 as transparent A19, $\overline{RD}$/E, $\overline{WR}$ or R/$\overline{W}$, transparent PC0–PC2, ALE in non-multiplexed modes.
13. Multiplexed inputs: any of the following inputs that are latched by the ALE (or AS): A0/AD0–A15/AD15, $\overline{CSI}$/A19 as ALE dependent A19, ALE dependent PC0–PC2.
14. $\overline{CSOi}$ = any of the chip-select output signals coming through Port B ($\overline{CS0}$–$\overline{CS7}$) or through Port C ($\overline{CS8}$–$\overline{CS10}$).
15. CSADOUT1, which internally enables the address transfer to Port A, should be derived only from direct PAD input signals, otherwise the address propagation delay is slowed down.
16. CSADIN and CSADOUT2, which internally enable the data-in or data-out transfers, respectively, can be derived from any combination of direct PAD inputs and multiplexed PAD inputs.
17. The write operation signals are included in the $\overline{CSOi}$ expression.
18. Multiplexed PAD inputs: any of the following PAD inputs that are latched by the ALE (or AS) in the multiplexed modes: A11/AD11–A15/AD15, $\overline{CSI}$/A19 as ALE dependent A19, ALE dependent PC0–PC2.
19. $\overline{CSOi}$ product terms can include any of the PAD input signals except for reset and $\overline{CSI}$.

Pin Capacitance[20]

Symbol	Parameter	Conditions	Typical[21]	Max	Unit
C_{IN}	Capacitance (for input pins only)	V_{IN} = 0 V	4	6	pF
C_{OUT}	Capacitance (for input/output pins)	V_{OUT} = 0 V	8	12	pF
C_{VPP}	Capacitance (for WR/V_{PP} or R/W/V_{PP})	V_{PP} = 0 V	18	25	pF

NOTES: 20. This paramter is only sampled and is not 100% tested.
21. Typical values are for T_A = 25°C and nominal supply voltages.

Figure 12. AC Testing Input/Output Waveform

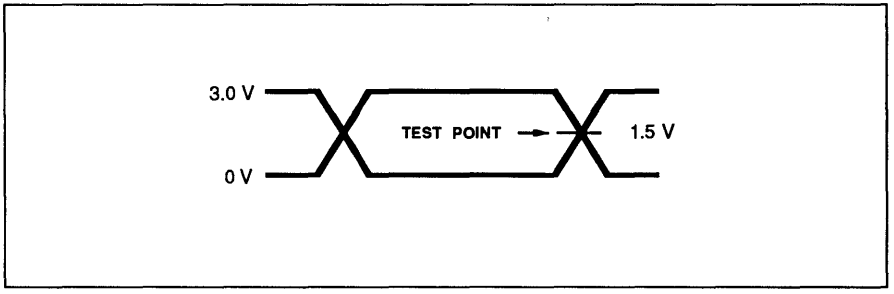
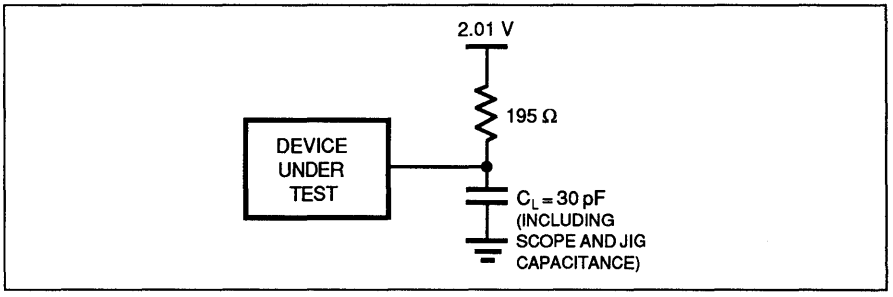


Figure 13. AC Testing Load Circuit



Erasure and Programming

To clear all locations of their programmed contents, expose the device to ultra-violet light source. A dosage of 15 W second/cm^2 is required. This dosage can be obtained with exposure to a wavelength of 2537 Å and intensity of 12000 µW/cm^2 for 15 to 20 minutes. The device should be about 1 inch from the source, and all filters should be removed from the UV light source prior to erasure.

The PSD3XX and similar devices will erase with light sources having wavelengths shorter than 4000 Å. Although the erasure times will be much longer than with UV sources at 2537 Å, exposure to fluorescent light and sunlight eventually erases the device. For maximum system reliability, these sources should be avoided. If used in such an environment, the package windows should be covered by an opaque substance.

Upon delivery from WSI, or after each erasure, the PSD3XX device has all bits in the PAD and EPROM in the "1" or high state. The configuration bits are in the "0" or low state. The code, configuration, and PAD MAP data are loaded through the procedure of programming.

Pin Assignments

Pin Name	44-Pin PLCC/CLCC Package
$\overline{BHE}/\overline{PSEN}$	1
$\overline{WR}/V_{PP}$ or $R/\overline{W}$	2
RESET	3
PB7	4
PB6	5
PB5	6
PB4	7
PB3	8
PB2	9
PB1	10
PB0	11
GND	12
ALE or AS	13
PA7	14
PA6	15
PA5	16
PA4	17
PA3	18
PA2	19
PA1	20
PA0	21
$\overline{RD}/E/\overline{DS}$	22
AD0/A0	23
AD1/A1	24
AD2/A2	25
AD3/A3	26
AD4/A4	27
AD5/A5	28
AD6/A6	29
AD7/A7	30
AD8/A8	31
AD9/A9	32
AD10/A10	33
GND	34
AD11/A11	35
AD12/A12	36
AD13/A13	37
AD14/A14	38
AD15/A15	39
PC0	40
PC1	41
PC2	42
A19/$\overline{CSI}$	43
V_{CC}	44

Package Information

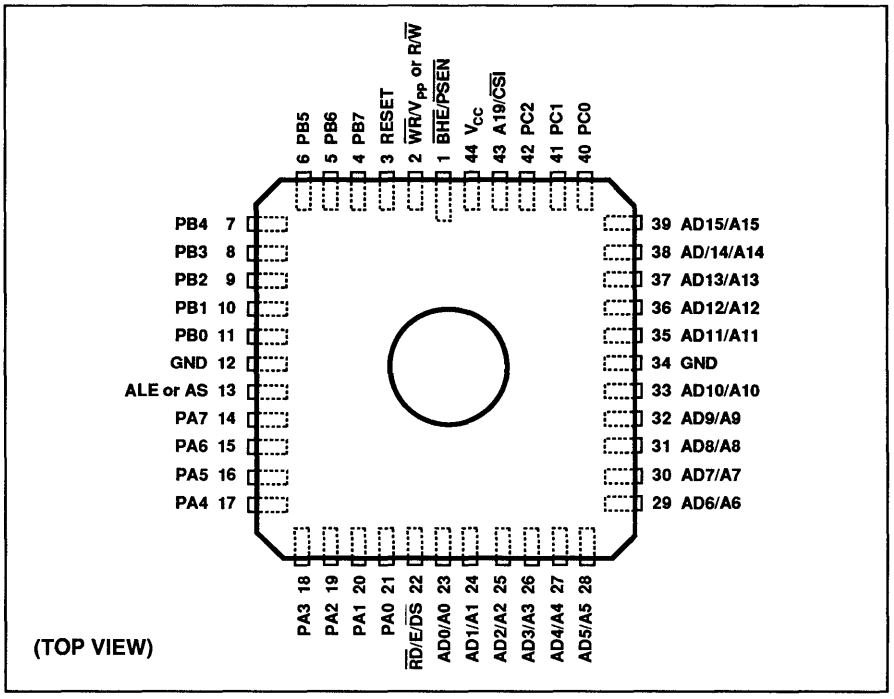


Figure 1. Drawing L4 — 44 Pin Ceramic Leaded Chip Carrier (CLCC) with Window (Package Type L)

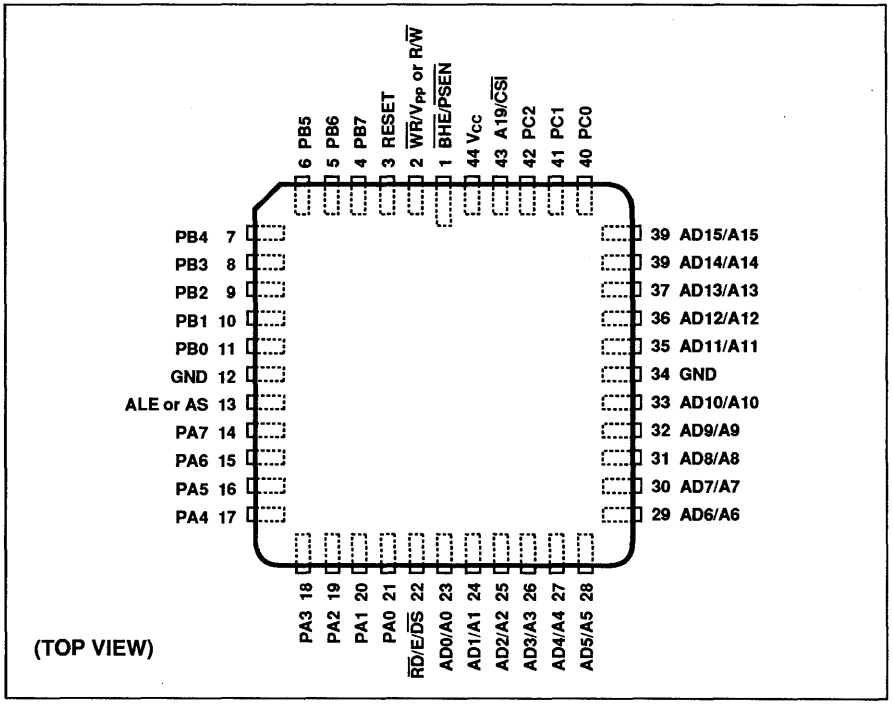


Figure 2. Drawing J2 — 44 Pin Plastic Leaded Chip Carrier (PLCC) with Window (Package Type J)

Ordering Information

Part Number	Spd. (ns)	Package Type	Package Drawing	Operating Temperature Range	WSI Manufacturing Procedure
PSD303-90 A	90	44-pin PLCC	J2	Commercial	Standard
PSD303-90 KA	90	44-pin CLCC	L4	Commercial	Standard
PSD303-12 A	120	44-pin PLCC	J2	Commercial	Standard
PSD303-12 KA	120	44-pin CLCC	L4	Commercial	Standard
PSD303-15 A	150	44-pin PLCC	J2	Commercial	Standard
PSD303-15I A	150	44-pin PLCC	J2	Industrial	Standard
PSD303-15KA	150	44-pin CLCC	L4	Commercial	Standard
PSD303-15I KA	150	44-pin CLCC	L4	Industrial	Standard
PSD303-20 A	200	44-pin PLCC	J2	Commercial	Standard
PSD303-20I A	200	44-pin PLCC	J2	Industrial	Standard
PSD303-20 KA	200	44-pin CLCC	L4	Commercial	Standard
PSD303-20I KA	200	44-pin CLCC	L4	Industrial	Standard

Field-programmable microcontroller peripheral — PSD313

Key Features

- Single Chip Programmable Peripheral for Microcontroller-based Applications
- 19 Individually Configurable I/O pins that can be used as:
  - Microcontroller I/O port expansion
  - Programmable Address Decoder (PAD) I/O
  - Latched address output
  - Open drain or CMOS
- Two Programmable Arrays (PAD A & PAD B)
  - Total of 40 Product Terms and up to 16 Inputs and 24 Outputs
  - Direct Address Decoding up to 1 Meg address space and up to 16 Meg with paging
  - Logic replacement
- "No Glue" Microcontroller Chip-Set
  - Built-in address latches for multiplexed address/data bus
  - Non-multiplexed address/data bus mode
  - 8-bit data bus width
  - ALE and Reset polarity programmable
  - Selectable modes for read and write control bus as $\overline{RD}/\overline{WR}$, $R/\overline{W}/E$, or $R/\overline{W}/\overline{DS}$
  - $\overline{PSEN}$ pin for 8051 users
- Built-In Page Logic
  - To Expand the Address Space of Microcontrollers with Limited Address Space Capabilities
  - Up to 16 pages
- 1 M bit of UV EPROM
  - Configurable as 128K x 8
  - Divides into 8 equal mappable blocks for optimized mapping
  - Block resolution is 16K x 8
  - 120 ns EPROM access time, including input latches and PAD address decoding.
- 16 Kbit Static RAM
  - Configurable as 2K x 8
  - 120 ns SRAM access time, including input latches and PAD address decoding
- Address/Data Track Mode
  - Enables easy Interface to Shared Resources (e.g., Mail Box SRAM) with other Microcontrollers or a Host Processor
- Built-In Security
  - Locks the PSD313 and PAD Decoding Configuration
- Available in a Choice of Packages
  - 44 Pin PLDCC and CLDCC
- Simple Menu-Driven Software: Configure the PSD313 on an IBM PC
- Pin Compatible with the PSD311 and PSD312

Security Mode

Security Mode in the PSD3XX locks the contents of the PAD A , PAD B and all the configuration bits. The EPROM, SRAM, and I/O contents can be accessed only through the PAD. The Security Mode can be set by the MAPLE or Programming software. In window packages, the mode is erasable through UV full part erasure. In the security mode, the PSD3XX contents cannot be copied on a programmer.

CMiser-Bit

The CMiser-Bit provides a programmable option for power-sensitive applications that require further reduction in power consumption. The CMiser-Bit (CMiser = 1) in the Maple portion of the PSD3XX sytem development software can be used to reduce power consumption. The CMiser-Bit turns off the EPROM blocks in the PSD3XX whenever the EPROM is not accessed, thereby reducing the active current consumed by the PSD3XX.

In the default mode, or if the PSD3XX is configured without programming the CMiser-Bit (CMiser = 0), the device operates at specified speed and power rating as specified in the A.C. and D.C. Characteristics.

However, if the CMiser-Bit is programmed (CMiser = 1), the device consumes even lower current, and is reflected in the data sheet. This mode has an adder in propagation delay in T5, T6, and T7 parameters in the A.C. Characteristics, and should be added to compute worst-case timing requirements in the application.

Absolute Maximum Ratings[1]

Symbol	Parameter	Condition	Min	Max	Unit
T_{STG}	Storage Temperature	CERDIP	– 65	+ 150	°C
		PLASTIC	– 65	+ 125	°C
	Voltage on any Pin	With Respect to GND	– 0.6	+ 7	V
V_{PP}	Programming Supply Voltage	With Respect to GND	– 0.6	+ 14	V
V_{CC}	Supply Voltage	With Respect to GND	– 0.6	+ 7	V
	ESD Protection			>2000	V

NOTE: 1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at theses or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods of time may affect device reliability.

Operating Range

Range	Temperature	V_{CC}	V_{CC} Tolerance		
			-12	-15	-20
Commercial	0° C to +70°C	+ 5 V	± 10%	± 10%	± 10%
Industrial	–40° C to +80°C	+ 5 V		± 10%	± 10%
Military	–55° C to +125°C	+ 5 V			± 10%

Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	Supply Voltage	All Speeds	4.5	5	5.5	V
V_{IH}	High-level Input Voltage	V_{CC} = 4.5 V to 5.5 V	2			V
V_{IL}	Low-level Input Voltage	V_{CC} = 4.5 V to 5.5 V	0		0.8	V

DC Characteristics

Symbol	Parameter	Conditions				CMiser = 1 Subtract:			Unit
			Min	Typ	Max	Min	Typ	Max	
V_{OL}	Output Low Voltage	I_{OL} = 20 µA V_{CC} = 4.5 V		0.01	0.1				V
		I_{OL} = 8 mA V_{CC} = 4.5 V		0.15	0.45				V
V_{OH}	Output High Voltage	I_{OH} = –20 µA V_{CC} = 4.5 V	4.4	4.49					V
		I_{OH} = –2 mA V_{CC} = 4.5 V	2.4	3.9					V
I_{SB1}	V_{CC} Standby Current (CMOS) (Notes 2 and 4)	Comm'l		50	100				µA
		Ind/Mil		75	150				µA
I_{CC1}	Active Current (CMOS) (No Internal Memory Block Selected) (Notes 2 and 5)	Comm'l (Note 6)		16	35		7	10	mA
		Comm'l (Note 7)		28	50		7	10	mA
		Ind/Mil (Note 6)		16	45		7	10	mA
		Ind/Mil (Note 7)		28	60		7	10	mA
I_{CC2}	Active Current (CMOS) (EPROM Block Selected) (Notes 2 and 5)	Comm'l (Note 6)		16	35		0	0	mA
		Comm'l (Note 7)		28	50		0	0	mA
		Ind/Mil (Note 6)		16	45		0	0	mA
		Ind/Mil (Note 7)		28	60		0	0	mA
I_{CC3}	Active Current (CMOS) (SRAM Block Selected (Notes 2and 5)	Comm'l (Note 6)		47	80		7	10	mA
		Comm'l (Note 7)		59	95		7	10	mA
		Ind/Mil (Note 6)		47	100		7	10	mA
		Ind/Mil (Note 7)		59	115		7	10	mA
I_{LI}	Input Leakage Current	V_{IN} = 5.5 V or GND	–1	±0.1	1				µA
I_{LO}	Output Leakage Current	V_{OUT} = 5.5 V or GND	–10	±5	10				µA

NOTES: 2. CMOS inputs: GND ± 0.3 V or V_{CC} ± 0.3V.
3. TTL inputs: $V_{IL} \leq 0.8$ V, $V_{IH} \geq 2.0$ V.
4. $\overline{CSI}$/A19 is high and the part is in a power-down configuration mode.
5. Add 3.0 mA/MHz for AC power component (power = AC + DC).
6. Ten (10) PAD product terms active. (Add 380 µA per product term, typical, or 480 µA per product term maximum
7. Forty-one (41) PAD product terms active.

AC Characteristics

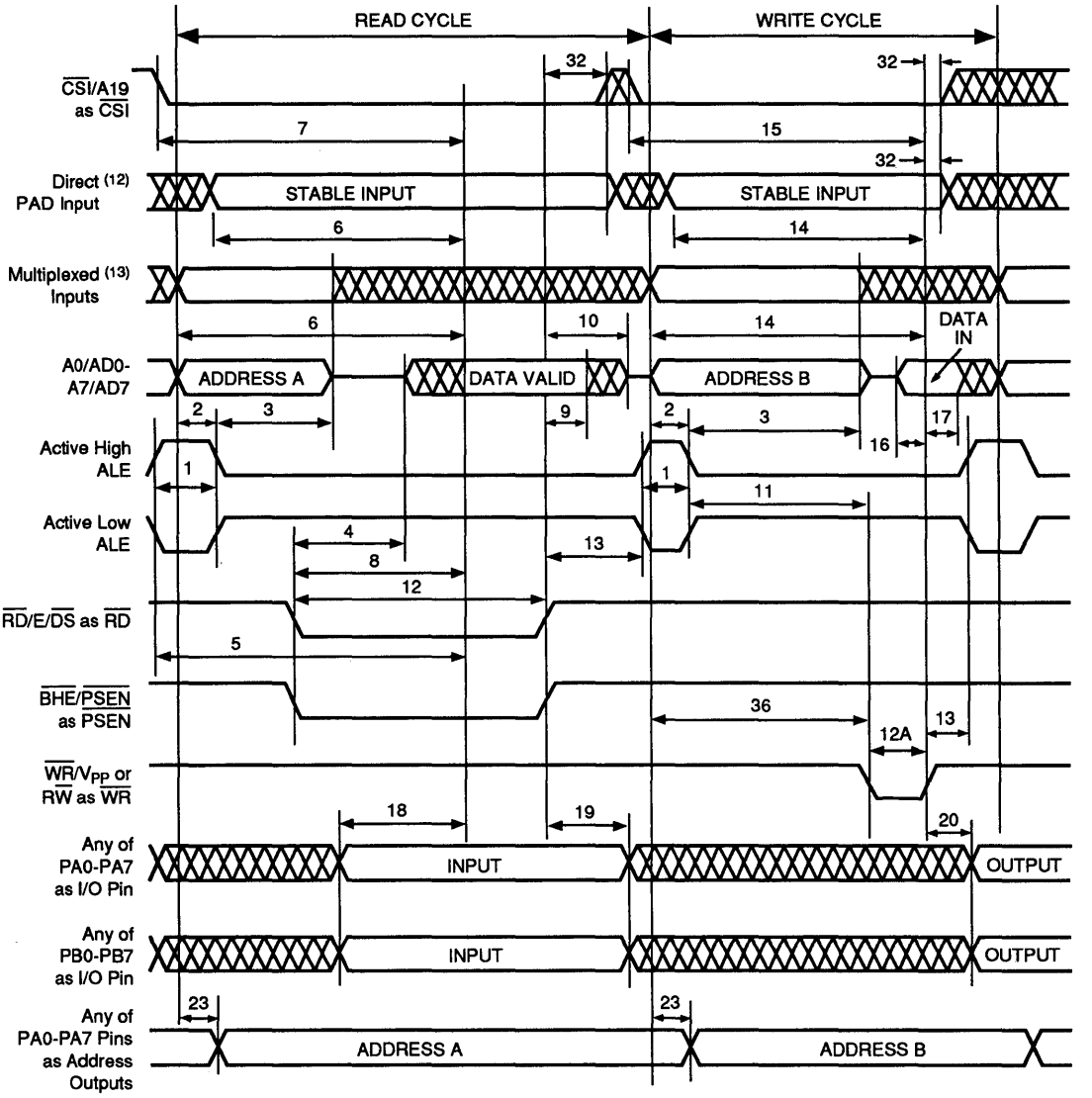
Symbol	Parameter	-90		-12		-15		-20		CMiser = 1 Add:	Unit
		Min	Max	Min	Max	Min	Max	Min	Max		
T1	ALE or AS Pulse Width	20		30		40		50		0	ns
T2	Address Set-up Time	5		9		12		15		0	ns
T3	Address Hold Time	8		9		12		15		0	ns
T4	Leading Edge of Read to Data Active	0		0		0		0		0	ns
T5	ALE Valid to Data Valid		100		130		160		200	10	ns
T6	Address Valid to Data Valid		90		120		150		200	10	ns
T7	$\overline{CSI}$ Active to Data Valid		100		130		160		200	15	ns
T8	Leading Edge of Read to Data Valid		32		38		55		60	0	ns
T9	Read Data Hold Time	0		0		0		0		0	ns
T10	Trailing Edge of Read to Data High-Z		32		32		35		40	0	ns
T11	Trailing Edge of ALE or AS to Leading Edge of Write	0		0		0		0		0	ns
T12	$\overline{RD}$, E, $\overline{PSEN}$, or $\overline{DS}$ Pulse Width	40		45		60		75		0	ns
T12A	$\overline{WR}$ Pulse Width	20		25		35		45		0	ns
T13	Trailing Edge of Write or Read to Leading Edge of ALE or AS	0		0		0		0		0	ns
T14	Address Valid to Trailing Edge of Write	90		120		150		200		0	ns
T15	$\overline{CSI}$ Active to Trailing Edge of Write	100		130		160		200		0	ns
T16	Write Data Set-up Time	20		25		30		40		0	ns
T17	Write Data Hold Time	5		5		10		15		0	ns
T18	Port to Data Out Valid Propagation Delay		30		30		35		45	0	ns
T19	Port Input Hold Time	0		0		0		0		0	ns
T20	Trailing Edge of Write to Port Output Valid	40		40		50		60		0	ns
T21	ADi or Control to CSOi Valid	6	25	6	30	6	35	5	45	0	ns
T22	ADi or Control to CSOi Invalid	5	25	5	30	4	35	4	45	0	ns

AC Characteristics (Cont.)

Symbol	Parameter	-90		-12		-15		-20		CMiser = 1 Add:	Unit
		Min	Max	Min	Max	Min	Max	Min	Max		
T23	Track Mode Address Propagation Delay: CSADOUT1 Already True		22		22		28		28	0	ns
T23A	Track Mode Address Propagation Delay: CSADOUT1 Becomes True During ALE or AS		33		33		50		50	0	ns
T24	Track Mode Trailing Edge of ALE or AS to Address High-Z		32		32		35		40	0	ns
T25	Track Mode Read Propagation Delay		29		29		35		35	0	ns
T26	Track Mode Read Hold Time	11	29	11	29	10	29	10	35	0	ns
T27	Track Mode Write Cycle, Data Propagation Delay		20		20		30		30	0	ns
T28	Track Mode Write Cycle, Write to Data Propagation Delay	8	30	8	30	7	40	7	55	0	ns
T29	Hold Time of Port A Valid During Write $\overline{CSOi}$ Trailing Edge	2		2		2		2		0	ns
T30	$\overline{CSI}$ Active to $\overline{CSOi}$ Active	9	40	9	45	9	50	8	60	0	ns
T31	$\overline{CSI}$ Inactive to $\overline{CSOi}$ Inactive	9	40	9	45	9	50	8	60	0	ns
T32	Direct PAD Input as Hold Time	10		10		12		15		0	ns
T33	R/$\overline{W}$ Active to E or $\overline{DS}$ Start	20		20		30		40		0	ns
T34	E or $\overline{DS}$ End to R/$\overline{W}$	20		20		30		40		0	ns
T35	AS Inactive to E high	0		0		0		0		0	ns
T36	Address to Leading Edge of Write	20		20		25		30		0	ns

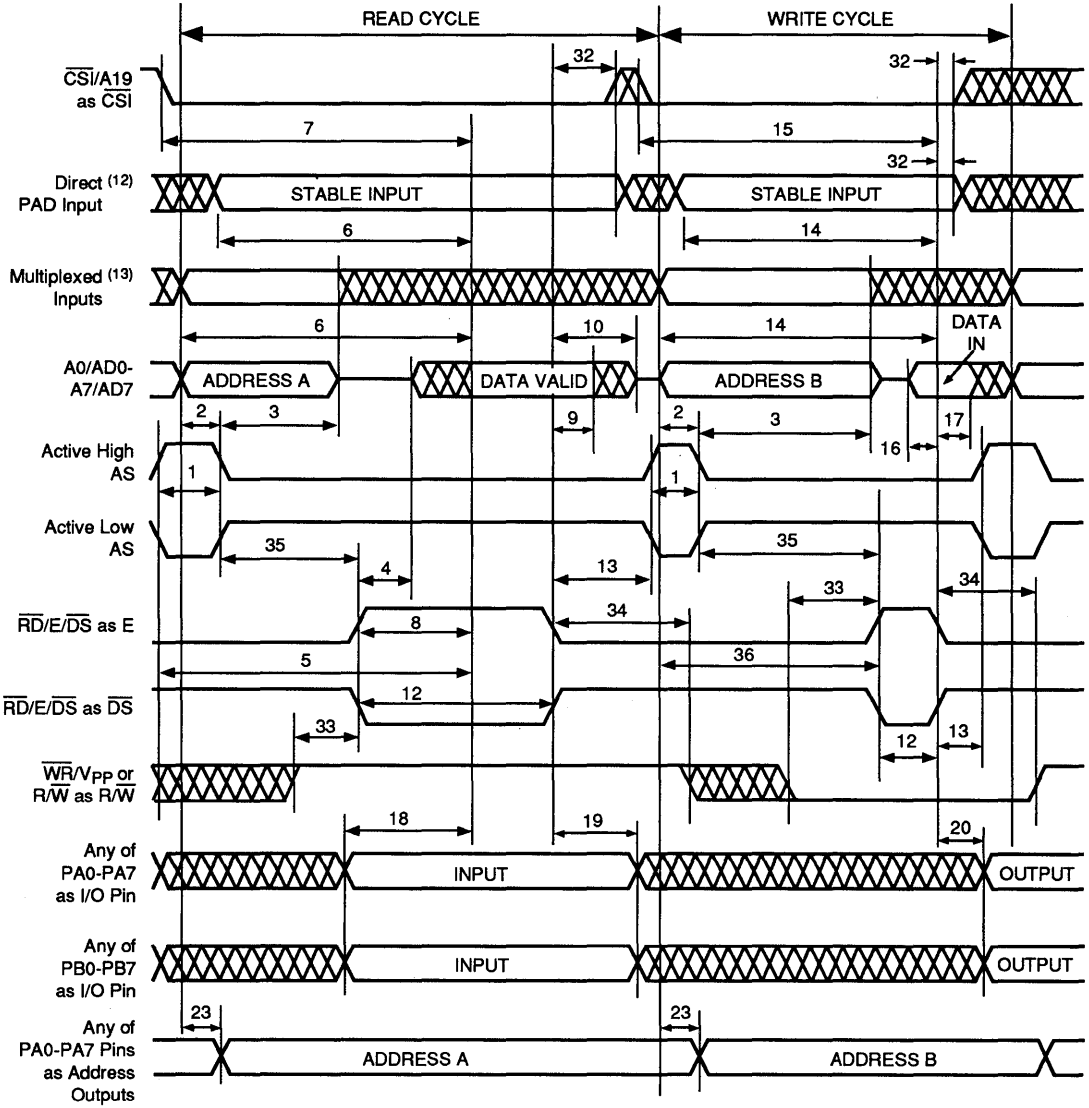
NOTES: 8. ADi = any address line.
9. $\overline{CSOi}$ = any of the chip-select output signals coming through Port B ($\overline{CS0}$–$\overline{CS7}$) or through Port C ($\overline{CS8}$–$\overline{CS10}$).
10. Direct PAD input = any of the following direct PAD input lines: $\overline{CSI}$/A19 as transparent A19, $\overline{RD}$/E/$\overline{DS}$, $\overline{WR}$ or R/$\overline{W}$, transparent PC0–PC2, ALE (or AS).
11. Control signals $\overline{RD}$/E/$\overline{DS}$ or $\overline{WR}$ or R/$\overline{W}$.

Figure 1. Timing of 8-Bit Multiplexed Address/DataBus, CRRWR = 0



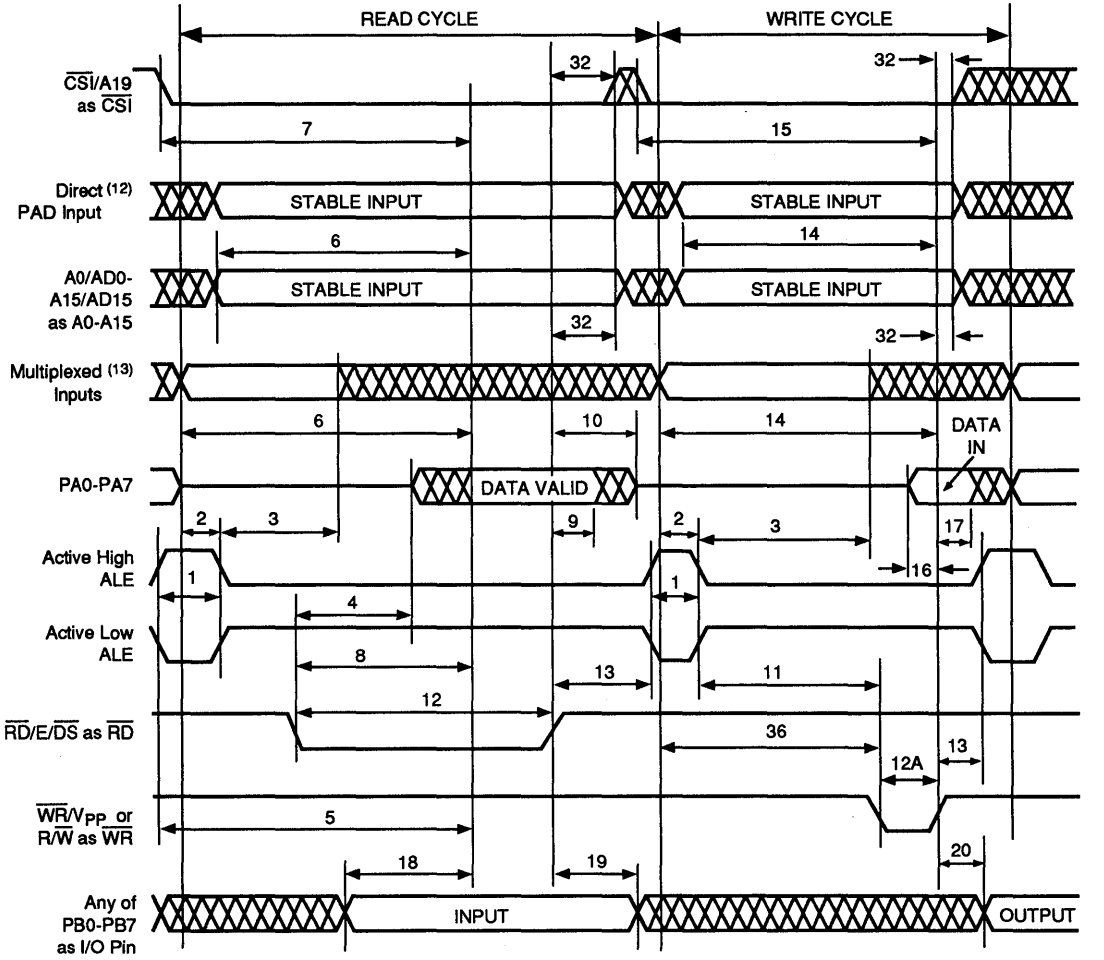
See referenced notes on page 144.

Figure 2. Timing of 8-Bit Multiplexed Address/DataBus, CRRWR = 1



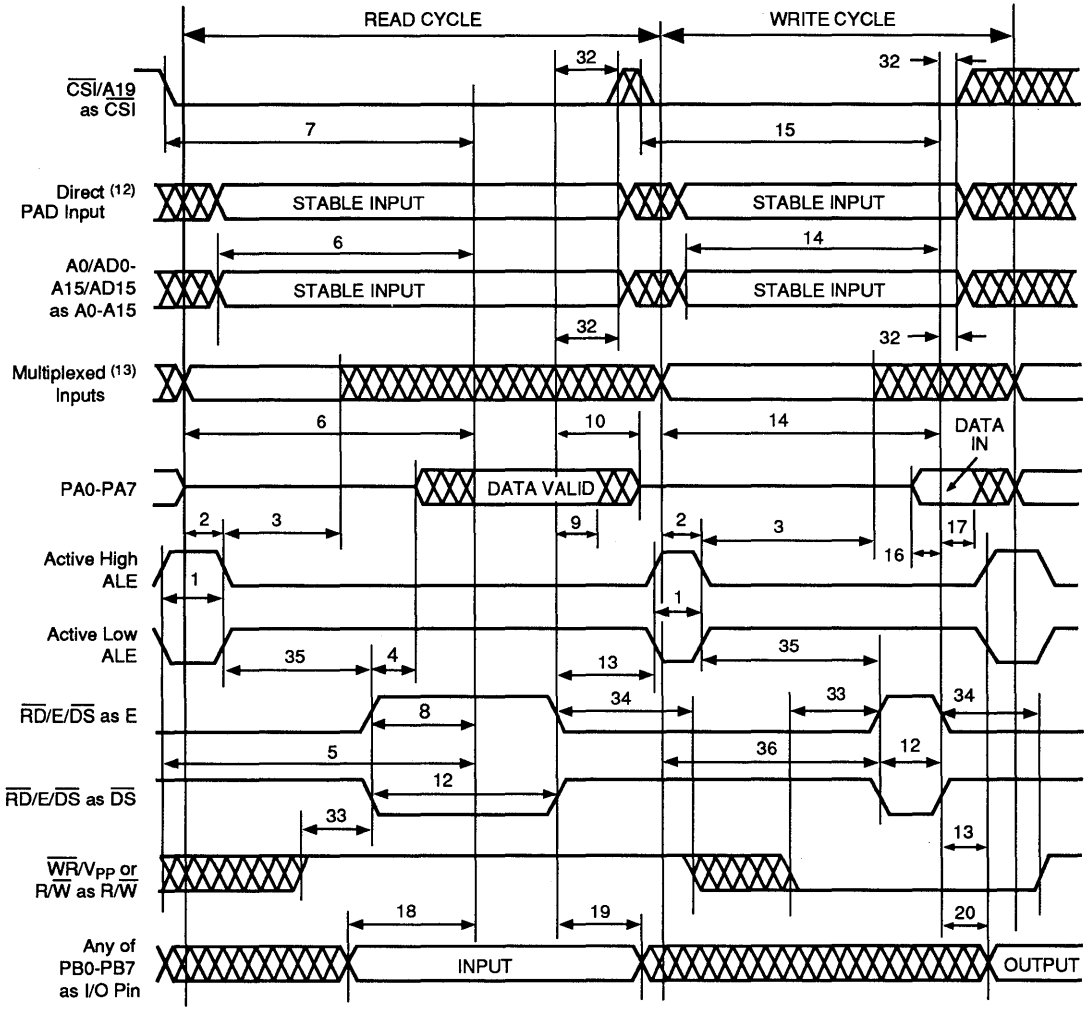
See referenced notes on page 144.

Figure 3. Timing of 8-Bit Data, Non-Multiplexed Address/DataBus, CRRWR = 0



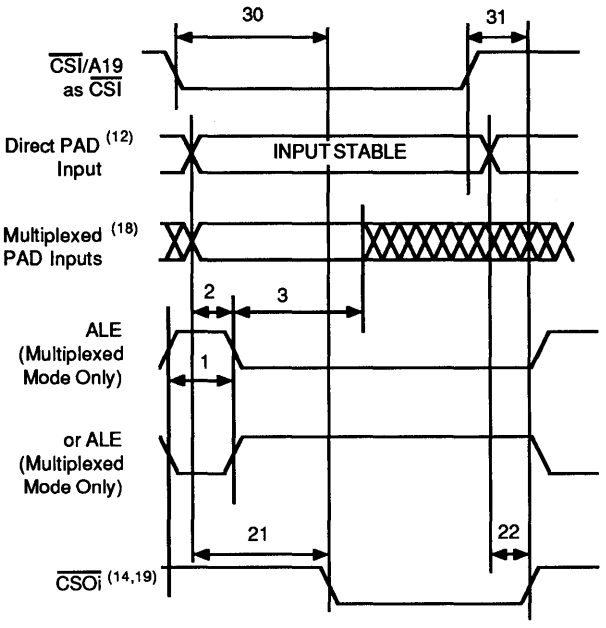
See referenced notes on page 144.

Figure 4. Timing of 8-Bit Data, Non-Multiplexed Address/DataBus, CRRWR = 1



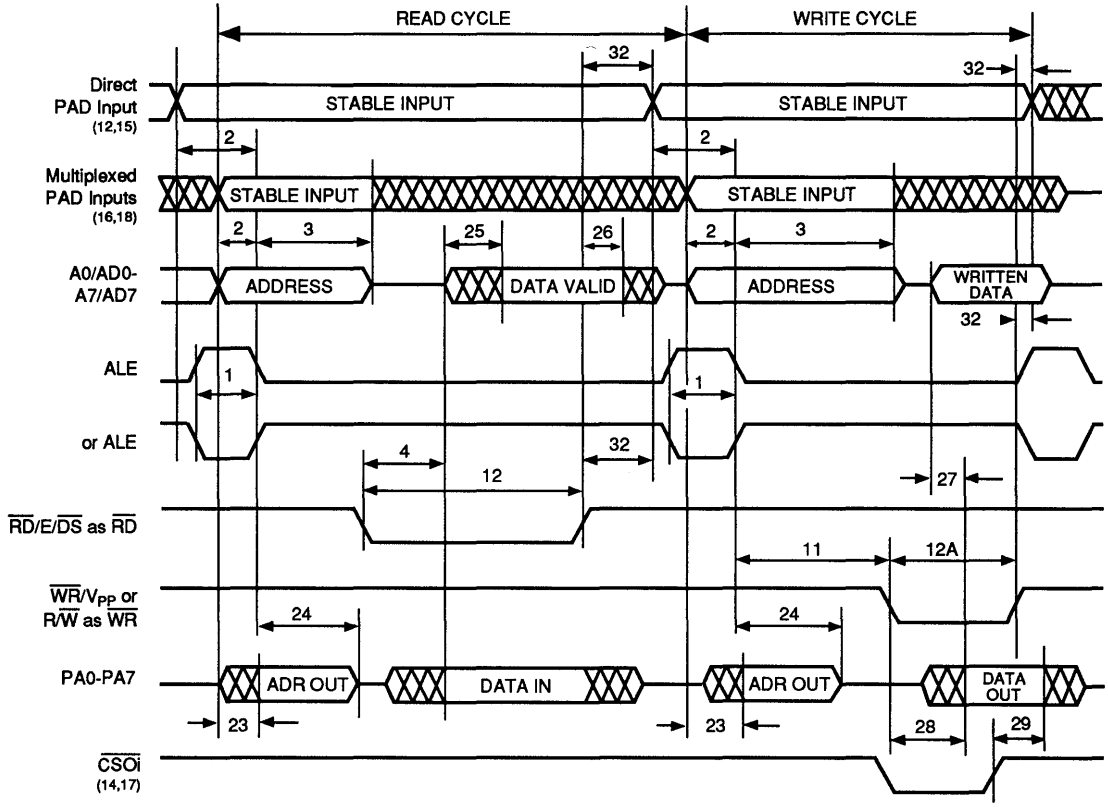
See referenced notes on page 144.

Figure 5. Chip-Select Output Timing



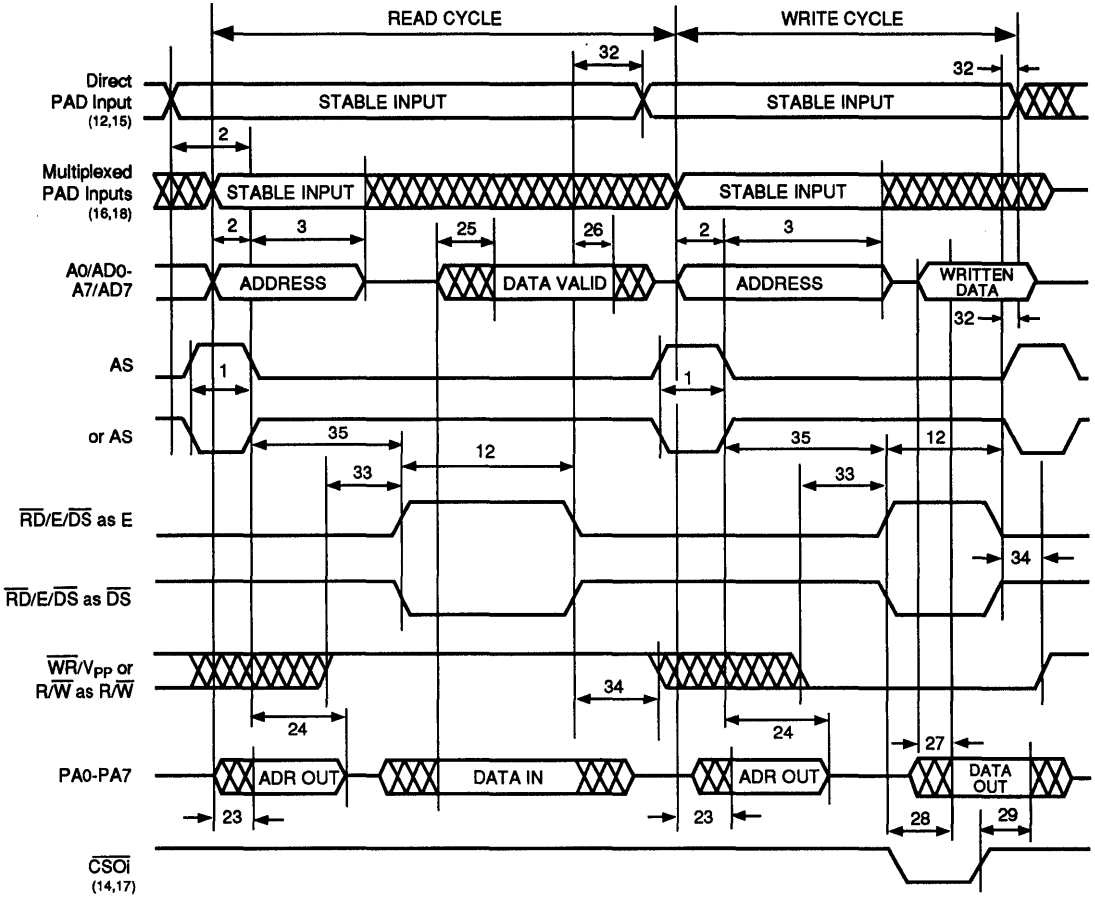
See referenced notes on page 144.

Figure 6. Port A as AD0–AD7 Timing (Track Mode), CRRWR = 0



See referenced notes on page 144.

Figure 7. Port A as AD0–AD7 Timing (Track Mode), CRRWR = 1



Notes for Timing Diagrams

12. Direct PAD input = any of the following direct PAD input lines: $\overline{CSI}$/A19 as transparent A19, $\overline{RD}$/E, $\overline{WR}$ or R/$\overline{W}$, transparent PC0–PC2, ALE in non-multiplexed modes.
13. Multiplexed inputs: any of the following inputs that are latched by the ALE (or AS): A0/AD0–A15/AD15, $\overline{CSI}$/A19 as ALE dependent A19, ALE dependent PC0–PC2.
14. $\overline{CSOi}$ = any of the chip-select output signals coming through Port B ($\overline{CS0}$–$\overline{CS7}$) or through Port C ($\overline{CS8}$–$\overline{CS10}$).
15. CSADOUT1, which internally enables the address transfer to Port A, should be derived only from direct PAD input signals, otherwise the address propagation delay is slowed down.
16. CSADIN and CSADOUT2, which internally enable the data-in or data-out transfers, respectively, can be derived from any combination of direct PAD inputs and multiplexed PAD inputs.
17. The write operation signals are included in the $\overline{CSOi}$ expression.
18. Multiplexed PAD inputs: any of the following PAD inputs that are latched by the ALE (or AS) in the multiplexed modes: A11/AD11–A15/AD15, $\overline{CSI}$/A19 as ALE dependent A19, ALE dependent PC0–PC2.
19. $\overline{CSOi}$ product terms can include any of the PAD input signals except for reset and $\overline{CSI}$.

Pin Capacitance[20]

Symbol	Parameter	Conditions	Typical[21]	Max	Unit
C_{IN}	Capacitance (for input pins only)	V_{IN} = 0 V	4	6	pF
C_{OUT}	Capacitance (for input/output pins)	V_{OUT} = 0 V	8	12	pF
C_{VPP}	Capacitance (for WR/V_{PP} or R/W/V_{PP})	V_{PP} = 0 V	18	25	pF

NOTES: 20. This paramter is only sampled and is not 100% tested.
21. Typical values are for T_A = 25°C and nominal supply voltages.

Figure 8. AC Testing Input/Output Waveform

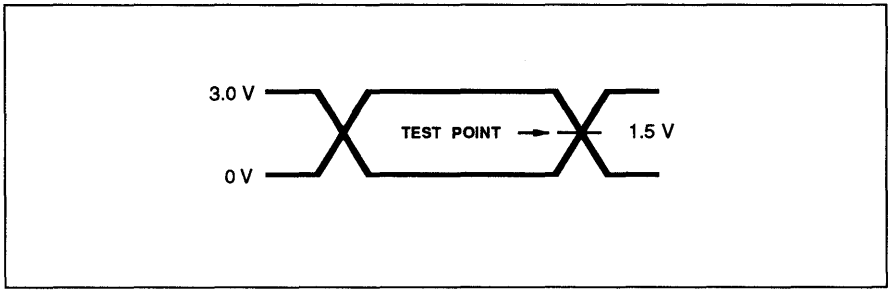
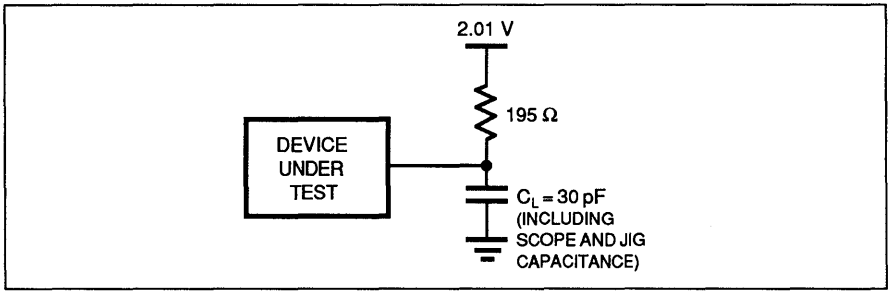


Figure 9. AC Testing Load Circuit



Erasure and Programming

To clear all locations of their programmed contents, expose the device to ultra-violet light source. A dosage of 15 W second/cm^2 is required. This dosage can be obtained with exposure to a wavelength of 2537 Å and intensity of 12000 µW/cm^2 for 15 to 20 minutes. The device should be about 1 inch from the source, and all filters should be removed from the UV light source prior to erasure.

The PSD3XX and similar devices will erase with light sources having wavelengths shorter than 4000 Å. Although the erasure times will be much longer than with UV sources at 2537 Å, exposure to fluorescent light and sunlight eventually erases the device. For maximum system reliability, these sources should be avoided. If used in such an environment, the package windows should be covered by an opaque substance.

Upon delivery, or after each erasure, the PSD3XX device has all bits in the PAD and EPROM in the "1" or high state. The configuration bits are in the "0" or low state. The code, configuration, and PAD MAP data are loaded through the procedure of programming.

Pin Assignments

Pin Name	44-Pin PLCC/CLCC Package
$\overline{PSEN}$	1
$\overline{WR}/V_{PP}$ or R/$\overline{W}$	2
RESET	3
PB7	4
PB6	5
PB5	6
PB4	7
PB3	8
PB2	9
PB1	10
PB0	11
GND	12
ALE or AS	13
PA7	14
PA6	15
PA5	16
PA4	17
PA3	18
PA2	19
PA1	20
PA0	21
$\overline{RD}$/E/$\overline{DS}$	22
AD0/A0	23
AD1/A1	24
AD2/A2	25
AD3/A3	26
AD4/A4	27
AD5/A5	28
AD6/A6	29
AD7/A7	30
A8	31
A9	32
A10	33
GND	34
A11	35
A12	36
A13	37
A14	38
A15	39
PC0	40
PC1	41
PC2	42
A19/$\overline{CSI}$	43
V_{CC}	44

Package Information

Figure 10. Drawing L4 — 44 Pin Ceramic Leaded Chip Carrier (CLCC) with Window (Package Type L)

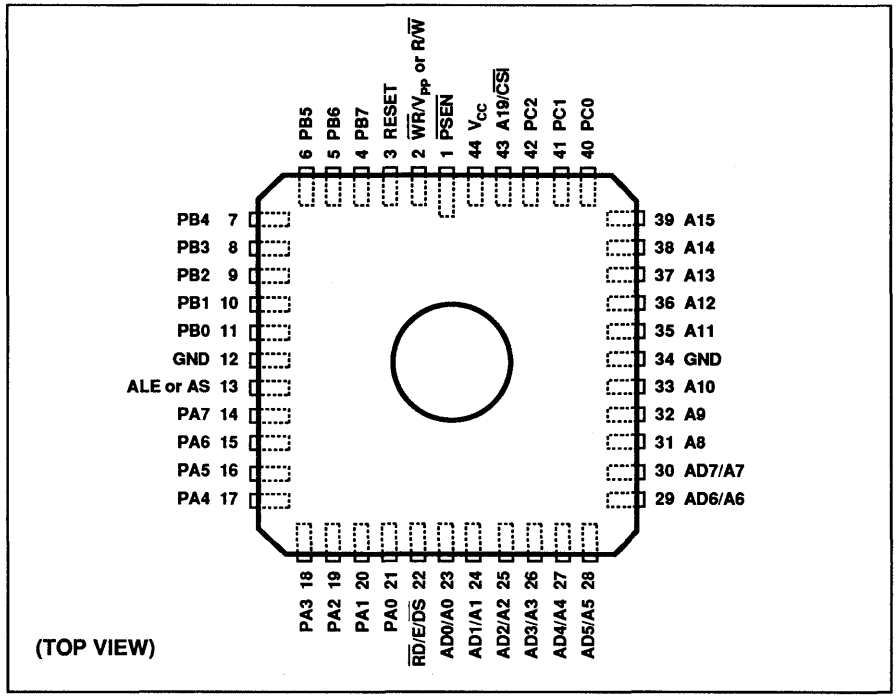
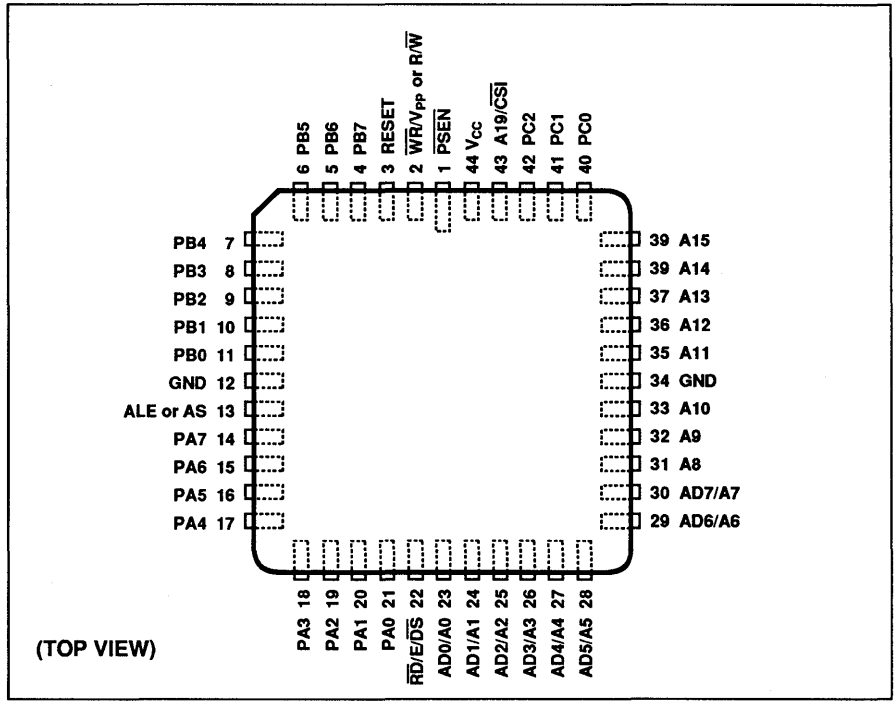


Figure 11. Drawing J2 — 44 Pin Plastic Leaded Chip Carrier (PLCC) with Window (Package Type J)



Ordering Information

Part Number	Spd. (ns)	Package Type	Package Drawing	Operating Temperature Range	Manufacturing Procedure
PSD313-90 A	90	44-pin PLCC	J2	Commercial	Standard
PSD313-90 KA	90	44-pin CLCC	L4	Commercial	Standard
PSD313-12 A	120	44-pin PLCC	J2	Commercial	Standard
PSD313-12 KA	120	44-pin CLCC	L4	Commercial	Standard
PSD313-15 A	150	44-pin PLCC	J2	Commercial	Standard
PSD313-15I A	150	44-pin PLCC	J2	Industrial	Standard
PSD313-15 KA	150	44-pin CLCC	L4	Commercial	Standard
PSD313-15I KA	150	44-pin CLCC	L4	Industrial	Standard
PSD313-20 A	200	44-pin PLCC	J2	Commercial	Standard
PSD313-20I A	200	44-pin PLCC	J2	Industrial	Standard
PSD313-20 KA	200	44-pin CLCC	L4	Commercial	Standard
PSD313-20I KA	200	44-pin CLCC	L4	Industrial	Standard

Section 2
PSD3XXL Family

PSD3XXL Programmable Microcontroller Peripherals

INDEX

3-volt single-chip microcontroller peripherals — PSD3XXL Family

Key Features

- ❑ Eliminates mixing and matching discrete low-voltage parts
- ❑ 3.0 to 5.5 volt operation
- ❑ 19 Individually Configurable I/O pins that can be used as:
  - — Microcontroller I/O port expansion
  - — Programmable Address Decoder (PAD) I/O
  - — Latched address output
  - — Open drain or CMOS
- ❑ Two Programmable Arrays (PAD A & PAD B)
  - — Direct Address Decoding up to 1 Meg address space
  - — Logic replacement of discrete low-voltage PALs®
- ❑ 256Kb to 1Mb of EPROM
- ❑ 16Kb of SRAM
- ❑ "No Glue" Microcontroller Chip-Set
  - — Built-in address latches for multiplexed address/data bus
  - — Non-multiplexed address/data bus mode
  - — ALE polarity programmable
  - — Selectable modes for read and write control
- ❑ 250 ns access time, including input latches and PAD address decoding.
- ❑ Built-In Page Logic
  - — To Expand the Microcontroller Address Space
  - — Up to 16 1Mb pages
- ❑ Address/Data Track Mode
  - — Enables easy Interface to Shared Resources (e.g., Mail Box SRAM) with other Microcontrollers or a Host Processor
- ❑ CMiser-Bit
  - — Programmable option to further reduce power consumption
- ❑ Built-In Security Bit
  - — Locks the Device and PAD Decoding Configuration
- ❑ Available in a Choice of Packages
  - — 44 Pin PLDCC or CLDCC
- ❑ Simple Menu-Driven Software: Configure the Device on an IBM PC

PSD3XXL Family Feature Summary

Part	PLD Inputs/ Product Terms	Ports	EPROM Size	SRAM Size	Configuration	Memory Paging	C-Miser Bit	Security Bit
PSD301®L	14/40	19	256 Kb	16 Kb	x8 or x16		X	X
PSD311L	14/40	19	256 Kb	16 Kb	x8		X	X
PSD302L	18/40	19	512 Kb	16 Kb	x8 or x16	X	X	X
PSD312L	18/40	19	512 Kb	16 Kb	x8	X	X	X
PSD303L	18/40	19	1 Mb	16 Kb	x8 or x16	X	X	X
PSD313L	18/40	19	1 Mb	16 Kb	x8	X	X	X

3-volt single-chip microcontroller peripherals | PSD3XXL Family

Partial Listing of Microcontrollers Supported

- **Motorola family:**
  M6805, M68HC11, M68HC16, M68000/10/20, M60008, M683XX
- **Intel family:**
  8031/8051, 8096/8098, 80186/88, 80196/98
- **Signetics:**
  SC80C451, SC80552
- **TI:**
  SC80C451, TMS320C14
- **Zilog:**
  Z8, Z80, Z180
- **National:**
  HPC16000, HPC46400

Applications

- Computers (Notebook and Portable PCs)
  - Fixed Disk Control, Modem, Imaging, Laser Printer Control
- Telecommunications
  - Modem, Cellular Phone, Digital PBX, Digital Speech, FAX, Digital Signal Processing
- Portable Industrial Equipment
  - Measurement Meters, Data Recorders
- Medical Instrumentation
  - Hearing Aids, Monitoring Equipment, Diagnostic Tools

Introduction

The PSD3XXL Series offers the latest members in the rapidly growing family of PSD devices. They are the market's first low-voltage single-chip solution for microcontroller-based applications where consistent specifications for design, fast time-to-market, small form factor, and low power consumptions are essential. When combined in an 8- or 16-bit system, virtually any microcontroller (68HC11, 8051, 80186, etc.) and the PSD3XXL device work together to create a very powerful chip-set solution. This implementation eliminates mixing and matching low voltage specifications for various discrete components. It also provides all the required control and peripheral elements needed in a microcontroller-based system with no external discrete "glue" logic required.

The solution comes complete with simple system software development tools for integrating the PSD3XXL with the microcontroller. Hosted on IBM PC platforms or compatibles, the easy to use software enables the designer to quickly configure the device and use it immediately.

Product Description

The PSD3XXL family integrates high performance user-configurable blocks of EPROM, SRAM, and programmable logic. The major functional blocks include two programmable logic arrays, PAD A and PAD B, 256K to 1Mbit of EPROM, 16K bits of SRAM, input latches, and output ports. The PSD3XXL family is ideal for applications requiring low power and very small form factors. These include hard disk control, modems, cellular telephones, instrumentation, computer peripherals, military and similar applications. Designers do not have to identify discrete devices at low voltages and then attempt to normalize specifications and operation at 3.3 V.

The PSD3XXL family offers a unique single-chip solution for microcontrollers that need:

- 3.3 volt system operation.
- I/O reconstruction (microcontrollers lose at least two I/O ports when accessing external resources).
- More EPROM and SRAM than the microcontroller's internal memory.
- Chip-select, control, or latched address lines that are otherwise implemented discretely.
- An interface to shared external resources.
- Expanded microcontroller address space.

WSI's PSD3XXL Family Architecture (Figure 1) can efficiently interface with, and enhance, any low-voltage 8- or 16-bit microcontroller system. This is the first solution that provides microcontrollers with port expansion, latched addresses, page logic, two programmable logic arrays (PAD A and PAD B), an interface to shared resources, 256K, 512K or 1M bit EPROM, and 16K bit SRAM on a single chip – all operating at 3.3 V in one package. The PSD3XXL family does not require any glue logic for interfacing to any 8- or 16-bit microcontroller.

The 8051 microcontroller family can take full advantage of the PSD3XXL's separate program and data address spaces. Users of the 68HCXX microcontroller family can change the functionality of the control signals and directly connect the R/$\overline{W}$ and E, or the R/$\overline{W}$ and $\overline{DS}$ signals. (Users of 16-bit microcontrollers, including the 80186, 8096, 80196 and 16XXX, can use the PSD301L/302L/303L in a 16-bit configuration). Address and data buses can be configured as separate or multiplexed, whichever is required by the host processor.

The flexibility of the PSD3XXL I/O ports permits interfacing to shared resources. The arbitration can be controlled internally by PAD A outputs. The user can assign the following functions to these ports: standard I/O pins, chip-select outputs from PAD A and PAD B, or latched address or multiplexed low-order address/data byte. This enables users to design add-on systems such as disk drives, modems, etc., that easily interface to the host bus (e.g., IBM PC, SCSI).

The page register extends the accessible address space of certain microcontrollers from 64 K to 1 M. There are 16 pages that can serve as base address inputs to the PAD, thereby enlarging the address space of 16 address line microcontrollers by a factor of 16.

Figure 1. PSD3XXL Family Architecture

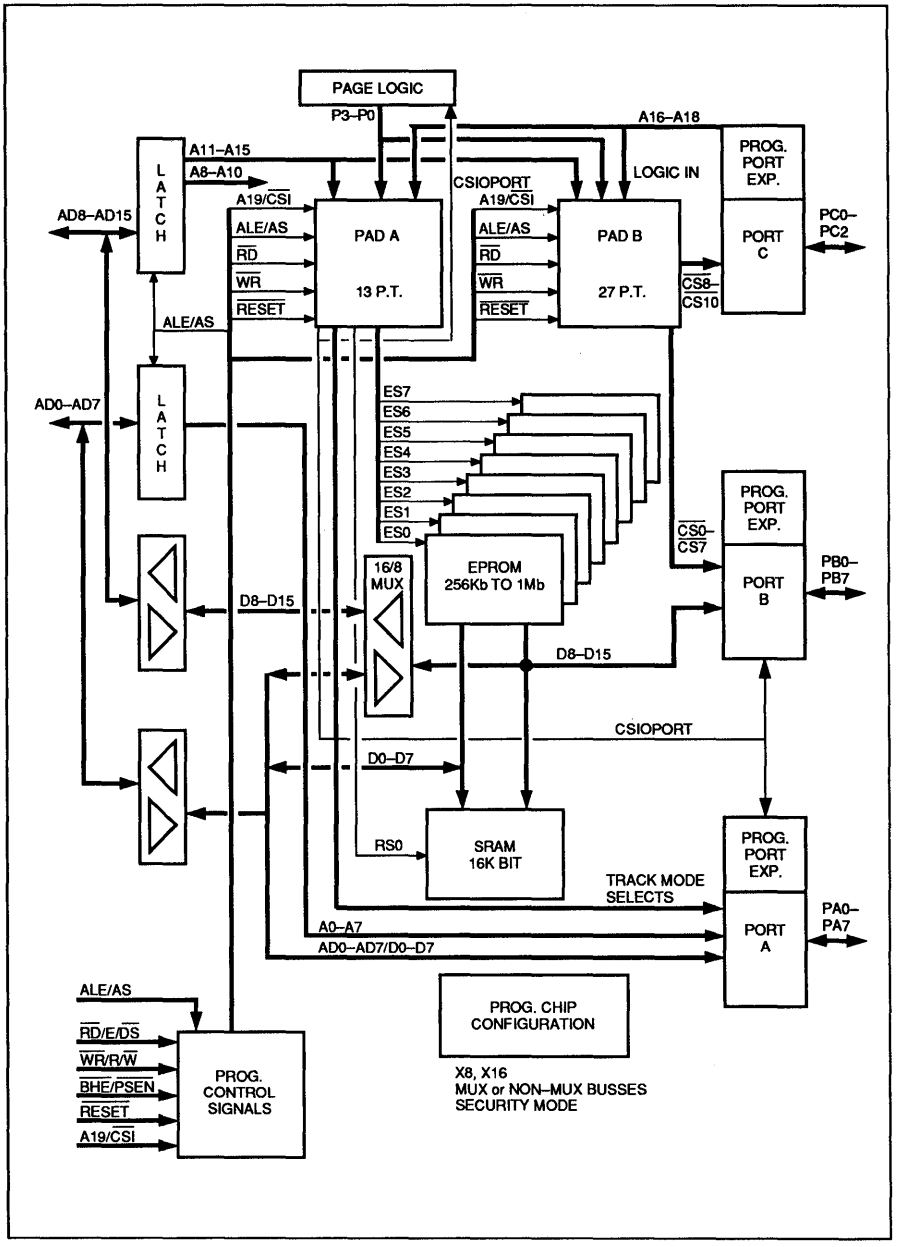


Table 1. PSD3XXL Pin Descriptions

Name	Type	Description
$\overline{BHE}/\overline{PSEN}$ (PSD30XL Devices) or	I	When the data bus width is 8 bits (CDATA = 0), this pin is $\overline{PSEN}$. In this mode, $\overline{PSEN}$ is the active low EPROM read pulse. The SRAM and I/O ports read signal is generated according to the description of the $\overline{WR}/V_{PP}$ or R/$\overline{W}$ and $\overline{RD}/E/\overline{DS}$ pins. If the host processor is a member of the 8031 family, $\overline{PSEN}$ must be connected to the corresponding host pin. In other 8-bit host processors that do not have a special EPROM-only read strobe, $\overline{PSEN}$ should be tied to V_{CC}. In this case, $\overline{RD}$ or E and R/$\overline{W}$ provide the read strobe for the SRAM, I/O ports, and EPROM. When the data bus width is configured as 16 (CDATA = 1), this pin is $\overline{BHE}$. When $\overline{BHE}$ is low, data bus bits D8–D15 are read from, or written into, the PSD3XXL, depending on the operation being read or write, respectively. In programming mode, this pin is pulsed between V_{PP} and 0.
$\overline{PSEN}$ (PSD31XL Devices Only)	I	The $\overline{PSEN}$ is the active low EPROM read pulse. The SRAM and I/O ports read signal is generated according to the description of the $\overline{WR}/V_{PP}$ or R/$\overline{W}$, and $\overline{RD}$/E pins. If the host processor is a member of the 8031 family, $\overline{PSEN}$ must be connected to the corresponding host pin. In other 8-bit host processors that do not have a special EPROM-only read strobe, $\overline{PSEN}$ should be tied to V_{CC}. In this case, $\overline{RD}$ or E and R/$\overline{W}$ provide the read strobe for the SRAM, I/O ports, and EPROM.
$\overline{WR}/V_{PP}$ or R/$\overline{W}$/V_{PP}	I	In the operating mode, this pin's function is $\overline{WR}$ (CRRWR = 0) or R/$\overline{W}$ (CRRWR = 1) when configured as R/$\overline{W}$. The following tables summarize the read and write operations (CRRWR = 1): CEDS = 0: R/$\overline{W}$ = X, E = 0, NOP; R/$\overline{W}$ = 0, E = 1, write; R/$\overline{W}$ = 1, E = 1, read CEDS = 1: R/$\overline{W}$ = X, $\overline{DS}$ = 1, NOP; R/$\overline{W}$ = 0, $\overline{DS}$ = 0, write; R/$\overline{W}$ = 1, $\overline{DS}$ = 0, read When configured as $\overline{WR}$, a write operation is executed during an active low pulse. When configured as R/$\overline{W}$, with R/$\overline{W}$ = 1 and E = 1, a read operation is executed; if R/$\overline{W}$ = 0 and E = 1, a write operation is executed. In programming mode, this pin must be tied to V_{PP} voltage.
$\overline{RD}$/E/$\overline{DS}$ (Note 2) or	I	The pin function depends on the CRRWR and CEDS configuration bits. If CRRWR = 0, RD is an active low read pulse. When CRRWR = 1, this pin and the R/$\overline{W}$ pin define the following cycle type: If CEDS = 0, E is an active high strobe. If CEDS = 1, DS is an active low strobe.
$\overline{RD}$/E (Note 3)	I	When configured as $\overline{RD}$ (CRRWR = 0), this pin provides an active low $\overline{RD}$ strobe. When configured as E (CRRWR = 1), this pin becomes an active high pulse, which, together with R/$\overline{W}$ defines the cycle type. Then, if R/$\overline{W}$ = 1 and E = 1, a read operation is executed. If R/$\overline{W}$ = 0 and E = 1, a write operation is executed.

Legend: The I/O column abbreviations are: I = input; I/O = input/output; P = power.

NOTE: 1. All the configuration bits mentioned in Table 1 appear in parentheses and are explained in the Configuration Register section.
2. PSD302L/312L/303L/313L only.
3. PSD301L/311L only.

Table 1. PSD3XXL Pin Descriptions (Cont.)

Name	Type	Description
$\overline{CSI}$/A19	I	This pin has two configurations. When it is $\overline{CSI}$ (CA19/$\overline{CSI}$ = 0) and the pin is asserted high, the device is deselected and powered down. (See Tables 12 and 13 for the chip state during power-down mode.) If the pin is asserted low, the chip is in normal operational mode. When it is configured as A19, (CA19/$\overline{CSI}$ = 1), this pin can be used as an additional input to the PAD. CADLOG3 = 1 defines the pin as an address; CADLOG3 = 0 defines it as a logic input. If it is an address, A19 can be latched with ALE (CADDHLT = 1) or be a transparent logic input (CADDHLT = 0). In this mode, there is no power-down capability.
$\overline{RESET}$	I	Reset is an active low pin. To reset the part, see Figure 10b. Also see Tables 10a, 10b and 11 for the chip state during and after reset.
ALE or AS	I	In the multiplexed modes, the ALE pin functions as an Address Latch Enable or as an Address strobe and can be configured as an active high or active low signal. The ALE or AS trailing edge latches lines AD15/A15–AD0/A0 and A16–A19 in 16-bit mode (AD7/A7–AD0/A0 and A16–A19 in 8-bit mode) and $\overline{BHE}$, depending on the PSD3XXL configuration. See Table 8. In the non-multiplexed modes, it can be used as a general-purpose logic input to the PAD.
PA7 PA6 PA5 PA4 PA3 PA2 PA1 PA0	I/O	PA7–PA0 is an 8-bit port that can be configured to track AD7/A7–AD0/A0 from the input (CPAF2 = 1). Otherwise (CPAF2 = 0), each bit can be configured separately as an I/O or lower-order latched address line. When configured as an I/O (CPAF1 = 0), the direction of the pin is defined by its direction bit, which resides in the direction register. If a pin is an I/O output, its data bit (which resides in the data register) comes out. When it is configured as a low-order address line (CPAF1 =1), A7–A0 can be made the corresponding output through this port (e.g., PA6 can be configured to be the A6 address line). Each port bit can be a CMOS output (CPACOD = 0) or an open drain output (CPACOD = 1). When the chip is in non-multiplexed mode (CADDRAT = 0), the port becomes the data bus lines (D0–D7). See Figure 4.
PB7 PB6 PB5 PB4 PB3 PB2 PB1 PB0	I/O	PB7–PB0 is an 8-bit port for which each bit can be configured as an I/O (CPBF = 1) or chip-select output (CPBF = 0). Each port bit can be a CMOS output (CPBCOD = 0) or an open drain output (CPBCOD = 1). When configured as an I/O, the direction of the pin is defined by its direction bit, which resides in the direction register. If a pin is an I/O output, its data (which resides in the data register) comes out. When configured as a chip-select output, $\overline{CS0}$–$\overline{CS3}$ are a function of up to four product terms of the inputs to the PAD B; $\overline{CS4}$,–$\overline{CS7}$ then are each a function of up to two product terms. On the PSD301L/302L/303L, when the chip is in non-multiplexed mode (CADDRAT = 0) and the data bus width is 16 (CDATA = 1), the port becomes the data bus (D8–D15). See Figure 6.

Table 1. PSD3XXL Pin Descriptions (Cont.)

Name	Type	Description
PC0 PC1 PC2	I/O	This is a 3-bit port for which each bit is configurable as a PAD A and B input or output. When configured as an input (CPCF = 0), a bit individually becomes an address (CADLOG = 1) or a logic input (CADLOG = 0). The addresses can be latched with ALE (CADDHLT = 1) or be transparent inputs to the PADs (CADDHLT = 0). When a pin is configured as an output (CPCF = 1), it is a function of one product term of all PAD inputs. See Figure 7.
AD0/A0 AD1/A1 AD2/A2 AD3/A3 AD4/A4 AD5/A5 AD6/A6 AD7/A7	I/O	In multiplexed mode, these pins are the multiplexed low-order address/data byte. After ALE latches the addresses, these pins input or output data, depending on the settings of the $\overline{RD}$/E ($\overline{RD}$/E/$\overline{DS}$ on the PSD302L/303L), $\overline{WR}$/V_{PP} or R/$\overline{W}$, and $\overline{BHE}$/$\overline{PSEN}$ pins. In non-multiplexed mode, these pins are the low-order address input.
AD8/A8 AD9/A9 AD10/A10 AD11/A11 AD12/A12 AD13/A13 AD14/A14 AD15/A15	I/O	In 16-bit multiplexed mode, these pins are the multiplexed high-order address/data byte. After ALE latches the addresses, these pins input or output data, depending on the settings of the $\overline{RD}$/E or $\overline{RD}$/E/$\overline{DS}$, $\overline{WR}$/V_{PP} or R/$\overline{W}$, and $\overline{BHE}$/$\overline{PSEN}$ pins. In all other modes, these pins are the high-order address input.
GND	P	V_{SS} (ground) pin.
V_{CC}	P	Supply voltage input.

Operating Modes

The PSD3XXL's four operating modes enable it to interface directly to 8- and 16-bit microcontrollers with multiplexed and non-multiplexed address/data buses. These operating modes are:

- ❑ Multiplexed 8-bit address/data bus
- ❑ Multiplexed 16-bit address/data bus (PSD30XL)
- ❑ Non-multiplexed address/data, 8-bit data bus
- ❑ Non-multiplexed 16-bit address/ data bus (PSD30XL)

Multiplexed 8-bit Address/Data Bus

This mode is used to interface to microcontrollers with an 8-bit data bus and a 16-bit or larger address bus. The address/data bus (AD0/A0–AD7/A7) is bi-directional and permits the latching of the address when the ALE signal is active. On the same pins, the data is read from or written to the device; this depends on the state of the $\overline{RD}$/E or $\overline{RD}$/E/$\overline{DS}$ pin, $\overline{BHE}$/$\overline{PSEN}$ or $\overline{PSEN}$ pin and $\overline{WR}$/V_{PP} or R/$\overline{W}$ pins. The high-order address/data bus (AD8/A8–AD15/A15) contains the high-order address bus byte. Ports A and B can be configured as in Table 2.

Multiplexed 16-bit Address/Data Bus

This mode is used to interface to microcontrollers with a 16-bit data bus and a 16-bit or larger address bus. The low-order address/data bus (AD0/A0–AD7/A7) is bi-directional and permits the latching of the address when the ALE signal is active. On the same pins, the data is read from or written to the device; this depends on the state of the $\overline{RD}$/E/$\overline{DS}$, $\overline{BHE}$/$\overline{PSEN}$, and $\overline{WR}$/V_{PP} or R/$\overline{W}$ pins. The high-order address/data bus (AD8/A8–AD15/A15) is bi-directional and permits latching of the high-order address when the ALE signal is active on the same pins. The high-order data bus is read from or written to the device, depending on the state of the $\overline{RD}$/E/$\overline{DS}$, $\overline{BHE}$/$\overline{PSEN}$, and $\overline{WR}$/V_{PP} or R/$\overline{W}$ pins. Ports A and B can be configured as in Table 2.

Non-Multiplexed Address/Data, 8-bit Data Bus

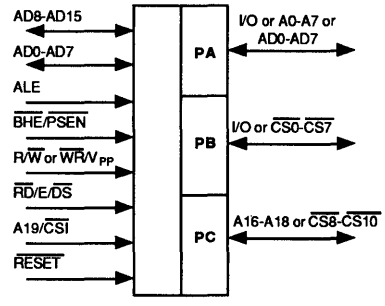
This mode is used to interface to non-multiplexed 8-bit microcontrollers with an 8-bit data bus and a 16-bit or larger address bus. The low-order address/data bus (AD0/A0–AD7/A7) is the low-order address input bus. The high-order address/data bus (AD8/A8–AD15/A15) (A8–A15 on the PSD31XL) is the high-order address bus byte. Port A is the low-order data bus. Port B can be configured as shown in Table 2.

Non-Multiplexed Address/Data, 16-bit Data Bus

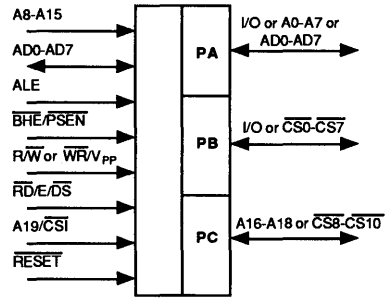
This mode is used to interface to non-multiplexed 16-bit microcontrollers with a 16-bit data bus and a 16-bit or larger address bus. The low-order address/data bus (AD0/A0–AD7/A7) is the low-order address input bus. The high-order address/data bus (AD8/A8–AD15/A15) is the high-order address bus byte. Port A is the low-order data bus. Port B is the high-order data bus.

Table 2 summarizes the effect of the different operating modes on ports A, B, and the address/data pins. The configuration of Port C is independent of the four operating modes.

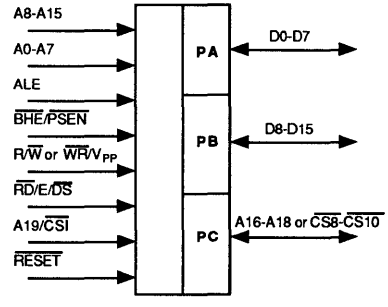
Figure 2a. PSD3XXL Port Configurations (x8/x16)



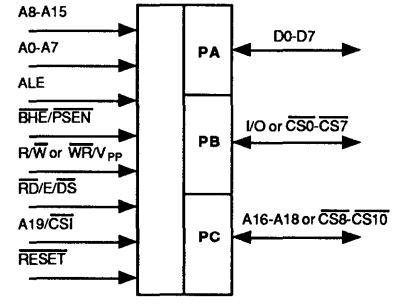
1. Configured for multiplexed 16-bit address/data bus.



2. Configured for multiplexed 8-bit address/data bus.

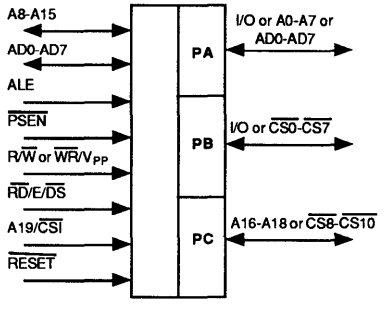


3. Configured for non-multiplexed 16-bit address/data bus.

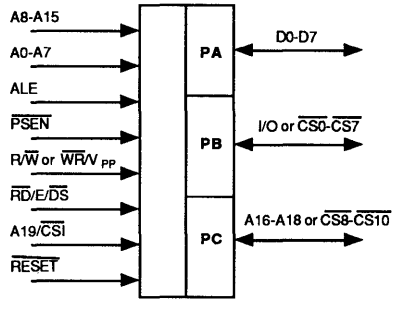


4. Configured for non-multiplexed address/data, 8-bit bus.

Figure 2b. PSD3XXL Port Configurations (x8 Only)



1. Configured for multiplexed 8-bit address/data bus.



2. Configured for non-multiplexed address/data, 8-bit bus.

Legend: AD8–AD15 = Addresses A8–A15 multiplexed with data lines D8–D15.
AD0–AD7 = Addresses A0–A7 multiplexed with data lines D0–D7.

Table 2. PSD30XL Bus and Port Configuration Options

	Multiplexed Address/Data	Non-Multiplexed Address/Data
8-bit Data Bus		
Port A	I/O or low-order address lines or Low-order multiplexed address/data byte	D0–D7 data bus byte
Port B	I/O or $\overline{CS0}$–$\overline{CS7}$	I/O and/or $\overline{CS0}$–$\overline{CS7}$
AD0/A0–AD7/A7	Low-order multiplexed address/data byte	Low-order address bus byte
AD8/A8–AD15/A15	High-order multiplexed address data byte	High-order address bus byte
16-bit Data Bus		
Port A	I/O or low-order address lines or Low-order multiplexed address/data byte	Low-order data bus byte
Port B	I/O or $\overline{CS0}$–$\overline{CS7}$	High-order data bus byte
AD0/A0–AD7/A7	Low-order multiplexed address/data byte	Low-order address bus byte
AD8/A8–AD15/A15	High-order multiplexed address/data byte	High-order address bus byte

Table 2a. PSD31XL Bus and Port Configuration Options

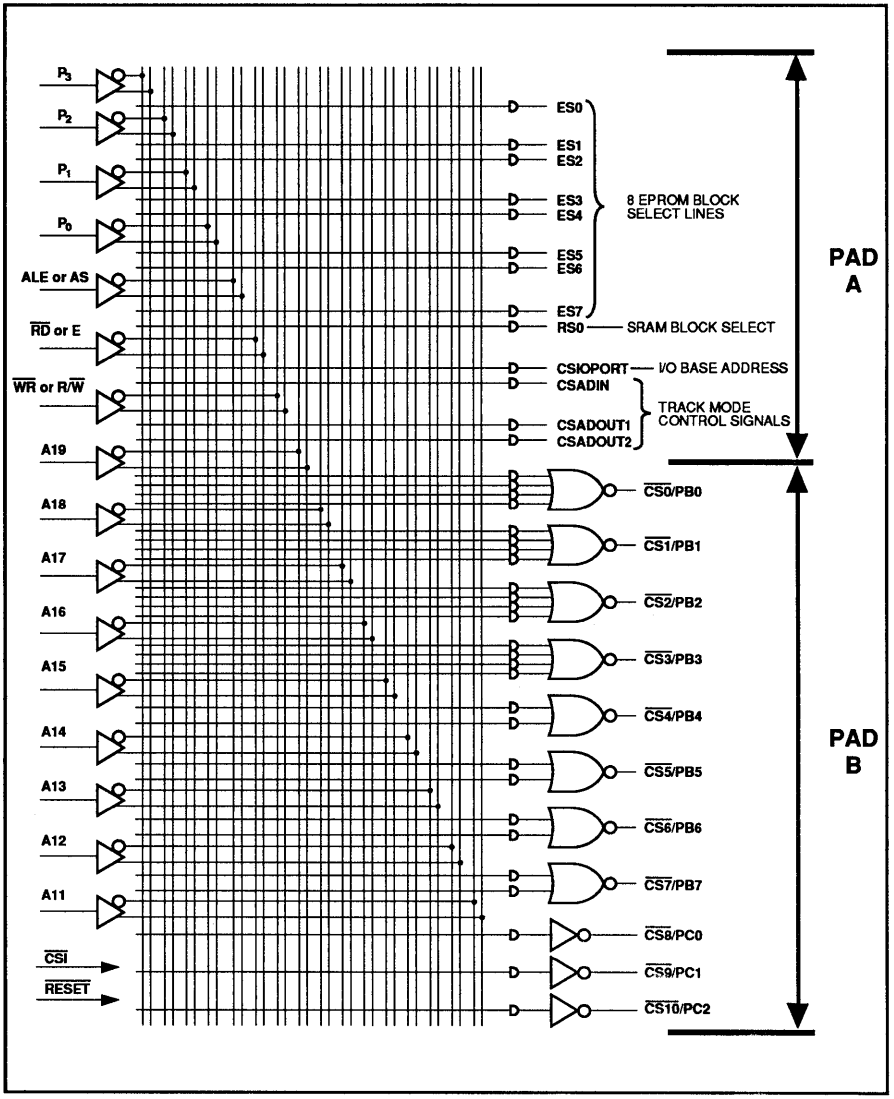
	Multiplexed Address/Data	Non-Multiplexed Address/Data
8-bit Data Bus		
Port A	I/O or low-order address lines or Low-order multiplexed address/data byte	D0–D7 data bus byte
Port B	I/O or $\overline{CS0}$–$\overline{CS7}$	I/O and/or $\overline{CS0}$–$\overline{CS7}$
AD0/A0–AD7/A7	Low-order multiplexed address/data byte	Low-order address bus byte
A8–A15	High-order address bus byte	High-order address bus byte

Programmable Address Decoder (PAD)

The PSD3XXL consists of two programmable arrays referred to as PAD A and PAD B (Figure 3). PAD A is used to generate chip select signals derived from the input address to the internal EPROM blocks, SRAM, I/O ports, and Track Mode signals. All its I/O functions are listed in Table 3 and shown in Figure 3. PAD B outputs to Ports B and C for off-chip usage.

PAD B can also be used to extend the decoding to select external devices or as a random logic replacement. The input bus to both PAD A and PAD B is the same. Using MAPLE software, each programmable bit in the PAD's array can have one of three logic states of 0, 1, and don't care (X). In a user's logic design, both PADs can share the same inputs using the X for input signals that are not supposed to affect other functions. The PADs use reprogrammable CMOS EPROM technology and can be programmed and erased by the user.

Figure 3. PAD Description



NOTES: 4. $\overline{CSI}$ is a power-down signal. When high, the PAD is in stand-by mode and all its outputs become non-active. See Tables 12 and 13.

5. $\overline{RESET}$ deselects all PAD output signals. See Tables 10 and 11.

6. A18, A17, and A16 are internally multiplexed with $\overline{CS10}$, $\overline{CS9}$, and $\overline{CS8}$, respectively. Either A18 or $\overline{CS10}$, A17 or $\overline{CS9}$, and A16 or $\overline{CS8}$ can be routed to the external pins of Port C. Port C can be configured as either input or output.

7. P_0–P_3 are not included on PSD3X1L devices.

Table 3. PSD3XXL PAD A and PAD B Functions

	Function
PAD A and PAD B Inputs	
A19/$\overline{CSI}$	In $\overline{CSI}$ mode (when high), PAD deselects all of its outputs and enters a power-down mode (see Tables 12 and 13). In A19 mode, it is another input to the PAD.
A16–A18	These are general purpose inputs from Port C. See Figure 3, Note 4.
A11–A15	These are address inputs.
P0–P3	These are page number inputs (for the PSD302L/312L/303L/313L only).
$\overline{RD}$ or E	This is the read pulse or enable strobe input.
$\overline{WR}$ or R/$\overline{W}$	This is the write pulse or R/$\overline{W}$ select signal.
ALE	This is the ALE input to the chip.
$\overline{RESET}$	This deselects all outputs from the PAD; it can not be used in product term equations. See Tables 10 and 11.
PAD A Outputs	
ES0–ES7	These are internal chip-selects to the 8 EPROM banks. Each bank can be located on any boundary that is a function of one product term of the PAD address inputs.
RS0	This is an internal chip-select to the SRAM. Its base address location is a function of one term of the PAD address inputs.
CSIOPORT	This internal chip-select selects the I/O ports. It can be placed on any boundary that is a function of one product term of the PAD inputs. See Tables 6 and 7.
CSADIN	This internal chip-select, when Port A is configured as a low-order address/data bus in the track mode (CPAF2 = 1), controls the input direction of Port A. CSADIN is gated externally to the PAD by the internal read signal. When CSADIN and a read operation are active, data presented on Port A flows out of AD0/A0–AD7/A7. This chip-select can be placed on any boundary that is a function of one product term of the PAD inputs. See Figure 5.
CSADOUT1	This internal chip-select, when Port A is configured as a low-order address/data bus in track mode (CPAF2 = 1), controls the output direction of Port A. CSADOUT1 is gated externally to the PAD by the ALE signal. When CSADOUT1 and the ALE signal are active, the address presented on AD0/A0–AD7/A7 flows out of Port A. This chip-select can be placed on any boundary that is a function of one product term of the PAD inputs. See Figure 5.
CSADOUT2	This internal chip-select, when Port A is configured as a low-order address/data bus in the track mode (CPAF2 = 1), controls the output direction of Port A. CSADOUT2 must include the write-cycle control signals as part of its product term. When CSADOUT2 is active, the data presented on AD0/A0–AD7/A7 flows out of Port A. This chip-select can be placed on any boundary that is a function of one product term of the PAD inputs. See Figure 5.
PAD B Outputs	
$\overline{CS0}$–$\overline{CS3}$	These chip-select outputs can be routed through Port B. Each of them is a function of up to four product terms of the PAD inputs.
$\overline{CS4}$–$\overline{CS7}$	These chip-select outputs can be routed through Port B. Each of them is a function of up to two product terms of the PAD inputs.
$\overline{CS8}$–$\overline{CS10}$	These chip-select outputs can be routed through Port C. See Figure 3, Note 4. Each of them is a function of one product term of the PAD inputs.

Configuration Bits

The configuration bits shown in Table 4 are non-volatile cells that let the user set the device, I/O, and control functions to the proper operational mode. Table 5 lists all configuration bits. The configuration bits are programmed and verified during the programming phase. In operational mode, they are not accessible. To simplify implementing a specific mode, use the PSD3XXL MAPLE software to set the bits.

Table 4. PSD3XXL Non-Volatile Configuration Bits

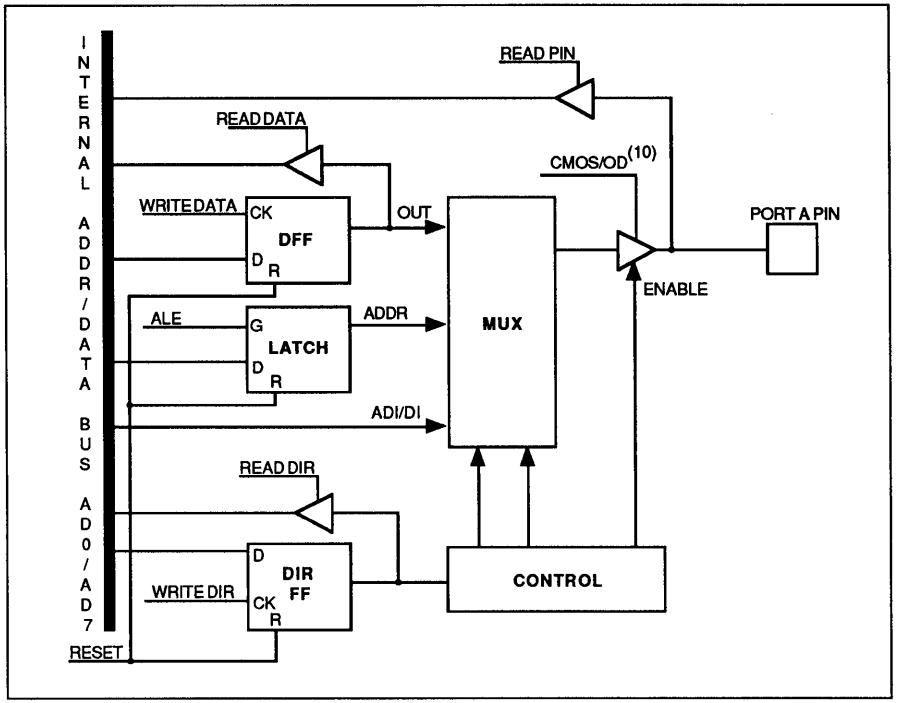
Use This Bit	To
CDATA	Set the data bus width to 8 or 16 bits (PSD30XL only).
CADDRDAT	Set the address/data buses to multiplexed or non-multiplexed mode.
CEDS	Determine the polarity and functionality of read and write. (Note 9)
CA19/$\overline{CSI}$	Set A19/$\overline{CSI}$ to $\overline{CSI}$ (power-down) or A19 input.
CALE	Set the ALE polarity.
CPAF2	Set Port A either to track the low-order byte of the address/data multiplexed bus or to select the I/O or address option.
CSECURITY	Set the security on or off (a secured part can not be duplicated).
$\overline{COMB}$/SEP	Set $\overline{PSEN}$ and $\overline{RD}$ for combined or separate address spaces (see Figures 9 and 10).
CPAF1 (8 Bits)	Configure each pin of Port A in multiplexed mode to be an I/O or address out.
CPACOD (8 Bits)	Configure each pin of Port A as an open drain or active CMOS pull-up output.
CPBF (8 Bits)	Configure each pin of Port B as an I/O or a chip-select output'
CPBCOD (8 Bits)	Configure each pin of Port B as an open drain or active CMOS pull-up output.
CPCF (3 Bits)	Configure each pin of Port C as an address input or a chip-select output.
CADDHLT	Configure pins A16 – A19 to go through a latch or to have their latch transparent.
CADLOG (4 Bits)	Configure A16 – A19 individually as logic or address inputs. (Note 9)
CATD	Configure pins A16–A19 as PAD logic inputs or high-order address inputs (Note 8).
CLOT	Determine in non-multiplexed mode if address inputs are transparent or latched (Note 9).
CRRWR	Set the $\overline{RD}$/E and $\overline{WR}$/V_{PP} or R/$\overline{W}$ pins to $\overline{RD}$ and $\overline{WR}$ pulse, or to E strobe and R/$\overline{W}$ status (Note 8).
CRRWR	Configure the polarity and control methods of read and write cycles. (Note 9)
CMISER	Controls the lower-power mode.

NOTES: 8. PSD31XL only.
9. PSD302L/312L/303L/313L only.

Port Functions

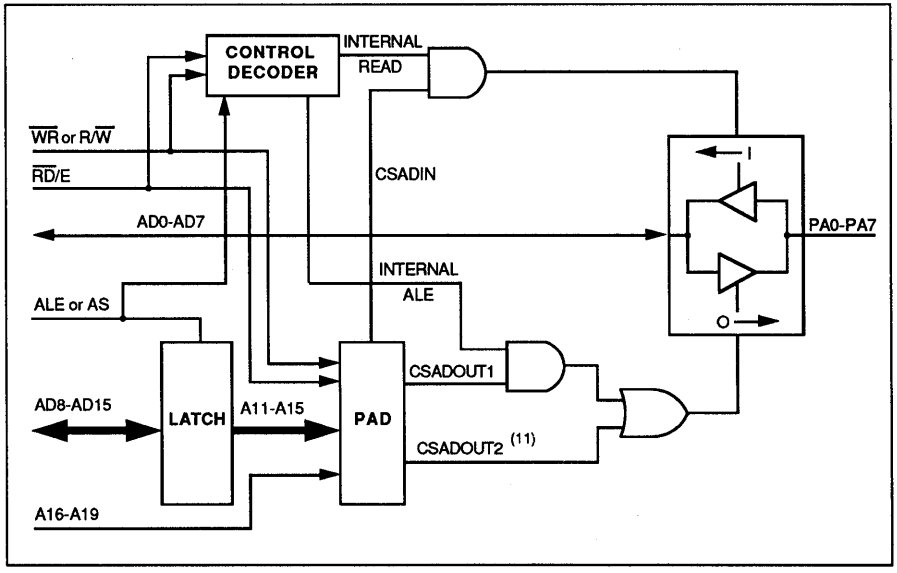
The PSD3XXL has three I/O ports (Ports A, B, and C) that are configurable at the bit level. This permits great flexibility and a high degree of customization for specific applications. The following is a description of each port. Figure 4 shows the pin structure of Port A.

Figure 4. Port A Pin Structure



NOTE: 10. CMOS/OD determines whether the output is open drain or CMOS.

Figure 5. Port A Track Mode



NOTE: 11. The expression for CSADOUT2 must include the following write operation cycle signals:
For CRRWR = 0, CSADOUT2 must include $\overline{WR}$ = 0.
For CRRWR = 1, CSADOUT2 must include E = 1 and R/$\overline{W}$ = 0.

Table 5. PSD3XXL Configuration Bits[12,13]

Configuration Bits	No. of Bits	Function
CDATA (Note 14)	1	8-bit or 16-bit Data Bus Width CDATA = 0 eight bits CDATA = 1 sixteen bits
CADDRDAT	1	ADDRESS/DATA Multiplexed (separate buses) CADDRDAT = 0, non-multiplexed CADDRDAT = 1, multiplexed
CA19/$\overline{CSI}$	1	A19 or $\overline{CSI}$ CA19/$\overline{CSI}$ = 0, enable power-down CA19/$\overline{CSI}$ = 1, enable A19 input to PAD
CALE	1	Active HIGH or Active LOW CALE = 0, Active high CALE = 1, Active low
$\overline{COMB}$/SEP	1	Combined or Separate Address Space for SRAM and EPROM 0 = Combined, 1 = Separate
CPAF1	8	Port A I/Os or A0–A7 CPAF1 = 0, Port A pin = I/O CPAF1 = 1, Port A pin = A0 – A7
CPAF2	1	Port A AD0–AD7 (address/data multiplexed bus) CPAF2 = 0, address or I/O on Port A (according to CPAF1) CPAF2 = 1, address/data multiplexed on Port A (track mode)
CATD (Note 16)	1	A16–A19 address or logic inputs CATD = 0, logic inputs CATD = 1, address inputs
CADDHLT	1	A16–A19 Transparent or Latched CADDHLT = 0, Address latch transparent CADDHLT = 1, Address latched (ALE dependent)
CSECURITY	1	SECURITY On/Off CSECURITY = 0, off CSECURITY = 1, on
CLOT (Note 15)	1	A0–A15 Address Inputs are transparent or ALE-dependent in non-multiplexed modes CLOT = 0, transparent CLOT = 1, ALE-dependent
CRRWR CEDS (Note 15)	2	Determine the polarity and control methods of read and write cycles. CEDS CRRWR 0 0 $\overline{RD}$ and $\overline{WR}$ active low pulses 0 1 R/$\overline{W}$ status and high E pulse 1 1 R/$\overline{W}$ status and low $\overline{DS}$ pulse
CRRWR (Note 16)	1	CRRWR = 0, $\overline{RD}$ and $\overline{WR}$ active low strobes CRRWR = 1, R/$\overline{W}$ status and E active high pulse
CPACOD	8	Port A CMOS or Open Drain Output CPACOD = 0, CMOS output CPACOD = 1, open-drain output
CPBF	8	Port B is I/O or $\overline{CS0}$– $\overline{CS7}$ CPBF = 0, Port B pin is $\overline{CS0}$ – $\overline{CS7}$ CPBF = 1, Port B pin is I/O

Table 5. PSD3XXL Configuration Bits (Cont.)

Configuration Bits	No. of Bits	Function
CPBCOD	8	Port B CMOS or Open Drain CPBCOD = 0, CMOS output CPBCOD = 1, open-drain output
CPCF	3	Port C A16–A18 or $\overline{CS8}$–$\overline{CS10}$ CPCF = 0, Port C pin is A16–A18 CPCF = 1, Port C pin is $\overline{CS8}$–$\overline{CS10}$
CADLOG (Note 15)	4	Port C: A16–A19 Address or Logic Input CADLOG = 0, Port C pin or A19/$\overline{CSI}$ is logic input CADLOG = 1, Port C pin or A19/$\overline{CSI}$ is address input
CMISER	1	Default: CMISER = 0 CMISER = 1, lower-power mode

NOTES: 12. WSI's Maple software will guide the user to the proper configuration choice.
13. In an unprogrammed or erased part, all configuration bits are 0.
14. PSD30XL only.
15. PSD3X2L/3X3L only.
16. PSD3X1L only.

Port Functions (Cont.)

Port A in Multiplexed Address/Data Mode

The default configuration of Port A is I/O. In this mode, every pin can be set as an input or output by writing into the respective pin's direction flip flop (DIR FF, in Figure 4). As an output, the pin level can be controlled by writing into the respective pin's data flip flop (DFF, in Figure 4). When DIR FF = 1, the pin is configured as an output. When DIR FF = 0, the pin is configured as an input. The controller can read the DIR FF bits by accessing the READ DIR register; it can read the DFF bits by accessing the READ DATA register. Port A pin levels can be read by accessing the READ PIN register. Individual pins can be configured as CMOS or open drain outputs. Open drain pins require external pull-up resistors. For addressing information, refer to Tables 6 and 7.

Alternatively, each bit of Port A can be configured as a low-order latched address bus bit. The address is provided by the port address latch, which latches the address on the trailing edge of ALE. PA0–PA7 can become A0–A7, respectively. This feature enables the user generate low-order address bits to access external peripherals or memory that require several low-order address lines.

Another mode of Port A (CPAF2 = 1) sets the entire port to track the inputs AD0/A0–AD7/A7, depending on specific address ranges defined by the PAD's CSADIN, CSADOUT1, and CSADOUT2 signals. This feature lets the user interface the microcontroller to shared external resources without requiring external buffers and decoders. In this mode, the port is effectively a bi-directional buffer. The direction is controlled by using the input signals ALE, $\overline{RD}$/E or $\overline{RD}$/E/$\overline{DS}$, $\overline{WR}$/V_{PP} or R/$\overline{W}$, and the internal PAD outputs $\overline{CS}$ADOUT1, $\overline{CS}$ADOUT2 and CSADIN (see Figure 5). When CSADOUT1 and ALE are true, the address on the input AD0/A0–AD7/A7 pins is output through Port A. (Carefully check the generation of CSADOUT1, and ensure that it is stable during the ALE pulse. When CSADOUT2 is active, a write operation is performed (see note to Figure 5). The data on the input AD0/A0–AD7/A7 pins flows out through Port A. When CSADIN and a read operation is performed (depending on the mode of the $\overline{RD}$/E or $\overline{RD}$/E/$\overline{DS}$, and $\overline{WR}$/V_{PP} or R/$\overline{W}$ pins), the data on Port A flows out through the AD0/A0–AD7/A7 pins. In this operational mode, Port A is tri-stated when none of the above-mentioned three conditions exist.

Port Functions (Cont.)

Port A in Non-Multiplexed Address/Data Mode

In this mode, Port A becomes the low order data bus byte of the chip. When reading an internal location, data is presented on Port A pins. When writing to an internal location, data present on Port A pins is written to that location.

Port B in Multiplexed Address/Data and in 8-Bit Non-Multiplexed Modes

The default configuration of Port B is I/O. In this mode, every pin can be set as an input or output by writing into the respective pin's direction flip flop (DIR FF, in Figure 6). As an output, the pin level can be controlled by writing into the respective pin's data flip flop (DFF, in Figure 6). When DIR FF = 1, the pin is configured as an output. When DIR FF = 0, the pin is configured as an input. The controller can read the DIR FF bits by accessing the READ DIR register; it can read the DFF bits by accessing the READ DATA register. Port B pin levels can be read by accessing the READ PIN register. Individual pins can be configured as CMOS or open drain outputs. Open drain pins require external pull-up resistors. For addressing information, refer to Tables 6 and 7.

Alternately, each bit of Port B can be configured to provide a chip-select output signal from PAD B. PB0–PB7 can provide $\overline{CS0}$–$\overline{CS7}$, respectively. Each of the signals $\overline{CS0}$–$\overline{CS3}$ is comprised of four product terms.Thus, up to four ANDed expressions can be ORed while deriving any of these signals. Each of the signals $\overline{CS4}$–$\overline{CS7}$ is comprised of two product terms. Thus, up to two ANDed expressions can be ORed while deriving any of these signals.

Port B in 16-Bit Non-Multiplexed Address/Data Mode (PSD30XL)

In this mode, Port B becomes the high-order data bus byte of the chip. When reading an internal high-order data bus byte location, the data is presented on Port B pins. When writing to an internal high-order data bus byte location, data present on Port B is written to that location. See Table 9.

Accessing the I/O Port Registers

Tables 6 and 7 show the offset values with the respect to the base address defined by the CSIOPORT. They let the user access the corresponding registers.

Port C in All Modes

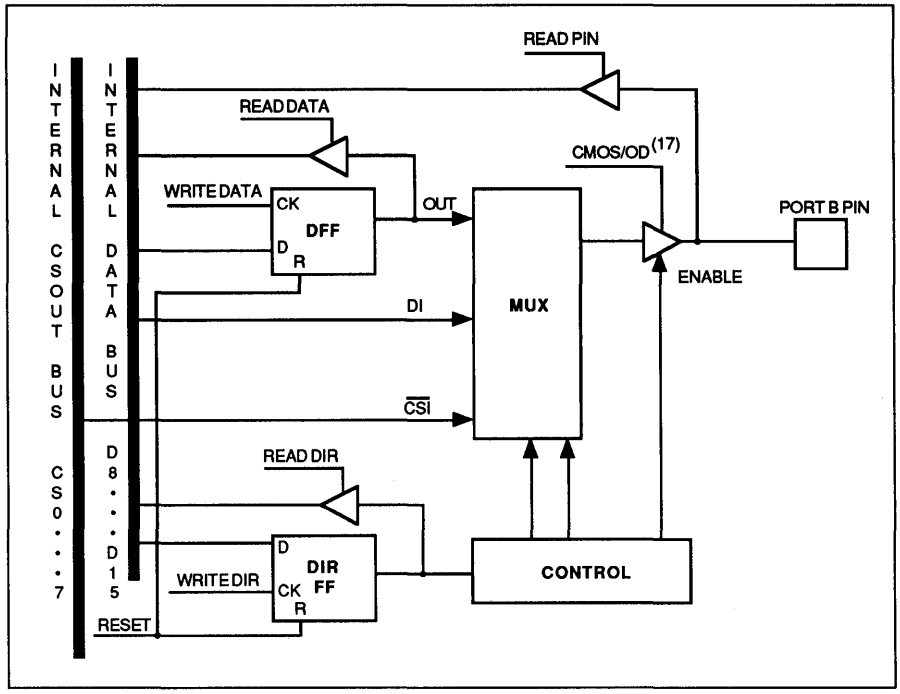
Each pin of Port C (shown in Figure 7) can be configured as an input to PAD A and PAD B or output from PAD B. As inputs, the pins are named A16–A18. Although the pins are given names of the high-order address bus, they can be used for any other address lines or logic inputs to PAD A and PAD B. For example, A8–A10 can also be connected to those pins, improving the boundaries of $\overline{CS0}$–$\overline{CS7}$ resolution to 256 bytes. As inputs, they can be individually configured to be logic or address inputs. A logic input uses the PAD only for Boolean equations that are implemented in any or all of the $\overline{CS0}$–$\overline{CS10}$ PAD B outputs. Port C addresses can be programmed to latch the inputs by the trailing edge ALE or to be transparent.

Alternately, PC0–PC2 can become $\overline{CS8}$–$\overline{CS10}$ outputs, respectively, providing the user with more external chip-select PAD outputs. Each of the signals $\overline{CS8}$–$\overline{CS10}$ is comprised of one product term.

ALE/AS and AD0/A0–AD15/A15 in Non-Multiplexed Modes

In non-multiplexed modes, AD0/A0–AD15/A15 are address inputs only and can become transparent (CLOT = 0) or ALE dependent (CLOT = 1). In transparent mode, the ALE/AS pin can be used as an additional logic input to the PADs. The non-multiplexed ALE dependent mode is useful in applications for which the host processor has a multiplex address/data bus and AD0/A0–AD7/A7 are not multiplexed with A0–A7 but rather are multiplexed with other address lines. In these applications, Port A serves as a data bus and each of its pins can be directly connected to the corresponding host's multiplexed pin, where that data bit is expected.
(See Table 8.)

Figure 6. Port B Pin Structure



NOTE: 17. CMOS/OD determines whether the output is open drain or CMOS.

Table 6. I/O Port Addresses in an 8-bit Data Bus Mode

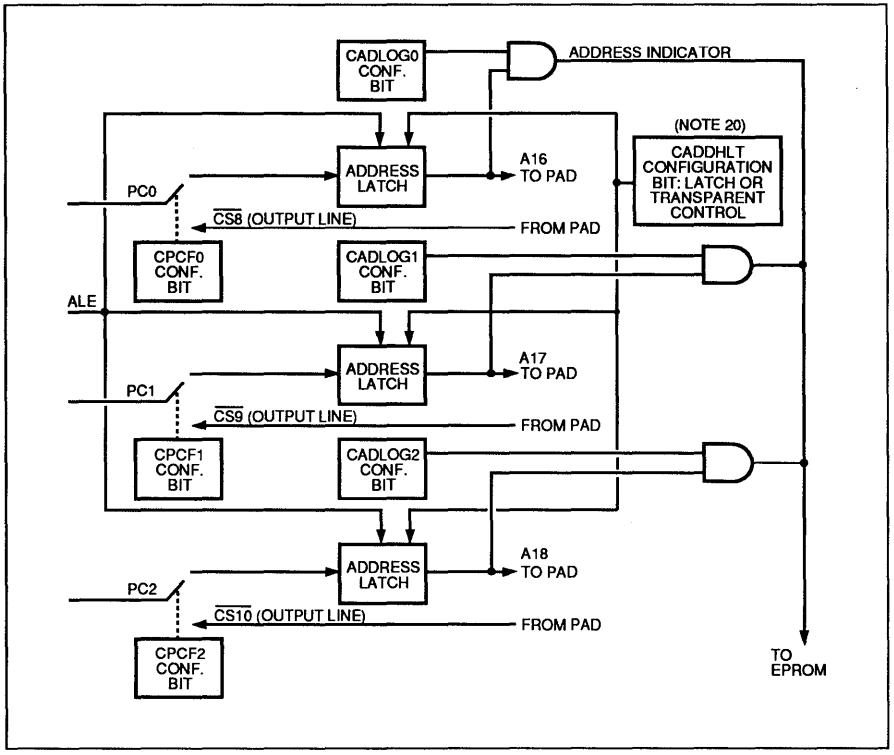
Register Name	Byte Size Access of the I/O Port Registers Offset from the CSIOPORT
Pin Register of Port A	+ 2 (accessible during read operation only)
Direction Register of Port A	+ 4
Data Register of Port A	+ 6
Pin Register of Port B	+ 3 (accessible during read operation only)
Direction Register of Port B	+ 5
Data Register of Port B	+ 7
Page Register	+18

Table 7. I/O Port Addresses in a 16-bit Data Bus Mode[18,19] (PSD30XL)

Register Name	Word Size Access of the I/O Port Registers Offset from the CSIOPORT
Pin Register of Ports B and A	+ 2 (accessible during read operation only)
Direction Register of Ports B and A	+ 4
Data Register of Ports B and A	+ 6

NOTES: 18. When the data bus width is 16, Port B registers can only be accessed if the $\overline{BHE}$ signal is low.
19. I/O Ports A and B are still byte-addressable, as shown in Table 6. For I/O Port B register access, $\overline{BHE}$ must be low.

Figure 7. Port C Structure



NOTES: 20. The CADDHLT configuration bit determines if A18–A16 are transparent via the latch, or if they must be latched by the trailing edge of the ALE strobe.

21. PSD3X2L/3X3L: Individual pins can be configured independently as address or logic inputs (CADLOG, bits 0–2).
PSD3X1L: All Port C pins are either address or logic inputs (CATD).

Port Functions (Cont.)

ALE/AS and AD0/A0–AD15/A15 in Non-Multiplexed Modes (PSD302L/303L)

In non-multiplexed modes, AD0/A0–AD15/A15 are address inputs only and can become transparent (CLOT = 0) or ALE dependent (CLOT = 1). In transparent mode, the ALE/AS pin can be used as an additional logic input to the PADs. The non-multiplexed ALE dependent mode is useful in applications for which the host processor has a multiplex address/data bus and AD0/A0–AD7/A7 are not multiplexed with A0–A7 but rather are multiplexed with other address lines. In these applications, Port A serves as a data bus and each of its pins can be directly connected to the corresponding host's multiplexed pin, where that data bit is expected. (See Table 8.)

ALE/AS and AD0/A0–AD7/A7 in Non-Multiplexed Modes (PSD31XL)

In non-multiplexed modes, A0–A15 are address inputs only and can become transparent (CLOT = 0) or ALE dependent (CLOT = 1). In transparent mode, the ALE/AS pin can be used as an additional logic input to the PADs. The non-multiplexed ALE dependent mode is useful in applications for which the host processor has a multiplex address/data bus and AD0/A0–AD7/A7 are not multiplexed with A0–A7 but rather are multiplexed with other address lines. In these applications, Port A serves as a data bus and each of its pins can be directly connected to the corresponding host's multiplexed pin, where that data bit is expected. (See Table 8.)

A16–A19 Inputs

If one or more of the pins PC0, PC1 PC2 and $\overline{CSI}$/A19 are configured as inputs, the configuration bits CADDHLT and CATD define their functionality inside the part. CADDHLT determines if these inputs are to be latched by the trailing edge of the ALE or AS signal (CADDHLT = 1), or enabled into the PSD3XX at all times (CADDHLT = 0, transparent mode). CATD determines whether these lines are high-order address lines, that take part in the derivation of memory and I/O select signals inside the chip (CATD = 1), or logic input lines that have no impact on memory or I/O selections (CATD = 0). Logic input lines typically participate in the Boolean expressions implemented in the PAD.

EPROM

The EPROM has 8 banks of memory. Each bank can be placed in any address location by programming the PAD. Bank0–Bank7 is selected by PAD outputs ES0–ES7, respectively.

Device	EPROM Size	EPROM Architecture		EPROM Bank Architecture (8 ea)	
		x8	x16	x8	x16
PSD301L	256Kb	32K x 8	16K x 16	4K x 8	2K x 16
PSD311L	256Kb	32K x 8	–	4K x 8	–
PSD302L	512Kb	64K x 8	32K x 16	8K x 8	4K x 16
PSD312L	512Kb	64K x 8	–	8K x 8	–
PSD303L	1Mb	128K x 8	64K x 16	16K x 8	8K x 16
PSD313L	1Mb	128K x 8	–	16K x 8	–

SRAM

Each PSD3XXL device has 16K bits of SRAM. Depending on the configuration of the data bus, the SRAM organization can be 2K x 8 (8-bit data bus) or 1K x 16 (16-bit data bus). The SRAM is selected by the RS0 output of the PAD.

Memory Paging (PSD3X2L/3X3L)

The page register consists of four flip-flops, which can be read from, or written to, through the I/O address space (CSIOPORT). The page register is connected to the D3–D0 lines. The Page Register address is CSIOPORT + 18H. The page register outputs are P3–P0, which are fed into the PAD. This enables the host microcontroller to enlarge its address space by a factor of 16 (there can be a maximum of 16 pages). See Figure 8.

Figure 8. Page Register (PSD3X2L/3X3L)

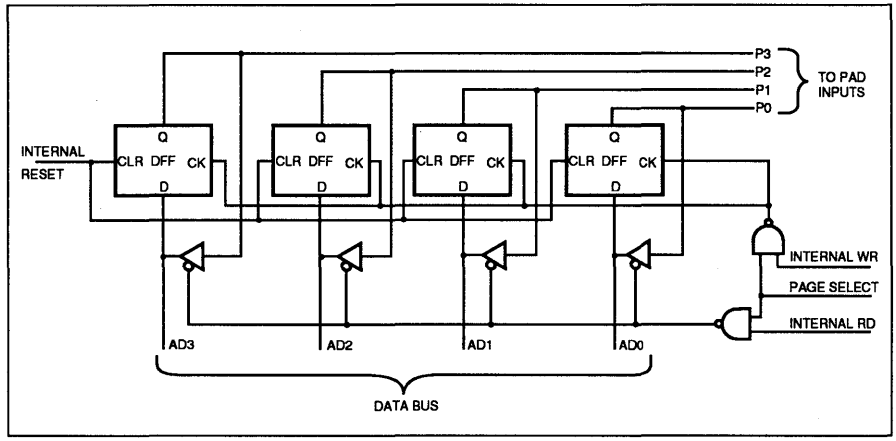


Table 8. Signal Latch Status in All Operating Modes

Signal Name	Configuration Bits	Configuration Mode	Signal Latch Status
AD8/A8–AD15/A15	CDATA , CADDRDAT, CLOT = 0	8-bit data, non-multiplexed	Transparent
	CDATA, CADDRDAT = 0, CLOT = 1		ALE Dependent
	CDATA = 1, CADDRDAT, CLOT = 0	16-bit data, non-multiplexed	Transparent
	CDATA = 1, CADDRDAT = 0, CLOT = 1		ALE Dependent
	CDATA = 0, CADDRDAT = 1	8-bit data, multiplexed	Transparent
	CDATA = 1, CADDRDAT = 1	16-bit data, multiplexed	ALE Dependent
AD0/A0-AD7/A7	CADDRDAT = 0, CLOT = 0	non-multiplexed modes	Transparent
	CADDRDAT = 0, CLOT = 1		ALE Dependent
	CADDRDAT = 1	multiplexed modes	ALE Dependent
$\overline{BHE}$/PSEN	CDATA = 0	8-bit data, $\overline{PSEN}$ is active	Transparent
	CDATA = 1, CADDRDAT = 0	16-bit data, non-multiplexed mode, $\overline{BHE}$ is active	Transparent
A19 and PC2–PC0	CDATA = 1, CADDRDAT = 1	16-bit data, multiplexed mode, $\overline{BHE}$ is active	ALE Dependent
	CADDHLT = 0	A16–A19 can become logic inputs	Transparent
	CADDHLT = 1	A16–A19 can become multiplexed address lines	ALE Dependent

Control Signals

The PSD3XXL control signals are $\overline{WR}/V_{PP}$ or R/$\overline{W}$, $\overline{RD}$/E or $\overline{RD}$/E/$\overline{DS}$, ALE, $\overline{BHE}$/$\overline{PSEN}$ or $\overline{PSEN}$, $\overline{RESET}$, and A19/$\overline{CSI}$. Each of these signals can be configured to meet the output control signal requirements of various microcontrollers.

$\overline{WR}/V_{PP}$ or R/$\overline{W}$

In operational mode, this signal can be configured as $\overline{WR}$ or R/$\overline{W}$. As $\overline{WR}$, all write operations are activated by an active low signal on this pin. As R/$\overline{W}$, the pin operates with the E strobe of the $\overline{RD}$/E/$\overline{DS}$ or $\overline{RD}$/E pin. When R/$\overline{W}$ is high, an active high signal on the $\overline{RD}$/E/$\overline{DS}$ or $\overline{RD}$/E pin performs a read operation. When R/$\overline{W}$ is low, an active high signal on the $\overline{RD}$/E/$\overline{DS}$ or $\overline{RD}$/E pin performs a write operation.

$\overline{RD}$/E/$\overline{DS}$ (or $\overline{RD}$/E on PSD3X1L)

In operational mode, this signal can be configured as $\overline{RD}$, E, or $\overline{DS}$. As $\overline{RD}$, all read operations are activated by an active low signal on this pin. As E, the pin operates with the R/$\overline{W}$ signal of the $\overline{WR}/V_{PP}$ or R/$\overline{W}$ pin. When R/$\overline{W}$ is high, an active high signal on the $\overline{RD}$/E/$\overline{DS}$ pin performs a read operation. When R/$\overline{W}$ is low, an active high signal on the $\overline{RD}$/E/$\overline{DS}$ pin performs a write operation.

As $\overline{DS}$, the pin functions with the R/$\overline{W}$ signal as an active low data strobe signal. As $\overline{DS}$, the R/$\overline{W}$ defines the mode of operation (Read or Write).

ALE or AS

ALE polarity is programmable. When programmed to be active high, a high on the pin causes the input address latches, Port A address latches, Port C, and A19 address latches to be transparent. The falling edge of ALE locks the information into the latches. When ALE is programmed to be active low, a low on the pin causes the input address latches, Port A address latches, Port C, and A19 address latches to be transparent. The rising edge of ALE locks the appropriate information into the latches.

$\overline{BHE}$/$\overline{PSEN}$

This pin's function depends on the PSD3XXL data bus width. If it is 8 bits, the pin is $\overline{PSEN}$; if it is 16 bits, the pin is $\overline{BHE}$. In 8-bit mode, the $\overline{PSEN}$ function enables the user to work with two address spaces: program memory and data memory (if COMB/SEP = 1). In this mode, an active low signal on the $\overline{PSEN}$ pin causes the EPROM to be read if selected. The SRAM and I/O ports read operation are done by $\overline{RD}$ low (CRRWR = 0), or by E high and R/$\overline{W}$ high (CRRWR = 1, CEDS = 0) or by $\overline{DS}$ low and R/$\overline{W}$ high (CRRWR, CEDS = 1).

Whenever a member of the 8031 family (or any other similar microcontroller) is used, the $\overline{PSEN}$ pin must be connected to the $\overline{PSEN}$ pin of the microcontroller.

If COMB/SEP = 0, the address spaces of the program and the data are combined. In this configuration (except for the 8031-type case mentioned above), the $\overline{PSEN}$ pin must be tied high to V_{CC}, and the EPROM, SRAM, and I/O ports are read by $\overline{RD}$ low (CRRWR = 0), or by E high and R/$\overline{W}$ high (CRRWR = 1, CEDS = 0) or by $\overline{DS}$ low and R/$\overline{W}$ high (CRRWR, CEDS = 1). See Figures 9 and 10.

In $\overline{BHE}$ mode, this pin enables accessing of the upper-half byte of the data bus. A low on this pin enables a write or read operation to be performed on the upper half of the data bus (see Table 9).

$\overline{RESET}$

This is an asynchronous input pin that clears and initializes the part. For the PSD3XXL, reset is a low signal only. Whenever the reset input is driven low for at least 500 ns, the chip is reset. After reset becomes high, the chip will be operational only after an additional 500 ns. See Figure 11. Note that during boot-up, the part is not automatically reset internally and does require an external reset. Tables 10a, 10b and 11 indicate the state of the part during and after reset.

Control Signals (Cont.)

A19/$\overline{CSI}$

When configured as $\overline{CSI}$, a high on this pin deselects, and powers down, the chip. A low on this pin puts the chip in normal operational mode. For PSD3XXL states during the power-down mode, see Tables 12 and 13, and Figure 12.

In A19 mode, the pin is an additional input to the PAD. It can be used as an address line (CADLOG3 = 1) or as a general-purpose logic input (CADLOG3 = 0). A19 can be configured as ALE dependent or as transparent input (see Table 8). In this mode, the chip is always enabled.

Figure 9. Combined Address Space

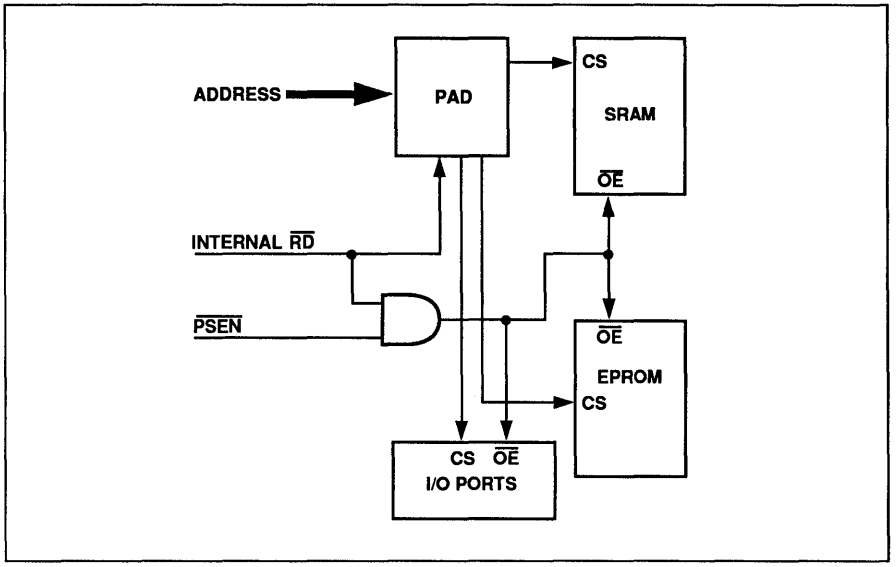


Table 9. High/Low Byte Selection Truth Table (In 16-Bit Configuration Only)

$\overline{BHE}$	A_0	Operation
0	0	Whole Word
0	1	Upper Byte From/To Odd Address
1	0	Lower Byte From/To Even Address
1	1	None

Figure 10. 8031-Type Separate Code and Data Address Spaces

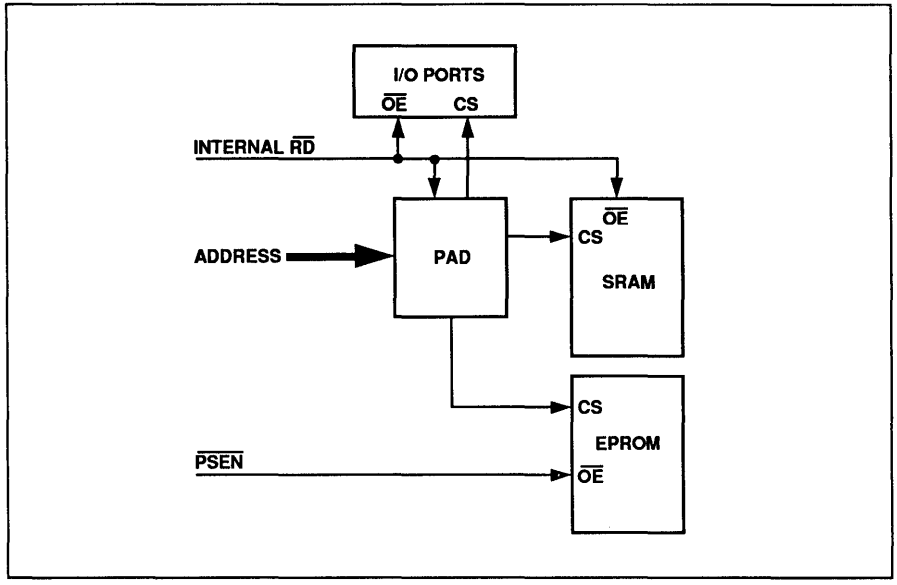


Table 10a. Signal States During Reset Cycle (RESET)

Signal	Condition
AD0/A0–AD15/A15	Input
PA0–PA7 (Port A)	Input
PB0–PB7 (Port B)	Input
PC0–PC2 (Port C)	Input

Table 10b. Signal States After Reset Cycle (RESET)

Signal	Configuration Mode	Condition
AD0/A0–AD7/A7	All	Input
A8–A15	All	Input
PA0–PA7) (Port A	I/O Tracking AD0/A0–AD7 Address outputs A0–A7	Input Input Low
PB0–PB7 (Port B)	I/O $\overline{CS7}$–$\overline{CS0}$ CMOS outputs $\overline{CS7}$–$\overline{CS0}$ open drain outputs	Input High Tri-stated
PC0–PC2 (Port C)	Address inputs A16–A18 $\overline{CS8}$–$\overline{CS10}$ CMOS outputs	Input High

Figure 11. The Reset Cycle (RESET)

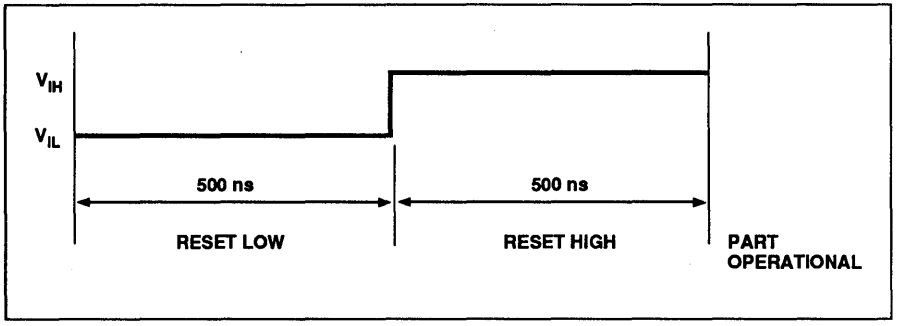
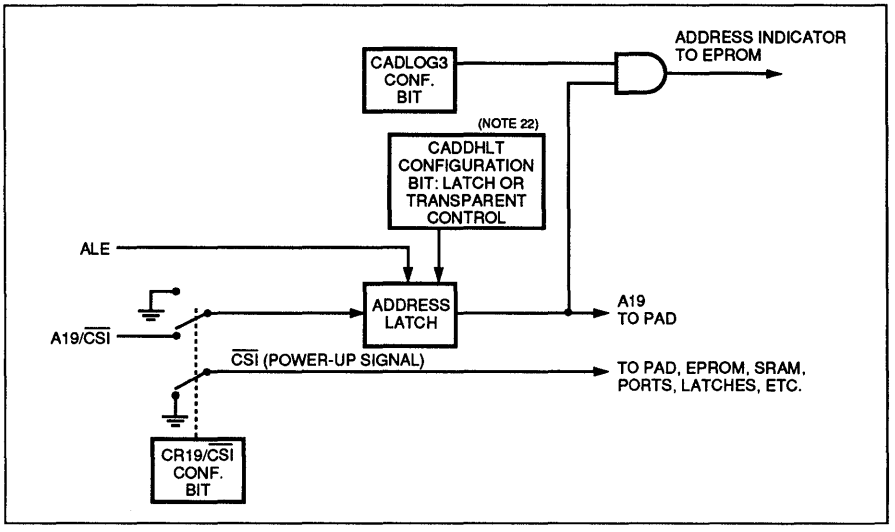


Table 11. Internal States During and After Reset Cycle

Component	Signals	Contents
PAD	$\overline{CS0}$–$\overline{CS10}$	All = 1 (Note 13)
	CSADIN, CSADOUT1, CSADOUT2, CSIOPORT, RS0, ES0 – ES7	All = 0 (Note 13)
Data register A	n/a	0
Direction register A	n/a	0
Data register B	n/a	0
Direction register B	n/a	0

NOTE: 23. All PAD outputs are in a non-active state.

Figure 12. A19/$\overline{CSI}$ Cell Structure



NOTES: 22. The CADDHLT configuration bit determines if A19–A16 are transparent via the latch, or if they must be latched by the trailing edge of the ALE strobe.

Table 12a. Signal States During Power-Down Mode (PSD30XL)

Signal	Configuration Mode	Condition
AD0/A0–AD15/A15	All	Input
PA0–PA7	I/O Tracking AD0/A0–AD7/A7 Address outputs A0–A7	Unchanged Input All 1's
PB0–PB7	I/O $\overline{CS0}$–$\overline{CS7}$ CMOS outputs $\overline{CS0}$–$\overline{CS7}$ open drain outputs	Unchanged All 1's Tri-stated
PC0–PC2	Address inputs A18–A16 $\overline{CS8}$–$\overline{CS10}$ CMOS outputs	Input All 1's

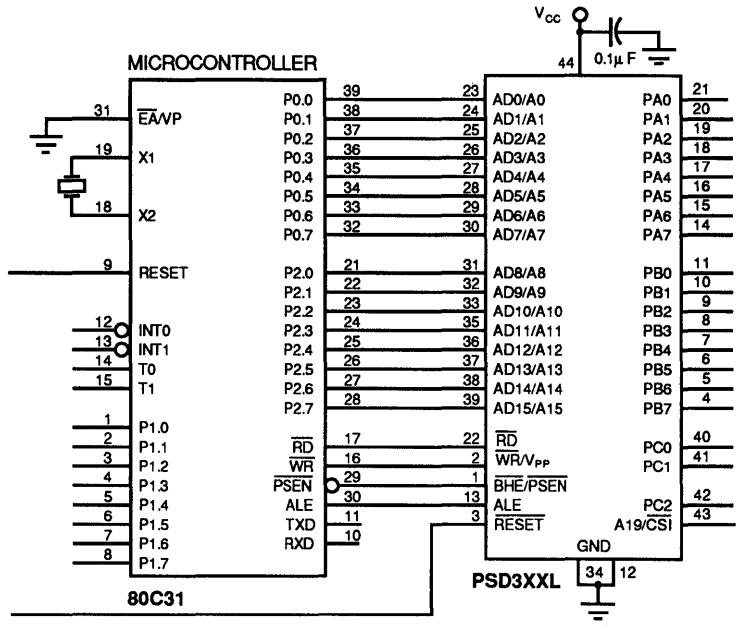
Table 12b. Signal States During Power-Down Mode (PSD31XL)

Signal	Configuration Mode	Condition
AD0/A0–AD7/A7	All	Input
A8–A15	All	Input
PA0–PA7	I/O Tracking AD0/A0–AD7/A7 Address outputs A0–A7	Unchanged Input All 1's
PB0–PB7	I/O $\overline{CS0}$–$\overline{CS7}$ CMOS outputs CS0–CS7 open drain outputs	Unchanged All 1's Tri-stated
PC0–PC2	Address inputs A18–A16 $\overline{CS8}$–$\overline{CS10}$ CMOS outputs	Input All 1's

Table 13. Internal States During Power-Down

Component	Signals	Contents
PAD	$\overline{CS0}$–$\overline{CS10}$	All 1's (deselected)
	CSADIN, CSADOUT1, CSADOUT2, CSIOPORT, RS0, ES0–ES7	All 0's (deselected)
Data register A Direction register A Data register B Direction register B	n/a n/a n/a n/a	All unchanged

Figure 13. PSD3XXL Interface With Intel's 80C31



NOTE: RESET to the PSD3XXL must be the output of a RESET chip or buffer. If RESET is the output of an RC circuit, a separate buffered RC RESET to the PSD3XXL (shorter than the 80C31 RC RESET) must be provided to avoid a race condition.

The configuration bits for Figure 13 are:

CALE	0	COMB/SEP	0 or 1 (both valid)
CDATA	0	CRRWR	0
CADDRDAT	1	CEDS	0

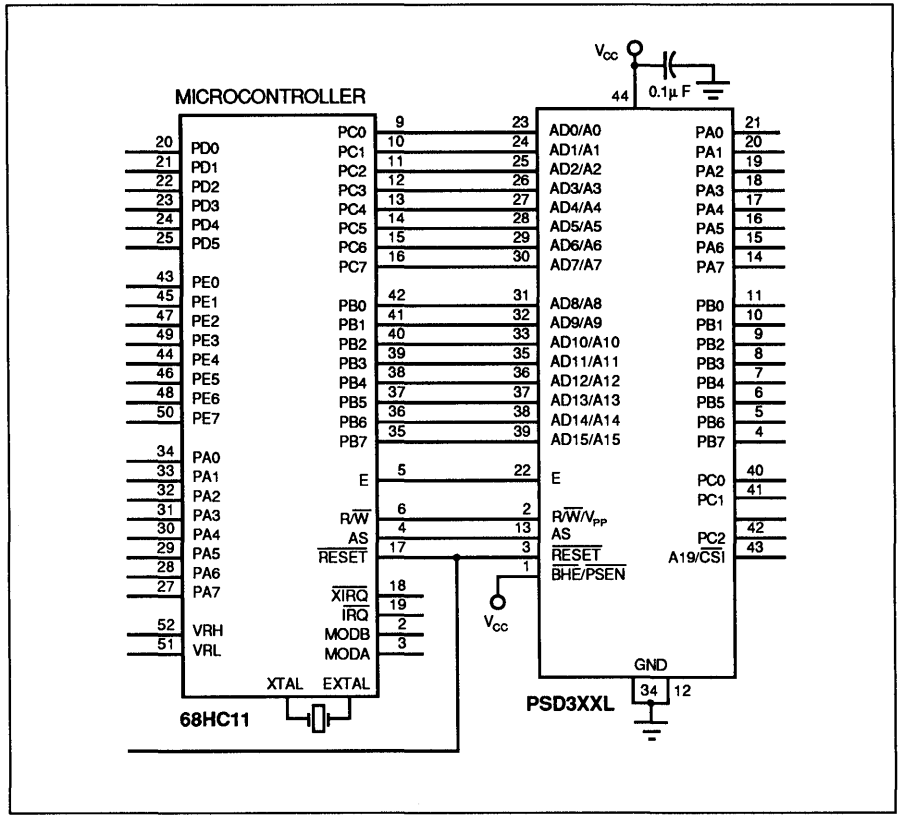
All other configuration bits may vary according to the application requirements.

System Applications

In Figure 13, the PSD3XXL is configured to interface with Intel's 80C31, which is a 16-bit address/8-bit data bus microcontroller. Its data bus is multiplexed with the low-order address byte. The 80C31 uses signals $\overline{RD}$ to read from data memory and $\overline{PSEN}$ to read from code memory. It uses $\overline{WR}$ to write into the data memory. It also uses active high reset and ALE signals. The rest of the configuration bits as well as the unconnected signals (not shown) are application specific and, thus, user dependent.

In Figure 14, the PSD3XXL is configured to interface with Motorola's 68HC11, which is a 16-bit address/8-bit data bus microcontroller. Its data bus is multiplexed with the low-order address byte. The 68HC11 uses E and R/W signals to derive the read and write strobes. It uses the term AS (address strobe) for the address latch pulse. $\overline{RESET}$ is an active low signal. The rest of the configuration bits as well as the unconnected signals (not shown) are specific and, thus, user dependent.

Figure 14. PSD3XXL Interface With Motorola's 68HC11



The configuration bits for Figure 14 are:

CALE	0	CRRWR	1
CDATA	0	CEDS	0
CADDRDAT	1		
COMB/SEP	0		

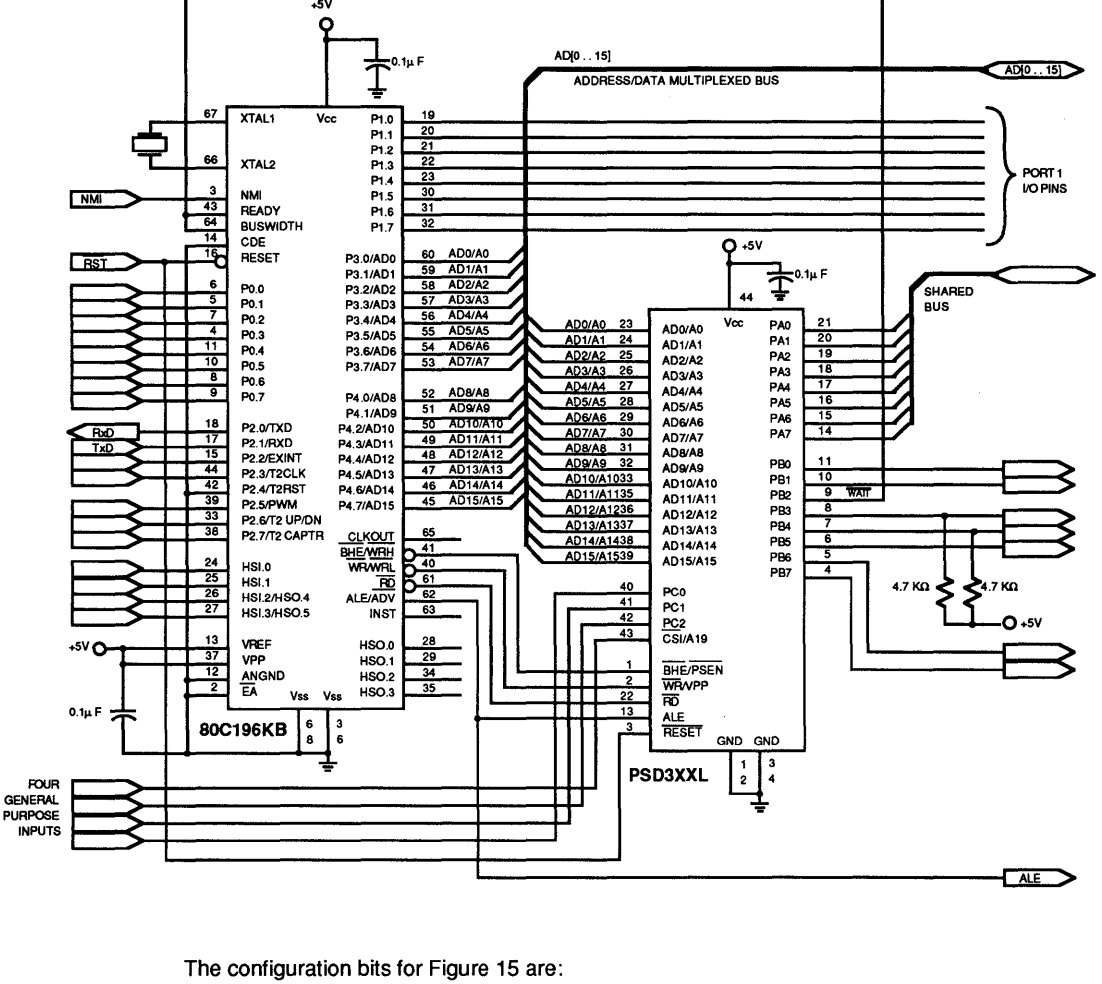
All other configuration bits may vary according to the application requirements.

System Applications (Cont.)

In Figure 15, the PSD3XXL is configured to work directly with Intel's 80C196KB microcontroller, which is a 16-bit address/16-bit data bus processor. Address and data lines multiplexed. In the example shown, all configuration bits are set. The PSD3XXL is configured to use PC0, PC1, PC2, and CSI/A19 as A16, A17, A18, and A19 inputs, respectively. These signals are independent of the ALE pulse (latch-transparent). They are used as four general-purpose logic inputs that take part in the PAD equations implementation.

Port A is configured to work in the special track mode, in which (for certain conditions) PA0–PA7 tracks lines AD0/A0–AD7/A7. Port B is configured to generate CS0–CS7. In this example, PB2 serves as a WAIT signal that slows down the 80C196KB during the access of external peripherals. These 8-bit wide peripherals are connected to the shared bus of Port A. The WAIT signal also drives the buswidth input of the microcontroller, so that every external peripheral cycle becomes an 8-bit data bus cycle. PB3 and PB4 are open-drain output signals; thus, they are pulled up externally.

Figure 15. PSD3XXL Interface With Intel's 80C196KB.



The configuration bits for Figure 15 are:

CALE	0	CSECURITY	Don't care
CDATA	1	CPCF2, CPCF1, CPCF0	0, 0, 0
CADDRDAT	1	CPACOD7–CPACOD0	00H
CPAF1	Don't care	CPBF7–CPBF0	00H
CPAF2	1	CPBCOD7–CPBCOD0	18H
CA19/$\overline{CSI}$	1	CEDS	0
CRRWR	0	CADLOG3—CADLOG0	0H
COMB/SEP	0		
CADDHLT	0		

Security Mode

Security Mode in the PSD3XX locks the contents of the PAD A , PAD B and all the configuration bits. The EPROM, SRAM, and I/O contents can be accessed only through the PAD. The Security Mode can be set by the MAPLE or Programming software. In window packages, the mode is erasable through UV full part erasure. In the security mode, the PSD3XX contents cannot be copied on a programmer.

CMiser-Bit

The CMiser-Bit provides a programmable option for power-sensitive applications that require further reduction in power consumption. The CMiser-Bit (CMiser = 1) in the Maple portion of the PSD3XX sytem development software can be used to reduce power consumption. The CMiser-Bit turns off the EPROM blocks in the PSD3XX whenever the EPROM is not accessed, thereby reducing the active current consumed by the PSD3XX.

In the default mode, or if the PSD3XX is configured without programming the CMiser-Bit (CMiser = 0), the device operates at specified speed and power rating as specified in the A.C. and D.C. Characteristics.

However, if the CMiser-Bit is programmed (CMiser = 1), the device consumes even lower current, and is reflected in the data sheet. This mode has an adder in propagation delay in T5, T6, and T7 parameters in the A.C. Characteristics, and should be added to compute worst-case timing requirements in the application.

3-volt single-chip microcontroller peripheral — PSD301L

Key Features

- ❑ Single Chip Programmable Peripheral for Microcontroller-based Applications
- ❑ 3.0 to 5.5 Volt Operation
- ❑ 19 Individually Configurable I/O pins that can be used as:
  - — Microcontroller I/O port expansion
  - — Programmable Address Decoder (PAD) I/O
  - — Latched address output
  - — Open drain or CMOS
- ❑ Two Programmable Arrays (PAD A and PAD B)
  - — Total of 40 Product Terms and up to 14 Inputs and 24 Outputs
  - — Address Decoding up to 1 MB
  - — Logic replacement
- ❑ "No Glue" Microcontroller Chip-Set
  - — Built-in address latches for multiplexed address/data bus
  - — Non-multiplexed address/data bus mode
  - — Selectable 8 or 16 bit data bus width
  - — ALE and Reset polarity programmable
  - — Selectable modes for read and write control bus as $\overline{RD}/\overline{WR}$ or R/$\overline{W}$/E
  - — $\overline{BHE}$ pin for byte select in 16-bit mode
  - — $\overline{PSEN}$ pin for 8051 users
- ❑ 256 Kbits of UV EPROM
  - — Configurable as 32K x 8 or as 16K x 16
  - — Divides into 8 equal mappable blocks for optimized mapping
  - — Block resolution is 4K x 8 or 2K x 16
  - — 250 ns EPROM access time, including input latches and PAD address decoding.
- ❑ 16 Kbit Static RAM
  - — Configurable as 2K x 8 or as 1K x 16
  - — 250 ns SRAM access time, including input latches and PAD address decoding
- ❑ Address/Data Track Mode
  - — Enables easy Interface to Shared Resources (e.g., Mail Box SRAM) with other Microcontrollers or a Host Processor
- ❑ Built-In Security
  - — Locks the PSD301L and PAD Decoding Configuration
- ❑ Available in a Choice of Packages
  - — 44 Pin PLDCC and CLDCC
- ❑ Simple Menu-Driven Software: Configure the PSD301L on an IBM PC
- ❑ Pin Compatible with the PSD3XX and PSD3XXL Series

Absolute Maximum Ratings[1]

Symbol	Parameter	Condition	Min	Max	Unit
T_{STG}	Storage Temperature	CERAMIC	−65	+150	°C
		PLASTIC	−65	+125	°C
T_{STG}	Storage Temperature		−65	+150	°C
	Voltage on any Pin	With Respect to GND	−0.6	+7	V
V_{PP}	Programming Supply Voltage	With Respect to GND	−0.6	+14	V
V_{CC}	Supply Voltage	With Respect to GND	−0.6	+7	V
	ESD Protection			>2000	V

NOTE: 1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods of time may affect device reliability.

Operating Range

Range	Temperature	V_{CC}
Commercial	0° C to +70°C	3.0 to 5.5 V

Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	Supply Voltage	All Speeds	3.0	3.3	5.5	V
V_{IH}	High-level Input Voltage	V_{CC} = 3.0 V to 5.5 V	0.7 V_{CC}		V_{CC} + 0.5	V
V_{IL}	Low-level Input Voltage	V_{CC} = 3.0 V to 5.5 V	−0.5		0.2 V_{CC}*	V
					0.3 V_{CC}**	V

*Before 8/1/1993.
**After 8/1/1993.

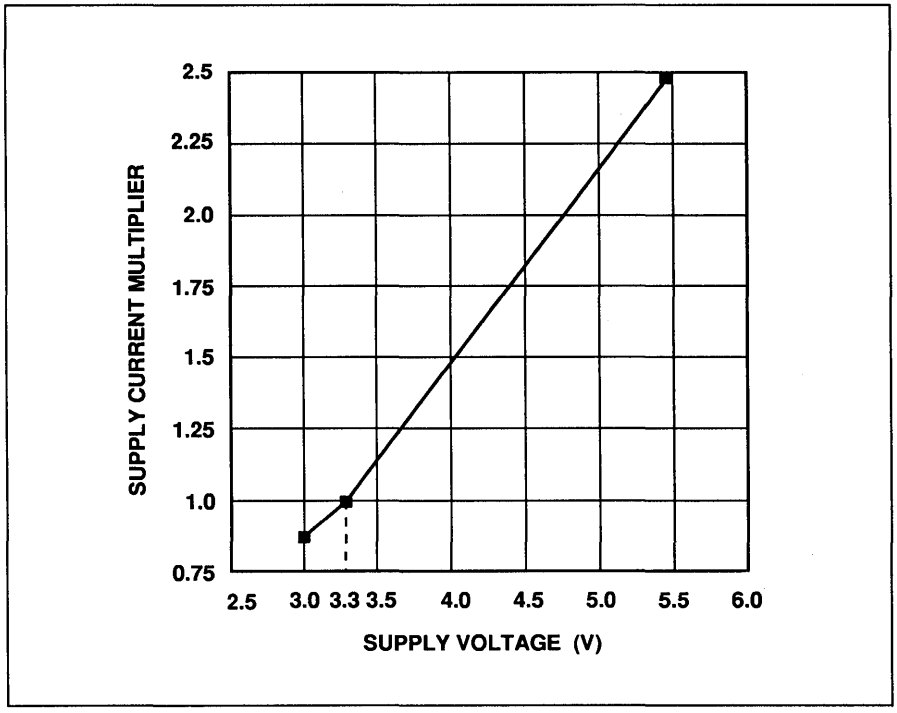
DC Characteristics

Symbol	Parameter	Conditions				CMiser = 1 Subtract:**			Unit
			Min	Typ	Max	Min	Typ	Max	
V_{OL}	Output Low Voltage	I_{OL} = 20 µA V_{CC} = 3.0 V		0.01	0.1				V
		I_{OL} = 4 mA V_{CC} = 3.0 V		0.15	0.4				V
V_{OH}	Output High Voltage	I_{OH} = –20 µA V_{CC} = 3.0 V	2.9	2.99					V
		I_{OH} = –1 mA V_{CC} = 3.0 V	2.4	2.6					V
I_{SB1}	V_{CC} Standby Current (CMOS) (Notes 2 and 3)	V_{CC} = 3.3 V		10*	25*				µA
				1**	5**				
I_{CC1}	Active Current (CMOS) (No Internal Memory Block Selected) (Notes 2 and 5)	V_{CC} = 3.3 V (Note 5)		6	12		3.0	5	mA
		V_{CC} = 3.3 V (Note 6)		10	20		3.0	5	mA
I_{CC2}	Active Current (CMOS) (EPROM Block Selected) (Notes 2 and 5)	V_{CC} = 3.3 V (Notes 5 and 7)		6	12		0	0	mA
		V_{CC} = 3.3 V (Note 6 and 7)		10	20		0	0	mA
I_{CC3}	Active Current (CMOS) (SRAM Block Selected) (Notes 2 and 5)	V_{CC} = 3.3 V (Note 5 and 7)		20	33		3	5	mA
		V_{CC} = 3.3 V (Notes 6 and 7)		24	40		3	5	mA
I_{LI}	Input Leakage Current	V_{IN} = V_{CC} or GND	–1	±0.1	1				µA
I_{LO}	Output Leakage Current	V_{OUT} = V_{CC} or GND	–10	±5	10				µA

NOTES: 2. CMOS inputs: GND ± 0.3 V or V_{CC} ± 0.3V.
3. $\overline{CSI}$/A19 is high and the part is in a power-down configuration mode.
4. Add 2.0 mA/MHz for AC power component (power = AC + DC).
5. Ten (10) PAD product terms active. (Add 190 µA per product term, typical, or 240 µA per product term maximum.)
6. Forty (40) PAD product terms active.
7. In 8-bit mode, an additional 3 mA Max can be saved under CMiser.

*Before 8/1/1993.
**After 8/1/1993.

Figure 1. Normalized Supply Current vs. Supply Voltage



The Normalized Supply Current vs. Supply Voltage graph shown above, provides a multiplier for any I_{SB} or I_{CC} value in the D.C. Characteristics table. As noted, it is normalized for a supply voltage of 3.3 volts. Since device characterization data shows very little supply current difference over speed, the multiplier includes all frequencies of operation from standby to quiescent to full dynamic speed. To use, calculate the supply current at 3.3 volts for your operation configuration using the D.C. Characteristics table. Then multiply that value by the Supply Current Multiplier for the supply voltage actually being used.

AC Characteristics[8] (See Timing Diagrams)

Symbol	Parameter	-25		-30		CMiser = 1 Add:**	Unit
		Min	Max	Min	Max		
T1	ALE or AS Pulse Width	75		80			ns
T2	Address Set-up Time	30		35			ns
T3	Address Hold Time	30		35		0	ns
T4	Leading Edge of Read to Data Active	0		0		0	ns
T5	ALE Valid to Data Valid		250		300	25	ns
T6	Address Valid to Data Valid		250		300	25	ns
T7	$\overline{CSI}$ Active to Data Valid		275		325	30	ns
T8	Leading Edge of Read to Data Valid		90		95	0	ns
T9	Read Data Hold Time	0		0		0	ns
T10	Trailing Edge of Read to Data High-Z		50		55	0	ns
T11	Trailing Edge of ALE or AS to Leading Edge of Write		40		45		ns
T12	$\overline{RD}$, E, $\overline{PSEN}$, $\overline{DS}$ Pulse Width	100		110		0	ns
T12A	$\overline{WR}$ Pulse Width	90		95		0	ns
T13	Trailing Edge of Write or Read to Leading Edge of ALE or AS	0		0		0	ns
T14	Address Valid to Trailing Edge of Write	250		300		0	ns
T15	$\overline{CSI}$ Active to Trailing Edge of Write	275		375		0	ns
T16	Write Data Set-up Time	60		65		0	ns
T17	Write Data Hold Time	25		30		0	ns
T18	Port to Data Out Valid Propagation Delay		70		75	0	ns
T19	Port Input Hold Time	0		0		0	ns
T20	Trailing Edge of Write to Port Output Valid	100		110		0	ns
T21	ADi or Control to $\overline{CSOi}$ Valid	6	80	5	85	0	ns
T22	ADi or Control to $\overline{CSOi}$ Invalid	4	80	4	85	0	ns
T23	Track Mode Address Propagation Delay: CSADOUT1 Already True		70		75	0	ns
T23A	Track Mode Address Propagation Delay: CSADOUT1 Becomes True During ALE or AS		100		110	0	ns
T24	Track Mode Trailing Edge of ALE or AS to Address High-Z		60		65	0	ns

NOTE: 8. These AC Characteristics are for V_{CC} = 3.0 – 3.6V.

AC Characteristics (Cont.)

Symbol	Parameter	-25		-30		CMiser = 1 Add:**	Unit
		Min	Max	Min	Max		
T24	Track Mode Trailing Edge of ALE or AS to Address High-Z		60		65	0	ns
T25	Track Mode Read Propagation Delay		70		75	0	ns
T26	Track Mode Read Hold Time	10	70	10	75		ns
T27	Track Mode Write Cycle, Data Propagation Delay		60		65	0	ns
T28	Track Mode Write Cycle, Write to Data Propagation Delay	7	80	7	85	0	ns
T29	Hold Time of Port A Valid During Write $\overline{CSOi}$ Trailing Edge	4		4		0	ns
T30	$\overline{CSI}$ Active to $\overline{CSOi}$ Active	9	110	8	120	0	ns
T31	$\overline{CSI}$ Inactive to $\overline{CSOi}$ Inactive	9	110	8	120	0	ns
T32	Direct PAD Input as Hold Time	24		30		0	ns
T33	R/$\overline{W}$ Active to E or $\overline{DS}$ Start	60		65		0	ns
T34	E or $\overline{DS}$ End to R/$\overline{W}$	60		65		0	ns
T35	AS Inactive to E high	40		45		0	ns
T36	Address to Leading Edge of Write	50		60		0	ns

NOTES: 9. ADi = any address line.
10. $\overline{CSOi}$ = any of the chip-select output signals coming through Port B ($\overline{CS0}$–$\overline{CS7}$) or through Port C ($\overline{CS8}$–$\overline{CS10}$).
11. Direct PAD input = any of the following direct PAD input lines: $\overline{CSI}$/A19 as transparent A19, $\overline{RD}$/E/$\overline{DS}$, $\overline{WR}$ or R/$\overline{W}$, transparent PC0–PC2, ALE (or AS).
12. Control signals $\overline{RD}$/E/$\overline{DS}$ or $\overline{WR}$ or R/$\overline{W}$.

**After 8/1/1993.

Figure 2. AC Testing Input/Output Waveform

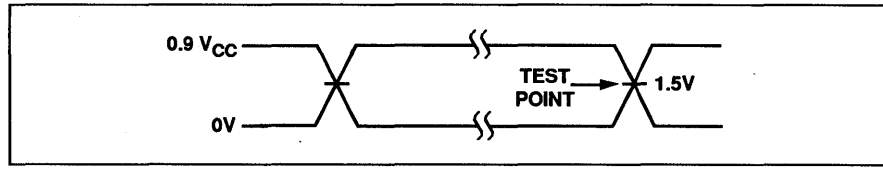


Figure 3. AC Testing Load Circuit

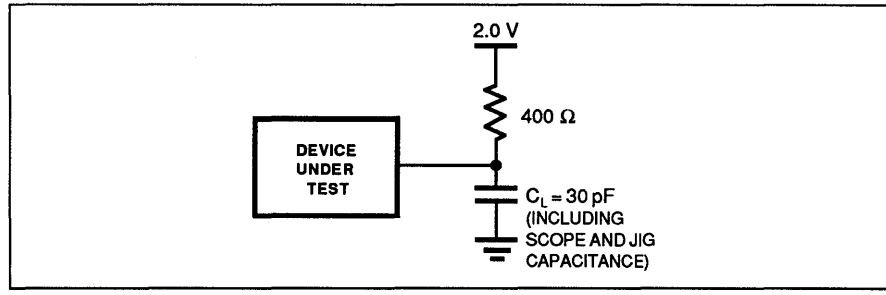


Figure 4. The Reset Cycle (RESET)

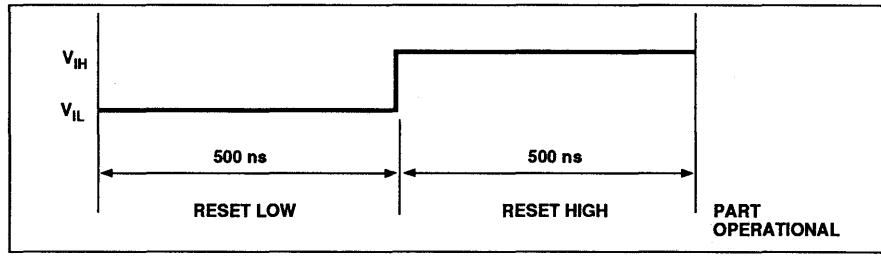
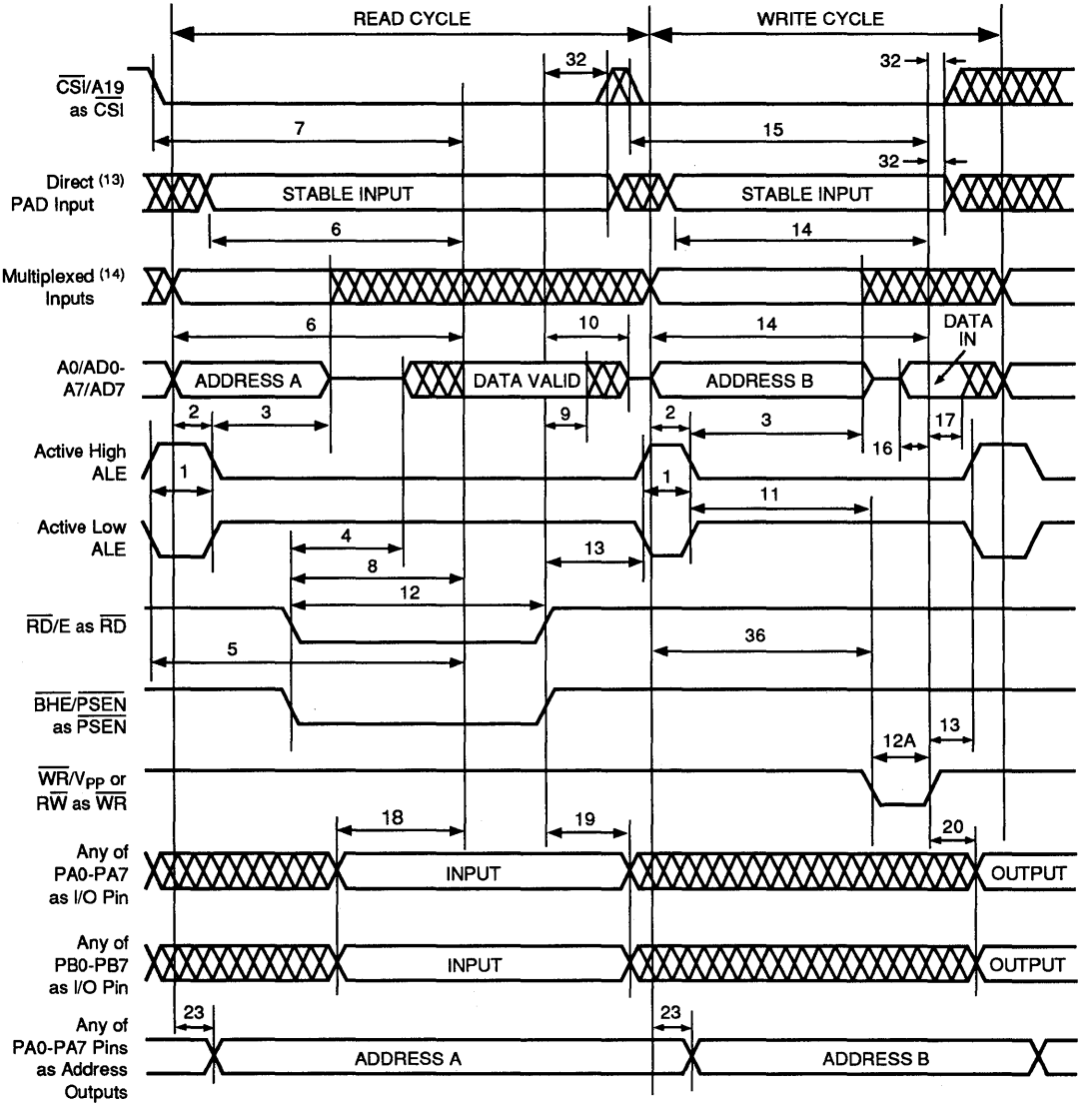
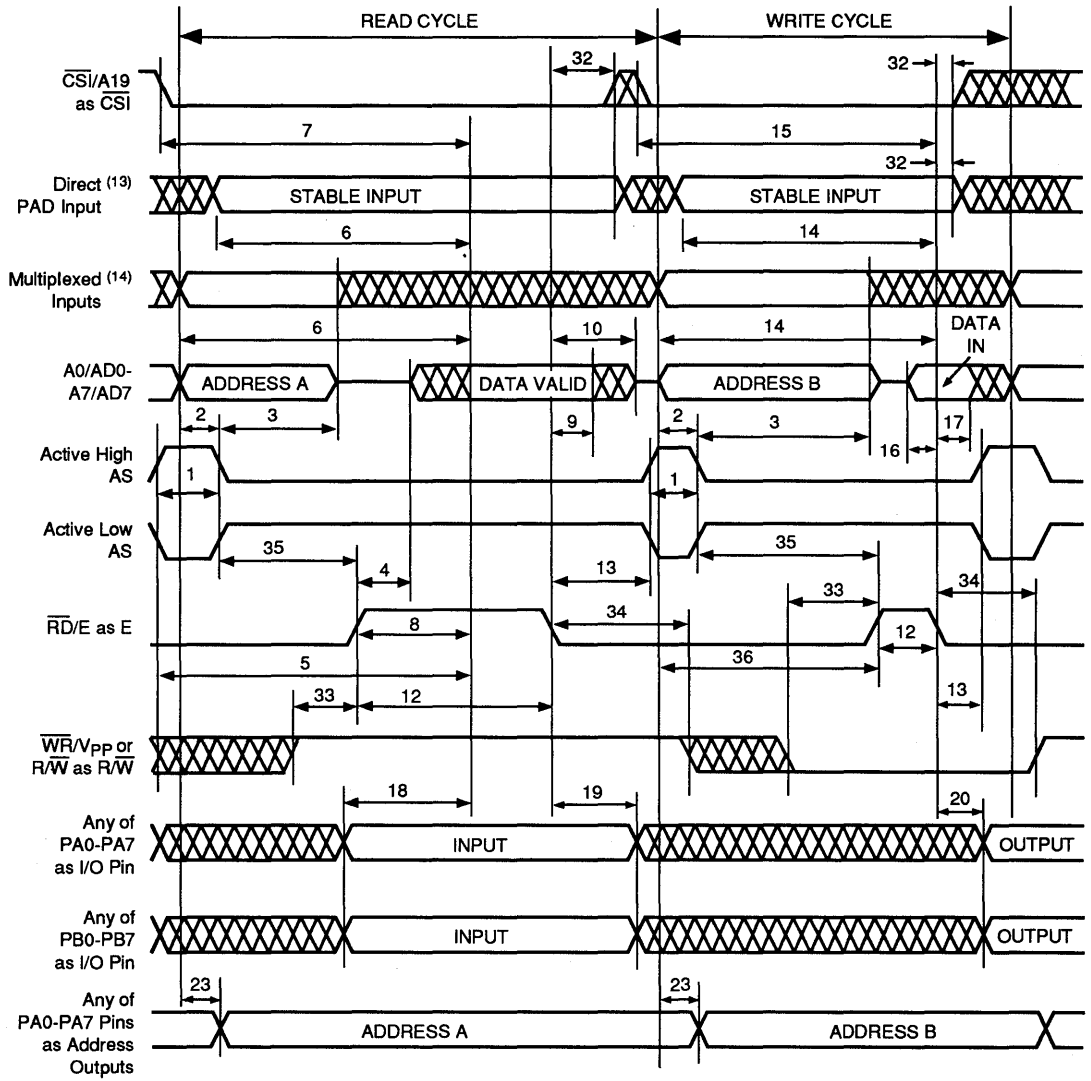


Figure 5. Timing of 8-Bit Multiplexed Address/Data Bus, CRRWR = 0



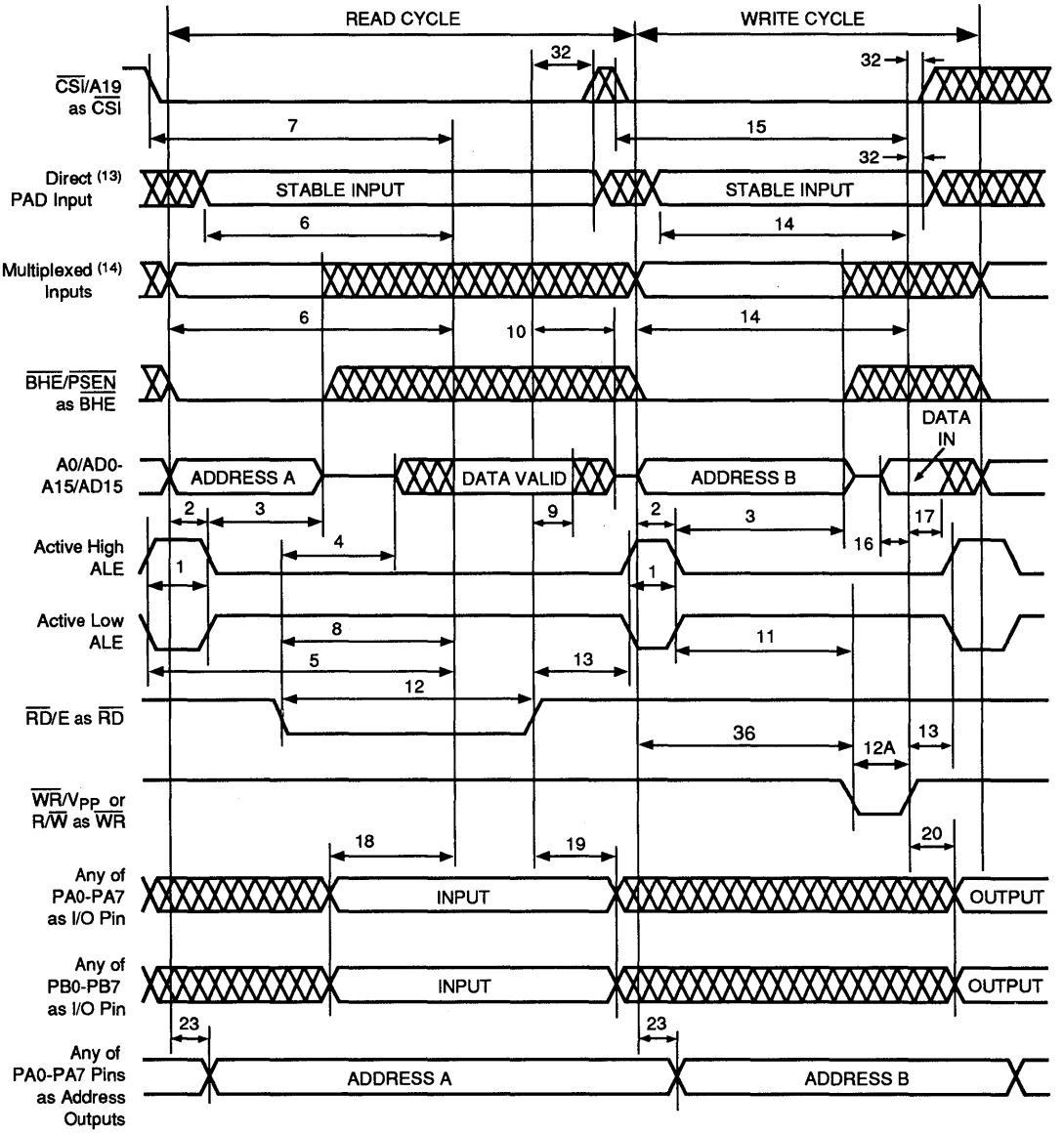
See referenced notes on page 198.

Figure 6. Timing of 8-Bit Multiplexed Address/Data Bus, CRRWR = 1



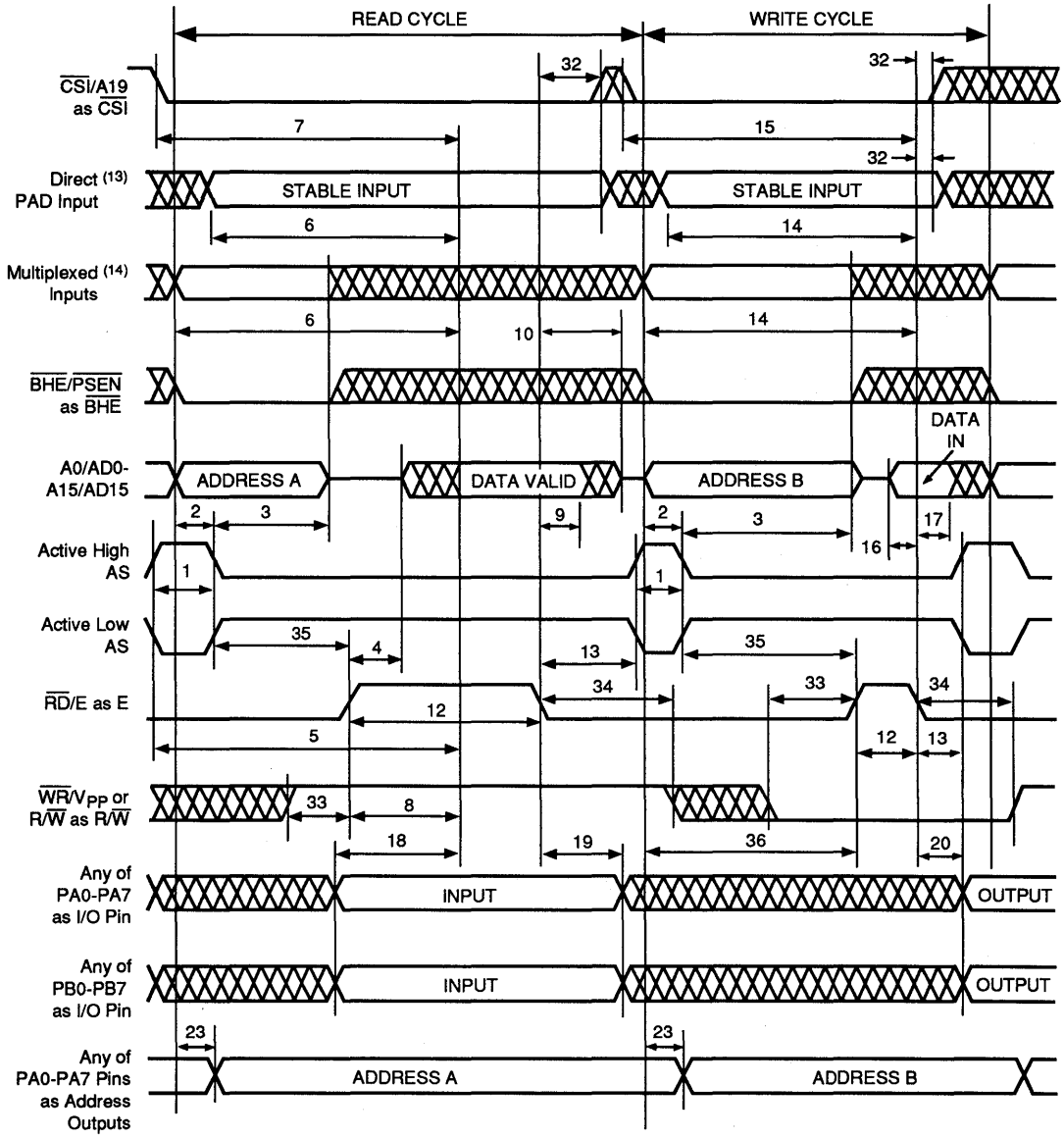
See referenced notes on page 198.

Figure 7. Timing of 16-Bit Multiplexed Address/Data Bus, CRRWR = 0



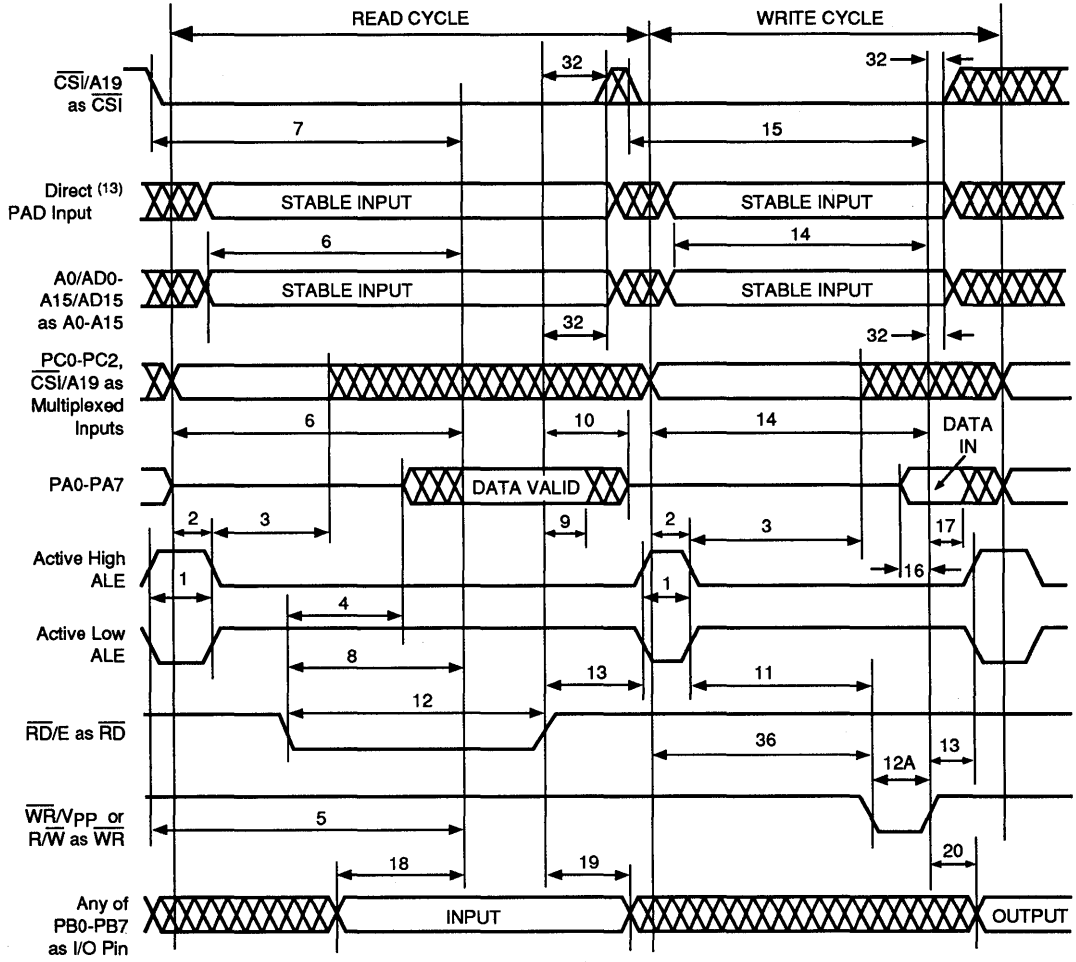
See referenced notes on page 198.

Figure 8. Timing of 16-Bit Multiplexed Address/Data Bus, CRRWR = 1



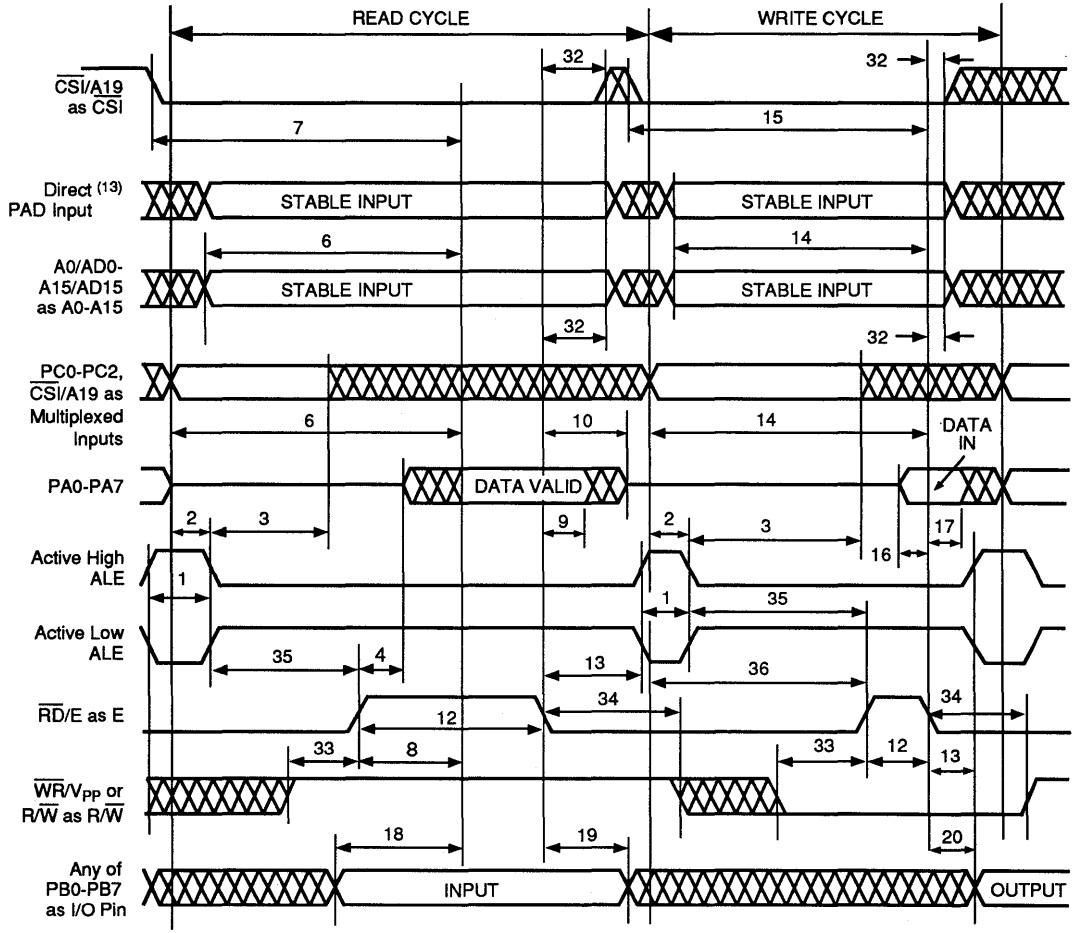
See referenced notes on page 198.

Figure 9. Timing of 8-Bit Data Non-Multiplexed Address/Data Bus, CRRWR = 0



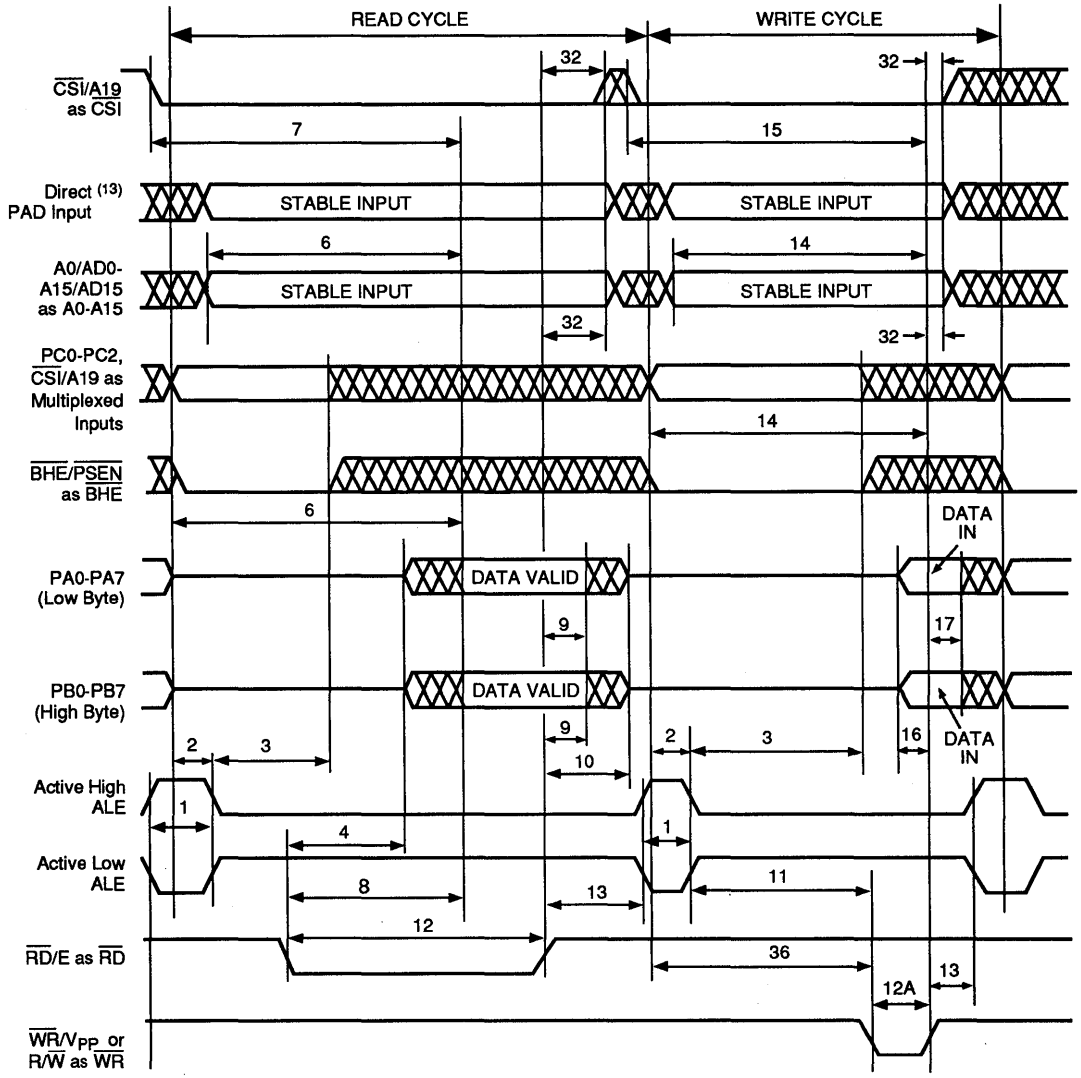
See referenced notes on page 198.

Figure 10. Timing of 8-Bit Data Non-Multiplexed Address/Data Bus, CRRWR = 1



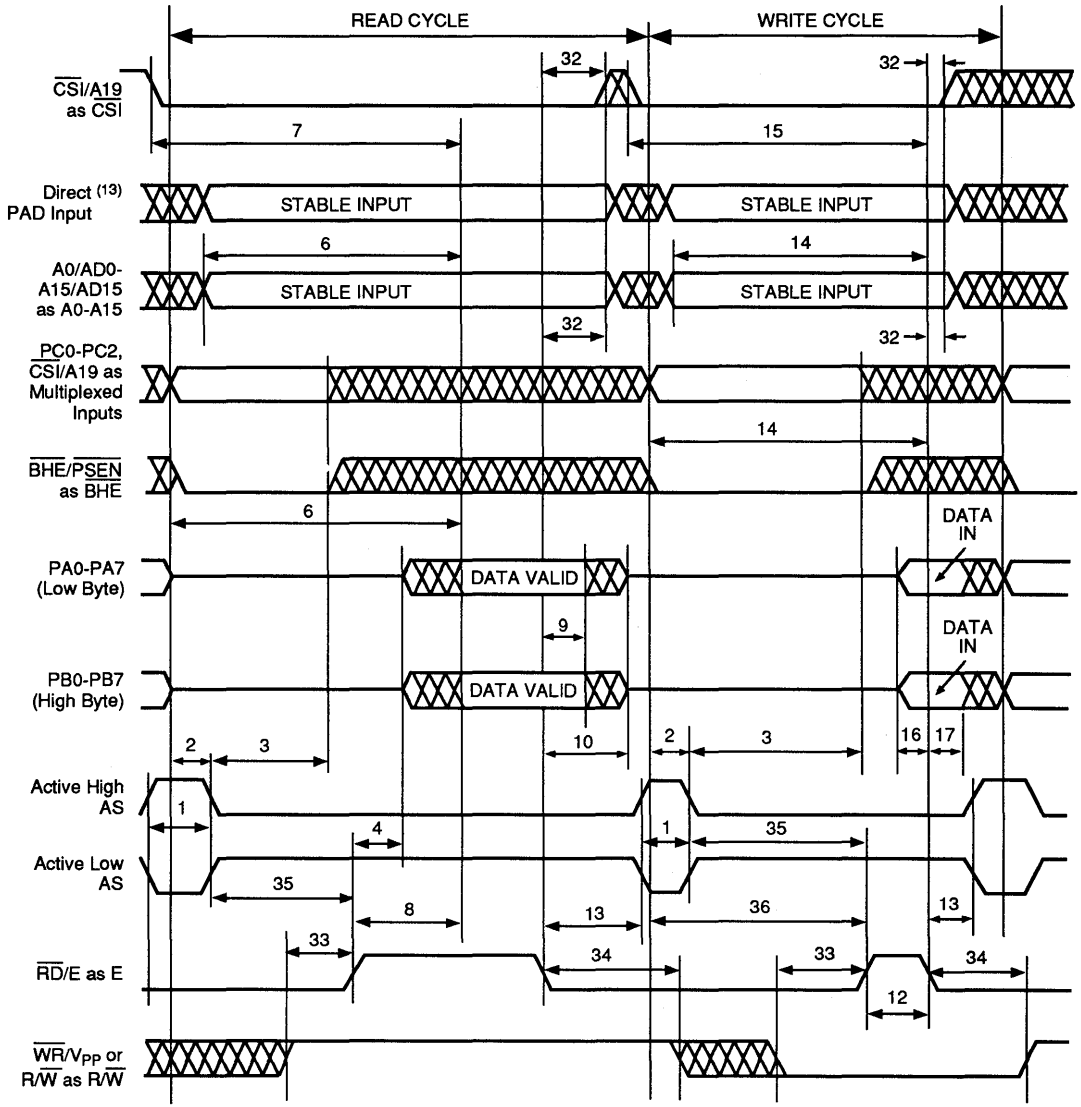
See referenced notes on page 198.

Figure 11. Timing of 16-Bit Non-Multiplexed Address/Data Bus, CRRWR = 0



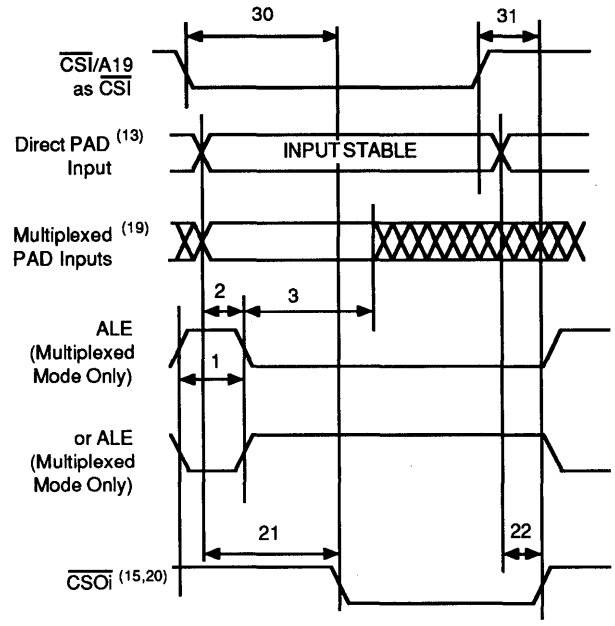
See referenced notes on page 198.

Figure 12. Timing of 16-Bit Non-Multiplexed Address/Data Bus, CRRWR = 1



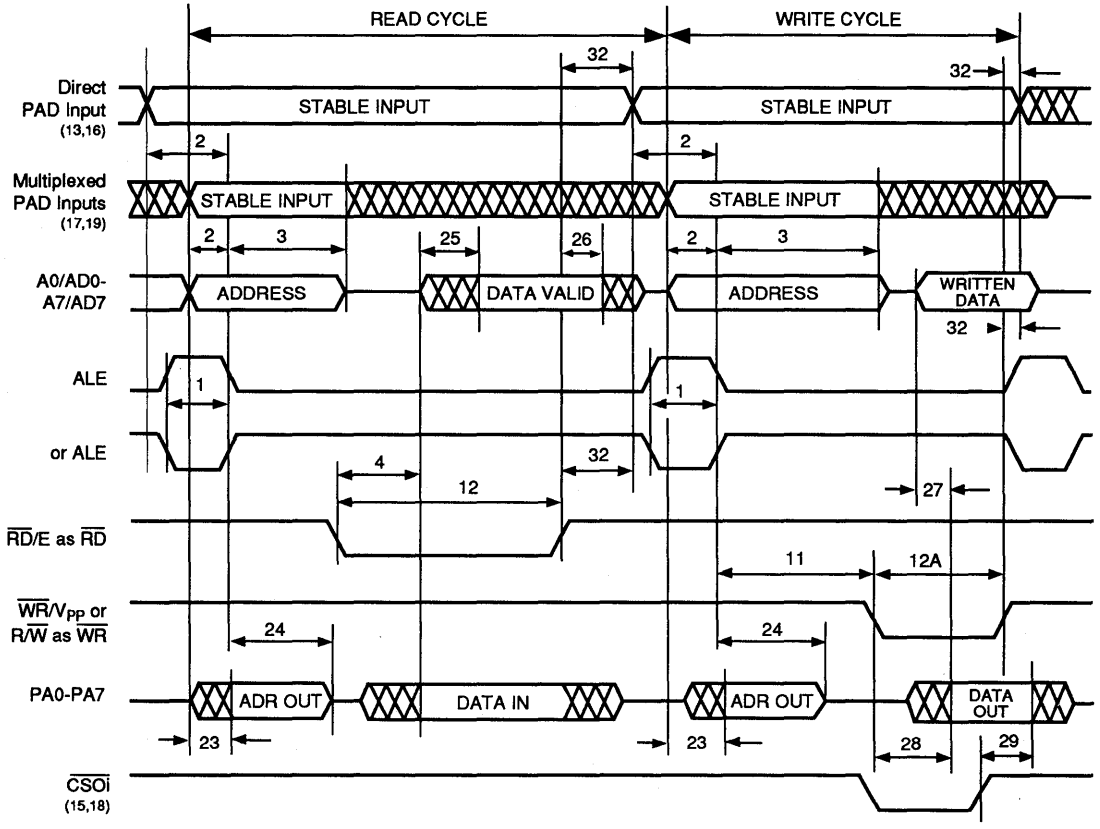
See referenced notes on page 198.

Figure 13. Chip-Select Output Timing



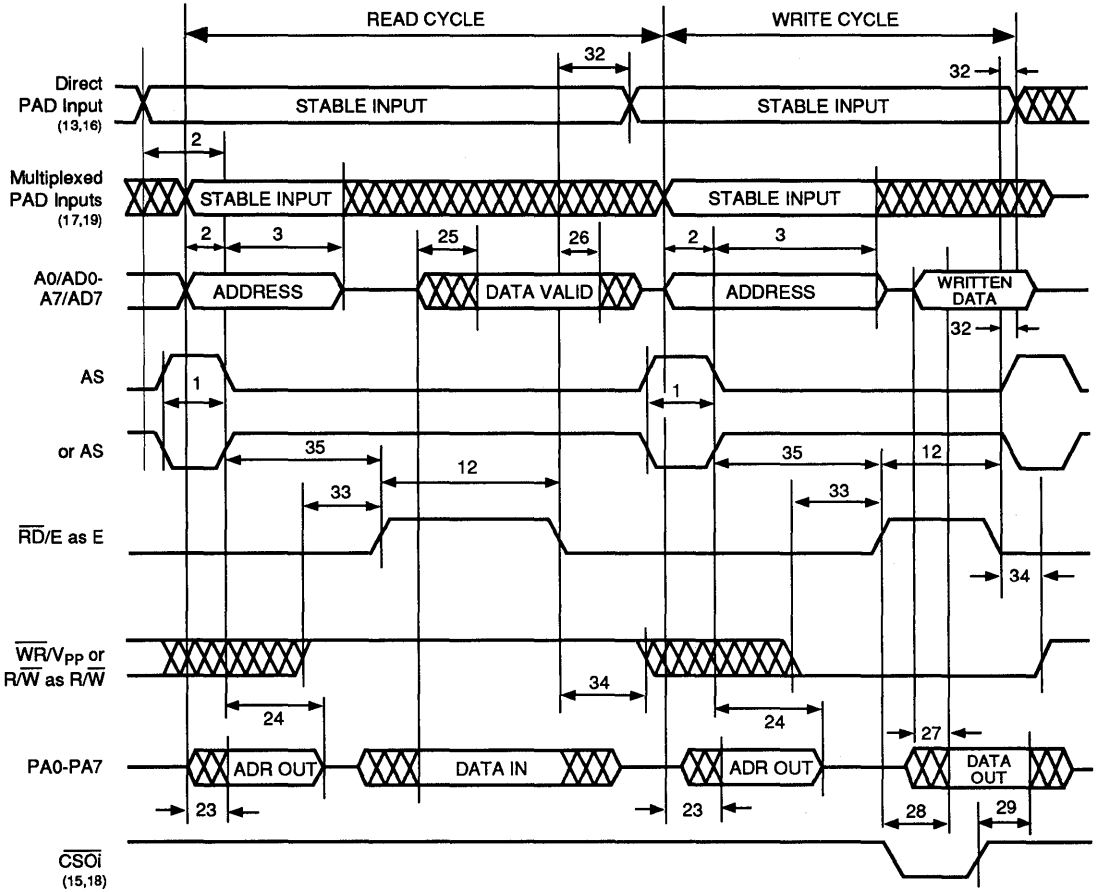
See referenced notes on page 198.

Figure 14. Port A as AD0 – AD7 Timing (Track Mode), CRRWR = 0



See referenced notes on page 198.

Figure 15. Port A as AD0 – AD7 Timing (Track Mode), CRRWR = 1



Notes for Timing Diagrams

13. Direct PAD input = any of the following direct PAD input lines: $\overline{CSI}$/A19 as transparent A19, $\overline{RD}$/E/$\overline{DS}$, $\overline{WR}$ or R/$\overline{W}$, transparent PC0–PC2, ALE in non-multiplexed modes.
14. Multiplexed inputs: any of the following inputs that are latched by the ALE (or AS): A0/AD0–A15/AD15, $\overline{CSI}$/A19 as ALE dependent A19, ALE dependent PC0–PC2.
15. $\overline{CSOi}$ = any of the chip-select output signals coming through Port B ($\overline{CS0}$–$\overline{CS7}$) or through Port C ($\overline{CS8}$–$\overline{CS10}$).
16. CSADOUT1, which internally enables the address transfer to Port A, should be derived only from direct PAD input signals, otherwise the address propagation delay is slowed down.
17. CSADIN and CSADOUT2, which internally enable the data-in or data-out transfers, respectively, can be derived from any combination of direct PAD inputs and multiplexed PAD inputs.
18. The write operation signals are included in the $\overline{CSOi}$ expression.
19. Multiplexed PAD inputs: any of the following PAD inputs that are latched by the ALE (or AS) in the multiplexed modes: A11/AD11–A15/AD15, $\overline{CSI}$/A19 as ALE dependent A19, ALE dependent PC0–PC2.
20. $\overline{CSOi}$ product terms can include any of the PAD input signals except for reset and $\overline{CSI}$.

Pin Capacitance[21]

$T_A = 25\,°C, f = 1\ MHz$

Symbol	Parameter	Conditions	Typical[22]	Max	Unit
C_{IN}	Capacitance (for input pins only)	$V_{IN} = 0$ V	4	6	pF
C_{OUT}	Capacitance (for input/output pins)	$V_{OUT} = 0$ V	8	12	pF
C_{VPP}	Capacitance (for $\overline{WR}/V_{PP}$ or $R/\overline{W}/V_{PP}$)	$V_{PP} = 0$ V	18	25	pF

NOTES: 21. This parameter is only sampled and is not 100% tested.
22. Typical values are for $T_A = 25°C$ and nominal supply voltages.

Erasure and Programming

To clear all locations of their programmed contents, expose the device to ultra-violet light source. A dosage of 15 W second/cm^2 is required. This dosage can be obtained with exposure to a wavelength of 2537 Å and intensity of 12000 μW/cm^2 for 15 to 20 minutes. The device should be about 1 inch from the source, and all filters should be removed from the UV light source prior to erasure.

The PSD301L and similar devices will erase with light sources having wavelengths shorter than 4000 Å. Although the erasure times will be much longer than with UV sources at 2537 Å, exposure to fluorescent light and sunlight eventually erases the device. For maximum system reliability, these sources should be avoided. If used in such an environment, the package windows should be covered by an opaque substance.

Upon delivery, or after each erasure, the PSD301L device has all bits in the PAD and EPROM in the "1" or high state. The configuration bits are in the "0" or low state. The code, configuration, and PAD MAP data are loaded through the procedure of programming

Pin Assignments

Pin Name	44-Pin PLCC/CLCC Package
$\overline{BHE}/\overline{PSEN}$	1
$\overline{WR}/V_{PP}$ or $R/\overline{W}$	2
$\overline{RESET}$	3
PB7	4
PB6	5
PB5	6
PB4	7
PB3	8
PB2	9
PB1	10
PB0	11
GND	12
ALE or AS	13
PA7	14
PA6	15
PA5	16
PA4	17
PA3	18
PA2	19
PA1	20
PA0	21
$\overline{RD}/E$	22
AD0/A0	23
AD1/A1	24
AD2/A2	25
AD3/A3	26
AD4/A4	27
AD5/A5	28
AD6/A6	29
AD7/A7	30
AD8/A8	31
AD9/A9	32
AD10/A10	33
GND	34
AD11/A11	35
AD12/A12	36
AD13/A13	37
AD14/A14	38
AD15/A15	39
PC0	40
PC1	41
PC2	42
A19/$\overline{CSI}$	43
V_{CC}	44

Package Information

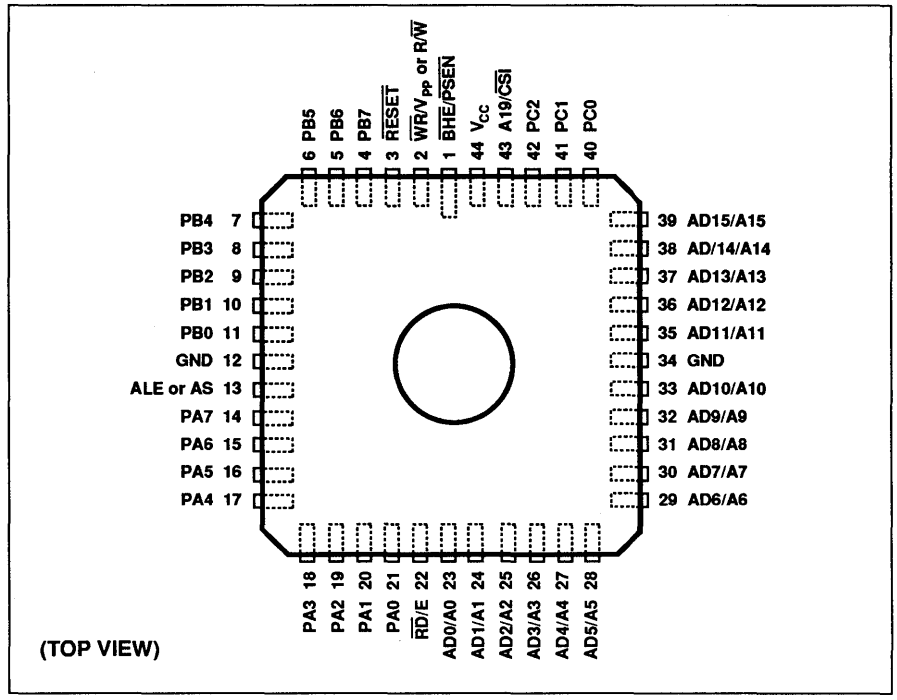


Figure 16. Drawing L4 – 44 Pin Ceramic Leaded Chip Carrier (CLCC) with Window (Package Type L)

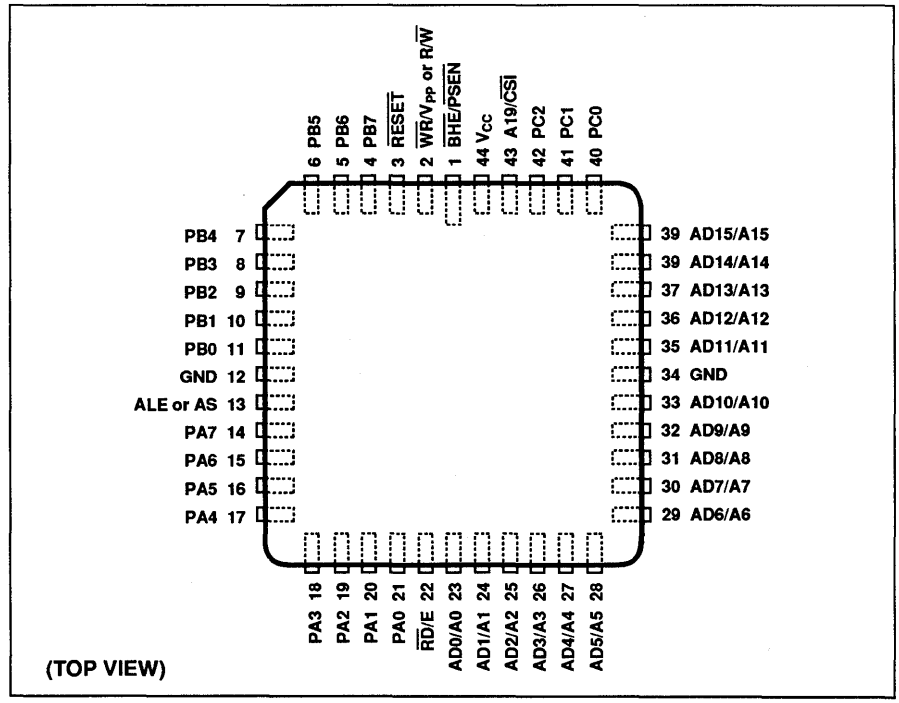


Figure 17. Drawing J2 – 44 Pin Plastic Leaded Chip Carrier (PLCC) (Package Type J)

Ordering Information

Part Number	Spd. (ns)	Package Type	Package Drawing	Operating Temperature Range	Manufacturing Procedure
PSD301L25 A	250	44-pin PLCC	J2	Commercial	Standard
PSD301L25 KA	250	44-pin CLCC	L4	Commercial	Standard
PSD301L30 A	300	44-pin PLCC	J2	Commercial	Standard
PSD301L30 KA	300	44-pin CLCC	L4	Commercial	Standard

3-volt single-chip microcontroller peripheral — PSD311L

Key Features

- ❑ Single Chip Programmable Peripheral for Microcontroller-based Applications
- ❑ 3.0 to 5.5 Volt Operation
- ❑ 19 Individually Configurable I/O pins that can be used as:
  - — Microcontroller I/O port expansion
  - — Programmable Address Decoder (PAD) I/O
  - — Latched address output
  - — Open drain or CMOS
- ❑ Two Programmable Arrays (PAD A and PAD B)
  - — Total of 40 Product Terms and up to 14 Inputs and 24 Outputs
  - — Address Decoding up to 1 Meg address space
  - — Logic replacement
- ❑ "No Glue" Microcontroller Chip-Set
  - — Built-in address latches for multiplexed address/data bus
  - — Non-multiplexed address/data bus mode
  - — 8-bit data bus width
  - — ALE and Reset polarity programmable
  - — Selectable modes for read and write control bus as $\overline{RD}/\overline{WR}$ or R/$\overline{W}$/E
  - — $\overline{PSEN}$ pin for 8051 users
- ❑ 256 Kbits of UV EPROM
  - — Organized as 32K x 8
  - — Divides into 8 equal mappable blocks for optimized mapping
  - — Block resolution is 4K x 8
  - — 250 ns EPROM access time, including input latches and PAD address decoding.
- ❑ 16 Kbit Static RAM
  - — Organized as 2K x 8
  - — 250 ns SRAM access time, including input latches and PAD address decoding
- ❑ Address/Data Track Mode
  - — Enables easy Interface to Shared Resources (e.g., Mail Box SRAM) with other Microcontrollers or a Host Processor
- ❑ Built-In Security
  - — Locks the PSD311L and PAD Decoding Configuration
- ❑ Available in a Choice of Packages
  - — 44 Pin PLDCC and CLDCC
- ❑ Simple Menu-Driven Software: Configure the PSD311L on an IBM PC
- ❑ Pin Compatible with the PSD3XX and PSD3XXL Series

Absolute Maximum Ratings[1]

Symbol	Parameter	Condition	Min	Max	Unit
T_{STG}	Storage Temperature	CERAMIC	−65	+150	°C
		PLASTIC	−65	+125	°C
T_{STG}	Storage Temperature		−65	+150	°C
	Voltage on any Pin	With Respect to GND	−0.6	+7	V
V_{PP}	Programming Supply Voltage	With Respect to GND	−0.6	+14	V
V_{CC}	Supply Voltage	With Respect to GND	−0.6	+7	V
	ESD Protection			>2000	V

NOTE: 1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods of time may affect device reliability.

Operating Range

Range	Temperature	V_{CC}
Commercial	0° C to +70°C	3.0 V to 5.5 V

Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	Supply Voltage	All Speeds	3.0	3.3	5.5	V
V_{IH}	High-level Input Voltage	V_{CC} = 3.0 V to 5.5 V	0.7 V_{CC}		V_{CC} + 0.5	V
V_{IL}	Low-level Input Voltage	V_{CC} = 3.0 V to 5.5 V	−0.5		0.2 V_{CC}*	V
					0.3 V_{CC}**	V

* Before 8/1/1993.
** After 8/1/1993.

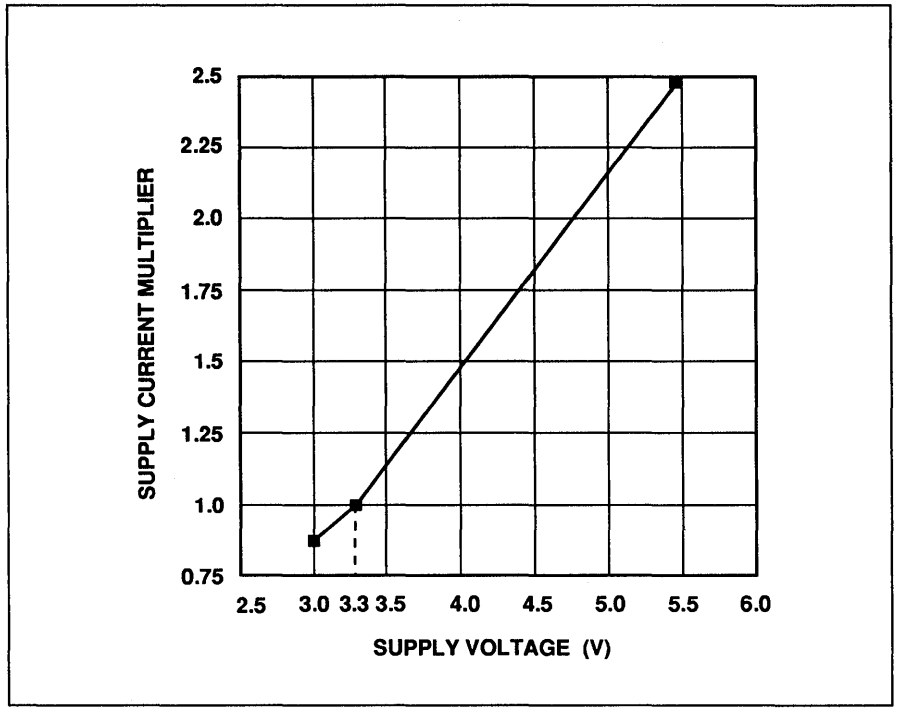
DC Characteristics

Symbol	Parameter	Conditions				CMiser = 1 Subtract:**			Unit
			Min	Typ	Max	Min	Typ	Max	
V_{OL}	Output Low Voltage	I_{OL} = 20 µA V_{CC} = 3.0 V		0.01	0.1				V
		I_{OL} = 4 mA V_{CC} = 3.0 V		0.15	0.4				V
V_{OH}	Output High Voltage	I_{OH} = –20 µA V_{CC} = 3.0 V	2.9	2.99					V
		I_{OH} = –1 mA V_{CC} = 3.0 V	2.4	2.6					V
I_{SB1}	V_{CC} Standby Current (CMOS) (Notes 2 and 3)	V_{CC} = 3.3 V		10*	25*				µA
				1**	5**				
I_{CC1}	Active Current (CMOS) (No Internal Memory Block Selected) (Notes 2 and 5)	V_{CC} = 3.3 V (Note 5)		6	12		3.0	5	mA
		V_{CC} = 3.3 V (Note 6)		10	20		3.0	5	mA
I_{CC2}	Active Current (CMOS) (EPROM Block Selected) (Notes 2 and 5)	V_{CC} = 3.3 V (Note 5)		6	12		2	3	mA
		V_{CC} = 3.3 V (Note 6)		10	20		2	3	
I_{CC3}	Active Current (CMOS) (SRAM Block Selected) (Notes 2 and 5)	V_{CC} = 3.3 V (Note 5)		20	33		5	8	mA
		V_{CC} = 3.3 V (Note 6)		24	40		5	8	mA
I_{LI}	Input Leakage Current	V_{IN} = V_{CC} or GND	–1	±0.1	1				µA
I_{LO}	Output Leakage Current	V_{OUT} = V_{CC} or GND	–10	±5	10				µA

NOTES: 2. CMOS inputs: GND ± 0.3 V or V_{CC} ± 0.3V.
3. $\overline{CSI}$/A19 is high and the part is in a power-down configuration mode.
4. Add 2.0 mA/MHz for AC power component (power = AC + DC).
5. Ten (10) PAD product terms active. (Add 190 µA per product term, typical, or 240 µA per product term maximum.)
6. Forty (40) PAD product terms active.

* Before 8/1/93.
** After 8/1/93.

Figure 1. Normalized Supply Current vs. Supply Voltage



The Normalized Supply Current vs. Supply Voltage graph shown above, provides a multiplier for any I_{SB} or I_{CC} value in the D.C. Characteristics table. As noted, it is normalized for a supply voltage of 3.3 volts. Since device characterization data shows very little supply current difference over speed, the multiplier includes all frequencies of operation from standby to quiescent to full dynamic speed. To use, calculate the supply current at 3.3 volts for your operation configuration using the D.C. Characteristics table. Then multiply that value by the Supply Current Multiplier for the supply voltage actually being used.

AC Characteristics[8] (See Timing Diagrams)

Symbol	Parameter	-25		-30		CMiser = 1 Add:**	Unit
		Min	Max	Min	Max		
T1	ALE or AS Pulse Width	75		80			ns
T2	Address Set-up Time	30		35			ns
T3	Address Hold Time	30		35		0	ns
T4	Leading Edge of Read to Data Active	0		0		0	ns
T5	ALE Valid to Data Valid		250		300	25	ns
T6	Address Valid to Data Valid		250		300	25	ns
T7	$\overline{CSI}$ Active to Data Valid		275		325	30	ns
T8	Leading Edge of Read to Data Valid		90		95	0	ns
T9	Read Data Hold Time	0		0		0	ns
T10	Trailing Edge of Read to Data High-Z		50		55	0	ns
T11	Trailing Edge of ALE or AS to Leading Edge of Write		40		45		ns
T12	$\overline{RD}$, E, $\overline{PSEN}$, $\overline{DS}$ Pulse Width	100		110		0	ns
T12A	$\overline{WR}$ Pulse Width	90		95		0	ns
T13	Trailing Edge of Write or Read to Leading Edge of ALE or AS	0		0		0	ns
T14	Address Valid to Trailing Edge of Write	250		300		0	ns
T15	$\overline{CSI}$ Active to Trailing Edge of Write	275		375		0	ns
T16	Write Data Set-up Time	60		65		0	ns
T17	Write Data Hold Time	25		30		0	ns
T18	Port to Data Out Valid Propagation Delay		70		75	0	ns
T19	Port Input Hold Time	0		0		0	ns
T20	Trailing Edge of Write to Port Output Valid	100		110		0	ns
T21	ADi or Control to $\overline{CSOi}$ Valid	6	80	5	85	0	ns
T22	ADi or Control to $\overline{CSOi}$ Invalid	4	80	4	85	0	ns
T23	Track Mode Address Propagation Delay: CSADOUT1 Already True		70		75	0	ns
T23A	Track Mode Address Propagation Delay: CSADOUT1 Becomes True During ALE or AS		100		110	0	ns

NOTE: 8. These AC Characteristics are for V_{CC} = 3.0 – 3.6V.

AC Characteristics (Cont.)

Symbol	Parameter	-25		-30		CMiser = 1 Add:**	Unit
		Min	Max	Min	Max		
T24	Track Mode Trailing Edge of ALE or AS to Address High-Z		60		65	0	ns
T25	Track Mode Read Propagation Delay		70		75	0	ns
T26	Track Mode Read Hold Time	10	70	10	75		ns
T27	Track Mode Write Cycle, Data Propagation Delay		60		65	0	ns
T28	Track Mode Write Cycle, Write to Data Propagation Delay	7	80	7	85	0	ns
T29	Hold Time of Port A Valid During Write $\overline{CSOi}$ Trailing Edge	4		4		0	ns
T30	$\overline{CSI}$ Active to $\overline{CSOi}$ Active	9	110	8	120	0	ns
T31	$\overline{CSI}$ Inactive to $\overline{CSOi}$ Inactive	9	110	8	120	0	ns
T32	Direct PAD Input as Hold Time	24		30		0	ns
T33	R/$\overline{W}$ Active to E or DS Start	60		65		0	ns
T34	E or $\overline{DS}$ End to R/$\overline{W}$	60		65		0	ns
T35	AS Inactive to E high	40		45		0	ns
T36	Address to Leading Edge of Write	50		60		0	ns

NOTES: 9. ADi = any address line.
10. $\overline{CSOi}$ = any of the chip-select output signals coming through Port B ($\overline{CS0}$–$\overline{CS7}$) or through Port C ($\overline{CS8}$–$\overline{CS10}$).
11. Direct PAD input = any of the following direct PAD input lines: $\overline{CSI}$/A19 as transparent A19, $\overline{RD}$/E/$\overline{DS}$, $\overline{WR}$ or R/$\overline{W}$, transparent PC0–PC2, ALE (or AS).
12. Control signals $\overline{RD}$/E/$\overline{DS}$ or $\overline{WR}$ or R/$\overline{W}$.

**After 8/1/1993.

Figure 2. AC Testing Input/Output Waveform

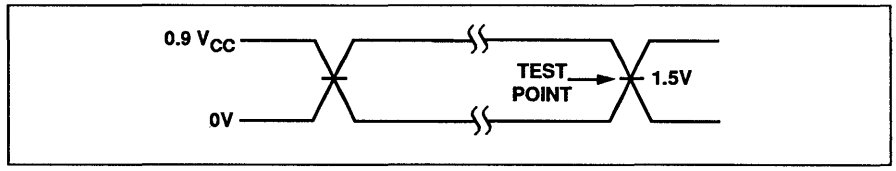


Figure 3. AC Testing Load Circuit

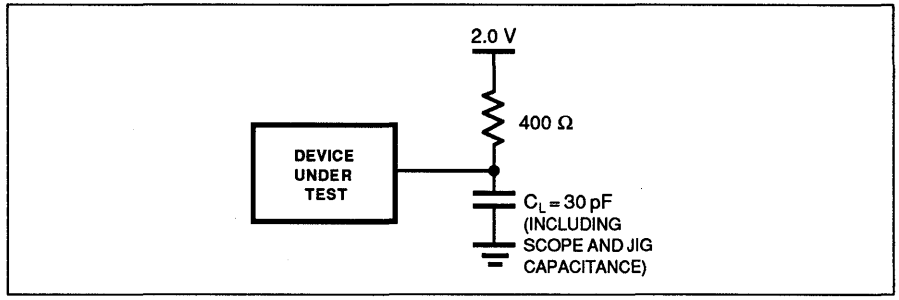


Figure 4. The Reset Cycle (RESET)

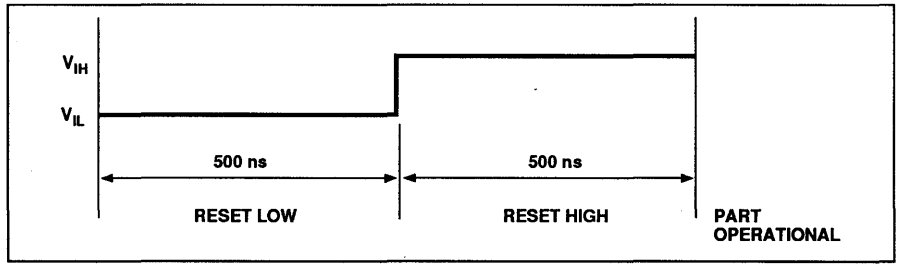
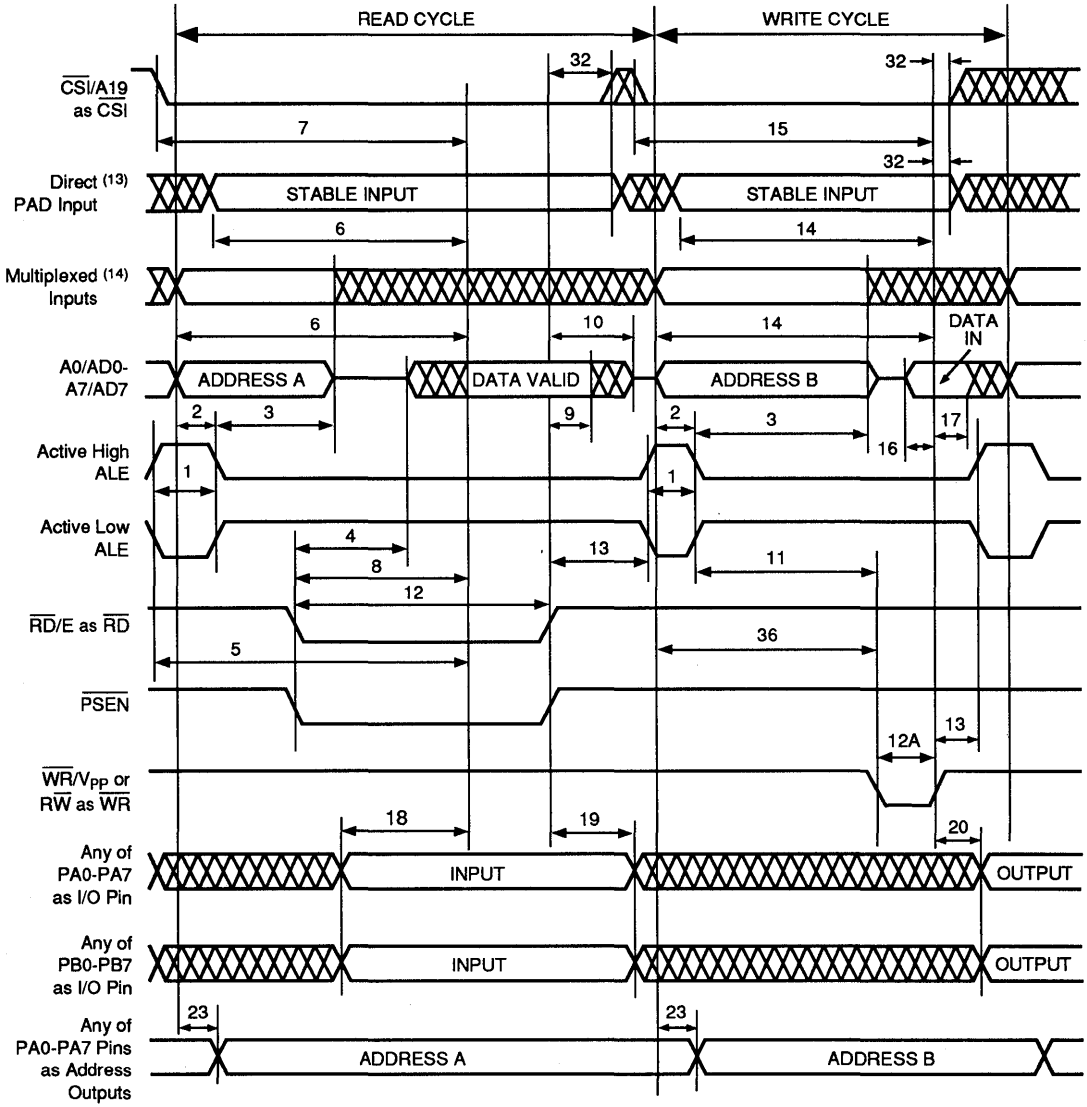
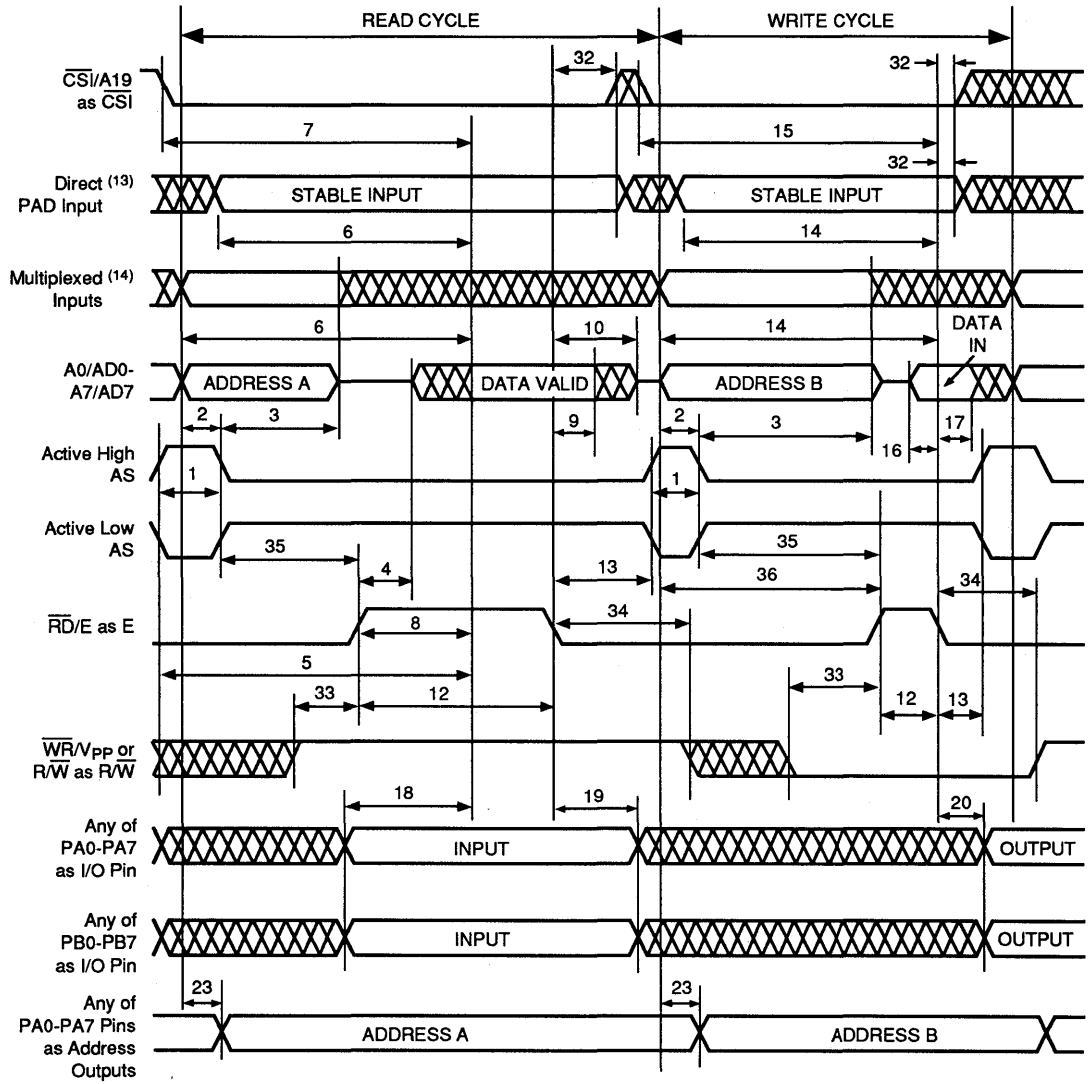


Figure 5. Timing of 8-Bit Multiplexed Address/Data Bus, CRRWR = 0



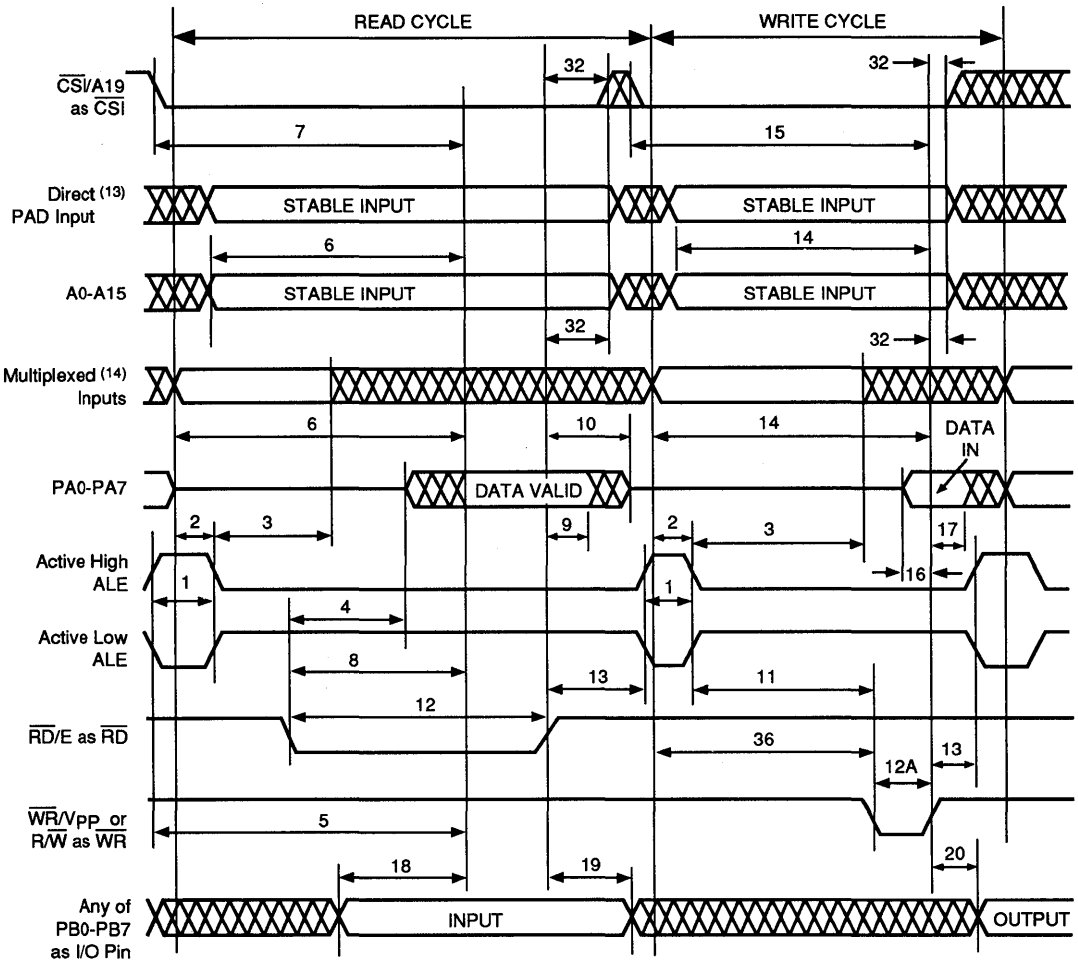
See referenced notes on page 216.

Figure 6. Timing of 8-Bit Multiplexed Address/Data Bus, CRRWR = 1



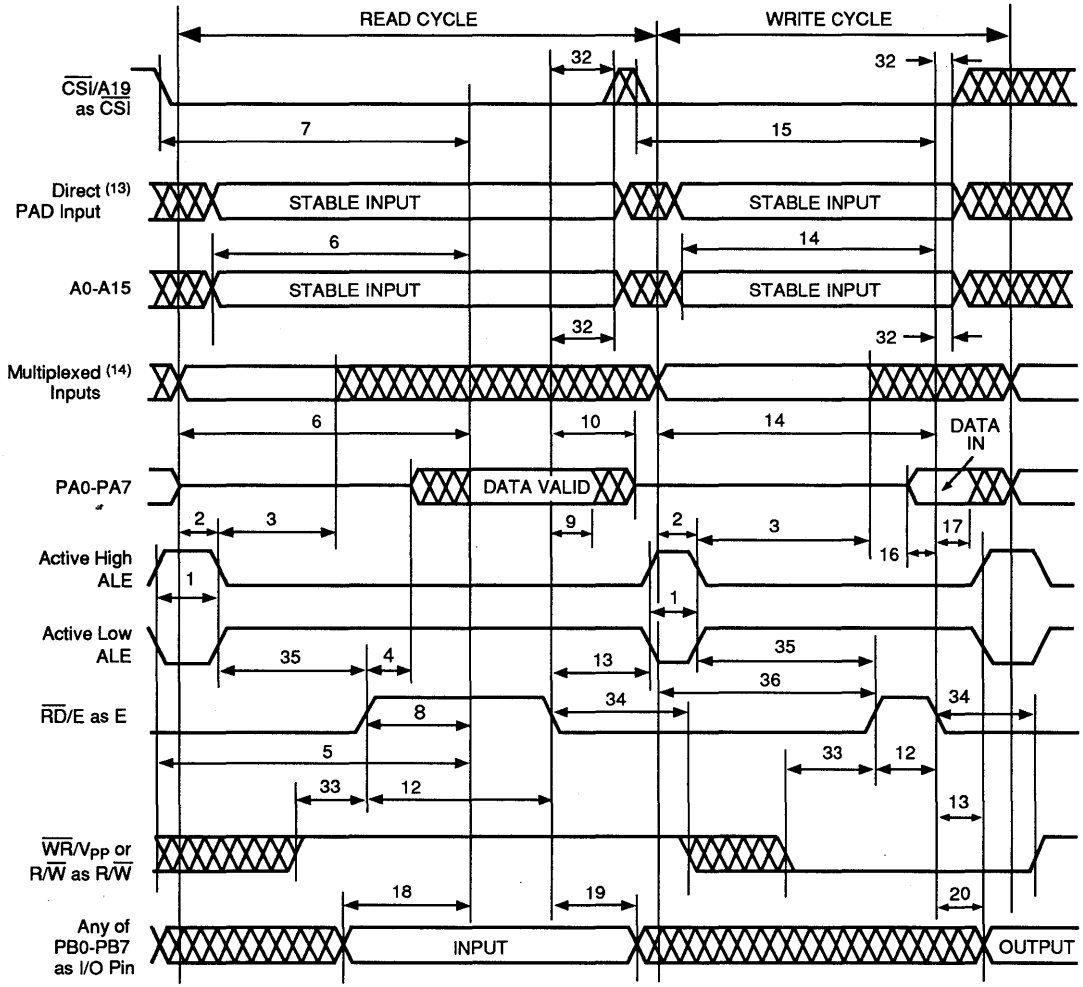
See referenced notes on page 216.

Figure 7. Timing of 8-Bit Data Non-Multiplexed Address/Data Bus, CRRWR = 0



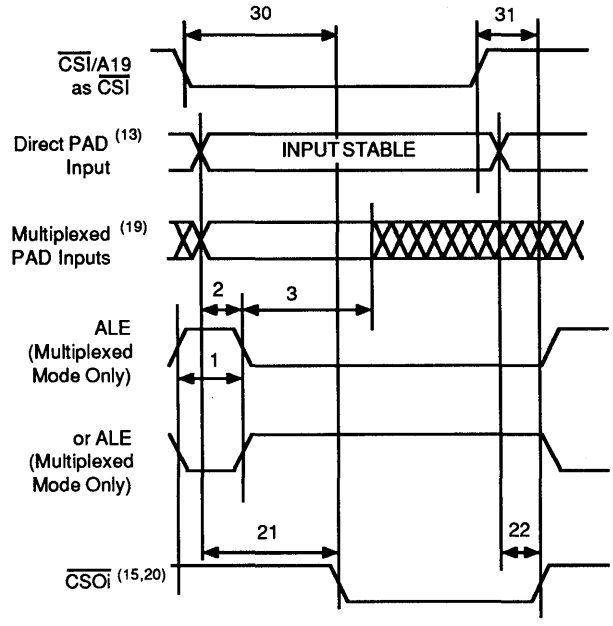
See referenced notes on page 216.

Figure 8. Timing of 8-Bit Data Non-Multiplexed Address/Data Bus, CRRWR = 1



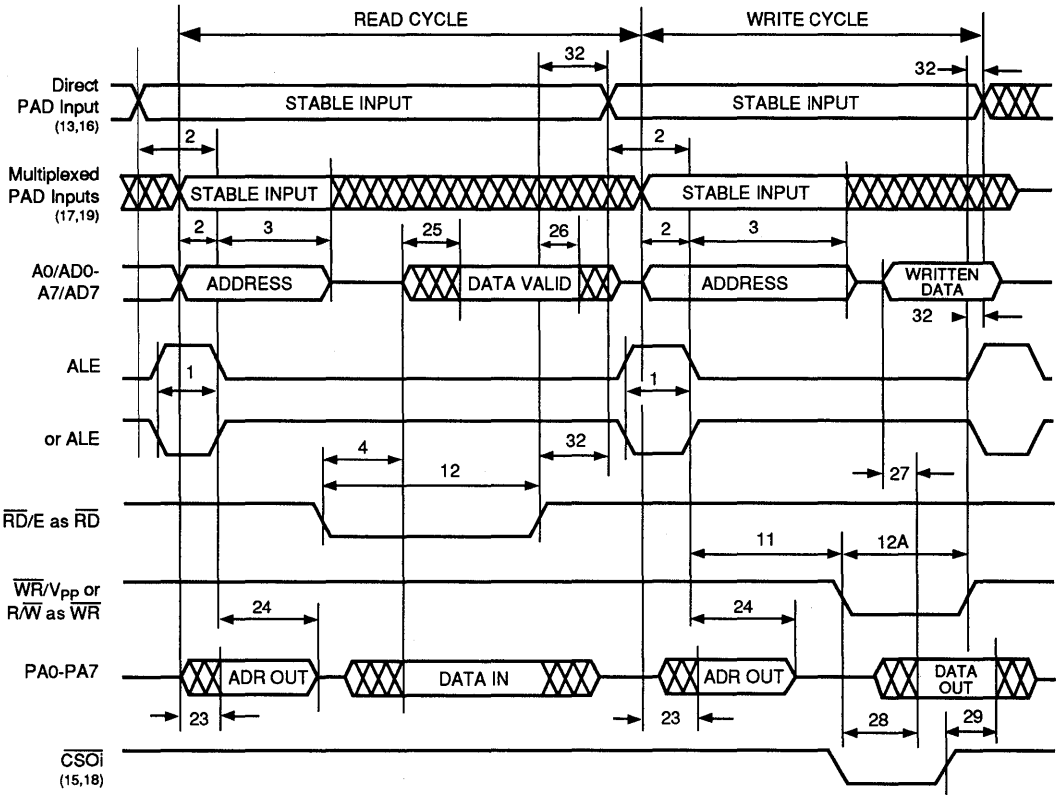
See referenced notes on page 216.

Figure 9. Chip-Select Output Timing



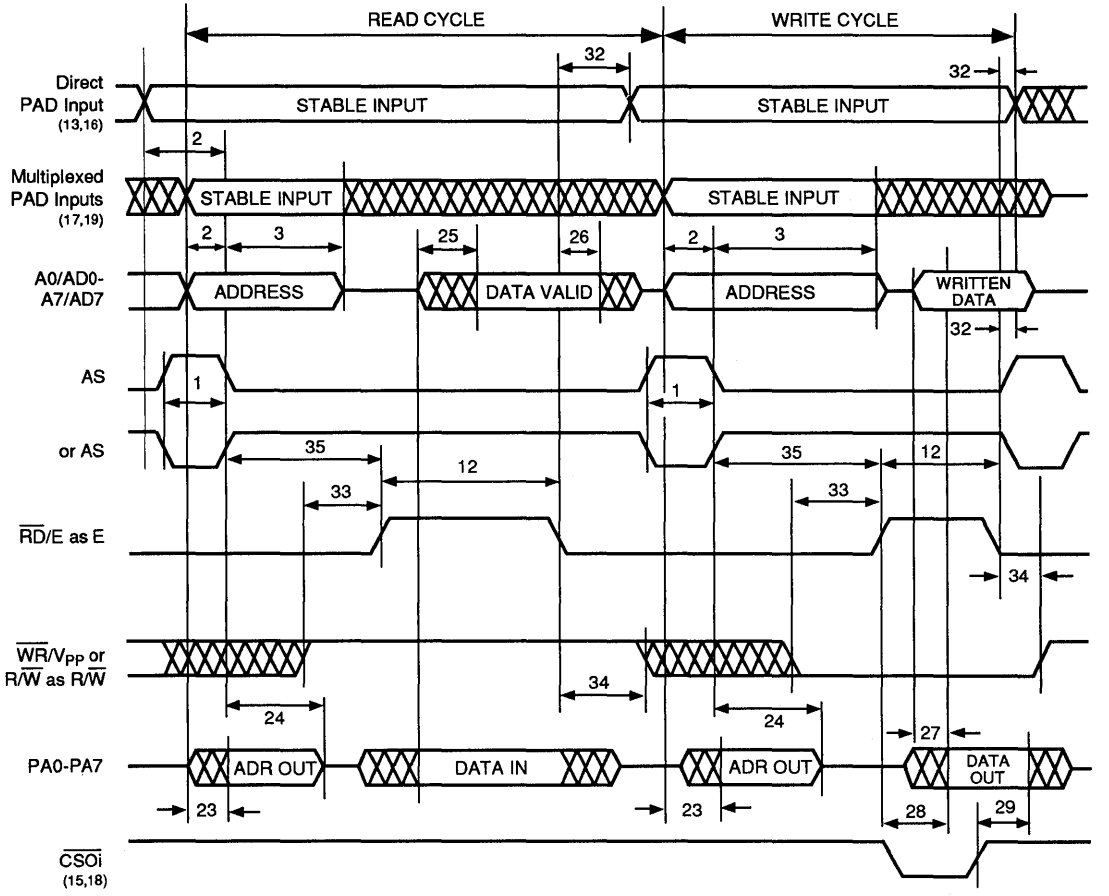
See referenced notes on page 216.

Figure 10. Port A as AD0 – AD7 Timing (Track Mode), CRRWR = 0



See referenced notes on page 216.

Figure 11. Port A as AD0 – AD7 Timing (Track Mode), CRRWR = 1



Notes for Timing Diagrams

13. Direct PAD input = any of the following direct PAD input lines: $\overline{CSI}$/A19 as transparent A19, $\overline{RD}$/E/$\overline{DS}$, $\overline{WR}$ or R/$\overline{W}$, transparent PC0–PC2, ALE in non-multiplexed modes.
14. Multiplexed inputs: any of the following inputs that are latched by the ALE (or AS): A0/AD0–A15/AD15, $\overline{CSI}$/A19 as ALE dependent A19, ALE dependent PC0–PC2.
15. $\overline{CSOi}$ = any of the chip-select output signals coming through Port B ($\overline{CS0}$–$\overline{CS7}$) or through Port C ($\overline{CS8}$–$\overline{CS10}$).
16. CSADOUT1, which internally enables the address transfer to Port A, should be derived only from direct PAD input signals, otherwise the address propagation delay is slowed down.
17. CSADIN and CSADOUT2, which internally enable the data-in or data-out transfers, respectively, can be derived from any combination of direct PAD inputs and multiplexed PAD inputs.
18. The write operation signals are included in the $\overline{CSOi}$ expression.
19. Multiplexed PAD inputs: any of the following PAD inputs that are latched by the ALE (or AS) in the multiplexed modes: A11/AD11–A15/AD15, $\overline{CSI}$/A19 as ALE dependent A19, ALE dependent PC0–PC2.
20. $\overline{CSOi}$ product terms can include any of the PAD input.signals except for reset and $\overline{CSI}$.

Pin Capacitance[21]

$T_A = 25\,°C, f = 1\,MHz$

Symbol	Parameter	Conditions	Typical[22]	Max	Unit
C_{IN}	Capacitance (for input pins only)	$V_{IN} = 0$ V	4	6	pF
C_{OUT}	Capacitance (for input/output pins)	$V_{OUT} = 0$ V	8	12	pF
C_{VPP}	Capacitance (for $\overline{WR}/V_{PP}$ or $R/\overline{W}/V_{PP}$)	$V_{PP} = 0$ V	18	25	pF

NOTES: 21. This parameter is only sampled and is not 100% tested.
22. Typical values are for $T_A = 25°C$ and nominal supply voltages.

Erasure and Programming

To clear all locations of their programmed contents, expose the device to ultra-violet light source. A dosage of 15 W second/cm² is required. This dosage can be obtained with exposure to a wavelength of 2537 Å and intensity of 12000 µW/cm² for 15 to 20 minutes. The device should be about 1 inch from the source, and all filters should be removed from the UV light source prior to erasure.

The PSD311L and similar devices will erase with light sources having wavelengths shorter than 4000 Å. Although the erasure times will be much longer than with UV sources at 2537 Å, exposure to fluorescent light and sunlight eventually erases the device. For maximum system reliability, these sources should be avoided. If used in such an environment, the package windows should be covered by an opaque substance.

Upon delivery, or after each erasure, the PSD311L device has all bits in the PAD and EPROM in the "1" or high state. The configuration bits are in the "0" or low state. The code, configuration, and PAD MAP data are loaded through the procedure of programming

Pin Assignments

Pin Name	44-Pin PLCC/CLCC Package
$\overline{PSEN}$	1
$\overline{WR}/V_{PP}$ or R/$\overline{W}$	2
$\overline{RESET}$	3
PB7	4
PB6	5
PB5	6
PB4	7
PB3	8
PB2	9
PB1	10
PB0	11
GND	12
ALE or AS	13
PA7	14
PA6	15
PA5	16
PA4	17
PA3	18
PA2	19
PA1	20
PA0	21
$\overline{RD}$/E	22
AD0/A0	23
AD1/A1	24
AD2/A2	25
AD3/A3	26
AD4/A4	27
AD5/A5	28
AD6/A6	29
AD7/A7	30
A8	31
A9	32
A10	33
GND	34
A11	35
A12	36
A13	37
A14	38
A15	39
PC0	40
PC1	41
PC2	42
A19/$\overline{CSI}$	43
V_{CC}	44

Package Information

Figure 12. Drawing L4 — 44 Pin Ceramic Leaded Chip Carrier (CLCC) with Window (Package Type L)

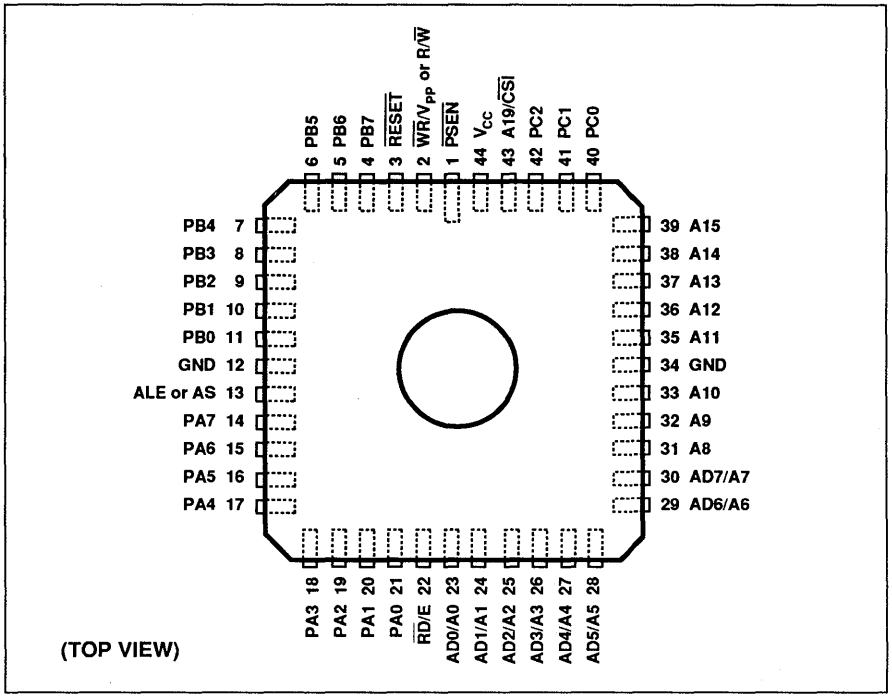
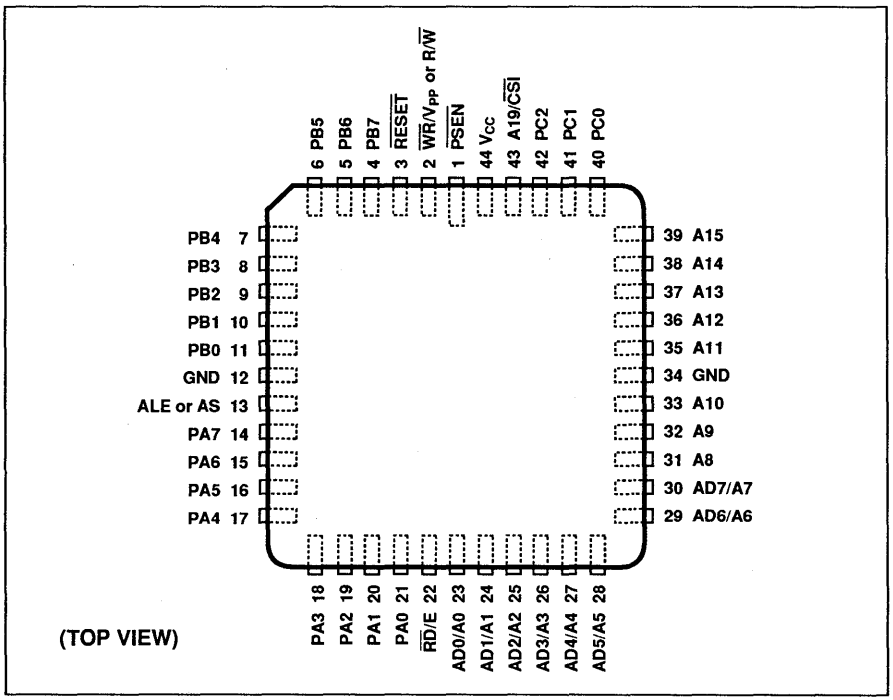


Figure 13. Drawing J2 — 44 Pin Plastic Leaded Chip Carrier (PLCC) (Package Type J)



Ordering Information

Part Number	Spd. (ns)	Package Type	Package Drawing	Operating Temperature Range	Manufacturing Procedure
PSD311L25 A	250	44-pin PLDCC	J2	Commercial	Standard
PSD311L25 KA	250	44-pin CLDCC	L4	Commercial	Standard
PSD311L30 A	300	44-pin PLDCC	J2	Commercial	Standard
PSD311L30 KA	300	44-pin CLDCC	L4	Commercial	Standard

3-volt single-chip microcontroller peripheral — PSD302L

Key Features

- ❑ Single Chip Programmable Peripheral for Microcontroller-based Applications
- ❑ 3.0 to 5.5 Volt Operation
- ❑ 19 Individually Configurable I/O pins that can be used as:
  - — Microcontroller I/O port expansion
  - — Programmable Address Decoder (PAD) I/O
  - — Latched address output
  - — Open drain or CMOS
- ❑ Two Programmable Arrays (PAD A & PAD B)
  - — Total of 40 Product Terms and up to 18 Inputs and 24 Outputs
  - — Direct Address Decoding up to 1 Meg address space and up to 16 Meg with paging
  - — Logic replacement
- ❑ "No Glue" Microcontroller Chip-Set
  - — Built-in address latches for multiplexed address/data bus
  - — Non-multiplexed address/data bus mode
  - — Selectable 8 or 16 bit data bus width
  - — ALE and Reset polarity programmable
  - — Selectable modes for read and write control bus as $\overline{RD}/\overline{WR}$, R/$\overline{W}$/E, or R/$\overline{W}$/$\overline{DS}$
  - — $\overline{BHE}$ pin for byte select in 16-bit mode
  - — $\overline{PSEN}$ pin for 8051 users
- ❑ Built-In Page Logic
  - — To Expand the Address Space of Microcontrollers with Limited Address Space Capabilities
  - — Up to 16 pages
- ❑ 512 Kbits of UV EPROM
  - — Configurable as 64K x 8 or as 32K x 16
  - — Divides into 8 equal mappable blocks for optimized mapping
  - — Block resolution is 8K x 8 or 4K x 16
  - — 250 ns EPROM access time, including input latches and PAD address decoding.
- ❑ 16 Kbit Static RAM
  - — Configurable as 2K x 8 or as 1K x 16
  - — 250 ns SRAM access time, including input latches and PAD address decoding
- ❑ Address/Data Track Mode
  - — Enables easy Interface to Shared Resources (e.g., Mail Box SRAM) with other Microcontrollers or a Host Processor
- ❑ CMiser-Bit
  - — Programmable option to further reduce power consumption
- ❑ Built-In Security
  - — Locks the PSD302L and PAD Decoding Configuration
- ❑ Available in a Choice of Packages
  - — 44 Pin PLDCC and CLDCC
- ❑ Simple Menu-Driven Software: Configure the PSD302L on an IBM PC
- ❑ Pin and Functionally Compatible with the PSD3XX and PSD3XXL Series

Absolute Maximum Ratings[1]

Symbol	Parameter	Condition	Min	Max	Unit
T_{STG}	Storage Temperature	CERAMIC	– 65	+ 150	°C
		PLASTIC	– 65	+ 125	°C
T_{STG}	Storage Temperature		– 65	+ 150	°C
	Voltage on any Pin	With Respect to GND	– 0.6	+ 7	V
V_{PP}	Programming Supply Voltage	With Respect to GND	– 0.6	+ 14	V
V_{CC}	Supply Voltage	With Respect to GND	– 0.6	+ 7	V
	ESD Protection			>2000	V

NOTE: 1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods of time may affect device reliability.

Operating Range

Range	Temperature	V_{CC}
Commercial	0° C to +70°C	3.0 V to 5.5 V

Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	Supply Voltage	All Speeds	3.0	3.3	5.5	V
V_{IH}	High-level Input Voltage	V_{CC} = 3.0 V to 5.5 V	0.7 V_{CC}		V_{CC} + 0.5	V
V_{IL}	Low-level Input Voltage	V_{CC} = 3.0 V to 5.5 V	– 0.5		0.2 V_{CC}*	V
					0.3 V_{CC}**	V

* Before 8/1/1993.
**After 8/1/1993.

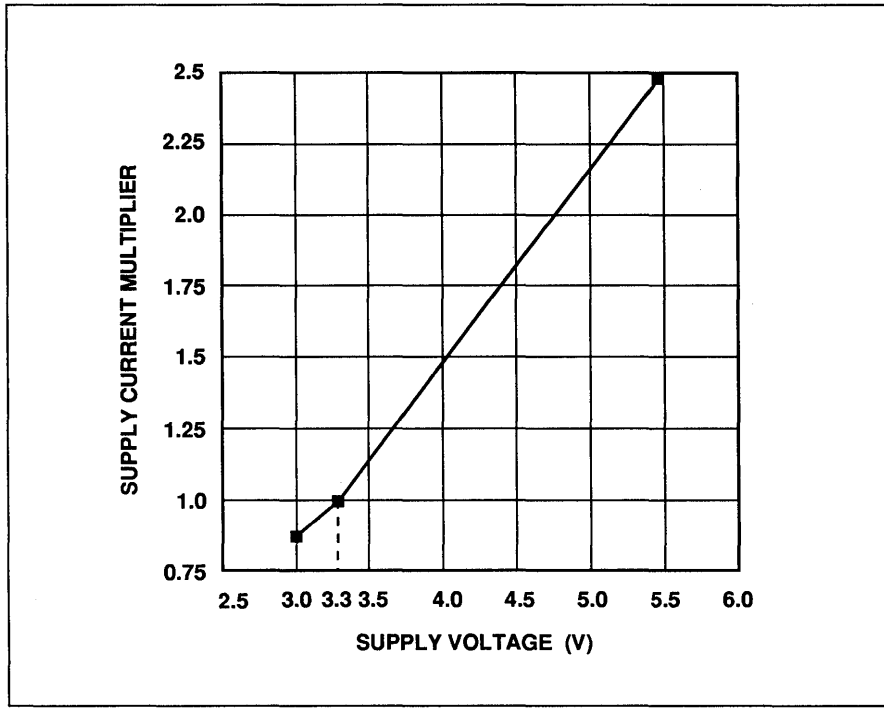
DC Characteristics

Symbol	Parameter	Conditions				CMiser = 1 Subtract:			Unit
			Min	Typ	Max	Min	Typ	Max	
V_{OL}	Output Low Voltage	I_{OL} = 20 µA V_{CC} = 3.0 V		0.01	0.1				V
		I_{OL} = 4 mA V_{CC} = 3.0 V		0.15	0.4				V
V_{OH}	Output High Voltage	I_{OH} = –20 µA V_{CC} = 3.0 V	2.9	2.99					V
		I_{OH} = –1 mA V_{CC} = 3.0 V	2.4	2.6					V
I_{SB1}	V_{CC} Standby Current (CMOS) (Notes 2 and 3)	V_{CC} = 3.3 V		10*	25*				µA
				1**	5**				
I_{CC1}	Active Current (CMOS) (No Internal Memory Block Selected) (Notes 2 and 5)	V_{CC} = 3.3 V (Note 5)		6	12		3.0	5	mA
		V_{CC} = 3.3 V (Note 6)		10	20		3.0	5	mA
I_{CC2}	Active Current (CMOS) (EPROM Block Selected) (Notes 2 and 5)	V_{CC} = 3.3 V (Notes 5 and 7)		6	12		0	0	mA
		V_{CC} = 3.3 V (Note 6 and 7)		10	20		0	0	mA
I_{CC3}	Active Current (CMOS) (SRAM Block Selected) (Notes 2 and 5)	V_{CC} = 3.3 V (Note 5 and 7)		20	33		3	5	mA
		V_{CC} = 3.3 V (Notes 6 and 7)		24	40		3	5	mA
I_{LI}	Input Leakage Current	V_{IN} = V_{CC} or GND	–1	±0.1	1				µA
I_{LO}	Output Leakage Current	V_{OUT} = V_{CC} or GND	–10	±5	10				µA

NOTES: 2. CMOS inputs: GND ± 0.3 V or V_{CC} ± 0.3V.
3. $\overline{CSI}$/A19 is high and the part is in a power-down configuration mode.
4. Add 2.0 mA/MHz for AC power component (power = AC + DC).
5. Ten (10) PAD product terms active. (Add 190 µA per product term, typical, or 240 µA per product term maximum.)
6. Forty (40) PAD product terms active.
7. In 8-bit mode, an additional 3 mA Max. can be saved under CMiser.

* Before 8/1/1993.
** After 8/1/1993.

Figure 1. Normalized Supply Current vs. Supply Voltage



The Normalized Supply Current vs. Supply Voltage graph shown above, provides a multiplier for any I_{SB} or I_{CC} value in the D.C. Characteristics table. As noted, it is normalized for a supply voltage of 3.3 volts. Since device characterization data shows very little supply current difference over speed, the multiplier includes all frequencies of operation from standby to quiescent to full dynamic speed. To use, calculate the supply current at 3.3 volts for your operation configuration using the D.C. Characteristics table. Then multiply that value by the Supply Current Multiplier for the supply voltage actually being used.

AC Characteristics[8] (See Timing Diagrams)

Symbol	Parameter	-25		-30		CMiser = 1 Add:	Unit
		Min	Max	Min	Max		
T1	ALE or AS Pulse Width	75		80			ns
T2	Address Set-up Time	30		35			ns
T3	Address Hold Time	30		35		0	ns
T4	Leading Edge of Read to Data Active	0		0		0	ns
T5	ALE Valid to Data Valid		250		300	25	ns
T6	Address Valid to Data Valid		250		300	25	ns
T7	$\overline{CSI}$ Active to Data Valid		275		325	30	ns
T8	Leading Edge of Read to Data Valid		90		95	0	ns
T9	Read Data Hold Time	0		0		0	ns
T10	Trailing Edge of Read to Data High-Z		50		55	0	ns
T11	Trailing Edge of ALE or AS to Leading Edge of Write		40		45		ns
T12	$\overline{RD}$, E, $\overline{PSEN}$, $\overline{DS}$ Pulse Width	100		110		0	ns
T12A	$\overline{WR}$ Pulse Width	90		95		0	ns
T13	Trailing Edge of Write or Read to Leading Edge of ALE or AS	0		0		0	ns
T14	Address Valid to Trailing Edge of Write	250		300		0	ns
T15	$\overline{CSI}$ Active to Trailing Edge of Write	275		375		0	ns
T16	Write Data Set-up Time	60		65		0	ns
T17	Write Data Hold Time	25		30		0	ns
T18	Port to Data Out Valid Propagation Delay		70		75	0	ns
T19	Port Input Hold Time	0		0		0	ns
T20	Trailing Edge of Write to Port Output Valid	100		110		0	ns
T21	ADi or Control to $\overline{CSOi}$ Valid	6	80	5	85	0	ns
T22	ADi or Control to $\overline{CSOi}$ Invalid	4	80	4	85	0	ns
T23	Track Mode Address Propagation Delay: CSADOUT1 Already True		70		75	0	ns
T23A	Track Mode Address Propagation Delay: CSADOUT1 Becomes True During ALE or AS		100		110	0	ns

NOTE: 8. These AC Characteristics are for V_{CC} = 3.0 – 3.6V.

AC Characteristics (Cont.)

Symbol	Parameter	-25		-30		CMiser = 1 Add:	Unit
		Min	Max	Min	Max		
T24	Track Mode Trailing Edge of ALE or AS to Address High-Z		60		65	0	ns
T25	Track Mode Read Propagation Delay		70		75	0	ns
T26	Track Mode Read Hold Time	10	70	10	75		ns
T27	Track Mode Write Cycle, Data Propagation Delay		60		65	0	ns
T28	Track Mode Write Cycle, Write to Data Propagation Delay	7	80	7	85	0	ns
T29	Hold Time of Port A Valid During Write $\overline{CSOi}$ Trailing Edge	4		4		0	ns
T30	$\overline{CSI}$ Active to $\overline{CSOi}$ Active	9	110	8	120	0	ns
T31	$\overline{CSI}$ Inactive to $\overline{CSOi}$ Inactive	9	110	8	120	0	ns
T32	Direct PAD Input as Hold Time	24		30		0	ns
T33	R/$\overline{W}$ Active to E or $\overline{DS}$ Start	60		65		0	ns
T34	E or $\overline{DS}$ End to R/$\overline{W}$	60		65		0	ns
T35	AS Inactive to E high	40		45		0	ns
T36	Address to Leading Edge of Write	50		60		0	ns

NOTES:
9. ADi = any address line.
10. $\overline{CSOi}$ = any of the chip-select output signals coming through Port B ($\overline{CS0}$–$\overline{CS7}$) or through Port C ($\overline{CS8}$–$\overline{CS10}$).
11. Direct PAD input = any of the following direct PAD input lines: $\overline{CSI}$/A19 as transparent A19, $\overline{RD}$/E/$\overline{DS}$, $\overline{WR}$ or R/$\overline{W}$, transparent PC0–PC2, ALE (or AS).
12. Control signals $\overline{RD}$/E/$\overline{DS}$ or $\overline{WR}$ or R/$\overline{W}$.

Figure 2. AC Testing Input/Output Waveform

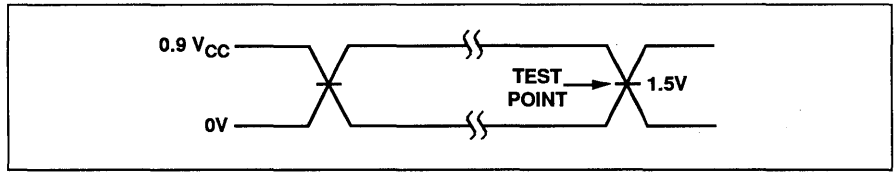


Figure 3. AC Testing Load Circuit

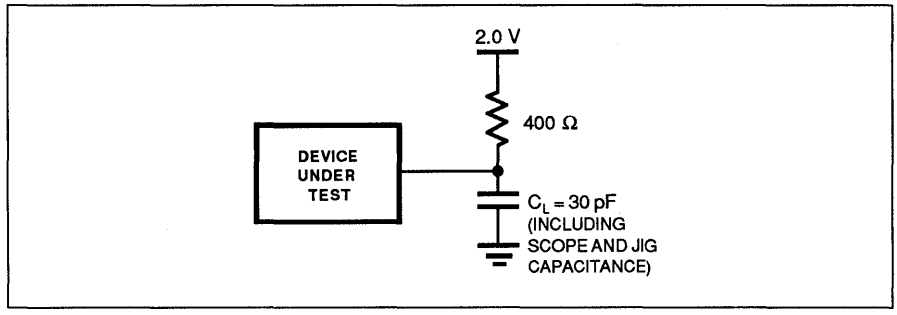


Figure 4. The Reset Cycle (RESET)

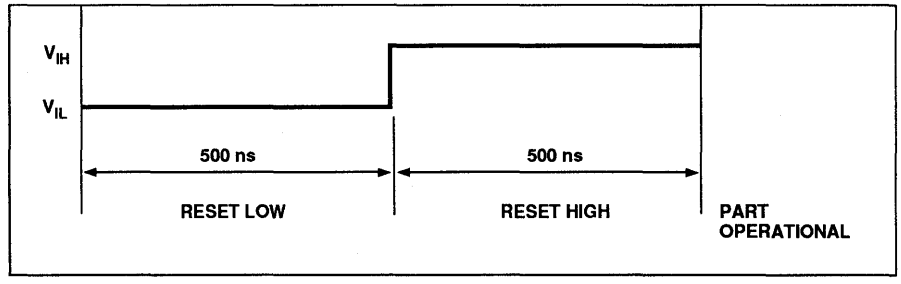
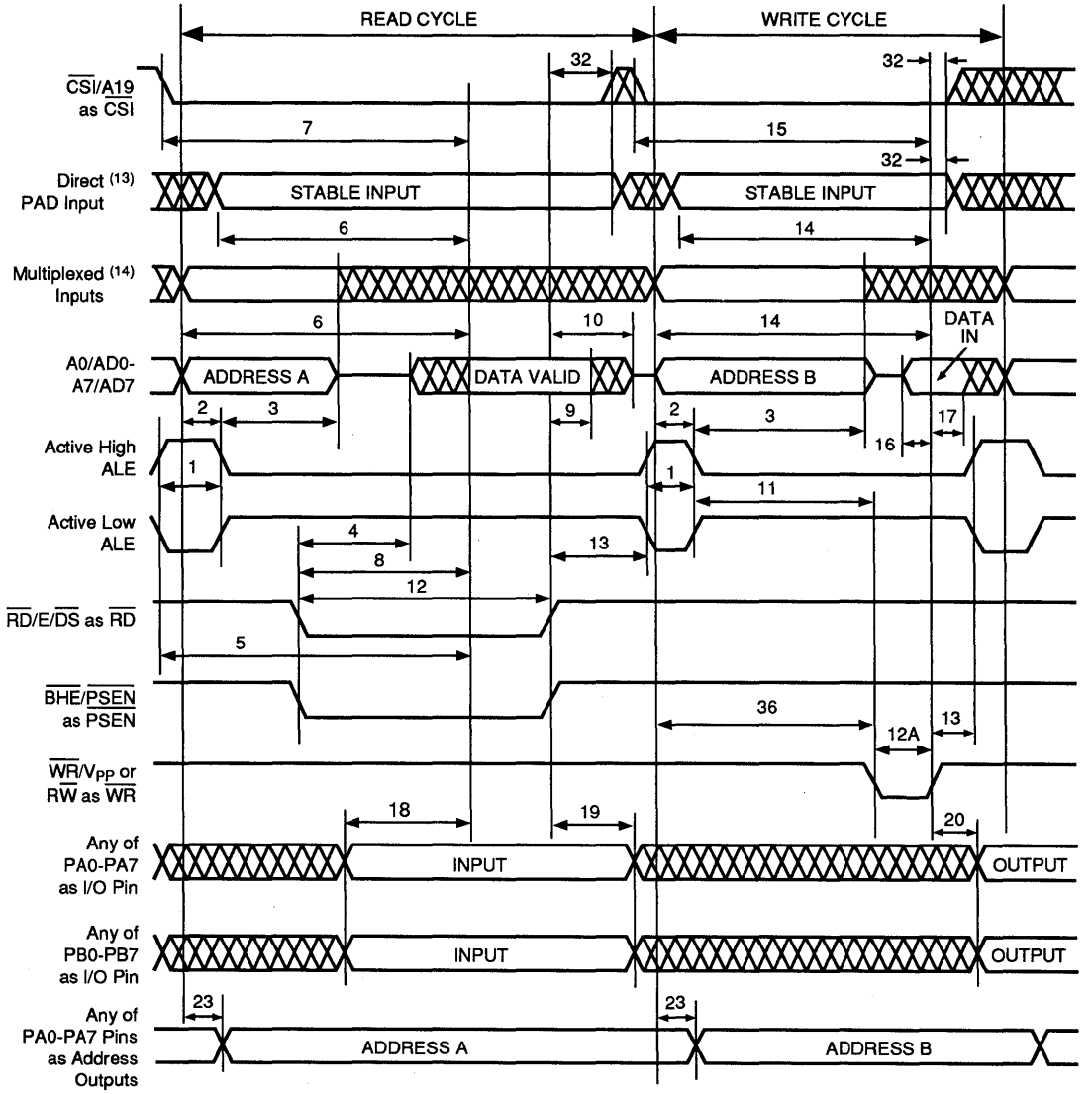
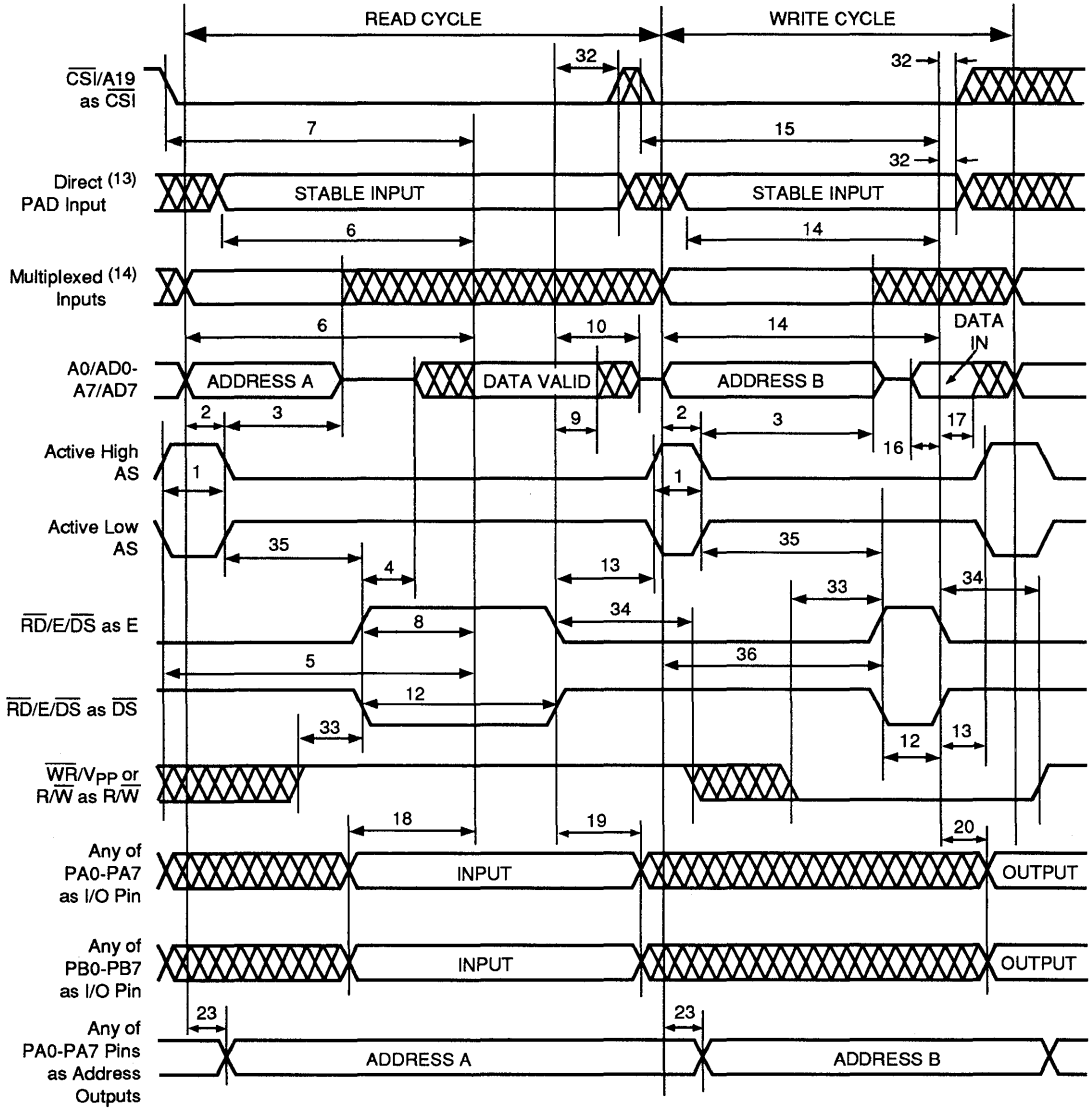


Figure 5. Timing of 8-Bit Multiplexed Address/Data Bus, CRRWR = 0



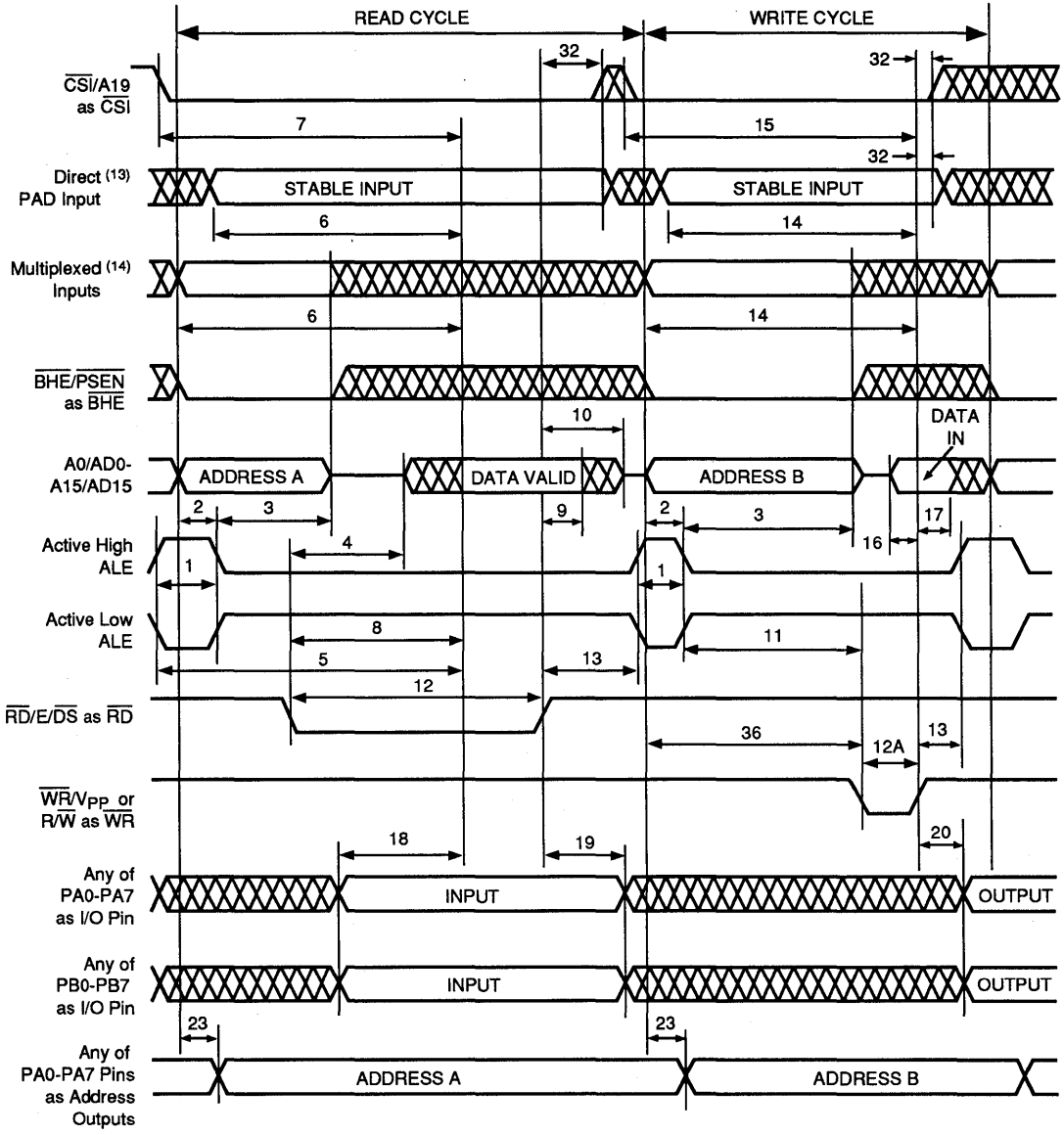
See referenced notes on page 238.

Figure 6. Timing of 8-Bit Multiplexed Address/Data Bus, CRRWR = 1



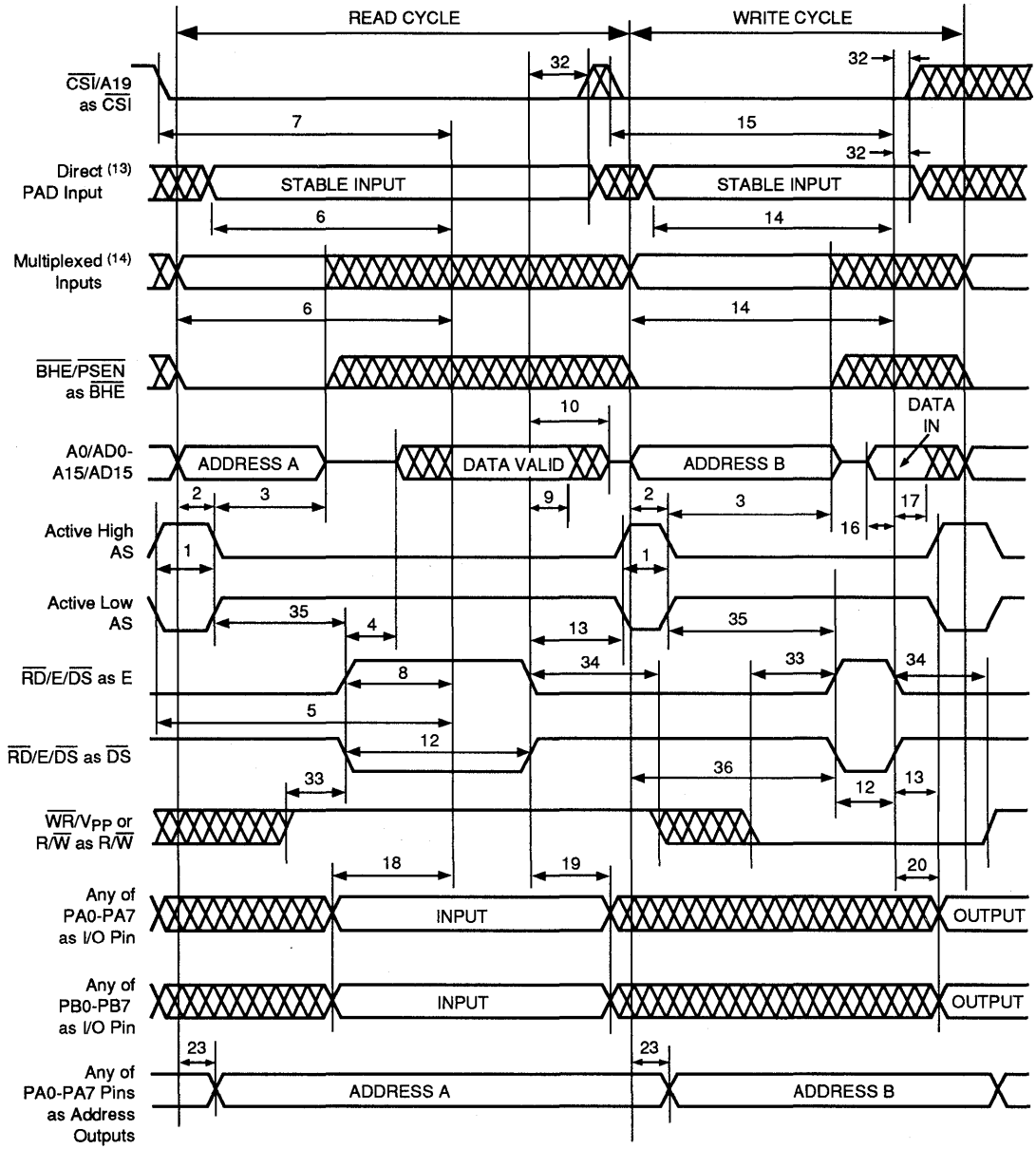
See referenced notes on page 238.

Figure 7. Timing of 16-Bit Multiplexed Address/Data Bus, CRRWR = 0



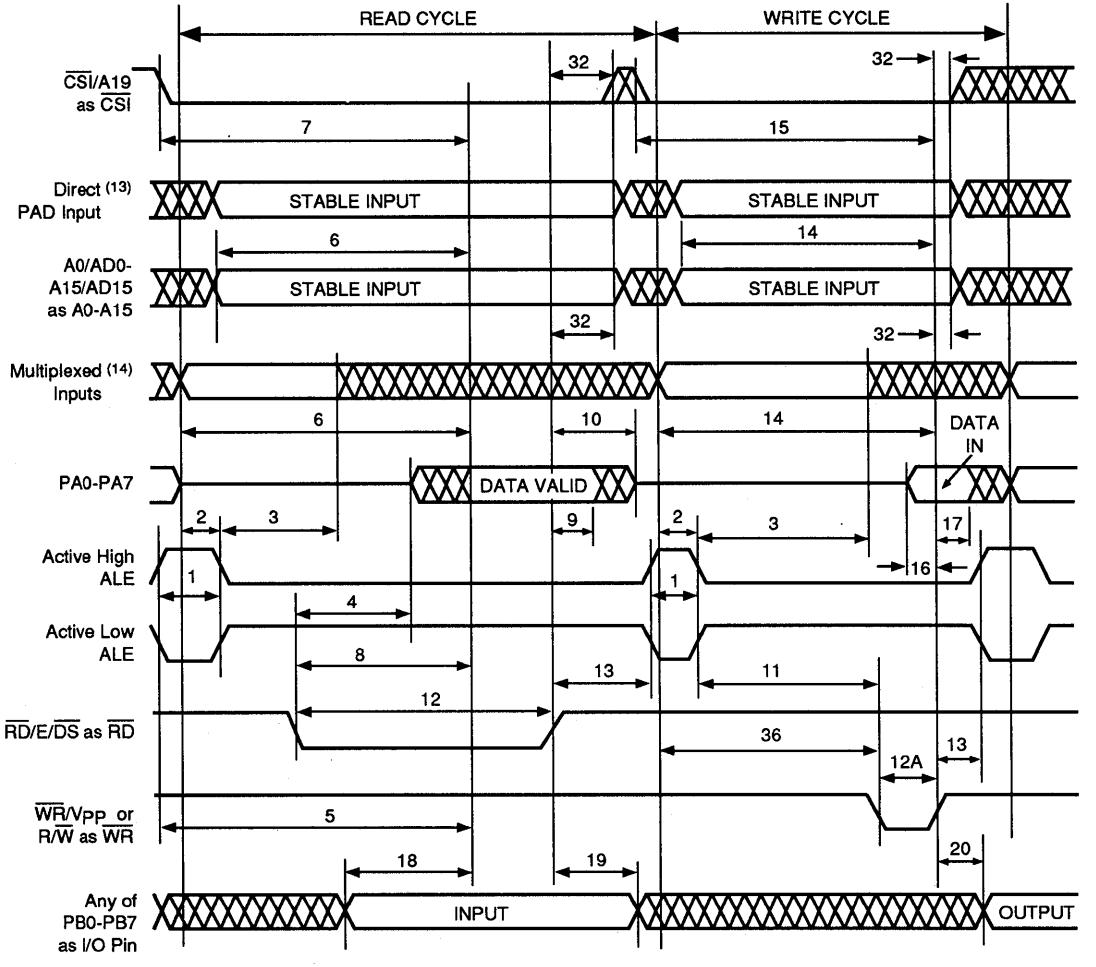
See referenced notes on page 238.

Figure 8. Timing of 16-Bit Multiplexed Address/Data Bus, CRRWR = 1



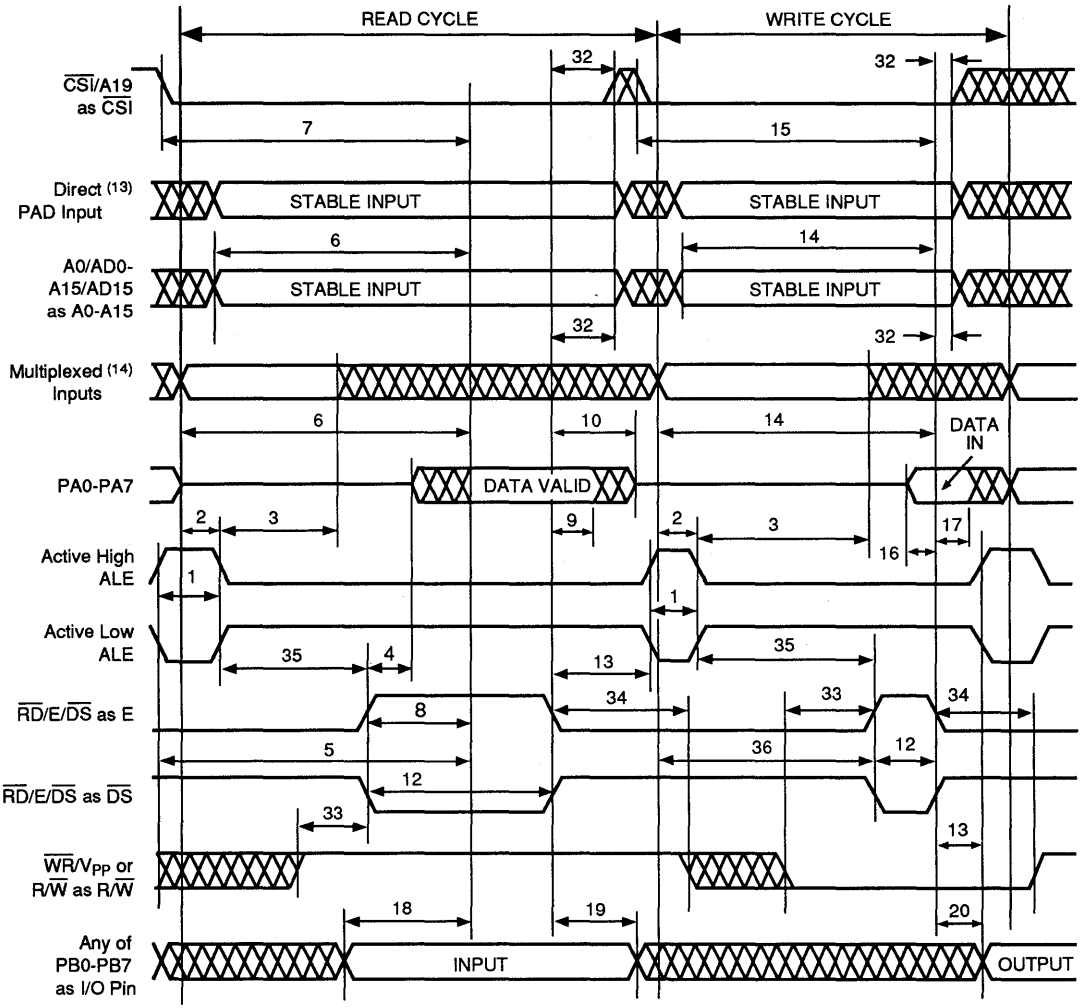
See referenced notes on page 238.

Figure 9. Timing of 8-Bit Data Non-Multiplexed Address/Data Bus, CRRWR = 0



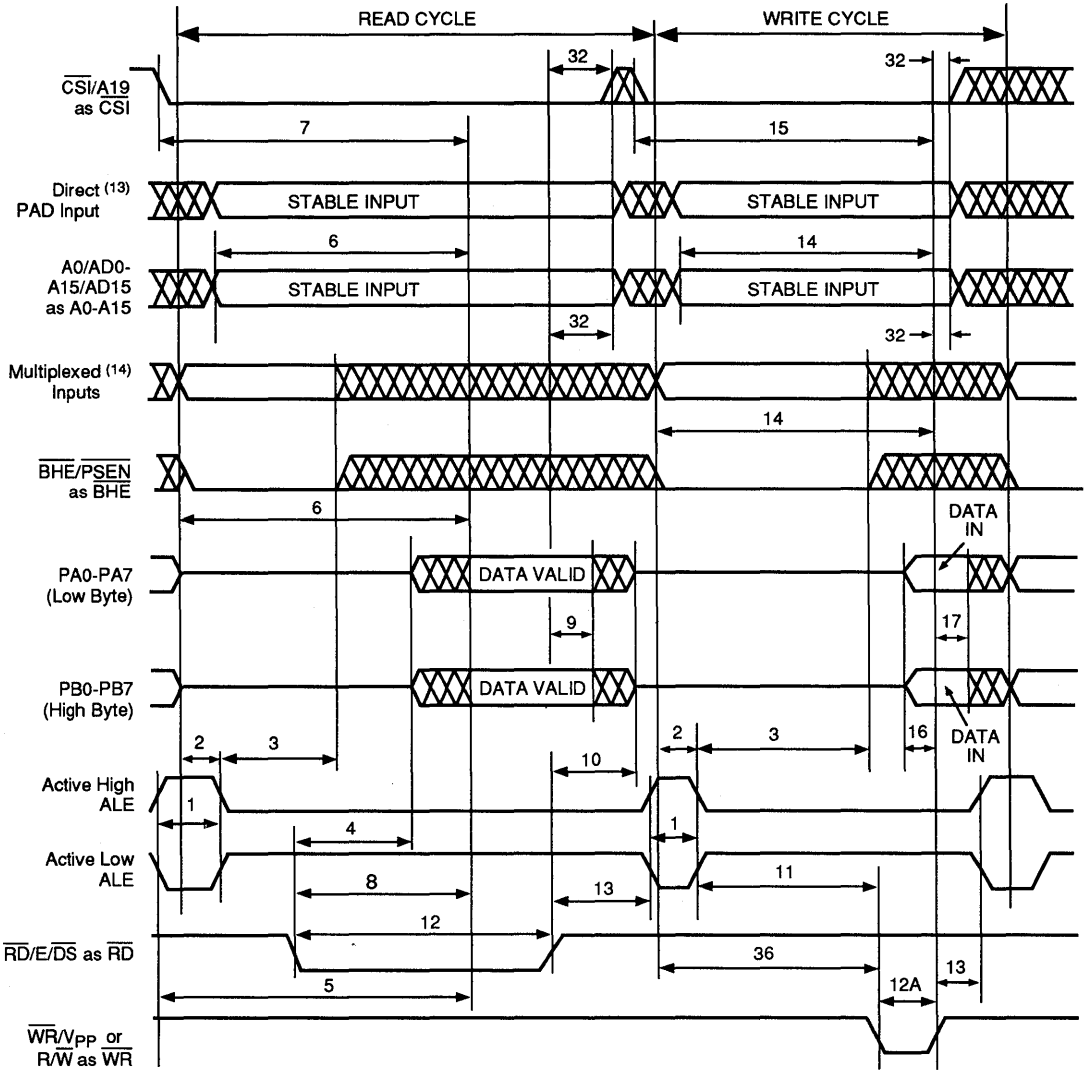
See referenced notes on page 238.

Figure 10. Timing of 8-Bit Data Non-Multiplexed Address/Data Bus, CRRWR = 1



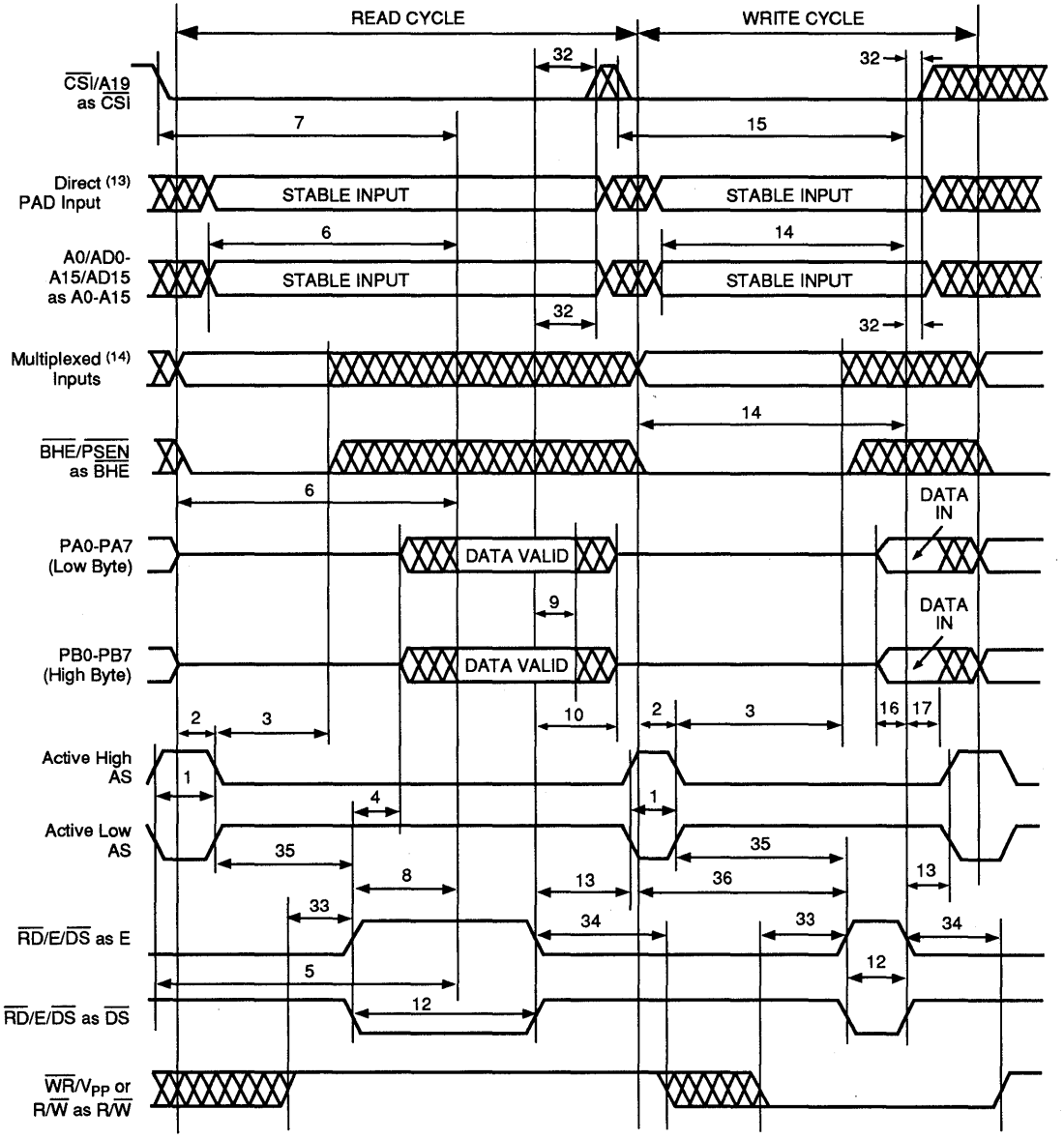
See referenced notes on page 238.

Figure 11. Timing of 16-Bit Non-Multiplexed Address/Data Bus, CRRWR = 0



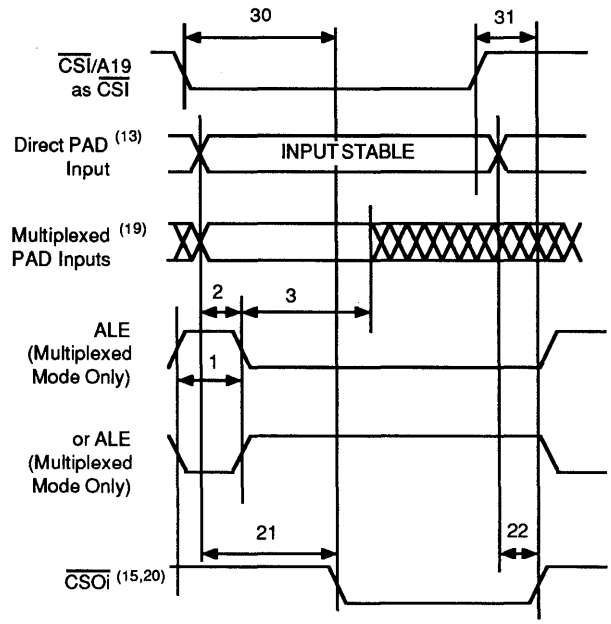
See referenced notes on page 238.

Figure 12. Timing of 16-Bit Non-Multiplexed Address/Data Bus, CRRWR = 1



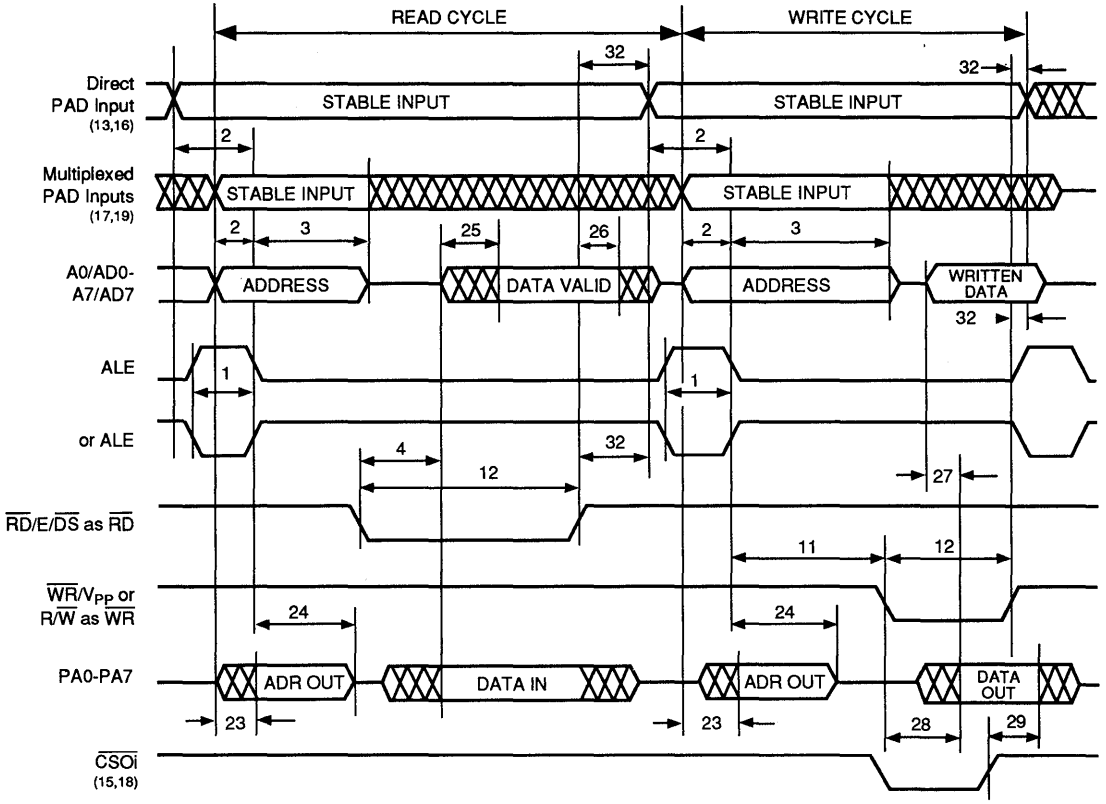
See referenced notes on page 238.

Figure 13. Chip-Select Output Timing



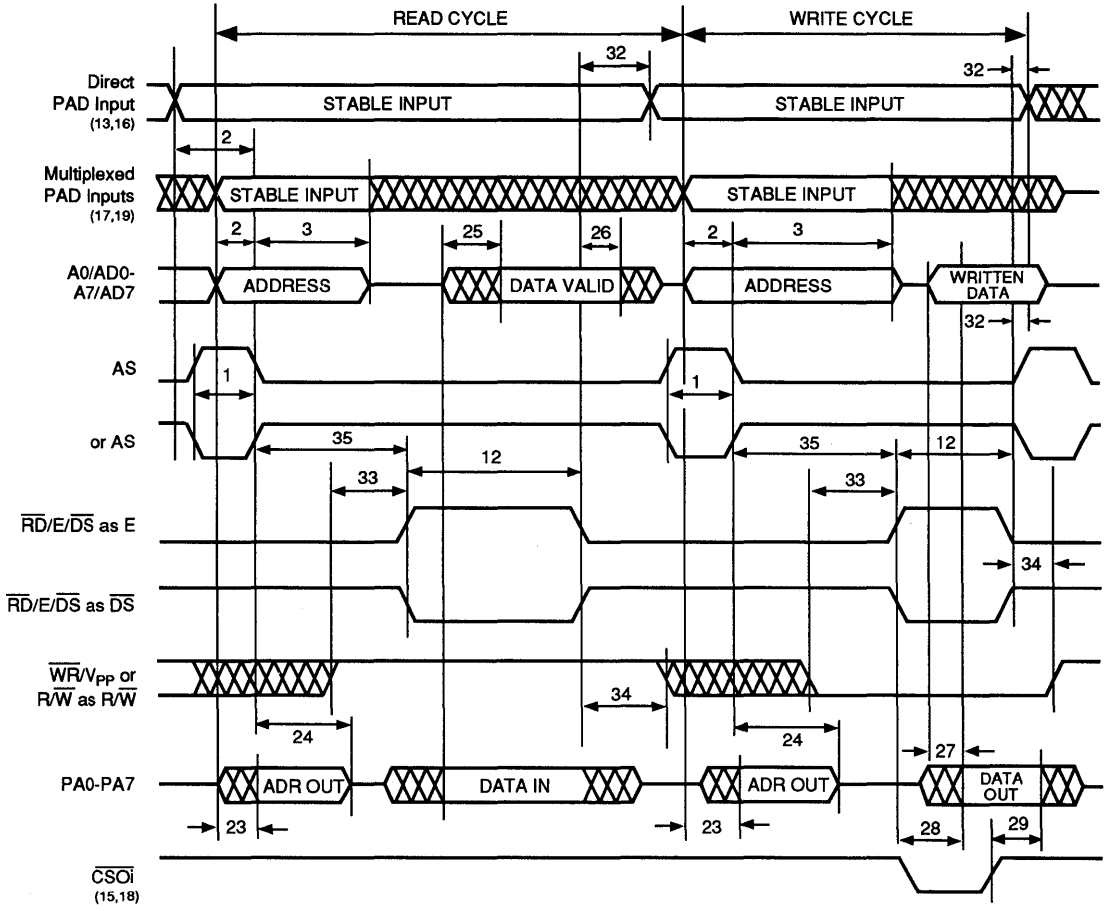
See referenced notes on page 238.

Figure 14. Port A as AD0 – AD7 Timing (Track Mode), CRRWR = 0



See referenced notes on page 238.

Figure 15. Port A as AD0 – AD7 Timing (Track Mode), CRRWR = 1



Notes for Timing Diagrams

13. Direct PAD input = any of the following direct PAD input lines: CSI/A19 as transparent A19, RD/E/DS, WR or R/W, transparent PC0–PC2, ALE in non-multiplexed modes.
14. Multiplexed inputs: any of the following inputs that are latched by the ALE (or AS): A0/AD0–A15/AD15, CSI/A19 as ALE dependent A19, ALE dependent PC0–PC2.
15. CSOi = any of the chip-select output signals coming through Port B (CS0–CS7) or through Port C (CS8–CS10).
16. CSADOUT1, which internally enables the address transfer to Port A, should be derived only from direct PAD input signals, otherwise the address propagation delay is slowed down.
17. CSADIN and CSADOUT2, which internally enable the data-in or data-out transfers, respectively, can be derived from any combination of direct PAD inputs and multiplexed PAD inputs.
18. The write operation signals are included in the CSOi expression.
19. Multiplexed PAD inputs: any of the following PAD inputs that are latched by the ALE (or AS) in the multiplexed modes: A11/AD11–A15/AD15, CSI/A19 as ALE dependent A19, ALE dependent PC0–PC2.
20. CSOi product terms can include any of the PAD input signals except for reset and CSI.

Pin Capacitance[21]

$T_A = 25\,°C, f = 1\ MHz$

Symbol	Parameter	Conditions	Typical[22]	Max	Unit
C_{IN}	Capacitance (for input pins only)	$V_{IN} = 0\ V$	4	6	pF
C_{OUT}	Capacitance (for input/output pins)	$V_{OUT} = 0\ V$	8	12	pF
C_{VPP}	Capacitance (for $\overline{WR}/V_{PP}$ or $R/\overline{W}/V_{PP}$)	$V_{PP} = 0\ V$	18	25	pF

NOTES: 21. This parameter is only sampled and is not 100% tested.
22. Typical values are for $T_A = 25°C$ and nominal supply voltages.

Erasure and Programming

To clear all locations of their programmed contents, expose the device to ultra-violet light source. A dosage of 15 W second/cm² is required. This dosage can be obtained with exposure to a wavelength of 2537 Å and intensity of 12000 µW/cm² for 15 to 20 minutes. The device should be about 1 inch from the source, and all filters should be removed from the UV light source prior to erasure.

The PSD302L and similar devices will erase with light sources having wavelengths shorter than 4000 Å. Although the erasure times will be much longer than with UV sources at 2537 Å, exposure to fluorescent light and sunlight eventually erases the device. For maximum system reliability, these sources should be avoided. If used in such an environment, the package windows should be covered by an opaque substance.

Upon delivery, or after each erasure, the PSD302L device has all bits in the PAD and EPROM in the "1" or high state. The configuration bits are in the "0" or low state. The code, configuration, and PAD MAP data are loaded through the procedure of programming

Pin Assignments

Pin Name	44-Pin PLCC/CLCC Package
$\overline{BHE}/\overline{PSEN}$	1
$\overline{WR}/V_{PP}$ or R/$\overline{W}$	2
$\overline{RESET}$	3
PB7	4
PB6	5
PB5	6
PB4	7
PB3	8
PB2	9
PB1	10
PB0	11
GND	12
ALE or AS	13
PA7	14
PA6	15
PA5	16
PA4	17
PA3	18
PA2	19
PA1	20
PA0	21
$\overline{RD}$/E/$\overline{DS}$	22
AD0/A0	23
AD1/A1	24
AD2/A2	25
AD3/A3	26
AD4/A4	27
AD5/A5	28
AD6/A6	29
AD7/A7	30
AD8/A8	31
AD9/A9	32
AD10/A10	33
GND	34
AD11/A11	35
AD12/A12	36
AD13/A13	37
AD14/A14	38
AD15/A15	39
PC0	40
PC1	41
PC2	42
A19/$\overline{CSI}$	43
V_{CC}	44

Package Information

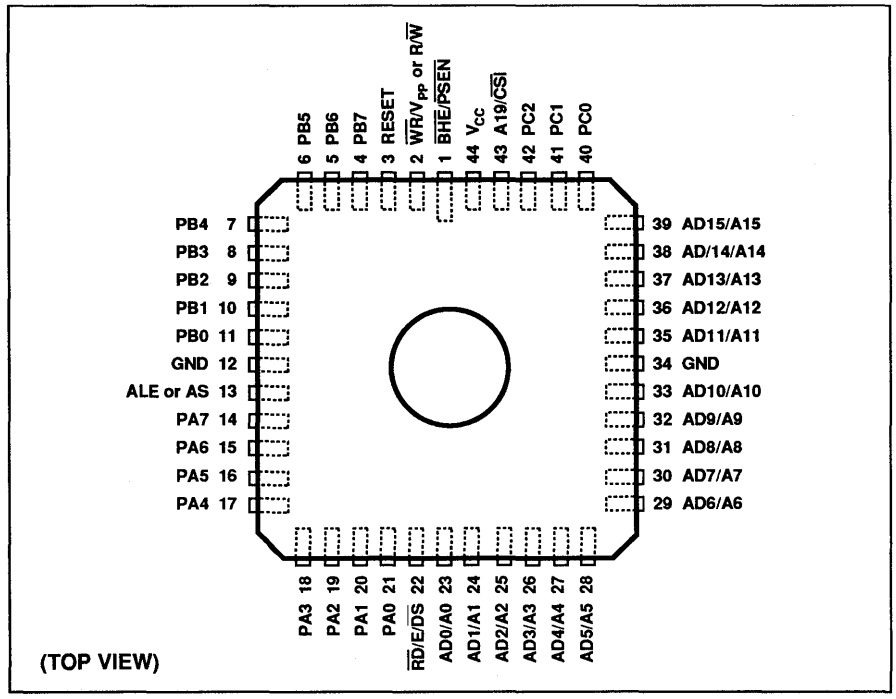


Figure 16. Drawing L4 — 44 Pin Ceramic Leaded Chip Carrier (CLCC) with Window (Package Type L)

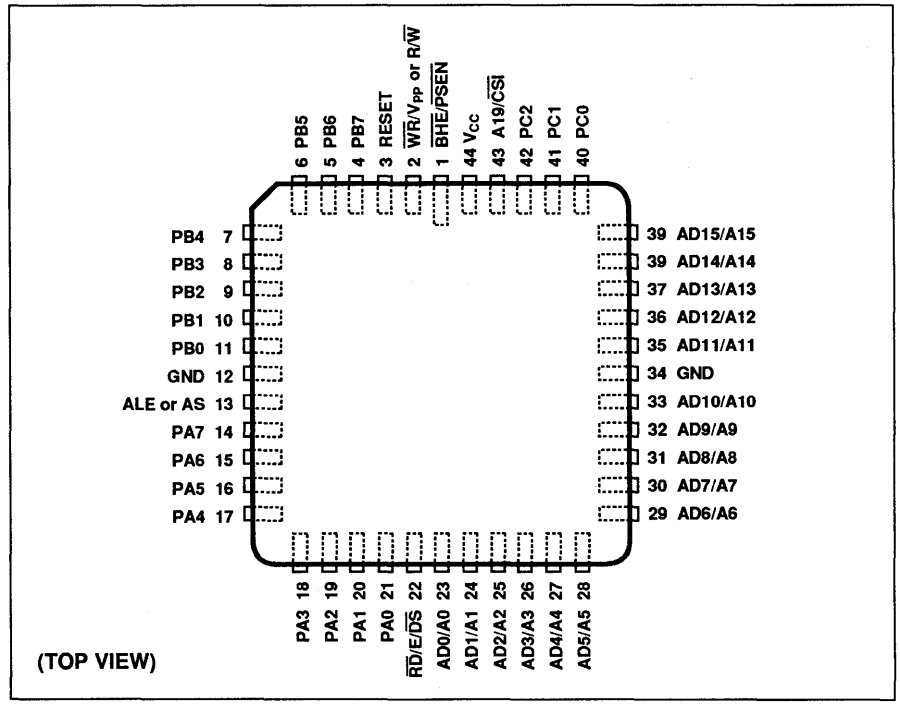


Figure 17. Drawing J2 — 44 Pin Plastic Leaded Chip Carrier (PLCC) with Window (Package Type J)

Ordering Information

Part Number	Spd. (ns)	Package Type	Package Drawing	Operating Temperature Range	Manufacturing Procedure
PSD302L25 A	250	44-pin PLDCC	J2	Commercial	Standard
PSD302L25 KA	250	44-pin CLDCC	L4	Commercial	Standard
PSD302L30 A	300	44-pin PLDCC	J2	Commercial	Standard
PSD302L30 KA	300	44-pin CLDCC	L4	Commercial	Standard

3-volt single-chip microcontroller peripheral PSD312L

Key Features

- ❑ Single Chip Programmable Peripheral for Microcontroller-based Applications
- ❑ 3.0 to 5.5 Volt Operation
- ❑ 19 Individually Configurable I/O pins that can be used as:
  - — Microcontroller I/O port expansion
  - — Programmable Address Decoder (PAD) I/O
  - — Latched address output
  - — Open drain or CMOS
- ❑ Two Programmable Arrays (PAD A & PAD B)
  - — Total of 40 Product Terms and up to 18 Inputs and 24 Outputs
  - — Direct Address Decoding up to 1 Meg address space and up to 16 Meg with paging
  - — Logic replacement
- ❑ "No Glue" Microcontroller Chip-Set
  - — Built-in address latches for multiplexed address/data bus
  - — Non-multiplexed address/data bus mode
  - — 8-bit data bus width
  - — ALE and Reset polarity programmable
  - — Selectable modes for read and write control bus as $\overline{RD}/\overline{WR}$, R/$\overline{W}$/E, or R/$\overline{W}$/$\overline{DS}$
  - — $\overline{PSEN}$ pin for 8051 users
- ❑ Built-In Page Logic
  - — To Expand the Address Space of Microcontrollers with Limited Address Space Capabilities
  - — Up to 16 pages
- ❑ 512 Kbits of UV EPROM
  - — Configurable as 64K x 8
  - — Divides into 8 equal mappable blocks for optimized mapping
  - — Block resolution is 8K x 8
  - — 250 ns EPROM access time, including input latches and PAD address decoding.
- ❑ 16 Kbit Static RAM
  - — Configurable as 2K x 8 or as 1K x 16
  - — 250 ns SRAM access time, including input latches and PAD address decoding
- ❑ Address/Data Track Mode
  - — Enables easy Interface to Shared Resources (e.g., Mail Box SRAM) with other Microcontrollers or a Host Processor
- ❑ CMiser-Bit
  - — Programmable option to further reduce power consumption
- ❑ Built-In Security
  - — Locks the PSD312L and PAD Decoding Configuration
- ❑ Available in a Choice of Packages
  - — 44 Pin PLDCC and CLDCC
- ❑ Simple Menu-Driven Software: Configure the PSD312L on an IBM PC
- ❑ Pin and Functionally Compatible with the PSD3XX and PSD3XXL Series.

Absolute Maximum Ratings[1]

Symbol	Parameter	Condition	Min	Max	Unit
T_{STG}	Storage Temperature	CERAMIC	−65	+150	°C
		PLASTIC	−65	+125	°C
T_{STG}	Storage Temperature		−65	+150	°C
	Voltage on any Pin	With Respect to GND	−0.6	+7	V
V_{PP}	Programming Supply Voltage	With Respect to GND	−0.6	+14	V
V_{CC}	Supply Voltage	With Respect to GND	−0.6	+7	V
	ESD Protection			>2000	V

NOTE: 1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods of time may affect device reliability.

Operating Range

Range	Temperature	V_{CC}
Commercial	0° C to +70°C	3.0 V to 5.5 V

Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	Supply Voltage	All Speeds	3.0	3.3	5.5	V
V_{IH}	High-level Input Voltage	V_{CC} = 3.0 V to 5.5 V	0.7 V_{CC}		V_{CC} + 0.5	V
V_{IL}	Low-level Input Voltage	V_{CC} = 3.0 V to 5.5 V	−0.5		0.2 V_{CC}*	V
					0.3 V_{CC}**	V

* Before 8/1/1993.
** After 8/1/1993.

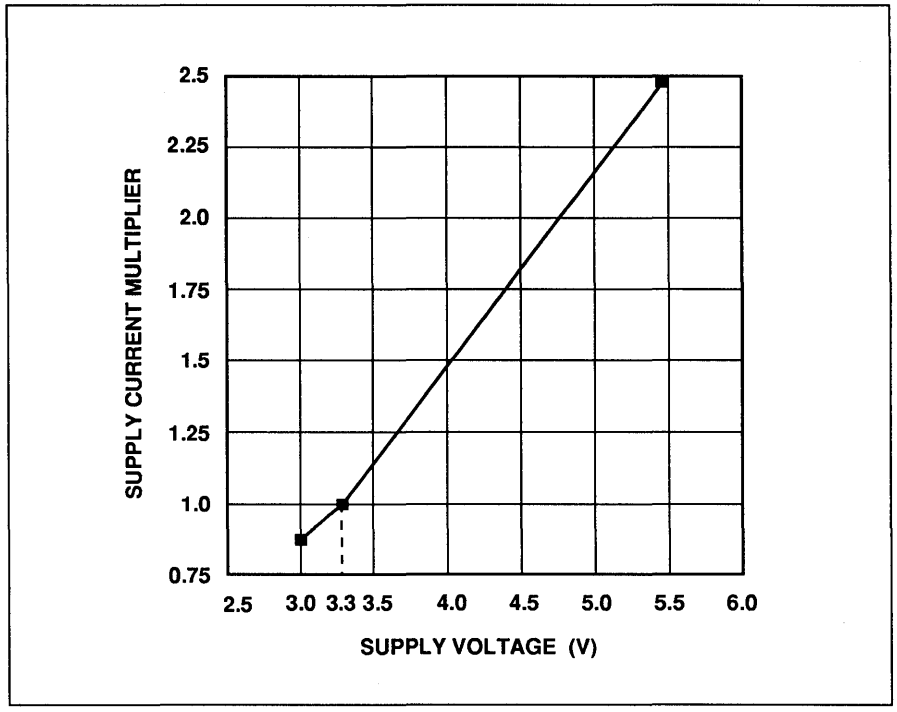
DC Characteristics

Symbol	Parameter	Conditions	CMiser = 1			Subtract:			Unit
			Min	Typ	Max	Min	Typ	Max	
V_{OL}	Output Low Voltage	I_{OL} = 20 µA V_{CC} = 3.0 V		0.01	0.1				V
		I_{OL} = 4 mA V_{CC} = 3.0 V		0.15	0.4				V
V_{OH}	Output High Voltage	I_{OH} = –20 µA V_{CC} = 3.0 V	2.9	2.99					V
		I_{OH} = –1 mA V_{CC} = 3.0 V	2.4	2.6					V
I_{SB1}	V_{CC} Standby Current (CMOS) (Notes 2 and 3)	V_{CC} = 3.3 V		10*	25*				µA
				1**	5**				
I_{CC1}	Active Current (CMOS) (No Internal Memory Block Selected) (Notes 2 and 5)	V_{CC} = 3.3 V (Note 5)		6	12		3.0	5	mA
		V_{CC} = 3.3 V (Note 6)		10	20		3.0	5	mA
I_{CC2}	Active Current (CMOS) (EPROM Block Selected) (Notes 2 and 5)	V_{CC} = 3.3 V (Note 5)		6	12		2	3	mA
		V_{CC} = 3.3 V (Note 6)		10	20		2	3	mA
I_{CC3}	Active Current (CMOS) (SRAM Block Selected) (Notes 2 and 5)	V_{CC} = 3.3 V (Note 5)		20	33		5	8	mA
		V_{CC} = 3.3 V (Note 6)		24	40		5	8	mA
I_{LI}	Input Leakage Current	V_{IN} = V_{CC} or GND	–1	±0.1	1				µA
I_{LO}	Output Leakage Current	V_{OUT} = V_{CC} or GND	–10	±5	10				µA

NOTES: 2. CMOS inputs: GND ± 0.3 V or V_{CC} ± 0.3V.
3. $\overline{CSI}$/A19 is high and the part is in a power-down configuration mode.
4. Add 2.0 mA/MHz for AC power component (power = AC + DC).
5. Ten (10) PAD product terms active. (Add 190 µA per product term, typical, or 240 µA per product term maximum.)
6. Forty (40) PAD product terms active.

* Before 8/1/1993.
** After 8/1/1993.

Figure 1. Normalized Supply Current vs. Supply Voltage



The Normalized Supply Current vs. Supply Voltage graph shown above, provides a multiplier for any I_{SB} or I_{CC} value in the D.C. Characteristics table. As noted, it is normalized for a supply voltage of 3.3 volts. Since device characterization data shows very little supply current difference over speed, the multiplier includes all frequencies of operation from standby to quiescent to full dynamic speed. To use, calculate the supply current at 3.3 volts for your operation configuration using the D.C. Characteristics table. Then multiply that value by the Supply Current Multiplier for the supply voltage actually being used.

AC Characteristics[8] (See Timing Diagrams)

Symbol	Parameter	-25		-30		CMiser = 1 Add:	Unit
		Min	Max	Min	Max		
T1	ALE or AS Pulse Width	75		80			ns
T2	Address Set-up Time	30		35			ns
T3	Address Hold Time	30		35		0	ns
T4	Leading Edge of Read to Data Active	0		0		0	ns
T5	ALE Valid to Data Valid		250		300	25	ns
T6	Address Valid to Data Valid		250		300	25	ns
T7	$\overline{CSi}$ Active to Data Valid		275		325	30	ns
T8	Leading Edge of Read to Data Valid		90		95	0	ns
T9	Read Data Hold Time	0		0		0	ns
T10	Trailing Edge of Read to Data High-Z		50		55	0	ns
T11	Trailing Edge of ALE or AS to Leading Edge of Write		40		45		ns
T12	$\overline{RD}$, E, $\overline{PSEN}$, $\overline{DS}$ Pulse Width	100		110		0	ns
T12A	$\overline{WR}$ Pulse Width	90		95		0	ns
T13	Trailing Edge of Write or Read to Leading Edge of ALE or AS	0		0		0	ns
T14	Address Valid to Trailing Edge of Write	250		300		0	ns
T15	$\overline{CSi}$ Active to Trailing Edge of Write	275		375		0	ns
T16	Write Data Set-up Time	60		65		0	ns
T17	Write Data Hold Time	25		30		0	ns
T18	Port to Data Out Valid Propagation Delay		70		75	0	ns
T19	Port Input Hold Time	0		0		0	ns
T20	Trailing Edge of Write to Port Output Valid	100		110		0	ns
T21	ADi or Control to $\overline{CSOi}$ Valid	6	80	5	85	0	ns
T22	ADi or Control to $\overline{CSOi}$ Invalid	4	80	4	85	0	ns
T23	Track Mode Address Propagation Delay: CSADOUT1 Already True		70		75	0	ns
T23A	Track Mode Address Propagation Delay: CSADOUT1 Becomes True During ALE or AS		100		110	0	ns

NOTE: 8. These AC Characteristics are for VCC = 3.0 – 3.6V.

AC Characteristics (Cont.)

Symbol	Parameter	-25		-30		CMiser = 1 Add:	Unit
		Min	Max	Min	Max		
T24	Track Mode Trailing Edge of ALE or AS to Address High-Z		60		65	0	ns
T25	Track Mode Read Propagation Delay		70		75	0	ns
T26	Track Mode Read Hold Time	10	70	10	75		ns
T27	Track Mode Write Cycle, Data Propagation Delay		60		65	0	ns
T28	Track Mode Write Cycle, Write to Data Propagation Delay	7	80	7	85	0	ns
T29	Hold Time of Port A Valid During Write $\overline{CSOi}$ Trailing Edge	4		4		0	ns
T30	$\overline{CSI}$ Active to $\overline{CSOi}$ Active	9	110	8	120	0	ns
T31	$\overline{CSI}$ Inactive to $\overline{CSOi}$ Inactive	9	110	8	120	0	ns
T32	Direct PAD Input as Hold Time	24		30		0	ns
T33	R/$\overline{W}$ Active to E or DS Start	60		65		0	ns
T34	E or $\overline{DS}$ End to R/$\overline{W}$	60		65		0	ns
T35	AS Inactive to E high	40		45		0	ns
T36	Address to Leading Edge of Write	50		60		0	ns

NOTES: 9. ADi = any address line.
10. $\overline{CSOi}$ = any of the chip-select output signals coming through Port B ($\overline{CS0}$–$\overline{CS7}$) or through Port C ($\overline{CS8}$–$\overline{CS10}$).
11. Direct PAD input = any of the following direct PAD input lines: $\overline{CSI}$/A19 as transparent A19, $\overline{RD}$/E/$\overline{DS}$, $\overline{WR}$ or R/$\overline{W}$, transparent PC0–PC2, ALE (or AS).
12. Control signals $\overline{RD}$/E/$\overline{DS}$ or $\overline{WR}$ or R/$\overline{W}$.

Figure 2. AC Testing Input/Output Waveform

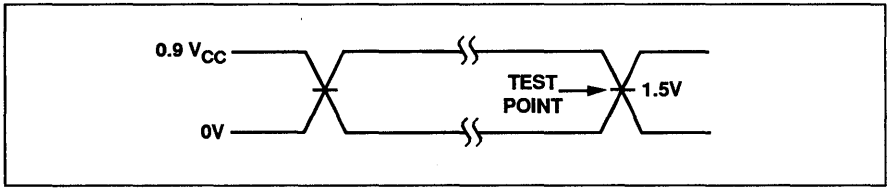


Figure 3. AC Testing Load Circuit

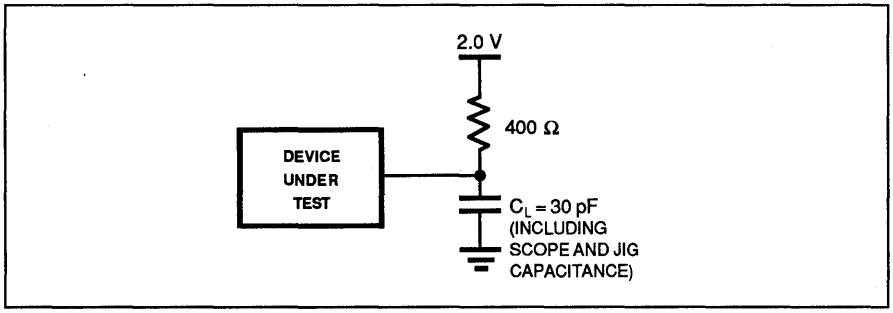


Figure 4. The Reset Cycle (RESET)

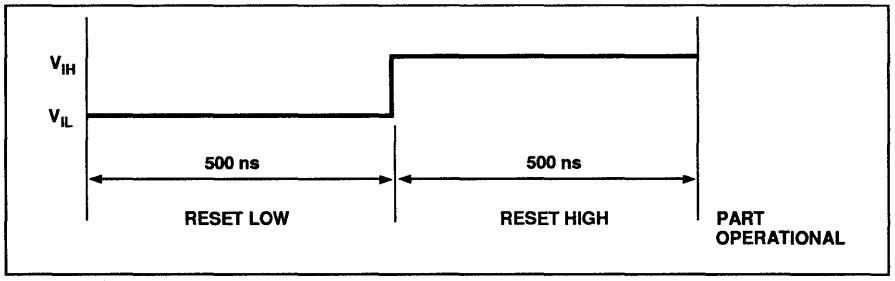
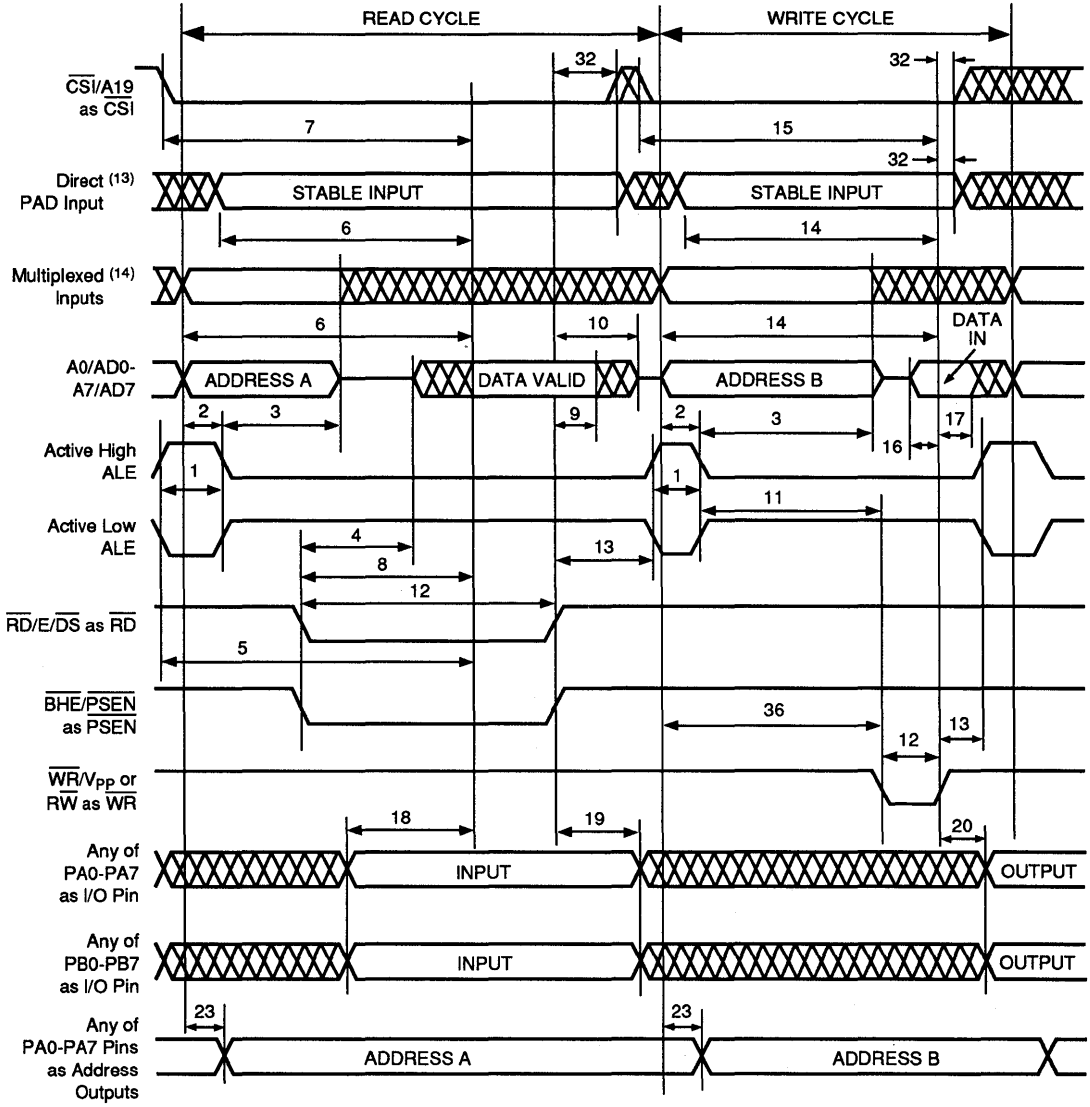
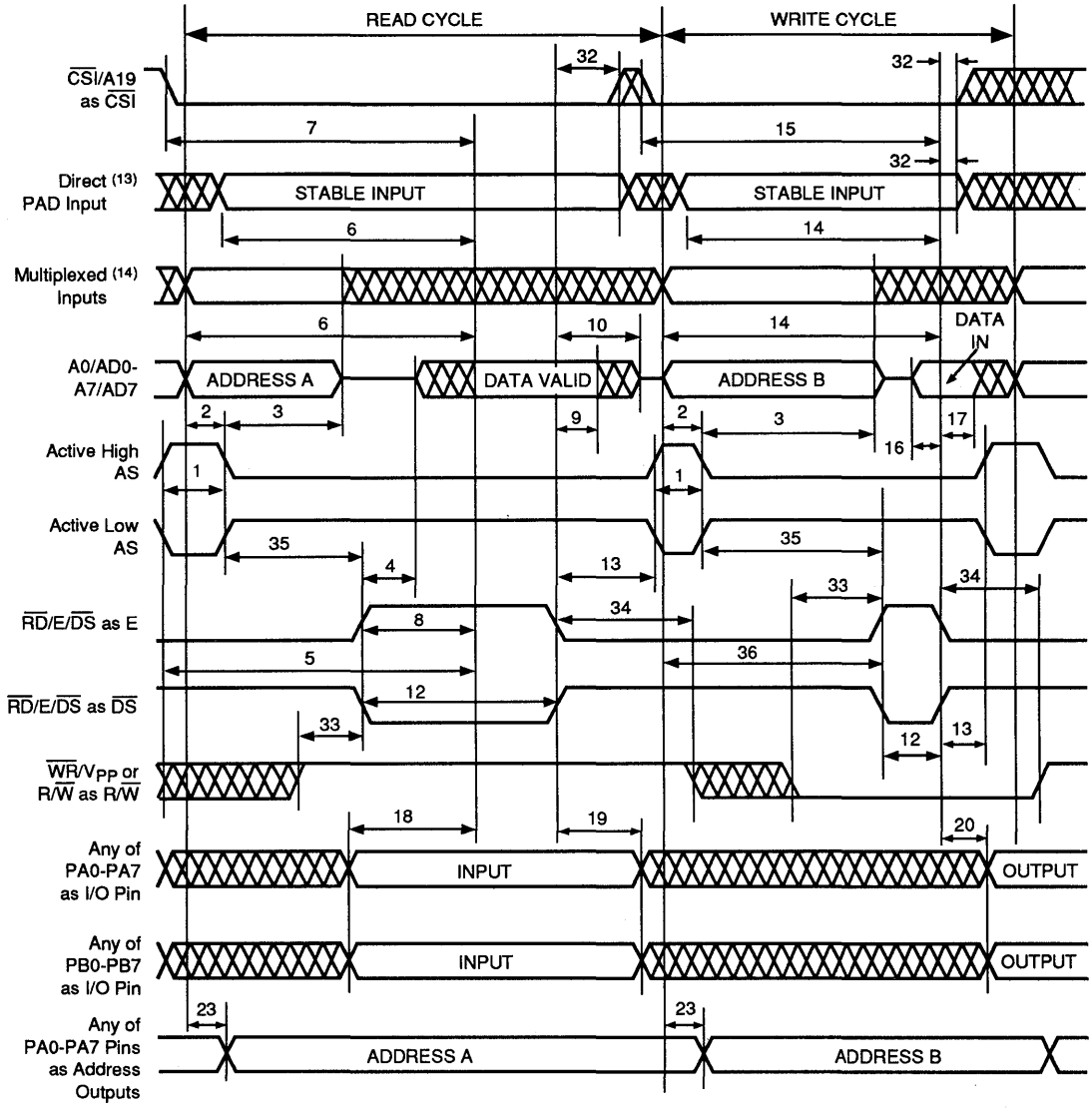


Figure 5. Timing of 8-Bit Multiplexed Address/Data Bus, CRRWR = 0



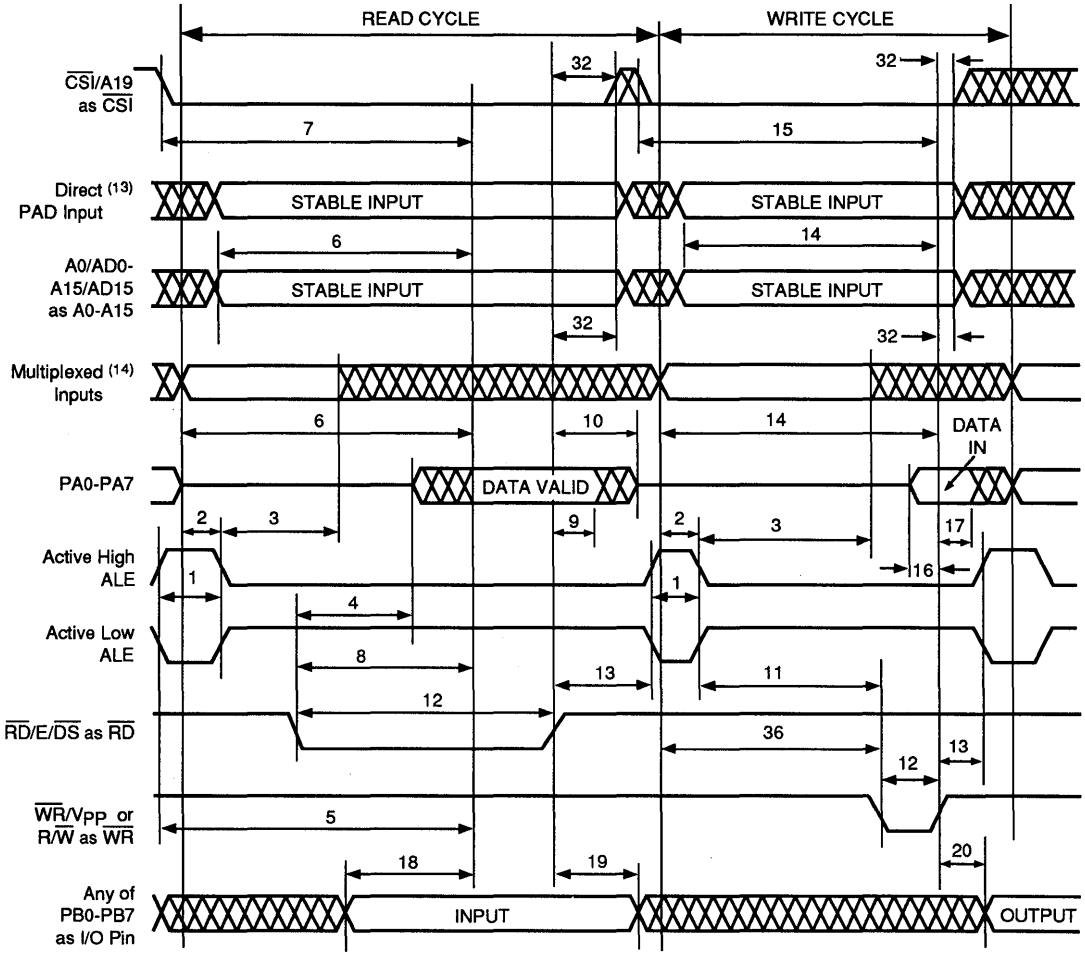
See referenced notes on page 256.

Figure 6. Timing of 8-Bit Multiplexed Address/Data Bus, CRRWR = 1



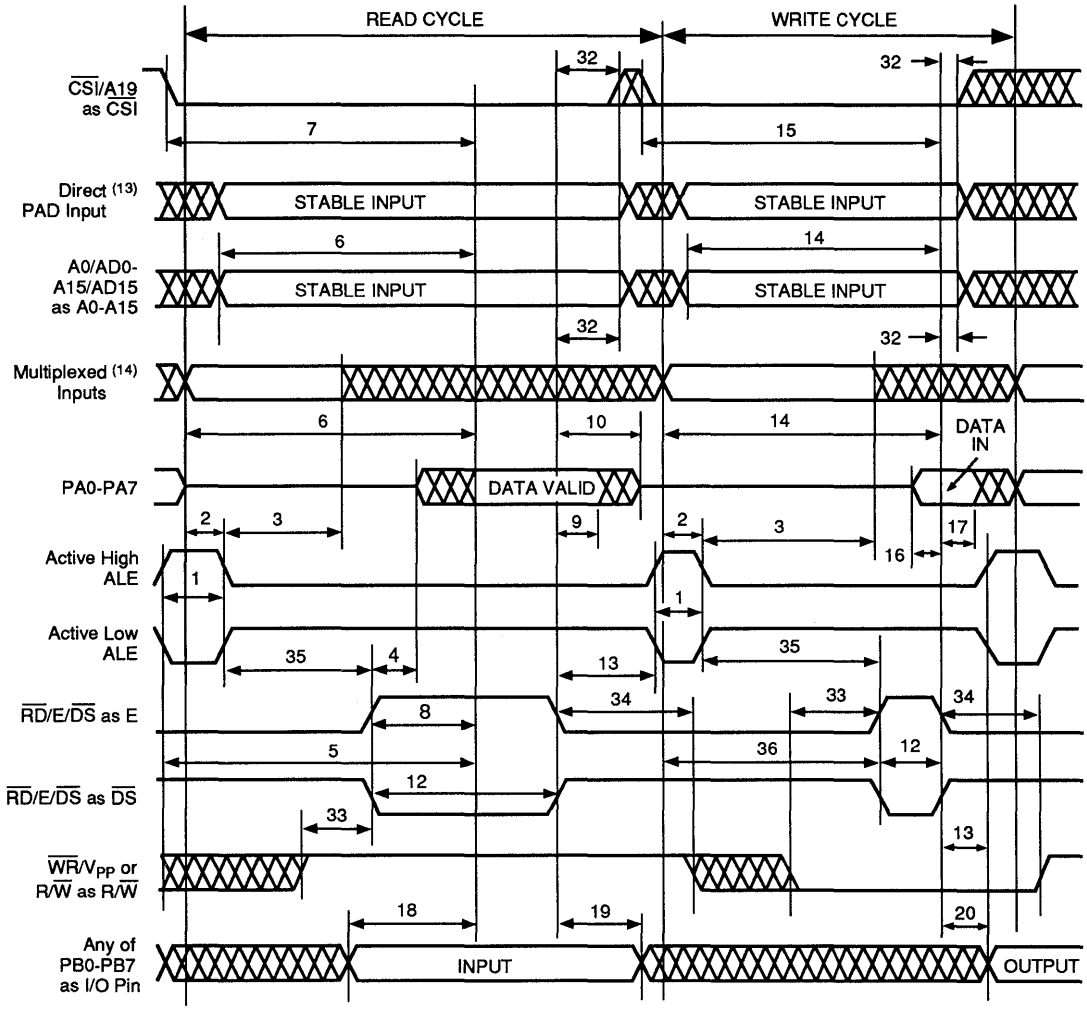
See referenced notes on page 256.

Figure 7. Timing of 8-Bit Data Non-Multiplexed Address/Data Bus, CRRWR = 0



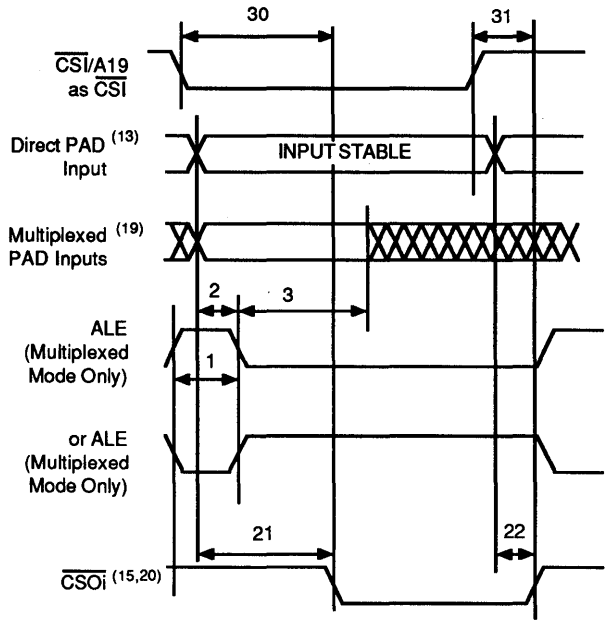
See referenced notes on page 256.

Figure 8. Timing of 8-Bit Data Non-Multiplexed Address/Data Bus, CRRWR = 1



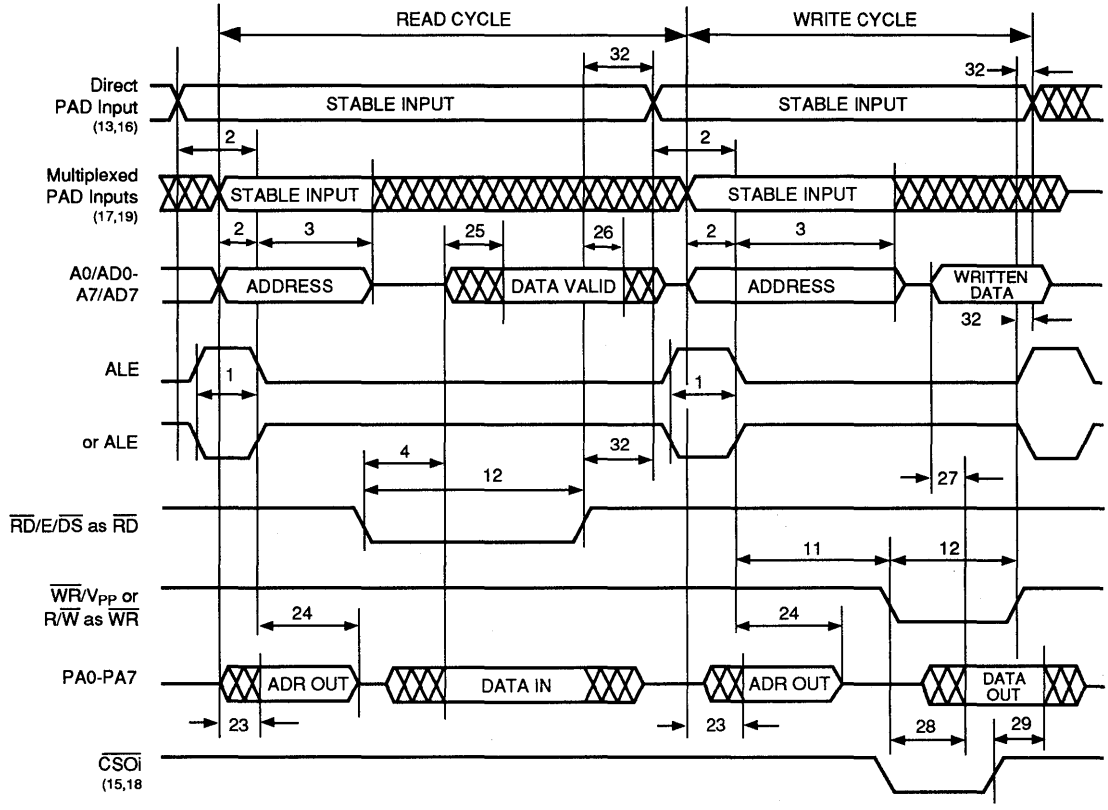
See referenced notes on page 256.

Figure 9. Chip-Select Output Timing



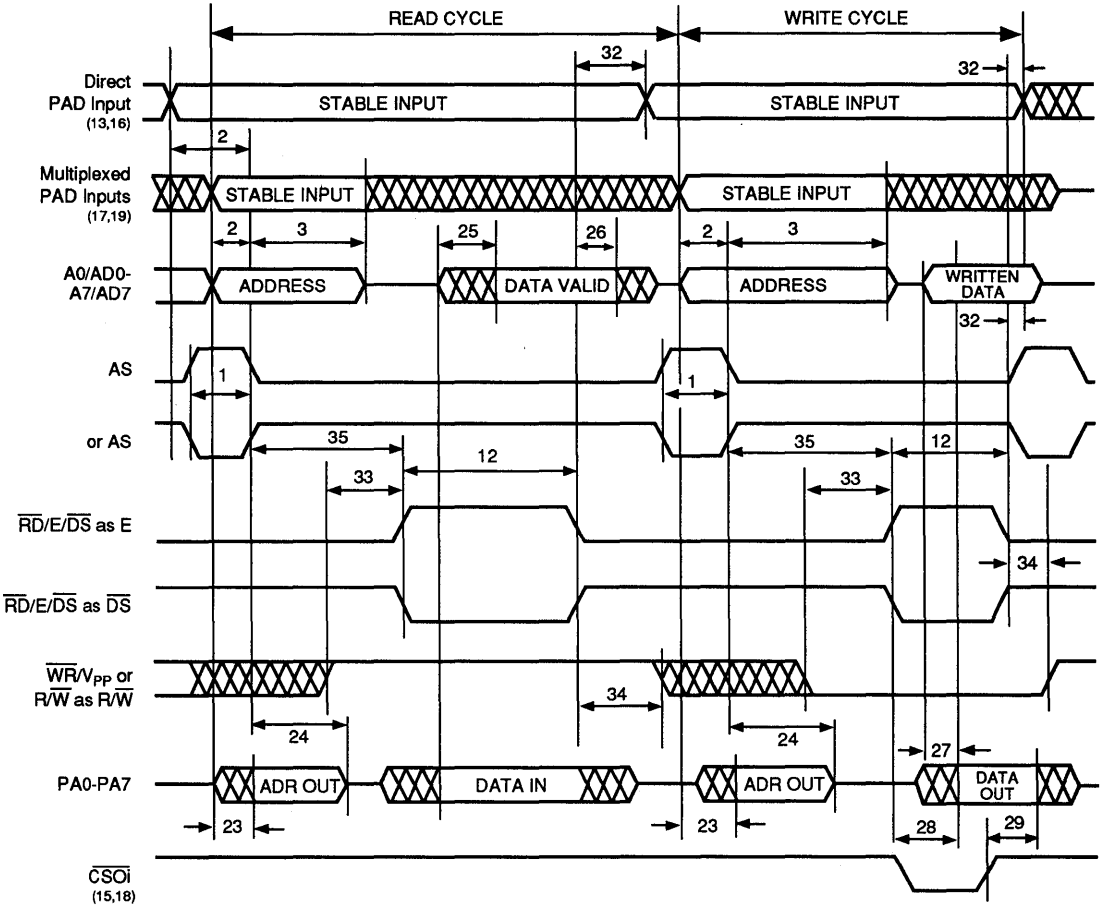
See referenced notes on page 256.

Figure 10. Port A as AD0 – AD7 Timing (Track Mode), CRRWR = 0



See referenced notes on page 256.

Figure 11. Port A as AD0 – AD7 Timing (Track Mode), CRRWR = 1



Notes for Timing Diagrams

13. Direct PAD input = any of the following direct PAD input lines: $\overline{CSI}$/A19 as transparent A19, $\overline{RD}$/E/$\overline{DS}$, $\overline{WR}$ or R/$\overline{W}$, transparent PC0–PC2, ALE in non-multiplexed modes.
14. Multiplexed inputs: any of the following inputs that are latched by the ALE (or AS): A0/AD0–A15/AD15, $\overline{CSI}$/A19 as ALE dependent A19, ALE dependent PC0–PC2.
15. $\overline{CSOi}$ = any of the chip-select output signals coming through Port B ($\overline{CS0}$–$\overline{CS7}$) or through Port C ($\overline{CS8}$–$\overline{CS10}$).
16. CSADOUT1, which internally enables the address transfer to Port A, should be derived only from direct PAD input signals, otherwise the address propagation delay is slowed down.
17. CSADIN and CSADOUT2, which internally enable the data-in or data-out transfers, respectively, can be derived from any combination of direct PAD inputs and multiplexed PAD inputs.
18. The write operation signals are included in the $\overline{CSOi}$ expression.
19. Multiplexed PAD inputs: any of the following PAD inputs that are latched by the ALE (or AS) in the multiplexed modes: A11/AD11–A15/AD15, $\overline{CSI}$/A19 as ALE dependent A19, ALE dependent PC0–PC2.
20. $\overline{CSOi}$ product terms can include any of the PAD input signals except for reset and $\overline{CSI}$.

Pin Capacitance[21]

$T_A = 25\,°C, f = 1\,MHz$

Symbol	Parameter	Conditions	Typical[22]	Max	Unit
C_{IN}	Capacitance (for input pins only)	$V_{IN} = 0$ V	4	6	pF
C_{OUT}	Capacitance (for input/output pins)	$V_{OUT} = 0$ V	8	12	pF
C_{VPP}	Capacitance (for $\overline{WR}/V_{PP}$ or $R/\overline{W}/V_{PP}$)	$V_{PP} = 0$ V	18	25	pF

NOTES: 21. This parameter is only sampled and is not 100% tested.
22. Typical values are for $T_A = 25°C$ and nominal supply voltages.

Erasure and Programming

To clear all locations of their programmed contents, expose the device to ultra-violet light source. A dosage of 15 W second/cm² is required. This dosage can be obtained with exposure to a wavelength of 2537 Å and intensity of 12000 μW/cm² for 15 to 20 minutes. The device should be about 1 inch from the source, and all filters should be removed from the UV light source prior to erasure.

The PSD312L and similar devices will erase with light sources having wavelengths shorter than 4000 Å. Although the erasure times will be much longer than with UV sources at 2537 Å, exposure to fluorescent light and sunlight eventually erases the device. For maximum system reliability, these sources should be avoided. If used in such an environment, the package windows should be covered by an opaque substance.

Upon delivery, or after each erasure, the PSD312L device has all bits in the PAD and EPROM in the "1" or high state. The configuration bits are in the "0" or low state. The code, configuration, and PAD MAP data are loaded through the procedure of programming

Pin Assignments

Pin Name	44-Pin PLCC/CLCC Package
$\overline{PSEN}$	1
$\overline{WR}/V_{PP}$ or R/$\overline{W}$	2
$\overline{RESET}$	3
PB7	4
PB6	5
PB5	6
PB4	7
PB3	8
PB2	9
PB1	10
PB0	11
GND	12
ALE or AS	13
PA7	14
PA6	15
PA5	16
PA4	17
PA3	18
PA2	19
PA1	20
PA0	21
$\overline{RD}$/E/$\overline{DS}$	22
AD0/A0	23
AD1/A1	24
AD2/A2	25
AD3/A3	26
AD4/A4	27
AD5/A5	28
AD6/A6	29
AD7/A7	30
A8	31
A9	32
A10	33
GND	34
A11	35
A12	36
A13	37
A14	38
A15	39
PC0	40
PC1	41
PC2	42
A19/$\overline{CSI}$	43
V_{CC}	44

Package Information

Figure 12. Drawing L4 — 44 Pin Ceramic Leaded Chip Carrier (CLCC) with Window (Package Type L)

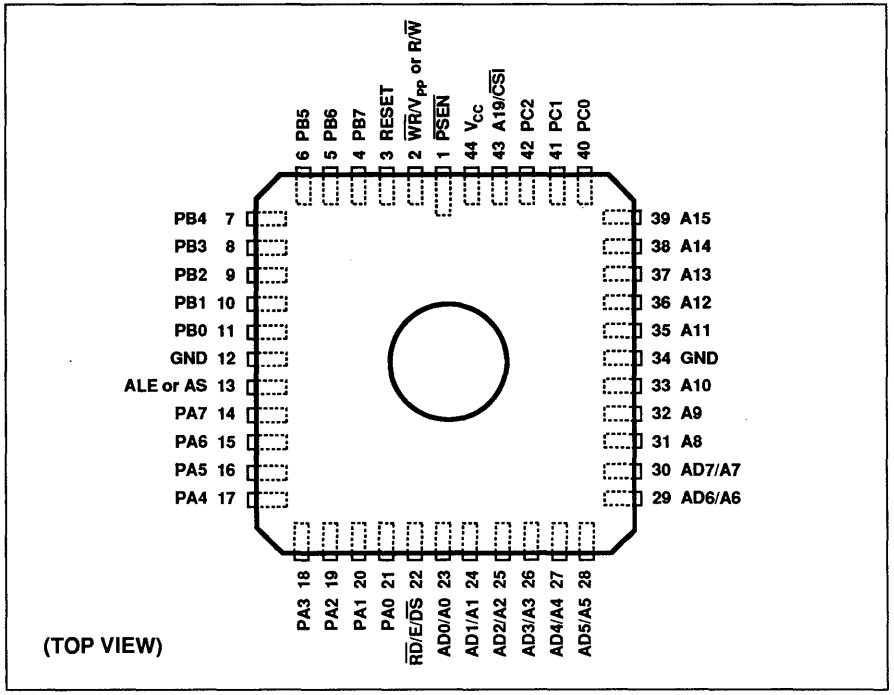
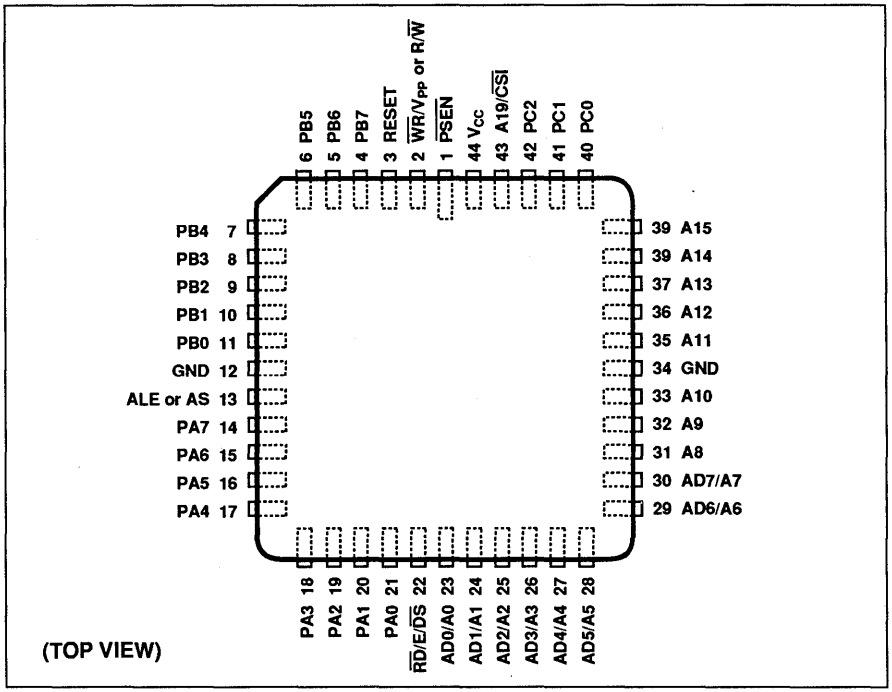


Figure 13. Drawing J2 — 44-Pin Plastic Leaded Chip Carrier (PLCC) (Package Type J)



Ordering Information

Part Number	Spd. (ns)	Package Type	Package Drawing	Operating Temperature Range	Manufacturing Procedure
PSD312L25 A	250	44-pin PLCC	J2	Commercial	Standard
PSD312L25 KA	250	44-pin CLCC	L4	Commercial	Standard
PSD312L30 A	300	44-pin PLCC	J2	Commercial	Standard
PSD312L30 KA	300	44-pin CLCC	L4	Commercial	Standard

3-volt single-chip microcontroller peripheral — PSD303L

Key Features

- ❑ Single Chip Programmable Peripheral for Microcontroller-based Applications
- ❑ 3.0 to 5.5 Volt Operation
- ❑ 19 Individually Configurable I/O pins that can be used as:
  - — Microcontroller I/O port expansion
  - — Programmable Address Decoder (PAD) I/O
  - — Latched address output
  - — Open drain or CMOS
- ❑ Two Programmable Arrays (PAD A & PAD B)
  - — Total of 40 Product Terms and up to 18 Inputs and 24 Outputs
  - — Direct Address Decoding up to 1 Meg address space and up to 16 Meg with paging
  - — Logic replacement
- ❑ "No Glue" Microcontroller Chip-Set
  - — Built-in address latches for multiplexed address/data bus
  - — Non-multiplexed address/data bus mode
  - — Selectable 8 or 16 bit data bus width
  - — ALE and Reset polarity programmable
  - — Selectable modes for read and write control bus as $\overline{RD}/\overline{WR}$, R/$\overline{W}$/E, or R/$\overline{W}$/$\overline{DS}$
  - — $\overline{BHE}$ pin for byte select in 16-bit mode
  - — $\overline{PSEN}$ pin for 8051 users
- ❑ Built-In Page Logic
  - — To Expand the Address Space of Microcontrollers with Limited Address Space Capabilities
  - — Up to 16 pages
- ❑ 1M bit of UV EPROM
  - — Configurable as 128K x 8 or as 64K x 16
  - — Divides into 8 equal mappable blocks for optimized mapping
  - — Block resolution is 16K x 8 or 8K x 16
  - — 250 ns EPROM access time, including input latches and PAD address decoding.
- ❑ 16 Kbit Static RAM
  - — Configurable as 2K x 8 or as 1K x 16
  - — 250 ns SRAM access time, including input latches and PAD address decoding
- ❑ Address/Data Track Mode
  - — Enables easy Interface to Shared Resources (e.g., Mail Box SRAM) with other Microcontrollers or a Host Processor
- ❑ CMiser-Bit
  - — Programmable option to further reduce power consumption
- ❑ Built-In Security
  - — Locks the PSD303L and PAD Decoding Configuration
- ❑ Available in a Choice of Packages
  - — 44 Pin PLDCC and CLDCC
- ❑ Simple Menu-Driven Software: Configure the PSD303L on an IBM PC
- ❑ Pin and Functionally Compatible with the PSD3XX and PSD3XXL Series

Absolute Maximum Ratings[1]

Symbol	Parameter	Condition	Min	Max	Unit
T_{STG}	Storage Temperature	CERAMIC	– 65	+ 150	°C
		PLASTIC	– 65	+ 125	°C
T_{STG}	Storage Temperature		– 65	+ 150	°C
	Voltage on any Pin	With Respect to GND	– 0.6	+ 7	V
V_{PP}	Programming Supply Voltage	With Respect to GND	– 0.6	+ 14	V
V_{CC}	Supply Voltage	With Respect to GND	– 0.6	+ 7	V
	ESD Protection			>2000	V

NOTE: 1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods of time may affect device reliability.

Operating Range

Range	Temperature	V_{CC}
Commercial	0° C to +70°C	3.0 V to 5.5 V

Recommended Operating Conditions

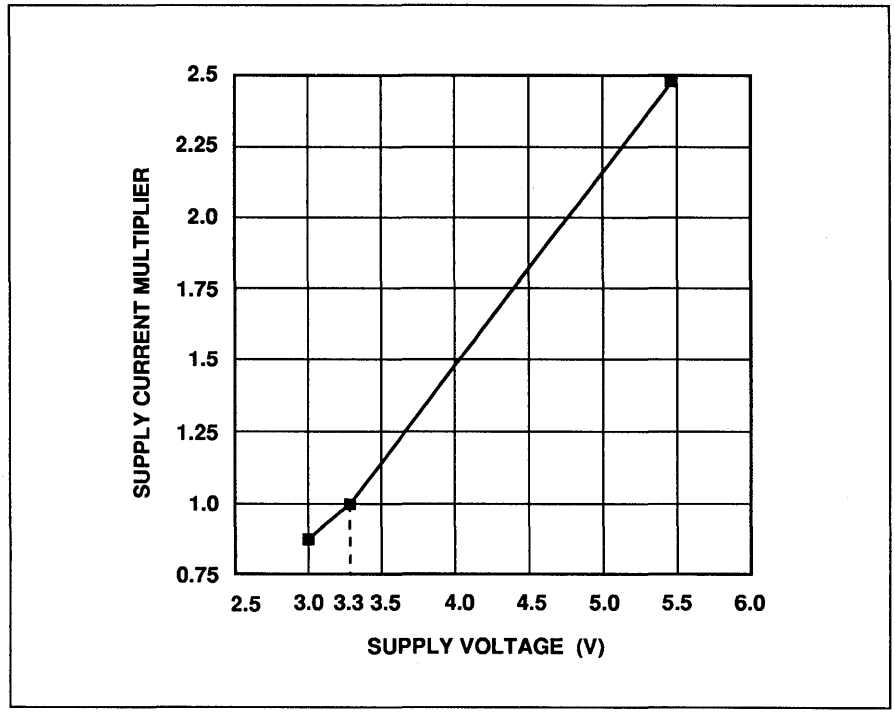
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	Supply Voltage	All Speeds	3.0	3.3	5.5	V
V_{IH}	High-level Input Voltage	V_{CC} = 3.0 V to 5.5 V	0.7 V_{CC}		V_{CC} + 0.5	V
V_{IL}	Low-level Input Voltage	V_{CC} = 3.0 V to 5.5 V	– 0.5		0.3 V_{CC}	V

DC Characteristics

Symbol	Parameter	Conditions				CMiser = 1 Subtract:			Unit
			Min	Typ	Max	Min	Typ	Max	
V_{OL}	Output Low Voltage	I_{OL} = 20 µA V_{CC} = 3.0 V		0.01	0.1				V
		I_{OL} = 4 mA V_{CC} = 3.0 V		0.15	0.4				V
V_{OH}	Output High Voltage	I_{OH} = –20 µA V_{CC} = 3.0 V	2.9	2.99					V
		I_{OH} = –1 mA V_{CC} = 3.0 V	2.4	2.6					V
I_{SB1}	V_{CC} Standby Current (CMOS) (Notes 2 and 3)	V_{CC} = 3.3 V		1	5				µA
I_{CC1}	Active Current (CMOS) (No Internal Memory Block Selected) (Notes 2 and 5)	V_{CC} = 3.3 V (Note 5)		6	12		3.0	5	mA
		V_{CC} = 3.3 V (Note 6)		10	20		3.0	5	mA
I_{CC2}	Active Current (CMOS) (EPROM Block Selected) (Notes 2 and 5)	V_{CC} = 3.3 V (Notes 5 and 7)		6	12		0	0	mA
		V_{CC} = 3.3 V (Note 6 and 7)		10	20		0	0	mA
I_{CC3}	Active Current (CMOS) (SRAM Block Selected) (Notes 2 and 5)	V_{CC} = 3.3 V (Note 5 and 7)		20	33		3	5	mA
		V_{CC} = 3.3 V (Notes 6 and 7)		24	40		3	5	mA
I_{LI}	Input Leakage Current	V_{IN} = V_{CC} or GND	–1	±0.1	1				µA
I_{LO}	Output Leakage Current	V_{OUT} = V_{CC} or GND	–10	±5	10				µA

NOTES: 2. CMOS inputs: GND ± 0.3 V or V_{CC} ± 0.3V.
3. $\overline{CSI}$/A19 is high and the part is in a power-down configuration mode.
4. Add 2.0 mA/MHz for AC power component (power = AC + DC).
5. Ten (10) PAD product terms active. (Add 190 µA per product term, typical, or 240 µA per product term maximum.)
6. Forty (40) PAD product terms active.
7. In 8-bit mode, an additional 3 mA Max. can be saved under CMiser.

Figure 1. Normalized Supply Current vs. Supply Voltage



The Normalized Supply Current vs. Supply Voltage graph shown above, provides a multiplier for any I_{SB} or I_{CC} value in the D.C. Characteristics table. As noted, it is normalized for a supply voltage of 3.3 volts. Since device characterization data shows very little supply current difference over speed, the multiplier includes all frequencies of operation from standby to quiescent to full dynamic speed. To use, calculate the supply current at 3.3 volts for your operation configuration using the D.C. Characteristics table. Then multiply that value by the Supply Current Multiplier for the supply voltage actually being used.

AC Characteristics[8] (See Timing Diagrams)

Symbol	Parameter	-25		-30		CMiser = 1 Add:	Unit
		Min	Max	Min	Max		
T1	ALE or AS Pulse Width	75		80			ns
T2	Address Set-up Time	30		35			ns
T3	Address Hold Time	30		35		0	ns
T4	Leading Edge of Read to Data Active	0		0		0	ns
T5	ALE Valid to Data Valid		250		300	25	ns
T6	Address Valid to Data Valid		250		300	25	ns
T7	$\overline{CSI}$ Active to Data Valid		275		325	30	ns
T8	Leading Edge of Read to Data Valid		90		95	0	ns
T9	Read Data Hold Time	0		0		0	ns
T10	Trailing Edge of Read to Data High-Z		50		55	0	ns
T11	Trailing Edge of ALE or AS to Leading Edge of Write		40		45		ns
T12	$\overline{RD}$, E, $\overline{PSEN}$, $\overline{DS}$ Pulse Width	100		110		0	ns
T12A	$\overline{WR}$ Pulse Width	90		95		0	ns
T13	Trailing Edge of Write or Read to Leading Edge of ALE or AS	0		0		0	ns
T14	Address Valid to Trailing Edge of Write	250		300		0	ns
T15	$\overline{CSI}$ Active to Trailing Edge of Write	275		375		0	ns
T16	Write Data Set-up Time	60		65		0	ns
T17	Write Data Hold Time	25		30		0	ns
T18	Port to Data Out Valid Propagation Delay		70		75	0	ns
T19	Port Input Hold Time	0		0		0	ns
T20	Trailing Edge of Write to Port Output Valid	100		110		0	ns
T21	ADi or Control to $\overline{CSOi}$ Valid	6	80	5	85	0	ns
T22	ADi or Control to $\overline{CSOi}$ Invalid	4	80	4	85	0	ns
T23	Track Mode Address Propagation Delay: CSADOUT1 Already True		70		75	0	ns
T23A	Track Mode Address Propagation Delay: CSADOUT1 Becomes True During ALE or AS		100		110	0	ns

NOTE: 8. These AC Characteristics are for VCC = 3.0 – 3.6V.

AC Characteristics (Cont.)

Symbol	Parameter	-25		-30		CMiser = 1 Add:	Unit
		Min	Max	Min	Max		
T24	Track Mode Trailing Edge of ALE or AS to Address High-Z		60		65	0	ns
T25	Track Mode Read Propagation Delay		70		75	0	ns
T26	Track Mode Read Hold Time	10	70	10	75		ns
T27	Track Mode Write Cycle, Data Propagation Delay		60		65	0	ns
T28	Track Mode Write Cycle, Write to Data Propagation Delay	7	80	7	85	0	ns
T29	Hold Time of Port A Valid During Write $\overline{CSOi}$ Trailing Edge	4		4		0	ns
T30	$\overline{CSI}$ Active to $\overline{CSOi}$ Active	9	110	8	120	0	ns
T31	$\overline{CSI}$ Inactive to $\overline{CSOi}$ Inactive	9	110	8	120	0	ns
T32	Direct PAD Input as Hold Time	24		30		0	ns
T33	R/$\overline{W}$ Active to E or DS Start	60		65		0	ns
T34	E or $\overline{DS}$ End to R/$\overline{W}$	60		65		0	ns
T35	AS Inactive to E high	40		45		0	ns
T36	Address to Leading Edge of Write	50		60		0	ns

NOTES: 9. ADi = any address line.
10. $\overline{CSOi}$ = any of the chip-select output signals coming through Port B ($\overline{CS0}$–$\overline{CS7}$) or through Port C ($\overline{CS8}$–$\overline{CS10}$).
11. Direct PAD input = any of the following direct PAD input lines: $\overline{CSI}$/A19 as transparent A19, $\overline{RD}$/E/$\overline{DS}$, $\overline{WR}$ or R/$\overline{W}$, transparent PC0–PC2, ALE (or AS).
12. Control signals $\overline{RD}$/E/$\overline{DS}$ or $\overline{WR}$ or R/$\overline{W}$.

Figure 2. AC Testing Input/Output Waveform

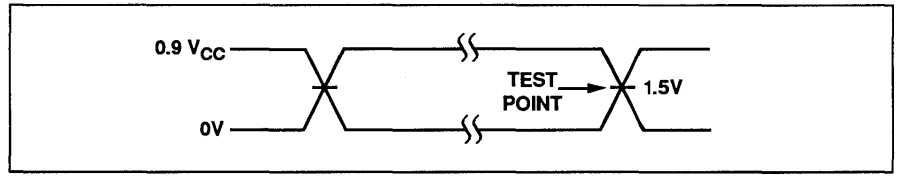


Figure 3. AC Testing Load Circuit

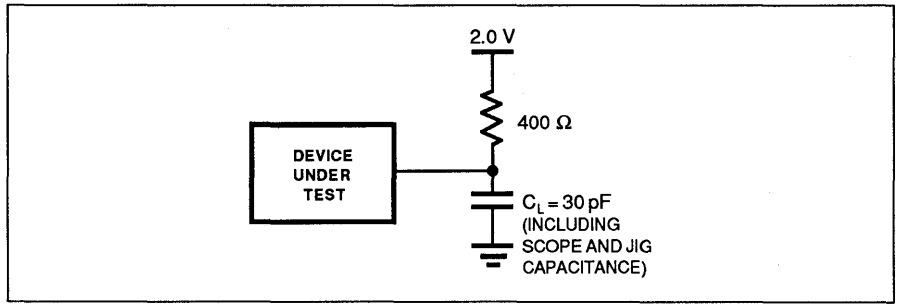


Figure 4. The Reset Cycle (RESET)

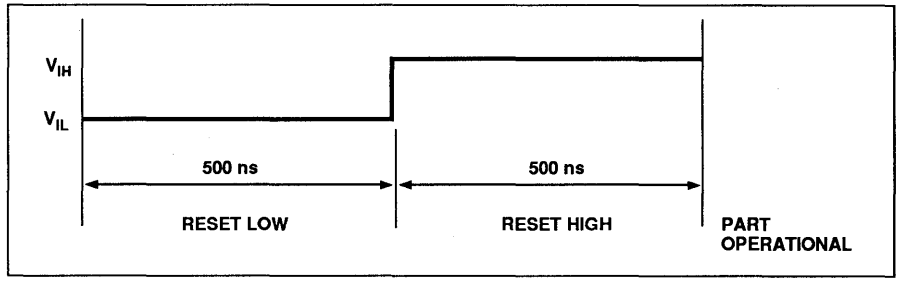
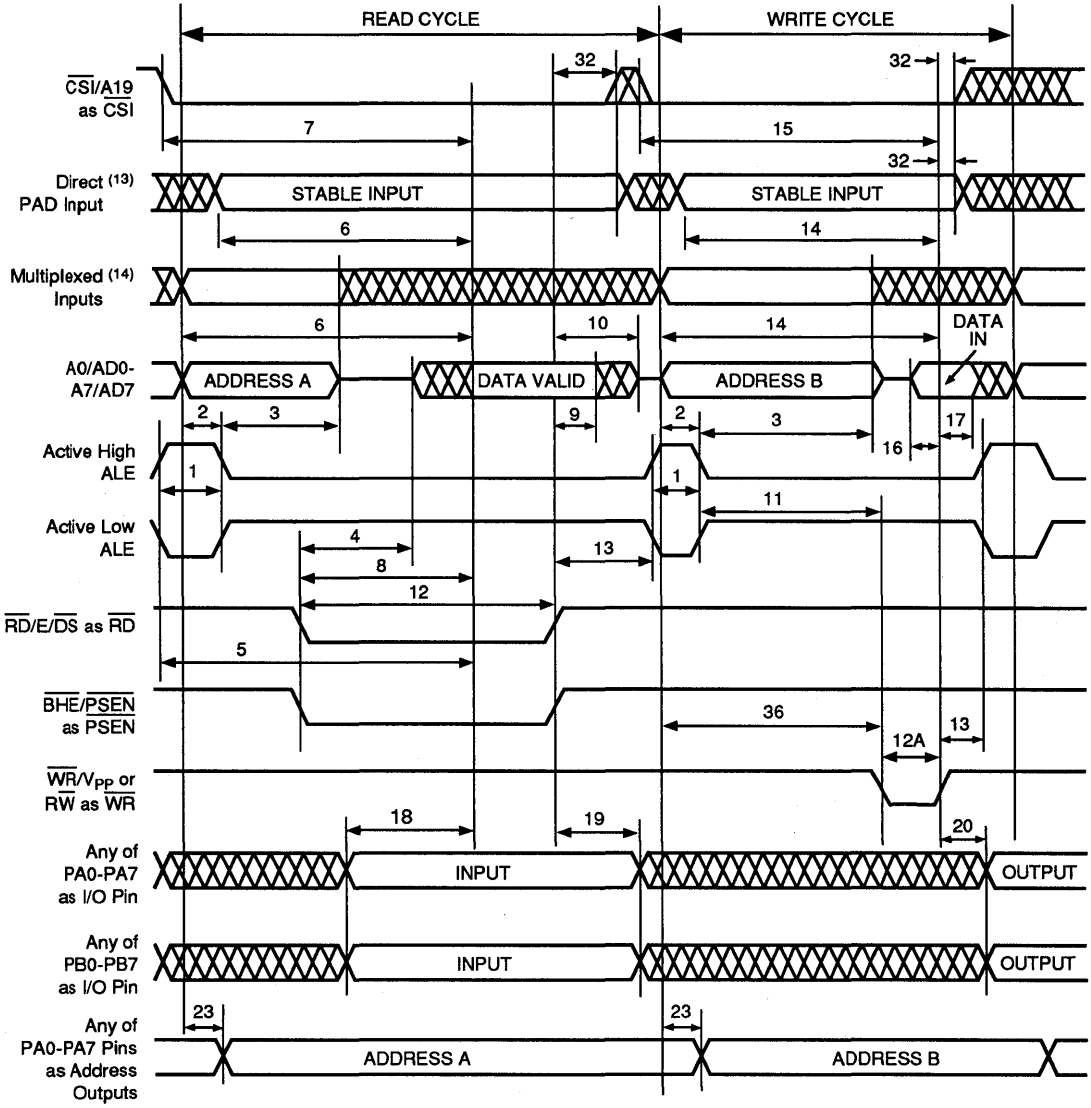
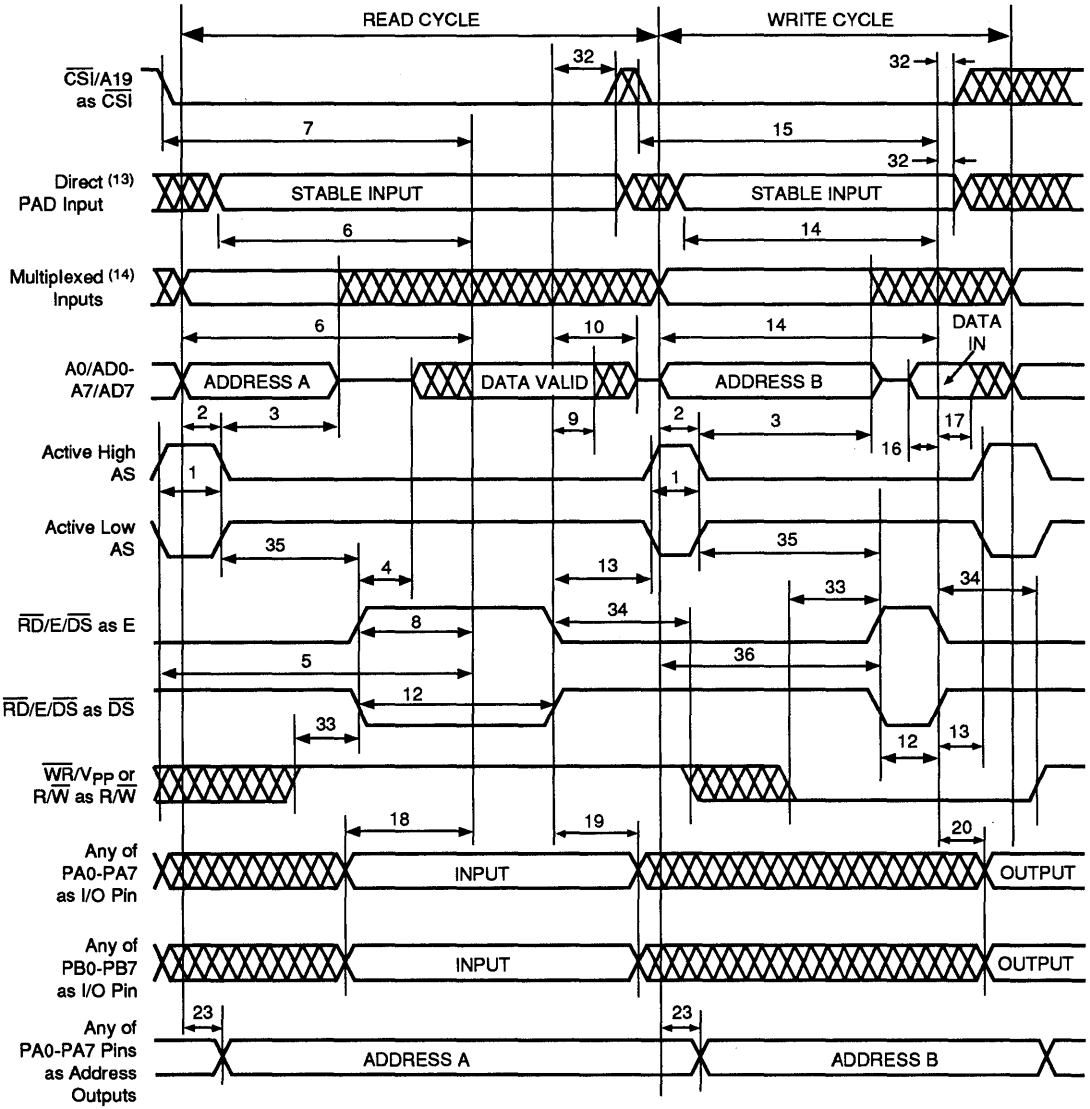


Figure 5. Timing of 8-Bit Multiplexed Address/Data Bus, CRRWR = 0



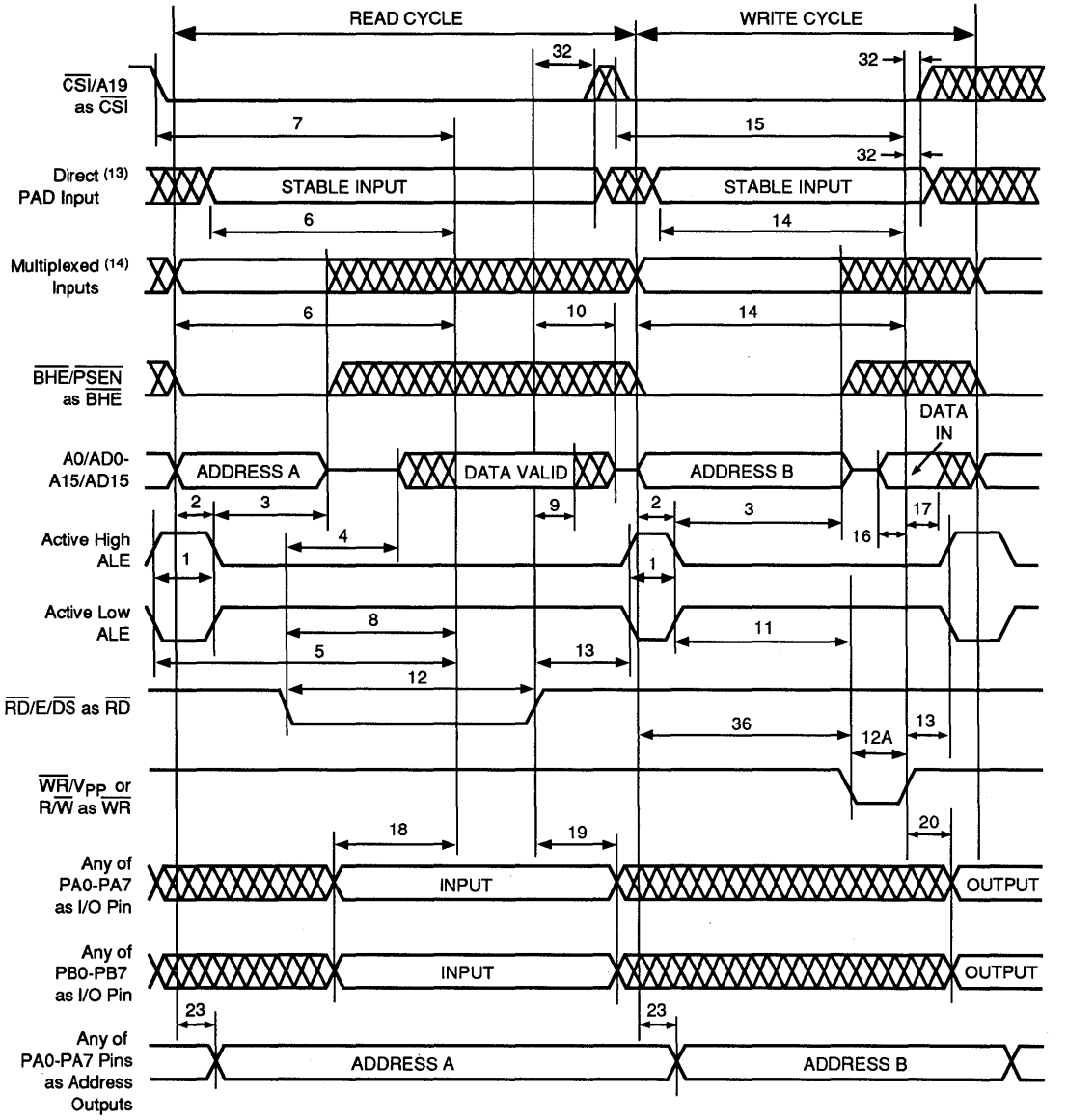
See referenced notes on page 278.

Figure 6. Timing of 8-Bit Multiplexed Address/Data Bus, CRRWR = 1



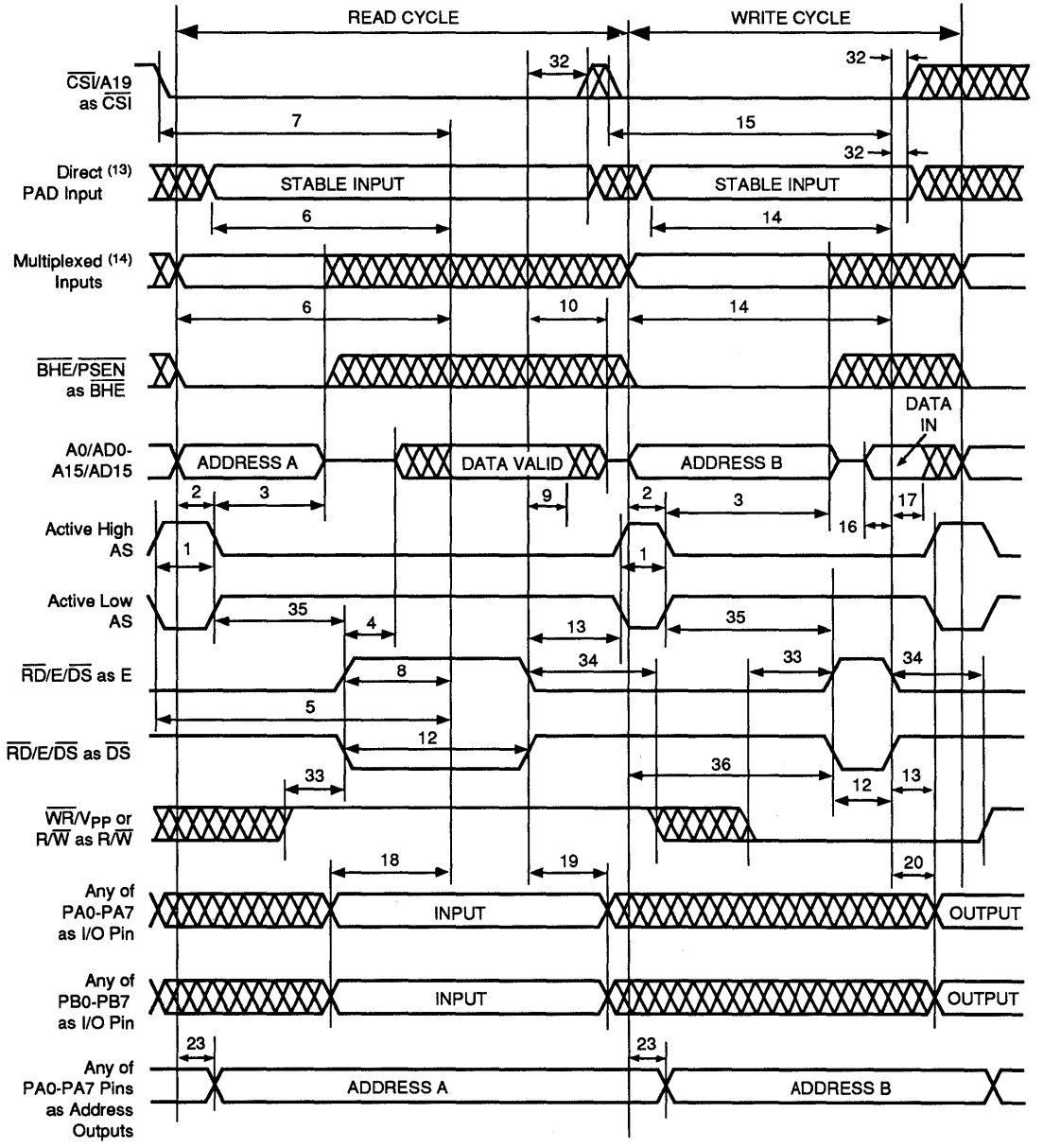
See referenced notes on page 278.

Figure 7. Timing of 16-Bit Multiplexed Address/Data Bus, CRRWR = 0



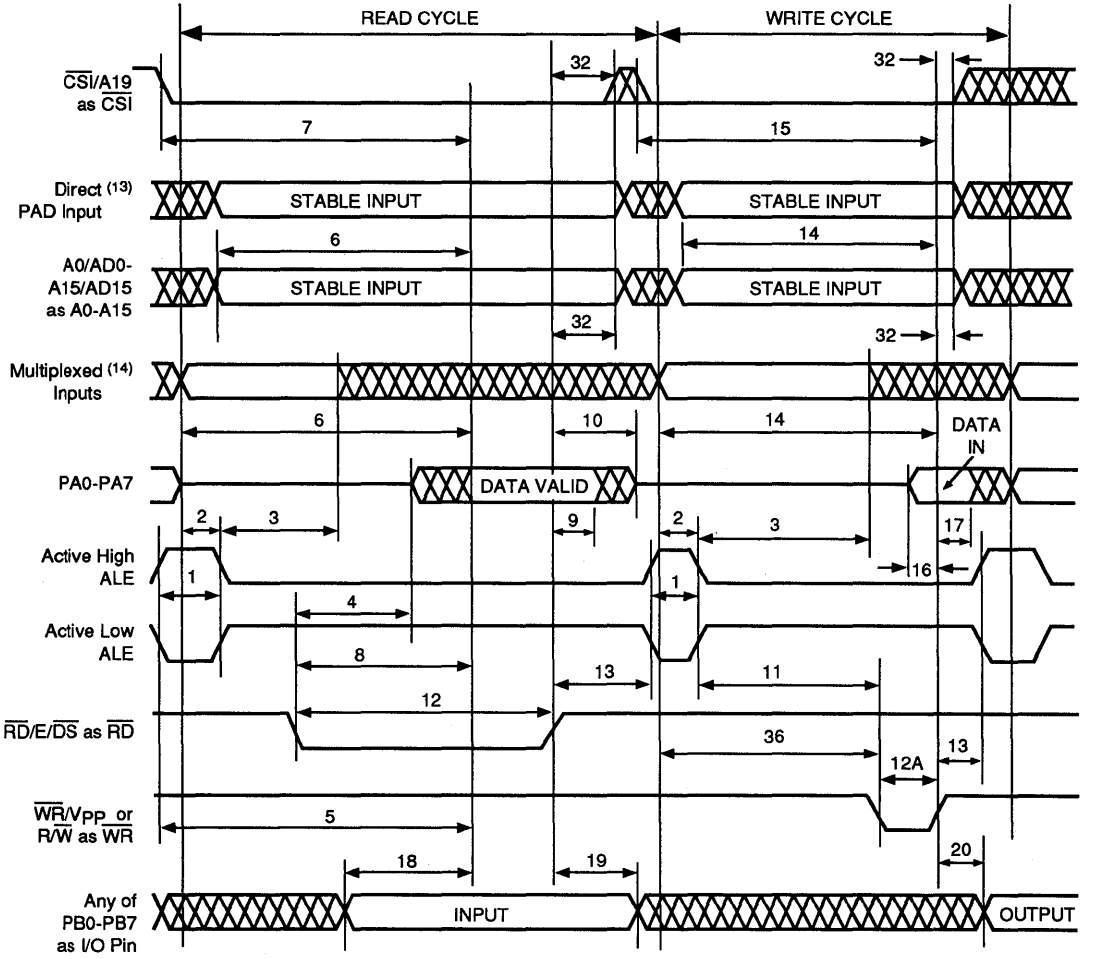
See referenced notes on page 278.

Figure 8. Timing of 16-Bit Multiplexed Address/Data Bus, CRRWR = 1



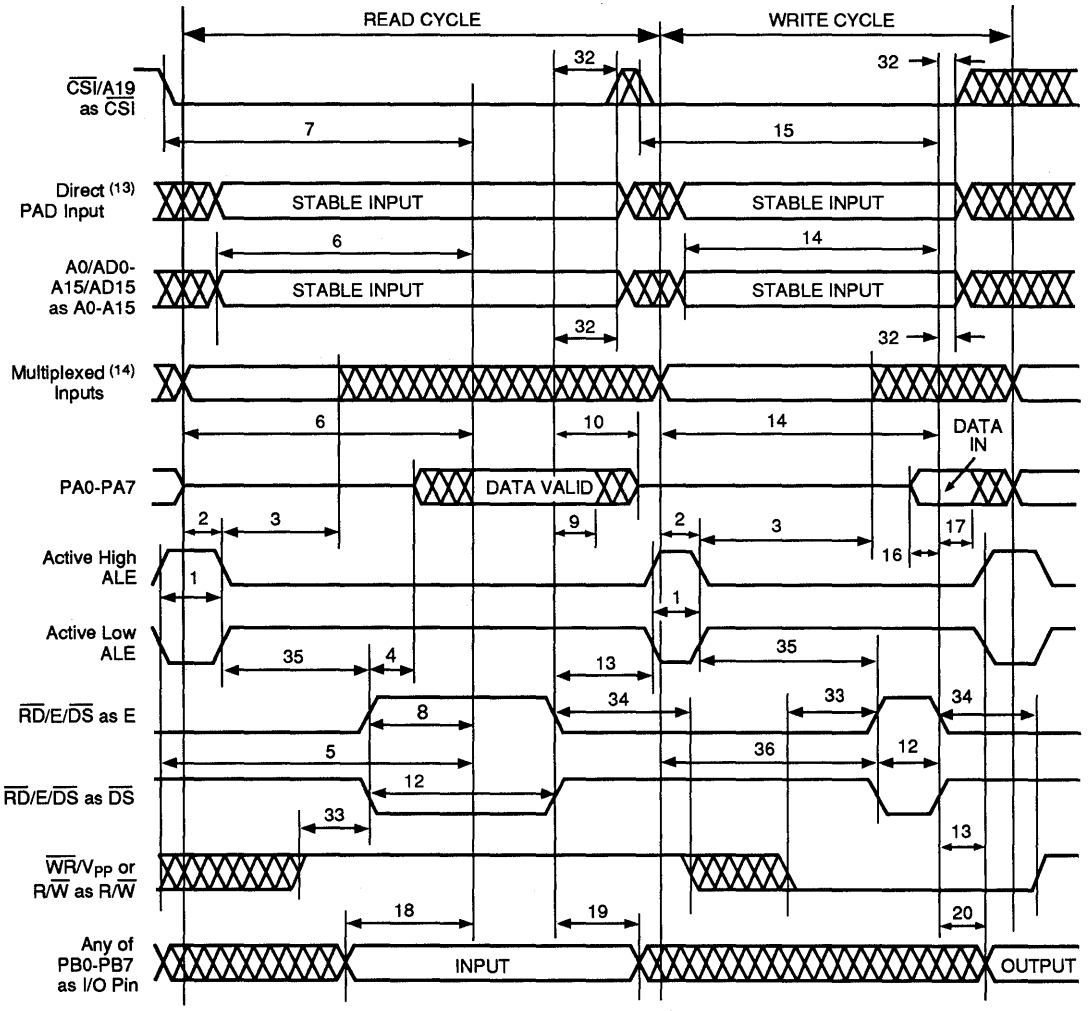
See referenced notes on page 278.

Figure 9. Timing of 8-Bit Data Non-Multiplexed Address/Data Bus, CRRWR = 0



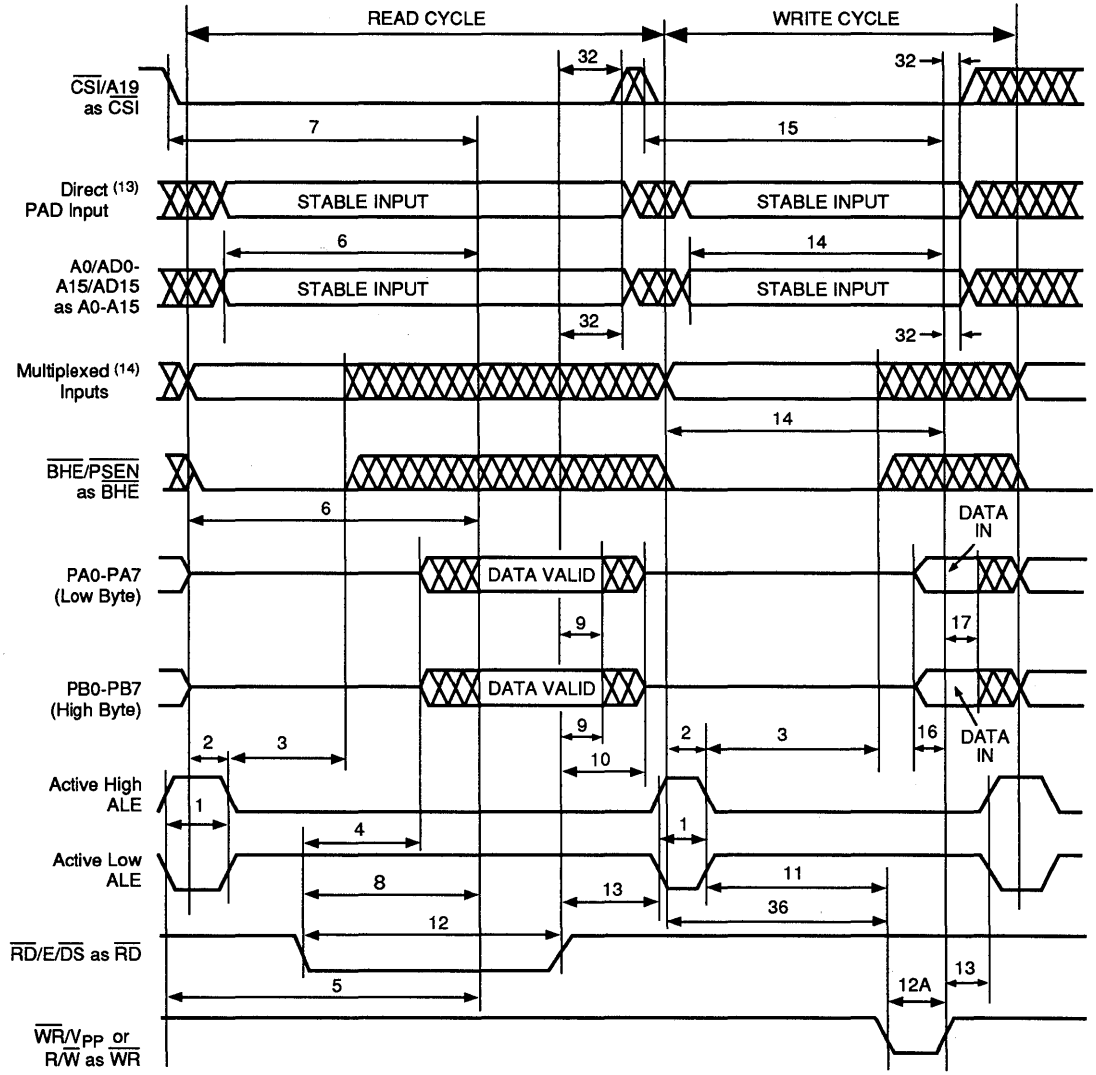
See referenced notes on page 278.

Figure 10. Timing of 8-Bit Data Non-Multiplexed Address/Data Bus, CRRWR = 1



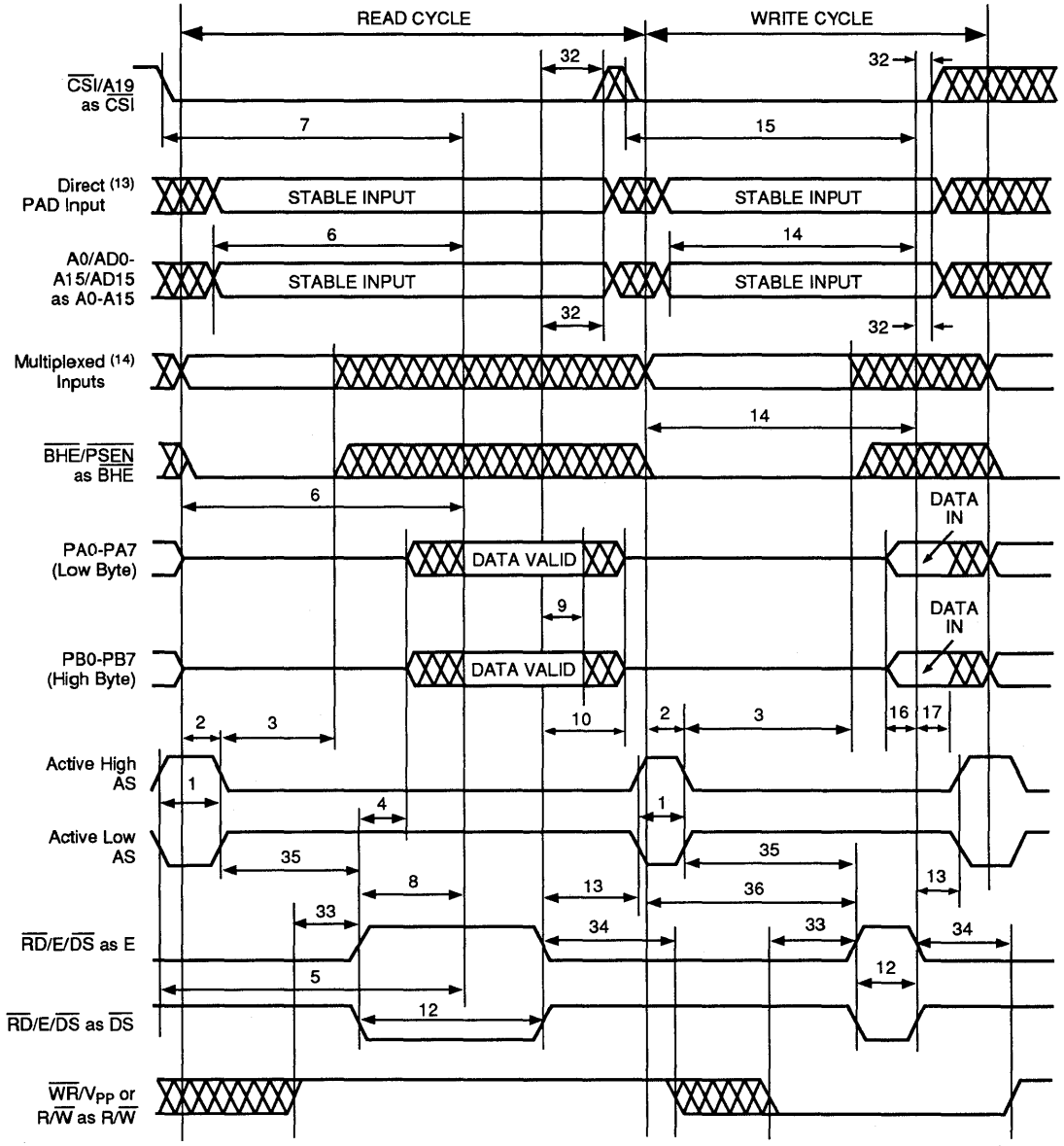
See referenced notes on page 278.

Figure 11. Timing of 16-Bit Non-Multiplexed Address/Data Bus, CRRWR = 0



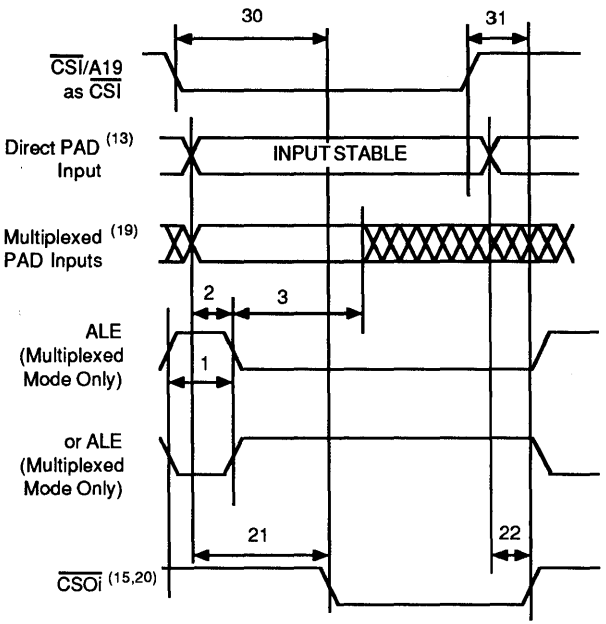
See referenced notes on page 278.

Figure 12. Timing of 16-Bit Non-Multiplexed Address/Data Bus, CRRWR = 1



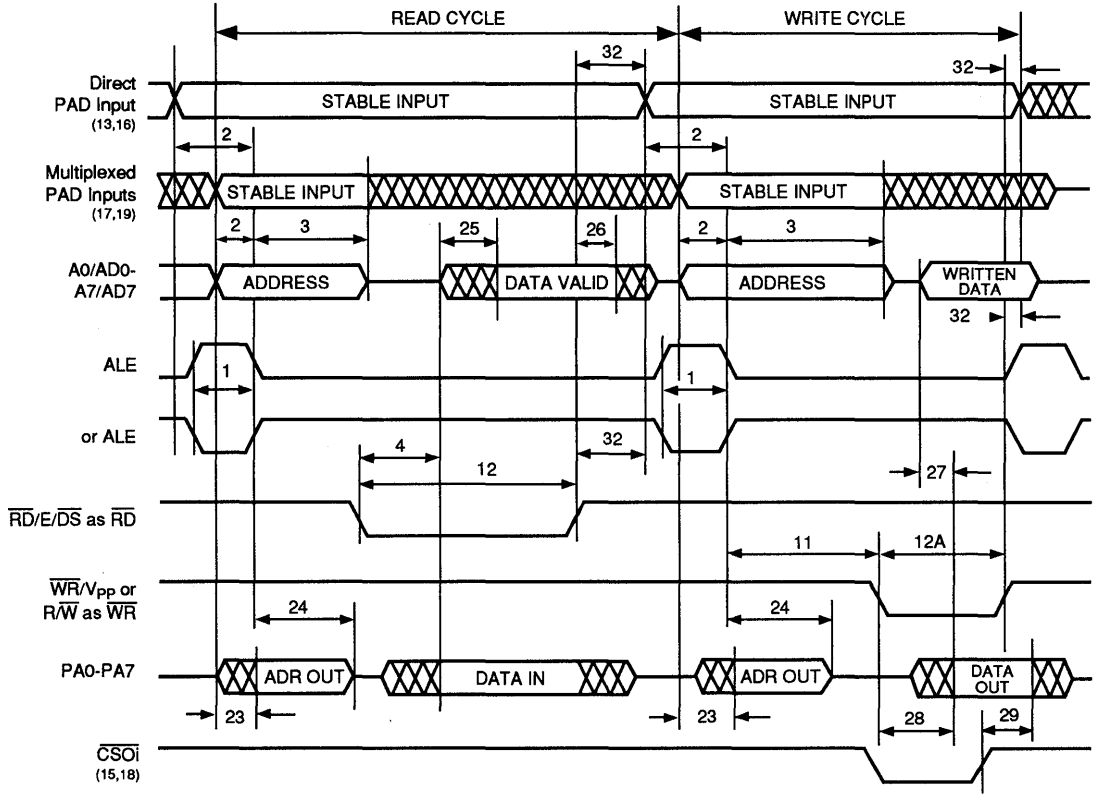
See referenced notes on page 278.

Figure 13. Chip-Select Output Timing



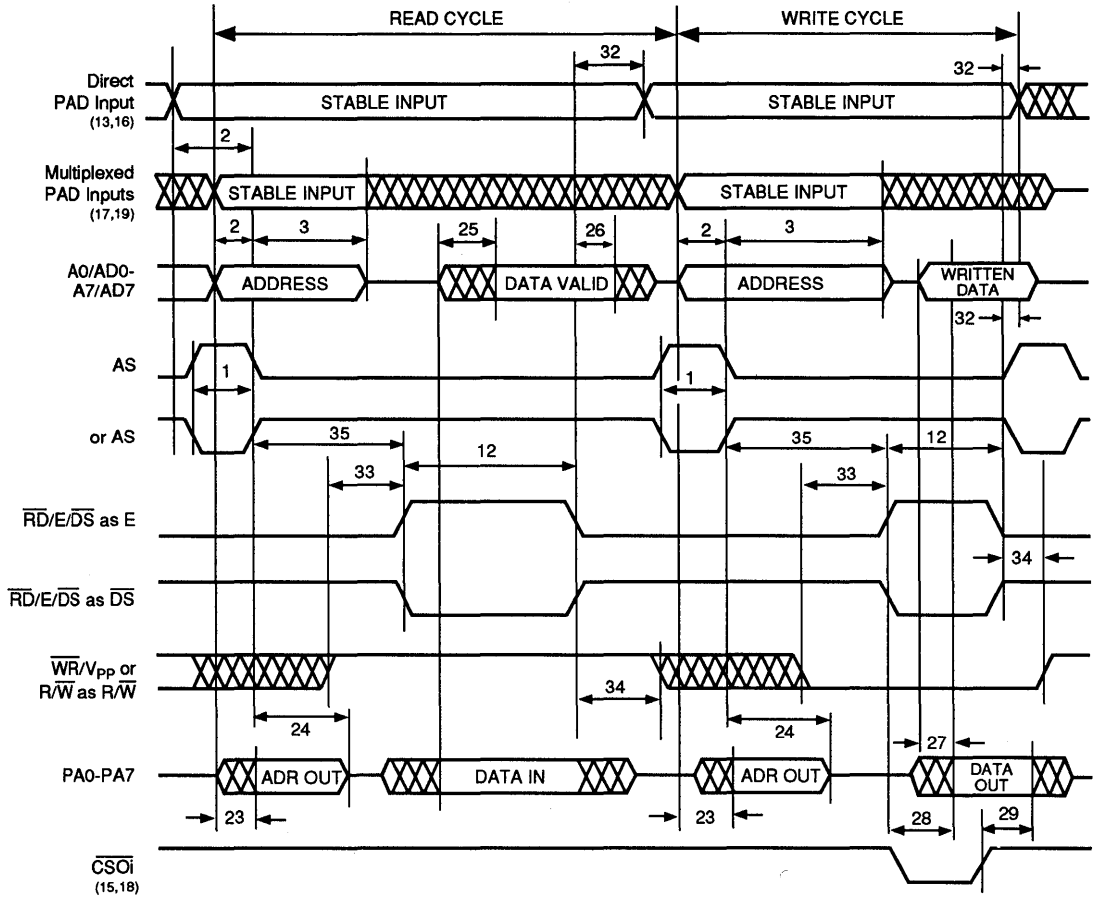
See referenced notes on page 278.

Figure 14. Port A as AD0 – AD7 Timing (Track Mode), CRRWR = 0



See referenced notes on page 278.

Figure 15. Port A as AD0 – AD7 Timing (Track Mode), CRRWR = 1



Notes for Timing Diagrams

13. Direct PAD input = any of the following direct PAD input lines: CSI/A19 as transparent A19, RD/E/DS, WR or R/W, transparent PC0–PC2, ALE in non-multiplexed modes.
14. Multiplexed inputs: any of the following inputs that are latched by the ALE (or AS): A0/AD0–A15/AD15, CSI/A19 as ALE dependent A19, ALE dependent PC0–PC2.
15. CSOi = any of the chip-select output signals coming through Port B (CS0–CS7) or through Port C (CS8–CS10).
16. CSADOUT1, which internally enables the address transfer to Port A, should be derived only from direct PAD input signals, otherwise the address propagation delay is slowed down.
17. CSADIN and CSADOUT2, which internally enable the data-in or data-out transfers, respectively, can be derived from any combination of direct PAD inputs and multiplexed PAD inputs.
18. The write operation signals are included in the CSOi expression.
19. Multiplexed PAD inputs: any of the following PAD inputs that are latched by the ALE (or AS) in the multiplexed modes: A11/AD11–A15/AD15, CSI/A19 as ALE dependent A19, ALE dependent PC0–PC2.
20. CSOi product terms can include any of the PAD input signals except for reset and CSI.

Pin Capacitance[21]

$T_A = 25\,°C, f = 1\,MHz$

Symbol	Parameter	Conditions	Typical[22]	Max	Unit
C_{IN}	Capacitance (for input pins only)	$V_{IN} = 0$ V	4	6	pF
C_{OUT}	Capacitance (for input/output pins)	$V_{OUT} = 0$ V	8	12	pF
C_{VPP}	Capacitance (for $\overline{WR}/V_{PP}$ or $R/\overline{W}/V_{PP}$)	$V_{PP} = 0$ V	18	25	pF

NOTES: 21. This parameter is only sampled and is not 100% tested.
22. Typical values are for $T_A = 25°C$ and nominal supply voltages.

Erasure and Programming

To clear all locations of their programmed contents, expose the device to ultra-violet light source. A dosage of 15 W second/cm² is required. This dosage can be obtained with exposure to a wavelength of 2537 Å and intensity of 12000 µW/cm² for 15 to 20 minutes. The device should be about 1 inch from the source, and all filters should be removed from the UV light source prior to erasure.

The PSD303L and similar devices will erase with light sources having wavelengths shorter than 4000 Å. Although the erasure times will be much longer than with UV sources at 2537 Å, exposure to fluorescent light and sunlight eventually erases the device. For maximum system reliability, these sources should be avoided. If used in such an environment, the package windows should be covered by an opaque substance.

Upon delivery, or after each erasure, the PSD303L device has all bits in the PAD and EPROM in the "1" or high state. The configuration bits are in the "0" or low state. The code, configuration, and PAD MAP data are loaded through the procedure of programming

Pin Assignments

Pin Name	44-Pin PLDCC/CLDCC Package
$\overline{BHE}/\overline{PSEN}$	1
$\overline{WR}/V_{PP}$ or $R/\overline{W}$	2
$\overline{RESET}$	3
PB7	4
PB6	5
PB5	6
PB4	7
PB3	8
PB2	9
PB1	10
PB0	11
GND	12
ALE or AS	13
PA7	14
PA6	15
PA5	16
PA4	17
PA3	18
PA2	19
PA1	20
PA0	21
$\overline{RD}/E/\overline{DS}$	22
AD0/A0	23
AD1/A1	24
AD2/A2	25
AD3/A3	26
AD4/A4	27
AD5/A5	28
AD6/A6	29
AD7/A7	30
AD8/A8	31
AD9/A9	32
AD10/A10	33
GND	34
AD11/A11	35
AD12/A12	36
AD13/A13	37
AD14/A14	38
AD15/A15	39
PC0	40
PC1	41
PC2	42
A19/$\overline{CSI}$	43
V_{CC}	44

Package Information

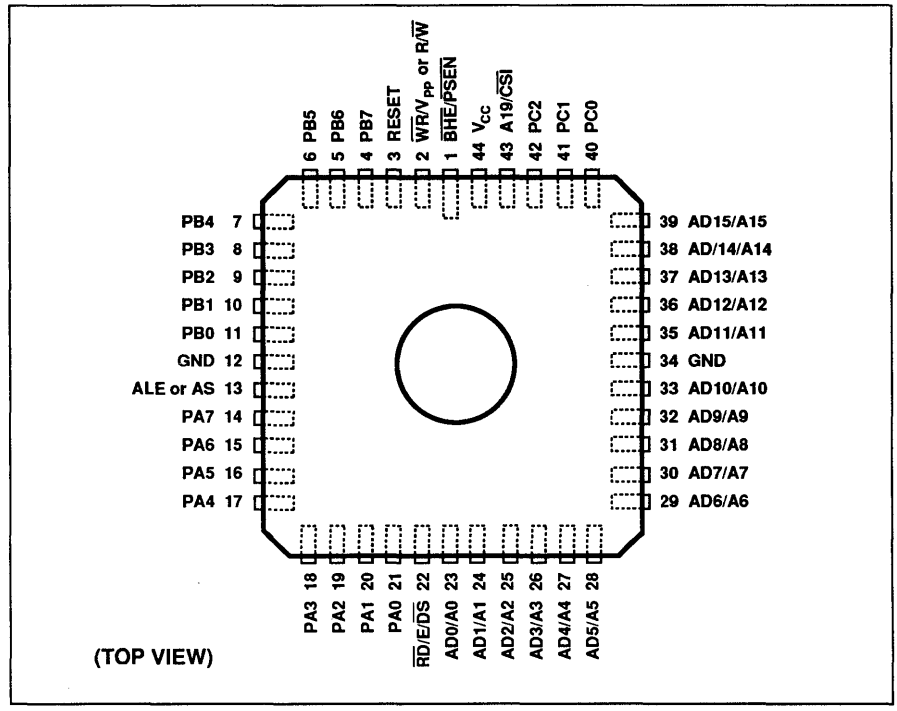


Figure 16. Drawing L4 — 44 Pin Ceramic Leaded Chip Carrier (CLCC) with Window (Package Type L)

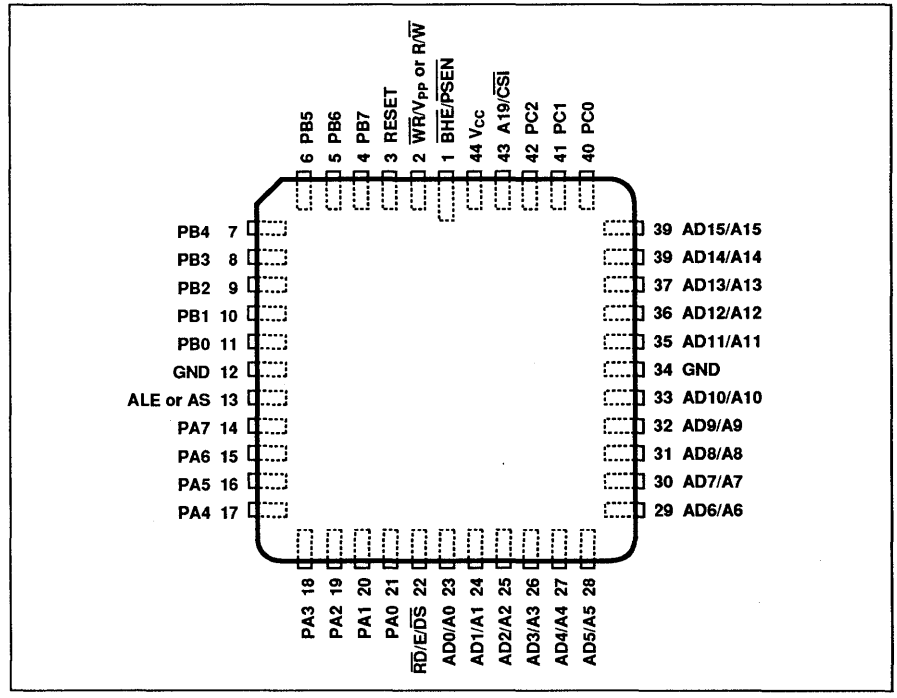


Figure 17. Drawing J2 — 44 Pin Plastic Leaded Chip Carrier (PLCC) (Package Type J)

Ordering Information

Part Number	Spd. (ns)	Package Type	Package Drawing	Operating Temperature Range	Manufacturing Procedure
PSD303L25 A	250	44-pin PLCC	J2	Commercial	Standard
PSD303L25 KA	250	44-pin CLCC	L4	Commercial	Standard
PSD303L30 A	300	44-pin PLCC	J2	Commercial	Standard
PSD303L30 KA	300	44-pin CLCC	L4	Commercial	Standard

3-volt single-chip microcontroller peripheral — PSD313L

Key Features

- ❑ Single Chip Programmable Peripheral for Microcontroller-based Applications
- ❑ 3.0 to 5.5 Volt Operation
- ❑ 19 Individually Configurable I/O pins that can be used as:
  - — Microcontroller I/O port expansion
  - — Programmable Address Decoder (PAD) I/O
  - — Latched address output
  - — Open drain or CMOS
- ❑ Two Programmable Arrays (PAD A & PAD B)
  - — Total of 40 Product Terms and up to 18 Inputs and 24 Outputs
  - — Direct Address Decoding up to 1 Meg address space and up to 16 Meg with paging
  - — Logic replacement
- ❑ "No Glue" Microcontroller Chip-Set
  - — Built-in address latches for multiplexed address/data bus
  - — Non-multiplexed address/data bus mode
  - — 8-bit data bus width
  - — ALE and Reset polarity programmable
  - — Selectable modes for read and write control bus as $\overline{RD}/\overline{WR}$, R/$\overline{W}$/E, or R/$\overline{W}$/$\overline{DS}$
  - — $\overline{PSEN}$ pin for 8051 users
- ❑ Built-In Page Logic
  - — To Expand the Address Space of Microcontrollers with Limited Address Space Capabilities
  - — Up to 16 pages
- ❑ 1M bit of UV EPROM
  - — Configurable as 128K x 8
  - — Divides into 8 equal mappable blocks for optimized mapping
  - — Block resolution is 16K x 8
  - — 250 ns EPROM access time, including input latches and PAD address decoding.
- ❑ 16 Kbit Static RAM
  - — Configurable as 2K x 8
  - — 250 ns SRAM access time, including input latches and PAD address decoding
- ❑ Address/Data Track Mode
  - — Enables easy Interface to Shared Resources (e.g., Mail Box SRAM) with other Microcontrollers or a Host Processor
- ❑ CMiser-Bit
  - — Programmable option to further reduce power consumption
- ❑ Built-In Security
  - — Locks the PSD313L and PAD Decoding Configuration
- ❑ Available in a Choice of Packages
  - — 44 Pin PLDCC and CLDCC
- ❑ Simple Menu-Driven Software: Configure the PSD313L on an IBM PC
- ❑ Pin and Functionally Compatible with the PSD3XX and PSD3XXL Series

Absolute Maximum Ratings[1]

Symbol	Parameter	Condition	Min	Max	Unit
T_{STG}	Storage Temperature	CERAMIC	−65	+150	°C
		PLASTIC	−65	+125	°C
T_{STG}	Storage Temperature		−65	+150	°C
	Voltage on any Pin	With Respect to GND	−0.6	+7	V
V_{PP}	Programming Supply Voltage	With Respect to GND	−0.6	+14	V
V_{CC}	Supply Voltage	With Respect to GND	−0.6	+7	V
	ESD Protection			>2000	V

NOTE: 1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods of time may affect device reliability.

Operating Range

Range	Temperature	V_{CC}
Commercial	0° C to +70°C	3.0 V to 5.5 V

Recommended Operating Conditions

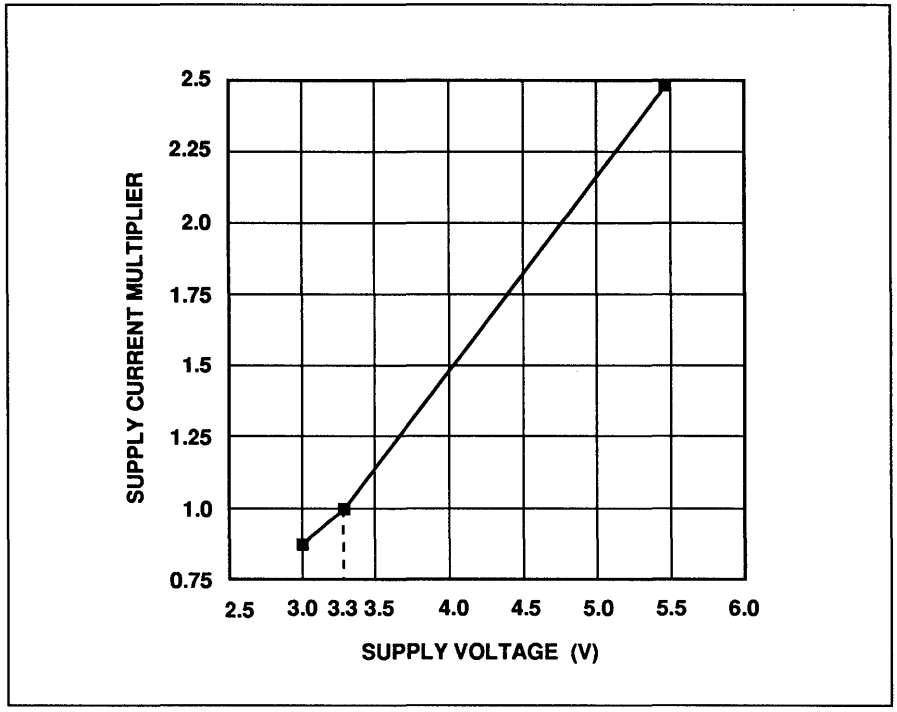
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	Supply Voltage	All Speeds	3.0	3.3	5.5	V
V_{IH}	High-level Input Voltage	V_{CC} = 3.0 V to 5.5 V	0.7 V_{CC}		V_{CC} + 0.5	V
V_{IL}	Low-level Input Voltage	V_{CC} = 3.0 V to 5.5 V	−0.5		0.3 V_{CC}	V

DC Characteristics

Symbol	Parameter	Conditions				CMiser = 1 Subtract:			Unit
			Min	Typ	Max	Min	Typ	Max	
V_{OL}	Output Low Voltage	I_{OL} = 20 µA V_{CC} = 3.0 V		0.01	0.1				V
		I_{OL} = 4 mA V_{CC} = 3.0 V		0.15	0.4				V
V_{OH}	Output High Voltage	I_{OH} = –20 µA V_{CC} = 3.0 V	2.9	2.99					V
		I_{OH} = –1 mA V_{CC} = 3.0 V	2.4	2.6					V
I_{SB1}	V_{CC} Standby Current (CMOS) (Notes 2 and 3)	V_{CC} = 3.3 V		1	5				µA
I_{CC1}	Active Current (CMOS) (No Internal Memory Block Selected) (Notes 2 and 5)	V_{CC} = 3.3 V (Note 5)		6	12		3.0	5	mA
		V_{CC} = 3.3 V (Note 6)		10	20		3.0	5	mA
I_{CC2}	Active Current (CMOS) (EPROM Block Selected) (Notes 2 and 5)	V_{CC} = 3.3 V (Note 5)		6	12		2	3	mA
		V_{CC} = 3.3 V (Note 6)		10	20		2	3	mA
I_{CC3}	Active Current (CMOS) (SRAM Block Selected) (Notes 2 and 5)	V_{CC} = 3.3 V (Note 5)		20	33		5	8	mA
		V_{CC} = 3.3 V (Note 6)		24	40		5	8	mA
I_{LI}	Input Leakage Current	V_{IN} = V_{CC} or GND	–1	±0.1	1				µA
I_{LO}	Output Leakage Current	V_{OUT} = V_{CC} or GND	–10	±5	10				µA

NOTES: 2. CMOS inputs: GND ± 0.3 V or V_{CC} ± 0.3V.
3. $\overline{CSI}$/A19 is high and the part is in a power-down configuration mode.
4. Add 2.0 mA/MHz for AC power component (power = AC + DC).
5. Ten (10) PAD product terms active. (Add 190 µA per product term, typical, or 240 µA per product term maximum.)
6. Forty (40) PAD product terms active.

Figure 1. Normalized Supply Current vs. Supply Voltage



The Normalized Supply Current vs. Supply Voltage graph shown above, provides a multiplier for any I_{SB} or I_{CC} value in the D.C. Characteristics table. As noted, it is normalized for a supply voltage of 3.3 volts. Since device characterization data shows very little supply current difference over speed, the multiplier includes all frequencies of operation from standby to quiescent to full dynamic speed. To use, calculate the supply current at 3.3 volts for your operation configuration using the D.C. Characteristics table. Then multiply that value by the Supply Current Multiplier for the supply voltage actually being used.

AC Characteristics[8] (See Timing Diagrams)

Symbol	Parameter	-25		-30		CMiser = 1 Add:	Unit
		Min	Max	Min	Max		
T1	ALE or AS Pulse Width	75		80			ns
T2	Address Set-up Time	30		35			ns
T3	Address Hold Time	30		35		0	ns
T4	Leading Edge of Read to Data Active	0		0		0	ns
T5	ALE Valid to Data Valid		250		300	25	ns
T6	Address Valid to Data Valid		250		300	25	ns
T7	$\overline{CSI}$ Active to Data Valid		275		325	30	ns
T8	Leading Edge of Read to Data Valid		90		95	0	ns
T9	Read Data Hold Time	0		0		0	ns
T10	Trailing Edge of Read to Data High-Z		50		55	0	ns
T11	Trailing Edge of ALE or AS to Leading Edge of Write		40		45		ns
T12	$\overline{RD}$, E, $\overline{PSEN}$, $\overline{DS}$ Pulse Width	100		110		0	ns
T12A	$\overline{WR}$ Pulse Width	90		95		0	ns
T13	Trailing Edge of Write or Read to Leading Edge of ALE or AS	0		0		0	ns
T14	Address Valid to Trailing Edge of Write	250		300		0	ns
T15	$\overline{CSI}$ Active to Trailing Edge of Write	275		375		0	ns
T16	Write Data Set-up Time	60		65		0	ns
T17	Write Data Hold Time	25		30		0	ns
T18	Port to Data Out Valid Propagation Delay		70		75	0	ns
T19	Port Input Hold Time	0		0		0	ns
T20	Trailing Edge of Write to Port Output Valid	100		110		0	ns
T21	ADi or Control to $\overline{CSOi}$ Valid	6	80	5	85	0	ns
T22	ADi or Control to $\overline{CSOi}$ Invalid	4	80	4	85	0	ns
T23	Track Mode Address Propagation Delay: CSADOUT1 Already True		70		75	0	ns
T23A	Track Mode Address Propagation Delay: CSADOUT1 Becomes True During ALE or AS		100		110	0	ns

NOTE: 8. These AC Characteristics are for VCC = 3.0 – 3.6V.

AC Characteristics (Cont.)

Symbol	Parameter	-25		-30		CMiser = 1 Add:	Unit
		Min	Max	Min	Max		
T24	Track Mode Trailing Edge of ALE or AS to Address High-Z		60		65	0	ns
T25	Track Mode Read Propagation Delay		70		75	0	ns
T26	Track Mode Read Hold Time	10	70	10	75		ns
T27	Track Mode Write Cycle, Data Propagation Delay		60		65	0	ns
T28	Track Mode Write Cycle, Write to Data Propagation Delay	7	80	7	85	0	ns
T29	Hold Time of Port A Valid During Write $\overline{CSOi}$ Trailing Edge	4		4		0	ns
T30	$\overline{CSI}$ Active to $\overline{CSOi}$ Active	9	110	8	120	0	ns
T31	$\overline{CSI}$ Inactive to $\overline{CSOi}$ Inactive	9	110	8	120	0	ns
T32	Direct PAD Input as Hold Time	24		30		0	ns
T33	R/$\overline{W}$ Active to E or $\overline{DS}$ Start	60		65		0	ns
T34	E or $\overline{DS}$ End to R/W	60		65		0	ns
T35	AS Inactive to E high	40		45		0	ns
T36	Address to Leading Edge of Write	50		60		0	ns

NOTES: 9. ADi = any address line.
10. $\overline{CSOi}$ = any of the chip-select output signals coming through Port B ($\overline{CS0}$–$\overline{CS7}$) or through Port C ($\overline{CS8}$–$\overline{CS10}$).
11. Direct PAD input = any of the following direct PAD input lines: $\overline{CSI}$/A19 as transparent A19, $\overline{RD}$/E/$\overline{DS}$, $\overline{WR}$ or R/$\overline{W}$, transparent PC0–PC2, ALE (or AS).
12. Control signals $\overline{RD}$/E/$\overline{DS}$ or $\overline{WR}$ or R/$\overline{W}$.

Figure 2. AC Testing Input/Output Waveform

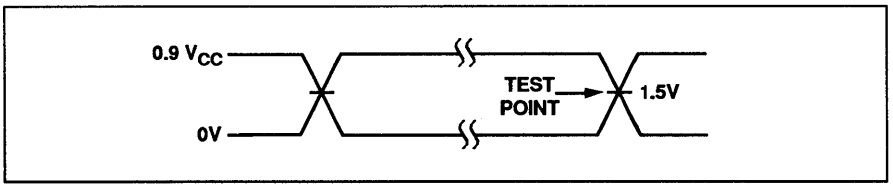


Figure 3. AC Testing Load Circuit

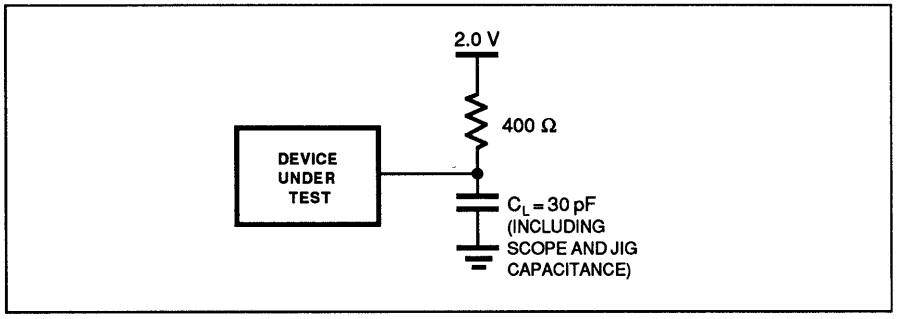


Figure 4. The Reset Cycle (RESET)

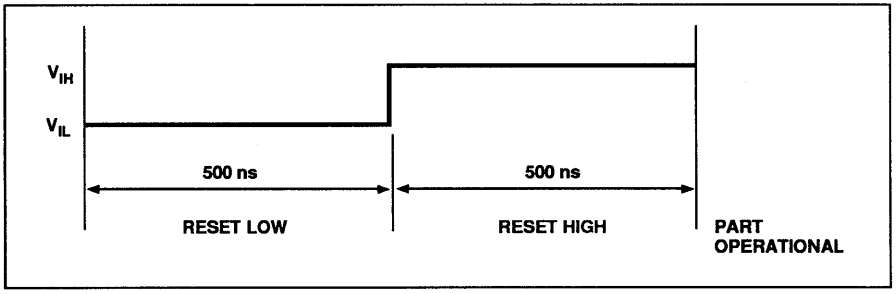
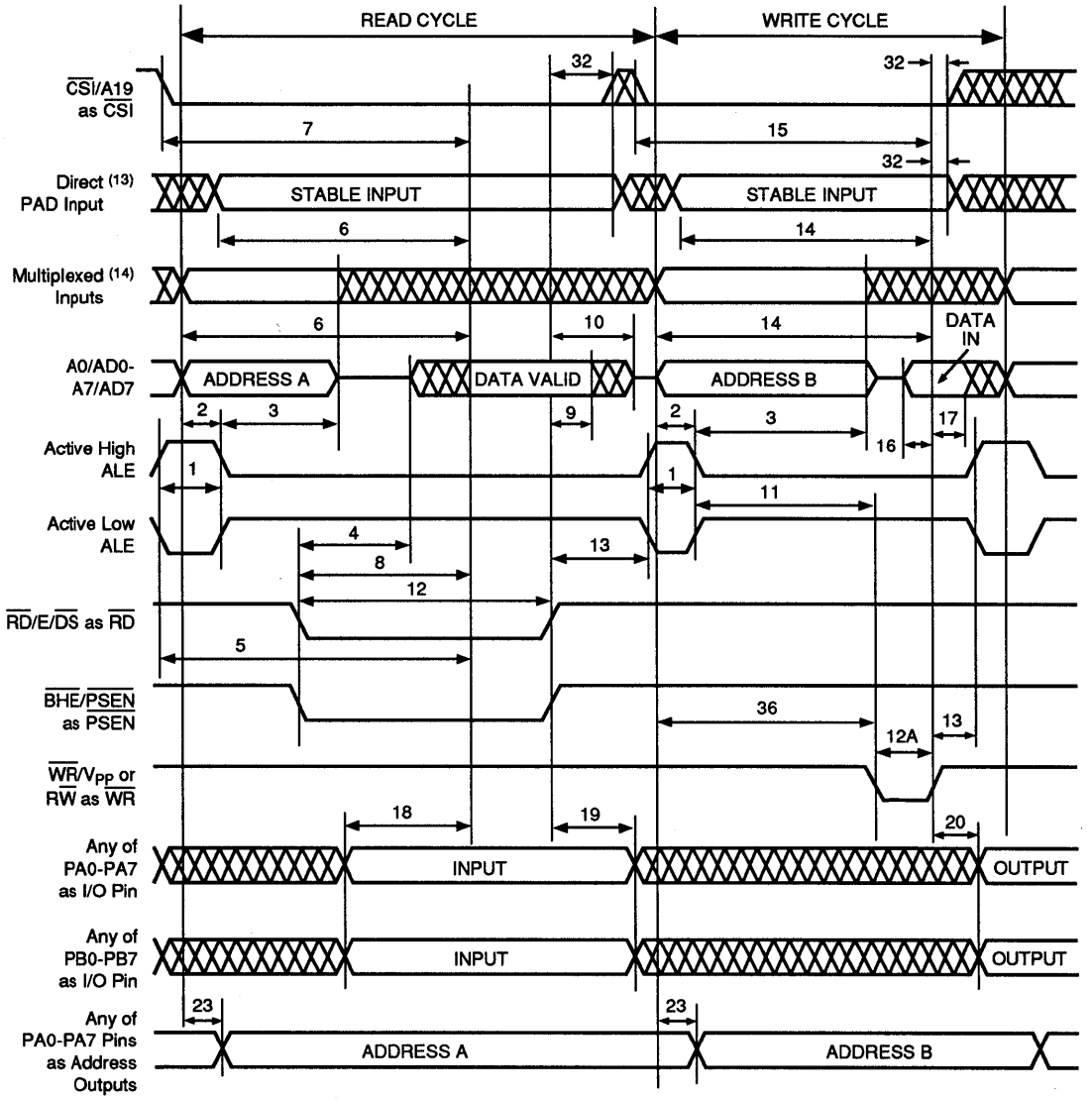
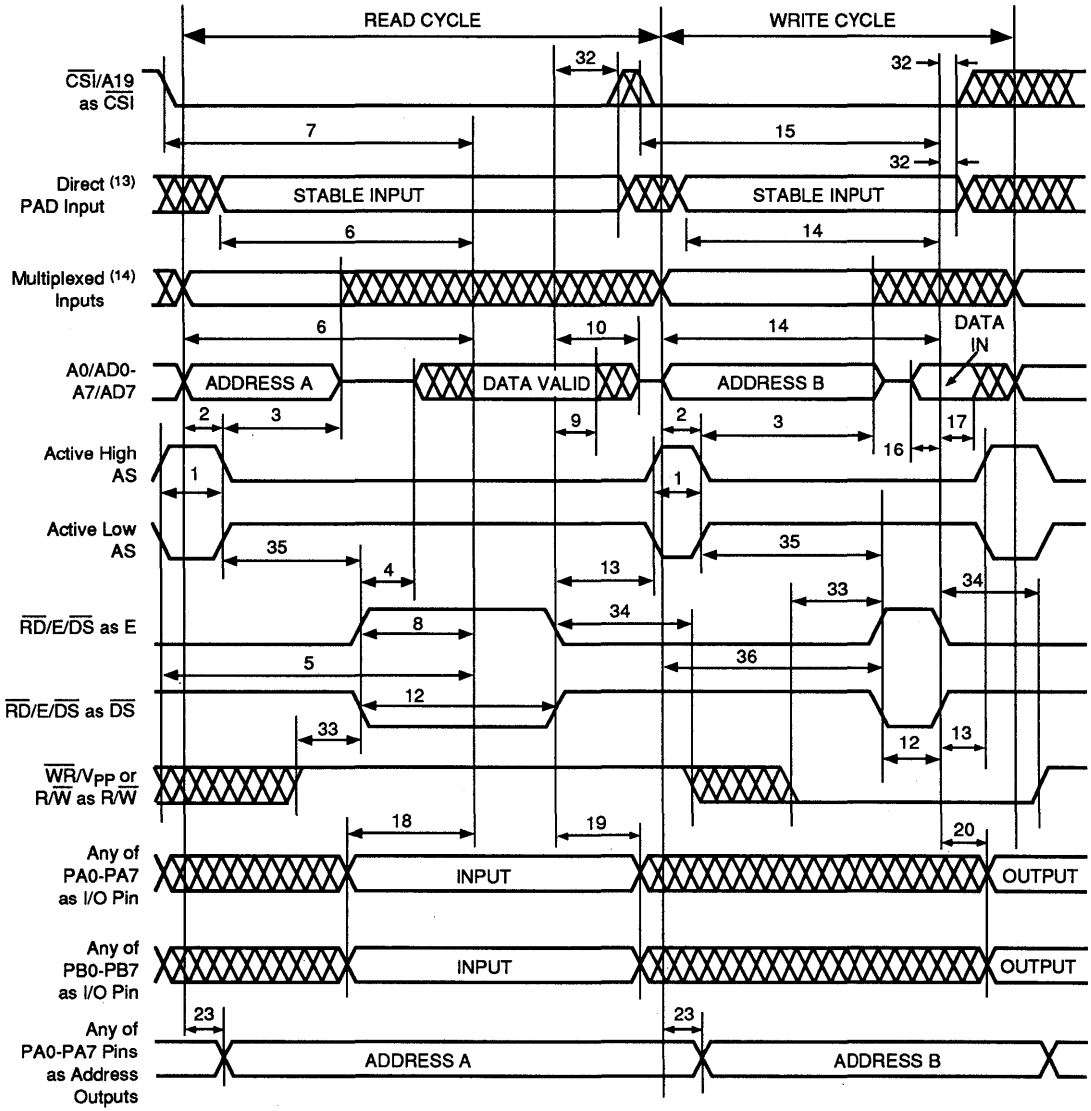


Figure 5. Timing of 8-Bit Multiplexed Address/Data Bus, CRRWR = 0



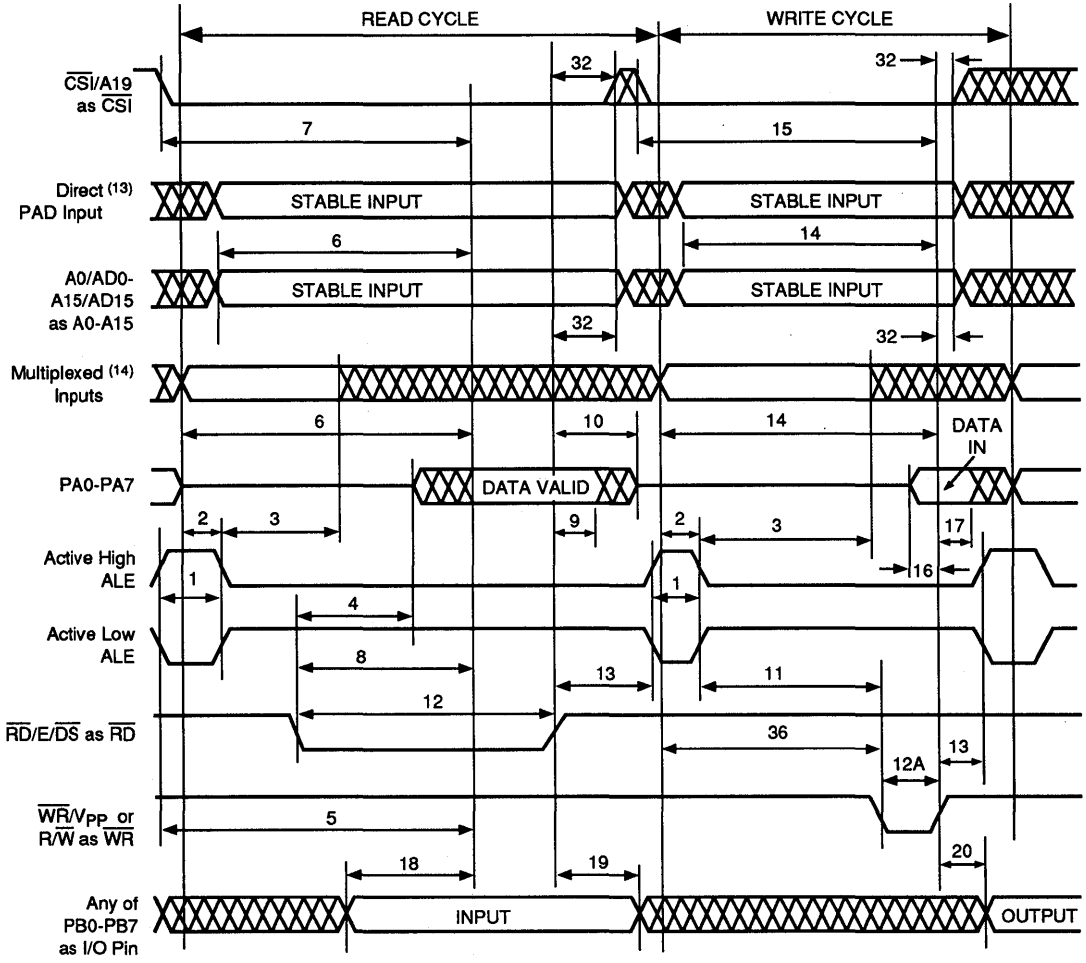
See referenced notes on page 296.

Figure 6. Timing of 8-Bit Multiplexed Address/Data Bus, CRRWR = 1



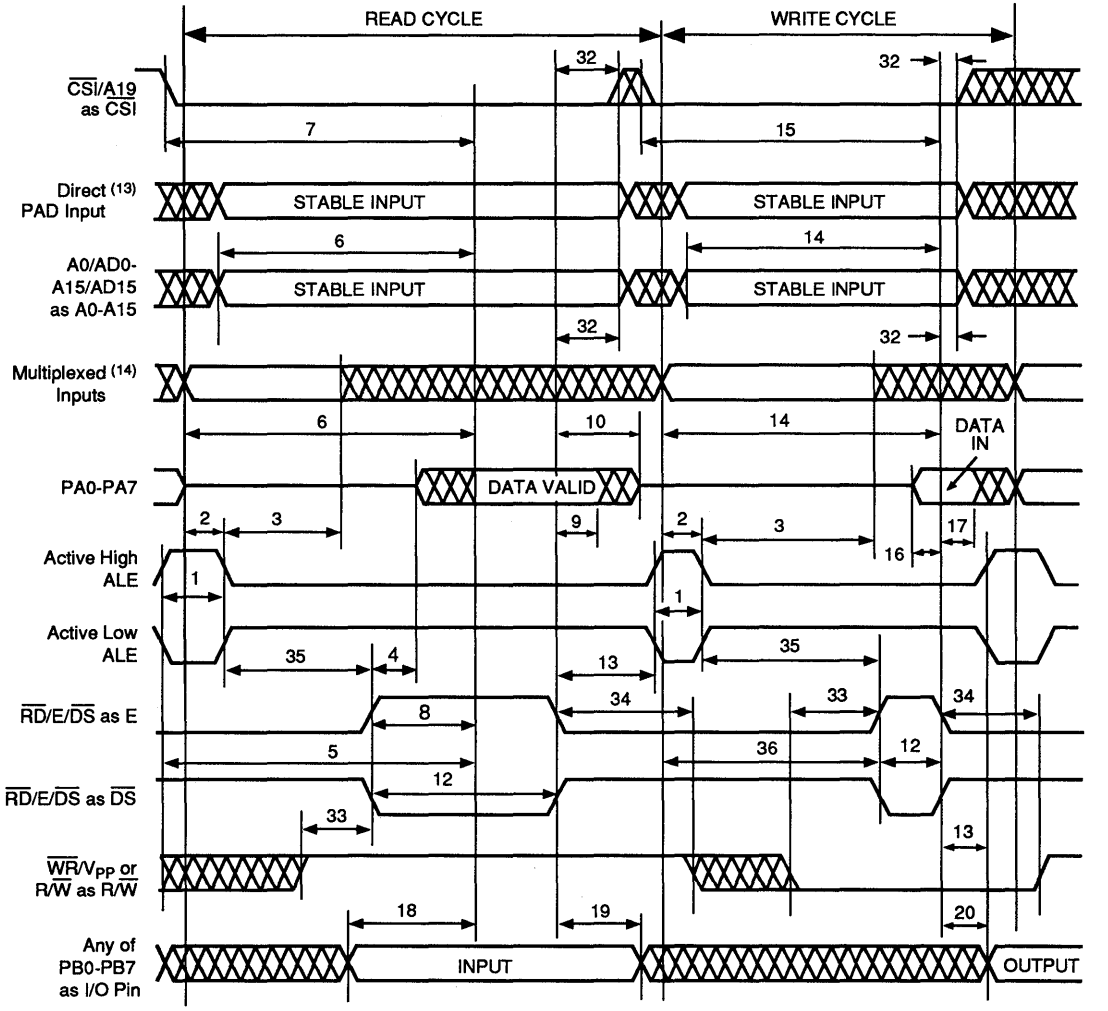
See referenced notes on page 296.

Figure 7. Timing of 8-Bit Data Non-Multiplexed Address/Data Bus, CRRWR = 0



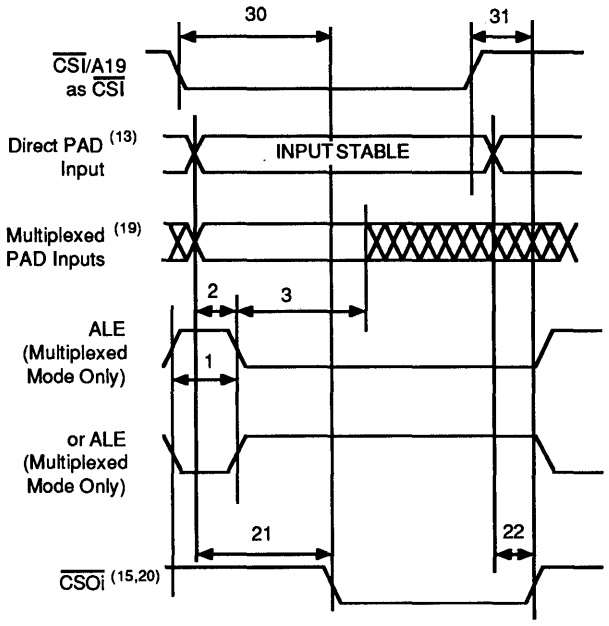
See referenced notes on page 296.

Figure 8. Timing of 8-Bit Data Non-Multiplexed Address/Data Bus, CRRWR = 1



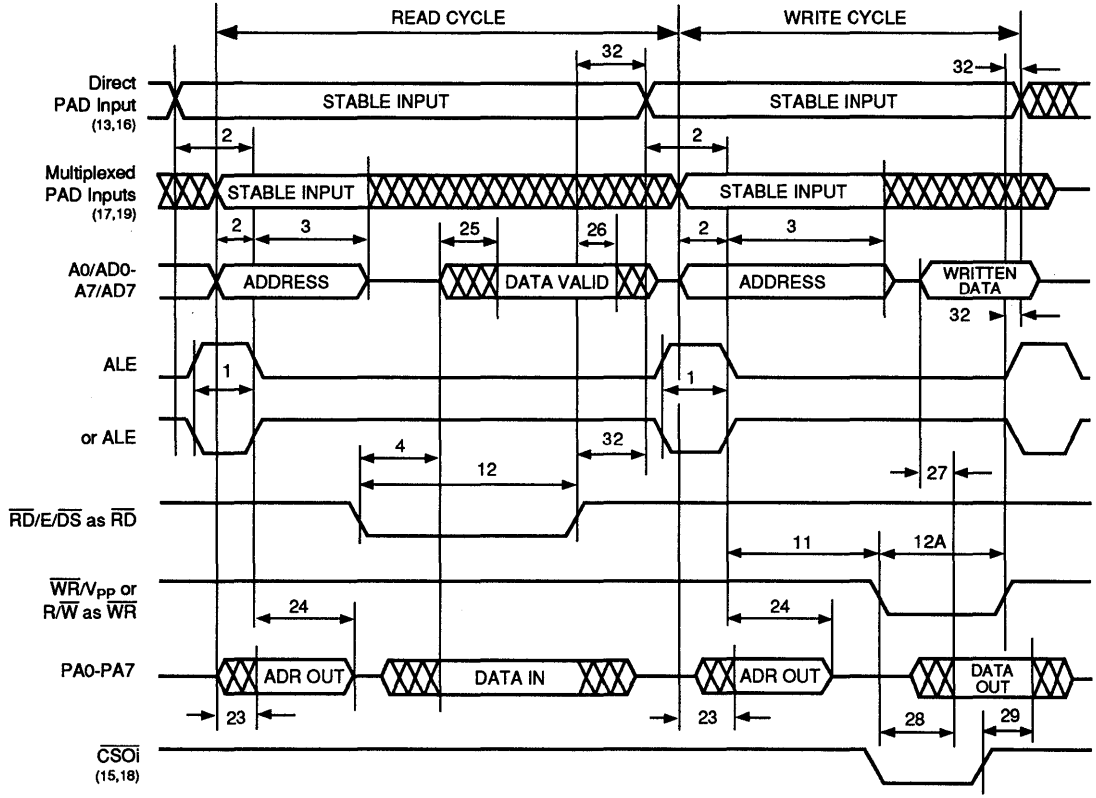
See referenced notes on page 296.

Figure 9. Chip-Select Output Timing



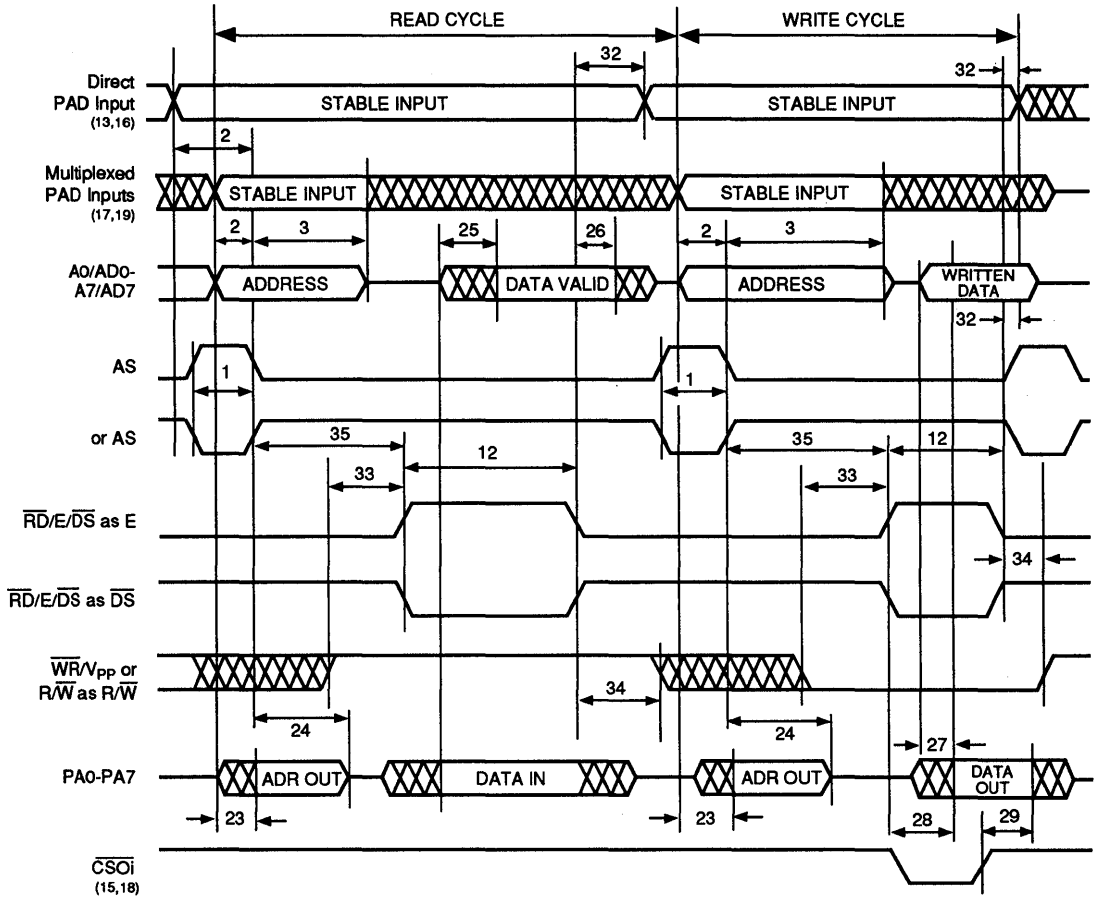
See referenced notes on page 296.

Figure 10. Port A as AD0 – AD7 Timing (Track Mode), CRRWR = 0



See referenced notes on page 296.

Figure 11. Port A as AD0 – AD7 Timing (Track Mode), CRRWR = 1



Notes for Timing Diagrams

13. Direct PAD input = any of the following direct PAD input lines: CSI/A19 as transparent A19, RD/E/DS, WR or R/W, transparent PC0–PC2, ALE in non-multiplexed modes.
14. Multiplexed inputs: any of the following inputs that are latched by the ALE (or AS): A0/AD0–A15/AD15, CSI/A19 as ALE dependent A19, ALE dependent PC0–PC2.
15. CSOi = any of the chip-select output signals coming through Port B (CS0–CS7) or through Port C (CS8–CS10).
16. CSADOUT1, which internally enables the address transfer to Port A, should be derived only from direct PAD input signals, otherwise the address propagation delay is slowed down.
17. CSADIN and CSADOUT2, which internally enable the data-in or data-out transfers, respectively, can be derived from any combination of direct PAD inputs and multiplexed PAD inputs.
18. The write operation signals are included in the CSOi expression.
19. Multiplexed PAD inputs: any of the following PAD inputs that are latched by the ALE (or AS) in the multiplexed modes: A11/AD11–A15/AD15, CSI/A19 as ALE dependent A19, ALE dependent PC0–PC2.
20. CSOi product terms can include any of the PAD input signals except for reset and CSI.

Pin Capacitance[21]

$T_A = 25\,°C, f = 1\,MHz$

Symbol	Parameter	Conditions	Typical[22]	Max	Unit
C_{IN}	Capacitance (for input pins only)	$V_{IN} = 0$ V	4	6	pF
C_{OUT}	Capacitance (for input/output pins)	$V_{OUT} = 0$ V	8	12	pF
C_{VPP}	Capacitance (for $\overline{WR}/V_{PP}$ or $R/\overline{W}/V_{PP}$)	$V_{PP} = 0$ V	18	25	pF

NOTES: 21. This parameter is only sampled and is not 100% tested.
22. Typical values are for $T_A = 25°C$ and nominal supply voltages.

Erasure and Programming

To clear all locations of their programmed contents, expose the device to ultra-violet light source. A dosage of 15 W second/cm^2 is required. This dosage can be obtained with exposure to a wavelength of 2537 Å and intensity of 12000 μW/cm^2 for 15 to 20 minutes. The device should be about 1 inch from the source, and all filters should be removed from the UV light source prior to erasure.

The PSD313L and similar devices will erase with light sources having wavelengths shorter than 4000 Å. Although the erasure times will be much longer than with UV sources at 2537 Å, exposure to fluorescent light and sunlight eventually erases the device. For maximum system reliability, these sources should be avoided. If used in such an environment, the package windows should be covered by an opaque substance.

Upon delivery, or after each erasure, the PSD313L device has all bits in the PAD and EPROM in the "1" or high state. The configuration bits are in the "0" or low state. The code, configuration, and PAD MAP data are loaded through the procedure of programming

Pin Assignments

Pin Name	44-Pin PLDCC/CLDCC Package
$\overline{PSEN}$	1
$\overline{WR}/V_{PP}$ or R/$\overline{W}$	2
$\overline{RESET}$	3
PB7	4
PB6	5
PB5	6
PB4	7
PB3	8
PB2	9
PB1	10
PB0	11
GND	12
ALE or AS	13
PA7	14
PA6	15
PA5	16
PA4	17
PA3	18
PA2	19
PA1	20
PA0	21
$\overline{RD}$/E/$\overline{DS}$	22
AD0/A0	23
AD1/A1	24
AD2/A2	25
AD3/A3	26
AD4/A4	27
AD5/A5	28
AD6/A6	29
AD7/A7	30
A8	31
A9	32
A10	33
GND	34
A11	35
A12	36
A13	37
A14	38
A15	39
PC0	40
PC1	41
PC2	42
A19/$\overline{CSI}$	43
V_{CC}	44

Package Information

Figure 12. Drawing L4 — 44 Pin Ceramic Leaded Chip Carrier (CLCC) with Window (Package Type L)

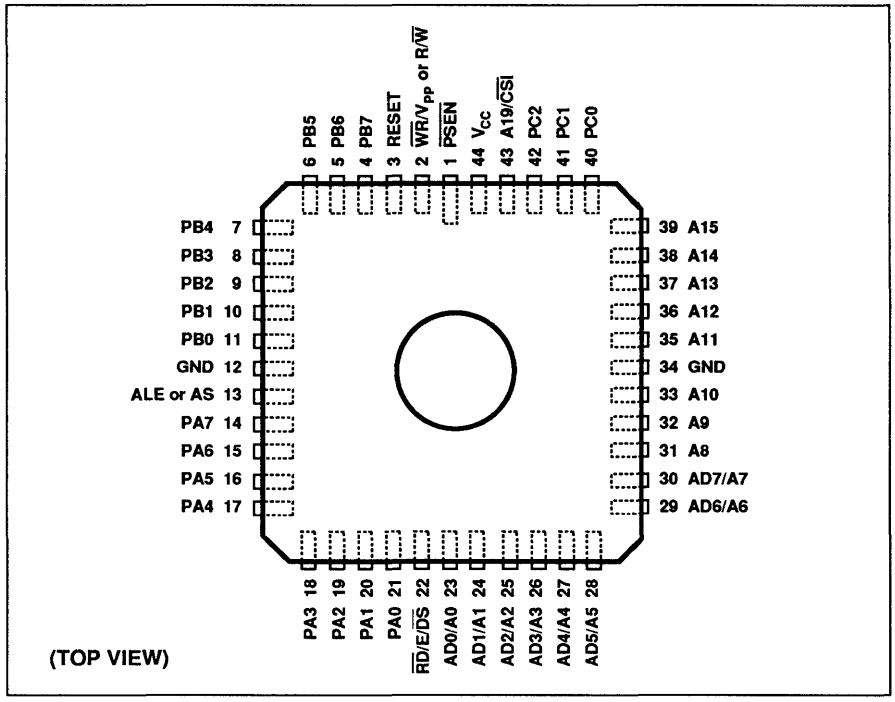
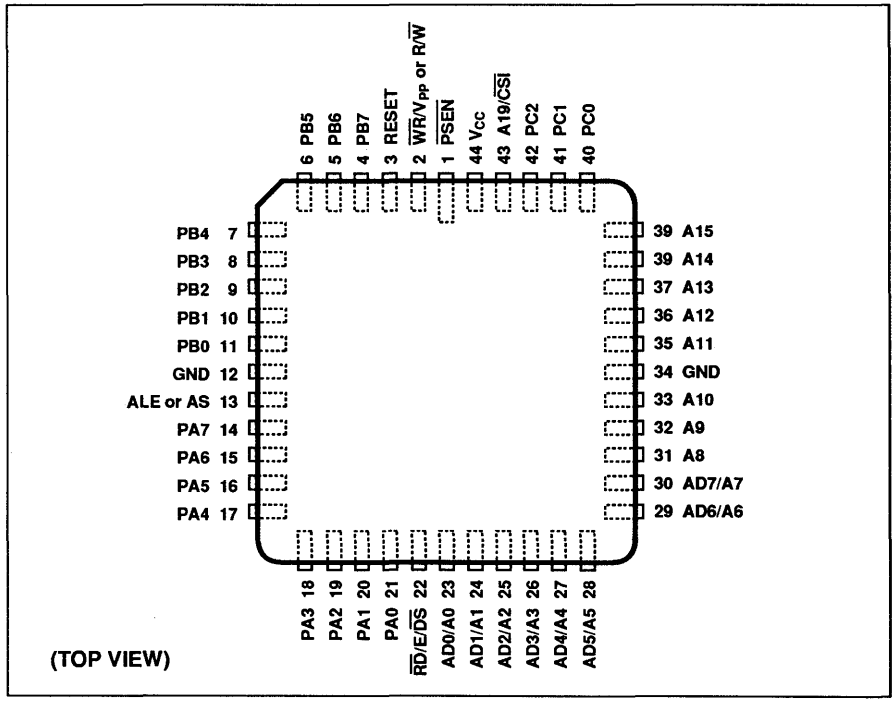


Figure 13. Drawing J2 — 44-Pin Plastic Leaded Chip Carrier (PLCC) (Package Type J)



Ordering Information

Part Number	Spd. (ns)	Package Type	Package Drawing	Operating Temperature Range	Manufacturing Procedure
PSD313L25 A	250	44-pin PLCC	J2	Commercial	Standard
PSD313L25 KA	250	44-pin CLCC	L4	Commercial	Standard
PSD313L30 A	300	44-pin PLCC	J2	Commercial	Standard
PSD313L30 KA	300	44-pin CLCC	L4	Commercial	Standard

Section 3
Application Notes

PSD3XX Programmable Microcontroller Peripherals

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PSD3XX Device Description PSD3XX

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Figures (Cont.)

Tables

Chapter 1

Introduction

The PSD3XX family of products include flexible I/O ports, PLD, Page Register, 256K to 1M EPROM, 16K bit SRAM and "Glueless" Logic Interface to the micro controller. The PSD3XX is ideal for microcontroller based applications where fast time-to-market, small form factor and low power consumption are essential. These applications include disk controllers, cellular phones, modems, fax machines, medical instrumentation, industrial control, automotive engine control and many others.

Traditionally, central processing units (CPUs) require the support of non-volatile memory for program storage, random access memory (RAM) for data storage, and some input/output (I/O) capability to communicate with external devices. The addition of general logic circuitry is necessary to 'glue' the parts of the system together. Figure 1 shows a block diagram of such a system, configured with a CPU (or microprocessor). The typical microprocessor also has integrated into it on-board timers, a small amount of RAM and ROM, as well as a limited I/O capability.

The microprocessor (and often the microcontroller) requires additional external support EPROM and RAM memory, additional ports, memory mapping logic, and sometimes latches to separate address and data from a multiplexed address/data bus. Until very recently, designers had to create a discrete solution from a number of chips, or generate a full custom solution. Now, the PSD3XX integrates the different system support blocks into a single-chip solution. This relieves the designer from the constraint of thinking that memory mapping, ports, and address latch requirements should be developed from separate elements.

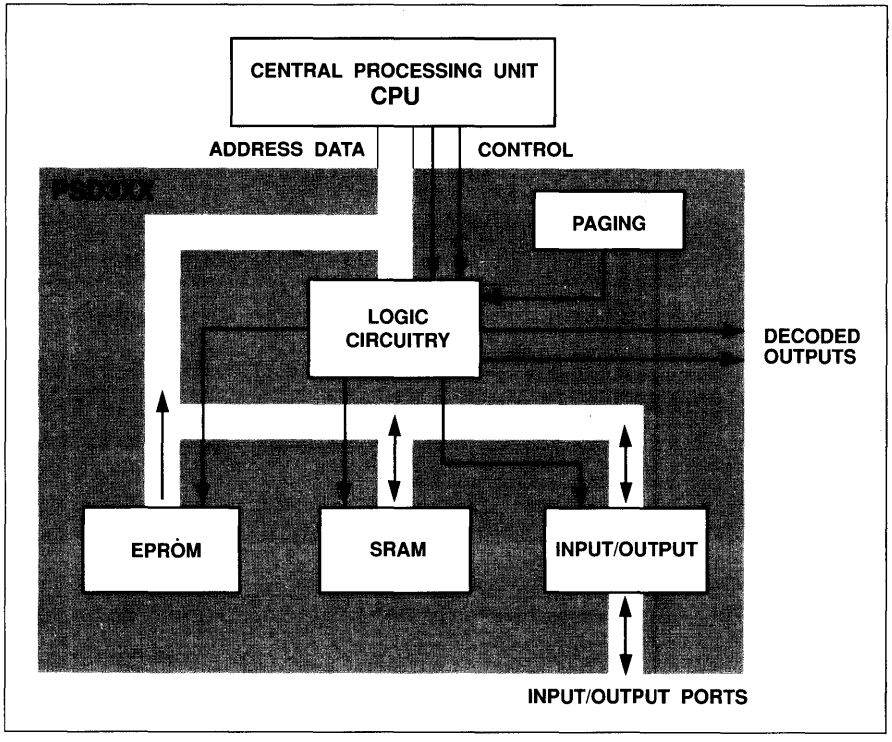


Figure 1. PSD3XX supports CPU as a Complete peripheral, memory, and logic subsystem

Introduction (Cont.)

This high integration of functionality into a single chip enables designers to reduce the overall chip count of the system. The result is increased system reliability, simpler PCB layout, and lower inventory and assembly costs. By integrating ports, latches, a Programmable Address Decoder (PAD), EPROM, and static RAM, the PSD3XX can bring the system solution down to only two chips: a microcontroller and a PSD3XX. The alternative solution would be discrete elements of RAM, EPROM, I/O mapped ports, and latches all mapped into the address scheme by a programmable logic device (PLD). This could escalate the chip count to 8–12 packages, depending on size and complexity.

For larger systems, multiple PSD3XX 's can be configured. Due to its versatility and flexibility, two or more PSDs can be cascaded either horizontally (increasing bus width) or vertically (increasing sub-system depth). This proportionally increases the complement of memory, I/O ports, and chip-selects without the need for additional external glue logic.

An additional feature of the PSD3XX is its ability to support a wide range of microcontrollers or microprocessors because it has been designed with a wide range of configurable options. The designer can program any one of a number of different options to create specific compatibility with a host processor. Furthermore, this can be done without the need for external glue logic.

WSI Software Support for the PSD Family

The PSD family can be easily configured from a low-cost software support package called MAPLE. Designed to run in an IBM/PC environment, MAPLE makes design and configuration of the PSD3XX a simple task. Memory mapping of EPROM and RAM blocks replaces PLD-like equations with user-friendly, high-level command entries.

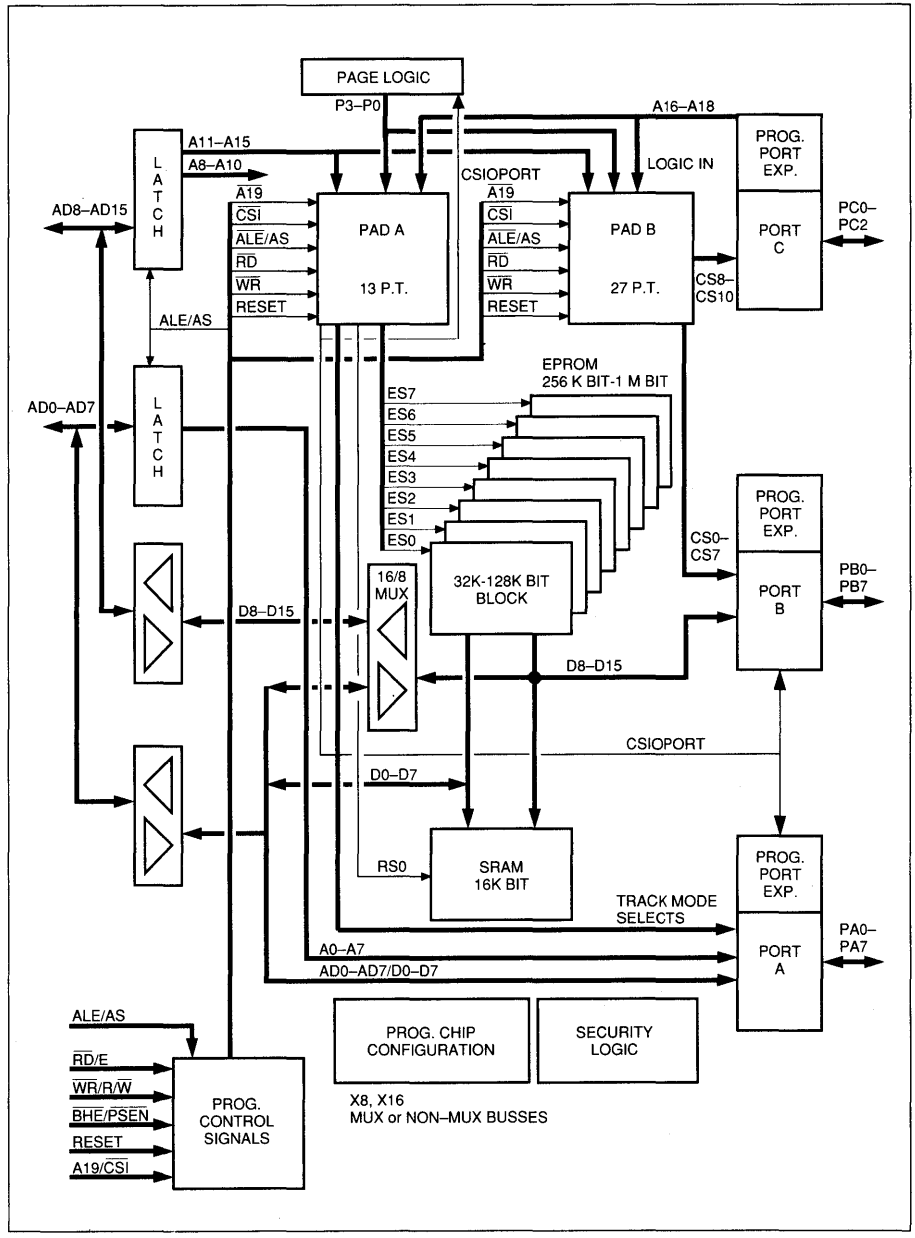
PSD3XX Architecture and Pin Nomenclature

The PSD3XX is available in a variety of 44-pin packages (see the PSD3XX Data Sheet). Figure 2 is a functional block diagram of the PSD3XX that shows the pin functions, internal architecture, and bus structure.

Inputs AD0–AD15 enter the PSD through latches. These can be programmed to latch the address/data inputs, removing the need for such devices as the 74HCT373 or 573. Alternatively, in the transparent mode they simply buffer address inputs. The Address Latch Enable (ALE) signal is available to register a valid address input on the AD0–AD15 lines; its active polarity is programmable. Another name for this input is Address Strobe (AS). It provides the same function and the same timing as the ALE, but this pin name is more appropriate to Motorola-type systems.' When either ALE or AS is valid, the latches are transparent; when inactive, the address/data inputs on AD0–AD15 remain latched.

The PSD3XX also contains a Programmable Address Decoder (PAD). Figure 2 shows that address inputs A11–A15 (and, possibly, inputs A16–A19) go directly to the PAD. Other inputs to the PAD include $\overline{RD}$(E), $\overline{WR}$ (R/$\overline{W}$), and ALE(AS). Programming of the PAD enables the designer to internally select the EPROM banks via internal chip-select lines ES0–ES7. An additional chip-select for the internal SRAM is available through RS0. Port C conveys either $\overline{CS8}$–$\overline{CS10}$ to external devices or receives A16–A18 inputs, directing them to the PAD. Also, A19 can be programmed to go directly into the PAD. Note that these lines are not necessarily dedicated to address inputs; they can be used as general purpose logic inputs. Thus, the PAD can be programmed to perform general combinational logic without adding any 'glue logic' to the overall system design. Address inputs A16–A19 can be used as general inputs to the PAD for implementing logic

Figure 2. PSD3XX Architecture.



PSD3XX Architecture and Pin Nomenclature (Cont.)

equations, and not for address decoding. If they are not used, A16–A19 are "don't care" conditions in memory map allocation. (See Figure 7 for a more detailed diagram of the PAD.)

The internal port options (Ports A and B) are both 8 bit-wide and can be programmed to act as traditional I/O ports. Port C is a 3-bit port designed to output logic functions from the PAD, receive address inputs A16–A18, or a combination of both. Ports A and B, however, are more complex because a number of different options can be selected with regard to system configuration. Figures 3, 4, 5, and 6 show the variety of configurations that are available to these ports.

Performance Characteristics

Two key timing parameters associated with the device are the EPROM/SRAM access times and the propagation delay through the PAD. The worst-case delay from valid address input to valid data output is 120 ns whether the address input is multiplexed or not. The cycle time of the system is virtually 120 ns with a small margin for address switching. This gives a system clock rate of about 8.3 MHz. Considering the power-down option, it takes 100 ns for active power input enabled through the $\overline{CSI}$ to valid data output. If the chip-select output option is chosen for either Port B or Port C, the propagation delay for address and control input through the PAD to valid chip-select output is 35 ns.

PSD3XX System Configuration for Port and I/O Options

In this section, the EPROM and SRAM are treated as separate entities and the four options available for configuring the PSD301 in a processor system are detailed. Figure 3 shows an 8-bit data configuration for systems that multiplex 8-bits of data (D0–D7) with the corresponding address inputs (A0–A7). Lines A8–A15 are dedicated to higher-order address inputs. Ports A and B are then available for data I/O and Port C is available for additional inputs, A16–A18 or chip-select outputs $\overline{CS8}$–$\overline{CS10}$. Port A also has the option of passing any one or all of the internally latched lower-order addresses (A0–A7) to the output. Another mode supported by Port A is called "track mode." In this mode, the PSD301 can be programmed to pass the I/Os AD0–AD7 through the device enabling a shared memory or peripheral resource to be accessed. Port B has an additional mode to the general port mode. The PSD301's on-chip PAD can be programmed to generate chip-select signals which can be routed to Port B's output for external chip selection as $\overline{CS0}$–$\overline{CS7}$. Port C can be programmed for inputs A16–A18 or as additional chip-select outputs $\overline{CS8}$–$\overline{CS10}$. Although labeled as address inputs, A16–A18 can be used for general Boolean inputs to the PAD array.

Figure 4 extends the option offered in Figure 3 to a 16-bit multiplexed bus. AD8–AD15 convey address and data I/O. The port options remain the same as for Figure 3; thus, these two configurations are suitable for multiplexed address/data systems of 8 or 16 bits.

Figures 5 and 6 show options for a non-multiplexed host processor or controller. Figure 5 is suited to byte-wide systems and Figure 6 to 16-bit word-wide configurations. In Figure 5, Port A is used for data D0–D7 but Port B is still available for general I/O operations or chip-select outputs. This configuration is suitable for processors such as the M68008.

The function of Port C is the same in all of the four modes of operation. For 16-bit data transfers, an additional 8 bits of data is required. Figure 6 shows Port B as the data bus for the higher-order data byte D8–D15. With D0–D7, this configuration is suitable for 16-bit microprocessors such as the M68000. Port C is available for address inputs or chip-select outputs.

Figure 3. 8-bit multiplexed address/data mode

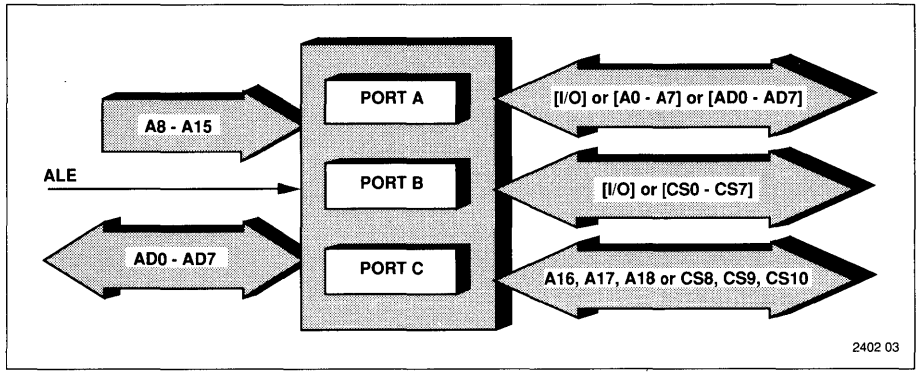


Figure 4. 16-bit multiplexed address/data mode.

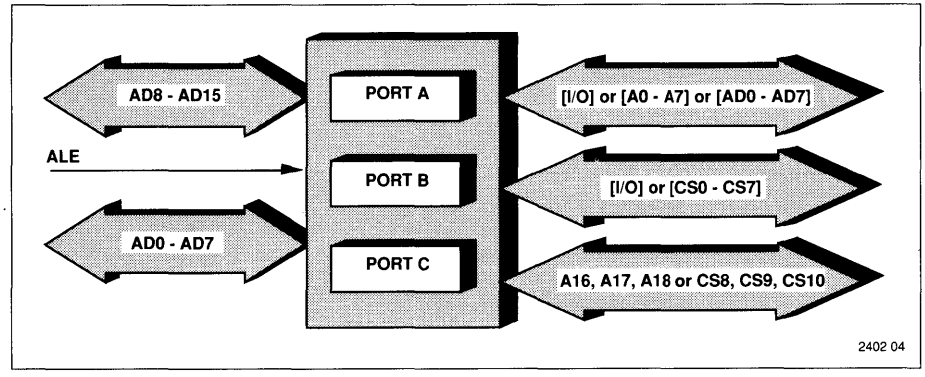


Figure 5. Non-multiplexed Mode 8-bit Data Bus

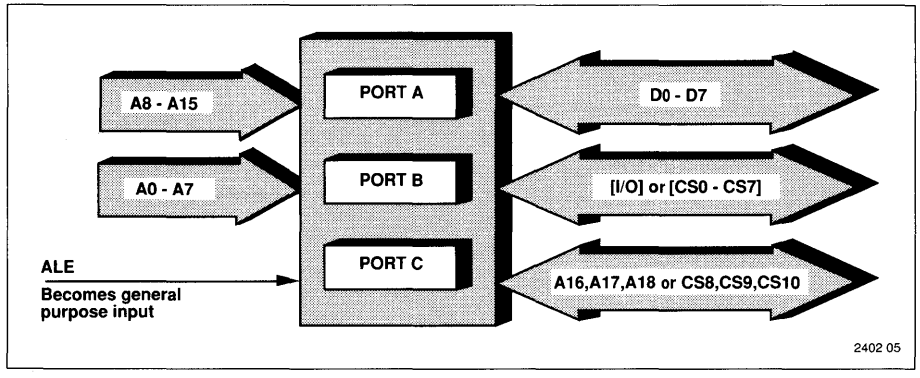
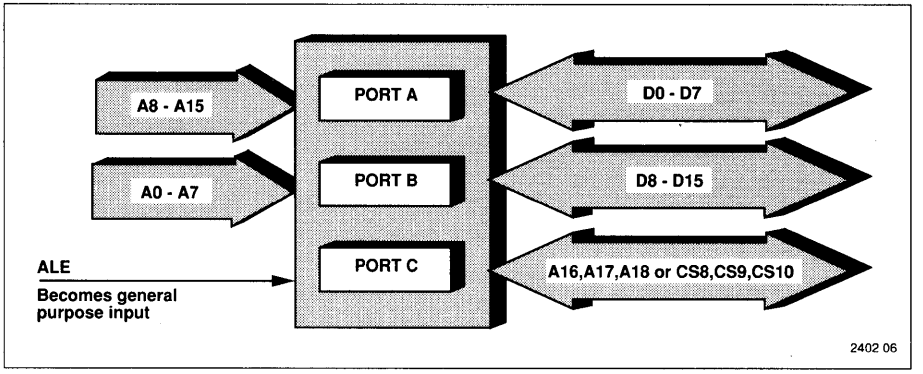


Figure 6. Non-multiplexed Mode 16-bit Data Bus



Address Inputs

The processor interface has 16 address inputs: AD0–AD15. The device can be programmed to accept either address inputs or multiplexed address/data inputs. The address lines can be latched into the one or two octal latches for multiplexed byte or word-wide buses respectively. The device is initially programmed with a word configuration setting the PSD3XX to a specific mode; for example, one configuration bit selects whether the address input is multiplexed with data or is a non-multiplexed dedicated address. In the non-multiplexed scheme, the input latches are held as transparent. When the address inputs are valid on the chip as A0–A15, they can be subdivided into two buses: as lower-order addresses (A1–A11), and as higher-order addresses (A12–A15). A1–A11 go directly to the EPROM and inputs A1–A10 go to the SRAM (see Figure 2). The EPROM blocks are selected through the PAD via outputs ES0–ES7 as shown in Figure 2; and the SRAM is selected by the RS0 output.

The address input lines A11–A15, along with possible additional address inputs A16–A19, go into the PAD array. These address inputs are available for mapping the blocks of memory into the map scheme of the system. One option is to program the additional address inputs as valid higher-order address inputs for memory addressing ranges above 64K bytes or 32K words. If A16–A18 are not required, these PAD inputs can be ignored. Only microprocessors and microcontrollers with a large addressing range use these higher-order address lines. A second option is to disregard these address inputs to the chip in favor of additional chip-select outputs. A third option is available if the designer does not need additional chip-select outputs or high-order address inputs. The inputs A16–A18 can be used as general-purpose logic inputs. Examples of this are illustrated in some of the following applications.

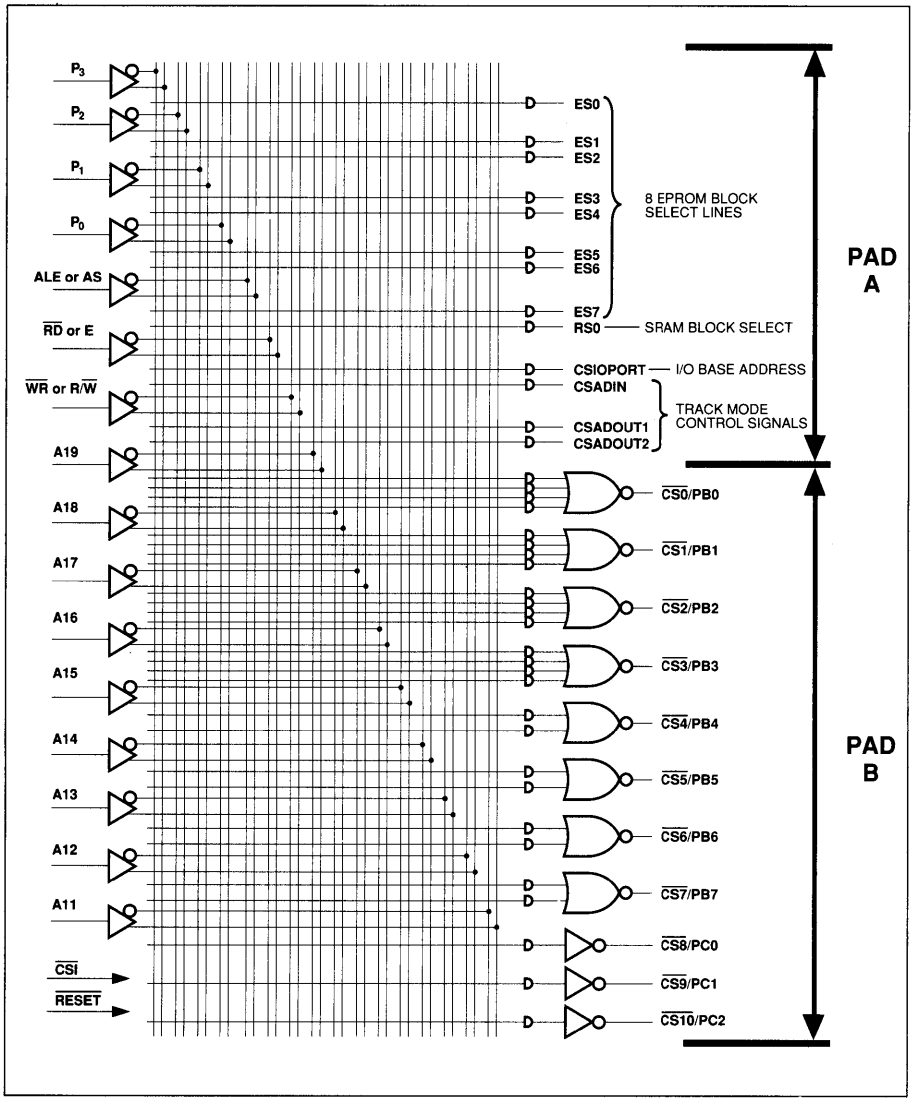
An interface with the Z80B microprocessor uses inputs A16, A17, and A18 for signals $\overline{M1}$, $\overline{MREQ}$, and $\overline{IORQ}$, respectively. In the M68008 application, two of these pins are programmed as $\overline{DTACK}$ and $\overline{BERR}$ from the PSD301 to the M68008. A wired-OR function can be implemented on the $\overline{DTACK}$ or $\overline{BERR}$ input if the user takes advantage of Port B's open-drain feature. If two PSD3XX devices are used together, the $\overline{DTACK}$ and $\overline{BERR}$ lines can be wired together and the external pull-up resistors can be used to tie these lines HIGH. It is also possible to use the internal PAD of one PSD3XX to gate these lines together and produce composite $\overline{DTACK}$ and $\overline{BERR}$ inputs to the M68008.

Internally, the memory blocks are arranged word-wide with a byte-wide isolation buffer separating the lower and upper bytes. This buffer is controlled from the configuration section of the PSD3XX. When the PSD3XX is configured to operate in word-wide mode, this buffer isolates the two buses into D0–D7 and D8–D15. In word-wide mode, the control of the data flow through this buffer is determined by BHE, A0, and the device's current configuration mode. Accessing byte-wide data can be thought of as accessing bytes on even and odd word boundaries or as two separate

Address Inputs (Cont.)

banks of byte-wide data. The total complement of EPROM is shown as eight banks. The chip-select outputs ES0-ES7 come from the PAD. These are programmable address and control decode signals from the PAD inputs. Figure 7 provides a detailed schematic diagram of the PAD in terms of a traditional PLD.

Figure 7. PSD3XX Programmable Array Decoder



PSD3XX Programmable Array Decoder (PAD)

The PAD is an EPROM-based reprogrammable logic fuse array with sum-of-product outputs. For Intel-type configurations, inputs to the PAD are A11–A19, ALE, $\overline{RD}$, and $\overline{WR}$. For Motorola type configurations, they are R/$\overline{W}$, AS, and E. The $\overline{CSI}$ and RESET inputs are used to deselect the PAD for power-down configurations and initialization, respectively. Internal to the PSD301 are the ES0–ES7 EPROM select lines. There is one product term dedicated to each EPROM block, and a single product term (RSO) for the SRAM selection. Address and control for each EPROM bank can programmed to a resolution of a 4K word boundary and positioned anywhere in the mapping scheme of the designer's system. Similarly, the SRAM can be positioned on 2K word boundaries.

Other internal product term outputs from the PAD are the CSIOPORT, CSADIN, CSADOUT1, and CSADOUT2 lines. A single product term generates the CSIOPORT signal; this provides a base address for Ports A and B. The registers relevant to these ports are addressed as a base offset (see Table 1). The CSADIN signal is used to control the input buffer in the track mode. It can be enabled to read data in a programmed address space from Port A through the PSD3XX. CSADOUT1–2 are used to control the multiplexed address and write data through the PSD3XX to the Port A pads. The address range is programmed into the PAD qualifying the address space, but CSADOUT1 is qualified by the ALE signal outside of the PAD. This automatically lets the design distinguish between address and write data. To qualify valid write data, the PSD3XX automatically includes the CSADOUT2 product term with the $\overline{WR}$ or R/$\overline{W}$ signal.

Table 1. Port Base Address Offset

Register Name	Offset From The CSIOPORT Base Address
Pin Register of Port A	+2 (Accessible only during Read)
Pin Register of Port B	+3 (Accessible only during Read)
Direction Register Port A	+4
Direction Register Port B	+5
Data Register Port A	+6
Data Register Port B	+7 (Byte Wide)
Pin Register of Ports A and B	+2 (Accessible only during Read)
Direction Register of Ports A and B	+4
Data Register of Ports A and B	+6 (Word Wide)

The PAD structure enables additional chip-selects to be routed to the Port B output pins. The four chip-select outputs ($\overline{CS0}$–$\overline{CS3}$) are supported by four product terms per output. $\overline{CS4}$–$\overline{CS7}$ have two product terms per output. The ability to use more than one product term from a chip-select enables the mapping of additional devices to be distributed through the address space, rather than selecting memory as a block. Sacrificing Port B terminals for chip-selects could occur in systems requiring a larger EPROM, RAM, or I/O space. Additional PSD3XX devices can be designed into a system by using the chip-select outputs from Port C or B of one master PSD3XX. This is required for addressing a space greater than 1M. Finally, the outputs of the sum-of-product terms are inverted to be consistent with active LOW chip-select inputs for additional external RAM, EPROM, peripherals, or busses. Port C has the capability of providing three additional external chip-selects, each supporting one product term per output.

Microcontroller/ Microprocessor Control Inputs

The control inputs are also programmable: $\overline{WR}$ or R/$\overline{W}$ and $\overline{RD}$ or E are used for read/write control of the internal EPROM, RAM, and I/O capability. Other control inputs are a programmable option for Bus High Enable or Program Store Enable ($\overline{BHE}$/$\overline{PSEN}$) and Address Latch Enable or Address Strobe (ALE/AS). These pins are selected to suit the bus protocol of the host processor or, where not applicable, they can be ignored. The $\overline{CSI}$/A19 input is available either for a power-down chip-select enable or as a higher-order address input without the power-down feature. The final control input is the RESET input; this also is a programmable option. Its active polarity can be chosen to be compatible with the host system. The function of the RESET input is to clear and initialize the PSD301 at start-up. All I/Os are set up as inputs and all outputs are either in a non-active or three-state condition.

Consequently, the PSD3XX is prevented from actively driving outputs during start-up. This feature was incorporated to prevent potential bus conflicts. In Figure 2, the $\overline{CSI}$ and RESET inputs are shown also as PAD inputs. $\overline{CSI}$ is a hardwire option into the PAD that powers down the internal circuitry and is used in power-sensitive applications. Neither signal is available as a programmable option.

Input and Output Ports

The port section comprises Port A (8 bits), Port B (8 bits), and Port C (3 bits). These support the many different I/O operations. For port expansion, Ports A and B can be configured as general I/O ports, each to convey eight bits of digital data to and from an external device. Figure 8 shows a single cell of Port A; Figure 9 shows a single cell of Port B.

Writing data to a port is similar to writing data to a RAM location. If a port is programmed as an output, data is loaded into the output register as if it were a RAM location. Although the ports are not bit addressable, individual bits can be selected as either input or output. Thus, PA0–5 can be set as data outputs while PA6 and PA7 can be configured as inputs. Any mix of I/Os is possible giving the ports additional flexibility.

The direction of data flow through the port is determined by the data direction register. This register is dynamically programmable so that the I/O direction through Ports A and B can be altered during the microcontroller program execution. The data direction register initializes with logic zeros after an active RESET and causes each port bit to be set as an input. This state of initialization guarantees that the ports are prevented from driving the output lines at start-up. If the user requires all the Port A or Port B bits to be inputs, the data direction register can be left in this default state. To enable it as an output, logic ones can be written into the data direction location.

Due to the internal design, it is possible to program Port A or Port B bit lines as inputs and still write data to the port locations. This is because both ports have on-chip latches and can hold data. These registers are hidden or buried; i.e., they exist in the port and their condition can be read back at any time. However, these outputs do not drive the output pins because the port has been enabled as an input.

To access the port as a memory mapped location, the initial selection is made through the PAD's CSIOPORT. This provides a base address from which the locations shown in Table 1 give access to the various ports or their options. The configuration support software automatically ensures that there is no conflict between an SRAM location and I/O port in the case of memory mapped peripherals. It is also possible for the PSD3XX to distinguish between I/O and memory mapped locations. The user can input memory and

Input and Output Ports (Cont.)

I/O control signals to the PAD through the A16–A18 inputs and program an active CSIOPORT output by decoding these signals. This can be achieved with Intel- and Zilog-type processors which have separate memory and I/O controls. Signal input through pins A16–A18 is made possible through Port C. This 3-bit port is responsible for either PAD chip-select outputs or address/logic inputs. CSIOPORT points to a base address at which Ports A and B reside. Table 1 provides the offset from the base address and the associated port function. Figure 2 shows that Port A is driven by a multiplexed address/data bus of AD0–AD7 and the selection of address/data is made from the configuration memory and internal control functions.

The other options available to the user are selecting 1) the shared resource or track mode where AD0–AD7 is routed directly through to the Port A output, or 2) the latched address A0–A7. In track mode, AD0–AD7 inputs to the PSD3XX are used to access local or private memory and peripherals and the outputs AD0–AD7 through Port A are used to access a public resource.

Figure 8. PSD3XX Port A Structure

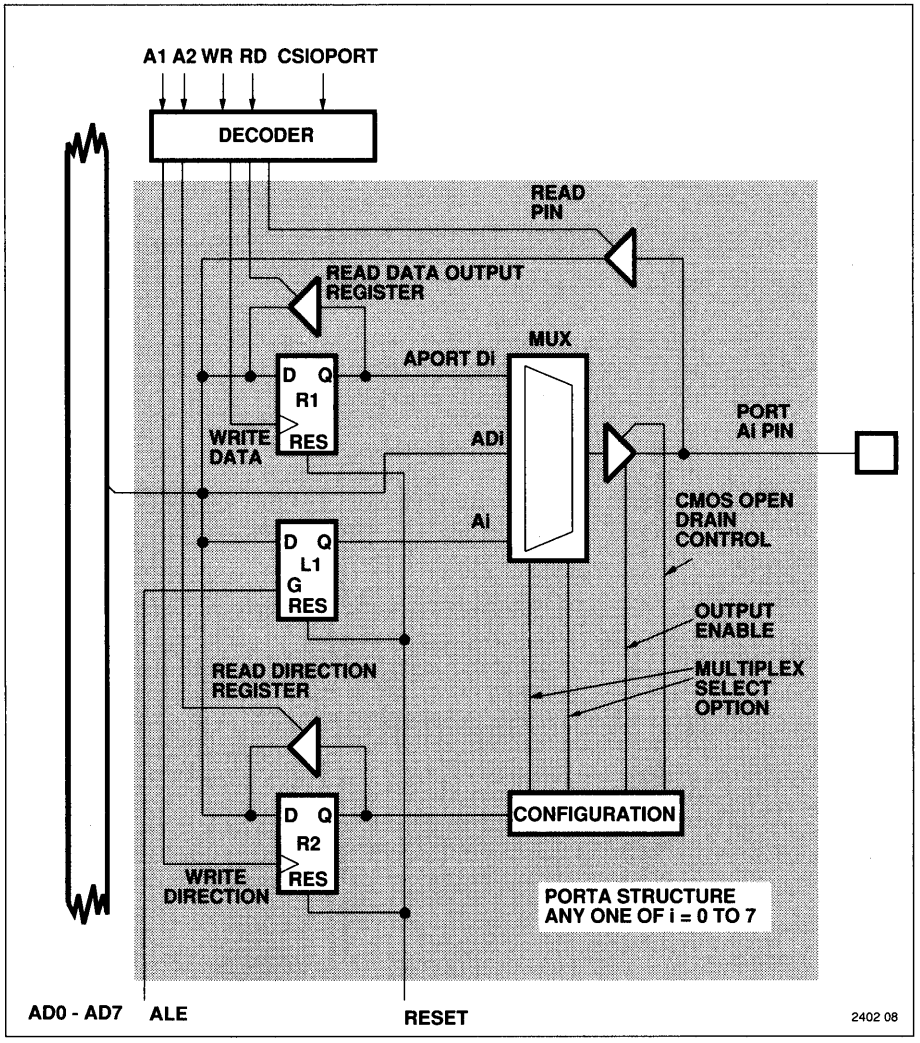
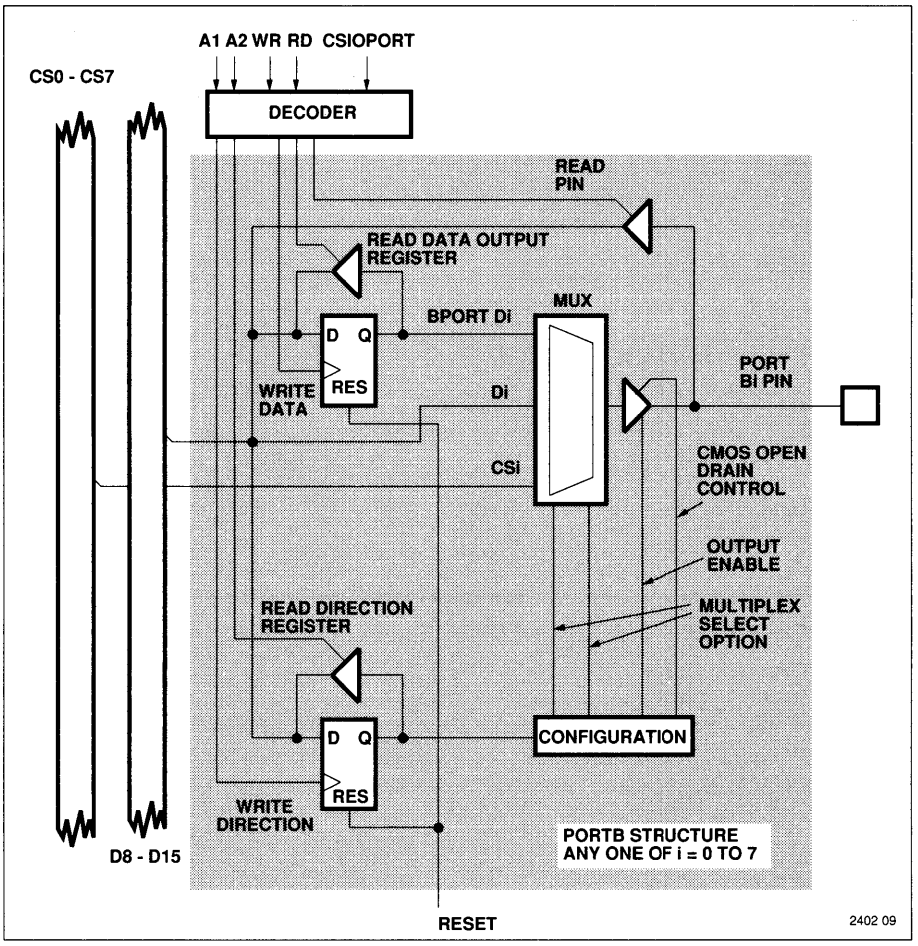


Figure 9. PSD3XX Port B Structure



PSD3XX General System Configuration

The PSD3XX family devices consists of two byte-wide configurable I/O ports (Ports A and B), 256K to 1M bits of EPROM, 16K bits of RAM, and the PAD. Additional I/O capability to and from the PAD is through a 3-bit I/O (Port C). There are also on-chip latches to support processors and controllers that multiplex address and data on the same bus. The EPROM memory section of the device is programmable just like a standard EPROM device. However, unlike the single-chip EPROM, the PSD3XX must also be configured to function into one of its many possible modes of operation. This is done by programming a non-volatile EPROM memory location with 45 configuration bits. These bits select the mode of operation and are programmed into the EPROM along with the hexadecimal microprocessor/microcontroller assembly language object code. When using MAPLE software, the assignment of logic conditions to the configuration bits locations is transparent to the user; the resultant word is merged with the EPROM code and the data map for the PAD.

PSD3XX General System Configuration (Cont.)

Table 2 shows the the configuration locations and their functional assignment. For example, one of the configuration bits enables the device architecture to be compatible for either byte- or word-wide data buses. This is the configuration data or CDATA bit. The 256 Kbits of EPROM can be configured as a 32K byte-wide bus for applications with an 8031 microcontroller or as a 16K word-wide bus for applications with an M68000 microprocessor. These configuration bits are discussed in detail as each feature is covered in this application note.

In addition to bus width, the polarity and mode of the bus control signals are programmable. There are two types of read/write control: one is consistent with either a Motorola and Texas Instruments control bus standard; the other is consistent with the Intel/National Semiconductor/Zilog control bus standard. The configure read and write bit (CRRWR), distinguishes between one of two conventions: either an Intel (8031) or Motorola (M68HC11) convention can be selected by programming this single bit in the configuration memory. The Intel device requires the PSD3XX to be programmed with an active LOW $\overline{RD}$ and $\overline{WR}$ controls (CRRWR = 0). For applications with the Motorola microprocessor, select the R/$\overline{W}$ and E option (CRRWR = 1). In addition to a choice of two READ/WRITE controls, the user can select either a multiplexed Address/Data Bus or separate address and data lines.

Figure 3 shows the configuration that is best suited for the 8031 microcontroller; Figure 4 shows the configuration for an 80196 microcontroller with a 16-bit multiplexed addressed/data bus. For the non-multiplexed modes:

Figure 5 applies to M6809 microprocessors, while Figure 6 shows the mode applicable to the M68000. Selection of multiplexed or non-multiplexed buses is a programmable option that can be invoked through the configure address/data multiplex (CADDRAT) bit. With the 8031 controller, address outputs A0–A7 are multiplexed with the data D0–D7 input/output lines to create a composite AD0–AD7 bus.

The PSD3XX's input latches can be programmed to catch a valid address when the microcontroller's ALE signal transitions from active HIGH to inactive LOW. The polarity of the ALE signal is also a programmable feature in the CALE field of the configuration table. Address latching can be programmed to occur on either an active HIGH or an active LOW ALE signal. With Intel devices, the address is valid when ALE is HIGH. Once latched, data or code can be read from, or written to, the PSD3XX. The CALE active HIGH or LOW ALE configuration bit only applies to addresses A0–A15. A separate configuration bit, (CADDHLT), exists for the control of the higher-order address inputs (A16–A19). If necessary, these addresses can also be latched by the host system.

The highest address input is A19 but this signal can be omitted in favor of a power-down chip-select input ($\overline{CSI}$). A19/$\overline{CSI}$ is selected by the CA19/$\overline{CSI}$ configuration bit. When the $\overline{CSI}$ input is selected and the pin is driven HIGH, the device can be powered-down consuming only standby power. When configured with other CMOS devices, the standby power is in the 80–250 µA range. Many CMOS microcontrollers do not need a large memory address space; thus, address inputs A16–A19 would be unnecessary. The CA19/$\overline{CSI}$ input can be programmed with a logic LOW to enable a power-down option for power sensitive applications.

The address/data multiplexed scheme also supports the 16-bit processors. In this case, AD0–AD15 convey a 16-bit address qualified by ALE (or AS for the Motorola convention) and 16-bits of data I/O. This feature is shown in Figure 4. A microcontroller that would use this scheme is the 80C196. The M68HC11, like the 8031, uses the 8-bit multiplexed scheme but with the Motorola convention for bus control.

Another control pin used for 80C31 applications used to distinguish between program and data memory is the $\overline{PSEN}$ output. The $\overline{COMB}$/SEP configuration bit should be programmed HIGH if data and memory are separate and LOW to configure a combined memory space in the PSD3XX. This is a

PSD3XX General System Configuration (Cont.)

useful feature for systems that require program memory and data memory to be in separate blocks.

For systems that use separate data and address buses, the address latches can be set into a transparent mode by clearing the CADDRDAT bit location. Thus, the PSD3XX is suitable for multiplexed or non-multiplexed bus structures employing 8- or 16-bit bus widths.

The RESET input to the PSD3XX enables the device to be initialized at start-up. RESET can be either active HIGH or active LOW depending on the processor type. The CRESET configuration bit selects the polarity of the RESET input: LOW for active LOW and HIGH for active HIGH RESET. Normally, memory systems do not require a RESET input; however, the PSD3XX contains data direction registers for the ports that must be initialized at start-up. Note that all port I/O buffers are automatically programmed as inputs during start-up.

Table 2. Non-volatile Configuration Bits

Configuration Bits	Number of Bits	Function
CDATA	1	CDATA . 0 = eight bits, 1 = sixteen bits
CADDRAT	1	ADDRESS/DATA Multiplexed. 0 = Non-multiplexed, 1 = Multiplexed
CRRWR	1	CRRWR. 0 = $\overline{RD}$ and $\overline{WR}$, 1 = R/$\overline{W}$ and E
CA19/$\overline{CSI}$	1	A19 or $\overline{CSI}$. 0 = Enable power-down, 1 = Enable A19
CALE	1	ALE Polarity. 0 = Active HIGH,1 = Active LOW
CRESET	1	CRESET. 0 = Active LOW RESET, 1 = Active HIGH RESET
$\overline{COMB}$/SEP	1	Combined or Separate Address Space for SRAM and EPROM. 0 = Combined, 1 = Separate
CPAF2	1	Port A Track Mode or Port Mode. 0 = Port or Address, 1 = AD0–AD7 Track Mode
CPAF1	8	Port A I/O or A0–A7. 0 = Port A pin is I/O, 1 = Port A pin is Address
CPBF	8	Port B I/O or CS. 0 = Port B pins are CSi (i = 0–7), 1 = Port B pins are I/O
CPCF	3	Port C A16–A18 or $\overline{CS8}$–$\overline{CS10}$. 0 = Port C pins are Address, 1 = Port C pins are Chip-select
CPACOD	8	Port A CMOS or Open Drain. 0 = CMOS drivers, 1 = Open Drain
CPBCOD	8	Port B CMOS or Open Drain. 0 = CMOS Drivers, 1 = Open Drain
CADDHLT	1	A16–A18 Transparent or Latched. 1 = Address latched, 0 = Address transparent
CSECURITY	1	CSECURITY On/Off. 0 = Off, 1 = On

PSD3XX Configuration for Port Reconstruction

A key feature of the PSD3XX is the concept of port reconstruction. When using microcontrollers with additional off-chip memory, port I/O address lines are sacrificed for address, data, and memory control lines. With a multiplexed address/data scheme, two 8-bit controller ports could be lost to address and

PSD3XX Configuration for Port Reconstruction (Cont.)

data. Furthermore, in some control applications, many port I/O bits are required to send actuating signals to solenoids, instrument displays, etc., and receive data through sensors and switch panels. In many control environments, a large amount of I/O capability is required; also, additional external memory is needed for microcontroller instructions to perform data manipulation. Without the PSD3XX , the supplement of extra ports as discrete latches addressed through logic decoders can add a number of chips to the final design. By using the PSD3XX, additional EPROM, RAM, and ports are all provided on one chip. Port reconstruction lets the designer reclaim the two ports sacrificed for the microcontroller's address and data.

Port configuration is achieved through the configuration register bits. CPAF1 configuration of Port A contains eight bits; programming a logic LOW assigns the selected bit with I/O capability as if it were a conventional port. If programmed HIGH, the internally latched address inputs A0–A7 are routed to Port A lines PA0–PA7. This feature enables other on-card peripherals to use A0–A7 as latched addresses. Without this feature, external peripherals to the PSD3XX would require an external octal latch to catch the multiplexed address when it becomes valid at the microcontroller's output. Configuration of Port A as general I/O or address/data is on a bit-wise basis; thus, the choice of port or address/data assignment can be mixed. For example, configuration code 11100000B programmed into location CPAF1 passes addresses A0–A2 to outputs PA0–PA2 and enables PA3–PA7 as conventional port lines.

Configuration bit CPAF2 is a 1-bit location. When programmed LOW, it selects the port/address option, as described above. If CPAF2 is programmed HIGH, port bits PA0–PA7 are set into track mode. Activity on the PA0–PA7 outputs follow logic transitions on inputs AD0–AD7. The multiplexed address/ data input is tracked through PA0–PA7. Track mode enables the host microcontroller to access a shared memory and peripheral resource through the PSD3XX while maintaining the ability to access its own (private) memory/peripheral resource directly from the microcontroller's address/data outputs. In this mode, the address/data AD0–AD7 passes through the PSD3XX logically unaltered. In summary, PA0–PA7 can be programmed as port I/O or latched address outputs A0–A7 (each bit being programmed on an individual basis), or as AD0–AD7 outputs (track mode).

Port B bits PB0–PB7 can be programmed either as regular port I/Os, or as chip-select outputs $\overline{CS0}$–$\overline{CS7}$ encoded from the PAD outputs. Figure 7 shows the PAD structure as a conventional PLD. Eight bits are programmed into CPBF. Logic LOW indicates that a port pin is a chip-select output derived from the PAD. Programming a logic HIGH sets the appropriate pin as an I/O function. The bit pattern 11111000B programmed into the CPBF location sets up PB0–PB4 as I/O ports and PB5–PB7 as chip-selects. The typical applications, where Port B is programmed as bi-directional, would be with microcontroller chips that need additional port bits. This would be in applications where port reconstruction is needed to drive many indicators, solenoids, read switches, sensors, etc. In large microprocessor-based systems, the chip-select option would probably be chosen; in this case, the PAD outputs select other PSD devices, DRAM memory chips, and peripherals such as timers, UARTs, etc.

The three bits comprising Port C can be programmed by the CPCF configuration bits. This group of three bits define whether Port C is used for inputs (typically A16–A18) or whether the pins are used as chip-select outputs from the PAD. Although labeled as A16–A18, the nomenclature of these pins does not constrain the designer to using these inputs as dedicated higher-order address inputs. In fact, they can be general-purpose inputs to the PAD for processors that do not have an address capability above 64K locations. When the PSD3XX is used with the Z80B microprocessor, the Port C inputs have been programmed as $\overline{MREQ}$, $\overline{IORQ}$, and $\overline{M1}$. In the case of an interface to the M6809B, two inputs of Port C have been converted to chip-select outputs for other memory devices and one output has been used to feedback a READY input to the M6809B. Port C can be used as a general I/O from the PAD in the form of address, control, and chip-select bits. A logic LOW programs a port bit as an input; a HIGH programs it as an output.

Chapter 2 Applications

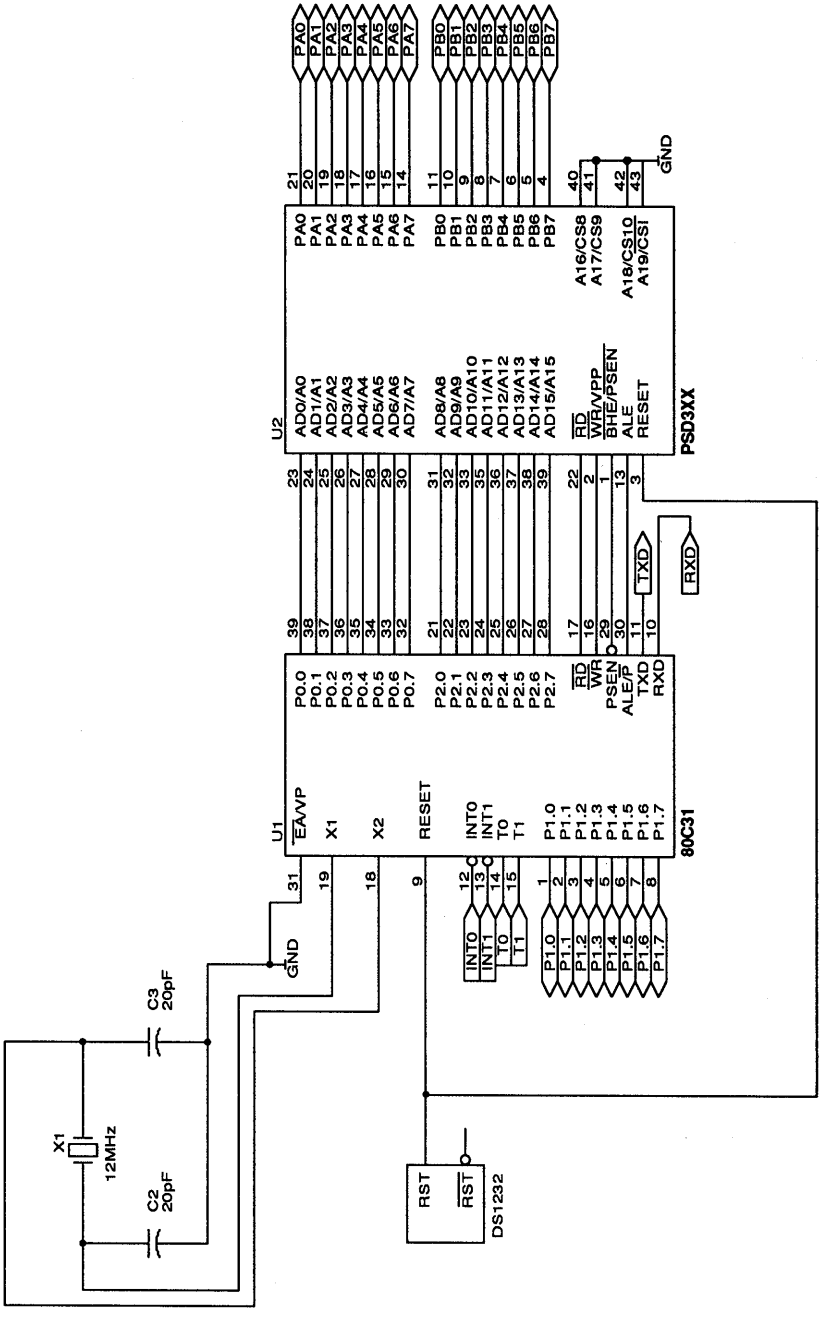
8-Bit Microcontroller to PSD3XX Interface

Figure 10 illustrates the minimum configuration of one controller and one PSD3XX. The application illustrates port reconstruction through the device's Port A and Port B I/O, reconstituting port 2 and port 0 of the microcontroller. Table 3 gives the configuration information that would be programmed in the configuration section of the PSD. Table 3 shows that both port I/Os have been programmed with CMOS load and drive characteristics. A feature of the 8051/8031 family is the $\overline{PSEN}$ signal, which determines whether the memory selection is active for executable code or data. This family of controllers has separate memory locations for code and data. To maintain full compatibility, the PSD3XX is also capable of being programmed to respond to the $\overline{PSEN}$ signal. When A16–A18 are programmed as inputs but not driven, they should be tied active HIGH or LOW. Unused inputs to the PSD3XX must not be permitted to float. Tying can be avoided on unused A16–A18 lines if these are programmed as 'dummy' $\overline{CS8}$–$\overline{CS10}$ outputs. A19/$\overline{CSI}$ cannot be programmed as an output; thus, it must be tied if not used.

Table 3. Small Controller System with One 80C31 and One PSD3XX

Configuration	Bits	Function
CDATA	0	8-bit data bus
CADDRDAT	1	Multiplexed address/data
CRRWR	0	Set $\overline{RD}$ and $\overline{WR}$ mode
CA19/$\overline{CSI}$	0	Set $\overline{CSI}$ input power-down mode
CALE	0	Active HIGH ALE
CRESET	1	Active HIGH RESET
$\overline{COMB}$/SEP	1	Code and data memory separate
CPAF2	0	Input/Output Port A
CPAF1	00H	Input/Output Port A (0–7)
CPBF	FFH	Input/Output Port B
CPCF	000B	Port C programmed for inputs
CPACOD	00H	Configure CMOS outputs Port A
CPBCOD	00H	Configure CMOS outputs Port B
CADDHLT	0	Transparent inputs A16–A19
CSECURITY	0	No security

Figure 10. 80C31/PSD3XX Applications



Two PSD3XX Byte-Wide Interfaces to the Intel 80C31

Figure 11 illustrates an extension to the previous design in that two PSD3XX devices have been used, doubling the memory and port resources of the system solution. In this application, the power-down capability has been used so that one PSD3XX can be active while the other device is in power-down mode. The mean power consumption is reduced, so this configuration can be considered for power-sensitive applications.

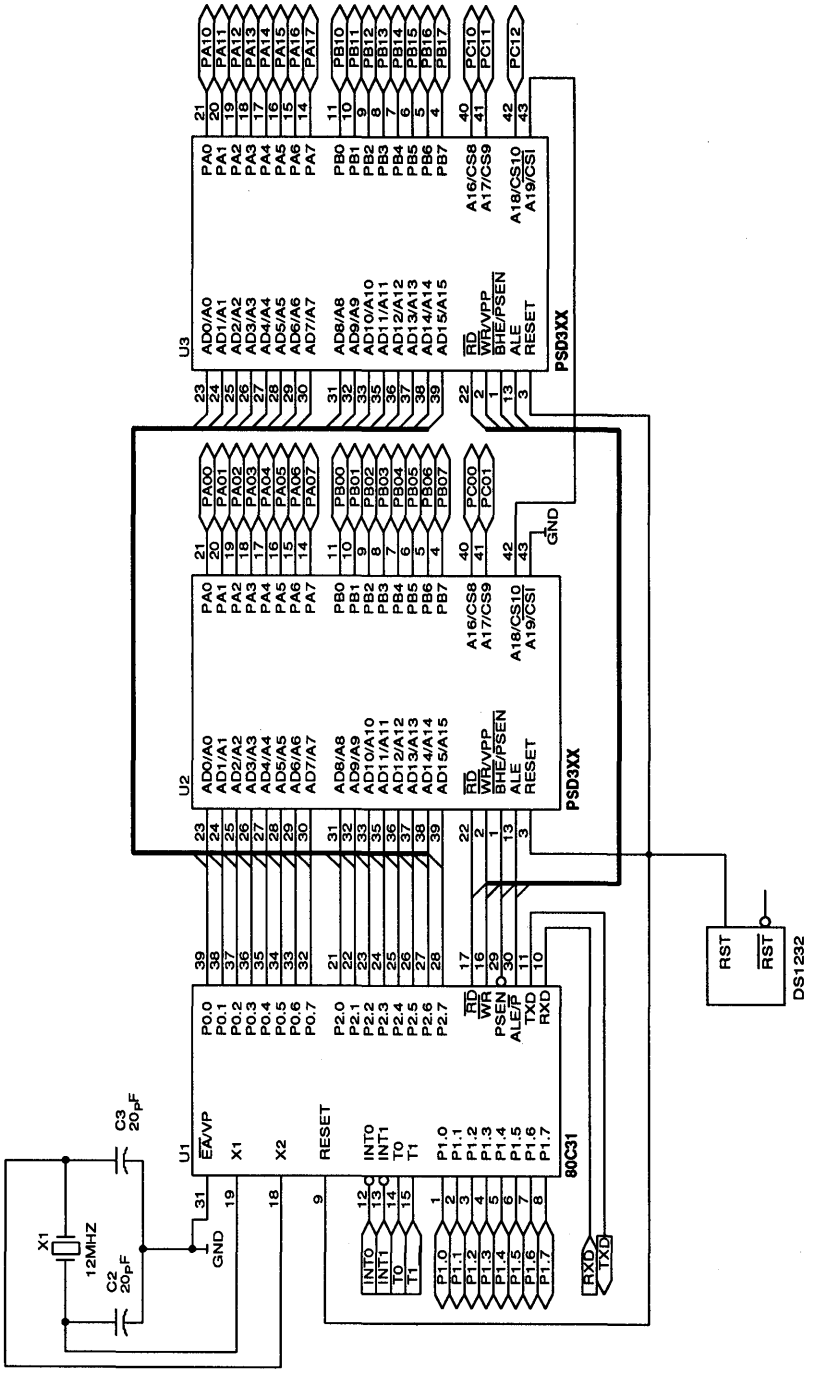
The configuration Table 4 indicates that Port C has been configured as outputs. Provided one PSD3XX is powered up for the whole address range, its PAD can decode an address range to select and deselect the second PSD3XX device through the $\overline{CS10}$ output. In Figure 11, the PAD output A18/$\overline{CS10}$ on PSD3XX U2 can be used to power-down the second PSD3XX through the A19/$\overline{CSI}$ input.

Table 4. 80C31 Interface to Two PSD3XX Devices with Power Economy Feature

Configuration	Bits	Function
CDATA	0	8-bit data bus
CADDRDAT	1	Multiplexed address/data
CRRWR	0	Set $\overline{RD}$ and $\overline{WR}$ mode
CA19/$\overline{CSI}$	0	Set $\overline{CSI}$ input power-down mode
CALE	0	Active HIGH ALE
CRESET	1	Active HIGH RESET
$\overline{COMB}$/SEP	1	Code and data memory separate
CPAF2	0	Input/Output Port A
CPAF1	00H	Input/Output Port A (0–7)
CPBF	FFH	Input/Output Port B
CPCF	111B	Outputs $\overline{CS8}$–$\overline{CS10}$
CPACOD	00H	Configure CMOS outputs Port A
CPBCOD	00H	Configure CMOS outputs Port B
CADDHLT	X	"Don't care" for latched A16–A19
CSECURITY	0	No security

It is not recommended that the two PSD3XX devices select each other because the PAD section of a PSD device is powered down with the rest of the device. At least one PAD decoder must be kept active to select and deselect others. Port C outputs $\overline{CS16}$–$\overline{CS18}$ can power-down as many as three other PSD3XX devices.

Figure 11. 80C31/2/PSD3XX Applications



PSD3XX M68HC11 Byte-Wide Interface

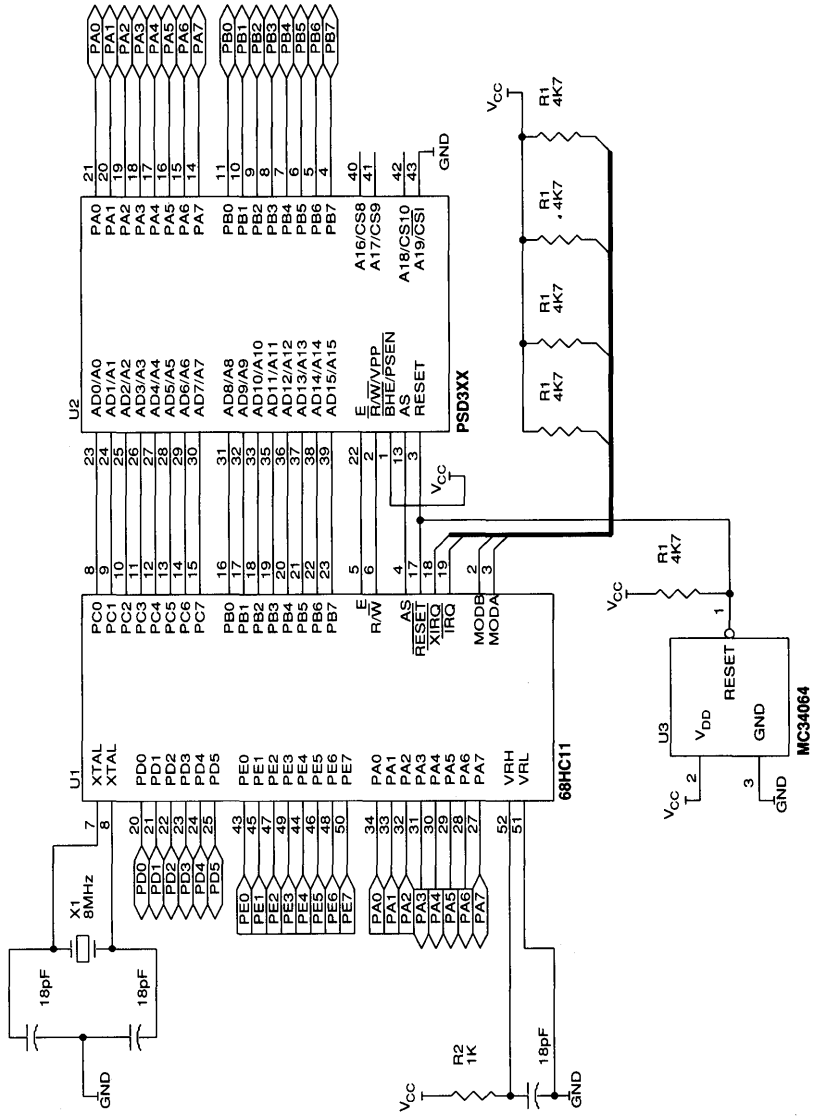
Figure 12 illustrates the configuration of an M68HC11 microcontroller which also uses the 8-bits wide multiplexed address/data bus. The application is similar to that given in Figures 6 and 7 except that the R/$\overline{W}$ and E control lines have been invoked to establish compatibility with the Motorola device. The address strobe output from the M68HC11 is HIGH so the AS(ALE) input is set HIGH. The SRAM and EPROM section are programmed as combined and both Ports A and B are enabled as I/Os with CMOS drives. Port C is programmed with chip-select outputs $\overline{CS8}$–$\overline{CS10}$. Other PSD3XX devices can be mapped into the addressing scheme or the lines can be programmed to transition as strobes in defined mapping areas. The latch enable bit for the higher-order address lines A16–A19 is not used establishing a don't care condition. The CADDHLT condition must be selected if any one of A16–A19 lines is selected as input to the PSD.

In this design, the security bit is programmed. This bit prevents the reading of the PAD configuration by an unauthorized user. Furthermore, if the security bit has been programmed, standard programming machines can not read the internal code of a PSD3XX . However, data can always be read from the EPROM, RAM, and ports. This provides normal use of the device. If the address map in the PAD cannot be interpreted, the actual location of data within the address and I/O space is difficult to determine. Besides programming the CSECURITY bit, added security can be applied by scrambling the sequence of address and data inputs. A short PASCAL or 'C' program can be written to reorganize the original Intel MCS code to be aligned with the scrambled pins. Table 5 indicates the configuration for the M68HC11/ PSD3XX interface.

Table 5. M68HC11 to PSD3XX Interface

Configuration	Bits	Function
CDATA	0	8-bit data bus
CADDRDAT	1	Multiplexed address/data
CRRWR	1	Set R/$\overline{W}$ and E mode
CA19/$\overline{CSI}$	0	Enable $\overline{CSI}$ input
CALE	0	Active HIGH AS (ALE)
CRESET	0	Active LOW RESET
$\overline{COMB}$/SEP	0	Combined memory mode
CPAF2	0	Input/Output Port A
CPAF1	00H	Input/Output Port A
CPBF	FFH	Input/Output Port B
CPCF	111B	Output $\overline{CS8}$–$\overline{CS10}$
CPACOD	00H	CMOS drivers
CPBCOD	00H	CMOS drivers
CADDHLT	X	"Don't care" A16–A19 not used
CSECURITY	1	Security on

Figure 12. 68HC11/PSD3XX Applications



8-BIT Non-Multiplexed PSD3XX Interface to M68008

Figure 13 illustrates an application in which the address and data are not multiplexed. The M68008 has an 8-bit data bus and 20-bit address bus. The PSD3XX can be programmed to support the microprocessor by providing data I/O through Port A. The address lines from the microprocessor go to inputs A0–A19. Port B outputs are used for external chip-selects to other MAP devices or other memory resources. The configuration has been set for compatibility with Motorola control signals. There are six chip-select outputs ($\overline{CS0}$–$\overline{CS5}$) and an address decode for $\overline{DTACK}$ and $\overline{BERR}$. The PAD decodes an address range which is fed back to the microprocessor through these inputs. Using the open-drain configuration has been implemented in Port B bits 6 and 7. The two pull-up resistors enable external memory and peripherals to access the $\overline{DTACK}$ and $\overline{BERR}$ inputs as a wired-OR function.

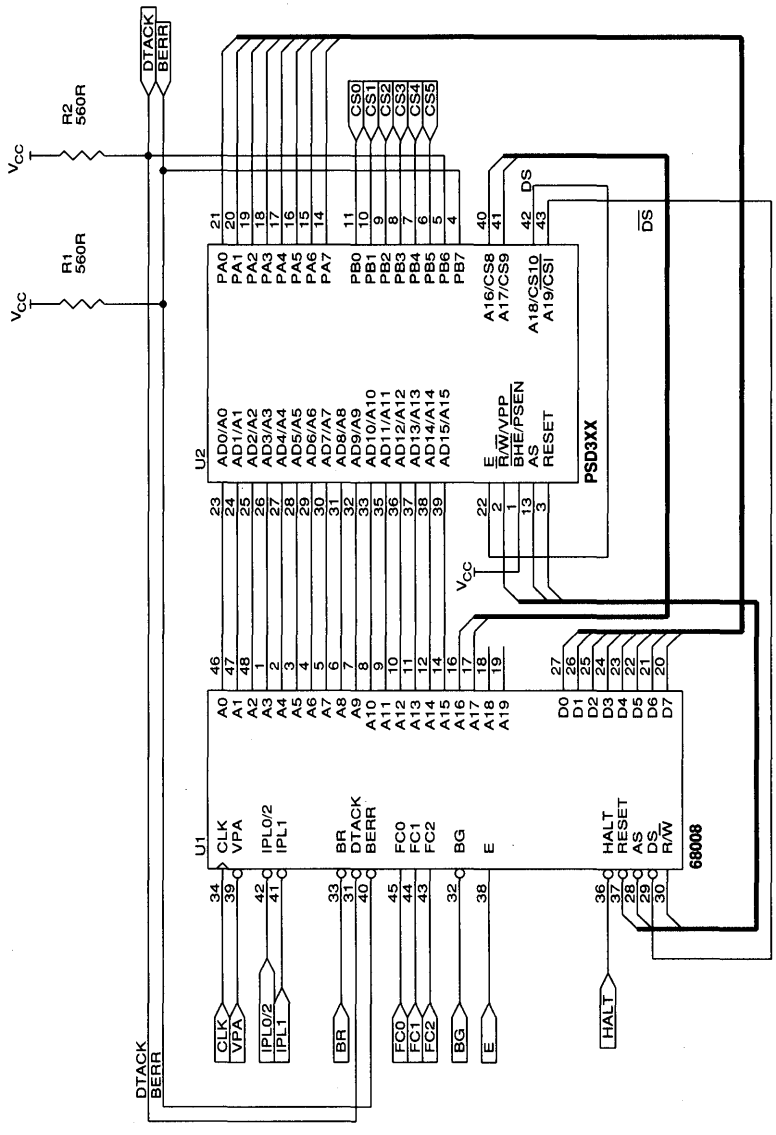
If other PSD3XX devices are mapped into the M68008 system, no additional glue logic is needed to avoid possible bus contention on these lines. In this application, ALE(AS) can be used as a general-purpose logic input to the PAD because the function of ALE becomes redundant in a non-multiplexed address/data bus. Also shown in Figure 13 is a method of inverting the active LOW $\overline{DS}$ (Data Strobe) M68008 output. The A19 input is enabled to the PSD internal PAD and inverted at the output of $\overline{CS10}$ to drive the PSD3XX E input. The E input must be active HIGH but $\overline{DS}$ is active LOW and qualifies a valid data transfer. Thus, the PAD must perform a signal inversion. The E signal output from the M68008 is used to interface to Motorola 8-bit peripherals. However, with Motorola microcontroller families such as the M68HC11, the E signal output can drive the E input to the PSD3XX. Table 6 gives the configuration information associated with the design given in Figure 13.

Table 6. M68008 to PSD3XX Interface

Configuration	Bits	Function
CDATA	0	8-bit data bus
CADDRDAT	0	Non-multiplexed address/data
CRRWR	1	Set R/$\overline{W}$ and E mode
CA19/$\overline{CSI}$	1	Enable A19 input[1]
CALE	X	"Don't care" non-multiplexed mode
CRESET	0	Active LOW RESET
$\overline{COMB}$/SEP	0	Combined memory mode
CPAF2	X	"Don't care" Port A used for data
CPAF1	XXH	"Don't care" Port A used for data
CPBF	00H	Port B used for chip-selects
CPCF	001B	Configure A16 and A17 In, $\overline{CS10}$ Out[2]
CPACOD	00H	CMOS drivers
CPBCOD	3FH	CMOS drivers, PB6, PB7 open drain
CADDHLT	0	Address latch transparent A16–A19
CSECURITY	1	Security on

1. The $\overline{DS}$ output from the M68008 drives the A19 input to the PSD3XX.
2. The internal PAD of the PSD3XX inverts the $\overline{DS}$ input to drive its own E input from the $\overline{CS10}$ PAD output. A16 and A17 are programmed as PSD inputs.

Figure 13. M68008/PSD3XX Applications



16-Bit Non-Multiplexed Address/Data PSD3XX Interface to M68000

An extension to the design is shown in Figure 14, with the configuration information shown in Table 7. The M68000 interface to the PSD3XX has a 16-bit data bus. Both Ports A and B are used to convey data. The generation of an E input to the PSD3XX has been extended from the signal inversion shown in Figure 13. The M68000 has two data strobe signals ($\overline{LDS}$ and $\overline{UDS}$), to qualify the lower and upper bytes of a 16-bit word. The $\overline{LDS}$ and $\overline{UDS}$ lines drive the A18 and A19 inputs and are gated to provide the correct logic condition into the M68000.

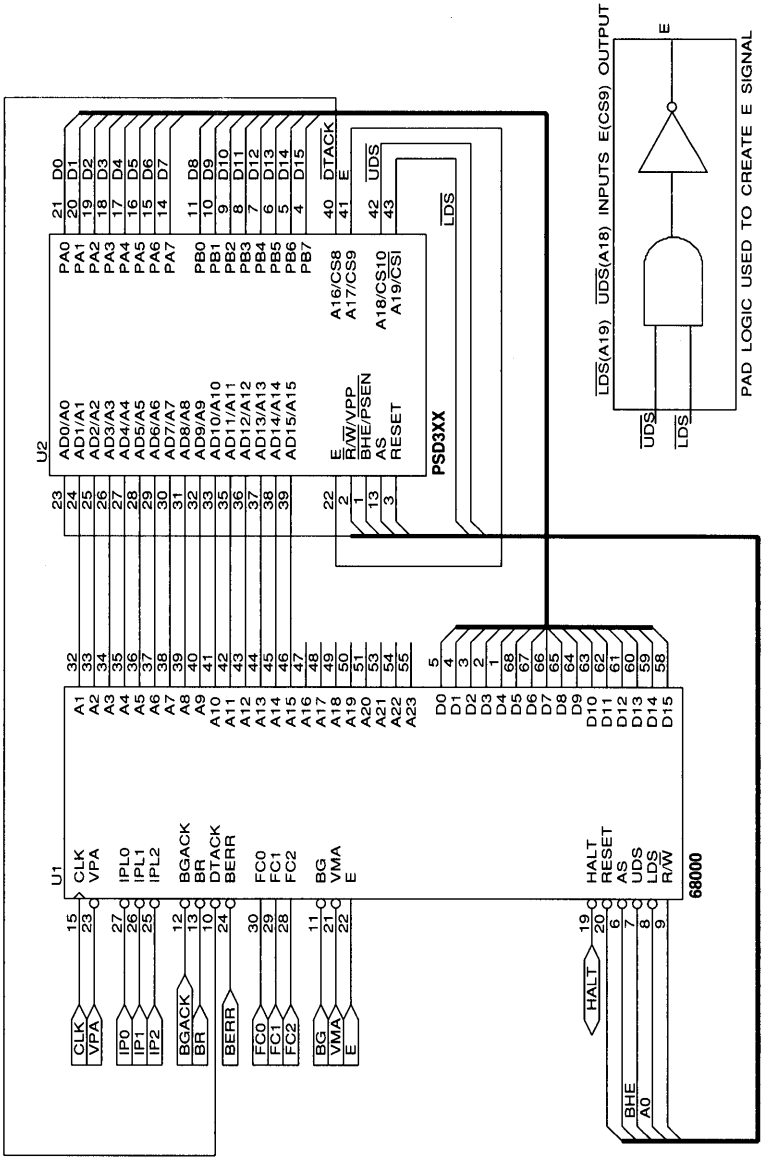
Table 7. M68000 Microprocessor to one PSD3XX Interface

Configuration	Bits	Function
CDATA	1	16-bit data bus
CADDRDAT	0	Non-multiplexed address/data
CRRWR	1	Set R/$\overline{W}$ and E control inputs
CA19/$\overline{CSI}$	1	Enable A19 input
CALE	X	ALE polarity set at "don't care"
CRESET	0	Active LOW RESET
$\overline{COMB}$/SEP	0	Combined memory mode
CPAF2	X	"Don't care" Port A
CPAF1	XX	"Don't care" Port A
CPBF	X	"Don't care" Port B
CPCF	110B	Enable A16 and A17 Out, A18 In[1]
CPACOD	00H	Configure CMOS buffers Port A
CPBCOD	00H	Configure CMOS buffers Port B
CADDHLT	0	Transparent A16–A19
CSECURITY	0	Security off

1. Outputs $\overline{UDS}$ and $\overline{LDS}$ drive the A18 and A19 inputs of the PAD and are gated internally to give a valid E input signal to the M68000 from the $\overline{CS9}$ output. DTACK comes from the $\overline{CS8}$ output.

This application takes advantage of the AS input which is redundant as a latch control input in a non-multiplexed system; however, it can be used as general-purpose logic input to the PAD. $\overline{CS9}$ and $\overline{CS8}$ are used as output signals to the M68000's DTACK and BERR inputs.

Figure 14. M68000/PSD3XX Applications



M68000/ 2X PSD3XX Applications

With the circuit design given in Figure 15, two PSD3XX devices are used in a byte-wide mode. One PSD stores the upper data byte and one the lower data byte of a 16-bit word. By using the devices in this way, two 6-bit wide ports can be created in Port B of each device. PB6 and PB7 are programmed as open-drain outputs and wired-OR giving composite DTACK and BERR feedback signals to the M68000. The generation of the E signal for both PSD devices is achieved in the same way it was in the M68008. The $\overline{LDS}$ and $\overline{UDS}$ inputs (to U2 and U3 respectively) are inverted by the PAD and drive the relevant E inputs. Table 8 gives the configuration information relevant to both PSD devices.

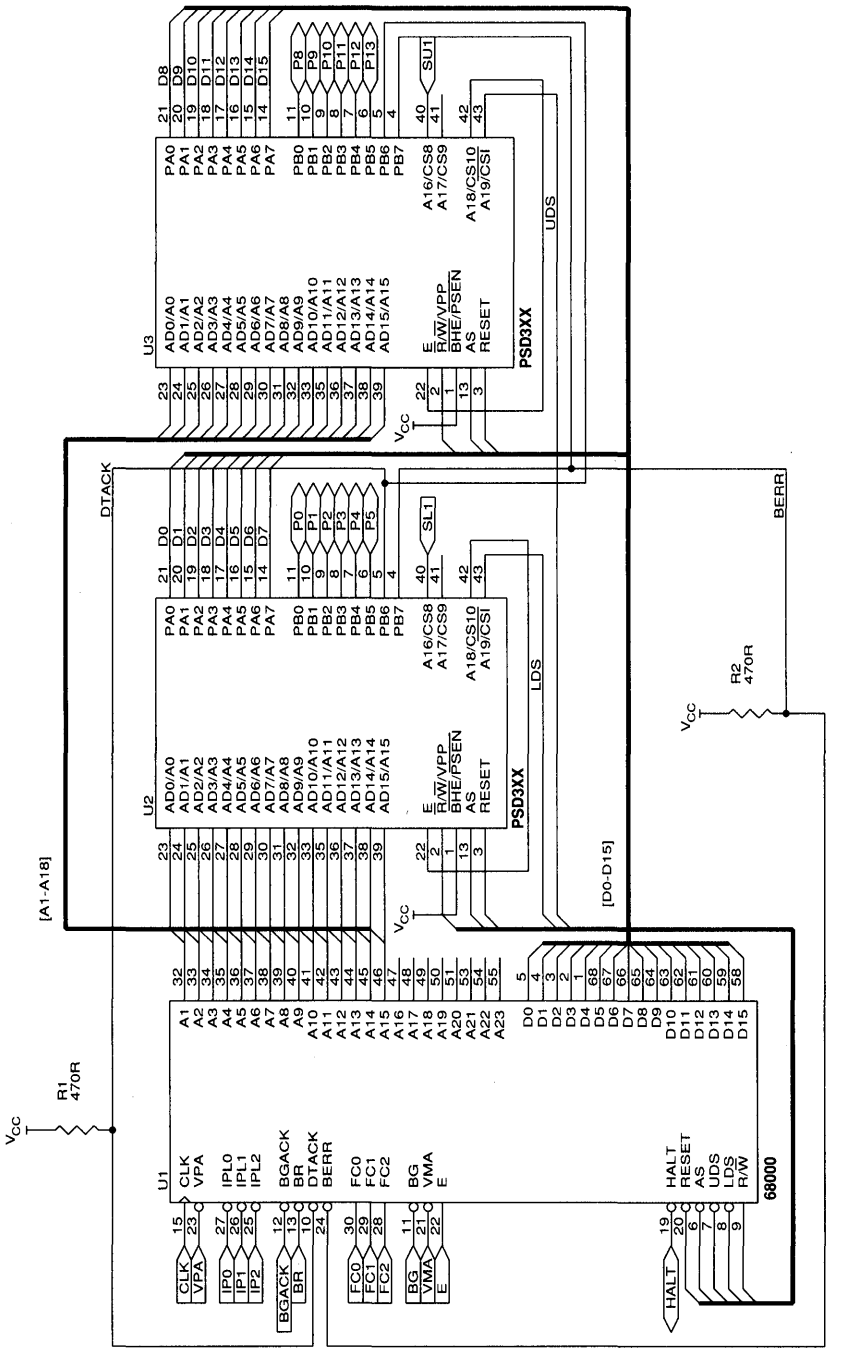
Table 8. M68000 Microprocessor to Two PSD3XX Devices in Parallel

Configuration	Bits	Function
CDATA	0	8-bit data bus
CADDRDAT	0	Non-multiplexed address/data
CRRWR	1	Set R/$\overline{W}$ and E control inputs
CA19/$\overline{CSI}$	1	Enable A19 input[1]
CALE	X	"Don't care" not used
CRESET	0	Active LOW RESET
$\overline{COMB}$/SEP	0	Combined memory mode
CPAF2	X	"Don't care" Port A used for data
CPAF1	XXH	"Don't care" Port A used for data
CPBF	FFH	Port B used for I/O
CPCF	111B	Configure $\overline{CS8}$–$\overline{CS10}$[2]
CPACOD	00H	CMOS drivers
CPBCOD	00H	CMOS drivers
CADDHLT	0	Transparent A19
CSECURITY	0	No security

1. A19 input to the PSD3XX's is used to receive $\overline{UDS}$ and $\overline{LDS}$ from the M68000 microprocessor. These signals are inverted by the PAD of each PSD3XX and fed back to the E input of each divice.

2. $\overline{CS10}$ of each PSD3XX drives the inverted $\overline{UDS}$ and $\overline{LDS}$ back to E input. Port C is programmed to output $\overline{CS8}$ and $\overline{CS9}$. Additional byte-wide peripherals can be configured to the system and selected by these signals.

Figure 15. M68000/ 2X PSD3XX Applications



16- Bit Address/ Data PSD3XX Interface to Intel 80186

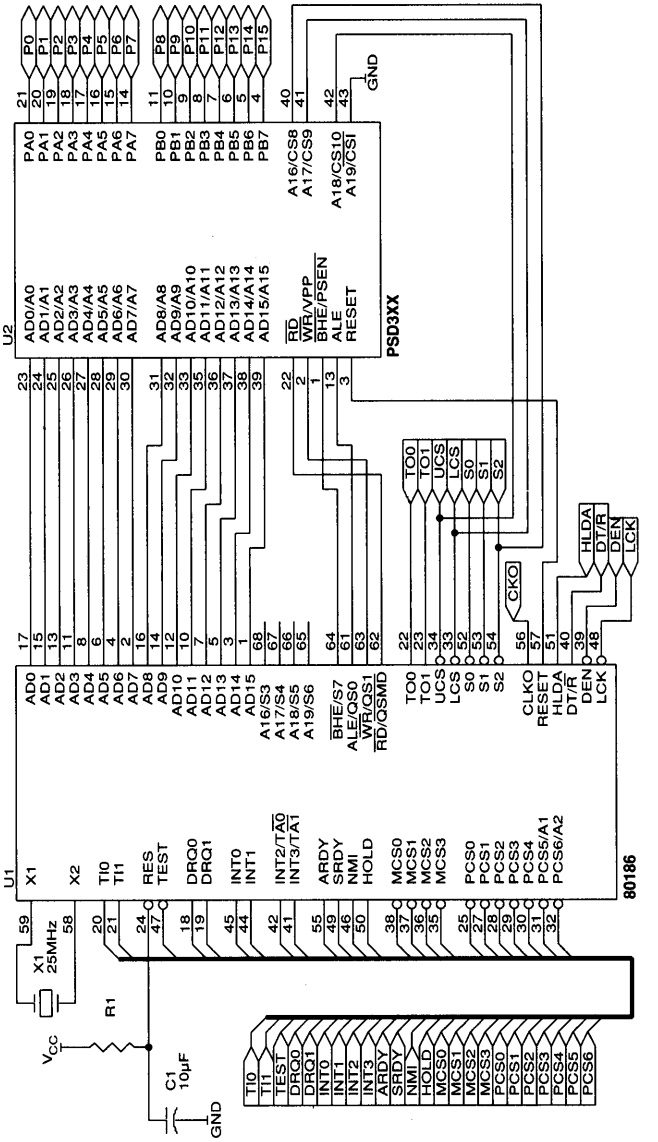
Figure 16 and Table 9 give the configuration of the PSD3XX in an Intel 80186 system. This device has a 16-bit multiplexed address/data bus. Ports A and B are used for data I/O functions, so this design can take advantage of the port expansion capability. To distinguish between memory and I/O functions, it is necessary to decode the S2 output from the 80186. This output line goes directly to the PAD through Port C bit zero. When LOW, this signal qualifies a memory access; when HIGH, it indicates that an I/O operation is in progress. Programming the PAD can use this input to differentiate between I/O and memory access.

Two additional signals from the 80186 are $\overline{UCS}$ and $\overline{LCS}$ (upper chip-select and lower chip-select, respectively). The signals have been included in the system to help minimize the requirement for additional glue logic. Both can be used in the PAD decoder to position sections of EPROM and RAM. The $\overline{UCS}$ is designed to decode addresses FFFFFH to a programmable limit. The 80186 begins executing from memory location FFFF0H after a system reset; thus, this signal should be used to select EPROM that contain a system initialization sequence. The $\overline{LCS}$ has been designed to program from 00000H up to a programmable limit. In this example, the RESET line from the 80186 is active HIGH and drives the RESET input of the PSD301 which is programmed to respond to a HIGH level.

Table 9. Intel 80186 to PSD3XX Configuration for CMOS Ports

Configuration	Bits	Function
CDATA	1	16-bit data bus
CADDRDAT	1	Multiplexed address/data
CRRWR	1	Set $\overline{RD}$ and $\overline{WR}$ mode
CA19/$\overline{CSI}$	1	$\overline{CSI}$ input to PAD
CALE	X	Active HIGH ALE
CRESET	0	Active LOW RESET
$\overline{COMB}$/SEP	0	Combined memory mode
CPAF2	X	I/O Port A
CPAF1	XXH	I/O Port A
CPBF	FFH	I/O Port B
CPCF	000B	Input A16–A18
CPACOD	00H	CMOS drivers
CPBCOD	00H	CMOS drivers
CADDHLT	0	Latched A16–A19
CSECURITY	0	No security

Figure 16. Intel 80186/ PSD3XX Applications



16-Bit Address/Data PSD3XX to Intel 80196 Interface

In Figure 17, the PSD3XX is connected to an Intel 80196 microcontroller. In many microcontroller applications it is necessary to illuminate indicators (such as LEDs). Here, the PSD3XX is used to drive LED indicator displays. High-efficiency LEDs can be illuminated through the open drain outputs of Port B. The configuration information in Table 10 indicates that Port B has open drain drivers to sink LED illumination current.

Table 10. Intel 80196 to PSD3XX Configuration for LED Drivers

Configuration	Bits	Function
CDATA	1	16-bit data bus
CADDRDAT	1	Multiplexed address/data
CRRWR	0	Set $\overline{RD}$ and $\overline{WR}$ mode
CA19/$\overline{CSI}$	X	"Don't care" A19/$\overline{CSI}$
CALE	0	Active HIGH ALE
CRESET	0	Active LOW RESET
$\overline{COMB}$/SEP	0	Combined memory mode
CPAF2	0	I/O Port A
CPAF1	00H	I/O Port A
CPBF	FFH	I/O Port B
CPCF	000B	Output A16–A18
CPACOD	00H	CMOS drivers
CPBCOD	FFH	Open drain drivers
CADDHLT	X	"Don't care" (not used)
CSECURITY	0	No security

Interfacing the PSD3XX to 8-Bit Microprocessors Z80 and M6809 Applications

Figures 18 and 19 illustrate the PSD3XX used with 8-bit microprocessors, such as the Z80B and M6809B. Tables 11 and 12 reflect the configuration of each design, respectively. The mode of operation is 8-bit data bus with a non-multiplexed address/data input. In the case of the Z80B, $\overline{CS8}$–$\overline{CS10}$ inputs are tied to $\overline{M1}$, $\overline{MREQ}$, and $\overline{IORQ}$ respectively. Since the PAD can be programmed to distinguish between memory and I/O operations, the Z80B system has access to an 8-bit data port Port B. With the M6809B system, $\overline{CS8}$ is used to respond to the MRDY input of the microprocessor and $\overline{CS9}$ and $\overline{CS10}$ are available for external chip-select.

Figure 17. Intel 80196/ PSD3XX Application Open Drain Drivers

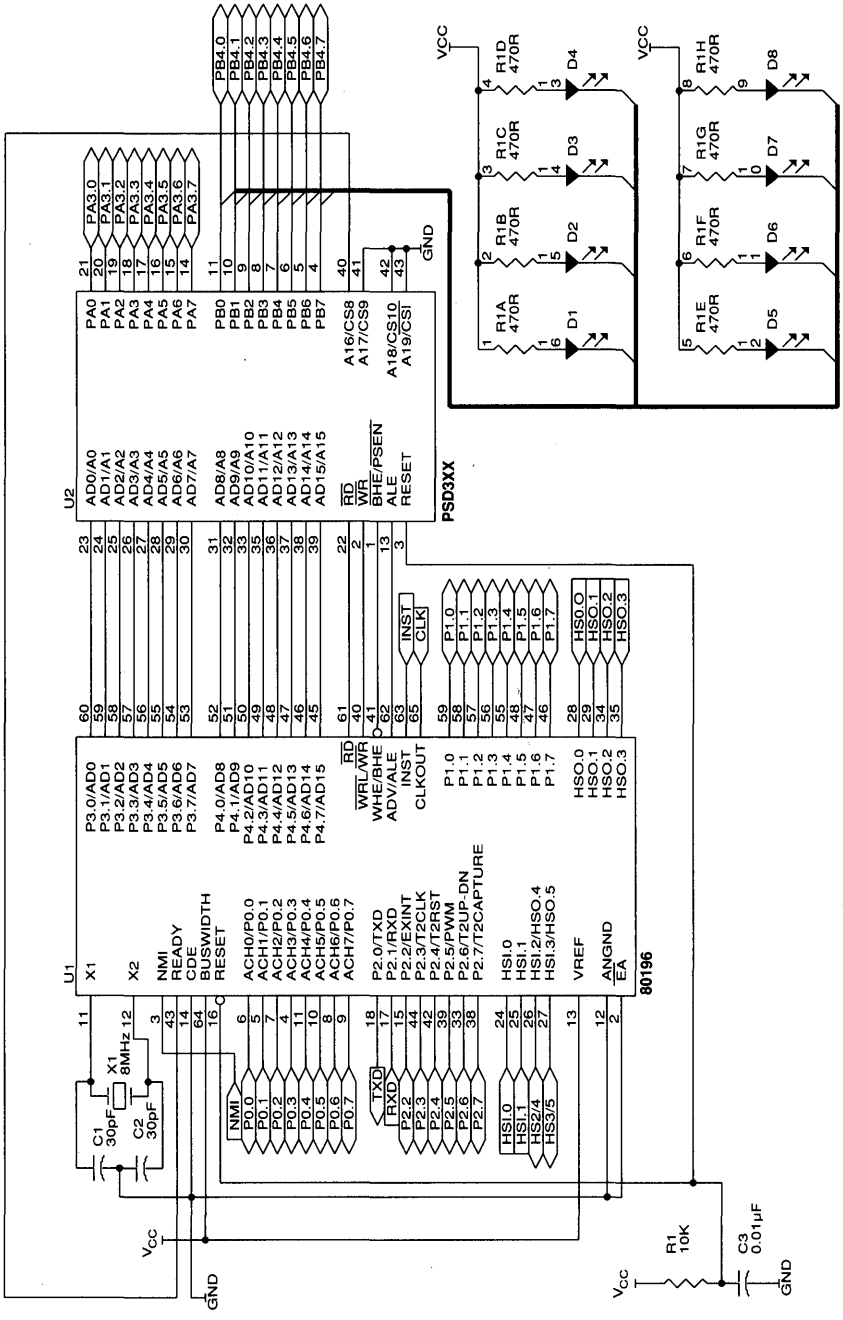


Table 11. Z80B to PSD3XX Interface

Configuration	Bits	Function
CDATA	0	8-bit data bus
CADDRDAT	0	Non-multiplexed address/data
CRRWR	0	Set $\overline{RD}$ and $\overline{WR}$ mode
CA19/$\overline{CSI}$	0	$\overline{CSI}$ input
CALE	X	"Don't care" (not used)
CRESET	0	Active LOW RESET
$\overline{COMB}$/SEP	0	Combined memory mode
CPAF2	X	"Don't care" Port A used for data
CPAF1	XXH	"Don't care" Port A used for data
CPBF	FFH	I/O Port B
CPCF	000B	Configure A16–A18 as inputs
CPACOD	00H	CMOS drivers
CPBCOD	00H	CMOS drivers
CADDHLT	0	A16–A18 transparent[1]
CSECURITY	0	No security

1. A16–A18 inputs are used as $\overline{M1}$, $\overline{MREQ}$, and $\overline{IORQ}$ inputs to the PAD from the Z80B output. Use the ALIAS command in the support software.

Table 12. M6809 to PSD3XX Interface

Configuration	Bits	Function
CDATA	0	8-bit data bus
CADDRDAT	0	Non-multiplexed address/data
CRRWR	1	Set R/$\overline{W}$ and E mode
CA19/$\overline{CSI}$	0	Enable $\overline{CSI}$ input
CALE	X	"Don't care" non-multiplexed mode
CRESET	0	Active LOW RESET
$\overline{COMB}$/SEP	0	Combined memory mode
CPAF2	X	"Don't care" Port A used for data
CPAF1	XXH	"Don't care" Port A used for data
CPBF	FFH	Port B used for I/O
CPCF	111B	$\overline{CS8}$–$\overline{CS10}$ outputs
CPACOD	00H	CMOS drivers
CPBCOD	00H	CMOS drivers
CADDHLT	0	"Don't care"
CSECURITY	0	No security

Figure 18
Z80B/PSD3XX
Applications

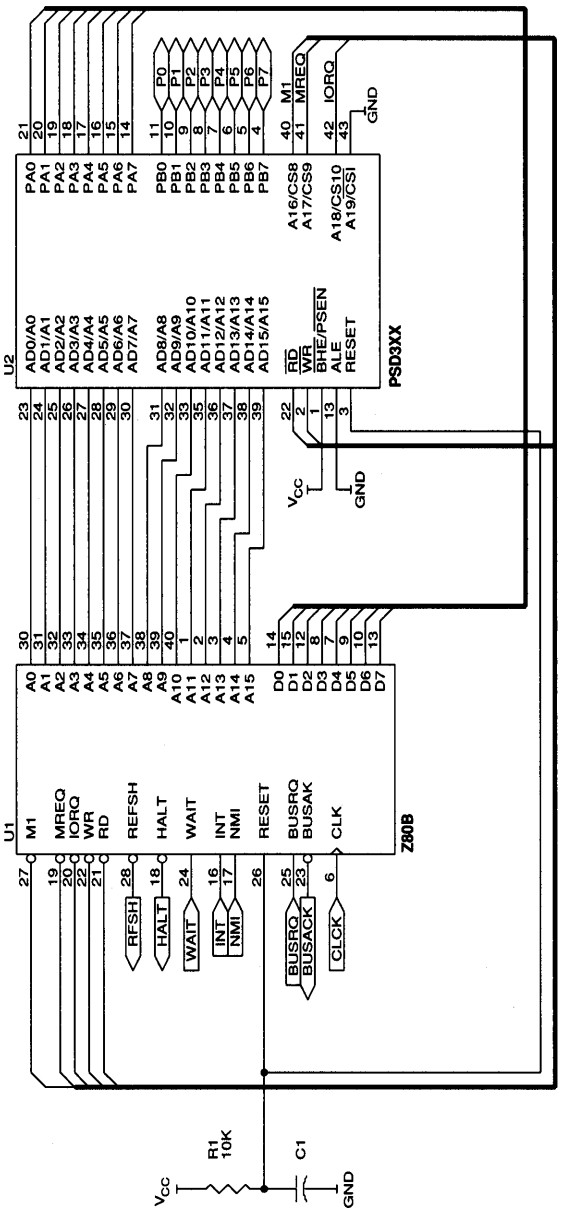
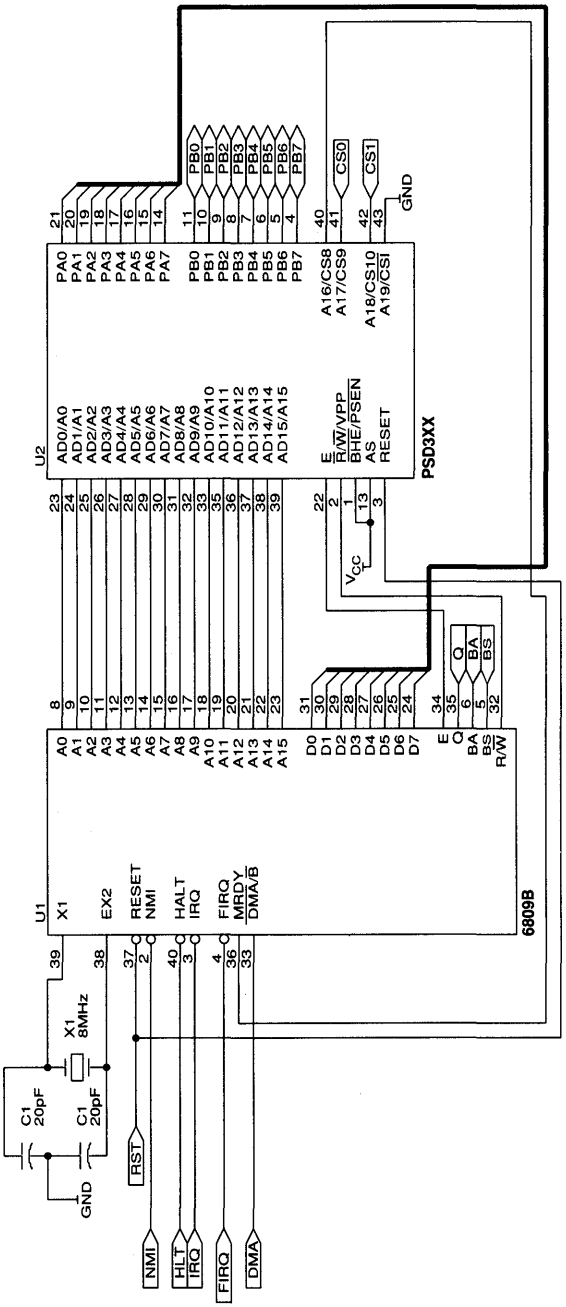


Figure 19
6809/PSD3XX
Applications



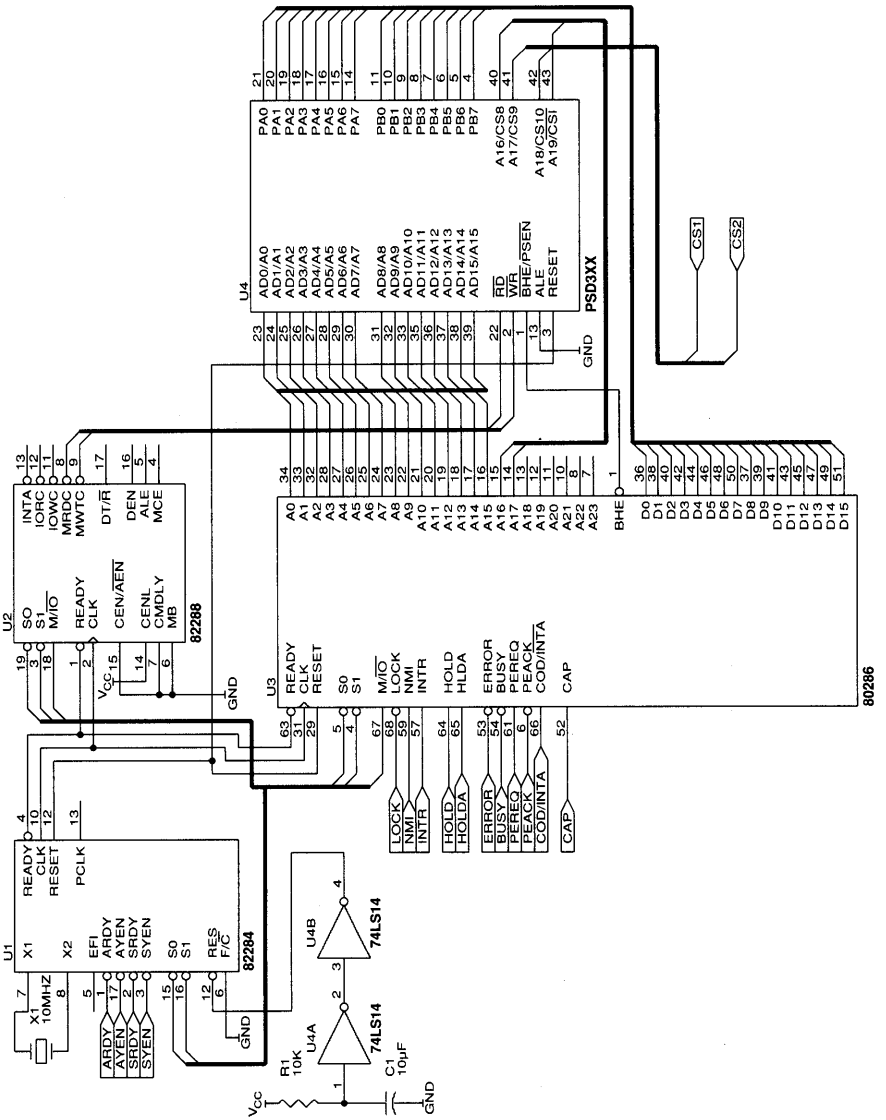
PSD3XX Interface to the Intel 80286

Figure 20 provides a schematic of the PSD3XX interface to an 80286. The device is configured for a 16-bit data bus in the non-multiplexed mode. Ports A and B are converted automatically for use as a bi-directional data path into the PSD3XX. (This was also the case for the M68000 microprocessor). To eliminate (or lessen) glue logic, $\overline{CS1}$ and $\overline{CS2}$ are generated from the internal PAD. This is programmed as an address decoder. Table 13 provides configuration information relevant to this system design.

Table 13. Intel 80286 to PSD3XX Interface

Configuration	Bits	Function
CDATA	1	16-bit data bus
CADDRDAT	0	Non-multiplexed address/data
CRRWR	0	Set $\overline{RD}$ and $\overline{WR}$ control inputs
CA19/$\overline{CSI}$	1	Enable A19 input
CALE	X	"Don't care" non-multiplexed mode
CRESET	1	Active HIGH RESET
$\overline{COMB}$/SEP	0	Combined memory mode
CPAF2	X	"Don't care" Port A used for data
CPAF1	XXH	"Don't care" Port A used for data
CPBF	XXH	"Don't care" Port B used for data
CPCF	011B	A16 input; $\overline{CS9}$ and $\overline{CS10}$ outputs
CPACOD	00H	CMOS drivers
CPBCOD	00H	CMOS drivers
CADDHLT	0	Transparent A16–A19 input
CSECURITY	0	No security

Figure 20 Intel 80286/ PSD3XX Applications



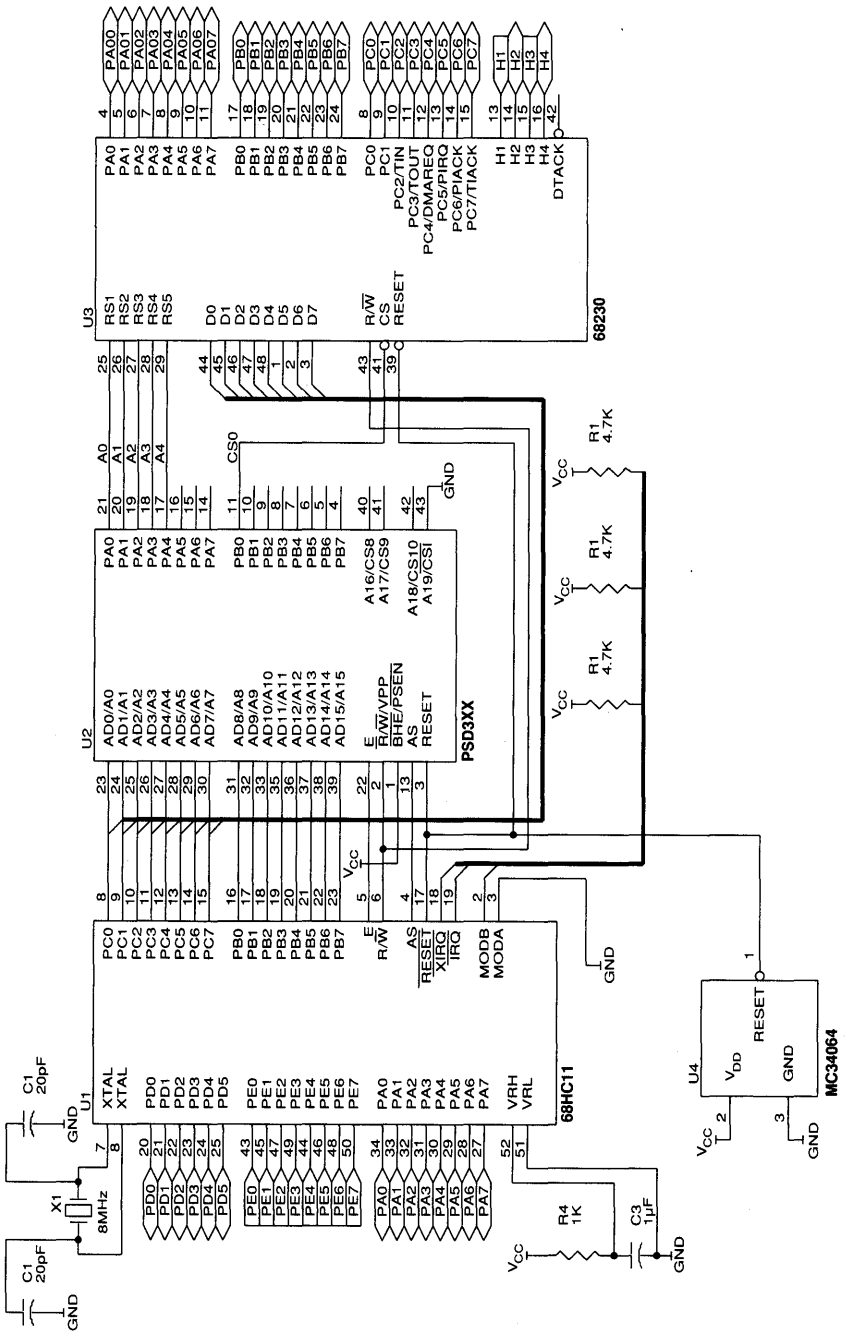
External Peripherals to the PSD3XX/M68HC11 Configuration

The configuration in Figure 21 illustrates how the user can feed address outputs from the internal latch to Port A. Addresses A0–A7, derived from a multiplexed address/data bus, can go directly to an additional peripheral without the need for an additional octal latch such as the 74HC373 or 74HC573. Port A can be used for address outputs A0–A7 while PB0–PB7 can be used as chip-selects. Lines A0–A4 of the PSD3XX drive the RS1–RS5 register select inputs of the M68230. For the M68HC11, the eight bits of address and data come from its PC port PC0–PC7 (AD0–AD7) and are latched by the AS input. Configured in this mode, the PSD3XX can address and map additional peripheral chips. Port A of the PSD3XX conveys the internally latched address outputs A0–A7 to the output and can be used to address registers in the peripheral chips while Port B outputs can place individual peripherals at peripheral or memory-mapped boundaries. Thus, a number of additional chips can be selected through Port B. This effectively can increase the port density of the system design. The general I/O capability can then be extended to extra ports, timers, UARTs, serial communications channels, keyboard interface devices, CRT controllers, etc. without the need for additional glue logic. Table 14 highlights the configuration information programmed into the PSD3XX when configuring the M68HC11 to a M68230 peripheral.

Table 14. M68HC11/PSD3XX to External Peripheral M68230 Interface

Configuration	Bits	Function
CDATA	0	8-bit data bus
CADDRDAT	1	Multiplexed address/data
CRRWR	1	Set R/$\overline{W}$ and E mode
CA19/$\overline{CSI}$	0	Set power-down mode
CALE	0	Active HIGH AS
CRESET	0	Active LOW RESET
$\overline{COMB}$/SEP	0	Combined memory mode
CPAF2	0	Port A = address A0–A7
CPAF1	FFH	Port A set for address
CPBF	00H	Port B set for chip-select
CPCF	111B	Port C set for chip-select
CPACOD	00H	CMOS buffers
CPBCOD	00H	CMOS buffers
CADDHLT	X	"Don't care"
CSECURITY	0	No security

Figure 21
M68HC11/PSD3XX
to M68230
Applications



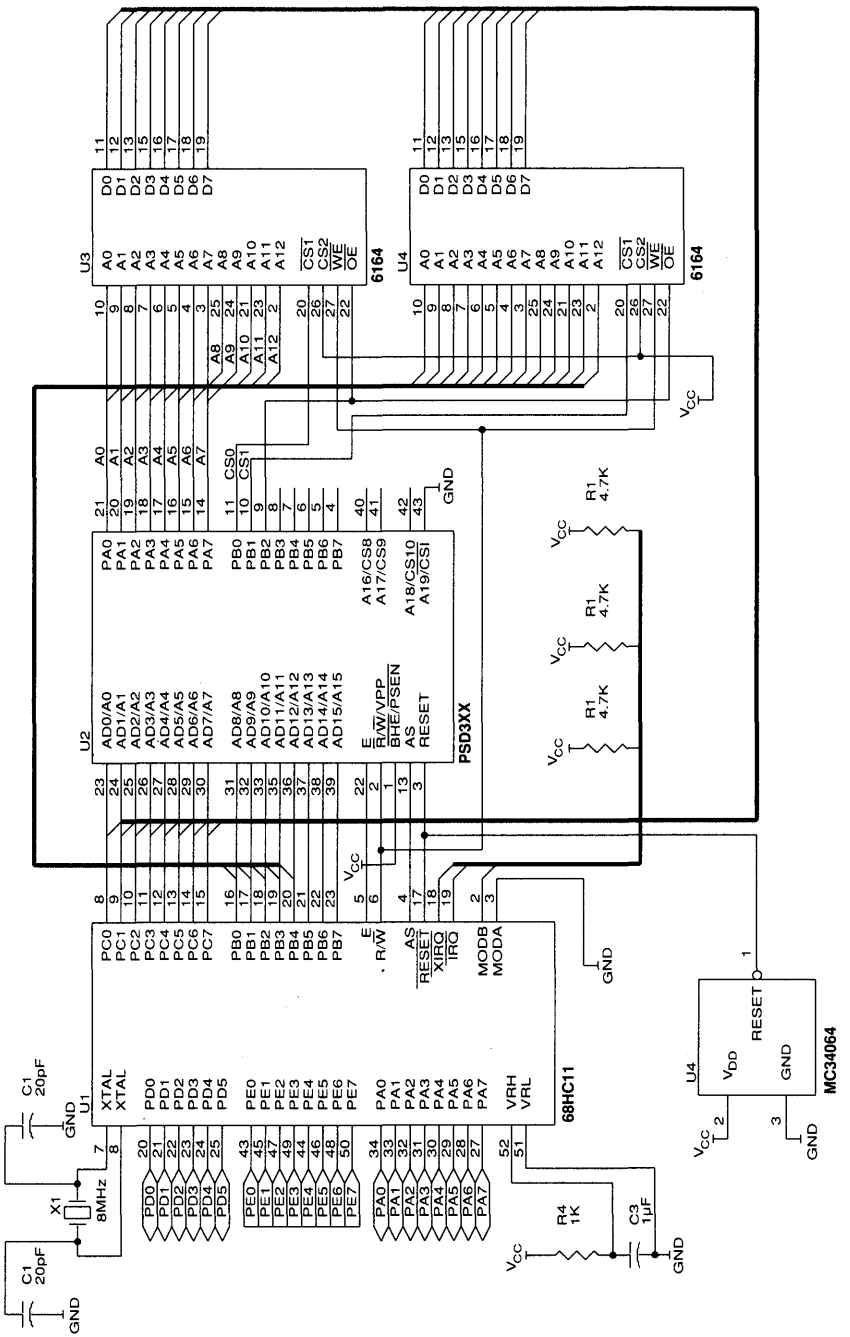
Additional External SRAM

Figure 22 illustrates how additional SRAMs can be configured into a system. This PSD3XX configuration is not limited to external peripheral expansion; it can also be used to add additional memory without the need for external glue logic. With an 8-bit address/data multiplexed scheme, the higher-order addresses (A8–A15) are non-multiplexed. These address lines are fed directly to the external SRAM from the microcontroller and do not need to go through the PSD3XX These lines can drive the RAM chip directly. Thus the M68HC11 system, which is highly memory-intensive and requires more RAM than the microcontroller and PSD3XX can supply, can take advantage of the configuration shown in Figure 23 which is detailed in Table 15.

Table 15. M68HC11/PSD3XX Configured to Address Additional SRAM

Configuration	Bits	Function
CDATA	1	8-bit data bus
CADDRDAT	0	Multiplexed address/data
CRRWR	1	Set R/$\overline{W}$ and E mode
CA19/$\overline{CSI}$	1	Set power-down mode
CALE	0	Active HIGH AS
CRESET	0	Active LOW RESET
$\overline{COMB}$/SEP	0	Combined memory mode
CPAF2	0	Port A = address A0–A7
CPAF1	FFH	Port A set for address
CPBF	00H	Port B set for chip-select
CPCF	111B	Port C set for chip-select
CPACOD	00H	CMOS buffers
CPBCOD	00H	CMOS buffers
CADDHLT	X	Latched A16–A19 "don't care"
CSECURITY	0	No security

Figure 22. M68HC11/PSD3XX to 16K SRAM Applications



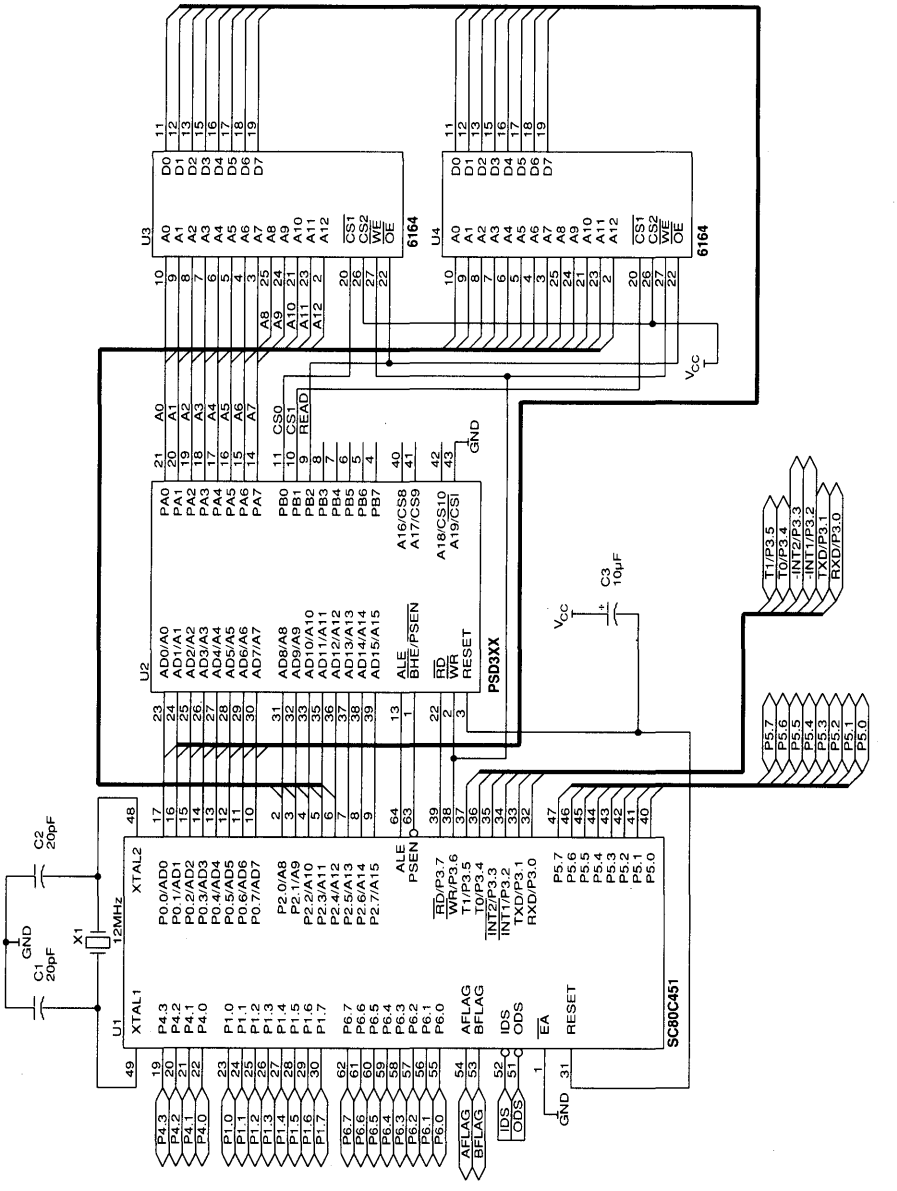
Additional External SRAM (Cont.)

Figure 23 illustrates, and Table 16 details, a similar system using the Signetics SC80C451. This microcontroller has many ports and some SRAM but requires off-chip EPROM to store programmed instructions. This device is similar to the 8051/31 family which uses the active LOW $\overline{PSEN}$ signal to differentiate between executable code and data. Since it is a multiplexed 8-bit machine, it can use the on-chip latches. In highly RAM-intensive applications, an additional two 8K x 8 SRAM chips can be included and selected through Port B. If additional SRAM chips are not needed, Ports A and B can recreate Ports 0 and 2 which are lost in addressing external memory.

Table 16. SC80C451/ PSD3XX Configured to Address Additional SRAM

Configuration	Bits	Function
CDATA	1	8-bit data bus
CADDRDAT	0	Multiplexed address/data
CRRWR	0	Set $\overline{RD}$ and $\overline{WR}$ mode
CA19/$\overline{CSI}$	0	Set power-down mode
CALE	0	Active HIGH ALE
CRESET	1	Active HIGH RESET
$\overline{COMB}$/SEP	1	Separate data/program memory
$CPAF_2$	0	Port A = address A0–A7
$CPAF_1$	FFH	Port A set for address
CPBF	00H	Port B set for chip-select
CPCF	111B	Port C set for chip-select
CPACOD	00H	CMOS buffers
CPBCOD	00H	CMOS buffers
CADDHLT	0	"Don't care" (not used)
CSECURITY	0	No security

Figure 23. SC80C451/ PSD3XX to 16K SRAM Applications



PSD3XX Used in Track Mode

Figure 24 illustrates a design that utilizes the track mode of operation that has been discussed but not illustrated in an application. Here, Port A passes or tracks through the multiplexed address and data of the 80196. Address and data outputs AD0–AD7 from the 80196 appear on the PSD3XX Port A pins. In this mode, the SRAM, shown in Figure 24 as U4, can be accessed either by the 80196 (used in byte mode) or by a second processor in the host system. The SRAM in the design can be used as a common resource. An example would be a system in which the host uses the memory to pass parameters to the local 80196. Table 17 gives the configuration data for an 80196/PSD301 interface to SRAM using Track Mode.

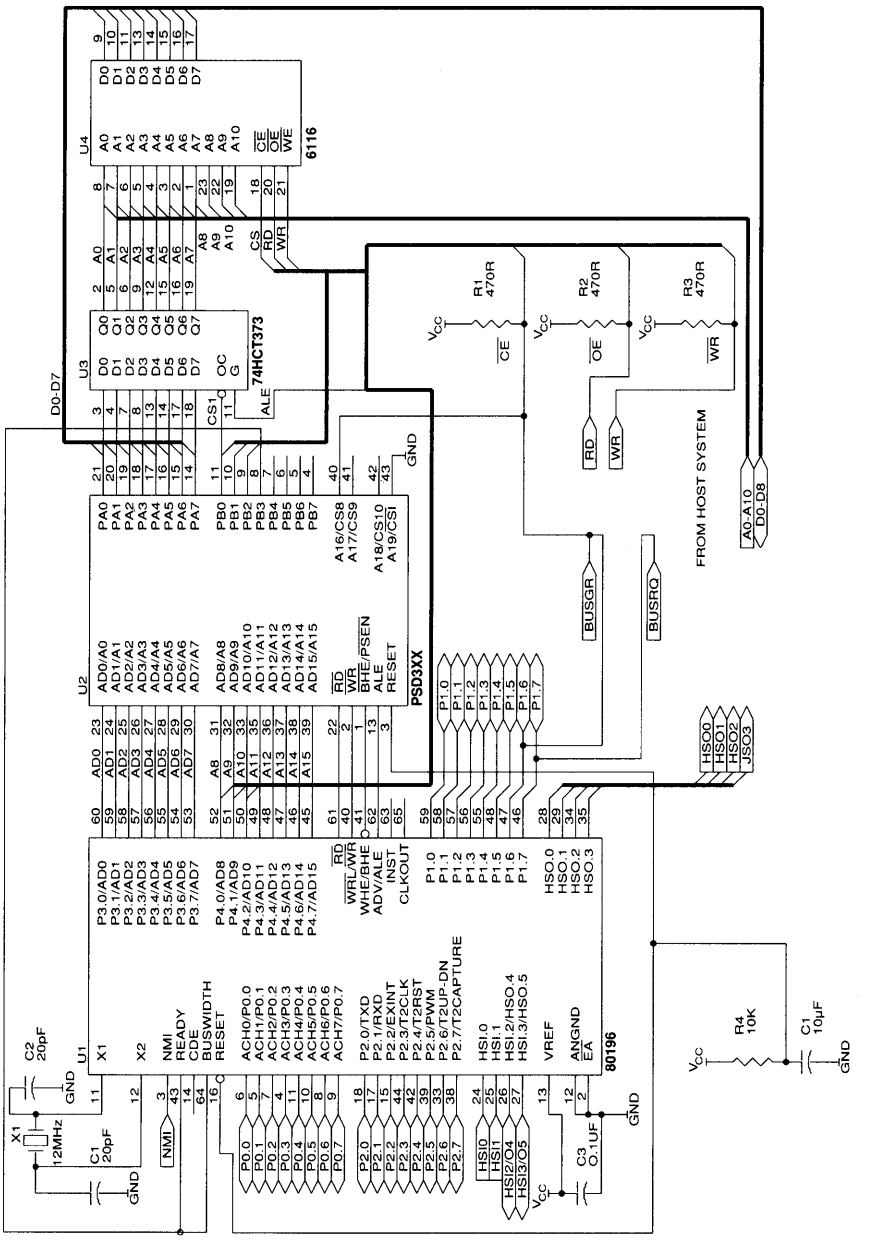
A Direct Memory Access can transfer data to the common memory via a BUSRQ/BUSGR handshake. Note that the PAD in the PSD3XX controls the three-state condition of the octal latch U3 74HCT373 enabling the host system to control SRAM addresses A0–A7. Port A of the PSD3XX is also put into a three-state condition during host-to-SRAM activity. In the design given in Figure 24, Port B outputs PB0, PB1, and PB2 are used to control the SRAM inputs $\overline{CE}$, $\overline{OE}$, and $\overline{WR}$ respectively. Also, A8, A9, and A10 are fed through the PAD as identity functions to the open drain drivers of PB3, PB4, and PB5 respectively. There is no track-through feature for these address lines; however, if they are fed through the PAD, they can drive the external memory resource as if they were tracked through.

The M80196 can operate in either byte- or word-wide mode controlled by its BUSWIDTH input. In this application, the PB6 output drives the BUSWIDTH line to switch between the byte-wide bus of the external SRAM and the word-wide interface of the PSD3XX. All Port B outputs, with the exception of PB6, are configured as open-drain. Provided the host system also has open drain/ collector drivers, both systems can access the SRAM without bus conflict. The only additional circuitry required would be the pull-up resistors.

Table 17. Intel 80196 to PSD3XX Used to Access External SRAM in Track Mode

Configuration	Bits	Function
CDATA	1	16-bit data bus
CADDRDAT	1	Multiplexed address/data
CRRWR	0	Set $\overline{RD}$ and $\overline{WR}$ mode
CA19/$\overline{CSI}$	0	Set power-down mode
CALE	0	Active HIGH ALE
CRESET	0	Active LOW RESET
$\overline{COMB}$/SEP	0	Separate data/program memory
CPAF2	1	Address/data (Track Mode)
CPAF1	XXH	"Don't care" in Track Mode
CPBF	00H	Port B set for chip-select outputs
CPCF	111B	Port C set for logic outputs
CPACOD	00H	CMOS buffers
CPBCOD	FFH	Open drain buffers
CADDHLT	X	Latched A16–A19 "don't care"
CSECURITY	0	No security

Figure 24. Intel 80196/ PSD3XX Track Mode to External SRAM



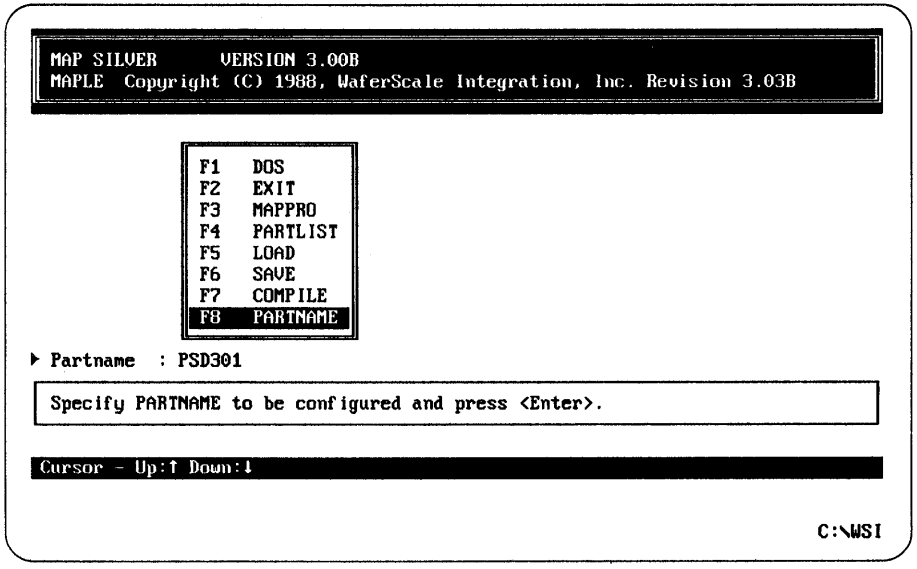
PSD3XX Device Description PSD3XX

Chapter 3

The support software for the PSD3XX family is designed to run on IBM PC XT/AT or 100% compatible systems. It is menu-driven and very user-friendly. In many cases it has the capability of preventing the user from creating invalid configurations. For example, in a non-multiplexed system with a 16-bit data bus, Ports A and B are used for data I/O. The software recognizes this and prevents the user from inadvertently programming Ports A and B as regular ports.

When running in the IBM PC environment, the PSD development software creates the menu shown in Figure 25. Initially, the designer selects the part type with the user key F8 or moves the screen cursor to PARTNAME. In the example shown, the selection for the part type is PSD301.

Figure 25. MAPLE Main Menu



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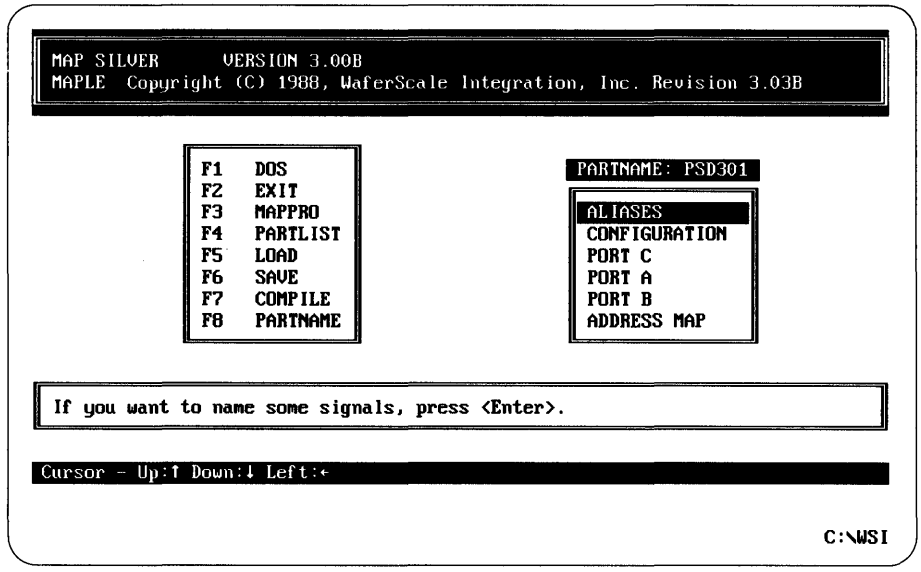
The menu listed to the left of Figure 25 links the function keys and their association. F1 suspends the MAPLE software to DOS for file editing or updating. F2 exits the program and returns the user to the DOS environment. F3 selects the programmer option so the user can program the compiled object file into the PSD301 device provided a programmer is connected to the system. The LOAD selection (F5), loads an existing program into the MAPLE environment for editing and compiling. F6 saves that program under a user-defined name. F7 compiles the user-generated file into an object file that can be transferred to the programmer. F8 provides part type selection, either PSD301 or MAP168.

Figure 26 illustrates a second menu to the right of the main menu. The list shows ALIASES, CONFIGURATION, PORT C, PORT A, PORT B, and ADDRESS MAP. The designer selects each choice, starting from ALIASES, and moves down through the list configuring each option.

Figure 26. MAPLE Menu with PARTNAME Submenu



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ALIASES Menu

The ALIASES selection lets the user individually define the port pins with user-relevant names. The circuit diagram shown in Figure 13 uses an M68008 processor, with BERR and DTACK signals coming from the PAD, as well as the remaining CS0, CS5 chip-select outputs.

Figure 27. CONFIGURATION Menu

Figure 27 gives the CONFIGURATION menu. In this case, the PSD301 has been configured for the system shown in Figure 10: interfacing to an 80C31; the 8-bit data/address bus is multiplexed. The chip-select input is chosen over the A19 input. The RESET and ALE polarity is set as active HIGH with $\overline{RD}$ and $\overline{WR}$ control inputs enabled. The inputs A16–A19 are transparent and separate strobes are enabled for SRAM and EPROM. This feature activates the $\overline{PSEN}$ input. In this configuration it is possible for the SRAM and EPROM to share the same address space. After the device is configured, Ports A, B, and C can be set up. If the main menu is invoked by selecting F1 (Figure 28), Port C can be selected as shown in Figure 26. Here, the individual selection of $\overline{CS}$/Ai configures the three pins as outputs.

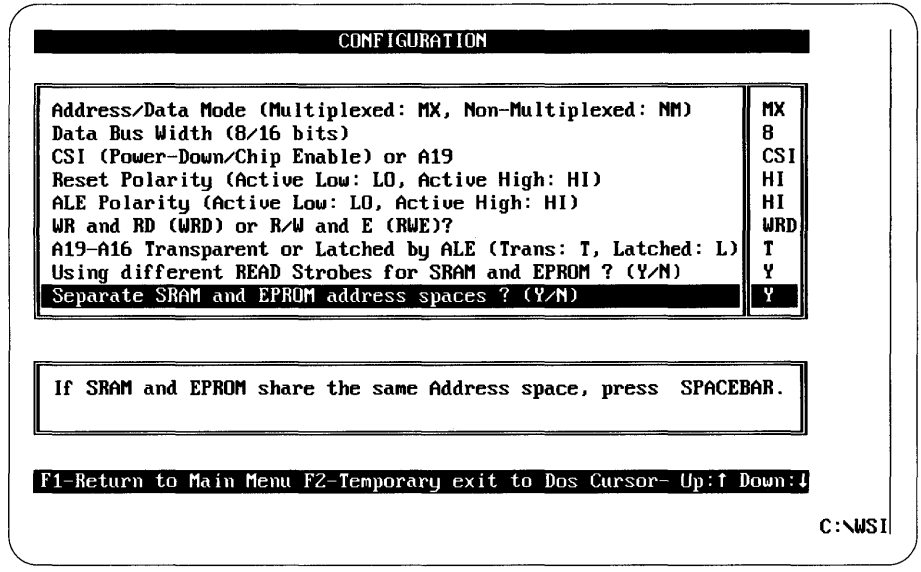

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Figure 28. Port C Configuration Menu

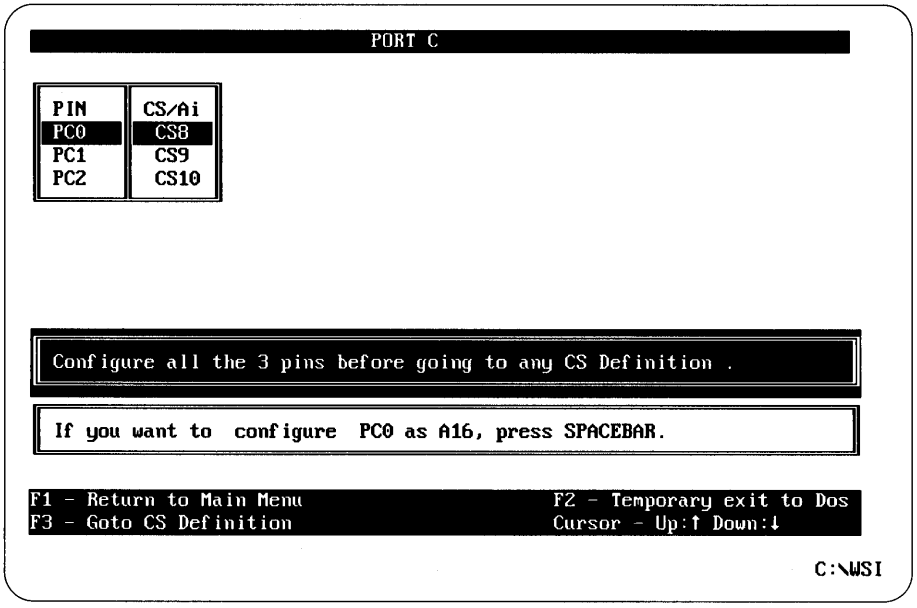

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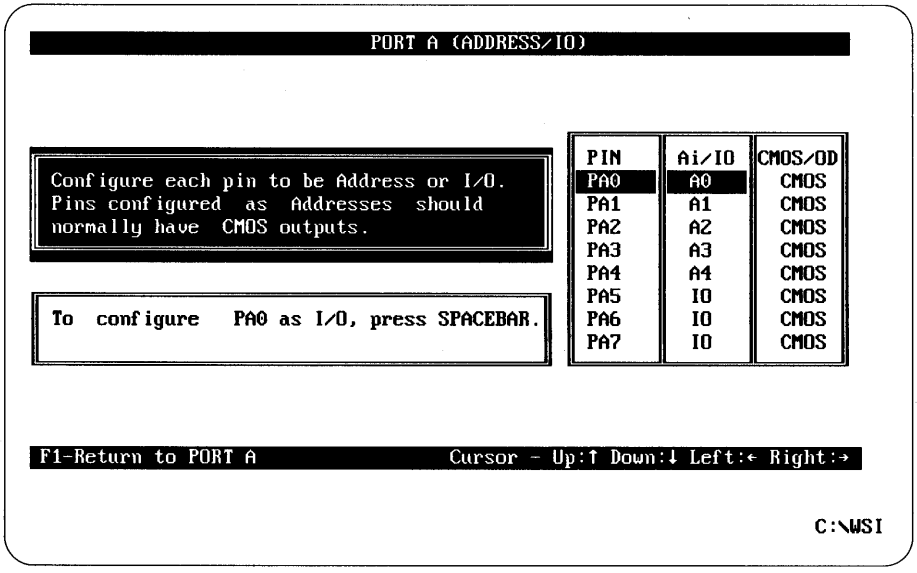
Figure 29. Port A Configuration Menu, Part 1.

Figure 29 shows the configuration of Port A. This could be applied to the example shown in Figure 21 which shows the PSD301 interfacing to an M68230. Port A passes the PSD301's internally latched address lines A0–A4 directly to the M68230. PA5–PA7 are configured as port outputs and can be used as general I/Os.



2402 29

Figure 30. Port A Configuration Menu, Part 2.

Port A can be programmed to be either address I/O or track mode, as illustrated in Figure 30. Track mode is selected if the designer wants to program the device as shown in Figure 24.

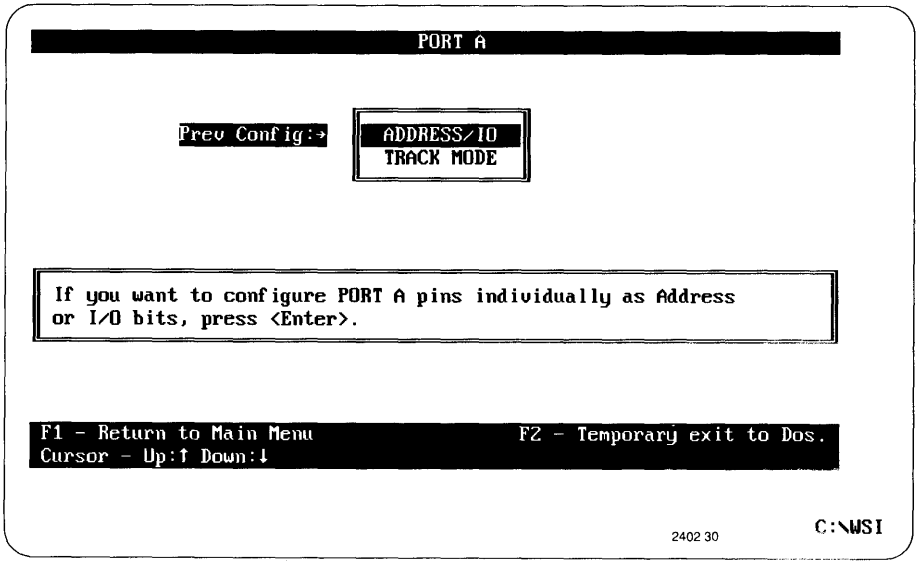


Figure 31. Port B Configuration Menu

Figure 31 gives the configuration of Port B. This is similar to the configuration pattern for the M68008 shown in Figure 13. Here, $\overline{CS6}$ and $\overline{CS7}$ have been programmed as open-drain outputs connected to the microprocessor's $\overline{DTACK}$ and $\overline{BERR}$, respectively.

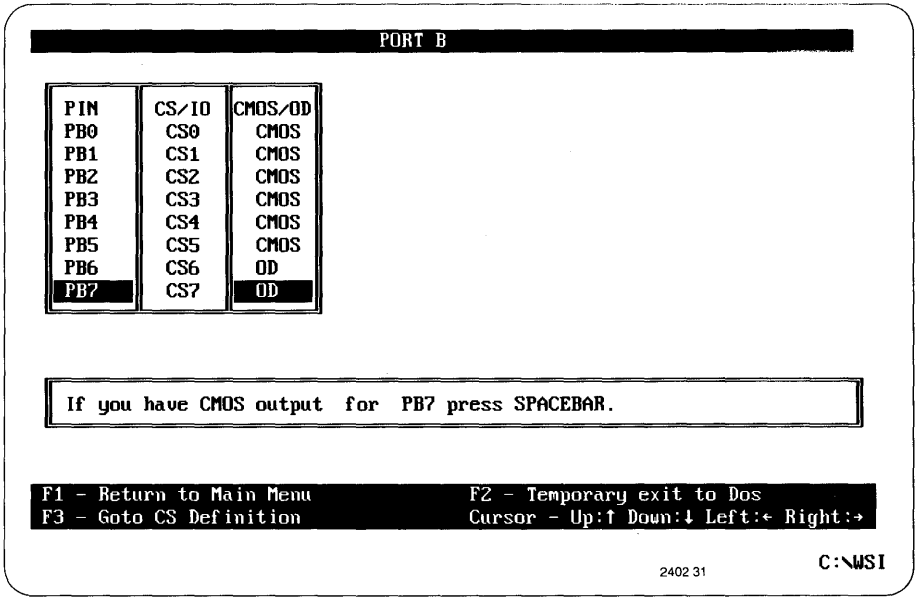
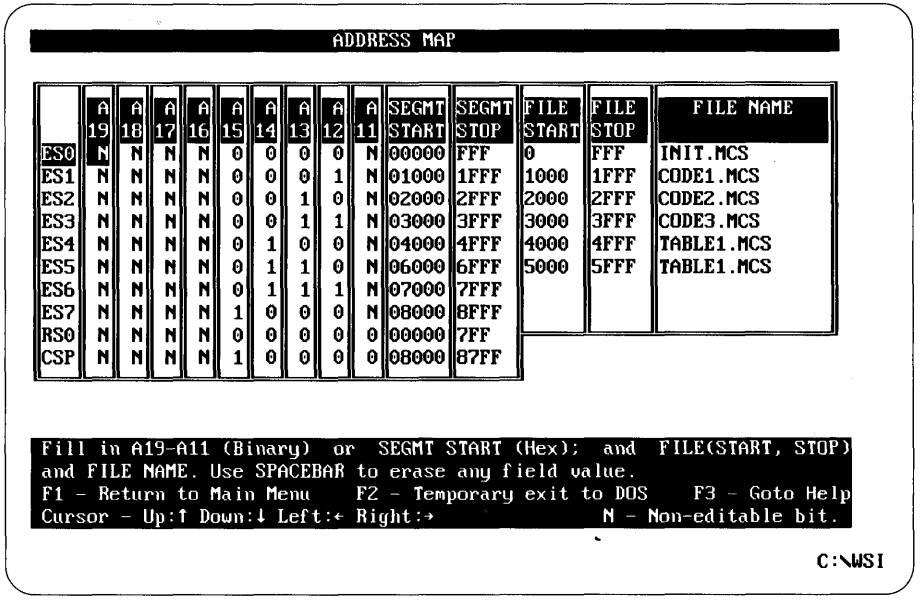


Figure 32. ADDRESS MAP Menu

Figure 32 shows the ADDRESS MAP menu. The designer can enter a binary code for the address range of the various select lines; ES0–ES7, RS0, and CSP, being the EPROM, SRAM, and PERIPHERAL assignments, respectively. A space for individual hexadecimal files is reserved under the FILENAME section. The Intel MCS files are listed as they would be compiled and programmed into the device.



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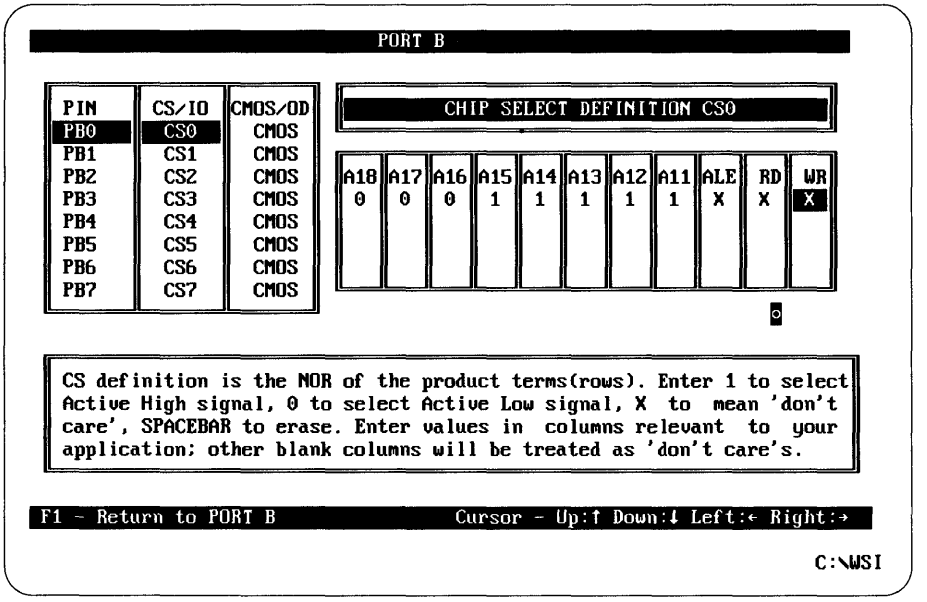
After configuration has been established, the user can return to the main menu and select the COMPILE option. The configuration is compiled and converted to a JEDEC array program map.

When successfully finished, the designer can select the MAPPRO option (see Figure 25), and when a WSI MAGICPRO™ programmer is available in the PC system, finalize the design by programming a PSD301.

The Address Map for Port B can be configured as shown in Figure 33. Per Figure 31, depress function key F3 to invoke the chip select definition. The entries can be made for logic HIGH, LOW, or "don't care" conditions.

Figure 33. Port B Configuration Menu with Address Map



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Summary

The PSD3XX microcontroller peripheral with memory, supported with low-cost software and programming capability form WSI, greatly simplifies the overall design of microcontroller based systems. The key advantage is the extensive condensing of glue logic, latches, ports, and discrete memory elements into a single-device, enhancing the reliability of the final product. Applications for the device extend to practically any area that uses microcontrollers or microprocessors, from modems and vending machines to disc controllers and high-end processor systems.

The PSD301 streamlines a microcontroller-based smart transmitter design PSD301

By Seyamak Keyghobad – Bailey Controls, and Karen Spesard – WSI

Abstract

A smart transmitter design is described which takes advantage of the integration capabilities and flexibility of WSI's PSD301 microcontroller peripheral. The following discussion illustrates how the PSD301, in effect, was responsible for eliminating an extra 2.5 inch diameter board in a system where real estate is at a premium by reducing the number of components from 12 down to 5.

Introduction

Designers of systems using microcontrollers and microprocessors often face the problem of how to integrate peripheral logic and memory functions into their designs without using many discrete chips and large areas of board space. For example, when external EPROM and SRAMs are configured into systems with ROMless microcontrollers, general I/O ports are typically sacrificed for address, data input/output, and control functions. When these I/O ports are depleted, the total chip count of the system is increased by requiring the use of additional external ports and steering logic. Designers, who have limited board space, such as found in the disk drive, modem, cellular phone, industrial/process control, and automotive industries, find this a critical problem.

The PSD301 programmable peripheral device from WSI solves this problem by integrating all SRAM, EPROM, programmable decoding and configurable I/O port functions needed in 8 or 16-bit microcontroller designs into a single-chip user-configurable solution. This is illustrated in the following industrial control application where the PSD301 eliminates seven chips and saves the designer from needing another board in the system.

The Design Application

The smart transmitter, shown in Figure 1, was developed by Bailey Controls, a manufacturer of process control instruments, to support a popular field bus protocol. One of its functions in this sensor application is to measure pressure, differential pressure, and flow rates through pipes in industrial environments such as chemical plants, oil refineries, or utility plants. A host system monitors the transmitter via a process control network.

The completed transmitter design consists of three main boards. The first board includes the power supply and communications hardware to provide power to the rest of the system and feedback to the process control network. It consists of communications transformers and line drivers/receivers.

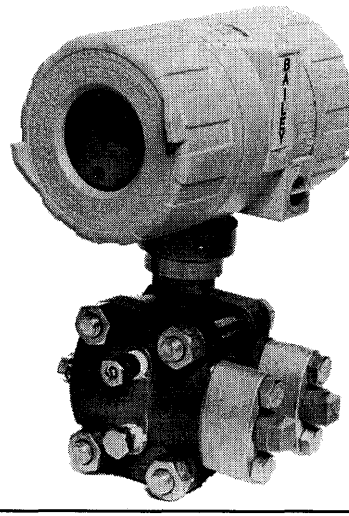
The second board is the digital microcontroller board and contains the 68HC11 microcontroller as well as the PSD301 programmable peripheral, a PLD, UART, and LCD display. Its function is to communicate and receive the inputs from the third board, process the data, and display the appropriate results to the LCD.

The third board or input board is mostly analog. It receives inputs from string gauge sensors which use a bridge circuit for measuring pressure using a diaphragm. The input board then converts the signals so the microcontroller can read them.

The PSD301 streamlines a microcontroller-based smart transmitter design

By Seyamak Keyghobad – Bailey Controls, and Karen Spesard – WSI

Figure 1. "Smart" Transmitter from Bailey Controls



▲ Pressure/Flow

Design Considerations

The smart transmitter system is rather small. Its case is only 2.5 inches in diameter and thus requires boards that fit this small form factor as shown in Figure 2. Not surprisingly, the major design consideration during development was board space. This was especially true for the microcontroller/digital board where real estate is at a very high premium.

One of the problems was that there were already requirements for the 68HC11 microcontroller, a 256K EPROM, 16K SRAM, a PLD, TTL logic, a UART, and an LCD display on the digital board. This meant extending the number of boards used beyond one unless a way could be found to integrate some of these elements.

Other important considerations, or goals actually, for the design were to reduce power consumption to less than 2.4W, improve reliability, lower design costs, and shorten the time-to-market.

To meet these objectives, Bailey Controls looked to user-configurable peripheral, the PSD301, for its integration capabilities, its flexibility, and its low power of less than 35 mA active and 90 µA typical powerdown.

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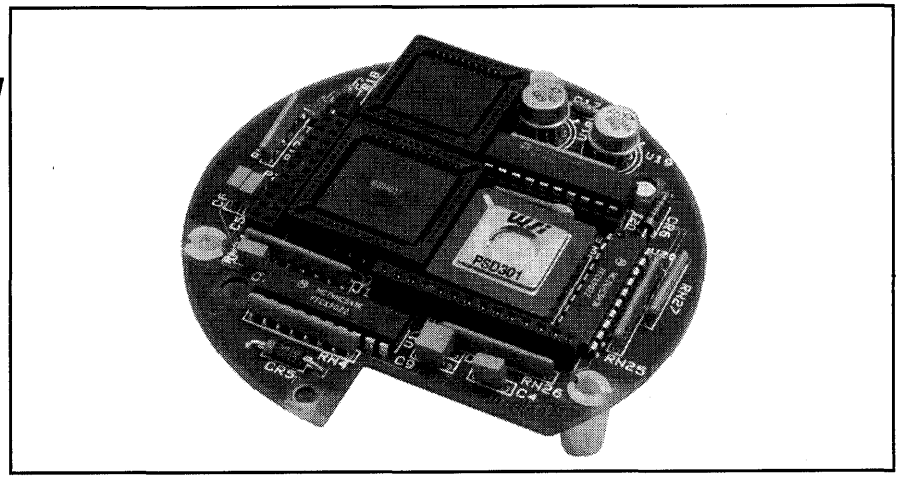
Figure 2. The Bailey Smart Transmitter Board Using the WSI PSD301.



PSD301 Architecture

The PSD301 is a field programmable device that has the ability to interface to virtually any 8- or 16-bit microcontroller without the need for external glue logic. This is possible because the PSD301 combines the elements necessary for a complete microcontroller peripheral solution, such as user-configurable logic, I/O ports, EPROM and SRAM, all into one device. The functional block diagram of the PSD301 in Figure 3 shows its main sections: the internal latches and control signals, the programmable address decoder (PAD), the memory, and the I/O ports.

The control signals and internal latches in the PSD301 were designed so interfacing to any microcontroller would be easy and require no glue logic. For instance, the PSD301 can interface directly to all multiplexed (and non-multiplexed) 8- and 16-bit microcontroller address/data buses because it has two on-chip 8-bit address latches. This means no external latches are required to interface to multiplexed buses. It also has programmable polarity on the control inputs ALE/AS and RESET, so they can be configured to be active high or active low.

The other control signals, $\overline{RD}$/E, and $\overline{WR}$/R/$\overline{W}$, are also programmable as /RD and /WR or E and R/$\overline{W}$, enabling direct interface to all Motorola- and Intel-type controllers.

The programmable array decoder (PAD) is an EPROM-based reprogrammable logic "fuse" array with 11 dedicated inputs, up to 4 general-purpose inputs, and up to 24 outputs. The PAD is used to configure the 8 EPROM blocks on 2K word boundaries and the SRAM on a 1K word boundary anywhere within a 1 Meg address space. It is also used to generate a base address for mapping ports A and B, as well as to provide mapping for the track mode. The PAD, like a traditional PLD, can generate up to eight sum-of-product outputs to extend address decoding to external peripherals or to implement logic replacement on a board.

Memory in the PSD301 is provided by EPROM for program and table storage and SRAM for scratch pad storage and development and diagnostic testing. The EPROM density is 256K bits and the SRAM density is 16K bits. Both can be operated in either word-wide or byte-wide fashion, which translates to a 32K x 8 or 16K x 16 EPROM configuration and a 2K x 8 or 1K x 16 SRAM configuration. As described above, the EPROM is divided into 8 blocks (of 4K x 8 or 2K x 16), with each block typically on a 2K boundary locatable within a 1 Meg address space.

There are 3 ports on the PSD301 that are highly flexible and programmable: Ports A, B and C, illustrated in Figure 4. Port A is an

The PSD301 streamlines a microcontroller-based smart transmitter design PSD301

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PSD301 Architecture (Cont.)

8-bit port that can be configured in a variety of ways. For example, if the PSD301 is in the multiplexed mode, port A can be configured pin-by-pin to be an I/O or a lower order latched address. Alternatively, port A can be configured in the track mode to transfer 8 bits of address and data inputs through port A. This enables the microcontroller to share external resources, such as additional SRAM, with other controllers. In either case, each port A output can be configured to be CMOS or open drain. If the PSD301 is in the non-multiplexed mode, port A becomes the lower order data for the chip.

Port B is another flexible 8-bit port. In the multiplexed mode or 8-bit non-multiplexed mode, each pin on port B can be customized to function as an I/O or a chip-select output. The chip-select signals are determined by the PAD programming and are used for general logic replacement or to extend the address decoding to external peripherals. Each pin in this mode can also be programmed to have a CMOS or an open drain output. In the 16-bit non-multiplexed mode, port B becomes the higher order data for the chip.

Port C is the third port which is available on the PSD301. It is a 3-bit port that can be programmed on a pin-by-pin basis to be chip-select outputs and/or general-purpose logic inputs or addresses to the PAD. Some uses for port C might be to extend the address range to 1 Meg, or to create finer address decoding resolution down to 256. Or, one might use port C to help create a simple state machine.

Simple Interfaces to the PSD301.

One of the overwhelming advantages of the PSD301 is its ability to interface to virtually any microcontroller without any glue logic, while providing additional I/O ports and memory. This is accomplished by configuring or programming the part to function in an operational mode geared for a specific application.

For instance, there are 45 configuration bits on the PSD301 that have to be programmed in addition to the EPROM prior to usage. These configuration bits are determined during development by the designer using the WSI MAPLE software package. After the configuration bits are determined, the EPROM code and configuration data can be merged during compilation and the part subsequently programmed.

Interfacing the PSD301 to different microcontrollers is accommodated by the configuration bits discussed above. To illustrate how this works, two examples are provided.

The first example is with the 80C196 microcontroller. This 16-bit microcontroller from Intel interfaces directly to the PSD301, providing it with additional off-chip program store EPROM and data store SRAM, as well as the flexibility that comes with three additional I/O ports. As illustrated in Figure 5, the 80C196's 16-bit multiplexed address/data bus and control signals ($\overline{RD}$,$\overline{WR}$, BHE, ALE, RESET) connect directly to the PSD301. This is achieved with the PSD301 in the following configuration:

- ❑ 16-bit data bus
- ❑ Multiplexed address/data
- ❑ $\overline{RD}$ and $\overline{WR}$ mode set
- ❑ Active HIGH ALE
- ❑ Active LOW RESET
- ❑ A16 A18 configured as output
- ❑ Combined memory mode

The other configuration options that are available, but not listed above, are application dependent and can be changed to meet the requirements of the design. For instance, on pin 43 (A19/$\overline{CSI}$), the power-down option $\overline{CSI}$ could be selected if

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Simple Interfaces to the PSD301 (Cont.)

power consumption savings is important. If it isn't and another logic input to the PAD would be helpful, A19 could be selected. And, if open-drain drivers are important on one of the ports to drive a display, for example, they also could be selected instead of CMOS drivers.

All other microcontrollers have simple interfaces to the PSD301 as well. This includes all the variations of microcontrollers in the 8-bit 68HC11 family from Motorola. For simplicity's sake, the PSD301 interface to 68HC11 versions with multiplexed address/data buses will be discussed, although the non-multiplexed versions will interface to the PSD301 in a similar manner, except in this case port A will become dedicated for 8-bit data.

Figure 6 illustrates the interconnections between the PSD301 and the 68HC11 microcontroller with multiplexed address/data buses. Again, all the address/data connections are direct, as well as the control signals (E, R/$\overline{W}$, AS, and /RESET). Because $\overline{BHE}$/$\overline{PSEN}$ is not used, this PSD301 input signal is tied HIGH.

The PSD301 must be programmed using WSI's MAPLE software package in the following modes to achieve this configuration:

- ❑ 8-bit data bus
- ❑ Multiplexed address/data
- ❑ R/$\overline{W}$ and E mode set
- ❑ Active HIGH AS (ALE)
- ❑ Active LOW RESET
- ❑ Combined memory mode

Again, other parameters on the PSD301 can be set to fit additional design requirements. These include the security bit, the port I/Os, and the PAD inputs and outputs.

The "Smart" Transmitter Design.

The microcomputer-based smart transmitter design, by Bailey Controls, requires program store 256K bits EPROM for storing algorithms and data store 16K bits SRAM for storing A/D, communication and LCD routines. It also requires two octal latches, a PLD, and a variety of glue logic to interface to its 68HC11 microcontroller, UART, and LCD display. This is illustrated in Figure 7. Of course, with board space on the digital board being limited, another board would have been needed to accommodate these components, unless they in some way could be integrated.

This is where the PSD301 provides exceptional value. As discussed, the PSD301 already integrates EPROM,[1] SRAM,[2] a PLD, and other glue logic all on one chip. It interfaces to the 68HC11 directly and actually integrates 8 chips from the alternative design into one, eliminating the need to add another board. The resultant architecture is illustrated in Figure 8.

Note that in the alternative design shown in Figure 7, ports typically lost when connecting the microcontroller to external memory had to be recreated externally with latches and buffers when memory was connected to the microcontroller. With the PSD301, these ports are recreated internally, eliminating the latches and buffers.

For example, to interface the PSD301 to the 24-character LCD display, each pin of

The PSD301 streamlines a microcontroller-based smart transmitter design

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The "Smart" Transmitter Design (Cont.)

port A is configured as an I/O and mapped to the byte-wide LCD data inputs. Then to write to or read from the LCD display, port A is accessed like a memory-mapped peripheral via an address offset from the base CSIOPORT defined in the PAD. Since port A is qualified by and handled through the PAD, there is no need for an external octal latch.

Other TTL logic is not required to interface to the 68HC11's control signals, memory, or peripherals either. It is all integrated in the PSD301. Thus, a smaller PLD than originally thought required in the design was used — a 16V8 instead of a 22V10 — because the PAD was able to reduce the amount of logic by creating chip selects for the UART and other logic functions.

Figure 3. PSD301 Architecture

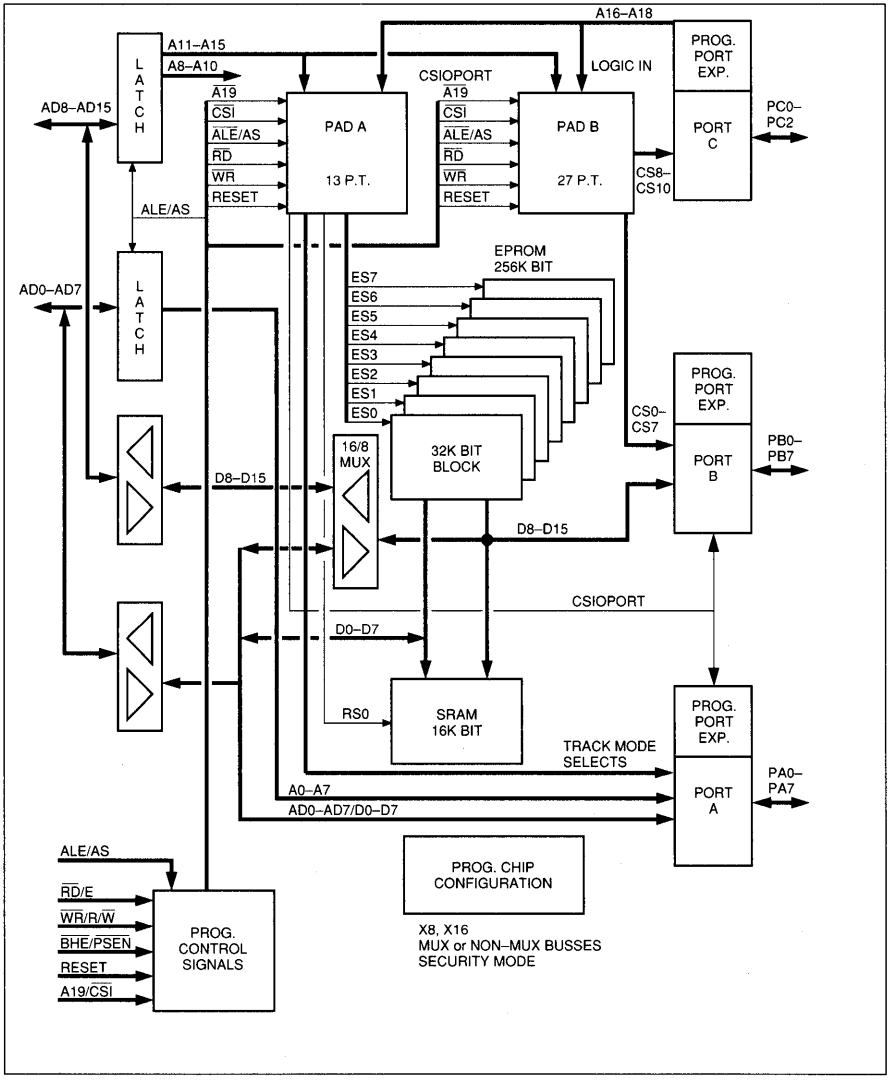

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Figure 4. PSD301 Multiplexed Address/Data Configuration

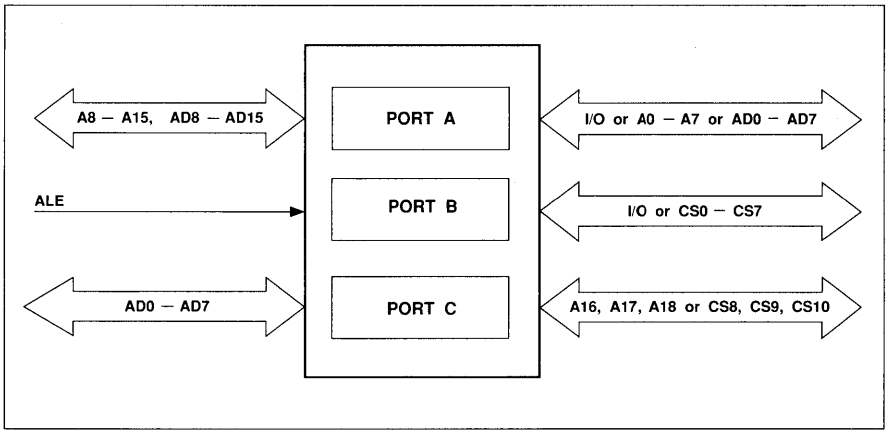


Figure 5. General Schematic Diagram of the 80C196 and PSD301.

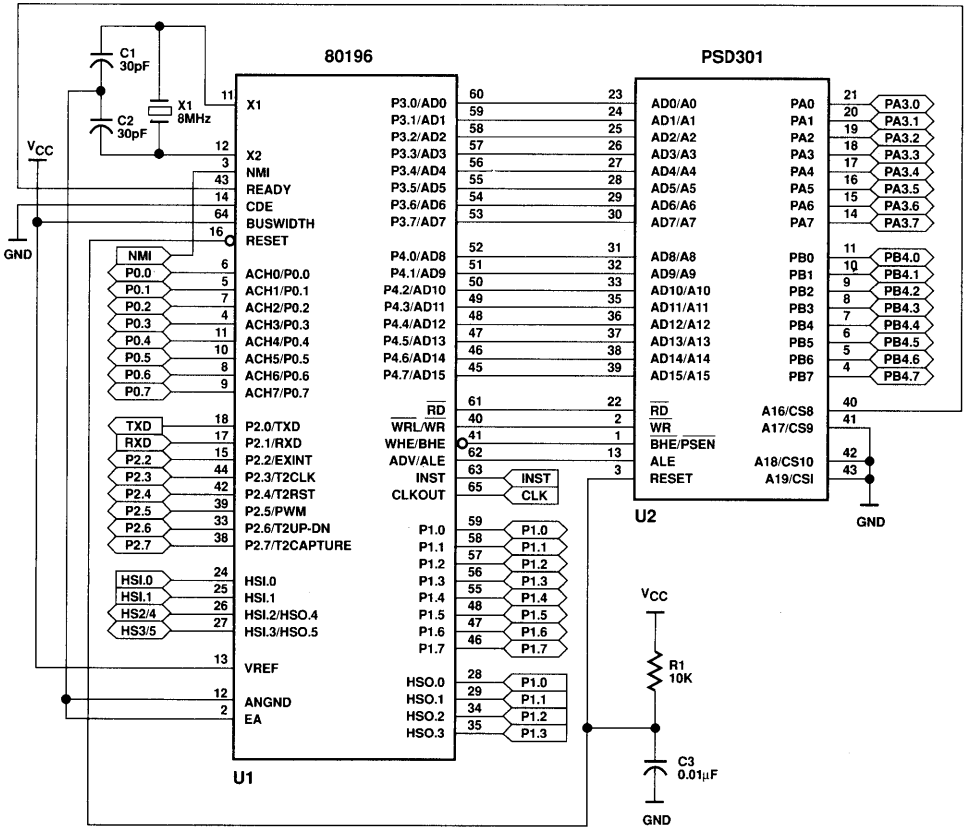
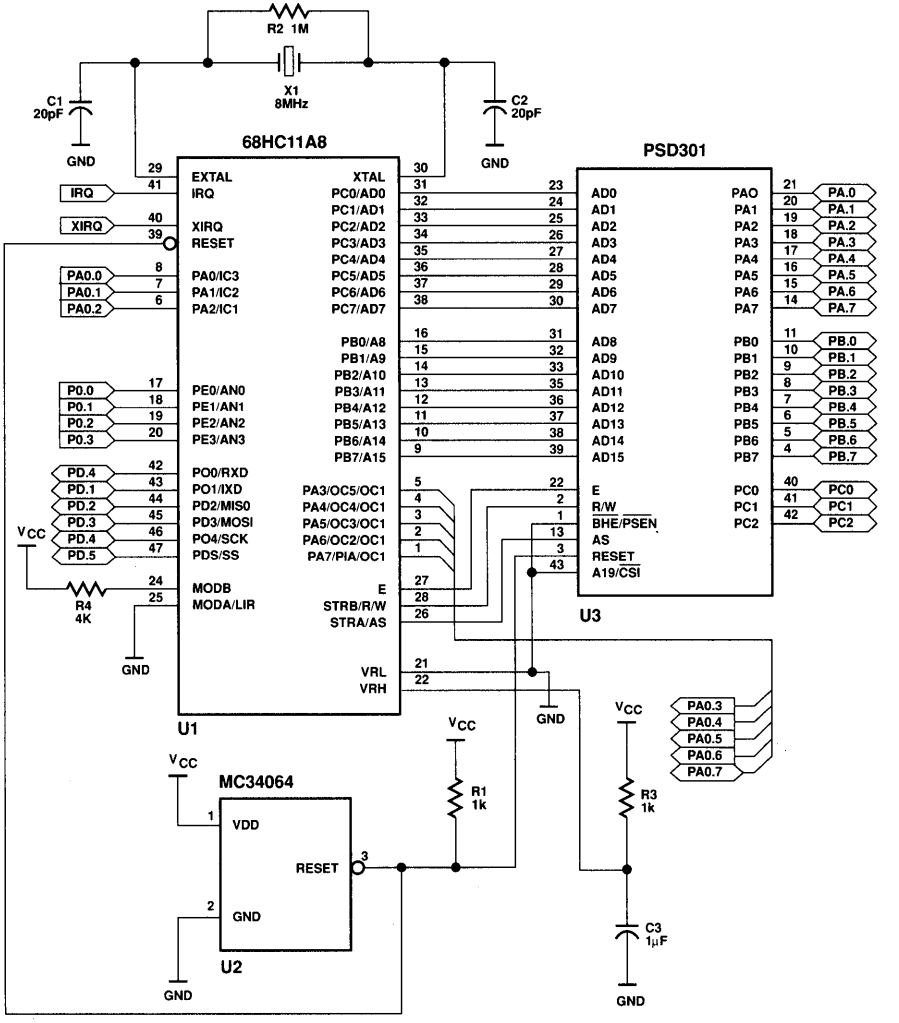


Figure 6. General Schematic Diagram of the 68HC11and PSD301.



The PSD301 streamlines a microcontroller-based smart transmitter design

By Seyamak Keyghobad – Bailey Controls, and Karen Spesard – WSI

Figure 7. Detailed Block Diagram of Bailey Control's Alternative Design Solution Without PSD301.

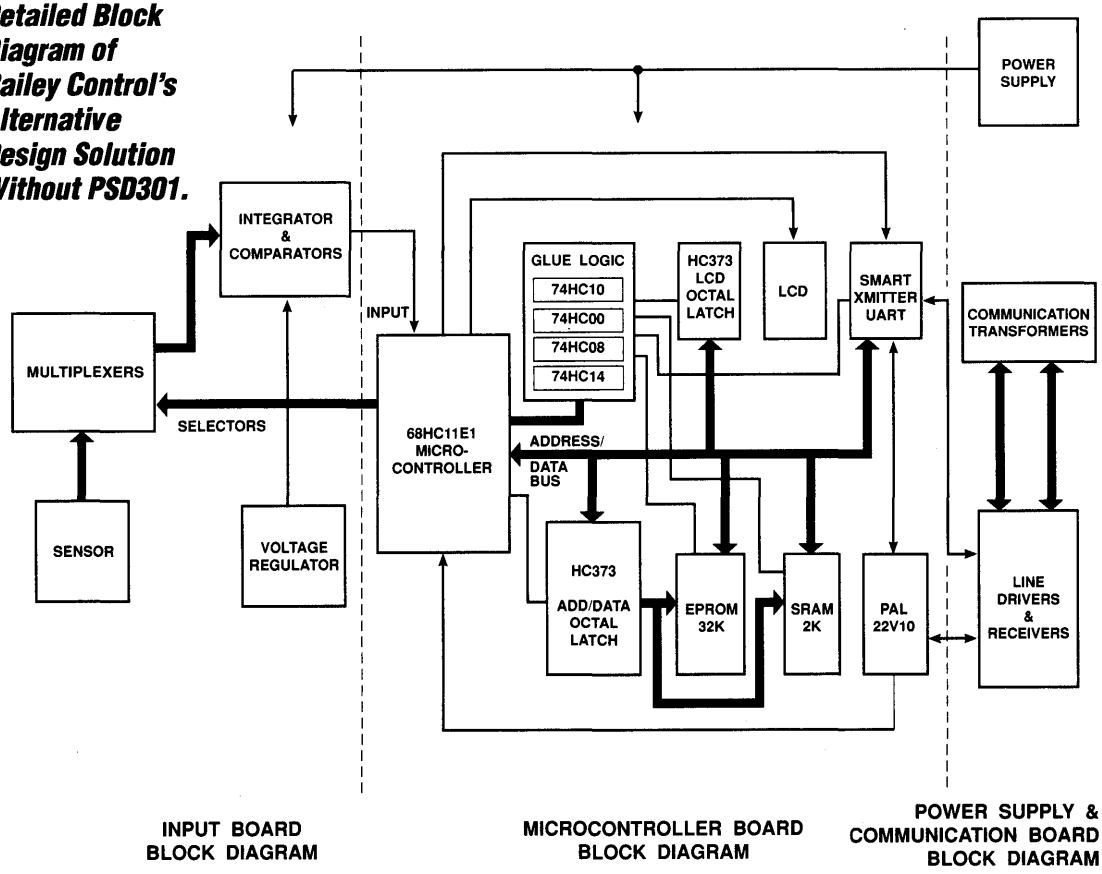


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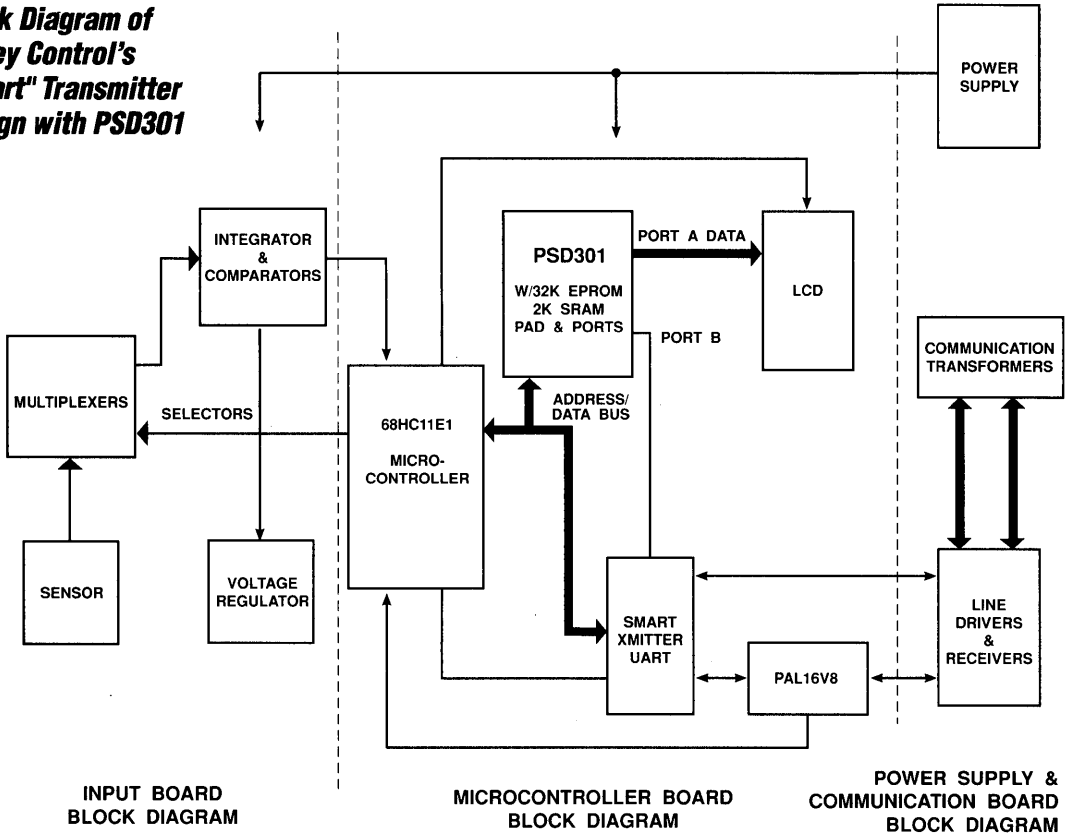
Figure 8. Block Diagram of Bailey Control's "Smart" Transmitter Design with PSD301



The PSD301 streamlines a microcontroller-based smart transmitter design

PSD301

By Seyamak Keyghobad – Bailey Controls, and Karen Spesard – WSI

PSD301 Bonuses

Besides considerably reducing board space in this smart transmitter design by reducing parts count, several other benefits of the PSD301 were also seen. These include reliability improvement, power consumption savings, inventory savings, faster time-to-market, and cost savings.

Reliability was improved because there are seven less chips required for implementation that could fail in the design. Also, by reducing chip count, 112 pins and about 100 traces were eliminated and the number of layers on the board were reduced from 8 to 4, making failures due to open or shorted pins and traces less likely to occur.

Power consumption was reduced because much faster discrete EPROM and SRAM devices with access times of ~75 ns would have been required in conjunction with glue logic for selecting different devices instead of using the PSD301, saving at least 20 mA Icc. (The access time for the PSD301 memories include decoding and input address latch delays). If the power-down feature on the PSD301 were also used, power savings could be increased further. For example, in a system which is accessing the PSD301 only a quarter of the time, the power consumption could be reduced by 75% to 8 mA typical.

As an added benefit, the PSD301 helped reduce inventory significantly by obsoleting multiple chips. And, if last minute changes in the design were required, the PSD301 would be able to accomodate them without additional hardware modifications. So, purchasing line item management is made simpler and easier.

With the reprogrammable PSD301, development time was kept to a minimum by easily accommodating design iterations in both hardware and software. Changes in I/O, address mapping, bus interface, and code were simple to make. Also, debugging was made easier with the PSD301's on-chip SRAM for down-loading test programs. This all helped to shorten the design development cycle, reduce development costs, and speed up market introduction of the smart transmitter.

By using the PSD301, cost savings were realized by reducing system cost with fewer boards (or reduced board space), improving reliability, and reducing inventory levels. Savings were also attributable to lower manufacturing costs because there were fewer parts to program and place. And by getting to market faster, profits were improved significantly.

Summary

The PSD301 peripheral solved a fundamental problem often seen in that instead of getting "locked into" an inflexible multiple chip memory sub-system solution, the PSD301 was able to provide much higher integration and flexibility all at the same time. Clearly, using the PSD301 was the better choice for the smart transmitter design.

Notes

1. If more EPROM was needed, the PSD302/312 w/512K bits EPROM and the PSD303/313 w/1024K bits EPROM are available in the same pinout and packages (please call your local WSI sales representative for availability). Or, multiple PSD301s can be cascaded together with the added benefit of increased functionality and I/O's.

2. If more SRAM is needed, it can be added externally without requiring any additional glue logic. See Application Note 011. Note that many engineers have 8K x 8 SRAM in their systems now – not because they need it, but because 2K x 8 SRAMs are not as readily available.

Appendix 1. PSD301 Configuration

```
        WSi PSD301 Configuration Save File for Smart Transmitter Design

                              ALIASES

CS0 = ASICCS
********************************************************************************
                       GLOBAL CONFIGURATION

Address/Data Mode:                                      MX
Data Bus Size:                                          8
CSI/A19:                                                CSI
Reset Polarity:                                         LO
ALE Polarity:                                           HI
WRD/RWE:                                                RWE
A16-A19 Transparent or Latched by ALE:                  T
Using different READ strobes for SRAM and EPROM:        N
********************************************************************************
                 PORT A CONFIGURATION (Address/IO)

 Bit No.      Ai/IO.      CMOS/OD.
    0          IO          CMOS
    1          IO          CMOS
    2          IO          CMOS
    3          IO          CMOS
    4          IO          CMOS
    5          IO          CMOS
    6          IO          CMOS
    7          IO          CMOS

********************************************************************************
                 PORT B CONFIGURATION

 Bit No.      CS/IO.      CMOS/OD.
    0          CS0          CMOS
    1          CS1          CMOS
    2          CS2          CMOS
    3          CS3          CMOS
    4          CS4          CMOS
    5          CS5          CMOS
    6          CS6          CMOS
    7          CS7          CMOS

           CHIP SELECT EQUATIONS

/ASICCS = /A15 * A14 * /A13 * /A12 *  E

/CS1 = /A15 * A14 * /A13 * A12 *  E

/CS2 = /A15 * A14 * A13 * /A12 *  E

/CS3 = /A15 * A14 * A13 * A12 *  E

/CS4 = /A15 * /A14 * /A13 * /A12 * /A11 *  E
   + /A15 * /A14 * /A13 * /A12 * /A11 * / R/W

/CS5 = /A15 * /A14 * /A13 * /A12 * A11 *  E
   + /A15 * /A14 * /A13 * /A12 * A11 * / R/W

/CS6 = /A15 * /A14 * /A13 * A12 * /A11 *  E
   + /A15 * /A14 * /A13 * A12 * /A11 * / R/W

/CS7 = /A15 * /A14 * /A13 * A12 * A11 *  E
   + /A15 * /A14 * /A13 * A12 * A11 * / R/W
```

Appendix 1. PSD301 Configuration (Cont.)

```
*******************************************************************************
              PORT C CONFIGURATION

 Bit No.      CS/Ai.
    0          CS8
    1          CS9
    2          CS10


          CHIP SELECT EQUATIONS

/CS8 = /A15 * /A14 * A13 * /A12 * /A11 *  R/W

/CS9 = /A15 * /A14 * A13 * /A12 * A11 *  R/W

/CS10 = /A15 * /A14 * A13 * A12 * /A11 *  R/W

*******************************************************************************
              ADDRESS  MAP

      A   A   A   A   A   A   A   A   A SEGMT  SEGMT   EPROM   EPROM   File Name
     19  18  17  16  15  14  13  12  11 STRT   STOP    START    STOP
ES0   N   N   N   N   1   0   0   0   N  8000   8FFF    8000    8fff    BCN2.0
ES1   N   N   N   N   1   0   0   1   N  9000   9FFF    9000    9fff    BCN2.0
ES2   N   N   N   N   1   0   1   0   N  A000   AFFF    a000    afff    BCN2.0
ES3   N   N   N   N   1   0   1   1   N  B000   BFFF    b000    bfff    BCN2.0
ES4   N   N   N   N   1   1   0   0   N  C000   CFFF    c000    cfff    BCN2.0
ES5   N   N   N   N   1   1   0   1   N  D000   DFFF    d000    dfff    BCN2.0
ES6   N   N   N   N   1   1   1   0   N  E000   EFFF    e000    efff    BCN2.0
ES7   N   N   N   N   1   1   1   1   N  F000   FFFF    f000    ffff    BCN2.0
RS0   N   N   N   N   0   1   1   0   0  6000   67FF
CSP   N   N   N   N   0   0   1   1   0  3000   37FF


*******************************  END  ****************************************
CDATA        = 0                          CPAF1 [0] = 0
CADDRDAT     = 1                          CPAF1 [1] = 0
CRRWR        = 1                          CPAF1 [2] = 0
CA19/(/CSI)  = 0                          CPAF1 [3] = 0
CALE         = 0                          CPAF1 [4] = 0
CRESET       = 0                          CPAF1 [5] = 0
COMB/SEP     = 0                          CPAF1 [6] = 0
CADDHLT      = 0                          CPAF1 [7] = 0

CPAF2        = 0

CPACOD [0] = 0                            CPBCOD [0] = 0
CPACOD [1] = 0                            CPBCOD [1] = 0
CPACOD [2] = 0                            CPBCOD [2] = 0
CPACOD [3] = 0                            CPBCOD [3] = 0
CPACOD [4] = 0                            CPBCOD [4] = 0
CPACOD [5] = 0                            CPBCOD [5] = 0
CPACOD [6] = 0                            CPBCOD [6] = 0
CPACOD [7] = 0                            CPBCOD [7] = 0

CPBF [0] = 0                              CPCF [0] = 1
CPBF [1] = 0                              CPCF [1] = 1
CPBF [2] = 0                              CPCF [2] = 1
CPBF [3] = 0
CPBF [4] = 0
CPBF [5] = 0
CPBF [6] = 0
CPBF [7] = 0
```

Using the PSD3XX PAD for system logic

PSD3XX

By Jeff Miller – WSI

Introduction

In 1990, WSI introduced the Programmable System Device (PSD): the first device in the world integrating UVEPROM, SRAM and programmable logic on a single chip of silicon. The highly-successful PSD301 was the first device in the PSD family and is currently used in applications ranging from fluid analyzers to high performance computers. The PSD device, by combining most of the peripheral functionality required by a typical microcontroller unit into one package, has enabled designers to greatly reduce part count, power and board space which has translated into significant cost savings.

Even if the PSD3XX family were simply a collection of EPROM and SRAM with an on-chip decoder, it would be capable of adding significant value to the system into which it were designed. However, the PSD3XX family is much more than just a combination of memory devices. The on-chip PLD may be used for many useful purposes in addition to providing the address decode capability. The purpose of this note is to demonstrate, in detail, the full capability of the PAD section of the PSD3XX family. A basic, though not extensive, knowledge of the PSD 3XX family and the Maple programming software is assumed by this note. Please consult Application Note 011 and/or the appropriate PSD3XX family data sheet for this general knowledge.

PAD Architectue

The Programmable Array Decoder (PAD) contained in the PSD3XX family is a standard PLD array designed to provide all of the internal memory and I/O device chip selects as well as an external logic replacement capability. It has 14 inputs, 24 outputs and 40 product terms with which to perform these functions. See Figure 1 for an illustration of the PAD.

The PAD's 14 inputs are as follows:

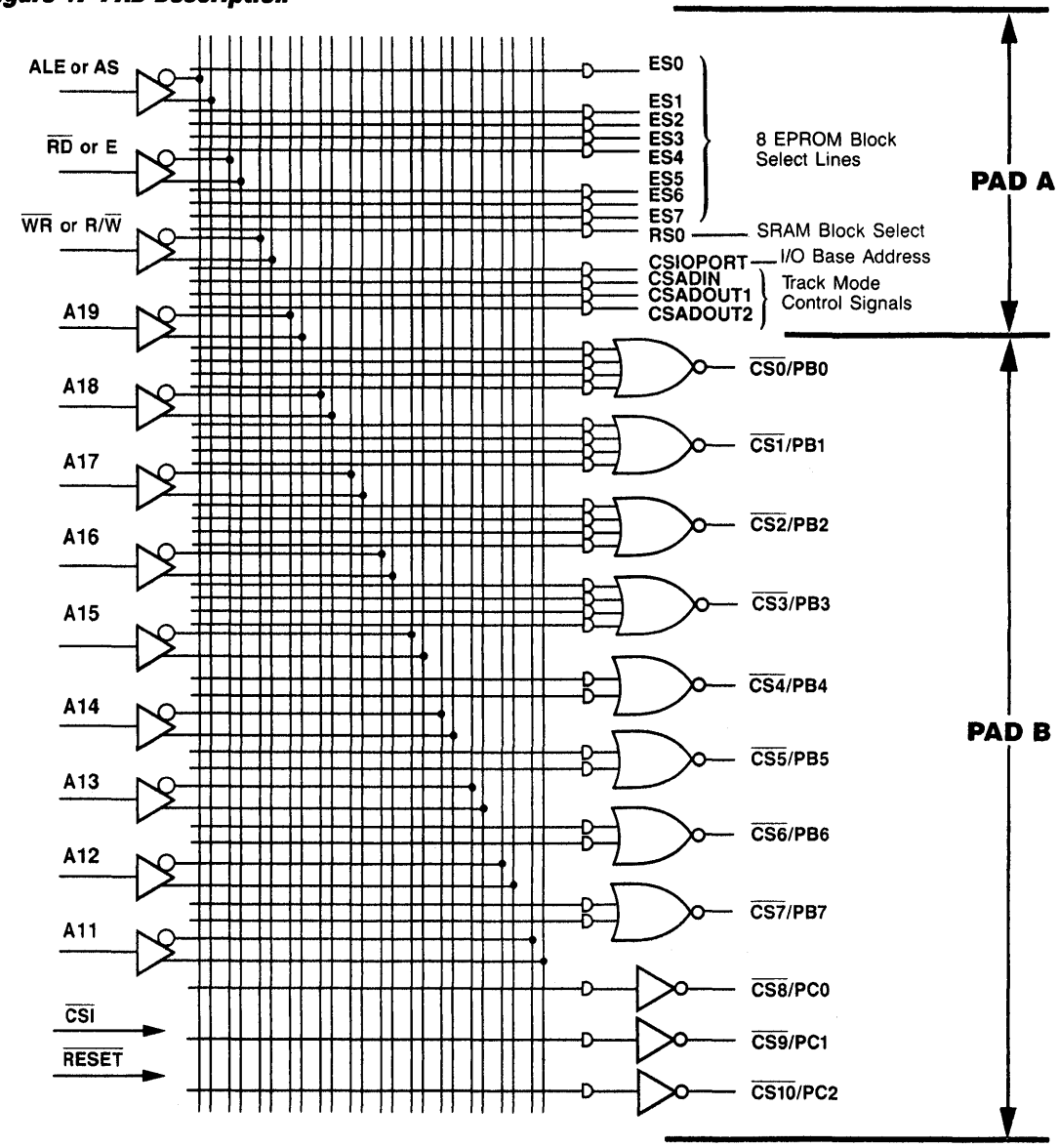
- A11 – A19
- ALE or AS
- $\overline{RD}$ or E
- $\overline{WR}$ or R/$\overline{W}$

The A11 – A19 pins are labeled as address inputs, however, they do not have to be. A11 - A15 are generally sourced by the microcontroller or microprocessor that is connected to the PSD device. If the controller generates more than 16 bits of address, the A16 – A19 inputs may be used to connect the high order address bits for a full 1 MByte of address space. If the controller does not require this much address space, A16 – A19 may be used for other purposes, like general I/O or logic inputs.

A19 is multiplexed with the $\overline{CSI}$ signal, which is used to place the PSD device in a low power mode when the system requires it. When configured as $\overline{CSI}$, the A19 pin may not be used for any other purpose except the power down mode. In this mode, the $\overline{CSI}$ signal is used by the PAD only to disable it, causing it to expend less power. When configured as A19, this signal may be used as a general purpose input to the PAD from the external system. This capability will be described in more detail later in this note. A16 – A18, when not necessary for address expansion, may also be used as general purpose inputs to the PAD. Thus, a total of four of the 14 PAD inputs may be general purpose, allowing the replacement of external logic by the PSD device. These inputs may be combined with the other PAD inputs to form complex equations involving addresses, strobes and external signals.

When attempting to visualize the full capability of the PAD outputs, it is most clear when it is broken into two sections, labeled in Figure 1 as PAD A and PAD B. PAD A is responsible for providing all of the internal chip selects for the EPROM, SRAM and I/O ports and the track mode control signals, and PAD B is responsible for the external logic replacement function.

Figure 1. PAD Description



PAD A

Thirteen of the 24 PAD outputs and thirteen of the 40 product terms are dedicated to PAD A. PAD A should be considered the internal address decoder, used to select the various on-chip memories and I/O devices according to the memory map programmed by the user. Each output has a single product term, allowing a particular resource to be allocated a single contiguous range of addresses which will be used to access it. All of the PAD inputs are available for generation of the PAD A outputs, allowing the designer to select internal resources using any combination of address, strobe and external signals.

PAD A (Cont.)

The PAD A outputs are as follows:

- ES0 – ES7
- RS0
- CSIOPORT
- CSADIN
- CSADOUT1
- CSADOUT2

ES0 – ES7 are used to select the internal EPROM resources. Using the PSD301 as an example, there are eight select lines with which to access 32 KBytes of EPROM. Thus, each select line can enable a block of 4 KBytes of EPROM configured as 4K x 8 or 2K x 16. Each block must be contiguous, but the blocks may be placed anywhere within the address space of the microcontroller.

RS0 is used to select the SRAM resource. This single signal accesses a single 2 KByte block of SRAM which may be configured as 2K x 8 or 1K x 16. Again, this block must be contiguous but may be placed anywhere in the address map.

CSIOPORT is the signal which defines the base address of the on-chip I/O ports and control registers. The I/O ports and control registers occupy a 2K block of addresses which, like the memories, must be contiguous but may be located anywhere in the address space of the microcontroller. Once configured in the address map, CSIOPORT defines the base address of these ports and registers. An offset is added to the base address to individually access the registers. Table 1 below lists the offset values for these registers.

CSADIN, CSADOUT1 and CSADOUT2 are used to control the Track Mode operation. The Track Mode is an available option for Port A to allow it to "track" the Address/Data bus inputs to the PSD device from the microcontroller. This provides the capability to connect the PSD device, and therefore the microcontroller, to one or more shared resources. These resources may be memory or other devices which must be accessed by more than one microprocessor or microcontroller.

CSADIN is generated when the microcontroller is attempting to read data from Port A in the track mode. It is generated from one product term involving the address inputs and the $\overline{RD}$ strobe (Intel mode) or R/$\overline{W}$ and E (Motorola mode). This allows the user to configure the address range in which the data is to be read from Port A. CSADOUT1 is generated when the microprocessor is accessing a "tracked" address. It is generated from a single product term involving the address inputs and ALE. When the address generated by the microcontroller is within the block specified by the user for track mode, and the ALE is active, CSADOUT1 becomes active, transferring the address and outputting it from Port A. CSADOUT2 is generated when the microcontroller is performing a write operation to a tracked address. It also has one product term involving the address inputs and $\overline{WR}$ (Intel mode) or R/$\overline{W}$ and E (Motorola mode). When the microcontroller performs a write to the appropriate address, CSADOUT2 is generated, transferring the data and outputting it from Port A. For further details on the operation of the Track Mode, please consult Application Note 017.

Table 1. I/O Port Offset Addresses

Register Name	Byte Size Access of the I/O Port Registers Offset from the CSIOPORT
Pin Register of Port A	+ 2 (accessible during read operation only)
Direction Register of Port A	+ 4
Data Register of Port A	+ 6
Pin Register of Port B	+ 3 (accessible during read operation only)
Direction Register of Port B	+ 5
Data Register of Port B	+ 7

Example: Address Mapping With PAD A

In this example, we will choose a sample address map which is similar to those used in typical microcontroller applications. This example assumes the use of a PSD301 device with 256 Kbits of EPROM and 16 Kbits of SRAM. Figure 2 below illustrates our sample address map.

In this example, we have located the boot code and interrupt service routines beginning at address 0000 in EPROM block 0. The SRAM is located in the 2K block beginning at address 0x1000 and can be used for the stack and/or other scratchpad data. The I/O ports occupy the 2K block beginning at address 0x1800. Addresses in this range will access ports A and B and their control registers. The area from 0x2000 to 0x8FFF is unused in this example, though it could be used for external resources as will be shown later. Finally, the main program resides in the 28K block of EPROM located from address 0x9000 to 0xFFFF and is selected by ES1 – ES7.

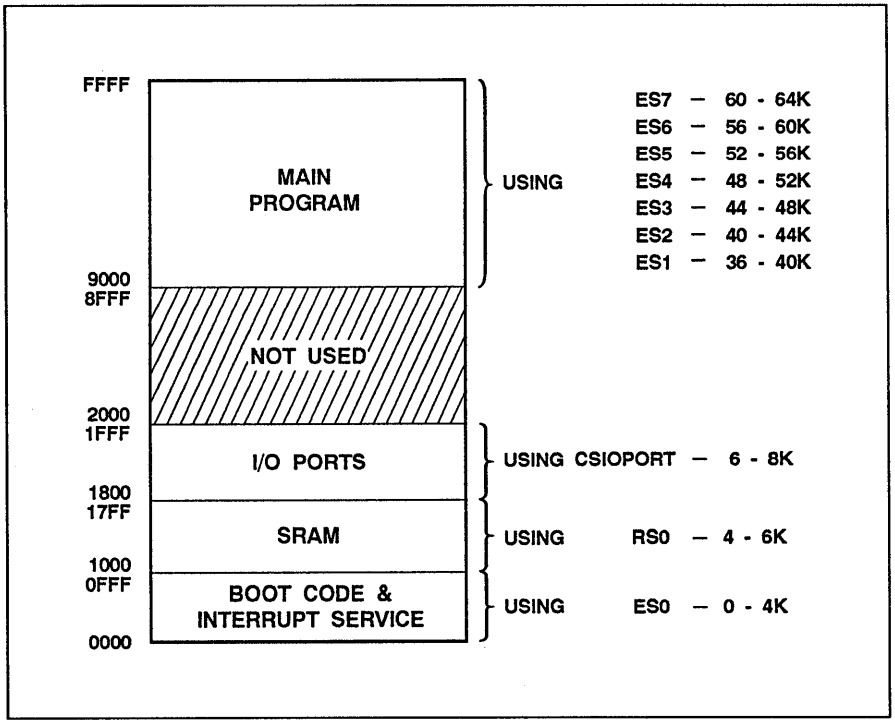
Configuring this memory map would normally require designing a decoder to generate the appropriate chip selects for each given address range. For example, assuming that a microcontroller with a 16-bit address bus is used, the chip select for EPROM bank 0 (ES0) would be generated with the following equation:

$$ES0 = /A12 \cdot /A13 \cdot /A14 \cdot /A15$$

Equations like this one would be formulated for each of the chip selects, and the entire function would probably be placed in some kind of programmable device. When the PSD device is used, PAD A replaces this programmable device. Programming PAD A to perform this function is a simple task using WSI's Maple software.

Entering the ADDRESS MAP menu in the Maple software running on a PC compatible computer, the user will see a screen similar to the one shown in Figure 3.

Figure 2. Example Memory Map



Example: Address Mapping With Pad A (Cont.)

Upon displaying this screen, the Maple software is ready for the user to enter the memory map data. This is performed quite simply by moving the cursor to the appropriate point with the arrow keys, and then entering the appropriate data. The address mapping may be entered in either of two ways. First, the user may select each address bit individually for each chip select and enter a 0 or 1 as appropriate for the equation desired. In our example, for ES0 we would enter a 0 in the columns for A12, A13, A14 and A15. The other bits are don't cares. In the other method of programming the pad, the user simply moves the cursor to the SEGMT START column and enters the desired starting address for the block. Again, using our sample memory map, the user would move to the SEGMT START column for ES0 and enter 0000. Maple then automatically programs the 0's and 1's into the address bits correctly to program a 4K block of EPROM beginning at address 0x0000. Note that all EPROM blocks must begin on 4K boundaries. Figure 3 shows the resulting address map table for our example.

The address inputs which were unused in this example (A16, A17, A18 and A19) could have been used as general purpose inputs to the PAD for specialized control of the on-chip memory and I/O resources. When this is done, the designer has complete flexibility as to the configuration of the PSD device resources and may easily absorb many system functions into the PSD device. More detail about the use of A16 – A19 will be provided later in this note.

PAD B

Eleven of the PAD outputs and 27 of the product terms are dedicated to PAD B. Where PAD A was used to control the on-chip PSD device resources, PAD B controls any off-chip resources required by the system. As with PAD A, all inputs to the PAD are available to PAD B, allowing the system designer to formulate outputs involving any combination of address, strobes and external signals. Unlike PAD A, several of the outputs of PAD B have up to four product terms each.

The outputs of PAD B are as follows:

- CS0 – 7 (Port B)
- CS8 – 10 (Port C)

The outputs from PAD B are brought to the outside world through Port B and Port C. These outputs are called chip selects, though they may be used for any function whatsoever. The port pins are configured as selected by the user when the device is programmed with the Maple output file. There are many configuration options for each port pin.

Figure 3. Maple Address Map Entry

ADDRESS MAP

	A 19	A 18	A 17	A 16	A 15	A 14	A 13	A 12	A 11	SEGMT START	SEGMT STOP	FILE START	FILE STOP	FILE NAME
ES0	X	X	X	X	0	0	0	0	N	0000	0FFF			
ES1	X	X	X	X	0	0	0	1	N	9000	9FFF			
ES2	X	X	X	X	1	0	1	0	N	A000	AFFF			
ES3	X	X	X	X	1	0	1	1	N	B000	BFFF			
ES4	X	X	X	X	1	1	0	0	N	C000	CFFF			
ES5	X	X	X	X	1	1	0	1	N	D000	DFFF			
ES6	X	X	X	X	1	1	1	0	N	E000	EFFF			
ES7	X	X	X	X	1	1	1	1	N	F000	FFFF			
RS0	X	X	X	X	0	0	0	1	0	1000	17FF			
CSP	X	X	X	X	0	0	0	1	1	1800	1FFF			

ALIASES:
Fill in A19 – A11 (Binary) or SEGMT START (Hex): and FILE (START, STOP) and FILE NAME, Use SPACEBAR to erase any field value.
F1 – Return to Main Menu F2 – Temporary Exit to DOS F3 – Go to Help
Cursor – UP: ↑ Down: ↓ Left Col: ← Right Col: → Right – F4 Left – F5

PAD B (Cont.)

If you require more information about port configuration, please consult application note 011. If the port outputs are configured as chip selects (outputs from the PAD), they may not be used for any other purpose. For example, the three Port C signals may be configured as chip selects (outputs) or addresses (inputs) but cannot be both. Fortunately, the flexibility of the PSD device and the Maple software allows the designer to configure each Port B and C pin individually, so that the number of outputs and inputs may be optimized for a particular design requirement. See Table 2 below for an example of this flexibility.

This sample port configuration demonstrates all of the possible uses of a particular port pin. Though only Ports B and C may be inputs or outputs to/from the PAD, Port A is included in the table for completeness. In this example, five of the port pins are configured as PAD outputs (CS) and two are configured as PAD inputs (A). The remaining port pins in this example are configured as either I/O or address outputs. Several of the CS outputs have been configured as open drain. This allows them to be connected together in a wired OR configuration to increase the number of product terms even further if desired.

Table 2. Sample Port Configuration

Pin	Configuration	CMOS/OD
PA0	Address Out	CMOS
PA1	Address Out	CMOS
PA2	Address Out	CMOS
PA3	Address Out	CMOS
PA4	I/O	CMOS
PA5	I/O	OD
PA6	I/O	OD
PA7	I/O	CMOS
PB0	$\overline{CS0}$	CMOS
PB1	$\overline{CS1}$	CMOS
PB2	$\overline{CS2}$	OD
PB3	$\overline{CS3}$	OD
PB4	I/O	CMOS
PB5	I/O	CMOS
PB6	I/O	CMOS
PB7	I/O	CMOS
PC0	A16	—
PC1	A17	—
PC2	$\overline{CS10}$	OD

Example: Generating a Logic Equation With PAD B

Assume that it is necessary to generate the following equation given the port configuration in Table 2 above. This equation is a simple OR of three product terms.

CS0 = A15 • A14 • /A13 • /A17 • RD
+ /A15 • A14 • A12 • WR + A16

Figure 4 illustrates the Maple programming sequence to generate this equation.

To program this equation, the PORT B menu is entered from the Maple software. CS0 is selected by moving the cursor to it using the arrow keys. With CS0 selected, the user then presses the F3 key to bring up the CHIP SELECT DEFINITION table for CS0. The table contains four rows for data entry, each one corresponding to one of the available product terms for CS0. Implementing this equation required using three of the four available product terms. The fourth is left blank and will not be used to generate the output.

To enter the equation into the table, simply move the cursor around into the appropriate position and enter a 1 if the corresponding signal should be high for the equation to be true, 0 if it should be low, and X or SPACE if the signal is a don't care. The first term of the equation requires a low on A17, a high on A15, a high on A14, a low on A13 and a high on RD for the term to become active. Thus, 1's are placed in the A15, A14 and RD positions,

Example: Generating a Logic Equation With PAD B (Cont.)

and 0's are placed in the A17 and A13 positions. The remaining terms in the equation are entered in the same way. Note that A17 and A16 in this example need not be address bits, but may instead be used to bring external signals into the PAD.

Four product terms are available on each of the CS0 – CS3 outputs, two terms are available on the CS4 – CS7 outputs and one term is available on CS8 – CS10. When planning the use of the PAD outputs, it is important to consider this so that the most efficient use of the product terms can be achieved.

Figure 4. Programming PAD Outputs

PORT B

PIN	CS/I/O	CMOS/OD
PB0	CS0	CMOS
PB1	CS1	CMOS
PB2	CS2	CMOS
PB3	CS3	CMOS
PB4	CS4	CMOS
PB5	CS5	CMOS
PB6	CS6	CMOS
PB7	CS7	CMOS

CHIP SELECT DEFINITION CS0

A19	A18	A17	A16	A15	A14	A13	A12	A11	ALE	RD	WR
X	X	0	X	1	1	0	X	X	X	1	X
X	X	X	X	0	1	X	1	X	X	X	1
X	X	X	1	X	X	X	X	X	X	X	X

ALIASES:

CS definition is the NOR of the product terms (rows). Enter 1 to select Active High signal, 0 to select Active Low signal, X to mean "don't care", SPACEBAR to erase. Enter values in columns relevant to your application; other blank columns will be treated as "don't cares".

F1 – Return to PORT B Cursor – Up: ↑ Down: ↓ Left: ← Right: →

Application Examples

The following section will illustrate the use of the PAD for system logic replacement in some common microcontroller applications.

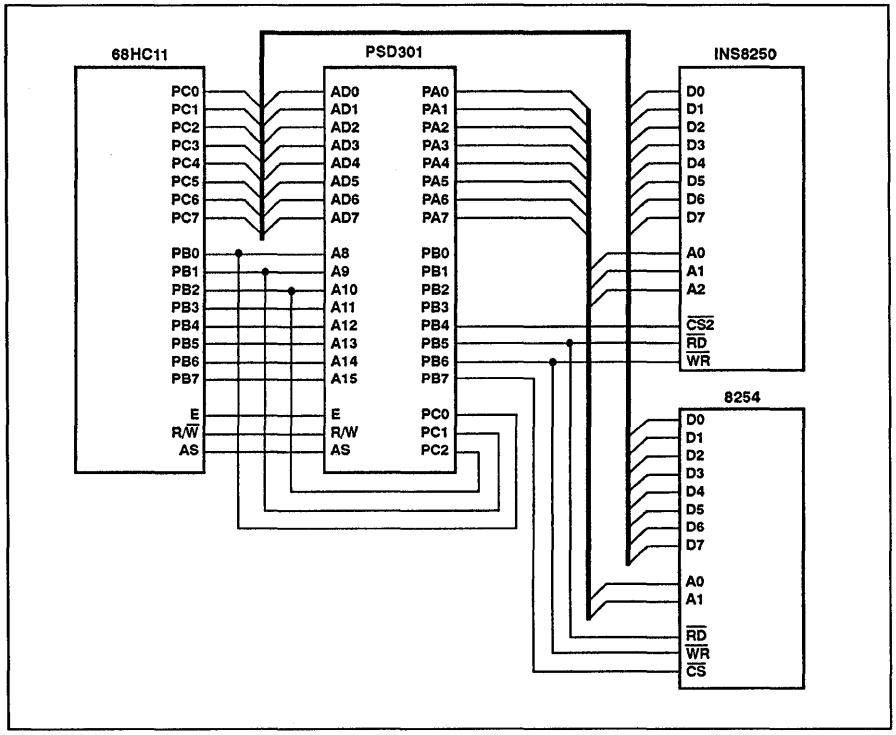
Basic Chip Select Generation

One of the simplest uses of PAD B is the generation of chip selects for off-chip resources such as I/O devices or memories. Figure 5 below depicts the connection between a 68HC11 microcontroller, the PSD301 and two common peripheral devices: the 8250 UART and the 8254 counter/timer.

The 68HC11 is an 8-bit microcontroller with a 16-bit address bus. The lower 8 bits of address are multiplexed with the data bus while the upper 8 bits are transmitted on their own bus. An address strobe (AS) is provided to latch the address off of the multiplexed bus. A R/$\overline{W}$ signal indicates whether the current bus transaction is a read or a write (R/$\overline{W}$ = 1 = read, R/$\overline{W}$ = 0 = write). The E signal is the clock used to strobe the data in or out of the microcontroller. The PSD301 can be configured to exactly match this signal definition and then connected as shown in the diagram. Not all of the 68HC11 or PSD301 signals are shown, only those relevant to this example of PAD capability.

The 8250 is a UART device commonly used in microcontroller systems to provide a serial data communication port. It has a simple bus interface, yet does not directly connect with the 68HC11 bus architecture. It requires an 8-bit bus to transfer data to and from the microcontroller and a separate 3-bit address bus used to access its internal registers. It also requires a chip select and separate read and write strobes ($\overline{RD}$ and $\overline{WR}$). The chip select is generated by decoding the address from the microcontroller. The $\overline{RD}$ and $\overline{WR}$ signals may be generated from the R/$\overline{W}$ and E signals

Figure 5. A Typical Microcontroller System



Application Examples (Cont.)

according to the following equations:

$$/RD = /(R/\overline{W} \bullet E)$$

$$/WR = /(/R/\overline{W} \bullet E)$$

These equations may be easily generated using PAD B and sent out through two of the chip select outputs. We have chosen CS5 and CS6, which come out on PB5 and PB6, for this example.

In order to provide the address lines to the 8250, we have configured Port A to output the latched address. This eliminates the need for any external latches to demultiplex the address/data bus from the microcontroller. Though all eight of the Port A pins have been configured as address outputs in this example, it is possible to configure only those address bits required for the application, A0 – A2 in this example, and configure the remaining Port A pins as general I/O.

The 8254 is a programmable interval timer which, like the 8250, is a peripheral used in many microcontroller applications. Its bus connection is very similar to the 8250, allowing it to use the same read and write strobes ($\overline{RD}$ and $\overline{WR}$) and address lines. It also requires a chip select which is decoded from the microcontroller address.

The chip selects for both of the peripheral devices may be easily decoded from the address inputs to PAD B. Normally, the addresses which are inputs to the PAD (A11 – A19) would give decoding resolution down to 2K. This means that each of the two peripheral devices that require chip selects would be allocated an address range of at least 2K. Since these devices do not require this much space and the 68HC11 has only a 16-bit address bus, it is possible to use the high order address inputs of the PSD device to improve the decoding resolution. To achieve this goal, we have configured Port C as address inputs A16 – A18, but have connected them to A8 – A10 from the microcontroller. This means that the PAD will now have

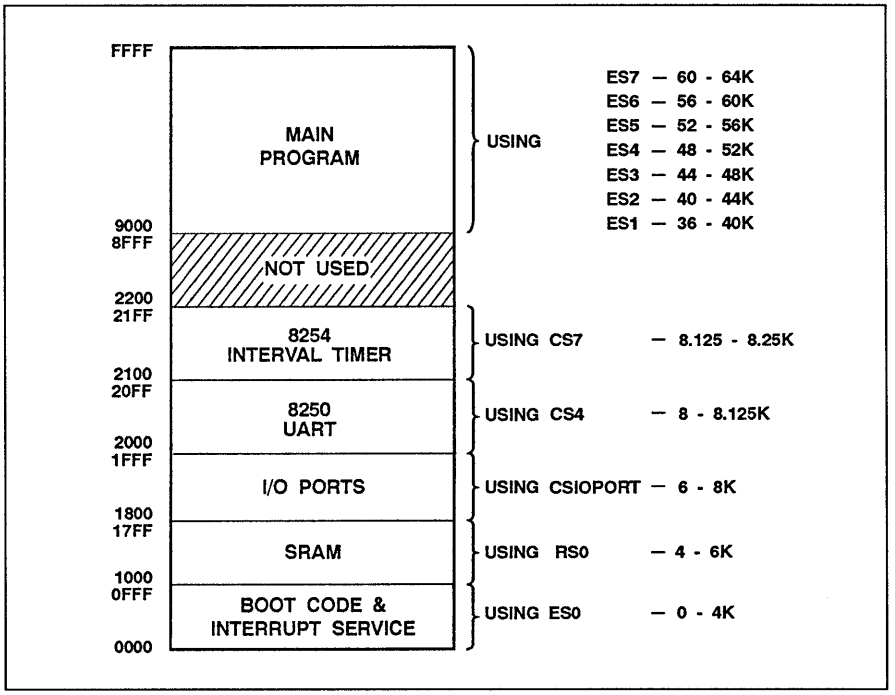
Application Examples (Cont.)

access to A8 – A15 for decoding, thus providing a resolution of 256 instead of 2K. This could actually be further reduced to a resolution of 128 if we were to configure the A19/CSI input to be A19, and then connect it to A7 from the microcontroller. In this example, we have not done this so that CSI is still available to place the PSD301 into low power mode if required.

We now have to define the addresses of each of the peripherals so that the chip select equations may be defined. We will start from the memory map provided earlier in Figure 2. This map allocated all of the internal resources of the PSD device. The external peripherals may be easily added to the unused area between addresses 0x2000 and 0x8FFF. Figure 6 depicts the new map with the external devices added. Notice that the internal resources can keep their original address mapping even though the additional address inputs (A8 – A10) have been added. This is because these inputs may be don't cares in the decoding for the internal resources even when they are being used for the external resources.

Now, to wrap up this simple design, we must enter the configuration and mapping information into Maple. The configuration of the PSD device must be consistent with the operation of the 68HC11 microcontroller. The address/data mode must be multiplexed, the data bus must be 8 bits wide, CSI/A19 may be configured either way, the reset polarity should be active low, the ALE polarity is active high, the read and write lines must be R/$\overline{W}$ and E, A19 – A16 should be latched so that these bits become available just like the rest of the address bus, and the read strobes for the

Figure 6. Memory Map With Peripherals



Application Examples (Cont.)

SRAM and EPROM will be the same. This configuration should be entered from the configuration menu of the Maple software.

The address map programming for this example will remain the same as the one used earlier in Figure 3. The only items remaining are the programming of the ports and the generation of the equations for the chip selects and read/write strobes. First we must configure Port A to provide the latched address to the peripherals. This is accomplished by entering the PORT A menu in the Maple software. Maple will then ask you if you would like Port A configured for address I/IO or the Track Mode. For this example, we will use the address/I/O configuration. Next, Port A must be configured pin for pin as an address output. This is easily performed by using the cursor keys to select the appropriate pin and pressing the SPACE BAR to change the configuration. It is also possible to configure each pin as an open drain or CMOS output, but for address outputs, it is better to make them CMOS.

Now, PORT C must be configured to provide the three additional address inputs. This is performed by entering the PORT C menu in Maple and selecting the appropriate pin with the cursor. Each pin should be configured as an address bit (Ai). Maple will call the pins A16 – A18 even though we will be using them as A8 – A10.

Lastly, we must configure the Port B outputs to become the chip selects and read/write strobes. First, the PORT B menu must be entered. Now, we must configure each pin as an I/O or CS output.
PB0 – PB3 may be configured as general purpose I/O pins. PB4 – PB7 must be configured as chip selects. Once configured as chip selects, the equations for each output may be entered by following the Maple instructions. The procedure is the same as the one used in the earlier chip select example. Our equations, including the ones developed earlier for the read and write strobes, are defined for each output as follows:

PB5 = /CS5 = /RD = /(R/W • $\overline{E}$)

PB6 = /CS6 = /WR = /(/R/W • $\overline{E}$)

PB4 = /CS4 = /8250CS = /(A15 • /A14 • A13 • /A12 • /A11 • /A18 • /A17 • /A16)

PB7 = /CS7 = /8254CS = /(A15 • /A14 • A13 • /A12 • /A11 • /A18 • /A17 • A16)

This completes the design integrating these four components with no additional logic whatsoever. There is also additional space in the PAD for more functions if necessary, so we have not yet reached the limit of the integration possibilities with the PSD301.

Wait State Generation

Often, when using some of the newer high-performance microcontrollers with slower external peripherals, it is not possible to complete a read or write cycle to the peripheral in the time allowed by the microcontroller's minimum bus cycle. In this case, one or more wait states must be added to slow the controller down to the speed of the peripheral. One way of doing this is to fix a number of wait states for all bus cycles to allow the slowest device enough time for its access. Some controllers even provide the capability to do this internally through the programming of a register. This works, of course, but can severely impact the performance of the system. There is no need to penalize the performance of the entire system, which can include zero wait state memory devices and other peripherals, simply because one or more of the external devices requires some number of wait states. It is possible, with minimal logic, to create a completely programmable automatic wait state generator using the PSD301 which will allow the fast resources to operate at zero wait states and still provide from one to eight wait states for the slower resources.

For this example, we will use an Intel 80C196KB microcontroller running at 12 MHz. This controller has the capability to operate in a 16-bit data mode, providing the opportunity to further increase performance if the system can also operate in this mode. The PSD301 does have the capability of operating in the 16-bit mode, making it a good match for the 80C196. We will assume that the 80C196 must be

Wait State Generation (Cont.)

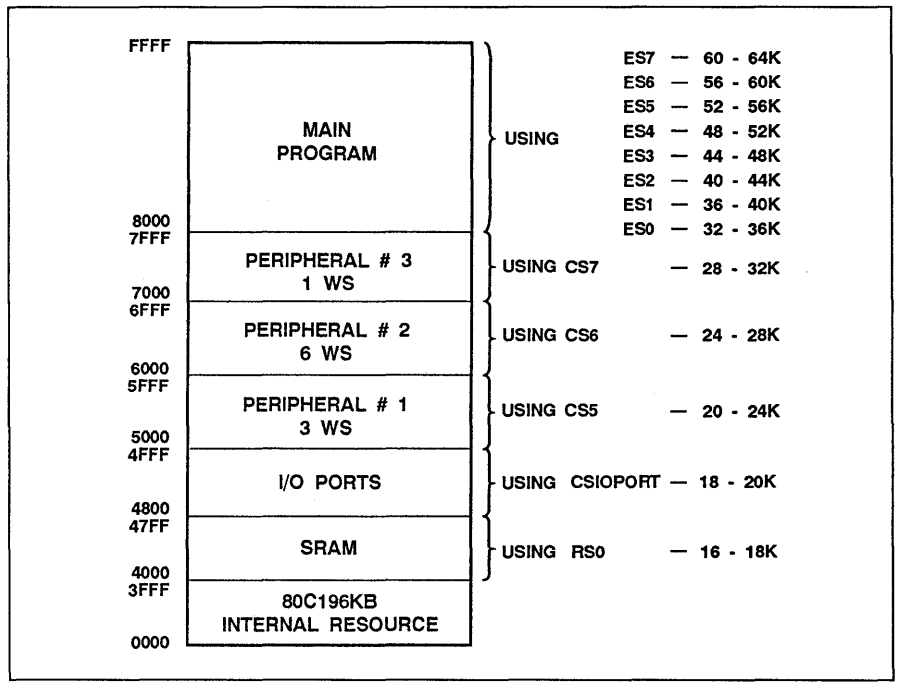
interfaced to several slow 8-bit peripherals requiring from one to eight wait states. With the PSD301, we can provide the correct number of wait states for each peripheral with the added capability of dynamically sizing the bus to the appropriate width for the current access.

The memory map we will use for this design is depicted in Figure 7. The internal resources of some 80C196 derivatives occupy most of the address space from 0x0000 to 0x3FFF, though some have less resources. Therefore, we have constructed the memory map to place the PSD device resources above address 0x4000. The PSD301 SRAM and I/O devices occupy from address 0x4000 to 0x4FFF. This leaves the area from 0x5000 to 0x7FFF for external peripherals while leaving 0x8000 to 0xFFFF for the EPROM banks. We assume that we must connect three external peripherals to the PSD device using this address space, one requiring one wait state, one requiring three and one requiring six. This memory map is entered into the part similarly to the previous examples.

To achieve the variable number of wait states, the ideal solution is to decode the address to determine the number of wait states required for a particular address range, and then to use a counter to count the appropriate number. By using the PAD to initialize an external counter, a variable wait state counter can be created in this manner. This wait state generator requires only one external device, a 74FCT191 counter. The circuit used to implement this function is illustrated in Figure 8. The 80C196KB is directly connected to the PSD device which in turn provides the three chip select signals for the external peripherals ($\overline{PER1CS}$, $\overline{PER2CS}$ and $\overline{PER3CS}$) as well as the wait state generator function and the dynamic bus sizing. Ports B and C are fully utilized to provide the logic inputs and outputs required to implement these functions, while Port A is still available for general I/O or address use.

This circuit uses PAD B to decode the addresses driven by the microcontroller and provide four outputs, based on these

Figure 7. Memory Map



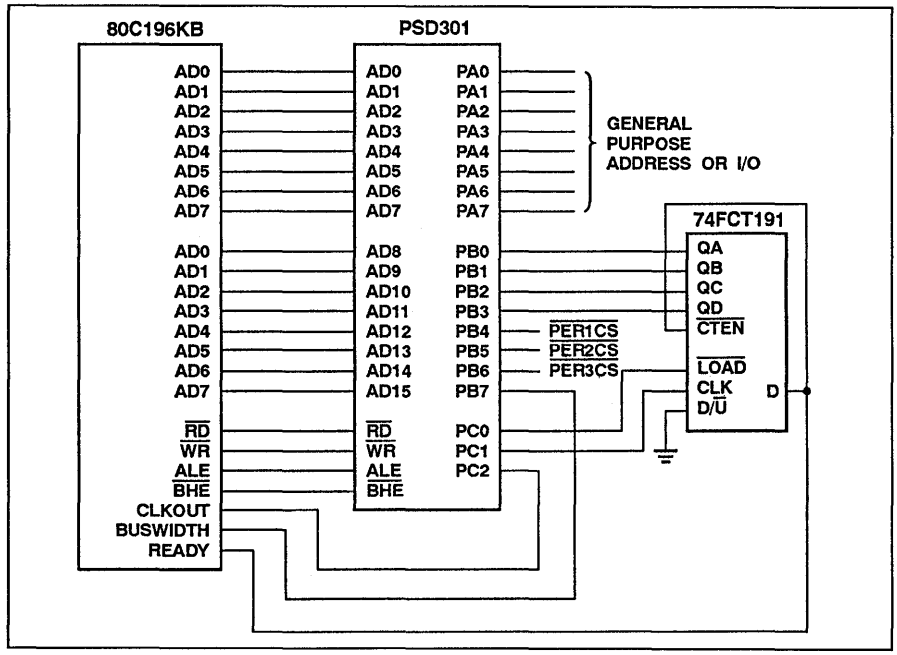
Wait State Generation (Cont.)

addresses, which are used to initialize the 74FCT191 counter with its initial value. The counter is initialized using ALE to latch these four PAD outputs. The load signal for the counter is active low, however, while ALE is active high, so ALE is inverted using PAD B and sent out through Port C. Though the 80C196KB can be configured to provide an active-low address strobe, $\overline{ADV}$, the timing of the signal is inappropriate for use as the $\overline{LOAD}$ input to the counter. Once the counter is initialized, it counts up from the initial value until the most significant bit increments from 0 to 1. The output of the most significant counter bit is routed to the READY input of the microcontroller. Thus, the controller will be held in wait states until the most significant counter bit is incremented. This output is also routed to the $\overline{CTEN}$ signal of the counter so that counting will cease once the READY signal has been issued to the controller. The clock for the counter is an inverted version of the CLKOUT signal from the controller. This clock must be inverted since the 80C196KB uses the falling edge of the clock to sample the READY input. PAD B again provides the inversion function by routing CLKOUT into one of the Port C pins, inverting it and routing it back out through another Port C pin.

The counter provides from zero to eight wait states depending on the initialized value. For zero wait states, the most significant counter bit is initialized to a "1", which provides the READY signal to the controller immediately and disables the counter from incrementing. If one wait state is desired, the counter is loaded with the value 7 (0111 binary) so that after it increments once, the most significant bit switches to a "1" and provides the READY to the controller. When two wait states are required, a 6 (0110 binary) is loaded into the counter, and so on for the rest of the wait state values.

To properly size the bus to the appropriate width, PAD B is again used to decode the addresses of the 8-bit devices. When the address of an 8-bit device is encountered, the BUSWIDTH signal is driven to configure the 80C196KB address to eight bits. For all other addresses, the width is

Figure 8. Wait State Generation Circuit



Wait State Generation (Cont.)

set for 16 bits. The BUSWIDTH signal is output from one of the Port B pins.

The PSD device must now be configured to provide the functions required by the example circuit. The configuration of the PSD must first be programmed to function with the 80C196KB. This is easily performed by the Maple software as in the previous example. The address/data mode should be multiplexed, the data bus width should be 16 bits, CSI/A19 may be configured as required for the application, the reset polarity should be active low, the ALE polarity should be active high, separate RD and WR strobes should be used and A19 – A16 should be transparent, not latched, since they are used as logic inputs to the PAD.

Next, we must program the functionality of Port C. For this example, PC0 and PC1 are used as outputs from the PAD to provide the LOAD and CLK signals for the '191 counter. This is performed by entering the PORT C menu in Maple and configuring PC0 and PC1 as CS8 and CS9, respectively. PC2 is used to input the CLKOUT signal from the microcontroller to the PAD so that it may be inverted. Therefore, it must be configured as address input A18. Now, the equations used to generate the PC0 and PC1 outputs must be entered into the PAD. PC0 is the LOAD signal which is just the ALE input inverted. PC1 is an inverted version of A18, which contains the CLKOUT signal. These equations are listed below:

PC0 = /LOAD = /ALE

PC1 = /CLKOUT = /A18

The equations are programmed by entering the CHIP SELECT DEFINITION menu for each of the two chip selects, as in the previous example, and entering the appropriate 1's, 0's and DON'T CARES. In the case of PC0, there are don't cares in all of the PAD inputs except ALE, where there is a 0. Similarly, for PC1, the A18 input is a 0 while the rest of the PAD inputs are don't cares.

Port A is usually configured next, and in this example it is free to be configured in any mode necessary for the application. It may become either I/O or address outputs, or may be set in the Track Mode as described earlier.

We are now ready to configure Port B. This example requires that all of the Port B pins be used as chip selects (logic outputs) from PAD B. PB0 – PB3 are used to initialize the counter with the correct number of wait states for each device. These outputs are defined according to the address ranges for each of the peripherals and the number of wait states required for each. Table 3 summarizes the outputs required for each peripheral so that we may define the correct equations for the outputs.

Table 3. Wait State Summary

Peripheral No.	Address Range	No. Wait States	PB0–PB3
1	0x5000-5FFF	3	1010
2	0x6000-6FFF	6	0100
3	0x7000-7FFF	1	1110

Wait State Generation (Cont.)

This table can be easily used to form the necessary equations for PB0 – PB3. PB3 can be considered the enable for the wait state generator which is active low only in the address ranges of the three peripherals. It must remain high for all other address ranges. The other three outputs simply encode the proper number of wait states. The resulting equations are listed below:

PB0 = /QA = /(A15 • A14 • A13 • /A12)

PB1 = /QB = /(A15 • A14 • /A13 • A12)

PB2 = /QC = /(A15 • A14 • A13 • /A12)

PB3 = /QD = /(A15 • A14 • /A13 • A12 + /A15 • A14 • A13 • /A12 + /A15 • A14 • A13 • A12)

PB4 – PB6 are used as chip selects for each of the three peripherals and are simply decoded from the address inputs by PAD B corresponding to the address ranges listed in Table 2. These equations are listed below:

PB4 = /PER1CS = /(A15 • A14 • /A13 • A12)

PB5 = /PER2CS = /(A15 • A14 • A13 • /A12)

PB6 = /PER3CS = /(A15 • A14 • A13 • A12)

Finally, PB7 is used to perform the bus sizing function. It should be sized to eight bits whenever any of the external peripherals is accessed. It should be sized to 16 bits for all other accesses. The 80C196KB requires a high on the BUSWIDTH input for 16-bit operation and a low for 8-bit operation. This is accomplished by the equation below:

PB7 = BUSWIDTH = /(A15 • A14 • A13 + /A15 • A14 • /A13 • A12)

This completes the equations for Port B. These equations are entered in the Maple software by selecting the Port B chip select definition screens as described in the previous example and entering 1's and 0's in the appropriate locations. Remember that don't cares (X's or blanks) must be entered in all inputs which are not used by a particular equation.

Finally, we must enter the memory map into Maple Address Map screen. This is performed as in the previous example by entering 1's, 0's or don't cares in the appropriate places.

Conclusion

The PSD device may be used in a variety of applications requiring the simplicity, space savings and performance possible by the integration of memory and programmable elements. But a significant portion of the value of the PSD device, is its ability to absorb much of the logic functionality which normally surrounds a microcontroller application. The programmability of the device allows the designer to make changes to both the software and the design itself as required. This is not possible with masked ROM or ASIC-based designs. The PSD device can truly turn a microcontroller into a complete two-chip solution.

Using memory paging with the PSD3XX

PSD3XX

By Jeff Miller – WSI

Introduction

The PSD3XX is a compact, high performance microcontroller peripheral used to extend the capabilities of a microcontroller in a space-limited embedded control system. It provides the programmable logic, memory and I/O requirements needed by most microcontroller designs in a single small package.

The PSD301, introduced in November 1990, was the first of a six-member family of devices providing varying amounts of on-chip resources. The PSD301 contains 32K Bytes of EPROM for program storage and 2K Bytes of SRAM scratchpad memory. As the family expanded, the EPROM memory size grew to 128K Bytes in some versions. This large memory may be needed in many applications requiring large feature sets. In many cases the microcontroller is capable of addressing only 64K Bytes of memory with its limited 16-bit address bus. In these applications, the designer is often faced with the difficult choice of eliminating features, using a more expensive microcontroller with a wider address bus, or adding external paging logic requiring several extra components.

With this in mind, designers at WSI have included a simple but very effective paging system in the PSD3XX models containing more than 32K Bytes of EPROM. This enables cost effective microcontrollers like the 80C31, 80196, Z80, 68HC11 and others to take full advantage of additional memory without any additional hardware or design effort.

What is Paging?

The primary purpose of a page register is to extend the width of the address bus by a number of bits to increase the size of the address space. These bits are added to the address bus as outputs of a register which is loaded from the data bus of the MCU. Each additional bit doubles the effective address space. Though the page register address bits increase address space, they are not the same as the true address bits which are generated by the microcontroller since they do not appear with the same timing or sequence of the address. They must be controlled carefully to avoid unexpected behavior. They can also be a problem for compiler-generated code since the compiler does not inherently know how to use a page register. Because of this, the designer must take care in designing software which uses the PSD3XX page register.

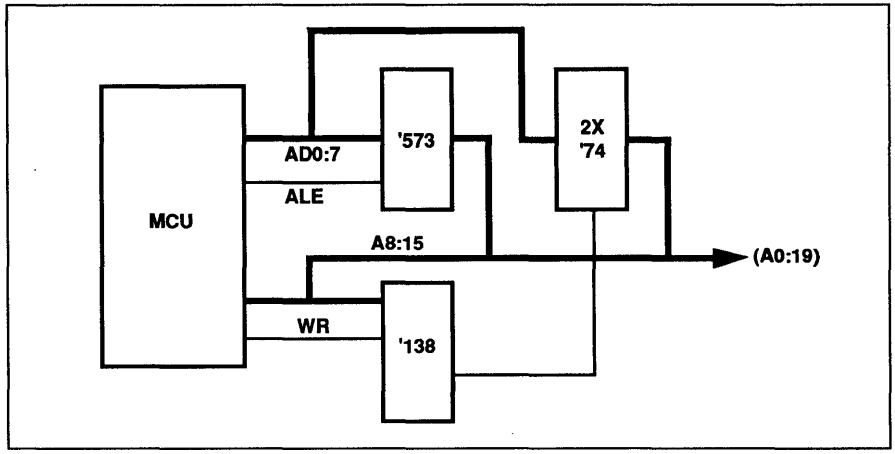
The purpose of this note is to explain the usage of the page register and some of the techniques which may be used when designing software which uses the page register. A typical page register design is shown in Figure 1. In the figure, a typical 8-bit microcontroller with a multiplexed address/data bus is shown connected with the logic required to implement a 4-bit page register. The least significant address bits are demultiplexed from the data bus by the '573 transparant latch, which is clocked by the ALE signal. The most significant 8-bits of address are driven directly by the microcontroller. When combined with the least significant address bits from the address latch, the address bus is 16-bits wide. This provides the capability to directly access 64K Bytes of address space, which may be any combination of program and data storage. To implement more address space, two '74 devices (a dual D-type flip flop) have been used to create a page register. The inputs of the '74 are four bits of the address/data bus. These bits are stored into the '74 when a write to a specific address, as decoded by the '138, is performed by the microcontroller. The outputs of the '74 form an additional 4 address bits, thus extending the address bus to 20-bits or 1 MByte of address space. The '74 page register can be considered to hold a page number. Each page number provides a complete duplication of the microcontroller's memory space. To get to another 64K Byte page of address space,

What is Paging (Cont.)

the controller simply has to change the page number by writing a different value to the page register.

The circuit below has one major complication. If the microcontroller is currently in a particular memory page, page X, and it changes the page number to Y using a store instruction which it fetched from page X, as soon as the store is complete the next instruction fetched will come from page Y. This means that page Y must pick up the programming sequence exactly as it was left off from page X. This is a complication that must be handled in software and can make programming very difficult. Additionally, interrupts can be a significant problem since they must force the program to an interrupt vector which may exist on a different page.

Figure 1. Discrete Page Register

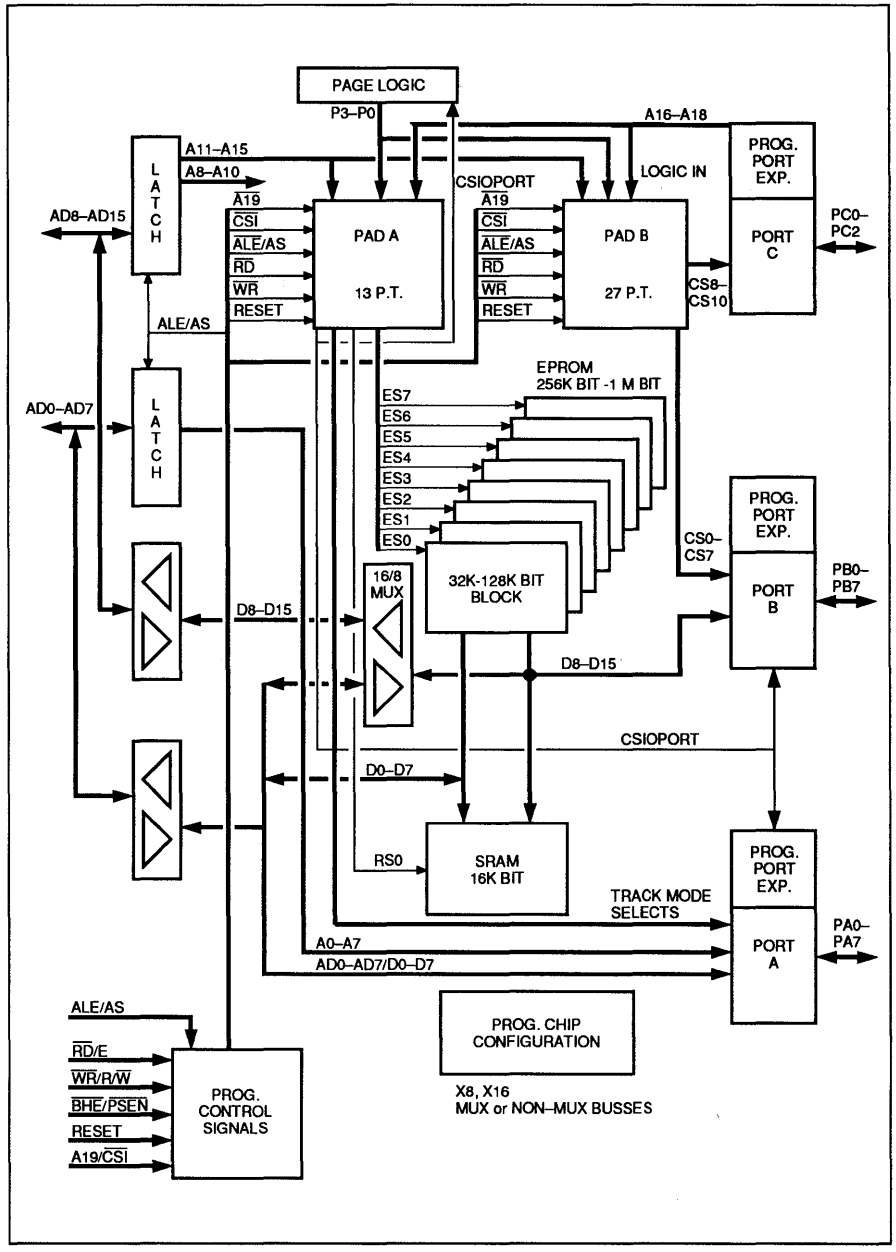


The PSD3XX Implementation

Figure 2 illustrates the block diagram of the PSD3XX with the internal page register. It is similar to the discrete circuit above, but with some important differences. The page register provides 4-bits of additional addressing capability, but does not provide them directly to the memory devices themselves. Instead, the page register output bits are taken into the Programmable Array Decoder of the PSD3XX. This enables the user to program them as necessary for the system design.

The PAD provides a flexibility that most page register implementations are not capable of providing. If you are unfamiliar with the capabilities of the PSD3XX PAD, please consult Application Note 014, *Using the PSD3XX PAD for System Logic Replacement*. Figure 3 illustrates the PAD logic in a PSD3XX with a page register. The PAD generates the outputs which are used to select the PSD3XX's eight EPROM blocks, the SRAM block, the I/O ports, the shared resource interface, the page register itself and all external functions which use the chip selects provided by Port B and Port C of the PSD3XX. Thus, the page register bits may be combined with the address bits and control signals in any combination to generate the select signals for all of the above resources. In addition, any or all of the page register bits may be don't cares in any or all of the PAD chip select equations, enabling the user to select which resources may be selcted from which page, or to select some resources from any page. This extremely useful feature enables the programmer to avoid the problem of software continuity between pages described above by making at least one of the EPROM blocks appear in all pages and then using that block to contain code for interrupt servicing and page switching. This is performed simply by making the page register bits 'don't cares' in the chip select equation for that block. All of this is fully programmable with the PSD3XX, enabling the designer to choose the paging scheme that is best for the application.

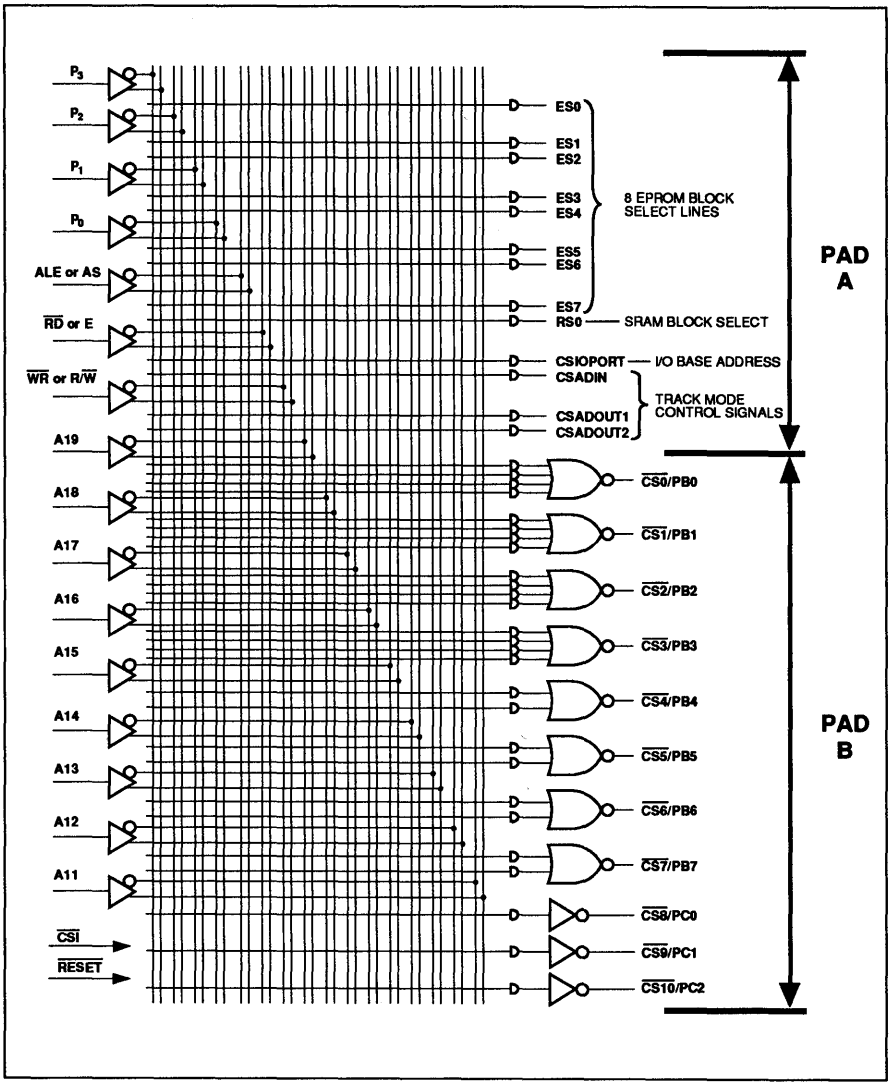
Figure 2. PSD3XX Architecture



The PSD3XX Implementation (Cont.)

The Microcontroller can write or read the page register to place a new page number in it or read the current page number. To perform this, the microcontroller must simply access the address programmed in the PAD for the page register. This address is based on the CSIOPORT select signal programming. If address 8000 hex is programmed for CSIOPORT, the corresponding page register address is 8018 hex and read and write data will be to and from the page register.

Figure 3. PSD3XX PAD Diagram



A Simple Paging Example

To illustrate the operation of the PSD3XX page register, assume that a designer requires a full 128K Bytes of program storage space, 32K Bytes of buffer SRAM and three peripheral devices which also must be memory mapped. We can also assume that the required program is easily broken into four modules which are somewhat independent, but do need the capability to call one another and must be able to pass global data among one another. Further, assume that the external peripheral devices may be selected from three of the four modules, but must not be accessed from the fourth for security reasons. Lastly, assume that the designer is constrained by cost and compatibility considerations to use an 8-bit microcontroller with a 16-bit address bus (in this example, an 8031).

These requirements may be easily implemented using the PSD313 device. The PSD313 is an 8-bit device with 128K Bytes of EPROM for program storage. It also contains the PAD and page register logic described above. The memory map required for this application is shown in Figure 4.

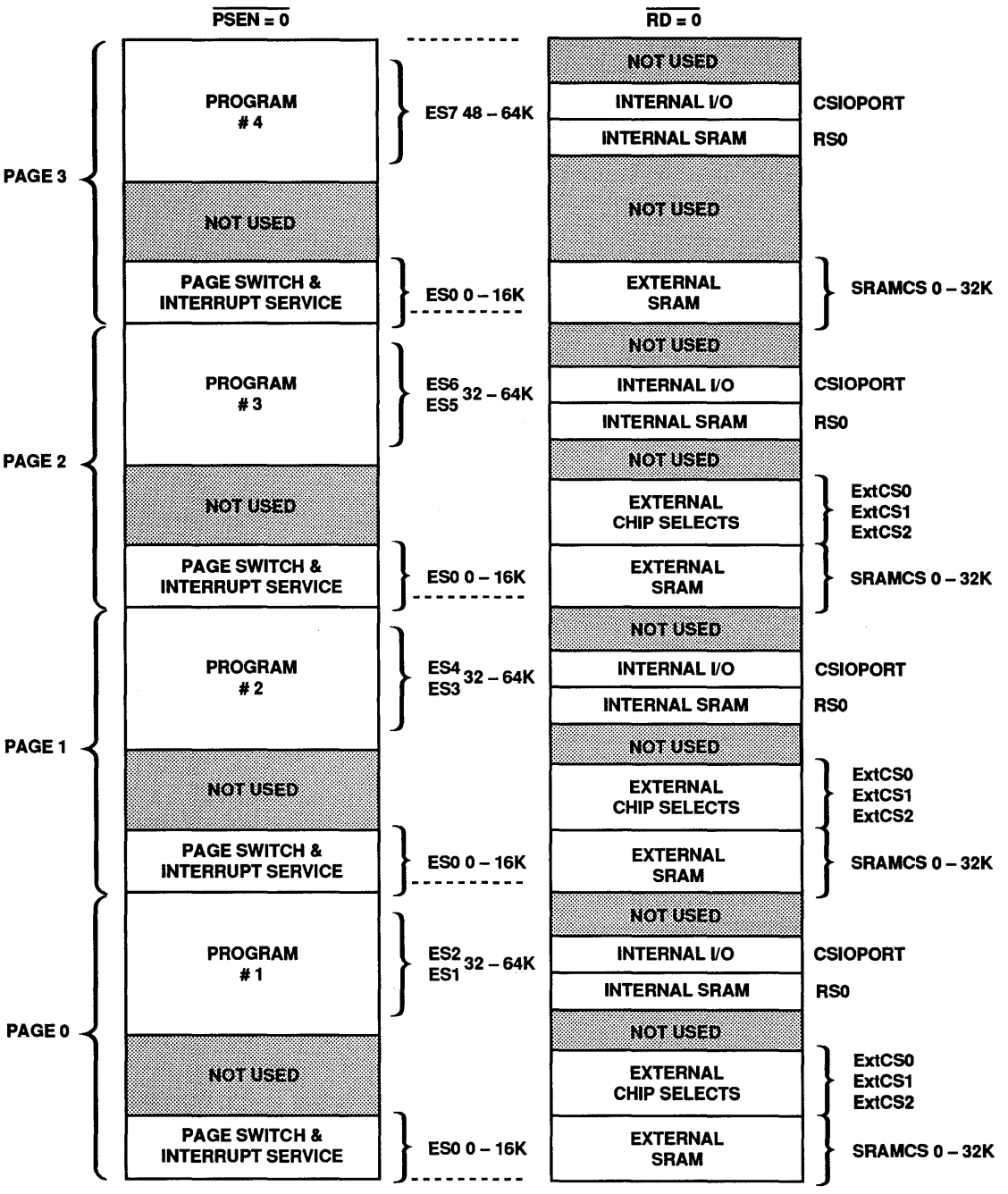
The memory map shown utilizes the page register to provide a unique address for all of the PSD313's 128K Bytes of EPROM in addition to the SRAM and peripherals. This memory map consists of four pages of 64K Bytes each. The map is further divided into program and data space by the PSEN and RD signals which are available in the 8031 microcontroller. This enables the PSD313 to overlap the addresses of the EPROM, I/O and SRAM. The pages are numbered 0 – 3, and are written into the page register by the microcontroller. The page register is part of the I/O addressing and resides in the RD = 0 map.

The software must be broken into four segments, one residing in each page, in order to function efficiently with this memory scheme. The software which enables the machine to boot, service interrupts and switch memory pages is located in a block of EPROM which is mapped into all memory pages. This enables simple page switching and interrupt servicing regardless of the page that the microcontroller is currently operating in. Locating an EPROM block in multiple pages is very simple using the PAD 'don't care' feature. In this example, EPROM block 0 has been chosen to hold the page-independent software. The PAD output which controls block 0 is ES0. Therefore, in the definition of the ES0 signal, all four of the page register bits (P0 – P3) are programmed as 'don't cares'. ES0 is further defined to be from address 0000 to 3FFF. Thus, whenever the microcontroller places an address on the bus which is in this range with PSEN low, the data will be read from EPROM block 0, regardless of the contents of the page register.

The remaining EPROM blocks are evenly distributed into the four pages. This segmentation has been used in this example, but there is no requirement that the pages contain equal memory sizes. Each can have a different amount of resources contained within it. We have placed EPROM blocks 1 and 2 in page 0. This is done by requiring P0 – P3 to be 0's to generate the ES1 and ES2 selects. Similarly, ES3 and ES4 in page 1, ES5 and ES6 in page 2 and ES7 in page 3 require the P0 – P3 signals to be in the correct states to generate the ES signals.

The SRAM and I/O devices most likely must be accessible from all pages, like the page switching software and interrupt service routines. In this way, each of the program segments may store and load data from the SRAM which may be used to pass global parameters among the programs. All programs may also communicate with the external I/O devices, which is most likely required. It is very important that the internal PSD3XX I/O registers, which include the I/O port control and data registers as well as the page register itself, be mapped into all pages. Otherwise, after the page has been switched, there will be no way of switching back to the original page since the page register would not be accessible. To make the page register accessible from all pages, the designer must simply make the page register bits (P0 – P3) 'don't cares' in the equation for the CSIOPORT signal. This can also be done for any of the external chip select equations which are generated by the PAD and brought to the outside world through Port B or Port C.

Figure 4. Memory Map



A Simple Paging Example (Cont.)

If it is desirable for some pages not to have access to some resources, this may be done also. The designer must simply use the page register bits in the equation which selects the resource which is to be protected. This can provide a program security or error handling feature while protecting certain I/O or memory devices from accidental corruption.

Figure 5 contains the output of WSi's Maple software for the above example. The part chosen to implement the sample design was the 8-bit only PSD313, chosen because it contains the required 128K Bytes of EPROM but is less expensive than the PSD303. The PSD303, which also contains 128K Bytes of EPROM, can be configured in a 16-bit data bus mode which would be suitable for use with 16-bit microcontrollers like the 80196.

The PSD313 was programmed and configured to implement the memory map shown in Figure 4. Not all of the capability of the PSD313 has been utilized in this example but is available to satisfy other system design requirements if necessary. The PSD313 has been configured to function with the 8031 microcontroller and its associated control signals. This can be seen in the Configuration portion of the output file in Figure 5. We have also configured Port B 0-3 to provide the required chip select functions for the external I/O and SRAM devices. These chip selects have been given the aliases ExtCS1, ExtCS2 and ExtCS3 for the I/O devices and SRAMCS for the SRAM. The equations entered for the chip selects correspond to the addresses for which they should be active. ExtCS1 will become active when address 8000 - 87FF hex is accessed. ExtCS2 and ExtCS3 will become active for addresses 8800 – 8FFF hex and 9000 – 97FF hex respectively. The SRAM chip select will become active for address 0 – 7FFF hex. All of these chip selects will function independently from the page register contents since the page register outputs (P0 – P3) do not appear in the equations. This means that all of these external devices will be selectable from any page.

The address map lists the start and stop addresses and the page numbers for each of the blocks of memory and I/O inside the PSD313. The first EPROM block is selected by ES0, which has been mapped from address 0000 to 3FFF hex. This block has been designated to contain the page switching software and the boot and interrupt service routines. Since all pages need the capability to switch from one to another, and since an interrupt may be received at any time while the software is executing in any page, EPROM block 0 has been made accessible from all pages by making the page register bits 'don't cares' (x's) in the address map for ES0.

ES1 and ES2 map EPROM blocks 1 and 2 into address 8000 – FFFF hex in page 0. Thus, whenever a program address within this range is accessed by the microcontroller while the page register contains a 0, ES1 or ES2 will activate EPROM block 1 or 2. While the microcontroller is executing code from one of these blocks in page 1, it may still access internal or external SRAM, or internal or external I/O without changing pages. ES3 – ES7 are mapped to pages 1 – 3 in a similar manner.

In addition to the external SRAM, the PSD313's internal SRAM has been mapped into all address pages where it may be used to supplement the microcontroller's register file and internal SRAM. This SRAM may be used for global variable storage, stack space or many other purposes. The PSD313's I/O ports have been mapped at address C800 – CFFF hex in this example. This places the page register address at C81A hex (see the PSD3XX data sheet for I/O addressing in the PSD3XX). As discussed earlier, the page register has been mapped into the same address from all memory pages, so that it may be accessed from all program subroutines in the system.

Figure 5. MAPLE Software Example

```
PSD PART USED: PSD313
********************PROJECT INFORMATION*****************
 Project Name   :    = Page Register App Note
 Your Name      :    = Jeff Miller
 Date           :    = 1/15/92
 Host Processor:     = 8031
*********************************************************

********************ALIASES*******************************
/CS4         = ExtCS1
/CS5         = ExtCS2
/CS6         = ExtCS3
/CS7         = SRAMCS
*********************************************************

********************GLOBAL CONFIGURATION*****************
 Address/Data  Mode:      MX
 Data Bus Size    :       8
 Reset  Polarity :        HI
 Security         :       OFF
 ALE Polarity     :       HI
 A15-A0  ALE dependent (Y) or Transparent (N):   N
 Using Different READ strobes for Data and Program: Y
*********************************************************

********************READ WRITE CONTROL*************
/RD and /WR

*********************************************

********************PORT A CONFIGURATION **********
ADDRESS/IO

*********************************************

********************PORT A (ADDRESS/IO)*****************
PIN     Ai/IO        CMOS/OD
PA0      A0           CMOS
PA1      A1           CMOS
PA2      A2           CMOS
PA3      A3           CMOS
PA4      A4           CMOS
PA5      A5           CMOS
PA6      A6           CMOS
PA7      A7           CMOS

*********************************************************

********************PORT B  CONFIGURATION***************

Pin    CS/IO        CMOS/OD

PB0      CS0          CMOS
PB1      CS1          CMOS
PB2      CS2          CMOS
PB3      CS3          CMOS
PB4      CS4          CMOS
PB5      CS5          CMOS
PB6      CS6          CMOS
PB7      CS7          CMOS
*********************************************************
```

Figure 5. MAPLE Software Example (Cont.)

```
******************PORT B CHIP SELECT EQUATIONS************

ExtCS1     =      / (A15 * /A14 * /A13 * /A12 * /A11 * /P0
                  + A15 * /A14 * /A13 * /A12 * /A11 * /P1)

ExtCS2     =      / (A15 * /A14 * /A13 * /A12 * A11 * /P0
                  + A15 * /A14 * /A13 * /A12 * A11 * /P1)

ExtCS3     =      / (A15 * /A14 * /A13 * A12 * /A11 * /P0
                  + A15 * /A14 * /A13 * A12 * /A11 * /P1)

SRAMCS     =      / (/A15)

******************PORT C CONFIGURATION******************

Pin       CS/Ai        LOGIC/ADDR

PC0        A16         LOGIC
PC1        A17         LOGIC
PC2        A18         LOGIC
A19        CSI

*********************************************************

*****************PORT C CHIP SELECT EQUATIONS***********

*******************************ADDRESS MAP**********************************

       A  A  A  A  A  A  A  A  A SEGMT SEGMT FILE  FILE  File Name   Page Reg Q.F
      19 18 17 16 15 14 13 12 11 STRT  STOP  STRT  STOP                3210   ALE

ES0    N  0  0  0  0  0  N  N  N  0     3fff  0     3fff  PROG0.HEX    XXXX   X
ES1    N  0  0  0  1  0  N  N  N  8000  bfff  0     3fff  PROG1.HEX    0000   X
ES2    N  0  0  0  1  1  N  N  N  c000  ffff  4000  7fff  PROG1.HEX    0000   X
ES3    N  0  0  0  1  0  N  N  N  8000  bfff  0     3fff  PROG2.HEX    0001   X
ES4    N  0  0  0  1  1  N  N  N  c000  ffff  4000  7fff  PROG2.HEX    0001   X
ES5    N  0  0  0  1  0  N  N  N  8000  bfff  0     3fff  PROG3.HEX    0010   X
ES6    N  0  0  0  1  1  N  N  N  c000  ffff  4000  7fff  PROG3.HEX    0010   X
ES7    N  0  0  0  1  1  N  N  N  c000  ffff  0     3fff  PROG4.HEX    0011   X
RS0    N  0  0  0  1  1  0  0  0  c000  c7ff   N/A   N/A   N/A          XXXX   X
CSP    N  0  0  0  1  1  0  0  1  c800  cfff   N/A   N/A   N/A          XXXX   X
*****************************************END*************************************


*********************ADDRESSES OF  I/O PORTS****************
Pin Register of Port A :       C802  Page (Binary): XXXX
Direction Register of Port A : C804
Data Register of Port A :      C806
Pin Register of Port B :       C803
Direction Register of Port B : C805
Data Register of Port B :      C807
Page Register :                C81A
************************************************************
```

Software Considerations

The software example shown in Figure 5, has been divided into four sections to facilitate placing it into the four pages. These four program blocks have been called PROG1.HEX, PROG2.HEX, PROG3.HEX and PROG4.HEX. In order to create these files to be loaded into the PSD3XX, the software designer must plan for this event when the software is written. It is most easily accomplished by breaking the tasks into logical groups that do not need to access one another frequently. Most software can be split in this manner. Then, the designer can create the page switching algorithm which is used to jump between the tasks which are on different pages.

There are many ways to implement this capability, but we will provide as an example one method which can be used. This method of memory paging involves the use of a table of addresses and page numbers of all program tasks which may be called from page to page. This table can be made global when the code is compiled so that it may be used in all four of the programs used in this example. This table would reside in EPROM block 0 along with the interrupt service routines and page switching algorithms so that it may be accessed from all memory pages. Thus, when PROG1 is executing and must run a task or subroutine which is in PROG2, the software should jump to the page switching algorithm while passing the table lookup address of the task that it wishes to run. In this way, only the pointer into the table must be known by all programs instead of the address and page number of each routine. This simplifies the process of modifying the software by permitting the programmer to keep all of the pointers into the table constant, even if the actual subroutine addresses change. In this table, the page switching routine will find the page that it must switch to as well as the address to jump to after the page has been switched. The return address and page number may simply be pushed onto the stack, which is stored in the SRAM. Since the SRAM is also page independent, all programs may share the same stack.

To build the table, the labels of all subroutines which may be shared among pages must be accumulated from all of the programs. These labels must be placed in the table along with the corresponding page numbers. This table must then be placed in the global EPROM block. The labels must be made global so that each program may have access to them. Then pointers into the table must be assigned, one for each global subroutine. These must also be made global so that they may be used by each program. The pointers must remain constant, even when the software is modified. This way, software modifications may change the values of the labels, but not the pointers.

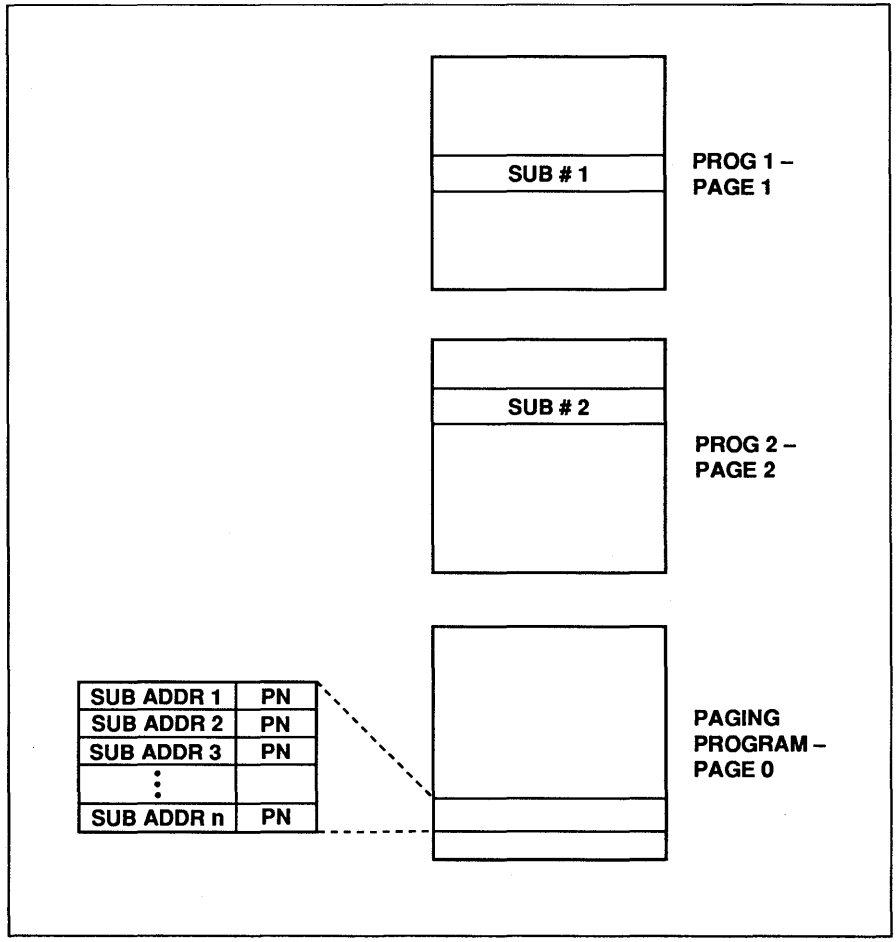
This provides a very clean paging solution which may be implemented using high level language compilers. The only penalty when using this method is the overhead experienced when switching from page to page. This overhead may be minimized by careful software design which minimizes the number of program calls and jumps between routines on different pages. Care must also be taken when nesting jumps from page to page if it is important to keep track of return addresses. Interrupts, since they are accessible from all pages, are very simple to handle. The page need not even be switched to service an interrupt unless the service routine needs to access a task which is not located in the global EPROM block. Even then, the only consideration is that before returning from the interrupt, the page number must be restored to its value prior to the interrupt. This paging scheme is illustrated in Figure 6.

Compiler Issues

The paging algorithm shown below is relatively easy to implement and somewhat automatic. However, it is not a totally transparent solution for the software programmer. There is such a solution available from at least one compiler manufacturer. Archimedes makes compilers for several microcontrollers including the 8031 family and 68HC11 family. These compilers are available with built in memory paging which use some of the microcontroller's port bits as additional address bits. These compilers generate bank switching code automatically which can be easily modified to utilize the page register inside the PSD3XX.

When this is done, the use of the page register becomes transparent to the user. The attached code excerpt shows the calling structure resulting from the use of the Archimedes compiler with the modifications to utilize the PSD3XX page register.

Figure 6. Software Paging Flow



Archimedes Code

```
 836
 837                    /* Init DCC & SCR registers */
 838                init_dsl_hdsl_dcc_scr();
\   0268  7400          MOV     A,#$BYTE3 init_dsl_hdsl_dcc_scr
\   026A  900000        MOV     DPTR,#REFFN init_dsl_hdsl_dcc_scr
\   026D  120000        LCALL   ?X_CALL_L18
 839
 840                    /* Init Master/Slave Polynomial */
 841                init_ms_poly();
\   0270  7400          MOV     A,#$BYTE3 init_ms_poly
\   0272  900000        MOV     DPTR,#$REFFN init_ms_poly
\   0275  120000        LCALL   ?X_CALL_L18
 842
 843
 844
 845            }
```

Notes: 1. $Byte 3 is a directive that addresses the "page" of the specified function.

2. $REFFN Addresses the 16-bit offset of the function.

```
        MODULE    ?BANK_SWITCHER_L18
        TITL      '8051 - C - BANK-SWITCHER'
        RSEG       RCODE
;-------------------------------------------------------------------;
;                                                                   ;
;                       - L18.S03 -                                 ;
;                                                                   ;
;       Function(s):    Banked switched CALL and RET                ;
;                                                                   ;
;       Must be tailored for actual bank-switching hardware.        ;
;       In the sample system the P1 port was used.                  ;
;                                                                   ;
;       Version: 4.00  [IANR]                                       ;
;                                                                   ;
;-------------------------------------------------------------------;

;-----------------------------------------------------;
;                                                     ;
;       Call a non-local function                     ;
;                                                     ;
;-----------------------------------------------------;
;                                                     ;
;       Inputs:                                       ;
;           Stack:  16-bit return address             ;
;           DPTR:  16-bit function-address            ;
;           A:  8-bit page address                    ;
;                                                     ;
;-----------------------------------------------------;
```

The above Archimedes code is courtesy of Jeff Fayne, Tellabs, Inc.

Archimedes Code (Cont.)

```
        PUBLIC   ?X_CALL_L18

?X_CALL_L18
 ==============================
        Save old bank
 ==============================

        PUSH   P1

 ==============================
        Bank-switch
 ==============================

        MOV    P1,A

 ==============================
        Go to function
 ==============================

        CLR    A
        JMP    @A+DPTR

;-------------------------------------------------------;
;                                                       ;
;       Leave current function                          ;
;                                                       ;
;-------------------------------------------------------;
;                                                       ;
;       Input:                                          ;
;          Stack:  24-bit return address                ;
;                                                       ;
;-------------------------------------------------------;
        PUBLIC  ?X_RET_L18

?X_RET_L18:
 ==============================
        Bank-switch
 ==============================

        POP    P1

 ==============================
        Return
 ==============================

        RET

        END
```

Conclusion

The PSD3XX page register system can greatly assist designers of systems requiring large memory spaces with 16-bit address buses. The PSD3XX offers capability not found in most discrete page register implementations. The capability to define global resources as well as page-specific resources enables the designer to implement the paging technique most suitable for the application. The page register is included in the PSD302, PSD312, PSD303 and PSD313 devices, all of which are pin compatible with one another. This provides the capability of expanding the memory size as required even after a system has been designed. The designer can simply drop the new, and larger, PSD3XX into the same footprint as the old, and update the software to add more memory pages. This capability can be important for product feature additions after a design is complete. Since the system is fully programmable, it may be updated and changed anytime.

Power considerations in the PSD3XX

PSD3XX

By Jeff Miller – WSI

Introduction

The PSD3XX is a configurable microcontroller peripheral integrating programmable logic, EPROM and SRAM technologies into a single piece of silicon. It has been used extensively in microcontroller applications around the world by virtue of its high level of integration, configurability and ease of use. This integration makes possible the design of very compact microcontroller systems, enabling the user to squeeze a great deal of functionality into a very small space. Thus, the PSD3XX has found its way into many small hand-held and/or battery operated applications such as cellular phones, medical instrumentation and laptop or notebook computers which usually require, in addition to small space, a very low power consumption.

The PSD3XX family is based on a patented high-performance CMOS technology and, like other CMOS devices, requires very low power consumption even when no particular effort is made to minimize the PSD3XX power. But, when some special care is taken during the programming and configuration of the device, power can be reduced even further, making the PSD3XX even more valuable in these power-sensitive applications. This application note will describe the methods which can be used to reduce the PSD3XX power consumption in both active and stand-by modes. It makes sense to use some of these techniques even when low power is not a primary design requirement since they are easy to implement and require no additional expense. We believe that proper implementation of the material in this note will make the PSD3XX an invaluable member of any low-power microcontroller system.

Power Use In The PSD3XX

The PSD3XX contains several modules internally, each of which can be considered a power consumer when in operation. These modules include the PAD, (Programmable Address Decoder)EPROM and SRAM blocks. The key to reducing the power used by the PSD3XX is to reduce the power used by each of these modules individually.

Under normal operation, several of the functional modules may be operating, while others may be standing by. A module in stand by uses much less power than one that is active. For example, whenever the SRAM is not being actively used, it is disabled and therefore consumes less power. This is also true of the PAD. A PAD term which is active expends more power than one which is inactive. This would also be true of the EPROM. However, in some PSD3XX models, the EPROM is always active, in which case it will always draw power. This is done in order to provide the best access time possible for the EPROM. The Low Power family of PSD3XXs does not keep the EPROM enabled at all times, and thus the designer can save power by minimizing the time during which the EPROM is accessed. Use of this feature does impact the speed of the PSD3XX EPROM, which results in the loss of the 120 ns speed grade. There are other methods of reducing EPROM power even when the EPROM is enabled. These will be discussed in detail later in this note. When the time that each PSD3XX function is kept in standby mode is maximized, the power expense is minimized.

There is a way to place the entire PSD3XX into the standby mode at once, thereby reducing power usage to the bare minimum. This can be done through the use of the CSI (Chip Select Input) pin. When the PSD3XX is deselected by the CSI pin, the entire part enters the standby mode using only about 50 μA of current. While in this mode, the PSD3XX is incapable of performing any functions, including PAD logic equations, but this is an excellent method of reducing system power in designs which have low active duty cycles.

Power considerations in the PSD3XX PSD3XX

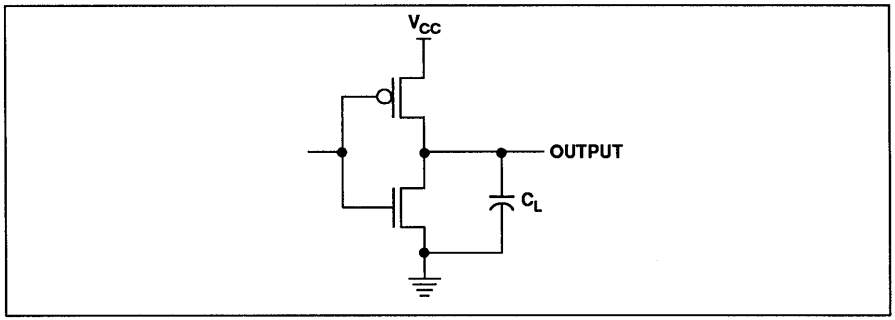
CMOS Power Characteristics

As a CMOS part, the PSD3XX behaves in the same way as other CMOS devices in terms of power dissipation. The PSD3XX consumes the most power when the temperature is low, the voltage is high and the frequency is high. Low temperature in CMOS devices, unlike in bipolar devices, causes the transistors to speed up, thus consuming more power. Therefore, if the system will never operate in low temperature environments, power dissipation will be lower. Another result of this characteristic is that CMOS parts do not generally experience thermal runaway. As temperature increases, the power expended by the CMOS device decreases, thus the part tends to effectively cool itself off.

Another characteristic of CMOS devices is the effect of voltage variations. CMOS behaves similarly to TTL devices with respect to voltage. When input voltage rises, the current drawn by a CMOS device also rises. As input voltage falls, input current also falls. Thus, the CMOS device will draw the least current at its lowest allowable supply voltage. This voltage is 4.5V in the PSD3XX. Taking the voltage below this level will generally slow the device down to below its specified speed as well as jeopardize its data retention capability. Between 4.5 and 5.5V, the PSD3XX varies by about 0.85mA per 0.1V variation. Thus, the PSD3XX will draw approximately 0.85 mA less current at 4.9V than at 5.0V V_{CC}.

Lastly, frequency of operation plays an important role in the power dissipation of a CMOS device. A CMOS gate expends the greatest power while it is switching between the logic 0 and logic 1 states, or vice versa. This can be easily understood when looking at the circuit diagram for a typical CMOS output shown in Figure 1.

Figure 1. Typical CMOS Output Circuit



The circuit above represents a typical CMOS inverter output. Normally, either the top transistor is off (output = logic 0) or the bottom transistor is off (output = logic 1). MOS transistors have very low leakage currents which means that under these normal conditions, very little current will be passing from V_{CC} to ground. However, when the input to the inverter is switching, both transistors will not switch from their present conditions to their new conditions at precisely the same instant. Therefore, both transistors will be on for a very brief instant during the transition. During this time there is a low impedance path from V_{CC} to ground and some current is drawn by the circuit. In addition, the output will have some load capacitance (C_L) which must be charged during switching, even if the load itself draws little or no static current. Thus, during the switching process the power expended by a CMOS device is at its highest.

The switching current drawn by the device is dependent on the number of times the outputs are forced to switch logic states in a unit of time. Therefore, the frequency of operation of the part directly influences its dynamic power consumption. The lower the operational frequency, the lower the dynamic power expended by the device. In the PSD3XX, frequency of operation is determined by the rate at which the addresses are changing, usually indicated by the frequency of the ALE or AS signal. Generally, the PSD3XX draws about 3 mA of additional current for each 1 MHz added to the frequency of operation.

Power Management Techniques In The PSD3XX

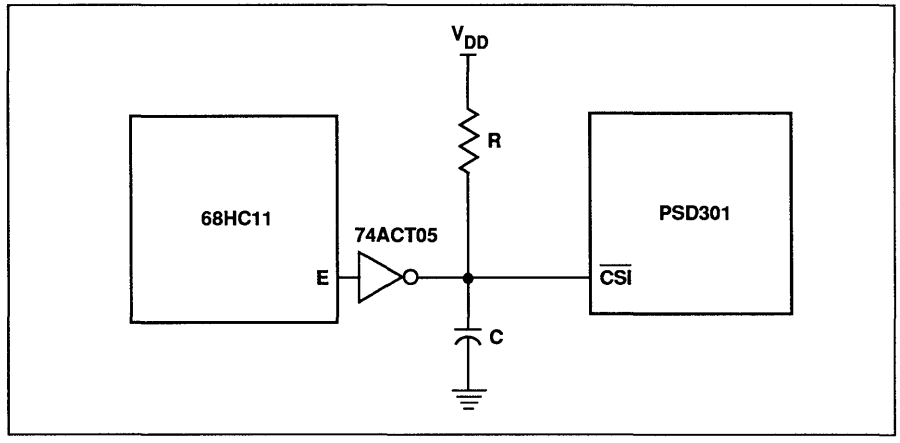
The above mentioned features and characteristics can be used to the designer's advantage when designing compact microcontroller systems which have a tight power budget. In the sections that follow, several methods for reducing the PSD3XX power will be presented.

Power Down Mode

Many system designs do not require the microcontroller, and therefore the PSD3XX, to operate continuously. Systems, like cellular telephones and notebook computers, spend a large amount of time inactive – waiting for something to happen like a press of a button or keyboard. During this time, many designers place the microcontroller into a low power idle or sleep mode. In the sleep mode, the controller expends significantly lower power. The microcontroller is usually awakened by some event – a key on a keypad being pressed, for instance, which may result in an interrupt. There is no need for the PSD3XX to be active during the time that the microcontroller is not active. Therefore, the PSD3XX should be placed in the power down mode (CSI inactive) to reduce the PSD3XX current down to its standby value.

The PSD3XX must also be awakened when the microcontroller is awakened so that it may provide an instruction to the controller when it requires one. If the microcontroller itself has a chip select output, like the Motorola 683XX series controllers, it may be used to awaken the PSD3XX as necessary. However, if it does not, there will be a problem. If the microcontroller itself is used to power down the PSD3XX, through an I/O port pin for example, there will be no way to power up the PSD3XX again since the PSD3XX itself contains the instruction that the microcontroller must use to activate the CSI signal to awaken the PSD3XX. The way to correct this situation is to design a circuit which detects when the microcontroller is coming out of its power down mode before it must fetch the first instruction. Such a circuit is depicted in Figure 2

Figure 2. Simple Power Down Circuit



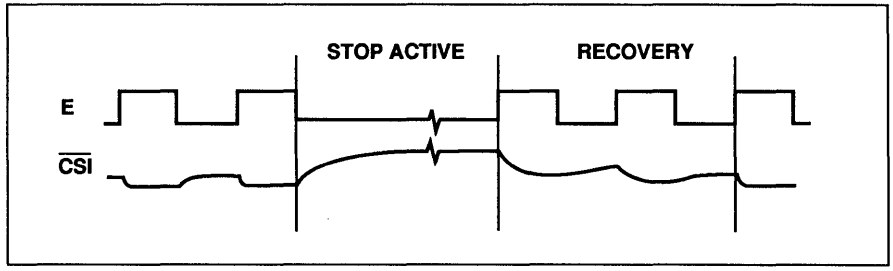
In this circuit diagram, a Motorola 68HC11 microcontroller is connected to a PSD3XX in a low power system. The circuit functions quite simply. The E signal from the HC11 is normally a free running clock at 1/4 the frequency of the input clock. When the HC11 is placed into the sleep mode by the software (by executing the STOP instruction), the E signal stops oscillating and remains low until an interrupt or internal timer event occurs. After the interrupt has been received by the controller, the E signal resumes toggling, but there will be a minimum of two E clock cycles prior to the first AS. This characteristic can be used to place the PSD3XX into its low power standby mode whenever the STOP has been executed in the HC11 and to awaken it before it must supply an instruction to the HC11.

Power Management Techniques In The PSD3XX (Cont.)

The ACT05 device shown in the diagram is simply an open collector inverter. When the E signal is oscillating, the output of the inverter will be toggling between ground and high impedance. When the output is at ground, the capacitor will rapidly discharge from its present state into the ACT05. When the output is high impedance, the capacitor will slowly charge up to V_{CC} through the resistor. Thus, under normal operation the $\overline{CSI}$ input of the PSD3XX will be at or near 0 V, provided the RC time constant is large enough to prevent the capacitor from charging up beyond a logic zero level of 0.6 V.

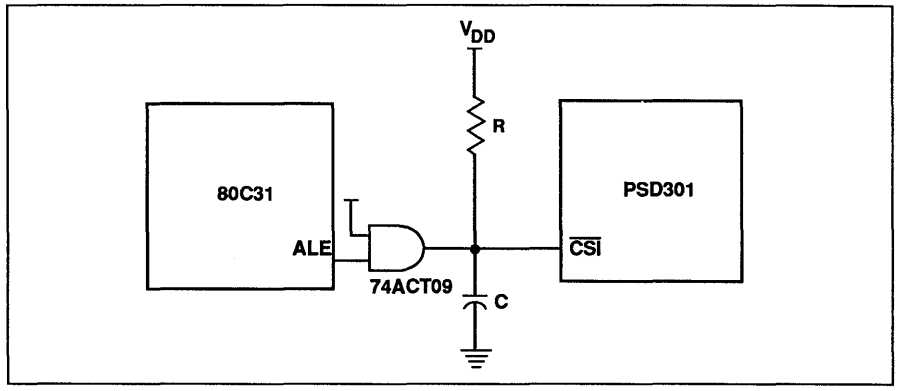
When the HC11 enters the sleep mode the E signal remains low. This enables the capacitor to slowly charge up to a logic one level which then places the PSD3XX into the standby mode in which it will consume only about 50µA of current. After the controller exits the sleep mode, the E signal will resume oscillating which rapidly discharges the capacitor. This, in turn, activates the $\overline{CSI}$ input to the PSD3XX, bringing it out of the power down mode. Since the E signal will oscillate for at least two full cycles before the first AS strobe begins a new bus cycle, the PSD3XX will have ample time to recover from the power down mode before having to supply an instruction to the HC11 for processing. In operation, the circuit results in a timing diagram similar to the one in Figure 3.

Figure 3. 68HC11 Stop Timing



A similar circuit can be used for Intel 8031 type controllers. Controllers conforming to the Intel 8031 family generally have two low power modes: IDLE and POWER DOWN. The IDLE mode causes the controller to cease instruction execution, but its internal clocks continue to run. This saves significant power while leaving the internal timers and other functions operational. When in the IDLE mode, both the ALE signal and the $\overline{PSEN}$ signal are held high. A circuit similar to the one illustrated for the 68HC11 may be used to detect the end of oscillation on the ALE signal. This circuit is shown in Figure 4.

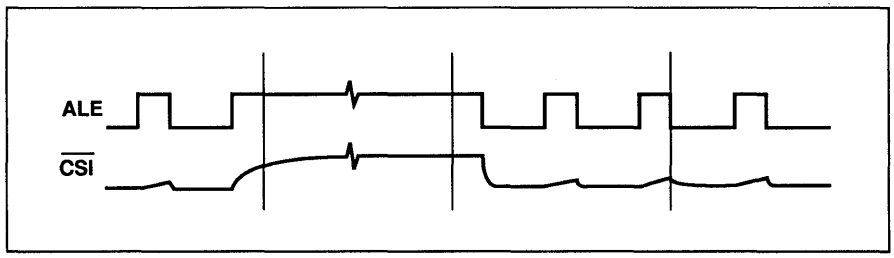
Figure 4. 8031 Idle Circuit



Power Management Techniques In The PSD3XX (Cont.)

The circuit operates on the same principle as the one used earlier for the Motorola processor. The ALE signal normally oscillates high for 2 clocks out of every 6 or 12 clocks, depending on whether instruction or data accesses are being performed. The software places the 8031 into the Idle mode by setting bit 0 in the PCON register. Once set, the ALE and $\overline{PSEN}$ signals remain high until an interrupt or hardware reset occur. During this time, the $\overline{CSI}$ signal will float high with the RC circuit, as in the earlier example. The ACT09 is simply an AND gate with an open collector output. It performs the same function as the inverter in the previous example without inverting the signal. When an interrupt or reset is received, the ALE signal begins to toggle again, but at least two "dummy" unused ALE cycles will occur before the first meaningful instruction is fetched, giving the PSD3XX time to recover from the power down mode. The timing for the above circuit is shown in Figure 5.

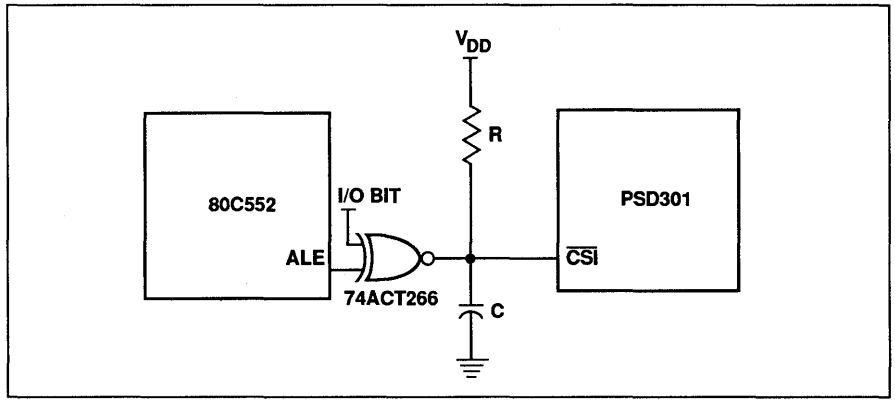
Figure 5. 8031 Idle Timing



If the system requires truly the lowest power available, the 8031 POWER DOWN mode may be used. This disables all internal operations of the 8031 as well as the external ones. Thus, any on-chip peripherals like timers and serial communication links will be disabled. This places the controller into its lowest power mode possible. Software may place the 8031 into the POWER DOWN mode by setting bit 1 in the PCON register. When execution of the instruction is complete, the ALE signal will be driven low and will remain in this state until a hardware reset is received. Thus, a circuit similar to the one above may be used to detect the static condition of the ALE signal, but an inverting gate must be used instead of the ACT09 (such as the ACT05 used in the Motorola example earlier).

If both the POWER DOWN and IDLE modes must be used, the gate may be replaced with an ACT266 exclusive NOR with an open collector output. This circuit is shown in Figure 6.

Figure 6. 8031 Power Down or Idle Circuit



Power Management Techniques In The PSD3XX (Cont.)

The I/O bit can be provided by either the PSD3XX or the controller itself. If the controller is used to provide the I/O bit, it must hold the correct value on the output even when in the idle or sleep mode, as the PSD3XX does. When the I/O bit is low, the POWER DOWN mode is enabled (a low on ALE and a LOW on the I/O bit will result in a high on $\overline{CSI}$). When the I/O bit is high, the IDLE mode is enabled (a high on ALE and a high on the I/O bit will result in a high on $\overline{CSI}$).

For all of the above circuits to operate correctly, the value of the RC network must be carefully calculated to insure proper operation in the normal mode. This means that under normal operation, $\overline{CSI}$ must never climb above 0.4 V, which will guarantee that it is always recognized by the PSD3XX as a low.

For example, the 68HC11 circuit shown in Figure 2 used the E signal from the controller to disable the PSD3XX. The E signal oscillates at 1/4 the frequency of the HC11's input clock. If an 8 MHz HC11 is used, the E signal will oscillate at 2 MHz. This results in an E signal clock period of 500 ns. During this 500 ns the E signal will be low for 250 ns. Thus, the RC network must be chosen to prevent the $\overline{CSI}$ signal from climbing above 0.4 V for at least 250 ns. The equation below governs the voltage across the capacitor (V_C), and thus the voltage present on the $\overline{CSI}$ pin:

$$V_C = V_{CC}(1 - e^{-t/RC})$$

where V_C is the voltage across the capacitor (which is the same as the $\overline{CSI}$ pin), V_{CC} is the supply voltage, and t is the time in seconds after the output of the open collector gate switches from a low to an open circuit. Solving for RC we get:

$$RC = -t/\ln(1-V_C/V_{CC})$$

In order to determine the minimum values for R and C, we must solve this equation for the point of time which is of interest. We must have V_C no greater than 0.4V at time t = 250 ns. Thus, with V_{CC} = 5 V, the equation may be rewritten as follows:

$$RC = -250 \times 10^{-9}/\ln(1 - 0.4/5.0) = 3.0 \times 10^{-6}$$

An acceptable RC network for this case might be a resistor of 100KΩ and a capacitor of 30pF. These values will provide no margin for the circuit so some additional resistance or capacitance may be desired. Of course, larger values may be used without harming the circuit, they will just cause the low power mode to be entered more slowly. The case of leaving the low power mode is less critical, since the capacitor will discharge more quickly through the gate than it will charge up through the resistor. In the interest of minimizing power use by the circuit itself, it is best to use a larger resistor value and a smaller capacitor value, since this will cause less current to be sunk by the gate which drives the circuit.

Using this equation, it is possible to determine the RC value required for any controller and/or frequency. It is only necessary to determine the length of time that the RC will be required to hold the $\overline{CSI}$ signal below 0.4 V and plug that value into the above equation.

If a more deterministic method is desired for placing the PSD3XX in the power down mode, a fully digital circuit may be implemented which uses very few additional components. This circuit is shown in Figure 7 for the 68HC11 controller.

This circuit performs the same function as the RC circuit described earlier, but does it digitally. The 74ACT164 is a shift register which is used in this example to detect when eight HC11 input clocks occur while the E signal remains low. In normal operation, no more than two clocks should occur without E transitioning from low to high, thus providing a clear to the ACT164. If the HC11 is stopped, the E signal will remain high until an interrupt is received, but the input clock continues to run freely. Thus, the shift register will shift in "one's" until the E signal goes high again. When the ACT164 has shifted eight times, the $\overline{CSI}$ signal will go high, placing the PSD3XX into the power down mode. The timing diagram corresponding to this circuit is shown in Figure 8.

Figure 7. Digital Sleep Circuit For 68HC11

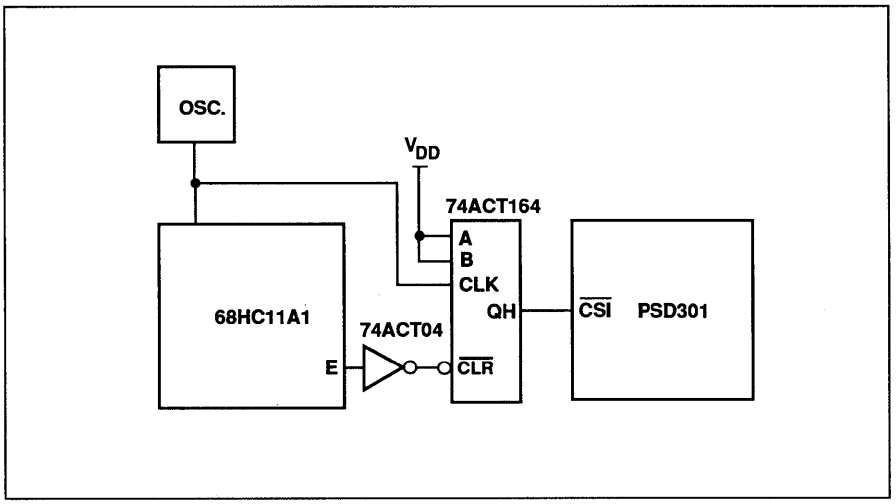
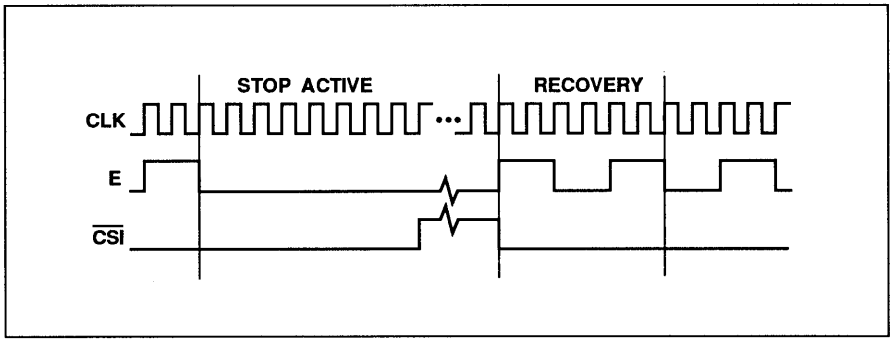


Figure 8. 68HC11 Stop Mode Timing



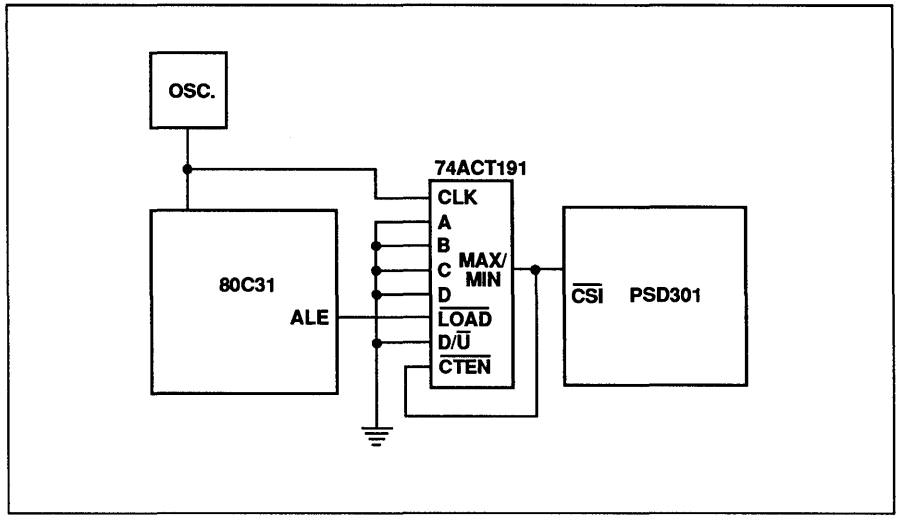
Power Management Techniques In The PSD3XX (Cont.)

A similar circuit may be used for the 8031 family of controllers, and is depicted in Figure 9.

This circuit, like the others, detects when ALE stops toggling. Since up to 10 clocks may normally occur without an ALE pulse, a counter which can count to at least 11 is required in order to function properly. Thus, an 8-bit shift register like the one used with the HC11 will not work. In this case, a 74ACT191 is used to count 16 clocks prior to raising its MAX/MIN output high. A low on the ALE signal will load zero's into the counter and clear the MAX/MIN output. The MAX/MIN output is also used as the counter enable to prevent the counter from counting further after attaining the count of 16. The circuit shown will function with the IDLE mode of the 8031. If the POWER DOWN mode is used, an inverter must be inserted in the ALE signal path.

Other controllers, not listed here, may also have power down modes which may function with these circuits. Any controller which has some sort of external indication when the power down mode has been entered may usually be used to place the PSD3XX in its low power mode also.

Figure 9. Digital Sleep Circuit for 8031 Family



Power Management Techniques In The PSD3XX (Cont.)

PAD Programming Techniques

The preceding section has described methods of using the power down capability of the PSD3XX with several microcontrollers. There are also techniques which may be utilized during programming of the device to further reduce power. These techniques can significantly reduce the power expended by the PSD3XX when it is in full operation.

The programmable logic section of the PSD3XX, called the PAD, provides much of its great flexibility and configurability. It is used to control the internal resources of the PSD3XX and can also be used to control external resources as well. The power use of the PAD varies greatly depending on how its product terms are programmed and used.

The PAD is illustrated in Figure 10. It is divided into two sections, called PAD A and PAD B. PAD A is responsible for generating the control and selection for the internal resources of the PSD3XX and utilizes 13 product terms to perform these functions. PAD B provides any external chip selection and logic replacement that is necessary for the system and has 27 product terms for this purpose. A single product term is functionally illustrated in Figure 11.

Each of the PAD inputs and its complement is available to each of the 40 product terms of the PAD. Each of these inputs is connected to an n-channel transistor which is used to connect the entire line to ground when the input is in the appropriate state. A high on the input to the gate causes the transistor to turn on. When the device is programmed, each of these transistors may be left in place or may be functionally removed (programmed out) from the circuit. If all of the transistors are programmed out, the line is left connected only to the pull-up resistor which makes it always high. Thus, the output of the inverter is always low. If an equation such as:

/CSx = In#1 • /In#2

is programmed into the PAD, the output $\overline{CSx}$ must be high except when In#1 is high and In#2 is low. Thus, all of the transistors are programmed out except the ones connected to In#1 and In#2. This means that unless In#1 is high and In#2 is low, there will always be at least one of the two remaining transistors turned on, which in turn results in the $\overline{CSx}$ output being high. When the appropriate input condition is met, the remaining two transistors will turn off, which allows the output to become low.

Figure 10. PAD Illustration

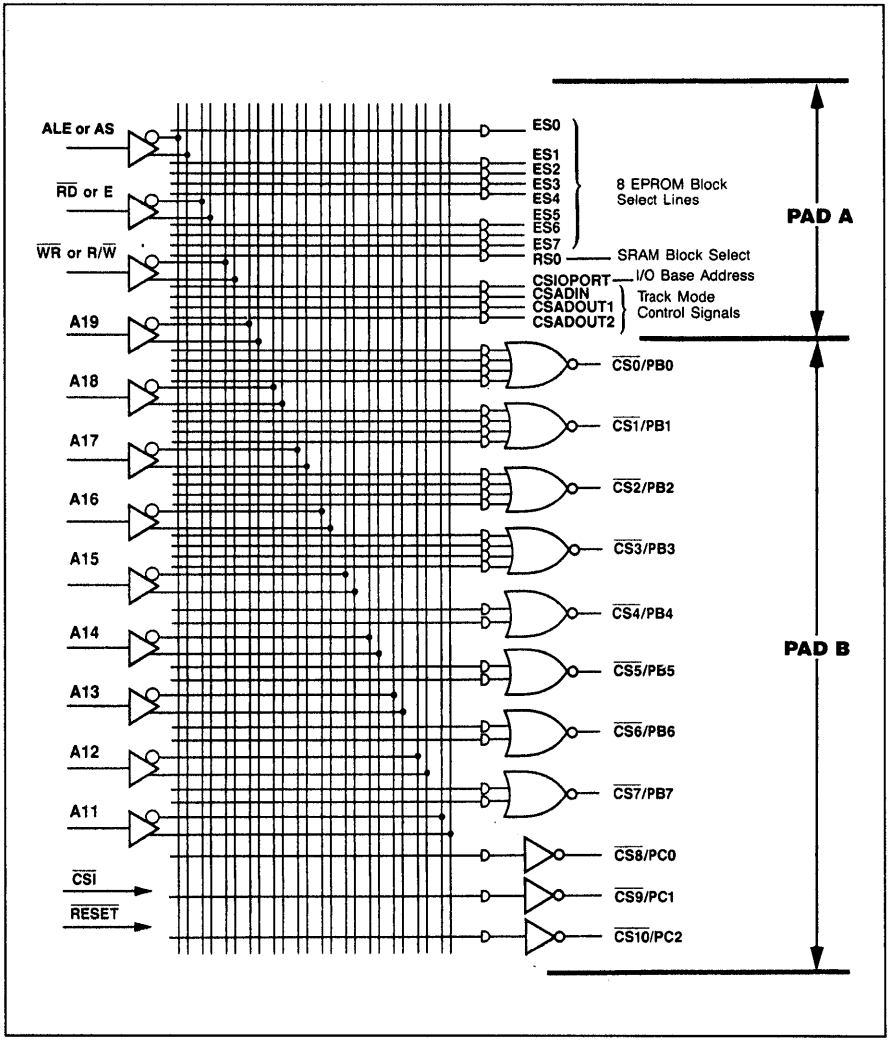
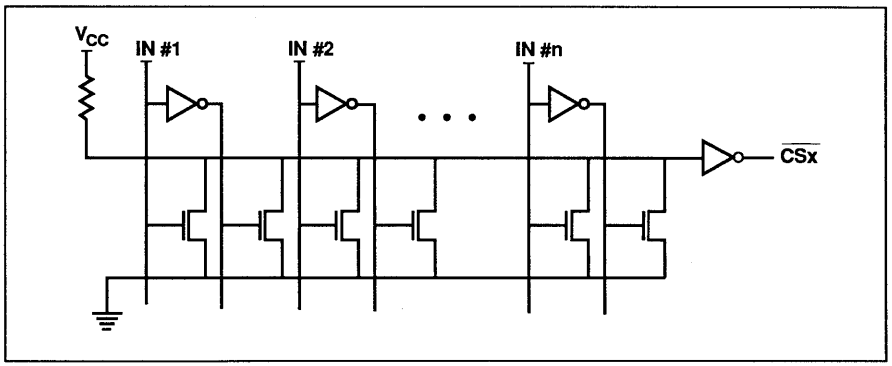


Figure 11. Product Term Functionality



Power Management Techniques In The PSD3XX (Cont.)

As can be seen in the figure, the product term expends very little power when all of the transistors are either programmed out or turned off. The only power used in this case is the result of the leakage current through the various off transistors, which is very low in CMOS technology. When one or more of the transistors is turned on, there will be current drawn through the pull-up resistor to ground. Therefore, the power used by a product term varies greatly according to the way it is programmed.

Experimental data has shown that a product term with all of the transistors programmed out draws approximately 380µA less current at room temperature and 5.0 V V_{CC} than a product term which has some active transistors. WSI's MAPLE software packages take advantage of this fact to reduce power as much as possible.

When the user intends to use some or all of the Port B pins as I/O signals, then they are not connected to the PAD in any way. Thus, the MAPLE software is free to program the unused PAD B product terms in any way. In MAPLE versions 4.03B and subsequent, the software automatically programs out all transistors in each unused product term, which can eliminate up to 24 product terms for Port B. This results in a power reduction of up to 9.1 mA.

If one or more of the Port C pins is programmed as an address or logic input, MAPLE is free again to program out all of the transistors in each unused PAD B product term dedicated to Port C. This can eliminate up to 3 additional product terms resulting in a power reduction of over 1 mA.

Finally, there are three product terms from PAD A which are dedicated to controlling the Port A Track Mode operation. If the Track Mode is not used in the application, these product terms may also be eliminated by MAPLE for a power reduction of over 1 mA.

The remaining ten product terms are the 8 EPROM select lines, the SRAM select line and the I/O port select line. These terms may not be eliminated by MAPLE without disrupting the operation of the device. But in a system which uses Port A and Port B as I/O or address outputs, and Port C as address or logic inputs, the total system power saving is 10.2 mA typical.

The same methods may also be used in non-multiplexed microcontroller applications. In this case, Port A and Port B may be used as microcontroller data input pins, depending on whether the controller is 8- or 16-bit. As in the earlier cases, if the ports are used as data input pins, they are not connected to the PAD which allows MAPLE to program out the appropriate product terms.

Again, MAPLE 4.03B or a subsequent revision must be used to obtain this capability. If your software is an older revision, contact your local WSI regional sales office for a free update.

EPROM Programming Techniques

Like the PAD, the EPROM in the PSD3XX uses varying amounts of power depending on how it is programmed. When programmed to a one, an EPROM bit draws more current than when programmed to a zero. Thus, for minimum power usage it is best to have the majority of the EPROM programmed to zeros.

Unfortunately, the contents of the EPROM are fixed by the program and data requirements of the system and thus cannot be easily optimized for power. However, the user can program all unused sections of the EPROM to zeros. This will not substantially cut the power used by the PSD3XX under normal operation when EPROM accesses are being performed, but it will reduce the power consumption during periods when there is not a valid address on the bus because these invalid addresses will often point to unused EPROM locations. When an EPROM location is currently addressed, it is expending power even if the $\overline{RD}$ or $\overline{PSEN}$ signals are not actually enabling an output. Therefore, it is best that unused EPROM locations be filled with zeros so that power is minimized during these periods of invalid addresses. It should be noted that all power figures used in this application note as well as those specified in the PSD3XX data sheet are based on an average of 50% "ones" and 50% "zeros" contained in the EPROM. An EPROM location programmed to "ones" will draw approximately 1.5 mA of additional current over an EPROM location programmed to "zeros".

Power Management Techniques In The PSD3XX (Cont.)

An even better way to help minimize power usage is to control the addresses which appear on the bus when there is no valid address being driven by the microcontroller. The least power expense will be when this unused address points to an area which has no PSD3XX resource mapped into it. This will result in no internal resource block receiving a chip select and thus the least amount of current will be drawn. The next best approach is to have the unused address point to an EPROM area containing zeros. The next lowest power would be to have the unused address point to an EPROM area containing something other than zeros. Finally, the highest power will occur when the unused address points to an SRAM location.

Since there is not much that can be done about the address that is appearing at the output of the microcontroller, the best that can be done is to know what address the controller will have active on its bus at various non-operational times and insure, if possible, that the PSD3XX's address map maps that address into a desired range of memory (preferably no memory at all). This will truly minimize the power expended by the PSD3XX during these times.

Summing It All Up

After taking all of these factors into account, what kind of power use can you expect from the PSD3XX in your own system? As a guideline, we will calculate the typical power required of a PSD3XX installed in a hypothetical system. The requirements of this system are listed in Table 1.

Using this information, we can calculate the approximate typical power requirements of the PSD3XX. Before we can begin, we must know what the base power of the PSD3XX is under the voltage and temperature conditions specified. The base power of the PSD3XX is the power used by the PSD3XX when only the product terms which control the EPROM, SRAM and I/O ports are not programmed out (10 active product terms). The base power also assumes that no internal resources (EPROM, SRAM and I/O ports) are being currently accessed. The current drawn by the PSD3XX under these conditions has been determined experimentally to be 16 mA. To this current, we must add additional current for the other active product terms, SRAM access and EPROM access.

Table 1. Hypothetical System Requirements

Characteristic	Specification
PSD3XX Operational Frequency	2 MHz
Port A	Address Output
Port B	4 Chip Select, 4 I/O
Port C	Logic inputs
$\overline{CSI}$	Configured for Auto. Power Down
V_{CC}	5.0 V
Temperature	25°C
Standby duty cycle	60%
EPROM duty cycle	30%
SRAM duty cycle	10%

Summing It All Up (Cont.)

The system is requiring only four of the 11 available chip select outputs. Therefore, most of the PAD B product terms may be programmed out. To determine how many product terms we will be using, we must look at the equations for the four chip selects. Assume that the following equations are to be used:

/CS#1 = /(A15 • A14 • RD + A13 • A12 • WR)

/CS#2 = /(/A18 + /A17)

/CS#3 = /(A16 • A18 + A17 • ALE)

/CS#4 = A17

In order to configure the system for the lowest power usage, we must be sure that we place these chip selects on the output pins which will require the minimum number of product terms to remain active. Since the maximum number of product terms required to generate the above equations is only two, there is no need to place these chip selects on Port B pin 0,1,2 or 3 since these pins each have four product terms. The lower power configuration would place these chip selects on Port B pin 4,5,6 and 7, where only two product terms will be drawing power for each chip select. One of the above chip selects, #4, actually requires only one product term, meaning that it could be placed on one of the Port C pins which have only one product term. However, all of Port C is used in this case as logic inputs (A16, A17 and A18) and therefore cannot be used as chip selects. Since the rest of the Port pins are not used as PAD outputs, the MAPLE software will automatically program them out.

If we do configure the chip selects to output on PB[0:3], we must add 8 product terms to the 10 used in calculating the base power number. Using the current per product term of 380µA provided earlier, eight additional product terms result in an additional 3.0 mA of current.

Experimental data has shown that accessing the SRAM results in an additional current expense of 31 mA above the base current. Also, accessing the EPROM draws an additional 0.5 mA over the base current. The standby current has been measured at 50 µA. Finally, we must consider the additional current used by the frequency of operation. This is 3 mA per 1 MHz for a total of 6 mA, since the PSD3XX will be operating at 2 MHz. This provides us with all of the data that we need to calculate the total power usage of the PSD3XX in this system.

Table 2 can be used to calculate the EPROM access current, the SRAM access current and the standby current.

Table 2. Summary of PSD3XX Current Usage In Hypothetical System

PSD3XX Block	Current Used
Base Configuration	16 mA
PAD (as configured)	3.0 mA
EPROM	0.5 mA
SRAM	31 mA
Frequency Component	6 mA
Standby Current	50 µA

Now, summarizing further, the total EPROM access current is:

Base Current + PAD Current + EPROM Current + Frequency Component
= 16 mA + 3.0 mA + 0.5 mA + 6 mA
= **25.5 mA**

The total SRAM access current is:

Base Current + PAD Current + SRAM Current + Frequency Component
= 16 mA + 3.0 mA + 31 mA + 6 mA
= **56.0 mA**

Summing It All Up (Cont.)

Now we must account for the duty cycle of the system to determine the total average power for the PSD3XX. In order to apply the duty cycle, we simply multiply each power component by its duty cycle and add them all together. The equation to perform this is given below:

$$\text{Total Current} = 0.6(i_{SBY}) + 0.3(i_{EPROM}) + 0.1(i_{SRAM})$$

where i_{SBY} is the standby current, i_{EPROM} is the active EPROM current and i_{SRAM} is the active SRAM current. Plugging in the numbers we developed earlier, the equation becomes:

$$\text{Total Current} = 0.6\ (50\ \mu A) + 0.3\ (25.5\ mA) + 0.1(56.0\ mA) = \underline{\mathbf{13.3\ mA}}$$

The average current drawn by the PSD3XX under the specified conditions of configuration, frequency and environment is therefore 13.3 mA. The peak typical current used by the PSD3XX is 54 mA while the SRAM is being accessed. The minimum current is 50 µA, drawn by the PSD3XX while it is in the Power Down mode. This compares very favorably with the typical current usage of a fully discrete solution.

Typical vs. Maximum Current

The typical and maximum current numbers are both specified by most integrated circuit manufacturers. Many designers are unsure of what these parameters are and how they relate to the power which will actually be dissipated by the system. This is compounded by the configurability of the PSD3XX.

The maximum power numbers published in most product specifications are usually chosen as the number which will never be exceeded by the device under any circumstances, including variations in processing, V_{CC} and temperature. To truly be a maximum number, all three of these parameters must be at their worst cases simultaneously, which is quite unlikely. Therefore, power use will more likely follow the typical values when the system is actually running.

In the PSD3XX data sheet published by WSI, two current values are published for typical conditions and another two are published for worst case conditions. These two sets of numbers are used to specify current use in two different PSD3XX configurations. The lower numbers represent the current drawn by the PSD3XX while configured with 10 active product terms. To arrive at the maximum value for this configuration, we assume that the programming of the device has not changed, but we take the temperature, voltage and processing to their worst case conditions. These numbers are generated again for the configuration of the PSD3XX which has all 40 product terms active. To determine the typical current drawn by the PSD3XX in your system, it is best to use the techniques presented in this application note. All of the typical current values used in this note are the result of careful experimentation, and should parallel very closely the values measured in your own system. To extrapolate the worst case current for your configuration from your calculated typical value, you must add about 50% to account for voltage, temperature and process variation.

When calculating the worst case current for your entire system it is usually best to use the typical current numbers for all of the components installed and then apply some margin to allow for worst case conditions. This is much more accurate than using the worst case parameters for each component since it is *extremely* unlikely that *all* of the components used are simultaneously at their worst case process parameters, though they may all be at worst case voltage and temperature. Usually 20% margin above the typical numbers will sufficiently cover the worst case for the entire system.

Table 3 summarizes the typical current numbers for the PSD3XX which can be used when calculating the current used in your own system.

Table 3. Summary of PSD3XX Typical Current Usage

Base Current (10 product terms, SRAM and EPROM Unselected)	16 mA
Additional Current per Product Term	0.38 mA
Additional Current for SRAM Access	31 mA
Additional Current for EPROM Access	0.5 mA
Additional Current for Frequency Effects	3 mA/MHz
Additional Current for Voltage > 5V	0.85 mA/0.1V
Standby Current	50 µA

Conclusion

The PSD3XX is a very important device in the design of compact, low-power systems. It provides a cost effective minimum part count solution for a typical microcontroller system. It also provides a very low power solution for those designs which are handheld and/or battery operated. As the PSD3XX family grows and evolves, more innovations will be presented in terms of integration and power usage. The new low power PSD3XX family will be introduced soon, providing the designer with an even lower power solution. Until then, use of the techniques described in this note will provide a minimum power solution for your microcontroller system.

Security of Design in the PSD3XX

PSD3XX

By Oudi Moran – WSI

Introduction

The PSD3XX is a family of field programmable and UV erasable microcontroller peripherals that have the ability to interface to virtually any microcontroller without the need for external glue logic.

Any PSD3XX family member is a complete microcontroller peripheral solution with Memory (EPROM, SRAM), Logic, I/O Ports and a Security bit on chip.

In today's competitive business environment, where the cost of the product and its quick introduction to market are the most important factors for success, some companies tend to copy a competitor's design. By doing so, they can save development time which can reduce their engineering cost and eventually reduce the product's price and its introduction time to the market.

This is true mainly for the consumer and commodity product markets where microcontrollers are widely used. The PSD3XX, as the primary microcontroller peripheral, contains all the important code and architectural data that a potential competitor may want to copy.

Since the PSD3XX is a field programmable device, its contents may be read by an I.C. programmer, decompiled and copied by a competitor.

Obviously, it is an undesirable situation for the EPROM, PAD and configuration data of the PSD3XX to fall into the hands of a competitor. To prevent this, the PSD3XX device implements a security "fuse" or programmable bit feature to protect its contents from unauthorized access and use by a competitor.

Uploading the programmed data from EPROM, PAD, ACR and NVM port configuration sections of a secured PSD3XX device is disabled by the security bit (if turned ON). The RAM of the programmer (after trying to upload a secured PSD3XX device) will contain invalid random data.

A secured PSD3XX device will function properly in the system – the microcontroller will be able to access the EPROM, SRAM, PAD and the I/O ports but any attempt to read or verify the contents of a secured PSD3XX by external hardware will fail.

Use of the Security Bit

PSD3XX devices contain non-volatile configuration bits to enable the user to set and configure the device to the proper operational mode. The configuration bits will configure the device to interface successfully with the microcontroller and also configure the PSD3XX I/O Ports. The configuration bits are programmed during the programming phase and cannot be accessed in operational mode.

During programming the configuration bits are programmed as two separate sections:

1) The ACR section of the PSD3XX device contains global configuration bits for proper microcontroller interface. The security bit resides as an individual configuration bit in the ACR section of the device.
2) The NVM section of the PSD3XX device contains port configuration bits for proper set up of Ports A, B and C.

PSD3XX devices use the security bit to prevent unauthorized access to the configuration data inside. Since the security bit is part of the ACR global configuration bits section, it can be programmed in the same manner as all other configuration bits.

All ACR and NVM configuration bits of the PSD3XX are non-volatile, so their contents will not be erased or corrupted during the power down mode of the device (when the PSD3XX is deselected with $\overline{CSI}$/A19 = High) or during power down when V_{CC} is removed.

Security of Design in the PSD3XX

By Oudi Moran – WSI

Use of the Security Bit (Cont.)

The security configuration bit is user programmable and UV erasable as well, so a secured part can be erased completely and be reprogrammed (only if the device is in a windowed package).

Setting the security bit will lock all the contents of the PAD, ACR global configuration bits, and NVM port configuration bits. By setting the security bit the device cannot be entered into Initialization and Override mode (resets the device and enters it to a known default configuration before activating the individual read mode for each section). Any attempt afterwards to enter the device to DIRECT mode for uploading or programming will fail. Setting the security bit prevents a programmer from directly accessing the various sections of the device.

Even though the EPROM, SRAM and I/O port contents are not directly disabled by setting the security bit, it is impossible to read them by using external equipment (except by the microcontroller in the system where the PSD3XX designed in). This is because the external equipment will lack information about the address mapping of the eight EPROM blocks, SRAM and I/O ports in the memory map of the microcontroller and the unknown status of the global and I/O port configuration bits.

Even if an unauthorized user figures out the configuration of the part by knowing what microcontroller is interfaced (ALE polarity, what type of read and write signals, etc.) and gets data out of the PSD3XX (after applying address and control signals to the device), the user will have no idea where it came from: EPROM, SRAM, I/O Port Register, Page Register, etc. This effectively renders the data useless.

Setting the Security Bit

The security configuration bit is called CSECURITY.

If CSECURITY = 0, it means security is off (security bit is not set and its value will be '1' in the object file).

If CSECURITY = 1, it means security is on (security bit is set and its value will be '0' in the object file).

Setting the security bit and activating the security mode can be done in two different ways:

1) By turning security ON in the configuration menu of Maple development software.

2) By setting the security in the programming software (done after the device is fully programmed and verified).

Using Maple development software to turn security ON gives the security bit the value '0', and will integrate it in one of the ACR addresses of the object file created after compilation. (See Security Bit File Location section of this document).

If Setting of the security bit is done in the programming software (Third party programming software or WSI Mappro programming software), the user should program and verify the device using a Maple generated object file (with security option OFF) and then set the security ON by using a separate programming software command.

Some third party programmer manufacturer's software will load the Maple generated object file but mask the security bit before programming the device. In that case the user will have to set the security bit (if necessary) by using a separate command in the programming software menu.

Security of Design in the PSD3XX

PSD3XX

By Oudi Moran – WSI

Security Bit File Location

The object file created by compilation with Maple software is an Intel Intelec format, compatible file.

The programming algorithm defines the address scrambling that translates the file addresses to device addresses (the address that the device "sees" on its address pins during programming). By looking at a screen dump or a hard copy of the object file the user can determine the status of the security bit.

The security bit of the PSD301/311 resides in data bit #1 of file address 81D3h. This address contains three configuration bits that reside in data bits 0 – 2, so this address in the file can have any value between 0 and 7.

If this address has a value X1X (where X can be either 0 or 1), the security bit is off ('1' value means an unprogrammed bit) and CSECURITY = 0 (displayed by Mappro WSI programmer interface software as SECA = 0).

If this address has a value X0X, the security bit is on and CSECURITY = 1 (displayed by Mappro WSI programmer interface software as SECA = 1).

The security bit of PSD302/312 resides in data bit #1 of file address 10253h. This address contains three configuration bits that reside in data bits 0 – 3 (bit 3 is reserved for future usage). This address can have any value between 0 and F. If this address has a value XX1X (where X can be either 0 or 1), the security bit is OFF ('1' value means an unprogrammed bit) and CSECURITY = 0 (displayed by Mappro WSI programmer interface software as SECA = 0). If this address has a value XX0X, the security bit is ON and CSECURITY = 1 (displayed by Mappro WSI programmer interface software as SECA = 1).

If users do not want to look for the security bit status in the object file, they can call MAPPRO programming software from the main menu of MAPLE, Load the RAM with the object file and Display the ACR configuration bits status on the screen.

The value of SECA will indicate the status of the security bit (SECA = 0 means security is OFF, SECA = 1 means security is ON).

Summary

The PSD3XX family of programmable microcontroller peripheral devices provides security of design not readily available in conventional PLDs and EPROMs.

Though not entirely fool-proof, the security bit feature helps make it more cost effective for competitors to design their own hardware instead of trying to copy systems that already exist.

The PSD311 simplifies an eight wire cable tester design and increases flexibility in the process

By Timothy E. Dunavin, Antec – Anixter Mfg. and Karen S. Spesard, WSI

Abstract

With the ever increasing complexity of wiring networks and cables to match a wide variety of computer and telecommunication systems, a means of testing them becomes a necessity. The wire tester design described below is a simple yet effective design which uses the Motorola 68HC11 and WSI PSD311 pair to create a system that insures 8-wire cables are wired properly, and at the same time offers a substantial increase in design flexibility over alternative hardware solutions.

Introduction

More and more microcontroller and microprocessor designers are trying to design integrated core-based systems with the intention of being able to easily configure their systems to fit a wide variety of product applications. The problem is that when these applications require new or changing features such as expanding I/Os or address maps, they may find their designs are not flexible enough to accommodate the new requirements, forcing a lengthy and expensive redesign anyway.

A solution to this problem is to design in user-configurable programmable peripheral products which are flexible enough to accommodate future design revisions without the need for board relayout. The PSD3XX family from WSI, Inc., fits this profile exactly in that the products can be tailored to a specific application and then can be re-configured for other applications using the same core design. Also, the PSD3XX product family can enhance microcontroller-based systems in other ways. For instance, it can improve system integration resulting in lower system costs, and it can significantly shorten time to market resulting in increased revenues and profits.

In the cable tester system in which the PSD311 was used with the 68HC11, the PSD311 integrates address decoding, latches, 32K x 8 EPROM, and 2K x 8 SRAM all into a one-chip user-configurable microcontroller peripheral. It also replaces the two ports lost by the 68HC11 to extend program and data memory outside the MCU with two additional configurable 8-bit I/O ports, and adds a third 3-bit port, while easily enabling still further port expansion .

The Cable Tester System Design

The cable tester described below operates by sending a known bit pattern through the cable under test and checking the bit pattern at the other end. The hardware configuration utilized to achieve this function is shown in Figure 1.

Note that there are very few components overall in the design. The core contains just the 68HC11 microcontroller from Motorola, the PSD311 Programmable Peripheral with Memory from WSI and a few other key components including a keypad, LCD display, and an optional RS232 communications device.

Also note that the interconnections between the 68HC11 and PSD311 are direct and require no "glue logic". That means that no external latches are needed to demultiplex the multiplexed address and data bus from the 68HC11. And, no other external logic is needed to generate the address mapping for the on-board EPROM and SRAM and to select external peripherals, or create the control signal interface. The PSD311 already incorporates these features internally, thereby simplifying the design considerably. In fact, the PSD311's architecture, as shown in Figure 2, specifically includes 32K x 8 mappable EPROM for program

The PSD311 simplifies an eight wire cable tester design and increases flexibility in the process

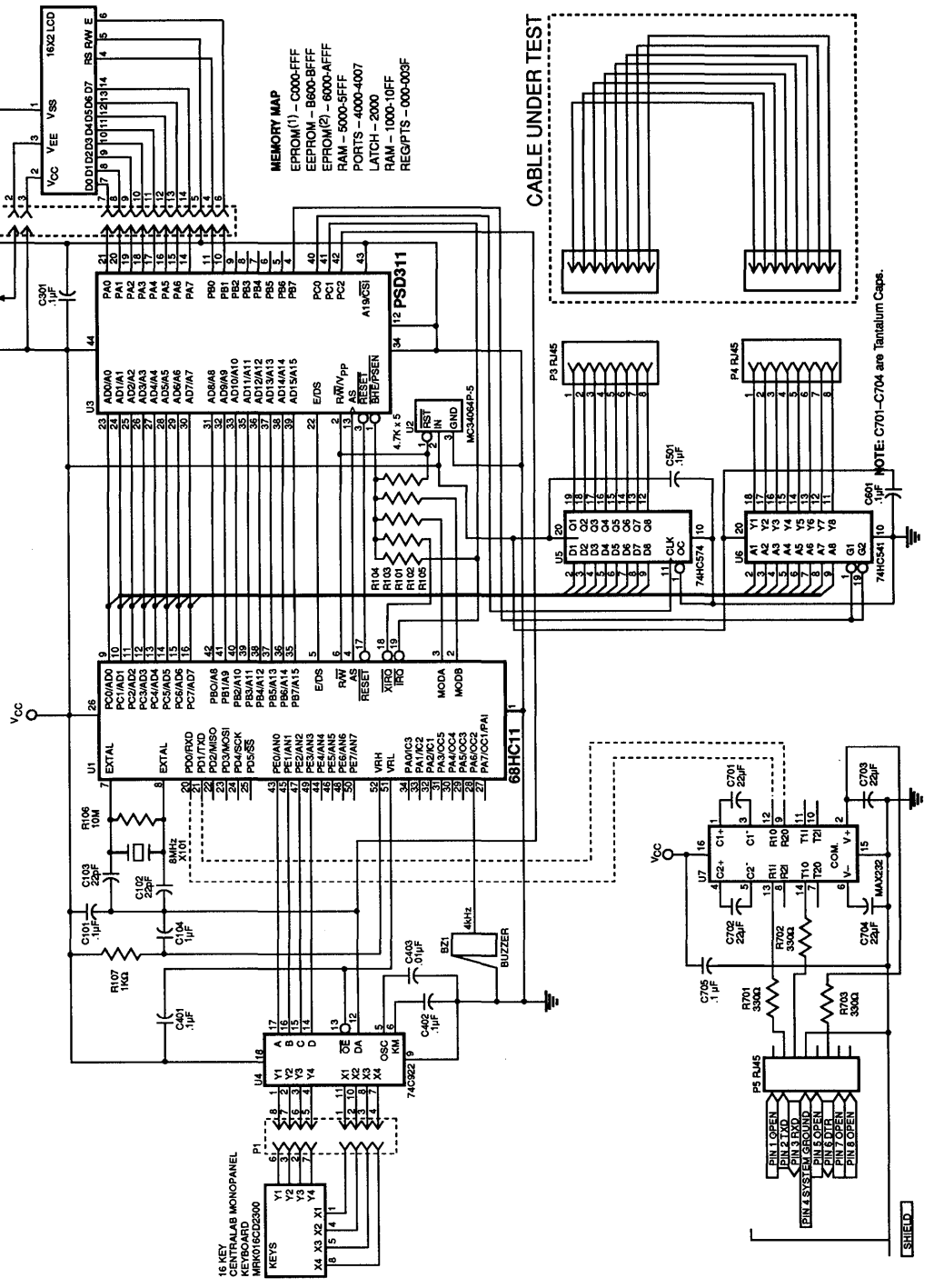
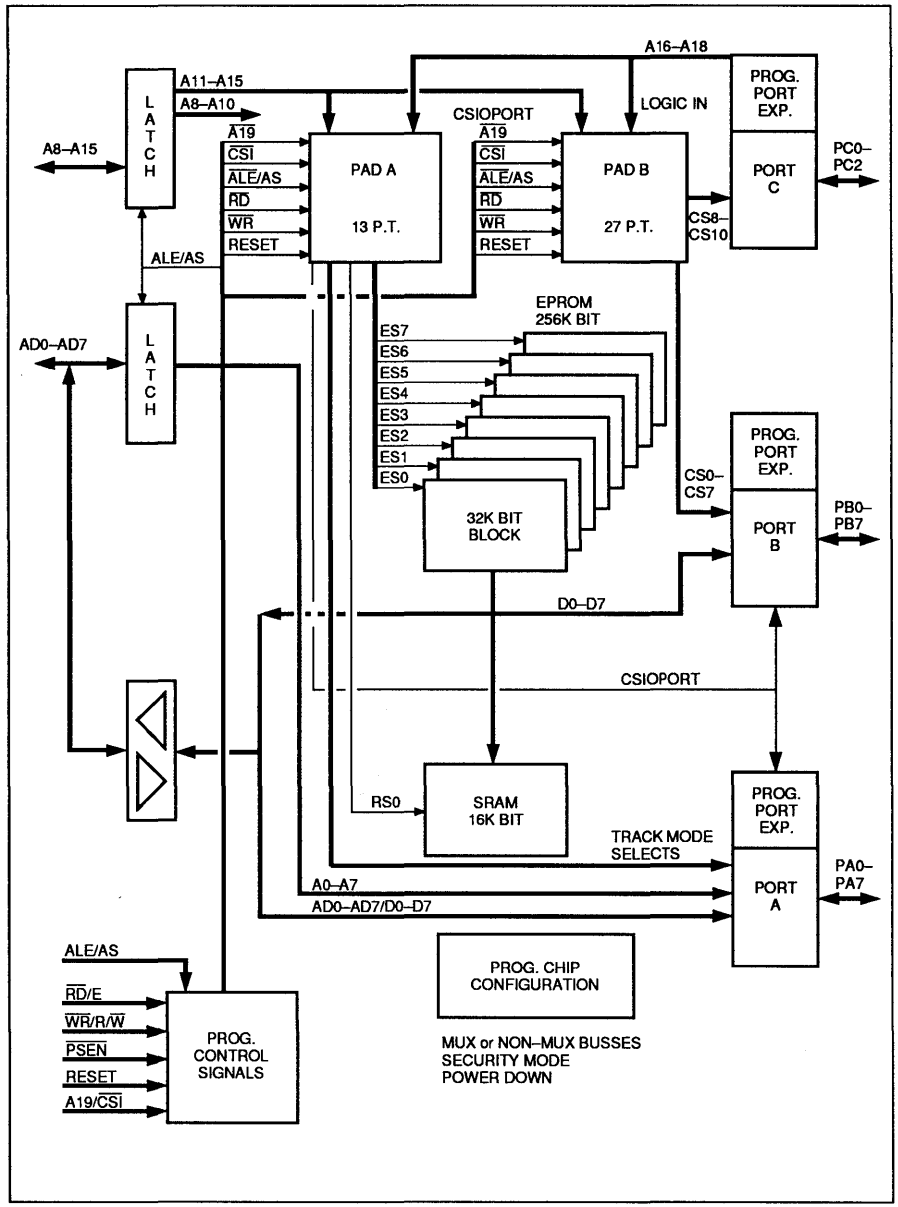


Figure 1. PSD311/68HC11 Implementation in the Cable Tester Design

The PSD311 simplifies an eight wire cable tester design and increases flexibility in the process

Figure 2. PSD311 Architecture



The PSD311 simplifies an eight wire cable tester design and increases flexibility in the process

The Cable Tester System Design (Cont.)

storage, 2K x 8 mappable SRAM for data storage (or 16K x 16 EPROM and 1K x 16 SRAM, if using the similar PSD301 configured to interface to x16 micros) three highly configurable I/O ports, a programmable address decoder, and chip select logic.

In this design, the reconstructed port space of the PSD311 is used to add a keypad and an LCD display to the system, as well as additional output control and input lines with an 8-bit latch and an 8-bit buffer/line driver. Besides these components, the completed cable tester design also includes an undervoltage sensing circuit for generating a reset signal and an encoder for interfacing to the keypad.

Interfacing To The PSD311

Not only does the PSD311 interface to the 68HC11 simply and directly because of its internal latches and programmable control signals – as it does with any 8-bit microcontroller – it also facilitates easy interfacing to other components. (The PSD301 interfaces to any 8-or 16-bit microcontroller.) This is possible because of its three I/O ports and the Programmable Address Decoder (PAD) which offer unsurpassed flexibility. The PAD block diagram is shown in Figure 3.

For instance, the no "glue-logic" interface of the keypad in the system is accomplished by using a 74C922 encoder in conjunction with the PAD section of the PSD311. The PAD is useful because the Data Available (DA) line of the 74C922 is a logic "1" when a key is pressed, and the signal must be inverted before it reaches the /IRQ input of the 68HC11. Connecting the encoder's DA line to the PSD311's PC2 pin and configuring it to be a general-purpose logic input enables the signal to be inverted inside the PAD. The inverted signal is then "outputed" on PC1 which is configured as a chip select and routed to /IRQ. (See Port C Configuration and Chip Select Equation in Appendix A.) This simple internal manipulation inside the PSD311 helps reduce the number of components in the system. By connecting the 74C922 outputs directly to PE0-PE3 on the 68HC11, reading of the data is straightforward.

The display used in the system is a 16 character by 2 line dot matrix LCD module. The interface to the LCD display is handled by mapping the data bus directly to Port A of the PSD311, which is configured pin-by-pin to be general-purpose I/O. The control logic for the LCD is handled through two pins on Port B: PB0 and PB1, which are also configured to be general-purpose I/O. (See Ports A and B Configuration in Appendix A.) With the display used as a "WOM" (Write Only Memory), its R/$\overline{W}$ line is tied to ground to free an I/O pin of the PSD311 for other purposes. To free up Port A completely on the PSD311, an alternative approach would have been to connect the LCD directly to the 68HC11.

To expand the I/O capabilities of the system further, two port pins from the PSD311 are used with a 74HC574 and a 74HC541 to create 8 additional inputs and 8 additional latched outputs, both at the same address. (This is shown in Figure 1.) The PSD311's chip select outputs from ports B and C are derived from the addresses, DS strobe, and R/$\overline{W}$ signal available as inputs into the PAD. These chip selects will enable data to be latched to the outputs or enable input data onto the extended address/data bus from the outside world, imitating the capability of a PIA.

The chip select equation for the output latch, 74HC574, is decoded from the upper address byte, the DS/E signal, and the active low R/$\overline{W}$ signal as follows:

/CS8 = /A15 • /A14 • A13 • /A12 • DS • /R/$\overline{W}$.

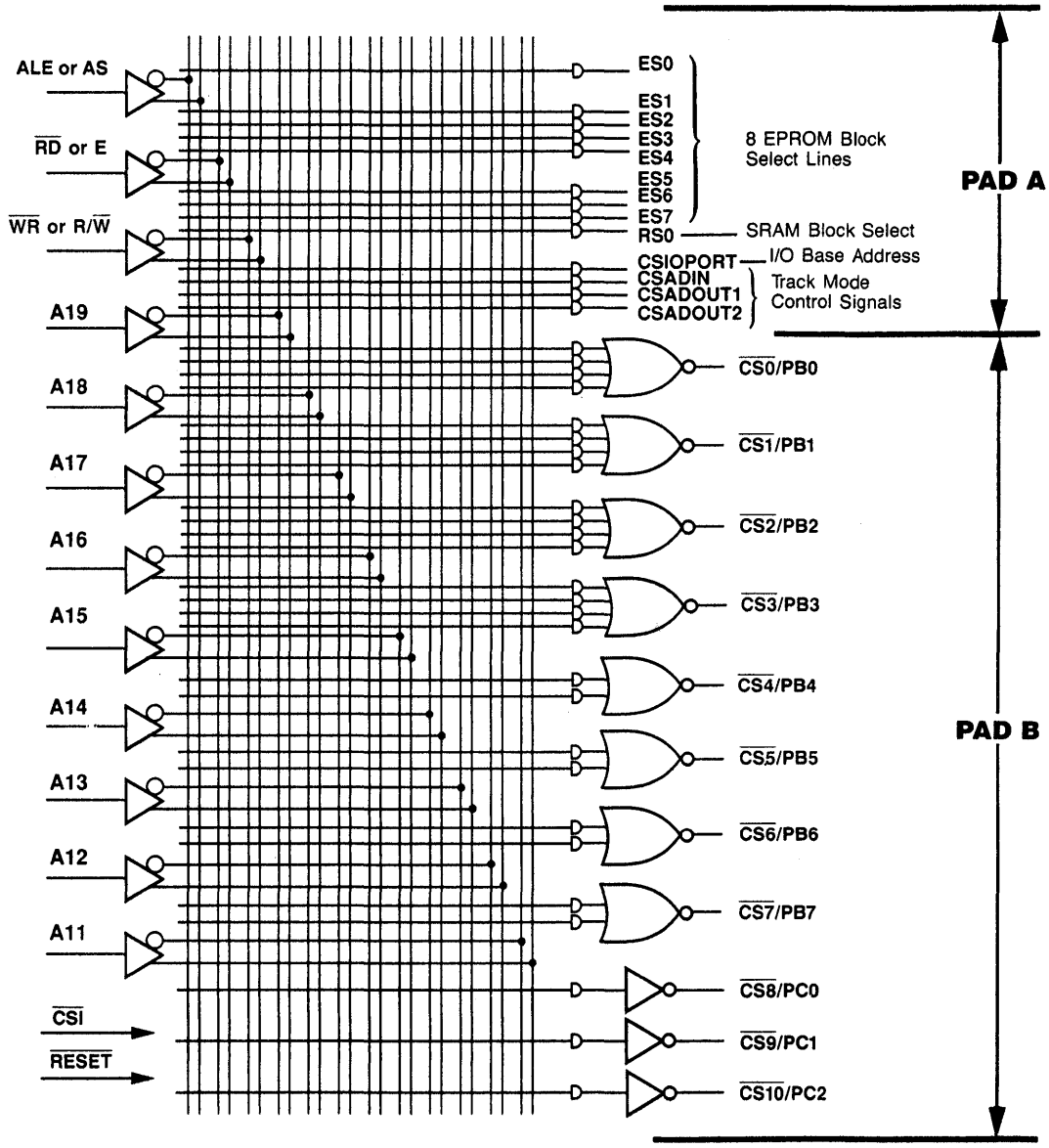
The resulting latched address is $2000H with DS = 1 and R/$\overline{W}$ = 0. The chip select equation for the input driver, 74HC541, is the same, because the address is the same ($2000H), except that R/$\overline{W}$ is active high. So, this equation becomes:

/CS9 = /A15 • /A14 • A13 • /A12 • DS • R/$\overline{W}$.

The PSD311 simplifies the interface to the program and data memory, external peripherals, and I/O ports in the system by integrating the address decoder internally. This is illustrated with the direct interconnection between the microcontroller and other peripherals and the PSD311, without the need for a PLD or other logic.

The PSD311 simplifies an eight wire cable tester design and increases flexibility in the process

Figure 3. Programmable Address Decoder Block Diagram



The PSD311 simplifies an eight wire cable tester design and increases flexibility in the process

Interfacing To The PSD311 (Cont.)

The PAD enables the 8 blocks of 4K bytes EPROM (256K bits) to be located anywhere within the available address space – in this case, the address space of the 68HC11 is 64K bytes. So, the EPROM memory is split into two segments of 16K bytes EPROM each, separated by the 512 bytes of the internal E2PROM on the 68HC11. This means that the first 4 EPROM blocks are mapped contiguously, as well as the last 4 EPROM blocks. Here,the program memory (6000H-9FFFH: EPROM2, and C000H-FFFFH: EPROM1) is allocated to the upper portion of address space.

The data or SRAM memory, on the other hand, is allocated to the lower portion of address space and is partitioned into two segments: one segment containing the SRAM internal to the 68HC11 (256 bytes) and the other containing the SRAM internal to the PSD311 (2K bytes). The SRAM in the PSD311 is mapped via the address decoder to location 5000H-5FFFH, respectively.

Data direction and data registers of the PSD311's two ports are paired and accessed via an offset from a configurable I/O port mapped base address, such as 4000H in this cable tester design. This enables 16-bit data instructions to access the two I/O ports together, which in turn reduces both the Load and Store times during program execution.

Benefits of the PSD311 Usage In System

Board layout of the cable tester design was greatly simplified with the PSD311. In fact, when pin 1 of the PSD311 is oriented 180 degrees from pin 1 of the 68HC11 in the PLCC package, port B of the 68HC11 is directly across from the AD8-AD15 pins of the PSD311. This positioning enables close layout of the two parts, greatly reducing costs due to less board space.

Additional space is saved by using the latch and buffer for general-purpose I/O instead of the larger and more expensive PIA. And other I/O port lines are not sacrificed by using the multiplexed address/data bus instead of the Serial Peripheral Interface of the 68HC11.

In fact, board space is estimated to have been reduced by more than 50% over the alternative cumbersome design because of the PSD311 positioning on the PC board, its port expansion capabilities, and of course, the number of parts it replaces: including a 256K EPROM, a 16K SRAM, a latch, a decoder, and other miscellaneous CMOS logic.

A benefit of parts reduction is lower CMOS power consumption that results from an integrated single-chip CMOS peripheral/ memory solution. By analyzing the power that would have been consumed with the alternative design and comparing that against the PSD311 solution, it was found that power was reduced by at least 30%. This translates into requiring a smaller power supply and a further reduction in cost.

The flexibility of the PSD311 in the cable tester design is also an advantage when design changes need to be made quickly. Since the I/O ports, PAD, control signals, and EPROM are all programmable, the part just needs to be reprogrammed when the configuration or program memory for the entire system needs modifying.

For instance, the current system has ten I/O, eleven input, and eleven output lines remaining. This can change if other variables need to be stored or other peripherals need to be accessed. To avoid relaying out another board to accommodate these changes, the PSD311 may be able to be reconfigured to easily handle them. Also, if more features and/or capabilities in EPROM are required, the PSD312 and PSD313 with 512Kbits (64K x 8) and 1Mbits (128K x 8) EPROM, respectively, are available in the same package and pinout.

The PSD311 also provides additional SRAM beyond the limited amount that may be on the microcontroller being used.
This provides obvious benefits including more scratchpad RAM for such uses as storing cable "signatures" and system tests that can be downloaded for diagnostic purposes.

The PSD311 simplifies an eight wire cable tester design and increases flexibility in the process

Benefits of the PSD311 Usage In System (Cont.)

But other benefits not readily seen are also important. For product designs that have a short life cycle and are "pushed" to go to market quickly, the additional SRAM gives the designer the option of writing the code in a high-level language such as "C", without the worry of running out of variable storage space. The capability of writing software in "C" could speed up the software development cycle, thereby reducing time-to-market!

Configuring and Programming the PSD311

All of the control logic, address mapping, and port configurations for the PSD311 are handled during device configuration as part of WSI's easy-to-use, menu-driven PSD MAPLE software program, which is included in the PSD-SILVER or PSD-GOLD software development package. See Appendix A for the PSD311 configuration used in this application.

After the configuration for the PSD311 has been determined and "Save"d, the hex file that is needed for programming the PSD311 is created. That is done during "Compile". "Compile" reads the code written for the microcontroller (in Intel hex format) and concatenates or merges it with the PSD311 configuration data to produce the desired output file for downloading to a programmer for programming.

That is all there is to programming the PSD311 which is now supported on industry-standard programmers like the Data I/O, BP Microsystems, Bytek, and Logical Devices programmers as well as the low-cost WSI MagicPro programmer.

The 68HC11/ PSD311 System Software

The software for the 68HC11 was written with a word processor and assembled using a cross assembler. A portion of the cable tester design code which is programmed into the PSD311 is listed in Appendix B. Here the register and RAM memory locations are set up within the first 64 clock cycles from reset of the 68HC11 and located at 0000H to enable easy Direct Addressing and Bit manipulations of often used registers.

Initialization of the Option Register, Timer prescaler, Stack and Serial Communications Interface complete the basic set up for the 68HC11 operation. Other initialization operations include: Ports A and B of the PSD311 which are set up as outputs for display control and data transfer operations, and the LCD display which is set up to display the first screen. Final initialization is achieved by setting several internal registers and clearing any pending interrupts. Now, the IRQ mask bit can be cleared and the main program loop entered.

Included in the code is a demonstration of some useful routines which will illustrate how to easily work with the Latch and Buffer expansion from the 68HC11/ PSD311. Remember that these extended addresses off the 68HC11 can be accessed in several ways. The example code shown uses the Bit Set and Bit Clear instructions in the indexed addressing mode. With these Bit Set and Bit Clear instructions, which are read-modify-write instructions, an additional register should be set up in the internal RAM, not on the latched (write-only) address, so the instructions will function properly. Data can then be manipulated and stored as a complete byte to the latch enabling data to be read and the current value in the latch to be checked. (Bit manipulation on the latched addresses using the indexed addressing mode will result in a correct bit change. However, the rest of the byte will be unusable as data on the bus will be scrambled at the rising edge of the chip select signal.) The latch and buffer expansion keeps software algorithms simple.

The PSD311 simplifies an eight wire cable tester design and increases flexibility in the process

The 68HC11/ PSD311 System Software (Cont.)

Regarding the software for the keypad, no debounce software is necessary because the 74C922 has a built in debounce circuit. Actually, direct access from Port E to the keypad data and the AND instruction allows easy compare and execution of the correct routine.

The remaining subroutines in the program are straightforward and basic to most microcontrollers and microprocessors. Those used by the 68HC11 are found in previously published handbooks and articles which can be obtained through your local Motorola sales office.

Putting the System to Work

The 68HC11/PSD311 cable tester design could be expanded very easily with software to learn many different wiring configurations and to check several cables against a good one. Its usefulness can also be increased by making it battery operated for field use because of the low current draw of the tester.

The cable tester, as designed, will display the test results and step through the program to show the pin by pin connections of the cable. Results are then stored and later fed into a computer through the RS232 communications port of the tester.

Summary

Requirements for microcontroller-based designs are continually changing and to be able to adapt to these changes means being flexible. Of course, flexibility in hardware is sometimes hard to achieve, while flexibility in software is mostly a given. One of the goals of the PSD3XX family of products is to bridge the gap in flexibility between hardware and software.

By that, it is meant that hardware will not be a gating item when developing a new design that needs to be introduced to market quickly. And the PSD311, as illustrated in this cable tester design, addresses that issue perfectly by providing a user-configurable peripheral solution for hardware designers. So, if an application is modified and the I/O configuration changes, or design fixes are required, the P.C. board does not have to be re-engineered. The PSD3XX can just be reprogrammed to reflect the new changes.

The flexibility provided by the PSD311 solution in this design is crucial in that it enabled development to be completed quickly and successfully using a "core" approach which can handle many different cable applications, including applications for telephone interconnections, printers, and local area networks.

The PSD311 simplifies an eight wire cable tester design and increases flexibility in the process

Appendix A. PSD311 Part Configuration Listed In .SV1 File

```
                              ALIASES
A16/CS8  = CS8
A17/CS9  = IRQ
A18/CS10 = DA
A19/CSI  = CSI
************************************************************************
                     GLOBAL CONFIGURATION
Address/Data Mode:                                    MX
Data Bus Size:                                        8
CSI/A19:                                              CSI
Reset Polarity:                                       LO
ALE Polarity:                                         HI
WRD/RWE:                                              RWE
A16-A19 Transparent or Latched by ALE:                T
Using different READ strobes for SRAM and EPROM: N
************************************************************************
              PORT A CONFIGURATION (Address/IO)

 Bit No.      Ai/IO.      CMOS/OD.
    0          IO          CMOS
    1          IO          CMOS
    2          IO          CMOS
    3          IO          CMOS
    4          IO          CMOS
    5          IO          CMOS
    6          IO          CMOS
    7          IO          CMOS
************************************************************************
                  PORT B CONFIGURATION

 Bit No.      CS/IO.      CMOS/OD.
    0          IO          CMOS
    1          IO          CMOS
    2          IO          CMOS
    3          IO          CMOS
    4          IO          CMOS
    5          IO          CMOS
    6          IO          CMOS
    7          CS7         CMOS

                  CHIP SELECT EQUATIONS

/CS7 = /A15 * /A14 * A13 * /A12 *  E  *  R/W
   +
************************************************************************
                  PORT C CONFIGURATION

 Bit No.      CS/Ai.
    0          CS8
    1          CS9
    2          A18

                  CHIP SELECT EQUATIONS

/CS8 = /A15 * /A14 * A13 * /A12 *  E  * / R/W
/IRQ = DA
************************************************************************
                     ADDRESS  MAP

      A  A  A  A  A  A  A  A  A  SEGMT   SEGMT  EPROM    EPROM   File Name
     19 18 17 16 15 14 13 12 11  STRT    STOP   START    STOP
ES0   N  X  N  N  0  1  1  0  N  6000    6FFF   6000     6fff    BASE301.OBJ
ES1   N  X  N  N  0  1  1  1  N  7000    7FFF
```

The PSD311 simplifies an eight wire cable tester design and increases flexibility in the process

Appendix A. PSD311 Part Configuration Listed in .SV1 File (Cont.)

```
ES2   N  X  N  N  1  0  0  0  N  8000    8FFF

ES3   N  X  N  N  1  0  0  1  N  9000    9FFF

ES4   N  X  N  N  1  1  0  0  N  C000    CFFF   c000     cfff     BASE301.OBJ
ES5   N  X  N  N  1  1  0  1  N  D000    DFFF   d000     dfff     BASE301.OBJ
ES6   N  X  N  N  1  1  1  0  N  E000    EFFF   e000     efff     BASE301.OBJ
ES7   N  X  N  N  1  1  1  1  N  F000    FFFF   f000     ffff     BASE301.OBJ
RS0   N  X  N  N  0  1  0  1  0  5000    57FF

CSP   N  X  N  N  0  1  0  0  0  4000    47FF
****************************** END ***********************************
CDATA        = 0
CADDRDAT     = 1
CRRWR        = 1
CA19/(/CSI)  = 0
CALE         = 0
CRESET       = 0
COMB/SEP     = 0
CADDHLT      = 0

CPAF2        = 0

CPAF1 [0] = 0
CPAF1 [1] = 0
CPAF1 [2] = 0
CPAF1 [3] = 0
CPAF1 [4] = 0
CPAF1 [5] = 0
CPAF1 [6] = 0
CPAF1 [7] = 0

CPACOD [0] = 0
CPACOD [1] = 0
CPACOD [2] = 0
CPACOD [3] = 0
CPACOD [4] = 0
CPACOD [5] = 0
CPACOD [6] = 0
CPACOD [7] = 0

CPBF [0] = 1
CPBF [1] = 1
CPBF [2] = 1
CPBF [3] = 1
CPBF [4] = 1
CPBF [5] = 1
CPBF [6] = 1
CPBF [7] = 0

CPBCOD [0] = 0
CPBCOD [1] = 0
CPBCOD [2] = 0
CPBCOD [3] = 0
CPBCOD [4] = 0
CPBCOD [5] = 0
CPBCOD [6] = 0
CPBCOD [7] = 0

CPCF [0] = 1
CPCF [1] = 1
CPCF [2] = 0
```

The PSD311 simplifies an eight wire cable tester design and increases flexibility in the process

Appendix B. Core System Software for Cable Tester Design

```
0000                    CPU     "6811.TBL"
0000                    HOF     "INT8"
                ;
                ;*************************************************************
                ;*      THE 68HC11 IN CONJUNCTION WITH THE PSD301            *
                ;*      ARE USED IN DEVELOPEMENT OF SOFTWARE FOR             *
                ;*      DISPLAY, KEYBOARD FUNCTION, AND OTHER APPL.          *
                ;*      MEMORY MAP:EPROM(1)   C000-FFFF (PROGRAM)            *
                ;*                 EEPROM     B600-BFFF (68HC11)             *
                ;*                 EPROM(2)   6000-9FFF (DATA)               *
                ;*                 RAM        5000-5FFF (PSD301)             *
                ;*                 I/O        4000-4007 (PSD301)             *
                ;*                 LAT        2000      (LATCH & BUFFER)     *
                ;*                 RAM        1000-10FF (68HC11)             *
                ;*                 I/O & REG  0000-003F (68HC11)             *
                ;*                                                           *
                ;*                    BY TIM DUNAVIN                         *
                ;*                      ANTEC                                *
                ;*                  ANIXTER MANUFACTURING                    *
                ;*************************************************************
                ;
6000                    ORG     06000H      ;DATA MEMORY
                ;
                ;***********************
                ;*    LOOKUP TABLES    *
                ;***********************
                ;
6000 3638484331DATTAB:  DFB     "68HC11/PSD311 UP",00H
                ;
6011 54494D4F54CREDITS: DFB     "TIMOTHY E. DUNAVIN"
6023 414E544543         DFB     "ANTEC - ANIXTER MFG."
6037 524F434B20         DFB     "ROCK FALLS, ILL. 61071"
                ;
                ;*************************************************************
                ;
C000                    ORG     0C000H      ;PROGRAM MEMORY
                ;
103D =          INIT:   EQU     103DH       ;RAM AND I/O MAPPING REGISTER
4000 =          PORTBC: EQU     04000H      ;I/O BASE ADDRESS OF THE 301
2000 =          LAT:    EQU     02000H      ;LATCH AND BUFFER
0000 =          KEY1:   EQU     00H         ;KEYPAD 1
0001 =          KEY2:   EQU     01H         ;KEYPAD 2
0002 =          KEY3:   EQU     02H         ;KEYPAD 3
0003 =          KEYA:   EQU     03H         ;KEYPAD A
0004 =          KEY4:   EQU     04H         ;KEYPAD 4
0005 =          KEY5:   EQU     05H         ;KEYPAD 5
0006 =          KEY6:   EQU     06H         ;KEYPAD 6
0007 =          KEYB:   EQU     07H         ;KEYPAD B
0008 =          KEY7:   EQU     08H         ;KEYPAD 7
0009 =          KEY8:   EQU     09H         ;KEYPAD 8
000A =          KEY9:   EQU     0AH         ;KEYPAD 9
000B =          KEYC:   EQU     0BH         ;KEYPAD C
000C =          KEYZ:   EQU     0CH         ;KEYPAD *
000D =          KEY0:   EQU     0DH         ;KEYPAD 0
000E =          KEYY:   EQU     0EH         ;KEYPAD #
000F =          KEYD:   EQU     0FH         ;KEYPAD D
                ;
```

The PSD311 simplifies an eight wire cable tester design and increases flexibility in the process

Appendix B. Core System Software for Cable Tester Design (Cont.)

```
                ;***********************************************
                ;*       INITIALIZATION ROUTINE                *
                ;***********************************************
                ;
                ;NOTE: OPTION and TMSK2 must be programed in first 64 E
                ;      cycles out of RESET
                ;
C000 0F         START:   SEI                  ;SET IRQ MASK
C001 8610                LDAA    #010H        ;SET RAM AT 1000 AND
C003 B7103D              STAA    INIT         ;SET REGISTERS AT 0000
                ;***********************************************
                ;
                ;******* 64 BYTES OF REGISTER AREA *******
0000 =          PORTA:   EQU     0000H        ;PORT A DATA REGISTER
                ;          .                  ;0001 IS RESERVED
0002 =          PIOC:    EQU     0002H        ;PARALLEL I/O CONTROL REGISTER
0003 =          PORTC:   EQU     0003H        ;PORT C DATA REGISTER (AD0 - AD7)
0004 =          PORTB:   EQU     0004H        ;PORT B DATA REGISTER (A8 - A15)
0005 =          PORTCL:  EQU     0005H        ;PORT C LATCHED DATA REGISTER
                                              ;0006 IS RESERVED
0007 =          DDRC:    EQU     0007H        ;DATA DIRECTION REG FOR PORT C
0008 =          PORTD:   EQU     0008H        ;PORT D DATA REGISTER (RxD, TxD, AND I/O)
0009 =          DDRD:    EQU     0009H        ;DATA DIRECTION REG FOR PORT D
000A =          PORTE:   EQU     000AH        ;PORT E DATA REGISTER
000B =          CFORC:   EQU     000BH        ;TIMER COMPARE FORCE REGISTER
000C =          OC1M:    EQU     000CH        ;OUTPUT COMPARE 1 MASK REGISTER
000D =          OC1D:    EQU     000DH        ;OUTPUT COMPARE 1 DATA REGISTER
000E =          TCNT:    EQU     000EH        ;TIMER COUNTER REGISTER (16 BIT)
                                              ;000F LSB TCNT
0010 =          TIC1:    EQU     0010H        ;TIMER INPUT CAPTURE REGISTER 1 (16 BIT)
                                              ;0011 LSB TIC1
0012 =          TIC2:    EQU     0012H        ;TIMER INPUT CAPTURE REGISTER 2 (16 BIT)
                                              ;0013 LSB TIC2
0014 =          TIC3:    EQU     0014H        ;TIMER INPUT CAPTURE REGISTER 3 (16 BIT)
                                              ;0015 LSB TIC3
0016 =          TOC1:    EQU     0016H        ;TIMER OUTPUT COMPARE REG 1 (16 BIT)
                                              ;0017 LSB TOC1
0018 =          TOC2:    EQU     0018H        ;TIMER OUTPUT COMPARE REG 2 (16 BIT)
                                              ;0019 LSB TOC2
001A =          TOC3:    EQU     001AH        ;TIMER OUTPUT COMPARE REG 3 (16 BIT)
                                              ;001B LSB TOC3
001C =          TOC4:    EQU     001CH        ;TIMER OUTPUT COMPARE REG 4 (16 BIT)
                                              ;001D LSB TOC4
001E =          TOC5:    EQU     001EH        ;TIMER OUTPUT COMPARE REG 5 / INPUT CAPTURE
                                              ;REGISTER 4 (16 BIT) -  001F LSB TOC5/TIC4
0020 =          TCTL1:   EQU     0020H        ;TIMER CONTROL REGISTER 1
0021 =          TCTL2:   EQU     0021H        ;TIMER CONTROL REGISTER 2
0022 =          TMSK1:   EQU     0022H        ;MAIN TIMER INT MASK REGISTER 1
0023 =          TFLG1:   EQU     0023H        ;MAIN TIMER INT. FLAG REG 1
0024 =          TMSK2:   EQU     0024H        ;MAIN TIMER INT MASK REGISTER 2
0025 =          TFLG2:   EQU     0025H        ;MAIN TIMER INT. FLAG REG 2
0026 =          PACTL:   EQU     0026H        ;PULSE ACCUMULATOR CONTROL REG
0027 =          PACNT:   EQU     0027H        ;PULSE ACCUMULATOR COUNT REG
0028 =          SPCR:    EQU     0028H        ;SPI CONTROL REGISTER
0029 =          SPSR:    EQU     0029H        ;SPI STATUS REGISTER
002A =          SPDR:    EQU     002AH        ;SPI DATA REGISTER
002B =          BAUD:    EQU     002BH        ;SCI BAUD RATE CONTROL REGISTER
002C =          SCCR1:   EQU     002CH        ;SCI CONTROL REGISTER 1
002D =          SCCR2:   EQU     002DH        ;SCI CONTROL REGISTER 2
002E =          SCSR:    EQU     002EH        ;SCI STATUS REGISTER
002F =          SCDR:    EQU     002FH        ;SCI DATA REGISTER
```

The PSD311 simplifies an eight wire cable tester design and increases flexibility in the process

Appendix B. Core System Software for Cable Tester Design (Cont.)

```
0030 =          ADCTL:   EQU     0030H       ;A/D CONTROL/STATUS REGISTER
0031 =          ADR1:    EQU     0031H       ;A/D RESULT REGISTER 1
0032 =          ADR2:    EQU     0032H       ;A/D RESULT REGISTER 2
0033 =          ADR3:    EQU     0033H       ;A/D RESULT REGISTER 3
0034 =          ADR4:    EQU     0034H       ;A/D RESULT REGISTER 4
                                             ;0035 - 0038 RESERVED
0039 =          OPTION:  EQU     0039H       ;SYSTEM CONFIGURATION OPTIONS
003A =          COPRST:  EQU     003AH       ;ARM/RESET COP TIMER CIRCUITRY
003B =          PPROG:   EQU     003BH       ;EEPROM PROGRAMMING REGISTER
003C =          HPRIO:   EQU     003CH       ;HIGHEST PRIORITY INTERRUPT
                ;INIT:   EQU     003DH       ;RAM AND I/O MAPPING REGISTER (NEW ADD.)
003E =          TEST1:   EQU     003EH       ;FACTORY TEST REGISTER
003F =          CONFIG:  EQU     003FH       ;CONFIGURATION CONTROL REGISTER
                ;
                ;******* 256 BYTES OF INTERNAL RAM *******
1000 =          FLAGS:   EQU     1000H       ;FLAG REGISTER
1001 =          LA1:     EQU     1001H       ;LATCH DATA REGISTER
1002 =          STOR:    EQU     1002H       ;BASIC RAM STORAGE AREA
10FF =          STACK:   EQU     10FFH       ;STACK AREA
                ;
                ;******* 2K X 8 EXTERNAL RAM ********
5000 =          MASSTOR: EQU     05000H      ;MASS STORAGE RAM IN PSD301
                ;
                ;******* EEROM AREA, 512 BYTES *******
B600 =          EROM:    EQU     0B600H      ;DATA RETENTION AREA
                ;
                ;***********************************************
C006 01                  NOP                 ;SLIGHT DELAY TO ALLOW REGISTER SET UP
C007 86E3                LDAA    #0E3H       ;SET UP OPTION REG. - ADPU =1, CSEL = 1,
                                              IRQE = 1
C009 9739                STAA    OPTION      ;(ENABLE EEPROM CHARGE PUMP, IRQ EDGE
                                              SENSITIVE)
C00B 8602                LDAA    #002H       ;SET TIMER PRESCALER TO 8
C00D 9724                STAA    TMSK2       ;AND DISABLE TIMER INTERRUPTS
C00F 7F0028              CLR     SPCR        ;DISABLE ALL SPI INT.
C012 8E10FF              LDS     #STACK      ;SET UP STACK
C015 8680                LDAA    #080H
C017 9726                STAA    PACTL       ;PA7 OUTPUT
                ;******* INITIALIZE THE SCI TO 9600 BAUD AT 8MHZ (DISABLED)
C019 86FC       ONSCI:   LDAA    #0FCH       ;INIT. PORT D DDR (02H)
C01B 9709                STAA    DDRD        ;PD0, PD1 - INPUT, PD2-PD5 - OUTPUT
C01D 8600                LDAA    #000H       ;SET UP PORT D
C01F 9708                STAA    PORTD
C021 7F002C              CLR     SCCR1       ;SET UP SER. COM. CON. REG. 1
C024 7F002D              CLR     SCCR2
C027 962E                LDAA    SCSR        ;TO CLEAR TDRE AND TC OF SCSR
C029 4F                  CLRA                ;READ STATUS REG., LOAD TRANS. DATA REG.
C02A 972F                STAA    SCDR
                ;******* INITIALIZE THE 301 FOR DISPLAY INTERFACE
C02C CEFFFF     ONPIA:   LDX     #0FFFFH     ;SET UP PORTS B & C AS OUTPUTS
C02F FF4004              STX     PORTBC+4
                ;******* DISPLAY SET UP (NEW REV. 15 MAY 91) *******
C032 CE2710     DISINIT: LDX     #02710H     ;100mS DELAY (POWER UP DELAY FOR DISPLAY)
C035 BDC0E1              JSR     TDELAY      ;TIME DELAY
C038 8630                LDAA    #030H       ;SET UP DISPLAY
C03A BDC0F4              JSR     SENDI       ;SEND INSTRUCTION (30 1ST TIME)
C03D CE0300              LDX     #00300H     ;6.1mS DELAY
```

The PSD311 simplifies an eight wire cable tester design and increases flexibility in the process

Appendix B. Core System Software for Cable Tester Design (Cont.)

```
C040 BDC0E1            JSR     TDELAY        ;TIME DELAY
C043 BDC0F4            JSR     SENDI         ;SEND INSTRUCTION (30 2ND TIME)
C046 BDC0DE            JSR     TD40          ;TIME DELAY
C049 BDC0F4            JSR     SENDI         ;SEND INSTRUCTION (30 3RD TIME)
C04C BDC0DE            JSR     TD40          ;TIME DELAY
C04F 8638              LDAA    #038H         ;FUNCTION SET (8 BIT-SINGLE LINE)
C051 BDC0F4            JSR     SENDI         ;SEND INSTRUCTION
C054 CE0280            LDX     #00280H       ;5mS DELAY
C057 BDC0E1            JSR     TDELAY        ;TIME DELAY
C05A 860C              LDAA    #00CH         ;DISPLAY ON - NO CURSOR
C05C BDC0F4            JSR     SENDI         ;SEND INSTRUCTION
C05F CE0280            LDX     #00280H       ;5mS DELAY
C062 BDC0E1            JSR     TDELAY        ;TIME DELAY
C065 8606              LDAA    #006H         ;ENTRY MODE SET
C067 BDC0F4            JSR     SENDI         ;SEND INSTRUCTION
C06A CE0280            LDX     #00280H       ;5mS DELAY
C06D BDC0E1            JSR     TDELAY        ;TIME DELAY
C070 BDC0EC            JSR     HOME          ;DISPLAY CURSOR HOME!
C073 CE0190            LDX     #00190H       ;4.0mS DELAY
C076 BDC0E1            JSR     TDELAY        ;TIME DELAY
C079 18CE6000          LDY     #DATTAB       ;TOP OF DATA TABLE
C07D BDC0CC            JSR     PDOD          ;SEND MESSAGE TO DISPLAY
                ;******* FINAL INIT. *******
C080 9629       FINIT: LDAA    SPSR          ;CLEAR ANY SPI INT.
C082 962A              LDAA    SPDR
C084 86FF              LDAA    #0FFH         ;CLEAR ANY TIMER INT.
C086 9723              STAA    TFLG1
C088 9725              STAA    TFLG2
C08A 962E              LDAA    SCSR          ;CLEAR ANY SCI INT.
C08C 962F              LDAA    SCDR
                ;
                ;EXAMPLES OF WORKING WITH LATCH AND BUFFER
C08E 7F2000            CLR     LAT           ;CLEAR LATCH
C091 CE1001            LDX     #LA1          ;SET INDEX
C094 1C0200            BSET    2,X,00H       ;SET BIT 2 OF LA1
C097 A600              LDAA    0,X           ;GET LATCH REGISTER
C099 B72000            STAA    LAT           ;STORE DATA TO LATCH
C09C B62000            LDAA    LAT           ;GET DATA FROM BUFFER
                ;
C09F BDC0B0            JSR     BEEP          ;SOUND OFF!
                ;
C0A2 0E                CLI                   ;CLEAR IRQ MASK
                ;
                ;*************************
                ;*       MAIN LOOP       *
                ;*************************
                ;
C0A3 01         LOOP:  NOP
C0A4 7EC0A3            JMP     LOOP          ;RETURN
                ;
                ;***********************************
                ;*       SUBROUTINES                *
                ;***********************************
                ;
                ;******* WATCHDOG SERVICE ROUTINE ******
C0A7 8655       DOG:   LDAA    #055H         ;RESET WATCHDOG TIMER
C0A9 973A              STAA    COPRST
C0AB 86AA              LDAA    #0AAH
C0AD 973A              STAA    COPRST
C0AF 39                RTS                   ;RETURN FROM SUB.
```

Appendix B. Core System Software for Cable Tester Design (Cont.)

```
                        ;
                        ;******* HOOTER OSC. ROUTINE ********
C0B0 18CE01FF   BEEP:   LDY     #001FFH     ;SET COUNT
C0B4 8640       BEEP1:  LDAA    #040H       ;BEEPER ON
C0B6 9700               STAA    PORTA
C0B8 CE0014             LDX     #00014H
C0BB BDC0E1             JSR     TDELAY      ;DELAY
C0BE 4F                 CLRA                ;BEEPER OFF
C0BF 9700               STAA    PORTA
C0C1 CE0014             LDX     #00014H
C0C4 BDC0E1             JSR     TDELAY      ;DELAY
C0C7 1809               DEY                 ;COUNT -1
C0C9 26E9               BNE     BEEP1       ;IF NOT DONE, KEEP GOING
C0CB 39                 RTS                 ;RETURN FROM SUB.
                        ;
                        ;******* PUT DATA ON DISPLAY ********
C0CC 18A600     PDOD:   LDAA    0,Y         ;GET BYTE
C0CF 2707               BEQ     PDOD1       ;IF END, GOTO NEXT1
C0D1 BDC100             JSR     SENDD
C0D4 1808               INY                 ;NEXT BYTE
C0D6 20F4               BRA     PDOD        ;RETURN TO NEXT
C0D8 39         PDOD1:  RTS                 ;RETURN FROM SUB.
                        ;
                        ;******* TIME DELAY ROUTINE *********
C0D9 CE0002     TD20:   LDX     #00002H     ;20uS DELAY
C0DC 2003               BRA     TDELAY
C0DE CE000F     TD40:   LDX     #0000FH     ;150uS DELAY
C0E1 09         TDELAY: DEX                 ;DECRAMENT COUNT
C0E2 8C0000             CPX     #00000H     ;COUNT = 0?
C0E5 26FA               BNE     TDELAY      ;IF NOT DONE, GOTO TDELAY
C0E7 39                 RTS                 ;RETURN FRO SUB.
                        ;
                        ;******* CLEAR SCREEN, CURSOR HOME, AND SEND INSTRUCTION *******
C0E8 8601       CSCREEN: LDAA   #001H       ;CLEAR DISPLAY
C0EA 2008               BRA     SENDI       ;SEND INSTRUCTION
C0EC 8602       HOME:   LDAA    #002H       ;CURSOR HOME
C0EE 2004               BRA     SENDI       ;SEND INSTRUCTION
C0F0 86C0       LINE2:  LDAA    #0C0H       ;SET CURSOR TO LINE 2
C0F2 2000               BRA     SENDI       ;SEND INSTRUCTION
C0F4 CE4000     SENDI:  LDX     #PORTBC     ;SET UP DATA TRANSFER
C0F7 A706               STAA    6,X         ;STORE AT PIA PORT A
C0F9 1C0702             BSET    7,X,02H     ;DISPLAY E HIGH
C0FC 1D0702             BCLR    7,X,02H     ;DISPLAY E LOW
C0FF 39                 RTS                 ;RETURN FROM SUB.
                        ;
                        ;******* SEND DATA TO DISPLAY ********
C100 CE4000     SENDD:  LDX     #PORTBC     ;SET UP DATA TRANSFER
C103 A706               STAA    6,X         ;SEND DATA
C105 1C0701             BSET    7,X,01H     ;DISPLAY RS HIGH
C108 1C0702             BSET    7,X,02H     ;DISPLAY E HIGH
C10B 1D0702             BCLR    7,X,02H     ;DISPLAY E LOW
C10E 1D0701             BCLR    7,X,01H     ;DISPLAY RS LOW
C111 BDC0DE             JSR     TD40        ;150uS TIME DELAY
C114 39                 RTS                 ;RETURN FROM SUB.
                        ;
                        ;*****************************************************
                        ;*      ROUTINE TO CHANGE BYTE IN EEROM              *
                        ;*      PRELOADED X = ADDRESS IN EEROM (B600 - B7FF) *
                        ;*      DATA TO BE STORED, IS IN "STOR"              *
                        ;*      (THIS IS A MOTOROLA ROUTINE)                 *
                        ;*****************************************************
```

The PSD311 simplifies an eight wire cable tester design and increases flexibility in the process

Appendix B. Core System Software for Cable Tester Design (Cont.)

```
C115 A600      CHGBYT:  LDAA    0,X          ;GET DATA AT ADDRESS TO BE CHANGED
C117 81FF               CMPA    #0FFH        ;CHECK IF ERASED
C119 2717               BEQ     CHGBYT1      ;JUMP IF BYTE ERASED
C11B 8616               LDAA    #016H        ;SET BYTE, ERASE, AND EELAT
C11D 973B               STAA    PPROG
C11F 86FF               LDAA    #0FFH
C121 A700               STAA    0,X
C123 8617               LDAA    #017H        ;SET EEPRG
C125 973B               STAA    PPROG
C127 3C                 PSHX                 ;SAVE X
C128 CE0300             LDX     #00300H
C12B BDC0E1             JSR     TDELAY       ;20mS TIME DELAY
C12E 38                 PULX                 ;RESTORE X
C12F 4F                 CLRA                 ;CLEAR BYTE, ERASE, EELAT, AND EEPRG
C130 973B               STAA    PPROG        ;END OF BYTE ERASE
C132 8602      CHGBYT1: LDAA    #002H        ;SET EELAT - DO BYTE PROGRAM
C134 973B               STAA    PPROG
C136 B61002             LDAA    STOR         ;GET DATA TO BE STORED
C139 A700               STAA    0,X          ;STORE IN NEW LOCATION IN EEROM
C13B 7C003B             INC     PPROG
C13E 3C                 PSHX                 ;SAVE X
C13F CE0300             LDX     #00300H
C142 BDC0E1             JSR     TDELAY       ;20mS DELAY
C145 38                 PULX                 ;RESTORE X
C146 7A003B             DEC     PPROG        ;CLEAR EEPRG
C149 7F003B             CLR     PPROG        ;CLEAR EELAT, END OF BYTE PROGRAM
C14C 39                 RTS                  ;RETURN FROM SUB.
                ;
                ;*******************************************************
                ;*       ROUTINE TO SET UP A/D CONVERTER                *
                ;*       ACC A = VALUE TO INITIATE CONVERSION           *
                ;*       BEFORE ENTRY TO THIS ROUTINE                   *
                ;*******************************************************
C14D 9730      CONV:    STAA    ADCTL        ;SET UP A/D CONVERTER
C14F 133080FC  CONV1:   BRCLR   ADCTL,80H,CONV1 ;WAIT HERE TILL CONVERSION COMPLETE
C153 39                 RTS                  ;RETURN FROM SUB.
                ;
                ;*****************************
                ;*    INTERRUPT ROUTINES     *
                ;*****************************
                ;
                ;*******************************************************
                ;*       SERIAL COMMUNICATIONS INTERFACE - IRQ          *
                ;*******************************************************
                ;
C154 3B         SCOM:    RTI                  ;RETURN FROM INT.
                ;
                ;*******************************
                ;*  SERIAL TRANSFER COMPLETE   *
                ;*******************************
                ;
C155 3B         TRANC:   RTI                  ;RETURN FROM INT.
                ;
                ;*********************************
                ;*  PULSE ACCUMLATOR INPUT EDGE  *
                ;*********************************
                ;
C156 3B         PULSEE:  RTI                  ;RETURN FROM INT.
                ;
                ;*********************************
                ;*  PULSE ACCUMULATOR OVERFLOW   *
                ;*********************************
```

Appendix B. Core System Software for Cable Tester Design (Cont.)

```
                        ;
C157 3B                 PULSEO:  RTI                    ;RETURN FROM INT.
                        ;
                        ;********************
                        ;*  TIMER OVERFLOW  *
                        ;********************
                        ;
C158 3B                 TIMEO:   RTI                    ;RETURN FROM INT.
                        ;
                        ;*****************************
                        ;*  TIMER OUTPUT COMPARE 5   *
                        ;*****************************
                        ;
C159 3B                 COMP5:   RTI                    ;RETURN FROM INT.
                        ;
                        ;*****************************
                        ;*  TIMER OUTPUT COMPARE 4   *
                        ;*****************************
                        ;
C15A 3B                 COMP4:   RTI                    ;RETURN FROM INT.
                        ;
                        ;*****************************
                        ;*  TIMER OUTPUT COMPARE 3   *
                        ;*****************************
                        ;
C15B 3B                 COMP3:   RTI                    ;RETURN FROM INT.
                        ;
                        ;*****************************
                        ;*  TIMER OUTPUT COMPARE 2   *
                        ;*****************************
                        ;
C15C 3B                 COMP2:   RTI                    ;RETURN FROM INT.
                        ;
                        ;*****************************
                        ;*  TIMER OUTPUT COMPARE 1   *
                        ;*****************************
                        ;
C15D 3B                 COMP1:   RTI                    ;RETURN FROM INT.
                        ;
                        ;*****************************
                        ;*  TIMER INPUT COMPARE 3    *
                        ;*****************************
                        ;
C15E 3B                 ICOMP3:  RTI                    ;RETURN FROM INT.
                        ;
                        ;*****************************
                        ;*  TIMER INPUT COMPARE 2    *
                        ;*****************************
                        ;
C15F 3B                 ICOMP2:  RTI                    ;RETURN FROM INT.
                        ;
                        ;*****************************
                        ;*  TIMER INPUT COMPARE 1    *
                        ;*****************************
                        ;
C160 3B                 ICOMP1:  RTI                   ;RETURN FROM INT.
                        ;
                        ;*****************************
                        ;*  REAL TIME INT. ROUTINE   *
                        ;*****************************
                        ;
C161 3B                 REALT:   RTI                    ;RETURN FROM INT.
                        ;
```

Appendix B. Core System Software for Cable Tester Design (Cont.)

```
                        ;**********************
                        ;*  IRQ INT. ROUTINE  *
                        ;**********************
                        ;
C162 960A       DOIT:   LDAA    PORTE       ;GET KEYBOARD DATA
C164 840F               ANDA    #00FH       ;FILTER DATA
                        ;
C166 8100               CMPA    #KEY1       ;1 KEY?
C168 2601               BNE     DOIT10      ;IF NOT GOTO DOIT10
C16A 3B                 RTI                 ;RETURN FROM INT.
                        ;
C16B 8101       DOIT10: CMPA    #KEY2       ;2 KEY?
C16D 2601               BNE     DOIT20      ;IF NOT GOTO DOIT20
C16F 3B                 RTI                 ;RETURN FROM INT.
                        ;
C170 8102       DOIT20: CMPA    #KEY3       ;3 KEY?
C172 2601               BNE     DOIT30      ;IF NOT, GOTO DOIT30
C174 3B                 RTI                 ;RETURN FROM INT.
                        ;
C175 8103       DOIT30: CMPA    #KEYA       ;A KEY?
C177 2601               BNE     DOIT40      ;IF NOT GOTO DOIT40
C179 3B                 RTI                 ;RETURN FROM INT.
                        ;
C17A 8104       DOIT40: CMPA    #KEY4       ;4 KEY?
C17C 2601               BNE     DOIT50      ;IF NOT GOTO DOIT50
C17E 3B                 RTI                 ;RETURN FROM INT.
                        ;
C17F 8105       DOIT50: CMPA    #KEY5       ;5 KEY?
C181 2601               BNE     DOIT60      ;IF NOT GOTO DOIT60
C183 3B                 RTI                 ;RETURN FROM INT.
                        ;
C184 8106       DOIT60: CMPA    #KEY6       ;6 KEY?
C186 2601               BNE     DOIT70      ;IF NOT GOTO DOIT70
C188 3B                 RTI                 ;RETURN FROM INT.
                        ;
C189 8107       DOIT70: CMPA    #KEYB       ;B KEY?
C18B 2601               BNE     DOIT80      ;IF NOT GOTO DOIT80
C18D 3B                 RTI                 ;RETURN FROM INT.
                        ;
C18E 8108       DOIT80: CMPA    #KEY7       ;7 KEY?
C190 2601               BNE     DOIT90      ;IF NOT GOTO DOIT90
C192 3B                 RTI                 ;RETURN FROM INT.
                        ;
C193 8109       DOIT90: CMPA    #KEY8       ;8 KEY?
C195 2601               BNE     DOIT100     ;IF NOT GOTO DOIT100
C197 3B                 RTI                 ;RETURN FROM INT.
                        ;
C198 810A       DOIT100: CMPA   #KEY9       ;9 KEY?
C19A 2601               BNE     DOIT110     ;IF NOT GOTO DOIT110
C19C 3B                 RTI                 ;RETURN FROM INT.
                        ;
C19D 810B       DOIT110: CMPA   #KEYC       ;C KEY?
C19F 2601               BNE     DOIT120     ;IF NOT GOTO DOIT120
C1A1 3B                 RTI                 ;RETURN FROM INT.
                        ;
C1A2 810C       DOIT120: CMPA   #KEYZ       ;* KEY?
C1A4 2601               BNE     DOIT130     ;IF NOT GOTO DOIT130
C1A6 3B                 RTI                 ;RETURN FROM INT.
```

The PSD311 simplifies an eight wire cable tester design and increases flexibility in the process

Appendix B. Core System Software for Cable Tester Design (Cont.)

```
                        ;
C1A7 810D       DOIT130: CMPA    #KEY0          ;0 KEY?
C1A9 2601                BNE     DOIT140        ;IF NOT GOTO DOIT140
C1AB 3B                  RTI                    ;RETURN FROM INT.
                        ;
C1AC 810E       DOIT140: CMPA    #KEYY          ;# KEY?
C1AE 2601                BNE     DOIT150        ;IF NOT GOTO DOIT150
C1B0 3B                  RTI                    ;RETURN FROM INT.
                        ;
C1B1 810F       DOIT150: CMPA    #KEYD          ;D KEY?
C1B3 2600                BNE     DOIT160        ;IF NOT GOTO DOIT160
C1B5 3B         DOIT160: RTI                    ;RETURN FROM INT.
                        ;
                        ;*******************************
                        ;*  XIRQ SERVICE ROUTINE       *
                        ;*******************************
C1B6 3B         NOMASK:  RTI                    ;RETURN FROM INT.
                        ;
                        ;*******************************
                        ;*  SWI SERVICE ROUTINE        *
                        ;*******************************
C1B7 3B         INTER:   RTI                    ;RETURN FROM INT.
                        ;
                        ;*********************************
                        ;*  RESET AND INTERRUPT VECTORS    *
                        ;*********************************
                        ;
FFC0                     ORG     0FFC0H
                        ;
FFC0            RES:     DFS     11*2           ;NOT USED
FFD6 C154       SERCOM:  DWM     SCOM           ;SERIAL COMM. INT.
FFD8 C155       SPISTC:  DWM     TRANC          ;SERIAL TRANSFER COMPLETE
FFDA C156       PAIE:    DWM     PULSEE         ;PULSE ACCUMLATOR INPUT EDGE
FFDC C157       PAOV:    DWM     PULSEO         ;PULSE ACCUMULATOR OVERFLOW
FFDE C158       TOV:     DWM     TIMEO          ;TIMER OVERFLOW
FFE0 C159       TOCP5:   DWM     COMP5          ;TIMER OUTPUT COMPARE 5
FFE2 C15A       TOCP4:   DWM     COMP4          ;TIMER OUTPUT COMPARE 4
FFE4 C15B       TOCP3:   DWM     COMP3          ;TIMER OUTPUT COMPARE 3
FFE6 C15C       TOCP2:   DWM     COMP2          ;TIMER OUTPUT COMPARE 2
FFE8 C15D       TOCP1:   DWM     COMP1          ;TIMER OUTPUT COMPARE 1
FFEA C15E       TICP3:   DWM     ICOMP3         ;TIMER INPUT COMPARE 3
FFEC C15F       TICP2:   DWM     ICOMP2         ;TIMER INPUT COMPARE 2
FFEE C160       TICP1:   DWM     ICOMP1         ;TIMER INPUT COMPARE 1
FFF0 C161       RTIME:   DWM     REALT          ;REAL-TIME INT.
FFF2 C162       IRQ:     DWM     DOIT           ;TIMER/VIA INT.
FFF4 C1B6       XIRQ:    DWM     NOMASK         ;NON-MASKABLE INT.
FFF6 C1B7       SWI:     DWM     INTER          ;SOFTWARE INT.
FFF8 C000       IOT:     DWM     START          ;ILLEGAL OPCODE TRAP (START OVER)
FFFA C000       COPS:    DWM     START          ;COP FAILURE (RESET)
FFFC C000       COPS1:   DWM     START          ;COP CLOCK MONITOR FAIL (RESET)
FFFE C000       RESET:   DWM     START          ;RESET
                        ;
                        ;************************************************
0000                     END                    ;THE END!!!!!
```

Benefits of 16-bit design with PSD3XX

PSD3XX

By Ching Lee – WSI

Introduction

Embedded controller architecture has been evolving from 4-bit, 8-bit to 16-bit through the years. The increase in the data bus bandwidth is a natural progression for microcontrollers to achieve higher performance. Today, 16-bit embedded controllers such as the 80C196 and 683XX families provide excellent performance at reasonable cost. Yet many designers are weary of the cost of higher chip count, more board space and power consumption in 16-bit applications and prefer to stay with 8-bit designs. Some microcontroller manufacturers tackle this problem by introducing processors with 16-bit internal architectures but have 8-bit external data busses. Later additional enhancements such as dynamic bus sizing provide the choice of selecting either an 8 or 16-bit bus for further cost reduction. This compromise certainly increases the performance; it is still not as good as a true 16-bit implementation.

With the introduction of the PSD3XX family of field programmable microcontroller peripherals from WSI, there is no reason not to use 16-bit microcontrollers. The PSD3XX provides an integrated solution in a single chip, which includes user configurable I/O ports, Chip Select outputs, logic replacement, Page Register, Programmable Address Decoder (PAD), EPROM and SRAM. The PSD3XX is a perfect match for 16-bit microcontroller applications. In this application note, we will look at some of the advantages of 16-bit designs, and how PSD3XX interfaces to microcontrollers such as the 80C196 and 68302.

Typical 16-Bit Microcontroller System Architecture

There is no one standard 16-bit architecture, especially in the field of embedded controller applications. For a typical 80C196 design, the basic building block consists of two address latches (74AC373), address decoding logic (with PAL or discrete logic), program memory (EPROMs), data memory (one or more SRAM), and I/O devices.

Figure 1 is the schematic of such a system. In this design, 64K bytes of program memory/EPROM, and a 2K byte SRAM for scratch pad are required. Since the 80C196 has only 64K byte memory space, the INST signal provides the paging capability, with program memory residing in the first 64K page while SRAM and I/O devices occupy the second page. The I/O section consists of one output port (74AC374) and other peripheral devices. The chip select signals for the I/O devices and memory are connected directly from the decoding PAL outputs. The processor's data bus width is determined by the type of bus cycle. EPROM accesses are 16-bits wide, SRAM is 8-bits while I/O bus cycles can be 8 or 16-bits, depending on the device being accessed. The BWIDTH output from the PAL informs the processor what type of bus width is to be expected for that particular cycle.

An I/O device usually takes longer time to complete the bus cycle. Let us assume, in this case, I/O devices require 3 wait states with the exception of the I/O latch. The configuration register of the 80C196 is then programmed to insert 3 wait states. Whenever there is an I/O bus cycle, the READY output signal from the PAL goes low to activate the processor's wait state control to insert the programmed amount of wait state. For memory bus cycles, no wait state is inserted.

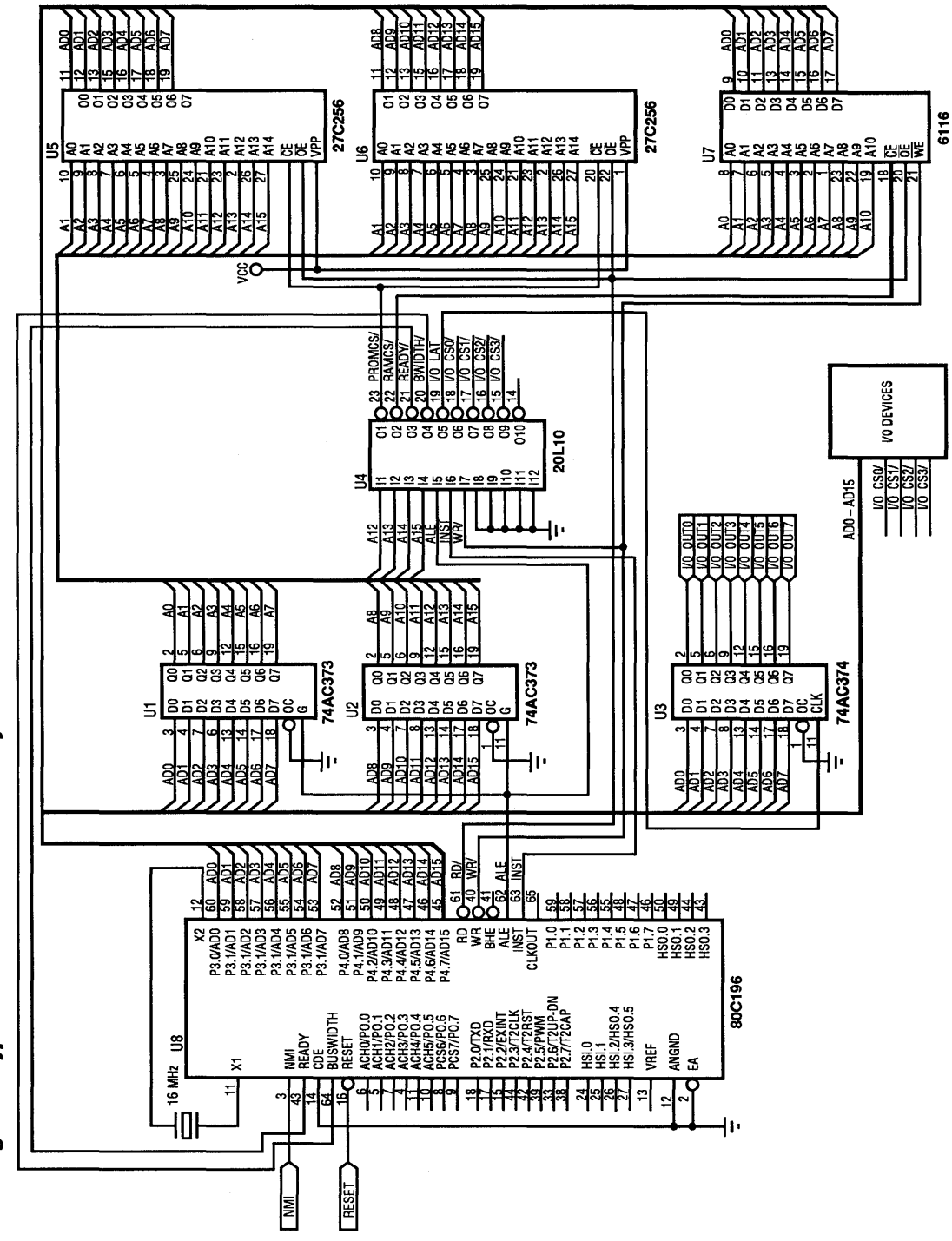


Figure 1. Typical 16-Bit Microcontroller System Architecture

Typical 16-Bit Microcontroller System Architecture (Cont.)

Table 1 is the memory address map of the 80C196 microcontroller, and the addresses of the I/O devices. Address locations 0000H through 00FFH and 1FFEH through 207FH are reserved for the microcontroller. The remaining locations can be used for program/data memory or memory mapped I/O devices. EPROM occupies the first 64K bytes, where program codes start from 2080H to FFFFH, and a 2K look-up table resides inside the EPROM from location 1000H to 17FFH. The 2K scratch RAM and I/O starts from 4000H in the second page.

The address map requires the following PAL equations to be programmed to the decoder PAL. The IO_CS lines are enabled after ALE goes low.

```
EPROMCS  = INST
         + INST/ * A15/ * A14/

RAMCS    = INST/ * A15/ * A14 * A13/ * A12/

BWIDTH   = RAMCS
         + IO_CS0
         + IO_CS1
         + IO_LAT

READY    = IO_CS0
         + IO_CS1
         + IO_CS2
         + IO_CS3

IO_LAT   = INST/ * WR  * A15/ * A14 * A13/* A12
IO_CS0   = INST/ * ALE/ * A15/ * A14 * A13 * A12/ "I/O DEV.#0
IO_CS1   = INST/ * ALE/ * A15/ * A14 * A13 * A12  "I/O DEV.#1
IO_CS2   = INST/ * ALE/ * A15  * A14/ * A13/* A12/ "I/O DEV.#2
IO_CS3   = INST/ * ALE/ * A15  * A14/ * A13/* A12  "I/O DEV.#3
```

Table 1. 80C196 Memory Map

Device	INST (Page)	Address (Hex)	Buswidth (Bit)
EPROM (Code)	1	2080 – FFFF	16
EPROM (Table + Data)	X	1000 – 27FF	16
RAM	0	4000 – 47FF	8
I/O_LATCH	0	5000	8
I/O_CS0	0	6000	8
I/O_CS1	0	7000	8
I/O_CS2	0	8000	16
I/O_CS3	0	9000	16

16-Bit Performance Advantages

It is obvious that a 16-bit bus provides more performance than an 8-bit bus, at least the data bus bandwidth will double. The following factors contribute to the performance improvement:

Program Code Fetch

Instructions such as ANDB of the 80C196 consists of 4 bytes. In an 8-bit bus system it takes 4 bus cycles to fetch the instruction, while in 16-bit bus designs it takes only 2 bus cycles.

Data Fetch

For applications with high data transfer rate, where indexed or indirect references are frequently used, a 16-bit bus takes much less time to accomplish the same job.

Queue Flush for Branch/Jump Instructions

A pre-fetch queue usually speeds up instruction execution time by providing instructions to the Execution Unit in a timely manner. However there is a penalty which goes with the queue when a successful branch or jump instruction is executed. The queue has to be flushed, Program Counter to be reloaded, and new instructions to be fetched. A 16-bit bus helps to fill up the queue much faster. This is critical to system performance since Branch/Jump instructions are the most frequently used instructions in general.

Free Up The System Bus

The microcontroller reduces its number of operand fetches in a 16-bit bus, freeing the bus for other devices which share the same bus. In system which has a DMA Controller or Slave Processor sharing the same memory space with the microcontroller, the less usage of the memory bus will enhance system performance.

Let us look at a sample program to calculate the differences in execution time between an 8 and a 16-bit bus. In the typical 16-bit design example above, there is a look-up table residing in the EPROM. A look-up table is a quick way for the program to provide an output to an I/O device based on the input value without getting into complex mathematical operations. The following program, which is published in Intel application note AP-248, does table look-up and interpolation.

Assuming the 80C196 queue is always full, to execute the following code takes 128 state times in a 16-bit bus. In an 8-bit bus, it takes 32 more state times just to fetch the codes and data, not including the time the microcontroller waits for the queue to be filled. The estimated performance penalty for an 8-bit bus in this application is at least 25%, and will certainly be more in the actual run time environment. The published statement from Intel is that it is difficult to measure the 8-bit bus performance penalty, but has shown to be up to 30%, depending on the instruction mix.

The 16-bit bus design will increase the system performance, especially for microcontrollers which usually don't have internal program cache or a pre-fetch pipeline queue to lessen the penalty caused by the bottle neck on the memory bus. The 80C196 has an internal 4 byte queue. This helps execution time but bus width still remains the critical factor.

Table Look-up and Interpolation

```
RSEG  at 22H

IN-VAL:          dsb      1        ;Actual Input Value
TABLE_LOW:       dsw      1
TABLE_HIGH:      dsw      1
IN_DIF:          dsw      1        ;Upper Input-Lower Input
IN_DIFB:         equ      IN_DIF   :byte
TAB_DIF:         dsw      1        ;Upper Output- Lower Output
OUT:             dsw      1
RESULT:          dsw      1
OUT_DIF:         dsl      1        ;Delta Out

CSEG at 2080H

LD     SP, #100h

Look:

LDB    AL, IN_VAL                 ;Load temp with Actual Value
SHRB   AL, #3                     ;Divide the byte by 8
ANDB   AL, #11111110B             ;Insure AL is a word address
                                  ;This effectively divides AL by 2
                                  ;so AL = IN_VAL/16
LDBZE  AX, AL                     ;Load byte AL to word AX
LD     TABLE_LOW, TABLE [AX]
                                  ;TABLE_LOW is loaded with the value
                                  ;in the table at table location AX
LD     TABLE_HIGH, (TABLE+2)[AX]
                                  ;TABLE_HIGH is loaded with the value
                                  ;in the table at table loc. AX+2
                                  ;(The next value in the table)
SUB    TAB_DIF, TABLE_HIGH, TABLE_LOW
                                  ;TAB_DIF=TABLE_HIGH - TABLE_LOW
ANDB   IN_DIFB, IN_VAL, #0FH
                                  ;IN_DIFB=least significant 4 bits of
                                  ;IN_VAL
LDBZE  IN_DIF,IN_DIFB             ;Load byte IN_DIFB to word IN_DIF
MUL    OUT_DIF, IN_DIF, TAB_DIF
                                  ;Output_difference =
                                  ;Input_difference * Table_difference
SHRAL  OUT_DIF, #4                ;Divide by 16 (2**4)
ADD    OUT, OUT_DIF, TABLE_LOW
                                  ;Add output difference to output
                                  ;generated with truncated IN_VAL as input
SHRA   OUT, #4                    ;Round to 12-bit answer
ADDC   OUT, ZERO                  ;Round up if Carry = 1

No_Inc:

ST     OUT, RESULT                ;Store OUT to RESULT
BR     Look                       ;Branch to "Look"

CSEG   at 2100h

Table:
       DCW    0000H,  2000H,  3400H,  4C00H ;A random function
       DCW    5D00H,  6A00H,  7200H,  7800H
       DCW    7B00H,  7D00H,  7600H,  6D00H
       DCW    5D00H,  4B00H,  3400H,  2200H
       DCW    1000H
END
```

PSD3XX Solution for 16-Bit Microcontroller

In this section, we will see how a single PSD302 is able to replace all the basic building blocks as shown in the design example in Figure 1. As seen from the block diagram (Figure 2.), the PSD302 provides the following functional blocks:

- 64K bytes EPROM, as 64K x 8 or 32K x 16
- 2K bytes SRAM, as 2K x 8 or 1K x 16, expanding the microcontroller's internal scratch SRAM
- Address latches/data buffers, bus interface to most microcontrollers.
- Programmable Address Decoder (PAD); provides PAL type function: 18 inputs, 24 outputs and 40 product terms.
- Port A: an 8–bit port, each bit can be configured as :
  - I/O line
  - latched address output (A0–A7)
  - track AD0/AD7 as I/O lines in track mode for shared access.
  - data port D0/D7 in non-multiplexed mode
  - CMOS or open drain output
- Port B: an 8-bit port, each bit can be configured as :
  - I/O line
  - chip select or logic replacement output from the PAD
  - D8–D15 in non-multiplexed mode
  - CMOS or open drain output
- Port C: 3-bit port, each bit can be configured as input to or output from the PAD
- Page Register: a 4-bit Page Register for bank switching
- A19/$\overline{CSI}$ input pin for power down configuration

Figure 3 is the schematic of the design example with the PSD302. Not all the functions of the PSD3XX are utilized in this example. The Page Register is not used since the INST signal from the 80C196 can be easily included in the PAD for page decoding (for design with the Page Register, see WSI Application Note 015). The internal EPROM and SRAM of the PSD302 replaces U5, U6, and U7 in Figure 1. Port A is configured as an I/O port to replace U3, the I/O latch. The PAD provides decoding functions for all the chip selects, as well as the READY and BWIDTH inputs to the microcontroller. Please note the PSD302 is able to provide a 16-bit SRAM for faster data accesses.

In this application the PSD302 is configured to operate in a 16-bit, multiplexed mode. The PAL equations are programmed into the PAD. Depending on the particular bus cycle, the PSD302 latches the micro-controller address, determines which device is to be enabled, and provides data output for a read cycle. If it is an I/O bus cycle, either Port A is enabled or one of the I/O_CS lines are activated. At the same time, the appropriate READY and BWIDTH signals are generated.

Figure 2. PSD302 Block Diagram

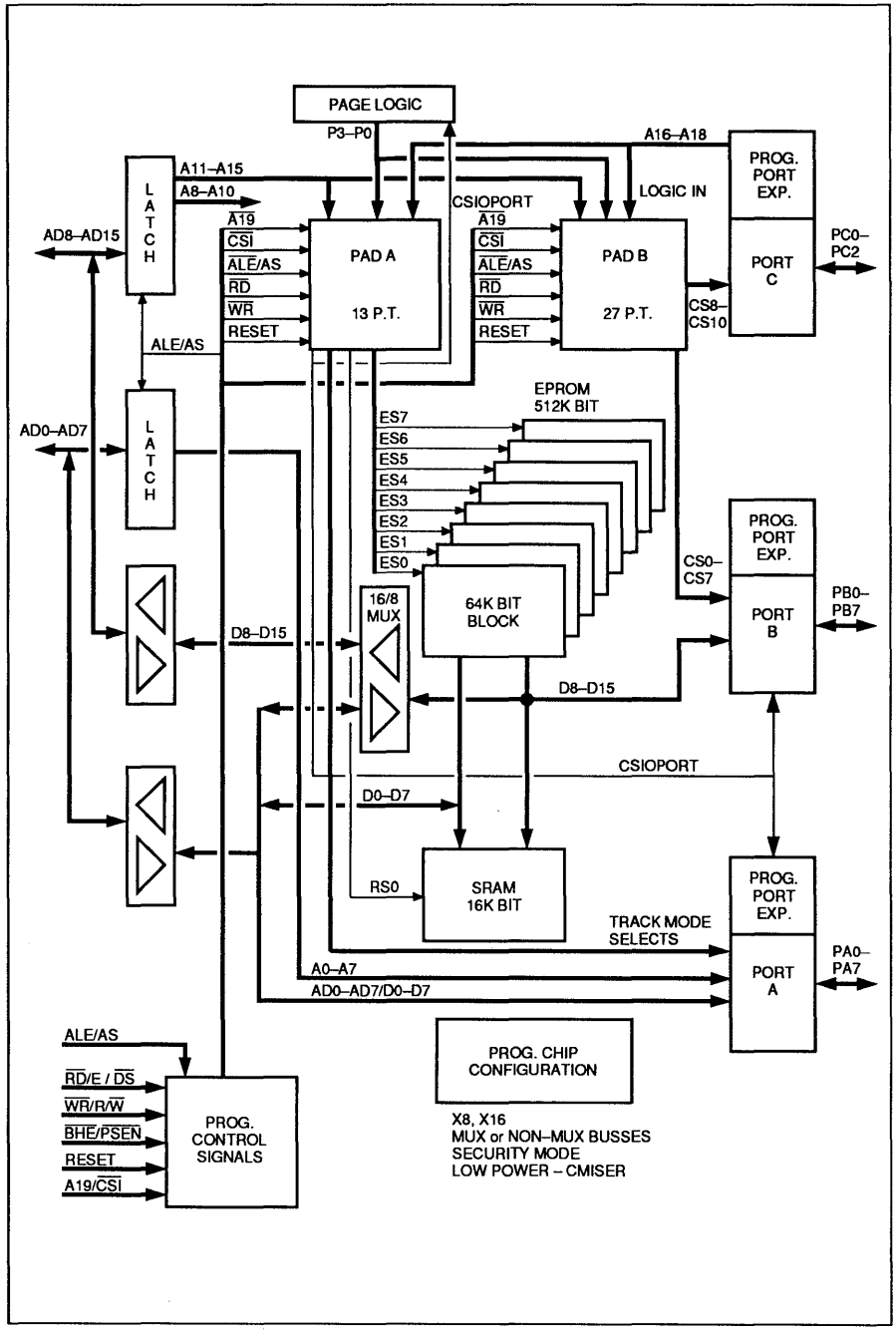
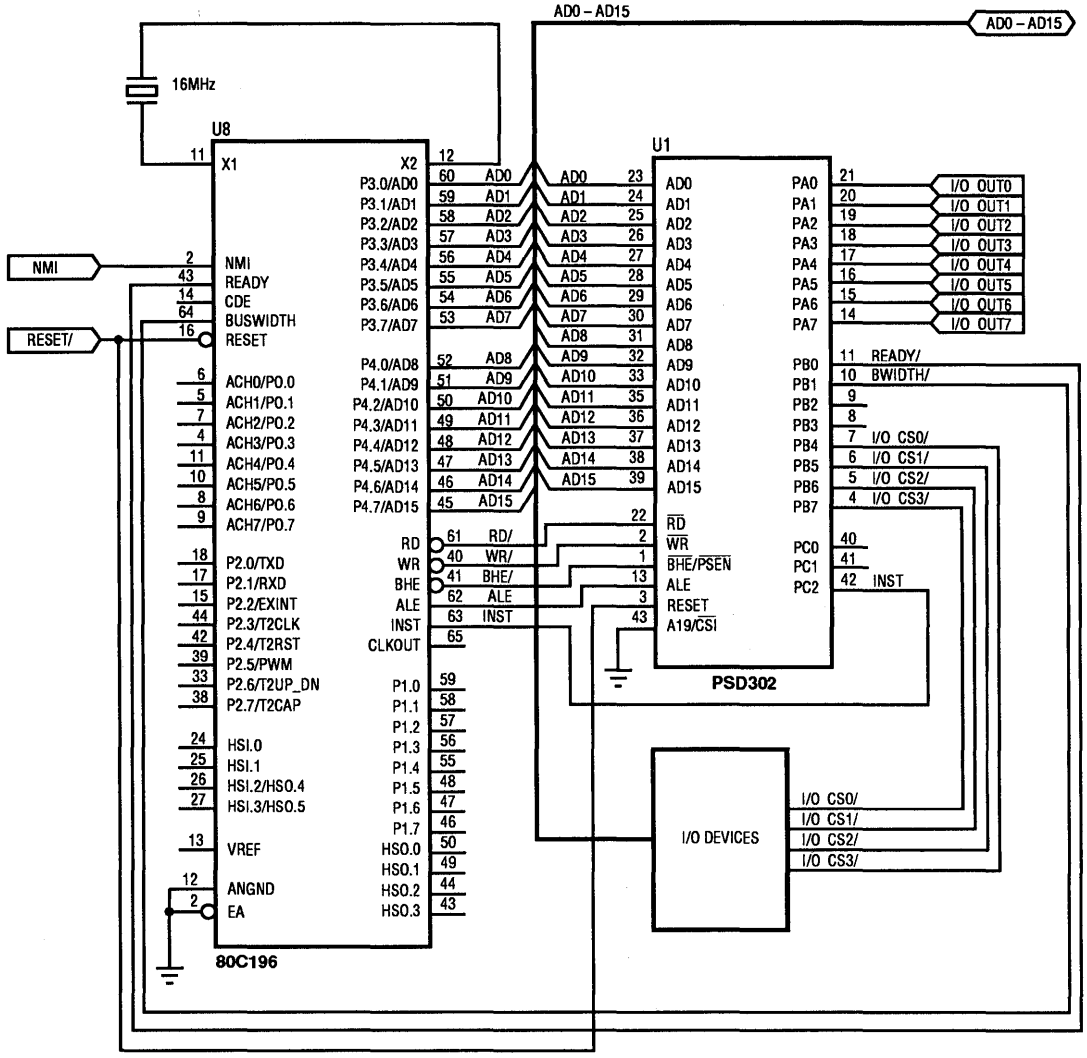


Figure 3. Design Example with PSD302



PSD3XX Solution for 16-Bit Microcontroller (Cont.)

WSI supplies PSD users with easy to use software tools and programming devices. MAPLE software, which is PC based, enables designers to configure the PSD3XX. Some of the computer screen configuration displays for this design example are shown in Figure 4. Figure 4A is the address map decode for the EPROM, SRAM and Port A. Figure 4B is the truth table input for the READY signal.

Figure 4A. PSD3XX Address Map

ADDRESS MAP

	A 19	A 18	A 17	A 16	A 15	A 14	A 13	A 12	A 11	SEGMT START	SEGMT STOP	FILE START	FILE STOP	FILE NAME
ES0	N	0	X	X	0	0	0	N	N			0	1FFF	TEST.HEX
ES1	N	X	X	X	0	0	1	N	N			2000	3FFF	TEST.HEX
ES2	N	1	X	X	0	1	0	N	N			4000	5FFF	TEST.HEX
ES3	N	1	X	X	0	1	1	N	N			6000	7FFF	TEST.HEX
ES4	N	1	X	X	1	0	0	N	N			8000	9FFF	TEST.HEX
ES5	N	1	X	X	1	0	1	N	N			A000	BFFF	TEST.HEX
ES6	N	1	X	X	1	1	0	N	N			C000	DFFF	TEST.HEX
ES7	N	1	X	X	1	1	1	N	N			E000	FFFF	TEST.HEX
RS0	N	0	X	X	0	1	0	0	0			N/A	N/A	N/A
CSP	N	0	X	X	0	1	0	1	0			N/A	N/A	N/A

ALIAS: A18 = INST →

Fill in A19 – A12 (Binary) or SEGMT START (Hex); and FILE (START, STOP) FILE NAME, P3..P0, and ALE/AS. Use SPACEBAR to erase any field value.
F1 – Return to Main Menu F2 – Temporary Exit to DOS F3 – Go to Help
Cursor – UP: ↑ Down: ↓ Left Col: ← Right Col: → Right – F4 Left – F5

PART NAME: PSD302 C:\WSI\OLDMAP

Figure 4B. READY Signal Truth Table

PORT B

PIN	CS/I/O	CMOS/OD
PB0	CS0	CMOS
PB1	CS1	CMOS
PB2	CS2	CMOS
PB3	CS3	CMOS
PB4	CS4	CMOS
PB5	CS5	CMOS
PB6	CS6	CMOS
PB7	CS7	CMOS

CHIP SELECT DEFINITION READY

A18	A17	A16	A15	A14	A13	A12	A11	RD	WR	ALE	P3
0	X	X	0	1	1	0	X	X	X	0	X
0	X	X	0	1	1	1	X	X	X	0	X
0	X	X	1	0	0	0	X	X	X	0	X
0	X	X	1	0	0	1	X	X	X	0	X

ALIAS: A18 = INST →

CS definition is the NOR of the product terms (rows). Enter 1 to select High signal, 0 to select Active Low signal, X to mean "don't care", SPACEBAR to erase. Enter values in columns relevant to your application; leave other columns untouched.

F1 – Return to PORT B Menu Cursor – Up↑ Down↓ Left← Right→

PART NAME: PSD302 C:\WSI\OLDMAP

PSD3XX Solution for 16-Bit Processor with Non-Multiplexed Bus

A PSD3XX can be configured to operate in the 16-bit mode with a non-multiplexed bus. In this case, the microcontroller address lines A0–A15 are tied to AD0–AD15 inputs of the PSD3XX; Port A and B of the PSD3XX are then configured as data ports, connecting to data bus D0–D15. In applications where the EPROM space in a PSD3XX is not enough, or a large amount of I/O lines and chip selects are needed, two PSD3XXs will provide a viable solution. Connecting two PSD3XXs to a microcontroller needs special consideration.

Figure 5 shows a basic design of a 68302 microcontroller interfacing to two PSD312s. The implementation is fairly straightforward; the two PSD302's are configured to work in 8-bit non-multiplexed mode. The first PSD302 (U2) occupies the even bank of the memory space of the 68302; the second PSD302 (U3) occupies the odd bank. The 68302 has no A0 in the address bus; it depends on signals UDS/ and LDS/ (Upper and Lower Data Strobe) to control the flow of data on the data bus as shown in Table 2.

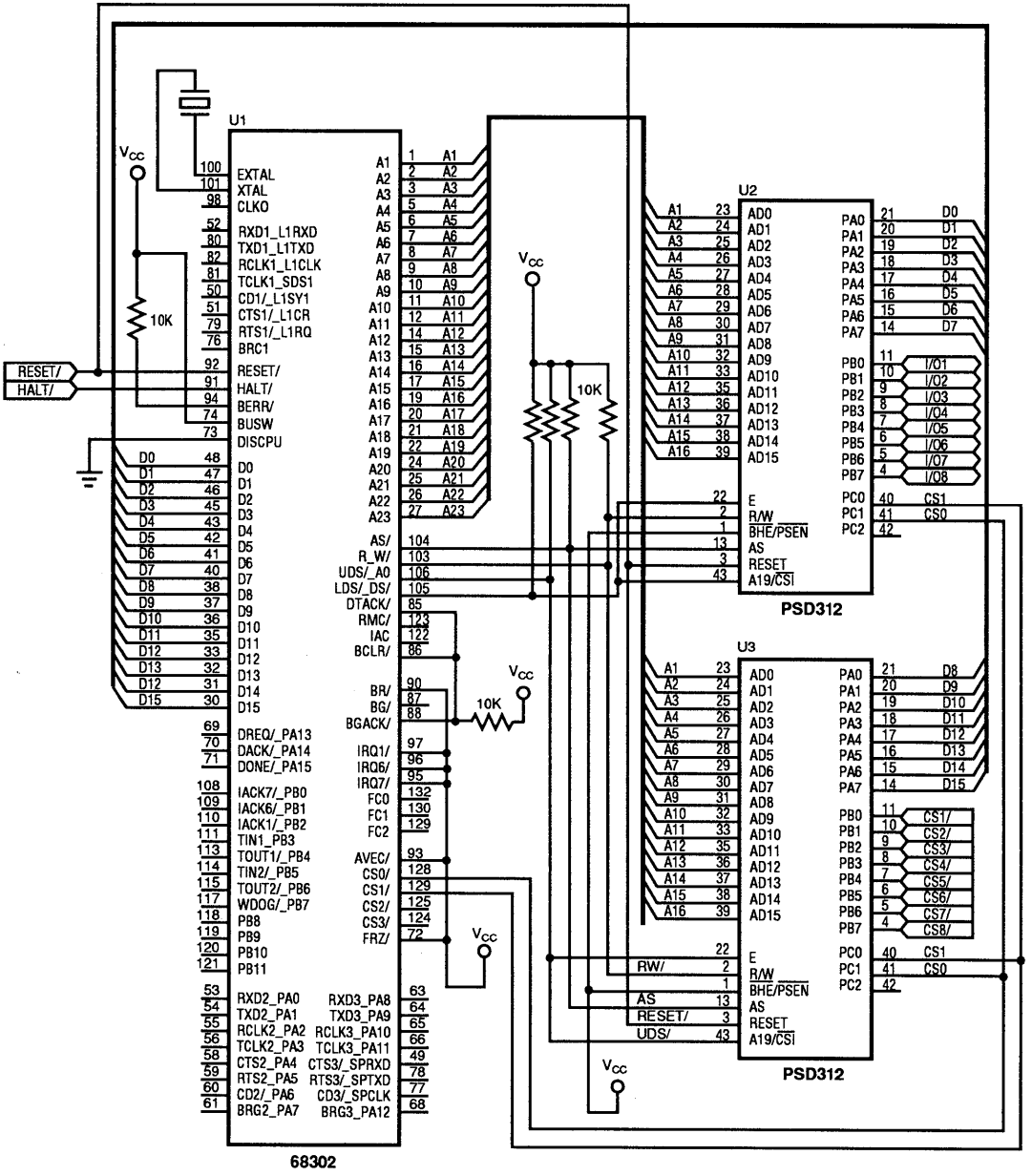
Table 2. 68302 Byte Enable

UDS/	LDS/	D8–D15	D0–D7
Low	Low	Enabled	Enabled
Low	High	Enabled	Disabled
High	Low	Disabled	Enabled
High	High	Disabled	Disabled

The above table is also true for most other microcontrollers. Some use different signal names, such as HBE/ for UDS/ and A0 is equivalent to LDS/. The decoding for bank select is the same for both cases. The following points must be considered when configuring the PSD3XX for this type of application:

- Address inputs to the PSD3XX have to shift right by one. Address line A1 connects to AD0 pin of the PSD3XX and so on. For processors which have A0, A0 is no longer used as address input.
- Provide bank select signals to the appropriate PSD3XX for proper bank decoding. The even bank PSD3XX must include signal LDS/ as input to the PAD, and the odd bank PSD3XX requires the signal UDS/. These signals can be connected to Port C or the A19/$\overline{CSI}$ pin in order to be routed as PAD inputs.
- While inside the MAPLE software during PSD3XX configuration, the address map decode of the EPROM, SRAM, I/O port must also reflect the shift of the address inputs.
- The codes of the user's program have to be split into two files, one for the even bank PSD3XX and one for the odd bank PSD3XX.

Figure 5. PSD3XX Interface to 68302



PSD3XX Solution for 16-Bit Microcontroller with Non-Multiplexed Bus

Figure 6 shows the address map of the odd bank PSD3XX. In the map table, the columns A19, A17, A16 are input signals of UDS, CS0 and CS1. Since this is the decoding for the odd bank, UDS (column A19) has to be low for any of the PSD3XX devices to be enabled.

Furthermore, the CS0 selects the EPROM and CS1 selects SRAM and I/O Port. The chip select logic of the 68302 also generates the programmed amount of wait state internally.

The columns A15, A14, A13 in the address map are actually A16, A15 and A14 after the input address lines to the PSD3XX are shifted by one. Entries to the SEGMT START/STOP or FILE START/STOP columns must also change to reflect the shift of the address lines. For example, the top address of the EPROM (128K bytes) was 1FFFF, and is now 0FFFF after the shift.

Figure 6. Address Map, Odd Bank PSD3XX

ADDRESS MAP

	A 19	A 18	A 17	A 16	A 15	A 14	A 13	A 12	A 11	SEGMT START	SEGMT STOP	FILE START	FILE STOP	FILE NAME
ES0	0	X	0	1	0	0	0	N	N			0	1FFF	ODD.HEX
ES1	0	X	0	1	0	0	1	N	N			2000	3FFF	ODD.HEX
ES2	0	X	0	1	0	1	0	N	N			4000	4FFF	ODD.HEX
ES3	0	X	0	1	0	1	1	N	N			6000	7FFF	ODD.HEX
ES4	0	X	0	1	1	0	0	N	N			8000	9FFF	ODD.HEX
ES5	0	X	0	1	1	0	1	N	N			A000	BFFF	ODD.HEX
ES6	0	X	0	1	1	1	0	N	N			C000	DFFF	ODD.HEX
ES7	0	X	0	1	1	1	1	N	N			E000	FFFF	ODD.HEX
RS0	0	X	1	0	0	0	0	0	0			N/A	N/A	N/A
CSP	0	X	1	0	1	0	0	0	0			N/A	N/A	N/A

ALIAS: A19 = UDS →

Fill in A19 – A12 (Binary) or SEGMT START (Hex); and FILE (START, STOP) FILE NAME, P3..P0, and ALE/AS. Use SPACEBAR to erase any field value.
F1 – Return to Main Menu F2 – Temporary Exit to DOS F3 – Go to Help
Cursor – UP: ↑ Down: ↓ Left Col: ← Right Col: → Right – F4 Left – F5

Conclusion

After going through the design examples with the PSD3XX, it is not difficult to see the advantages the PSD3XX family offers over designs with discrete ICs. Besides providing 16-bit performance, PSD3XX devices are able to replace 7 ICs in the 80C196 example. This not only reduces the board size dramatically but also provides benefits such as cost reduction in board manufacturing, higher product reliability, lower power consumption and reduced component cost.

Other PSD3XX advantages over the discrete component design include the power down mode to reduce power consumption when the microcontroller is idle. The security feature protects the code stored in the EPROM from illegal copy. The flexibility, programmability, and ease of use which come with the PSD3XX truly make it an optimal solution for 16-bit embedded applications.

Section 4
Development Systems

PSD3XX Programmable Microcontroller Peripherals

INDEX

MagicPro® is a registered trademark of WaferScale Integration, Inc.

PSDGold/PSDSilver Development System

PSD3XX

Description

PSDGold/PSDSilver is a complete set of IBM-PC-based development tools. They provide the integrated easy-to-use environment to support PSD3XX family.

The tools run on an IBM-PC XT, AT or compatible computer running MS-DOS version 3.1 or later.

MAPLE

MAPLE is the Locator Editor. It has the following features:

- ❑ Simple Menu Driven Commands for selecting different configurations of the PSD3XX
  - – Byte wide or word wide operation.
  - – Address or Chip Select Input (CSI) Mode.
  - – PAD security option.
- ❑ Generating the PAD programming data that maps the EPROM, SRAM and Chip Selects Outputs to the user's address space.
- ❑ Combining all the different files to be programmed into the EPROM segments.

MAPPRO

MAPPRO is the interface software that enables the user to program a PSD3XX on the WS6000 MagicPro® programmer. The MAPPRO enables the user to load the program into the programmer and to execute the following operations.

- ❑ Help
- ❑ Upload RAM from MAP
- ❑ Load RAM from disk
- ❑ Write RAM to FILE
- ❑ Display MAP data
- ❑ Blank test MAP
- ❑ Verify MAP
- ❑ Program MAP
- ❑ Configuration
- ❑ Quit

WS6000 MagicPro® Programmer

The WS6000 MagicPro Programmer is an engineering development tool designed to program all WSI programmable products (EPROMs, RPROMs, PAC1000, PSD3XX family and SAM448). It is used within the IBM-PC and compatible environment. The MagicPro consists of a short plug-in board and a Remote Socket Adaptor (RSA). It occupies a short expansion slot in the PC. The RSA has two ZIF-DIP sockets that will support 24, 28, 32 and 40 pin standard 600 mil or slim 300 mil DIP packages without adaptors. Other packages are supported using adaptors.

PSDGold/PSDSilver Development System

PSD3XX

PSDGold

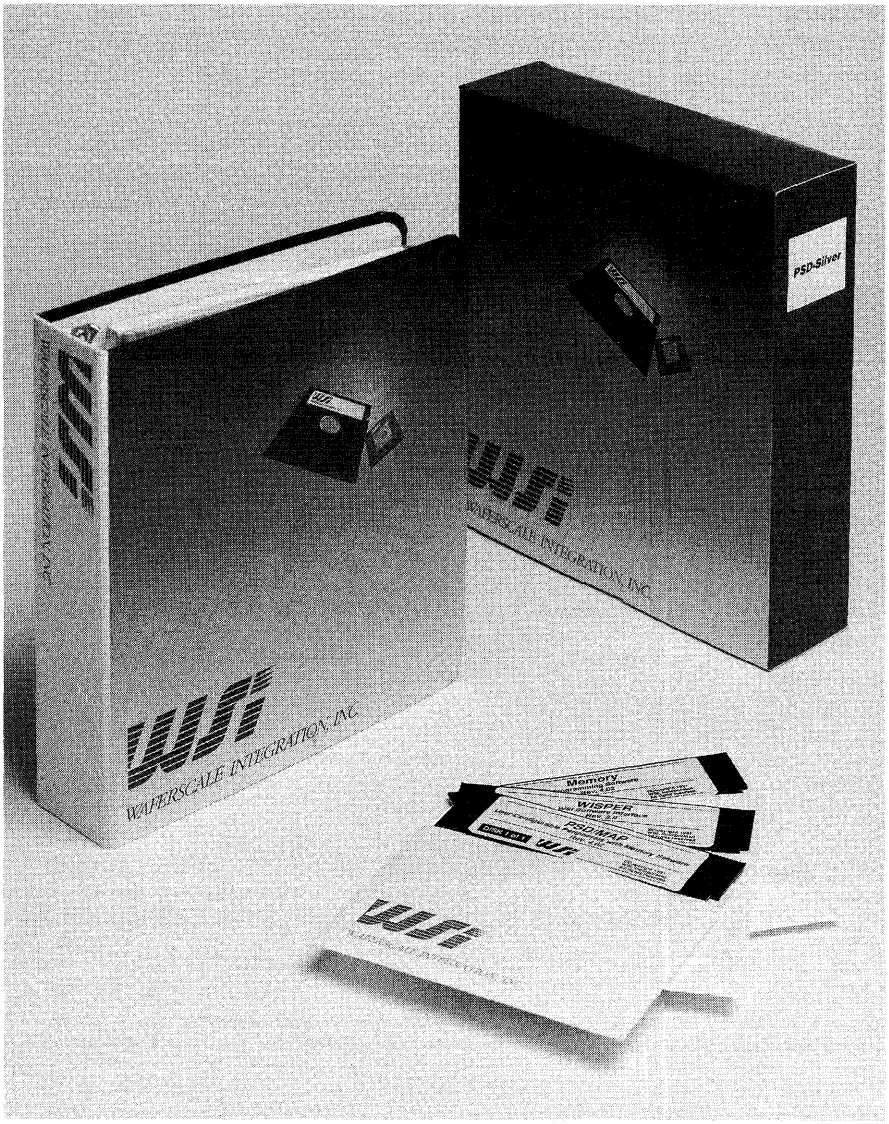
Contents

- ❑ MAPLE-MAP Locator editor.
- ❑ MAPPRO
  Interface software to MAP168 device programmer (MagicPro)
- ❑ Software user's manual
- ❑ WS6000 MagicPro Programmer
- ❑ A Socket Adaptor and Two Product Samples

PSDGold/PSDSilver Development System

PSD3XX

PSDSilver



Contents

- ❑ MAPLE-MAP Locator editor.
- ❑ MAPPRO
  Interface software to PSD100 device programmer (MagicPro)
- ❑ Software user's manual

WS6015 Socket Adaptor

The WS6015 is a socket adaptor that mounts on the MagicPro RSA and adapts the PSD3XX or MAP168 in a 44-pin PGA package to the programmer.

WS6020 Socket Adaptor

The WS6020 is a socket adaptor that mounts on the MagicPro RSA and adapts the PSD3XX in a 52-pin PQFP package to the programmer.

WS6021 Socket Adaptor

The WS6021 is a socket adaptor that mounts on the MagicPro RSA and adapts the PSD3XX in a 44 pin CLDCC or PLDCC package to the programmer.

Ordering Information

Product	Description
PSDSilver	Contains PSD3XX and PSD100 Software (MAPLE-MAP and MAPPRO), Software User's Manual.
PSDGold	Contains PSD-Silver, WS6000 MagicPro Programmer, a Socket Adaptor and Two Product Samples.

MagicPro® Memory and Programmable Peripheral Programmer

WS6000

Key Features

- ❑ Programs All CMOS Memory and Programmable Peripheral Products and all future Programmable Products
- ❑ Programs 24, 28, 32 and 40 Pin Standard 600 Mil or Slim 300 Mil Dip Packages without Adaptors
- ❑ Programs LCC, PGA and QFP Packaged Product by Using Adaptors
- ❑ Easy-to-Use Menu-Driven Software
- ❑ Compatible with IBM PC/XT/AT Family of Computers (and True Plug-Compatible

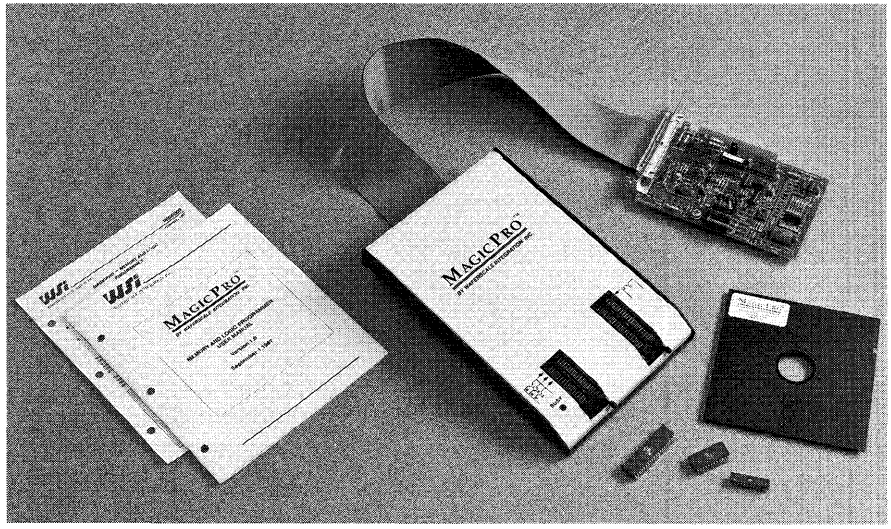
General Description

MagicPro is an engineering development tool designed to program Programmable Peripherals. It is used within the IBM-PC® and compatible computers. The MagicPro is meant to bridge the gap betweeen the introduction of a new programmable product and the availability of programming support from programmer manufacturers (e.g., Data I/O, etc.). The MagicPro programmer and accompanying software enable quick programming of newly released programmable products, thus accelerating the system design process.

The MagicPro plug-in board is integrated easily into the IBM-PC. It occupies a short expansion slot and its software requires only 256K bytes of computer memory. The two external ZIF-Dip sockets in the Remote Socket Adaptor (RSA) support 24, 28, 32 and 40 pin standard 600 mil or slim 300 mil Dip packages without adaptors. LCC, PGA and QFP packages are supported using adaptors.

Many features of the MagicPro Programmer show its capabilities in supporting future products. Some of these are:

- ❑ 24 to 40 pin JEDEC Dip Pinouts
- ❑ 1 Meg Address Space (20 address lines)
- ❑ 16 Data I/O Lines



MagicPro® Memory and Programmable Peripheral Programmer

WS6000

General Description (Cont.)

The MagicPro menu driven software makes using different features of the MagicPro an easy task. Software updates are done via floppy disk which eliminates the need for adding a new memory device for system upgrading.

The MagicPro reads Intel Hex format for use with assemblers and compilers.

MagicPro Commands

- ❑ Help
- ❑ Upload RAM from Device
- ❑ Load RAM from Disk
- ❑ Write RAM to Disk
- ❑ Display RAM Data
- ❑ Edit RAM
- ❑ Move/Copy RAM
- ❑ Fill RAM
- ❑ Blank Test Device
- ❑ Verify Device
- ❑ Program Device
- ❑ Select Device
- ❑ Configuration
- ❑ Quit MagicPro

Technical Information

❑ ***Size:***
IBM-PC Short Length Card

❑ ***Port Address Location:***
100H to 1FFH – default 140H (if a conflict exists with this address space, the address location can be changed in software and with the switches on the plug-in board.)

❑ ***System Memory Requirements:***
256K Bytes of RAM

❑ ***Power:***
+ 5 Volts, 0.03 Amp; +12 Volts, 0.04 Amp

❑ ***Remote Socket Adaptor (RSA):***
The RSA contains two ZIF-Dip sockets that are used to program and read WSI programmable products. The 32 pin ZIF-Dip socket supports 24, 28 and 32 pin standard 600 mil or slim 300 mil Dip packaged product. The 40 pin ZIF-Dip socket supports all 40 pin Dip packages. Adaptor sockets are available for LCC, PGA and QFP packages.

MagicPro® Memory and Programmable Peripheral Programmer

WS6000

Ordering Information

The WS6000 MagicPro System Contains:

- ❑ MagicPro IBM-PC Plug-in Programmer Board
- ❑ MagicPro Remote Socket Adaptor and Cable
- ❑ MagicPro Operating System Floppy Disk and Operating Manual

The WS6000 MagicPro Adaptors Include:

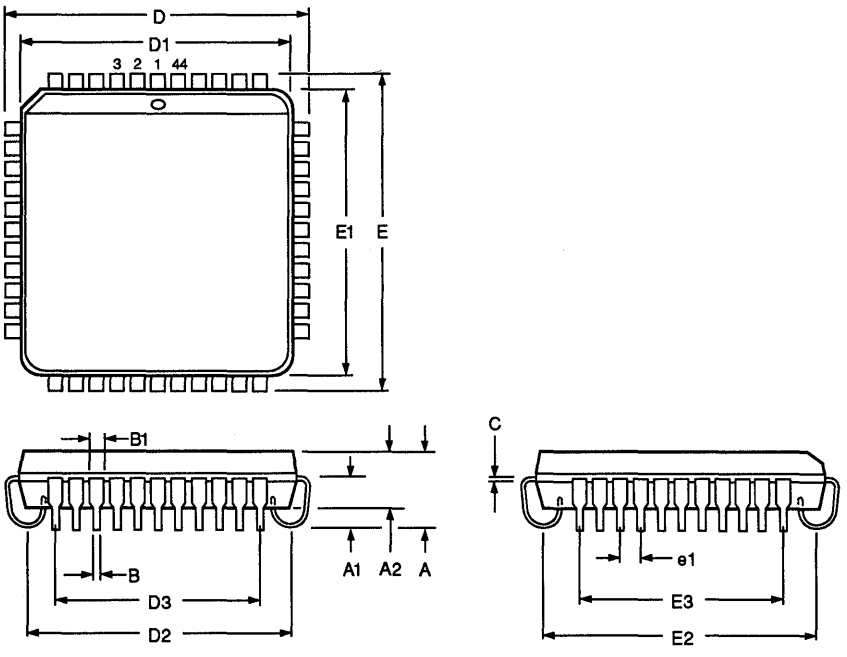
- ❑ WS6001 28-Pin CLLCC Package Adaptor for Memory.
- ❑ WS6008 28-Pin Dip Adaptor for SAM448
- ❑ WS6009 28-Pin PLDCC/CLDCC/ CLLCC Package Adaptor for SAM448
- ❑ WS6010 88-Pin PGA Package Adaptor for PAC1000
- ❑ WS6012 32-Pin CLDCC/CLLCC/PLDCC Package Adaptor for Memory
- ❑ WS6020 52-Pin PQFP Package Adaptor for PSD3XX
- ❑ WS6021 44-Pin CLDCC/PLDCC Package Adaptor for PSD3XX/3XXL
- ❑ WS6022 44-Pin PGA Package Adaptor for PSD3XX/3XXL
- ❑ WS6023 100-Pin PQFP Package Adaptor for PAC1000
- ❑ WS6024 28-Pin CLLCC Package Adaptor for Memory
- ❑ WS6025 32-Pin PLDCC/CLDCC Package Adaptor for Memory (WS57C51B/C Only)
- ❑ WS6026 32-Pin CLLCC Package Adaptor for Memory (WS57C51B/C Only)
- ❑ WS6027 32-Pin PLDCC/CLDCC Package Adaptor for Memory (WS57C71C Only)
- ❑ WS6028 32-Pin CLLCC Package Adaptor for Memory (WS57C71C Only)

Section 5
Package Outlines

INDEX

Package Outlines

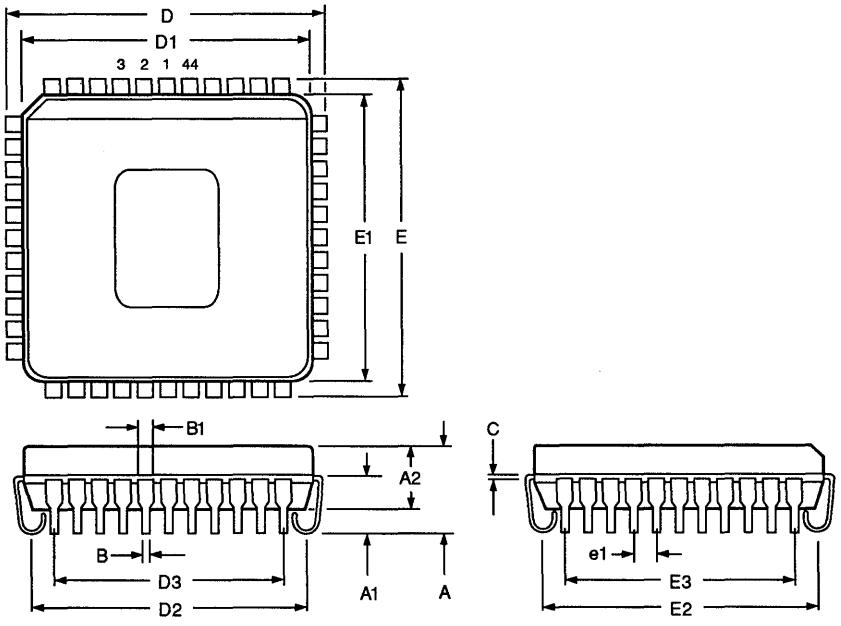
J2 44-PIN PLASTIC LEADED CHIP CARRIER (PLCC) (PACKAGE TYPE J)



Family: Plastic Leaded Chip Carrier						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
A	4.19	4.57		0.165	0.180	
A1	2.54	2.79		0.100	0.110	
A2	3.76	3.96		0.148	0.156	
B	0.33	0.53		0.013	0.021	
B1	0.66	0.81		0.026	0.032	
C	0.246	0.262		0.0097	0.0103	
D	17.40	17.65		0.685	0.695	
D1	16.51	16.61		0.650	0.654	
D2	14.99	16.00		0.590	0.630	
D3	12.70		Reference	0.500		Reference
E	17.40	17.65		0.685	0.695	
E1	16.51	16.61		0.650	0.654	
E2	14.99	16.00		0.590	0.630	
E3	12.70		Reference	0.500		Reference
e1	1.27		Reference	0.050		Reference
N	44			44		

Package Outlines

L4 44-PIN CERAMIC LEADED CHIP CARRIER (CLCC) WITH WINDOW (PACKAGE TYPE L)

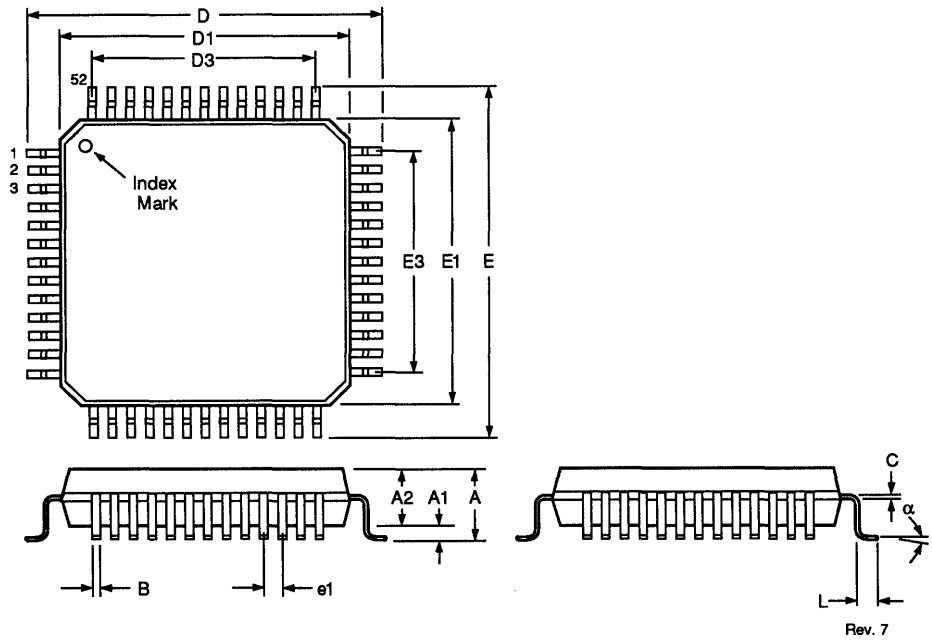


Family: Ceramic Leaded Chip Carrier-CERQUAD						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
A	3.94	4.57		0.155	0.180	
A1	2.29	2.92		0.095	0.115	
A2	3.05	3.68		0.120	0.145	
B	0.43	0.53		0.017	0.021	
B1	0.66	0.81		0.026	0.032	
C	0.15	0.25		0.006	0.010	
D	17.40	17.65		0.685	0.695	
D1	16.31	16.66		0.642	0.656	
D2	14.99	16.00		0.590	0.630	
D3	12.70		Reference	0.500		Reference
E	17.40	17.65		0.685	0.695	
E1	16.31	16.66		0.642	0.656	
E2	14.99	16.00		0.590	0.630	
E3	12.70		Reference	0.500		Reference
e1	1.27		Reference	0.050		Reference
N	44			44		

L4

Package Outlines

Q2 52-PIN PLASTIC QUAD FLATPACK (PQFP)



Family: Plastic Quad Flatpack						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	8°		0°	8°	
A	2.55	3.05		0.100	0.120	
A1	0.00	0.25		0.000	0.010	
A2	2.55	2.80		0.100	0.110	
B	0.35	0.50		0.014	0.020	
C	0.13	0.23		0.005	0.009	
D	17.65	18.15		0.695	0.715	
D1	13.95	14.05		0.549	0.553	
D3	12.00		Reference	0.472		Reference
E	17.65	18.15		0.695	0.715	
E1	13.95	14.05		0.549	0.553	
E3	12.00		Reference	0.472		Reference
e1	1.00		Reference	0.0394		Reference
L	0.65	0.95		0.026	0.037	
N	52			52		

Q2

Section 6
Sales Offices, Representatives & Distributors

Sales Offices, Representatives and Distributors

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Printed in the USA Date of release: 05-93

9398 652 55011

98-8080-800 3089M/30M/FP/0693 476pp

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