PHILIPS

ICs for telephony

IC03 1987

PHILIPS

Data handbook

Electronic components and materials

Integrated circuits

Book IC03 1987

Integrated circuits for telephony

Bipolar, MOS

INTEGRATED CIRCUITS FOR TELEPHONY
BIPOLAR, MOS

DATA HANDBOOK SYSTEM

Our Data Handbook System comprises more than 60 books with specifications on electronic components, subassemblies and materials. It is made up of four series of handbooks:

ELECTRON TUBES	BLUE
SEMICONDUCTORS	RED
INTEGRATED CIRCUITS	PURPLE
COMPONENTS AND MATERIALS	GREEN

The contents of each series are listed on pages iv to vii.

The data handbooks contain all pertinent data available at the time of publication, and each is revised and reissued periodically.

When ratings or specifications differ from those published in the preceding edition they are indicated with arrows in the page margin. Where application information is given it is advisory and does not form part of the product specification.

Condensed data on the preferred products of Philips Electronic Components and Materials Division is given in our Preferred Type Range catalogue (issued annually).

Information on current Data Handbooks and on how to obtain a subscription for future issues is available from any of the Organizations listed on the back cover.
Product specialists are at your service and enquiries will be answered promptly.

ELECTRON TUBES (BLUE SERIES)

The blue series of data handbooks comprises:

T1 **Tubes for r.f. heating**

T2a **Transmitting tubes for communications, glass types**

T2b **Transmitting tubes for communications, ceramic types**

T3 **Klystrons**

T4 **Magnetrons for microwave heating**

T5 **Cathode-ray tubes**
Instrument tubes, monitor and display tubes, C.R. tubes for special applications

T6 **Geiger-Müller tubes**

T8 **Colour display systems**
Colour TV picture tubes, colour data graphic display tube assemblies, deflection units

T9 **Photo and electron multipliers**

T10 **Plumbicon camera tubes and accessories**

T11 **Microwave semiconductors and components**

T12 **Vidicon and Newvicon camera tubes**

T13 **Image intensifiers and infrared detectors**

T15 **Dry reed switches**

T16 **Monochrome tubes and deflection units**
Black and white TV picture tubes, monochrome data graphic display tubes, deflection units

SEMICONDUCTORS (RED SERIES)

The red series of data handbooks comprises:

S1 **Diodes**
Small-signal silicon diodes, voltage regulator diodes (< 1,5 W), voltage reference diodes, tuner diodes, rectifier diodes

S2a **Power diodes**

S2b **Thyristors and triacs**

S3 **Small-signal transistors**

S4a **Low-frequency power transistors and hybrid modules**

S4b **High-voltage and switching power transistors**

S5 **Field-effect transistors**

S6 **R.F. power transistors and modules**

S7 **Surface mounted semiconductors**

S8a **Light-emitting diodes**

S8b **Devices for optoelectronics**
Optocouplers, photosensitive diodes and transistors, infrared light-emitting diodes and infrared sensitive devices, laser and fibre-optic components

S9 **Power MOS transistors**

S10 **Wideband transistors and wideband hybrid IC modules**

S11 **Microwave transistors**

S12 **Surface acoustic wave devices**

S13 **Semiconductor sensors**

***S14** **Liquid Crystal Displays**

*To be issued shortly.

INTEGRATED CIRCUITS (PURPLE SERIES)

The NEW SERIES of handbooks is now completed. With effect from the publication date of this handbook the "N" in the handbook code number will be deleted.
Handbooks to be replaced during 1986 are shown below.

The purple series of handbooks comprises:

IC01	**Radio, audio and associated systems** Bipolar, MOS	new issue 1986 IC01N 1985
IC02a/b	**Video and associated systems** Bipolar, MOS	new issue 1986 IC02Na/b 1985
IC03	**Integrated circuits for telephony** Bipolar, MOS	new issue 1987 IC03N 1985
IC04	**HE4000B logic family** CMOS	new issue 1986 IC4 1983
IC05N	**HE4000B logic family — uncased ICs** CMOS	published 1984
IC06N	**High-speed CMOS; PC74HC/HCT/HCU** Logic family	published 1986
IC08	**ECL 10K and 100K logic families**	New issue 1986 IC08N 1984
IC09N	**TTL logic series**	published 1986
IC10	**Memories** MOS, TTL, ECL	new issue 1986 IC7 1982
IC11N	**Linear LSI**	published 1985
Supplement to IC11N	**Linear LSI**	published 1986
IC12	**I²C-bus compatible ICs**	not yet issued
IC13	**Semi-custom** Programmable Logic Devices (PLD)	new issue 1986 IC13N 1985
IC14N	**Microprocessors, microcontrollers and peripherals** Bipolar, MOS	published 1985
IC15	**FAST TTL logic series**	new issue 1986 IC15N 1985
IC16	**CMOS integrated circuits for clocks and watches**	first issue 1986
IC17	**Integrated Services Digital Networks (ISDN)**	not yet issued
IC18	**Microprocessors and peripherals**	new issue 1986*

* The Microprocessors were included in handbook IC14N 1985, so IC18 will replace that part of IC14N.

COMPONENTS AND MATERIALS (GREEN SERIES)

The green series of data handbooks comprises:

C2	Television tuners, coaxial aerial input assemblies, surface acoustic wave filters
C3	Loudspeakers
C4	Ferroxcube potcores, square cores and cross cores
C5	Ferroxcube for power, audio/video and accelerators
C6	Synchronous motors and gearboxes
C7	Variable capacitors
C8	Variable mains transformers
C9	Piezoelectric quartz devices
C11	Varistors, thermistors and sensors
C12	Potentiometers, encoders and switches
C13	Fixed resistors
C14	Electrolytic and solid capacitors
C15	Ceramic capacitors
C16	Permanent magnet materials
C17	Stepping motors and associated electronics
C18	Direct current motors
C19	Piezoelectric ceramics
C20	Wire-wound components for TVs and monitors
C22	Film capacitors

PREFACE

PREFACE

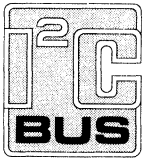
More than ten years on from our first dedicated ICs for telephony, the pace of progress in telecommunication continues to accelerate. An already-wide range of design possibilities offered by well established circuits and enhanced by new ICs has been dramatically extended in concepts that include microcontrollers linked to peripheral circuits via the two-wire I^2C (Inter-IC) data bus.

Telephony concepts range from simple pulse dialling to the most advanced feature-phones and from cordless telephones to cellular radio. The concepts include both bipolar and HCMOS ICs (with 2,5 V to 6 V operating voltage range) with most telephony ICs supplied in space-saving small-outline (SO) packages as well as standard DIL.

An Integrated Services Digital Network (ISDN) which allows transmission and reception of digitized voice, data and video signals is now in the final stages of development and we are well advanced in the development of a range of ICs with ISDN-Oriented Modular (IOM) architecture to form the vital interfaces between ISDN networks and the wide variety of subscriber terminals. We are also introducing the Integrated Services Terminal (IST) bus and associated ICs which are ISDN-compatible and allow up to 31 subscriber terminals to be interconnected via a simple, easy to install, twisted-pair cable. Specifications for IST bus and IOM ICs will be published separately.

SELECTION GUIDE

FUNCTIONAL INDEX



Purchase of Philips' I^2C components conveys a license under the Philips' I^2C patent to use the components in the I^2C-system provided the system conforms to the I^2C specifications defined by Philips.

NUMERICAL INDEX

PULSE DIALLER CIRCUITS WITH REDIAL, PCD332X FAMILY

functional survey		PCD							
		3320	3321	3322	3323	3324	3325A	3326	3327*
Number of pins		18	18	18	28	18	18	18	18
Dialling pulse frequency	10 Hz	●	●	●	●	●	●	●	●
selectable with F01, F02	16, 20 Hz		●		●	●	●	●	●
Mark/space ratio	3:2	●	●	●	●	●	●	●	●
selectable with M/S	2:1		●		●	●	●		●
Inter-digit pause duration	8 x T_{DP}	●	●	●	●	●	●	●	●
selectable with IDP	9 x T_{DP}				●				
Reset delay for line power breaks	1,6 x T_{DP}	●	●	●	●	●	●	●	●
selectable with RDS	3,2 x T_{DP}				●				
Access pauses repeated during redial			●		●	●	●	●	●
Manual insertion of access pauses			●		●	●	●	●	●
Automatic access pause insertion	1 max.					●			
	2 max.		●		●			●	
Access pause duration	32 x T_{DP}		●		●	●		●	
selectable with APD	64 x T_{DP}				●			●	
not automatically terminated							●		●
$\overline{M1}$, inverted mute output		●		●	●				
M2, strobe output				●	●				
M3, AND function of mute (M1) and inverted dialling pulse (DP) outputs		●			●				
CL, clock output					●				
APO, access pause output					●				
HOLD, dialling-interrupt input		●		●	●				
APO + HOLD, internally connected			●			●	●	●	●
APR, access pause reset input					●				
AAE, automatic access pause enable					●				

T_{DP} = dialling pulse period.
* PCD3327 for ceramic resonator.

Features common to all PCD332X family

OSC IN, OSC OUT } on-chip oscillator input and output
C1 to C3, column keyboard inputs with on-chip pull down
R1 to R4, row keyboard inputs with on-chip pull-up
CE, chip enable input
DP, dialling pulse drive output to external line-switching transistor or relay
M1, mute output

SPEECH/TRANSMISSION CIRCUITS, TEA1060 FAMILY

functional survey	TEA				
	1060	1061	1066T	1067	1068
Microphone inputs:					
low sensitivity; dynamic or magnetic	●		●	●	●
medium sensitivity; dynamic or magnetic	●		●	●	●
eletret with preamplifier		●	●	●	●
piezo-electric		●	●	●	●
Receiver outputs:					
dynamic or magnetic	●	●	●	●	●
piezo-electric	●	●	●	●	●
Electronic mute input	●	●	●	●	●
DTMF input	●	●	●	●	●
Voltage regulator:					
adjustable d.c. voltage	●	●	●	●	●
adjustable d.c. resistance	●	●	●	●	●
Power-down input	●	●	●	●	●
Gain control:					
control can be switched-off	●	●	●	●	●
adaptable to exchange voltage and impedance	●	●	●	●	●
SO encapsulation			●	●	●
Parallel operation possible				●	

MICROCONTROLLERS FOR TELEPHONE SETS

type number of family	short description	type number of standard version	type number or customized version
PCD3343	dedicated single-chip, 8-bit microcontroller for telephone sets; available in standard or customized versions; 3K x 8 ROM; 224 x 8 RAM	PCD3341	PCD3343/0XX
PCD3315C	dedicated single-chip, 8-bit microcontroller for telephone sets; available in standard or customized versions; 1,5K x 8 ROM; 160 x 8 RAM	PCD3315/502 PCD3315/503	PCD3315/5XX

ARCHITECTURE OF ELECTRONIC SUBSCRIBER SETS

Telephones for pulse dialling

Telephones for DTMF dialling

ARCHITECTURE OF ELECTRONIC SUBSCRIBER SETS

The path to electronic operation

The first step in converting subscriber sets to electronic operation is usually in the replacement of the rotary dial by a push-button keyboard which operates either with a pulse generator for interrupted current-loop dialling, or with a tone generator for DTMF dialling (this division of techniques has resulted in two main streams of telephone production; pulse dialling and tone dialling). Subsequent steps for improvement are in the replacement of the carbon microphone by an active transducer such as an electret or electro-dynamic microphone, and replacement of the transformer hybrid by an integrated speech/transmission circuit. The sequence continues with the inclusion of features such as repertory dialling, last-number redial, extended redial, dialled number display, and tarif-unit metering. Some sets may also have the capability of either pulse or DTMF dialling.

The ringer is a completely separate function and can therefore be replaced by electronics at any stage.

Basic telephones for pulse dialling

Figs 1, 2 and 3 show the architecture of basic push-button subscriber sets for interrupted current-loop dialling using ICs from the PCD332X family.

In Fig. 1 an insert unit to perform the dial function is shown in a conventional set with a transformer hybrid. A muting relay inhibits the speech function during dialling.

Fig. 2 shows a parallel circuit in which the line current flows through either the speech part or a dummy load and is interrupted by the M3 output of the dialling IC. Note that the conventional speech circuit operating with two wires may be replaced by a speech/transmission circuit (from the TEA1060 family). This allows the possibility of operating the speech IC in the handset with only a two-wire cable.

In Fig. 3 the dialling IC operates in conjunction with a transmission IC with common-line interface. The latter works with any kind of microphone and earpiece and has a special input for muting. For this function we have a family of speech/transmission ICs (the TEA1060 family).

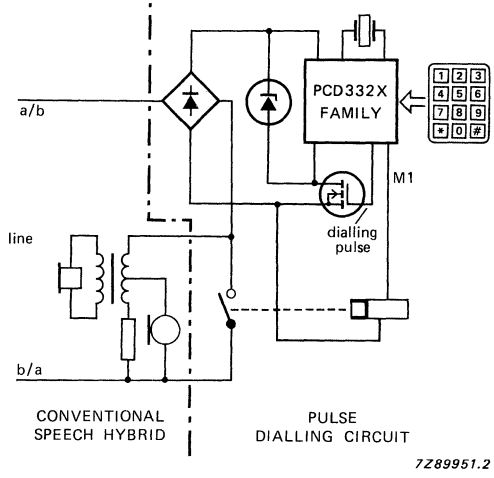


Fig. 1 Pulse dial insert unit replacing the rotary dial in a conventional telephone set.

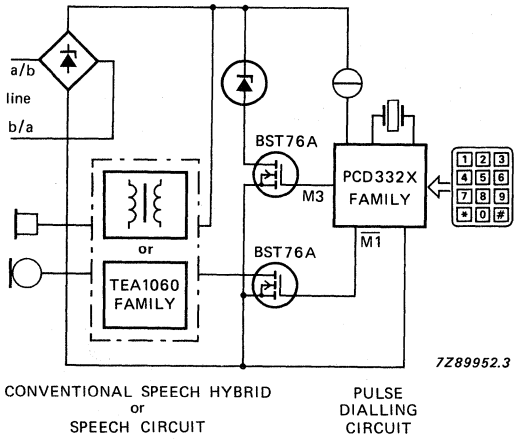


Fig. 2 Pulse dial basic set with either conventional or electronic speech.

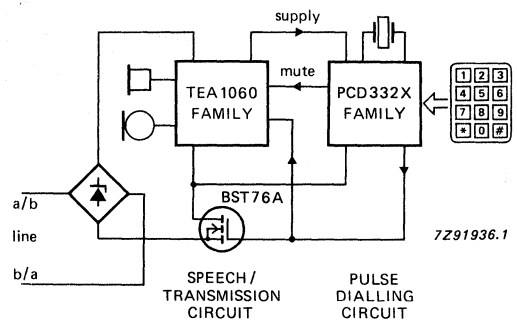


Fig. 3 Pulse dial basic set with two ICs and common line interface.

Basic telephones for DTMF dialling

Figs 4, 5, 6 and 7 show the architecture of four basic push-button sets for DTMF dialling.

In Fig. 4 a conventional speech circuit with a transformer hybrid is used together with a DTMF generator; this requires a DTMF generator which has an output stage, line interface and mute switch.

Fig. 5 shows the same DTMF generator applied with an electronic speech circuit. Both DTMF generator and speech circuit have interfaces to the line.

In Fig. 6 only the speech circuit interfaces to the line. The DTMF generator is connected to the speech circuit which has a DTMF and a mute input for this purpose. The speech circuit incorporates a voltage stabilizer and audio output stage for both speech and DTMF signals. Note that the speech ICs in this application are the same as used for the pulse dial application shown in Fig. 3.

The application of a combined DTMF/transmission circuit (TEA1046) is shown in Fig. 7.

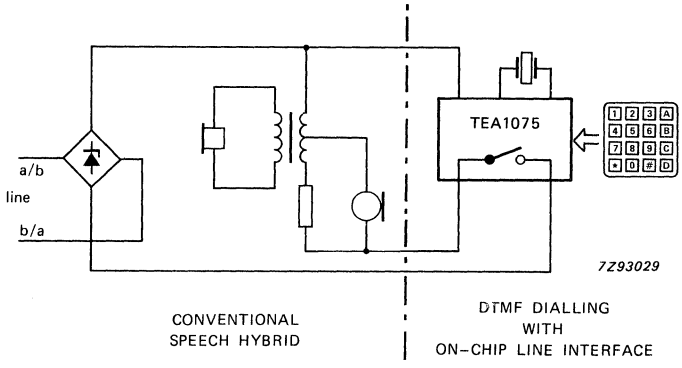


Fig. 4 DTMF set using a conventional speech circuit.

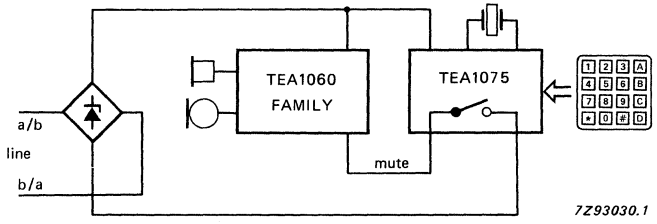


Fig. 5 Full electronic DTMF set.

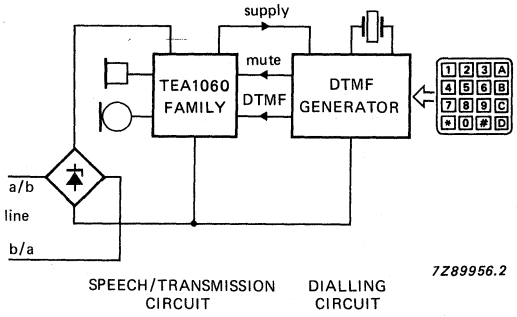


Fig. 6 DTMF basic set with two ICs and common line interface.

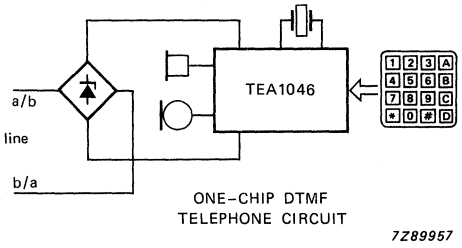


Fig. 7 Electronic speech and DTMF on a single chip.

Basic telephones for both pulse and DTMF dialling

The architecture of a push-button subscriber set for both pulse and DTMF dialling is shown in Fig. 8. This concept includes last-number redial and flash. The speech circuit is the only part interfacing with the line, the dialler circuit being connected via the DTMF, mute and power-down pins.

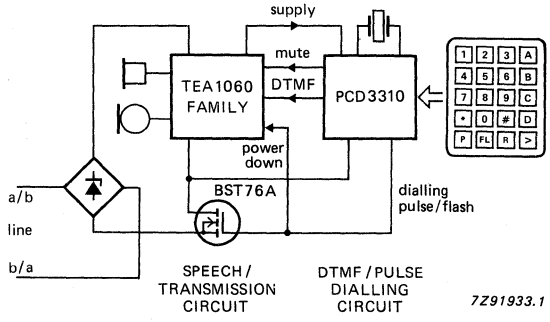


Fig. 8 Subscriber set architecture for pulse and DTMF dialling.

Feature telephones

The subscriber set shown in Fig. 9 has added features including last-number redial, extended redial, repertory dialling and register recall. It is constructed around the PCD3315C telephone microcontroller and a PCD3312 DTMF generator. Pre-programmed versions of the PCD3315C are available (PCD3315/502 and PCD3315/503).

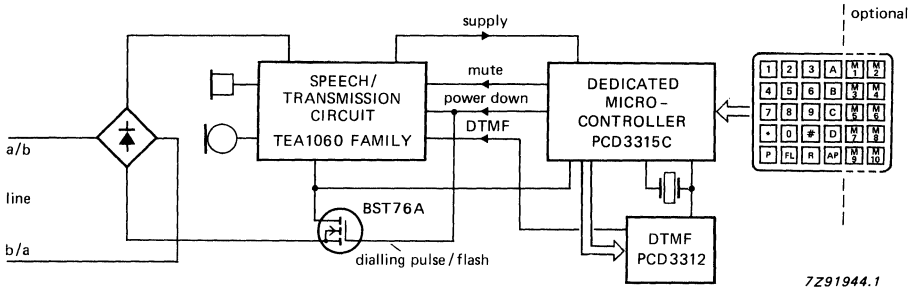


Fig. 9 Feature telephone using a dedicated microcontroller (PCD3315C).

Even more features can be obtained by using the telephone microcontroller PCD3343. This interfaces with the I^2C bus – a two-wire serial input/output data bus – which allows peripheral devices to be added. An example of this is shown in Fig. 10 with the additions of a larger repertory dial memory and dialled number display. In this way, up to eight CMOS RAMs (PCF8571) can be used to augment the on-chip storage capacity of the PCF3343 (ten 16-digit numbers). Other additions can be an LCD driver (PCF8576 or PCF8577), a clock/timer circuit (PCF8573) and DTMF generator (PCD3312). There is also a DTMF generator (PCD3311) which operates with a 4 or 8-bit microcontroller, and a pre-programmed version of the PCD3343 which is available under the type number PCD3341.

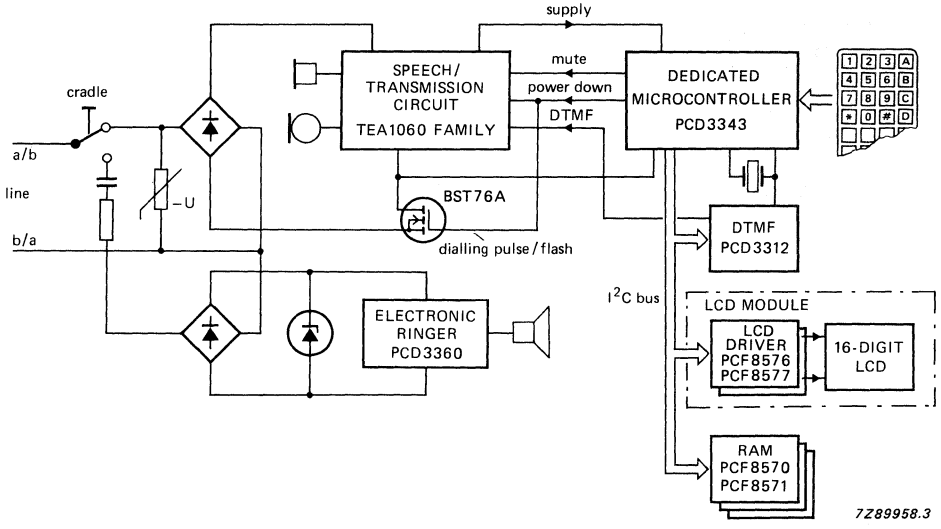


Fig. 10 Feature-phone using dedicated microcontroller PCD3343.

Fig. 11 shows an application in which a general-purpose microcomputer or a personal computer with parallel input/output can be used in conjunction with the TEA1046 DTMF/speech/transmission IC (this has microcomputer-compatible keyboard inputs).

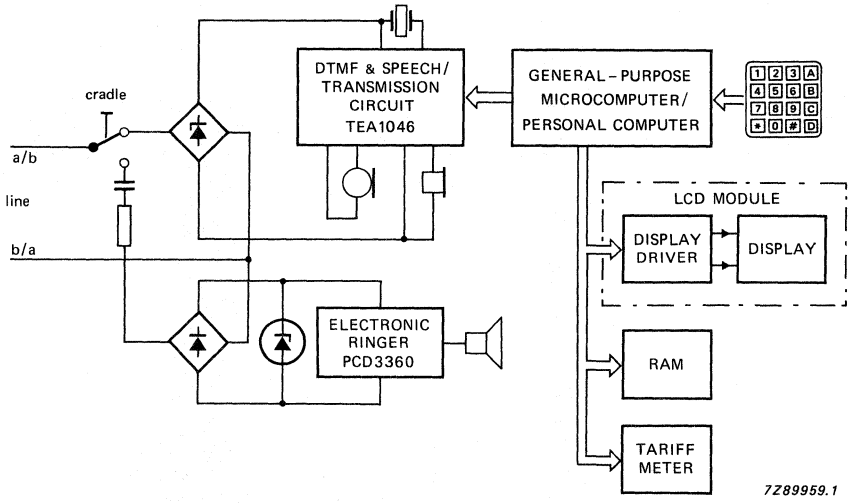


Fig. 11 Application utilizing a general-purpose microcomputer with parallel input/output.

Loudspeaking facilities

A simple but effective audio amplifier is shown in Fig. 12. The peripheral supply circuit (TEA1080) uses the line input to power the loudspeaker amplifier (TDA7050) and other peripheral devices if required. The TDA7050 is a dual-channel amplifier making either single-ended or bridge-tied load (BTL) configurations possible.

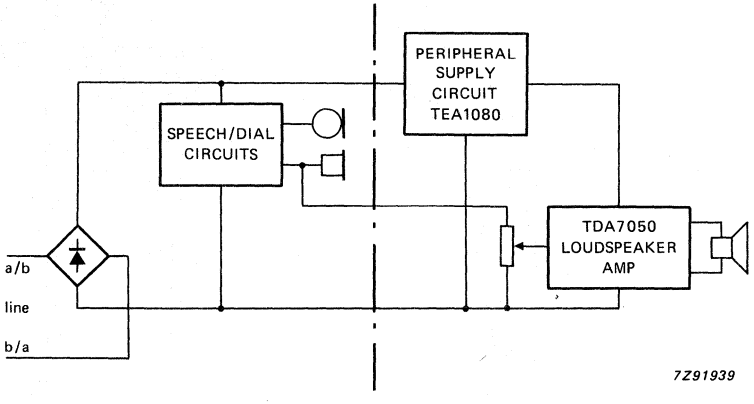
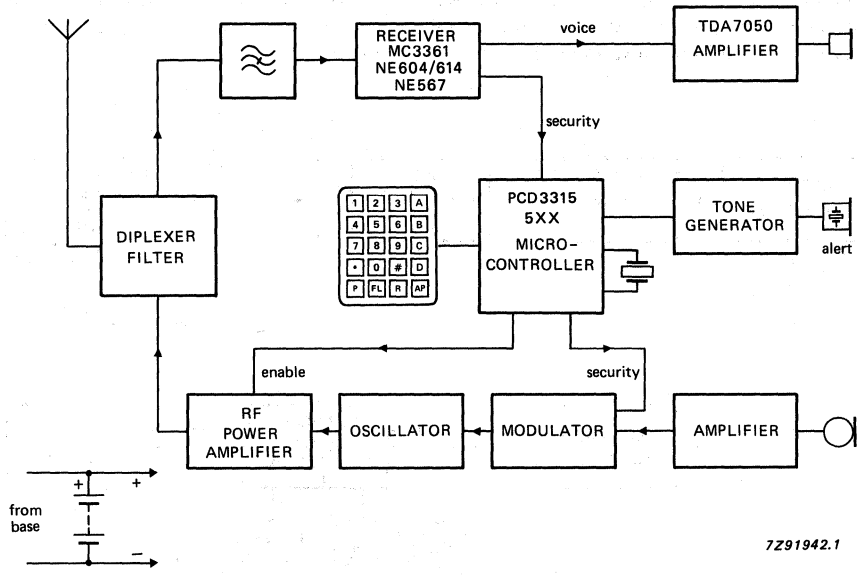


Fig. 12 Audio power amplifier for loudspeaking.

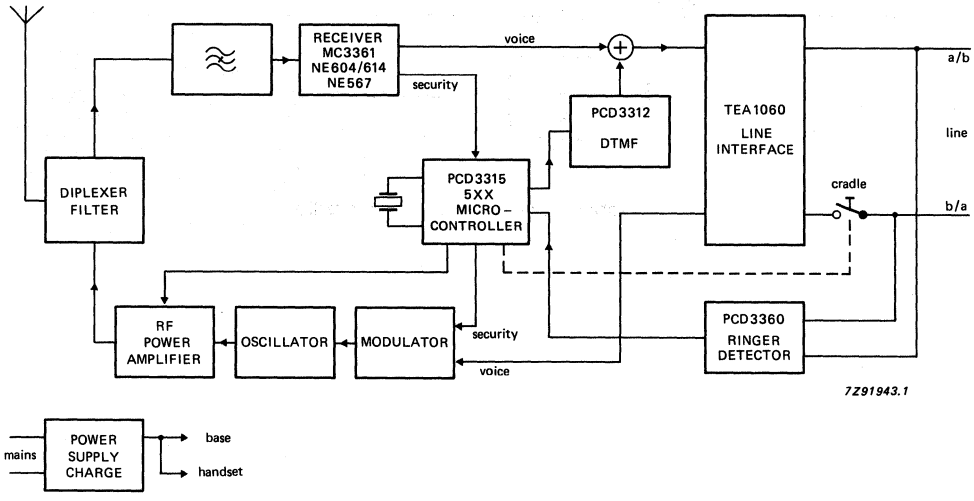
Cordless telephones

Our dedicated ICs for telephony will enhance any attractive mobile telephone design. The cordless telephone concept shown in Fig. 13 operates with carrier frequencies of 46/49 MHz (FCC standards) and incorporates a security code system to protect transmissions between base and remote units.

The base and the remote units both utilize the single-chip FM radio receiver (MC3361) which requires few external components and is simple to align. A pilot tone is used to separate voice and data, detection of the pilot tone is implemented with our tone decoder SE/NE567. Also both units use the dedicated microcontroller (PCD3315) which, as well as the standard dialling functions, provides the two-way, 16-bit, random-generated, security code system. In DTMF systems, the PCD3315 will control a PCD3312 dialler. The voice output of the remote unit is driven by earpiece/loudspeaker amplifier TDA7050. In the base unit the TEA1060 provides the line interface for the speech/transmission part and the PCD3360 detects the ringer voltage.



(a) Remote unit.



(b) Base unit.

Fig. 13 Advanced cordless telephone.

Cellular radio

Cellular mobile communications systems employ hybrid technologies that bring together analogue voice processing and digital data communications. As can be seen in Fig. 14, our integrated circuits fulfill many of the vital functions required for mobile equipment of the new era.

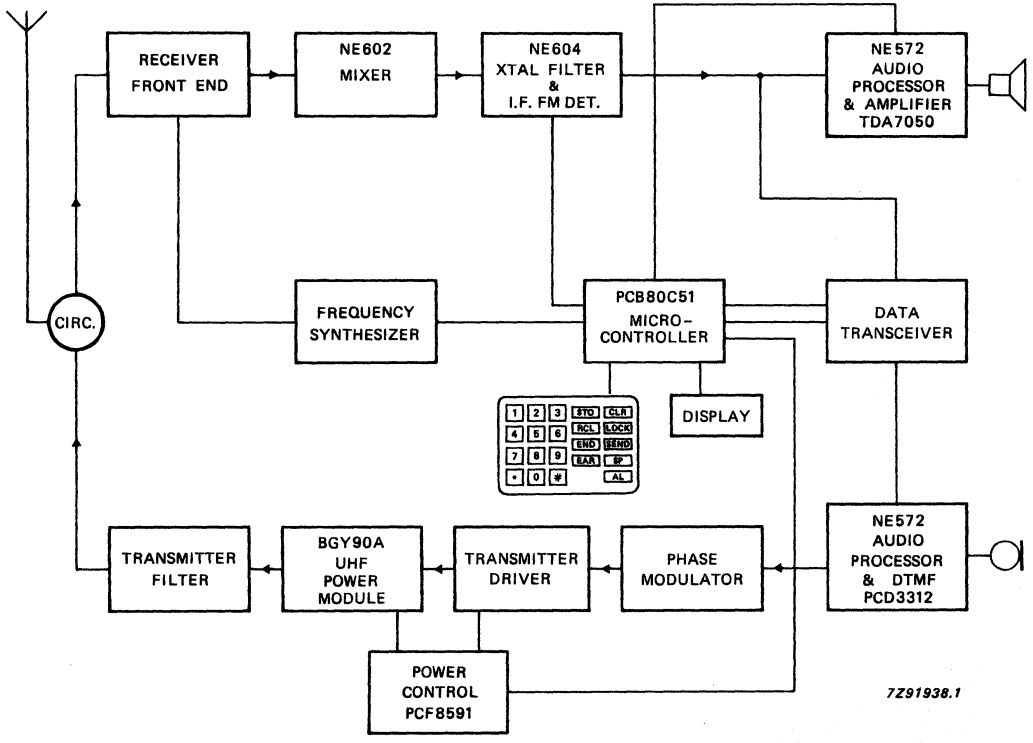


Fig. 14 Mobile transceiver for cellular radio.

GENERAL

Product status definitions

for type numbers with prefixes MC, NE, SA, SE

Ordering information

for type numbers with prefixes MC, NE, SA, SE

Type designation

for type numbers with prefixes MEA, PCB, PCD, PCF, TDA, TEA

Rating systems

for type numbers with prefixes MEA, PCB, PCD, PCF, TDA, TEA

Handling MOS devices

DEFINITIONS		
Data Sheet Identification	**Product Status**	**Definition**
Objective Specification	**Formative or In Design**	This data sheet contains the design target or goal specifications for product development. Specifications may change in any manner without notice.
Preliminary Specification	**Preproduction Product**	This data sheet contains preliminary data and supplementary data will be published at a later date. Signetics reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product Specification	**Full Production**	This data sheet contains Final Specifications. Signetics reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

ORDERING INFORMATION

Signetics' Linear LSI integrated circuit products may be ordered by contacting either the local Signetics sales office, Signetics representatives and/or Signetics authorized distributors. A complete listing is located in the back of this manual.

Minimum Factory Order:

Commercial Product:
$1000 per order
$250 per line item per order

Military Product:
$250 per line item per order

Table 1 provides part number information concerning Signetics originated products.

Table 2 is a cross reference of both the old and new package suffixes for all presently existing types, while Tables 3 and 4 provide appropriate explanations on the various prefixes employed in the part number descriptions.

As noted in Table 3, Signetics defines device operating temperature range by the appropriate prefix. It should be noted, however, that devices with a SE prefix (– 55°C to + 125°C) indicates only its operating temperature range and *not* its military qualification status. The military qualification status of any Linear LSI product can be determined by either looking in the Military Section in this manual and/or contacting your local sales office.

Table 1 PART NUMBER DESCRIPTION

PART NUMBER	CROSS REF PART NO.	PRODUCT FAMILY	PRODUCT DESCRIPTION
NE5537N	LF398	LIN	Sample & Hold Amp

NE5537N
- LF398 → Product Family: LIN Analog Products, MIL Military Products
- Sample & Hold Amp → Description of Product Function
- N → Package Descriptions—See Table 2
- 37 → Device Number
- NE → Device Family and Temperature Range Prefix—See Tables 3 & 4

Table 2 PACKAGE DESCRIPTIONS

Old	New	PACKAGE DESCRIPTION
A,AA	N	14-lead plastic DIL
A	N-14	14-lead plastic DIL (Selected Analog products only)
B,BA	N	16-lead plastic DIL
-	D	Microminiature package (SO)
F	F	14, 16, 18, 22 and 24-lead ceramic (Cerdip) DIL
I,IK	I	14, 16, 18, 22, 28 and 4-lead ceramic DIL
K	H	10-lead TO-100
L	H	10-lead high-profile TO-100 can
NA,NX	N	24-lead plastic DIL
Q,R	Q	10, 14, 16 and 24-lead ceramic flat
T,TA	H	8-lead TO-99
U	U	SIL Plastic power
V	N	8-lead plastic DIL
XA	N	18-lead plastic DIL
XC	N	20-lead plastic DIL
XC	N	22-lead plastic DIL
XL,XF	N	28-lead plastic DIL

Table 3 SIGNETICS PREFIX AND DEVICE TEMPERATURE

PREFIX	DEVICE TEMPERATURE RANGE
N	0° to + 70°C
S	– 55° to + 125°C
NE	0° to + 70°C
SE	– 55° to + 125°C
SA	– 40° to + 85°C

Table 4 INDUSTRY STANDARD PREFIX

PREFIX	DEVICE FAMILY
AM	Linear Industry Standard
CA	Linear Industry Standard
DAC	Linear Industry Standard
JB	Mil Rel—Jan Qualified—Old Designator
JM	Mil Rel—Jan Qualified—New Designator
LF	Linear Industry Standard
LM	Linear Industry Standard
M	Mil Rel—Jan Processed
MC	Linear Industry Standard
NE	Linear Industry Standard
SA	Linear Industry Standard
SE	Linear Industry Standard
SG	Linear Industry Standard
μA	Linear Industry Standard
ULN	Linear Industry Standard

PRO ELECTRON TYPE DESIGNATION CODE FOR INTEGRATED CIRCUITS

This type nomenclature applies to semiconductor monolithic, semiconductor multi-chip, thin-film, thick-film and hybrid integrated circuits.

A basic number consists of:

THREE LETTERS FOLLOWED BY A SERIAL NUMBER

FIRST AND SECOND LETTER

1. DIGITAL FAMILY CIRCUITS

   The FIRST TWO LETTERS identify the FAMILY (see note 1).

2. SOLITARY CIRCUITS

   The FIRST LETTER divides the solitary circuits into:

   S : Solitary digital circuits
   T : Analogue circuits
   U : Mixed analogue/digital circuits

   The SECOND LETTER is a serial letter without any further significance except 'H' which stands for hybrid circuits.

3. MICROPROCESSORS

   The FIRST TWO LETTERS identify microprocessors and correlated circuits as follows:

   MA : { Microcomputer / Central processing unit
   MB : Slice processor (see note 2)
   MD : Correlated memories
   ME : Other correlated circuits (interface, clock, peripheral controller, etc.)

4. CHARGE-TRANSFER DEVICES AND SWITCHED CAPACITORS

   The FIRST TWO LETTERS identify the following:

   NH : Hybrid circuits
   NL : Logic circuits
   NM : Memories
   NS : Analogue signal processing, using switched capacitors
   NT : Analogue signal processing, using CTDs
   NX : Imaging devices
   NY : Other correlated circuits

Notes

1. A logic family is an assembly of digital circuits designed to be interconnected and defined by its basic electrical characteristics (such as: supply voltage, power consumption, propagation delay, noise immunity).
2. By 'slice processor' is meant: a functional slice of microprocessor.

THIRD LETTER

It indicates the operating ambient temperature range.
The letters A to G give information about the temperature:

A : temperature range not specified
B : 0 to + 70 °C
C : −55 to + 125 °C
D : −25 to + 70 °C
E : −25 to + 85 °C
F : −40 to + 85 °C
G : −55 to + 85 °C

If a circuit is published for another temperature range, the letter indicating a narrower temperature range may be used or the letter 'A'.

Example: the range 0 to + 75 °C can be indicated by 'B' or 'A'.

SERIAL NUMBER

This may be either a 4-digit number assigned by Pro Electron, or the serial number (which may be a combination of figures and letters) of an existing company type designation of the manufacturer.

To the basic type number may be added:

A VERSION LETTER

Indicates a minor variant of the basic type or the package. Except for 'Z', which means customized wiring, the letter has no fixed meaning. The following letters are recommended for package variants:

C : for cylindrical
D : for ceramic DIL
F : for flat pack
L : for chip on tape
P : for plastic DIL
Q : for QIL
T : for miniature plastic (mini-pack)
U : for uncased chip

Alternatively a TWO LETTER SUFFIX may be used instead of a single package version letter, if the manufacturer (sponsor) wishes to give more information.

FIRST LETTER: General shape

C : Cylindrical
D : Dual-in-line (DIL)
E : Power DIL (with external heatsink)
F : Flat (leads on 2 sides)
G : Flat (leads on 4 sides)
K : Diamond (TO-3 family)
M : Multiple-in-line (except Dual-, Triple-, Quadruple-in-line)
Q : Quadruple-in-line (QIL)
R : Power QIL (with external heatsink)
S : Single-in-line
T : Triple-in-line

SECOND LETTER: Material

C : Metal-ceramic
G : Glass-ceramic (cerdip)
M : Metal
P : Plastic

A hyphen precedes the suffix to avoid confusion with a version letter.

RATING SYSTEMS

The rating systems described are those recommended by the International Electrotechnical Commission (IEC) in its Publication 134.

DEFINITIONS OF TERMS USED

Electronic device. An electronic tube or valve, transistor or other semiconductor device.

Note
This definition excludes inductors, capacitors, resistors and similar components.

Characteristic. A characteristic is an inherent and measurable property of a device. Such a property may be electrical, mechanical, thermal, hydraulic, electro-magnetic, or nuclear, and can be expressed as a value for stated or recognized conditions. A characteristic may also be a set of related values, usually shown in graphical form.

Bogey electronic device. An electronic device whose characteristics have the published nominal values for the type. A bogey electronic device for any particular application can be obtained by considering only those characteristics which are directly related to the application.

Rating. A value which establishes either a limiting capability or a limiting condition for an electronic device. It is determined for specified values of environment and operation, and may be stated in any suitable terms.

Note
Limiting conditions may be either maxima or minima.

Rating system. The set of principles upon which ratings are established and which determine their interpretation.

Note
The rating system indicates the division of responsibility between the device manufacturer and the circuit designer, with the object of ensuring that the working conditions do not exceed the ratings.

ABSOLUTE MAXIMUM RATING SYSTEM

Absolute maximum ratings are limiting values of operating and environmental conditions applicable to any electronic device of a specified type as defined by its published data, which should not be exceeded under the worst probable conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device, taking no responsibility for equipment variations, environmental variations, and the effects of changes in operating conditions due to variations in the characteristics of the device under consideration and of all other electronic devices in the equipment.

The equipment manufacturer should design so that, initially and throughout life, no absolute maximum value for the intended service is exceeded with any device under the worst probable operating conditions with respect to supply voltage variation, equipment component variation, equipment control adjustment, load variations, signal variation, environmental conditions, and variations in characteristics of the device under consideration and of all other electronic devices in the equipment.

DESIGN MAXIMUM RATING SYSTEM

Design maximum ratings are limiting values of operating and environmental conditions applicable to a bogey electronic device of a specified type as defined by its published data, and should not be exceeded under the worst probable conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device, taking responsibility for the effects of changes in operating conditions due to variations in the characteristics of the electronic device under consideration.

The equipment manufacturer should design so that, initially and throughout life, no design maximum value for the intended service is exceeded with a bogey device under the worst probable operating conditions with respect to supply voltage variation, equipment component variation, variation in characteristics of all other devices in the equipment, equipment control adjustment, load variation, signal variation and environmental conditions.

DESIGN CENTRE RATING SYSTEM

Design centre ratings are limiting values of operating and environmental conditions applicable to a bogey electronic device of a specified type as defined by its published data, and should not be exceeded under normal conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device in average applications, taking responsibility for normal changes in operating conditions due to rated supply voltage variation, equipment component variation, equipment control adjustment, load variation, signal variation, environmental conditions, and variations in the characteristics of all electronic devices.

The equipment manufacturer should design so that, initially, no design centre value for the intended service is exceeded with a bogey electronic device in equipment operating at the stated normal supply voltage.

HANDLING MOS DEVICES

Though all our MOS integrated circuits incorporate protection against electrostatic discharges, they can nevertheless be damaged by accidental over-voltages. In storing and handling them, the following precautions are recommended.

Caution

Testing or handling and mounting call for special attention to personal safety. Personnel handling MOS devices should normally be connected to ground via a resistor.

Storage and transport

Store and transport the circuits in their original packing. Alternatively, use may be made of a conductive material or special IC carrier that either short-circuits all leads or insulates them from external contact.

Testing or handling

Work on a conductive surface (e.g. metal table top) when testing the circuits or transferring them from one carrier to another. Electrically connect the person doing the testing or handling to the conductive surface, for example by a metal bracelet and a conductive cord or chain. Connect all testing and handling equipment to the same surface.
Signals should not be applied to the inputs while the device power supply is off. All unused input leads should be connected to either the supply voltage or ground.

Mounting

Mount MOS integrated circuits on printed circuit boards *after* all other components have been mounted. Take care that the circuits themselves, metal parts of the board, mounting tools, and the person doing the mounting are kept at the same electric (ground) potential. If it is impossible to ground the printed-circuit board the person mounting the circuits should touch the board before bringing MOS circuits into contact with it.

Soldering

Soldering iron tips, including those of low-voltage irons, or soldering baths should also be kept at the same potential as the MOS circuits and the board.

Static charges

Dress personnel in clothing of non-electrostatic material (no wool, silk or synthetic fibres). After the MOS circuits have been mounted on the board proper handling precautions should still be observed. Until the sub-assemblies are inserted into a complete system in which the proper voltages are supplied, the board is no more than an extension of the leads of the devices mounted on the board. To prevent static charges from being transmitted through the board wiring to the device it is recommended that conductive clips or conductive tape be put on the circuit board terminals.

Transient voltages

To prevent permanent damage due to transient voltages, do not insert or remove MOS devices, or printed-circuit boards with MOS devices, from test sockets or systems with power on.

Voltage surges

Beware of voltage surges due to switching electrical equipment on or off, relays and d.c. lines.

DEVICE DATA

Low Power FM IF

Linear Products

DESCRIPTION

The MC3361 is a monolithic low-power FM IF signal processing system consisting of an oscillator, mixer, limiting amplifier, quadrature detector, filter amplifier, squelch, scan control and mute switch. It is intended for use in narrow band FM dual conversion communications equipment. The MC3361 is available in a 16-lead, dual-in-line plastic package and 16-lead SO (surface-mounted miniature package).

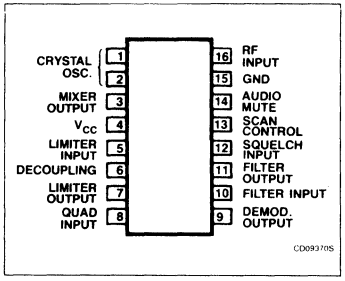
FEATURES

- **2.0V to 8.0V operation**
- **Low current: 4.2mA typ at V_{CC} = 4.0V_{DC}**
- **Excellent sensitivity: 2.0μV for −3dB limiting typ**
- **Low external parts count**
- **Operation to 60MHz**

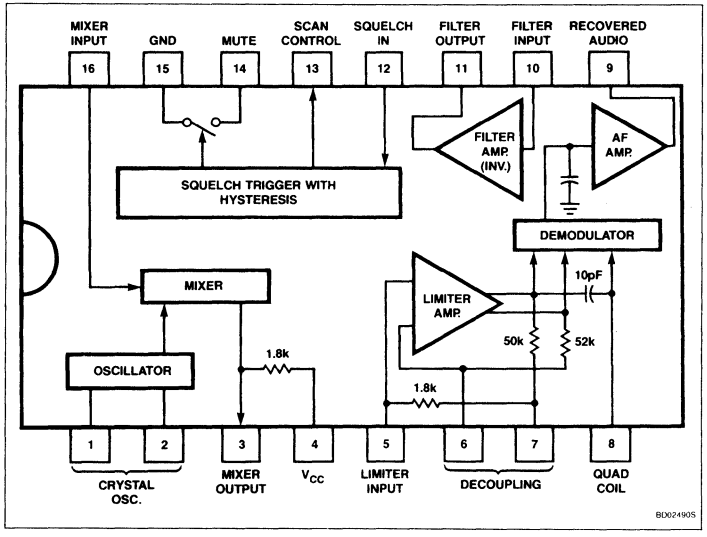
APPLICATIONS

- **Cordless telephone**
- **Narrow band receivers**
- **Remote control**

PIN CONFIGURATION



BLOCK DIAGRAM



ORDERING CODE

DESCRIPTION	ORDER CODE
Plastic; 0 to +70°C	MC3361N
Plastic; SO (surface-mounted miniature package); 0 to +70°C	MC3361D

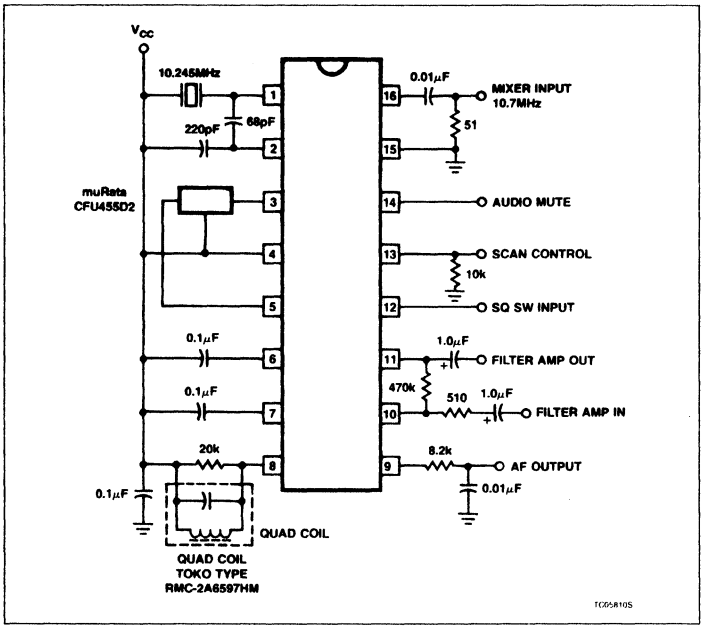
ABSOLUTE MAXIMUM RATINGS (T_A = 25°C, unless otherwise noted)

SYMBOL	PARAMETER	PIN	RATING	UNIT
V_{CC} (Max)	Power supply voltage	4	10	V_{DC}
V_{CC}	Generating supply voltage range	4	2.0 to 8.0	V_{DC}
	Detector input voltage	8	1.0	V_{P-P}
V_{16}	Input voltage ($V_{CC} \geq 4.0V$)	16	1.0	V_{RMS}
V_{14}	Mute function	14	−0.5 to 5.0	V_{PK}
T_J	Junction temperature		150	°C
T_A	Operating ambient temperature range		−30 to +75	°C
T_{STG}	Storage temperature range		−65 to +150	°C

AC & DC ELECTRICAL CHARACTERISTICS (V_{CC} = 4.0V_{DC}, f_O = 10.7MHz, Δf = ±3.0kHz, f_{MOD} = 1.0kHz, T_A = 25°C unless otherwise noted.)

PARAMETER	PIN	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
Drain current (no signal) Squelch off Squelch on	4			 4.2 5.4	 7.0 9.0	mA
Input limiting voltage	16	−3.0dB limiting		2.0	6.0	μV
Detector output voltage	9			2.0		V_{DC}
Detector output impedance				450		Ω
Recovered audio output voltage	9	V_{IN} = 10mV_{RMS}	100	150	270	mV_{RMS}
Filter gain (10kHz)		V_{IN} = 1.0mV_{RMS}	40	46		dB
Filter output voltage	11			1.7		V_{DC}
Trigger hysteresis				50		mV
Mute function low	14			10		Ω
Mute function high	14			10		MΩ
Scan function low (mute off)	13	V_{12} = 1.0V_{DC}			0.5	V_{DC}
Scan function high (mute on)	13	V_{12} = GND	3.5			V_{DC}
Mixer conversion gain	3			27		dB
Mixer input resistance	16			3.6		kΩ
Mixer input capacitance	16			2.2		pF

TEST CIRCUIT



VOICE SYNTHESIZER

GENERAL DESCRIPTION

The MEA8000 is a 24-pin N-MOS integrated circuit for generating good quality speech from digital code with a programmable bit rate. The circuit is primarily intended for applications in microprocessor controlled systems, where the speech code is stored separately.

Features

- Interfaces easily with most popular microprocessors and microcomputer
- 8-bit wide data bus
- 32-bit wide data buffer holding speech frame codes
- Digital filter of 8th order with 3 programmable formant frequencies, one fixed formant frequency, and 4 programmable formant bandwidths
- Programmable amplitudes
- Programmable duration of each frame; 8, 16, 32 or 64 ms
- Synthesis occupies less than 1% of control processor time
- Capable of sophisticated unvoiced sound generation
- Crystal controlled oscillator or external (TTL) clock
- Minimal external audio filter requirement
- Single + 5 V power supply

QUICK REFERENCE DATA

parameter	condition	symbol	min.	typ.	max.	unit
Supply voltage	pin 13	V_{DD}	4,5	5,0	5,5	V
Supply current	no audio load	I_{DD}	–	30	50	mA
Inputs						
Input voltage	HIGH	V_{IH}	2,0	–	V_{DD}	V
Input voltage	LOW	V_{IL}	−0,5	–	0,8	V
Input capacitance		C_I	–	–	7	pF
Outputs						
Output voltage	$-I_{OH}$ = 100 μA	V_{OH}	2,4	–	–	V
Output voltage	I_{OL} = 1,6 mA	V_{OL}	–	–	0,4	V
Capacitance		C_L	–	–	30	pF
Operating ambient temperature range		T_{amb}	0	–	+ 70	°C

PACKAGE OUTLINE

24-lead DIL; plastic (SOT-101A).

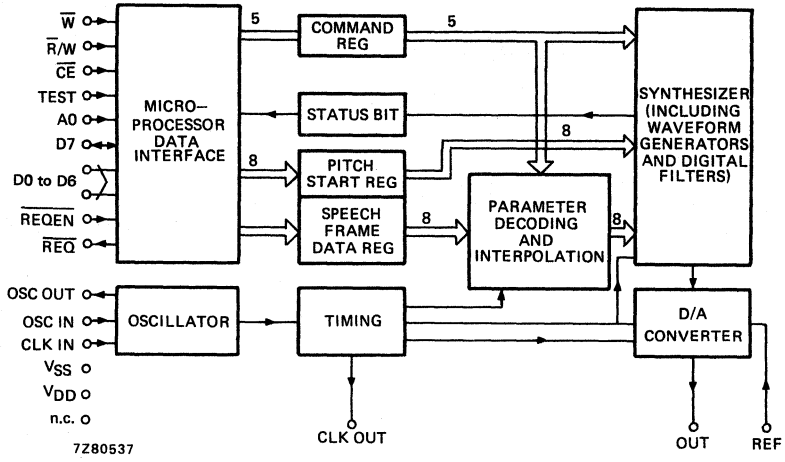


Fig. 1 Block diagram.

PINNING

1	V_{SS}	ground
2	$\overline{REQ}$	data request
3	D7	data bus
4	D6	
5	D5	
6	D4	
7	D3	
8	D2	
9	D1	
10	D0	
11	A0	data/control input
12	$\overline{CE}$	chip enable
13	V_{DD}	supply voltage
14	$\overline{REQEN}$	request enable input
15	N.C.	not connected
16	OSC IN	internal oscillator
17	OSC OUT	
18	CLK IN	clock input
19	REF	reference current
20	OUT	speech output
21	CLK OUT	internal clock output
22	$\overline{R}/W$	read/write
23	$\overline{W}$	write
24	TEST	test use only

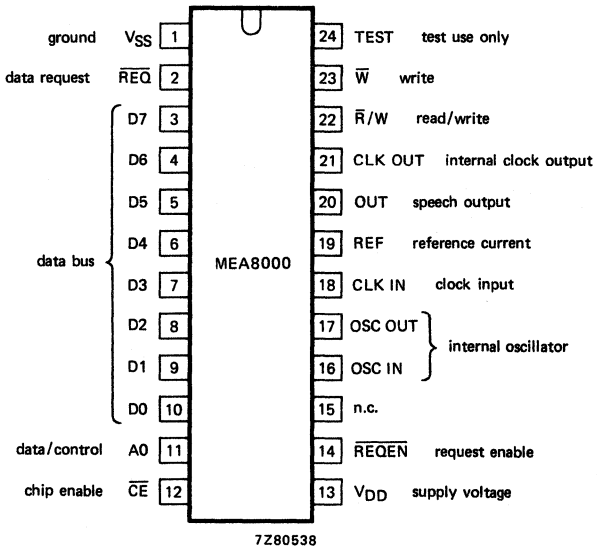


Fig. 2 Pinning diagram.

FUNCTIONAL DESCRIPTION (pin number)

Control

D0 to D7	(10 to 3)	Data bus to which command or speech can be written.
D7	(3)	Data port via which the status can be read.
$\overline{CE}$	(12)	Chip enable (chip select).
$\overline{W}$	(23)	Write.
$\overline{R}$/W	(22)	Read/Write The control signals $\overline{W}$ and $\overline{R}$/W allow connections to most microcomputers or microprocessors (see timing diagrams).
A0	(11)	Data/control input: discriminates between speech code input buffer (A0 = '0') and command register (A0 = '1') during a 'write' operation.
$\overline{REQ}$	(2)	Data request (open drain output); output signal which follows inverse of the status REQ bit, but only if enabled by either the ROE bit in the command register or the external $\overline{REQEN}$ pin.
$\overline{REQEN}$	(14)	Request enable input; $\overline{REQEN}$ = '0' enables the status REQ output, independent of the status of the command register.

Timing

OSC IN	(16)	Connections for internal clock oscillator; nominal crystal frequency 4 MHz.
OSC OUT	(17)	
CLK IN	(18)	Clock input for external clock, TTL compatible, 4 MHz.
CLK OUT	(21)	A buffered output for the internal clock cycle (which is equal to CLK divided by 3). May be used as a clock, for a microprocessor, for example.

Output

REF	(19)	Input pin for biasing the audio output level. This reference current can be derived from a resistor to the positive supply.
OUT	(20)	Speech output; this output is a 64 kHz pulse, modulated in both width and amplitude. It is configured as a current sink with a saturating voltage of about 3 V.

Supply

V_{DD}	(13)	Single supply voltage, nominally 5 V, but battery operation is possible.
V_{SS}	(1)	Ground.
TEST	(24)	Used for testing purposes. Changes other pin functions. Must be tied to ground for user operation.
NC	(15)	It is recommended to ground this pin.

HANDLING

Inputs and outputs are protected against electrostatic charge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see 'Handling MOS Devices').

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage range		V_{DD}	−0,5	+ 7	V
Voltage with respect to V_{SS}	on any pin	V_I	−0,5	+ 7	V
Output voltage	pins 2 and 20	V_{REQ}, V_{OUT}		15	V
Storage temperature range		T_{stg}	−20	+ 125	°C
Operating ambient temperature range		T_{amb}	0	+ 70	°C

CHARACTERISTICS

T_{amb} = 25 °C; V_{DD} = 5 V, unless otherwise specified; all voltages referenced to V_{SS}

parameter	conditions	symbol	min.	typ.	max.	unit
Symbol						
Supply voltage	note 1	V_{DD}	4,5	5,0	5,5	V
Supply current	no audio load	I_{DD}	–	30	50	mA
Inputs						
D0 to D7, A0, $\overline{CE}$, $\overline{W}$, $\overline{R}$/W, $\overline{REQEN}$, CLK IN						
Input voltage HIGH		V_{IH}	2,0	–	V_{DD}	V
Input voltage LOW		V_{IL}	–0,5	–	0,8	V
Input leakage current	note 2	I_{IR}	–	–	10	μA
Input capacitance		C_I	–	–	7	pF
Outputs						
D7 (I/O), CLK OUT						
Output voltage HIGH	$-I_{OH}$ = 100 μA	V_{OH}	2,4	–	–	V
Output voltage LOW	I_{OL} = 1,6 mA	V_{OL}	–	–	0,4	V
Output load capacitance		C_L	–	–	50	pF
$\overline{REQ}$						
Output voltage HIGH	open drain	V_{OH}	–	–	13,2	V
Output voltage LOW	I_{OL} = 1,6 mA	V_{OL}	–	–	0,4	V
Output load capacitance		C_L	–	–	50	pF
Audio output						
Reference current	pin 19; note 8	I_{REF}	–	–	0,3	mA
Output current	pin 20; peak value					
	I_{REF} = 0 mA	I_{OUT}	–	100	–	μA
	I_{REF} = 0,1 mA	I_{OUT}	–	1,7	–	mA
	I_{REF} = 0,3 mA	I_{OUT}	–	5	–	mA
Output voltage	pin 20; for linear operation; note 3; I_{REF} = 0,1 mA	V_{OUT}	2,5	–	13,2	V
Oscillator						
Crystal frequency	internal	f_{XTAL}	–		4,00	MHz
Clock frequency	external	f_{CLK}	–		4,00	MHz

TIMING CHARACTERISTICS (note 4) (Figs 6 and 7)

parameter	condition	symbol	min.	typ.	max.	unit
Write enable		t_{WR}	200	–	–	ns
Address set-up		t_{AS}	30	–	–	ns
Address hold		t_{AH}	30	–	–	ns
Data set-up for write		t_{DS}	150	–	–	ns
Data hold for write		t_{DH}	30	–	–	ns
Request hold	note 5	t_{RH}	–	–	350	ns
Request next	note 6 clock frequency = 3,84 MHz	t_{RN}	–	–	3	μs
Read enable		t_{RD}	200	–	–	ns
Data delay for read	note 7	t_{DD}	–	–	150	ns
Data floating for read	note 7	t_{DF}	–	–	150	ns
Request valid before write		t_{RV}	0	–	–	ns
Request output enable response		t_{ROE}	–	–	750	ns
Control set-up		t_{CS}	20	–	–	ns
Control hold		t_{CH}	20	–	–	ns

Notes

1. The circuit will continue to operate from a supply of up to 6,5 V, but without necessarily meeting the specification.
2. This is also valid for V_{DD} = 0 V.
3. This permits the connection of the output load to a supply higher than that supplying the synthesizer.
4. Timing reference level is 1,5 V.
5. An external pull-up resistor is required, as this is an open drain output.
   The time (t_{RH}) to reach 2,0 V is specified at a load to 5 V of 3,3 kΩ and 50 pF.
6. Between two data write operations of one speech frame.
7. Levels greater than 2,0 V for a '1' or less than 0,8 V for a '0' are reached with a load of one TTL input and 50 pF.
8. Typical voltage level at the REF pin is 2,5 V.

OPERATION PRINCIPLE

The MEA8000 has been designed for a vocal tract modelling technique of voice synthesis. This method gives the lowest possible bit rate for speech quality which is acceptable for most industrial applications.

Figure 3 shows a simplified electronic model of the human vocal tract as a formant synthesizer. A combination of a periodic signal, representing the pitch of the original speech, and an aperiodic signal, representing the unvoiced sound in the speech. Both these signals are fed to a variable filter comprising four resonantors (via an amplifier which controls the amplitude of the synthesized sound). The resonators model the sound in accordance with the formats in the original speech. Each resonator is controlled by two parameters, one for the resonant frequency and one for the bandwidth.
The information required to control the synthesizer is:

- pitch
- amplitude
- voice/unvoiced source selector

} excitation source (vocal cords)

- filter control — spectrum shaping (vocal tract)

A good replica of the original speech is obtained by periodic updating of this control information.

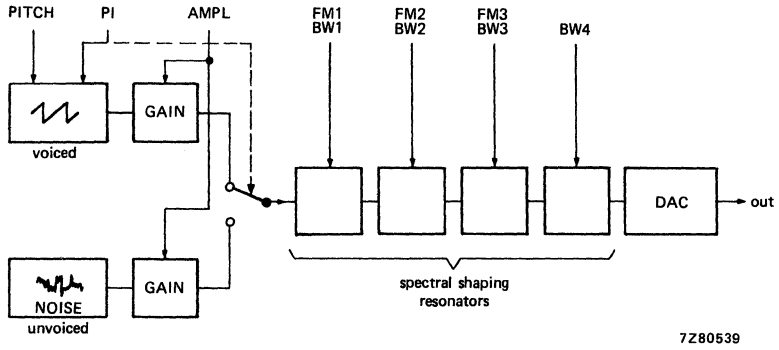


Fig. 3 Electronic model of human vocal tract.

OPERATION

Speech is generated by suitable filtering of a relatively low frequency sawtooth waveform for voiced sounds, or of random noise for unvoiced sounds. New parameters for both the digital waveform generator and the digital filter are supplied to the synthesizer in coded groups of 4 bytes via the data bus. The code group also contains the duration of the next speech frame to be produced (8, 16, 32 or 64 ms).

The output sample rate is 64 kHz or 8 times the internal sample rate with linear interpolation in between. This greatly reduces the need for an external analogue output filter.

Modes of operation

1. STOP mode: characterised by a silent output and the status $\overline{\text{REQ}}$ bit set to '1'. This mode is entered from power up or by STOP command. The mode is entered automatically if at the end of an active speech frame the next four parameter bytes are not yet received while the CONT bit in the command register is a '0'. In the latter case the final speech frame will be repeated once but with a decaying amplitude and the same pitch.
2. ACTIVE mode: a speech sample is being produced.
3. CONTINUOUS mode: entered if an active speech frame is finished and new data is not supplied in time while the CONT bit in the command register is a '1'. The synthesizer will repeat the last speech frame indefinitely until all four new data bytes are received, or a STOP command, or a reset of the CONT bit.

Speech code input buffer

Speech code is written to the synthesizer when $\overline{CE}$ and $\overline{W}$ are both '0', while $\overline{R}/W$ = '1' and A0 = '0'. Also the status $\overline{REQ}$ bit must read a '1', otherwise the synthesizer is still busy and will not react to a data write operation.
Starting from the STOP mode, the first data will be interpreted as a starting value for the PITCH. Thereafter every four successive data bytes are treated as a group of speech code. The coded speech frame format is shown in Fig. 4.

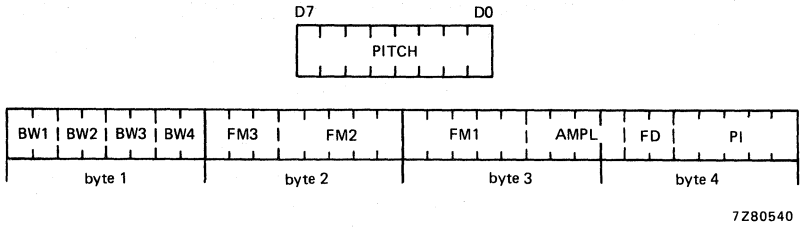


Fig. 4 Format of coded speech frame.

code	bits	parameter
PITCH	8	initial value for pitch
FD	2	speech frame duration
PI	5	pitch increment (rate of change) or noise selection
AMPL	4	amplitude
FM1	5	frequency of 1st formant
FM2	5	frequency of 2nd formant
FM3	3	frequency of 3rd formant
FM4	0	frequency of 4th formant (fixed)
BW1	2	bandwidth of 1st formant
BW2	2	bandwidth of 2nd formant
BW3	2	bandwidth of 3rd formant
BW4	2	bandwidth of 4th formant

During each data write operation, the status REQ bit will be cleared to '0'.
It appears within a few microseconds, requesting the next byte of the group.
The request for the first byte of the next group always appears shortly after the beginning of the current speech frame, and all four bytes must be provided before it finishes. This leaves the control circuit (i.e. microprocessor) enough time to use polling, instead of interrupts, as the minimum time of a speech is 8 ms.

When in the STOP mode the synthesizer will commence producing sound after receipt of 1 + 4 bytes.

Status bit

The status bit is accessed at $\overline{CE}$ = $\overline{R}/W$ = '0'.
The status of $\overline{W}$ and A0 are arbitrary.
Pin D7 reveals the request for a (next) speech code byte: '0' = busy, '1' = request for data.

Command register

A command is written to the synthesizer at $\overline{CE}$ = $\overline{W}$ = '0' while A0 = $\overline{R}$/W = '1'.

D7	D6	D5	D4	D3	D2	D1	D0
			STOP	CONT enable	CONT	ROE enable	ROE
NOT USED			'0' = INVALID '1' = STOP	00 = INVALID 01 = INVALID 10 = SLOW STOP 11 = CONTINUE		00 = INVALID 01 = INVALID 10 = DISABLE $\overline{REQ}$ OUTPUT 11 = ENABLE $\overline{REQ}$ OUTPUT	

STOP — Stop mode. This results in an immediate reset of the synthesizer to the STOP mode. The ROE and CONT are not affected by this command.

CONT — Continuous mode. This bit can be set or cleared only if the corresponding CONT enable bit is programmed as a '1'. In the continuous mode the synthesizer will not revert to the STOP mode if all four parameters are not received before the end of the current speech frame, but repeat it indefinitely.

If CONT = '1' the last frame will be repeated once with decaying amplitude and the same pitch before the stop mode is entered.

ROE — Request Output Enable. This can be set or cleared only if the corresponding ROE enable bit is a '1'. ROE determines whether the request in the status bit appears on the $\overline{REQ}$ pin.

Note: the same can be achieved by connecting the $\overline{REQEN}$ pin (request enable) to a '0'.

After power on, the command register bits CONT and ROE will both be zero. Thus power on equals the command 00011010 = 1 A (hexadecimal).

Control signals

With the three control signals $\overline{CE}$, $\overline{W}$ and $\overline{R}$/W the synthesizer is made compatible with most microprocessors and microcomputers.

$\overline{CR}$	$\overline{W}$	$\overline{R}$/W	A0		Operation
0	0	1	0		WRITE DATA
0	0	1	1		WRITE COMMAND
0	X	0	X		READ STATUS
0	1	1	X		3-STATE DATA BUS
1	X	X	X		3-STATE DATA BUS

Power supply

During (slow) power up or power down the circuit will not produce any spurious sound. As soon as the supply is high enough for reliable operation, the circuit will be in the STOP mode with ROE = CONT = '0'.

Timing diagrams

The control signals $\overline{CE}$, R/W and $\overline{W}$ have been specified to enable easy interface to most microprocessors and microcomputers. For instance, with connection to an MAB8048 microcomputer the R/W and $\overline{W}$ inputs can be used as the $\overline{RD}$ and $\overline{WR}$ strobe inputs.

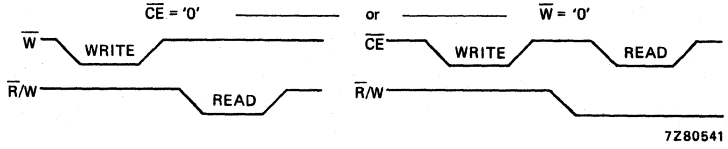


Fig. 5 Typical waveforms of the control signals.

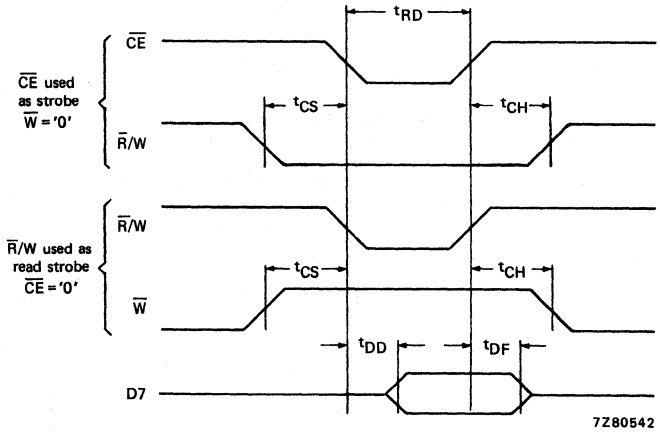


Fig. 6 Read timing.

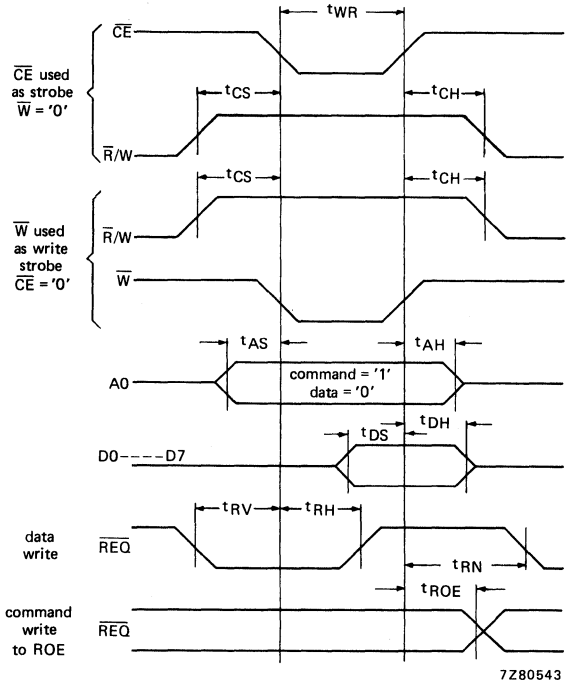
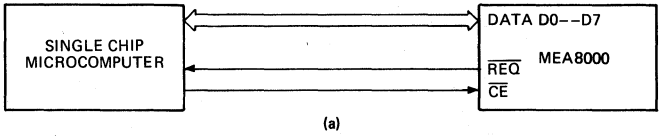
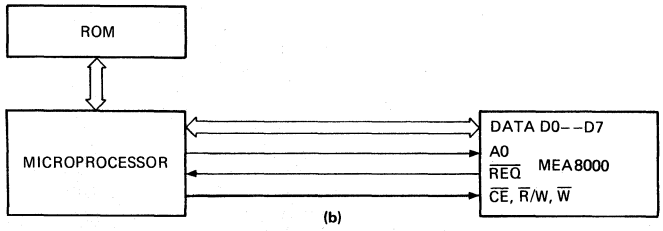


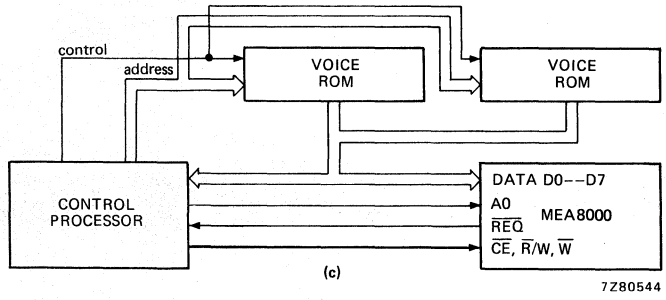
Fig. 7 Write timing.



(a) Minimum system of single chip microcomputer with voice ROM on board.



(b) MEA8000 as a microprocessor peripheral.



(c) Applications using separate voice ROMs.

Fig. 8 Typical applications.

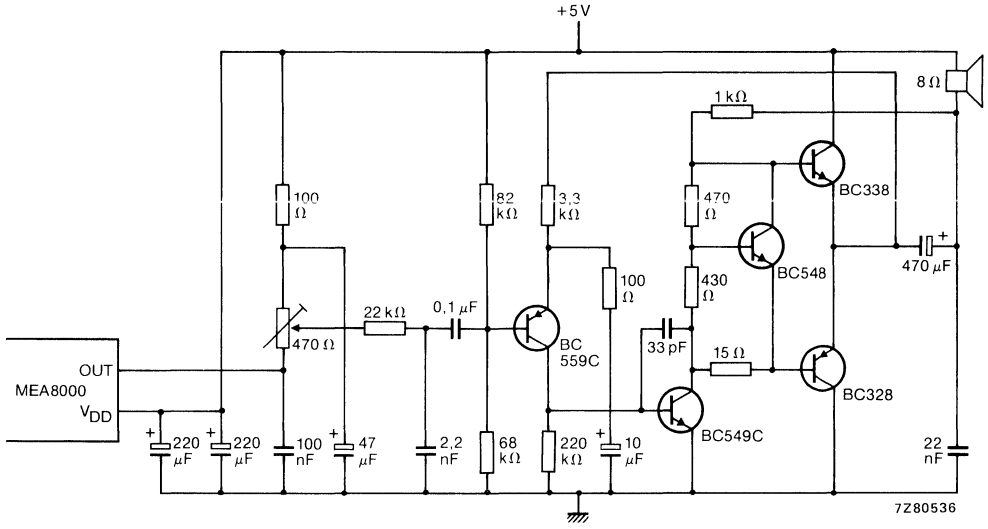


Fig. 9 Typical output applications.

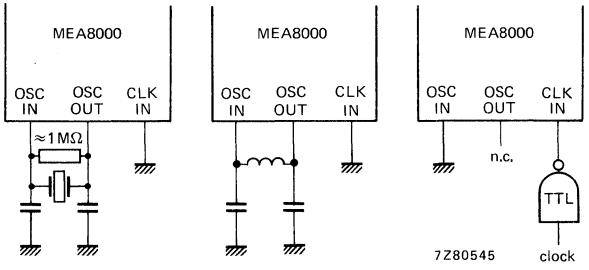


Fig. 10 Oscillator/clock configurations.

TONE DECODER/PHASE LOCKED LOOP

DESCRIPTION

The SE/NE567 tone and frequency decoder is a highly stable phase-locked loop with synchronous AM lock detection and power output circuitry. Its primary function is to drive a load whenever a sustained frequency within its detection band is present at the self-biased input. The bandwidth center frequency, and output delay are independently determined by means of four external components.

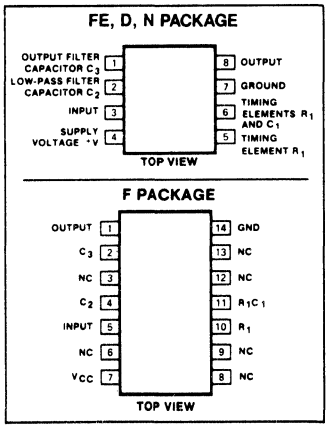
FEATURES

- **Wide frequency range (.01Hz to 500kHz)**
- **High stability of center frequency**
- **Independently controllable bandwidth (up to 14 percent)**
- **High out-band signal and noise rejection**
- **Logic-compatible output with 100mA current sinking capability**
- **Inherent immunity to false signals**
- **Frequency adjustment over a 20 to 1 range with an external resistor**
- **Military processing available**

APPLICATIONS

- **Touch Tone® decoding**
- **Carrier current remote controls**
- **Ultrasonic controls (remote TV, etc.)**
- **Communications paging**
- **Frequency monitoring and control**
- **Wireless intercom**
- **Precision oscillator**

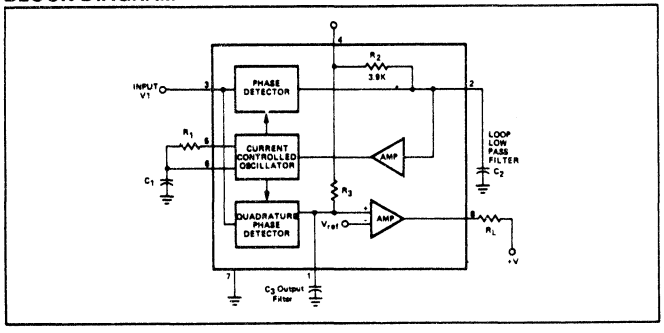
PIN CONFIGURATIONS



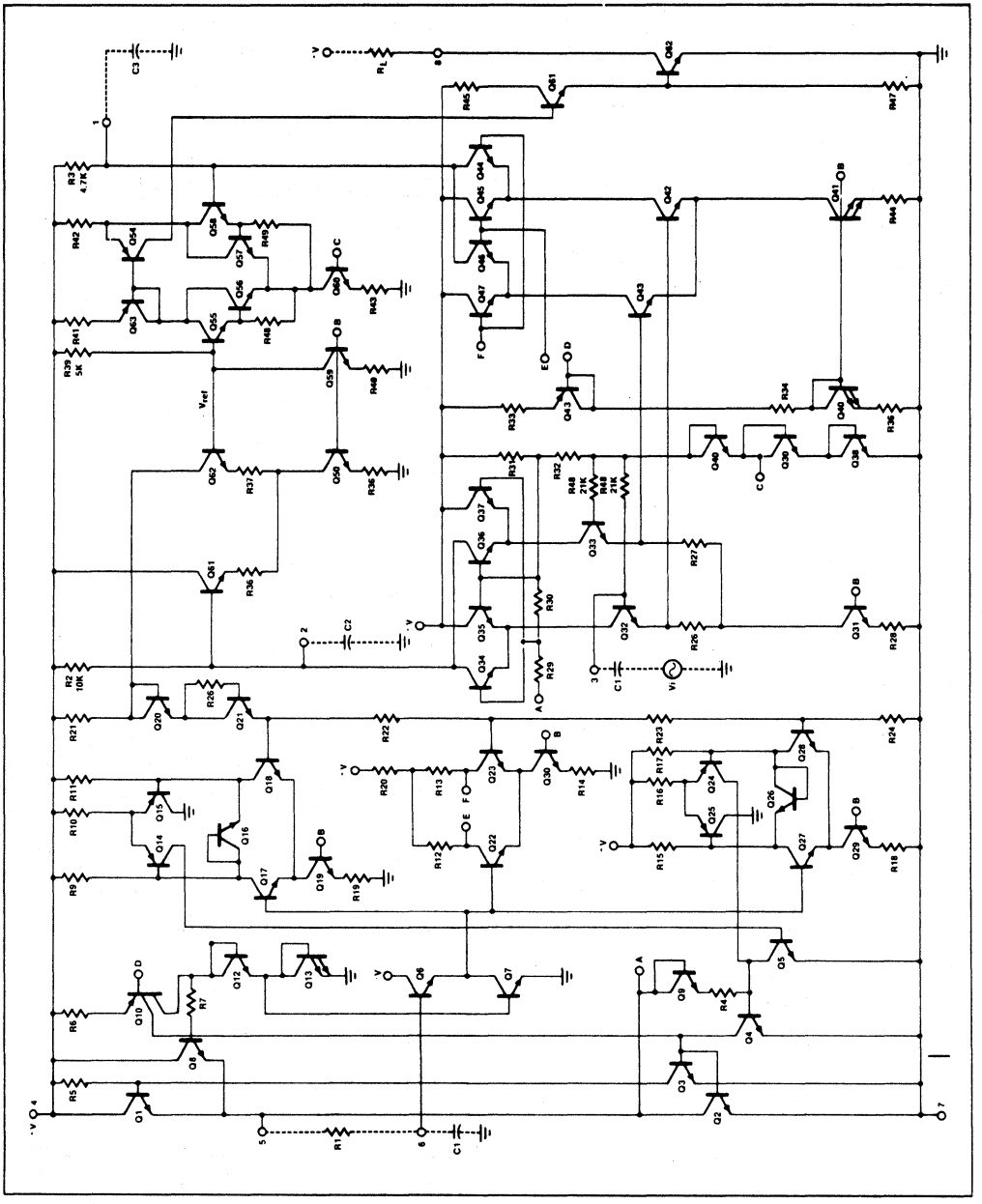
ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Operating temperature		
NE567	0 to +70	°C
SE567	-55 to +125	°C
Operating voltage	10	V
Positive voltage at input	0.5 + Vs	V
Negative voltage at input	-10	Vdc
Output voltage (collector of output transistor)	15	Vdc
Storage temperature	-65 to +150	°C
Power dissipation	300	mW

BLOCK DIAGRAM



EQUIVALENT SCHEMATIC



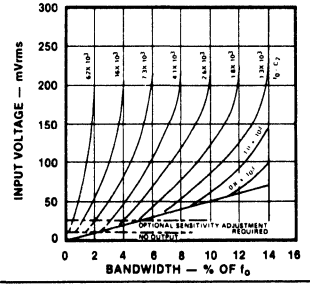
DC ELECTRICAL CHARACTERISTICS (V+ = 5.0V; T_A = 25°C unless otherwise specified.)

PARAMETER	TEST CONDITIONS	SE567			NE567			UNIT
		Min	Typ	Max	Min	Typ	Max	
CENTER FREQUENCY[1]								
Highest center frequency (f_o)			500			500		kHz
Center frequency stability[2]	-55 to +125°C		35±140			35±140		ppm/°C
	0 to +70°C		35±60			35±60		ppm/°C
Center frequency distribution	f_o = 100kHz = 1.1/R_1C_1	-10	0	+10	-10	0	+10	%
Center frequency shift with supply voltage	f_o = 100kHz = 1.1/R_1C_1		0.5	1		0.7	2	%/V
DETECTION BANDWIDTH								
Largest detection bandwidth	f_o = 100kHz = 1.1/R_1C_1	12	14	16	10	14	18	% of f_o
Largest detection bandwidth skew			2	4		3	6	% of f_o
Largest detection bandwidth—variation with temperature	V_i = 300mVrms		±0.1			±0.1		%/°C
Largest detection bandwidth—variation with supply voltage	V_i = 300mVrms		±2			±2		%/V
INPUT								
Input resistance		15	20	25	15	20	25	kΩ
Smallest detectable input voltage (V_i)	I_L = 100mA, f_i = f_o		20	25		20	25	mVrms
Largest no-output input voltage	I_L = 100mA, f_i = f_o	10	15		10	15		mVrms
Greatest simultaneous outband signal to inband signal ratio			+6			+6		dB
Minimum input signal to widebahd noise ratio	B_n = 140kHz		-6			-6		dB
OUTPUT								
Fastest on-off cycling rate			f_o/20			f_o/20		
"1" output leakage current	V_8 = 15V		0.01	25		0.01	25	μA
"0" output voltage	I_L = 30mA		0.2	0.4		0.2	0.4	V
	I_L = 100mA		0.6	1.0		0.6	1.0	V
Output fall time[3]	R_L = 50Ω		30			30		ns
Output rise time[3]	R_L = 50Ω		150			150		ns
GENERAL								
Operating voltage range		4.75		9.0	4.75		9.0	V
Supply current quiescent			6	8		7	10	mA
Supply current—activated	R_L = 20kΩ		11	13		12	15	mA
Quiescent power dissipation			30			35		mW

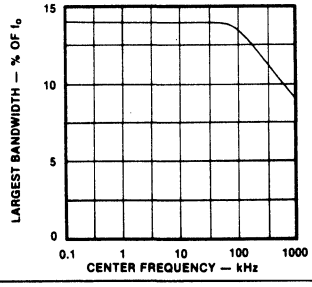
NOTES
1. Frequency determining resistor R_1 should be between 2 and 20kΩ.
2. Applicable over 4.75 to 5.75 volts. See graphs for more detailed information.
3. Pin 8 to Pin 1 feedback R_L network selected to eliminate pulsing during turn-on and turn-off.

TYPICAL PERFORMANCE CHARACTERISTICS

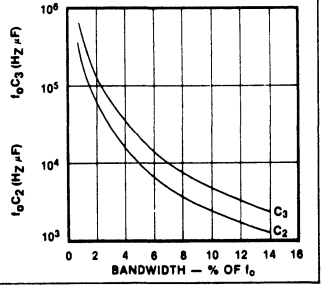
BANDWIDTH vs INPUT SIGNAL AMPLITUDE



LARGEST DETECTION BANDWIDTH vs OPERATING FREQUENCY

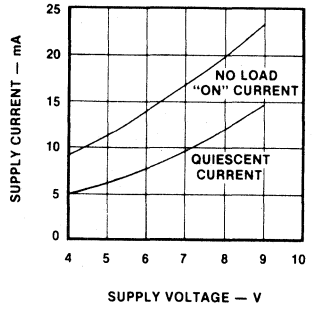


DETECTION BANDWIDTH AS A FUNCTION OF C_2 and C_3

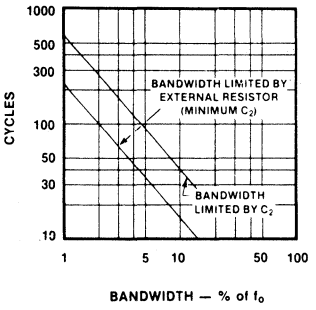


TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

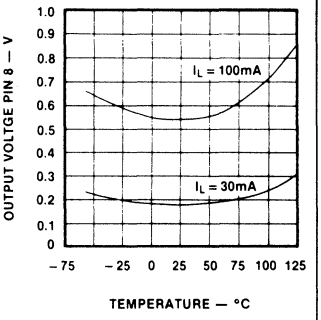
TYPICAL SUPPLY CURRENT vs SUPPLY VOLTAGE



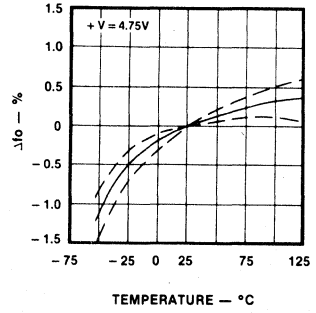
GREATEST NUMBER OF CYCLES BEFORE OUTPUT



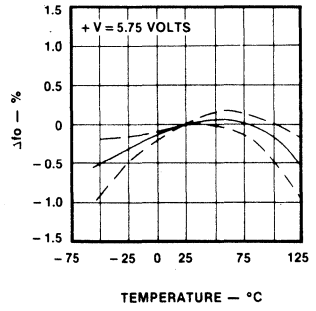
TYPICAL OUTPUT VOLTAGE vs TEMPERATURE



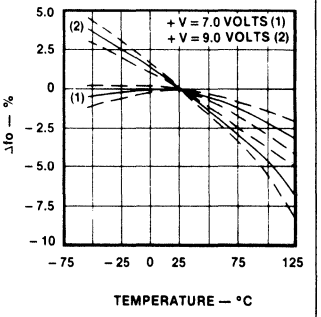
TYPICAL FREQUENCY DRIFT WITH TEMPERATURE (MEAN AND S.D.)



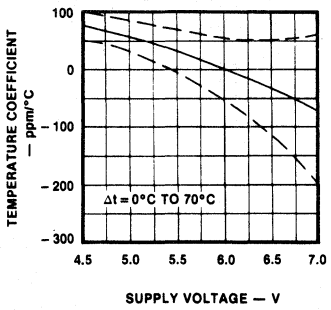
TYPICAL FREQUENCY DRIFT WITH TEMPERATURE (MEAN AND S.D.)



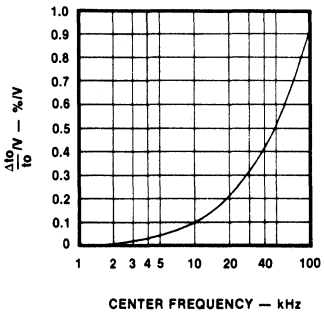
TYPICAL FREQUENCY DRIFT WITH TEMPERATURE (MEAN AND S.D.)



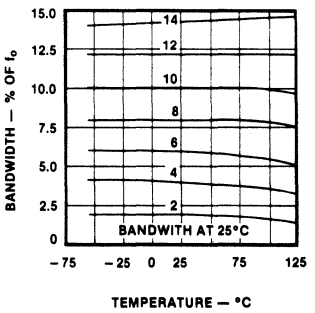
CENTER FREQUENCY TEMPERATURE COEFFICIENT (MEAN AND S.D.)



CENTER FREQUENCY SHIFT WITH SUPPLY VOLTAGE CHANGE vs OPERATING FREQUENCY



TYPICAL BANDWIDTH VARIATION WITH TEMPERATURE



DESIGN FORMULAS

$$f_0 \simeq \frac{1.1}{R_1 C_1}$$

$$BW \simeq 1070 \sqrt{\frac{V_i}{f_0 C_2}} \text{ in \% of } f_0, V_i \leq 200mVrms$$

Where

V_i = Input Voltage (Vrms)
C_2 = Low-Pass Filter Capacitor (μF)

PHASE LOCKED LOOP TERMINOLOGY CENTER FREQUENCY (fo)

The free-running frequency of the current controlled oscillator (CCO) in the absence of an input signal.

Detection Bandwidth (BW)

The frequency range, centered about f_0, within which an input signal above the threshold voltage (typically 20mVrms) will cause a logical zero state on the output. The detection bandwidth corresponds to the loop capture range.

Lock Range

The largest frequency range within which an input signal above the threshold voltage will hold a logical zero state on the output.

Detection Band Skew

A measure of how well the detection band is centered about the center frequency, f_0. The skew is defined as $(f_{max} + f_{min} - 2f_0)/2f_0$ where fmax and fmin are the frequencies corresponding to the edges of the detection band. The skew can be reduced to zero if necessary by means of an optional centering adjustment.

OPERATING INSTRUCTIONS

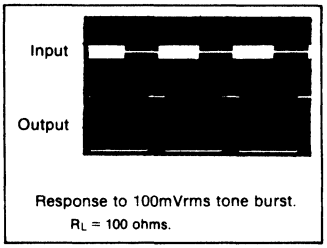
Figure 1 shows a typical connection diagram for the 567. For most applications, the following three-step procedure will be sufficient for choosing the external components R_1, C_1, C_2 and C_3.

1. Select R_1 and C_1 for the desired center frequency. For best temperature stability, R_1 should be between 2K and 20K ohm, and the combined temperature coefficient of the R_1C_1 product should have sufficient stability over the projected temperature range to meet the necessary requirements.

2. Select the low pass capacitor, C_2, by referring to the Bandwidth versus Input Signal Amplitude graph. If the input amplitude variation is known, the appropriate value of f_0C_2 necessary to give the desired bandwidth may be found. Conversely, an area of operation may be selected on this graph and the input level and C_2 may be adjusted accordingly. For example, constant bandwidth operation requires that input amplitude be above 200mVrms. The bandwidth, as noted on the graph, is then controlled solely by the f_0C_2 product (f_0 (Hz), C_2 (μ fd)).

3. The value of C_3 is generally non-critical. C_3 sets the band edge of a low pass filter which attenuates frequencies outside the detection band to elminate spurious outputs. If C_3 is too small, frequencies just outside the detection band will switch the output stage on and off at the beat frequency, or the output may pulse on and off during the turn-on transient. If C_3 is too large, turn-on and turn-off of the output stage will be delayed until the voltage on C_3 passes the threshold voltage. (Such delay may be desirable to avoid spurious outputs due to translent frequencies.) A typical minimum value for C_3 is $2C_2$.

TYPICAL RESPONSE



Response to 100mVrms tone burst.
R_L = 100 ohms.

Response to same input tone burst with wideband noise.
$\frac{S}{N}$ = -6db R_L = 100 ohms
Noise Bandwidth = 140Hz

AVAILABLE OUTPUTS (Figure 2)

The primary output is the uncommitted output transistor collector, pin 8. When an in-band input signal is present, this transistor saturates; its collector voltage being less than 1.0 volt (typically 0.6V) at full output current (100mA). The voltage at pin 2 is the phase detector output which is a linear function of frequency over the range of 0.95 to 1.05 f_0 with a slope of about 20mV per percent of frequency deviation. The average voltage at pin 1 is, during lock, a function of the inband input amplitude in accordance with the transfer characteristic given. Pin 5 is the controlled oscillator square wave

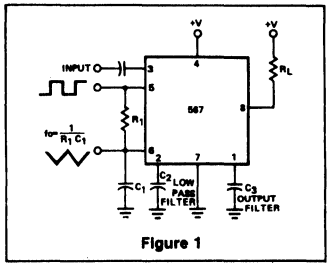


Figure 1

output of magnitude $(+V - 2V_{be}) \simeq (+V - 1.4V)$ having a dc average of +V/2. A 1kΩ load may be driven from pin 5. Pin 6 is an exponential triangle of 1 volt peak-to-peak with an average dc level of +V/2. Only high impedance loads may be connected to pin 6 without affecting the CCO duty cycle or temperature stability.

OPERATING PRECAUTIONS

A brief review of the following precautions will help the user achieve the high level of performance of which the 567 is capable.

1. Operation in the high input level mode (above 200mV) will free the user from bandwidth variations due to changes in the in-band signal amplitude. The input stage is now limiting, however, so that out-band signals or high noise levels can cause an apparent bandwidth reduction as the in-band signal is suppressed. Also, the limiting action will create in-band components from sub-harmonic signals, so the 567 becomes sensitive to signals at $f_0/3$, $f_0/5$, etc.

2. The 567 will lock onto signals near $(2n + 1) f_0$, and will give an output for signals near $(4n + 1) f_0$ where n = 0, 1, 2, etc. Thus, signals at $5f_0$ and $9f_0$ can cause an unwanted output. If such signals are anticipated, they should be attenuated before reaching the 567 input.

3. Maximum immunity from noise and out-band signals is afforded in the low input level (below 200mVrms) and reduced bandwidth operating mode. However, decreased loop damping causes the worse-case lock-up time to increase, as shown by the Greatest Number of Cycles Before Output vs Bandwidth graph.

4. Due to the high switching speeds (20ns) associated with 567 operation, care should be taken in lead routing. Lead lengths should be kept to a minimum. The power supply should be adequately bypassed close to the 567 with a 0.01μF or greater capacitor; grounding paths should be carefully chosen to avoid ground loops and

unwanted voltage variations. Another factor which must be considered is the effect of load energization on the power supply. For example, an incandescent lamp typically draws 10 times rated current at turn-on. This can cause supply voltage fluctuations which could, for example, shift the detection band of narrow-band systems sufficiently to cause momentary loss of lock. The result is a low-frequency oscillation into and out of lock. Such effects can be prevented by supplying heavy load currents from a separate supply or increasing the supply filter capacitor.

SPEED OF OPERATION

Minimum lock-up time is related to the natural frequency of the loop. The lower it is, the longer becomes the turn-on transient. Thus, maximum operating speed is obtained when C_2 is at a minimum. When the signal is first applied, the phase may be such as to initially drive the controlled oscillator away form the incoming frequency rather than toward it. Under this condition, which is of course unpredictable, the lock-up transient is at its worst and the theoretical minimum lock-up time is not achievable. We must simply wait for the transient to die out.

The following expressions give the values of C_2 and C_3 which allow highest operating speeds for various band center frequencies. The minimum rate at which digital information may be detected without information loss due to the turn-on transient or output chatter is about 10 cycles per bit, corresponding to an information transfer rate of $f_o/10$ baud.

$$C_2 = \frac{130}{f_o}\ \mu F$$

$$C_3 = \frac{260}{f_o}\ \mu F$$

In cases where turn-off time can be sacrificed to achieve fast turn-on, the optional sensitivity adjustment circuit can be used to move the quiescent C_3 voltage lower (closer to the threshold voltage). However, sensitivity to beat frequencies, noise and extraneous signals will be increased.

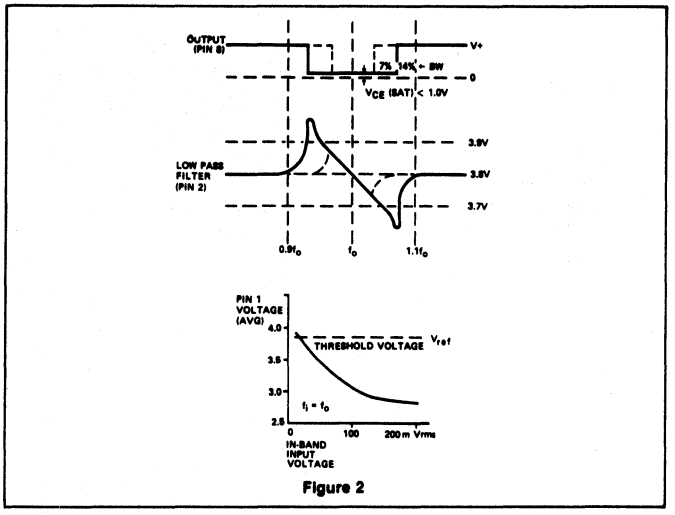


Figure 2

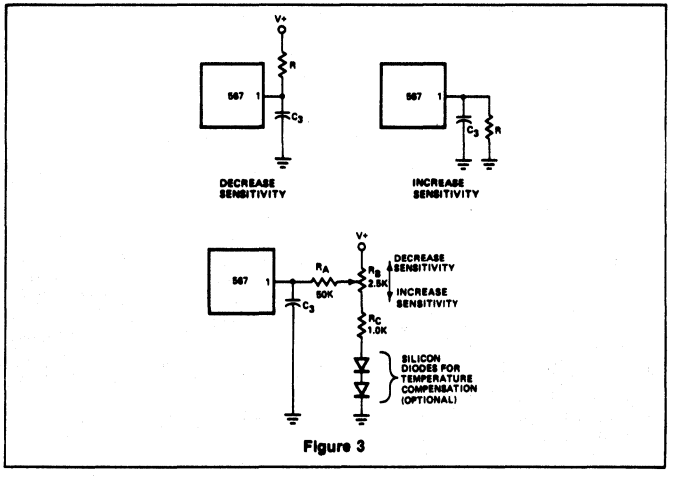


Figure 3

OPTIONAL CONTROLS (Figure 3)

The 567 has been designed so that, for most applications, no external adjustments are required. Certain applications, however, will be greatly facilitated if full advantage is taken of the added control possibilities available through the use of additional external components. In the diagrams given, typical values are suggested where applicable. For best results the resistors used, except where noted, should have the same temperature coefficient. Ideally, silicon diodes would be low-resistivity types, such as forward-biased transistor base-emmiter junctions. However, ordinary low-voltage diodes should be adequate for most applications.

SENSITIVITY ADJUSTMENT

(Figure 3)

When operated as a very narrow band detector (less than 8 percent), both C_2 and C_3 are made quite large In order to improve noise and outband signal rejection. This will inevitably slow the response time. If, however, the output stage is biased closer to the threshold level, the turn-on time can be improved. This is accomplished by drawing additional current to terminal 1. Under this condition, the 567 will also give an output for lower-level signals (10mV or lower).

By adding current to terminal 1, the output stage is biased further away from the threshold voltage. This is most useful when, to obtain maximum operating speed, C_2 and C_3 are made very small. Normally, frequencies just outside the detection band could cause false outputs under this condition. By desensitizing the output stage, the outband beat notes do not feed through to the output stage. Since the input level must be somewhat greater when the output stage is made less sensitive, rejection of third harmonics or in-band harmonics (of lower frequency signals) is also improved.

CHATTER PREVENTION (Figure 4)

Chatter occurs in the output stage when C_3 is relatively small, so that the lock transient and the AC components at the quadrature phase detector (lock detector) output cause the output stage to move through its threshold more than once. Many loads, for example lamps and relays, will not respond to the chatter. However, logic may recognize the chatter as a series of outputs. By feeding the output stage output back to its input (pin 1) the chatter can be eliminated. Three schemes for doing this are given in Figure 4. All operate by feeding the first output step (either on or off) back to the input, pushing the input past the threshold until the transient conditions are over. It is only necessary to assure that the feedback time constant is not so large as to prevent operation at the highest anticipated speed. Although chatter can always be eliminated by making C_3 large, the feedback circuit will enable faster operation of the 567 by allowing C_3 to be kept small. Note that if the feedback time constant is made quite large, a short burst at the input frequency can be stretched into a long output pulse. This may be useful to drive, for example, stepping relays.

DETECTION BAND CENTERING (OR SKEW) ADJUSTMENT

(Figure 5)

When it is desired to alter the location of the detection band (corresponding to the loop capture range) within the lock range, the circuits shown above can be used. By moving the detection band to one edge of the range, for example, input signal variations will expand the detection band in only one direction. This may prove useful when a strong but undesirable signal is expected on one side or the other of the center frequency. Since R_B also alters the duty cycle slightly, this method may be used to obtain a precise duty cycle when the 567 is used as an oscillator.

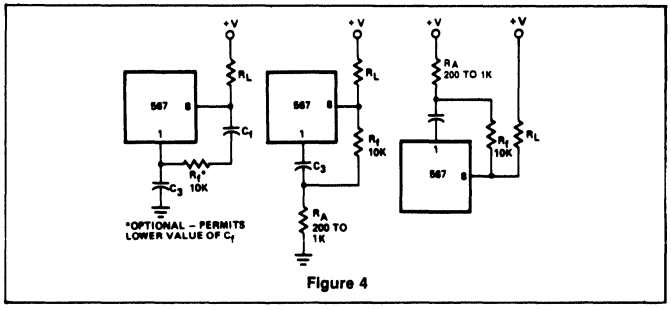


Figure 4

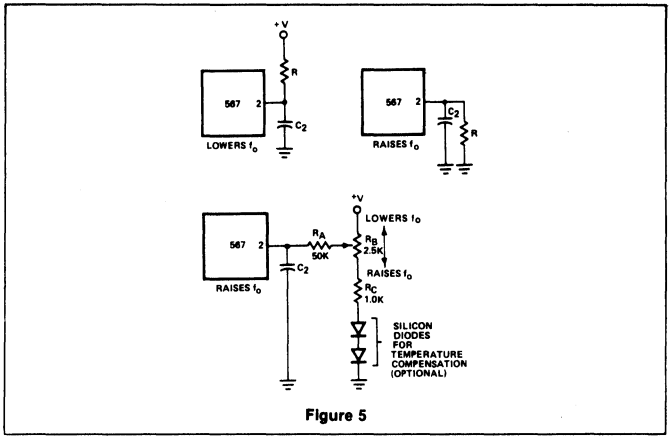


Figure 5

ALTERNATE METHOD OF BANDWIDTH REDUCTION

(Figure 6)

Although a large value of C_2 will reduce the bandwidth, it also reduces the loop damping so as to slow the circuit response time. This may be undesirable. Bandwidth can be reduced by reducing the loop gain. This scheme will improve damping and permit faster operation under narrow-band conditions. Note that the reduced impedance level at terminal 2 will require that a larger value of C_2 be used for a given filter cutoff frequency. If more than three 567s are to be used, the network of R_B and R_C can be eliminated and the R_A resistors connected together. A capacitor between this junction and ground may be required to shunt high frequency components.

OUTPUT LATCHING (Figure 7)

To latch the output on after a signal is received, it is necessary to provide a feedback resistor around the output stage (between pins 8 and 1). Pin 1 is pulled up to unlatch the output stage.

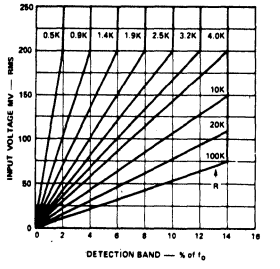
REDUCTION OF C1 VALUE

(Figure 8)

For precision very low-frequency applications, where the value of C_1 becomes large, an overall cost savings may be achieved by inserting a voltage follower between the R_1 C_1 junction and pin 6, so as to allow a higher value of R_1 and a lower value of C_1 for a given frequency.

PROGRAMMING

To change the center frequency, the value of R_1 can be changed with a mechanical or solid state switch, or additional C_1 capacitors may be added by grounding them through saturating npn transistors.



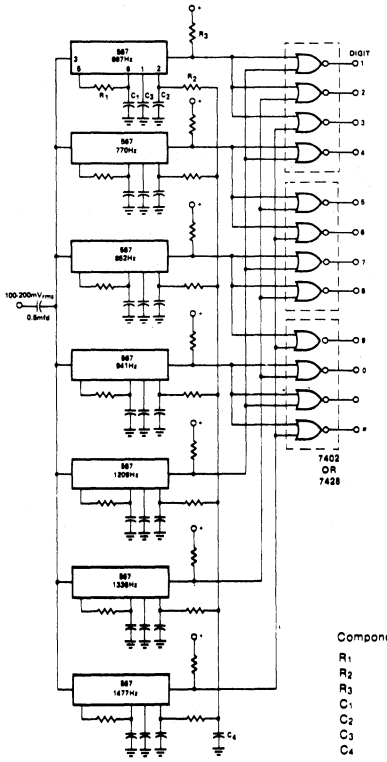
NOTE

Adjust control for symmetry of detection band edges about f_o.

Figure 6

TYPICAL APPLICATIONS

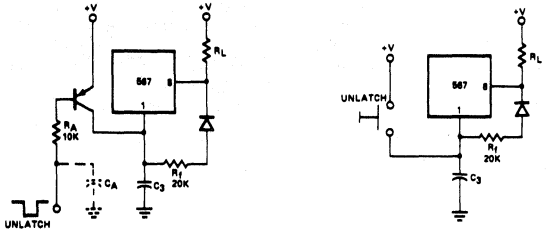
TOUCH-TONE® DECODER



Component values (Typical)

R_1	6.8 to 15K ohm
R_2	4.7K ohm
R_3	20K ohm
C_1	0.10mfd
C_2	1.0mfd 5V
C_3	2.2mfd 6V
C_4	250 µF 6V

OUTPUT LATCHING



C_A prevents latch-up when power supply is turned on.

Figure 7

PRECISION VLF

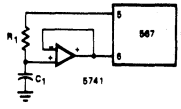
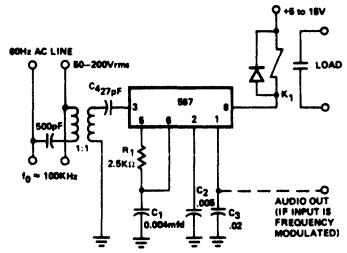


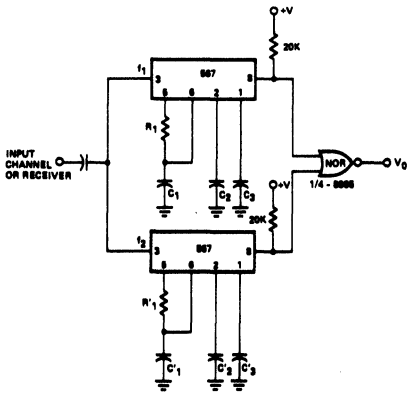
Figure 8

TYPICAL APPLICATIONS (Cont'd)

CARRIER-CURRENT REMOTE CONTROL OR INTERCOM

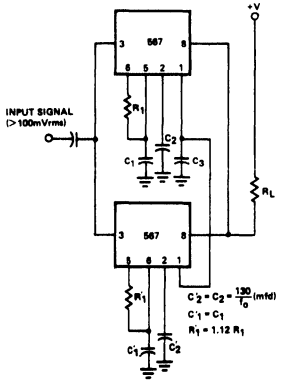


DUAL-TONE DECODER

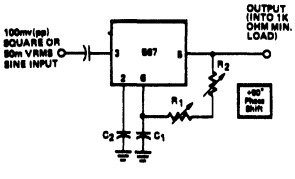


1. Resistor and capacitor values chosen for desired frequencies and bandwidth.
2. If C_3 is made large so as to delay turn-on of the top 567, decoding of sequential (f_1 f_2) tones is possible.

24% BANDWIDTH TONE DECODER



0° to 180° PHASE SHIFTER

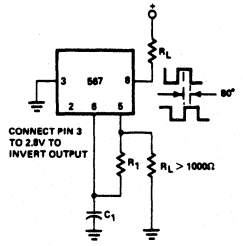


$R_2 \sim R_1/5$

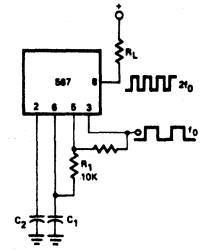
Adjust R_1 so that $\phi = 90°$ with control midway

TYPICAL APPLICATIONS (Cont'd)

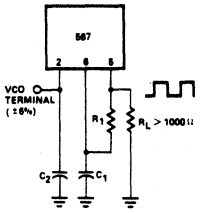
OSCILLATOR WITH QUADRATURE OUTPUT



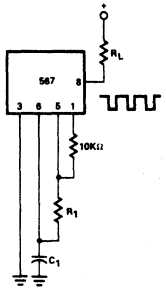
OSCILLATOR WITH DOUBLE FREQUENCY OUTPUT



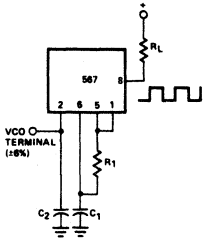
PRECISION OSCILLATOR WITH 20ns SWITCHING



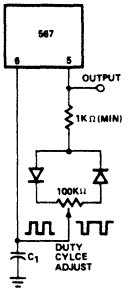
PULSE GENERATOR WITH 25% DUTY CYCLE



PRECISION OSCILLATOR TO SWITCH 100ma LOADS



PULSE GENERATOR



*For additional information, consult the Applications Section.

COMPANDOR

DESCRIPTION

The NE570/571 is a versatile low cost dual gain control circuit in which either channel may be used as a dynamic range compressor or expandor. Each channel has a full wave rectifier to detect the average value of the signal; a linerarized, temperature compensated variable gain cell; and an operational amplifier.

The NE570/571 is well suited for use in cellular radio and radio communications systems, modems, telephone, and satellite broadcast/receive audio sytems.

FEATURES

- **Complete compressor and expandor in 1 IC**
- **Temperature compensated**
- **Greater than 110dB dynamic range**
- **Operates down to 6Vdc**
- **System levels adjustable with external components**
- **Distortion may be trimmed out**

CIRCUIT DESCRIPTION

The NE570/571 compandor building blocks, as shown in the block diagram, are a full wave rectifier, a variable gain cell, an operational amplifier and a bias system. The arrangement of these blocks in the IC result in a circuit which can perform well with few external components, yet can be adapted to many diverse applications.

The full wave rectifier rectifies the input current which flows from the rectifier input, to an internal summing node which is biased at V_{REF}. The rectified current is averaged on an external filter capacitor tied to the C_{RECT} terminal, and the average value of the input current controls the gain of the variable gain cell. The gain will thus be proportional to the average value of the input signal for capacitively coupled voltage inputs as shown in the following equation. Note that for capacitively coupled inputs there is no offset voltage capable of producing a gain error. The only error will come from the bias current of the rectifier (supplied internally) which is less than .1μA.

$$G \propto \frac{|V_{IN} - V_{REF}|\ avg.}{R_1} \quad \text{or} \quad G \propto \frac{|V_{IN}|\ avg.}{R_1}$$

The speed with which gain changes to follow changes in input signal levels is determined by the rectifier filter capacitor. A small capacitor will yield rapid response but will not fully filter low frequency signals. Any ripple on the gain control signal will modulate the signal passing through the variable gain cell. In an expandor or compressor application, this would lead to third harmonic distortion, so there is a tradeoff to be made between fast attack and decay times, and distortion. For step changes in amplitude, the change in gain with time is shown by this equation.

$$G(t) = (G_{initial} - G_{final})\ e^{-t/\tau} + G_{final};\ \tau = 10K \times C_{RECT}$$

The variable gain cell is a current in, current out device with the ratio I_{OUT}/I_{IN} controlled by the rectifier. I_{IN} is the current which flows from the ΔG input to an internal summing node biased at V_{REF}. The following equation applies for capacitively coupled inputs. The output current, I_{OUT}, is fed to the summing node of the op amp.

$$I_{IN} = \frac{V_{IN} - V_{REF}}{R_2} = \frac{V_{IN}}{R_2}$$

A compensation scheme built into the ΔG cell compensates for temperature, and cancels out odd harmonic distortion. The only distortion which remains is even harmonics, and they exist only because of internal offset voltages. The THD trim terminal provides a means for nulling the internal offsets for low distortion operation.

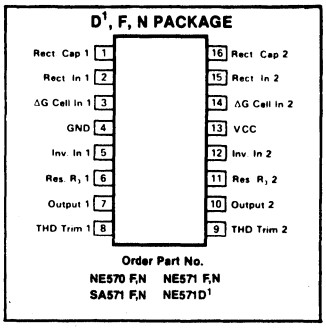
The operational amplifier (which is internally compensated) has the non-inverting input tied to V_{REF}, and the inverting input connected to the ΔG cell output as well as brought out externally. A resistor, R_3, is brought out from the summing node and allows compressor or expandor gain to be determined only by internal components.

Note:
1. Supplied only in large SO (Small Outline) package.

APPLICATIONS

- **Cellular radio**
- **Telephone trunk compandor—570**
- **Telephone subscriber compandor—571**
- **High level limiter**
- **Low level expandor—noise gate**
- **Dynamic noise reduction systems**
- **Voltage controlled amplifier**
- **Dynamic filters**

PIN CONFIGURATION

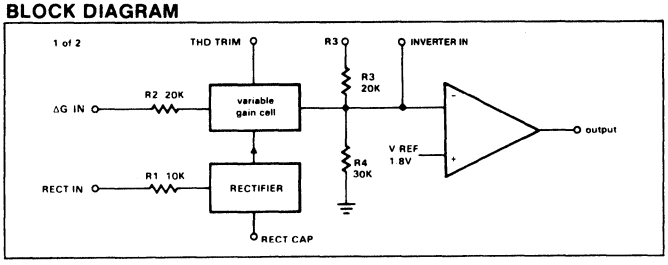


NOTES:
1. SOL - Released in Large SO package only.
2. SOL and non-standard pinout.
3. SO and non-standard pinouts.

ABSOLUTE MAXIMUM RATINGS

	PARAMETER	RATING	UNIT
	Positive supply		Vdc
	570	24	
	571	18	
T_A	Operating temperature range		
	NE	0 to 70	°C
	SA	-40 to +85	°C
P_D	Power dissipation	400	mW

BLOCK DIAGRAM

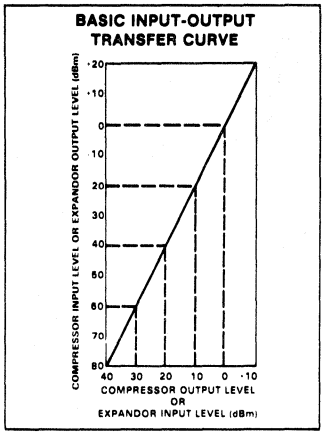


The output stage is capable of ±20mA output current. This allows a +13dBm (3.5V rms) output into a 300Ω load which, with a series resistor and proper transformer, can result in +13dBm with a 600Ω output impedance.

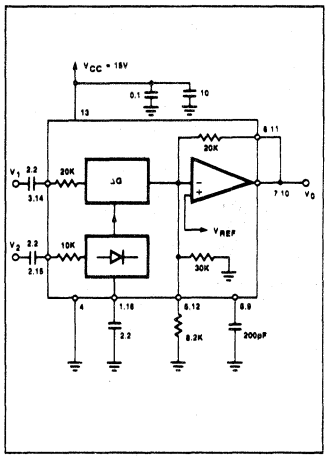
A band gap reference provides the reference voltage for all summing nodes, a regulated supply voltage for the rectifier and ΔG cell, and a bias current for the ΔG cell. The low tempco of this type of reference provides very stable biasing over a wide temperature range.

The typical performance characteristics illustration shows the basic input-output transfer curve for basic compressor or expandor circuits.

TYPICAL PERFORMANCE CHARACTERISTICS



TYPICAL TEST CIRCUIT



DC ELECTRICAL CHARACTERISTICS

$T_A = 25°C$, $V_{CC} = 15$ Except where indicated, the 571 specifications are identical to 570

PARAMETER	TEST CONDITIONS	NE570			NE/SA571[5]			UNIT
		Min	Typ	Max	Min	Typ	Max	
V_{CC} Supply voltage		6		24	6		18	V
I_{CC} Supply current	No signal		3.2	4.8		3.2	4.8	mA
Output current capability		±20			± 20			mA
Output slew rate			± .5			± .5		V/us
Gain cell distortion[2]	Untrimmed		.3	1.0		.5	2.0	%
	Trimmed		05			.1		
Resistor tolerance			±5	±15		± 5	± 15	%
Internal reference voltage		1.7	1.8	1.9	1.65	1.8	1.95	V
Output dc shift[3]	Untrimmed		±20	±50		±30	±100	mV
Expandor output noise	No signal, 15Hz-20kHz[1]		20	45		20	60	μV
			-15					dBRNC
Unity gain level		-1	0	+1	-1.5	0	+1.5	dBm
Gain change[2,4]	-40°C < T < 70°C		±.1			±.1		dB
	0°C < T < 70°C		±.1	±.2		±.1	±.4	
Reference drift[4]	-40°C < T < 70°C		+2, -25	10, -40		+2, -25	+20, -50	mV
	0°C < T < 70°C		±5	±10		±5	±20	
Resistor drift[4]	-40°C < T < 70°C		+8,-0					%
	0°C < T < 70°C		+1,-0					
Tracking error (measured relative to value at unity gain) equals $[V_O - V_O(\text{unity gain})]$ dB $- V_2$dBm	Rectifier input, $V_2 = +6$dBm, $V_1 = 0$dB		±.2					dB
	$V_2 = -30$dBm, $V_1 = 0$dB		+.2	-.5,+1		+.2	-1,+1.5	
Channel Separation		60				60		dB

NOTES:

1. Input to V_1 and V_2 grounded.
2. Measured at 0dBm, 1kHz.
3. Expandor ac input change from no signal to 0dBm.
4. Relative to value at $T_A = 25°C$.
5. Electrical characteristics for the SA571 only are specified over −40 to +85°C temperature range.

INTRODUCTION

Much interest has been expressed in high performance electronic gain control circuits. For non-critical applications, an integrated circuit operational transconductance amplifier can be used, but when high performance is required, one has to resort to complex discrete circuitry with many expensive, well matched components. This paper describes an inexpensive integrated circuit, the NE570 Compandor, which offers a pair of high performance gain control circuits featuring low distortion (<.1%), high signal to noise ratio (90dB), and wide dynamic range (110dB).

CIRCUIT BACKGROUND

The NE570 Compandor was originally designed to satisfy the requirements of the telephone system. When several telephone channels are multiplexed onto a common line, the resulting signal to noise ratio is poor and companding is used to allow a wider dynamic range to be passed through the channel. Figure 1 graphically shows what a compandor can do for the signal to noise ratio of a restricted dynamic range channel. The input level range of +20 to −80dB is shown undergoing a 2 to 1 compression where a 2dB input level change is compressed into a 1dB output level change by the compressor. The original 100dB of dynamic range is thus compressed to a 50dB range for transmission through a restricted dynamic range channel. A complementary expansion on the receiving end restores the original signal levels and reduces the channel noise by as much as 45dB.

The significant circuits in a compressor or expandor are the rectifier and the gain control element. The phone system requires a simple full wave averaging rectifier with good accuracy, since the rectifier accuracy determines the (input) output level tracking accuracy. The gain cell determines the distortion and noise characterics, and the phone system specifications here are very loose. These specs could have been met with a simple operational transconductance multiplier, or OTA, but the gain of an OTA is proportional to temperature and this is very undesirable. Therefore, a linearized transconductance multiplier was designed which is insensitive to temperature and offers low noise and low distortion performance. These features make the circuit useful in audio and data systems as well as in telecommunications systems.

BASIC CIRCUIT HOOKUP AND OPERATION

Figure 2 shows the block diagram of one half of the chip, (there are two identical channels on the I.C.). The full wave averaging rectifier provides a gain control current, I_G, for the variable gain (ΔG) cell. The output of the ΔG cell is a current which is fed to the summing node of the operational amplifier. Resistors are provided to establish circuit gain and set the output dc bias.

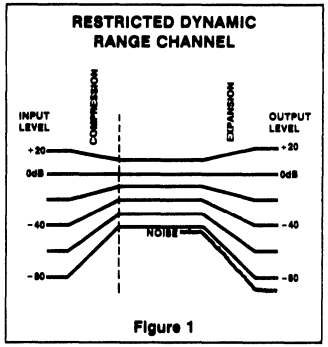


Figure 1

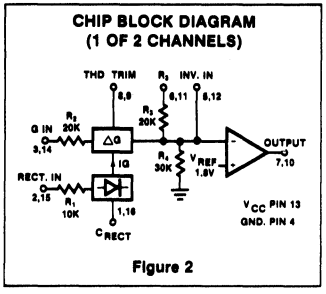


Figure 2

The circuit is intended for use in single power supply systems, so the internal summing nodes must be biased at some voltage above ground. An internal band gap voltage reference provides a very stable, low noise 1.8 volt reference denoted V_{ref}. The non-inverting input of the op amp is tied to V_{ref}, and the summing nodes of the rectifier and ΔG cell (located, at the right, of R_1 and R_2) have the same potential. The THD trim pin is also at the V_{ref} potential.

Figure 3 shows how the circuit is hooked up to realize an expandor. The input signal, V_{in}, is applied to the inputs of both the rectifier and the ΔG cell. When the input signal drops by 6dB, the gain control current will drop by a factor of 2, and so the gain will drop 6dB. The output level at V_{out} will thus drop 12dB, giving us the desired 2 to 1 expansion.

Figure 4 shows the hookup for a compressor. This is essentially an expandor placed in the feedback loop of the op amp. The ΔG cell is set up to provide ac feedback only, so a separate dc feedback loop is provided by the two R_{dc} and C_{dc}. The values of R_{dc} will determine the dc bias at the output of the op amp. The output will bias to:

$$V_{out}\,dc = 1 + \frac{R_{dc1}+R_{dc2}}{R_4} V_{ref} = \left(1 + \frac{R_{dc\ tot}}{30K}\right) 1.8V$$

The output of the expandor will bias up to:

$$V_{out}\,dc = 1 + \frac{R_3}{R_4} V_{ref} = \left(1 + \frac{20K}{30K}\right) 1.8V = 3.0V$$

The output will bias to 3.0V when the internal resistors are used. External resistors may be placed in series with R_3, (which will affect the gain), or in parallel with R_4 to raise the dc bias to any desired value.

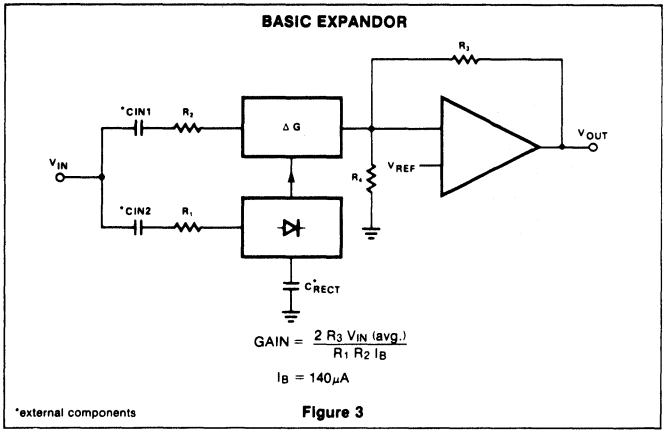


Figure 3

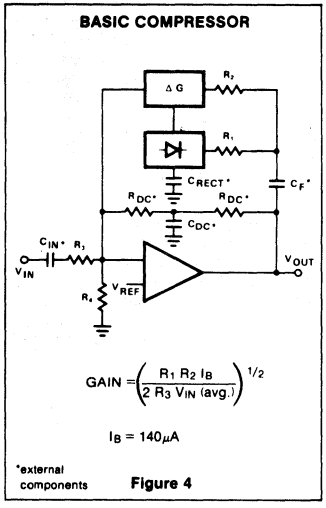


Figure 4

CIRCUIT DETAILS-RECTIFIER

Figure 5 shows the concept behind the full wave averaging rectifier. The input current to the summing node of the op amp, V_{in}/R_1, is supplied by the output of the op amp. If we can mirror the op amp output current into a unipolar current, we will have an ideal rectifier. The output current is averaged by R_5, Cr, which set the averaging time constant, and then mirrored with a gain of 2 to become I_G, the gain control current.

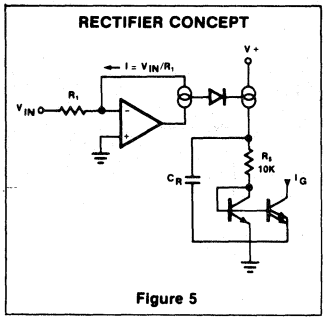


Figure 5

Figure 6 shows the rectifier circuit in more detail. The op amp is a one stage op amp, biased so that only one output device is on at a time. The non-inverting input, (the base of Q_1), which is shown grounded, is actually tied to the internal 1.8V V_{ref}. The inverting input is tied to the op amp output, (the emitters of Q_5 and Q_6), and the input summing resistor R_1. The single diode between

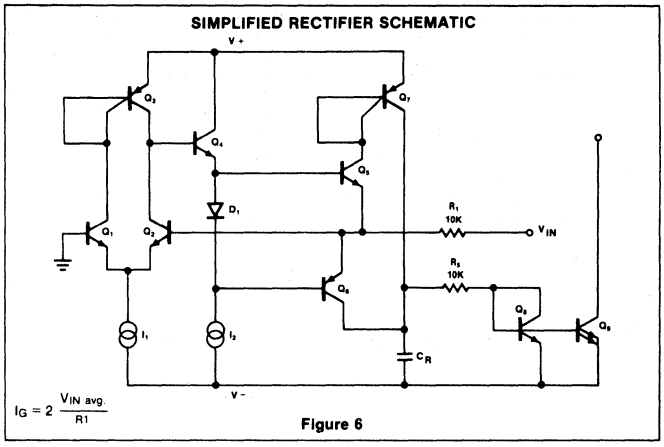


Figure 6

the bases of Q_5 and Q_6 assures that only one device is on at a time. To detect the output current of the op amp, we simply use the collector currents of the output devices Q_5 and Q_6. Q_6 will conduct when the input swings positive and Q_5 conducts when the input swings negative. The collector currents will be in error by the α of Q_5 or Q_6 on negative or positive signal swings, respectively. IC's such as this have typical npn β's of 200 and pnp β's of 40. The α's of .995 and .975 will produce errors of .5% on negative swings and 2.5% on positive swings. The 1.5% average of these errors yields a mere .13dB gain error.

At very low input signal levels the bias current of Q_2, (typically 50nA), will become significant as it must be supplied by Q_5. Another low level error can be caused by dc coupling into the rectifier. If an offset voltage exists between the V_{in} input pin and the base of Q_2, an error current of V_{os}/R_1 will be generated. A mere 1mv of offset will cause an input current of 100na which will produce twice the error of the input bias current. For highest accuracy, the rectifier should be coupled into capacitively. At high input levels the β of the pnp Q_6 will begin to suffer, and there will be an increasing error until the circuit saturates. Saturation can be avoided by limiting the current into the rectifier input to 250μa. If necessary, an external resistor may be placed in series with R_1 to limit the current to this value. Figure 7 shows the rectifier accuracy vs input level at a frequency of 1kHz.

At very high frequencies, the response of the rectifier will fall off. The rolloff will be more pronounced at lower input levels due to the increasing amount of gain required to switch between Q_5 or Q_6 conducting. The rectifier frequency response for input levels of 0dBm, -20dBm, and -40dBm is shown in Figure 8. The response at all three levels is flat to well above the audio range.

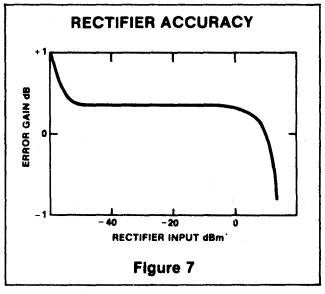


Figure 7

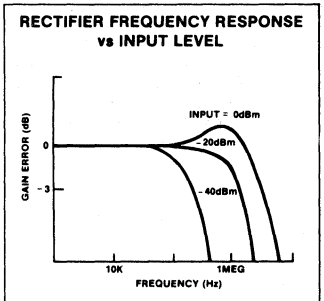


Figure 8

VARIABLE GAIN CELL

Figure 9 is a diagram of the variable gain cell. This is a linerarized two quadrant transconductance multiplier[1,2]. Q_1, Q_2 and the op amp provide a predistorted drive signal for the gain control pair, Q_3, Q_4. The gain is controlled by I_G and a current mirror provides the output current.

The op amp maintains the base and collector of Q_1 at ground potential (V_{ref}) by controlling the base of Q_2. The input current I_{in} ($= V_{IN}/R_2$) is thus forced to flow through Q_1 along with the current I_1, so $I_{C1} = I_1 + I_{in}$. Since I_2 has been set at twice the value of I_1, the current through Q_2 is $I_2-(I_1+I_{in}) = I_1-I_{in} = I_{C2}$. The op amp has thus forced a linear current swing between Q_1 and Q_2, by providing the proper drive to the base of Q_2. This drive signal will be linear for small signals, but very non-linear for large signals, since it is compensating for the non-linearity of the differential pair Q_1, Q_2 under large signal conditions.

The key to the circuit is that this same predistorted drive signal is applied to the gain control pair Q_3 and Q_4. When two differential pairs of transistors have the same signal applied, their collector current ratios will be identical, regardless of the magnitude of the currents. This gives us:

$$\frac{I_{C1}}{I_{C2}} = \frac{I_{C4}}{I_{C3}} = \frac{I_1+I_{in}}{I_1-I_{in}}$$

plus the relationships $I_G = I_{C3}+I_{C4}$ and $I_{out} = I_{C4}-I_{C3}$ will yield the multiplier transfer function,

$$I_{out} = \frac{I_G}{I_1} I_{in} = \frac{V_{in}}{R_2} \frac{I_G}{I_1}$$

this equation is linear and temperature insensitive, but it assumes ideal transistors.

If the transistors are not perfectly matched, a parabolic, non-linearity is generated, which results in 2nd harmonic distortion. Figure 10 gives an indication of the maginitude of the distortion caused by a given input level and offset voltage. The distortion is linearly proportional to the magnitude of the offset and the input level. Saturation of the gain cell occurs at a +8dBm level. At a nominal operating level of 0dBm, a 1mv offset will yield .34% of second harmonic distortion. Most circuits are somewhat better than this, which means our overall offsets are typically about 1/2mv. The distortion is not affected by the magnitude of the gain control current, and it does not increase as the gain is changed. This second harmonic distortion could be eliminated by making perfect transistors, but since that would be difficult, we have had to resort to other methods. A trim pin has been provided to allow trimming of the internal offsets to zero, which effectively eliminated second harmonic distortion. Figure 11 shows the simple trim network required.

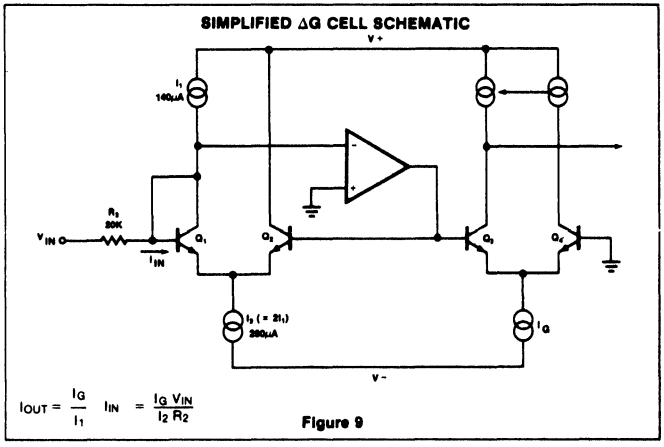


Figure 9

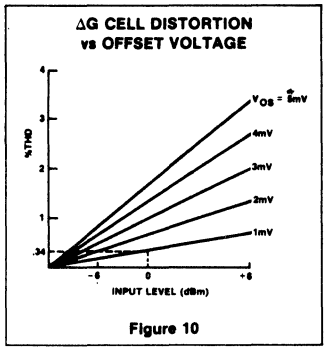


Figure 10

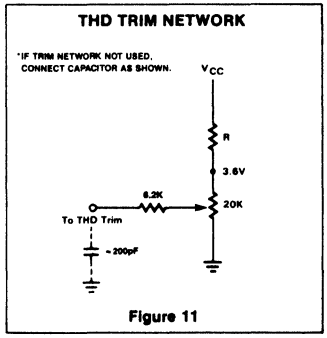


Figure 11

Figure 12 shows the noise performance of the ΔG cell. The maximum output level before clipping occurs in the gain cell is plotted along with the output noise in a 20kHz bandwidth. Note that the noise drops as the gain is reduced for the first 20dB of gain reduction. At high gains, the signal to noise ratio is 90dB, and the total dynamic range from maximum signal to minimum noise is 110dB.

Control signal feed-through is generated in the gain cell by imperfect device matching and mismatches in the current sources I_1 and I_2. When no input signal is present, changing I_G will cause a small output signal. The distortion trim is effective in nulling out any control signal feed-through, but in general, the null for minimum feed-through will be different than the null in distortion. The control signal feed-through can be trimmed independently of distortion by tying a current source to the ΔG input pin. This effectively trims I_1. Figure 13 shows such a trim network.

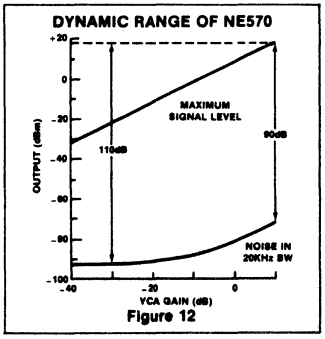


Figure 12

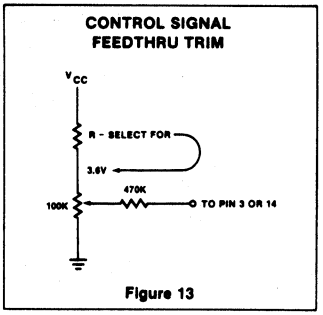


Figure 13

OPERATIONAL AMPLIFIER

The main op amp shown in the chip block diagram is equivalent to a 741 with a 1MHz bandwidth. Figure 14 shows the basic circuit. Split collectors are used in the input pair to reduce g_m, so that a small compensation capacitor of just 10pf may be used. The output stage, although capable of output currents in excess of 20ma., is biased for a low quiescent current to conserve power. When driving heavy loads, this leads to a small amount of crossover distortion.

RESISTORS

Inspection of the gain equations in Figure 3 and 4 will show that the basic compressor and expandor circuit gains may be set entirely by resistor ratios and the internal voltage reference. Thus, any form of resistors that match well would suffice for these simple hookups, and absolute accuracy and temperature coefficient would be of no importance. However, as one starts to modify the gain equation with external resistors, the internal resistor accuracy and tempco become very significant. Figure 15 shows the effects of temperature on the diffused resistors which are normally used in integrated circuits, and the ion implanted resistors which are used in this circuit. Over the critical 0°C to 70°C temperature range, there is a 10 to 1 improvement in drift from a 5% change for the diffused resistors, to a .5% change for the implemented resistors. The implanted resistors have another advantage in that they can be made 1/7 the size of the diffused resistors due to the higher resistivity. This saves a significant amount of chip area.

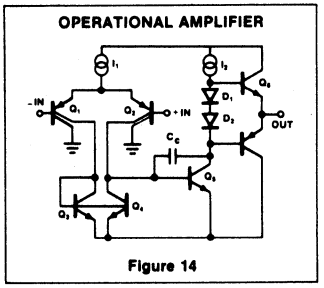


Figure 14

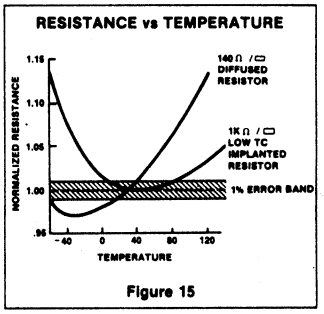


Figure 15

***For additional information, consult the Applications Section.**

PROGRAMMABLE ANALOG COMPANDOR

DESCRIPTION

The NE572 is a dual channel, high performance gain control circuit in which either channel may be used for dynamic range compression or expansion. Each channel has a full wave rectifier to detect the average value of input signal; a linearized, temperature compensated variable gain cell (ΔG) and a dynamic time constant buffer. The buffer permits independent control of dynamic attack and recovery time with minimum external components and improved low frequency gain control ripple distortion over previous compandors.

The NE572 is intended for noise reduction in high performance audio systems. It can also be used in a wide range of communication systems and video recording applications.

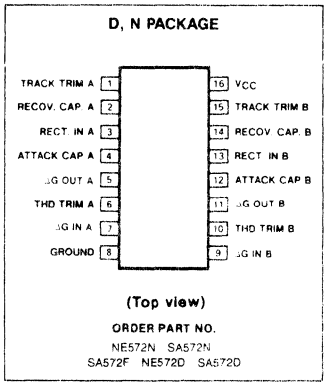
FEATURES

- **Independent control of attack and recovery time.**
- **Improved low frequency gain control ripple**
- **Complementary gain compression and expansion with external Op Amp**
- **Wide dynamic range—greater than 110dB**
- **Temperature compensated gain control**
- **Low distortion gain cell**
- **Low noise—6μV typical**
- **Wide supply voltage range—6V–22V**
- **System level adjustable with external components.**

APPLICATIONS

- **Dynamic noise reduction system**
- **Voltage control amplifier**
- **Stereo expandor**
- **Automatic level control**
- **High level limiter**
- **Low level noise gate**
- **State variable filter**

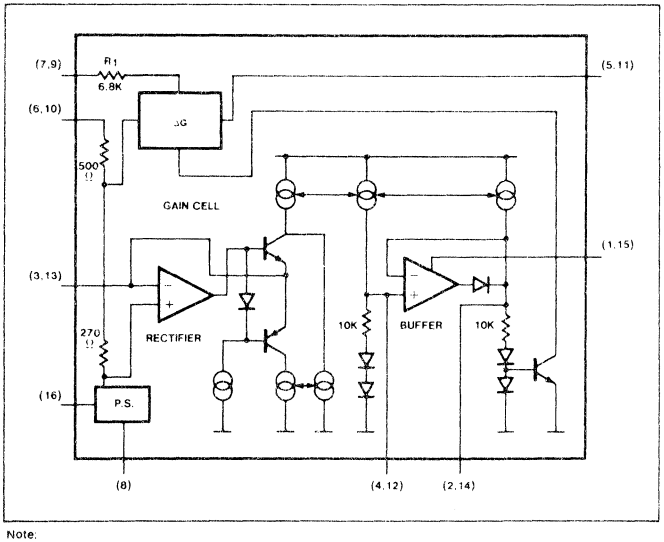
PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
V_{CC}	Supply voltage	22	VDC
T_A	Operating temperature range	0 to 70	°C
P_D	Power dissipation	500	mW

BLOCK DIAGRAM

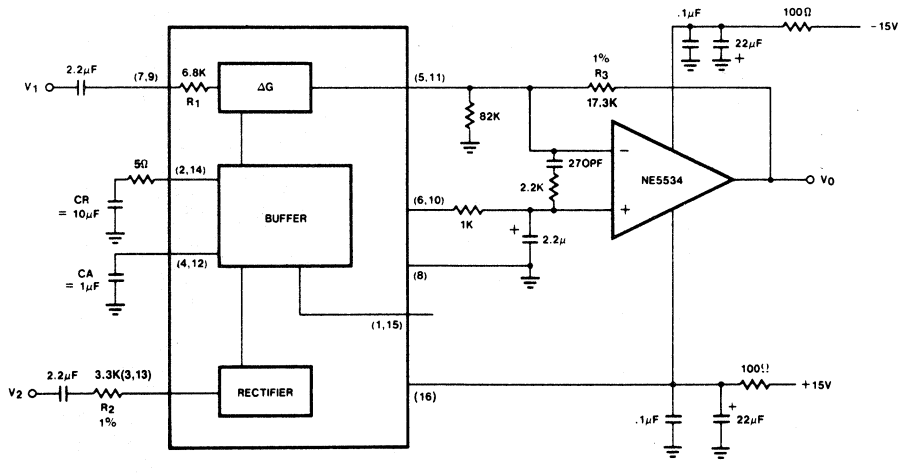


Note:
1. Supplied only in large SO (Small Outline) package.

ELECTRICAL CHARACTERISTICS Standard Test Conditions (unless otherwise noted) V_{CC} = 15V TA = 25°C Expandor mode (see test circuit) Input signals at unity gain level (OdB) = 100mV RMS at 1KHz, $V_1 = V_2$, R_2 = 3.3K, R_3 = 17.3K

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V_{CC}	Supply voltage		6		22	V_{DC}
I_{CC}	Supply current	No Signal			6	mA
	Internal voltage reference		2.3	2.5	2.7	V_{DC}
THD	(untrimmed)	1kHz C_A = 1.0μF		.2	1.0	%
THD	(trimmed)	1kHz C_R = 10μF		.05		%
THD	(trimmed)	100Hz		.25		%
	No signal output noise	Input to V_1 and V_2 grounded (20-20kHz)		6	25	uV
	DC level shift (untrimmed)	Input change from no signal to 100mV RMS		±20	±50	MV
	Unity gain level		−1	0	+1	dB
	Large signal distortion	$V_1 = V_2$ = 400mV		0.7	3.0	%
	Tracking error (measured relative to value at unity gain output) = [$V_O - V_O$(unity gain)] dB − V_2 (dBm)	Rectifier input V_2 = +6dB, V_1 = OdB V_2 = −30dB, V_1 = OdB		±.2 ±.5	 −1.5 +.8	dB
	Channel crosstalk	200mV RMS into channel A, measured output on channel B	60			dB
	Power supply rejection ratio	120Hz		70		dB

TEST CIRCUIT



AUDIO SIGNAL PROCESSING IC COMBINES VCA AND FAST ATTACK-SLOW RECOVERY LEVEL SENSOR

In high performance audio gain control applications it is desirable to independently control the attack and recovery time of the gain control signal. This is true, for example, in compandor applications for noise reduction. In high end systems the input signal is usually split into two or more frequency bands to optimize the dynamic behavior for each band. This reduces low frequency distortion due to control signal ripple, phase distortion, high frequency channel overload and noise modulation. Because of the expense in hardware, multiple band signal processing up to now was limited to professional audio applications.

With the introduction of the Signetics NE572 this high performance noise reduction concept becomes feasible for consumer hi fi applications. The NE572 is a dual channel gain control IC. Each channel has a linearized, temperature compensated gain cell and an improved level sensor. In conjunction with an external low noise op amp for current to voltage conversion, the VCA features low distortion, low noise and wide dynamic range. The novel level sensor which provides gain control current for the VCA gives lower gain control ripple and independent control of fast attack, slow recovery dynamic response. An attack capacitor CA with an internal 10K resistor RA defines the attack time TA. The recovery time TR of a tone burst is defined by a recovery capacitor CR and an internal 10K resistor R_R. Typical attack time of 4MS for the high frequency spectrum and 40MS for the low frequency band can be obtained with .1μF and 1.0μF attack capacitors respectively. Recovery time of 200MS can be obtained with a 4.7μF external capacitor. With the recovery capacitor added in the level sensor, the gain control ripple for low frequency signals is much lower than that of a simple RC ripple filter. As a result the residual third harmonic distortion of low frequency signal in a two quad transconductance amplifier is greatly improved. With the 1.0μF attack capacitor and 4.7μF recovery capacitor for a 100HZ signal the third harmonic distortion is improved by more than 10db over the simple RC ripple filter with a single 1.0μF attack and recovery capacitor, while the attack time remains the same.

The NE572 is assembled in a standard 16 pin dual in line plastic package and in oversized SO (Small Outline) package. It operates over wide supply range from 6V to 22V. Supply current is less than 6mA. The NE572 is designed for consumer application over a temperature range 0-70°C. The SA572 is intended for applications from −40°C to +85°C.

NE572 BASIC APPLICATIONS

Description

The NE572 consists of two linearized, temperature compensated gain cells (ΔG) each with a full-wave rectifier and a buffer amplifier as shown in the block diagram. The two channels share a 2.5V common bias reference derived from the power supply but otherwise operate independently. Because of inherent low distortion, low noise and the capability to linearize large signals, a wide dynamic range can be obtained. The buffer amplifiers are provided to permit control of attack time and recovery time independent of each other. Partitioned as shown in the block diagram, the IC allows flexibility in the design of system levels that optimize DC shift, ripple distortion, tracking accuracy and noise floor for a wide range of application requirements.

Gain Cell

Figure 1 shows the circuit configuration of the gain cell. Bases of the differential pairs $Q_1 - Q_2$ and $Q_3 - Q_4$ are both tied to the output and inputs of OPA A_1. The negative feedback through Q_1 holds the V_{BE} of $Q_1 - Q_2$ and the V_{BE} of $Q_3 - Q_4$ equal. The following relationship can be derived from the transistor model equation in the forward active region.

$$\Delta V_{BE_{Q_3-Q_4}} = \Delta_{BE_{Q_1-Q_2}}$$

$$(V_{BE} = V_T \ln IC/IS)$$

$$V_T \ln\left(\frac{\frac{1}{2}I_G + \frac{1}{2}I_O}{I_S}\right) - V_T \ln\left(\frac{\frac{1}{2}I_G - \frac{1}{2}I_O}{I_S}\right)$$

$$= V_T \ln\left(\frac{I_1 + I_{in}}{I_S}\right) - V_T \ln\left(\frac{I_2 - I_1 - I_{in}}{I_S}\right) \quad \text{--(2)}$$

where $I_{in} = \frac{V_{in}}{R_1}$

$R_1 = 6.8K$

$I_1 = 140\mu A$

$I_2 = 280\mu A$

I_O is the differential output current of the gain cell and I_G is the gain control current of the gain cell.

If all transistors Q_1 through Q_4 are of the same size, equation (2) can be simplfied to:

$$I_O = \frac{2}{I_2} \cdot I_{in} \cdot I_G - \frac{1}{I_2}(I_2 - 2I_1) \cdot I_G \qquad (3)$$

The first term of eqn. (3) shows the multiplier relationship of a linearized two quadrant transconductance amplifier. The second term is the gain control feed through due to the mismatch of devices. In the design this

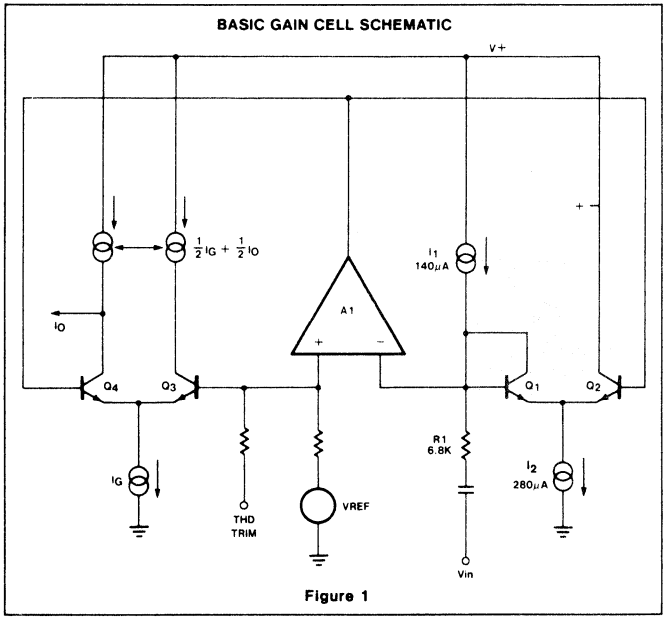


Figure 1

has been minimized by large matched devices and careful layout. Offset voltage is caused by the device mismatch and it leads to even harmonic distortion. The offset voltage can be trimmed out by feeding a current source within ±25μA into the THD trim pin. The residual distortion is third harmonic distortion and is caused by gain control ripple. In a compandor system, available control of fast attack and slow recovery improves ripple distortion significantly. At the unity gain level of 100mV, the gain cell gives THD (total harmonic distortion) of .17% TYP. Output noise with no input signals is only 6μV in the audio spectrum (10HZ-20KHZ). The output current I_O must feed the virtual ground input of an operational amplifier with a resistor from output to inverting input. The non-inverting input of the operational amplifier has to be biased at VREF if the output current I_O is dc coupled.

Rectifier

The rectifier is a full-wave design as shown in Figure 2. The input voltage is converted to current through the input resistor R2 and turns on either Q5 or Q6 depending on the signal polarity. Deadband of the voltage to current converter is reduced by the loop gain of the gain block A2. If AC coupling is used, the rectifier error comes only from input bias current of gain block A2. The input bias current is typically about 70nA. Frequency response of the gain block A2 also causes second order error at high frequency. The collector current of Q6 is mirrored and summed at the collector of Q5 to form the full wave rectified output current I_R. The rectifier transfer function is

$$\frac{V_{IN} - V_{REF}}{R_2} \qquad (4)$$

If Vin is A.C. coupled, then the equation will be reduced to:

$$I_{RAC} = \frac{Vin\,(AVG)}{R_2}$$

The internal bias scheme limits the maximum output current I_R to be around 300μA. Within a ± 1dB error band the input range of the rectifier is about 52dB.

Buffer Amplifier

In audio systems, it is desirable to have fast attack time and slow recovery time for a tone burst input. The fast attack time reduces transient channel overload but also causes low frequency ripple distortion. The low frequency ripple distortion can be improved with the slow recovery time. If different attack times are implemented in corresponding frequency spectrums in a split band audio system, high quality performance can be achieved. The buffer amplifier is designed to make this feature available with minimum external components. Refer-

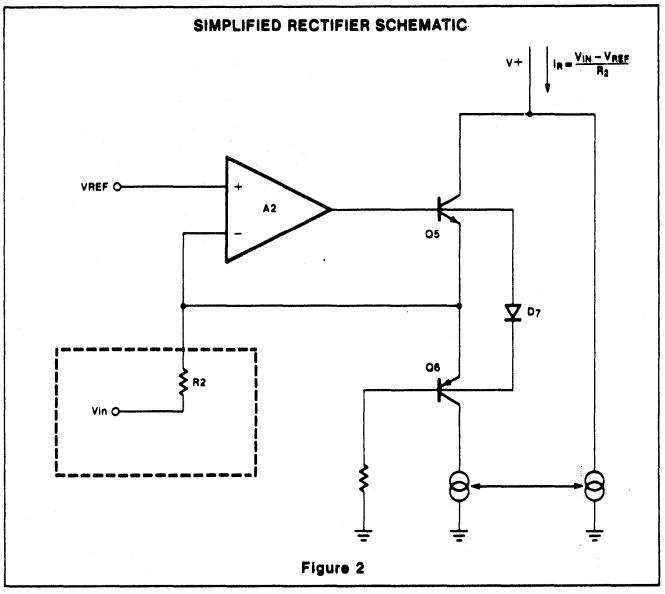


Figure 2

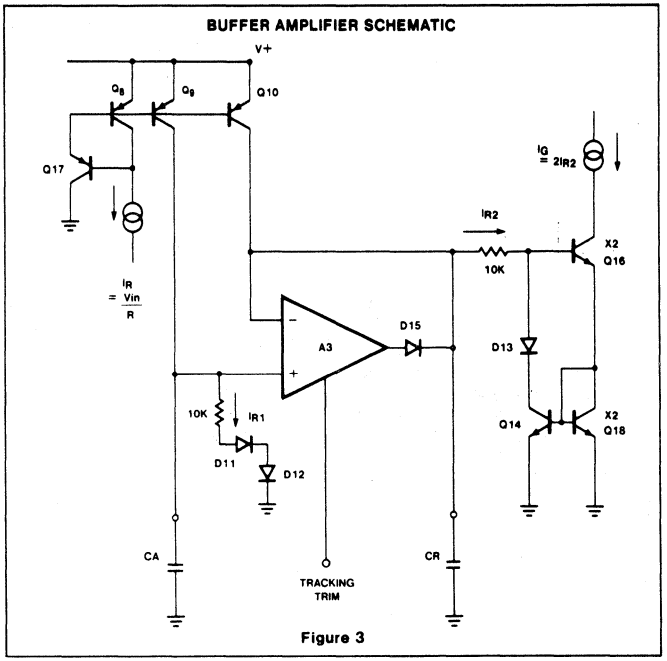


Figure 3

ring to Figure 3, the rectifier output current is mirrored into the input and output of the unipolar buffer amplifier A_3 through Q_8, Q_9 and Q_{10}. Diodes D_{11} and D_{12} improve tracking accuracy and provide common mode bias for A_3. For a positive going input signal, the buffer amplifier acts like a voltage follower. Therefore, the output impedance of A_3 makes the contribution of capacitor CR to attack time insignificant. Neglecting diode impedance the gain Ga(t) for ΔG can be expressed as follows.

$$Ga(t) = (Ga_{INT} - Ga_{FNL}) \cdot e^{\frac{-t}{\tau A}} + Ga_{FNL}$$

Ga_{INT} = Initial Gain

$\tau A = R_A \cdot CA = 10K \cdot CA$ Ga_{FNL} = Final Gain

where τA is the attack time constant and RA is a 10K internal resistor. Diode D_{15} opens the feedback loop of A_3 for a negative going signal if the value of capacitor CR is larger than capacitor CA. The recovery time depends only on CR • R_R. If the diode impedance is assumed negligible, the dynamic gain G_R (t) for ΔG is expressed as follows.

$$G_R(t) = (G_{R\,INT} - G_{R\,FNL}) \cdot e^{\frac{-t}{\tau R}} + G_{R\,FNL}$$

$\tau R = R_R \cdot CR = 10K \cdot CR$

where τR is the recovery time constant and R_R is a 10K internal resistor. The gain control current is mirrored to the gain cell through Q_{14}. The low level gain errors due to input bias current of A_2 and A_3 can be trimmed through the tracking trim PIN into A_3 with a current source of $\pm 3\mu A$.

Basic Expandor

Figure 4 shows an application of the circuit as a simple expandor. The gain expression of the system is given by

$$\frac{V_{OUT}}{V_{IN}} = \frac{2}{I_1} \cdot \frac{R_3 \cdot V_{IN(AVG)}}{R_2 \cdot R_1\ (I_1 = 140\mu A)} \qquad (5)$$

Both the resistors R_1 and R_2 are tied to internal summing nodes. R_1 is a 6.8K internal resistor. The maximum input current into the gain cell can be as large as $140\mu A$. This corresponds to a voltage level of $140\mu A$ • 6.8K = 952mV peak. The input peak current into the rectifier is limited to $300\mu A$ by the internal bias system. Note that the value of R_1 can be increased to accommodate higher input level. R_2 and R_3 are external resistors. It is easy to adjust the ratio of R3/R2 for desirable system voltage and current levels. A small R2 results in higher gain control current and smaller static and dynamic tracking error. However, an impedance buffer A_1 may be necessary if the input is voltage drive with large source impedance.

The gain cell output current feeds the summing node of the external OPA A_2. R_3 and A_2 convert the gain cell output current to the output voltage. In high performance applications, A_2 has to be low noise, high speed and wide band so that the high performance output of the gain cell will not be degraded. The non-inverting input of A_2 can be biased at the low noise internal reference PIN 6 or 10. Resistor R_4 is used to biased up the output DC level of A_2 for maximum swing. The output DC level of A_2 is given by

$$V_{ODC} = V_{REF}\left(1 + \frac{R_3}{R_4}\right) - V_B\frac{R_3}{R_4} \qquad (6)$$

V_B can be tied to a regulated power supply for a dual supply system and be grounded for a single supply system. CA sets the attack time constant and CR sets the recovery time constant.

BASIC EXPANDOR SCHEMATIC

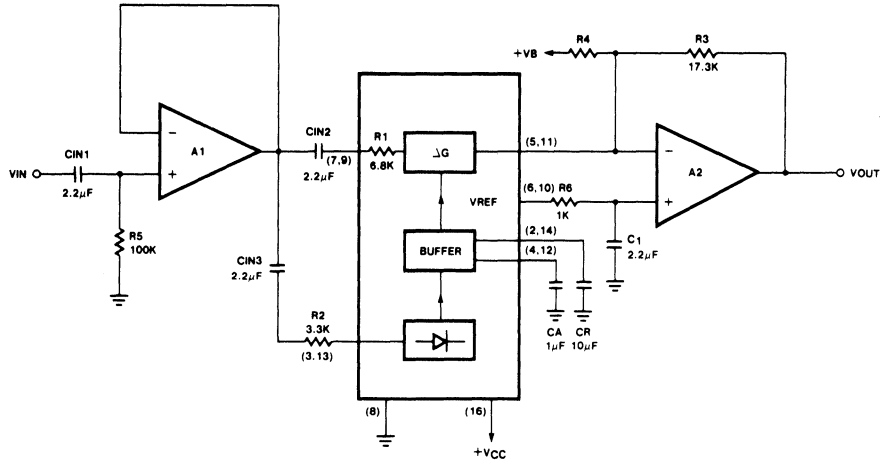


Figure 4

Basic Compressor

Figure 5 shows the hook-up of the circuit as a compressor. The IC is put in the feedback loop of the OPA A_1. The system gain expression is as follows:

$$\frac{V_{OUT}}{V_{IN}} = \left(\frac{I_1}{2} \cdot \frac{R_2 \cdot R_1}{R_3 \cdot V_{IN}(AVG)}\right)^{1/2} \quad (7)$$

RDC1, RDC2, and CDC form a dc feedback for A_1. The output DC level of A_1 is given by

$$V_{ODC} = V_{REF}\left(1 + \frac{R_{DC1} + R_{DC2}}{R_4}\right) - V_B \cdot \left(\frac{R_{DC1} + R_{DC2}}{R_4}\right) \quad (8)$$

The zener diodes D_1 and D_2 are used for channel overload protection.

Basic Compandor System

The above basic compressor and expandor can be applied to systems such as tape/disc noise reduction, digital audio, bucket brigade delay lines. Additional system design techniques such as bandlimiting, band splitting, pre-emphasis, de-emphasis and equalization are easy to incorporate. The IC is a versatile functional block to achieve a high performance audio system. Figure 6 shows the system level diagram for reference.

For additional information, refer to the Applications Section.

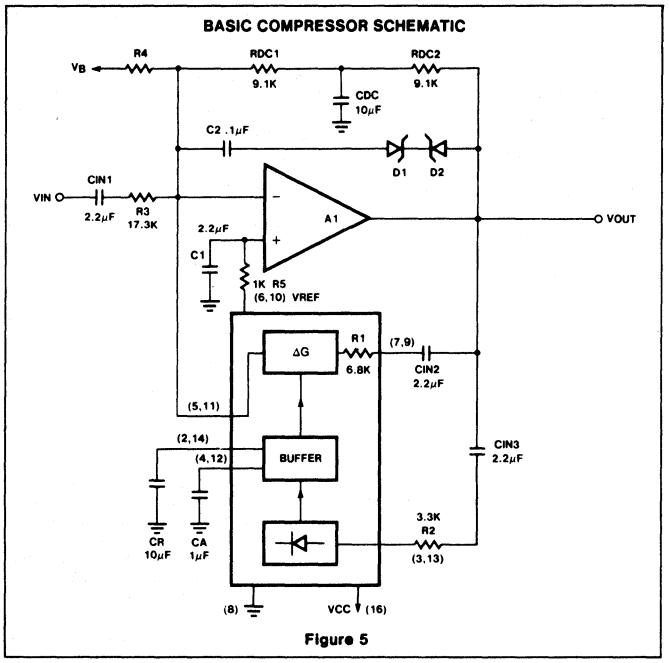


Figure 5

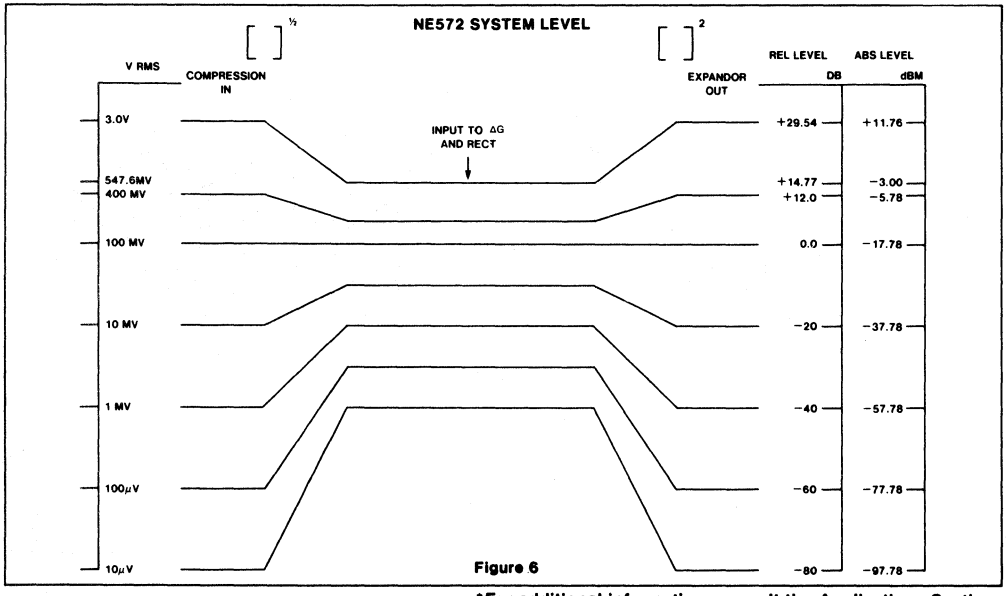


Figure 6

*For additional information, consult the Applications Section.

Double Balanced Mixer And Oscillator

Linear Products

DESCRIPTION

The SA/NE602 is a low-power VHF monolithic double balanced mixer with input amplifier, on-board oscillator, and voltage regulator. It is intended for high performance, low power communication systems. The guaranteed parameters of the SA602 make this device particularly well suited for cellular radio applications. The mixer is a "Gilbert cell" multiplier configuration which typically provides 18dB of gain at 45MHz. The oscillator will operate to 200MHz. It can be configured as a crystal oscillator, a tuned tank oscillator, or a buffer for an external L.O. The noise figure at 45MHz is typically less than 5dB. The gain, intercept performance, low-power and noise characteristics make the SA/NE602 a superior choice for high-performance battery operated equipment. It is available in an 8-lead dual-in-line plastic package and an 8-lead SO (surface-mount miniature package).

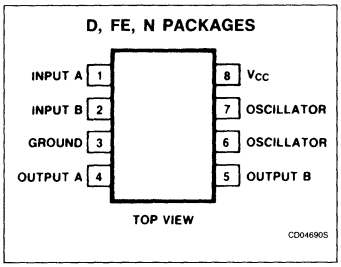
FEATURES

- **Low current consumption: 2.4mA typical**
- **Excellent noise figure: < 5.0dB typical at 45MHz**
- **High operating frequency**
- **Excellent gain, intercept and sensitivity**
- **Low external parts count; suitable for crystal/ceramic filters**
- **SA602 meets cellular radio specifications**

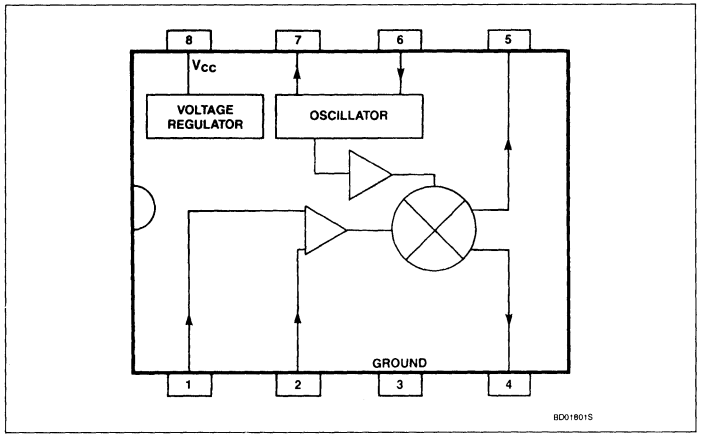
APPLICATIONS

- **Cellular radio mixer/oscillator**
- **Portable radio**
- **VHF transceivers**
- **RF data links**
- **HF/VHF frequency conversion**
- **Instrumentation frequency conversion**
- **Broadband LAN's**

PIN CONFIGURATION



BLOCK DIAGRAM



ORDERING CODE

DESCRIPTION	ORDER CODE
Dual-in-Line, Plastic; 0 to +70°C	NE602N
Dual-in-Line, Small Outline; 0 to +70°C	NE602D
Cerdip; 0 to 70°C	NE602FE
Dual-in-Line, Plastic; −40 to +85°C	SA602N
Dual-in-Line, Small Outline; −40 to +85°C	SA602D
Cerdip; −40 to +85°C	SA602FE

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Maximum operating voltage	9	V
Storage temperature	−65 to +150	°C
Operating temperature NE602 SA602	 0 to +70 −40 to +85	 °C °C

AC/DC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_{CC} = 6V$, Figure 1

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Power supply voltage range		4.5		8.0	V
DC current drain			2.4	2.8	mA
Input signal frequency			500		MHz
Oscillator frequency			200		MHz
Noise figured at 45MHz			5.0	6.0	dB
Third order intercept point	RF_{IN} = −45dBm: f_1 = 45.0 f_2 = 45.06		−15	−17	dBm
Conversion gain at 45MHz		14			dB
RF input resistance		1.5			kΩ
RF input capacitance			3	3.5	pF
Mixer output resistance	(Pin 4 or 5)		1.5		kΩ

TEST CONFIGURATION

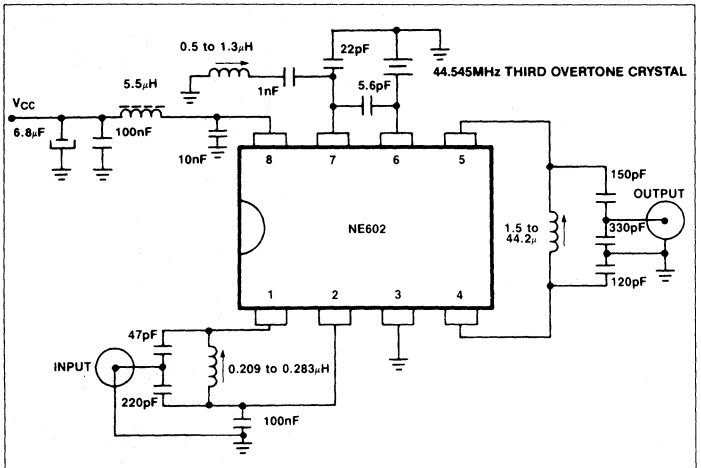


Figure 1

DESCRIPTION OF OPERATION

The SA/NE602 is a Gilbert cell, an oscillator/buffer, and a temperature compensated bias network as shown in the equivalent circuit. The Gilbert cell is a differential amplifier (Pins 1 and 2) which drives a balanced switching cell. The differential input stage provides gain and determines the noise figure and signal handling performance of the system.

The SA/NE602 is designed for optimum low power performance. When used with the SA604 as a 45MHz cellular radio 2nd IF and demodulator, the SA602 is capable of receiving −119dBm signals with a 12dB S/N ratio. Third order intercept is typically −15dBm (that's approximately +5dBm output intercept because of the RF gain). The system designer must be cognizant of this large signal limitation. When designing LAN's or other closed systems where transmission levels are high, and small signal or signal-to-noise issues not critical, the input to the NE602 should be appropriately scaled.

Besides excellent low power performance well into VHF, the SA/NE602 is designed to be flexible. The input, output, and oscillator ports can support a variety of configurations provided the designer understands certain constraints, which will be explained here.

The RF inputs (Pins 1 and 2) are biased internally. They are symmetrical. The equivalent AC input impedence is approximately 1.5K || 3pF through 50MHz. Pins 1 and 2 can be used interchangeably, but they should not be DC biased externally. Figure 3 shows three typical input configurations.

The mixer outputs (Pins 4 and 5) are also internally biased. Each output is connected to the internal positive supply by a 1.5kΩ resistor. This permits direct output termination yet allows for balanced output as well. Figure 4 shows three single ended output configurations and a balanced output.

The oscillator is capable of sustaining oscillation beyond 200MHz in crystal or tuned tank configurations. The upper limit of operation is determined by tank "Q" and required drive levels. The higher the "Q" of the tank or the smaller the required drive, the higher the permissible oscillation frequency. If the required L.O. is beyond oscillation limits, or the system calls for an external L.O., the external signal can be injected at Pin 6 through a DC blocking capacitor. External L.O. should be at least 200mVpp.

Figure 5 shows several proven oscillator circuits. Figure 5A is appropriate for cellular radio. As shown, an overtone mode of operation is utilized. Capacitor C3 and inductor L1 suppress oscillation at the crystal fundamental frequency. In the fundamental mode, the suppression network is omitted.

Figure 6 shows a Colpitts varacter tuned tank oscillator suitable for synthesizer controlled applications. It is important to buffer the output of this circuit to assure that switching spikes from the first counter or prescaler do not end up in the oscillator spectrum. The dual-gate MOSFET provides optimum isolation with low current. The FET offers good isolation, simplicity, and low current, while the bipolar transistors provide the simple solution for non-critical applications. The resistive divider in the emitter follower circuit should be chosen to provide the minimum input signal which will assure correct system operation.

When operated above 100MHz, the oscillator may not start if the Q of the tank is too low. A 22kΩ resistor from Pin 7 to ground will increase the DC bias current of the oscillator transistor. This improves the AC operating characteristic of the transistor and should help the oscillator to start. 22kΩ will not upset the other DC biasing internal to the device, but smaller resistance values should be avoided.

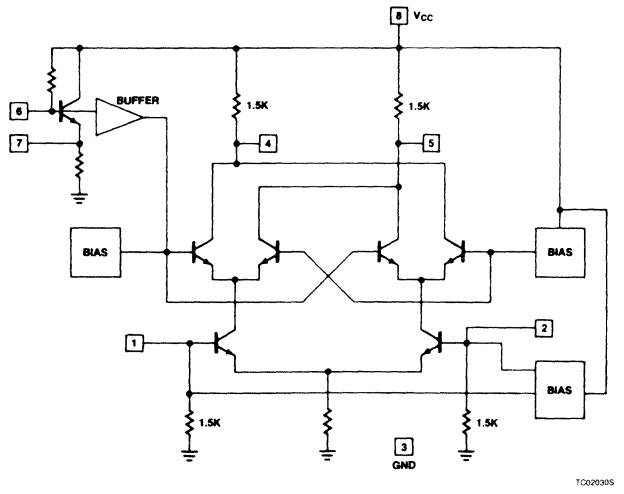
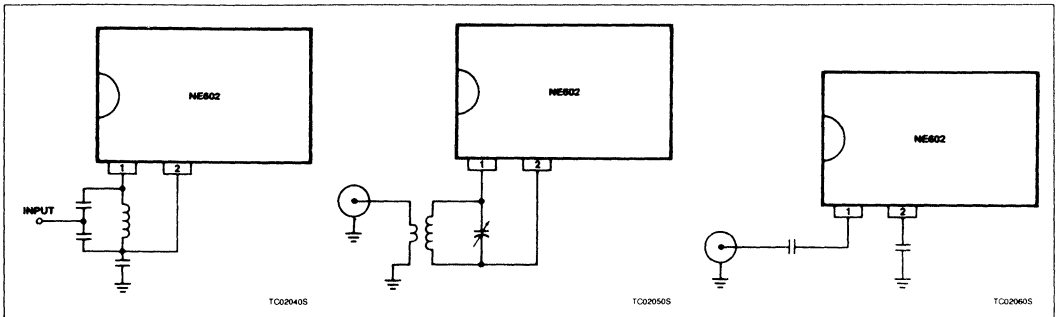


Figure 2. Equivalent Circuit

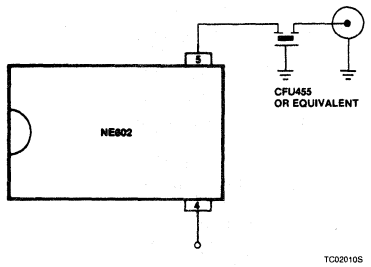


a. Single-Ended Tuned Input

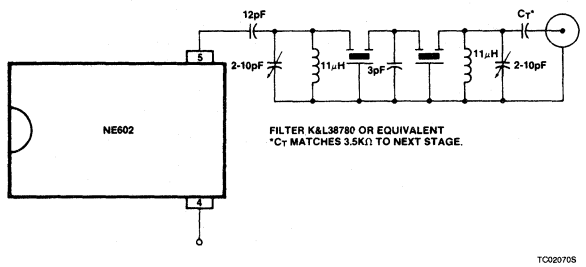
b. Balanced Input (For Attenuation Of Second Order Products)

c. Single-Ended Untuned Input

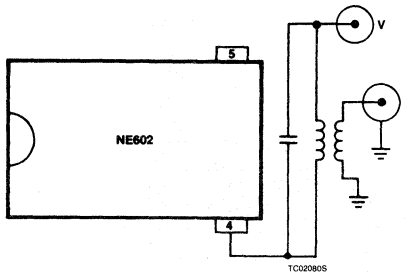
Figure 3. Input Configuration



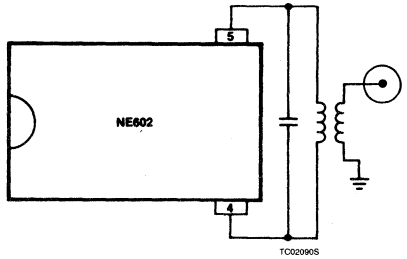
a. Single-Ended Ceramic Filter



b. Single-Ended Crystal Filter

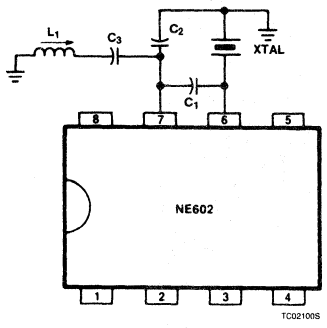


c. Single-Ended IFT

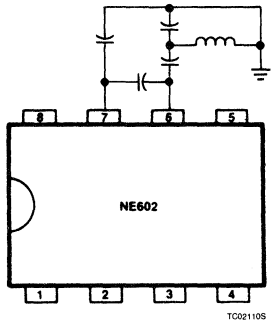


d. Balanced Output

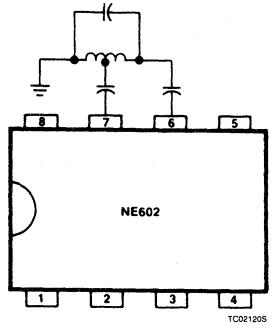
Figure 4. Output Configuration



a. Colpitts Crystal Oscillator (Overtone Mode)



b. Colpitts L/C Tank Oscillator



c. Hartley L/C Tank Oscillator

Figure 5. Oscillator Circuits

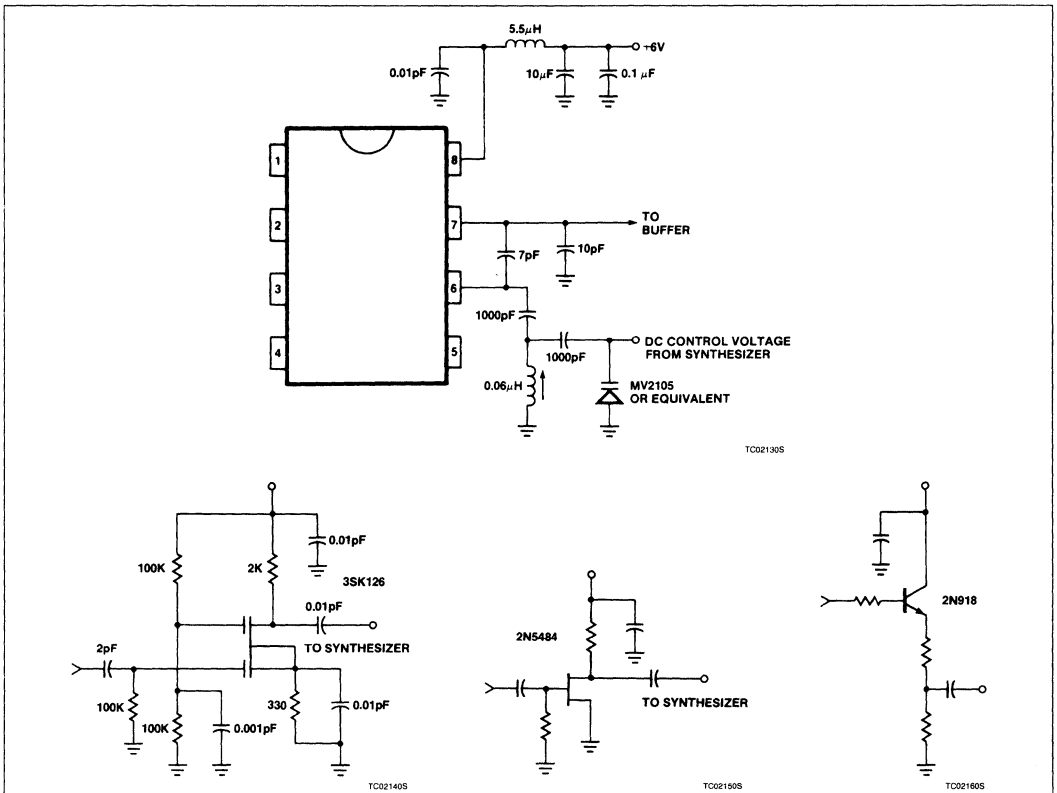


Figure 6. Colpitts Oscillator Suitable For Synthesizer Applications And Typical Buffers

TEST CONFIGURATION

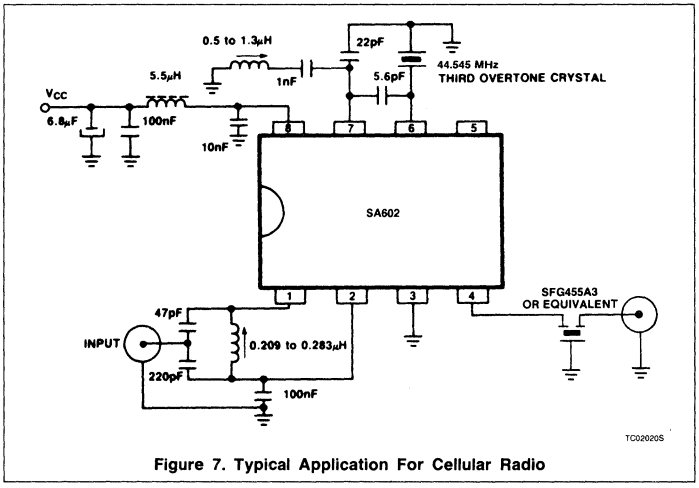


Figure 7. Typical Application For Cellular Radio

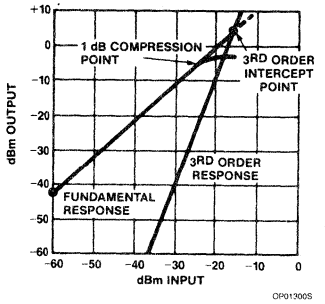


Figure 8. SA/NE602 3RD Order Intermod And 1dB Compression Point Performance

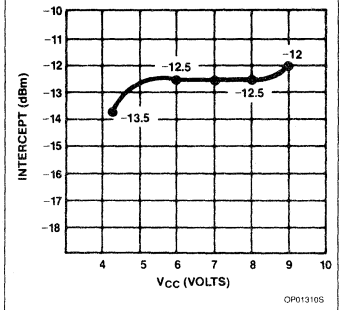


Figure 9. Input Third Order Intercept Point Vs V_{CC}

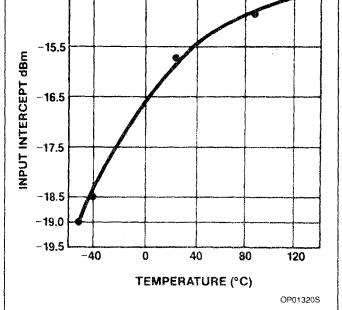


Figure 10. Third Order Intercept Point vs Temperature

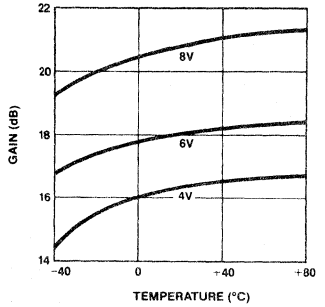


Figure 11

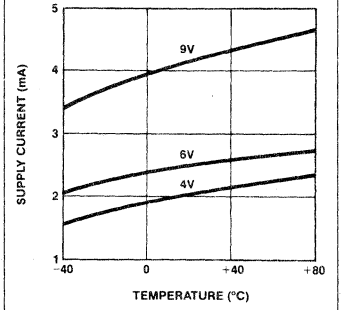


Figure 12

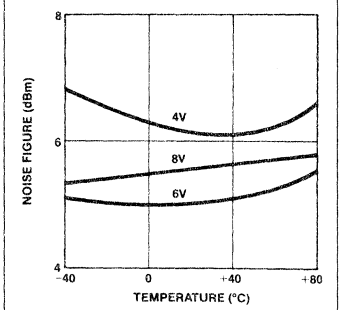


Figure 13

Low Power FM I.F. System

DESCRIPTION

The SA/NE604 is a monolithic low power FM IF system incorporating two limiting intermediate frequency amplifiers, quadrature detector, muting, logarithmic signal strength indicator, and voltage regulator. The SA/NE604 is available in a 16 lead dual-in-line plastic package and 16 lead SO (surface mounted miniature package).

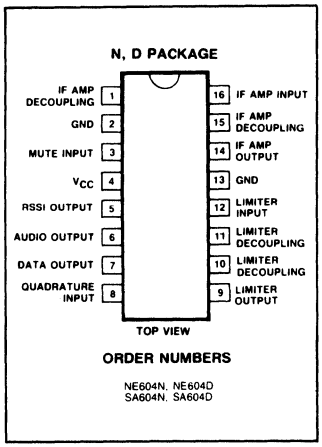
FEATURES

- **Low power consumption: 2.3mA typical**
- **Logarithmic Received Signal Strength Indicator (RSSI) with a dynamic range in excess of 90dB**
- **Separate data output**
- **Audio output with muting**
- **Low external count; suitable for crystal/ceramic filters**
- **Excellent sensitivity: 1.5μV across input pins (0.27 μV into 50Ω matching network) for 12dB SINAD (Signal to Noise and Distortion ratio) at 455kHz**

APPLICATIONS

- **Cellular Radio FM IF**
- **Communications receivers**
- **Intermediate frequency amplification and detection up to 10.7MHz**
- **RF level meter**
- **Spectrum analyzer**

PIN CONFIGURATION



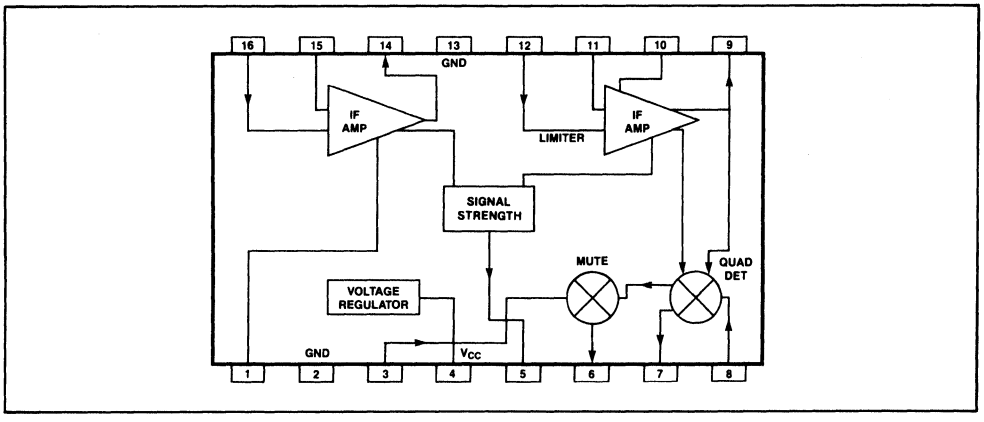
ORDER NUMBERS

NE604N, NE604D
SA604N, SA604D

ABSOLUTE MAXIMUM RATINGS

SYMBOL AND PARAMETER	RATING	UNIT
Maximum operating voltage	9	V
Storage temperature	−65 to +150	°C
Operating temperature		
NE604	0 to +70	°C
SA604	−40 to +85	°C

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

$T_A = 25°C$, $V_{CC} = +6$ volts, unless otherwise stated.

SYMBOL AND PARAMETER	SA/NE604			UNITS
	Min	Typ	Max	
Power supply voltage range	4.5	-	8.0	V
D.C. current drain	-	2.3	2.7	mA
I.F. frequency	-	-	10.7	MHz
RSSI range	TBD	90	-	dB
RSSI accuracy	-	±1.5	-	dB
I.F. input impedance	1.5	-	-	kΩ
I.F. output impedance	1.0	-	-	kΩ
Limiter input impedance	1.5	-	-	kΩ
Quadrature detector data output impedance	50	-	-	kΩ
Muted audio out impedance	-	50	-	kΩ
Mute - switch input threshold (on)	1.7	-	-	V
(off)	-	-	1.0	V

CIRCUIT DESCRIPTION

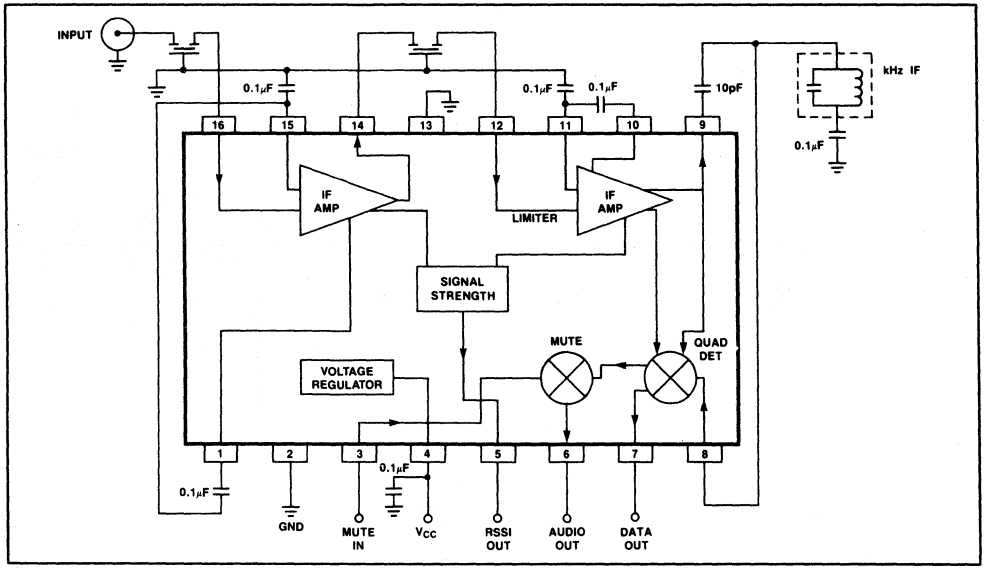
The SA/NE604's IF amplifier has a gain of 30dB, bandwidth of 15MHz, with an input impedance of 1.5KΩ and an output impedance of 1.0KΩ. The limiter has a gain of 60dB, bandwidth of 15MHz, and an input impedance of 1.5KΩ. An interstage filter between the IF Amplifier and Limiter is recommended to reduce wideband noise. The quadrature detector input (pin 8) impedance is 40KΩ.

The data (unmuted output) and audio (muted output) both have 50KΩ output impedance and their detected signals are 180 degrees out of phase with each other. The mute input (pin 3) has a very high impedance and is compatible with three and five volt CMOS and TTL levels. Little or no DC level shift occurs after muting when the quadrature detector is adjusted to the IF center frequency. Muting will attenuate the audio signal by more than 60dB and no voltage spikes will be generated by muting.

The logarithmic signal strength indicator is a current source output with maximum source current of 50 microamps. The signal strength indicator's transfer function is approximately 10 microamp per 20dB and is independent of IF frequency. The interstage filter must have a 6dB insertion loss to optimize slope linearity.

Pins 1, 16, 15, 14, 12, 11, 10, 9, and 8 do not need external bias and should not have a DC path.

TYPICAL APPLICATION



Double Balanced Mixer And Oscillator

Linear Products

DESCRIPTION

The NE612 is a low-power VHF monolithic double balanced mixer with on-board oscillator and voltage regulator. It is intended for low cost, low power communication systems with signal frequencies to 500MHz and local oscillator frequencies as high as 200MHz. The mixer is a "Gilbert cell" multiplier configuration which provides gain of 14dB or more at 49MHz.

The oscillator can be configured for a crystal, a tuned tank operation, or as a buffer for an external L.O. Noise figure at 49MHz is typically below 6dB and makes the device well suited for high performance cordless telephone. The low power consumption makes the NE612 excellent for battery operated equipment. Networking and other communications products can benefit from very low radiated energy levels within systems. The NE612 is available in an 8- lead dual-in-line plastic package and an 8-lead SO (surface mounted miniature package).

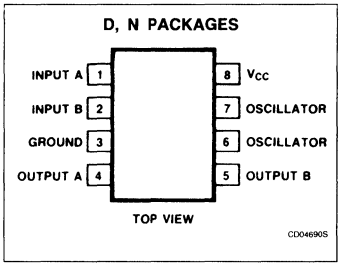
FEATURES

- **Low current consumption**
- **Low cost**
- **Operation to 500MHz**
- **Low radiated energy**
- **Low external parts count; suitable for crystal/ceramic filter**
- **Excellent sensitivity, gain, and noise figure**

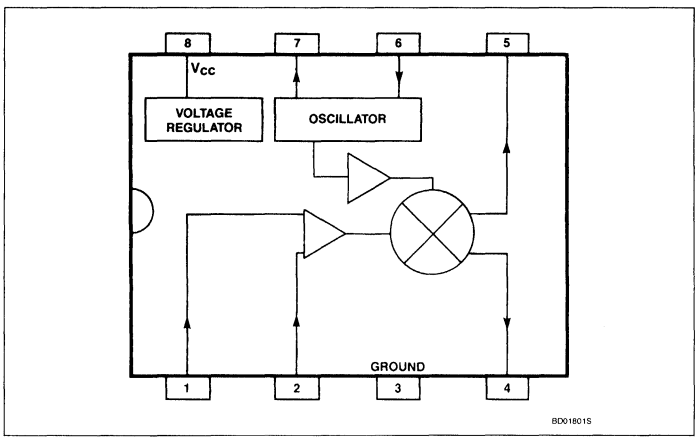
APPLICATIONS

- **Cordless telephone**
- **Portable radio**
- **VHF transceivers**
- **RF data links**
- **Sonabuoys**
- **Communications receivers**
- **Broadband LAN's**
- **HF and VHF frequency conversion**

PIN CONFIGURATION



BLOCK DIAGRAM



ORDERING CODE

DESCRIPTION	ORDER CODE
Dual-in-line, plastic; 0 to +70°C	NE612N
Dual-in-line, small outline; 0 to +70°C	NE612D

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Maximum operating voltage	9	V
Storage temperature	−65 to +150	°C
Operating temperature	0 to +70	°C

AC/DC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_{CC} = 6V$, Figure 1

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Power supply voltage range		4.5		8.0	V
DC current drain			2.4	2.8	mA
Input signal frequency			500		MHz
Oscillator frequency			200		MHz
Noise figured at 49MHz			5.0		dB
Third order intercept point at 49MHz	$RF_{IN} = -45dBm$		−15		dBm
Conversion gain at 49MHz		14			dB
RF input resistance		1.5			kΩ
RF input capacitance			3		pF
Mixer output resistance	(Pin 4 or 5)		1.5		kΩ

TEST CONFIGURATION

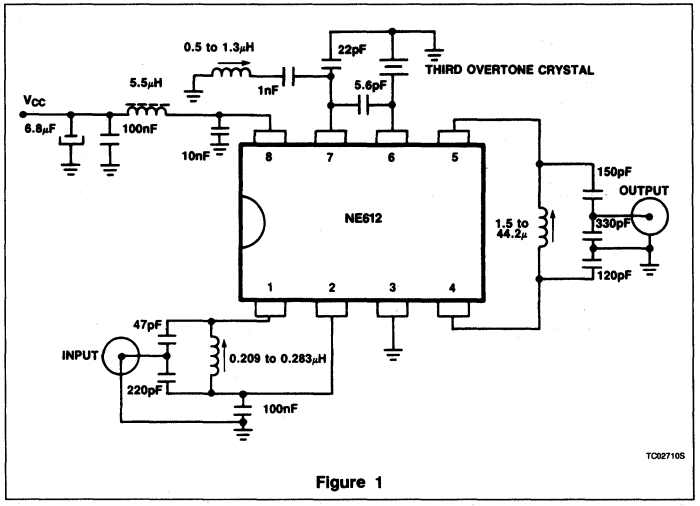


Figure 1

DESCRIPTION OF OPERATION

The NE612 is a Gilbert cell, an oscillator/buffer, and a temperature compensated bias network as shown in the equivalent circuit. The Gilbert cell is a differential amplifier (Pins 1 and 2) which drives a balanced switching cell. The differential input stage provides gain and determines the noise figure and signal handling performance of the system.

The NE612 is designed for optimum low power performance. When used with the NE614 as a 49MHz cordless telephone system, the NE612 is capable of receiving −119dBm signals with a 12dB S/N ratio. Third order intercept is typically −15dBm (that's approximately +5dBm output intercept because of the RF gain). The system designer must be cognizant of this large signal limitation. When designing LAN's or other closed systems where transmission levels are high, and small signal or signal-to-noise issues not critical, the input to the NE612 should be appropriately scaled.

Besides excellent low power performance well into VHF, the SA612 is designed to be flexible. The input, output, and oscillator ports can support a variety of configurations provided the designer understands certain constraints, which will be explained here.

The RF inputs (Pins 1 and 2) are biased internally. They are symmetrical. The equivalent AC input impedance is approximately 1.5K || 3pF through 50MHz. Pins 1 and 2 can be used interchangeably, but they should not be DC biased externally. Figure 3 shows three typical input configurations.

The mixer outputs (Pins 4 and 5) are also internally biased. Each output is connected to the internal positive supply by a 1.5kΩ resistor. This permits direct output termination yet allows for balanced output as well. Figure 4 shows three single-ended output configurations and a balanced output.

The oscillator is capable of sustaining oscillation beyond 200MHz in crystal or tuned tank configurations. The upper limit of operation is determined by tank "Q" and required drive levels. The higher the Q of the tank or the smaller the required drive, the higher the permissible oscillation frequency. If the required L.O. is beyond oscillation limits, or the system calls for an external L.O., the external signal can be injected at Pin 6 through a DC blocking capacitor. External L.O. should be 200mVpp minimum to 300mVpp maximum.

Figure 5 shows several proven oscillator circuits. Figure 5A is appropriate for cordless telephone. In this circuit a third overtone parallel mode crystal with approximately 5pF load capacitance should be specified. Capacitor C3 and inductor L1 act as a fundamental trap. In fundamental mode oscillation the trap is omitted.

Figure 6 shows a Colpitts varacter tuned tank oscillator suitable for synthesizer controlled applications. It is important to buffer the output of this circuit to assure that switching spikes from the first counter or prescaler do not end up in the oscillator spectrum. The dual-gate MOSFET provides optimum isolation with low current. The FET offers good isolation, simplicity, and low current, while the bipolar circuits provide the simple solution for non-critical applications. The resistive divider in the emitter follower circuit should be chosen to provide the minimum input signal which will assume correct system operation.

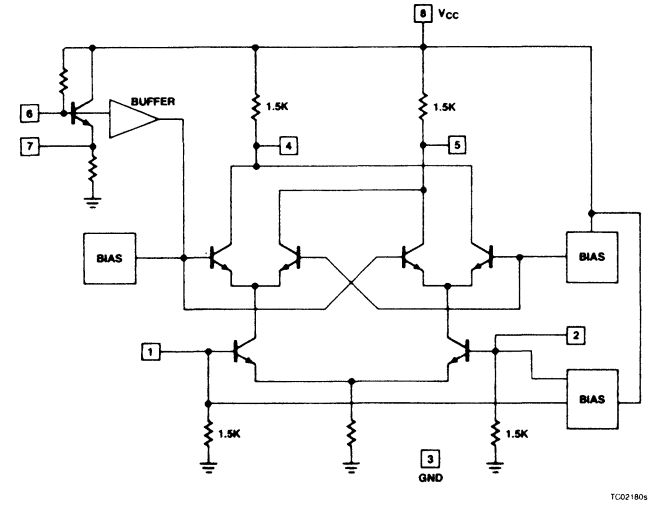
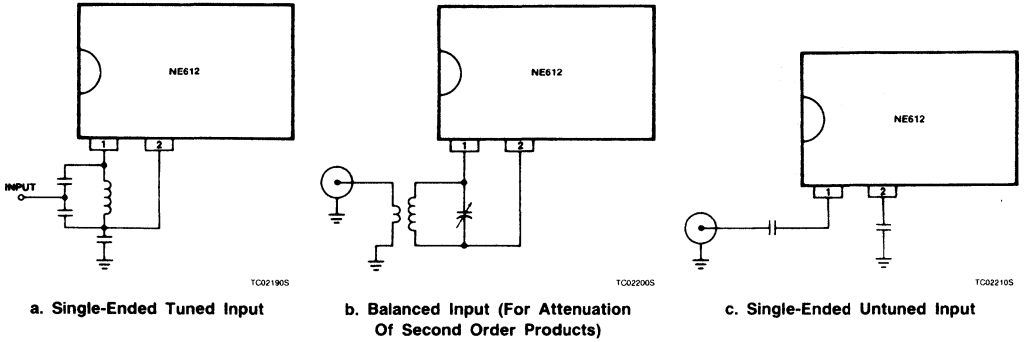


Figure 2. Equivalent Circuit

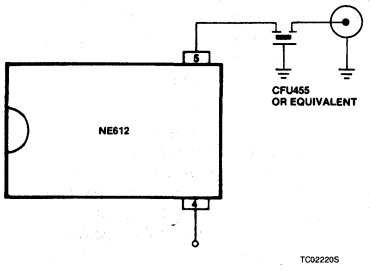


a. Single-Ended Tuned Input

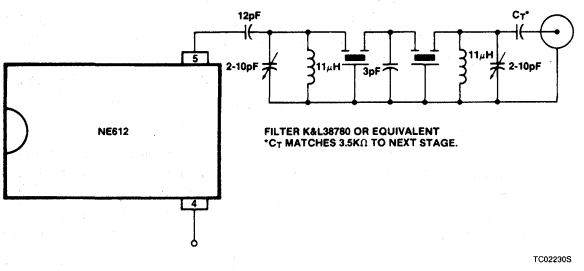
b. Balanced Input (For Attenuation Of Second Order Products)

c. Single-Ended Untuned Input

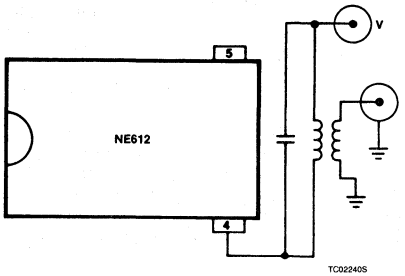
Figure 3. Input Configuration



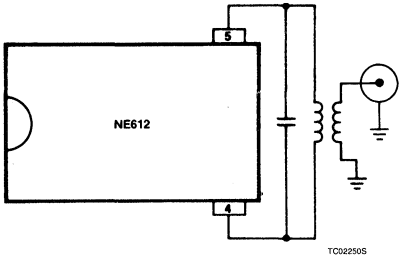
a. Single-Ended Ceramic Filter



b. Single-Ended Crystal Filter

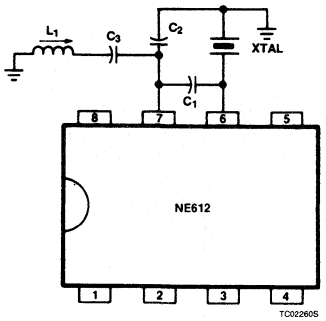


c. Single-Ended IFT

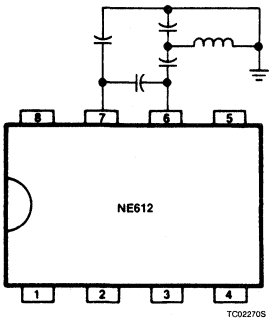


d. Balanced Output

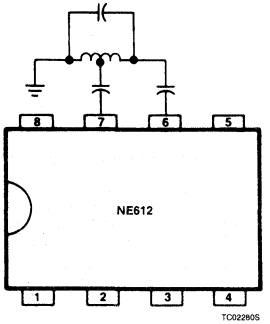
Figure 4. Output Configuration



a. Colpitts Crystal Oscillator (Overtone Mode)



b. Colpitts L/C Tank Oscillator



c. Hartley L/C Tank Oscillator

Figure 5. Oscillator Circuits

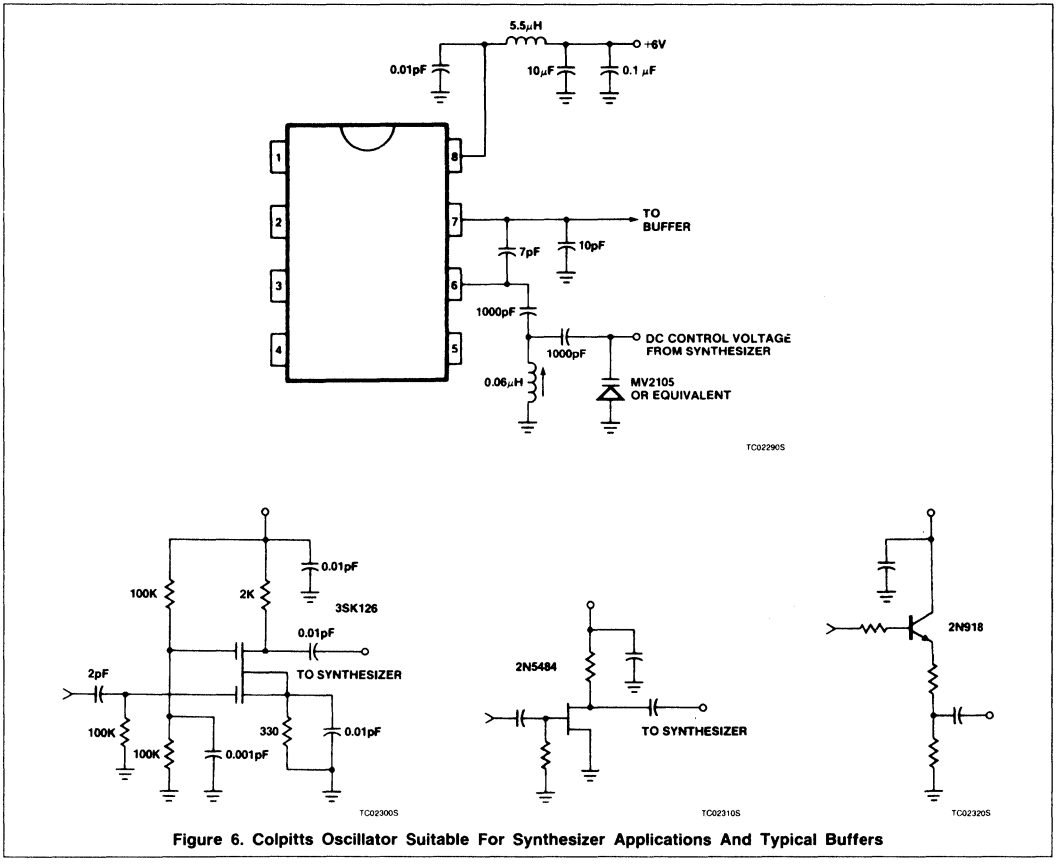


Figure 6. Colpitts Oscillator Suitable For Synthesizer Applications And Typical Buffers

TEST CONFIGURATION

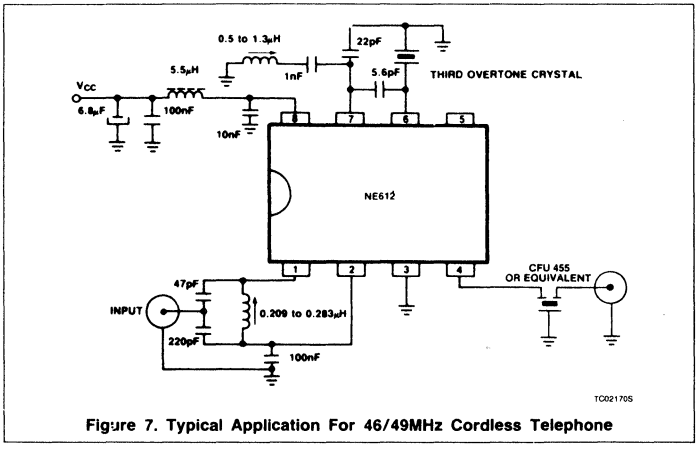


Figure 7. Typical Application For 46/49MHz Cordless Telephone

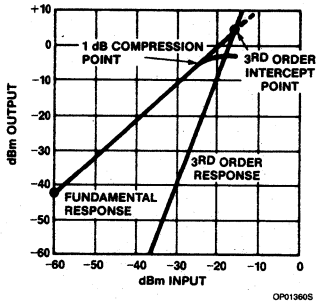


Figure 8. SA/NE612 Third Order Intermod And 1dB Compression Point Performance

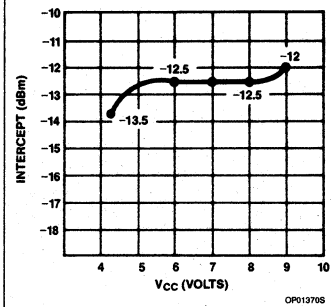


Figure 9. Input Third Order Intercept Point vs V_{CC}

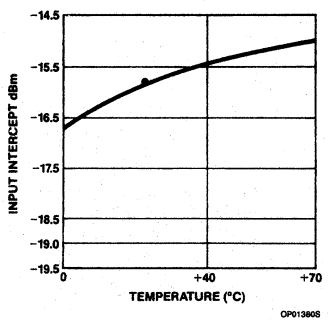


Figure 10. Third Order Intercept Point vs Temperature

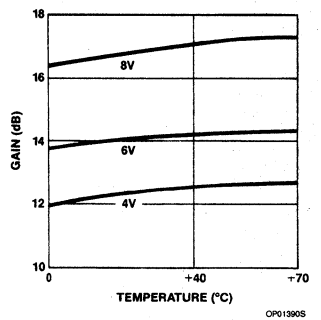


Figure 11

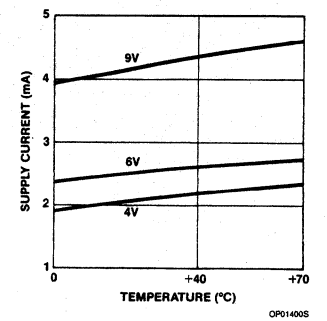


Figure 12

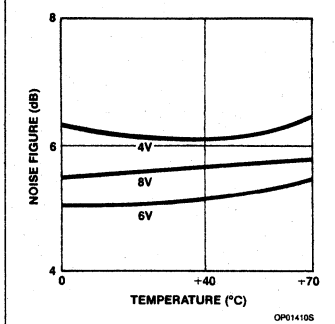


Figure 13

Low Power FM IF System

Linear Products

DESCRIPTION

The NE614 is a monolithic low-power FM IF system incorporating two limiting intermediate frequency amplifiers, quadrature detector, muting, logarithmic signal strength indicator, and voltage regulator. The NE614 is available in a 16-lead dual-in-line plastic package and 16-lead SO (surface-mounted miniature package).

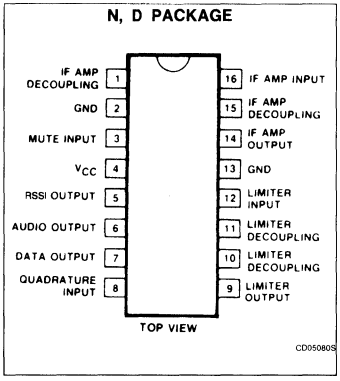
FEATURES

- **Low-power consumption**
- **Logarithmic signal strength indicator**
- **Separate data output**
- **Audio output with muting**
- **Low external count; suitable for crystal/ceramic filters**
- **Excellent sensitivity**

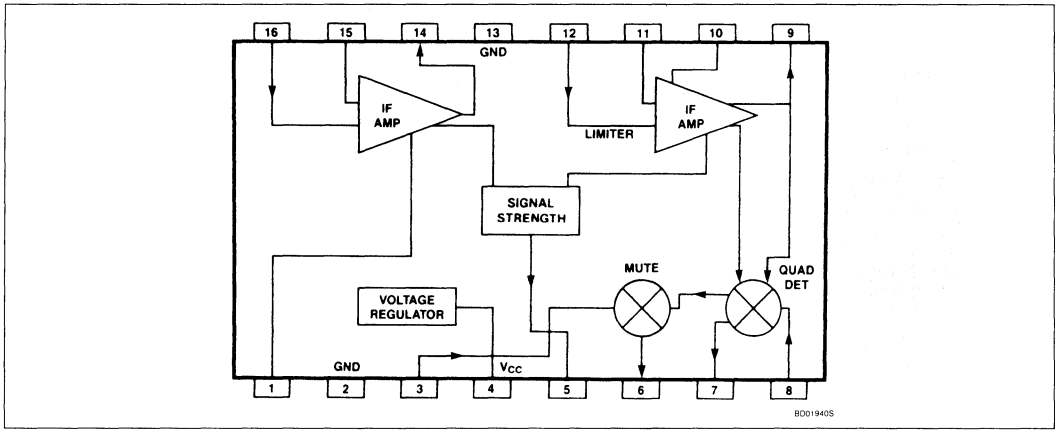
APPLICATIONS

- **Cellular Radio FM IF**
- **Communications receivers**
- **Intermediate frequency amplification and detection up to 15MHz**
- **RF level meter**
- **Spectrum analyzer**
- **Instrumentation**
- **Cordless telephone**
- **Remote control**

PIN CONFIGURATION



BLOCK DIAGRAM



ORDERING CODE

DESCRIPTION	ORDER CODE
Plastic; 0 to +70°C	NE614N
Plastic; SO (surface-mounted miniature package); 0 to +70°C	NE614D

ABSOLUTE MAXIMUM RATINGS

SYMBOL AND PARAMETER	RATING	UNIT
Maximum operating voltage	9	V
Storage temperature	−65 to +150	°C
Operating temperature NE614	0 to +70	°C

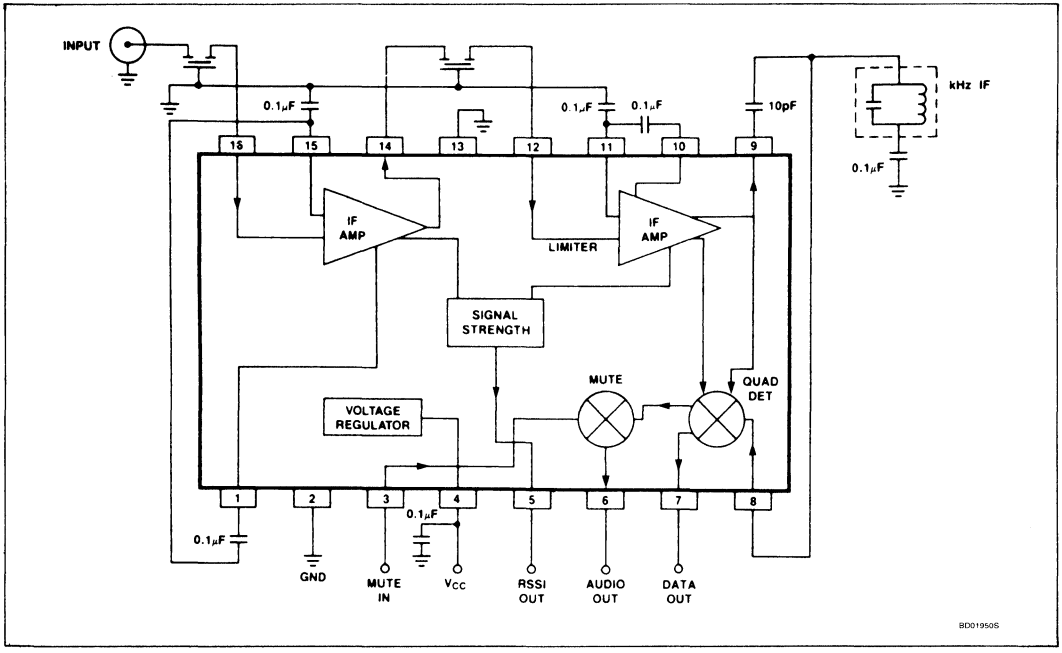
DC ELECTRICAL CHARACTERISTICS $T_A = 25°C$; $V_{CC} = +6V$ unless otherwise stated.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power supply voltage range		4.5		8.0	V
DC current drain				3.0	mA
Mute switch input threshold (on) (off)		1.7		 1.0	V V

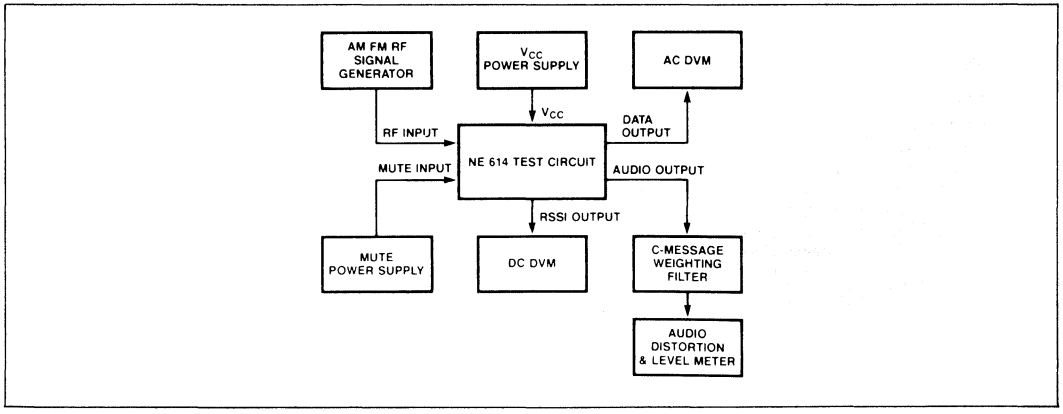
AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$; $V_{CC} = +6V$ unless otherwise stated. RF frequency = 455kHz; RF level = −47dBm; FM modulation = 1kHz with +8kHz peak deviation. Audio output with C-message weighted filter and de-emphasis capacitor.

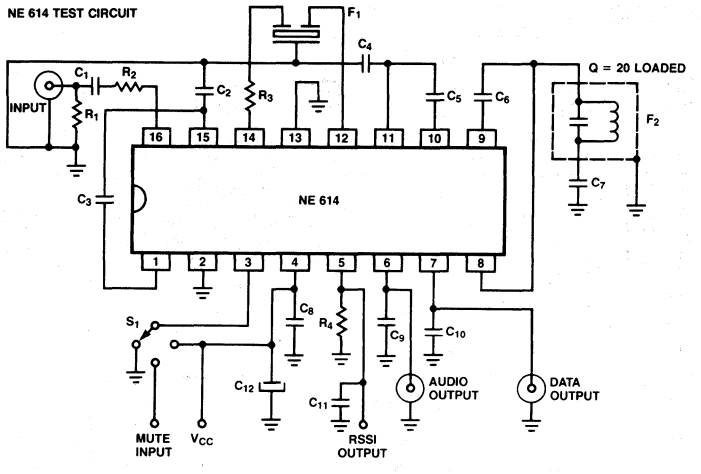
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input limiting − 3dB	Test at pin 16		−90	−80	dBm
AM rejection	80% AM 1kHz	30			dB
Recovered audio level	After C filter and de-emphasis capacitor	80	100		mV_{rms}
Recovered data level		250	350		mV_{rms}
SINAD sensitivity	RF level − 97dBm	8	12		dB
THD		−35			dB
Signal-to-noise ratio	No modulation		75		dB
IF input impedance		1.5			kΩ
IF output impedance		1.0			kΩ
Limiter input impedance		1.5			kΩ
Quadrature detector data output impedance		50			kΩ
Muted audio output impedance			50		kΩ

TYPICAL APPLICATION



TEST SET-UP





C1 10nF +80 – 20% 63V K10000-Z5V Ceramic
C2 100nF ± 10% 50V Polyester
C3 100nF ± 10% 50V Polyester
C4 100nF ± 10% 50V Polyester
C5 100nF ± 10% 50V Polyester
C6 10pF ± 2% 100V NPO Ceramic
C7 100nF ± 10% 50V Polyester
C8 100nF ± 10% 50V Polyester
C9 15nF ± 10% 50V Polyester
C10 150pF ± 2% 100V N1500 Ceramic
C11 1nF ± 10% 100V K2000-Y5P Ceramic
C12 6.8μF ± 20% 25V Tantalum
F1 455kHz Ceramic Filter Murata SFG455A3
F2 455kHz IF Filter A2549
R1 51Ω ± 1% 1/4W Metal Film
R2 1500Ω ± 1% 1/4W Metal Film
R3 1500Ω ± 5% 1/8W Carbon Composition
R4 100kΩ ± 1% 1/4W Metal Film

Figure 1. NE614 Test Circuit And Parts List

Description of Operation

The NE614 is comprised of five subsystems for IF signal processing. These subsystems, two IF limiting amplifiers, quadrature detector, audio mute, and logarithmic signal strength, can be configured to satisfy many high-performance or low-power systems objectives. Internal temperature compensated bias regulation completes the circuitry.

Figure 2 shows the equivalent circuits of the NE614.

Limiting Amplifiers

The NE614 has two independent limiting IF amplifiers. The first has a typical gain of 30dB. The second typically has 60dB gain. Both have 1.5K nominal input impedance and 15MHz bandwidth. The output impedance of the first limiter is approximately 1kΩ. These impedances permit direct interface with popular ceramic filters such as the SFU455. On the surface, the 1K output of the first limiter would not seem correct. However, approximately 6dB insertion loss is required between limiter stages to optimize the linearity of the signal strength indicator. The impedance mismatch has little effect on passband. Use of an interstage filter reduces wideband noise. A DC blocking capacitor or L/C filter can also be used.

As the signal frequency increases, the 90dB total gain can become a source of instability. Figure 3 shows the limiters as a closed loop system with stray capacitance and the equivalent AC input impedance setting the loop gain.

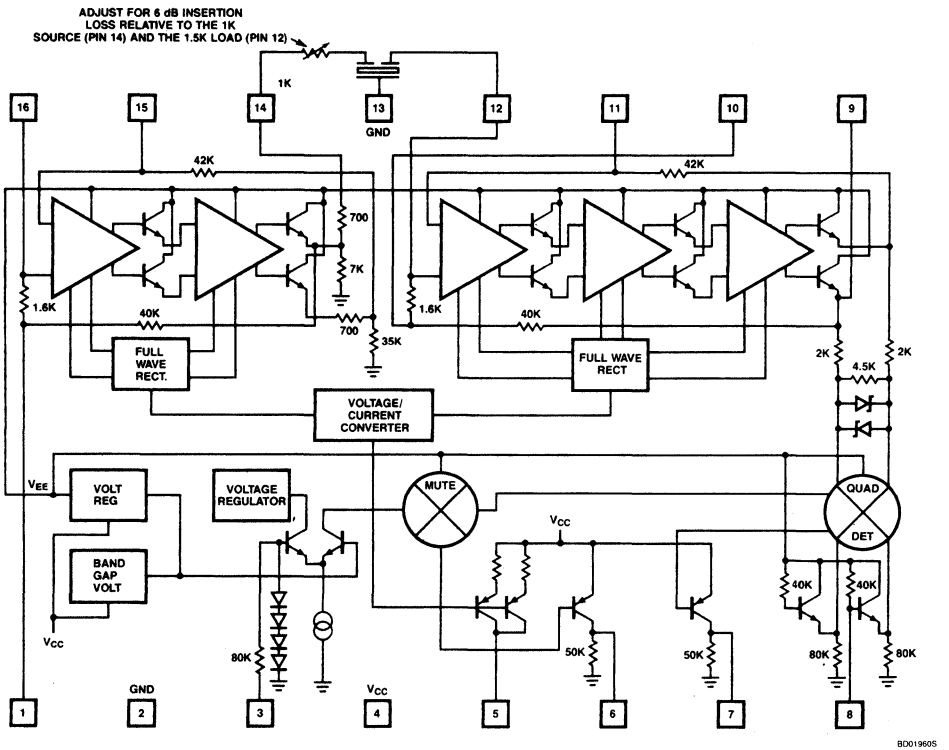


Figure 2. Equivalent Circuit

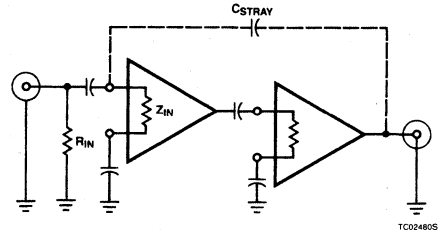
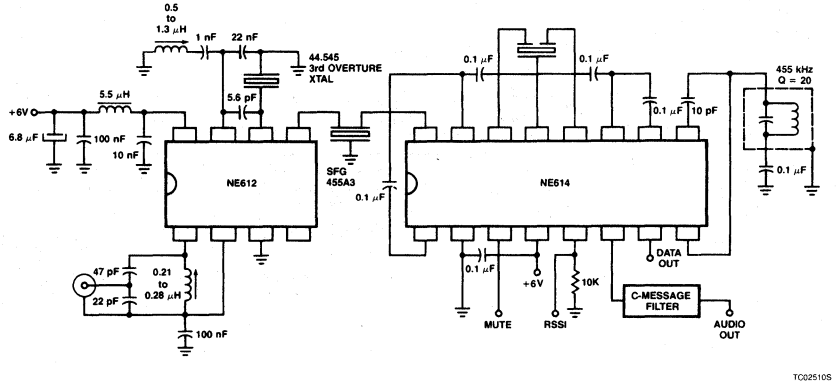


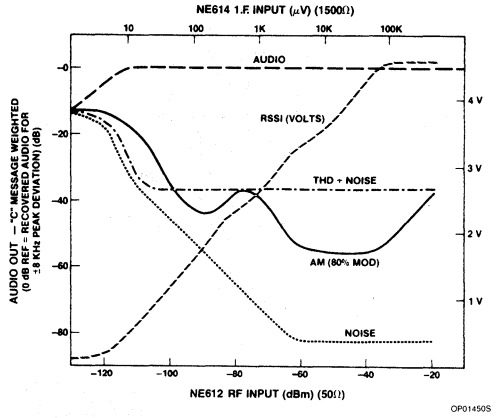
Figure 3. Considerations For Stability

The equivalent AC attenuation factor from the output to the input must be greater than 90dB or oscillation can occur. The input impedance of the device is nominally 1.5K. The stray layout capacitance is a frequency-dependent impedance so that as the frequency of operation or the value of stray capacitance increases, the output-to-input attenuation factor decreases. Keep stray capacitance low by using good RF layout technique. Sockets should be avoided above 455kHz.

Good RF layout is the proper way to avoid instability. However, if system constraints require, stability can be achieved by only using one of the limiting amplifiers, or by adding a resistance, R_{IN}, which will increase the attenuation factor.



a. NE614 Application Circuit



b. Typical Application Circuit Performance

Figure 4

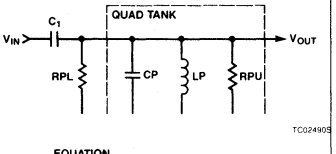
Adding an input resistor is an easy way to reduce the attenuation factor, but may make correct termination of interstage filters difficult or impossible. At 455kHz instability should not be a problem if reasonable RF layout is used. Figure 4a indicates a 455kHz circuit configuration which should serve as a reasonable starting point for many applications. This circuit is configured for 46/49MHz cordless telephone.

Quadrature Detector

The detector of the NE614 is a four quadrant multiplier of the Gilbert cell type. It can be used for frequency or amplitude demodulation. Figure 4b indicates a typical quadrature FM configuration. Fully limited in-phase signal is applied to the multiplier internally. 90° phase shift is accomplished with the L/C tuned circuit connected directly to Pin 8 and capacitively to Pin 9. Because of the DC bias of the NE614, the phase shift network must be returned to ground through a low impedance capacitor. Recovered signal is continuously available at Pin 7 or on a switched basis at Pin 6.

Table 1. System Parameters as Applied to Figure 4A

$\Delta\omega$	=	2π*8kHz
ω_0	=	2π*455kHz
CP	=	180pF
RPU	=	233K
RPL	=	40K
LP	=	644μH
Q	≈	20



EQUATION

$$\frac{V_{OUT}}{V_{IN}} = \frac{j\omega C_1}{\frac{1}{RPL \quad RPU}\left(1 + j2Q\frac{\Delta\omega}{\omega_0}\right) + j\omega C_1}$$

Q = ω_0 (RPL RPU) CP

$\Delta\omega$ = PEAK DEVIATION

ω_0 = CENTER FREQUENCY

TC02500S

Figure 5. General Equations For Quadrature Coil

The quadrature coil or crystal/ceramic discriminator affects three system parameters: Bandwidth, linearity, and detected signal amplitude. Figure 6 shows three quadrature curves.

Curve A has the most narrow bandwidth and high peak-to-peak output versus frequency deviation corresponding to a high Q network. Curve C is very low Q with good linearity and shows how very large deviations can be processed. Curve B shows how the quadrature network can cause non-linearity in the detected output. A typical loaded Q for the 455kHz quadrature coil of Figure 4 is 20. Using the test circuit of Figure 4 with an input of −47dBm, the recovered audio is typically $90mV_{rms}$ with −35dB distortion.

While the NE614 was designed principally for FM applications, the detector can be used for synchronous amplitude demodulation if the carrier is limited through the internal circuitry and AGC'd external to the device. The AGC'd signal is applied to Pin 8 instead of a quadrature signal. The signal strength indicator can control AGC. A low pass filter on the output completes the demodulator. Figure 7 shows the equivalent circuit.

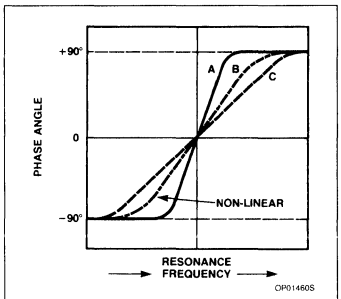


Figure 6. Quadrature

Audio Mute

An electronic switch permits muting or squelch of one of the demodulated outputs. The data (unmuted output) and audio (muted output) both have 50kΩ output impedance and their detected signals are 180 degrees out of phase with each other. The mute input (Pin 3) has a very high impedance and is compatible with three and five volt CMOS and TTL levels. Little or no DC level shift occurs after muting when the quadrature detector is adjusted to the IF center frequency. Muting will attenuate the audio signal by more than 60dB and no voltage spikes will be generated by muting.

Signal Strength Indicator

The logarithmic signal strength indicator is a current source output with maximum source current of 50 microamps. The signal strength indicator's transfer function is approximately 10 microamps per 20dB and is independent of IF frequency. The interstage filter must have a 6dB insertion loss to optimize slope linearity.

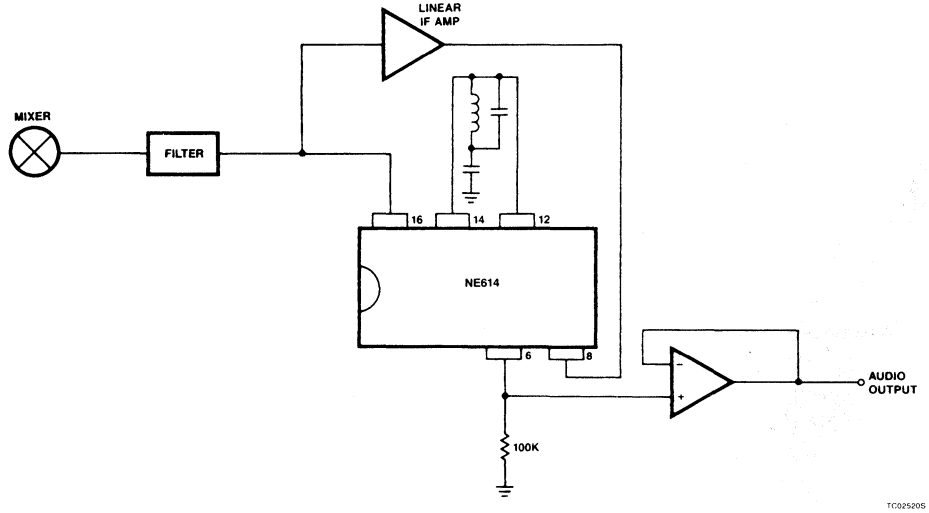


Figure 7. Synchronous AM Detection

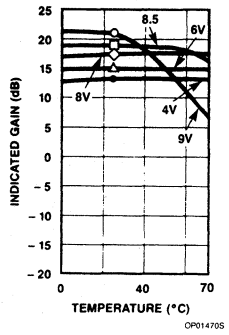


Figure 8. NE614 Indicated Gain vs Temperature and Voltage

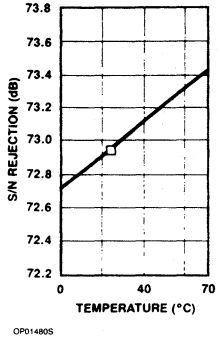


Figure 9. NE614 Signal-To-Noise Ratio vs Temperature

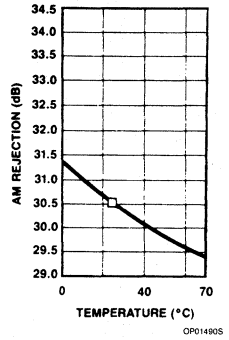


Figure 10. NE614 AM Rejection vs Temperature

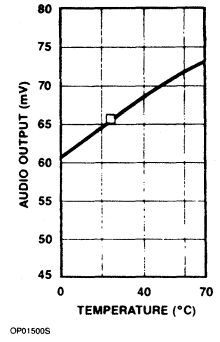


Figure 11. NE614 Audio Output vs Temperature

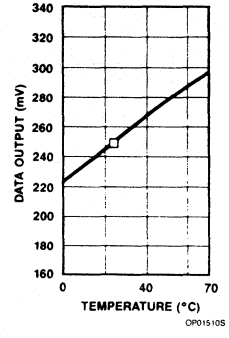


Figure 12. NE614 Data Output vs Temperature

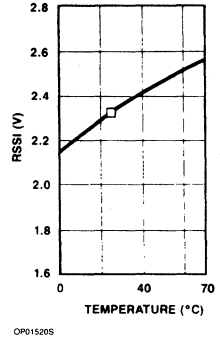


Figure 13. RSSI vs Temperature

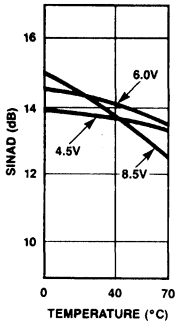


Figure 14. NE614 SINAD vs Temperature and V_{CC}

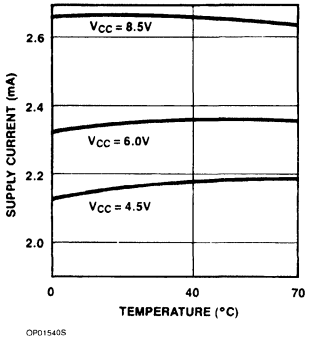


Figure 15. NE614 Supply Current vs Temperature

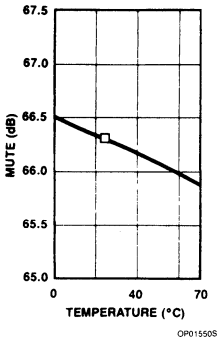


Figure 16. NE614 Muting vs Temperature

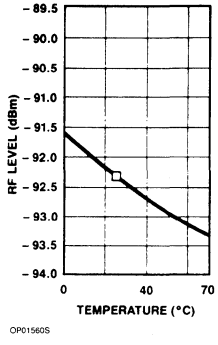


Figure 17. NE614 Limiting RF Level vs Temperature

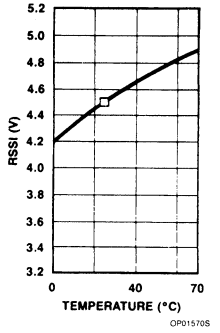


Figure 18. NE614 Large Signal Uncompensated RSSI Voltage vs Temperature

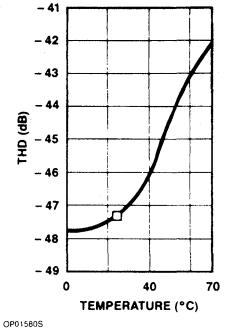


Figure 19. NE614 Total Harmonic Distortion vs Temperature

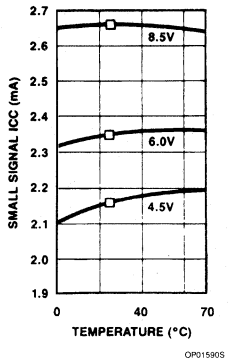


Figure 20. NE614 Supply Current vs Temperature and Voltage

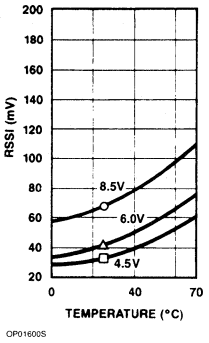


Figure 21. Small Signal RSSI vs Temperature and Voltage

Call Progress Decoder

DESCRIPTION

The NE5900 call progress decoder is a low cost, low power CMOS integrated circuit designed to interface with a microprocessor controlled smart telephone capable of making pre-programmed telephone calls. The call progress decoder provides information to permit microprocessor decisions whether to initiate, continue, or terminate calls. A tri-state, 3-bit output code indicates the presence of dial tone, audible ringback, busy signal, or recorder tones.

A front-end bandpass filter is accomplished with switched capacitors. The bandshaped signal is detected and the cadence is measured prior to output decoding. In addition to the three data bits, a buffered bandpass output and envelope output are available. All logic inputs and outputs can interface with LSTTL, CMOS, and NMOS.

Circuit features include low power consumption and easy application. Few and inexpensive external components are required. A typical application requires a 3.58MHz crystal or clock, 470kΩ resistor, and two bypass capacitors. The NE5900 is effective where traditional call progress tones, PBX tones, and precision call progress tones must be correctly interpreted with a single circuit.

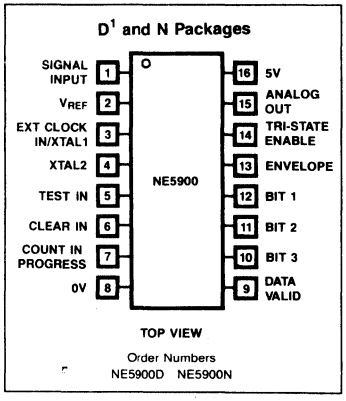
FEATURES

- **Fully decoded tri-state call progress status output**
- **Works with traditional, precision, or PBX call progress tones**
- **Low power consumption**
- **Low cost 3.58MHz crystal or clock**
- **No calibration or adjustment**
- **Interfaces with LSTLL, CMOS, NMOS**
- **Easy application**

APPLICATIONS

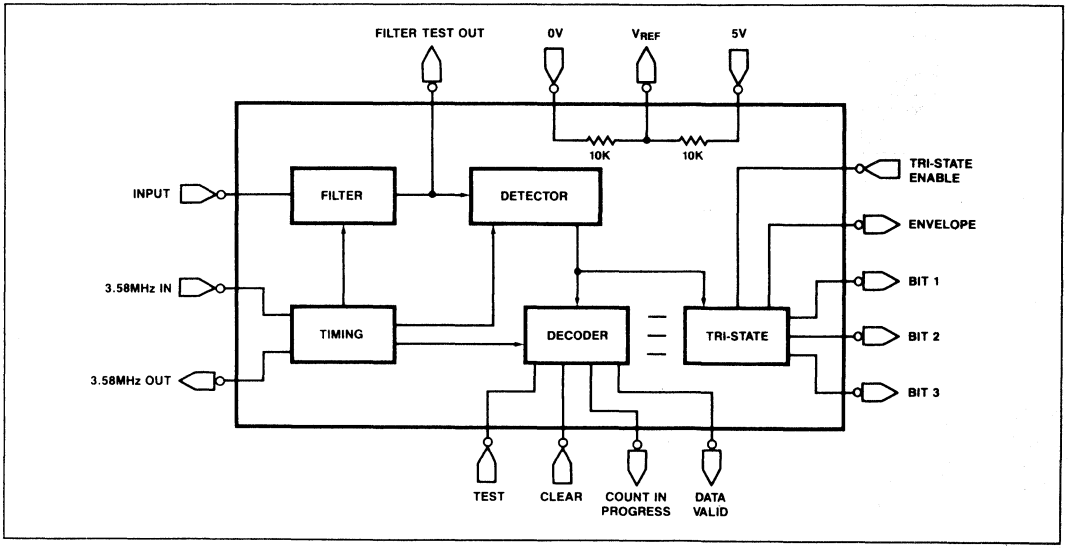
- **Modems**
- **PBXs**
- **Security equipment**
- **Auto dialers**
- **Answering machines**
- **Remote diagnostics**

PIN CONFIGURATION



NOTES:
1. SOL — Released in large SO package only.
2. SOL *and* non-standard pinout.
3. SO *and* non-standard pinout.

BLOCK DIAGRAM CPD



ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNITS
Power Supply Voltage	9	V
Logic Control Input Voltages	−0.3 to +16	V
All Other Input Voltages[1]	−0.3 to V_{CC} + 0.3	V
Output Voltages	−0.3 to V_{CC} + 0.3	V
Storage Temperature	−65 to +150	°C
Operating Temperature	0 to +70	°C
Lead Soldering Temperature (10 sec)	+300	°C
Junction Temperature	+150	°C

NOTE:
1. Includes Pin 3 — Ext Clock In

ELECTRICAL CHARACTERISTICS Unless otherwise stated V_{DD} = 5.0V, f_{OSC} = 3.58MHz 0°C, T_A = 70°C

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			Min	Typ	Max	
	Power supply voltage	Functional	4.5		5.5	V
	Quiescent current	No input, no load			10	mA
	Quiescent current	No input, no load, T_A = 25°C		3	TBD	mA
	Input range[1]	f_{IN} = 300 to 640Hz, ENV output = 1	−40		0	dB
	Signal rejection	All frequencies, ENV output = 0			−50	dB
	Low frequency rejection	Input = 0dB max, ENV output = 0			180	Hz
	High frequency rejection	Input = 0dB max, ENV output = 0	800			Hz
V_{IH}	Logic 1 input voltage	Pins 6, 14	2.0		15	V
V_{IL}	Logic 0 input voltage	Pins 6, 14	0		0.8	V
I_{IH}	Logic 1 input current	V_{IN} = 5.0V Pins 3, 6, 14			1	μADC
I_{IL}	Logic 0 input current	V_{IN} = 0V Pins 3, 6, 14	−1			μADC
V_{IH}	Osc (Pin 3)	EXT clock	V_{DD} − 1		V_{DD}	V
V_{IH}	Osc (Pin 3)	EXT clock	0		1	V
V_{OL}		I_{SINK} = 1.6mA Pins 7, 9, 10, 11, 12, 13			0.4	V
V_{OH}		I_{SOURCE} = 0.5mA Pins 7, 9, 10, 11, 12, 13	4.6			V
I_{OZ}	Tri-State leakage	V_O = V_{DD} or 0V Pins 10, 11, 12, 13			3.0	μA
	Filter output voltage	R_1 = 1MΩ, f_{IN} = 480Hz, 0dB	TBD			V_{pp}
	Pin 1 input impedance[2]	f = 500Hz	1			MΩ
V_{REF}			2.4	2.5	2.6	V
R_{REF}				5		kΩ
t_{PDLH}				TBD		
t_{PDHL}				TBD		

NOTES:
1. 0dB = 0.775V RMS
2. By design — not tested

TRUTH TABLE — DECODED OUTPUT Test and clear inputs low

	BIT 1	BIT 2	BIT 3	DATA VALID	TRI-STATE
Dial Tone	0	0	0	1	1
Ring	1	0	0	1	1
Busy	0	1	0	1	1
Reorder	0	0	1	1	1
Overflow	1	1	1	1	1
Count in Progress	X	X	X	X	X
Outputs Disabled	High Z	High Z	High Z	X	0

DESCRIPTION OF OPERATION

The NE5900 call progress decoder was designed to accommodate the various call progress tone systems which are presently in use in the U.S. and many other parts of the world. To identify dial tone, ringback, busy signals, or reorder tones, the NE5900 uses a cadence counting technique. This eliminates the problem of identifying the specific tones by their individual frequencies, which are not standard from system to system.

Figure 1 shows some of the call progress tones which can be encountered when calling from phone system to system within the U.S.

Note that although the frequencies are not standardized, the cadence or interruption rate does not vary. Even the three types of reorder tones share the same period of 0.5 sec.

Figure 2 shows a profile of the tone energy described in Figure 1. Note the double ring (audible ringback) which can be encountered with PBXs.

TONE	FREQUENCY (Hz)	CADENCE
PRECISION DIAL TONE	350 + 440	CONTINUOUS
OLD DIAL TONES	600 + 120 OR 133, AND OTHER COMBINATIONS	CONTINUOUS
PRECISION BUSY	480 + 620	0.5 SEC ON 0.5 SEC OFF
OLD BUSY	600 + 120	0.5 SEC ON 0.5 SEC OFF
PRECISION REORDER	480 + 620	0.3 SEC ON LOCAL 0.2 SEC OFF REORDER
OLD REORDER	600 + 120	0.2 SEC ON TOLL 0.3 SEC OFF REORDER 0.25 SEC ON TOLL 0.25 SEC OFF LOCAL
PRECISION AUDIBLE RINGBACK	440 + 480	2 SEC ON 4 SEC OFF
OLD AUDIBLE RINGBACK	420 + 40 AND OTHER COMBINATIONS	2 SEC ON 4 SEC OFF

Figure 1. Call Progress Tones

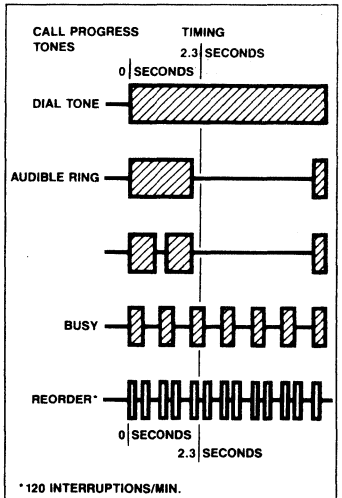


Figure 2. Energy Profile of Call Progress Timing

The NE5900 uses the signal in the call progress tone passband and the cadence or interrupt rate of the signal to determine which call progress tone is present.

Figure 3 shows a detailed block diagram of the NE5900.

The signal input from the phone line is coupled through a 470kΩ resistor which, together with two internal capacitors and an internal resistor, form an anti-aliasing filter. The 470kΩ resistor also provides protection from line transients.

Following this is a switched capacitor bandpass filter which accepts call progress tones and inhibits tones not in the call progress band of 300Hz to 640Hz. The bandpass limits are determined by the input clock frequency of 3.58MHz. An on-board inverter between pins 3 and 4 can be used either as a parallel mode crystal oscillator or as a buffer for an external 3.58MHz clock signal. The switched capacitor filters provide typical rejection of greater than 40dB for frequencies below 120Hz and above 1.6kHz.

The decoder responds to signals between 300Hz and 640Hz over an amplitude range of 0dB to −40dB (0dB = 0.775VRMS). The decoder will not respond to any signals below −50dB or to tones up to 0dB which are below 180Hz or above 800Hz. Dropouts of 20msec or bursts of only 20msec duration are ignored. A gap of 40msec or a valid tone of 40msec is detected.

The buffered output of the switched capacitor filter is available at the analog output, pin 15. A logic output representing the detected envelope of this signal is available at the envelope output, pin 13.

At the start of an in-band tone (envelope output goes high), a 2.3-second interval is timed out. Transitions of the envelope during this interval are counted to determine the signal present. At 2.3 seconds, the three bits of data representing this decision are stored in the latch and appear at the outputs. A data valid signal goes high at this time, signaling that the data bits, pins 10–12, can be read.

The output code is as follows:

	PIN 12	PIN 11	PIN 10
DIAL TONE	0	0	0
RINGING SIGNAL	1	0	0
BUSY SIGNAL	0	1	0
REORDER TONE	0	0	1
OVERFLOW	1	1	1

The overflow condition occurs in the event that too many transitions occur during the 2.3-second interval. This can result from noise, voice, or other line disturbances not normally present during the post-dialing interval.

The clear input resets all internal registers and the output latch, and is to be set low after the completion of dialing. The test pin is for production test only and must be kept low in all user applications.

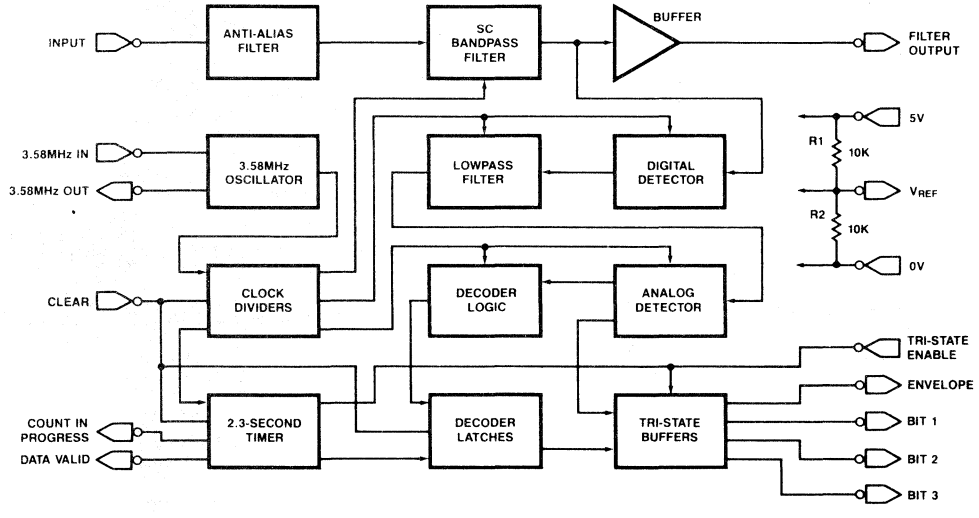


Figure 3. Detailed Block Diagram CPD

Figure 4 shows a typical application of the call progress decoder.

In this application only one external component is needed and no microprocessor activity other than clear is required.

Figure 5 shows the recommended direct interface to the telephone line. Bus connection is possible by utilizing tri-state, and internal timing is accomplished with a 3.58MHz crystal.

The designer can utilize the input signal, clock, bus, or microprocessor interface which best serves the application. Figure 6 gives a typical timing diagram for the application of Figures 4 and 5.

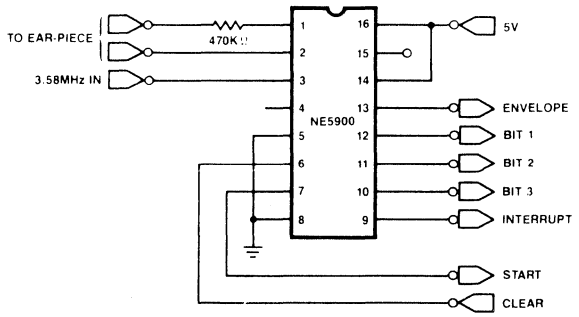


Figure 4. Typical Application

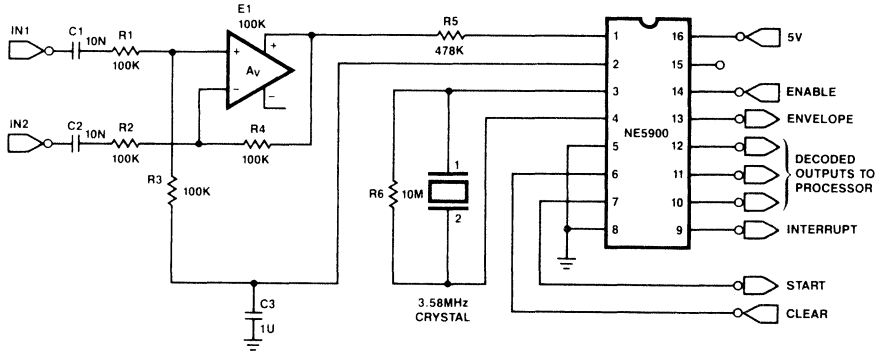


Figure 5. Typical Two-Wire Application

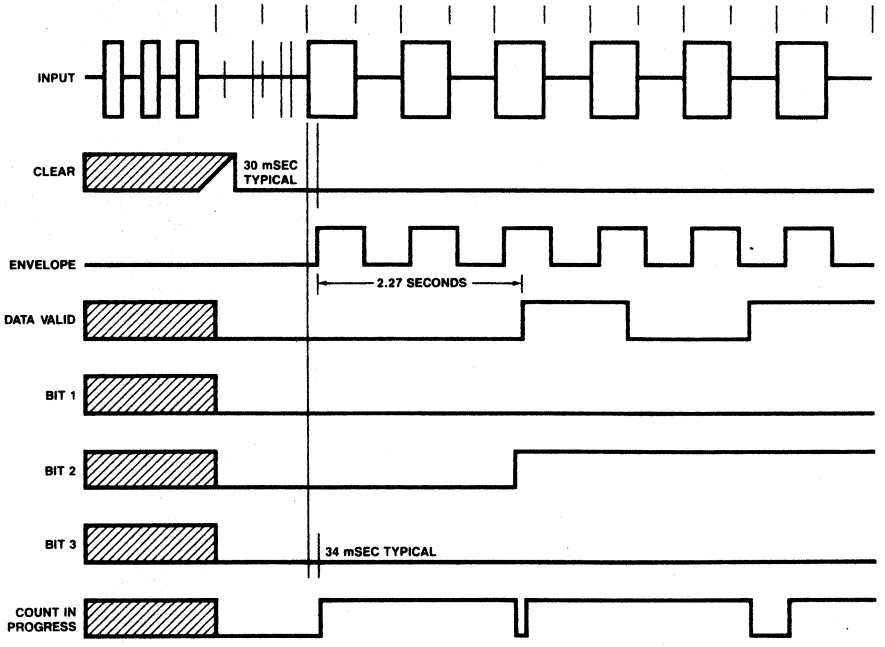

INPUT
CLEAR
30 mSEC
TYPICAL
ENVELOPE
2.27 SECONDS
DATA VALID
BIT 1
BIT 2
BIT 3
34 mSEC TYPICAL
COUNT IN
PROGRESS

Figure 6

LOW COST SPEECH DEMONSTRATION BOARD

GENERAL DESCRIPTION

The low cost speech demonstration board is designed to add voice output to existing card based electronic equipment with the minimum of additional effort and components. The majority of components used are of the CMOS type with low power consumption making the board suitable for battery operation.

Applications include speech evaluation and speech demonstration.

FEATURES

- PCF8200 speech synthesizer
  - Male and female speech of very high quality
  - CMOS technology
  - Extended operating temperature range
  - Programmable speaking speed
- Low current consumption
  - All major components use CMOS technology (PCF8200, 80C39 and 27C64)
- Very large vocabulary up to 12 minutes
  - 4 EPROM sockets
  - EPROM selection for 27C16 to 27C256
  - Low data rates for synthesizer (average 1500 bits per second)
- Easy interfacing
  - 8-bit parallel data bus/key switch input
  - Volume control, speaker connection
  - Control signals (e.g. RESET, BUSY etc etc)
- Simple operating modes
  - ROM selection
  - Word sequence within a ROM
  - Repeat last utterence
  - Control software is readily customizeable
  - To implement parameter download from external source
- Single Eurocard size PC board
- Single + 5 V supply
- Low cost

APPLICATIONS

- OEM design-in
- May be simply used with many card systems for speech evaluation
- Speech demonstration
  - Particularly simple when used with the OM8201 (Speech Demonstration Box)

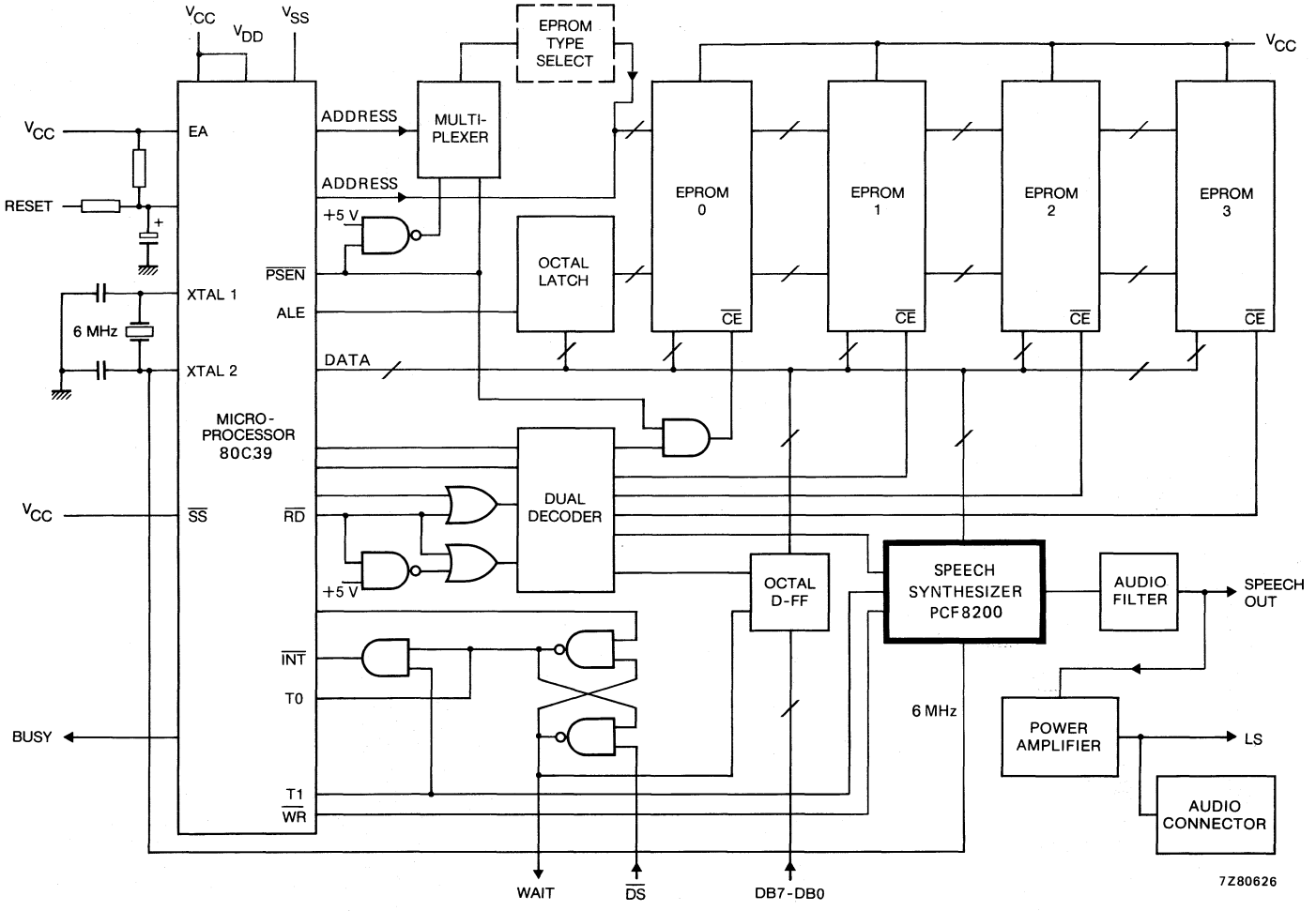


Fig. 1 Block diagram.

OPERATION

HARDWARE DESCRIPTION

The main controlling microprocessor is an 80C39 running at 6 MHz. This device supplies all of the main controlling signals for the board operation and the interfacing to any external system.
Four sockets are provided for EPROMS which contain speech coding. These may be 27C16 types, through to 27C256 types; the sockets will be a low insertion force type to allow for easy customizing.
The board will be supplied with one socket occupied by a 27C64 which will contain the control program and some speech examples. All four EPROM sockets must contain the same EPROM type.

The speech synthesizer PCF8200 converts the coding into a speech output. This synthesizer has been designed to simulate the human vocal tract using five formants for male and four formants for female speech. Periodic updating of the parameters for these formants can produce very high quality speech.

The output of the synthesizer can be fed into an audio amplifier, TDA7050, via a resistor-capacitor filter network which provides a frequency cut-off above 5 kHz of about 25 dB. The configuration of the audio amplifier used on this board gives an output of 140 mW peak power into a 25 Ω speaker from a 5 V supply.

Connections are made to the board via a standard DIN/IEC connector. This allows access to the 8-bit parallel data bus so that speech coding from an external source may be used, if implemented, and allows the selection of speech phrases by an external system, such as a microcomputer or even a bank of switches. The same connector also permits the addition of a volume control, loudspeaker, a high impedance audio output, and power supply. The control signals RESET, BUSY, WAIT and DS are also taken to the outside of the board. There is also a loudspeaker plug on the board.

All components are contained on a standard single Eurocard, and therefore suitable for rack mounted equipment.

SOFTWARE DESCRIPTION

All the software required to operate the board is contained in the only EPROM supplied. The software is written in modular from so that it is possible for a customer to alter or add to any particular function which suits his applications. An industrial standard microprocessor was chosen so that readily available development systems could be used to facilitate this modification.

There are four main modes of operation:

- ROM Selection
- Word Sequence
- Repeat Word
- Speaking Speed Selection

These modes are all controlled by software.

ROM Selection mode permits access to an individual EPROM and pronounces the first utterence from that EPROM.

Word Sequence gives the next word (activated by repeated access to the same EPROM) and if continually exercised will keep looping on the words in that EPROM.

The Repeat Word command allows indefinate repetition of the last utterance pronounced.

The Speaking Speed Selection allows the utterence to be pronounced at a different speed.

The software also controls the address sequencing within the utterance and ensures that the required data is supplied to the synthesizer.

There are also some examples of words/utterences encoded in the remainder of the supplied EPROM. These words are intended for demonstration purposes and will show the features of the synthesizer when selected. The main features being illustrated are:

- Male speech in several languages
- Female speech in several languages
- Programmable speaking speed

ORDERING INFORMATION

Product name: Low Cost Speech Demonstration Board

Type number: OM8200

Ordering code: 9337 541 30000

Orders should be placed with your local Philips/Signetics agency.

SPEECH ANALYSIS/EDITING SYSTEM

GENERAL DESCRIPTION

The OM8210 is a speech analysing/editing system, and comprises of a speech adapter box and associated software. The system uses either the HP9816S or IBM-PC personal computer.
The OM8210 and the computer function together to produce speech coding for the PCF8200.
The system has many commands available, mostly single key operations, which gives it flexability.

FEATURES

- Input sampling of analogue speech signals
- Speech analysis
- Graphic parameter representation
- Parameter editing screen
- Conversion of parameters to PCF8200 synthesizer
- EPROM programming
- Parameter storage on floppy disc
- Speech output via PCF8200 voice synthesizer

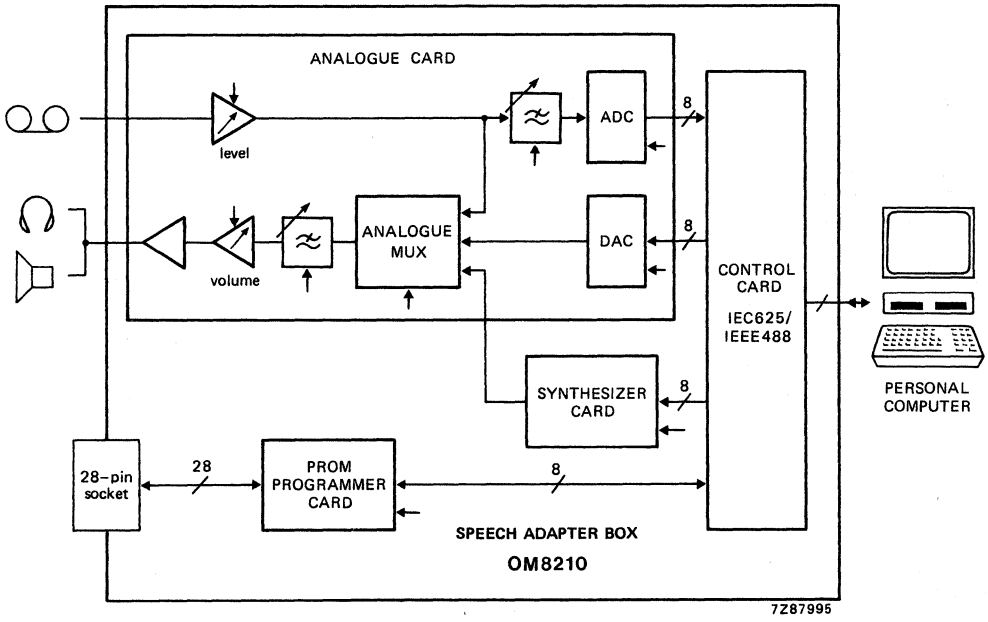


Fig. 1 Block diagram.

HARDWARE DESCRIPTION

The hardware for the OM8210 is contained in an attractive box with access to all the interconnections (IEC 625, interface loudspeaker, headphones, tape input, and EPROM socket), from the front panel. There are four single Eurocards and a power supply forming the speech adapter box.
These cards are:

- Analogue Card
- Synthesizer Card
- EPROM Card
- Control Card

Analogue Card

On this card, the level of the recorded audio input signal is adjusted by an electronic potentiometer. Before the audio is sampled, frequencies higher than half the sampling frequency are removed by a switched capacitor filter of the type normally used for codecs. A 12-bit analogue-to-digital converter (ADC) produces the digital samples that are sent to the control card. An 8-bit digital-to-analogue converter (DAC) on the analogue card allows the sampled speech to be output. The audio input signal, the sampled speech and the synthesized speech are selected by an analogue multiplexer, filtered, and adjusted for volume before reproduction by a loudspeaker.

The use of integrated electronic potentiometers and codec filters substantially reduces the number of components required while maintaining high performance.

Synthesizer Card

This card accommodates the PCF8200 voice synthesizer and a small amount of peripheral components and a socket for the MEA8000 voice synthesizer.

EPROM Programmer Card

This card allows four different types of EPROM (2716, 2732, 2732A and 2764) to be programmed under software control. All the hardware to generate the programming voltages and the programming waveforms are on this card.

Control Card

This card performs three functions:

- IEC 625/IEEE 488 interface
- Control sequencer
- Clock generator

The IEC/IEEE interface is a simple talker/listener implementation with a HEF4738 circuit.

An FPLA control sequencer provides the handshake signals for IEC/IEEE interface and the chip enable signals for the rest of the system (the ADC, the DAC, the synthesizer and control circuits).

The filter sampling frequency is generated with a software programmable PLL frequency synthesizer. The speech sampling frequency is derived from the filter sampling frequency by frequency division. Hence, the filter frequency cut-off and the sample rate of the ADC and the DAC are automatically linked.

The hardware includes all the necessary cables, adapter plug, loudspeaker, headphone and power supply.

SOFTWARE DESCRIPTION

The software for this speech coding system has been developed and arranged for optimum user convenience. There are eight modes available.

Each mode and each command in the mode is selected by single key entries. Commands that can destroy data have to be confirmed before they are executed. More than 100 commands are available. The modes are:

Sample Mode	Samples and digitizes the recorded speech, the amplitude can be checked and speech segments selected. The sampled speech is stored in a memory and can be displayed or made audible.
Analysis Mode	Generates speech parameters from samples. The analysis selects the voiced/unvoiced sections, extracts the formants (5 for male and 4 for female), amplitude, and the pitch, and quantisizes the speech parameters.
Parameter Edit Mode	Speech parameters are displayed graphically on the VDU and can be edited to correct errors in the analysis, improve speech quality by altering contours, or amplitudes, concatenate sounds and optimize data rate by editing the frame duration.
Code Mode	Generates PCF8200 code and permits the arrangement of utterences in the optimum order of application. This mode also generates the address map at the head of the EPROM.
EPROM Mode	Used to program/read EPROMS with data for the code memory also possible is a new check, bit check and verification commands.
File Mode	Stores speech parameters or codes on disc, can also assemble code speech segment from an already existing library.
Media Mode	For diskette initialization and making back-up copies.
Option Mode	Allows the system configuration to be read or changed.

The software is supplied on two diskettes, one labelled 'BOOT' which wakes up the system and also contains the system library routines. The other diskette labelled 'SPEECH' contains the speech program, the disc initialization and the file handler programs. The 'BOOT' disc is not required during operation, giving a free disc drive with the system for a diskette to store speech parameter files.

Computer System

The following equipment is required to make a complete Hewlett Packard based editing system:
- HP9816S-630 (optimum computer type) or HP9817
- HP9121D (dual floppy disc)
- Additional memory card for the HP9816S (512 K bytes total required)

The following equipment is required to make a complete IBM based editing system:
- IBM-PC or PC-XT or Philips P3100
- Additional memory (512 K recommended)
- Display graphics card (Hercules monochrome)
- IEEE488 card (Tecmar Rev. D.)

ORDERING INFORMATION

Product name: Speech Analysis/Editing System

Type number: OM8210

Ordering code: 9337 561 50112

The computer system should be purchased from your local agents.
The OM8210 should be ordered through your local Philips/Signetics agent.

SINGLE-CHIP 8-BIT MICROCONTROLLER

DESCRIPTION

The PCB80C51 family of single-chip 8-bit microcontrollers is manufactured in an advanced CMOS process. The family consists of the following members:

- PCB80C31BH: ROM-less version of the PCB80C51BH
- PCB80C51BH: 4 K bytes mask-programmable ROM, 128 bytes RAM

In the following, the generic term "PCB80C51BH" is used to refer to both family members.

The device provides hardware features, architectural enhancements and new instructions to function as a controller for applications requiring up to 64 K bytes of program memory and/or up to 64 K bytes of data storage.

The PCB80C51BH contains a non-volatile 4 K x 8 read-only program memory (not ROM-less version); a volatile 128 x 8 read/write data memory; 32 I/O lines; two 16-bit timer/event counters; a five-source, two-priority-level, nested interrupt structure; a serial I/O port for either multi-processor communications, I/O expansion, or full duplex UART; and on-chip oscillator and timing circuits. For systems that require extra capability, the PCB80C51BH can be expanded using standard TTL compatible memories and logic.

The PCB80C31BH/80C51BH has two software selectable modes of reduced activity for further power reduction — Idle and Power Down.
The Idle modes freezes the CPU while allowing the RAM, timers, serial port and interrupt system to continue functioning.
The Power Down mode saves the RAM contents but freezes the oscillator causing all other chip functions to be inoperative.

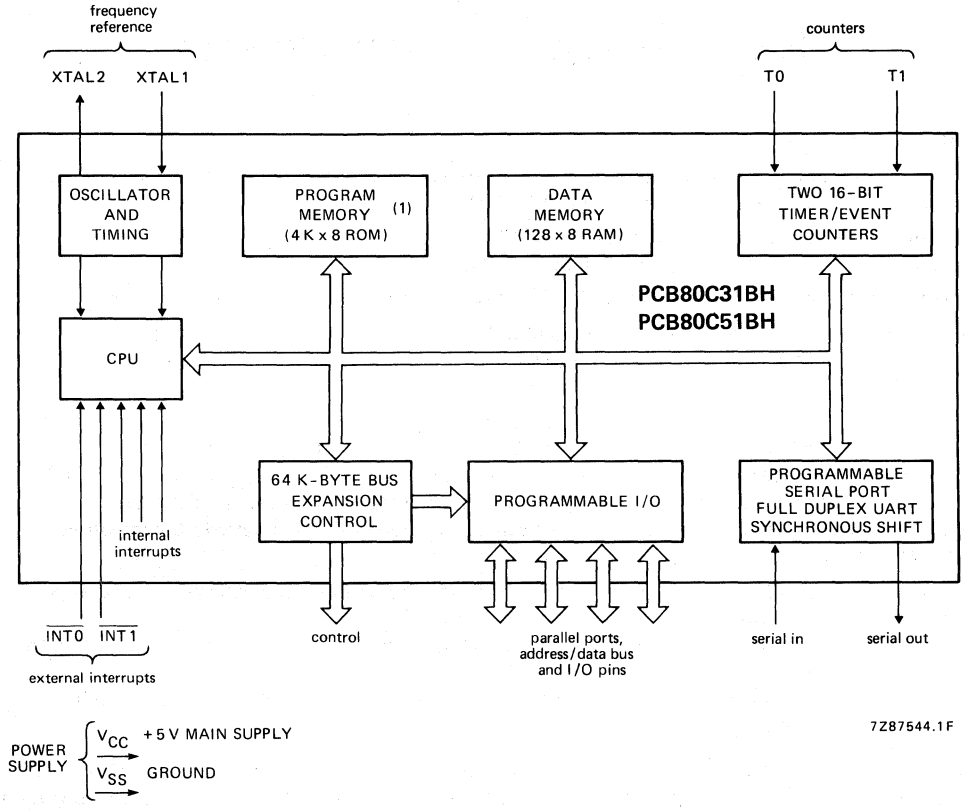
The device also functions as an arithmetic processor having facilities for both binary and BCD arithmetic plus bit-handling capabilities. The instruction set consists of 255 instructions; 44% one-byte, 41% two-byte and 15% three-byte. With a 12 MHz crystal for example, 58% of the instructions are executed in 1 μs and 40% in 2 μs. Multiply and divide instructions require 4 μs. Multiply, divide, subtract and compare are among the many instructions added to the standard PCB80C48 instruction set.
Software development to be announced: PCB85C51 in piggy-back.

Features

- 4 K x 8 ROM (80C51BH only), 128 x 8 RAM
- Four 8-bit ports, 32 I/O lines
- Two 16-bit timer/event counters
- Full-duplex serial port
- External memory expandable to 128 K, external ROM up to 64 K and/or external RAM up to 64 K
- Boolean processing
- 218 bit-addressable locations
- On-chip oscillator
- Five-source interrupt structure with two priority levels
- 58% of instructions executed in 1 μs; multiply and divide in 4 μs; all others executed in 2 μs (at 12 MHz clock)
- Enhanced architecture with:
  non-page-oriented-instructions
  direct addressing
  four 8-byte + 1-byte register banks
  stack depth up to 128-bytes
  multiply, divide, subtract and compare instructions.
- Available as
  PCB80C51/C31BH with 1,2 to 16 MHz
  PCF80C51/C31BH with 1,2 to 12 MHz

PACKAGE OUTLINES

PCB/PCF80C31BH/51BHP: 40-lead DIL; plastic (SOT-129).
PCB/PCF80C31BH/51BHWP: 44-lead PLCC; plastic, leaded-chip-carrier (SOT-187A).



(1) PCB80C51BH only.

Fig. 1 Block diagram.

type	temp. range	frequency range	$I_{CC\,max}$ at 5,5 V
PCB80C51BH PCB80C31BH	0 – 70 °C	1,2 – 16 MHz	23 mA*
PCF80C51BH PCF80C31BH	–40 – + 85 °C	1,2 – 12 MHz	18 mA*

* Preliminary value.

STATIC CMOS EEPROM (256 x 8 BIT)

GENERAL DESCRIPTION

The PCB8582 is a 2K-bit 5 V electrically erasable programmable read only memory (EEPROM) organized as 256 by 8 bits. It is designed in a floating gate CMOS technology.

As data bytes are received and transmitted via the serial I^2C bus, an eight pin DIL package is sufficient. Up to eight PCB8582 devices may be connected to the I^2C bus.

Chip select is accomplished by three address inputs.

Features

- Non-volatile storage of 2K-bit organized as 256 x 8
- Only one power supply required (5 V)
- On chip voltage multiplier for erase/write
- Serial input/output bus (I^2C)
- Automatic word address incrementing
- Low power consumption
- One point erase/write timer
- Power on reset
- 10 000 erase/write cycles per byte
- 10 years non-volatile data retention
- Infinite number of read cycles
- Pin and address compatible to PCF8570, PCF8571 and PCD8572

- A version for extended temperature range; −40 to + 85 °C in preparation: PCF8582.

PACKAGE OUTLINE

PCB8582P: 8-lead DIL; plastic (SOT-97AE).

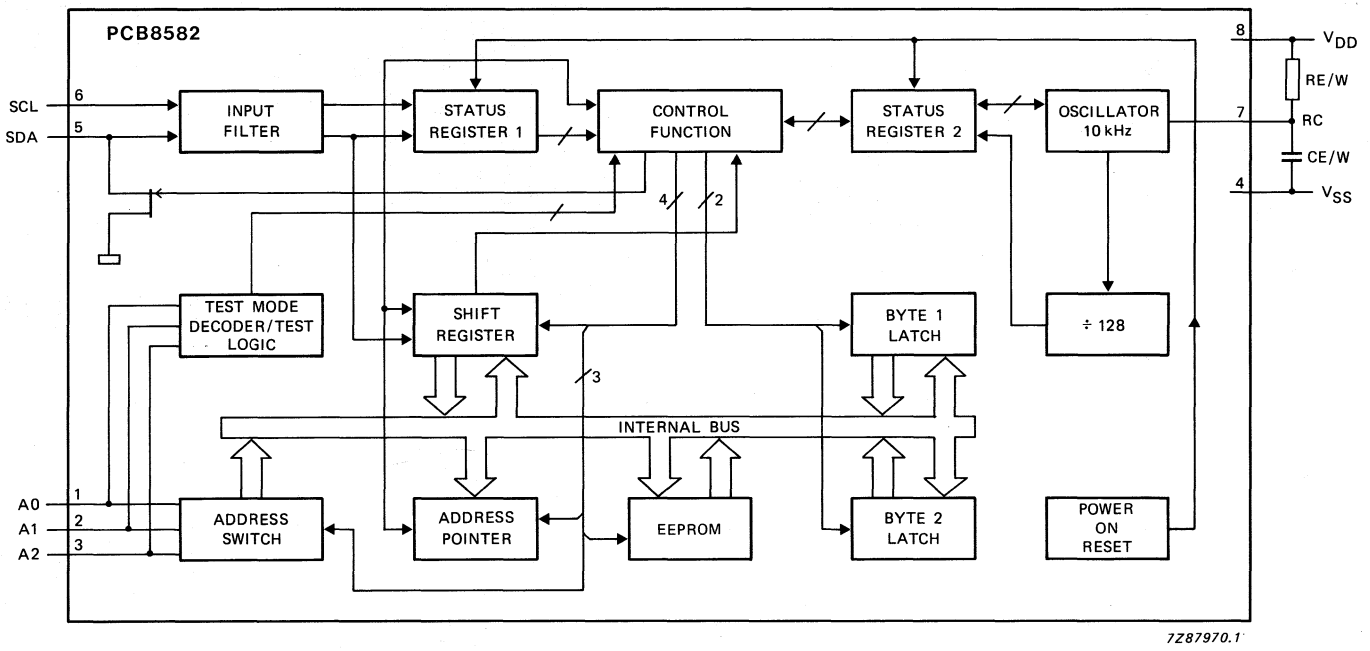


Fig. 1 Block diagram.

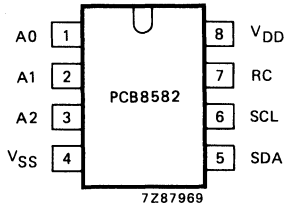


Fig. 2 Pinning diagram.

1 A0
2 A1 address inputs/test
3 A2 mode select
4 V_{SS} ground
5 SDA, 6 SCL: I^2C bus lines
7 RC input for timer constant
8 V_{DD} positive supply

FUNCTIONAL DESCRIPTION

Characteristics of the I^2C bus

The I^2C bus is intended for communication between different ICs. The serial bus consists of two bi-directional lines, one for data signals (SDA), and one for clock signals (SCL). Both the SDA and the SCL lines must be connected to a positive supply voltage via a pull-up resistor.

The following protocol has been defined:
Data transfer may be initiated only when the bus is not busy.
During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as control signals.

Accordingly, the following bus conditions have been defined:
Bus not busy: both data and clock lines remain HIGH.
Start data transfer: a change in the state of the data line, from HIGH to LOW, while the clock is HIGH defines the start condition.
Stop data transfer: a change in the state of the data line, from LOW to HIGH, while the clock is HIGH, defines the stop condition.
Data valid: the state of the data line represents valid data when, after a start condition, the data line is stable for the duration of the HIGH period of the clock signal. The data on the line may be changed during the LOW period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a start condition and terminated with a stop condition; the number of the data bytes, transfered between the start and stop conditions is limited to two bytes in the ERASE/WRITE mode and unlimited in the READ mode. The information is transmitted in bytes and each receiver acknowledges with a ninth bit.

Within the I^2C bus specifications a low-speed mode (2 kHz clock rate) and a high-speed mode (100 kHz clock rate) are defined. The PCB8582 works in both modes.
By definition a device that gives out a signal is called a "transmitter", and the device which receives the signal is called a "receiver". The device which controls the signal is called the "master". The devices that are controlled by the master are called "slaves".

Each word of eight bits is followed by one acknowledge bit. This acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master generates an extra acknowledge related clock pulse.
A slave receiver which is addressed is obliged to generate an acknowledge after the reception of each byte.
Also, a master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter.
The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the high period of the acknowledge related clock pulse.
Set-up-and hold times must be taken into account. A master receiver must signal an end of data to the slave transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this case the transmitter must leave the data line HIGH to enable the master generation of the stop condition.

DEVELOPMENT DATA

Note

The general characteristics and detailed specification of the I²C bus are described in a separate data sheet (serial data buses) in handbook: ICs for digital systems in radio, audio and video equipment.

I²C bus protocol

The I²C bus configuration for different READ and WRITE cycles of the PCB8582 are shown in Fig. 3, (a) and (b).

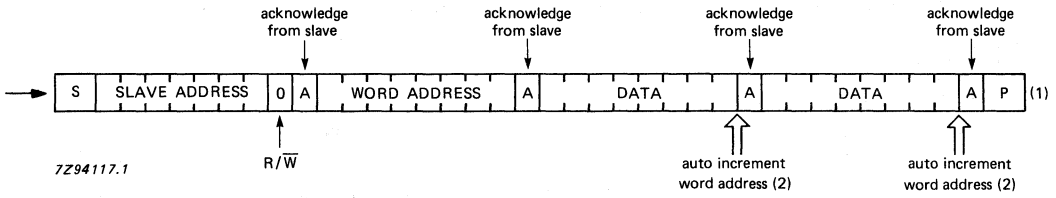


Fig. 3(a) Slave receiver ERASE/WRITE mode.

1. After this stop condition the erase/write cycle starts and the bus is free for another transmission; the duration of the erase/write cycle is approximatly 20 ms if only one byte is written, and 40 ms, if two bytes are written. During the erase/write cycle the slave receiver does not send an acknowledge bit if addressed via I²C bus.
2. The second data byte is voluntary. Trying to erase/write more than two bytes is not allowed.

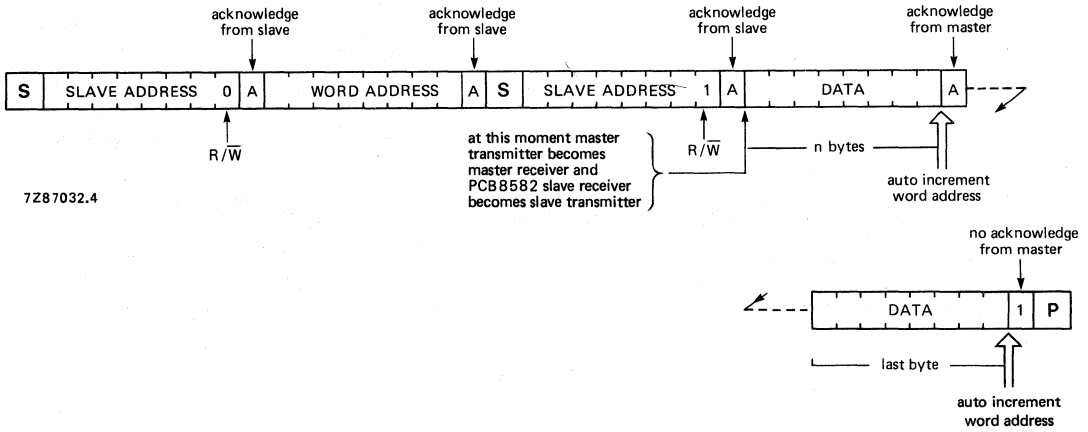


Fig. 3(b) Master reads PCB8582 slave after setting word address. (WRITE word address; READ data).

Note: The slave address is defined in accordance with the I²C bus specification as:

1	0	1	0	A2	A1	A0	R/W

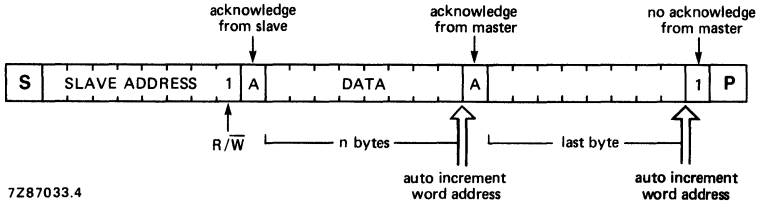


Fig. 3(c) Master reads PCB8582 slave immediately after first byte (READ mode).

I²C bus timing

Fig. 4 shows the I²C bus timing.

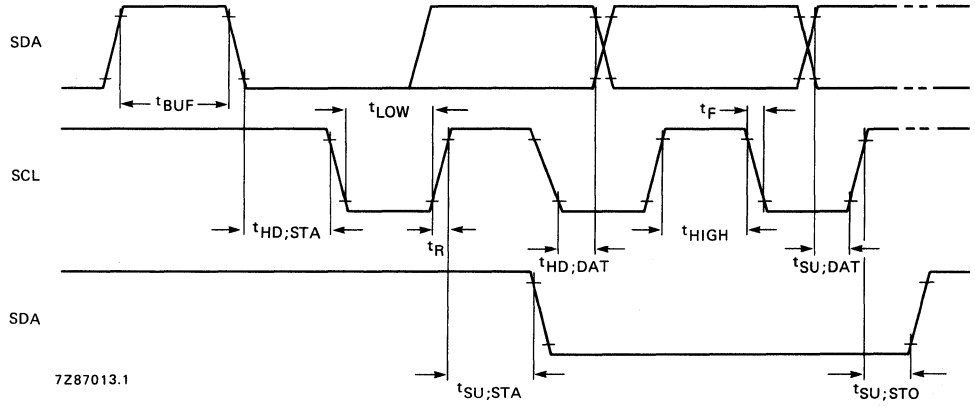


Fig. 4 Timing requirements for the I²C bus.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_{DD}	−0,3 to 7 V
Voltage, on any input pin (input impedance 500 Ω)	V_I	V_{SS}−0,8 to V_{DD} +0,8 V
Operating temperature range	T_{amb}	0 to +70 °C
Storage temperature range	T_{stg}	−65 to +150 °C
Current into any input pin	I_I	1 mA
Output current	I_O	10 mA

DEVELOPMENT DATA

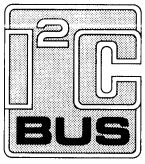
CHARACTERISTICS

V_{DD} = 5 V; V_{SS} = 0 V; T_{amb} = 0 to + 70 °C, unless otherwise specified.

parameter	symbol	min.	typ.	max.	unit
Operating supply voltage	V_{DD}	4,5	5	5,5	V
Operating supply current, READ (f_{SLC} = 100 kHz)	I_{DDR}	–	0,1	0,2	mA
Operating supply current, WRITE/ERASE	I_{DDW}	–	1	2	mA
Standby supply current (V_{DD} = 5 V)	I_{DDO}	–	5	10	μA
Input SCL and input/output SDA					
Input/output SDA:					
Input voltage LOW	V_{IL}	–0,3	–	1,5	V
Input voltage HIGH	V_{IH}	3	–	V_{DD}+0,8	V
Output voltage LOW (I_{OL} = 3 mA, V_{DD} = 4,5 V)	V_{OL}	–	–	0,4	V
Output leakage current HIGH (V_{OH} = V_{DD})	I_{OH}	–	–	1	μA
Input leakage current (A0,A1,A2, SCL), (note 1)	$\pm I_{IN}$	–	–	1	μA
Clock frequency	f_{SCL}	0	–	100	kHz
Input capacity (SCL,SDA)	C_I	–	–	7	pF
Noise suppression time constant at SCL and SDA input	t_I	0,25	0,5	1	μs
Time the bus must be free before a new transmission can start	t_{BUF}	4,7	–	–	μs
Hold time start condition. After this period the first clock pulse is generated	$t_{HD;STA}$	4	–	–	μs
The LOW period of the clock	t_{LOW}	4,7	–	–	μs
The HIGH period of the clock	t_{HIGH}	4	–	–	μs
Set-up time for start condition (only relevent for a repeated start condition)	$t_{SU;STA}$	4,7	–	–	μs
Hold time DATA for:					
CBUS compatible masters	$t_{HD;DAT}$	5	–	–	μs
I^2C devices (note 2)	$t_{HD;DAT}$	0	–	–	μs
Set-up time DATA	$t_{SU;DAT}$	250	–	–	ns
Rise time for both SDA and SCL lines	t_R	–	–	1	μs
Fall time for both SDA and SCL lines	t_F	–	–	300	ns
Set-up time for stop condition	$t_{SU;STO}$	4,7	–	–	μs
Erase/write timer constant (note 3)					
Erase/write cycle time	$t_{E/W}$	20	–	100	ms
Erase/write timing capacitor for erase/write cycle of 30 ms	$C_{E/W}$	–	3,3	–	nF
Erase/write timing resistor for erase/write cycle of 30 ms	$R_{E/W}$	–	56	–	kΩ
Data retention time	t_S	10	–	–	years

Notes to the characteristics

1. Selection of the chip address is done by connecting the A0, A1, and A2 inputs either to V_{SS} or V_{DD}.
2. A transmitter must internally provide a hold time to bridge the undefined region (maximum 300 ns) of the falling edge of SCL.
3. Endurance (number of erase/write cycles), NE/W, is 10^4 E/W cycles.



Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

DEVELOPMENT DATA

PULSE AND DTMF DIALLER WITH REDIAL

GENERAL DESCRIPTION

The PCD3310 is a single-chip silicon gate CMOS integrated circuit with an on-chip oscillator for a 3,58 MHz crystal. It is a dual-standard dialling circuit for either pulse dialling (PD) or dual tone multi-frequency (DTMF) dialling.

Input data is derived from any standard matrix keyboard for dialling in either DP or DTMF mode. Numbers of up to 23 digits can be retained in RAM for redial and notepad facilities.

In DTMF mode bursts as well as pauses are timed to a minimum, in manual dialling the maximum depends on the key depression time.

Features

- Pulse and DTMF dialling
- 23-digit capacity for redial operation (cursor method)
- Memory clear and electronic notepad
- Mixed mode dialling; start with PD and end with DTMF dialling
- Dual redial buffers for PABX and public calls
- Four extra function keys; program, flash, redial, PD to DTMF (mixed dialling)
- DTMF timing:
  - manual dialling — minimum duration for bursts and pauses
  - redialling — calibrated timing
- On-chip voltage reference for supply and temperature independent tone output
- On-chip filtering for low output distortion (CEPT CS 203 compatible)
- On-chip oscillator uses low-cost 3,58 MHz (tv colour burst) crystal
- Uses standard single-contact or double-contact (common left open) keyboard
- Keyboard entries fully debounced
- Flash (register recall) output

QUICK REFERENCE DATA

Operating supply voltage	V_{DD}	2,5 to 6,0	V
Standby supply voltage	V_{DDO}	1,8 to 6,0	V
Low standby current (on hook) at V_{DDO} = 1,8 V	I_{DDO}	max. 5	μA
Operating currents at V_{DD} = 3,0 V			
conversation mode	I_{DDC}	max. 150	μA
pulse dialling mode	I_{DDP}	max. 200	μA
DTMF dialling mode	I_{DDF}	max. 1,2	mA
DTMF output voltage level (r.m.s. values)			
HIGH group	$V_{HG(rms)}$	typ. 192	mV
LOW group	$V_{LG(rms)}$	typ. 150	mV
Pre-emphasis of group	ΔV_G	typ. 2,1	dB
Total harmonic distortion	THD	−25	dB
Operating ambient temperature range	T_{amb}	−25 to + 70	°C

PACKAGE OUTLINES

PCD3310P: 20-lead DIL; plastic (SOT-146).
PCD3310T: 28-lead mini-pack; plastic (SO-28; SOT-136A).

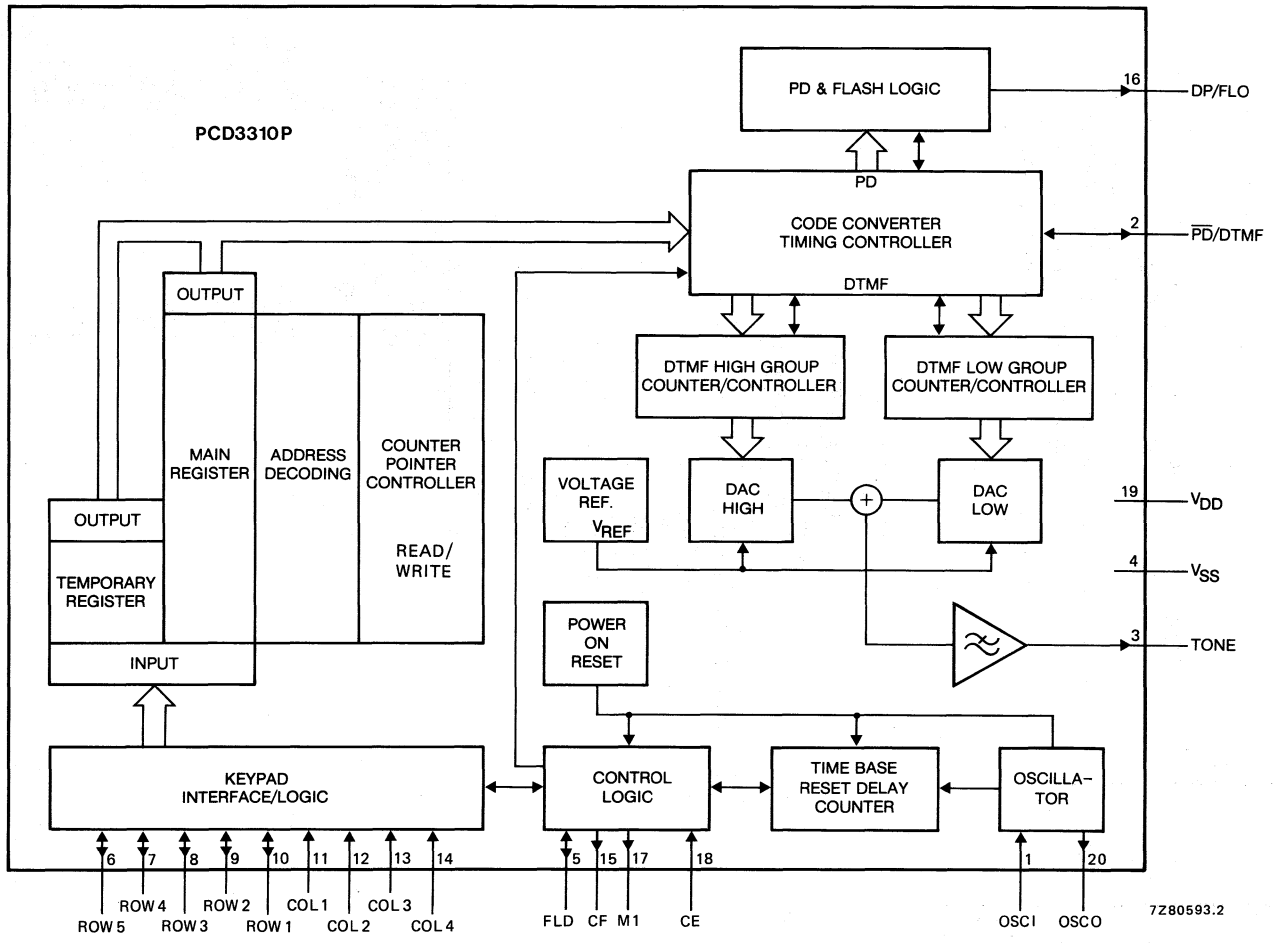


Fig. 1 Block diagram; PCD3310P.

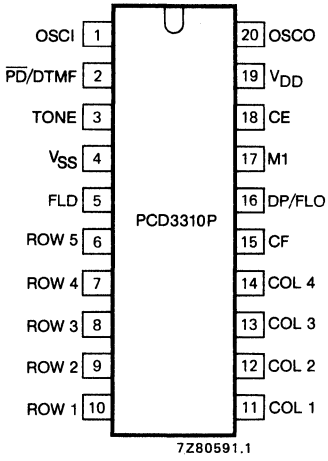
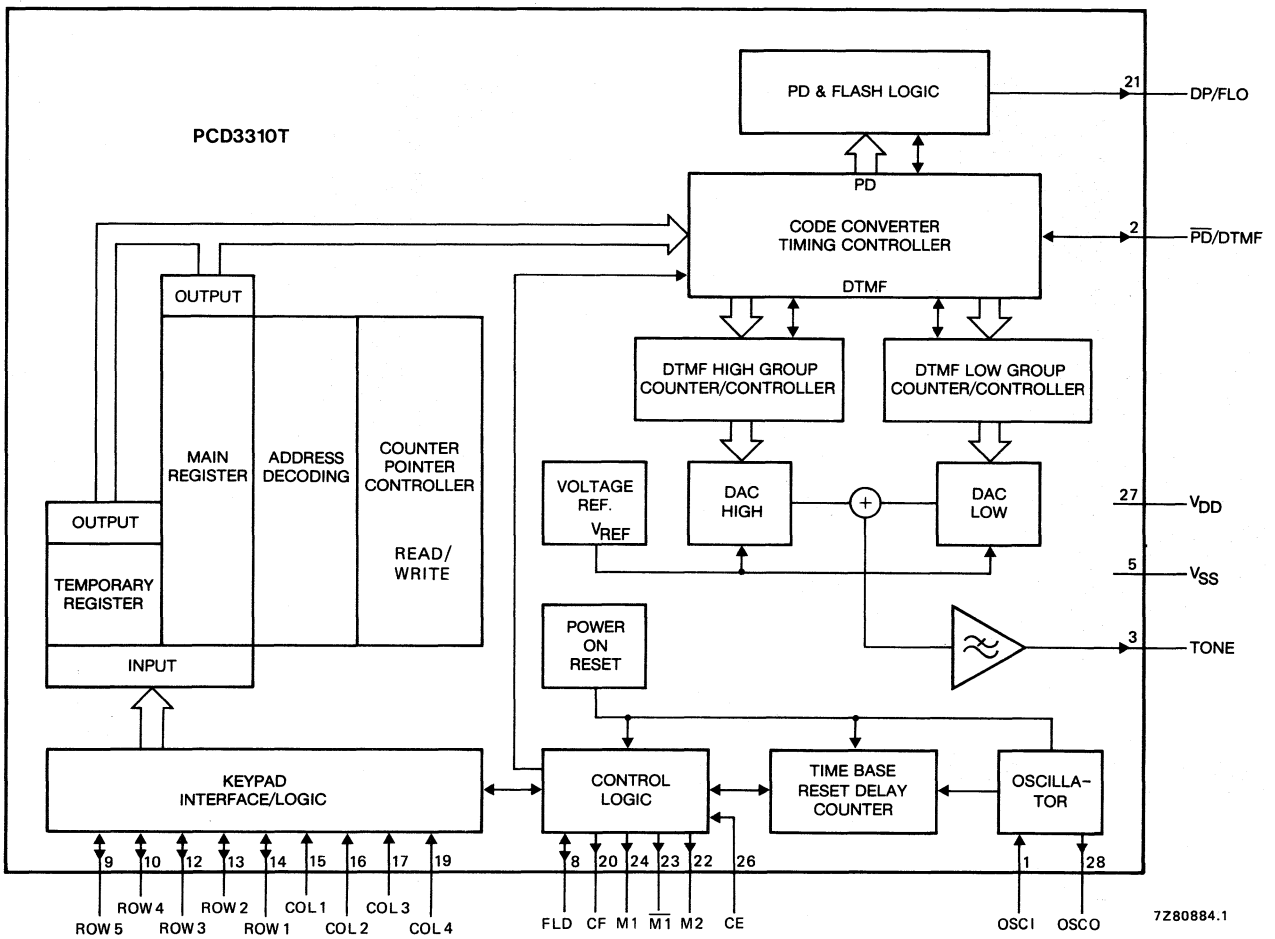


Fig. 2 Pinning diagram; PCD3310P.

PINNING

1	OSCI	oscillator input
2	$\overline{PD}$/DTMF	select pin; pulse or DTMF dialling
3	TONE	single or dual tone frequency output
4	V_{SS}	negative supply
5	FLD	flash duration control input/output
6	ROW 5	scanning row keyboard input/outputs
7	ROW 4	
8	ROW 3	
9	ROW 2	
10	ROW 1	
11	COL 1	sense column keyboard inputs with internal pull-ups
12	COL 2	
13	COL 3	
14	COL 4	
15	CF	330 Hz confidence tone output to provide audible feedback of key entries
16	DP/FLO	dialling pulse and flash output
17	M1	muting output
18	CE	chip enable input
19	V_{DD}	positive supply
20	OSCO	oscillator output

DEVELOPMENT DATA



Note: Pins 4, 6, 7, 11, 18 and 25 are not connected.

Fig. 3 Block diagram; PCD3310T.

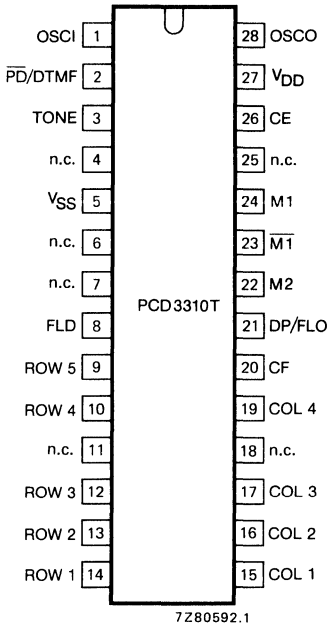


Fig. 4 Pinning diagram for PCD3310T.

PINNING

1	OSCI	oscillator input
2	$\overline{PD}$/DTMF	select pin; pulse or DTMF dialling
3	TONE	single or dual tone frequency output
4	n.c.	not connected
5	V_{SS}	negative supply
6	n.c.	not connected
7	n.c.	not connected
8	FLD	flash duration control input/output
9	ROW 5	scanning row keyboard input/outputs
10	ROW 4	
11	n.c.	not connected
12	ROW 3	scanning row keyboard input/outputs
13	ROW 2	
14	ROW 1	
15	COL 1	sense column keyboard inputs with internal pull-ups
16	COL 2	
17	COL 3	
18	n.c.	not connected
19	COL 4	sense column keyboard input with internal pull-up
20	CF	330 Hz confidence tone output to provide audible feedback of key entries
21	DP/FLO	dialling pulse and flash output
22	M2	strobe; active HIGH during transmission
23	$\overline{M1}$	inverted mute output
24	M1	muting output
25	n.c.	not connected
26	CE	chip enable input
27	V_{DD}	positive supply
28	OSCO	oscillator output

DEVELOPMENT DATA

FUNCTIONAL DESCRIPTION

Power supply (V_{DD}; V_{SS})

The positive supply of the circuit (V_{DD}) must meet the voltage requirements as indicated in the characteristics.
To avoid undefined states of the device when powered-on, an internal reset circuit clears the control logic and counters.
If V_{DD} drops below the minimum standby supply voltage of 1,8 V the power-on-reset circuit inhibits redialling after hook-off.
The power-on-reset signal has the highest priority it blocks and resets the complete circuit without delay regardless of the state of chip enable input (CE).

Clock oscillator (OSCI, OSCO)

The time base for the PCD3310 for both PD and DTMF modes is a crystal controlled on-chip oscillator which is completed by connecting a 3,58 MHz crystal between the OSCI and OSCO pins.

Chip Enable (CE)

The CE input enables the circuit and is used to initialize the IC.

CE = LOW provides the static standby condition. In this state the clock oscillator is disabled, all registers and logic are reset with the exception of the Write Address Counter (WAC) and Temporary Write Address Counter (TWAC) which point to the last entered digit (see Fig. 7). The keyboard input is inhibited, but data previously entered is saved in the redial register as long as V_{DD} is higher than $V_{DDO(min)}$.
The current drawn is I_{DDO} (standby current) and serves to retain data in the redial register during hook-on

CE = HIGH activates the clock oscillator and the circuit changes from static standby condition to the conversation mode. The current consumption is I_{DDC} until the first digit is entered from the keyboard. Then a dialling or redialling operation starts. The operating current is I_{DDP} if in the pulse dialling mode, or I_{DDF} if the DTMF dialling mode is selected.

If the CE input is taken to a LOW level for more than time t_{rd} (see Fig. 11a, Fig. 11b and timing data) an internal reset pulse will be generated at the end of the t_{rd} period. The system changes to the static standby state. Short CE pulses of $< t_{rd}$ will not affect the operation of the circuit and reset pulses are not produced.

Mode selection ($\overline{PD}$/DTMF)

PD mode

If $\overline{PD}$/DTMF = V_{SS} the pulse mode is selected. Entries of non-numeric keys are neglected, they are neither stored in the redial register nor transmitted.

DTMF mode

If $\overline{PD}$/DTMF = V_{DD} the dual tone multi-frequency dialling mode is selected. Each non-function pushbutton activated corresponds to a combination of two tones, each one out of four possible LOW and HIGH group frequencies. The frequencies are transmitted with a constant amplitude, regardless of power supply variations, and filtered off harmonic content to fulfil the CEPT CS 203 recommendations.

The transmission time is calibrated for redial. In manual operation the duration of bursts and pauses is the actual pushbutton depress time, but not less than the minimum transmission time (t_t) or minimum pause time (t_p).

Mixed mode

When the $\overline{PD}$/DTMF pin is open-circuit the mixed mode is selected. After activation of CE or FL (flash) the circuit starts as a pulse dialler and remains in this state until a non-numeric (A, B, C, D, *, #) or the ">" key is activated. Then the circuit changes over to DTMF dialling and remains there until FL is activated or, after a static standby condition, CE is re-activated.

A connection between $\overline{PD}$/DTMF pin and V_{DD} also initiates DTMF dialling. Chip enable, FL or a connection of $\overline{PD}$/DTMF pin to V_{SS} sets the circuit back to pulse dialling.

Keyboard inputs/outputs

The sense column inputs COL 1 to COL 4 and the scanning row outputs ROW 1 to ROW 5 of the PCD3310 are directly connected to the keyboard as shown in Fig. 5.
All keyboard entries are debounced on both the leading and trailing edges for approximately time t_e as shown in Fig. 11. Each entry is tested for validity.

When a pushbutton is pressed, keyboard scanning starts and only returns to the sense mode after release of the pushbutton.

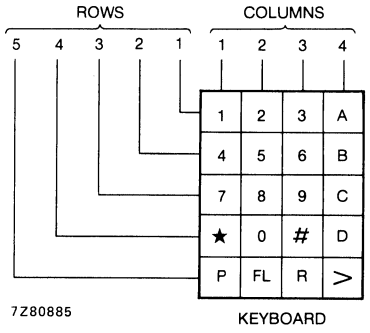


Fig. 5 Keyboard organization.

Row 5 of the keyboard contains the following special function keys:

- P memory clear and programming (notepad)
- FL flash or register recall
- R redial
- > change of dial mode from PD to DTMF in mixed dialling mode

In pulse dialling mode the valid keys are the 10 numeric pushbuttons (0 to 9). The non-numeric keys (A, B, C, D, *, #) have no effect on the dialling or the redial storage. Valid function keys are P, FL and R.

In DTMF mode all non-function keys are valid. They are transmitted as a dual tone combination and at the same time stored in the redial register. Valid function keys are P, FL and R.

In mixed mode all key entries are valid and executed accordingly.

DEVELOPMENT DATA

FUNCTIONAL DESCRIPTION (continued)

Flash duration control (FLD)

Flash (or register recall) is activated by the FL key and can be used in DTMF and pulse dialling mode. Pressing the FL pushbutton will produce a timed line-break of 100 ms (min.) at the DP/FLO output. During the conversation mode this flash pulse entry will act as a chip enable. This flash pulse duration (t_{FL}) is calibrated and can be prolonged with an external resistor and capacitor connected to the FLD input/output (see Fig. 6).

The flash pulse resets the read address counter (RAC). Later redial is possible (see redial procedure with the "Flash" inserted telephone number). The counter of the reset delay time is held during the period of t_{FL}.

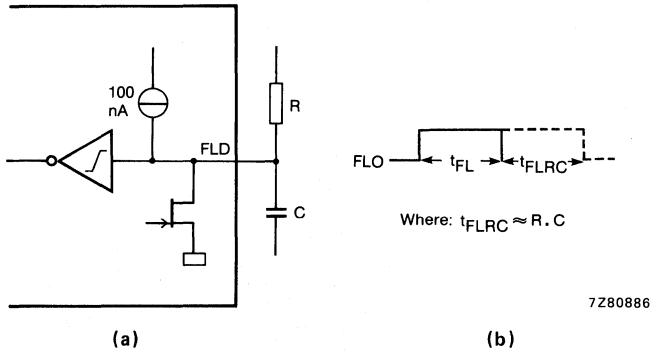


Fig. 6 Flash pulse duration setting.

TONE output (DTMF mode)

The single and dual tones which are provided at the TONE output are filtered by an on-chip switched-capacitor filter, followed by an on-chip active RC low-pass filter.

Therefore, the total harmonic distortion of the DTMF tones fulfils the CEPT CS 203 recommendations. An on-chip reference voltage provides output-tone levels independent of the supply voltage. Table 1 shows the frequency tolerance of the output tones for DTMF signalling.

Table 1 Frequency tolerance of the output tones for DTMF signalling

row/ column	standard frequency Hz	tone output frequency Hz (1)	frequency deviation	
			%	Hz
row 1	697	697,90	+ 0,13	+ 0,90
row 2	770	770,46	+ 0,06	+ 0,46
row 3	852	850,45	−0,18	−1,55
row 4	941	943,23	+ 0,24	+ 2,23
col 1	1209	1206,45	−0,21	−2,55
col 2	1336	1341,66	+ 0,42	+ 5,66
col 3	1477	1482,21	+ 0,35	+ 5,21
col 4	1633	1638,24	+ 0,32	+ 5,25

(1) Tone output frequency when using a 3,579 545 MHz crystal.

When the DTMF mode is selected output tones are timed in manual dialling with a minimum duration of bursts and pauses, and in redial with a calibrated timing. Single tones may be generated for test purposes (CE = HIGH). Each row and column has one corresponding frequency. High group frequencies are generated by connecting the column to V_{SS}. Low group frequencies are generated by forcing the row to V_{DD}. The single tone frequency will be transmitted during activation time, but it is neither calibrated nor stored.

Dial pulse and flash output (DP/FLO)

This is a combined output which provides control signals for proper timing in pulse dialling or for a calibrated break in both dialling modes (flash or register recall).

Mute output (M1)

During pulse dialling the mute output becomes active HIGH for the period of the inter-digit pause, break time and make time. It remains at this level until the last digit is pulsed out.

During DTMF dialling the mute output becomes active HIGH for the period of tone transmission and remains at this level until the end of hold-over time. It is also active HIGH during flash and flash hold-over time.

Mute output ($\overline{M1}$)

Inverted output of M1. In the PCD3310P it is only available as a bonding option of M1.

Strobe output (M2)

Active HIGH output during actual dialling; i.e. during break or make time in pulse dialling, or during tone ON/OFF in DTMF dialling.

Confidence tone output (CF)

When any of the keys are activated a square-wave is generated and appears at this output to serve as an acoustic feedback for the user.

DIALLING PROCEDURES (see also Figs 8, 9 and 10)

Dialling

After CE has risen to V_{DD} the oscillator starts running and the Read Address Counter (RAC) is set to the first address (see Fig. 7). By entering the first valid digit, the Temporary Write Address Counter (TWAC) will be set to the first address, the decoded digit will be stored in the register and the TWAC incremented to the next address. Any subsequent keyboard entry will be decoded and stored in the redial register after validation. The first 5 valid entries have no effect on the main register and its associated write address counter. After the sixth valid digit is entered TWAC indicates an overflow condition. The data from the temporary register will be copied into the 5 least significant places of the main register and TWAC into the WAC. All following digits (including the sixth digit) will be stored in the main register (a total of not more than 23). If more than 23 digits are entered redial will be inhibited. If not more than 5 digits are entered only the temporary register and the associated TWAC are affected. All entries are debounced on both the leading and trailing edges for at least time t_e as shown in Fig. 11. Each entry is tested for validity before being deposited in the redial register.

- In DTMF mode all non-function keys are valid
- In PD mode only numeric keys are valid

Simultaneous to their acceptance and corresponding to the selected mode (PD, DTMF or mixed), the entries are transmitted as PD pulse-trains or as DTMF frequencies in accordance with postal requirements. Non-numeric entries are neglected during pulse dialling, they are neither stored nor transmitted.

Redialling

After CE has risen to V_{DD} the oscillator starts running and the Read Address Counter (RAC) is set to the first address to be sent. The PCD3310 is in the conversation mode.

If "R" is the first keyboard entry the circuit starts redialling the contents of the temporary register. If the overflow flag of the TWAC was set in the previous dialling, the redialling continues in the main register. If the flag was not set, the number residing in the temporary register will only be redialled until the temporary read and write registers are equal.

Before pressing "R" a dialling sequence with up to 4 digits is possible. If the digits are equal to the corresponding ones in the main register, then redial starts in the main register until the last digit stored is transmitted.

Timing in the DTMF mode is calibrated for both tone bursts and pauses.

In mixed mode only the first part entered (the pulse dialled part of the stored number) can be redialled.

During redial keyboard entries (function or non-function) are not accepted until the circuit returns to the conversation mode after completion of redialling.

No redial activity takes place if one of the following events occur:

- Power-on reset
- Memory clear ("P" without successive data entry)
- Memory overflow (more than 23 valid data entries)

DEVELOPMENT DATA

Notepad

The redial register can also be used as a notepad. In conversation mode a number with up to 23 digits can be entered and stored for redialling. By activating the program key (P) the WAC and TWAC pointers are reset. This acts like a memory clear (redial is inhibited). Afterwards, by entering and storing any digits, redialling will be possible after flash or hook on and off.

During notepad programming the numbers entered will neither be transmitted nor is the mute active, only the confidence tone is generated.

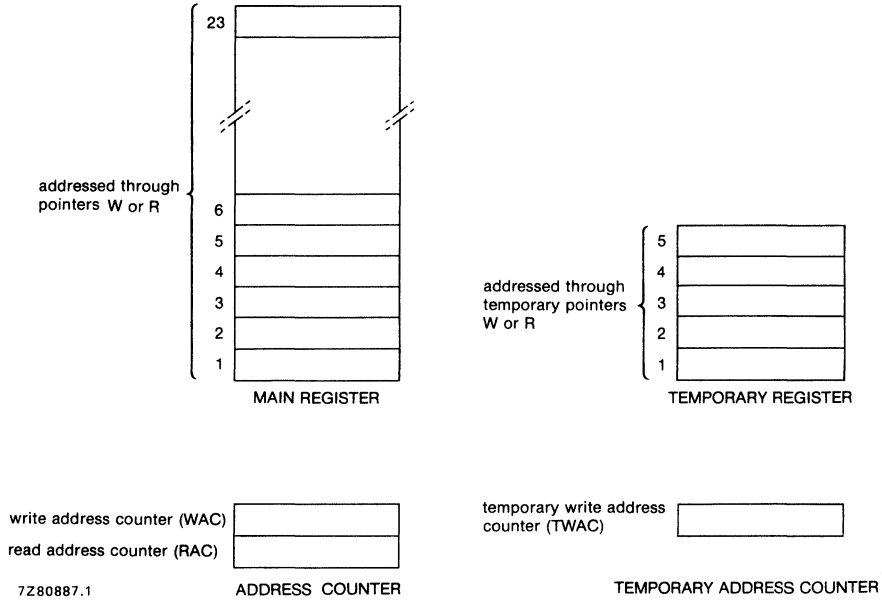
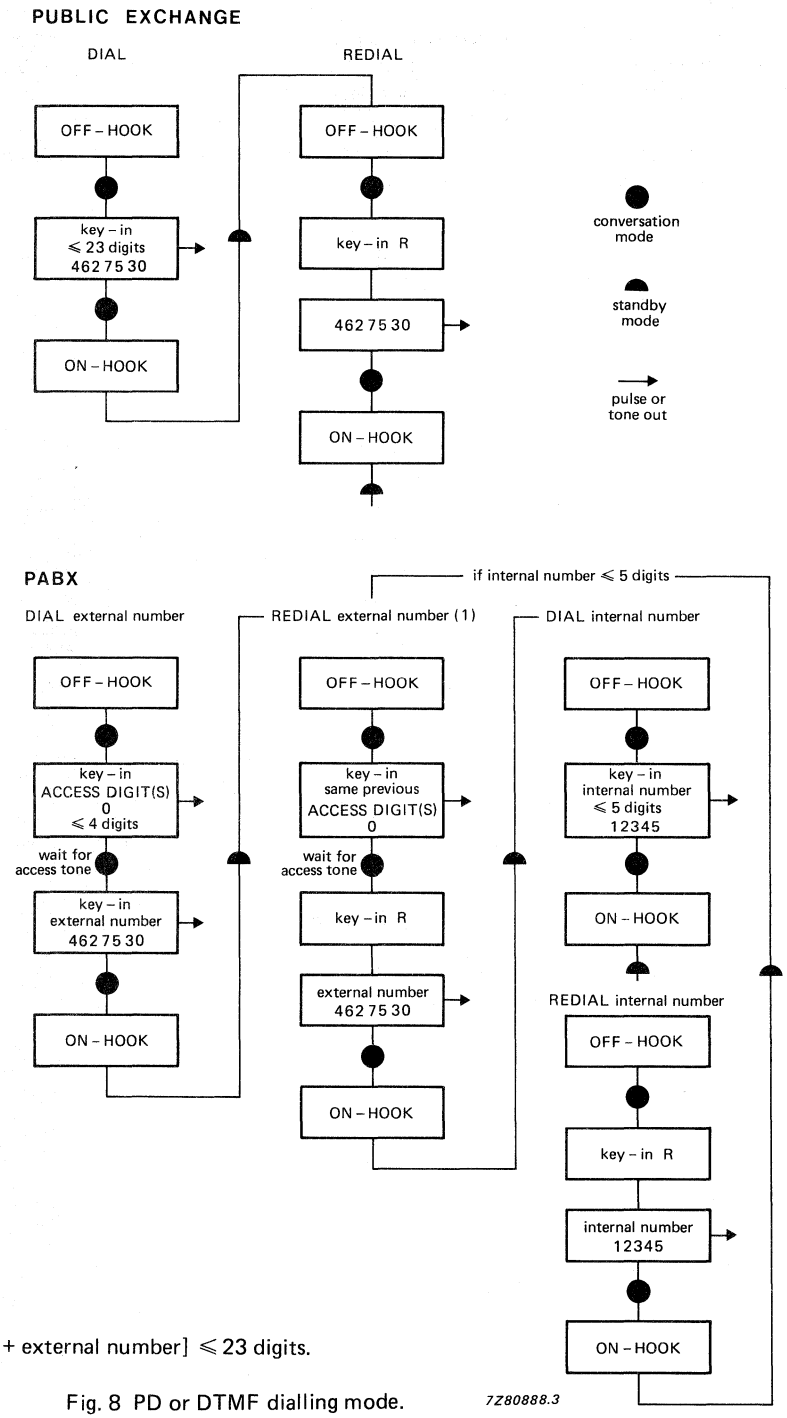


Fig. 7 Program memory map.

DIALLING PROCEDURES (continued)



(1) If [access digit(s) + external number] ⩽ 23 digits.

Fig. 8 PD or DTMF dialling mode.

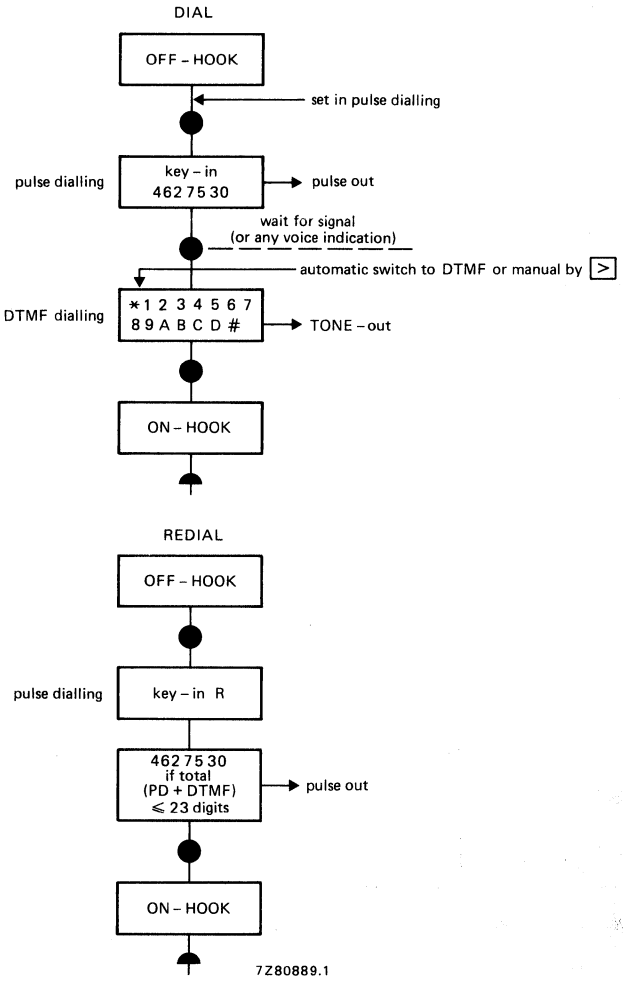


Fig. 9 PD/DTMF mixed mode dialling.

DIALLING PROCEDURES (continued)

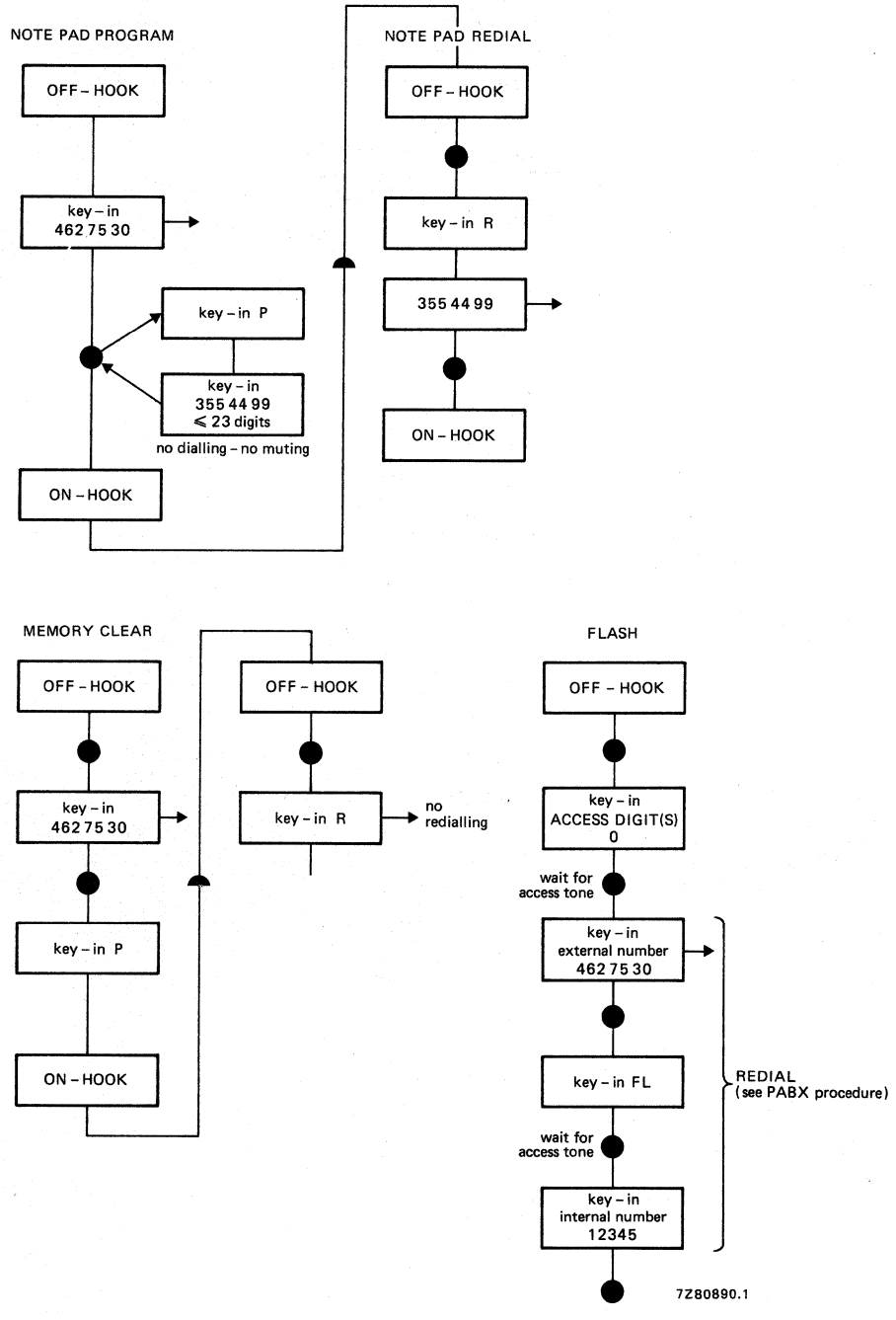


Fig. 10 Notepad, memory clear, flash; independent of dialling mode.

DEVELOPMENT DATA

TIMING

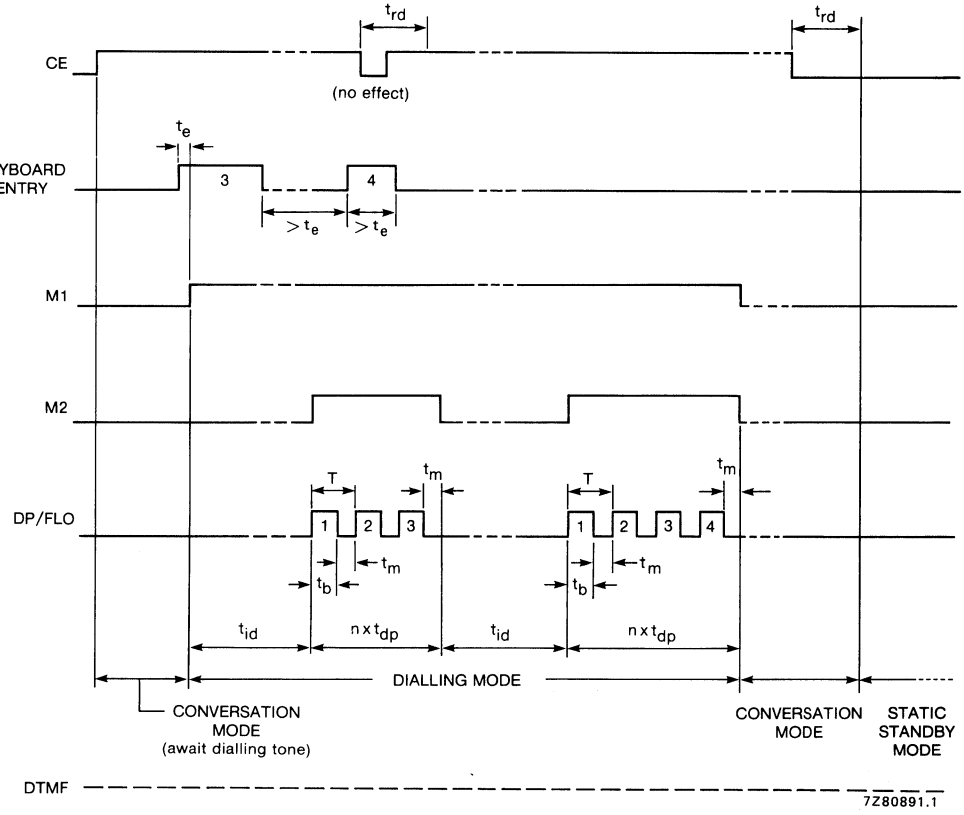


Fig. 11a Timing diagram for dialling mode defined by $\overline{PD}$/DTMF selection pin; pulse dialling ($\overline{PD}$/DTMF = V_{SS}).

TIMING (continued)

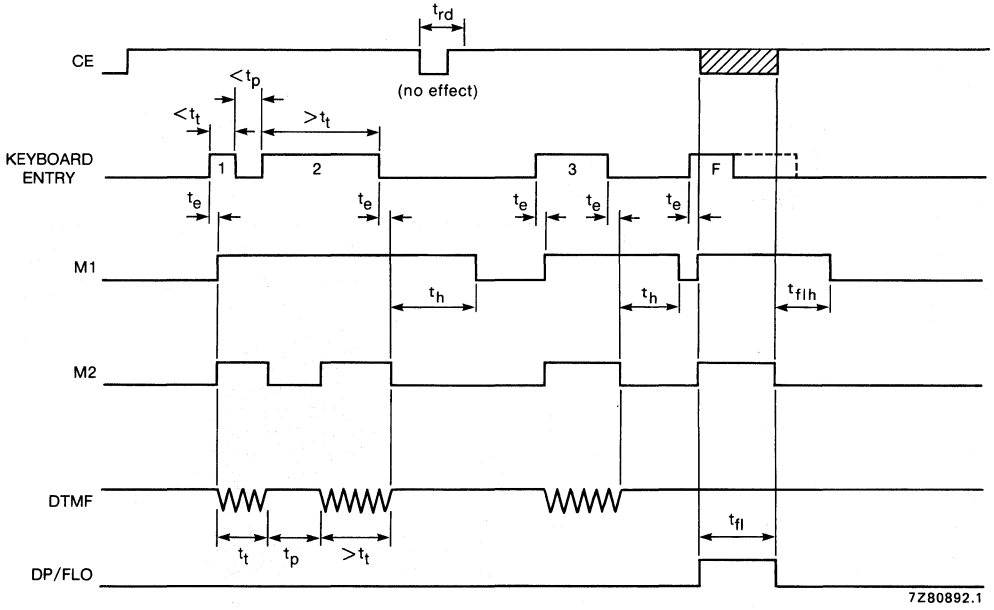


Fig. 11b Timing diagram for dialling mode defined by $\overline{PD}$/DTMF selection pin; DTMF dialling ($\overline{PD}$/DTMF = V_{DD}).

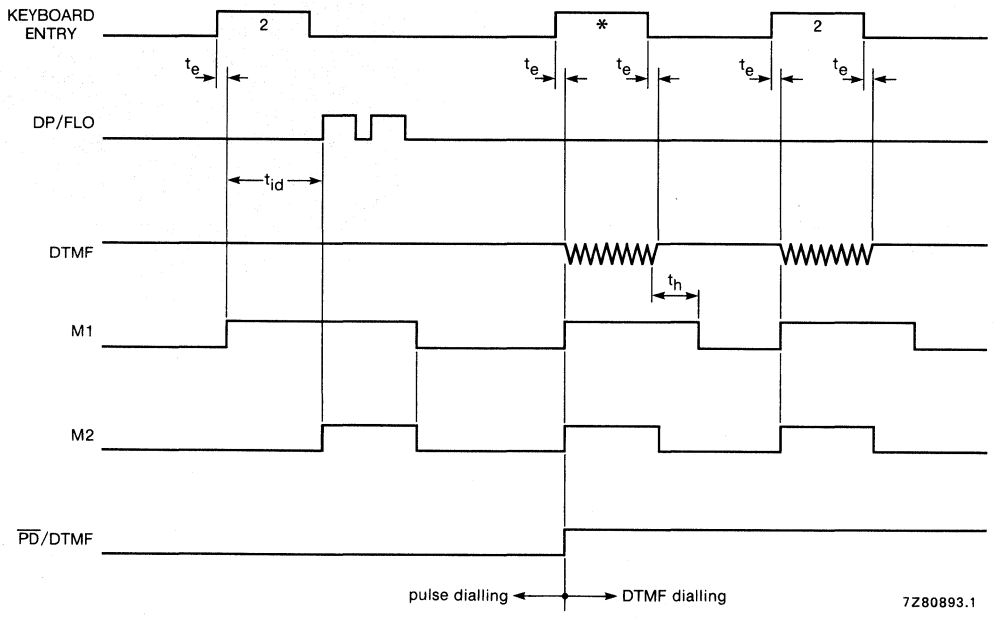


Fig. 11c Timing diagram for dialling mode defined by $\overline{PD}$/DTMF selection pin; mixed mode ($\overline{PD}$/DTMF open-circuit).

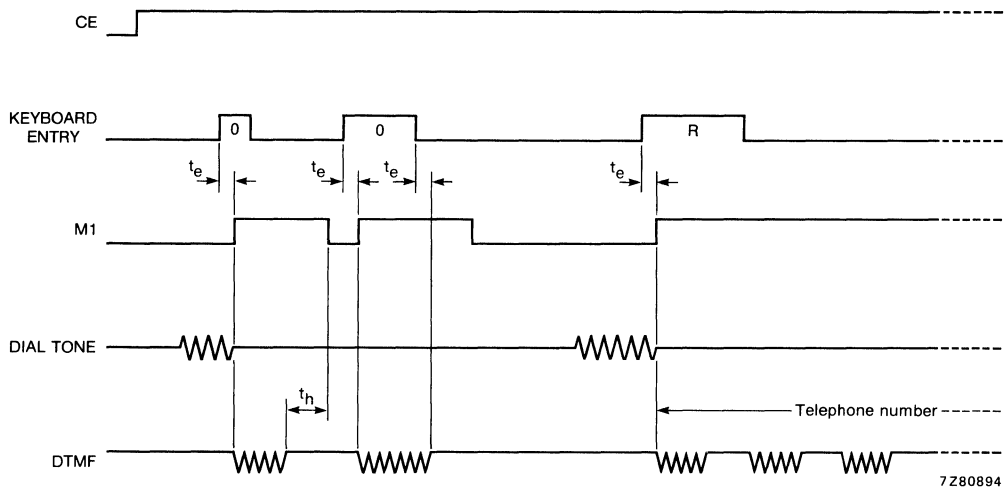


Fig. 12 Timing diagram showing REDIAL where PABX access digits are the first keyboard entries; DTMF dialling with $\overline{PD}$/DTMF = V_{DD}.

DEVELOPMENT DATA

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range	V_{DD}		−0,8 to 8	V
Supply current	I_{DD}	max.	50	mA
D.C. current into any input or output	$\pm I_I, \pm I_O$	max.	10	mA
All input voltages	V_I		−0,8 V to V_{DD} + 0,8	V
Total power dissipation	P_{tot}	max.	300	mW
Power dissipation per output	P_O	max.	50	mW
Storage temperature range	T_{stg}		−65 to + 150	°C
Operating ambient temperature range	T_{amb}		−25 to + 70	°C

CHARACTERISTICS

V_{DD} = 3 V; V_{SS} = 0 V; crystal parameters: f_{osc} = 3,579545 MHz; R_S = 100 Ω max.; T_{amb} = −25 to + 70 °C; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply					
Operating supply voltage	V_{DD}	2,5	–	6,0	V
Standby supply voltage	V_{DDO}	1,8	–	6,0	V
Operating supply current					
conversation mode (oscillator ON)	I_{DDC}	–	–	150	μA
pulse dialling or flash	I_{DDP}	–	–	200	μA
DTMF dialling (tone ON)	I_{DDF}	–	0,6	1,2	mA
DTMF dialling (tone OFF)	I_{DDF}	–	–	200	μA
Standby supply current (oscillator OFF; note 1) at V_{DD} = 1,8 V; T_{amb} = 25 °C	I_{DDO}	–	–	5	μA
INPUTS					
Input voltage LOW (any pin)	V_{IL}	0	–	$0{,}3V_{DD}$	V
Input voltage HIGH (any pin)	V_{IH}	$0{,}7V_{DD}$	–	V_{DD}	V
Input leakage current; CE	$\lvert I_{IL}\rvert$	–	–	1	μA
Keyboard inputs					
Keyboard ON current	I_{ON}	–	–	45	μA
Keyboard OFF current	I_{OFF}	7,5	–	–	μA
OUTPUTS					
Output sink current at $V_{OL} = V_{SS} + 0{,}5$ V					
M1, $\overline{M1}$, M2, DP/FLO, CF, FLD	I_{OL}	0,7	–	–	mA
$\overline{PD}$/DTMF (note 2)	I_{OL}	–	1	–	mA
Output source current at $V_{OH} = V_{DD} - 0{,}5$ V					
M1, $\overline{M1}$, M2, DP/FLO, CF	$-I_{OH}$	0,6	–	–	mA
$\overline{PD}$/DTMF (note 2)	$-I_{OH}$	–	1	–	mA
FLD (note 3)	$-I_{OH}$	–	100	–	nA
TIMING AND FREQUENCY					
Clock start-up time	t_{on}	–	4	–	ms
Debounce time	t_e	–	12	–	ms
Reset delay time	t_{rd}	–	160	–	ms
Confidence tone frequency	f_{ct}	–	330	–	Hz

parameter	symbol	min.	typ.	max.	unit
TONE output (see Fig. 13) at V_{DD} = 2,5 to 6 V					
DTMF output voltage levels (r.m.s. value)					
HIGH group	$V_{HG(rms)}$	158	192	205	mV
LOW group	$V_{LG(rms)}$	125	150	160	mV
Frequency deviation	$\Delta f/f$	−0,6	–	+ 0,6	%
D.C. voltage level	V_{DC}	–	$\frac{1}{2}V_{DD}$	–	V
Output impedance	$\lvert Z_O \rvert$	–	0,1	0,5	kΩ
Pre-emphasis of group	ΔV_G	1,85	2,1	2,35	dB
Total harmonic distortion at T_{amb} = 25 °C (note 4)	THD	–	−25	–	dB
Transmission and pause time					
Manual dialling	t_t, t_p	68	–	–	ms
Redialling	t_t, t_p	68	70	72	ms
Flash pulse duration	t_{FL}	98	100	102	ms
Flash hold-over time	t_{flh}	31	33	34	ms
Hold-over time (muting on M1)	t_h	78	80	81	ms
Pulse dialling (PD)					
Dialling pulse frequency	f_{dp}	9,8	10	10,4	Hz
Inter-digit pause	t_{id}	828	840	844	ms
Break time (note 5)	t_b	65	67	68	ms
Make time (note 5)	t_m	31	33	34	ms

DEVELOPMENT DATA

Notes to the characteristics

1. Crystal connected between OSCI and OSCO; CE at V_{SS} and all other pins open-circuit.
2. < |10 mA| dynamic current to set/reset $\overline{PD}$/DTMF pin (mixed mode).
3. Flash inactive; $V_{OH} = V_{SS}$.
4. Related to the level of the LOW group frequency component (CEPT CS 203).
5. Mark-to-space ratio 2 : 1.

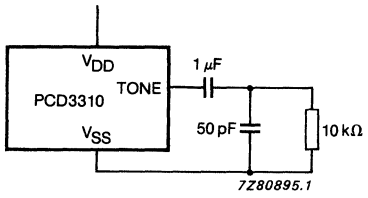
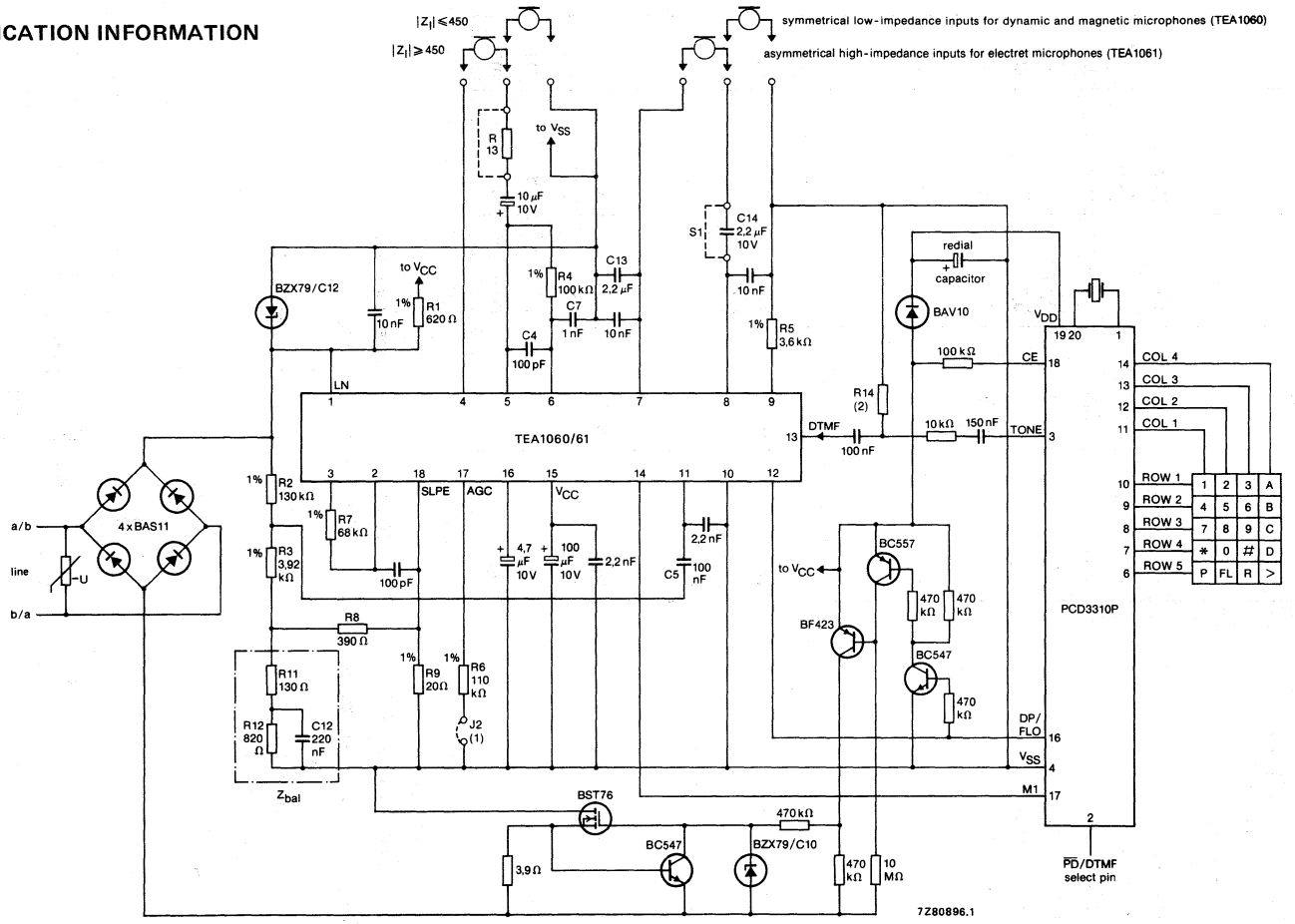


Fig. 13 Tone output test circuit.

APPLICATION INFORMATION



(1) Automatic line compensation obtained by connecting R6 to V_{SS}.

(2) The value of resistor R14 is determined by the required level at LN and the DTMF gain of the TEA1060.

Fig. 14 Application diagram of the full electronic basic telephone set.

DTMF/MODEM/MUSICAL-TONE GENERATORS

GENERAL DESCRIPTION

The PCD3311 and PCD3312 are single-chip silicon gate CMOS integrated circuits. They are intended to provide dual-tone multi-frequency (DTMF) combinations required for tone dialling systems in telephone sets which contain a microcontroller for the control functions.

The various audio output frequencies are generated from an on-chip 3,58 MHz quartz crystal-controlled oscillator.

The devices can interface directly to all standard microcontrollers by accepting a binary-coded parallel input or serial data input (I^2C bus).

With their on-chip voltage reference the PCD3311 and PCD3312 provide constant output amplitudes which are independent of the operating supply voltage and ambient temperature.

An on-chip filtering system assures a very low total harmonic distortion in accordance with the CEPT CS 203 recommendations.

In addition to the standard DTMF frequencies the devices provide 12 MODEM frequencies (300 to 1200 bits per second) used in simplex MODEM applications and two octaves of musical scale in steps of semitones.

Features

- Stabilized output voltage level
- Low output distortion with on-chip filtering (CEPT CS 203 compatible)
- Latched inputs for data bus applications
- I^2C bus compatible
- Mode select input (selection of parallel or serial data input)
- MODEM and melody tone generators

QUICK REFERENCE DATA

parameter	symbol	min.	typ.	max.	unit
Operating supply voltage	V_{DD}	2,5	–	6,0	V
Operating supply current	I_{DD}	–	–	1,2	mA
Static standby current	I_{DDO}	–	–	3	μA
DTMF output voltage level (r.m.s. values)					
HIGH group	$V_{HG(rms)}$	158	192	205	mV
LOW group	$V_{LG(rms)}$	125	150	160	mV
Pre-emphasis of group	ΔV_G	1,85	2,10	2,35	dB
Total harmonic distortion	THD	–	–25	–	dB
Operating ambient temperature range	T_{amb}	–25	–	+70	°C

PACKAGE OUTLINES

PCD3311P: 14-lead DIL; plastic (SOT-27KE).
PCD3311T: 16-lead mini-pack; plastic (SO-16L; SOT-162A).
PCD3312P: 8-lead DIL; plastic (SOT-97AE).
PCD3312T: 8-lead mini-pack; plastic (SO-8L; SOT-176).

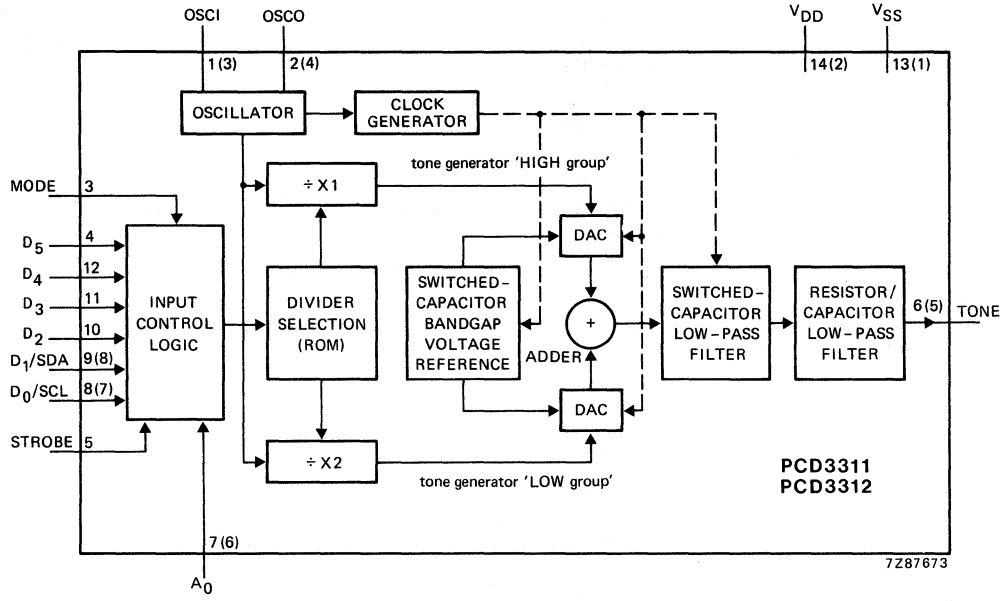


Fig. 1 Block diagram; the pin numbers in parenthesis refer to the PCD3312.

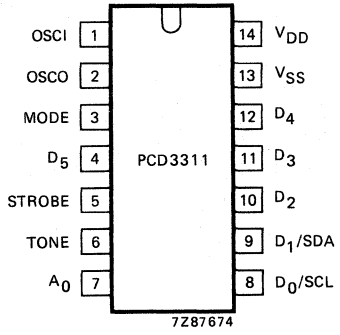


Fig. 2 Pinning diagram for the PCD3311.

PINNING

1	OSCI	oscillator input
2	OSCO	oscillator output
3	MODE	mode select input; used for the selection between serial mode (MODE = LOW) and parallel mode (MODE = HIGH)
4	D_5	parallel data input*
5	STROBE	strobe input; used for the loading of data in the parallel mode
6	TONE	frequency output for single or dual tones
7	A_0	slave address input in the serial mode; must be connected to V_{DD} or V_{SS}
8	D_0/SCL	parallel data input* or serial clock line (I^2C bus)
9	D_0/SDA	parallel data input* or serial data line (I^2C) bus)
10	D_2	parallel data inputs*
11	D_3	
12	D_4	
13	V_{SS}	negative supply
14	V_{DD}	positive supply

* MODE = HIGH.

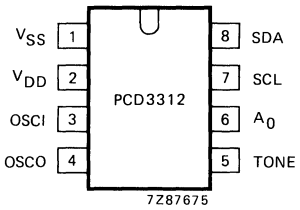


Fig. 3 Pinning diagram for the PCD3312.

PINNING

1	V_{SS}	negative supply
2	V_{DD}	positive supply
3	OSCI	oscillator input
4	OSCO	oscillator output
5	TONE	frequency output for single or dual tones
6	A_0	slave address input in the serial mode; must be connected to V_{DD} or V_{SS}
7	SCL	serial clock line (I^2C bus)
8	SDA	serial data line (I^2C bus)

FUNCTIONAL DESCRIPTION

Clock/oscillator (OSCI and OSCO)

The timebase for the PCD3311 and PCD3312 is a crystal-controlled oscillator with a 3,58 MHz quartz crystal connected between OSCI and OSCO. Alternatively, the OSCI input can be driven from an external clock.

Mode select (MODE)

This input selects the data input mode. When connected to V_{DD}, data can be received in the parallel mode (only for the PCD3311), or, when connected to V_{SS} or left open, data can be received via the serial I^2C bus (for both PCD3311 and PCD3312).

Parallel mode can only be obtained for the PCD3311 by setting MODE input HIGH.

Data inputs (D_0, D_1, D_2, D_3, D_4 and D_5)

Inputs D_0 and D_1 have no internal pull-down or pull-up resistors and must not be left open in any application. Inputs D_2 to D_5 have internal pull-down. D_5 and D_4 are used to select between DTMF dual, DTMF single, MODEM and melody tones (see Table 1). D_3 to D_0 select the combination of the tones for DTMF or single-tone itself.

Table 1 D_5 and D_4 in accordance with the selected application

D_5	D_4	application
0	0	DTMF single tones; standby; melody tones
0	1	DTMF dual tones (all 16 combinations)
1	0	MODEM tones; standby; melody tones
1	1	melody tones

1 = H = HIGH voltage level
0 = L = LOW voltage level

Note: Tables 2, 3, 4 and 5 show all input codes and their corresponding output frequencies.

DEVELOPMENT DATA

FUNCTIONAL DESCRIPTION (continued)

Strobe input (STROBE, only for the PCD3311)

This input (with internal pull-down) allows the loading of parallel data into D_0 to D_5 when MODE is HIGH.

The data inputs must be stable preceeding the positive-going edge of the strobe pulse (active HIGH). Input data are loaded at the negative-going edge of the strobe pulse and then the corresponding tone (or standby mode) is provided at the TONE output. The output remains unchanged until the negative-going edge of the next STROBE pulse (for new data) is received.

Serial mode can only be obtained for the PCD3311 by setting MODE input LOW.

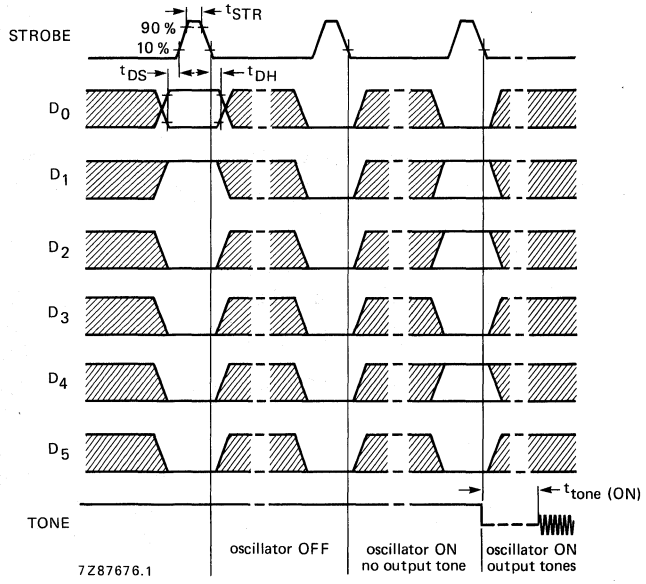


Fig. 4 Timing diagram showing control possibilities of the oscillator and the TONE output (e.g. 770 Hz + 1477 Hz) in the parallel mode (MODE = HIGH).

Serial clock and data inputs (SCL and SDA)

SCL and SDA are combined with D_0 and D_1 respectively. For the PCD3311 the selection of SCL and SDA is controlled by the MODE input. SCL and SDA are serial clock and data lines according to the I^2C bus specification (see "CHARACTERISTICS OF THE I^2C BUS"). Both inputs must be pulled-up externally to V_{DD}.

Address input (A_0)

A_0 is the slave address input and it identifies the device when up to two PCD3311 or PCD3312 devices are connected to the same I^2C bus. In any case A_0 must be connected to V_{DD} or V_{SS}.

I²C bus data configuration (see Fig. 5)

The PCD3311 and PCD3312 are always slave receivers in the I²C bus configuration (R/$\overline{W}$ bit = 0).

The slave address consists of 7 bits in the serial mode for the PCD3311 as well as for the PCD3312, where the least significant bit is selectable by hardware on input A_0 and the other more significant bits are internally fixed. In the serial mode the same input codes are used as in the parallel mode (see Tables 2, 3, 4, and 5). D_6 and D_7 are don't care (X) bits.

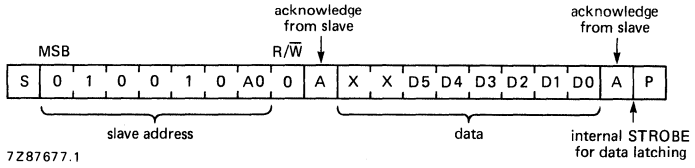


Fig. 5 I²C bus data format.

Tone output (TONE)

The single and the dual tones which are provided at the TONE output are filtered by an on-chip switched-capacitor filter, followed by an active RC low-pass filter. Therefore, the total harmonic distortion of the DTMF tones fulfils the CEPT CS 203 recommendations. An on-chip reference voltage provides output-tone levels independent of the supply voltage. Table 3 shows the frequency tolerance of the output tones for DTMF signalling; Tables 4 and 5 for the modem and melody tones.

Power-on reset

In order to avoid undefined states of the devices when the power is switched ON, an internal reset circuit sets them to the standby mode (oscillator OFF).

Table 2 Input data for control (no output tone; TONE at V_{DD})

D_5	D_4	D_3	D_2	D_1	D_0	HEX	oscillator
X	0	0	0	0	0	00/20	ON
X	0	0	0	0	1	01/21	OFF
X	0	0	0	1	0	02/22	OFF
X	0	0	0	1	1	03/23	OFF

1 = H = HIGH voltage level
0 = L = LOW voltage level
X= don't care

DEVELOPMENT DATA

FUNCTIONAL DESCRIPTION (continued)

Table 3 Input data for DTMF

D_5	D_4	D_3	D_2	D_1	D_0	HEX	symbol	standard frequency Hz	tone output freq. Hz**	frequency deviation %	frequency deviation Hz
0	0	1	0	0	0	08		697	697,90	+ 0,13	+ 0,90
0	0	1	0	0	1	09		770	770,46	+ 0,06	+ 0,46
0	0	1	0	1	0	0A		852	850,45	−0,18	−1,55
0	0	1	0	1	1	0B		941	943,23	+ 0,24	+ 2,23
0	0	1	1	0	0	0C		1209	1206,45	−0,21	−2,55
0	0	1	1	0	1	0D		1336	1341,66	+ 0,42	+ 5,66
0	0	1	1	1	0	0E		1477	1482,21	+ 0,35	+ 5,21
0	0	1	1	1	1	0F		1633	1638,24	+ 0,32	+ 5,24
0	1	0	0	0	0	10	0	941+1336			
0	1	0	0	0	1	11	1	697+1209			
0	1	0	0	1	0	12	2	697+1336			
0	1	0	0	1	1	13	3	697+1477			
0	1	0	1	0	0	14	4	770+1209			
0	1	0	1	0	1	15	5	770+1336			
0	1	0	1	1	0	16	6	770+1477			
0	1	0	1	1	1	17	7	852+1209			
0	1	1	0	0	0	18	8	852+1336			
0	1	1	0	0	1	19	9	852+1477			
0	1	1	0	1	0	1A	A	697+1633			
0	1	1	0	1	1	1B	B	770+1633			
0	1	1	1	0	0	1C	C	852+1633			
0	1	1	1	0	1	1D	D	941+1633			
0	1	1	1	1	0	1E	*	941+1209			
0	1	1	1	1	1	1F	#	941+1477			

Table 4 Input data for MODEM frequencies

D_5	D_4	D_3	D_2	D_1	D_0	HEX	standard frequency Hz	tone output freq. Hz**	frequency deviation %	frequency deviation Hz	remarks
1	0	0	1	0	0	24	1300	1296,94	−0,24	−3,06	V.23
1	0	0	1	0	1	25	2100	2103,14	+ 0,15	+ 3,14	
1	0	0	1	1	0	26	1200	1197,17	−0,24	−2,83	Bell 202
1	0	0	1	1	1	27	2200	2192,01	−0,36	−7,99	
1	0	1	0	0	0	28	980	978,82	−0,12	−1,18	V.21
1	0	1	0	0	1	29	1180	1179,03	−0,08	−0,97	
1	0	1	0	1	0	2A	1070	1073,33	+ 0,31	+ 3,33	Bell 103
1	0	1	0	1	1	2B	1270	1265,30	−0,37	−4,70	
1	0	1	1	0	0	2C	1650	1655,66	+ 0,34	+ 5,66	V.21
1	0	1	1	0	1	2D	1850	1852,77	+ 0,15	+ 2,77	
1	0	1	1	1	0	2E	2025	2021,20	−0,19	−3,80	Bell 103
1	0	1	1	1	1	2F	2225	2223,32	−0,08	−1,68	

** Tone output frequency when using a 3,579 545 MHz crystal.

1 = H = HIGH voltage level
0 = L = LOW voltage level

Table 5 Input data for melody tones

D_5	D_4	D_3	D_2	D_1	D_0	HEX	note	standard frequency Hz*	tone output frequency Hz**
1	1	0	0	0	0	30	D#5	622,3	622,5
1	1	0	0	0	1	31	E5	659,3	659,5
1	1	0	0	1	0	32	F5	698,5	697,9
1	1	0	0	1	1	33	F#5	740,0	741,1
1	1	0	1	0	0	34	G5	784,0	782,1
1	1	0	1	0	1	35	G#5	830,6	832,3
1	1	0	1	1	0	36	A5	880,0	879,3
1	1	0	1	1	1	37	A#5	932,3	931,9
1	1	1	0	0	0	38	B5	987,8	985,0
1	1	1	0	0	1	39	C6	1046,5	1044,5
1	1	1	0	1	0	3A	C#6	1108,7	1111,7
1	0	1	0	0	1	29	D6	1174,7	1179,0
1	1	1	0	1	1	3B	D#6	1244,5	1245,1
1	1	1	1	0	0	3C	E6	1318,5	1318,9
1	1	1	1	0	1	3D	F6	1396,9	1402,1
0	0	1	1	1	0	0E	F#6	1480,0	1482,2
1	1	1	1	1	0	3E	G6	1568,0	1572,0
1	0	1	1	0	0	2C	G#6	1661,2	1655,7
1	1	1	1	1	1	3F	A6	1760,0	1768,5
0	0	0	1	0	0	04	A#6	1864,7	1875,1
0	0	0	1	0	1	05	B6	1975,5	1970,0
1	0	0	1	0	1	25	C7	2093,0	2103,1
1	0	1	1	1	1	2F	C#7	2217,5	2223,3
0	0	0	1	1	0	06	D7	2349,3	2358,1
0	0	0	1	1	1	07	D#7	2489,0	2470,4

* Standard scale based on A4 = 440 Hz.

** Tone output frequency when using a 3,579 545 MHz crystal.

1 = H = HIGH voltage level

0 = L = LOW voltage level

DEVELOPMENT DATA

CHARACTERISTICS OF THE I²C BUS

The I²C bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals.

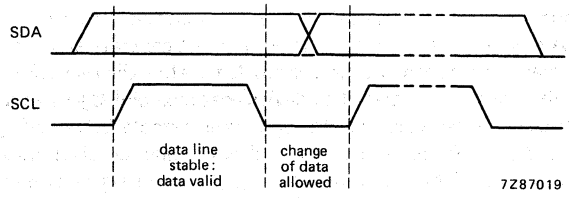


Fig. 6 Bit transfer.

Start and stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the stop condition (P).

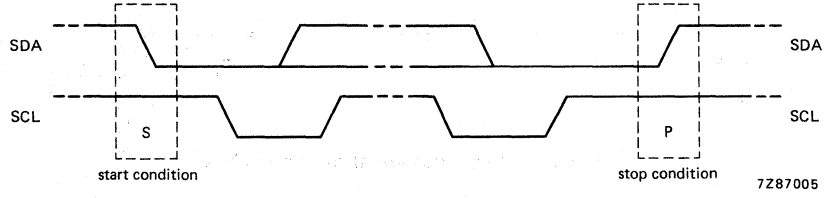


Fig. 7 Definition of start and stop conditions.

System configuration

A device generating a message is a "transmitter", a device receiving a message is the "receiver". The device that controls the message is the "master" and the devices which are controlled by the master are the "slaves".

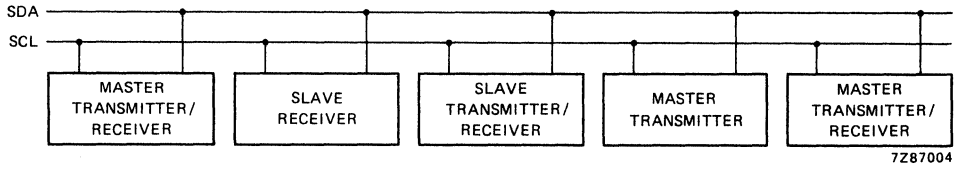


Fig. 8 System configuration.

Acknowledge

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse, set-up and hold times must be taken into account. A master receiver must signal an end of data to the transmitter by *not* generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

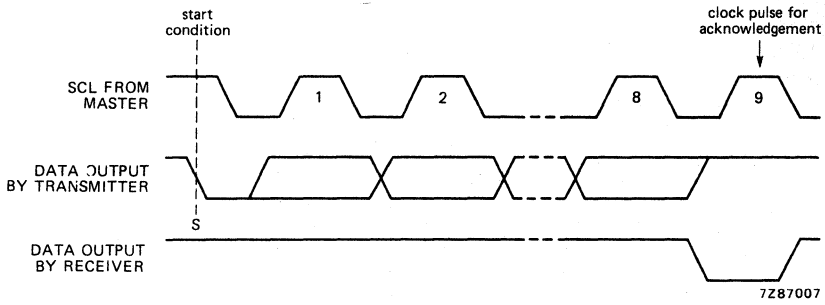


Fig. 9 Acknowledgement on the I^2C bus.

CHARACTERISTICS OF THE I²C BUS (continued)

Timing specifications

Within the I²C bus specifications a high-speed mode and a low-speed mode are defined. The ICs operate in both modes and the timing requirements are as follows:

High-speed mode

Masters generate a bus clock with a maximum frequency of 100 kHz. Detailed timing is shown in Fig. 10.

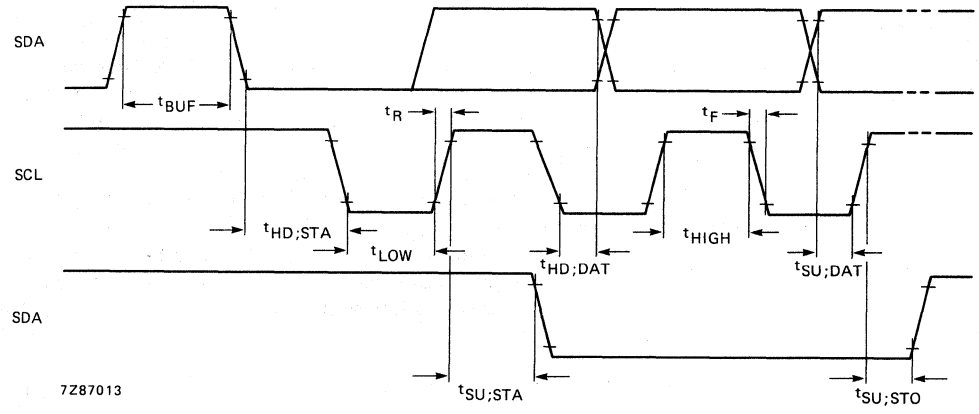


Fig. 10 Timing of the high-speed mode.

Where:

t_{BUF}	$t \geqslant t_{LOWmin}$	The minimum time the bus must be free before a new transmission can start
$t_{HD;STA}$	$t \geqslant t_{HIGHmin}$	Start condition hold time
t_{LOWmin}	4,7 μs	Clock LOW period
$t_{HIGHmin}$	4 μs	Clock HIGH period
$t_{SU;STA}$	$t \geqslant t_{LOWmin}$	Start condition set-up time, only valid for repeated start code
$t_{HD;DAT}$	$t \geqslant 0$ μs	Data hold time
$t_{SU;DAT}$	$t \geqslant 250$ ns	Data set-up time
t_R	$t \leqslant 1$ μs	Rise time of both the SDA and SCL line
t_F	$t \leqslant 300$ ns	Fall time of both the SDA and SCL line
$t_{SU;STO}$	$t \geqslant t_{LOWmin}$	Stop condition set-up time

Note

All the timing values refer to V_{IH} and V_{IL} levels with a voltage swing of V_{SS} to V_{DD}.

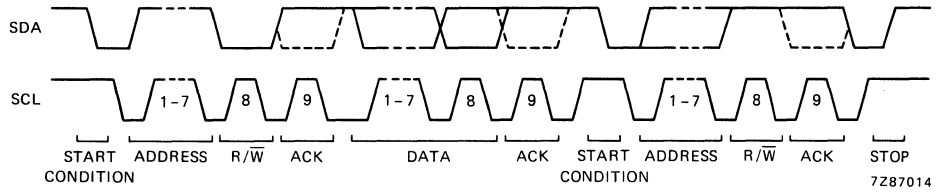


Fig. 11 Complete data transfer in the high-speed mode.

Where:

Clock t_{LOWmin}	4,7 μs
$t_{HIGHmin}$	4 μs
The dashed line is the acknowledgement of the receiver	
Mark-to-space ratio	1 : 1 (LOW-to-HIGH)
Max. number of bytes	unrestricted
Premature termination of transfer	allowed by generation of STOP condition
Acknowledge clock bit	must be provided by the master

Low-speed mode

Masters generate a bus clock with a maximum frequency of 2 kHz; a minimum LOW period of 105 μs and a minimum HIGH period of 365 μs. The mark-to-space ratio is 1 : 3 LOW-to-HIGH. Detailed timing is shown in Fig. 12.

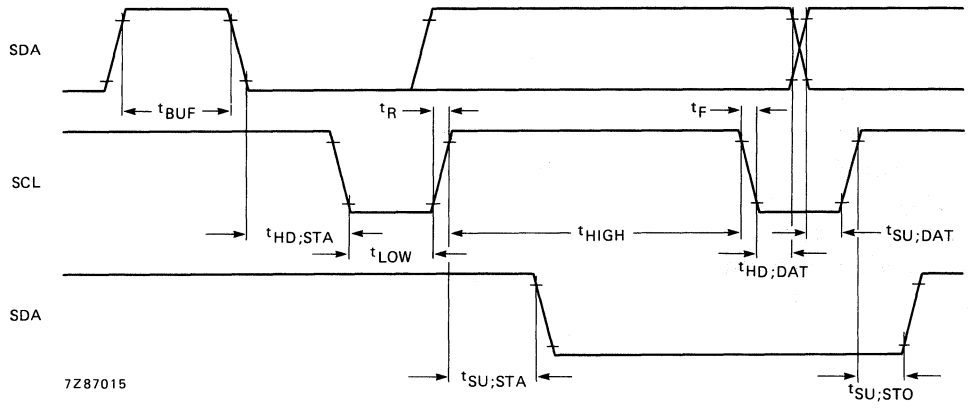


Fig. 12 Timing of the low-speed mode.

DEVELOPMENT DATA

Timing specifications (continued)

Where:

t_{BUF}	$t \geqslant 105\ \mu s$ (t_{LOWmin})
$t_{HD;STA}$	$t \geqslant 365\ \mu s$ ($t_{HIGHmin}$)
t_{LOW}	$130\ \mu s \pm 25\ \mu s$
t_{HIGH}	$390\ \mu s \pm 25\ \mu s$
$t_{SU;STA}$	$130\ \mu s \pm 25\ \mu s$ *
$t_{HD;DAT}$	$t \geqslant 0\ \mu s$
$t_{SU;DAT}$	$t \geqslant 250$ ns
t_R	$t \leqslant 1\ \mu s$
t_F	$t \leqslant 300$ ns
$t_{SU;STO}$	$130\ \mu s \pm 25\ \mu s$

Note

All the timing values refer to V_{IH} and V_{IL} levels with a voltage swing of V_{SS} to V_{DD}. For definitions see high-speed mode.

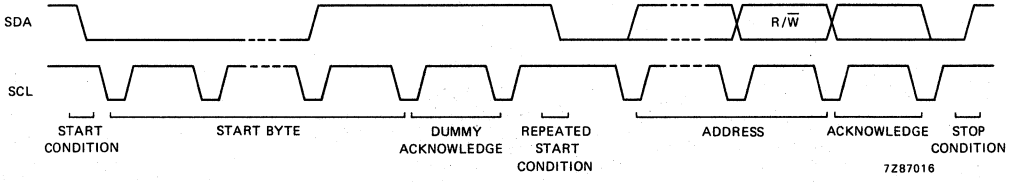


Fig. 13 Complete data transfer in the low-speed mode.

Where:

Clock t_{LOWmin}	$130\ \mu s \pm 25\ \mu s$
$t_{HIGHmin}$	$390\ \mu s \pm 25\ \mu s$
Mark-to-space ratio	1 : 3 (LOW-to-HIGH)
Start byte	0000 0001
Max. number of bytes	6
Premature termination of transfer	not allowed
Acknowledge clock bit	must be provided by master

Note

The general characteristics and detailed specification of the I^2C bus are described in a separate data sheet (serial data buses) in handbook "ICs for digital systems in radio, audio and video equipment".

* Only valid for repeated start code.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage range	V_{DD}	−0,8	+ 8,0	V
Input voltage range (any input)	V_I	−0,8	V_{DD}+0,8	V
D.C. input current (any input)	$\pm I_I$	–	10	mA
D.C. output current (any output)	$\pm I_O$	–	10	mA
Supply current	$\pm I_{DD}$; $\pm I_{SS}$	–	50	mA
Power dissipation per output	P_O	–	50	mW
Total power dissipation per package	P_{tot}	–	300	mW
Operating ambient temperature range	T_{amb}	−25	+ 70	°C
Storage temperature range	T_{stg}	−65	+ 150	°C

CHARACTERISTICS

V_{DD} = 2,5 to 6 V; V_{SS} = 0 V; crystal parameters: f_{osc} = 3,579 545 MHz, R_{Smax} = 50 Ω; T_{amb} = −25 to + 70 °C; unless otherwise specified

DEVELOPMENT DATA

parameter	symbol	min.	typ.	max.	unit
Operating supply voltage	V_{DD}	2,5	–	6,0	V
Operating supply current (note 1) oscillator ON; V_{DD} = 3 V					
no output tone	I_{DD}	–	50	100	μA
single output tone	I_{DD}	–	0,5	1,0	mA
dual output tone	I_{DD}	–	0,6	1,2	mA
Static standby current oscillator OFF; note 1	I_{DDO}	–	–	3	μA
Inputs/outputs (SDA)					
D_0 to D_5; MODE; STROBE					
Input voltage LOW	V_{IL}	0	–	0,3 x V_{DD}	V
Input voltage HIGH	V_{IH}	0,7 x V_{DD}	–	V_{DD}	V
D_2 to D_5; MODE; STROBE; A_0					
Pull-down input current $V_I = V_{DD}$	$-I_{IL}$	30	150	300	nA
SCL (D_0); SDA (D_1)					
Output current LOW (SDA) V_{OL} = 0,4 V	I_{OL}	3	–	–	mA
Clock frequency (see Fig. 10)	f_{SCL}	–	–	100	kHz
Input capacitance; $V_I = V_{SS}$	C_I	–	–	7	pF
Allowable input spike pulse width	t_I	–	–	100	ns

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
TONE output (see Fig. 14)					
DTMF output voltage levels (r.m.s. values)					
HIGH group	$V_{HG(rms)}$	158	192	205	mV
LOW group	$V_{LG(rms)}$	125	150	160	mV
D.C. voltage level	V_{DC}	–	½ V_{DD}	–	V
Pre-emphasis of group	ΔV_G	1,85	2,10	2,35	dB
Total harmonic distortion T_{amb} = 25 °C					
dual tone; note 2	THD	–	–25	–	dB
modem tone, note 3	THD	–	–29	–	dB
Output impedance	$\|Z_O\|$	–	0,1	0,5	kΩ
OSCI input					
Maximum allowable amplitude at OSCI	$V_{OSC(p-p)}$	–	–	$V_{DD}-V_{SS}$	V
Timing (V_{DD} = 3 V)					
Oscillator start-up time	$t_{OSC(ON)}$	–	3	–	ms
TONE start-up time; note 4	$t_{TONE(ON)}$	–	0,5	–	ms
STROBE pulse width; note 5	t_{STR}	400	–	–	ns
Data set-up time; note 5	t_{DS}	150	–	–	ns
Data hold time; note 5	t_{DH}	100	–	–	ns

Notes to the characteristics

1. Crystal is connected between OSCI and OSCO; D_0/SCL and D_1/SDA via a resistance of 5,6 kΩ to V_{DD}; all other pins left open.
2. Related to the level of the LOW group frequency component (CEPT CS 203).
3. Related to the level of the fundamental frequency.
4. Oscillator must be running.
5. Values are referenced to the 10% and 90% levels of the relevant pulse amplitudes, with a total voltage swing from V_{SS} to V_{DD}.

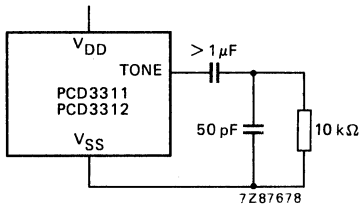


Fig. 14 TONE output test circuit.

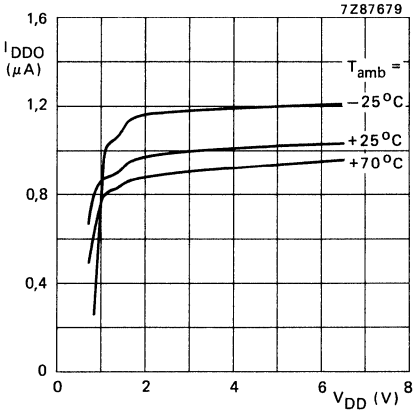


Fig. 15 Standby supply current as a function of supply voltage; oscillator OFF.

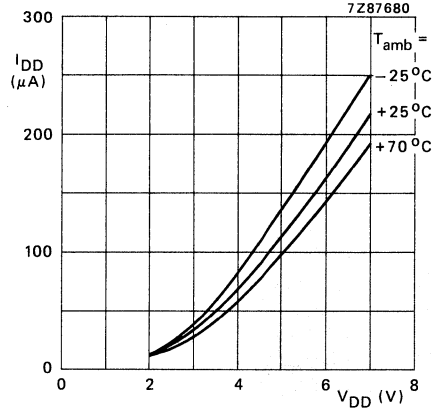


Fig. 16 Operating supply current as a function of supply voltage; oscillator ON; no output at TONE.

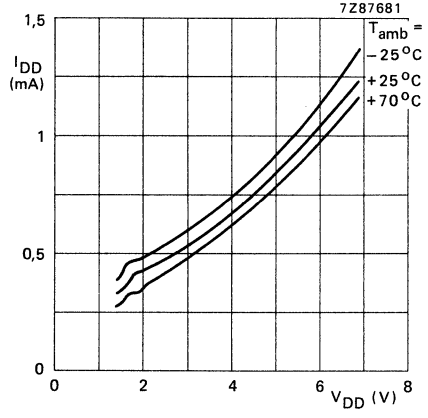


Fig. 17 Operating supply current as a function of supply voltage; oscillator ON; dual tone at TONE.

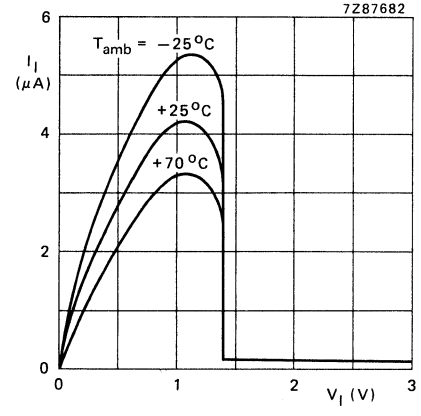


Fig. 18 Pull-down input current as a function of input voltage; V_{DD} = 3 V.

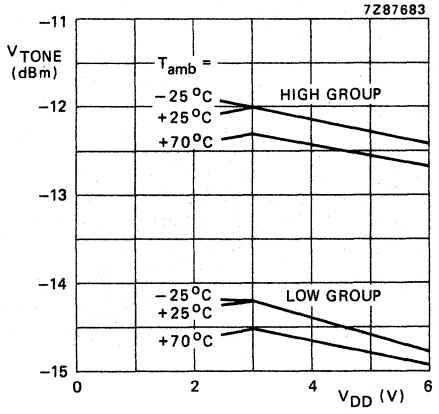


Fig. 19 DTMF output voltage levels as a function of operating supply voltage; R_L = 1 MΩ.

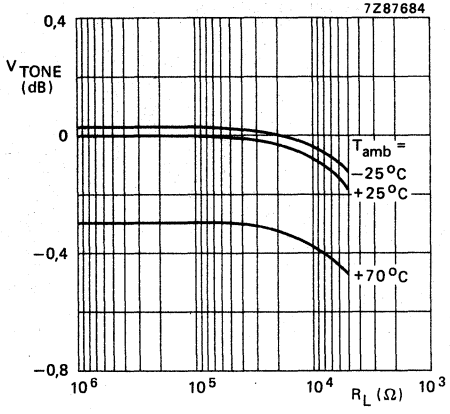


Fig. 20 Dual tone output voltage level as a function of output load resistance.

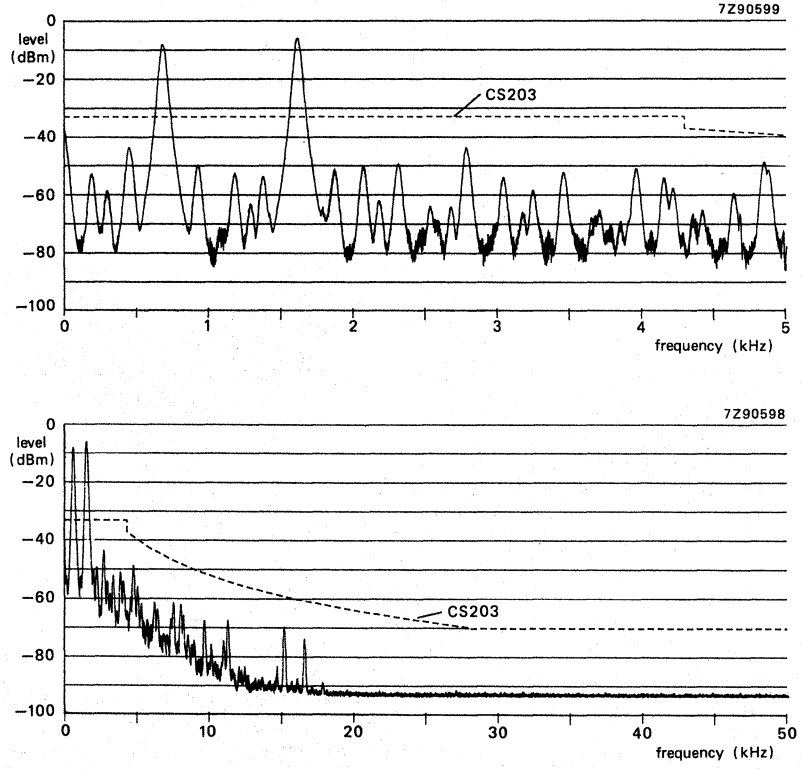


Fig. 21 Typical frequency spectrum of a dual tone signal after flat-band amplification of 6 dB.

APPLICATION INFORMATION

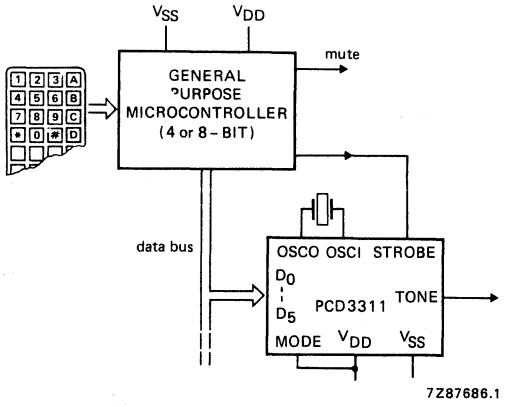


Fig. 22 PCD3311 driven by a microcontroller with parallel data-bus.

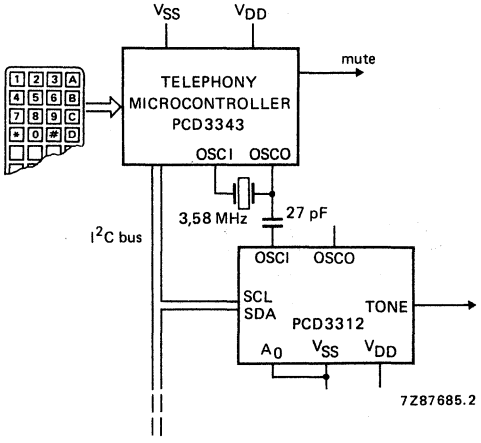


Fig. 23 PCD3312 driven by telephony microcontroller PCD3343 with serial I/O (I^2C bus).
The PCD3343 is a single-chip 8-bit microcontroller with 3K ROM/224 RAM bytes. The same application is possible with the PCD3311 with MODE = V_{SS}.

Purchase of Philips' I^2C components conveys a license under the Philips' I^2C patent to use the components in the I^2C-system provided the system conforms to the I^2C specifications defined by Philips.

CMOS REDIAL AND REPERTORY DIALLER

GENERAL DESCRIPTION

The PCD3315 is a single chip CMOS dialler IC for telephone sets. It has two dialling modes; pulse dialling (PD), and dual tone multi-frequency (DTMF) when used in conjunction with tone generator PCD3312. In addition to manual dialling it also features several automatic functions, e.g. redial, extended redial, notepad and repertory dial.

Features

- Pulse dialling
- DTMF dial control of tone generator PCD3312
- Redial
- Extended redial
- Electronic notepad
- Ten repertory dial numbers
- 18-digit capacity for each autodial memory
- Maximum of 36 digits per call
- Flash or register recall
- Uses standard 4 x 4 keyboard (single or double contact)
- Four extra function keys: program/autodial, flash, redial, access pause
- Access pause generation and termination
- Automatic recognition of PABX-digits; resulting in an access pause insertion
- Hold input and access pause output (APO) to adjust the duration of the access pause and facilitate use of tone recognizers
- Four diode or strap functions: general/German, access pause time, reset delay time, general: mark-space ratio/German: prepulse
- Manual reset of autodial RAM
- On-chip power-on reset
- Programmed for improved noise immunity

QUICK REFERENCE DATA

Operating supply voltage	V_{DD}	2,5 to 6,0	V
Standby supply voltage	V_{DDO}	min. 1	V
Operating currents at V_{DD} = 3 V			
conversation mode	I_{DD}	typ. 270	μA
dialling mode	I_{DD}	typ. 500	μA
Standby supply current at V_{DD} = 1,8 V; T_{amb} = 25 °C	I_{DD}	typ. 1,2	μA
Crystal frequency	f	3,58	MHz
Operating ambient temperature range	T_{amb}	−25 to + 70	°C

PACKAGE OUTLINES

PCD3315P: 28-lead DIL; plastic (SOT-117).
PCD3315T: 28-lead mini-pack; plastic (SO-28; SOT-136A).

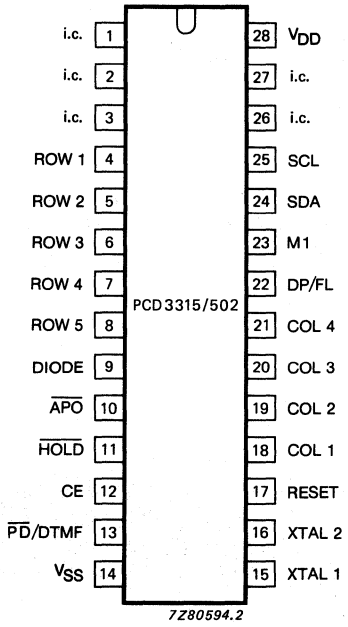


Fig. 1 Pinning diagram.

PINNING

1	i.c.	internally connected
2	i.c.	internally connected
3	i.c.	internally connected
4	ROW 1	scanning row keyboard outputs
5	ROW 2	
6	ROW 3	
7	ROW 4	
8	ROW 5	
9	DIODE	diode option output
10	$\overline{\text{APO}}$	access pause output
11	$\overline{\text{HOLD}}$	hold input
12	CE	chip enable input
13	$\overline{\text{PD}}$/DTMF	input to select pulse or DTMF dialling
14	V_{SS}	negative supply
15	XTAL 1	crystal pins
16	XTAL 2	
17	RESET	reset input/output
18	COL 1	sense column keyboard inputs
19	COL 2	
20	COL 3	
21	COL 4	
22	DP/FL	dialling pulse and flash output
23	M1	muting output
24	SDA	serial data
25	SCL	serial clock
26	i.c	internally connected
27	i.c	internally connected
28	V_{DD}	positive supply

FUNCTIONAL DESCRIPTION

Power supply (V_{DD}; V_{SS})

The minimum supply voltage and supply current depend on the operating modes:

- Standby
- Conversation
- Dialling

(see operational description)

Oscillator (XTAL 1; XTAL 2)

The timebase for the PCD3315 is a crystal-controlled oscillator with a 3,58 MHz quartz crystal connected between XTAL 1 and XTAL 2. The oscillator will run when the CE = HIGH.
The output XTAL 2 can drive the oscillator input of the PCD3312 via a capacitor.

Keyboard inputs/outputs (COL 1 to 4; ROW 1 to 5)

The sense column COL 1 to COL 4 and the scanning row outputs ROW 1 to ROW 4 are directly connected to a 4 x 4 single contact keyboard matrix. An extra row (ROW 5) is added to address four additional function keys that are required for autodial functions. The keyboard organization is shown in Fig. 2. Keyboard entries are valid 20 ms (debounce time) after the leading edge and until 20 ms after the trailing edge of the keyboard entry.
In pulse dialling mode the valid keys are the 10 numeric keys (0 to 9). The 6 non-numeric keys (A, B, C, D, *, #) have no effect on the dialling and are ignored.
In DTMF dialling mode the 10 numeric keys and the 6 non-numeric keys are valid.

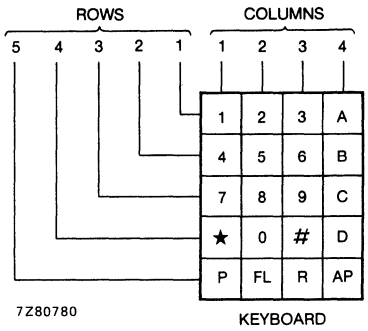


Fig. 2 Keyboard organization.

Diode option output (DIODE)

An extra row is added to the keyboard matrix to provide several selections:

- Access pause duration
- Reset delay time
- Mark/space ratio or prepulse yes/no
- General or German version

Dialling pulse and flash output (DP/FL)

This output drives the line interrupter circuit. In pulse dialling mode it controls the timing for the line interrupter. This output also provides a "Flash" pulse which generates a 95 ms line break. In the German version this "Flash" occurs only in the DTMF dialling mode.

FUNCTION DESCRIPTION (continued)

Chip enable input (CE)

The CE input is used for hook-detection.
Hook-off will result in CE = HIGH. This will change the circuit state from standby to operational mode and also initialize the circuit.
When the circuit detects a line break longer than the reset delay time, it will switch the IC to the standby mode. This essentially achieves a low standby current during hook-on.
During access pauses the reset delay time is longer because the telephone line supply is switched over, which may result in longer line drops.

Mute output (M1)

This output is active during:

- In pulse dialling mode; Mute = HIGH during interdigit pause plus dialling pulses
- In DTMF dialling mode; Mute = HIGH during DTMF bursts plus hold-over time
- During access pauses; Mute = HIGH during the mute hold-over time
- During flash; Mute = HIGH
- During programming

Hold input ($\overline{HOLD}$); access pause output ($\overline{APO}$)

The hold input suspends dialling after completion of the current digit, or in pulse dialling during the inter-digit pause.
The hold function facilitates an extra time delay during dialling under the control of external circuitry, i.e. a dialling tone recognizer.
In the hold state ($\overline{HOLD}$ = LOW) the muting output is also LOW, thus the IC is in the conversation mode.
The $\overline{HOLD}$ input can be controlled by the access pause output ($\overline{APO}$) directly, or indirectly via a dialling tone recognizer (see Fig. 3). The $\overline{APO}$ output will go LOW when an access pause is recognized.

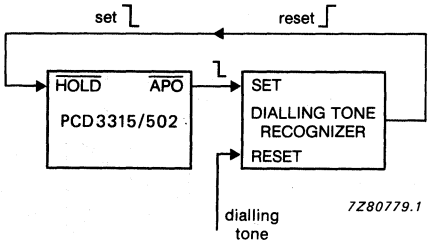


Fig. 3 Automatic variation of length of an access pause under the control of a dialling tone recognizer.

Serial data (SDA); serial clock (SCL)

The serial I/O lines SDA and SCL are used to control the PCD3312 in the DTMF dialling mode (see Fig. 5). Both outputs require external pull-up resistors.

Dialling mode selection input ($\overline{PD}$/DTMF)

This input selects the dialling mode:

- $\overline{PD}$/DTMF = LOW selects pulse dialling
- $\overline{PD}$/DTMF = HIGH selects DTMF dialling

Reset input/output (RESET)

When the reset input is active HIGH it can be used to initialize the IC.
In normal application this is achieved by the CE input.
Reset is also an output of the internal power-on-reset circuit, which generates a reset pulse if V_{DD} drops below 1,3 V (typ.).

OPERATION

The PCD3315 has 3 operating modes:

- Standby
- Conversation
- Dialling

Standby mode

When the chip enable input (CE) is LOW the IC is in the standby mode.
The oscillator is switched off and the IC requires only a low standby current (1,2 μA typ.) for memory retention.
0,5 ms after CE becomes HIGH the circuit will leave the standby mode and enter the conversation mode.

Conversation mode

In this mode the IC is active in order to scan the keyboard entries. Mute and dialling pins are inactive.
The current consumption is 270 μA (typ.) at V_{DD} = 3 V.

Dialling mode

The IC will be switched to the fully operational mode in the following circumstances:

- A valid keyboard entry
- Dialling mode
- Programming mode

The current consumption is 500 μA (typ.) at V_{DD} = 3 V.

The PCD3315 has two dialling modes:

- Pulse dialling direct via DP/FL output
- DTMF dialling via PCD3312 using the serial I/O lines SDA and SCL

Pulse dialling

The timing sequence for pulse dialling is shown in Fig. 4a.
Output DP/FL starts with an inter-digit pause, followed by a sequence of pulses corresponding with the digit for transmission. The dialling frequency is fixed at 10 Hz, the break and make times are 60 ms and 40 ms respectively.
In the general version with diode option the user can also select break and make times of 67 ms and 33 ms respectively.
The muting pulse will overlap the total dialling sequence. After dialling the muting output (M1) goes LOW and the circuit is switched to the conversation mode.

DTMF dialling

The timing sequence for DTMF dialling is shown in Fig. 4b.
The PCD3312 generates the selected DTMF tones via the serial I/O lines SDA and SCL. These tones are transmitted with minimum tone burst durations of 70,70 ms (for the German version 80,80 ms).
The maximum tone burst duration is equal to the key depression time.
After dialling the muting output goes LOW after a hold-over time of 80 ms and the circuit is switched to the conversation mode.

OPERATION (continued)

Normal dialling

The IC has a working register with a maximum capacity of 18 positions. Entries in these positions maybe:

- 10 numeric digits 0 to 9
- Manually programmed access pauses
- 6 non-numeric special keys (*, #, A, B, C, D) in DTMF mode

If none of the special keys have been pressed the contents of the working register will be stored automatically in the Redial Buffer.
The number of digits can be extended to a maximum of 36, but this will result in a redial memory clear after hook-on. This is also valid for manual dialling after automatic dialling.

Automatic dialling

In addition to manual dialling the IC provides the following automatic functions:

- Redial of the last manually dialled number (German version)
  or
  Redial of the last dialled number (general version)
- Extended redial
- Electronic notepad
- Maximum of 10 repertory dialling numbers

The maximum capacity of the registers for these numbers is also 18 positions. The 6 non-numeric digits (*, #, A, B, C, D) will not be stored.

To achieve these automatic dialling functions an extra row of the keyboard is required which contains the following special function keys:

- P programming/automatic dialling
- FL flash or register recall
- R redial
- AP manual access pause entry

Besides the operational procedure for automatic dialling, there are also procedures for programming these numbers into the memory (see Table 1).

Table 1 Keying procedures for dial and program operation

mode	operation	program
redial	R	automatic
extended redial	P • R	TN • P
notepad	P ◦ R	dial • P • P • TN ◦ P
repertory dial	P • d	$\overline{P}$ • d • TN
PABX digits	automatic	$\overline{P}$ • R • d_1 (d_2) R d_3 (d_4)
reset autodial	hook-on	
RAM	$\overline{2, 5, 8, 0}$	
	hook-off	
	2, 5, 8, 0	

Where:

P = press and release P-key
$\overline{P}$ = press and keep P-key pressed
R = press and release R-key
TN = telephone number

$\underline{d}$ = digit 0 to 9
$\overline{2, 5, 8, 0}$ = press and keep pressed keys 2, 5, 8 and 0
2, 5, 8, 0 = release keys 2, 5, 8 and 0

Access pause

During a dialling sequence it may be necessary to insert a wait time to ensure correct dialling.
A dialling sequence can always be interrupted by the $\overline{HOLD}$ input through an access pause recognition, which results in a fixed time delay.
There are 3 possibilities **to enter** an access pause:

- At manual dialling by pressing the AP key
- At auto dialling by recognition of the AP-code in the memory
- Recognition of PABX digits, after which an automatic access pause will be inserted

There are 4 possibilities **to terminate** an access pause:

- $\overline{HOLD}$, $\overline{APO}$ pins directly interconnected; after a fixed time delay of 3 or 5 seconds in pulse dialling; 1,5 or 2,5 seconds in DTMF dialling. The fixed time delay is determined by a diode strap
- $\overline{HOLD}$, $\overline{APO}$ pins interconnected via an RC network; after a fixed time delay of 3 or 5 seconds in pulse dialling; 1,5 or 2,5 seconds in DTMF dialling – plus an additional time delay determined by the RC values
- $\overline{APO}$ pin enables a dialling tone recognizer, which controls the $\overline{HOLD}$ input (see Fig. 3)
- $\overline{HOLD}$ input connected to V_{DD}; no access pause

During the access pause the muting output remains active during hold-over time. In order to handle longer line drops during access pauses, the PCD3315 automatically switches to the maximum reset delay time of 320 ms.

PABX digits

The PCD3315 will detect pre-programmed PABX digits and insert an access pause in the dialling sequence. The reserved capacity is for two different PABX numbers with a maximum of 2 digits each.

Program procedure: $\overline{P} \cdot R \cdot d_1, d_2\ R\ d_3\ d_4$.

Notepad

In the conversation mode the notepad procedure will overwrite the extended redial buffer, without dialling-out digits. After hook-off this number can be recalled through the extended redial buffer.

Store procedure : P • P • TN P
Dial : P • R

Flash (see Fig. 4b)

Flash or register recall is activated by the flash key which results in a timed line break at output pin DP/FL. This line break is of a fixed 95 ms duration in both pulse and DTMF dialling modes. In the German version it is only applicable to the DTMF mode.
In the dialling procedure a flash entry will initialize the IC and thus the working register which acts like a chip enable procedure.

Memory clear

A built-in manually total memory clear to facilitate resetting of the autodial RAM after servicing, maintenance or telephone set delivery.

Procedure: hook-on, press and keep depressed keys 2, 5, 8, 0;
hook-off, release keys 2, 5, 8, 0.

OPERATION (continued)

Program security

Security measures are incorporated in the IC to avoid incorrect dialling operations and hang-ups. The program has a built-in RAM check procedure to protect the autodial numbers stored in the RAM. If one or more bits of this RAM are changed during standby or the battery falls below 1,3 V (typ.), this will result in a memory clear to avoid subsequent incorrect dialling.

Diode options

There are 4 different diode or strap options which are an extension of the keyboard matrix. Addressing is via the 4 colums and diode pins.
There are two possibilities:

- Without diode
- With diode (cathode on row-side)

The built-in selections are shown in Table 2.

Table 2 Diode option selections

column	description	without diode	with diode	remarks
4	version	German	general	–
1	break, make-time	60,40 ms	67,33 ms	general version
1	prepulse	no	yes	German version
2	access pause	3 s	5 s	pulse dialling
2	access pause	1,5 s	2,5 s	DTMF dialling
3	reset delay time	160 ms	320 ms	–

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 28)	V_{DD}		−0,8 to + 8	V
All input voltages	V_I		0,8 to V_{DD} + 0,8	V
D.C. current into any input of output	$\pm I_I, \pm I_O$	max.	10	mA
Total power dissipation (see note)	P_{tot}	max.	500	mW
Power dissipation per output	P_O	max.	50	mW
Storage temperature range	T_{stg}		−65 to + 150	°C
Operating ambient temperature range	T_{amb}		−25 to + 70	°C
Operating junction temperature	T_j	max.	125	°C

Note

Thermal resistance (junction to ambient)				
for SOT-117	$R_{th\ j\text{-}a}$	max.	120	K/W
for SOT-136A	$R_{th\ j\text{-}a}$	max.	150	K/W

D.C. CHARACTERISTICS

V_{DD} = 2,5 to 6 V; V_{SS} = 0 V; T_{amb} = −25 to + 70 °C; all voltages with respect to V_{SS}; f = 3,58 MHz with R_S = 50 Ω; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply voltage					
operating	V_{DD}	2,5	–	6	V
STOP mode for RAM retention	V_{DD}	1,0**	–	6	V
Supply current					
dialling mode					
at V_{DD} = 3 V	I_{DD}	–	500	–	μA
conversation mode					
at V_{DD} = 3 V	I_{DD}	–	270	–	μA
STOP mode*					
at V_{DD} = 1,8 V; T_{amb} = 25 °C	I_{DD}	–	1,2	2,5	μA
at V_{DD} = 1,8 V; T_{amb} = 55 °C	I_{DD}	–	–	5	μA
at V_{DD} = 1,8 V; T_{amb} = 70 °C	I_{DD}	–	–	10	μA
RESET I/O					
Switching level	V_{RESET}	–	1,2	1,5	V
Sink current					
at $V_{DD} > V_{RESET}$	I_{OL}	–	7	–	μA
Inputs					
Input voltage LOW	V_{IL}	0	–	$0{,}3V_{DD}$	V
Input voltage HIGH	V_{IH}	$0{,}7V_{DD}$	–	V_{DD}	V
Input leakage current					
at $V_{SS} < V_I < V_{DD}$	$\pm I_{IL}$	–	–	1	μA
Outputs					
Output voltage LOW					
at $V_I = V_{SS}$ or V_{DD}; $\lvert I_O \rvert < 1$ μA	V_{OL}	–	–	0,05	V
Output sink current LOW					
at V_{DD} = 3 V; V_O = 0,4 V	I_{OL}	0,6	1,5	–	mA
Pull-up output source current HIGH (except SDA, SCL)					
at V_{DD} = 3 V; $V_O = 0{,}9V_{DD}$	$-I_{OH}$	10	–	–	μA
at V_{DD} = 3 V; $V_O = V_{SS}$	$-I_{OH}$	–	–	200	μA

* Crystal connected between XTAL 1 and XTAL 2; SCL and SDA pulled to V_{DD} via 5,6 kΩ resistor; CE and $\overline{PD}$/DTMF at V_{SS}.

** Because RAM is cleared if POR is activated by software, this value must be max. V_{RESET}.

Table 3 Timing date, general version

parameter	symbol	min.	typ.		unit
			*	**	
Reset delay time	t_{rds}	–	160	320	ms
Reset delay time during access pause	t_{rds}	–	320	320	ms
Keyboard debounce time	t_{db}	–	20	20	ms
Flash time	t_{fl}	–	95	95	ms
Pulse dialling					
Dial frequency	f_d	–	10	10	Hz
Break/make time	$t_{b/m}$	–	60,40	67,33	ms
Interdigit pause	t_{idp}	–	840	840	ms
Access pause	t_{ap}	–	3	5	s
Mute hold-over time ▲	t_h	–	1	1	s
DTMF dialling					
Tone transmission time	t_t	70 or key-down time			ms
Tone pause time	t_p	70	–	–	ms
Mute hold-over time during dialling	t_h	–	150	150	ms
Mute hold-over time during access pause	t_h	–	1	1	s
Access pause	t_{ap}	–	1,5	2,5	s

Table 4 Timing data, German version

parameter	symbol	min.	typ.		unit
			*	**	
Reset delay time	t_{rds}	–	160	320	ms
Reset delay time during access pause	t_{rds}	–	320	320	ms
Keyboard debounce time	t_{db}	–	20	20	ms
Pulse dialling					
Dial frequency	f_d	–	10	10	Hz
Break/make time	$t_{b/m}$	–	60,40	60,40	ms
Interdigit pause	t_{idp}	–	840	840	ms
Access pause	t_{ap}	–	3	5	s
Mute hold-over time ▲	t_h	–	1	3	s
Prepulse time	t_{pp}	–	–	20	ms
DTMF dialling					
Tone transmission time	t_t	80 or key-down time			ms
Tone pause time	t_p	80	–	–	ms
Mute hold-over time during dialling	t_h	–	160	160	ms
Mute hold-over time during access pause	t_h	–	1	1	s
Access pause	t_{ap}	–	1,5	2,5	s
Flash time	t_{fl}	–	95	95	ms

* Without diode.
** With diode.
▲ Only during access pause.

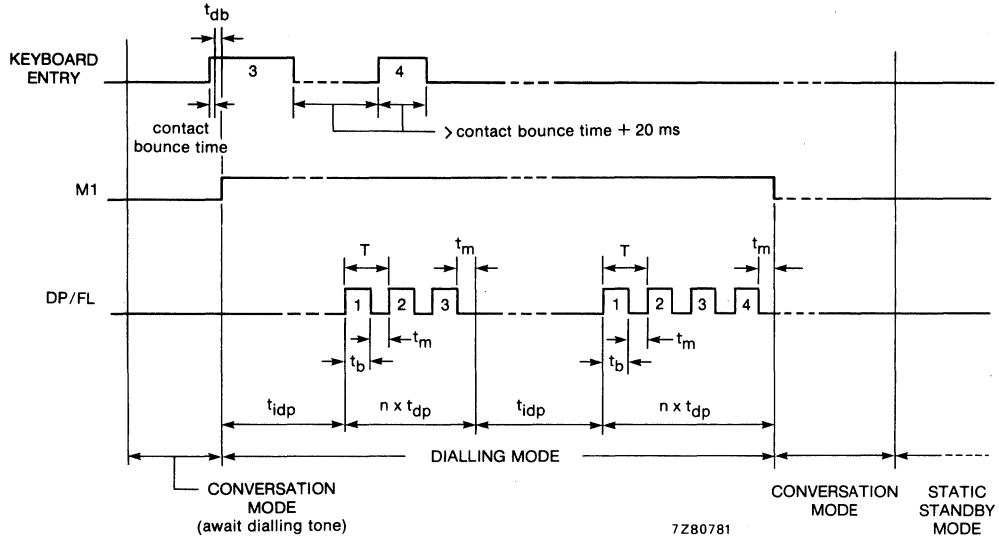


Fig. 4a Timing diagram for pulse dialling mode, defined by $\overline{PD}$/DTMF = LOW (V_{SS}).

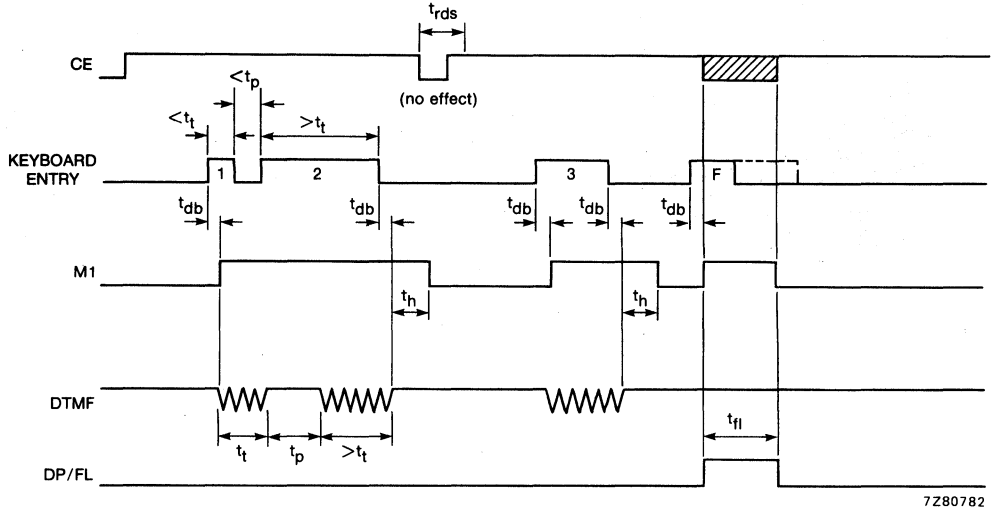


Fig. 4b Timing diagram for DTMF dialling mode, defined by $\overline{PD}$/DTMF = HIGH (V_{DD}).

APPLICATION INFORMATION

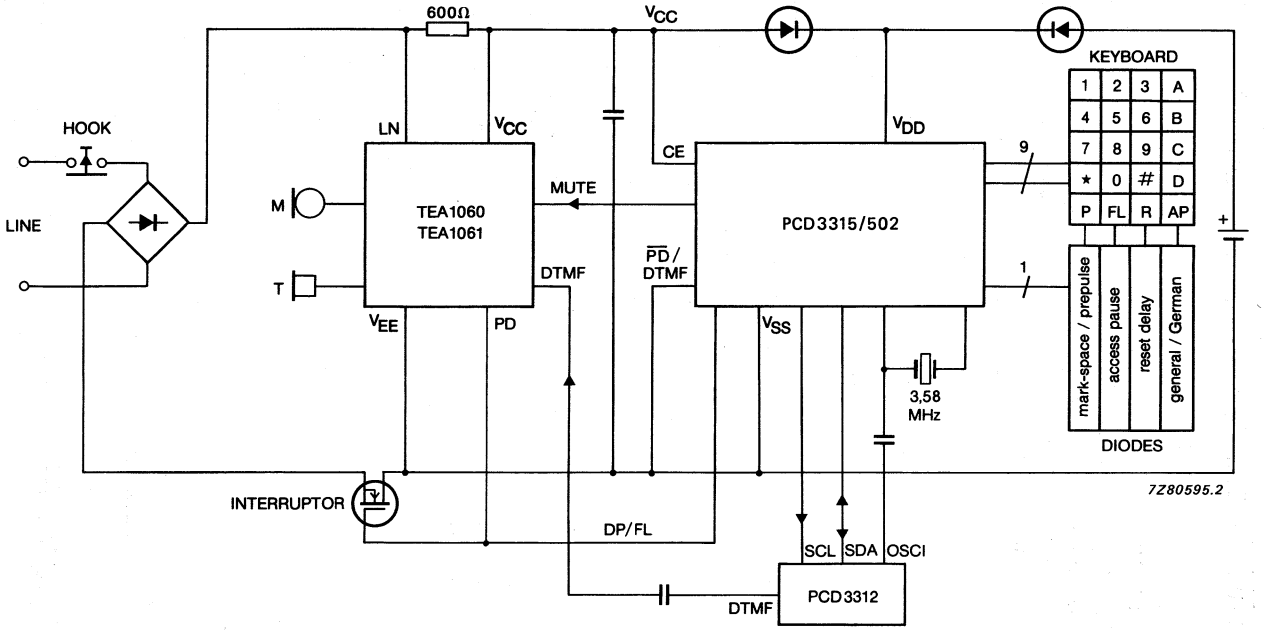


Fig. 5 Block diagram of feature phone.

CMOS REDIAL AND REPERTORY DIALLER

GENERAL DESCRIPTION

The PCD3315/503 is a single chip CMOS dialler IC for telephone sets. It has two dialling modes; pulse dialling (PD), and dual tone multi-frequency (DTMF) when used in conjunction with tone generator PCD3312. In addition to manual dialling it also features several automatic functions, e.g. redial, extended redial, notepad and repertory dial.

Features

- Pulse dialling
- DTMF dial control of tone generator PCD3312
- Redial
- Extended redial
- Electronic notepad
- Ten repertory dial numbers
- Successsive dial and autodial procedures during a single call
- 18-digit capacity for each autodial memory
- Number of digits per call is infinite (FIFO register)
- Flash or register recall
- Uses standard 4 x 4 keyboard (single or double contact)
- Four extra function keys: program/autodial, flash, redial, access pause
- Keyboard expansion is possible to accomodate the 10 repertory dialling numbers
- Access pause generation and termination.
- Automatic recognition of PABX-digits; resulting in an access pause insertion
- Hold input and access pause output (APO) to adjust the duration of the access pause and facilitate use of tone recognizers
- Four diode or strap functions: mark-space ratio, FLASH time, access pause time and tone bursts time
- Manual reset of autodial RAM
- On-chip power-on reset
- Programmed for improved noise immunity

QUICK REFERENCE DATA

Operating supply voltage	V_{DD}	2,5 to 6,0	V
Standby supply voltage	V_{DDO}	min. 1	V
Operating currents at V_{DD} = 3 V			
conversation mode	I_{DD}	typ. 270	μA
dialling mode	I_{DD}	typ. 500	μA
Standby supply current at V_{DD} = 1,8 V; T_{amb} = 25 °C	I_{DD}	typ. 1,2	μA
Crystal frequency	f	3,58	MHz
Operating ambient temperature range	T_{amb}	−25 to +70	°C

PACKAGE OUTLINES

PCD3315P: 28-lead DIL; plastic (SOT-117).
PCD3315T: 28-lead mini-pack; plastic (SO-28; SOT-136A).

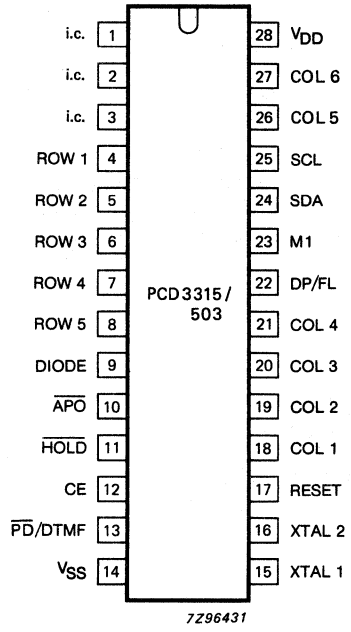


Fig. 1 Pinning diagram.

PINNING

1	i.c.	internally connected
2	i.c.	internally connected
3	i.c.	internally connected
4	ROW 1	scanning row keyboard outputs
5	ROW 2	
6	ROW 3	
7	ROW 4	
8	ROW 5	
9	DIODE	diode option output
10	$\overline{\text{APO}}$	access pause output
11	$\overline{\text{HOLD}}$	hold input
12	CE	chip enable input
13	$\overline{\text{PD}}$/DTMF	input to select pulse or DTMF dialling
14	V_{SS}	negative supply
15	XTAL 1	crystal pins
16	XTAL 2	
17	RESET	reset input/output
18	COL 1	sense column keyboard inputs
19	COL 2	
20	COL 3	
21	COL 4	
22	DP/FL	dialling pulse and flash output
23	M1	muting output
24	SDA	serial data
25	SCL	serial clock
26	COL 5	sense column keyboard inputs
27	COL 6	
28	V_{DD}	positive supply

FUNCTIONAL DESCRIPTION

Power supply (V_{DD}; V_{SS})

The minimum supply voltage and supply current depend on the operating modes:

- Standby
- Conversation
- Dialling

(see operational description)

Oscillator (XTAL 1; XTAL 2)

The timebase for the PCD3315/503 is a crystal-controlled oscillator with a 3,58 MHz quartz crystal connected between XTAL 1 and XTAL 2. The oscillator will run when the CE = HIGH.
The output XTAL 2 can drive the oscillator input of the PCD3312 via a capacitor.

Keyboard inputs/outputs (COL 1 to 6; ROW 1 to 5)

The sense column COL 1 to COL 4 and the scanning row outputs ROW 1 to ROW 4 are directly connected to a 4 x 4 single contact keyboard matrix. An extra row (ROW 5) is added to address four additional function keys that are required for autodial functions.
Repertory dialler extension (ROW 1 to ROW 5/COL 5 and COL 6): 10 extra keys to access by single button repertory numbers (on-chip RAM). The keyboard organization is shown in Fig. 2. Keyboard entries are valid 20 ms (debounce time) after the leading edge and until 20 ms after the trailing edge of the keyboard entry.
In pulse dialling mode the valid keys are the 10 numeric keys (0 to 9). The 6 non-numeric keys (A, B, C, D, *, #) have no effect on the dialling and are ignored.
In DTMF dialling mode the 10 numeric keys and the 6 non-numeric keys are valid.

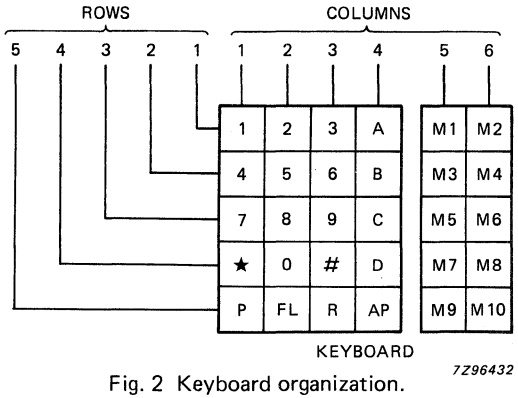


Fig. 2 Keyboard organization.

Diode option output (DIODE)

An extra row is added to the keyboard matrix to provide several selections:

- Access pause duration
- "Flash" time selection
- Mark/space ratio
- Tone burst time selection

Dialling pulse and flash output (DP/FL)

This output drives the line interrupter circuit. In pulse dialling mode it controls the timing for the line interrupter. This output also provides a "Flash" pulse which generates a 95/650 ms line break, selected via a diode option.

FUNCTION DESCRIPTION (continued)

Chip enable input (CE)

The CE input is used for hook-detection.
Hook-off will result in CE = HIGH. This will change the circuit state from standby to operational mode and also initialize the circuit.
When the circuit detects a line break longer than the reset delay time, it will switch the IC to the standby mode. This essentially achieves a low standby current during hook-on.
During access pauses the reset delay time is longer because the telephone line supply is switched over, which may result in longer line drops.

Mute output (M1)

This output is active:

- In pulse dialling mode; Mute = HIGH during inter-digit pause plus dialling pulses
- In DTMF dialling mode; Mute = HIGH during DTMF bursts plus hold-over time
- During access pauses; Mute = HIGH during the mute hold-over time
- During flash; Mute = HIGH
- During programming.

Hold input ($\overline{\text{HOLD}}$); **access pause output** ($\overline{\text{APO}}$)

The hold input suspends dialling after completion of the current digit, or in pulse dialling during the inter-digit pause.
The hold function facilitates an extra time delay during dialling under the control of external circuitry, i.e. a dialling tone recognizer.
In the hold state ($\overline{\text{HOLD}}$ = LOW) the muting output is also LOW, thus the IC is in the conversation mode.
The $\overline{\text{HOLD}}$ input can be controlled by the access pause output ($\overline{\text{APO}}$) directly, or indirectly via a dialling tone recognizer (see Fig. 3). The $\overline{\text{APO}}$ output will go LOW when an access pause is recognized.

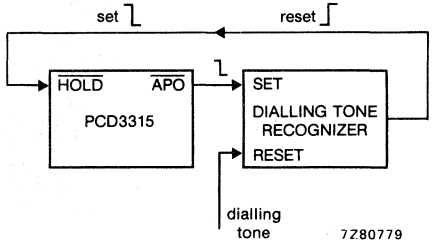


Fig. 3 Automatic variation of length of an access pause under the control of a dialling tone recognizer.

Serial data (SDA); **serial clock** (SCL)

The serial I/O lines SDA and SCL are used to control the PCD3312 in the DTMF dialling mode (see Fig. 5). Both outputs require external pull-up resistors.

Dialling mode selection input ($\overline{\text{PD}}$/DTMF)

This input selects the dialling mode:

- $\overline{\text{PD}}$/DTMF = LOW selects pulse dialling
- $\overline{\text{PD}}$/DTMF = HIGH selects DTMF dialling

Reset input/output (RESET)

When the reset input is active HIGH it can be used to initialize the IC.
In normal application this is achieved by the CE input.
Reset is also an output of the internal power-on-reset circuit, which generates a reset pulse if V_{DD} drops below 1,3 V (typ.).

OPERATION

The PCD3315/503 has 3 operating modes:

- Standby
- Conversation
- Dialling

Standby mode

When the chip enable input (CE) is LOW the IC is in the standby mode.
The oscillator is switched off and the IC requires only a low standby current (1,2 μA typ.) for memory retention.
0,5 ms after CE becomes HIGH the circuit will leave the standby mode and enter the conversation mode.

Conversation mode

In this mode the IC is active in order to scan the keyboard entries. Mute and dialling pins are inactive.
The current consumption is 270 μA (typ.) at V_{DD} = 3 V.

Dialling mode

The IC will be switched to the fully operational mode in the following circumstances:

- A valid keyboard entry
- Dialling mode
- Programming mode

The current consumtion is 500 μA (typ.) at V_{DD} = 3 V.

The PCD3315/503 has two dialling modes:

- Pulse dialling direct via DP/FL output
- DTMF dialling via PCD3312 using the serial I/O lines SDA and SCL

Pulse dialling

The timing sequence for pulse dialling is shown in Fig. 4a.
Output DP/FL starts with an inter-digit pause, followed by a sequence of pulses corresponding with the digit for transmission. The dialling frequency is fixed at 10 Hz, the break and make times are 60 ms and 40 ms respectively.
With diode option the user can also select break and make times of 67 ms and 33 ms respectively.
The muting pulse will overlap the total dialling sequence. After dialling the muting output (M1) goes LOW and the circuit is switched to the conversation mode.

DTMF dialling

The timing sequence for DTMF dialling is shown in Fig. 4b.
The PCD3312 generates the selected DTMF tones via the serial I/O lines SDA and SCL. These tones are transmitted with minimum tone burst durations of 70,70 ms or 100,100 ms with diode option.
The maximum tone burst duration is equal to the key depression time.
After dialling the muting output goes LOW after a hold-over time of 80 ms and the circuit is switched to the conversation mode.

OPERATION

Normal dialling

The IC has a working register with a maximum capacity of 18 positions. Entries in these positions maybe:

- 10 numeric digits 0 to 9
- Manually programmed access pauses
- 6 non-numeric special keys (*, #, A, B, C, D) in DTMF mode

If none of the special keys have been pressed the contents of the working register will be stored automatically in the Redial Buffer.
The number of digits can be extended but this will result in a redial memory clear after hook-on.
Up to 18 digits can be stored in the redial register. After the main store overflows, a 10-digit First-in First-out (FIFO) register takes over as buffer. After transmitting the first digit of the FIFO register this place is automatically cleared and new data can be stored there. In this way an unlimited number can be transmitted if the key-in rate is not too fast. However if this FIFO register also overflows (more than 10 digits in store) further input will be ignored.
This is also valid for manual dialling after automatic dialling.

Automatic dialling

In addition to manual dialling the IC provides the following automatic functions:

- Redial of the last dialled number
- Extended redial
- Electronic notepad
- Maximum of 10 repertory dialling numbers

The maximum capacity of the registers for these numbers is also 18 positions. The 6 non-numeric digits (*, #, A, B, C, D) will not be stored.

To achieve these automatic dialling functions an extra row of the keyboard is required which contains the following special function keys:

- P programming/automatic dialling
- FL flash or register recall
- R redial
- AL manual access pause entry

Besides the operational procedure for automatic dialling, there are also procedures for programming these numbers into the memory (see Table 1).

Table 1 Keying procedures for dial and program operation

mode	operation	program
redial	R	automatic
extended redial	P · R	TN · P
notepad	P · R	$\underline{\text{dial}}$ · P · P · TN · P
repertory dial	P · d	$\overline{\text{P}}$ · d · TN
or	M	$\overline{\text{P}}$ · M · TN
PABX digits	automatic	$\overline{\text{P}}$ · R · d_1 (d_2) R d_3 (d_4)
reset autodial	$\underline{\text{hook-on}}$	
RAM	$\overline{2, 5, 8, 0}$	
	hook-off	
	2, 5, 8, 0	

Where:

P = press and release P-key
$\overline{\text{P}}$ = press and keep P-key pressed
R = press and release R-key
TN = telephone number
$\underline{\text{d}}$ = digit 0 to 9
$\overline{2, 5, 8, 0}$ = press and keep pressed keys 2, 5, 8 and 0
2, 5, 8, 0 = release keys 2, 5, 8 and 0
M = press and release M-key

DEVELOPMENT DATA

Successive repertory dialling during a call

It is possible to dial more than one repertory number during one single telephone call using the following procedures:

- Redial, extended redial or a repertory number followed by new digits
- Repertory number followed by one or more repertory numbers
- Normal dial, redial or extended redial followed by one or more repertory numbers

Repertory button dialling via extended keyboard

The PCD3315/503 has the facility to store 10 repertory numbers, activated by the P-button with a number key or by using direct button action. Then the stored numbers can be re-called by pressing one of the 10 name buttons. The keyboard extension is connected via pins 26 and 27.

OPERATION (continued)

Access pause

During a dialling sequence it may be necessary to insert a wait time to ensure correct dialling.
A dialling sequence can always be interrupted by the $\overline{\text{HOLD}}$ input through an access pause recognition, which results in a fixed time delay.
There are 3 possibilities **to enter** an access pause:

- At manual dialling by pressing the AP key
- At auto dialling by recognition of the AP-code in the memory
- Recognition of PABX digits, after which an automatic access pause will be inserted

There are 4 possibilities **to terminate** an access pause:

- $\overline{\text{HOLD}}$, $\overline{\text{APO}}$ pins directly interconnected; after a fixed time delay of 3 or 5 seconds in pulse dialling; 1,5 or 2,5 seconds in DTMF dialling. The fixed time delay is determined by a diode strap
- $\overline{\text{HOLD}}$, $\overline{\text{APO}}$ pins interconnected via an RC network; after a fixed time delay of 3 or 5 seconds in pulse dialling; 1,5 or 2,5 seconds in DTMF dialling – plus an additional time delay determined by the RC values
- $\overline{\text{APO}}$ pin enables a dialling tone recognizer, which controls the $\overline{\text{HOLD}}$ input (see Fig. 3)
- $\overline{\text{HOLD}}$ input connected to V_{DD}; no access pause

During the access pause the muting output remains active during hold-over time. In order to handle longer line drops during access pauses, the PCD3315 automatically switches to the maximum reset delay time of 320 ms.

PABX digits

The PCD3315/503 will detect pre-programmed PABX digits and insert an access pause in the dialling sequence. The reserved capacity is for two different PABX numbers with a maximum of 2 digits each.

Program procedure: $\overline{P} \cdot R \cdot d_1, d_2\ R\ d_3\ d_4$.

Notepad

In the conversation mode the notepad procedure will overwrite the extended redial buffer, without dialling-out digits. After hook-off this number can be recalled through the extended redial buffer.

Store procedure : $P \cdot P \cdot \overline{TN}\ P$
Dial : $P \cdot R$

Flash (see Fig. 4b)

Flash or register recall is activated by the flash key which results in a timed line break at output pin DP/FL. This line break is of a fixed 95 or 650 ms duration in both pulse and DTMF dialling modes. In the dialling procedure a flash entry will initialize the IC and thus the working register which acts like a chip enable procedure.

Memory clear

A built-in manually total memory clear to facilitate resetting of the autodial RAM after servicing, maintenance or telephone set delivery.

Procedure: hook-on, press and keep depressed keys 2, 5, 8, 0;
hook-off, release keys 2, 5, 8, 0.

Program security

Security measures are incorporated in the IC to avoid incorrect dialling operations and hang-ups. The program has a built-in RAM check procedure to protect the autodial numbers stored in the RAM. If one or more bits of this RAM are changed during standby or the battery falls below 1,3 V (typ.), this will result in a memory clear to avoid subsequent incorrect dialling.

Diode options

There are 4 different diode or strap options which are an extension of the keyboard matrix. Addressing is via the 4 columns and diode pins.
There are two possibilities:

- Without diode
- With diode (cathode on row-side)

The built-in selections are shown in Table 2.

Table 2 Diode option selections

column	description	without diode	with diode	remarks
4	tone burst	100,100 ms	70,70 ms	–
1	break, make-time	60,40 ms	67,33 ms	–
2	access pause	3 s	5 s	pulse dialling
2	access pause	1,5 s	2,5 s	DTMF dialling
3	flash time	95 ms	650 ms	–

DEVELOPMENT DATA

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 28)	V_{DD}		−0,8 to + 8	V
All input voltages	V_I		0,8 to V_{DD} + 0,8	V
D.C. current into any input of output	$\pm I_I, \pm I_O$	max.	10	mA
Total power dissipation (see note)	P_{tot}	max.	500	mW
Power dissipation per output	P_O	max.	50	mW
Storage temperature range	T_{stg}		−65 to + 150	°C
Operating ambient temperature range	T_{amb}		−25 to + 70	°C
Operating junction temperature	T_j	max.	125	°C

Note

Thermal resistance (junction to ambient)

for SOT-117	$R_{th\ j\text{-}a}$	max.	120	K/W
for SOT-136A	$R_{th\ j\text{-}a}$	max.	150	K/W

D.C. CHARACTERISTICS

V_{DD} = 2,5 to 6 V; V_{SS} = 0 V; T_{amb} = −25 to + 70 °C; all voltages with respect to V_{SS}; f = 3,58 MHz with R_S = 50 Ω; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply voltage					
operating	V_{DD}	2,5	–	6	V
STOP mode for RAM retention	V_{DD}	1,0**	–	6	V
Supply current					
dialling mode					
at V_{DD} = 3 V	I_{DD}	–	500	–	μA
conversation mode					
at V_{DD} = 3 V	I_{DD}	–	270	–	μA
STOP mode*					
at V_{DD} = 1,8 V; T_{amb} = 25 °C	I_{DD}	–	1,2	2,5	μA
at V_{DD} = 1,8 V; T_{amb} = 55 °C	I_{DD}	–	–	5	μA
at V_{DD} = 1,8 V; T_{amb} = 70 °C	I_{DD}	–	–	10	μA
RESET I/O					
Switching level	V_{RESET}	–	1,2	1,5	V
Sink current					
at $V_{DD} > V_{RESET}$	I_{OL}	–	7	–	μA
Inputs					
Input voltage LOW	V_{IL}	0	–	$0{,}3V_{DD}$	V
Input voltage HIGH	V_{IH}	$0{,}7V_{DD}$	–	V_{DD}	V
Input leakage current					
at $V_{SS} < V_I < V_{DD}$	$\pm I_{IL}$	–	–	1	μA
Outputs					
Output voltage LOW					
at $V_I = V_{SS}$ or V_{DD}; $\|I_O\| < 1$ μA	V_{OL}	–	–	0,05	V
Output sink current LOW					
at V_{DD} = 3 V; V_O = 0,4 V	I_{OL}	0,6	1,5	–	mA
Pull-up output source current HIGH (except SDA, SCL)					
at V_{DD} = 3 V; $V_O = 0{,}9V_{DD}$	$-I_{OH}$	10	–	–	μA
at V_{DD} = 3 V; $V_O = V_{SS}$	$-I_{OH}$	–	–	200	μA

* Crystal connected between XTAL 1 and XTAL 2; SCL and SDA pulled to V_{DD} via 5,6 kΩ resistor; CE and $\overline{PD}$/DTMF at V_{SS}.

** Because RAM is cleared if POR is activated by software, this value must be max. V_{RESET}.

Table 3 Timing data

parameter	symbol	typ.		unit
		without diode	with diode	
Reset delay time	t_{rds}	160	160	ms
Reset delay time during access pause	t_{rds}	320	320	ms
Keyboard debounce time	t_{db}	20	20	ms
Flash time	t_{fl}	95	650	ms
Pulse dialling				
Dial frequency	f_d	10	10	Hz
Break/make time	$t_{b/m}$	60,40	67,33	ms
Interdigit pause	t_{idp}	840	840	ms
Access pause	t_{ap}	3	5	s
Mute hold-over time ▲	t_h	1	1	s
DTMF dialling				
Tone transmission time	t_t	min. 100 or key-down time	min. 70 or key-down time	ms
Tone pause time	t_p	min. 100	min. 70	ms
Mute hold-over time during dialling	t_h	$80 + t_p$	$80 + t_p$	ms
Mute hold-over time during access pause	t_h	1	1	s
Access pause	t_{ap}	1,5	2,5	s

DEVELOPMENT DATA

▲ Only during access pause.

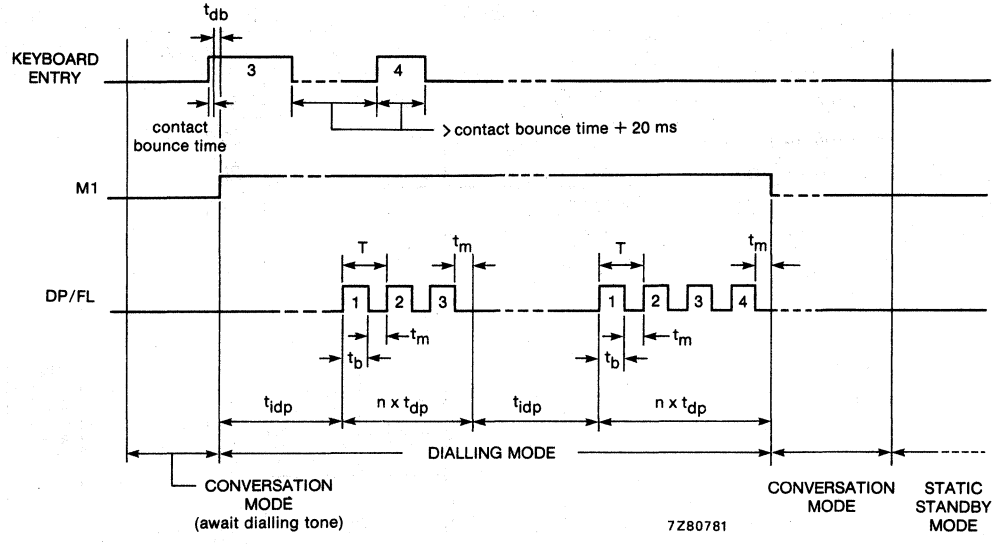


Fig. 4a Timing diagram for pulse dialling mode, defined by $\overline{PD}$/DTMF = LOW (V_{SS}).

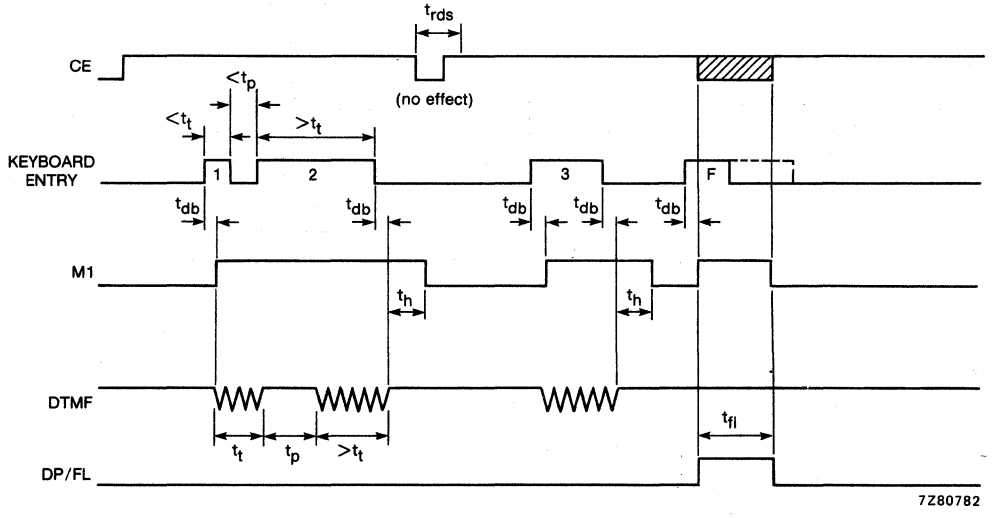


Fig. 4b Timing diagram for DTMF dialling mode, defined by $\overline{PD}$/DTMF = HIGH (V_{DD}).

APPLICATION INFORMATION

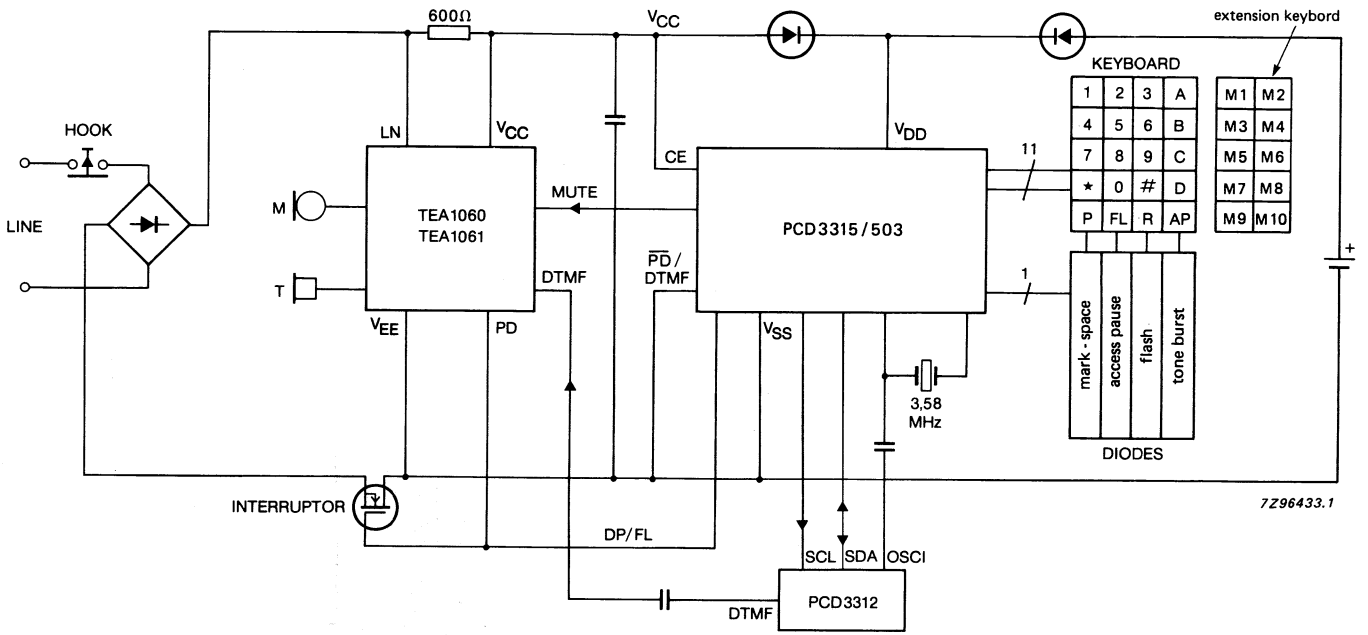


Fig. 5 Block diagram of feature phone.

CMOS MICROCONTROLLER FOR TELEPHONE SETS

GENERAL DESCRIPTION

The PCD3315C is a single-chip 8-bit microcontroller fabricated in CMOS and is a member of the PCD3343 family. It has special on-chip features for application in telephone sets.

Features

- 8-bit CPU, ROM, RAM, I/O in a single 28-lead DIL or SO package
- 1536 ROM bytes
- 160 RAM bytes
- 20 quasi-bidirectional I/O port lines
- Two test inputs: one of which is also the external interrupt input (CE/$\overline{T0}$)
- Single-level vectored interrupts: external, timer/event counter
- 8-bit programmable timer/event counter
- Over 80 instructions (based on MAB8048, MAB8400, PCD3343 and PCF8500)
- All instructions 1 or 2 cycles
- Clock frequency 100 kHz to 10 MHz
- Single supply voltage from 1,8 V to 6 V
- Low standby voltage and current
- STOP and IDLE mode
- On-chip oscillator with output drive capability for peripherals
- Configuration of all I/O port lines individually selected by mask: pull-up, open drain or push-pull
- Power-on-reset circuit and low supply voltage detection
- Reset state of all ports individually selected by mask
- Operating temperature range: −25 to + 70 °C

PACKAGE OUTLINES

PCD3315CP: 28-lead DIL; plastic (SOT-117).
PCD3315CT: 28-lead mini-pack; plastic (SO-28; SOT-136A).

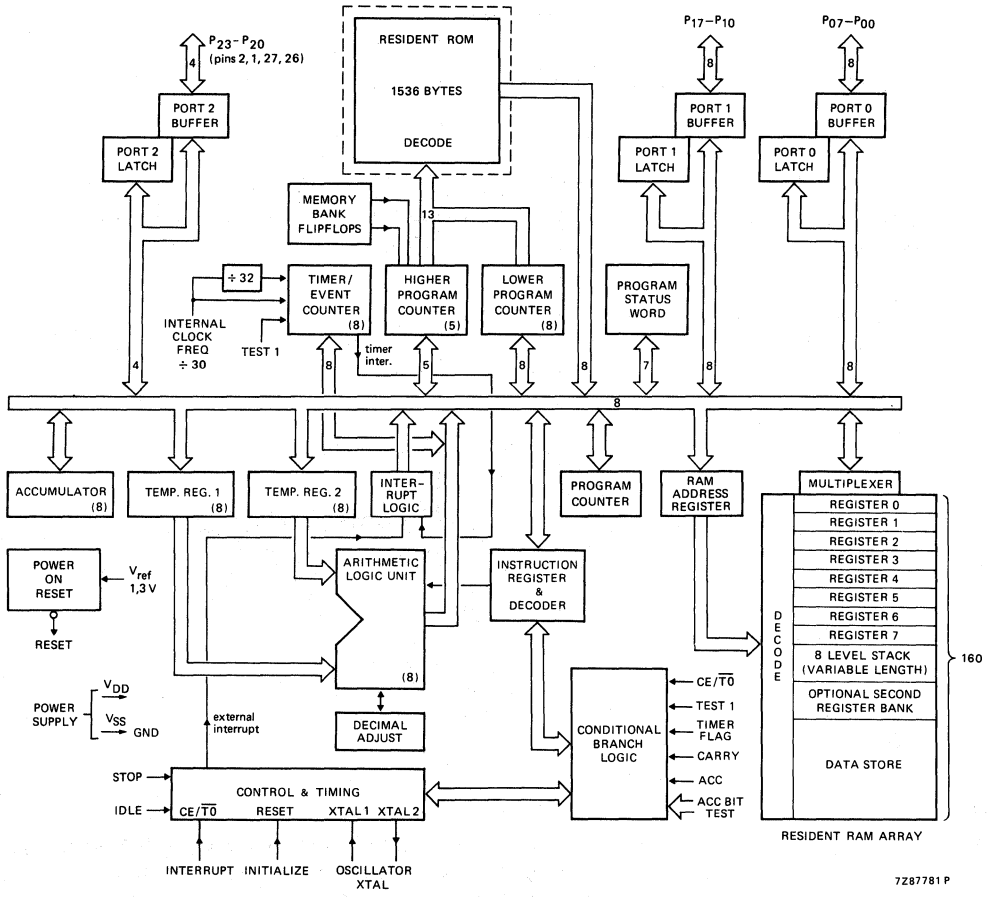
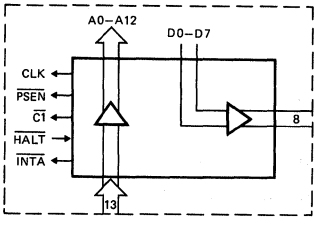
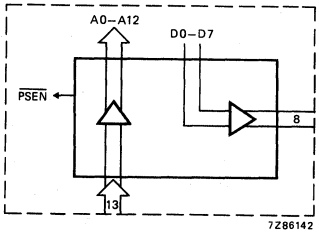


Fig. 1 Block diagram; PCD3315C.



(a)

Fig. 1a Replacement of dotted part in Fig. 1, for the PCD8500F bond-out version.



(b)

Fig. 1b Replacement of dotted part in Fig. 1, for the PCF8500B 'Piggy-back' version.

DEVELOPMENT DATA

PINNING

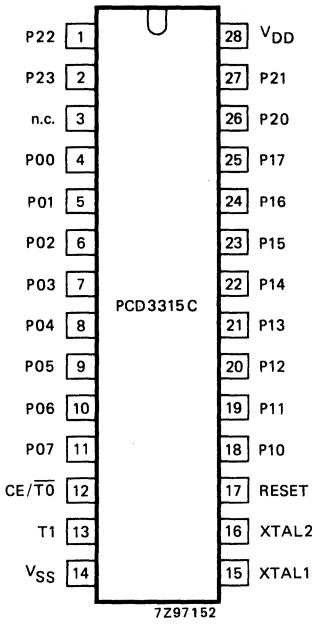


Fig. 2 Pinning diagram: PCD3315C.

PIN DESIGNATION

3	n.c.	not connected
4-11	P00-P07	**Port 0**: 8-bit quasi-bidirectional I/O port.
12	CE/$\overline{T0}$	**Interrupt/Test 0**: external interrupt input (sensitive to positive-going edge edge)/test input pin; when used as a test input directly tested by conditional branch instructions JT0 and JNT0.
13	T1	**Test 1**: test input pin, directly tested by conditional branch instructions JT1 and JNT1. T1 also functions as an input to the 8-bit timer/event counter, using the STRT CNT instruction.
14	V_{SS}	**Ground**: circuit earth potential.
15	XTAL 1	**Crystal input**: connection to timing component (crystal) which determines the frequency of the internal oscillator; also the input for an external clock source.
16	XTAL 2	connection to the other side of the timing component.
17	RESET	**Reset input**: used to initialize the processor (active HIGH), or output of power-on-reset circuit.
18-25	P10-P17	**Port 1**: 8-bit quasi-bidirectional I/O port.
26, 27, 1, 2	P20-P23	**Port 2**: 4-bit quasi-bidirectional I/O port.
28	V_{DD}	**Power supply**: 1,8 V to 6 V.

D.C. CHARACTERISTICS

V_{DD} = 2,5 to 6 V; V_{SS} = 0 V; T_{amb} = −25 to + 70 °C; all voltages with respect to V_{SS}; f = 3,58 MHz with R_S = 50 Ω; unless otherwise specified.

parameter	symbol	min.	typ.	max.	unit
Supply voltage					
operating	V_{DD}	1,8	–	6	V
STOP mode for RAM retention	V_{DD}	1,0	–	6	V
Supply current					
operating					
at V_{DD} = 3 V	I_{DD}	–	350	–	μA
IDLE mode					
at V_{DD} = 3 V	I_{DD}	–	150	–	μA
STOP mode (note 1)					
at V_{DD} = 1,8 V; T_{amb} = 25 °C	I_{DD}	–	1,2	2,5	μA
at V_{DD} = 1,8 V; T_{amb} = 55 °C	I_{DD}	–	–	5	μA
at V_{DD} = 1,8 V; T_{amb} = 70 °C	I_{DD}	–	–	10	μA
RESET I/O					
Switching level	V_{RESET}	–	1,2	–	V
Sink current					
at $V_{DD} > V_{RESET}$	I_{OL}	–	7	–	μA
Inputs					
Input voltage LOW	V_{IL}	0	–	$0{,}3V_{DD}$	V
Input voltage HIGH	V_{IH}	$0{,}7V_{DD}$	–	V_{DD}	V
Input leakage current					
at $V_{SS} < V_I < V_{DD}$	$\pm I_{IL}$	–	–	1	μA
Outputs					
Output voltage LOW					
at $V_I = V_{SS}$ or V_{DD}; $\lvert I_O \rvert < 1$ μA	V_{OL}	–	–	0,05	V
Output sink current LOW					
at V_{DD} = 3 V; V_O = 0,4 V	I_{OL}	0,6	1,5	–	mA
Pull-up output source current HIGH					
at V_{DD} = 3 V; $V_O = 0{,}9V_{DD}$	$-I_{OH}$	10	–	–	μA
at V_{DD} = 3 V; $V_O = V_{SS}$	$-I_{OH}$	–	–	200	μA
Push-pull output source current HIGH					
at V_{DD} = 3 V; $V_O = V_{DD}$−0,4 V	$-I_{OH}$	0,6	1,5	–	mA

Note 1

Crystal connected between XTAL 1 and XTAL 2; pin 2 pulled to V_{DD} via 5,6 kΩ resistor; CE and T1 at V_{SS}.

C-MOS INTERRUPTED CURRENT-LOOP DIALLING CIRCUIT

The PCD3320 is a single chip silicon-gate C-MOS integrated circuit. It is intended to convert pushbutton keyboard entries into streams of correctly-timed line current interruptions. The input data is derived from a telephone keyboard with a 3 x 4 pushbutton matrix. Numbers with up to 23 digits can be retained in a RAM for redial. A delayed reset is built-in for line power breaks.

The circuit has the following features:

- Operation from 2,5 V to 6 V supply.
- Static standby operation down to 1,8 V.
- Low current consumption; typ. 40 μA.
- Low static standby current; typ. 1 μA.
- On-chip oscillator for 3,58 MHz crystal.
- Fully decoded and debounced inputs for 3 x 4 matrix keyboard.
- All inputs with pull-up/pull-down (except CE).
- 23-digit capacity for redial operation.
- Circuit reset for line power breaks; $>$ 160 ms.
- Dialling pulse frequency: 10 Hz.
- Test pulse frequency: 932 Hz.
- Hold facility for lengthening the inter-digit period.
- Memory overflow possibility (with internally disabled redial).
- All inputs are internally protected against electrostatic charges.
- High input noise immunity.

PACKAGE OUTLINES

PCD3320P : 18-lead DIL; plastic (SOT-102GE).
PCD3320D: 18-lead DIL; ceramic (SOT-133B).

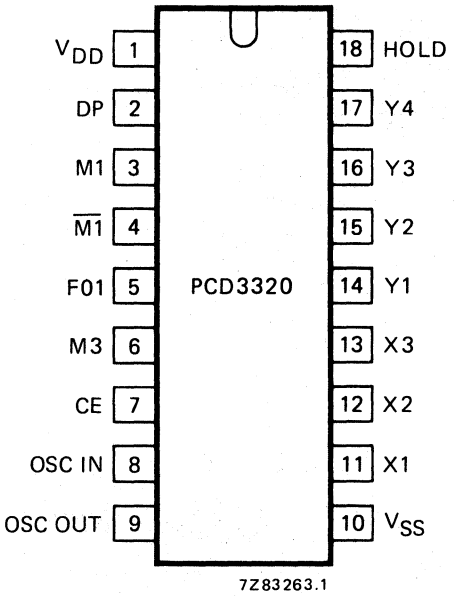


Fig. 1 Pinning diagram.

PINNING

1	V_{DD}	positive supply
10	V_{SS}	negative supply

Inputs

5	F01	the dialling pulse frequency is defined by the logic state of this input
7	CE	Chip Enable; used to initialize the system; to select between the operational mode and the static standby mode; to handle line power breaks.
11	X1	column keyboard inputs with pull-down on chip
12	X2	
13	X3	
14	Y1	row keyboard inputs with pull-up on chip
15	Y2	
16	Y3	
17	Y4	
18	HOLD	interrupts dialling after completion of the current digit or immediately following an inter-digit pause (t_{id}); further keyboard data will be accepted

Outputs

2	DP	Dialling Pulse; drive of the external line switching transistor or relay
3	M1	Muting; normally used for muting during the dialling sequence
4	$\overline{M1}$	inverted output of M1
6	M3	AND function, with $\overline{DP}$ and M1 as input, for direct drive of a switching transistor for dialling pulses and muting.

Oscillator

8	OSC IN	input and output of the on-chip oscillator
9	OSC OUT	

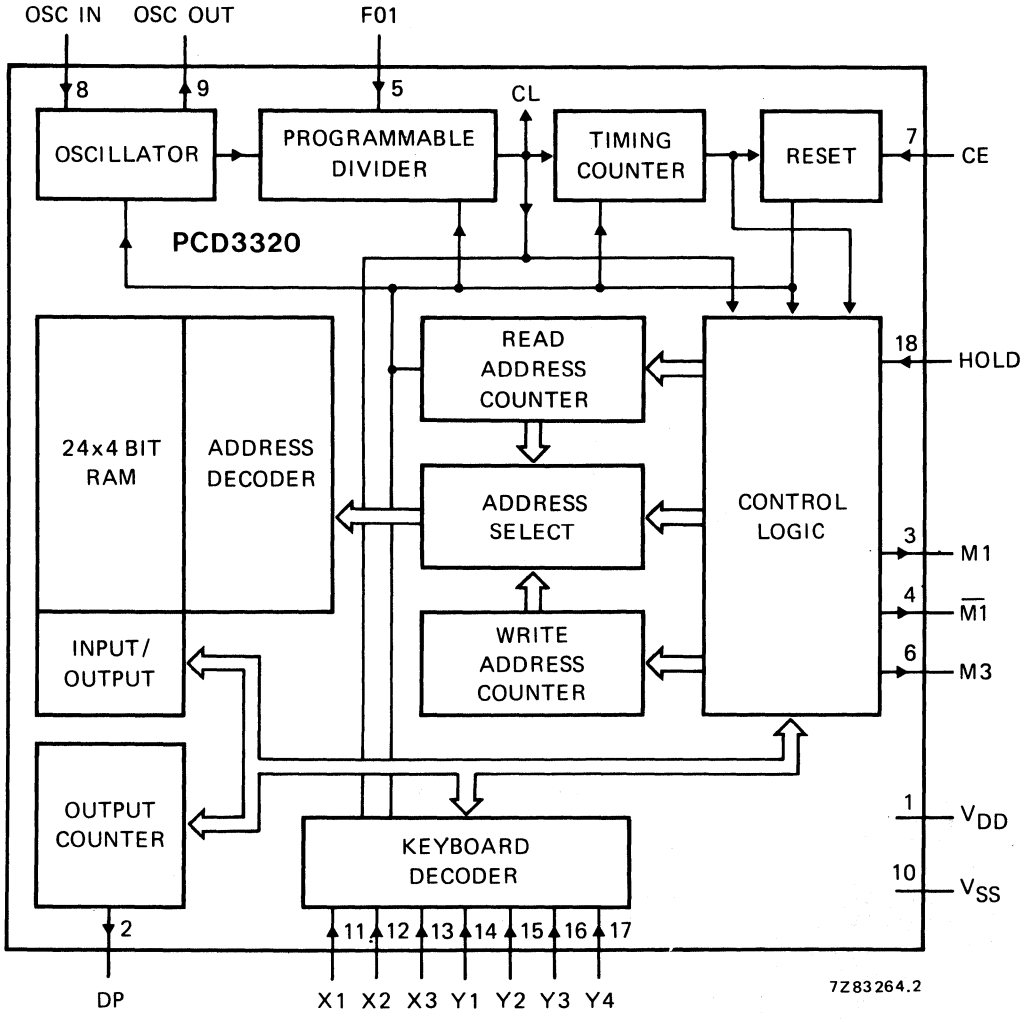


Fig. 2 Block diagram.

FUNCTIONAL DESCRIPTION (see also Fig. 2)

Clock oscillator (OSC IN, OSC OUT)

The time base for the PCD3320 is a crystal controlled on-chip oscillator which is completed only by connecting a crystal between the OSC IN and OSC OUT pins. The oscillator is followed by a frequency divider of which the division ratio can be externally set by input F01 to provide one of two chip system clocks; the 'normal' clock frequency (F01 = LOW) and the test frequency (F01 = HIGH).

Alternatively, the OSC IN input may be driven from an external clock signal.

Chip Enable (CE)

The CE input is used to initialize the chip system.

CE = LOW provides the static standby condition. In this mode the clock oscillator is off and internal registers are clamped reset with the exception of the WRITE ADDRESS COUNTER (WAC). The keyboard input is inhibited, but data previously entered is saved in the RAM.

When CE = HIGH the clock oscillator is operating, the internal registers are enabled and data can be entered from the keyboard.

If the CE input is taken to a LOW level for more than the time t_{rd} (see Figs 5 and 6 and timing data) an internal reset pulse will be generated at the end of the t_{rd} period. The system is then in the static standby mode. Short CE pulses of $< t_{rd}$ will not affect the operation of the circuit. No reset pulses are then produced.

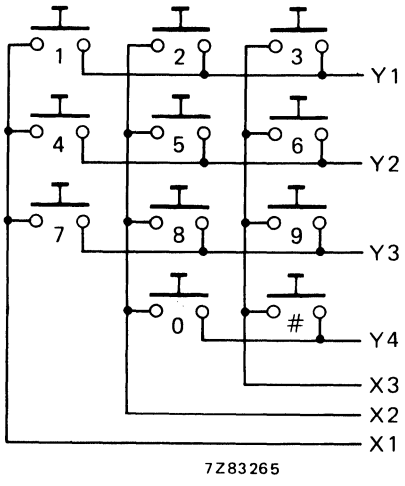
Debouncing keyboard entries

The column keyboard inputs to the integrated circuit (X_n) and the row keyboard inputs (Y_n) are for direct connection to a 3 x 4 single contact keyboard matrix (with or without common contact) as shown in Fig. 3, or to a double contact keyboard with a common left open (see Fig. 4). An entry is decoded into a 4-bit binary keycode by the keyboard decoder when one column input is connected to one row input or, when one column input is set HIGH and one row input is set LOW. Any other input combinations will be judged to be not valid and will not be accepted. Valid inputs are debounced on the leading and trailing edges as shown in Fig. 5. Keyboard entries are only decoded into 4-bit binary keycodes and written into the RAM if the keyboard contact remains closed for four or five clock pulse periods (entry period t_e). The next keyboard entry will not be accepted until the previously closed contact has been open for three or four clock pulse periods. The one clock pulse period of uncertainty in the debouncing process arises because keyboard entries are not detected until the trailing edge of the first clock pulse after the entry.

Data entry

After each keyboard entry has been debounced and decoded, the keycode is written into the RAM, and the WAC is incremented by one to select the next RAM location where the next keycode will be stored. As each keycode is recalled from the RAM for line pulsing, the READ ADDRESS COUNTER (RAC) is incremented by one to select the RAM location of the next keycode to be recalled. Consequently, the difference between the contents of the WAC and of the RAC represents the number of keycodes that have been written into the RAM but not yet converted into line pulses. If more than 23 keycodes are written into the RAM, memory overflow results and the excess keycode replace the data in the lower numbered RAM locations. In this event, since an erroneous number is stored, automatic redialling is inhibited until the WAC has been reset by the first digit entry of the next telephone call.

If the first pushbutton to be pressed is not redial (#), the WAC is reset during entry time t_e, the corresponding keycode is written into the first RAM location, and the WAC is then incremented by one. If the first pushbutton to be pressed is redial (#), the WAC is not reset and the keycodes stored in the RAM are sequentially recalled and converted into correctly timed dialling pulses at output DP. During redial no keyboard entry will be accepted and stored in the RAM. But, when all in the RAM stored numbers have been pulsed out, new keyboard entry will be accepted, stored in the RAM and converted into correctly timed dialling pulses.



Redial.

Fig. 3 Single contact keyboard.

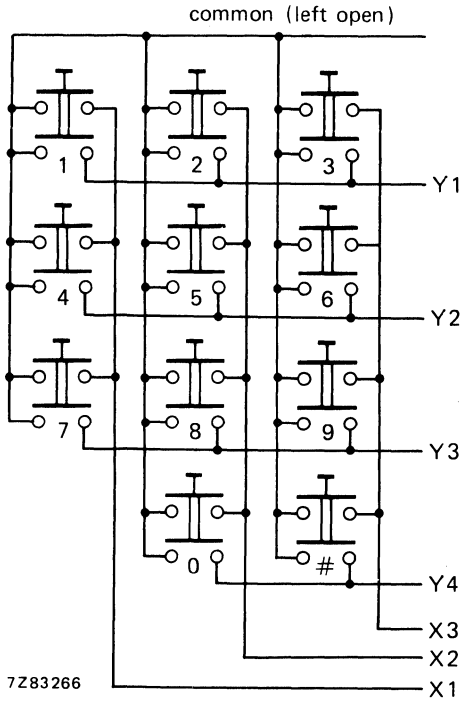


Fig. 4 Double contact keyboard.

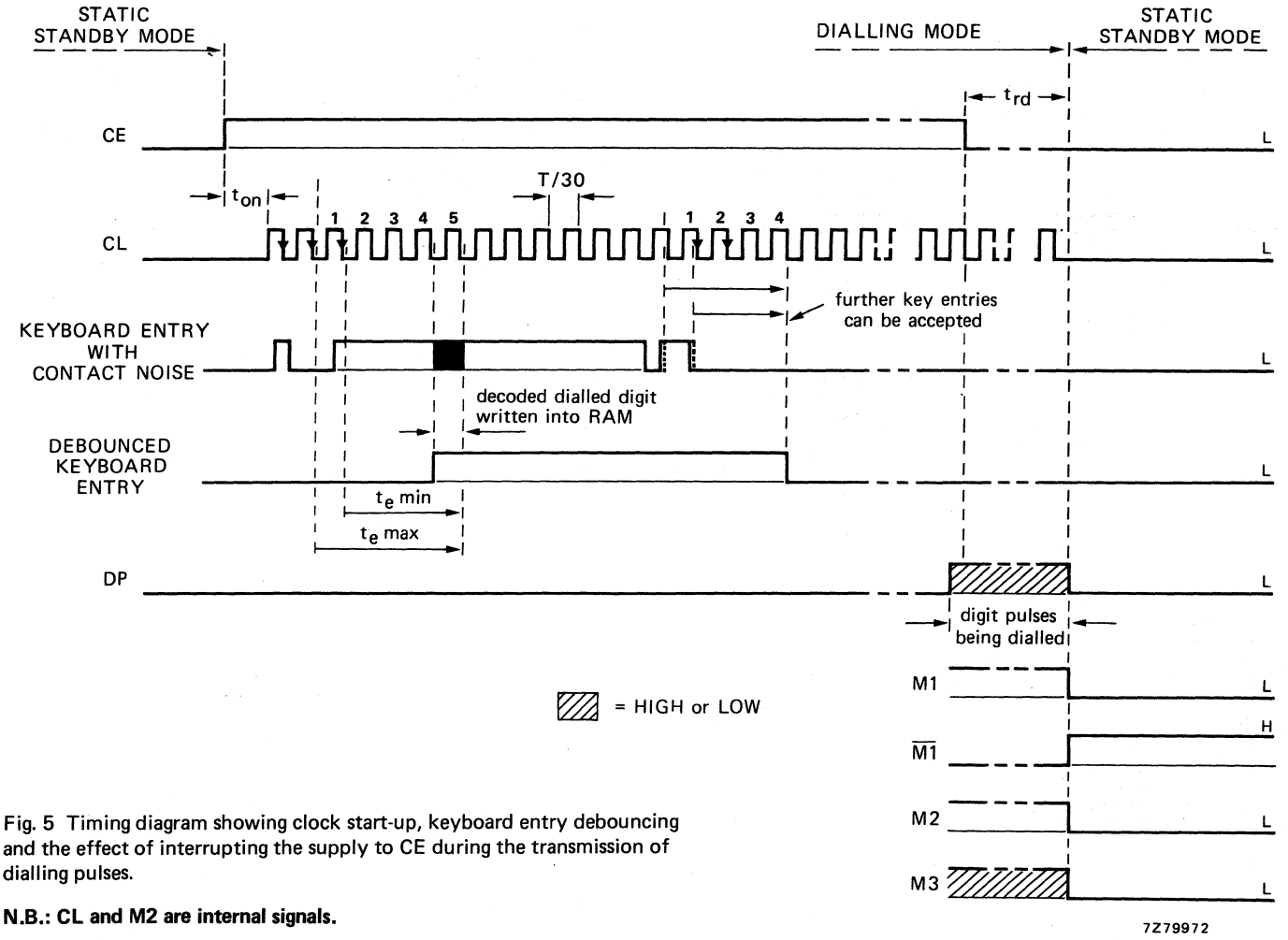


Fig. 5 Timing diagram showing clock start-up, keyboard entry debouncing and the effect of interrupting the supply to CE during the transmission of dialling pulses.

N.B.: CL and M2 are internal signals.

Dialling sequence

The dialling sequence can be initiated under either of the following two conditions:

- The supply to the integrated circuit is derived from the telephone lines via the cradle contacts (power supply before keyboard entry); see Fig. 6.

Then, approximately 4 ms (t_{on}) after CE goes HIGH, the clock pulse generator starts and, ten clock pulse periods (t_d) later, a prepulse with a duration of ten clock pulse periods (t_d) appears at outputs M1 and M3. This prepulse ensures that, if a polarized muting relay with two stable positions is used, it switches to the de-muted position so that the circuit is then in the conversation mode whilst the subscriber awaits the dialling tone. When the first digit of the required number is entered at the keyboard, data entry period t_e commences.

- The supply to the integrated circuit is derived from the telephone lines via the cradle contacts in series with a common keyboard contact (Fig. 7).

When the first digit of the required number is entered at the keyboard, the common keyboard contact connects the line voltage to V_{DD} and CE becomes HIGH. Approximately 4 ms (t_{on}) after CE goes HIGH, the clock pulse generator starts and data entry period t_e commences. After period t_e, M1 goes HIGH and the pushbutton can be released. The supply to V_{DD} and CE is then maintained via the muting circuit controlled by M1.

The further dialling sequence will be described with the aid of Fig. 6. When the keyboard entry has been decoded and written into the RAM, M1 goes HIGH to mute the telephone and an inter-digit pause (t_{id}) ensues. M2 then goes HIGH (M2 is an internally generated signal, used for explanation only), the RAC addresses the RAM and the first keycode is loaded into the register of the output counter which generates the appropriate number of correctly-timed dialling pulses at outputs DP and M3. When the digit has been pulsed out, M2 goes LOW, the RAC is incremented by one and the procedure repeats until the WAC and RAC contents are equal (all digits pulsed out). Output M1 then goes LOW, the circuit assumes the conversation mode. The circuit reverts to the static standby mode if CE goes LOW for more than the reset delay time (t_{rd} = 1,6 dialling pulse periods) at any time during the conversation or dialling mode (e.g. because the handset is replaced). CE remains LOW although V_{DD} is maintained by a back-up supply (e.g. because an external diode isolates CE from the back-up supply connected to V_{DD}). The RAM retains its contents for subsequent automatic redialling as long as the back-up supply maintains V_{DD} above V_{DDO} = 1,8 V.

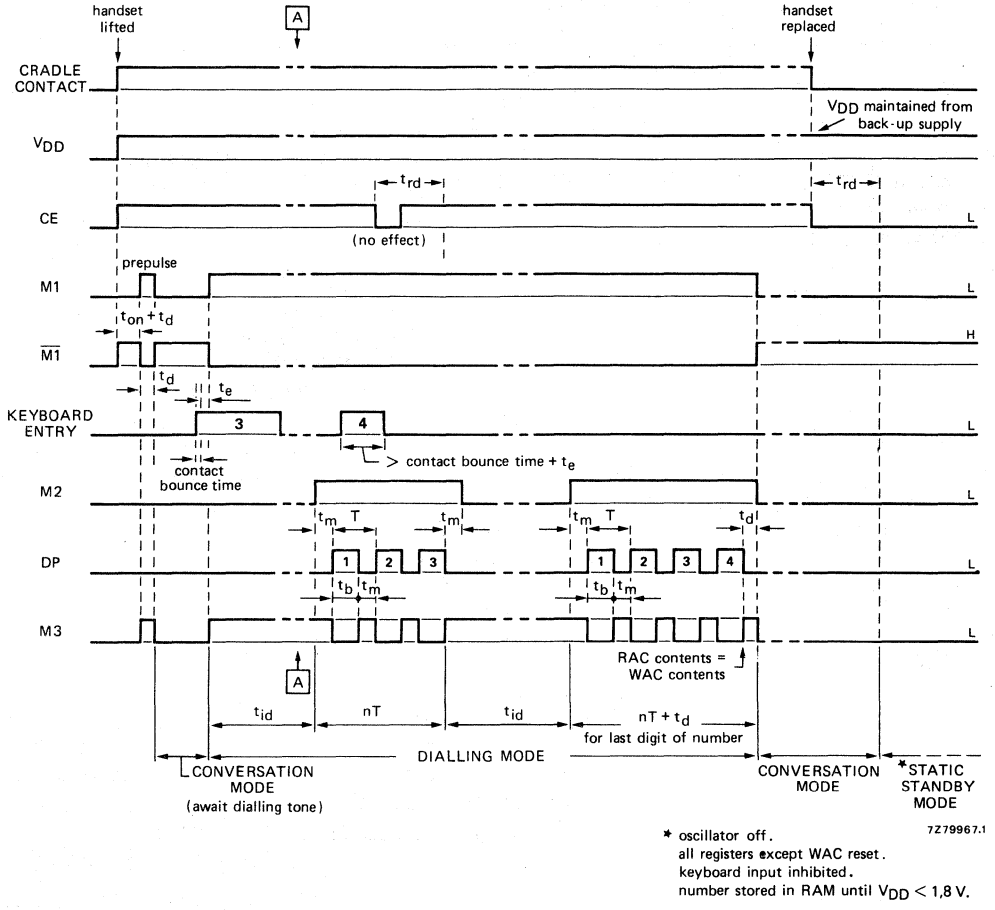


Fig. 6 Timing diagram of dialling sequence with V_{DD} and CE HIGH before keyboard entry (e.g. supply via the cradle contacts). M2 is an internal signal.

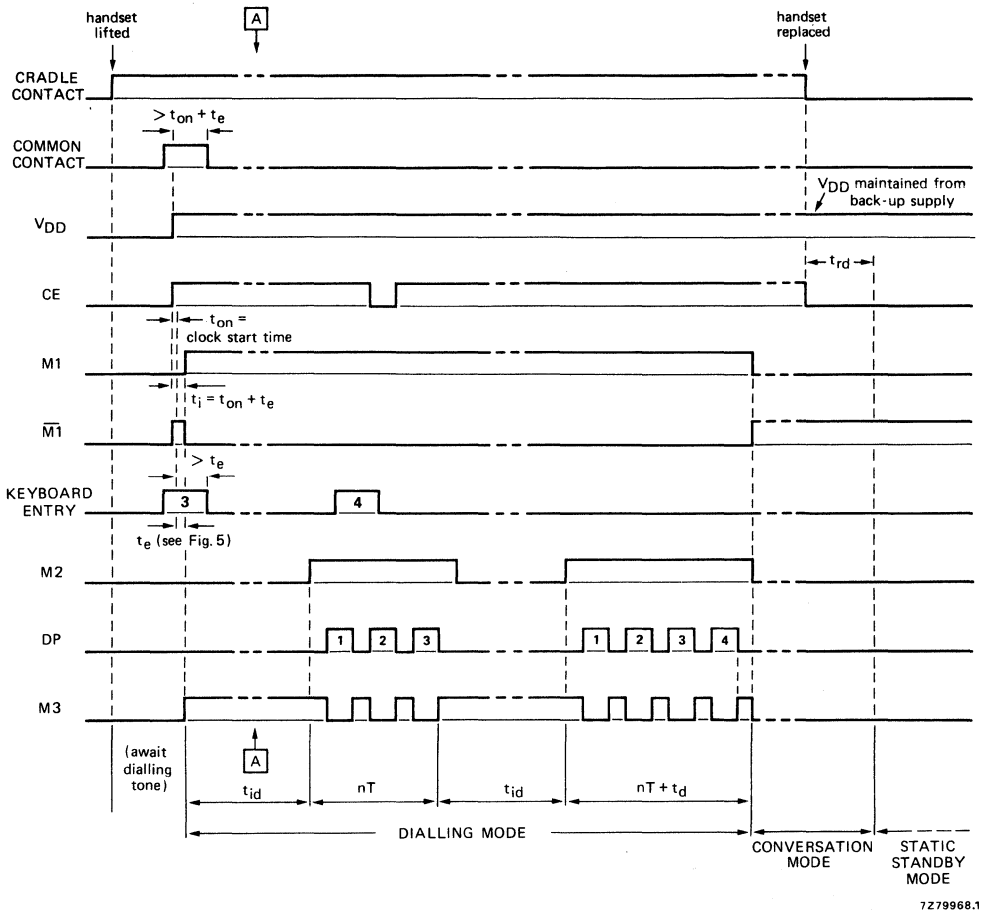


Fig. 7 Timing diagram for initiating the dialling mode with V_{DD} and CE initially supplied via the cradle contacts in series with a common contact on the keyboard. See Fig. 6 for pulse timings after point A. M2 is an internal signal.

Hold function

As shown in Fig. 8, the hold function allows the interval between consecutive pulsed digits to be prolonged under the control of external equipment. When the HOLD input is set HIGH, the dialling pulse-train is interrupted as soon as M2 goes LOW to signal that the current digit has been pulsed out. In the hold condition, further keyboard entries will be accepted, debounced, decoded and stored in that RAM. No further keycodes will be read from the RAM and converted into dialling pulses on M3 and DP until the HOLD input is set LOW again and an inter-digit pause has elapsed.

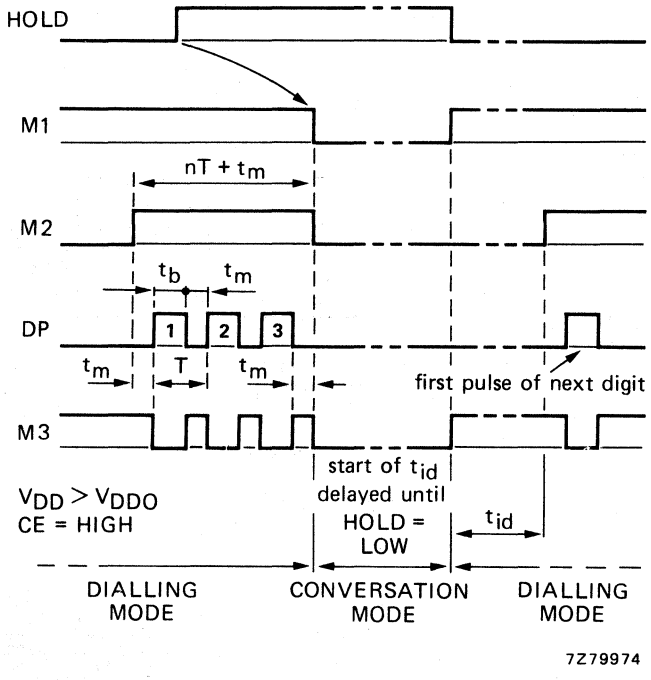


Fig. 8 Timing diagram showing the effect of activating the HOLD input during the transmission of dialling pulses. M2 is an internal signal.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_{DD}	−0,3 to 8 V
Voltage on any pin	V_I	V_{SS}−0,3 to V_{DD} + 0,3 V
Operating ambient temperature range	T_{amb}	−25 to + 70 °C
Storage temperature range	T_{stg}	−55 to + 125 °C

CHARACTERISTICS

V_{DD} = 3 V; V_{SS} = 0 V; crystal parameters: f_{osc} = 3,58 MHz, R_{Smax} = 100 Ω (note 3); T_{amb} = 25 °C; unless otherwise specified

	symbol	min.	typ.	max.		conditions
Operating supply voltage	V_{DD}	2,5	3	6	V	T_{amb} = −25 to + 70 °C
Standby supply voltage (note 1)	V_{DDO}	1,8	–	6	V	T_{amb} = −25 to + 70 °C
Operating supply current	I_{DD}	–	40	–	μA	CE = HIGH; notes 2, 3
	I_{DD}	–	50	100	μA	CE = HIGH; V_{DD} = 6 V; notes 2, 3
Standby supply current	I_{DDO}	–	1	5	μA	CE = LOW; note 2
	I_{DDO}	–	–	2	μA	V_{DD} = 1,8 V; T_{amb} = −25 to + 70 °C
Input voltage LOW	V_{IL}	–	–	0,3 V_{DD}		1,8 V ⩽ V_{DD} ⩽ 6 V
Input voltage HIGH	V_{IH}	0,7 V_{DD}	–	–		1,8 V ⩽ V_{DD} ⩽ 6 V
Input leakage current; CE LOW	$-I_{IL}$	–	–	50	nA	CE = LOW
HIGH	I_{IH}	–	–	50	nA	CE = HIGH
Pull-down input current F01, HOLD	I_{IH}	30	100	300	nA	V_I = V_{DD}
Matrix keyboard operation						
Keyboard current	I_K	–	10	–	μA	X connected to Y, CE = HIGH
Keyboard 'ON' resistance	R_{KON}	–	–	500	Ω	contact ON; note 4
Keyboard 'OFF' resistance	R_{KOFF}	1	–	–	MΩ	contact OFF; note 4
Other keyboard operation						
Input current for X_n 'ON'	I_{IH}	–	–	30	μA	V_I = 1,5 to 3 V
Input current for Y_n 'ON'	$-I_{IL}$	10	–	–	μA	V_I = 0 to 2,5 V
Input current Y_n	$-I_I$	–	–	0,7	mA	V_I = V_{SS}
Output sink current	I_{OL}	0,7	1,5	3,2	mA	V_{OL} = 0,5 V
Output source current	$-I_{OH}$	0,65	1,3	2,7	mA	V_{OH} = 2,5 V

Notes

1. V_{DDO} = 1,8 V only for redial.
2. All other inputs and outputs open.
3. Stray capacitance between pins 8 and 9 < 3 pF.
4. Guarantees correct keyboard operation.

TIMING DATA I

V_{DD} = 3 V; V_{SS} = 0 V; crystal parameters: f_{osc} = 3,58 MHz; R_{Smax} = 100 Ω

	symbol	min.	typ.	max.		conditions
Clock start-up time	t_{on}	–	4	–	ms	Figs 6, 7; note 1
Initial data entry time ($t_i = t_{on} + t_e$)	$t_{i\,min}$	–	18	–	ms	F01 = LOW } Fig. 7
	$t_{i\,max}$	–	4	–	ms	F01 = HIGH } Fig. 7

TIMING DATA II (exact values)

V_{DD} = 2,5 to 6 V; V_{SS} = 0 V; f_{osc} = 3,58 MHz

	symbol	F01 = LOW (dialling)	F01 = HIGH (testing)		conditions
Dialling pulse frequency	f_{DP}	10,13	932,2	Hz	note 2
Dialling pulse period; $1/f_{DP}$	T_{DP}	98,7	1,073	ms	Figs 6, 7
Prepulse duration; 1/3 x T_{DP}	t_d	33	0,358	ms	Figs 6, 7
Inter-digit pause; 8 x T_{DP}	t_{id}	790	8,58	ms	Figs 6, 7
Break time; 3/5 x T_{DP}	t_b	59,2	0,644	ms	Fig. 6
Make time; 2/5 x T_{DP}	t_m	39,5	0,429	ms	Fig. 6
Debounce time					
min. 4/30 x T_{DP}	$t_{e\,min}$	13,2	0,143	ms	Fig. 5
max.; 1/6 x T_{DP}	$t_{e\,max}$	16,5	0,179	ms	Fig. 5
Reset delay time; 1,6 x T_{DP}	t_{rd}	158	1,7	ms	Figs 5, 6, 7

Notes

1. Stray capacitance between pins 8 and 9 < 3 pF.
2. Exactly 10 Hz and 920 Hz respectively when a 3,5328 MHz crystal is used.

TYPICAL CURVES

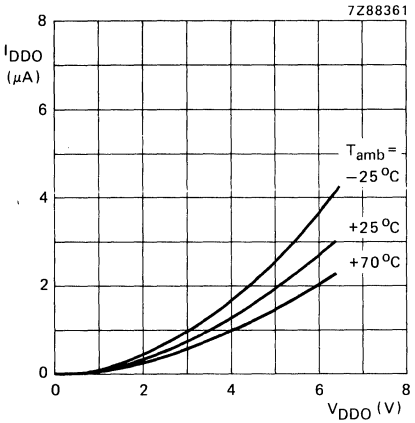


Fig. 9 Standby supply current as a function of standby supply voltage.

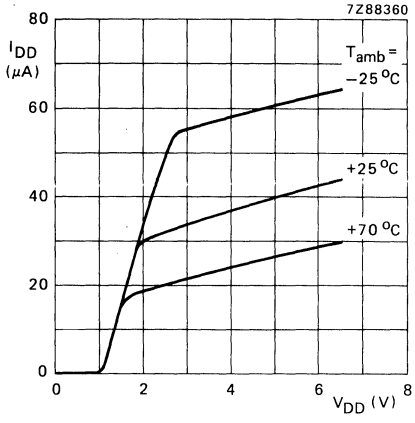


Fig. 10 Operating supply current as a function of operating supply voltage.

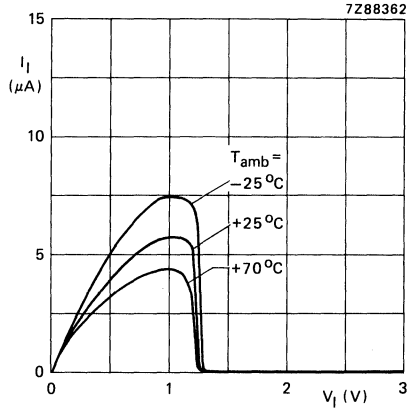


Fig. 11 Pull-down input current as a function of input voltage at V_{DD} = 3 V.

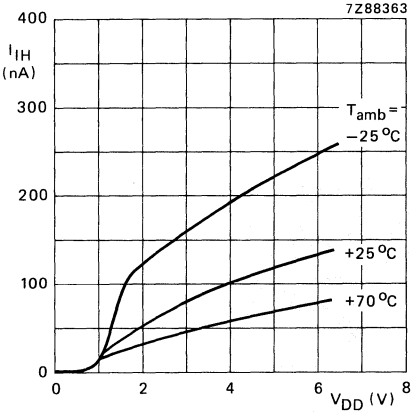


Fig. 12 Pull-down input current as a function of supply voltage at $V_I = V_{DD}$.

TYPICAL CURVES (continued)

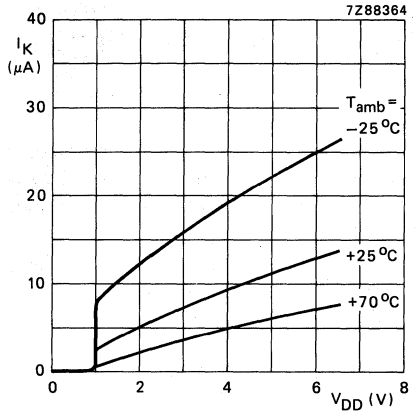


Fig. 13 Keyboard current as a function of supply voltage; X-pins connected to Y-pins.

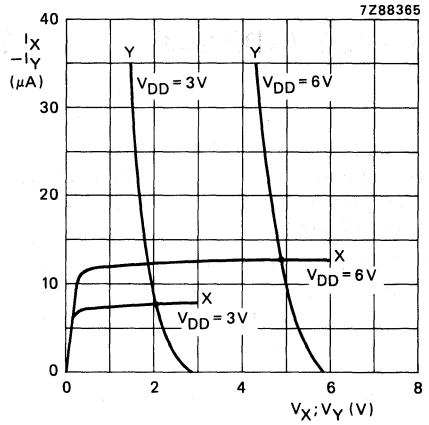


Fig. 14 Keyboard input characteristics at T_{amb} = 25 °C.

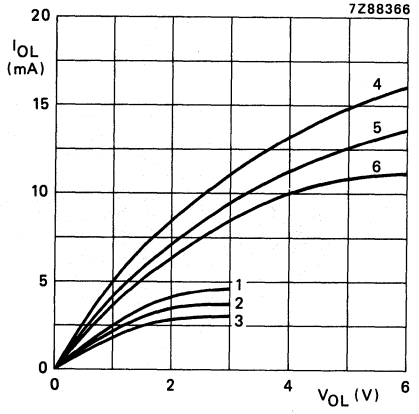


Fig. 15 Output (N-channel) sink characteristics for M1, $\overline{M1}$, M3 and DP.

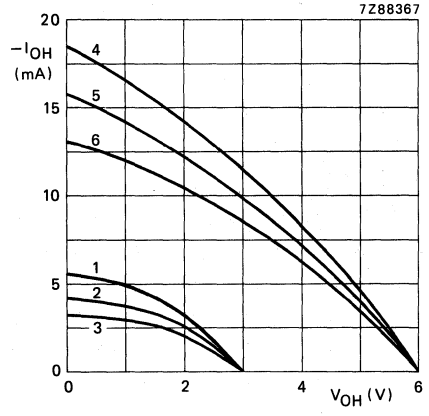


Fig. 16 Output (P-channel) source characteristics for M1, $\overline{M1}$, M3 and DP.

Curves for Figs 15 and 16

T_{amb}	V_{DD} = 3 V	V_{DD} = 6 V
−25 °C	1	4
+25 °C	2	5
+70 °C	3	6

C-MOS INTERRUPTED CURRENT-LOOP DIALLING CIRCUIT

The PCD3321 is a single chip silicon-gate C-MOS integrated circuit. It is intended to convert pushbutton keyboard entries into streams of correctly-timed line current interruptions. The input data is derived from a telephone keyboard with a 3 x 4 pushbutton matrix. Numbers with up to 23 digits can be retained in a RAM for redial. A delayed reset is built-in for line power breaks.

The PCD3321 can regenerate access pauses during redial. During the original entry, access pauses are stored either automatically or via the keyboard. A regenerated access pause can be terminated during redial in three ways: automatically after a built-in time, or via the keyboard, or with an external dial tone recogniser circuit. This makes the circuit very suitable for redial in PABX (Private Automatic Branch Exchange) systems. The PCD3321 is pin to pin compatible with the DF320 and the MT4320 (however, including additional functions).

The circuit has the following features:

- Operation from 2,5 V to 6 V supply.
- Static standby operation down to 1,8 V.
- Low current consumption; typ. 40 μA.
- Low static standby current; typ. 1 μA.
- On-chip oscillator for 3,58 MHz crystal.
- Fully decoded and debounced inputs for 3 x 4 matrix keyboard.
- 23-digit capacity, including access pauses, for redial operation.
- Memory overflow possibility (with internally disabled redial).
- Selectable dialling pulse frequency: 10 Hz, 16 Hz and 20 Hz.
- Test pulse frequency: 932 Hz.
- Selectable dialling pulse mark/space ratios; 2 : 1 or 3 : 2.
- Hold facility for lengthening the inter-digit period.
- Circuit reset for line power breaks; $>$ 160 ms (10 Hz dialling pulse frequency).
- Access pause generation automatically or via the keyboard.
- Access pause reset:
  automatically after 3 s (10 Hz dialling pulse frequency),
  via the keyboard,
  with external tone recogniser.
- All inputs with pull-up/pull-down (except CE).
- All inputs are internally protected against electrostatic charges.
- High input noise immunity.

PACKAGE OUTLINES

PCD3321P: 18-lead DIL; plastic (SOT-102GE).
PCD3321D: 18-lead DIL; ceramic (SOT-133B).

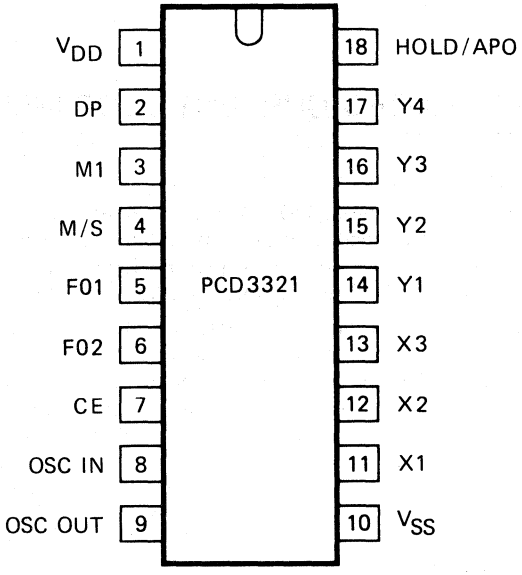


Fig. 1 Pinning diagram.

PINNING

1	V_{DD}	positive supply
10	V_{SS}	negative supply

Inputs

4	M/S	controls the mark-to-space ratio of the line pulses
5	F01	the dialling pulse frequency is defined by the logic state of these two inputs
6	F02	
7	CE	Chip Enable; used to initialize the system; to select between the operational mode and the static standby mode; to handle line power breaks
11	X1	column keyboard inputs with pull-down on chip
12	X2	
13	X3	
14	Y1	row keyboard inputs with pull-up on chip
15	Y2	
16	Y3	
17	Y4	

Outputs

2	DP	Dialling Pulse; drive of the external line switching transistor or relay
3	M1	Muting; normally used for muting during the dialling sequence

Input/output

18	HOLD/APO	This pin will go HIGH when an access pause code is read from the memory during pulsing and will interrupt dialling. It can also be externally controlled; it will interrupt dialling after completion of the current digit or immediately during an inter-digit pause (t_{id}); further keyboard data will be accepted.

Oscillator

8	OSC IN	input and output of the on-chip oscillator
9	OSC OUT	

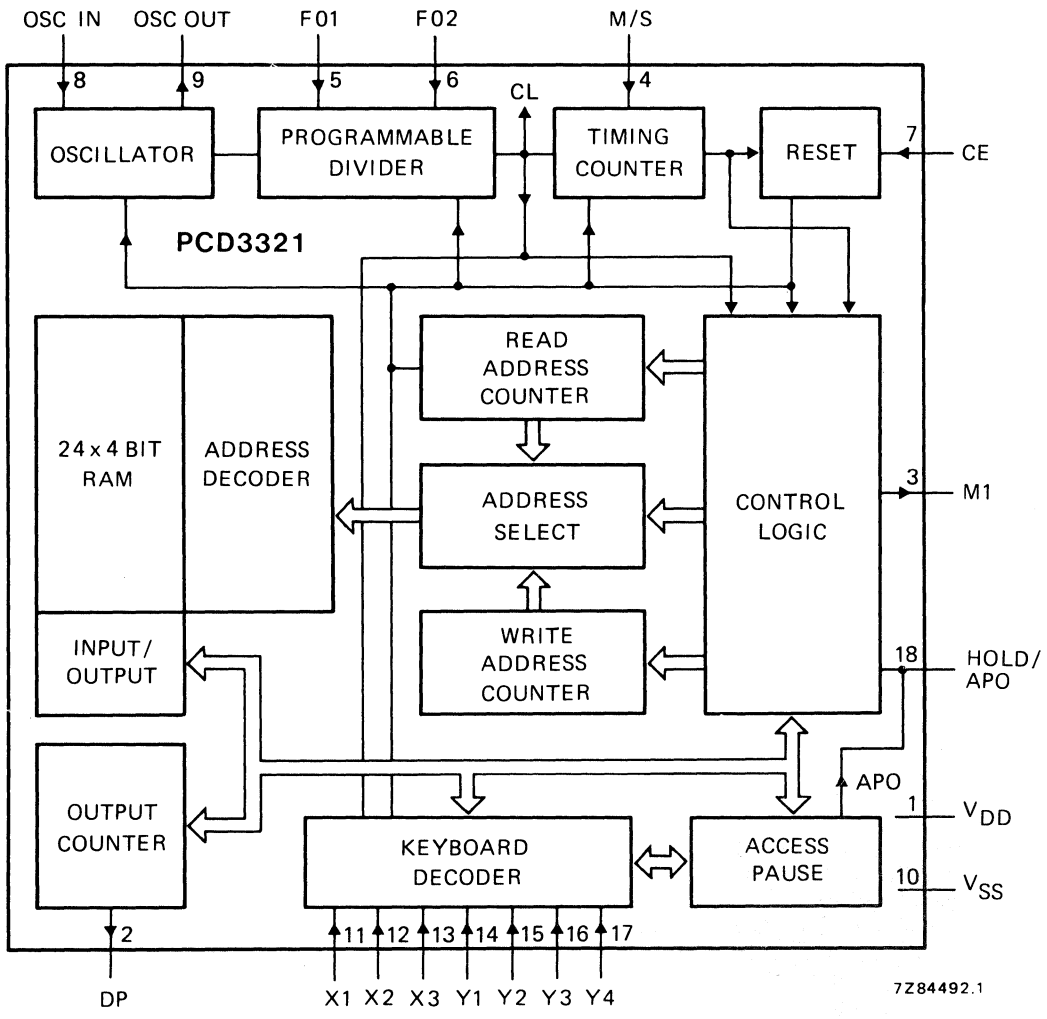


Fig. 2 Block diagram.

FUNCTIONAL DESCRIPTION (see also Fig. 2)

Clock oscillator (OSC IN, OSC OUT)

The time base for the PCD3321 is a crystal controlled on-chip oscillator which is completed only by connecting a crystal between the OSC IN and OSC OUT pins. The oscillator is followed by a frequency divider of which the division ratio can be externally set (F01 and F02) to provide one of four chip system clocks; three 'normal' clock frequencies and one higher test frequency.

Alternatively, the OSC IN input may be driven from an external clock signal.

Chip Enable (CE)

The CE input is used to initialize the chip system.

CE = LOW provides the static standby condition. In this mode the clock oscillator is off and internal registers are clamped reset with the exception of the WRITE ADDRESS COUNTER (WAC). The keyboard input is inhibited, but data previously entered is saved in the RAM.

When CE = HIGH the clock oscillator is operating, the internal registers are enabled and data can be entered from the keyboard.

If the CE input is taken to a LOW level for more than the time t_{rd} (see Figs 5 and 6 and timing data) an internal reset pulse will be generated at the end of the t_{rd} period. The system is then in the static standby mode. Short CE pulses of $< t_{rd}$ will not affect the operation of the circuit. No reset pulses are then produced.

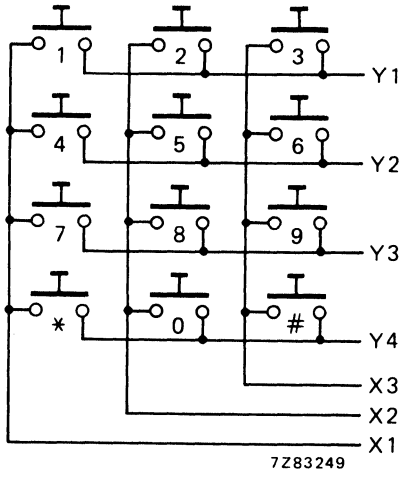
Debouncing keyboard entries

The column keyboard inputs to the integrated circuit (X_n) and the row keyboard inputs (Y_n) are for direct connection to a 3 x 4 single contact keyboard matrix (with or without common contact) as shown in Fig. 3, or to a double contact keyboard with a common left open (see Fig. 4). An entry is decoded into a 4-bit binary keycode by the keyboard decoder when one column input is connected to one row input or, when one column input is set HIGH and one row input is set LOW. Any other input combinations will be judged to be not valid and will not be accepted. Valid inputs are debounced on the leading and trailing edges as shown in Fig. 5. Keyboard entries are only decoded into 4-bit binary keycodes and written into the RAM if the keyboard contact remains closed for four or five clock pulse periods (entry period t_e). The next keyboard entry will not be accepted until the previously closed contact has been open for three or four clock pulse periods. The one clock pulse period of uncertainty in the debouncing process arises because keyboard entries are not detected until the trailing edge of the first clock pulse after the entry.

Data entry

After each keyboard entry has been debounced and decoded, the keycode is written into the RAM, and the WAC is incremented by one to select the next RAM location where the next keycode will be stored. As each keycode is recalled from the RAM for line pulsing, the READ ADDRESS COUNTER (RAC) is incremented by one to select the RAM location of the next keycode to be recalled. Consequently, the difference between the contents of the WAC and of the RAC represents the number of keycodes that have been written into the RAM but not yet converted into line pulses. If more than 23 keycodes are written into the RAM, memory overflow results and the excess keycode replace the data in the lower numbered RAM locations. In this event, since an erroneous number is stored, automatic redialling is inhibited until the WAC has been reset by the first digit entry of the next telephone call.

If the first pushbutton to be pressed is not redial (#), the WAC is reset during entry time t_e, the corresponding keycode is written into the first RAM location, and the WAC is then incremented by one. If the first pushbutton to be pressed is redial (#), the WAC is not reset and the keycodes stored in the RAM are sequentially recalled and converted into correctly timed dialling pulses at output DP. If the redial pushbutton (#) is operated again during the redialling sequence it will be decoded as an Access Pause Reset. This function will be described later during the description of the access pause system of the PCD3321. During redial no keyboard entry will be accepted and stored in the RAM. But, when all in the RAM stored numbers have been pulsed out, new keyboard entry will be accepted, stored at the RAM position after the last digit code of the original entry and converted into correctly timed dialling pulses.



★ Access pause set.

Redial or Access Pause Reset.

Fig. 3 Single contact keyboard.

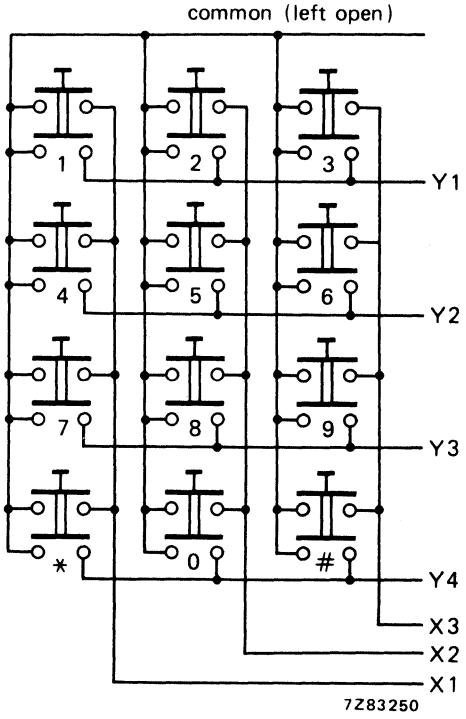


Fig. 4 Double contact keyboard.

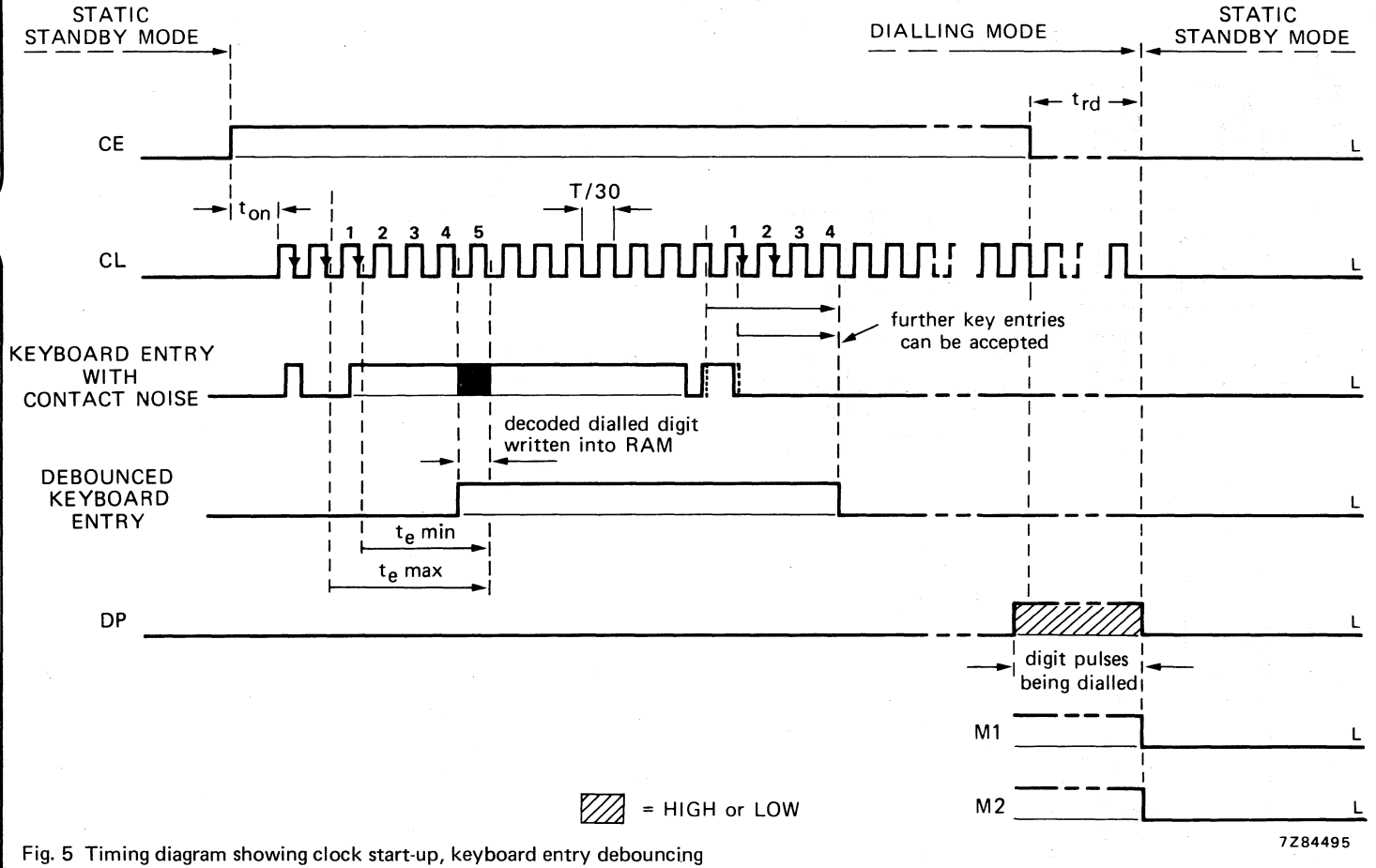


Fig. 5 Timing diagram showing clock start-up, keyboard entry debouncing and the effect of interrupting the supply to CE during the transmission of dialling pulses.

N.B.: CL and M2 are internal signals.

Dialling sequence

The dialling sequence can be initiated under either of the following two conditions:

- The supply to the integrated circuit is derived from the telephone lines via the cradle contacts (power supply before keyboard entry); see Fig. 6.

Then, approximately 4 ms (t_{on}) after CE goes HIGH, the clock pulse generator starts and, ten clock pulse periods (t_d) later, a prepulse with a duration of ten clock pulse periods (t_d) appears at output M1. This prepulse ensures that, if a polarized muting relay with two stable positions is used, it switches to the de-muted position so that the circuit is then in the conversation mode whilst the subscriber awaits the dialling tone. When the first digit of the required number is entered at the keyboard, data entry period t_e commences.

- The supply to the integrated circuit is derived from the telephone lines via the cradle contacts in series with a common keyboard contact (Fig. 7).

When the first digit of the required number is entered at the keyboard, the common keyboard contact connects the line voltage to V_{DD} and CE becomes HIGH. Approximately 4 ms (t_{on}) after CE goes HIGH, the clock pulse generator starts and data entry period t_e commences. After period t_e, M1 goes HIGH and the pushbutton can be released. The supply to V_{DD} and CE is then maintained via the muting circuit controlled by M1.

The further dialling sequence will be described with the aid of Fig. 6. When the keyboard entry has been decoded and written into the RAM, M1 goes HIGH to mute the telephone and an inter-digit pause (t_{id}) ensues. M2 then goes HIGH (M2 is an internally generated signal, used for explanation only), the RAC addresses the RAM and the first keycode is loaded into the register of the output counter which generates the appropriate number of correctly-timed dialling pulses at output DP. When the digit has been pulsed out, M2 goes LOW, the RAC is incremented by one and the procedure repeats until the WAC and RAC contents are equal (all digits pulsed out). Output M1 then goes LOW, the circuit assumes the conversation mode. The circuit reverts to the static standby mode if CE goes LOW for more than the reset delay time (t_{rd} = 1,6 dialling pulse periods) at any time during the conversation or dialling mode (e.g. because the handset is replaced). CE remains LOW although V_{DD} is maintained by a back-up supply (e.g. because an external diode isolates CE from the back-up supply connected to V_{DD}). The RAM retains its contents for subsequent automatic redialling as long as the back-up supply maintains V_{DD} above V_{DDO} = 1,8 V.

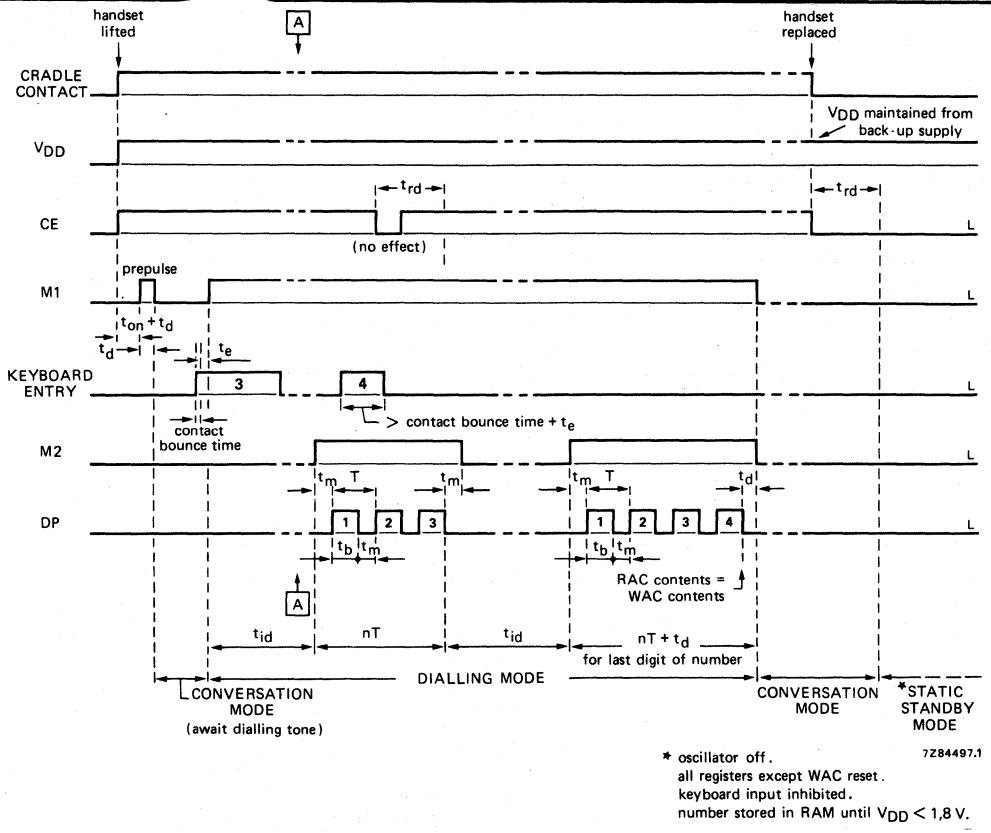


Fig. 6 Timing diagram of dialling sequence with V_{DD} and CE HIGH before keyboard entry (e.g. supply via the cradle contacts). M2 is an internal signal.

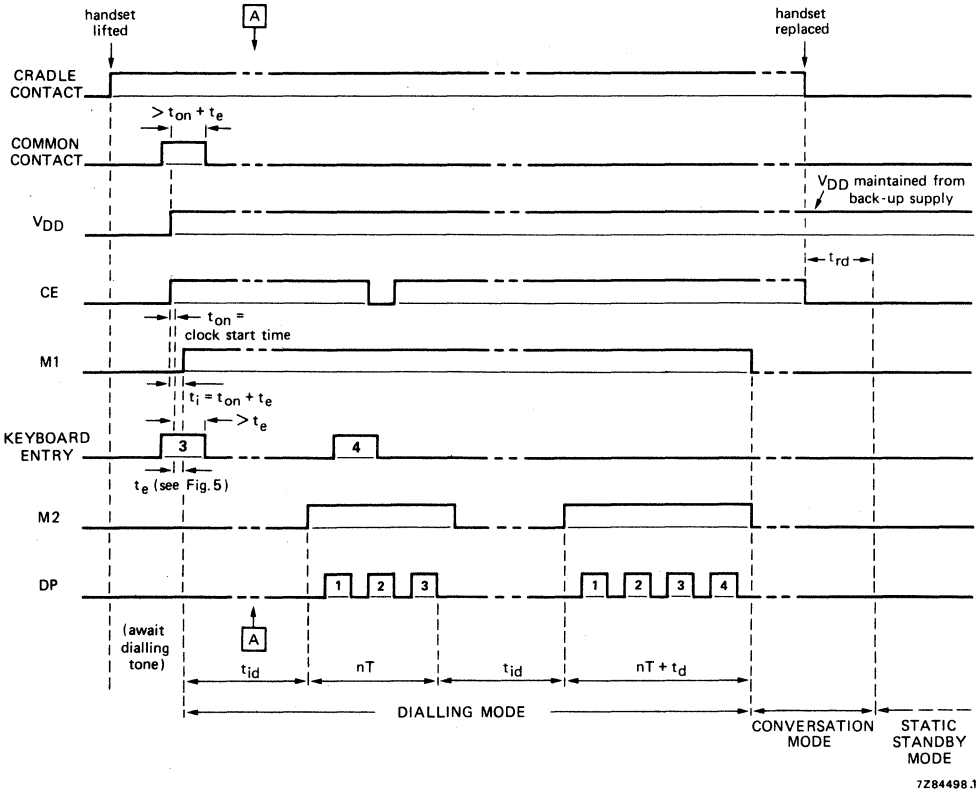


Fig. 7 Timing diagram for initiating the dialling mode with V_{DD} and CE initially supplied via the cradle contacts in series with a common contact on the keyboard. See Fig. 6 for pulse timings after point A. M2 is an internal signal.

Hold function

As shown in Fig. 8, the hold function allows the interval between consecutive pulsed digits to be prolonged under the control of external equipment. When the HOLD/APO is set HIGH, the dialling pulse-train is interrupted as soon as M2 goes LOW to signal that the current digit has been pulsed out. In the hold condition, further keyboard entries will be accepted, debounced, decoded and stored in that RAM. No further keycodes will be read from the RAM and converted into dialling pulses on DP until the HOLD/APO is set LOW again and an inter-digit pause has elapsed.

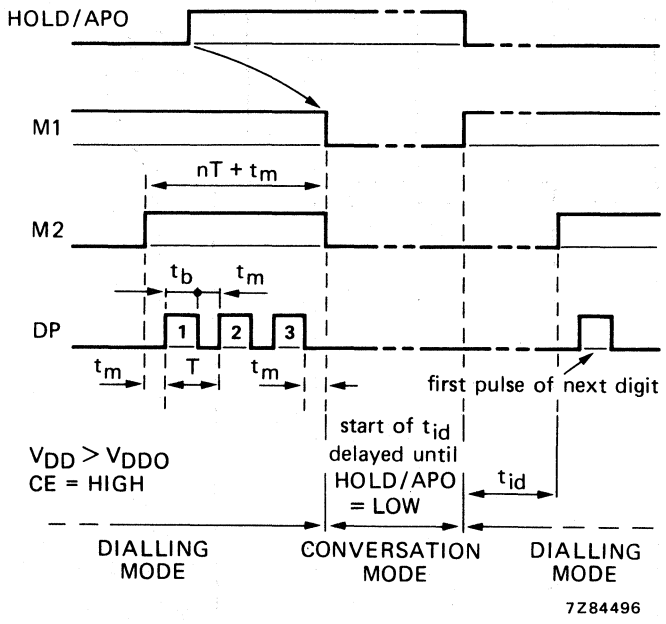


Fig. 8 Timing diagram showing the effect of activating the HOLD/APO during the transmission of dialling pulses. M2 is an internal signal.

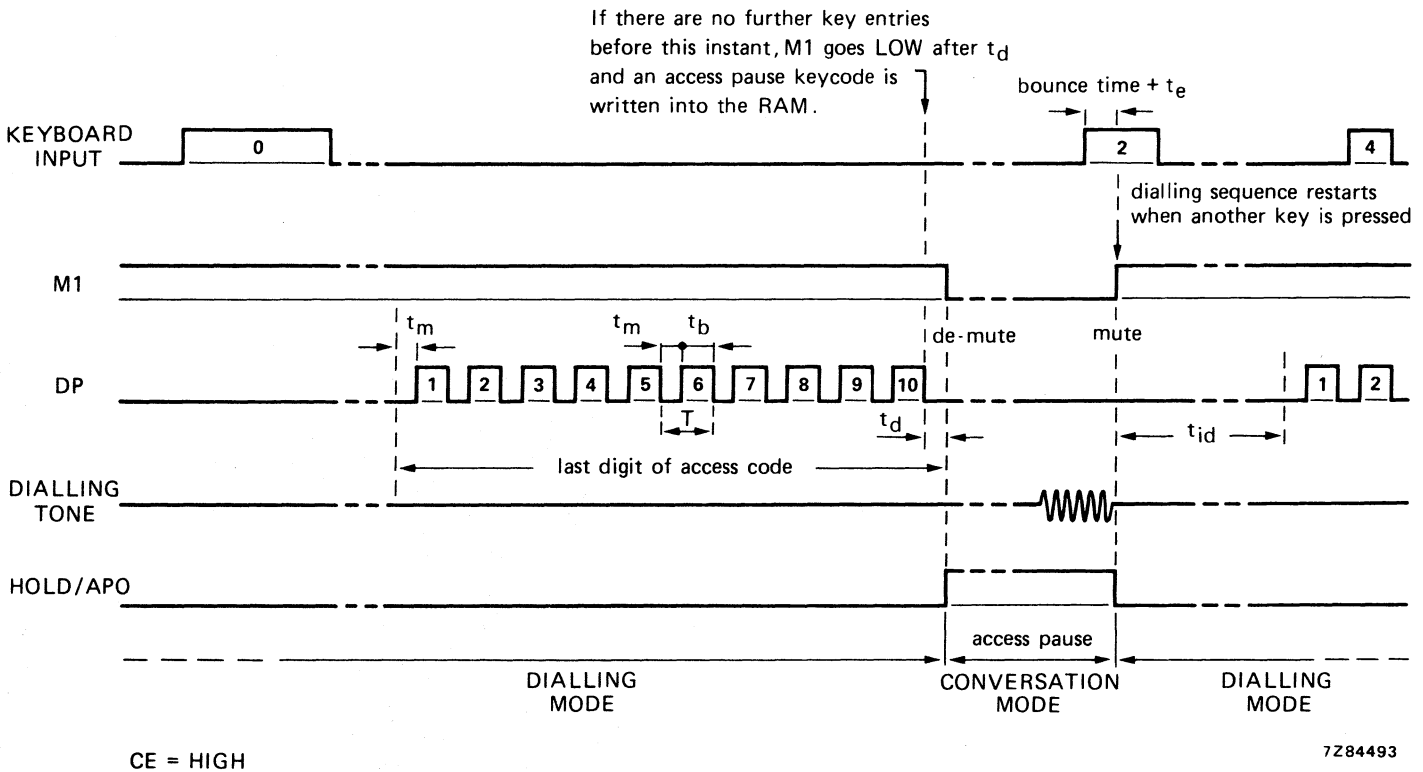
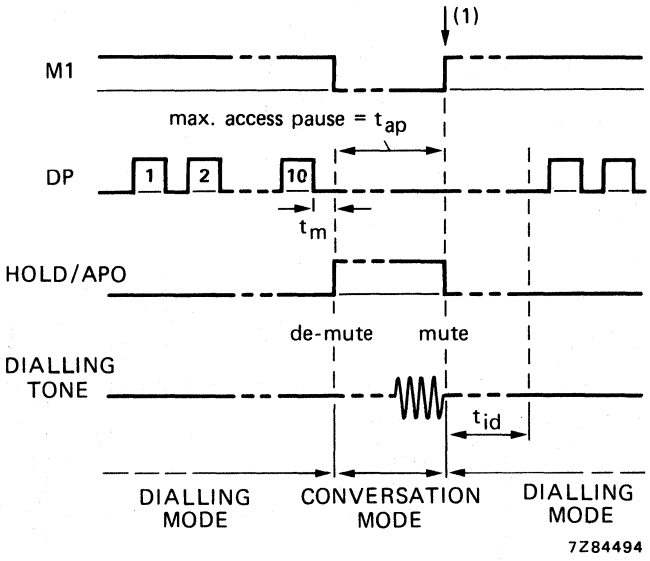


Fig. 9 Dialling sequence showing how an access pause code is automatically stored in the RAM for possible redialling if no further key entries are made until all of the previously entered digits have been transmitted. The dialling sequence continues when another key is pressed.

Access pause regeneration during redial

During original entry, access pause codes can be stored at the appropriate positions in the RAM. During redial the Access Pause Output (HOLD/APO)will go HIGH as soon as an access pause code is read from the RAM, thereby interrupting dialling until HOLD/APO is made LOW again as described above. In this way the normal inter-digit pause with a duration t_{id} can be replaced by a proper access pause. An access pause code is now automatically stored in the RAM during original entry, when M1 goes LOW, after all digits so far entered have been transmitted (see Fig. 6). This occurs between entering of the trunk exchange code and the subscriber code, whilst the access tone is available. Up to two access pauses can be entered into the RAM in this manner. Alternatively, the access pause key (★) can still be pressed to insert (more) access pauses manually (digits + access pauses ≤ 23).
During redial, access pauses will be automatically regenerated.

Three methods of terminating an access pause:
1. Automatically, if the built-in time t_{ap} expires; HOLD/APO then goes LOW.
2. Manually, by pressing the redial key before t_{ap} expires.
3. With an external tone recogniser, by forcing HOLD/APO to LOW or HIGH respectively, for shortening or lengthening an access pause.



(1) a. Access pause (t_{ap}) expires or press redial before end of t_{ap}.

b. HOLD/APO controlled by tone recogniser:
HOLD/APO forced to LOW before t_{ap} expires; access pause $< t_{ap}$
HOLD/APO forced to HIGH after t_{ap} expires; access pause $> t_{ap}$.

Fig. 10 Timing diagram showing Access Pause Reset.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_{DD}	−0,3 to 8 V
Voltage on any pin	V_I	V_{SS} −0,3 to V_{DD} + 0,3 V
Operating ambient temperature range	T_{amb}	−25 to +70 °C
Storage temperature range	T_{stg}	−55 to +125 °C

CHARACTERISTICS

V_{DD} = 3 V; V_{SS} = 0 V; crystal parameters: f_{osc} = 3,58 MHz, R_{Smax} = 100 Ω (note 3); T_{amb} = 25 °C; unless otherwise specified.

	symbol	min.	typ.	max.		conditions
Operating supply voltage	V_{DD}	2,5	3	6	V	T_{amb} = −25 to +70 °C
Standby supply voltage (note 1)	V_{DDO}	1,8	–	6	V	T_{amb} = −25 to +70 °C
Operating supply current	I_{DD}	–	40	–	μA	CE = HIGH; notes 2, 3
	I_{DD}	–	50	100	μA	CE = HIGH; V_{DD} = 6 V; notes 2, 3
Standby supply current	I_{DDO}	–	1	5	μA	CE = LOW; note 2
	I_{DDO}	–	–	2	μA	V_{DD} = 1,8 V; T_{amb} = −25 to +70 °C
Input voltage LOW	V_{IL}	–	–	0,3 V_{DD}		1,8 V ⩽ V_{DD} ⩽ 6 V
Input voltage HIGH	V_{IH}	0,7 V_{DD}	–	–		1,8 V ⩽ V_{DD} ⩽ 6 V
Input leakage current; CE						
LOW	$-I_{IL}$	–	–	50	nA	CE = LOW
HIGH	I_{IH}	–	–	50	nA	CE = HIGH
Pull-up input current M/S	$-I_{IL}$	30	100	300	nA	V_I = V_{SS}
Pull-down input current F01, F02	I_{IH}	30	100	300	nA	V_I = V_{DD}
Matrix keyboard operation						
Keyboard current	I_K	–	10	–	μA	X connected to Y, CE = HIGH
Keyboard 'ON' resistance	R_{KON}	–	–	500	Ω	contact ON; note 4
Keyboard 'OFF' resistance	R_{KOFF}	1	–	–	MΩ	contact OFF; note 4
Other keyboard operation						
Input current for X_n 'ON'	I_{IH}	–	–	30	μA	V_I = 1,5 to 3 V
Input current for Y_n 'ON'	$-I_{IL}$	10	–	–	μA	V_I = 0 to 2,5 V
Input current Y_n	$-I_I$	–	–	0,7	mA	V_I = V_{SS}

Notes

1. V_{DDO} = 1,8 V only for redial.
2. All other inputs and outputs open.
3. Stray capacitance between pins 8 and 9 < 3 pF.
4. Guarantees correct keyboard operation.

CHARACTERISTICS (continued)

	symbol	min.	typ.	max.		conditions
Outputs M1, DP						
sink current	I_{OL}	0,7	1,5	3,2	mA	V_{OL} = 0,5 V
source current	$-I_{OH}$	0,65	1,3	2,7	mA	V_{OH} = 2,5 V
Latch output HOLD/APO						
sink current	I_{OL}	50	130	300	μA	V_{OL} = 0,5 V
source current	$-I_{OH}$	45	110	250	μA	V_{OH} = 2,5 V

TIMING DATA

V_{DD} = 2,5 to 6 V; V_{SS} = 0 V; f_{osc} = 3,579545 MHz

input levels of F01 and F02 (V_{SS} = LOW; V_{DD} = HIGH)		V_{F01}	LOW	HIGH	LOW	HIGH		
		V_{F02}	LOW	HIGH	HIGH	LOW		conditions (note 4)
		symbol				(test mode)		
Dialling pulse frequency	$1/T_{DP}$	f_{DP}	10,13	15,54	19,42	939,2	Hz	note 1
Dialling pulse period	$1/f_{DP}$	T_{DP}	98,7	64,4	51,5	1,073	ms	
Clock pulse frequency	$30 \times f_{DP}$	f_{CL}	303,9	466,1	582,6	27965	Hz	
Break time (note 2)	$3/5 \times T_{DP}$	t_b	59,2	38,6	30,9	0,644	ms	M/S = H; n.c.
Make time (note 2)	$2/5 \times T_{DP}$	t_m	39,5	25,8	20,6	0,429	ms	M/S = H; n.c.
Break time (note 3)	$2/3 \times T_{DP}$	t_b	65,8	42,9	34,6	0,715	ms	M/S = L
Make time (note 3)	$1/3 \times T_{DP}$	t_m	32,9	21,5	17,2	0,358	ms	M/S = L
Inter-digit pause	$8 \times T_{DP}$	t_{id}	790	515	412	8,58	ms	
Reset delay time	$1,6 \times T_{DP}$	t_{rd}	158	103	82,4	1,72	ms	
Access pause time	$32 \times T_{DP}$	t_{ap}	3,16	2,06	1,65	0,034	s	
Prepulse duration	$1/3 \times T_{DP}$	t_d	33	21,5	17,2	0,358	ms	
Debounce time								
min	$4/30 \times T_{DP}$	$t_{e\,min}$	13,2	8,58	6,87	0,143	ms	
max.	$1/6 \times T_{DP}$	$t_{e\,max}$	16,5	10,7	8,58	0,179	ms	
Clock start-up time		$t_{on\,typ}$	4	–	–	–	ms	CE: $V_{SS} \rightarrow V_{DD}$ (note 5)
Initial data entry time (typ.)	$t_{on} + t_e$	t_i	18	14	12	4	ms	

Notes

1. Exactly 10 Hz with 3,5328 MHz crystal.
2. Mark-to-space ratio: 3:2.
3. Mark-to-space ratio: 2:1.
4. In the n.c. (not connected) condition, the input is drawn to the appropriate state by the internal pull-up/pull-down current.
5. Stray capacitance between pins 8 and 9: < 3 pF.

TYPICAL CURVES

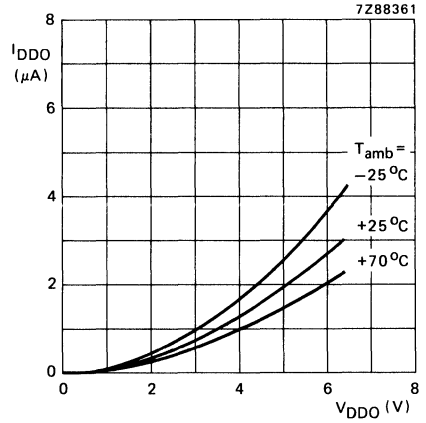


Fig. 11 Standby supply current as a function of standby supply voltage.

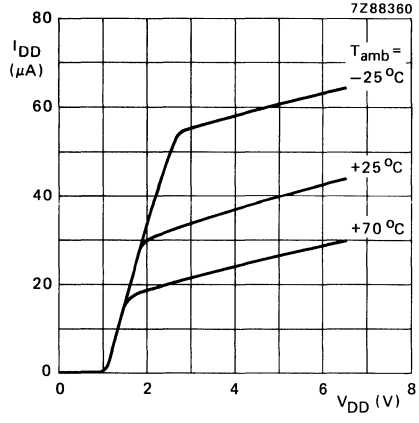


Fig. 12 Operating supply current as a function of operating supply voltage.

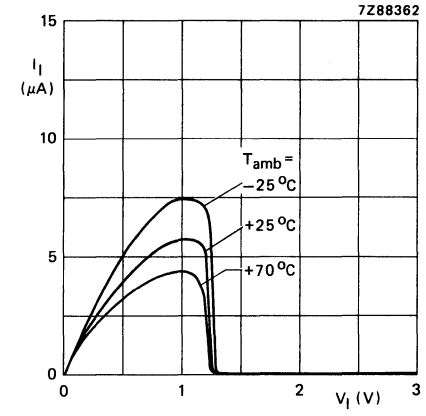


Fig. 13 Pull-down input current as a function of input voltage at V_{DD} = 3 V.

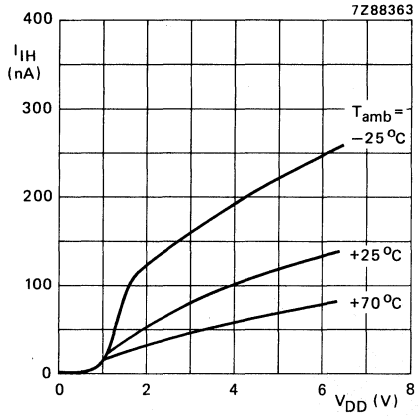


Fig. 14 Pull-down input current as a function of supply voltage at $V_I = V_{DD}$.

TYPICAL CURVES (continued)

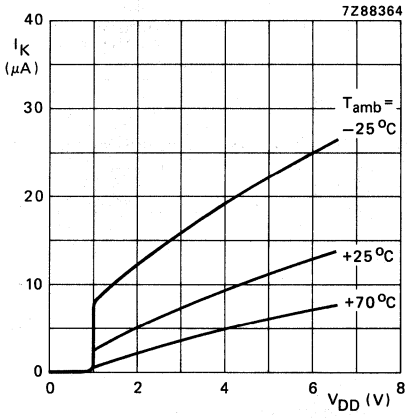


Fig. 15 Keyboard current as a function of supply voltage; X-pins connected to Y-pins.

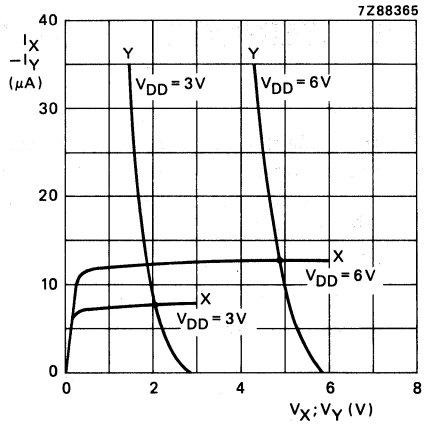


Fig. 16 Keyboard input characteristics at T_{amb} = 25 °C.

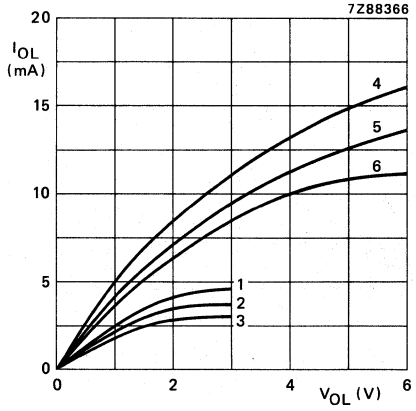


Fig. 17 Output (N-channel) sink characteristics for M1 and DP.

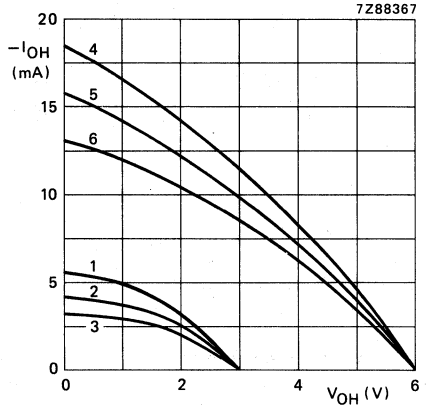


Fig. 18 Output (P-channel) source characteristics for M1 and DP.

Curves for Figs 17 and 18

T_{amb}	V_{DD} = 3 V	V_{DD} = 6 V
−25 °C	1	4
+25 °C	2	5
+70 °C	3	6

C-MOS INTERRUPTED CURRENT-LOOP DIALLING CIRCUIT

The PCD3322 is a single chip silicon-gate C-MOS integrated circuit. It is intended to convert pushbutton keyboard entries into streams of correctly-timed line current interruptions. The input data is derived from a telephone keyboard with a 3 x 4 pushbutton matrix. Numbers with up to 23 digits can be retained in a RAM for redial. A delayed reset is built-in for line power breaks.

The circuit has the following features:

- Operation from 2,5 V to 6 V supply.
- Static standby operation down to 1,8 V.
- Low current consumption; typ. 40 μA.
- Low static standby current; typ. 1 μA.
- On-chip oscillator for 3,58 MHz crystal.
- Fully decoded and debounced inputs for 3 x 4 matrix keyboard.
- All inputs with pull-up/pull-down (except CE).
- 23-digit capacity for redial operation.
- Circuit reset for line power breaks; $>$ 160 ms.
- Dialling pulse frequency: 10 Hz.
- Test pulse frequency: 932 Hz.
- Hold facility for lengthening the inter-digit period.
- Memory overflow possibility (with internally disabled redial.
- All inputs are internally protected against electrostatic charges.
- High input noise immunity.

PACKAGE OUTLINES

PCD3322P: 18-lead DIL; plastic (SOT-102GE).
PCD3322D: 18-lead DIL; ceramic (SOT-133B).

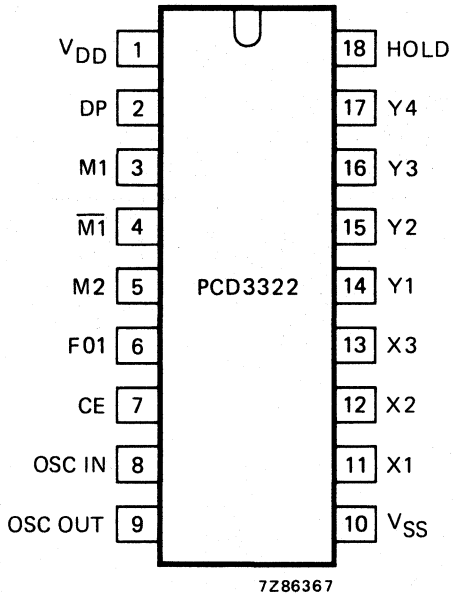


Fig. 1 Pinning diagram.

PINNING

1	V_{DD}	positive supply
10	V_{SS}	negative supply

Inputs

6	F01	the dialling pulse frequency is defined by the logic state of this input
7	CE	Chip Enable; used to initialize the system; to select between the operational mode and the static standby mode; to handle line power breaks.
11	X1	column keyboard inputs with pull-down on chip
12	X2	
13	X3	
14	Y1	row keyboard inputs with pull-up on chip
15	Y2	
16	Y3	
17	Y4	
18	HOLD	interrupts dialling after completion of the current digit or immediately following an inter-digit pause (t_{id}); further keyboard data will be accepted

Outputs

2	DP	Dialling Pulse; drive of the external line switching transistor or relay
3	M1	Muting; normally used for muting during the dialling sequence
4	$\overline{M1}$	inverted output of M1
5	M2	strobe; HIGH during pulsing of each digit, LOW during an inter-digit pause

Oscillator

8	OSC IN	input and output of the on-chip oscillator
9	OSC OUT	

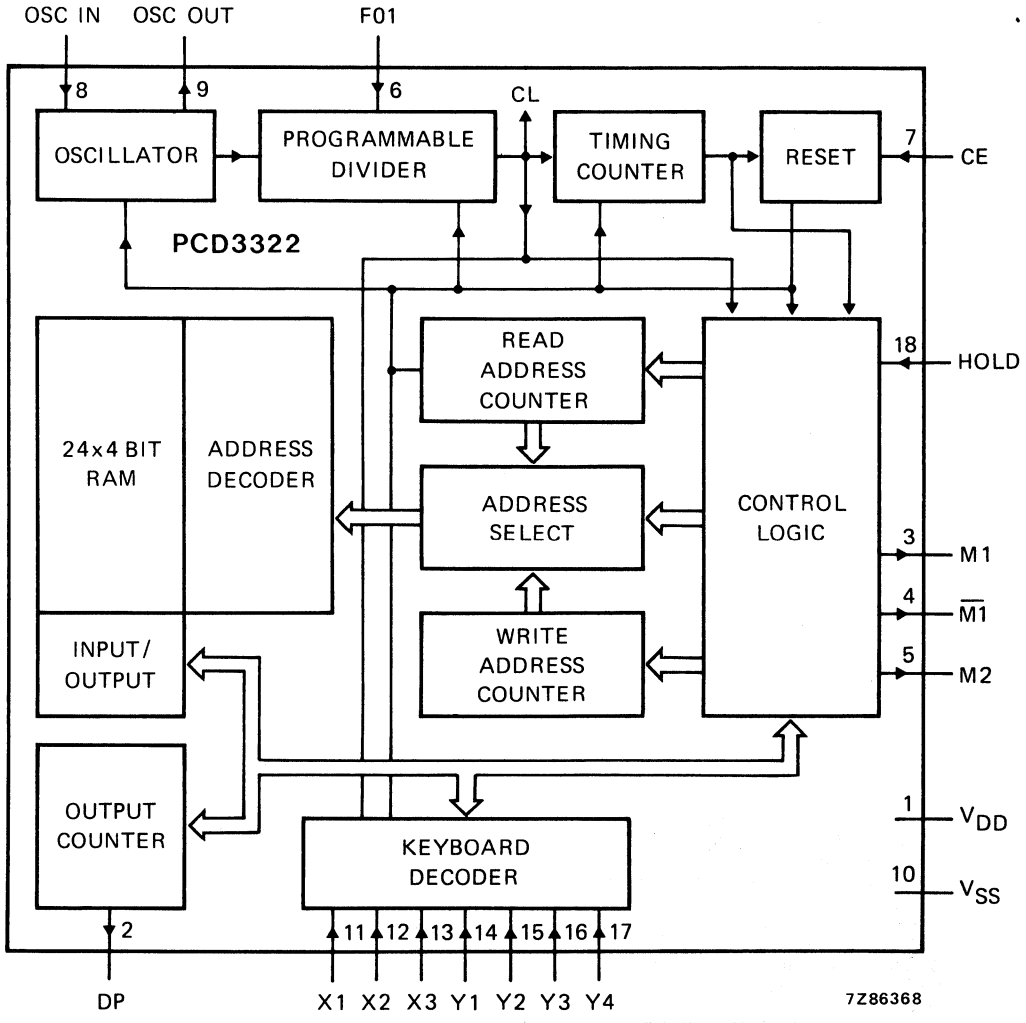


Fig. 2 Block diagram.

FUNCTIONAL DESCRIPTION (see also Fig. 2)

Clock oscillator (OSC IN, OSC OUT)

The time base for the PCD3322 is a crystal controlled on-chip oscillator which is completed only by connecting a crystal between the OSC IN and OSC OUT pins. The oscillator is followed by a frequency divider of which the division ratio can be externally set by input F01 to provide one of two chip system clocks; the 'normal' clock frequency (F01 = LOW) and the test frequency (F01 = HIGH).

Alternatively, the OSC IN input may be driven from an external clock signal.

Chip Enable (CE)

The CE input is used to initialize the chip system.

CE = LOW provides the static standby condition. In this mode the clock oscillator is off and internal registers are clamped reset with the exception of the WRITE ADDRESS COUNTER (WAC). The keyboard input is inhibited, but data previously entered is saved in the RAM.

When CE = HIGH the clock oscillator is operating, the internal registers are enabled and data can be entered from the keyboard.

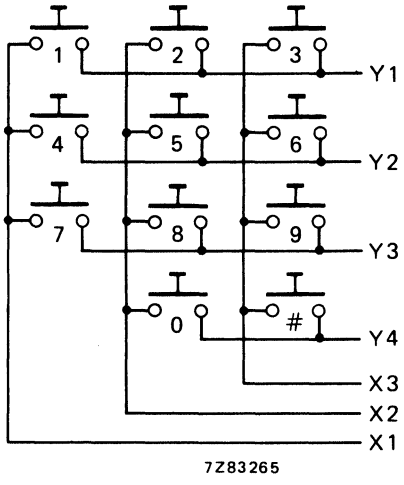
If the CE input is taken to a LOW level for more than the time t_{rd} (see Figs 5 and 6 and timing data) an internal reset pulse will be generated at the end of the t_{rd} period. The system is then in the static standby mode. Short CE pulses of $< t_{rd}$ will not affect the operation of the circuit. No reset pulses are then produced.

Debouncing keyboard entries

The column keyboard inputs to the integrated circuit (X_n) and the row keyboard inputs (Y_n) are for direct connection to a 3 x 4 single contact keyboard matrix (with or without common contact) as shown in Fig.3, or to a double contact keyboard with a common left open (see Fig. 4). An entry is decoded into a 4-bit binary keycode by the keyboard decoder when one column input is connected to one row input or, when one column input is set HIGH and one row input is set LOW. Any other input combinations will be judged to be not valid and will not be accepted. Valid inputs are debounced on the leading and trailing edges as shown in Fig. 5. Keyboard entries are only decoded into 4-bit binary keycodes and written into the RAM if the keyboard contact remains closed for four or five clock pulse periods (entry period t_e). The next keyboard entry will not be accepted until the previously closed contact has been open for three or four clock pulse periods. The one clock pulse period of uncertainty in the debouncing process arises because keyboard entries are not detected until the trailing edge of the first clock pulse after the entry.

Data entry

After each keyboard entry has been debounced and decoded, the keycode is written into the RAM, and the WAC is incremented by one to select the next RAM location where the next keycode will be stored. As each keycode is recalled from the RAM for line pulsing, the READ ADDRESS COUNTER (RAC) is incremented by one to select the RAM location of the next keycode to be recalled. Consequently, the difference between the contents of the WAC and of the RAC represents the number of keycodes that have been written into the RAM but not yet converted into line pulses. If more than 23 keycodes are written into the RAM, memory overflow results and the excess keycode replace the data in the lower numbered RAM locations. In this event, since an erroneous number is stored, automatic redialling is inhibited until the WAC has been reset by the first digit entry of the next telephone call.
If the first pushbutton to be pressed is not redial (#), the WAC is reset during entry time t_e, the corresponding keycode is written into the first RAM location, and the WAC is then incremented by one. If the first pushbutton to be pressed is redial (#), the WAC is not reset and the keycodes stored in the RAM are sequentially recalled and converted into correctly timed dialling pulses at output DP. During redial no keyboard entry will be accepted and stored in the RAM. But, when all in the RAM stored numbers have been pulsed out, new keyboard entry will be accepted, stored in the RAM and converted into correctly timed dialling pulses.



Redial.

Fig. 3 Single contact keyboard.

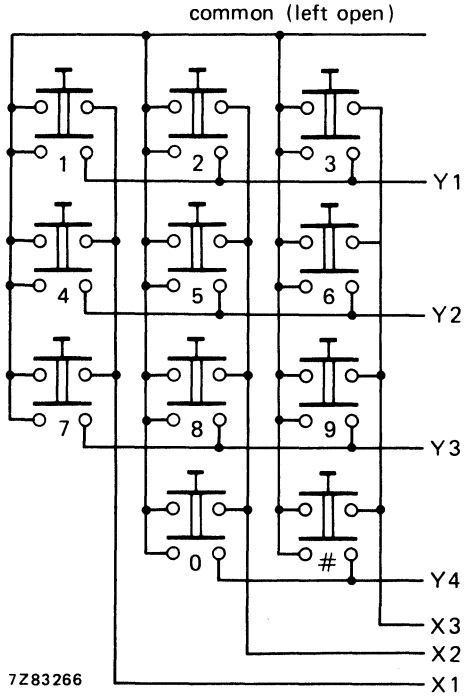


Fig. 4 Double contact keyboard.

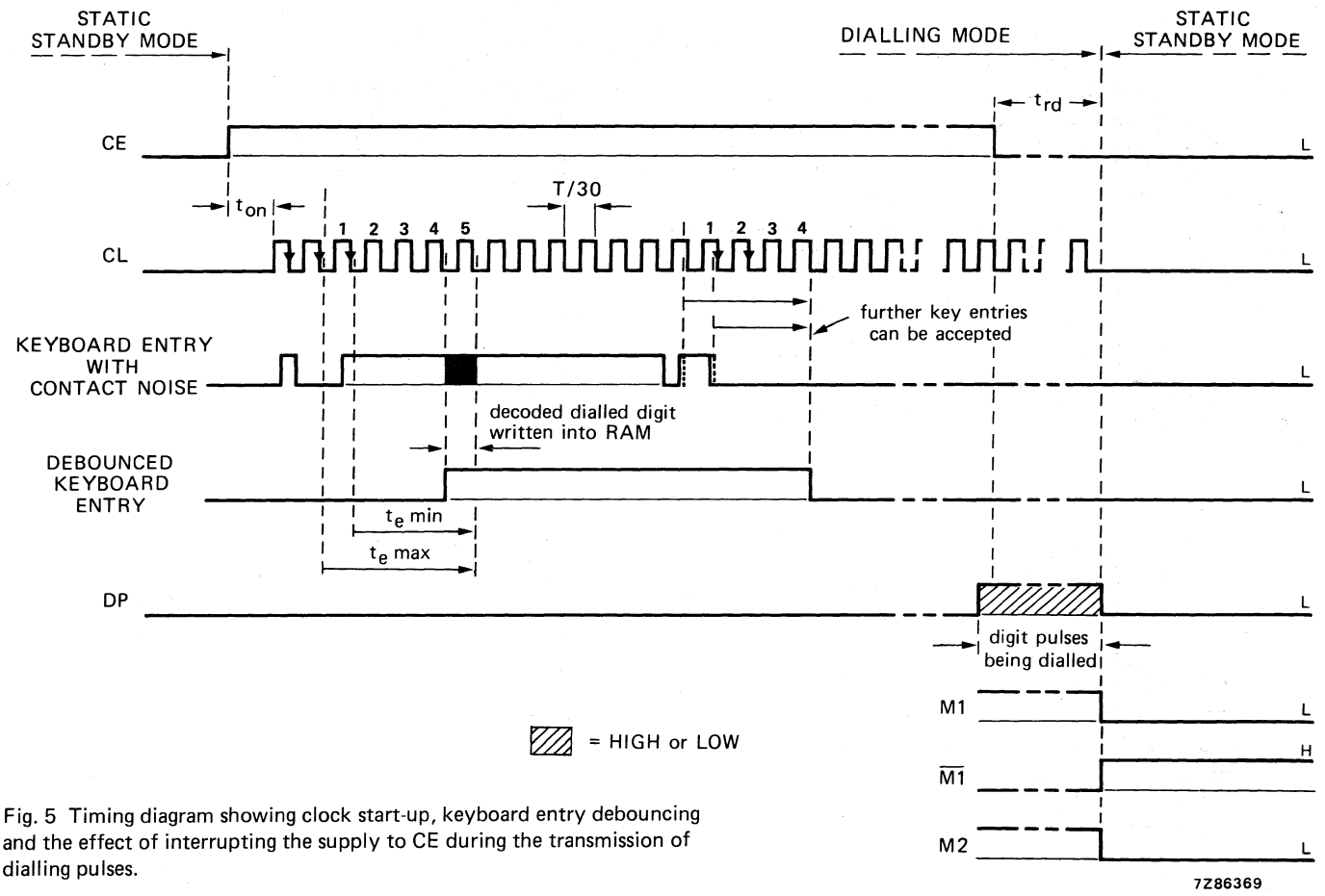


Fig. 5 Timing diagram showing clock start-up, keyboard entry debouncing and the effect of interrupting the supply to CE during the transmission of dialling pulses.

N.B.: CL is an internal signal.

Dialling sequence

The dialling sequence can be initiated under either of the following two conditions:

- The supply to the integrated circuit is derived from the telephone lines via the cradle contacts (power supply before keyboard entry); see Fig. 6.

Then, approximately 4 ms (t_{on}) after CE goes HIGH, the clock pulse generator starts and, ten clock pulse periods (t_d) later, a prepulse with a duration of ten clock pulse periods (t_d) appears at output M1. This prepulse ensures that, if a polarized muting relay with two stable positions is used, it switches to the de-muted position so that the circuit is then in the conversation mode whilst the subscriber awaits the dialling tone. When the first digit of the required number is entered at the keyboard, data entry period t_e commences.

- The supply to the integrated circuit is derived from the telephone lines via the cradle contacts in series with a common keyboard contact (Fig. 7).

When the first digit of the required number is entered at the keyboard, the common keyboard contact connects the line voltage to V_{DD} and CE becomes HIGH. Approximately 4 ms (t_{on}) after CE goes HIGH, the clock pulse-generator starts and data entry period t_e commences. After period t_e, M1 goes HIGH and the pushbutton can be released. The supply to V_{DD} and CE is then maintained via the muting circuit controlled by M1.

The further dialling sequence will be described with the aid of Fig. 6. When the keyboard entry has been decoded and written into the RAM, M1 goes HIGH to mute the telephone and an inter-digit pause (t_{id}) ensues. M2 then goes HIGH, the RAC addresses the RAM and the first keycode is loaded into the register of the output counter which generates the appropriate number of correctly-timed dialling pulses at output DP. When the digit has been pulsed out, M2 goes LOW, the RAC is incremented by one and the procedure repeats until the WAC and RAC contents are equal (all digits pulsed out). Output M1 then goes LOW, the circuit assumes the conversation mode. The circuit reverts to the static standby mode if CE goes LOW for more than the reset delay time (t_{rd} = 1,6 dialling pulse periods) at any time during the conversation or dialling mode (e.g. because the handset is replaced). CE remains LOW although V_{DD} is maintained by a back-up supply (e.g. because an external diode isolates CE from the back-up supply connected to V_{DD}). The RAM retains its contents for subsequent automatic redialling as long as the back-up supply maintains V_{DD} above V_{DDO} = 1,8 V.

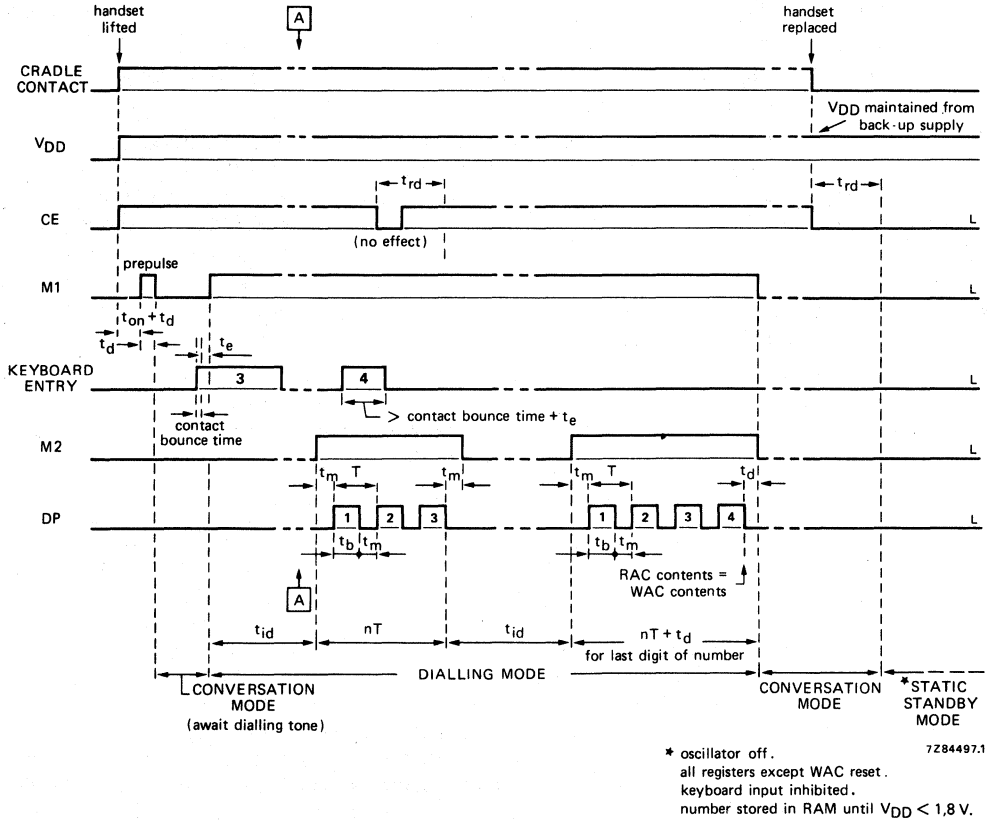


Fig. 6 Timing diagram of dialling sequence with V_{DD} and CE HIGH before keyboard entry (e.g. supply via the cradle contacts).

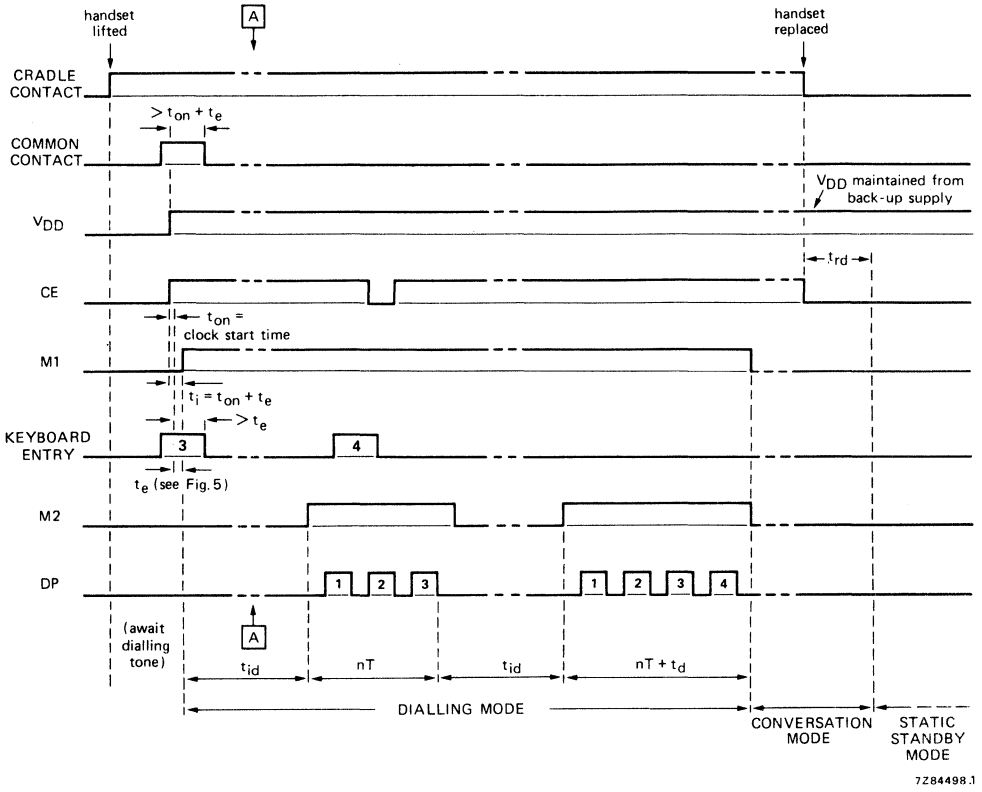


Fig. 7 Timing diagram for initiating the dialling mode with V_{DD} and CE initially supplied via the cradle contacts in series with a common contact on the keyboard. See Fig. 6 for pulse timings after point A.

Hold function

As shown in Fig. 8, the hold function allows the interval between consecutive pulsed digits to be prolonged under the control of external equipment. When the HOLD input is set HIGH, the dialling pulse-train is interrupted as soon as M2 goes LOW to signal that the current digit has been pulsed out. In the hold condition, further keyboard entries will be accepted, debounced, decoded and stored in that RAM. No further keycodes will be read from the RAM and converted into dialling pulses on DP until the HOLD input is set LOW again and an inter-digit pause has elapsed.

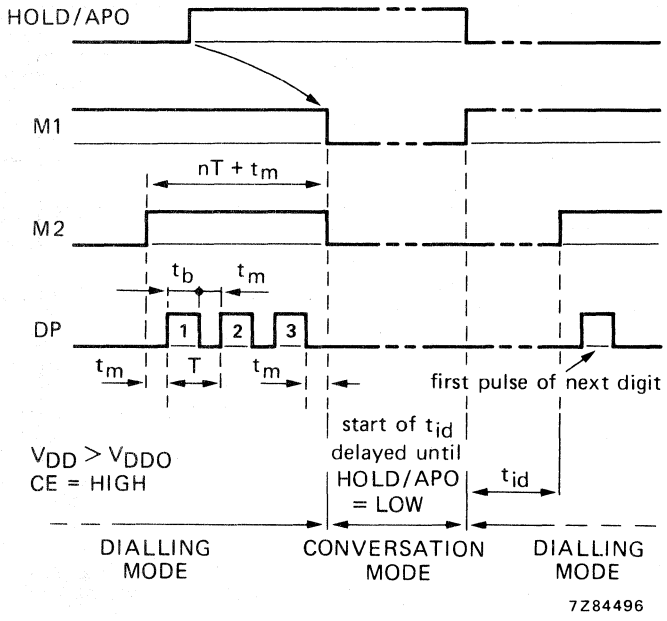


Fig. 8 Timing diagram showing the effect of activating the HOLD input during the transmission of dialling pulses.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_{DD}	−0,3 to 8 V
Voltage on any pin	V_I	V_{SS}−0,3 to V_{DD} + 0,3 V
Operating ambient temperature range	T_{amb}	−25 to + 70 °C
Storage temperature range	T_{stg}	−55 to + 125 °C

CHARACTERISTICS

V_{DD} = 3 V; V_{SS} = 0 V; crystal parameters: f_{osc} = 3,58 MHz, R_{Smax} = 100 Ω (note 3); T_{amb} = 25 °C; unless otherwise specified

	symbol	min.	typ.	max.		conditions
Operating supply voltage	V_{DD}	2,5	3	6	V	T_{amb} = −25 to + 70 °C
Standby supply voltage (note 1)	V_{DDO}	1,8	–	6	V	T_{amb} = −25 to + 70 °C
Operating supply current	I_{DD}	–	40	–	μA	CE = HIGH; notes 2, 3
	I_{DD}	–	50	100	μA	CE = HIGH; V_{DD} = 6 V; notes 2, 3
Standby supply current	I_{DDO}	–	1	5	μA	CE = LOW; note 2
	I_{DDO}	–	–	2	μA	V_{DD} = 1,8 V; T_{amb} = −25 to + 70 °C
Input voltage LOW	V_{IL}	–	–	0,3 V_{DD}		1,8 V ⩽ V_{DD} ⩽ 6 V
Input voltage HIGH	V_{IH}	0,7 V_{DD}	–	–		1,8 V ⩽ V_{DD} ⩽ 6 V
Input leakage current; CE						
LOW	$-I_{IL}$	–	–	50	nA	CE = LOW
HIGH	I_{IH}	–	–	50	nA	CE = HIGH
Pull-down input current F01, HOLD	I_{IH}	30	100	300	nA	$V_I = V_{DD}$
Matrix keyboard operation						
Keyboard current	I_K	–	10	–	μA	X connected to Y, CE = HIGH
Keyboard 'ON' resistance	R_{KON}	–	–	500	Ω	contact ON; note 4
Keyboard 'OFF' resistance	R_{KOFF}	1	–	–	MΩ	contact OFF; note 4
Other keyboard operation						
Input current for X_n 'ON'	I_{IH}	–	–	30	μA	V_I = 1,5 to 3 V
Input current for Y_n 'ON'	$-I_{IL}$	10	–	–	μA	V_I = 0 to 2,5 V
Input current Y_n	$-I_I$	–	–	0,7	mA	$V_I = V_{SS}$
Output sink current	I_{OL}	0,7	1,5	3,2	mA	V_{OL} = 0,5 V
Output source current	$-I_{OH}$	0,65	1,3	2,7	mA	V_{OH} = 2,5 V

Notes

1. V_{DDO} = 1,8 V only for redial.
2. All other inputs and outputs open.
3. Stray capacitance between pins 8 and 9 < 3 pF.
4. Guarantees correct keyboard operation.

TIMING DATA I

V_{DD} = 3 V; V_{SS} = 0 V; crystal parameters: f_{osc} = 3,58 MHz; R_{Smax} = 100 Ω

	symbol	min.	typ.	max.		conditions
Clock start-up time	t_{on}	–	4	–	ms	Figs 6, 7; note 1
Initial data entry time ($t_i = t_{on} + t_e$)	$t_{i\ min}$	–	18	–	ms	F01 = LOW } Fig. 7
	$t_{i\ max}$	–	4	–	ms	F01 = HIGH } Fig. 7

TIMING DATA II (exact values)

V_{DD} = 2,5 to 6 V; V_{SS} = 0 V; f_{osc} = 3,58 MHz

	symbol	F01 = LOW (dialling)	F01 = HIGH (testing)		conditions
Dialling pulse frequency	f_{DP}	10,13	932,2	Hz	note 2
Dialling pulse period; $1/f_{DP}$	T_{DP}	98,7	1,073	ms	Figs 6, 7
Prepulse duration; $1/3 \times T_{DP}$	t_d	33	0,358	ms	Figs 6, 7
Inter-digit pause; $8 \times T_{DP}$	t_{id}	790	8,58	ms	Figs 6, 7
Break time; $3/5 \times T_{DP}$	t_b	59,2	0,644	ms	Fig. 6
Make time; $2/5 \times T_{DP}$	t_m	39,5	0,429	ms	Fig. 6
Debounce time					
min. $4/30 \times T_{DP}$	$t_{e\ min}$	13,2	0,143	ms	Fig. 5
max.; $1/6 \times T_{DP}$	$t_{e\ max}$	16,5	0,179	ms	Fig. 5
Reset delay time; $1,6 \times T_{DP}$	t_{rd}	158	1,7	ms	Figs 5, 6, 7

Notes

1. Stray capacitance between pins 8 and 9 < 3 pF.
2. Exactly 10 Hz and 920 Hz respectively when a 3,5328 MHz crystal is used.

TYPICAL CURVES

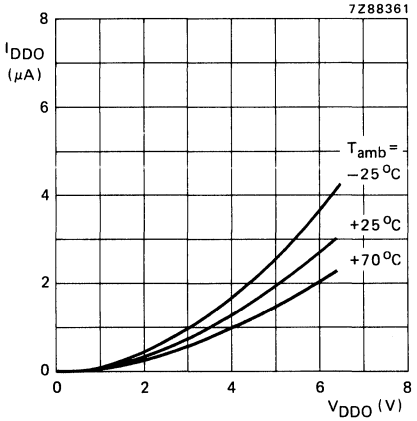


Fig. 9 Standby supply current as a function of standby supply voltage.

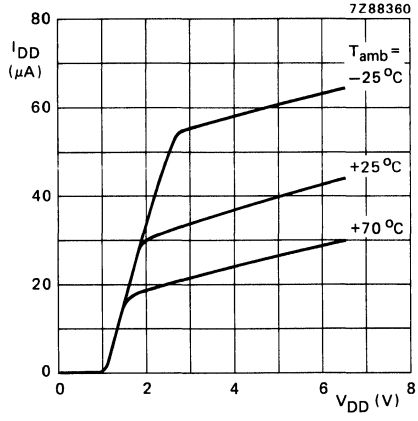


Fig. 10 Operating supply current as a function of operating supply voltage.

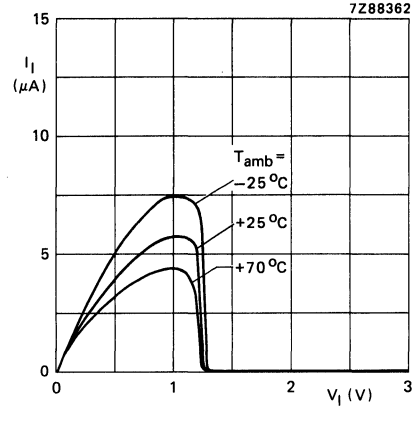


Fig. 11 Pull-down input current as a function of input voltage at V_{DD} = 3 V.

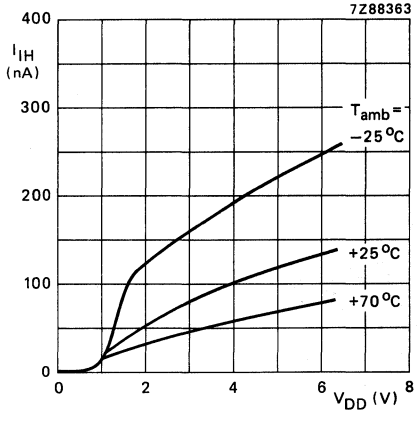


Fig. 12 Pull-down input current as a function of supply voltage at $V_I = V_{DD}$.

TYPICAL CURVES (continued)

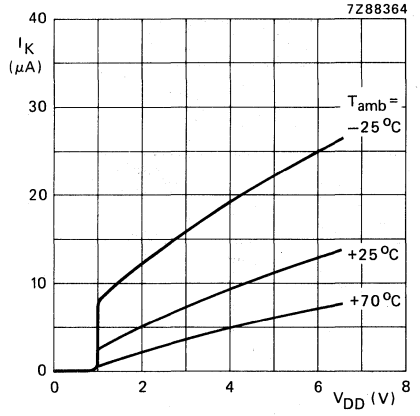


Fig. 13 Keyboard current as a function of supply voltage; X-pins connected to Y-pins.

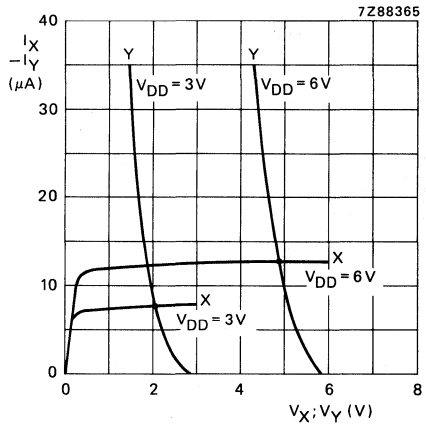


Fig. 14 Keyboard input characteristics at T_{amb} = 25 °C.

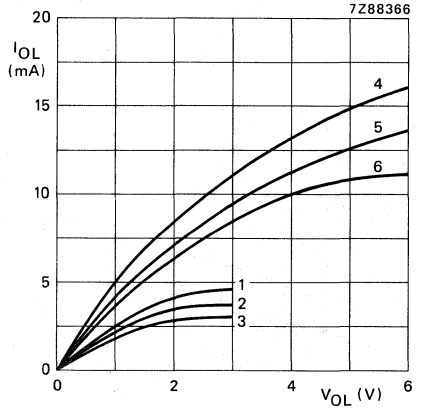


Fig. 15 Output (N-channel) sink characteristics for M1, $\overline{M1}$, M2 and DP.

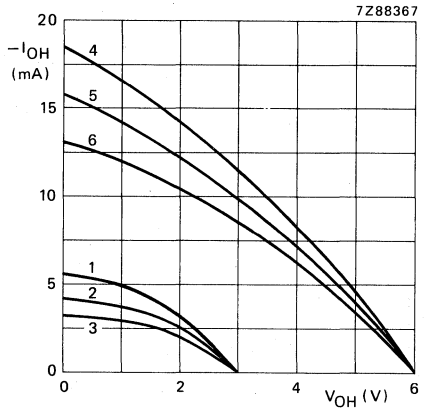


Fig. 16 Output (P-channel) source characteristics for M1, $\overline{M1}$, M2 and DP.

Curves for Figs 15 and 16

T_{amb}	V_{DD} = 3 V	V_{DD} = 6 V
−25 °C	1	4
+25 °C	2	5
+70 °C	3	6

C-MOS INTERRUPTED CURRENT-LOOP DIALLING CIRCUIT

The PCD3323 is a single chip silicon-gate C-MOS integrated circuit. It is intended to convert pushbutton keyboard entries into streams of correctly-timed line current interruptions. The input data is derived from a telephone keyboard with a 3 x 4 pushbutton matrix. Numbers with up to 23 digits can be retained in a RAM for redial. A delayed reset is built-in for line power breaks.

The PCD3323 can regenerate access pauses during redial. During the original entry, access pauses are stored either automatically or via the keyboard. A regenerated access pause can be terminated during redial in three ways: automatically after a built-in time, or via the keyboard, or with an external dial tone recogniser circuit. This makes the circuit very suitable for redial in PABX (Private Automatic Branch Exchange) systems.

The circuit has the following features:

- Operation from 2,5 V to 6 V supply.
- Static standby operation down to 1,8 V.
- Low current consumption; typ. 40 μA.
- Low static standby current; typ. 1 μA.
- On-chip oscillator for 3,58 MHz crystal.
- Fully decoded and debounced inputs for 3 x 4 matrix keyboard.
- 23-digit capacity, including access pauses, for redial operation.
- Memory overflow possibility (with internally disabled redial).
- Selectable dialling pulse frequency: 10 Hz, 16 Hz and 20 Hz.
- Test pulse frequency: 932 Hz.
- Selectable dialling pulse mark/space ratios; 2 : 1 or 3 : 2.
- Selectable inter-digit pause (t_{id}); 8 or 9 times the pulse period (T_{DP}).
- Hold facility for lengthening the inter-digit period.
- Selectable circuit reset for line power breaks; $>$ 160 ms or $>$ 320 ms (10 Hz dialling pulse frequency).
- Access pause generation automatically or via the keyboard.
- Access pause reset:
  automatically after 3 s or 6 s (10 Hz dialling pulse frequency),
  via the keyboard,
  with external tone recogniser.
- All inputs with pull-up/pull-down (except CE).
- All inputs are internally protected against electrostatic charges.
- High input noise immunity.

PACKAGE OUTLINES

PCD3323P : 28-lead DIL; plastic (SOT-117).
PCD3323D: 28-lead DIL; ceramic (SOT-135A).
PCD3323T: 28-lead flat pack; plastic (SO-28; SOT-136A).

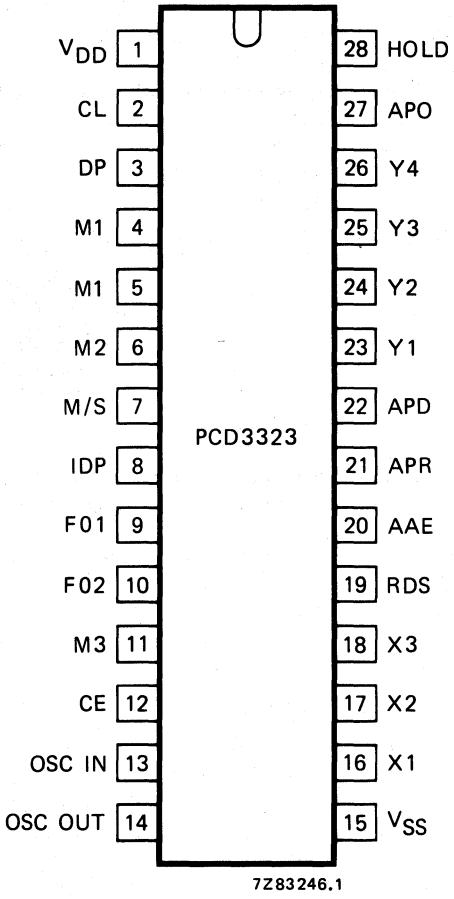


Fig. 1 Pinning diagram.

PINNING

1	V_{DD}	positive supply
15	V_{SS}	negative supply

Inputs

7	M/S	controls the mark-to-space ratio of the line pulses
8	IDP	Inter-Digit-Pause; this occurs before each digit appears at the line output; the duration (t_{id}) can be controlled with this pin
9	F01	the dialling pulse frequency is defined by the logic state of these two inputs
10	F02	
12	CE	Chip Enable; used to initialize the system; to select between the operational mode and the static standby mode; to handle line power breaks
16	X1	column keyboard inputs with pull-down on chip
17	X2	
18	X3	
19	RDS	Reset Delay Selection; delay select for chip enable (CE) activity.

20	AAE	Automatic Access Pause Enable; AAE = HIGH: the circuit generates a maximum of two automatic pauses; AAE = LOW: only manual pauses (via keyboard) are possible
21	APR	Access Pause Reset; when any external circuit makes APR = HIGH, a current access pause will be terminated
22	APD	Access Pause Delay; selects the maximum duration of an access pause if no external Access Pause Reset appears.
23	Y1	row keyboard inputs with pull-up on chip
24	Y2	
25	Y3	
26	Y4	
28	HOLD	interrupts dialling after completion of the current digit or immediately during an inter-digit pause (t_{id}); further keyboard data will be accepted

Outputs

2	CL	output of the internal system clock; external forcing is possible for frequencies not selectable with F01/F02
3	DP	Dialling Pulse; drive of the external line switching transistor or relay
4	M1	Muting; normally used for muting during the dialling sequence
5	$\overline{M1}$	inverted output of M1
6	M2	strobe; HIGH during pulsing of each digit, LOW during an inter-digit pause
11	M3	AND function, with $\overline{DP}$ and M1 as input, for direct drive of a switching transistor for dialling pulses and muting
27	APO	Access Pause Output; this output will go HIGH when an access pause code is read from the memory during pulsing.

Oscillator

13	OSC IN	input and output of the on-chip oscillator
14	OSC OUT	

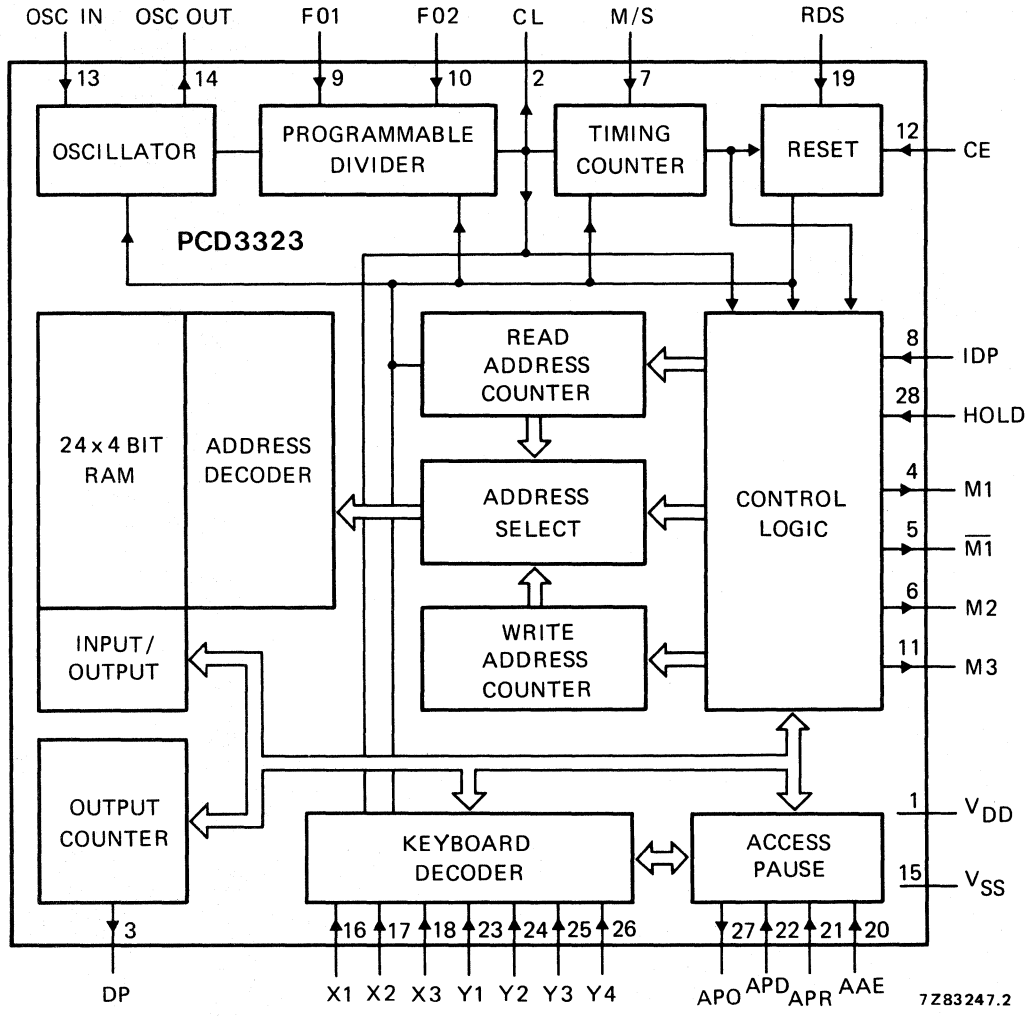


Fig. 2 Block diagram.

FUNCTIONAL DESCRIPTION (see also Fig. 2)

Clock oscillator (OSC IN, OSC OUT)

The time base for the PCD3323 is a crystal controlled on-chip oscillator which is completed only by connecting a crystal between the OSC IN and OSC OUT pins. The oscillator is followed by a frequency divider of which the division ratio can be externally set (F01 and F02) to provide one of four chip system clocks; three 'normal' clock frequencies and one higher test frequency.
The system clock is available on pin CL and can be used for external logic. External forcing of CL is possible for frequencies which are not selectable with F01/F02.
Alternatively, the OSC IN input may be driven from an external clock signal.

Chip Enable (CE)

The CE input is used to initialize the chip system.

CE = LOW provides the static standby condition. In this mode the clock oscillator is off and internal registers are clamped reset with the exception of the WRITE ADDRESS COUNTER (WAC). The keyboard input is inhibited, but data previously entered is saved in the RAM.

When CE = HIGH the clock oscillator is operating, the internal registers are enabled and data can be entered from the keyboard.

If the CE input is taken to a LOW level for more than the time t_{rd} (see Figs 5 and 6 and timing data) an internal reset pulse will be generated at the end of the t_{rd} period. The system is then in the static standby mode. Short CE pulses of $< t_{rd}$ will not affect the operation of the circuit. No reset pulses are then produced. The t_{rd} pulse duration is selected by the RDS input.

Debouncing keyboard entries

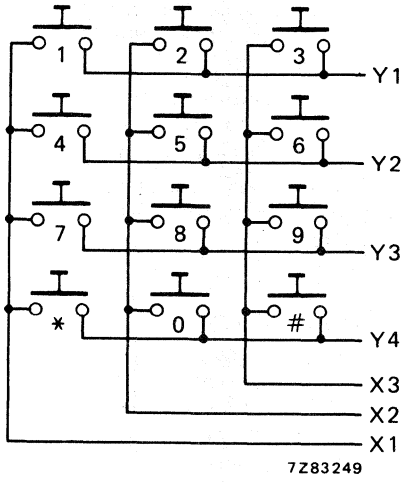
The column keyboard inputs to the integrated circuit (X_n) and the row keyboard inputs (Y_n) are for direct connection to a 3 x 4 single contact keyboard matrix (with or without common contact) as shown in Fig. 3, or to a double contact keyboard with a common left open (see Fig. 4). An entry is decoded into a 4-bit binary keycode by the keyboard decoder when one column input is connected to one row input or, when one column input is set HIGH and one row input is set LOW. Any other input combinations will be judged to be not valid and will not be accepted. Valid inputs are debounced on the leading and trailing edges as shown in Fig. 5. Keyboard entries are only decoded into 4-bit binary keycodes and written into the RAM if the keyboard contact remains closed for four or five clock pulse periods (entry period t_e). The next keyboard entry will not be accepted until the previously closed contact has been open for three or four clock pulse periods. The one clock pulse period of uncertainty in the debouncing process arises because keyboard entries are not detected until the trailing edge of the first clock pulse after the entry.

Data entry

After each keyboard entry has been debounced and decoded, the keycode is written into the RAM, and the WAC is incremented by one to select the next RAM location where the next keycode will be stored. As each keycode is recalled from the RAM for line pulsing, the READ ADDRESS COUNTER (RAC) is incremented by one to select the RAM location of the next keycode to be recalled. Consequently, the difference between the contents of the WAC and of the RAC reprents the number of keycodes that have been written into the RAM but not yet converted into line pulses. If more than 23 keycodes are written into the RAM, memory overflow results and the excess keycode replace the data in the lower numbered RAM locations. In this event, since an erroneous number is stored, automatic redialling is inhibited until the WAC has been reset by the first digit entry of the next telephone call.

If the first pushbutton to be pressed is not redial (#), the WAC is reset during entry time t_e, the corresponding keycode is written into the first RAM location, and the WAC is then incremented by one. If the first pushbutton to be pressed is redial (#), the WAC is not reset and the keycodes stored in the RAM are sequentially recalled and converted into correctly timed dialling pulses at output DP.

If the redial pushbutton (#) is operated again during the redialling sequence it will be decoded as an Access Pause Reset. This function will be described later during the description of the access pause system of the PCD3323. During redial no keyboard entry will be accepted and stored in the RAM. But, when all in the RAM stored numbers have been pulsed out, new keyboard entry will be accepted, stored at the RAM position after the last digit code of the original entry and converted into correctly timed dialling pulses.



★ Access pause set.

Redial or Access Pause Reset.

Fig. 3 Single contact keyboard.

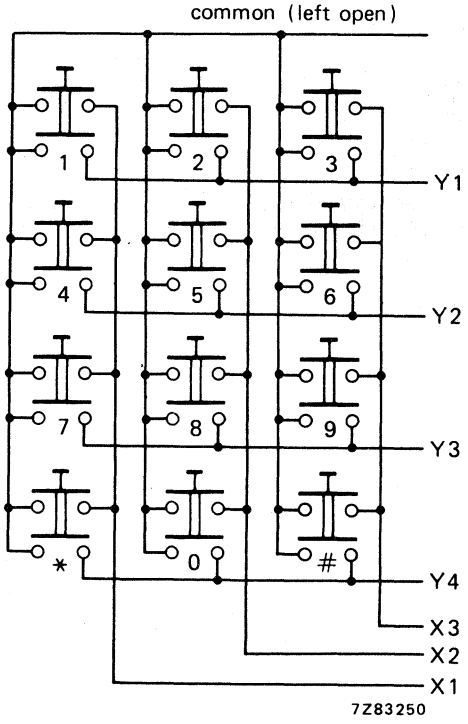


Fig. 4 Double contact keyboard.

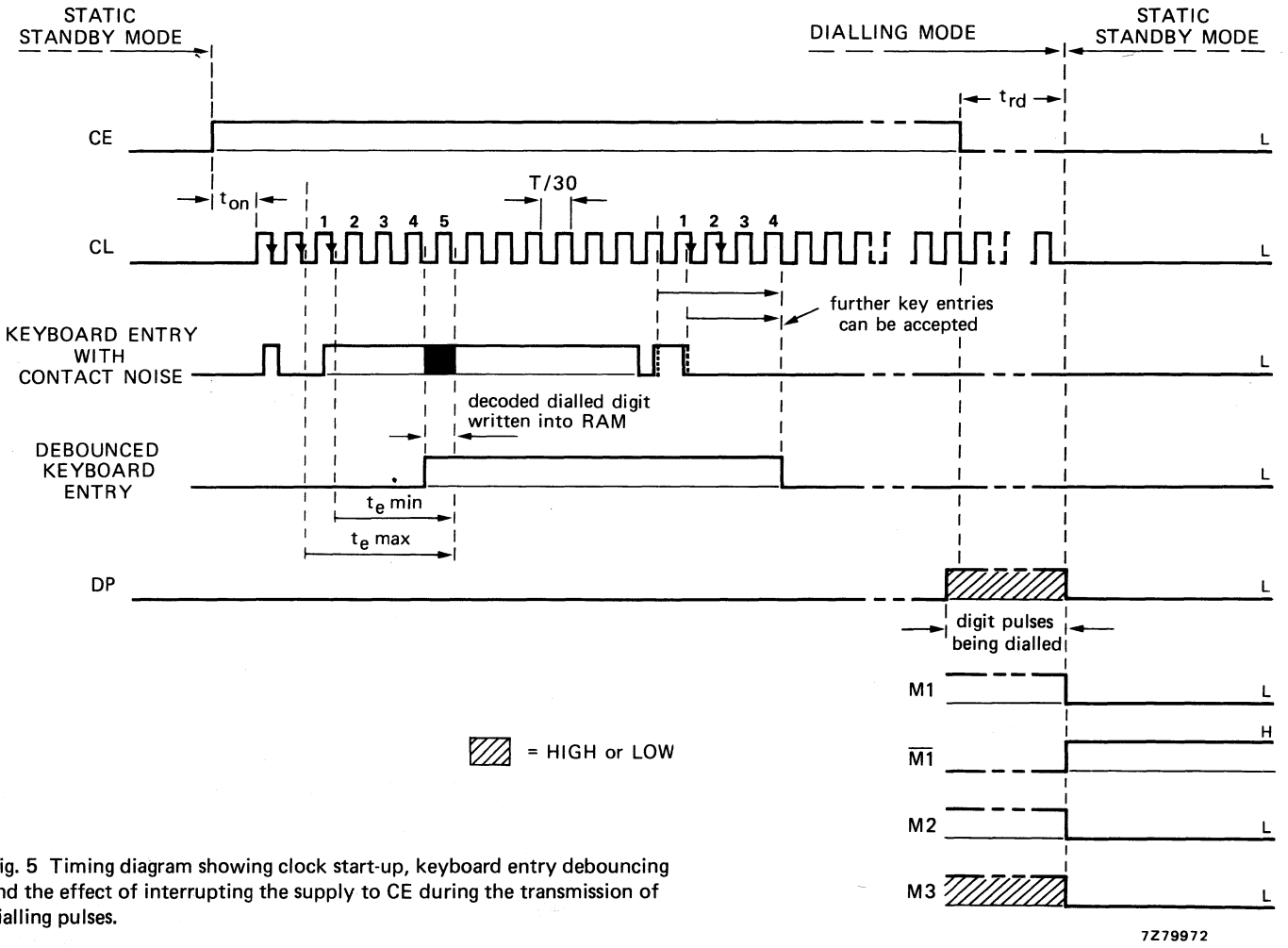


Fig. 5 Timing diagram showing clock start-up, keyboard entry debouncing and the effect of interrupting the supply to CE during the transmission of dialling pulses.

Dialling sequence

The dialling sequence can be initiated under either of the following two conditions:

- The supply to the integrated circuit is derived from the telephone lines via the cradle contacts (power supply before keyboard entry); see Fig. 6.

Then, approximately 4 ms (t_{on}) after CE goes HIGH, the clock pulse generator starts and, ten clock pulse periods (t_d) later, a prepulse with a duration of ten clock pulse periods (t_d) appears at outputs M1 and M3. This prepulse ensures that, if a polarized muting relay with two stable positions is used, it switches to the de-muted position so that the circuit is then in the conversation mode whilst the subscriber awaits the dialling tone. When the first digit of the required number is entered at the keyboard, data entry period t_e commences.

- The supply to the integrated circuit is derived from the telephone lines via the cradle contacts in series with a common keyboard contact (Fig. 7).

When the first digit of the required number is entered at the keyboard, the common keyboard contact connects the line voltage to V_{DD} and CE becomes HIGH. Approximately 4 ms (t_{on}) after CE goes HIGH, the clock pulse generator starts and data entry period t_e commences. After period t_e, M1 goes HIGH and the pushbutton can be released. The supply to V_{DD} and CE is then maintained via the muting circuit controlled by M1.

The further dialling sequence will be described with the aid of Fig. 6. When the keyboard entry has been decoded and written into the RAM, M1 goes HIGH to mute the telephone and an inter-digit pause (t_{id}) ensues. M2 then goes HIGH, the RAC addresses the RAM and the first keycode is loaded into the register of the output counter which generates the appropriate number of correctly-timed dialling pulses at outputs DP and M3. When the digit has been pulsed out, M2 goes LOW, the RAC is incremented by one and the procedure repeats until the WAC and RAC contents are equal (all digits pulsed out). Output M1 then goes LOW, the circuit assumes the conversation mode. The circuit reverts to the static standby mode if CE goes LOW for more than the reset delay time (t_{rd} = 1,6 or 3,2 dialling pulse periods) at any time during the conversation or dialling mode (e.g. because the handset is replaced). CE remains LOW although V_{DD} is maintained by a back-up supply (e.g. because an external diode isolates CE from the back-up supply connected to V_{DD}). The RAM retains its contents for subsequent automatic redialling as long as the back-up supply maintains V_{DD} above V_{DDO} = 1,8 V.

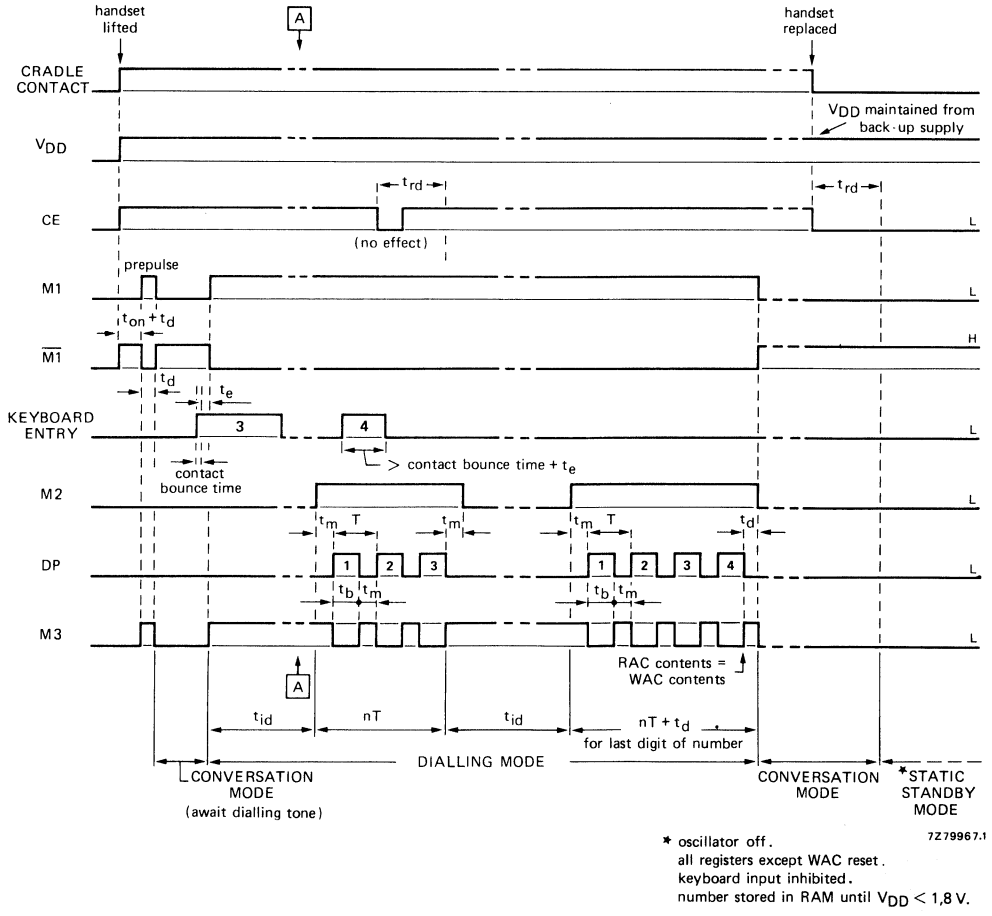


Fig. 6 Timing diagram of dialling sequence with V_{DD} and CE HIGH before keyboard entry (e.g. supply via the cradle contacts).

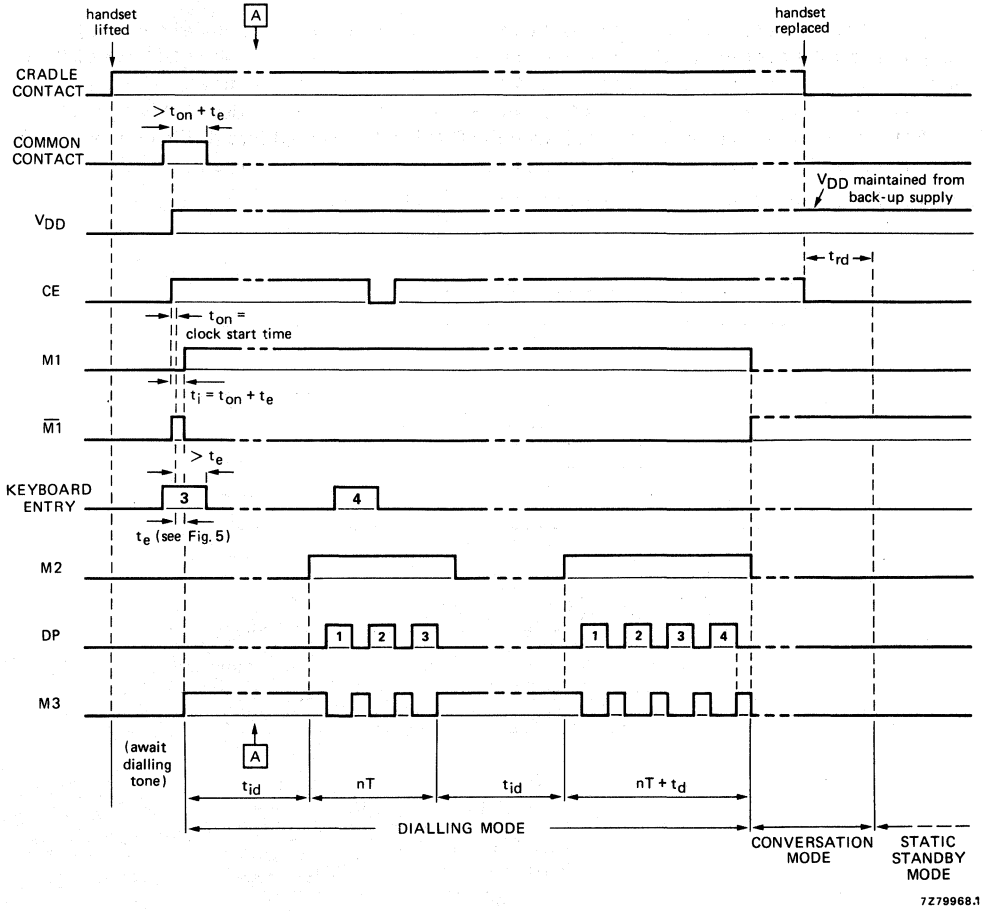


Fig. 7 Timing diagram for initiating the dialling mode with V_{DD} and CE initially supplied via the cradle contacts in series with a common contact on the keyboard. See Fig. 6 for pulse timings after point A.

Hold function

As shown in Fig. 8, the hold function allows the interval between consecutive pulsed digits to be prolonged under the control of external equipment. When the HOLD input is set HIGH, the dialling pulse-train is interrupted as soon as M2 goes LOW to signal that the current digit has been pulsed out. In the hold condition, further keyboard entries will be accepted, debounced, decoded and stored in that RAM. No further keycodes will be read from the RAM and converted into dialling pulses on M3 and DP until the HOLD input is set LOW again and an inter-digit pause has elapsed.

HOLD can be controlled by the Access Pause Output (see next section).

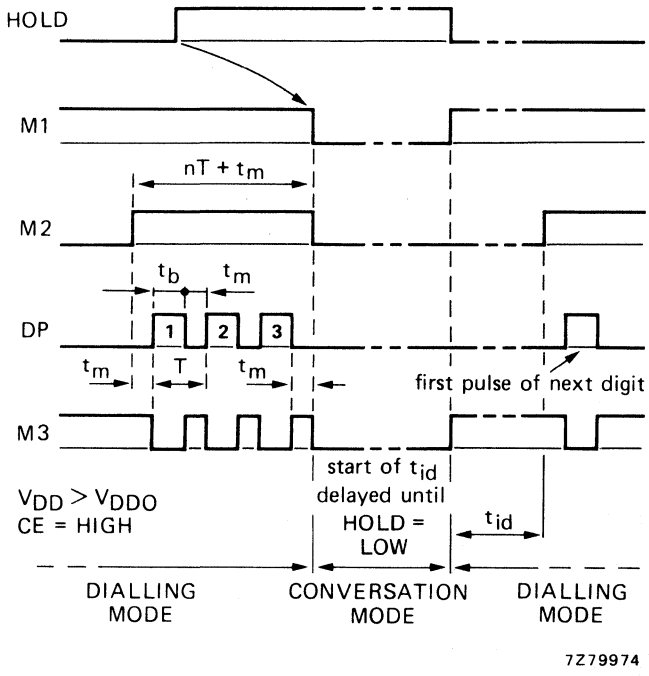


Fig. 8 Timing diagram showing the effect of activating the HOLD input during the transmission of dialling pulses.

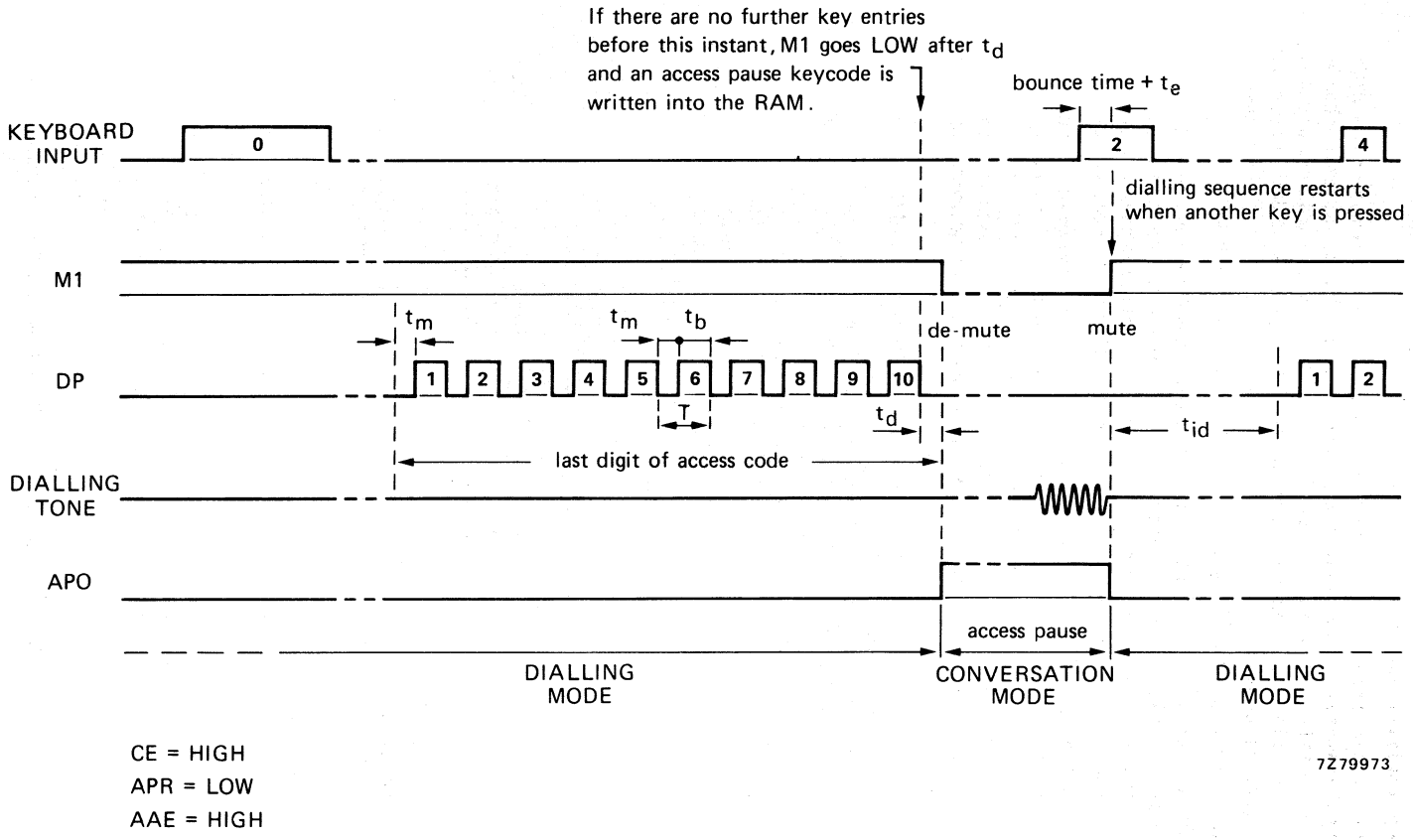


Fig. 9 Dialling sequence showing how an access pause code is automatically stored in the RAM for possible redialling if no further key entries are made until all of the previously entered digits have been transmitted. The dialling sequence continues when another key is pressed.

Access pause regeneration during redial

During original entry, access pause codes can be stored at the appropriate positions in the RAM. During redial the Access Pause Output (APO) will go HIGH as soon as an access pause code is read from the RAM. This can be used to make HOLD = HIGH, thereby interrupting dialling until HOLD is made LOW again as described above. In this way the normal inter-digit pause with a duration t_{id} can be replaced by a proper access pause.

Access pause codes can be stored in two ways:

- *Manually,* with AAE and APR both LOW. In this case access pause codes can only be stored by pressing the access pause key (★) between entering the trunk exchange code and the subscriber code, or at any other moment an access pause is required. The number of access pauses that can be inserted in this manner is only limited by the capacity of the RAM (digits + access pauses ⩽ 23).
- *Automatically,* with AAE = HIGH and APR = LOW (see Fig. 9). An access pause code is now automatically stored in the RAM during original entry, when M1 goes LOW, after all digits so far entered have been transmitted (see Fig. 6). This occurs between entering of the trunk exchange code and the subscriber code, whilst the access tone is available. Up to two access pauses can be entered into the RAM in this manner. Alternatively, the access pause key can still be pressed to insert (more) access pauses manually.

During redial, access pauses will be regenerated only if APR = LOW and with APO connected to HOLD; they can be terminated in three ways (see Fig. 10 and next page).

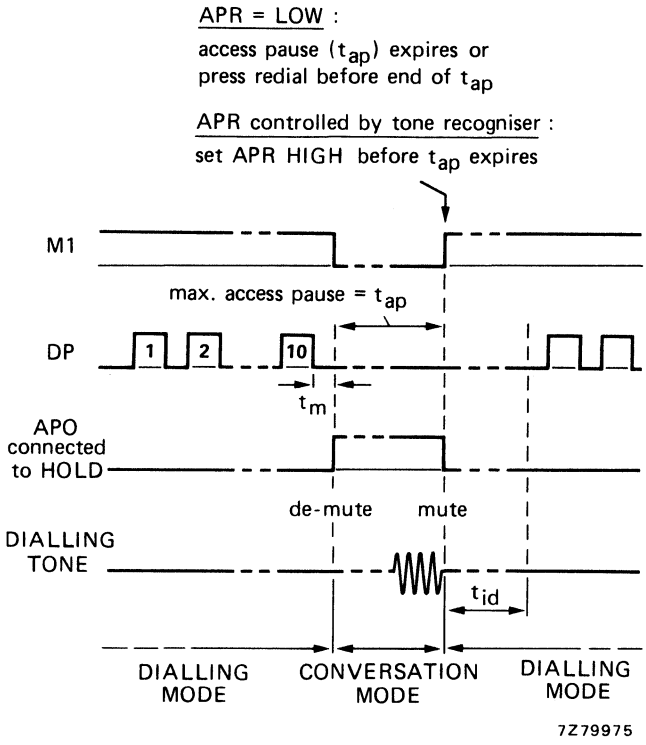


Fig. 10 Timing diagram showing Access Pause Reset for APR = LOW or APR is controlled by tone recogniser.

Three methods of terminating an access pause:

1. Automatically, if the built-in time t_{ap} expires; APO then goes LOW; t_{ap} can be set to one of two values with the Access Pause Delay (APD) select input.
2. Manually, by pressing the redial key before t_{ap} expires.
3. By making APR = HIGH before t_{ap} expires, with an external tone recogniser (see Fig. 11).

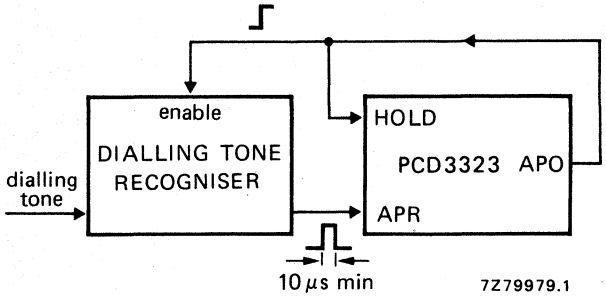


Fig. 11 Circuit for automatic termination of an access pause during redialling by using a tone recogniser to set APR to HIGH for more than 10 μs.

Access pauses longer than t_{ap} can be obtained by connecting APO to HOLD via a latching device. Figure 12 shows a tone recogniser circuit, which automatically terminates access pauses upon receipt of the access tone, whether this is before or after t_{ap} expires.

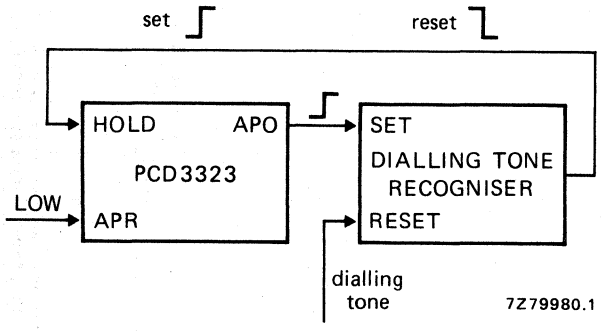


Fig. 12 Circuit for automatically shortening or lengthening an access pause under the control of a tone recogniser. For timing diagram see Fig. 13.

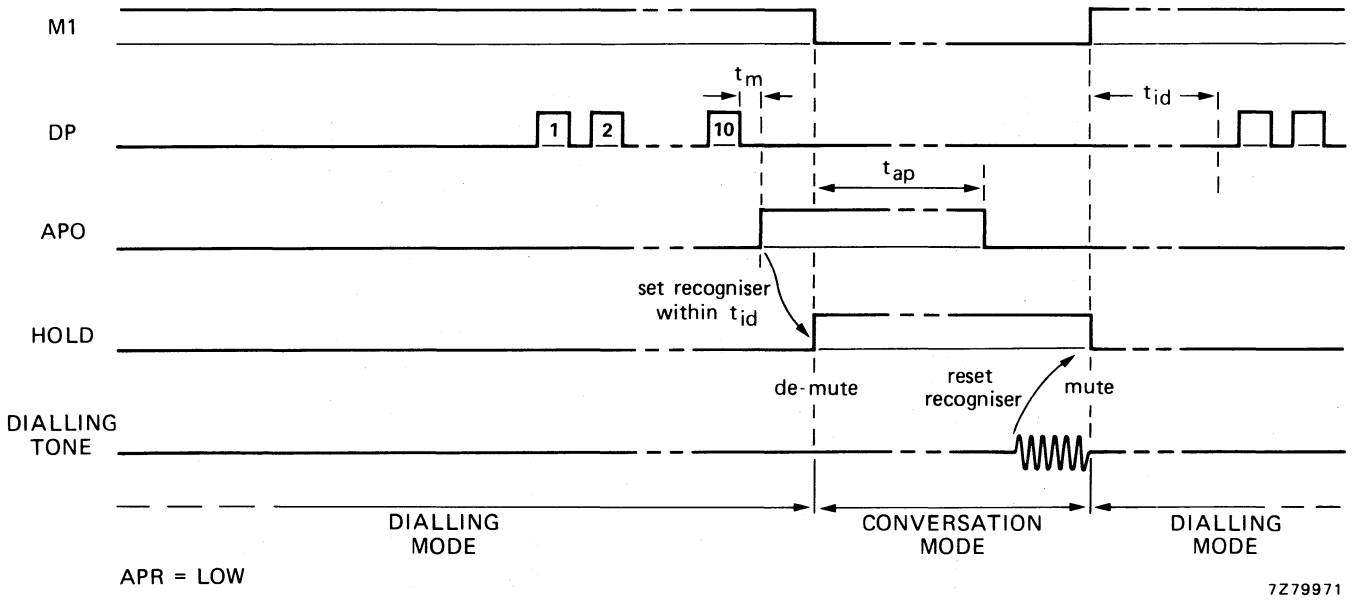


Fig. 13 Timing diagram showing automatic shortening or lengthening an access pause; for the circuit see Fig. 12.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_{DD}	−0,3 to 8 V
Voltage on any pin	V_I	V_{SS}−0,3 to V_{DD} + 0,3 V
Operating ambient temperature range	T_{amb}	−25 to + 70 °C
Storage temperature range	T_{stg}	−55 to + 125 °C

CHARACTERISTICS

V_{DD} = 3 V; V_{SS} = 0 V; crystal parameters: f_{osc} = 3,58 MHz, R_{Smax} = 100 Ω (note 3); T_{amb} = 25 °C; unless otherwise specified

	symbol	min.	typ.	max.		conditions
Operating supply voltage	V_{DD}	2,5	3	6	V	T_{amb} = −25 to + 70 °C
Standby supply voltage (note 1)	V_{DDO}	1,8	–	6	V	T_{amb} = −25 to + 70 °C
Operating supply current	I_{DD}	–	40	–	μA	CE = HIGH; notes 2, 3
	I_{DD}	–	50	100	μA	CE = HIGH; V_{DD} = 6 V; notes 2, 3
Standby supply current	I_{DDO}	–	1	5	μA	CE = LOW; note 2
	I_{DDO}	–	–	2	μA	V_{DD} = 1,8 V; T_{amb} = −25 to + 70 °C
Input voltage LOW	V_{IL}	–	–	0,3 V_{DD}		1,8 V ⩽ V_{DD} ⩽ 6 V
Input voltage HIGH	V_{IH}	0,7 V_{DD}	–	–		1,8 V ⩽ V_{DD} ⩽ 6 V
Input leakage current; CE						
LOW	$-I_{IL}$	–	–	50	nA	CE = LOW
HIGH	I_{IH}	–	–	50	nA	CE = HIGH
Pull-up input current M/S, APR	$-I_{IL}$	30	100	300	nA	V_I = V_{SS}
Pull-down input current IDP, F01, F02, HOLD, AAE, ADP, RDS	I_{IH}	30	100	300	nA	V_I = V_{DD}
Matrix keyboard operation						
Keyboard current	I_K	–	10	–	μA	X connected to Y, CE = HIGH
Keyboard 'ON' resistance	R_{KON}	–	–	500	Ω	contact ON; note 4
Keyboard 'OFF' resistance	R_{KOFF}	1	–	–	MΩ	contact OFF; note 4
Other keyboard operation						
Input current for X_n 'ON'	I_{IH}	–	–	30	μA	V_I = 1,5 to 3 V
Input current for Y_n 'ON'	$-I_{IL}$	10	–	–	μA	V_I = 0 to 2,5 V
Input current Y_n	$-I_I$	–	–	0,7	mA	V_I = V_{SS}

Notes

1. V_{DDO} = 1,8 V only for redial.
2. All other inputs and outputs open.
3. Stray capacitance between pins 13 and 14 < 3 pF.
4. Guarantees correct keyboard operation.

CHARACTERISTICS (continued)

	symbol	min.	typ.	max.		conditions
Outputs M1, $\overline{M1}$, M2, M3, DP						
sink current	I_{OL}	0,7	1,5	3,2	mA	V_{OL} = 0,5 V
source current	$-I_{OH}$	0,65	1,3	2,7	mA	V_{OH} = 2,5 V
Outputs CL, APO						
sink current	I_{OL}	50	130	300	μA	V_{OL} = 0,5 V
source current	$-I_{OH}$	45	110	250	μA	V_{OH} = 2,5 V

TIMING DATA

V_{DD} = 3 V; V_{SS} = 0 V; f_{osc} = 3,58 MHz

	symbol	min.	typ.	max.		conditions
Clock start-up time	t_{on}	–	4	–	ms	CE: $V_{SS} \rightarrow V_{DD}$ (note)
APR-hold time	t_{APRH}	10	–	–	μs	see Fig. 11

Note: stray capacitance between pins 13 and 14 < 3 pF.

TIMING DATA (continued)

V_{DD} = 2,5 to 6 V; V_{SS} = 0 V; f_{osc} = 3,579545 MHz

input levels of F01 and F02 (V_{SS} = LOW; V_{DD} = HIGH)		V_{F01}	LOW	HIGH	LOW	HIGH		conditions (note 4)
		V_{F02}	LOW	HIGH	HIGH	LOW		
		symbol				(test mode)		
Dialling pulse frequency	$1/T_{DP}$	f_{DP}	10,13	15,54	19,42	932,2	Hz	note 1
Dialling pulse period	$1/f_{DP}$	T_{DP}	98,7	64,4	51,5	1,073	ms	
Clock pulse frequency	$30 \times f_{DP}$	f_{CL}	303,9	466,1	582,6	27965	Hz	
Break time (note 2)	$3/5 \times T_{DP}$	t_b	59,2	38,6	30,9	0,644	ms	M/S = H; n.c.
Make time (note 2)	$2/5 \times T_{DP}$	t_m	39,5	25,8	20,6	0,429	ms	M/S = H; n.c.
Break time (note 3)	$2/3 \times T_{DP}$	t_b	65,8	42,9	34,6	0,715	ms	M/S = L
Make time (note 3)	$1/3 \times T_{DP}$	t_m	32,9	21,5	17,2	0,358	ms	M/S = L
Inter-digit pause	$8 \times T_{DP}$	t_{id}	790	515	412	8,58	ms	IDP = L; n.c.
	$9 \times T_{DP}$	t_{id}	888	579	463	9,65	ms	IDP = H
Reset delay time	$1,6 \times T_{DP}$	t_{rd}	158	103	82,4	1,72	ms	RDS = L; n.c.
	$3,2 \times T_{DP}$	t_{rd}	316	206	165	3,43	ms	RDS = H
Access pause time	$32 \times T_{DP}$	t_{ap}	3,16	2,06	1,65	0,034	s	APD = L; n.c.
	$64 \times T_{DP}$	t_{ap}	6,32	4,12	3,30	0,069	s	APD = H
Prepulse duration	$1/3 \times T_{DP}$	t_d	33	21,5	17,2	0,358	ms	
Debounce time								
min.	$4/30 \times T_{DP}$	$t_{e\,min}$	13,2	8,58	6,87	0,143	ms	
max.	$1/6 \times T_{DP}$	$t_{e\,max}$	16,5	10,7	8,58	0,179	ms	
Initial data entry time (typ.)	$t_{on} + t_e$	t_i	18	14	12	4	ms	

Notes

1. Exactly 10 Hz with 3,5328 MHz crystal.
2. Mark-to-space ratio: 3: 2.
3. Mark-to-space ratio: 2: 1.
4. In the n.c. (not connected) condition, the input is drawn to the appropriate state by the internal pull-up/pull-down current.

TYPICAL CURVES

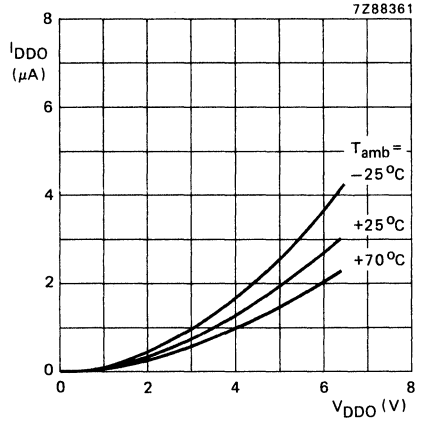


Fig. 14 Standby supply current as a function of standby supply voltage.

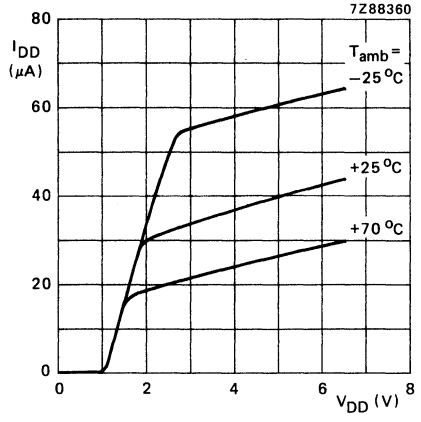


Fig. 15 Operating supply current as a function of operating supply voltage.

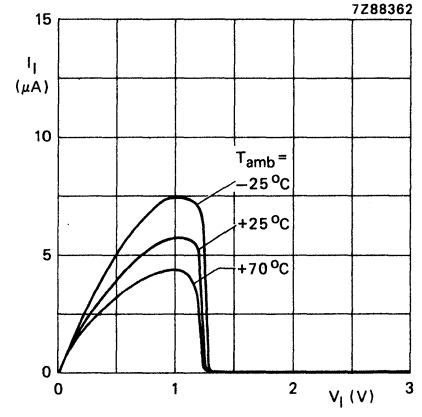


Fig. 16 Pull-down input current as a function of input voltage at V_{DD} = 3 V.

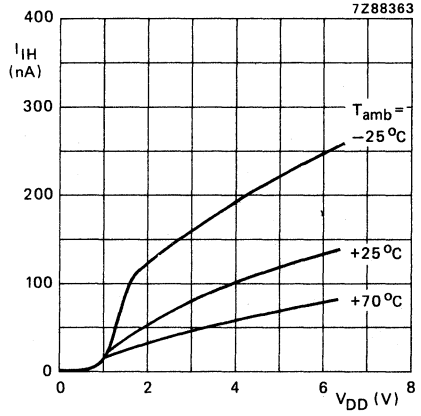


Fig. 17 Pull-down input current as a function of supply voltage at $V_I = V_{DD}$.

TYPICAL CURVES (continued)

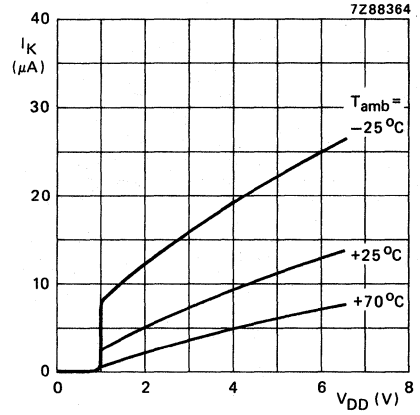


Fig. 18 Keyboard current as a function of supply voltage; X-pins connected to Y-pins.

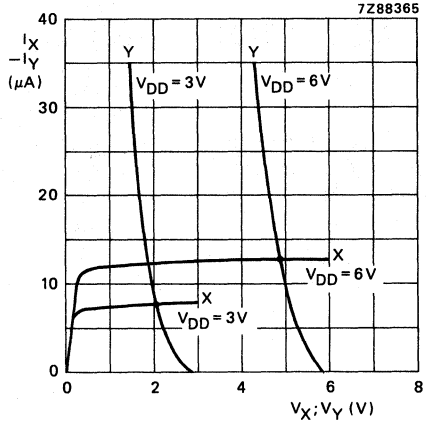


Fig. 19 Keyboard input characteristics at T_{amb} = 25 °C.

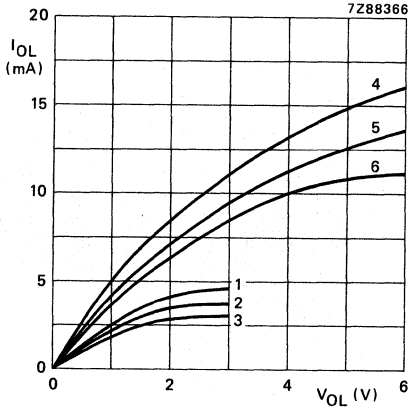


Fig. 20 Output (N-channel) sink characteristics for M1, $\overline{M1}$, M2, M3 and DP.

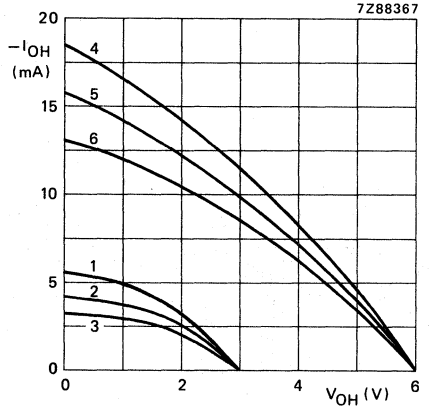


Fig. 21 Output (P-channel) source characteristics for M1, $\overline{M1}$, M2, M3 and DP.

Curves for Figs 20 and 21

T_{amb}	V_{DD} = 3 V	V_{DD} = 6 V
−25 °C	1	4
+25 °C	2	5
+70 °C	3	6

C-MOS INTERRUPTED CURRENT-LOOP DIALLING CIRCUIT

The PCD3324 is a single chip silicon-gate C-MOS integrated circuit. It is intended to convert pushbutton keyboard entries into streams of correctly-timed line current interruptions. The input data is derived from a telephone keyboard with a 3 x 4 pushbutton matrix. Numbers with up to 23 digits can be retained in a RAM for redial. A delayed reset is built-in for line power breaks.

The PCD3324 can regenerate access pauses during redial. During the original entry, only one access pause is stored automatically or several via the keyboard. A regenerated access pause can be terminated during redial in three ways: automatically after a built-in time, or via the keyboard, or with an external dial tone recogniser circuit. This makes the circuit very suitable for redial in PABX (Private Automatic Branch Exchange) systems. The PCD3324 is pin to pin compatible with the DF320 and the MT4320 (however, including additional functions).

The circuit has the following features:

- Operation from 2,5 V to 6 V supply.
- Static standby operation down to 1,8 V.
- Low current consumption; typ. 40 μA.
- Low static standby current; typ. 1 μA.
- On-chip oscillator for 3,58 MHz crystal.
- Fully decoded and debounced inputs for 3 x 4 matrix keyboard.
- 23-digit capacity, including access pauses, for redial operation.
- Memory overflow possibility (with internally disabled redial).
- Selectable dialling pulse frequency: 10 Hz, 16 Hz and 20 Hz.
- Test pulse frequency: 932 Hz.
- Selectable dialling pulse mark/space ratios; 2 : 1 or 3 : 2.
- Hold facility for lengthening the inter-digit period.
- Circuit reset for line power breaks; $>$ 160 ms (10 Hz dialling pulse frequency).
- Access pause generation automatically or via the keyboard.
- Access pause reset:
  automatically after 3 s (10 Hz dialling pulse frequency),
  via the keyboard,
  with external tone recogniser.
- All inputs with pull-up/pull-down (except CE).
- All inputs are internally protected against electrostatic charges.
- High input noise immunity.

PACKAGE OUTLINES

PCD3324P : 18-lead DIL; plastic (SOT-102GE).
PCD3324D: 18-lead DIL; ceramic (SOT-133B).

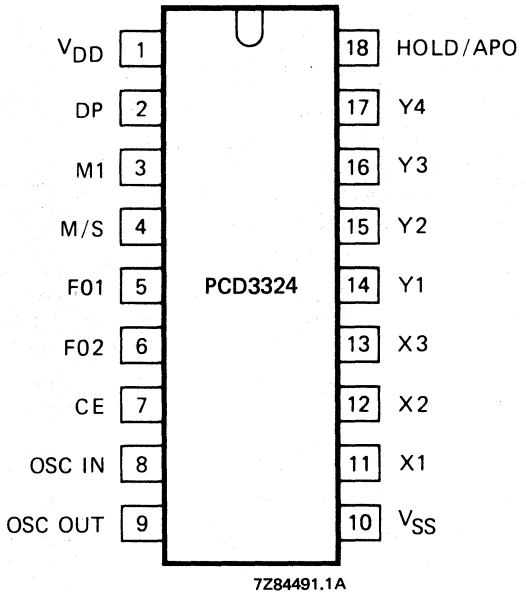


Fig. 1 Pinning diagram.

PINNING

1	V_{DD}	positive supply
10	V_{SS}	negative supply

Inputs

4	M/S	controls the mark-to-space ratio of the line pulses
5	F01	the dialling pulse frequency is defined by the logic state of these two inputs
6	F02	
7	CE	Chip Enable; used to initialize the system; to select between the operational mode and the static standby mode; to handle line power breaks
11	X1	column keyboard inputs with pull-down on chip
12	X2	
13	X3	
14	Y1	row keyboard inputs with pull-up on chip
15	Y2	
16	Y3	
17	Y4	

Outputs

2	DP	Dialling Pulse; drive of the external line switching transistor or relay
3	M1	Muting; normally used for muting during the dialling sequence

Input/output

18	HOLD/APO	This pin will go HIGH when an access pause code is read from the memory during pulsing and will interrupt dialling. It can also be externally controlled; it will interrupt dialling after completion of the current digit or immediately during an inter-digit pause (t_{id}); further keyboard data will be accepted.

Oscillator

8	OSC IN	input and output of the on-chip oscillator
9	OSC OUT	

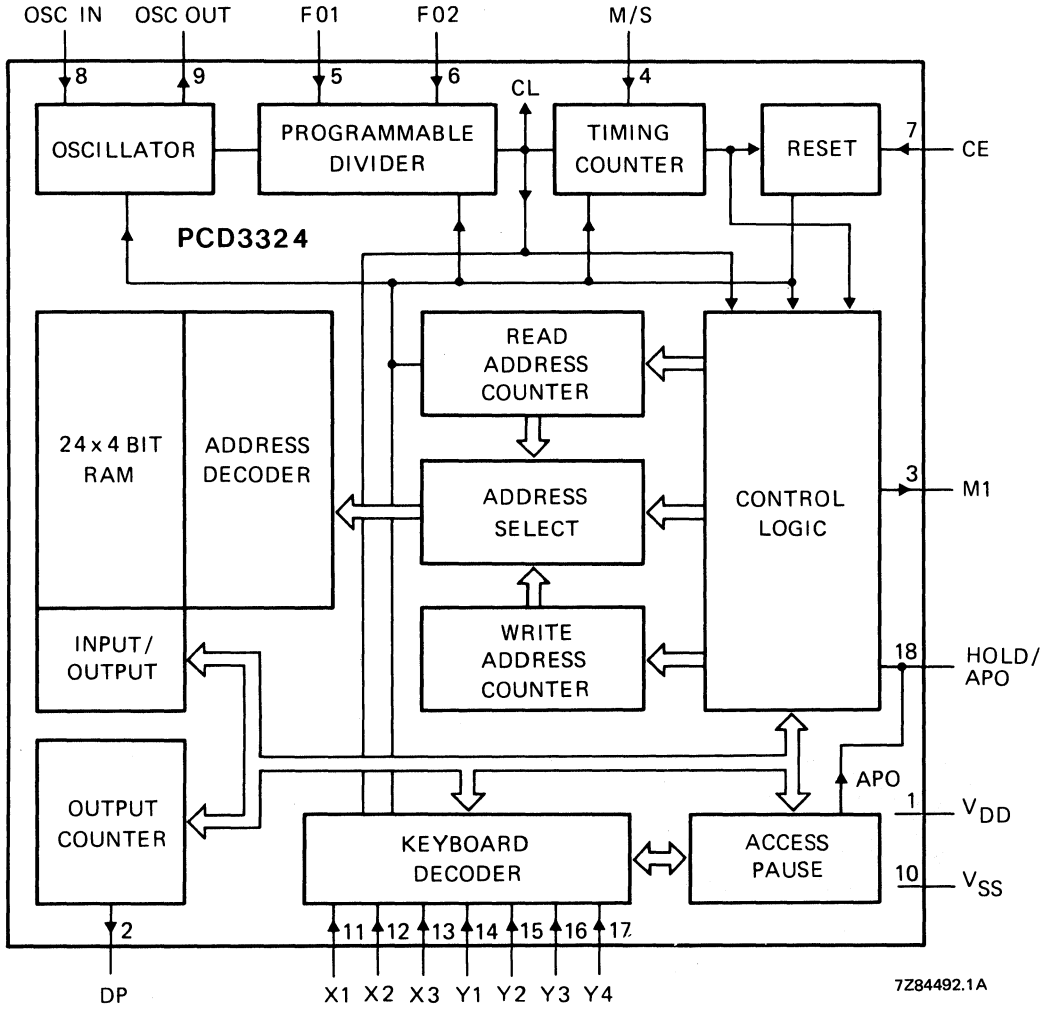


Fig. 2 Block diagram.

FUNCTIONAL DESCRIPTION (see also Fig. 2)

Clock oscillator (OSC IN, OSC OUT)

The time base for the **PCD3324** is a crystal controlled on-chip oscillator which is completed only by connecting a crystal between the OSC IN and OSC OUT pins. The oscillator is followed by a frequency divider of which the division ratio can be externally set (F01 and F02) to provide one of four chip system clocks; three 'normal' clock frequencies and one higher test frequency.

Alternatively, the OSC IN input may be driven from an external clock signal.

Chip Enable (CE)

The CE input is used to initialize the chip system.

CE = LOW provides the static standby condition. In this mode the clock oscillator is off and internal registers are clamped reset with the exception of the WRITE ADDRESS COUNTER (WAC). The keyboard input is inhibited, but data previously entered is saved in the RAM.

When CE = HIGH the clock oscillator is operating, the internal registers are enabled and data can be entered from the keyboard.

If the CE input is taken to a LOW level for more than the time t_{rd} (see Figs 5 and 6 and timing data) an internal reset pulse will be generated at the end of the t_{rd} period. The system is then in the static standby mode. Short CE pulses of $< t_{rd}$ will not affect the operation of the circuit. No reset pulses are then produced.

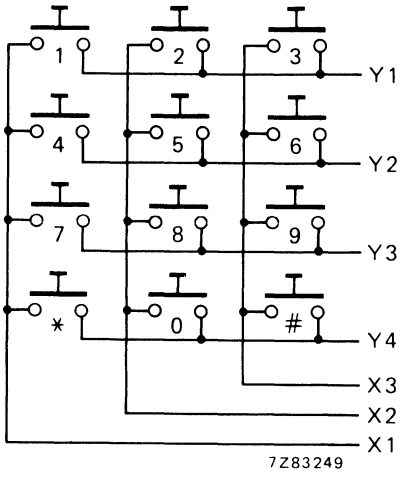
Debouncing keyboard entries

The column keyboard inputs to the integrated circuit (X_n) and the row keyboard inputs (Y_n) are for direct connection to a 3 x 4 single contact keyboard matrix (with or without common contact) as shown in Fig. 3, or to a double contact keyboard with a common left open (see Fig. 4). An entry is decoded into a 4-bit binary keycode by the keyboard decoder when one column input is connected to one row input or, when one column input is set HIGH and one row input is set LOW. Any other input combinations will be judged to be not valid and will not be accepted. Valid inputs are debounced on the leading and trailing edges as shown in Fig. 5. Keyboard entries are only decoded into 4-bit binary keycodes and written into the RAM if the keyboard contact remains closed for four or five clock pulse periods (entry period t_e). The next keyboard entry will not be accepted until the previously closed contact has been open for three or four clock pulse periods. The one clock pulse period of uncertainty in the debouncing process arises because keyboard entries are not detected until the trailing edge of the first clock pulse after the entry.

Data entry

After each keyboard entry has been debounced and decoded, the keycode is written into the RAM, and the WAC is incremented by one to select the next RAM location where the next keycode will be stored. As each keycode is recalled from the RAM for line pulsing, the READ ADDRESS COUNTER (RAC) is incremented by one to select the RAM location of the next keycode to be recalled. Consequently, the difference between the contents of the WAC and of the RAC represents the number of keycodes that have been written into the RAM but not yet converted into line pulses. If more than 23 keycodes are written into the RAM, memory overflow results and the excess keycode replace the data in the lower numbered RAM locations. In this event, since an erroneous number is stored, automatic redialling is inhibited until the WAC has been reset by the first digit entry of the next telephone call.

If the first pushbutton to be pressed is not redial (#), the WAC is reset during entry time t_e, the corresponding keycode is written into the first RAM location, and the WAC is then incremented by one. If the first pushbutton to be pressed is redial (#), the WAC is not reset and the keycodes stored in the RAM are sequentially recalled and converted into correctly timed dialling pulses at output DP. If the redial pushbutton (#) is operated again during the redialling sequence it will be decoded as an Access Pause Reset. This function will be described later during the description of the access pause system of the PCD3324. During redial no keyboard entry will be accepted and stored in the RAM. But, when all in the RAM stored numbers have been pulsed out, new keyboard entry will be accepted, stored at the RAM position after the last digit code of the original entry and converted into correctly timed dialling pulses.



★ Access pause set.

Redial or Access Pause Reset.

Fig. 3 Single contact keyboard.

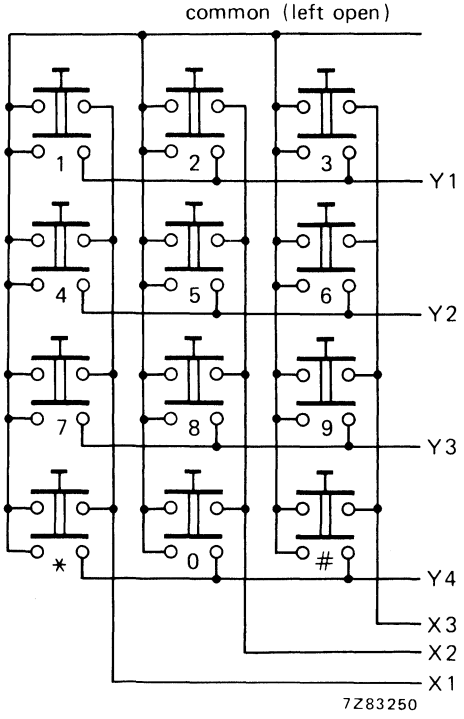


Fig. 4 Double contact keyboard.

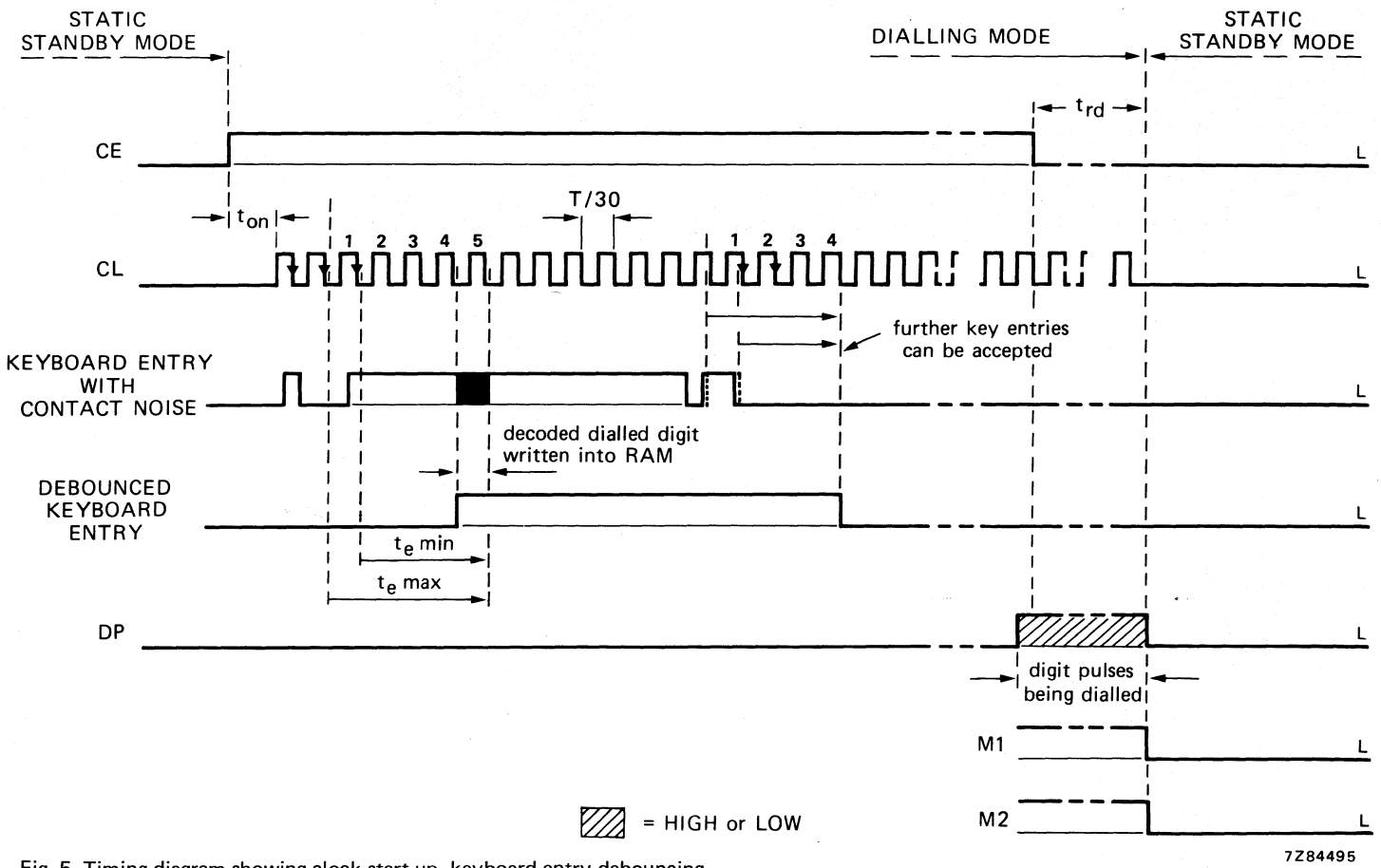


Fig. 5 Timing diagram showing clock start-up, keyboard entry debouncing and the effect of interrupting the supply to CE during the transmission of dialling pulses.

N.B.: CL and M2 are internal signals.

Dialling sequence

The dialling sequence can be initiated under either of the following two conditions:

- The supply to the integrated circuit is derived from the telephone lines via the cradle contacts (power supply before keyboard entry); see Fig. 6.

Then, approximately 4 ms (t_{on}) after CE goes HIGH, the clock pulse generator starts and, ten clock pulse periods (t_d) later, a prepulse with a duration of ten clock pulse periods (t_d) appears at output M1. This prepulse ensures that, if a polarized muting relay with two stable positions is used, it switches to the de-muted position so that the circuit is then in the conversation mode whilst the subscriber awaits the dialling tone. When the first digit of the required number is entered at the keyboard, data entry period t_e commences.

- The supply to the integrated circuit is derived from the telephone lines via the cradle contacts in series with a common keyboard contact (Fig. 7).

When the first digit of the required number is entered at the keyboard, the common keyboard contact connects the line voltage to V_{DD} and CE becomes HIGH. Approximately 4 ms (t_{on}) after CE goes HIGH, the clock pulse generator starts and data entry period t_e commences. After period t_e, M1 goes HIGH and the pushbutton can be released. The supply to V_{DD} and CE is then maintained via the muting circuit controlled by M1.

The further dialling sequence will be described with the aid of Fig. 6. When the keyboard entry has been decoded and written into the RAM, M1 goes HIGH to mute the telephone and an inter-digit pause (t_{id}) ensues. M2 then goes HIGH (M2 is an internally generated signal, used for explanation only), the RAC addresses the RAM and the first keycode is loaded into the register of the output counter which generates the appropriate number of correctly-timed dialling pulses at output DP. When the digit has been pulsed out, M2 goes LOW, the RAC is incremented by one and the procedure repeats until the WAC and RAC contents are equal (all digits pulsed out). Output M1 then goes LOW, the circuit assumes the conversation mode. The circuit reverts to the static standby mode if CE goes LOW for more than the reset delay time (t_{rd} = 1,6 dialling pulse periods) at any time during the conversation or dialling mode (e.g. because the handset is replaced). CE remains LOW although V_{DD} is maintained by a back-up supply (e.g. because an external diode isolates CE from the back-up supply connected to V_{DD}). The RAM retains its contents for subsequent automatic redialling as long as the back-up supply maintains V_{DD} above V_{DDO} = 1,8 V.

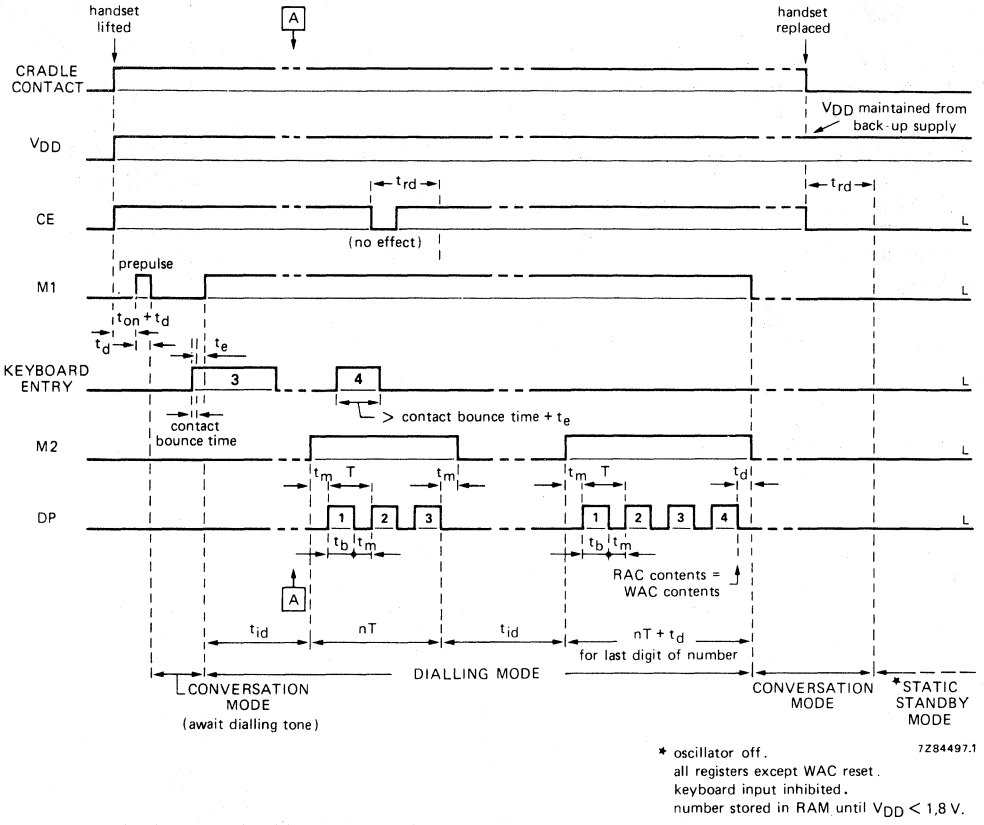


Fig. 6 Timing diagram of dialling sequence with V_{DD} and CE HIGH before keyboard entry (e.g. supply via the cradle contacts). M2 is an internal signal.

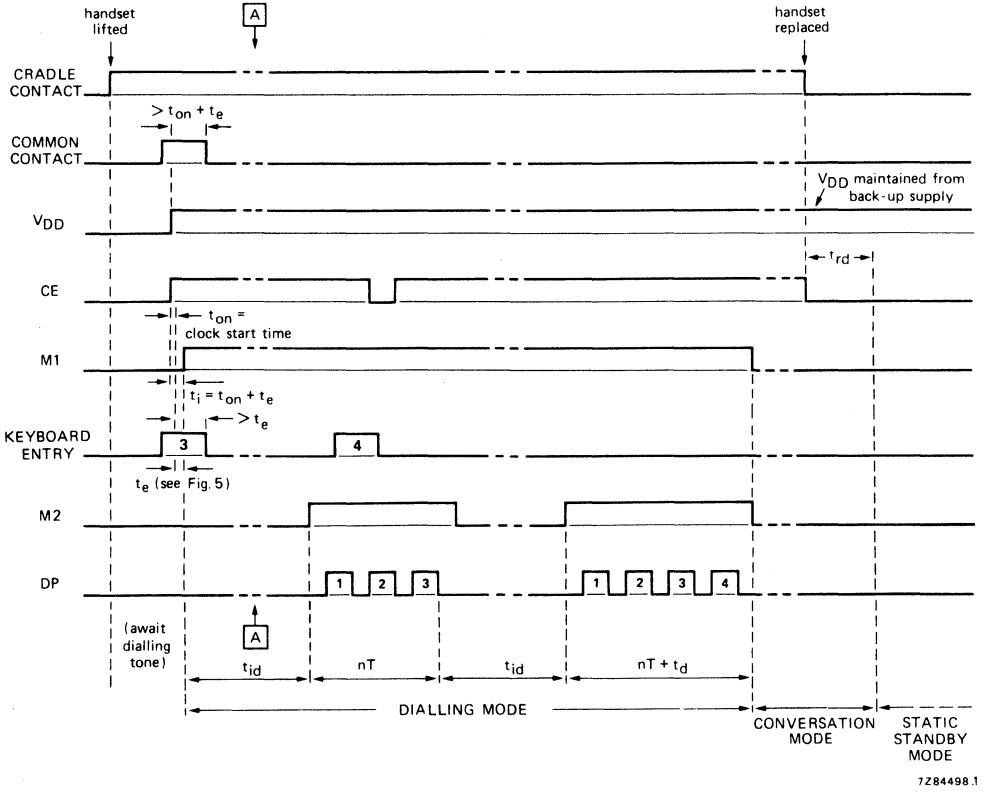


Fig. 7 Timing diagram for initiating the dialling mode with V_{DD} and CE initially supplied via the cradle contacts in series with a common contact on the keyboard. See Fig. 6 for pulse timings after point A. M2 is an internal signal.

Hold function

As shown in Fig. 8, the hold function allows the interval between consecutive pulsed digits to be prolonged under the control of external equipment. When the HOLD/APO is set HIGH, the dialling pulse-train is interrupted as soon as M2 goes LOW to signal that the current digit has been pulsed out. In the hold condition, further keyboard entries will be accepted, debounced, decoded and stored in that RAM. No further keycodes will be read from the RAM and converted into dialling pulses on DP until the HOLD/APO is set LOW again and an inter-digit pause has elapsed.

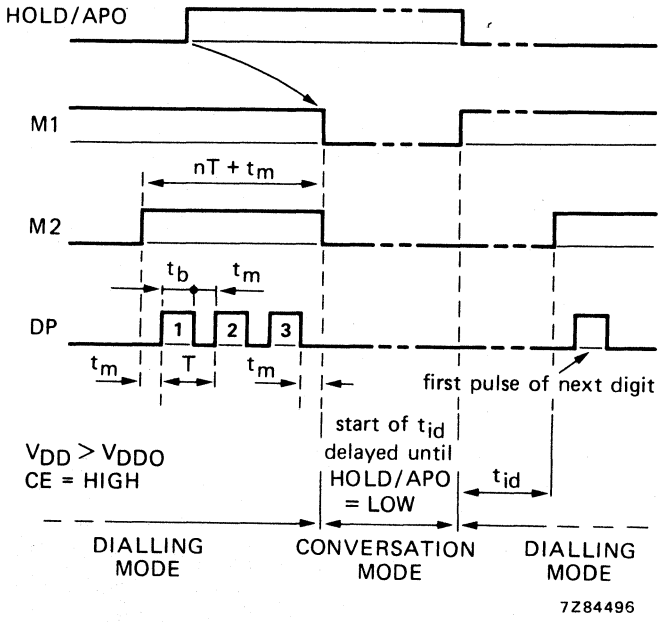


Fig. 8 Timing diagram showing the effect of activating the HOLD/APO during the transmission of dialling pulses. M2 is an internal signal.

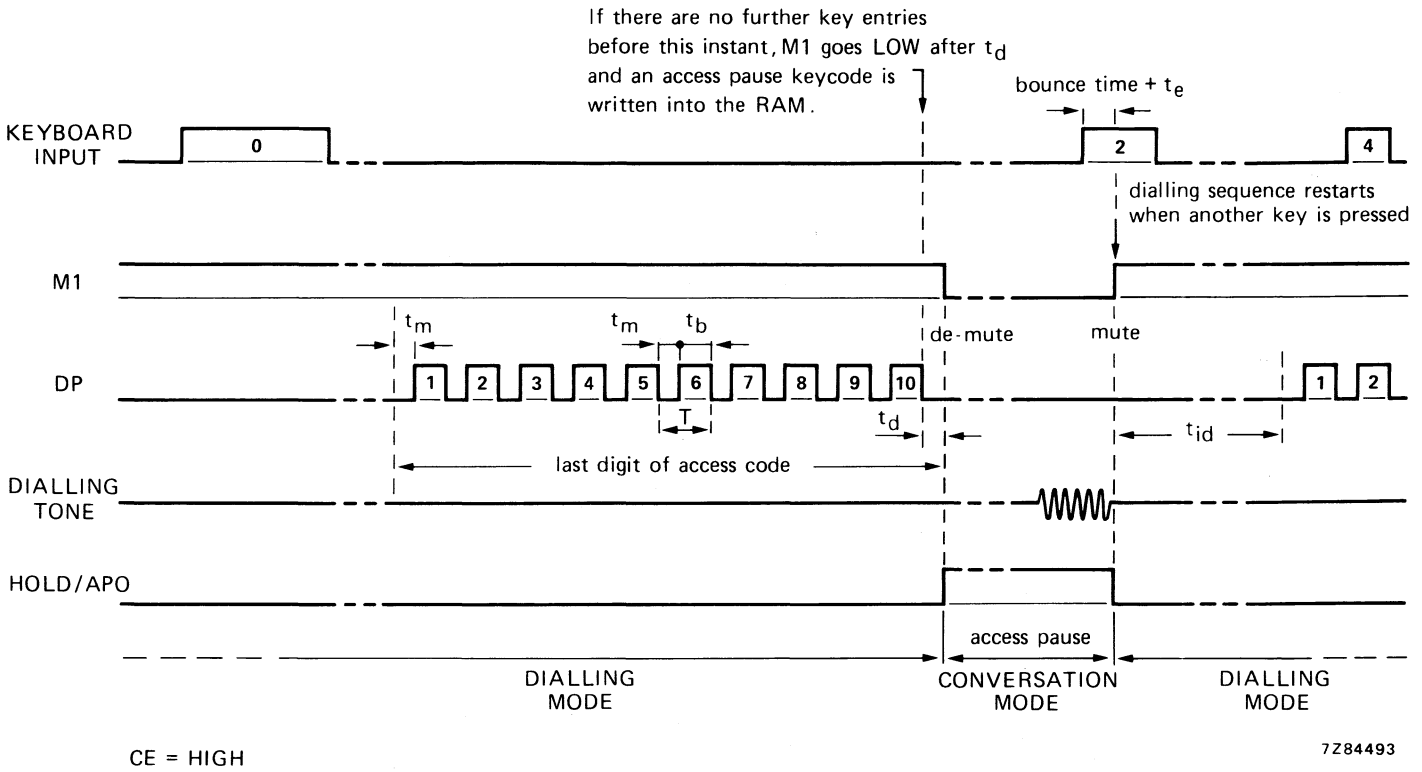
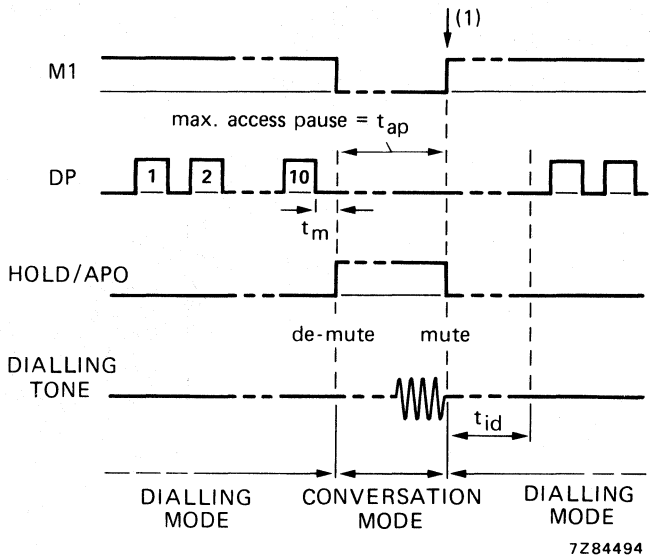


Fig. 9 Dialling sequence showing how an access pause code is automatically stored in the RAM for possible redialling if no further key entries are made until all of the previously entered digits have been transmitted. The dialling sequence continues when another key is pressed.

Access pause regeneration during redial

During original entry, access pause codes can be stored at the appropriate positions in the RAM. During redial the Access Pause Output (HOLD/APO)will go HIGH as soon as an access pause code is read from the RAM, thereby interrupting dialling until HOLD/APO is made LOW again as described above. In this way the normal inter-digit pause with a duration t_{id} can be replaced by a proper access pause. An access pause code is now automatically stored in the RAM during original entry, when M1 goes LOW, after all digits so far entered have been transmitted (see Fig. 6). This occurs between entering of the trunk exchange code and the subscriber code, whilst the access tone is available. Only one access pause can be entered into the RAM in this manner. Alternatively, the access pause key (★) can still be pressed to insert (more) access pauses manually (digits + access pauses ⩽ 23).
During redial, access pauses will be automatically regenerated.

Three methods of terminating an access pause:
1. Automatically, if the built-in time t_{ap} expires; HOLD/APO then goes LOW.
2. Manually, by pressing the redial key before t_{ap} expires.
3. With an external tone recogniser, by forcing HOLD/APO to LOW or HIGH respectively, for shortening or lengthening an access pause.



(1) a. Access pause (t_{ap}) expires or press redial before end of t_{ap}.

b. HOLD/APO controlled by tone recogniser:
HOLD/APO forced to LOW before t_{ap} expires; access pause $< t_{ap}$
HOLD/APO forced to HIGH after t_{ap} expires; access pause $> t_{ap}$.

Fig. 10 Timing diagram showing Access Pause Reset.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_{DD}	−0,3 to 8 V
Voltage on any pin	V_I	V_{SS} −0,3 to V_{DD} + 0,3 V
Operating ambient temperature range	T_{amb}	−25 to +70 °C
Storage temperature range	T_{stg}	−55 to +125 °C

CHARACTERISTICS

V_{DD} = 3 V; V_{SS} = 0 V; crystal parameters: f_{osc} = 3,58 MHz, R_{Smax} = 100 Ω (note 3); T_{amb} = 25 °C; unless otherwise specified.

	symbol	min.	typ.	max.		conditions
Operating supply voltage	V_{DD}	2,5	3	6	V	T_{amb} = −25 to +70 °C
Standby supply voltage (note 1)	V_{DDO}	1,8	–	6	V	T_{amb} = −25 to +70 °C
Operating supply current	I_{DD}	–	40	–	μA	CE = HIGH; notes 2, 3
	I_{DD}	–	50	100	μA	CE = HIGH; V_{DD} = 6 V; notes 2, 3
Standby supply current	I_{DDO}	–	1	2	μA	CE = LOW; note 2
	I_{DDO}	–	–	2	μA	V_{DD} = 1,8 V; T_{amb} = −25 to +70 °C
Input voltage LOW	V_{IL}	–	–	0,3 V_{DD}		1,8 V ⩽ V_{DD} ⩽ 6 V
Input voltage HIGH	V_{IH}	0,7 V_{DD}	–	–		1,8 V ⩽ V_{DD} ⩽ 6 V
Input leakage current; CE						
LOW	$-I_{IL}$	–	–	50	nA	CE = LOW
HIGH	I_{IH}	–	–	50	nA	CE = HIGH
Pull-up input current M/S	$-I_{IL}$	30	100	300	nA	V_I = V_{SS}
Pull-down input current F01, F02	I_{IH}	30	100	300	nA	V_I = V_{DD}
Matrix keyboard operation						
Keyboard current	I_K	–	10	–	μA	X connected to Y, CE = HIGH
Keyboard 'ON' resistance	R_{KON}	–	–	500	Ω	contact ON; note 4
Keyboard 'OFF' resistance	R_{KOFF}	1	–	–	MΩ	contact OFF; note 4
Other keyboard operation						
Input current for X_n 'ON'	I_{IH}	–	–	30	μA	V_I = 1,5 to 3 V
Input current for Y_n 'ON'	$-I_{IL}$	10	–	–	μA	V_I = 0 to 2,5 V
Input current Y_n	$-I_I$	–	–	0,7	mA	V_I = V_{SS}

Notes

1. V_{DDO} = 1,8 V only for redial.
2. All other inputs and outputs open.
3. Stray capacitance between pins 8 and 9 < 3 pF.
4. Guarantees correct keyboard operation.

CHARACTERISTICS (continued)

	symbol	min.	typ.	max.		conditions
Outputs M1, DP						
sink current	I_{OL}	0,7	1,5	3,2	mA	V_{OL} = 0,5 V
source current	$-I_{OH}$	0,65	1,3	2,7	mA	V_{OH} = 2,5 V
Latch output HOLD/APO						
sink current	I_{OL}	50	130	300	μA	V_{OL} = 0,5 V
source current	$-I_{OH}$	45	110	250	μA	V_{OH} = 2,5 V

TIMING DATA

V_{DD} = 2,5 to 6 V; V_{SS} = 0 V; f_{osc} = 3,579545 MHz

input levels of F01 and F02 (V_{SS} = LOW; V_{DD} = HIGH)		V_{F01}	LOW	HIGH	LOW	HIGH		
		V_{F02}	LOW	HIGH	HIGH	LOW		conditions (note 4)
		symbol				(test mode)		
Dialling pulse frequency	$1/T_{DP}$	f_{DP}	10,13	15,54	19,42	939,2	Hz	note 1
Dialling pulse period	$1/f_{DP}$	T_{DP}	98,7	64,4	51,5	1,073	ms	
Clock pulse frequency	$30 \times f_{DP}$	f_{CL}	303,9	466,1	582,6	27965	Hz	
Break time (note 2)	$3/5 \times T_{DP}$	t_b	59,2	38,6	30,9	0,644	ms	M/S = H; n.c.
Make time (note 2)	$2/5 \times T_{DP}$	t_m	39,5	25,8	20,6	0,429	ms	M/S = H; n.c.
Break time (note 3)	$2/3 \times T_{DP}$	t_b	65,8	42,9	34,6	0,715	ms	M/S = L
Make time (note 3)	$1/3 \times T_{DP}$	t_m	32,9	21,5	17,2	0,358	ms	M/S = L
Inter-digit pause	$8 \times T_{DP}$	t_{id}	790	515	412	8,58	ms	
Reset delay time	$1,6 \times T_{DP}$	t_{rd}	158	103	82,4	1,72	ms	
Access pause time	$32 \times T_{DP}$	t_{ap}	3,16	2,06	1,65	0,034	s	
Prepulse duration	$1/3 \times T_{DP}$	t_d	33	21,5	17,2	0,358	ms	
Debounce time								
min	$4/30 \times T_{DP}$	$t_{e\,min}$	13,2	8,58	6,87	0,143	ms	
max.	$1/6 \times T_{DP}$	$t_{e\,max}$	16,5	10,7	8,58	0,179	ms	
Clock start-up time		$t_{on\,typ}$	4	—	—	—	ms	CE: $V_{SS} \rightarrow V_{DD}$ (note 5)
Initial data entry time (typ.)	$t_{on} + t_e$	t_i	18	14	12	4	ms	

Notes

1. Exactly 10 Hz with 3,5328 MHz crystal.
2. Mark-to-space ratio: 3:2.
3. Mark-to-space ratio: 2:1.
4. In the n.c. (not connected) condition, the input is drawn to the appropriate state by the internal pull-up/pull-down current.
5. Stray capacitance between pins 8 and 9: < 3 pF.

TYPICAL CURVES

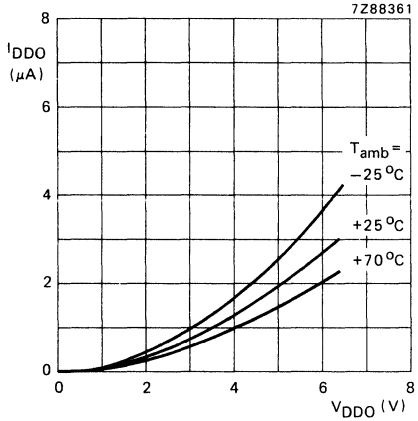


Fig. 11 Standby supply current as a function of standby supply voltage.

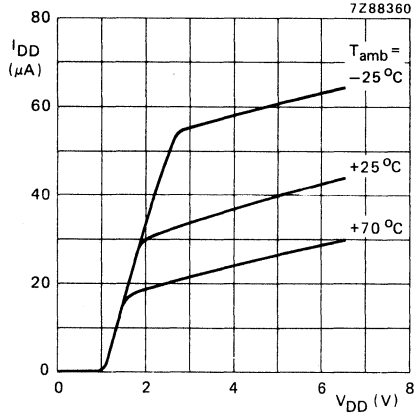


Fig. 12 Operating supply current as a function of operating supply voltage.

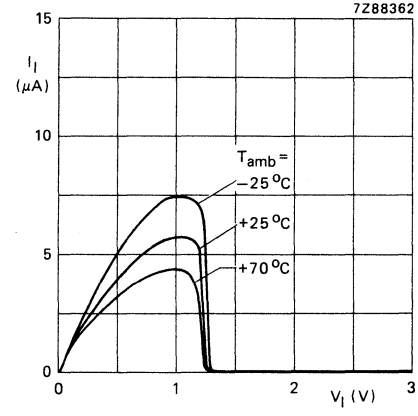


Fig. 13 Pull-down input current as a function of input voltage at V_{DD} = 3 V.

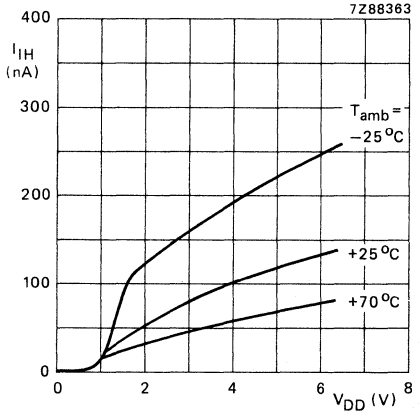


Fig. 14 Pull-down input current as a function of supply voltage at $V_I = V_{DD}$.

TYPICAL CURVES (continued)

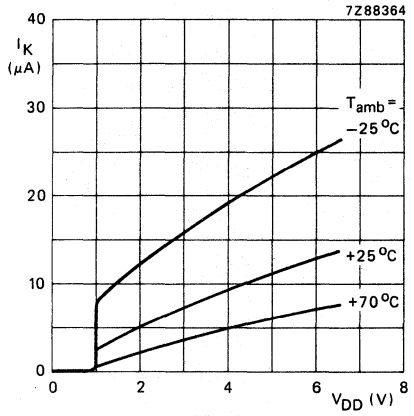


Fig. 15 Keyboard current as a function of supply voltage; X-pins connected to Y-pins.

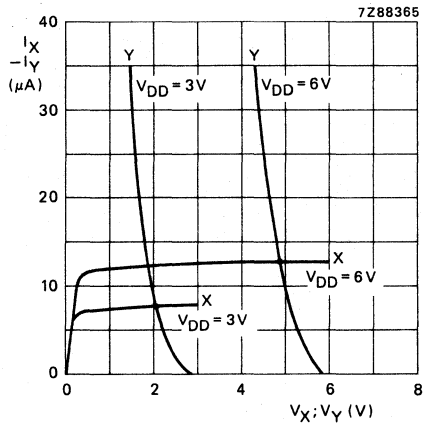


Fig. 16 Keyboard input characteristics at T_{amb} = 25 °C.

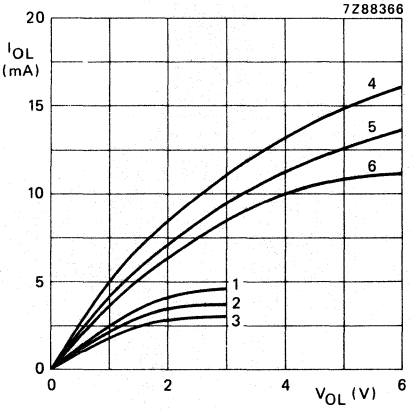


Fig. 17 Output (N-channel) sink characteristics for M1 and DP.

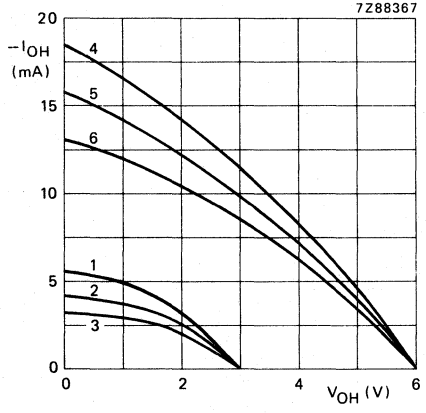


Fig. 18 Output (P-channel) source characteristics for M1 and DP.

Curves for Figs 17 and 18

T_{amb}	V_{DD} = 3 V	V_{DD} = 6 V
−25 °C	1	4
+25 °C	2	5
+70 °C	3	6

C-MOS INTERRUPTED CURRENT-LOOP DIALLING CIRCUIT

The PCD3325A is a single chip silicon-gate C-MOS integrated circuit. It converts pushbutton keyboard entries into streams of correctly-timed line current interruptions. The input data is derived from a telephone keyboard with a 3 x 4 pushbutton matrix. Numbers with up to 23 digits can be retained in a RAM for redial. A delayed reset is built-in for line power breaks.

The PCD3325A can regenerate access pauses during redial. During the original entry, access pauses are stored via the keyboard. A regenerated access pause can be terminated during redial in two ways: via the keyboard, or with an external dial tone recogniser circuit. This makes the circuit very suitable for redial in PABX (Private Automatic Branch Exchange) systems. The PCD3325A is pin to pin compatible with the DF320 and the MT4320 (however, including additional functions).

The circuit has the following features:

- Operation from 2,5 V to 6 V supply.
- Static standby operation down to 1,8 V.
- Low current consumption; typ. 40 μA.
- Low static standby current; typ. 1 μA.
- On-chip oscillator for 3,58 MHz crystal.
- Fully decoded and debounced inputs for 3 x 4 matrix keyboard.
- 23-digit capacity, including access pauses, for redial operation.
- Memory overflow possibility (with internally disabled redial).
- Selectable dialling pulse frequency: 10 Hz, 16 Hz and 20 Hz.
- Test pulse frequency: 932 Hz.
- Selectable dialling pulse mark/space ratios; 2 : 1 or 3 : 2.
- Hold facility for lengthening the inter-digit period.
- Circuit reset for line power breaks; $>$ 160 ms (10 Hz dialling pulse frequency).
- Access pause generation via the keyboard.
- Access pause reset:
  via the keyboard,
  with external tone recogniser.
- All inputs with pull-up/pull-down (except CE).
- All inputs are internally protected against electrostatic charges.
- High input noise immunity.

PACKAGE OUTLINE

18-lead DIL; plastic (SOT-102GE).

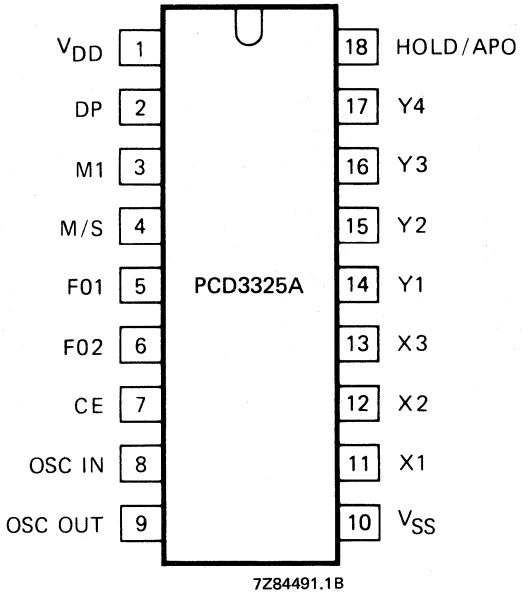


Fig. 1 Pinning diagram.

PINNING

1	V_{DD}	positive supply
10	V_{SS}	negative supply

Inputs

4	M/S	controls the mark-to-space ratio of the line pulses
5	F01	the dialling pulse frequency is defined by the logic state of these two inputs
6	F02	
7	CE	Chip Enable; used to initialize the system; to select between the operational mode and the static standby mode; to handle line power breaks
11	X1	column keyboard inputs with pull-down on chip
12	X2	
13	X3	
14	Y1	row keyboard inputs with pull-up on chip
15	Y2	
16	Y3	
17	Y4	

Outputs

2	DP	Dialling Pulse; drive of the external line switching transistor or relay
3	M1	Muting; normally used for muting during the dialling sequence

Input/output

18	HOLD/APO	This pin will go HIGH when an access pause code is read from the memory during pulsing and will interrupt dialling. It can also be externally controlled; it will interrupt dialling after completion of the current digit or immediately during an inter-digit pause (t_{id}); further keyboard data will be accepted.

Oscillator

8	OSC IN	input and output of the on-chip oscillator
9	OSC OUT	

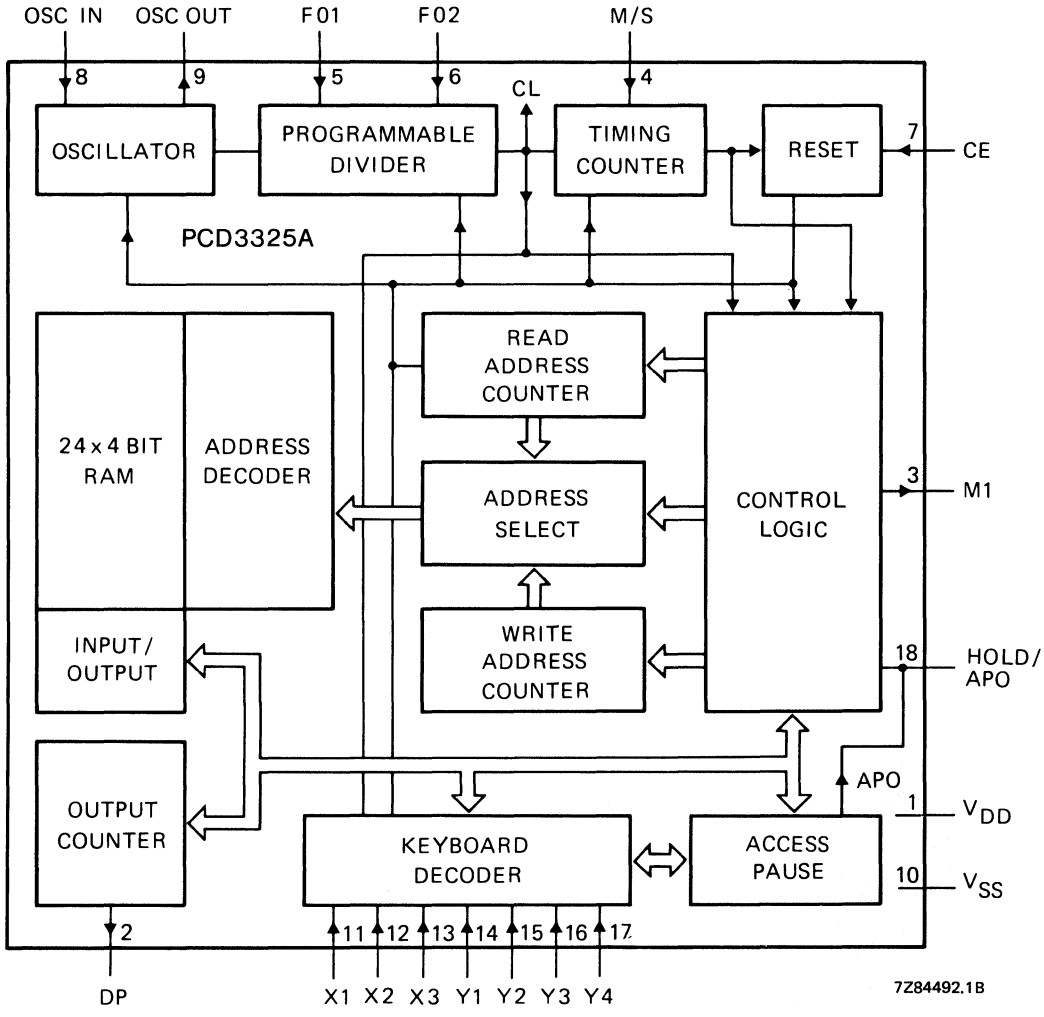


Fig. 2 Block diagram.

DEVELOPMENT DATA

FUNCTIONAL DESCRIPTION (see also Fig. 2)

Clock oscillator (OSC IN, OSC OUT)

The time base for the PCD3325A is a crystal controlled on-chip oscillator which is completed only by connecting a crystal between the OSC IN and OSC OUT pins. The oscillator is followed by a frequency divider of which the division ratio can be externally set (F01 and F02) to provide one of four chip system clocks; three 'normal' clock frequencies and one higher test frequency.

Alternatively, the OSC IN input may be driven from an external clock signal.

Chip Enable (CE)

The CE input is used to initialize the chip system.

CE = LOW provides the static standby condition. In this mode the clock oscillator is off and internal registers are clamped reset with the exception of the WRITE ADDRESS COUNTER (WAC). The keyboard input is inhibited, but data previously entered is saved in the RAM.

When CE = HIGH the clock oscillator is operating, the internal registers are enabled and data can be entered from the keyboard.

If the CE input is taken to a LOW level for more than the time t_{rd} (see Figs 5 and 6 and timing data) an internal reset pulse will be generated at the end of the t_{rd} period. The system is then in the static standby mode. Short CE pulses of $< t_{rd}$ will not affect the operation of the circuit. No reset pulses are then produced.

Debouncing keyboard entries

The column keyboard inputs to the integrated circuit (X_n) and the row keyboard inputs (Y_n) are for direct connection to a 3 x 4 single contact keyboard matrix (with or without common contact) as shown in Fig. 3, or to a double contact keyboard with a common left open (see Fig. 4). An entry is decoded into a 4-bit binary keycode by the keyboard decoder when one column input is connected to one row input or, when one column input is set HIGH and one row input is set LOW. Any other input combinations will be judged to be not valid and will not be accepted. Valid inputs are debounced on the leading and trailing edges as shown in Fig. 5. Keyboard entries are only decoded into 4-bit binary keycodes and written into the RAM if the keyboard contact remains closed for four or five clock pulse periods (entry period t_e). The next keyboard entry will not be accepted until the previously closed contact has been open for three or four clock pulse periods. The one clock pulse period of uncertainty in the debouncing process arises because keyboard entries are not detected until the trailing edge of the first clock pulse after the entry.

Data entry

After each keyboard entry has been debounced and decoded, the keycode is written into the RAM, and the WAC is incremented by one to select the next RAM location where the next keycode will be stored. As each keycode is recalled from the RAM for line pulsing, the READ ADDRESS COUNTER (RAC) is incremented by one to select the RAM location of the next keycode to be recalled. Consequently, the difference between the contents of the WAC and of the RAC represents the number of keycodes that have been written into the RAM but not yet converted into line pulses. If more than 23 keycodes are written into the RAM, memory overflow results and the excess keycodes replace the data in the lower numbered RAM locations. In this event, since an erroneous number is stored, automatic redialling is inhibited until the WAC has been reset by the first digit entry of the next telephone call.

If the first pushbutton to be pressed is not redial (#), the WAC is reset during entry time t_e, the corresponding keycode is written into the first RAM location, and the WAC is then incremented by one. If the first pushbutton to be pressed is redial (#), the WAC is not reset and the keycodes stored in the RAM are sequentially recalled and converted into correctly timed dialling pulses at output DP. If the redial pushbutton (#) is operated again during the redialling sequence it will be decoded as an Access Pause Reset. This function will be described later during the description of the access pause system of the PCD3325A. During redial no keyboard entry will be accepted and stored in the RAM. But, when all in the RAM stored numbers have been pulsed out, new keyboard entry will be accepted, stored at the RAM position after the last digit code of the original entry and converted into correctly timed dialling pulses.

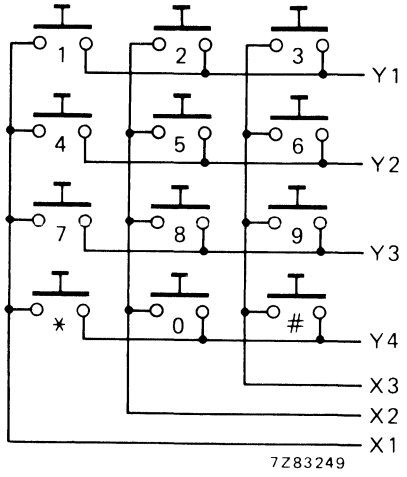


Fig. 3 Single contact keyboard.

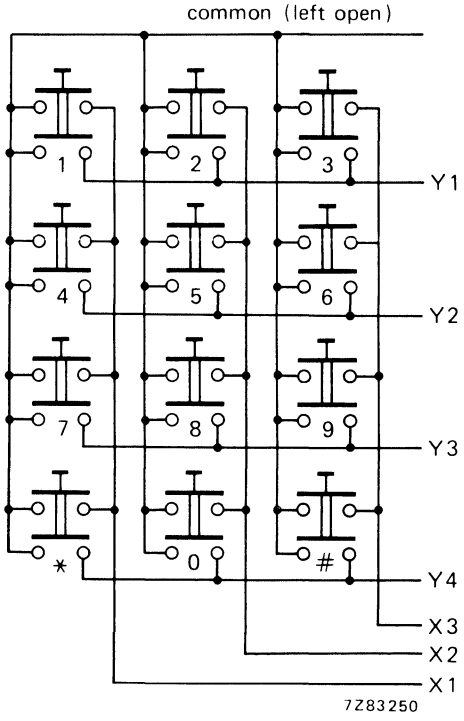


Fig. 4 Double contact keyboard.

DEVELOPMENT DATA

* Access pause set.

Redial or Access Pause Reset.

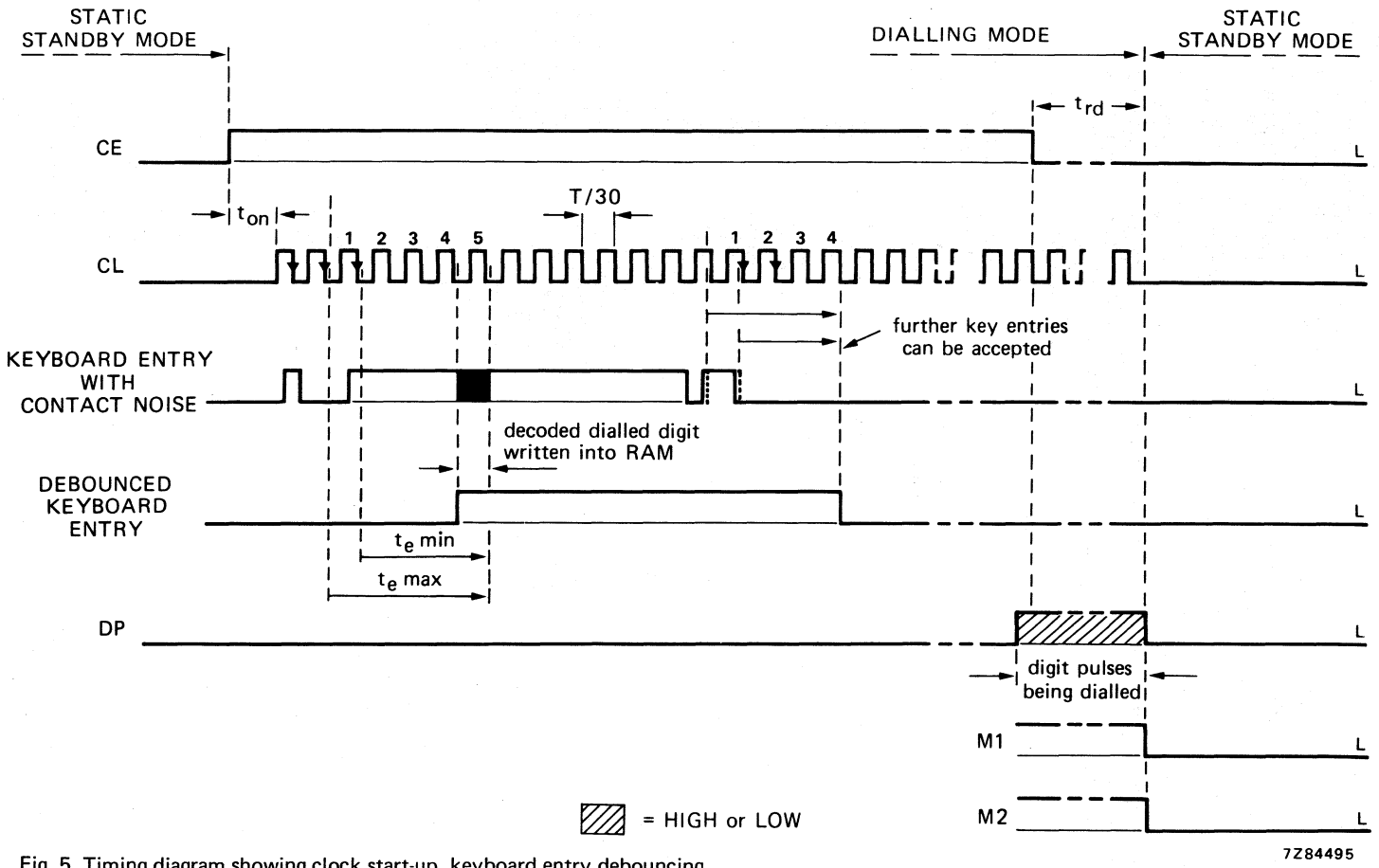


Fig. 5 Timing diagram showing clock start-up, keyboard entry debouncing and the effect of interrupting the supply to CE during the transmission of dialling pulses.

N.B.: CL and M2 are internal signals.

Dialling sequence

The dialling sequence can be initiated under either of the following two conditions:

- The supply to the integrated circuit is derived from the telephone lines via the cradle contacts (power supply before keyboard entry); see Fig. 6.

Then, approximately 4 ms (t_{on}) after CE goes HIGH, the clock pulse generator starts and, ten clock pulse periods (t_d) later, a prepulse with a duration of ten clock pulse periods (t_d) appears at output M1. This prepulse ensures that, if a polarized muting relay with two stable positions is used, it switches to the de-muted position so that the circuit is then in the conversation mode whilst the subscriber awaits the dialling tone. When the first digit of the required number is entered at the keyboard, data entry period t_e commences.

- The supply to the integrated circuit is derived from the telephone lines via the cradle contacts in series with a common keyboard contact (Fig. 7).

When the first digit of the required number is entered at the keyboard, the common keyboard contact connects the line voltage to V_{DD} and CE becomes HIGH. Approximately 4 ms (t_{on}) after CE goes HIGH, the clock pulse generator starts and data entry period t_e commences. After period t_e, M1 goes HIGH and the pushbutton can be released. The supply to V_{DD} and CE is then maintained via the muting circuit controlled by M1.

The further dialling sequence will be described with the aid of Fig. 6. When the keyboard entry has been decoded and written into the RAM, M1 goes HIGH to mute the telephone and an inter-digit pause (t_{id}) ensues. M2 then goes HIGH (M2 is an internally generated signal, used for explanation only), the RAC addresses the RAM and the first keycode is loaded into the register of the output counter which generates the appropriate number of correctly-timed dialling pulses at output DP. When the digit has been pulsed out, M2 goes LOW, the RAC is incremented by one and the procedure repeats until the WAC and RAC contents are equal (all digits pulsed out). Output M1 then goes LOW, the circuit assumes the conversation mode. The circuit reverts to the static standby mode if CE goes LOW for more than the reset delay time (t_{rd} = 1,6 dialling pulse periods) at any time during the conversation or dialling mode (e.g. because the handset is replaced). CE remains LOW although V_{DD} is maintained by a back-up supply (e.g. because an external diode isolates CE from the back-up supply connected to V_{DD}). The RAM retains its contents for subsequent automatic redialling as long as the back-up supply maintains V_{DD} above V_{DDO} = 1,8 V.

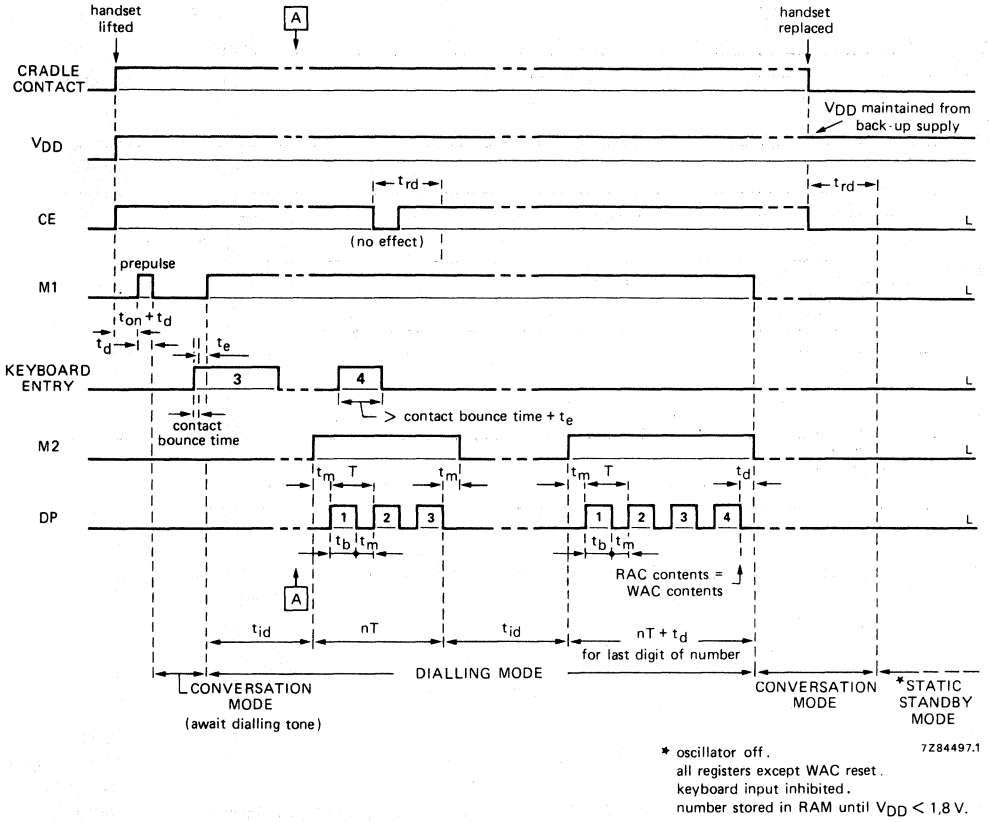


Fig. 6 Timing diagram of dialling sequence with V_{DD} and CE HIGH before keyboard entry (e.g. supply via the cradle contacts). M2 is an internal signal.

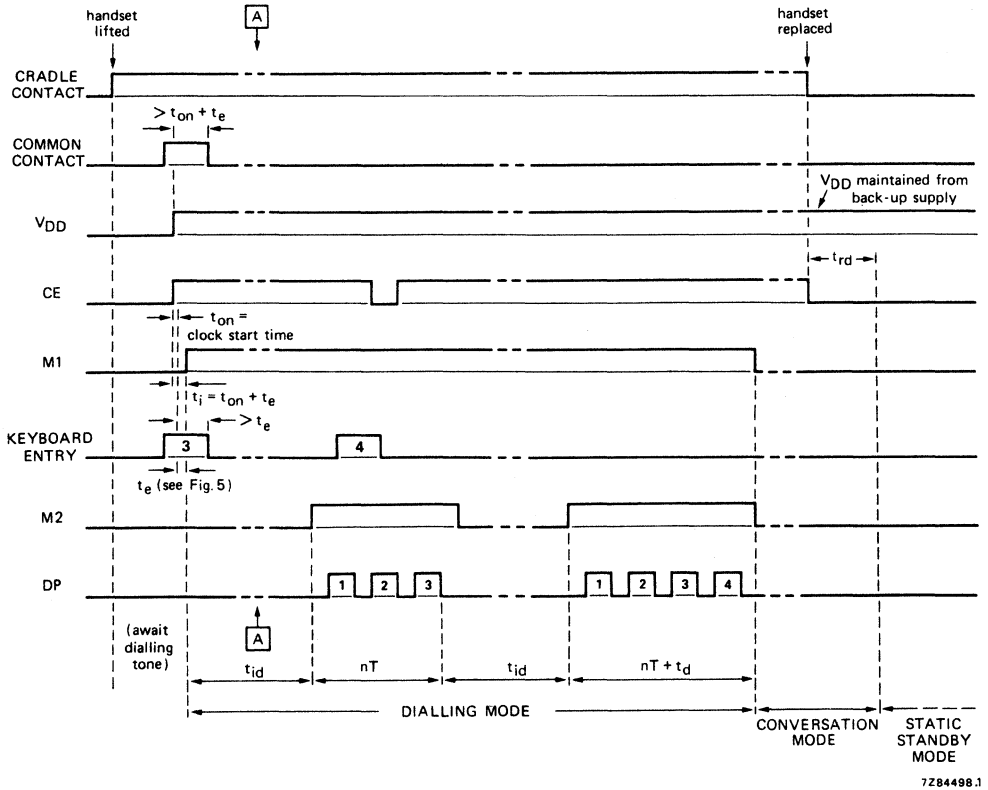


Fig. 7 Timing diagram for initiating the dialling mode with V_{DD} and CE initially supplied via the cradle contacts in series with a common contact on the keyboard. See Fig. 6 for pulse timings after point A. M2 is an internal signal.

Hold function

As shown in Fig. 8, the hold function allows the interval between consecutive pulsed digits to be prolonged under the control of external equipment. When the HOLD/APO is set HIGH, the dialling pulse-train is interrupted as soon as M2 goes LOW to signal that the current digit has been pulsed out. In the hold condition, further keyboard entries will be accepted, debounced, decoded and stored in that RAM. No further keycodes will be read from the RAM and converted into dialling pulses on DP until the HOLD/APO is set LOW again and an inter-digit pause has elapsed.

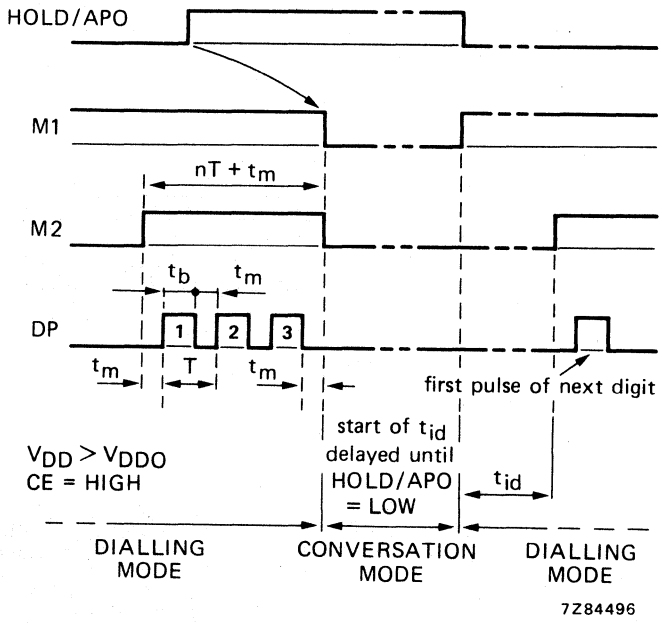


Fig. 8 Timing diagram showing the effect of activating the HOLD/APO during the transmission of dialling pulses. M2 is an internal signal.

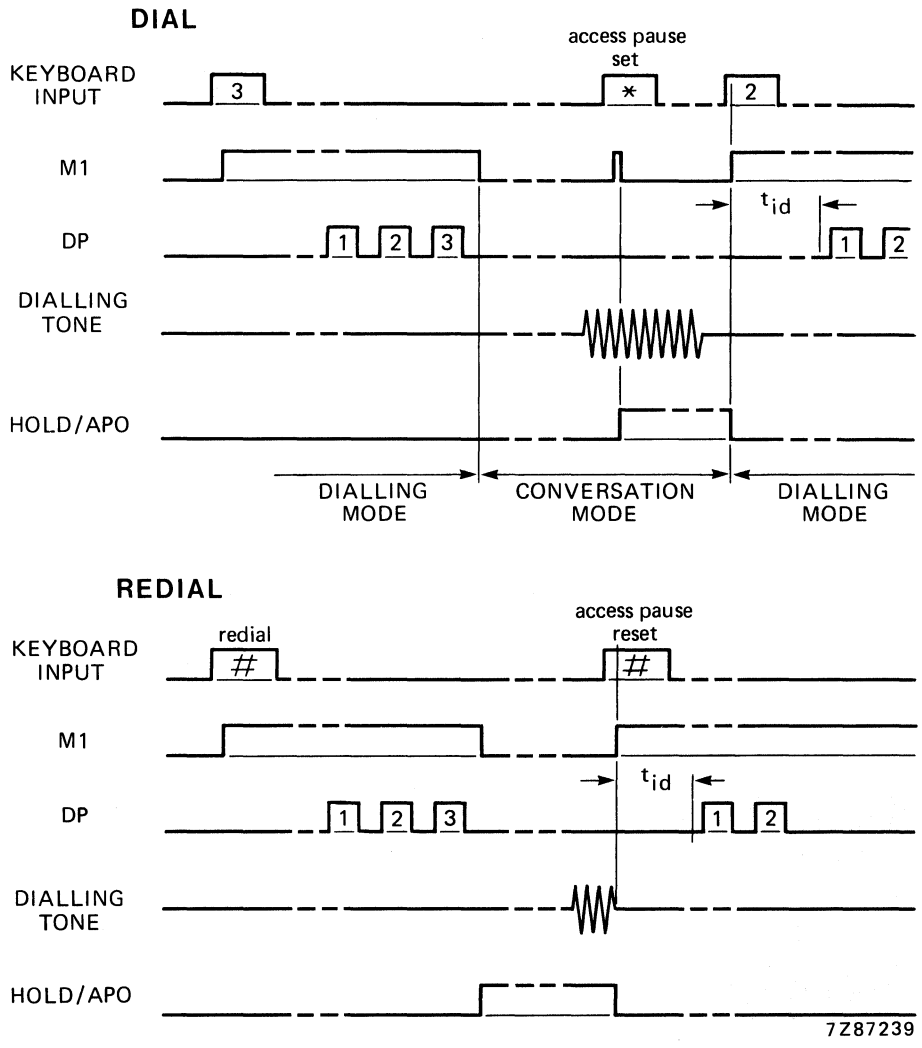


Fig. 9 Dialling sequence showing how an access pause code is stored in the RAM (DIAL) and how the access pause code is reset during the REDIAL.

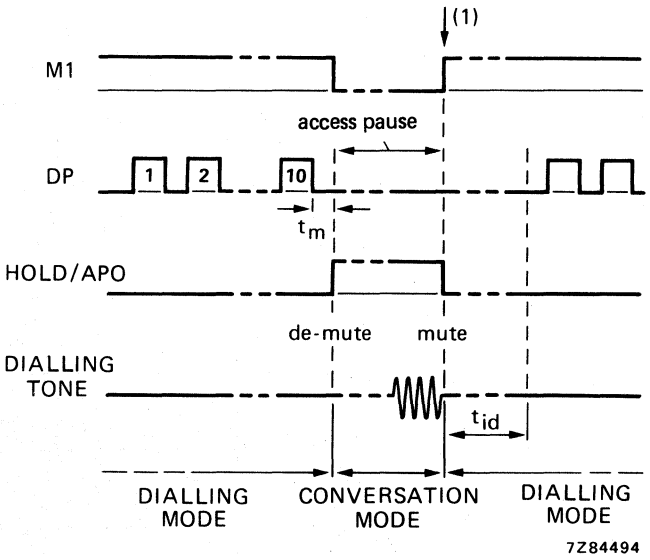
Note: access pause can be reset by pressing any key.

Access pause regeneration during redial

During original entry, access pause codes can be stored at the appropriate positions in the RAM. During redial the Access Pause Output (HOLD/APO) will go HIGH as soon as an access pause code is read from the RAM, thereby interrupting dialling until HOLD/APO is made LOW again as described above. In this way the normal inter-digit pause with a duration t_{id} can be replaced by a proper access pause. An access pause code is stored in the RAM during original entry by pressing the access pause key (*) between entering the trunk exchange code and the subscriber code, or at any other moment an access pause is required. The number of access pauses that can be inserted in this manner is only limited by the capacity of the RAM (digits + access pauses $\leqslant$ 23).

During redial, access pauses will be automatically regenerated.
Two methods of terminating an access pause:

1. Manually, by pressing the redial key (#)
2. With an external tone recogniser, by forcing HOLD/APO to LOW.



(1) a. Access pause reset by pressing redial key (#).
b. HOLD/APO controlled by tone recogniser:
HOLD/APO forced to LOW.

Fig. 10 Timing diagram showing Access Pause Reset, during redial.

Note: access pause can be reset by pressing any key.

DEVELOPMENT DATA

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_{DD}	−0,3 to 8 V
Voltage on any pin	V_I	V_{SS} −0,3 to V_{DD} + 0,3 V
Operating ambient temperature range	T_{amb}	−25 to +70 °C
Storage temperature range	T_{stg}	−55 to +125 °C

CHARACTERISTICS

V_{DD} = 3 V; V_{SS} = 0 V; crystal parameters: f_{osc} = 3,58 MHz, R_{Smax} = 100 Ω (note 3); T_{amb} = 25 °C; unless otherwise specified.

	symbol	min.	typ.	max.		conditions
Operating supply voltage	V_{DD}	2,5	3	6	V	T_{amb} = −25 to +70 °C
Standby supply voltage (note 1)	V_{DDO}	1,8	–	6	V	T_{amb} = −25 to +70 °C
Operating supply current	I_{DD}	–	40	–	μA	CE = V_{DD}; notes 2, 3
	I_{DD}	–	50	100	μA	CE = V_{DD}; V_{DD} = 6 V; notes 2, 3
Standby supply current	I_{DDO}	–	1	5	μA	CE = V_{SS} ; note 2
	I_{DDO}	–	–	2	μA	V_{DD} = 1,8 V T_{amb} = −25 to +70 °C
Input voltage LOW	V_{IL}	–	–	0,3 V_{DD}		1,8 V ⩽ V_{DD} ⩽ 6 V
Input voltage HIGH	V_{IH}	0,7 V_{DD}	–	–		1,8 V ⩽ V_{DD} ⩽ 6 V
Input leakage current; CE						
LOW	$-I_{IL}$	–	–	50	nA	CE = V_{SS}
HIGH	I_{IH}	–	–	50	nA	CE = V_{DD}
Pull-up input current M/S	$-I_{IL}$	30	100	300	nA	V_I = V_{SS}
Pull-down input current F01, F02	I_{IH}	30	100	300	nA	V_I = V_{DD}
Matrix keyboard operation						
Keyboard current	I_K	–	10	–	μA	X connected to Y, CE = HIGH
Keyboard 'ON' resistance	R_{KON}	–	–	500	Ω	contact ON; note 4
Keyboard 'OFF' resistance	R_{KOFF}	1	–	–	MΩ	contact OFF; note 4
Other keyboard operation						
Input current for X_n 'ON'	I_{IH}	–	–	30	μA	V_I = 1,5 to 3 V
Input current for Y_n 'ON'	$-I_{IL}$	10	–	–	μA	V_I = 0 to 2,5 V
Input current Y_n	$-I_I$	–	–	0,7	mA	V_I = V_{SS}

Notes

1. V_{DDO} = 1,8 V only for redial.
2. All other inputs and outputs open.
3. Stray capacitance between pins 8 and 9 < 3 pF.
4. Guarantees correct keyboard operation.

CHARACTERISTICS (continued)

	symbol	min.	typ.	max.		conditions
Outputs M1, DP						
sink current	I_{OL}	0,7	1,5	3,2	mA	V_{OL} = 0,5 V
source current	$-I_{OH}$	0,65	1,3	2,7	mA	V_{OH} = 2,5 V
Latch output HOLD/APO						
sink current	I_{OL}	50	130	300	μA	V_{OL} = 0,5 V
source current	$-I_{OH}$	45	110	250	μA	V_{OH} = 2,5 V

TIMING DATA

V_{DD} = 2,5 to 6 V; V_{SS} = 0 V; f_{osc} = 3,579545 MHz

input levels of F01 and F02 (V_{SS} = LOW; V_{DD} = HIGH)		V_{F01}	LOW	HIGH	LOW	HIGH		
		V_{F02}	LOW	HIGH	HIGH	LOW		conditions (note 4)
		symbol				(test mode)		
Dialling pulse frequency	$1/T_{DP}$	f_{DP}	10,13	15,54	19,42	939,2	Hz	note 1
Dialling pulse period	$1/f_{DP}$	T_{DP}	98,7	64,4	51,5	1,073	ms	
Clock pulse frequency	$30 \times f_{DP}$	f_{CL}	303,9	466,1	582,6	27965	Hz	
Break time (note 2)	$3/5 \times T_{DP}$	t_b	59,2	38,6	30,9	0,644	ms	M/S = H; n.c.
Make time (note 2)	$2/5 \times T_{DP}$	t_m	39,5	25,8	20,6	0,429	ms	M/S = H; n.c.
Break time (note 3)	$2/3 \times T_{DP}$	t_b	65,8	42,9	34,6	0,715	ms	M/S = L
Make time (note 3)	$1/3 \times T_{DP}$	t_m	32,9	21,5	17,2	0,358	ms	M/S = L
Inter-digit pause	$8 \times T_{DP}$	t_{id}	790	515	412	8,58	ms	
Reset delay time	$1,6 \times T_{DP}$	t_{rd}	158	103	82,4	1,72	ms	
Prepulse duration	$1/3 \times T_{DP}$	t_d	33	21,5	17,2	0,358	ms	
Debounce time								
min	$4/30 \times T_{DP}$	$t_{e\,min}$	13,2	8,58	6,87	0,143	ms	
max.	$1/6 \times T_{DP}$	$t_{e\,max}$	16,5	10,7	8,58	0,179	ms	
Clock start-up time		$t_{on\,typ}$	4	—	—	—	ms	CE: $V_{SS} \rightarrow V_{DD}$ (note 5)
Initial data entry time (typ.)	$t_{on} + t_e$	t_i	18	14	12	4	ms	

Notes

1. Exactly 10 Hz with 3,5328 MHz crystal.
2. Mark-to-space ratio: 3:2.
3. Mark-to-space ratio: 2:1.
4. In the n.c. (not connected) condition, the input is drawn to the appropriate state by the internal pull-up/pull-down current.
5. Stray capacitance between pins 8 and 9: < 3 pF.

DEVELOPMENT DATA

TYPICAL CURVES

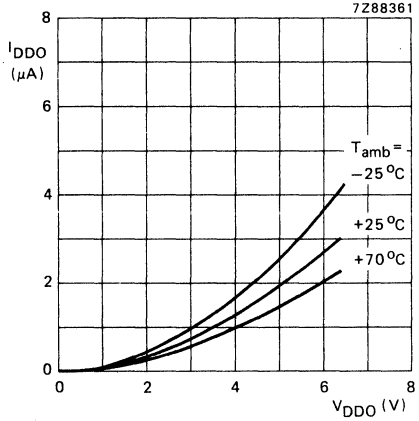


Fig. 11 Standby supply current as a function of standby supply voltage.

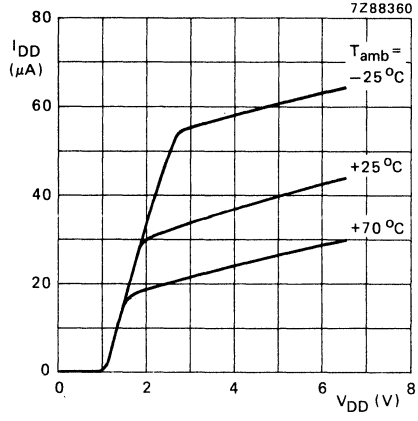


Fig. 12 Operating supply current as a function of operating supply voltage.

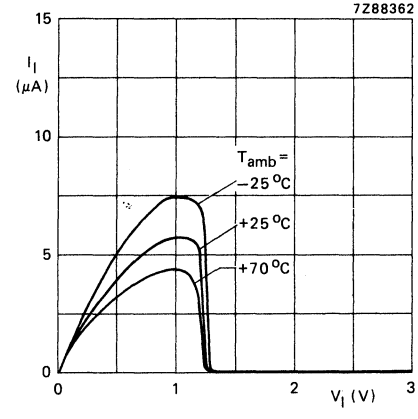


Fig. 13 Pull-down input current as a function of input voltage at V_{DD} = 3 V.

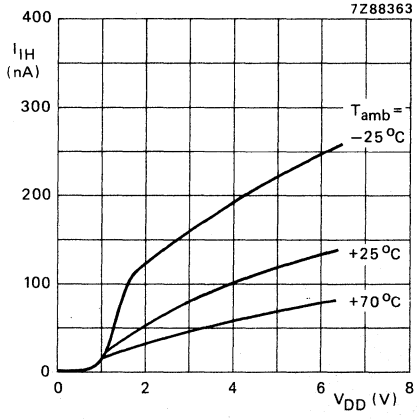


Fig. 14 Pull-down input current as a function of supply voltage at $V_I = V_{DD}$.

TYPICAL CURVES (continued)

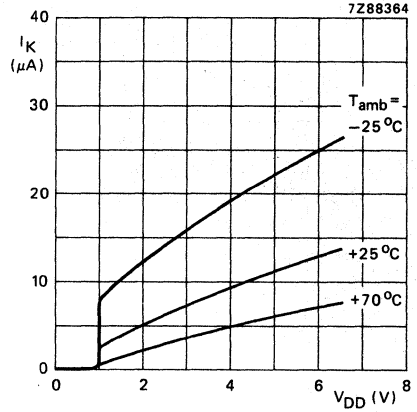


Fig. 15 Keyboard current as a function of supply voltage; X-pins connected to Y-pins.

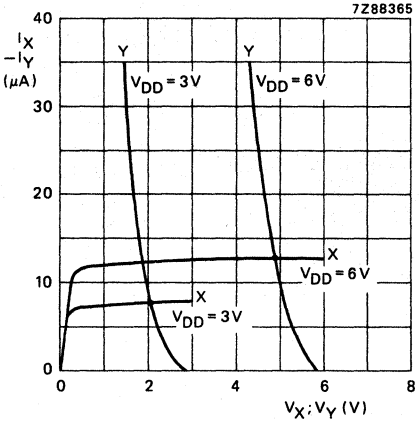


Fig. 16 Keyboard input characteristics at T_{amb} = 25 °C.

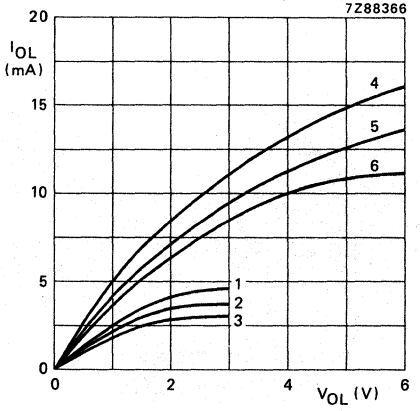


Fig. 17 Output (N-channel) sink characteristics for M1 and DP.

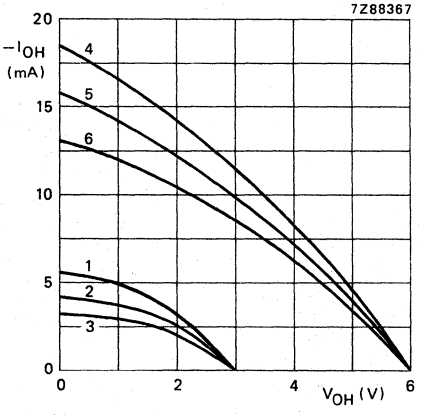


Fig. 18 Output (P-channel) source characteristics for M1 and DP.

Curves for Figs 17 and 18

T_{amb}	V_{DD} = 3 V	V_{DD} = 6 V
−25 °C	1	4
+25 °C	2	5
+70 °C	3	6

C-MOS INTERRUPTED CURRENT-LOOP DIALLING CIRCUIT

The PCD3326 is a single chip silicon-gate C-MOS integrated circuit. It is intended to convert pushbutton keyboard entries into streams of correctly-timed line current interruptions. The input data is derived from a telephone keyboard with a 3 x 4 pushbutton matrix. Numbers with up to 23 digits can be retained in a RAM for redial. A delayed reset is built-in for line power breaks.

The PCD3326 can regenerate access pauses during redial. During the original entry, access pauses are stored either automatically or via the keyboard. A regenerated access pause can be terminated during redial in three ways: automatically after a built-in time, or via the keyboard, or with an external dial tone recogniser circuit. This makes the circuit very suitable for redial in PABX (Private Automatic Branch Exchange) systems.

The circuit has the following features:

- Operation from 2,5 V to 6 V supply.
- Static standby operation down to 1,8 V.
- Low current consumption; typ. 40 μA.
- Low static standby current; typ. 1 μA.
- On-chip oscillator for 3,58 MHz crystal.
- Fully decoded and debounced inputs for 3 x 4 matrix keyboard.
- 23-digit capacity, including access pauses, for redial operation.
- Memory overflow possibility (with internally disabled redial).
- Selectable dialling pulse frequency: 10 kHz, 16 Hz and 20 Hz.
- Test pulse frequency: 932 Hz.
- Hold facility for lengthening the inter-digit period.
- Circuit reset for line power breaks; $>$ 160 ms (10 Hz dialling pulse frequency).
- Access pause generation automatically or via the keyboard.
- Access pause reset:
  automatically after 3 s or 6 s (10 Hz dialling pulse frequency),
  via the keyboard,
  with external tone recogniser.
- All inputs with pull-up/pull-down (except CE)
- All inputs are internally protected against electrostatic charges.
- High input noise immunity.

PACKAGE OUTLINES

PCD3326P: 18-lead DIL; plastic (SOT-102GE).

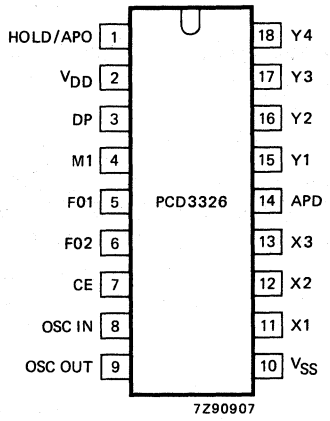


Fig. 1 Pinning diagram.

PINNING

2	V_{DD}	positive supply
10	V_{SS}	negative supply

Inputs

5	F01	the dialling pulse frequency is defined by the logic state of these two inputs
6	F02	
7	CE	Chip Enable; used to initialize the system; to select between the operational mode and the static standby mode; to handle line power breaks
11	X1	column keyboard inputs with pull-down on chip
12	X2	
13	X3	
14	APD	Access Pause Delay; selects the maximum duration of an access pause.
15	Y1	row keyboard inputs with pull-up on chip
16	Y2	
17	Y3	
18	Y4	

Outputs

3	DP	Dialling Pulse; drive of the external line switching transistor or relay
4	M1	Muting; normally used for muting during the dialling sequence

Input/output

1	HOLD/APO	This pin will go HIGH when an access pasue code is read from the memory during pulsing and will interrupt dialling. It can also be externally controlled; it will interrupt dialling after completion of the current digit or immediately during an inter-digit pause (t_{id}); further keyboard data will be accepted.

Oscillator

8	OSC IN	input and output of the on-chip oscillator
9	OSC OUT	

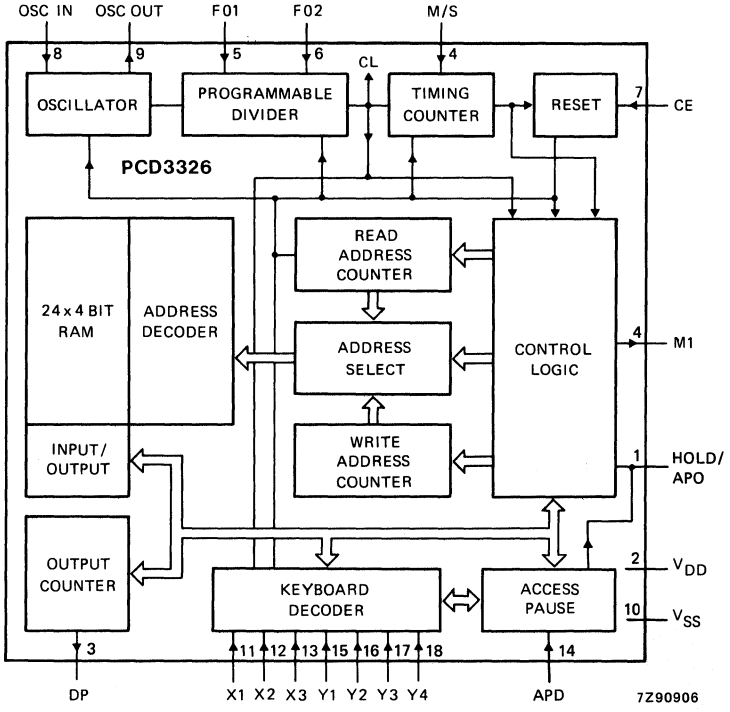


Fig. 2 Block diagram.

FUNCTIONAL DESCRIPTION (see also Fig. 2)

Clock oscillator (OSC IN, OSC OUT)

The time base for the PCD3326 is a crystal controlled on-chip oscillator which is completed only by connecting a crystal between the OSC IN and OSC OUT pins. The oscillator is followed by a frequency divider of which the division ratio can be externally set (F01 and F02) to provide one of four chip system clocks; three 'normal' clock frequencies and one higher test frequency.

Alternatively, the OSC IN input may be driven from an external clock signal.

Chip Enable (CE)

The CE input is used to initialize the chip system.

CE = V_{SS} provides the static standby condition. In this mode the clock oscillator is off and internal registers are clamped reset with the exception of the WRITE ADDRESS COUNTER (WAC). The keyboard input is inhibited, but data previously entered is saved in the RAM.

When CE = V_{DD} the clock oscillator is operating, the internal registers are enabled and data can be entered from the keyboard.

If the CE input is taken to a LOW level for more than the time t_{rd} (see Figs 5 and 6 and timing data) an internal reset pulse will be generated at the end of the t_{rd} period. The system is then in the static standby mode. Short CE pulses of $< t_{rd}$ will not affect the operation of the circuit. No reset pulses are then produced.

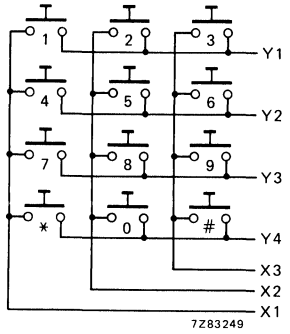
Debouncing keyboard entries

The column keyboard inputs to the integrated circuit (X_n) and the row keyboard inputs (Y_n) are for direct connection to a 3 x 4 single contact keyboard matrix (with or without common contact) as shown in Fig. 3, or to a double contact keyboard with a common left open (see Fig. 4). An entry is decoded into a 4-bit binary keycode by the keyboard decoder when one column input is connected to one row input or, when one column input is set HIGH and one row input is set LOW. Any other input combinations will be judged to be not valid and will not be accepted. Valid inputs are debounced on the leading and trailing edges as shown in Fig. 5. Keyboard entries are only decoded into 4-bit binary keycodes and written into the RAM if the keyboard contact remains closed for four or five clock pulse periods (entry period t_e). The next keyboard entry will not be accepted until the previously closed contact has been open for three or four clock pulse periods. The one clock pulse period of uncertainty in the debouncing process arises because keyboard entries are not detected until the trailing edge of the first clock pulse after the entry.

Data entry

After each keyboard entry has been debounced and decoded, the keycode is written into the RAM, and the WAC is incremented by one to select the next RAM location where the next keycode will be stored. As each keycode is recalled from the RAM for line pulsing, the READ ADDRESS COUNTER (RAC) is incremented by one to select the RAM location of the next keycode to be recalled. Consequently, the difference between the contents of the WAC and of the RAC represents the number of keycodes that have been written into the RAM but not yet converted into line pulses. If more than 23 keycodes are written into the RAM, memory overflow results and the excess keycode replace the data in the lower numbered RAM locations. In this event, since an erroneous number is stored, automatic redialling is inhibited until the WAC has been reset by the first digit entry of the next telephone call.

If the first pushbutton to be pressed is not redial (#), the WAC is reset during entry time t_e, the corresponding keycode is written into the first RAM location, and the WAC is then incremented by one. If the first pushbutton to be pressed is redial (#), the WAC is not reset and the keycodes stored in the RAM are sequentially recalled and converted into correctly timed dialling pulses at output DP. If the redial pushbutton (#) is operated again during the redialling sequence it will be decoded as an Access Pause Reset. This function will be described later during the description of the access pause system of the PCD3326. During redial no keyboard entry will be accepted and stored in the RAM. But, when all in the RAM stored numbers have been pulsed out, new keyboard entry will be accepted, stored at the RAM position after the last digit code of the original entry and converted into correctly timed dialling pulses.



★ Access pause set.

Redial or Access Pause Reset.

Fig. 3 Single contact keyboard.

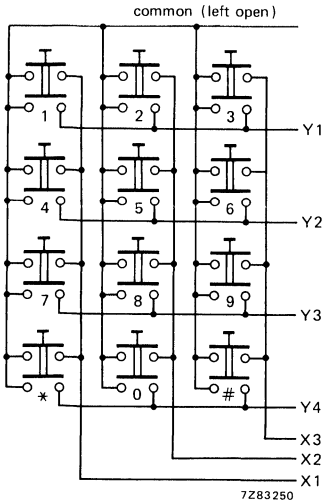


Fig. 4 Double contact keyboard.

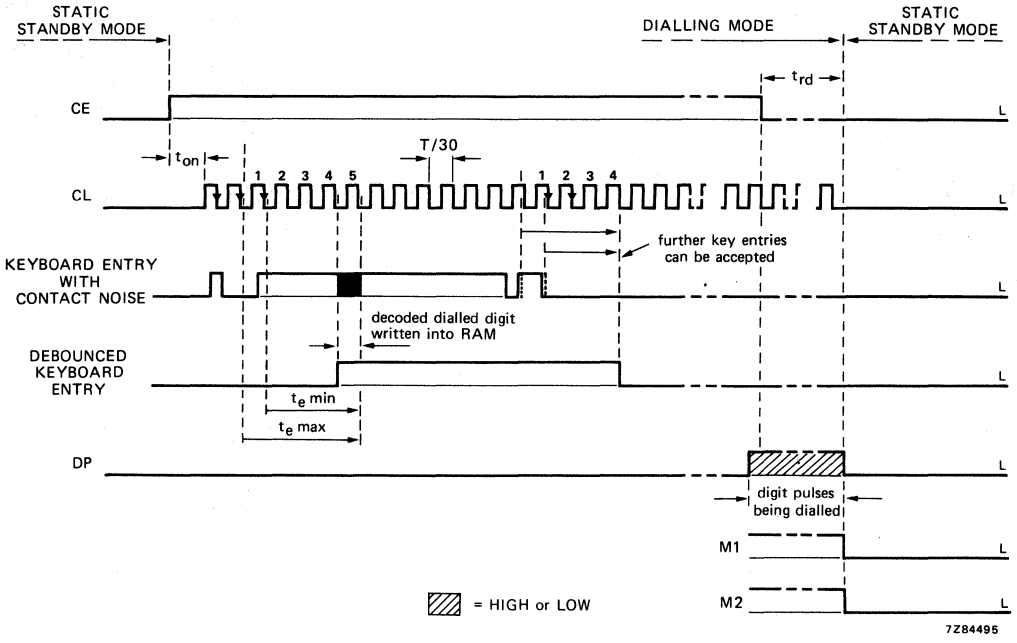


Fig. 5 Timing diagram showing clock start-up, keyboard entry debouncing and the effect of interrupting the supply to CE during the transmission of dialling.

N.B.: CL and M2 are internal signals.

Dialling sequence

The dialling sequence can be initiated under either of the following two conditions:

- The supply to the integrated circuit is derived from the telephone lines via the cradle contacts (power supply before keyboard entry); see Fig. 6.

Then, approximately 4 ms (t_{on}) after CE goes HIGH, the clock pulse generator starts and, ten clock pulse periods (t_d) later, a prepulse with a duration of ten clock pulse periods (t_d) appears at output M1. This prepulse ensures that, if a polarized muting relay with two stable positions is used, it switches to the de-muted position so that the circuit is then in the conversation mode whilst the subscriber awaits the dialling tone. When the first digit of the required number is entered at the keyboard, data entry period t_e commences.

- The supply to the integrated circuit is derived from the telephone lines via the cradle contacts in series with a common keyboard contact (Fig. 7).

When the first digit of the required number is entered at the keyboard, the common keyboard contact connects the line voltage to V_{DD} and CE becomes HIGH. Approximately 4 ms (t_{on}) after CE goes HIGH, the clock pulse generator starts and data entry period t_e commences. After period t_e, M1 goes HIGH and the pushbutton can be released. The supply to V_{DD} and CE is then maintained via the muting circuit controlled by M1.

The further dialling sequence will be described with the aid of Fig. 6. When the keyboard entry has been decoded and written into the RAM, M1 goes HIGH to mute the telephone and an inter-digit pause (t_{id}) ensues. M2 then goes HIGH (M2 is an internally generated signal, used for explanation only), the RAC addresses the RAM and the first keycode is loaded into the register of the output counter which generates the appropriate number of correctly-timed dialling pulses at output DP. When the digit has been pulsed out, M2 goes LOW, the RAC is incremented by one and the procedure repeats until the WAC and RAC contents are equal (all digits pulsed out). Output M1 then goes LOW, the circuit assumes the conversation mode. The circuit reverts to the static standby mode if CE goes LOW for more than the reset delay time (t_{rd} = 1,6 dialling pulse periods) at any time during the conversation or dialling mode (e.g. because the handset is replaced). CE remains LOW although V_{DD} is maintained by a back-up supply (e.g. because an external diode isolates CE from the back-up supply connected to V_{DD}). The RAM retains its contents for subsequent automatic redialling as long as the back-up supply maintains V_{DD} above V_{DDO} = 1,8 V.

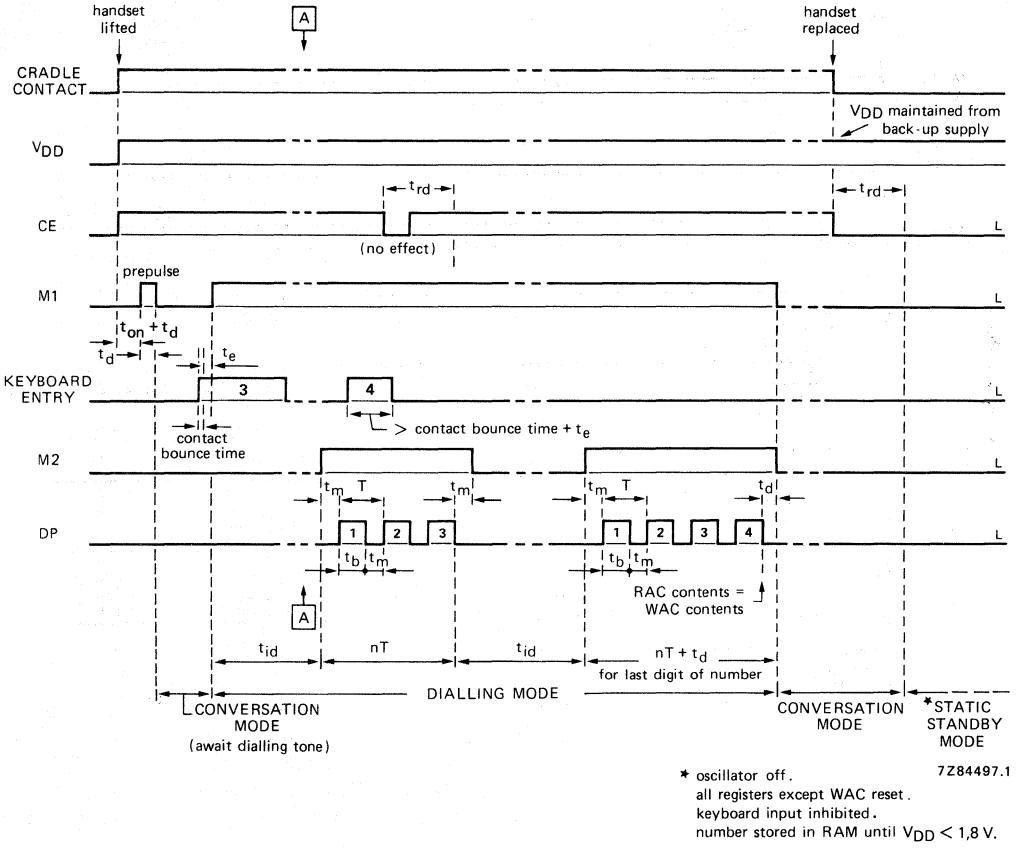


Fig. 6 Timing diagram of dialling sequence with V_{DD} and CE HIGH before keyboard entry (e.g. supply via the cradle contacts). M2 is an internal signal.

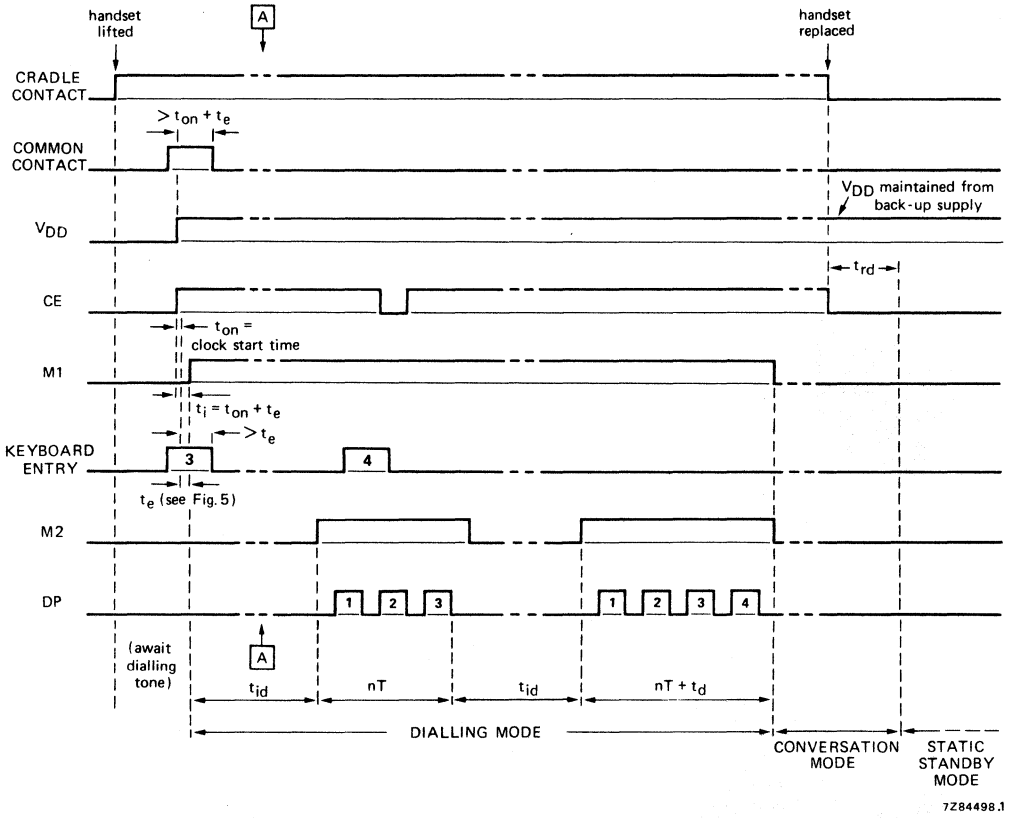


Fig. 7 Timing diagram for initiating the dialling mode with V_{DD} and CE initially supplied via the cradle contacts in series with a common contact on the keyboard. See Fig. 6 for pulse timings after point A. M2 is an initial signal.

Hold function

As shown in Fig. 8, the hold function allows the interval between consecutive pulsed digits to be prolonged under the control of external equipment. When the HOLD/APO is set HIGH, the dialling pulse train is interrupted as soon as M2 goes LOW to signal that the current digit has been pulsed out. In the hold condition, further keyboard entries will be accepted, debounced, decoded and stored in the RAM. No further keycodes will be read from the RAM and converted into dialling pulses on DP until the HOLD/APO is set LOW again and an inter-digit pause has elapsed.

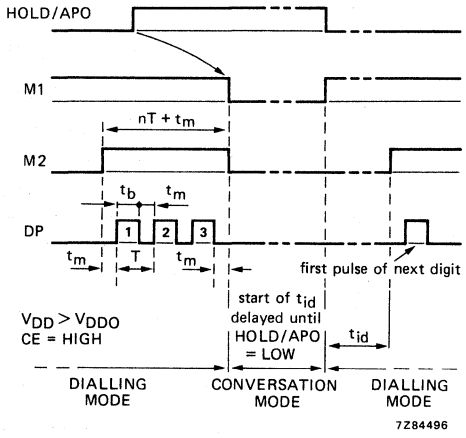


Fig. 8 Timing diagram showing the effect of activating the HOLD/APO during the transmission of dialling pulses. M2 is an internal signal.

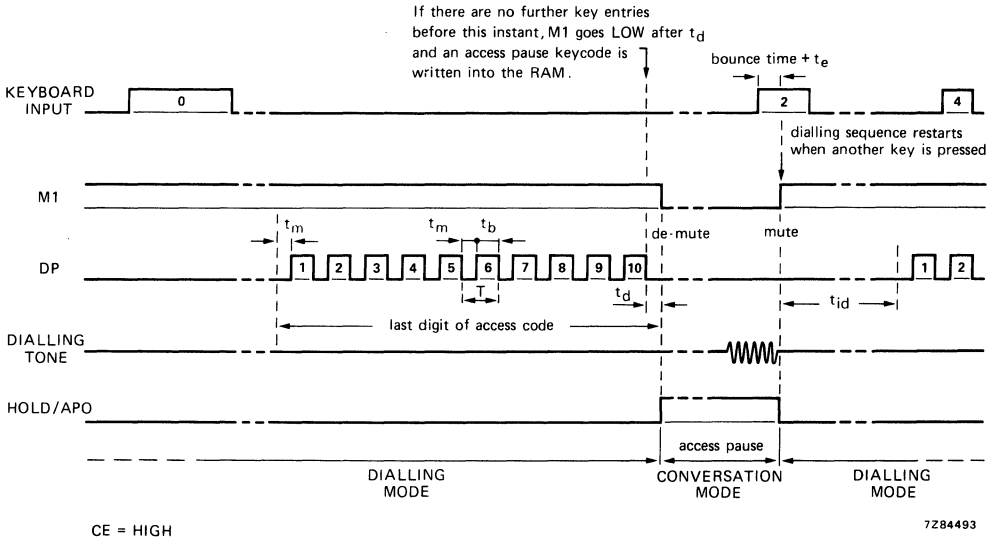
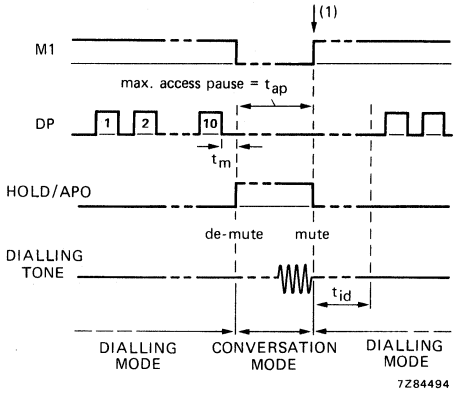


Fig. 9 Dialling sequence showing how an access pause code is automatically stored in the RAM for possible redialling if no further key entries are made until all of the previously entered digits have been transmitted. The dialling sequence continues when another key is pressed.

Access pause regeneration during redial

During original entry, access pause codes can be stored at the appropriate positions in the RAM. During redial the Access Pause Output (HOLD/APO)will go HIGH as soon as an access pause code is read from the RAM, thereby interrupting dialling until HOLD/APO is made LOW again as described above. In this way the normal inter-digit pause with a duration t_{id} can be replaced by a proper access pause. An access pause code is now automatically stored in the RAM during original entry, when M1 goes LOW, after all digits so far entered have been transmitted (see Fig. 6). This occurs between entering of the trunk exchange code and the subscriber code, whilst the access tone is available. Up to two access pauses can be entered into the RAM in this manner. Alternatively, the access pause key (★) can still be pressed to insert (more) access pauses manually (digits + access pauses $\leqslant 23$).
During redial, access pauses will be automatically regenerated.

Three methods of terminating an access pause:
1. Automatically, if the built-in time t_{ap} expires; HOLD/APO then goes LOW; tap can be set to one of two values with the Access Pause Delay (APD) select input.
2. Manually, by pressing the redial key before t_{ap} expires.
3. With an external tone recogniser, by forcing HOLD/APO to LOW or HIGH respectively, for shortening or lengthening an access pause.



(1) a. Access pause (t_{ap}) expires or press redial before end of t_{ap}.

b. HOLD/APO controlled by tone recogniser:
HOLD/APO forced to LOW before t_{ap} expires; access pause $< t_{ap}$
HOLD/APO forced to HIGH after t_{ap} expires; access pause $> t_{ap}$.

Fig. 10 Timing diagram showing Access Pause Reset.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_{DD}	−0,3 to 8 V
Voltage on any pin	V_I	V_{SS} −0,3 to V_{DD} + 0,3 V
Operating ambient temperature range	T_{amb}	−25 to +70 °C
Storage temperature range	T_{stg}	−55 to +125 °C

CHARACTERISTICS

V_{DD} = 3 V; V_{SS} = 0 V; crystal parameters: f_{osc} = 3,58 MHz, R_{Smax} = 100 Ω (note 3); T_{amb} = 25 °C; unless otherwise specified.

	symbol	min.	typ.	max.		conditions
Operating supply voltage	V_{DD}	2,5	3	6	V	T_{amb} = −25 to +70 °C
Standby supply voltage (note 1)	V_{DDO}	1,8	–	6	V	T_{amb} = −25 to +70 °C
Operating supply current	I_{DD}	–	40	–	μA	CE = V_{DD}; notes 2, 3
	I_{DD}	–	50	100	μA	CE = V_{DD}; V_{DD} = 6 V; notes 2, 3
Standby supply current	I_{DDO}	–	1	2	μA	CE = V_{SS}; note 2
	I_{DDO}	–	–	2	μA	V_{DD} = 1,8 V; T_{amb} = −25 to +70 °C
Input voltage LOW	V_{IL}	–	–	0,3 V_{DD}		1,8 V ⩽ V_{DD} ⩽ 6 V
Input voltage HIGH	V_{IH}	0,7 V_{DD}	–	–		1,8 V ⩽ V_{DD} ⩽ 6 V
Input leakage current; CE						
LOW	$-I_{IL}$	–	–	50	nA	CE = V_{SS}
HIGH	I_{IH}	–	–	50	nA	CE = V_{DD}
Pull-up input current M/S	$-I_{IL}$	30	100	300	nA	V_I = V_{SS}
Pull-down input current F01, F02, APD	I_{IH}	30	100	300	nA	V_I = V_{DD}
Matrix keyboard operation						
Keyboard current	I_K	–	10	–	μA	X connected to Y, CE = V_{DD}
Keyboard 'ON' resistance	R_{KON}	–	–	500	Ω	contact ON; note 4
Keyboard 'OFF' resistance	R_{KOFF}	1	–	–	MΩ	contact OFF; note 4
Other keyboard operation						
Input current for X_n 'ON'	I_{IH}	–	–	30	μA	V_I = 1,5 to 3 V
Input current for Y_n 'ON'	$-I_{IL}$	10	–	–	μA	V_I = 0 to 2,5 V
Input current Y_n	$-I_I$	–	–	0,7	mA	V_I = V_{SS}

Notes

1. V_{DDO} = 1,8 V only for redial.
2. All other inputs and outputs open.
3. Stray capacitance between pins 8 and 9 < 3 pF.
4. Guarantees correct keyboard operation.

CHARACTERISTICS (continued)

	symbol	min.	typ.	max.		conditions
Outputs M1, DP						
sink current	I_{OL}	0,7	1,5	3,2	mA	V_{OL} = 0,5 V
source current	$-I_{OH}$	0,65	1,3	2,7	mA	V_{OH} = 2,5 V
Latch output HOLD/APO						
sink current	I_{OL}	50	130	300	μA	V_{OL} = 0,5 V
source current	$-I_{OH}$	45	110	250	μA	V_{OH} = 2,5 V

TIMING DATA

V_{DD} = 2,5 to 6 V; V_{SS} = 0 V; f_{osc} = 0 V; f_{osc} = 3,579545 MHz

input levels of F01 and F02		V_{F01}	LOW	HIGH	LOW	HIGH		
(V_{SS} = LOW; V_{DD} = HIGH)		V_{F02}	LOW	HIGH	HIGH	LOW		conditions (note 3)
		symbol				(test mode)		
Dialling pulse frequency	$1/T_{DP}$	f_{DP}	10,13	15,54	19,42	939,2	Hz	note 1
Dialling pulse period	$1/f_{DP}$	T_{DP}	98,7	64,4	51,5	1,073	ms	
Clock pulse frequency	30 x f_{DP}	f_{CL}	303,9	466,1	582,6	27965	Hz	
Break time (note 2)	3/5 x T_{DP}	t_b	59,2	38,6	30,9	0,644	ms	M/S = H; n.c.
Make time (note 2)	2/5 x T_{DP}	t_m	39,5	25,8	20,6	0,429	ms	M/S = H; n.c.
Inter-digit pause	8 x T_{DP}	t_{id}	790	515	412	8,58	ms	
Reset delay time	1,6 x T_{DP}	t_{rd}	158	103	82,4	1,72	ms	
Access pause time	32 x T_{DP}	t_{ap}	3,16	2,06	1,65	0,034	s	ADP = L; nc
	64 x T_{DP}	t_{ap}	6,32	4,12	3,30	0,069	s	ADP = H
Prepulse duration	1/3 x T_{DP}	t_d	33	21,5	17,2	0,358	ms	
Debounce time								
min.	4/30 x T_{DP}	$t_{e\,min}$	13,2	8,58	6,87	0,143	ms	
max.	1/6 x T_{DP}	$t_{e\,max}$	16,5	10,7	8,58	0,179	ms	
Clock start-up time		$t_{on\,typ}$	4	4	4	4	ms	CE: V_{SS} → V_{DD} (note 4)
Initial data entry time (typ.)	$t_{on} + t_e$	t_i	18	14	12	4	ms	

Notes

1. Exactly 10 Hz with 3,5328 MHz crystal.
2. Mark-to-space ratio: 3:2.
3. In the n.c. (not connected) condition, the input is drawn to the appropriate state by the internal pull-up/pull-down current.
4. Stray capacitance between pins 8 and 9: < 3 pF.

TYPICAL CURVES

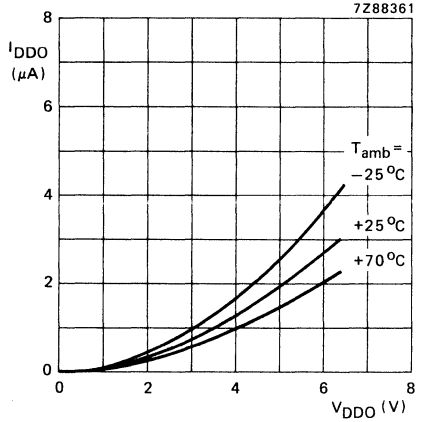


Fig. 11 Standby supply current as a function of standby supply voltage.

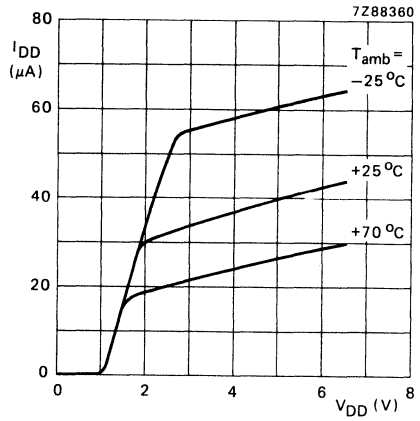


Fig. 12 Operating supply current as a function of operating supply voltage.

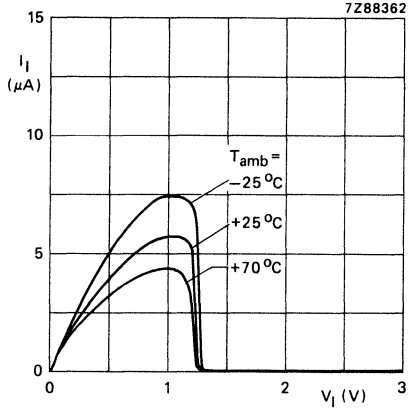


Fig. 13 Pull-down input current as a function of input voltage at V_{DD} = 3 V.

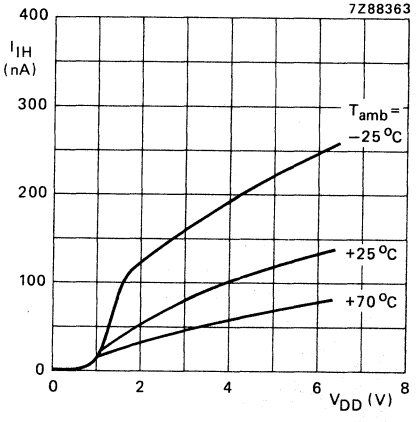


Fig. 14 Pull-down input current as a function of supply voltage at $V_I = V_{DD}$.

TYPICAL CURVES (continued)

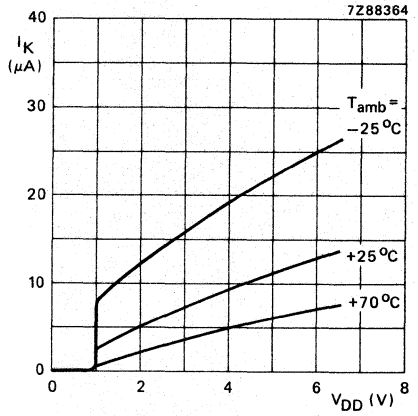


Fig. 15 Keyboard current as a function of supply voltage;
X-pins connected to Y-pins.

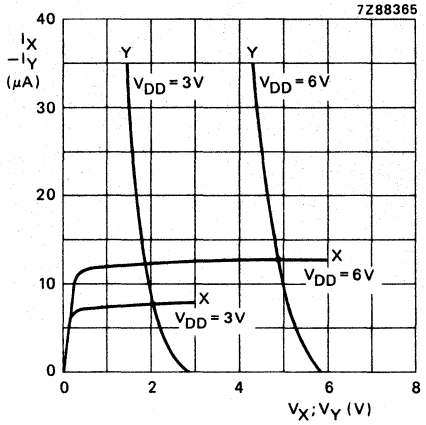


Fig. 16 Keyboard input characteristics at T_{amb} = 25 °C.

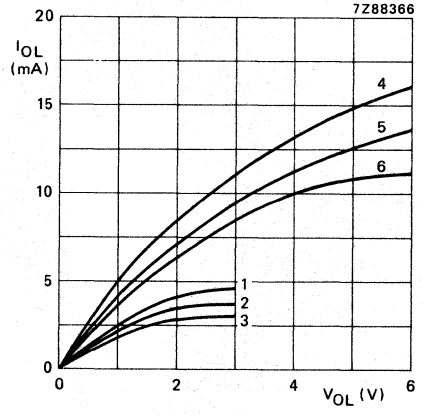


Fig. 17 Output (N-channel) sink characteristics for M1 and DP.

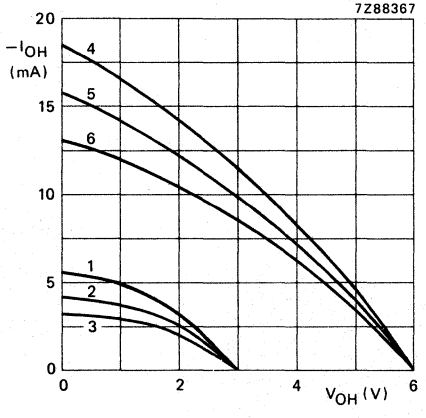


Fig. 18 Output (P-channel) source characteristics for M1 and DP.

Curves for Figs 17 and 18

T_{amb}	V_{DD} = 3 V	V_{DD} = 6 V
−25 °C	1	4
+25 °C	2	5
+70 °C	3	6

PULSE DIALLER WITH REDIAL

GENERAL DESCRIPTION

The PCD3327 is a single-chip silicon-gate CMOS integrated pulse dialler with radial function. The 455 kHz frequency reference for the on-chip oscillator is performed by an inexpensive ceramic resonator. It converts pushbutton keyboard entries into streams of correctly-timed line interruptions. The input data is derived from a telephone keyboard with a 3 x 4 pushbutton matrix. Numbers with up to 23 digits can be retained in a RAM for redial. A delayed reset is built-in for line power breaks in order to avoid untimely line interrupts.

Features

- Direct telephone line operation
- Inexpensive standard single-contact keyboard use
- Ceramic resonator for the frequency reference
- CMOS technology for low voltage operation (2,5 V to 6,0 V)
- Mark/space ratio selectable
- Redial facility with 23 digit capacity (memory overflow)
- Circuit reset for line power breaks
- Mute output
- Automatic reset of access pauses

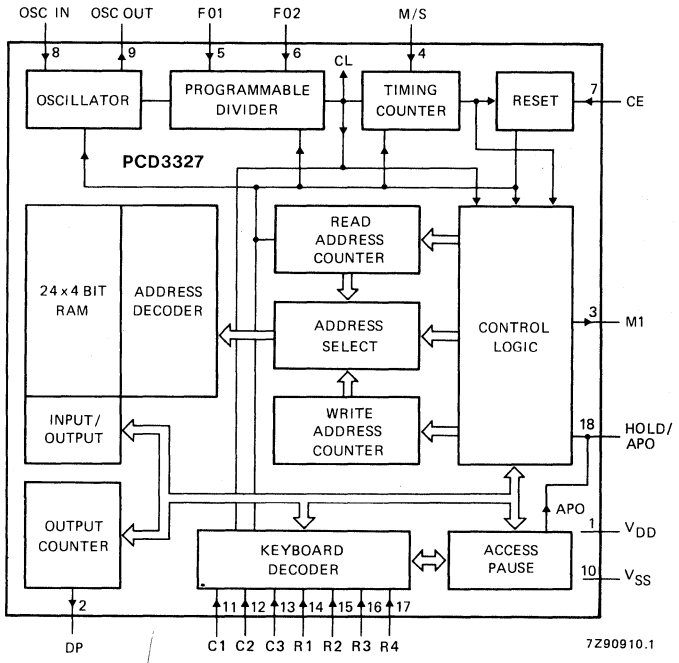


Fig. 1 Block diagram.

PACKAGE OUTLINES

PCD3327P : 18-lead DIL; plastic (SOT-102GE).
PCD3327U: die in trays.

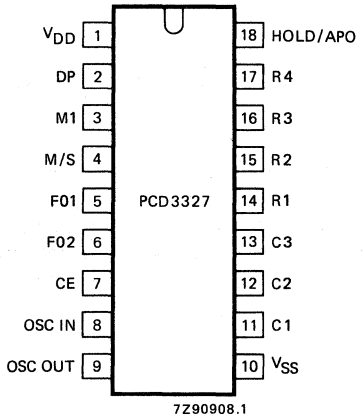


Fig. 2 Pinning diagram.

1	V_{DD}	positive supply
10	V_{SS}	negative supply

Inputs

4	M/B	mark/space input; controls the mark-to-space ratio of the line pulses
5	F01	the dialling pulse frequency is defined by the logic state of these two inputs
6	F02	
7	CE	Chip Enable; used to initialize the system; to select between the operational mode and the static standby mode; to handle line power breaks
11	C1	column keyboard inputs with pull-down on chip
12	C2	
13	C3	
14	R1	row keyboard inputs with pull-up on chip
15	R2	
16	R3	
17	R4	

Outputs

2	DP	Dialling Pulse; drive of the external line switching transistor or relay
3	M1	Muting; normally used for muting during the dialling sequence

Input/output

18	HOLD/AP0	This pin will go HIGH when an access pause code is read from the memory during pulsing and will interrupt dialling. It can also be externally controlled; it will interrupt dialling after completion of the current digit or immediately during an inter-digit pause (t_{id}); further keyboard data will be accepted.

Oscillator

8	OSC IN	input and output of the on-chip oscillator
9	OSC OUT	

FUNCTIONAL DESCRIPTION

Power supply (V_{DD}, V_{SS})

Pin 1 (V_{DD}) is the positive supply pin of the IC and the voltage is measured referenced to pin 10 (V_{SS}). This voltage must not exceed 6 V. For a redial operation, the RAM content is retained if V_{DD} does not drop below 1,8 V.

Oscillator input/output (OSC IN, OSC OUT)

The PCD3327 contains an oscillator with sufficient gain to provide oscillation when using an inexpensive 455 kHz ceramic resonator. In addition, two external capacitors are required (see Fig. 3). Alternatively, the OSC IN input pin may be driven from an external 455 kHz clock signal.

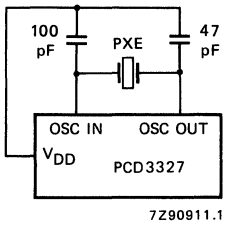


Fig. 3 Oscillator circuit.

Mark/space selection (M/S)

The mark/space ratio of the line pulse can be selected by connecting M/S (pin 4) to either V_{DD} or V_{SS} with mark/space ratio of 3 : 2 or 2 : 1 respectively (see also section Timing Data).

Chip enable (CE)

This input is used to control between the standby mode (ON-HOOK) and the operation mode (OFF-HOOK). When ON-HOOK (CE is LOW) the clock oscillator is off and the internal registers are clamped reset with the exception of the Write Address Counter (WAC). The keyboard input is inhibited, but data previously entered is saved in the RAM (under static standby condition).

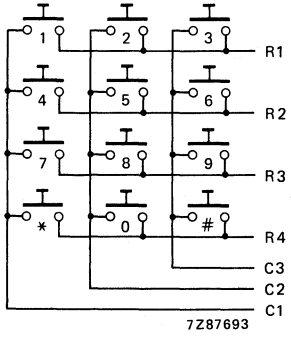
When OFF-HOOK (CE is HIGH) the clock oscillator is operating, the internal registers are enabled and data can be entered from the keyboard.

The CE input is also used to handle the line power breaks. If this input is taken to a LOW level for more than the time t_{rd} (see section Timing Data) an internal reset pulse will be generated at the end of the t_{rd} period. The system is then in the static standby mode. Short pulses ($< t_{rd}$) on the CE input will not affect the operation of the circuit and no reset pulses are then produced.

FUNCTIONAL DESCRIPTION (continued)

Keyboard inputs (R_n, C_n)

The column keyboard inputs (C_n) and the row keyboard inputs (R_n) are for direct connection to a 3 x 4 single contact keyboard matrix (see Fig. 4). Column and row keyboard inputs have on-chip pull-up and pull-down respectively. A valid key entry is defined by a single column input being connected to a single row input or, when a single column input is set HIGH and a single row input is set LOW. Any other input combinations will be judged to be not valid and will not be accepted. The valid inputs are debounced on the leading and trailing edges. Keyboard entries are only decoded into 4-bit binary keycodes and written into the RAM if the keyboard contact remains closed for four or five clock pulse periods. The next keyboard entry will not be accepted until the previously closed contact has been open for three or four clock pulse periods.



* Access pause set.

\# Redial or access pause reset.

Fig. 4 Single-contact keyboard.

Mute output (M1)

The M1 output is normally used for muting of the speech network during the dialling sequence. Figure 5 shows the timing diagram of the mute output (see also section Dialling Sequence).

Pulse output (DP)

This output is used to drive the external line switching transistor or relay. It provides the output pulse frequency with the correct Make/Break, the pulse rate and the inter-digit pause timing (see Fig. 5).

Dialling frequency selection (F01, F02)

The dialling pulse frequency is defined by the logic states of the inputs F01 and F02. With F01 = HIGH and F02 = LOW the device is in the test mode and the pulse frequency is increased by a factor 92 (see section Timing Data).

Dialling sequence

The dialling sequence can be initiated under the following condition:

- The supply to the integrated circuit is derived from the telephone lines via the cradle contacts (power supply before keyboard entry); see Fig. 5.

Then, approximately 4 ms (t_{on}) after CE goes HIGH, the clock pulse generator starts and, ten clock pulse periods (t_d) later, a prepulse with a duration of ten clock pulse periods (t_d) appears at the mute output M1. This prepulse ensures, that if a polarized muting relay with two stable positions is used, it switches to the de-muted position so that the circuit is then in the speech mode whilst the subscriber awaits the dialling tone. When the first digit of the required number is entered at the keyboard, data entry period t_e commences.

The further dialling sequence will be described with the aid of Fig. 5. When the keyboard entry has been decoded and written into the RAM, M1 goes HIGH to mute the telephone and an inter-digit pause (t_{id}) ensues. M2 Then goes HIGH (M2 is an internally generated signal, used for explanation only), the RAC (Read Address Counter) addresses the RAM and the first keycode is loaded into the register of the output counter which generates the appropriate number of correctly-timed dialling pulses at output DP. When the digit has been pulsed out, M2 goes LOW, the RAC is incremented by one and the procedure repeats until the WAC and RAC contents are equal (all digits pulsed out). Output M1 then goes LOW, the circuit assumes the speech mode. The circuit reverts to the static standby mode if CE goes LOW for more than the reset delay time (t_{rd} = 1,6 dialling pulse periods) at any time during speech or dialling mode (e.g. because the handset is replaced). CE remains LOW although V_{DD} is maintained by a back-up supply (e.g. is an external diode isolates CE from the back-up supply connected to V_{DD}). The RAM retains its contents for subsequent automatic redialling as long as the back-up supply maintains V_{DD} above V_{DD0} = 1,8 V.

Access pause generation during dial and redial

During original entry, access pause codes can be stored at the appropriate positons in the RAM. During radial the Access Pause Output (HOLD/APO) will go HIGH as soon as an access pause code is read from the RAM, thereby interrupting dialling until HOLD/APO is made LOW. In this way the normal inter-digit pause with a duration t_{id} can be replaced by a proper access pause. An access pause code is stored in the RAM during original entry by pressing the access pause key (*) between entering the trunk exchange code and the subscriber code, or at any other moment an access pause is required. The number of access pause that can be inserted in this manner is only limited by the capacity of the RAM (digits + access pauses < 23).

During redial, access pauses will be automatically regenerated.
Three methodes of terminating an access pause:

1. Automatically, if the built-in time t_{ap} expires; HOLD/APO then goes LOW.
2. Manually, by pressing the redial key before t_{ap} expires.
3. With an external tone recognizer, by forcing HOLD/APO to LOW or HIGH respectively, for shortening or lengthening an access pause.

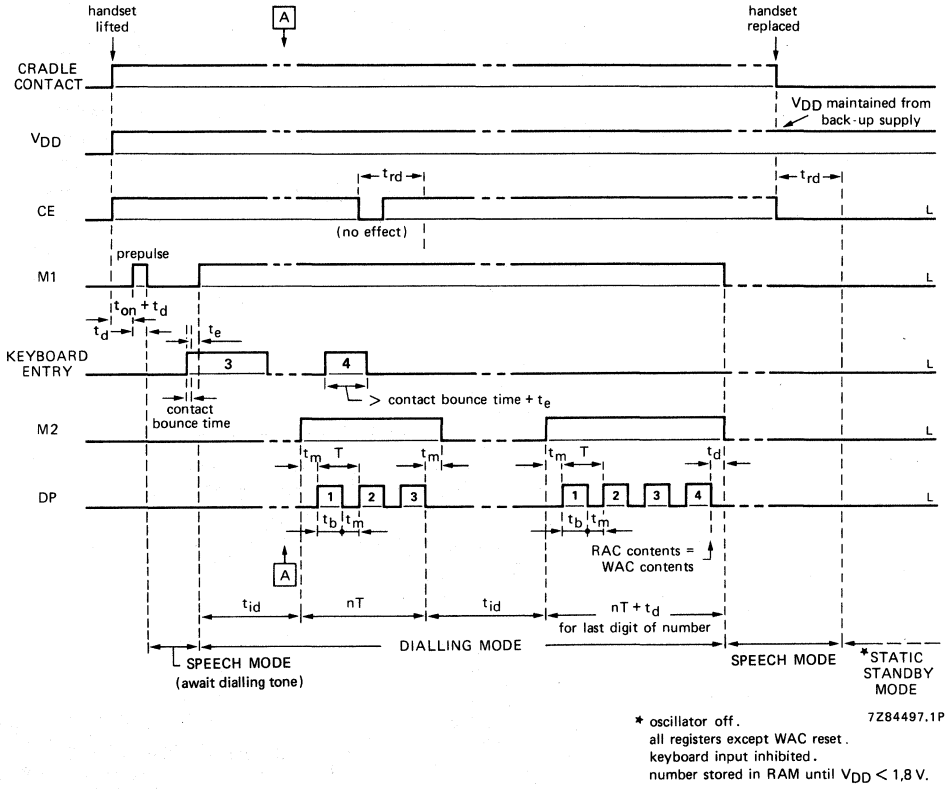


Fig. 5 Timing diagram of dialling sequence with V_{DD} and CE is HIGH before keyboard entry (e.g. supply via the craddle contacts). M2 is an internal signal.

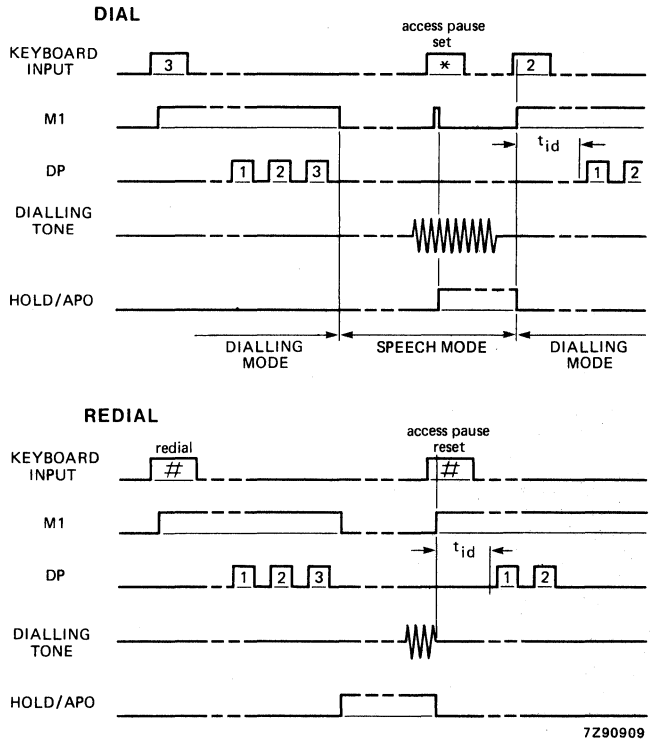


Fig. 6 Dialling sequence showing how an access pause code is stored in the RAM (DIAL) and how the access pause code is reset during the REDIAL.

Note: access pause can be reset before t_{ap} expires by pressing any key or by HOLD/APO forced to LOW.

DEVELOPMENT DATA

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage range	V_{DD}	−0,3	+ 8,0	V
Voltage on any input pin	V_I	V_{SS} − 0,3	V_{DD} + 0,3	V
Operating ambient temperature range	T_{amb}	−25	+ 70	°C
Storage temperature range	T_{stg}	−55	+ 125	°C

CHARACTERISTICS

V_{DD} = 3 V; V_{SS} = 0 V; ceramic resonator parameters: f_{osc} = 455 kHz, R_{Smax} = 12 Ω; $C_{o\,max}$ = 300 pF; T_{amb} = 25 °C; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit	conditions
Supply						
Operating supply voltage	V_{DD}	2,5	3,0	6,0	V	T_{amb} = −25 to + 70 °C
Standby supply voltage (note 1)	V_{DD0}	1,8	–	6,0	V	T_{amb} = −25 to + 70 °C
Operating supply current	I_{DD}	–	40	–	μA	CE = V_{DD}; note 2
	I_{DD}	–	50	100	μA	CE = V_{DD}; V_{DD} = 6 V; note 2
Standby supply current	I_{DD0}	–	1	5	μA	CE = V_{SS}; note 2
Inputs						
Input voltage LOW	V_{IL}	–	–	$0{,}3V_{DD}$	V	1,8 V < V_{DD} < 6 V
Input voltage HIGH	V_{IH}	$0{,}7V_{DD}$	–	–	V	1,8 V < V_{DD} < 6 V
Input leakage current						
CE input: LOW	$-I_{IL}$	–	–	50	nA	CE = V_{SS}
HIGH	I_{IH}	–	–	50	nA	CE = V_{DD}
Pull-up input current M/S	$-I_{IL}$	30	100	300	nA	V_I = V_{SS}
Pull-down input current; F01, F02	I_{IH}	30	100	300	nA	V_I = V_{DD}
Matrix keyboard operation						
Keyboard current	I_K	–	10	–	μA	CE = V_{DD}; note 3
Keyboard resistance						
"ON"	R_{KON}	–	–	500	Ω	contact ON; note 4
"OFF"	R_{KOFF}	1	–	–	MΩ	contact OFF; note 4
Other keyboard operation						
Input current						
C_n "ON"	I_{IH}	–	–	30	μA	V_I = 1,5 to 3 V
R_n "ON"	$-I_{IL}$	10	–	–	μA	V_I = 0 to 2,5 V
R_n	$-I_I$	–	–	0,7	mA	V_I = V_{SS}
Outputs						
Sink current						
M1, DP	I_{OL}	0,7	1,5	3,2	mA	V_{OL} = 0,5 V
HOLD/APO (latch)	I_{OL}	50	130	300	μA	V_{OL} = 0,5 V
Source current						
M1, DP	$-I_{OH}$	0,65	1,3	2,7	mA	V_{OH} = 2,5 V
HOLD/APO (latch)	$-I_{OH}$	45	110	250	μA	V_{OH} = 2,5 V

Notes to characteristics

1. V_{DD0} = 1,8 V only for redial.
2. All other inputs and outputs open.
3. C_n connected to R_n.
4. Guarantees correct keyboard operation.

DEVELOPMENT DATA

TIMING DATA

V_{DD} = 2,5 to 6 V; V_{SS} = 0 V; f_{osc} = 455 kHz

		V_{F01}	LOW	HIGH	LOW	HIGH		
		V_{F02}	LOW	HIGH	HIGH	LOW		
parameter		symbol				(test mode)	unit	conditions see also note 4
Dialling pulse frequency	$1/T_{DP}$	f_{DP}	10,3	15,8	19,7	948	Hz	note 1
Dialling pulse period	$1/f_{DP}$	T_{DP}	97	63	51	1,05	ms	
Clock pulse frequency	$30 \times f_{DP}$	f_{CL}	309	474	592	28 438	Hz	
Break time	$3/5 \times T_{DP}$	t_b	58	38	30	0,63	ms	note 2
Make time	$2/5 \times T_{DP}$	t_m	39	25	20	0,42	ms	note 2
Break time	$2/3 \times T_{DP}$	t_b	65	42	34	0,70	ms	note 3
Make time	$1/3 \times T_{DP}$	t_m	32	21	17	0,35	ms	note 3
Inter-digit pause	$8 \times T_{DP}$	t_{id}	776	506	405	8,4	ms	
Reset delay time	$1,6 \times T_{DP}$	t_{rd}	155	101	81	1,7	ms	
Access pause duration	$32 \times T_{DP}$	t_{ap}	3,11	2,03	1,62	0,034	s	
Prepulse duration	$1/3 \times T_{DP}$	t_d	32	21	17	0,35	ms	
Debounce time min.	$4/30 \times T_{DP}$	$t_{e\,min}$	13	8,4	6,7	0,14	ms	
max.	$1/6 \times T_{DP}$	$t_{e\,max}$	16	10,5	8,4	0,18	ms	
Clock start-up time; typical		$t_{on\,typ}$	4	4	4	4	ms	CE: $V_{SS} \rightarrow V_{DD}$
Initial data entry time; typical	$t_{on} + t_e$	t_i	18	14	12	4	ms	

Notes to timing data

1. f_{DP} is exactly 10 Hz with a 441,6 kHz PXE.
2. Mark-to-space ratio is 3 : 2; M/S is HIGH (not connected).
3. Mark-to-space ratio is 2 : 1; M/S is LOW.
4. In the not connected condition, the input is drawn to the appropriate state by the internal pull-up/pull-down current.

TYPICAL CURVES

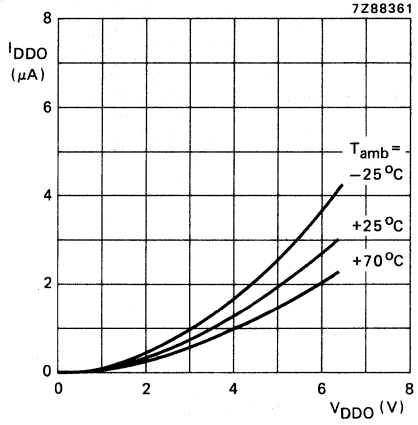


Fig. 7 Standby supply current as a function of standby supply voltage.

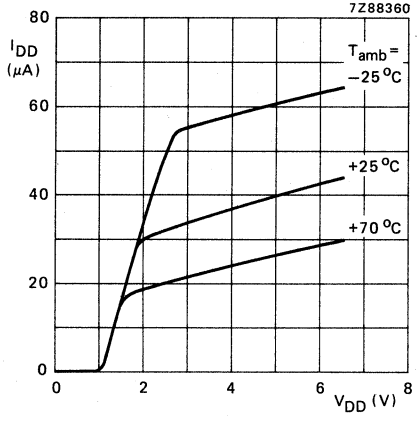


Fig. 8 Operating supply current as a function of operating supply voltage.

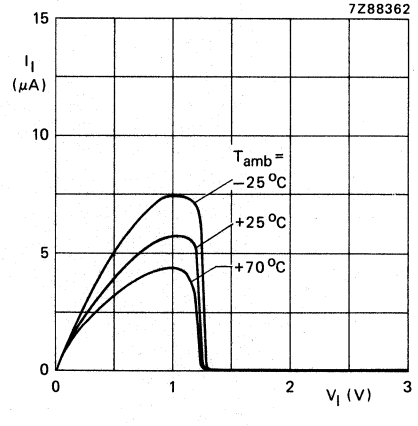


Fig. 9 Pull-down current as a function of input voltage at V_{DD} = 3 V.

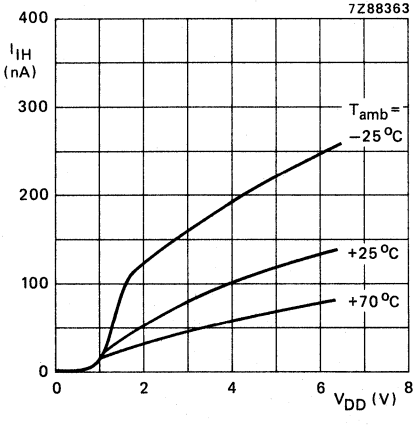


Fig. 10 Pull-down input current as a function of supply voltage at $V_I = V_{DD}$.

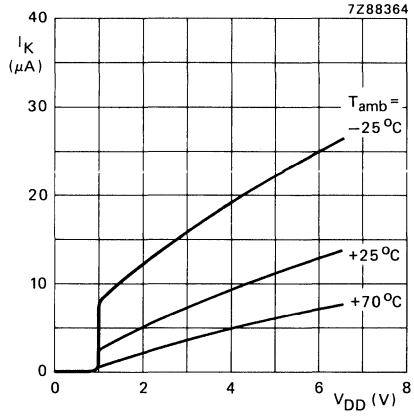


Fig. 11 Keyboard current as a function of supply voltage; R_n pins connected to C_n pins.

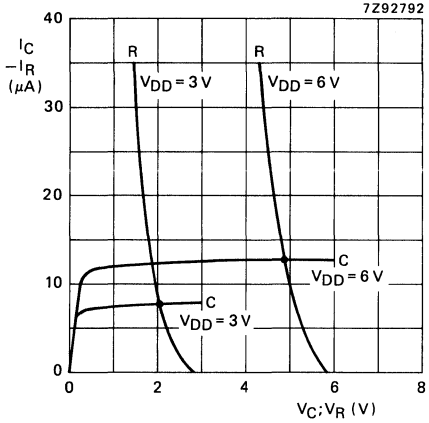


Fig. 12 Keyboard input characteristics at T_{amb} = 25 °C.

DEVELOPMENT DATA

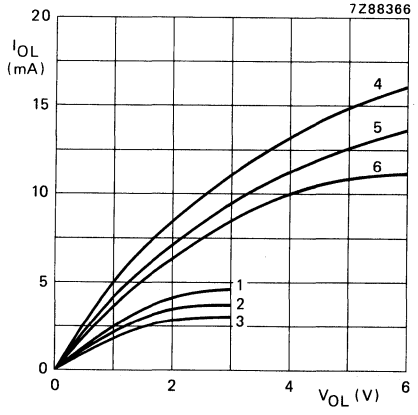


Fig. 13 Output (N-channel) sink characteristics for M1 and DP outputs.

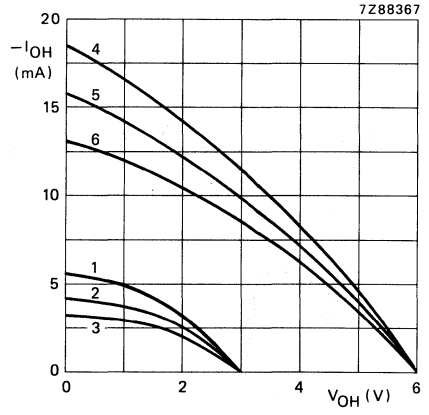


Fig. 14 Output (P-channel) source characteristics of M1 and DP outputs.

Curves for Figs 13 and 14

T_{amb}	V_{DD} = 3 V	V_{DD} = 6 V
−25 °C	1	4
+25 °C	2	5
+70 °C	3	6

CMOS REPERTORY DIALLER TELEPHONE SET CONTROLLER

GENERAL DESCRIPTION

The PCD3341 is a low threshold voltage IC fabricated in CMOS. It is designed to control display, redial and repertory dialling in a telephone set. The IC has two dialling modes; pulse dialling (PD) and dual tone multi-frequency (DTMF). The architecture of the PCD3341 is identical to that of the PCD3343. It comprises an 8-bit CPU, 224 RAM bytes and 3K ROM bytes (the ROM is already programmed). The operating supply voltage is 2,5 to 6,0 V with a low current consumption in all operating modes: standby, conversation and dialling modes.
Up to 18 digits and 2 manual access pauses can be stored for redial, extended redial and direct dial purposes together with on-chip storage for 10 repertory numbers.
For expansion of the system the PCD3341 provides a two wire serial input/output port, in accordance with the I²C bus specifications, to control the DTMF tone generator, LCD drivers and additional RAMs for additional repertory numbers.

Features

- Pulse dialling
- DTMF dial control of tone generator PCD3312
- Redial
- Extended redial
- Electronic notepad
- Direct dialling (emergency call)
- On-chip storage for 10 repertory dial numbers
- 18-digit capacity for each autodial memory
- Flash or register recall
- Access pause generation and termination
- Manual reset of autodial RAM
- On-chip power-on reset
- Programmed for improved noise immunity
- Extention possible with external RAM for up to 110 repertory dial numbers
- Uses standard 4 x 4 keyboard (single or double contact)
- Additional 10-digits first in first out memory, for infinite long numbers control an LCD via the I²C bus.
- Four extra function keys: program/autodial, flash, redial, access pause
- Keyboard expansion possible for 10 separated repertory dialled numbers
- Automatic recognition of PABX-digits; resulting in an access pause insertion
- Hold input and access pause output (APO) to adjust the duration of the access pause and facilitate use of tone recognizers
- Six diode or strap functions: mark-to-space ratio, tone burst time, inter-digit pause time, access pause time, normal or expanded keyboard, normal or direct dialling

QUICK REFERENCE DATA

Operating supply voltage	V_{DD}	2,5 to 6,0	V
Standby supply voltage	V_{DD}	min. 1,8	V
Operating currents at V_{DD} = 3 V			
conversation mode	I_{DDC}	typ. 270	μA
dialling mode	I_{DDD}	typ. 600	μA
Standby supply current			
at V_{DD} = 1,8 V; T_{amb} = 25 °C	I_{DDO}	typ. 1,2	μA
Crystal frequency	f	3,58	MHz
Operating ambient temperature range	T_{amb}	−25 to + 70	°C

PACKAGE OUTLINES

PCD3341P: 28-lead DIL; plastic (SOT-117).
PCD3341T: 28-lead mini-pack; plastic (SO-28; SOT-136A).

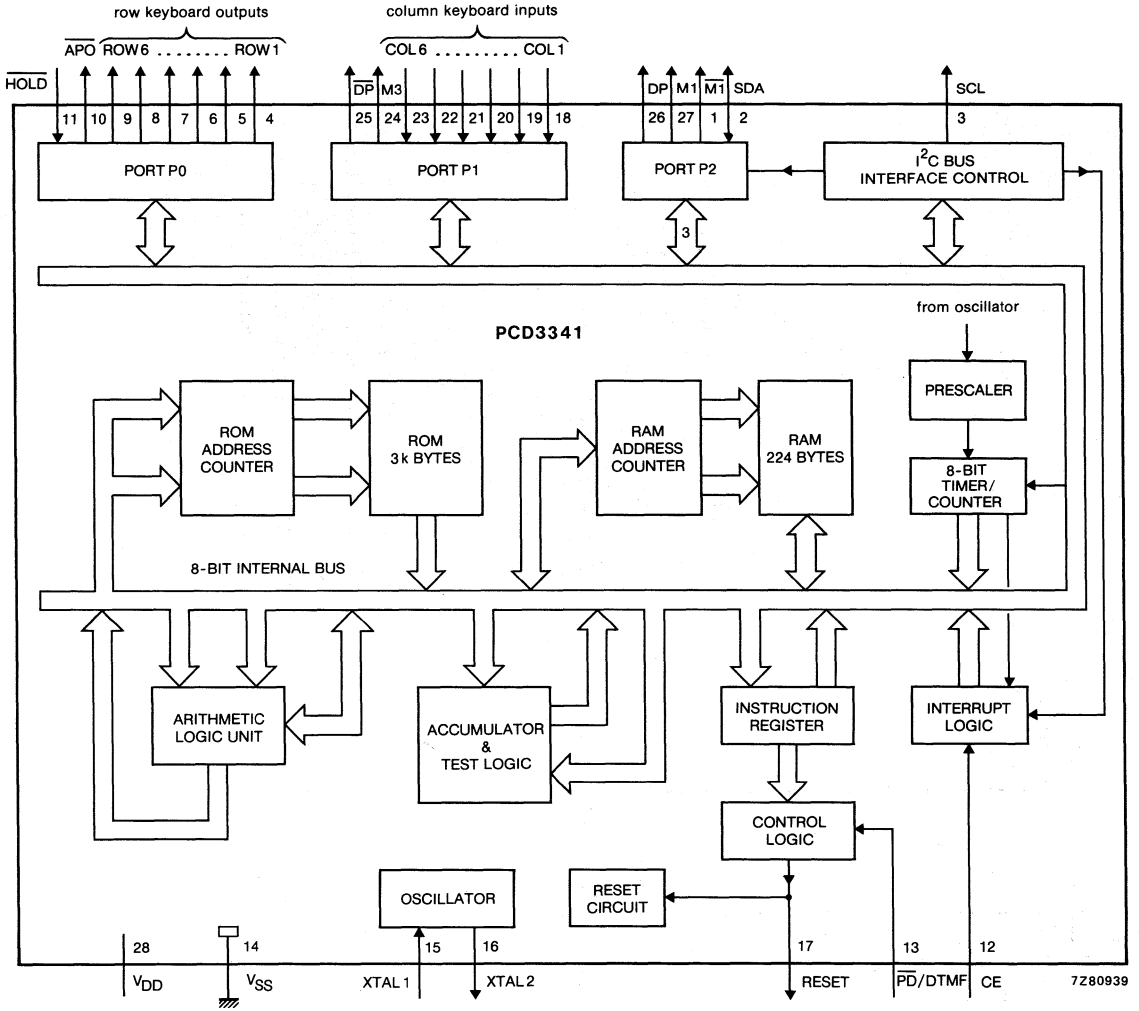


Fig. 1 Block diagram.

DEVELOPMENT DATA

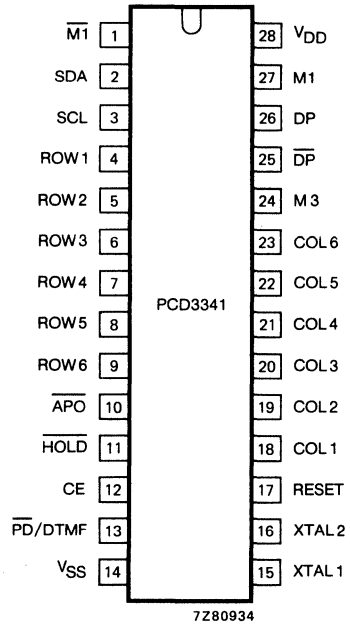


Fig. 2 Pinning diagram.

PINNING

1	$\overline{M1}$	inverted output of M1
2	SDA	serial data
3	SCL	serial clock
4	ROW 1	scanning row keyboard outputs
5	ROW 2	
6	ROW 3	
7	ROW 4	
8	ROW 5	
9	ROW 6	
10	$\overline{APO}$	access pause output
11	$\overline{HOLD}$	hold input
12	CE	chip enable input
13	$\overline{PD}$/DTMF	input to select pulse or DTMF dialling
14	V_{SS}	negative supply
15	XTAL 1	input to on-chip oscillator
16	XTAL 2	output from on-chip oscillator
17	RESET	reset input/output
18	COL 1	sense column keyboard inputs
19	COL 2	
20	COL 3	
21	COL 4	
22	COL 5	
23	COL 6	
24	M3	muting output
25	$\overline{DP}$	inverted pulse dialling output
26	DP	pulse dialling output
27	M1	muting output
28	V_{DD}	positive supply

FUNCTIONAL DESCRIPTION

Power supply (V_{DD}; V_{SS})

Power supply must be retained for data storage.

Clock oscillator (XATL 1; XTAL 2)

The time base for the PCD3341 is a crystal controlled on-chip oscillator which is completed by connecting a 3,58 MHz crystal between XTAL 1 and XTAL 2. The oscillator starts when V_{DD} reaches the operating voltage level and CE = HIGH. The output XTAL 2 can be used to drive the oscillator input of the PCD3312.

Chip Enable (CE)

This active HIGH input is used to initialize part of the system, to select the operational or standby mode and to handle line power breaks.

Pulse dialling outputs (DP; $\overline{DP}$)

DP output drives an external switching transistor or relay in pulse dialling mode. This output is also used to pulse out a calibrated FLASH pulse (recall register) of 90 ms duration as soon as the keyboard input FLASH is activated by depressing the key F. The FLASH function acts like CE with respect to redial.

Muting outputs (M1; $\overline{M1}$; M3)

M1 output is used for muting during the dialling sequence. For pulse dialling M1 goes HIGH with the first inter-digit pause and remains active for 33 or 40 ms (mark-to-space selection) following the last break pulse after the last digit held in store has been transmitted. In DTMF dialling, input $\overline{PD}$/DTMF is HIGH. M1 is HIGH as long as two out of the eight frequency signals are sent, then remains HIGH for an additional 80 ms (hold-over time).
$\overline{M1}$ output is the inverted output of M1.
M3 output is an AND function with $\overline{DP}$ and M1 as input, used for direct drive of a switching transistor for dialling pulses and muting.

Hold input ($\overline{HOLD}$); **access pause output** ($\overline{APO}$)

The hold input suspends dialling after completion of the current digit, or in pulse dialling during an inter-digit pause.
The hold function facilitates an extra time delay during dialling under control of external circuits (dialling tone recognizer). In the hold state ($\overline{HOLD}$ = LOW) the muting output is also LOW, thus the IC is in the conversation mode. The $\overline{HOLD}$ input can be controlled by the access pause output (APO) directly or indirectly via a dialling tone recognizer (see Fig. 3). The tone recognizer automatically terminates access pauses upon receipt of the access tone, regardless of whether this occurs during or after the access pause time (t_{ap}). The $\overline{APO}$ output will go LOW when an access pause is recognized.

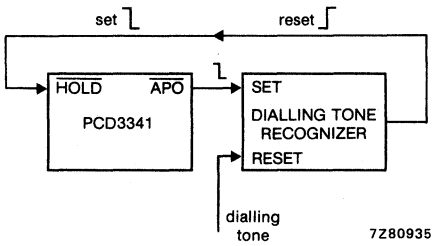


Fig. 3 Automatic variation of length of an access pause under control of a dialling tone recognizer.

Serial data (SDA); **serial clock** (see Fig. 8)

The serial I/O lines SDA and SCL are used to control the PCD3312 in the DTMF dialling mode, additional RAMs (PCD8570) for repertory dialling and LCD drivers (PCF8577). Both outputs require external pull-up resistors.

Keyboard inputs/outputs (COL 1 to 6; ROW 1 to 6)

The sense column inputs COL 1 to COL 6 and the scanning row outputs ROW 1 to ROW 6 are directly connected to a 4 x 4 single contact keyboard matrix. The keyboard organization is shown in Fig. 4.
In pulse dialling mode the valid keys are the 10 numeric keys (0 to 9). The 6 non-numeric keys (A, B, C, D, *, #) have no effect on the dialling.
In DTMF dialling mode the 10 numeric keys and the 6 non-numeric keys are valid. On-chip repertory dialling uses the 10 numeric numbers (no external RAM).
With extended repertory dialling 10 extra keys (M1 to M10) are used (on-chip or external RAM).
Row 5 of the keyboard contains the following special function keys:

- P memory clear and programming (notepad)
- FL flash or register recall
- R redial
- AP manual access pause entry

Diode options (ROW 6)

Row 6 is added to the keyboard matrix to provide the following selections:

Mark-to-space ratio (M/S)
OFF M/S 3:2
ON M/S 2:1

Tone burst time (t_{tb})
OFF t_{tb} = 70 ms
ON t_{tb} = 100 ms

Inter-digit pause (IDP)
OFF IDP = 900 ms
ON IDP = 500 ms

Access pause time (t_{ap})
OFF t_{ap} = 1,5 s (DTMF); 3 s (PD)
ON t_{ap} = 2,5 s (DTMF); 5 s (PD)

Keyboard expansion (EKB)
OFF normal keyboard
ON expanded keyboard

Normal/direct call (N/D)
OFF normal call mode
ON direct call (emergency)

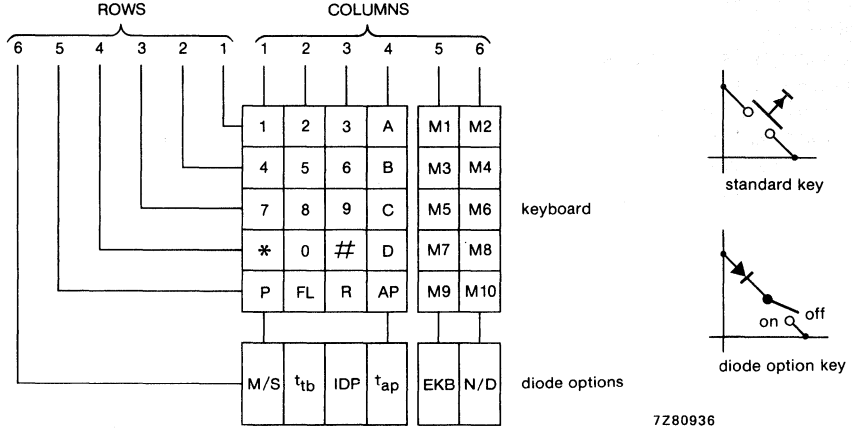


Fig. 4 Keyboard organization.

FUNCTIONAL DESCRIPTION (continued)

Dialling mode selection input ($\overline{PD}$/DTMF)

This input selects the dialling mode:

- $\overline{PD}$/DTMF = LOW selects pulse dialling
- $\overline{PD}$/DTMF = HIGH selects DTMF dialling

Reset input/output (RESET)

When the reset input is active HIGH it can be used to initialize the IC.
In normal application this is achieved by the CE input.
Reset is also an output of the internal power-on-reset circuit, which generates a reset pulse if V_{DD} drops below 1,3 V (typ.).

OPERATION

The PCD3341 has 3 operating modes:

- Standby
- Conversation
- Dialling

Standby mode

When the chip enable input (CE) is LOW the IC is disabled. In the standby mode the only current drawn is from a back up supply (battery or line powered), for memory retention, holding up to 13 call numbers for repertory and redialling.

Conversation mode

After the handset is lifted CE is activated and V_{DD} rises to the working voltage. M1 muting is inactive and speech or dial tone can be heard. With the oscillator operating the chip is ready to accept keyboard entries. Current consumption is $< 300\ \mu A$.

Dialling mode

The dialling mode starts with first valid keyboard entry when it initiates:

- a normal call of a newly dialled number
  or
- a repertory or redialling cycle of previously entered and stored numbers

The current consumption is $< 600\ \mu A$.

Pulse dialling ($\overline{PD}$/DTMF = LOW)

The keyboard entry initiates a recall from a previously stored number or is a simultaneous keying-in and pulsing-out activity, with storing for possible later recall. If in the recalled number or at keying-in the keys *, #, A, B, C, D keys are used these digits will not be transmitted. Normally, keying-in is faster than pulsing-out (fed from the redial register). Pulsing sequences start with M1 going HIGH followed by an inter-digit pause of 900 or 500 ms duration (diode option IDP), followed by a sequence of pulses corresponding to the present digit in store. Each pulse starts with a mark (line break) followed by space (line make).
The pulse period is 100 ms with a mark-to-space ratio of 3:2 or 2:1 (diode option). After transmission os a digit, the next digit will be processed again starting with an inter-digit pause. The pulsing is suspensed if $\overline{HOLD}$ goes LOW. It will be terminated if the current memory content has been transmitted or the handset is replaced (CE = LOW $< t_{rd}$). The pulses are available on the DP line.
After completion of the number string M1 goes LOW and the circuit changes from dialling mode to conversation mode.

Dual Tone Multi Frequency dialling ($\overline{PD}$/DTMF = HIGH)

The PCD3341 converts keyboard inputs into serial data, via the I^2 bus lines SDA and SCL, suitable for control of the PCD3312 DTMF tone generator. These tones are transmitted with minimum tone burst durations of 70, 70 ms. The maximum tone burst duration is equal to the key depression time. With redial and repertory dialling tones are automatically fed at a rate of 70, 70 ms. After dialling the muting output goes LOW after a hold-over time of 80 ms and the circuit is switched to the conversation mode.

DEVELOPMENT DATA

SYSTEM EXTENSION

The PCD3341 can control the extensions of a telephone set via its I²C bus. Both in DTMF dialling and pulse dialling, an extended repertory dialler provides more than 10 stored on-chip numbers and the indication on a L.C. display of all keys pressed (programming or dialling procedure).
The following ICs can be used in combination with the PCD3341:

- PCD3312 DTMF generator
- PCD8570 256 x 8 static CMOS RAM
- PCF8577 2 LCD drivers in LCD module

DTMF dialling

By using a PCD3312 DTMF generator with I²C bus interface, the PCD3341 may be extended to Dual Tone Multi Frequency dialling applications. This is selected when the input pin $\overline{PD}$/DTMF = HIGH. DTMF dialling is much faster than pulse dialling. Each keypad digit corresponds to a unique combination of two frequencies; one from a group of 4 high frequencies, and one from a group of 4 low frequencies. Both frequencies are applied simultaneously to the line.
The PCD3341 is capable of directly driving the PCD3312 oscillator.

Repertory dialling

If more than 10 stored numbers are required repertory dialling can be extended by the I²C bus lines and external CMOS RAMs (PCD8570) with serial interface. With a RAM capacity of 256 x 8 bits another 20 stored numbers can be added. A maximum of 5 external RAMs can be served by the PCD3341 directly. This provides a telephone with a total capacity of 110 (100) stored numbers.
The number of external RAMs connected on the I²C bus lines is automatically checked by the PCD3341 at initial turn-on.
To identify each RAM, the PCD8570 has 3 hardware address pins (A2, A1, A0) which allows a maximum of 8 RAMs to be connected.

Table 1 Repertory number organisation

PCD8570 address			Keyboard digit(s)	
A2	A1	A0	Without EKB	With EKB
0	0	0	10 to 29	00 to 19
0	0	1	30 to 49	20 to 39
0	1	0	50 to 69	40 to 59
0	1	1	70 to 89	60 to 79
1	0	0	90 to 99	80 to 99
PCD3341			00 to 09	M1 to M10

Display

To display the dialled phone number or programmed number the PCD3341 provides the signals to control a LC Display module using two PCD8577 duplex drivers. These signals are fed via the I²C bus lines.
In the dialling and programming modes the digits are displayed from right to left in the sequence entered by the keyboard. The access pause is indicated by the bar. If the number of digits exceeds 16, they drop out on the left side of the display.

OPERATING PROCEDURE

Initialization

At the first application of the standby power supply, the PCD3341 will clear the RAM in order to avoid a wrong content.
By lifting the handset the buffer capacitor for V_{DD} is charged to the operating voltage. CE will than be activated. Within start-up time the oscillator starts and the initialization program begins.

Automatic access pause setting

Before the start procedure, the system can also be initialized by setting the access pause system (e.g. for PABX applications). The circuit will automatically insert an access pause after recognition of access of a number within a digit group. This (or these) digit(s) must be programmed. Up to a maximum of 3 digits per group can be programmed.
The procedure is as follows:

- Depress and hold pushbutton P
- Press and release pushbutton R
- Enter 1, 2 or 3 digits as access digit for first group
- Release pushbutton P (only if no second group is required)
- Press and release pushbutton R
- Enter 1, 2 or 3 digits for second group
- Release pushbutton P

Apart from the procedure that automatically detectes and insertes access pause(s), a telephone number with up to 2 additional manually inserted access pauses can be dialled or programmed, by pressing button AP. In DTMF dialling mode each access pause has a duration of 1,5 or 2,5 seconds. In PD mode each access pause has a duration of 3 or 5 seconds.

Data entry

The debounce keyboard entries are written into the on-chip CMOS RAM in consecutive order.

Dialling

If the first pushbutton pressed is 0 to 9 in pulse dialling or 0-9, A to D, *, # in DTMF dialling, digits are entered into the redial register after initial clearing. During the data entry the circuit starts with the transmission of the call and is unaffected by the speed of entry. Transmission continues as long as further data input has to be processed. Up to 18 digits can be stored in the redial register. After the main store overflows, a 10 digit First-In First-Out register (FIFO) takes over as buffer. After transmitting the first digit of the FIFO register this position is automatically cleared to provide space for the storage of new data. In this way, the total number that can be transmitted is unlimited, provided the key-in rate is not excessive. However, if the FIFO register overflows (more than 10 digits in store) further input will be ignored.

Redial

If the first digit entered is "REDIAL" R, the stored number in the redial register will be recalled and transmitted.
If the current content is less than 18 digits, new digits entered are appended automatically to the redial number. After the 18th digit has been entered the FIFO register will take over as previously described in the dialling section.

OPERATING PROCEDURE (continued)

Extended Redial

The dialled number is saved in the extended redial buffer if pushbutton P is the last key pressed before the handset is replaced.
By pressing and releasing pushbutton P followed by pressing and releasing pushbutton R, will cause the extended redial register to be recalled and transmitted in the same manner as by redial. If less than 18 digits are contained in the extended redial register, digits can be added until the total content is 18. After the 18th digit the FIFO register will take over as before. The original number is not affected by the new digits

Direct call/Emergency call

This is a diode option usually operated by a turn key switch. If set the programmed number will be dialled by pressing ANY key. In normal mode the turn key switch is positioned OFF with the diode option OFF.
Programmed is achieved by lifting the handset, depressing the P pushbutton with key in the OFF position, then turning the key switch to ON position (diode option ON). The required telephone number is now entered. Pushbutton P can now be released and the handset replaced.
After programming, the key switch can remain in the ON position (activating emergency call) or be switched off (normal mode). If the key switch is the ON position, emergency calling is possible by removing the handset and pressing ANY pushbutton.

Repertory dialling

The PCD3341 has an on-chip CMOS RAM to store up to ten 18 digit numbers, and can be extended up to 100 (110) numbers using external CMOS RAMs with 2-line serial interface. The circuit automatically checks the number of external RAMs. If no external RAM is connected the on-chip repertory is limited to 10 numbers. In this application the standard keypad (0 to 9) and one digit address can be used. With the diode option EKB (expanded keyboard) ON the extended keypad matrix (M1 to M10) can be used to access the on-chip repertory. If external RAMs are connected the capacity of the repertory can be increased up to 100 (110) numbers. In this application the standard keypad (0 to 9) and/or the extended keypad (M1 to M10) can be used to access the repertory (see Table 1).
Programming is possible only after the handset is lifted and no pushbutton is operated before P.
Programming is achieved by pushbutton P being continually depressed, entering the repertory address of one or two digits, followed by the number (including access digits) then releasing pushbutton P.
The designated telephone number, including access digits, is dialled after pressing pushbutton P followed by the address. With extended keypad a single address pushbutton is required. After transmission of the repertory sequence, it is possible to manually enter additional digits (see redial).

Successive repertory dialling during a call (chain dialling)

It is possible to dial more than one repertory number during one single telephone call.
The following procedures are possible:

- Redial, extended redial or a repertory number followed by new digits
- Repertory number followed by one or more repertory numbers
- Normal dial, redial or extended redial followed by one or more repertory numbers

Note pad

Note pad provides the facility to store a number during conversation mode without dialling and muting. This number will be stored in the extended redial register and recalled with the extended redial procedure.
The programming procedure is as follows:

- Depress and release pushbutton P
- Depress and release pushbutton P
- Enter the telephone number
- Depress and release pushbutton P

If a wrond number is entered, correction is achieved by re-starting the programming procedure.

Memory clear

A built-in manually total clear facilitates resetting of the autodial RAM after servicing, maintenance or telephone set delivery.
The procedure is as follows:

- Hook-on, depress and keep depressed keys 2, 5, 8, 0
- Hook-off, release keys 2, 5, 8, 0

Table 2 Display indications

procedure	key procedure	display indication
Programming automatic access pauses after access digits	$\bar{P}$R00R9	Pr–00–9
dialling	004627530	00–4627530
redial	R	r=00–4627530
Extended redial		
programming	004627530P	00–4627530P
dialling	PR	Pr=00–4627530
emergency redial		
programming	N/D OFF, $\bar{P}$, N/D ON(+ TN)	PH–00–4627530
dialling	N/D ON any key	H=00–4627530
repertory programming	$\bar{P}$12004627530	P12–00–4627530
programming	$\bar{P}$12004627530	P12–00–4627530
dialling	P12	P12=00–4627530
repertory with extended keyboard		
programming	$\bar{P}$ M1 004627530	PM1–00–4627530
dialling	M1	M1=00–4627530
note pad programming	PP0080808P	7530PP00–808080P
note pad dialling	PR	00–808080
error	incorrect key procedure	≡

Where: TN = telephone number
P = depress and release pushbutton P
$\bar{P}$ = depress pushbutton P continually during programming
R = depress and release pushbutton R

RATINGS

Limiting values in accordance with the Absolute maximum System (IEC 134)

Supply voltage range (pin 28)	V_{DD}		−0,8 to 8	V
D.C. current into any input or output	$\pm I_I, \pm I_O$	max.	10	mA
All input voltages	V_I	V_{SS} −0,8 V to V_{DD}	+ 0,8	V
Total power dissipation	P_{tot}	max.	500	mW
Power dissipation per output	P_O	max.	50	mW
Storage temperature range	T_{stg}		−65 to + 150	°C
Operating ambient temperature range	T_{amb}		−25 to + 70	°C

DEVELOPMENT DATA

CHARACTERISTICS

V_{DD} = 3 V; V_{SS} = 0 V; crystal parameters: f_{osc} = 3,57954 MHz; R_S = 50 Ω max.; T_{amb} = 25 °C; unless otherwise specified.

parameter	symbol	min.	typ.	max.	unit
Supply					
Operating supply voltage	V_{DD}	2,5	3	6,0	V
Operating supply current					
conversation mode (CE = 1)	I_{DDC}	–	270	–	μA
dialling mode (CE = 1)	I_{DDD}	–	600	–	μA
Standby supply voltage (CE = 0)	V_{DDO}	1,8	3	6,0	V
Standby supply current (CE = 0)	I_{DDO}	–	–	2,5	μA
RESET I/O					
Switching level					
at $V_{DD} < V_{RESET}$	V_{RESET}	–	1,3	1,5	V
Sink current					
at $V_{DD} < V_{RESET}$	I_{OL}	–	7	–	μA
Inputs					
Input voltage LOW (any pin)	V_{IL}	0	–	$0{,}3V_{DD}$	V
Input voltage HIGH (any pin)	V_{IH}	$0{,}7V_{DD}$	–	–	V
Input leakage current; CE					
at $V_I = V_{SS}$ to V_{DD}	$-I_{IL}$	–	–	100	nA
at CE = 1	I_{IL}	–	–	1	μA
Keyboard contact resistance					
Keyboard ON	R_{KON}	–	–	1	kΩ
Keyboard OFF	R_{KOFF}	100	–	–	kΩ
Outputs					
M1, $\overline{M1}$, M3, DP, $\overline{DP}$					
Output sink current					
at V_{OL} = 0,4 V	I_{OL}	–	1,5	–	mA
Output source current					
at V_{OH} = 2,6 V (push-pull)	$-I_{OH}$	–	1,5	–	mA
SDA, SCL					
Output sink current					
at V_{OL} = 0,4 V	I_{OL}	1,5	–	–	mA
Output source leakage current					
at V_{OH} = 0 to V_{DD} (open drain)	$-I_{OH}$	–	–	1	μA

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Inputs/Outputs					
COL 1 to 6, ROW 1 to 6, $\overline{HOLD}$, $\overline{APO}$					
Output sink current					
at V_{OL} = 0,4 V	I_{OL}	0,6	1,5	–	mA
Output source current					
at V_{OH} = 2,6 V	$-I_{OH}$	25	–	–	μA
Output source current					
at $V_{OH} = V_{SS}$	$-I_{OH}$	–	–	200	μA
TIMING (see Figs. 5, 6 and 7)					
Clock start-up time	t_{ON}	–	–	10	ms
Oscillator period	C_P	–	–	0,279	μs
Pulse dialling ($\overline{PD}$/DTMF input LOW; M/S diode OFF)					
Mark-to-space ratio 3:2					
Dialling pulse frequency	f_{DP}	–	9,94	–	Hz
Dialling pulse period	t_{DP}	–	100,6	–	ms
Break time	t_b	–	60,3	–	ms
Make time	t_m	–	40,3	–	ms
Mark-to-space ratio 2:1 (M/S diode ON)					
Dialling pulse frequency	f_{DP}	–	9,94	–	Hz
Dialling pulse period	t_{DP}	–	100,6	–	ms
Break time	t_b	–	67	–	ms
Make time	t_m	–	33,5	–	ms
Access pause					
t_{ap} diode OFF	t_{ap}	–	3	–	s
t_{ap} diode ON	t_{ap}	–	5	–	s
Mute hold-over time during access pause	t_h	–	1	–	s
Inter-digit pause					
IDP diode OFF	t_{id}	–	892	–	ms
IDP diode ON	t_{id}	–	496	–	ms
Reset delay time	t_{rd}	–	160,9	180	ms
Reset delay time during access pause	t_{rd}	–	302	320	ms
Debounce time	t_e	13,5	–	–	ms
Flash pulse duration	t_{FL}	–	94	–	ms

parameter	symbol	min.	typ.	max.	unit
DTMF dialling ($\overline{PD}$/DTMF input HIGH; SDA timing via PCD3312)					
Tone transmission time (t_{tb} diode OFF)	t_t	–	74	–	ms
Tone break time	t_b	–	74	–	ms
Mute hold-over time during dialling	t_h	–	154	–	ms
Tone transmission time (t_{tb} diode ON)	t_t	–	101	–	ms
Tone break time	t_b	–	101	–	ms
Mute hold-over time during dialling	t_h	–	101	–	ms
Access pause					
t_{ap} diode OFF	t_{ap}	–	1,5	–	s
t_{ap} diode ON	t_{ap}	–	2,5	–	s
Mute hold-over time during access pause	t_h	–	1	–	s

DEVELOPMENT DATA

Timing diagrams

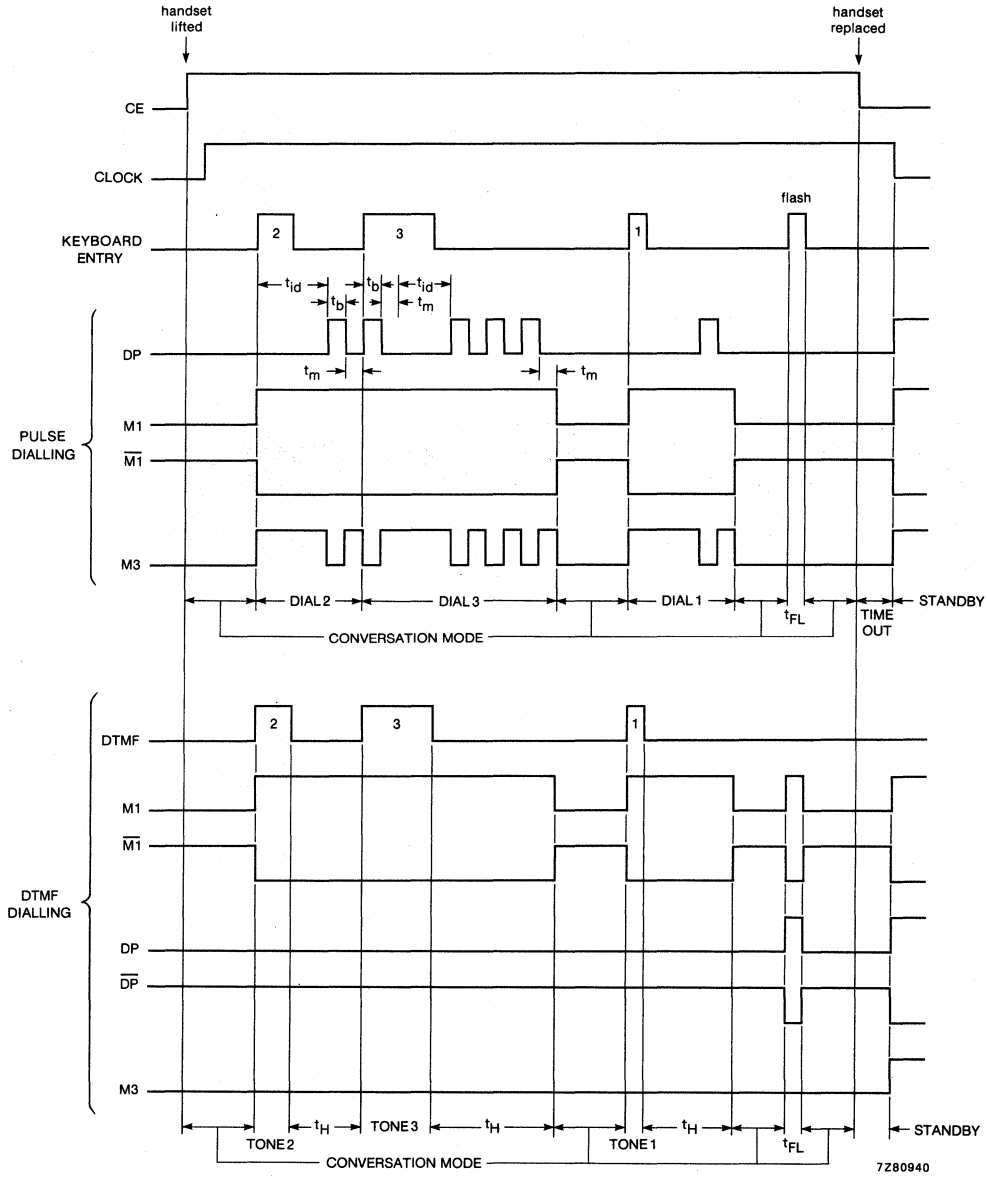


Fig. 5 Pulse dialling; DTMF dialling.

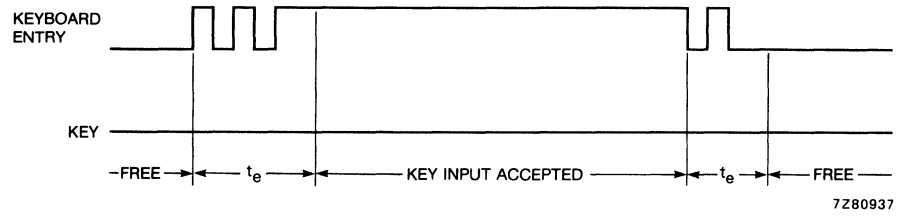


Fig. 6 Keyboard entry with noise debounced.

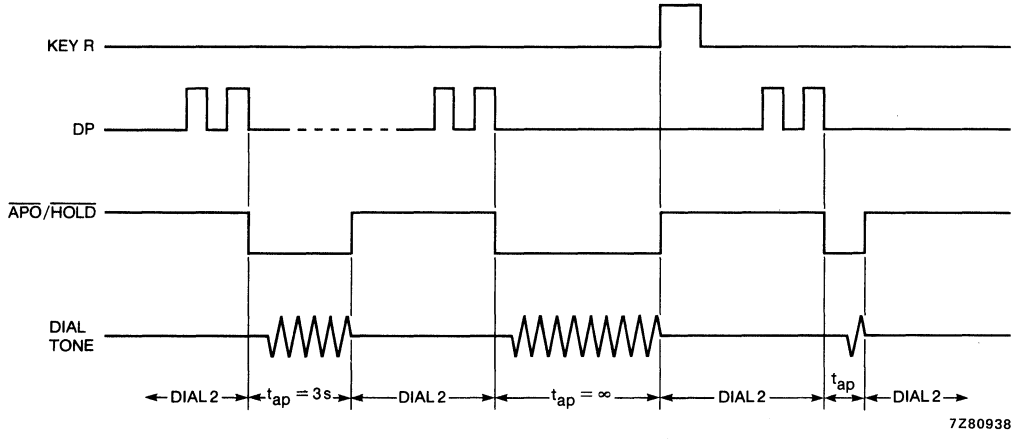


Fig. 7 Access pause with reset by; internal 3 s timer, key R, tone recognizer.

DEVELOPMENT DATA

Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

APPLICATION INFORMATION

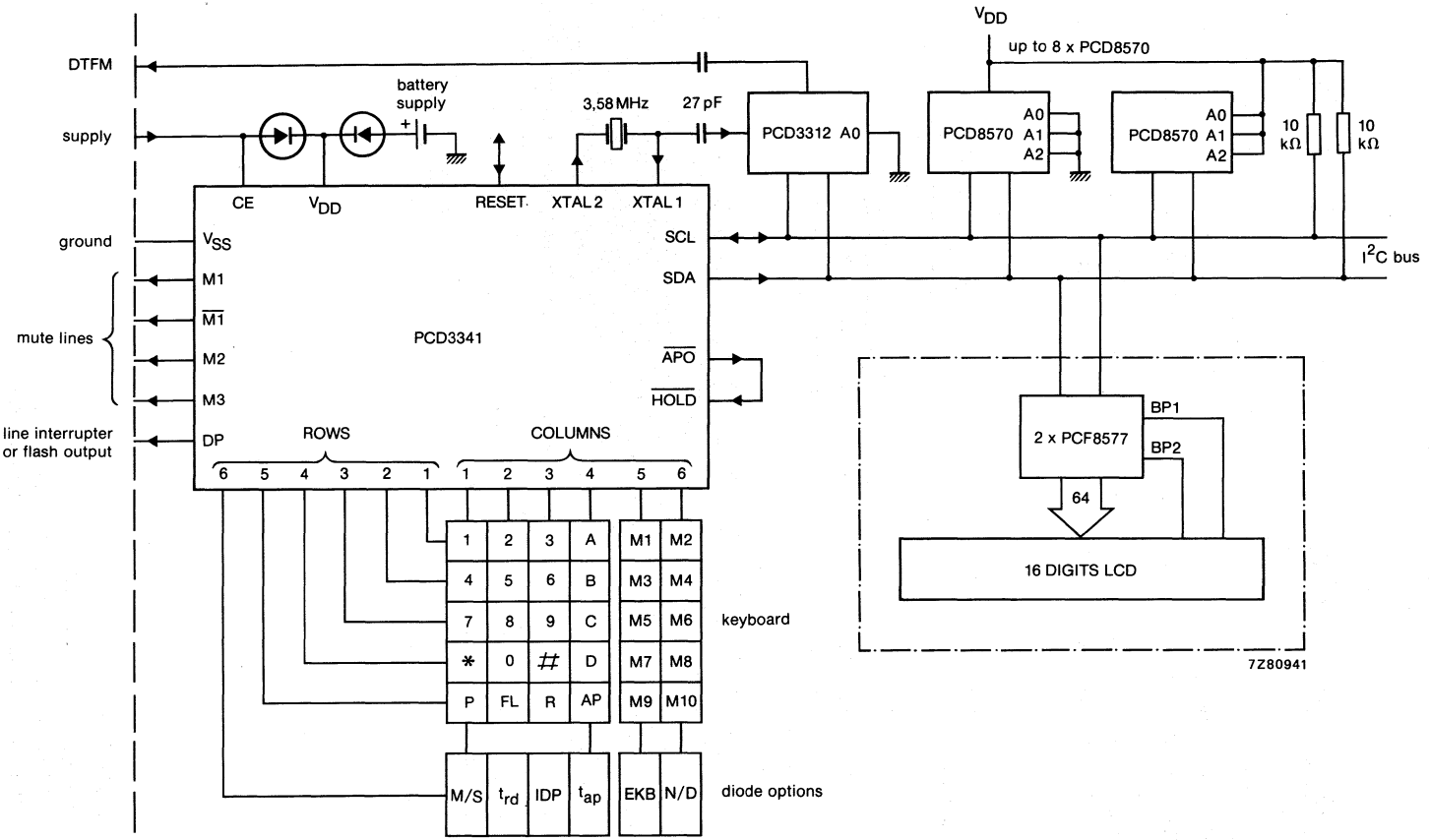


Fig. 8 PCD3341 in combination with PCD3312 (DTMF dialler), PCD8570 (2 K RAM) and PCF8577 (display drivers).

CMOS MICROCONTROLLER FOR TELEPHONE SETS

GENERAL DESCRIPTION

The PCD3343 is a single-chip 8-bit microcontroller fabricated in CMOS. It has special on-chip features ← for application in telephone sets.
The device is mask programmable, designed to provide telephone dialling facilities such as redial, repertory dial, emergency call, keyboard scan and control for liquid crystal display, pulse dial and/or DTMF dial via dedicated peripheral.

Features

- 8-bit CPU, ROM, RAM, I/O in a single 28-lead DIL or SO package
- 3 K ROM bytes
- 224 RAM bytes
- 20 quasi-bidirectional I/O port lines
- Two test inputs: one of which is also the external interrupt input (CE/$\overline{T0}$)
- Single-level vectored interrupts: external, timer/event counter, serial I/O
- Serial I/O which can be used in bus systems with more than one master (serial I/O data via an existing port line and clock via a dedicated line)
- 8-bit programmable timer/event counter
- Over 80 instructions (based on MAB8048, MAB8400 and PCF8500)
- All instructions 1 or 2 cycles
- Clock frequency 100 kHz to 10 MHz
- Single supply voltage from 1,8 V to 6 V
- Low standby voltage and current
- STOP and IDLE mode
- On-chip oscillator with output drive capability for peripherals (e.g. PCD3312 DTMF generator)
- Configuration of all I/O port lines individually selected by mask: pull-up, open drain or push-pull
- Power-on-reset circuit and low supply voltage detection
- Reset state of all ports individually selected by mask
- Operating temperature range: −25 to + 70 °C

PACKAGE OUTLINES

PCD3343P: 28-lead DIL; plastic (SOT-117).
PCD3343D: 28-lead DIL; ceramic (CERDIP) (SOT-135A).
PCD3343T: 28-lead mini-pack; plastic (SO-28; SOT-136A).

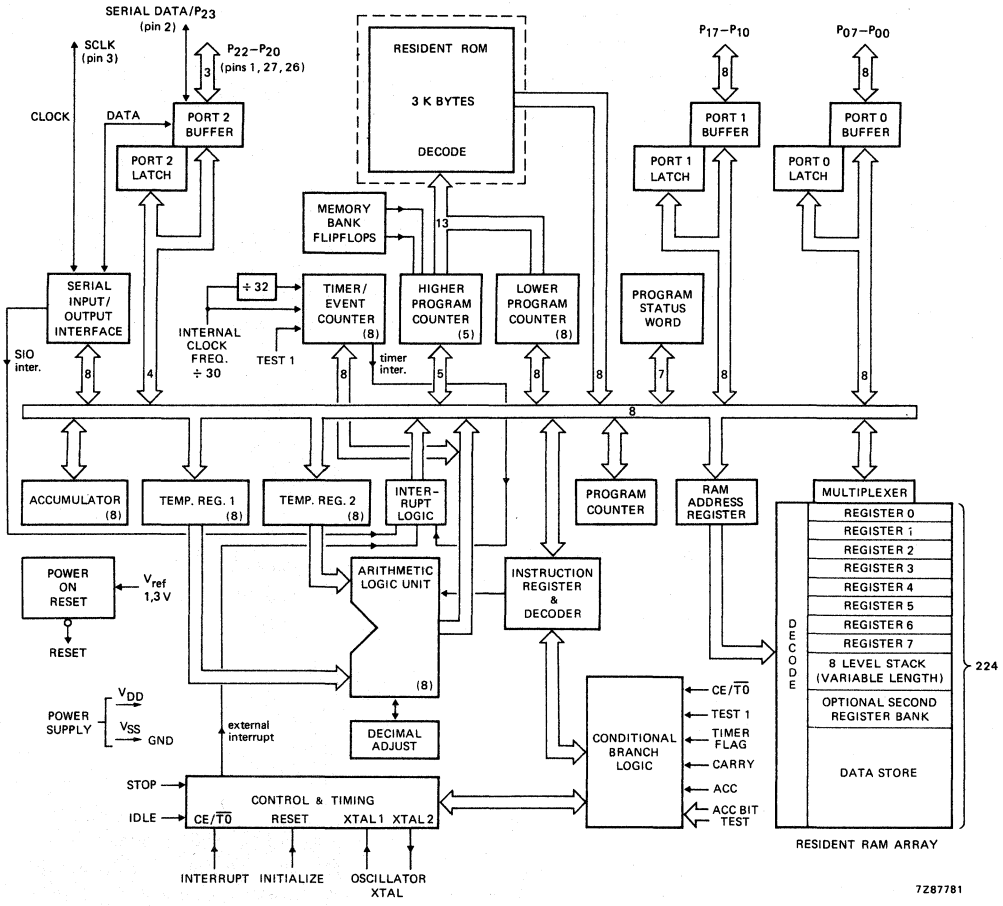
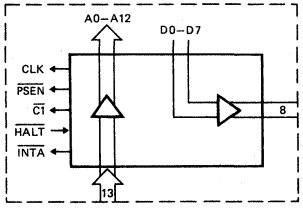
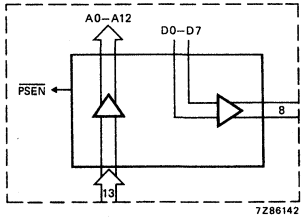


Fig. 1 Block diagram; PCD3343.



(a)

Fig. 1a Replacement of dotted part in Fig. 1, for the PCF8500F bond-out version.

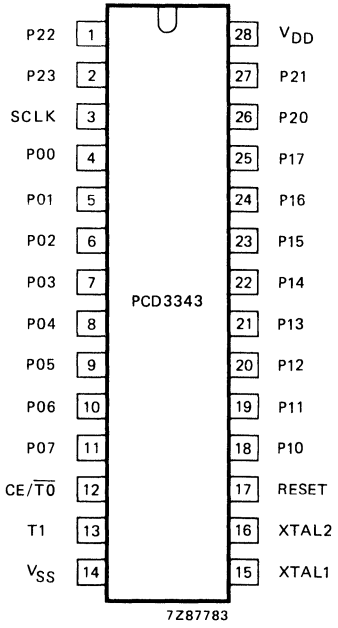


(b)

Fig. 1b Replacement of dotted part in Fig. 1, for the PCF8500B 'Piggy-back' version.

DEVELOPMENT DATA

PINNING



Note CE/$\overline{T0}$ is labelled $\overline{INT}$/T0 on the PCF8500B and has inverted polarity.

Fig. 2 Pinning diagram: PCD3343 and bottom pinning PCF8500B.

PIN DESIGNATION

3	SCLK	**Clock**: bidirectional clock for serial I/O.
4-11	P00-P07	**Port 0**: 8-bit quasi-bidirectional I/O port.
12	CE/$\overline{T0}$	**Interrupt/Test 0**: external interrupt input (sensitive to positive-going edge)/test input pin; when used as a test input directly tested by conditional branch instructions JT0 and JNT0.
13	T1	**Test 1**: test input pin, directly tested by conditional branch instructions JT1 and JNT1. T1 also functions as an input to the 8-bit timer/event counter, using the STRT CNT instruction.
14	V_{SS}	**Ground**: circuit earth potential.
15	XTAL 1	**Crystal input**: connection to timing component (crystal) which determines the frequency of the internal oscillator; also the input for an external clock source.
16	XTAL 2	connection to the other side of the timing component.
17	RESET	**Reset input**: used to initialize the processor (active HIGH), or output of power-on-reset circuit.
18-25	P10-P17	**Port 1**: 8-bit quasi-bidirectional I/O port.
26, 27, 1, 2	P20-P23	**Port 2**: 4-bit quasi-bidirectional I/O port. P23 is the serial data input/output in serial I/O mode.
28	V_{DD}	**Power supply**: 1,8 V to 6 V.

PINNING (continued)

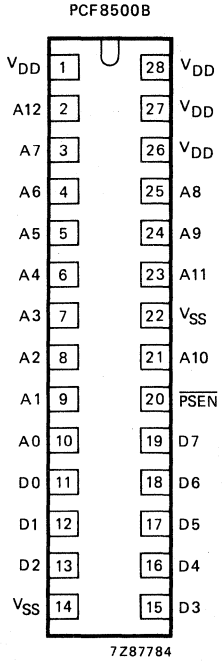


Fig. 3 Pinning diagram: PCF8500B 'Piggy-back' version top pinning; to access a 2732 or 2764 EPROM.

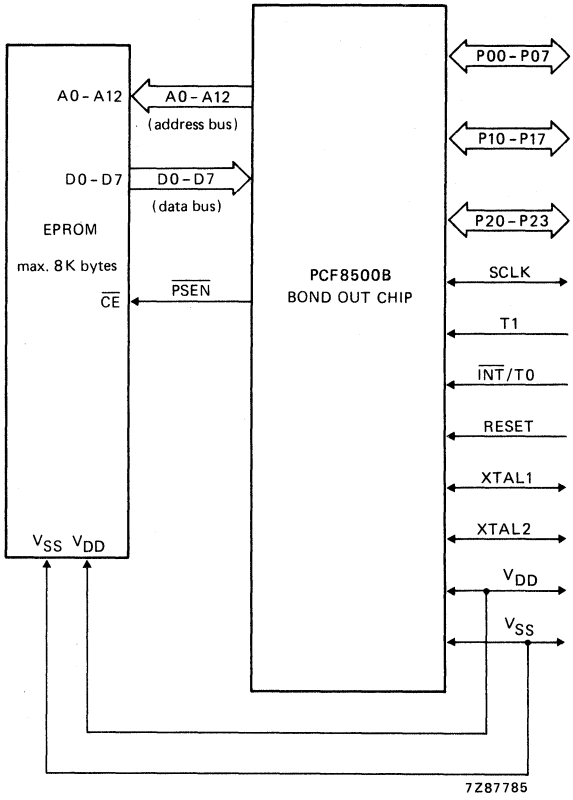


Fig. 3a Connection of EPROM to 'Piggy-back' package PCF8500B.

PIN DESIGNATION

14, 22	V_{SS}	**Ground**
1, 26-28	V_{DD}	**Power supply**
10-3, 25, 24, 21, 23, 2	A0-A12	**Address outputs**
11-13, 15-19	D0-D7	**Data**
20	$\overline{PSEN}$	**Program store enable**

Notes

1. RAM capacity of PCF8500B is 256 bytes.
2. Access time for ROMS/EPROMS to be below 7 x $1/f_{XTAL}$.
3. Pin 12 CE/$\overline{T0}$ is on the PCF8500B, inverted and labelled $\overline{INT}$/T0.

FUNCTIONAL DESCRIPTION

Bond-out version PCF8500F

The PCF8500F is a microcontroller that contains no on-board ROM, but has all address and data lines brought-out to access an external ROM or EPROM. This version has more pins than the PCD3343 with on-board ROM (see Fig. 1a). The RAM has 256 bytes. It can address 8 K bytes of ROM.

'Piggy-back' version PCF8500B

The PCF8500B is a special package that has standard pinning to the bottom which facilitates insertion as a mask-programmed device. An EPROM can be mounted on top in an additional socket. The total package height is greater than the standard DIL package. The RAM has 256 bytes and can also address 8 K bytes of program memory.

Program memory PCD3343

The program memory consists of 3072 bytes (8-bit words), in a read-only memory (ROM). Each location is directly addressable by the program counter. The memory is mask-programmed at the factory. Figure 4 shows the program memory map.

Four program memory locations are of special importance:

- Location 0; contains the first instruction to be executed after the processor is initialized (RESET),
- Location 3; contains the first byte of an external interrupt service subroutine,
- Location 5; contains the first byte of a serial I/O interrupt service subroutine,
- Location 7; contains the first byte of a timer/event counter interrupt service subroutine.

Program memory is arranged in banks of 2 K bytes, which are selected by SEL MB instructions. The program memory is further divided into location 'pages', each of 256 bytes. This latter division applies only for conditional branches. Memory bank boundaries can be crossed only by using the unconditional branch instructions after the appropriate memory bank has been selected. A CALL instruction can transfer control to a subroutine on any 'page'; RET and RETR instructions can transfer control from a subroutine back to the main program.

Data memory PCD3343

Data memory consists of 224 bytes (8-bit words), random-access data memory (RAM). All locations are indirectly addressable using RAM pointer registers; up to 16 designated locations are directly addressable. Memory also includes an 8-level program counter stack addressed by a 3-bit stack pointer. Figure 5 shows the data memory map.

Working registers

Locations 0 to 7 are designated as working registers, directly addressable by the direct register instructions. Ease of addressing, and a minimum requirement of instruction bytes to manipulate their contents, makes these locations suitable for storing frequently addressed intermediate results. This bank of registers can be selected by the SEL RB0 instruction.

Executing the select register bank instruction SEL RB1, designates locations 24 to 31 as working registers, instead of locations 0 to 7, and these are then directly addressable. This second bank of working registers may be used as an extension of the first or reserved for use during interrupt service subroutines saving the first bank for use in the main program. If the second bank is not used, locations 24 to 31 may serve as general purpose RAM.

The first locations of each bank contain the RAM pointer registers R0, R1, R0' and R1', which indirectly address all RAM locations.

All RAM locations make efficient program loop counters when used with the decrement register and test instruction DJNZ.

FUNCTIONAL DESCRIPTION (continued)

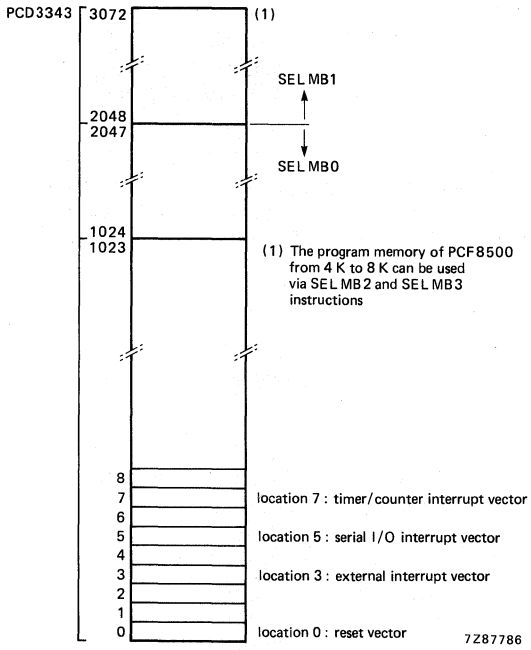


Fig. 4 Program memory map.

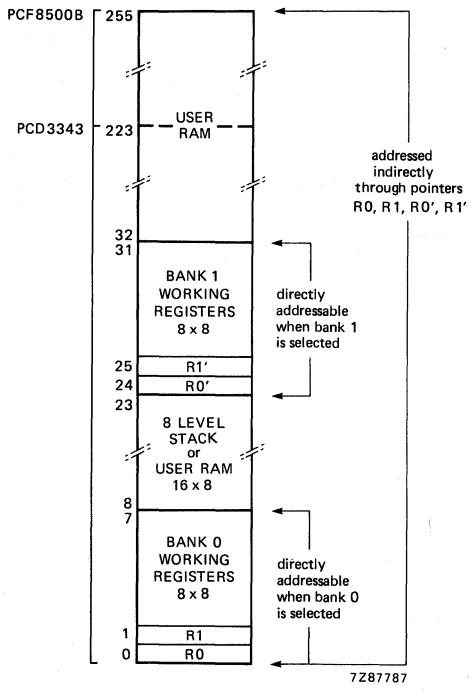


Fig. 5 Data memory map.

Program counter stack

Locations 8 to 23 may be designated as an 8-level program counter stack (2 locations per level), or as general purpose RAM. The program counter stack (Fig. 6) enables the processor to keep track of the return addresses and status generated by interrupts or CALL instructions by storing the contents of the program counter prior to servicing the subroutine. A 3-bit stack pointer determines which of the eight register pairs of the program counter stack will be loaded with next generated return address.

The stack pointer, when initialized to 000 by RESET, points to RAM locations 8 and 9. On the first subroutine CALL or interrupt, the contents of the program counter and bits 4, 6 and 7 of the program status word (PSW) are transferred to locations 8 and 9. The stack pointer increments by one and points to locations 10 and 11 ready for another CALL. Because an address may be up to 13 bits long, two bytes must be used to store each address.

At the end of a subroutine, which is signalled by a return instruction (RET or RETR), the stack pointer decrements by one and the contents of the register pair on top of the stack are transferred to the program counter. The saved PSW bits are transferred to the PSW only by the RETR instruction.

If not all 8 levels of subroutine and interrupt nesting are used, the unused portion of the stack may be used as any other indirectly addressable RAM locations. Possible locations from 32 to 223 may be used for storage of program variables or data.

Nesting of subroutines within subroutines can continue up to 8 times without overflowing the stack. If overflow does occur the deepest address stored (locations 8 and 9) will be overwritten and lost since the stack pointer overflows from 111 to 000. It also underflows from 000 to 111.

The value of the saved contents of the program counter is different for an interrupt CALL compared to a normal CALL to subroutine. With an interrupt CALL, the program counter return address is saved; with a subroutine CALL, the saved program counter value is one less than the program counter return address.

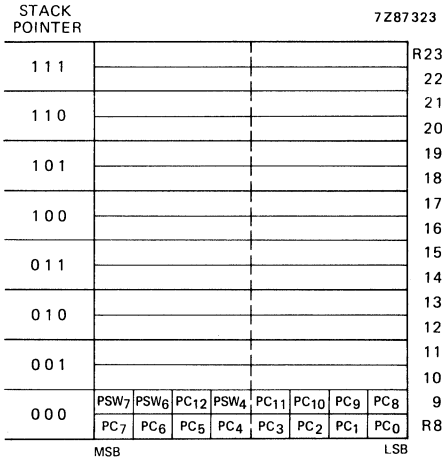


Fig. 6 Program counter stack.

IDLE and STOP modes

IDLE mode

When the microcontroller enters the IDLE mode via the IDLE instruction (H'01') the oscillator, timer/counter and serial I/O are kept running. The microcontroller exits from the IDLE mode by one of three interrupts if they are enabled or by activating a RESET. If the interrupt is not enabled the processor will remain in the IDLE mode. An active signal on the RESET pin restarts the microcontroller and a normal RESET sequence is executed (see Fig. 7).

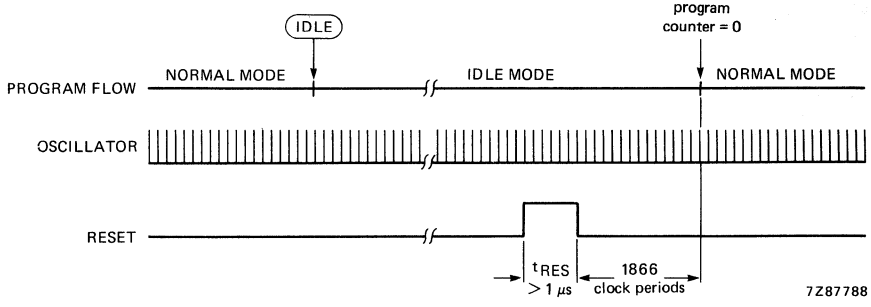


Fig. 7 Exit from IDLE mode via a RESET.

FUNCTIONAL DESCRIPTION (continued)

An active signal coming from an enabled interrupt causes the execution of the normal interrupt routine since normal interrupt scanning is still being carried out. A LOW-to-HIGH transition on the external interrupt pin (CE/$\overline{T0}$) reactivates the microcontroller. A HIGH level applied to CE/$\overline{T0}$ will reactivate the microcontroller only in the STOP mode. Thus, if CE/$\overline{T0}$ was HIGH before the microcontroller entered the IDLE mode, it must go LOW before the microcontroller can be reactivated (see Fig. 8).

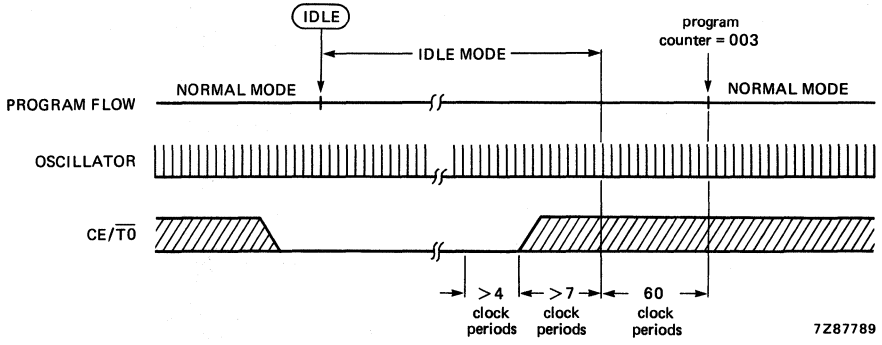


Fig. 8 Exit from IDLE mode via an interrupt.

Wake-up from the IDLE mode is ensured when CE/$\overline{T0}$ is LOW for 4 CP (clock periods) followed by a HIGH for 7 CP. After the initial forced CALL H'003' operation (60 CP) the program continues with the external interrupt service routine.

STOP mode

The microcontroller enters the STOP mode by the STOP instruction (H'22'). The oscillator is switched off. The internal status of the CPU, RAM contents and the state of I/O ports are not affected. The microcontroller can be brought-out of the STOP mode by an active signal at the external interrupt input or by an external RESET signal. When one of these two signals is applied an internal delay of 1866 CP is provided to ensure that all internal clocks are operating correctly before restart (see Fig. 9).

If the microcontroller exits from the STOP mode by activating RESET, a normal RESET sequence is executed.

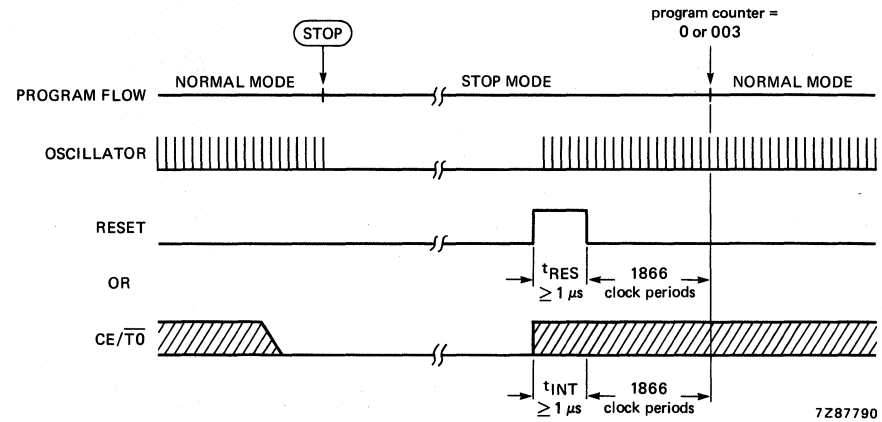


Fig. 9 Entering and exiting the STOP mode.

If the microcontroller exits the STOP mode by pulling the external interrupt input pin HIGH, an interrupt sequence is executed only if the external interrupt is enabled. In this event the microcontroller resumes the normal program sequence after returning from the interrupt routine, as in the normal mode. If the interrupt is not enabled, it continues the normal program sequence, executing the instruction following the STOP instruction.

The microcontroller is restarted by a HIGH level applied at the CE/$\overline{T0}$ pin, and not by a LOW-to-HIGH transition as in a normal interrupt mechanism.

When the CE/$\overline{T0}$ level is active during the STOP instruction then no STOP is executed.

A HIGH level on the external interrupt input of at least 1 μs will cause the microcontroller to exit the STOP mode.

I/O facilities

The PCD3343 family has 23 I/O lines arranged as:

- Port 0 parallel port of 8 lines (P00 to P07)
- Port 1 parallel port of 8 lines (P10 to P17)
- Port 2 parallel port of 4 lines (P20 to P23)
- SCLK serial I/O consisting of a data line shared with a parallel port line (P23) and a separate clock line SCLK
- CE/$\overline{T0}$ external interrupt and test input. When used as a test input can be directly tested by conditional branch instructions JT0 and JNT0
- T1 test input which can alter program sequences when tested by conditional jump instructions JT1 and JNT1. T1 also functions as an input to the 8-bit timer/event counter.

Parallel ports

All parallel ports can be used as outputs or inputs, their structure is quasi-bidirectional.
Output data written to a port is latched and remains unchanged until rewritten.
Input data is not latched and so must be present until read by an input instruction.

Input lines are fully CMOS compatible, output lines can drive one LS-TTL or CMOS load.

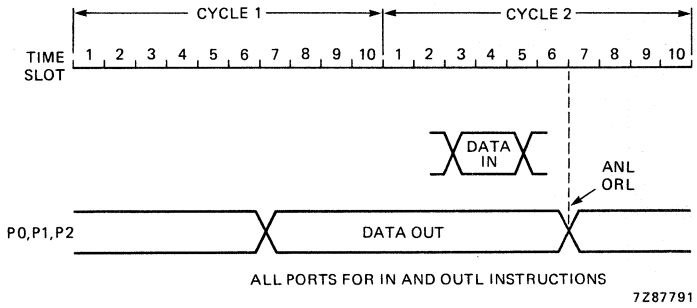


Fig. 10 Timing diagram of all ports on IN and OUTL instructions; for ANL and ORL instructions, the ports change on the time slot 7 of cycle 2.

Fig. 11 shows the quasi-bidirectional I/O interface with push-pull output and switched pull-up current source.
Each line is pulled up to V_{DD} via a constant current source (TR4), which is enabled via TR3 whenever one of the two output latches contains a logic 1. This current provides sufficient source current for a TTL HIGH level, yet can be pulled LOW by an external CMOS device, thus allowing the same pin to be used for both input and output.

FUNCTIONAL DESCRIPTION (continued)

When a logic 1 is written to the line for the first time (MQ = 1, SQ = 0), TR2 is switched on for the duration of the internal write pulse (one oscillator period), to provide a fast transition from logic 0 to logic 1. Subsequent writing of a logic 1 to the port lines will not switch TR2 on. This prevents unnecessary current through external components connected to the port lines of the same port which might be in the input mode and also connected to ground.

When a logic 0 is written to the line, TR3 switches off the current source. Current sinking capability is provided by TR1, which is now switched on. When used as an input, a logic 1 must first be written to the line, otherwise TR1 will remain low impedance.

In telephone applications this switched pull-up source may not be sufficient. Therefore the PCD3343 offers the possibility to select individually 19 of the 20 parallel port pins (not P23), by the following mask options:

Option 1- STANDARD PORT; quasi-bidirectional I/O with switched pull-up current source of 100 μA (typ.) and P-channel booster transistor TR2 (1,5 mA). TR2 is only active during 1 clock cycle (0,28 μs at 3,58 MHz).

Option 2- OPEN DRAIN; quasi-bidirectional I/O with only an N-channel open drain output. Application as an output requires connection of an external pull-up resistor (Fig. 12).

Option 3- PUSH-PULL OUTPUT; drive capability of the output will be 1,5 mA (typ.) at V_{DD} = 3 V in both polarities. To avoid a large current flowing through the output transistors during the input mode, these push-pull pins must only be used as outputs (Fig. 13).

Also, individual mask selection of the RESET state of these port pins can be achieved by appending the following options S and R to options 1, 2 or 3.

Option S-SET; after RESET this pin will be initialized to HIGH.

Option R-RESET; after RESET this pin will be initialized to LOW.

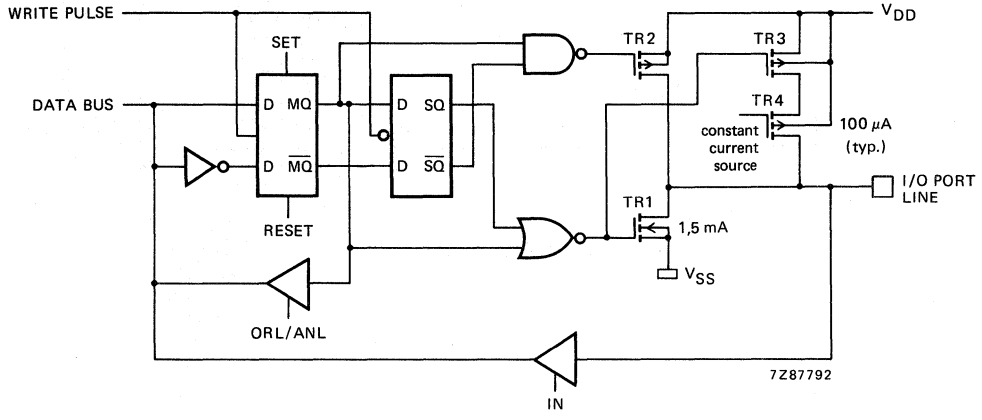


Fig. 11 Standard output with switched pull-up current source.

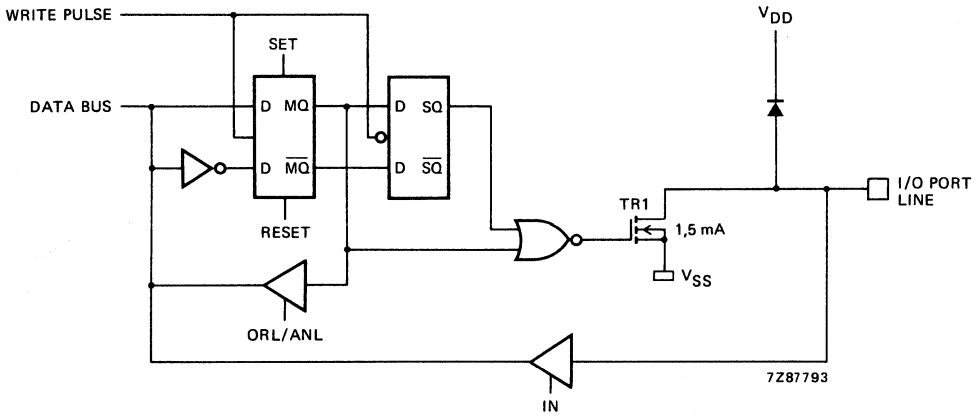


Fig. 12 Open drain output.

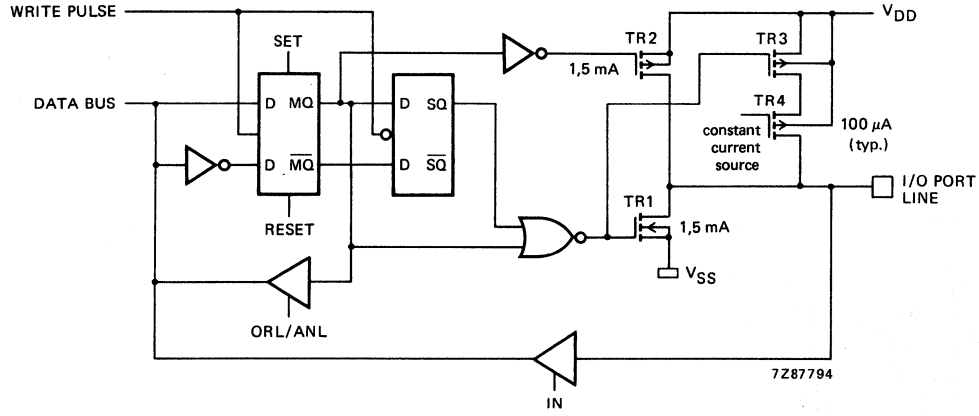


Fig. 13 Push-pull output.

FUNCTIONAL DESCRIPTION (continued)

Serial I/O (SIO)

The PCD3343 has an on-chip serial I/O interface. This SIO interface is a versatile feature in an intelligent telephone set, as shown in application diagram Fig. 32.

In this application the SIO is used to communicate with the different peripherals, such as:

- DTMF generator (PCD3312)
- LCD drivers (PCF8577)
- External RAM (PCD8571)
- Clock calendar (PCB8573)

No extra hardware is required for decoding, addressing and data processing.

Whereas a normal microcontroller must regularly monitor the serial data bus for the presence of data, the serial I/O interface detects, receives and converts the serial data stream into parallel format without interrupting the execution of the current program. An interrupt is sent to the PCD3343 only when a complete byte is received. It then reads the data byte in one instruction. Likewise during transmission the serial I/O interface performs parallel to serial conversion and subsequent serial output of the data. The microcontroller is only interrupted in the execution of its programmed tasks when a complete byte has been transmitted.

The design of the PCD3343 serial I/O system allows any number of devices from PCF8500 family (clips) to be connected via the two-line serial bus. The ability of any devices to communicate, without interrupting the operation of any other devices on the bus, is an outstanding attribute of the system. This is achieved by allocating a specific 7-bit address to each device and providing a system whereby a device reacts only to a message prefixed with its own address or the 'general CALL' address. Address recognition is performed by the interface hardware so that operation of the microcontroller need only be interrupted when a valid address has been received. This saves significant processing time and memory space compared with a conventional microcontroller employing a software serial interface. When the addressing facility is not required, for instance in a system with only two microcontrollers, direct data transfer without addressing can be performed. In multi-master systems, an automatically invoked arbitration procedure prevents two or more devices from continuing simultaneous transmission.

In NORMAL (running) and IDLE mode, the serial I/O logic remains active; its internal system clock will be switched off when there is no activity on the serial bus.

After execution of the STOP instruction, the oscillator of the PCD3343 is switched off. This means that the serial I/O logic will remain in the state it was at the occurance of the STOP instruction. To avoid "bus block" problems and to assure correct start-up of the bus after exit from the STOP mode, the user should disable the serial logic (ESO = 0) prior to the execution of the STOP instruction. This must be carried out only when the PCD3343 has finished a serial data transfer.

Serial I/O interface

Figure 14 shows the serial I/O interface. The clock line of the serial bus has exclusive use of pin 3 (SCLK) while the data line shares pin 2 (serial data) with the I/O line P23 of port 2. When the serial I/O is enabled, P23 is disabled as a parallel port line; (P23 and SCLK only open drain).

The microcontroller and interface communicate via the internal microcontroller bus and the Serial Interrupt Request line. Data and information controlling the operation of the interface are stored in four registers:

- Data shift register (S0)
- Serial I/O interface status word (S1)
- Serial clock control word (S2)
- Address register

Data shift register (S0)

Register S0 converts serial data to parallel format and vice versa. A pending interrupt is generated only after a complete byte has been transmitted, or after a complete data byte, specific address or 'general CALL' address has been received. The most significant bit is transmitted first.

Serial I/O interface status word (S1)

Register S1 provides information concerning the state of the interface and stores information from the microcontroller. Bits 0 to 3 are duplicated: control bits in these positions can only be written by the microcontroller, while interface bits can only be read.

MST and TRX (see Table 1)

These bits determine the operating mode of the serial I/O interface.

Table 1 Operating modes of the serial I/O interface

MST	TRX	operating mode
0	0	slave receiver
1	0	master receiver
0	1	slave transmitter
1	1	master transmitter

BB: Bus Busy.

This is the flag which indicates the status of the bus.

PIN: Pending Interrupt Not

PIN = '0' indicates the presence of a pending interrupt, which will cause a Serial Interrupt Request when the serial interrupt mechanism is enabled.

ESO: Enable Serial output

The ESO flag enables/disables the serial I/O interface: ESO = '1' enables, ESO = '0' disables. ESO can only be written by software.

BC0, BC1 and BC2

Bits BC0, BC1 and BC2 indicate the number of bits received or transmitted in a data stream. These bits can only be written by software.

AL: Arbitration Lost

The arbitration lost flag is set by hardware when the serial I/O interface, as master transmitter, loses a bus arbitration procedure.

AAS: Addressed As Slave

This flag is set by hardware when the interface detects either its own specific address or the 'general CALL' address as the first byte of a transfer and the interface has been programmed to operate in the address recognition mode.

AD0: Address Zero

This flag is set by hardware after detection of the 'general CALL' address when the interface is operating in the address recognition mode.

LRB: Last Received Bit

This contains either the last data bit received or, for a transmitting device in the acknowledgement mode, the acknowledgement signal from the receiving device.

Bits AL, AAS, AD0 and LRB can only be read by software.

FUNCTIONAL DESCRIPTION (continued)

Serial clock control word (S2)

Bits 0 to 4 of the clock control register S2 are used to set the frequency of the serial clock signal. When a 3,58 MHz crystal is used, the frequency of the serial clock can be varied between 92 kHz and 580 Hz (see Table 2). An asymmetrical clock with a HIGH-to-LOW ratio of 3 : 1 can be generated using bit 5. The asymmetrical clock allows a microcontroller more time per clock period for sampling the data line, making the timing of this action less critical. Bit 6 can be used to activate the acknowledge mode of the serial I/O. S2 is a write only register.

Address register

The address register contains the 7-bit address back-up latches and the bit (ALS) used to enable/disable the address recognition mode. The address register can be written using the MOV S0, A and MOV S0, # data instructions, but only when ES0 = '0'.

Serial I/O interrupt logic

An EN SI instruction enables and a DIS SI instruction disables the interrupt logic. When the logic is enabled, a pending interrupt results in a serial I/O interrupt to the processor, causing a CALL to location 5 in the ROM. When disabled, the presence of an interrupt is still indicated by PIN in S1, allowing the interrupt to be serviced. However, vectored interrupt will not occur.

DEVELOPMENT DATA

Table 2 SIO clock pulse frequency control when using a 3,58 MHz crystal

hexadecimal S20-S24 code	divisor	f_{SCLK} (kHz) (approximate)
0	not allowed	
1	39	92
2	45	80
3	51	70
4	63	57
5	75	48
6	87	41
7	99	36
8	123	29
9	147	24
A	171	21
B	195	18
C	243	15
D	291	12
E	339	11
F	387	9,2
10	483	7,4
11	579	6,2
12	675	5,3
13	771	4,6
14	963	3,7
15	1155	3,1
16	1347	2,7
17	1539	2,3
18	1923	1,9
19	2307	1,6
1A	2691	1,3
1B	3075	1,2
1C	3843	0,93
1D	4611	0,78
1E	5379	0,67
1F	6147	0,58

FUNCTIONAL DESCRIPTION (continued)

Table 3 Serial I/O addresses for telephony peripherals

type	address 7	6	5	4	3	2	1	0	description
PCF8570A	1	0	1	0	A2	A1	X	R/$\overline{W}$	2 K RAM
PCF8570	1	0	1	0	A2	A1	A0	R/$\overline{W}$	2 K RAM
PCD8571	1	0	1	0	A2	A1	A0	R/$\overline{W}$	1 K RAM
PCD3311	0	1	0	0	1	0	A0	R/$\overline{W}$	DTMF dialler
PCD3312	0	1	0	0	1	0	A0	R/$\overline{W}$	DTMF dialler
PCE2111	0	0	0	0	0	0	1	0	LCD driver *
PCD8573	1	1	0	1	0	A1	A0	R/$\overline{W}$	clock calendar
PCF8574	0	0	1	1	A2	A1	A0	R/$\overline{W}$	8-bit I/O expander
PCF8576	0	1	1	1	0	0	SA0	R/$\overline{W}$	1 : 4 LCD driver
PCF8577	0	1	1	1	0	1	0	R/$\overline{W}$	1 : 2 LCD driver

* LCD driver requires an additional enable line.

DEVELOPMENT DATA

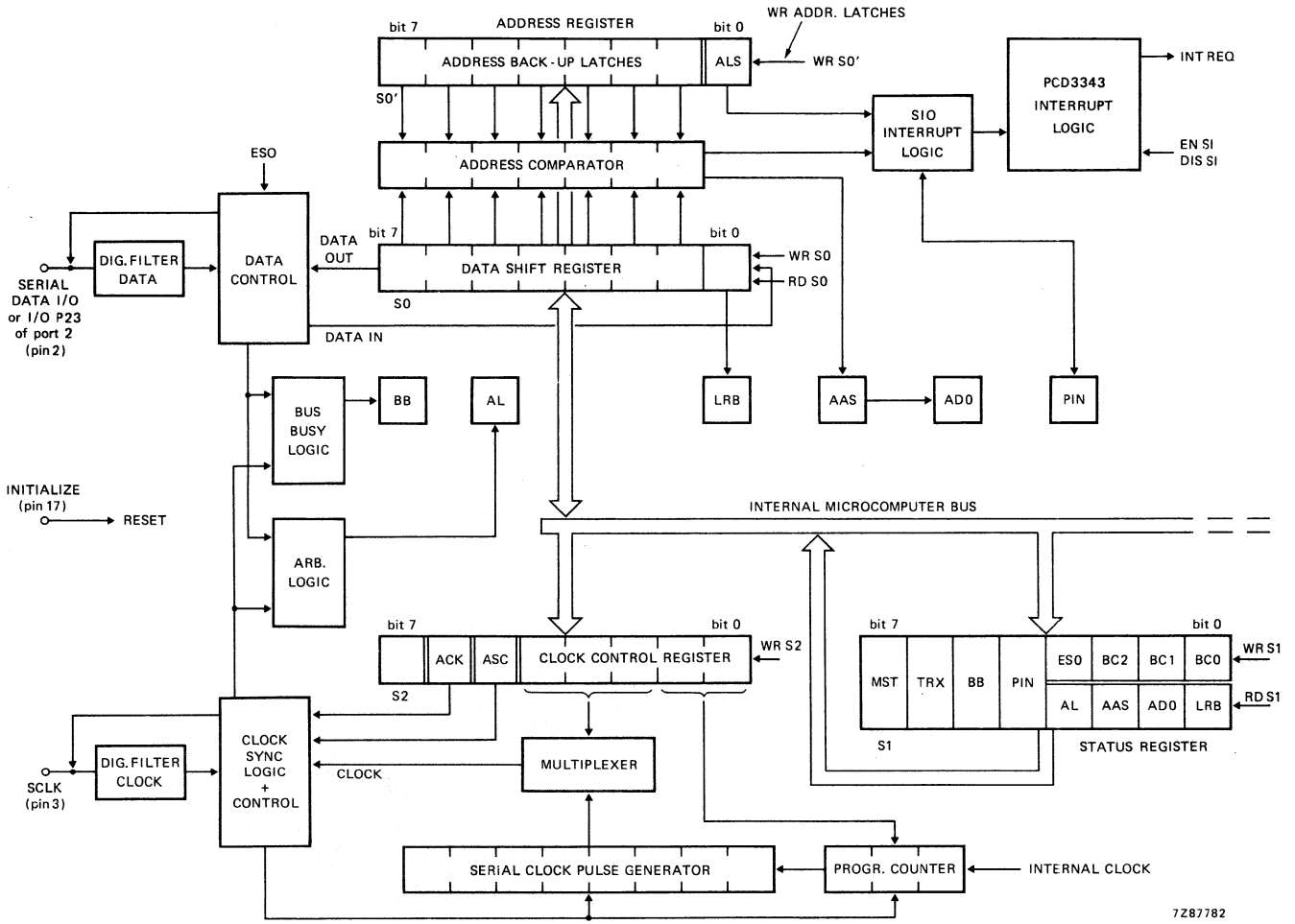


Fig. 14 Serial I/O interface.

FUNCTIONAL DESCRIPTION (continued)

Interrupts (see Fig. 15)

When the external interrupt is enabled, a LOW-to-HIGH transition on the CE/$\overline{T0}$ input initiates an external interrupt subroutine which causes a CALL to program memory location 3 following completion of the current instruction.
The interrupt must remain enabled until the interrupt instruction is completed, otherwise the next instruction of the main program will be executed. Serial I/O interrupt, when enabled, causes a CALL to location 5, and a timer/event counter overflow forces a CALL to location 7 when the timer interrupt is enabled.

When an interrupt subroutine starts, the contents of the program counter and bits 4, 6 and 7 of the PSW have been saved in the program counter stack. Accumulator contents have to be saved by software. Interrupt acknowledgement can be carried out by software via port pins. All interrupt subroutines must reside in memory bank 0.

Since the interrupt system is single level, once an interrupt is detected, all further interrupt requests are latched, but ignored, pending a RETR instruction to re-enable the interrupt input logic. After executing RETR, the program continues in the main part; this is independent of the occurance of a second interrupt during the running of the first routine. If 2 or 3 interrupts occur simultaneously, their priority is:

- (1) external
- (2) serial I/O
- (3) timer/event counter

An external interrupt can be generated by using the timer/counter in the event counter mode. The counter is first preset to (H'FF'), then EN TCNTI instruction is executed. A LOW-to-HIGH transition of the T1 input will then initiate an interrupt subroutine and cause a CALL to location 7.

On execution of a DIS I instruction, the PCD3343 always clears the digital filter/latch and the External Interrupt Flag.

The Timer Flag (TF) is reset only when the JTF or JNTF instruction is executed or after RESET.

The Timer Interrupt Flag is set when timer overflow occurs, only if the timer interrupt is enabled.

The microcontroller will exit the IDLE mode when any one of the following three interrupts is enabled:

- External
- Serial I/O
- Timer/event counter

There is no internal pull-up or pull-down device connected to the external interrupt input (pin 12). If required pin 12 must be externally connected to a resistor ($R \leqslant 100\ k\Omega$). When the external interrupt is not used pin 12 must be connected to V_{SS}.

DEVELOPMENT DATA

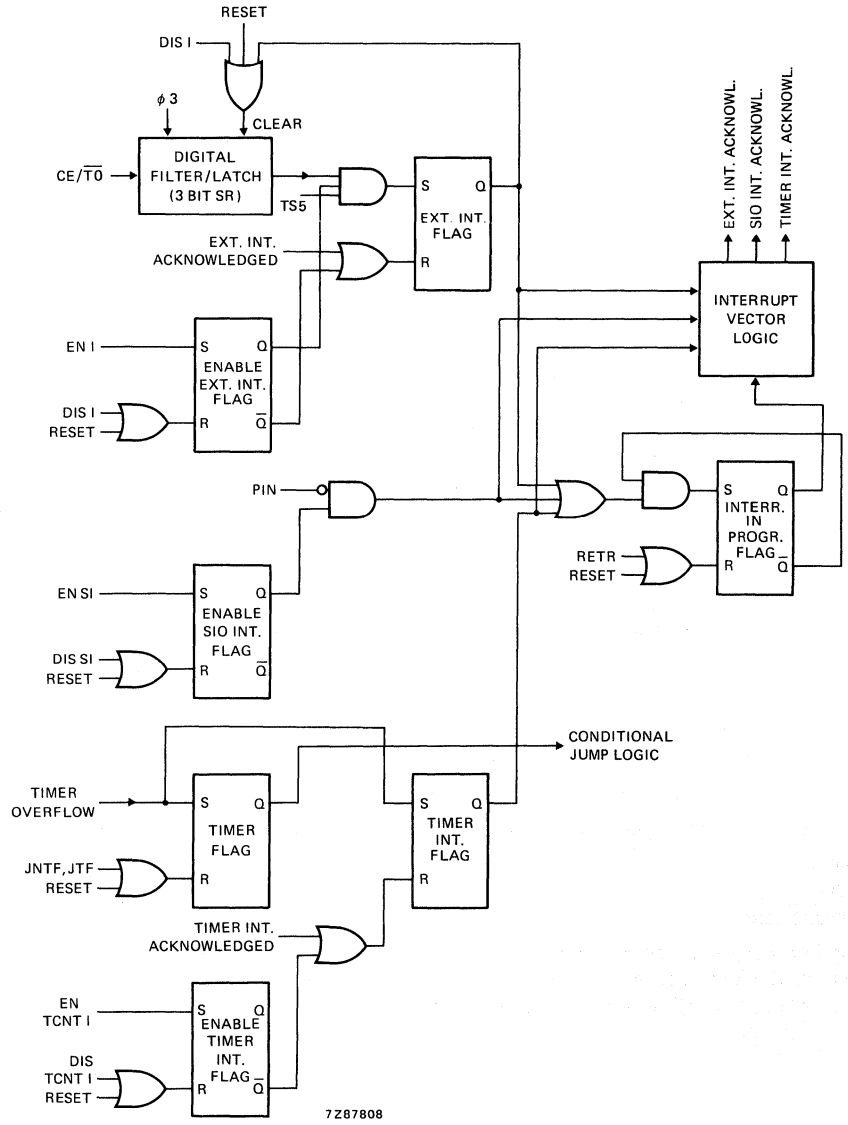


Fig. 15 Interrupt logic.

Notes to figure 15

1. CE/$\overline{T0}$ positive edge is always latched in the digital filter/latch.
2. Correct interrupt timing in ensured when CE/$\overline{T0}$ is LOW for > 4 CP followed by a HIGH for > 7 CP.
3. When the interrupt in progress flag is set, further interrupts are latched but ignored, until RETR is executed.
4. A DIS I instruction always clears a pending external interrupt.

FUNCTIONAL DESCRIPTION (continued)

Oscillator (see Fig. 16)

The 3,58 MHz oscillator can be inhibited by the STOP instruction under software control. It is also inhibited when a low-voltage condition is present to prevent discharge of a weak back-up battery.

Provided the supply voltage is within the operating range, the oscillator will be restarted after a STOP instruction by a HIGH level at either the CE/$\overline{TO}$ or RESET pin.

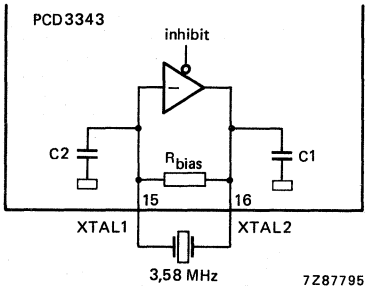


Fig. 16 Oscillator with integrated elements.

The oscillator has the output drive capability for the DTMF generator (PCD3311/3312) via pin 16 (XTAL 2). An external clock can be applied to pin 15 (XTAL 1). A machine cycle consists of 10 time slots, each time slot being 3 oscillator periods.

In telephony applications the 3,58 MHz crystal provides a 8,4 μs machine cycle. The range of the clock frequency is from 100 kHz up to a maximum which is a function of the supply voltage (see Fig. 23).

Timer/event counter (see Fig. 17)

An internal 8-bit up-counter is provided. This can count external events, modulo-32 machine cycles, or machine cycles directly. Table 4 gives the instructions that control the counter and the prescaler, and the functions performed.

When used as a timer, the input to the counter is either the overflow or input of a 5-bit prescaler. When used as an event counter, LOW-to-HIGH transitions on pin 13 (T1) are counted. The maximum rate at which the counter may be incremented is once every machine cycle (182,6 kHz for a 8,4 μs machine cycle). When the counter overflows, the timer flag is set. The flag can be tested and reset using the JTF (jump if timer flag = 1) or JNTF instruction. Overflow also generates an interrupt to the processor via setting of the Timer Interrpt Flag when the timer/event counter interrupt is enabled.

Table 4 Timer/event counter control

function	timer mode modulo-1, modulo-32*	counter mode
CLEAR	MOV T,A (A) = 0 or RESET	MOV T,A (A) = 0 or RESET
PRESET	MOV T,A	MOV T,A
START	STRT T	STRT CNT
STOP	STOP TCNT or RESET	STOP TCNT or RESET
TEST	JTF/JNTF	JTF/JNTF
READ**	MOV A,T	MOV A,T

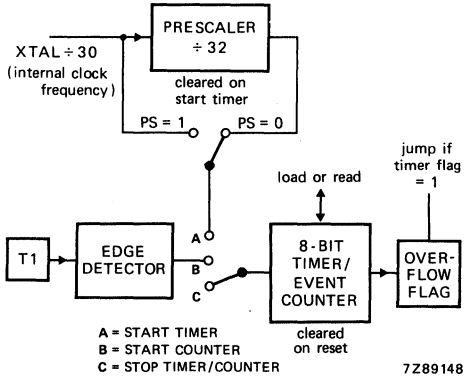


Fig. 17 Timer/event counter.

DEVELOPMENT DATA

Program status word (see Fig. 18)

The program status word (PSW) is an 8-bit word (1 byte) in the CPU which stores information about the current status of the microcontroller.
The PSW bits are:

- Bits 0 to 2 — stack pointer bits (SP_0, SP_1, SP_2)
- Bit 3 — prescaler select (PS);
  0 = modulo-32; 1 = modulo-1 (no prescaling)
- Bit 4 — working register bank select (RBS);
  0 = register bank 0; 1 = register bank 1
- Bit 5 — not used (1)
- Bit 6 — auxiliary carry (AC); half-carry bit generated by an ADD instruction and used by the decimal adjust instruction DA A
- Bit 7 — carry (CY); the carry flag indicates that previous operation has resulted in an overflow of the accumulator.

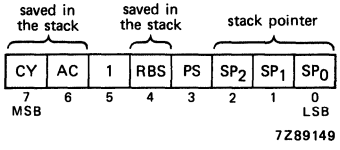


Fig. 18 Program status word.

* With prescaler select, PS = 0, the timer counts modulo-32 machine cycles, with PS = 1 it counts modulo-1 cycles (prescaler not used); prescaler cleared with STRT T, prescaler not readable.

** READ does not disturb the counting process.

FUNCTIONAL DESCRIPTION (continued)

Program status word (continued)

All bits can be read using the MOV A, PSW instruction. Bits 7 and 6 are set and cleared by CPU operation. Bit 4 can be changed by a SEL RB instruction, bit 3 by the MOV PSW, A instruction, and bits 0, 1 and 2 by the CALL, RET or RETR instructions and in the event of an interrupt. Bits 7, 6 and 4 are stored in the program counter stack during subroutine and interrupt calls. These bits are restored in the PSW with a RETR (return and restore) instruction which must be used at the end of an interrupt and can be used at the end of a normal subroutine. The RET instruction has no restore feature and cannot be used at the end of an interrupt.

Program counter (see Fig. 19)

A 13-bit program counter is used to facilitate 8 K bytes of ROM being addressed. The arrangement of the bits is shown in figure 19. During an interrupt subroutine PC_{11} and PC_{12} are forced to logic 0. All 13 bits are saved in the stack during CALL and interrupt routines.

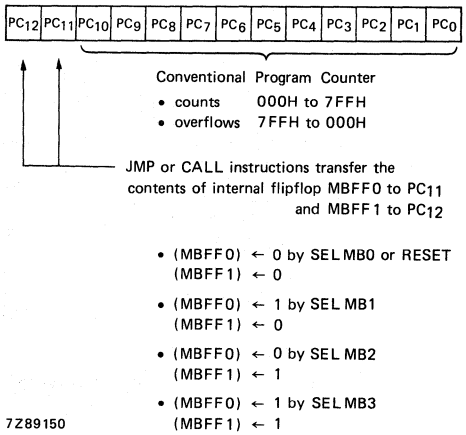


Fig. 19 Program counter.

Central processing unit

The PCD3343 has arithmetic, logical and branching capabilities. The DA A, SWAP A and XCHD instructions simplify BCD arithmetic and the handling of nibbles. The MOVP A,@A instruction permits efficient table look-up from the current ROM page.

Conditional branch logic

The conditional branch logic within the processor enables several conditions, internal and external to the processor, to be tested by the user's program. Table 5 lists the conditional jump instructions used to change the program sequence. The DJNZ instruction decrements a designated register or data memory location and branches if the contents are not zero. This instruction is useful for looping control. The JMPP@A instruction allows multiway branches to destinations determined by the contents of the accumulator.

Table 5 Conditional branches

test	jump condition	jump instruction
accumulator	all bits zero	JZ
	any bit non-zero	JNZ
accumulator bit test	1	JB0 to JB7
carry flag	1	JC
	0	JNC
timer overflow flag	1	JTF
	0	JNTF
test input T0	1	JNT0
	0	JT0*
test input T1	1	JT1
	0	JNT1
register	non-zero	DJNZ

Test input T1 (pin 13)

The T1 input line can be used as:

- A test input for branch instructions JT1 and JNT1
- An external input to the event counter

When used as a test input:

- JT1 instruction tests for logic 1 level
- JNT1 instruction tests for logic 0 level

When used as an input to the event counter, T1 must be LOW for > 4 CP, followed by a HIGH for > 4 CP. The transition can be recognized with a repetition rate of once per 30 oscillator clock periods (1 machine cycle).

There is no internal pull-up or pull-down resistor connected to the T1 input. If required it must be externally connected to a resistor ($R = \leqslant 100$ kΩ). When T1 is not used pin 13 must be connected to V_{DD} or V_{SS}.

Reset (pin 17)

A positive-going signal on the RESET input/output:

- Sets the program counter to zero
- Selects location 0 of memory band 0 and register bank 0
- Sets the stack pointer to zero (000); pointing to RAM address 8
- Disables the interrupts (external, timer and serial I/O)
- Stops the timer/event counter, then sets it to zero
- Sets the timer prescaler to modulo-32
- Resets the timer flag
- Sets all ports according to reset states
- Sets the serial I/O to slave receiver mode and disables the serial I/O
- Cancels IDLE and STOP mode

After the voltage is applied to RESET an internal delay of 1866 CP is introduced before the microcontroller commences operation.

* Because of the inverted interrupt input CE/$\overline{T0}$ the conditional jump JT0 is also inverted.

FUNCTIONAL DESCRIPTION (continued)

Power-on-reset and low-voltage detection (see Fig. 20)

In telephony applications, correct operation of the PCD3343 during moments of slowly changing supply voltages and low-voltage conditions is essential. This is achieved by the addition of an internal power-on-reset and low-voltage detection circuit.
To allow an external RESET signal being fed into the PCD3343, the reset pin (pin 17) has been configured as an input/output.

While a reset condition exists in the detection circuit, pin 17 is pulled HIGH by TR1 controlled by the reset circuit.
When the reset condition is not present a pull-down current source (TR2) will be activated. TR2 forces pin 17 LOW thus removing the RESET signal from the microcontroller.

Since the level at pin 17 is recognized by the microcontroller, the reset time constant can be stretched by connecting an external capacitor between V_{DD} and pin 17 (see Fig. 22).

The signal at pin 17 can also be used as an output to reset other devices in the system.

The internal reset circuit monitors the PCD3343 supply voltage. If the voltage drops below the switching level (typ. 1,3 V), a reset (HIGH) is applied to pin 17. This reset is removed (pin 17 goes LOW), after a fixed delay (t_d), when the supply voltage rises above the switching level again. The delay ensures a complete reset even when the supply voltage quickly rises above switching level after initial switch-on.

During a low-voltage condition the oscillator is inhibited to prevent complete discharge of a weak battery. The timing of the power-on-reset and low-voltage detection circuit is shown in figure 21.

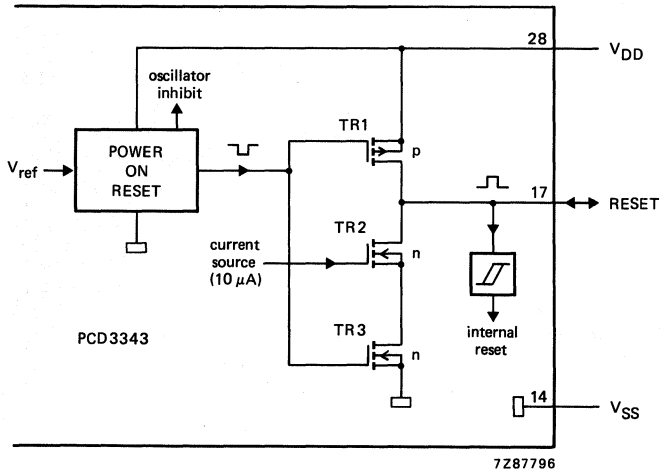
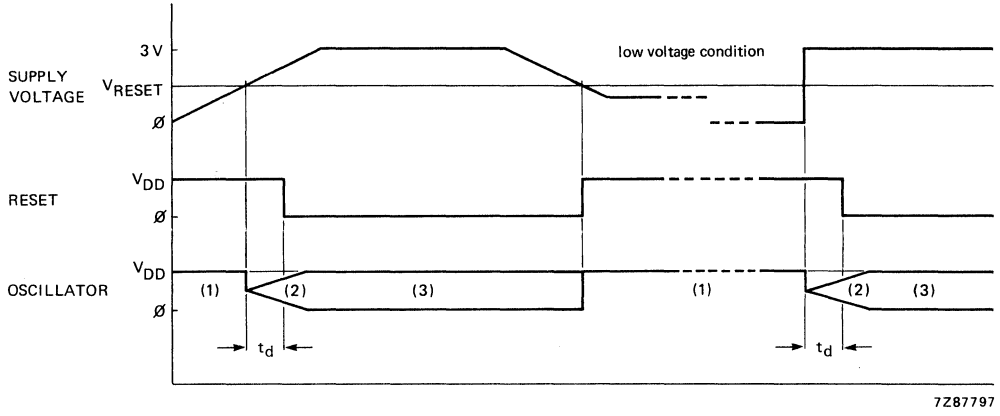


Fig. 20 Power-on-reset configuration.



Where: (1) Oscillator inhibited
(2) Oscillator starting
(3) Oscillator running, but may be stopped with a STOP condition

Fig. 21 Timing of power-on-reset and low-voltage detection.

DEVELOPMENT DATA

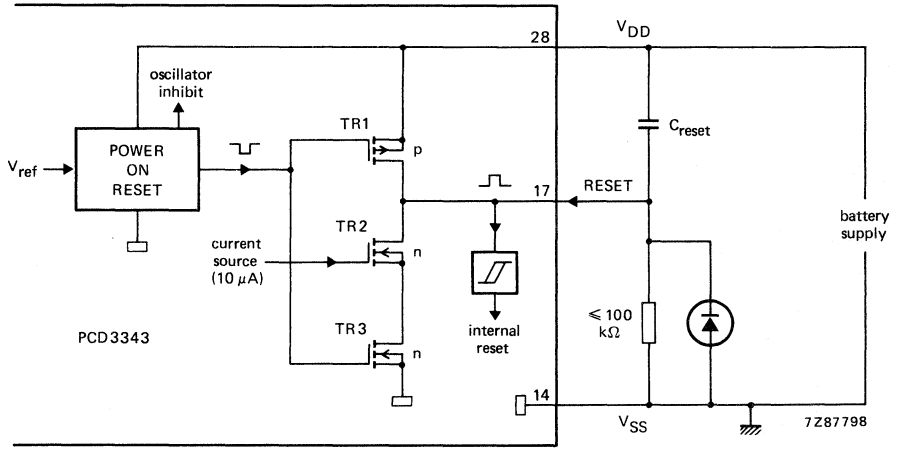


Fig. 22 Stretched power-on-reset with external capacitor.

INSTRUCTION SET

The PCD3343 instruction set consists of over 80 one and two byte instructions and is based on the MAB8048 instruction set. New instructions include those for serial I/O operation and memory bank selection. Program code efficiency is high because all RAM locations and all ROM locations on a 256 byte page require only a single byte address.

Table 8 gives the instruction set of the PCD3343. Table 7 shows the instruction map and Table 6 details the symbols and definition descriptions that are used.

Table 6 Symbols and definitions used in Table 8

symbol	definition description
A	accumulator
addr	program memory address
Bb	bit designation (b = 0-7)
RBS	register bank select
C	carry bit (bit CY)
CNT	event counter
D	mnemonic for 4-bit digit (nibble)
data	8-bit number or expression
I	interrupt
MB	memory bank
MBFF	memory bank flip-flop
P	mnemonic for 'in-page' operation
PC	program counter
Pp	port designation (p = 0, 1 or 2)
PSW	program status word
RB	register bank
Rr	register designation (r = 0-7)
Sn	serial I/O register
SP	stack pointer
T	timer
TF	timer flag
T0, T1	test 0 and 1 inputs
#	immediate data prefix
@	indirect address prefix
(X)	contents of X
((X))	contents of location addressed by X
←	is replaced by
↔	is exchanged with

Table 7 PCD3343 instruction map

first hexadecimal character of opcode

second hexadecimal character of opcode

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	NOP	IDLE		ADD A,#data	JMP page 0	EN I	JNTF addr	DEC A	IN A,Pp 0 1 2				MOV A,Sn 0 1			
1	INC @Rr 0 1		JB0 addr	ADDC A,#data	CALL page 0	DIS I	JTF addr	INC A	INC Rr 0 1 2 3 4 5 6 7							
2	XCH A,@Rr 0 1		STOP	MOV A,#data	JMP page 1	EN TCNTI	JNTO addr	CLR A	XCH A,Rr 0 1 2 3 4 5 6 7							
3	XCHD A,@Rr 0 1		JB1 addr		CALL page 1	DIS TCNTI	JTO addr	CPL A	OUTL Pp,A 0 1 2				MOV Sn,A 0 1 2			
4	ORL A,@Rr 0 1		MOV A,T	ORL A,#data	JMP page 2	STRT CNT	JNT1 addr	SWAP A	ORL A,Rr 0 1 2 3 4 5 6 7							
5	ANL A,@Rr 0 1		JB2 addr	ANL A,#data	CALL page 2	STRT T	JT1 addr	DA A	ANL A,Rr 0 1 2 3 4 5 6 7							
6	ADD A,@Rr 0 1		MOV T,A		JMP page 3	STOP TCNT		RRC A	ADD A,Rr 0 1 2 3 4 5 6 7							
7	ADDC A,@Rr 0 1		JB3 addr		CALL page 3			RR A	ADDC A,Rr 0 1 2 3 4 5 6 7							
8				RET	JMP page 4	EN SI			ORL Pp,#data 0 1 2							
9			JB4 addr	RETR	CALL page 4	DIS SI	JNZ addr	CLR C	ANL Pp,#data 0 1 2				MOV Sn,#data 0 1 2			
A	MOV @Rr,A 0 1			MOVP A,@A	JMP page 5	SEL MB2		CPL C	MOV Rr,A 0 1 2 3 4 5 6 7							
B	MOV @Rr,#data 0 1		JB5 addr	JMPP @A	CALL page 5	SEL MB3			MOV Rr,#data 0 1 2 3 4 5 6 7							
C	DEC @Rr 0 1				JMP page 6	SEL RB0	JZ addr	MOV A,PSW	DEC Rr 0 1 2 3 4 5 6 7							
D	XRL A,@Rr 0 1		JB6 addr	XRL A,#data	CALL page 6	SEL RB1		MOV PSW,A	XRL A,Rr 0 1 2 3 4 5 6 7							
E	DJNZ @Rr,addr 0 1				JMP page 7	SEL MB0	JNC addr	RL A	DJNZ Rr, addr 0 1 2 3 4 5 6 7							
F	MOV A,@Rr 0 1		JB7 addr		CALL page 7	SEL MB1	JC addr	RLC A	MOV A,Rr 0 1 2 3 4 5 6 7							

INSTRUCTION SET (continued)

Table 8 Instruction set

	mnemonic	opcode (hex.)	bytes/ cycles	description	function		notes
ACCUMULATOR	ADD A, Rr	6*	1/1	Add register contents to A	(A)←(A) + (Rr)	r = 0–7	1
	ADD A, @Rr	60 61	1/1	Add RAM data, addressed by Rr, to A	(A)←(A) + ((R0)) (A)←(A) + ((R1))		1
	ADD A, #data	03 data	2/2	Add immediate data to A	(A)←(A) + data		1
	ADDC A, Rr	7*	1/1	Add carry and register contents to A	(A)←(A) + (Rr) + (C)	r = 0–7	1
	ADDC A, @Rr	70 71	1/1	Add carry and RAM data, addressed by Rr, to A	(A)←(A) + ((R0)) + (C) (A)←(A) + ((R1)) + (C)		1
	ADDC A, #data	13 data	2/2	Add carry and immediate data to A	(A)←(A) + data + (C)		1
	ANL A, Rr	5*	1/1	'AND' Rr with A	(A)←(A) AND (Rr)	r = 0–7	
	ANL A, @Rr	50 51	1/1	'AND' RAM data, addressed by Rr, with A	(A)←(A) AND ((R0)) (A)←(A) AND ((R1))		
	ANL A, #data	53 data	2/2	'AND' immediate data with A	(A)←(A) AND data		
	ORL A, Rr	4*	1/1	'OR' Rr with A	(A)←(A) OR (Rr)	r = 0–7	
	ORL A, @Rr	40 41	1/1	'OR' RAM data, addressed by Rr, with A	(A)←(A) OR ((R0)) (A)←(A) OR ((R1))		
	ORL A, #data	43 data	2/2	'OR' immediate data with A	(A)←(A) OR data		
	XRL A, Rr	D*	1/1	'XOR' Rr with A	(A)←(A) XOR (Rr)	r = 0–7	
	XRL A, @Rr	D0 D1	1/1	'XOR' RAM, addressed by Rr, with A	(A)←(A) XOR ((R0)) (A)←(A) XOR ((R1))		
	XRL A, #data	D3 data	2/2	'XOR' immediate data with A	(A)←(A) XOR data		
	INC A	17	1/1	increment A by 1	(A)←(A) + 1		
	DEC A	07	1/1	decrement A by 1	(A)←(A) −1		
	CLR A	27	1/1	clear A to zero	(A)←0		
	CPL A	37	1/1	one's complement A	(A)←NOT(A)		
	RL A	E7	1/1	rotate A left	$(A_{n+1})\leftarrow(A_n)$ $(A_0)\leftarrow(A_7)$	n = 0–6	

ACCUMULATOR (cont.)	RLC A	F7	1/1	rotate A left through carry	$(A_{n+1})\leftarrow A_n$ $(A_0)\leftarrow(C)$, $(C)\leftarrow(A_7)$	n = 0–6	2
	RR A	77	1/1	rotate A right	$(A_n)\leftarrow(A_{n+1})$ $(A_7)\leftarrow(A_0)$	n = 0–6	
	RRC A	67	1/1	rotate A right through carry	$(A_n)\leftarrow(A_{n+1})$ $(A_7)\leftarrow(C)$, $(C)\leftarrow(A_0)$	n = 0–6	2
	DA A	57	1/1	decimal adjust A			2
	SWAP A	47	1/1	swap nibbles of A	$(A_{4-7})\leftrightarrow(A_{0-3})$		
DATA MOVES	MOV A, Rr	F*	1/1	move register contents to A	(A)←(Rr)	r = 0–7	
	MOV A, @Rr	F0 F1	1/1	move RAM data, addressed by Rr, to A	(A)←((R0)) (A)←((R1))		
	MOV A, #data	23 data	2/2	move immediate data to A	(A)←data		
	MOV Rr, A	A*	1/1	move accumulator contents to register	(Rr)←(A)	r = 0–7	
	MOV @Rr, A	A0 A1	1/1	move accumulator contents to RAM location addressed by Rr	((R0))←(A) ((R1))←(A)		
	MOV Rr, #data	B* data	2/2	move immediate data to Rr	(Rr)←data		
	MOV @Rr, #data	B0 data B1 data	2/2	move immediate data to RAM location addressed by Rr	((R0))←data ((R1))←data		
	XCH A, Rr	2*	1/1	exchange accumulator contents with Rr	(A)↔(Rr)	r = 0–7	
	XCH A, @Rr	20 21	1/1	exchange accumulator contents with RAM data addressed by Rr	(A)↔((R0)) (A)↔((R1))		
	XCHD A, @Rr	30 31	1/1	exchange lower nibbles of A and RAM data addressed by Rr	$(A_{0-3})\leftrightarrow((R0_{0-3}))$ $(A_{0-3})\leftrightarrow((R1_{0-3}))$		
	MOV A, PSW	C7	1/1	move PSW contents to accumulator	(A)←(PSW)		
	MOV PSW, A	D7	1/1	move accumulator bit 3 to PSW_3	$(PSW_3)\leftarrow(A_3)$		3
	MOVP A, @A	A3	1/2	move indirectly addressed data in current page to A	$(PC_{0-7})\leftarrow(A)$, $(A)\leftarrow((PC))$		
FLAGS	CLR C	97	1/1	clear carry bit	(C)←0		2
	CPL C	A7	1/1	complement carry bit	(C)←NOT(C)		2

	mnemonic	opcode (hex.)	bytes/ cycles	description	function	notes
REGISTER	INC Rr	1*	1/1	increment register by 1	(Rr)←(Rr) + 1 r = 0–7	
	INC @Rr	10 11	1/1	increment RAM data, addressed by Rr, by 1	((R0))←((R0)) + 1 ((R1))←((R1)) + 1	
	DEC Rr	C*	1/1	decrement register by 1	(Rr)←(Rr) – 1 r = 0–7	
	DEC @Rr	C0 C1	1/1	decrement RAM data, addressed by Rr, by 1	((R0))←((R0)) – 1 ((R1))←((R1)) – 1	
BRANCH	JMP addr	● 4 address	2/2	unconditional jump within a 2 K bank	(PC_{8-10})←$addr_{8-10}$ (PC_{0-7})←$addr_{0-7}$ (PC_{11-12})←MBFF 0–1	
	JMPP @A	B3	1/2	indirect jump within a page	(PC_{0-7})←((A))	
	DJNZ Rr, addr	E* address	2/2	decrement Rr by 1 and jump if not zero to addr	(Rr)←(Rr) – 1 r = 0–7 if (Rr) not zero (PC_{0-7})←addr	
	DJNZ @Rr, addr	E0	2/2	decrement RAM data, addressed by Rr by 1 and jump if not zero to addr	((R0))←((R0)) – 1 if ((R0)) not zero (PC_{0-7})←addr	
		E1			((R1))←((R1)) – 1 if ((R1)) not zero (PC_{0-7})←addr	
	JBb addr	▲ 2 address	2/2	jump to addr if Acc. bit b = 1	if b = 1 : (PC_{0-7})←addr b = 0–7	
	JC addr	F6 address	2/2	jump to addr if C = 1	if C = 1 : (PC_{0-7})←addr	
	JNC addr	E6 address	2/2	jump to addr if C = 0	if C = 0 : (PC_{0-7})←addr	
	JZ addr	C6 address	2/2	jump to addr if A = 0	if A = 0 : (PC_{0-7})←addr	
	JNZ addr	96 address	2/2	jump to addr if A is NOT zero	if A≠0 : (PC_{0-7})←addr	
	JT0 addr	36 address	2/2	jump to addr if T0 = 0	if T0 = 0: (PC_{0-7})←addr	
	JNT0 addr	26 address	2/2	jump to addr if T0 = 1	if T0 = 1: (PC_{0-7})←addr	
	JT1 addr	56 address	2/2	jump to addr if T1 = 1	if T1 = 1: (PC_{0-7})←addr	
	JNT1 addr	46 address	2/2	jump to addr if T1 = 0	if T1 = 0: (PC_{0-7})←addr	
	JTF addr	16 address	2/2	jump to addr if Timer Flag = 1	if TF = 1: (PC_{0-7})←addr	4
	JNTF addr	06 address	2/2	jump to addr if Timer Flag = 0	if TF = 0: (PC_{0-7})←addr	

TIMER/EVENT COUNTER	MOV A, T	42	1/1	move timer/event counter contents to accumulator	(A)←(T)	
	MOV T, A	62	1/1	move accumulator contents to timer/event counter	(T)←(A)	
	STRT CNT	45	1/1	start event counter		
	STRT T	55	1/1	start timer		
	STOP TCNT	65	1/1	stop timer/event counter		
	EN TCNTI	25	1/1	enable timer/event counter interrupt		
	DIS TCNTI	35	1/1	disable timer/event counter interrupt		
CONTROL	EN I	05	1/1	enable external interrupt		
	DIS I	15	1/1	disable external interrupt		
	SEL RB0	C5	1/1	select register bank 0	(RBS)←0	5
	SEL RB1	D5	1/1	select register bank 1	(RBS)←1	5
	SEL MB0	E5	1/1	select program memory bank 0	(MBFF0)←0, (MBFF1)←0	
	SEL MB1	F5	1/1	select program memory bank 1	(MBFF0)←1, (MBFF1)←0	
	SEL MB2	A5	1/1	select program memory bank 2	(MBFF0)←0, (MBFF1)←1	
	SEL MB3	B5	1/1	select program memory bank 3	(MBFF0)←1, (MBFF1)←1	
	STOP	22	1/1	enter STOP mode		
	IDLE	01	1/1	enter IDLE mode		
SUBROUTINE	CALL addr	▲ 4 address	2/2	jump to subroutine	((SP))←(PC), ($PSW_{4, 6, 7}$) 6 (SP)←(SP) + 1 (PC_{8-10})←$addr_{8-10}$ (PC_{0-7})←$addr_{0-7}$ (PC_{11-12})←MBFF 0–1	6
	RET	83	1/2	return from subroutine	(SP)←(SP) – 1 (PC)←((SP))	6
	RETR	93	1/2	return from interrupt and restore bits 4, 6, 7 of PSW	(SP)←(SP) – 1 ($PSW_{4, 6, 7}$) + (PC)←((SP))	6

	mnemonic	opcode (hex.)	bytes/ cycles	description	function	notes
PARALLEL INPUT/OUTPUT	IN A, Pp	08 09 0A	1/2	input port p data to accumulator	(A)←(P0) (A)←(P1) (A)←(P2)	 7
	OUTL Pp, A	38 39 3A	1/2	output accumulator data to port p	(P0)←(A) (P1)←(A) (P2)←(A)	
	ANL Pp, #data	98 99 9A	2/2	AND port p data with immediate data	(P0)←(P0) AND data (P1)←(P1) AND data (P2)←(P2) AND data	
	ORL Pp, #data	88 89 8A	2/2	OR port p data with immediate data	(P0)←(P0) OR data (P1)←(P1) OR data (P2)←(P2) OR data	
SERIAL INPUT/OUTPUT	MOV A, S_n	0C 0D	1/2	move serial I/O register contents to accumulator	(A)←(S0) (A)←(S1)	 8
	MOV S_n, A	3C 3D 3E	1/2	move accumulator contents to serial I/O register	(S0)←(A) (S1)←(A) (S2)←(A)	 9
	MOV S_n, #data	9C 9D 9E	2/2	move immediate data to serial I/O register	(S0)←data (S1)←data (S2)←data	
	EN SI	85	1/1	enable serial I/O interrupt		
	DIS SI	95	1/1	disable serial I/O interrupt		
	NOP	00	1/1	no operation		

Notes to Table 8

1. PSW CY, AC affected
2. PSW CY affected
3. PSW PS affected
4. Execution of JTF and JNTF instructions resets the Timer Flag (TF).

* : 8, 9, A, B, C, D, E, F
● : 0, 2, 4, 6, 8, A, C, E
▲ : 1, 3, 5, 7, 9, B, D, F

5. PSW RBS affected
6. PSW SP_0, SP_1, SP_2 affected
7. (A) = 1111 P23, P22, P21, P20.
8. (S1) has a different meaning for read and write operation, see serial I/O interface.
9. (S2) is a write only register. Reading S2 will give value FFH.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 28)	V_{DD}		−0,8 to + 8	V
All input voltages	V_I		0,8 to V_{DD} + 0,8	V
D.C. current into any input or output	$\pm I_I, \pm I_O$	max.	10	mA
Total power dissipation (see note)	P_{tot}	max.	500	mW
Power dissipation per output				
except P23, SCLK	P_O	max.	50	mW
P23, SCLK	P_O	max.	180	mW
Storage temperature range	T_{stg}		−65 to + 150	°C
Operating ambient temperature range	T_{amb}		−25 to + 70	°C
Operating junction temperature	T_j	max.	125	°C

Note

Thermal resistance (junction to ambient)				
for SOT-117	$R_{th\ j\text{-}a}$	max.	120	K/W
for SOT-135A	$R_{th\ j\text{-}a}$	max.	60	K/W
for SOT-136A	$R_{th\ j\text{-}a}$	max.	150	K/W

DEVELOPMENT DATA

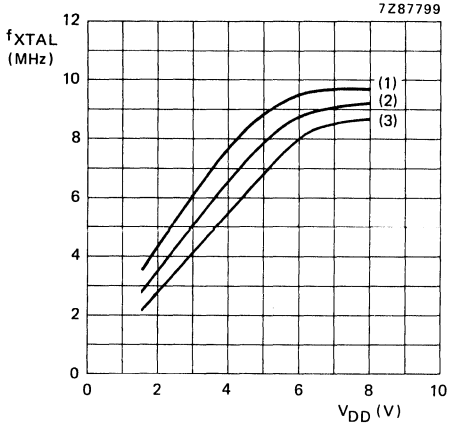
D.C. CHARACTERISTICS

V_{DD} = 2,75 to 6 V; V_{SS} = 0 V; T_{amb} = −25 to + 70 °C; all voltages with respect to V_{SS}; f = 3,58 MHz with R_S = 50 Ω; unless otherwise specified.

parameter	symbol	min.	typ.	max.	unit
Supply voltage					
operating (see Fig. 23)	V_{DD}	1,8	–	6	V
STOP mode for RAM retention	V_{DD}	1,0	–	6	V
Supply current					
operating					
at V_{DD} = 3 V (see Fig. 24)	I_{DD}	–	600	–	μA
IDLE mode					
at V_{DD} = 3 V (see Fig. 25)	I_{DD}	–	300	–	μA
STOP mode (see Fig. 26 and note 1)					
at V_{DD} = 1,8 V; T_{amb} = 25 °C	I_{DD}	–	1,2	2,5	μA
at V_{DD} = 1,8 V; T_{amb} = 55 °C	I_{DD}	–	–	5	μA
at V_{DD} = 1,8 V; T_{amb} = 70 °C	I_{DD}	–	–	10	μA
RESET I/O					
Switching level	V_{RESET}	–	1,3	–	V
Sink current					
at $V_{DD} > V_{RESET}$	I_{OL}	–	7	–	μA
Inputs					
Input voltage LOW	V_{IL}	0	–	$0{,}3V_{DD}$	V
Input voltage HIGH	V_{IH}	$0{,}7V_{DD}$	–	V_{DD}	V
Input leakage current					
at $V_{SS} < V_I < V_{DD}$	$\pm I_{IL}$	–	–	1	μA
Outputs					
Output voltage LOW					
at $V_I = V_{SS}$ or V_{DD}; $\lvert I_O \rvert < 1$ μA	V_{OL}	–	–	0,05	V
Output sink current LOW					
at V_{DD} = 3 V; V_O = 0,4 V					
except P23/SDA, SCLK (see Fig. 27)	I_{OL}	0,75	1,5	–	mA
P23/SDA, SCLK (see Fig. 28)	I_{OL}	1,5	–	–	mA
Pull-up output source current HIGH (see Fig. 29)					
at V_{DD} = 3 V; $V_O = 0{,}9V_{DD}$	$-I_{OH}$	25	–	–	μA
at V_{DD} = 3 V; $V_O = V_{SS}$	$-I_{OH}$	–	–	200	μA
Push-pull output source current HIGH					
at V_{DD} = 3 V; $V_O = V_{DD}$−0,4 V	$-I_{OH}$	0,75	1,5	–	mA

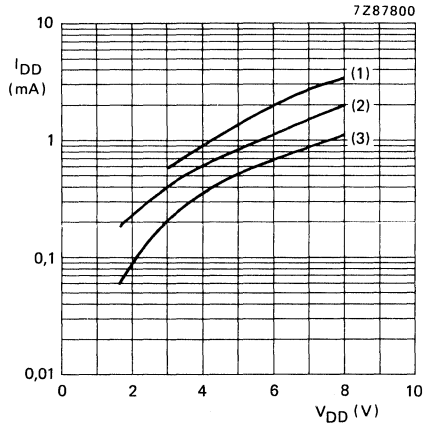
Note 1

Crystal connected between XTAL 1 and XTAL 2; SCL and SDA pulled to V_{DD} via 5,6 kΩ resistor; CE and T1 at V_{SS}.



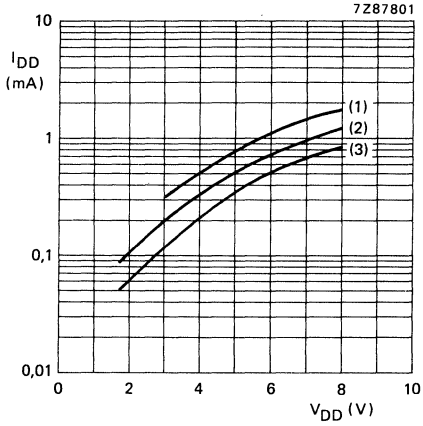
(1) $T_{amb} = -25$ °C
(2) $T_{amb} = 25$ °C
(3) $T_{amb} = 70$ °C

Fig. 23 Maximum clock frequency (f_{XTAL}) as a function of the supply voltage (V_{DD}).



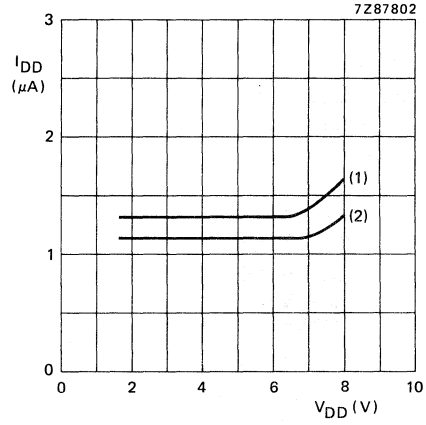
(1) clock frequency = 4 MHz
(2) clock frequency = 2 MHz
(3) clock frequency = 500 kHz

Fig. 24 Typical supply current (I_{DD}) in operating mode as a function of the supply voltage (V_{DD}); $T_{amb} = 25$ °C.



(1) clock frequency = 4 MHz
(2) clock frequency = 2 MHz
(3) clock frequency = 500 kHz

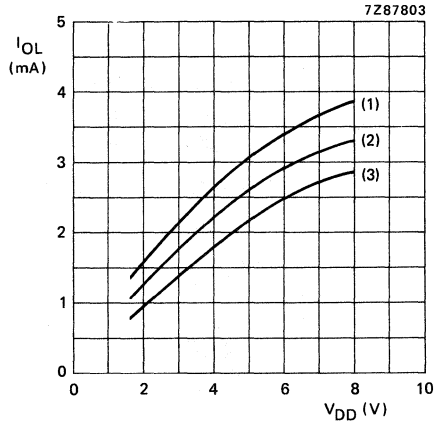
Fig. 25 Typical supply current (I_{DD}) in IDLE mode as a function of the supply voltage (V_{DD}); $T_{amb} = 25$ °C.



(1) $T_{amb} = 70$ °C
(2) $T_{amb} = 25$ °C

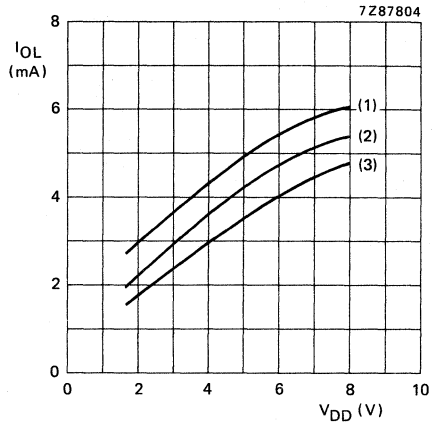
Fig. 26 Typical supply current (I_{DD}) in STOP mode as a function of the supply voltage (V_{DD}).

DEVELOPMENT DATA



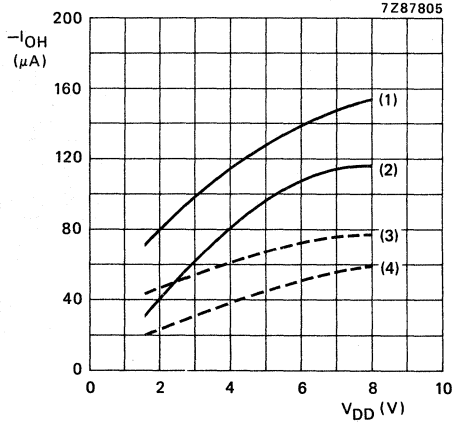
(1) $T_{amb} = -25\ ^{o}C$
(2) $T_{amb} = 25\ ^{o}C$
(3) $T_{amb} = 70\ ^{o}C$

Fig. 27 Output sink current LOW (I_{OL}), except outputs P23/SDA and SCLK, as a function of supply voltage (V_{DD}); $V_O = 0{,}4$ V.



(1) $T_{amb} = -25\ ^{o}C$
(2) $T_{amb} = +25\ ^{o}C$
(3) $T_{amb} = +70\ ^{o}C$

Fig. 28 Output current LOW (I_{OL}), outputs P23/SDA and SCLK, as a function of supply voltage (V_{DD}); $V_O = 0{,}4$ V.



(1) $T_{amb} = 25\ ^{o}C$; $V_O = V_{SS}$
(2) $T_{amb} = 25\ ^{o}C$; $V_O = 0{,}9V_{DD}$
(3) $T_{amb} = 70\ ^{o}C$; $V_O = V_{SS}$
(4) $T_{amb} = 70\ ^{o}C$; $V_O = 0{,}9V_{DD}$

Fig. 29 Output source current HIGH ($-I_{OH}$) as a function of supply voltage (V_{DD}).

A.C. CHARACTERISTICS

Rise and fall times between 10 and 90% levels; C_L = 50 pF

parameter	symbol	at 70 °C max. value			unit
	V_{DD}	1,8	3,0	6,0	V
Fall time	t_f	200	100	70	ns
Rise time	t_r	200	100	80	ns

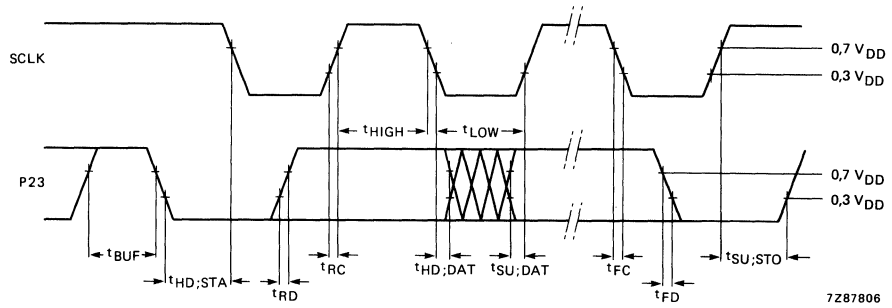


Fig. 30 PCD3343 timing requirements for the P23 and SCLK *input* signals.

Table 9 Input timing shown in figure 30

symbol	timing
t_{BUF}	$\geqslant 14t_{XTAL}$
$t_{HD;STA}$	$\geqslant 14t_{XTAL}$
t_{HIGH}	$\geqslant 17t_{XTAL}$
t_{LOW}	$\geqslant 17t_{XTAL}$
$t_{SY;STO}$	$\geqslant 14t_{XTAL}$
$t_{HD;DAT}$	> 0
$t_{SU;DAT}$	$\geqslant 250$ ns
t_{RD}	$\leqslant 1\ \mu s$
t_{RC}	$\leqslant 1\ \mu s$
t_{FD}	$\leqslant 1\ \mu s$
t_{FC}	$\leqslant 0{,}3\ \mu s$

Notes to Table 9

t_{XTAL} = one period of the XTAL input frequency (f_{XTAL})
= 280 ns for f_{XTAL} = 3,58 MHz.
These figures apply to all modes.

DEVELOPMENT DATA

A.C. CHARACTERISTICS (continued)

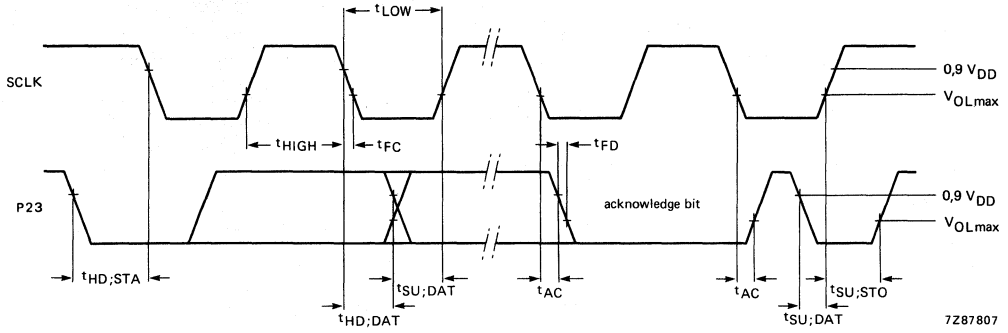


Fig. 31 PCD3343 timing requirements for the P23 and SCLK *output* signals.

Table 10 Output timing shown in figure 31

symbol	timing	
	normal mode (ASC in S2 = 0)	low-speed mode (ASC in S2 = 1)
$t_{HD;STA}$	½ (DF + 9) t_{XTAL}	¾ (DF + 9) t_{XTAL}
t_{HIGH}	½ (DF) t_{XTAL}	¾ (DF) t_{XTAL}
t_{LOW}	½ (DF) t_{XTAL}	¼ (DF) t_{XTAL}
$t_{SU;STO}$	½ (DF − 3) t_{XTAL}	¼ (DF − 3) t_{XTAL}
$t_{HD;DAT}$ (slave transmitter)		
any DF	$\geqslant 9t_{XTAL}$	$\geqslant 9t_{XTAL}$
	$\leqslant 12t_{XTAL}$	$\leqslant 12t_{XTAL}$
$t_{HD;DAT}$ (master transmitter)		
for DF $\leqslant$ 51	$\geqslant 9t_{XTAL}$	–
	$\leqslant 12t_{XTAL}$	–
for DF $\leqslant$ 99	–	$\geqslant 9t_{XTAL}$
	–	$\leqslant 12t_{XTAL}$
$t_{SU;DAT}$ (master transmitter)		
for DF > 51	$\geqslant 15t_{XTAL}$	–
	$\leqslant 24t_{XTAL}$	–
for DF > 99	–	$\geqslant 15t_{XTAL}$
for DF $\leqslant$ 51	$\geqslant 9t_{XTAL}$	$\leqslant 24t_{XTAL}$
for DF $\leqslant$ 99	–	$\geqslant 9t_{XTAL}$
t_{AC}	$\geqslant 9t_{XTAL}$	$\geqslant 9t_{XTAL}$
	$\leqslant 12t_{XTAL}$	$\leqslant 12t_{XTAL}$
t_{FD}, t_{FC}	$\leqslant$ 100 ns at C_b = 400 pF	$\leqslant$ 100 ns at C_b = 400 pF

Notes to Table 10

t_{XTAL} = one period of the XTAL input frequency (f_{XTAL})
= 280 ns for f_{XTAL} = 3,58 MHz.
DF = divisor (see Table 2 Serial I/O section).
C_b = the maximum bus capacitance for each line.

DEVELOPMENT DATA

APPLICATION INFORMATION

A block diagram of an electronic featurephone built around the PCD3343 is shown in figure 32. It comprises the following dedicated telephony IC's:

- TEA1060/1061 transmission circuit for telephony
- PCD3312 DTMF generator with Serial I/O
- PCE2111 or PCF8577 2 LCD drivers in LCD module MB7020160
- PCD8571 1 K RAM's with Serial I/O; the number of RAM's depends on the required amount of stored telephone numbers
- PCD3360/3361 programmable multi-tone ringer

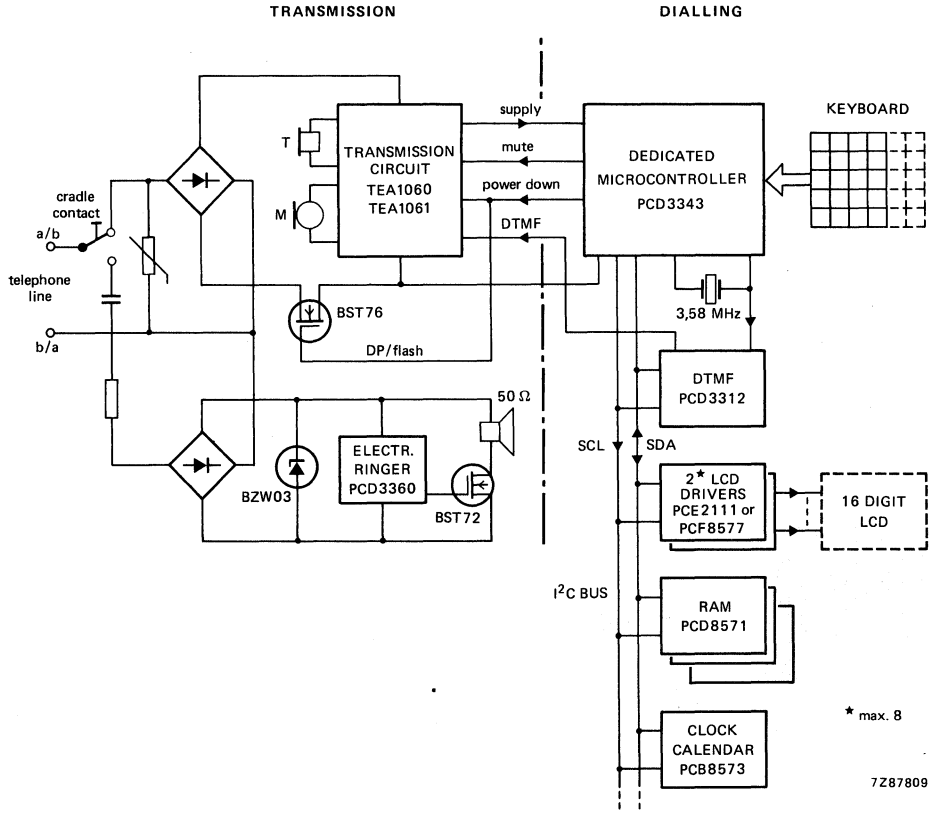


Fig. 32 Block diagram of electronic featurephone with common line interface.

A detailed application diagram of the PCD3343 with PCD3312 (DTMF), two PCD8571 (RAM) and two PCE2111 (LCD display drivers) is shown in figure 33.

Row 5 of the keyboard contains the following special keys:

- P program and autodial
- FL flash or register recall
- R redial or extended redial
- AP access pause

Row 6 contains the different diode options.

Columns 5 and 6 contain the button keys M0 to M9; single name keys for repertory telephone numbers.

APPLICATION INFORMATION (continued)

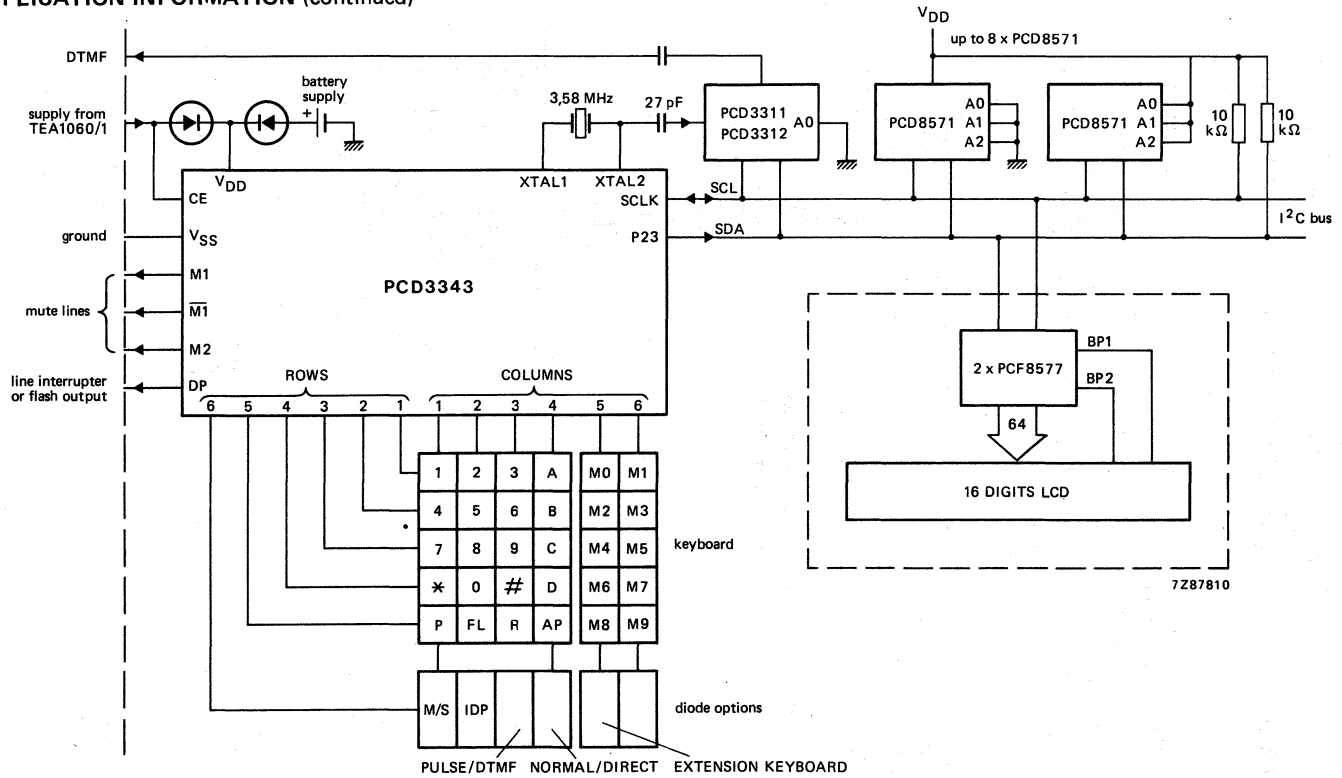


Fig. 33 Application diagram of PCD3343 for electronic featurephone with associated keyboard.

Additional information is available on request for the following:

- Serial I/O
- I^2C bus specification
- Interrupt logic
- Instruction set descriptions
- Software routines for an intelligent telephone set

PROGRAMMABLE MULTI-TONE TELEPHONE RINGER

GENERAL DESCRIPTION

The PCD3360 is a CMOS integrated circuit, designed to replace the electro-mechanical bell in telephone sets. It meets most postal requirements, particularly with tone sequence possibilities and input frequency selectivity. Output signals for a loudspeaker or for a piezo-electric (PXE) transducer are provided. No audio transformer is required since the loudspeaker is driven in class D.

Features

- Output signals for electro-dynamic transducer (loudspeaker) or for piezo-electric transducer (PXE)
- 7 basic frequencies (tones) and a pause
- 4 selectable tone sequences
- 4 selectable repetition rates
- 3 selectable impedance settings
- 3-step automatic swell
- Delta-modulated output signal that approximates a sinewave
- Input frequency discriminator with selectable upper and lower frequency limits
- Output for optical signal

Note

Tone sequences (up to 16 tones long), impedance settings and automatic swell levels are mask programmable for customized versions.

QUICK REFERENCE DATA

Available frequencies (tones)		533/600/667/800/ 1000/1067 and 1333	Hz
Number of intervals per tone sequence		15 or 16	
Lower limits of frequency discriminator		13,33 or 20	Hz
Upper limits of frequency discriminator		30 or 60	Hz
Impedance settings (with 50 Ω loudspeaker)	approx.	7 or 10,5 or 17,5	kΩ
Switch-on delay at 25 Hz	max.	60	ms

PACKAGE OUTLINES

PCD3360P: 16-lead DIL; plastic (SOT-38).
PCD3360T: 16-lead mini-pack; plastic (SO-16L; SOT-162A).

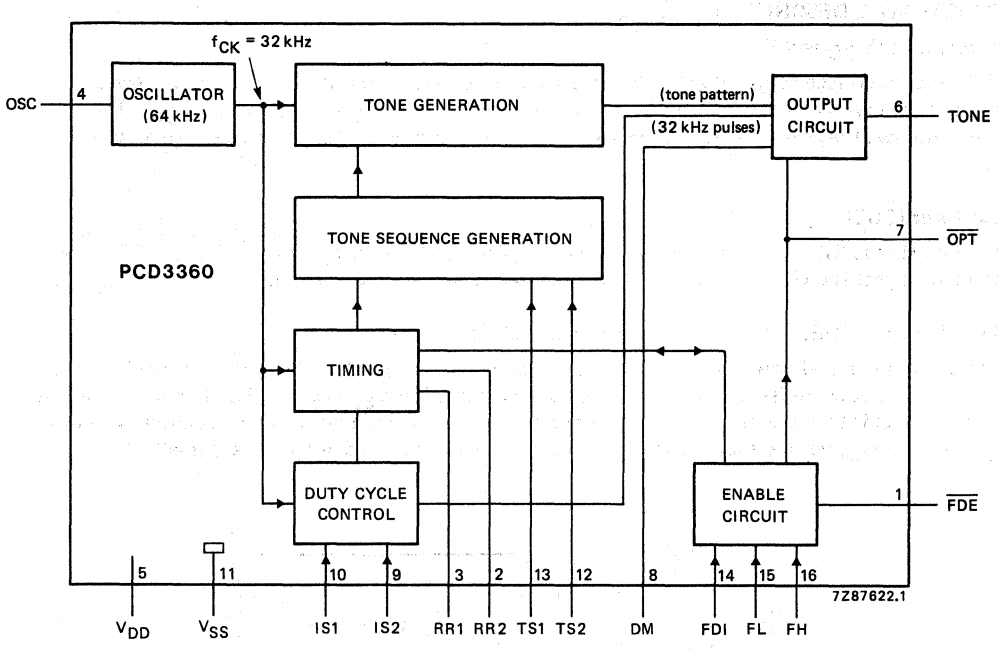


Fig. 1 Block diagram.

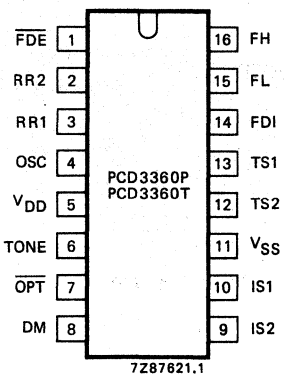


Fig. 2 Pinning diagram for PCD3360P and PCD3360T.

PINNING

1	$\overline{FDE}$	frequency discriminator enable
2	RR2	repetition rate selection
3	RR1	repetition rate selection
4	OSC	oscillator
5	V_{DD}	positive supply
6	TONE	tone output
7	$\overline{OPT}$	optical signal output
8	DM	drive mode selection
9	IS2	impedance setting and automatic swell
10	IS1	impedance setting and automatic swell
11	V_{SS}	negative supply
12	TS2	tone sequence selection
13	TS1	tone sequence selection
14	FDI	frequency discriminator input
15	FL	lower frequency limit selection
16	FH	ıcy limit selection

FUNCTIONAL DESCRIPTION (see Fig. 1)

Supply pins (V_{DD} and V_{SS})

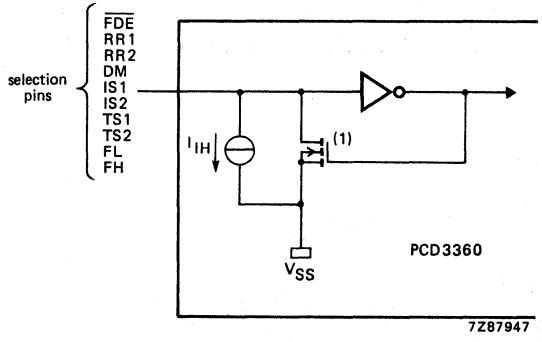
If the supply voltage (V_{DD}) drops below the standby voltage (V_{SB}), the oscillator and most other functions are switched off and the supply current is reduced to the standby current (I_{SB}). The automatic swell register retains its information until V_{DD} drops further to a value V_{AS} at which reset occurs.

Oscillator (OSC)

The 64 kHz oscillator is operated via an external resistor and capacitor connected to pin OSC. The oscillator signal is divided by two to provide the 32 kHz internal system clock.

Selection pins ($\overline{FDE}$, RR2, RR1, DM, IS2, IS1, TS2, TS1, FL and FH)

These pins are pulled down internally by a pull-down current I_{IH} when they are connected to V_{DD}, and by a pull-down resistance R_{IL} when they are connected to V_{SS} (see Fig. 3). Thus when the pins are open-circuit they are defined LOW. Therefore only a single-contact switch is required to connect the pins to V_{DD}; yet the supply current is only marginally increased as I_{IH} is very small.



(1) Transistor resistance = R_{IL} when switched on.

Fig. 3 Input circuit of selection pins.

Frequency discriminator circuit (pins $\overline{FDE}$ and FDI)

The frequency discriminator circuit prevents the ringer being activated by dial pulses, speech or other unqualified signals.

The circuit is enabled or disabled by input $\overline{FDE}$.

When $\overline{FDE}$ is HIGH, FDI acts as a logic enable input.
The circuit will produce tone sequences provided FDI is HIGH and V_{DD} exceeds V_{SB}.
When $\overline{FDE}$ is LOW, FDI acts as the frequency discriminator input.
The circuit will produce tone sequences provided V_{DD} exceeds V_{SB} and the signal at FDI fulfils the conditions set by FL and FH.

When the frequency discriminator is enabled ($V_{DD} > V_{SB}$ and $\overline{FDE}$ = LOW) the circuit will start to produce tone sequences after two rising or two falling edges have occurred at FDI. The time between these edges must be within the limits set by FL and FH.

FUNCTIONAL DESCRIPTION (continued)

The circuit will continue to produce tone sequences provided the time between subsequent falling edges or between subsequent rising edges remains within the limits set by FL and FH, otherwise it will stop. Because two edges are required for detection, either positive or negative, the switch-on delay will vary between 1 and 1,5 cycles of the incoming ringing frequency.

FDI has a Schmitt-trigger action; the levels are set by an external resistor R2 (see Fig. 8) and an internal sink current that is switched from 20 μA (typ.) for FDI = LOW to $< 0{,}1$ μA for FDI = HIGH. Excess current entering FDI via R2 is absorbed by internal diodes clamped to V_{DD} and V_{SS}.

Selection of frequency discriminator limits (FL and FH)

With the frequency discriminator enabled ($V_{DD} > V_{SB}$ and $\overline{FDE}$ = LOW) the lower and upper limits of the input frequency are set by inputs FL and FH as shown by Table 1 and Table 2 respectively.

Table 1 Selection of lower frequency discriminator limits (f_{osc} = 64 kHz)

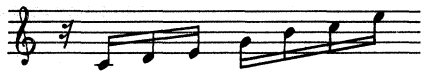
FL input state	lower discriminator limit (Hz)
LOW	20
HIGH	13,33

Table 2 Selection of upper frequency discriminator limits (f_{osc} = 64 kHz)

FH input state	upper discriminator limit (Hz)
LOW	60
HIGH	30

Selection of tone sequences (TS1 and TS2)

A tone sequence is composed of 15 or 16 equal time intervals. Each time interval may be filled with one of seven available tones or with a pause; these are shown together with their corresponding internal ROM tone code in Fig. 4.



tone key	–	c	d	e	g	b	c	e
frequency (Hz)	0	533	600	667	800	1000	1067	1333
frequency ratio		8	9	10	12	15	16	20
tone code	0	1	2	3	4	5	6	7

7Z87948

Fig. 4 Available tones and their corresponding internal ROM tone code.

Four tone sequences are programmed in the internal ROM (see Fig. 5). Inputs TS1 and TS2 determine which tone sequence is selected and output at pin TONE. The sequences are mask programmable with any length up to 16 time intervals.

The tone sequences are repeated continuously provided the enable conditions at inputs $\overline{FDE}$ and FDI are valid and $V_{DD} > V_{SB}$; the first sequence always starts with the first tone shown in Fig. 5.

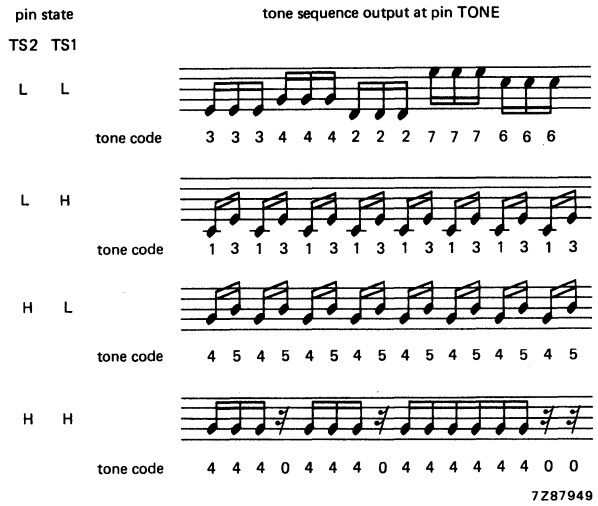


Fig. 5 Tone sequences mask-programmed in the PCD3360.

Selection of repetition rates (RR1 and RR2)

The duration of a time interval within a tone sequence is determined by the state of inputs RR1 and RR2 as shown in Table 3. The resultant variation of repetition rate acts as a distinguishing feature between adjacent telephones.

Table 3 Duration of time intervals (f_{osc} = 64 kHz)

input state		time interval ms
RR1	RR2	
L	L	15
L	H	30
H	L	45
H	H	60

The repetition rate variation can be extended by mask programming (for customer defined versions) the same tone combination for all 4 tone sequences, but with a different number of time intervals per tone. Thus the repetition rate can be selected from 16 values by inputs RR1, RR2, TS1 and TS2.

DEVELOPMENT DATA

FUNCTIONAL DESCRIPTION (continued)

Drive mode selection (DM)

The output signal at pin TONE can be selected for application with electro-dynamic or piezo-electric transducers. An example of both signals, for a tone frequency of 667 Hz, is shown in Fig. 6.

Loudspeaker mode

In the loudspeaker mode (DM = LOW), pin TONE outputs a delta-modulated signal that approximates a sinewave sampled at a rate of 32 kHz. The output pulse duration is determined by pins IS1 and IS2. The resultant acoustic spectrum is aurally more acceptable and has greater penetration than a square wave spectrum because more power is concentrated at the fundamental frequency.

PXE mode

In the PXE mode (DM = HIGH), pin TONE outputs a square wave. In this mode the ringer impedance and sound pressure level are determined by the characteristics (e.g. the size) of the PXE transducer; inputs IS1 and IS2 are inactive.

Setting of impedance, sound pressure level and automatic swell (IS1 and IS2)

With DM = LOW (loudspeaker mode), inputs IS1 and IS2 determine the pulse duration of the output signal and thereby the d.c. resistance R_{xy} (seen at points x and y in Fig. 8), the input impedance Z_I and and also the Sound Pressure Level (SPL). The selection of 3 impedance settings and automatic swell is shown in Table 4.

Table 4 Setting of pulse duration and automatic swell (DM = LOW)

input state		function	ringing burst number (N)	pulse duration (μs)		R_{xy} (kΩ)	Z_I (kΩ)	SPL (dBr)
IS1	IS2			fund.	harm.			
			1	1,9	–	40	tbf	tbf
L	L	automatic	2	2,9	–	20	17,5	–4
		swell	> 2	4,1	1,8	5	7	0
L	H		–	2,9	–	20	17,5	–4
H	L	constant	–	3,8	–	10	10,5	tbf
H	H	level	–	5,4	–	5	7	0

Where:

1. Typical pulse duration values of the fundamental and harmonic frequencies are for f_{osc} = 64 kHz and f_{CK} = 32 kHz.
2. SPL is the relative Sound Pressure Level, and 0 dBr is defined as the SPL for IS1 = IS2 = HIGH.
3. Values of the d.c. resistance R_{xy}, bell impedance (Z_I) and SPL are valid for a value of input voltage V_I = 40 V_{rms} at 25 Hz in Fig. 8.

Setting of impedance, sound pressure level and automatic swell

When pins IS1 and IS2 are both LOW, the circuit operates in the automatic swell mode. The SPL then increases in three steps so that the maximum level is reached for the third ringing burst.
Each time V_{DD} drops below V_{AS} the automatic swell register is reset and the next ringing burst is considered as N = 1 (see Table 4).
A buffer capacitor C3 (see Fig. 8) must hold $V_{DD} > V_{AS}$ during the time between two consecutive ringing bursts of a series.

For each of the other three combinations of pins IS1 and IS2 the pulse duration has a constant value. Thus the ringer can be designed so that the impedance represented at the telephone line will comply with postal requirements that vary in relation to parallel or series connections of more than one ringer.

To satisfy some applications, a harmonic signal is added to the fundamental frequency in the last step of the automatic swell mode. The pulses representing this harmonic signal are interleaved with the pulses of the fundamental signal (see Fig. 7). The difference in pulse duration shown in Table 4, is chosen so that the harmonic level is 10 dB below the fundamental level.
The harmonic frequency range is from 2 kHz to 3,2 kHz. The individual harmonic frequencies for the seven tone codes and the relative fundamental frequencies are shown in Table 5.

Table 5 Harmonic frequency in relation to tone code and fundamental frequency

tone code	frequency (Hz)	
	fundamental	harmonic
1	533	3200
2	600	2400
3	667	2667
4	800	3200
5	1000	2000
6	1067	2133
7	1333	2667

Using a single mask it is possible to program the following:–

- Addition of harmonics in all the other input states of IS1 and IS2
- All pulse duration values
- Other even harmonic frequencies.

Optical output ($\overline{OPT}$)

The $\overline{OPT}$ output is designed to drive an optical signal transducer or lamp. It is LOW when the ringer circuit is enabled and HIGH when the ringer circuit is disabled. This output can also be used to switch the transmitter ON and OFF in the base of a cordless telephone set.

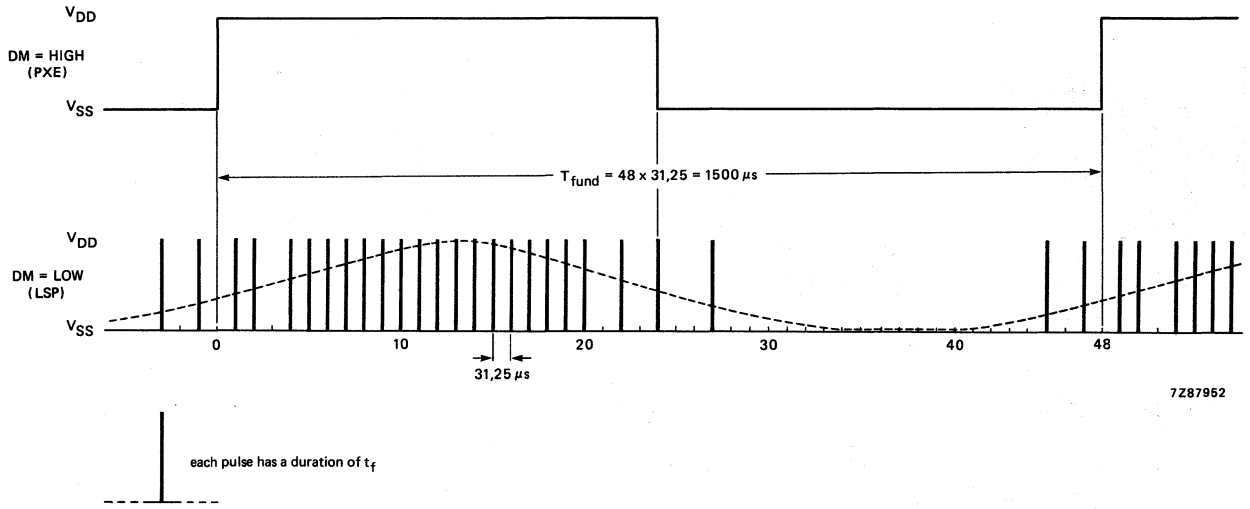


Fig. 6 Fundamental signal (667 Hz) at pin TONE
(for f_{osc} = 64 kHz, to provide f_{CK} = 32 kHz).

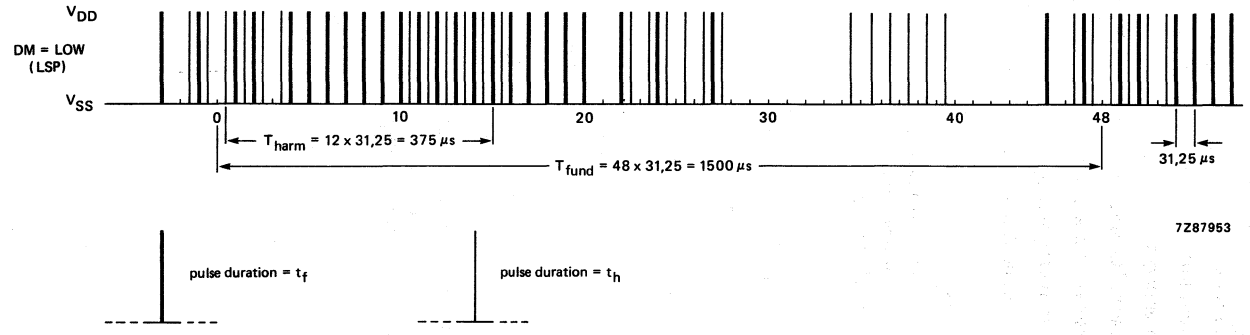


Fig. 7 Fundamental signal (667 Hz) + harmonic signal (2667 Hz) at pin TONE
(for f_{osc} = 64 kHz, to provide f_{CK} = 32 kHz).

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range	V_{DD}		−0,8 to + 9	V
Supply current	I_{DD}	max.	50	mA
D.C. current into any input or output	$\pm I_I, \pm I_O$	max.	10	mA
All input voltages	V_I		−0,8 V to V_{DD} + 0,8	V
Total power dissipation	P_{tot}	max.	300	mW
Total dissipation per output	P_O	max.	50	mW
Storage temperature range	T_{stg}		−65 to + 150	°C
Operating ambient temperature range	T_{amb}		−25 to + 70	°C

HANDLING

Inputs and outputs are protected against electrostatic charge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see 'Handling MOS Devices').

DEVELOPMENT DATA

D.C. CHARACTERISTICS

V_{DD} = 6 V; V_{SS} = 0; f_{osc} = 64 kHz; T_{amb} = −25 to + 70 °C; valid enable conditions at FDI and $\overline{FDE}$; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply					
Operating supply voltage	V_{DD}	V_{SB}+0,1	–	8,0	V
Standby supply voltage (note 1)	V_{SB}	3,9	4,8	5,7	V
Supply voltage for automatic swell reset (note 2)	V_{AS}	–	0,5V_{SB}	–	V
Operating supply current (note 3)	I_{DD}	–	110	140	μA
Standby supply current at $V_{DD} < V_{SB}$ (note 4)	I_{SB}	–	3	8	μA
Inputs					
Input voltage LOW (any pin)	V_{IL}	0	–	0,3V_{DD}	V
Input voltage HIGH (any pin)	V_{IH}	0,7V_{DD}	–	V_{DD}	V
Pull-down circuits of inputs FDE, RR1, RR2, DM, IS1, IS2, TS1, TS2, FL, FH					
pull-down resistance with input at V_{SS}	R_{IL}	–	20	–	kΩ
pull-down current with input at V_{DD}	I_{IH}	–	0,1	–	μA
Pull-down circuit of FDI					
pull-down current with V_{FDI} = 0,3V_{DD}; T_{amb} = 25 °C	I_{SL}	14	23	32	μA
temperature coefficient of I_{SL}	$-\Delta I_{SL}$	–	0,5	–	%/°C
pull-down current with V_{FDI} = 0,8V_{DD}	I_{SH}	–	0,1	–	μA
pull-down current with $V_{DD} < V_{SB}$	I_{SX}	–	0,1	–	μA
Current into input FDI (note 5)	± I_{IS}	–	–	0,2	mA
Outputs					
TONE, $\overline{OPT}$					
Output sink current at V_{OL} = 0,5 V	I_{OL}	1	2	–	mA
Output source current at $V_{OH} = V_{DD}$−0,5 V	$-I_{OH}$	1	2	–	mA

A.C. CHARACTERISTICS

V_{DD} = 6 V; V_{SS} = 0; f_{osc} = 64 kHz; T_{amb} = −25 to + 70 °C; valid enable conditions at FDI and $\overline{FDE}$; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Switch-on delay (with $\overline{FDE}$ = LOW and ringing frequency within limits set by FL and FH)	$t_{d(on)}$	1	–	1,5	note 6
Switch-off delay (with $\overline{FDE}$ = LOW)					
at FL = LOW	$t_{d(off)}$	–	–	50	ms
at FL = HIGH	$t_{d(off)}$	–	–	75	ms
Oscillator frequency at R_{osc} = 365 kΩ; C_{osc} = 56 pF; T_{amb} = 25 °C (note 7)	f_{osc}	60	64	68	kHz
Frequency variation					
as a function of V_{DD}	$-\Delta f_{osc}$	–	1	–	%/V
as a function of T_{amb}	$-\Delta f_{osc}$	–	0,05	–	%/K

DEVELOPMENT DATA

Notes to the characteristics

1. For $V_{DD} < V_{SB}$ the circuit is in standby.
2. At $V_{DD} = V_{AS}$ the automatic swell register is reset.
3. R_{osc} = 365 kΩ; C_{osc} = 56 pF; FDI = $\overline{FDE}$ = V_{DD}; all other inputs and outputs open circuit.
4. The standby supply current is measured with all inputs and outputs open-circuit with the exception of OSC.
5. The current I_{IS} is clamped to V_{DD} and to V_{SS} by two internal diodes. Correct operation is ensured with $V_{FDI} > V_{DD}$ or $V_{FDI} < V_{SS}$, provided the maximum value of I_{IS} is not exceeded. (The input FDI has an extended HIGH and LOW input voltage range.)
6. The switch-on delay is measured in cycles of incoming ringing frequency.
7. Lead lengths of R_{osc} and C_{osc} to be kept to a minimum.

APPLICATION INFORMATION

Application of the PCD3360 in a telephone ringer circuit together with a loudspeaker is shown in Fig. 8.

The threshold levels V_H and V_L of the frequency discriminator circuit are determined by:

- The logic threshold of input FDI ($0{,}5V_{DD}$ typ. 3,4 V for V_{DD} = 6,8 V)
- The pull-down current of input FDI (20 μA typ. for FDI $<$ 3,4 V)
- The value of R2 (680 kΩ in Fig. 8)

For a positive slope, the voltage at R2 must exceed the value V_H before FDI will become HIGH; V_H is the sum of the input threshold and the voltage drop across R2 thus:

$V_H = 3{,}4 + (680 \times 10^3) \times (20 \times 10^{-6}) = 17$ V.

For a negative slope, the voltage at R2 must decrease below the value V_L before FDI will become LOW. Because the current into FDI is negligible with FDI = HIGH the voltage drop across R2 can be discounted, thus V_L = 3,4 V.

The minimum operating voltage across C3 is 17,8 V which is determined by:

- The minimum operating voltage of the PCD3360 (5,8 V)
- The supply current of the PCD3360 (120 μA max.)
- The value of R3 (100 kΩ in Fig. 8)

The total switch-on delay equals approximately the time required to charge the supply capacitor C3 to the minimum operating value, plus the specified switch-on delay of the PCD3360.

The high operating voltage combined with the class D output stage ensures optimal energy conversion and thereby a high sound level. The design can easily be optimized for parallel or series connection of more than one ringer. The diode bridge, zener diode (D1) and resistor R1 protect the ringer against transients up to 5 kV. During these surges the voltage on the 68 V zener diode (BZW03) can rise to 100 V; the DMOS transistor BST72A (TR1) has a maximum drain-source voltage of 100 V. Up to 220 V, 50 Hz can be applied to the a/b terminals without damaging the ringer.
The choke (L1) in series with the 50 Ω loudspeaker increases the sound pressure level by approximately 3 dB by suppression of the 32 kHz carrier frequency and its sidebands.
The flyback diode BAX18A (D2) is a fast type with low forward voltage to obtain high efficiency.

Application of the PCD3360 together with a PXE transducer is shown in Fig. 9. The only significant difference between Fig. 8 and Fig. 9 is the output stage. Two BST72A transistors provide an output voltage swing almost equal to the voltage at C3. Pins IS1 and IS2 are inoperative because DM = HIGH. Volume control is possible using resistor R_V.

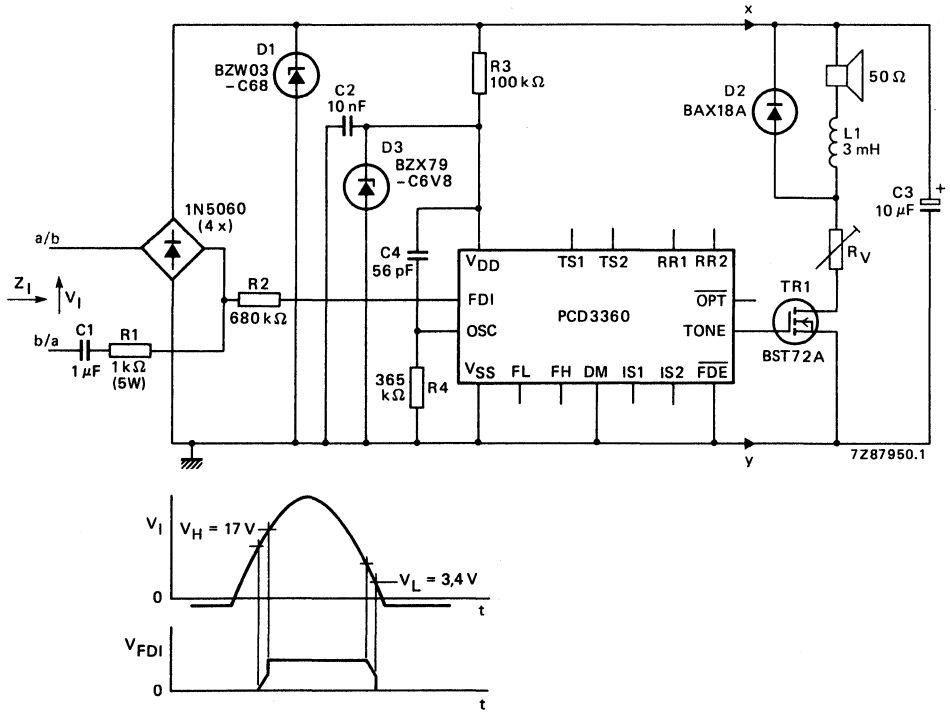


Fig. 8 Transformerless electronic ringer with PCD3360 and a loudspeaker.

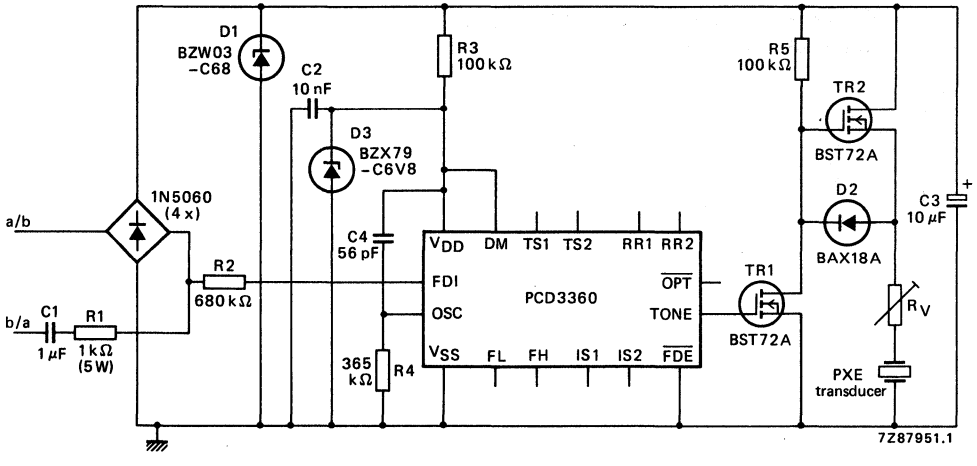


Fig. 9 PCD3360 ringer with PXE transducer.

DEVELOPMENT DATA

MICROPOWER D.C. VOLTAGE DETECTOR

GENERAL DESCRIPTION

The PCF1251 is a CMOS micropower d.c. voltage detector and it is especially designed for power-on/off voltage detection monitoring and reset. The IC has an extremely low current consumption and is therefore particularly suited for battery operated applications. The internal bandgap reference voltage is stable with temperature variations. The voltage trip-point and the hysteresis can be set independently with external resistors. Two of the four outputs can be delayed with an external capacitor.

Features

- Extremely low current consumption
- Built-in bandgap voltage reference
- Wide range of voltage trip-points
- Two pairs of outputs; one pair with delay possibility
- 8-lead DIL or SO-8 mini-pack (plastic packages)

QUICK REFERENCE DATA

parameter	symbol	min.	typ.	max.	unit
Supply voltage range with respect to V_{SS}	V_{DD}	1	–	6	V
Supply current	I_{DD}	–	1	–	μA
Output currents at V_{DD} = 1 V	I_O	–	2	–	mA
Bandgap voltage reference at 25 °C	V_{REF}	1,05	1,15	1,25	V

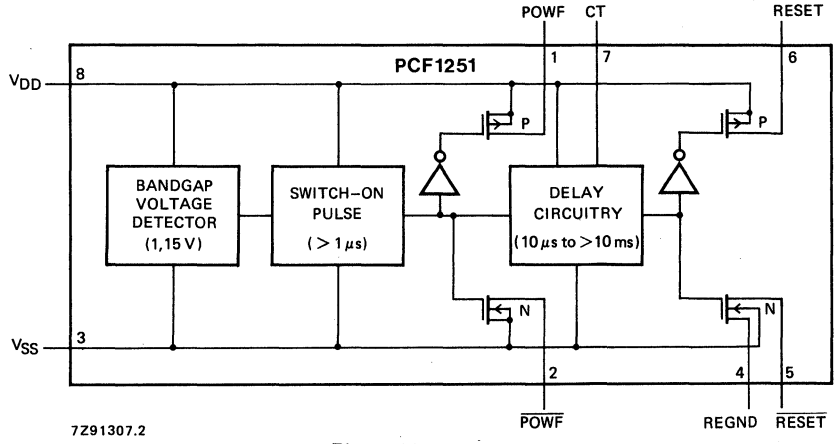


Fig. 1 Block diagram.

PACKAGE OUTLINES

PCF1251P: 8-lead DIL; plastic (SOT-97AE).
PCF1251T: 8-lead mini-pack; plastic (SO-8; SOT-96A).

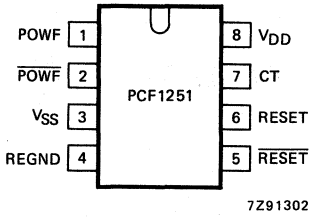


Fig. 2 Pinning diagram.

PINNING

1	POWF	power-fail output
2	$\overline{\text{POWF}}$	power-fail output (inverted)
3	V_{SS}	negative supply voltage
4	REGND	reset ground
5	$\overline{\text{RESET}}$	reset output (inverted; delayed)
6	RESET	reset output (delayed)
7	CT	capacitor for additional delay
8	V_{DD}	positive supply voltage

FUNCTIONAL DESCRIPTION

The PCF1251 consists of a bandgap voltage reference, a comparator and delay circuitry (see Fig. 1). The supply voltage of the circuit (V_{DD} with respect to V_{SS}) is compared with an internal bandgap voltage reference by means of a special comparator. This comparator is connected to the circuit supply voltage. As long as the supply voltage is above the reference voltage level, the four open-drain outputs are all switched off and an extended drain-source voltage of up to 6 V is allowed. When the supply voltage is reduced and reaches the reference voltage level (V_{REF}), the power-fail outputs are switched on (p-channel for POWF and n-channel for $\overline{\text{POWF}}$ outputs). After a delay, determined by an external capacitor between pins CT and V_{DD}, the outputs RESET and $\overline{\text{RESET}}$ are switched on. The same delay will be active when the supply voltage is increased again and exceeds the internal voltage reference, resulting in switching off the outputs.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage with respect to V_{SS}	V_{DD}	–	8	V
Output voltage at pin 2 V_{DD} with respect to V_2	V_2	–	8	V
Output voltage at pin 5 (pin 4 at V_{SS}) V_{DD} with respect to V_5	V_5	–	8	V
Output voltage at pin 1 V_1 with respect to V_{SS}	V_1	–	8	V
Output voltage at pin 6 V_6 with respect to V_{SS}	V_6	–	8	V
Voltage at pin 7 (CT)	V_7	−0,5	V_{DD} + 0,5	V
Current at pin 7 (CT)	I_7	–	20	mA
Output currents at pins 1, 2, 5 and 6	$\lvert I_O \rvert$	–	25	mA
Total power dissipation	P_{tot}	–	150	mW
Operating ambient temperature range	T_{amb}	−40	+85	°C
Storage temperature range	T_{stg}	−55	+125	°C

HANDLING

Inputs and outputs are protected against electrostatic charge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see 'Handling MOS Devices').

CHARACTERISTICS

V_{DD} = 1 to 6 V; V_{SS} = 0 V; T_{amb} = −40 to + 85 °C; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Operating supply voltage	V_{DD}	1	–	6	V
Operating supply current V_{DD} = 6 V; all outputs open	I_{DD}	–	1	3	μA
Bandgap voltage reference; T_{amb} = 25 °C	V_{REF}	1,05	1,15	1,25	V
V_{REF} temperature coefficient	$\Delta V_{REF}/\Delta T$	–	−0,4	–	mV/K
Output current at pins 2 and 5 T_{amb} = 25 °C; $V_{DD} < V_{REF}$; V_O = 0,4 V with respect to V_{SS}	I_O	1	2	–	mA
Output current at pins 1 and 6 T_{amb} = 25 °C; $V_{DD} < V_{REF}$; $-V_O$ = 0,4 V with respect to V_{DD}	$-I_O$	1	2	–	mA

(1) For correct switching of the outputs the slew rate of the supply voltage should be less than 1 V/ms.

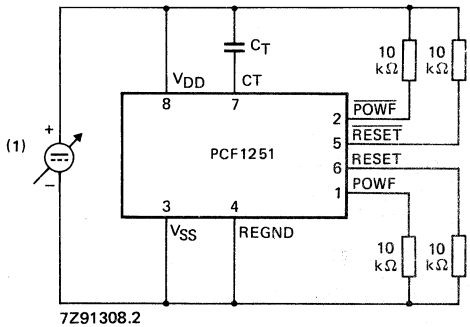


Fig. 3 Test circuit for timing measurements.

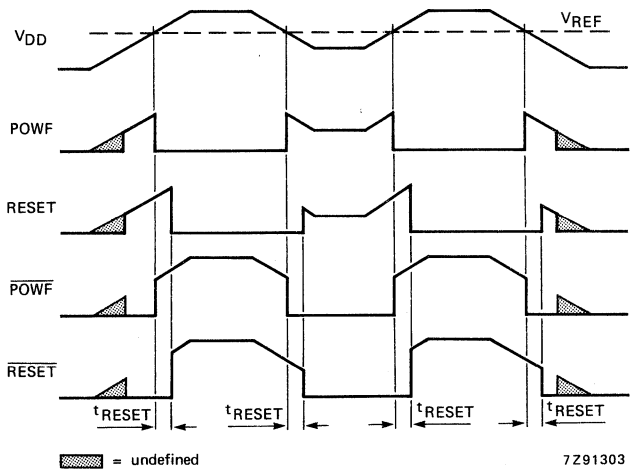


Fig. 4 Timing diagram for slow supply voltage changes.

(1) $t_{RESET} = [0{,}1\ ms + 3{,}2\ ms \times C_T\ (nF)]\ ^{+75\%}_{-50\%}$

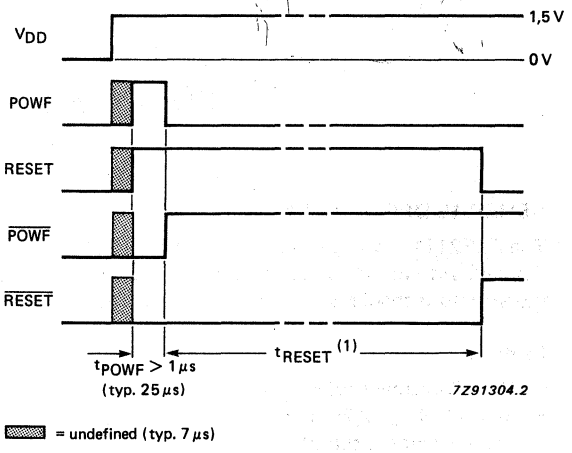


Fig. 5 Timing diagram for fast supply voltage switching on (non-repetitive).

APPLICATION INFORMATION

(1) The value of capacitor C is chosen to limit the slew rate of the supply voltage to less than 1 V/ms (e.g. the hysteresis voltage step on resistor R3).

(2) CT (pin 7) is a high-impedance connection for the capacitor C_T. This capacitor adds to the reset delay time provided by an internal current source (120 nA) and capacitor. Care must be taken to avoid external leakage current at this pin but the pin should not be left open circuit as stray capacitances to V_{SS} can then disturb the delay function.

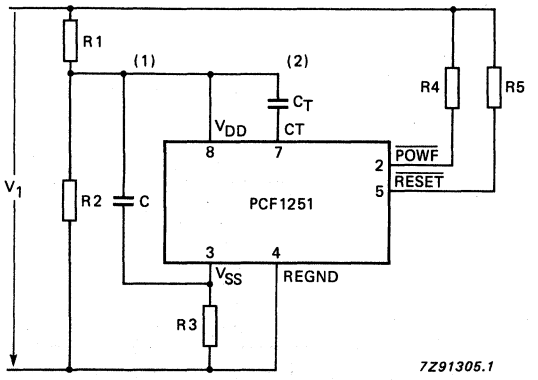


Fig. 6 Application circuit diagram.

(1) $V_{HYST} = V_{TRIP} \times \frac{R3}{R3+R4}$; (0,2 V max.)

(2) $V_{TRIP} = V_{REF} \times \frac{R1+R2}{R2}$

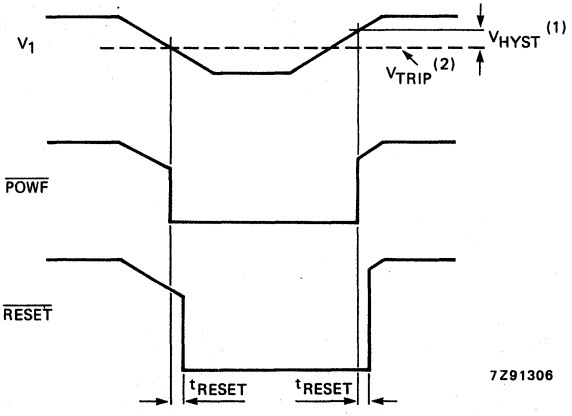


Fig. 7 Timing diagram for the circuit of Fig. 6.

LCD DUPLEX DRIVER

GENERAL DESCRIPTION

The PCF2111 is a single chip, silicon gate CMOS circuit designed to drive an LCD (Liquid Crystal Display) with up to 64 segments in a duplex manner; specially for low voltage applications. A three-line bus structure enables serial data transfer with microcontrollers. All inputs are CMOS/NMOS compatible.

Features

- 64 LCD-segment drive capability
- Supply voltage 2,25 to 6,5 V
- Low current consumption
- Serial data input
- CBUS control
- One-point built-in oscillator
- Expansion possiblity

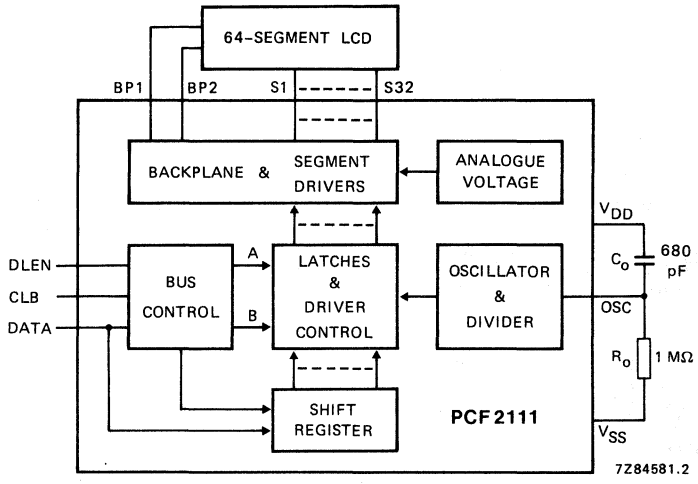


Fig. 1 Block diagram.

PACKAGE OUTLINES

PCF2111P: 40-lead DIL; plastic (SOT-129).
PCF2111T: 40-lead mini-pack; plastic (VSO-40; SOT-158A).

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage with respect to V_{SS}	V_{DD}		−0,3 to 8 V
Voltage on any pin	V_n	V_{SS}	−0,3 to V_{DD} + 0,3 V
Operating ambient temperature range	T_{amb}		−40 to + 85 °C
Storage temperature range	T_{stg}		−55 to + 125 °C

HANDLING

Inputs and outputs are protected against electrostatic charge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see 'Handling MOS devices').

CHARACTERISTICS

V_{DD} = 2,25 to 6,5 V; V_{SS} = 0 V; T_{amb} = −40 to + 85 °C; R_o = 1 MΩ; C_o = 680 pF; unless otherwise specified

parameter	condition	symbol	min.	typ.	max.	unit
Supply current	no external load	I_{DD}	–	10	50	μA
Supply current	no external load; T_{amb} = −25 to + 85 °C	I_{DD}	–	–	30	μA
Display frequency	see Fig. 8; T = 680 μs	f_{LCD}	60	80	100	Hz
D.C. component of LCD drive	with respect to V_{SX}	V_{BP}	–	± 10	–	mV
Load on each segment driver			–	–	10	MΩ
			–	–	500	pF
Load on each backplane driver			–	–	1	MΩ
			–	–	5	nF
Input voltage HIGH	see Fig. 9	V_{IH}	2	–	–	V
Input voltage LOW	see Fig. 9	V_{IL}	–	–	0,6	V
Rise time V_{BP} to V_{SX}	max. load	t_r	–	20	–	μs
Inputs CLB, DATA, DLEN	see note on next page					
Input capacitance	for SOT-129 package	C_{IN}	–	–	10	pF
	for SOT-158A package	C_{IN}	–	–	5	pF
Rise and fall times	see Fig. 2	t_r, t_f	–	–	10	μs
CLB pulse width HIGH	see Fig. 2	t_{WH}	1	–	–	μs
CLB pulse width LOW	see Fig. 2	t_{WL}	9	–	–	μs

CHARACTERISTICS (continued)

parameter	condition	symbol	min.	typ.	max.	unit
Data set-up time DATA → CLB	see Fig. 2	t_{SUDA}	8	–	–	μs
Data hold time DATA → CLB	see Fig. 2	t_{HDDA}	8	–	–	μs
Enable set-up time DLEN → CLB	see Fig. 2	t_{SUEN}	1	–	–	μs
Disable set-up time CLB → DLEN	see Fig. 2	t_{SUDI}	8	–	–	μs
Set-up time (load pulse) DLEN → CLB	see Fig. 2	t_{SULD}	8	–	–	μs
Busy-time from load pulse to next start of transmission	see Fig. 2	t_{BUSY}	8	–	–	μs
Set-up time (leading zero) DATA → CLB	see Fig. 2	t_{SULZ}	8	–	–	μs

Note

All timing values are referred to $V_{IH\ min}$ and $V_{IL\ max}$* (see Fig. 2). If external resistors are used in the bus lines (see Fig. 9), the extra time constant has to be added.

* With an input voltage swing of $V_{IL\ max}$–0,1 V to V_{IHmin} + 0,1 V.

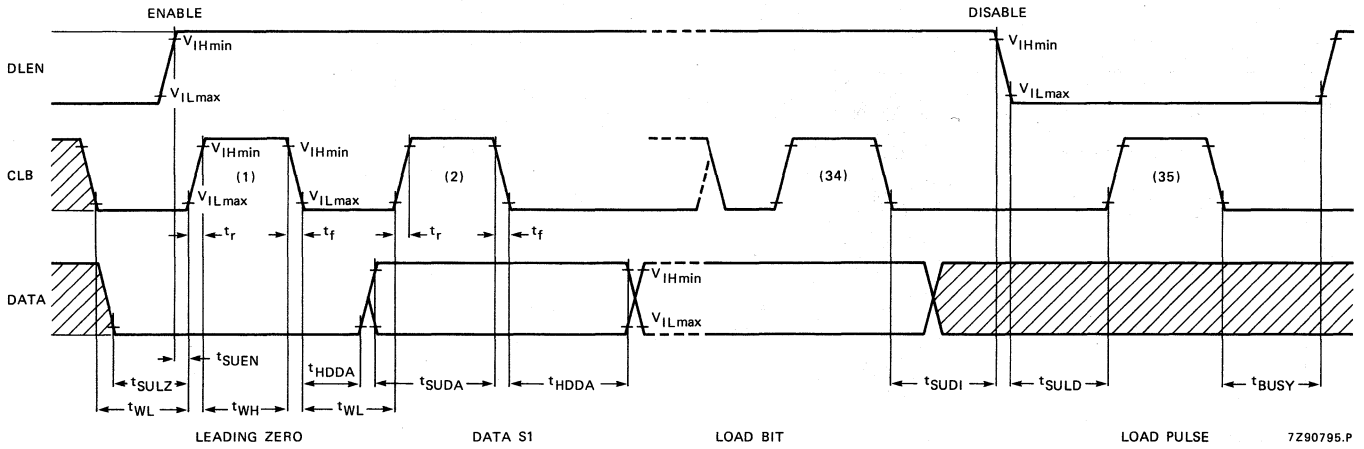


Fig. 2 CBUS timing.

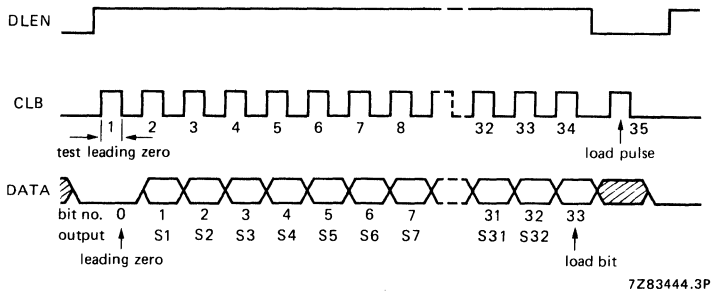


Fig. 3 CBUS data format.

Notes to Fig. 3

An LCD segment is activated when the corresponding DATA-bit is HIGH.
When DATA-bit 33 is HIGH, the A-latches (BP1) are loaded. With DATA-bit 33 LOW, the B-latches (BP2) are loaded. CLB-pulse 35 transfers data from shift register to selected latches.

The following tests are carried out by the bus control logic:

a. Test on leading zero.
b. Test on number of DATA-bits.
c. Test of disturbed DLEN and DATA signals during transmission.

If one of the test conditions is not fulfilled, no action follows the load condition (load pulse with DLEN is LOW) and the driver is ready to receive new data.

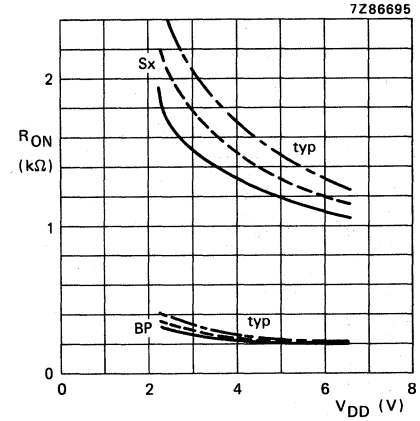


Fig. 4 Output resistance of backplane and segments.
——— T_{amb} = −40 °C; − − − T_{amb} = + 25 °C; − · − · T_{amb} = +85 °C.

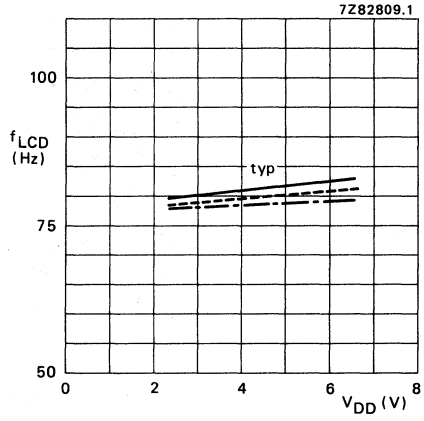


Fig. 5 Display frequency as a function of supply voltage; R_oC_o = 680 μs.
——— T_{amb} = −40 °C; − − − T_{amb} = + 25 °C; − · − · T_{amb} = +85 °C.

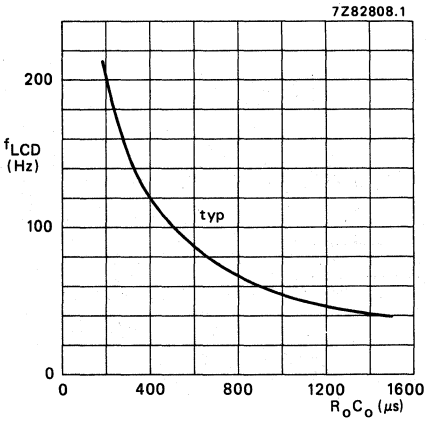


Fig. 6 Display frequency as a function of R_o x C_o time; T_{amb} = 25 °C.

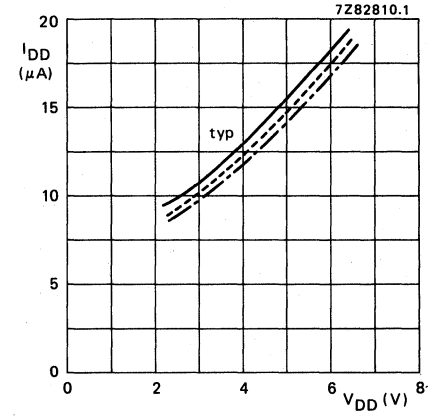


Fig. 7 Supply current as a function of supply voltage.
——— T_{amb} = −40 °C; − − − T_{amb} = + 25 °C; − · − · T_{amb} = +85 °C.

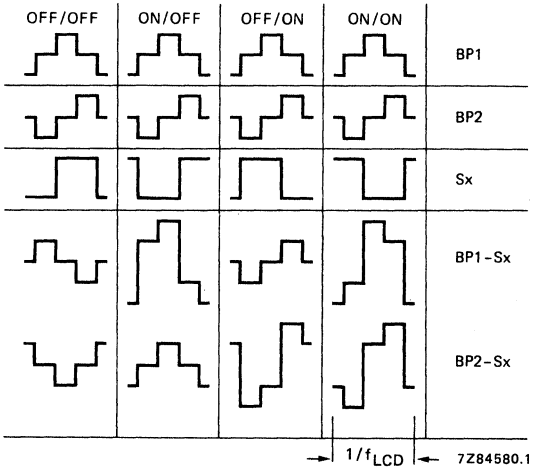


Fig. 8 Timing diagram.

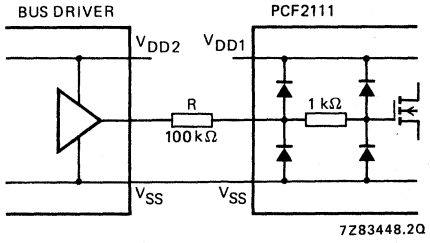
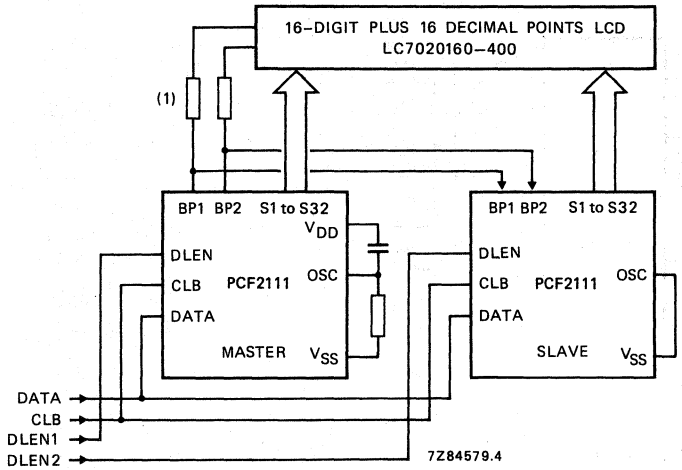


Fig. 9 Input circuitry.

Note to Fig. 9

V_{SS} line is common. In systems where it is expected that $V_{DD2} > V_{DD1} + 0{,}5$ V, a resistor should be inserted to reduce the current flowing through the input protection.
Maximum input current $\leqslant$ 40 μA.



(1) In the slave mode, the serial resistors between BP1 and BP2 of the PCF2111 and the backplane of the LCD must be $> 2{,}7\ k\Omega$. In most applications the resistance of the interconnection to the LCD already has a higher value.

Fig. 10 Diagram showing expansion possibility for a 16-digit plus 16 decimal points LCD.

Note to Fig. 10

By connecting OSC to V_{SS} the BP-pins become inputs and generate signals synchronized to the single oscillator frequency, thus allowing expansion of several PCF2111, PCF2110 and PCF2100 ICs up to the BP drive capability of the master.

PCF2100 is a 40 LCD-segment driver; PCF2110 is a 60 LCD-segment driver plus 2 LED driver outputs.

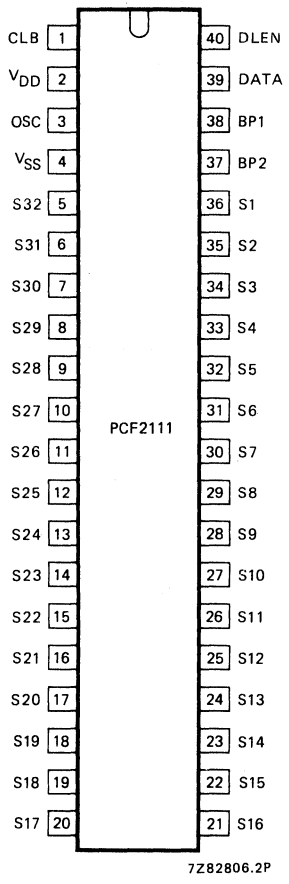


Fig. 11 Pinning diagram.

PINNING

Supply

2	V_{DD}	Positive supply
4	V_{SS}	Negative supply

Inputs

3	OSC	Oscillator input	
39	DATA	Data line	CBUS
40	DLEN	Data line enable	CBUS
1	CLB	Clock burst	CBUS

Outputs

38	BP1	Backplane drivers (common of LCD)
37	BP2	Backplane drivers (common of LCD)
S1 to S32		LCD driver outputs

VOICE SYNTHESIZER

GENERAL DESCRIPTION

The PCF8200 is a CMOS integrated circuit for generating good quality speech from digital code with a programmable bit rate. The circuit is primarily intended for applications in microprocessor controlled systems, where the speech code is stored separately.
Applications include automotive, telephony, personal computers, annunciators, aids for the handicapped, and general industrial devices.

Features

- Male and female speech with good quality
- Speech-band from 0 to 5 kHz
- Bit-rate between 455 bits/second and 4545 bits/second
- Programmable frame duration
- Programmable speaking speed
- CMOS technology
- Operating temperature range −40 to + 85 °C
- Single 5 V supply with low power consumption and power-down stand-by mode
- Interfaces easily with most popular microcomputers and microprocessors through 8 bit parallel bus or I^2C bus
- Software readable status word (parallel bus or I^2C bus)
- BUSY-signal and $\overline{REQ}$-signal hardware readable
- Internal low-pass filter and 11-bit D/A converter

QUICK REFERENCE DATA

parameter	symbol	min.	typ.	max.	unit
Supply voltage	V_{DD}	–	5	–	V
Supply current	I_{DD}	–	12	#	mA
Supply current (stand-by)	$I_{DD(SB)}$	–	1	–	μA
Inputs					
Input voltage	V_{IH}	2,0	–	V_{DD}	V
Input voltage	V_{IL}	0	–	0,8	V
Input capacitance	C_I	–	7	–	pF
Outputs (D5 to D7)					
Output voltage high	V_{OH}	3,5	–	V_{DD}	V
Output voltage low	V_{OL}	0	–	0,4	V
Load capacitance	C_L	–	–	80	pF
Operating ambient temperature range	T_{amb}	−40	–	+ 85	°C

Value not yet available.

PACKAGE OUTLINE

24-lead DIL; plastic (SOT-101A).

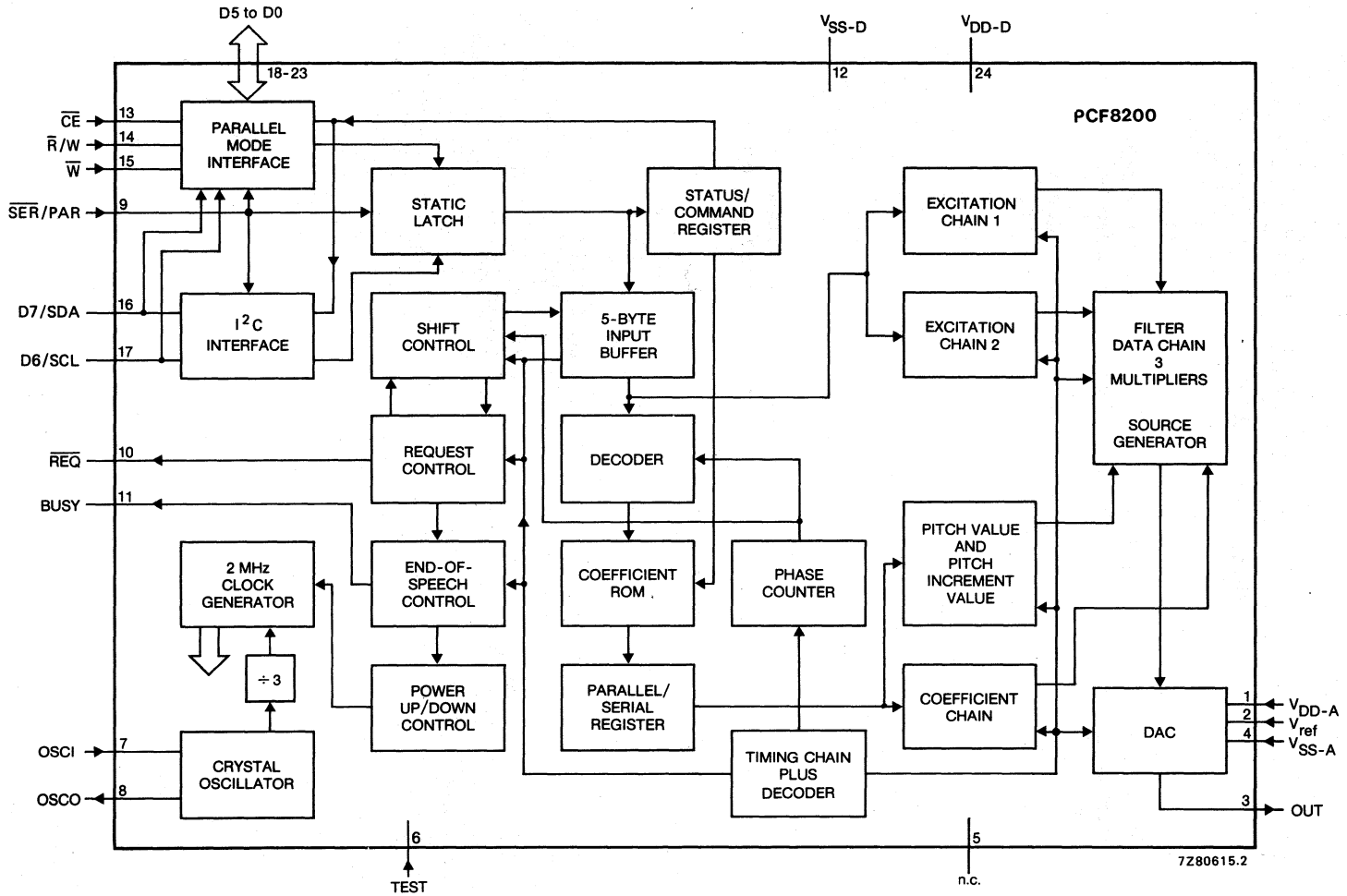


Fig. 1 Block diagram.

PINNING

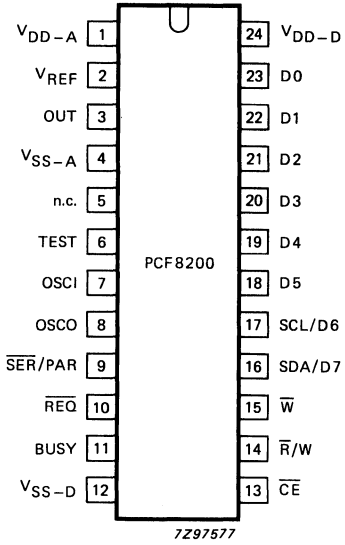


Fig. 2 Pinning diagram.

DEVELOPMENT DATA

1	V_{DD-A}	positive supply voltage for DAC output stage
2	V_{REF}	DAC reference voltage input
3	OUT	speech output
4	V_{SS-A}	negative supply voltage for DAC stage
5	n.c.	not connected
6	TEST	for normal operation this pin must be grounded (V_{SS})
7	OSCI	oscillator input
8	OSCO	oscillator output
9	$\overline{SER}$/PAR	for parallel data bus operation this pin is hard-wired to V_{DD}, or to V_{SS} to enable the I^2C bus
10	$\overline{REQ}$	status bit indicating request for data
11	BUSY	status indicating synthesizer busy
12	V_{SS-D}	negative supply voltage for digital circuits
13	$\overline{CE}$	chip-enable input
14	R/$\overline{W}$	read/write control input
15	$\overline{W}$	write input
16	SDA/D7	I^2C bus serial data input/output (serial mode) or parallel data input/output D7 (parallel mode)
17	SCL/D6	I^2C bus serial clock input/output (serial mode) or parallel data input/output D6 (parallel mode)
18	D5	parallel data input/outputs
19	D4	
20	D3	
21	D2	
22	D1	
23	D0	
24	V_{DD-D}	positive supply voltage for digital circuits

FUNCTIONAL DESCRIPTION

The synthesizer has been designed for a vocal tract modelling technique of voice synthesis. An excitation signal is fed to a series of resonators. Each resonator simulates one of the formants in the original speech. It is controlled by two parameters, one for the resonant frequency and one for the bandwidth. Five formants are needed for male speech and four for female speech. The output of this system is defined by the excitation signal, the amplitude values and the resonator settings. By periodic updating of all parameters very high quality speech can be produced.

OPERATION

Speech characteristics change quite slowly, therefore the control parameters for the speech synthesizer can be adequately updated every few tens of milliseconds with interpolation during the interval to ensure a smooth changeover from one parameter value to the next. In the PCF8200 the standard-frame duration can be set to 8,8 , 10,4, 12,8 or 17,6 milliseconds with the speed-option, speaking speed, in the command-register.
The duration of each individual speech frame is programmable to be 1, 2, 3 or 5 times the standard-frame duration.

	10	01	00	11	FS0, FS1
00	8,8	10,4	12,8	17,6	ms
01	17,6	20,8	25,6	35,2	ms
10	26,4	31,2	38,4	52,8	ms
11	44,0	52,0	64,0	88,0	ms
FD1, FD0					

Table 1. Frame duration as a function of speed-option (FS1, FS0) and frame-duration (FD1, FD0).

The excitation signal is a random noise source for unvoiced sounds and a programmable pulse generator for voiced sounds. Both sources have an amplitude modulator which is updated 8 times in one speech-frame by linear interpolation. The pitch is updated every 1/8 of a standard frame.

The excitation signal is filtered with a five formant filter for male speech and a four formant filter for female speech. The formant filter is a cascade of all second-order sections. The control parameters, formant-frequency and formant-bandwidth, are updated eight times per speech frame by linear interpolation.
A block diagram of the formant synthesizer is shown in Fig. 3.

The filter output is upsampled to 80 kHz and filtered with a digital low-pass filter. Before the signal is digital to analogue converted (DAC), with an 11-bit switched capacitor DAC, the signal is multiplied with a DAC-amplitude factor. The use of a digital filter means that no external audio filtering is required for low-medium applications and minimal filtering is required for those applications requiring very high quality speech.

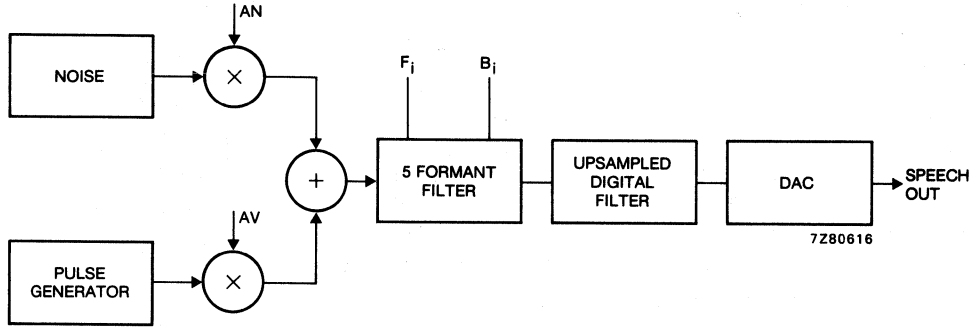


Fig. 3 Block diagram of formant synthesizer.

DATA FORMAT

Three types of format are used for data transfer to the synthesizer.

DAC-amplitude factor

The DAC-amplitude factor is one byte, which is used to optimize the digital speech signal to the 11-bit DAC. It is the first byte after a STOP or a BADSTOP or V_{DD} on. Table 2 indicates the amplitude factor.

byte	factor	dB
01110000	3,5	10,88
10110000	3,25	10,24
00110000	3,0	9,54
11010000	2,75	8,97
01010000	2,5	7,96
10010000	2,25	7,04
00010000	2,0	6,02
11100000	1,75	4,86
01100000	1,5	3,52
10100000	1,25	1,94
00100000	1,0	0,00
11000000	0,75	−2,50
01000000	0,5	−6,02
10000000	0,25	−12,04
00000000	0,0	
11110000	HEX code F0 is not allowed as a DAC amplitude	

Table 2 DAC amplitude factor.

Start pitch

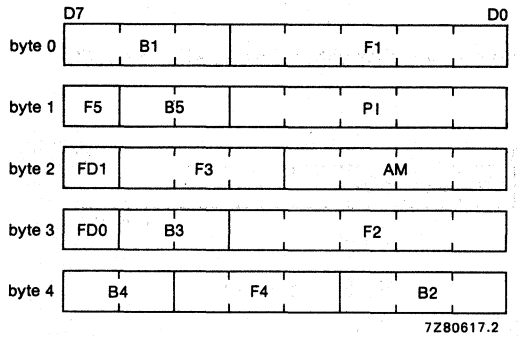
The second byte after a STOP or BADSTOP, or V_{DD} on is the start pitch. It is a one byte start value for the on-chip pitch-period generator.

Frame Data

The frame data is a five byte block which contains the filter and source information:

pitch increment/decrement value	5 bits
amplitude	4 bits
frame duration	2 bits
frequency of 1st formant	5 bits
frequency of 2nd formant	5 bits
frequency of 3rd formant	3 bits
frequency of 4th formant	3 bits
frequency of 5th formant	1 bit
bandwidth of 1st formant	3 bits
bandwidth of 2nd formant	3 bits
bandwidth of 3rd formant	2 bits
bandwidth of 4th formant	2 bits
bandwidth of 5th formant	2 bits
	40 bits = 5 bytes

The frame-data bits are organized as shown in Fig. 4.



It is not allowed to set byte 0 to the hexadecimal value 00.

Fig. 4 Format of frame-date.

CONTROL FORMAT

Command Write

A command write consists of two bytes, and it may occur before a data block. The four bits which can be written are shown in Fig. 5.

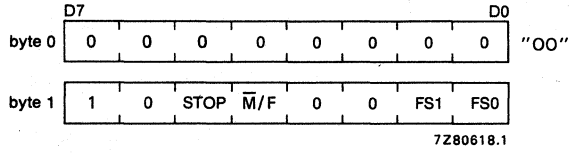


Fig. 5 Control write: first byte fixed, second byte control.

FS0, FS1 speed option

FS1	FS0	speech speed	standard-frame duration
0	0	100%	12,8 ms
0	1	145%	8,8 ms
1	0	123%	10,4 ms
1	1	73%	17,6 ms

$\overline{M}$/F, male/female option

$\overline{M}$/F = 0 male quantization table
= 1 female quantization table

STOP

STOP = 1 stop; repeat last complete frame with amplitude = 0 (no excitation signal)
= 0 if the frame data is not sent within the duration of a half frame, there will be a BADSTOP:

1. $\overline{REQ}$ = 1 STOP = 0
2. Repeat last frame with amplitude = 0
3. BUSY = 0

Status Read

Three status bits can be read out at any time without a preceding byte (00).
This is shown in Fig. 6.

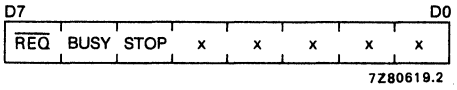


Fig. 6 Status read.

$\overline{REQ}$	= 1	No data required
	= 0	Synthesizer requesting for new data
BUSY	= 1	Busy (an utterance is pronounced)
	= 0	Idle, $\overline{REQ}$ will set to 1; the synthesizer is in STOP or BADSTOP mode
STOP		The STOP bit is the same as the stop bit written to the synthesizer during a command write. STOP = 1, BUSY = 0 stopped by the user. STOP = 0, BUSY = 0 BADSTOP because the data was not sent in time.

After initial power-up the status/command register is set to the following status:

FS0, FS1	= 0	Standard-frame duration of 12,8 ms
$\overline{M}$/F	= 0	Male quantization table
STOP	= 0	
BUSY	= 0	Idle
$\overline{REQ}$	= 1	No data required

DEVELOPMENT DATA

INTERFACE PROTOCOL

Data can be written to the synthesizer when $\overline{REQ}$ = 0 or, when $\overline{REQ}$ = 1 and BUSY = 0. Figure 7 shows the interface protocol of the synthesizer.

In parallel mode the synthesizer is activated by sending the DAC-amplitude factor. In serial mode the DAC-amplitude factor can be sent as soon as the synthesizer is powered-up.

The I²C transmitter/receiver will then acknowledge. When the request for the pitch-byte occurs the byte must be provided within the duration of a half standard frame. If the byte is not provided in time a BADSTOP will be generated.

During each data write operation, the status bit $\overline{REQ}$ will be set to '1'.
Within a frame data block, it disappears within a few microseconds, asking for the next byte of that block. If the bytes of frame data are not provided within the time-duration of a half frame, a BADSTOP will be generated.

I²C ADDRESS

On chip there is a I²C slave receiver/transmitter with the address:

7 6 5 4 3 2 1 0
0 0 1 0 0 0 0 R/W

POWER UP

The synthesizer will be set to power-up on a parallel-write sequence.

PAR-mode: The input-latches are active so they can receive the first byte

SER-mode: The I^2C transmitter/receiver will not acknowledge until the synthesizer has powered-up. To power up the synthesizer a parallel write sequence (Fig. 9) must be made to the synthesizer by using external logic for the control lines; at least one line must be toggled, $\overline{CE}$, while $\overline{W} = 0$ and $\overline{R}/W = 1$.
The synthesizer can be set to permanent power-up by hard-wired control pins ($\overline{CE} = 0$, $\overline{R}/W = 1$, $\overline{W} = 0$).

POWER DOWN MODE

When BUSY = 0 the synthesizer will be set to power-down. In the power-down mode the status/command register will be retained.
In power-down mode the clock-oscillator is switched off. After initial V_{DD} the synthesizer is in power-down mode.

HANDLING

All inputs and outputs are protected against electrostatic charge under normal handling conditions.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage	any pin with respect to V_{SS}	V_{DD}	−0,3	7,5	V
Input voltage	any pin with respect to V_{SS}	V_I	−0,3	7,5	V
Output voltage	any pin with respect to V_{SS}	V_O	−0,3	7,5	V
D.C. input diode current	$V_I < V_{SS}$	$-I_{IK}$	–	20	mA
	$V_I > V_{DD}$	I_{IK}	–	20	mA
D.C. output diode current	$V_O < V_{SS}$	$-I_{OK}$	–	20	mA
	$V_O > V_{DD}$	I_{OK}	–	20	mA
Operating ambient temperature range		T_{amb}	−40	85	°C
Storage temperature range		T_{stg}	−55	125	°C

CHARACTERISTICS

T_{amb} = −45 to + 85 °C; supply voltage (V_{DD} to V_{SS}) = 4,5 to 5,5 V with respect to V_{SS}, unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply					
Supply voltage	V_{DD}	4,5	5,0	5,5	V
Supply current	I_{DD}	–	10	–	mA
Standby current	$I_{DD(SB)}$	–	200	–	μA
Inputs					
$\overline{CE}$, R/$\overline{W}$, $\overline{W}$					
Input voltage HIGH	V_{IH}	2,0	–	V_{DD}	V
Input voltage LOW	V_{IL}	0	–	0,8	V
Input leakage current V_{in} = 0 to 5,5 V	I_{IR}	−10	–	10	μA
Rise and fall times (note 2)	t_{rf}	–	–	50	ns
Input capacitance	C_I	–	–	7	pF
OSCI					
Input voltage HIGH	V_{IH}	2,2	–	V_{DD}	V
Input voltage LOW	V_{IL}	0	–	0,8	V
Input leakage current V_{in} = 0 to 5,5 V	I_{IR}	−10	–	10	μA
Rise and fall times (note 2)	t_{rf}	–	–	50	ns
Input capacitance	C_I	–	–	7	pF
PARALLEL MODE					
Input Characteristics (D0 to D7)					
Input voltage HIGH	V_{IH}	2,0	–	V_{DD}	V
Input voltage LOW	V_{IL}	0	–	0,8	V
Input leakage current (V_{in} = 0 to 5,5 V, output off)	I_{IR}	−10	–	10	μA
Input capacitance	C_I	–	–	7	pF
Output Characteristics (D5 to D7 only)					
Output voltage HIGH (I_{OH} = −100 μA)	V_{OH}	3,5	–	V_{DD}	V
Output voltage LOW (I_{OL} = 3,2 mA)	V_{OL}	0	–	0,4	V
Load capacitance	C_L	–	–	80	pF
Rise and fall times (note 3)	t_{rf}	–	–	50	ns
SERIAL MODE					
Input characteristics (SDA and SDL)					
Input voltage HIGH	V_{IH}	3,0	–	V_{DD}	V
Input voltage LOW	V_{IL}	0	–	1,5	V
Input leakage current (V_{in} = 0 to 5,5 V, output off)	I_{IR}	−10	–	10	μA
Input capacitance	C_I	–	–	10	pF

DEVELOPMENT DATA

parameter	symbol	min.	typ.	max.	unit
Output Characteristics (SDA only, open drain)					
Output voltage LOW (I_{OL} = 3 mA)	V_{OL}	0	–	0,4	V
OSCILLATOR					
Crystal frequency	f_{XTAL}	–	6	6,1	MHz
V_{REF}					
Reference voltage	V_{REF}	1,9	–	$\frac{V_{DD}-1,5}{1,25}$	V
Input leakage current (active)	I_{IR}	–	5	–	μA
Outputs					
$\overline{REQ}$, BUSY					
Output voltage HIGH (I_{OH} = 100 μA)	V_{OH}	3,5	–	V_{DD}	V
Output voltage LOW (I_{OL} = 3,2 mA)	V_{OL}	0	–	0,4	V
Load capacitance	C_L	–	–	80	pF
Rise and fall times (note 3)	t_{rf}	–	–	50	ns
OUT					
Output voltage	V_{OUT}	0,66 x V_{REF}		1,34 x V_{REF}	V
Minimum external load		600	–	–	Ω
Timing characteristics (note 1) (Figs 8 and 9)					
Write enable	t_{WR}	200	–	–	ns
Data set-up for write	t_{DS}	150	–	–	ns
Data hold for write	t_{DH}	30	–	–	ns
Read enable	t_{RD}	200	–	–	ns
Data delay for read (note 2)	t_{DD}	–	–	150	ns
Data floating for read (note 2)	t_{DF}	–	–	150	ns
Control set-up	t_{CS}	0	–	–	ns
Control hold	t_{CH}	0	–	–	ns
REQ new (new byte of the same speech frame)	t_{RN}	–	# (≈ 3)		μs
REQ Valid	t_{RV}	0	–	–	ns
REQ Hold	t_{RH}	–	250	#	ns

NOTES TO THE CHARACTERISTICS

1. Timing reference level is 1,5 V; supply 5 V ± 10%; temperature range of −40 °C to 85 °C.
2. Levels greater than 2 V for a '1' or less than 0,8 V for a '0' are reached with a load of one TTL input and 50 pF.
3. Rise and fall times between 0,6 V and 2,2 V levels.

Values not yet available.

DEVELOPMENT DATA

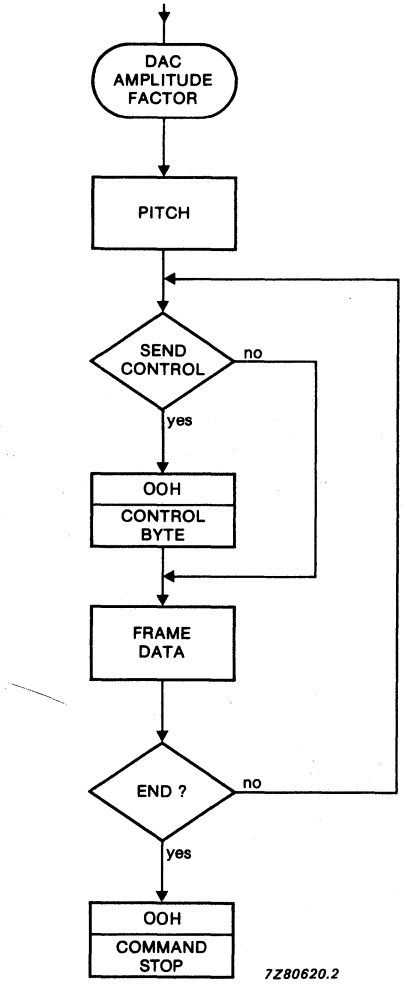
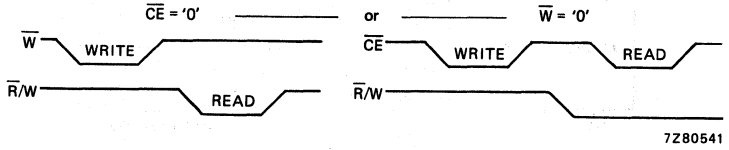


Fig. 7 Interface protocol.

Timing diagrams

The control signals $\overline{CE}$, $\overline{R}/W$ and $\overline{W}$ have been specified to enable easy interface to most microprocessors and microcomputers. For instance with connection to an MAB8048 microcomputer the $\overline{R}/W$ and $\overline{W}$ inputs can be used as the RD and WR strobe inputs.



Typical connection of control signals.

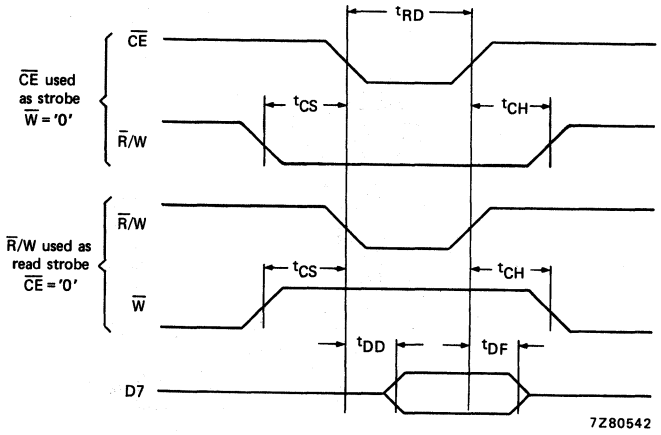


Fig. 8 Read timing.

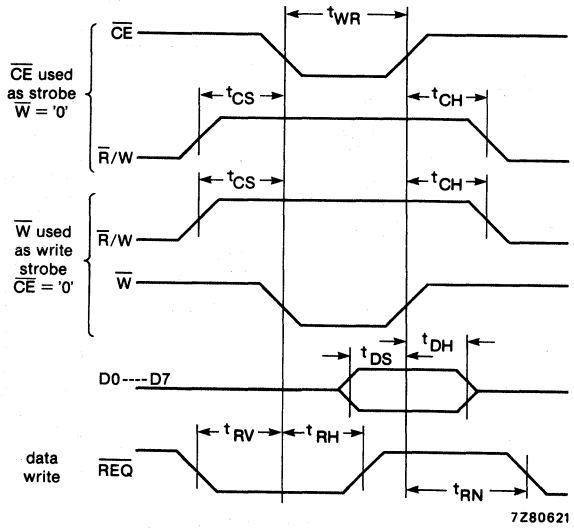


Fig. 9 Write timing.

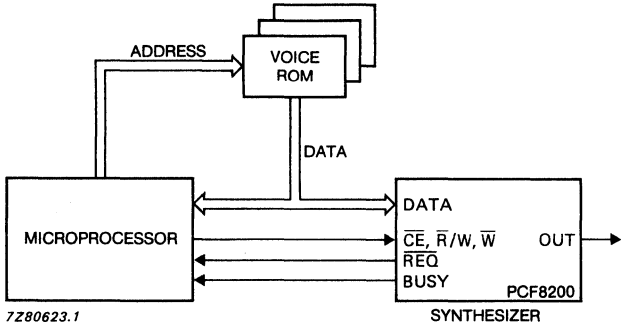


Fig. 10 Typical application configuration with parallel interface.

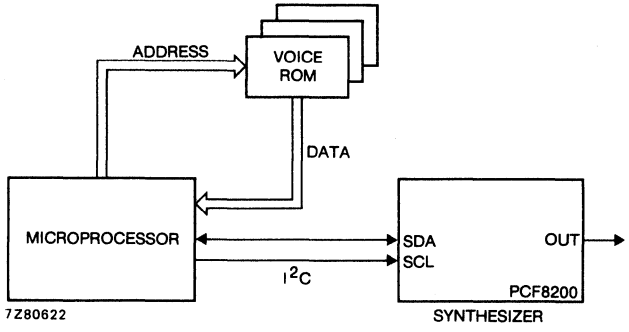


Fig. 11 Typical application configuration with series interface.

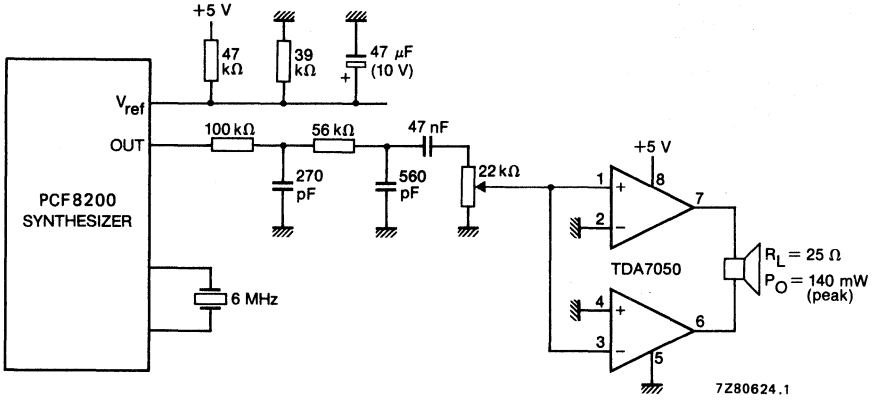


Fig. 12 An example of an output configuration.

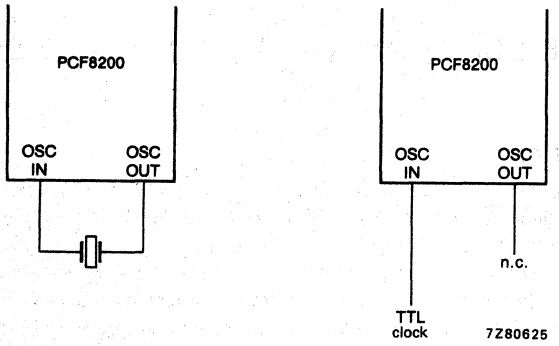


Fig. 13 Oscillator clock configurations.

UNIVERSAL LCD DRIVER FOR LOW MULTIPLEX RATES

GENERAL DESCRIPTION

The PCF8566 is a peripheral device which interfaces to almost any liquid crystal display (LCD) having low multiplex rates. It generates the drive signals for any static or multiplexed LCD containing up to four backplanes and up to 24 segments and can easily be cascaded for larger LCD applications. The PCF8566 is compatible with most microprocessors/microcontrollers and communicates via a two-line bidirectional bus (I^2C). Communication overheads are minimized by a display RAM with auto-incremented addressing, by hardware subaddressing and by display memory switching (static and duplex drive modes).

Features

- Single-chip LCD controller/driver
- Selectable backplane drive configuration: static or 2/3/4 backplane multiplexing
- Selectable display bias configuration: static, 1/2 or 1/3
- Internal LCD bias generation with voltage-follower buffers
- 24 segment drives: up to twelve 8-segment numeric characters; up to six 15-segment alphanumeric characters; or any graphics of up to 96 elements
- 24 x 4-bit RAM for display data storage
- Auto-incremented display data loading across device subaddress boundaries
- Display memory bank switching in static and duplex drive modes
- Versatile blinking modes
- LCD and logic supplies may be separated
- 3 V to 6 V power supply range
- Low power consumption
- Power-saving mode for extremely low power consumption in battery-operated and telephone applications
- I^2C bus interface
- TTL/CMOS compatible
- Compatible with any 4-bit, 8-bit or 16-bit microprocessors/microcontrollers
- May be cascaded for large LCD applications (up to 1536 segments possible)
- Cascadable with the 40 segment LCD driver PFC8576
- Optimized pinning for single plane wiring in both single and multiple PCF8566 applications
- Space-saving 40-lead plastic mini-pack (VSO-40; SOT-158A)
- No external components required (even in multiple device applications)
- Manufactured in silicon gate CMOS process

Purchase of Philips' I^2C components conveys a license under the Philips' I^2C patent to use the components in the I^2C-system provided the system conforms to the I^2C specification defined by Philips.

PACKAGE OUTLINES

PCF8566T: 40-lead mini-pack; (VSO-40; SOT-158A).
PCF8566P: 40-lead DIL; plastic (SOT-129).

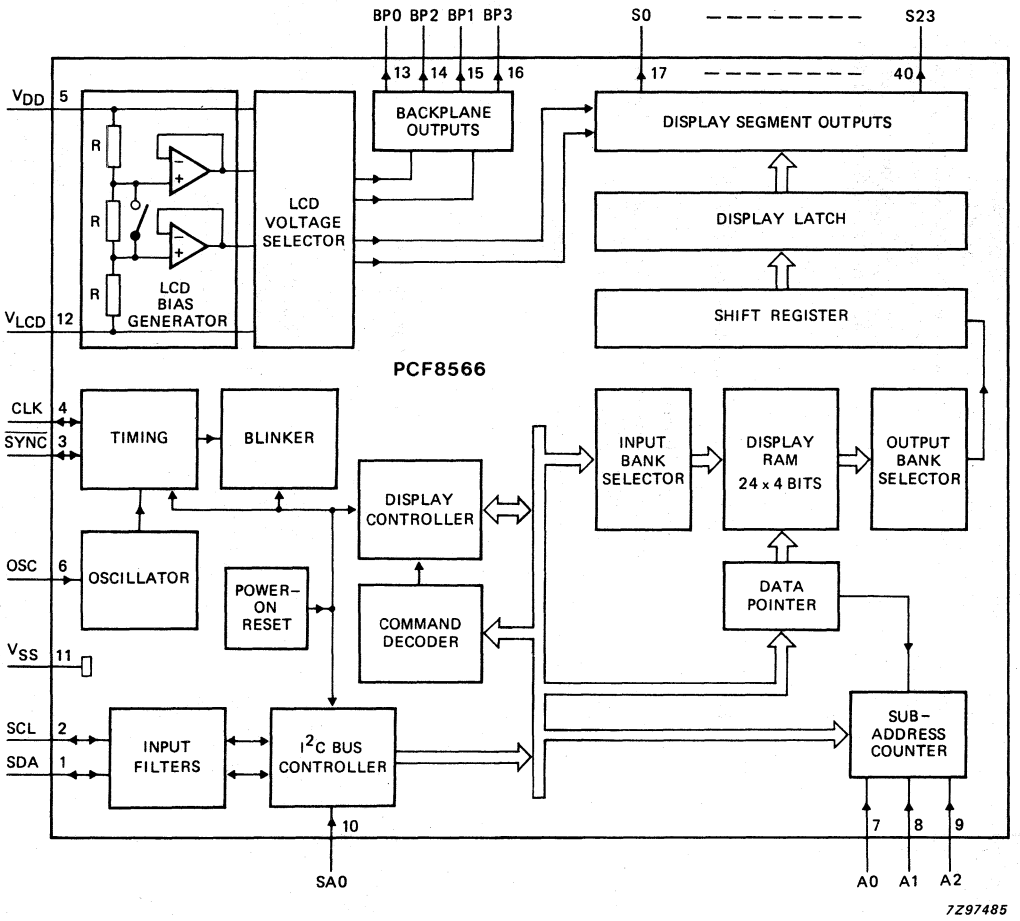


Fig. 1 Block diagram.

DEVELOPMENT DATA

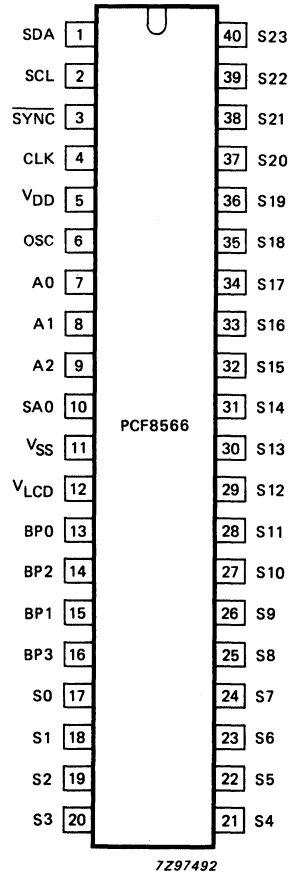


Fig. 2 Pinning diagram.

PINNING

1	SDA	I^2C bus data input/output
2	SCL	I^2C bus clock input/output
3	$\overline{SYNC}$	cascade synchronization input/output
4	CLK	external clock input/output
5	V_{DD}	positive supply voltage
6	OSC	oscillator input
7	A0	I^2C bus subaddress inputs
8	A1	I^2C bus subaddress inputs
9	A2	I^2C bus subaddress inputs
10	SA0	I^2C bus slave address bit 0 input
11	V_{SS}	logic ground
12	V_{LCD}	LCD supply voltage
13	BP0	LCD backplane outputs
14	BP2	LCD backplane outputs
15	BP1	LCD backplane outputs
16	BP3	LCD backplane outputs
17 to 40	S0 to S23	LCD segment outputs

FUNCTIONAL DESCRIPTION

The PCF8566 is a versatile peripheral device designed to interface any microprocessor to a wide variety of LCDs. It can directly drive any static or multiplexed LCD containing up to four backplanes and up to 24 segments. The display configurations possible with the PCF8566 depend on the number of active backplane outputs required; a selection of display configurations is given in Table 1.

Table 1 Selection of display configurations

active back-plane outputs	no. of segments	7-segment numeric	14-segment alphanumeric	dot matrix
4	96	12 digits + 12 indicator symbols	6 characters + 12 indicator symbols	96 dots (4 x 24)
3	72	9 digits + 9 indicator symbols	4 characters + 16 indicator symbols	72 dots (3 x 24)
2	48	6 digits + 6 indicator symbols	3 characters + 6 indicator symbols	48 dots (2 x 24)
1	24	3 digits + 3 indicator symbols	1 characters + 10 indicator symbols	24 dots

All of the display configurations given in Table 1 can be implemented in the typical system shown in Fig. 3. The host microprocessor/microcontroller maintains the two-line I^2C bus communication channel with the PCF8566. The internal oscillator is selected by tying OSC (pin 6) to V_{SS}. The appropriate biasing voltages for the multiplexed LCD waveforms are generated internally. The only other connections required to complete the system are to the power supplies (V_{DD}, V_{SS} and V_{LCD}) and to the LCD panel chosen for the application.

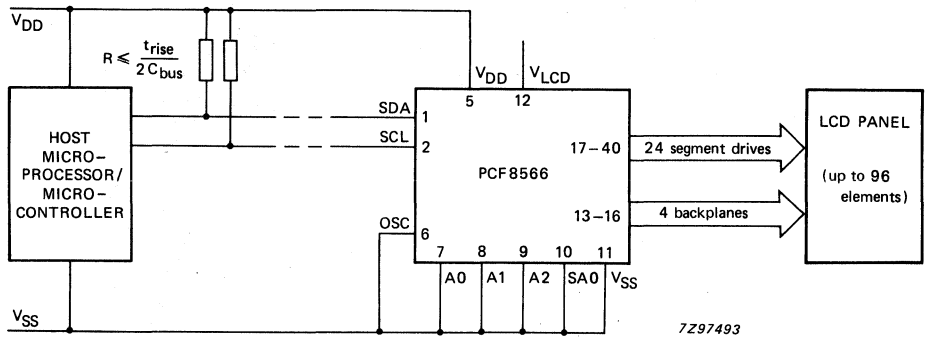


Fig. 3 Typical system configuration.

Power-on reset

At power-on the PCF8566 resets to a defined starting condition as follows:

1. All backplane outputs are set to V_{DD}.
2. All segment outputs are set to V_{DD}.
3. The drive mode '1 : 4 multiplex with 1/3 bias' is selected.
4. Blinking is switched off.
5. Input and output bank selectors are reset (as defined in Table 5).
6. The I^2C bus interface is initialized.
7. The data pointer and the subaddress counter are cleared.

Data transfers on the I^2C bus should be avoided for 1 ms following power-on to allow completion of the reset action.

LCD bias generation

The full-scale LCD voltage (V_{op}) is obtained from $V_{DD} - V_{LCD}$. The LCD voltage may be temperature compensated externally through the V_{LCD} supply to pin 12. Fractional LCD biasing voltages are obtained from an internal voltage divider of three series resistors connected between V_{DD} and V_{LCD}. The centre resistor can be switched out of circuit to provide a ½ bias voltage level for the 1 : 2 multiplex configuration.

DEVELOPMENT DATA

LCD voltage selector

The LCD voltage selector coordinates the multiplexing of the LCD according to the selected LCD drive configuration. The operation of the voltage selector is controlled by MODE SET commands from the command decoder. The biasing configurations that apply to the preferred modes of operation, together with the biasing characteristics as functions of $V_{op} = V_{DD} - V_{LCD}$ and the resulting discrimination ratios (D), are given in Table 2.

Table 2 Preferred LCD drive modes: summary of characteristics

LCD drive mode	LCD bias configuration	$\frac{V_{off(rms)}}{V_{op}}$	$\frac{V_{on\ (rms)}}{V_{op}}$	$D = \frac{V_{on(rms)}}{V_{off(rms)}}$
static (1 BP)	static (2 levels)	0	1	∞
1 : 2 MUX (2 BP)	1/2 (3 levels)	$\sqrt{2}/4 = 0{,}354$	$\sqrt{10}/4 = 0{,}791$	$\sqrt{5} = 2{,}236$
1 : 2 MUX (2 BP)	1/3 (4 levels)	$1/3 = 0{,}333$	$\sqrt{5}/3 = 0{,}745$	$\sqrt{5} = 2{,}236$
1 : 3 MUX (3 BP)	1/3 (4 levels)	$1/3 = 0{,}333$	$\sqrt{33}/9 = 0{,}638$	$\sqrt{33}/3 = 1{,}915$
1 : 4 MUX (4 BP)	1/3 (4 levels)	$1/3 = 0{,}333$	$\sqrt{3}/3 = 0{,}577$	$\sqrt{3} = 1{,}732$

LCD voltage selector (continued)

A practical value for V_{op} is determined by equating $V_{off(rms)}$ with a defined LCD threshold voltage (V_{th}), typically when the LCD exhibits approximately 10% contrast. In the static drive mode a suitable choice is $V_{op} \gtrapprox 3\,V_{th}$.

Multiplex drive ratios of 1 : 3 and 1 : 4 with 1/2 bias are possible but the discrimination and hence the contrast ratios are smaller ($\sqrt{3}$ = 1,732 for 1 : 3 multiplex or $\sqrt{21}/3$ = 1,528 for 1 : 4 multiplex). The advantage of these modes is a reduction of the LCD full scale voltage V_{op} as follows:

1 : 3 multiplex (1/2 bias) : $V_{op} = \sqrt{6}\,V_{off(rms)} = 2{,}449\,V_{off(rms)}$

1 : 4 multiplex (1/2 bias) : $V_{op} = 4\sqrt{3}/3\,V_{off(rms)} = 2{,}309\,V_{off(rms)}$

These compare with $V_{op} = 3\,V_{off(rms)}$ when 1/3 bias is used.

LCD drive mode waveforms

The static LCD drive mode is used when a single backplane is provided in the LCD. Backplane and segment drive waveforms for this mode are shown in Fig. 4.

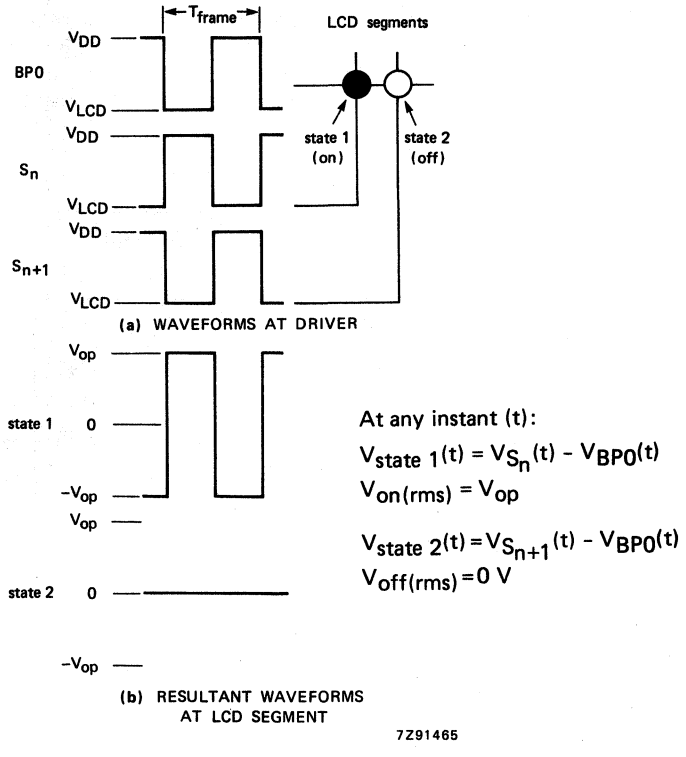


Fig. 4 Static drive mode waveforms: $V_{op} = V_{DD} - V_{LCD}$.

When two backplanes are provided in the LCD the 1 : 2 multiplex drive mode applies. The PCF8566 allows use of 1/2 or 1/3 bias in this mode as shown in Figs 5 and 6.

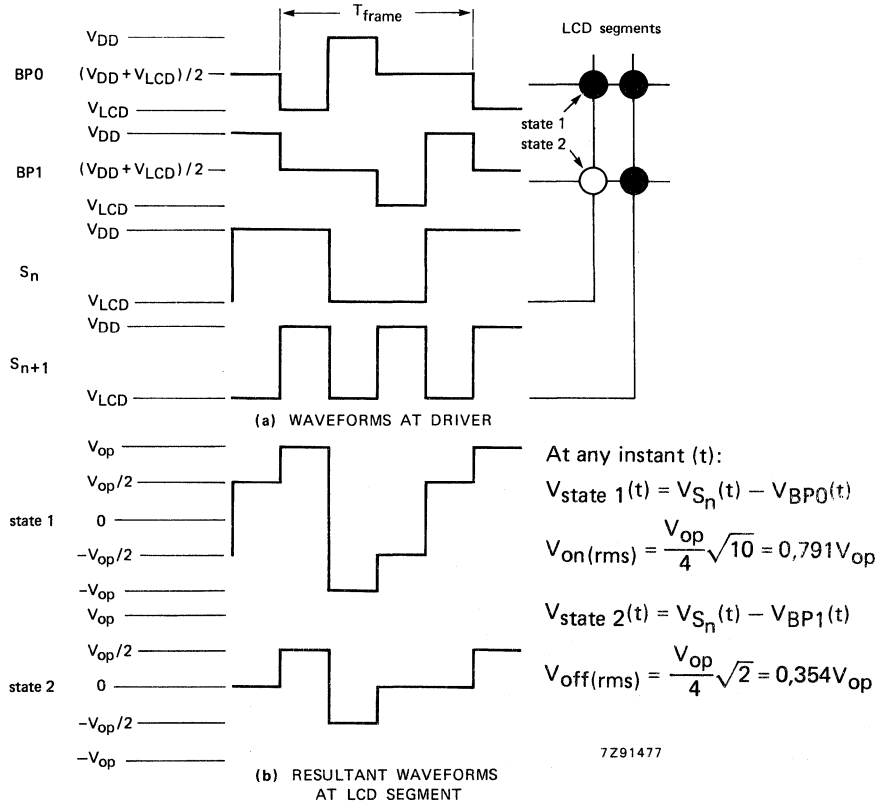


Fig. 5 Waveforms for 1 : 2 multiplex drive mode with 1/2 bias: $V_{op} = V_{DD} - V_{LCD}$.

DEVELOPMENT DATA

LCD drive mode waveforms (continued)

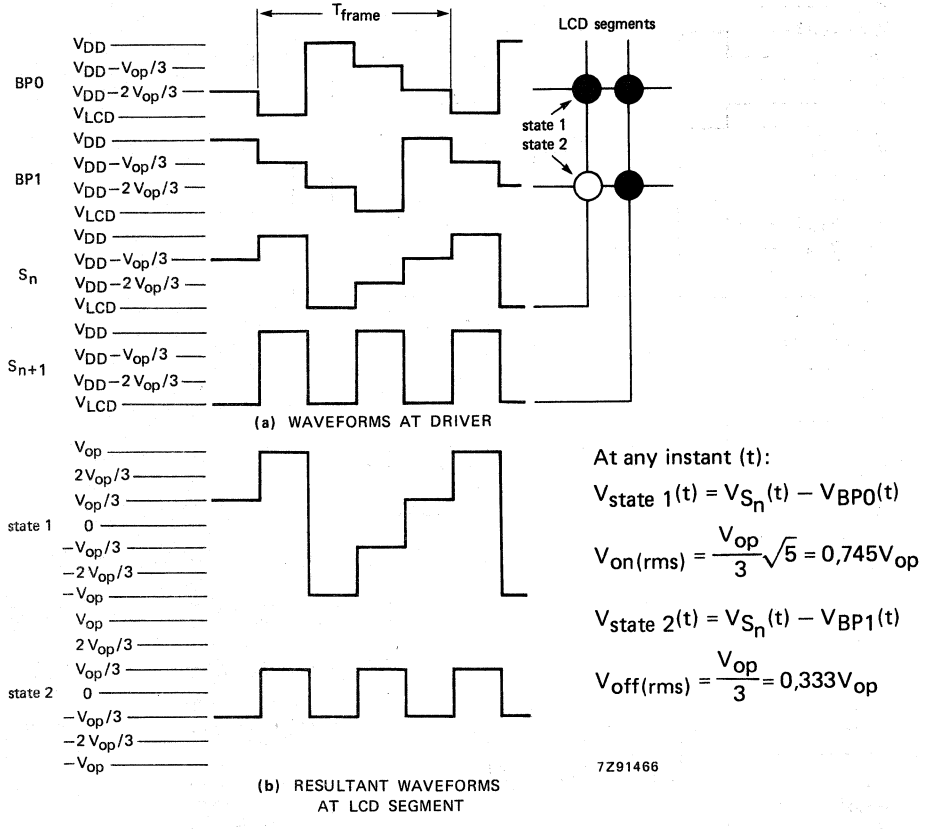


Fig. 6 Waveforms for 1 : 2 multiplex drive mode with 1/3 bias: $V_{op} = V_{DD} - V_{LCD}$.

The backplane and segment drive wavefront for the 1 : 3 multiplex drive mode (three LCD backplanes) and for the 1 : 4 multiplex drive mode (four LCD backplanes) are shown in Figs 7 and 8 respectively.

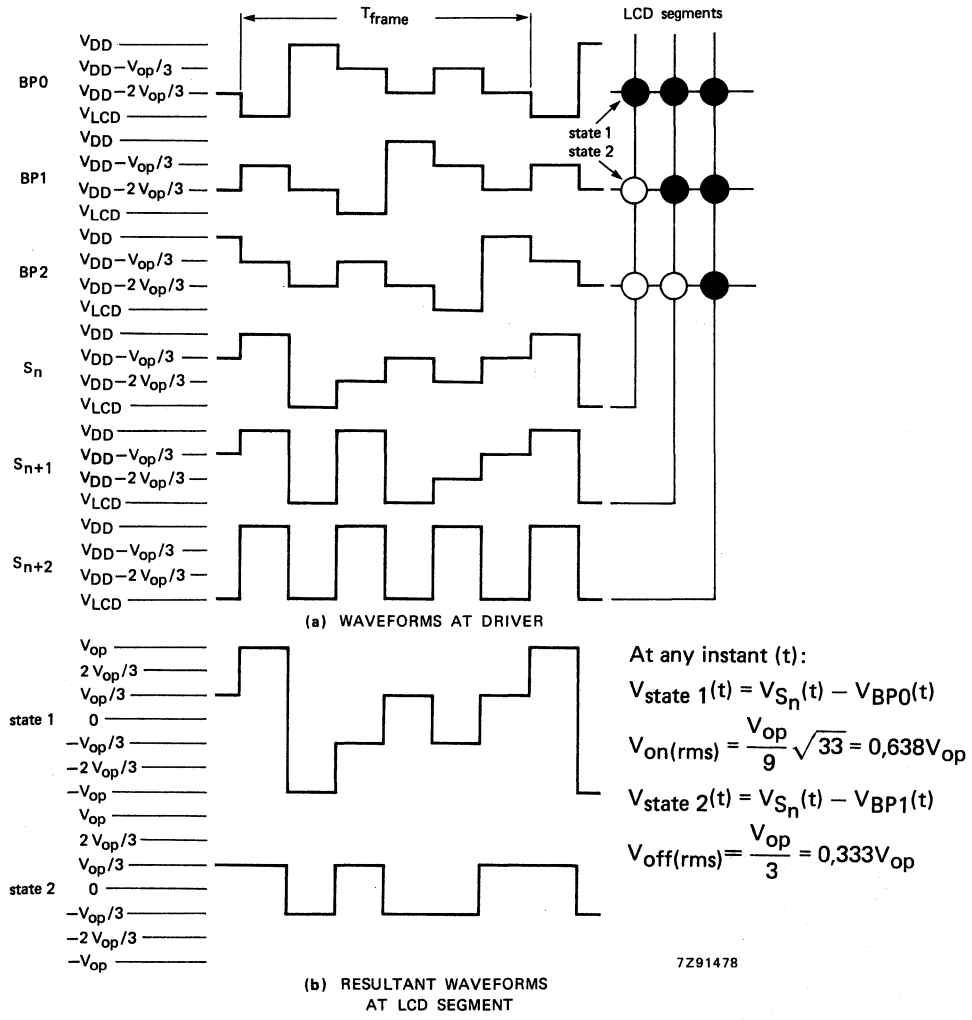


Fig. 7 Waveforms for 1 : 3 multiplex drive mode: $V_{op} = V_{DD} - V_{LCD}$.

LCD drive mode waveforms (continued)

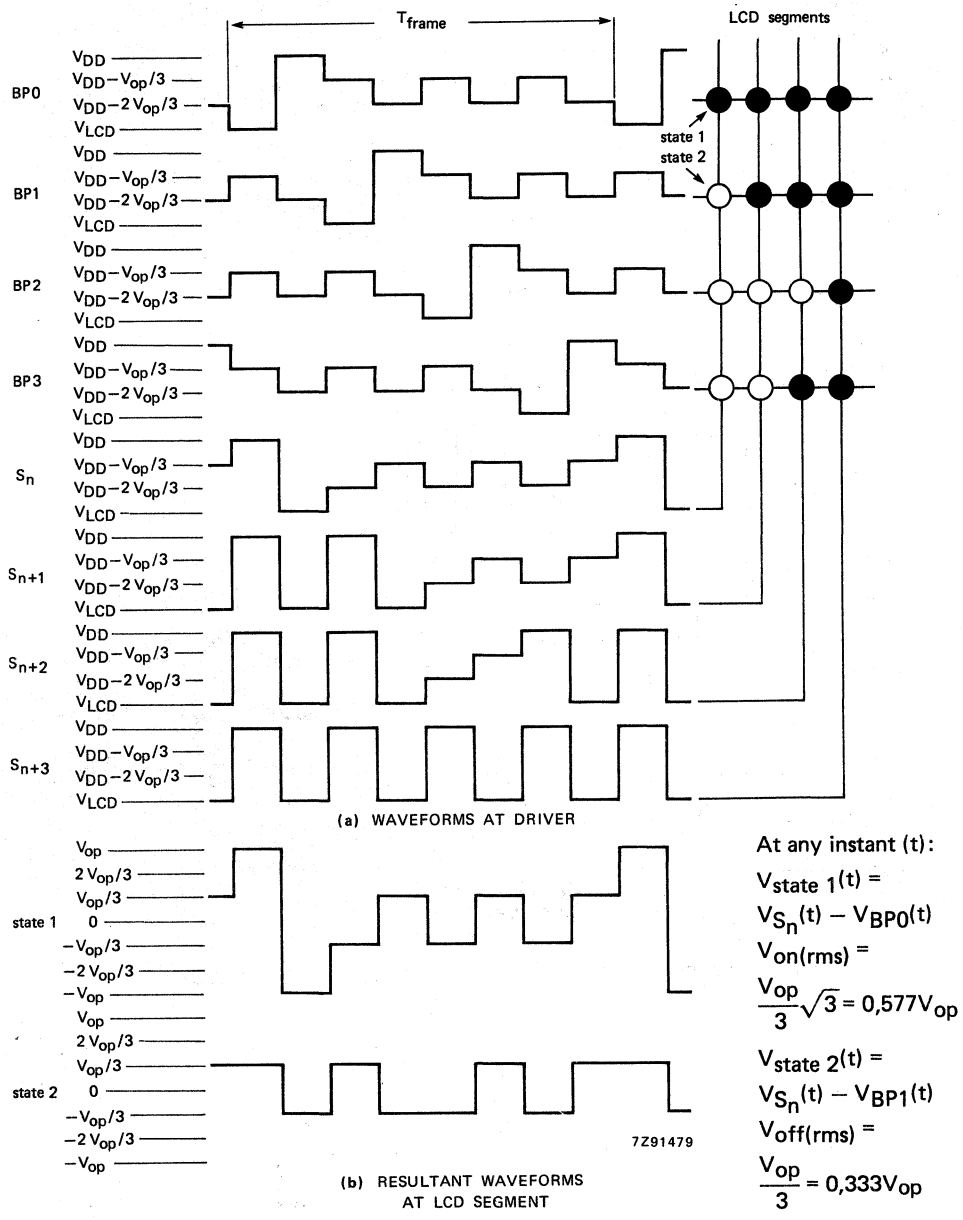


Fig. 8 Waveforms for 1 : 4 multiplex drive mode: $V_{op} = V_{DD} - V_{LCD}$.

Oscillator

The internal logic and the LCD drive signals of the PCF8566 or PCF8576 are timed either by the built-in oscillator or from an external clock.

The clock frequency (f_{CLK}) determines the LCD frame frequency and the maximum rate for data reception from the I^2C bus. To allow I^2C bus transmissions at their maximum data rate of 100 kHz, f_{CLK} should be chosen to be above 125 kHz.

A clock signal must always be supplied to the device; removing the clock may freeze the LCD in a d.c. state.

Internal clock

When the internal oscillator is used, OSC (pin 6) should be tied to V_{SS}. In this case, the output from CLK (pin 4) provides the clock signal for cascaded PCF8566s and PCF8576s in the system.

External clock

The condition for external clock is made by tying OSC (pin 6) to V_{DD}; CLK (pin 4) then becomes the external clock input.

Timing

The timing of the PCF8566 organizes the internal data flow of the device. This includes the transfer of display data from the display RAM to the display segment outputs. In cascaded applications, the synchronization signal $\overline{SYNC}$ maintains the correct timing relationship between the PCF8566s in the system. The timing also generates the LCD frame frequency which it derives as an integer multiple of the clock frequency (Table 3). The frame frequency is set by MODE SET commands when internal clock is used, or by the frequency applied to pin 4 when external clock is used.

Table 3 LCD frame frequencies

PCF8566 mode	f_{frame}	nominal f_{frame} (Hz)
normal mode	$f_{CLK}/2880$	64
power-saving mode	$f_{CLK}/480$	64

The ratio between the clock frequency and the LCD frame frequency depends on the mode in which the device is operating. In the power-saving mode the reduction ratio is six times smaller; this allows the clock frequency to be reduced by a factor of six. The reduced clock frequency results in a significant reduction in power dissipation. The lower clock frequency has the disadvantage of increasing the response time when large amounts of display data are transmitted on the I^2C bus. When a device is unable to 'digest' a display data byte before the next one arrives, it holds the SCL line low until the first display data byte is stored. This slows down the transmission rate of the I^2C bus but no data loss occurs.

Display latch

The display latch holds the display data while the corresponding multiplex signals are generated. There is a one-to-one relationship between the data in the display latch, the LCD segment outputs and one column of the display RAM.

Shift register

The shift register serves to transfer display information from the display RAM to the display latch while previous data are displayed.

Segment outputs

The LCD drive section includes 24 segment outputs S0 to S23 (pins 17 to 40) which should be connected directly to the LCD. The segment output signals are generated in accordance with the multiplexed backplane signals and with the data resident in the display latch. When less than 24 segment outputs are required the unused segment outputs should be left open.

Backplane outputs

The LCD drive section includes four backplane outputs BP0 to BP3 which should be connected directly to the LCD. The backplane output signals are generated in accordance with the selected LCD drive mode. If less than four backplane outputs are required the unused outputs can be left open. In the 1 : 3 multiplex drive mode BP3 carries the same signal as BP1, therefore these two adjacent outputs can be tied together to give enhanced drive capabilities. In the 1 : 2 multiplex drive mode BP0 and BP2, BP1 and BP3 respectively carry the same signals and may also be paired to increase the drive capabilities. In the static drive mode the same signal is carried by all four backplane outputs and they can be connected in parallel for very high drive requirements.

Display RAM

The display RAM is a static 24 x 4-bit RAM which stores LCD data. A logic 1 in the RAM bit-map indicates the 'on' state of the corresponding LCD segment; similarly, a logic 0 indicates the 'off' state. There is a one-to-one correspondence between the RAM addresses and the segment outputs, and between the individual bits of a RAM word and the backplane outputs. The first RAM column corresponds to the 24 segments operated with respect to backplane BP0 (Fig. 9). In multiplexed LCD applications the segment data of the second, third and fourth column of the display RAM are time-multiplexed with BP1, BP2 and BP3 respectively.

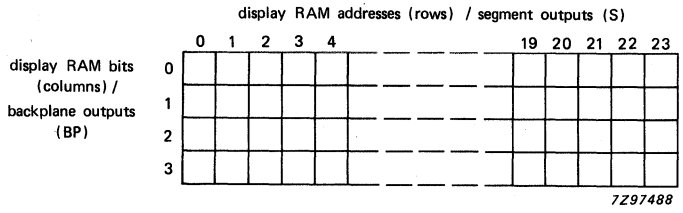


Fig. 9 Display RAM bit-map showing direct relationship between display RAM addresses and segment outputs, and between bits in a RAM word and backplane outputs.

When display data are transmitted to the PCF8566 the display bytes received are stored in the display RAM according to the selected LCD drive mode. To illustrate the filling order, an example of a 7-segment numeric display showing all drive modes is given in Fig. 10; the RAM filling organization depicted applies equally to other LCD types.

With reference to Fig. 10, in the static drive mode the eight transmitted data bits are placed in bit 0 of eight successive display RAM addresses. In the 1 : 2 multiplex drive mode the eight transmitted data bits are placed in bits 0 and 1 of four successive display RAM addresses. In the 1 : 3 multiplex drive mode these bits are placed in bits 0, 1 and 2 of three successive addresses, with bit 2 of the third address left unchanged. This last bit may, if necessary, be controlled by an additional transfer to this address but care should be taken to avoid overriding adjacent data because full bytes are always transmitted. In the 1 : 4 multiplex drive mode the eight transmitted data bits are placed in bits 0, 1, 2 and 3 of two successive display RAM addresses.

Data pointer

The addressing mechanism for the display RAM is realized using the data pointer. This allows the loading of an individual display data byte, or a series of display data bytes, into any location of the display RAM. The sequence commences with the initialization of the data pointer by the LOAD DATA POINTER command. Following this, an arriving data byte is stored starting at the display RAM address indicated by the data pointer thereby observing the filling order shown in Fig. 10. The data pointer is automatically incremented according to the LCD configuration chosen. That is, after each byte is stored, the contents of the data pointer are incremented by eight (static drive mode), by four (1 : 2 multiplex drive mode), by three (1 : 3 multiplex drive mode) or by two (1 : 4 multiplex drive mode).

Subaddress counter

The storage of display data is conditioned by the contents of the subaddress counter. Storage is allowed to take place only when the contents of the subaddress counter agree with the hardware subaddress applied to A0, A1 and A2 (pins 7, 8, and 9). A0, A1 and A2 should be tied to V_{SS} or V_{DD}. The subaddress counter value is defined by the DEVICE SELECT command. If the contents of the subaddress counter and the hardware subaddress do not agree then data storage is inhibited but the data pointer is incremented as if data storage had taken place. The subaddress counter is also incremented when the data pointer overflows.

The storage arrangements described lead to extremely efficient data loading in cascaded applications. When a series of display bytes are being sent to the display RAM, automatic wrap-over to the next PCF8566 occurs when the last RAM address is exceeded. Subaddressing across device boundaries is successful even if the change to the next device in the cascade occurs within a transmitted character.

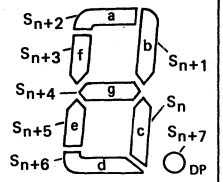
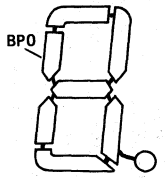
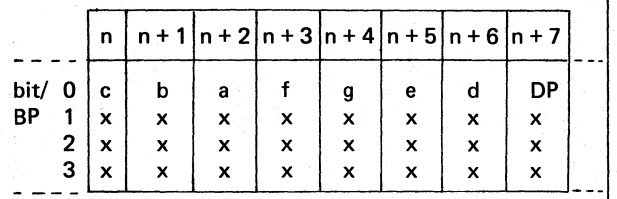
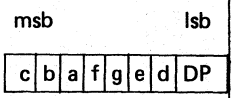
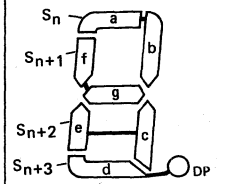
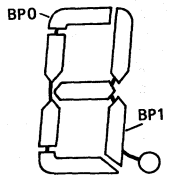
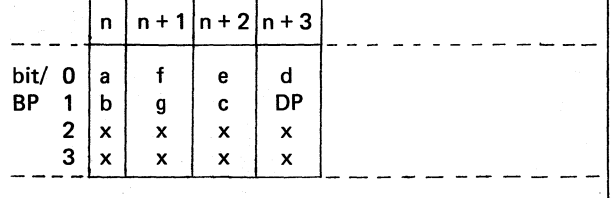
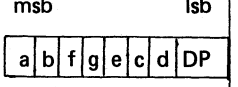
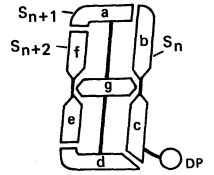
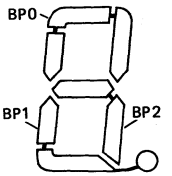
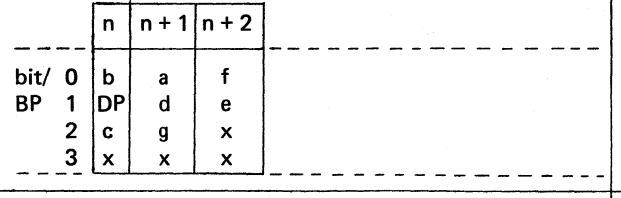
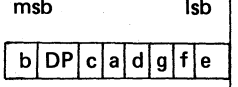
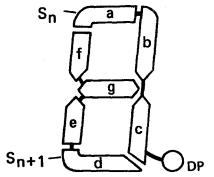
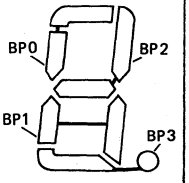
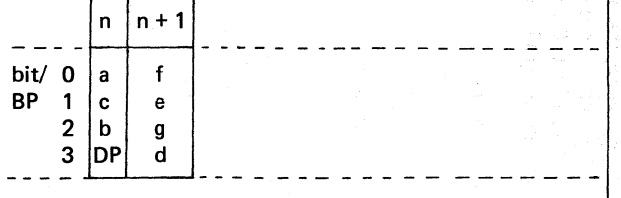
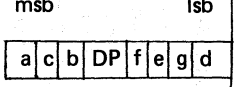
drive mode	LCD segments	LCD backplanes	display RAM filling order	transmitted display byte
static				
1 : 2 multiplex				
1 : 3 multiplex				
1 : 4 multiplex				

Fig. 10 Relationships between LCD layout, drive mode, display RAM filling order and display data transmitted over the I²C bus (x = data bit unchanged).

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Output bank selector

This selects one of the four bits per display RAM address for transfer to the display latch. The actual bit chosen depends on the particular LCD drive mode in operation and on the instant in the multiplex sequence. In 1 : 4 multiplex, all RAM addresses of bit 0 are the first to be selected, these are followed by the contents of bit 1, bit 2 and then bit 3. Similarly in 1 : 3 multiplex, bits 0, 1 and 2 are selected sequentially. In 1 : 2 multiplex, bits 0 then 1 are selected and, in the static mode, bit 0 is selected.

The PCF8566 includes a RAM bank switching feature in the static and 1 : 2 multiplex drive modes. In the static drive mode, the BANK SELECT command may request the contents of bit 2 to be selected for display instead of bit 0 contents. In the 1 : 2 drive mode, the contents of bits 2 and 3 may be selected instead of bits 0 and 1. This gives the provision for preparing display information in an alternative bank and to be able to switch to it once it is assembled.

Input bank selector

The input bank selector loads display data into the display RAM according to the selected LCD drive configuration. Display data can be loaded in bit 2 in static drive mode or in bits 2 and 3 in 1 : 2 drive mode by using the BANK SELECT command. The input bank selector functions independently of the output bank selector.

Blinker

The display blinking capabilities of the PCF8566 are very versatile. The whole display can be blinked at frequencies selected by the BLINK command. The blinking frequencies are integer multiples of the clock frequency; the ratios between the clock and blinking frequencies depend on the mode in which the device is operating, as shown in Table 4.

An additional feature is for an arbitrary selection of LCD segments to be blinked. This applies to the static and 1 : 2 LCD drive modes and can be implemented without any communication overheads. By means of the output bank selector, the displayed RAM banks are exchanged with alternate RAM banks at the blinking frequency. This mode can also be specified by the BLINK command.

In the 1 : 3 and 1 : 4 multiplex modes, where no alternate RAM bank is available, groups of LCD segments can be blinked by selectively changing the display RAM data at fixed time intervals.

If the entire display is to be blinked at a frequency other than the nominal blinking frequency, this can be effectively performed by resetting and setting the display enable bit E at the required rate using the MODE SET command.

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Table 4 Blinking frequencies

blinking mode	normal operating mode ratio	power-saving mode ratio	nominal blinking frequency f_{blink} (Hz)
off	–	–	blinking off
2 Hz	$f_{CLK}/92160$	$f_{CLK}/15360$	2
1 Hz	$f_{CLK}/184320$	$f_{CLK}/30720$	1
0,5 Hz	$f_{CLK}/368640$	$f_{CLK}/61440$	0,5

CHARACTERISTICS OF THE I²C BUS

The I²C bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals.

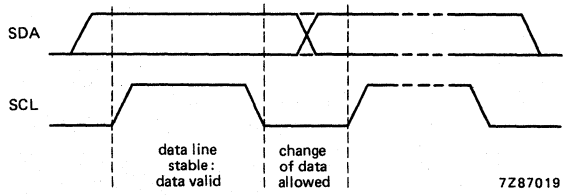


Fig. 11 Bit transfer.

Start and stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line while the clock is HIGH is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the stop condition (P).

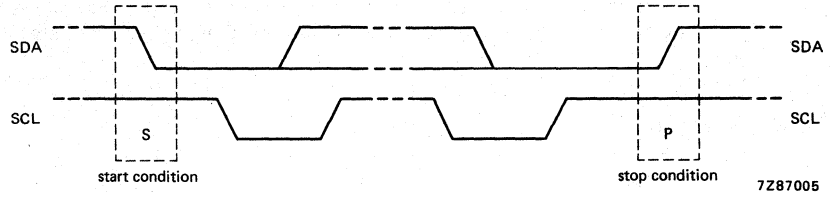


Fig. 12 Definition of start and stop conditions.

System configuration

A device generating a message is a "transmitter", a device receiving a message is a "receiver". The device that controls the message is the "master" and the devices which are controlled by the master are the "slaves".

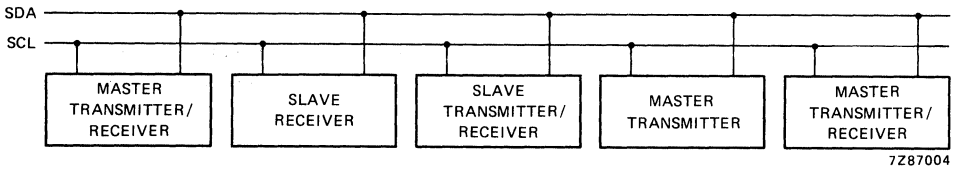


Fig. 13 System configuration.

Acknowledge

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is not limited. Each byte is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse, set up and hold times must be taken into account. A master receiver must signal an end of data to the transmitter by *not* generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

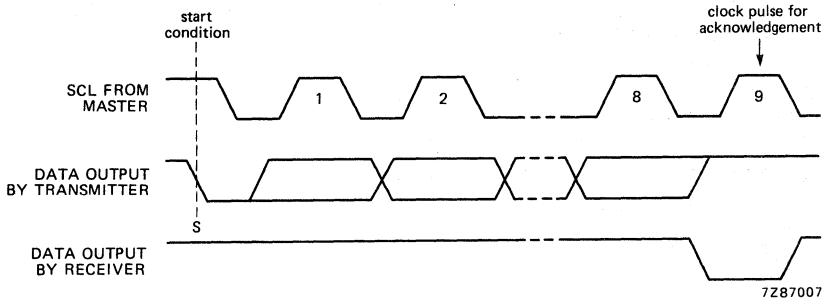


Fig. 14 Acknowledgement on the I²C bus.

Note

The general characteristics and detailed specification of the I²C bus are described in a separate data sheet (serial data buses) in handbook: ICs for digital systems in radio, audio and video equipment.

PCF8566 I²C bus controller

The PCF8566 acts as an I²C slave receiver. It does not initiate I²C bus transfers or transmit data to an I²C master receiver. The only data output from the PCF8566 are the acknowledge signals of the selected devices. Device selection depends on the I²C bus slave address, on the transferred command data and on the hardware subaddress.

In single device applications, the hardware subaddress inputs A0, A1 and A2 are normally left open or tied to V_{SS} which defines the hardware subaddress 0. In multiple device applications A0, A1 and A2 are tied to V_{SS} or V_{DD} according to a binary coding scheme such that no two devices with a common I²C slave address have the same hardware subaddress.

In the power-saving mode it is possible that the PCF8566 is not able to keep up with the highest transmission rates when large amounts of display data are transmitted. If this situation occurs, the PCF8566 forces the SCL line LOW until its internal operations are completed. This is known as the 'clock synchronization feature' of the I²C bus and serves to slow down fast transmitters. Data loss does not occur.

Input filters

To enhance noise immunity in electrically adverse environments, RC low-pass filters are provided on the SDA and SCL lines.

I²C bus protocol

Two I²C bus slave addresses (0111110 and 0111111) are reserved for PCF8566. The least-significant bit of the slave address that a PCF8566 will respond to is defined by the level tied at its input SA0 (pin 10). Therefore, two types of PCF8566 can be distinguished on the same I²C bus which allows:

(a) up to 16 PCF8566s on the same I²C bus for very large LCD applications;

(b) the use of two types of LCD multiplex on the same I²C bus.

The I²C bus protocol is shown in Fig. 15. The sequence is initiated with a start condition (S) from the I²C bus master which is followed by one of the two PCF8566 slave addresses available. All PCF8566s with the corresponding SA0 level acknowledge in parallel the slave address but all PCF8566s with the alternative SA0 level ignore the whole I²C bus transfer. After acknowledgement, one or more command bytes (m) follow which define the status of the addressed PCF8566s. The last command byte is tagged with a cleared most-significant bit, the continuation bit C. The command bytes are also acknowledged by all addressed PCF8566s on the bus.

After the last command byte, a series of display data bytes (n) may follow. These display data bytes are stored in the display RAM at the address specified by the data pointer and the subaddress counter. Both data pointer and subaddress counter are automatically updated and the data are directed to the intended PCF8566 device. The acknowledgement after each byte is made only by the (A0, A1, A2) addressed PCF8566. After the last display byte, the I²C bus master issues a stop condition (P).

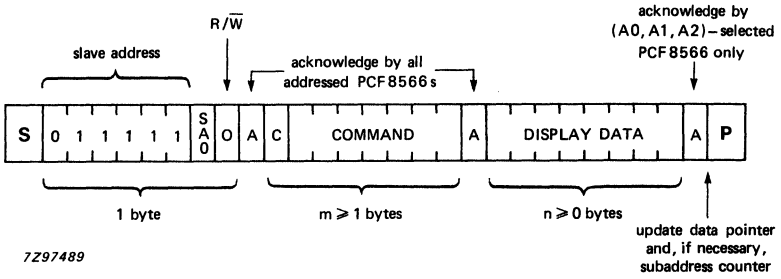


Fig. 15 I²C bus protocol.

Command decoder

The command decoder identifies command bytes that arrive on the I²C bus. All available commands carry a continuation bit C in their most-significant bit position (Fig. 16). When this bit is set, it indicates that the next byte of the transfer to arrive will also represent a command. If the bit is reset, it indicates the last command byte of the transfer. Further bytes will be regarded as display data.

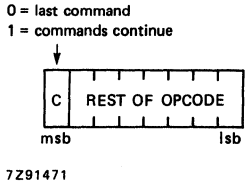


Fig. 16 General format of command byte.

The five commands available to the PCF8566 are defined in Table 5.

Command decoder (continued)

Table 5 Definition of PCF8566 commands

command/opcode	options	description
MODE SET C 1 0 LP E B M1 M0	LCD drive mode: bits M1 M0 static (1 BP): 0 1 1 : 2 MUX (2 BP): 1 0 1 : 3 MUX (3 BP): 1 1 1 : 4 MUX (4 BP): 0 0	Defines LCD drive mode
	LCD bias: bit B 1/3 bias: 0 1/2 bias: 1	Defines LCD bias configuration
	display status: bit E disabled (blank): 0 enabled: 1	Defines display status The possibility to disable the display allows implementation of blinking under external control
	mode: bit LP normal mode: 0 power-saving mode: 1	Defines power dissipation mode
LOAD DATA POINTER C 0 0 P4 P3 P2 P1 P0	bits P4 P3 P2 P1 P0 5-bit binary value of 0 to 23	Five bits of immediate data, bits P4 to P0, are transferred to the data pointer to define one of twenty-four display RAM addresses
DEVICE SELECT C 1 1 0 0 A2 A1 A0	bits A0 A1 A2 3-bit binary value of 0 to 7	Three bits of immediate data, bits A0 to A2, are transferred to the subaddress counter to define one of eight hardware subaddresses

<table>
<tr><th>command/opcode</th><th>options</th><th>description</th></tr>
<tr><td>BANK SELECT
<table><tr><td>C</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>I</td><td>O</td></tr></table></td><td><table><tr><td>static</td><td>1 : 2 MUX</td><td>bit I</td></tr><tr><td>RAM bit 0
RAM bit 2</td><td>RAM bits 0, 1
RAM bits 2, 3</td><td>0
1</td></tr></table><table><tr><td>static</td><td>1 : 2 MUX</td><td>bit O</td></tr><tr><td>RAM bit 0
RAM bit 2</td><td>RAM bits 0, 1
RAM bits 2, 3</td><td>0
1</td></tr></table></td><td>Defines input bank selection (storage of arriving display data)

Defines output bank selection (retrieval of LCD display data)

The BANK SELECT command has no effect in 1 : 3 and 1 : 4 multiplex drive modes</td></tr>
<tr><td>BLINK
<table><tr><td>C</td><td>1</td><td>1</td><td>1</td><td>0</td><td>A</td><td>BF1</td><td>BF0</td></tr></table></td><td><table><tr><td>blink frequency</td><td>bits BF1</td><td>BF0</td></tr><tr><td>off
2 Hz
1 Hz
0,5 Hz</td><td>0
0
1
1</td><td>0
1
0
1</td></tr></table><table><tr><td>blink mode</td><td>bit A</td></tr><tr><td>normal blinking
alternation blinking</td><td>0
1</td></tr></table></td><td>Defines the blinking frequency

Selects the blinking mode; normal operation with frequency set by bits BF1, BF0, or blinking by alternation of display RAM banks. Alternation blinking does not apply in 1 : 3 and 1 : 4 multiplex drive modes</td></tr>
</table>

Display controller

The display controller executes the commands identified by the command decoder. It contains the status registers of the PCF8566 and coordinates their effects. The controller is also responsible for loading display data into the display RAM as required by the filling order.

Cascaded operation

In large display configurations, up to 16 PCF8566s can be distinguished on the same I²C bus by using the 3-bit hardware subaddress (A0, A1, A2) and the programmable I²C slave address (SA0). It is also possible to cascade up to 16 PCF8566s. When cascaded, several PCF8566s are synchronized so that they can share the backplane signals from one of the devices in the cascade. Such an arrangement is cost-effective in large LCD applications since the backplane outputs of only one device need to be through-plated to the backplane electrodes of the display. The other PCF8566s of the cascade contribute additional segment outputs but their backplane outputs are left open (Fig. 17).

The $\overline{\text{SYNC}}$ line is provided to maintain the correct synchronization between all cascaded PCF8566s. This synchronization is guaranteed after the power-on reset. The only time that $\overline{\text{SYNC}}$ is likely to be needed is if synchronization is accidently lost (e.g. by noise in adverse electrical environments; or by the definition of a multiplex mode when PCF8566s with differing SA0 levels are cascaded). $\overline{\text{SYNC}}$ is organized as an input/output pin; the output section being realized as an open-drain driver with an internal pull-up resistor. A PCF8566 asserts the $\overline{\text{SYNC}}$ line at the onset of its last active backplane signal and monitors the $\overline{\text{SYNC}}$ line at all other times. Should synchronization in the cascade be lost, it will be restored by the first PCF8566 to assert $\overline{\text{SYNC}}$. The timing relationships between the backplane waveforms and the $\overline{\text{SYNC}}$ signal for the various drive modes of the PCF8576 are shown in Fig. 18. The waveforms are identical with the parent device PCF8576. Casadability between PCF8566s and PCF8576s is possible, giving cost effective LCD applications.

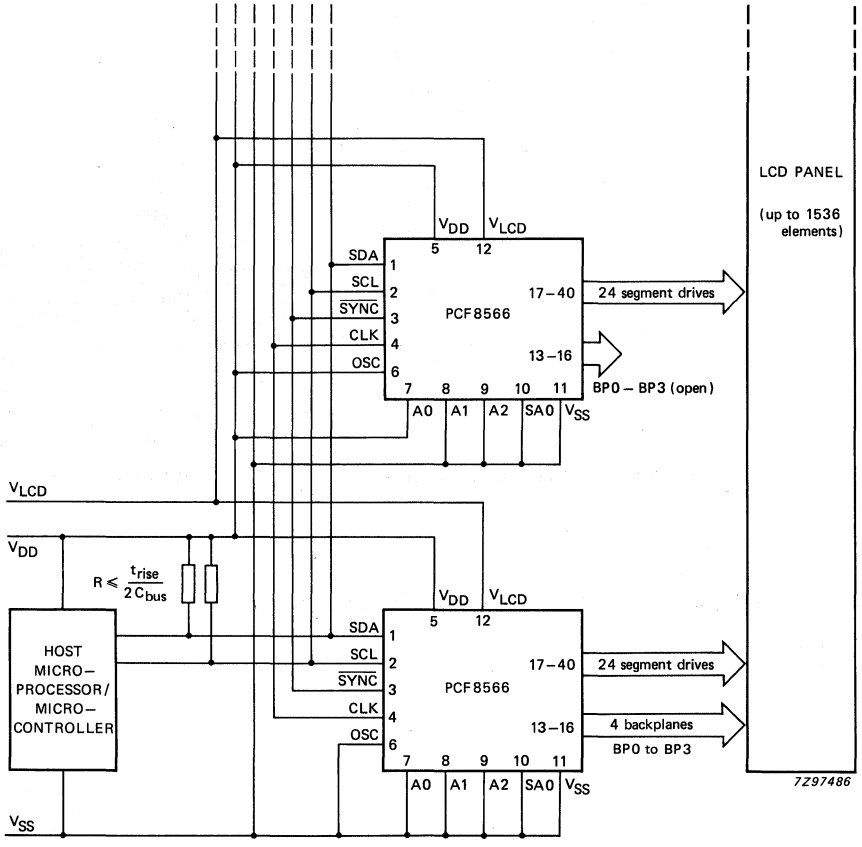


Fig. 17 Cascaded PCF8566 configuration.

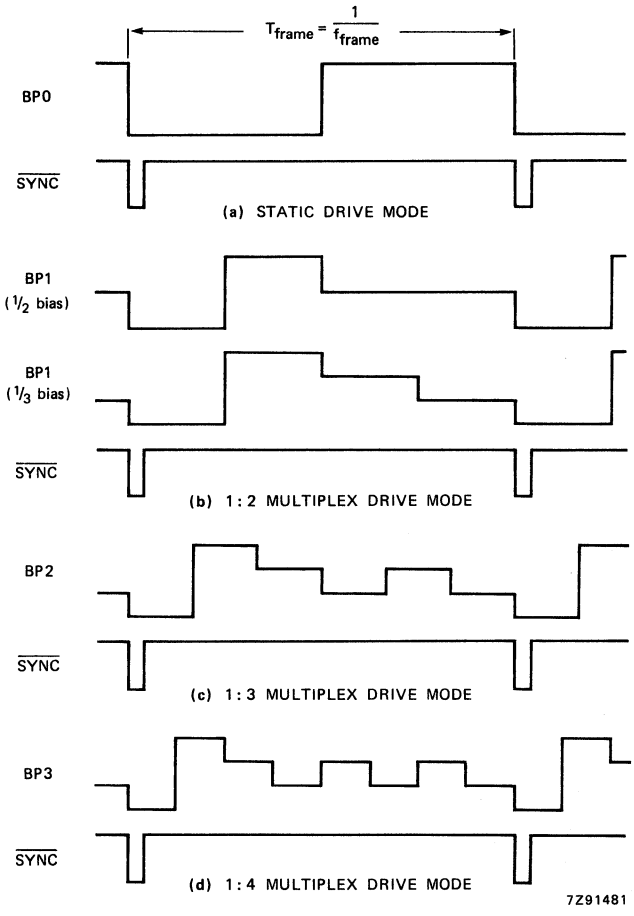


Fig. 18 Synchronization of the cascade for the various PCF8566 drive modes.

For single plane wiring of PCF8566s, see section "APPLICATION INFORMATION".

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range; see note	V_{DD}		−0,5 to + 7 V
LCD supply voltage range	V_{LCD}		V_{DD} −7 to V_{DD} V
Input voltage range (SCL; SDA; A0 to A2; OSC; CLK; $\overline{SYNC}$; SA0)	V_I		V_{SS} −0,5 to V_{DD} + 0,5 V
Output voltage range (S0 to S23; BP0 to BP3)	V_O		V_{LCD} −0,5 to V_{DD} + 0,5 V
D.C. input current	$\pm I_I$	max.	20 mA
D.C. output current	$\pm I_O$	max.	25 mA
V_{DD}, V_{SS} or V_{LCD} current	$\pm I_{DD}$, $\pm I_{SS}$, $\pm I_{LCD}$	max.	50 mA
Power dissipation per package	P_{tot}	max.	400 mW
Power dissipation per output	P_O	max.	100 mW
Storage temperature range	T_{stg}		−65 to + 150 °C

Note

Inputs and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is advised to take handling precautions appropriate to handling MOS devices (see 'Handling MOS devices').

D.C. CHARACTERISTICS

V_{SS} = 0 V; V_{DD} = 3 to 6 V; V_{LCD} = V_{DD} −3 to V_{DD} −6 V;

T_{amb} = −40 to +85 °C; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Operating supply voltage	V_{DD}	3	–	6	V
LCD supply voltage	V_{LCD}	V_{DD} −6	–	V_{DD} −3	V
Operating supply current (normal mode) at f_{CLK} = 200 kHz (note 1)	I_{DD}	–	–	180	μA
Power-saving mode supply current at V_{DD} = 3,5 V; V_{LCD} = 0 V; f_{CLK} = 35 kHz; A0, A1 and A2 tied to V_{SS} (note 1)	I_{LP}	–	–	60	μA

DEVELOPMENT DATA

parameter	symbol	min.	typ.	max.	unit
Logic					
Input voltage LOW	V_{IL}	V_{SS}	–	$0,3\ V_{DD}$	V
Input voltage HIGH	V_{IH}	$0,7\ V_{DD}$	–	V_{DD}	V
Output voltage LOW at I_O = 0 mA	V_{OL}	–	–	0,05	V
Output voltage HIGH at I_O = 0 mA	V_{OH}	V_{DD} –0,05	–	–	V
Output current LOW (CLK, $\overline{SYNC}$) at V_{OL} = 1,0 V; V_{DD} = 5 V	I_{OL1}	1	–	–	mA
Output current HIGH (CLK) at V_{OH} = 4,0 V; V_{DD} = 5 V	I_{OH}	–	–	–1	mA
Output current LOW (SDA; SCL) at V_{OL} = 0,4 V; V_{DD} = 5 V	I_{OL2}	3	–	–	mA
Leakage current (SAO, CLK, OSC, A0, A1, A2, SCL, SDA) at $V_I = V_{SS}$ or V_{DD}	$\pm I_L$	–	–	1	μA
Pull-up resistor ($\overline{SYNC}$)	R_{SYNC}	15	25	60	kΩ
Power-on reset level (note 2)	V_{REF}	–	1,3	1,8	V
Tolerable spike width on bus	t_{sw}	–	–	100	ns
Input capacitance (note 3)	C_I	–	–	7	pF
LCD outputs					
D.C. voltage component (BP0 to BP3) at C_{BP} = 35 nF	$\pm V_{BP}$	–	20	–	mV
D.C. voltage component (S0 to S23) at C_S = 5 nF	$\pm V_S$	–	20	–	mV
Output impedance (BP0 to BP3) at $V_{LCD} = V_{DD}$ –5 V (note 4)	R_{BP}	–	–	5	kΩ
Output impedance (S0 to S23) at $V_{LCD} = V_{DD}$ –5 V (note 4)	R_S	–	–	7,0	kΩ

A.C. CHARACTERISTICS (note 5)

V_{SS} = 0 V; V_{DD} = 3 to 6 V; V_{LCD} = V_{DD} −3 to V_{DD} −6 V;
T_{amb} = −40 to +85 °C; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Oscillator frequency (normal mode) (note 6)	f_{CLK}	125	200	315	kHz
Oscillator frequency (power-saving mode) at V_{DD} = 3,5 V	f_{CLKLP}	21	31	48	kHz
CLK HIGH time	t_{CLKH}	1	–	–	μs
CLK LOW time	t_{CLKL}	1	–	–	μs
$\overline{SYNC}$ propagation delay	t_{PSYNC}	–	–	400	ns
$\overline{SYNC}$ LOW time	t_{SYNCL}	1	–	–	μs
Driver delays with test loads at V_{LCD} = V_{DD} −5 V	t_{PLCD}	–	–	30	μs
I²C bus					
Bus free time	t_{BUF}	4,7	–	–	μs
Start condition hold time	$t_{HD;STA}$	4	–	–	μs
SCL LOW time	t_{LOW}	4,7	–	–	μs
SCL HIGH time	t_{HIGH}	4	–	–	μs
Start condition set-up time (repeated start code only)	$t_{SU;STA}$	4,7	–	–	μs
Data hold time	$t_{HD;DAT}$	0	–	–	μs
Data set-up time	$t_{SU;DAT}$	250	–	–	ns
Rise time	t_R	–	–	1	μs
Fall time	t_F	–	–	300	ns
Stop condition set-up time	$t_{SU;STO}$	4,7	–	–	μs

Notes to characteristics

1. Outputs open; inputs at V_{SS} or V_{DD}; external clock with 50% duty factor; I²C bus inactive.
2. Resets all logic when $V_{DD} < V_{REF}$.
3. Periodically sampled, not 100% tested.
4. Outputs measured one at a time.
5. All timing values referred to V_{IH} and V_{IL} levels with an input voltage swing of V_{SS} to V_{DD}.
6. At $f_{CLK} < 125$ kHz, I²C bus maximum transmission speed is derated.

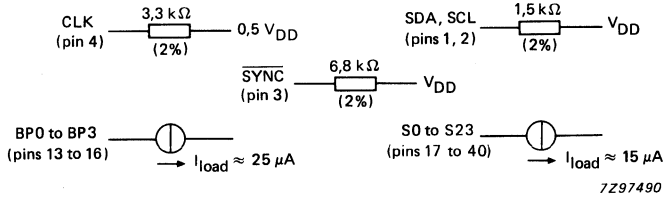


Fig. 19 Test loads.

DEVELOPMENT DATA

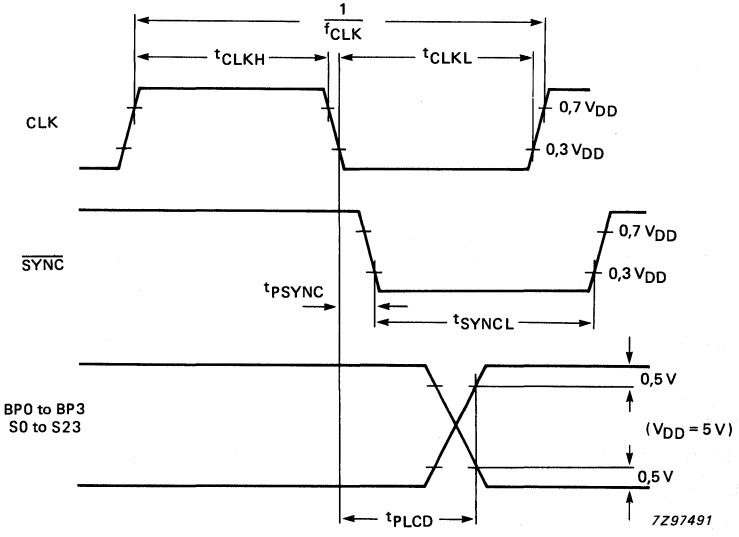


Fig. 20 Driver timing waveforms.

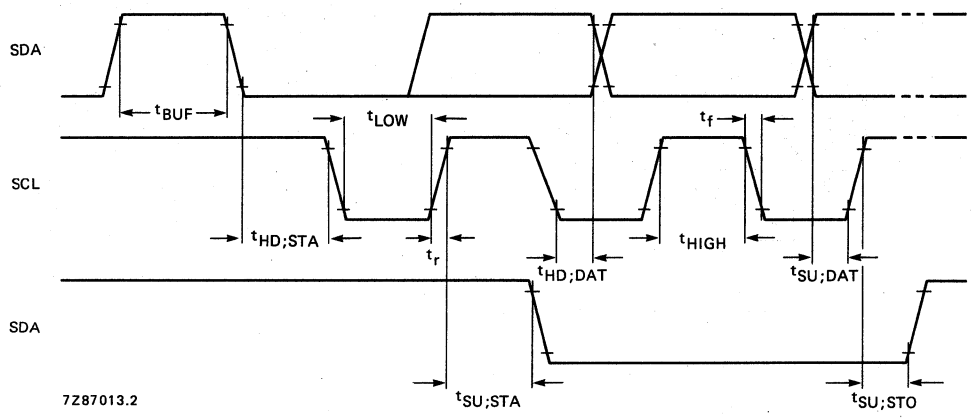
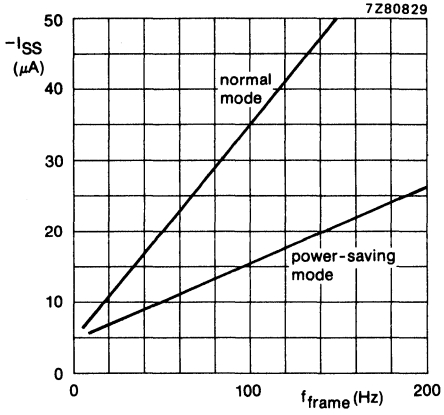
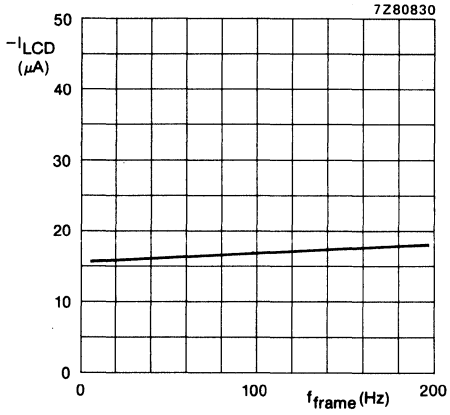


Fig. 21 I^2C bus timing waveforms.

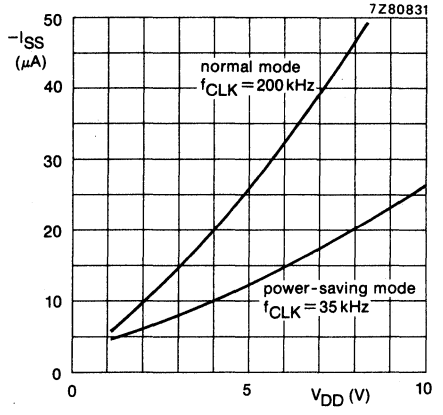
DEVELOPMENT DATA



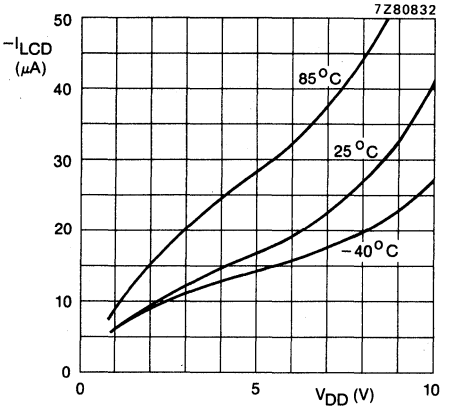
(a) V_{DD} = 5 V; V_{LCD} = 0 V; T_{amb} = 25 °C.



(b) V_{DD} = 5 V; V_{LCD} = 0 V; T_{amb} = 25 °C.

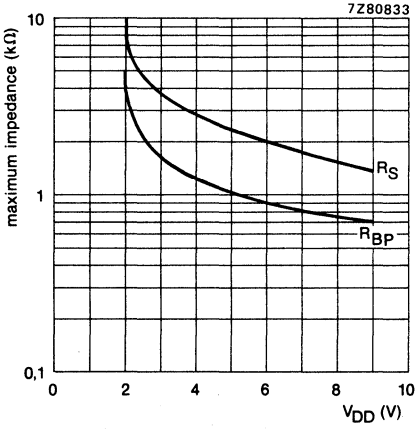


(c) V_{LCD} = 0 V; external clock; T_{amb} = −40 to + 85 °C.

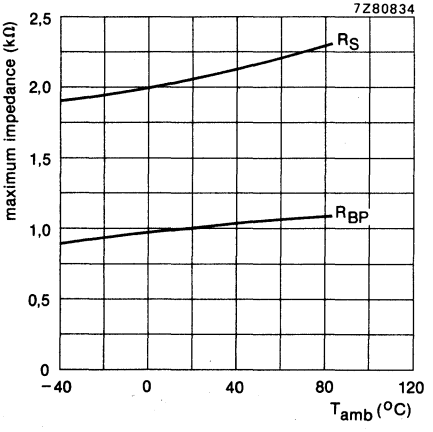


(d) V_{LCD} = 0 V; external clock; f_{CLK} = nominal frequency.

Fig. 22 Typical supply current characteristics.



(a) V_{LCD} = 0 V; T_{amb} = 25 °C.



(b) V_{DD} = 5 V; V_{LCD} = 0 V.

Fig. 23 Typical characteristics of LCD outputs.

APPLICATION INFORMATION

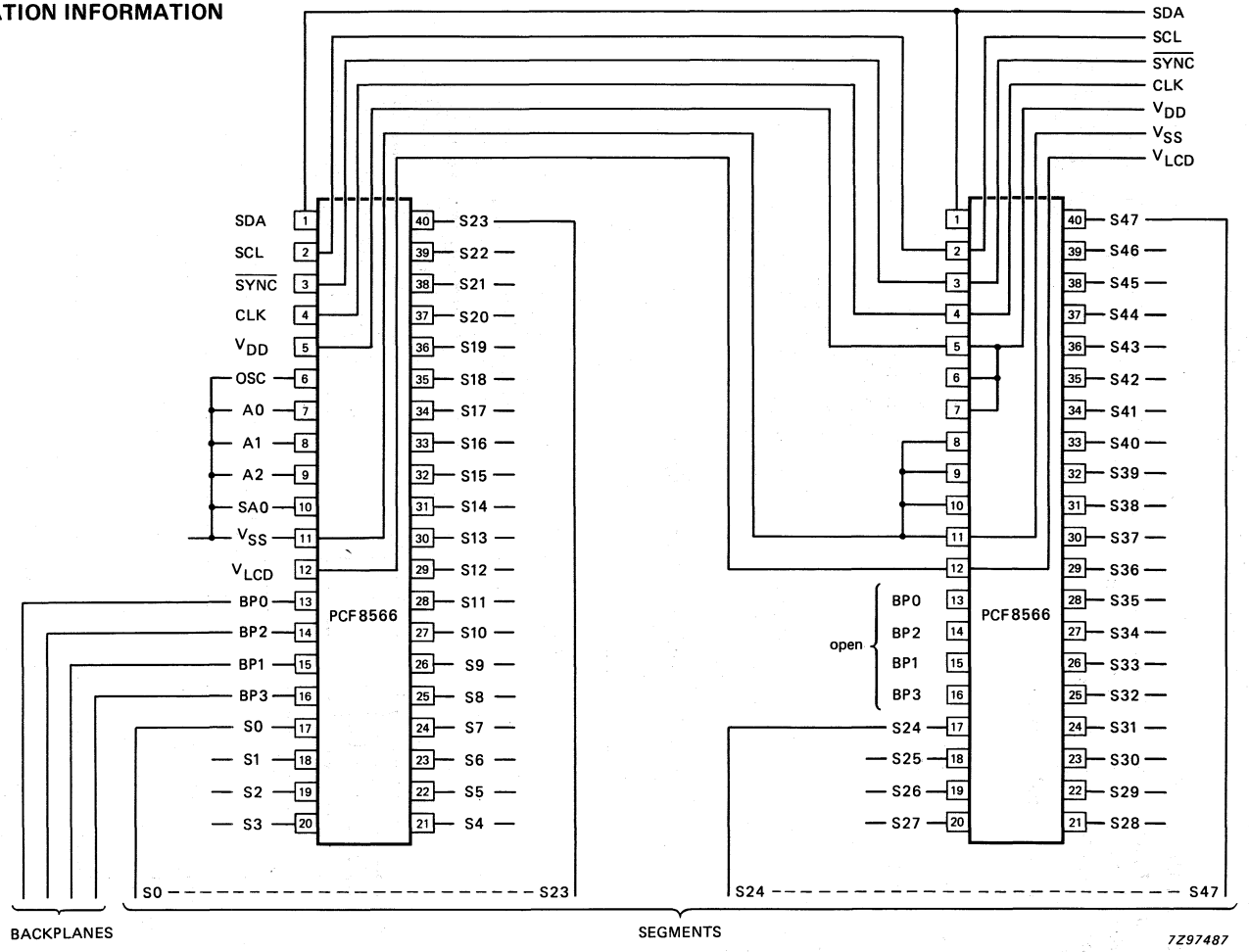


Fig. 24 Single plane wiring of packaged PCF8566s.

256 x 8-BIT STATIC RAM

GENERAL DESCRIPTION

The PCF8570 is a low power 2048-bit static CMOS RAM organized as 256 words by 8-bits. Addresses and data are transferred serially via a two-line bidirectional bus (I^2C). The built-in word address register is incremented automatically after each written or read data byte. Three address pins A0, A1, A2 are used for programming the hardware address, allowing the use of up to eight devices connected to the bus without additional hardware.

Features

- Operating supply voltage 2,5 V to 6 V
- Low data retention voltage min. 1,0 V
- Low standby current max. 15 μA
- Power saving mode typ. 50 nA
- Serial input/output bus (I^2C)
- Address by 3 hardware address pins
- Automatic word address incrementing
- 8-lead DIL package

Applications

- Telephony
- Radio and television
- Video cassette recorder
- General purpose

RAM expansion for stored numbers in repertory dialling (e.g. PCD3343 applications)
channel presets

RAM expansion for the microcontroller families MAB8400 and PCF84C00

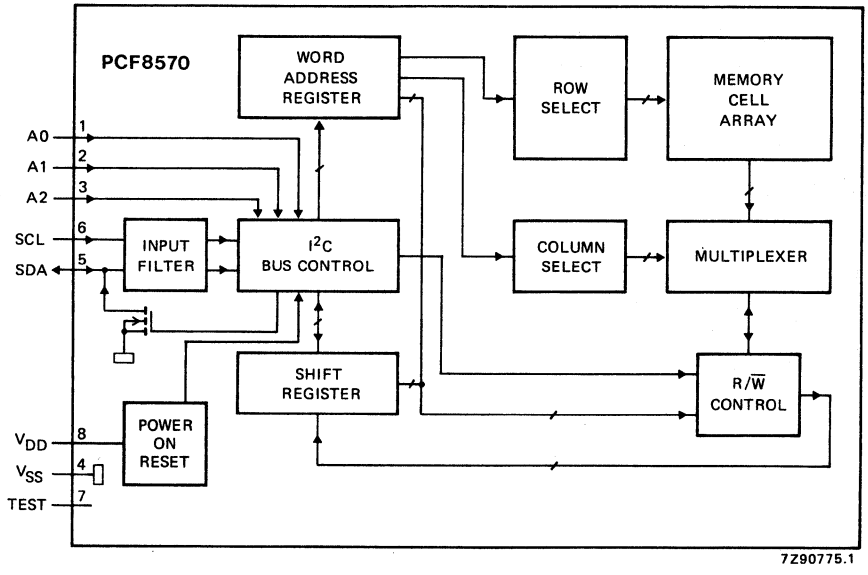


Fig. 1 Block diagram.

PACKAGE OUTLINES

PCF8570P: 8-lead DIL; plastic (SOT-97AE).
PCF8570T: 8-lead mini-pack plastic (SO-8L; SOT-176).

PINNING

1 to 3	A0 to A2	address inputs	
4	V_{SS}	negative supply	
5	SDA	serial data line	I^2C bus
6	SCL	serial clock line	I^2C bus
7	TEST	test input for test speed-up; must be connected to V_{SS} when not in use (power saving mode, see Figs 14 and 15)	
8	V_{DD}	positive supply	

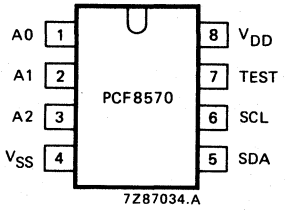


Fig. 2 Pinning diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range (pin 8)	V_{DD}		−0,8 to + 8,0	V
Voltage range on any input	V_I		−0,8 to V_{DD} + 0,8	V
D.C. input current (any input)	$\pm I_I$	max.	10	mA
D.C. output current (any output)	$\pm I_O$	max.	10	mA
Supply current (pin 4 or pin 8)	$\pm I_{DD}$; I_{SS}	max.	50	mA
Power dissipation per package	P_{tot}	max.	300	mW
Power dissipation per output	P	max.	50	mW
Storage temperature range	T_{stg}		−65 to + 150	°C
Operating ambient temperature range	T_{amb}		−40 to + 85	°C

CHARACTERISTICS

V_{DD} = 2,5 to 6 V; V_{SS} = 0 V; T_{amb} = −40 to + 85 °C unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply					
Supply voltage	V_{DD}	2,5	–	6	V
Supply current at $V_I = V_{SS}$ or V_{DD}					
operating at f_{SCL} = 100 kHz	I_{DD}	–	–	200	μA
standby at f_{SCL} = 0 Hz	I_{DDO}	–	–	15	μA
standby at T_{amb} = −25 to + 70 °C	I_{DDO}	–	–	5	μA
Power-on reset voltage level*	V_{POR}	1,5	1,9	2,3	V
Inputs; input/output SDA					
Input voltage LOW**	V_{IL}	−0,8	–	0,3 x V_{DD}	V
Input voltage HIGH**	V_{IH}	0,7 x V_{DD}	–	V_{DD} + 0,8	V
Output current LOW at V_{OL} = 0,4 V	I_{OL}	3	–	–	mA
Output leakage current HIGH at $V_{OH} = V_{DD}$	I_{OH}	–	–	250	nA
Input leakage current at $V_I = V_{DD}$ or V_{SS}	$\pm I_I$	–	–	250	nA
Clock frequency (Fig. 7)	f_{SCL}	0	–	100	kHz
Input capacitance (SCL, SDA) at $V_I = V_{SS}$	C_I	–	–	7	pF
Tolerable spike width on bus	t_{SW}	–	–	100	ns
LOW V_{DD} data retention					
Supply voltage for data retention	V_{DDR}	1	–	6	V
Supply current at V_{DDR} = 1 V	I_{DDR}	–	–	5	μA
Supply current at V_{DDR} = 1 V; T_{amb} = −25 to + 70 °C	I_{DDR}	–	–	2	μA
Power saving mode (Figs 14 and 15)					
Supply current at T_{amb} = 25 °C; TEST = V_{DDR}	I_{DDR}	–	50	400	nA

* The power-on reset circuit resets the I^2C bus logic when $V_{DD} < V_{POR}$.

** If the input voltages are a diode voltage above or below the supply voltage V_{DD} or V_{SS} an input current will flow; this current must not exceed ± 0,5 mA.

CHARACTERISTICS OF THE I²C BUS

The I²C bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals.

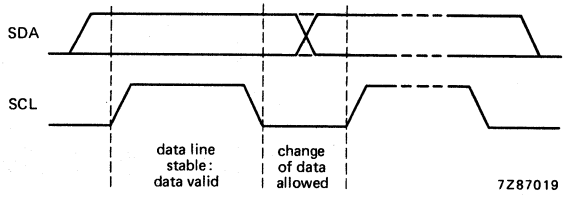


Fig. 3 Bit transfer.

Start and stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the stop condition (P).

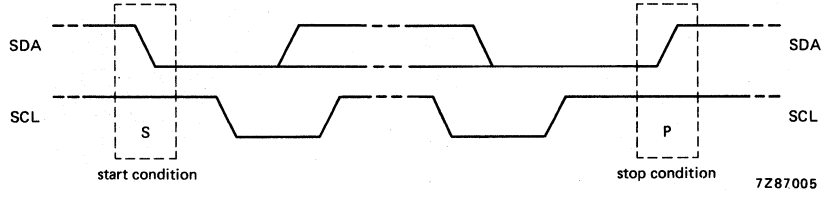


Fig. 4 Definition of start and stop conditions.

System configuration

A device generating a message is a "transmitter", a device receiving a message is the "receiver". The device that controls the message is the "master" and the devices which are controlled by the master are the "slaves".

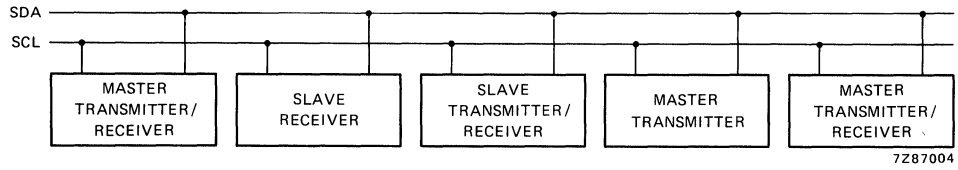


Fig. 5 System configuration.

Acknowledge

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse, set-up and hold times must be taken into account. A master receiver must signal an end of data to the transmitter by *not* generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

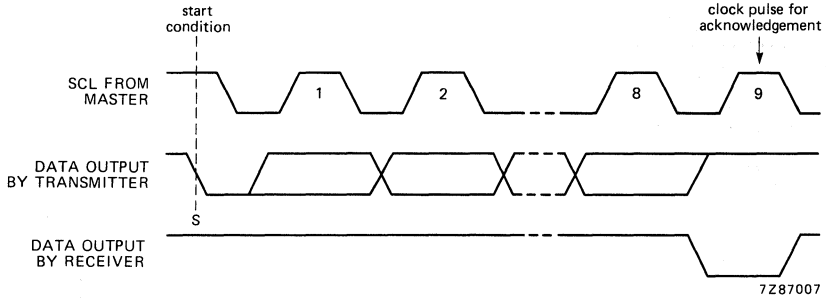


Fig. 6 Acknowledgement on the I^2C bus.

Timing specifications

Within the I²C bus specifications a high-speed mode and a low-speed mode are defined. The device operates in both modes and the timing requirements are as follows:

High-speed mode

Masters generate a bus clock with a maximum frequency of 100 kHz. Detailed timing is shown in Fig. 7.

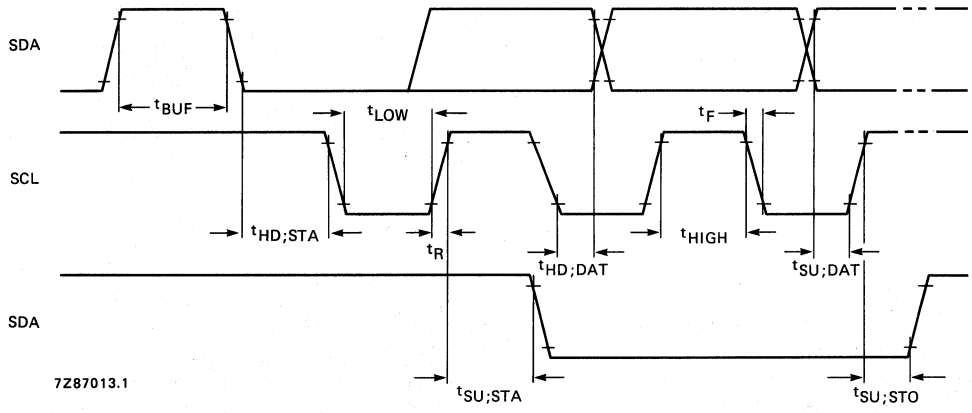


Fig. 7 Timing of the high-speed mode.

Where:

t_{BUF}	$t \geqslant t_{LOWmin}$	The minimum time the bus must be free before a new transmission can start
$t_{HD;STA}$	$t \geqslant t_{HIGHmin}$	Start condition hold time
t_{LOWmin}	4,7 μs	Clock LOW period
$t_{HIGHmin}$	4 μs	Clock HIGH period
$t_{SU;STA}$	$t \geqslant t_{LOWmin}$	Start condition set-up time, only valid for repeated start code
$t_{HD;DAT}$	$t \geqslant 0$ μs	Data hold time
$t_{SU;DAT}$	$t \geqslant 250$ ns	Data set-up time
t_R	$t \leqslant 1$ μs	Rise time of both the SDA and SCL line
t_F	$t \leqslant 300$ ns	Fall time of both the SDA and SCL line
$t_{SU;STO}$	$t \geqslant t_{LOWmin}$	Stop condition set-up time

Note

All the timing values refer to V_{IH} and V_{IL} levels with a voltage swing of V_{SS} to V_{DD}.

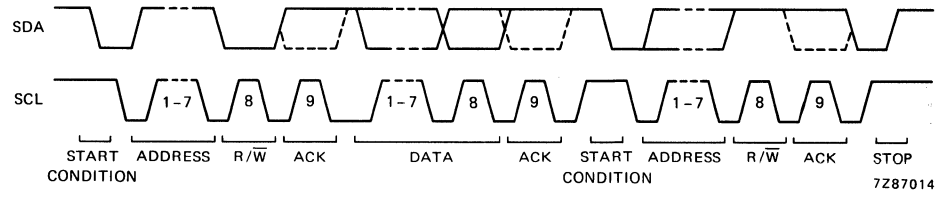


Fig. 8 Complete data transfer in the high-speed mode.

Where:

Clock t_{LOWmin}	4,7 μs
$t_{HIGHmin}$	4 μs
The dashed line is the acknowledgement of the receiver	
Mark-to-space ratio	1 : 1 (LOW-to-HIGH)
Max. number of bytes	unrestricted
Premature termination of transfer	allowed by generation of STOP condition
Acknowledge clock bit	must be provided by the master

Low-speed mode

Masters generate a bus clock with a maximum frequency of 2 kHz; a minimum LOW period of 105 μs and a minimum HIGH period of 365 μs. The mark-to-space ratio is 1 : 3 LOW-to-HIGH. Detailed timing is shown in Fig. 9.

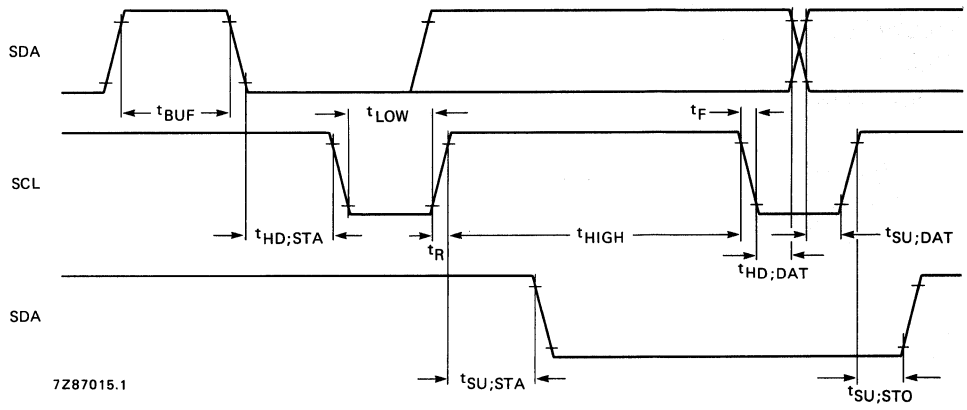


Fig. 9 Timing of the low-speed mode.

Timing specifications (continued)

Where:

t_{BUF}	$t \geqslant 105\ \mu s$ (t_{LOWmin})
$t_{HD;STA}$	$t \geqslant 365\ \mu s$ ($t_{HIGHmin}$)
t_{LOW}	$130\ \mu s \pm 25\ \mu s$
t_{HIGH}	$390\ \mu s \pm 25\ \mu s$
$t_{SU;STA}$	$130\ \mu s \pm 25\ \mu s$ *
$t_{HD;DAT}$	$t \geqslant 0\ \mu s$
$t_{SU;DAT}$	$t \geqslant 250$ ns
t_R	$t \leqslant 1\ \mu s$
t_F	$t \leqslant 300$ ns
$t_{SU;STO}$	$130\ \mu s \pm 25\ \mu s$

Note

All the timing values refer to V_{IH} and V_{IL} levels with a voltage swing of V_{SS} to V_{DD}. For definitions see high-speed mode.

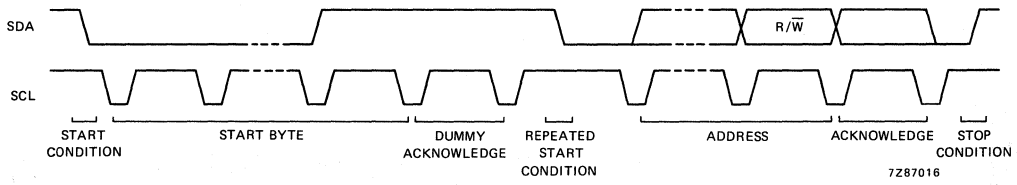


Fig. 10 Complete data transfer in the low-speed mode.

Where:

Clock t_{LOWmin}	$130\ \mu s \pm 25\ \mu s$
$t_{HIGHmin}$	$390\ \mu s \pm 25\ \mu s$
Mark-to-space ratio	1 : 3 (LOW-to-HIGH)
Start byte	0000 0001
Max. number of bytes	6
Premature termination of transfer	not allowed
Acknowledge clock bit	must be provided by master

Note

The general characteristics and detailed specification of the I^2C bus are described in a separate data sheet (serial data buses) in handbook "ICs for digital systems in radio, audio and video equipment".

* Only valid for repeated start code.

Bus protocol

Before any data is transmitted on the I²C bus, the device which should respond is addressed first. The addressing is always done with the first byte transmitted after the start procedure. The I²C bus configuration for different PCF8570 READ and WRITE cycles is shown in Fig. 11.

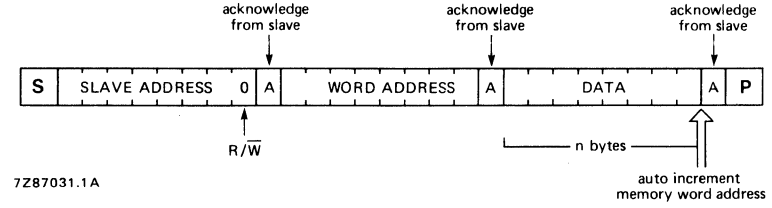


Fig. 11(a) Master transmits to slave receiver (WRITE mode).

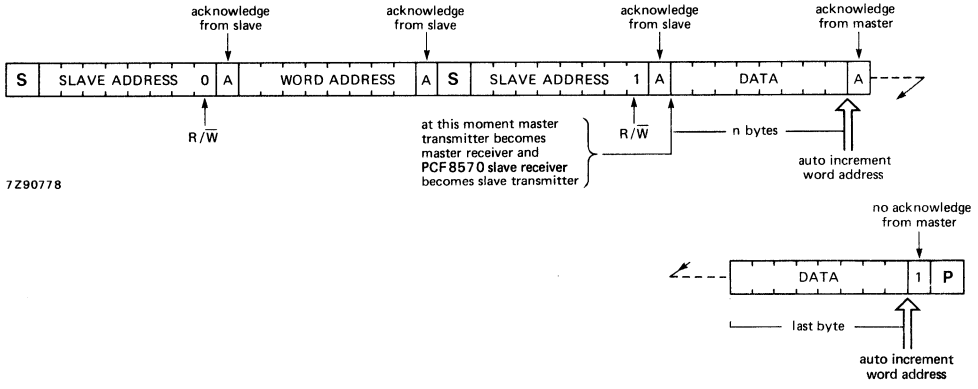


Fig. 11(b) Master reads after setting word address (WRITE word address; READ data).

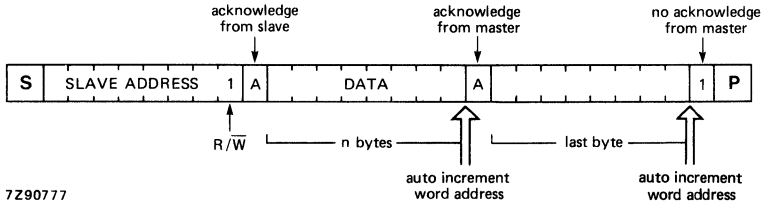


Fig. 11(c) Master reads slave immediately after first byte (READ mode).

APPLICATION INFORMATION

The PCF8570 slave address has a fixed combination 1010 as group 1, while group 2 is fully programmable (see Fig. 12).

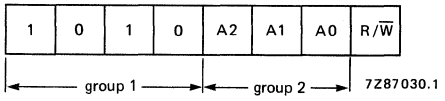


Fig. 12 PCF8570 address.

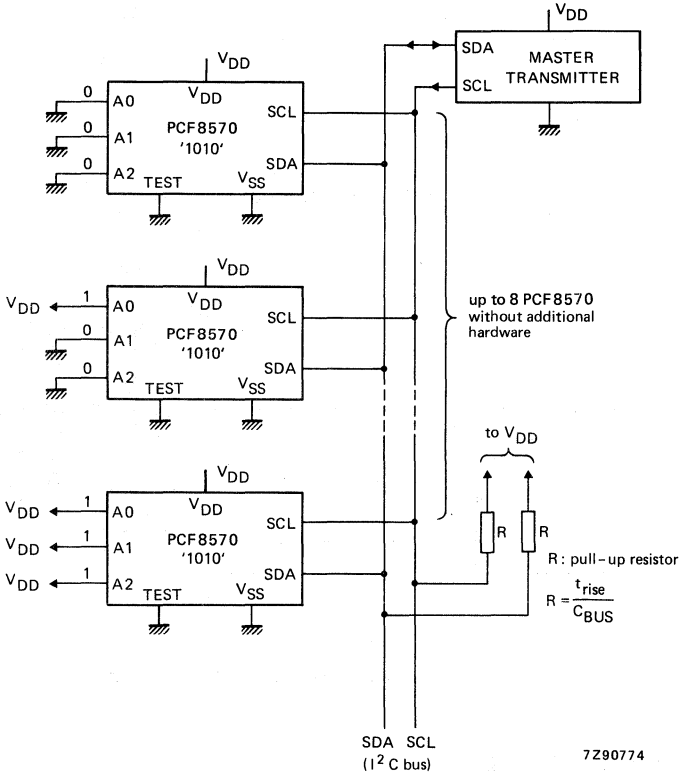


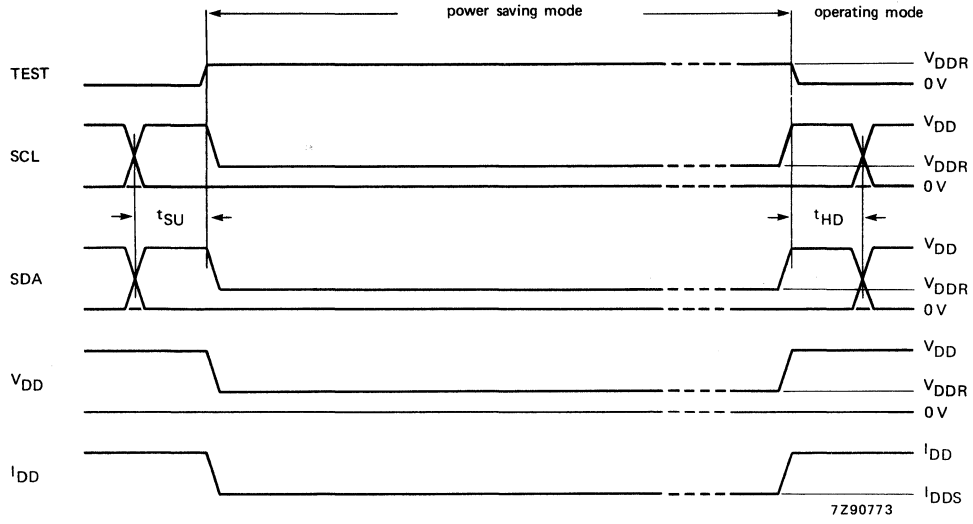
Fig. 13 PCF8570 application diagram.

Note

A0, A1, and A2 inputs must be connected to V_{DD} or V_{SS} but not left open.

POWER SAVING MODE

With the condition TEST = V_{DDR}, the PCF8570 goes into the power saving mode and the I^2C bus logic is reset.



Where:
$t_{SU} \geqslant 4\ \mu s$
$t_{HD} \geqslant 4\ \mu s$

Fig. 14 Timing for power saving mode.

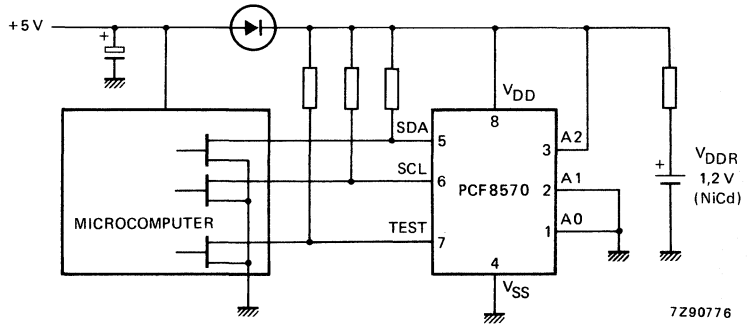
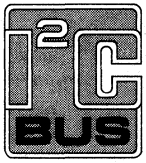


Fig. 15 Application example for power saving mode.

Note to Fig. 15

1. In the operating mode, TEST = 0.
2. In the power saving mode, TEST = V_{DDR}.



Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specification defined by Philips.

128 x 8-BIT STATIC RAM

GENERAL DESCRIPTION

The PCF8571 is a low power 1024-bit static CMOS RAM organized as 128 words by 8-bits. Addresses and data are transferred serially via a two-line bidirectional bus (I^2C). The built-in word address register is incremented automatically after each written or read data byte. Three address pins A0, A1, A2 are used for programming the hardware address, allowing the use of up to eight devices connected to the bus without additional hardware.

Features

- Operating supply voltage 2,5 V to 6 V
- Low data retention voltage min. 1,0 V
- Low standby current max. 5 μA
- Power saving mode typ. 50 nA
- Serial input/output bus (I^2C)
- Address by 3 hardware address pins
- Automatic word address incrementing
- 8-lead DIL package

Applications

- Telephony — RAM expansion for stored numbers in repertory dialling (e.g. PCD3340 applications)
- Radio and television — channel presets
- Video cassette recorder
- General purpose — RAM expansion for the microcomputer families MAB8400 and PCF84C00

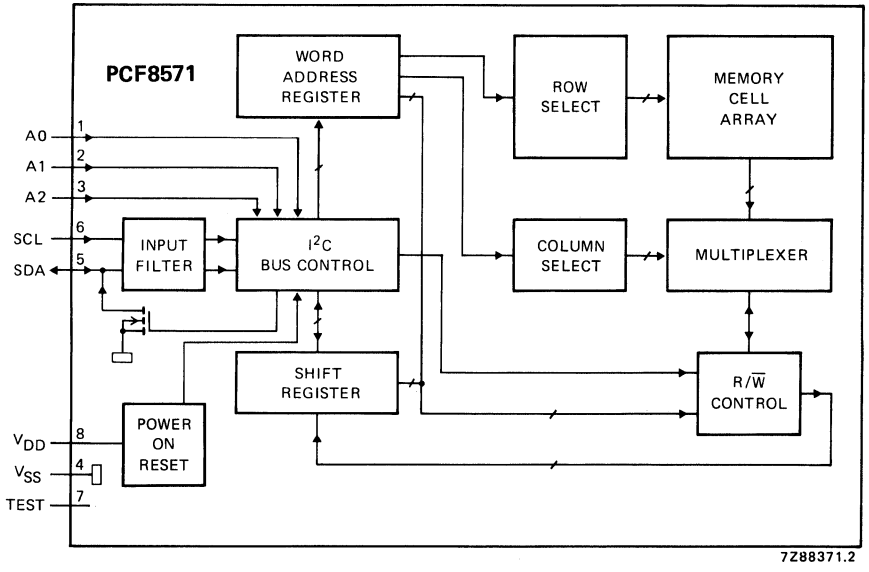


Fig. 1 Block diagram.

PACKAGE OUTLINES

PCF8571P : 8-lead DIL; plastic (SOT-97AE).
PCF8571T : 8-lead mini-pack (SO-8L; SOT-176).

PINNING

1 to 3	A0 to A2	address inputs
4	V_{SS}	negative supply
5	SDA	serial data line } I^2C bus
6	SCL	serial clock line } I^2C bus
7	TEST	test input for test speed-up; must be connected to V_{SS} when not in use (power saving mode, see Fig. 14 and 15)
8	V_{DD}	positive supply

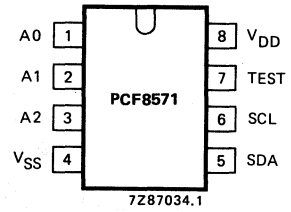


Fig. 2 Pinning diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range (pin 8)	V_{DD}		−0,8 to + 8,0 V
Voltage range on any input	V_I		−0,8 to V_{DD} + 0,8 V
D.C. input current (any input)	$\pm I_I$	max.	10 mA
D.C. output current (any output)	$\pm I_O$	max.	10 mA
Supply current (pin 4 or pin 8)	$\pm I_{DD}; I_{SS}$	max.	50 mA
Power dissipation per package	P_{tot}	max.	300 mW
Power dissipation per output	P	max.	50 mW
Storage temperature range	T_{stg}		−65 to + 150 °C
Operating temperature range	T_{amb}		−40 to + 85 °C

CHARACTERISTICS

V_{DD} = 2,5 to 6 V; V_{SS} = 0 V; T_{amb} = −40 to + 85 °C unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
SUPPLY					
Supply voltage	V_{DD}	2,5	–	6	V
Supply current					
$V_I = V_{SS}$ or V_{DD}					
operating at f_{SCL} = 100 kHz;	I_{DD}	–	–	200	μA
standby at f_{SCL} = 0 Hz	I_{DDO}	–	–	15	μA
standby at T_{amb} = −25 to 70 °C	I_{DDO}	–	–	5	μA
Power-on reset voltage level at $V_{SCL} = V_{SDA} = V_{DD}$	V_{POR}	1,5	1,9	2,3	V
Inputs; input/output SDA					
Input voltage LOW**	V_{IL}	−0,8	–	0,3 x V_{DD}	V
Input voltage HIGH**	V_{IH}	0,7 x V_{DD}	–	V_{DD} + 0,8	V
Output current LOW at V_{OL} = 0,4 V	I_{OL}	3	–	–	mA
Output leakage current HIGH at $V_{OH} = V_{DD}$	I_{OH}	–	–	250	nA
Input leakage current at $V_I = V_{DD}$ or V_{SS}	$\pm I_I$	–	–	250	nA
Clock frequency (Fig. 7)	f_{SCL}	0	–	100	kHz
Input capacitance (SCL, SDA) at $V_I = V_{SS}$	C_I	–	–	7	pF
Tolerable spike width on bus	t_{SW}	–	–	100	ns
LOW V_{DD} data retention					
Supply voltage for data retention	V_{DDR}	1	–	6	V
Supply current at V_{DDR} = 1 V	I_{DDR}	–	–	5	μA
Supply current at V_{DDR} = 1 V; T_{amb} = −25 to 70 °C	I_{DDR}	–	–	2	μA
Power saving mode (Fig. 14)					
Supply current at T_{amb} = 25 °C; TEST = V_{DDR}	I_{DDS}	–	50	200	nA

* The power-on reset circuit resets the I^2C bus logic when $V_{DD} < V_{POR}$.

** If the input voltages are a diode voltage above or below the supply voltage V_{DD} or V_{SS} an input current will flow: this current must not exceed ± 0,5 mA.

CHARACTERISTICS OF THE I²C BUS

The I²C bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals.

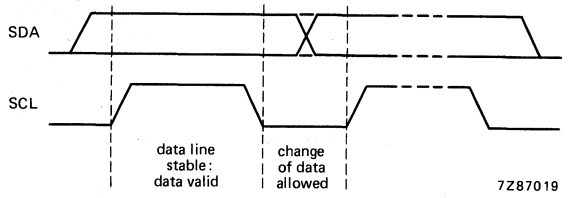


Fig. 3 Bit transfer.

Start and stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the stop condition (P).

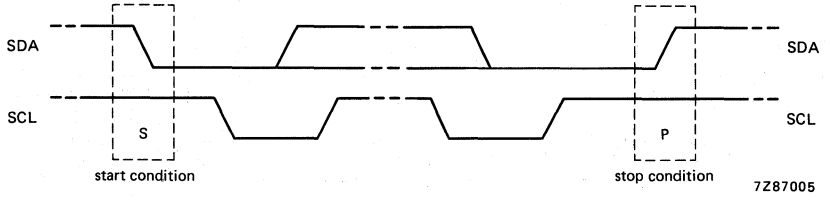


Fig. 4 Definition of start and stop conditions.

System configuration

A device generating a message is a "transmitter", a device receiving a message is the "receiver". The device that controls the message is the "master" and the devices which are controlled by the master are the "slaves".

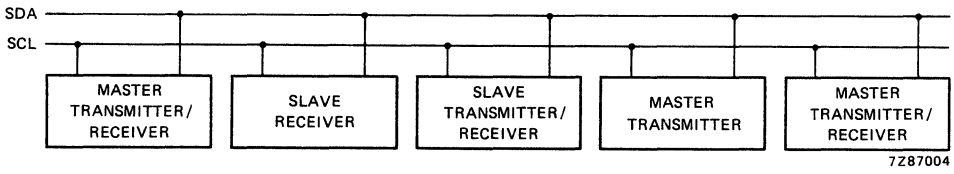


Fig. 5 System configuration.

Acknowledge

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse, set-up and hold times must be taken into account. A master receiver must signal an end of data to the transmitter by *not* generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

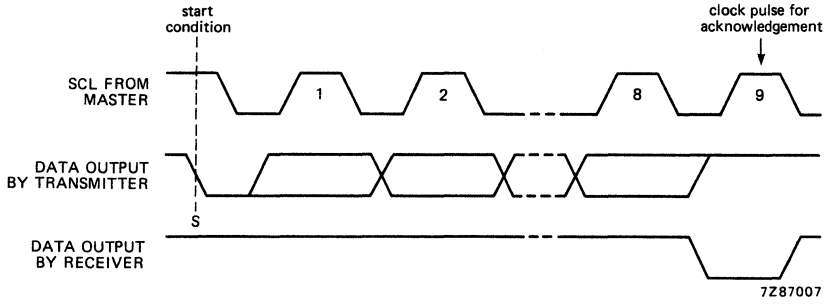


Fig. 6 Acknowledgement on the I^2C bus.

Timing specifications

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Masters generate a bus clock with a maximum frequency of 100 kHz. Detailed timing is shown in Fig. 7.

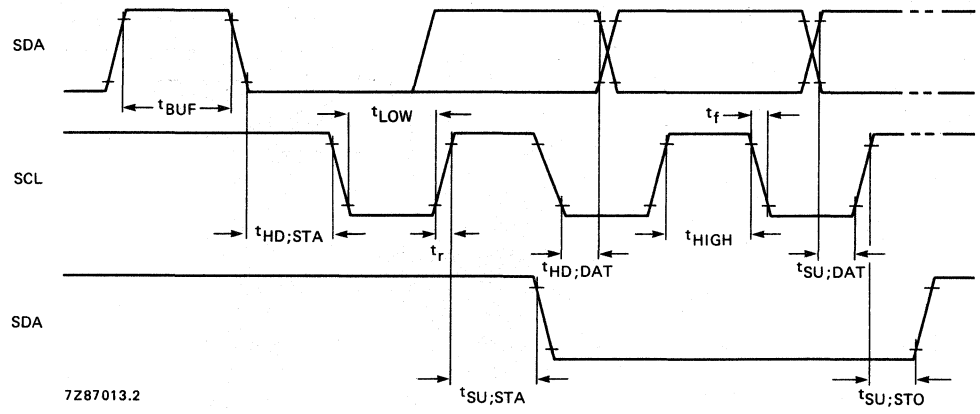


Fig. 7 Timing of the high-speed mode.

Where:

t_{BUF}	$t \geqslant t_{LOWmin}$	The minimum time the bus must be free before a new transmission can start
$t_{HD;STA}$	$t \geqslant t_{HIGHmin}$	Start condition hold time
t_{LOWmin}	4,7 μs	Clock LOW period
$t_{HIGHmin}$	4 μs	Clock HIGH period
$t_{SU;STA}$	$t \geqslant t_{LOWmin}$	Start condition set-up time, only valid for repeated start code
$t_{HD;DAT}$	$t \geqslant 0$ μs	Data hold time
$t_{SU;DAT}$	$t \geqslant 250$ ns	Data set-up time
t_r	$t \leqslant 1$ μs	Rise time of both the SDA and SCL line
t_f	$t \leqslant 300$ ns	Fall time of both the SDA and SCL line
$t_{SU;STO}$	$t \geqslant t_{LOWmin}$	Stop condition set-up time

Note

All the timing values refer to V_{IH} and V_{IL} levels with a voltage swing of V_{SS} to V_{DD}.

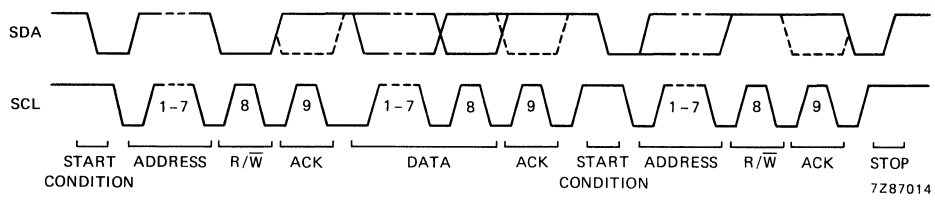


Fig. 8 Complete data transfer in the high-speed mode.

Where:

Clock t_{LOWmin}	4,7 μs
$t_{HIGHmin}$	4 μs

The dashed line is the acknowledgement of the receiver

Mark-to-space ratio	1 : 1 (LOW-to-HIGH)
Max. number of bytes	unrestricted
Premature termination of transfer	allowed by generation of STOP condition
Acknowledge clock bit	must be provided by the master

Low-speed mode

Masters generate a bus clock with a maximum frequency of 2 kHz; a minimum LOW period of 105 μs and a minimum HIGH period of 365 μs. The mark-to-space ratio is 1 : 3 LOW-to-HIGH. Detailed timing is shown in Fig. 9.

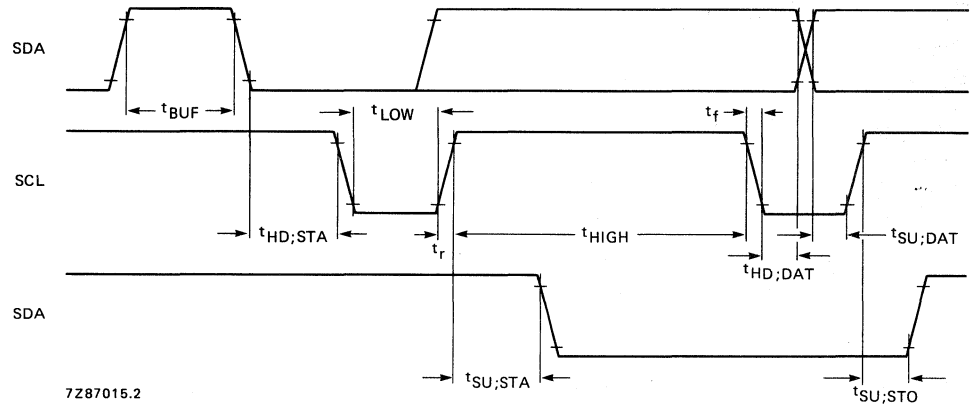


Fig. 9 Timing of the low-speed mode.

Timing specifications (continued)

Where:

t_{BUF}	$t \geqslant 105\ \mu s$ (t_{LOWmin})
$t_{HD;STA}$	$t \geqslant 365\ \mu s$ ($t_{HIGHmin}$)
t_{LOW}	$130\ \mu s \pm 25\ \mu s$
t_{HIGH}	$390\ \mu s \pm 25\ \mu s$
$t_{SU;STA}$	$130\ \mu s \pm 25\ \mu s$ *
$t_{HD;DAT}$	$t \geqslant 0\ \mu s$
$t_{SU;DAT}$	$t \geqslant 250$ ns
t_r	$t \leqslant 1\ \mu s$
t_f	$t \leqslant 300$ ns
$t_{SU;STO}$	$130\ \mu s \pm 25\ \mu s$

Note

All the timing values refer to V_{IH} and V_{IL} levels with a voltage swing of V_{SS} to V_{DD}. For definitions see high-speed mode.

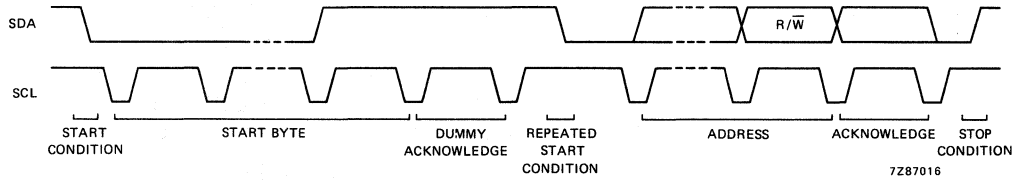


Fig. 10 Complete data transfer in the low-speed mode.

Where:

Clock t_{LOWmin}	$130\ \mu s \pm 25\ \mu s$
$t_{HIGHmin}$	$390\ \mu s \pm 25\ \mu s$
Mark-to-space ratio	1 : 3 (LOW-to-HIGH)
Start byte	0000 0001
Max. number of bytes	6
Premature termination of transfer	not allowed
Acknowledge clock bit	must be provided by master

Note

The general characteristics and detailed specification of the I^2C bus are described in a separate data sheet (serial data buses) in handbook "ICs for digital systems in radio, audio and video equipment".

* Only valid for repeated start code.

Bus protocol

Before any data is transmitted on the I²C bus, the device which should respond is addressed first. The addressing is always done with the first byte transmitted after the start procedure. The I²C bus configuration for different PCF8571 READ and WRITE cycles is shown in Fig. 11.

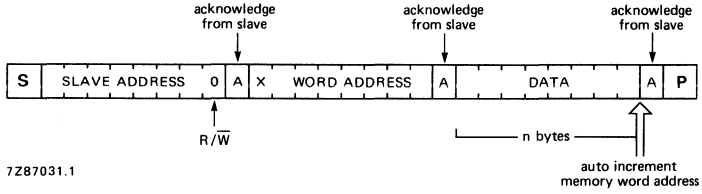


Fig. 11(a) Master transmits to slave receiver (WRITE mode).

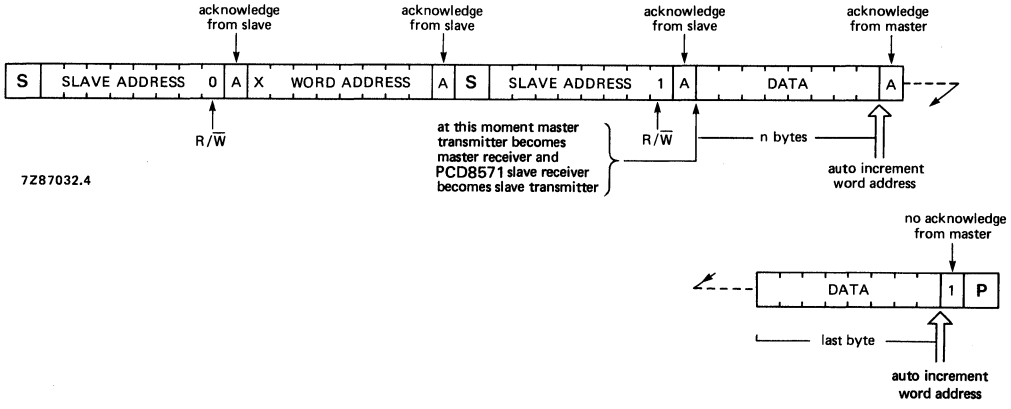


Fig. 11(b) Master reads after setting word address (WRITE word address; READ data).

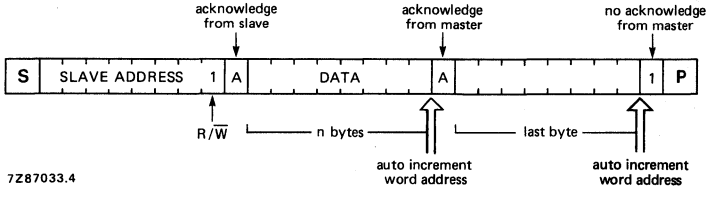


Fig. 11(c) Master reads slave immediately after first byte (READ mode).

Note

X = don't care bit.

APPLICATION INFORMATION

The PCF8571 slave address has a fixed combination 1010 as group 1, while group 2 is fully programmable (see Fig. 12).

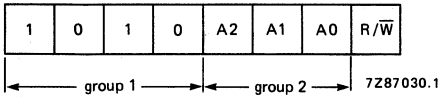


Fig. 12 PCF8571 address.

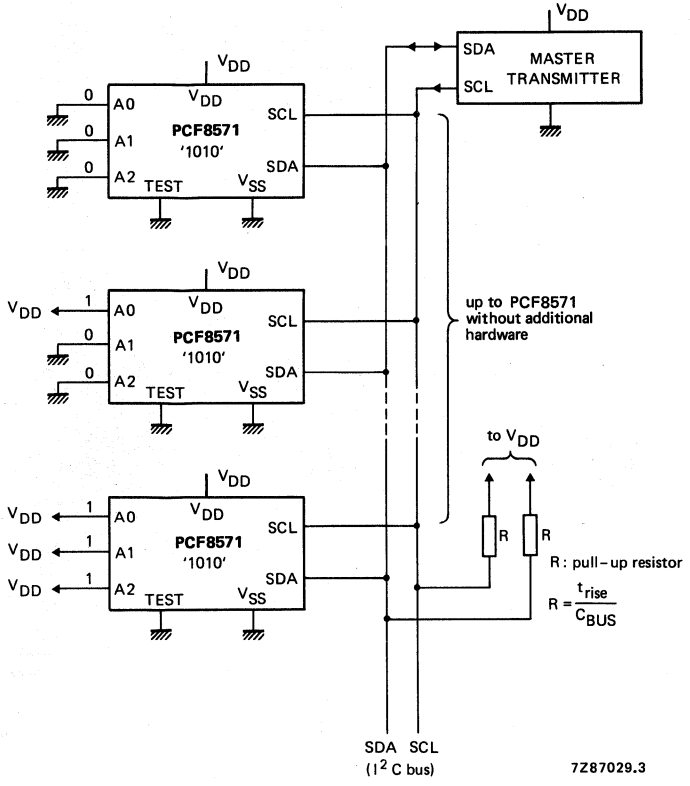


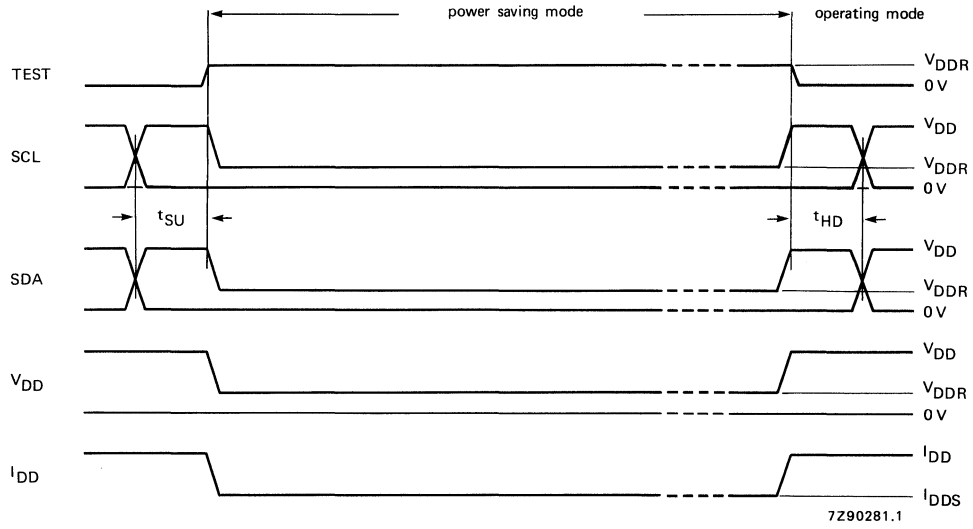
Fig. 13 PCF8571 application diagram.

Note

A0, A1, and A2 inputs must be connected to V_{DD} or V_{SS} but not left open.

POWER SAVING MODE

With the condition TEST = V_{DDR}, the PCF8571 goes into the power saving mode and I^2C bus logic is reset.



Where:
$t_{SU} \geqslant 4\ \mu s$
$t_{HD} \geqslant 4\ \mu s$

Fig. 14 Timing for power saving mode.

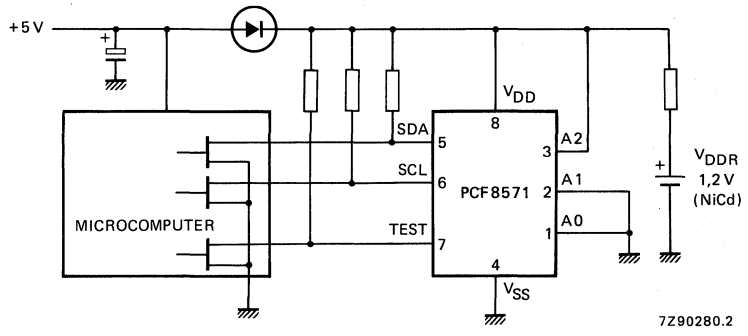
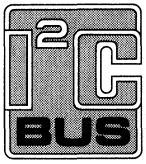


Fig. 15 Application example for power saving mode.

Note

1. In the operating mode, TEST = 0.
2. In the power saving mode, TEST = V_{DDR}.



Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

CLOCK/CALENDAR WITH SERIAL I/O

GENERAL DESCRIPTION

The PCF8573 is a low threshold, monolithic CMOS circuit that functions as a real time clock/calendar in the Inter IC (I^2C) bus-oriented microcomputer systems. The device includes an addressable time counter and an addressable alarm register, both for minutes, hours, days and months. Three special control/status flags, COMP, POWF and NODA, are also available. Information is transferred serially via a two line bidirectional bus (I^2C). Back-up for the clock during supply interruptions is provided by a 1,2 V nickel cadmium battery. The time base is generated from a 32,768 kHz crystal-controlled oscillator.

Features

- Serial input/output bus (I^2C) interface for minutes, hours, days and months
- Additional pulse outputs for seconds and minutes
- Alarm register for presetting a time for alarm or remote switching functions
- Battery back-up for clock function during supply interruption
- Crystal oscillator control (32,768 kHz)

QUICK REFERENCE DATA

Supply voltage range (clock)	$V_{DD}-V_{SS1}$		1,1 to 6,0 V
Supply voltage range (I^2C interface)	$V_{DD}-V_{SS2}$		2,5 to 6,0 V
Crystal oscillator frequency	f_{osc}	typ.	32,768 kHz

PACKAGE OUTLINES

PCF8573P: 16-lead DIL; plastic (SOT-38).
PCF8573T: 16-lead mini-pack; plastic (SO-16L; SOT-162A).

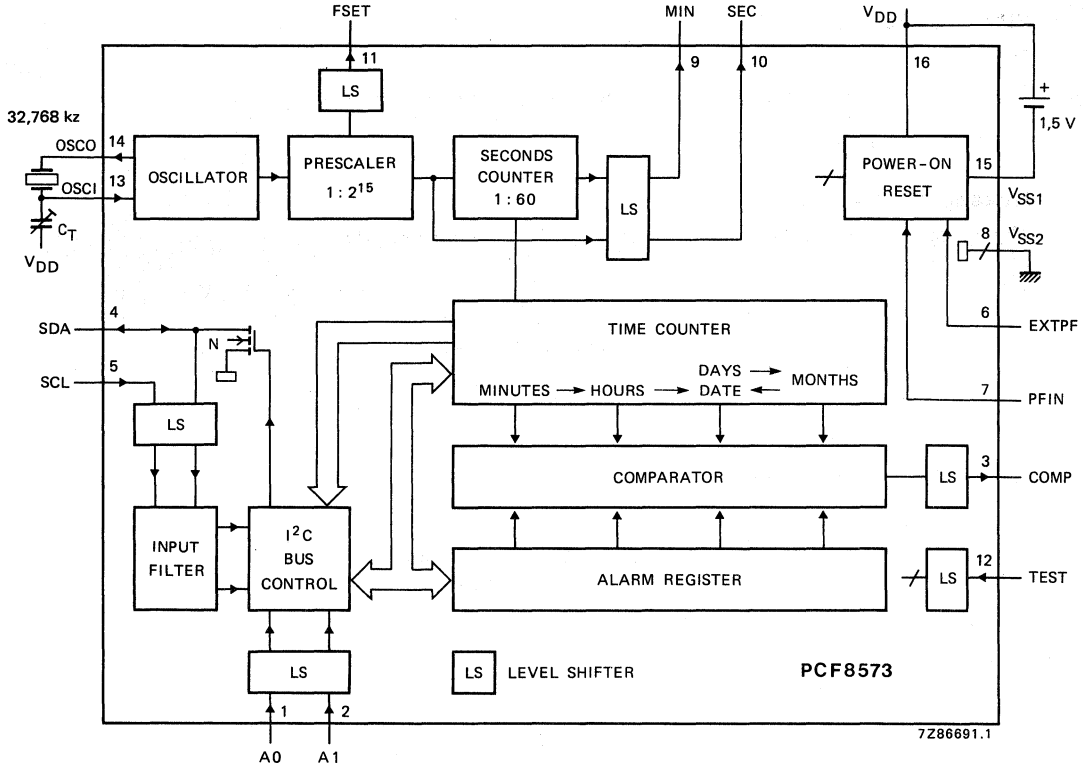


Fig. 1 Block diagram.

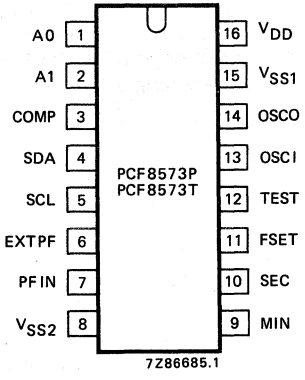


Fig. 2 Pinning diagram.

PINNING

1	A0	address input	
2	A1	address input	
3	COMP	comparator output	
4	SDA	serial data line	I^2C bus
5	SCL	serial clock line	I^2C bus
6	EXTPF	enable power fail flag input	
7	PFIN	power fail flag input	
8	V_{SS2}	negative supply 2 (I^2C interface)	
9	MIN	one pulse per minute output	
10	SEC	one pulse per second output	
11	FSET	oscillator tuning output	
12	TEST	test input; must be connected to V_{SS2} when not in use	
13	OSCI	oscillator input	
14	OSCO	oscillator input/output	
15	V_{SS1}	negative supply 1 (clock)	
16	V_{DD}	common positive supply	

FUNCTIONAL DESCRIPTION

Oscillator

The PCF8573 has an integrated crystal-controlled oscillator which provides the timebase for the prescaler. The frequency is determined by a single 32,768 kHz crystal connected between OSCI and OSCO. A trimmer is connected between OSCI and V_{DD}.

Prescaler and time counter

The prescaler provides a 128 Hz signal at the FSET output for fine adjustment of the crystal oscillator without loading it. The prescaler also generates a pulse once a second to advance the seconds counter. The carry of the prescaler and the seconds counter are available at the outputs SEC, MIN respectively, and are also readable via the I^2C bus. The mark-to-space ratio of both signals is 1 : 1. The time counter is advanced one count by the falling edge of output signal MIN. A transition from HIGH to LOW of output signal SEC triggers MIN to change state. The time counter counts minutes, hours, days and months, and provides a full calendar function which needs to be corrected once every four years. Cycle lengths are shown in Table 1.

Table 1 Cycle length of the time counter

unit	number of bits	counting cycle	carry for following unit	content of month counter
minutes	7	00 to 59	59 → 00	
hours	6	00 to 23	23 → 00	
days	6	01 to 28	28 → 01	2 (see note)
			or 29 → 01	
		01 to 30	30 → 01	4, 6, 9, 11
		01 to 31	31 → 01	1, 3, 5, 7, 8, 10, 12
months	5	01 to 12	12 → 01	

Note: Day counter may be set to 29 by a write transmission with EXECUTE ADDRESS.

Alarm register

The alarm register is a 24-bit memory. It stores the time-point for the next setting of the status flag COMP. Details of writing and reading of the alarm register are included in the description of the characteristics of the I^2C bus.

Comparator

The comparator compares the contents of the alarm register and the time counter, each with a length of 24 bits. When these contents are equal the flag COMP will be set 4 ms after the falling edge of MIN. This set condition occurs once at the beginning of each minute. This information is latched, but can be cleared by an instruction via the I^2C bus. A clear instruction may be transmitted immediately after the flag is set and will be executed. Flag COMP information is also available at the output COMP. The comparison may be based upon hours and minutes only if the internal flag NODA (no date) is set. Flag NODA can be set and cleared by separate instructions via the I^2C bus, but it is undefined until the first set or clear instruction has been received. Both COMP and NODA flags are readable via the I^2C bus.

FUNCTIONAL DESCRIPTION (continued)

Power on/power fail detection

If the voltage $V_{DD}-V_{SS1}$ falls below a certain value the operation of the clock becomes undefined. Thus a warning signal is required to indicate that faultless operation of the clock is not guaranteed. This information is latched in a flag called POWF (Power Fail) and remains latched after restoration of the correct supply voltage until a write procedure with EXECUTE ADDRESS has been received. The flag POWF can be set by an internally generated power fail level-discriminator signal for application with ($V_{DD}-V_{SS1}$) greater than V_{TH1}, or by an externally generated power fail signal for application with ($V_{DD}-V_{SS1}$) less than V_{TH1}. The external signal must be applied to the input PFIN. The input stage operates with signals of any slow rise and fall times. Internally or externally controlled POWF can be selected by input EXTPF as shown in Table 2.

Table 2 Power fail selection

EXTPF	PFIN	function
0	0	power fail is sensed internally
0	1	test mode
1	0	power fail is sensed externally
1	1	no power fail sensed

0 : connected to V_{SS1} (LOW)
1 : connected to V_{DD} (HIGH)

The external power fail control operates by absence of the $V_{DD}-V_{SS2}$ supply. Therefore the input levels applied to PFIN and EXTPF must be within the range of $V_{DD}-V_{SS1}$. A LOW level at PFIN indicates a power fail. POWF is readable via the I^2C bus. A power on reset for the I^2C bus control is generated on-chip when the supply voltage $V_{DD}-V_{SS2}$ is less than V_{TH2}.

Interface level shifters

The level shifters adjust the 5 V operating voltage ($V_{DD}-V_{SS2}$) of the microcontroller to the internal supply voltage ($V_{DD}-V_{SS1}$) of the clock/calendar. The oscillator and counter are not influenced by the $V_{DD}-V_{SS2}$ supply voltage. If the voltage $V_{DD}-V_{SS2}$ is absent ($V_{SS2} = V_{DD}$) the output signal of the level shifter is HIGH because V_{DD} is the common node of the $V_{DD}-V_{SS2}$ and the $V_{DD}-V_{SS1}$ supplies. Because the level shifters invert the input signal, the internal circuit behaves as if a LOW signal is present on the inputs. FSET, SEC, MIN and COMP are CMOS push-pull output stages. The driving capability of these outputs is lost when the supply voltage $V_{DD}-V_{SS2} = 0$.

CHARACTERISTICS OF THE I²C BUS

The I²C bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

Bit transfer (see Fig. 3)

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals.

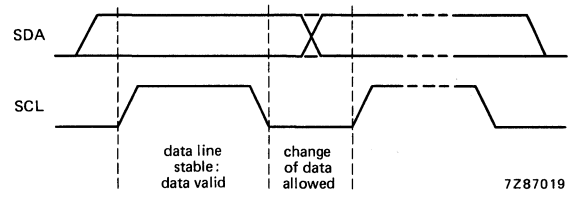


Fig. 3 Bit transfer.

Start and stop conditions (see Fig. 4)

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the stop condition (P).

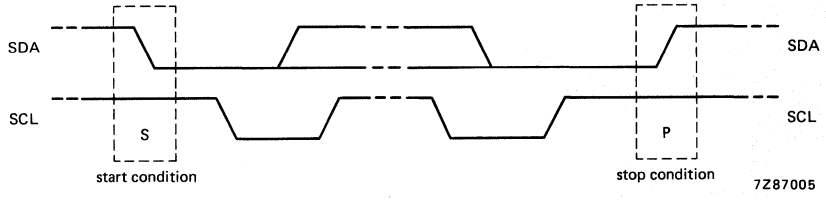


Fig. 4 Definition of start and stop conditions.

System configuration (see Fig. 5)

A device generating a message is a "transmitter", a device receiving a message is the "receiver". The device that controls the message is the "master" and the devices which are controlled by the master are the "slaves".

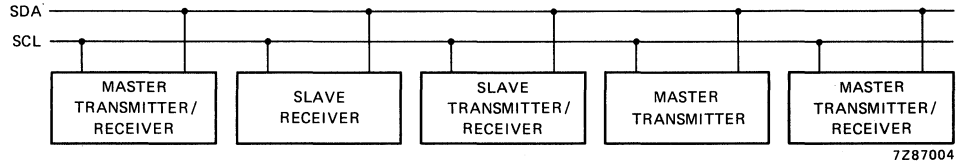


Fig. 5 System configuration.

CHARACTERISTICS OF THE I²C bus (continued)

Acknowledge (see Fig. 6)

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse, set up and hold times must be taken into account. A master receiver must signal an end of data to the transmitter by *not* generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition. (See Fig. 13 and Fig. 14.)

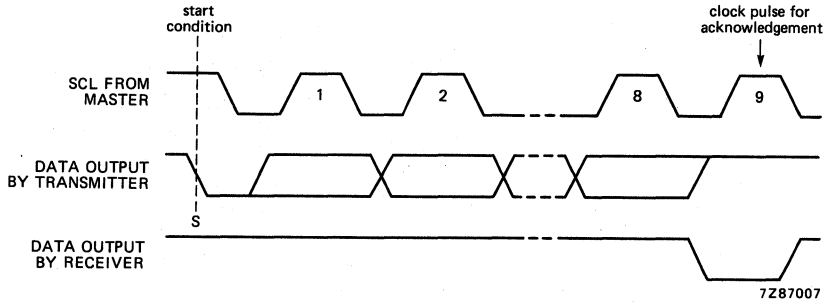


Fig. 6 Acknowledgement on the I²C bus.

Timing specifications

Within the I²C bus specifications a high-speed mode and a low-speed mode are defined. The PCF8573 operates in both modes and the timing requirements are as follows:

High-speed mode

Masters generate a bus clock with a maximum frequency of 100 kHz. Detailed timing is shown in Fig. 7.

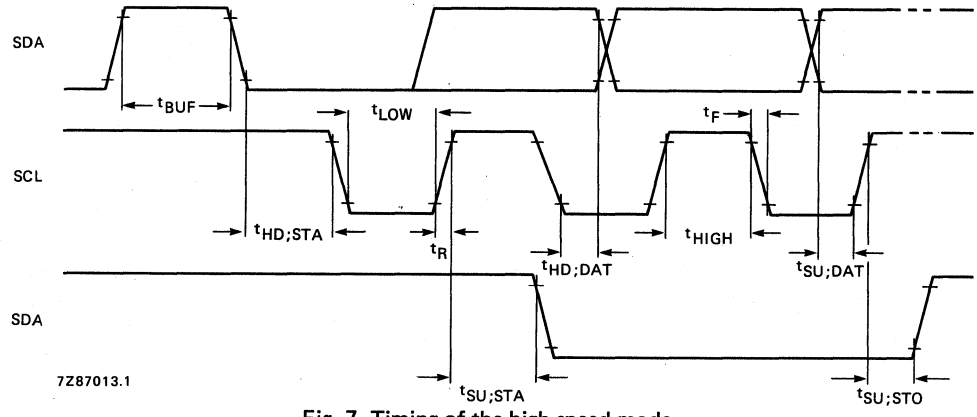


Fig. 7 Timing of the high-speed mode.

Where:

t_{BUF}	$t \geqslant t_{LOWmin}$	The minimum time the bus must be free before a new transmission can start
$t_{HD;STA}$	$t \geqslant t_{HIGHmin}$	Start condition hold time
t_{LOWmin}	4,7 μs	Clock LOW period
$t_{HIGHmin}$	4 μs	Clock HIGH period
$t_{SU;STA}$	$t \geqslant t_{LOWmin}$	Start condition set-up time, only valid for repeated start code
$t_{HD;DAT}$	$t \geqslant 0$ μs	Data hold time
$t_{SU;DAT}$	$t \geqslant 250$ ns	Data set-up time
t_R	$t \leqslant 1$ μs	Rise time of both the SDA and SCL line
t_F	$t \leqslant 300$ ns	Fall time of both the SDA and SCL line
$t_{SU;STO}$	$t \geqslant t_{LOWmin}$	Stop condition set-up time

Note

All the values refer to V_{IH} and V_{IL} levels with a voltage swing of V_{DD} to V_{SS2}.

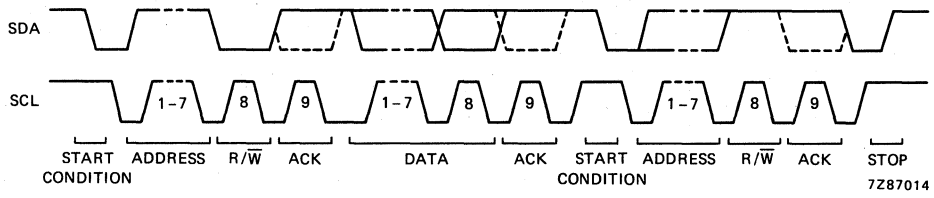


Fig. 8 Complete data transfer in the high-speed mode.

Where:

Clock t_{LOWmin}	4,7 μs
$t_{HIGHmin}$	4 μs
The dashed line is the acknowledgement of the receiver	
Mark-to-space ratio	1 : 1 (LOW-to-HIGH)
Max. number of bytes	unrestricted
Premature termination of transfer	allowed by generation of STOP condition
Acknowledge clock bit	must be provided by the master

CHARACTERISTICS OF THE I²C BUS (continued)

Low-speed mode

Masters generate a bus clock with a maximum frequency of 2 kHz; a minimum LOW period of 105 μs and a minimum HIGH period of 365 μs. The mark-to-space ratio is 1 : 3 LOW-to-HIGH. Detailed timing is shown in Fig. 9.

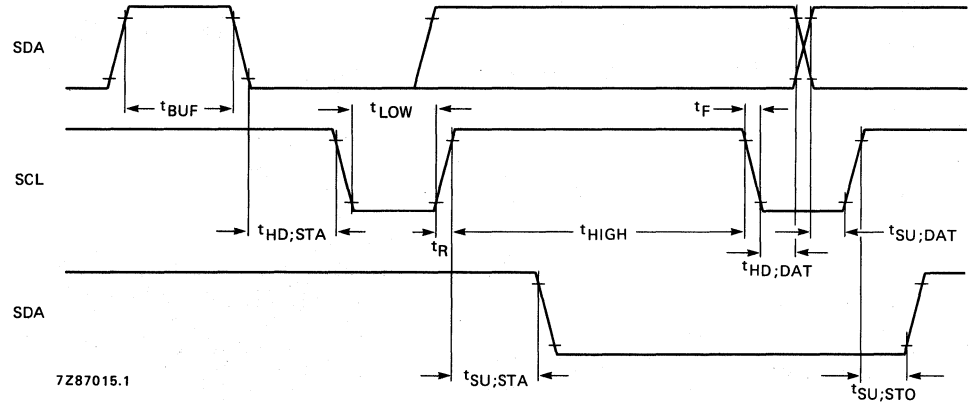


Fig. 9 Timing of the low-speed mode.

Where:

t_{BUF}	$t \geqslant 105\ \mu s$ (t_{LOWmin})
$t_{HD;STA}$	$t \geqslant 365\ \mu s$ ($t_{HIGHmin}$)
t_{LOW}	$130\ \mu s \pm 25\ \mu s$
t_{HIGH}	$390\ \mu s \pm 25\ \mu s$
$t_{SU;STA}$	$130\ \mu s \pm 25\ \mu s$*
$t_{HD;DAT}$	$t \geqslant 0\ \mu s$
$t_{SU;DAT}$	$t \geqslant 250$ ns
t_R	$t \leqslant 1\ \mu s$
t_F	$t \leqslant 300$ ns
$t_{SU;STO}$	$130\ \mu s \pm 25\ \mu s$

Note

All the values refer to V_{IH} and V_{IL} levels with a voltage swing of V_{DD} to V_{SS2}, for definitions see high-speed mode.

* Only valid for repeated start code.

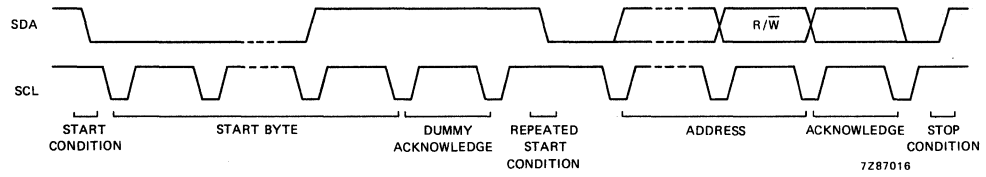


Fig. 10 Complete data transfer in the low-speed mode.

Where:

Clock t_{LOWmin}	130 μs ± 25 μs
$t_{HIGHmin}$	390 μs ± 25 μs
Mark-to-space ratio	1 : 3 (LOW-to-HIGH)
Start byte	0000 0001
Max. number of bytes	6
Premature termination of transfer	not allowed
Acknowledge clock bit	must be provided by master

Note

The general characteristics and detailed specification of the I^2C bus are described in a separate data sheet (serial data buses) in handbook: ICs for digital systems in radio, audio and video equipment.

ADDRESSING

Before any data is transmitted on the I²C bus, the device which should respond is addressed first. The addressing is always done with the first byte transmitted after the start procedure.

Slave address

The clock/calendar acts as a slave receiver or slave transmitter. Therefore the clock signal SCL is only an input signal, but the data signal SDA is a bidirectional line. The clock calendar slave address is shown in Fig. 11.

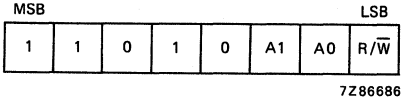


Fig. 11 Slave address.

The subaddress bits A0 and A1 correspond to the two hardware address pins A0 and A1 which allows the device to have 1 of 4 different addresses.

Clock/calendar READ/WRITE cycles

The I²C bus configuration for different clock/calendar READ and WRITE cycles is shown in Fig. 12 and Fig. 13.

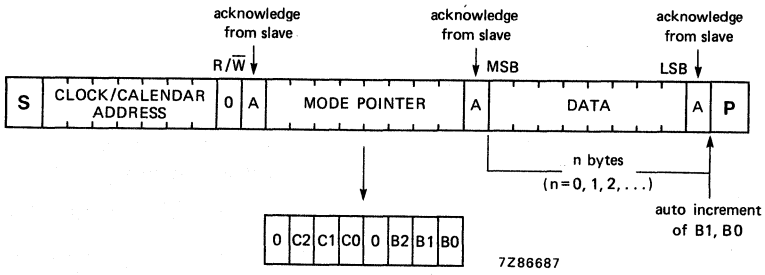


Fig. 12 Master transmitter transmits to clock/calendar slave receiver.

The write cycle is used to set the time counter, the alarm register and the flags. The transmission of the clock/calendar address is followed by the MODE-POINTER-WORD which contains a CONTROL-nibble (Table 3) and an ADDRESS-nibble (Table 4). The ADDRESS-nibble is valid only if the preceding CONTROL-nibble is set to EXECUTE ADDRESS. The third transmitted word contains the data to be written into the time counter or alarm register.

Table 3 CONTROL-nibble

	C2	C1	C0	function
0	0	0	0	execute address
0	0	0	1	read control/status flags
0	0	1	0	reset prescaler, including seconds counter; without carry for minute counter
0	0	1	1	time adjust, with carry for minute counter (see note)
0	1	0	0	reset NODA flag
0	1	0	1	set NODA flag
0	1	1	0	reset COMP flag

Note

If the seconds counter is below 30 there is no carry. This causes a time adjustment of max. −30 s. From the count 30 there is a carry which adjusts the time by max. + 30 s.

Table 4 ADDRESS-nibble

	B2	B1	B0	addressed to:
0	0	0	0	time counter hours
0	0	0	1	time counter minutes
0	0	1	0	time counter days
0	0	1	1	time counter months
0	1	0	0	alarm register hours
0	1	0	1	alarm register minutes
0	1	1	0	alarm register days
0	1	1	1	alarm register months

At the end of each data word the address bits B1, B0 will be incremented automatically provided the preceding CONTROL-nibble is set to EXECUTE ADDRESS. There is no carry to B2.

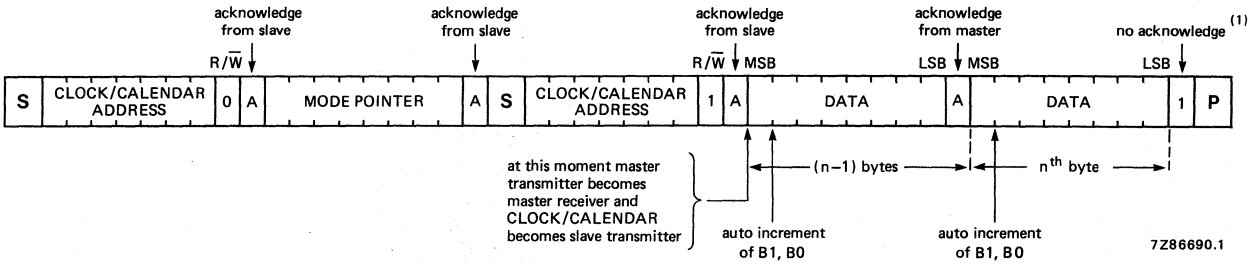
Table 5 shows the placement of the BCD upper and lower digits in the DATA byte for writing into the addressed part of the time counter and alarm register respectively.

Table 5 Placement of BCD digits in the DATA byte

MSB				DATA			LSB	
upper digit				lower digit				
UD	UC	UB	UA	LD	LC	LB	LA	addressed to:
X	X	D	D	D	D	D	D	hours
X	D	D	D	D	D	D	D	minutes
X	X	D	D	D	D	D	D	days
X	X	X	D	D	D	D	D	months

Where "X" is the don't care bit and "D" is the data bit.

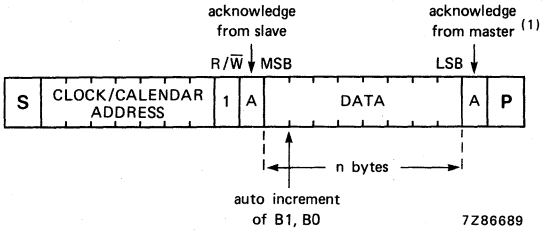
Acknowledgement response of the clock calendar as slave receiver is shown in Table 6.



(1) The master receiver must signal an end of data to the slave transmitter by *not* generating an acknowledge on the *last byte* that has been clocked out of the slave.

Fig. 13 Master transmitter reads clock/calendar after setting mode pointer.

To read the addressed part of the time counter and alarm register, plus information from specified control/status flags, the BCD digits in the DATA byte are organized as shown in Table 7.



(1) The master receiver must signal an end of data to the slave transmitter by *not* generating an acknowledge on the *last byte* that has been clocked out of the slave.

Fig. 14 Master reads clock/calendar immediately after first byte.

The status of the MODE-POINTER-WORD concerning the CONTROL-nibble remains unchanged until a write to MODE POINTER condition occurs.

ADDRESSING (continued)

Table 6 Slave receiver acknowledgement

mode pointer								acknowledge on byte		
								address	mode pointer	data
	C2	C1	C0		B2	B1	B0			
0	0	0	0	0	X	X	X	yes	yes	yes
0	0	0	0	1	X	X	X	yes	no	no
0	0	0	1	X	X	X	X	yes	yes	no
0	0	1	0	X	X	X	X	yes	yes	no
0	0	1	1	X	X	X	X	yes	yes	no
0	1	0	0	X	X	X	X	yes	yes	no
0	1	0	1	X	X	X	X	yes	yes	no
0	1	1	0	X	X	X	X	yes	yes	no
0	1	1	1	X	X	X	X	yes	no	no
1	X	X	X	X	X	X	X	yes	no	no

Where "X" is the don't care bit.

Table 7 Organization of the BCD digits in the DATA byte

MSB DATA LSB								
upper digit				lower digit				
UD	UC	UB	UA	LD	LC	LB	LA	addressed to
0	0	D	D	D	D	D	D	hours
0	D	D	D	D	D	D	D	minutes
0	0	D	D	D	D	D	D	days
0	0	0	D	D	D	D	D	months
0	0	0	*	**	NODA	COMP	POWF	control/status flags

Where: "D" is the data bit.
* = minutes.
** = seconds.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage ranges	$V_{DD}-V_{SS1}$		−0,3 to + 8	V
	$V_{DD}-V_{SS2}$		−0,3 to + 8	V
Voltage on pins 4 and 5			V_{SS2}−0,8 to V_{DD} + 0,8	V*
Voltage on pins 6, 7, 13 and 14			V_{SS1}−0,6 to V_{DD} + 0,6	V
Voltage on any other pin			V_{SS2}−0,6 to V_{DD} + 0,6	V
Input current	I_I	max.	10	mA
Output current	I_O	max.	10	mA
Power dissipation per output	P_O	max.	100	mW
Total power dissipation per package	P_{tot}	max.	200	mW
Operating ambient temperature range	T_{amb}		−40 to + 85	°C
Storage temperature range	T_{stg}		−55 to + 125	°C

HANDLING

Inputs and outputs are protected against electrostatic charge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see 'Handling MOS Devices').

* Impedance min. 500 Ω.

CHARACTERISTICS

V_{SS2} = 0 V; T_{amb} = −40 to + 85 °C unless otherwise specified. Typical values at T_{amb} = + 25 °C

parameter	symbol	min.	typ.	max.	unit	
Supply						
Supply voltage (I^2C interface)	$V_{DD}-V_{SS2}$	2,5	5	6,0	V	
Supply voltage (clock)	$V_{DD}-V_{SS1}$	1,3	1,5	$(V_{DD}-V_{SS2})$	V	←
Supply voltage (clock) at $t_{HD} > 500$ ns	$V_{DD}-V_{SS1}$	1,1	1,5	$(V_{DD}-V_{SS2})$	V	←
Supply current V_{SS1}						
at $V_{DD}-V_{SS1}$ = 1,5 V	$-I_{SS1}$	–	3	10	μA	
at $V_{DD}-V_{SS1}$ = 5 V	$-I_{SS1}$	–	12	50	μA	
Supply current V_{SS2} at $V_{DD}-V_{SS2}$ = 5 V (I_O = 0 mA on all outputs)	$-I_{SS2}$	–	–	50	μA	
Inputs SCL, SDA, A0, A1, TEST						
Input voltage HIGH	V_{IH}	0,7 x V_{DD}	–	–	V	
Input voltage LOW	V_{IL}	–	–	0,3 x V_{DD}	V	
Input leakage current at $V_I = V_{SS2}$ to V_{DD}	$\pm I_I$	–	–	1	μA	
Inputs EXTPF, PFIN						
Input voltage HIGH	$V_{IH}-V_{SS1}$	0,7 x $(V_{DD}-V_{SS1})$	–	–	V	
Input voltage LOW	$V_{IL}-V_{SS1}$	0	–	0,3 x $(V_{DD}-V_{SS1})$	V	
Input leakage current						
at $V_I = V_{SS1}$ to V_{DD}	$\pm I_I$	–	–	1	μA	
at T_{amb} = 25 °C; $V_I = V_{SS1}$ to V_{DD}	$\pm I_I$	–	–	0,1	μA	
Outputs SEC, MIN, COMP, FSET (normal buffer outputs)						
Output voltage HIGH						
at $V_{DD}-V_{SS2}$ = 2,5 V; $-I_O$ = 0,1 mA	V_{OH}	$V_{DD}-0,4$	–	–	V	
at $V_{DD}-V_{SS2}$ = 4 to 6 V; $-I_O$ = 0,5 mA	V_{OH}	$V_{DD}-0,4$	–	–	V	
Output voltage LOW						
at $V_{DD}-V_{SS2}$ = 2,5 V; I_O = 0,3 mA	V_{OL}	–	–	0,4	V	
at $V_{DD}-V_{SS2}$ = 4 to 6 V; I_O = 1,6 mA	V_{OL}	–	–	0,4	V	

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Output SDA (N-channel open drain)					
Output "ON": I_O = 3 mA at $V_{DD}-V_{SS2}$ = 2,5 to 6 V	V_{OL}	–	–	0,4	V
Output "OFF" (leakage current) at $V_{DD}-V_{SS2}$ = 6 V; V_O = 6 V	I_O	–	–	1	μA
Internal threshold voltage					
Power failure detection	V_{TH1}	1	1,2	1,4	V
Power "ON" reset at $V_{SCL} = V_{SDA} = V_{DD}$	V_{TH2}	1,5	2,0	2,5	V
Rise and fall times of input signals					
Input EXTPF	t_r, t_f	–	–	1	μs
Input PFIN	t_r, t_f	–	–	∞	μs
Input signals except EXTPF and PFIN between V_{IL} and V_{IH} levels					
rise time	t_r	–	–	1	μs
fall time	t_f	–	–	0,3	μs
Frequency at SCL at $V_{DD}-V_{SS2}$ = 4 to 6 V					
Pulse width LOW (see Figs 7 and 9)	t_{LOW}	4,7	–	–	μs
Pulse width HIGH (see Figs 7 and 9)	t_{HIGH}	4	–	–	μs
Noise suppression time constant at SCL and SDA input	T_I	0,25	1	2,5	μs
Input capacitance (SCL, SDA)	C_I	–	–	7	pF
Oscillator					
Integrated oscillator capacitance	C_{out}	–	40	–	pF
Oscillator feedback resistance	R_f	–	3	–	MΩ
Oscillator stability for: $\Delta(V_{DD}-V_{SS1})$ = 100 mV at $V_{DD}-V_{SS1}$ = 1,55 V; T_{amb} = 25 °C	f/f_{osc}	–	2×10^{-6}	–	–
Quartz crystal parameters					
Frequency = 32,768 kHz					
Series resistance	R_S	–	–	40	kΩ
Parallel capacitance	C_L	–	9	–	pF
Trimmer capacitance	C_T	5	–	25	pF

Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

APPLICATION INFORMATION

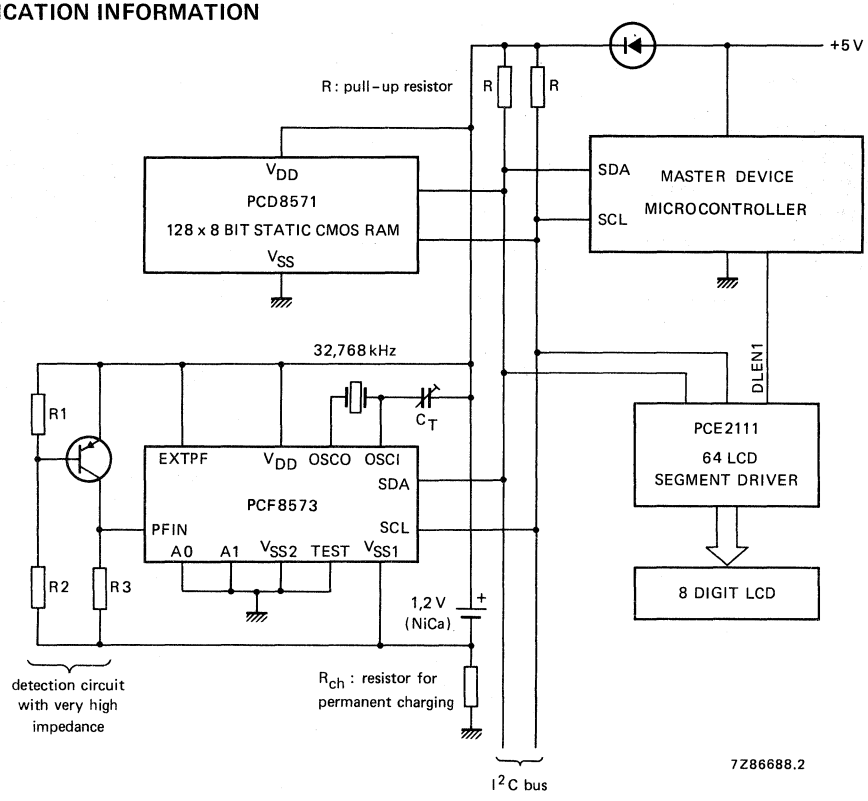


Fig. 15 Application example of the PCF8573 clock/calendar.

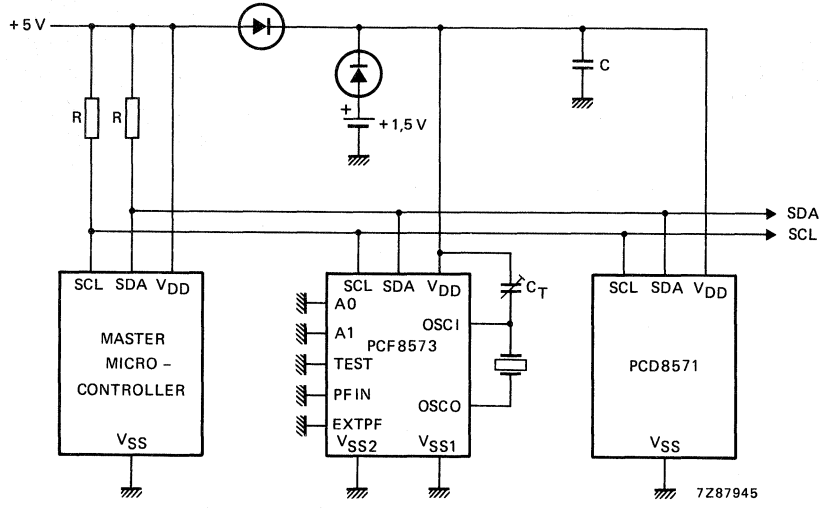


Fig. 16 Application example of the PCF8573 with common V_{SS1} and V_{SS2} supply.

REMOTE 8-BIT I/O FOR I²C BUS

GENERAL DESCRIPTION

The PCF8574 is a single-chip silicon gate CMOS circuit. It provides remote I/O expansion for the MAB8400 and PCF8500 microcomputer families via the two-line serial bidirectional bus (I²C).
It can also interface microcomputers without a serial interface to the I²C bus (as a slave function only).
The device consists of an 8-bit quasi-bidirectional port and an I²C interface.
The PCF8574 has low current consumption and includes latched outputs with high current drive capability for directly driving LEDs. It also possesses an interrupt line (INT) which is connected to the interrupt logic of the microcomputer on the I²C bus. By sending an interrupt signal on this line, the remote I/O can inform the microcomputer if there is incoming data on its ports without having to communicate via the I²C bus. This means that the PCF8574 can remain a simple slave device.

Features

- Operating supply voltage 2,5 V to 6 V
- Low stand-by current consumption max. 10 μA
- Bidirectional expander
- Open drain interrupt output
- 8-bit remote I/O port for the I²C bus
- Peripheral for the MAB8400 and PCF8500 microcomputer families
- Latched outputs with high current drive capability for directly driving LEDs
- Address by 3 hardware address pins for use of up to 8 devices (up to 16 possible with mask option)

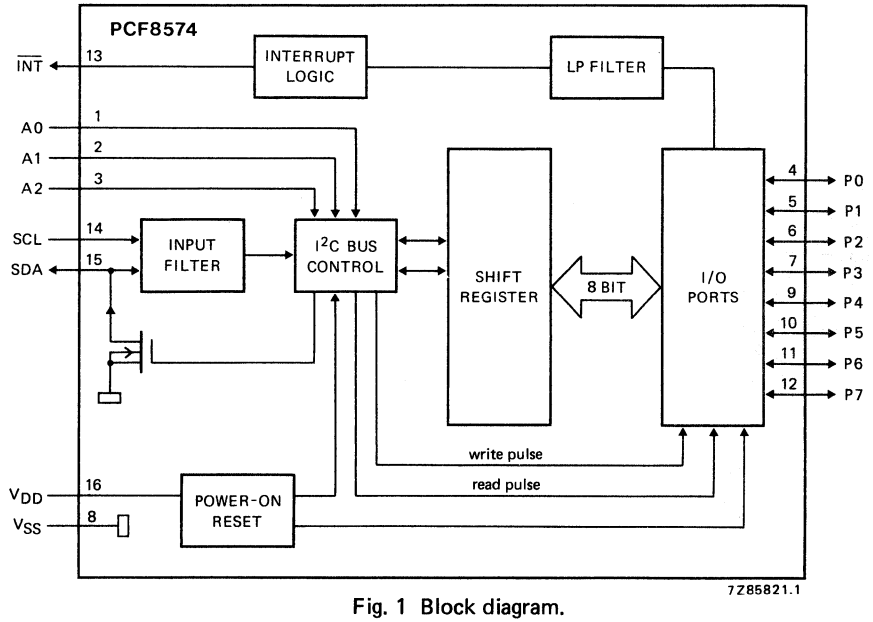


Fig. 1 Block diagram.

PACKAGE OUTLINES

PCF8574P: 16-lead DIL; plastic (SOT-38).
PCF8574T: 16-lead mini-pack; plastic (SO-16L; SOT-162A).

PINNING

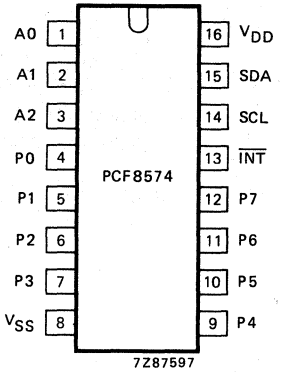


Fig. 2 Pinning diagram.

1 to 3	A0 to A2	address inputs
4 to 7 9 to 12	P0 to P3 P4 to P7	8-bit quasi-bidirectional I/O port
8	V_{SS}	negative supply
13	$\overline{INT}$	interrupt output
14	SCL	serial clock line
15	SDA	serial data line
16	V_{DD}	positive supply

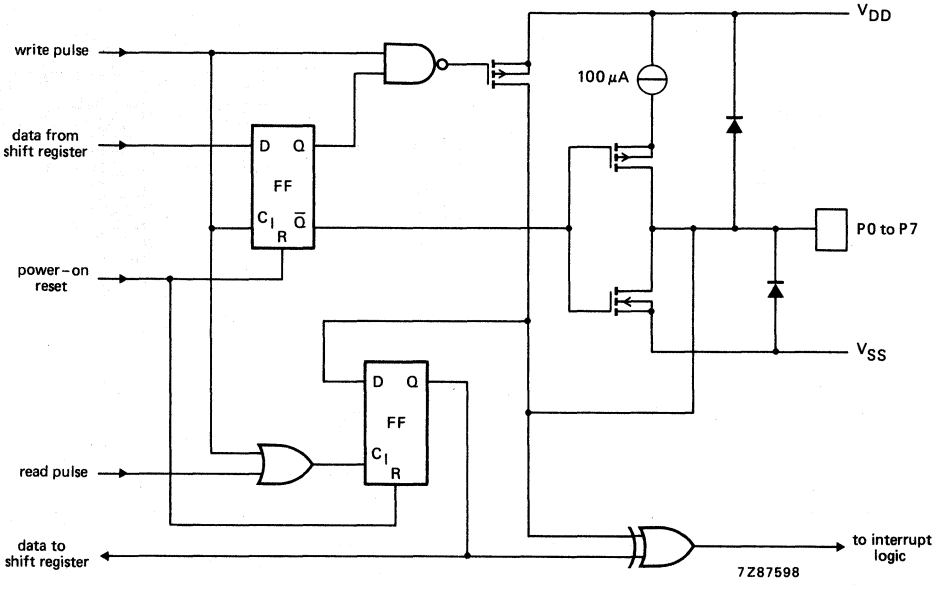


Fig. 3 Simplified schematic diagram of each port.

CHARACTERISTICS OF THE I²C BUS

The I²C bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals.

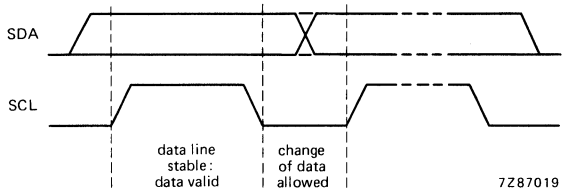


Fig. 4 Bit transfer.

Start and stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the stop condition (P).

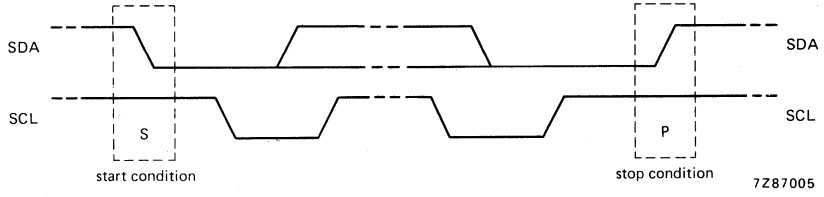


Fig. 5 Definition of start and stop conditions.

System configuration

A device generating a message is a "transmitter", a device receiving a message is the "receiver". The device that controls the message is the "master" and the devices which are controlled by the master are the "slaves".

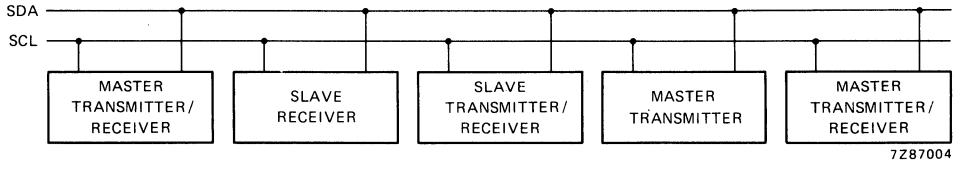


Fig. 6 System configuration.

CHARACTERISTICS OF THE I²C BUS (continued)

Acknowledge

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse, set up and hold times must be taken into account. A master receiver must signal an end of data to the transmitter by *not* generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

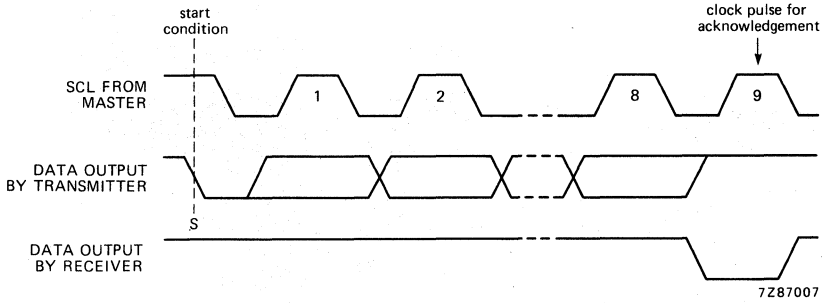


Fig. 7 Acknowledgement on the I²C bus.

Timing specifications

Within the I²C bus specifications a high-speed mode and a low-speed mode are defined. The PCF8574 operates in both modes and the timing requirements are as follows:

High-speed mode

Masters generate a bus clock with a maximum frequency of 100 kHz. Detailed timing is shown in Fig. 8.

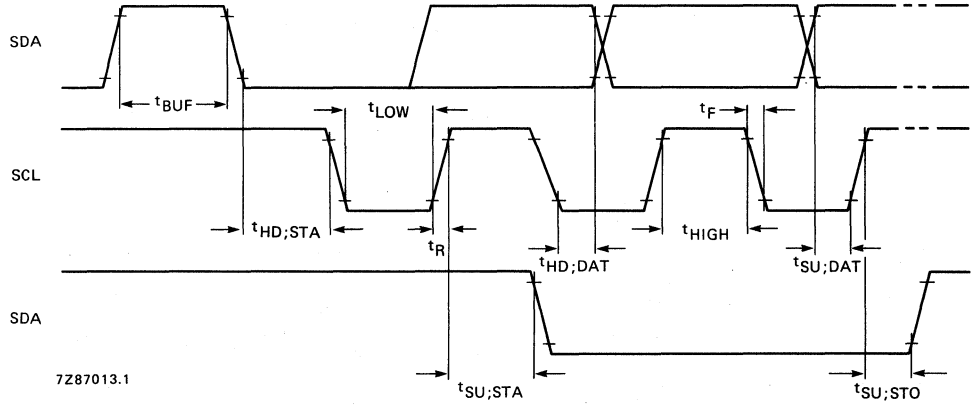


Fig. 8 Timing of the high-speed mode.

Where:

t_{BUF}	$t \geqslant t_{LOWmin}$	The minimum time the bus must be free before a new transmission can start
$t_{HD;STA}$	$t \geqslant t_{HIGHmin}$	Start condition hold time
t_{LOWmin}	4,7 μs	Clock LOW period
$t_{HIGHmin}$	4 μs	Clock HIGH period
$t_{SU;STA}$	$t \geqslant t_{LOWmin}$	Start condition set-up time, only valid for repeated start code
$t_{HD;DAT}$	$t \geqslant 0$ μs	Data hold time
$t_{SU;DAT}$	$t \geqslant 250$ ns	Data set-up time
t_R	$t \leqslant 1$ μs	Rise time of both the SDA and SCL line
t_F	$t \leqslant 300$ ns	Fall time of both the SDA and SCL line
$t_{SU;STO}$	$t \geqslant t_{LOWmin}$	Stop condition set-up time

Note

All the values refer to V_{IH} and V_{IL} levels with a voltage swing of V_{SS} to V_{DD}.

DEVELOPMENT DATA

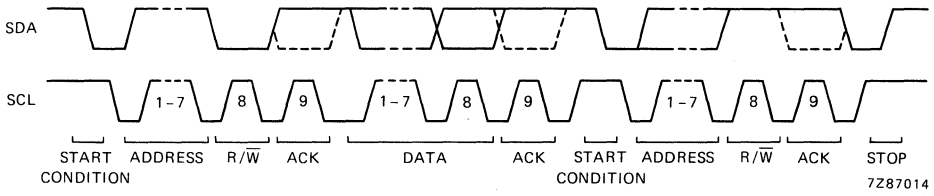


Fig. 9 Complete data transfer in the high-speed mode.

Where:

Clock t_{LOWmin}	4,7 μs
$t_{HIGHmin}$	4 μs
The dashed line is the acknowledgement of the receiver	
Mark-to-space ratio	1 : 1 (LOW-to-HIGH)
Max. number of bytes	unrestricted
Premature termination of transfer	allowed by generation of STOP condition
Acknowledge clock bit	must be provided by the master

CHARACTERISTICS OF THE I²C BUS (continued)

Low-speed mode

Masters generate a bus clock with a maximum frequency of 2 kHz; a minimum LOW period of 105 μs and a minimum HIGH period of 365 μs. The mark-to-space ratio is 1 : 3 LOW-to-HIGH. Detailed timing is shown in Fig. 10.

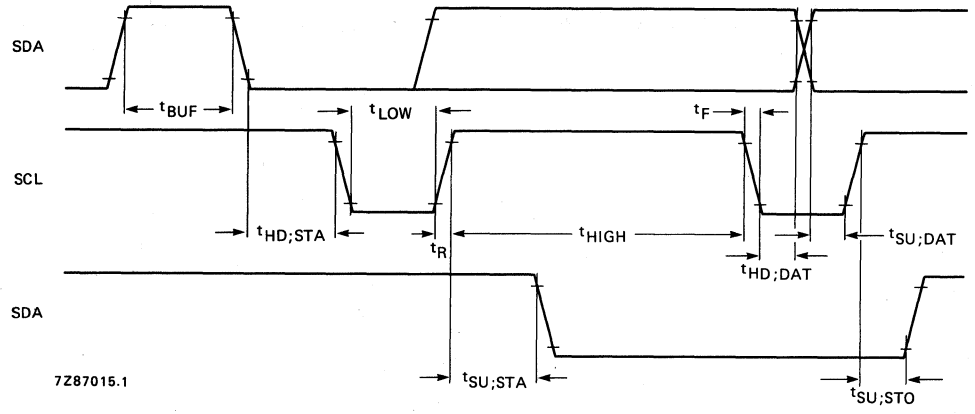


Fig. 10 Timing of the low-speed mode.

Where:

t_{BUF}	$t \geqslant 105\ \mu s$ (t_{LOWmin})
$t_{HD;STA}$	$t \geqslant 365\ \mu s$ ($t_{HIGHmin}$)
t_{LOW}	130 μs ± 25 μs
t_{HIGH}	390 μs ± 25 μs
$t_{SU;STA}$	130 μs ± 25 μs *
$t_{HD;DAT}$	$t \geqslant 0\ \mu s$
$t_{SU;DAT}$	$t \geqslant 250$ ns
t_R	$t \leqslant 1\ \mu s$
t_F	$t \leqslant 300$ ns
$t_{SU;STO}$	130 μs ± 25 μs

Note

All the values refer to V_{IH} and V_{IL} levels with a voltage swing of V_{SS} to V_{DD}, for definitions see high-speed mode.

* Only valid for repeated start code.

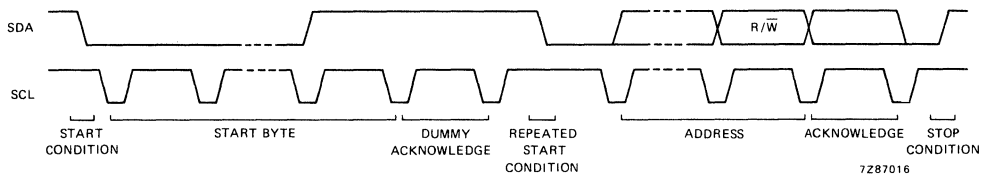


Fig. 11 Complete data transfer in the low-speed mode.

Where:	
Clock t_{LOWmin}	130 μs ± 25 μs
$t_{HIGHmin}$	390 μs ± 25 μs
Mark-to-space ratio	1 : 3 (LOW-to-HIGH)
Start byte	0000 0001
Maximum number of bytes	6
Premature termination of transfer	not allowed
Acknowledge clock bit	must be provided by master

Note

The general characteristics and detailed specification of the I²C bus are described in a separate data sheet (serial data buses) in handbook: ICs for digital systems in radio, audio and video equipment.

DEVELOPMENT DATA

FUNCTIONAL DESCRIPTION

Addressing (see Figs 12 and 13)

Each bit of the PCF8574 I/O port can be independently used as an input or an output. Input data is transferred from the port to the microcomputer by the READ mode. Output data is transmitted to the port by the WRITE mode.

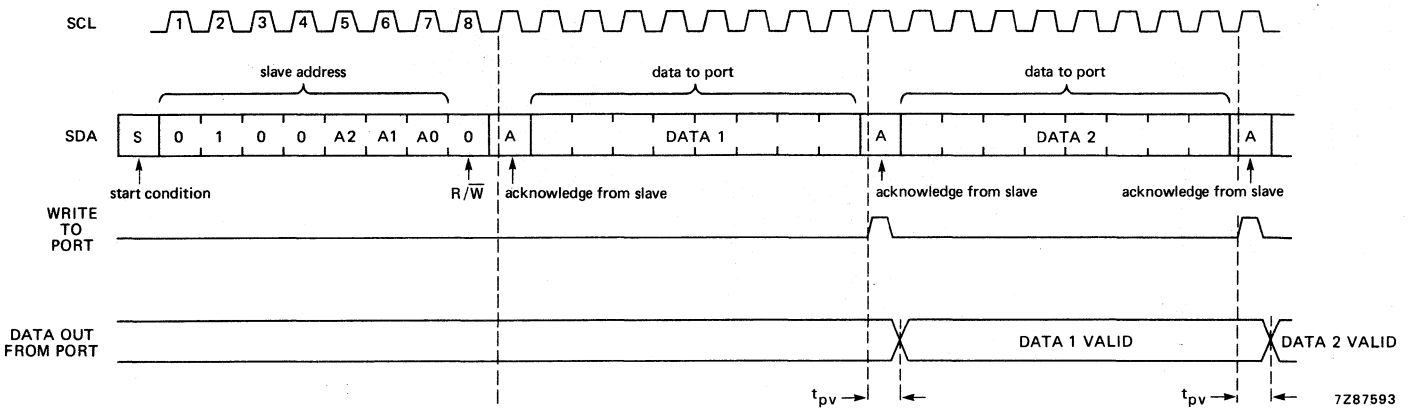


Fig. 12 WRITE mode (output port).

DEVELOPMENT DATA

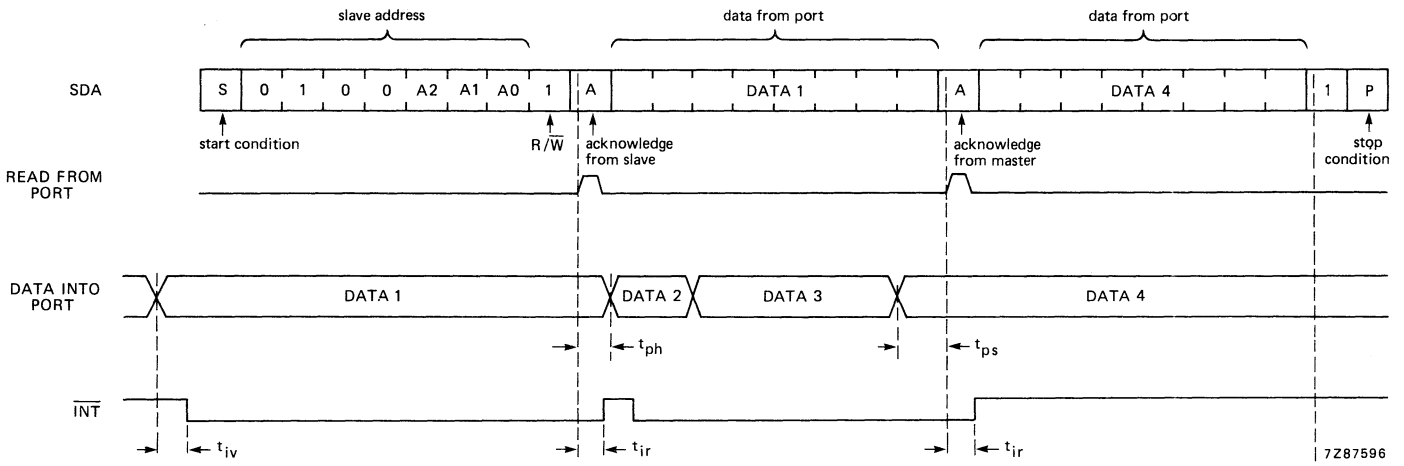


Fig. 13 READ mode (input port).

Note

A LOW-to-HIGH transition of SDA, while SCL is HIGH is defined as the stop condition (P). Transfer of data can be stopped at any moment by a stop condition. When this occurs, data present at the last acknowledge phase is valid (output mode). Input data is lost.

Interrupt (see Figs 14 and 15)

The PCF8574 provides an open drain output ($\overline{INT}$) which can be fed to a corresponding input of the microcomputer. This gives these chips a type of master function which can initiate an action elsewhere in the system.

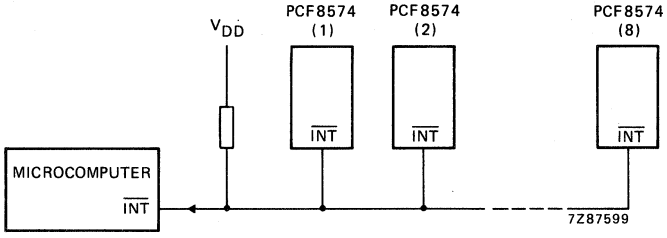


Fig. 14 Application of multiple PCF8574s with interrupt.

An interrupt is generated by any rising or falling edge of the port inputs in the input mode. After time t_{iv} the signal $\overline{INT}$ is valid.
Resetting and reactivating the interrupt circuit is achieved when data on the port is changed to the original setting or data is read from or written to the port which has generated the interrupt.
Resetting occurs as follows:

- In the READ mode at the acknowledge bit after the rising edge of the SCL signal.
- In the WRITE mode at the acknowledge bit after the HIGH to LOW transition of the SCL signal.

Each change of the ports after the resettings will be detected and after the next rising clock edge, will be transmitted as $\overline{INT}$.
Reading from or writing to another device does not affect the interrupt circuit.

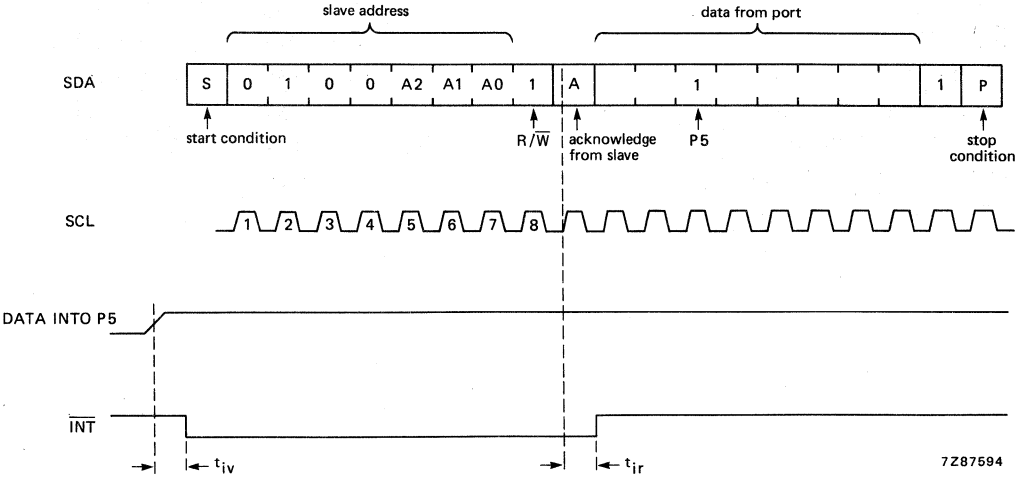


Fig. 15 Interrupt generated by a change of input to port P5.

FUNCTIONAL DESCRIPTION (continued)

Quasi-bidirectional I/O ports (see Fig. 16)

A quasi-bidirectional port can be used as an input or output without the use of a control signal for data direction. The bit designated as an input must first be loaded with a logic 1. In this mode only a current source to V_{DD} is active. An additional strong pull-up to V_{DD} allows fast rising edges into heavily loaded outputs. These devices turn on when an output changes from LOW to HIGH, and are switched off by the negative edge of SCL. SCL should not remain HIGH when a short-circuit to V_{SS} is allowed (input mode).

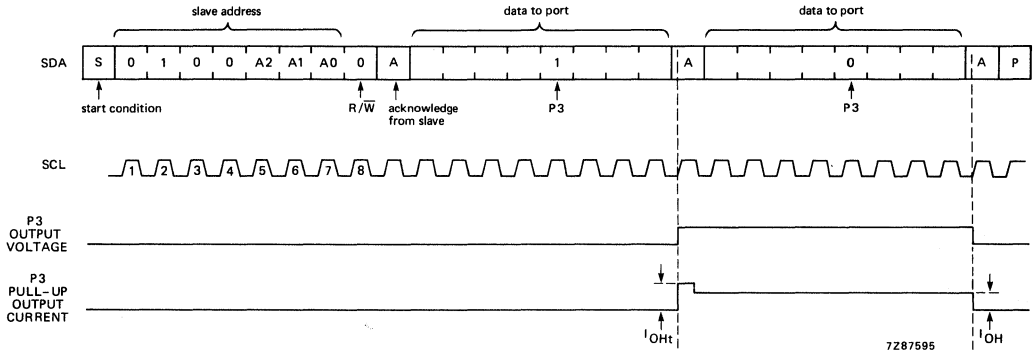


Fig. 16 Transient pull-up current I_{OHt} while P3 changes from LOW-to-HIGH and back to LOW.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range	V_{DD}		−0,5 to + 7 V
Input voltage range (any pin)	V_I		V_{SS}−0,5 to V_{DD} + 0,5 V
D.C. current into any input	$\pm I_I$	max.	20 mA
D.C. current into any output	$\pm I_O$	max.	25 mA
V_{DD} or V_{SS} current	$\pm I_{DD}$; I_{SS}	max.	100 mA
Total power dissipation	P_{tot}	max.	400 mW
Power dissipation per output	P_o	max.	100 mW
Storage temperature range	T_{stg}		−65 to + 150 °C
Operating ambient temperature range	T_{amb}		−40 to + 85 °C

DEVELOPMENT DATA

CHARACTERISTICS

V_{DD} = 2,5 to 6 V; V_{SS} = 0 V; T_{amb} = −40 to + 85 °C unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply (pin 16)					
Supply voltage	V_{DD}	2,5	–	6	V
Supply current					
at V_{DD} = 6 V; no load, inputs at V_{DD}, V_{SS}					
operating; (SCL = 100 kHz)	I_{DD}	–	40	100	μA
standby	I_{DDO}	–	1,5	10	μA
Power-on reset voltage level (note 1)	V_{REF}	–	1,3	2,4	V
Input SCL; input/output SDA (pins 14; 15)					
Input voltage LOW	V_{IL}	−0,5 V	–	$0,3V_{DD}$	V
Input voltage HIGH	V_{IH}	$0,7V_{DD}$	–	V_{DD} + 0,5 V	V
Output current LOW					
at V_{OL} = 0,4 V	I_{OL}	3	–	–	mA
Input/Output leakage current	$\|I_L\|$	–	–	100	nA
Clock frequency (see Fig. 8)	f_{SCL}	–	–	100	kHz
Tolerable spike width					
at SCL and SDA input	t_s	–	–	100	ns
Input capacitance (SCL, SDA)					
at $V_I = V_{SS}$	C_I	–	–	7	pF
I/O ports (pins 4 to 7; 9 to 12)					
Input voltage LOW	V_{IL}	−0,5 V	–	$0,3V_{DD}$	V
Input voltage HIGH	V_{IH}	$0,7V_{DD}$	–	V_{DD} + 0,5 V	V
Maximum allowed input current					
through protection diode					
at $V_I \geqslant V_{DD}$ or $\leqslant V_{SS}$	$\pm I_{IHL}$	–	–	400	μA
Output current LOW					
at V_{OL} = 1 V; V_{DD} = 5 V	I_{OL}	10	30	–	mA
Output current HIGH					
at $V_{OH} = V_{SS}$ (current source only)	$-I_{OH}$	30	100	300	μA
Transient pull-up current HIGH					
during acknowledge (see Fig. 16)					
at $V_{OH} = V_{SS}$	$-I_{OHt}$	–	0,5	–	mA
Input/Output capacitance	$C_{I/O}$	–	–	10	pF
Port timing; $C_L \leqslant 100$ pF (see Figs 12 and 13)					
Output data valid	t_{pv}	–	–	4	μs
Input data set-up	t_{ps}	0	–	–	μs
Input data hold	t_{ph}	4	–	–	μs

parameter	symbol	min.	typ.	max.	unit
Interrupt $\overline{INT}$ (pin 13)					
Output current LOW at V_{OL} = 0,4 V	I_{OL}	1,6	–	–	mA
Output current HIGH at $V_{OH} = V_{DD}$	$\|I_{OH}\|$	–	–	100	nA
$\overline{INT}$ timing; $C_L \leqslant 100$ pF (see Fig. 13)					
Input data valid	t_{iv}	–	–	4	μs
Reset delay	t_{ir}	–	–	4	μs
Select inputs A0, A1, A2 (pins 1 to 3)					
Input voltage LOW	V_{IH}	−0,5 V	–	$0{,}3V_{DD}$	V
Input voltage HIGH	V_{IH}	$0{,}7V_{DD}$	–	V_{DD} + 0,5 V	V
Input leakage current at $V_I = V_{DD}$ or V_{SS}	$\|I_L\|$	–	–	100	nA

DEVELOPMENT DATA

Note 1

The power-on reset circuit resets the I²C bus logic with $V_{DD} < V_{REF}$ and sets all ports to logic 1 (input mode with current source to V_{DD}).

Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

UNIVERSAL LCD DRIVER FOR LOW MULTIPLEX RATES

GENERAL DESCRIPTION

The PCF8576 is a peripheral device which interfaces to almost any liquid crystal display (LCD) having low multiplex rates. It generates the drive signals for any static or multiplexed LCD containing up to four backplanes and up to 40 segments and can easily be cascaded for larger LCD applications. The PCF8576 is compatible with most microprocessors and communicates via a two-line bidirectional bus (I^2C). Communication overheads are minimized by a display RAM with auto-incremented addressing, by hardware subaddressing and by display memory switching (static and duplex drive modes).

Features

- Single-chip LCD controller/driver
- Selectable backplane drive configuration: static or 2/3/4 backplane multiplexing
- Selectable display bias configuration: static, 1/2 or 1/3
- Internal LCD bias generation with voltage-follower buffers
- 40 segment drives: up to twenty 8-segment numeric characters; up to ten 15-segment alphanumeric characters; or any graphics of up to 160 elements
- 40 x 4-bit RAM for display data storage
- Auto-incremented display data loading across device subaddress boundaries
- Display memory bank switching in static and duplex drive modes
- Versatile blinking modes
- LCD and logic supplies may be separated
- Wide power supply range: from 2 V for low-threshold LCDs and up to 9 V for guest-host LCDs and high-threshold (automobile) twisted nematic LCDs
- Low power consumption
- Power-saving mode for extremely low power consumption in battery-operated and telephone applications
- I^2C bus interface
- TTL/CMOS compatible
- Compatible with any 4-bit, 8-bit or 16-bit microprocessors
- May be cascaded for large LCD applications (up to 2560 segments possible)
- Optimized pinning for single plane wiring in both single and multiple PCF8576 applications
- Space-saving 56-lead plastic mini-pack (VSO-56)
- Very low external component count (at most one resistor, even in multiple device applications)
- Compatible with chip-on-glass technology
- Manufactured in silicon gate CMOS process

PACKAGE OUTLINES

PCF8576T: 56-lead mini-pack; plastic (VSO-56; SOT-190).
PCF8576U: uncased chip in tray

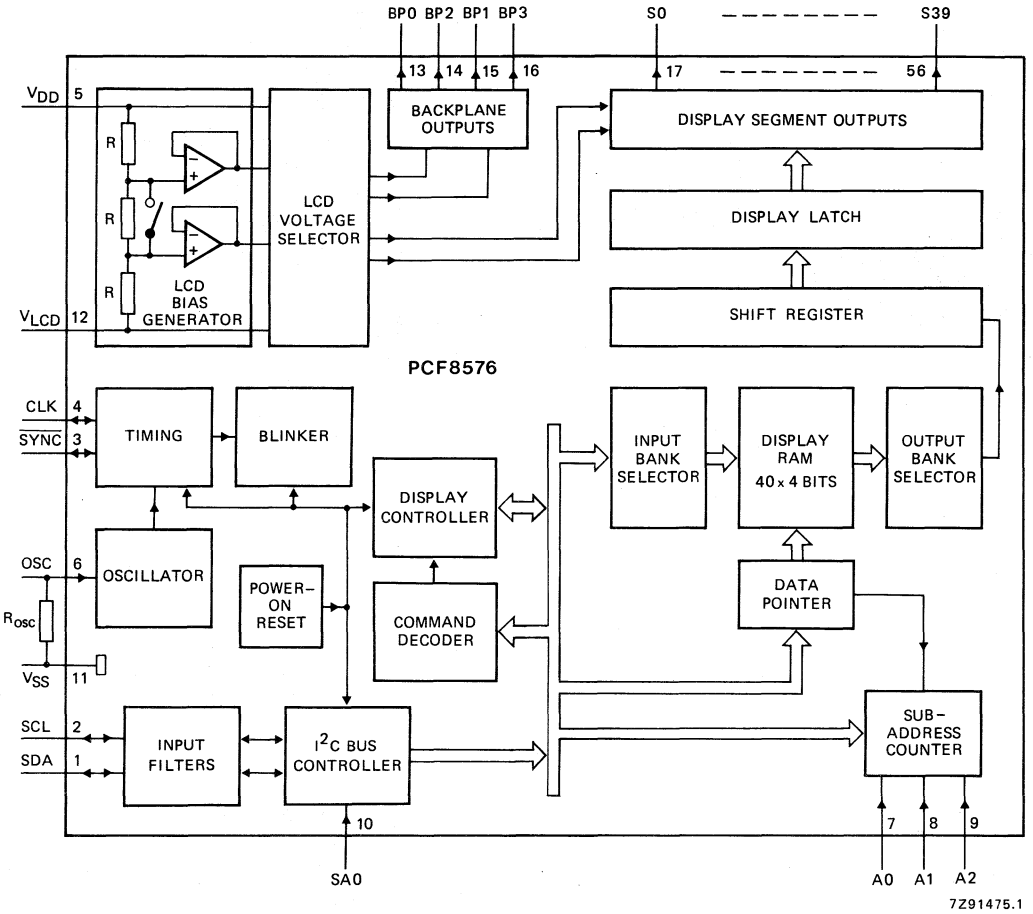


Fig. 1 Block diagram.

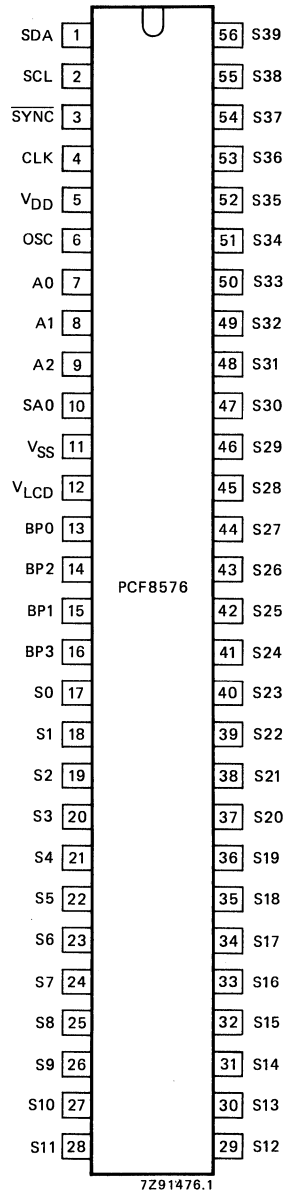


Fig. 2 Pinning diagram.

PINNING

1	SDA	I^2C bus data input/output
2	SCL	I^2C bus clock input/output
3	$\overline{SYNC}$	cascade synchronization input/output
4	CLK	external clock input/output
5	V_{DD}	positive supply voltage
6	OSC	oscillator input
7	A0	I^2C bus subaddress inputs
8	A1	
9	A2	
10	SA0	I^2C bus slave address bit 0 input
11	V_{SS}	logic ground
12	V_{LCD}	LCD supply voltage
13	BP0	LCD backplane outputs
14	BP2	
15	BP1	
16	BP3	
17 to 56	S0 to S39	LCD segment outputs

FUNCTIONAL DESCRIPTION

The PCF8576 is a versatile peripheral device designed to interface any microprocessor to a wide variety of LCDs. It can directly drive any static or multiplexed LCD containing up to four backplanes and up to 40 segments. The display configurations possible with the PCF8576 depend on the number of active backplane outputs required; a selection of display configurations is given in Table 1.

Table 1 Selection of display configurations

active back-plane outputs	no. of segments	7-segment numeric	14-segment alphanumeric	dot matrix
4	160	20 digits + 20 indicator symbols	10 characters + 20 indicator symbols	160 dots (4 x 40)
3	120	15 digits + 15 indicator symbols	8 characters + 8 indicator symbols	120 dots (3 x 40)
2	80	10 digits + 10 indicator symbols	5 characters + 10 indicator symbols	80 dots (2 x 40)
1	40	5 digits + 5 indicator symbols	2 characters + 12 indicator symbols	40 dots

All of the display configurations given in Table 1 can be implemented in the typical system shown in Fig. 3. The host microprocessor maintains the 2-line I²C bus communication channel with the PCF8576. A resistor connected between OSC (pin 6) and V_{SS} (pin 11) controls the device clock frequency. The appropriate biasing voltages for the multiplexed LCD waveforms are generated internally. The only other connections required to complete the system are to the power supplies (V_{DD}, V_{SS} and V_{LCD}) and to the LCD panel chosen for the application.

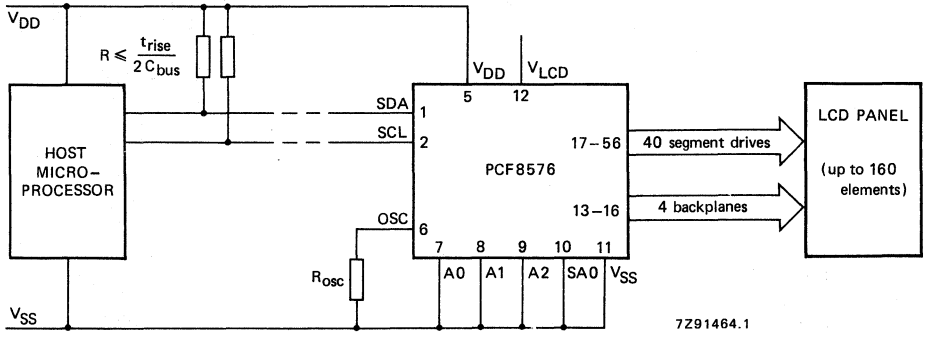


Fig. 3 Typical system configuration.

Power-on reset

At power-on the PCF8576 resets to a defined starting condition as follows:

1. All backplane outputs are set to V_{DD}.
2. All segment outputs are set to V_{DD}.
3. The drive mode '1 : 4 multiplex with 1/3 bias' is selected.
4. Blinking is switched off.
5. Input and output bank selectors are reset (as defined in Table 5).
6. The I^2C bus interface is initialized.
7. The data pointer and the subaddress counter are cleared.

Data transfers on the I^2C bus should be avoided for 1 ms following power-on to allow completion of the reset action.

LCD bias generator

The full-scale LCD voltage (V_{op}) is obtained from $V_{DD} - V_{LCD}$. The LCD voltage may be temperature compensated externally through the V_{LCD} supply to pin 12. Fractional LCD biasing voltages are obtained from an internal voltage divider of three series resistors connected between V_{DD} and V_{LCD}. The centre resistor can be switched out of circuit to provide a ½ bias voltage level for the 1 : 2 multiplex configuration.

LCD voltage selector

The LCD voltage selector coordinates the multiplexing of the LCD according to the selected LCD drive configuration. The operation of the voltage selector is controlled by MODE SET commands from the command decoder. The biasing configurations that apply to the preferred modes of operation, together with the biasing characteristics as functions of $V_{op} = V_{DD} - V_{LCD}$ and the resulting discrimination ratios (D), are given in Table 2.

Table 2 Preferred LCD drive modes: summary of characteristics

LCD drive mode	LCD bias configuration	$\frac{V_{off(rms)}}{V_{op}}$	$\frac{V_{on\ (rms)}}{V_{op}}$	$D = \frac{V_{on(rms)}}{V_{off(rms)}}$
static (1 BP)	static (2 levels)	0	1	∞
1 : 2 MUX (2 BP)	1/2 (3 levels)	$\sqrt{2}/4 = 0{,}354$	$\sqrt{10}/4 = 0{,}791$	$\sqrt{5} = 2{,}236$
1 : 2 MUX (2 BP)	1/3 (4 levels)	$1/3 = 0{,}333$	$\sqrt{5}/3 = 0{,}745$	$\sqrt{5} = 2{,}236$
1 : 3 MUX (3 BP)	1/3 (4 levels)	$1/3 = 0{,}333$	$\sqrt{33}/9 = 0{,}638$	$\sqrt{33}/3 = 1{,}915$
1 : 4 MUX (4 BP)	1/3 (4 levels)	$1/3 = 0{,}333$	$\sqrt{3}/3 = 0{,}577$	$\sqrt{3} = 1{,}732$

LCD voltage selector (continued)

A practical value for V_{op} is determined by equating $V_{off(rms)}$ with a defined LCD threshold voltage (V_{thLCD}), typically when the LCD exhibits approximately 10% contrast. In the static drive mode a suitable choice is $V_{op} \gtrapprox 3\,V_{thLCD}$.
Multiplex drive ratios of 1 : 3 and 1 : 4 with 1/2 bias are possible but the discrimination and hence the contrast ratios are smaller ($\sqrt{3} = 1{,}732$ for 1 : 3 multiplex or $\sqrt{21}/3 = 1{,}528$ for 1 : 4 multiplex).
The advantage of these modes is a reduction of the LCD full scale voltage V_{op} as follows:

1 : 3 multiplex (1/2 bias) : $V_{op} = \sqrt{6}\,V_{off(rms)} = 2{,}449\,V_{off(rms)}$

1 : 4 multiplex (1/2 bias) : $V_{op} = 4\sqrt{3}/3\,V_{off(rms)} = 2{,}309\,V_{off(rms)}$

These compare with $V_{op} = 3\,V_{off(rms)}$ when 1/3 bias is used.

LCD drive mode waveforms

The static LCD drive mode is used when a single backplane is provided in the LCD. Backplane and segment drive waveforms for this mode are shown in Fig. 4.

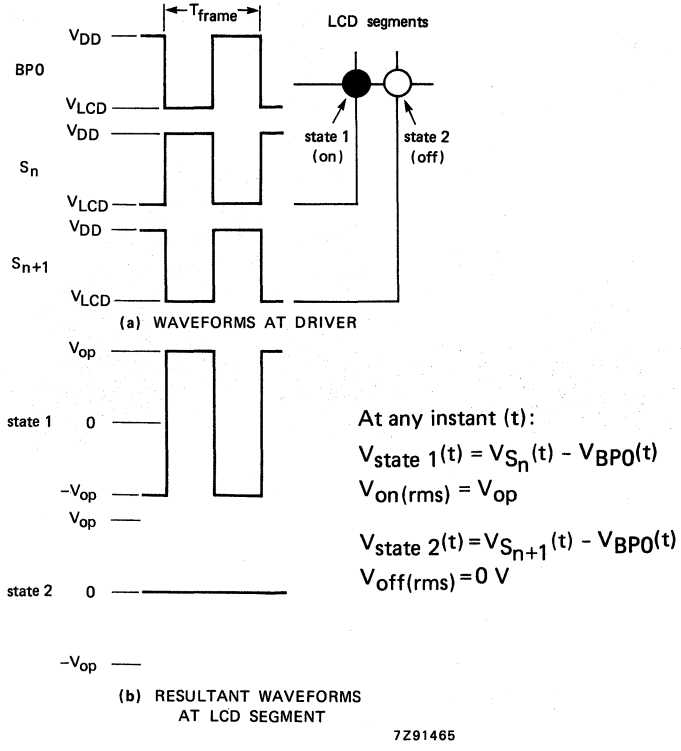


Fig. 4 Static drive mode waveforms: $V_{op} = V_{DD} - V_{LCD}$.

When two backplanes are provided in the LCD the 1 : 2 multiplex drive mode applies. The PCF8576 allows use of 1/2 or 1/3 bias in this mode as shown in Figs 5 and 6.

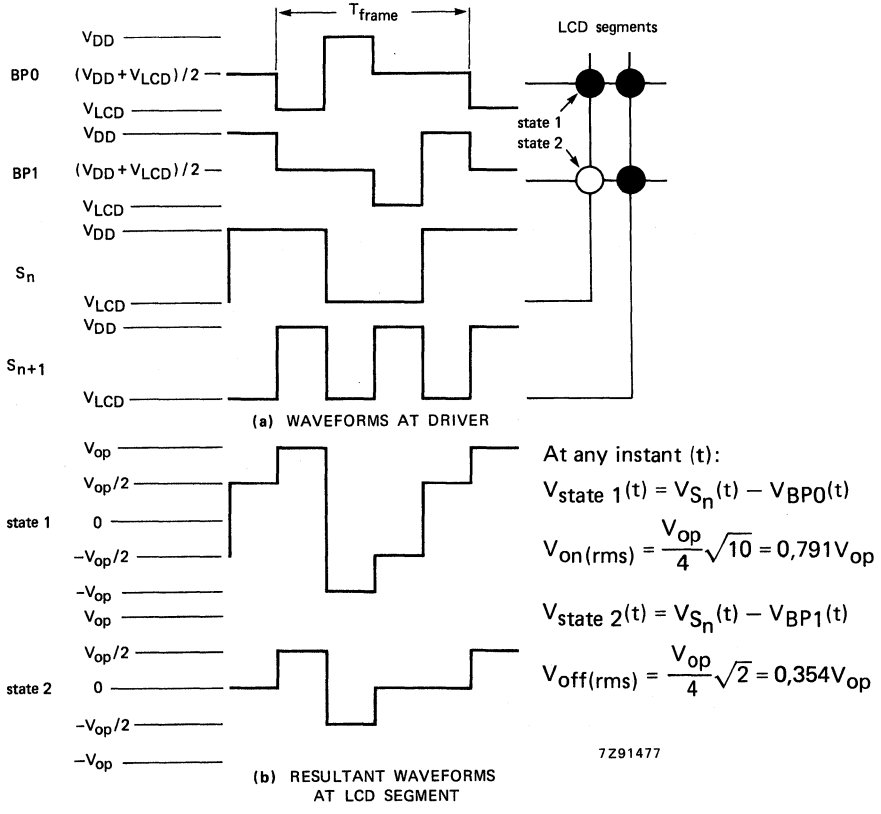


Fig. 5 Waveforms for 1 : 2 multiplex drive mode with 1/2 bias: $V_{op} = V_{DD} - V_{LCD}$.

LCD drive mode waveforms (continued)

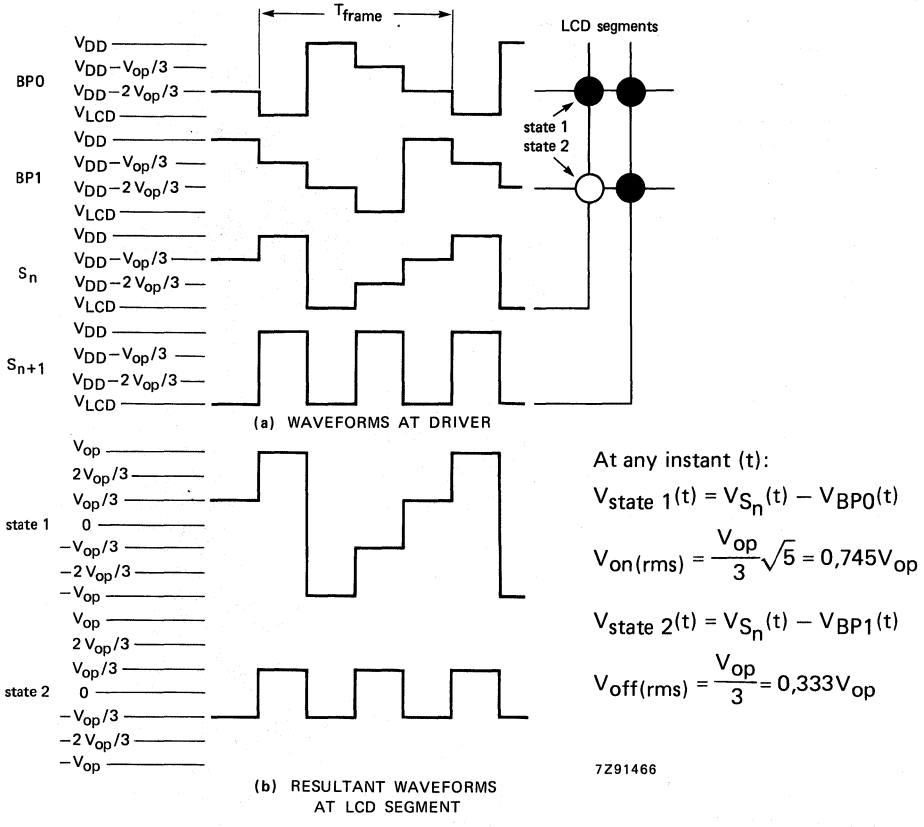


Fig. 6 Waveforms for 1 : 2 multiplex drive mode with 1/3 bias: $V_{op} = V_{DD} - V_{LCD}$.

The backplane and segment drive wavefront for the 1 : 3 multiplex drive mode (three LCD backplanes) and for the 1 : 4 multiplex drive mode (four LCD backplanes) are shown in Figs 7 and 8 respectively.

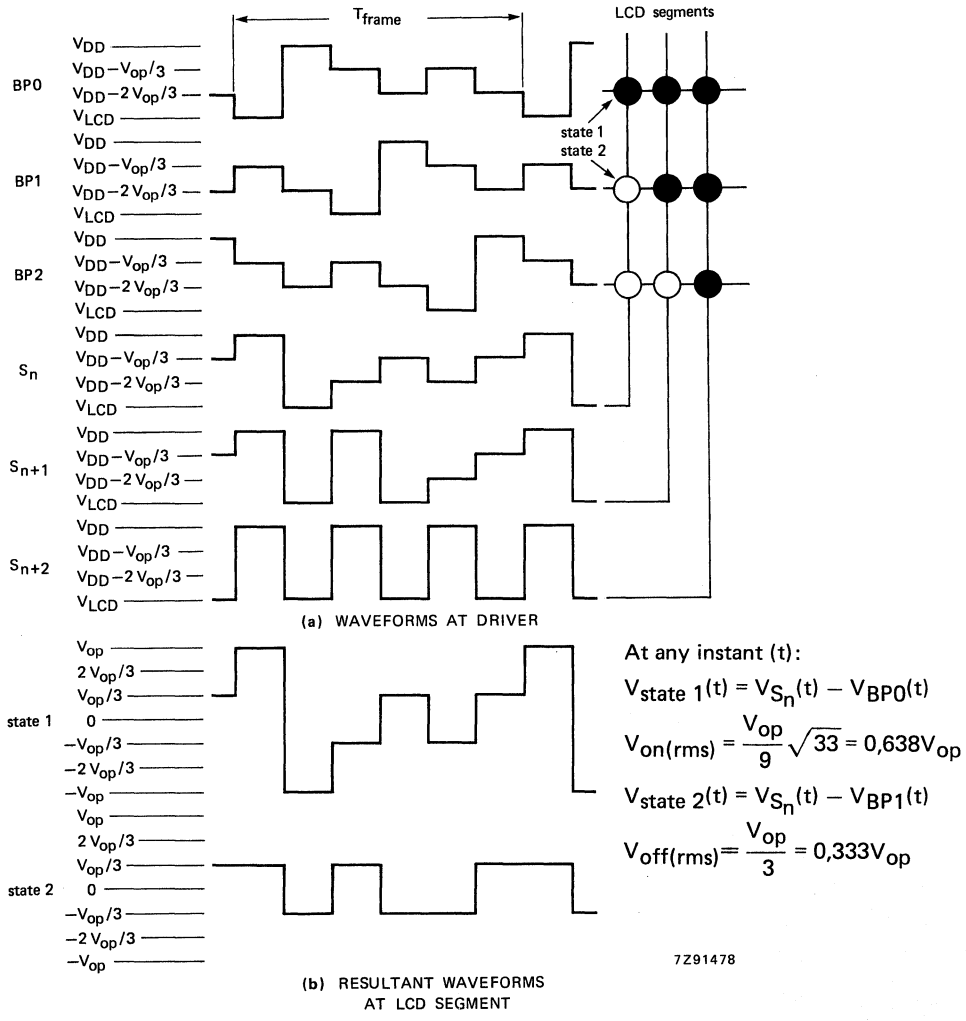


Fig. 7 Waveforms for 1 : 3 multiplex drive mode: $V_{op} = V_{DD} - V_{LCD}$.

LCD drive mode waveforms (continued)

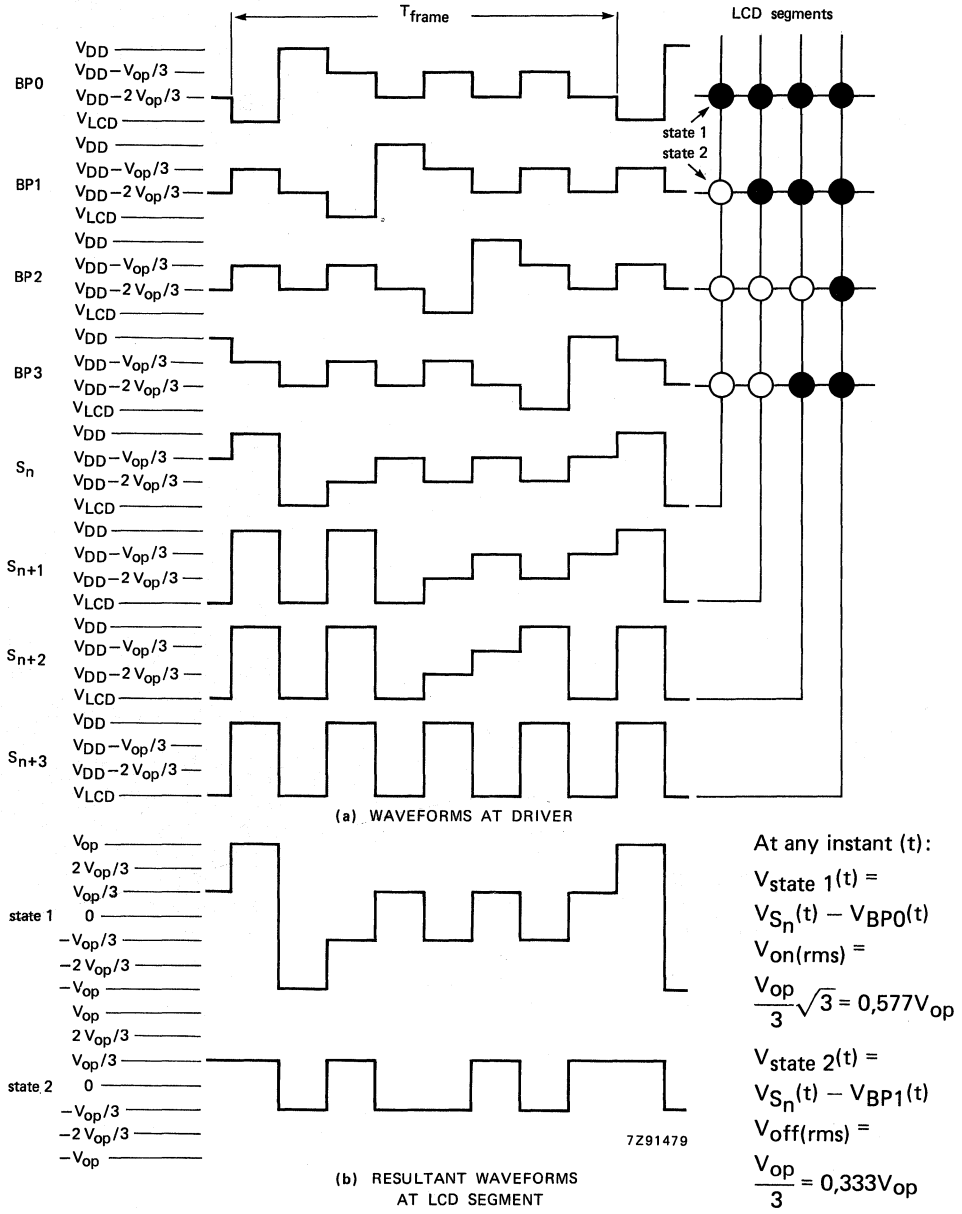


Fig. 8 Waveforms for 1 : 4 multiplex drive mode: $V_{op} = V_{DD} - V_{LCD}$.

Oscillator

Internal clock

The internal logic and the LCD drive signals of the PCF8576 are timed either by the built-in oscillator or from an external clock. When the internal oscillator is used, frequency control is performed by a single resistor connected between OSC (pin 6) and V_{SS} (pin 11) as shown in Fig. 9. In this case, the output from CLK (pin 4) provides the clock signal for cascaded PCF8576s in the system.

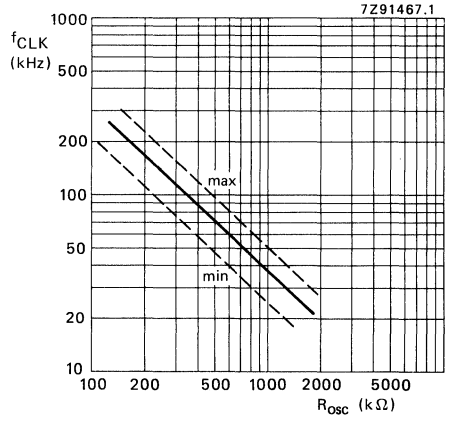


Fig. 9 Oscillator frequency as a function of R_{osc}: $f_{CLK} \approx (3{,}4 \times 10^7 / R_{osc})$ kHz·Ω.

External clock

The condition for external clock is made by tying OSC (pin 6) to V_{DD}; CLK (pin 4) then becomes the external clock input.

The clock frequency (f_{CLK}) determines the LCD frame frequency and the maximum rate for data reception from the I^2C bus. To allow I^2C bus transmissions at their maximum data rate of 100 kHz, f_{CLK} should be chosen to be above 125 kHz.

A clock signal must always be supplied to the device; removing the clock may freeze the LCD in a d.c. state.

Timing

The timing of the PCF8576 organizes the internal data flow of the device. This includes the transfer of display data from the display RAM to the display segment outputs. In cascaded applications, the synchronization signal $\overline{SYNC}$ maintains the correct timing relationship between the PCF8576s in the system. The timing also generates the LCD frame frequency which it derives as an integer multiple of the clock frequency (Table 3). The frame frequency is set by the choice of value for R_{osc} when internal clock is used, or by the frequency applied to pin 4 when external clock is used.

Table 3 LCD frame frequencies

PCF8576 mode	recommended R_{osc} (kΩ)	f_{frame}	nominal f_{frame} (Hz)
normal mode	180	$f_{CLK}/2880$	64
power-saving mode	1200	$f_{CLK}/480$	64

Timing (continued)

The ratio between the clock frequency and the LCD frame frequency depends on the mode in which the device is operating. In the normal mode, R_{osc} = 180 kΩ will result in the nominal frame frequency. In the power-saving mode the reduction ratio is six times smaller; this allows the clock frequency to be reduced by a factor of six and for the same frame frequency R_{osc} will be 1,2 MΩ. The reduced clock frequency and the increased value of R_{osc} together contribute to a significant reduction in power dissipation. The lower clock frequency has the disadvantage of increasing the response time when large amounts of display data are transmitted on the I^2C bus. When a device is unable to 'digest' a display data byte before the next one arrives, it holds the SCL line LOW until the first display data byte is stored. This slows down the transmission rate of the I^2C bus but no data loss occurs.

Display latch

The display latch holds the display data while the corresponding multiplex signals are generated. There is a one-to-one relationship between the data in the display latch, the LCD segment outputs and one column of the display RAM.

Shift register

The shift register serves to transfer display information from the display RAM to the display latch while previous data are displayed.

Segment outputs

The LCD drive section includes 40 segment outputs S0 to S39 (pins 17 to 56) which should be connected directly to the LCD. The segment output signals are generated in accordance with the multiplexed backplane signals and with the data resident in the display latch. When less than 40 segment outputs are required the unused segment outputs should be left open.

Backplane outputs

The LCD drive section includes four backplane outputs BP0 to BP3 which should be connected directly to the LCD. The backplane output signals are generated in accordance with the selected LCD drive mode. If less than four backplane outputs are required the unused outputs can be left open. In the 1 : 3 multiplex drive mode BP3 carries the same signal as BP1, therefore these two adjacent outputs can be tied together to give enhanced drive capabilities. In the 1 : 2 multiplex drive mode BP0 and BP2, BP1 and BP3 respectively carry the same signals and may also be paired to increase the drive capabilities. In the static drive mode the same signal is carried by all four backplane outputs and they can be connected in parallel for very high drive requirements.

Display RAM

The display RAM is a static 40 x 4-bit RAM which stores LCD data. A logic 1 in the RAM bit-map indicates the 'on' state of the corresponding LCD segment; similarly, a logic 0 indicates the 'off' state. There is a one-to-one correspondence between the RAM addresses and the segment outputs, and between the individual bits of a RAM word and the backplane outputs. The first RAM column corresponds to the 40 segments operated with respect to backplane BP0 (Fig. 10). In multiplexed LCD applications the segment data of the second, third and fourth column of the display RAM are time-multiplexed with BP1, BP2 and BP3 respectively.

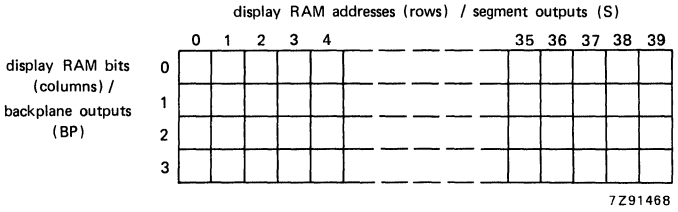


Fig. 10 Display RAM bit-map showing direct relationship between display RAM addresses and segment outputs, and between bits in a RAM word and backplane outputs.

When display data are transmitted to the PCF8576 the display bytes received are stored in the display RAM according to the selected LCD drive mode. To illustrate the filling order, an example of a 7-segment numeric display showing all drive modes is given in Fig. 11; the RAM filling organization depicted applies equally to other LCD types.

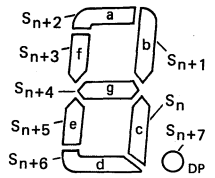
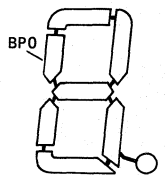
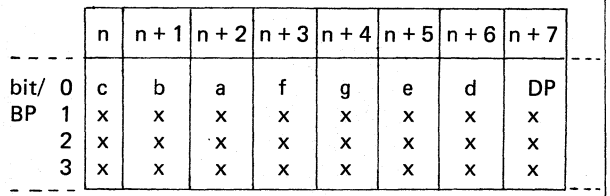
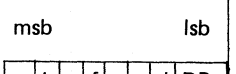
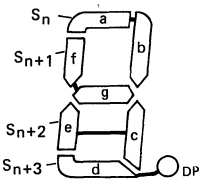
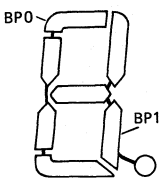
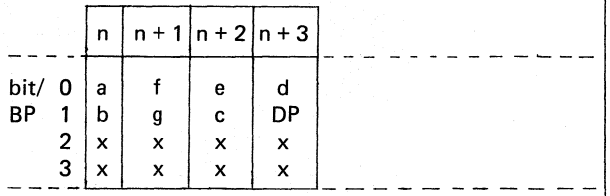
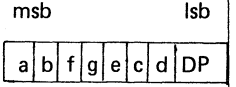
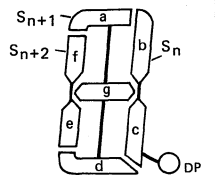
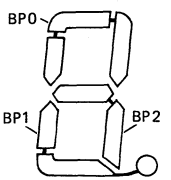
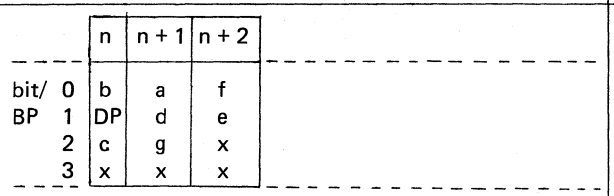
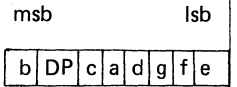
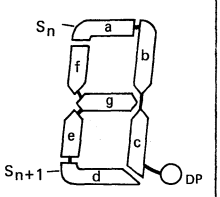
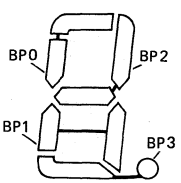
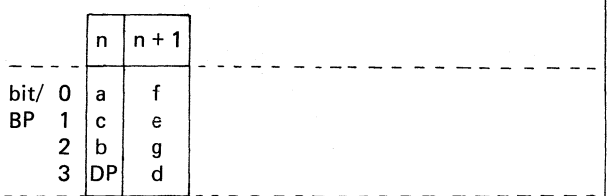
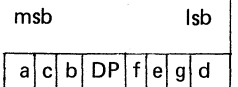
With reference to Fig. 11, in the static drive mode the eight transmitted data bits are placed in bit 0 of eight successive display RAM addresses. In the 1 : 2 multiplex drive mode the eight transmitted data bits are placed in bits 0 and 1 of four successive display RAM addresses. In the 1 : 3 multiplex drive mode these bits are placed in bits 0, 1 and 2 of three successive addresses, with bit 2 of the third address left unchanged. This last bit may, if necessary, be controlled by an additional transfer to this address but care should be taken to avoid overriding adjacent data because full bytes are always transmitted. In the 1 : 4 multiplex drive mode the eight transmitted data bits are placed in bits 0, 1, 2 and 3 of two successive display RAM addresses.

Data pointer

The addressing mechanism for the display RAM is realized using the data pointer. This allows the loading of an individual display data byte, or a series of display data bytes, into any location of the display RAM. The sequence commences with the initialization of the data pointer by the LOAD DATA POINTER command. Following this, an arriving data byte is stored starting at the display RAM address indicated by the data pointer thereby observing the filling order shown in Fig. 11. The data pointer is automatically incremented according to the LCD configuration chosen. That is, after each byte is stored, the contents of the data pointer are incremented by eight (static drive mode), by four (1 : 2 multiplex drive mode), by three (1 : 3 multiplex drive mode) or by two (1 : 4 multiplex drive mode).

Subaddress counter

The storage of display data is conditioned by the contents of the subaddress counter. Storage is allowed to take place only when the contents of the subaddress counter agree with the hardware subaddress applied to A0, A1 and A2 (pins 7, 8, and 9). The subaddress counter value is defined by the DEVICE SELECT command. If the contents of the subaddress counter and the hardware subaddress do not agree then data storage is inhibited but the data pointer is incremented as if data storage had taken place. The subaddress counter is also incremented when the data pointer overflows.

drive mode	LCD segments	LCD backplanes	display RAM filling order	transmitted display byte
static				
1 : 2 multiplex				
1 : 3 multiplex				
1 : 4 multiplex				

	n	n + 1	n + 2	n + 3	n + 4	n + 5	n + 6	n + 7
bit/ 0	c	b	a	f	g	e	d	DP
BP 1	x	x	x	x	x	x	x	x
2	x	x	x	x	x	x	x	x
3	x	x	x	x	x	x	x	x

	n	n + 1	n + 2	n + 3
bit/ 0	a	f	e	d
BP 1	b	g	c	DP
2	x	x	x	x
3	x	x	x	x

	n	n + 1	n + 2
bit/ 0	b	a	f
BP 1	DP	d	e
2	c	g	x
3	x	x	x

	n	n + 1
bit/ 0	a	f
BP 1	c	e
2	b	g
3	DP	d

msb							lsb
c	b	a	f	g	e	d	DP

msb							lsb
a	b	f	g	e	c	d	DP

msb							lsb
b	DP	c	a	d	g	f	e

msb							lsb
a	c	b	DP	f	e	g	d

Fig. 11 Relationships between LCD layout, drive mode, display RAM filling order and display data transmitted over the I²C bus (x = data bit unchanged).

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Subaddress counter (continued)

The storage arrangements described lead to extremely efficient data loading in cascaded applications. When a series of display bytes are being sent to the display RAM, automatic wrap-over to the next PCF8576 occurs when the last RAM address is exceeded. Subaddressing across device boundaries is successful even if the change to the next device in the cascade occurs within a transmitted character (such as during the 14th display data byte transmitted in 1 : 3 multiplex mode).

Output bank selector

This selects one of the four bits per display RAM address for transfer to the display latch. The actual bit chosen depends on the particular LCD drive mode in operation and on the instant in the multiplex sequence. In 1 : 4 multiplex, all RAM addresses of bit 0 are the first to be selected, these are followed by the contents of bit 1, bit 2 and then bit 3. Similarly in 1 : 3 multiplex, bits 0, 1 and 2 are selected sequentially. In 1 : 2 multiplex, bits 0 then 1 are selected and, in the static mode, bit 0 is selected.

The PCF8576 includes a RAM bank switching feature in the static and 1 : 2 multiplex drive modes. In the static drive mode, the BANK SELECT command may request the contents of bit 2 to be selected for display instead of bit 0 contents. In the 1 : 2 drive mode, the contents of bits 2 and 3 may be selected instead of bits 0 and 1. This gives the provision for preparing display information in an alternative bank and to be able to switch to it once it is assembled.

Input bank selector

The input bank selector loads display data into the display RAM according to the selected LCD drive configuration. Display data can be loaded in bit 2 in static drive mode or in bits 2 and 3 in 1 : 2 drive mode by using the BANK SELECT command. The input bank selector functions independently of the output bank selector.

Blinker

The display blinking capabilities of the PCF8576 are very versatile. The whole display can be blinked at frequencies selected by the BLINK command. The blinking frequencies are integer multiples of the clock frequency; the ratios between the clock and blinking frequencies depend on the mode in which the device is operating, as shown in Table 4.

An additional feature is for an arbitrary selection of LCD segments to be blinked. This applies to the static and 1 : 2 LCD drive modes and can be implemented without any communication overheads. By means of the output bank selector, the displayed RAM banks are exchanged with alternate RAM banks at the blinking frequency. This mode can also be specified by the BLINK command.

In the 1 : 3 and 1 : 4 multiplex modes, where no alternate RAM bank is available, groups of LCD segments can be blinked by selectively changing the display RAM data at fixed time intervals.

If the entire display is to be blinked at a frequency other than the nominal blinking frequency, this can be effectively performed by resetting and setting the display enable bit E at the required rate using the MODE SET command.

Blinker (continued)

Table 4 Blinking frequencies

blinking mode	normal operating mode ratio	power-saving mode ratio	nominal blinking frequency f_{blink} (Hz)
off	–	–	blinking off
2 Hz	$f_{CLK}/92160$	$f_{CLK}/15360$	2
1 Hz	$f_{CLK}/184320$	$f_{CLK}/30720$	1
0,5 Hz	$f_{CLK}/368640$	$f_{CLK}/61440$	0,5

CHARACTERISTICS OF THE I²C BUS

The I²C bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals.

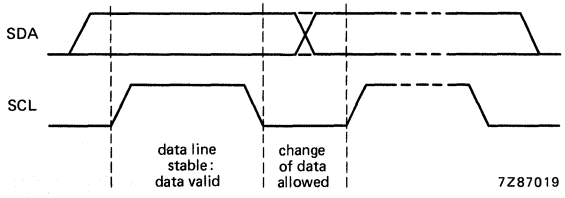


Fig. 12 Bit transfer.

Start and stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line while the clock is HIGH is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the stop condition (P).

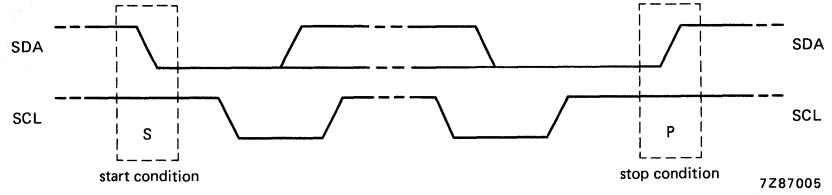


Fig. 13 Definition of start and stop conditions.

System configuration

A device generating a message is a "transmitter", a device receiving a message is a "receiver". The device that controls the message is the "master" and the devices which are controlled by the master are the "slaves".

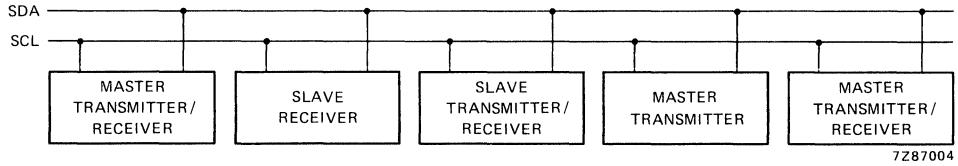


Fig. 14 System configuration.

Acknowledge

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is not limited. Each byte is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse, set up and hold times must be taken into account. A master receiver must signal an end of data to the transmitter by *not* generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

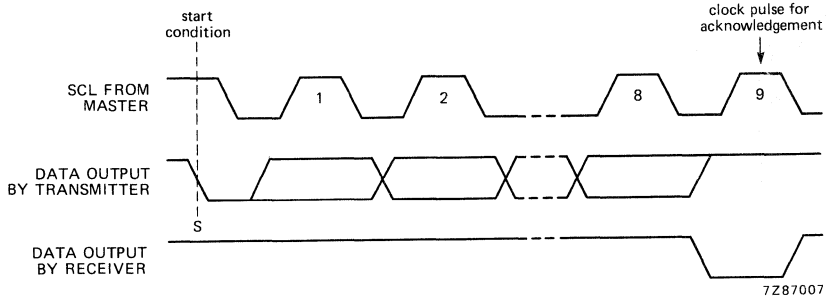


Fig. 15 Acknowledgement on the I^2C bus.

Note

The general characteristics and detailed specification of the I^2C bus are described in a separate data sheet (serial data buses) in handbook: ICs for digital systems in radio, audio and video equipment.

PCF8576 I²C bus controller

The PCF8576 acts as an I²C slave receiver. It does not initiate I²C bus transfers or transmit data to an I²C master receiver. The only data output from the PCF8576 are the acknowledge signals of the selected devices. Device selection depends on the I²C bus slave address, on the transferred command data and on the hardware subaddress.

In single device applications, the hardware subaddress inputs A0, A1 and A2 are normally tied to V_{SS} which defines the hardware subaddress 0. In multiple device applications A0, A1 and A2 are tied to V_{SS} or V_{DD} according to a binary coding scheme such that no two devices with a common I²C slave address have the same hardware subaddress.

In the power-saving mode it is possible that the PCF8576 is not able to keep up with the highest transmission rates when large amounts of display data are transmitted. If this situation occurs, the PCF8576 forces the SCL line LOW until its internal operations are completed. This is known as the 'clock synchronization feature' of the I²C bus and serves to slow down fast transmitters. Data loss does not occur.

Input filters

To enhance noise immunity in electrically adverse environments, RC low-pass filters are provided on the SDA and SCL lines.

I²C bus protocol

Two I²C bus slave addresses (0111000 and 0111001) are reserved for PCF8576. The least-significant bit of the slave address that a PCF8576 will respond to is defined by the level tied at its input SA0 (pin 10). Therefore, two types of PCF8576 can be distinguished on the same I²C bus which allows:

(a) up to 16 PCF8576s on the same I²C bus for very large LCD applications;

(b) the use of two types of LCD multiplex on the same I²C bus.

The I²C bus protocol is shown in Fig. 16. The sequence is initiated with a start condition (S) from the I²C bus master which is followed by one of the two PCF8576 slave addresses available. All PCF8576s with the corresponding SA0 level acknowledge in parallel the slave address but all PCF8576s with the alternative SA0 level ignore the whole I²C bus transfer. After acknowledgement, one or more command bytes (m) follow which define the status of the addressed PCF8576s. The last command byte is tagged with a cleared most-significant bit, the continuation bit C. The command bytes are also acknowledged by all addressed PCF8576s on the bus.

After the last command byte, a series of display data bytes (n) may follow. These display data bytes are stored in the display RAM at the address specified by the data pointer and the subaddress counter. Both data pointer and subaddress counter are automatically updated and the data are directed to the intended PCF8576 device. The acknowledgement after each byte is made only by the (A0, A1, A2) addressed PCF8576. After the last display byte, the I²C bus master issues a stop condition (P).

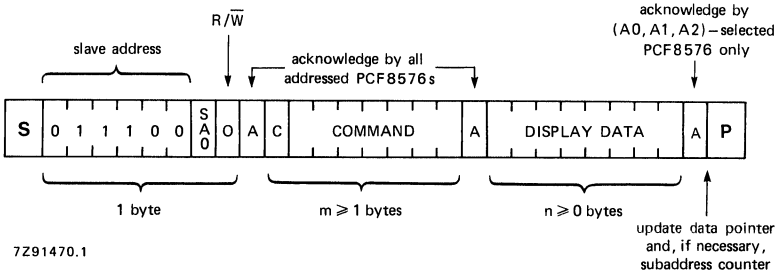


Fig. 16 I²C bus protocol.

Command decoder

The command decoder identifies command bytes that arrive on the I²C bus. All available commands carry a continuation bit C in their most-significant bit position (Fig. 17). When this bit is set, it indicates that the next byte of the transfer to arrive will also represent a command. If the bit is reset, it indicates the last command byte of the transfer. Further bytes will be regarded as display data.

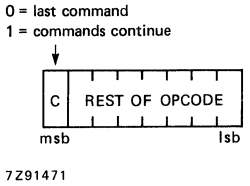


Fig. 17 General format of command byte.

The five commands available to the PCF8576 are defined in Table 5.

Command decoder (continued)

Table 5 Definition of PCF8576 commands

command/opcode	options	description
MODE SET C 1 0 LP E B M1 M0	LCD drive mode: bits M1 M0 static (1 BP): 0 1 1 : 2 MUX (2 BP): 1 0 1 : 3 MUX (3 BP): 1 1 1 : 4 MUX (4 BP): 0 0	Defines LCD drive mode
	LCD bias: bit B 1/3 bias: 0 1/2 bias: 1	Defines LCD bias configuration
	display status: bit E disabled (blank): 0 enabled: 1	Defines display status The possibility to disable the display allows implementation of blinking under external control
	mode: bit LP normal mode: 0 power-saving mode: 1	Defines power dissipation mode
LOAD DATA POINTER C 0 P5 P4 P3 P2 P1 P0	bits P5 P4 P3 P2 P1 P0 6-bit binary value of 0 to 39	Six bits of immediate data, bits P5 to P0, are transferred to the data pointer to define one of forty display RAM addresses
DEVICE SELECT C 1 1 0 0 A2 A1 A0	bits A0 A1 A2 3-bit binary value of 0 to 7	Three bits of immediate data, bits A0 to A2, are transferred to the subaddress counter to define one of eight hardware subaddresses

<table>
<tr><th>command/opcode</th><th>options</th><th>description</th></tr>
<tr><td>BANK SELECT
<table><tr><td>C</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>I</td><td>O</td></tr></table></td><td><table><tr><td>static</td><td>1 : 2 MUX</td><td>bit I</td></tr><tr><td>RAM bit 0
RAM bit 2</td><td>RAM bits 0, 1
RAM bits 2, 3</td><td>0
1</td></tr></table><table><tr><td>static</td><td>1 : 2 MUX</td><td>bit O</td></tr><tr><td>RAM bit 0
RAM bit 2</td><td>RAM bits 0, 1
RAM bits 2, 3</td><td>0
1</td></tr></table></td><td>Defines input bank selection (storage of arriving display data)

Defines output bank selection (retrieval of LCD display data)

The BANK SELECT command has no effect in 1 : 3 and 1 : 4 multiplex drive modes</td></tr>
<tr><td>BLINK
<table><tr><td>C</td><td>1</td><td>1</td><td>1</td><td>0</td><td>A</td><td>BF1</td><td>BF0</td></tr></table></td><td><table><tr><td>blink frequency</td><td>bits BF1</td><td>BF0</td></tr><tr><td>off
2 Hz
1 Hz
0,5 Hz</td><td>0
0
1
1</td><td>0
1
0
1</td></tr></table><table><tr><td>blink mode</td><td>bit A</td></tr><tr><td>normal blinking
alternation blinking</td><td>0
1</td></tr></table></td><td>Defines the blinking frequency

Selects the blinking mode; normal operation with frequency set by bits BF1, BF0, or blinking by alternation of display RAM banks. Alternation blinking does not apply in 1 : 3 and 1 : 4 multiplex drive modes</td></tr>
</table>

Display controller

The display controller executes the commands identified by the command decoder. It contains the status registers of the PCF8576 and coordinates their effects. The controller is also responsible for loading display data into the display RAM as required by the filling order.

Cascaded operation

In large display configurations, up to 16 PCF8576s can be distinguished on the same I²C bus by using the 3-bit hardware subaddress (A0, A1, A2) and the programmable I²C slave address (SA0). It is also possible to cascade up to 16 PCF8576s. When cascaded, several PCF8576s are synchronized so that they can share the backplane signals from one of the devices in the cascade. Such an arrangement is cost-effective in large LCD applications since the backplane outputs of only one device need to be through-plated to the backplane electrodes of the display. The other PCF8576s of the cascade contribute additional segment outputs but their backplane outputs are left open (Fig. 18).

The $\overline{\text{SYNC}}$ line is provided to maintain the correct synchronization between all cascaded PCF8576s. This synchronization is guaranteed after the power-on reset. The only time that $\overline{\text{SYNC}}$ is likely to be needed is if synchronization is accidently lost (e.g. by noise in adverse electrical environments; or by the definition of a multiplex mode when PCF8576s with differing SA0 levels are cascaded). $\overline{\text{SYNC}}$ is organized as an input/output pin; the output section being realized as an open-drain driver with an internal pull-up resistor. A PCF8576 asserts the $\overline{\text{SYNC}}$ line at the onset of its last active backplane signal and monitors the $\overline{\text{SYNC}}$ line at all other times. Should synchronization in the cascade be lost, it will be restored by the first PCF8576 to assert $\overline{\text{SYNC}}$. The timing relationships between the backplane waveforms and the $\overline{\text{SYNC}}$ signal for the various drive modes of the PCF8576 are shown in Fig. 19.

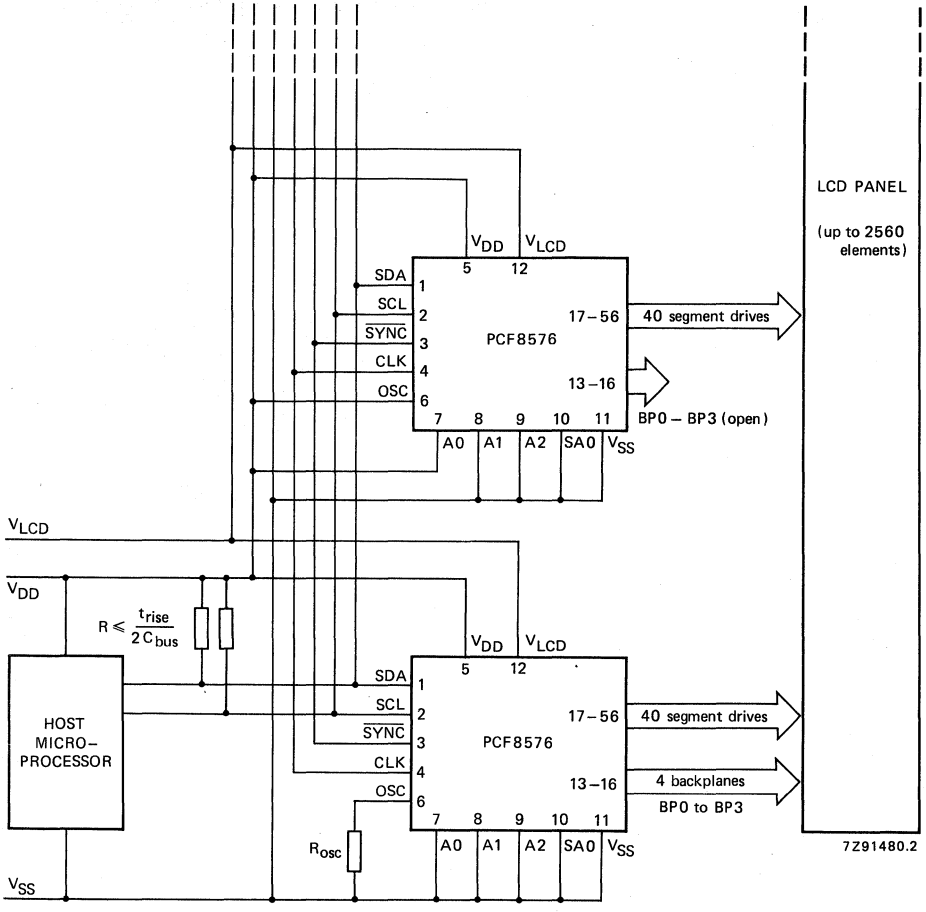


Fig. 18 Cascaded PCF8576 configuration.

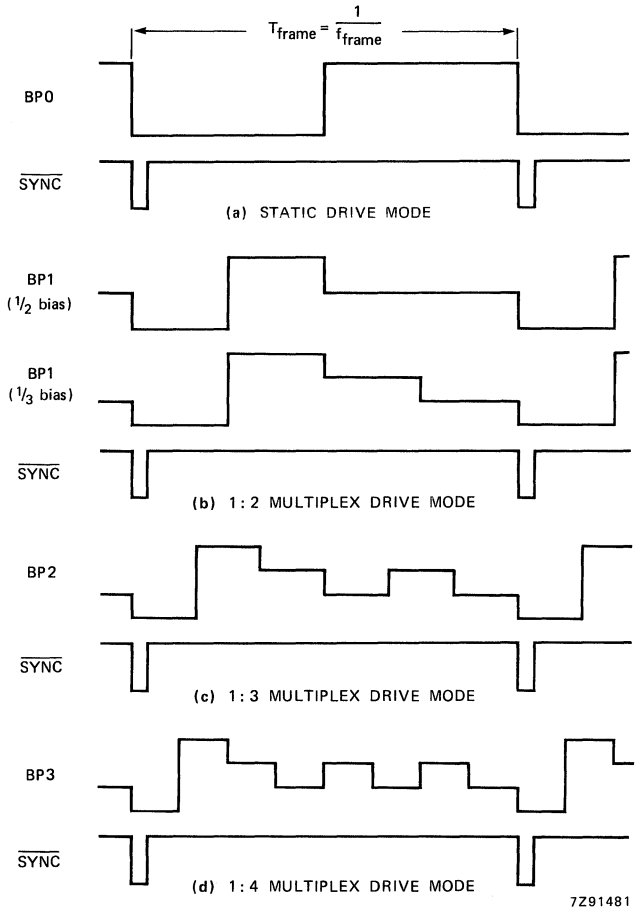


Fig. 19 Synchronization of the cascade for the various PCF8576 drive modes.

For single plane wiring of packaged PCF8576s and chip-on-glass cascading, see application information.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range	V_{DD}		−0,5 to + 11 V
LCD supply voltage range	V_{LCD}		V_{DD}−11 to V_{DD} V
Input voltage range (SCL; SDA; A0 to A2; OSC; CLK; $\overline{SYNC}$; SA0)	V_I		V_{SS} −0,5 to V_{DD} + 0,5 V
Output voltage range (S0 to S39; BP0 to BP3)	V_O		V_{LCD}−0,5 to V_{DD} + 0,5 V
D.C. input current	$\pm I_I$	max.	20 mA
D.C. output current	$\pm I_O$	max.	25 mA
V_{DD}, V_{SS} or V_{LCD} current	$\pm I_{DD}$, $\pm I_{SS}$, $\pm I_{LCD}$	max.	50 mA
Power dissipation per package	P_{tot}	max.	400 mW
Power dissipation per output	P_O	max.	100 mW
Storage temperature range	T_{stg}		−65 to + 150 °C

D.C. CHARACTERISTICS

V_{SS} = 0 V; V_{DD} = 2 to 9 V; V_{LCD} = V_{DD}−2 to V_{DD}−9 V;
T_{amb} = −40 to + 85 °C; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Operating supply voltage	V_{DD}	2	–	9	V
LCD supply voltage (note 1)	V_{LCD}	V_{DD}−9	–	V_{DD}−2	V
Operating supply current (normal mode) at f_{CLK} = 200 kHz (note 2)	I_{DD}	–	–	180	μA
Power-saving mode supply current at V_{DD} = 3,5 V; V_{LCD} = 0 V; f_{CLK} = 35 kHz (note 2)	I_{LP}	–	–	60	μA
LCD supply current (normal mode) at f_{CLK} = 200 kHz (note 2)	I_{LCD}	–	–	120	μA
Logic					
Input voltage LOW	V_{IL}	V_{SS}	–	0,3 V_{DD}	V
Input voltage HIGH	V_{IH}	0,7 V_{DD}	–	V_{DD}	V
Output voltage LOW at I_O = 0 mA	V_{OL}	–	–	0,05	V
Output voltage HIGH at I_O = 0 mA	V_{OH}	V_{DD}−0,05	–	–	V
Output current LOW (CLK, $\overline{SYNC}$) at V_{OL} = 1,0 V; V_{DD} = 5 V	I_{OL1}	1	–	–	mA
Output current HIGH (CLK) at V_{OH} = 4,0 V; V_{DD} = 5 V	I_{OH}	–	–	−1	mA
Output current LOW (SDA; SCL) at V_{OL} = 0,4 V; V_{DD} = 5 V	I_{OL2}	3	–	–	mA
Leakage current (SA0; A0 to A2; CLK; SCL; SDA) at V_I = V_{SS} or V_{DD}	$\pm I_{L1}$	–	–	1	μA

parameter	symbol	min.	typ.	max.	unit
Leakage current (OSC) at $V_I = V_{DD}$	$\pm I_{L2}$	–	–	1	μA
Pull-up resistor ($\overline{SYNC}$)	R_{SYNC}	20	50	150	kΩ
Power-on reset level (note 3)	V_{REF}	–	1,0	1,6	V
Tolerable spike width on bus	t_{sw}	–	–	100	ns
Input capacitance (note 4)	C_I	–	–	7	pF
LCD outputs					
D.C. voltage component (BP0 to BP3) at C_{BP} = 35 nF	$\pm V_{BP}$	–	20	–	mV
D.C. voltage component (S0 to S39) at C_S = 5 nF	$\pm V_S$	–	20	–	mV
Output impedance (BP0 to BP3) at $V_{LCD} = V_{DD}-5$ V (note 5)	R_{BP}	–	–	5	kΩ
Output impedance (S0 to S39) at $V_{LCD} = V_{DD}-5$ V (note 5)	R_S	–	–	7,0	kΩ

A.C. CHARACTERISTICS (note 6)

V_{SS} = 0 V; V_{DD} = 2 to 9 V; $V_{LCD} = V_{DD}-2$ to $V_{DD}-9$ V;

$T_{amb} = -40$ to + 85 °C; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Oscillator frequency (normal mode) at V_{DD} = 5 V; R_{osc} = 180 kΩ (note 7)	f_{CLK}	125	185	288	kHz
Oscillator frequency (power-saving mode) at V_{DD} = 3,5 V; R_{osc} = 1,2 MΩ	f_{CLKLP}	21	31	48	kHz
CLK HIGH time	t_{CLKH}	1	–	–	μs
CLK LOW time	t_{CLKL}	1	–	–	μs
$\overline{SYNC}$ propagation delay	t_{PSYNC}	–	–	400	ns
$\overline{SYNC}$ LOW time	t_{SYNCL}	1	–	–	μs
Driver delays with test loads at $V_{LCD} = V_{DD}-5$ V	t_{PLCD}	–	–	30	μs

A.C. CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
I²C bus high-speed mode					
Bus free time	t_{BUF}	4,7	–	–	μs
Start condition hold time	$t_{HD;STA}$	4	–	–	μs
SCL LOW time	t_{LOW}	4,7	–	–	μs
SCL HIGH time	t_{HIGH}	4	–	–	μs
Start condition set-up time (repeated start code only)	$t_{SU;STA}$	4,7	–	–	μs
Data hold time	$t_{HD;DAT}$	0	–	–	μs
Data set-up time	$t_{SU;DAT}$	250	–	–	ns
Rise time	t_R	–	–	1	μs
Fall time	t_F	–	–	300	ns
Stop condition set-up time	$t_{SU;STO}$	4,7	–	–	μs
I²C bus low-speed mode					
Bus free time	t_{BUF}	105	–	–	μs
Start condition hold time	$t_{HD;STA}$	365	–	–	μs
SCL LOW time	t_{LOW}	105	–	155	μs
SCL HIGH time	t_{HIGH}	365	–	415	μs
Start condition set-up time (repeated start code only)	$t_{SU;STA}$	105	–	155	μs
Data hold time	$t_{HD;DAT}$	0	–	–	μs
Data set-up time	$t_{SU;DAT}$	250	–	–	ns
Rise time	t_R	–	–	1	μs
Fall time	t_F	–	–	300	ns
Stop condition set-up time	$t_{SU;STO}$	105	–	155	μs

Notes to characteristics

1. $V_{LCD} < V_{DD}-3$ V for 1/3 bias.
2. Outputs open; inputs at V_{SS} or V_{DD}; external clock with 50% duty cycle; I²C bus inactive.
3. Resets all logic when $V_{DD} < V_{REF}$.
4. Periodically sampled, not 100% tested.
5. Outputs measured one at a time.
6. All timing values referred to V_{IH} and V_{IL} levels with an input voltage swing of V_{SS} to V_{DD}.
7. At $f_{CLK} < 125$ kHz, I²C bus maximum transmission speed is derated.

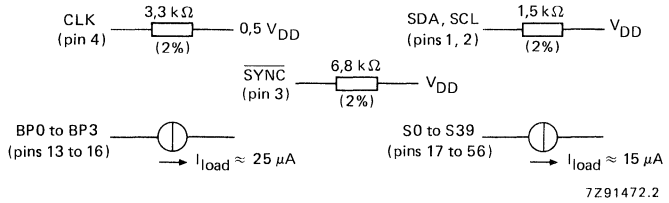


Fig. 20 Test loads.

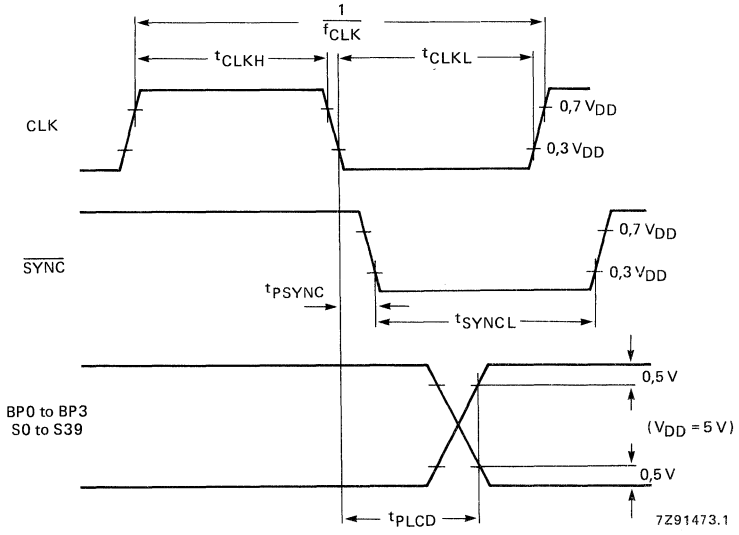


Fig. 21 Driver timing waveforms.

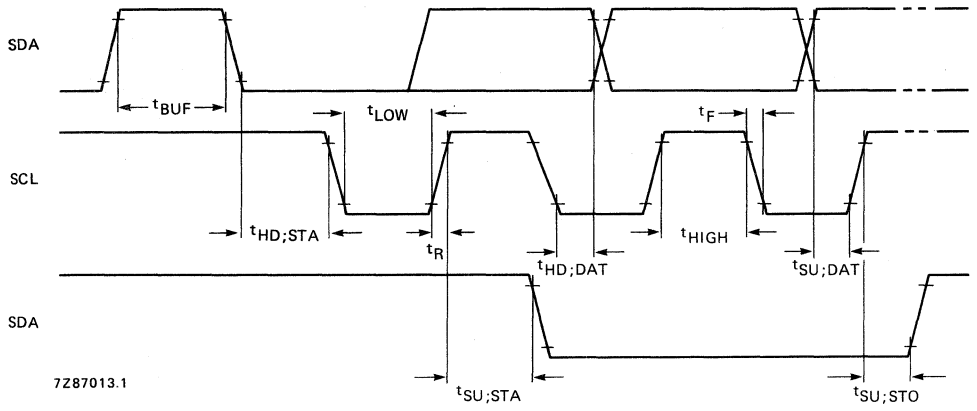


Fig. 22 I²C bus high-speed mode timing waveforms.

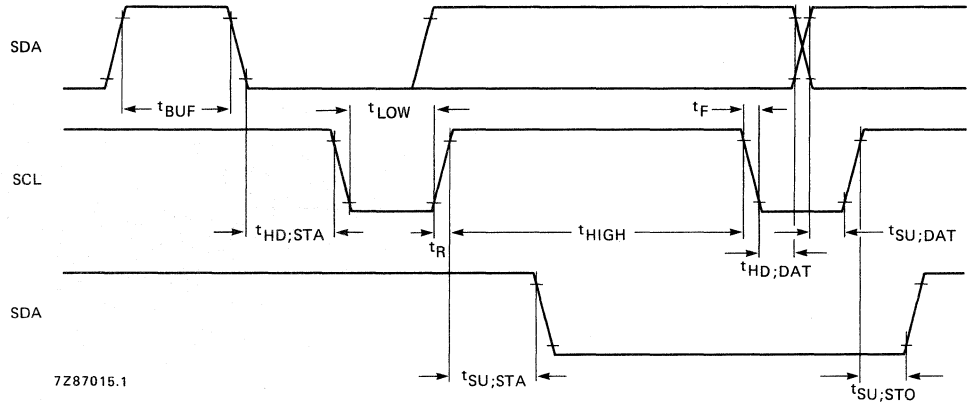
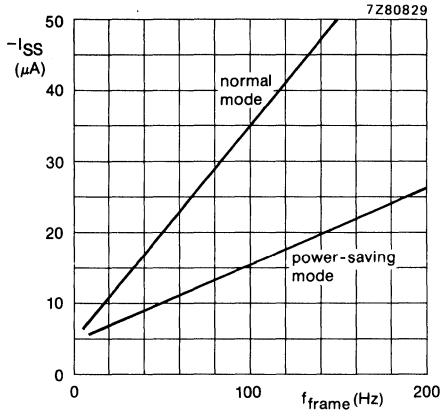
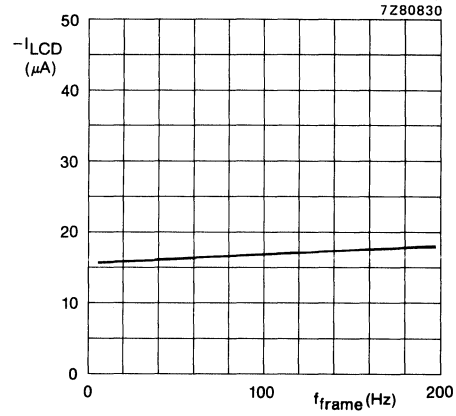


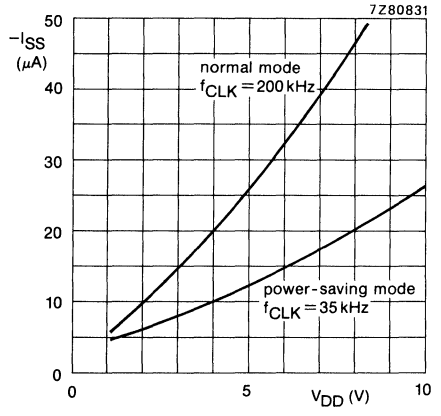
Fig. 23 I²C bus low-speed mode timing waveforms.



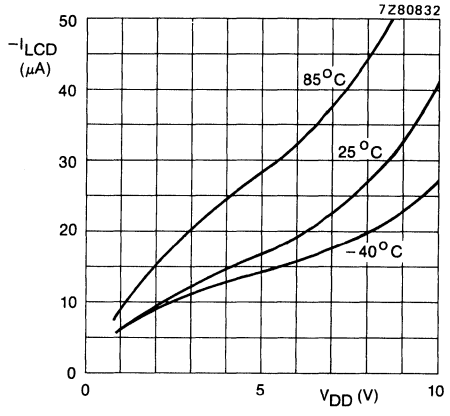
(a) V_{DD} = 5 V; V_{LCD} = 0 V; T_{amb} = 25 °C.



(b) V_{DD} = 5 V; V_{LCD} = 0 V; T_{amb} = 25 °C.

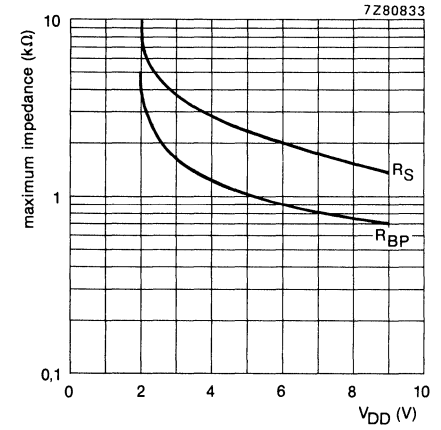


(c) V_{LCD} = 0 V; external clock; T_{amb} = −40 to + 85 °C.

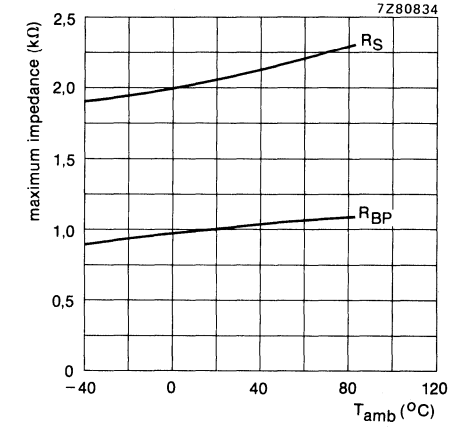


(d) V_{LCD} = 0 V; external clock; f_{CLK} = nominal frequency.

Fig. 24 Typical supply current characteristics.



(a) V_{LCD} = 0 V; T_{amb} = 25 °C.



(b) V_{DD} = 5 V; V_{LCD} = 0 V.

Fig. 25 Typical characteristics of LCD outputs.

APPLICATION INFORMATION

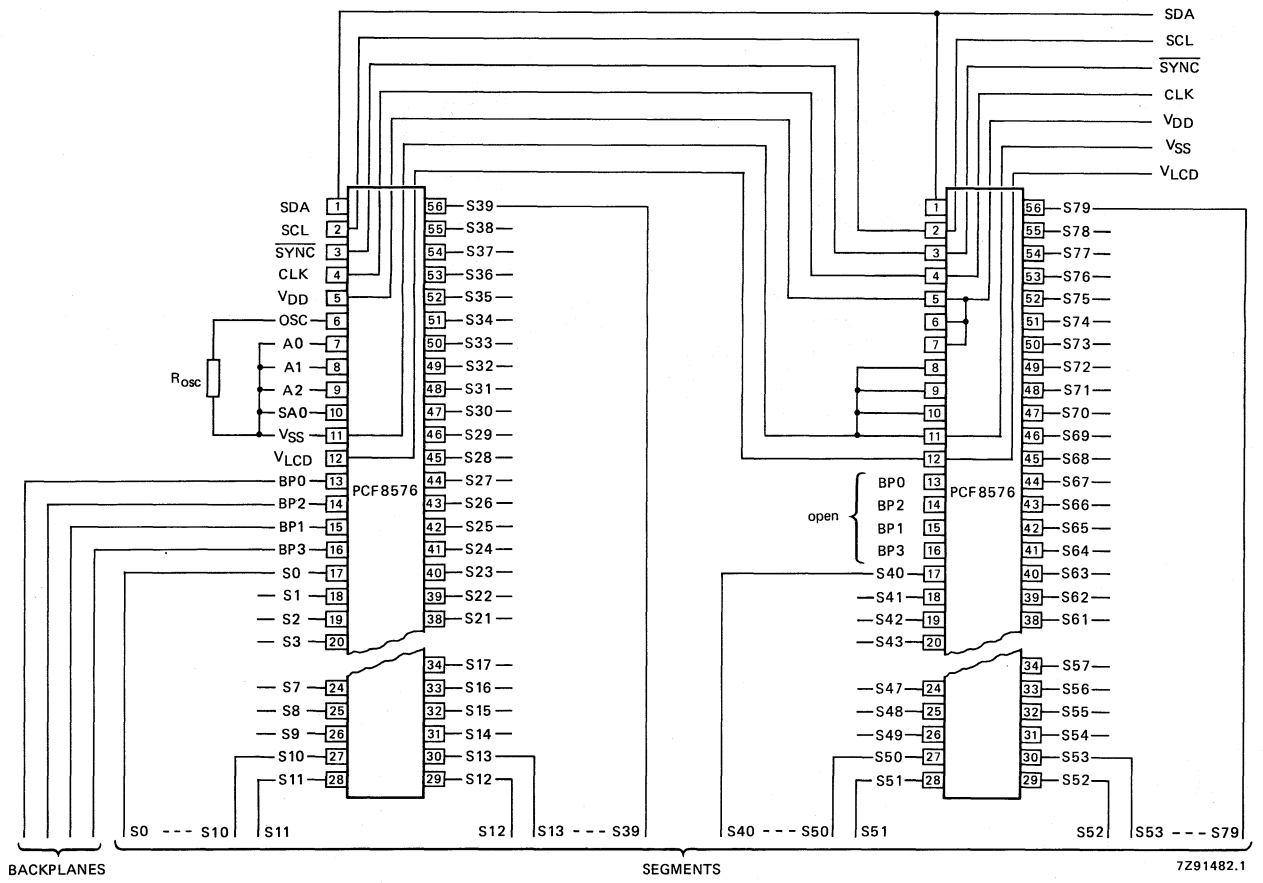


Fig. 26 Single plane wiring of packaged PCF8576s.

Chip-on-glass cascadability in single plane

In chip-on-glass technology, where driver devices are bonded directly onto the glass of the LCD, it is important that the devices may be cascaded without the crossing of conductors, but the paths of conductors can be continued on the glass under the chip. All of this is facilitated by the PCF8576 bonding pad layout (Fig. 27). Pads needing bus interconnection between all PCF8576s of the cascade are V_{DD}, V_{SS}, CLK, SCL, SDA and $\overline{SYNC}$. These lines may be led to the corresponding pads of the next PCF8576 through the wide opening between the V_{LCD} pad and the backplane output pads. The only bussed line that does not require a second opening to lead through to the next PCF8576 is V_{LCD}, being the cascade centre. The placing of V_{LCD} adjacent to V_{SS} allows the two supplies to be tied together.

Fig. 28 shows the connection diagram for a cascaded PCF8576 application with single plane wiring. Note the use of the open space between the V_{LCD} pad and the backplane output pads to route V_{DD}, V_{SS}, CLK, SCL, SDA and $\overline{SYNC}$. The external connections may be made to either end of the cascade, wherever most convenient for the connector.

When an external clocking source is to be used, OSC of all devices should be tied to V_{DD}. The pads OSC, A0, A1, A2 and SA0 have been placed between V_{SS} and V_{DD} to facilitate wiring of oscillator, hardware subaddress and slave address.

APPLICATION INFORMATION (continued)

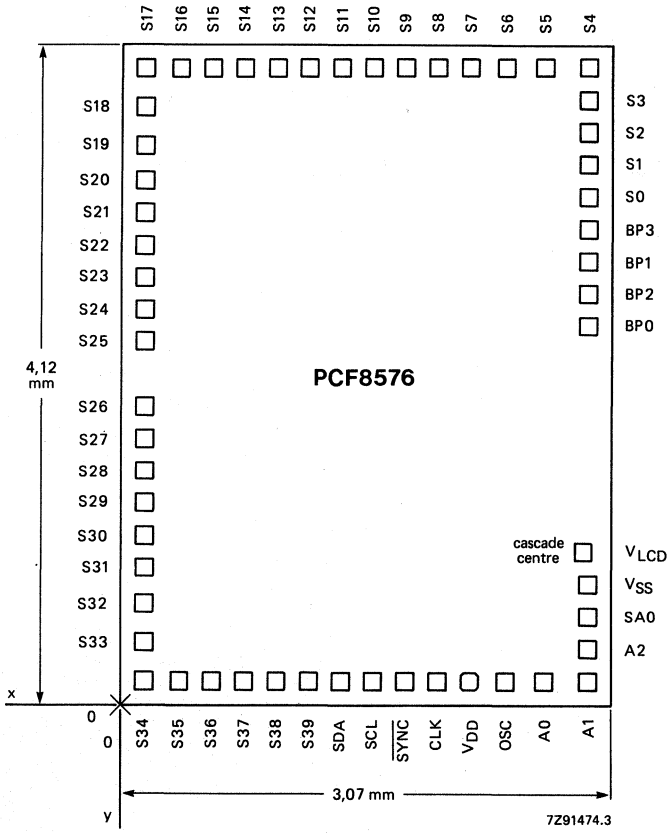


Fig. 27 PCF8576 bonding pad locations.

Bonding pad locations

All x/y coordinates are referenced to left-hand bottom corner (0/0, Fig. 27).

Dimensions in μm

pad	x	y	
S34	160	160	bottom
S35	380		
S36	580		
S37	780		
S38	980		
S39	1180		
SDA	1380		
SCL	1580		
SYNC	1780		
CLK	1980		
V_{DD}	2180		
OSC	2400		
A0	2640		
A1	2910	160	bottom
S17	160	3960	top
S16	380		
S15	580		
S14	780		
S13	980		
S12	1180		
S11	1380		
S10	1580		
S9	1780		
S8	1980		
S7	2180		
S6	2400		
S5	2640		
S4	2910	3960	top

pad	x	y	
S33	160	400	left
S32		640	
S31		860	
S30		1060	
S29		1260	
S28		1460	
S27		1660	
S26		1860	
S25		2260	
S24		2460	
S23		2660	
S22		2860	
S21		3060	
S20		3260	
S19		3480	
S18	160	3720	left
A2	2910	360	right
SA0		560	
V_{SS}		760	
V_{LCD}		960	
BP0		2360	
BP2		2560	
BP1		2760	
BP3		2960	
S0		3160	
S1		3360	
S2		3560	
S3	2910	3760	right

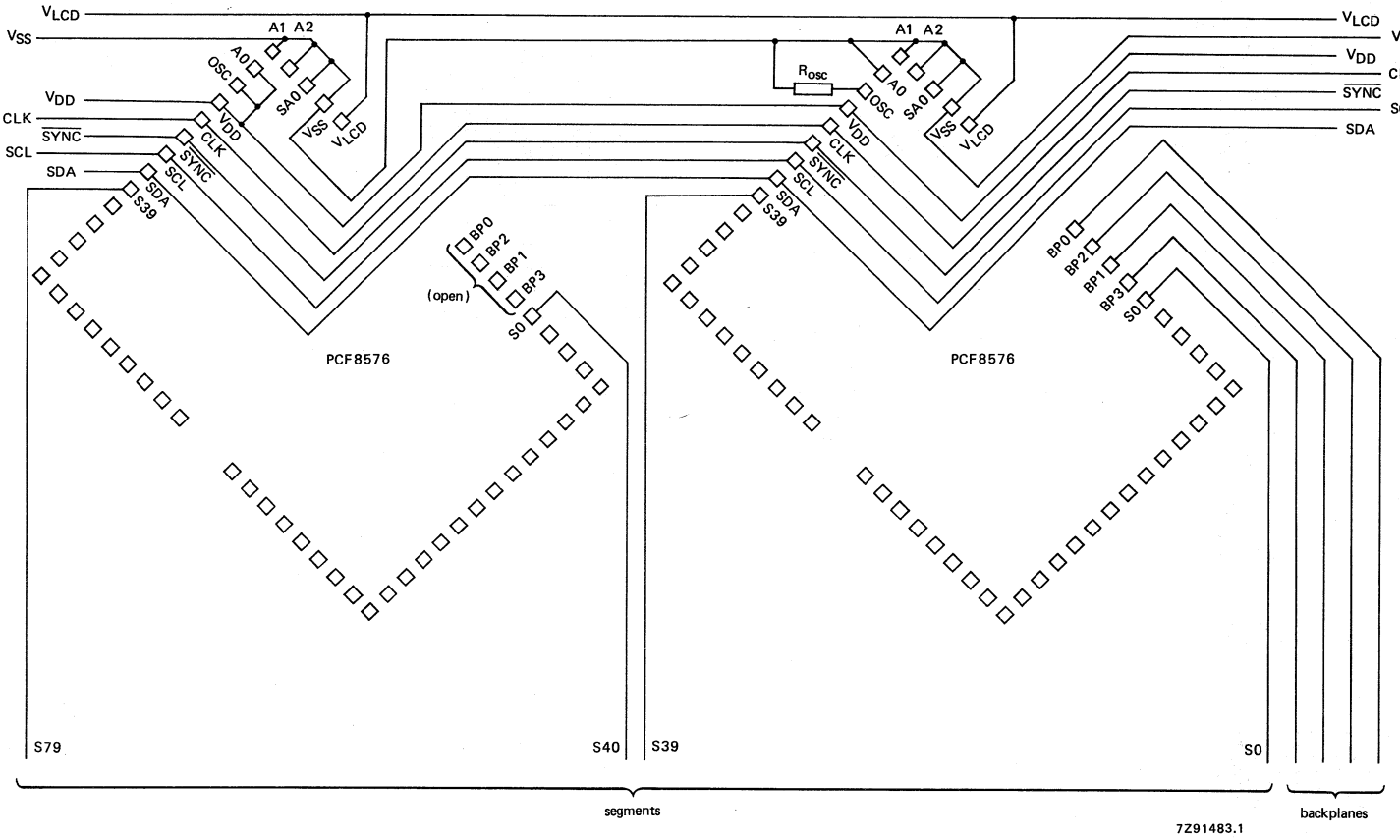
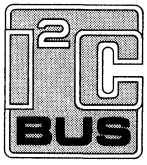


Fig. 28 Chip-on-glass application; cascaded PCF8576s with single-plane wiring (viewed from back of chip).



Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

LCD DIRECT/DUPLEX DRIVER WITH I²C BUS INTERFACE

GENERAL DESCRIPTION

The PCF8577 is a single chip, silicon gate CMOS circuit. It is designed to drive liquid crystal displays with up to 32 segments directly, or 64 segments in a duplex manner.

The two-line I²C bus interface substantially reduces wiring overheads in remote display applications. Bus traffic is minimized in multiple IC applications by automatic address incrementing, hardware sub-addressing and display memory switching (direct drive mode).

The PCF8577 and PCF8577A differ only in their slave address.

Features

- Direct/duplex drive modes with up to 32/64 LCD-segment drive capability per device
- Operating supply voltage: 2,5 to 9 V
- Low power consumption
- I²C bus interface
- Optimized pinning for single plane wiring
- Single-pin built-in oscillator
- Auto-incremented loading across device sub-address boundaries
- Display memory switching in direct drive mode
- May be used for I²C bus output expander
- System expansion up to 256 segments (512 segments with PCF8577A)
- Power-on-reset sets all segments off (to blank)

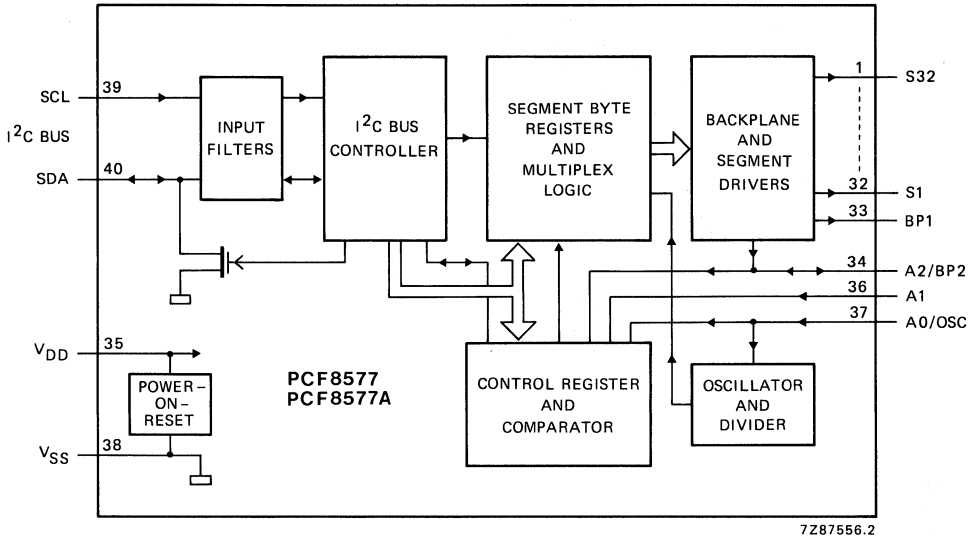


Fig. 1 Block diagram.

PACKAGE OUTLINES

PCF8577P, PCF8577AP: 40-lead DIL; plastic (SOT-129).
PCF8577T, PCF8577AT: 40-lead mini-pack; plastic (VSO-40; SOT-158A).

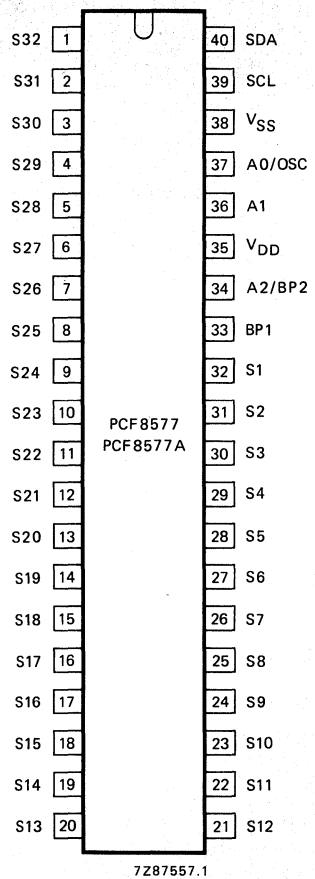


Fig. 2 Pinning diagram.

PINNING

Supply

35	V_{DD}	positive supply
38	V_{SS}	negative supply

I^2C bus

40	SDA	I^2C bus data line
39	SCL	I^2C bus clock line

Inputs

36	A1	hardware address line
37	A0/OSC	hardware address line/oscillator pin

Outputs

1 – 32	S1 – S32	segment outputs

Input – Output

34	A2/BP2	harware address line/cascade sync input/backplane output
33	BP1	cascade sync input/backplane output

FUNCTIONAL DESCRIPTION

Hardware sub-address A0, A1, A2

The hardware sub-address lines A0, A1, A2 are used to program the device sub-address for each PCF8577 on the bus. Lines A0 and A2 are shared with OSC and BP2 respectively to reduce pin-out requirements.

A0/OSC Line A0 is defined as LOW (logic 0) when this pin is used for the local oscillator or when connected to V_{SS}. Line A0 is defined as HIGH (logic 1) when connected to V_{DD}.

A1 Line A1 must be defined as LOW (logic 0) or as HIGH (logic 1) by connection to V_{SS} or V_{DD} respectively.

A2/BP2 In the direct drive mode the second backplane signal BP2 is not used and the A2/BP2 pin is exclusively the A2 input. Line A2 is defined as LOW (logic 0) when connected to V_{SS} or, if this is not possible, by leaving it unconnected (internal pull-down). Line A2 is defined as HIGH (logic 1) when connected to V_{DD}.

In the duplex drive mode the second backplane signal BP2 is required and the A2 signal is undefined. In this mode device selection is made exclusively from lines A0 and A1.

Oscillator A0/OSC

The PCF8577 has a single-pin built-in oscillator which provides the modulation for the LCD segment driver outputs. One external resistor and one external capacitor are connected to the A0/OSC pin to form the oscillator. In an expanded system containing more than one PCF8577 the backplane signals are usually common to all devices and only one oscillator is needed. The devices which are not used for the oscillator are put into the expansion mode by connecting the A0/OSC pin to either V_{DD} or V_{SS} depending on the required state for A0. In the expansion mode each PCF8577 is synchronized from the backplane signal(s).

User-accessible registers

There are nine user-accesible 1-byte registers. The first is a control register which is used to control the loading of data into the segment byte registers and to select display options. The other eight are segment byte registers, split into two banks of storage, which store the segment data. The set of even numbered segment byte registers is called BANK A. Odd numbered segment byte registers are called BANK B.

There are two slave addresses, one for PCF8577, and one for PCF8577A (see Fig. 14). All addressed devices load the second byte into the control register and each device maintains an identical copy of the control byte in the control register at all times (see I²C bus protocol Fig. 15).

The control register is shown in more detail in Fig. 3. The least-significant bits select which device and which segment byte register are loaded next. This part of the register is therefore called the Segment Byte Vector (SBV).

The upper three bits of the SBV (V5 to V3) are compared with the hardware sub-address input signals A2, A1 and A0. If they are the same then the device is enabled for loading, if not the device ignores incoming data but remains active.

The three least-significant bits of the SBV (V2 to V0) address one of the segment byte registers within the enabled chip for loading segment data.

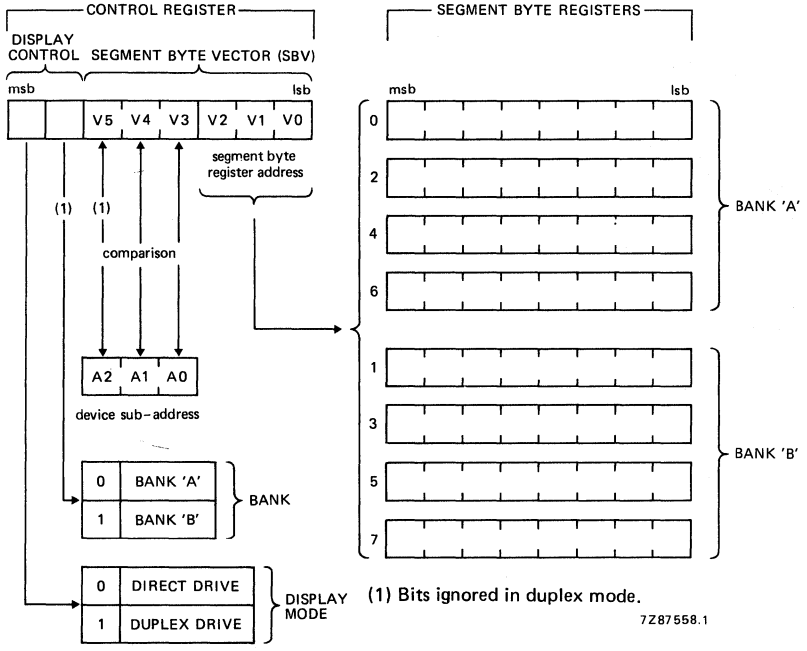


Fig. 3 PCF8577 register organization.

FUNCTIONAL DESCRIPTION (continued)

The control register also has two display control bits. These bits are named MODE and BANK. The MODE bit selects whether the display outputs are configured for direct or duplex drive displays. The BANK bit allows the user to display BANK A or BANK B.

Auto-incremented loading

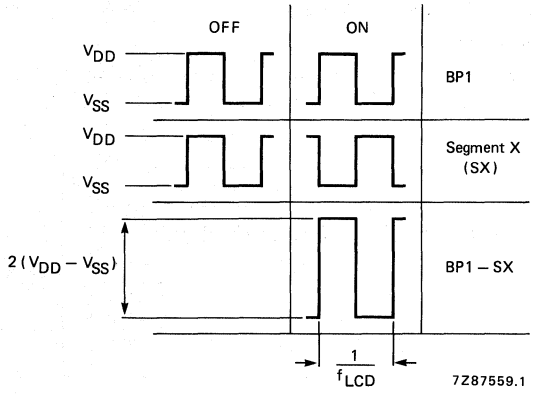
After each segment byte is loaded the SBV is incremented automatically, thus auto-incremented loading occurs if more than one segment byte is received in a data transfer.

Since the SBV addresses both device and segment registers, auto-incremented loading may proceed across device boundaries provided that the hardware sub-addresses are arranged contiguously.

Direct drive mode

The PCF8577 is set to the direct drive mode by loading the MODE control bit with logic 0. In this mode only four bytes are needed to store the data for the 32 segment drivers. Setting the BANK bit to logic 0 selects even bytes (BANK A); setting the BANK bit to logic 1 selects odd bytes (BANK B).

In the direct drive mode the SBV is auto-incremented by two after the loading of each segment byte register. This means that auto-incremented loading of BANK A or BANK B is possible. Either bank may be completely or partially loaded irrespective of which bank is being displayed. Direct drive output waveforms are shown in Fig. 4.



$V_{ON} = V_{DD} - V_{SS}$

$V_{OFF} = 0$

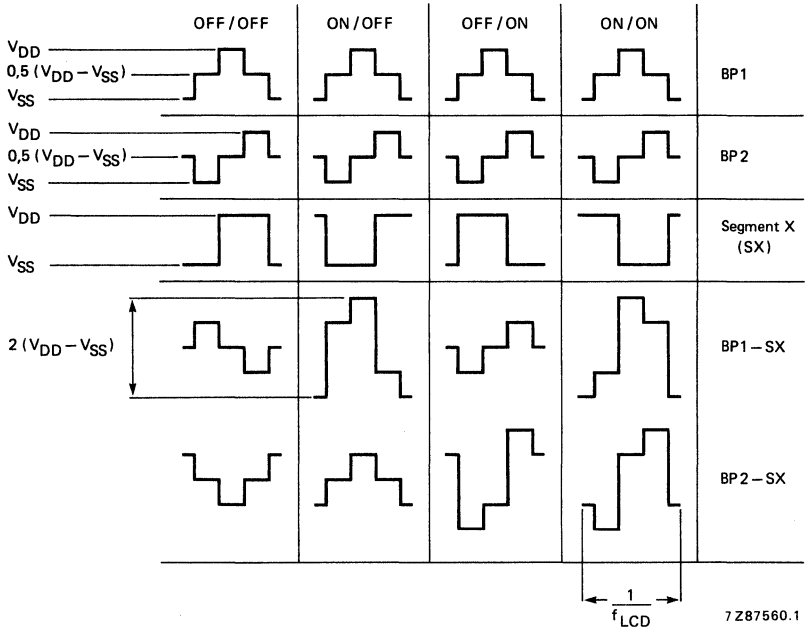
Fig. 4 Direct drive mode display output waveforms.

Duplex mode

The PCF8577 is set to the duplex mode by loading the MODE bit with logic 1. In this mode a second backplane signal (BP2) is needed and pin A2/BP2 is used for this; therefore A2 and its equivalent SBV bit V5 are undefined. The SBV auto-increments by one between loaded bytes.

All of the segment bytes are needed to store data for the 32 segment drivers and the BANK bit is ignored.

Duplex mode output waveforms are shown in Fig. 5.



$V_{ON} = 0,79\ (V_{DD} - V_{SS})$

$V_{OFF} = 0,35\ (V_{DD} - V_{SS})$

$\frac{V_{ON}}{V_{OFF}} = 2,26$

Fig. 5 Duplex mode display output waveforms.

DEVELOPMENT DATA

CHARACTERISTICS OF THE I²C BUS

The I²C bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals.

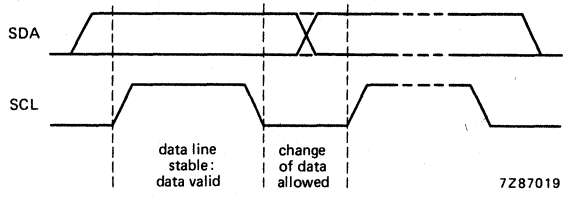


Fig. 6 Bit transfer.

Start and stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the stop condition (P).

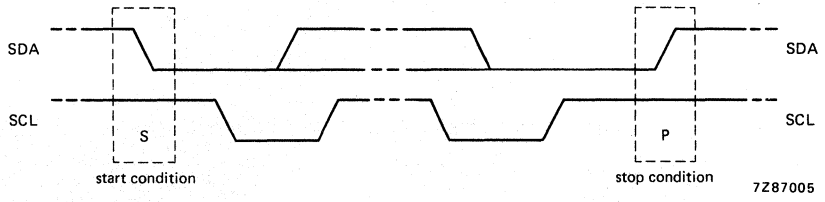


Fig. 7 Definition of start and stop conditions.

System configuration

A device generating a message is a "transmitter", a device receiving a message is the "receiver". The device that controls the message is the "master" and the devices which are controlled by the master are the "slaves".

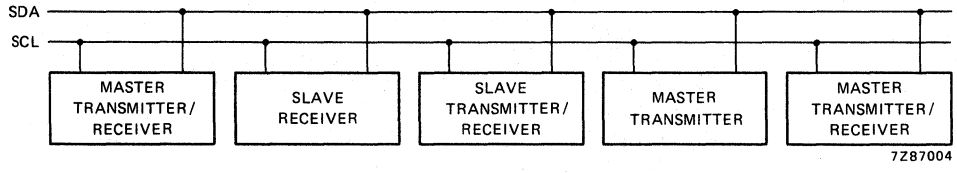


Fig. 8 System configuration.

Acknowledge

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is not limited. Each byte is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse, set up and hold times must be taken into account. A master receiver must signal an end of data to the transmitter by *not* generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

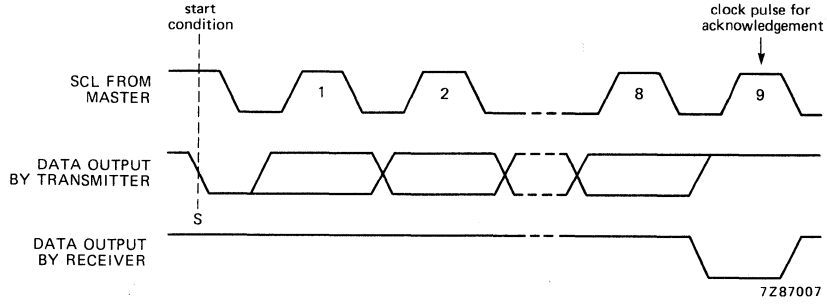


Fig. 9 Acknowledgement on the I²C bus.

Timing specifications

Within the I²C bus specifications a high-speed mode and a low-speed mode are defined. The PCF8577 operates in both modes and the timing requirements are as follows:

High-speed mode

Masters generate a bus clock with a maximum frequency of 100 kHz. Detailed timing is shown in Fig. 10.

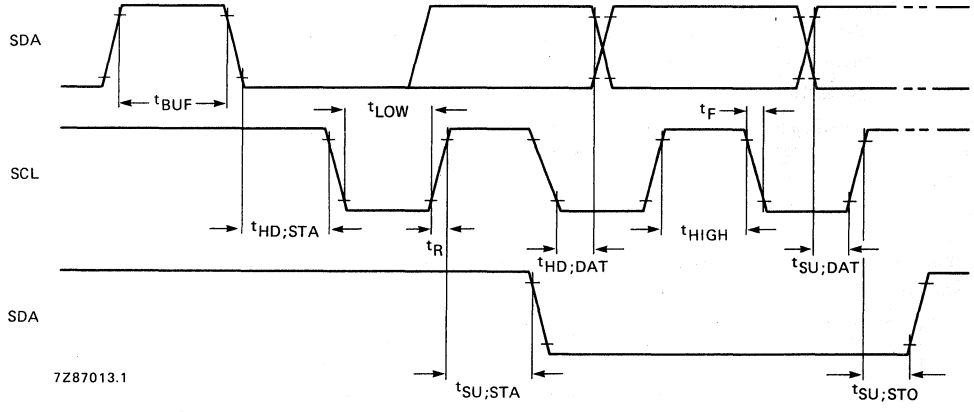


Fig. 10 Timing of the high-speed mode.

CHARACTERISTICS OF THE I²C BUS (continued)

Where:

t_{BUF}	$t \geqslant t_{LOWmin}$	The minimum time the bus must be free before a new transmission can start
$t_{HD;STA}$	$t \geqslant t_{HIGHmin}$	Start condition hold time
t_{LOWmin}	4,7 μs	Clock LOW period
$t_{HIGHmin}$	4 μs	Clock HIGH period
$t_{SU;STA}$	$t \geqslant t_{LOWmin}$	Start condition set-up time, only valid for repeated start code
$t_{HD;DAT}$	$t \geqslant 0$ μs	Data hold time
$t_{SU;DAT}$	$t \geqslant 250$ ns	Data set-up time
t_R	$t \leqslant 1$ μs	Rise time of both the SDA and SCL line
t_F	$t \leqslant 300$ ns	Fall time of both the SDA and SCL line
$t_{SU;STO}$	$t \geqslant t_{LOWmin}$	Stop condition set-up time

Note

All the timing values referred to V_{IH} and V_{IL} levels with a voltage swing of V_{SS} to V_{DD}.

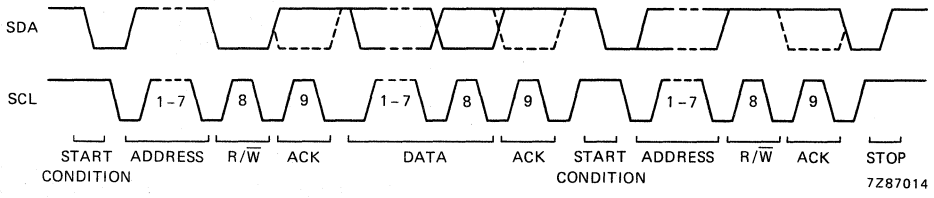


Fig. 11 Complete data transfer in the high-speed mode.

Where:

Clock t_{LOWmin}	4,7 μs
$t_{HIGHmin}$	4 μs
The dashed line is the acknowledgement of the receiver	
Mark-to-space ratio	1 : 1 (LOW-to-HIGH)
Max. number of bytes	unrestricted
Premature termination of transfer	allowed by generation of STOP condition
Acknowledge clock bit	must be provided by the master

Low-speed mode

Masters generate a bus clock with a maximum frequency of 2 kHz; a minimum LOW period of 105 μs and a minimum HIGH period of 365 μs. The mark-to-space ratio is 1 : 3 LOW-to-HIGH. Detailed timing is shown in Fig. 12.

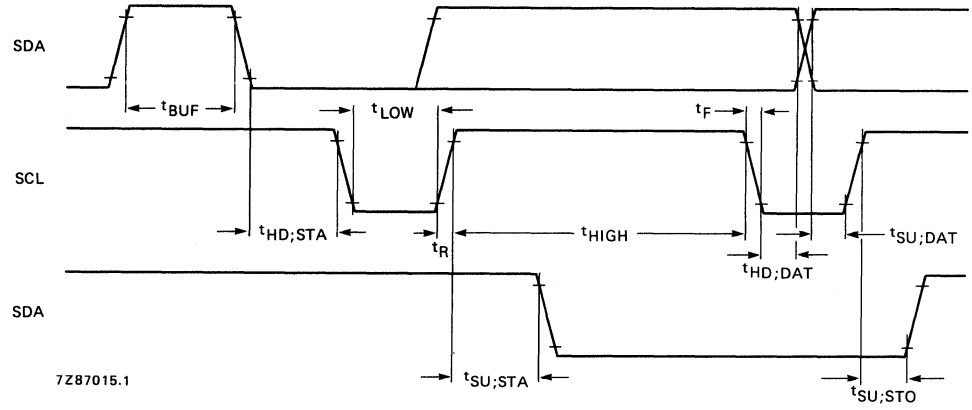


Fig. 12 Timing of the low-speed mode.

Where:

t_{BUF}	$t \geqslant 105\ \mu s$ (t_{LOWmin})
$t_{HD;STA}$	$t \geqslant 365\ \mu s$ ($t_{HIGHmin}$)
t_{LOW}	130 μs ± 25 μs
t_{HIGH}	390 μs ± 25 μs
$t_{SU;STA}$	130 μs ± 25 μs*
$t_{HD;DAT}$	$t \geqslant 0\ \mu s$
$t_{SU;DAT}$	$t \geqslant 250$ ns
t_R	$t \leqslant 1\ \mu s$
t_F	$t \leqslant 300$ ns
$t_{SU;STO}$	130 μs ± 25 μs

Note

All the timing values referred to V_{IH} and V_{IL} levels with a voltage swing of V_{SS} to V_{DD}, for definitions see high-speed mode.

* Only valid for repeated start code.

CHARACTERISTICS OF THE I²C BUS (continued)

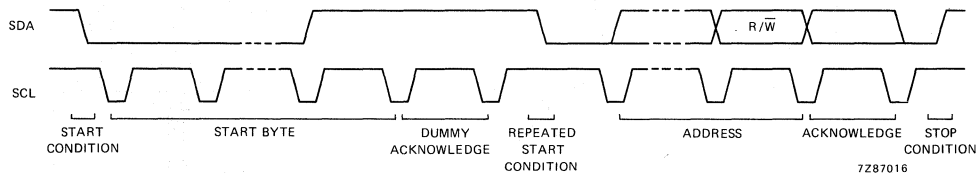


Fig. 13 Complete data transfer in the low-speed mode.

Where:

Clock t_{LOWmin}	130 μs ± 25 μs
$t_{HIGHmin}$	390 μs ± 25 μs
Mark-to-space ratio	1 : 3 (LOW-to-HIGH)
Start byte	0000 0001
Maximum number of bytes	6
Premature termination of transfer	not allowed
Acknowledge clock bit	must be provided by master

Note

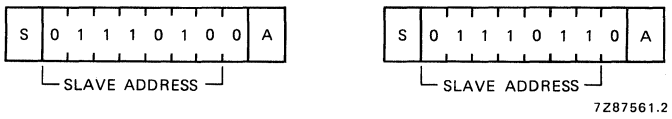
The general characteristics and detailed specification of the I²C bus are described in a separate data sheet (serial data buses) in handbook: ICs for digital systems in radio, audio and video equipment.

ADDRESSING

Before any data is transmitted on the I²C bus, the device which should respond is addressed first. The addressing is always done with the first byte transmitted after the start procedure.

Slave address

The slave address for PCF8577 and PCF8577A are shown in Fig. 14.



(a) PCF8577. (b) PCF8577A.

Fig. 14 PCF8577 and PCF8577A slave addresses.

I²C bus protocol

The PCF8577 I²C bus protocol is shown in Fig. 15.

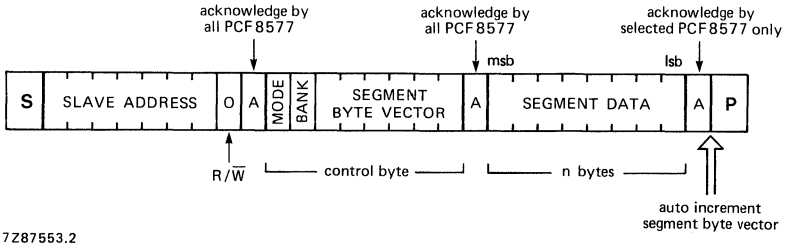


Fig. 15 I²C bus protocol.

The PCF8577 is a slave receiver and has a fixed slave address (Fig. 14). All PCF8577 on the same bus acknowledge the slave address in parallel. The second byte is always the control byte and is loaded into the control register of each PCF8577 on the bus. Subsequent data bytes are loaded into the segment registers of the selected device. Any number of data bytes may be loaded in one transfer and in an expanded system rollover of the SBV from 111 111 to 000 000 is allowed. If a stop (P) condition is given after the control byte acknowledge the segment data remains unchanged. This allows the BANK bit to be toggled without changing the segment register contents. During loading of segment data only the selected PCF8577 gives an acknowledge. Loading is terminated by generating a stop (P) condition.

DEVELOPMENT DATA

DISPLAY MEMORY MAPPING

The mapping between the eight segment registers and the segment outputs S1 to S32 is shown in Tables 1 and 2.

Since only one register bit per segment is needed in the direct drive mode, the BANK bit allows swapping of display information. If BANK is set to logic 0 even bytes (BANK A) are displayed; if BANK is set to logic 1 odd bytes (BANK B) are displayed. BP1 is always used for the backplane output in the direct drive mode.

Table 1 Segment byte — segment driver mapping in the direct drive mode.

MODE	BANK	V2	V1	V0	SEGMENT REGISTER / BIT	MSB 7	6	5	4	3	2	1	LSB 0	BACKPLANE
0	0	0	0	0	0	S8	S7	S6	S5	S4	S3	S2	S1	BP1
0	1	0	0	1	1	S8	S7	S6	S5	S4	S3	S2	S1	BP1
0	0	0	1	0	2	S16	S15	S14	S13	S12	S11	S10	S9	BP1
0	1	0	1	1	3	S16	S15	S14	S13	S12	S11	S10	S9	BP1
0	0	1	0	0	4	S24	S23	S22	S21	S20	S19	S18	S17	BP1
0	1	1	0	1	5	S24	S23	S22	S21	S20	S19	S18	S17	BP1
0	0	1	1	0	6	S32	S31	S30	S29	S28	S27	S26	S25	BP1
0	1	1	1	1	7	S32	S31	S30	S29	S28	S27	S26	S25	BP1

Mapping example: bit 0 of register 7 controls the LCD segment S25 if BANK bit is a logic 1.

DISPLAY MEMORY MAPPING (continued)

Even bytes (BANK A) correspond to backplane 1 (BP1) and odd bytes (BANK B) correspond to backplane 2 (BP2).

Table 2 Segment byte — segment driver mapping in the duplex mode.

MODE	BANK	V2	V1	V0	SEGMENT REGISTER / BIT	M S B 7	6	5	4	3	2	1	L S B 0	BACKPLANE
1	x	0	0	0	0	S8	S7	S6	S5	S4	S3	S2	S1	BP1
1	x	0	0	1	1	S8	S7	S6	S5	S4	S3	S2	S1	BP2
1	x	0	1	0	2	S16	S15	S14	S13	S12	S11	S10	S9	BP1
1	x	0	1	1	3	S16	S15	S14	S13	S12	S11	S10	S9	BP2
1	x	1	0	0	4	S24	S23	S22	S21	S20	S19	S18	S17	BP1
1	x	1	0	1	5	S24	S23	S22	S21	S20	S19	S18	S17	BP2
1	x	1	1	0	6	S32	S31	S30	S29	S28	S27	S26	S25	BP1
1	x	1	1	1	7	S32	S31	S30	S29	S28	S27	S26	S25	BP2

X = don't care.

Mapping example: bit 7 of register 5 controls the LCD segment S24/BP2.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range	V_{DD}	−0,5 to 11	V
Voltage on any pin	V_I	V_{SS} − 0,8 to V_{DD} + 0,8	V
D.C. input current	$\pm I_I$	max. 20	mA
D.C. output current	$\pm I_O$	max. 25	mA
V_{DD} or V_{SS} current	$\pm I_{DD}$, I_{SS}	max. 50	mA
Power dissipation per package	P_{tot}	max. 500*	mW
Power dissipation per output	P	max. 100	mW
Operating ambient temperature range	T_{amb}	−40 to +85	°C
Storage temperature range	T_{stg}	−65 to +150	°C

* Derate 7,7 mW/K when $T_{amb} > 60$ °C.

DEVELOPMENT DATA

CHARACTERISTICS

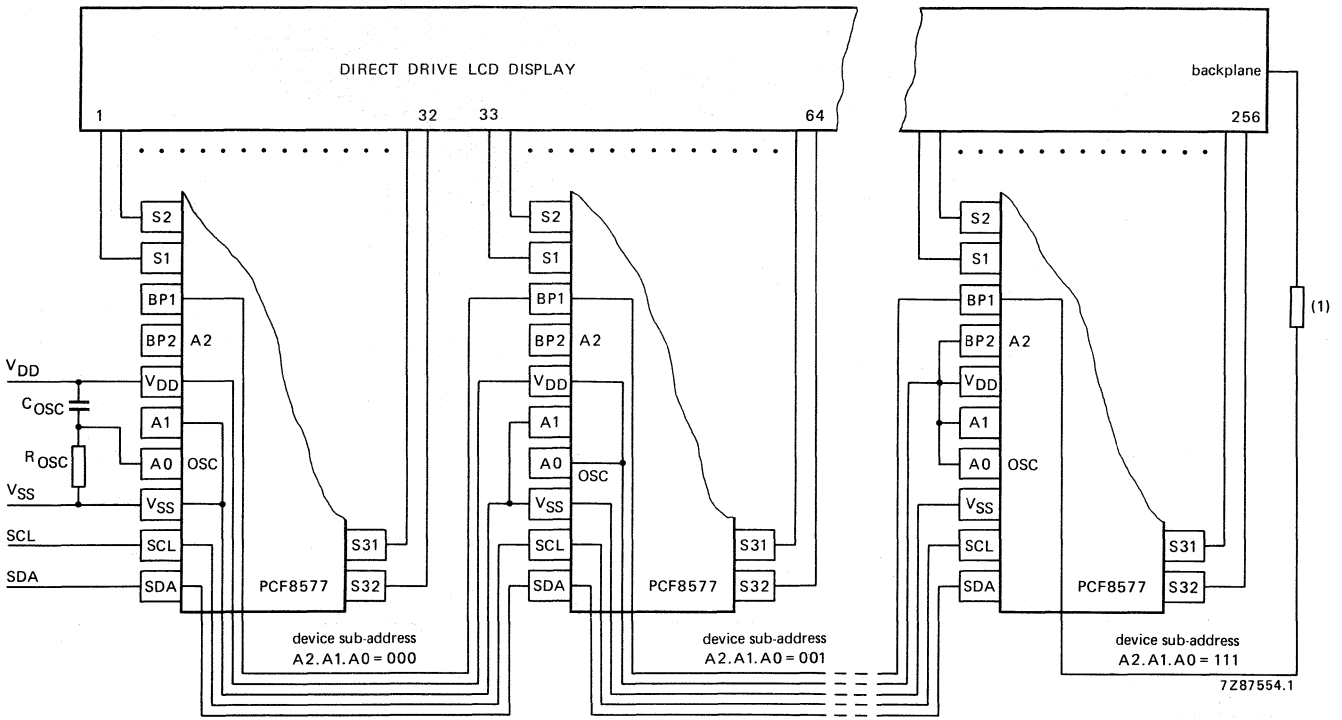
V_{DD} = 2,5 to 9 V; V_{SS} = 0 V; T_{amb} = −40 to + 85 °C unless otherwise specified

parameter	symbol	min.	typ.*	max.	unit
Supply voltage	V_{DD}	2,5	–	9,0	V
Supply current					
f_{SCL} = 100 kHz; no load; R_{OSC} = 1 MΩ	I_{DD}	–	80	250	μA
f_{SCL} = 0; no load; R_{OSC} = 1 MΩ; V_{DD} = 5 V; T_{amb} = 25 °C	I_{DD}	–	35	70	μA
Power-on-reset level**	V_{REF}	–	1,1	2,0	V
Input SCL; input/output SDA					
input voltage LOW	V_{IL}	0	–	0,8	V
input voltage HIGH	V_{IH}	2,0	–	9,0	V
output current LOW at V_{OL} = 0,4 V	I_{OL}	3,0	–	–	mA
output leakage current HIGH at V_{OH} = V_{DD}	I_{OH}	–	–	250	nA
tolerable spike width on bus	t_{sw}	–	–	100	ns
input capacitance at V_I = V_{SS}	C_I	–	–	7	pF
A1 input leakage current at V_I = V_{SS} or V_{DD}	I_I	–	–	250	nA
A2/BP2 input current at V_I = V_{DD}	I_I	–	2,0	–	μA
A0/OSC input current at V_I = V_{SS} or V_{DD}	$\pm I_I$	–	5,0	–	μA
DC component of LCD driver	$\pm V_{BP}$	–	20	–	mV
Segment loads	C_{SX}	–	–	5	nF
	R_{SX}	1	–	–	MΩ
Segment output current at V_{OL} = 0,4 V; V_{DD} = 5 V	I_{OL}	0,3	–	–	mA
Segment output current at V_{OH} = V_{DD} − 0,4 V; V_{DD} = 5 V	$-I_{OH}$	0,3	–	–	mA
Backplane load (direct drive)	C_{BP}	–	–	50	nF
	R_{BP}	100	–	–	kΩ
Backplane loads (duplex drive)	C_{BP}	–	–	35	nF
	R_{BP}	100	–	–	kΩ
Rise and fall times (V_{BP} − V_{SX}) at maximum load	t_r, t_f	–	–	200	μs
Display frequency at C_{OSC} = 680 pF; R_{OSC} = 1 MΩ	f_{LCD}	65	90	120	Hz

* V_{DD} = 5 V; T_{amb} = 25 °C.

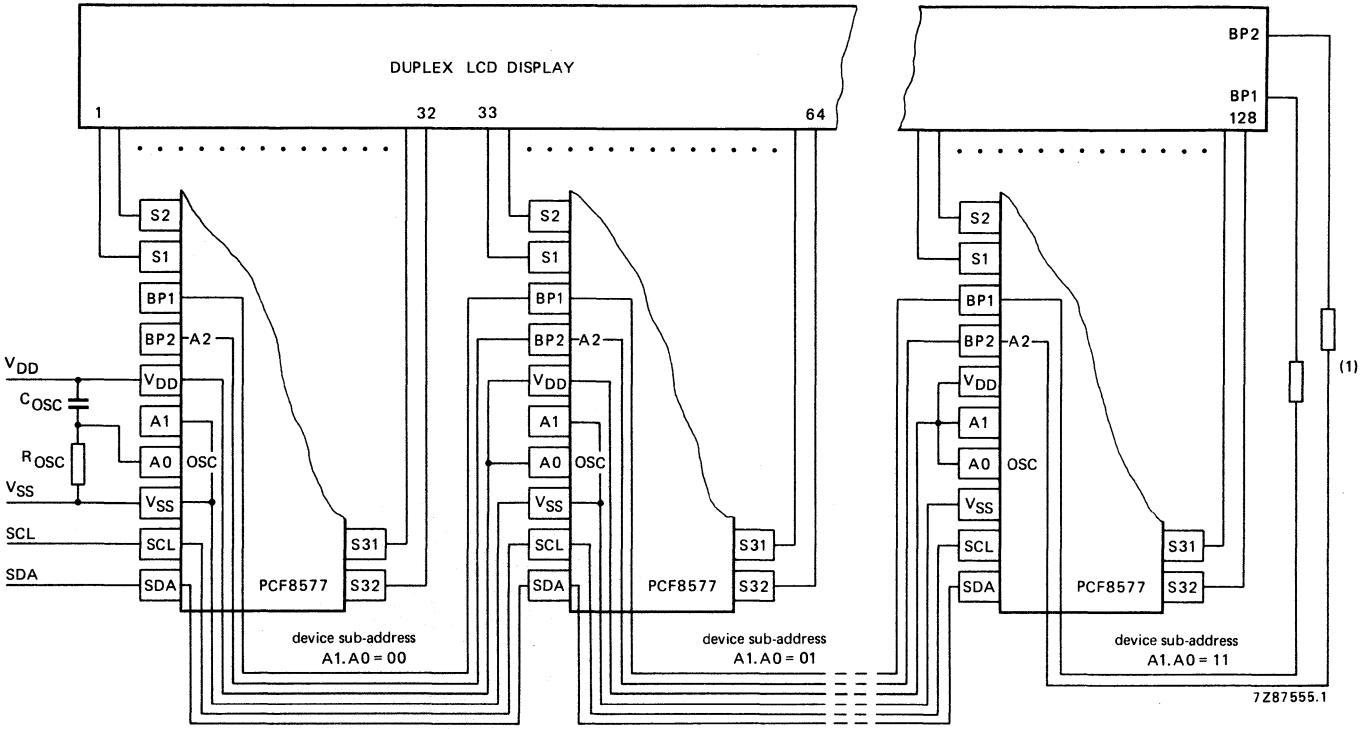
** The power-on-reset circuit resets the I²C bus logic with $V_{DD} < V_{REF}$.

APPLICATION INFORMATION



(1) The series resistance of the display backplane must be greater than 1 Ω.

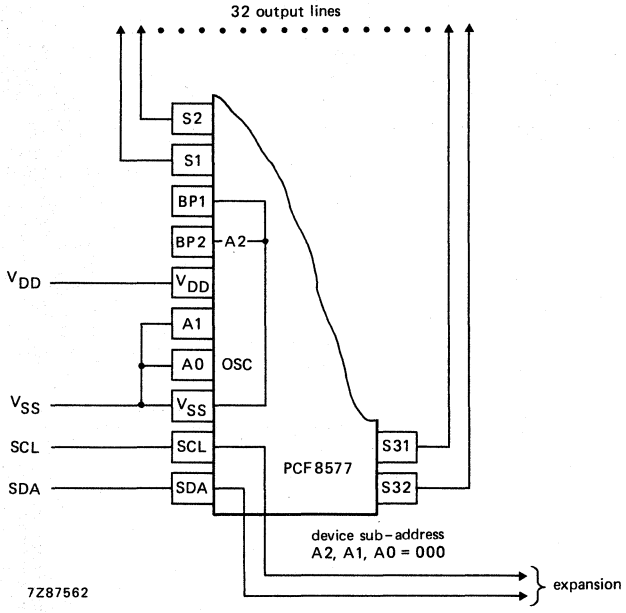
Fig. 16 Direct drive display; expansion to 256 segments using eight PCF8577.



(1) The series resistances of the display backplanes must be greater than 1 kΩ.

Fig. 17 Duplex display; expansion to 2 x 128 segments using four PCF8577.

APPLICATION INFORMATION (continued)



Notes

1. MODE bit must always be set to 0 (direct drive)
2. BANK switching is permitted
3. BP1 must always be connected to V_{SS} and A0/OSC must be connected to either V_{DD} or V_{SS} (no LCD modulation)

Fig. 18 Use of PCF8577 as 32-bit output expander in I²C bus application.

Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

8-BIT A/D AND D/A CONVERTER

GENERAL DESCRIPTION

The PCF8591 is a single chip, single supply low power 8-bit CMOS data acquisition device with four analogue inputs, one analogue output and a serial I^2C bus interface. Three address pins A0, A1 and A2 are used for programming the hardware address, allowing the use of up to eight devices connected to the I^2C bus without additional hardware. Address, control and data to and from the device are transferred serially via the two-line bidirectional bus (I^2C).

The functions of the device include analogue input multiplexing, on-chip track and hold function, 8-bit analogue-to-digital conversion and an 8-bit digital-to-analogue conversion. The maximum conversion rate is given by the maximum speed of the I^2C bus.

FEATURES

- Single power supply
- Operating supply voltage 2,5 V to 6 V
- Low standby current
- Serial input/output via I^2C bus
- Address by 3 hardware address pins
- Sampling rate given by I^2C bus speed
- 4 analogue inputs programmable as single-ended or differential inputs
- Auto-incremented channel selection
- Analogue voltage range from V_{SS} to V_{DD}
- On-chip track and hold circuit
- 8-bit successive approximation A/D conversion
- Multiplying DAC with one analogue output

APPLICATIONS

Closed loop control systems; low power converter for remote data acquisition; battery operated equipment; acquisition of analogue values in automotive, audio and TV applications.

PACKAGE OUTLINES

PCF8591P:16-lead DIL; plastic (SOT-38).
PCF8591T:16-lead mini-pack; plastic (SO-16L; SOT-162A).

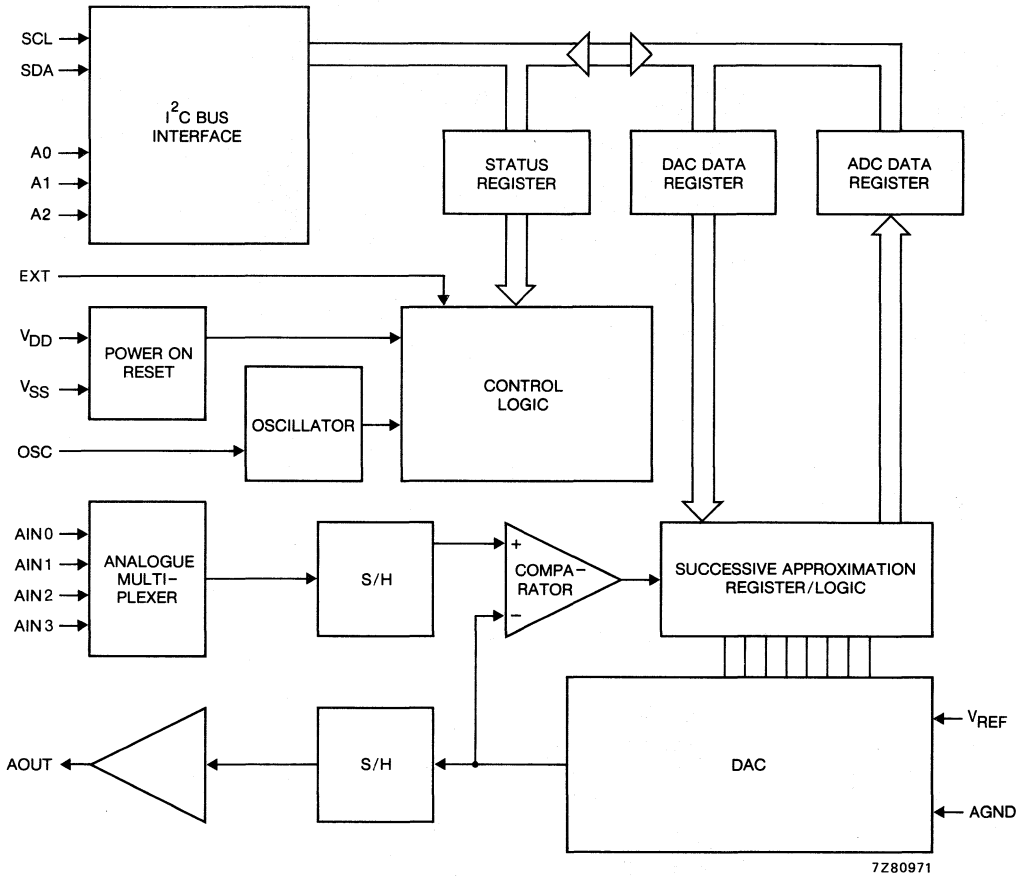


Fig. 1 Block diagram.

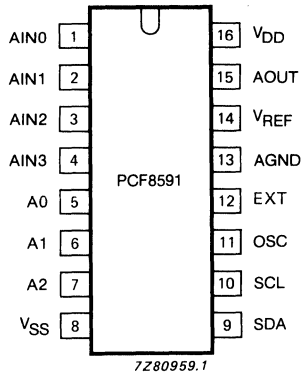


Fig. 2 Pinning diagram.

PINNING

1.	AIN0	analogue inputs (A/D converter)
2.	AIN1	
3.	AIN2	
4.	AIN3	
5.	A0	hardware address
6.	A1	
7.	A2	
8.	V_{SS}	negative supply voltage
9.	SDA	I^2C bus data input/output
10.	SCL	I^2C bus clock input/output
11.	OSC	oscillator input/output
12.	EXT	external/internal switch for oscillator input
13.	AGND	analogue ground
14.	V_{REF}	voltage reference input
15.	AOUT	analogue output (D/A converter)
16	V_{DD}	positive supply voltage

FUNCTIONAL DESCRIPTION

DEVELOPMENT DATA

Adressing

Each PCF8591 device in an I^2C bus system is activated by sending a valid address to the device. The address consists of a fixed part and a programmable part. The programmable part must be set according to the address pins A0, A1 and A2. The address always has to be sent as the first byte after the start condition in the I^2C bus protocol. The last bit of the address byte is the read/write-bit which sets the direction of the following data transfer (see Figs 3 and 10).

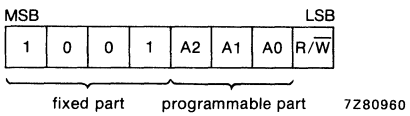


Fig. 3 Address byte.

Control byte

The second byte sent to a PCF8591 device will be stored in its control register and is required to control the device function.

The upper nibble of the control register is used for enabling the analogue output, and for programming the analogue inputs as single-ended or differential inputs. The lower nibble selects one of the analogue input channels defined by the upper nibble (see Fig. 4). If the auto-increment flag is set the channel number is incremented automatically after each A/D conversion.

The selection of a non-existing input channel results in the highest available channel number being allocated. Therefore, if the auto-increment flag is set, the next selected channel will be always channel 0. The most significant bits of both nibbles are reserved for future functions and have to be set to 0. After a power-on reset condition all bits of the control register are reset to 0. The D/A converter and the oscillator are disabled for power saving. The analogue output is switched to a high impedance state.

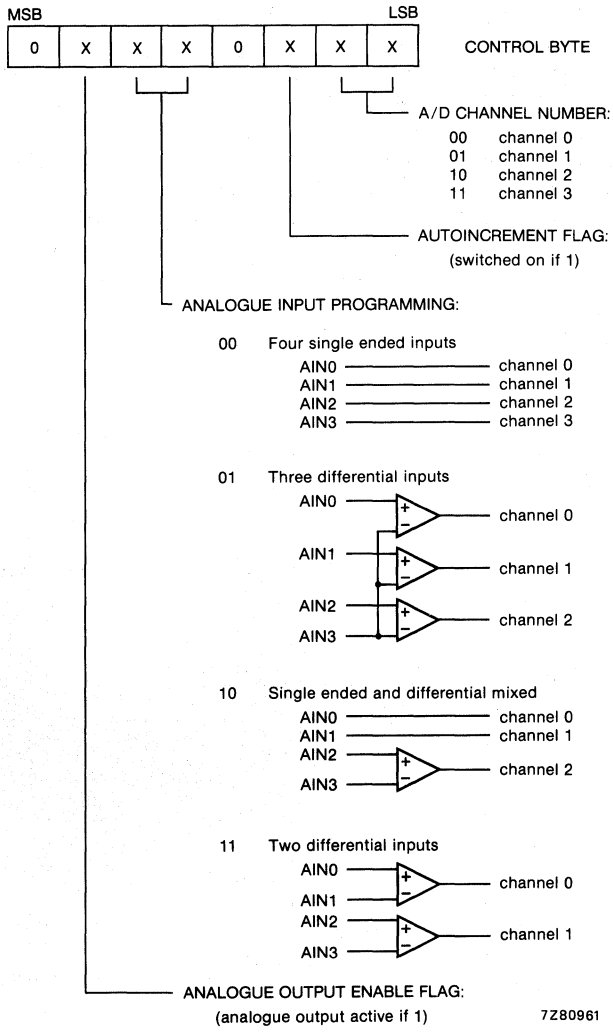


Fig. 4 Control byte.

D/A conversion

The third byte sent to a PCF8591 device is stored in the DAC data register and is converted to the corresponding analogue voltage using the on-chip D/A converter. This D/A converter consists of a resistor divider chain connected to the external reference voltage with 256 taps and selection switches. The tap-decoder switches one of these taps to the DAC output line (see Fig. 5).

The analogue output voltage is buffered by an auto-zeroed unity gain amplifier. This buffer amplifier may be switched on or off by setting the analogue output enable flag of the control register. In the active state the output voltage is held until a further data byte is sent.

The on-chip D/A converter is also used for successive approximation A/D conversion. In order to release the DAC for an A/D conversion cycle the unity gain amplifier is equipped with a track and hold circuit. This circuit holds the output voltage while executing the A/D conversion.

The output voltage supplied to the analogue output AOUT is given by the formula shown in Fig. 6. The waveforms of a D/A conversion sequence are shown in Fig. 7.

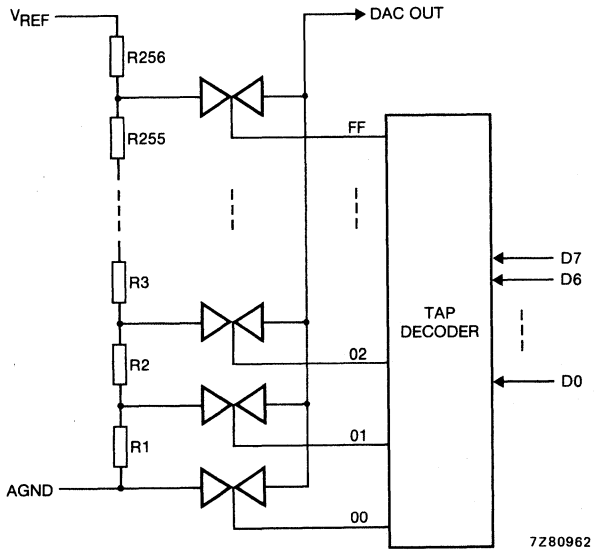


Fig. 5 DAC resistor divider chain.

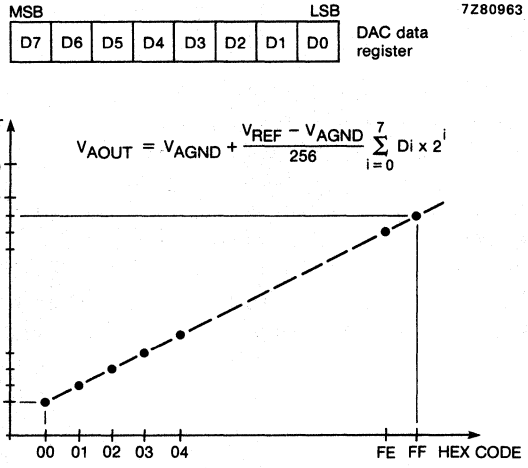


Fig. 6 DAC data and d.c. conversion characteristics.

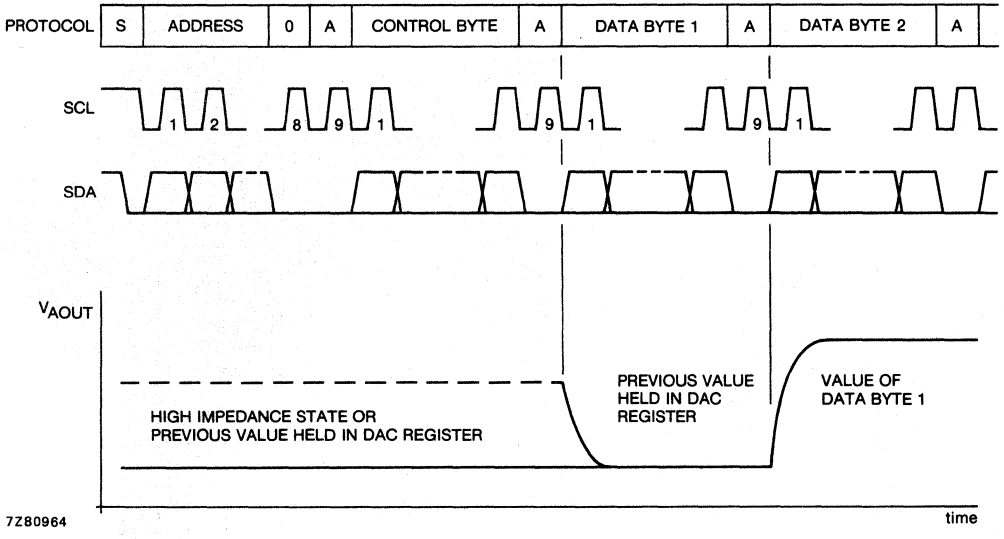


Fig. 7 D/A conversion sequence.

A/D conversion

The A/D converter makes use of the successive approximation conversion technique. The on-chip D/A converter and a high gain comparator are used temporarily during an A/D conversion cycle.

An A/D conversion cycle is always started after sending a valid read mode address to a PCF8591 device. The A/D conversion cycle is triggered at the trailing edge of the acknowledge clock pulse and is executed while transmitting the result of the previous conversion (see Fig. 8).

Once a conversion cycle is triggered an input voltage sample of the selected channel is stored on the chip and is converted to the corresponding 8-bit binary code. Samples picked up from differential inputs are converted to an 8-bit two's complement code (see Fig. 9). The conversion result is stored in the ADC data register and awaits transmission. If the auto-increment flag is set the next channel is selected.

The first byte transmitted in a read cycle contains the conversion result code of the previous read cycle. After a power-on reset condition the first byte read is a hexadecimal 80. The protocol of an I^2C bus read cycle is shown in Fig. 10.

The maximum A/D conversion rate is given by the actual speed of the I^2C bus.

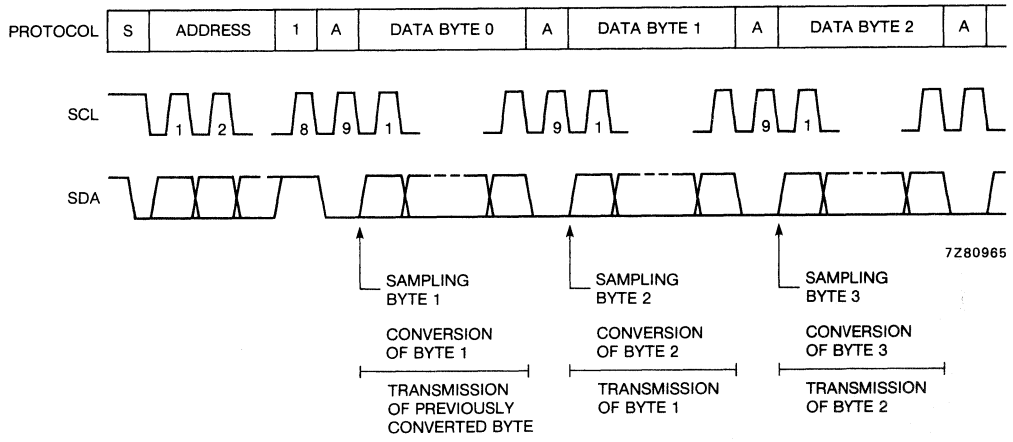


Fig. 8 A/D conversion sequence.

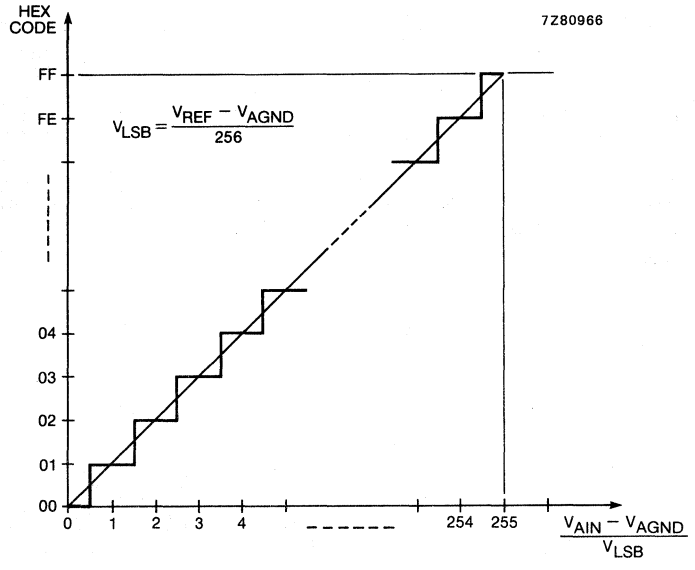


Fig. 9a A/D conversion characteristics of single-ended inputs.

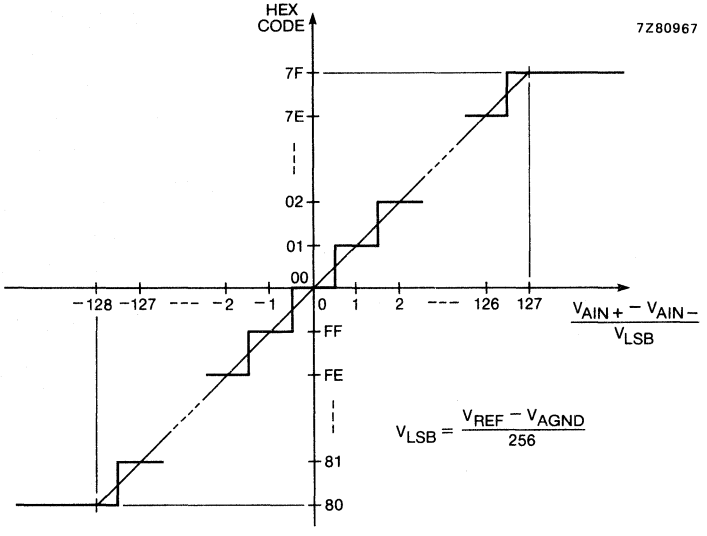


Fig. 9b A/D conversion characteristics of differential inputs.

Reference voltage

For the D/A and A/D conversion either a stable external voltage reference or the supply voltage has to be applied to the resistor divider chain (pins V_{REF} and AGND). The AGND pin has to be connected to the system analogue ground and may have a d.c. off-set with reference to V_{SS}.

A low frequency may be applied to the V_{REF} and AGND pins. This allows the use of the D/A converter as a one-quadrant multiplier; see Application Information and Fig. 6.

The A/D converter may also be used as a one or two quadrant analogue divider. The analogue input voltage is divided by the reference voltage. The result is converted to a binary code. In this application the user has to keep the reference voltage stable during the conversion cycle.

Oscillator

An on-chip oscillator generates the clock signal required for the A/D conversion cycle and for refreshing the auto-zeroed buffer amplifier. When using this oscillator the EXT pin has to be connected to V_{SS}. At the OSC pin the oscillator frequency is available.

If the EXT pin is connected to V_{DD} the oscillator output OSC is switched to a high impedance state allowing the user to feed an external clock signal to OSC.

Bus protocol

After a start condition a valid hardware address has to be sent to a PCF8591 device. The read/write bit defines the direction of the following single or multiple byte data transfer. For the format and the timing of the start condition (S), the stop condition (P) and the acknowledge bit (A) refer to the I^2C bus characteristics. In the write mode a data transfer is terminated by sending either a stop condition or the start condition of the next data transfer.

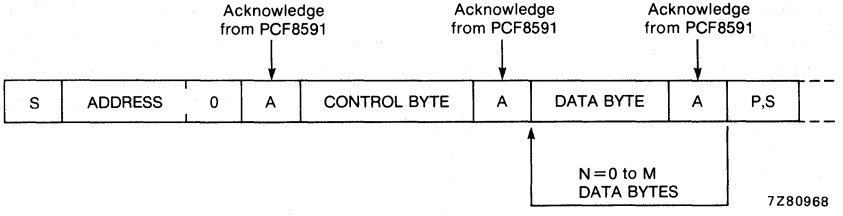


Fig. 10a Bus protocol for write mode, D/A conversion.

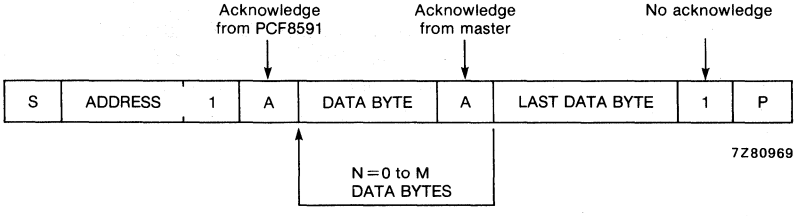


Fig. 10b Bus protocol for read mode, A/D conversion.

CHARACTERICS OF THE I²C BUS

The I²C bus is for bidirectional, two-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor. Data transfer may be initiated only when the bus is not busy.

Bit transfer

One data bit is transfered during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as a control signal.

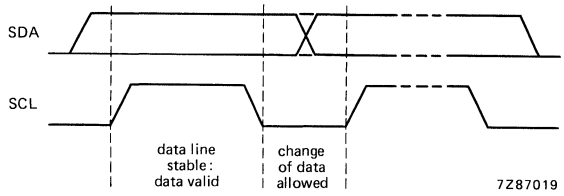


Fig. 11 Bit transfer.

Start and stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH, is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH, is defined as the stop condition (P).

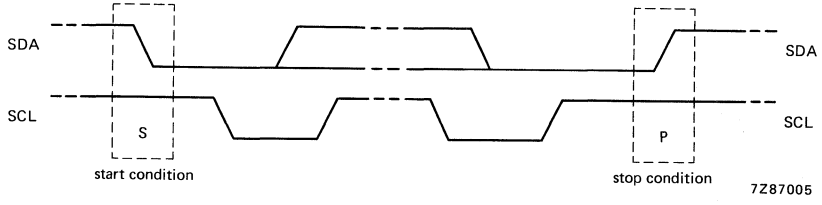


Fig. 12 Definition of start and stop condition.

System configuration

A device generating a message is a "transmitter", a device receiving a message is the "receiver". The device that controls the message is the "master" and the devices which are controlled by the master are the "slaves".

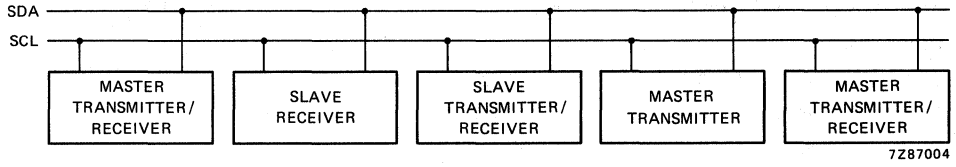


Fig. 13 System configuration.

Acknowledge.

The number of data bytes transfered between the start and stop conditions from transmitter to receiver is not limited. Each data byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master also generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse. A master receiver must signal an end of data to the transmitter by *not* generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

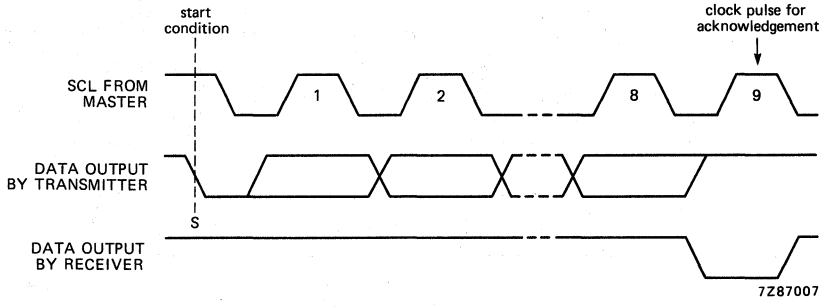


Fig. 14 Acknowledgement on the I^2C bus.

Timing specifications

All the timing values are valid within the operating supply voltage and ambient temperature range and refer to V_{IL} and V_{IH} with an input voltage swing of V_{SS} to V_{DD}.

parameter	symbol	min.	typ.	max.	unit
SCL clock frequency	f_{SCL}	–	–	100	kHz
Tolerable spike width on bus	t_{SW}	–	–	100	ns
Bus free time	t_{BUF}	4,0	–	–	μs
Start condition set-up time	$t_{SU;STA}$	4,0	–	–	μs
Start condition hold time	$t_{HD;STA}$	4,7	–	–	μs
SCL LOW time	t_{LOW}	4,7	–	–	μs
SCL HIGH time	t_{HIGH}	4,0	–	–	μs
SCL and SDA rise time	t_R	–	–	1,0	μs
SCL and SDA fall time	t_F	–	–	0,3	μs
Data set-up time	$t_{SU;DAT}$	250	–	–	ns
Data hold time	$t_{HD;DAT}$	0	–	–	ns
SCL LOW to data out valid	$t_{VD;DAT}$	–	–	3,4	μs
Stop condition set-up time	$t_{SU;STO}$	4,0	–	–	μs

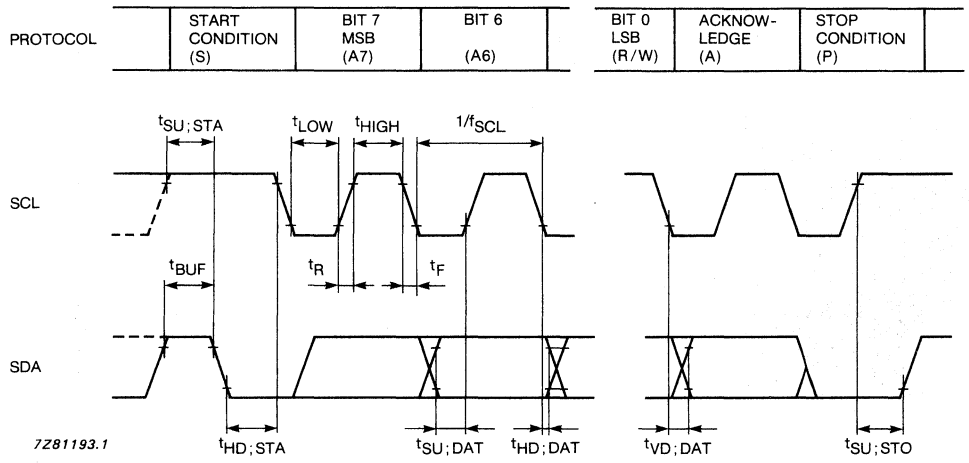


Fig. 15 I^2C bus timing diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range	V_{DD}		−0,5 to +8,0 V
Voltage on any pin	V_I		−0,5 to V_{DD} +0,5 V
Input current d.c.	I_I	max.	10 mA
Output current d.c.	I_O	max.	20 mA
V_{DD} or V_{SS} current	I_{DD}, I_{SS}	max.	50 mA
Power dissipation per package	P_{tot}	max.	300 mW
Power dissipation per output	P	max.	100 mW
Storage temperature range	T_{stg}		−65 to +150 °C
Operating ambient temperature range	T_{amb}		−40 to +85 °C

Note:

Inputs and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is advised to take handling precautions appropriate to handling MOS devices (see 'Handling MOS devices').

CHARACTERISTICS

V_{DD} = 2,5 V to 6 V; V_{SS} = 0 V; T_{amb} = −40 °C to +85 °C unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage	operating	V_{DD}	2,5	–	6,0	V
Supply current	standby $V_I = V_{SS}$ or V_{DD}; no load	I_{DD0}	–	1	15	μA
Supply current	operating; AOUT off; f_{SCL} = 100 kHz	I_{DD1}	–	125	250	μA
Supply current	AOUT active; f_{SCL} = 100 kHz	I_{DD2}	–	0,45	1,0	mA
Power-on reset level	note 1	V_{POR}	0,8	–	2,0	V
Digital inputs/output	SCL, SDA, A0, A1, A2					
Input voltage	LOW	V_{IL}	0	–	0,3 x V_{DD}	V
Input voltage	HIGH	V_{IH}	0,7 x V_{DD}	–	V_{DD}	V
Input current	leakage; $V_I = V_{SS}$ to V_{DD}	I_I	–	–	250	nA
Input capacitance		C_I	–	–	5	pF
SDA output current	leakage; HIGH at $V_{OH} = V_{DD}$	I_{OH}	–	–	250	nA
SDA output current	LOW at V_{OL} = 0,4 V	I_{OL}	3,0	–	–	mA

parameter	conditions	symbol	min.	typ.	max.	unit
Reference voltage inputs	V_{REF}, AGND					
Voltage range	reference	V_{REF}	V_{AGND}	–	V_{DD}	V
Voltage range	analogue ground	V_{AGND}	V_{SS}	–	V_{REF}	V
Input current	leakage	I_I	–	–	250	nA
Input resistance	V_{REF} to AGND	R_{REF}	–	100	–	kΩ
Oscillator	OSC, EXT					
Input current	leakage	I_I	–	–	250	nA
Oscillator frequency		f_{OSC}	0,75	–	1,25	MHz

D/A CHARACTERISTICS

V_{DD} = 5,0 V; V_{SS} = 0 V; V_{REF} = 5,0 V; V_{AGND} = 0 V; R_{load} = 10 kΩ; C_{load} = 100 pF; T_{amb} = −40 °C to +85 °C unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Analogue output						
Output voltage range	no resistive load	V_{OA}	V_{SS}	–	V_{DD}	V
Output voltage range	R_{load} = 10 kΩ	V_{OA}	V_{SS}	–	0,9xV_{DD}	V
Output current	leakage; AOUT disabled	I_{LO}	–	–	250	nA
Accuracy						
Offset error	T_{amb} = 25 °C	OS_e	–	–	50	mV
Linearity error		L_e	–	–	±1,5	LSB
Gain error	no resistive load	G_e	–	–	1	%
Settling time	to ½ LSB full scale step	t_{DAC}	–	–	90	μs
Conversion rate		f_{DAC}	–	–	11,1	kHz
Supply noise rejection	at f = 100 Hz; V_{DD} = 0,1 V_{PP}	SNRR	–	40	–	dB

DEVELOPMENT DATA

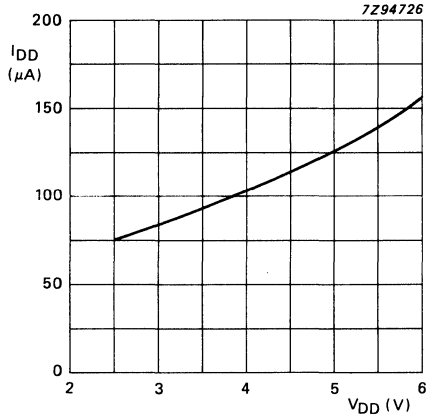
A/D CHARACTERISTICS

V_{DD} = 5,0 V; V_{SS} = 0 V; V_{REF} = 5,0 V; V_{AGND} = 0 V; R_{source} = 10 kΩ; T_{amb} = −40 °C to +85 °C unless otherwise specified

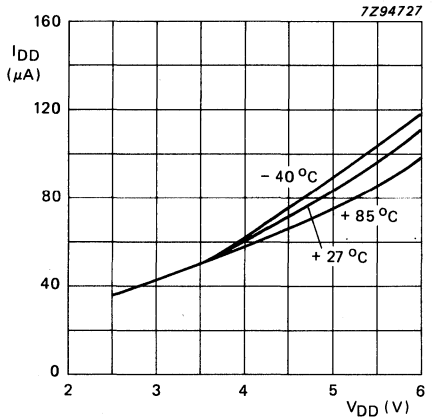
parameter	conditions	symbol	min.	typ.	max.	unit
Analogue inputs						
Input voltage range		V_{IA}	V_{SS}	–	V_{DD}	V
Input current	leakage	I_{IA}	–	–	100	nA
Input capacitance		C_{IA}	–	10	–	pF
Input capacitance	differential	C_{ID}	–	10	–	pF
Single-ended voltage	measuring range	V_{IS}	V_{AGND}	–	V_{REF}	V
Differential voltage	measuring range; $V_{FS} = V_{REF} - V_{AGND}$	V_{ID}	$\frac{-V_{FS}}{2}$	–	$\frac{+V_{FS}}{2}$	V
Accuracy						
Offset error	T_{amb} = 25 °C	OS_e	–	–	20	mV
Linearity error		L_e	–	–	±1,5	LSB
Gain error		G_e	–	–	1	%
Gain error	small-signal; ΔV_{IN} = 16 LSB	GS_e	–	–	5	%
Rejection ratio	common-mode	CMRR	–	60	–	dB
Supply noise rejection	at f = 100 Hz; $V_{DDN} = 0{,}1 \times V_{PP}$	SNRR	–	40	–	dB
Conversion time		t_{ADC}	–	–	90	μs
Sampling/conversion rate		f_{ADC}	–	–	11,1	kHz

Note

1. The power on reset circuit resets the I^2C bus logic when V_{DD} is less than V_{POR}.



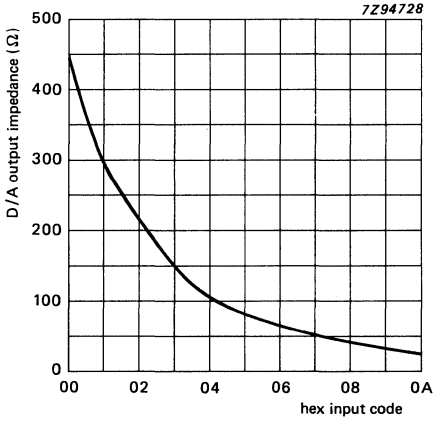
(a) internal oscillator; T_{amb} = + 27 °C.



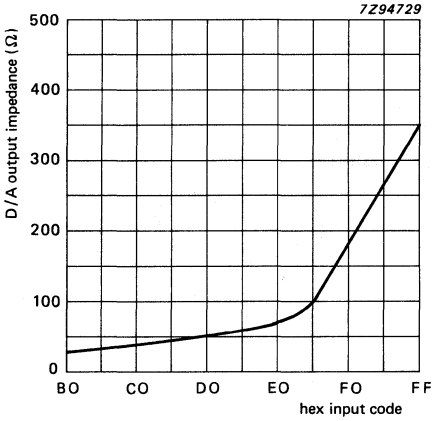
(b) external oscillator.

Fig. 16 Operating supply current against supply voltage (analogue output disabled).

DEVELOPMENT DATA



(a) output impedance near negative power rail; T_{amb} = + 27 °C.



(b) output impedance near positive power rail; T_{amb} = + 27 °C.

Fig. 17 Output impedance of analogue output buffer (near power rails).

The x-axis represents the hex input-code equivalent of the output voltage.

APPLICATION INFORMATION

Inputs must be connected to V_{SS} or V_{DD} when not in use. Analogue inputs may also be connected to AGND or V_{REF}.

In order to prevent excessive ground and supply noise and to minimize cross-talk of the digital to analogue signal paths the user has to design the printed-circuit board layout very carefully. Supply lines common to a PCF8591 device and noisy digital circuits and ground loops should be avoided. Decoupling capacitors (> 10 μF) are recommended for power supply and reference voltage inputs.

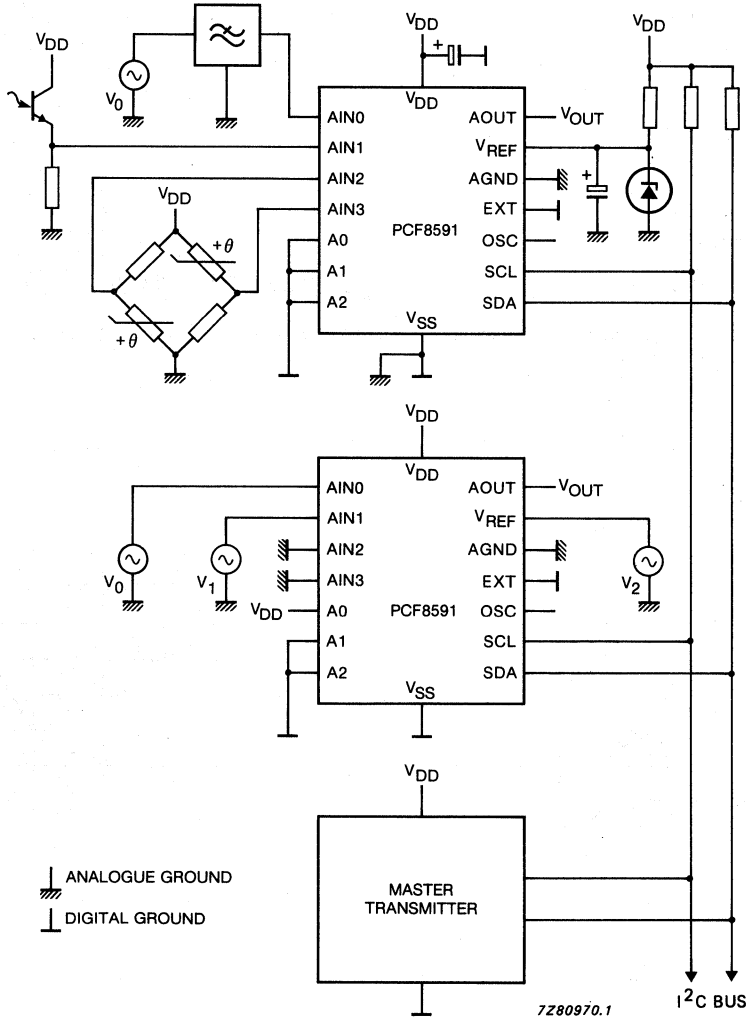


Fig. 18 Application diagram.

Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specification defined by Philips.

LOW VOLTAGE MONO/STEREO POWER AMPLIFIER

GENERAL DESCRIPTION

The TDA7050T is a low voltage audio amplifier for small radios with headphones (such as watch, pen and pocket radios) in mono (bridge-tied load) or stereo applications.

Features

- Limited to battery supply application only (typ. 3 and 4 V)
- Operates with supply voltage down to 1,6 V
- No external components required
- Very low quiescent current
- Fixed integrated gain of 26 dB, floating differential input
- Flexibility in use – mono BTL as well as stereo
- Small dimension of encapsulation (see package design example)

QUICK REFERENCE DATA

Supply voltage range	V_P	1,6 to 6,0	V
Total quiescent current (at V_P = 3 V)	I_{tot}	typ. 3,2	mA
Bridge tied load application (BTL)			
Output power at R_L = 32 Ω V_P = 3 V; d_{tot} = 10%	P_o	typ. 140	mW
D.C. output offset voltage between the outputs	$\|\Delta V\|$	max. 70	mV
Noise output voltage (r.m.s. value) at f = 1 kHz; R_S = 5 kΩ	$V_{no(rms)}$	typ. 140	μV
Stereo application			
Output power at R_L = 32 Ω d_{tot} = 10%; V_P = 3 V	P_o	typ. 35	mW
d_{tot} = 10%; V_P = 4,5 V	P_o	typ. 75	mW
Channel separation at R_S = 0 Ω; f = 1 kHz	α	typ. 40	dB
Noise output voltage (r.m.s. value) at f = 1 kHz; R_S = 5 kΩ	$V_{no(rms)}$	typ. 100	μV

PACKAGE OUTLINE

8-lead mini-pack; plastic (SO-8; SOT-96A).

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	6 V
Peak output current	I_{OM}	max.	150 mA
Total power dissipation	see derating curve Fig. 1		
Storage temperature range	T_{stg}	−55 to + 150	°C
Crystal temperature	T_c	max.	100 °C
A.C. and d.c. short-circuit duration at V_P = 3,0 V (during mishandling)	t_{sc}	max.	5 s

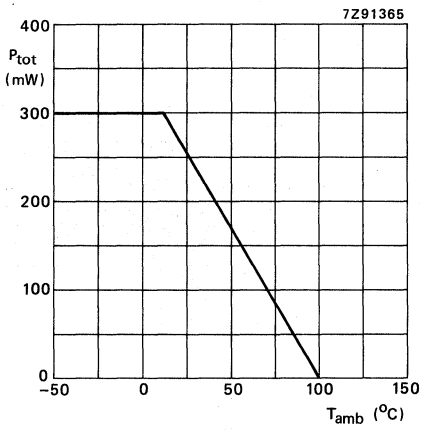


Fig. 1 Power derating curve.

SO PACKAGE DESIGN EXAMPLE

To achieve the small dimension of the encapsulation the SO package is preferred with only 8 pins. Because a heatsink is not applicable, the dissipation is limited by the thermal resistance of the 8-pin SO encapsulation until:

$$\frac{T_{j\,max} - T_{amb}}{R_{th\,j\text{-}a}} = \frac{100-60}{300} = 0{,}1\ \text{W}.$$

CHARACTERISTICS

V_P = 3 V; f = 1 kHz; R_L = 32 Ω; T_{amb} = 25 °C; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply					
Supply voltage	V_P	1,6	–	6,0	V
Total quiescent current	I_{tot}	–	3,2	4	mA
Bridge-tied load application (BTL); see Fig. 4					
Output power*					
V_P = 3,0 V; d_{tot} = 10%	P_o	–	140	–	mW
V_P = 4,5 V; d_{tot} = 10% (R_L = 64 Ω)	P_o	–	150	–	mW
Voltage gain	G_v	–	32	–	dB
Noise output voltage (r.m.s. value)					
R_S = 5 kΩ; f = 1 kHz	$V_{no(rms)}$	–	140	–	μV
R_S = 0 Ω; f = 500 kHz; B = 5 kHz	$V_{no(rms)}$	–	tbf	–	μV
D.C. output offset voltage (at R_S = 5 kΩ)	$\lvert\Delta V\rvert$	–	–	70	mV
Input impedance (at R_S = ∞)	$\lvert Z_i\rvert$	1	–	–	MΩ
Input bias current	I_i	–	40	–	nA
Stereo application; see Fig. 5					
Output power*					
V_P = 3,0 V; d_{tot} = 10%	P_o	–	35	–	mW
V_P = 4,5 V; d_{tot} = 10%	P_o	–	75	–	mW
Voltage gain	G_v	–	26	–	dB
Noise output voltage (r.m.s. value)					
R_S = 5 kΩ; f = 1 kHz	$V_{no(rms)}$	–	100	–	μV
R_S = 0 Ω; f = 500 kHz; B = 5 kHz	$V_{no(rms)}$	–	tbf	–	μV
Channel separation					
R_S = 0 Ω; f = 1 kHz	α	30	40	–	dB
Input impedance (at R_S = ∞)	$\lvert Z_i\rvert$	2	–	–	MΩ
Input bias current	I_i	–	20	–	nA

* Output power is measured directly at the output pins of the IC. It is shown as a function of the supply voltage in Fig. 2 (BTL application) and Fig. 3 (stereo application).

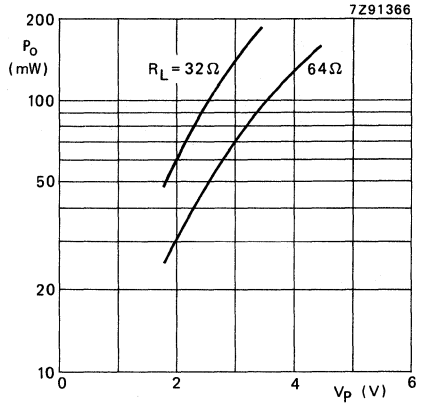


Fig. 2 Output power across the load impedance (R_L) as a function of supply voltage (V_P) in BTL application. Measurements were made at f = 1 kHz; d_{tot} = 10%; T_{amb} = 25 °C.

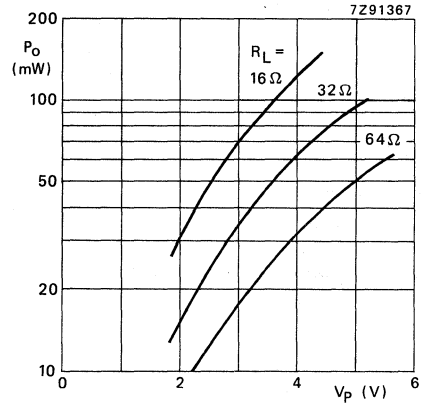


Fig. 3 Output power across the load impedance (R_L) as a function of supply voltage (V_P) in stereo application. Measurements were made at f = 1 kHz; d_{tot} = 10%; T_{amb} = 25 °C.

APPLICATION INFORMATION

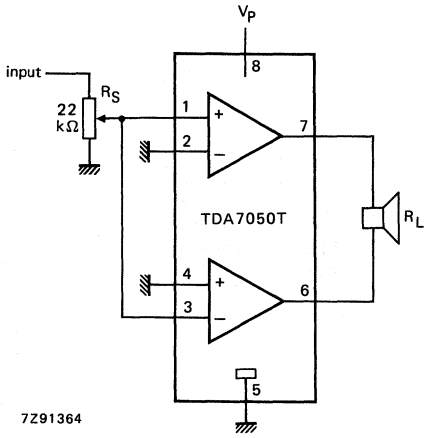


Fig. 4 Application diagram (BTL); also used as test circuit.

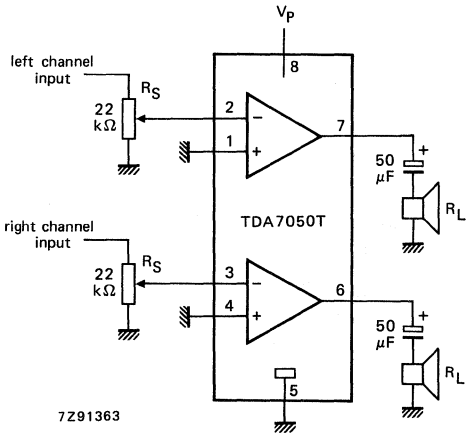


Fig. 5 Application diagram (stereo); also used as test circuit.

TELEPHONE TRANSMISSION CIRCUIT FOR HANDSFREE LOUDSPEAKING

GENERAL DESCRIPTION

The TEA1042 is a bipolar integrated circuit performing all speech and line interface functions in electronic telephone sets. It is especially designed for handsfree loudspeaking equipment.

Its features are:

- Supplied from telephone line current
- Voltage regulator with adjustable d.c. voltage drop and d.c. resistance
- High and low-impedance handset microphone inputs
- High-impedance base microphone input
- Handset/base selection input
- Muting input for pulse or DTMF dialling
- Gain setting facility on all amplifiers
- Line current dependent gain control facility with corrections for the exchange supply voltage and its feeding bridge resistance
- Supply output for additional circuits.

QUICK REFERENCE DATA

Line voltage at I_{line} = 15 mA	V_{line}	typ.	4,2 V
Line current operating range	I_{line}		10 to 140 mA
Telephone line impedance	$\|Z_{line}\|$	nom.	600 Ω
Supply current	I_{CC}	typ.	1 mA
Voltage gain, transmitting amplifier			
MIC1 input	A_{vd}	typ.	44,5 dB
MIC2 input	A_{vd}	typ.	20 dB
MIC3 input	A_{vd}	typ.	20 dB
DTMF input	A_{vd}	typ.	26 dB
Voltage gain, receiving amplifier	A_{vd}	typ.	27 dB
Gain adjustment range			
transmitting amplifier	ΔA_{vd}	typ.	± 6 dB
receiving amplifier	ΔA_{vd}	typ.	± 8 dB
Range of gain control with line current, all amplifiers	ΔA_{vd}	typ.	6 dB
Exchange supply voltage range	V_{exch}		24 to 60 V
Exchange feeding bridge resistance	R_{exch}		400 or 800 Ω
Operating ambient temperature range	T_{amb}		−25 to + 70 °C

PACKAGE OUTLINE

24-lead DIL; plastic (SOT-101A).

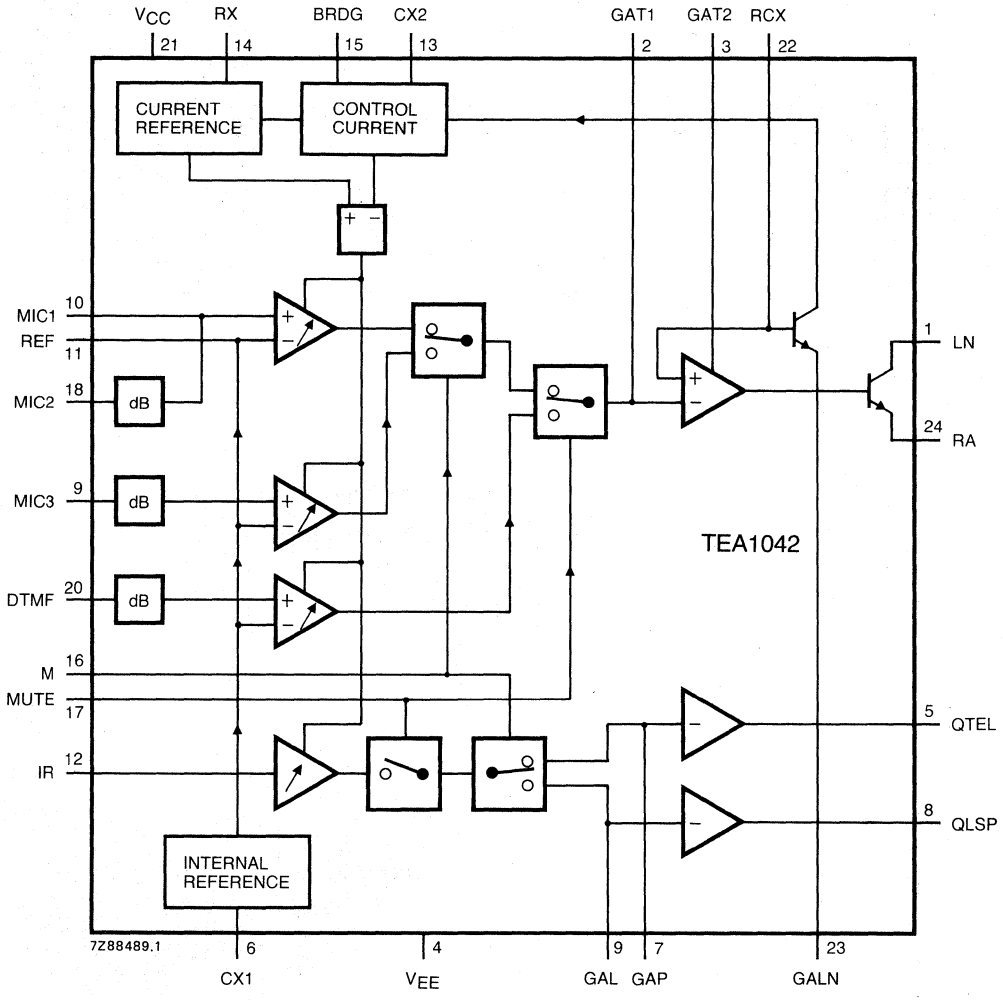


Fig. 1 Block diagram. The blocks marked dB are attenuators. The M and MUTE inputs operate analogue switches that activate or inhibit the inputs and outputs as required by their function.

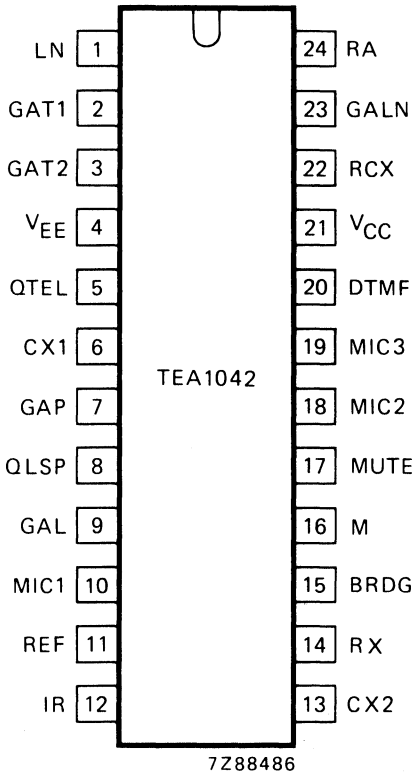


Fig. 2 Pinning diagram.

PINNING

1	LN	positive line terminal
2	GAT1	gain adjustment; transmitting amplifier
3	GAT2	gain adjustment; transmitting amplifier
4	V_{EE}	negative line terminal
5	QTEL	handset telephone output
6	CX1	reference decoupling
7	GAP	gain adjustment; telephone amplifier
8	QLSP	loudspeaker preamplifier output
9	GAL	gain adjustment; loudspeaker preamplifier
10	MIC1	low-impedance handset microphone input
11	REF	reference voltage
12	IR	receiving amplifier input
13	CX2	external stabilizing capacitor
14	RX	external resistor
15	BRDG	selection input for gain control adaptation to feeding bridge impedance
16	M	mode (handset/base selection) input
17	MUTE	mute input
18	MIC2	high-impedance handset microphone input
19	MIC3	base microphone input
20	DTMF	dual-tone multi-frequency input
21	V_{CC}	positive supply
22	RCX	line voltage adjustment and voltage regulator decoupling
23	GALN	gain control with line current; all amplifiers
24	RA	d.c. resistance adjustment

FUNCTIONAL DESCRIPTION

The TEA1042 contains two receiving amplifiers, a transmitting amplifier, means to switch the inputs and the outputs, means to adjust the gain of all amplifiers individually, means to vary the gain with the line current and means to adjust the d.c. voltage drop and d.c. resistance. See the block diagram, Fig. 1.

Supply: LN, V_{CC}, V_{EE}, RA, CX1 and CX2 (pins 1, 21, 4, 24, 6 and 13)

The circuit is supplied from the line current, the arrangement is shown in Fig. 3. The circuit develops its own supply voltage at V_{CC} (pin 21). This supply voltage may also be used to supply an external circuit, e.g. a CMOS pulse or DTMF dialler or an electret microphone amplifier stage. The current available for this circuit depends on external components, see Fig. 4.

All line current has to flow through the circuit. If the line current exceeds the current required by the circuit itself via V_{CC} (pin 21), i.e. about 1 mA, plus the current required by the peripheral circuits connected to this pin, then the excess current is diverted via LN, the positive line terminal (pin 1), to RA (d.c. resistance adjustment; pin 24).

The minimum line voltage may be chosen by external resistor R5 and the variation with line current by external resistor R10. The circuit regulates the line voltage at T_{amb} = 25 °C to:

$$V_{line} = V_{LN} = \frac{R5 + R9}{R9} \times 0{,}62 + I_{LN} \times R10,$$

I_{LN} being the current diverted via LN.

A regulator decoupling capacitor has to be connected between RCX (pin 22) and V_{EE}, the negative line terminal (pin 4), a smoothing capacitor has to be connected between V_{CC} (pin 21) and V_{EE}, and a stabilizing capacitor between CX2 (pin 13) and V_{EE}. Further a decoupling capacitor has to be connected between CX1 (reference decoupling; pin 6) and V_{EE} (pin 4).

The dynamic impedance that the circuit presents to the line in the speech band is determined primarily by resistor R1 connected between LN (pin 1) and V_{CC} (pin 21).

Mode (handset/base selection) input M (pin 16)

The mode input permits selection of operation via the handset or via the base. A HIGH level on the M input or an open circuit selects handset operation, i.e. it activates the microphone inputs MIC1 and MIC2 and the handset telephone output QTEL. A LOW level on M selects the base microphone input MIC3 and the loudspeaker preamplifier output QLSP.

Microphone inputs MIC1, MIC2 and MIC3 (pins 10, 18 and 19)

Handset and base may be equipped with a sensitive microphone, e.g. an electret microphone with pre-amplifier. This has to be connected to the MIC2 or MIC3 input respectively. The available gain from these inputs is typ. 20 dB.

The handset may also be equipped with an insensitive low-impedance microphone, e.g. a dynamic or magnetic microphone. This has to be connected between MIC1 (pin 10) and (REF (pin 11). The available gain from this input is typ. 44,1 dB.

Dual-tone multi-frequency input DTMF and mute input MUTE (pins 20 and 17)

A HIGH level on the MUTE input inhibits all microphone inputs and the telephone and loudspeaker outputs QTEL and QLSP and enables the DTMF input, a LOW level does the reverse. Switching the MUTE input will not produce any clicks on the line or in the telephone or loudspeaker. The available gain from the DTMF input is typ. 25,6 dB.

Telephone output QTEL and loudspeaker preamplifier output QLSP (pins 5 and 8)

As described before, the M input determines which of the outputs QTEL and QLSP will be activated. The receiving amplifier input IR (pin 12) is the input for both outputs. For both outputs the available gain is typ. 27 dB. The output QTEL is intended for telephone capsules with an impedance of 150 Ω or more. The QLSP output is intended to drive a power amplifier. Its output impedance is less than 1 kΩ.

Gain adjustment: GAT1, GAT2, GAP and GAL (pins 2, 3, 7 and 9)

The gain of the transmitting amplifier may be adjusted by an external resistor R2 connected between GAT1 and GAT2 (pins 2 and 3; see Fig. 9). This adjustment influences the sensitivity of the inputs MIC1, MIC2, MIC3 and DTMF to the same amount. The gain is proportional to R2 and inversely proportional to R10 and R12.

The gain of the telephone amplifier may be adjusted by an external resistor R14 between GAP (pin 7) and CX1 (pin 6). The gain is proportional to R14 and inversely proportional to R12.

The gain of the loudspeaker preamplifier may be adjusted by an external resistor R13 between GAL (pin 9) and CX1 (pin 6). The gain is proportional to R13 and inversely proportional to R12.

Gain control with line current: GALN (pin 23)

The circuit offers a facility to automatically vary the gain of all its amplifiers with the line current. In this way the circuit compensates for differences in line attenuation. The variation is accomplished by connecting an external resistor R11 between GALN (pin 23) and V_{EE} (pin 4). The value of this resistor should be chosen in accordance with the supply voltage of the exchange (see Figs 5 and 6).

If no gain variation with line current is required the GALN connection may be left open. All amplifiers have their maximum gain then.

Selection input for gain control adaptation to feeding bridge impedance: BRDG (pin 15)

A LOW level at the BRDG input optimizes the gain control characteristics of the circuit for a 400 Ω feeding bridge in the exchange, a HIGH level for 800 Ω.

Side tone suppression

In the circuit diagram shown in Fig. 9 side tone suppression is obtained with components C2, R3, R4, R7 and R8. Their component values have to be chosen to suit the cable type used. This network attenuates the signal from the telephone line to the IR input of the receiving amplifier. This attenuation may be adjusted by choosing the value of R7 without affecting the side tone suppression.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply current			
d.c.	I_{line}	max.	140 mA
non-repetitive ($t < 100$ h)	I_{line}	max.	250 mA
Storage temperature range	T_{stg}	−40 to +125	°C
Operating ambient temperature range	T_{amb}	−25 to +70	°C
Junction temperature	T_j	max.	150 °C

CHARACTERISTICS

I_{line} = 10 to 140 mA; f = 1000 Hz; T_{amb} = 25 °C, unless otherwise specified.

parameter	symbol	min.	typ.	max.	unit
Supply: LN and V_{CC} (pins 1 and 21)					
Line voltage					
I_{line} = 15 mA	V_{line}	4,05	4,25	4,45	V
I_{line} = 50 mA	V_{line}	4,7	5,1	5,5	V
I_{line} = 100 mA	V_{line}	5,2	6,1	7,0	V
Variation with temperature	$-\Delta V_{line}/\Delta T$	10	12	14	mV/K
Line current operating range	I_{line}	10	–	140	mA
Supply current at V_{CC} = 2,3 V; I_{line} = 15 mA	I_{CC}	–	–	1,6	mA
V_{CC} = 2,3 V; I_{line} = 15 mA; T_{amb} = 55 °C	I_{CC}	–	–	1,0	mA
Mode (handset/base selection) input M (pin 16)					
Input voltage					
HIGH level	V_{IH}	1	–	V_{CC}	V
LOW level	V_{IL}	0	–	0,2	V
Input current	$-I_{16}$	–	8	20	μA
Attenuation of non-selected signals	$-\Delta A_{vd}$	45	–	–	dB
Low-impedance handset microphone input MIC1 and reference voltage pin REF (pins 10 and 11)					
Input impedance	$\lvert Z_{10\text{-}11}\rvert$	2,3	3	3,6	kΩ
Voltage gain, see Fig. 7	A_{vd}	43,5	44,5	45,5	dB
High-impedance handset microphone input MIC2 (pin 18)					
Input impedance	$\lvert Z_{18\text{-}4}\rvert$	36,4	47	57,6	kΩ
Voltage gain, see Fig. 7	A_{vd}	19,3	20,2	21,2	dB
Base microphone input MIC3 (pin 19)					
Input impedance	$\lvert Z_{19\text{-}4}\rvert$	36,4	47	57,6	kΩ
Voltage gain, see Fig. 7	A_{vd}	19,3	20,2	21,2	dB
DTMF input (pin 20)					
Input impedance	$\lvert Z_{20\text{-}4}\rvert$	12	15,5	18,9	kΩ
Voltage gain, see Fig. 7	A_{vd}	25	26	26,9	dB
Gain adjustment pins; transmitting amplifier: GAT1 and GAT2 (pins 2 and 3)					
Gain adjustment range	ΔA_{vd}	–	± 6	–	dB
Gain variation with frequency, f = 300 to 4000 Hz	ΔA_{vd}	–	± 0,5	–	dB
Gain variation with temperature at I_{line} = 50 mA; T_{amb} = −5 to +45 °C	ΔA_{vd}	–	± 0,5	–	dB

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Transmitting amplifier output LN (pin 1)					
Output voltage at I_{line} = 15 mA; R_{line} = 600 Ω; d = 2%	$v_{LN(rms)}$	1,4	–	–	V
Psophometrically weighted* noise output voltage at I_{line} = 15 mA; R_{line} = 600 Ω	$v_{LN(rms)}$	–	−70	–	dBmp
MUTE input (pin 17)					
Input voltage					
HIGH level	V_{IH}	1	–	V_{CC}	V
LOW level	V_{IL}	0	–	0,1	V
Input current	$-I_{17}$	–	8	20	μA
Attenuation of non-selected signals	$-\Delta A_{vd}$	45	–	–	dB
Receiving amplifier input IR (pin 12)					
Input impedance	$\lvert Z_{12\text{-}4}\rvert$	7,8	10	12,3	kΩ
Telephone output QTEL (pin 5)					
Voltage gain at I_{line} = 15 mA; R_{load} = 150 Ω; R13 = 15 kΩ; see Fig. 8	A_{vd}	25,4	26,6	27,8	dB
Gain variation with frequency, f = 300 to 4000 Hz	ΔA_{vd}	–	±0,5	–	dB
Gain variation with temperature at I_{line} = 50 mA; T_{amb} = −5 to +45 °C	ΔA_{vd}	–	±0,5	–	dB
Maximum output voltage at I_{line} = 15 mA; R_{load} = 150 Ω; d = 2%	$v_{O(rms)}$	325	–	–	mV
Psophometrically weighted* noise output voltage at I_{line} = 15 mA	$v_{O(rms)}$	–	40	–	μV
Gain adjustment pin; telephone amplifier: GAP (pin 7)					
Gain adjustment range	ΔA_{vd}	–	±8	–	dB
Loudspeaker preamplifier output QLSP (pin 8)					
Voltage gain at I_{line} = 15 mA; R_{load} = 10 kΩ; R14 = 15 kΩ; see Fig. 8	A_{vd}	26,6	27,6	28,6	dB
Gain variation with frequency, f = 300 to 4000 Hz	ΔA_{vd}	–	±0,5	–	dB
Gain variation with temperature	ΔA_{vd}	–	±0,5	–	dB
Psophometrically weighted* noise output voltage at I_{line} = 15 mA	$v_{O(rms)}$	–	40	–	μV
Output impedance	$\lvert Z_{8\text{-}4}\rvert$	–	–	1	kΩ
Gain adjustment pin; loudspeaker preamplifier: GAL (pin 9)					
Gain adjustment range	ΔA_{vd}	–	±8	–	dB

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Selection input for gain control adaptation to feeding bridge impedance BRDG (pin 15)					
Input voltage					
HIGH level	V_{IH}	1	–	V_{CC}	V
LOW level	V_{IL}	0	–	0,1	V
Input current	$-I_{15}$	–	8	20	μA
Gain control with line current pin GALN (pin 23)					
Gain control range	ΔA_{vd}	–	6	–	dB
Highest line current for maximum gain, R11 = 105 kΩ;					
BRDG = HIGH (R_{exch} = 800 Ω)	I_{line}	22,5	25	27,5	mA
BRDG = LOW (R_{exch} = 400 Ω)	I_{line}	31,5	35	38,5	mA
Lowest line current for minimum gain, R11 = 105 kΩ;					
BRDG = HIGH (R_{exch} = 800 Ω)	I_{line}	49,5	55	60,5	mA
BRDG = LOW (R_{exch} = 400 Ω)	I_{line}	81	90	99	mA

* P53 curve.

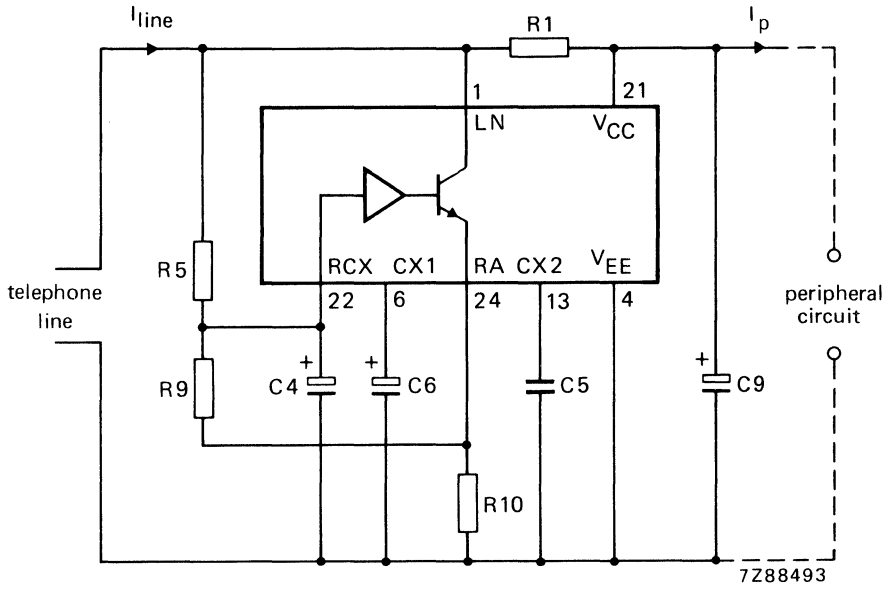


Fig. 3 Supply arrangement.

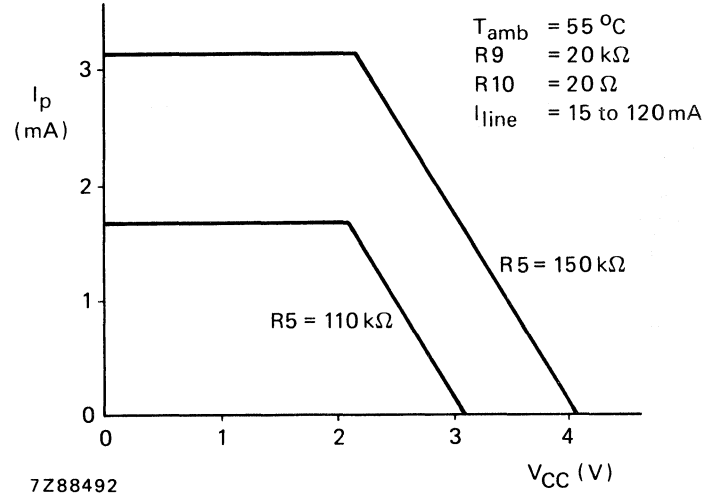


Fig. 4 Maximum current I_p available from V_{CC} for external (peripheral) circuits.

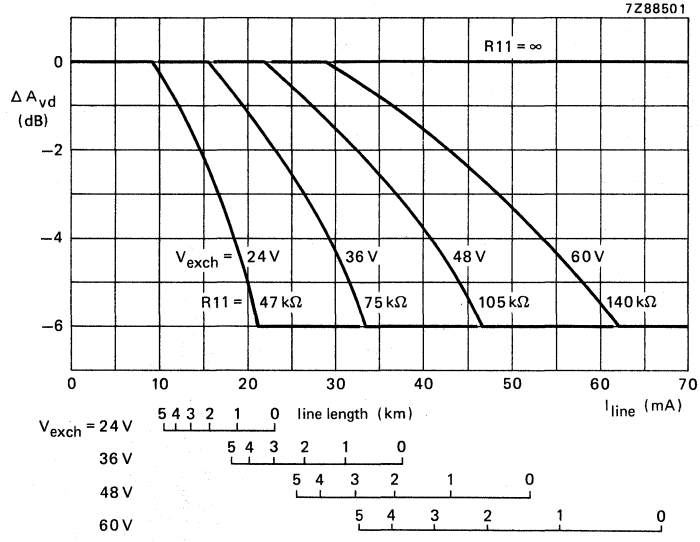


Fig. 5 Gain variation with line current, with R11 as a parameter, and with the BRDG input HIGH, i.e. the circuit optimized for 800 Ω. The values chosen for R11 suit the usual values for the supply voltage of the exchange. The curves are valid for 0,5 mm twisted-pair cables with an attenuation of 1,2 dB/km and a d.c. resistance of 176 Ω/km.

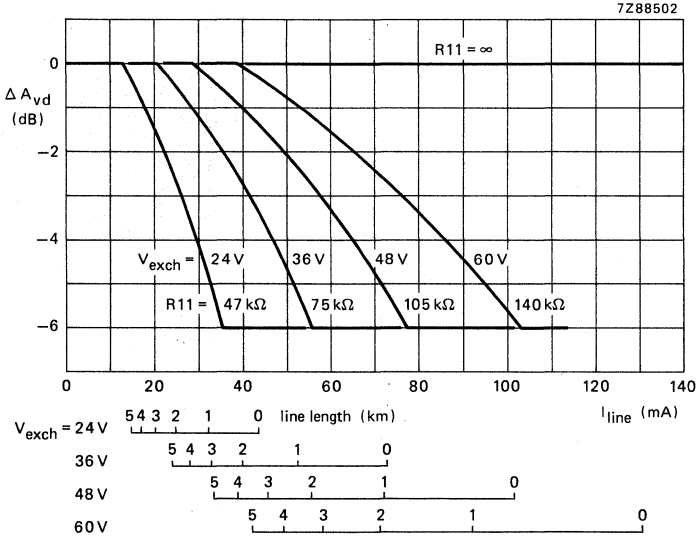


Fig. 6 Gain variation with line current, with R11 as a parameter, and with the BRDG input LOW, i.e. the circuit optimized for 400 Ω. The values chosen for R11 suit the usual values for the supply voltage of the exchange. The curves are valid for 0,5 mm twisted-pair cables with an attenuation of 1,2 dB/km and a d.c. resistance of 176 Ω/km.

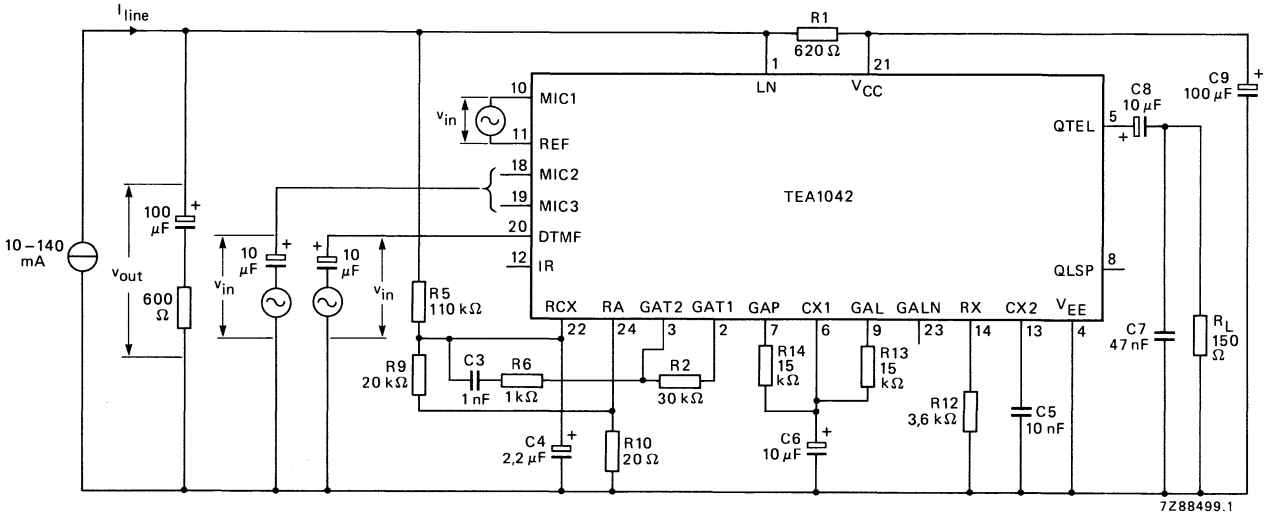


Fig. 7 Test circuit for defining voltage gain of MIC1, MIC2, MIC3 and DTMF inputs. Gain is defined as: $A_{vd} = 20 \log |v_{out}/v_{in}|$. For measuring the MIC1 or MIC2 input the M input should be HIGH and the MUTE input LOW, for measuring the MIC3 input M and MUTE should both be LOW and for measuring the DTMF input M and MUTE should be HIGH. Inputs not under test should be open.

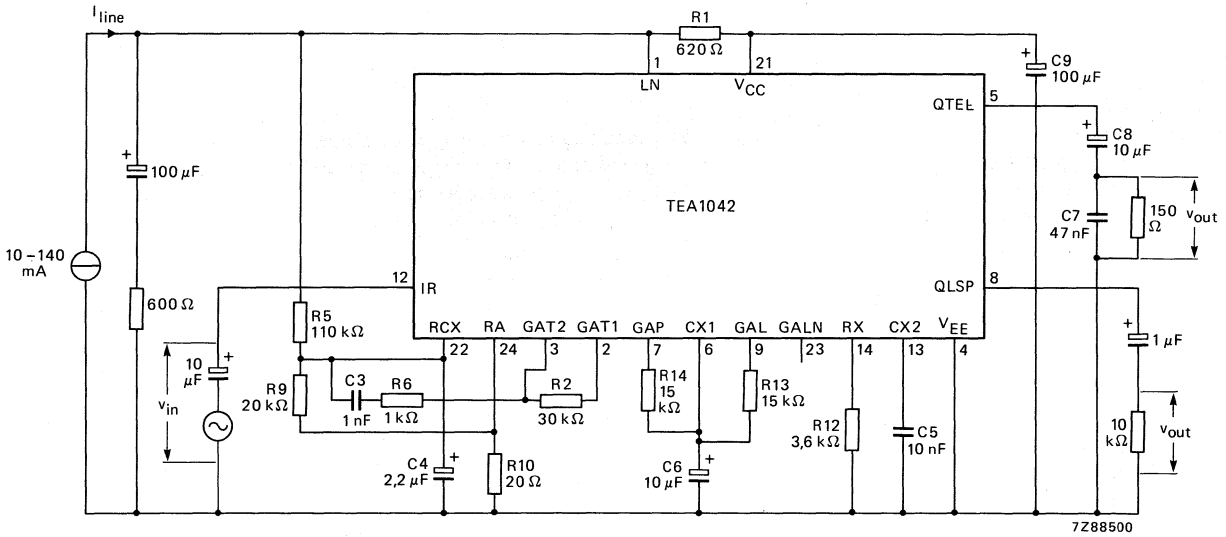


Fig. 8 Test circuit for defining voltage gain of QTEL and QLSP outputs. Gain is defined as: $A_{vd} = 20 \log |v_{out}/v_{in}|$. For measuring the QTEL output the M input should be HIGH and the MUTE input LOW, for measuring the QLSP output M and MUTE should both be LOW.

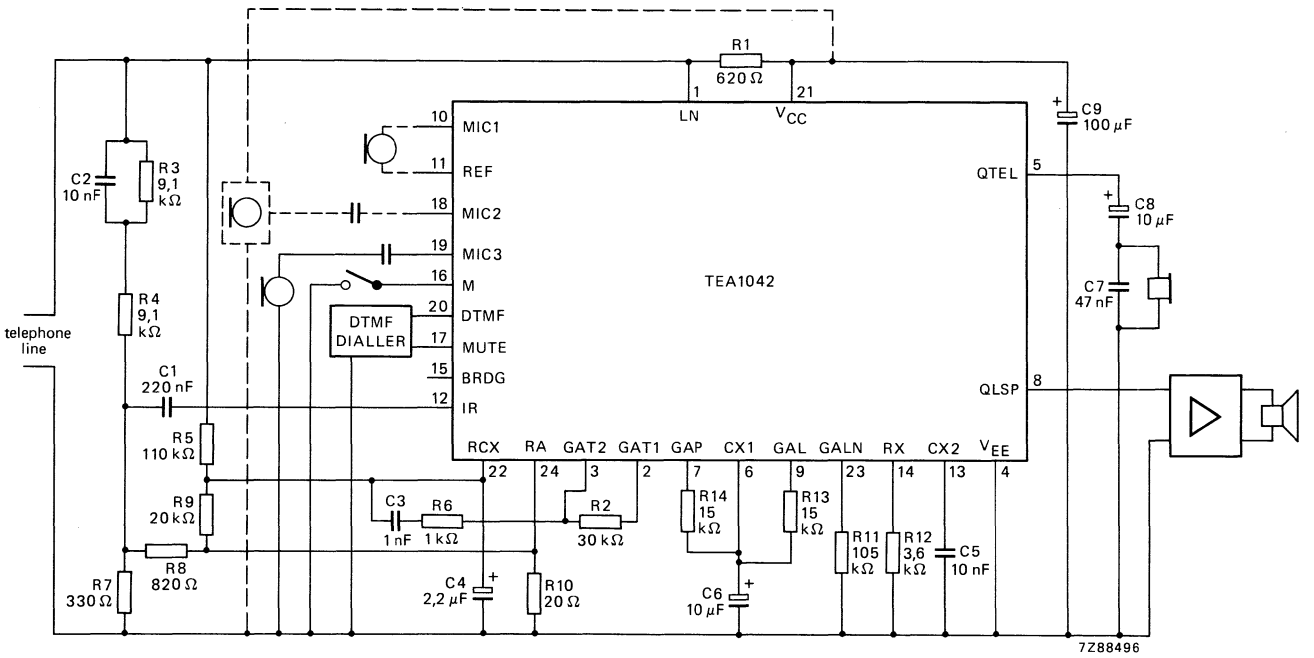


Fig. 9 Typical application of the TEA1042 in an electronic handsfree telephone set. The connections to the MIC1 and MIC2 inputs are alternatives. The connection to the BRDG input is not shown, see the Functional Description. The diagram does not show voice switches and associated control circuits required in a practical circuit for stable loudspeaking operation.

APPLICATION INFORMATION SUPPLIED ON REQUEST

DTMF/SPEECH TRANSMISSION INTEGRATED CIRCUIT FOR TELEPHONE APPLICATIONS

This integrated circuit is a dual-tone multi-frequency (DTMF) generator and a speech transmission circuit on a single chip. It supplies frequency combinations in accordance with CCITT recommendations for use in push-button telephones. It can be operated with a single contact keyboard or via a direct interface with a microcomputer. I^2L technology allows digital and analogue functions to be implemented on the same chip.

The speech-transmission part incorporates microphone and telephone amplifiers, anti-sidetone and line adaption. The microphone inputs, suitable for different types of transducer, are symmetrical to allow long cable connections with good immunity against radio-frequency interference.

The logic inputs contain an interference circuit to guarantee well defined states and on and off resistance of the keyboard contacts.

Features

- stabilized DTMF levels to be set externally
- wide operating range of line current and temperature
- no individual DTMF level adjustments required
- microcomputer compatible logic inputs
- gain setting for microphone and receiver amplifiers
- internally generated electronic muting
- low spreads on amplifier gains
- low number of external components
- on-chip oscillator for 3,58 MHz crystal

QUICK REFERENCE DATA

Line voltage	V_L	typ. 4,8	V
Line current	I_L	10 to 120	mA
Adjustable dynamic resistance	R_i	600 to 900	Ω
Microphone signal amplification	A_M	typ. 50	dB
Receiver signal amplification	A_T	typ. 20	dB
DTMF tone levels (adjustable)			
lower tones	V_{LG}	max. −6	dBm
higher tones	V_{HG}	max. −4	dBm
Operating temperature range	T_{amb}	−25 to + 70	°C

PACKAGE OUTLINE

TEA1046P: 24-lead DIL, plastic (SOT-101A).

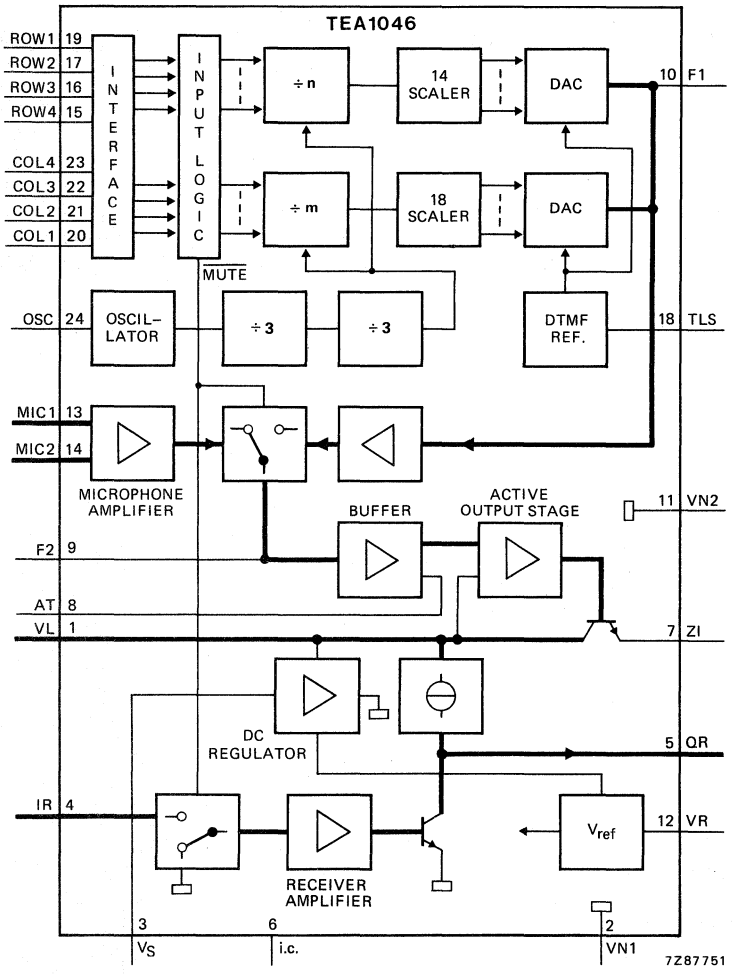


Fig. 1 Functional block diagram.

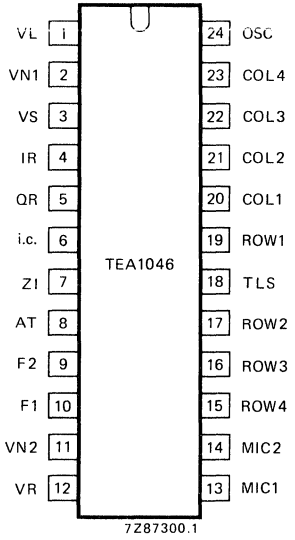


Fig. 2 Pinning diagram.

PINNING

1	VL	positive line voltage
2	VN1	negative line voltage
3	VS	voltage stabilizer filter
4	IR	receiver amplifier input
5	QR	receiver amplifier output
6	i.c.	internally connected
7	ZI	impedance setting input
8	AT	anti-sidetone output
9	F2	second filter
10	F1	first filter
11	VN2	negative line voltage
12	VR	reference voltage output
13	MIC1	microphone input (pos.)
14	MIC2	microphone input (neg.)
15	ROW4	row input 941 Hz/BCD input
16	ROW3	row input 852 Hz/BCD input
17	ROW2	row input 770 Hz/BCD input
18	TLS	DTMF level setting
19	ROW1	row input 697 Hz/BCD input
20	COL1	column input 1209 Hz/mute input
21	COL2	column input 1336 Hz/mute input
22	COL3	column input 1477 Hz/enable input
23	COL4	column input 1633 Hz/mute input
24	OSC	oscillator input

FUNCTIONAL DESCRIPTION

Voltage regulator (Fig. 3)

Different line lengths and feeding bridge resistances of the exchange cause a large line current range to supply this circuit. As all functions on this chip are working within a total current of 10 mA, the rest of the line current is shunted by the voltage regulator circuit. It regulates the voltage drop over the circuit on a nominal level of 4,8 V.

The capacitor connected to input VS provides a low-pass filter function to avoid influence of the audio signals on the line.

The static behaviour of the voltage regulator is expressed by:

$$V_L = V_o + (I_L - I_i)\ R13$$

where V_o = 4,8 V at T_{amb} = 25 °C and R13 = 5 Ω, I_i = 10 mA.

The dynamic impedance of the regulator is equivalent to a resistor in series with a simulated inductor:

$$Zr\ (\omega) = R_{eq} + j\omega L_{eq}$$

where R_{eq} = R13 = 5 Ω
$L_{eq} \approx$ 5 H (C_{VS} = 68 μF).

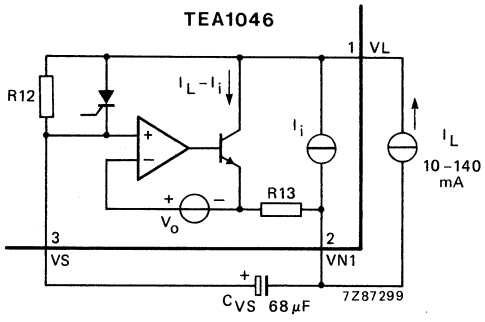


Fig. 3 Voltage regulator principle.

Within limited values, the d.c. level V_L can be decreased by connecting a resistor in parallel with R12, or increased by connecting a resistor in parallel with C_{VS}. The shunt regulator contains a thyristor which short-circuits R12 for a short period during switch-on time; this reduces the overshoot voltage to only 1 V above the level set by the regulator.

Active output stage

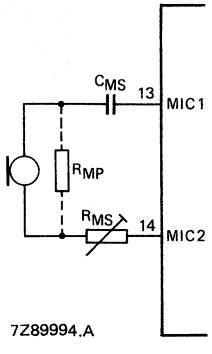
The amplifier consists of a voltage to current converter with a class-A output stage. Because of the feedback from the line to the input the circuit acts as a dynamic resistance (R_a). This resistance can be adjusted by the external resistor R_{ZI} (Fig. 11) and the value can be found by:

$$R_a = 8{,}93 \times R_{ZI}\ (\Omega)$$

The total dynamic resistance R_i equals R_a parallel with the resistance R_P of all other circuit parts, which value is approximately 7 kΩ.
With R_{ZI} = 75 Ω, R_a = 670 Ω and R_i = 610 Ω.
For R_{ZI} = 120 Ω, R_a = 1070 Ω and R_i = 900 Ω.

Microphone amplifier (Figs 4 and 5)

Pins 13 and 14 respectively are the non-inverting and inverting inputs for the microphone. The purely symmetrical inputs are suitable for low ohmic dynamic or magnetic capsules. The input impedance equals 4 kΩ. The voltage amplification from microphone input to pin 1 (VL) is 50 dB and if a lower gain is required the attenuation for a series resistor R_{MS} will be:

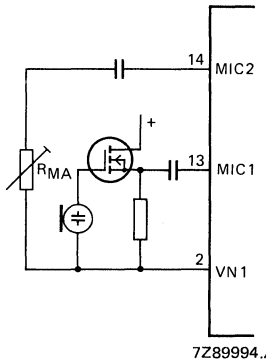


$$\frac{A_M(R_{MS} \neq 0)}{A_M(R_{MS} = 0)} = \frac{4}{4 + R_{MS}} \quad (R_{MS} \text{ in k}\Omega)$$

$$A_M = \left|\frac{V_L}{V_M}\right|.$$

Fig. 4 Symmetrical microphone connection. Resistor R_{MP} may be used to lower the microphone termination resistance.

The microphone amplifier also has an excellent behaviour for connection of an electret microphone with built in FET-source follower. In this condition pin 14 is decoupled for a.c. and the amplifier is driven at pin 13. The input impedance in this asymmetrical mode is 22 kΩ. If attenuation of the amplification is required the value of R_{MA} is given by:



$$\frac{A_M(R_{MA} \neq 0)}{A_M(R_{MA} = 0)} = \frac{22 + R_{MA}}{22 + 11\,R_{MA}} \qquad (R_{MA} \text{ in k}\Omega)$$

$$A_M = \left| \frac{V_L}{V_{MIC1}} \right|$$

Fig. 5 Electret microphone circuit.

Receiver amplifier and anti-sidetone network (Fig. 14)

This amplifier is a non-inverting, fixed feedback amplifier with a class-A output stage. The gain is fixed and measures 20 dB from pin 4 (IR) to pin 5 (QR). The output is intended to drive dynamic capsules of nom. 220 Ω. For capsule impedances (Z_T) less than 220 Ω the maximum output voltage swing is determined by Z_T and the bias current of 3,9 mA. For Z_T greater than 220 Ω the maximum voltage swing is determined and soft-limited internally. The received line signal is attenuated by the anti-sidetone network and can be adjusted using R_{AT}. The amplification from the line to the telephone output is given by:

$$A_T = 10\,\frac{R_{AT}}{R_{AT} + Z_S} \times \frac{Z_T}{Z_T + R_O}$$

Z_S is the impedance of the anti-sidetone network
Z_T is the capsule impedance
R_O is the amplifier output resistance

Optimum side-tone suppression is obtained as Z_S (R_{A1}, R_{A2} and C_A) equals

$$Z_S = K\,\frac{Z_L \times R_i}{Z_L + R_i}$$

Z_L = line terminating impedance
R_i = output stage impedance / / passive circuit impedance
K = 200

In the application of Fig. 14 the network is optimized for 2 km of twisted copper wire (ϕ 0,5 mm) cable with a d.c. resistance of 176 Ω/km. The side-tone suppression in the range from 0 to 10 km is at least 10 dB compared with the case when no compensation is applied.

Keyboard inputs

Inputs for the logic control are compatible with different types of keyboard. Using a keyboard, tone combinations are generated:

- by connecting one of the row inputs to one of the column inputs by means of a single switch of the matrix
- by applying a dual contact keyboard having its common row contact tied to VN1 and the common column contact tied to VR.

Single tones can be generated by connecting the column input to VR or the row input to VN1.

An anti-bounce circuit eliminates switch bounce for up to 2 ms. Two key roll-over is provided by blocking other inputs as soon as one key is pressed.

Microcomputer mode (Figs 6 to 10)

The inputs for keyboard connections can also be used for direct connection to a microcomputer. If the column inputs are interconnected and made HIGH (= VR) the row inputs are changed to another mode, allowing the circuit to be driven by 4-bit data plus an enable signal. In this mode, it is also possible to connect a separate mute enable signal on inputs COL1, 2 and 4 and a tone enable input on COL3.

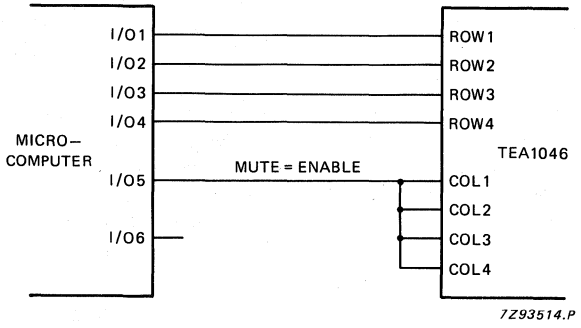


Fig. 6 Microcomputer mode. All column inputs interconnected.

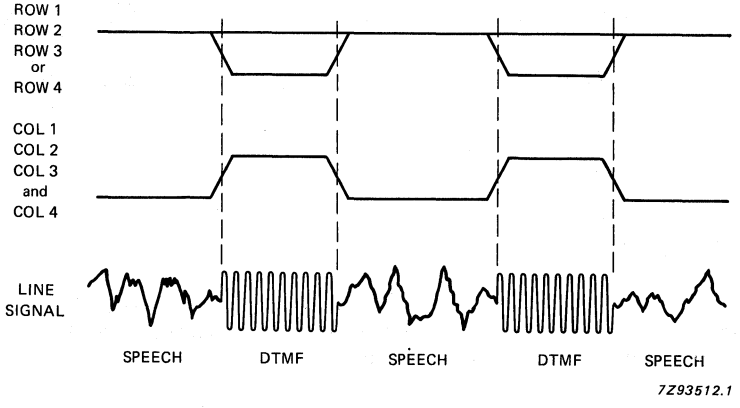


Fig. 7 Tone/speech waveform in circuit diagram Fig. 6.

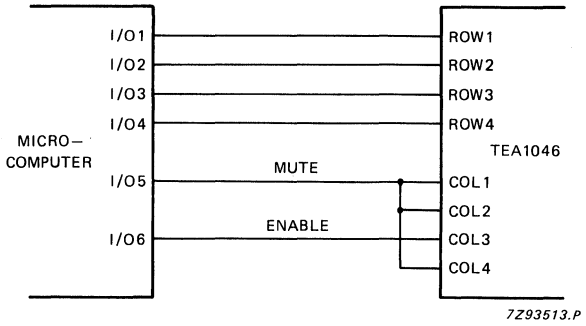


Fig. 8 Microcomputer mode. Column inputs COL1, 2 and 4 interconnected.

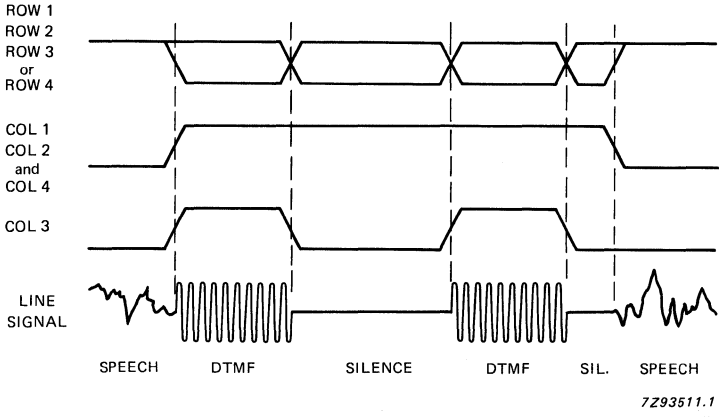


Fig. 9 Tone/speech waveform in circuit diagram Fig. 8.

Truth table microcomputer mode

row				column		tones Hz	symbol	mute
1	2	3	4	1, 2, 4	3			
H	H	H	H	L	L	–	–	off
X	X	X	X	H	L	–	–	on
H	H	H	H	H	H	697/1209	1	on
H	H	H	L	H	H	697/1336	2	on
H	H	L	H	H	H	697/1477	3	on
H	H	L	L	H	H	697/1633	A	on
H	L	H	H	H	H	770/1209	4	on
H	L	H	L	H	H	770/1336	5	on
H	L	L	H	H	H	770/1477	6	on
H	L	L	L	H	H	770/1633	B	on
L	H	H	H	H	H	852/1209	7	on
L	H	H	L	H	H	852/1336	8	on
L	H	L	H	H	H	852/1477	9	on
L	H	L	L	H	H	852/1633	C	on
L	L	H	H	H	H	941/1209	*	on
L	L	H	L	H	H	941/1336	0	on
L	L	L	H	H	H	941/1477	#	on
L	L	L	L	H	H	941/1633	D	on

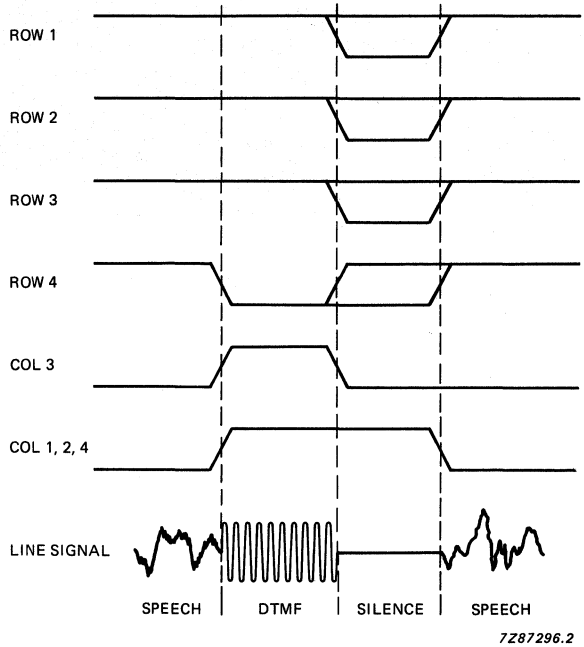


Fig. 10 Waveforms tones 687/1336 Hz (dialling number 2).

Dial tone generator

The crystal oscillator frequency (3,579 545 MHz) is divided by a factor of nine to give the clock frequency. A maximum division error of 0,25% is achieved in the TEA1046; CCITT recommendations are that tones should be within 1,5% of the specified frequencies.

The output from the dividers for the higher and the lower frequency tones are symmetrical square-wave pulses which contain considerable odd-numbered harmonics. The lower order odd numbered harmonics (11th and less) are eliminated by synthesising the tone frequencies as crude stepped sinewave approximations. Each half cycle of the tone waveform comprises seven discrete amplitudes for the lower frequency tones and nine discrete amplitudes for the higher frequency tones. Each amplitude increment is generated by switching on and off an individual current source for the duration of each step of the sinewave. The frequency of the tones is varied by changing the duration of each step. This circuit allows the connecting of two low-pass first order filters to pins 9 and 10 to reduce distortion of the DTMF harmonics.

The second filter is also used for filtering the microphone signal. If lower requirements for the distortion can be applied the filter at pin 10 can be omitted. In that case the filter at pin 9 must have a lower cut-off frequency (1800 Hz) to achieve a correct pre-emphasis since the roll-off of the filters is compensated internally.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply current	I_P	max.	150 mA
Surge current ($t_p < 250\ \mu s$)	I_S	max.	850 mA
Operating ambient temperature range	T_{amb}	−25 to + 70	°C
Storage temperature range	T_{stg}	−55 to + 125	°C
Junction temperature	T_j	max.	125 °C

CHARACTERISTICS

T_{amb} = 25 °C; I_L = 15 mA; f = 1 kHz; unless otherwise specified. See also Fig. 11.

parameter	symbol	min.	typ.	max.	unit
Supply					
Line voltage d.c.					
I_L = 15 mA	V_L	4,3	4,8	5,3	V
I_L = 50 mA	V_L	4,5	5,0	5,5	V
I_L = 120 mA	V_L	5,0	5,4	6,5	V
Temperature coefficient	TC	–	−10	–	mV/K
Line current range	I_L	10	–	120	mA
Stabilized voltage (pin 3)					
I_L = 15 mA	V_S	–	3,5	–	V
I_L = 120 mA	V_S	–	4,0	–	V
Reference voltage (pin 12)	V_R	–	1,0	–	V

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Microphone					
Input resistance (symmetrical)	R_i 13-14	–	4	–	kΩ
Input resistance (asymmetrical)	R_i 13	–	22	–	kΩ
Voltage amplification R_L = 600 Ω	A_M	49	50	51	dB
Temperature coefficient	TC	–	0,01	–	dB/K
Common mode rejection ratio	CMRR	60	–	–	dB
Distortion at V_L = 3 dBm	d_t	–	–	2	%
Noise output voltage Z_L = 600 Ω; psophometrically weighted (P53 curve)	V_{NO}	–	–	–65	dBmp
Amplification reduction during dialling	ΔA_M	70	–	–	dB
Anti-sidetone					
Voltage amplification, microphone to anti-sidetone output (R_{AT} = 3,9 kΩ)	A_{AT}	–	25	–	dB
Transmitter output stage					
Dynamic resistance setting range	R_i	600	–	900	Ω
Variation of output impedance over line current range R_i = 600 Ω	ΔZ_o	–	100	–	Ω
Balance return loss from 300 up to 3400 Hz at 600 Ω (R_{ZI} = 75 Ω, C_L = 10 nF)	BRL	20	–	–	dB
at 900 Ω (R_{ZI} = 120 Ω, C_L = 30 nF)	BRL	20	–	–	dB
Receiver amplifier					
Voltage amplification R_T = 350 Ω	A_T	19	20	21	dB
Amplification variation f = 300 to 3400 Hz	$\Delta A_T/f$	–	0	–	dB
Amplification variation in temperature and current range	$\Delta A_T/T$	–	–	–0,5	dB
Amplification reduction during dialling	ΔA_T	60	–	–	dB
Output voltage swing (d_t = 10%)	$V_{o(p\text{-}p)}$	1300	1600	–	mV
Output impedance	Z_o	–	4	7	Ω
Input impedance	Z_i	–	100	–	kΩ
Output distortion level < –7 dBV	d_o	–	–	2	%
Output noise voltage psophometrically weighted (P53 curve)	$V_{no(rms)}$	–	–	150	μV
Bias current	I_M	–	3,9	–	mA

parameter	symbol	min.	typ.	max.	unit
DTMF generator					
Tone frequencies					
low tones (row inputs)			697, 770, 852, 941		Hz
high tones (column inputs)			1209, 1336, 1477, 1633		Hz
Dividing error					
crystal frequency = 3,58 MHz	Δf_d	−0,25	–	−0,05	%
Tone output level					
$I_L > 10$ mA					
lower tones	V_{LG}	−11	–	−6	dBm
higher tones	V_{HG}	−9	–	−4	dBm
Distortion with respect to total level	d_{tot}	–	−34	−25	dB
Tolerance on output level					
over temp. and current range	ΔV_o	−2	–	2	dB
Pre-emphasis higher tones					
over temp. and current range					
at $C_{F1} = C_{F2} = 10$ nF	ΔV_{HG}	1	2	3	dB
Tone delay					
after key actuation	t_d	–	10	–	μs
Switch delay time speech/mute					
after key release	t_d	–	10	–	μs
Switch bounce elimination	t_{sb}	–	2	–	ms
Keyboard inputs					
Contact off resistance	R_{Koff}	250	–	–	kΩ
Contact on resistance	R_{Kon}	–	–	10	kΩ
Lower frequency inputs (ROW1, 2, 3, 4)					
voltage LOW	V_{IL}	–	–	1,1	V
voltage HIGH	V_{IH}	1,5	–	–	V
current LOW	I_{IL}	–	20	–	μA
current HIGH (maximum allowable = 1 mA)	I_{IH}	0	–	–	μA
Higher frequency inputs (COL1, 2, 3, 4)					
voltage LOW	V_{IL}	–	–	0,5	V
voltage HIGH	V_{IH}	0,9	–	–	V
current LOW	I_{IL}	0	–	–	μA
current HIGH (maximum allowable = 1 mA)	I_{IH}	–	20	–	μA

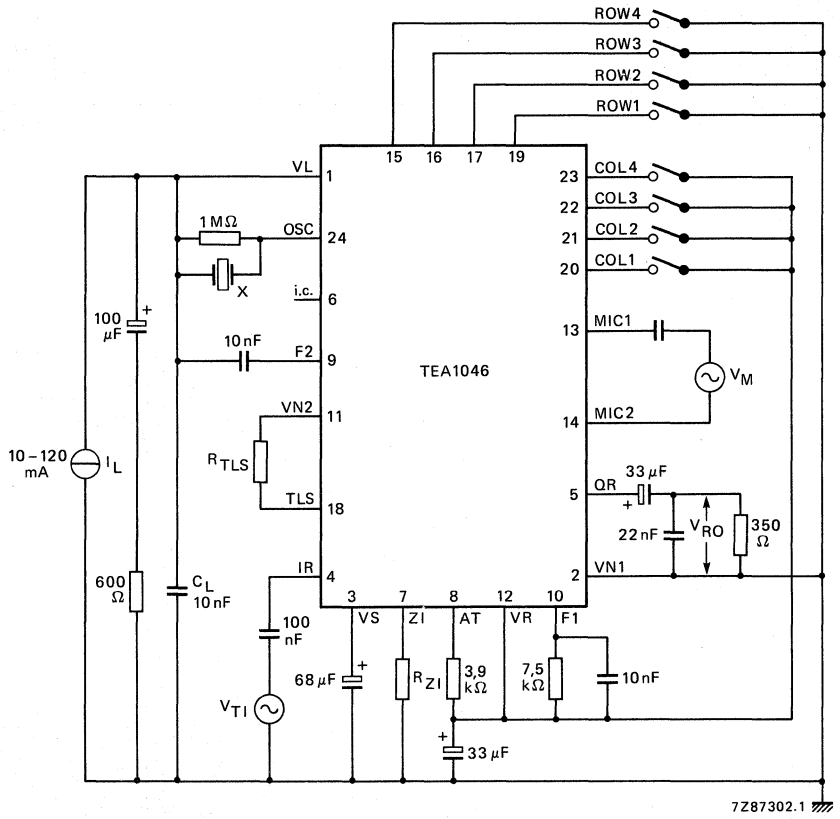


Fig. 11 Test circuit for measuring amplifier voltage gains and frequencies and levels of DTMF generator.
X = 3,58 MHz.

$$A_M = \left|\frac{V_L}{V_M}\right| \quad (V_{TI} = 0) \qquad A_T = \left|\frac{V_{RO}}{V_{IR}}\right| \quad (V_M = 0) \qquad A_{AT} = \left|\frac{V_{AT}}{V_M}\right| \quad (V_{TI} = 0)$$

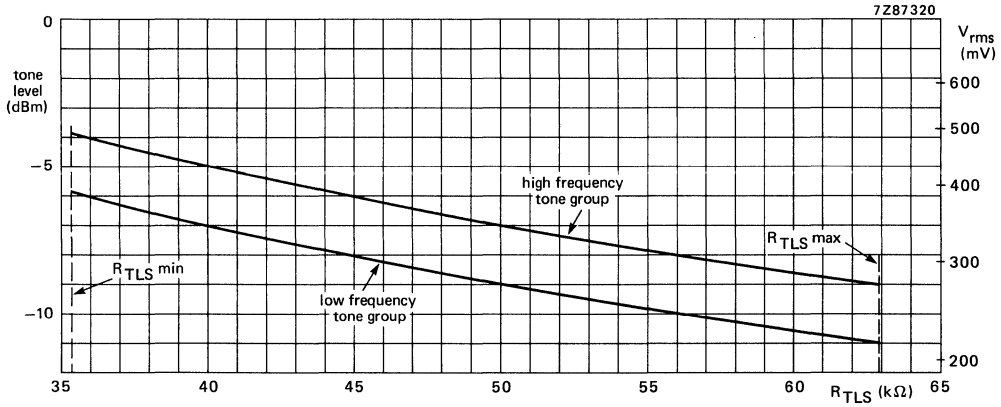


Fig. 12 DTMF level selection. The curve is valid for a dynamic impedance of 600 Ω (R_{ZI} = 75 Ω).

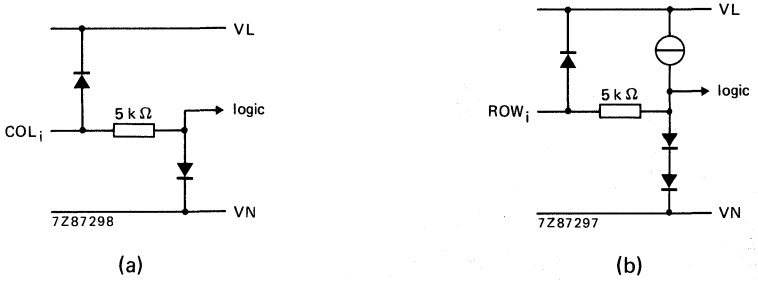


Fig. 13 Equivalent configuration of inputs: (a) COL1, 2, 3 and 4; (b) ROW1, 2, 3 and 4.

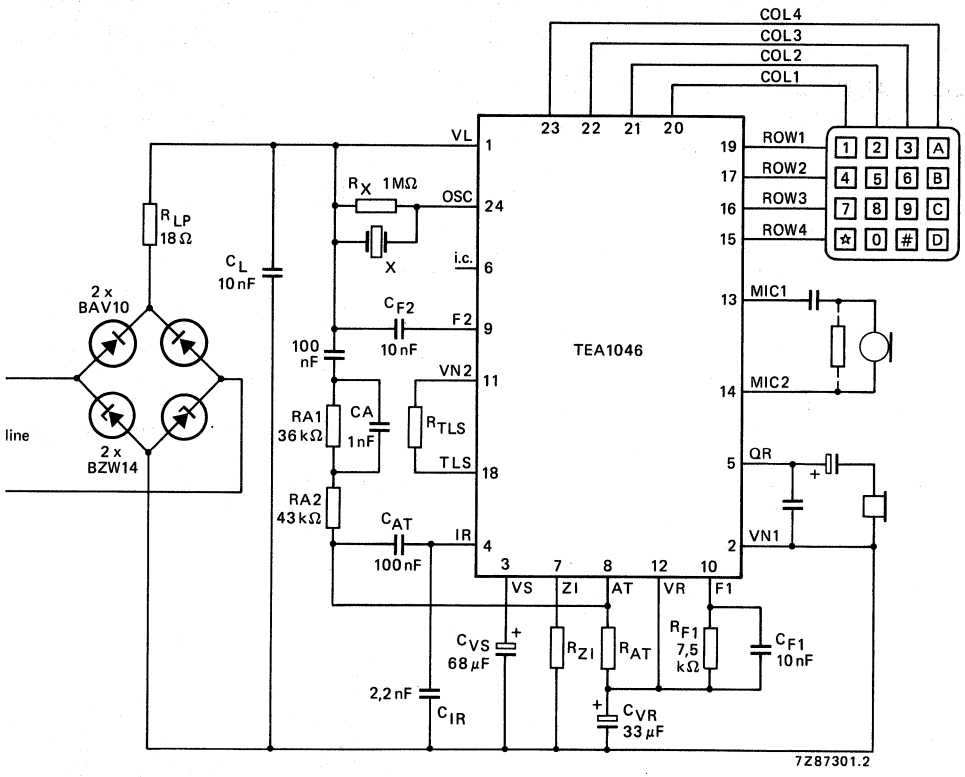


Fig. 14 Application diagram TEA1046 using dynamic transducers, R_{MS}, R_{AT}, R_{ZI} and R_{TLS} determined by transducers and system requirements.

VERSATILE TELEPHONE TRANSMISSION CIRCUITS WITH DIALLER INTERFACE

GENERAL DESCRIPTION

The TEA1060 and TEA1061 are bipolar integrated circuits performing all speech, and line interface functions required in fully electronic telephone sets. The circuits internally perform electronic switching between dialling and speech.

Features

- Voltage regulator with adjustable static resistance
- Provides supply for external circuitry
- Symmetrical low-impedance inputs for dynamic and magnetic microphones (TEA1060)
- Symmetrical high-impedance inputs for piezoelectric microphone (TEA1061)
- Asymmetrical high-impedance input for electret microphone (TEA1061)
- DTMF signal input with confidence tone
- Mute input for pulse or DTMF dialling
- Power down input for pulse dial or register recall
- Receiving amplifier for magnetic, dynamic or piezoelectric earpieces
- Large amplification setting range on microphone and earpiece amplifiers
- Line loss compensation facility, line current dependent (microphone and earpiece amplifiers)
- Gain control adaptable to exchange supply
- Possibility of DC line voltage adjustment

QUICK REFERENCE DATA

Line voltage at I_{line} = 15 mA	V_{LN}	typ. 4,45	V
Line current operating range (pin 1)	I_{line}	10 to 140	mA
Internal supply current			
power down input LOW	I_{CC}	typ. 1	mA
power down input HIGH	I_{CC}	typ. 55	μA
Supply current for peripherals at I_{line} = 15 mA, mute input HIGH			
$V_{CC} > 2,2$ V	I_P	max. 2,5	mA
$V_{CC} > 3,0$ V	I_P	max. 1,2	mA
Voltage amplification range			
microphone amplifier			
TEA1060	A_{vd}	44 to 60	dB
TEA1061	A_{vd}	30 to 46	dB
receiving amplifier	A_{vd}	17 to 39	dB
Line loss compensation			
Amplification control range	ΔA_{vd}	typ. 6	dB
Exchange supply voltage range	V_{exch}	24 to 60	V
Exchange feeding bridge resistance range	R_{exch}	400 to 1000	Ω
Operating ambient temperature range	T_{amb}	−25 to + 75	°C

PACKAGE OUTLINE

18-lead DIL; plastic (SOT-102HE).

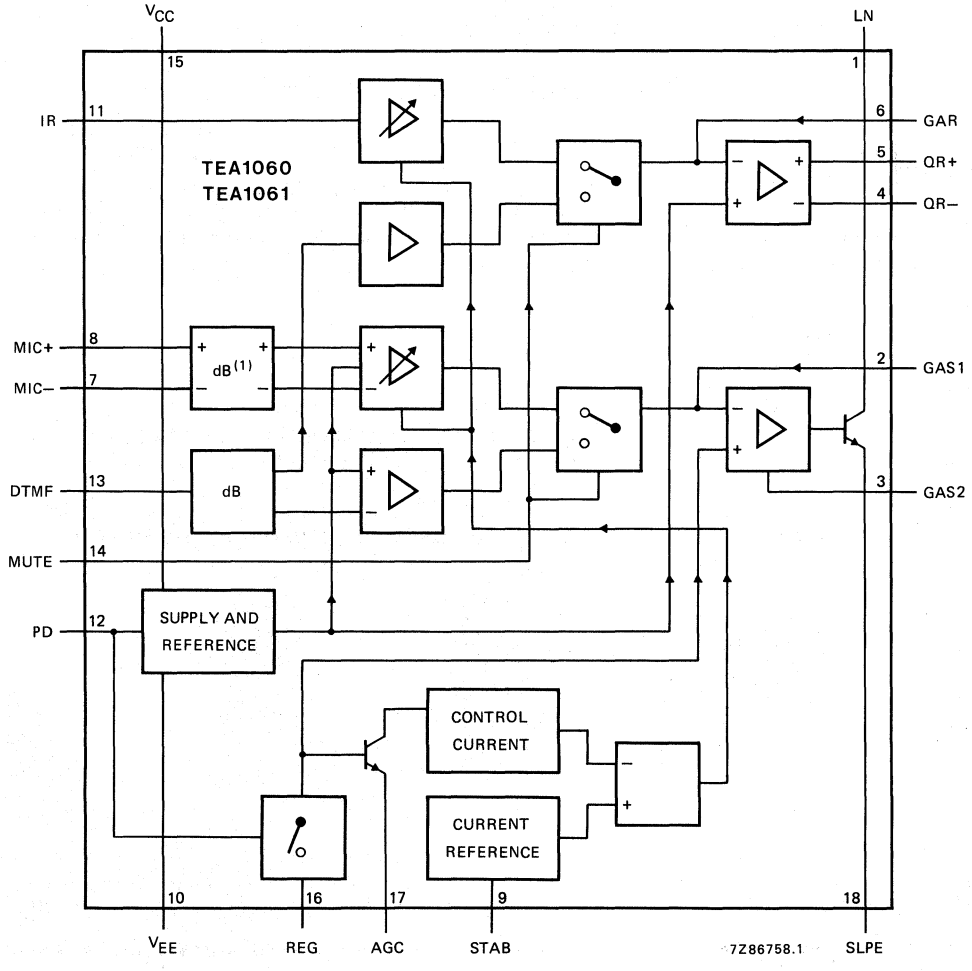


Fig. 1 Block diagram.

The blocks marked "dB" are attenuators. The block marked (1) is only present in the TEA1061.

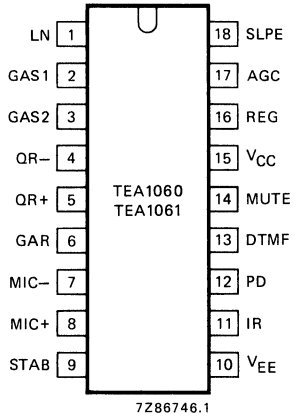


Fig. 2 Pinning diagram.

PINNING

1	LN	positive line connection
2	GAS1	gain adjustment connection, sending amplifier
3	GAS2	gain adjustment connection, sending amplifier
4	QR–	inverting output, receiving amplifier
5	QR+	non-inverting output, receiving amplifier
6	GAR	gain adjustment connection, receiving amplifier
7	MIC–	non-inverting microphone input
8	MIC+	inverting microphone input
9	STAB	current stabilizer connection
10	V_{EE}	negative line connection
11	IR	receiving amplifier input
12	PD	power-down input
13	DTMF	dual-tone multi-frequency input
14	MUTE	mute input
15	V_{CC}	positive supply decoupling connection
16	REG	voltage regulator decoupling connection
17	AGC	automatic gain control input
18	SLPE	slope (d.c. resistance) adjustment connection

FUNCTIONAL DESCRIPTION

Supply: V_{CC}, LN, SLPE, REG and STAB

The circuit and its peripheral circuits usually are supplied from the telephone line. The circuit develops its own supply voltage at V_{CC} and regulates its voltage drop. The supply voltage V_{CC} may also be used to supply external peripheral circuits, e.g. dialling and control circuits.

The supply has to be decoupled by connecting a smoothing capacitor between V_{CC} and V_{EE}; the internal voltage regulator has to be decoupled by a capacitor from REG to V_{EE}. An internal current stabilizer is set by a resistor of 3,6 kΩ between STAB and V_{EE}.

The d.c. current flowing into the set is determined by the exchange supply voltage (V_{exch}), the feeding bridge resistance (R_{exch}), the d.c. resistance of the subscriber line (R_{line}) and the d.c. voltage on the subscriber set (see Fig. 3).

If the line current (I_{line}) exceeds the current I_{CC} + 0,5 mA required by the circuit itself (I_{CC} ca. 1 mA), plus the current I_P required by the peripheral circuits connected to V_{CC}, then the voltage regulator diverts the excess current via LN.

The voltage regulator adjusts the average voltage on LN to:

$$V_{LN} = V_{ref} + I_{SLPE} \times R9 = V_{ref} + (I_{line} - I_{CC} - 0{,}5 \times 10^{-3} - I_P) \times R9.$$

V_{ref} being an internally generated temperature compensated reference voltage of 4,2 V and R9 being an external resistor connected between SLPE and V_{EE}. The preferred value of R9 is 20 Ω. Changing R9 will have influence on microphone gain, DTMF gain, gain control characteristics, side tone and maximum output swing on LN.
Under normal conditions $I_{SLPE} \geqslant I_{CC}$ + 0,5 mA + I_P. The static behaviour of the circuit then equals a 4,2 V voltage regulator diode with an internal resistance R9. In the audio frequency range the dynamic impedance equals R1. The internal reference voltage can be adjusted by means of an external resistor R_{VA}.

FUNCTIONAL DESCRIPTION (continued)

Supply: V_{CC}, LN, SLPE, REG and STAB (continued)

This resistor connected between pins 1 and 16 (LN and REG) will decrease the internal reference voltage. R_{VA} connected between pins 16 and 18 (REG and SLPE) will increase the internal reference voltage.

The current I_P available from V_{CC} for supplying peripheral circuits depends on external components and on the line current. Fig. 4 shows this current for $V_{CC} > 2{,}2$ V and for $V_{CC} > 3$ V. Of which 3 V is the minimum supply voltage for most CMOS circuits including a diode voltage drop for an enable diode. If MUTE is LOW the available current is further reduced when the receiving amplifier is driven.

Microphone inputs MIC+ and MIC− and gain adjustment connections GAS1 and GAS2

The TEA1060 and TEA1061 have symmetrical microphone inputs.
The TEA1060 is intended for low-sensitivity low-impedance dynamic or magnetic microphones. Its input impedance is 8,2 kΩ (2 x 4,1 kΩ and its voltage amplification is typ. 52 dB.
The TEA1061 is intended for a piezoelectric microphone or an electret microphone with built-in FET source follower. Its input impedance is 40,8 kΩ (2 x 20,4 kΩ) and its voltage amplification is typ. 38 dB. The arrangements with the microphone types mentioned are shown in Fig. 5.

The amplification of the microphone amplifier in both types can be adjusted over a range of + and −8 dB to suit the sensitivity of the transducer used. The amplification is proportional to external resistor R7 connected between GAS1 and GAS2.

An external capacitor C6 of 100 pF between GAS1 and SLPE is required to ensure stability. A larger value may be chosen to obtain a first-order low-pass filter. The cut-off frequency corresponds with the time constant R7 x C6.

Mute input MUTE

A HIGH level at MUTE enables the DTMF input and inhibits the microphone inputs and the receiving amplifier, a LOW level or an open circuit does the reverse. Switching the mute input will cause negligible clicks at the telephone outputs and on the line.

Dual-tone multi-frequency input DTMF

When the DTMF input is enabled, dialling tones may be sent onto the line. The voltage amplification from DTMF to LN is typ. 25,5 dB and varies with R7 in the same way as the amplification of the microphone amplifier. The signalling tones can be heard in the earpiece at a low level (confidence tone).

Receiving amplifier: IR, QR+, QR− and GAR

The receiving amplifier has one input IR and two complementary outputs, a non-inverting output QR+ and an inverting output QR−. These outputs may be used for single-ended or for differential drive, depending on the sensitivity and type of earpiece used (see Fig. 6). Amplification from IR to QR+ is typ. 25 dB. This will be sufficient for low-impedance magnetic or dynamic earpieces; these are suited for single-ended drive. By using both outputs (differential drive) the amplification is increased by 6 dB and differential drive becomes possible. This feature can be used in case the earpiece impedance exceeds 450 Ω (high-impedance dynamic, magnetic or piezoelectric earpieces).

The output voltage of the receiving amplifier is specified for continuous-wave drive. The maximum output voltage will be higher under speech conditions, where the ratio of peak and r.m.s. value is higher.

The amplification of the receiving amplifier can be adjusted over a range of + and −8 dB to suit the sensitivity of the transducer used. The amplification is proportional to external resistor R4 connected from GAR to QR+.

Two external capacitors C4 = 100 pF and C7 = 10 x C4 = 1 nF are necessary to ensure stability. A larger value of C4 may be chosen to obtain a first-order low-pass filter. The "cut-off" frequency corresponds with the time constant R4 x C4.

Automatic gain control input AGC

Automatic line loss compensation will be obtained by connecting a resistor R6 from AGC to V_{EE}. This automatic gain control varies the amplification of the microphone amplifier and the receiving amplifier in accordance with the d.c. line current. The control range is 6 dB. This corresponds with a line length of 5 km for a 0,5 mm diameter copper twisted-pair cable with a d.c. resistance of 176 Ω/km and an average attenuation of 1,2 dB/km.

Resistor R6 should be chosen in accordance with the exchange supply voltage and its feeding bridge resistance (see Fig. 7 and Table 1). Different values of R6 give the same ratio of line currents for begin and end of the control range.

If automatic line loss compensation is not required AGC may be left open. The amplifiers then all give their maximum amplification as specified.

Power-down input PD

During pulse dialling or register recall (timed loop break) the telephone line is interrupted, as a consequence it provides no supply for the transmission circuit and the peripherals connected to V_{CC}. These gaps have to be bridged by the charge in the smoothing capacitor C1. The requirements on this capacitor are relaxed by applying a HIGH level to the PD input during the time of the loop break, which reduces the supply current from typ. 1 mA to typ. 55 μA.

A HIGH level at PD further disconnects the capacitor at REG, with the effect that the voltage stabilizer will have no switch-on delay after line interruptions. This results in no contribution of the IC to the current waveform during pulse dialling or register recall.

When this facility is not required PD may be left open.

Side-tone suppression

Suppression of the transmitted signal in the earpiece is obtained by the anti-side-tone network consisting of $R1//Z_{line}$, R2, R3, R8 and Z_{bal} (see Fig. 10). Maximum compensation is obtained when the following conditions are fulfilled:

a) $R9.R2 = R1(R3 + [R8//Z_{bal}])$

b) $[Z_{bal}/(Z_{bal} + R8)] = [Z_{line}/(Z_{line} + R1)]$

If fixed values are chosen for R1, R2, R3 and R9, then condition a) will always be fulfilled provided that $|R8//Z_{bal}| \ll R3$.

To obtain optimum side-tone-suppression, condition b) has to be fulfilled resulting in:

$$Z_{bal} = (R8/R1)Z_{line} = k.Z_{line}$$

where k is a scale factor; $k = (R8/R1)$

Scale factor k (value of R8) must be chosen to meet the following criteria:

- compatibility with a standard capacitor from the E6 or E12 range for Z_{bal}
- $|Z_{bal}//R8| \ll R3$
- $|Z_{bal}+R8| \gg R9$

In practice Z_{line} varies strongly with line length and cable type; consequently an average value has to be chosen for Z_{bal}. The suppression further depends on the accuracy with which Z_{bal} equals the average line impedance.

FUNCTIONAL DESCRIPTION (continued)

Side-tone suppression (continued)

The anti-side-tone network as used in the standard application (Fig. 10) attenuates the signal from the line with 32 dB. The attenuation is nearly flat over the audio-frequency range.
Instead of the above described special bridge, the conventional Wheatstone bridge configuration can be used as an alternative anti-side tone circuit. Both bridges can be used with either a resistive set impedance or with a complex set impedance.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Positive line voltage (d.c.)	V_{LN}	max.	12	V
Repetitive line voltage during switch-on or line interruption	V_{LN}	max.	13,2	V
Repetitive peak line voltage t_p/P = 1 ms/5 s; R_{10} = 13 Ω; R_9 = 20 Ω (see Fig. 10)	$V_{LN(RM)}$	max.	28	V
→ Line current	I_{line}	max.	140	mA
Voltage on all other pins	V_i	max.	V_{CC} + 0,7	V
	$-V_i$	max.	0,7	V
Total power dissipation	P_{tot}	max.	640	mW
Storage temperature range	T_{stg}		−40 to + 125	°C
Operating ambient temperature range	T_{amb}		−25 to + 75	°C

CHARACTERISTICS

I_{line} = 10 to 140 mA; V_{EE} = 0 V; f = 800 Hz; T_{amb} = 25 °C, R9 = 20 Ω; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply: LN and V_{CC} (pins 1 and 15)					
Voltage drop over circuit					
at I_{line} = 5 mA	V_{LN}	3,95	4,25	4,55	V
at I_{line} = 15 mA	V_{LN}	4,25	4,45	4,65	V
at I_{line} = 100 mA	V_{LN}	5,40	6,10	7	V
at I_{line} = 140 mA	V_{LN}	–	–	8	V
Variation with temperature					
at I_{line} = 15 mA	$\Delta V_{LN}/\Delta T$	−4	−2	0	mV/K
Voltage drop over circuit					
at I_{line} = 15 mA					
$R_{VA} = R_{1\text{-}16}$ = 68 kΩ	V_{LN}	3,50	3,80	4,05	V
$R_{VA} = R_{16\text{-}18}$ = 39 kΩ	V_{LN}	4,70	5,0	5,30	V
Supply current					
PD = LOW; V_{CC} = 2,8 V	I_{CC}	–	0,96	1,30	mA
PD = HIGH; V_{CC} = 2,8 V	I_{CC}	–	55	82	μA
Microphone inputs MIC+ and MIC (pins 7 and 8)					
Input impedance					
TEA1060	$\lvert z_{is} \rvert$	3,3	4,1	4,9	kΩ
TEA1061	$\lvert z_{is} \rvert$	16,5	20,4	24,3	kΩ
Common-mode rejection ratio; TEA1060	k_{CMR}	–	82	–	dB
Voltage amplification					
I_{line} = 15 mA; R7 = 68 kΩ					
TEA1060	A_{vd}	51	52	53	dB
TEA1061	A_{vd}	37	38	39	dB
Variation with frequency					
at f = 300 to 3400 Hz	$\Delta A_{vd}/\Delta f$	−0,5	± 0,2	+ 0,5	dB
Variation with temperature at					
I_{line} = 50 mA; T_{amb} = −25 to + 75 °C	$\Delta A_{vd}/\Delta T$	–	± 0,2	–	dB
Dual-tone multi-frequency input DTMF (pin 13)					
Input impedance	$\lvert z_{is} \rvert$	16,8	20,7	24,6	kΩ
Voltage amplification					
I_{line} = 15 mA; R7 = 68 kΩ	A_{vd}	24,5	25,5	26,5	dB
Variation with frequency					
f = 300 to 3400 Hz	$\Delta A_{vd}/\Delta f$	−0,5	± 0,2	+ 0,5	dB
Variation with temperature at					
I_{line} = 50 mA; T_{amb} = −25 to + 75 °C	$\Delta A_{vd}/\Delta T$	–	± 0,2	–	dB
Gain adjustment GAS1 and GAS2 (pins 2 and 3)					
Amplification variation with R7 connected between pins 2 and 3; transmitting amplifier	ΔA_{vd}	−8	–	+ 8	dB

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Transmitting amplifier output LN (pin 1)					
Output voltage at I_{line} = 15 mA;					
d_{tot} = 2%	$V_{LN(rms)}$	1,9	2,3	–	V
d_{tot} = 10%	$V_{LN(rms)}$	–	2,6	–	V
Noise output voltage					
I_{line} = 15 mA; R7 = 68 kΩ; pins 7 and 8 open psophometrically weighted (P53 curve)	$V_{no(rms)}$	–	−70	–	dBmp
Receiving amplifier input IR (pin 11)					
Input impedance	$\|z_{is}\|$	16,5	20,4	24,3	kΩ
Receiving amplifier outputs QR+ and QR− (pins 5 and 4)					
Output impedance; single-ended	$\|z_{os}\|$	–	4	–	Ω
Voltage amplification from pin 11 to pin 4 or 5					
I_{line} = 15 mA; R4 = 100 kΩ;					
single-ended; R_L = 300 Ω	A_{vd}	24	25	26	dB
differential; R_L = 600 Ω	A_{vd}	30	31	32	dB
Variation with frequency					
f = 300 to 3400 Hz	$\Delta A_{vd}/\Delta f$	−0,5	± 0,2	+ 0,5	dB
Variation with temperature					
I_{line} = 50 mA; T_{amb} = −25 to + 75 °C	$\Delta A_{vd}/\Delta T$	–	± 0,2	–	dB
Output voltage at I_p = 0; d_{tot} = 2%;					
sine-wave drive; R4 = 100 kΩ					
single-ended; R_L = 150 Ω	$V_{o(rms)}$	0,3	0,38	–	V
single-ended; R_L = 450 Ω	$V_{o(rms)}$	0,4	0,52	–	V
differential; C_L = 47 nF					
R_{series} = 100 Ω; f = 3400 Hz	$V_{o(rms)}$	0,8	1,0	–	V
Noise output voltage					
I_{line} = 15 mA; R4 = 100 kΩ; pin 11 open psophometrically weighted (P53 curve)					
single-ended; R_L = 300 Ω	$V_{no(rms)}$	–	50	–	μV
differential; R_L = 600 Ω	$V_{no(rms)}$	–	100	–	μV
Gain adjustment GAR (pin 6)					
Amplification variation with R4 between pins 6 and 5; receiving amplifier	ΔA_{vd}	−8	–	+8	dB
MUTE input (pin 14)					
Input voltage					
HIGH	V_{IH}	1,5	–	V_{CC}	V
LOW	V_{IL}	–	–	0,3	V
Input current	I_{MUTE}	–	8	15	μA

parameter	symbol	min.	typ.	max.	unit
Reduction of voltage amplification from MIC+ and MIC− to LN at MUTE = HIGH	$-\Delta A_{vd}$	–	70	–	dB
Voltage amplification from DTMF to QR+ or QR−; MUTE = HIGH; R4 = 100 kΩ; single-ended load R_L = 300 Ω	A_{vd}	−21	−19	−17	dB
Power down input PD (pin 12)					
Input voltage					
HIGH	V_{IH}	1,5	–	V_{CC}	V
LOW	V_{IL}	–	–	0,3	V
Input current	I_{PD}	–	5	10	μA
Automatic gain control input AGC (pin 17)					
Controlling the gain from pin 11 to pins 4-5 and the gain from pins 7-8 to pin 1 R6 = 110 kΩ (connected between pins 17 and 10) amplification control range	$-\Delta A_{vd}$	–	6	–	dB
Highest line current for maximum amplification	I_{line}	–	22	–	mA
Lowest line current for minimum amplification	I_{line}	–	60	–	mA

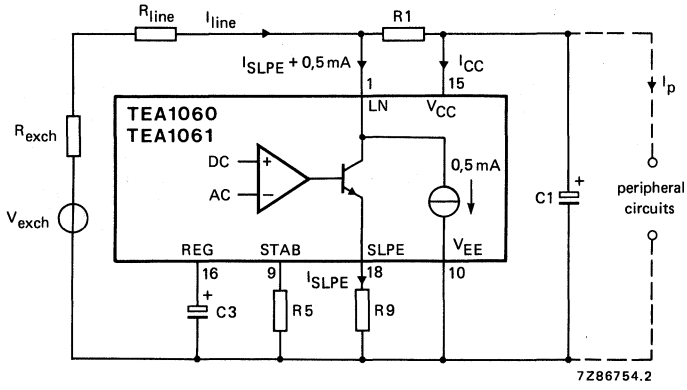
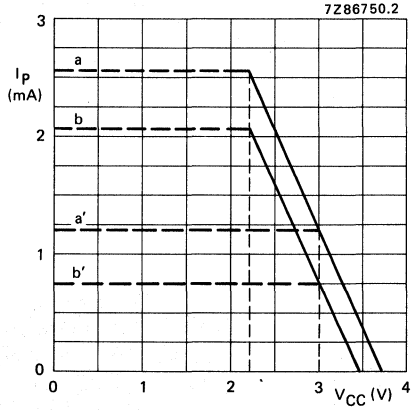


Fig. 3 Supply arrangement.



I_{line} = 15 mA at V_{LN} = 4,45 V
R1 = 620 Ω
R9 = 20 Ω

Fig. 4 Maximum current I_p available from V_{CC} for external (peripheral) circuitry with $V_{CC} > 2{,}2$ V and $V_{CC} > 3$ V. Curves (a) and (a') are valid when the receiving amplifier is not driven or when MUTE = HIGH, curves (b) and (b') are valid when MUTE = LOW and the receiving amplifier is driven, $V_{o(rms)}$ = 150 mV, R_L = 150 Ω (asymmetrical).
a) = 2,55 mA; b) = 2,1 mA; a') = 1,2 mA and b') = 0,75 mA.

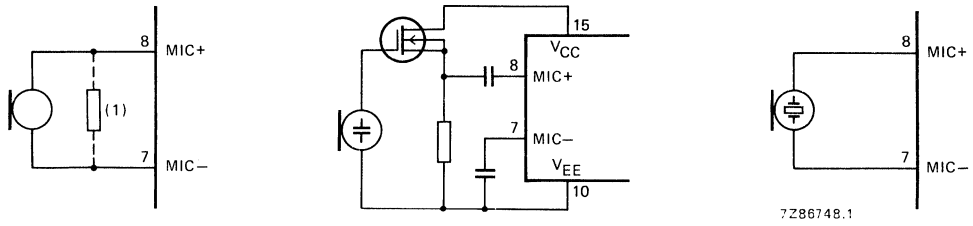


Fig. 5 Alternative microphone arrangements. a) magnetic or dynamic microphone, TEA1060. The resistor marked (1) may be connected to lower the terminating impedance. b) electret microphone, TEA1061. c) piezoelectric microphone, TEA1061.

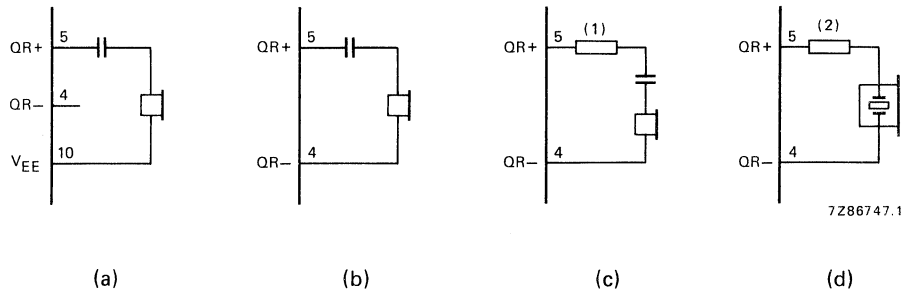


Fig. 6 Alternative receiver arrangements. a) dynamic telephone with less than 450 Ω impedance. b) dynamic telephone with more than 450 Ω impedance. c) magnetic telephone with more than 450 Ω impedance. The resistor marked (1) may be connected to prevent distortion (inductive load) d) piezoelectric telephone. The resistor marked (2) is required to increase the phase margin (capacitive load).

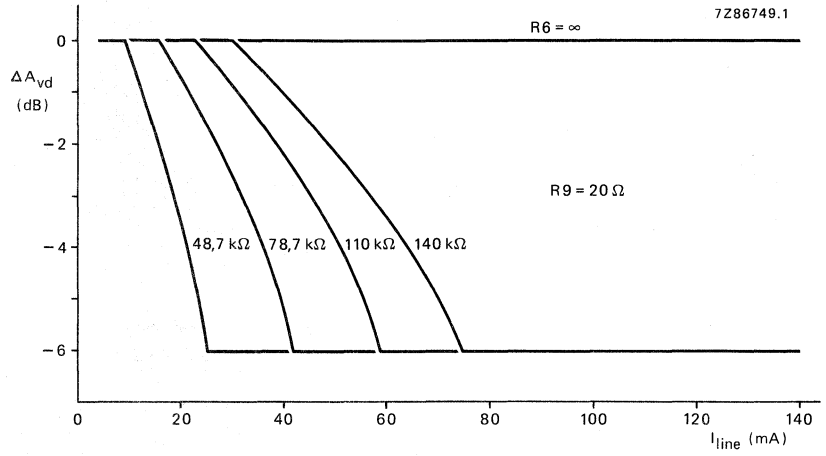


Fig. 7 Variation of amplification with line current, with R6 as a parameter.

		R_{exch} (Ω)			
		400	600	800	1000
		R6 (kΩ)			
V_{exch} (V)	24	61,9	48,7	X	X
	36	100	78,7	68	60,4
	48	140	110	93,1	82
	60	X	X	120	102

Table 1. Values of resistor R6 for optimum line loss compensation, for various usual values of exchange supply voltage V_{exch} and exchange feeding bridge resistance R_{exch}; R9 = 20 Ω.

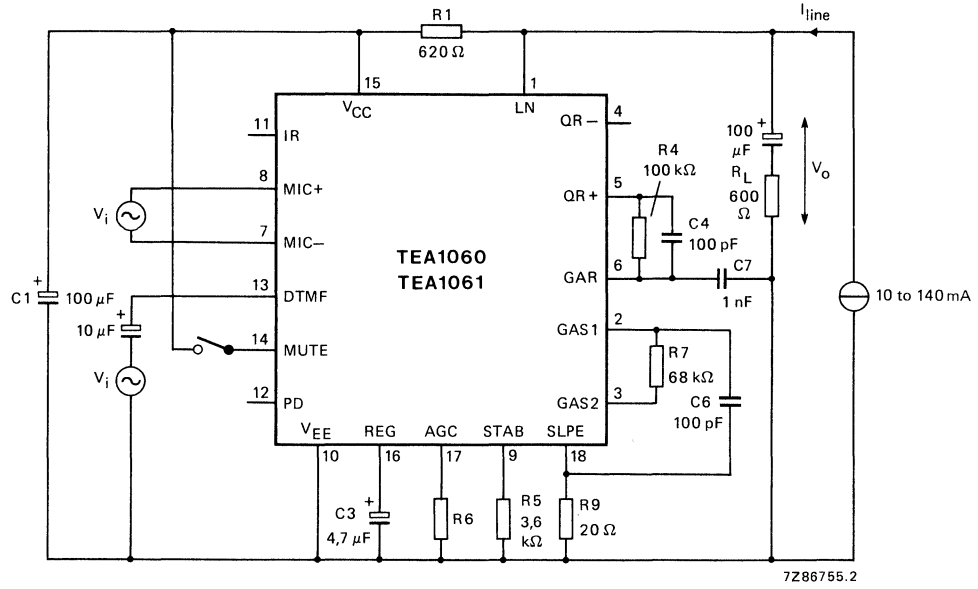


Fig. 8 Test circuit for defining voltage amplification of MIC+, MIC– and DTMF inputs. Voltage amplification is defined as: $A_{vd} = 20 \log |V_o/V_i|$. For measuring the amplification from MIC+ and MIC– the MUTE input should be LOW or open, for measuring the DTMF input MUTE should be HIGH. Inputs not under test should be open.

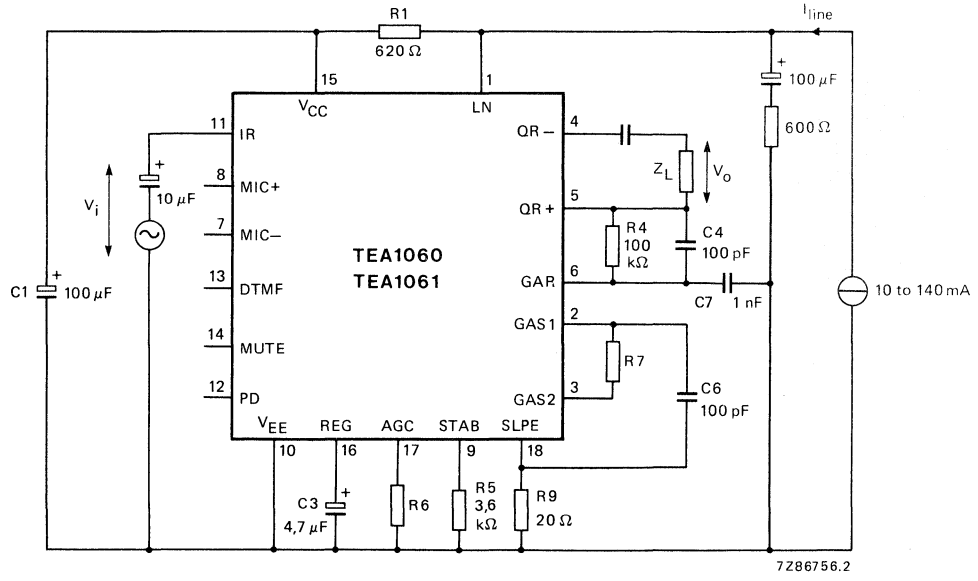


Fig. 9 Test circuit for defining voltage amplification of the receiving amplifier. Voltage amplification is defined as: $A_{vd} = 20 \log |V_o/V_i|$.

APPLICATION INFORMATION

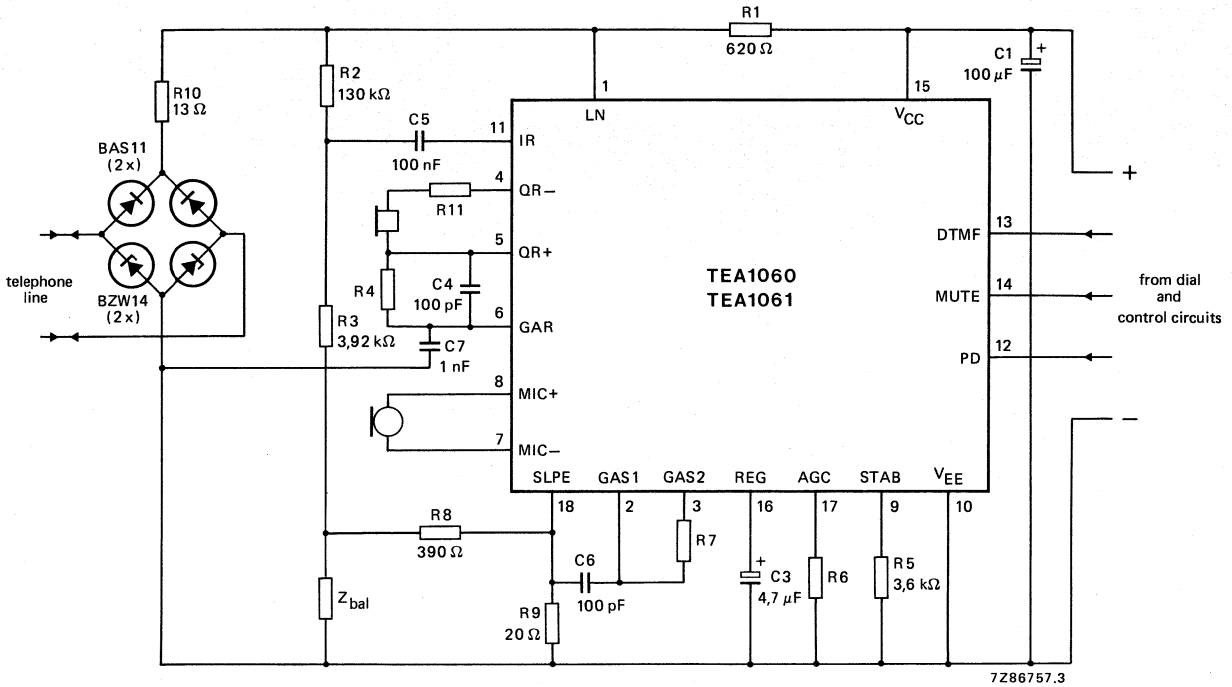


Fig. 10 Typical application of the TEA1060 or TEA1061, shown here with a piezoelectric earpiece and DTMF dialling. The bridge to the left and R10 limit the current into the circuit and the voltage across the circuit during line transients. Pulse dialling or register recall require a different protection arrangement.

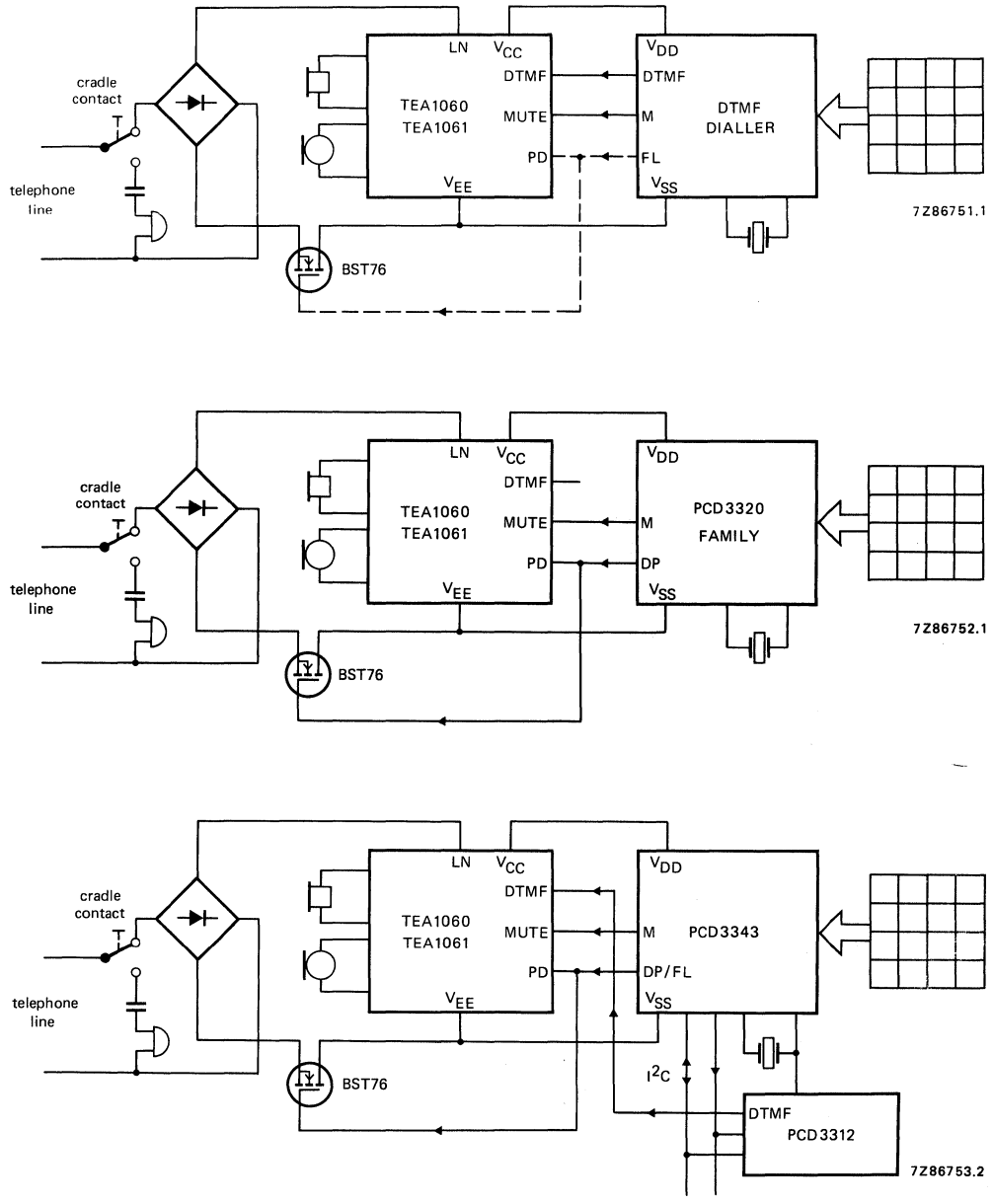


Fig. 11 Typical applications of the TEA1060 or TEA1061 (simplified). a) DTMF set with a CMOS DTMF dialling circuit. The dashed lines show an optional flash (register recall by timed loop break). b) Pulse dial set with the one of the PCD3320 family of CMOS interrupted current-loop dialling circuits. c) Dual-standerd (pulse and DTMF) feature phone with the PCD3343 CMOS telephone controller and the PCD3312 CMOS DTMF generator with I^2C bus.

VERSATILE TELEPHONE TRANSMISSION CIRCUIT WITH DIALLER INTERFACE

GENERAL DESCRIPTION

The TEA1066T is a bipolar integrated circuit performing all speech, and line interface functions required in fully electronic telephone sets. The circuit internally performs electronic switching between dialling and speech.

Features

- Voltage regulator with adjustable static resistance
- Provides supply for external circuitry
- Symmetrical low-impedance inputs for dynamic and magnetic microphones
- Symmetrical high-impedance inputs for piezoelectric microphone
- Asymmetrical high-impedance input for electret microphone
- DTMF signal input with confidence tone
- Mute input for pulse or DTMF dialling
- Power down input for pulse dial or register recall
- Receiving amplifier for magnetic, dynamic or piezoelectric earpieces
- Large amplification setting range on microphone and earpiece amplifiers
- Line loss compensation facility, line current dependent (microphone and earpiece amplifiers)
- Gain control adaptable to exchange supply
- Possibility of d.c. line voltage adjustment

QUICK REFERENCE DATA

Line voltage at I_{line} = 15 mA	V_{LN}	typ. 4,45	V
Line current operating range	I_{line}	10 to 100	mA
Internal supply current			
power down input LOW	I_{CC}	typ. 1	mA
power down input HIGH	I_{CC}	typ. 55	μA
Voltage amplification range microphone amplifier			
low impedance inputs (pins 9 and 7)	A_{vd}	44 to 60	dB
high impedance inputs (pins 10 and 8)	A_{vd}	30 to 46	dB
receiving amplifier	A_{vd}	17 to 39	dB
Supply current for peripherals			
I_{line} = 15 mA; MUTE input HIGH			
$V_{CC} > 2,2$ V	I_p	max. 2,5	mA
$V_{CC} > 3,0$ V	I_p	max. 1,2	mA
Line loss compensation			
Amplification control range	ΔA_{vd}	typ. 6	dB
Exchange supply voltage range	V_{exch}	24 to 60	V
Exchange feeding bridge resistance range	R_{exch}	400 to 1000	Ω
Operating ambient temperature range	T_{amb}	−25 to + 75	°C

PACKAGE OUTLINE

20-lead MINI-PACK; plastic (SO-20; SOT-163A).

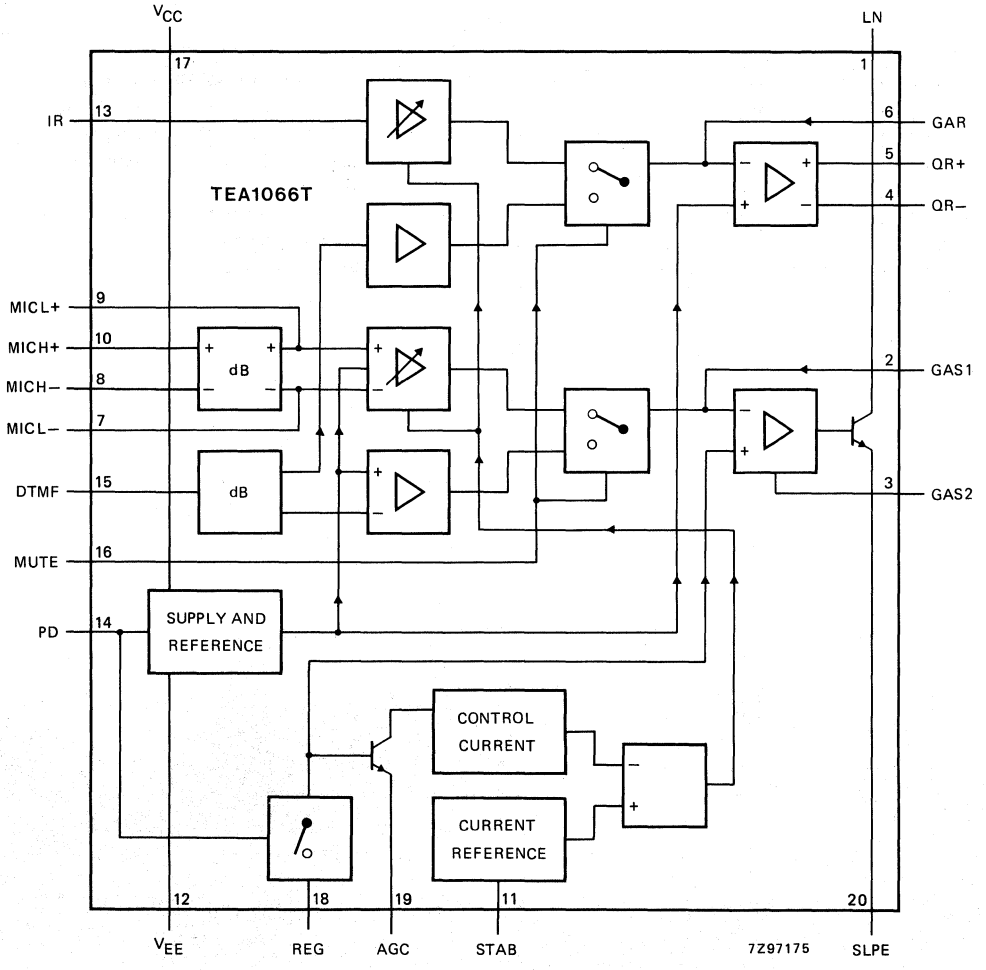


Fig. 1 Block diagram.

The blocks marked "dB" are attenuators.

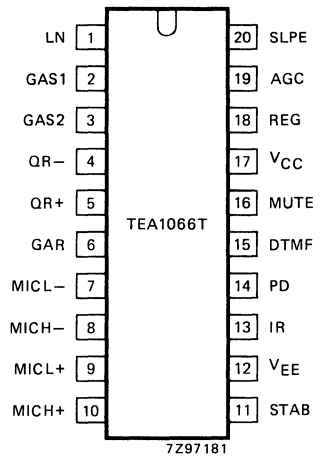


Fig. 2 Pinning diagram.

PINNING

1	LN	positive line terminal
2	GAS1	gain adjustment transmitting amplifier
3	GAS2	gain adjustment transmitting amplifier
4	QR−	inverting output, receiving amplifier
5	QR+	non-inverting output, receiving amplifier
6	GAR	gain adjustment receiving amplifier
7	MICL−	inverting microphone input, low impedance
8	MICH−	inverting microphone input, high impedance
9	MICL+	non-inverting microphone input, low impedance
10	MICH+	non-inverting microphone input, high impedance
11	STAB	current stabilizer
12	V_{EE}	negative line terminal
13	IR	receiving amplifier input
14	PD	power-down input
15	DTMF	dual-tone multi-frequency input
16	MUTE	mute input
17	V_{CC}	positive supply decoupling
18	REG	voltage regulator decoupling
19	AGC	automatic gain control input
20	SLPE	slope (d.c. resistance) adjustment

FUNCTIONAL DESCRIPTION

Supply: V_{CC}, LN, SLPE, REG and STAB

The circuit and its peripheral circuits usually are supplied from the telephone line. The circuit develops its own supply voltage at V_{CC} and regulates its voltage drop. The supply voltage V_{CC} may also be used to supply external peripheral circuits, e.g. dialling and control circuits.

The supply has to be decoupled by connecting a smoothing capacitor between V_{CC} and V_{EE}; the internal voltage regulator has to be decoupled by a capacitor from REG to V_{EE}. An internal current stabilizer is set by a resistor of 3,6 kΩ between STAB and V_{EE}.

The d.c. current flowing into the set is determined by the exchange supply voltage V_{exch}, the feeding bridge resistance R_{exch}, the d.c. resistance of the subscriber line R_{line} and the d.c. voltage on the subscriber set (see Fig. 3).

If the line current I_{line} exceeds the current I_{CC} + 0,5 mA required by the circuit itself, about 1 mA, plus the current I_p required by the peripheral circuits connected to V_{CC}, then the voltage regulator diverts the excess current via LN.

The voltage regulator adjusts the average voltage on LN to:
$V_{LN} = V_{ref} + I_{SLPE} \times R9 = V_{ref} + (I_{line} - I_{CC} - 0{,}5 \times 10^{-3} - I_p) \times R9$. V_{ref} being an internally generated temperature compensated reference voltage of 4,2 V and R9 being an external resistor connected between SLPE and V_{EE}. The preferred value for R9 is 20 Ω. Changing R9 will have influence on microphone gain, gain control characteristics, side tone and maximum output swing on LN.

FUNCTIONAL DESCRIPTION (continued)

Under normal conditions $I_{SLPE} \geqslant I_{CC} + 0{,}5\ mA + I_p$. The static behaviour of the circuit then equals a 4,2 V voltage regulator diode with an internal resistance R9. In the audio frequency range the dynamic impedance equals R1. The internal reference voltage can be adjusted by means of an external resistor R_{VA}. This R_{VA} connected between LN and REG (pins 1 and 16) will decrease the internal reference voltage. R_{VA} connected between REG and SLPE (pins 16 and 18) will increase the internal reference voltage.

The current I_p available from V_{CC} for supplying peripheral circuits depends on external components and on the line current. Fig. 4 shows this current for $V_{CC} > 2{,}2$ V and > 3 V. 3 volt being the minimum supply voltage for most CMOS circuits including a diode voltage drop for an enable diode. If MUTE is LOW the available current is further reduced when the receiving amplifier is driven.

Microphone inputs MICL+, MICH+, MICL− and MICH− and gain adjustment connections GAS1 and GAS2

The TEA1066T has symmetrical microphone inputs. The MICL+ and MICL− inputs are intended for low-sensitivity, low-impedance dynamic or magnetic microphones. Input impedance is 8,2 kΩ (2 x 4,1 kΩ) and its voltage amplification is typ. 52 dB. The MICH+ and MICH− inputs are intended for a piezoelectric microphone or an electret microphone with built-in FET source follower. Its input impedance is 40,8 kΩ (2 x 20,4 kΩ) and its voltage amplification is typical 38 dB.
The arrangements with the microphone types mentioned are shown in Fig. 5.

The amplification of the microphone amplifiers can be adjusted over a range of + and −8 dB to suit the sensitivity of the transducer used. The amplification is proportional to external resistor R7 connected between GAS1 and GAS2.

An external capacitor C6 of 100 pF between GAS1 and SLPE is required to ensure stability. A larger value may be chosen to obtain a first-order low-pass filter. The cut-off frequency corresponds with the time constant R7 x C6.

Mute input MUTE

A HIGH level at MUTE enables the DTMF input and inhibits the microphone inputs and the receiving amplifier; a LOW level or an open circuit does the reverse. Switching the mute input will cause negligible clicks at the telephone outputs and on the line.

Dual-tone multi-frequency input DTMF

When the DTMF input is enabled, dialling tones may be sent onto the line. The voltage amplification from DTMF to LN is typ. 25,5 dB and varies with R7 in the same way as the amplification of the microphone amplifier. The signalling tones can be heard in the earpiece at a low level (confidence tone).

Receiving amplifier: IR, QR+, QR− and GAR

The receiving amplifier has one input IR and two complementary outputs, a non-inverting output QR+ and an inverting output QR−. These outputs may be used for single-ended or for differential drive, depending on the sensitivity and type of earpiece used (see Fig. 6). Amplification from IR to QR+ is typ. 25 dB. This will be sufficient for low-impedance magnetic or dynamic earpieces; these are suited for single-ended drive. By using both outputs (differential drive) the amplification is increased by 6 dB and differential drive becomes possible. This feature can be used in case the earpiece impedance exceeds 450 Ω (high-impedance dynamic, magnetic or piezo-electric earpieces.

The output voltage of the receiving amplifier is specified for continuous-wave drive. The maximum output voltage will be higher under speech conditions, where the ratio of peak and r.m.s. value is higher.

The amplification of the receiving amplifier can be adjusted over a range of + and −8 dB to suit the sensitivity of the transducer used. The amplification is proportional to external resistor R4 connected from GAR to QR+.

Two external capacitors C4 = 100 pF and C6 = 10 x C4 = 1 nF are necessary to ensure stability. A larger value of C4 may be chosen to obtain a first-order, low-pass filter. The "cut-off' frequency corresponds with the time constant R4 x C4.

Automatic gain control input AGC

Automatic line loss compensation will be obtained by connecting a resistor R6 from AGC to V_{EE}. This automatic gain control varies the amplification of the microphone amplifier and the receiving amplifier in accordance with the d.c. line current. The control range is 6 dB. This corresponds with a line length of 5 km for a 0,5 mm diameter copper twisted-pair cable with a d.c. resistance of 176 Ω/km and an average attenuation of 1,2 dB/km.

Resistor R6 should be chosen in accordance with the exchange supply voltage and its feeding bridge resistance (see Fig. 7 and Table 1). Different values of R6 give the same ratio of line currents for begin and end of the control range.

If automatic line loss compensation is not required AGC may be left open. The amplifiers then all give their maximum amplification as specified.

Power-down input PD

During pulse dialling or register recall (timed loop break) the telephone line is interrupted, as a consequence it provides no supply for the transmission circuit and the peripherals connected to V_{CC}. These gaps have to be bridged by the charge in the smoothing capacitor C1. The requirements on this capacitor are relaxed by applying a HIGH level to the PD input during the time of the loop break, which reduces the supply current from typ. 1 mA to typ. 55 μA.

A HIGH level at PD further disconnects the capacitor at REG, with the effect that the voltage stabilizer will have no switch-on delay after line interruptions. This results in no contribution of the IC to the current waveform during pulse dialling or register recall.
When this facility is not required PD may be left open.

Side-tone suppression

Suppression of the transmitted signal in the earpiece is obtained by the anti-side-tone network consisting of $R1//Z_{line}$, R2, R3, R8, R9 and Z_{bal} (see Fig. 10). Maximum compensation is obtained when the following conditions are fulfilled:

a) $R9.R2 = R1(R3 + [R8//Z_{bal}])$

b) $[Z_{bal}/(Z_{bal} + R8)] = [Z_{line}/(Z_{line} + R1)]$

If fixed values are chosen for R1, R2, R3 and R9, then condition a) will always be fulfilled provided that $|R8//Z_{bal}| < R3$.
To obtain optimum side tone suppression, condition b) has to be fulfilled resulting in:

$$Z_{bal} = (R8/R1)\, Z_{line} = k.Z_{line}$$

where k is a scale factor; k = (R8/R1).

Scale factor k (value of R8) must be chosen to meet the following criteria:
- compatibility with a standard capacitor from the E6 or E12 range for Z_{bal}
- $|Z_{bal}//R8| \ll R3$
- $|Z_{bal}+R8| \gg R9$

In practice Z_{line} varies strongly with line length and cable type; consequently an average value has to be chosen for Z_{bal}. The suppression further depends on the accuracy with which Z_{bal}/k equals the average line impedance.

FUNCTIONAL DESCRIPTION (continued)

The anti-side-tone network as used in the standard application (Fig. 10) attenuates the signal from the line with 32 dB. The attenuation is nearly flat over the audio-frequency range.
Instead of the above described special TEA1066 bridge, the conventional Wheatstone bridge configuration can be used as an alternative anti-side-tone circuit. Both bridge types can be used with either a resistive set impedance or with a complex set impedance.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Positive line voltage (d.c.)	V_{LN}	max.	12	V
Repetitive line voltage during switch-on or line interruption	V_{LN}	max.	13,2	V
Repetitive peak line voltage t_p/P = 1 ms/5 s; R_{lim} = 13 Ω; R_{10} = 13 Ω; R_9 = 20 Ω (see Fig. 10)	$V_{LN(RM)}$	max.	28	V
Line current	I_{line}	max.	100	mA
Voltage on all other pins	V_i	max.	V_{CC} + 0,7	V
	$-V_i$	max.	0,7	V
Total power dissipation	P_{tot}	max.	450	mW
Storage temperature range	T_{stg}		−40 to + 125	°C
Operating ambient temperature range	T_{amb}		−25 to + 75	°C

CHARACTERISTICS

$I_{line} = I_1 = 10$ to 100 mA; $V_{EE} = 0$ V; f = 800 Hz; R9 = 20 Ω; $T_{amb} = 25\ ^{o}C$; unless otherwise specified.

parameter	symbol	min.	typ.	max.	unit
Supply: LN and V_{CC} (pins 1 and 17)					
Voltage drop over circuit					
at I_{line} = 5 mA	$V_{1\text{-}12}$	3,95	4,25	4,55	V
at I_{line} = 15 mA	$V_{1\text{-}12}$	4,25	4,45	4,65	V
at I_{line} = 100 mA	$V_{1\text{-}12}$	5,40	6,10	7,00	V
Voltage drop variation with temperature at I_{line} = 15 mA	ΔV_{LN}	−4	−2	0	mV/K
Voltage drop over circuit at I_{line} = 15 mA;					
$R_{VA} = R_{1\text{-}16}$ = 68 kΩ	V_{LN}	3,50	3,80	4,05	V
$R_{VA} = R_{18\text{-}20}$ = 39 kΩ	V_{LN}	4,70	5,0	5,30	V
Supply current (pin 17)					
PD (pin 14) = LOW; V_{CC} = 2,8 V	I_{CC}	–	0,96	1,3	mA
PD (pin 14) = HIGH; V_{CC} = 2,8 V	I_{CC}	–	55	82	μA
Microphone inputs MICL+ and MICL−; MICH+ and MICH−					
Input impedance					
MICL+ (pin 9); MICL− (pin 7)	$\lvert z_{is}\rvert$	3,3	4,1	4,9	kΩ
MICH+ (pin 10); MICH− (pin 8)	$\lvert z_{is}\rvert$	16,5	20,4	24,3	kΩ
Common-mode rejection ratio	k_{CMR}	–	82	–	dB
Voltage amplification at I_{line} = 15 mA; R7 = 68 kΩ					
MICL+; MICL−	A_{vd}	51	52	53	dB
MICH+; MICH−	A_{vd}	37	38	39	dB
Variation with frequency at f = 300 to 3400 Hz	$\Delta A_{vd}/\Delta f$	−0,5	± 0,2	+ 0,5	dB
Variation with temperature at I_{line} = 50 mA; T_{amb} = −25 to + 75 °C	$\Delta A_{vd}/\Delta T$	–	± 0,2	–	dB
Dual-tone multi-frequency input DTMF (pin 15)					
Input impedance	$\lvert z_{is}\rvert$	16,8	20,7	24,6	kΩ
Voltage amplification (pin 15 to pin 1) at I_{line} = 15 mA; R7 = 68 kΩ	A_{vd}	24,5	25,5	26,5	dB
Variation with frequency at f = 300 to 3400 Hz	$\Delta A_{vd}/\Delta f$	−0,5	+ 0,2	+ 0,5	dB
Variation with temperature at I_{line} = 50 mA; T_{amb} = −25 to + 75 °C	$\Delta A_{vd}/\Delta T$	–	± 0,2	–	dB

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Gain adjustment connections GAS1 and GAS2 (pins 2 and 3)					
Amplification variation with R7, transmitting amplifier	ΔA_{vd}	−8	−	+ 8	dB
Transmitting amplifier output LN (pin 1)					
Output voltage at I_{line} = 15 mA;					
d_{tot} = 2%	$V_{LN(rms)}$	1,9	2,3	−	V
d_{tot} = 10 %	$V_{LN(rms)}$	−	2,6	−	V
Noise output voltage at I_{line} = 15 mA; R7 = 68 kΩ; microphone inputs open; psophometrically weighted (P53 curve)	$V_{no(rms)}$	−	−70	−	dBmp
Receiving amplifier input IR (pin 13)					
Input impedance	$\lvert z_{is} \rvert$	16,5	20,4	24,3	kΩ
Receiving amplifier outputs QR+ and QR− (pins 5 and 4)					
Output impedance; single-ended	$\lvert z_{os} \rvert$	−	4	−	Ω
Voltage amplification from pin 13 to pins 4 or 5					
I_{line} = 15 mA; R4 = 100 kΩ;					
single-ended; R_L = 300 Ω	A_{vd}	24	25	26	dB
differential; R_L = 600 Ω	A_{vd}	30	31	32	dB
Amplification variation at f = 300 to 3400 Hz	$\Delta A_{vd}/\Delta f$	−0,5	± 0,2	+ 0,5	dB
Amplification variation I_{line} = 50 mA; T_{amb} = −25 to + 75 °C	$\Delta A_{vd}/\Delta T$	−	± 0,2	−	dB
Output voltage at I_p = 0; d_{tot} = 2%; sine-wave drive; R4 = 100 kΩ					
single-ended; R_L = 150 Ω	$V_{o(rms)}$	0,30	0,38	−	V
single-ended; R_L = 450 Ω	$V_{o(rms)}$	0,4	0,52	−	V
differential; C_L = 47 nF; R_{series} = 100 Ω; f = 3400 Hz	$V_{o(rms)}$	0,8	1,0	−	V
Noise output voltage I_{line} = 15 mA; R4 = 100 kΩ; pin 13 (IR) open psophometrically weighted (P53 curve)					
single-ended R_L = 300 Ω	$V_{no(rms)}$	−	50	−	μV
differential R_L = 600 Ω	$V_{no(rms)}$	−	100	−	μV
Gain adjustment GAR (pin 6)					
Amplification variation with R4 connected between pin 6 and pin 5; receiving amplifier	ΔA_{vd}	−8	−	+ 8	dB

parameter	symbol	min.	typ.	max.	unit
MUTE input (pin 16)					
Input voltage					
HIGH	V_{IH}	1,5	–	V_{CC}	V
LOW	I_{IL}	–	–	0,3	V
Input current	I_{14}	–	5	10	μA
Reduction of voltage amplification from MICL+ (pin 9) and MICL– (pin 7) to LN (pin 1) at MUTE = HIGH	ΔA_{vd}	–	70	–	dB
Voltage amplification from DTMF to QR+ or QR– at MUTE = HIGH; R4 = 100 kΩ single-ended load R_L = 300 Ω	A_{vd}	–21	–19	–17	dB
Power-down input PD (pin 14)					
Input voltage					
HIGH	V_{IH}	1,5	–	V_{CC}	V
LOW	V_{IL}	–	–	0,3	V
Input current	I_{14}	–	5	10	μA
Automatic gain control input AGC (pin 19)					
Amplification control range from pin 13 to pins 4 and 5 from pins 9 and 7 to pin 1 R6 = $R_{19\text{-}12}$ = 110 kΩ					
Amplification control range	$-\Delta A_{vd}$	–	6	–	dB
Highest line current for maximum amplification	I_{line}	–	22	–	mA
Lowest line current for minimum amplification	I_{line}	–	60	–	mA

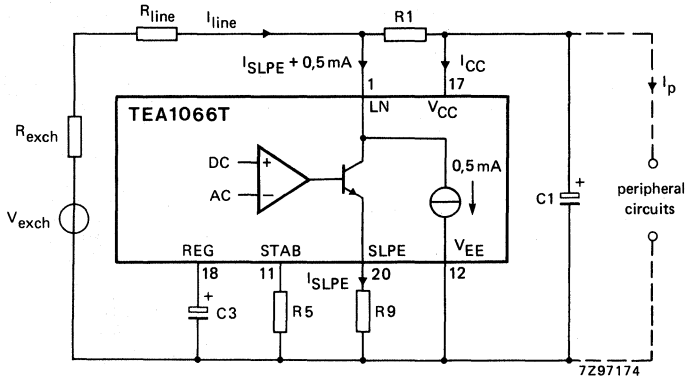


Fig. 3 Supply arrangement.

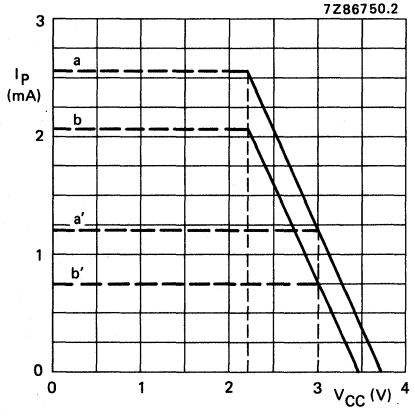


Fig. 4 Maximum current I_p available from V_{CC} for external (peripheral) circuitry with $V_{CC} > 2$ V and $V_{CC} > 3$ V. Curves (a) and (a') are valid when the receiving amplifier is not driven or when MUTE = HIGH, curves (b) and (b') are valid when MUTE = LOW and the receiving amplifier is driven, $V_{o(rms)} = 150$ mV, $R_L = 150\ \Omega$ (asymmetrical).
$I_{line} = 15$ mA; $V_{LN} = 4{,}45$ V; R1 = 620 Ω and R9 = 20 Ω.
(a) = 2,55 mA; (b) = 2,1 mA; (a') = 1,2 mA and (b') = 0,75 mA.

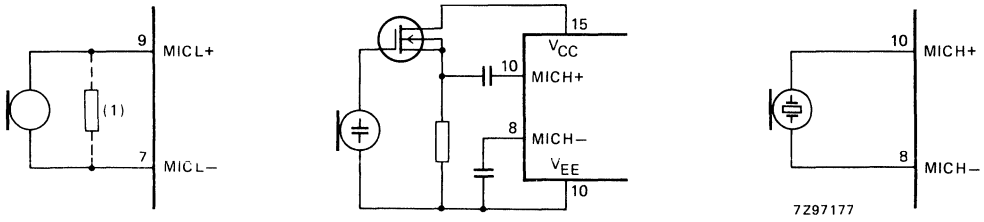


Fig. 5 Alternative microphone arrangements. (a) magnetic or dynamic microphone. The resistor marked (1) may be connected to lower the terminating impedance. (b) electret microphone, (c) piezo-electric microphone.

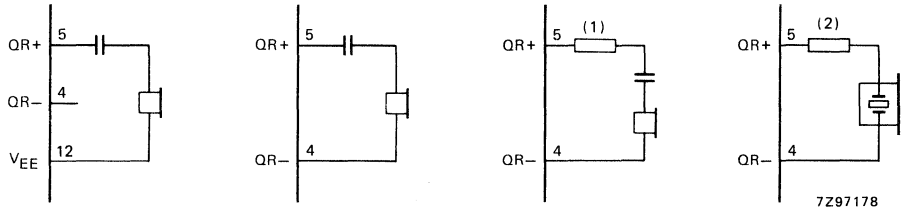


Fig. 6 Alternative receiver arrangements. (a) dynamic telephone with less than 450 Ω impedance. (b) dynamic telephone with more than 450 Ω impedance. (c) magnetic telephone with more than 450 Ω impedance. The resistor marked (1) may be connected to prevent distortion (inductive load). (d) piezoelectric telephone. The resistor marked (2) is required to increase the phase margin (capacitive load).

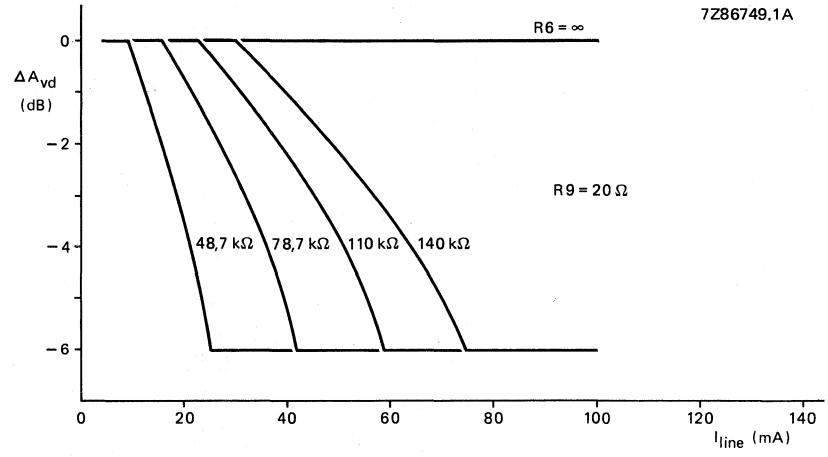


Fig. 7 Variation of amplification with line current, with R6 as a parameter.

		R_{exch} (Ω)			
		400	600	800	1000
		R6 (kΩ)			
V_{exch} (V)	24	61,9	48,7	X	X
	36	100	78,7	68	60,4
	48	140	110	93,1	82
	60	X	X	120	102

Table 1. Values of resistor R6 for optimum line loss compensation, for various usual values of exchange supply voltage V_{exch} and exchange feeding bridge resistance R_{exch}; R9 = 20 Ω.

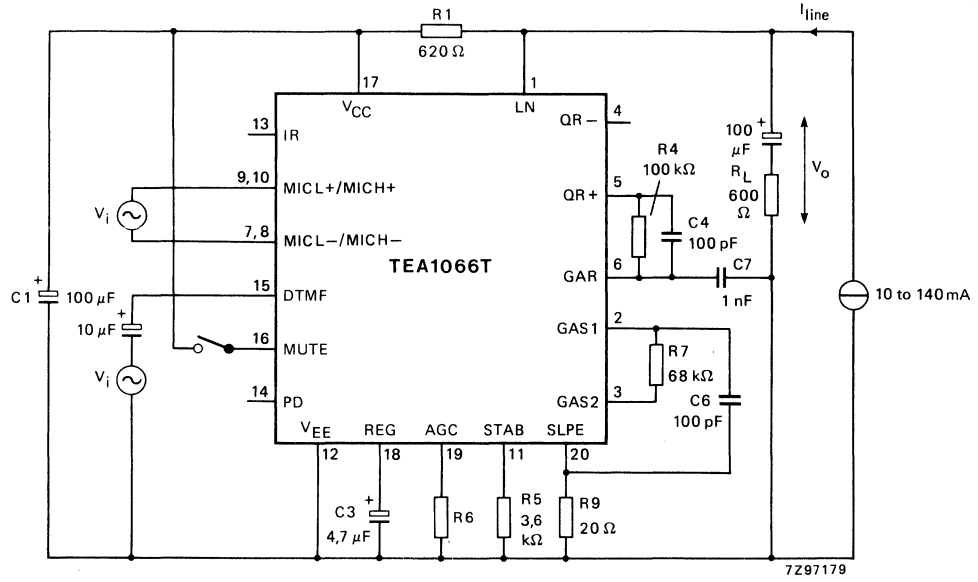


Fig. 8 Test circuit for defining voltage amplification of MICL+, MICL−, MICH+, MICH− and DTMF inputs. Voltage amplification is defined as: $A_{vd} = 20 \log |V_o/V_i|$. For measuring the amplification from MICL+; MICL− or MICH+ and MICH− the MUTE input should be LOW or open, for measuring the DTMF input MUTE should be HIGH. Inputs not under test should be open.

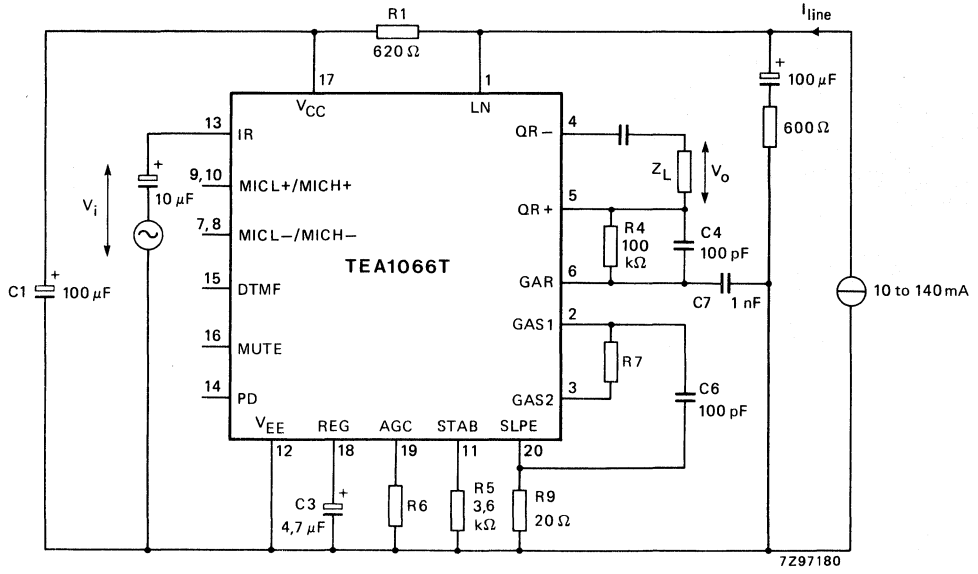


Fig. 9 Test circuit for defining voltage amplification of the receiving amplifier. Voltage amplification is defined as: $A_{vd} = 20 \log |V_o/V_i|$.

APPLICATION INFORMATION

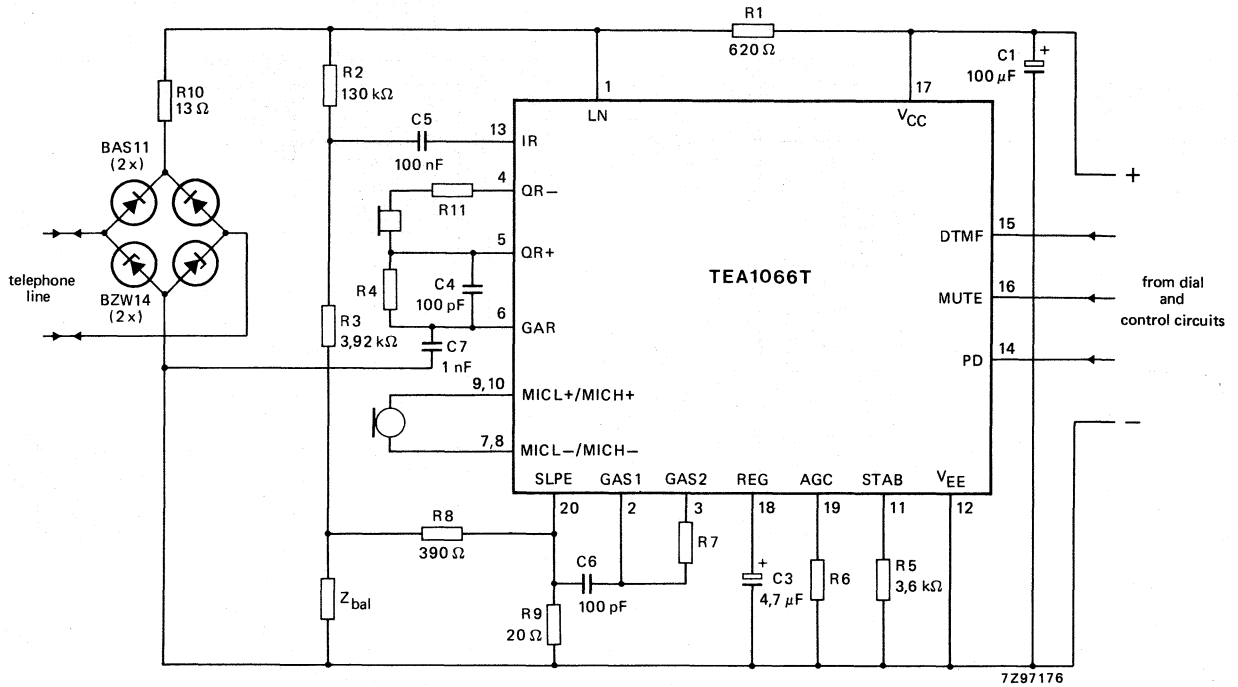


Fig. 10 Typical application of the TEA1066T, shown here with a piezoelectric earpiece and DTMF dialling. The bridge to the left and R10 limit the current into the circuit and the voltage across the circuit during line transients. Pulse dialling or register recall require a different protection arrangement.

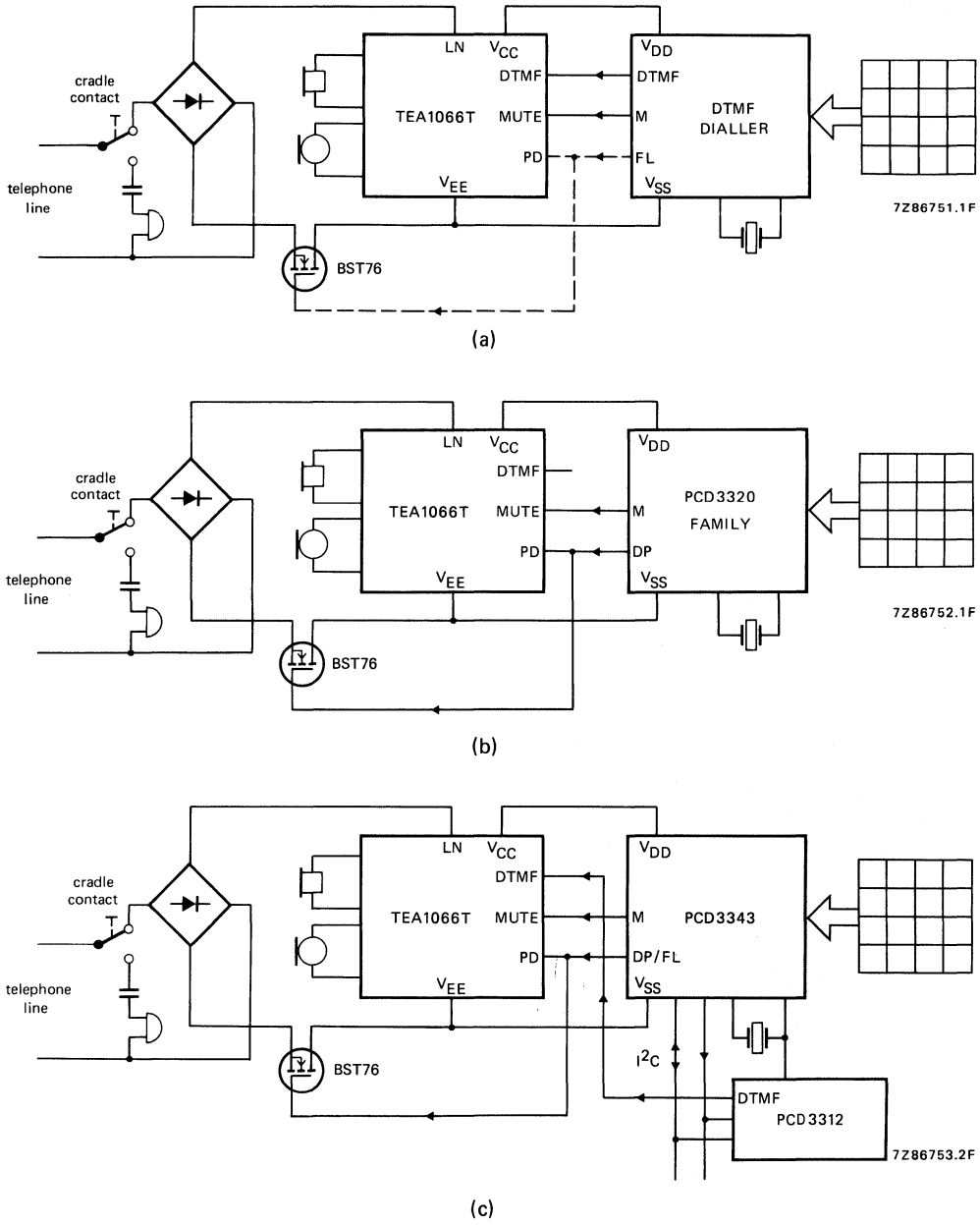


Fig. 11 Typical applications of the TEA1066T (simplified). (a) DTMF set with a CMOS DTMF dialling circuit. The dashed lines show an optional flash (register recall by timed loop break).
b: Pulse dial set with one of the PCD3320 family of CMOS interrupted current-loop dialling circuits.
(c) Dual-standard (pulse and DTMF) feature phone with the PCD3343 CMOS telephone controller and the PCD3312 CMOS DTMF generator with I^2C bus.

LOW VOLTAGE VERSATILE TELEPHONE TRANSMISSION CIRCUIT WITH DIALLER INTERFACE

GENERAL DESCRIPTION

The TEA1067 is a bipolar integrated circuit performing all speech and line interface functions required in fully electronic telephone sets. It performs electronic switching between dialling and speech. The circuit is able to operate down to DC line voltage of 1,6 V (with reduced performance) to facilitate the use of more telephone sets in parallel.

Features

- Low DC line voltage; operates down to 1,6 V (excluding polarity guard)
- Voltage regulator with adjustable static resistance
- Provides supply with limited current for external circuitry
- Symmetrical high-impedance inputs (64 kΩ) for dynamic, magnetic or piezoelectric microphones
- Asymmetrical high-impedance input (32 kΩ) for electret microphone
- DTMF signal input with confidence tone
- Mute input for pulse or DTMF dialling
- Power down input for pulse dial or register recall
- Receiving amplifier for magnetic, dynamic or piezoelectric earpieces
- Large amplification setting range on microphone and earpiece amplifiers
- Line loss compensation facility, line current dependent (microphone and earpiece amplifiers)
- Gain control adaptable to exchange supply
- Possibility to adjust the DC line voltage

QUICK REFERENCE DATA

Line voltage at I_{line} = 15 mA	V_{LN}	typ. 3,9	V
Line current operating range (pin 1)			
normal operation	I_{line}	11 to 140	mA
with reduced performance	I_{line}	1 to 11	mA
Internal supply current			
power down input LOW	I_{CC}	typ. 1	mA
power down input HIGH	I_{CC}	typ. 55	μA
Supply current for peripherals			
at I_{line} = 15 mA, mute input HIGH			
$V_{CC} > 2,2$ V	I_P	typ. 1,8	mA
$V_{CC} > 2,8$ V	I_P	typ. 0,7	mA
Voltage amplification range			
microphone amplifier	A_{vd}	44 to 52	dB
receiving amplifier	A_{vd}	20 to 45	dB
Line loss compensation			
Amplification control range	A_{vd}	typ. 6	dB
Exchange supply voltage range	V_{exch}	24 to 60	V
Exchange feeding brdige resistance range	R_{exch}	400 to 1000	Ω
Operating ambient temperature range	T_{amb}	−25 to + 75	°C

PACKAGE OUTLINE

18-lead dual in-line; plastic (SOT-102HE).

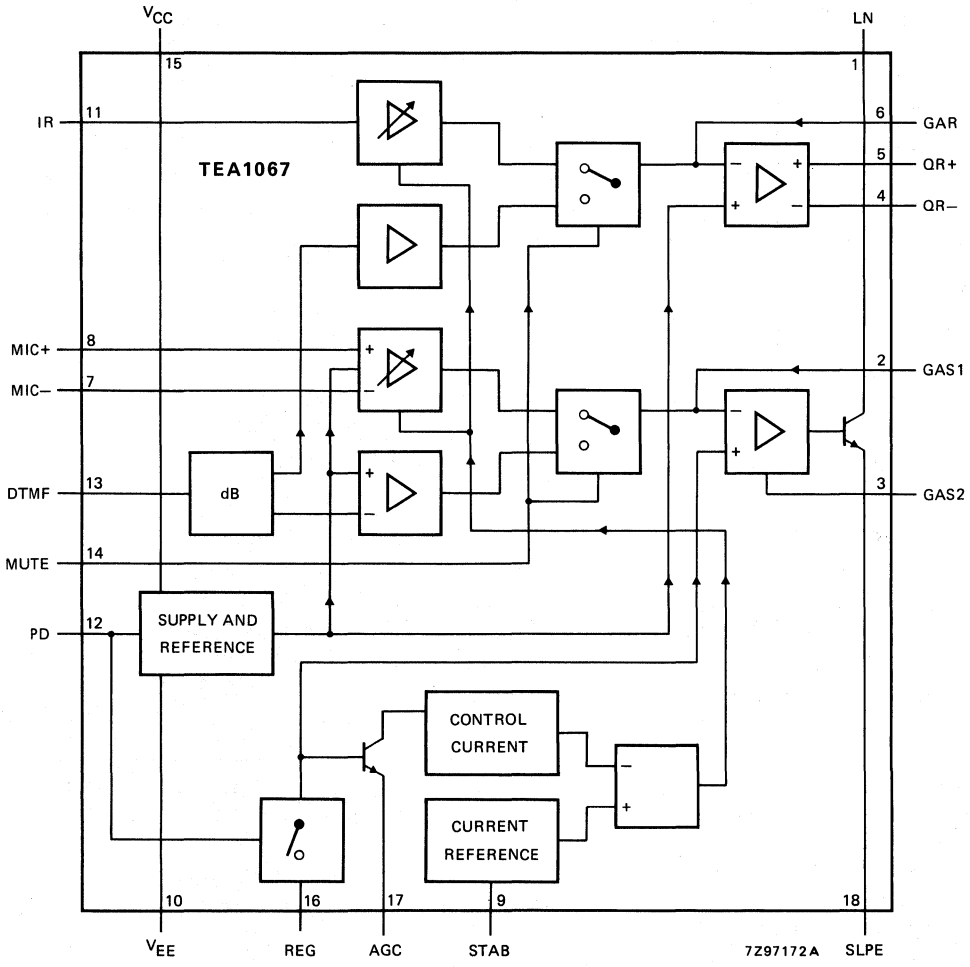


Fig. 1 Block diagram.

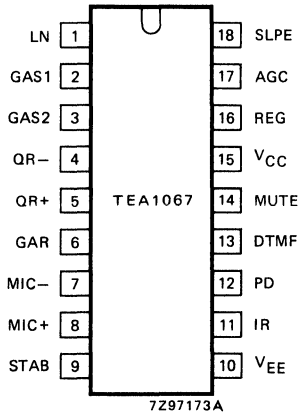


Fig. 2 Pinning diagram.

PINNING

1	LN	positive line terminal
2	GAS1	gain adjustment; transmitting amplifier
3	GAS2	gain adjustment; transmitting amplifier
4	QR–	inverting output, receiving amplifier
5	QR+	non-inverting output, receiving amplifier
6	GAR	gain adjustment; receiving amplifier
7	MIC–	inverting microphone input
8	MIC+	non-inverting microphone input
9	STAB	current stabilizer
10	V_{EE}	negative line terminal
11	IR	receiving amplifier input
12	PD	power-down input
13	DTMF	dual-tone multi-frequency input
14	MUTE	mute input
15	V_{CC}	positive supply decoupling
16	REG	voltage regulator decoupling
17	AGC	automatic gain control input
18	SLPE	slope (d.c. resistance) adjustment

DEVELOPMENT DATA

FUNCTIONAL DESCRIPTION

Supply: V_{CC}, LN, SLPE, REG and STAB

The circuit and its peripheral circuits usually are supplied from the telephone line. The circuit develops its own supply voltage at V_{CC} and regulates its voltage drop. The supply voltage V_{CC} may also be used to supply external peripheral circuits, e.g. dialling and control circuits.

The supply has to be decoupled by connecting a smoothing capacitor between V_{CC} and V_{EE}; the internal voltage regulator has to be decoupled by a capacitor from REG to V_{EE}. An internal current stabilizer is set by a resistor of 3,6 kΩ between STAB and V_{EE}.

The DC current flowing into the set is determined by the exchange supply voltage V_{exch}, the feeding bridge resistance R_{exch}, the d.c. resistance of the subscriber line R_{line} and the DC voltage on the subscriber set (see Fig. 3).

If the line current I_{line} exceeds the current I_{CC} + 0,5 mA required by the circuit itself ($I_{CC} \simeq 1$ mA), plus the current I_p required by the peripheral circuits connected to V_{CC}, then the voltage regulator diverts the excess current via LN.

The voltage regulator adjusts the average voltage on LN to:

$$V_{LN} = V_{ref} + I_{SLPE} \times R9 = V_{ref} + (I_{line} - I_{CC} - 0{,}5 \times 10^{-3} - I_P) \times R9.$$

V_{ref} being an internally generated temperature compensated reference voltage of 3,6 V and R9 being an external resistor connected between SLPE and V_{EE}. The preferred value of R9 is 20 Ω. Changing R9 will have influence on microphone gain, DTMF gain, gain control characteristics, side tone, maximum output swing on LN and on the DC characteristic (especially in the low voltage part). Under normal conditions $I_{SLPE} \gg I_{CC}$ + 0,5 mA + I_p. The static behaviour of the circuit then equals a 3,6 V voltage regulator diode with an internal resistance R9. In the audio frequency range the dynamic impedance equals R1. The internal reference voltage can be adjusted by means of an external resistor R_{VA}. R_{VA} (1-16) connected between pins LN and REG will decrease the internal reference voltage. R_{VA} (16-18) connected between REG and SLPE will increase the internal reference voltage.

At line currents below 9 mA the internal reference voltage is automatically adjusted to a lower value (Typ. 1,6 V at 1 mA). This means that the operation of more telephone sets in parallel is possible with DC line voltages (excluding the polarity guard) down to an absolute minimum voltage of 1,6 V.
At line currents below 9 mA the circuit has limited sending and receiving levels.

FUNCTIONAL DESCRIPTION (continued)

The current I_p available from V_{CC} for supplying peripheral circuits depends on external components and on the line current. Fig. 4 shows this current for $V_{CC} > 2{,}2$ V minimum. If MUTE is LOW the available current is further reduced when the receiving amplifier is driven. To increase the supply possibilities, the supply IC TEA1080 can be connected in parallel with R1 (Fig. 11(c)). An alternative is to set the DC line voltage to a higher value by means of an external resistor R_{VA} (16-18) connected between REG and SLPE.

Microphone inputs MIC+ and MIC– and gain pins: GAS1 and GAS2

The TEA1067 has symmetrical microphone inputs. Its input impedance is 64 kΩ (2 x 32 kΩ) and its voltage amplification is typ. 52 dB. Either dynamic, magnetic, piezoelectric microphones or an electret microphone with built-in FET source follower can be used.
The arrangements with the microphone types mentioned are shown in Fig. 5.

The amplification of the microphone amplifier can be adjusted between 44 dB to 52 dB to suit the sensitivity of the transducer used. The amplification is proportional to external resistor R7 connected between GAS1 and GAS2. An amplification more than 52 dB is possible (up to 60 dB), however in that case the spread of the DC voltage (V_{LN}) will increase and the minimum voltage at 11 mA (V_{LN} = 3,55 V) cannot be guaranteed. An external capacitor C6 of 100 pF between GAS1 and SLPE is required to ensure stability. A larger value may be chosen to obtain a first-order low-pass filter. The cut-off frequency corresponds with the time constant R7 x C6.

Mute input: MUTE

A HIGH level at MUTE enables the DTMF input and inhibites the microphone inputs and the receiving amplifier input: a LOW level or an open circuit does the reverse. Switching the mute input will cause negligible clicks at the telephone outputs and on the line. In case the line current drops below 6 mA (parallel operation of more sets) the circuit is always in speech condition independent of the DC level applied to the MUTE input.

Dual-tone multi-frequency input DTMF

When the DTMF input is enabled, dialling tones may be sent onto the line. The voltage amplification from DTMF to LN is typ. 25,5 dB and varies with R7 in the same way as the amplification of the microphone amplifier. The signalling tones can be heard in the earpiece at a low level (confidence tone).

Receiving amplifier: IR, QR+, QR– and GAR

The receiving amplifier has one input IR and two complementary outputs, a non-inverting output QR+ and an inverting output QR–. These outputs may be used for single-ended or for differential drive, depending on the sensitivity and type of earpiece used (see Fig. 6). Amplification from IR to QR+ is typ. 31 dB. This will be sufficient for low-impedance magnetic or dynamic earpieces; these are suited for single-ended drive. By using both outputs (differential drive) the amplification is increased by 6 dB and differential drive becomes possible. This feature can be used in case the earpiece impedance exceeds 450 Ω (high-impedance dynamic, magnetic or piezoelectric earpieces).

The output voltage of the receiving amplifier is specified for continuous-wave drive. The maximum output voltage will be higher under speech conditions, where the ratio of peak and r.m.s. value is higher.

The amplification of the receiving amplifier can be adjusted between 20 and 39 dB with single ended drive and between 26 and 45 dB in case of differential drive to suit the sensitivity of the transducer used. The amplification is proportional to external resistor R4 connected from GAR to QR+.

Two external capacitors C4 = 100 pF and C7 = 10 x C4 = 1 nF are necessary to ensure stability.
A larger value of C4 may be chosen to obtain a first-order low-pass filter. The "cut-off" frequency corresponds with the time constant R4 x C4.

Automatic gain control input AGC

Automatic line loss compensation will be obtained by connecting a resistor R6 from AGC to V_{EE}. This automatic gain control varies the amplification of the microphone amplifier and the receiving amplifier in accordance with the d.c. line current. The control range is 6 dB. This corresponds with a line length of 5 km for a 0,5 mm diameter copper twisted-pair cable with a DC resistance of 176 Ω/km and an average attenuation of 1,2 dB/km.

Resistor R6 should be chosen in accordance with the exchange supply voltage and its feeding bridge resistance (see Fig. 7 and Table 1). Different values of R6 give the same ratio of line currents for begin and end of the control range. If automatic line loss compensation is not required AGC may be left open. The amplifiers then all give their maximum amplification as specified.

Power-down input PD

During pulse dialling or register recall (timed loop break) the telephone line is interrupted, as a consequence it provides no supply for the transmission circuit and the peripherals connected to V_{CC}. These gaps have to be bridged by the charge in the smoothing capacitor C1. The requirements on this capacitor are relaxed by applying a HIGH level to the PD input during the time of the loop break, which reduces the supply current from typ. 1 mA to typ. 55 μA.

A HIGH level at PD further disconnects the capacitor at REG, with the effect that the voltage stabilizer will have no switch-on delay after line interruptions. This results in no contribution of the IC to the current waveform during pulse dialling or register recall.
When this facility is not required PD may be left open.

DEVELOPMENT DATA

Side-tone suppression

Suppression of the transmitted signal in the earpiece is obtained by the anti-side-tone network consisting of $R1//Z_{line}$, R2, R3, R8, R9 and Z_{bal} (see Fig. 10). Maximum compensation is obtained when the following conditions are fulfilled:

a) $R9.R2 = R1(R3 + [R8//Z_{bal}])$

b) $[Z_{bal}/(Z_{bal} + R8)] = [Z_{line}/(Z_{line} + R1)]$

If fixed values are chosen for R1, R2, R3 and R9, then condition a) will always be fulfilled provided that $|R8//Z_{bal}| \ll R3$.

To obtain optimum side-tone-suppression, condition b) has to be fulfilled resulting in:

$$Z_{bal} = (R8/R1)Z_{line} = k.Z_{line}$$

where k is a scale factor; $k = (R8/R1)$.

Scale factor k (value of R8) must be chosen to meet the following criteria:

- compatibility with a standard capacitor from the E6 or E12 range for Z_{bal}
- $|Z_{bal}//R8| \ll R3$
- $|Z_{bal} + R8| \ll R9$

In practice Z_{line} varies strongly with the line length and cable type; consequently an average value has to be chosen for Z_{bal}. The suppression further depends on the accuracy with which Z_{bal}/k equals the average line impedance.

The anti-side-tone network as used in the standard application (Fig. 10) attenuates the signal from the line with 32 dB. The attenuation is nearly flat over the audio-frequency range.
Instead of the above described special bridge, the conventional Wheatstone bridge configuration can be used as an alternative anti-side-tone circuit. Both bridges can be used with either a resistive set impedance or with a complex set impedance.
More information can be found in the application report.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Positive line voltage continuous	V_{LN}	max.	12	V
Repetitive line voltage during switch-on or line interruption	V_{LN}	max.	13,2	V
Repetitive peak line voltage t_p/p = 1 ms/5 s; R10 = 13 Ω; R9 = 20 Ω (see Fig. 10)	V_{LN}	max.	28	V
Line current	I_{line}		140	mA
Voltage on all other pins	V_i	max.	V_{CC} + 0,7	V
	$-V_i$	max.	0,7	V
Total power dissipation	P_{tot}	max.	640	mW
Storage temperature range	T_{stg}		−40 to + 125	°C
Operating ambient temperature range	T_{amb}		−25 to + 75	°C

CHARACTERISTICS

I_{line} = 11 to 140 mA; V_{EE} = 0 V; f = 800 Hz; T_{amb} = 25 °C; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply: LN and V_{CC} (pins 1 and 15)					
Voltage drop over circuit; between pin 1 and pin 10 = V_{LN}; microphone inputs open					
at I_{line}	V_{LN}	–	1,6	–	V
at I_{line} = 4 mA	V_{LN}	1,75	2,0	2,25	V
at I_{line} = 7 mA	V_{LN}	2,25	2,8	3,35	V
at I_{line} = 11 mA	V_{LN}	3,55	3,8	4,05	V
at I_{line} = 15 mA	V_{LN}	3,65	3,90	4,15	V
at I_{line} = 100 mA	V_{LN}	4,9	5,6	6,5	V
at I_{line} = 140 mA	V_{LN}	–	–	7,5	V
Variation with temperature at I_{line} = 15 mA	$\Delta V_{LN}/\Delta T$	−3	−1	1	mV/K
Voltage drop over circuit with external resistor R_{VA}; at I_{line} = 15 mA					
R_{VA} (pin 1 to pin 16) = 68 kΩ	V_{LN}	3,1	3,4	3,7	V
R_{VA} (pin 16 to pin 18) = 39 kΩ	V_{LN}	4,2	4,5	4,8	V
Supply current I_{CC}; current into pin 15					
PD = LOW (pin 12); V_{CC} = 2,8 V	I_{CC}	–	1,0	1,35	mA
PD = HIGH (pin 12); V_{CC} = 2,8 V	I_{CC}	–	55	82	μA
Current available from pin 15 to supply peripheral circuits; at I_{line} = 15 mA; $V_{CC} >$ = 2,2 V; Mute = High	I_P	1,4	1,8	–	mA

DEVELOPMENT DATA

parameter	symbol	min.	typ.	max.	unit
Microphone inputs MIC+ and MIC– (pins 7 and 8)					
Input impedance					
Differential (between pins 7 and 8)	$\lvert z_{is} \rvert$	51	64	77	kΩ
Single ended (pin 7 or w.r.t. V_{EE})	$\lvert z_{is} \rvert$	25,5	32	38,5	kΩ
Common-mode rejection ratio	k_{CMR}	–	82	–	dB
Voltage amplification (from pin 7-8 to pin 1); I_{line} = 15 mA; R7 = 68 kΩ	A_{vd}	51	52	53	dB
Variation with frequency at f = 300 to 3400 Hz	$\Delta A_{vd}/\Delta f$	–0,5	± 0,2	+ 0,5	dB
Variation with temperature at I_{line} = 50 mA; T_{amb} = –25 to + 75 °C	$\Delta A_{vd}/\Delta T$	–	t.b.n.	–	dB
Dual-tone multi-frequency input DTMF (pin 13)					
Input impedance	$\lvert z_{is} \rvert$	t.b.n.	20,7	t.b.n.	kΩ
Voltage amplification (from pin 13 to pin 1); at I_{line} = 15 mA; R7 = 68 kΩ	A_{vd}	24,5	25,5	26,5	dB
Variation with frequency f = 300 to 3400 Hz	$\Delta A_{vd}/\Delta f$	–0,5	± 0,2	+ 0,5	dB
Variation with temperature at I_{line} = 50 mA; T_{amb} = –25 to + 75 °C	$\Delta A_{vd}/\Delta T$	–	± 0,2	–	dB
Gain adjustment GAS1 and GAS2 (pins 2 and 3)					
Amplification variation with R7 (connected between pins 2 and 3), transmitting amplifier	ΔA_{vd}	–8	–	0	dB
Sending amplifier output LN (pin 1)					
Output voltage at I_{line} = 15 mA;					
d_{tot} = 2%	$V_{LN(rms)}$	–	1,9	–	V
d_{tot} = 10%	$V_{LN(rms)}$	1,9	2,2	–	V
at I_{line} = 4 mA; d_{tot} = 10%	$V_{LN(rms)}$	–	0,8	–	V
at I_{line} = 7 mA; d_{tot} = 10%	$V_{LN(rms)}$	–	1,4	–	V
Noise output voltage I_{line} = 15 mA; R7 = 68 kΩ; 200 Ω between pins 7 and 8; psophometrically weighted (P53 curve)	$V_{no(rms)}$	–	–72	–	dBmp
Receiving amplifier input IR (pin 11)					
Input impedance	$\lvert z_{is} \rvert$	t.b.n.	20	t.b.n.	kΩ

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Receiving amplifier outputs QR+ and QR− (pins 5 and 4)					
Output impedance; single-ended	$\|z_{os}\|$	–	4	–	Ω
Voltage amplification from pin 11 to pin 4-5 at I_{line} = 15 mA; R4 = 100 kΩ;					
single ended; R_L = 300 Ω (from pin 11 to pins 4-5)	A_{vd}	30	31	32	dB
differential; R_L = 600 Ω (from pin 11 to pins 4-5)	A_{vd}	36	37	38	dB
Variation with frequency, f = 300 to 3400 Hz	$\Delta A_{vd}/\Delta f$	−0,5	± 0,2	+ 0,5	dB
Variation with temperature I_{line} = 50 mA; T_{amb} = −25 to + 75 °C	$\Delta A_{vd}/\Delta T$	–	± 0,2	–	dB
Output voltage at I_p = 0; d_{tot} = 2%; sine-wave drive; R4 = 100 kΩ					
single-ended; R_L = 150 Ω	$V_{o(rms)}$	0,25	0,29	–	V
single-ended; R_L = 450 Ω	$V_{o(rms)}$	0,45	0,55	–	V
differential; C_L = 47 nF (100 Ω series resistors); f = 3400 Hz	$V_{o(rms)}$	0,65	0,80	–	V
Output voltage at I_p = 0; d_{tot} = 10%; sine-wave drive; R4 = 100 kΩ; R_L = 150 Ω					
I_{line} = 4 mA	$V_{o(rms)}$	–	15	–	mV
I_{line} = 7 mA	$V_{o(rms)}$	–	130	–	mV
Noise output voltage I_{line} = 15 mA; R4 = 100 kΩ; pin 11 open psophometrically weighted (P53 curve)					
single-ended; R_L = 300 Ω	$V_{no(rms)}$	–	50	–	μV
differential; R_L = 600 Ω	$V_{no(rms)}$	–	100	–	μV
Gain adjustment GAR (pin 6)					
Amplification variation with R4 (connected between pins 6 and 5), receiving amplifier	ΔA_{vd}	−11	–	+ 8	dB
MUTE input (pin 14)					
Input voltage					
HIGH	V_{IH}	1,5	–	V_{CC}	V
LOW	I_{IL}	–	–	0,3	V
Input current	I_{MUTE}	–	8	15	μA
Reduction of voltage amplification from MIC+ (pin 7) and MIC− (pin 8) to LN at MUTE = HIGH	ΔA_{vd}	–	70	–	dB

parameter	symbol	min.	typ.	max.	unit
Voltage amplification from DTMF (pin 13) to QR+ (pin 5) or QR– (pin 4) at MUTE = HIGH; single-ended load R_L = 300 Ω	A_{vd}	–21	–19	–17	dB
Power-down input PD (pin 12)					
Input voltage					
HIGH	V_{IH}	1,5	–	V_{CC}	V
LOW	V_{IL}	–	–	0,3	V
Input current (into pin 12)	I_{PD}	–	5	10	μA
Automatic gain control input AGC (pin 17)					
Controlling the gain from pin 11 to pins 4-5 and the gain from pins 7-8 to pin 1 R6 = 110 kΩ (between pins 17 and 10) Amplification control range	A_{vd}	–	–6	–	dB
Highest line current for maximum amplification	I_{line}	–	22	–	mA
Lowest line current for minimum amplification	I_{line}	–	60	–	mA

DEVELOPMENT DATA

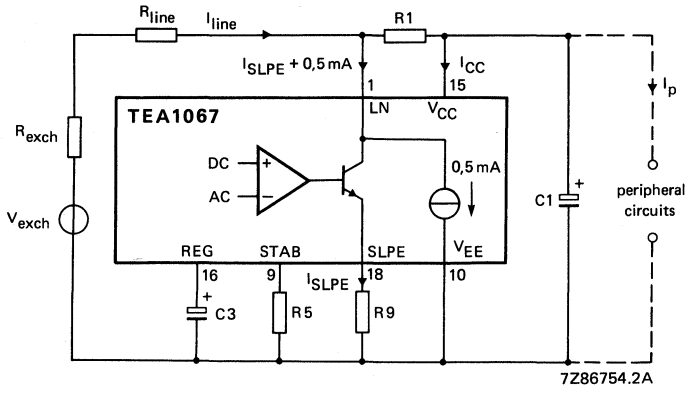
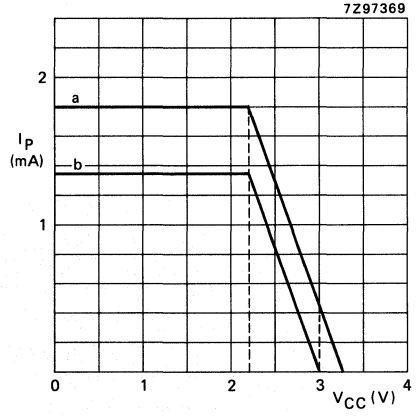


Fig. 3 Supply arrangement.



a) = 1,8 mA, b) = 1,35 mA
I_{line} = 15 mA at V_{LN} = 3,9 V
R1 = 620 Ω and R9 = 20 Ω

Fig. 4 Typical current I_p available from V_{CC} for peripheral circuitry with $V_{CC} >= 2{,}2$ V. Curve (a) is valid when the receiving amplifier is not driven or when MUTE = HIGH, curve (b) is valid when MUTE = LOW and the receiving amplifier is driven; $V_{o(rms)}$ = 150 mV, R_L = 150 Ω asymmetrical. The supply possibilities can be increased simply by setting the voltage drop over the circuit V_{LN} to a higher value by means of resistor R_{VA} (16-18).

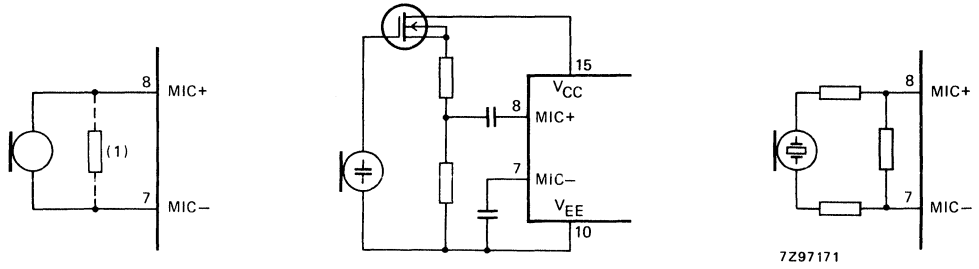


Fig. 5 Alternative microphone arrangements. a: magnetic or dynamic microphone. The resistor marked (1) may be connected to lower the terminating impedance. In case of sensitive microphone types a resistor attenuator can be used to prevent overloading of the microphone inputs (b) electret microphone, (c) piezoelectric microphone.

DEVELOPMENT DATA

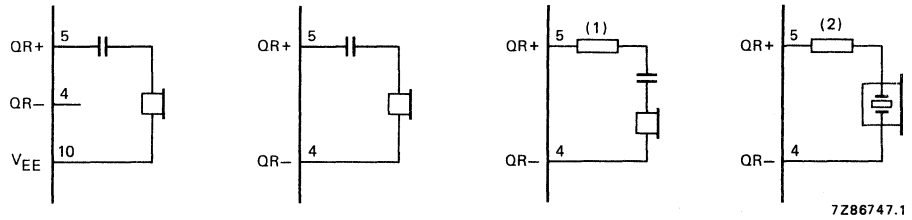


Fig. 6 Alternative receiver arrangements. (a) dynamic telephone with less than 450 Ω impedance. (b) dynamic telephone with more than 450 Ω impedance. (c) magnetic telephone with more than 450 Ω impedance. The resistor marked (1) may be connected to prevent distortion (inductive load). (d) piezoelectric telephone. The resistor marked (2) is required to increase the phase margin (capacitive load).

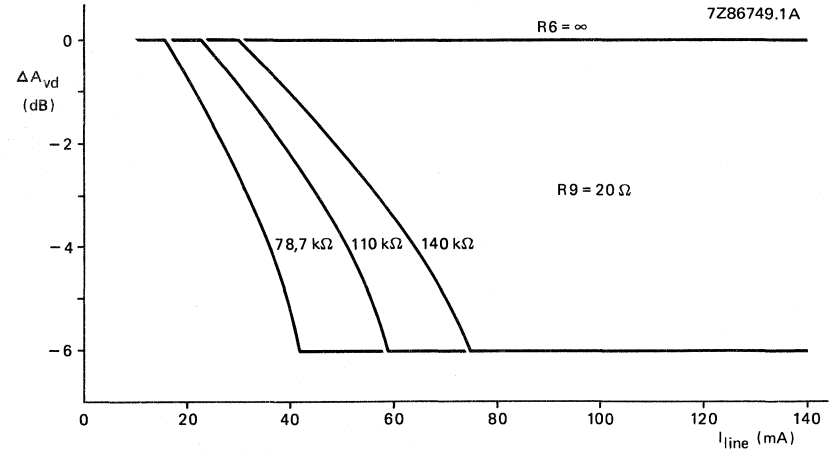


Fig. 7 Variation of amplification with line current, with R6 as a parameter.

		R_{exch} (Ω)			
		400	600	800	1000
		R6 (kΩ)			
V_{exch} (V)	36	100	78,7	X	X
	48	140	110	93,1	82
	60	X	X	120	102

R9 = 20 Ω

Table 1. Values of resistor R6 for optimum line loss compensation, for various usual values of exchange supply voltage V_{exch} and exchange feeding bridge resistance R_{exch}.

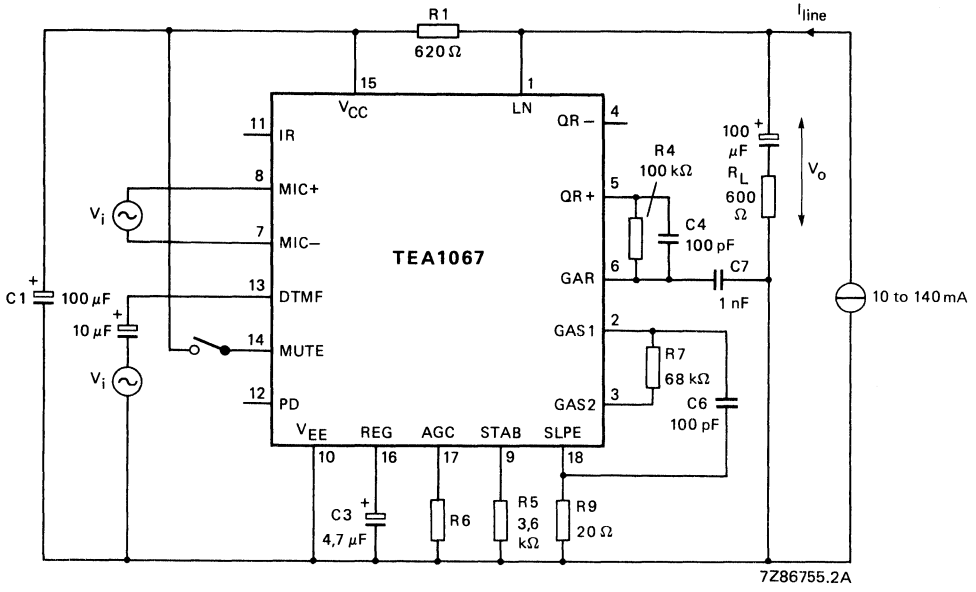


Fig. 8 Test circuit for defining voltage amplification of MIC+, MIC– and DTMF inputs. Voltage amplification is defined as: $A_{vd} = 20 \log |V_o/V_i|$. For measuring the amplification from MIC+ and MIC– the MUTE input should be LOW or open, for measuring the DTMF input MUTE should be HIGH. Inputs not under test should be open.

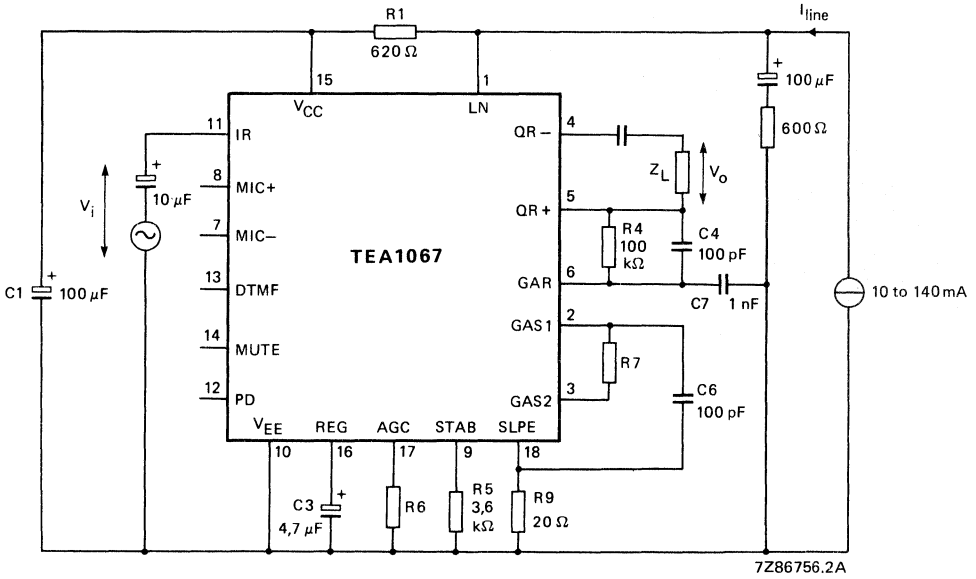


Fig. 9 Test circuit for defining voltage amplification of the receiving amplifier. Voltage amplification is defined as: $A_{vd} = 20 \log |V_o/V_i|$.

DEVELOPMENT DATA

APPLICATION INFORMATION

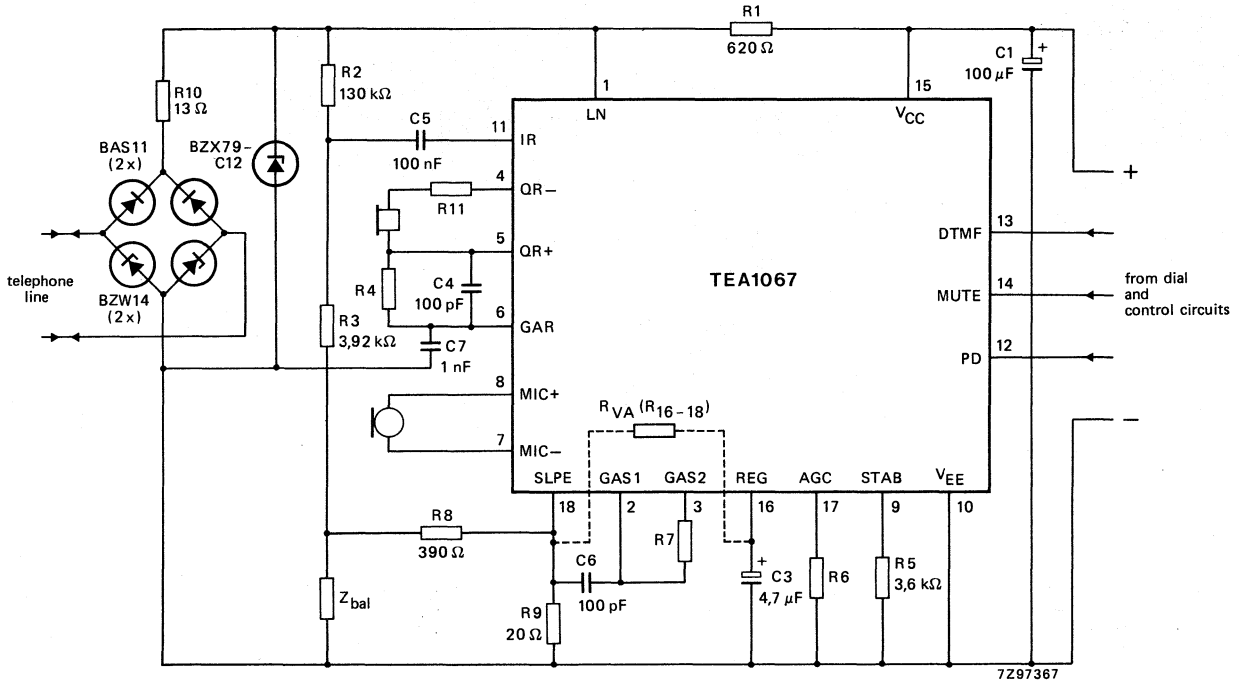


Fig. 10 Typical application of the TEA1067, shown here with a piezoelectric earpiece and DTMF dialling. The bridge to the left, the zener diode and R10 limit the current into the circuit during and the voltage across the circuit during line transients. Pulse dialling or register recall require a different protection arrangement. By means of resistor R_{VA} (R_{16-18}) the DC line voltage can be set to a higher value.

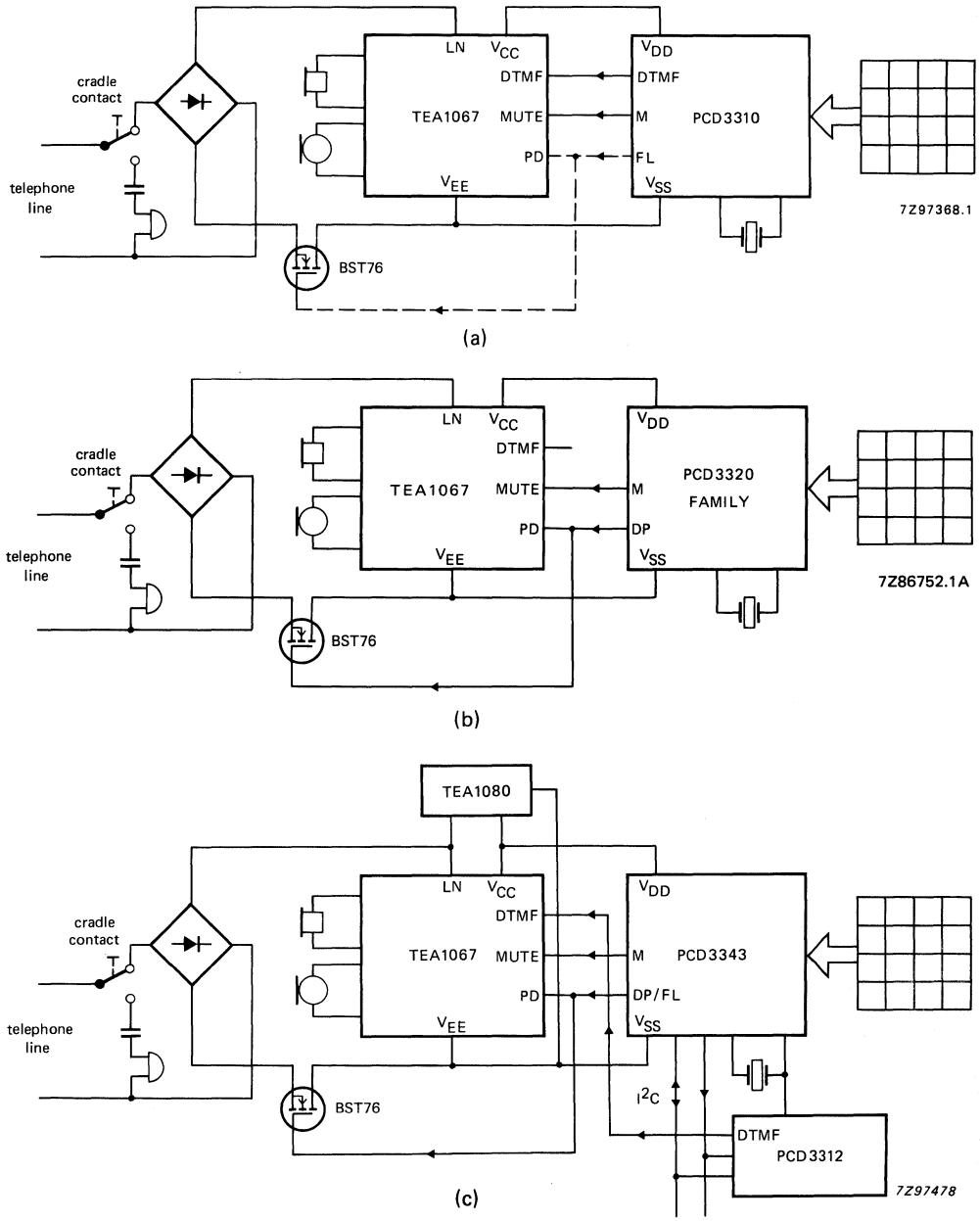


Fig. 11 Typical applications of the TEA1067 (simplified).

a) DTMF-Pulse set with CMOS-bilingual dialling circuit PCD3310. The dashed lines show an optional flash (register recall by timed loop break).

b) Pulse dial set with one of the PCD3320 family of CMOS interrupted current-loop dialling circuits.

c) Dual-standard (pulse and DTMF) feature phone with the PCD3343 CMOS telephone controller and the PCD3312 CMOS DTMF general with I^2C bus. Supply is provided by the TEA1080 supply circuit.

VERSATILE TELEPHONE TRANSMISSION CIRCUIT

GENERAL DESCRIPTION

The TEA1068 is a bipolar integrated circuit performing all speech and line interface functions required in fully electronic telephone sets. The circuit internally performs electronic switching between dialling and speech.

Features

- Voltage regulator with adjustable static resistance
- Provides supply for external circuitry
- Symmetrical high-impedance inputs (64 kΩ) for dynamic, magnetic or piezoelectric microphones
- Asymmetrical high-impedance input (32 kΩ) for electret microphone
- DTMF signal input with confidence tone
- Mute input for pulse or DTMF dialling
- Power down input for pulse dial or register recall
- Receiving amplifier for magnetic, dynamic or piezoelectric earpieces
- Large amplification setting range on microphone and earpiece amplifiers
- Line loss compensation facility, line current dependent for microphone and receiving amplifiers
- Gain control adaptable to exchange supply
- Possibility to adjust the d.c. line voltage

QUICK REFERENCE DATA

Line voltage at I_{LN} = 15 mA	V_{LN}	typ. 4,45	V
Line current operating range	I_{LN}	10 to 140	mA
Internal supply current			
power down input PD = LOW	I_{CC}	typ. 1	mA
Power down input PD = HIGH	I_{CC}	typ. 55	μA
Supply current for peripherals at I_{line} = 15 mA, mute input HIGH			
$V_{CC} > 2,2$ V	I_P	max. 2,5	mA
$V_{CC} > 3,0$ V	I_P	max. 1,2	mA
Voltage amplification range			
microphone amplifier	A_{vd}	44 to 60	dB
receiving amplifier	A_{vd}	17 to 39	dB
Line loss compensation			
Amplification control range	ΔA_{vd}	typ. 6	dB
Exchange supply voltage range	V_{exch}	24 to 60	V
Exchange feeding bridge resistance range	R_{exch}	400 to 1000	Ω
Operating ambient temperature range	T_{amb}	−25 to +75	°C

PACKAGE OUTLINE

18-lead DIL; plastic (SOT-102HE).

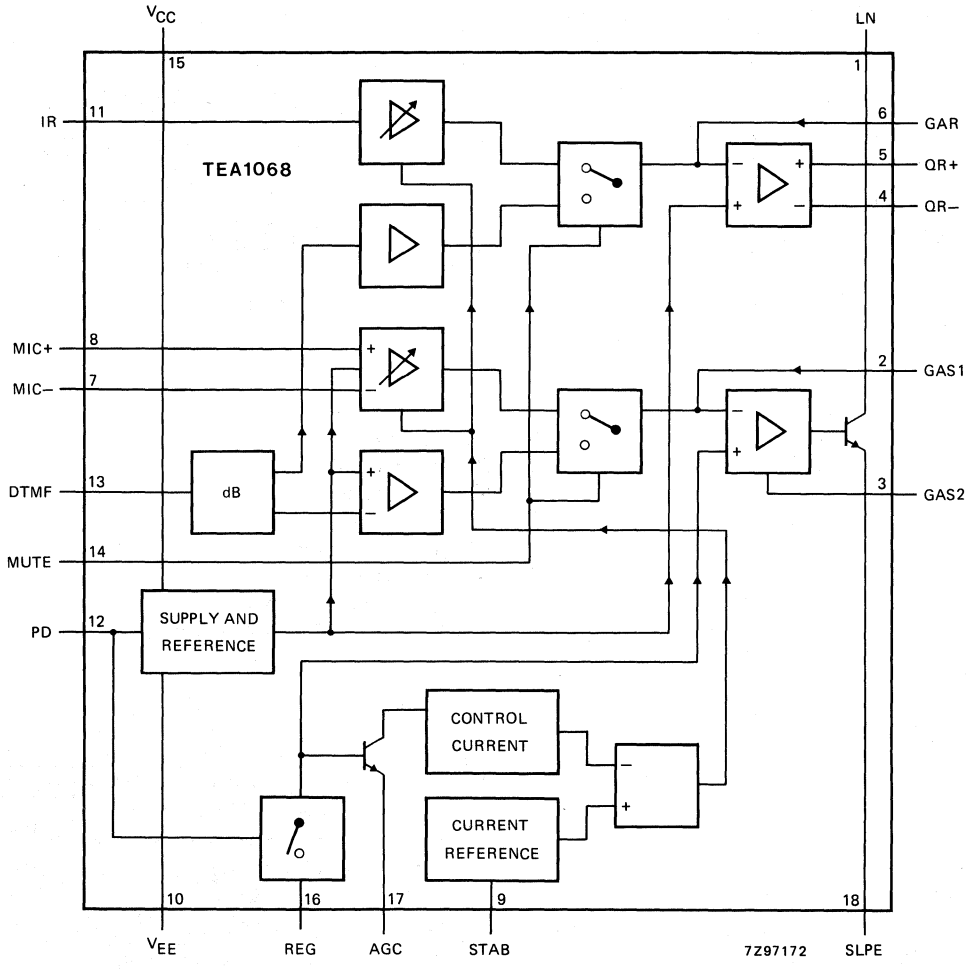


Fig. 1 Block diagram.

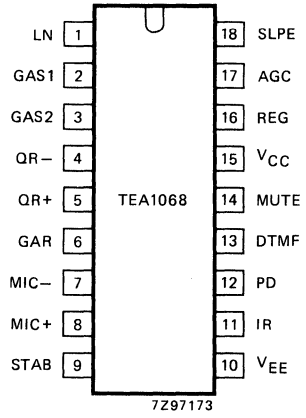


Fig. 2 Pinning diagram.

PINNING

1	LN	positive line connection
2	GAS1	gain adjustment connection, sending amplifier
3	GAS2	gain adjustment connection, sending amplifier
4	QR−	inverting output, receiving amplifier
5	QR+	non-inverting output, receiving amplifier
6	GAR	gain adjustment connection, receiving amplifier
7	MIC+	non-inverting microphone input
8	MIC−	inverting microphone input
9	STAB	current stabilizer connection
10	V_{EE}	negative line connection
11	IR	receiving amplifier input
12	PD	power-down input
13	DTMF	dual-tone multi-frequency input
14	MUTE	mute input
15	V_{CC}	positive supply decoupling connection
16	REG	voltage regulator decoupling connection
17	AGC	automatic gain control input
18	SLPE	slope (d.c. resistance) adjustment connection

DEVELOPMENT DATA

FUNCTIONAL DESCRIPTION

Supply: V_{CC}, LN, SLPE, REG and STAB

The circuit and its peripheral circuits usually are supplied from the telephone line. The circuit develops its own supply voltage at V_{CC} and regulates its voltage drop. The supply voltage V_{CC} may also be used to supply external peripheral circuits, e.g. dialling and control circuits.

The supply has to be decoupled by connecting a smoothing capacitor between V_{CC} and V_{EE}; the internal voltage regulator has to be decoupled by a capacitor from REG to V_{EE}. An internal current stabilizer is set by a resistor of 3,6 kΩ between STAB and V_{EE}.

The d.c. current flowing into the set is determined by the exchange supply voltage V_{exch}, the feeding bridge resistance R_{exch}, the d.c. resistance of the subscriber line R_{line} and the d.c. voltage on the subscriber set (see Fig. 3).

If the line current I_{line} exceeds the current I_{CC} + 0,5 mA required by the circuit itself, (I_{CC} ca. 1 mA), plus the current I_p required by the peripheral circuits connected to V_{CC}, then the voltage regulator diverts the excess current via LN.

The voltage regulator adjusts the average voltage on LN to:
$V_{LN} = V_{ref} + I_{SLPE} \times R9 = V_{ref} + (I_{line} - I_{CC} - 0{,}5.10^{-3} - I_p) \times R9$.

V_{ref} being an internally generated temperature compensated reference voltage of 4,2 V and R9 being an external resistor connected between SLPE and V_{EE}. The preferred value of R9 is 20 Ω. Changing R9 will have influence on microphone gain, DTMF gain, gain control characteristics, side tone and maximum output swing on LN.
Under normal conditions $I_{SLPE} \gg I_{CC}$ + 0,5 mA + I_p. The static behaviour of the circuit then equals a 4,2 V voltage regulator diode with an internal resistance R9. In the audio frequency range the dynamic impedance equals R1.

FUNCTIONAL DESCRIPTION (continued)

The internal reference voltage can be adjusted by means of an external resistor R_{VA}. This resistor connected between LN (pin 1) and REG (pin 16) will decrease the internal reference voltage. R_{VA} connected between REG (pin 16) and SLPE (pin 18) will increase the internal reference voltage. The current I_p available from V_{CC} for supplying peripheral circuits depends on external components and on the line current. Fig. 4 shows this current for $V_{CC} > 2{,}2$ V and for $V_{CC} > 3$ V. Of which 3 V being the minimum supply voltage for most CMOS circuits including a diode voltage drop for an enable diode. If MUTE is LOW the available current is further reduced when the receiving amplifier is driven.

Microphone inputs MIC+ and MIC– and gain adjustment pins GAS1 and GAS2

The TEA1068 has symmetrical microphone inputs. Its input impedance is 64 kΩ (2 x 32 kΩ) and its voltage amplification is typical 52 dB. Either dynamic, magnetic, piezoelectric microphones or an electret microphone with built-in FET source follower can be used.

The arrangements with the microphone types mentioned are shown in Fig. 5.

The amplification of the microphone amplifier can be adjusted over a range of + or –8 dB to suit the sensitivity of the transducer used. The amplification is proportional to external resistor R7 connected between GAS1 and GAS2.

An external capacitor C6 of 100 pF between GAS1 and SLPE is required to ensure stability. A larger value may be chosen to obtain a first-order low-pass filter. The cut-off frequency corresponds with the time constant R7 x C6.

Mute input MUTE

A HIGH level at MUTE enables the DTMF input and inhibits the microphone inputs and the receiving amplifier input, a LOW level or an open circuit does the reverse. Switching the mute input will cause negligible clicks at the telephone outputs and on the line.

Dual-tone multi-frequency input DTMF

When the DTMF input is enabled, dialling tones may be sent onto the line. The voltage amplification from DTMF to LN is typ. 25,5 dB and varies with R7 in the same way as the amplification of the microphone amplifier. The signalling tones can be heard in the earpiece at a low level (confidence tone).

Receiving amplifier: IR, QR+, QR– and GAR

The receiving amplifier has one input IR and two complementary outputs, a non-inverting output QR+ and an inverting output QR–. These outputs may be used for single-ended or for differential drive, depending on the sensitivity and type of earpiece used (see Fig. 6). Amplification from IR to QR+ is typ. 25 dB. This will be sufficient for low-impedance magnetic or dynamic earpieces; these are suited for single-ended drive. By using both outputs (differential drive) the amplification is increased by 6 dB and this makes differential drive possible. This feature can be used in case the earpiece impedance exceeds 450 Ω (high-impedance dynamic, magnetic or piezoelectric earpieces).

The output voltage of the receiving amplifier is specified for continuous-wave drive. The maximum output voltage will be higher under speech conditions, where the ratio of peak and r.m.s. value is higher.

The amplification of the receiving amplifier can be adjusted over a range of + and –8 dB to suit the sensitivity of the transducer used. The amplification is proportional to external resistor R4 connected from GAR to QR+.

Two external capacitors C4 (100 pF) and C7 (10 x C4 = 1 nF) are necessary to ensure stability. A larger value of C4 may be chosen to obtain a first-order low-pass filter. The cut-off frequency corresponds with the time constant R4 x C4.

Automatic gain control input AGC

Automatic line loss compensation will be obtained by connecting a resistor R6 from AGC to V_{EE}. This automatic gain control varies the amplification of the microphone amplifier and the receiving amplifier in accordance with the d.c. line current. The control range is 6 dB. This corresponds with a line length of 5 km for a 0,5 mm diameter copper twisted-pair cable with a d.c. resistance of 176 Ω/km and an average attenuation of 1,2 dB/km.

Resistor R6 should be chosen in accordance with the exchange supply voltage and its feeding bridge resistance (see Fig. 7 and Table 1). Different values of R6 give the same ratio of line currents for begin and end of the control range.

If automatic line loss compensation is not required AGC may be left open. The amplifiers then all give their maximum amplification as specified.

Power-down input PD

During pulse dialling or register recall (timed loop break) the telephone line is interrupted, as a consequence it provides no supply for the transmission circuit and the peripherals connected to V_{CC}. These gaps have to be bridged by the charge in the smoothing capacitor C1. The requirements on this capacitor are relaxed by applying a HIGH level to the PD input during the time of the loop break, which reduces the supply current from typ. 1 mA to typ. 55 μA.

A HIGH level at PD further disconnects the capacitor at REG, with the effect that the voltage stabilizer will have no switch-on delay after line interruptions. This results in no contribution of the IC to the current waveform during pulse dialling or register recall.
When this facility is not required PD may be left open.

Side-tone suppression

Suppression of the transmitted signal in the earpiece is obtained by the anti-side-tone network consisting of $R1//Z_{line}$, R2, R3, R8, R9 and Z_{bal} (see Fig. 10). Maximum compensation is obtained when the following conditions are fulfilled:

a) $R9.R2 = R1(R3 + [R8//Z_{bal}])$

b) $[Z_{bal}/(Z_{bal} + R8)] = [Z_{line}/(Z_{line} + R1)]$.

If fixed values are chosen for R1, R2, R3 and R9 then condition a) will always be fulfilled provided that $|R8//Z_{bal}| \ll R3$.
To obtain optimum side tone suppression condition b) has to be fulfilled resulting in:

$$Z_{bal} = (R8/R1)Z_{line} = k.Z_{line}$$

where k is a scale factor $k = (R8/R1)$.
Scale factor k (value of R8) must be chosen to meet the following criteria:
– compatibility with a standard capacitor from the E6 or E12 range for Z_{bal}
– $|Z_{bal}//R8| \ll R3$
– $|Z_{bal}+R8| \gg R9$

In practice Z_{line} varies strongly with line length and cable type; consequently an average value has to be chosen for Z_{bal}. The suppression further depends on the accuracy with which Z_{bal}/k equals the average line impedance.

The anti-side-tone network as used in the standard application (Fig. 10) attenuates the signal from the line with 32 dB. The attenuation is nearly flat over the audio frequency range.

Instead of the above described special TEA1068 bridge, the conventional Wheatstone bridge configuration can be used as an alternative anti-side-tone circuit. Both bridge types can be used with either a resistive set impedance or with a complex set impedance.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Positive line voltage (d.c.)	V_{LN}	max.	12	V
Repetitive line voltage during switch-on or line interruption	V_{LN}	max.	13,2	V
Repetitive peak line voltage t_p/P = 1 ms/5 s; R_{10} = 13 Ω; R_g = 20 Ω (see Fig. 10)	V_{LNRM}	max.	28	V
Line current	I_{line}	max.	140	mA
Voltage on all other pins	V_i	max.	V_{CC} + 0,7	V
	$-V_i$	max.	0,7	V
Total power dissipation	P_{tot}	max.	640	mW
Storage temperature range	T_{stg}		−40 to + 125	°C
Operating ambient temperature range	T_{amb}		−25 to + 75	°C

CHARACTERISTICS

$I_{line} = I_1 = 10$ to 140 mA; $V_{EE} = V10 = 0$ V; f = 800 Hz; R9 = 20 Ω; $T_{amb} = 25$ °C; unless otherwise specified.

parameter	symbol	min.	typ.	max.	unit
Supply: LN and V_{CC} (pins 1 and 15)					
Voltage drop over circuit V_{1-10} microphone inputs open					
at I_{line} = 5 mA	V_{LN}	3,95	4,25	4,55	V
at I_{line} = 15 mA	V_{LN}	4,20	4,45	4,70	V
at I_{line} = 100 mA	V_{LN}	5,4	6,1	7	V
at I_{line} = 140 mA	V_{LN}	–	–	8	V
Variation with temperature at I_{line} = 15 mA	$\Delta V_{LN}/\Delta T$	−4	−2	0	mV/K
Voltage drop over circuit at I_{line} = 15 mA					
$R_{VA} = R_{1-16}$ = 68 kΩ	V_{LN}	3,45	3,80	4,10	V
$R_{VA} = R_{16-18}$ = 39 kΩ	V_{LN}	4,65	5,0	5,35	V
Supply current					
PD (pin 12) = LOW; V_{CC} = 2,8 V	I_{CC}	–	0,96	1,30	mA
PD (pin 12) = HIGH; V_{CC} = 2,8 V	I_{CC}	–	55	82	μA
Microphone inputs MIC+ and MIC− (pins 8 and 7)					
Input impedance					
differential (between pins 7 and 8)	$\lvert z_{is} \rvert$	51	64	77	kΩ
single-ended (pin 7-10 or pin 8-10)	$\lvert z_{is} \rvert$	25,5	32	38,5	kΩ
Common-mode rejection ratio	k_{CMR}	–	82	–	dB
Voltage amplification (pins 7, 8-1) I_{line} = 15 mA; R7 = 68 kΩ	A_{vd}	51	52	53	dB
Variation with frequency at f = 300 to 3400 Hz	$\Delta A_{vd}/\Delta f$	−0,5	± 0,2	+ 0,5	dB
Variation with temperature at I_{line} = 50 mA; T_{amb} = −25 to + 75 °C	$\Delta A_{vd}/\Delta T$	–	± 0,2	–	dB
Dual-tone multi-frequency input DTMF (pin 13)					
Input impedance	$\lvert z_{is} \rvert$	16,8	20,7	24,6	kΩ
Voltage amplification I_{line} = 15 mA; R7 = 68 kΩ	A_{vd}	24,5	25,5	26,5	dB
Variation with frequency f = 300 to 3400 Hz	$\Delta A_{vd}/\Delta f$	−0,5	± 0,2	+ 0,5	dB
Variation with temperature at I_{line} = 50 mA; T_{amb} = −25 to + 75 °C	$\Delta A_{vd}/\Delta T$	–	± 0,2	–	dB
Gain adjustment GAS1 and GAS2 (pins 2 and 3)					
Amplification variation with R7 transmitting amplifier	ΔA_{vd}	−8	–	+ 8	dB

DEVELOPMENT DATA

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Transmitting amplifier output LN (pin 1)					
Output voltage at I_{line} = 15 mA;					
d_{tot} = 2%	$V_{LN(rms)}$	1,9	2,3	–	V
d_{tot} = 10%	$V_{LN(rms)}$	–	2,6	–	V
Noise output voltage					
I_{line} = 15 mA; R7 = 68 kΩ; R_{7-8} = 200 Ω psophometrically weighted (P53 curve)	$V_{no(rms)}$	–	−72	–	dBmp
Receiving amplifier input IR (pin 11)					
Input impedance	$\|z_{is}\|$	16,5	20,4	24,3	kΩ
Receiving amplifier outputs QR+ and QR− (pins 5 and 4)					
Output impedance; single-ended	$\|z_{os}\|$	–	4	–	Ω
Voltage amplification from pin 11 to pins 4 or 5) I_{line} = 15 mA; R4 = 100 kΩ;					
single-ended; R_L = 300 Ω	A_{vd}	24	25	26	dB
differential; R_L = 600 Ω	A_{vd}	30	31	32	dB
Variation with frequency, f = 300 to 3400 Hz	$\Delta A_{vd}/\Delta f$	−0,5	± 0,2	+ 0,5	dB
Variation with temperature I_{line} = 50 mA; T_{amb} = −25 to + 75 °C	$\Delta A_{vd}/\Delta T$	–	± 0,2	–	dB
Output voltage at I_p = 0; d_{tot} = 2%; R4 = 100 kΩ; sine-wave drive					
single-ended; R_L = 150 Ω	$V_{o(rms)}$	0,3	0,38	–	V
single-ended; R_L = 450 Ω	$V_{o(rms)}$	0,4	0,52	–	V
differential; C_L = 47 nF; (100 Ω series resistor); f = 3400 Hz	$V_{o(rms)}$	0,8	1,0	–	V
Noise output voltage I_{line} = 15 mA; R4 = 100 kΩ; pin 11 = IR = open psophometrically weighted (P53 curve)					
single-ended; R_L = 300 Ω	$V_{no(rms)}$	–	50	–	μV
differential; R_L = 600 Ω	$V_{no(rms)}$	–	100	–	μV
Gain adjustment GAR (pin 6)					
Amplification variation with R4 between pins 6 and 5 receiving amplifier	ΔA_{vd}	−8	–	+ 8	dB

parameter	symbol	min.	typ.	max.	unit
MUTE input (pin 14)					
Input voltage					
HIGH	V_{IH}	1,5	–	V_{CC}	V
LOW	V_{IL}	–	–	0,3	V
Input current	I_{MUTE}	–	8	15	μA
Reduction of voltage amplification					
MIC+ and MIC– to LN at MUTE = HIGH	A_{vd}	–	70	–	dB
Voltage amplification from					
DTMF to QR+ or QR– at MUTE = HIGH					
R4 = 100 kΩ; R_L single-ended = 300 Ω	A_{vd}	–21	–19	–17	dB
Power-down input PD (pin 12)					
Input voltage					
HIGH	V_{IH}	1,5	–	V_{CC}	V
LOW	V_{IL}	–	–	0,3	V
Input current	I_{PD}	–	5	10	μA
Automatic gain control AGC (pin 17)					
Controlling the gain from pin 11 to pins 4 and 5 and the gain from pins 7 and 8 to pin 1					
R6 = 110 kΩ; connected between pins 17 and 10					
Amplification control range	$-\Delta A_{vd}$	–	6	–	dB
Highest line current for A_{max}	I_{line}	–	22	–	mA
Lowest line current for A_{min}	I_{line}	–	60	–	mA

DEVELOPMENT DATA

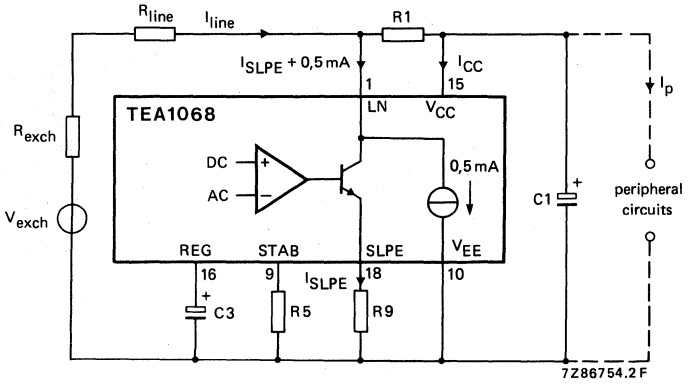


Fig. 3 Supply arrangement.

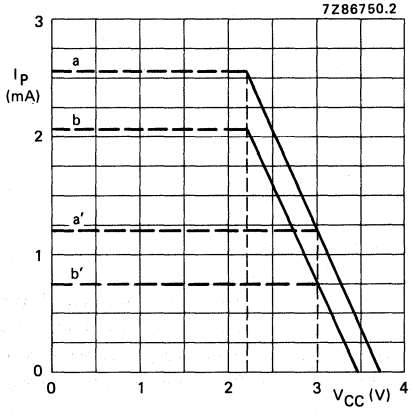


Fig. 4 Maximum current I_p available from V_{CC} for peripheral circuitry with $V_{CC} > 2{,}2$ V and $V_{CC} > 3$ V. Curves (a) and (a') are valid when the receiving amplifier is not driven or when MUTE is HIGH, curves (b) and (b') are valid when MUTE is LOW and the receiving amplifier is driven at $V_{o(rms)} = 150$ mV and $R_L = 150\ \Omega$ asymmetrical.
$I_{line} = 15$ mA at $V_{LN} = 4{,}45$ V; R1 = 620 Ω and R9 = 20 Ω.
a) = 2,55 mA; b) = 2,1 mA; a') = 1,2 mA and b') = 0,75 mA.

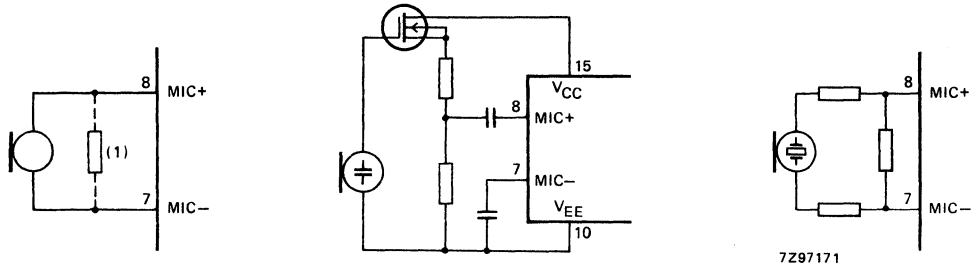


Fig. 5 Alternative microphone arrangements. a: magnetic or dynamic microphone. The resistor marked (1) may be connected to lower the terminating impedance. In case of sensitive microphone types a resistor attenuator can be used to prevent overloading of the microphone inputs (b) electret microphone, (c) piezoelectric microphone.

DEVELOPMENT DATA

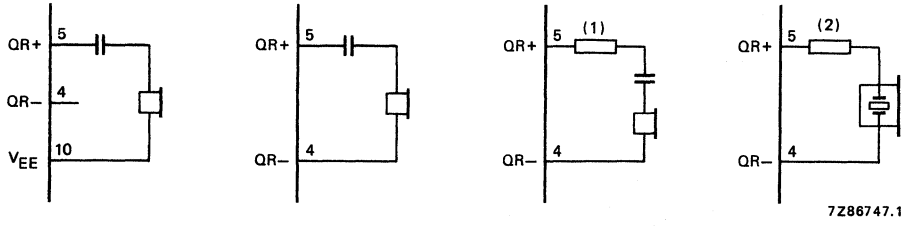


Fig. 6 Alternative receiver arrangements. (a) dynamic telephone with less than 450 Ω impedance. (b) dynamic telephone with more than 450 Ω impedance. (c) magnetic telephone with more than 450 Ω impedance. The resistor marked (1) may be connected to prevent distortion (inductive load). (d) piezoelectric telephone. The resistor marked (2) is required to increase the phase margin (capacitive load).

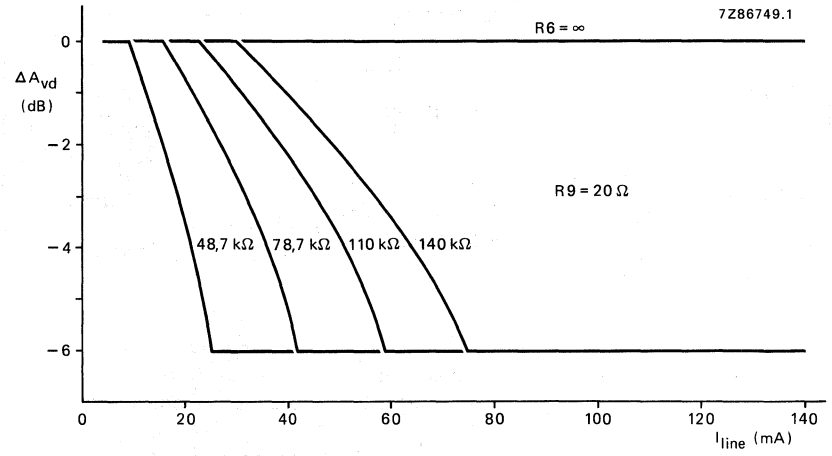


Fig. 7 Variation of amplification with line current, with R6 as a parameter.

		R_{exch} (Ω)			
		400	600	800	1000
		R6 (kΩ)			
V_{exch} (V)	24	61,9	48,7	X	X
	36	100	78,7	68	60,4
	48	140	110	93,1	82
	60	X	X	120	102

R9 = 20 Ω

Table 1. Values of resistor R6 for optimum line loss compensation, for various usual values of exchange supply voltage V_{exch} and exchange feeding bridge resistance R_{exch}.

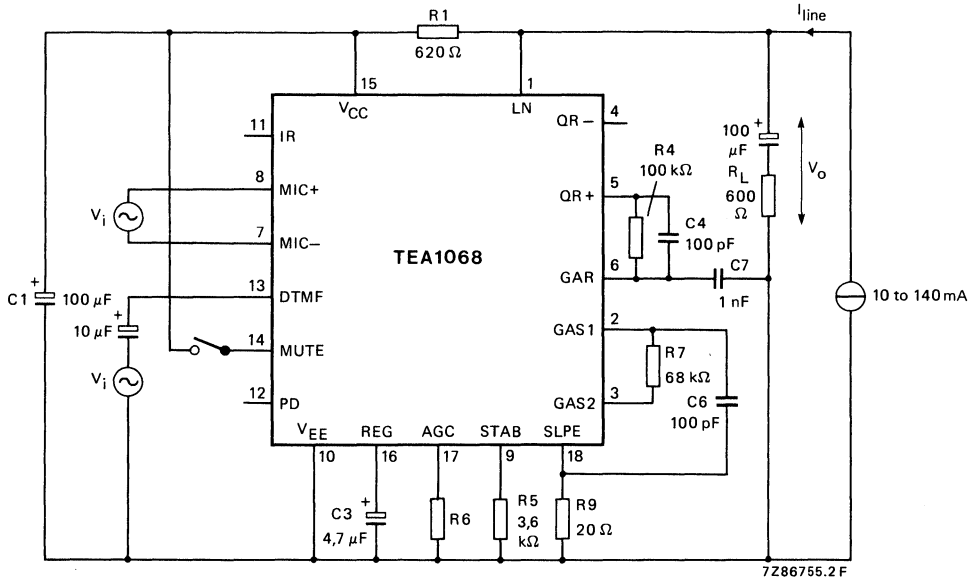


Fig. 8 Test circuit for defining voltage amplification of MIC+, MIC– and DTMF inputs. Voltage amplification is defined as: $A_{vd} = 20 \log |V_o/V_i|$. For measuring the amplification from MIC+ and MIC– the MUTE input should be LOW or open, for measuring the DTMF input MUTE should be HIGH. Inputs not under test should be open.

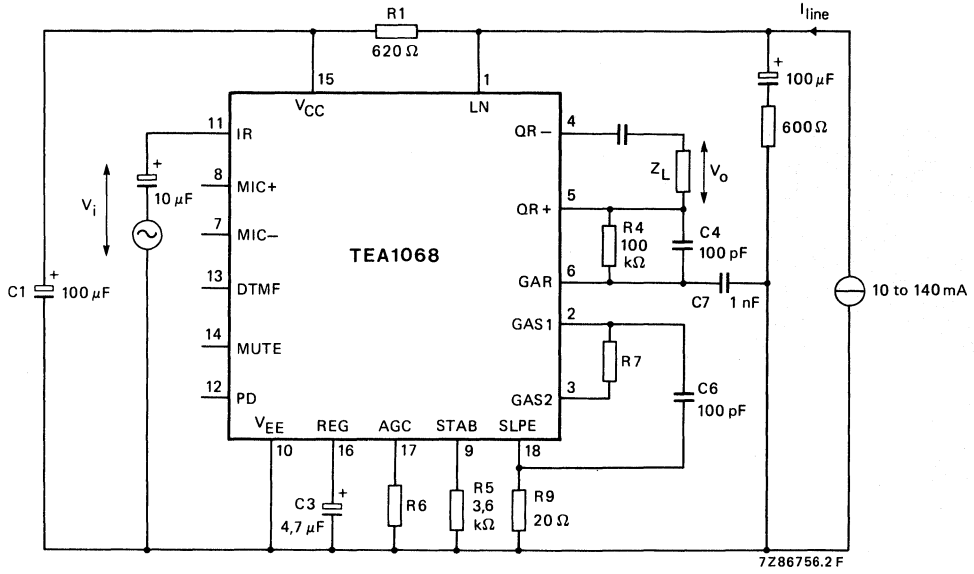


Fig. 9 Test circuit for defining voltage amplification of the receiving amplifier. Voltage amplification is defined as: $A_{vd} = 20 \log |V_o/V_i|$.

APPLICATION INFORMATION

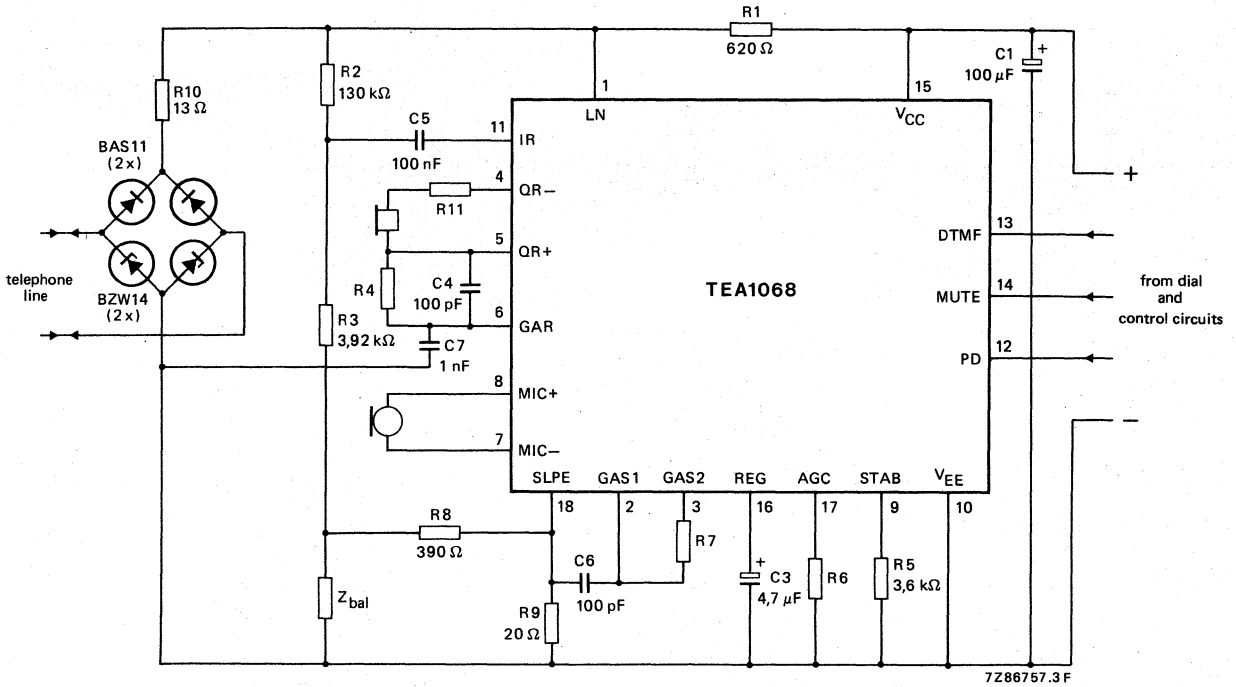


Fig. 10 Typical application of the TEA1068, shown here with a piezoelectric earpiece and DTMF dialling. The bridge to the left, the zener diode and R10 limit the current into the circuit during and the voltage across the circuit during line transients. Pulse dialling or register recall require a different protection arrangement.

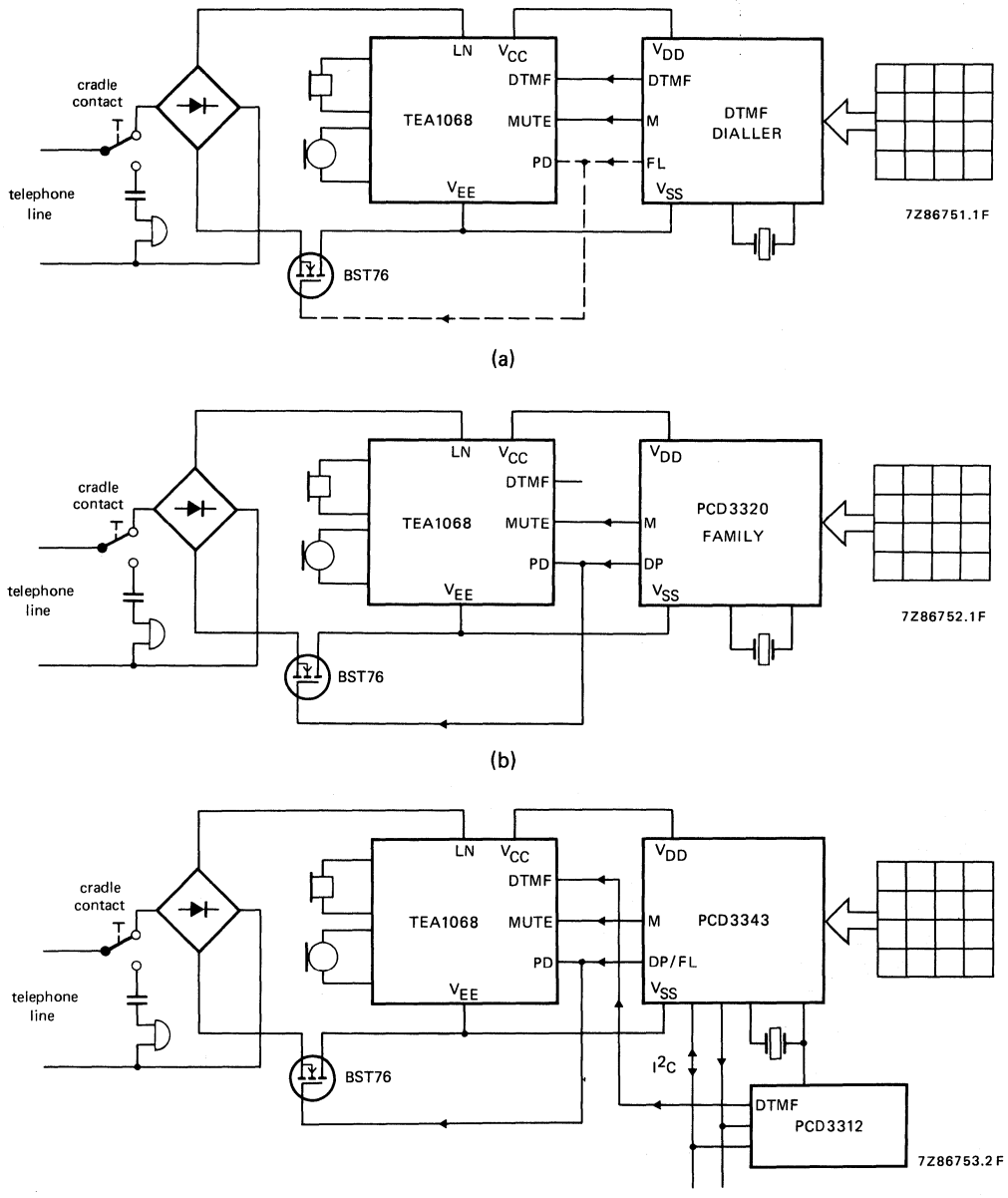


Fig. 11 Typical applications of the TEA1068 (simplified).

a: DTMF set with a CMOS DTMF dialling circuit. The dashed lines show an optional flash (register recall by times loop break).

b: Pulse dial set with the one of the PCD3320 family of CMOS interrupted current-loop dialling circuits.

c: Dual-standard (pulse and DTMF) feature phone with the PCD3343 CMOS telephone controller and the PCD3312 CMOS DTMF generator with I^2C bus.

DTMF GENERATOR FOR TELEPHONE DIALLING

The TEA1075 is a dual tone multi-frequency (DTMF) generator with line interface for use in push-button telephone sets containing an electronic speech circuit or a conventional hybrid transformer. The IC contains a mute switch handling the full line current, which allows two-wire connection between dial and speech parts. The logic inputs can be operated with a single contact keyboard or via a direct interface with a microcontroller. The line interface incorporates a filter amplifier, an output stage and a voltage regulator all of which are switched off when the speech circuit is connected to the line. The tone generator is supplied by a temperature compensated current stabilizer and is driven by a 3,58 MHz crystal.

The logic inputs contain an interface circuit which ensures well-defined states of the keyboard.

Features

- Two wire connection between dial and speech parts allowed
- Wide operating line current and temperature range
- No individual tone level adjustment required
- Few external components required
- All mute functions on chip
- Common inputs for keyboard and microcontroller
- Signal levels are independent from line current and temperature
- All pins protected against electrostatic discharges
- On-chip output stage and line regulator
- Single tone generation possible

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Operating d.c. line voltage	I_L = 15 mA	V_L	3,0	3,3	3,6	V
Line current range						
TEA1075P	–	I_L	10	–	120	mA
TEA1075T	–	I_L	10	–	90	mA
DTMF output levels (adjustable)						
low tones	$I_L > 12$ mA	V_{LG}	−11	–	−6	dBm
high tones	$I_L > 12$ mA	V_{HG}	−9	–	−4	dBm
Pre-emphasis	–	$V_{HG}-V_{LG}$	1	2	3	dB
Operating ambient temperature range	–	T_{amb}	−25	–	+ 70	°C

PACKAGE OUTLINES

TEA1075P: 18-lead DIL; plastic (SOT-102HE).
TEA1075T: 20-lead mini-pack; plastic (SO-20; SOT-163A).

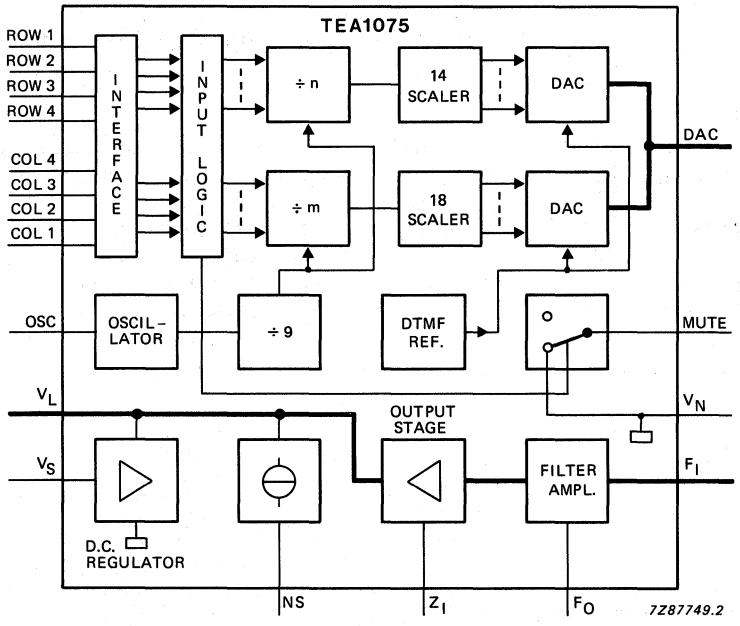


Fig. 1 Block diagram.

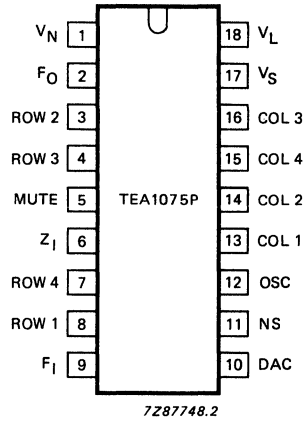


Fig. 2 Pinning diagram; TEA1075P.

PINNING

1	V_N	negative line voltage
2	F_O	filter output
3	ROW 2	row input 770 Hz/BCD input
4	ROW 3	row input 852 Hz/BCD input
5	MUTE	mute switch
6	Z_I	impedance setting terminal
7	ROW 4	row input 941 Hz/BCD input
8	ROW 1	row input 697 Hz/BCD input
9	F_I	filter input
10	DAC	DTMF level setting
11	NS	noise suppression input
12	OSC	oscillator input
13	COL 1	column input 1209 Hz/mute input
14	COL 2	column input 1336 Hz/mute input
15	COL 4	column input 1633 Hz/mute input
16	COL 3	column input 1477 Hz/enable input
17	V_S	voltage regulator filter
18	V_L	positive line voltage

DEVELOPMENT DATA

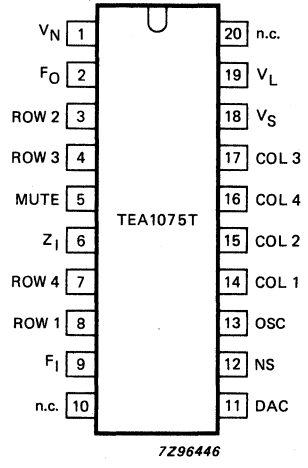


Fig. 3 Pinning diagram; TEA1075T.

1	V_N	negative line voltage
2	F_O	filter output
3	ROW 2	row input 770 Hz/BCD input
4	ROW 3	row input 852 Hz/BCD input
5	MUTE	mute switch
6	Z_I	impedance setting terminal
7	ROW 4	row input 941 Hz/BCD input
8	ROW 1	row input 697 Hz/BCD input
9	F_I	filter input
10	n.c.	not connected
11	DAC	DTMF level setting
12	NS	noise suppression input
13	OSC	oscillator input
14	COL 1	column input 1209 Hz/mute input
15	COL 2	column input 1336 Hz/mute input
16	COL 4	column input 1633 Hz/mute input
17	COL 3	column input 1477 Hz/enable input
18	V_S	voltage regulator filter
19	V_L	positive line voltage
20	n.c.	not connected

FUNCTIONAL DESCRIPTION

Voltage regulator

The voltage regulator is switched on when a keyboard button is pressed. It regulates the d.c. voltage drop across the IC to a nominal level of 3,3 V, shunting excess line current to maintain a working current of 8 mA within the chip. The voltage regulator is switched to a higher voltage level when the keyboard button is released.

The capacitor connected to input V_S provides a low-pass filter function to avoid influence of audio signals on the line. For a short period during switch-on time the capacitor is directly connected to the line to be charged and to reduce overshoot voltages.

When the TEA1075 is in the stand-by mode the voltage regulator circuit conducts as the d.c. line voltage set by the speech part reaches 6,0 V. Part of the line current then flows through the regulator.

Active output stage

The transmitter amplifier consists of a voltage to current converter with a class-A output stage. The circuit acts as a dynamic resistance (R_i) because of the feedback from the line to the input. This impedance can be set by output Z_I at pin 6:
R_i = 900 Ω if pin 6 is left open
R_i = 600 Ω if pin 6 is connected to V_N (pin 1).
The impedance is high as long as no key is depressed (stand-by mode).

Speech muting (see Fig. 4)

All mute functions are performed by internal switches. Pressing any keyboard push button switches the TEA1075 to the operating mode and isolates the speech part from the line.

The line adaption is taken over by the dial circuit which causes:
- line voltage to be set by the voltage regulator of the TEA1075
- impedance to be set by the active output stage of the TEA1075
- audio output stage to be connected to the line for DTMF tone transmission.

During the stand-by mode (no key pressed) the voltage on the line is set by the speech circuit. The minimum d.c. operating voltage of the dial circuit to guarantee detection of push button operation on the keyboard is 2,5 V. The impedance is equivalent to an 8 kΩ resistance and the current consumption 3 mA at V_L = 4,5 V. The stand-by current is used for the logic part as well as driving current for the internal switch which can switch the full line current available.

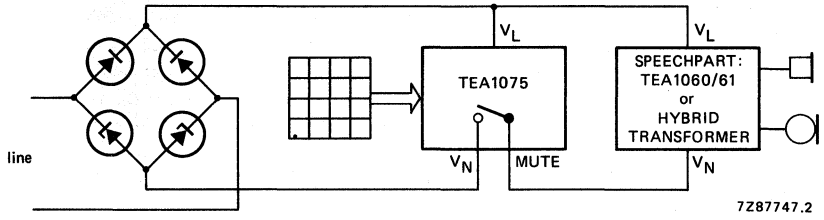


Fig. 4 Muting system.

Oscillator and DTMF generator

The crystal oscillator frequency (3,579 545 MHz) is divided by a factor of nine to give the clock frequency. A maximum division error of 0,31% is achieved in the TEA1075; CCITT recommendations are that tones should be within 1,5% of the specified frequencies.
A bias resistor of 1 to 4,7 MΩ must be connected between the oscillator input and V_L. An external frequency generator can be connected instead of a crystal (see Fig. 6).

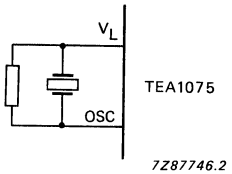


Fig. 5 Quartz crystal oscillator.

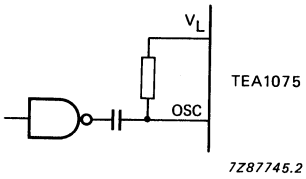


Fig. 6 External frequency generator.

The output from the dividers for the higher and the lower frequency tones are symmetrical square-wave pulses which contain considerable odd-numbered harmonics. The lower order odd-numbered harmonics (11th and less) are eliminated by synthesizing the tone frequencies as crude stepped sinewave approximations. Each half cycle of the tone waveform comprises seven discrete amplitudes for the lower frequency tone and nine for the higher frequency tone. Each amplitude increment is generated by switching on and off an individual current source for the duration of each step of the sinewave.
The frequency of the tones is varied by changing the duration of each step. This circuit allows the connection of a first or second order filter, depending on the distortion requirements (see filter and DTMF level).

Table 1 Deviation of ROW and COLUMN frequencies

	required freq. Hz	deviation %	real freq. Hz		required freq. Hz	deviation %	real freq. Hz
ROW 1	697	−0,24	695,33	COL 1	1209	−0,31	1205,23
ROW 2	770	−0,28	767,81	COL 2	1336	−0,10	1334,66
ROW 3	852	−0,25	849,84	COL 3	1477	−0,27	1473,06
ROW 4	941	−0,31	938,04	COL 4	1633	−0,18	1603,03

Filter and DTMF level

The output current from the DAC causes a voltage drop across R_{TLS}. At this point the signal path is broken to allow insertion of filter components in series with the amplifier input at pin 9.
The output of this amplifier is brought out to pin 2 to allow connection of filter components in the feedback path to provide additional attenuation of the higher-order odd harmonics of the tone frequencies.

The output amplitude of the tones is directly proportional to the value of R_{TLS} and can therefore be adjusted to meet specific requirements. Fig. 7 shows the output level as a function of R_{TLS} with R_i = 600 Ω. If R_i = 900 Ω, R_{TLS} must be multiplied by 1,28.

FUNCTIONAL DESCRIPTION (continued)

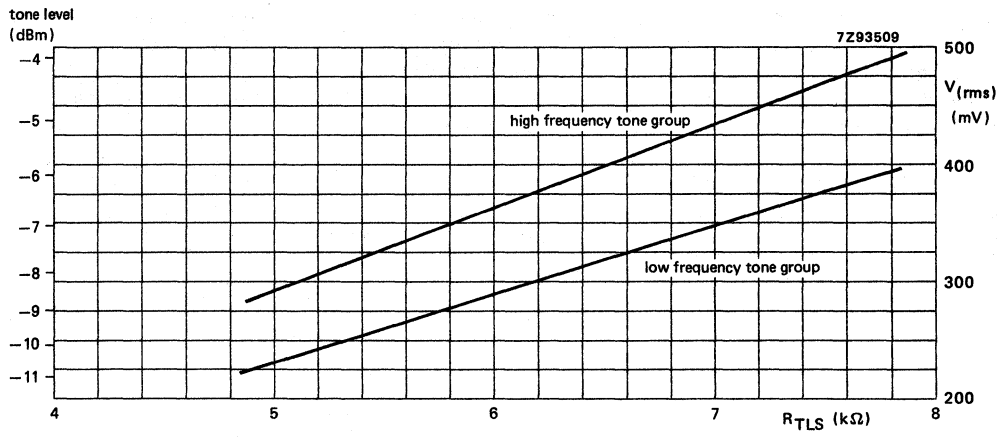


Fig. 7 DTMF level selection (R_i = 600 Ω).

When R_{TLS} is selected for the required tone level, C_{FI} can be calculated to minimize influence of the filter characteristic on the pre-emphasis parameter. The time constant for a single pole filter is determined by:

$$R_{TLS} \times C_{FI} = 26\ \mu s \text{ (see Fig. 17)}$$

If higher attenuation is required a second-order filter can be applied. The time constants for a second order filter are determined by:

$$R_{TLS} \times C_{FO} = 46\ \mu s \text{ and } R_{FS} \times C_{FI} = 59\ \mu s \text{ (see Fig. 16)}$$

Keyboard inputs

Inputs for the logic control are compatible with different types of keyboard. Tone combination are generated by:

- connecting one of the row inputs to one of the column inputs by one switch of a single contact keyboard

or

- application of a double contact keyboard with the common row contact tied to V_N and the common column contact connected to V_L via a 68 kΩ resistor.

Single tones can be generated by connecting a row input to V_N or a column input to V_L via a 68 kΩ resistor.

A debounce circuit eliminates switch bounce.

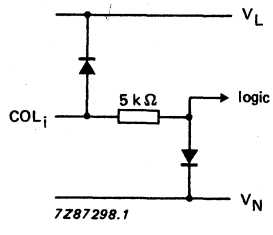


Fig. 8 Configuration of column inputs.

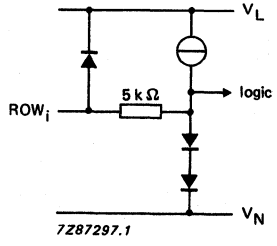


Fig. 9 Configuration of row inputs.

Microcontroller mode

The inputs for the keyboard can be used for direct connection to a microcontroller. If the column inputs are interconnected and made HIGH (> 0,9 V) the row inputs are changed to another mode, allowing the circuit to be driven by 4-bit data plus an enable signal. In this mode, it is possible to connect a separate mute enable signal on inputs COL 1, COL 2 and COL 4 and a tone enable input on COL 3.

Table 2 Truth table; microcontroller mode.

row				column		tones	symbol	mute *
1	2	3	4	1, 2, 4	3	Hz		
H	H	H	H	L	L	–	–	off
X	X	X	X	H	L	–	–	on
H	H	H	H	H	H	697/1209	1	on
H	H	H	L	H	H	697/1336	2	on
H	H	L	H	H	H	697/1477	3	on
H	H	L	L	H	H	697/1633	A	on
H	L	H	H	H	H	770/1209	4	on
H	L	H	L	H	H	770/1336	5	on
H	L	L	H	H	H	770/1477	6	on
H	L	L	L	H	H	770/1633	B	on
L	H	H	H	H	H	852/1209	7	on
L	H	H	L	H	H	852/1336	8	on
L	H	L	H	H	H	852/1477	9	on
L	H	L	L	H	H	852/1633	C	on
L	L	H	H	H	H	941/1209	*	on
L	L	H	L	H	H	941/1336	0	on
L	L	L	H	H	H	941/1477	#	on
L	L	L	L	H	H	941/1633	D	on

DEVELOPMENT DATA

* Mute "on" = switch between pin 5 and pin 1 is open.

FUNCTIONAL DESCRIPTION (continued)

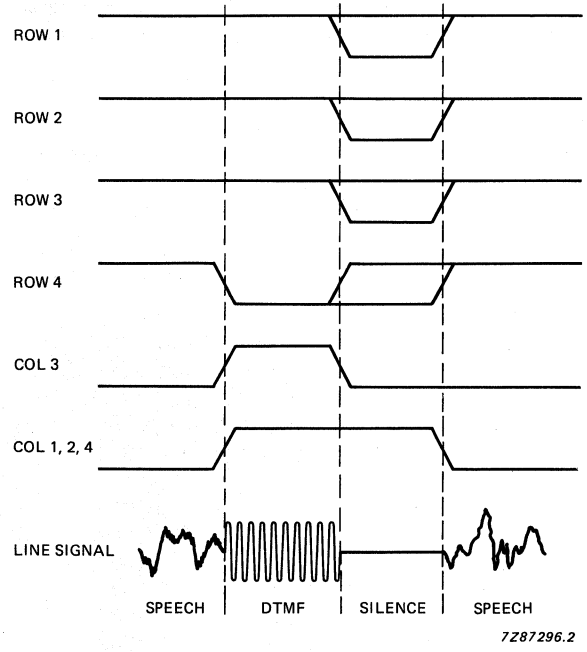


Fig. 10 Waveform tones 697/1336 Hz (dialling number 2).

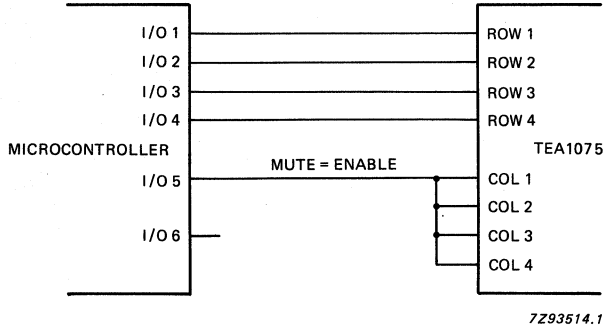


Fig. 11 Microcontroller mode; all column inputs interconnected.

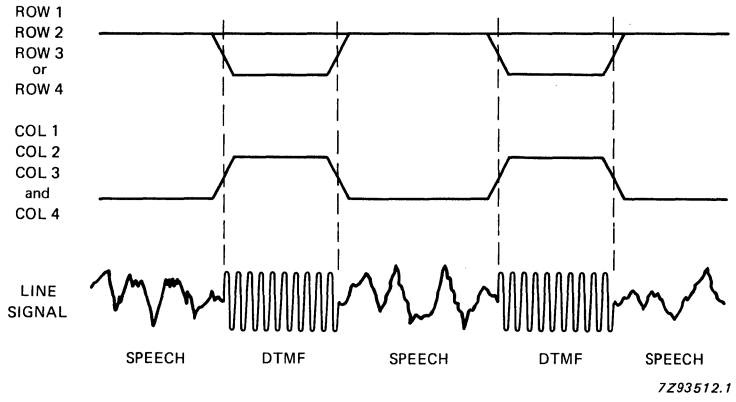


Fig. 12 Tone/speech waveform in application diagram Fig. 11.

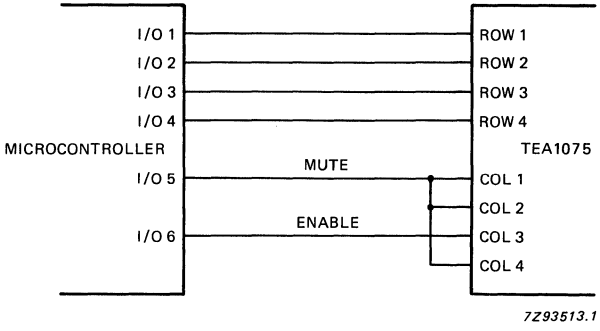


Fig. 13 Microcontroller mode; column inputs COL 1, 2 and 4 interconnected.

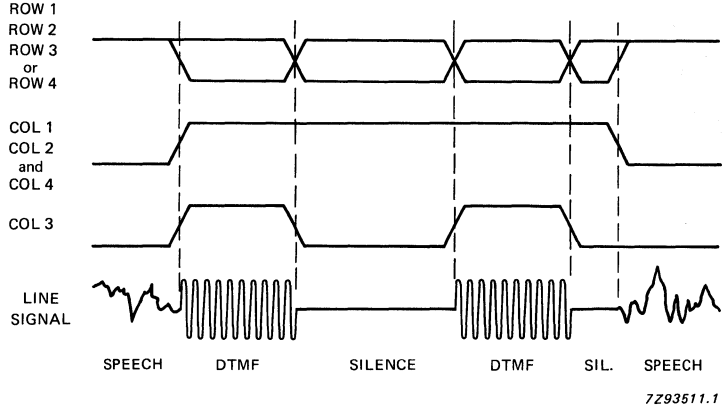


Fig. 14 Tone/speech waveform in application diagram Fig. 13.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply current	I_P	max.	150	mA
Surge current ($t_p < 250\ \mu s$)	I_S	max.	1000	mA
Input voltage (any pin)	V_I		$(V_N - 0{,}5)$ to $(V_L + 0{,}5)$	V
D.C. line voltage	V_L	max.	10	V
Total power dissipation				
TEA1075P	P_{tot}	max.	750	mW
TEA1075T	P_{tot}	max.	450	mW
Storage temperature range	T_{stg}		−55 to +125	°C
Operating ambient temperature range	T_{amb}		−25 to +70	°C
Junction temperature	T_j	max.	125	°C

DEVELOPMENT DATA

CHARACTERISTICS

I_L = 15 mA; f = 1 kHz; T_{amb} = 25 °C unless otherwise specified. Measured in Fig. 15.

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Dial mode						
D.C. line voltage						
	I_L = 15 mA	V_L	3,0	3,3	3,6	V
	I_L = 50 mA	V_L	3,2	3,7	4,2	V
	I_L = 90 mA	V_L	3,6	4,2	4,9	V
	I_L = 120 mA	V_L	4,2	4,7	5,4	V
Temperature coefficient over temperature range	–	TC	–	–8	–	mV/K
Line current range						
TEA1075P	–	I_L	10	–	120	mA
TEA1075T	–	I_L	10	–	90	mA
Stand-by mode						
Standby current						
	V_L = 4,5 V	I_{LS}	–	3,2	4,0	mA
	V_L = 6,0 V	I_{LS}	–	6,7	–	mA
D.C. line voltage						
	I_L = 15 mA	V_L	–	6,4	–	V
	I_L = 70 mA	V_L	–	7,4	–	V
Temperature coefficient over temperature range	–	TC	–	19	–	mV/K
Mute switch (no key pressed)						
Mute output sink current						
TEA1075P	–	I_{MS}	–	–	120	mA
TEA1075T	–	I_{MS}	–	–	90	mA
Saturation voltage						
	I_{MS} = 15 mA; V_L = 4,5 V	V_{MT}	–	65	100	mV
	I_{MS} = 75 mA; V_L = 4,5 V	V_{MT}	–	320	500	mV
Balance return loss from 300 to 3400 Hz Speech part: 600 Ω	V_L = 4,5 V	BRLS	20	–	–	dB
	V_L = 6,0 V	BRLS	18	–	–	dB
Switch delay after key release	–	t_{dr}	–	–	10	μs

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Transmitter output stage						
Dynamic resistance setting range	pin 6 open	R_i	–	900	–	Ω
	pin 6 to V_N	R_i	–	600	–	Ω
Variation of output impedance over the line current range						
	R_i = 600 Ω	ΔZ_O	–	100	–	Ω
	R_i = 900 Ω	ΔZ_O	–	200	–	Ω
Balance return loss from 300 to 3400 Hz	R_i = 600 Ω	BRL	20	–	–	dB
Total harmonic distortion with respect to total output level	–	THD	–	–40	–	dB
DTMF generator						
Tone frequencies						
low tones (row inputs)	–		697, 770, 852, 941			Hz
high tones (column inputs)	–		1209, 1336, 1477, 1633			Hz
Crystal frequency dividing error	f = 3,579545 MHz	Δf_d	–0,1	–	–0,31	%
Tone output level (adjustable) low tones						
	$I_L > 10$ mA	V_{LG}	–11	–	–8	dBm
	$I_L > 12$ mA	V_{LG}	–11	–	–6	dBm
high tones						
	$I_L > 10$ mA	V_{HG}	–9	–	–6	dBm
	$I_L > 12$ mA	V_{HG}	–9	–	–4	dBm
Variation of output voltage level as a function of temperature and line current range	–	ΔV_O	–2	–	+ 2	dB
Pre-emphasis high/low tones as a function of temperature and line current range	–	$V_{HG}-V_{LG}$	1	2	3	dB
Tone delay after key depressed	–	t_{td}	–	–	5	ms
Debounce time	–	t_d	–	2	–	ms

parameter	conditions	symbol	min.	typ.	max.	unit
Keyboard inputs						
Keyboard ON resistance	–	$R_{K\,ON}$	–	–	10	kΩ
Keyboard OFF resistance	–	$R_{K\,OFF}$	300	–	–	kΩ
Low frequency inputs (ROW 1, 2, 3, 4)						
input voltage LOW	–	V_{IL}	–	–	1,1	V
input voltage HIGH	–	V_{IH}	1,5	–	–	V
d.c. input current	V_{IL} dial mode	I_{ILD}	–	30	–	μA
High frequency inputs (COL 1, 2, 3, 4)						
input voltage LOW	–	V_{IL}	–	–	0,5	V
input voltage HIGH	–	V_{IH}	0,9	–	–	V
d.c. input current	V_{IH} dial mode	I_{IHD}	–	50	–	μA

DEVELOPMENT DATA

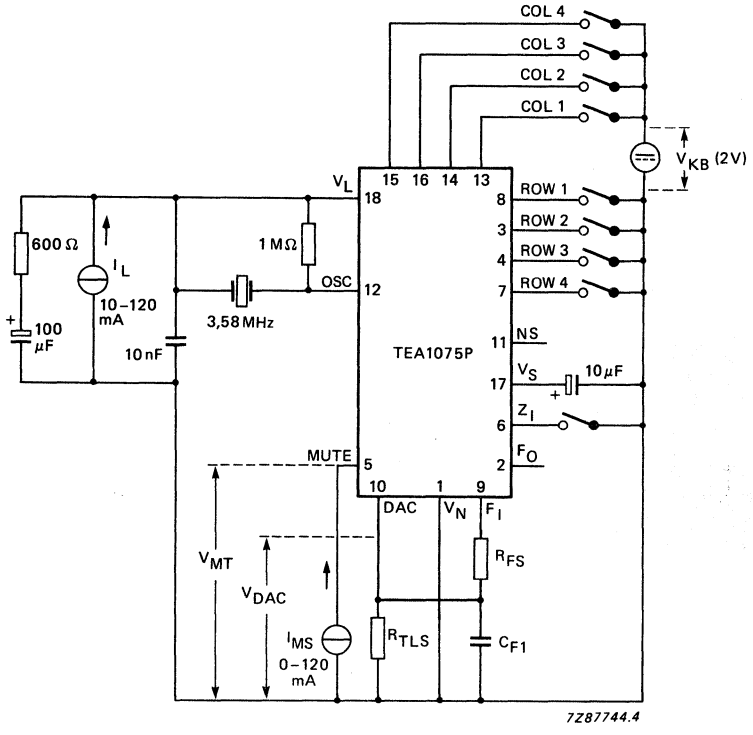
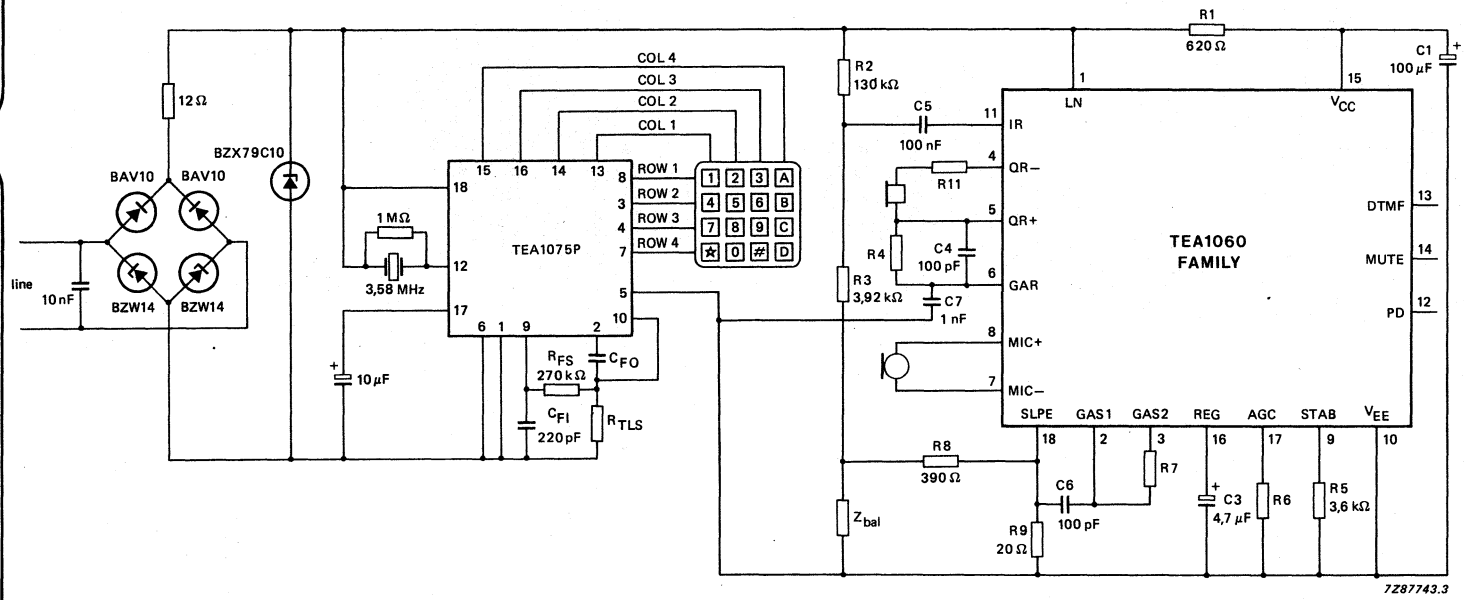


Fig. 15 Test circuit.

APPLICATION INFORMATION



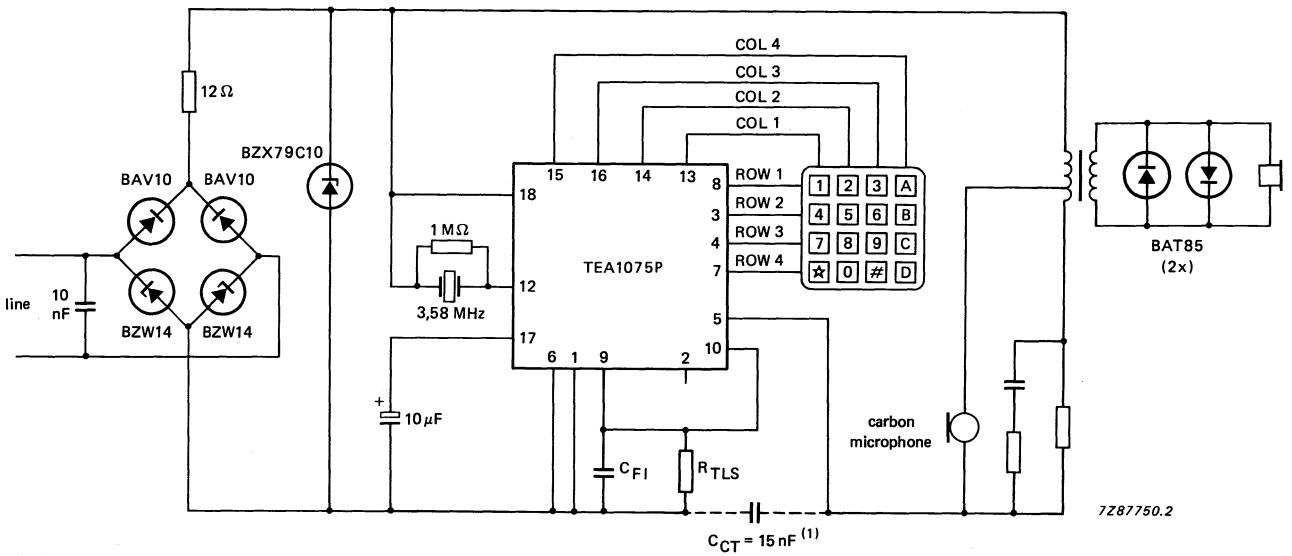
Note

Fig. 16 is an application diagram of a complete DTMF telephone set incorporating an IC of the TEA1060 family (electronic speech/transmission circuit) and the TEA1075P both set to an impedance of 600 Ω. The TEA1075 P is using a second-order filter for low harmonic distortion (CEPT T/CS 34-08). Dial and speech functions are completely separate allowing line adaption to be carried out by either the TEA1075P or the IC of TEA1060 family.

Start and stop currents of the TEA1060 family gain control function are changed when the current through the TEA1075P is increased at maximum I_L and T_{amb}.

Both application diagrams (Figs 16 and 17) include protection circuitry.

Fig. 16 DTMF telephone set with TEA1075P using a second-order filter and an electronic speech/transmission circuit.



(1) Capacitor C_{CT} is connected only when the confidence tone is required.

Fig. 17 DTMF telephone set with TEA1075P using a single pole filter and a classical hybrid transformer as the transmission part.

SUPPLY CIRCUIT FOR TELEPHONE SET PERIPHERALS

GENERAL DESCRIPTION

The TEA1080 is a bipolar integrated circuit intended for use in line powered telephone sets to supply peripheral circuits for extended dialling and/or loudspeaking facilities.

The IC uses a part of the surplus of the line current normally sinked in the voltage regulator of the applied speech/transmission circuit.

Features

- High input impedance for audio signals
- High output current
- Large audio signal handling
- Low distortion
- Two modes of operation:
  - regulated output voltage
  - constant d.c. voltage drop in series with a resistor between line and output terminal
- Low number of external components

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
D.C. line voltage		V_{LN}	2,5	–	10	V
D.C. output voltage		V_O	2,0	–	9,5	V
Voltage drop line/output		$V_{LN} - V_O$	0,5	–	–	V
Series resistance		$R_{1\text{-}8}$	–	18	–	Ω
Output current	V_{LN} = 4 V, TEA1080P	I_O	–	–	30	mA
Output current	V_{LN} = 4 V, TEA1080T	I_O	–	–	20	mA
A.C. line voltage	V_{LN} = 4,5 V; I_O = 15 mA; d = 2%	$v_{LN(rms)}$	–	1,5	–	V
Internal supply current		I_{INT}	–	–	1	mA
Operating ambient temperature range		T_{amb}	–25	–	+ 70	°C

PACKAGE OUTLINES

TEA1080P: 8-lead dual in-line; plastic (SOT-97AE).
TEA1080T: 8-lead mini-pack; plastic (SO-8; SOT-96A).

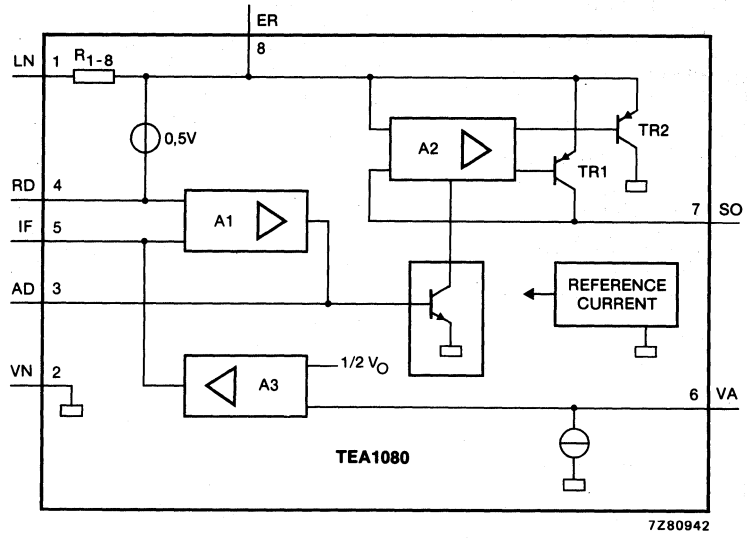


Fig. 1 Block diagram.

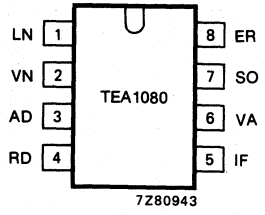


Fig. 2 Pinning diagram.

PINNING

1	LN	positive line terminal
2	VN	negative line terminal
3	AD	amplifier decoupling
4	RD	regulator input
5	IF	input low-pass filter
6	VA	output voltage adjustment
7	SO	supply output
8	ER	supply terminal of the internal circuit

FUNCTIONAL DESCRIPTION

The TEA1080 is the interface between the telephone line and the peripheral devices, which have to be supplied. The circuit can be connected directly to the telephone line (via the diode bridge) because of its high input impedance. An inductor function is obtained by amplifier A1, resistor $R_{1\text{-}8}$ (Fig. 1) and external low-pass RC filter.

Amplifier A2 controls both transistors TR1 and TR2. To avoid a large increase of the distortion the input current will flow to ground (via TR2) during the time that the momentary line voltage drops below the output voltage.

The internal circuitry is biased by a temperature and line voltage compensated reference current source.

Supply LN and VN (pins 1 and 2)

The input terminals LN and VN can be connected directly to the line. The minimum required d.c. line voltage at the input is given by:

$$V_{LN\,min} = I_1 \times R_{1\text{-}8} + v_{LN\,min} + v_{LN(P)} \quad (V)$$

in which:

I_1 = input current
$R_{1\text{-}8}$ = internal series resistance
$v_{LN\,min}$ = minimum level of a.c. line voltage (1,8 V at I_O = 5 mA)
$v_{LN(P)}$ = required peak level of a.c. line voltage

The internal current (I_{INT}) consumption is typical 0,7 mA at I_O = 0 mA and V_{LN} = 5 V and will be maximum 1 mA at V_{LN} = 10 V.

Output voltage SO and VA (pins 7 and 6)

The output SO (pin 7) supplies the peripheral circuits. The circuit includes two modes for regulation of the output voltage:

without external resistor R_V (see Figs 3 and 17)

the output voltage is expressed by

$$V_O = V_{LN} - (I_1 \times R_{1\text{-}8} + 0{,}5) \quad (V)$$

in which:

V_{LN} = line voltage
I_1 = input current
$R_{1\text{-}8}$ = internal series resistance (typ. 18 Ω)

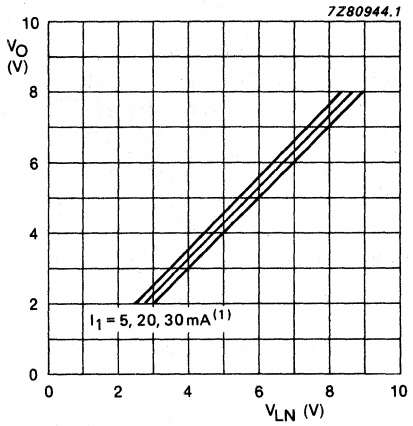
with external resistor R_V, connected between SO and VA (see Figs 4 and 17), the output voltage will be regulated at a constant level of

$$V_O = 2 \times I_6 \times R_V \quad (V)$$

as soon as the line voltage $V_{LN} > 2 \cdot I_6 \cdot R_V + I_1 \cdot R_{1\text{-}8} + 0{,}5$ (V)

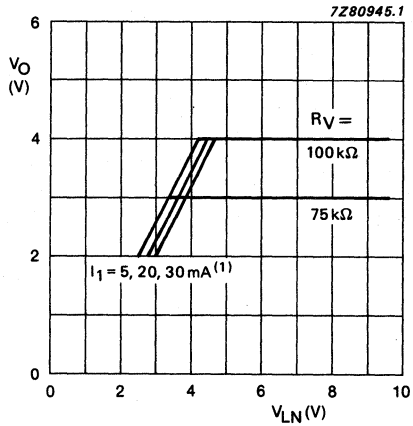
The control current I_6 is typical 20 μA.

DEVELOPMENT DATA



(1) I_1 = 30 mA is only valid for TEA1080P

Fig. 3 Output voltage versus line voltage for application without R_V.



(1) I_1 = 30 mA is only valid for TEA1080P

Fig. 4 Output voltage versus line voltage (R_V = 75 or 100 kΩ).

Input current I_1 and output I_O

The minimum line current (I_{SET}), available for the telephone set must be sufficient to cover the specified minimum line current ($I_{LN\,min}$) of the speech/transmission IC and the maximum input current ($I_{1\,max}$) required by the application of the TEA1080. $I_{SET} = I_{LN\,min} + I_{1\,max}$.

At $v_{LN(rms)} < 150$ mV the input current I_1 can be approximated by:

$$I_1 = I_{INT} + k \cdot I_O \quad \text{(mA)}$$

in which:

I_{INT} = internal supply current (0,7 mA at V_{LN} = 5 V)
k = correction factor which depends on the output current
  k = 1,04 for I_O = 1 mA
  k = 1,08 for I_O = 20 mA
  k = 1,12 for I_O = 30 mA

For large line signals the a.c. line voltage may drop below V_O + 0,4 V. The instantaneous current flows from LN to SO (pin 1 to pin 7) into the output load during the time $V_{LN} > V_O$ + 0,4 V and will be internally rerouted to VN (pin 2) during the time $V_{LN} < V_O$ + 0,4 V in order to prevent distortion of the line signal.

The input current for $V_{LN(rms)}$ = 1 V and without R_V can be approximated by:

$$I_1 = I_{INT} + 2 \cdot k \cdot I_O \quad \text{(mA)}$$

If R_V is not applied the ratio between input current I_1 and output current I_O is shown in Fig. 7 for different line signal levels.

When R_V is applied the ratio I_1/I_O is given in Fig. 8 for V_{LN} = 4 V and in Fig. 9 for V_{LN} = 5 V.

Input impedance IF (pin 5)

The equivalent circuit diagram for small a.c. signals is shown in Fig. 5. The input impedance is mainly determined by the negative input impedance Z_I which is 10 kΩ in parallel with L1.

$L_I = C_L \cdot R_L \cdot R_{1\text{-}8} = 10$ H if $C_L = 4{,}7\ \mu$F, $R_L = 100$ kΩ and $R_{1\text{-}8} = 18\ \Omega$.

The filter elements C_L and R_L are connected to pin 1 (LN) and pin 5 (IF) respectively to pin 5 (IF) and pin 7 (SO). See Figs 15, 16 and 17.

The absolute value of the input impedance for audio frequencies is more than 8 kΩ with $L_I = 10$ H.

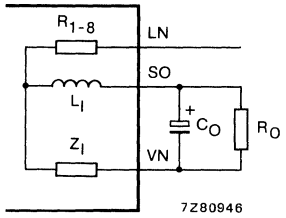


Fig. 5 Equivalent circuit diagram for small signals.

Decoupling ER and AD (See Fig. 15)

An external capacitor $C_r = 27$ pF between ER (pin 8) and AD (pin 3) is required to ensure stability. Capacitor C_d (68 pF) between AD (pin 3) and VN (pin 2) limits the distortion at high output currents and high line levels.

A.C. behaviour

R_V not applied

The voltage drop V_{LN}-V_O between LN (pin 1) and SO (pin 7) as a function of a.c. line signal for different output currents is given in Fig. 10, while Fig. 11 presents the a.c. line voltage for 2% distortion as a function of the output current for some d.c. line voltages.

R_V connected (75 kΩ)

Figures 12 and 13 show the decrease of the output voltage, relative to V_O at $I_O = 0$ as a function of the a.c. line signal if the d.c. output voltage is 3 V and if the d.c. line voltage is 4 respectively 5 volt. The a.c. line signal for 2% distortion as a function of the output current is shown in Fig. 14.

DEVELOPMENT DATA

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	typ.	max.	unit
Positive d.c. line voltage	V_{LN}	–	–	10	V
Voltage on all other terminals	V	V_{VN}–0,5	–	V_{LN}+0,5	V
Input current (d.c.)					
TEA1080P	I_1	–	–	120	mA
TEA1080T	I_1	–	–	80	mA
Current into terminals					
IF, VA, RD and AD	$I_{5,6,4,3}$	–1	–	+ 1	mA
Total power dissipation	P_{tot}	see derating curve Fig. 6			
Storage temperature range	T_{stg}	–40	–	+ 125	°C
Operating ambient temperature range	T_{amb}	–25	–	+ 70	°C
Junction temperature	T_j	–	–	+ 125	°C

THERMAL RESISTANCE

From junction to ambient in free air					
TEA1080P	$R_{th\ j\text{-}a}$	=		120	K/W
TEA1080T (mounted on printed circuit board; 50 x 50 x 1,5 mm)	$R_{th\ j\text{-}a}$	=		260	K/W

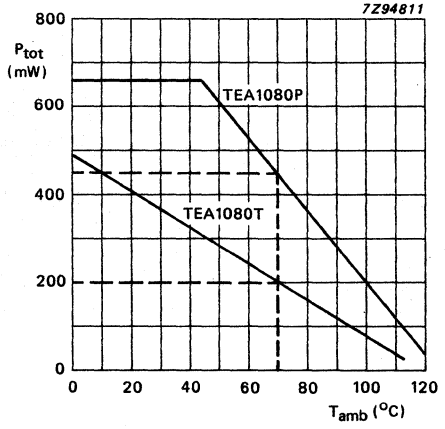


Fig. 6 Power derating curve.

DEVELOPMENT DATA

CHARACTERISTICS

V_{LN} = 5 V; $v_{LN(rms)}$ = 100 mV; I_O = 5 mA; f = 1 kHz; R_L = 100 kΩ; R_V = 75 kΩ; C_L = 4,7 μF; T_{amb} = 25 °C, unless otherwise specified (see Figs 15 and 16)

parameter	conditions	symbol	min.	typ.	max.	unit
Operating d.c. line voltage		V_{LN}	2,5	–	10	V
Momentary line voltage		V_{LN}	1,8	–	10	V
R_V = 75 kΩ						
Input current	v_{LN} = 0 V	I_1	–	5,7	–	mA
	$v_{LN(rms)}$ = 100 mV	I_1	–	5,7	–	mA
	$v_{LN(rms)}$ = 1,5 V	I_1	–	7,5	–	mA
	$v_{LN(rms)}$ = 1,5 V; I_O = 15 mA	I_1	–	24	–	mA
Output voltage		V_O	–	3	–	V
Voltage variation with temperature	TEA1080P	$\Delta V_O/\Delta T$	–	0,2	–	mV/K
Voltage variation with temperature	TEA1080T	$\Delta V_O/\Delta T$	–	1	–	mV/K
Variation over output current and line voltage range		ΔV_O	–	#	–	mV
Control current		I_6	–	20	–	μA
R_V not applied						
Input current	v_{LN} = 0	I_1	–	5,7	–	mA
	$v_{LN(rms)}$ = 100 mV	I_1	–	6	–	mA
	$v_{LN(rms)}$ = 1,5 V	I_1	–	11	–	mA
	$v_{LN(rms)}$ = 1,5 V; I_O = 15 mA	I_1	–	33	–	mA
Voltage drop		V_{LN}-V_O	–	0,6	–	V
Output current	TEA1080P	I_O	–	–	30	mA
Output current	TEA1080T	I_O	–	–	20	mA
Internal series resistance		R_{1-8}	–	18	–	Ω
Input impedance		$\|Z_I\|$	8	–	–	kΩ
Internal supply current	I_O = 0 mA	I_{INT}	–	0,7	–	mA
A.C. line voltage	d < 2%; V_{LN} = 4 V	$V_{LN(rms)}$	–	1,5	–	V
Noise on voltage output	v_{LN} = 0 mV; R_L = 600 Ω; P53 curve	$v_{no(rms)}$	–	#	–	dBmp
Start time		t_{st}	–	#	–	ms

Value not available.

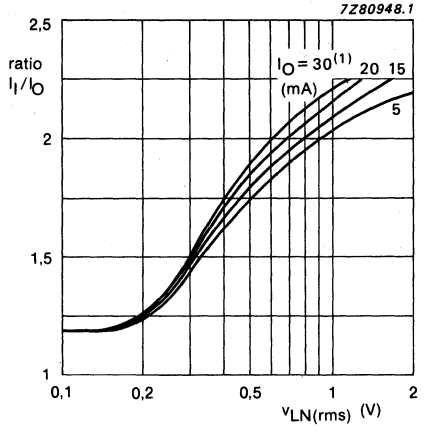


Fig. 7 Ratio of input and output current as a function of a.c. line voltage. R_V is not applied.

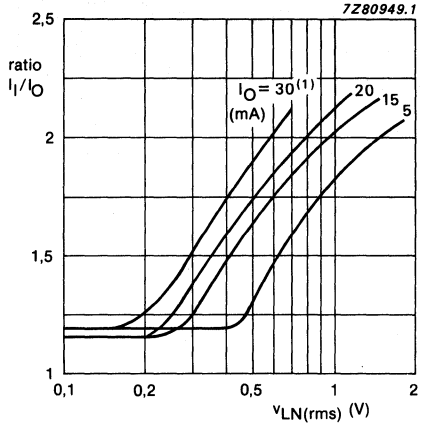


Fig. 8 Ratio of input and output current as a function of a.c. line voltage. R_V = 75 kΩ, V_{LN} = 4 V, V_O = 3 V.

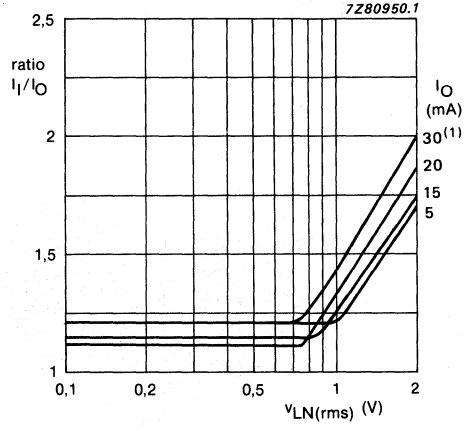


Fig. 9 Ratio of input and output current as a function of a.c. line voltage. R_V = 75 kΩ, V_{LN} = 5 V, V_O = 3 V.

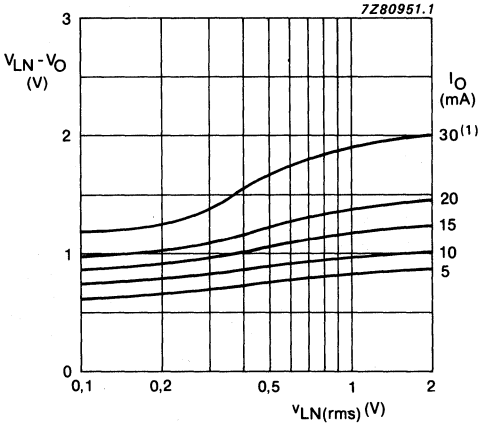


Fig. 10 Voltage drop between input and output voltage as a function of a.c. line voltage. R_V is not applied.

(1) I_O = 30 mA is only valid for TEA1080P, $I_{O\,max}$ = 20 mA for TEA1080T.

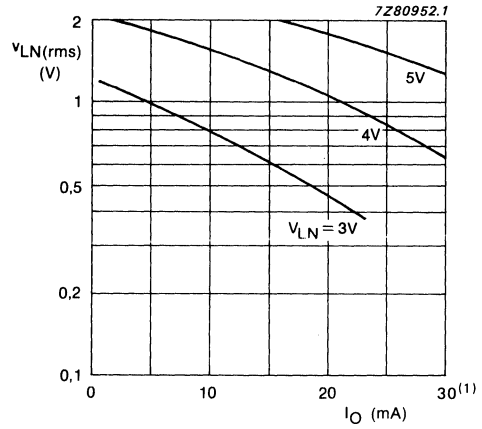


Fig. 11 A.C. line voltage as a function of output current.
d_{tot} = 2%; R_V not applied.

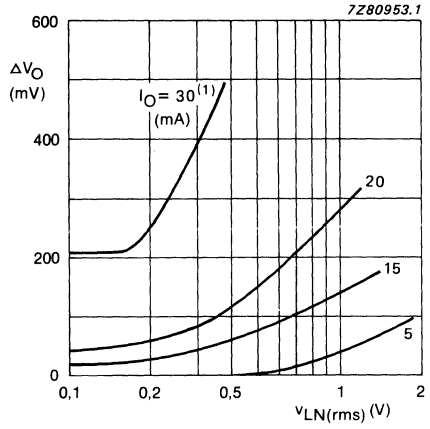


Fig. 12 Output voltage drop as a function of a.c. line voltage.
R_V = 75 kΩ, V_{LN} = 4 V, V_O = 3 V.

DEVELOPMENT DATA

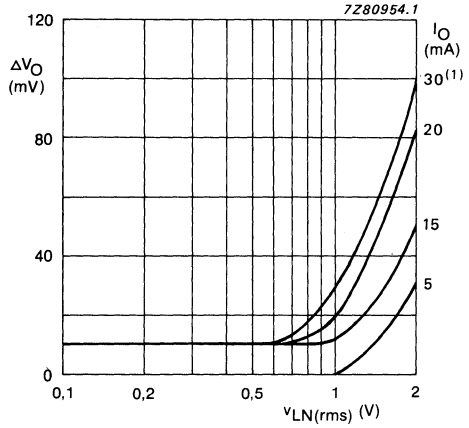


Fig. 13 Output voltage drop as a function of a.c. line voltage.
R_V = 75 kΩ, V_{LN} = 5 V, V_O = 3 V.

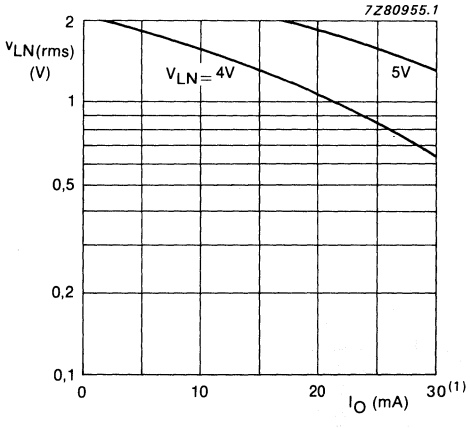


Fig. 14 A.C. line voltage as a function of output current at d_{tot} = 2%.
R_V = 75 kΩ and V_O = 3 V.

(1) I_O = 30 mA is only valid for TEA1080P, $I_{O\,max}$ = 20 mA for TEA1080T.

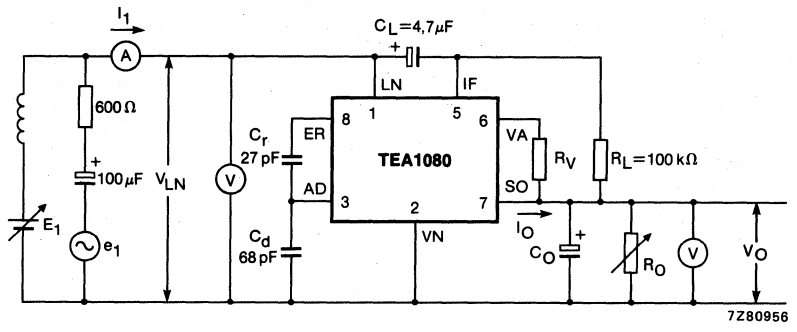


Fig. 15 Test circuit diagram d.c. characteristics. V_O versus V_{LN} (with and without R_V), a.c. line voltage = v_{LN}, internal supply current = I_{INT}, noise output voltage = v_{no}.

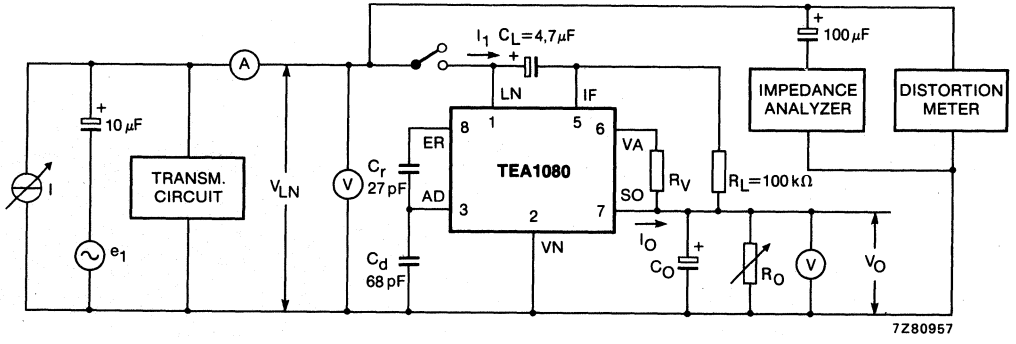


Fig. 16 Test circuit diagram a.c. characteristics. I_1 versus v_{LN} (for different I_O), input impedance = Z_I, line distortion versus v_{LN} and I_O, start time = t_{st}.

APPLICATION INFORMATION

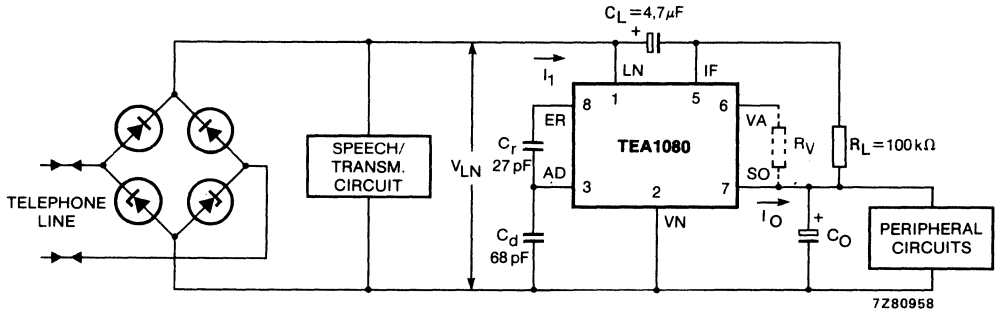


Fig. 17 Application circuit diagram.

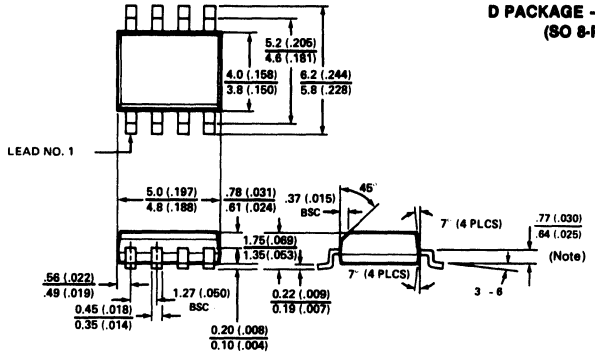
DEVELOPMENT DATA

PACKAGE INFORMATION

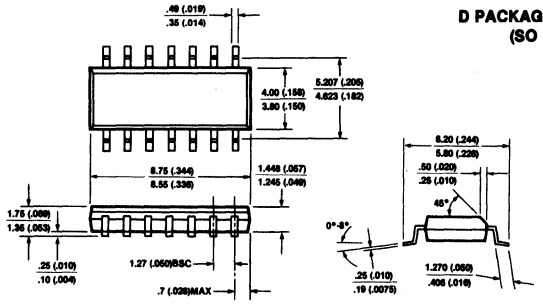
Package outlines

Soldering

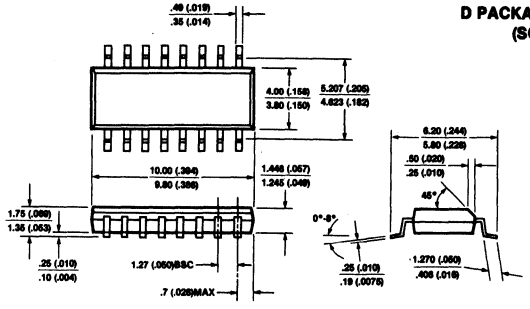
**D PACKAGE — PLASTIC
(SO 8-PIN)**



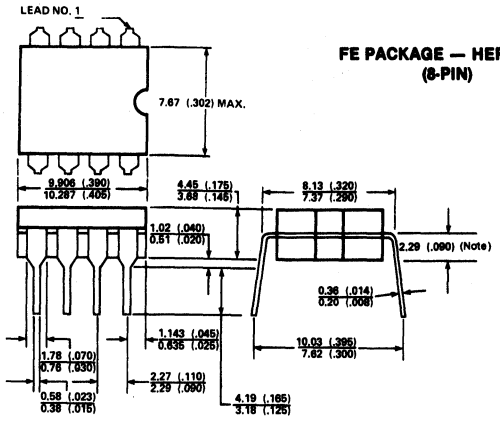
**D PACKAGE — PLASTIC
(SO 14-PIN)**



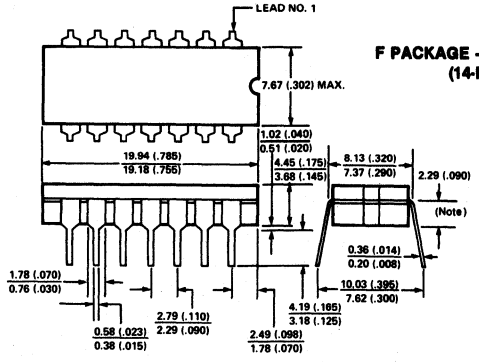
**D PACKAGE — PLASTIC
(SO 16-PIN)**



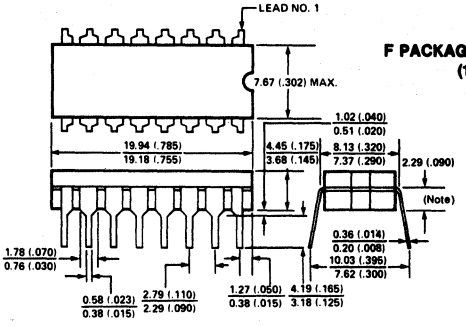
Note:
Dimensions shown are metric units (millimeters), except those in parentheses which are English units (inches).



FE PACKAGE — HERMETIC (8-PIN)



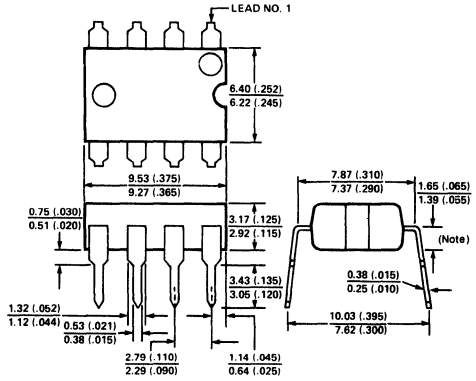
F PACKAGE — HERMETIC (14-PIN)



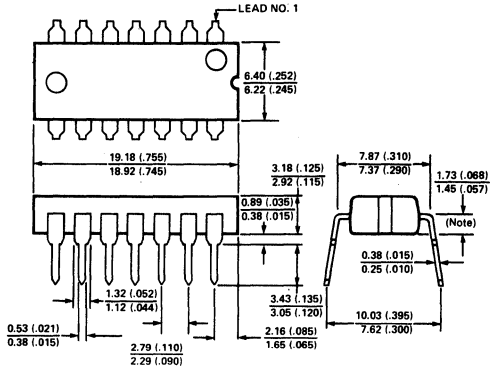
F PACKAGE — HERMETIC (16-PIN)

Note:
Dimensions shown are metric units (millimeters), except those in parentheses which are English units (inches).

N PACKAGE — PLASTIC
(8-PIN)

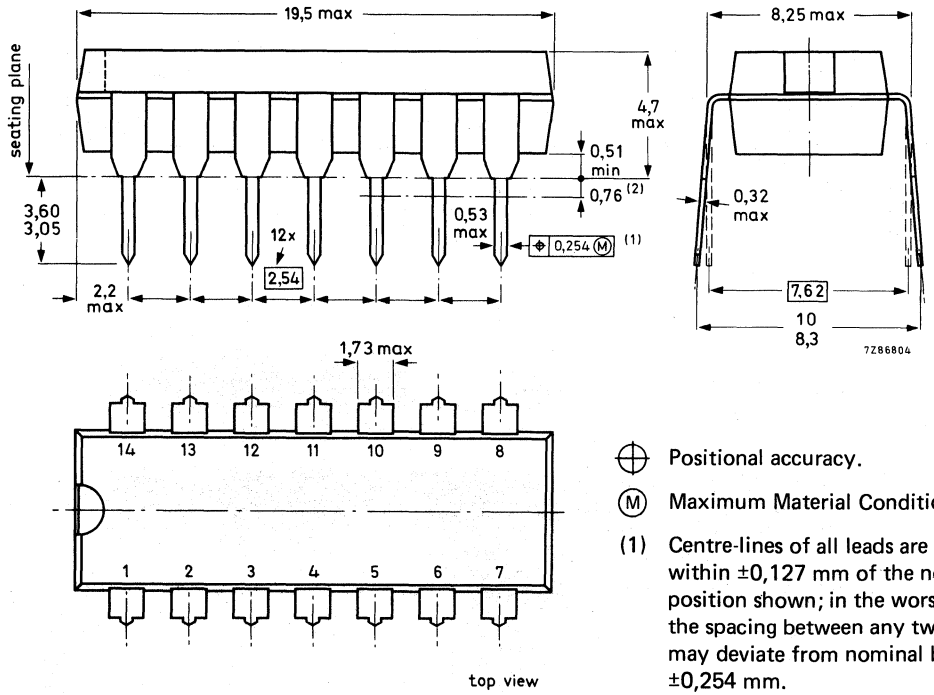


N PACKAGE — PLASTIC
(14-PIN)



Note:
Dimensions shown are metric units (millimeters), except those in parentheses which are English units (inches).

14-LEAD DUAL IN-LINE; PLASTIC (SOT-27KE, ME, MF)



⊕ Positional accuracy.

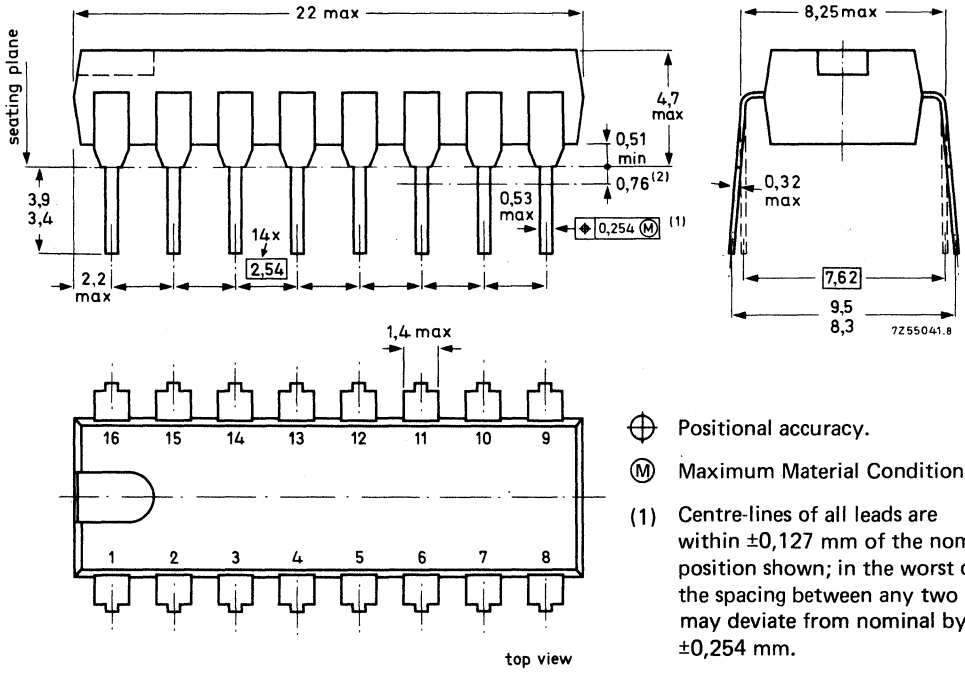
Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

Dimensions in mm

16-LEAD DUAL IN-LINE; PLASTIC (SOT-38)



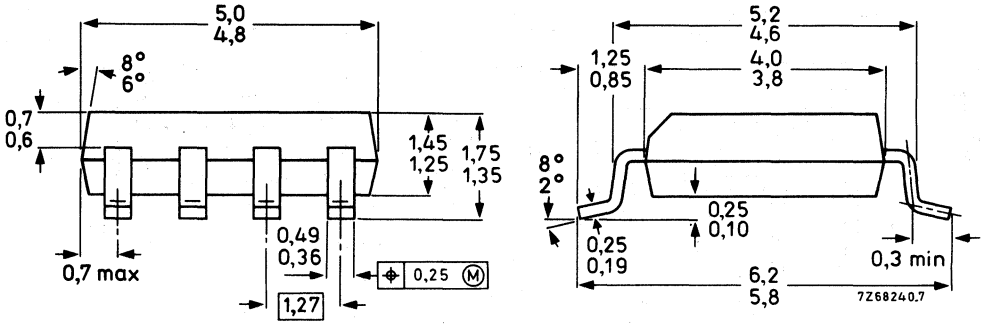
⊕ Positional accuracy.

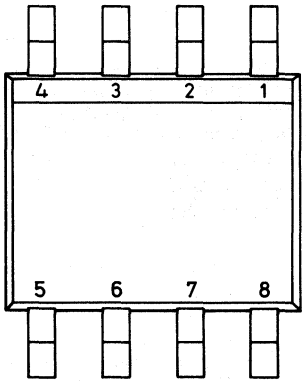
Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

8-LEAD MINI-PACK; PLASTIC (SO-8; SOT-96A)





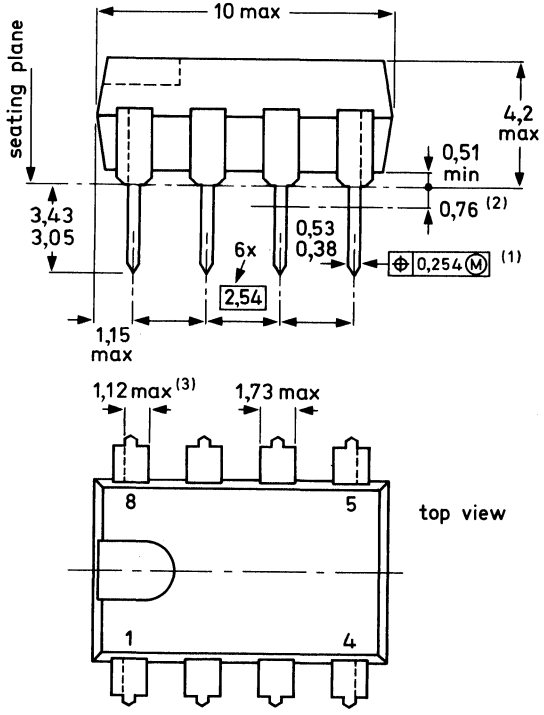
top view

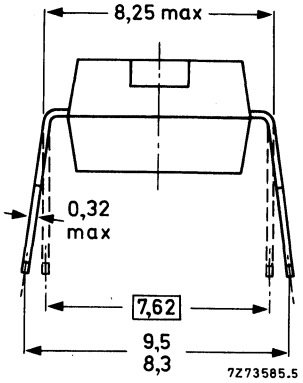
Dimensions in mm

⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

8-LEAD DUAL IN-LINE; PLASTIC (SOT-97AE, DE, EE)





Dimensions in mm

⊕ Positional accuracy.

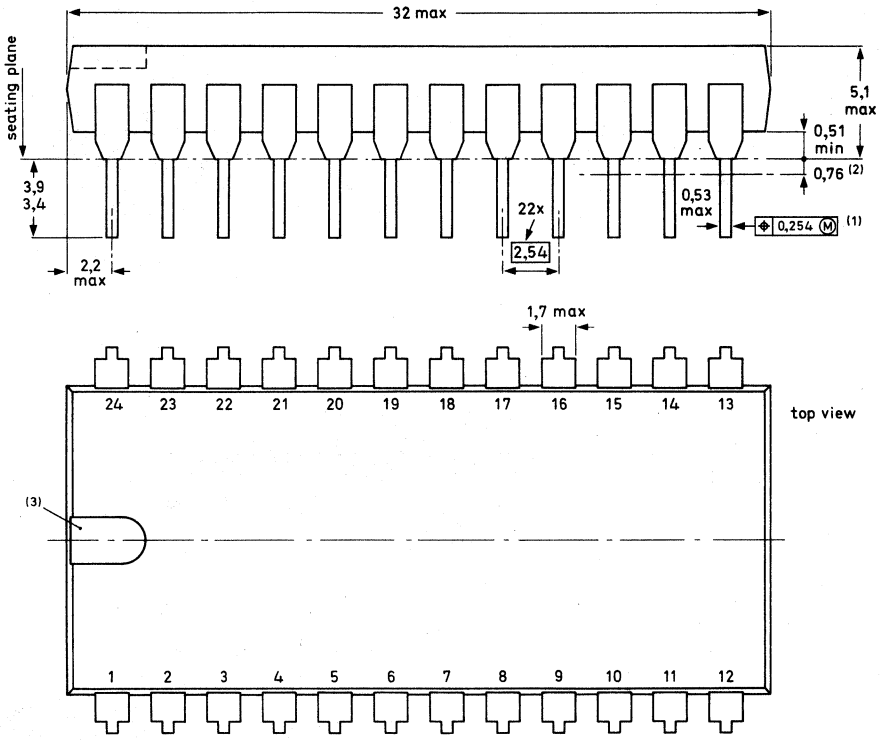
Ⓜ Maximum Material Condition.

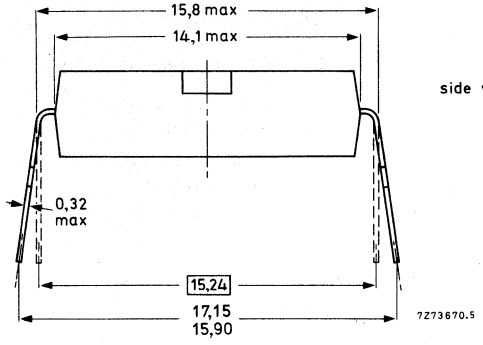
(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

(3) Only for devices with asymmetrical end-leads.

24-LEAD DUAL IN-LINE; PLASTIC (SOT-101A, B, F, G, L)





⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

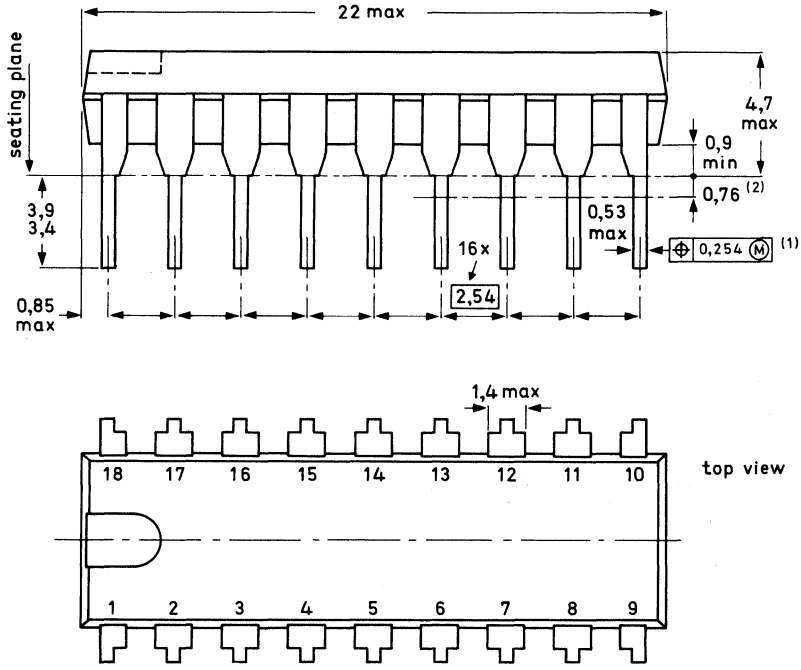
(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

(3) Index may be horizontal as shown, or vertical.

Dimensions in mm

18-LEAD DUAL IN-LINE; PLASTIC (SOT-102HE, HG, KE, ME, PG)



⊕ Positional accuracy.

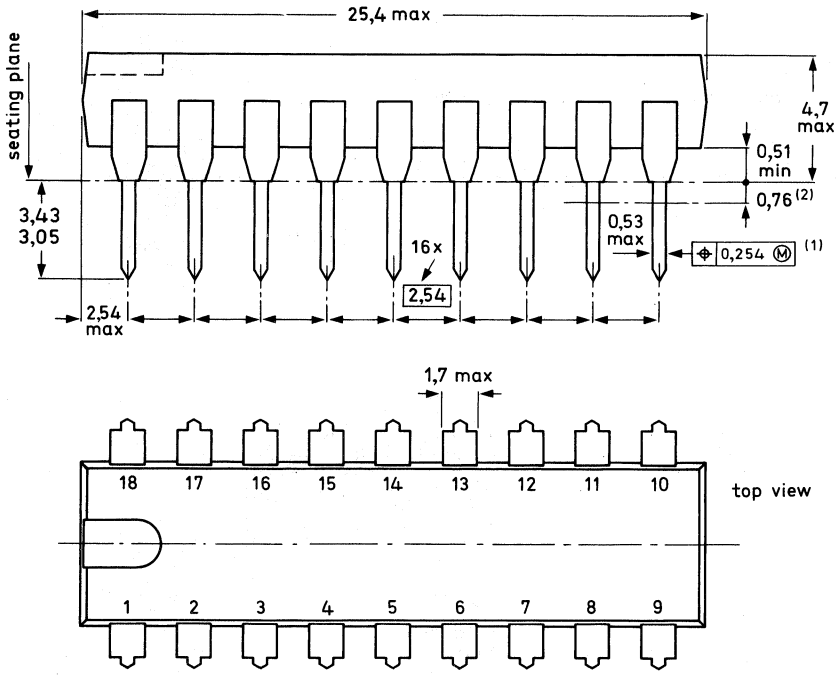
Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

Dimensions in mm

18-LEAD DUAL IN-LINE; PLASTIC (SOT-102NE, GE, PE)



⊕ Positional accuracy.

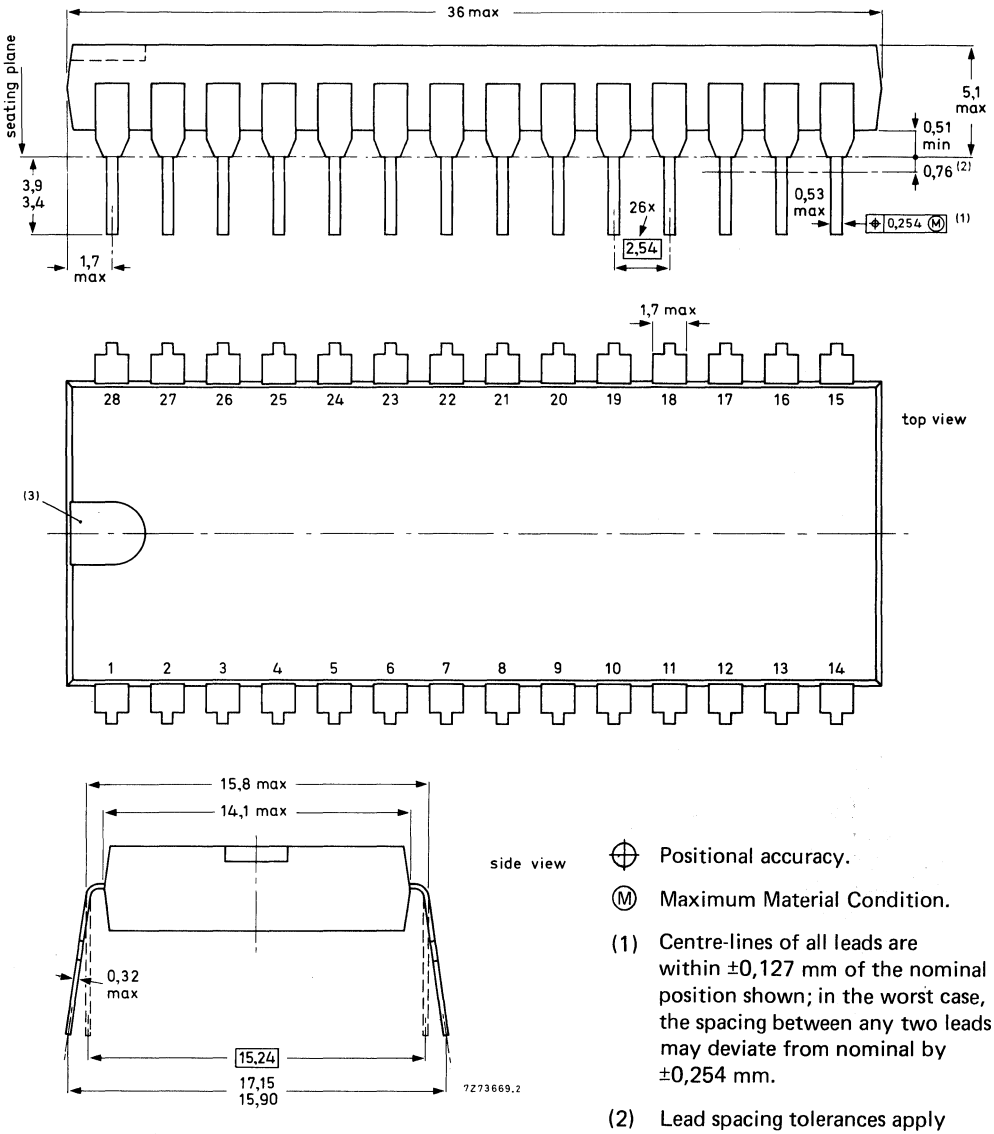
Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

Dimensions in mm

28-LEAD DUAL IN-LINE; PLASTIC (SOT-117)



⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

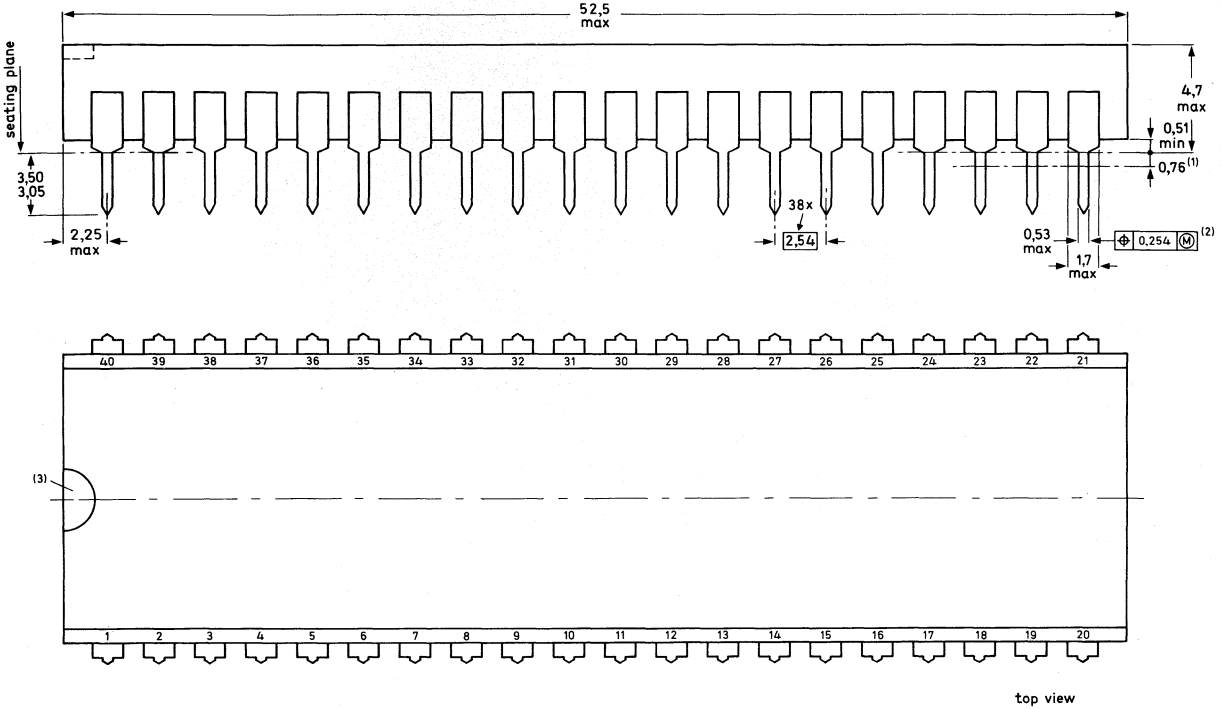
(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

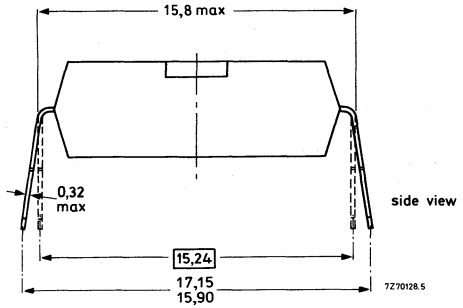
(2) Lead spacing tolerances apply from seating plane to the line indicated.

(3) Index may be horizontal as shown, or vertical.

Dimensions in mm

40-LEAD DUAL IN-LINE; PLASTIC (SOT-129)





⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

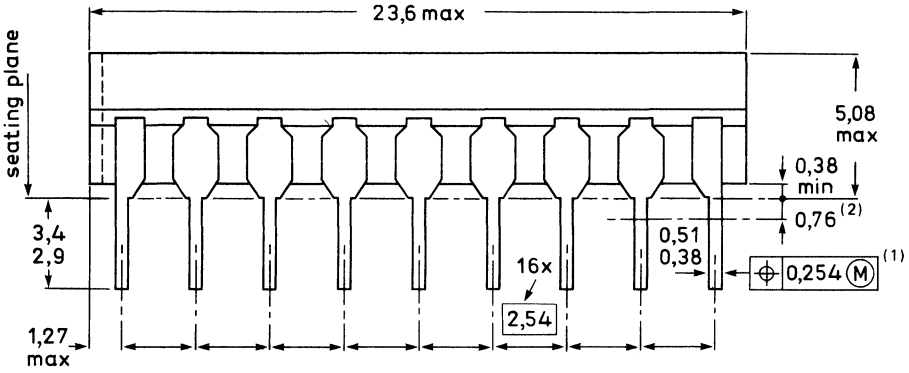
(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

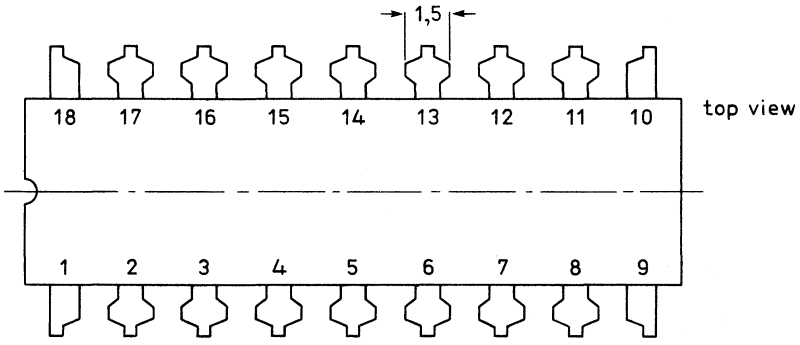
(2) Lead spacing tolerances apply from seating plane to the line indicated.

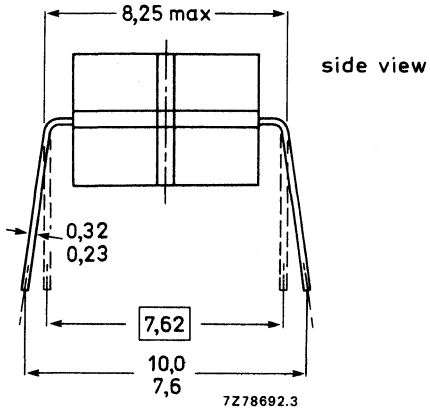
(3) Index may be horizontal as shown, or vertical.

Dimensions in mm

18-LEAD DUAL IN-LINE; CERAMIC (CERDIP) (SOT-133B)







⊕ Positional accuracy.

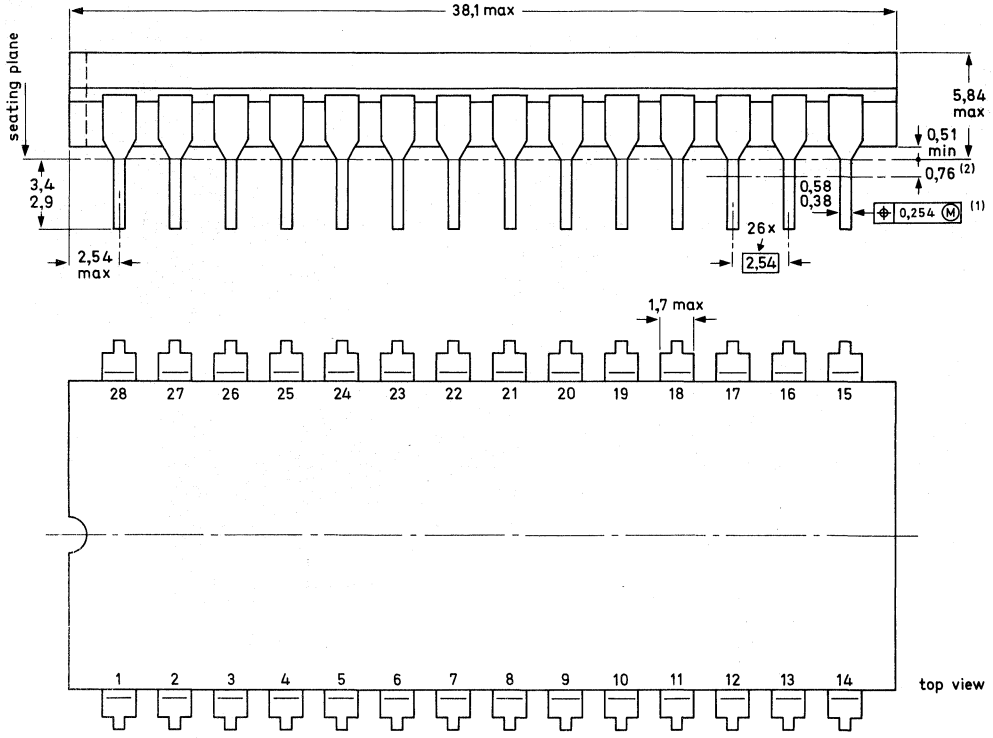
Ⓜ Maximum Material Condition.

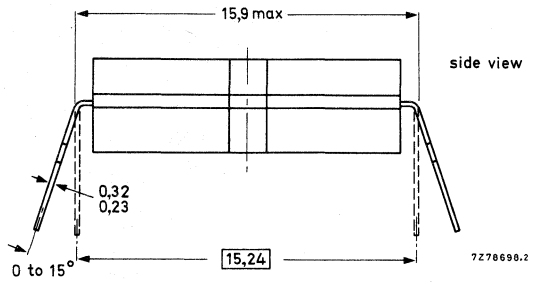
(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

Dimensions in mm

28-LEAD DUAL IN-LINE; CERAMIC (CERDIP) (SOT-135A)





⊕ Positional accuracy.

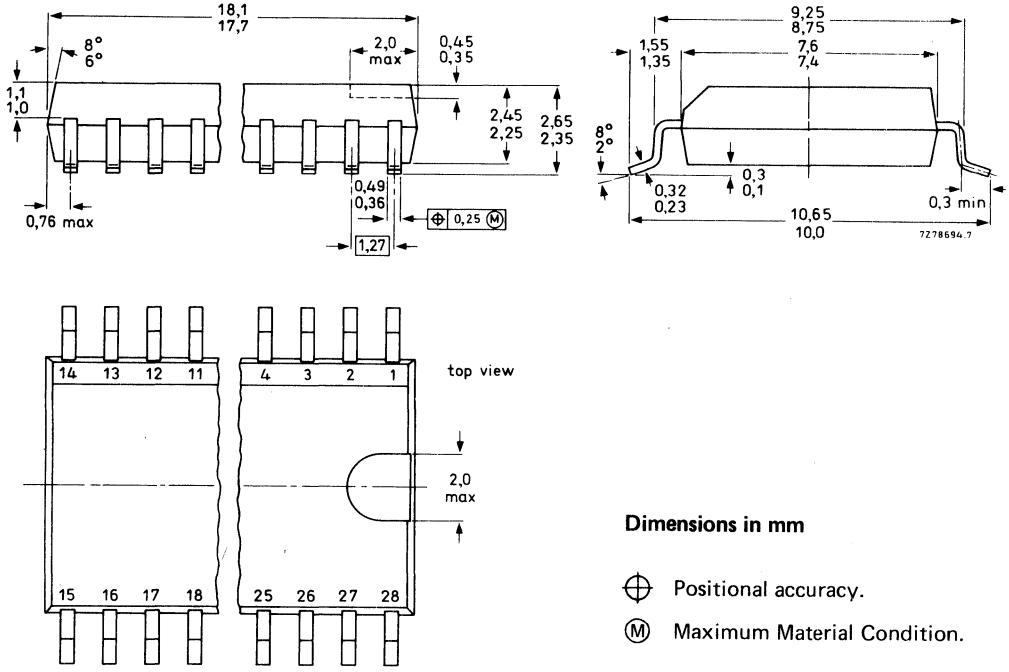
Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

Dimensions in mm

28-LEAD MINI-PACK; PLASTIC (SO-28; SOT-136A)

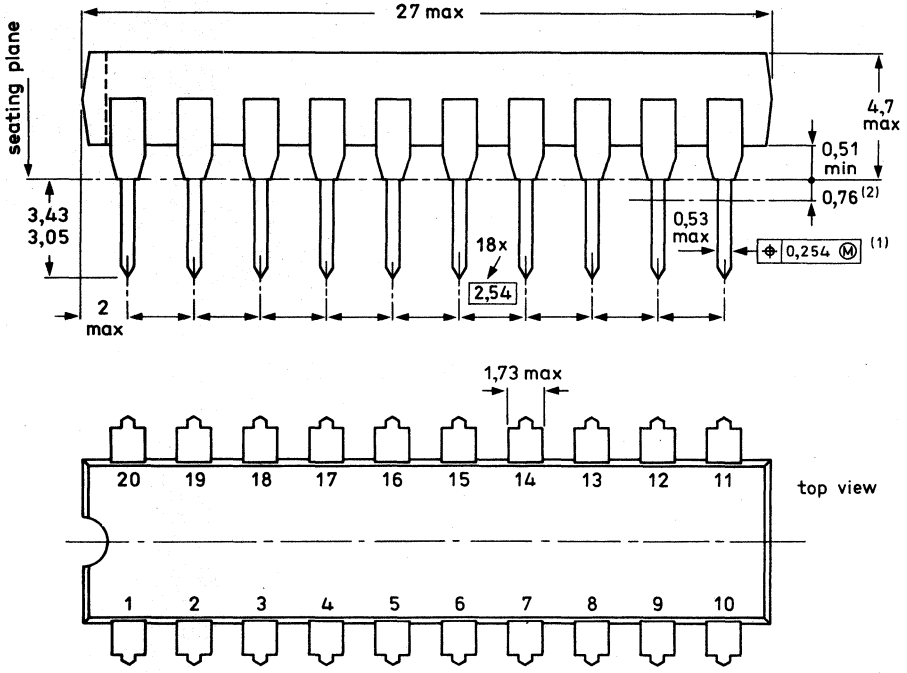


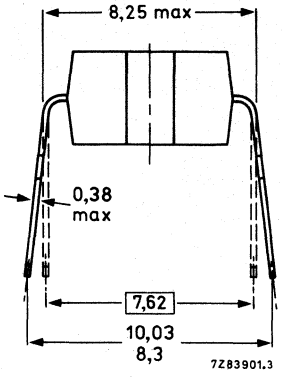
Dimensions in mm

⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

20-LEAD DUAL IN-LINE; PLASTIC (SOT-146)





side view

⊕ Positional accuracy.

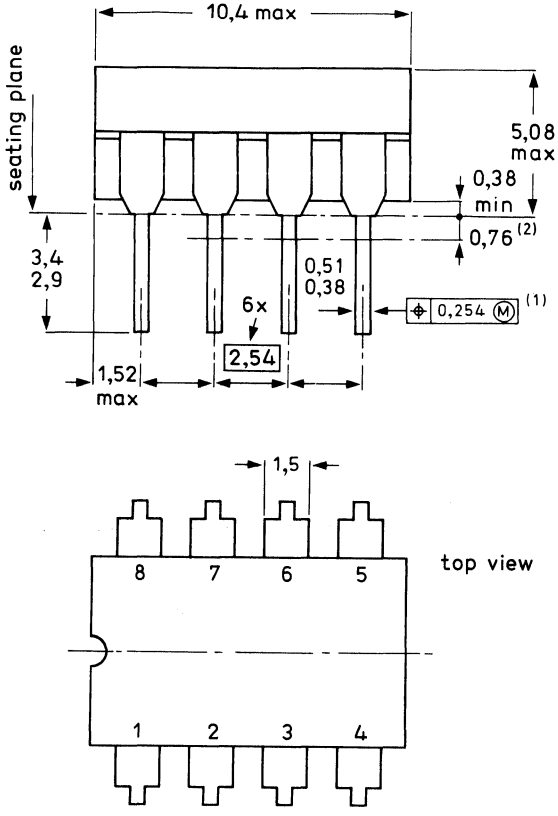
Ⓜ Maximum Material Condition.

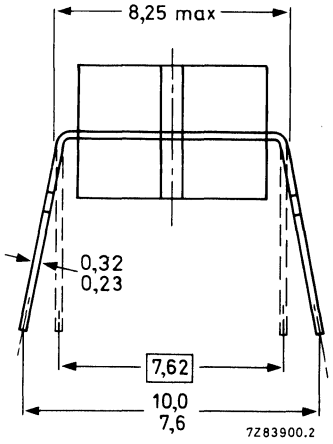
(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

Dimensions in mm

8-LEAD DUAL IN-LINE; CERAMIC (CERDIP) (SOT-151A)





⊕ Positional accuracy.

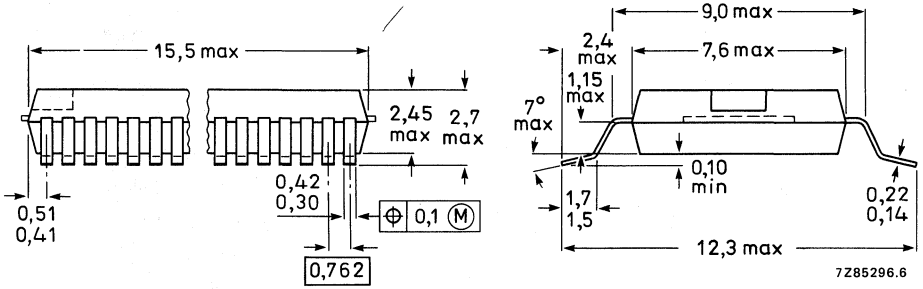
Ⓜ Maximum Material Condition.

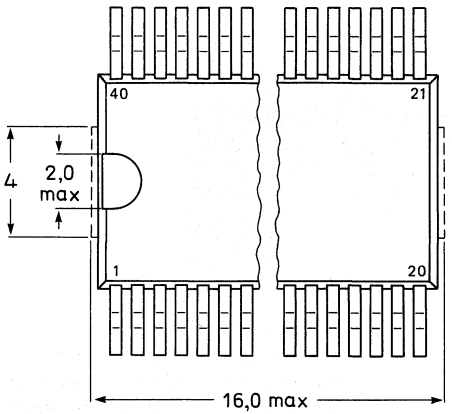
(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

Dimensions in mm

40-LEAD MINI-PACK; PLASTIC (VSO-40; SOT-158A)





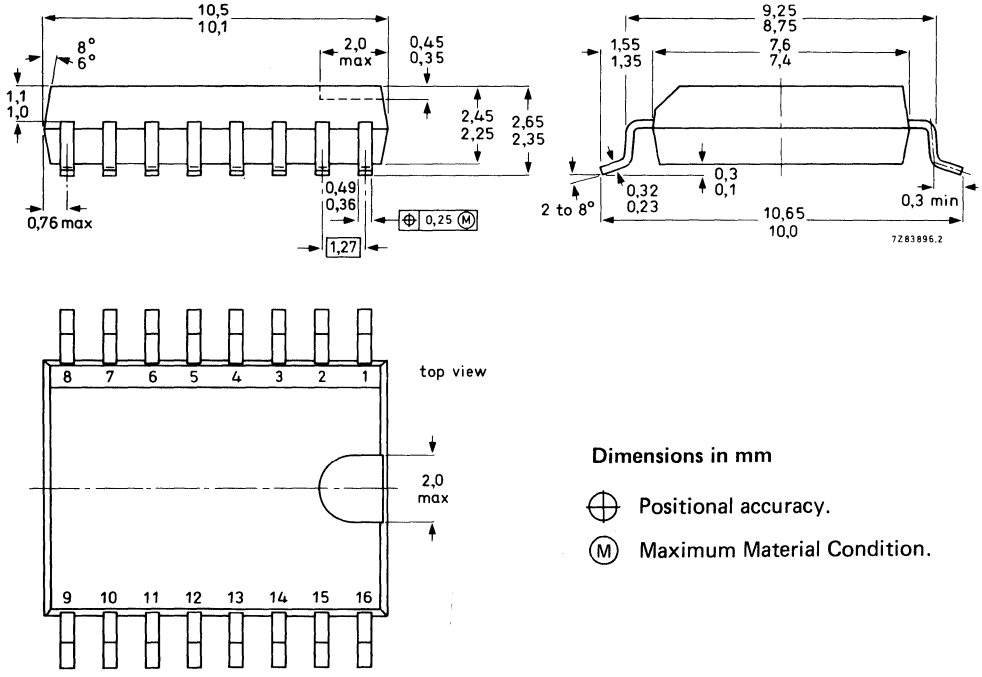
top view

Dimensions in mm

⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

16-LEAD MINI-PACK; PLASTIC (SO-16L; SOT-162A)

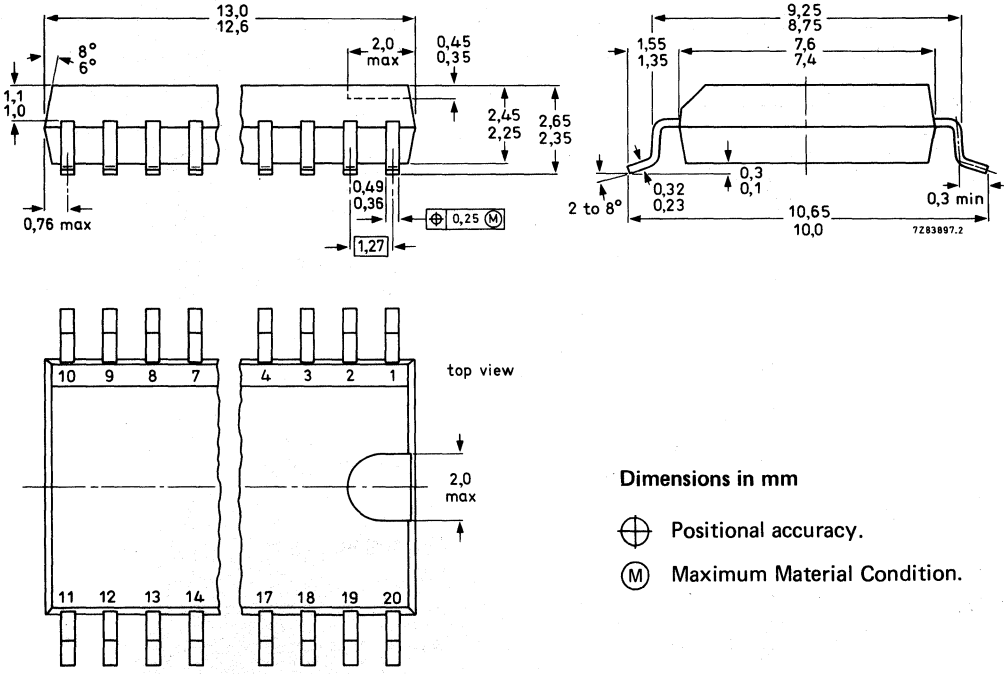


Dimensions in mm

⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

20-LEAD MINI-PACK; PLASTIC (SO-20; SOT-163A)

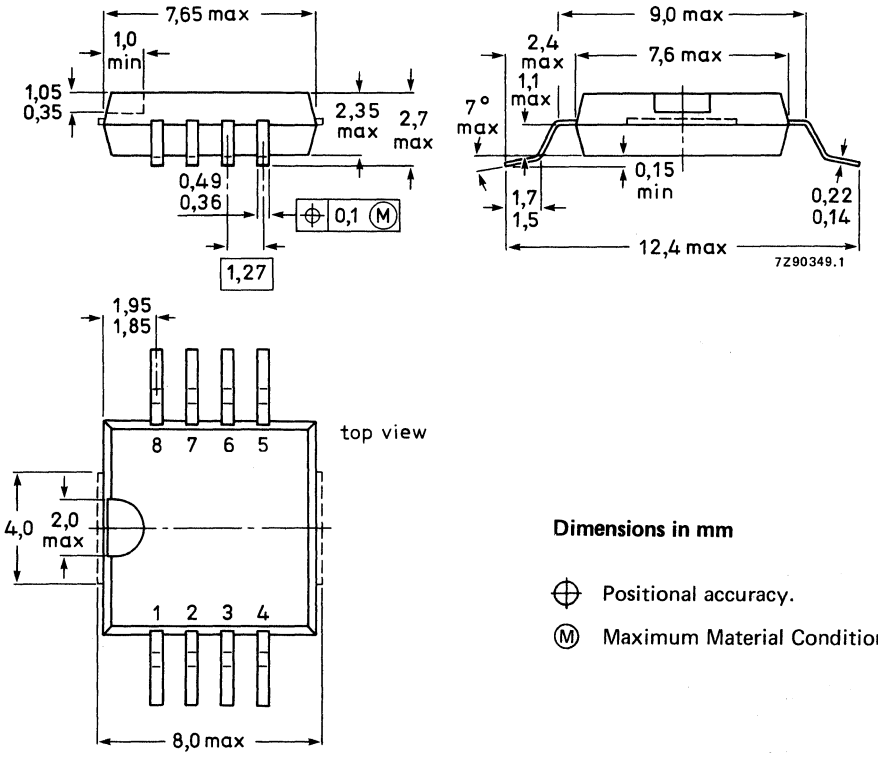


Dimensions in mm

⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

8-LEAD MINI-PACK; PLASTIC (SO-8L; SOT-176)

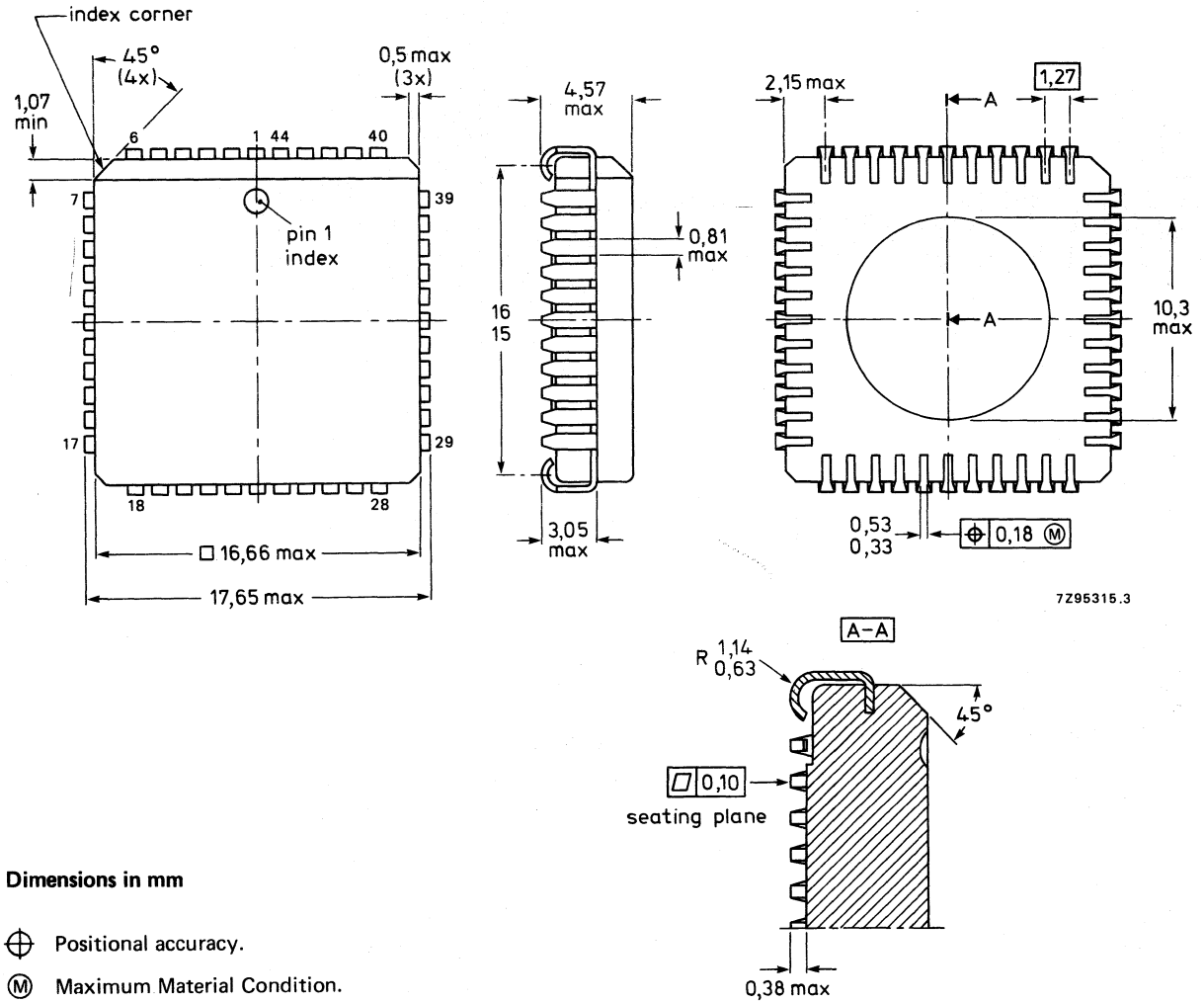


Dimensions in mm

⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

44-LEAD PLASTIC LEADED CHIP-CARRIER (PLCC); SOT-187A

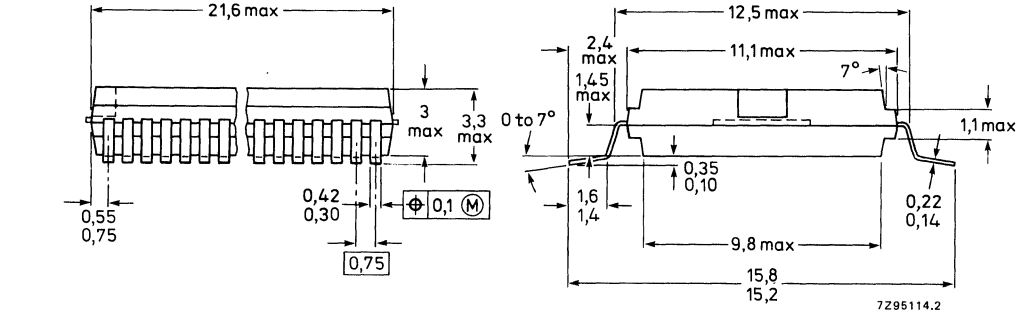


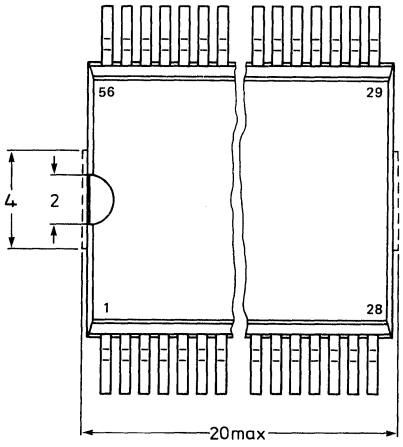
Dimensions in mm

⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

56-LEAD MINI-PACK; PLASTIC (VSO-56; SOT-190)





top view

Dimensions in mm

⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

SOLDERING PLASTIC DUAL IN-LINE (DIL) PACKAGES

1. **By hand**

   Apply the soldering iron below the seating plane (or not more than 2 mm above it).
   If its temperature is below 300 °C it must not be in contact for more than 10 seconds; if between 300 °C and 400 °C, for not more than 5 seconds.

2. **By dip or wave**

   The maximum permissible temperature of the solder is 260 °C; this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.
   The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

3. **Repairing soldered joints**

   The same precautions and limits apply as in (1) above.

SOLDERING PLASTIC MINI-PACK (SO) PACKAGES

1. **By hand-held soldering iron or pulse-heated solder tool**

   Apply the heating tool to the flat part of the lead only. Contact time must be limited to 10 seconds at up to 300 °C. When using proper tools, all leads can be soldered in one operation within 2 to 5 seconds at between 270 and 320 °C. (Pulse-heated soldering is not recommended for SO packages).

   For pulse-heated solder tool (resistance) soldering of VSO packages, solder is applied to substrate by dipping or by an extra thick tin/lead plating before package placement.

2. **By wave**

   Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder bath is 10 seconds, if allowed to cool to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

   A modified wave soldering technique is recommended, using two solder waves (dual-wave); a first turbulent wave with high upward pressure is followed by a smooth, laminar wave. A mildly activated flux will eliminate the need for removal of corrosive residues in most applications.

3. **By solder paste reflow**

   Reflow soldering requires the solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the substrate by screen printing or pressure-syringe dispensing before device placement.

   Several techniques exist for reflowing, for example, thermal conduction by heated belt, infrared, and vapour-phase reflow. Dwell times vary between 8 and 60 seconds according to method. Typical reflow temperatures range from 215 to 250 °C.

   Pre-heating is necessary to dry paste and evaporate binding agent, and to reduce thermal shock on entry to reflow zone.

4. **Repairing soldered joints**

   The same precautions and limits apply as in (1) above.

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