PHILIPS

Data handbook

Electronic components and materials

Integrated circuits

Supplement to Book IC06N 1985

High-speed CMOS

PC54/74HC/HCT/HCU

Logic family

SUPPLEMENT

PHILIPS

High-speed CMOS

Supplement to IC06N 1985

HIGH-SPEED CMOS PC74/HC/HCT/HCU LOGIC FAMILY

DATA HANDBOOK SYSTEM

Our Data Handbook System comprises more than 60 books with specifications on electronic components, subassemblies and materials. It is made up of four series of handbooks:

ELECTRON TUBES	BLUE
SEMICONDUCTORS	RED
INTEGRATED CIRCUITS	PURPLE
COMPONENTS AND MATERIALS	GREEN

The contents of each series are listed on pages iv to viii.

The data handbooks contain all pertinent data available at the time of publication, and each is revised and reissued periodically.

When ratings or specifications differ from those published in the preceding edition they are indicated with arrows in the page margin. Where application information is given it is advisory and does not form part of the product specification.

Condensed data on the preferred products of Philips Electronic Components and Materials Division is given in our Preferred Type Range catalogue (issued annually).

Information on current Data Handbooks and on how to obtain a subscription for future issues is available from any of the Organizations listed on the back cover.
Product specialists are at your service and enquiries will be answered promptly.

ELECTRON TUBES (BLUE SERIES)

The blue series of data handbooks comprises:

T1 **Tubes for r.f. heating**

T2a **Transmitting tubes for communications, glass types**

T2b **Transmitting tubes for communications, ceramic types**

T3 **Klystrons**

T4 **Magnetrons for microwave heating**

T5 **Cathode-ray tubes**
Instrument tubes, monitor and display tubes, C.R. tubes for special applications

T6 **Geiger-Müller tubes**

T7 **Gas-filled tubes** (will not be reprinted)

T8 **Colour display systems**
Colour TV picture tubes, colour data graphic display tube assemblies, deflection units

T9 **Photo and electron multipliers**

T10 **Plumbicon camera tubes and accessories**

T11 **Microwave semiconductors and components**

T12 **Vidicon and Newvicon camera tubes**

T13 **Image intensifiers**

T14 **Infrared detectors**

T15 **Dry reed switches**

Data collations on these subjects are available now.
Data Handbooks will be published in 1985.

T16 **Monochrome tubes and deflection units**
Black and white TV picture tubes, monochrome data graphic display tubes, deflection units

SEMICONDUCTORS (RED SERIES)

The red series of data handbooks comprises:

S1 **Diodes**
Small-signal germanium diodes, small-signal silicon diodes, voltage regulator diodes (< 1,5 W), voltage reference diodes, tuner diodes, rectifier diodes

S2a **Power diodes**

S2b **Thyristors and triacs**

S3 **Small-signal transistors**

S4a **Low-frequency power transistors and hybrid modules**

S4b **High-voltage and switching power transistors**

S5 **Field-effect transistors**

S6 **R.F. power transistors and modules**

S7 **Surface mounted semiconductors**

S8 **Devices for optoelectronics**
Photosensitive diodes and transistors, light-emitting diodes, displays, photocouplers, infrared sensitive devices, photoconductive devices.

S9 **Power MOS transistors**

S10 **Wideband transistors and wideband hybrid IC modules**

S11 **Microwave transistors**

S12 **Surface acoustic wave devices**

INTEGRATED CIRCUITS (PURPLE SERIES)

The purple series of data handbooks comprises:

EXISTING SERIES		Superseded by:
IC1	**Bipolar ICs for radio and audio equipment**	IC01N
IC2	**Bipolar ICs for video equipment**	IC02Na and IC02Nb
IC3	**ICs for digital systems in radio, audio and video equipment**	IC01N, IC02Na and IC02Nb
IC4	**Digital integrated circuits** CMOS HE4000B family	
IC5	**Digital integrated circuits – ECL** ECL10 000 (GX family), ECL100 000 (HX family), dedicated designs	IC08N
IC6	**Professional analogue integrated circuits**	
IC7	**Signetics bipolar memories**	
IC8	**Signetics analogue circuits**	IC11N
IC9	**Signetics TTL logic**	IC09N and IC15N
IC10	**Signetics Integrated Fuse Logic (IFL)**	IC13N
IC11	**Microprocessors, microcomputers and peripheral circuitry**	IC14N

NEW SERIES

IC01N	**Radio, audio and associated systems** Bipolar, MOS	(published 1985)
IC02Na	**Video and associated systems** Bipolar, MOS Types MAB8031AH to TDA1524A	(published 1985)
IC02Nb	**Video and associated systems** Bipolar, MOS Types TDA2501 to TEA1002	(published 1985)
IC03N	**Integrated circuits for telephony**	(published 1985)
IC04N	**HE4000B logic family** CMOS	
IC05N	**HE4000B logic family — uncased ICs** CMOS	(published 1984)
IC06N	**High-speed CMOS; PC54/74HC/HCT/HCU** Logic family	(published 1985)
Supplement to IC06N	**High-speed CMOS; PC74HC/HCT/HCU** Logic family	(published 1985)
IC07N	**High-speed CMOS; PC54/74HC/HCT/HCU — uncased ICs** Logic family	
IC08N	**ECL 10K and 100K logic families**	(published 1984)
IC09N	**TTL logic series**	(published 1984)
IC10N	**Memories** MOS, TTL, ECL	
IC11N	**Linear LSI**	(published 1985)
IC12N	**Semi-custom gate arrays & cell libraries** ISL, ECL, CMOS	
IC13N	**Semi-custom** Integrated Fuse Logic	(published 1985)
IC14N	**Microprocessors, microcontrollers & peripherals** Bipolar, MOS	(published 1985)
IC15N	**FAST TTL logic series**	(published 1984)

Note

Books available in the new series are shown with their date of publication.

COMPONENTS AND MATERIALS (GREEN SERIES)

The green series of data handbooks comprises:

C1 **Programmable controller modules**
PLC modules, PC20 modules

C2 **Television tuners, coaxial aerial input assemblies, surface acoustic wave filters**

C3 **Loudspeakers**

C4 **Ferroxcube potcores, square cores and cross cores**

C5 **Ferroxcube for power, audio/video and accelerators**

C6 **Synchronous motors and gearboxes**

C7 **Variable capacitors**

C8 **Variable mains transformers**

C9 **Piezoelectric quartz devices**

C10 **Connectors**

C11 **Non-linear resistors**
Voltage dependent resistors (VDR), light dependent resistors (LDR), negative temperature coefficient thermistors (NTC), positive temperature coefficient thermistors (PTC)

C12 **Potentiometers, encoders and switches**

C13 **Fixed resistors**

C14 **Electrolytic and solid capacitors**

C15 **Ceramic capacitors**

C16 **Permanent magnet materials**

C17 **Stepping motors and associated electronics**

C18 **Direct current motors**

C19 **Piezoelectric ceramics**

C20 **Wire-wound components for TVs and monitors**

C21* **Assemblies for industrial use**
HNIL FZ/30 series, NORbits 60-, 61-, 90-series, input devices

C22 **Film capacitors**

* Will be issued in 1985.

INTRODUCTION

INTRODUCTION TO HANDBOOK IC06N SUPPLEMENT – HIGH-SPEED CMOS

Since the issue of our most recent data handbook on high-speed CMOS, IC06N (published Spring 1985), we have significantly extended our HCMOS PC74HC/HCT/HCU logic family and have upgraded the family specifications. To inform you of the new circuits and family specifications we have published this supplement to IC06N. The supplement will be incorporated in the next revision of handbook IC06N, due in the beginning of 1986.

The upgrades are:

- 74HC/HCT/HCU family is now specified for an operating ambient temperature range of −40 to + 85 °C and an extended range of −40 to + 125 °C;
- noise immunity has been improved by up to 50% for HC types, with a specified switching level for V_{IL} of 30% of the supply voltage V_{CC};
- 74HC/HCT/HCU family is available in SO plastic mini-packs for surface mounting as well as in plastic DIL packages.

Because the 74HC/HCT/HCU family can now be used over the extended operating ambient temperature range, we no longer supply the 54HC/HCT/HCU family.

The 74HCMOS family is manufactured using a self-aligning 3 μm polycrystalline silicon-gate CMOS process combined with local oxidation of silicon (LOCOS). The circuits have the low power consumption, high immunity to input noise and wide operating temperature range of earlier silicon-gate CMOS circuits together with the high-speed and drive capability of bipolar, low power Schottky TTL (LSTTL).

Many 74HCMOS circuits are pin-compatible with existing 54/74 LSTTL and HE4000B CMOS digital logic circuits. The 74HCT circuits are an ideal replacement for LSTTL circuits and can interface between CMOS and TTL.

All 74HCMOS circuits are fully buffered*, operate up to 60 MHz (typ.) and have gate delays of about 8 ns. Two types of circuits are available:

HC CMOS input switching levels ($\frac{1}{2}V_{CC}$), power supply = 2 to 6 V;

HCT TTL input switching levels (1.3 V), power supply = 5 V (typ.).

* An unbuffered HCMOS circuit is available: hex inverter HCU04.

Features

- Very low power dissipation
- DC noise margin of HC types twice that of TTL devices
- 30/70% switching levels
- Fanout capability of 10 LSTTL loads (4 mA); this is increased to 15 LSTTL loads (6 mA) in circuits having bus-driver outputs
- Wide operating voltage range
- Latch-up free operation
- Improved protection against electrostatic discharge
- Functions and pinning identical to our popular LSTTL and CMOS HE4000B families of integrated circuits
- Analog switching types operating up to 10 V
- Symmetrical output sourcing and sinking currents and equal output rise and fall times
- Available in plastic SO packages for surface mounting and plastic DIL packages
- Choice of operating ambient temperature range: −40 to + 85 °C or −40 to + 125 °C
- Meets JEDEC standard No. 7

SELECTION GUIDE

HCMOS 74HC/HCT/HCU FAMILY

Type numbers have a suffix which signifies the type of package:
P = plastic DIL; T = plastic SO mini-pack

* Types with a bus-driver output stage.

Type numbers have a suffix which signifies the type of package:
P = plastic DIL; T = plastic SO mini-pack

* Types with a bus-driver output stage.

HCMOS 74HC/HCT/HCU FAMILY

* Types with a bus driver output stage.

HCMOS FAMILY CHARACTERISTICS

GENERAL

These family specifications cover the common electrical ratings and characteristics of the entire HCMOS 74HC/HCT/HCU family, unless otherwise specified in the individual device data sheet.

INTRODUCTION

The 74HC/HCT/HCU high-speed Si-gate CMOS logic family combines the low power advantages of the HE4000B family with the high speed and drive capability of the low power Schottky TTL (LSTTL).

The family will have the same pin-out as the 74 series and provide the same circuit functions.

In these families are included several HE4000B family circuits which do not have TTL counterparts, and some special circuits.

The basic family of buffered devices, designated as XX74HCXXXXX, will operate at CMOS input logic levels for high noise immunity, negligible typical quiescent supply and input current. It is operated from a power supply of 2 to 6 V.

A subset of the family, designated as XX74HCTXXXXX, with the same features and functions as the "HC-types", will operate at standard TTL power supply voltage (5 V ± 10%) and logic input levels (0,8 to 2,0 V) for use as pin-to-pin compatible CMOS replacements to reduce power consumption without loss of speed. These types are also suitable for converted switching from TTL to CMOS.

Another subset, the XX74HCUXXXXX, consists of single-stage unbuffered CMOS compatible devices for application in RC or crystal controlled oscillators and other types of feedback circuits which operate in the linear mode.

HANDLING MOS DEVICES

Inputs and outputs are protected against electrostatic effects in a wide variety of device-handling situations.
However, to be totally safe, it is desirable to take handling precautions into account (see also chapter "APPLICATION NOTES" section "HANDLING CMOS DEVICES").

RECOMMENDED OPERATING CONDITIONS FOR 74HC/HCT

SYMBOL	PARAMETER	74HC			74HCT			UNIT	CONDITIONS
		min.	typ.	max.	min.	typ.	max.		
V_{CC}	DC supply voltage	2.0	5.0	6.0	4.5	5.0	5.5	V	
V_I	DC input voltage range	0		V_{CC}	0		V_{CC}	V	
V_O	DC output voltage range	0		V_{CC}	0		V_{CC}	V	
T_{amb}	operating ambient temperature range	−40		+85	−40		+85	°C	see DC and AC CHAR. per device
T_{amb}	operating ambient temperature range	−40		+125	−40		+125	°C	
t_r, t_f	input rise and fall times except for Schmitt-trigger inputs		6.0	1000 500 400		6.0	500	ns	V_{CC} = 2.0 V V_{CC} = 4.5 V V_{CC} = 6.0 V

Note

For analog switches, e.g. "4016", "4051 series", "4351 series", "4066" and "4067", 10 V is specified as the maximum operating voltage.

RECOMMENDED OPERATING CONDITIONS FOR 74HCU

SYMBOL	PARAMETER	74HCU			UNIT	CONDITIONS
		min.	typ.	max.		
V_{CC}	DC supply voltage	2.0	5.0	6.0	V	
V_I	DC input voltage range	0		V_{CC}	V	
V_O	DC output voltage range	0		V_{CC}	V	
T_{amb}	operating ambient temperature range	−40		+85	°C	see DC and AC CHAR. per device
T_{amb}	operating ambient temperature range	−40		+125	°C	

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
V_{CC}	DC supply voltage	−0.5	+7	V	
$\pm I_{IK}$	DC input diode current		20	mA	for $V_I < -0.5$ or $V_I > V_{CC} + 0.5$ V
$\pm I_{OK}$	DC output diode current		20	mA	for $V_O < -0.5$ or $V_O > V_{CC} + 0.5$ V
$\pm I_O$	DC output source or sink current – standard outputs – bus driver outputs		 25 35	 mA mA	for -0.5 V $< V_O < V_{CC} + 0.5$ V
$\pm I_{CC}$; $\pm I_{GND}$	DC V_{CC} or GND current for types with: – standard outputs – bus driver outputs		 50 70	 mA mA	
T_{stg}	storage temperature range	−65	+150	°C	
P_{tot}	power dissipation per package				for temperature range: −40 to +85 °C 74HC/HCT/HCU
	plastic DIL		500	mW	above +60 °C: derate linearly with 8 mW/K
	plastic mini-pack (SO)		400	mW	above +60 °C: derate linearly with 6 mW/K
P_{tot}	power dissipation per package				for temperature range: −40 to +125 °C 74HC/HCT/HCU
	plastic DIL		500	mW	above +70 °C: derate linearly with 8 mW/K
	plastic mini-pack (SO)		400	mW	above +70 °C: derate linearly with 6 mW/K

Note

For analog switches, e.g. "4016", "4051 series", "4351 series", "4066" and "4067", 11 V is specified as the maximum operating voltage.

DC CHARACTERISTICS FOR 74HC

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		74HC								V_{CC} V	V_I	OTHER
		+25			−40 to +85		−40 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
V_{IH}	HIGH level input voltage	1.5 3.15 4.2	1.3 2.4 3.1		1.5 3.15 4.2		1.5 3.15 4.2		V	2.0 4.5 6.0		
V_{IL}	LOW level input voltage		0.7 1.8 2.3	0.5 1.35 1.8		0.5 1.35 1.8		0.5 1.35 1.8	V	2.0 4.5 6.0		
V_{OH}	HIGH level output voltage all outputs	1.9 4.4 5.9	2.0 4.5 6.0		1.9 4.4 5.9		1.9 4.4 5.9		V	2.0 4.5 6.0	V_{IH} or V_{IL}	$-I_O = 20\ \mu A$ $-I_O = 20\ \mu A$ $-I_O = 20\ \mu A$
V_{OH}	HIGH level output voltage standard outputs	3.98 5.48			3.84 5.34		3.7 5.2		V	4.5 6.0	V_{IH} or V_{IL}	$-I_O = 4.0$ mA $-I_O = 5.2$ mA
V_{OH}	HIGH level output voltage bus driver outputs	3.98 5.48			3.84 5.34		3.7 5.2		V	4.5 6.0	V_{IH} or V_{IL}	$-I_O = 6.0$ mA $-I_O = 7.8$ mA
V_{OL}	LOW level output voltage all outputs		0 0 0	0.1 0.1 0.1		0.1 0.1 0.1		0.1 0.1 0.1	V	2.0 4.5 6.0	V_{IH} or V_{IL}	$I_O = 20\ \mu A$ $I_O = 20\ \mu A$ $I_O = 20\ \mu A$
V_{OL}	LOW level output voltage standard outputs			0.26 0.26		0.33 0.33		0.4 0.4	V	4.5 6.0	V_{IH} or V_{IL}	$I_O = 4.0$ mA $I_O = 5.2$ mA
V_{OL}	LOW level output voltage bus driver outputs			0.26 0.26		0.33 0.33		0.4 0.4	V	4.5 6.0	V_{IH} or V_{IL}	$I_O = 6.0$ mA $I_O = 7.8$ mA
$\pm I_I$	input leakage current			0.1		1.0		1.0	μA	6.0	V_{CC} or GND	
$\pm I_{OZ}$	3-state OFF-state current			0.5		5.0		10.0	μA	6.0	V_{IH} or V_{IL}	$V_O = V_{CC}$ or GND
I_{CC}	quiescent supply current **SSI** **flip-flops** **MSI**			 2.0 4.0 8.0		 20.0 40.0 80.0		 40.0 80.0 160.0	 μA μA μA	 6.0 6.0 6.0	 V_{CC} or GND	 $I_O = 0$ $I_O = 0$ $I_O = 0$

DC CHARACTERISTICS FOR 74HCT

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		74HCT								V_{CC} V	V_I	OTHER
		+25			−40 to +85		−40 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
V_{IH}	HIGH level input voltage	2.0			2.0		2.0		V	4.5 to 5.5		
V_{IL}	LOW level input voltage			0.8		0.8		0.8	V	4.5 to 5.5		
V_{OH}	HIGH level output voltage all outputs	4.4	4.5		4.4		4.4		V	4.5	V_{IH} or V_{IL}	$-I_O = 20\ \mu A$
V_{OH}	HIGH level output voltage standard outputs	3.98			3.84		3.7		V	4.5	V_{IH} or V_{IL}	$-I_O = 4.0$ mA
V_{OH}	HIGH level output voltage bus driver outputs	3.98			3.84		3.7		V	4.5	V_{IH} or V_{IL}	$-I_O = 6.0$ mA
V_{OL}	LOW level output voltage all outputs		0	0.1		0.1		0.1	V	4.5	V_{IH} or V_{IL}	$I_O = 20\ \mu A$
V_{OL}	LOW level output voltage standard outputs			0.26		0.33		0.4	V	4.5	V_{IH} or V_{IL}	$I_O = 4.0$ mA
V_{OL}	LOW level output voltage bus driver outputs			0.26		0.33		0.4	V	4.5	V_{IH} or V_{IL}	$I_O = 6.0$ mA
$\pm I_I$	input leakage current			0.1		1.0		1.0	μA	5.5	V_{CC} or GND	
$\pm I_{OZ}$	3-state OFF-state current			0.5		5.0		10.0	μA	5.5	V_{IH} or V_{IL}	$V_O = V_{CC}$ or GND per input pin; other inputs at V_{CC} or GND; $I_O = 0$
I_{CC}	quiescent supply current SSI flip-flops MSI			 2.0 4.0 8.0		 20.0 40.0 80.0		 40.0 80.0 160.0	 μA μA μA	 5.5 5.5 5.5	V_{CC} or GND	 $I_O = 0$ $I_O = 0$ $I_O = 0$
ΔI_{CC}	additional quiescent supply current per input pin for unit load coefficient is 1 (note 1)		100	360		450		490	μA	4.5 to 5.5	V_{CC} −2.1 V	other inputs at V_{CC} or GND; $I_O = 0$

Note

1. The additional quiescent supply current per input is determined by the ΔI_{CC} unit load, which has to be multiplied by the unit load coefficient as given in the individual data sheets. For dual supply systems the theoretical worst-case ($V_I = 2.4$ V; $V_{CC} = 5.5$ V) specification is: $\Delta I_{CC} = 0.65$ mA (typical) and 1.8 mA (maximum) across temperature.

DC CHARACTERISTICS FOR 74HCU

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		74HCU								V_{CC} V	V_I	OTHER
		+25			−40 to +85		−40 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
V_{IH}	HIGH level input voltage	1.7 3.6 4.8			1.7 3.6 4.8		1.7 3.6 4.8		V	2.0 4.5 6.0		
V_{IL}	LOW level input voltage			0.3 0.9 1.2		0.3 0.9 1.2		0.3 0.9 1.2	V	2.0 4.5 6.0		
V_{OH}	HIGH level output voltage	1.8 4.0 5.5			1.8 4.0 5.5		1.8 4.0 5.5		V	2.0 4.5 6.0	V_{IH} or V_{IL}	$-I_O = 20\ \mu A$ $-I_O = 20\ \mu A$ $-I_O = 20\ \mu A$
V_{OH}	HIGH level output voltage	3.98 5.48			3.84 5.34		3.7 5.2		V	4.5 6.0	V_{CC} or GND	$-I_O = 4.0$ mA $-I_O = 5.2$ mA
V_{OL}	LOW level output voltage			0.2 0.5 0.5		0.2 0.5 0.5		0.2 0.5 0.5	V	2.0 4.5 6.0	V_{IH} or V_{IL}	$I_O = 20\ \mu A$ $I_O = 20\ \mu A$ $I_O = 20\ \mu A$
V_{OL}	LOW level output voltage			0.26 0.26		0.33 0.33		0.4 0.4	V	4.5 6.0	V_{CC} or GND	$I_O = 4.0$ mA $I_O = 5.2$ mA
$\pm I_I$	input leakage current			0.1		1.0		1.0	μA	6.0	V_{CC} or GND	
I_{CC}	quiescent supply current SSI			2.0		20.0		40.0	μA	6.0	V_{CC} or GND	$I_O = 0$

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{THL}/ t_{TLH}	output transition time standard outputs			75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Figs 3 and 4
t_{THL}/ t_{TLH}	output transition time bus driver outputs			60 12 10		75 15 13		90 18 15	ns	2.0 4.5 6.0	Figs 3 and 4

AC CHARACTERISTICS FOR 74HCU

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCU								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{THL}/ t_{TLH}	output transition time			75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 1

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{THL}/ t_{TLH}	output transition time standard outputs			15		19		22	ns	4.5	Figs 8 and 9
t_{THL}/ t_{TLH}	output transition time bus driver outputs			12		15		18	ns	4.5	Figs 8 and 9

HCU TYPES

AC WAVEFORMS 74HCU

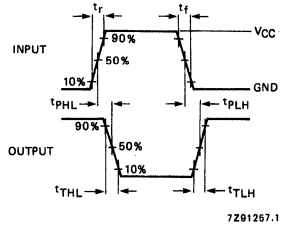


Fig. 1 Input rise and fall times, transition times and propagation delays for combinatorial logic ICs.

TEST CIRCUIT FOR 74HCU

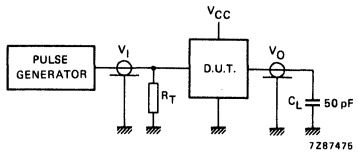


Fig. 2 Test circuit.

Definitions for Fig. 2:

C_L = load capacitance including jig and probe capacitance (see AC CHARACTERISTICS for values).
R_T = termination resistance should be equal to the output impedance Z_O of the pulse generator.

HC TYPES

AC WAVEFORMS 74HC

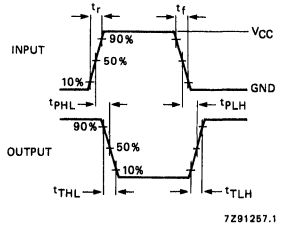


Fig. 3 Input rise and fall times, transition times and propagation delays for combinatorial logic ICs.

AC WAVEFORMS 74HC

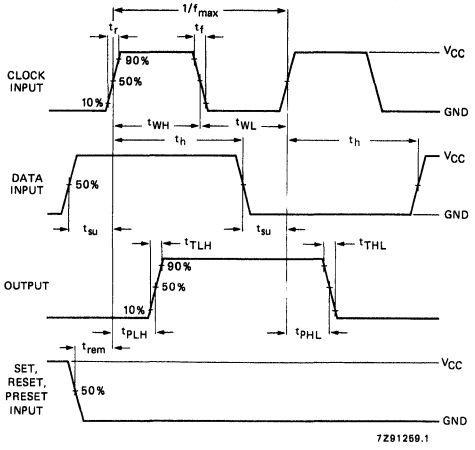


Fig. 4 Set-up times, hold times, removal times, propagation delays and the maximum clock pulse frequency for sequential logic ICs.

Notes to Fig. 4

1. In Fig. 4 the active transition of the clock is going from LOW-to-HIGH and the active level of the forcing signals (SET, RESET and PRESET) is HIGH. The actual direction of the transition of the clock input and the actual active levels of the forcing signals are specified in the individual device data sheet.
2. For AC measurements: $t_r = t_f = 6$ ns; when measuring f_{max}, there is no constraint on t_r, t_f or pulse width.

HC TYPES (continued)

TEST CIRCUIT FOR 74HC

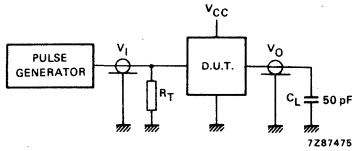


Fig. 5 Test circuit.

Definitions for Fig. 5:

C_L = load capacitance including jig and probe capacitance (see AC CHARACTERISTICS for values).
R_T = termination resistance should be equal to the output impedance Z_O of the pulse generator.

AC WAVEFORMS 74HC (continued)

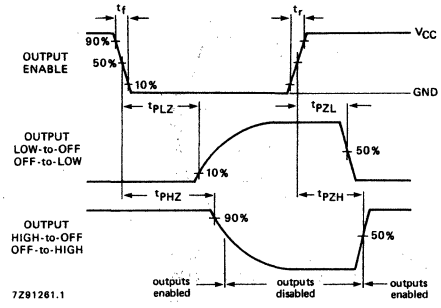
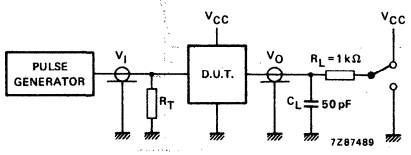


Fig. 6 Propagation delays of 3-state outputs.

TEST CIRCUIT FOR 74HC



Switch position

TEST	SWITCH
t_{PZH}	GND
t_{PZL}	V_{CC}
t_{PHZ}	GND
t_{PLZ}	V_{CC}

Note to switch position table

For open-drain N-channel outputs t_{PLZ} and t_{PZL} are applicable.

Fig. 7 Test circuit for 3-state outputs.

Definitions for Fig. 7:

C_L = load capacitance including jig and probe capacitance (see AC CHARACTERISTICS for values).
R_T = termination resistance should be equal to the output impedance Z_O of the pulse generator.

HCT TYPES

AC WAVEFORMS 74HCT

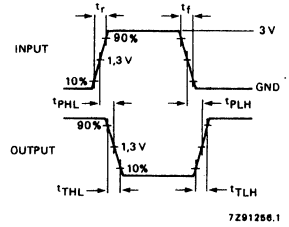


Fig. 8 Input rise and fall times, transition times and propagation delays for combinatorial logic ICs.

AC WAVEFORMS 74HCT

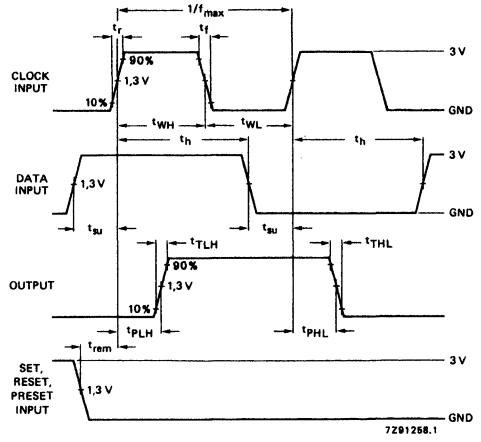


Fig. 9 Set-up times, hold times, removal times, propagation delays and the maximum clock pulse frequency for sequential logic ICs.

Notes to Fig. 9

1. In Fig. 9 the active transition of the clock is going from LOW-to-HIGH and the active level of the forcing signals (SET, RESET and PRESET) is HIGH. The actual direction of the transition of the clock input and the actual active levels of the forcing signals are specified in the individual device data sheet.
2. For AC measurements: $t_r = t_f = 6$ ns; when measuring f_{max}, there is no constraint on t_r, t_f or pulse width.

TEST CIRCUIT FOR 74HCT

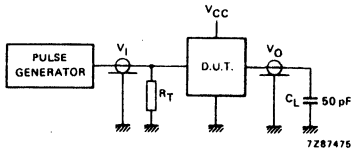


Fig. 10 Test circuit.

Definitions for Fig. 10:

C_L = load capacitance including jig and probe capacitance (see AC CHARACTERISTICS for values).
R_T = termination resistance should be equal to the output impedance Z_O of the pulse generator.

HCT TYPES (continued)

AC WAVEFORMS 74HCT (continued)

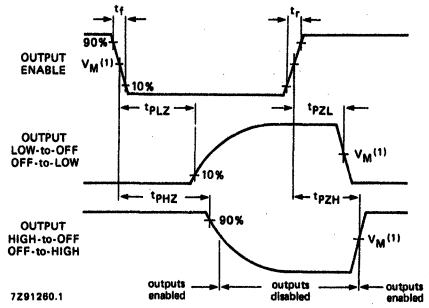
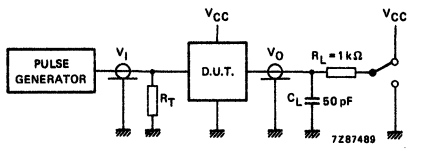


Fig. 11 Propagation delays of 3-state outputs.

TEST CIRCUIT FOR 74HCT



Switch position

TEST	SWITCH
t_{PZH}	GND
t_{PZL}	V_{CC}
t_{PHZ}	GND
t_{PLZ}	V_{CC}

Note to switch position table

For open-drain N-channel outputs t_{PLZ} and t_{PZL} are applicable.

Fig. 12 Test circuit for 3-state outputs.

Definitions for Fig. 12:

C_L = load capacitance including jig and probe capacitance (see AC CHARACTERISTICS for values).
R_T = termination resistance should be equal to the output impedance Z_O of the pulse generator.

INTRODUCTION

The HCMOS HC/HCT/HCU data sheets have been configured for quick usability.

They are self-contained and should require minimum reference to other sections for amplifying information.

For examples of AC waveforms and test circuits see section "FAMILY CHARACTERISTICS".

TYPICAL PROPAGATION DELAY AND FREQUENCY

The typical propagation delays listed at the top of the data sheets are the average between t_{PLH} and t_{PHL} for the most significant data path through the part with a 15 pF load.

In case of clocked products, this is sometimes the maximum frequency of operation. In any event, this number is under the operating conditions of V_{CC} = 5.0 V and T_{amb} = 25 °C.

For the typical operating frequency this is the maximum device operating frequency with 50% duty factor and no constraints on t_r and t_f.

LOGIC SYMBOLS

There are two types of logic symbols. The conventional one, "Logic Symbol", explicitly shows the internal logic (except for complex logic). The other is "IEC Logic Symbol" as developed by the IEC (International Electrotechnical Commission).

IEC has been developing a very powerful symbolic language that can show the relationship of each input of a digital logic circuit to each output without explicitly showing the internal logic. Internationally, Working Group 2 of IEC Technical Committee TC-3 has prepared a new document (Publication 617-12) that consolidates the original work started in the mid-1960's and published in 1972 (Publication 117-15), and the amendments and supplements that have been followed.

RATINGS

The "RATINGS" table (Limiting values in accordance with the Absolute Maximum System - IEC134) carries the maximum limits to which the device can be subjected without damaging it; there is no implication that the device will function at these extreme conditions. Thus, specifications such as the most negative voltage that may be applied to the outputs only guarantees that if less than -0.5 V is applied to the output pin, after that voltage is removed, the device will still be functional and its useful life will not have been shortened. The maximum rated supply voltage of 7 V is well below the typical breakdown voltage of 18 V. The DC input and output diode currents are often referred to, that at these values no latch-up of the devices occur.

RECOMMENDED OPERATING CONDITIONS

The "RECOMMENDED OPERATING CONDITIONS" table has a dual purpose. In one sense, it sets some environmental conditions (operating free-air temperature), and in another, it sets the conditions under which the limits set forth in the "DC CHARACTERISTICS" table and the "AC CHARACTERISTICS" table will be met. Another way of looking at this table is to think of it not as a set of limits guaranteed by the manufacturer, but as the conditions used to test the parts and guarantee that they will then meet the limits set forth in the DC and AC CHARACTERISTICS tables.

DC CHARACTERISTICS

This table reflects the DC limits used during the testing operations. The input threshold values of V_{IH} and V_{IL} can be tested by the user with parametric test equipment; if V_{IH} and V_{IL} are applied to the inputs, the outputs will be at the voltages guaranteed by the "DC CHARACTERISTICS" table. There is a tendency on the part of some users to use V_{IH} and V_{IL} as conditions applied to the inputs to test the device for functionality in a "function-table exercizer" mode. This frequently causes problems because of the noise present at the test head of automated test equipment. Parametric tests, such as those used for the output levels under the V_{IH} and V_{IL} conditions are done fairly slowly, on the order of milliseconds, and any noise present at the inputs has settled out before the outputs are measured. But in functionality testing, the outputs are examined much faster, before the noise on the inputs has settled out and the device has assumed its final and correct output state. Thus, V_{IH} and V_{IL} should never be used in testing the functionality of any HCMOS device type. For these types of tests, input voltages of V_{CC} and 0 V should be used for the HIGH and LOW states, respectively.

In no way does this imply that the devices are noise sensitive in the final system. The use of "hard" HIGHs and LOWs during functional testing is done primarily to reduce the effects of the large amounts of noise typically present at the test heads of automated test equipment with cables that may at times reach one meter or more.
The situation in a system on a PC-board is less severe than in a noisy production environment.

Compared to TTL no output HIGH short-circuit current is specified. The intention of this current, e.g., for calculating propagation delays under capacitive load conditions, is fully covered by the HCMOS output drive graphs and propagation delay increase versus load capacitance.

The quiescent supply current is the leakage current of all the reversed biased diodes and the OFF-state MOS transistors and is tested with the input at V_{CC} or GND. Its value is typically in the low nA region.

AC CHARACTERISTICS

The "AC CHARACTERISTICS" table contains the guaranteed limits when tested under the conditions set forth in the AC Test Circuits and Waveforms section.

TEST CIRCUITS AND WAVEFORMS

For CMOS no load resistor to V_{CC} or GND is applied, because CMOS inputs draw only a negligible amount of input leakage current. Also for HCT outputs, which reference level is the LSTTL established value of 1.3 V, a resistive load is not applied. In case of real TTL loads, the LOW-to- HIGH propagation delay is decreased marginally and the

HIGH-to-LOW propagation delay will increase marginally due to the active DC TTL input current.

The test circuit for 3-state outputs is self explanatory. Special attention needs the disable time definition in the waveforms.

As shown in Fig. 6 (section "FAMILY CHARACTERISTICS" - AC WAVEFORMS for 74HC), the disable times are measured at the point where the output voltage has risen or fallen by 10% of the voltage swing.

Since the rising or falling waveform is RC-controlled, the 10% of change is more linear and is less susceptible to external and circuit influences.

TEST CIRCUIT AND WAVEFORMS (continued)

More importantly, from the system designer's point of view, 10% is adequate to ensure that a device output has turned OFF. It also gives system designers more realistic delay times to use in calculating minimum cycle times. To study the break before make characteristic the user may substract the 10% RC-time, being 5 ns, from the values given in the data sheet, in order to know the real internal disable propagation delay.

Good, high-frequency wiring practices should be used in constructing test jigs. Leads on the load capacitor should be as short as possible to minimize ripples on the output waveform transitions and to minimize undershoot. Generous ground metal (preferably a ground plane) should be used for the same reasons. A V_{CC} bypass capacitor should be provided at the test socket, also with minimum lead lenghts. Input signals should have rise and fall times of 6 ns, a signal swing of 0 V to V_{CC} for HC and 0 V to 3 V for HCT, 1.0 MHz square wave is recommended for most propagation delay tests. The repetition rate must necessarily be increased for testing f_{max}. Two pulse generators are usually required for testing such parameters as set-up time, hold time, removal time, ect. f_{max} is also tested with 6 ns input rise and fall times, and a repetition time, with a 50% duty factor, but for typical f_{max} as high as 60 MHz, there are no constraints on rise and fall times.

DEFINITIONS OF SYMBOLS AND TERMS USED IN HCMOS DATA SHEETS

Currents

Positive current is defined as conventional current flow into a device.
Negative current is defined as conventional current flow out of a device.

I_{CC} Quiescent power supply current; the current flowing into the V_{CC} supply terminal.

ΔI_{CC} Additional quiescent supply current per input pin at a specified input voltage and V_{CC}.

I_{GND} Quiescent power supply current; the current flowing into the GND terminal.

I_I Input leakage current; the current flowing into a device at a specified input voltage and V_{CC}.

I_{IK} Input diode current; the current flowing into a device at a specified input voltage.

I_O Output source or sink current; the current flowing into a device at a specified output voltage.

I_{OK} Output diode current; the current flowing into a device at a specified output voltage.

I_{OZ} OFF-state output current; the leakage current flowing into the output of a 3-state device in the OFF-state, when the output is connected to V_{CC} or GND.

I_S Analog switch leakage current; the current flowing into an analog switch at a specified voltage across the switch and V_{CC}.

Voltages

All voltages are referenced to GND (ground), which is typically 0 V.

GND Supply voltage; for a device with a single negative power supply, the most negative power supply, used as the reference level for other voltages; typically ground.

V_{CC} Supply voltage; the most positive potential on the device.

V_{EE} Supply voltage; one of two (GND and V_{EE}) negative power supplies.

V_H Hysteresis voltage; difference between the trigger levels, when applying a positive and a negative-going input signal.

V_{IH} HIGH level input voltage ; the range of input voltages that represents a logic HIGH level in the system.

V_{IL} LOW level input voltage; the range of input voltages that represents a logic LOW level in the system.

V_{OH} HIGH level output voltage ; the range of voltages at an output terminal with a specified output loading and supply voltage. Device inputs are conditioned to establish a HIGH level at the output.

V_{OL} LOW level output voltage; the range of voltages at an output terminal with a specified output loading and supply voltage. Device inputs are conditioned to establish a LOW level at the output.

V_{T+} Trigger threshold voltage; positive-going signal.

V_{T-} Trigger threshold voltage; negative-going signal.

Analog terms

R_{ON} ON-resistance; the effective ON-state resistance of an analog switch, at a specified voltage across the switch and output load.

ΔR_{ON} ΔON-resistance; the difference in ON-resistance between any two switches of an analog device at a specified voltage across the switch and output load.

Capacitances

C_I Input capacitance; the capacitance measured at a terminal connected to an input of a device.

$C_{I/O}$ Input/Output capacitance; the capacitance measured at a terminal connected to an I/O-pin (e.g. a transceiver).

C_L Output load capacitance; the capacitance connected to an output terminal including jig and probe capacitance.

C_{PD} Power dissipation capacitance; the capacitance used to determine the dynamic power dissipation per logic function, when no extra load is provided to the device.

C_S Switch capacitance; the capacitance of a terminal to a switch of an analog device.

AC switching parameters

f_i Input frequency; for combinatorial logic devices the maximum number of inputs and outputs switching in accordance with the device function table. For sequential logic devices the clock frequency using alternate HIGH and LOW for data input or using the toggle mode, whichever is applicable.

f_o Output frequency; each output.

f_{max} Maximum clock frequency; clock input waveforms should have a 50% duty factor and be such as to cause the outputs to be switching from 10%V_{CC} to 90%V_{CC} in accordance with the device function table.

t_h Hold time; the interval immediately following the active transition of the timing pulse (usually the clock pulse) or following the transition of the control input to its latching level, during which interval the data to be recognized must be maintained at the input to ensure their continued recognition. A negative hold time indicates that the correct logic level may be released prior to the timing pulse and still be recognized.

t_r, t_f Clock input rise and fall times; 10% and 90% values.

AC switching parameters (continued)

t_{PHL} Propagation delay; the time between the specified reference points, normally the 50% points for PC54/74HC and PC54/74HCU devices on the input and output waveforms and the 1,3 V point for the PC54/74HCT devices, with the output changing from the defined HIGH level to the defined LOW level.

t_{PLH} Propagation delay; the time between the specified reference points, normally the 50% points for PC54/74HC and PC54/74HCU devices on the input and output waveforms and the 1,3 V point for the PC54/74HCT devices, with the output changing from the defined LOW level to the defined HIGH level.

t_{PHZ} 3-state output disable time; the time between the specified reference points, normally the 50% points for the PC54/74HC and PC54/74HCU devices and the 1,3 V points for the PC54/74HCT devices on the output enable input voltage waveform and a point representing 10% of the output swing on the output voltage waveform of a 3-state device, with the output changing from a HIGH level (V_{OH}) to a high impedance OFF-state (Z).

t_{PLZ} 3-state output disable time; the time between the specified reference points, normally the 50% points for the PC54/74HC and PC54/74HCU devices and the 1,3 V points for the PC54/74HCT devices on the output enable input voltage waveform and a point representing 10% of the output swing on the output voltage waveform of a 3-state device, with the output changing from a LOW level (V_{OL}) to a high impedance OFF-state (Z).

t_{PZH} 3-state output enable time; the time between the specified reference points, normally the 50% points for the PC54/74HC devices and the 1,3 V points for the PC54/74HCT devices on the output enable input voltage waveform and the 50% point on the output voltage waveform of a 3-state device, with the output changing from a high impedance OFF-state (Z) to a HIGH level (V_{OH}).

t_{PZL} 3-state output enable time; the time between the specified reference points, normally the 50% points for the PC54/74HC devices and the 1,3 V points for the PC54/74HCT devices on the output enable input voltage waveform and the 50% point on the output voltage waveform of a 3-state device, with the output changing from a high impedance OFF-state (Z) to a LOW level (V_{OL}).

t_{rem} Removal time; the time between the end of an overriding asynchronous input, typically a clear or reset input, and the earliest permissible beginning of a synchronous control input, typically a clock input, normally measured at the 50% points for PC54/74HC and PC54/74HCU devices and the 1,3 V points for the PC54/74HCT devices on both input voltage waveforms.

t_{su} Set-up time; the interval immediately preceding the active transition of the timing pulse (usually the clock pulse) or preceding the transition of the control input to its latching level, during which interval the data to be recognized must be maintained at the input to ensure their recognition. A negative set-up time indicates that the correct logic level may be initiated sometime after the active transition of the timing pulse and still be recognized.

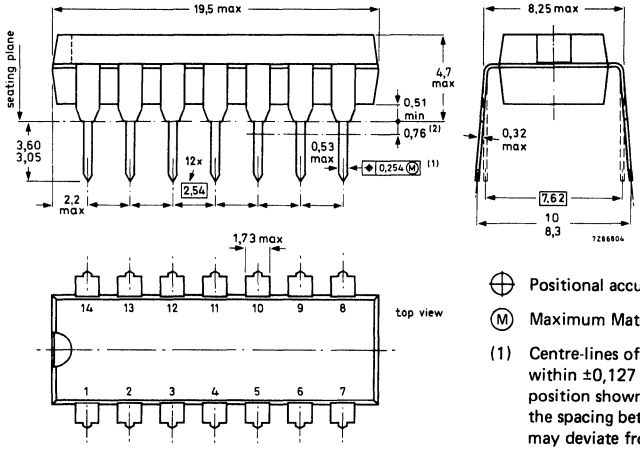
t_{THL} Output transition time; the time between two specified reference points on a waveform, normally 90% and 10% points, that is changing from HIGH-to- LOW.

t_{TLH} Output transition time; the time between two specified reference points on a waveform, normally 10% and 90% points, that is changing from LOW-to- HIGH.

t_w Pulse width; the time between the 50% amplitude points on the leading and trailing edges of a pulse for PC54/74HC and PC54/74HCU devices and at the 1,3 V points for PC54/74HCT devices.

PACKAGE OUTLINES

14-LEAD DUAL IN-LINE; PLASTIC (SOT-27)



Dimensions in mm

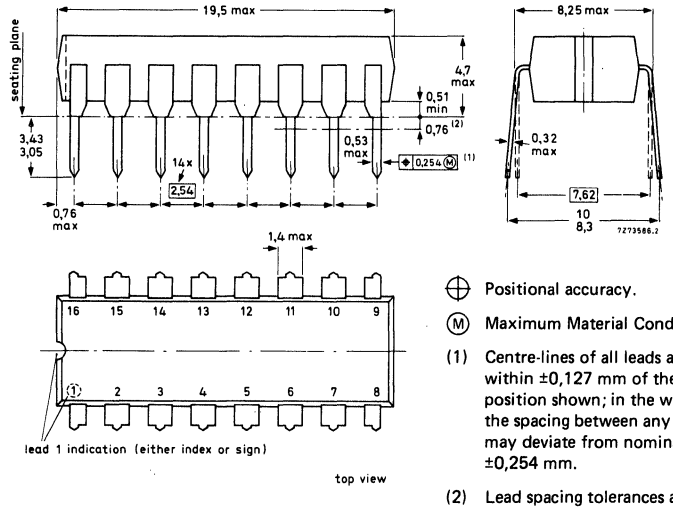
⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

16-LEAD DUAL IN-LINE; PLASTIC (SOT-38Z)



Dimensions in mm

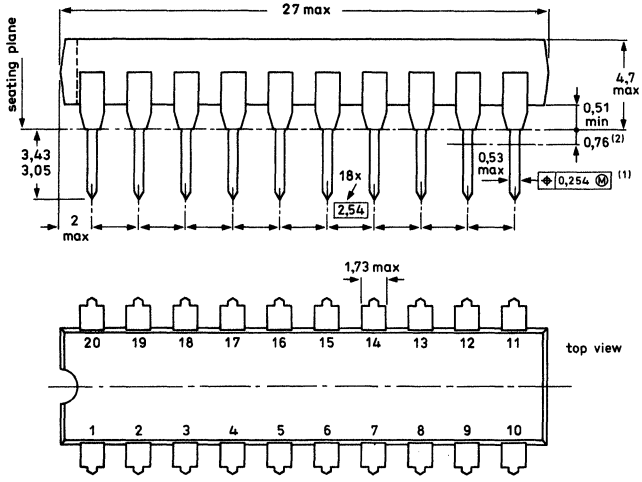
⊕ Positional accuracy.

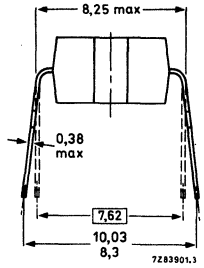
Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

20-LEAD DUAL IN-LINE; PLASTIC (SOT-146)





Dimensions in mm

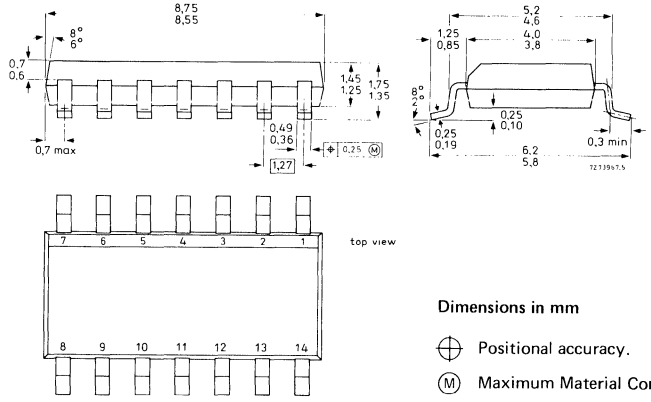
⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

14-LEAD MINI-PACK; PLASTIC (SO-14; SOT-108A)

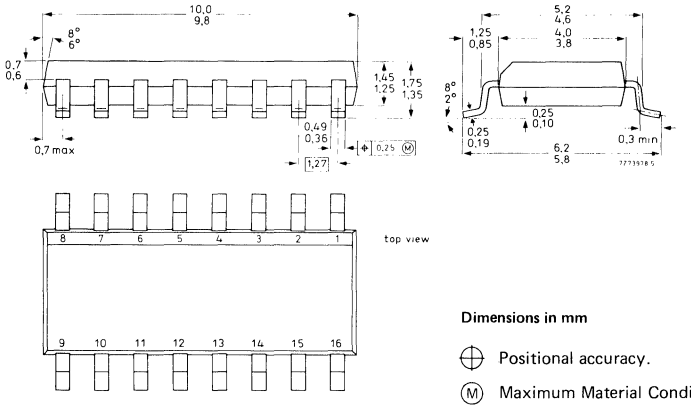


Dimensions in mm

⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

16-LEAD MINI-PACK; PLASTIC (SO-16; SOT-109A)

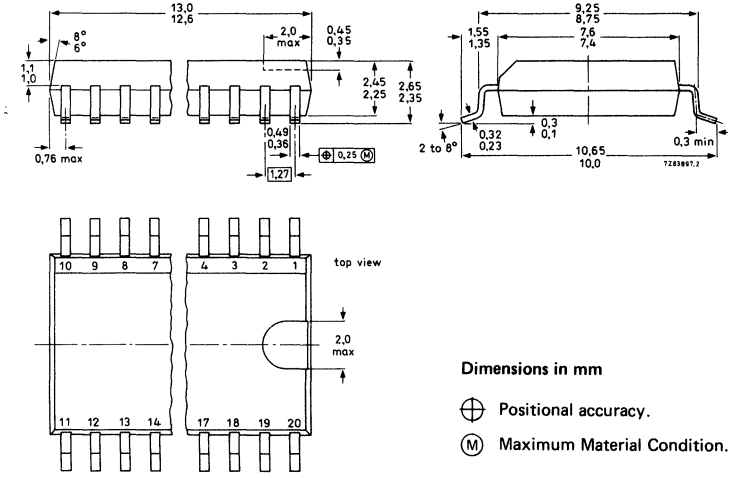


Dimensions in mm

⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

20-LEAD MINI-PACK; PLASTIC (SO-20; SOT-163A)



Dimensions in mm

⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

DEVICE DATA

QUAD 2-INPUT NAND GATE

FEATURES

- **Level shift capability**
- **Output capability: standard (open drain)**
- **I_{CC} category: SSI**

GENERAL DESCRIPTION

The 74HC/HCT03 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7.

The 74HC/HCT03 provide the 2-input NAND function.

The 74HC/HCT03 have open-drain N-transistor outputs, which are not clamped by a diode connected to V_{CC}. In the OFF-state, i.e. when one input is LOW, the output may be pulled to any voltage between GND and V_{Omax}. This allows the device to be used as a LOW-to-HIGH or HIGH-to-LOW level shifter. For digital operation and OR-tied output applications, these devices must have a pull-up resistor to establish a logic HIGH level.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PZL}/ t_{PLZ}	propagation delay	C_L = 15 pF R_L = 1 kΩ V_{CC} = 5 V	8	9	ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per gate	notes 1, 2 and 3	4.0	4.0	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to detemine the dynamic power dissipation (P_D in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o) +$$

$$+ \Sigma (V_O^2 / R_L) \text{ duty factor LOW where:}$$

f_i = input frequency in MHz
f_o = output frequency in MHz
V_O = output voltage in V
$\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
$\Sigma (V_O^2 / R_L)$ = sum of outputs
C_L = output load capacitance in pF
V_{CC} = supply voltage in V
R_L = pull-up resistor in MΩ

2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V
3. The given value of C_{PD} is obtained with:
   C_L = 0 pF and R_L = ∞

ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT03P: 14-lead DIL; plastic (SOT-27).
PC74HC/HCT03T: 14-lead mini-pack; plastic (SO-14; SOT-108A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 4, 9, 12	1A to 4A	data inputs
2, 5, 10, 13	1B to 4B	data inputs
3, 6, 8, 11	1Y to 4Y	data outputs
7	GND	ground (0 V)
14	V_{CC}	positive supply voltage

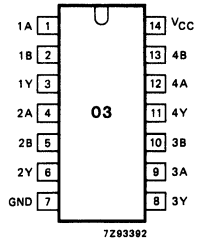


Fig. 1 Pin configuration.

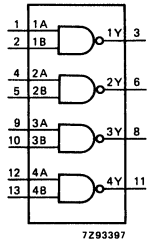


Fig. 2 Logic symbol.

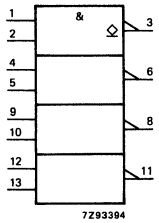


Fig. 3 IEC logic symbol.

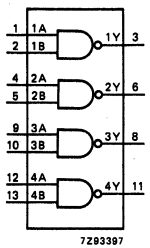


Fig. 4 Functional diagram.

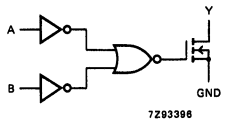


Fig. 5 Logic diagram (one gate).

FUNCTION TABLE

INPUTS		OUTPUT
nA	nB	nY
L	L	Z
L	H	Z
H	L	Z
H	H	L

H = HIGH voltage level
L = LOW voltage level
Z = high impedance OFF-state

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)
Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
V_{CC}	DC supply voltage	−0.5	+7	V	
I_{IK}	DC input diode current		20	mA	for $V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V
$-I_{OK}$	DC output diode current		20	mA	for $V_O < -0.5$ V
$-I_O$	DC output source or sink current		25	mA	for -0.5 V $< V_O$
$\pm I_{CC}$; $\pm I_{GND}$	DC VCC or GND current		50	mA	
T_{stg}	storage temperature range	−65	+150	°C	
P_{tot}	power dissipation per package				for temperature range; −40 to +85 °C 74HC/HCT
	plastic DIL		500	mW	above +60 °C: derate linearly with 8 mW/K
	plastic mini-pack (SO)		400	mW	above +60 °C: derate linearly with 6 mW/K
P_{tot}	power dissipation per package				for temperature range; −40 to +125 °C 74HC/HCT
	plastic DIL		500	mW	above +70 °C: derate linearly with 8 mW/K
	plastic mini-pack (SO)		400	mW	above +70 °C: derate linearly with 6 mW/K

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications", except that the V_{OH} values are not valid for open drain. They are replaced by I_{OH} as given below.

Output capability: standard (open drain), excepting V_{OH}
I_{CC} category: SSI

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		74HCT								V_{CC} V	V_I	OTHER
		+25			−40 to +85		−40 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
I_{OH}	HIGH level output leakage current			0.5		5.0		10.0	μA	2.0 to 6.0	V_{IL}	V_O = 6.0 V

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PZL}/ t_{PLZ}	propagation delay nA, nB to nY			100 20 17		125 25 21		150 30 26	ns	2.0 4.5 6.0	Fig. 6
t_{THL}	output transition time			75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 6

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications", except that the V_{OH} values are not valid for open drain. They are replaced by I_{OH} as given below.

Output capability: standard (open drain), excepting V_{OH}
I_{CC} category: SSI

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		74HCT								V_{CC} V	V_I	OTHER
		+25			−40 to +85		−40 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
I_{OH}	HIGH level output leakage current			0.5		5.0		10.0	μA	4.5 to 5.5	V_{IL}	V_O = 6.0 V

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
nA, nB	1.0

AC CHARACTERISTICS FOR 74HCT

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PZL}/ t_{PLZ}	propagation delay nA, nB, to nY			24		30		36	ns	4.5	Fig. 6
t_{THL}	output transition time			15		19		22	ns	4.5	Fig. 6

AC WAVEFORMS

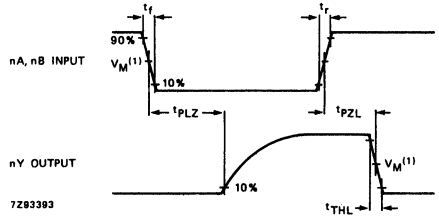


Fig. 6 Waveforms showing the input (nA, nB) to output (nY) propagation delays and the output transition times.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

TEST CIRCUIT AND WAVEFORMS

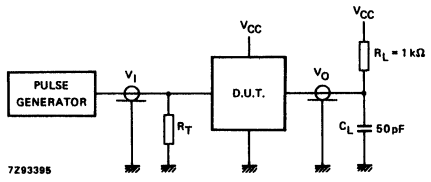


Fig. 7 Test circuit (open drain)

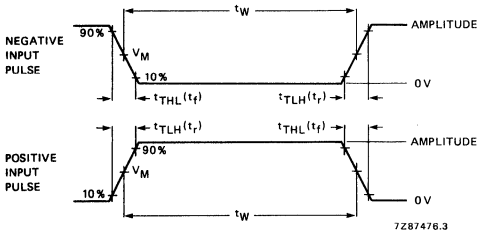


Fig. 8 Input pulse definitions.

Definitions for Figs. 7 and 8:

C_L = load capacitance including jig and probe capacitance (see AC CHARACTERISTICS for values).

R_T = termination resistance should be equal to the output impedance Z_O of the pulse generator.

t_r = t_f = 6 ns; when measuring f_{max}, there is no constraint on t_r, t_f or pulse width.

FAMILY	AMPLITUDE	V_M	t_r; t_f	
			f_{max}; PULSE WIDTH	OTHER
74HC	V_{CC}	50%	< 2 ns	6 ns
74HCT	3.0 V	1.3 V	< 2 ns	6 ns

HEX INVERTER

FEATURES

- **Output capability: standard**
- **I_{CC} category: SSI**

GENERAL DESCRIPTION

The 74HCU04 is a high-speed Si-gate CMOS device and is pin compatible with low power Schottky TTL (LSTTL). It is specified in compliance with JEDEC standard no. 7.

The 74HCU04 is a general purpose hex inverter. Each of the six inverters is a single stage.

FUNCTION TABLE

INPUT	OUTPUT
nA	nY
L	H
H	L

H = HIGH voltage level
L = LOW voltage level

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay nA to nY	C_L = 15 pF; V_{CC} = 5 V	5	ns
C_I	input capacitance		3.5	pF
C_{PD}	power dissipation capacitance per inverter	notes 1 and 2	10	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
2. V_I = GND to V_{CC}

ORDERING INFORMATION/PACKAGE OUTLINES

PC74HCU04P: 14-lead DIL; plastic (SOT-27).
PC74HCU04T: 14-lead mini-pack; plastic (SO-14; SOT-108A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 3, 5, 9, 11, 13	1A to 6A	data inputs
2, 4, 6, 8, 10, 12	1Y to 6Y	data outputs
7	GND	ground (0 V)
14	V_{CC}	positive supply voltage

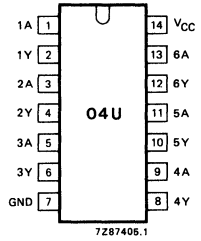


Fig. 1 Pin configuration.

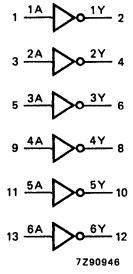


Fig. 2 Logic symbol.

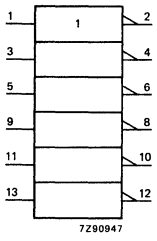


Fig. 3 IEC logic symbol.

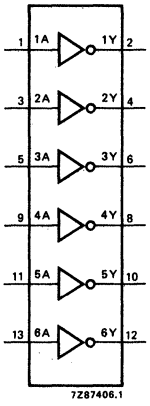


Fig. 4 Functional diagram.

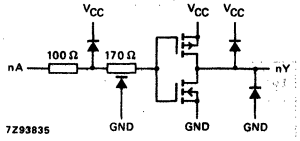


Fig. 5 Schematic diagram (one inverter).

DC CHARACTERISTICS FOR 74HCU

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		74HCU								V_{CC} V	V_I	OTHER
		+25			-40 to +85		-40 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
V_{IH}	HIGH level input voltage	1.7 3.6 4.8			1.7 3.6 4.8		1.7 3.6 4.8		V	2.0 4.5 6.0		
V_{IL}	LOW level input voltage			0.3 0.9 1.2		0.3 0.9 1.2		0.3 0.9 1.2	V	2.0 4.5 6.0		
V_{OH}	HIGH level output voltage	1.8 4.0 5.5			1.8 4.0 5.5		1.8 4.0 5.5		V	2.0 4.5 6.0	V_{IH} or V_{IL}	$-I_O = 20\ \mu A$ $-I_O = 20\ \mu A$ $-I_O = 20\ \mu A$
V_{OH}	HIGH level output voltage	3.98 5.48			3.84 5.34		3.7 5.2		V	4.5 6.0	V_{CC} or GND	$-I_O = 4.0$ mA $-I_O = 5.2$ mA
V_{OL}	LOW level output voltage			0.2 0.5 0.5		0.2 0.5 0.5		0.2 0.5 0.5	V	2.0 4.5 6.0	V_{IH} or V_{IL}	$I_O = 20\ \mu A$ $I_O = 20\ \mu A$ $I_O = 20\ \mu A$
V_{OL}	LOW level output voltage			0.26 0.26		0.33 0.33		0.4 0.4	V	4.5 6.0	V_{CC} or GND	$I_O = 4.0$ mA $I_O = 5.2$ mA
$\pm I_I$	input leakage current			0.1		1.0		1.0	μA	6.0	V_{CC} or GND	
I_{CC}	quiescent supply current			2.0		20.0		40.0	μA	6.0	V_{CC} or GND	$I_O = 0$

AC CHARACTERISTICS FOR 74HCU

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCU								V_{CC} V	WAVEFORMS
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delay nA to nY			70 14 12		90 18 15		105 21 18	ns	2.0 4.5 6.0	Fig. 6
t_{THL}/ t_{TLH}	output transition time			75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 6

AC WAVEFORMS

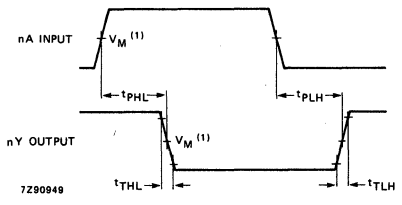


Fig. 6 Waveforms showing the data input (nA) to data output (nY) propagation delays and the output transition times.

Note to AC waveforms

(1) V_M = 50%; V_I = GND to V_{CC}.

TYPICAL TRANSFER CHARACTERISTICS

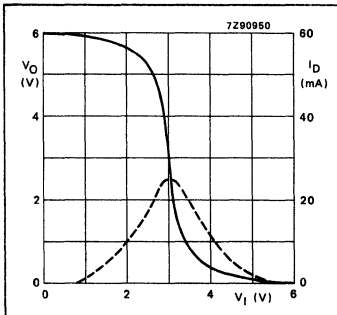


Fig. 7

—— V_O; – – – – I_D (drain current)

I_O = 0; V_{CC} = 6.0 V.

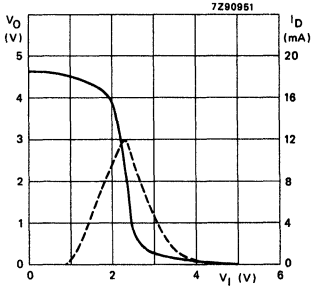


Fig. 8

—— V_O; – – – – I_D (drain current)

I_O = 0; V_{CC} = 4.5 V.

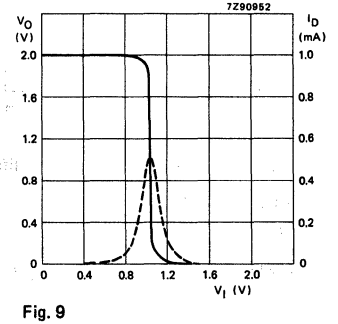


Fig. 9

—— V_O; – – – – I_D (drain current)

I_O = 0; V_{CC} = 2.0 V.

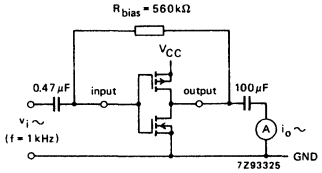


Fig. 10 Test set-up for measuring forward transconductance $g_{fs} = di_o/dv_i$ at v_o is constant (see also graph Fig. 11).

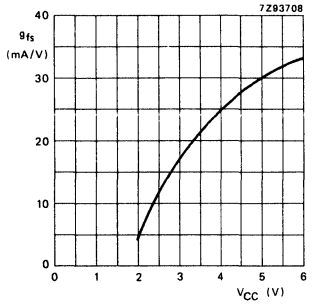


Fig. 11 Typical forward transconductance g_{fs} as a function of the supply voltage V_{CC} at T_{amb} = 25 °C.

APPLICATION INFORMATION

Some applications for the "HCU04" are:

- In crystal oscillator designs (see chapter "Application information").
- Linear amplifier (see Fig. 12).

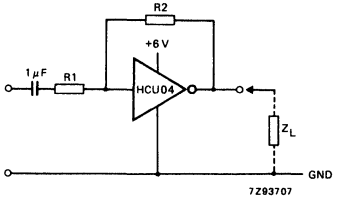


Fig. 12 HCU04 used as a linear amplifier.

Note to Fig. 12

$Z_L > 10$ kΩ; $A_{u\ max} = 20$ (typ.)

Where: $A_u = -\frac{R2}{R1}$; $V_{O\ max\ (p\text{-}p)} \approx V_{CC} - 2$ V centered at ½ V_{CC}

10 kΩ ≤ R1, R2 ≤ 1 MΩ

Typical unity gain bandwidth product is 3 MHz.

QUAD 2-INPUT AND GATE

FEATURES

- Output capability: standard
- I_{CC} category: SSI

GENERAL DESCRIPTION

The 74HC/HCT08 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7.

The 74HC/HCT08 provide the 2-input AND function.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay nA, nB to nY	C_L = 15 pF; V_{CC} = 5 V	7	10	ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per gate	notes 1 and 2	10	20	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

ORDERING INFORMATION/PACKAGE OUTLINES

PC47HC/HCT08P: 14-lead DIL; plastic (SOT-27).
PC74HC/HCT08T: 14-lead mini-pack; plastic (SO-14; SOT-108A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 4, 9, 12	1A to 4A	data inputs
2, 5, 10, 13	1B to 4B	data inputs
3, 6, 8, 11	1Y to 4Y	data outputs
7	GND	ground (0 V)
14	V_{GC}	positive supply voltage

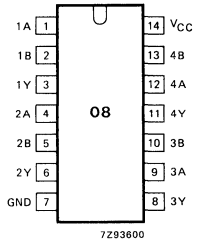


Fig. 1 Pin configuration.

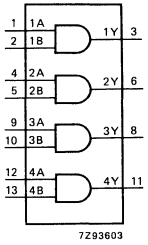


Fig. 2 Logic symbol.

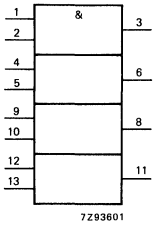


Fig. 3 IEC logic symbol.

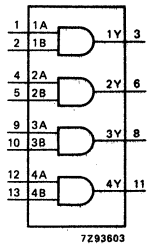


Fig. 4 Functional diagram.

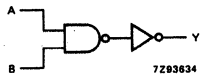


Fig. 5 HC logic diagram (one gate).

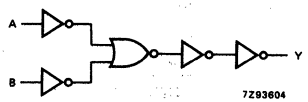


Fig. 6 HCT logic diagram (one gate).

FUNCTION TABLE

INPUTS		OUTPUT
nA	nB	nY
L	L	L
L	H	L
H	L	L
H	H	H

H = HIGH voltage level
L = LOW voltage level

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: SSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	WAVEFORMS
		+25			–40 to +85		–40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delay nA, nB to nY			80 16 14		100 20 17		120 24 20	ns	2.0 4.5 6.0	Fig. 7
t_{THL}/ t_{TLH}	output transition time			75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 7

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: SSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
nA, nB	0.6

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay nA, nB to nY			27		34		41	ns	4.5	Fig. 7
t_{THL}/t_{TLH}	output transition time			15		19		22	ns	4.5	Fig. 7

AC WAVEFORMS

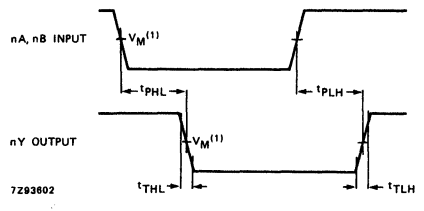


Fig. 7 Waveforms showing the input (nA, nB) to output (nY) propagation delays and the output transition times.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

TRIPLE 3-INPUT NAND GATE

FEATURES

- **Output capability: standard**
- **I_{CC} category: SSI**

GENERAL DESCRIPTION

The 74HC/HCT10 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7.

The 74HC/HCT10 provide the 3-input NAND function.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/ t_{PLH}	propagation delay nA, nB, nC to nY	C_L = 15 pF V_{CC} = 5 V	8	10	ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per gate	notes 1 and 2	12	14	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT10P: 14-lead DIL; plastic (SOT-27).
PC74HC/HCT10T: 14-lead mini-pack; plastic (SO-14; SOT-108A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 3, 9	1A to 3A	data inputs
2, 4, 10	1B to 3B	data inputs
13, 5, 11	1C to 3C	data inputs
12, 6, 8	1Y to 3Y	data outputs
7	GND	ground (0 V)
14	V_{CC}	positive supply voltage

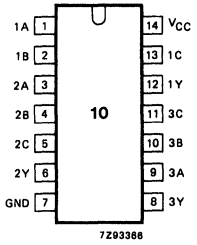


Fig. 1 Pin configuration.

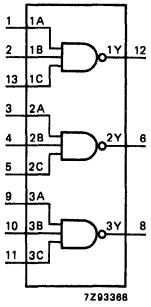


Fig. 2 Logic symbol.

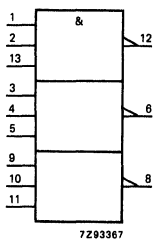


Fig. 3 IEC logic symbol.

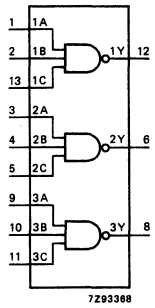


Fig. 4 Functional diagram.

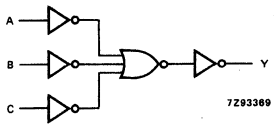


Fig. 5 Logic diagram (one gate).

FUNCTION TABLE

INPUTS			OUTPUT
nA	nB	nC	nY
L	L	L	H
L	L	H	H
L	H	L	H
L	H	H	H
H	L	L	H
H	L	H	H
H	H	L	H
H	H	H	L

H = HIGH voltage level
L = LOW voltage level

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: SSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delay nA, nB, nC to nY			100 20 17		125 25 21		150 30 26	ns	2.0 4.5 6.0	Fig. 6
t_{THL}/ t_{TLH}	output transition time			75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 6

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: SSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
nA, nB, nC	1.5

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay nA, nB, nC to nY			24		30		36	ns	4.5	Fig. 6
t_{THL}/t_{TLH}	output transition time			15		19		22	ns	4.5	Fig. 6

AC WAVEFORMS

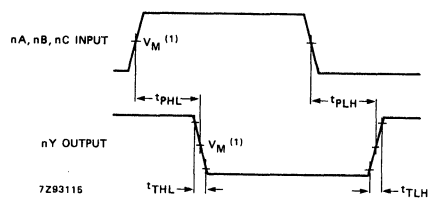


Fig. 6 Waveforms showing the input (nA, nB, nC) to output (nY) propagation delays and the output transition times.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

HEX INVERTING SCHMITT TRIGGER

FEATURES

- **Output capability: standard**
- **I_{CC} category: SSI**

GENERAL DESCRIPTION

The 74HC/HCT14 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7.

The 74HC/HCT14 provide six inverting buffers with Schmitt-trigger action. They are capable of transforming slowly changing input signals into sharply defined, jitter-free output signals.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay nA to nY	C_L = 15 pF; V_{CC} = 5 V	11	16	ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per gate	notes 1 and 2	7.0	8.0	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT14P: 14-lead DIL; plastic (SOT-27).
PC74HC/HCT14T: 14-lead mini-pack; plastic (SO-14; SOT-108A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 3, 5, 9, 11, 13	1A to 6A	data inputs
2, 4, 6, 8, 10, 12	1Y to 6Y	data outputs
7	GND	ground (0 V)
14	V_{CC}	positive supply voltage

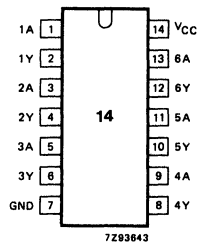


Fig. 1 Pin configuration.

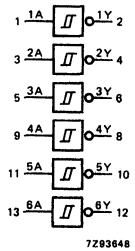


Fig. 2 Logic symbol.

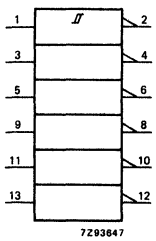


Fig. 3 IEC logic symbol.

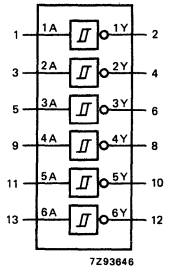


Fig. 4 Functional diagram.

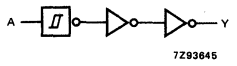


Fig. 5 Logic diagram (one Schmitt trigger).

FUNCTION TABLE

INPUT	OUTPUT
nA	nY
L	H
H	L

H = HIGH voltage level
L = LOW voltage level

APPLICATIONS

- **Wave and pulse shapers**
- **Astable multivibrators**
- **Monostable multivibrators**

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications". Transfer characteristics are given below.

Output capability: standard
I_{CC} category: SSI

Transfer characteristics for 74HC

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
V_{T+}	positive-going threshold	0.7 1.7 2.1		1.5 3.15 4.2	0.7 1.7 2.1	1.5 3.15 4.2	0.7 1.7 2.1	1.5 3.15 4.2	V	2.0 4.5 6.0	Figs 6 and 7
V_{T-}	negative-going threshold	0.3 0.9 1.2		1.0 2.2 3.0	0.3 0.9 1.2	1.0 2.2 3.0	0.3 0.9 1.2	1.0 2.2 3.0	V	2.0 4.5 6.0	Figs 6 and 7
V_H	hysteresis ($V_{T+} - V_{T-}$)	0.2 0.4 0.6		1.0 1.4 1.6	0.2 0.4 0.6	1.0 1.4 1.6	0.2 0.4 0.6	1.0 1.4 1.6	V	2.0 4.5 6.0	Figs 6 and 7

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delay nA, nB to nY			125 25 21		155 31 26		190 38 32	ns	2.0 4.5 6.0	Fig. 8
t_{THL}/ t_{TLH}	output transition time			75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 8

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications". Transfer characteristics are given below.

Output capability: standard
I_{CC} category: SSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
nA	0.3

Transfer characteristics for 74HCT

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
V_{T+}	positive-going threshold	1.2 1.4		1.9 2.1	1.2 1.4	1.9 2.1	1.2 1.4	1.9 2.1	V	4.5 5.5	Figs 6 and 7
V_{T-}	negative-going threshold	0.5 0.6		1.2 1.4	0.5 0.6	1.2 1.4	0.5 0.6	1.2 1.4	V	4.5 5.5	Figs 6 and 7
V_H	hysteresis ($V_{T+} - V_{T-}$)	0.4 0.4		– –	0.4 0.4	– –	0.4 0.4	– –	V	4.5 5.5	Figs 6 and 7

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay nA, nB to nY			38		48		57	ns	4.5	Fig. 8
t_{THL}/t_{TLH}	output transition time			15		19		22	ns	4.5	Fig. 8

TRANSFER CHARACTERISTIC WAVEFORMS

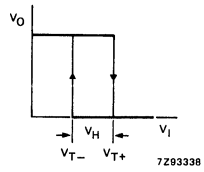


Fig. 6 Transfer characteristic.

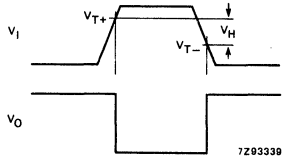


Fig. 7 Waveforms showing the definition of V_{T+}, V_{T-} and V_H; where V_{T+} and V_{T-} are between limits of 20% and 70%.

AC WAVEFORMS

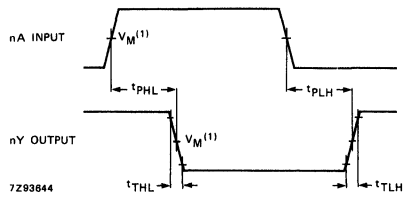


Fig. 8 Waveforms showing the input (nA, nB) to output (nY) propagation delays and the output transition times.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

QUAD BUFFER/LINE DRIVER; 3-STATE

FEATURES

- **Output capability: bus driver**
- **I_{CC} category: MSI**

GENERAL DESCRIPTION

The 74HC/HCT125 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7.

The 74HC/HCT125 are four non-inverting buffer/line drivers with 3-state outputs. The 3-state outputs (nY) are controlled by the output enable input ($n\overline{OE}$). A HIGH at $n\overline{OE}$ causes the outputs to assume a HIGH impedance OFF-state.

The "125" is identical to the "126" but has active LOW enable inputs.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay nA to nY	C_L = 15 pF; V_{CC} = 5 V	8	10	ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per buffer	notes 1 and 2	22	24	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT125P: 14-lead DIL; plastic (SOT-27).
PC74HC/HCT125T: 14-lead mini-pack; plastic (SO-14; SOT-108A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 4, 10, 13	$1\overline{OE}$ to $4\overline{OE}$	output enable inputs (active LOW)
2, 5, 9, 12	1A to 4A	data inputs
3, 6, 8, 11	1Y to 4Y	data outputs
7	GND	ground (0 V)
14	V_{CC}	positive supply voltage

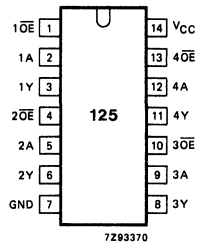


Fig. 1 Pin configuration.

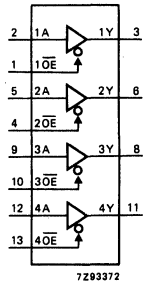


Fig. 2 Logic symbol.

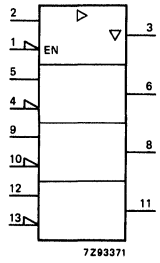


Fig. 3 IEC logic symbol.

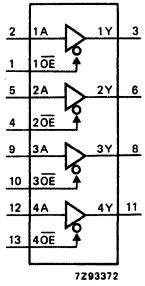


Fig. 4 Functional diagram.

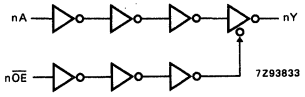


Fig. 5 Logic diagram (one buffer).

FUNCTION TABLE

INPUTS		OUTPUT
$n\overline{OE}$	nA	nY
L	L	L
L	H	H
H	X	Z

H = HIGH voltage level
L = LOW voltage level
X = don't care
Z = high impedance OFF-state

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay nA to nY			100 20 17		125 25 21		150 30 26	ns	2.0 4.5 6.0	Fig. 6
t_{PZH}/t_{PZL}	3-state output enable time $n\overline{OE}$ to nY			150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 7
t_{PHZ}/t_{PLZ}	3-state output disable time $n\overline{OE}$ to nY			150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 7
t_{THL}/t_{TLH}	output transition time			60 12 10		75 15 13		90 18 15	ns	2.0 4.5 6.0	Fig. 6

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver
I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
nA, $n\overline{OE}$	1.00

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay nA to nY			26		33		39	ns	4.5	Fig. 6
t_{PZH}/t_{PZL}	3-state output enable time $n\overline{OE}$ to nY			30		38		45	ns	4.5	Fig. 7
t_{PHZ}/t_{PLZ}	3-state output disable time $n\overline{OE}$ to nY			30		38		45	ns	4.5	Fig. 7
t_{THL}/t_{TLH}	output transition time			12		15		18	ns	4.5	Fig. 6

AC WAVEFORMS

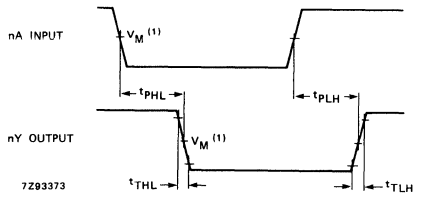


Fig. 6 Waveforms showing the input (nA) to output (nY) propagation delays and the output transition times.

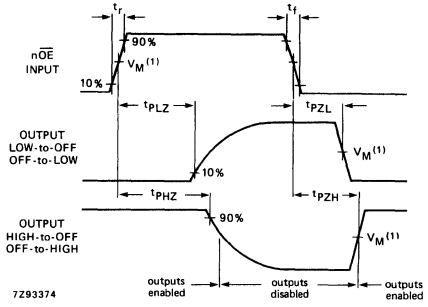


Fig. 7 Waveforms showing the 3-state enable and disable times.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

QUAD BUFFER/LINE DRIVER; 3-STATE

FEATURES

- **Output capability: bus driver**
- **I_{CC} category: MSI**

GENERAL DESCRIPTION

The 74HC/HCT126 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7.

The HC/HCT126 are four non-inverting buffer/line drivers with 3-state outputs. The 3-state outputs (nY) are controlled by the output enable input (nOE). A LOW at nOE causes the outputs to assume a HIGH impedance OFF-state.

The "126" is identical to the "125" but has active HIGH enable inputs.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay nA to nY	C_L = 15 pF; V_{CC} = 5 V	8	10	ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per buffer	notes 1 and 2	22	24	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT126P: 14-lead DIL; plastic (SOT-27).
PC74HC/HCT126T: 14-lead mini-pack; plastic (SO-14; SOT-108A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 4, 10, 13	1OE to 4OE	output enable inputs (active HIGH)
2, 5, 9, 12	1A to 4A	data inputs
3, 6, 8, 11	1Y to 4Y	data outputs
7	GND	ground (0 V)
14	V_{CC}	positive supply voltage

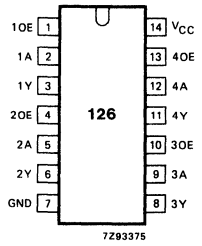


Fig. 1 Pin configuration.

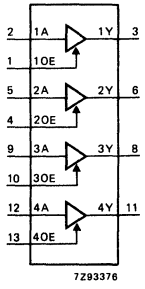


Fig. 2 Logic symbol.

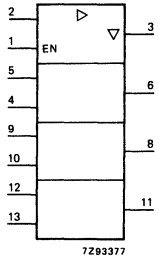


Fig. 3 IEC logic symbol.

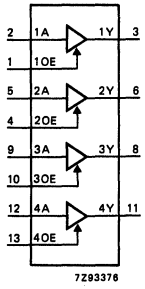


Fig. 4 Functional diagram.

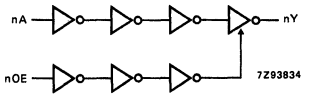


Fig. 5 Logic diagram (one buffer).

FUNCTION TABLE

INPUTS		OUTPUT
nOE	nA	nY
H	L	L
H	H	H
L	X	Z

H = HIGH voltage level
L = LOW voltage level
X = don't care
Z = high impedance OFF-state

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay nA to nY			100 20 17		125 25 21		150 30 26	ns	2.0 4.5 6.0	Fig. 6
t_{PZH}/t_{PZL}	3-state output enable time nOE to nY			150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 7
t_{PHZ}/t_{PLZ}	3-state output disable time nOE to nY			150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 7
t_{THL}/t_{TLH}	output transition time			60 12 10		75 15 13		90 18 15	ns	2.0 4.5 6.0	Fig. 6

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver
I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
nA, nOE	1.00

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay nA to nY			26		33		39	ns	4.5	Fig. 6
t_{PZH}/t_{PZL}	3-state output enable time nOE to nY			35		44		53	ns	4.5	Fig. 7
t_{PHZ}/t_{PLZ}	3-state output disable time nOE to nY			26		33		39	ns	4.5	Fig. 7
t_{THL}/t_{TLH}	output transition time			12		15		18	ns	4.5	Fig. 6

AC WAVEFORMS

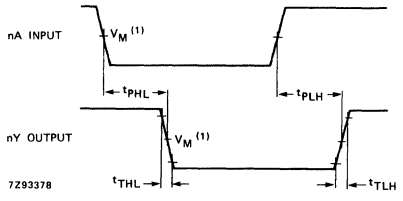


Fig. 6 Waveforms showing the input (nA) to output (nY) propagation delays and the output transition times.

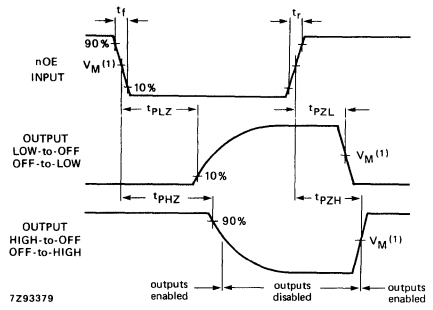


Fig. 7 Waveforms showing the 3-state enable and disable times.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

QUAD 2-INPUT NAND SCHMITT TRIGGER

FEATURES

- **Output capability: standard**
- **I_{CC} category: SSI**

GENERAL DESCRIPTION

The 74HC/HCT132 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7.

The 74HC/HCT132 contain four 2-input NAND gates which accept standard input signals. They are capable of transforming slowly changing input signals into sharply defined, jitter-free output signals.

The gate switches at different points for positive and negative-going signals. The difference between the positive voltage V_{T+} and the negative voltage V_{T-} is defined as the hysteresis voltage V_H.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay nA, nB to nY	C_L = 15 pF; V_{CC} = 5 V	10	16	ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per gate	notes 1 and 2	24	20	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT132P: 14-lead DIL; plastic (SOT-27).
PC74HC/HCT132T: 14-lead mini-pack; plastic (SO-14; SOT-108A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 4, 9, 12	1A to 4A	data inputs
2, 5, 10, 13	1B to 4B	data inputs
3, 6, 8, 11	1Y to 4Y	data outputs
7	GND	ground (0 V)
14	V_{CC}	positive supply voltage

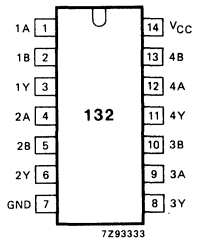


Fig. 1 Pin configuration.

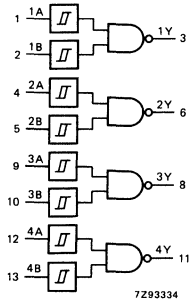


Fig. 2 Logic symbol.

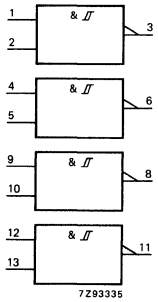


Fig. 3 IEC logic symbol.

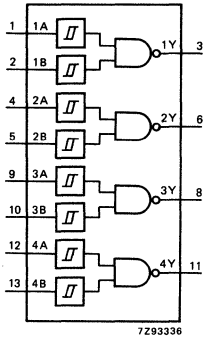


Fig. 4 Functional diagram.

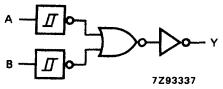


Fig. 5 Logic diagram (one Schmitt trigger).

APPLICATIONS

- Wave and pulse shapers
- Astable multivibrators
- Monostable multivibrators

FUNCTION TABLE

INPUTS		OUTPUT
nA	nB	nY
L	L	H
L	H	H
H	L	H
H	H	L

H = HIGH voltage level
L = LOW voltage level

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications". Transfer characteristics are given below.

Output capability: standard
I_{CC} category: SSI

Transfer characteristics for 74HC

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
V_{T+}	positive-going threshold	0.7 1.7 2.1		1.5 3.15 4.2	0.7 1.7 2.1	1.5 3.15 4.2	0.7 1.7 2.1	1.5 3.15 4.2	V	2.0 4.5 6.0	Figs 6 and 7
V_{T-}	negative-going threshold	0.3 0.9 1.2		1.0 2.2 3.0	0.3 0.9 1.2	1.0 2.2 3.0	0.3 0.9 1.2	1.0 2.2 3.0	V	2.0 4.5 6.0	Figs 6 and 7
V_H	hysteresis ($V_{T+} - V_{T-}$)	0.2 0.4 0.6		1.0 1.4 1.6	0.2 0.4 0.6	1.0 1.4 1.6	0.2 0.4 0.6	1.0 1.4 1.6	V	2.0 4.5 6.0	Figs 6 and 7

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delay nA, nB to nY			125 25 21		155 31 26		190 38 32	ns	2.0 4.5 6.0	Fig. 8
t_{THL}/ t_{TLH}	output transition time			75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 8

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications". Transfer characteristics are given below.

Output capability: standard
I_{CC} category: SSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

input	unit load coefficient
nA, nB	0,3

Transfer characteristics for 74HCT

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
V_{T+}	positive-going threshold	1.2 1.4		1.9 2.1	1.2 1.4	1.9 2.1	1.2 1.4	1.9 2.1	V	4.5 5.5	Figs 6 and 7
V_{T-}	negative-going threshold	0.5 0.6		1.2 1.4	0.5 0.6	1.2 1.4	0.5 0.6	1.2 1.4	V	4.5 5.5	Figs 6 and 7
V_H	hysteresis ($V_{T+} - V_{T-}$)	0.4 0.4		– –	0.4 0.4	– –	0.4 0.4	– –	V	4.5 5.5	Figs 6 and 7

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delay nA, nB to nY			33		41		50	ns	4.5	Fig. 8
t_{THL}/ t_{TLH}	output transition time			15		19		22	ns	4.5	Fig. 8

TRANSFER CHARACTERISTIC WAVEFORMS

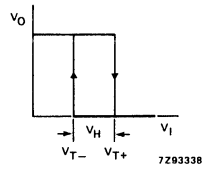


Fig. 6 Transfer characteristic.

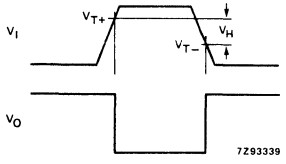


Fig. 7 Waveforms showing the definition of V_{T+}, V_{T-} and V_H; where V_{T+} and V_{T-} are between limits of 20% and 70%.

AC WAVEFORMS

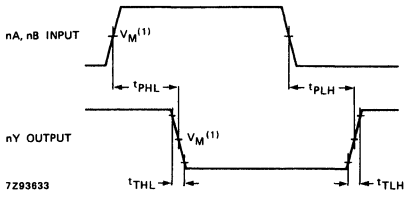


Fig. 8 Waveforms showing the input (nA, nB) to output (nY) propagation delays and the output transition times.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

PRESETTABLE SYNCHRONOUS BCD DECADE COUNTER; ASYNCHRONOUS RESET

FEATURES

- Synchronous counting and loading
- Two count enable inputs for n-bit cascading
- Positive-edge triggered clock
- Asynchronous reset
- Output capability: standard
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT160 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7.

The 74HC/HCT160 are synchronous presettable decade counters which feature an internal look-ahead carry and can be used for high-speed counting. Synchronous operation is provided by having all flip-flops clocked simultaneously on the positive-going edge of the clock (CP).

The outputs (Q_0 to Q_3) of the counters may be preset to a HIGH or LOW level. A LOW level at the parallel enable input ($\overline{PE}$) disables the counting action and causes the data at the data inputs (D_0 to D_3) to be loaded into the counter on the positive-going edge of the clock (providing that the set-up and hold time requirements for $\overline{PE}$ are met). Preset takes place regardless of the levels at count enable inputs (CEP and CET).

(continued on next page)

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}	propagation delay CP to Q_n CP to TC $\overline{MR}$ to Q_n $\overline{MR}$ to TC CET to TC	C_L = 15 pF V_{CC} = 5 V	 18 23 20 23 11	 21 27 23 26 14	 ns ns ns ns ns
t_{PLH}	propagation delay CP to Q_n CP to TC CET to TC		 15 18 11	 16 19 7	 ns ns ns
f_{max}	maximum clock frequency		32	30	MHz
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per package	notes 1 and 2	33	34	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT160P: 16-lead DIL; plastic (SOT-38Z).
PC74HC/HCT160T: 16-lead mini-pack; plastic (SO-16; SOT-109A).

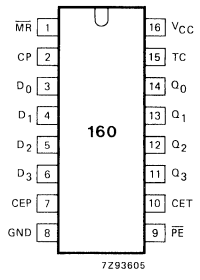


Fig. 1 Pin configuration.

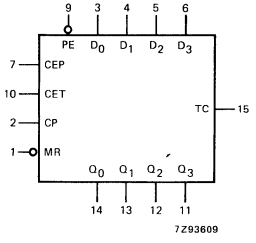


Fig. 2 Logic symbol.

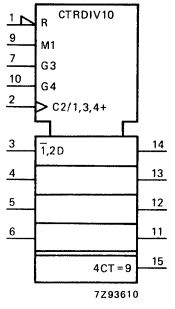


Fig. 3 IEC logic symbol.

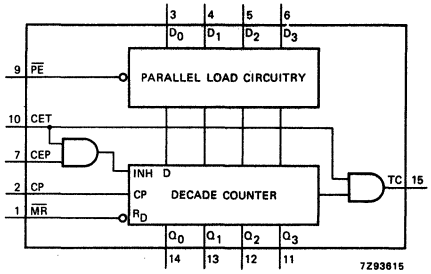


Fig. 4 Functional diagram.

GENERAL DESCRIPTION (Cont'd.)

A LOW level at the master reset input ($\overline{MR}$) sets all four outputs of the flip-flops (Q_0 to Q_3) to LOW level regardless of the levels at CP, $\overline{PE}$, CET and CEP inputs (thus providing an asynchronous clear function).

The look-ahead carry simplifies serial cascading of the counters. Both count enable inputs (CEP and CET) must be HIGH to count. The CET input is fed forward to enable the terminal count output (TC). The TC output thus enabled will produce a HIGH output pulse of a duration approximately equal to a HIGH level output of Q_0. This pulse can be used to enable the next cascaded stage.

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	$\overline{MR}$	asynchronous master reset (active LOW)
2	CP	clock input (LOW-to-HIGH, edge-triggered)
3, 4, 5, 6	D_0 to D_3	data inputs
7	CEP	count enable input
8	GND	ground (0 V)
9	$\overline{PE}$	parallel enable input (active LOW)
10	CET	count enable carry input
14, 13, 12, 11	Q_0 to Q_3	flip-flop outputs
15	TC	terminal count output
16	V_{CC}	positive supply voltage

FUNCTION TABLE

OPERATING MODE	INPUTS						OUTPUTS	
	$\overline{MR}$	CP	CEP	CET	$\overline{PE}$	D_n	Q_n	TC
reset (clear)	L	X	X	X	X	X	L	L
parallel load	H	↑	X	X	l	l	L	L
	H	↑	X	X	l	h	H	*
count	H	↑	h	h	h	X	count	*
hold (do nothing)	H	X	l	X	h	X	q_n	*
	H	X	X	l	h	X	q_n	L

Note to function table

* The TC output is HIGH when CET is HIGH and the counter is at terminal count (HLLH).

H = HIGH voltage level
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition
L = LOW voltage level
l = LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition
q = lower case letters indicate the state of the referenced output one set-up time prior to the LOW-to-HIGH CP transition
X = don't care
↑ = LOW-to-HIGH CP transition

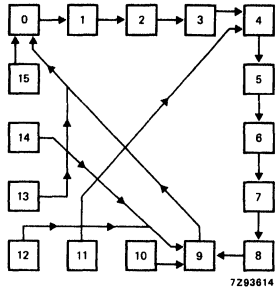


Fig. 5 State diagram.

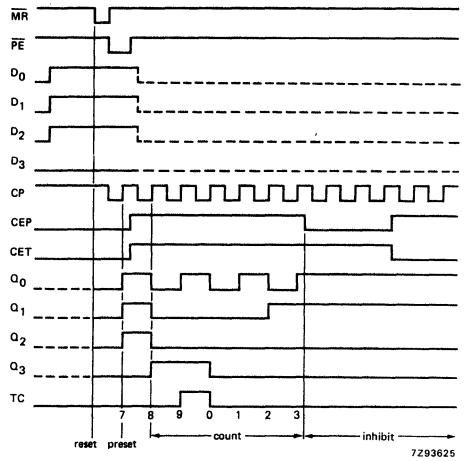


Fig. 6 Typical timing sequence: reset outputs to zero; preset to BCD seven; count to eight, nine, zero, one, two and three; inhibit.

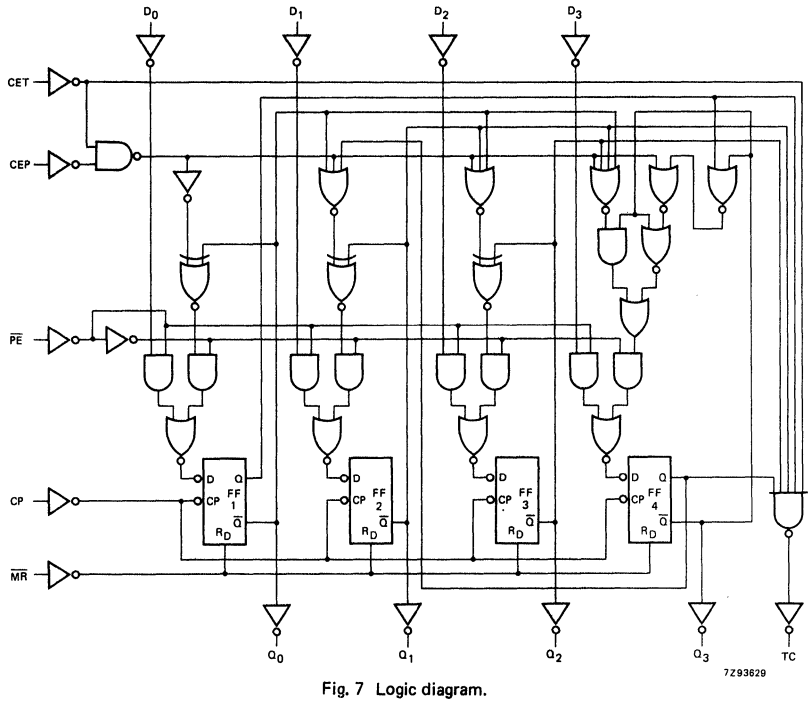


Fig. 7 Logic diagram.

DEVELOPMENT DATA

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay CP to Q_n			205 41 35		255 51 43		310 62 53	ns	2.0 4.5 6.0	Fig. 8
t_{PHL}/t_{PLH}	propagation delay CP to TC			225 45 38		280 56 48		340 68 58	ns	2.0 4.5 6.0	Fig. 8
t_{PHL}	propagation delay $\overline{MR}$ to Q_n			210 42 36		265 53 45		315 63 54	ns	2.0 4.5 6.0	Fig. 9
t_{PHL}	propagation delay $\overline{MR}$ to TC			225 45 38		280 56 48		340 68 58	ns	2.0 4.5 6.0	Fig. 9
t_{PHL}/t_{PLH}	propagation delay CET to TC			150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 10
t_{THL}/t_{TLH}	output transition time			75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Figs 8 and 10
t_W	clock pulse width HIGH or LOW	140 28 24			175 35 30		210 42 36		ns	2.0 4.5 6.0	Fig. 8
t_W	master reset pulse width; LOW	80 16 14			100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 9
t_{rem}	removal time $\overline{MR}$ to CP	100 20 17			125 25 21		150 30 26		ns	2.0 4.5 6.0	Fig. 9
t_{su}	set-up time D_n to CP	100 20 17			125 25 21		150 30 26		ns	2.0 4.5 6.0	Fig. 11
t_{su}	set-up time $\overline{PE}$ to CP	150 30 26			190 38 33		225 45 38		ns	2.0 4.5 6.0	Fig. 11
t_{su}	set-up time CEP, CET to CP	200 40 34			250 50 43		300 60 51		ns	2.0 4.5 6.0	Fig. 12
t_h	hold time D_n, $\overline{PE}$, CEP, CET to CP	0 0 0			0 0 0		0 0 0		ns	2.0 4.5 6.0	Figs 11 and 12
f_{max}	maximum clock pulse frequency	4 18 21			3 14 16		2 12 14		MHz	2.0 4.5 6.0	Fig. 8

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications.
To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
$\overline{MR}$	0.95
CP	0.80
CEP	0.25

INPUT	UNIT LOAD COEFFICIENT
D_n	0.25
CET	1.05
$\overline{PE}$	0.30

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay CP to Q_n			43		54		65	ns	4.5	Fig. 8
t_{PHL}	propagation delay CP to TC			54		68		81	ns	4.5	Fig. 8
t_{PLH}	propagation delay CP to TC			45		56		68	ns	4.5	Fig. 8
t_{PHL}	propagation delay $\overline{MR}$ to Q_n			50		63		75	ns	4.5	Fig. 9
t_{PHL}	propagation delay $\overline{MR}$ to TC			50		63		75	ns	4.5	Fig. 9
t_{PHL}	propagation delay CET to TC			35		44		53	ns	4.5	Fig. 10
t_{PLH}	propagation delay CET to TC			17		21		26	ns	4.5	Fig. 10
t_{THL}/t_{TLH}	output transition time			15		19		22	ns	4.5	Figs 8 and 10
t_W	clock pulse width HIGH or LOW	31			39		47		ns	4.5	Fig. 8
t_W	master reset pulse width; LOW	20			25		30		ns	4.5	Fig. 9
t_{rem}	removal time $\overline{MR}$ to CP	20			25		30		ns	4.5	Fig. 9
t_{su}	set-up time D_n to CP	20			25		30		ns	4.5	Fig. 11
t_{su}	set-up time $\overline{PE}$ to CP	35			44		53		ns	4.5	Fig. 11
t_{su}	set-up time CEP, CET to CP	40			50		60		ns	4.5	Fig. 12
t_h	hold time D_n, $\overline{PE}$, CEP, CET to CP	0			0		0		ns	4.5	Figs 11 and 12
f_{max}	maximum clock pulse frequency	16			13		11		MHz	4.5	Fig. 8

DEVELOPMENT DATA

AC WAVEFORMS

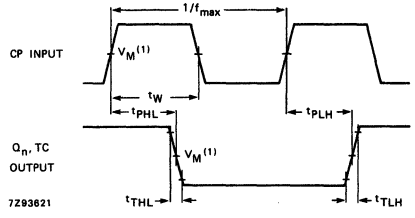


Fig. 8 Waveforms showing the clock (CP) to outputs (Q_n, TC) propagation delays, the clock pulse width, the output transition times and the maximum clock frequency.

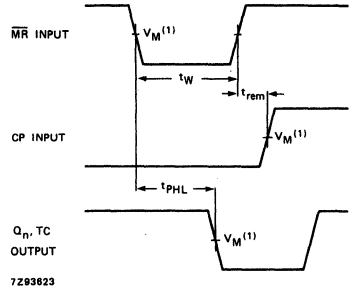


Fig. 9 Waveforms showing the master reset ($\overline{MR}$) pulse width, the master reset to output (Q_n, TC) propagation delays and the master reset to clock (CP) removal time.

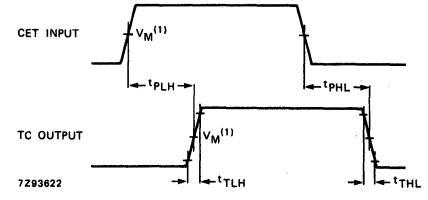


Fig. 10 Waveforms showing the input (CET) to output (TC) propagation delays and output transition times.

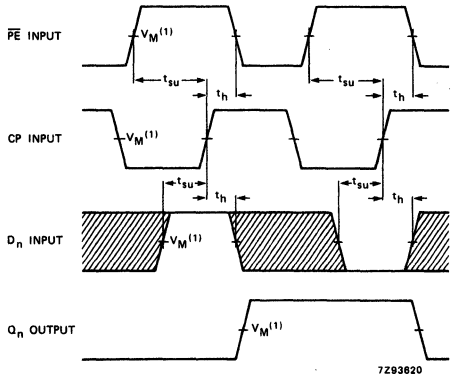


Fig. 11 Waveforms showing the data set-up and hold times for the input (D_n) and parallel enable input $\overline{PE}$.

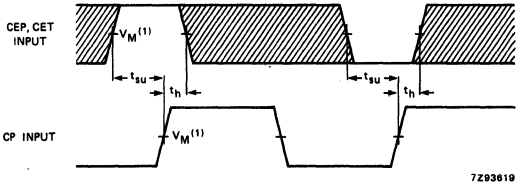


Fig. 12 Waveforms showing the CEP and CET set-up and hold times.

Note to Figs 11 and 12

The shaded areas indicate when the input is permitted to change for predictable output performance.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

PRESETTABLE SYNCHRONOUS 4-BIT BINARY COUNTER; ASYNCHRONOUS RESET

FEATURES

- **Synchronous counting and loading**
- **Two count enable inputs for n-bit cascading**
- **Positive-edge triggered clock**
- **Asynchronous reset**
- **Output capability: standard**
- **I_{CC} category: MSI**

GENERAL DESCRIPTION

The 74HC/HCT161 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7.

The 74HC/HCT161 are synchronous presettable binary counters which feature an internal look-ahead carry and can be used for high-speed counting. Synchronous operation is provided by having all flip-flops clocked simultaneously on the positive-going edge of the clock (CP).

The outputs (Q_0 to Q_3) of the counters may be preset to a HIGH or LOW level. A LOW level at the parallel enable input ($\overline{PE}$) disables the counting action and causes the data at the data inputs (D_0 to D_3) to be loaded into the counter on the positive-going edge of the clock (providing that the set-up and hold time requirements for $\overline{PE}$ are met). Preset takes place regardless of the levels at count enable inputs (CEP and CET).

(continued on next page)

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay CP to Q_n CP to TC $\overline{MR}$ to Q_n $\overline{MR}$ to TC CET to TC	C_L = 15 pF V_{CC} = 5 V	 18 21 19 19 10	 19 24 23 26 14	 ns ns ns ns ns
f_{max}	maximum clock frequency		43	43	MHz
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per package	notes 1 and 2	33	35	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT161P: 16-lead DIL; plastic (SOT-38Z).
PC74HC/HCT161T: 16-lead mini-pack; plastic (SO-16; SOT-109A).

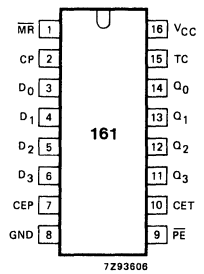


Fig. 1 Pin configuration.

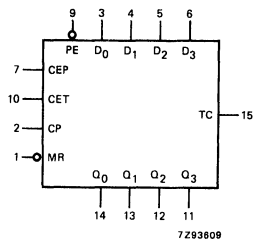


Fig. 2 Logic symbol.

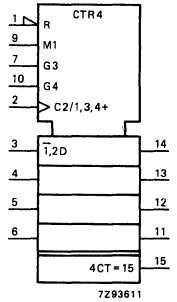


Fig. 3 IEC logic symbol.

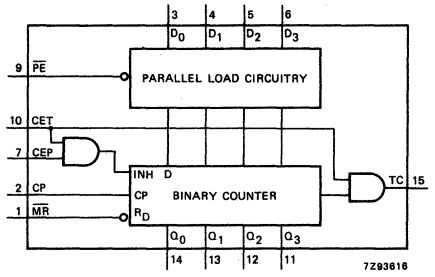


Fig. 4 Functional diagram.

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	$\overline{MR}$	asynchronous master reset (active LOW)
2	CP	clock input (LOW-to-HIGH, edge-triggered)
3, 4, 5, 6	D_0 to D_3	data inputs
7	CEP	count enable input
8	GND	ground (0 V)
9	$\overline{PE}$	parallel enable input (active LOW)
10	CET	count enable carry input
14, 13, 12, 11	Q_0 to Q_3	flip-flop outputs
15	TC	terminal count output
16	V_{CC}	positive supply voltage

FUNCTION TABLE

OPERATING MODE	INPUTS						OUTPUTS	
	$\overline{MR}$	CP	CEP	CET	$\overline{PE}$	D_n	Q_n	TC
reset (clear)	L	X	X	X	X	X	L	L
parallel load	H	↑	X	X	l	l	L	L
	H	↑	X	X	l	h	H	*
count	H	↑	h	h	h	X	count	*
hold (do nothing)	H	X	l	X	h	X	q_n	*
	H	X	X	l	h	X	q_n	L

Note to function table

* The TC output is HIGH when CET is HIGH and the counter is at terminal count (HHHH).

H = HIGH voltage level
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition
L = LOW voltage level
l = LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition
q = lower case letters indicate the state of the referenced output one set-up time prior to the LOW-to-HIGH CP transition
X = don't care
↑ = LOW-to-HIGH CP transition

GENERAL DESCRIPTION (Cont'd.)

A LOW level at the master reset input ($\overline{MR}$) sets all four outputs of the flip-flops (Q_0 to Q_3) to LOW level regardless of the levels at CP, $\overline{PE}$, CET and CEP inputs (thus providing an asynchronous clear function).

The look-ahead carry simplifies serial cascading of the counters. Both count enable inputs (CEP and CET) must be HIGH to count. The CET input is fed forward to enable the terminal count output (TC). The TC output thus enabled will produce a HIGH output pulse of a duration approximately equal to a HIGH level output of Q_0. This pulse can be used to enable the next cascaded stage.

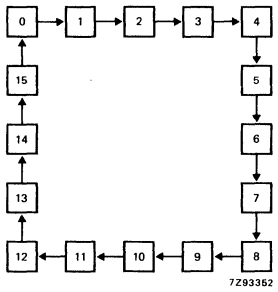


Fig. 5 State diagram.

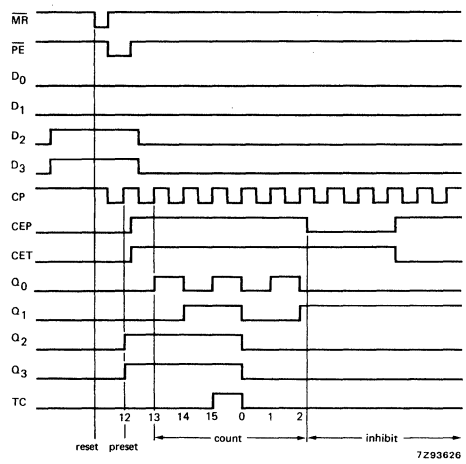


Fig. 6 Typical timing sequence: reset outputs to zero; preset to binary twelve; count to thirteen, fourteen, fifteen, zero, one and two; inhibit.

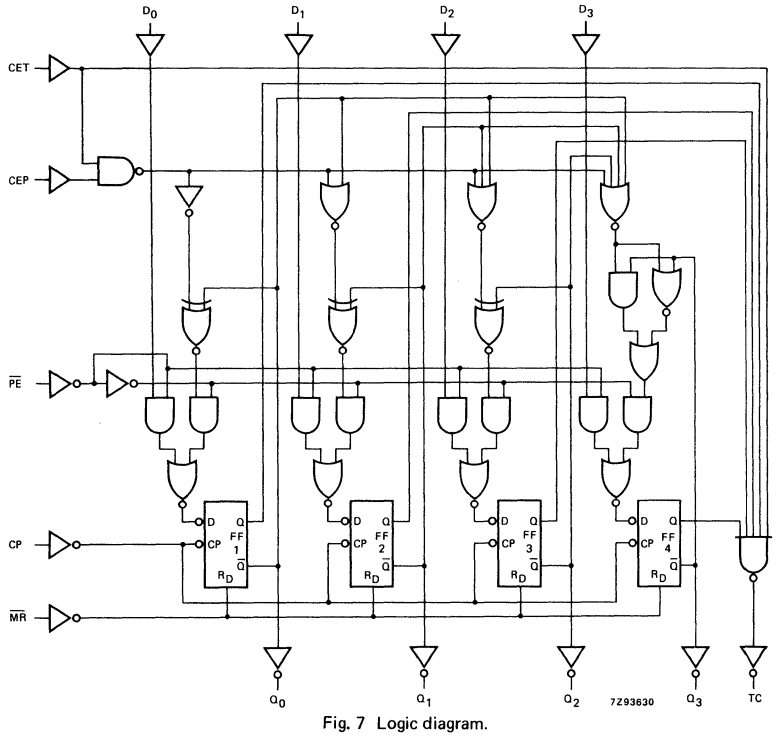


Fig. 7 Logic diagram.

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay CP to Q_n			205 41 35		255 51 43		310 62 53	ns	2.0 4.5 6.0	Fig. 8
t_{PHL}/t_{PLH}	propagation delay CP to TC			225 45 38		280 56 48		340 68 58	ns	2.0 4.5 6.0	Fig. 8
t_{PHL}	propagation delay $\overline{MR}$ to Q_n			225 45 38		280 56 48		340 68 58	ns	2.0 4.5 6.0	Fig. 9
t_{PHL}	propagation delay $\overline{MR}$ to TC			220 44 37		275 55 47		330 66 56	ns	2.0 4.5 6.0	Fig. 9
t_{PHL}/t_{PLH}	propagation delay CET to TC			150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 10
t_{THL}/t_{TLH}	output transition time			75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Figs 8 and 10
t_W	clock pulse width HIGH or LOW	110 22 19			140 28 24		165 33 28		ns	2.0 4.5 6.0	Fig. 8
t_W	master reset pulse width; LOW	100 20 17			125 25 21		150 30 26		ns	2.0 4.5 6.0	Fig. 9
t_{rem}	removal time $\overline{MR}$ to CP	100 20 17			125 25 21		150 30 26		ns	2.0 4.5 6.0	Fig. 9
t_{su}	set-up time D_n to CP	100 20 17			125 25 21		150 30 26		ns	2.0 4.5 6.0	Fig. 11
t_{su}	set-up time $\overline{PE}$ to CP	150 30 26			190 38 33		225 45 38		ns	2.0 4.5 6.0	Fig. 11
t_{su}	set-up time CEP, CET to CP	200 40 34			250 50 43		300 60 51		ns	2.0 4.5 6.0	Fig. 12
t_h	hold time D_n, $\overline{PE}$, CEP, CET to CP	0 0 0			0 0 0		0 0 0		ns	2.0 4.5 6.0	Figs 11 and 12
f_{max}	maximum clock pulse frequency	5 23 27			4 18 21		3 15 18		MHz	2.0 4.5 6.0	Fig. 8

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications.
To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
$\overline{MR}$	0.95
CP	0.80
CEP	0.25

INPUT	UNIT LOAD COEFFICIENT
D_n	0.25
CET	0.75
$\overline{PE}$	0.30

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay CP to Q_n			43		54		65	ns	4.5	Fig. 8
t_{PHL}/t_{PLH}	propagation delay CP to TC			47		59		71	ns	4.5	Fig. 8
t_{PHL}	propagation delay $\overline{MR}$ to Q_n			46		58		69	ns	4.5	Fig. 9
t_{PHL}	propagation delay $\overline{MR}$ to TC			51		64		77	ns	4.5	Fig. 9
t_{PHL}/t_{PLH}	propagation delay CET to TC			35		44		53	ns	4.5	Fig. 10
t_{THL}/t_{TLH}	output transition time			15		19		22	ns	4.5	Figs 8 and 10
t_W	clock pulse width HIGH or LOW	22			28		33		ns	4.5	Fig. 8
t_W	master reset pulse width; LOW	20			25		30		ns	4.5	Fig. 9
t_{rem}	removal time $\overline{MR}$ to CP	20			25		30		ns	4.5	Fig. 9
t_{su}	set-up time D_n to CP	20			25		30		ns	4.5	Fig. 11
t_{su}	set-up time $\overline{PE}$ to CP	35			44		53		ns	4.5	Fig. 11
t_{su}	set-up time CEP, CET to CP	40			50		60		ns	4.5	Fig. 12
t_h	hold time D_n, $\overline{PE}$, CEP, CET to CP	0			0		0		ns	4.5	Figs 11 and 12
f_{max}	maximum clock pulse frequency	23			18		15		MHz	4.5	Fig. 8

AC WAVEFORMS

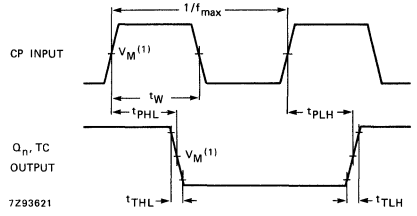


Fig. 8 Waveforms showing the clock (CP) to outputs (Q_n, TC) propagation delays, the clock pulse width, the output transition times and the maximum clock frequency.

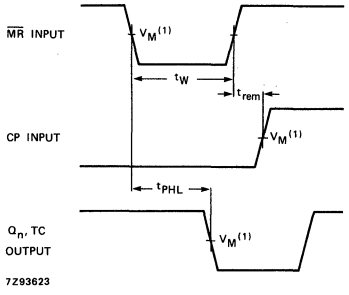


Fig. 9 Waveforms showing the master reset ($\overline{MR}$) pulse width, the master reset to output (Q_n, TC) propagation delays and the master reset to clock (CP) removal time.

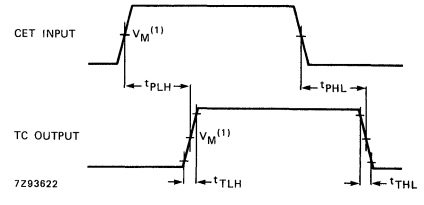


Fig. 10 Waveforms showing the input (CET) to output (TC) propagation delays and output transition times.

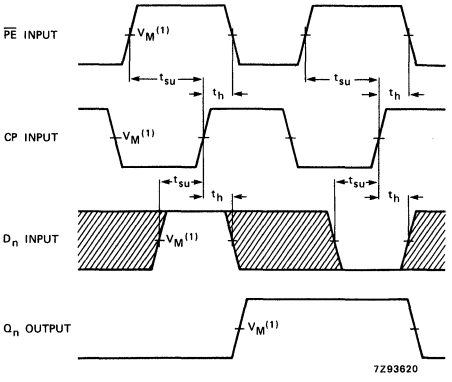


Fig. 11 Waveforms showing the set-up and hold times for the input (D_n) and parallel enable input $\overline{PE}$.

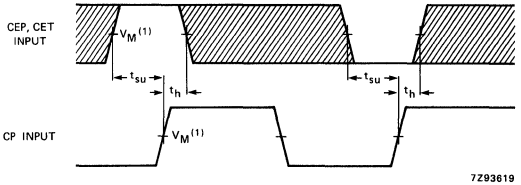


Fig. 12 Waveforms showing the CEP and CET set-up and hold times.

Note to Figs 11 and 12

The shaded areas indicate when the input is permitted to change for predictable output performance.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

PRESETTABLE SYNCHRONOUS BCD DECADE COUNTER; SYNCHRONOUS RESET

FEATURES

- Synchronous counting and loading
- Two count enable inputs for n-bit cascading
- Positive-edge triggered clock
- Synchronous reset
- Output capability: standard
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT162 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7.

The 74HC/HCT162 are synchronous presettable decade counters which feature an internal look-ahead carry and can be used for high-speed counting. Synchronous operation is provided by having all flip-flops clocked simultaneously on the positive-going edge of the clock (CP).

The outputs (Q_0 to Q_3) of the counters may be preset to a HIGH or LOW level. A LOW level at the parallel enable input ($\overline{PE}$) disables the counting action and causes the data at the data inputs (D_0 to D_3) to be loaded into the counter on the positive-going edge of the clock (providing that the set-up and hold time requirements for $\overline{PE}$ are met). Preset takes place regardless of the levels at count enable inputs (CEP and CET).

For the "162" the clear function is synchronous.

(continued on next page)

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}	propagation delay CP to Q_n CP to TC CET to TC	C_L = 15 pF V_{CC} = 5 V	 18 23 11	 20 26 15	 ns ns ns
t_{PLH}	propagation delay CP to Q_n CP to TC CET to TC		 15 18 11	 15 18 9	 ns ns ns
f_{max}	maximum clock frequency		32	30	MHz
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per package	notes 1 and 2	28	28	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT162P: 16-lead DIL; plastic (SOT-38Z).
PC74HC/HCT162T: 16-lead mini-pack; plastic (SO-16; SOT-109A).

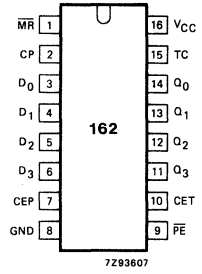


Fig. 1 Pin configuration.

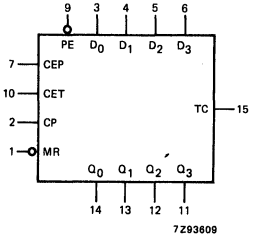


Fig. 2 Logic symbol.

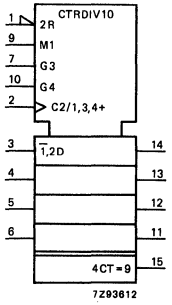


Fig. 3 IEC logic symbol.

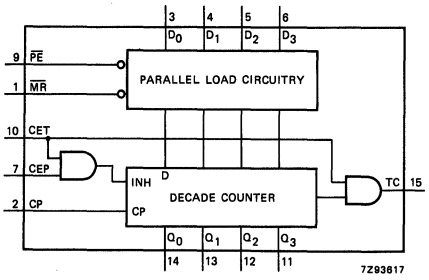


Fig. 4 Functional diagram.

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	$\overline{MR}$	synchronous master reset (active LOW)
2	CP	clock input (LOW-to-HIGH, edge-triggered)
3, 4, 5, 6	D_0 to D_3	data inputs
7	CEP	count enable input
8	GND	ground (0 V)
9	$\overline{PE}$	parallel enable input (active LOW)
10	CET	count enable carry input
14, 13, 12, 11	Q_0 to Q_3	flip-flop outputs
15	TC	terminal count output
16	V_{CC}	positive supply voltage

FUNCTION TABLE

OPERATING MODE	INPUTS						OUTPUTS	
	$\overline{MR}$	CP	CEP	CET	$\overline{PE}$	D_n	Q_n	TC
reset (clear)	l	↑	X	X	X	X	L	L
parallel load	h	↑	X	X	l	l	L	L
	h	↑	X	X	l	h	H	*
count	h	↑	h	h	h	X	count	*
hold (do nothing)	h	X	l	X	h	X	q_n	*
	h	X	X	l	h	X	q_n	L

Note to function table

* The TC output is HIGH when CET is HIGH and the counter is at terminal count (HLLH).

H = HIGH voltage level
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition
L = LOW voltage level
l = LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition
q = lower case letters indicate the state of the referenced output one set-up time prior to the LOW-to-HIGH CP transition
X = don't care
↑ = LOW-to-HIGH CP transition

GENERAL DESCRIPTION (Cont'd.)

A LOW level at the master reset input ($\overline{MR}$) sets all four outputs of the flip-flops (Q_0 to Q_3) to LOW level after the next positive-going transition on the clock (CP) input (provided that the set-up and hold time requirements for $\overline{MR}$ are met). This action occurs regardless of the levels at $\overline{PE}$, CET and CEP inputs.
This synchronous reset feature enables the designer to modify the maximum count with only one external NAND gate.

The look-ahead carry simplifies serial cascading of the counters. Both count enable inputs (CEP and CET) must be HIGH to count. The CET input is fed forward to enable the terminal count output (TC). The TC output thus enabled will produce a HIGH output pulse of a duration approximately equal to a HIGH level output of Q_0. This pulse can be used to enable the next cascaded stage.

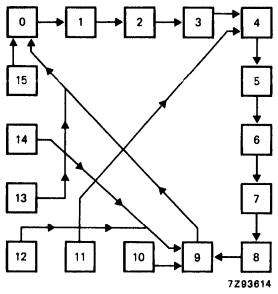


Fig. 5 State diagram.

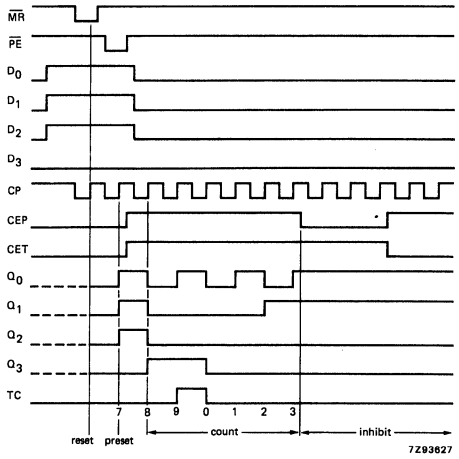


Fig. 6 Typical timing sequence: reset outputs to zero; preset to BCD seven; count to eight, nine, zero, one, two and three; inhibit.

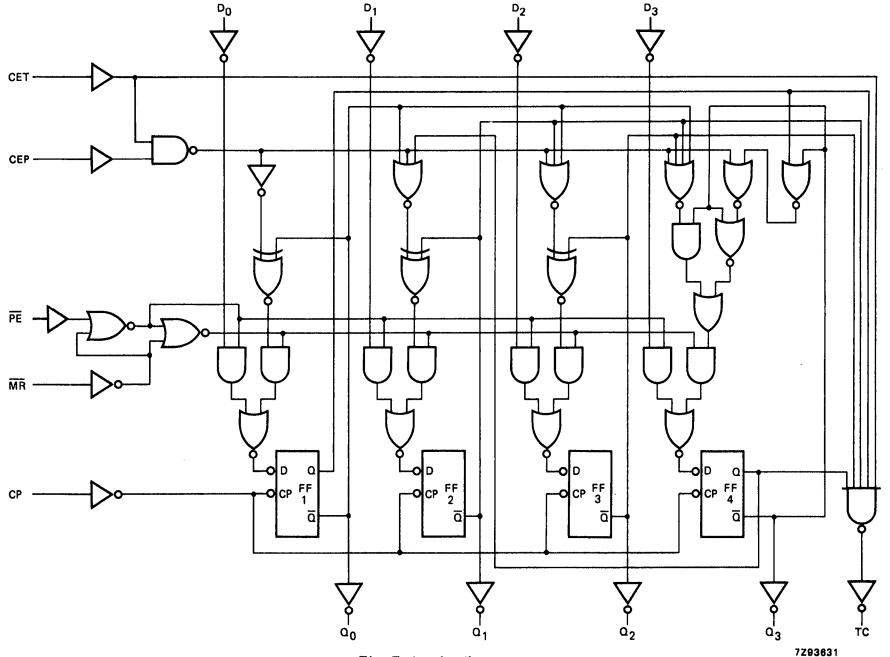


Fig. 7 Logic diagram.

DEVELOPMENT DATA

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delay CP to Q_n			205 41 35		255 51 43		310 62 53	ns	2.0 4.5 6.0	Fig. 8
t_{PHL}/ t_{PLH}	propagation delay CP to TC			225 45 38		280 56 48		340 68 58	ns	2.0 4.5 6.0	Fig. 8
t_{PHL}/ t_{PLH}	propagation delay CET to TC			150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 9
t_{THL}/ t_{TLH}	output transition time			75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Figs 8 and 9
t_W	clock pulse width HIGH or LOW	140 28 24			175 35 30		210 42 36		ns	2.0 4.5 6.0	Fig. 8
t_{su}	set-up time $\overline{MR}$, D_n to CP	100 20 17			125 25 21		150 30 26		ns	2.0 4.5 6.0	Figs 10 and 11
t_{su}	set-up time $\overline{PE}$ to CP	150 30 26			190 38 33		225 45 38		ns	2.0 4.5 6.0	Fig. 10
t_{su}	set-up time CEP, CET to CP	200 40 34			250 50 43		300 60 51		ns	2.0 4.5 6.0	Fig. 12
t_h	hold time D_n, $\overline{PE}$, CEP, CET, $\overline{MR}$ to CP	0 0 0			0 0 0		0 0 0		ns	2.0 4.5 6.0	Figs 10, 11 and 12
f_{max}	maximum clock pulse frequency	4 18 21			3 14 16		2 12 14		MHz	2.0 4.5 6.0	Fig. 8

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
$\overline{MR}$	0.95
CP	0.80
CEP	0.25

INPUT	UNIT LOAD COEFFICIENT
D_n	0.25
CET	1.05
$\overline{PE}$	0.30

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay CP to Q_n			43		54		65	ns	4.5	Fig. 8
t_{PHL}	propagation delay CP to TC			51		64		77	ns	4.5	Fig. 8
t_{PLH}	propagation delay CP to TC			45		56		68	ns	4.5	Fig. 8
t_{PHL}	propagation delay CET to TC			35		44		53	ns	4.5	Fig. 9
t_{PLH}	propagation delay CET to TC			24		30		36	ns	4.5	Fig. 9
t_{THL}/t_{TLH}	output transition time			15		19		22	ns	4.5	Figs 8 and 9
t_W	clock pulse width HIGH or LOW	31			39		47		ns	4.5	Fig. 8
t_{su}	set-up time D_n to CP	20			25		30		ns	4.5	Fig. 10
t_{su}	set-up time $\overline{PE}$ to CP	35			44		53		ns	4.5	Fig. 10
t_{su}	set-up time CEP, CET to CP	40			50		60		ns	4.5	Fig. 12
t_{su}	set-up time $\overline{MR}$ to CP	20			25		30		ns	4.5	Fig. 11
t_h	hold time D_n, $\overline{PE}$, CEP, CET, $\overline{MR}$ to CP	0			0		0		ns	4.5	Figs 10, 11 and 12
f_{max}	maximum clock pulse frequency	16			13		11		MHz	4.5	Fig. 8

DEVELOPMENT DATA

AC WAVEFORMS

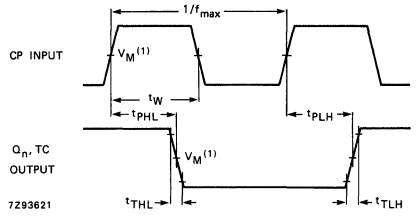


Fig. 8 Waveforms showing the clock (CP) to outputs (Q_n, TC) propagation delays, the clock pulse width, the output transition times and the maximum clock frequency.

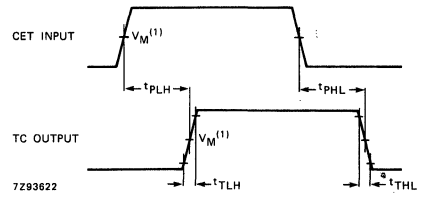


Fig. 9 Waveforms showing the input (CET) to output (TC) propagation delays and output transition times.

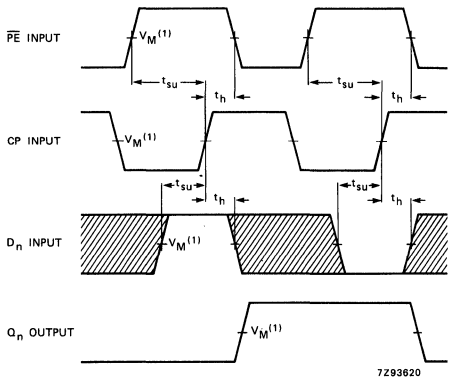


Fig. 10 Waveforms showing the set-up and hold times for the input (D_n) and parallel enable input ($\overline{PE}$).

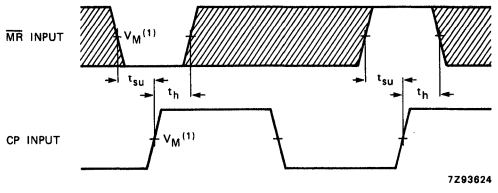


Fig. 11 Waveforms showing the $\overline{MR}$ set-up and hold times.

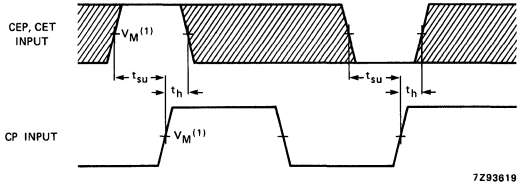


Fig. 12 Waveforms showing the CEP and CET set-up and hold times.

Note to Figs 10, 11 and 12

The shaded areas indicate when the input is permitted to change for predictable output performance.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

PRESETTABLE SYNCHRONOUS 4-BIT BINARY COUNTER; SYNCHRONOUS RESET

FEATURES

- Synchronous counting and loading
- Two count enable inputs for n-bit cascading
- Positive-edge triggered clock
- Synchronous reset
- Output capability: standard
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT163 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7.

The 74HC/HCT163 are synchronous presettable binary counters which feature an internal look-ahead carry and can be used for high-speed counting. Synchronous operation is provided by having all flip-flops clocked simultaneously on the positive-going edge of the clock (CP).
The outputs (Q_0 to Q_3) of the counters may be preset to a HIGH or LOW level. A LOW level at the parallel enable input ($\overline{PE}$) disables the counting action and causes the data at the data inputs (D_0 to D_3) to be loaded into the counter on the positive-going edge of the clock (providing that the set-up and hold time requirements for $\overline{PE}$ are met). Preset takes place regardless of the levels at count enable inputs (CEP and CET).

For the "163" the clear function is synchronous.

(continued on next page)

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay CP to Q_n CP to TC CET to TC	C_L = 15 pF V_{CC} = 5 V	 17 21 10	 19 25 14	 ns ns ns
f_{max}	maximum clock frequency		50	49	MHz
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per package	notes 1 and 2	20	22	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to $V_{CC} - 1.5$ V

ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT163P: 16-lead DIL; plastic (SOT-38Z).
PC74HC/HCT163T: 16-lead mini-pack; plastic (SO-16; SOT-109A).

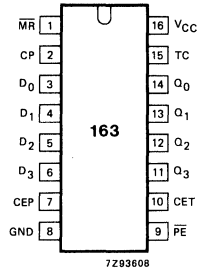


Fig. 1 Pin configuration.

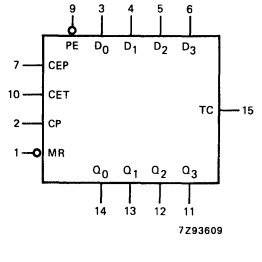


Fig. 2 Logic symbol.

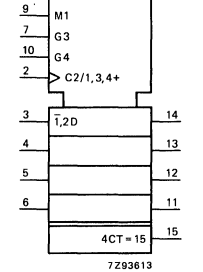


Fig. 3 IEC logic symbol.

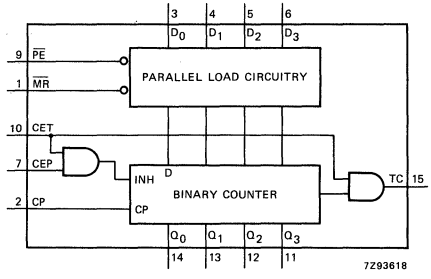


Fig. 4 Functional diagram.

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	$\overline{MR}$	synchronous master reset (active LOW)
2	CP	clock input (LOW-to-HIGH, edge-triggered)
3, 4, 5, 6	D_0 to D_3	data inputs
7	CEP	count enable input
8	GND	ground (0 V)
9	$\overline{PE}$	parallel enable input (active LOW)
10	CET	count enable carry input
14, 13, 12, 11	Q_0 to Q_3	flip-flop outputs
15	TC	terminal count output
16	V_{CC}	positive supply voltage

FUNCTION TABLE

OPERATING MODE	INPUTS						OUTPUTS	
	$\overline{MR}$	CP	CEP	CET	$\overline{PE}$	D_n	Q_n	TC
reset (clear)	l	↑	X	X	X	X	L	L
parallel load	h	↑	X	X	l	l	L	L
	h	↑	X	X	l	h	H	*
count	h	↑	h	h	h	X	count	*
hold (do nothing)	h	X	l	X	h	X	q_n	*
	h	X	X	l	h	X	q_n	L

Note to function table

* The TC output is HIGH when CET is HIGH and the counter is at terminal count (HHHH).

H = HIGH voltage level
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition
L = LOW voltage level
l = LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition
q = lower case letters indicate the state of the referenced output one set-up time prior to the LOW-to-HIGH CP transition
X = don't care
↑ = LOW-to-HIGH CP transition

GENERAL DESCRIPTION (Cont'd)

A LOW level at the master reset input ($\overline{MR}$) sets all four outputs of the flip-flops (Q_0 to Q_3) to LOW level after the next positive-going transition on the clock (CP) input (provided that the set-up and hold time requirements for $\overline{MR}$ are met). This action occurs regardless of the levels at $\overline{PE}$, CET and CEP inputs.
This synchronous reset feature enables the designer to modify the maximum count with only one external NAND gate.

The look-ahead carry simplifies serial cascading of the counters. Both count enable inputs (CEP and CET) must be HIGH to count. The CET input is fed forward to enable the terminal count output (TC). The TC output thus enabled will produce a HIGH output pulse of a duration approximately equal to a HIGH level output of Q_0. This pulse can be used to enable the next cascaded stage.

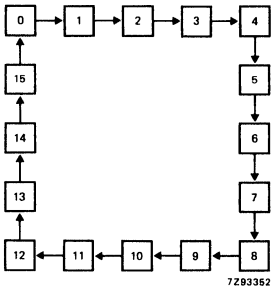


Fig. 5 State diagram.

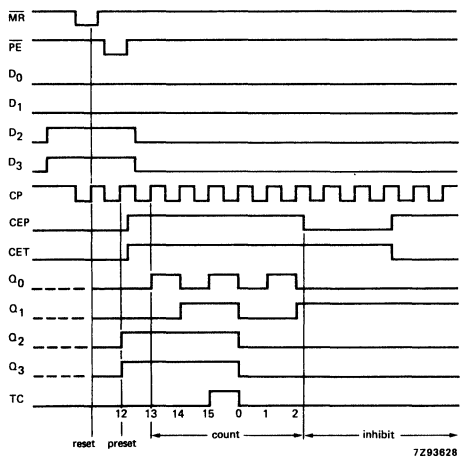


Fig. 6 Typical timing sequence: reset outputs to zero; preset to binary twelve; count to thirteen, fourteen, fifteen, zero, one and two; inhibit.

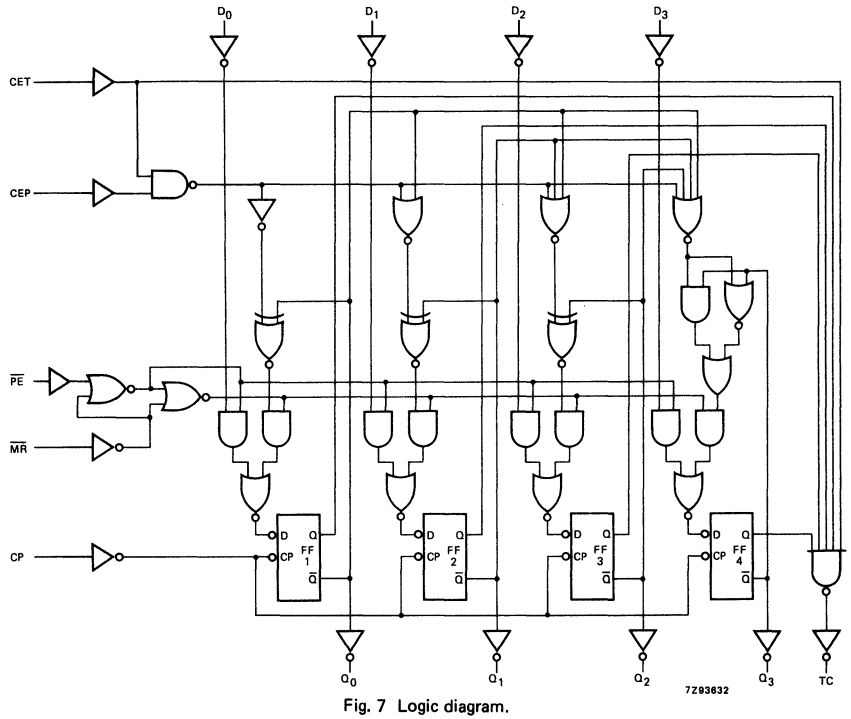


Fig. 7 Logic diagram.

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay CP to Q_n			205 41 35		255 51 43		310 62 53	ns	2.0 4.5 6.0	Fig. 8
t_{PHL}/t_{PLH}	propagation delay CP to TC			215 43 37		270 54 46		320 65 55	ns	2.0 4.5 6.0	Fig. 8
t_{PHL}/t_{PLH}	propagation delay CET to TC			150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 9
t_{THL}/t_{TLH}	output transition time			75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Figs 8 and 9
t_W	clock pulse width HIGH or LOW	90 18 15			115 23 20		135 27 23		ns	2.0 4.5 6.0	Fig. 8
t_{su}	set-up time $\overline{MR}$, D_n to CP	100 20 17			125 25 21		150 30 26		ns	2.0 4.5 6.0	Figs 10 and 11
t_{su}	set-up time $\overline{PE}$ to CP	150 30 26			190 38 33		225 45 38		ns	2.0 4.5 6.0	Fig. 10
t_{su}	set-up time CEP, CET to CP	175 35 30			220 44 37		265 53 45		ns	2.0 4.5 6.0	Fig. 12
t_h	hold time D_n, $\overline{PE}$, CEP, CET, $\overline{MR}$ to CP	0 0 0			0 0 0		0 0 0		ns	2.0 4.5 6.0	Figs 10, 11 and 12
f_{max}	maximum clock pulse frequency	5 27 32			4 22 26		4 18 21		MHz	2.0 4.5 6.0	Fig. 8

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
$\overline{MR}$	0.95
CP	1.10
CEP	0.25

INPUT	UNIT LOAD COEFFICIENT
D_n	0.25
CET	0.75
$\overline{PE}$	0.30

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay CP to Q_n			43		54		65	ns	4.5	Fig. 8
t_{PHL}/t_{PLH}	propagation delay CP to TC			49		61		74	ns	4.5	Fig. 8
t_{PHL}/t_{PLH}	propagation delay CET to TC			35		44		53	ns	4.5	Fig. 9
t_{THL}/t_{TLH}	output transition time			15		19		22	ns	4.5	Figs 8 and 9
t_W	clock pulse width HIGH or LOW	22			28		33		ns	4.5	Fig. 8
t_{su}	set-up time $\overline{MR}$, D_n to CP	20			25		30		ns	4.5	Figs 10 and 11
t_{su}	set-up time $\overline{PE}$ to CP	35			44		53		ns	4.5	Fig. 10
t_{su}	set-up time CEP, CET to CP	40			50		60		ns	4.5	Fig. 12
t_h	hold time D_n, $\overline{PE}$, CEP, CET, $\overline{MR}$ to CP	0			0		0		ns	4.5	Figs 10, 11 and 12
f_{max}	maximum clock pulse frequency	26			21		17		MHz	4.5	Fig. 8

AC WAVEFORMS

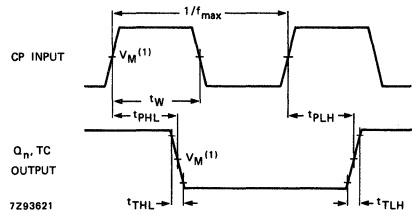


Fig. 8 Waveforms showing the clock (CP) to outputs (Q_n, TC) propagation delays, the clock pulse width, the output transition times and the maximum clock frequency.

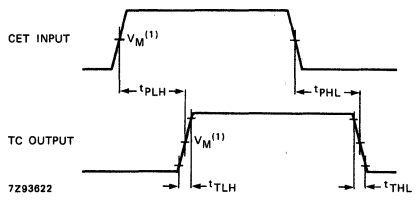


Fig. 9 Waveforms showing the input (CET) to output (TC) propagation delays and output transition times.

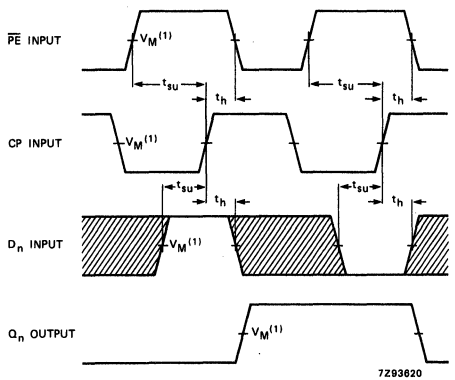


Fig. 10 Waveforms showing the set-up and hold times for the input (D_n) and parallel enable input ($\overline{PE}$).

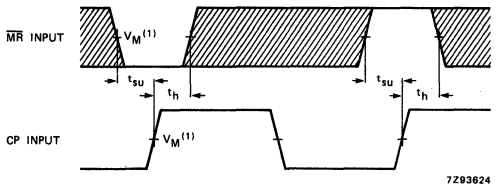


Fig. 11 Waveforms showing the $\overline{MR}$ set-up and hold times.

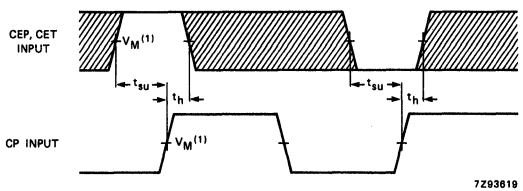


Fig. 12 Waveforms showing the CEP and CET set-up and hold times.

Note to Figs 10, 11 and 12

The shaded areas indicate when the input is permitted to change for predictable output performance.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

QUAD D-TYPE FLIP-FLOP; POSITIVE-EDGE TRIGGER; 3-STATE

FEATURES

- **Gated input enable for hold (do noting) mode**
- **Gated output enable control**
- **Edge-triggered D-type register**
- **Asynchronous master reset**
- **Output capability: bus driver**
- **I_{CC} category: MSI**

GENERAL DESCRIPTION

The 74HC/HCT173 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7.

The 74HC/HCT173 are 4-bit parallel load registers with clock enable control, 3-state buffered outputs (Q_0 to Q_3) and master reset (MR).

When the two clock enable inputs ($\overline{E}_1$ and $\overline{E}_2$) are LOW, the data on the D_n inputs is loaded into the register synchronously with the LOW-to-HIGH clock (CP) transition. When one or both $\overline{E}_n$ inputs are HIGH one set-up time prior to the LOW-to-HIGH clock transition, the register will retain the previous data. Data inputs and clock enable inputs are fully edge-triggered and must be stable only one set-up time prior to the LOW-to-HIGH clock transition.

The master reset input (MR) is an active HIGH asynchronous input. When MR is HIGH, all four flip-flops are reset (cleared) independently of any other input condition.

The 3-state output buffers are controlled by a 2-input NOR gate. When both output enable inputs ($\overline{OE}_1$ and $\overline{OE}_2$) are LOW, the data in the register is presented to the Q_n outputs. When one or both $\overline{OE}_n$ inputs are HIGH, the outputs are forced to a high impedance OFF-state. The 3-state output buffers are completely independent of the register operation; the $\overline{OE}_n$ transition does not affect the clock and reset operations.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay CP to Q_n MR to Q_n	C_L = 15 pF V_{CC} = 5 V	23 17	22 18	ns ns
f_{max}	maximum clock frequency		54	50	MHz
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per flip-flop	notes 1 and 2	25	28	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT173P: 16-lead DIL; plastic (SOT-38Z).
PC74HC/HCT173T: 16-lead mini-pack; plastic (SO-16; SOT-109A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 2	$\overline{OE}_1$, $\overline{OE}_2$	output enable input (active LOW)
3, 4, 5, 6	Q_0 to Q_3	3-state flip-flop outputs
7	CP	clock input (LOW-to-HIGH, edge-triggered)
8	GND	ground (0 V)
9, 10	$\overline{E}_1$, $\overline{E}_2$	clock enable inputs (active LOW)
14, 13, 12, 11	D_0 to D_3	data inputs
15	MR	asynchronous master reset (active HIGH)
16	V_{CC}	positive supply voltage

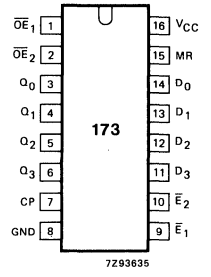


Fig. 1 Pin configuration.

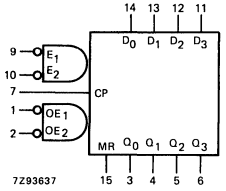


Fig. 2 Logic symbol.

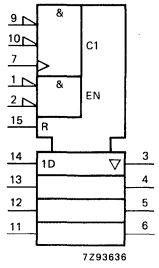


Fig. 3 IEC logic symbol.

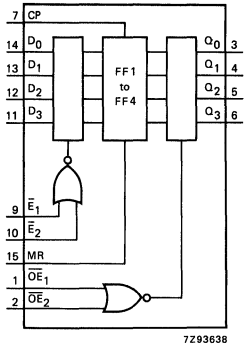


Fig. 4 Functional diagram.

FUNCTION TABLE

REGISTER OPERATING MODES	INPUTS					OUTPUTS
	MR	CP	$\overline{E}_1$	$\overline{E}_2$	D_n	Q_n (register)
reset (clear)	H	X	X	X	X	L
parallel load	L	↑	l	l	l	L
	L	↑	l	l	h	H
hold (no change)	L	X	h	X	X	q_n
	L	X	X	h	X	q_n

3-STATE BUFFER OPERATING MODES	INPUTS			OUTPUTS			
	Q_n (register)	$\overline{OE}_1$	$\overline{OE}_2$	Q_0	Q_1	Q_2	Q_3
read	L	L	L	L	L	L	L
	H	L	L	H	H	H	H
disabled	X	H	X	Z	Z	Z	Z
	X	X	H	Z	Z	Z	Z

H = HIGH voltage level
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition
L = LOW voltage level
l = LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition
q = lower case letters indicate the state of the referenced input (or output) one set-up time prior to the LOW-to-HIGH CP transition
X = don't care
Z = high impedance OFF-state
↑ = LOW-to-HIGH CP transition

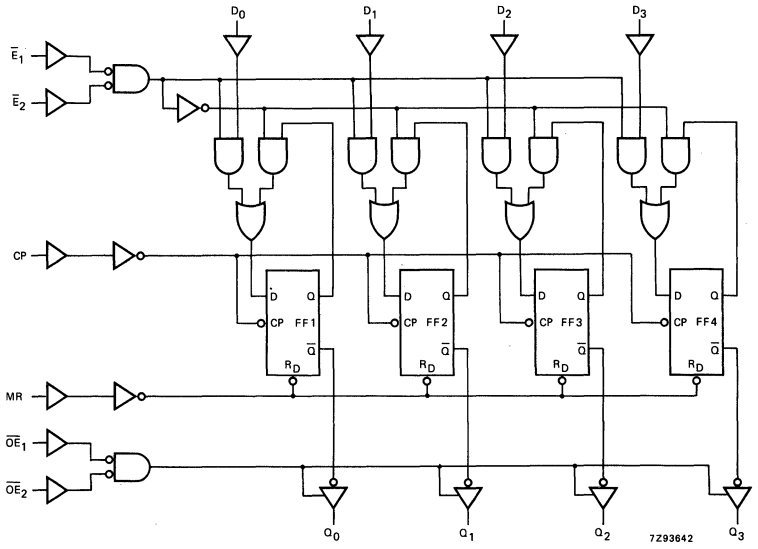


Fig. 5 Logic diagram.

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f = 6$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay CP to Q_n			225 45 38		280 56 48		340 68 58	ns	2.0 4.5 6.0	Fig. 6
t_{PHL}	propagation delay MR to Q_n			200 40 34		250 50 43		300 60 51	ns	2.0 4.5 6.0	Fig. 7
t_{PZH}/t_{PZL}	3-state output enable time $\overline{OE}_n$ to Q_n			150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 8
t_{PHZ}/t_{PLZ}	3-state output disable time $\overline{OE}_n$ to Q_n			150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 8
t_{THL}/t_{TLH}	output transition time			60 12 10		75 15 13		90 18 15	ns	2.0 4.5 6.0	Fig. 6
t_W	clock pulse width HIGH or LOW	100 20 17			125 25 21		150 30 26		ns	2.0 4.5 6.0	Fig. 6
t_W	master reset pulse width; HIGH	80 16 14			100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 7
t_{rem}	removal time MR to CP	75 15 13			95 19 16		110 22 19		ns	2.0 4.5 6.0	Fig. 7
t_{su}	set-up time $\overline{E}_n$ to CP	125 25 21			155 31 26		190 38 32		ns	2.0 4.5 6.0	Fig. 9
t_{su}	set-up time D_n to CP	100 20 17			125 25 21		150 30 26		ns	2.0 4.5 6.0	Fig. 9
t_h	hold time $\overline{E}_n$ to CP	0 0 0			0 0 0		0 0 0		ns	2.0 4.5 6.0	Fig. 9
t_h	hold time D_n to CP	0 0 0			0 0 0		0 0 0		ns	2.0 4.5 6.0	Fig. 9
f_{max}	maximum clock pulse frequency	5 25 30			4 20 24		3 17 20		MHz	2.0 4.5 6.0	Fig. 6

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver
I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications.
To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
$\overline{OE}_1$, $\overline{OE}_2$	1.00
MR, CP	0.50
$\overline{E}_1$, $\overline{E}_2$	0.25
D_n	0.25

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f = 6$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay CP to Q_n			43		54		65	ns	4.5	Fig. 6
t_{PHL}	propagation delay MR to Q_n			40		50		60	ns	4.5	Fig. 7
t_{PZH}/t_{PZL}	3-state output enable time $\overline{OE}_n$ to Q_n			35		44		53	ns	4.5	Fig. 8
t_{PHZ}/t_{PLZ}	3-state output disable time $\overline{OE}_n$ to Q_n			30		38		45	ns	4.5	Fig. 8
t_{THL}/t_{TLH}	output transition time			12		15		19	ns	4.5	Fig. 6
t_W	clock pulse width HIGH or LOW	25			31		38		ns	4.5	Fig. 6
t_W	master reset pulse width; HIGH	15			19		22		ns	4.5	Fig. 7
t_{rem}	removal time MR to CP	15			19		22		ns	4.5	Fig. 7
t_{su}	set-up time $\overline{E}_n$ to CP	30			38		45		ns	4.5	Fig. 9
t_{su}	set-up time D_n to CP	25			31		38		ns	4.5	Fig. 9
t_h	hold time $\overline{E}_n$ to CP	0			0		0		ns	4.5	Fig. 9
t_h	hold time D_n to CP	0			0		0		ns	4.5	Fig. 9
f_{max}	maximum clock pulse frequency	20			16		13		MHz	4.5	Fig. 6

AC WAVEFORMS

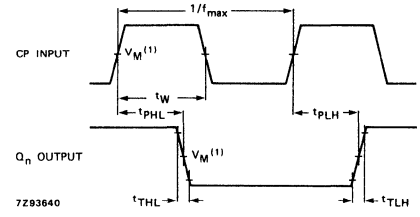


Fig. 6 Waveforms showing the clock (CP) to output (Q_n) propagation delays, the clock pulse width, the output transition times and the maximum clock pulse frequency.

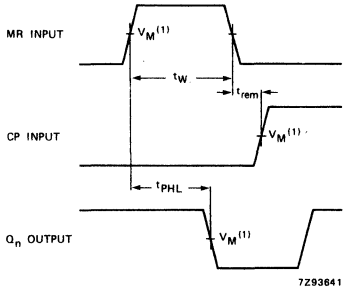


Fig. 7 Waveforms showing the master reset (MR) pulse width, the master reset to output (Q_n) propagation delays and the master reset to clock (CP) removal time.

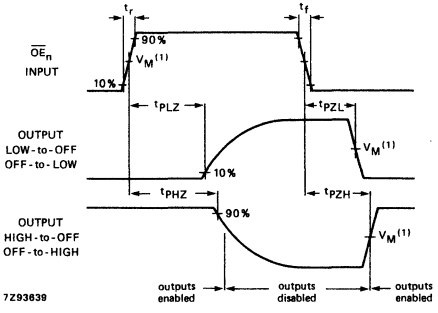


Fig. 8 Waveforms showing the 3-state enable and disable times.

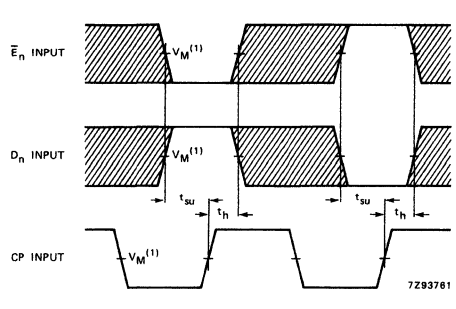


Fig. 9 Waveforms showing the data set-up and hold times from input ($\overline{E}_n$, D_n) to clock (CP).

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

Note to Fig. 9

The shaded areas indicate when the input is permitted to change for predictable output performance.

HEX D-TYPE FLIP-FLOP WITH RESET; POSITIVE-EDGE TRIGGER

FEATURES

- **Six edge-triggered D-type flip-flops**
- **Asynchronous master reset**
- **Output capability: standard**
- **I_{CC} category: MSI**

GENERAL DESCRIPTION

The 74HC/HCT174 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7.

The 74HC/HCT174 have six edge-triggered D-type flip-flops with individual D inputs and Q outputs. The common clock (CP) and master reset ($\overline{MR}$) inputs load and reset (clear) all flip-flops simultaneously.

The register is fully edge-triggered. The state of each D input, one set-up time prior to the LOW-to-HIGH clock transition, is transferred to the corresponding output of the flip-flop.

A LOW level on the $\overline{MR}$ input forces all outputs LOW, independently of clock or data inputs.

The device is useful for applications requiring true outputs only and clock and master reset inputs that are common to all storage elements.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay CP to Q_n $\overline{MR}$ to Q_n	C_L = 15 pF V_{CC} = 5 V	14 13	17 17	ns ns
f_{max}	maximum clock frequency		60	54	MHz
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per flip-flop	notes 1 and 2	17	17	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT174P: 16-lead DIL; plastic (SOT-38Z).
PC74HC/HCT174T: 16-lead mini-pack; plastic (SO-16; SOT-109A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	$\overline{MR}$	asynchronous master reset (active LOW)
2, 5, 7, 10, 12, 15	Q_0 to Q_5	flip-flop outputs
3, 4, 6, 11, 13, 14	D_0 to D_5	data inputs
8	GND	ground (0 V)
9	CP	clock input (LOW-to-HIGH, edge-triggered)
16	V_{CC}	positive supply voltage

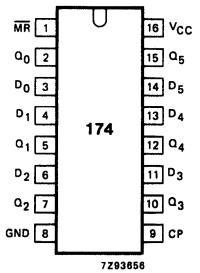


Fig. 1 Pin configuration.

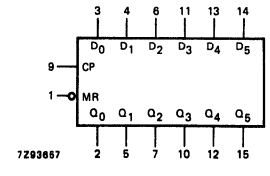


Fig. 2 Logic symbol.

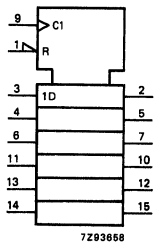


Fig. 3 IEC logic symbol.

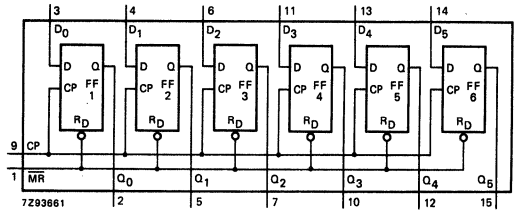


Fig. 4 Functional diagram.

FUNCTION TABLE

OPERATING MODES	INPUTS			OUTPUTS
	$\overline{MR}$	CP	D_n	Q_n
reset (clear)	L	X	X	L
load "1"	H	↑	h	H
load "0"	H	↑	l	L

H = HIGH voltage level
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition
L = LOW voltage level
l = LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition
X = don't care
↑ = LOW-to-HIGH CP transition

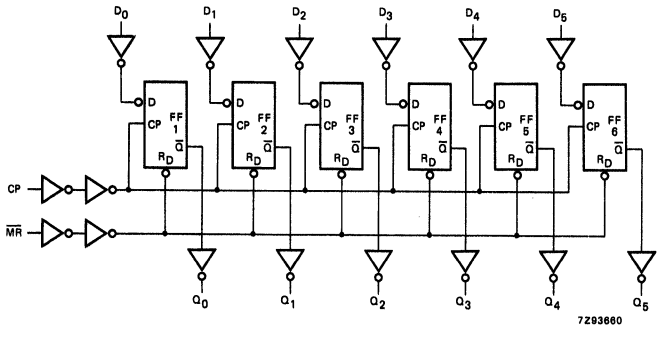


Fig. 5 Logic diagram.

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f = 6$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay CP to Q_n			170 34 29		215 43 37		255 51 43	ns	2.0 4.5 6.0	Fig. 6
t_{PHL}	propagation delay $\overline{MR}$ to Q_n			150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 7
t_{THL}/t_{TLH}	output transition time			75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 6
t_W	clock pulse width HIGH or LOW	80 16 14			100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 6
t_W	master reset pulse width; HIGH	80 16 14			100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 7
t_{rem}	removal time $\overline{MR}$ to CP	5 5 5			5 5 5		5 5 5		ns	2.0 4.5 6.0	Fig. 7
t_{su}	set-up time D_n to CP	80 16 14			100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 8
t_h	hold time CP to D_n	5 5 5			5 5 5		5 5 5		ns	2.0 4.5 6.0	Fig. 8
f_{max}	maximum clock pulse frequency	6 30 35			5 24 28		4 20 24		MHz	2.0 4.5 6.0	Fig. 6

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications.
To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
D_n	0.25
$\overline{CP}$	1.30
$\overline{MR}$	1.25

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay CP to Q_n			40		50		60	ns	4.5	Fig. 6
t_{PHL}	propagation delay $\overline{MR}$ to Q_n			40		50		60	ns	4.5	Fig. 7
t_{THL}/t_{TLH}	output transition time			15		19		22	ns	4.5	Fig. 6
t_W	clock pulse width HIGH or LOW	20			25		30		ns	4.5	Fig. 6
t_W	master reset pulse width; HIGH	20			25		30		ns	4.5	Fig. 7
t_{rem}	removal time $\overline{MR}$ to CP	12			15		18		ns	4.5	Fig. 7
t_{su}	set-up time D_n to CP	16			20		24		ns	4.5	Fig. 8
t_h	hold time CP to D_n	5			5		5		ns	4.5	Fig. 8
f_{max}	maximum clock pulse frequency	25			20		17		MHz	4.5	Fig. 6

AC WAVEFORMS

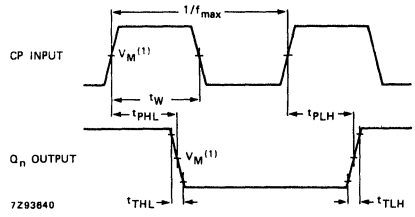


Fig. 6 Waveforms showing the clock (CP) to output (Q_n) propagation delays, the clock pulse width, the output transition times and the maximum clock pulse frequency.

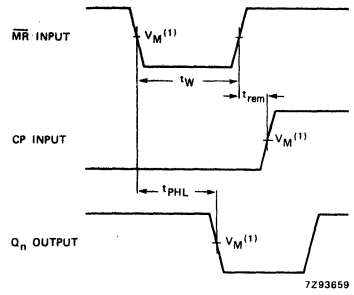


Fig. 7 Waveforms showing the master reset ($\overline{MR}$) pulse width, the master reset to output (Q_n) propagation delays and the master reset to clock (CP) removal time.

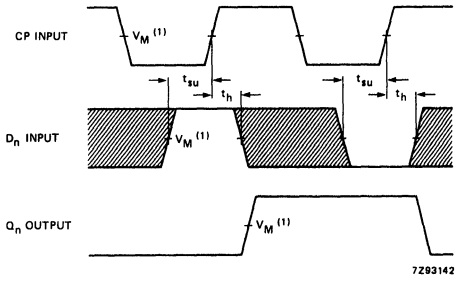


Fig. 8 Waveforms showing the data set-up and hold times for the data input (D_n).

Note to Fig. 8

The shaded areas indicate when the input is permitted to change for predictable output performance.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

LOOK-AHEAD CARRY GENERATOR

FEATURES

- **Provides carry look-ahead across a group of four ALU's**
- **Multi-level look-ahead for high-speed arithmetic operation over long word length**
- **Output capability: standard**
- **I_{CC} category: MSI**

GENERAL DESCRIPTION

The 74HC/HCT182 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7.

The 74HC/HCT182 carry look-ahead generators accept up to four pairs of active LOW carry propagate ($\overline{P}_0$, $\overline{P}_1$, $\overline{P}_2$, $\overline{P}_3$) and carry generate ($\overline{G}_0$, $\overline{G}_1$, $\overline{G}_2$, $\overline{G}_3$) signals and an active HIGH carry input (C_n). The devices provide anticipated active HIGH carries (C_{n+x}, C_{n+y}, C_{n+z}) across four groups of binary adders.

The "182" also has active LOW carry propagate ($\overline{P}$) and carry generate ($\overline{G}$) outputs which may be used for further levels of look-ahead.

The logic equations provided at the outputs are:

$$C_{n+x} = G_0 + P_0C_n$$
$$C_{n+y} = G_1 + P_1G_0 + P_1P_0C_n$$
$$C_{n+z} = G_2 + P_2G_1 + P_2P_1G_0 + P_2P_1P_0C_n$$
$$\overline{G} = \overline{G_3 + P_3G_2 + P_3P_2G_1 + P_3P_2P_1G_0}$$
$$\overline{P} = \overline{P_3P_2P_1P_0}$$

The "182" can also be used with binary ALU's in an active LOW or active HIGH input operand mode. The connections to and from the ALU to the carry look-ahead generator are identical in both cases.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay $\overline{P}_n$ to $\overline{P}$ C_n to any output $\overline{P}_n$ or $\overline{G}_n$ to any output	C_L = 15 pF V_{CC} = 5 V	12 17 15	15 22 18	ns ns ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per package	notes 1 and 2	51	51	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT182P: 16-lead DIL; plastic (SOT-38Z).
PC74HC/HCT182T: 16-lead mini-pack; plastic (SO-16; SOT-109A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
3, 1, 14, 5	$\overline{G}_0$ to $\overline{G}_3$	carry generate inputs (active LOW)
4, 2, 15, 6	$\overline{P}_0$ to $\overline{P}_3$	carry propagate inputs (active LOW)
7	$\overline{P}$	carry propagate output (active LOW)
8	GND	ground (0 V)
9	C_{n+z}	function output
10	$\overline{G}$	carry generate output (active LOW)
11	C_{n+y}	function output
12	C_{n+x}	function output
13	C_n	carry input (active HIGH)
16	V_{CC}	positive supply voltage

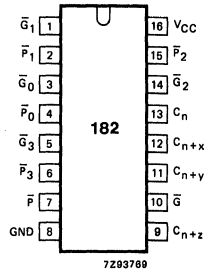


Fig. 1 Pin configuration.

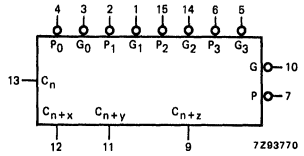


Fig. 2 Logic symbol.

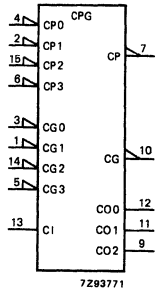


Fig. 3 IEC logic symbol.

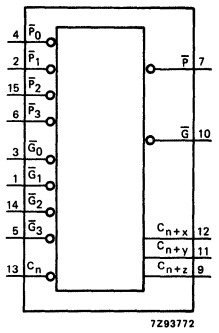


Fig. 4 Functional diagram.

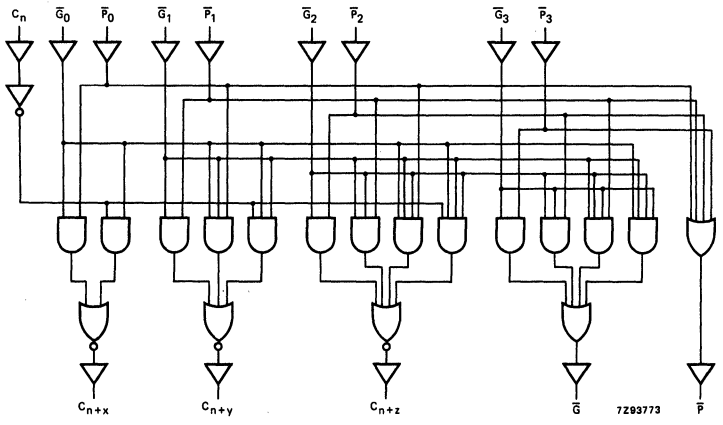


Fig. 5 Logic diagram.

FUNCTION TABLE

INPUTS									OUTPUTS				
C_n	$\overline{G}_0$	$\overline{P}_0$	$\overline{G}_1$	$\overline{P}_1$	$\overline{G}_2$	$\overline{P}_2$	$\overline{G}_3$	$\overline{P}_3$	C_{n+x}	C_{n+y}	C_{n+z}	$\overline{G}$	$\overline{P}$
X	H	H							L				
L	H	X							L				
X	L	X							H				
H	X	L							H				
X	X	X	H	H						L			
X	H	H	H	X						L			
L	H	X	L	X						L			
X	X	X	X	X						H			
X	L	X	X	L						H			
H	X	L	X	L						H			
X	X	H	H	H	H	H					L		
X	H	H	H	H	H	X					L		
L	X	H	H	X	H	X					L		
X	X	H	H	X	L	X					H		
X	X	X	X	L	X	X					H		
H	X	X	X	L	L	L					H		
X	X	X	X	X	H	H	H	H				H	
X	H	X	H	H	H	X	H	X				H	
L	X	X	L	X	X	L	X	X				H	
X	X	X	X	L	X	L	X	L				H	
X	X	X	X	X	L	L	L	L				L	
X	X	X	X	L	L	L	X	L				L	
X	X	X	X	L	X	L	X	L				L	
X	X	X	X	L	X	L	X	L				L	
		H		X		X		X					H
		X		H		X		X					H
		X		X		H		X					H
		X		X		X		H					H
		L		L		L		L					L

H = HIGH voltage level
L = LOW voltage level
X = don't care

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".
Output capability: standard
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delay $\overline{P}_n$ to $\overline{P}$			130 26 22		165 33 28		195 39 33	ns	2.0 4.5 6.0	Fig. 6
t_{PHL}/ t_{PLH}	propagation delay C_n to any output			170 34 29		215 43 37		255 51 43	ns	2.0 4.5 6.0	Fig. 6
t_{PHL}/ t_{PLH}	propagation delay $\overline{P}_n$ or $\overline{G}_n$ to any output			155 31 26		195 39 33		235 47 40	ns	2.0 4.5 6.0	Fig. 6
t_{THL}/ t_{TLH}	output transition time			75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 6

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
$\overline{G}_0$, $\overline{G}_1$, $\overline{P}_0$, $\overline{P}_1$, $\overline{P}_2$	1.50
$\overline{G}_3$	0.30
$\overline{G}_2$, $\overline{P}_3$, C_n	1.25

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delay $\overline{P}_n$ to $\overline{P}$			31		39		47	ns	4.5	Fig. 6
t_{PHL}/ t_{PLH}	propagation delay C_n to any output			45		56		68	ns	4.5	Fig. 6
t_{PHL}/ t_{PLH}	propagation delay $\overline{P}_n$ or $\overline{C}_n$ to any output			38		48		57	ns	4.5	Fig. 6
t_{THL}/ t_{TLH}	output transition time			15		19		22	ns	4.5	Fig. 6

AC WAVEFORMS

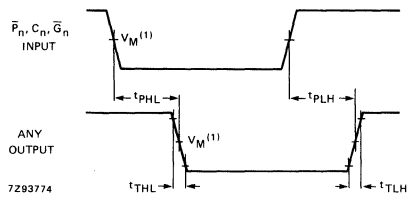


Fig. 6 Waveforms showing the input ($\overline{P}_n$, C_n, $\overline{G}_n$) to any output propagation delays and the output transition times.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}
HCT: V_M = 1.3 V; V_I = GND to 3 V.

QUAD 2-INPUT EXCLUSIVE-NOR GATE

FEATURES

- **Output capability: standard**
- **I_{CC} category: SSI**

GENERAL DESCRIPTION

The 74HC7266 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7.

The 74HC7266 provide the EXCLUSIVE-NOR function with active push-pull output.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
			HC	
t_{PHL}/t_{PLH}	propagation delay nA, nB to nY	C_L = 15 pF; V_{CC} = 5 V	11	ns
C_I	input capacitance		3.5	pF
C_{PD}	power dissipation capacitance per gate	note 1	18	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} – 1.5 V

ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC7266P: 14-lead DIL; plastic (SOT-27).
PC74HC7266T: 14-lead mini-pack; plastic (SO-14; SOT-108A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 5, 8, 12	1A to 4A	data inputs
2, 6, 9, 13	1B to 4B	data inputs
3, 4, 10, 11	1Y to 4Y	data outputs
7	GND	ground (0 V)
14	V_{CC}	positive supply voltage

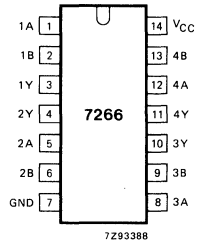


Fig. 1 Pin configuration.

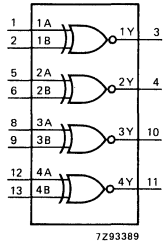


Fig. 2 Logic symbol.

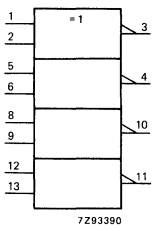


Fig. 3 IEC logic symbol.

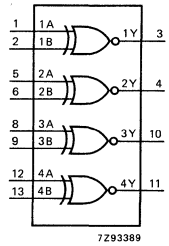


Fig. 4 Functional diagram.

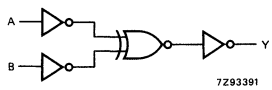


Fig. 5 Logic diagram (one gate).

FUNCTION TABLE

INPUTS		OUTPUT
nA	nB	nY
L	L	H
L	H	L
H	L	L
H	H	H

H = HIGH voltage level
L = LOW voltage level

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: SSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delay nA, nB to nY			120 24 20		150 30 26		180 36 31	ns	2.0 4.5 6.0	Fig. 6
t_{THL}/ t_{TLH}	output transition time			75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 6

AC WAVEFORMS

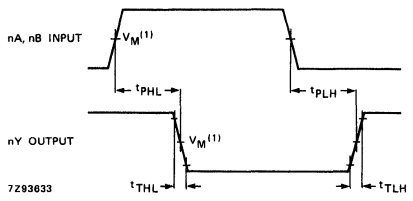


Fig. 6 Waveforms showing the input (nA, nB) to output (nY) propagation delays and the output transition times.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

HEX BUFFER/LINE DRIVER; 3-STATE

FEATURES

- **Non-inverting outputs**
- **Output capability: bus driver**
- **I_{CC} category: MSI**

GENERAL DESCRIPTION

The 74HC/HCT365 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7.

The 74HC/HCT365 are hex non-inverting buffer/line drivers with 3-state outputs. The 3-state outputs (nY) are controlled by the output enable inputs ($\overline{OE}_1$, $\overline{OE}_2$).

A HIGH on $\overline{OE}_n$ causes the outputs to assume a high impedance OFF-state.

The "365" is identical to the "366" but has non-inverting outputs.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay nA to nY	C_L = 15 pF; V_{CC} = 5 V	8	11	ns
C_I	input capacitance		3,5	3,5	pF
C_{PD}	power dissipation capacitance per buffer	notes 1 and 2	32	30	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT365P: 16-lead DIL; plastic (SOT-38Z).
PC74HC/HCT365T: 16-lead mini-pack; plastic (SO-16; SOT-109A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 15	$\overline{OE}_1$, $\overline{OE}_2$	output enable inputs (active LOW)
2, 4, 6, 10, 12, 14	1A to 6A	data inputs
3, 5, 7, 9, 11, 13	1Y to 6Y	data outputs
8	GND	ground (0 V)
16	V_{CC}	positive supply voltage

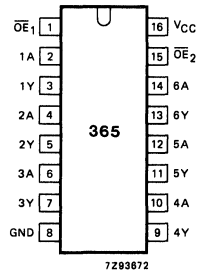


Fig. 1 Pin configuration.

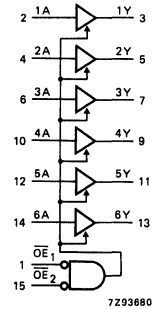


Fig. 2 Logic symbol.

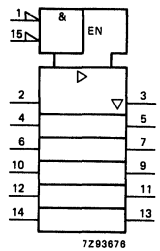


Fig. 3 IEC logic symbol.

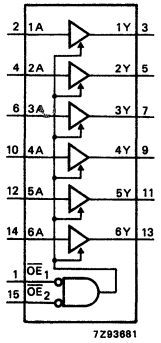


Fig. 4 Functional diagram.

FUNCTION TABLE

INPUTS			OUTPUT
$\overline{OE}_1$	$\overline{OE}_2$	nA	nY
L	L	L	L
L	L	H	H
X	H	X	Z
H	X	X	Z

H = HIGH voltage level
L = LOW voltage level
X = don't care
Z = high impedance OFF-state

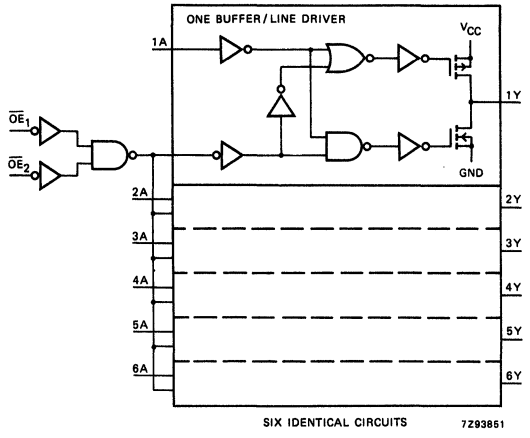


Fig. 5 Logic diagram.

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delay nA to nY			110 22 19		140 28 24		165 33 28	ns	2.0 4.5 6.0	Fig. 6
t_{PZH}/ t_{PZL}	3-state output enable time $\overline{OE}_n$ to nY			150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 7
t_{PHZ}/ t_{PLZ}	3-state output disable time $\overline{OE}_n$ to nY			150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 7
t_{THL}/ t_{TLH}	output transition time			60 12 10		75 15 13		90 18 15	ns	2.0 4.5 6.0	Fig. 6

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver
I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications.
To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
$\overline{OE}_1$	1.00
$\overline{OE}_2$	0.90
nA	1.00

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} V	WAVEFORMS
		+25			–40 to +85		–40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay nA to nY			25		31		38	ns	4.5	Fig. 6
t_{PZH}/t_{PZL}	3-state output enable time $\overline{OE}_n$ to nY			35		44		53	ns	4.5	Fig. 7
t_{PHZ}/t_{PLZ}	3-state output disable time $\overline{OE}_n$ to nY			35		44		53	ns	4.5	Fig. 7
t_{THL}/t_{TLH}	output transition time			12		15		18	ns	4.5	Fig. 6

AC WAVEFORMS

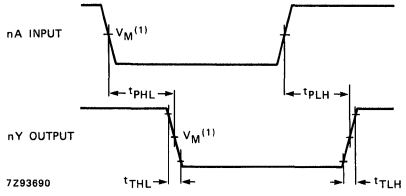


Fig. 6 Waveforms showing the input (nA) to output (nY) propagation delays and the output transition times.

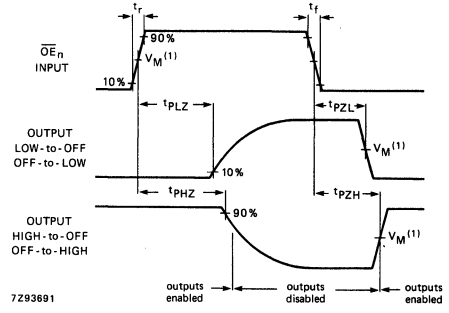


Fig. 7 Waveforms showing the 3-state enable and disable times.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

HEX BUFFER/LINE DRIVER; 3-STATE; INVERTING

FEATURES

- **Inverting outputs**
- **Output capability: bus driver**
- **I_{CC} category: MSI**

GENERAL DESCRIPTION

The 74HC/HCT366 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7.

The 74HC/HCT366 are hex inverting buffer/line drivers with 3-state outputs. The 3-state outputs (nY) are controlled by the output enable inputs ($\overline{OE}_1$, $\overline{OE}_2$).

A HIGH on $\overline{OE}_n$ causes the outputs to assume a high impedance OFF-state.

The "366" is identical to the "365" but has inverting outputs.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay nA to n$\overline{Y}$	C_L = 15 pF V_{CC} = 5 V	10	12	ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per buffer	notes 1 and 2	30	31	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT366P: 16-lead DIL; plastic (SOT-38Z).
PC74HC/HCT366T: 16-lead mini-pack; plastic (SO-16; SOT-109A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 15	$\overline{OE}_1$, $\overline{OE}_2$	output enable inputs (active LOW)
2, 4, 6, 10, 12, 14	1A to 6A	data inputs
3, 5, 7, 9, 11, 13	1$\overline{Y}$ to 6$\overline{Y}$	data outputs
8	GND	ground (0 V)
16	V_{CC}	positive supply voltage

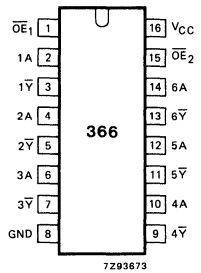


Fig. 1 Pin configuration.

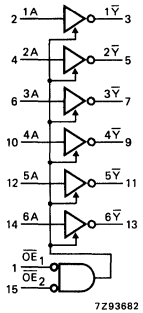


Fig. 2 Logic symbol.

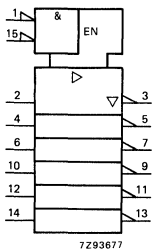


Fig. 3 IEC logic symbol.

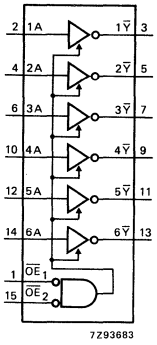


Fig. 4 Functional diagram.

FUNCTION TABLE

INPUTS			OUTPUT
$\overline{OE}_1$	$\overline{OE}_2$	nA	nȲ
L	L	L	H
L	L	H	L
X	H	X	Z
H	X	X	Z

H = HIGH voltage level
L = LOW voltage level
X = don't care
Z = high impedance OFF-state

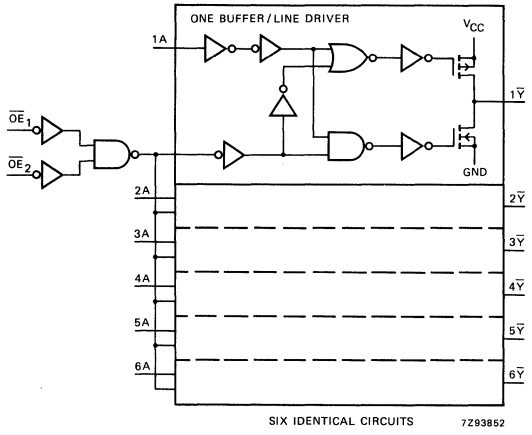


Fig. 5 Logic diagram.

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delay nA to n$\overline{Y}$			125 25 21		155 31 26		190 38 32	ns	2.0 4.5 6.0	Fig. 6
t_{PZH}/ t_{PZL}	3-state output enable time $\overline{OE}_n$ to n$\overline{Y}$			150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 7
t_{PHZ}/ t_{PLZ}	3-state output disable time $\overline{OE}_n$ to n$\overline{Y}$			150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 7
t_{THL}/ t_{TLH}	output transition time			60 12 10		75 15 13		90 18 15	ns	2.0 4.5 6.0	Fig. 6

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver
I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications.
To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
$\overline{OE}_1$	1.00
$\overline{OE}_2$	0.90
nA	1.00

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay nA to n$\overline{Y}$			30		38		45	ns	4.5	Fig. 6
t_{PZH}/t_{PZL}	3-state output enable time $\overline{OE}_n$ to n$\overline{Y}$			35		44		53	ns	4.5	Fig. 7
t_{PHZ}/t_{PLZ}	3-state output disable time $\overline{OE}_n$ to n$\overline{Y}$			35		44		53	ns	4.5	Fig. 7
t_{THL}/t_{TLH}	output transition time			12		15		18	ns	4.5	Fig. 6

AC WAVEFORMS

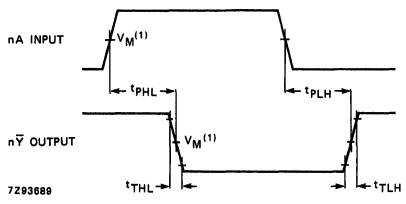


Fig. 6 Waveforms showing the input (nA) to output (n$\overline{Y}$) propagation delays and the output transition times.

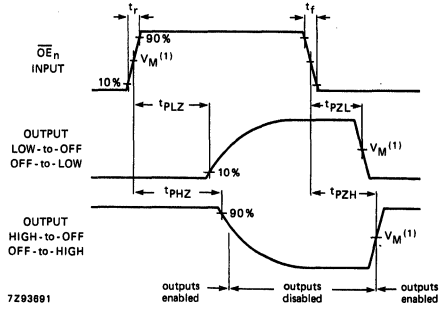


Fig. 7 Waveforms showing the 3-state enable and disable times.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

HEX BUFFER/LINE DRIVER; 3-STATE

FEATURES

- **Non-inverting outputs**
- **Output capability: bus driver**
- **I_{CC} category: MSI**

GENERAL DESCRIPTION

The 74HC/HCT367 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL(LSTTL). They are specified in compliance with JEDEC standard no. 7.

The 74HC/HCT367 are hex non-inverting buffer/line drivers with 3-state outputs. The 3-state outputs (nY) are controlled by the output enable inputs ($1\overline{OE}$, $2\overline{OE}$).

A HIGH on $n\overline{OE}$ causes the outputs to assume a high impedance OFF-state.

The "367" is identical to the "368" but has non-inverting outputs.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay nA to nY	C_L = 15 pF; V_{CC} = 5 V	8	11	ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per buffer	notes 1 and 2	32	33	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacitance in pF
   f_o = output frequency in MHz; V_{CC} = supply voltage in V
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT367P: 16-lead DIL; plastic (SOT-38Z).
PC74HC/HCT367T: 16-lead mini-pack; plastic (SO-16; SOT-109A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 15	$1\overline{OE}$, $2\overline{OE}$	output enable inputs (active LOW)
2, 4, 6, 10, 12, 14	1A to 6A	data inputs
3, 5, 7, 9, 11, 13	1Y to 6Y	data outputs
8	GND	ground (0 V)
16	V_{CC}	positive supply voltage

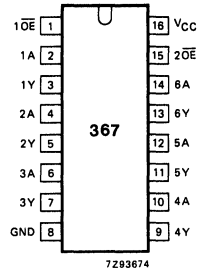


Fig. 1 Pin configuration.

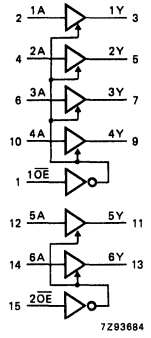


Fig. 2 Logic symbol.

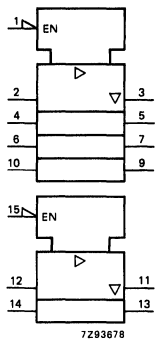


Fig. 3 IEC logic symbol.

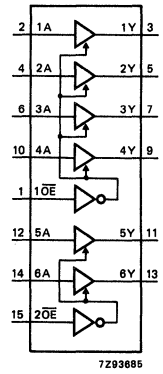


Fig. 4 Functional diagram.

FUNCTION TABLE

INPUTS		OUTPUTS
$n\overline{OE}$	nA	nY
L	L	L
L	H	H
H	X	Z

H = HIGH voltage level
L = LOW voltage level
X = don't care
Z = high impedance OFF-state

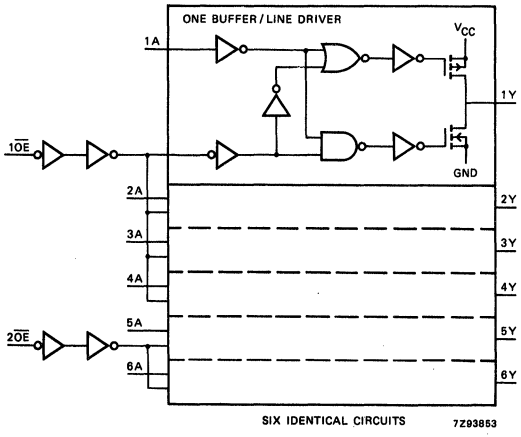


Fig. 5 Logic diagram.

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delay nA to nY			110 22 23		140 28 24		165 33 28	ns	2.0 4.5 6.0	Fig. 6
t_{PZH}/ t_{PZL}	3-state output enable time $n\overline{OE}$ to nY			150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 7
t_{PHZ}/ t_{PLZ}	3-state output disable time $n\overline{OE}$ to nY			175 35 30		220 44 37		265 53 45	ns	2.0 4.5 6.0	Fig. 7
t_{THL}/ t_{TLH}	output transition time			60 12 10		75 15 13		90 18 15	ns	2.0 4.5 6.0	Fig. 6

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver
I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
$1\overline{OE}$	1.00
$2\overline{OE}$	0.90
nA	1.00

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} V	WAVEFORMS
		+25			−40 to + 85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay nA to nY			25		31		38	ns	4.5	Fig. 6
t_{PZH}/t_{PZL}	3-state output enable time $n\overline{OE}$ to nY			35		44		53	ns	4.5	Fig. 7
t_{PHZ}/t_{PLZ}	3-state output disable time $n\overline{OE}$ to nY			35		44		53	ns	4.5	Fig. 7
t_{THL}/t_{TLH}	output transition time			12		15		18	ns	4.5	Fig. 6

AC WAVEFORMS

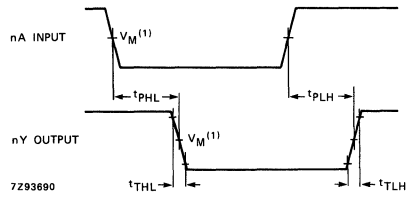


Fig. 6 Waveforms showing the input (nA) to output (nY) propagation delays and the output transition times.

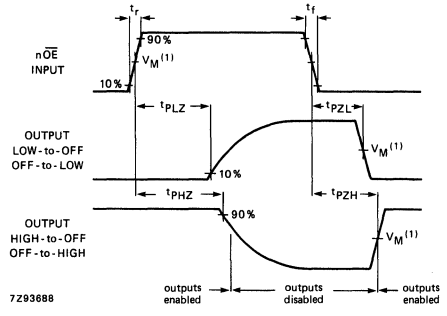


Fig. 7 Waveforms showing the 3-state enable and disable times.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

HEX BUFFER/LINE DRIVER; 3-STATE; INVERTING

FEATURES

- **Inverting outputs**
- **Output capability: bus driver**
- **I_{CC} category: MSI**

GENERAL DESCRIPTION

The 74HC/HCT368 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7.

The 74HC/HCT368 are hex inverting buffer/line drivers with 3-state outputs. The 3-state outputs ($n\overline{Y}$) are controlled by the output enable inputs ($1\overline{OE}$, $2\overline{OE}$).

A HIGH on $n\overline{OE}$ causes the outputs to assume a high impedance OFF-state.

The "368" is identical to the "367" but has inverting outputs.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay nA to $n\overline{Y}$	C_L = 15 pF; V_{CC} = 5 V	8	9	ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per buffer	notes 1 and 2	30	30	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT368P: 16-lead DIL; plastic (SOT-38Z).
PC74HC/HCT368T: 16-lead mini-pack; plastic (SO-16; SOT-109A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 15	$1\overline{OE}$, $2\overline{OE}$	output enable inputs (active LOW)
2, 4, 6, 10, 12, 14	1A to 6A	data inputs
3, 5, 7, 9, 11, 13	$1\overline{Y}$ to $6\overline{Y}$	data outputs
8	GND	ground (0 V)
16	V_{CC}	positive supply voltage

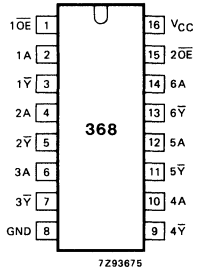


Fig. 1 Pin configuration.

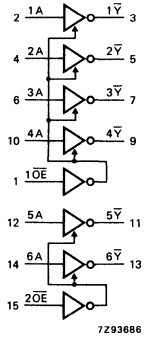


Fig. 2 Logic symbol.

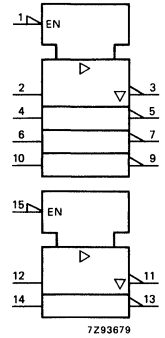


Fig. 3 IEC logic symbol.

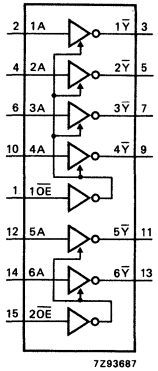


Fig. 4 Functional diagram.

FUNCTION TABLE

INPUTS		OUTPUTS
n$\overline{OE}$	nA	n$\overline{Y}$
L	L	H
L	H	L
H	X	Z

H = HIGH voltage level
L = LOW voltage level
X = don't care
Z = high impedance OFF-state

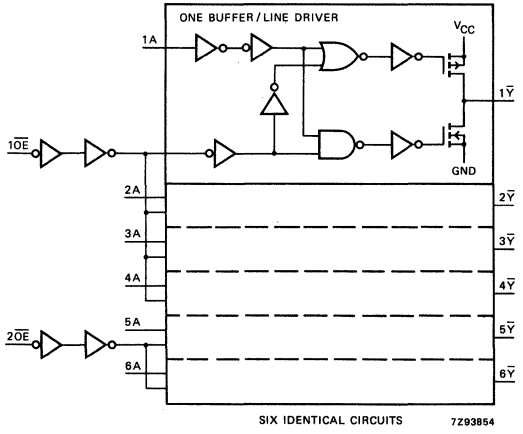


Fig. 5 Logic diagram.

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".
Output capability: bus driver
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delay nA to n$\overline{Y}$			95 19 16		120 24 20		145 29 25	ns	2.0 4.5 6.0	Fig. 6
t_{PZH}/ t_{PZL}	3-state output enable time n$\overline{OE}$ to n$\overline{Y}$			150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 7
t_{PHZ}/ t_{PLZ}	3-state output disable time n$\overline{OE}$ to n$\overline{Y}$			150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 7
t_{THL}/ t_{TLH}	output transition time			60 12 10		75 15 13		90 18 15	ns	2.0 4.5 6.0	Fig. 6

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".
Output capability: bus driver
I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications.
To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
1$\overline{OE}$	1.00
2$\overline{OE}$	0.90
nA	1.00

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay nA to n$\overline{Y}$			25		31		38	ns	4.5	Fig. 6
t_{PZH}/t_{PZL}	3-state output enable time n$\overline{OE}$ to n$\overline{Y}$			35		44		53	ns	4.5	Fig. 7
t_{PHZ}/t_{PLZ}	3-state output disable time n$\overline{OE}$ to n$\overline{Y}$			35		44		53	ns	4.5	Fig. 7
t_{THL}/t_{TLH}	output transition time			12		15		18	ns	4.5	Fig. 6

AC WAVEFORMS

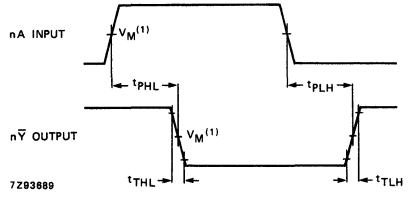


Fig. 6 Waveforms showing the input (nA) to output (n$\overline{Y}$) propagation delays and the output transition times.

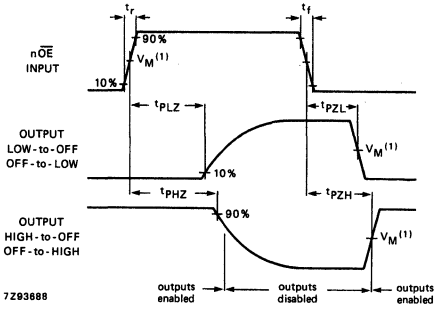


Fig. 7 Waveforms showing the 3-state enable and disable times.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

DUAL DECADE RIPPLE COUNTER

FEATURES

- **Two BCD decade or bi-quinary counters**
- **One package can be configured to divide-by-2, 4, 5, 10, 20, 25, 50 or 100**
- **Two master reset inputs to clear each decade counter individually**
- **Output capability: standard**
- **I_{CC} category: MSI**

GENERAL DESCRIPTION

The 74HC/HCT390 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7.

The 74HC/HCT390 are dual 4-bit decade ripple counters divided into four separately clocked sections. The counters have two divide-by-2 sections and two divide-by-5 sections. These sections are normally used in a BCD decade or bi-quinary configuration, since they share a common master reset input (nMR). If the two master reset inputs (1MR and 2MR) are used to simultaneously clear all 8 bits of the counter, a number of counting configurations are possible within one package. The separate clocks ($n\overline{CP}_0$ and $n\overline{CP}_1$) of each section allow ripple counter or frequency division applications of divide-by-2, 4, 5, 10, 20, 25, 50 or 100.

(continued on next page)

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay $n\overline{CP}_0$ to nQ_0 $n\overline{CP}_1$ to nQ_1 $n\overline{CP}_1$ to nQ_2 $n\overline{CP}_1$ to nQ_3 $n\overline{CP}_0$ to nQ_2 MR to Q_n	C_L = 15 pF V_{CC} = 5 V	 14 15 21 15 32 16	 17 18 26 18 39 18	 ns ns ns ns ns ns
f_{max}	maximum clock frequency $n\overline{CP}_0$, $n\overline{CP}_1$		58	58	MHz
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per counter	notes 1 and 2	21	22	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT390P: 16-lead DIL; plastic (SOT-38Z).
PC74HC/HCT390T: 16-lead mini-pack; plastic (SO-16; SOT-109A).

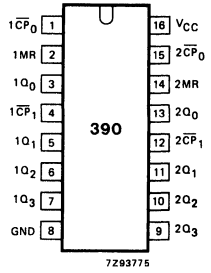


Fig. 1 Pin configuration.

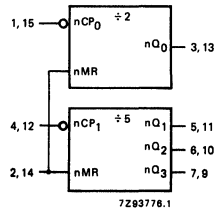


Fig. 2 Logic symbol.

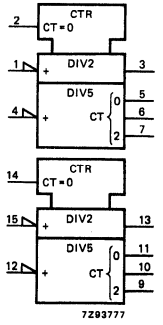


Fig. 3 IEC logic symbol.

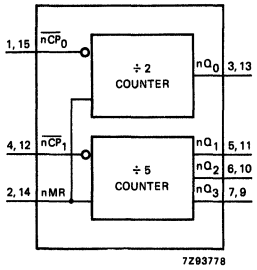


Fig. 4 Functional diagram.

GENERAL DESCRIPTION (Cont'd.)

Each section is triggered by the HIGH-to-LOW transition of the clock inputs ($n\overline{CP}_0$ and $n\overline{CP}_1$).
For BCD decade operation, the nQ_0 output is connected to the $n\overline{CP}_1$ input of the divide-by-5 section. For bi-quinary decade operation, the nQ_3 output is connected to the $n\overline{CP}_0$ input and nQ_0 becomes the decade output.

The master reset inputs (1MR and 2MR) are active HIGH asynchronous inputs to each decade counter which operates on the portion of the counter identified by the "1" and "2" prefixes in the pin configuration. A HIGH level on the nMR input overrides the clocks and sets the four outputs LOW.

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 15	$1\overline{CP}_0$, $2\overline{CP}_0$	clock input divide-by-2 section (HIGH-to-LOW, edge-triggered)
2, 14	1MR, 2MR	asynchronous master reset inputs (active HIGH)
3, 5, 6, 7	$1Q_0$ to $1Q_3$	flip-flop outputs
4, 12	$1\overline{CP}_1$, $2\overline{CP}_1$	clock input divide-by-5 section (HIGH-to-LOW, edge triggered)
8	GND	ground (0 V)
13, 11, 10, 9	$2Q_0$ to $2Q_3$	flip-flop outputs
16	V_{CC}	positive supply voltage

BCD COUNT SEQUENCE FOR 1/2 THE "390"

COUNT	OUTPUTS			
	Q_0	Q_1	Q_2	Q_3
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H

Note

Output Q_0 connected to $n\overline{CP}_1$ with counter input on $n\overline{CP}_0$.

H = HIGH voltage level
L = LOW voltage level

BI-QUINARY COUNT SEQUENCE FOR 1/2 THE "390"

COUNT	OUTPUTS			
	Q_0	Q_1	Q_2	Q_3
0	L	L	L	L
1	L	H	L	L
2	L	L	H	L
3	L	H	H	L
4	L	L	L	H
5	H	L	L	L
6	H	H	L	L
7	H	L	H	L
8	H	H	H	L
9	H	L	L	H

Note

Output Q_3 connected to $n\overline{CP}_0$ with counter input on $n\overline{CP}_1$.

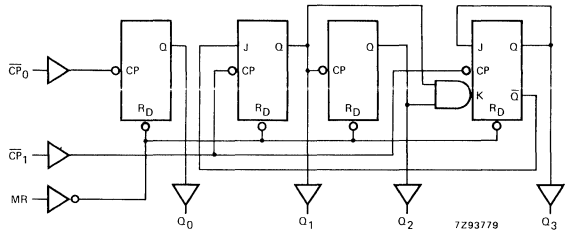


Fig. 5 Logic diagram (one counter).

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay $n\overline{CP}_0$ to nQ_0			145 29 25		180 36 31		220 44 38	ns	2.0 4.5 6.0	Fig. 6
t_{PHL}/t_{PLH}	propagation delay $n\overline{CP}_1$ to nQ_1			155 31 26		195 39 33		235 47 40	ns	2.0 4.5 6.0	Fig. 6
t_{PHL}/t_{PLH}	propagation delay $n\overline{CP}_1$ to nQ_2			210 42 36		265 53 45		315 63 54	ns	2.0 4.5 6.0	Fig. 6
t_{PHL}/t_{PLH}	propagation delay $n\overline{CP}_1$ to nQ_3			155 31 26		195 39 33		235 47 40	ns	2.0 4.5 6.0	Fig. 6
t_{PHL}/t_{PLH}	propagation delay nMR to nQ_n			165 33 28		205 41 35		250 50 43	ns	2.0 4.5 6.0	Fig. 7
t_{THL}/t_{TLH}	output transition time			75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 6
t_W	clock pulse width $n\overline{CP}_0$, $n\overline{CP}_1$	90 18 15			115 23 20		135 27 23		ns	2.0 4.5 6.0	Fig. 6
t_W	master reset pulse width nMR	100 20 17			125 25 21		150 30 26		ns	2.0 4.5 6.0	Fig. 7
t_{rem}	removal time nMR to $n\overline{CP}_n$	75 15 13			95 19 16		110 22 19		ns	2.0 4.5 6.0	Fig. 7
f_{max}	maximum clock pulse frequency $n\overline{CP}_0$, $n\overline{CP}_1$	5 27 32			4 22 25		4 18 21		MHz	2.0 4.5 6.0	Fig. 6

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications.
To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
$n\overline{CP}_0$	0.45
$n\overline{CP}_1$, nMR	0.60

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay $n\overline{CP}_0$ to nQ_0			34		43		51	ns	4.5	Fig. 6
t_{PHL}/t_{PLH}	propagation delay $n\overline{CP}_1$ to nQ_1			38		48		57	ns	4.5	Fig. 6
t_{PHL}/t_{PLH}	propagation delay $n\overline{CP}_1$ to nQ_2			51		64		77	ns	4.5	Fig. 6
t_{PHL}/t_{PLH}	propagation delay $n\overline{CP}_1$ to nQ_3			38		48		57	ns	4.5	Fig. 6
t_{PHL}/t_{PLH}	propagation delay nMR to nQ_n			36		45		54	ns	4.5	Fig. 7
t_{THL}/t_{TLH}	output transition time			15		19		22	ns	4.5	Fig. 6
t_W	clock pulse width $n\overline{CP}_0$, $n\overline{CP}_1$	18			23		27		ns	4.5	Fig. 6
t_W	master reset pulse width nMR	15			19		22		ns	4.5	Fig. 7
t_{rem}	removal time nMR to $n\overline{CP}_n$	15			19		22		ns	4.5	Fig. 7
f_{max}	maximum clock pulse frequency $n\overline{CP}_0$, $n\overline{CP}_1$	27			22		18		MHz	4.5	Fig. 6

AC WAVEFORMS

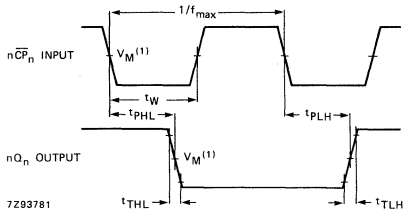


Fig. 6 Waveforms showing the clock ($n\overline{CP}_n$) to output (nQ_n) propagation delays, the clock pulse width, the output transition times and the maximum clock frequency.

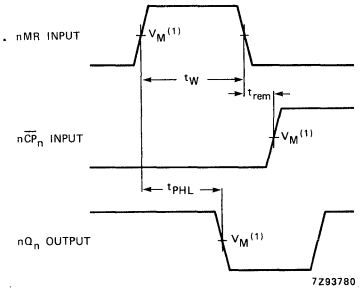


Fig. 7 Waveforms showing the master reset (nMR) pulse width, the master reset to output (nQ_n) propagation delays and the master reset to clock ($n\overline{CP}_n$) removal time.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

OCTAL D-TYPE FLIP-FLOP; POSITIVE-EDGE TRIGGER; 3-STATE; INVERTING

FEATURES

- 3-state inverting outputs for bus oriented applications
- 8-bit positive-edge triggered register
- Common 3-state output enable input
- Independent register and 3-state buffer operation
- Output capability: bus driver
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT564 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7.

The 74HC/HCT564 are octal D-type flip-flops featuring separate D-type inputs for each flip-flop and inverting 3-state outputs for bus oriented applications. A clock (CP) and an output enable ($\overline{OE}$) input are common to all flip-flops.

The 8 flip-flops will store the state of their individual D-inputs that meet the set-up and hold times requirements on the LOW-to-HIGH CP transition.
When $\overline{OE}$ is LOW, the contents of the 8 flip-flops are available at the outputs. When $\overline{OE}$ is HIGH, the outputs go to the high impedance OFF-state. Operation of the $\overline{OE}$ input does not affect the state of the flip-flops.

The "564" is functionally identical to the "574", but has inverting outputs. The "564" is functionally identical to the "534", but has a different pinning.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay CP to $\overline{Q}_n$	C_L = 15 pF; V_{CC} = 5 V	15	16	ns
f_{max}	maximum clock frequency		60	54	MHz
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per flip-flop	notes 1 and 2	30	30	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacitance in pF
   f_o = output frequency in MHz; V_{CC} = supply voltage in V
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT564P: 20-lead DIL; plastic (SOT-146).
PC74HC/HCT564T: 20-lead mini-pack; plastic (SO-20; SOT-163A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	$\overline{OE}$	3-state output enable input (active LOW)
2, 3, 4, 5, 6, 7, 8, 9	D_0 to D_7	data inputs
10	GND	ground (0 V)
11	CP	clock input (LOW-to-HIGH, edge-triggered)
19, 18, 17, 16, 15, 14, 13, 12	$\overline{Q}_0$ to $\overline{Q}_7$	3-state flip-flop outputs
20	V_{CC}	positive supply voltage

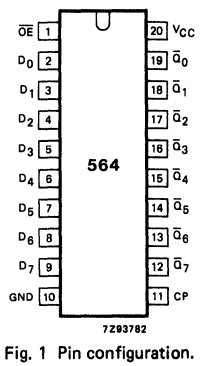


Fig. 1 Pin configuration.

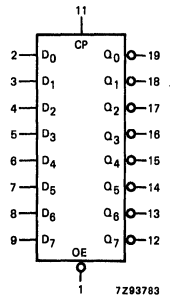


Fig. 2 Logic symbol.

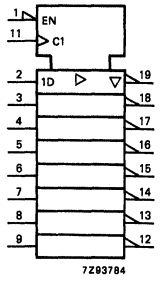


Fig. 3 IEC logic symbol.

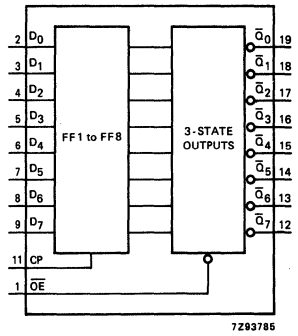


Fig. 4 Functional diagram.

FUNCTION TABLE

OPERATING MODES	INPUTS			INTERNAL FLIP-FLOPS	OUTPUTS
	$\overline{OE}$	CP	D_n		$\overline{Q}_0$ to $\overline{Q}_7$
load and read register	L	↑	l	L	H
	L	↑	h	H	L
load register and disable outputs	H	↑	l	L	Z
	H	↑	h	H	Z

H = HIGH voltage level
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition
L = LOW voltage level
l = LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition
Z = high impedance OFF-state
↑ = LOW-to-HIGH clock transition

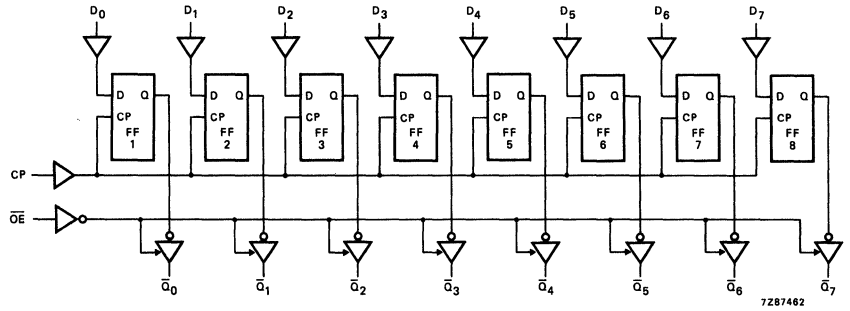


Fig. 5 Logic diagram.

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f = 6$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay CP to $\overline{Q}_n$			165 33 28		205 41 35		250 50 43	ns	2.0 4.5 6.0	Fig. 6
t_{PZH}/t_{PZL}	3-state output enable time $\overline{OE}$ to $\overline{Q}_n$			175 35 30		220 44 37		265 53 45	ns	2.0 4.5 6.0	Fig. 8
t_{PHZ}/t_{PLZ}	3-state output disable time $\overline{OE}$ to $\overline{Q}_n$			150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 8
t_{THL}/t_{TLH}	output transition time			60 12 10		75 15 13		90 18 15	ns	2.0 4.5 6.0	Fig. 6
t_W	clock pulse width HIGH or LOW	80 16 14			100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 6
t_{su}	set-up time D_n to CP	80 16 14			100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 7
t_h	hold time D_n to CP	5 5 5			5 5 5		5 5 5		ns	2.0 4.5 6.0	Fig. 7
f_{max}	maximum clock pulse frequency	6 30 35			5 24 28		4 20 24		MHz	2.0 4.5 6.0	Fig. 6

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver
I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
$\overline{OE}$	0.80
D_0 to D_7	0.25
CP	1.00

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f = 6$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay CP to $\overline{Q}_n$			35		44		53	ns	4.5	Fig. 6
t_{PZH}/t_{PZL}	3-state output enable time $\overline{OE}$ to $\overline{Q}_n$			35		44		53	ns	4.5	Fig. 8
t_{PHZ}/t_{PLZ}	3-state output disable time $\overline{OE}$ to $\overline{Q}_n$			30		38		45	ns	4.5	Fig. 8
t_{THL}/t_{TLH}	output transition time			12		15		18	ns	4.5	Fig. 6
t_W	clock pulse width HIGH or LOW	20			25		30		ns	4.5	Fig. 6
t_{su}	set-up time D_n to CP	20			25		30		ns	4.5	Fig. 7
t_h	hold time D_n to CP	5			5		5		ns	4.5	Fig. 7
f_{max}	maximum clock pulse frequency	25			20		17		MHz	4.5	Fig. 6

AC WAVEFORMS

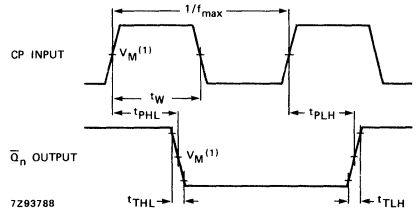


Fig. 6 Waveforms showing the clock (CP) to output ($\overline{Q}_n$) propagation delays, the clock pulse width, the output transition times and the maximum clock pulse frequency.

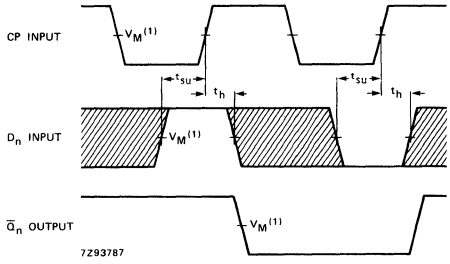


Fig. 7 Waveforms showing the data set-up and hold times for the data input (D_n).

Note to Fig. 7

The shaded areas indicate when the input is permitted to change for predictable output performance.

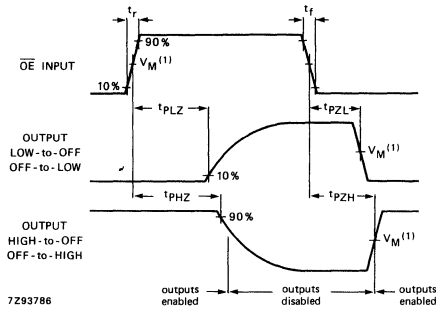


Fig. 8 Waveforms showing the 3-state enable and disable times.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

8-BIT SHIFT REGISTER WITH INPUT LATCHES

FEATURES

- 8-bit parallel input latches
- Shift register has direct overriding load and clear
- Output capability: standard
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT7597 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7.

The 74HC/HCT7597 both consist of an 8-bit storage latch feeding a parallel-in, serial-out 8-bit shift register.

When LE is HIGH, data at the D_n inputs enter the latches. In this condition the latches are transparent, i.e. a latch output will change state each time its corresponding D-input changes.

When LE is LOW the latches store the information that was present at the D-inputs, a set-up time preceding the HIGH-to-LOW transition of LE.

The shift register has a positive edge-triggered clock, direct load (from storage) and clear inputs.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay SH_{CP} to Q	C_L = 15 pF; V_{CC} = 5 V	15	17	ns
	LE to Q		22	27	ns
	$\overline{PL}$ to Q		19	23	ns
	D_7 to Q		19	24	ns
f_{max}	maximum clock frequency SH_{CP}		60	60	MHz
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per package		29	30	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacitance in pF
   f_o = output frequency in MHz; V_{CC} = supply voltage in V
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT7597P: 16-lead DIL; plastic (SOT-38Z).
PC74HC/HCT7597T: 16-lead mini-pack; plastic (SO-16; SOT-109A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
8	GND	ground (0 V)
9	Q	serial data output
10	$\overline{MR}$	asynchronous reset input (active LOW)
11	SH_{CP}	shift clock input (LOW-to-HIGH, edge-triggered)
12	LE	latch enable input (active HIGH)
13	$\overline{PL}$	parallel load input (active LOW)
14	D_S	serial data input
15, 1, 2, 3, 4, 5, 6, 7	D_0 to D_7	parallel data inputs
16	V_{CC}	positive supply voltage

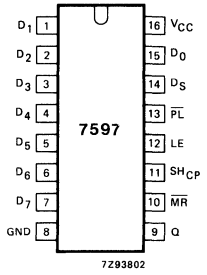


Fig. 1 Pin configuration.

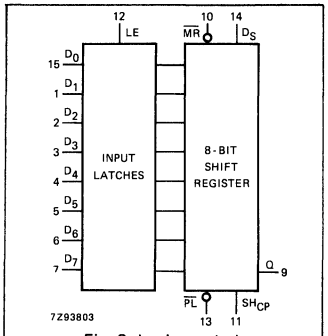


Fig. 2 Logic symbol.

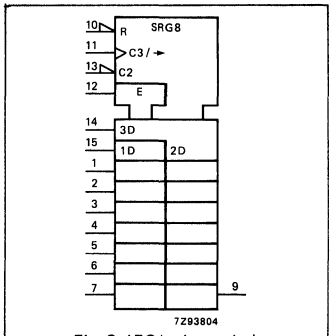


Fig. 3 IEC logic symbol.

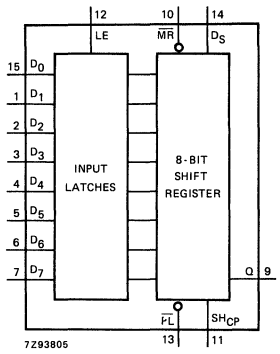


Fig. 4 Functional diagram.

FUNCTION TABLE

LE	SH_{CP}	$\overline{PL}$	$\overline{MR}$	FUNCTION
H	X	X	X	data loaded to input latches
H	X	L	H	data loaded from inputs to shift register
L	X	L	H	stored data loaded to shift register
X	X	L	H	data transferred from input latches to shift register
X	X	L	L	invalid logic, state of shift register indeterminate when signals removed
X	X	H	L	shift register cleared
X	↑	H	H	shift register clocked $Q_n = Q_{n-1}$, $Q_0 = D_S$

H = HIGH voltage level
L = LOW voltage level
X = don't care
↑ = LOW-to-HIGH CP transition

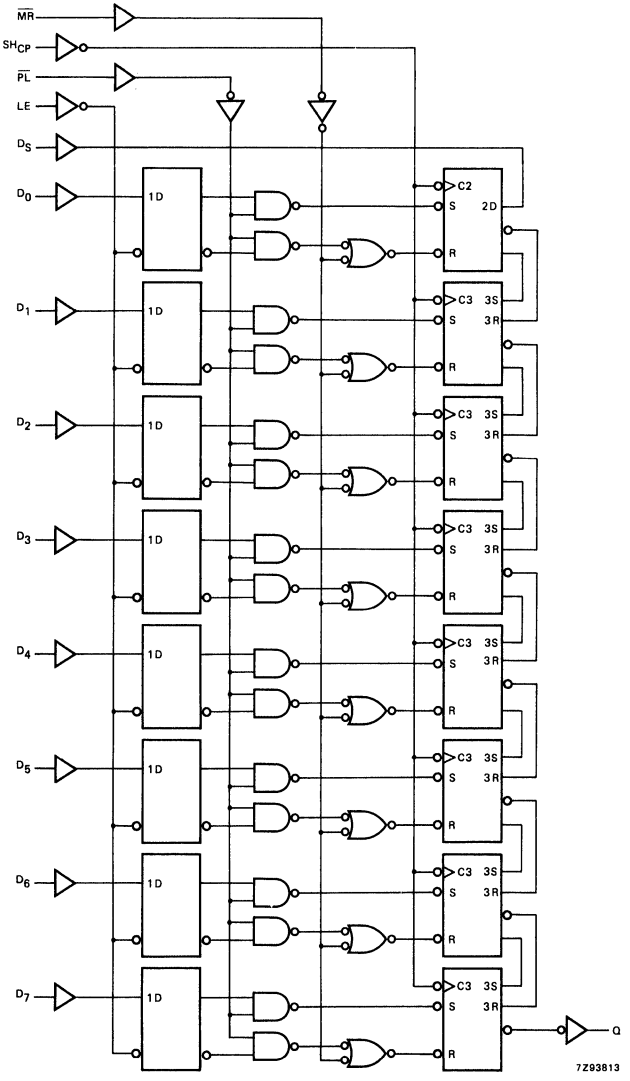


Fig. 5 Logic diagram.

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f = 6$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay SH_{CP} to Q			175 35 30		220 44 37		265 53 45	ns	2.0 4.5 6.0	Fig. 6
t_{PHL}	propagation delay $\overline{MR}$ to Q			175 35 30		220 44 37		265 53 45	ns	2.0 4.5 6.0	Fig. 7
t_{PHL}/t_{PLH}	propagation delay LE to Q			250 50 43		315 63 54		375 75 64	ns	2.0 4.5 6.0	Fig. 8
t_{PHL}/t_{PLH}	propagation delay $\overline{PL}$ to Q			190 38 32		240 48 41		285 57 48	ns	2.0 4.5 6.0	Fig. 9
t_{PHL}/t_{PLH}	propagation delay D_7 to Q			190 38 32		240 48 41		285 57 48	ns	2.0 4.5 6.0	Fig. 10
t_{THL}/t_{TLH}	output transition time			75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 9
t_W	SH_{CP} pulse width HIGH or LOW	80 16 14			100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 6
t_W	LE pulse width HIGH	80 16 14			100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 8
t_W	$\overline{MR}$ pulse width LOW	80 16 14			100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 7
t_W	$\overline{PL}$ pulse width HIGH or LOW	80 16 14			100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 9
t_{rem}	removal time $\overline{MR}$ to SH_{CP}	50 10 9			65 13 11		75 15 13		ns	2.0 4.5 6.0	Fig. 11
t_{rem}	removal time $\overline{MR}$ to $\overline{PL}$	100 20 17			125 25 21		150 30 26		ns	2.0 4.5 6.0	
t_{su}	set-up time D_n to LE	80 16 14			100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 12
t_{su}	set-up time D_S to SH_{CP}	80 16 14			100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 12
t_{su}	set-up time $\overline{PL}$ to SH_{CP}	80 16 14			100 20 17		120 24 20		ns	2.0 4.5 6.0	

AC CHARACTERISTICS FOR 74HC (Continued)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_h	hold time D_n to LE	4 4 4			4 4 4		4 4 4		ns	2.0 4.5 6.0	Fig. 12
t_h	hold time D_S to SH_{CP}	2 2 2			2 2 2		2 2 2		ns	2.0 4.5 6.0	Fig. 12
t_h	hold time $\overline{PL}$ to SH_{CP}	2 2 2			2 2 2		2 2 2		ns	2.0 4.5 6.0	
f_{max}	maximum pulse frequency SH_{CP}	6 30 35			5 24 28		4 20 24		MHz	2.0 4.5 6.0	Fig. 6

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications.
To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
D_S	0.25
D_n	0.40
$\overline{PL}$, $\overline{MR}$, LE, SH_{CP}	1.50

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f = 6$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay SH_{CP} to Q			35		44		53	ns	4.5	Fig. 6
t_{PHL}	propagation delay $\overline{MR}$ to Q			42		53		63	ns	4.5	Fig. 7
t_{PHL}/t_{PLH}	propagation delay LE to Q			56		70		84	ns	4.5	Fig. 8
t_{PHL}/t_{PLH}	propagation delay $\overline{PL}$ to Q			46		58		69	ns	4.5	Fig. 9
t_{PHL}/t_{PLH}	propagation delay D_7 to Q			49		61		74	ns	4.5	Fig. 10
t_{THL}/t_{TLH}	output transition time			15		19		22	ns	4.5	Fig. 9
t_W	SH_{CP} pulse width HIGH or LOW	16			20		24		ns	4.5	Fig. 6
t_W	LE pulse width HIGH	16			20		24		ns	4.5	Fig. 8
t_W	$\overline{MR}$ pulse width LOW	20			25		30		ns	4.5	Fig. 7
t_W	$\overline{PL}$ pulse width HIGH or LOW	18			23		27		ns	4.5	Fig. 9
t_{rem}	removal time $\overline{MR}$ to SH_{CP}	10			13		15		ns	4.5	Fig. 11
t_{rem}	removal time $\overline{MR}$ to $\overline{PL}$	20			25		30		ns	4.5	
t_{su}	set-up time D_n to LE	16			20		24		ns	4.5	Fig. 12
t_{su}	set-up time D_S to SH_{CP}	16			20		24		ns	4.5	Fig. 12
t_{su}	set-up time $\overline{PL}$ to SH_{CP}	16			20		24		ns	4.5	
t_h	hold time D_n to LE	4			4		4		ns	4.5	Fig. 12
t_h	hold time D_S to SH_{CP}	2			2		2		ns	4.5	Fig. 12
t_h	hold time PL to SH_{CP}	2			2		2		ns	4.5	
f_{max}	maximum pulse frequency SH_{CP}	30			24		20		MHz	4.5	Fig. 6

AC WAVEFORMS

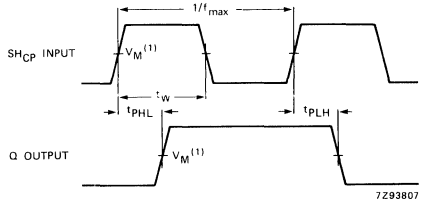


Fig. 6 Waveforms showing the SH_{CP} input to Q output propagation delays, the SH_{CP} pulse width and maximum clock pulse frequency.

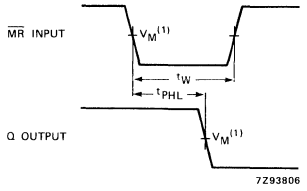


Fig. 7 Waveforms showing the $\overline{MR}$ input to Q output propagation delay and the $\overline{MR}$ pulse width.

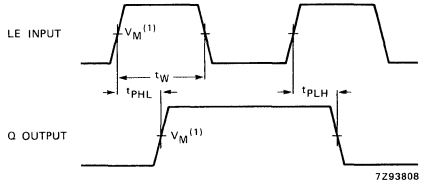


Fig. 8 Waveforms showing the LE input to Q output propagation delays and the LE pulse width.

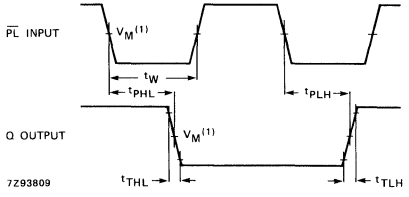


Fig. 9 Waveforms showing the $\overline{PL}$ input to Q output propagation delays, $\overline{PL}$ pulse width and output transition times.

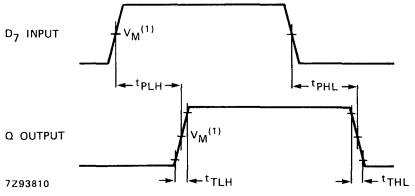


Fig. 10 Waveforms showing the D_7 input to Q output propagation delays.

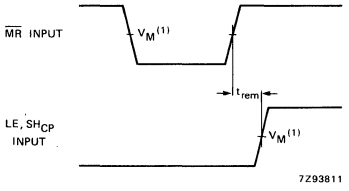


Fig. 11 Waveforms showing the $\overline{MR}$ input to LE, SH_{CP} removal times.

AC WAVEFORMS (Continued)

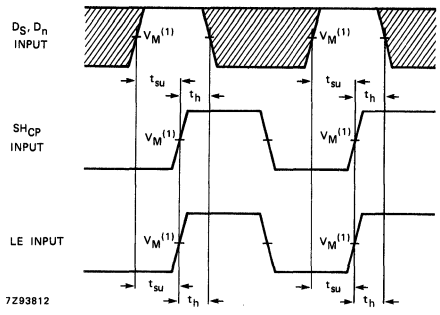


Fig. 12 Waveforms showing hold and set-up times for D_S, D_n inputs to SH_{CP}, LE inputs.

Note to Fig. 12

The shaded areas indicate when the input is permitted to change for predictable output performance.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

JOHNSON DECADE COUNTER WITH 10 DECODED OUTPUTS

FEATURES

- **Output capability: standard**
- **I_{CC} category: MSI**

GENERAL DESCRIPTION

The 74HC/HCT4017 are high-speed Si-gate CMOS devices and are pin compatible with the "4017" of the "4000B" series. They are specified in compliance with JEDEC standard no. 7.

The 74HC/HCT4017 are 5-stage Johnson decade counters with 10 decoded active HIGH outputs (Q_0 to Q_9), an active LOW output from the most significant flip-flop ($\overline{Q}_{5\text{-}9}$), active HIGH and active LOW clock inputs (CP_0 and $\overline{CP}_1$) and an overriding asynchronous master reset input (MR).

The counter is advanced by either a LOW-to-HIGH transition at CP_0 while $\overline{CP}_1$ is LOW or a HIGH-to-LOW transition at $\overline{CP}_1$ while CP_0 is HIGH (see also function table).

When cascading counters, the $\overline{Q}_{5\text{-}9}$ output, which is LOW while the counter is in states 5, 6, 7, 8 and 9, can be used to drive the CP_0 input of the next counter.

A HIGH on MR resets the counter to zero ($Q_0 = \overline{Q}_{5\text{-}9}$ = HIGH; Q_1 to Q_9 = LOW) independent of the clock inputs (CP_0 and $\overline{CP}_1$).

Automatic code correction of the counter is provided by an internal circuit: following any illegal code the counter returns to a proper counting mode within 11 clock pulses.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay CP_0, $\overline{CP}_1$ to Q_n	C_L = 15 pF; V_{CC} = 5 V	19	21	ns
f_{max}	maximum clock frequency		60	60	MHz
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per package	notes 1 and 2	35	36	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT4017P: 16-lead DIL; plastic (SOT-38Z).
PC74HC/HCT4017T: 16-lead mini-pack; plastic (SO-16; SOT-109A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
3, 2, 4, 7, 10, 1, 5, 6, 9, 11	Q_0 to Q_9	decoded outputs
8	GND	ground (0 V)
12	$\overline{Q}_{5\text{-}9}$	carry output (active LOW)
13	$\overline{CP}_1$	clock input (HIGH-to-LOW, edge-triggered)
14	CP_0	clock input (LOW-to-HIGH, edge-triggered)
15	MR	master reset input (active HIGH)
16	V_{CC}	positive supply voltage

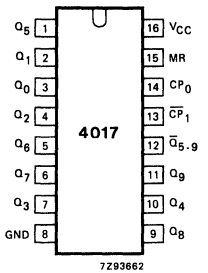


Fig. 1 Pin configuration.

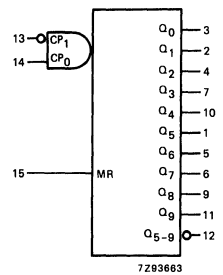


Fig. 2 Logic symbol.

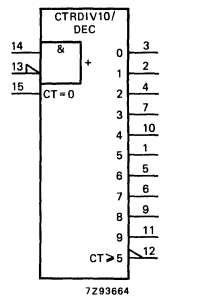


Fig. 3 IEC logic symbol.

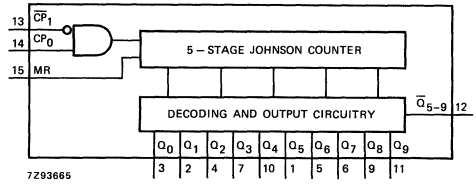


Fig. 4 Functional diagram.

FUNCTION TABLE

MR	CP_0	$\overline{CP}_1$	OPERATION
H	X	X	$Q_0 = Q_{5-9} = H$; Q_1 to $Q_9 = L$
L	H	↓	counter advances
L	↑	L	counter advances
L	L	X	no change
L	X	H	no change
L	H	↑	no change
L	↓	L	no change

H = HIGH voltage level
L = LOW voltage level
X = don't care
↑ = LOW-to-HIGH clock transition
↓ = HIGH-to-LOW clock transition

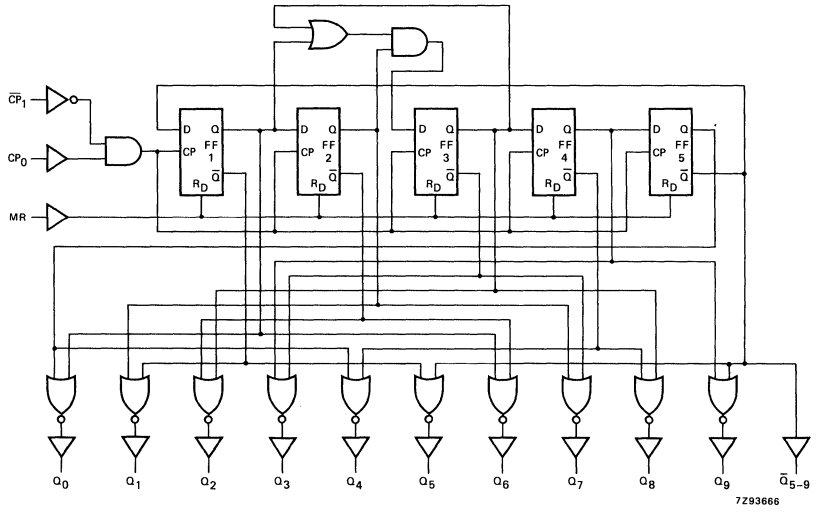


Fig. 5 Logic diagram.

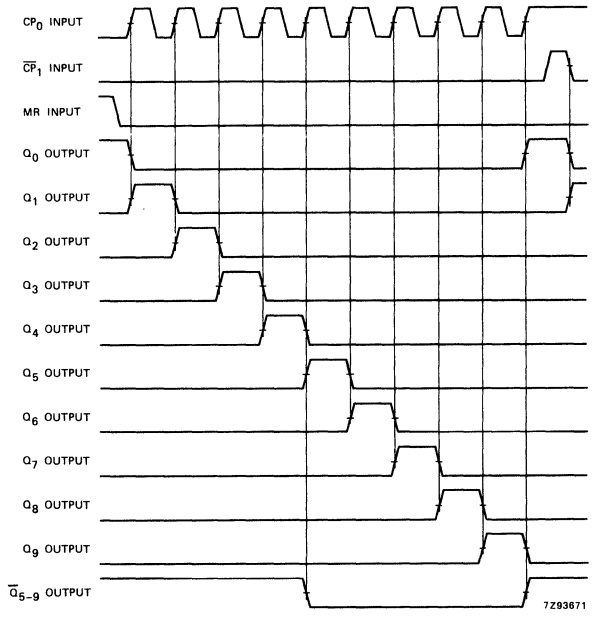


Fig. 6 Timing diagram.

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f = 6$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay CP_0 to Q_n			230 46 39		290 58 49		345 69 59	ns	2.0 4.5 6.0	Fig. 9
t_{PHL}/t_{PLH}	propagation delay CP_0 to $\overline{Q}_{5\text{-}9}$			230 46 39		290 58 49		345 69 59	ns	2.0 4.5 6.0	Fig. 9
t_{PHL}/t_{PLH}	propagation delay $\overline{CP}_1$ to Q_n			250 50 43		315 63 54		375 75 64	ns	2.0 4.5 6.0	Fig. 9
t_{PHL}/t_{PLH}	propagation delay $\overline{CP}_1$ to $\overline{Q}_{5\text{-}9}$			250 50 43		315 63 54		375 75 64	ns	2.0 4.5 6.0	Fig. 9
t_{PHL}	propagation delay MR to Q_{1-9}			230 46 39		290 58 49		345 69 59	ns	2.0 4.5 6.0	Fig. 8
t_{PLH}	propagation delay MR to $\overline{Q}_{5\text{-}9}$, Q_0			230 46 39		290 58 49		345 69 59	ns	2.0 4.5 6.0	Fig. 8
t_{THL}/t_{TLH}	output transition time			75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 9
t_W	clock pulse width HIGH or LOW	80 16 14			100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 8
t_W	master reset pulse width; HIGH	80 16 14			100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 8
t_{rem}	removal time MR to CP_0, $\overline{CP}_1$	5 5 5			5 5 5		5 5 5		ns	2.0 4.5 6.0	Fig. 8
t_{su}	set-up time $\overline{CP}_1$ to CP_0; CP_0 to $\overline{CP}_1$	75 15 13			95 19 16		110 22 19		ns	2.0 4.5 6.0	Fig. 7
t_h	hold time CP_0 to $\overline{CP}_1$; $\overline{CP}_1$ to CP_0	50 10 9			65 13 11		75 15 13		ns	2.0 4.5 6.0	Fig. 7
f_{max}	maximum clock pulse frequency	6 30 25			5 24 28		4 20 24		MHz	2.0 4.5 6.0	Fig. 8

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
$\overline{CP}_1$	0.40
CP_0	0.25
MR	0.50

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f = 6$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay CP_0 to Q_n			46		58		69	ns	4.5	Fig. 9
t_{PHL}/t_{PLH}	propagation delay CP_0 to $\overline{Q}_{5\text{-}9}$			46		58		69	ns	4.5	Fig. 9
t_{PHL}/t_{PLH}	propagation delay $\overline{CP}_1$ to Q_n			50		63		75	ns	4.5	Fig. 9
t_{PHL}/t_{PLH}	propagation delay $\overline{CP}_1$ to $\overline{Q}_{5\text{-}9}$			50		63		75	ns	4.5	Fig. 9
t_{PHL}/t_{PLH}	propagation delay MR to Q_{1-9}			46		58		69	ns	4.5	Fig. 8
t_{PLH}	propagation delay MR to $\overline{Q}_{5\text{-}9}$, Q_0			46		58		69	ns	4.5	Fig. 8
t_{THL}/t_{TLH}	output transition time			15		19		22	ns	4.5	Fig. 9
t_W	clock pulse width HIGH or LOW	16			20		24		ns	4.5	Fig. 8
t_W	master reset pulse width; HIGH	16			20		24		ns	4.5	Fig. 8
t_{rem}	removal time MR to CP_0, $\overline{CP}_1$	5			5		5		ns	4.5	Fig. 8
t_{su}	set-up time $\overline{CP}_1$ to CP_0; CP_0 to $\overline{CP}_1$	15			19		22		ns	4.5	Fig. 7
t_h	hold time CP_0 to $\overline{CP}_1$; $\overline{CP}_1$ to CP_0	10			13		15		ns	4.5	Fig. 7
f_{max}	maximum clock pulse frequency	30			24		20		MHz	4.5	Fig. 8

AC WAVEFORMS

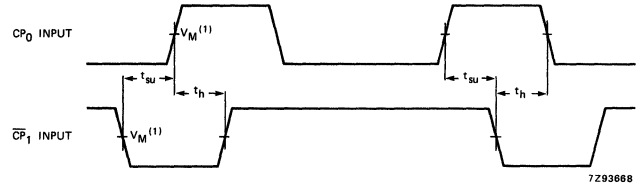


Fig. 7 Waveforms showing hold and set-up times for CP_0 to $\overline{CP}_1$ and $\overline{CP}_1$ to CP_0.

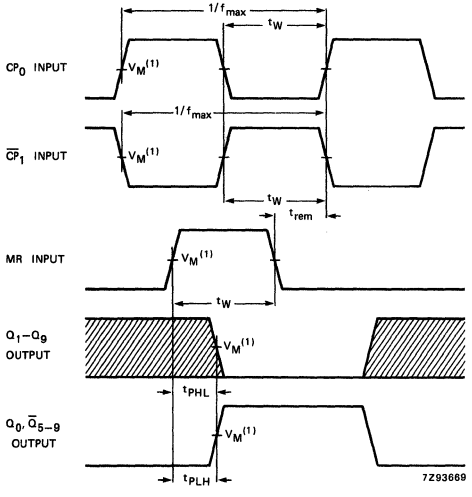


Fig. 8 Waveforms showing the minimum pulse widths for CP_0, $\overline{CP}_1$ and MR inputs; the recovery time for MR and the propagation delays for MR to Q_n and $\overline{Q}_{5\text{-}9}$ outputs.

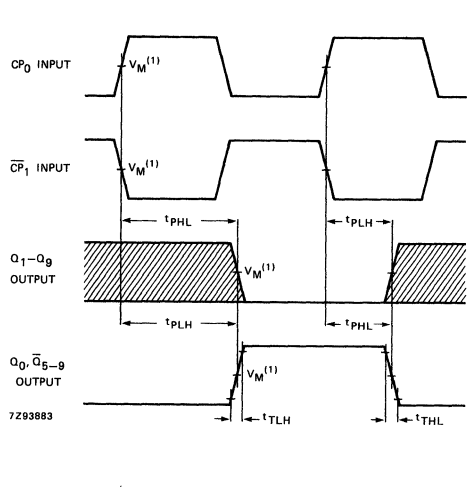


Fig. 9 Waveforms showing the propagation delays for CP_0, $\overline{CP}_1$ to Q_n, $\overline{Q}_{5\text{-}9}$ outputs and the output transition times.

Note to Figs 8 and 9

Conditions:
$\overline{CP}_1$ = LOW while CP_0 is triggered on a LOW-to-HIGH transition and CP_0 = HIGH, while $\overline{CP}_1$ is triggered on a HIGH-to-LOW transition.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

APPLICATION INFORMATION

Some applications for the "4017" are:

- Decade counter with decimal decoding
- 1 out of n decoding counter (when cascaded)
- Sequential controller
- Timer

Figure 10 shows a technique for extending the number of decoded output states for the "4017".
Decoded outputs are sequential within each stage and from stage to stage, with no dead time (except propagation delay).

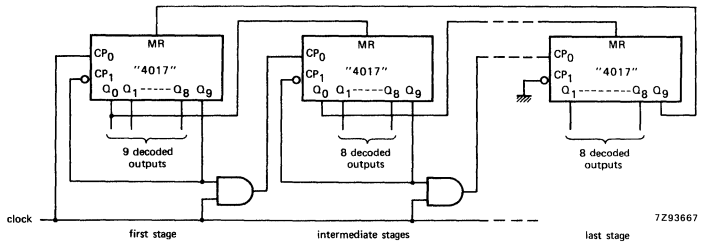


Fig. 10 Counter expansion

Note to Fig. 10

It is essential not to enable the counter on $\overline{CP}_1$ when CP_0 is HIGH, or on CP_0 when $\overline{CP}_1$ is LOW, as this would cause an extra count.

14-STAGE BINARY RIPPLE COUNTER

FEATURES

- **Output capability: standard**
- **I_{CC} category: MSI**

GENERAL DESCRIPTION

The 74HC/HCT4020 are high-speed Si-gate CMOS devices and are pin compatible with the "4020" of the "4000B" series. They are specified in compliance with JEDEC standard no. 7.

The 74HC/HCT4020 are 14-stage binary ripple counters with a clock input ($\overline{CP}$), an overriding asynchronous master reset input (MR) and twelve fully buffered parallel outputs (Q_0, Q_3 to Q_{13}).

The counter is advanced on the HIGH-to-LOW transition of $\overline{CP}$.

A HIGH on MR clears all counter stages and forces all outputs LOW, independent of the state of $\overline{CP}$.

Each counter stage is a static toggle flip-flop.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay $\overline{CP}$ to Q_0 Q_n to Q_{n+1} MR to Q_n	C_L = 15 pF V_{CC} = 5 V	 11 7 18	 15 7 20	 ns ns ns
f_{max}	maximum clock frequency		60	50	MHz
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per package	notes 1 and 2	19	20	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT4020P: 16-lead DIL; plastic (SOT-38Z).
PC74HC/HCT4020T: 16-lead mini-pack; plastic (SO-16; SOT-109A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
9, 7, 5, 4, 6, 13, 12, 14, 15, 1, 2, 3	Q_0, Q_3 to Q_{13}	parallel outputs
8	GND	ground (0 V)
10	$\overline{CP}$	clock input (HIGH-to-LOW, edge-triggered)
11	MR	master reset input (active HIGH)
16	V_{CC}	positive supply voltage

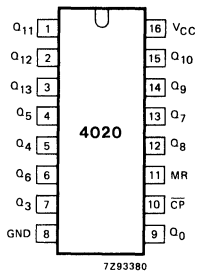


Fig. 1 Pin configuration.

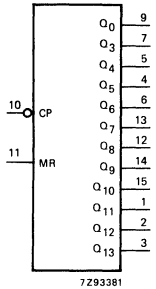


Fig. 2 Logic symbol.

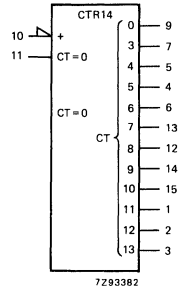


Fig. 3 IEC logic symbol.

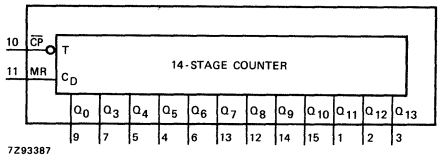


Fig. 4 Functional diagram.

FUNCTION TABLE

INPUTS		OUTPUTS
$\overline{CP}$	MR	Q_0, Q_3 to Q_{13}
↑	L	no change
↓	L	count
X	H	L

H = HIGH voltage level
L = LOW voltage level
X = don't care
↑ = LOW-to-HIGH clock transition
↓ = HIGH-to-LOW clock transition

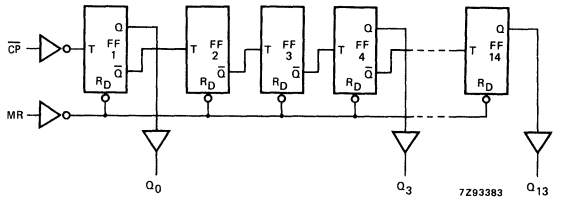


Fig. 5 Logic diagram.

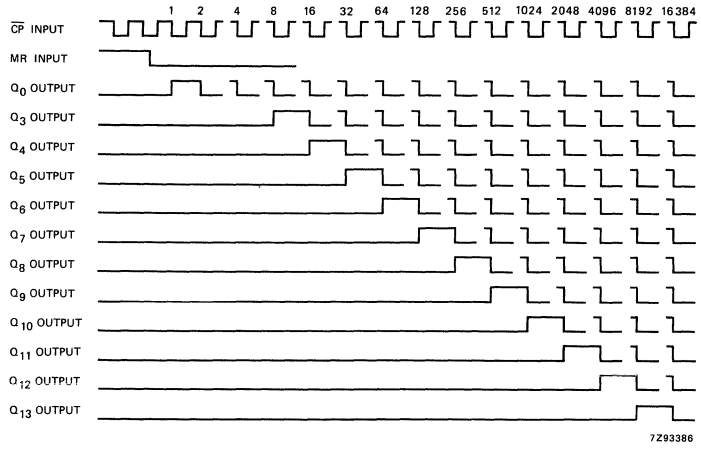


Fig. 6 Timing diagram.

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delay $\overline{CP}$ to Q_0			140 28 24		175 35 30		210 42 36	ns	2.0 4.5 6.0	Fig. 7
t_{PHL}/ t_{PLH}	propagation delay Q_n to Q_{n+1}			75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 7
t_{PHL}	propagation delay MR to Q_n			200 40 34		250 50 43		300 60 51	ns	2.0 4.5 6.0	Fig. 8
t_{THL}/ t_{TLH}	output transition time			75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 7
t_W	clock pulse width HIGH	80 16 14			100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 7
t_W	master reset pulse width HIGH	80 16 14			100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 8
t_{rem}	removal time MR to $\overline{CP}$	50 10 9			65 13 11		75 15 13		ns	2.0 4.5 6.0	Fig. 8
f_{max}	maximum clock pulse frequency	6 30 35			5 24 28		4 20 24		MHz	2.0 4.5 6.0	Fig. 7

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications.
To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
$\overline{CP}$	0.85
MR	1.10

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay $\overline{CP}$ to Q_0			36		45		54	ns	4.5	Fig. 7
t_{PHL}/t_{PLH}	propagation delay Q_n to Q_{n+1}			15		19		22	ns	4.5	Fig. 7
t_{PHL}	propagation delay MR to Q_n			45		56		68	ns	4.5	Fig. 8
t_{THL}/t_{TLH}	output transition time			15		19		22	ns	4.5	Fig. 7
t_W	clock pulse width HIGH	20			25		30		ns	4.5	Fig. 7
t_W	master reset pulse width HIGH	20			25		30		ns	4.5	Fig. 8
t_{rem}	removal time MR to $\overline{CP}$	10			13		15		ns	4.5	Fig. 8
f_{max}	maximum clock pulse frequency	23			24		20		MHz	4.5	Fig. 7

AC WAVEFORMS

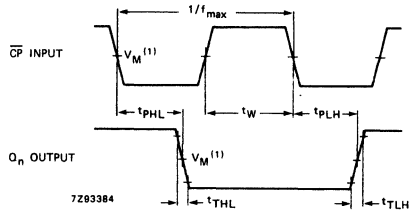


Fig. 7 Waveforms showing the clock ($\overline{CP}$) to output (Q_n) propagation delays, the clock pulse width, the output transition times and the maximum clock frequency.

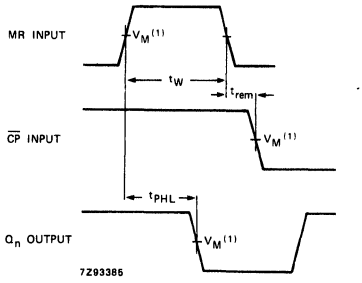


Fig. 8 Waveforms showing the master reset (MR) pulse width, the master reset to output (Q_n) propagation delays and the master reset to clock ($\overline{CP}$) removal time.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

12-STAGE BINARY RIPPLE COUNTER

FEATURES

- **Output capability: standard**
- **I_{CC} category: MSI**

GENERAL DESCRIPTION

The 74HC/HCT4040 are high-speed Si-gate CMOS devices and are pin compatible with the "4040" of the "4000B" series. They are specified in compliance with JEDEC standard no. 7.

The 74HC/HCT4040 are 12-stage binary ripple counters with a clock input ($\overline{CP}$), an overriding asynchronous master reset input (MR) and twelve parallel outputs (Q_0 to Q_{11}).

The counter is advances on the HIGH-to-LOW transition of $\overline{CP}$.

A HIGH on MR clears all counter stages and forces all outputs LOW, independent of the state of $\overline{CP}$.

Each counter stage is a static toggle flip-flop.

APPLICATIONS

- **Frequency dividing circuits**
- **Time delay circuits**
- **Control counters**

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay $\overline{CP}$ to Q_0 Q_n to Q_{n+1}	C_L = 15 pF V_{CC} = 5 V	14 8	16 8	ns ns
f_{max}	maximum clock frequency		60	60	MHz
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per package	notes 1 and 2	20	20	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT4040P: 16-lead DIL; plastic (SOT-38Z).
PC74HC/HCT4040T: 16-lead mini-pack; plastic (SO-16; SOT-109A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
8	GND	ground (0 V)
9, 7, 6, 5, 3, 2, 4, 13, 12, 14, 15, 1	Q_0 to Q_{11}	parallel outputs
10	$\overline{CP}$	clock input (HIGH-to-LOW, edge-triggered)
11	MR	master reset input (active HIGH)
16	V_{CC}	positive supply voltage

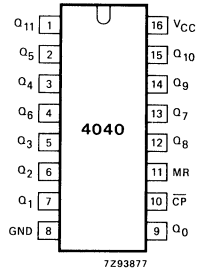


Fig. 1 Pin configuration.

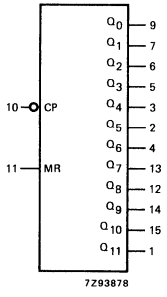


Fig. 2 Logic symbol.

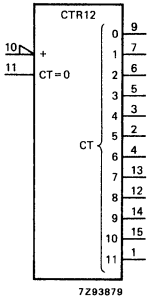


Fig. 3 IEC logic symbol.

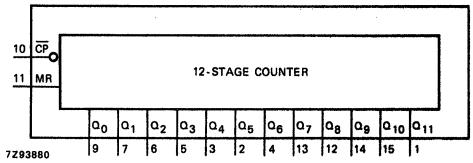


Fig. 4 Functional diagram.

FUNCTION TABLE

INPUTS		OUTPUTS
$\overline{CP}$	MR	Q_n
↑	L	no change
↓	L	count
X	H	L

H = HIGH voltage level
L = LOW voltage level
X = don't care
↑ = LOW-to-HIGH clock transition
↓ = HIGH-to-LOW clock transition

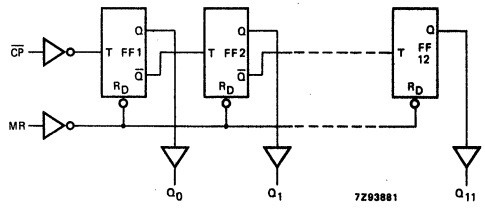


Fig. 5 Logic diagram.

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f = 6$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay $\overline{CP}$ to Q_0			150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 6
t_{PHL}/t_{PLH}	propagation delay Q_n to Q_{n+1}			100 20 17		125 25 21		150 26 22	ns	2.0 4.5 6.0	Fig. 6
t_{PHL}	propagation delay MR to Q_n			200 40 34		250 50 43		300 60 51	ns	2.0 4.5 6.0	Fig. 6
t_{THL}/t_{TLH}	output transition time			75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 6
t_W	clock pulse width HIGH or LOW	80 16 14			100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 6
t_W	master reset pulse width; HIGH	80 16 14			100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 6
t_{rem}	removal time MR to $\overline{CP}$	50 10 9			65 13 11		75 15 13		ns	2.0 4.5 6.0	Fig. 6
f_{max}	maximum clock pulse frequency	6 30 35			5 24 28		4 20 24		MHz	2.0 4.5 6.0	Fig. 6

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications.
To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
$\overline{CP}$	0.85
MR	1.10

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f = 6$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay $\overline{CP}$ to Q_0			35		44		53	ns	4.5	Fig. 6
t_{PHL}/t_{PLH}	propagation delay Q_n to Q_{n+1}			20		25		30	ns	4.5	Fig. 6
t_{PHL}	propagation delay MR to Q_n			45		56		68	ns	4.5	Fig. 6
t_{THL}/t_{TLH}	output transition time			15		19		22	ns	4.5	Fig. 6
t_W	clock pulse width HIGH or LOW	16			20		24		ns	4.5	Fig. 6
t_W	master reset pulse width; HIGH	16			20		24		ns	4.5	Fig. 6
t_{rem}	removal time MR to $\overline{CP}$	10			13		15		ns	4.5	Fig. 6
f_{max}	maximum clock pulse frequency	30			24		20		MHz	4.5	Fig. 6

AC WAVEFORMS

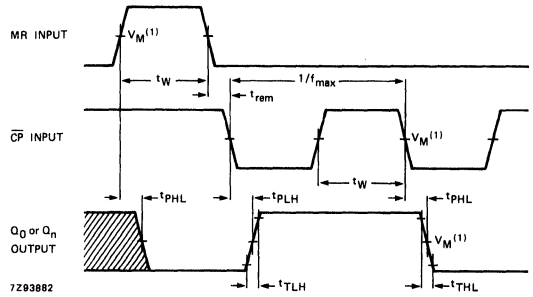


Fig. 6 Waveforms showing the clock ($\overline{CP}$) to output (Q_n) propagation delays, the clock pulse width, the output transition times and the maximum clock pulse frequency.

Also showing the master reset (MR) pulse width, the master reset to output (Q_n) propagation delays and the master reset to clock ($\overline{CP}$) removal time.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

HEX INVERTING HIGH-TO-LOW LEVEL SHIFTER

FEATURES

- **Output capability: standard**
- **I_{CC} category: SSI**

GENERAL DESCRIPTION

The 74HC4049 is a high-speed Si-gate CMOS device and is pin compatible with the "4049" of the "4000B" series. It is specified in compliance with JEDEC standard no. 7.

The 74HC4049 provides six inverting buffers with a modified input protection structure, which has no diode connected to V_{CC}. Input voltages of up to 15 V may therefore be used.
This feature enables the inverting buffers to be used as logic level translators, which will convert high level logic to low level logic, while operating from a low voltage power supply. For example 15 V logic ("4000B series") can be converted down to 2 V logic.

The actual input switch level remains related to the V_{CC} and is the same as mentioned in the family characteristics. At the same time each part can be used as a simple inverter without level translation.

APPLICATIONS

- **Converting 15 V logic ("4000B" series) down to 2 V logic.**

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
			HC	
t_{PHL}/t_{PLH}	propagation delay nA to n$\overline{Y}$	C_L = 15 pF V_{CC} = 5 V	7	ns
C_I	input capacitance		3.5	pF
C_{PD}	power dissipation capacitance per buffer	note 1	15	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6ns

Note

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V

ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC4049P: 16-lead DIL; plastic (SOT-38Z).
PC74HC4049T: 16-lead mini-pack; plastic (SO-16; SOT-109A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	V_{CC}	positive supply voltage
2, 4, 6, 10, 12, 15	1$\overline{Y}$ to 6$\overline{Y}$	data outputs
3, 5, 7, 9, 11, 14	1A to 6A	data inputs
8	GND	ground (0 V)
13, 16	n.c.	not connected

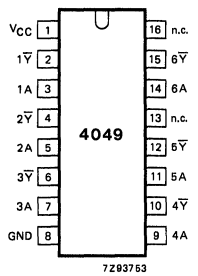


Fig. 1 Pin configuration.

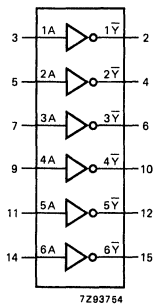


Fig. 2 Logic symbol.

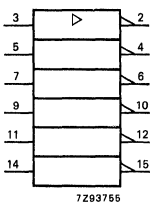


Fig. 3 IEC logic symbol.

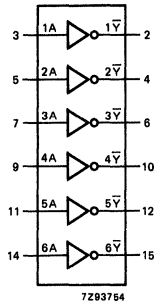


Fig. 4 Functional diagram.

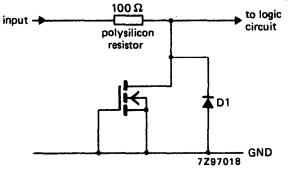


Fig. 5 Input protection for HC4049. Single sided thick oxide field effect transistor as input protection.

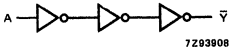


Fig. 6 Logic diagram (one level shifter).

FUNCTION TABLE

INPUT	OUTPUT
nA	nȲ
L H	H L

H = HIGH voltage level
L = LOW voltage level

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)
Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
V_{CC}	DC supply voltage	−0.5	+7	V	
V_{IK}	DC input voltage range	−0.5	+16	V	
$-I_{IK}$	DC input diode current		20	mA	for $V_I < -0.5$ V
$\pm I_{OK}$	DC output diode current		20	mA	for $V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V
$\pm I_O$	DC output source or sink current - standard outputs		25	mA	for $-0.5\text{ V} < V_O < V_{CC} + 0.5$ V
$\pm I_{CC}$; $\pm I_{GND}$	DC V_{CC} or GND current for types with: - standard outputs		50	mA	
T_{stg}	storage temperature range	−65	+150	°C	
P_{tot}	power dissipation per package				for temperature range: −40 to +85 °C 74HC
	plastic DIL		500	mW	above +60 °C: derate linearly with 8 mW/K
	plastic mini-pack (SO)		400	mW	above +60 °C: derate linearly with 6 mW/K
P_{tot}	power dissipation per package				for temperature range: −40 to +125 °C 74HC
	plastic DIL		500	mW	above +70 °C: derate linearly with 8 mW/K
	plastic mini-pack (SO)		400	mW	above +70 °C: derate linearly with 6 mW/K

DC CHARA TERISTICS FOR 74HC

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		74HC								V_{CC} V	V_I	OTHER
		+25			−40 to +85		−40 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
V_{IH}	HIGH level input voltage	1.5 3.15 4.2	1.3 2.4 3.1		1.5 3.15 4.2		1.5 3.15 4.2		V	2.0 4.5 6.0		
V_{IL}	LOW level input voltage		0.7 1.8 2.3	0.5 1.35 1.8		0.5 1.35 1.8		0.5 1.35 1.8	V	2.0 4.5 6.0		
V_{OH}	HIGH level output voltage all outputs	1.9 4.4 5.9	2.0 4.5 6.0		1.9 4.4 5.9		1.9 4.4 5.9		V	2.0 4.5 6.0	V_{IH} or V_{IL}	$-I_O = 20\ \mu A$ $-I_O = 20\ \mu A$ $-I_O = 20\ \mu A$
V_{OH}	HIGH level output voltage standard outputs	3.98 5.48			3.84 5.34		3.7 5.2		V	4.5 6.0	V_{IH} or V_{IL}	$-I_O = 4.0$ mA $-I_O = 5.2$ mA
V_{OL}	LOW level output voltage all outputs			0.1 0.1 0.1		0.1 0.1 0.1		0.1 0.1 0.1	V	2.0 4.5 6.0	V_{IH} or V_{IL}	$I_O = 20\ \mu A$ $I_O = 20\ \mu A$ $I_O = 20\ \mu A$
V_{OL}	LOW level output voltage standard outputs			0.26 0.26		0.33 0.33		0.4 0.4	V	4.5 6.0	V_{IH} or V_{IL}	$I_O = 4.0$ mA $I_O = 5.2$ mA
$\pm I_I$	input leakage current			0.1		1.0		1.0	μA	6.0	V_{CC} or GND	
				0.5		5.0		5.0	μA	2.0 to 6.0	15 V	
I_{CC}	quiescent supply current			2.0		20.0		40.0	μA	6.0	15 V or GND	

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f = 6$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delay nA to nȲ			85 17 14		105 21 18		130 26 22	ns	2.0 4.5 6.0	Fig. 7
t_{THL}/ t_{TLH}	output transition time			75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 7

AC WAVEFORMS

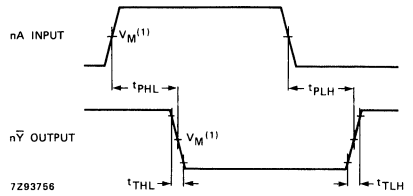


Fig. 7 Waveforms showing the input (nA) to output (nȲ) propagation delays and the output transition times.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

HEX HIGH-TO-LOW LEVEL SHIFTER

FEATURES

- **Output capability: standard**
- **I_{CC} category: SSI**

GENERAL DESCRIPTION

The 74HC4050 is a high-speed Si-gate CMOS device and is pin compatible with the "4050" of the "4000B" series. It is specified in compliance with JEDEC standard no. 7.

The 74HC4050 provides six non-inverting buffers with a modified input protection structure, which has no diode connected to V_{CC}. Input voltages of up to 15 V may therefore be used. This feature enables the non-inverting buffers to be used as logic level translators, which will convert high level logic to low level logic, while operating from a low voltage power supply. For example 15 V logic ("4000B series") can be converted down to 2 V logic.

The actual input switch level remains related to the V_{CC} and is the same as mentioned in the family characteristics.

APPLICATIONS

- **Converting 15 V logic ("4000B" series) down to 2 V logic.**

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
			HC	
t_{PHL}/t_{PLH}	propagation delay nA to nY	C_L = 15 pF V_{CC} = 5 V	7	ns
C_I	input capacitance		3.5	pF
C_{PD}	power dissipation capacitance per buffer	note 1	14	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Note

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):

   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:

   f_i = input frequency in MHz
   f_o = output frequency in MHz
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V

ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC4050P: 16-lead DIL; plastic (SOT-38Z).
PC74HC4050T: 16-lead mini-pack; plastic (SO-16; SOT-109A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	V_{CC}	positive supply voltage
2, 4, 6, 10, 12, 15	1Y to 6Y	data outputs
3, 5, 7, 9, 11, 14	1A to 6A	data inputs
8	GND	ground (0 V)
13, 16	n.c.	not connected

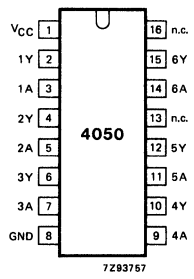


Fig. 1 Pin configuration.

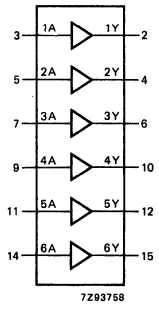


Fig. 2 Logic symbol.

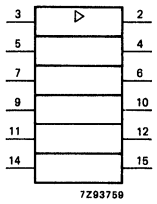


Fig. 3 IEC logic symbol.

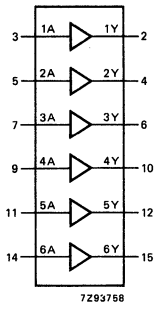


Fig. 4 Functional diagram.

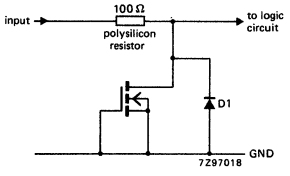


Fig. 5 Input protection for HC4050. Single sided thick oxide field effect transistor as input protection.

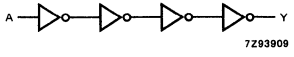


Fig. 6 Logic diagram (one level shifter).

FUNCTION TABLE

INPUT	OUTPUT
nA	nY
L	L
H	H

H = HIGH voltage level
L = LOW voltage level

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)
Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
V_{CC}	DC supply voltage	−0.5	+7	V	
V_{IK}	DC input voltage range	−0.5	+16	V	
$-I_{IK}$	DC input diode current		20	mA	for $V_I < -0.5$ V
$\pm I_{OK}$	DC output diode current		20	mA	for $V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V
$\pm I_O$	DC output source or sink current - standard outputs		25	mA	for -0.5 V $< V_O < V_{CC} + 0.5$ V
$\pm I_{CC}$; $\pm I_{GND}$	DC V_{CC} or GND current for types with: - standard outputs		50	mA	
T_{stg}	storage temperature range	−65	+150	°C	
P_{tot}	power dissipation per package plastic DIL		500	mW	for temperature range: −40 to +85 °C 74HC above +60 °C: derate linearly with 8 mW/K
	plastic mini-pack (SO)		400	mW	above +60 °C: derate linearly with 6 mW/K
P_{tot}	power dissipation per package plastic DIL		500	mW	for temperature range: −40 to +125 °C 74HC above +70 °C: derate linearly with 8 mW/K
	plastic mini-pack (SO)		400	mW	above +70 °C: derate linearly with 6 mW/K

DC CHARACTERISTICS FOR 74HC

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		74HC								V_{CC} V	V_I	OTHER
		+25			−40 to +85		−40 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
V_{IH}	HIGH level input voltage	1.5 3.15 4.2	1.3 2.4 3.1		1.5 3.15 4.2		1.5 3.15 4.2		V	2.0 4.5 6.0		
V_{IL}	LOW level input voltage		0.7 1.8 2.3	0.5 1.35 1.8		0.5 1.35 1.8		0.5 1.35 1.8	V	2.0 4.5 6.0		
V_{OH}	HIGH level output voltage all outputs	1.9 4.4 5.9	2.0 4.5 6.0		1.9 4.4 5.9		1.9 4.4 5.9		V	2.0 4.5 6.0	V_{IH} or V_{IL}	$-I_O = 20\ \mu A$ $-I_O = 20\ \mu A$ $-I_O = 20\ \mu A$
V_{OH}	HIGH level output voltage standard outputs	3.98 5.48			3.84 5.34		3.7 5.2		V	4.5 6.0	V_{IH} or V_{IL}	$-I_O = 4.0$ mA $-I_O = 5.2$ mA
V_{OL}	LOW level output voltage all outputs			0.1 0.1 0.1		0.1 0.1 0.1		0.1 0.1 0.1	V	2.0 4.5 6.0	V_{IH} or V_{IL}	$I_O = 20\ \mu A$ $I_O = 20\ \mu A$ $I_O = 20\ \mu A$
V_{OL}	LOW level output voltage standard outputs			0.26 0.26		0.33 0.33		0.4 0.4	V	4.5 6.0	V_{IH} or V_{IL}	$I_O = 4.0$ mA $I_O = 5.2$ mA
$\pm I_I$	input leakage current			0.1		1.0		1.0	μA	6.0	V_{CC} or GND	
				0.5		5.0		5.0	μA	2.0 to 6.0	15 V	
I_{CC}	quiescent supply current			2.0		20.0		40.0	μA	6.0	15 V or GND	

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f = 6$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delay na to nY			85 17 14		105 21 18		130 26 22	ns	2.0 4.5 6.0	Fig. 7
t_{THL}/ t_{TLH}	output transition time			75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 7

AC WAVEFORMS

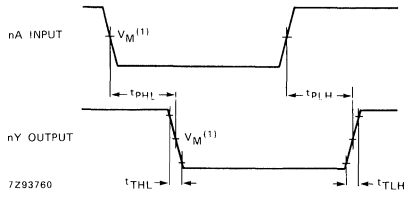


Fig. 7 Waveforms showing the input (nA) to output (nY) propagation delays and the output transition times.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

8-STAGE SHIFT-AND-STORE BUS REGISTER

FEATURES

- **Ouput capability: standard**
- **I_{CC} catagory: MSI**

GENERAL DESCRIPTION

The 74HC/HCT4094 are high-speed Si-gate CMOS devices and are pin compatible with the "4094" of the "4000B" series. They are specified in compliance with JEDEC standard no. 7.

The 74HC/HCT4094 are 8-stage serial shift registers having a storage latch associated with each stage for strobing data from the serial input (D) to the parallel buffered 3-state outputs (QP_0 to QP_7). The parallel outputs may be connected directly to common bus lines. Data is shifted on the positive-going clock (CP) transitions. The data in each shift register stage is transferred to the storage register when the strobe input (STR) is HIGH. Data in the storage register appears at the outputs whenever the output enable input (OE) signal is HIGH.

Two serial outputs (QS_1 and QS_2) are available for cascading a number of "4094" devices. Data is available at QS_1 on the positive-going clock edges to allow high-speed operation in cascaded systems in which the clock rise time is fast. The same serial information is available at QS_2 on the next negative-going clock edge and is for cascading "4094" devices when the clock rise time is slow.

APPLICATIONS

- **Serial-to-parallel data conversion**
- **Remote control holding register**

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay CP to QS_1 CP to QS_2 CP to QP_n STR to QP_n	C_L = 15 pF V_{CC} = 5 V	 15 13 19 18	 19 18 21 20	 ns ns ns ns
f_{max}	maximum clock frequency		60	60	MHz
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per package	notes 1 and 2	83	92	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT4094P: 16-lead DIL; plastic (SOT-38Z).
PC74HC/HCT4094T: 16-lead mini-pack; plastic (SO-16; SOT-109A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	STR	strobe input
2	D	serial input
3	CP	clock input
4, 5, 6, 7, 14, 13, 12, 11	QP_0 to QP_7	parallel outputs
8	GND	ground (0 V)
9, 10	QS_1, QS_2	serial outputs
15	OE	output enable input
16	V_{CC}	positive supply voltage

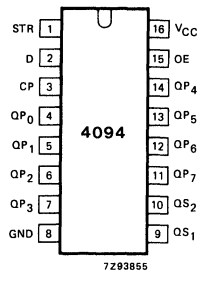


Fig. 1 Pin configuration.

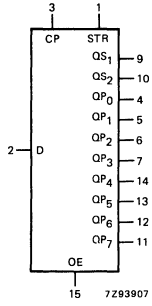


Fig. 2 Logic symbol.

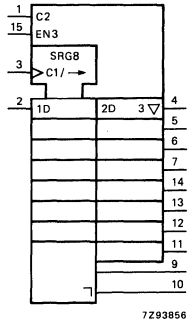


Fig. 3 IEC logic symbol.

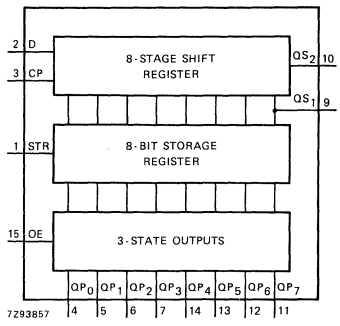


Fig. 4 Functional diagram.

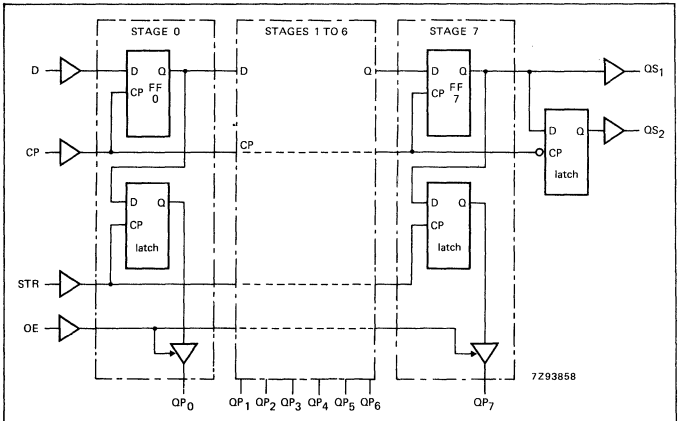


Fig. 5 Logic diagram.

FUNCTION TABLE

INPUTS				PARALLEL OUTPUTS		SERIAL OUTPUTS	
CP	OE	STR	D	QP_0	QP_n	QS_1	QS_2
↑	L	X	X	Z	Z	Q'_6	NC
↓	L	X	X	Z	Z	NC	QP_7
↑	H	L	X	NC	NC	Q'_6	NC
↑	H	H	L	L	QP_{n-1}	Q'_6	NC
↑	H	H	H	H	QP_{n-1}	Q'_6	NC
↓	H	H	H	NC	NC	NC	QP_7

H = HIGH voltage level
L = LOW voltage level
X = don't care
Z = high impedance OFF-state
NC = no change
↑ = LOW-to-HIGH CP transition
↓ = HIGH-to-LOW CP transition
Q'_6 = the information in the seventh register stage is transferred to the 8th register stage and QS_n output at the positive clock edge

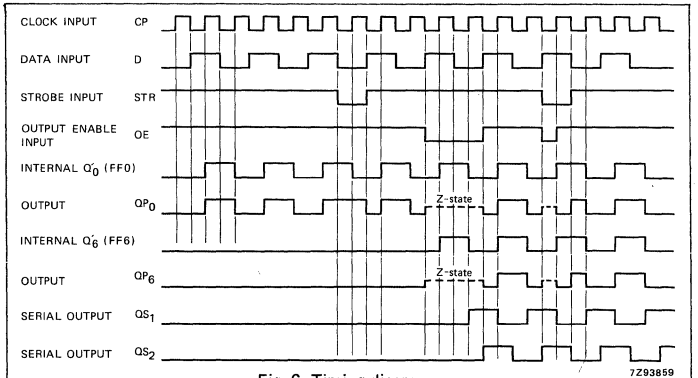


Fig. 6 Timing diagram.

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC									
		+25			–40 to +85		–40 to +125			V_{CC} V	WAVEFORMS
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay CP to QS_1			180 36 31		225 45 38		270 54 46	ns	2.0 4.5 6.0	Fig. 7
t_{PHL}/t_{PLH}	propagation delay CP to QS_2			160 32 27		200 40 34		240 48 41	ns	2.0 4.5 6.0	Fig. 7
t_{PHL}/t_{PLH}	propagation delay CP to QP_n			230 46 39		290 58 49		345 69 59	ns	2.0 4.5 6.0	Fig. 7
t_{PHL}/t_{PLH}	propagation delay STR to QP_n			210 42 36		265 53 45		315 63 54	ns	2.0 4.5 6.0	Fig. 8
t_{THL}/t_{TLH}	output transition time			75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 7
t_{PZH}/t_{PZL}	3-state output enable time OE to QP_n			175 35 30		220 44 37		265 53 45	ns	2.0 4.5 6.0	Fig. 9
t_{PHZ}/t_{PLZ}	3-state output disable time OE to QP_n			150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 9
t_W	clock pulse width HIGH or LOW	80 16 14			100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 7
t_W	strobe pulse width HIGH or LOW	80 16 14			100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 8
t_{su}	set-up time D to CP	60 12 10			75 15 13		90 18 15		ns	2.0 4.5 6.0	Fig. 10
t_h	hold time D to CP	5 5 5			5 5 5		5 5 5		ns	2.0 4.5 6.0	Fig. 10
f_{max}	maximum clock pulse frequency	6 30 35			5 24 28		4 20 24		MHz	2.0 4.5 6.0	Fig. 7

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
OE, CP	1.50
D	0.40
STR	1.00

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay CP to QS_1			45		56		68	ns	4.5	Fig. 7
t_{PHL}/t_{PLH}	propagation delay CP to QS_2			42		53		63	ns	4.5	Fig. 7
t_{PHL}/t_{PLH}	propagation delay CP to QP_n			50		63		75	ns	4.5	Fig. 7
t_{PHL}/t_{PLH}	propagation delay STR to QP_n			48		60		72	ns	4.5	Fig. 8
t_{THL}/t_{TLH}	output transition time			15		19		22	ns	4.5	Fig. 7
t_{PZH}/t_{PZL}	3-state output enable time OE to QP_n			35		44		53	ns	4.5	Fig. 9
t_{PHZ}/t_{PLZ}	3-state output disable time OE to QP_n			35		44		53	ns	4.5	Fig. 9
t_W	clock pulse width HIGH or LOW	16			20		24		ns	4.5	Fig. 7
t_W	strobe pulse width HIGH or LOW	16			20		24		ns	4.5	Fig. 8
t_{su}	set-up time D to CP	12			15		18		ns	4.5	Fig. 10
t_h	hold time D to CP	5			5		5		ns	4.5	Fig. 10
f_{max}	maximum clock pulse frequency	30			24		20		MHz	4.5	Fig. 7

AC WAVEFORMS

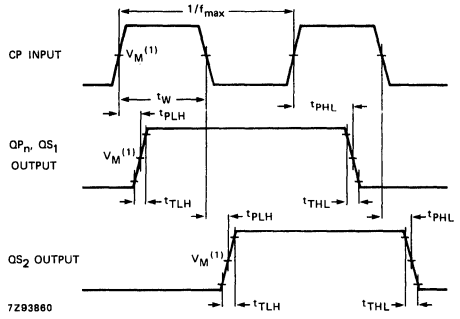


Fig. 7 Waveforms showing the clock (CP) to output (QP_n, QS_1, QS_2) propagation delays, the clock pulse width and the maximum clock frequency.

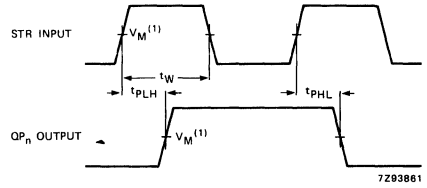


Fig. 8 Waveforms showing the strobe (STR) to output (QP_n) propagation delays and the strobe pulse width.

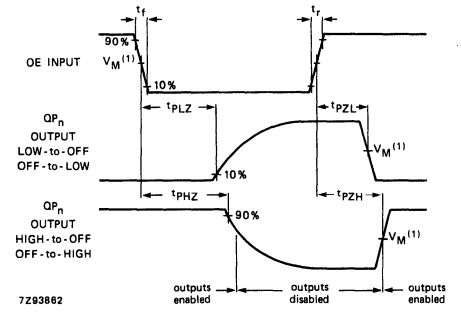


Fig. 9 Waveforms showing the 3-state enable and disable times for input OE.

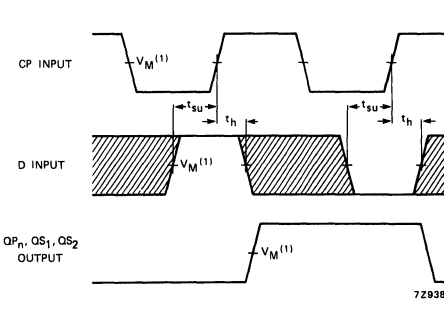


Fig. 10 Waveforms showing the data set-up and hold times for the data input (D).

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

Note to Fig. 10

The shaded areas indicate when the input is permitted to change for predictable output performance.

BCD TO 7-SEGMENT LATCH/DECODER/DRIVER

FEATURES

- **Latch storage of BCD inputs**
- **Blanking input**
- **Lamp test input**
- **Driving common cathode LED displays**
- **Guaranteed 10 mA drive capability per output**
- **Output capability: non-standard**
- **I_{CC} category: MSI**

GENERAL DESCRIPTION

The 74HC/HCT4511 are high-speed Si-gate CMOS devices and are pin compatible with "4511" of the "4000B" series. They are specified in compliance with JEDEC standard no. 7.

The 74HC/HCT4511 are BCD to 7-segment latch/decoder/drivers with four address inputs (D_1 to D_4), an active LOW latch enable input ($\overline{LE}$), an active LOW ripple blanking input ($\overline{BI}$), an active LOW lamp test input ($\overline{LT}$), and seven active HIGH segment outputs (Q_a to Q_g).

When $\overline{LE}$ is LOW, the state of the segment outputs (Q_a to Q_g) is determined by the data on D_1 to D_4.
When $\overline{LE}$ goes HIGH, the last data present on D_1 to D_4 are stored in the latches and the segment outputs remain stable.
When $\overline{LT}$ is LOW, all the segment outputs are HIGH independent of all other input conditions. With $\overline{LT}$ HIGH, a LOW on $\overline{BI}$ forces all segment outputs LOW. The inputs $\overline{LT}$ and $\overline{BI}$ do not affect the latch circuit.

APPLICATIONS

- **Driving LED displays**
- **Driving incandescent displays**
- **Driving fluorescent displays**
- **Driving LCD displays**
- **Driving gas discharge displays**

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay D_n to Q_n $\overline{LE}$ to Q_n $\overline{BI}$ to Q_n $\overline{LT}$ to Q_n	C_L = 15 pF V_{CC} = 5 V	 26 23 18 12	 26 24 19 13	 ns ns ns ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per latch	notes 1 and 2	63	64	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT4511P: 16-lead DIL; plastic (SOT-38Z).
PC74HC/HCT4511T: 16-lead mini-pack; plastic (SO-16; SOT-109A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
3	$\overline{LT}$	lamp test input (active LOW)
4	$\overline{BI}$	ripple blanking input (active LOW)
5	$\overline{LE}$	latch enable input (active LOW)
7, 1, 2, 6	D_1 to D_4	BCD address inputs
8	GND	ground (0 V)
13, 12, 11, 10, 9, 15, 14	Q_a to Q_g	segments outputs
16	V_{CC}	positive supply voltage

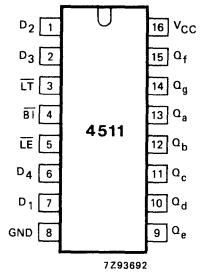


Fig. 1 Pin configuration.

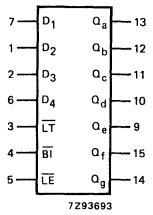


Fig. 2 Logic symbol.

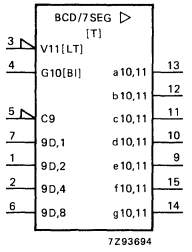


Fig. 3 IEC logic symbol.

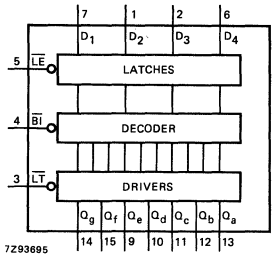


Fig. 4 Functional diagram.

FUNCTION TABLE

INPUTS							OUTPUTS							DISPLAY
$\overline{LE}$	$\overline{BI}$	$\overline{LT}$	D_4	D_3	D_2	D_1	Q_a	Q_b	Q_c	Q_d	Q_e	Q_f	Q_g	
X	X	L	X	X	X	X	H	H	H	H	H	H	H	8
X	L	H	X	X	X	X	L	L	L	L	L	L	L	blank
L	H	H	L	L	L	L	H	H	H	H	H	H	L	0
L	H	H	L	L	L	H	L	H	H	L	L	L	L	1
L	H	H	L	L	H	L	H	H	L	H	H	L	H	2
L	H	H	L	L	H	H	H	H	H	H	L	L	H	3
L	H	H	L	H	L	L	L	H	H	L	L	H	H	4
L	H	H	L	H	L	H	H	L	H	H	L	H	H	5
L	H	H	L	H	H	L	L	L	H	H	H	H	H	6
L	H	H	L	H	H	H	H	H	H	L	L	L	L	7
L	H	H	H	L	L	L	H	H	H	H	H	H	H	8
L	H	H	H	L	L	H	H	H	H	L	L	H	H	9
L	H	H	H	L	H	L	L	L	L	L	L	L	L	blank
L	H	H	H	L	H	H	L	L	L	L	L	L	L	blank
L	H	H	H	H	L	L	L	L	L	L	L	L	L	blank
L	H	H	H	H	L	H	L	L	L	L	L	L	L	blank
L	H	H	H	H	H	L	L	L	L	L	L	L	L	blank
L	H	H	H	H	H	H	L	L	L	L	L	L	L	blank
H	H	H	X	X	X	X	*							*

* Depends upon the BCD-code applied during the LOW-to-HIGH transition of $\overline{LE}$.

H = HIGH voltage level
L = LOW voltage level
X = don't care

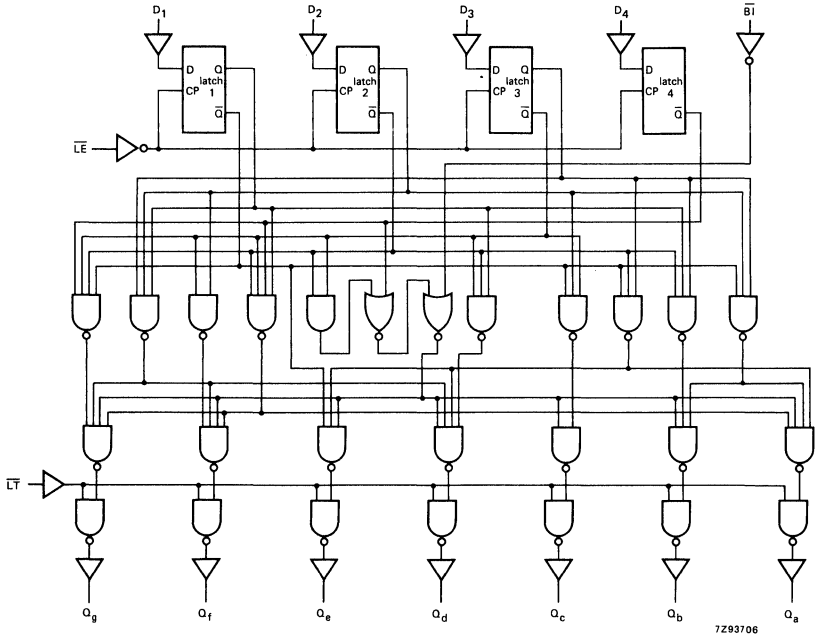


Fig. 5 Logic diagram.

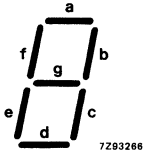


Fig. 6 Segment designation.

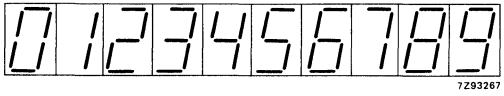


Fig. 7 Display.

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard, excepting V_{OH} which is given below
I_{CC} category: MSI

Non-standard DC characteristics for 74HC

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		74HC										
		+25			−40 to +85		−40 to +125			V_{CC} V	V_I	$-I_O$ mA
		min.	typ.	max.	min.	max.	min.	max.				
V_{OH}	HIGH level output voltage	3.98 3.60			3.84 3.35		3.70 3.10		V	4.5	V_{IH} or V_{IL}	7.5 10.0
V_{OH}	HIGH level output voltage	5.60 5.48 4.80			5.45 5.34 4.50		5.35 5.20 4.20		V	6.0	V_{IH} or V_{IL}	7.5 10.0 15.0

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC									
		+25			−40 to +85		−40 to +125			V_{CC} V	WAVEFORMS
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delay D_n to Q_n			300 60 51		375 75 64		450 90 77	ns	2.0 4.5 6.0	Fig. 8
t_{PHL}/ t_{PLH}	propagation delay $\overline{LE}$ to Q_n			270 54 46		330 68 58		405 81 69	ns	2.0 4.5 6.0	Fig. 9
t_{PHL}/ t_{PLH}	propagation delay $\overline{BT}$ to Q_n			220 44 37		275 55 47		330 66 56	ns	2.0 4.5 6.0	Fig. 10
t_{PHL}/ t_{PLH}	propagation delay $\overline{LT}$ to Q_n			150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 8
t_{THL}/ t_{TLH}	output transition time			75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Figs 8, 9 and 10
t_W	latch enable pulse width LOW	80 16 14			100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 9
t_{su}	set-up time D_n to $\overline{LE}$	60 12 10			75 15 13		90 18 15		ns	2.0 4.5 6.0	Fig. 11
t_h	hold time D_n to $\overline{LE}$	0 0 0			0 0 0		0 0 0		ns	2.0 4.5 6.0	Fig. 11

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard, excepting V_{OH} which is given below
I_{CC} category: MSI

Non-standard DC characteristics for 74HCT

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		74HCT										
		+25			−40 to +85		−40 to +125			V_{CC} V	V_I	$-I_O$ mA
		min.	typ.	max.	min.	max.	min.	max.				
V_{OH}	HIGH level output voltage	3.98 3.60			3.84 3.35		3.70 3.10		V	4.5	V_{IH} or V_{IL}	7.5 10.0

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications.
To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
$\overline{LT}$, $\overline{LE}$	1.50
$\overline{BI}$, D_n	0.30

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT									
		+25			−40 to +85		−40 to +125			V_{CC} V	WAVEFORMS
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delay D_n to Q_n			60		75		90	ns	4.5	Fig. 8
t_{PHL}/ t_{PLH}	propagation delay $\overline{LE}$ to Q_n			54		68		81	ns	4.5	Fig. 9
t_{PHL}/ t_{PLH}	propagation delay $\overline{BI}$ to Q_n			44		55		66	ns	4.5	Fig. 10
t_{PHL}/ t_{PLH}	propagation delay $\overline{LT}$ to Q_n			30		38		45	ns	4.5	Fig. 8
t_{THL}/ t_{TLH}	output transition time			15		19		22	ns	4.5	Figs 8, 9 and 10
t_W	latch enable pulse width LOW	16			20		24		ns	4.5	Fig. 9
t_{su}	set-up time D_n to $\overline{LE}$	12			15		18		ns	4.5	Fig. 11
t_h	hold time D_n to $\overline{LE}$	0			0		0		ns	4.5	Fig. 11

AC WAVEFORMS

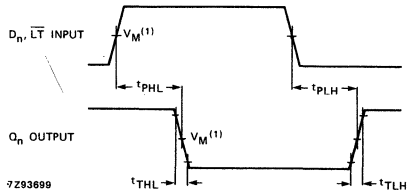


Fig. 8 Waveforms showing the input (D_n, $\overline{LT}$) to output (Q_n) propagation delays and the output transition times.

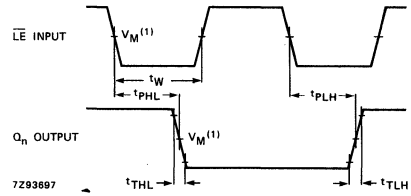


Fig. 9 Waveforms showing the input ($\overline{LE}$) to output (Q_n) propagation delays and the latch enable pulse width.

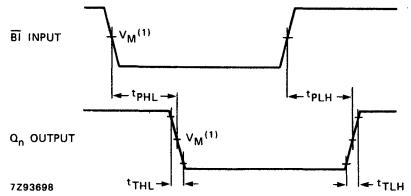


Fig. 10 Waveforms showing the input ($\overline{BI}$) to output (Q_n) propagation delays.

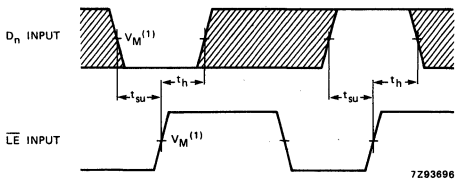


Fig. 11 Waveforms showing the data set-up and hold times for D_n input to $\overline{LE}$ input.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

Note to Fig. 11

The shaded areas indicate when the input is permitted to change for predictable output performance.

APPLICATION DIAGRAMS

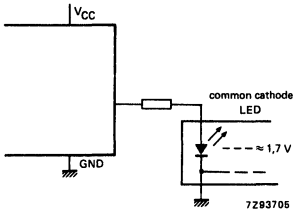


Fig. 12 Connection to common cathode LED display readout.

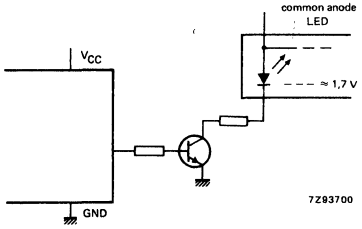
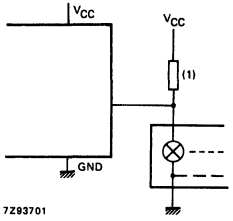


Fig. 13 Connection to common anode LED display readout.



(1) A filament pre-warm resistor to reduce thermal shock and to increase effective cold resistance of the filament is recommended.

Fig. 14 Connection to incandescent display readout.

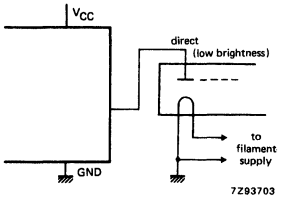


Fig. 15 Connection to fluorescent display readout.

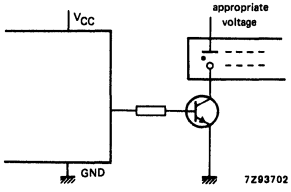


Fig. 16 Connection to gas discharge display readout.

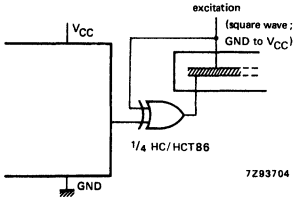


Fig. 17 Connection to LCD display readout. (Direct DC drive is not recommended as it can shorten the life of LCD displays).

DUAL SYNCHRONOUS BCD COUNTER

FEATURES

- **Output capability: standard**
- **I_{CC} category: MSI**

GENERAL DESCRIPTION

The 74HC/HCT4518 are high-speed Si-gate CMOS devices and are pin compatible with the "4518" of the "4000B" series. They are specified in compliance with JEDEC standard no. 7.

The 74HC/HCT4518 are dual 4-bit internally synchronous BCD counters with an active HIGH clock input (nCP_0) and an active LOW clock input ($n\overline{CP}_1$), buffered outputs from all four bit positions (nQ_0 to nQ_3) and an active HIGH overriding asynchronous master reset input (nMR).

The counter advances on either the LOW-to-HIGH transition of nCP_0 if $n\overline{CP}_1$ is HIGH or the HIGH-to-LOW transition of $n\overline{CP}_1$ if nCP_0 is LOW. Either nCP_0 or $n\overline{CP}_1$ may be used as the clock input to the counter and the other clock input may be used as a clock enable input. A HIGH on nMR resets the counter (nQ_0 to nQ_3 = LOW) independent of nCP_0 and $n\overline{CP}_1$.

APPLICATIONS

- **Multistage synchronous counting**
- **Multistage asynchronous counting**
- **Frequency dividers**

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay nCP_0, $n\overline{CP}_1$ to nQ_n	C_L = 15 pF; V_{CC} = 5 V	20	23	ns
t_{PHL}	propagation delay nMR to nQ_n		13	14	ns
f_{max}	maximum clock frequency		60	52	MHz
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per counter	notes 1 and 2	27	27	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacitance in pF
   f_o = output frequency in MHz; V_{CC} = supply voltage in V
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT4518P: 16-lead DIL; plastic (SOT-38Z).
PC74HC/HCT4518T: 16-lead mini-pack, plastic (SO-16; SOT-109A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 9	$1CP_0$, $2CP_0$	clock inputs (LOW-to-HIGH, edge-triggered)
2, 10	$1\overline{CP}_1$, $2\overline{CP}_1$	clock inputs (HIGH-to-LOW, edge-triggered)
3, 4, 5, 6	$1Q_0$ to $1Q_3$	data outputs
7, 15	1MR, 2MR	asynchronous master reset inputs (active HIGH)
8	GND	ground (0 V)
11, 12, 13, 14	$2Q_0$ to $2Q_3$	data outputs
16	V_{CC}	positive supply voltage

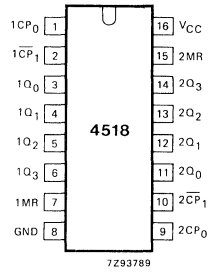


Fig. 1 Pin configuration.

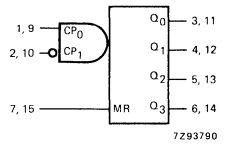


Fig. 2 Logic symbol.

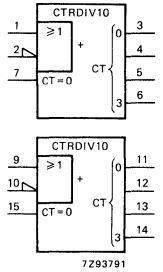


Fig. 3 IEC logic symbol.

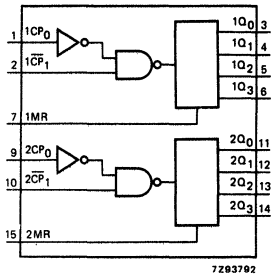


Fig. 4 Functional diagram.

FUNCTION TABLE

nCP_0	$n\overline{CP}_1$	MR	MODE
↑	H	L	counter advances
L	↓	L	counter advances
↓	X	L	no change
X	↑	L	no change
↑	L	L	no change
H	↓	L	no change
X	X	H	Q_0 to Q_3 = LOW

H = HIGH voltage level
L = LOW voltage level
X = don't care
↑ = LOW-to-HIGH clock transition
↓ = HIGH-to-LOW clock transition

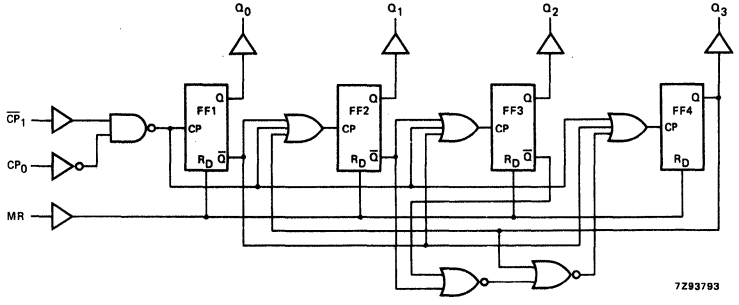


Fig. 5 Logic diagram (one counter).

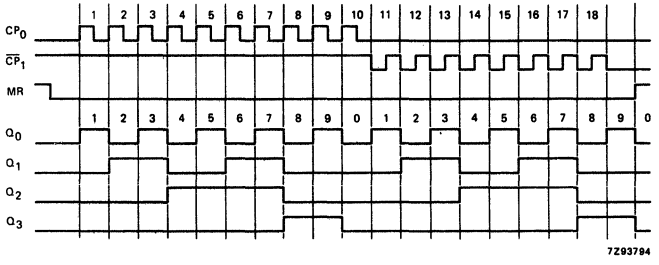


Fig. 6 Timing diagram.

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delay nCP_0, $n\overline{CP}_1$ to nQ_n			240 48 41		300 60 51		360 72 61	ns	2.0 4.5 6.0	Fig. 9
t_{PHL}/ t_{PLH}	propagation delay nMR to nQ_n			150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 8
t_{THL}/ t_{TLH}	output transition time			75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 9
t_W	clock pulse width HIGH or LOW	80 16 14			100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 8
t_W	master reset pulse width HIGH	120 24 20			150 30 26		180 36 31		ns	2.0 4.5 6.0	Fig. 8
t_{rem}	removal time nMR to nCP_0, $n\overline{CP}_1$	0 0 0			0 0 0		0 0 0		ns	2.0 4.5 6.0	Fig. 8
t_{su}	set-up time $n\overline{CP}_1$ to nCP_0; nCP_0 to $n\overline{CP}_1$	80 16 14			100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 7
f_{max}	maximum clock pulse frequency nCP_0, $n\overline{CP}_1$	6 30 35			5 24 28		4 20 24		MHz	2.0 4.5 6.0	Fig. 8

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
nCP_0, $n\overline{CP}_1$	0.30
nMR	1.50

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay nCP_0, $n\overline{CP}_1$ to nQ_n			53		66		80	ns	4.5	Fig. 9
t_{PHL}	propagation delay nMR to nQ_n			35		44		53	ns	4.5	Fig. 8
t_{THL}/t_{TLH}	output transition time			15		19		22	ns	4.5	Fig. 9
t_W	clock pulse width HIGH or LOW	20			25		30		ns	4.5	Fig. 8
t_W	master reset pulse width HIGH	20			25		30		ns	4.5	Fig. 8
t_{rem}	removal time nMR to nCP_0, $n\overline{CP}_1$	0			0		0		ns	4.5	Fig. 8
t_{su}	set-up time $n\overline{CP}_1$ to nCP_0; nCP_0 to $n\overline{CP}_1$	16			20		24		ns	4.5	Fig. 7
f_{max}	maximum clock pulse frequency nCP_0, $n\overline{CP}_1$	25			20		17		MHz	4.5	Fig. 8

AC WAVEFORMS

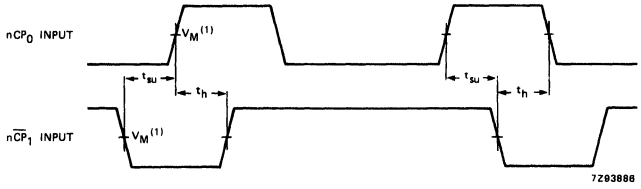


Fig. 7 Waveforms showing hold and set-up times for nCP_0 to $n\overline{CP}_1$ and $n\overline{CP}_1$ to nCP_0.

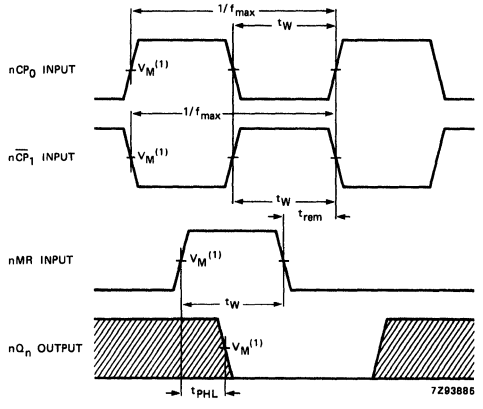


Fig. 8 Waveforms showing the minimum pulse widths for nCP_0, $n\overline{CP}_1$ and nMR inputs; the removal time for nMR and the propagation delay for nMR to nQ_n outputs.

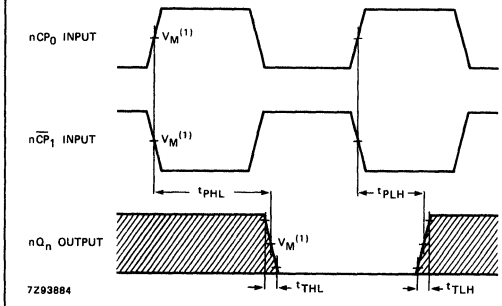


Fig. 9 Waveforms showing the propagation delays for nCP_0, $n\overline{CP}_1$ to nQ_n outputs and the output transition times.

Note to Fig. 8 and Fig. 9

Conditions:

$n\overline{CP}_1$ =HIGH while nCP_0 is triggered on a LOW-to-HIGH transition and nCP_0 = LOW , while $n\overline{CP}_1$ is triggered on a HIGH-to-LOW transition.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

DUAL 4-BIT SYNCHRONOUS BINARY COUNTER

FEATURES

- **Output capability: standard**
- **I_{CC} category: MSI**

GENERAL DESCRIPTION

The 74HC/HCT4520 are high-speed Si-gate CMOS devices and are pin compatible with the "4520" of the "4000B" series. They are specified in compliance with JEDEC standard no. 7.

The 74HC/HCT4520 are dual 4-bit internally synchronous binary counters with an active HIGH clock input (nCP_0) and an active LOW clock input ($n\overline{CP}_1$), buffered outputs from all four bit positions (nQ_0 to nQ_3) and an active HIGH overriding asynchronous master reset input (nMR).

The counter advances on either the LOW-to-HIGH transition of nCP_0 if $n\overline{CP}_1$ is HIGH or the HIGH-to-LOW transition of $n\overline{CP}_1$ if nCP_0 is LOW. Either nCP_0 or $n\overline{CP}_1$ may be used as the clock input to the counter and the other clock input may be used as a clock enable input. A HIGH on nMR resets the counter (nQ_0 to nQ_3 = LOW) independent of nCP_0 and $n\overline{CP}_1$.

APPLICATIONS

- **Multistage synchronous counting**
- **Multistage asynchronous counting**
- **Frequency dividers**

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay nCP_0, $n\overline{CP}_1$ to nQ_n	C_L = 15 pF; V_{CC} = 5 V	23	25	ns
t_{PHL}	propagation delay nMR to nQ_n		13	14	ns
f_{max}	maximum clock frequency		65	52	MHz
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per counter	notes 1 and 2	29	29	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacitance in pF
   f_o = output frequency in MHz; V_{CC} = supply voltage in V
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT4520P: 16-lead DIL; plastic (SOT-38Z).
PC74HC/HCT4520T: 16-lead mini-pack; plastic (SO-16; SOT-109A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 9	$1CP_0$, $2CP_0$	clock inputs (LOW-to-HIGH, edge-triggered)
2, 10	$1\overline{CP}_1$, $2\overline{CP}_1$	clock inputs (HIGH-to-LOW, edge-triggered)
3, 4, 5, 6	$1Q_0$ to $1Q_3$	data outputs
7, 15	1MR, 2MR	asynchronous master reset inputs (active HIGH)
8	GND	ground (0 V)
11, 12, 13, 14	$2Q_0$ to $2Q_3$	data outputs
16	V_{CC}	positive supply voltage

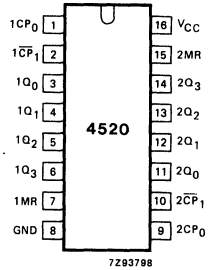


Fig. 1 Pin configuration.

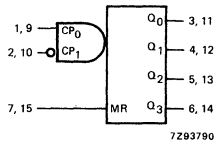


Fig 2 Logic symbol.

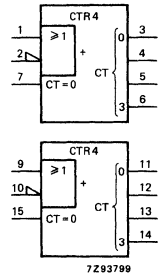


Fig. 3 IEC logic symbol.

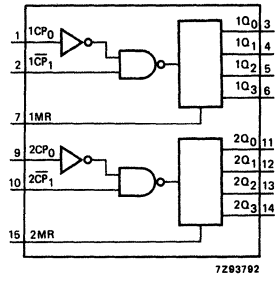


Fig. 4 Functional diagram.

FUNCTION TABLE

nCP_0	$n\overline{CP}_1$	MR	MODE
↑	H	L	counter advances
L	↓	L	counter advances
↓	X	L	no change
X	↑	L	no change
↑	L	L	no change
H	↓	L	no change
X	X	H	Q_0 to Q_3 = LOW

H = HIGH voltage level
L = LOW voltage level
X = don't care
↑ = LOW-to-HIGH clock transition
↓ = HIGH-to-LOW clock transition

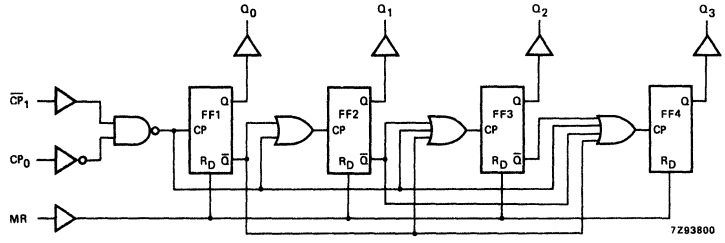


Fig. 5 Logic diagram (one counter).

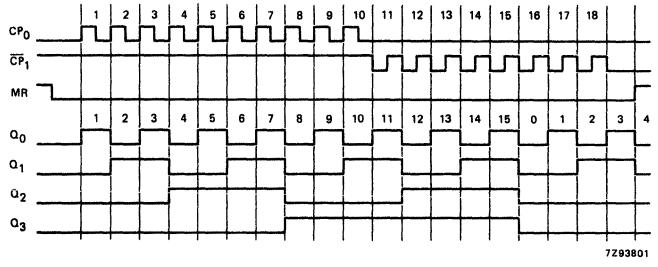


Fig. 6 Timing diagram.

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay nCP_0 to nQ_n			240 48 41		300 60 51		360 72 61	ns	2.0 4.5 6.0	Fig. 8
t_{PHL}/t_{PLH}	propagation delay $n\overline{CP}_1$ to nQ_n			240 48 41		300 60 51		360 72 61	ns	2.0 4.5 6.0	Fig. 8
t_{PHL}	propagation delay nMR to nQ_n			150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 9
t_{THL}/t_{TLH}	output transition time			75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 8
t_W	clock pulse width HIGH or LOW	80 16 14			100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 7
t_W	master reset pulse width HIGH	120 24 20			150 30 26		180 36 31		ns	2.0 4.5 6.0	Fig. 7
t_{rem}	removal time nMR to nCP_0, $n\overline{CP}_1$	0 0 0			0 0 0		0 0 0		ns	2.0 4.5 6.0	Fig. 7
t_{su}	set-up time $n\overline{CP}_1$ to nCP_0, nCP_0 to $n\overline{CP}_1$	80 16 14			100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 8
f_{max}	maximum clock pulse frequency	6 30 35			5 24 28		4 20 24		MHz	2.0 4.5 6.0	Fig. 7

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
nCP_0, $n\overline{CP}_1$	0.30
nMR	1.50

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay nCP_0 to nQ_n			53		66		80	ns	4.5	Fig. 8
t_{PHL}/t_{PLH}	propagation delay $n\overline{CP}_1$ to nQ_n			53		66		80	ns	4.5	Fig. 8
t_{PHL}	propagation delay nMR to nQ_n			35		44		53	ns	4.5	Fig. 9
t_{THL}/t_{TLH}	output transition time			15		19		22	ns	4.5	Fig. 8
t_W	clock pulse width HIGH or LOW	20			25		30		ns	4.5	Fig. 7
t_W	master reset pulse width HIGH	20			25		30		ns	4.5	Fig. 7
t_{rem}	removal time nMR to nCP_0, $n\overline{CP}_1$	0			0		0		ns	4.5	Fig. 7
t_{su}	set-up time $n\overline{CP}_1$ to nCP_0, nCP_0 to $n\overline{CP}_1$	16			20		24		ns	4.5	Fig. 8
f_{max}	maximum clock pulse frequency	25			20		17		MHz	4.5	Fig. 7

AC WAVEFORMS

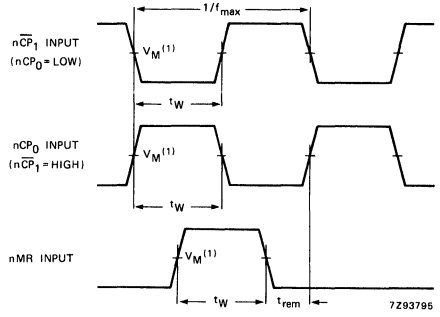


Fig. 7 Waveforms showing removal time for nMR; minimum nCP_0, $n\overline{CP}_1$, nMR pulse widths and maximum clock pulse frequency.

Conditions:

$n\overline{CP}_1$ = HIGH while nCP_0 is triggered on a LOW-to-HIGH transition; t_W and t_{rem} also apply when nCP_0 = LOW and $n\overline{CP}_1$ is triggered on a HIGH-to-LOW transition.

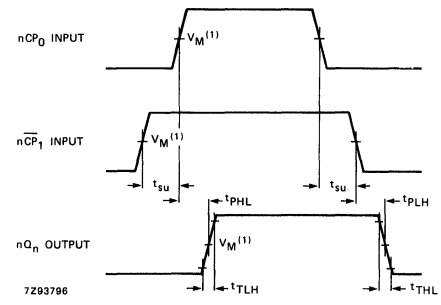


Fig. 8 Waveforms showing set-up times for nCP_0 to $n\overline{CP}_1$ and $n\overline{CP}_1$ to nCP_0, propagation delays and output transition times.

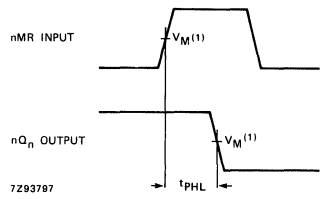


Fig. 9 Waveforms showing propagation delay from nMR to nQ_n output.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

8-BIT SYNCHRONOUS BINARY DOWN COUNTER

FEATURES

- **Cascadable**
- **Synchronous or asynchronous preset**
- **Output capability: standard**
- **I_{CC} category: MSI**

GENERAL DESCRIPTION

The 74HC/HCT40103 are high-speed Si-gate CMOS devices and are pin compatible with the "40103" of the "4000B" series. They are specified in compliance with JEDEC standard no. 7.

The 74HC/HCT40103 consist each of an 8-bit synchronous down counter with a single output which is active when the internal count is zero. The "40103" contains a single 8-bit binary counter and has control inputs for enabling or disabling the clock (CP), for clearing the counter to its maximum count, and for presetting the counter either synchronously or asynchronously. All control inputs and the terminal count output ($\overline{TC}$) are active-LOW logic.

In normal operation, the counter is decremented by one count on each positive-going transition of the clock (CP). Counting is inhibited when the terminal enable input ($\overline{TE}$) is HIGH. The terminal count output ($\overline{TC}$) goes LOW when the count reaches zero if $\overline{TE}$ is LOW, and remains LOW for one full clock period.

When the synchronous preset enable input ($\overline{PE}$) is LOW, data at the jam input (P_0 to P_7) is clocked into the counter on the next positive-going clock transition regardless of the state of $\overline{TE}$.
When the asynchronous preset enable input ($\overline{PL}$) is LOW, data at the jam input (P_0 to P_7) is asynchronously forced into the counter regardless of the state of $\overline{PE}$, $\overline{TE}$, or CP. The jam inputs (P_0 to P_7) represent a single 8-bit binary word.

(continued on next page)

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay CP to $\overline{TC}$	C_L = 15 pF; V_{CC} = 5 V	30	30	ns
f_{max}	maximum clock frequency		32	30	MHz
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per counter	notes 1 and 2	25	27	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT40103P: 16-lead DIL; plastic (SOT-38Z).
PC74HC/HCT40103T: 16-lead mini-pack; plastic (SO-16; SOT-109A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	CP	clock input (LOW-to-HIGH, edge-triggered)
2	$\overline{MR}$	asynchronous master reset input (active LOW)
3	$\overline{TE}$	terminal enable input
4, 5, 6, 7, 10, 11, 12, 13	P_0 to P_7	jam inputs
8	GND	ground (0 V)
9	$\overline{PL}$	asynchronous preset enable input (active LOW)
14	$\overline{TC}$	terminal count output (active LOW)
15	$\overline{PE}$	synchronous preset enable input (active LOW)
16	V_{CC}	positive supply voltage

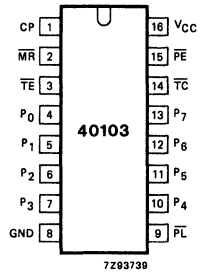


Fig. 1 Pin configuration.

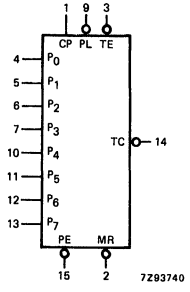


Fig. 2 Logic symbol.

IN PROGRESS

Fig. 3 IEC logic symbol.

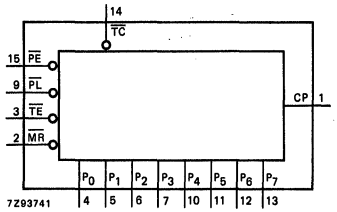


Fig. 4 Functional diagram.

FUNCTION TABLE

CONTROL INPUTS				PRESET MODE	ACTION
$\overline{MR}$	$\overline{PL}$	$\overline{PE}$	$\overline{TE}$		
H	H	H	H	synchronous	inhibit counter
H	H	H	L		count down
H	H	L	X		preset on next LOW-to HIGH clock transition
H	L	X	X	asynchronous	preset asynchronously
L	X	X	X		clear to maximum count

Notes to function table

1. Clock connected to CP.
2. Synchronous operation: changes occur on the LOW-to-HIGH CP transition.
3. Jam inputs: MSD = P_7, LSD = P_0.

H = HIGH voltage level
L = LOW voltage level
X = don't care

GENERAL DESCRIPTION (Cont'd)

When the master reset input ($\overline{MR}$) is LOW, the counter is asynchronously cleared to its maximum count (decimal 255) regardless of the state of any other input. The precedence relationship between control inputs is indicated in the function table.

If all control inputs except $\overline{TE}$ are HIGH at the time of zero count, the counters will jump to the maximum count, giving a counting sequence of 256 clock pulses long.
The "40103" may be cascaded using the $\overline{TE}$ input and the $\overline{TC}$ output, in either a synchronous or ripple mode.

APPLICATIONS

- **Divide-by-n counters**
- **Programmable timers**
- **Interrupt timers**
- **Cycle/program counters**

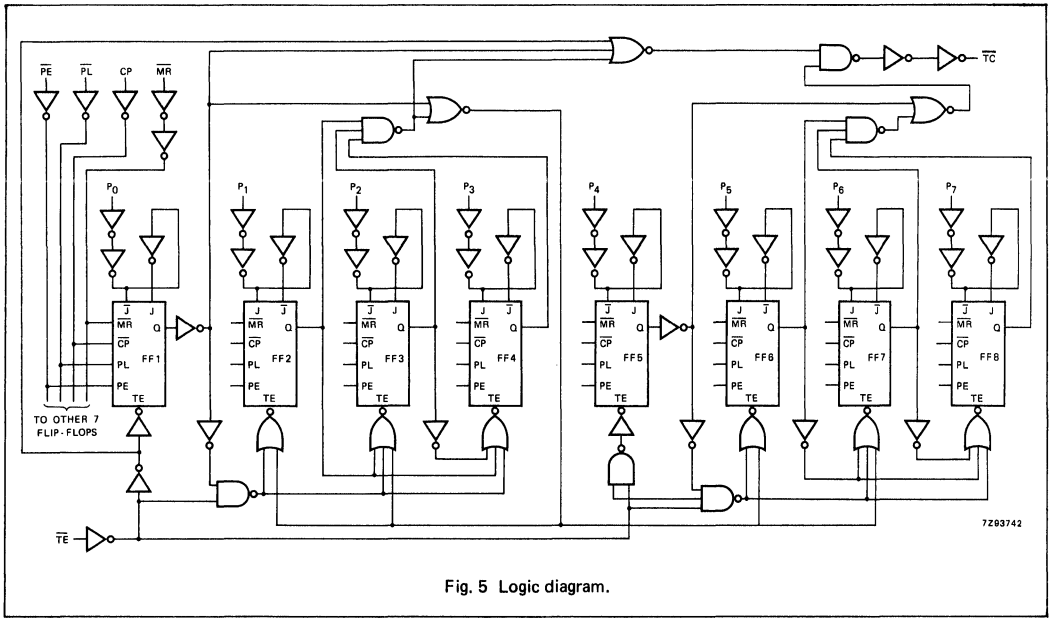


Fig. 5 Logic diagram.

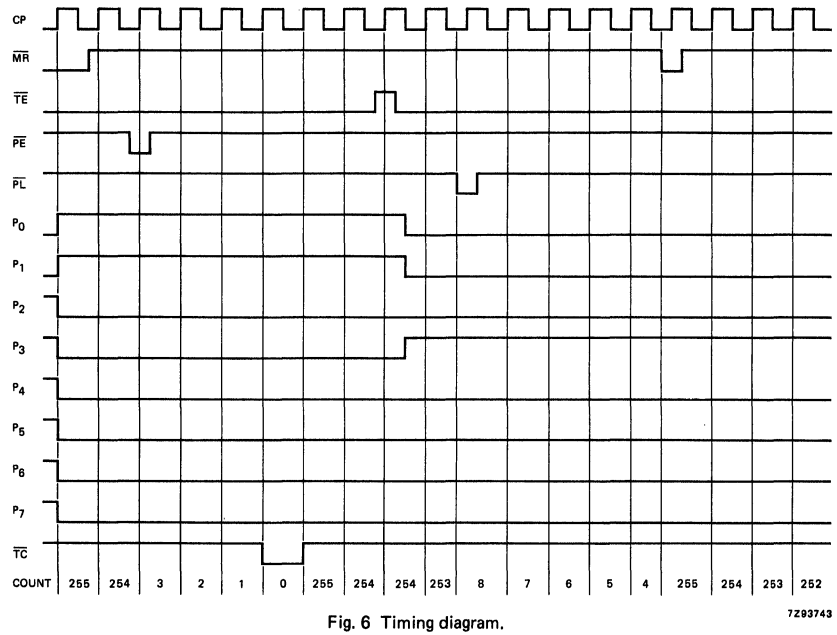


Fig. 6 Timing diagram.

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	WAVEFORMS
		+25			–40 to +85		–40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delay CP to $\overline{TC}$			300 60 51		375 75 64		450 90 77	ns	2.0 4.5 6.0	Fig. 7
t_{PHL}/ t_{PLH}	propagation delay $\overline{TE}$ to $\overline{TC}$			200 40 34		250 50 43		300 60 51	ns	2.0 4.5 6.0	Fig. 8
t_{PHL}/ t_{PLH}	propagation delay $\overline{PL}$ to $\overline{TC}$			275 55 47		345 69 59		415 83 71	ns	2.0 4.5 6.0	Fig. 9
t_{PHL}	propagation delay $\overline{MR}$ to $\overline{TC}$			275 55 47		345 69 59		415 83 71	ns	2.0 4.5 6.0	Fig. 9
t_{THL}/ t_{TLH}	output transition time			75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Figs. 7 and 8
t_W	clock pulse width HIGH or LOW	165 33 28			205 41 35		250 50 43		ns	2.0 4.5 6.0	Fig. 7
t_W	master reset pulse width LOW	150 30 26			190 38 33		225 45 38		ns	2.0 4.5 6.0	Fig. 9
t_W	preset enable pulse width $\overline{PL}$; LOW	125 25 21			155 31 26		190 38 32		ns	2.0 4.5 6.0	Fig. 9
t_{rem}	removal time $\overline{MR}$ to CP	50 10 9			65 13 11		75 15 13		ns	2.0 4.5 6.0	Fig. 10
t_{su}	set-up time $\overline{PE}$ to CP	100 20 17			125 25 21		150 30 26		ns	2.0 4.5 6.0	Fig. 11
t_{su}	set-up time $\overline{TE}$ to CP	175 35 30			220 44 37		265 53 45		ns	2.0 4.5 6.0	Fig. 11
t_{su}	set-up time P_n to CP	100 20 17			125 25 21		150 30 26		ns	2.0 4.5 6.0	Fig. 12
t_h	hold time $\overline{PE}$ to CP	0 0 0			0 0 0		0 0 0		ns	2.0 4.5 6.0	Fig. 11

AC CHARACTERISTICS FOR 74HC (Cont'd)

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC									
		+25			−40 to +85		−40 to +125			V_{CC} V	WAVEFORMS
		min.	typ.	max.	min.	max.	min.	max.			
t_h	hold time $\overline{TE}$ to CP	0 0 0			0 0 0		0 0 0		ns	2.0 4.5 6.0	Fig. 11
t_h	hold time P_n to CP	5 5 5			5 5 5		5 5 5		ns	2.0 4.5 6.0	Fig. 12
f_{max}	maximum clock pulse frequency	3 15 18			2 12 14		2 10 12		MHz	2.0 4.5 6.0	Fig. 7

DEVELOPMENT DATA

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
$\overline{CP}$, $\overline{PE}$	1.50
$\overline{MR}$	1.00
TE	0.80
P_n	0.25

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay CP to $\overline{TC}$			60		75		90	ns	4.5	Fig. 7
t_{PHL}/t_{PLH}	propagation delay $\overline{TE}$ to $\overline{TC}$			50		63		75	ns	4.5	Fig. 8
t_{PHL}/t_{PLH}	propagation delay $\overline{PL}$ to $\overline{TC}$			60		75		90	ns	4.5	Fig. 9
t_{PHL}	propagation delay $\overline{MR}$ to $\overline{TC}$			60		63		75	ns	4.5	Fig. 9
t_{THL}/t_{TLH}	output transition time			15		19		22	ns	4.5	Figs. 7 and 8
t_W	clock pulse width HIGH or LOW	35			44		53		ns	4.5	Fig. 7
t_W	master reset pulse width LOW	40			50		60		ns	4.5	Fig. 9
t_W	preset enable pulse width $\overline{PL}$; LOW	38			48		57		ns	4.5	Fig. 9
t_{rem}	removal time $\overline{MR}$ to CP	10			13		15		ns	4.5	Fig. 10
t_{su}	set-up time $\overline{PE}$ to CP	20			25		30		ns	4.5	Fig. 11
t_{su}	set-up time $\overline{TE}$ to CP	40			50		60		ns	4.5	Fig. 11
t_{su}	set-up time P_n to CP	24			30		36		ns	4.5	Fig. 12
t_h	hold time $\overline{PE}$ to CP	0			0		0		ns	4.5	Fig. 11

AC CHARACTERISTICS FOR 74HCT (Cont'd)

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_h	hold time $\overline{TE}$ to CP	0			0		0		ns	4.5	Fig. 11
t_h	hold time P_n to CP	5			5		5		ns	4.5	Fig. 12
f_{max}	maximum clock pulse frequency	14			11		9		MHz	4.5	Fig. 7

DEVELOPMENT DATA

AC WAVEFORMS

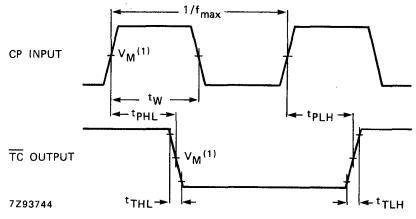


Fig. 7 Waveforms showing the clock input (CP) to $\overline{TC}$ propagation delays, the clock pulse width, the output transition times and the maximum clock pulse frequency.

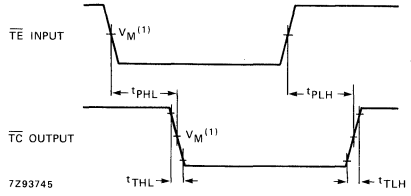


Fig. 8 Waveforms showing the $\overline{TE}$ to $\overline{TC}$ propagation delays.

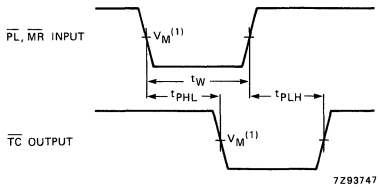


Fig. 9 Waveforms showing $\overline{PL}$, $\overline{MR}$ to $\overline{TC}$ propagation delays.

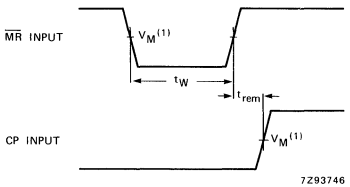


Fig. 10 Waveforms showing removal time for $\overline{MR}$.

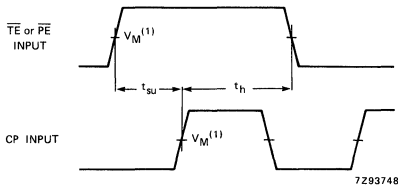


Fig. 11 Waveforms showing hold and set-up times for $\overline{MR}$ or $\overline{PE}$ to CP.

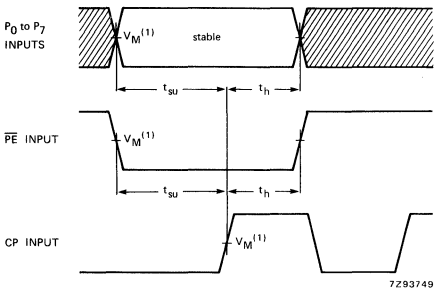


Fig. 12 Waveforms showing hold and set-up times for P_n, $\overline{PE}$ to CP.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

Note to Fig. 12

The shaded areas indicate when the input is permitted to change for predictable output performance.

4-BIT X 16-WORD FIFO REGISTER

FEATURES

- **Independent asynchronous inputs and outputs**
- **Expandable in either direction**
- **Reset capability**
- **Status indicators on inputs and outputs**
- **3-state outputs**
- **Output capability: standard**
- **I_{CC} category: MSI**

GENERAL DESCRIPTION

The 74HC/HCT40105 are high-speed Si-gate CMOS devices and are pin compatible with the "40105" of the "4000B" series. They are specified in compliance with JEDEC standard no. 7.

The 74HC/HCT40105 are first-in/first-out (FIFO) "elastic" storage registers that can store sixteen 4-bit words. The "40105" is capable of handling input and output data at different shifting rates. This feature makes it particularly useful as a buffer between asynchronous systems. Each word position in the register is clocked by a control flip-flop, which stores a marker bit. A "1" signifies that the position's data is filled and a "0" denotes a vacancy in that position. The control flip-flop detects the state of the preceding flip-flop and communicates its own status to the succeeding flip-flop. When a control flip-flop is in the "0" state and sees a "1" in the preceding flip-flop, it generates a clock pulse that transfers data from the preceding four data latches into its own four data latches and resets the preceding flip-flop to "0". The first and last control flip-flops have buffered outputs. Since all empty locations "bubble" automatically to the input end, and all valid data ripples through to the output end, the status of the first control flip-flop (data-in ready output - DIR) indicates if the FIFO is full, and the status of the last flip-flop (data-out ready output - DOR) indicates if the FIFO

(continued on next page)

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay MR to DIR, DOR	C_L = 15 pF, V_{CC} = 5 V	15	15	ns
	propagation delay $\overline{SO}$ to Q_n		35	35	ns
t_{PHL}	propagation delay SI to DIR		18	18	ns
	propagation delay $\overline{SO}$ to DOR		18	18	ns
f_{max}	maximum clock frequency		32	30	MHz
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per package	notes 1 and 2	134	145	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT40105P: 16-lead DIL; plastic (SOT-38Z).
PC74HC/HCT40105T: 16-lead mini-pack; plastic (SO-16; SOT-109A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	$\overline{OE}$	output enable input (active LOW)
2	DIR	data-in ready output
3	SI	shift-in input (LOW-to-HIGH, edge-triggered)
4, 5, 6, 7	D_0 to D_3	parallel data inputs
8	GND	ground (0 V)
9	MR	asynchronous master reset input (active HIGH)
13, 12, 11, 10	Q_0 to Q_3	3-state data outputs
14	DOR	data-out ready output
15	$\overline{SO}$	shift-out input (HIGH-to-LOW, edge-triggered)
16	V_{CC}	positive supply voltage

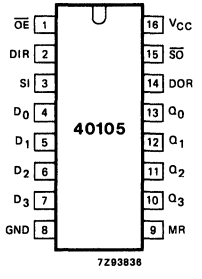


Fig. 1 Pin configuration.

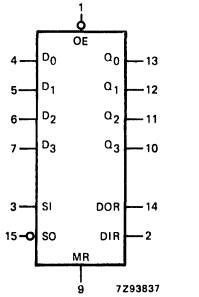


Fig. 2 Logic symbol.

IN PROGRESS

Fig. 3 IEC logic symbol.

GENERAL DESCRIPTION (Cont'd)

contains data. As the earliest data is removed from the bottom of the data stack (output end), all data entered later will automatically ripple toward the output.

Loading data

Data can be entered whenever the DIR flag is HIGH, by a LOW-to-HIGH transition on the shift-in input (SI). This input must go LOW momentarily before the next word is accepted by the FIFO. The DIR flag will go LOW momentarily, until the data has been transferred to the second location. The DIR flag remains LOW when all 16 word locations are filled with valid data, and further pulses on the SI input will be ignored until DIR goes HIGH.

Unloading data

As soon as the first word has rippled to the output, the data-out ready output (DOR) goes HIGH and data of the first word is available on the outputs.

Data of other words can be removed by a negative-going transition on the shift-out input ($\overline{SO}$). This negative-going transition causes the DOR signal to go LOW, while the next word moves to the output. As long as valid data is available in the FIFO, the DOR signal will go HIGH again signifying that the next word is ready at the output. When the FIFO is empty, DOR will remain LOW, and any further commands will be ignored until a "1" marker ripples down to the last control register and DOR goes HIGH.
If during unloading SI is LOW, data on the data input of the FIFO is entered in the first location.

Master reset

A HIGH on the master reset input (MR) sets all the control logic marker bits to "0". DOR goes LOW and DIR goes HIGH. The contents of the data register are not changed but will be superseded when the first word is loaded. Thus MR does not clear data within the register but only the control logic. If the shift-in flag (SI) is HIGH during the master reset pulse, data present at the input (D_0 to D_3) is immediately moved into the first location upon completion of the reset process.

3-state outputs

In order to facilitate data busing, 3-state outputs (Q_0 to Q_3) are provided on the data output lines, while the load condition of the register can be detected by the state of the DOR output. A HIGH on the 3-state control flag (output enable input $\overline{OE}$) forces the outputs into the high-impedance OFF-state mode.

Cascading

The "40105" can be cascaded to form longer registers simply by connecting the DIR outputs to the $\overline{SO}$ inputs and the DOR outputs to the SI inputs.
In the cascading mode, a master reset pulse must be applied after the supply voltage is turned on. For words wider than 4 bits, the DIR and DOR outputs must be gated together with AND gates. Their outputs drive the SI and $\overline{SO}$ inputs in parallel, if expansion occurs in both directions (see Figs. 6 and 7).

APPLICATIONS

- **Bit-rate smoothing**
- **CPU/terminal buffering**
- **Data communications**
- **Peripheral buffering**
- **Line printer input buffers**
- **Auto-diallers**
- **CRT buffer memories**
- **Radar data acquisition**

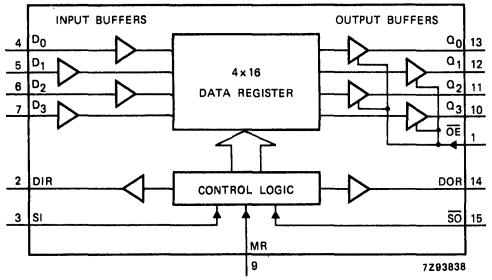


Fig. 4 Functional diagram.

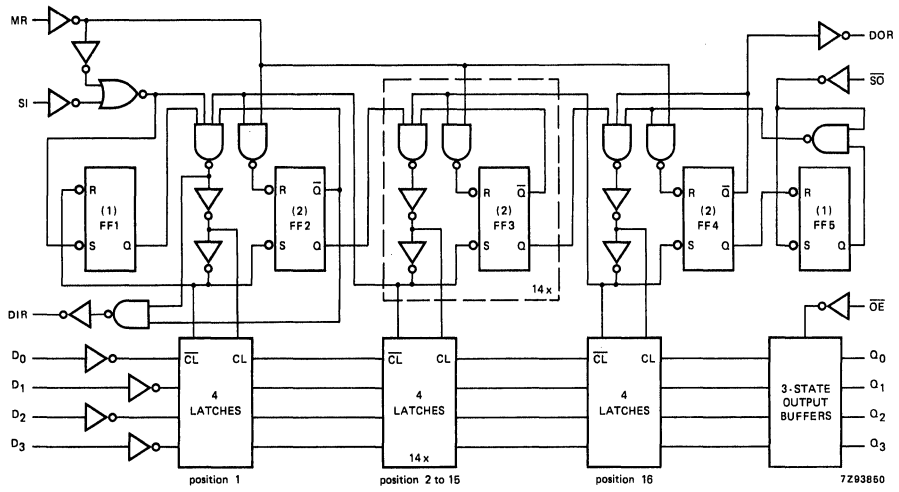


Fig. 5 Logic diagram.

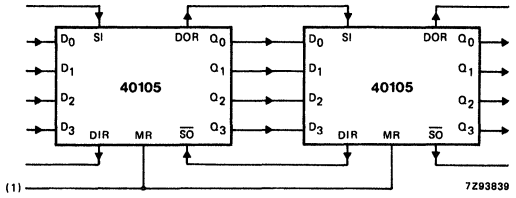
Notes to Fig. 5

(see control flip-flops)

(1) LOW on $\overline{S}$ input of FF1 and FF5 will set Q output to HIGH independent of state on $\overline{R}$ input.

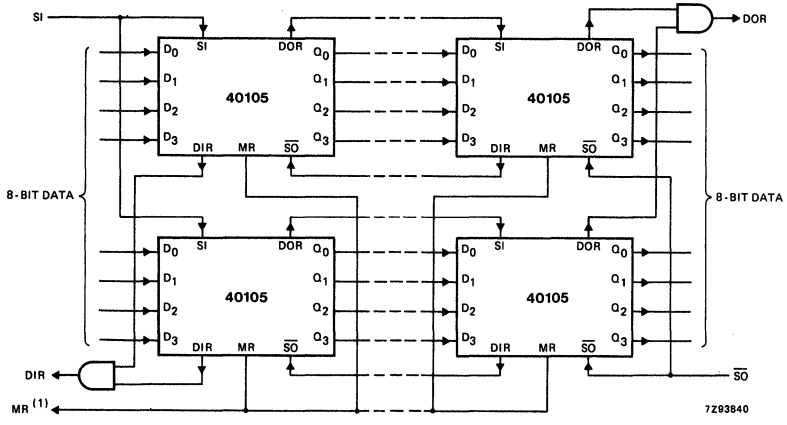
(2) LOW on $\overline{R}$ input of FF2 and FF3 will set Q output to LOW independent of state on $\overline{S}$ input.

DEVELOPMENT DATA



(1) Master reset pulse must be applied when cascading by 16 n-bits.

Fig. 6 Expansion; 4-bits wide-by-16 n-bits long.



(1) Master reset pulse must be applied when cascading by 16 n-bits.

Fig. 7 Expansion; 8-bits wide-by-16 n-bits long.

DEVELOPMENT DATA

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay MR to DIR, DOR			175 35 30		220 44 37		265 53 45	ns	2.0 4.5 6.0	Fig. 8
t_{PHL}	propagation delay SI to DIR			210 42 36		265 53 45		315 63 54	ns	2.0 4.5 6.0	Fig. 9
t_{PHL}	propagation delay $\overline{SO}$ to DOR			210 42 36		265 53 45		315 63 54	ns	2.0 4.5 6.0	Fig. 10
t_{PHL}/t_{PLH}	propagation delay $\overline{SO}$ to Q_n			400 80 68		500 100 85		600 120 102	ns	2.0 4.5 6.0	Fig. 11
t_{PLH}	propagation delay/ripple through delay SI to DOR			2000 400 340		2500 500 425		3000 600 510	ns	2.0 4.5 6.0	Fig. 12
t_{PLH}	propagation delay/ripple through delay $\overline{SO}$ to DIR			2500 500 425		3125 625 532		3750 750 638	ns	2.0 4.5 6.0	Fig. 13
t_{THL}/t_{TLH}	output transition time			75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 11
t_{PZH}/t_{PZL}	3-state output enable $\overline{OE}$ to Q_n			150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 14
t_{PHZ}/t_{PLZ}	3-state output disable time $\overline{OE}$ to Q_n			140 28 24		175 35 30		210 42 36	ns	2.0 4.5 6.0	Fig. 14
t_W	SI pulse width HIGH or LOW	80 16 14			100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 9
t_W	$\overline{SO}$ pulse width HIGH or LOW	120 24 20			150 30 26		180 36 31		ns	2.0 4.5 6.0	Fig. 10
t_W	DIR pulse width HIGH or LOW	220 44 37			275 55 47		330 66 56		ns	2.0 4.5 6.0	Fig. 9

AC CHARACTERISTICS FOR 74HC (Cont'd)

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_W	DOR pulse width HIGH or LOW	220 44 37			275 55 47		330 66 56		ns	2.0 4.5 6.0	Fig. 10
t_W	MR pulse width HIGH	80 16 14			100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 8
t_{rem}	removal time MR to SI	50 10 9			65 13 11		75 15 13		ns	2.0 4.5 6.0	Fig. 15
t_{su}	set-up time D_n to SI	−35 −7 −6			−45 −9 −7		−55 −11 −9		ns	2.0 4.5 6.0	Fig. 16
t_h	hold time D_n to SI	125 25 21			155 31 26		190 38 32		ns	2.0 4.5 6.0	Fig. 16
f_{max}	maximum pulse frequency SI, $\overline{SO}$	3 15 18			2 12 14		2 10 12		MHz	2.0 4.5 6.0	Figs 9 and 10

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications.
To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
$\overline{OE}$	0.75
SI	0.40
D_n	0.30
$\overline{MR}$	1.50
$\overline{SO}$	0.40

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay MR to DIR, DOR			36		45		54	ns	4.5	Fig. 8
t_{PHL}/t_{PLH}	propagation delay SI to DIR			42		53		63	ns	4.5	Fig. 9
t_{PHL}	propagation delay $\overline{SO}$ to DOR			42		53		63	ns	4.5	Fig. 10
t_{PHL}/t_{PLH}	propagation delay $\overline{SO}$ to Q_n			80		100		120	ns	4.5	Fig. 11
t_{PLH}	propagation delay/ripple through delay SI to DOR			400		500		600	ns	4.5	Fig. 12
t_{PLH}	propagation delay/ripple through delay $\overline{SO}$ to DIR			500		625		750	ns	4.5	Fig. 13
t_{THL}/t_{TLH}	output transition time			15		19		22	ns	4.5	Fig. 11
t_{PZH}/t_{PZL}	3-state output enable time $\overline{OE}$ to Q_n			35		44		53	ns	4.5	Fig. 14
t_{PHZ}/t_{PLZ}	3-state output disable time $\overline{OE}$ to Q_n			30		38		45	ns	4.5	Fig. 14
t_W	SI pulse width HIGH or LOW	16			20		24		ns	4.5	Fig. 9
t_W	$\overline{SO}$ pulse width HIGH or LOW	16			20		24		ns	4.5	Fig. 10

DEVELOPMENT DATA

AC CHARACTERISTICS FOR 74HCT (Cont'd)

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_W	DIR pulse width HIGH or LOW	40			50		60		ns	4.5	Fig. 9
t_W	DOR pulse width HIGH or LOW	40			50		60		ns	4.5	Fig. 10
t_W	MR pulse width HIGH	16			20		24		ns	4.5	Fig. 8
t_{rem}	removal time MR to SI	15			19		22		ns	4.5	Fig. 15
t_{su}	set-up time D_n to SI	−7			−9		−11		ns	4.5	Fig. 16
t_h	hold time D_n to SI	25			31		38		ns	4.5	Fig. 16
f_{max}	maximum pulse frequency SI, $\overline{SO}$	14			11		9		MHz	4.5	Figs 9 and 10

DEVELOPMENT DATA

AC WAVEFORMS

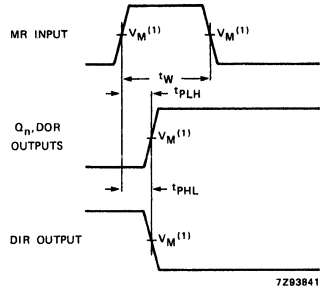


Fig. 8 Waveforms showing the MR input to DIR, DOR output propagation delays and the MR pulse width.

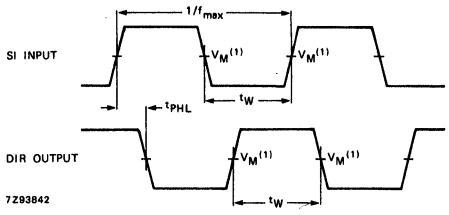


Fig. 9 Waveforms showing the SI input to DIR output propagation delay. The SI, DIR pulse widths and SI maximum pulse frequency.

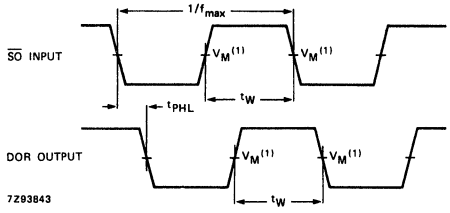


Fig. 10 Waveforms showing the $\overline{SO}$ input to DOF output propagation delay. The $\overline{SO}$, DOR p lse widths and $\overline{SO}$ maximum pulse frequency.

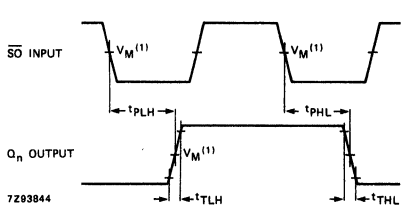


Fig. 11 Waveforms showing $\overline{SO}$ input to Q_n output propagation delays and output transition time.

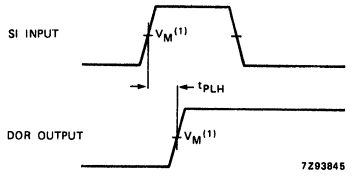


Fig. 12 Waveforms showing the SI input to DOR output propagation/ripple through delay.

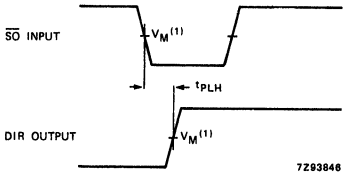


Fig. 13 Waveforms showing the $\overline{SO}$ input to DIR output propagation/ripple through delay.

AC WAVEFORMS (Cont'd)

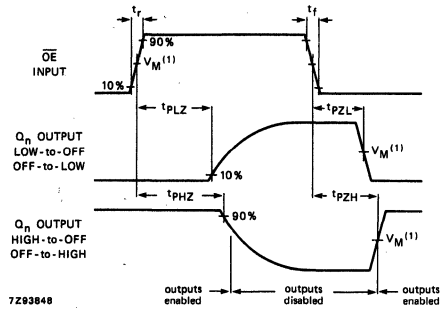


Fig. 14 Waveforms showing the 3-state enable and disable times for input $\overline{OE}$.

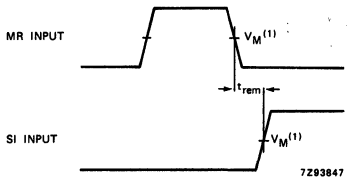


Fig. 15 Waveforms showing the MR input to SI input removal time.

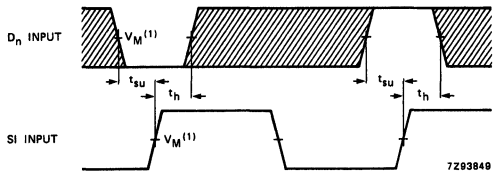


Fig. 16 Waveforms showing hold and set-up times for D_n input to SI input.

Note to Fig. 16

The shaded areas indicate when the input is permitted to change for predictable output performance.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

NOTES