PHILIPS

Video and associated systems
Types MAB8031AH to TDA1524A

IC02Na New series 1985

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Data handbook

Electronic components and materials

Integrated circuits

Book IC02Na 1985
New series

Video and associated systems

Bipolar, MOS

Types MAB8031AH to TDA1524A

NEW HANDBOOK SERIES

VIDEO AND ASSOCIATED SYSTEMS
BIPOLAR, MOS
Types MAB8031AH to TDA1524A

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DATA HANDBOOK SYSTEM

Our Data Handbook System comprises more than 60 books with specifications on electronic components, subassemblies and materials. It is made up of four series of handbooks:

ELECTRON TUBES	BLUE
SEMICONDUCTORS	RED
INTEGRATED CIRCUITS	PURPLE
COMPONENTS AND MATERIALS	GREEN

The contents of each series are listed on pages iv to viii.

The data handbooks contain all pertinent data available at the time of publication, and each is revised and reissued periodically.

When ratings or specifications differ from those published in the preceding edition they are indicated with arrows in the page margin. Where application information is given it is advisory and does not form part of the product specification.

Condensed data on the preferred products of Philips Electronic Components and Materials Division is given in our Preferred Type Range catalogue (issued annually).

Information on current Data Handbooks and on how to obtain a subscription for future issues is available from any of the Organizations listed on the back cover.
Product specialists are at your service and enquiries will be answered promptly.

ELECTRON TUBES (BLUE SERIES)

The blue series of data handbooks comprises:

T1 **Tubes for r.f. heating**

T2a **Transmitting tubes for communications, glass types**

T2b **Transmitting tubes for communications, ceramic types**

T3 **Klystrons**

T4 **Magnetrons for microwave heating**

T5 **Cathode-ray tubes**
Instrument tubes, monitor and display tubes, C.R. tubes for special applications

T6 **Geiger-Müller tubes**

T7 **Gas-filled tubes** (will not be reprinted)

T8 **Picture tubes and components**
Colour TV picture tubes, black and white TV picture tubes, colour monitor tubes for data graphic display, monochrome monitor tubes for data graphic display, components for colour television, components for black and white television and monochrome data graphic display

T9 **Photo and electron multipliers**

T10 **Plumbicon camera tubes and accessories**

T11 **Microwave semiconductors and components**

T12 **Vidicon and Newvicon camera tubes**

T13 **Image intensifiers**

T14 **Infrared detectors**

T15 **Dry reed switches**

Data collations on these subjects are available now.
Data Handbooks will be published in 1985.

T16 **Monochrome tubes and deflection units**
Black and white TV picture tubes, monochrome data graphic display tubes, deflection units

SEMICONDUCTORS (RED SERIES)

The red series of data handbooks comprises:

S1 **Diodes**
Small-signal germanium diodes, small-signal silicon diodes, voltage regulator diodes (< 1,5 W), voltage reference diodes, tuner diodes, rectifier diodes

S2a **Power diodes**

S2b **Thyristors and triacs**

S3 **Small-signal transistors**

S4a **Low-frequency power transistors and hybrid modules**

S4b **High-voltage and switching power transistors**

S5 **Field-effect transistors**

S6 **R.F. power transistors and modules**

S7 **Surface mounted semiconductors**

S8 **Devices for optoelectronics**
Photosensitive diodes and transistors, light-emitting diodes, displays, photocouplers, infrared sensitive devices, photoconductive devices.

S9 **Power MOS transistors**

S10 **Wideband transistors and wideband hybrid IC modules**

S11 **Microwave semiconductors** (to be published in this series in 1985)
At present available in Handbook T11

S12 **Surface acoustic wave devices**

INTEGRATED CIRCUITS (PURPLE SERIES)

The purple series of data handbooks comprises:

EXISTING SERIES		Superseded by:
IC1	**Bipolar ICs for radio and audio equipment**	
IC2	**Bipolar ICs for video equipment**	IC02N
IC3	**ICs for digital systems in radio, audio and video equipment**	
IC4	**Digital integrated circuits** CMOS HE4000B family	
IC5	**Digital integrated circuits – ECL** ECL10 000 (GX family), ECL100 000 (HX family), dedicated designs	IC08N
IC6	**Professional analogue integrated circuits**	
IC7	**Signetics bipolar memories**	
IC8	**Signetics analogue circuits**	IC11N
IC9	**Signetics TTL logic**	IC09N and IC15N
IC10	**Signetics Integrated Fuse Logic (IFL)**	IC13N
IC11	**Microprocessors, microcomputers and peripheral circuitry**	

NEW SERIES

IC01N	**Radio, audio and associated systems** Bipolar, MOS	
IC02N	**Video and associated systems** Bipolar, MOS	(published 1985)
IC03N	**Telephony equipment** Bipolar, MOS	
IC04N	**HE4000B logic family** CMOS	
IC05N	**HE4000B logic family uncased integrated circuits** CMOS	(published 1984)
IC06N	**High-speed CMOS; PC54/74HC/HCT/HCU** Logic family	(published 1985)
IC07N	**PC54/74HC/HCU/HCT uncased integrated circuits** HCMOS	
IC08N	**10K and 100K logic family** ECL	(published 1984)
IC09N	**Logic series** TTL	(published 1984)
IC10N	**Memories** MOS, TTL, ECL	
IC11N	**Linear LSI**	(published 1985)
IC12N	**Semi-custom gate arrays & cell libraries** ISL, ECL, CMOS	
IC13N	**Semi-custom** Integrated Fuse Logic	(published 1985)
IC14N	**Microprocessors, microcontrollers & peripherals** Bipolar, MOS	
IC15N	**Logic series** FAST TTL	(published 1984)

Note

Books available in the new series are shown with their date of publication.

COMPONENTS AND MATERIALS (GREEN SERIES)

The green series of data handbooks comprises:

C1 **Programmable controller modules**
PLC modules, PC20 modules

C2 **Television tuners, coaxial aerial input assemblies, surface acoustic wave filters**

C3 **Loudspeakers**

C4 **Ferroxcube potcores, square cores and cross cores**

C5 **Ferroxcube for power, audio/video and accelerators**

C6 **Synchronous motors and gearboxes**

C7 **Variable capacitors**

C8 **Variable mains transformers**

C9 **Piezoelectric quartz devices**

C10 **Connectors**

C11 **Non-linear resistors**
Voltage dependent resistors (VDR), light dependent resistors (LDR), negative temperature coefficient thermistors (NTC), positive temperature coefficient thermistors (PTC)

C12 **Potentiometers, encoders and switches**

C13 **Fixed resistors**

C14 **Electrolytic and solid capacitors**

C15 **Ceramic capacitors**

C16 **Permanent magnet materials**

C17 **Stepping motors and associated electronics**

C18 **Direct current motors**

C19 **Piezoelectric ceramics**

C20 **Wire-wound components for TVs and monitors**

C21 **Assemblies for industrial use**
HNIL FZ/30 series, NORbits 60-, 61-, 90-series, input devices

C22 **Film capacitors**

INTRODUCTION

This new edition of the data handbook for video and associated systems has been expanded to include MOS as well as bipolar integrated circuits as the use of MOS circuits in video equipment is becoming more and more widespread (remote control, digital tuning, teletext, etc.).

The expansion of data has made it necessary to produce this handbook in two volumes: IC02Na; IC02Nb.
IC02Na contains device data on types MAB8031AH to TDA1524A.
IC02Nb contains device data on types TDA2501 to TEA1002.
Each volume contains an index, associated information and package outlines.

The data handbook now includes dedicated video circuits and general purpose products (microcontrollers, display circuits, etc.) that find application in video systems. Full specifications are provided for the dedicated circuits; in some cases the general purpose circuits have short-form specifications. More detailed information can be found in the relevant data sheets and handbooks.

I²C bus compatible ICs

Some of the ICs in this handbook are I²C bus compatible (indicated by the logo shown below). The following clause applies:

Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C system provided the system conforms to the I²C specifications defined by Philips.

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MAB8048HWP	single-chip 8-bit μC; 1Kx8 ROM, 64x8 RAM	44-PLCC; SOT-187	a-31
MAB8048HT	single-chip 8-bit μC; 1Kx8 ROM, 64x8 RAM	VSO-40; SOT-158A	a-31
MAB8049HP	single-chip 8-bit μC; 2Kx8 ROM, 128x8 RAM	SOT-129	a-33
MAB8049HWP	single-chip 8-bit μC; 2Kx8 ROM, 128x8 RAM	44-PLCC; SOT-187	a-33
MAB8049HT	single-chip 8-bit μC; 2Kx8 ROM, 128x8 RAM	VSO-40; SOT-158A	a-33
MAB8050HP	single-chip 8-bit μC; 4Kx8 ROM, 256x8 RAM	SOT-129	a-35
MAB8051AHP	single-chip 8-bit μC; 4Kx8 ROM, 128x8 RAM	SOT-129	a-29
MAB8051AHWP	single-chip 8-bit μC; 4Kx8 ROM, 128x8 RAM	44-PLCC; SOT-187	a-29
MAB8400B	single-chip 8-bit μC; 128 RAM bytes	28/28 "Piggy back"	a-37
MAB8400WP	single-chip 8-bit μC; 128 RAM bytes	68-PLCC; SOT-188A	a-37
MAB8401B	like MAB8400 but with 8-bit LED-driver	28/28 "Piggy back"	a-37
MAB8401WP	like MAB8400 but with 8-bit LED-driver	68-PLCC; SOT-188A	a-37
MAB8410P	single-chip 8-bit μC; 1K ROM/64 RAM bytes	SOT-117A	a-37
MAB8410T	single-chip 8-bit μC; 1K ROM/64 RAM bytes	SO-28; SOT-136A	a-37
MAB8420P	single-chip 8-bit μC; 2K ROM/64 RAM bytes	SOT-117A	a-37
MAB8420T	single-chip 8-bit μC; 2K ROM/64 RAM bytes	SO-28; SOT-136A	a-37
MAB8421P	single-chip 8-bit μC; 2K ROM/64 RAM bytes plus 8-bit LED driver	SOT-117A	a-37
MAB8421T	single-chip 8-bit μC; 2K ROM/64 RAM bytes plus 8-bit LED driver	SO-28; SOT-136A	a-37
MAB8422P	single-chip 8-bit μC; 2K ROM/64 RAM bytes	SOT-146	a-39
MAB8440P	single-chip 8-bit μC; 4K ROM/128 RAM bytes	SOT117A	a-37

type number	description	package code	page
MAB8440T	single-chip 8-bit μC; 4K ROM/128 RAM bytes	SO-28; SOT-136A	a-37
MAB8441P	single-chip 8-bit μC; 4K ROM/128 RAM bytes plus 8-bit LED driver	SOT-117A	a-37
MAB8441T	single-chip 8-bit μC; 2K ROM/128 RAM bytes plus 8-bit LED driver	SO-28; SOT-136A	a-37
MAB8442P	single-chip 8-bit μC; 4K ROM/128 RAM bytes	SOT-146	a-39
MAB8461P	single-chip 8-bit μC; 6K ROM/128 RAM bytes plus 8-bit LED driver	SOT-117A	a-37
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MAF8031AHWP	single-chip 8-bit μC; ROM-less version of MAB8051AH; extended temperature	44-PLCC; SOT-187	a-29
MAF8035HLP	single-chip 8-bit μC; ROM-less version of MAB8048H; extended temperature	SOT-129	a-31
MAF8035HLWP	single-chip 8-bit μC; ROM-less version of MAB8048H; extended temperature	44-PLCC; SOT-187	a-31
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MAF80A39HLP	single-chip 8-bit μC; ROM-less version of MAB80A49H; reduced frequency; extended temperature	SOT-129	a-33
MAF8048HP	single-chip 8-bit μC; 1Kx8 ROM, 64x8 RAM; extended temperature	SOT-129	a-31
MAF8048HWP	single-chip 8-bit μC; 1Kx8 ROM, 64x8 RAM; extended temperature	44-PLCC; SOT-187	a-31
MAF8049HP	single-chip 8-bit μC; 2Kx8 ROM, 128x8 RAM; extended temperature	SOT-129	a-33
MAF8049HWP	single-chip 8-bit μC; 2Kx8 ROM, 128x8 RAM; extended temperature	44-PLCC; SOT-187	a-33
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MAF8051AHP	single-chip 8-bit μC; 4Kx8 ROM, 128x8 RAM; extended temperature	SOT-129	a-29
MAF8051AHWP	single-chip 8-bit μC; 4Kx8 ROM, 128x8 RAM; extended temperature	44-PLCC; SOT-187	a-29
MAF8410P	single-chip 8-bit μC; 1K ROM/64 RAM bytes	SOT-117A	a-37
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MAF8421P	single-chip 8-bit μC; 2K ROM/64 RAM bytes plus 8-bit LED driver	SOT-117A	a-37
MAF8422P	single-chip 8-bit μC; 2K ROM/64 RAM bytes; extended temperature	SOT-146	a-39
MAF84A22P	single-chip 8-bit μC; 2K ROM/64 RAM bytes; reduced frequency; extended temperature	SOT-146	a-39
MAF8440P	single-chip 8-bit μC; 4K ROM/128 RAM bytes	SOT-117A	a-37

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MAF84A42P	single-chip 8-bit μC; 4K ROM/128 RAM bytes; reduced frequency; extended temperature	SOT-146	a-39
MAF8461P	single-chip 8-bit μC; 6K ROM/128 RAM bytes plus 8-bit LED driver	SOT-117A	a-37
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PCB80C48WP	single-chip 8-bit μC; 1Kx8 ROM, 64x8 RAM	44-PLCC;SOT-187	a-41
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type number	description	package code	page
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type number	description	package code	page
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TDA2594	horizontal combination with transmitter identification	SOT-102DS	b-229
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TDA3651	vertical deflection circuit	SOT-110B	b-515
TDA3651A	vertical deflection circuit	SOT-131B	b-523
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TDA3652	vertical deflection circuit	SOT-131B	b-531
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TDA5030	mixer/oscillator for VHF tuner	SOT-102HE	b-695
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GENERAL

Type designation
Rating systems
Handling MOS devices

PRO ELECTRON TYPE DESIGNATION CODE FOR INTEGRATED CIRCUITS

This type nomenclature applies to semiconductor monolithic, semiconductor multi-chip, thin-film, thick-film and hybrid integrated circuits.

A basic number consists of:

THREE LETTERS FOLLOWED BY A SERIAL NUMBER

FIRST AND SECOND LETTER

1. DIGITAL FAMILY CIRCUITS

   The FIRST TWO LETTERS identify the FAMILY (see note 1).

2. SOLITARY CIRCUITS

   The FIRST LETTER divides the solitary circuits into:

   S : Solitary digital circuits
   T : Analogue circuits
   U : Mixed analogue/digital circuits

   The SECOND LETTER is a serial letter without any further significance except 'H' which stands for hybrid circuits.

3. MICROPROCESSORS

   The FIRST TWO LETTERS identify microprocessors and correlated circuits as follows:

   MA : { Microcomputer / Central processing unit
   MB : Slice processor (see note 2)
   MD : Correlated memories
   ME : Other correlated circuits (interface, clock, peripheral controller, etc.)

4. CHARGE-TRANSFER DEVICES AND SWITCHED CAPACITORS

   The FIRST TWO LETTERS identify the following:

   NH : Hybrid circuits
   NL : Logic circuits
   NM : Memories
   NS : Analogue signal processing, using switched capacitors
   NT : Analogue signal processing, using CTDs
   NX : Imaging devices
   NY : Other correlated circuits

Notes

1. A logic family is an assembly of digital circuits designed to be interconnected and defined by its basic electrical characteristics (such as: supply voltage, power consumption, propagation delay, noise immunity).
2. By 'slice processor' is meant: a functional slice of microprocessor.

THIRD LETTER

It indicates the operating ambient temperature range.
The letters A to G give information about the temperature:

A : temperature range not specified
B : 0 to + 70 °C
C : −55 to + 125 °C
D : −25 to + 70 °C
E : −25 to + 85 °C
F : −40 to + 85 °C
G : −55 to + 85 °C

If a circuit is published for another temperature range, the letter indicating a narrower temperature range may be used or the letter 'A'.

Example: the range 0 to + 75 °C can be indicated by 'B' or 'A'.

SERIAL NUMBER

This may be either a 4-digit number assigned by Pro Electron, or the serial number (which may be a combination of figures and letters) of an existing company type designation of the manufacturer.

To the basic type number may be added:

A VERSION LETTER

Indicates a minor variant of the basic type or the package. Except for 'Z', which means customized wiring, the letter has no fixed meaning. The following letters are recommended for package variants:

C : for cylindrical
D : for ceramic DIL
F : for flat pack
L : for chip on tape
P : for plastic DIL
Q : for QIL
T : for miniature plastic (mini-pack)
U : for uncased chip

Alternatively a TWO LETTER SUFFIX may be used instead of a single package version letter, if the manufacturer (sponsor) wishes to give more information.

FIRST LETTER: General shape

C : Cylindrical
D : Dual-in-line (DIL)
E : Power DIL (with external heatsink)
F : Flat (leads on 2 sides)
G : Flat (leads on 4 sides)
K : Diamond (TO-3 family)
M : Multiple-in-line (except Dual-, Triple-, Quadruple-in-line)
Q : Quadruple-in-line (QIL)
R : Power QIL (with external heatsink)
S : Single-in-line
T : Triple-in-line

SECOND LETTER: Material

C : Metal-ceramic
G : Glass-ceramic (cerdip)
M : Metal
P : Plastic

A hyphen precedes the suffix to avoid confusion with a version letter.

RATING SYSTEMS

The rating systems described are those recommended by the International Electrotechnical Commission (IEC) in its Publication 134.

DEFINITIONS OF TERMS USED

Electronic device. An electronic tube or valve, transistor or other semiconductor device.

Note
This definition excludes inductors, capacitors, resistors and similar components.

Characteristic. A characteristic is an inherent and measurable property of a device. Such a property may be electrical, mechanical, thermal, hydraulic, electro-magnetic, or nuclear, and can be expressed as a value for stated or recognized conditions. A characteristic may also be a set of related values, usually shown in graphical form.

Bogey electronic device. An electronic device whose characteristics have the published nominal values for the type. A bogey electronic device for any particular application can be obtained by considering only those characteristics which are directly related to the application.

Rating. A value which establishes either a limiting capability or a limiting condition for an electronic device. It is determined for specified values of environment and operation, and may be stated in any suitable terms.

Note
Limiting conditions may be either maxima or minima.

Rating system. The set of principles upon which ratings are established and which determine their interpretation.

Note
The rating system indicates the division of responsibility between the device manufacturer and the circuit designer, with the object of ensuring that the working conditions do not exceed the ratings.

ABSOLUTE MAXIMUM RATING SYSTEM

Absolute maximum ratings are limiting values of operating and environmental conditions applicable to any electronic device of a specified type as defined by its published data, which should not be exceeded under the worst probable conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device, taking no responsibility for equipment variations, environmental variations, and the effects of changes in operating conditions due to variations in the characteristics of the device under consideration and of all other electronic devices in the equipment.

The equipment manufacturer should design so that, initially and throughout life, no absolute maximum value for the intended service is exceeded with any device under the worst probable operating conditions with respect to supply voltage variation, equipment component variation, equipment control adjustment, load variations, signal variation, environmental conditions, and variations in characteristics of the device under consideration and of all other electronic devices in the equipment.

DESIGN MAXIMUM RATING SYSTEM

Design maximum ratings are limiting values of operating and environmental conditions applicable to a bogey electronic device of a specified type as defined by its published data, and should not be exceeded under the worst probable conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device, taking responsibility for the effects of changes in operating conditions due to variations in the characteristics of the electronic device under consideration.

The equipment manufacturer should design so that, initially and throughout life, no design maximum value for the intended service is exceeded with a bogey device under the worst probable operating conditions with respect to supply voltage variation, equipment component variation, variation in characteristics of all other devices in the equipment, equipment control adjustment, load variation, signal variation and environmental conditions.

DESIGN CENTRE RATING SYSTEM

Design centre ratings are limiting values of operating and environmental conditions applicable to a bogey electronic device of a specified type as defined by its published data, and should not be exceeded under normal conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device in average applications, taking responsibility for normal changes in operating conditions due to rated supply voltage variation, equipment component variation, equipment control adjustment, load variation, signal variation, environmental conditions, and variations in the characteristics of all electronic devices.

The equipment manufacturer should design so that, initially, no design centre value for the intended service is exceeded with a bogey electronic device in equipment operating at the stated normal supply voltage.

HANDLING MOS DEVICES

Though all our MOS integrated circuits incorporate protection against electrostatic discharges, they can nevertheless be damaged by accidental over-voltages. In storing and handling them, the following precautions are recommended.

Caution

Testing or handling and mounting call for special attention to personal safety. Personnel handling MOS devices should normally be connected to ground via a resistor.

Storage and transport

Store and transport the circuits in their original packing. Alternatively, use may be made of a conductive material or special IC carrier that either short-circuits all leads or insulates them from external contact.

Testing or handling

Work on a conductive surface (e.g. metal table top) when testing the circuits or transferring them from one carrier to another. Electrically connect the person doing the testing or handling to the conductive surface, for example by a metal bracelet and a conductive cord or chain. Connect all testing and handling equipment to the same surface.
Signals should not be applied to the inputs while the device power supply is off. All unused input leads should be connected to either the supply voltage or ground.

Mounting

Mount MOS integrated circuits on printed circuit boards *after* all other components have been mounted. Take care that the circuits themselves, metal parts of the board, mounting tools, and the person doing the mounting are kept at the same electric (ground) potential. If it is impossible to ground the printed-circuit board the person mounting the circuits should touch the board before bringing MOS circuits into contact with it.

Soldering

Soldering iron tips, including those of low-voltage irons, or soldering baths should also be kept at the same potential as the MOS circuits and the board.

Static charges

Dress personnel in clothing of non-electrostatic material (no wool, silk or synthetic fibres). After the MOS circuits have been mounted on the board proper handling precautions should still be observed. Until the sub-assemblies are inserted into a complete system in which the proper voltages are supplied, the board is no more than an extension of the leads of the devices mounted on the board. To prevent static charges from being transmitted through the board wiring to the device it is recommended that conductive clips or conductive tape be put on the circuit board terminals.

Transient voltages

To prevent permanent damage due to transient voltages, do not insert or remove MOS devices, or printed-circuit boards with MOS devices, from test sockets or systems with power on.

Voltage surges

Beware of voltage surges due to switching electrical equipment on or off, relays and d.c. lines.

DEVICE DATA

FOR DETAILED INFORMATION SEE RELEVANT DATA BOOK OR DATA SHEET

SINGLE-CHIP 8-BIT MICROCONTROLLER

DESCRIPTION

The MAB8051AH family of single-chip 8-bit microcontrollers is manufactured in an advanced 2 μ NMOS process. The family consists of the following members:

- MAB8031AH: ROM-less version of the MAB8051AH
- MAB8051AH: 4 K bytes ROM, 128 bytes RAM

Both types are available in 8, 10 and 12 MHz versions. In the following, the generic term "MAB8051AH" is used to refer to both family members.

The device provides hardware features, architectural enhancements and new instructions to function as a controller for applications requiring up to 64 K bytes of program memory and/or up to 64 K bytes of data storage.

The MAB8051AH contains a non-volatile 4 K x 8 read-only program memory (not ROM-less version); a volatile 128 x 8 read/write data memory; 32 I/O lines; two 16-bit timer/event counters; a five-source, two-priority-level, nested interrupt structure; a serial I/O port for either multi-processor communications, I/O expansion, or full duplex UART; and on-chip oscillator and timing circuits. For systems that require extra capability, the MAB8051AH can be expanded using standard TTL compatible memories and logic.

The device also functions as an arithmetic processor having facilities for both binary and BCD arithmetic plus bit-handling capabilities. The instruction set consists of 255 instructions; 44% one-byte, 41% two-byte and 15% three-byte. With a 12 MHz crystal, 58% of the instructions are executed in 1 μs and 40% in 2 μs. Multiply and divide instructions require 4 μs. Multiply, divide, subtract and compare are among the many instructions added to the standard MAB8048H instruction set.

Features

- 4 K x 8 ROM (8051AH only), 128 x 8 RAM
- Four 8-bit ports, 32 I/O lines
- Two 16-bit timer/event counters
- Full-duplex serial port
- External memory expandable to 128 K
- Boolean processing
- 218 bit-addressable locations
- On-chip oscillator
- Five-source interrupt structure with two priority levels
- 58% of instructions executed in 1 μs; multiply and divide in 4 μs (at 12 MHz clock)
- Enhanced architecture with:
  - non-page-oriented instructions
  - direct addressing
  - four 8-bit register banks
  - stack depth up to 128-bytes
  - multiply, divide, substract and compare.

PACKAGE OUTLINES

MAB8031/51AHP; MAF8031/51AHP: 40-lead DIL; plastic (SOT-129).
MAB8031/51AHWP; MAF8031/51AHWP: 44-lead, plastic leaded-chip-carrier (PLCC); SOT-187.

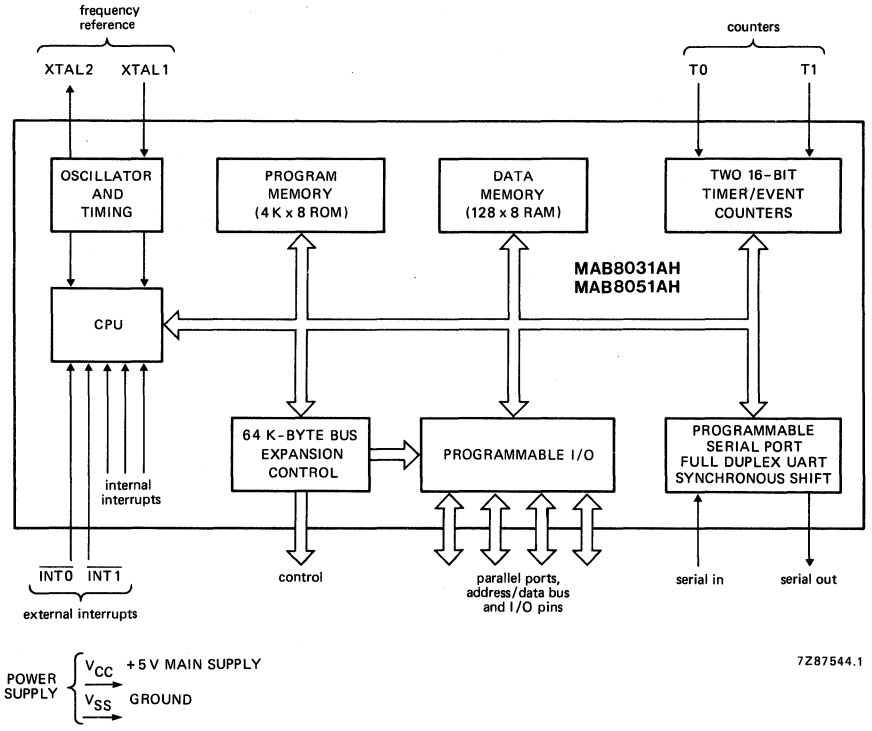


Fig. 1 Block diagram.

FOR DETAILED INFORMATION SEE RELEVANT DATA BOOK OR DATA SHEET

SINGLE-CHIP 8-BIT MICROCONTROLLER

DESCRIPTION

The MAB8048H family of single-chip 8-bit microcontrollers are fabricated in H-MOS.
Two interchangeable (pin compatible) versions are available:

- The **MAB8048H** with resident mask-programmed ROM,
- The **MAB8035HL** without resident program memory for use with external EPROM/ROM.

The MAB8048H family are designed to be efficient control processors as well as arithmetic processors. Their instruction set allows the user to directly set and reset individual I/O lines as well as test individual bits within the accumulator. A large variety of branch and table look-up instructions enable efficient implementation of standard logic functions. Code efficiency is high; over 70% of the instructions are single byte; all others are two byte.

An on-chip 8-bit counter is provided, which can count either machine cycles (÷ 32) or external events. The counter can be programmed to cause an interrupt to the processor.
Program and data memories can be expanded using standard devices. Input/output capabilities can be expanded using standard devices.

FEATURES

- 8-bit CPU, ROM, RAM, I/O in a single 40-pin package
- 1 K x 8 ROM, 64 x 8 RAM, 27 I/O lines
- Internal counter/timer
- Internal oscillator, clock driver
- Single-level interrupts: external and counter/timer
- 17 internal registers: accumulator, 16 addressable registers
- Over 90 instructions: 70% single byte
- All instructions: 1 or 2 cycles (1,875 μs per cycle)
- Easily expandable memory and I/O
- TTL compatible inputs and outputs
- Single 5 V supply

APPLICATIONS

- Peripheral interfaces and controllers
- Test and measurement instruments
- Sequencers
- Audio/video systems
- Environmental control systems
- Modems and data enciphering

PACKAGE OUTLINES

MAB8035HLP; MAB8048HP: 40-lead DIL; plastic (SOT-129).
MAB8035HLWP; MAB8048HWP: 44-lead, plastic leaded-chip-carrier (PLCC); SOT-187.
MAB8035HLT; MAB8048HT: 40-lead mini-pack; plastic (VSO-40; SOT-158A).
MAF8035HLP; MAF8048HP: 40-lead DIL; plastic (SOT-129).
MAF8035HLWP; MAF8048HWP: 44-lead, plastic leaded-chip-carrier (PLCC); SOT-187.

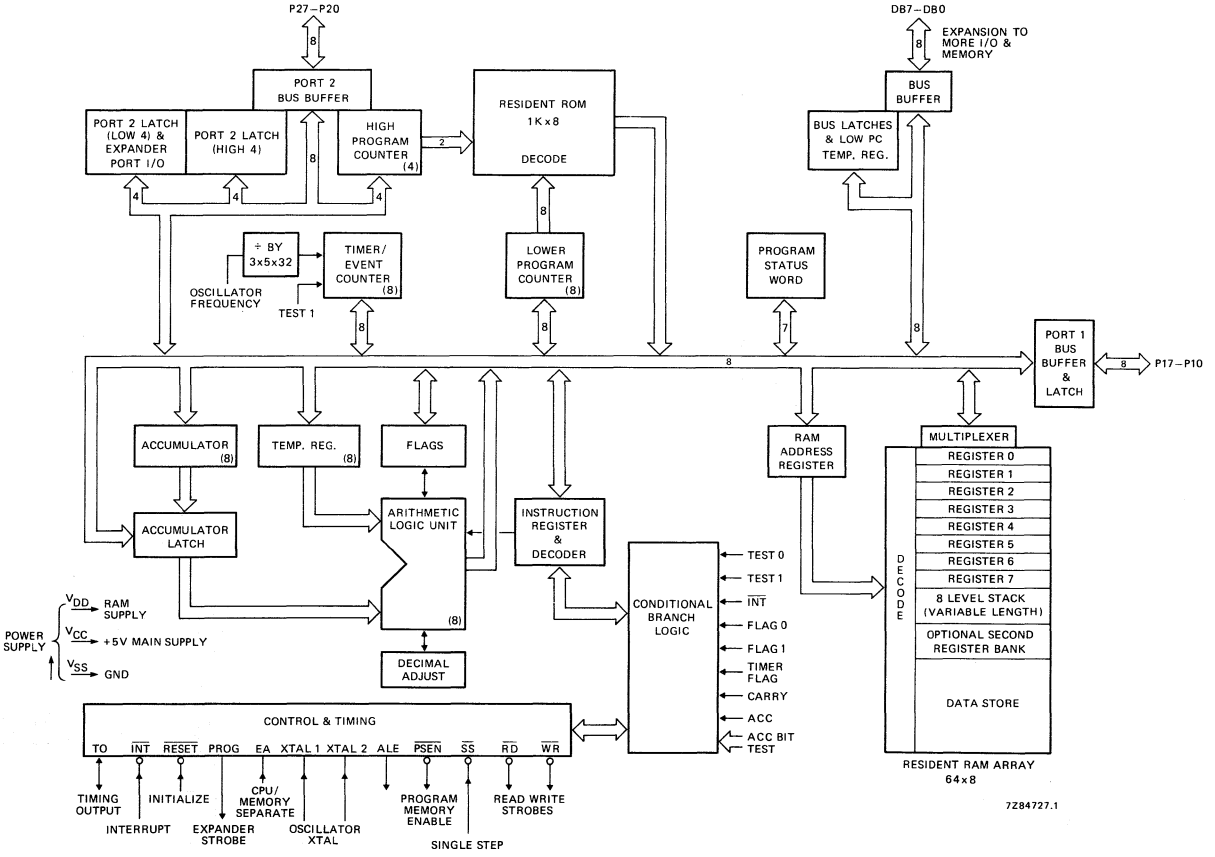


Fig. 1 Block diagram.

FOR DETAILED INFORMATION SEE RELEVANT DATA BOOK OR DATA SHEET

SINGLE-CHIP 8-BIT MICROCONTROLLER

DESCRIPTION

The MAB8049H family of single-chip 8-bit microcontrollers are fabricated in H-MOS.
Two interchangeable (pin compatible) versions are available:

- The MAB8049H with resident mask-programmed ROM,
- The MAB8039HL without resident program memory for use with external EPROM/ROM.

The MAB8049H family are designed to be efficient control processors as well as arithmetic processors. Their instruction set allows the user to directly set and reset individual I/O lines as well as test individual bits within the accumulator. A large variety of branch and table look-up instructions enable efficient implementation of standard logic functions. Code efficiency is high; over 70% of the instructions are single byte; all others are two byte.

An on-chip 8-bit counter is provided, which can count either machine cycles (÷ 32) or external events. The counter can be programmed to cause an interrupt to the processor.
Program and data memories can be expanded using standard devices. Input/output capabilities can be expanded using standard devices.

FEATURES

- 8-bit CPU, ROM, RAM, I/O in a single 40-pin package
- 2 K x 8 ROM, 128 x 8 RAM, 27 I/O lines
- Internal counter/timer
- Internal oscillator, clock driver
- Single-level interrupts: external and counter/timer
- 17 internal registers: accumulator, 16 addressable registers
- Over 90 instructions: 70% single byte
- All instructions: 1 or 2 cycles
- Easily expandable memory and I/O
- TTL compatible inputs and outputs
- Single 5 V supply
- Standard and extended temperature range

APPLICATIONS

- Peripheral interfaces and controllers
- Test and measurement instruments
- Sequencers
- Audio/video systems
- Environmental control systems
- Modems and data enciphering

PACKAGE OUTLINES

MAB8039HLP; MAB8049HP: 40-lead DIL; plastic (SOT-129).
MAB8039HLWP; MAB8049HWP: 44-lead, plastic leaded-chip-carrier (PLCC); SOT-187.
MAB8039HLT; MAB8049HT: 40-lead mini-pack; plastic (VSO-40; SOT-158A).
MAF8039HLP; MAF8049HP : 40-lead DIL; plastic (SOT-129).
MAF8039HLWP; MAF8049HWP: 44-lead, plastic leaded-chip-carrier (PLCC); SOT-187.
MAF80A39HLP; MAF80A49HP: 40-lead DIL; plastic (SOT-129).

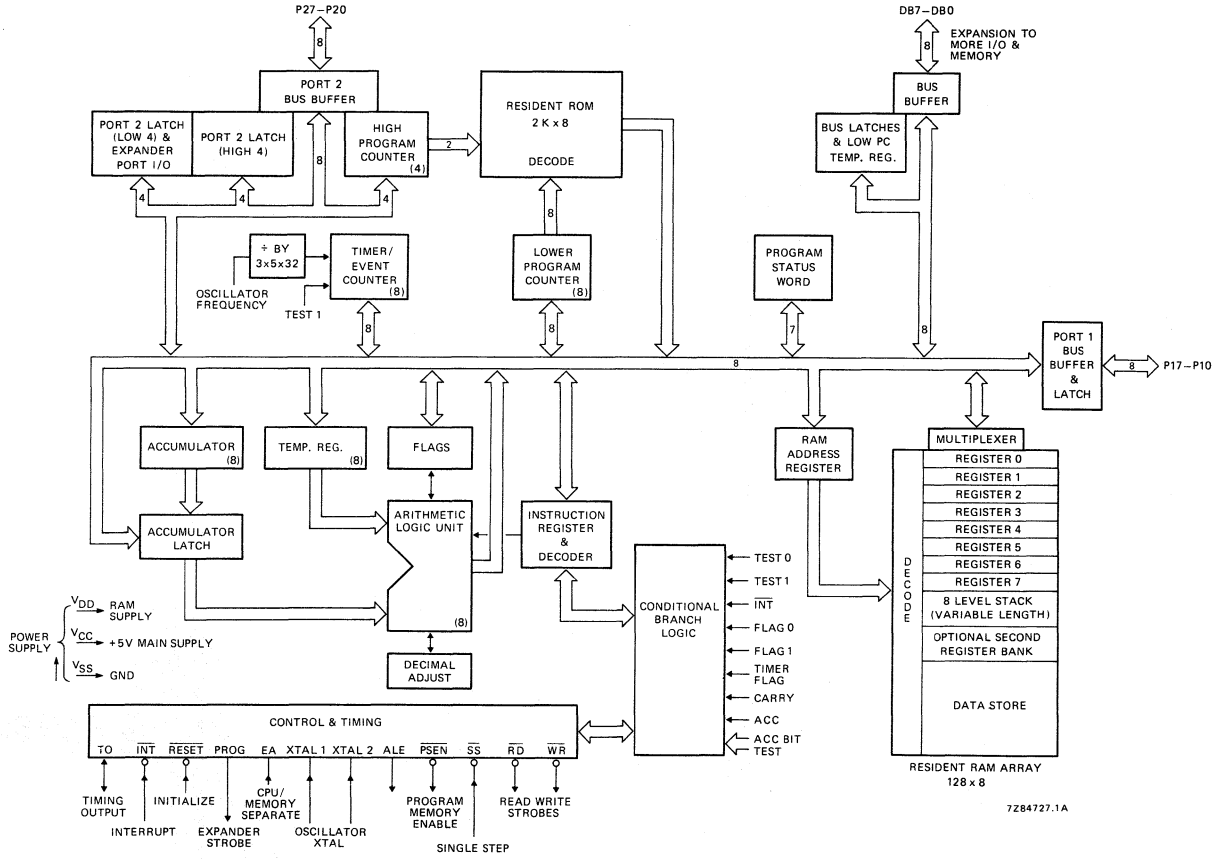


Fig. 1 Block diagram.

FOR DETAILED INFORMATION SEE RELEVANT DATA BOOK OR DATA SHEET

SINGLE-CHIP 8-BIT MICROCONTROLLER

DESCRIPTION

The MAB8050H family of single-chip 8-bit microcontrollers are fabricated in H-MOS.
Two interchangeable (pin compatible) versions are available:

- The **MAB8050H** with resident mask-programmed ROM,
- The **MAB8040L** without resident program memory for use with external EPROM/ROM.

The MAB8040H family are designed to be efficient control processors as well as arithmetic processors. Their instruction set allows the user to directly set and reset individual I/O lines as well as test individual bits within the accumulator. A large variety of branch and table look-up instructions enable efficient implementation of standard logic functions. Code efficiency is high; over 70% of the instructions are single byte; all others are two byte.

An on-chip 8-bit counter is provided, which can count either machine cycles (÷ 32) or external events. The counter can be programmed to cause an interrupt to the processor.
Program and data memories can be expanded using standard devices. Input/output capabilities can be expanded using standard devices.

FEATURES

- 8-bit CPU, ROM, RAM, I/O in a single 40-pin package
- 4 K x 8 ROM, 256 x 8 RAM, 27 I/O lines
- Internal counter/timer
- Internal oscillator, clock driver
- Single-level interrupts: external and counter/timer
- 17 internal registers: accumulator, 16 addressable registers
- Over 90 instructions: 70% single byte
- All instructions: 1 or 2 cycles (1,36/2,5 μs per cycle)
- Easily expandable memory and I/O
- TTL compatible inputs and outputs
- Single 5 V supply

APPLICATIONS

- Peripheral interfaces and controllers
- Test and measurement instruments
- Sequencers
- Audio/video systems
- Environmental control systems
- Modems and data enciphering

PACKAGE OUTLINES

MAB8040HLP; MAB8050HP: 40-lead DIL; plastic (SOT-129).

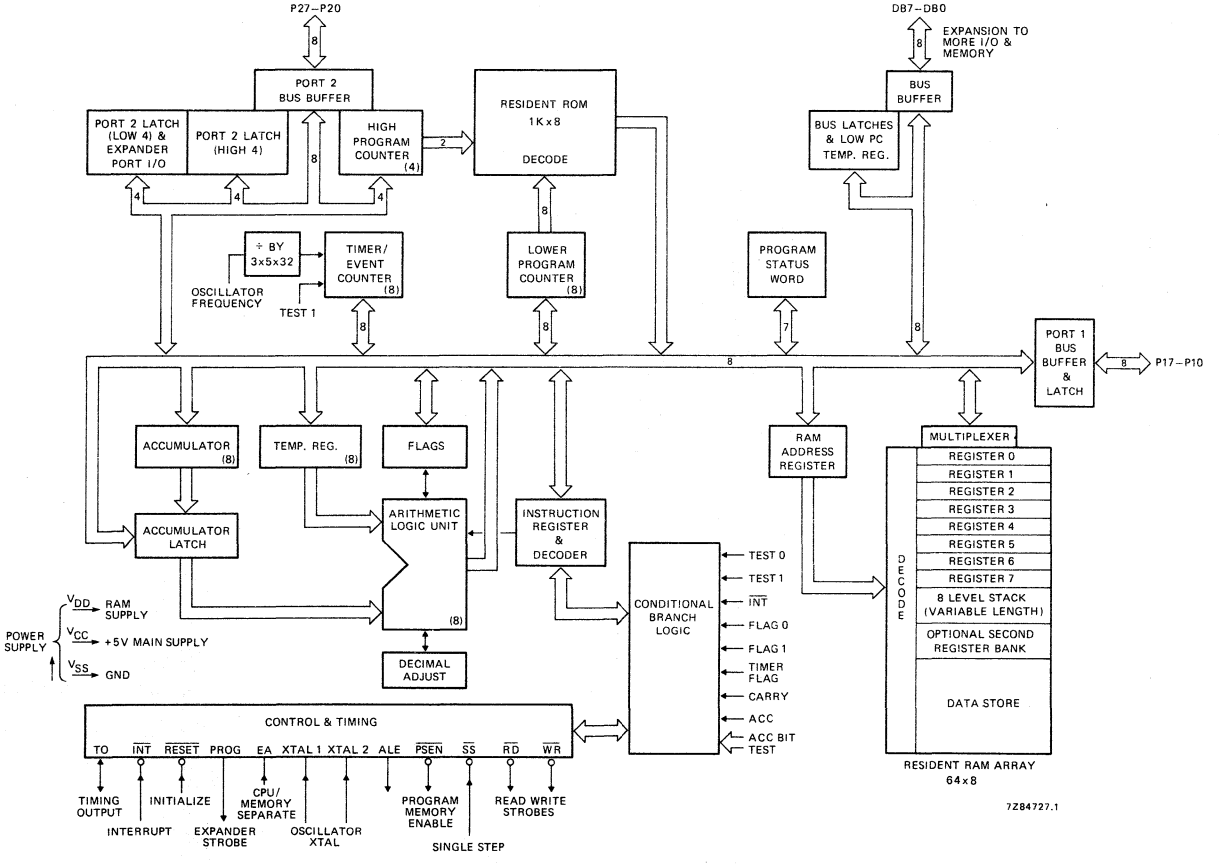


Fig. 1 Block diagram.

FOR DETAILED INFORMATION SEE RELEVANT DATA BOOK OR DATA SHEET

SINGLE-CHIP 8-BIT MICROCONTROLLER

DESCRIPTION

The MAB84XX family of microcontrollers is fabricated in NMOS. The family consists of 8 devices:

- MAB8400 – 128 RAM bytes, external program memory
- MAB8401 – like 8400 but with 8-bit LED-driver (10 mA), emulation of MAB/F 8422/42* possible
- MAB/F 8410 – 1K ROM/ 64 RAM bytes
- MAB/F 8420 – 2K ROM/ 64 RAM bytes
- MAB/F 8440 – 4K ROM/128 RAM bytes
- MAB/F 8421 – 2K ROM/ 64 RAM bytes plus 8-bit LED-driver
- MAB/F 8441 – 4K ROM/128 RAM bytes plus 8-bit LED-driver
- MAB/F 8461 – 6K ROM/128 RAM bytes plus 8-bit LED-driver

Each version has 20 quasi-bidirectional I/O port lines, one serial I/O line, one single-level vectored interrupt, an 8-bit timer event counter and on-board clock oscillator and clock circuits. Two 20-pin versions, MAB/F 8422 and MAB/F 8442* are also available.

This microcontroller family is designed to be an efficient controller as well as an arithmetic processor. The instruction set is based on that of the MAB8048. The microcontrollers have extensive bit handling abilities and facilities for both binary and BCD arithmetic.

For detailed information see the "Users manual Single-chip microcomputer" (supplied upon request).

* See data sheet on MAB/F 8422/42.

Features

- 8-bit: CPU, ROM, RAM and I/O in a single 28-lead DIL package
- 1K, 2K, 4K or 6K ROM bytes plus a ROM-less version
- 64 or 128 RAM bytes
- 20 quasi-bidirectional I/O port lines
- Two testable inputs: one of which can be used to detect zero cross-over, the other is also the external interrupt input
- Single level vectored interrupts: external, timer/event counter, serial I/O
- Serial I/O that can be used in single or multi-master systems (serial I/O data via an existing port line and clock via a dedicated line)
- 8-bit programmable timer/event counter
- Internal oscillator, generated with inductor, crystal, ceramic resonator or external source
- Over 80 instructions (based on MAB8048) all of 1 or 2 cycles
- Single 5 V power supply (± 10%)
- Operating temperature ranges:

0 to + 70 °C	MAB84XX family
–40 to + 85 °C	MAF84XX family
–40 to + 110 °C	MAF84AXX family

PACKAGE OUTLINES

MAB8400/01B: 28-lead 'Piggy-back' package (with up to 28-pin EPROM on top).
MAB8400WP: 68-lead plastic leaded-chip-carrier (PLCC); SOT-188A.
MAB8401WP: 68-lead plastic leaded-chip-carrier (PLCC); SOT-188A.
MAB/F8410/20/21/40/41/61P: 28-lead DIL; plastic (SOT-117A).
MAB8410/20/21/40/41T: 28-lead mini-pack; plastic (SO-28; SOT-136A).

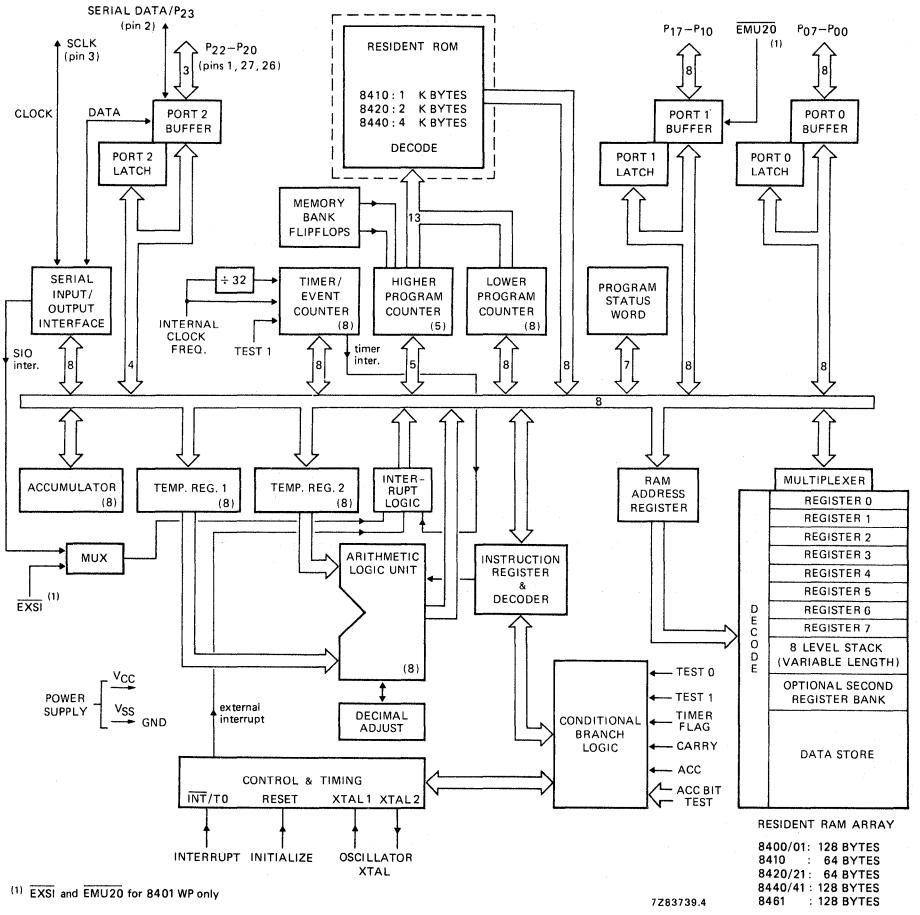


Fig. 2a Block diagram of the MAB8400 family.

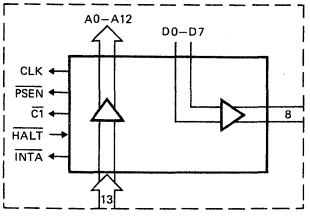


Fig. 2b Replacement of dotted part in Fig. 2a, showing the MAB8400F bond-out version.

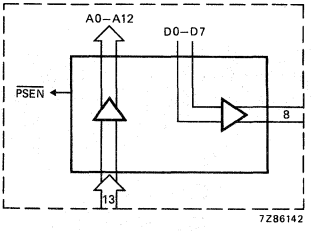


Fig. 2c Replacement of dotted part in Fig. 2a, for the MAB8400B 'Piggy-back' version.

FOR DETAILED INFORMATION SEE RELEVANT DATA BOOK OR DATA SHEET

SINGLE-CHIP 8-BIT MICROCONTROLLER

The MAB8422/8442 is a high-performance microcontroller incorporating dedicated hardware, memory capacity and I/O lines. This dedication means a microcontroller can be economically installed in high-volume products where its main function is control.

The MAB8422/8442 is a 20 pin, single-chip 8-bit microcontroller that has been developed from the 28 pin MAB8420/8440 microcontrollers. The versions are:

- MAB8422 - 2K ROM/64 RAM bytes
- MAB8442 - 4K ROM/128 RAM bytes

Each version has 15 I/O port lines comprising one 8-bit parallel port (P0), one 2-bit parallel port (P10 and P11 that are shared with the serial I/O lines SDA and SCL), one 3-bit parallel port (P20-P22) and two input lines ($\overline{INT}$/T0 and T1).

The serial I/O interface is I^2C compatible and therefore the MAB8422/8442 can operate as a slave or a master in single and multi-master systems. Conversion from parallel to serial data when transmitting, and vice versa when receiving, is done mainly in software. There is a minimum of hardware for the serial I/O implemented. This hardware is controlled by the status of the SDA and SCL lines and can be read or written under software control. Standard software for I^2C-bus control is available on request.

Features

- 8-bit: CPU, ROM, RAM and I/O
- 20 pin package
- MAB8422: 2K ROM/64 RAM bytes
- MAB8442: 4K ROM/128 RAM bytes
- 13 quasi-bidirectional I/O port lines
- Two testable inputs $\overline{INT}$/T0 and T1
- High current output on P0 (I_{OL} = 10 mA at V_{OL} = 1 V)
- One interrupt line combined with the testable input line $\overline{INT}$/T0
- Single-level interrupts: external, timer/event counter, serial I/O
- I^2C-compatible serial I/O that can be used in single or multi-master systems (serial I/O data and clock via P10 and P11 port lines, respectively)
- 8-bit programmable timer/event counter
- Internal oscillator, generated with inductor, crystal, ceramic resonator or external source
- Over 80 instructions (based on MAB8048)
- All instructions 1 or 2 cycles, cycle time dependent on oscillator frequency
- Single 5 V power supply
- 0 to 70 °C operating temperature range, also versions for −40 to 85 °C and −40 to 110 °C

PACKAGE OUTLINES

MAB/F8422/42P: 20-lead DIL; plastic (SOT-146).
MAF84A22/A42P: 20-lead DIL; plastic (SOT-146).

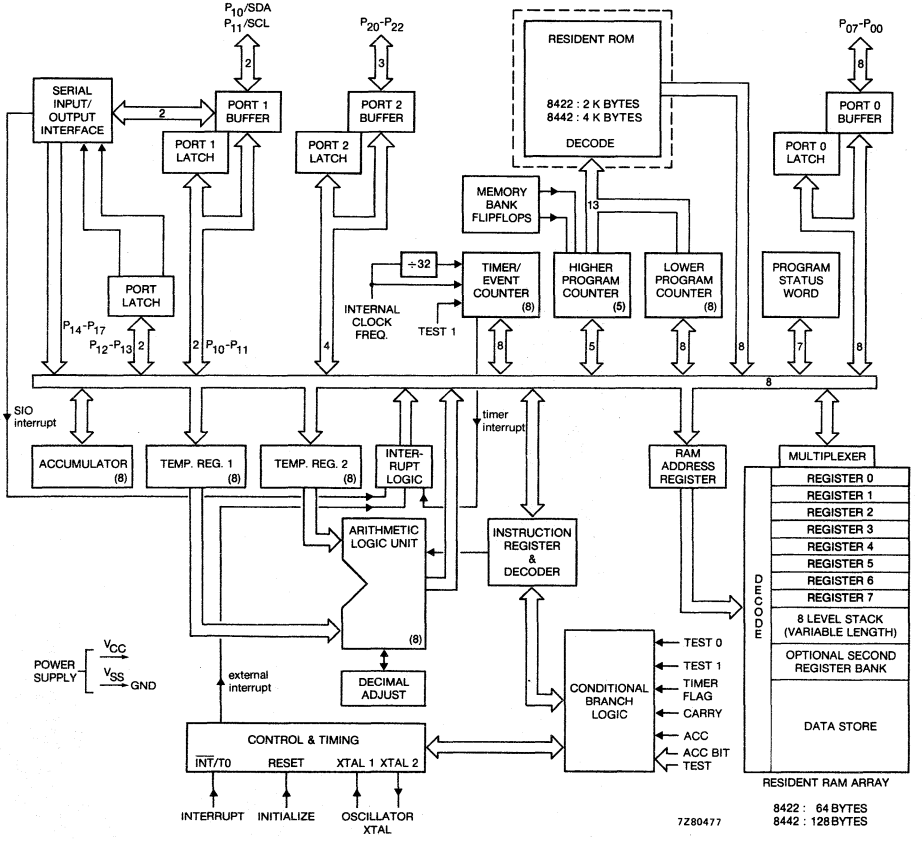


Fig. 1 Block diagram of the MAB8422/8442.

FOR DETAILED INFORMATION SEE RELEVANT DATA BOOK OR DATA SHEET

SINGLE-CHIP 8-BIT CMOS MICROCONTROLLER

DESCRIPTION

The PC80CXX family of single-chip 8-bit CMOS microcontrollers consists of:

- The PCB80C48 and PCB80C49 with resident mask programmed ROM.
- The PCB80C35 and PCB80C39 without resident program memory for use with external EPROM/ROM.

All versions are pin and function compatible to their NMOS counter parts but with additional features and high performance.

The PC80CXX family are designed to be efficient control processors as well as arithmetic processors. Their instruction set allows the user to directly set and reset individual I/O lines as well as test individual bits within the accumulator. A large variety of branch and table look-up instructions enable efficient implementation of standard logic functions. Code efficiency is high; over 70% of the instructions are single byte; all others are two byte.

An on-chip 8-bit counter is provided, which can count either machine cycles (÷ 32) or external events. The counter can be programmed to cause an interrupt to the processor.
Program and data memories can be expanded using standard devices. Input/output capabilities can be expanded using standard devices.
The family has low power consumption and in addition a power-save is provided.

FEATURES

- 8-bit CPU, ROM, RAM, I/O in a single 40-pin package
- PCB80C48: 1K x 8 ROM, 64 x 8 RAM
- PCB80C49: 2K x 8 ROM, 128 x 8 RAM
- Internal counter/timer
- Internal oscillator, clock driver
- Single-level interrupts: external and counter/timer
- 17 internal registers: accumulator, 16 addressable registers
- Over 90 instructions: 70% single byte
- All instructions: 1 or 2 cycles
- Easily expandable memory and I/O
- TTL compatible inputs and outputs
- Single 5 V supply
- Wide frequency operating range
- Low current consumption

APPLICATIONS

- Peripheral interfaces and controllers
- Test and measurement instruments
- Sequencers
- Audio/video systems
- Environmental control systems
- Modems and data enciphering

PACKAGE OUTLINES

PCB80C35/C39/C48/C49P: 40-lead DIL; plastic (SOT-129).
PCB80C35/C39/C48/C49WP: 44-lead plastic leaded-chip-carrier (PLCC); SOT-187.

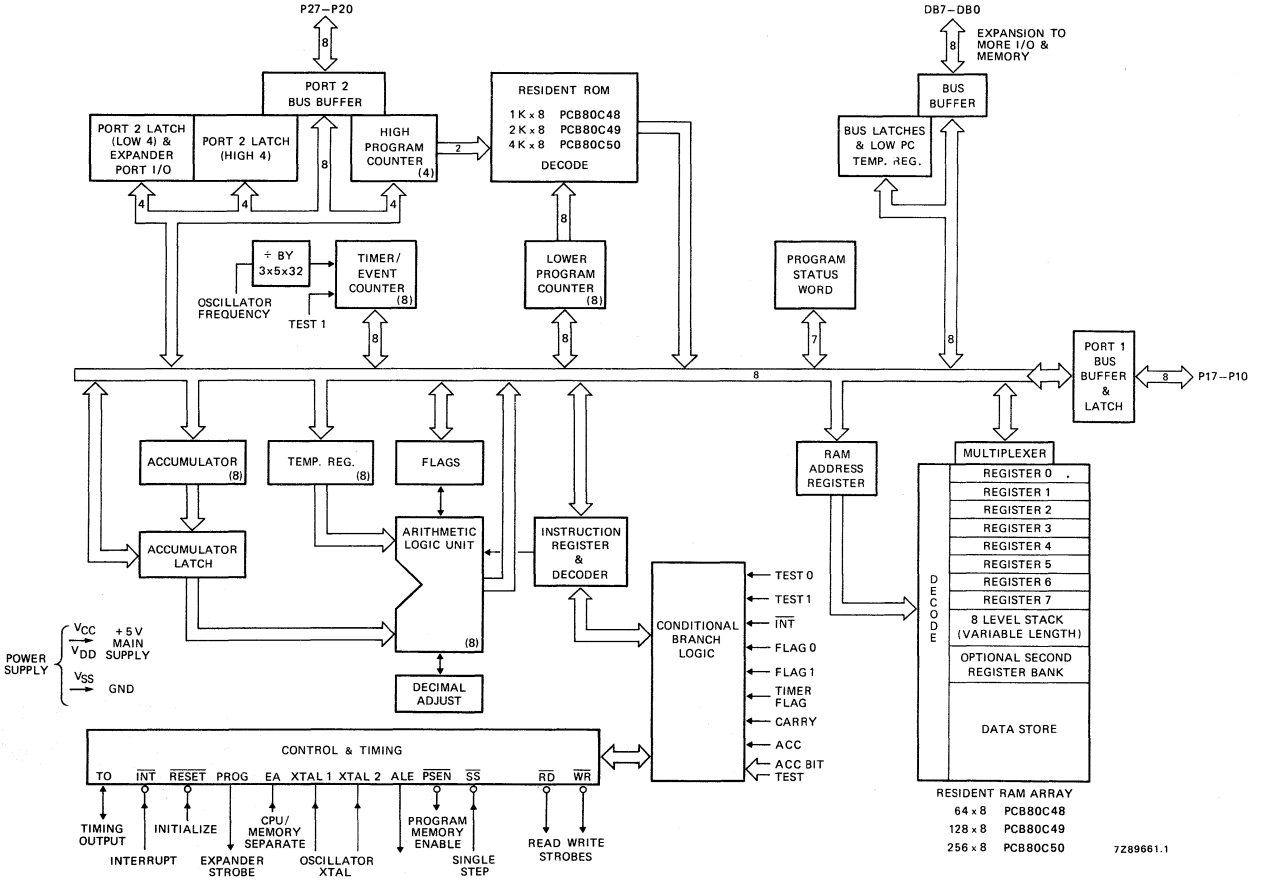


Fig. 1 Block diagram.

LCD DUPLEX DRIVER

GENERAL DESCRIPTION

The PCF2100 is a single chip, silicon gate CMOS circuit designed to drive an LCD (Liquid Crystal Display) with up to 40 segments in a duplex manner; specially for low voltage applications. A three-line bus structure enables serial data transfer with microcontrollers. All inputs are CMOS/NMOS compatible.

Features

- 40 LCD-segment drive capability
- Supply voltage 2,25 to 6,5 V
- Low current consumption
- Serial data input
- CBUS control
- One-point built-in oscillator
- Expansion possibility

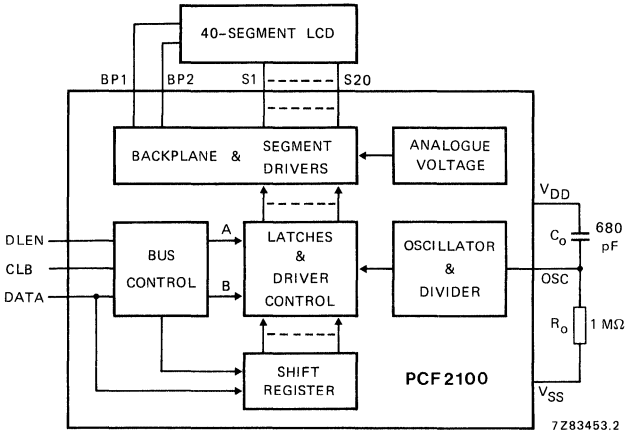


Fig. 1 Block diagram.

PACKAGE OUTLINES

PCF2100P: 28-lead DIL; plastic (SOT-117D).
PCF2100T: 28-lead mini-pack; plastic (SO-28; SOT-136A).

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage with respect to V_{SS}	V_{DD}		−0,3 to 8 V
Voltage on any pin	V_n	V_{SS}	−0,3 to V_{DD} + 0,3 V
Operating ambient temperature range	T_{amb}		−40 to + 85 °C
Storage temperature range	T_{stg}		−55 to + 125 °C

HANDLING

Inputs and outputs are protected against electrostatic charge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see 'Handling MOS devices').

CHARACTERISTICS

V_{DD} = 2,25 to 6,5 V; V_{SS} = 0 V; T_{amb} = −40 to + 85 °C; R_o = 1 MΩ; C_o = 680 pF; unless otherwise specified

parameter	condition	symbol	min.	typ.	max.	unit
Supply current	no external load	I_{DD}	–	10	50	μA
Supply current	no external load; T_{amb} = −25 to + 85 °C	I_{DD}	–	–	30	μA
Display frequency	see Fig. 8; T = 680 μs	f_{LCD}	60	80	100	Hz
D.C. component of LCD drive	with respect to V_{SX}	V_{BP}	–	± 10 [1]	–	mV
Load on each segment driver			–	–	10	MΩ
			–	–	500	pF
Load on each backplane driver			–	–	1	MΩ
			–	–	5	nF
Input voltage HIGH	see Fig. 9	V_{IH}	2	–	–	V
Input voltage LOW	see Fig. 9	V_{IL}	–	–	0,6	V
Rise time V_{BP} to V_{SX}	max. load	t_r	–	20	–	μs
Inputs CLB, DATA, DLEN	see note on next page					
Rise and fall times	see Fig. 2	t_r, t_f	–	–	10	μs
CLB pulse width HIGH	see Fig. 2	t_{WH}	1	–	–	μs
CLB pulse width LOW	see Fig. 2	t_{WL}	9	–	–	μs

CHARACTERISTICS (continued)

parameter	condition	symbol	min.	typ.	max.	unit
Data set-up time DATA → CLB	see Fig. 2	t_{SUDA}	8	–	–	μs
Data hold time DATA → CLB	see Fig. 2	t_{HDDA}	8	–	–	μs
Enable set-up time DLEN → CLB	see Fig. 2	t_{SUEN}	1	–	–	μs
Disable set-up time CLB → DLEN	see Fig. 2	t_{SUDI}	8	–	–	μs
Set-up time (load pulse) DLEN → CLB	see Fig. 2	t_{SULD}	8	–	–	μs
Busy-time from load pulse to next start of transmission	see Fig. 2	t_{BUSY}	8	–	–	μs
Set-up time (leading zero) DATA → CLB	see Fig. 2	t_{SULZ}	8	–	–	μs

Note

All timing values are referred to $V_{IH\,min}$ and $V_{IL\,max}$* (see Fig. 2). If external resistors are used in the bus lines (see Fig. 9), the extra time constant has to be added.

* With an input voltage swing of V_{ILmax} – 0,1 V to V_{IHmin} + 0,1 V.

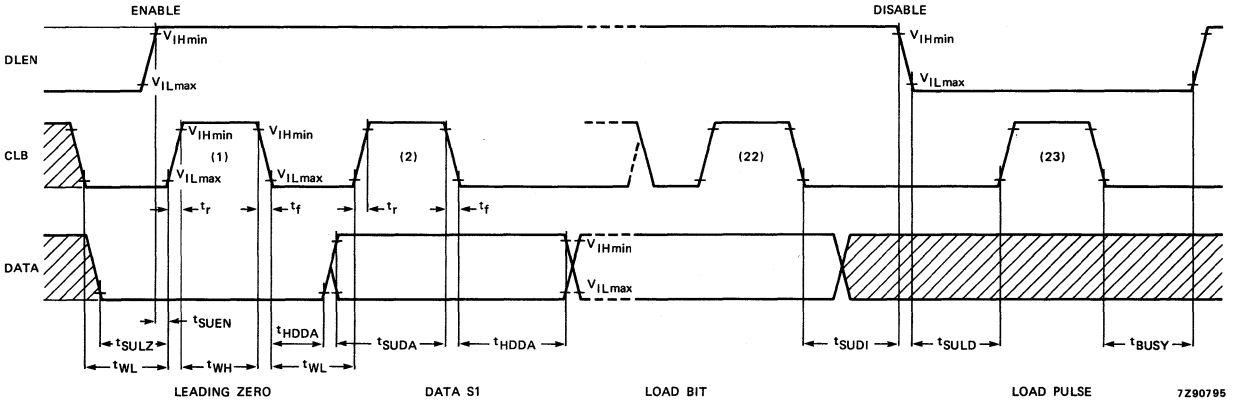


Fig. 2 CBUS timing.

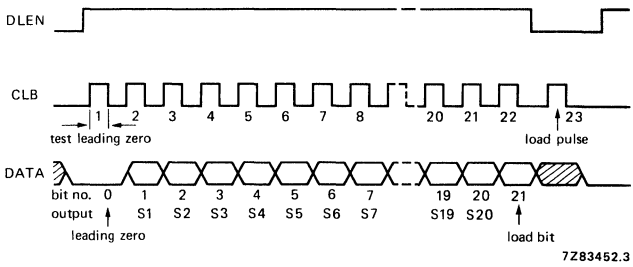


Fig. 3 CBUS data format.

Notes to Fig. 3

An LCD segment is activated when the corresponding DATA-bit is HIGH.

When DATA-bit 21 is HIGH, the A-latches (BP1) are loaded. With DATA-bit 21 LOW, the B-latches (BP2) are loaded.
CLB-pulse 23 transfers data from shift register to selected latches.

The following tests are carried out by the bus control logic:

a. Test on leading zero.
b. Test on number of DATA-bits.
c. Test of disturbed DLEN and DATA signals during transmission.

If one of the test conditions is not fulfilled, no action follows the load conditions (load pulse width DLEN is LOW) and the driver is ready to receive new data.

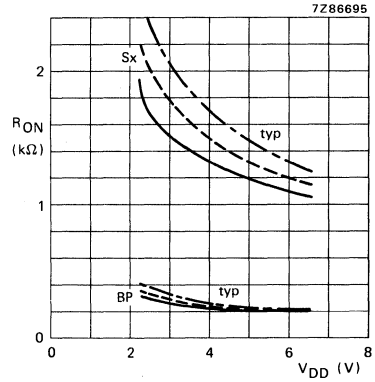


Fig. 4 Output resistance of backplane and segments.
——— T_{amb} = –40 °C; – – – T_{amb} = + 25 °C; – · – · T_{amb} = +85 °C.

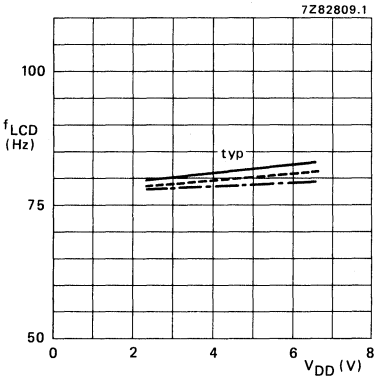


Fig. 5 Display frequency as a function of supply voltage; R_oC_o = 680 μs.
——— T_{amb} = –40 °C; – – – T_{amb} = + 25 °C; – · – · T_{amb} = +85 °C.

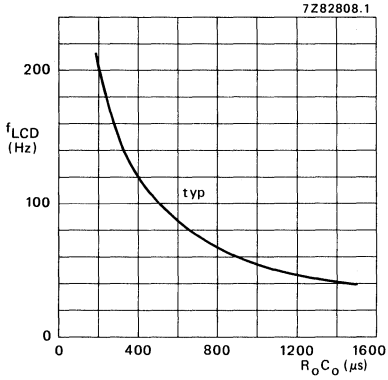


Fig. 6 Display frequency as a function of R_o x C_o time; T_{amb} = 25 °C.

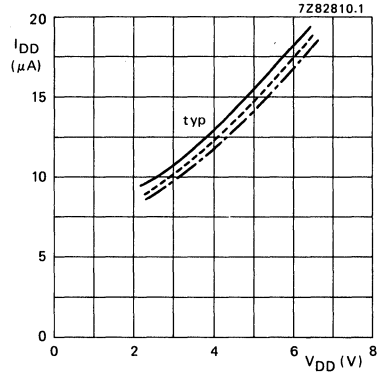


Fig. 7 Supply current as a function of supply voltage.
——— T_{amb} = –40 °C; – – – T_{amb} = + 25 °C; – · – · T_{amb} = +85 °C.

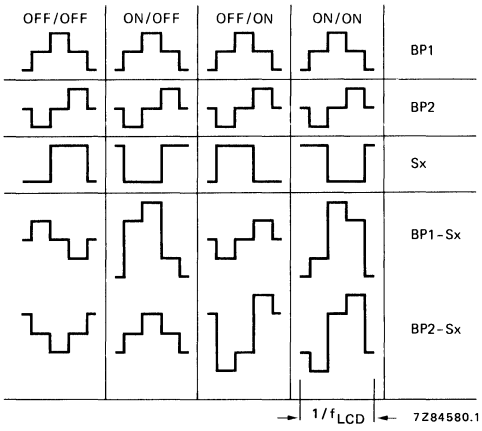


Fig. 8 Timing diagram.

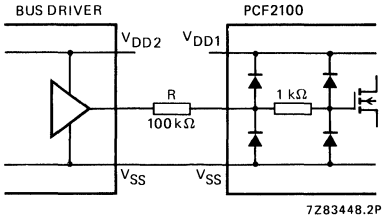
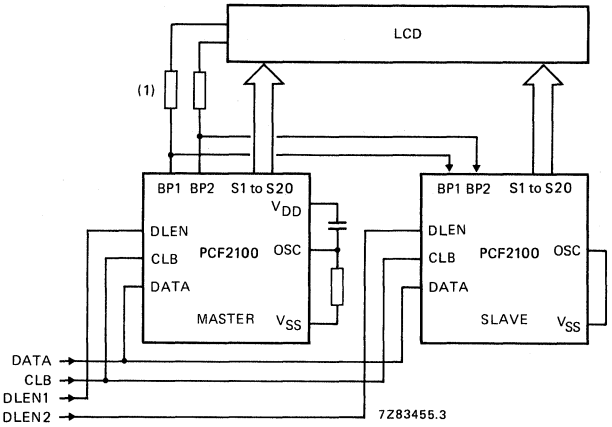


Fig. 9 Input circuitry.

Note to Fig. 9

V_{SS} line is common. In systems where it is expected that $V_{DD2} > V_{DD1} + 0{,}5$ V, a resistor should be inserted to reduce the current flowing through the input protection.
Maximum input current $\leqslant 40\ \mu A$.



(1) In the slave mode, the serial resistors between BP1 and BP2 of the PCF2100 and the backplane of the LCD must be $> 2{,}7$ kΩ. In most applications the resistance of the interconnection to the LCD already has a higher value.

Fig. 10 Diagram showing expansion possibility.

Note to Fig. 10

By connecting OSC to V_{SS} the BP-pins become inputs and generate signals synchronized to the single oscillator frequency, thus allowing expansion of several PCF2111, PCF2110 and PCF2100 ICs up to the BP drive capability of the master.

PCF2111 is a 64 LCD-segment driver.
PCF2110 is a 60 LCD-segment driver plus 2 LED driver outputs.

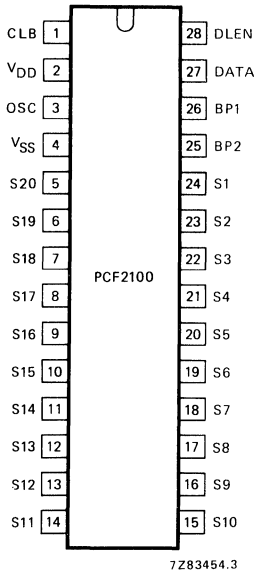


Fig. 11 Pinning diagram.

PINNING

Supply

2	V_{DD}	Positive supply
4	V_{SS}	Negative supply

Inputs

3	OSC	Oscillator input	
27	DATA	Data line	CBUS
28	DLEN	Data line enable	CBUS
1	CLB	Clock burst	CBUS

Outputs

26	BP1	Backplane drivers (common of LCD)
25	BP2	Backplane drivers (common of LCD)
S1 to S20		LCD driver outputs

LCD DUPLEX DRIVER

GENERAL DESCRIPTION

The PCF2110 is a single chip, silicon gate CMOS circuit designed to drive 2 LEDs (Light Emitting Diodes) and an LCD (Liquid Crystal Display) with up to 60 segments in a duplex manner; specially for low voltage applications. A three-line bus structure enables serial data transfer with microcontrollers. All inputs are CMOS/NMOS compatible.

Features

- 60 LCD-segment drive capability
- Two LED-driver outputs
- Supply voltage 2,25 to 6,5 V
- Low current consumption
- Serial data input
- CBUS control
- One-point built-in oscillator
- Expansion possibility

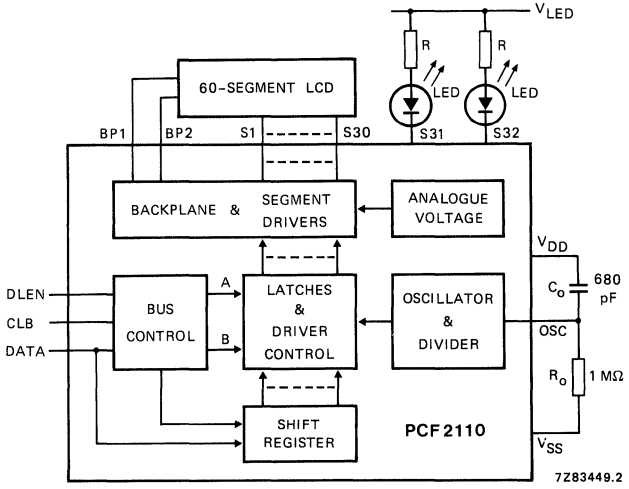


Fig. 1 Block diagram.

PACKAGE OUTLINES

PCF2110P: 40-lead DIL; plastic (SOT-129).
PCF2110T: 40-lead mini-pack; plastic (VSO-40; SOT-158A).

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage with respect to V_{SS}	V_{DD}		−0,3 to 8 V
Voltage on any pin	V_n	V_{SS}	−0,3 to V_{DD} + 0,3 V
Operating ambient temperature range	T_{amb}		−40 to + 85 °C
Storage temperature range	T_{stg}		−55 to + 125 °C

HANDLING

Inputs and outputs are protected against electrostatic charge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see 'Handling MOS devices').

CHARACTERISTICS

V_{DD} = 2,25 to 6,5 V; V_{SS} = 0 V; T_{amb} = −40 to + 85 °C; R_o = 1 MΩ; C_o = 680 pF; unless otherwise specified

parameter	condition	symbol	min.	typ.	max.	unit
Supply current	no external load	I_{DD}	–	10	50	μA
Supply current	no external load; T_{amb} = −25 to + 85 °C	I_{DD}	–	–	30	μA
Display frequency	see Fig. 9; T = 680 μs	f_{LCD}	60	80	100	Hz
D.C. component of LCD drive	with respect to V_{SX}	V_{BP}	–	± 10	–	mV
Load on each segment driver			–	–	10	MΩ
			–	–	500	pF
Load on each backplane driver			–	–	1	MΩ
			–	–	5	nF
Input voltage HIGH	see Fig. 10	V_{IH}	2	–	–	V
Input voltage LOW	see Fig. 10	V_{IL}	–	–	0,6	V
Rise time V_{BP} to V_{SX}	max. load	t_r	–	20	–	μs
LED outputs S31, S32	V_{DD} = 3 V; T_{amb} = 25 °C					
Output resistance	V_{OL} = 0,2 V; see Fig. 4	R_{out}	–	–	25	Ω
Drain voltage	N-channel OFF	V_{LED}	–	–	8	V
Drain current	maximum value	I_{LEDmax}	–	–	50	mA
Total power dissipation		P_{tot}	–	–	400	mW
Inputs CLB, DATA, DLEN	see note on next page					
Input capacitance	for SOT-129 package	C_{IN}	–	–	10	pF
	for SOT-158A package	C_{IN}	–	–	5	pF
Rise and fall times	see Fig. 2	t_r, t_f	–	–	10	μs
CLB pulse width HIGH	see Fig. 2	t_{WH}	1	–	–	μs
CLB pulse width LOW	see Fig. 2	t_{WL}	9	–	–	μs

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Data set-up time DATA → CLB	see Fig. 2	t_{SUDA}	8	–	–	μs
Data hold time DATA → CLB	see Fig. 2	t_{HDDA}	8	–	–	μs
Enable set-up time DLEN → CLB	see Fig. 2	t_{SUEN}	1	–	–	μs
Disable set-up time CLB → DLEN	see Fig. 2	t_{SUDI}	8	–	–	μs
Set-up time (load pulse) DLEN → CLB	see Fig. 2	t_{SULD}	8	–	–	μs
Busy-time from load pulse to next start of transmission	see Fig. 2	t_{BUSY}	8	–	–	μs
Set-up time (leading zero) DATA → CLB	see Fig. 2	t_{SULZ}	8	–	–	μs

Note

All timing values are referred to $V_{IH\,min}$ and $V_{IL\,max}$*(see Fig. 2). If external resistors are used in the bus lines (see Fig. 10), the extra time constant has to be added.

* With an input voltage swing of $V_{IL\,max}$–0,1 V to V_{IHmin} + 0,1 V.

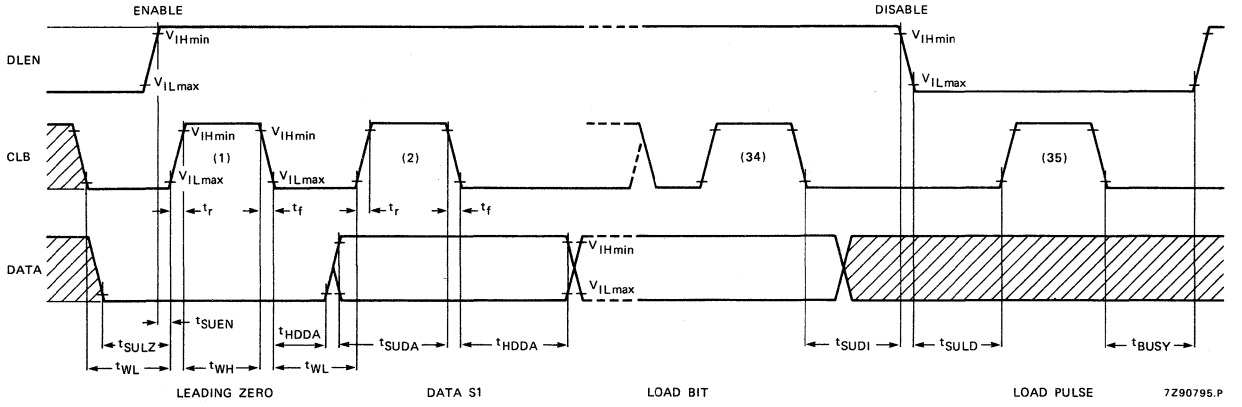


Fig. 2 CBUS timing.

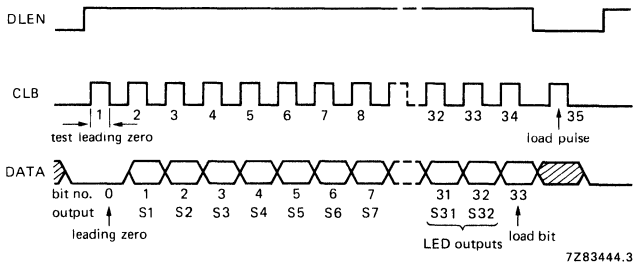


Fig. 3 CBUS data format.

Notes to Fig. 3

An LCD segment is activated when the corresponding DATA-bit is HIGH.

When DATA-bit 33 is HIGH, the A-latches (BP1) are loaded. Bits 31 and 32 contain the LED output information. With DATA-bit 33 LOW, the B-latches (BP2) are loaded and bits 31 and 32 are ignored. CLB-pulse 35 transfers data from shift register to selected latches.

The following tests are carried out by the bus control logic:

a. Test on leading zero.
b. Test on number of DATA-bits.
c. Test of disturbed DLEN and DATA signals during transmission.

If one of the test conditions is not fulfilled, no action follows the load condition (load pulse with DLEN is LOW) and the driver is ready to receive new data.

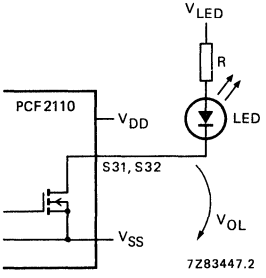


Fig. 4 LED driver circuitry.

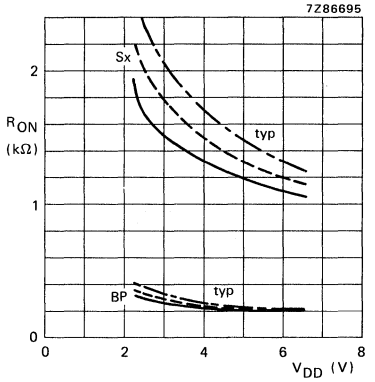


Fig. 5 Output resistance of backplane and segments.
——— T_{amb} = –40 °C; – – – T_{amb} = + 25 °C; – · – · T_{amb} = +85 °C.

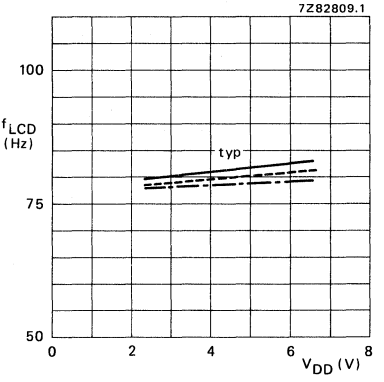


Fig. 6 Display frequency as a function of supply voltage; R_oC_o = 680 μs.
——— T_{amb} = –40 °C; – – – T_{amb} = + 25 °C; – · – · T_{amb} = +85 °C.

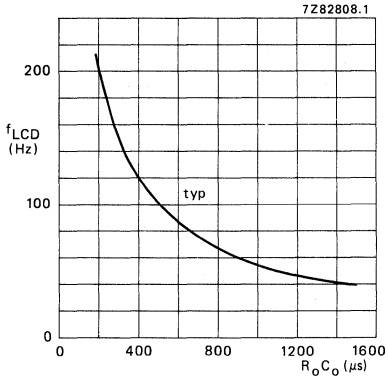


Fig. 7 Display frequency as a function of R_o x C_o time; T_{amb} = 25 °C.

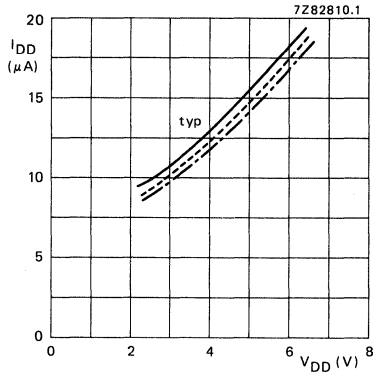


Fig. 8 Supply current as a function of supply voltage.
——— T_{amb} = –40 °C; – – – T_{amb} = + 25 °C; – · – · T_{amb} = +85 °C.

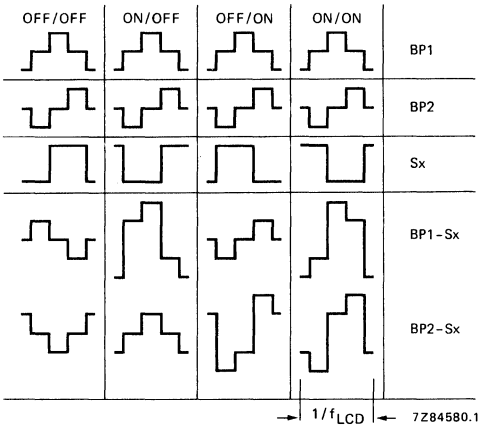


Fig. 9 Timing diagram.

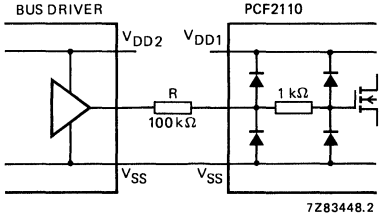
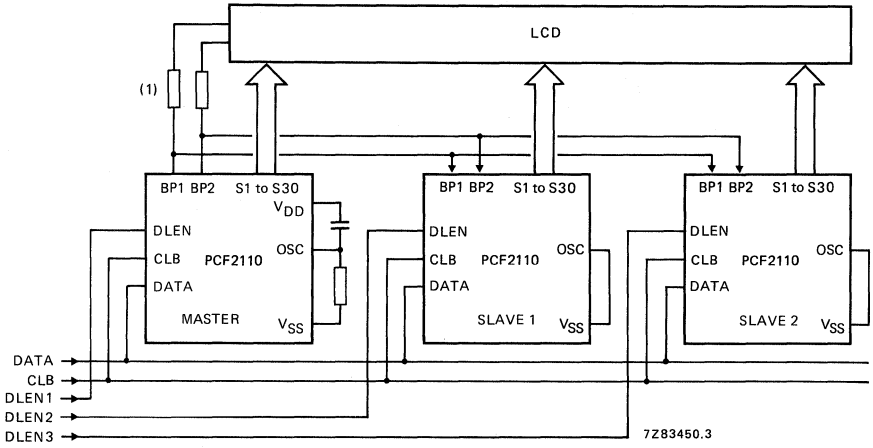


Fig. 10 Input circuitry.

Note to Fig. 10

V_{SS} line is common. In systems where it is expected that $V_{DD2} > V_{DD1} + 0{,}5$ V, a resistor should be inserted to reduce the current flowing through the input protection.
Maximum input current $\leqslant 40\ \mu A$.



(1) In the slave mode, the serial resistors between BP1 and BP2 of the PCF2110 and the backplane of the LCD must be $> 2{,}7\ k\Omega$. In most applications the resistance of the interconnection to the LCD already has a higher value.

Fig. 11 Diagram showing expansion possibility.

Note to Fig. 11

By connecting OSC to V_{SS} the BP-pins become inputs and generate signals synchronized to the single oscillator frequency, thus allowing expansion of several PCF2100, PCF2110 and PCF2111 ICs up to the BP drive capability of the master.

PCF2100 is a 40 LCD-segment driver.
PCF2111 is a 64 LCD-segment driver.

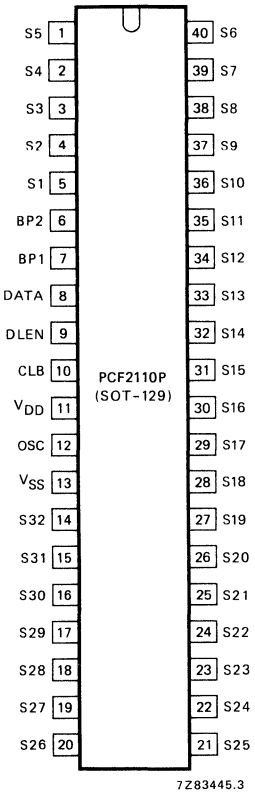


Fig. 12 Pinning diagram for SOT-129 package.

PINNING

Supply

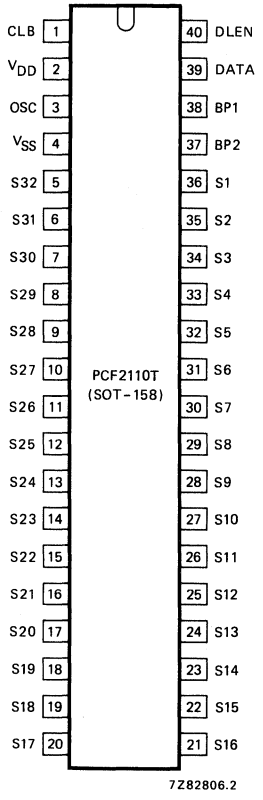
11	V_{DD}	Positive supply
13	V_{SS}	Negative supply

Inputs

12	OSC	Oscillator input	
8	DATA	Data line	CBUS
9	DLEN	Data line enable	CBUS
10	CLB	Clock burst	CBUS

Outputs

7	BP1	Backplane drivers (common of LCD)
6	BP2	Backplane drivers (common of LCD)
S1 to S30		LCD driver outputs
S31, S32		LED driver outputs



PINNING

Supply

2	V_{DD}	Positive supply
4	V_{SS}	Negative supply

Inputs

3	OSC	Oscillator input	
39	DATA	Data line	CBUS
40	DLEN	Data line enable	CBUS
1	CLB	Clock burst	CBUS

Outputs

38	BP1	Backplane drivers (common of LCD)
37	BP2	Backplane drivers (common of LCD)
S1 to S30		LCD driver outputs
S31, S32		LED driver outputs

Fig. 13 Pinning diagram for VSO-40; SOT-158A package.

LCD DUPLEX DRIVER

GENERAL DESCRIPTION

The PCF2111 is a single chip, silicon gate CMOS circuit designed to drive an LCD (Liquid Crystal Display) with up to 64 segments in a duplex manner; specially for low voltage applications. A three-line bus structure enables serial data transfer with microcontrollers. All inputs are CMOS/NMOS compatible.

Features

- 64 LCD-segment drive capability
- Supply voltage 2,25 to 6,5 V
- Low current consumption
- Serial data input
- CBUS control
- One-point built-in oscillator
- Expansion possiblity

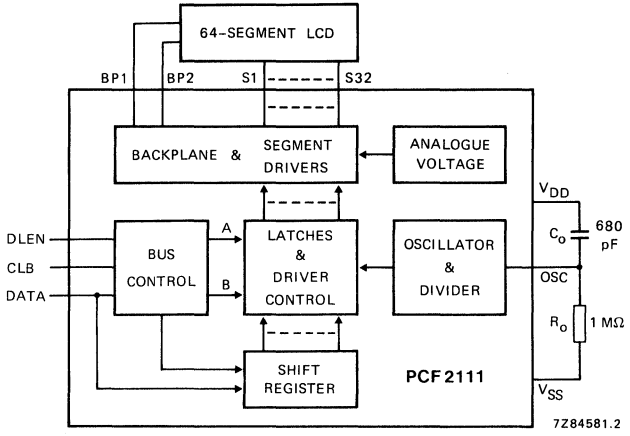


Fig. 1 Block diagram.

PACKAGE OUTLINES

PCF2111P: 40-lead DIL; plastic (SOT-129).
PCF2111T: 40-lead mini-pack; plastic (VSO-40; SOT-158A).

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage with respect to V_{SS}	V_{DD}		−0,3 to 8 V
Voltage on any pin	V_n	V_{SS}	−0,3 to V_{DD} + 0,3 V
Operating ambient temperature range	T_{amb}		−40 to + 85 °C
Storage temperature range	T_{stg}		−55 to + 125 °C

HANDLING

Inputs and outputs are protected against electrostatic charge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see 'Handling MOS devices').

CHARACTERISTICS

V_{DD} = 2,25 to 6,5 V; V_{SS} = 0 V; T_{amb} = −40 to + 85 °C; R_o = 1 MΩ; C_o = 680 pF; unless otherwise specified

parameter	condition	symbol	min.	typ.	max.	unit
Supply current	no external load	I_{DD}	—	10	50	μA
Supply current	no external load; T_{amb} = −25 to + 85 °C	I_{DD}	–	–	30	μA
Display frequency	see Fig. 8; T = 680 μs	f_{LCD}	60	80	100	Hz
D.C. component of LCD drive	with respect to V_{SX}	V_{BP}	–	± 10	–	mV
Load on each segment driver			–	–	10	MΩ
			–	–	500	pF
Load on each backplane driver			–	–	1	MΩ
			–	–	5	nF
Input voltage HIGH	see Fig. 9	V_{IH}	2	–	–	V
Input voltage LOW	see Fig. 9	V_{IL}	–	–	0,6	V
Rise time V_{BP} to V_{SX}	max. load	t_r	–	20	–	μs
Inputs CLB, DATA, DLEN	see note on next page					
Input capacitance	for SOT-129 package	C_{IN}	–	–	10	pF
	for SOT-158A package	C_{IN}	–	–	5	pF
Rise and fall times	see Fig. 2	t_r, t_f	–	–	10	μs
CLB pulse width HIGH	see Fig. 2	t_{WH}	1	–	–	μs
CLB pulse width LOW	see Fig. 2	t_{WL}	9	–	–	μs

CHARACTERISTICS (continued)

parameter	condition	symbol	min.	typ.	max.	unit
Data set-up time DATA → CLB	see Fig. 2	t_{SUDA}	8	–	–	μs
Data hold time DATA → CLB	see Fig. 2	t_{HDDA}	8	–	–	μs
Enable set-up time DLEN → CLB	see Fig. 2	t_{SUEN}	1	–	–	μs
Disable set-up time CLB → DLEN	see Fig. 2	t_{SUDI}	8	–	–	μs
Set-up time (load pulse) DLEN → CLB	see Fig. 2	t_{SULD}	8	–	–	μs
Busy-time from load pulse to next start of transmission	see Fig. 2	t_{BUSY}	8	–	–	μs
Set-up time (leading zero) DATA → CLB	see Fig. 2	t_{SULZ}	8	–	–	μs

Note

All timing values are referred to $V_{IH\ min}$ and $V_{IL\ max}$* (see Fig. 2). If external resistors are used in the bus lines (see Fig. 9), the extra time constant has to be added.

* With an input voltage swing of $V_{IL\ max}$–0,1 V to V_{IHmin} + 0,1 V.

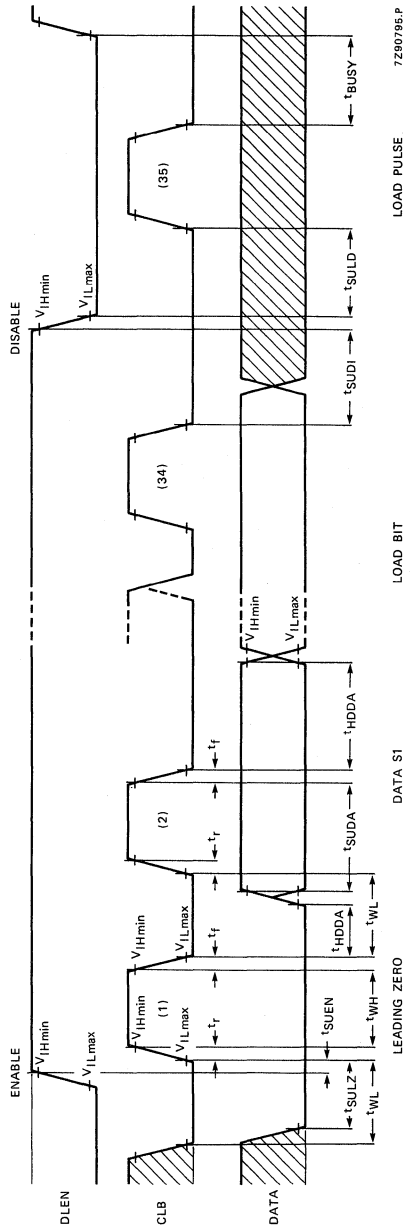


Fig. 2 CBUS timing.

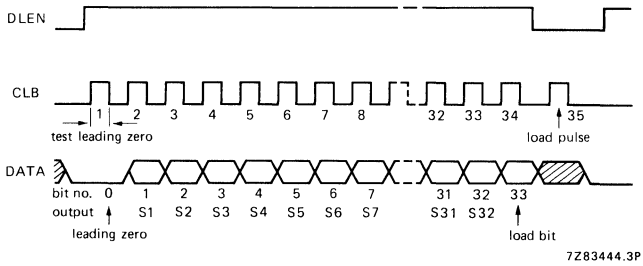


Fig. 3 CBUS data format.

Notes to Fig. 3

An LCD segment is activated when the corresponding DATA-bit is HIGH.
When DATA-bit 33 is HIGH, the A-latches (BP1) are loaded. With DATA-bit 33 LOW, the B-latches (BP2) are loaded. CLB-pulse 35 transfers data from shift register to selected latches.

The following tests are carried out by the bus control logic:

a. Test on leading zero.
b. Test on number of DATA-bits.
c. Test of disturbed DLEN and DATA signals during transmission.

If one of the test conditions is not fulfilled, no action follows the load condition (load pulse with DLEN is LOW) and the driver is ready to receive new data.

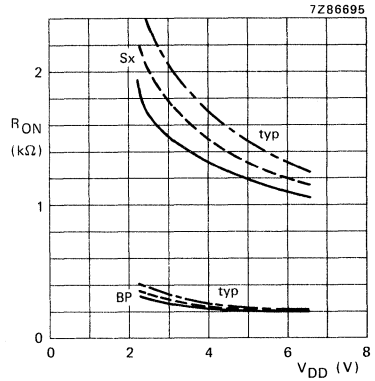


Fig. 4 Output resistance of backplane and segments.
——— T_{amb} = −40 °C; − − − T_{amb} = + 25 °C; — · — · T_{amb} = + 85 °C.

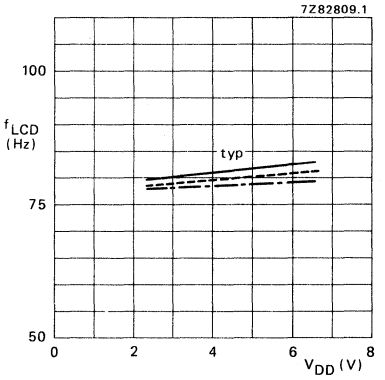


Fig. 5 Display frequency as a function of supply voltage; R_oC_o = 680 μs.
——— T_{amb} = −40 °C; − − − T_{amb} = + 25 °C; — · — · T_{amb} = + 85 °C.

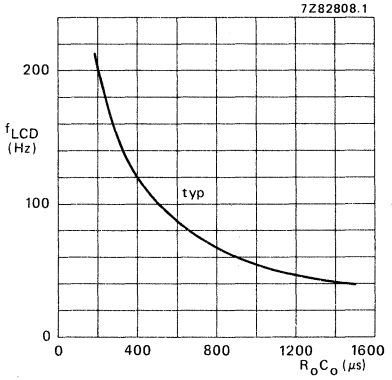


Fig. 6 Display frequency as a function of R_o x C_o time; T_{amb} = 25 °C.

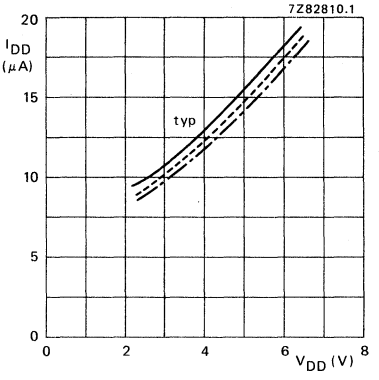


Fig. 7 Supply current as a function of supply voltage.
——— T_{amb} = −40 °C; − − − T_{amb} = + 25 °C; — · — · T_{amb} = + 85 °C.

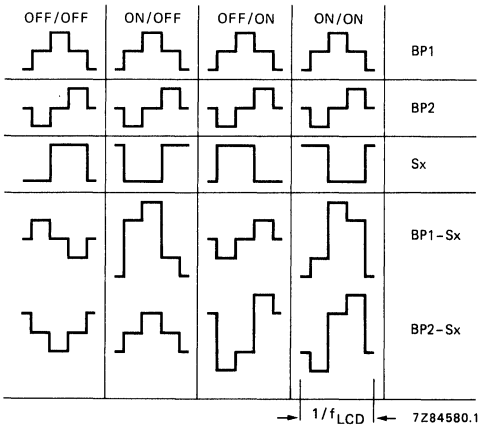


Fig. 8 Timing diagram.

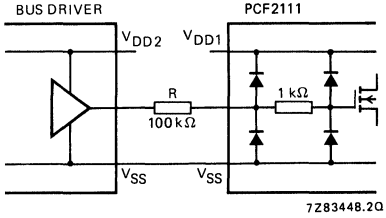
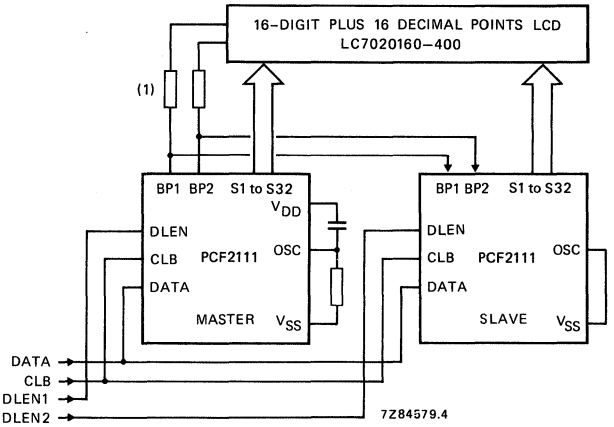


Fig. 9 Input circuitry.

Note to Fig. 9

V_{SS} line is common. In systems where it is expected that $V_{DD2} > V_{DD1} + 0{,}5$ V, a resistor should be inserted to reduce the current flowing through the input protection.
Maximum input current $\leqslant 40\ \mu A$.



(1) In the slave mode, the serial resistors between BP1 and BP2 of the PCF2111 and the backplane of the LCD must be $> 2{,}7\ k\Omega$. In most applications the resistance of the interconnection to the LCD already has a higher value.

Fig. 10 Diagram showing expansion possibility for a 16-digit plus 16 decimal points LCD.

Note to Fig. 10

By connecting OSC to V_{SS} the BP-pins become inputs and generate signals synchronized to the single oscillator frequency, thus allowing expansion of several PCF2111, PCF2110 and PCF2100 ICs up to the BP drive capability of the master.

PCF2100 is a 40 LCD-segment driver; PCF2110 is a 60 LCD-segment driver plus 2 LED driver outputs.

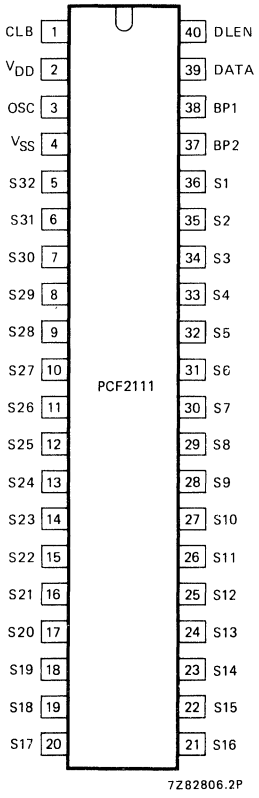


Fig. 11 Pinning diagram.

PINNING

Supply

2	V_{DD}	Positive supply
4	V_{SS}	Negative supply

Inputs

3	OSC	Oscillator input	
39	DATA	Data line	CBUS
40	DLEN	Data line enable	CBUS
1	CLB	Clock burst	CBUS

Outputs

38	BP1	Backplane drivers (common of LCD)
37	BP2	Backplane drivers (common of LCD)
S1 to S32		LCD driver outputs

LCD DRIVER

GENERAL DESCRIPTION

The PCF2112 is a single chip, silicon gate CMOS circuit designed to drive an LCD (Liquid Crystal Display) with up to 32 segments in direct drive; specially for low voltage applications. A three-line bus structure enables serial data transfer with microcontrollers. All inputs are CMOS/NMOS compatible.

Features

- 32 LCD-segment drive capability.
- Supply voltage 2,25 to 6,5 V.
- Low current consumption.
- Serial data input.
- CBUS control.
- One-point built-in oscillator.
- Expansion possibility.

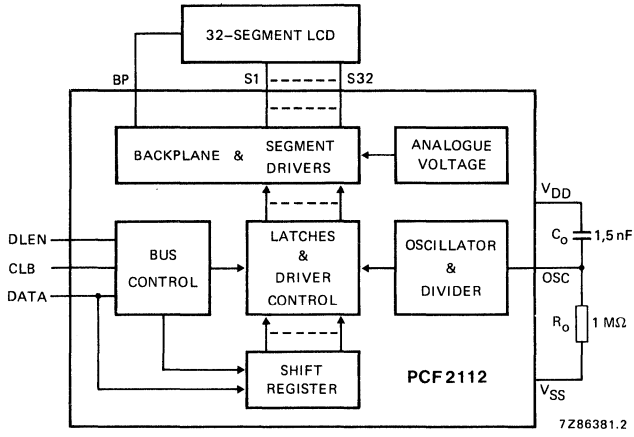


Fig. 1 Block diagram.

PACKAGE OUTLINES

PCF2112P: 40-lead DIL; plastic (SOT-129).
PCF2112T: 40-lead mini-pack; plastic (VSO-40; SOT-158A).

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage with respect to V_{SS}	V_{DD}	−0,3 to 8 V
Voltage on any pin	V_n	V_{SS}−0,3 to V_{DD} + 0,3 V
Operating ambient temperature range	T_{amb}	−40 to + 85 °C
Storage temperature range	T_{stg}	−55 to + 125 °C

HANDLING

Inputs and outputs are protected against electrostatic charge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see 'Handling MOS devices').

CHARACTERISTICS

V_{DD} = 2,25 to 6,5 V; V_{SS} = 0 V; T_{amb} = −40 to + 85 °C; R_o = 1 MΩ; C_o = 1,5 nF; unless otherwise specified.

parameter	condition	symbol	min.	typ.	max.	unit
Supply current	no external load	I_{DD}	–	10	50	μA
→ Supply current	no external load; T_{amb} = −25 to +85 °C	I_{DD}	–	–	30	μA
Display frequency	T = 1,5 ms	f_{LCD}	30	40	50	Hz
Output resistance of each segment	I_o = 10 μA	R_s	–	–	10	kΩ
Output resistance of backplane	I_o = 10 μA	R_{BP}	–	–	2	kΩ
Input voltage HIGH	see Fig. 8	V_{IH}	2	–	–	V
Input voltage LOW	see Fig. 8	V_{IL}	–	–	0,6	V
Inputs CLB,DATA,DLEN	see note on next page					
Input capacitance	for SOT-129 package	C_{IN}	–	–	10	pF
	for SOT-158A package	C_{IN}	–	–	5	pF
Rise and fall times	see Fig. 2	t_r, t_f	–	–	10	μs
CLB pulse width HIGH	see Fig. 2	t_{WH}	1	–	–	μs
CLB pulse width LOW	see Fig. 2	t_{WL}	9	–	–	μs

CHARACTERISTICS (continued)

parameter	condition	symbol	min.	typ.	max.	unit
Data set-up time DATA → CLB	see Fig. 2	t_{SUDA}	8	–	–	μs
Data hold time DATA → CLB	see Fig. 2	t_{HDDA}	8	–	–	μs
Enable set-up time DLEN → CLB	see Fig. 2	t_{SUEN}	1	–	–	μs
Disable set-up time CLB → DLEN	see Fig. 2	t_{SUDI}	8	–	–	μs
Set-up time (load pulse) DLEN → CLB	see Fig. 2	t_{SULD}	8	–	–	μs
Busy-time from load pulse to next start of transmission	see Fig. 2	t_{BUSY}	8	–	–	μs
Set-up time (leading zero) DATA → CLB	see Fig. 2	t_{SULZ}	8	–	–	μs

Note

All timing values are referred to V_{IHmin} and V_{ILmax}*(see Fig. 2). If external resistors are used in the bus lines (see Fig. 8), an extra time constant has to be added. ←

* With an input voltage swing of V_{ILmax}–0,1 V to V_{IHmin} + 0,1 V.

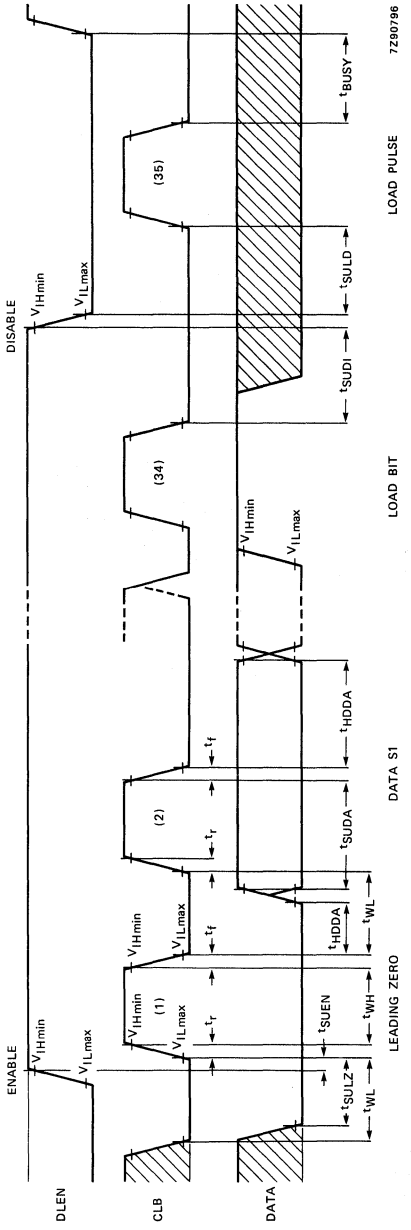


Fig. 2 CBUS timing.

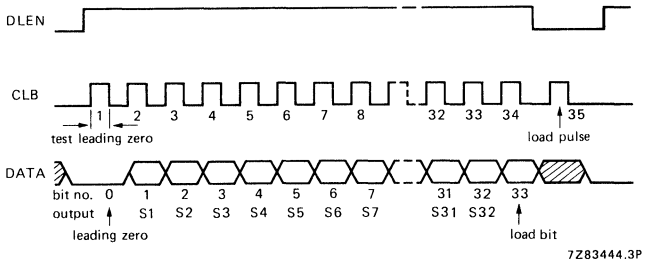


Fig. 3 Data format.

Notes to Fig. 3

An LCD segment is activated when the corresponding DATA-bit is HIGH.
When DATA-bit 33 is HIGH, the latches are loaded. CLB-pulse 35 transfers data from shift register to latches.

The following tests are carried out by the bus control logic:

a. Test on leading zero.
b. Test on number of DATA-bits.
c. Test of disturbed DLEN and DATA signals during transmission.

If one of the test conditions is not fulfilled, no action follows the load condition (load pulse with DLEN is LOW) and the driver is ready to receive new data.

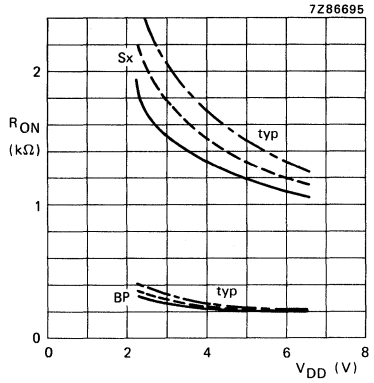


Fig. 4 Output resistance of backplane and segments.
——— T_{amb} = –40 °C; – – – T_{amb} = + 25 °C; – · – T_{amb} = + 85 °C.

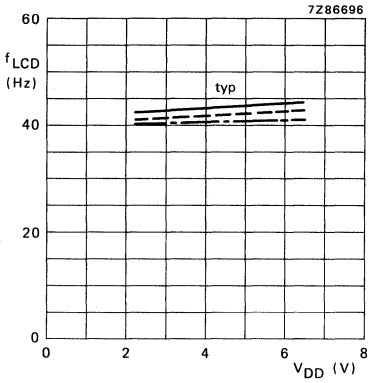


Fig. 5 Display frequency as a function of supply voltage; R_oC_o = 1,5 ms.
——— T_{amb} = –40 °C; – – – T_{amb} = + 25 °C; – · – T_{amb} = + 85 °C.

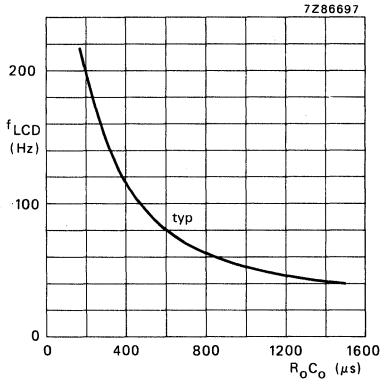


Fig. 6 Display frequency as a function of R_o x C_o time; T_{amb} = 25 °C.

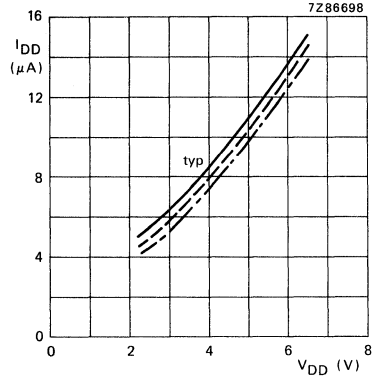


Fig. 7 Supply current as a function of supply voltage.
——— T_{amb} = –40 °C; – – – T_{amb} = + 25 °C; – · – T_{amb} = + 85 °C.

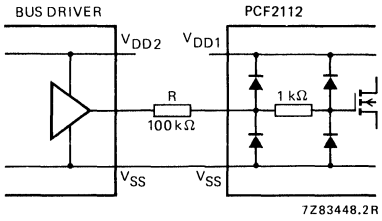
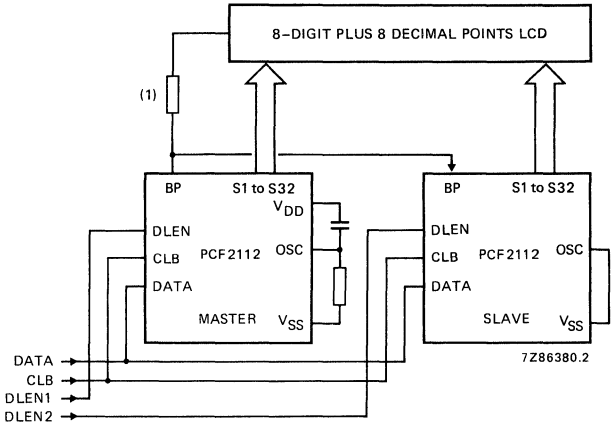


Fig. 8 Input circuitry.

Note to Fig. 8

V_{SS} line is common. In systems where it is expected that $V_{DD2} > V_{DD1} + 0{,}5$ V, a resistor should be inserted to reduce the current flowing through the input protection.
Maximum input current $\leqslant 40\ \mu A$.



(1) In the slave mode, the serial resistor between BP of the PCF2112 and the backplane of the LCD must be $> 2{,}7$ kΩ. In most applications the resistance of the interconnection to the LCD already has a higher value. ←

Fig. 9 Diagram showing expansion possibility for an 8-digit plus 8 decimal points LCD.

Note to Fig. 9

By connecting OSC to V_{SS} the BP-pin becomes input and generates signals synchronized to the single oscillator frequency, thus allowing expansion of several PCF2112 ICs up to the BP drive capability of the master.

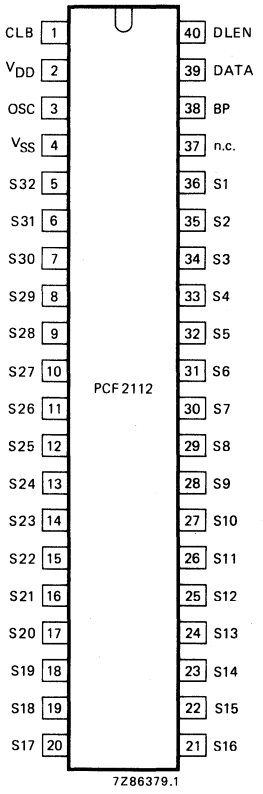


Fig. 10 Pinning diagram.

PINNING

Supply

2	V_{DD}	Positive supply
4	V_{SS}	Negative supply

Inputs

3	OSC	Oscillator input	
39	DATA	Data line	CBUS
40	DLEN	Data line enable	CBUS
1	CLB	Clock burst	CBUS

Outputs

38	BP	Back plane driver (common of LCD)
S1 to S32		LCD driver outputs
37	n.c.	not connected

CLOCK/CALENDAR WITH SERIAL I/O

GENERAL DESCRIPTION

The PCF8573 is a low threshold, monolithic CMOS circuit that functions as a real time clock/calendar in the Inter IC (I^2C) bus-oriented microcomputer systems. The device includes an addressable time counter and an addressable alarm register, both for minutes, hours, days and months. Three special control/status flags, COMP, POWF and NODA, are also available. Information is transferred serially via a two line bidirectional bus (I^2C). Back-up for the clock during supply interruptions is provided by a 1,2 V nickel cadmium battery. The time base is generated from a 32,768 kHz crystal-controlled oscillator.

Features

- Serial input/output bus (I^2C) interface for minutes, hours, days and months
- Additional pulse outputs for seconds and minutes
- Alarm register for presetting a time for alarm or remote switching functions
- Battery back-up for clock function during supply interruption
- Crystal oscillator control (32,768 kHz)

QUICK REFERENCE DATA

Supply voltage range (clock)	$V_{DD}-V_{SS1}$		1,1 to 6,0 V
Supply voltage range (I^2C interface)	$V_{DD}-V_{SS2}$		2,5 to 6,0 V
Crystal oscillator frequency	f_{osc}	typ.	32,768 kHz

PACKAGE OUTLINES

PCF8573P: 16-lead DIL; plastic (SOT-38).
PCF8573T: 16-lead mini-pack; plastic (SO-16L; SOT-162A).

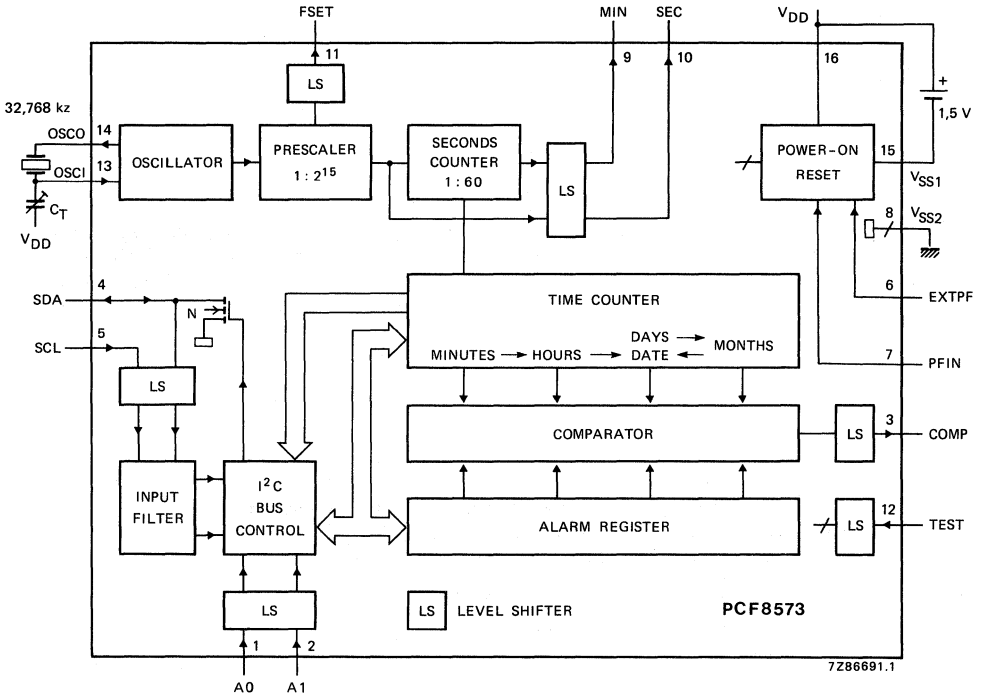


Fig. 1 Block diagram.

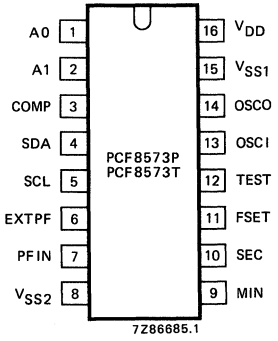


Fig. 2 Pinning diagram.

PINNING

1	A0	address input
2	A1	address input
3	COMP	comparator output
4	SDA	serial data line (I^2C bus)
5	SCL	serial clock line (I^2C bus)
6	EXTPF	enable power fail flag input
7	PFIN	power fail flag input
8	V_{SS2}	negative supply 2 (I^2C interface)
9	MIN	one pulse per minute output
10	SEC	one pulse per second output
11	FSET	oscillator tuning output
12	TEST	test input; must be connected to V_{SS2} when not in use
13	OSCI	oscillator input
14	OSCO	oscillator input/output
15	V_{SS1}	negative supply 1 (clock)
16	V_{DD}	common positive supply

FUNCTIONAL DESCRIPTION

Oscillator

The PCF8573 has an integrated crystal-controlled oscillator which provides the timebase for the prescaler. The frequency is determined by a single 32,768 kHz crystal connected between OSCI and OSCO. A trimmer is connected between OSCI and V_{DD}.

Prescaler and time counter

The prescaler provides a 128 Hz signal at the FSET output for fine adjustment of the crystal oscillator without loading it. The prescaler also generates a pulse once a second to advance the seconds counter. The carry of the prescaler and the seconds counter are available at the outputs SEC, MIN respectively, and are also readable via the I^2C bus. The mark-to-space ratio of both signals is 1 : 1. The time counter is advanced one count by the falling edge of output signal MIN. A transition from HIGH to LOW of output signal SEC triggers MIN to change state. The time counter counts minutes, hours, days and months, and provides a full calendar function which needs to be corrected once every four years. Cycle lengths are shown in Table 1.

Table 1 Cycle length of the time counter

unit	number of bits	counting cycle	carry for following unit	content of month counter
minutes	7	00 to 59	59 → 00	
hours	6	00 to 23	23 → 00	
days	6	01 to 28	28 → 01	2 (see note)
			or 29 → 01	
		01 to 30	30 → 01	4, 6, 9, 11
		01 to 31	31 → 01	1, 3, 5, 7, 8, 10, 12
months	5	01 to 12	12 → 01	

Note: Day counter may be set to 29 by a write transmission with EXECUTE ADDRESS.

Alarm register

The alarm register is a 24-bit memory. It stores the time-point for the next setting of the status flag COMP. Details of writing and reading of the alarm register are included in the description of the characteristics of the I^2C bus.

Comparator

The comparator compares the contents of the alarm register and the time counter, each with a length of 24 bits. When these contents are equal the flag COMP will be set 4 ms after the falling edge of MIN. This set condition occurs once at the beginning of each minute. This information is latched, but can be cleared by an instruction via the I^2C bus. A clear instruction may be transmitted immediately after the flag is set and will be executed. Flag COMP information is also available at the output COMP. The comparison may be based upon hours and minutes only if the internal flag NODA (no date) is set. Flag NODA can be set and cleared by separate instructions via the I^2C bus, but it is undefined until the first set or clear instruction has been received. Both COMP and NODA flags are readable via the I^2C bus.

FUNCTIONAL DESCRIPTION (continued)

Power on/power fail detection

If the voltage $V_{DD}-V_{SS1}$ falls below a certain value the operation of the clock becomes undefined. Thus a warning signal is required to indicate that faultless operation of the clock is not guaranteed. This information is latched in a flag called POWF (Power Fail) and remains latched after restoration of the correct supply voltage until a write procedure with EXECUTE ADDRESS has been received. The flag POWF can be set by an internally generated power fail level-discriminator signal for application with ($V_{DD}-V_{SS1}$) greater than V_{TH1}, or by an externally generated power fail signal for application with ($V_{DD}-V_{SS1}$) less than V_{TH1}. The external signal must be applied to the input PFIN. The input stage operates with signals of any slow rise and fall times. Internally or externally controlled POWF can be selected by input EXTPF as shown in Table 2.

Table 2 Power fail selection

EXTPF	PFIN	function
0	0	power fail is sensed internally
0	1	test mode
1	0	power fail is sensed externally
1	1	no power fail sensed

0 : connected to V_{SS1} (LOW)
1 : connected to V_{DD} (HIGH)

The external power fail control operates by absence of the $V_{DD}-V_{SS2}$ supply. Therefore the input levels applied to PFIN and EXTPF must be within the range of $V_{DD}-V_{SS1}$. A LOW level at PFIN indicates a power fail. POWF is readable via the I^2C bus. A power on reset for the I^2C bus control is generated on-chip when the supply voltage $V_{DD}-V_{SS2}$ is less than V_{TH2}.

Interface level shifters

The level shifters adjust the 5 V operating voltage ($V_{DD}-V_{SS2}$) of the microcontroller to the internal supply voltage ($V_{DD}-V_{SS1}$) of the clock/calendar. The oscillator and counter are not influenced by the $V_{DD}-V_{SS2}$ supply voltage. If the voltage $V_{DD}-V_{SS2}$ is absent ($V_{SS2} = V_{DD}$) the output signal of the level shifter is HIGH because V_{DD} is the common node of the $V_{DD}-V_{SS2}$ and the $V_{DD}-V_{SS1}$ supplies. Because the level shifters invert the input signal, the internal circuit behaves as if a LOW signal is present on the inputs. FSET, SEC, MIN and COMP are CMOS push-pull output stages. The driving capability of these outputs is lost when the supply voltage $V_{DD}-V_{SS2} = 0$.

CHARACTERISTICS OF THE I²C BUS

The I²C bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

Bit transfer (see Fig. 3)

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals.

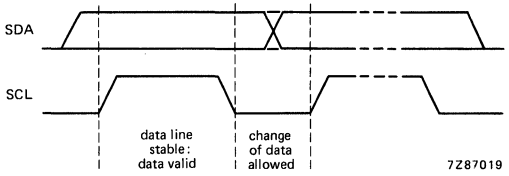


Fig. 3 Bit transfer.

Start and stop conditions (see Fig. 4)

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the stop condition (P).

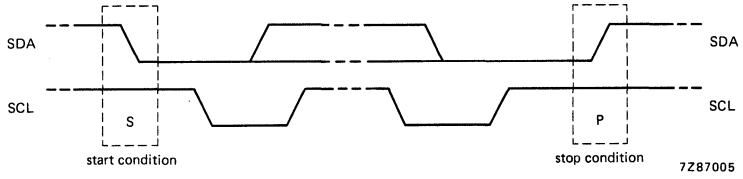


Fig. 4 Definition of start and stop conditions.

System configuration (see Fig. 5)

A device generating a message is a "transmitter", a device receiving a message is the "receiver". The device that controls the message is the "master" and the devices which are controlled by the master are the "slaves".

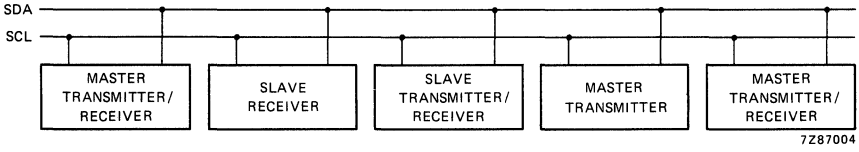


Fig. 5 System configuration.

CHARACTERISTICS OF THE I²C bus (continued)

Acknowledge (see Fig. 6)

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse, set up and hold times must be taken into account. A master receiver must signal an end of data to the transmitter by *not* generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition. (See Fig. 13 and Fig. 14.)

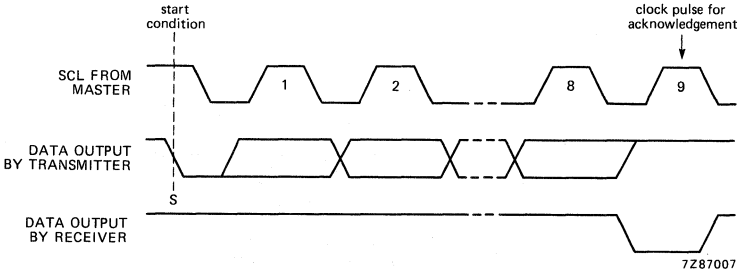


Fig. 6 Acknowledgement on the I²C bus.

Timing specifications

Within the I²C bus specifications a high-speed mode and a low-speed mode are defined. The PCF8573 operates in both modes and the timing requirements are as follows:

High-speed mode

Masters generate a bus clock with a maximum frequency of 100 kHz. Detailed timing is shown in Fig. 7.

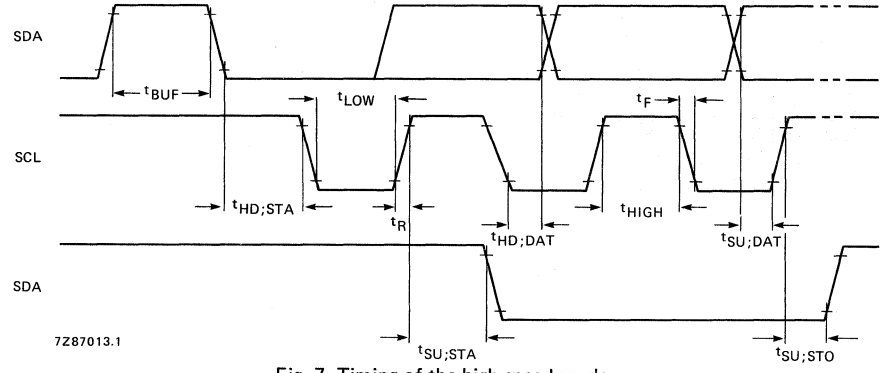


Fig. 7 Timing of the high-speed mode.

Where:

t_{BUF}	$t \geqslant t_{LOWmin}$	The minimum time the bus must be free before a new transmission can start
$t_{HD;STA}$	$t \geqslant t_{HIGHmin}$	Start condition hold time
t_{LOWmin}	4,7 μs	Clock LOW period
$t_{HIGHmin}$	4 μs	Clock HIGH period
$t_{SU;STA}$	$t \geqslant t_{LOWmin}$	Start condition set-up time, only valid for repeated start code
$t_{HD;DAT}$	$t \geqslant 0$ μs	Data hold time
$t_{SU;DAT}$	$t \geqslant 250$ ns	Data set-up time
t_R	$t \leqslant 1$ μs	Rise time of both the SDA and SCL line
t_F	$t \leqslant 300$ ns	Fall time of both the SDA and SCL line
$t_{SU;STO}$	$t \geqslant t_{LOWmin}$	Stop condition set-up time

Note

All the values refer to V_{IH} and V_{IL} levels with a voltage swing of V_{DD} to V_{SS2}.

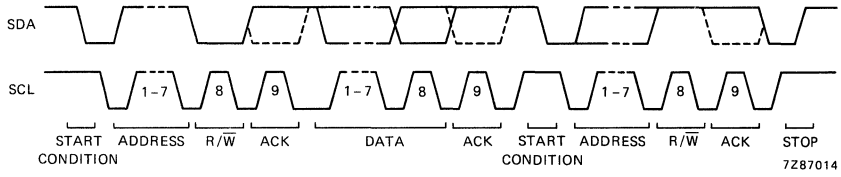


Fig. 8 Complete data transfer in the high-speed mode.

Where:

Clock t_{LOWmin}	4,7 μs
$t_{HIGHmin}$	4 μs
The dashed line is the acknowledgement of the receiver	
Mark-to-space ratio	1 : 1 (LOW-to-HIGH)
Max. number of bytes	unrestricted
Premature termination of transfer	allowed by generation of STOP condition
Acknowledge clock bit	must be provided by the master

DEVELOPMENT DATA

CHARACTERISTICS OF THE I²C BUS (continued)

Low-speed mode

Masters generate a bus clock with a maximum frequency of 2 kHz; a minimum LOW period of 105 μs and a minimum HIGH period of 365 μs. The mark-to-space ratio is 1 : 3 LOW-to-HIGH. Detailed timing is shown in Fig. 9.

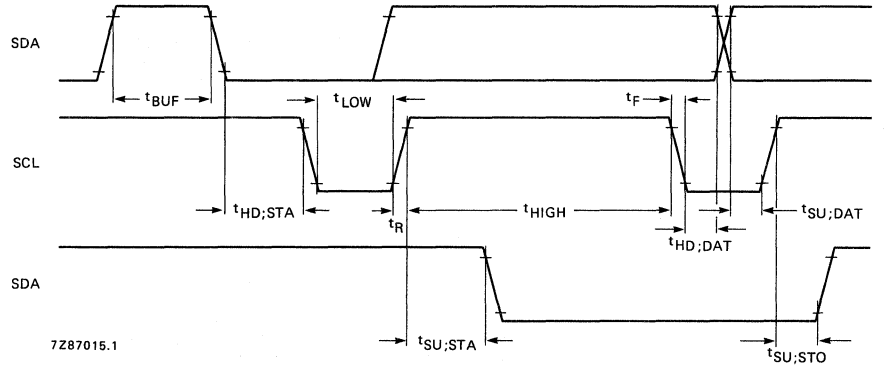


Fig. 9 Timing of the low-speed mode.

Where:

t_{BUF}	$t \geqslant 105\ \mu s$ (t_{LOWmin})
$t_{HD;STA}$	$t \geqslant 365\ \mu s$ ($t_{HIGHmin}$)
t_{LOW}	130 μs ± 25 μs
t_{HIGH}	390 μs ± 25 μs
$t_{SU;STA}$	130 μs ± 25 μs*
$t_{HD;DAT}$	$t \geqslant 0\ \mu s$
$t_{SU;DAT}$	$t \geqslant 250$ ns
t_R	$t \leqslant 1\ \mu s$
t_F	$t \leqslant 300$ ns
$t_{SU;STO}$	130 μs ± 25 μs

Note

All the values refer to V_{IH} and V_{IL} levels with a voltage swing of V_{DD} to V_{SS2}, for definitions see high-speed mode.

* Only valid for repeated start code.

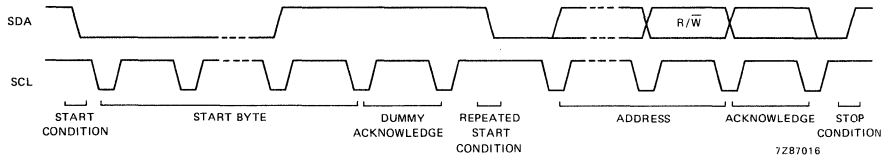


Fig. 10 Complete data transfer in the low-speed mode.

Where:

Clock t_{LOWmin}	130 μs ± 25 μs
$t_{HIGHmin}$	390 μs ± 25 μs
Mark-to-space ratio	1 : 3 (LOW-to-HIGH)
Start byte	0000 0001
Max. number of bytes	6
Premature termination of transfer	not allowed
Acknowledge clock bit	must be provided by master

Note

The general characteristics and detailed specification of the I^2C bus are described in a separate data sheet (serial data buses) in handbook: ICs for digital systems in radio, audio and video equipment.

ADDRESSING

Before any data is transmitted on the I²C bus, the device which should respond is addressed first. The addressing is always done with the first byte transmitted after the start procedure.

Slave address

The clock/calendar acts as a slave receiver or slave transmitter. Therefore the clock signal SCL is only an input signal, but the data signal SDA is a bidirectional line. The clock calendar slave address is shown in Fig. 11.

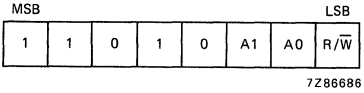


Fig. 11 Slave address.

The subaddress bits A0 and A1 correspond to the two hardware address pins A0 and A1 which allows the device to have 1 of 4 different addresses.

Clock/calendar READ/WRITE cycles

The I²C bus configuration for different clock/calendar READ and WRITE cycles is shown in Fig. 12 and Fig. 13.

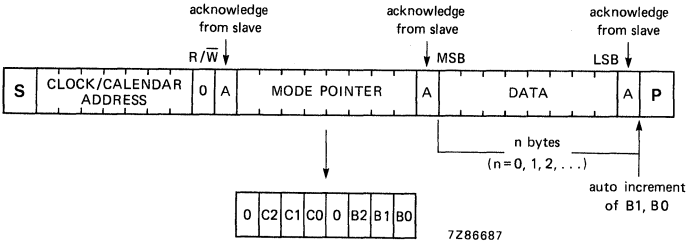


Fig. 12 Master transmitter transmits to clock/calendar slave receiver.

The write cycle is used to set the time counter, the alarm register and the flags. The transmission of the clock/calendar address is followed by the MODE-POINTER-WORD which contains a CONTROL-nibble (Table 3) and an ADDRESS-nibble (Table 4). The ADDRESS-nibble is valid only if the preceding CONTROL-nibble is set to EXECUTE ADDRESS. The third transmitted word contains the data to be written into the time counter or alarm register.

Table 3 CONTROL-nibble

	C2	C1	C0	function
0	0	0	0	execute address
0	0	0	1	read control/status flags
0	0	1	0	reset prescaler, including seconds counter; without carry for minute counter
0	0	1	1	time adjust, with carry for minute counter (see note)
0	1	0	0	reset NODA flag
0	1	0	1	set NODA flag
0	1	1	0	reset COMP flag

Note

If the seconds counter is below 30 there is no carry. This causes a time adjustment of max. –30 s. From the count 30 there is a carry which adjusts the time by max. + 30 s.

Table 4 ADDRESS-nibble

	B2	B1	B0	addressed to:
0	0	0	0	time counter hours
0	0	0	1	time counter minutes
0	0	1	0	time counter days
0	0	1	1	time counter months
0	1	0	0	alarm register hours
0	1	0	1	alarm register minutes
0	1	1	0	alarm register days
0	1	1	1	alarm register months

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At the end of each data word the address bits B1, B0 will be incremented automatically provided the preceding CONTROL-nibble is set to EXECUTE ADDRESS. There is no carry to B2.

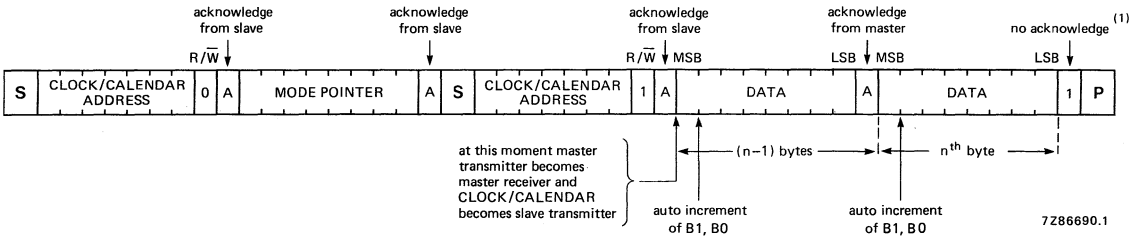
Table 5 shows the placement of the BCD upper and lower digits in the DATA byte for writing into the addressed part of the time counter and alarm register respectively.

Table 5 Placement of BCD digits in the DATA byte

MSB			DATA				LSB	
upper digit				lower digit				
UD	UC	UB	UA	LD	LC	LB	LA	addressed to:
X	X	D	D	D	D	D	D	hours
X	D	D	D	D	D	D	D	minutes
X	X	D	D	D	D	D	D	days
X	X	X	D	D	D	D	D	months

Where "X" is the don't care bit and "D" is the data bit.

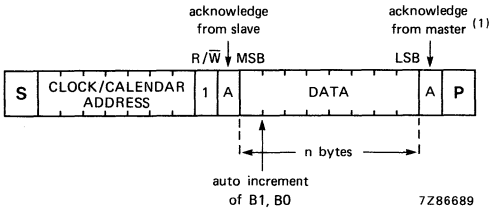
Acknowledgement response of the clock calendar as slave receiver is shown in Table 6.



(1) The master receiver must signal an end of data to the slave transmitter by *not* generating an acknowledge on the *last byte* that has been clocked out of the slave.

Fig. 13 Master transmitter reads clock/calendar after setting mode pointer.

To read the addressed part of the time counter and alarm register, plus information from specified control/status flags, the BCD digits in the DATA byte are organized as shown in Table 7.



(1) The master receiver must signal an end of data to the slave transmitter by *not* generating an acknowledge on the *last byte* that has been clocked out of the slave.

Fig. 14 Master reads clock/calendar immediately after first byte.

The status of the MODE-POINTER-WORD concerning the CONTROL-nibble remains unchanged until a write to MODE POINTER condition occurs.

ADDRESSING (continued)

Table 6 Slave receiver acknowledgement

mode pointer								acknowledge on byte		
								address	mode pointer	data
	C2	C1	C0		B2	B1	B0			
0	0	0	0	0	X	X	X	yes	yes	yes
0	0	0	0	1	X	X	X	yes	no	no
0	0	0	1	X	X	X	X	yes	yes	no
0	0	1	0	X	X	X	X	yes	yes	no
0	0	1	1	X	X	X	X	yes	yes	no
0	1	0	0	X	X	X	X	yes	yes	no
0	1	0	1	X	X	X	X	yes	yes	no
0	1	1	0	X	X	X	X	yes	yes	no
0	1	1	1	X	X	X	X	yes	no	no
1	X	X	X	X	X	X	X	yes	no	no

Where "X" is the don't care bit.

Table 7 Organization of the BCD digits in the DATA byte

MSB DATA LSB								
upper digit				lower digit				
UD	UC	UB	UA	LD	LC	LB	LA	addressed to
0	0	D	D	D	D	D	D	hours
0	D	D	D	D	D	D	D	minutes
0	0	D	D	D	D	D	D	days
0	0	0	D	D	D	D	D	months
0	0	0	*	**	NODA	COMP	POWF	control/status flags

Where: "D" is the data bit.
* = minutes.
** = seconds.

DEVELOPMENT DATA

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage ranges	$V_{DD}-V_{SS1}$		−0,3 to + 8	V
	$V_{DD}-V_{SS2}$		−0,3 to + 8	V
Voltage on pins 4 and 5			V_{SS2}−0,8 to V_{DD} + 0,8	V*
Voltage on pins 6, 7, 13 and 14			V_{SS1}−0,6 to V_{DD} + 0,6	V
Voltage on any other pin			V_{SS2}−0,6 to V_{DD} + 0,6	V
Input current	I_I	max.	10	mA
Output current	I_O	max.	10	mA
Power dissipation per output	P_O	max.	100	mW
Total power dissipation per package	P_{tot}	max.	200	mW
Operating ambient temperature range	T_{amb}		−40 to + 85	°C
Storage temperature range	T_{stg}		−55 to + 125	°C

HANDLING

Inputs and outputs are protected against electrostatic charge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see 'Handling MOS Devices').

* Impedance min. 500 Ω.

DEVELOPMENT DATA

CHARACTERISTICS

V_{SS2} = 0 V; T_{amb} = −40 to + 85 °C unless otherwise specified. Typical values at T_{amb} = + 25 °C

parameter	symbol	min.	typ.	max.	unit
Supply					
Supply voltage (I^2C interface)	$V_{DD}-V_{SS2}$	2,5	5	6,0	V
Supply voltage (clock)	$V_{DD}-V_{SS1}$	1,1	1,5	($V_{DD}-V_{SS2}$)	V
Supply current V_{SS1}					
at $V_{DD}-V_{SS1}$ = 1,5 V	$-I_{SS1}$	–	3	10	μA
at $V_{DD}-V_{SS1}$ = 5 V	$-I_{SS1}$	–	12	50	μA
Supply current V_{SS2}					
at $V_{DD}-V_{SS2}$ = 5 V (I_O = 0 mA on all outputs)	$-I_{SS2}$	–	–	50	μA
Inputs SCL, SDA, A0, A1, TEST					
Input voltage HIGH	V_{IH}	0,7 x V_{DD}	–	–	V
Input voltage LOW	V_{IL}	–	–	0,3 x V_{DD}	V
Input leakage current at V_I = V_{SS2} to V_{DD}	$\pm I_I$	–	–	1	μA
Inputs EXTPF, PFIN					
Input voltage HIGH	$V_{IH}-V_{SS1}$	0,7 x ($V_{DD}-V_{SS1}$)	–	–	V
Input voltage LOW	$V_{IL}-V_{SS1}$	0	–	0,3 x ($V_{DD}-V_{SS1}$)	V
Input leakage current					
at V_I = V_{SS1} to V_{DD}	$\pm I_I$	–	–	1	μA
at T_{amb} = 25 °C; V_I = V_{SS1} to V_{DD}	$\pm I_I$	–	–	0,1	μA
Outputs SEC, MIN, COMP, FSET (normal buffer outputs)					
Output voltage HIGH					
at $V_{DD}-V_{SS2}$ = 2,5 V; $-I_O$ = 0,1 mA	V_{OH}	$V_{DD}-0,4$	–	–	V
at $V_{DD}-V_{SS2}$ = 4 to 6 V; $-I_O$ = 0,5 mA	V_{OH}	$V_{DD}-0,4$	–	–	V
Output voltage LOW					
at $V_{DD}-V_{SS2}$ = 2,5 V; I_O = 0,3 mA	V_{OL}	–	–	0,4	V
at $V_{DD}-V_{SS2}$ = 4 to 6 V; I_O = 1,6 mA	V_{OL}	–	–	0,4	V

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Output SDA (N-channel open drain)					
Output "ON": I_O = 3 mA at $V_{DD}-V_{SS2}$ = 2,5 to 6 V	V_{OL}	–	–	0,4	V
Output "OFF" (leakage current) at $V_{DD}-V_{SS2}$ = 6 V; V_O = 6 V	I_O	–	–	1	μA
Internal threshold voltage					
Power failure detection	V_{TH1}	1	1,2	1,4	V
Power "ON" reset at $V_{SCL} = V_{SDA} = V_{DD}$	V_{TH2}	1,5	2,0	2,5	V
Rise and fall times of input signals					
Input EXTPF	t_r, t_f	–	–	1	μs
Input PFIN	t_r, t_f	–	–	∞	μs
Input signals except EXTPF and PFIN between V_{IL} and V_{IH} levels					
rise time	t_r	–	–	1	μs
fall time	t_f	–	–	0,3	μs
Frequency at SCL at $V_{DD}-V_{SS2}$ = 4 to 6 V					
Pulse width LOW (see Figs 7 and 9)	t_{LOW}	4,7	–	–	μs
Pulse width HIGH (see Figs 7 and 9)	t_{HIGH}	4	–	–	μs
Noise suppression time constant at SCL and SDA input	T_I	0,25	1	2,5	μs
Input capacitance (SCL, SDA)	C_I	–	–	7	pF
Oscillator					
Integrated oscillator capacitance	C_{out}	–	40	–	pF
Oscillator feedback resistance	R_f	–	3	–	MΩ
Oscillator stability for: $\Delta(V_{DD}-V_{SS1})$ = 100 mV at $V_{DD}-V_{SS1}$ = 1,55 V; T_{amb} = 25 °C	f/f_{osc}	–	2×10^{-6}	–	–
Quartz crystal parameters					
Frequency = 32,768 kHz					
Series resistance	R_S	–	–	40	kΩ
Parallel capacitance	C_L	–	9	–	pF
Trimmer capacitance	C_T	5	–	25	pF

Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

DEVELOPMENT DATA

APPLICATION INFORMATION

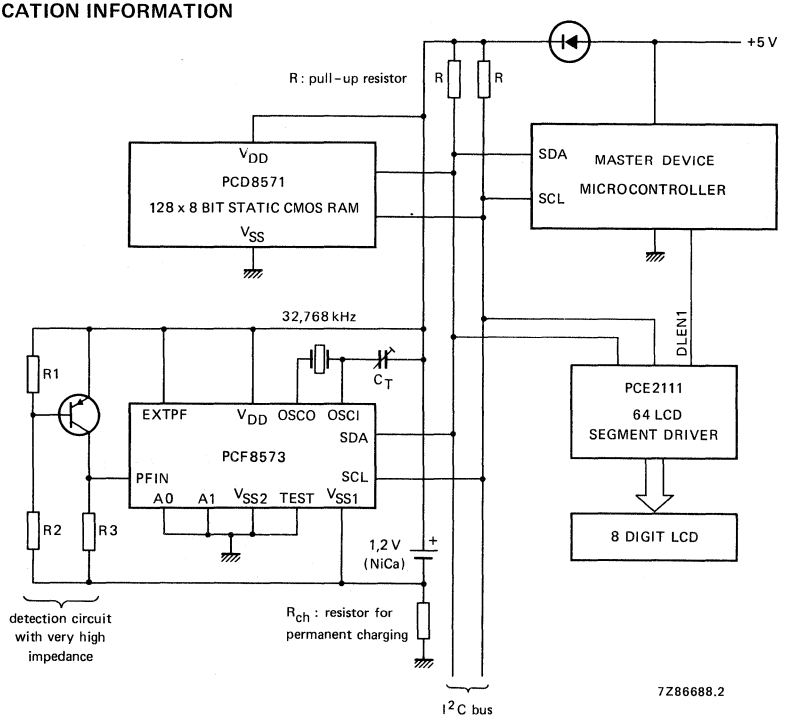


Fig. 15 Application example of the PCF8573 clock/calendar.

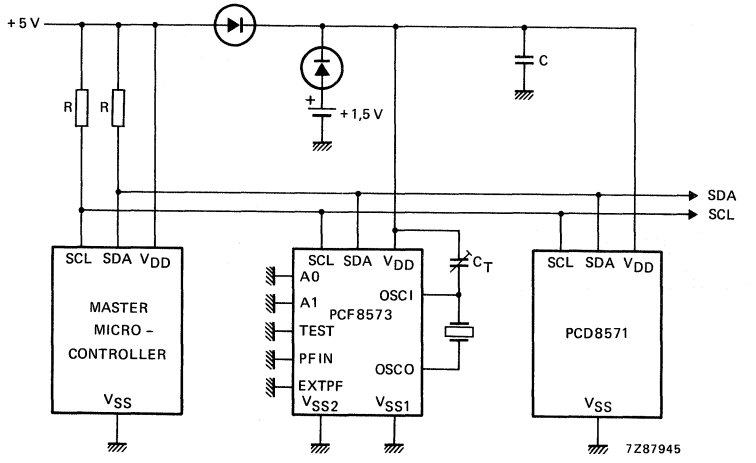


Fig. 16 Application example of the PCF8573 with common V_{SS1} and V_{SS2} supply.

7-BIT ANALOGUE-TO-DIGITAL CONVERTER (ADC 7)

GENERAL DESCRIPTION

The PNA7507, PNA7507A are monolithic NMOS 7-bit analogue-to-digital converters (ADC) designed for video applications. The difference between the two versions is the linearity. The device converts the analogue input signal into 7-bit binary coded digital words at a sampling rate of 15 MHz.

The circuit comprises 129 comparators, a reference resistor chain, transcoder stages, and TTL output buffers which are positive edge triggered. The digital output is selectable in two's complement or binary coding.

The use of separate outputs for overflow and underflow detection facilitates full-scale driving.

Features

- 7-bit resolution
- Digitizing rates up to 15 MHz
- No external sample and hold required
- High input impedance
- Binary or two's complement TTL outputs
- Overflow and underflow outputs
- Low reference current (200 μA typ.)
- Positive supply voltages (+ 5 V/+ 12 V)
- Low power consumption (350 mW typ.)
- Standard 24 pin package

Applications

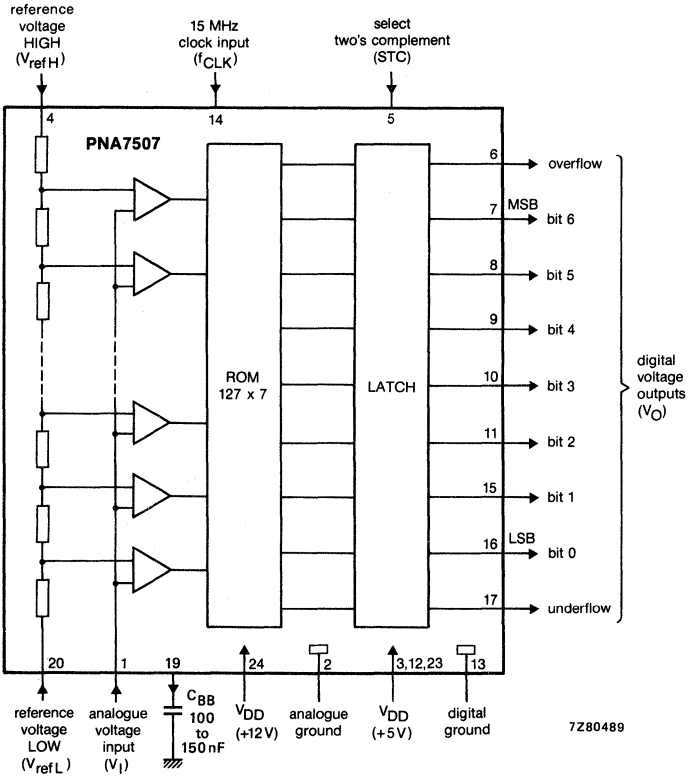
- High-speed A/D conversion
- Video signal digitizing
- Radar pulse analysis
- Transient signal analysis
- High energy physics research

QUICK REFERENCE DATA

Supply voltage range (pins 3, 12, 23)	V_{DD}	4,75 to	5,25	V
Supply voltage range (pin 24)	V_{DD}	11,4 to	12,6	V
Supply current (pins 3, 12, 23)	I_{DD}	typ.	40	mA
Supply current (pin 24)	I_{DD}	typ.	12	mA
Reference voltage LOW (pin 20)	V_{refL}	min.	2,4	V
Reference voltage HIGH (pin 4)	V_{refH}	max.	5,2	V
PNA7507				
Linearity (± 0,4% full scale)			± 1/2	LSB
PNA7507A				
Linearity (± 0,5% full scale)			± 2/3	LSB
Bandwidth (−3 dB)	B	min.	6	MHz
Clock frequency	f_{CLK}	max.	15	MHz
Total power dissipation	P_{tot}	typ.	350	mW

PACKAGE OUTLINE

24-lead DIL; plastic (SOT-101A).



Note

All three pins 3, 12 and 23 must be connected to positive supply voltage + 5 V.

Fig. 1 Block diagram.

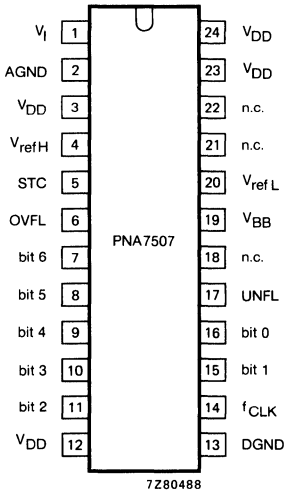


Fig. 2 Pinning diagram.

PINNING

1	V_I	analogue voltage input
2	AGND	analogue ground
3	V_{DD}	positive supply voltage (+ 5 V)
4	V_{refH}	reference voltage HIGH
5	STC	select two's complement
6	OVFL	overflow
7	bit 6	most-significant bit (MSB)
8	bit 5	
9	bit 4	
10	bit 3	
11	bit 2	
12	V_{DD}	positive supply voltage (+ 5 V)
13	DGND	digital ground
14	f_{CLK}	15 MHz clock input
15	bit 1	
16	bit 0	least-significant bit (LSB)
17	UNFL	underflow
18	n.c.	not connected
19	V_{BB}	back bias output
20	V_{refL}	reference voltage LOW
21	n.c.	not connected
22	n.c.	not connected
23	V_{DD}	positive supply voltage (+ 5 V)
24	V_{DD}	positive supply voltage (+ 12 V)

DEVELOPMENT DATA

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range (pins 3, 12, 23)	V_{DD}	−0,5 to	+ 7	V
Supply voltage range (pin 24)	V_{DD}	−0,5 to	+ 13,5	V
Input voltage range	V_I	−0,5 to	+ 7	V
Output current	I_O		5	mA
Total power dissipation	P_{tot}		tbf	mW
Storage temperature range	T_{stg}	−65 to	+ 150	°C
Operating ambient temperature range	T_{amb}	−10 to	+ 80	°C

HANDLING

Inputs and output are protected against electrostatic charge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see "Handling MOS Devices").

CHARACTERISTICS

$V_{DD5} = V_{3, 12, 23-13} = 4{,}75$ to 5,25 V; $V_{DD12} = V_{24-2} = 11{,}4$ to 12,6 V; $C_{BB} = 100$ nF; $T_{amb} = 0$ to + 70 °C; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply					
Supply voltage (pins 3, 12, 23)	V_{DD}	4,75	5,0	5,25	V
Supply voltage (pin 24)	V_{DD}	11,4	12,0	12,6	V
Supply current (pins 3, 12, 23)	I_{DD}	–	40	80	mA
Supply current (pin 24)	I_{DD}	–	12	20	mA
Reference voltages					
Reference voltage LOW (pin 20)	V_{refL}	2,4	2,5	2,6	V
Reference voltage HIGH (pin 4)	V_{refH}	5,0	5,1	5,2	V
Reference current	I_{ref}	120	200	280	μA
Inputs					
Clock input (pin 14)					
Input voltage LOW	V_{IL}	−0,3	–	0,8	V
Input voltage HIGH	V_{IH}	2,0	–	5,5	V
Digital input levels (STC, pin 5)*					
Input voltage LOW	V_{IL}	0	–	0,8	V
Input voltage HIGH	V_{IH}	2,0	–	5,5	V
Input current at $V_{5-13} = 0$ V	$-I_5$	35	–	150	μA
Input leakage current (not STC)	I_{LI}	–	–	10	μA
Analogue input levels (pin 1) at $V_{refL} = 2{,}5$ V; $V_{refH} = 5{,}1$ V					
Input voltage amplitude (peak-to-peak value)	$V_{I(p-p)}$	–	2,6	–	V
Input voltage (underflow)	V_I	–	2,5	–	V
Input voltage (overflow)	V_I	–	5,1	–	V
Offset input voltage (underflow)	$V_I - V_{refL}$	–	10	–	mV
Offset input voltage (overflow)	$V_I - V_{refH}$	–	−10	–	mV
Input capacitance	C_{1-2}	tbf	40	tbf	pF

* When input voltage is LOW binary coding is selected; when input voltage is HIGH two's complement is selected; if pin 5 is open-circuit the input is HIGH. For output coding see Table 1.

parameter	symbol	min.	typ.	max.	unit
Outputs					
Digital voltage outputs (pins 6 to 11 and 15 to 17)					
Output voltage LOW at I_O = 2 mA	V_{OL}	0	–	–0,4	V
Output voltage HIGH at $-I_O$ = 0,2 mA	V_{OL}	2,4	–	V_{DD5}	V
Timing (see also Fig. 3)					
Clock input (pin 14)					
Clock frequency	f_{CLK}	1	–	15	MHz
Clock cycle time LOW	t_{LOW}	22	–	–	ns
Clock cycle time HIGH	t_{HIGH}	22	–	–	ns
Input rise and fall times (note 1)					
rise time	t_r	–	–	3	ns
fall time	t_f	–	–	3	ns
Analogue input (pin 1)					
Bandwidth (–3 dB)	B	6	–	–	MHz
Aperture time delay (note 2)	t_{ad}	–	8	15	ns
Aperture jitter time	t_{aj}	–	0,2	0,4	ns
Digital outputs (note 3)					
Output hold time	t_{HOLD}	6	20	–	ns
Output delay time	t_d	–	35	50	ns
Internal delay	t_{CY}	–	3	–	clocks
Propagation delay time at f_{CLK} = 13,5 MHz	t_{pd}	228	–	272	ns
Transfer function					
PNA7507					
Linearity, integral and differential (± 0,4% full scale)		–	–	± 1/2	LSB
PNA7507A					
Linearity, integral and differential (± 0,5% full scale)		–	–	± 2/3	LSB

DEVELOPMENT DATA

Notes to timing characteristics

1. Clock input rise and fall times are at the maximum clock frequency (15 MHz).
2. The aperture time delay is referenced to the peak-to-peak value of the analogue input voltage at $V_{I(p\text{-}p)}$ = 2,6 V (full scale); f = 5 MHz.
3. The timing values of the digital outputs at pins 6 to 11 and 15 to 17 are measured with the clock input reference level at 1,5 V.

Table 1 Output coding (V_{refL} = 2,5 V; V_{refH} = 5,08 V)

step	V_{1-2} (typ.)	UNFL	OVFL	binary bit 6 – bit 0	two's complement bit 6 – bit 0
underflow	< 2,51	1	0	0 0 0 0 0 0 0	1 0 0 0 0 0 0
0	2,51	0	0	0 0 0 0 0 0 0	1 0 0 0 0 0 0
1	2,53	0	0	0 0 0 0 0 0 1	1 0 0 0 0 0 1
.	.	.	.	. . . .	. . . .
.	.	.	.	. . . .	. . . .
.	.	.	.	. . . .	. . . .
.	.	.	.	. . . .	. . . .
126	5,03	0	0	1 1 1 1 1 1 0	0 1 1 1 1 1 0
127	5,05	0	0	1 1 1 1 1 1 1	0 1 1 1 1 1 1
overflow	⩾ 5,07	0	1	1 1 1 1 1 1 1	0 1 1 1 1 1 1

steps 2 – 125

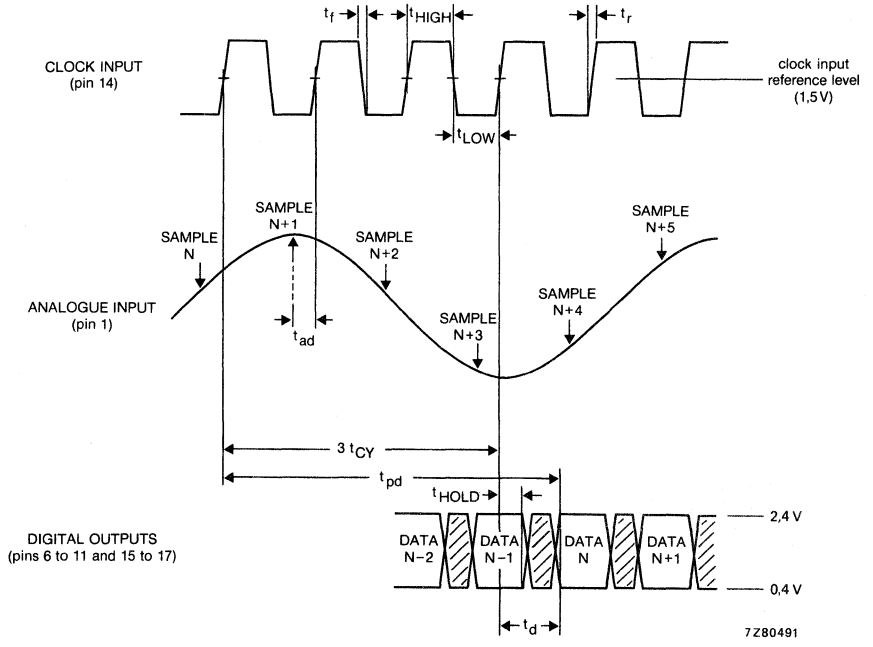


Fig. 3 Timing diagram.

APPLICATION INFORMATION

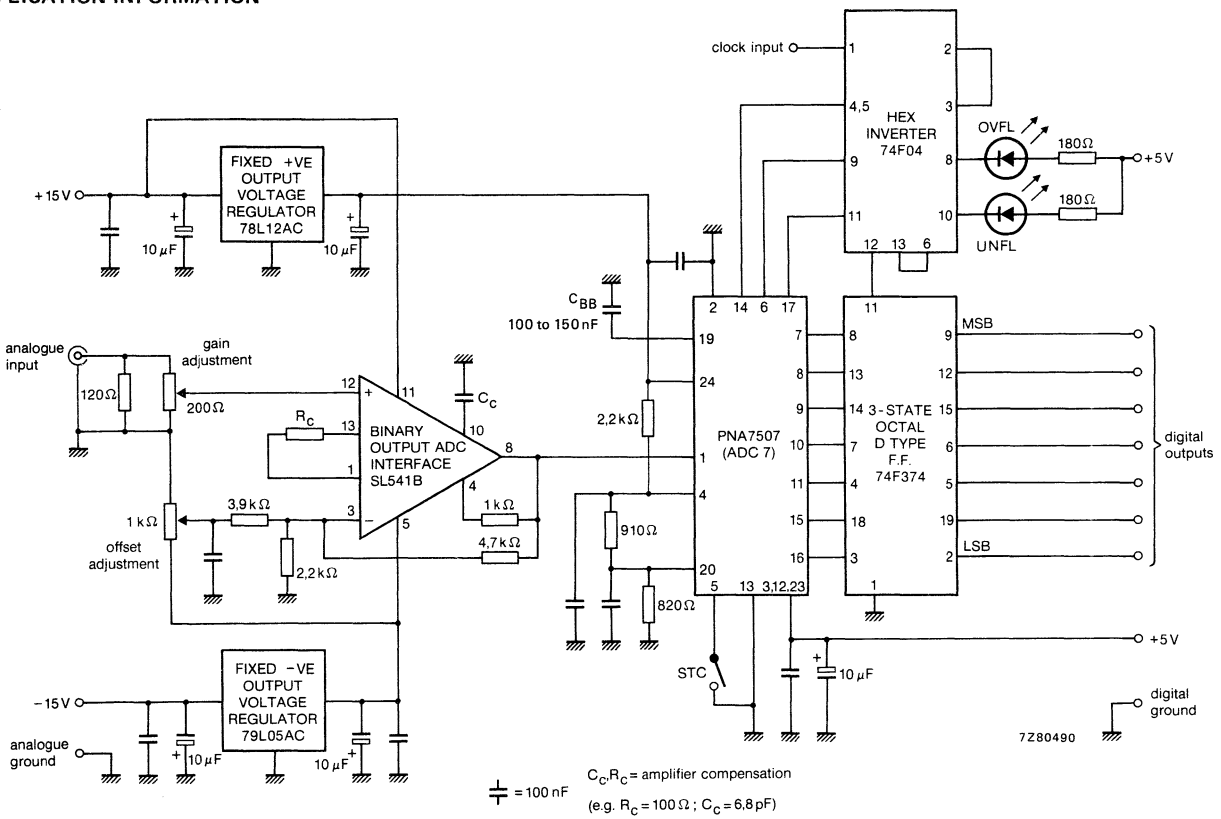


Fig. 4 Application circuit diagram.

8-BIT MULTIPLYING DAC

GENERAL DESCRIPTION

The PNA7518 is a NMOS 8-bit multiplying digital-to-analogue converter (DAC) designed for video applications. The device converts a digital input signal into a voltage-equivalent analogue output at a sampling rate of 30 MHz.

The input signal is latched, then fed to a decoder which switches a transfer gate array (1 out of 256) to select the appropriate analogue signal from a resistor chain. Two external reference voltages supply the resistor chain.

The input latches are positive-edge triggered. The output impedance is approximately 0,5 kΩ depending on the applied digital code. An additional operational amplifier is required for the 75 Ω output impedance. Two's complement is selected when STC (pin 11) is HIGH or is not connected.

Features

- TTL input levels
- Positive-edge triggered
- Analogue voltage output at 30 MHz sampling rate
- Binary or two's complement input
- Output voltage accuracy to within ± ½ of the input LSB

QUICK REFERENCE DATA

Supply voltage range (pin 16)	V_{DD}	4,5 to 5,5	V
Supply current (pin 16)	I_{DD}	typ. 50	mA
Reference voltage LOW (pin 2)	V_{refL}	min. 0	V
Reference voltage HIGH (pin 9)	V_{refH}	max. 2	V
Linearity at R_L = 200 kΩ; V_O = 2 V (peak-to-peak value)		± ½	LSB
Bandwidth (−3 dB) at C_L = 6 pF	B	min. 12	MHz
Clock frequency	f_{CLK}	max. 30	MHz
Total power dissipation	P_{tot}	typ. 300	mW

Applications

- Video data conversion
- CRT displays
- Waveform/test signal generation
- Colour/black-and-white graphics

PACKAGE OUTLINE

16-lead DIL; plastic (SOT-38WE-1).

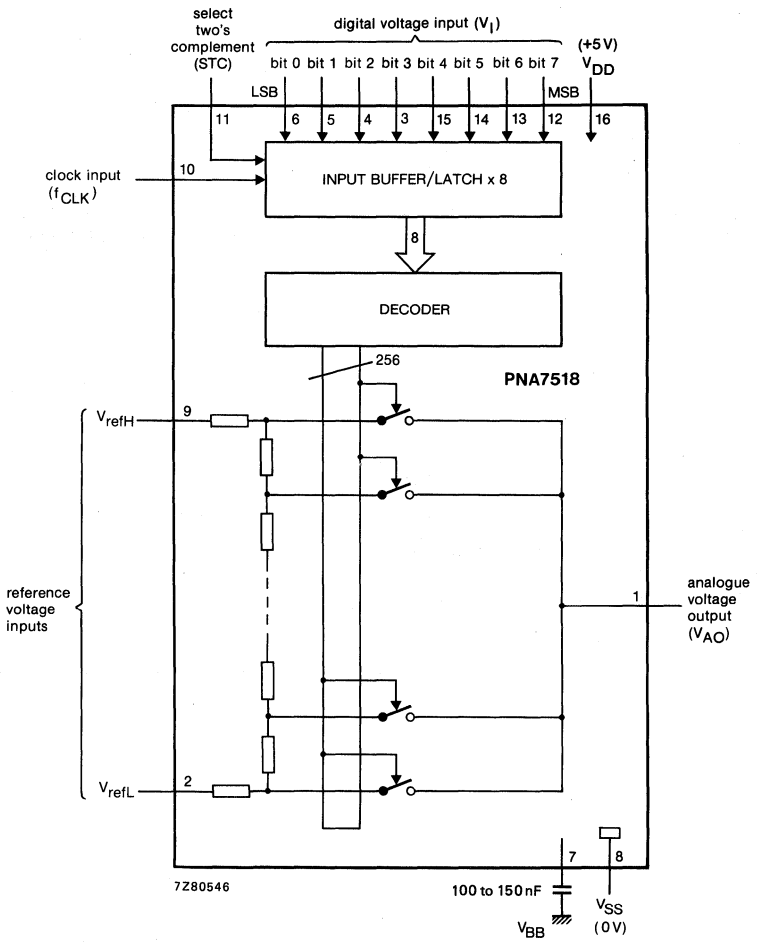


Fig. 1 Block diagram.

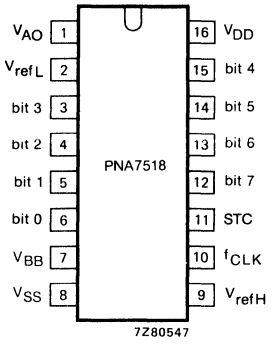


Fig. 2 Pinning diagram.

PINNING

1	V_{AO}	analogue output voltage
2	V_{refL}	reference voltage LOW
3	bit 3	digital voltage inputs (V_I)
4	bit 2	
5	bit 1	
6	bit 0	least-significant bit (LSB)
7	V_{BB}	back bias
8	V_{SS}	ground
9	V_{refH}	reference voltage HIGH
10	f_{CLK}	clock input
11	STC	select two's complement
12	bit 7	most-significant bit (MSB)
13	bit 6	digital voltage inputs (V_I)
14	bit 5	
15	bit 4	
16	V_{DD}	positive supply voltage

DEVELOPMENT DATA

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range (pin 16)	V_{DD}	−0,5 to + 7	V
Input voltage range (pins 3, 4, 5, 6, 11, 12, 13, 14 and 15)	V_I	−0,5 to + 7	V
Output voltage range (pin 1)	V_{AO}	−0,5 to + 7	V
Total power dissipation	P_{tot}	max. 400	mW
Storage temperature range	T_{stg}	−65 to + 150	°C
Operating ambient temperature range	T_{amb}	0 to + 70	°C

HANDLING

Inputs and outputs are protected against electrostatic charge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see "Handling MOS Devices").

CHARACTERISTICS

V_{DD} = 4,5 to 5,5; V_{SS} = 0 V; C_{BB} = 100 nF; T_{amb} = 0 to + 70 °C; unless otherwise specified.

parameter	symbol	min.	typ.	max.	unit
Supply (pin 16)					
Supply voltage	V_{DD}	4,5	5	5,5	V
Supply current	I_{DD}	–	50	80	mA
Reference voltages					
Reference voltage LOW (pin 2)	V_{refL}	−0,1	–	+ 2,1	V
Reference voltage HIGH (pin 9)	V_{refH}	−0,1	–	+ 2,1	V
Reference ladder	R_{ref}	150	230	300	Ω
Inputs					
Digital input levels (TTL) (note 1)					
input voltage LOW	V_{IL}	0	–	0,8	V
input voltage HIGH	V_{IH}	2,0	–	5,25	V
input leakage current	I_{LI}	–	–	10	μA
Clock input (pin 10)					
input voltage LOW	V_{IL}	0	–	0,8	V
input voltage HIGH	V_{IH}	2,0	–	5,25	V
input leakage current	I_{LI}	–	–	10	μA
frequency	f_{CLK}	1	–	30	MHz
pulse width HIGH	t_{PWH}	10	–	–	ns
pulse width LOW	t_{PWL}	10	–	–	ns
input rise time at f_{CLK} = 30 MHz	t_r	–	–	3	ns
input fall time at f_{CLK} = 30 MHz	t_f	–	–	3	ns
Output					
Analogue voltage output (pin 1) at R_L = 200 kΩ)	V_{AO}	0	–	2	V
Bandwidth (−3 dB) at C_L = 6 pF	B	12	18	–	MHz
Switching characteristics (Fig. 3)					
Data set-up time	$t_{SU;DAT}$	3	–	–	ns
Data hold time	$t_{HD;DAT}$	4	–	–	ns
Propagation delay time, input to output	t_{PD}	t_{CLK} + 15	t_{CLK} + 22	t_{CLK} + 30	ns
Settling time: 10 to 90% full-scale change; C_L = 6 pF; R_L = 200 kΩ	t_{S1}	–	13	20	ns
Settling time to ± 1 LSB; C_L = 6 pF; R_L = 200 kΩ	t_{S2}	–	40	–	ns

parameter	symbol	min.	typ.	max.	unit
Output transients (glitches) (note 2 and Fig. 3)					
1 LSB change:					
Maximum occurring at step 7F-80 (HEX)		–	3	–	LSB
area amplitude	V_g	–	23	–	LSB.ns
Generally:					
Maximum occurring at step 00-AA (HEX)		–	5	–	LSB
are amplitude	V_g	–	41	–	LSB.ns
Influence of clock frequency (note 2)					
Cross-talk at 2 x f_{CLK}					
amplitude		–	2	–	LSB
area		–	8	–	LSB.ns

Notes to the characteristics

1. Inputs bit 0 to bit 7 are positive-edge triggered.
2. Measured at V_{refH}-V_{refL} = 2,0 V; 1 x LSB = 7,8 mV. The energy equivalent of output transients is given as the area contained by the graph of output amplitude (LSB) against time (ns). The glitch area is independent of the value of V_{ref}. Glitch amplitudes and clock cross-talk can be reduced by using a shielded printed circuit board.

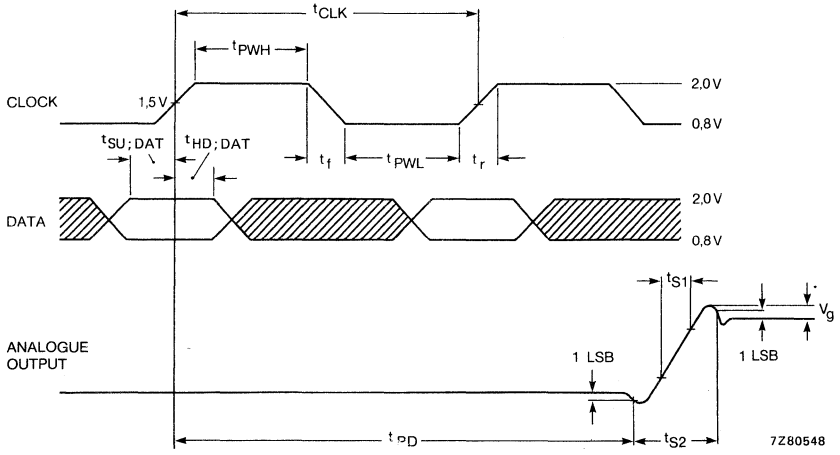


Fig. 3 Switching characteristics.

UNIVERSAL SYNC GENERATOR

GENERAL DESCRIPTION

The SAA1043 generates the synchronizing waveforms required in all types of video source equipment (video cameras, film-scanners, video games, computer displays and similar applications). The device is programmable to suit standards SECAM 1, SECAM 2, PAL/CCIR, NTSC 1, NTSC 2, and PAL-M; the video game 624 and 524-line standards; and can be synchronized to an external sync signal. Inputs and outputs are CMOS compatible.

Features

- Programmable to eight standards
- Horizontal frequency manipulation for application in non-standard systems
- Oscillator functions with LC or crystal elements
- Additional outputs to simplify camera signal processing
- Can be synchronized to an external sync signal
- Vertical reset for fast vertical lock
- Subcarrier lock in combination with subcarrier coupler SAA1044
- Very low power consumption

QUICK REFERENCE DATA

Supply voltage range (pin 28)	V_{DD}	5,7 to 7,5	V
Supply current (quiescent)	I_{DD}	max. 10	μA
Oscillator frequency	f_{OSCI}	max. 5,1	MHz

PACKAGE OUTLINE

28-lead DIL; plastic (SOT-117).

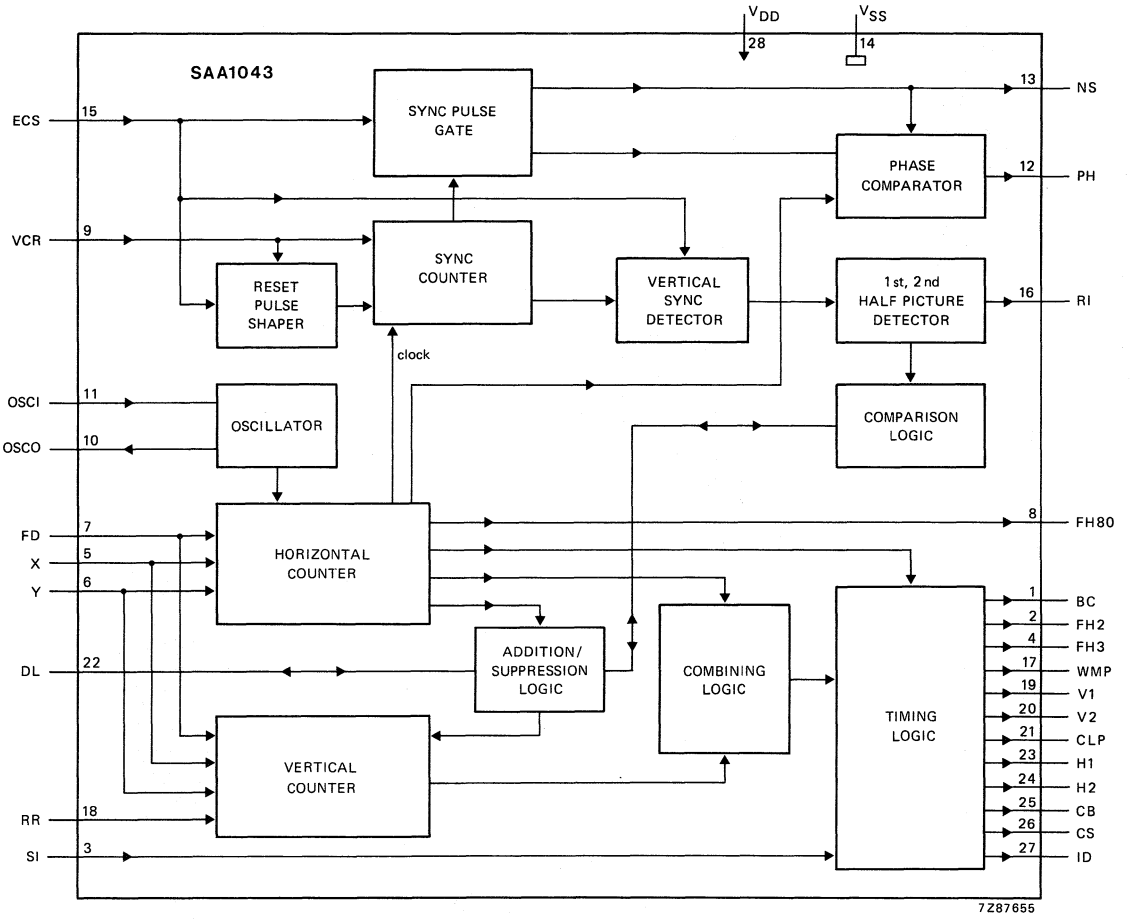


Fig. 1 Block diagram.

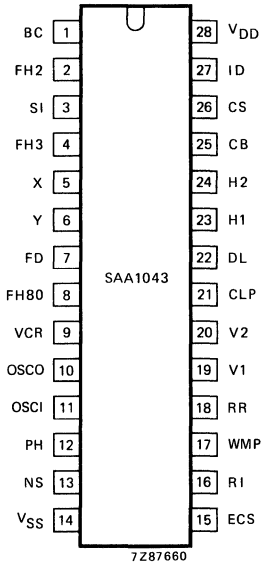


Fig. 2 Pinning diagram.

PINNING

1	BC	burst flag/chroma blanking (SECAM) output
2	FH2	PAL identification output
3	SI	set identification input (SECAM, PAL, PAL-M)
4	FH3	400 Hz (PAL); 360 HZ (NTSC, PAL-M) and $f_H/3$ (SECAM)
5	X	standard programming input
6	Y	standard programming input
7	FD	standard programming input
8	FH80	80 x f_H output (1,25 MHz)
9	VCR	VCR standard input
10	OSCO	oscillator output
11	OSCI	oscillator input
12	PH	phase detector output
13	NS	no-sync detector output
14	V_{SS}	negative supply voltage (ground)
15	ECS	external composite sync input
16	RI	vertical identification output
17	WMP	white measurement pulse output
18	RR	vertical reset input
19	V1	vertical drive output
20	V2	vertical drive output
21	CLP	clamp pulse output
22	DL	2 x f_H input/output
23	H1	horizontal drive output
24	H2	horizontal drive output
25	CB	composite blanking output
26	CS	composite sync output
27	ID	SECAM identification output
28	V_{DD}	positive supply voltage

FUNCTIONAL DESCRIPTION

Sync pulse generation

Programming of operating standard

The standard required for operation is programmed using the inputs X, Y and FD as shown in Table 1. The FD input selects 525 or 625-line working of the vertical counter (524 or 624-lines for video game standards) and also influences the choice of oscillator frequency as shown in Table 2.

Table 1 Programming of operating standard

standard	FD	X	Y
SECAM 1	0	0	0
SECAM 2	0	0	1
624	0	1	0
PAL/CCIR	0	1	1
NTSC 1	1	0	0
NTSC 2	1	0	1
524	1	1	0
PAL-M	1	1	1

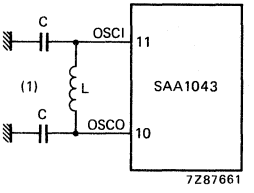
positive logic: 1 = HIGH; 0 = LOW

Oscillator

The built-in oscillator of the SAA1043 functions with an external LC-circuit (Fig. 3) or with a crystal of the parallel resonance type (Fig. 4). For operation in the VCR mode the LC oscillator circuit is recommended. The frequencies required for the operating standards are shown in Table 2.

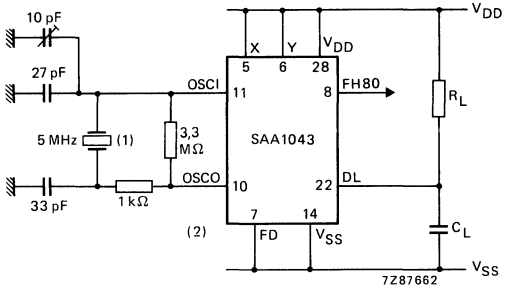
Table 2 Oscillator input frequencies

operating standard	osc. frequency (f_{OSCI}) MHz	vertical divider (FD)	vertical frequency (f_V) Hz	horizontal frequency (f_H) Hz
PAL, SECAM, 624	5,0	0	50	15625
NTSC, PAL-M, 524	5,034964	1	59,94	15734,26
PAL, SECAM, 624	2,5	H2 (pin 24)	50	15625
NTSC, PAL-M, 524	2,501748	H1 (pin 23)	59,94	15734,26



(1) Component values can be calculated from the formula $f_{OSCI} = 1/2\pi\sqrt{LC_v}$ where $C_v = C/2 + C_p$ and C_p = parasitic capacitance of typically 5 pF.

Fig. 3 LC oscillator circuit.



(1) Catalogue number of crystal: 8222 298 40760.

(2) All inputs not shown are at V_{SS}.

Fig. 4 Crystal oscillator circuit showing test set-up for oscillator frequency measurement.

DEVELOPMENT DATA

Synchronization to an external sync signal

Use is made of the phase comparator output PH to lock the internally generated sync pulses to an external sync signal. Reset pulses derived at each falling edge of the external sync signal (ECS) reset the the sync counter which is clocked at the internal horizontal frequency by the horizontal counter. At each horizontal scan period the sync counter opens the sync pulse gate and allows the ECS to be applied to the phase comparator where it is compared with the phase of the internally generated horizontal sync pulse. When the two signals are in phase the output PH is in a high impedance state. When a phase difference exists PH is pulled towards V_{DD} or V_{SS} depending on the direction of the error (Fig. 5). The phase-analogue voltage on PH is used to correct the frequency at OSCI via a voltage-controlled oscillator and null the phase error between internal and external signals. Pulses occurring on the ECS outside of the sync pulse gating time (serration and equalization pulses) do not effect the phase comparator.

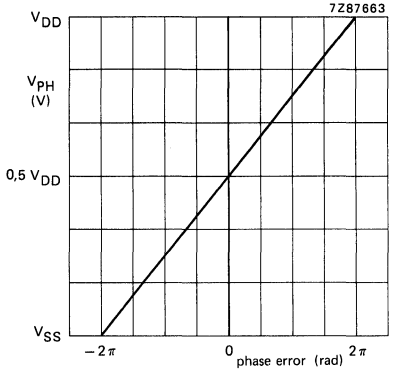


Fig. 5 Phase comparator characteristic.

FUNCTIONAL DESCRIPTION (continued)

Synchronization to an external sync signal (continued)

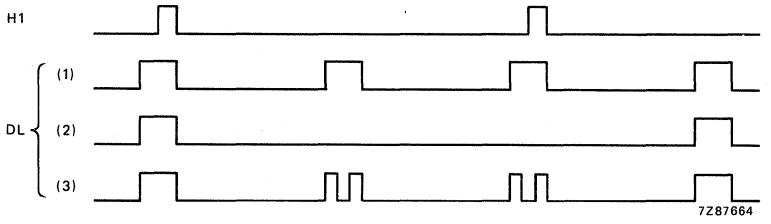
The circuit will lock to standard and non-standard sync signals. With standard signals the resetting of the sync counter is permitted after 3/4 of the horizontal scan period and if one reset pulse is missed the next pulse will reset the counter. With non-standard signals a narrow reset window is imposed to avoid disturbances which would otherwise be visible on the screen during vertical blanking time. The width of this window is $64 - 15{,}2 <$ reset time $< 64 + 15{,}2\ \mu s$. If a reset pulse does not occur within this window the same window timing is specified for the next horizontal scan.

A no-sync signal is generated by the sync pulse gate if the sync counter is not reset from the ECS. The no-sync signal (NS) occurs 6,4 μs after the time of the missing reset pulse.

Detection of the vertical sync in the ECS is performed using a double sampling method which minimizes detection failures. Vertical lock is performed by comparing the internal vertical sync with a pulse derived from the ECS and using the result to modify the period of the vertical counter. This is achieved by manipulating the DL ($2 \times f_H$) input to the vertical counter via the addition/subtraction logic. The DL puises are added or suppressed to bring the circuit into lock in the shortest possible time; the direction taken is determined by a logic decision based on the half picture in which the ECS derived pulse occurred.

Use in non-standard systems

For systems requiring a non-standard horizontal frequency the number of horizontal scans per picture can be manipulated using the open drain input/output DL. The addition or suppression of pulses during the high ohmic period of DL modifies the vertical counter value. The suppression of two DL pulses per half picture will give one extra horizontal scan and the addition of two DL pulses will remove one horizontal scan from the half picture (see Fig. 6).



(1) Normal waveform at DL; $f_{DL} = 2 \times f_H$.

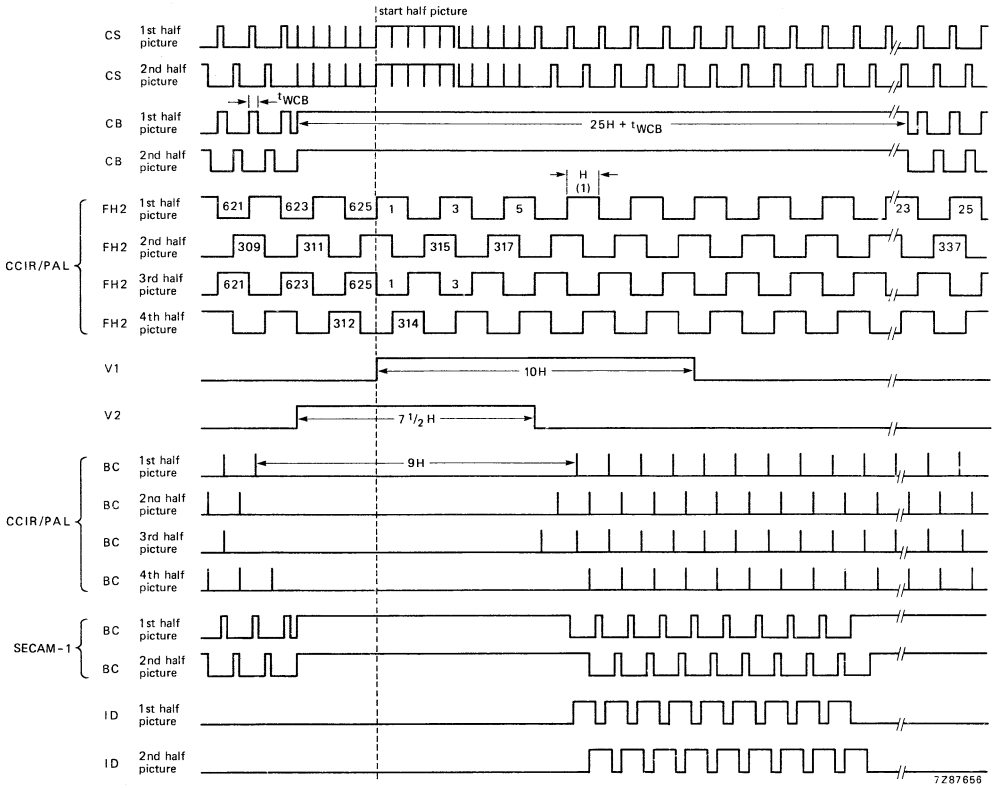
(2) Waveform at DL with two pulses suppressed increases the number of horizontal scans per half picture by 1.

(3) Waveform at DL with two additional pulses decreases the number of horizontal scans per half picture by 1.

Fig. 6 Manipulation of the horizontal frequency for non-standard systems.

Output waveforms

The output waveforms for the different modes of operation are shown in Figs 7 and 8.

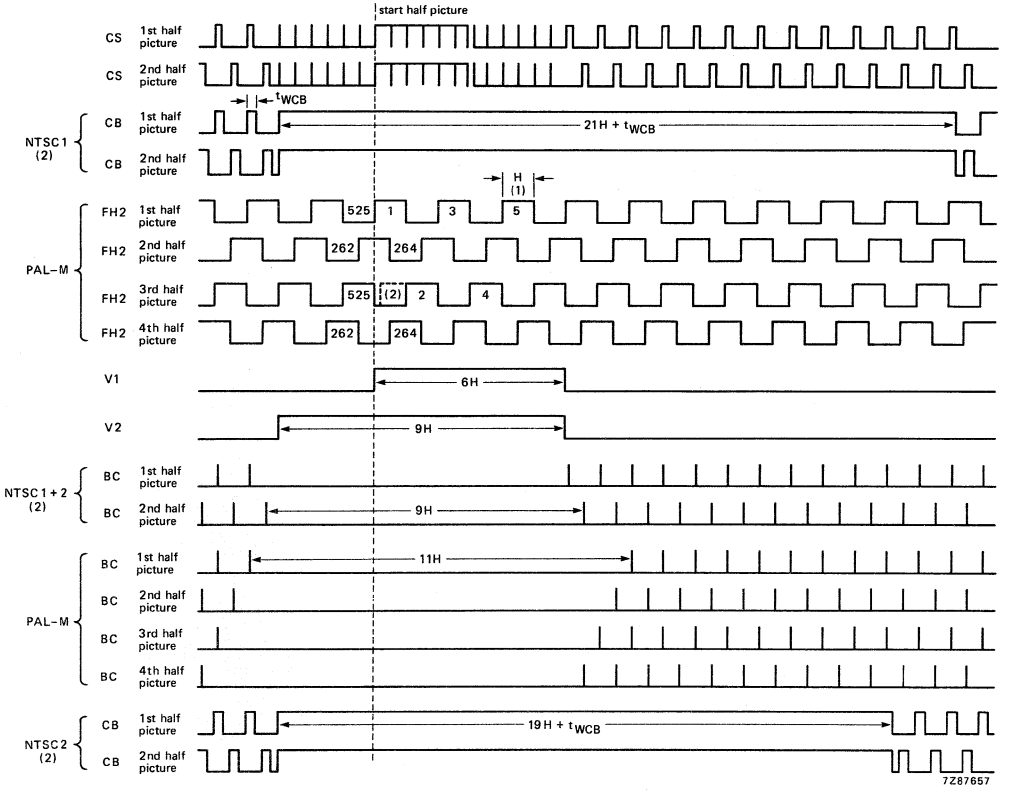


(1) H = 1 horizontal scan.

Fig. 7 Typical output waveforms for PAL/CCIR and SECAM. In the 624-line mode the output waveforms are identical to the 1st half picture of PAL/CCIR and are not interlaced (0,5H subtracted from the waveform timing).

FUNCTIONAL DESCRIPTION (continued)

Output waveforms (continued)



(1) H = 1 horizontal scan.

(2) NTSC mode reset; the 4th half picture is identical to the 2nd half picture for NTSC.

Fig. 8 Typical output waveforms for NTSC and PAL-M. In the 524-line mode the output waveforms are identical to the 1st half picture of NTSC and are not interlaced (0,5H subtracted from the waveform timing).

DEVELOPMENT DATA

WAVEFORM TIMING (Table 3, Figs 9 and 10)

The waveform timing depends on the frequency of the oscillator input (f_{OSCI}). This is shown in Table 3 as the number (n) of oscillations at OSCI. The timings given are derived from n x t_{OSCI} ± 100 ns. One horizontal scan (H) = 320 x t_{OSCI} = $1/f_H$. Note that the number of horizontal scans per half picture can be modified for non-standard systems using input/output DL as shown in Fig. 6.

Table 3 Waveform timing

parameter	symbol	PAL	NTSC	PAL-M	SECAM	unit	n
CS							
Horizontal sync pulse width	t_{WSC1}	4,8	4,77	4,77	4,8	µs	24
Equalizing pulse width	t_{WSC2}	2,4	2,38	2,38	2,4	µs	8
Serration pulse width	t_{WSC3}	4,8	4,77	4,77	4,8	µs	24
Duration of pre-equalizing pulses	–	2,5	3	3	2,5	H	
Duration of post-equalizing pulses	–	2,5	3	3	2,5	H	
Duration of serration pulses	–	2,5	3	3,5	2,5	H	
CB							
Horizontal blanking pulse width							
PAL/SECAM/PAL-M	t_{WCB}	12	–	11,12	12	µs	60
NTSC 1	t_{WCB}	–	11,12	–	–	µs	56
NTSC 2	t_{WCB}	–	10,53*	–	–	µs	53
Front porch	t_{PCBCS}	1,6	1,59	1,59	1,6	µs	8
Duration of vertical blanking							
PAL/SECAM/PAL-M		25H+t_{WCB}	–	21H+t_{WCB}	25H+t_{WCB}		
NTSC 1		–	21H+t_{WCB}	–	–		
NTSC 2		–	19H+t_{WCB}	–	–		
BC (PAL)							
Burst key pulse width	t_{WBC}	2,4	2,38	2,38	–	µs	12
Sync to burst delay	t_{PCSBC}	5,6	5,56	5,76	–	µs	28
Burst suppression	–	9	9	11	–	H	
Position of burst suppression: 1st half picture	–	H623 to H6	H523 to H6	H523 to H8	–	–	
2nd half picture	–	H310 to H318	H261 to H269	H260 to H270	–	–	
3rd half picture	–	H622 to H5	H523 to H6	H522 to H7	–	–	
4th half picture	–	H311 to H319	H261 to H269	H259 to H269	–	–	

WAVEFORM TIMING (continued)

Table 3 (continued)

parameter	symbol	PAL	NTSC	PAL-M	SECAM	unit	n
BC (SECAM)							
Chroma pulse width	t_{WBC}	–	–	–	7,2	µs	36
Chroma to sync delay	t_{PBCCS}	–	–	–	1,6	µs	8
Duration of vertical blanking: SECAM 1	1st half picture: 25H + t_{WBC} except H320 to H328 2nd half picture: 24,5H + t_{WBC} except H7 to H15						
SECAM 2	1st half picture: 25H + t_{WBC} 2nd half picture: 24,5H + t_{WBC}						
CLP							
Clamp pulse width	t_{WCLP}	2,4	2,38	2,38	2,4	µs	12
Sync to clamp delay	t_{PCSCLP}	2,4	2,38	2,38	2,4	µs	12
DL							
Frequency	f_{DL}	2 x f_H	2 x f_H	2 x f_H	2 x f_H	–	
Pulse width	t_{WDL}	9,6	9,53	9,53	9,6	µs	48
DL to sync delay	t_{PCLCS}	5,6	5,56	5,56	5,6	µs	28
FH80							
Frequency	f_{FH80}	80 x f_H	80 x f_H	80 x f_H	80 x f_H	–	
Sync to FH80 delay	–	0,2	0,2	0,2	0,2	µs	1
H1, H2							
H1 pulse width	t_{WH1}	7,2	7,15	7,15	7,2	µs	36
H2 pulse width	t_{WH2}	7,2	7,15	7,15	7,2	µs	36
H1 to sync delay	t_{PH1CS}	0,8	0,79	0,79	0,8	µs	4
Sync to H2 delay	t_{PCSH2}	0,8	0,79	0,79	0,8	µs	4
Repetition period	–	64	63,56	63,56	64	µs	
V1, V2							
V1 duration	–	10	6	6	10	H	
V2 duration	–	7,5	9	9	7,5	H	
V1 to sync delay	t_{PV1CS}	1,6	1,59	1,59	1,6	µs	8
Sync to V2 delay	t_{PV2CS}	1,6	1,59	1,59	1,6	µs	8
FH2							
Frequency	f_{FH2}	$f_H/2$	$f_H/2$	$f_H/2$	$f_H/2$	–	
Sync to FH2 delay	–	0	0	0	0	µs	
FH3							
Frequency	f_{FH3}	400	360	360	$f_H/3$	–	
Sync to FH3 delay	–	–	–	–	0	µs	

parameter	symbol	PAL	NTSC	PAL-M	SECAM	unit	n
WMP							
WMP pulse width	–	2,4	2,38	2,38	2,4	μs	12
Sync to WMP delay	–	34,4	34,16	34,16	34,4	μs	172
Duration of WMP	–	10	9	9	10	H	
Position of WMP							
1st half picture:	–	H163 to H173	H134 to H143	H134 to H143	H163 to H173	– –	
2nd half picture:	–	H475 to H485	H396 to H405	H396 to H405	H475 to H485	– –	
RI							
Frequency	–	$f_V/2$	$f_V/2$	$f_V/2$	$10f_H$	–	
Position of edges	–	H6 and H318	H7 and H269	H7 and H269	–	–	
ID							
ID pulse width	t_{WID}	12,0	11,12	11,12	12,0	μs	60
ID to sync delay	t_{PIDCS}	1,6	1,59	1,59	1,6	μs	8
Position of ID							
1st half picture:	–	H7 to H15	H8 to H22	H8 to H22	H7 to H15	–	
2nd half picture:	–	H320 to H328	H271 to H285	H271 to H285	H320 to H328	– –	

DEVELOPMENT DATA

* Horizontal blanking pulse width for NTSC 2 can be 11, 12 μs maximum.

WAVEFORM TIMING (continued)

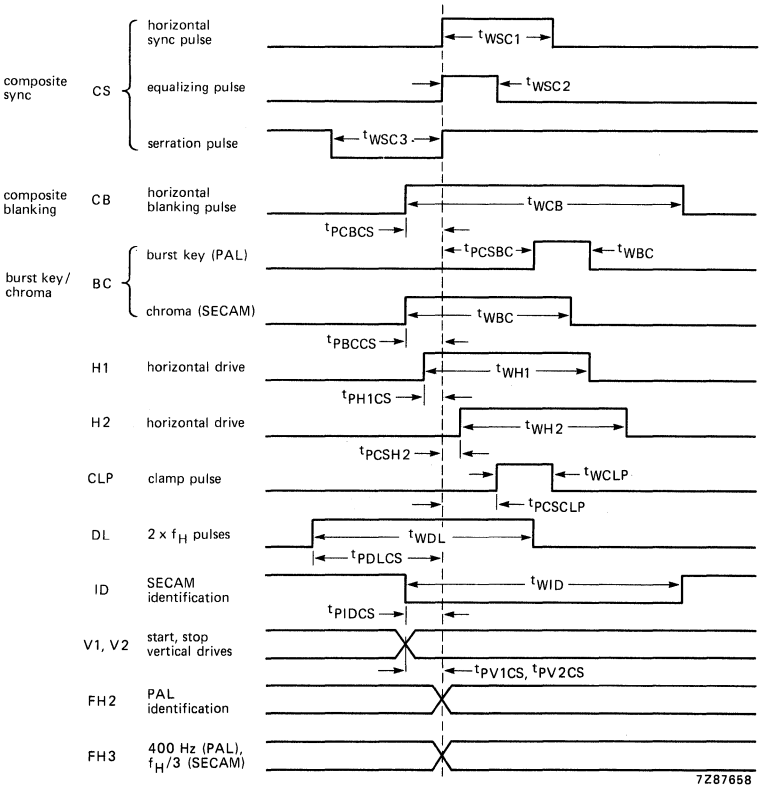


Fig. 9 Waveform timings: PAL/CCIR; SECAM; 624-line modes.

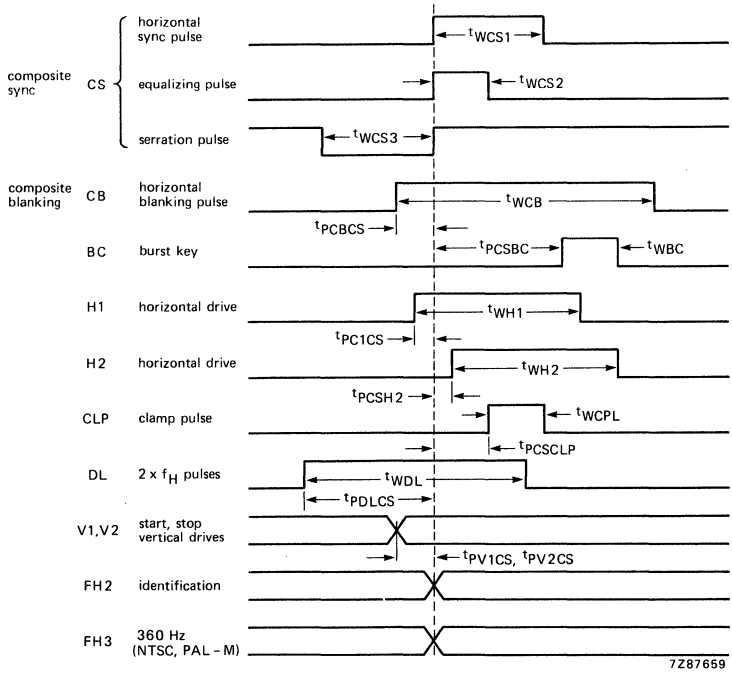


Fig. 10 Waveform timings: NTSC; PAL-M; 524-line modes.

DEVELOPMENT DATA

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range with respect to V_{SS}	V_{DD}		−0,5 to + 15	V
Input voltage range	V_I		−0,5 to (V_{DD} + 0,5)*	V
Input current	$\pm I_I$	max.	10	mA
Output voltage range	V_O		−0,5 to (V_{DD} + 0,5)*	V
Output current	$\pm I_O$	max.	10	mA
Power dissipation per output	P_O	max.	100	mW
Total power dissipation per package	P_{tot}	max.	200	mW
Operating ambient temperature range	T_{amb}		−25 to + 70	°C
Storage temperature range	T_{stg}		−55 to + 150	°C

* V_{DD} + 0,5 V not to exceed 15 V.

CHARACTERISTICS

V_{DD} = 5,7 to 7,5 V; V_{SS} = 0 V; T_{amb} = −25 to + 70 °C unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supplies					
Supply voltage	V_{DD}	5,7	–	7,5	V
Supply current (quiescent) at I_O = 0 mA at all outputs; V_{DD} = 7,5 V; T_{amb} = 25 °C	I_{DD}	–	–	10	μA
Inputs					
Input voltage HIGH	V_{IH}	0,7 x V_{DD}	–	V_{DD}	V
Input voltage LOW	V_{IL}	0	–	0,3 x V_{DD}	V
Input leakage current at V_I = 7,5 V; V_{DD} = 7,5 V; T_{amb} = 25 °V	I_{IR}	–	–	1	μA
Input leakage current at V_I = 0 V; V_{DD} = 7,5 V; T_{amb} = 25 °C	$-I_{IR}$	–	–	1	μA
Outputs (except PH and OSC0)					
Output voltage HIGH at $-I_{OH}$ = 0,5 mA	V_{OH}	V_{DD} − 0,5	–	–	V
Output voltage LOW at I_{OL} = 0,5 mA	V_{OL}	–	–	0,4	V
Output PH					
Output voltage HIGH at $-I_{OH}$ = 0,9 mA	V_{OH}	V_{DD} − 0,5	–	–	V
Output voltage LOW at I_{OL} = 1,0 mA	V_{OL}	–	–	0,4	V
Output leakage current at V_O = 7,5 V; V_{DD} = 7,5 V	I_{OR}	–	–	5	μA
Output leakage current at V_O = 7,5 V; V_{DD} = 7,5 V; T_{amb} = 25 °C	I_{OR}	–	–	1	μA
Output leakage current at V_O = 0 V; V_{DD} = 7,5 V	$-I_{OR}$	–	–	5	μA
Output leakage current at V_O = 0 V; V_{DD} = 7,5 V; T_{amb} = 25 °C	$-I_{OR}$	–	–	1	μA
Output OSCO					
Output voltage HIGH at V_{OSCI} = 0 V; $-I_{OH}$ = 0,9 mA	V_{OH}	V_{DD} - 0,5	–	–	V
Output voltage LOW at V_{OSCI} = V_{DD}; I_{OL} = 1,0 mA	V_{OL}	–	–	0,4	V

parameter	symbol	min.	typ.	max.	unit
Input/output DL (open drain)*					
Output voltage LOW at I_{OL} = 1,0 mA	V_{OL}	–	–	0,4	V
Output leakage current at V_O = 7,5 V; V_{DD} = 7,5 V	I_{OR}	–	–	5	μA
Output leakage current at V_O = 7,5 V; V_{DD} = 7,5 V; T_{amb} = 25 °C	I_{OR}	–	–	1	μA
Load resistance (Fig. 4)					
at V_{DD} = 5,7 V	R_L	1,4	–	–	kΩ
at V_{DD} = 7,5 V	R_L	0,82	–	–	kΩ
Time constant (Fig. 4)					
at V_{DD} = 5,7 V	R_LC_L	–	–	19	ns
at V_{DD} = 7,5 V	R_LC_L	–	–	13	ns
Oscillator frequency (Fig. 4)					
Maximum oscillator frequency at V_{DD} = 5,7 V	f_{OSCI}	5,1	–	–	MHz

DEVELOPMENT DATA

* An external pull-up resistor (3,9 kΩ) must be connected between DL and V_{DD}. The time constant R_LC_L must not exceed the values given.

APPLICATION INFORMATION

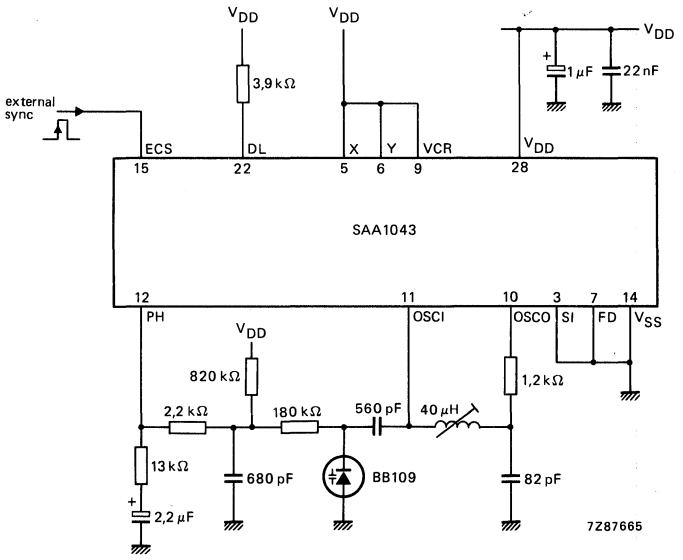


Fig. 11 Synchronizing circuit using passive filter network.

HANDLING

Inputs and outputs are protected against electrostatic charge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see 'Handling MOS Devices').

SUBCARRIER COUPLER

GENERAL DESCRIPTION

The SAA1044 maintains the correct relationship between subcarrier and horizontal scan frequencies when an exact coupling is required. It is for use in combination with sync generator SAA1043 for application in colour video sources (cameras, film-scanners and similar equipments).

Features

- Provides exact relationship between subcarrier and horizontal scan frequencies
- Accommodates all standard frequencies
- Facilitates GENLOCK (general locking) applications

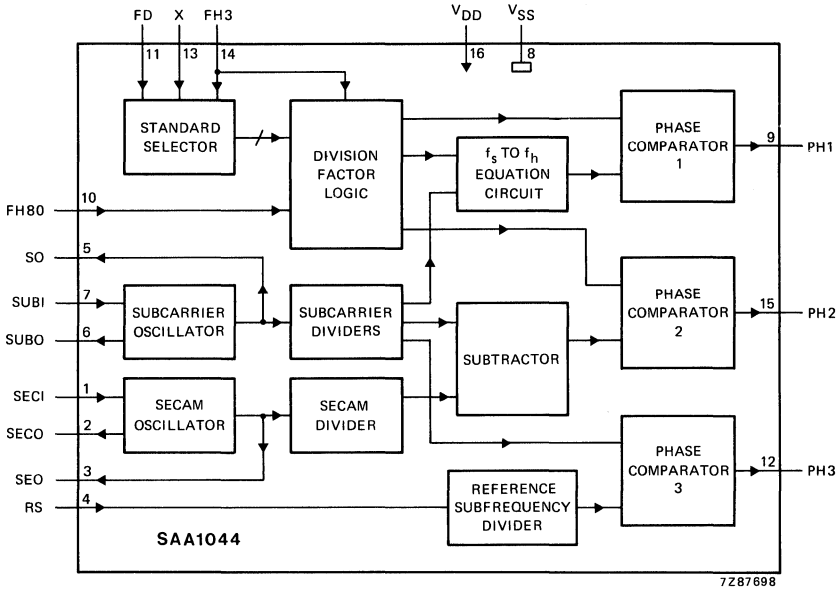


Fig. 1 Block diagram.

PACKAGE OUTLINE

16-lead DIL; plastic (SOT-38).

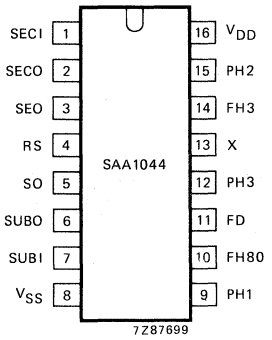


Fig. 2 Pinning diagram.

PINNING

1	SECI	SECAM oscillator input ($272f_H$)
2	SECO	SECAM oscillator output ($272f_H$)
3	SEO	inverted SECAM oscillator output
4	RS	reference subfrequency
5	SO	inverted subcarrier oscillator output
6	SUBO	subcarrier oscillator output
7	SUBI	subcarrier oscillator input
8	V_{SS}	negative supply voltage (ground)
9	PH1	phase comparator 1 output (FH80/SUBI)
10	FH80	1,25 MHz input (from SAA1043)
11	FD	standard programming input
12	PH3	phase comparator 3 output (RS/SUBI)
13	X	standard programming input
14	FH3	standard programming input (from SAA1043)
15	PH2	phase comparator 2 output (SECI/FH80)
16	V_{DD}	positive supply voltage

FUNCTIONAL DESCRIPTION

Programming of operating standard

The standard required for operation is programmed using the inputs FD, X and FH3 as shown in Table 1.

Table 1 Programming of operating standard

standard	FD	X	FH3	relationship of subcarrier frequency (f_S) to horizontal scan frequency (f_H)
PAL	0	1	400 Hz	$f_S = 283{,}7516f_H$
SECAM	0	0	don't care	$f_S = 282f_H$
PAL-N	1	1	400 Hz	$f_S = 229{,}2516f_H$
PAL-M	1	0	1	$f_S = 227{,}25f_H$
NTSC	1	0	0	$f_S = 227{,}5f_H$

Positive logic: 1 = HIGH; 0 = LOW

Subcarrier/horizontal scan frequency relationship

The input FH80 from SAA1043 is the reference for horizontal scan frequency (f_H). This frequency is reduced by a factor determined by the selected operating standard to give a value of $8f_H$ (PAL, SECAM) or $10f_H$ (PAL-N, PAL-M, NTSC) to phase comparator 1. The subcarrier frequency (f_S) is manipulated to provide a comparable value at the second input to the phase comparator. When the frequencies of the two inputs to phase comparator 1 are equal, the relationship between f_H and f_S is as shown in Table 1.

Phase comparator 1 functions with an exclusive-OR phase detector circuit and provides an output which may be used to control a voltage-controlled oscillator (VCO) via a low-pass filter. The VCO reference can be the subcarrier or the horizontal scan frequency and the filter can be active or passive, depending on application.

A second subcarrier oscillator circuit is provided for SECAM operation. The operating frequency of this is centred on $272f_H$ to give, when $f_S = 282f_H$, comparable values of $5f_H$ at the two inputs to phase comparator 2. A second VCO loop can be used to control the SECAM oscillator frequency.

The high degrees of accuracy and stability required for GENLOCK applications are met by phase comparator 3. This compares the internal subcarrier and external reference frequencies. To adjust the phase over 2π, this comparator has a linear characteristic over 4π. The output signal PH3 has a period time of $f_S/4$ and a duty cycle of between 12,5% and 62,5% giving a sensitivity of 240 mV/rad. Errors due to temperature variation are minimized by symmetrical circuit and chip design.

DEVELOPMENT DATA

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range with respect to V_{SS}	V_{DD}		−0,5 to + 15	V
Input voltage range	V_I		−0,5 to (V_{DD} + 0,5)*	V
Input current	$\pm I_I$	max.	10	mA
Output voltage range	V_O		−0,5 to (V_{DD} + 0,5)*	V
Output current	$\pm I_O$	max.	10	mA
Power dissipation per output	P_O	max.	100	mW
Total power dissipation per package	P_{tot}	max.	200	mW
Operating ambient temperature range	T_{amb}		−25 to + 70	°C
Storage temperature range	T_{stg}		−55 to + 150	°C

HANDLING

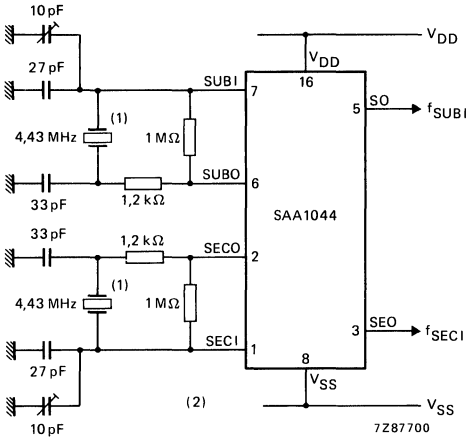
Inputs and outputs are protected against electrostatic charge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see 'Handling MOS Devices').

* V_{DD} + 0,5 V not to exceed 15 V.

CHARACTERISTICS

V_{DD} = 5,7 to 7,5 V; V_{SS} = 0 V; T_{amb} = −25 to + 70 °C unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supplies					
Supply voltage	V_{DD}	5,7	–	7,5	V
Supply current (quiescent) at I_O = 0 mA at all outputs; V_{DD} = 7,5 V; T_{amb} = 25 °C	I_{DD}	–	–	10	μA
Inputs					
Input voltage HIGH	V_{IH}	0,7 x V_{DD}	–	V_{DD}	V
Input voltage LOW	V_{IL}	0	–	0,3 x V_{DD}	V
Input leakage current at V_I = 7,5 V; V_{DD} = 7,5 V; T_{amb} = 25 °C	I_{IR}	–	–	1	μA
Input leakage current at V_I = 0 V; V_{DD} = 7,5 V; T_{amb} = 25 °C	$-I_{IR}$	–	–	1	μA
Outputs (except SECO and SUBO)					
Output voltage HIGH at $-I_{OH}$ = 0,5 mA	V_{OH}	V_{DD} −0,5	–	–	V
Output voltage LOW at I_{OL} = 0,5 mA	V_{OL}	–	–	0,4	V
Outputs SECO and SUBO					
Output voltage HIGH at $-I_{OH}$ = 0,9 mA	V_{OH}	V_{DD} −0,5	–	–	V
Output voltage LOW at I_{OL} = 1,0 mA	V_{OL}	–	–	0,4	V
Oscillator frequency (Fig. 3)					
Maximum oscillator frequency at V_{DD} = 5,7 V	f_{SUBI} } f_{SECI} }	5,1	–	–	MHz

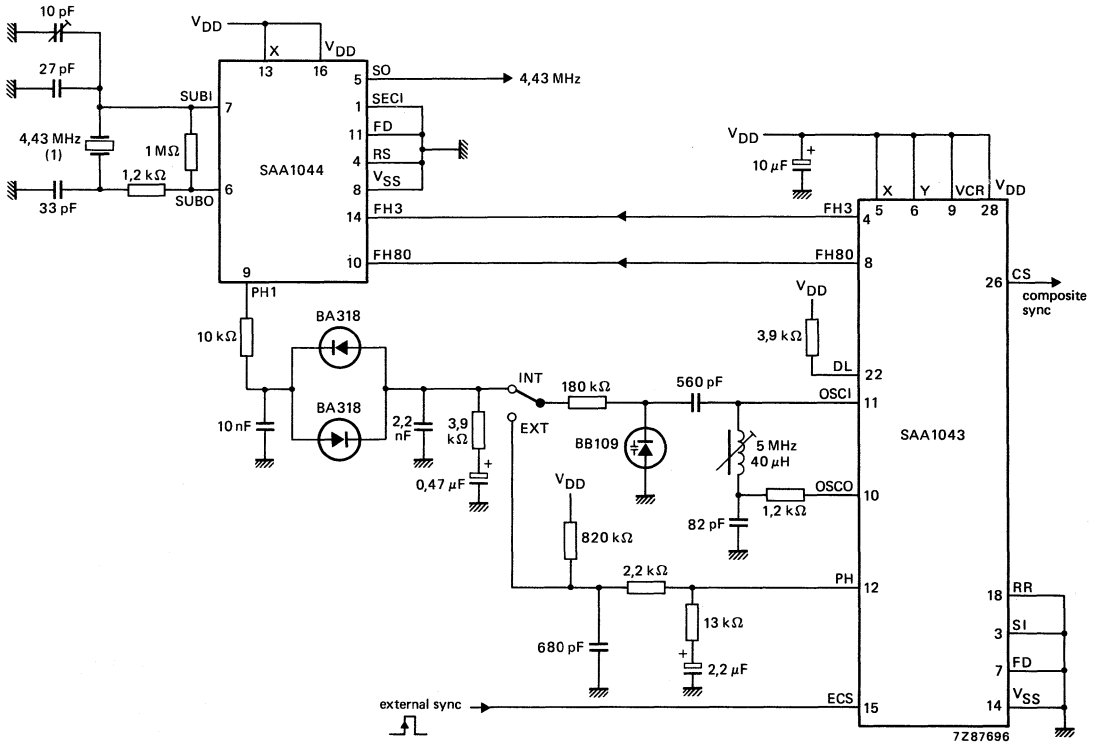


(1) Catalogue number of crystal: 4322 143 04040.
(2) Inputs not shown are don't care.

Fig. 3 Test set-up for oscillator frequency measurement.

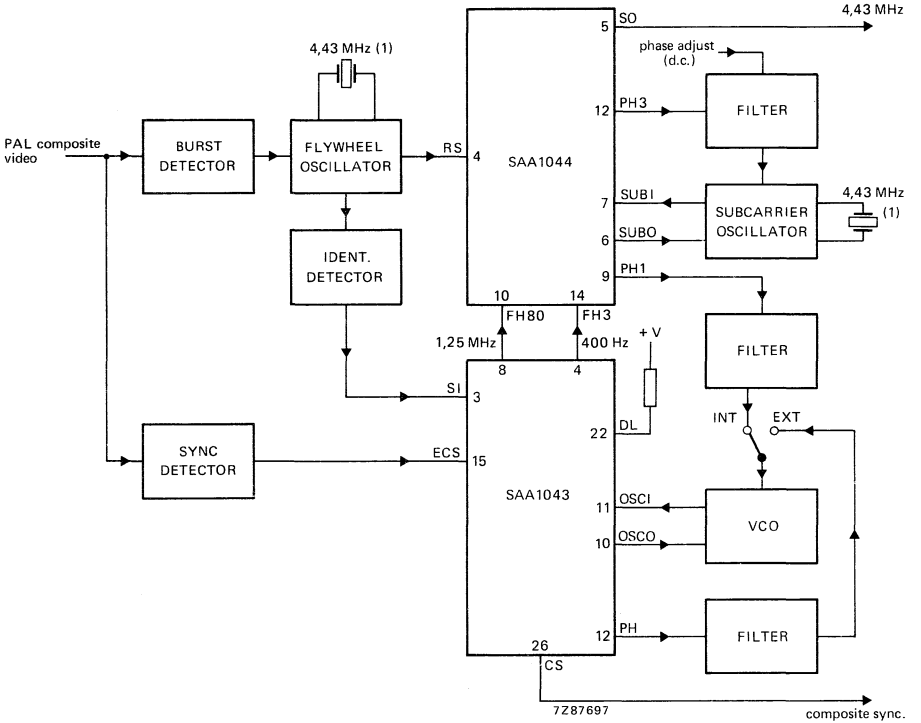
DEVELOPMENT DATA

APPLICATION INFORMATION



(1) Catalogue number of crystal: 4322 143 04040.

Fig. 4 Subcarrier coupling for PAL application; external synchronization is selected with switch in EXT condition.



(1) Catalogue number of crystal: 4322 143 04040.

Fig. 5 Subcarrier coupling for PAL GENLOCK application.

PLL FREQUENCY SYNTHESIZER

The integrated circuit SAA1056P together with a suitable prescaler (e.g. SAA1059) and a loop filter forms a complete PLL frequency synthesizer for AM/FM radio tuning systems.

Features

- Bus control for the selection of 17-bit words.
- 17-bit latch, for data storage.
- Control lines TTL compatible by means of level shifters.
- Decoupled oscillator frequency output (system clock for other ICs).
- Choice of 4 reference frequencies.

QUICK REFERENCE DATA

Supply voltage ranges	V_{DD}	8 to 10 V
	V_{DDI}	4,5 to 5,5 V
Operating ambient temperature range	T_{amb}	−20 to +80 °C
Maximum input frequency	f_I	4 MHz

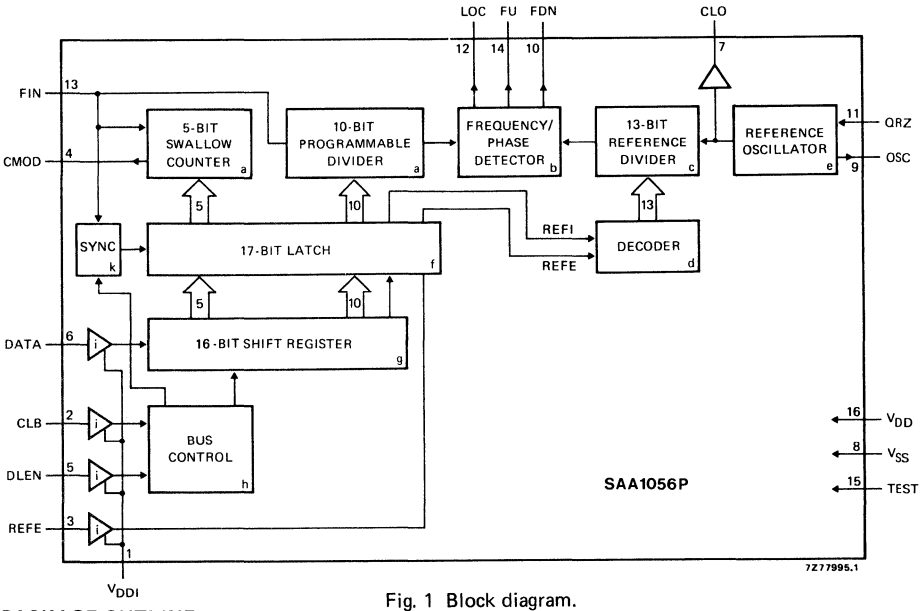


Fig. 1 Block diagram.

PACKAGE OUTLINE

16-lead DIL; plastic (SOT-38Z).

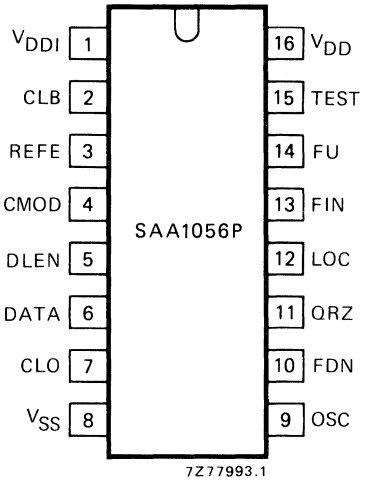


Fig. 2 Pinning diagram.

PINNING

16	V_{DD}	positive supply
8	V_{SS}	ground (0 V)
1	V_{DDI}	supply voltage for the level shifters

Inputs

13	FIN	input frequency; maximum 4 MHz	
6	DATA	data input	CBUS
2	CLB	clock burst	CBUS
5	DLEN	data line enable	CBUS
3	REFE	reference frequency selection	
11	QRZ	quartz crystal input (4 MHz)	

Outputs

4	CMOD	count mode output for prescaler
12	LOC	lock detector output
10	FDN	phase detector output; frequency down
14	FU	phase detector output; frequency up
7	CLO	system clock for other ICs (4 MHz)
9	OSC	quartz crystal oscillator output

GENERAL DESCRIPTION

The integrated circuit SAA1056P, together with a suitable prescaler (32/33) and loop-filter, forms a complete synthesizer function for AM/FM radio tuning systems.

The circuit comprises the following blocks:

a. A dividing circuit formed by a 5-bit binary Swallow counter and a 10-bit binary programmable divider.
b. A frequency/phase detector which, via an external loop-filter, generates the control voltage for the voltage-controlled oscillator (VCO). The detector also gives a lock indication.
c. A 13-bit binary reference frequency divider. This divider delivers the reference frequency to the frequency/phase detector.
d. The decoder delivers the dividing number for the reference divider. Depending on the logic state of the 2 inputs (REFI, REFE), four different dividing ratios (160, 400, 800 and 8000) for the reference frequencies can be fed to the frequency/phase detector.
e. A reference frequency oscillator. Together with a 4 MHz crystal a stable frequency is generated, from which the reference frequencies are derived. The 4 MHz signal is also available at a decoupled output as a system clock for other ICs.
f. A 17-bit latch to store the data for the dividing number of the programmable divider (block a) and 2 bits for reference frequency choice.
g. A 16-bit shift register to receive the serial data for the latch.
h. A bus control to protect the data transfer against interferences.
i. Level shifters for the control inputs DATA, DLEN, CLB and REFE so no external interface is necessary between the SAA1056P on 9 V and the other ICs on 5 V.
k. Synchronization circuit for loading the latches.

HANDLING

Inputs and outputs are protected against electrostatic charge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see 'Handling MOS Devices').

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range ($V_{DDI} < V_{DD}$)	V_{DD}		−0,3 to + 15	V
Input voltage range	V_I		−0,3 to + V_{DD}	V
Input current (d.c.)	$\pm I_I$	max.	10	mA
Output current (d.c.)	$\pm I_O$	max.	10	mA
Current from V_{DDI} to V_{DD} (d.c.)	I	max.	10	mA
Power dissipation per output	P_O	max.	100	mW
Total power dissipation per package	P_{tot}	max.	240	mW
Operating ambient temperature range	T_{amb}		−20 to + 80	°C
Storage temperature range	T_{stg}		−55 to + 150	°C

D.C. CHARACTERISTICS

V_{SS} = 0; T_{amb} = −20 to + 80 °C; unless otherwise specified

	V_{DD} V	symbol	min.	typ.	max.		conditions
Supply voltages	–	V_{DD}	8	9	10	V	
	–	V_{DDI}	4,5	5	5,5	V	
Supply current	10	I_{DD}	–	–	100	μA	I_O = 0; $V_I = V_{DD}$ or V_{DDI} or V_{SS}
Inputs without level shifters; FIN, QRZ, TEST							
input voltage LOW	8 to 10	V_{IL}	0	–	0,3 V_{DD}	V	
input voltage HIGH	8 to 10	V_{IH}	0,7 V_{DD}	–	V_{DD}	V	
input current HIGH	10	I_{IH}	–	–	1	μA	V_I = 10 V
input current LOW	10	$-I_{IL}$	–	–	1	μA	V_I = 0
Inputs with level shifters DATA, CLB, DLEN, REFE at V_{DDI} = 4,5 to 5,5 V							
input voltage LOW	8 to 10	V_{IL}	0	–	0,2 V_{DDI}	V	
input voltage HIGH	8 to 10	V_{IH}	0,8 V_{DDI}	–	V_{DDI}	V	
input current HIGH	10	I_{IH}	–	–	1	μA	$V_I = V_{DDI}$
input current LOW	10	$-I_{IL}$	–	–	1	μA	V_I = 0
Output CMOD open-drain, n-channel							
output voltage LOW	8 to 10	V_{OL}	–	–	0,5	V	I_{OL} = 5,5 mA
output leakage current	10	I_{OR}	–	–	20	μA	V_O = 10 V
Outputs LOC, FU, FDN							
output voltage HIGH	8 to 10	V_{OH}	V_{DD}−0,5	–	–	V	$-I_O$ = 2,5 mA
output voltage LOW	8 to 10	V_{OL}	–	–	0,5	V	I_O = 5,5 mA
Output OSC							
output voltage HIGH	8 to 10	V_{OH}	V_{DD}−1	–	–	V	$-I_O$ = 1,2 mA; QRZ at V_{SS}
output voltage LOW	8 to 10	V_{OL}	–	–	1	V	I_O = 2 mA; QRZ at V_{DD}
Output CLO							
output voltage HIGH	8 to 10	V_{OH}	V_{DD}−1	–	–	V	$-I_O$ = 1,2 mA
output voltage LOW	8 to 10	V_{OL}	–	–	1	V	I_O = 4 mA

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = −20 to + 80 °C; unless otherwise specified

	V_{DD} V	symbol	min.	typ.	max.	conditions
Inputs without level shifters; FIN, QRZ						
input frequency	8 to 10	f_i	4	–	– MHz	
duty factor	8 to 10	δ	45	–	55 %	
rise/fall time	8 to 10	t_r, t_f	–	–	50 ns	
Inputs with level shifter DATA, CLB, DLEN, REFE						
rise/fall time	8 to 10	t_r, t_f	–	–	1 μs	
pulse width	–	t_{WH}, t_{WL}	500	–	– ns	at 0,8 x V_{DD} resp. 0,2 x V_{DD} levels
Output CMOD open-drain, n-channel						
fall time	8 to 10	t_f	–	–	20 ns	C_L = 25 pF; R_L = 1,2 kΩ ± 20%
Output CLO						
pulse period	8 to 10	T	250	–	– ns	see Figs 3 and 4
pulse width HIGH	–	t_{WH}	90	–	– ns	
pulse width LOW	–	t_{WL}	90	–	– ns	
Output LOC, FU, FDN rise/fall time	8 to 10	t_r, t_f	–	–	20 ns	C_L = 25 pF; R_L = 10 kΩ ± 10%

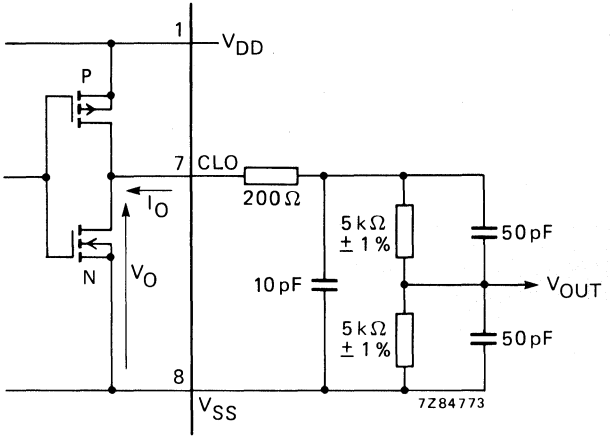


Fig. 3 Output CLO test circuit.

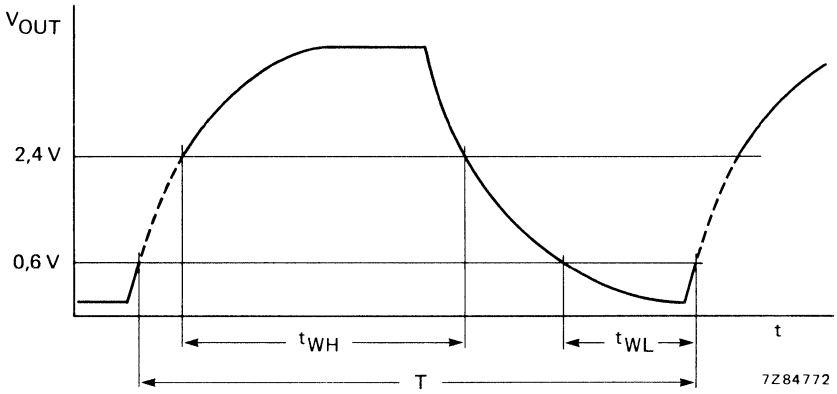


Fig. 4 Output voltage (V_{OUT}) of Fig. 3 as a function of time.

OPERATION DESCRIPTION

Data inputs (DLEN and DATA)

The SAA1056P accepts the serial 17-bit data word synchronized with the clock burst (CLB), are offered at the data input DATA. However, a command is accepted only when the data line enable input DLEN is HIGH at the same time.

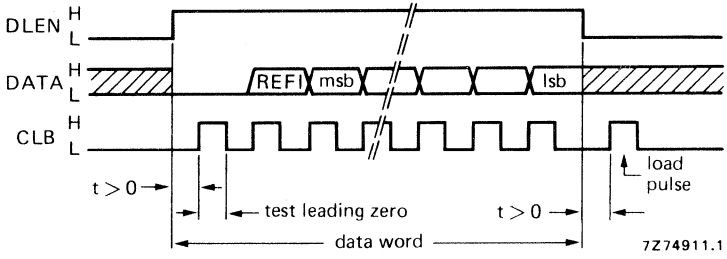


Fig. 5 Pulse diagram of the 17-bit data word.

OPERATION DESCRIPTION (continued)

Each data word must start with a leading zero. The SAA1056P checks the data word for the correct length (17 bits) including leading zero. The data word contains 15 bits as a binary coded ratio for the programmable divider. The first 10 bits program the 10-bit programmable divider and the next 5 bits program the Swallow counter (see Fig. 6). The 16th bit (REFI) determines the ratio of the reference divider in conjunction with the logic signal at input REFE.

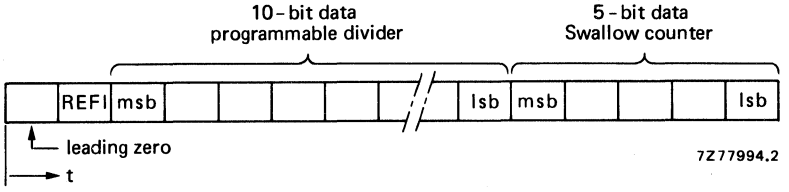


Fig. 6 Organization of a data word.

Setting the reference divider (input REFE and control-bit REFI)

The reference divider can be set to four different ratios, using the two signals REFE and REFI.

control bit REFI	input REFE	dividing ratio N_{ref}	reference frequency at f_{osc} = 4 MHz; f_{ref}
1	1	160	25 kHz
1	0	400	10 kHz
0	1	800	5 kHz
0	0	8000	0,5 kHz

Input frequency divider (FIN)

The input frequency is applied to input FIN for further processing in the circuit. It is divided in the Swallow counter and the 10-bit programmable divider corresponding to the received data word. The division ratio of the dividing circuit is given by the following equation:

$N = N_S + P \times N_P$ with: $N_P \leqslant N_S$; $0 \leqslant N_S \leqslant 31$

in which:

N = division ratio of total divider
N_S = value for the Swallow counter
P = lowest division ratio of prescaler
N_P = division ratio of the 10-bit programmable divider.

In combination with the 32/33 divider (SAA1059), the minimum and maximum dividing number can be calculated:

$$N_{min} = 0 + 32 \times 31 = 992$$
$$N_{max} = 31 + 32 \times 1023 = 32\,767$$

Count mode output for prescaler (CMOD)

Depending on the received data word, the 5-bit Swallow counter generates a signal for setting the prescaler.

0 = divide by low dividing number
1 = divide by high dividing number.

The signal appears about 150 ns after the input pulse FIN (see Fig. 7).

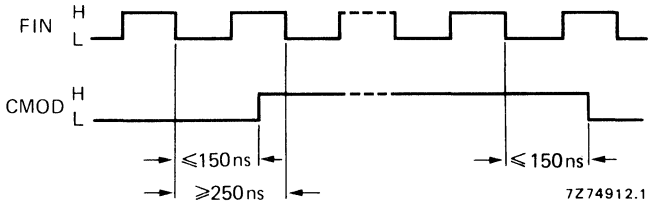


Fig. 7 Timing of the CMOD signal.

Phase detector (frequency up/down) and lock detector outputs (FDN, FU, LOC)

The frequency/phase detector outputs FDN and FU generate a control voltage via an external loop for the voltage-controlled oscillator (VCO).

FDN: phase detector output, frequency down
0 = active
1 = inactive

FU: phase detector output, frequency up
0 = inactive
1 = active

Output LOC generates an extra signal if the loop is locked.
0 = loop unlocked
1 = loop locked.

APPLICATION INFORMATION

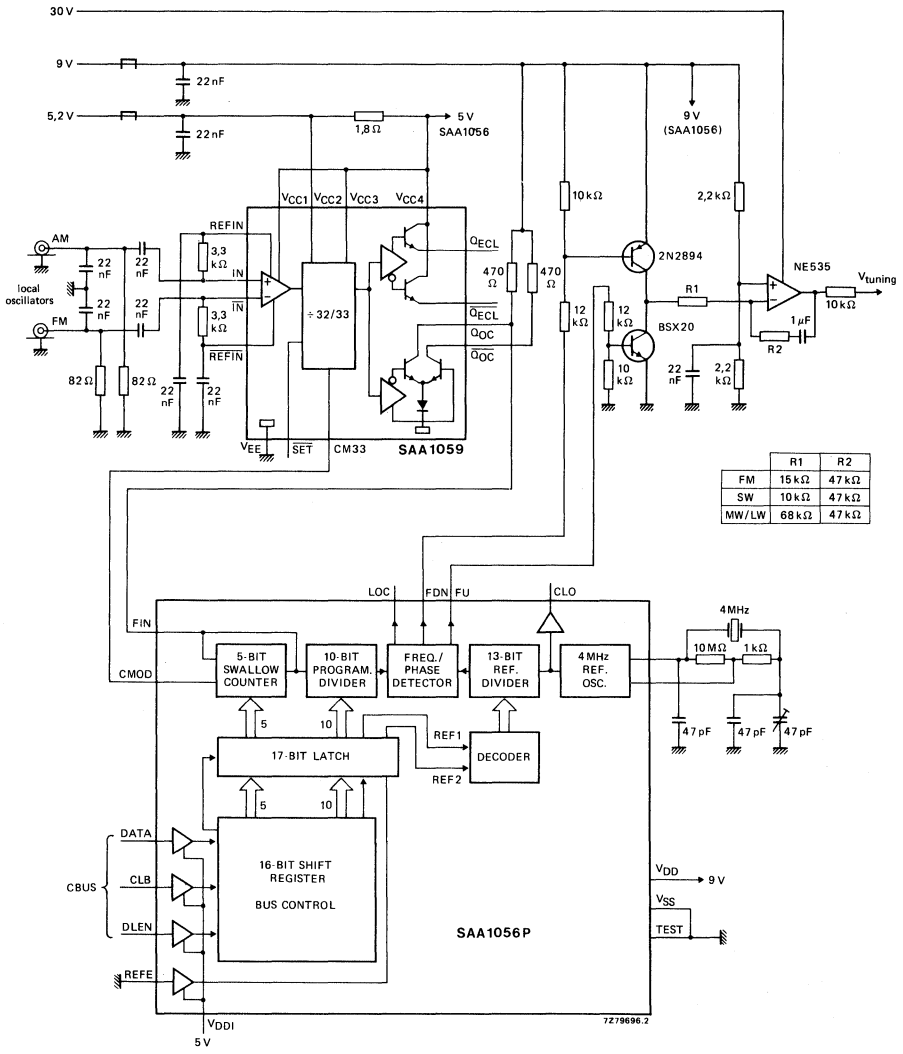


Fig. 8 A practical digital frequency synthesizer for a radio receiver.

RADIO TUNING PLL FREQUENCY SYNTHESIZER

The SAA1057 is a single chip frequency synthesizer IC in I^2L technology, which performs all the tuning functions of a PLL radio tuning system. The IC is applicable to all types of radio receivers, e.g. car radios, hi-fi radios and portable radios.

Features

- On-chip prescaler with up to 120 MHz input frequency.
- On-chip AM and FM input amplifiers with high sensitivity (30 mV and 10 mV respectively).
- Low current drain (typically 16 mA for AM and 20 mA for FM) over a wide supply voltage range (3,6 V to 12 V).
- On-chip amplifier for loop filter for both AM and FM (up to 30 V tuning voltage).
- On-chip programmable current amplifier (charge pump) to adjust the loop gain.
- Only one reference frequency for both AM and FM.
- High signal purity due to a sample and hold phase detector for the in-lock condition.
- High tuning speed due to a powerful digital memory phase detector during the out-lock condition.
- Tuning steps for AM are: 1 kHz or 1,25 kHz for a VCO frequency range of 512 kHz to 32 MHz.
- Tuning steps for FM are: 10 kHz or 12,5 kHz for a VCO frequency range of 70 MHz to 120 MHz.
- Serial 3-line bus interface to a microcomputer.
- Test/features.

QUICK REFERENCE DATA

Supply voltage ranges	V_{CC1}	3,6 to 12	V
	V_{CC2}	3,6 to 12	V
	V_{CC3}	V_{CC2} to 31	V
Supply currents	$I_{CC1} + I_{CC2}$	typ. 18	mA
	I_{CC3}	typ. 0,8	mA
Input frequency ranges			
at pin FAM	f_{FAM}	512 kHz to 32	MHz
at pin FFM	f_{FFM}	70 to 120	MHz
Maximum crystal input frequency	f_{XTAL}	> 4	MHz
Operating ambient temperature range	T_{amb}	−25 to + 80	°C

PACKAGE OUTLINE

18-lead DIL; plastic (SOT-102HE).

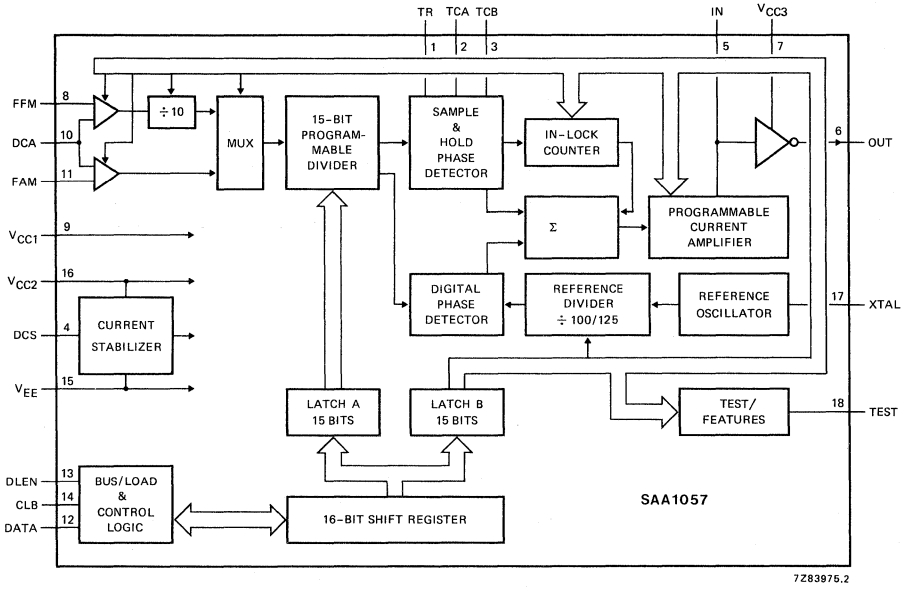


Fig. 1 Block diagram.

GENERAL DESCRIPTION

The SAA1057 performs the entire PLL synthesizer function (from frequency inputs to tuning voltage output) for all types of radios with the AM and FM frequency ranges.
The circuit comprises the following:

- Separate input amplifiers for the AM and FM VCO-signals.
- A divider-by-10 for the FM channel.
- A multiplexer which selects the AM or FM input.
- A 15-bit programmable divider for selecting the required frequency.
- A sample and hold phase detector for the in-lock condition, to achieve the high spectral purity of the VCO signal.
- A digital memory frequency/phase detector, which operates at a 32 times higher frequency than the sample and hold phase detector, so fast tuning can be achieved.
- An in-lock counter detects when the system is in-lock. The digital phase detector is switched-off automatically when an in-lock condition is detected.
- A reference frequency oscillator followed by a reference divider. The frequency is generated by a 4 MHz quartz crystal. The reference frequency can be chosen either 32 kHz or 40 kHz for the digital phase detector (that means 1 kHz and 1,25 kHz for the sample and hold phase detector), which results in tuning steps of 1 kHz and 1,25 kHz for AM, and 10 kHz and 12,5 kHz for FM.
- A programmable current amplifier (charge pump), which controls the output current of both the digital and the sample/hold phase detector in a range of 40 dB. It also allows the loop gain of the tuning system to be adjusted by the microcomputer.
- A tuning voltage amplifier, which can deliver a tuning voltage of up to 30 V.
- BUS; this circuitry consists of a format control part, a 16-bit shift register and two 15-bit latches. Latch A contains the to be tuned frequency information in a binary code. This binary-coded number, multiplied by the tuning spacing, is equal to the synthesized frequency. The programmable divider (without the fixed divide-by-10 prescaler for FM) can be programmed in a range between 512 and 32 767 (see Fig. 3). Latch B contains the control information.

OPERATION DESCRIPTION

Control information

The following functions can be controlled with the data word bits in latch B. For data word format and bit position see Fig. 3.

FM — FM/AM selection; '1' = FM, '0' = AM

REFH — reference frequency selection; '1' = 1,25 kHz, '0' = 1 kHz (sample and hold phase detector)

CP3, CP2, CP1, CP0 — control bits for the programmable current amplifier (see section Characteristics)

SB2 — enables last 8 bits (SLA to T0) of data word B; '1' = enables, '0' = disables; when programmed '0', the last 8 bits of data word B will be set to '0' automatically

SLA — load mode of latch A; '1' = synchronous, '0' = asynchronous

PDM1, PDM0 — phase detector mode

PDM1	PDM0	digital phase detector
0	X	automatic on/off
1	0	on
1	1	off

BRM — bus receiver mode bit; in this mode the supply current of the BUS receiver will be switched-off automatically after a data transmission (current-draw is reduced); '1' = current switched; '0' = current always on

T3 — test bit; must be programmed always '0'

T2 — test bit; selects the reference frequency (32 or 40 kHz) to the TEST pin

T1 — test bit; must be programmed always '0'

T0 — test bit; selects the output of the programmable counter to the TEST pin

T3	T2	T1	T0	TEST (pin 18)
0	0	0	0	1
0	1	0	0	reference frequency
0	0	0	1	output programmable counter
0	1	0	1	output in-lock counter '0' = out-lock '1' = in-lock

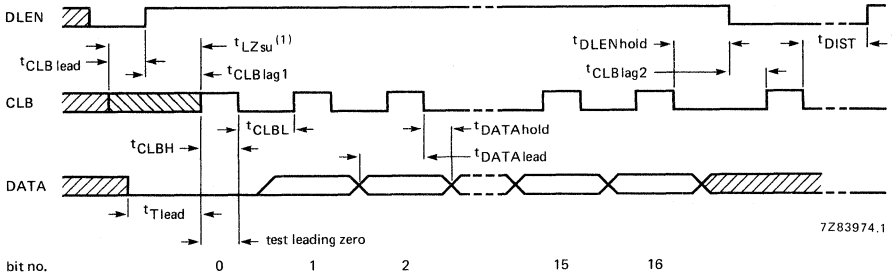


Fig. 2 BUS format.

(1) During the zero set-up time (t_{LZsu}) CLB can be LOW or HIGH, but no transient of the signal is permitted. This can be of use when an I^2C bus is used for other devices on the same data and clock lines.

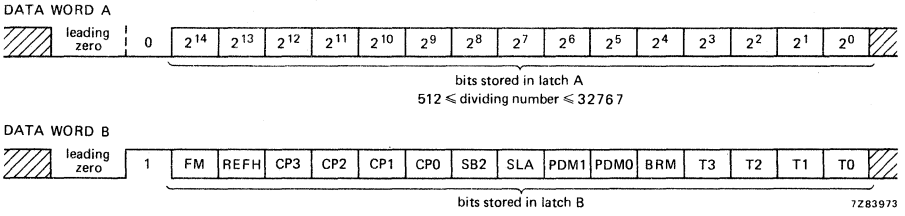


Fig. 3 Bit organization of data words A and B.

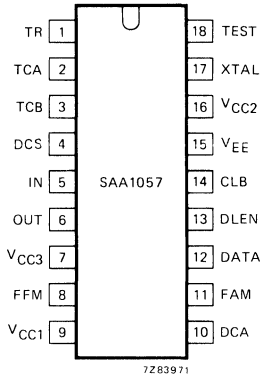


Fig. 4 Pinning diagram.

PINNING

1	TR	resistor/capacitors for sample and hold circuit
2	TCA	
3	TCB	
4	DCS	decoupling of supply
5	IN	input of output amplifier
6	OUT	output of output amplifier
7	V_{CC3}	positive supply voltage of output amplifier
8	FFM	FM signal input
9	V_{CC1}	positive supply voltage of high frequency logic part
10	DCA	decoupling of input amplifiers
11	FAM	AM signal input
12	DATA	BUS
13	DLEN	
14	CLB	
15	V_{EE}	ground
16	V_{CC2}	positive supply voltage of low frequency logic part and analogue part
17	XTAL	reference oscillator input
18	TEST	test output

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage; logic and analogue part	V_{CC1}; V_{CC2}	−0,3 to 13,2	V
Supply voltage; output amplifier	V_{CC3}	V_{CC2} to + 32	V
Total power dissipation	P_{tot}	max. 800	mW
Operating ambient temperature range	T_{amb}	−30 to + 85	°C
Storage temperature range	T_{stg}	−65 to + 150	°C

CHARACTERISTICS

V_{EE} = 0 V; V_{CC1} = V_{CC2} = 5 V; V_{CC3} = 30 V; T_{amb} = 25 °C; unless otherwise specified

	symbol	min.	typ.	max.		conditions
Supply voltages	V_{CC1}	3,6	5	12	V	
	V_{CC2}	3,6	5	12	V	
	V_{CC3}	V_{CC2}	–	31	V	
Supply currents*						
AM mode	I_{tot}	–	16	–	mA	$I_{tot} = I_{CC1} + I_{CC2}$ in-lock: BRM = '1'; PDM = '0'
FM mode	I_{tot}	–	20	–	mA	
	I_{CC3}	0,3	0,8	1,2	mA	I_{OUT} = 0
Operating ambient temperature	T_{amb}	−25	–	+80	°C	
RF inputs (FAM, FFM)						
AM input frequency	f_{FAM}	512 kHz	–	32	MHz	
FM input frequency	f_{FFM}	70	–	120	MHz	
Input voltage at FAM	$V_{i\ (rms)}$	30	–	500	mV	
Input voltage at FFM	$V_{i\ (rms)}$	10	–	500	mV	
Input resistance at FAM	R_i	–	2	–	kΩ	
Input resistance at FFM	R_i	–	135	–	Ω	
Input capacitance at FAM	C_i	–	3,5	–	pF	
Input capacitance at FFM	C_i	–	3	–	pF	
Voltage ratio allowed between selected and non-selected input	V_s/V_{ns}	–	−30	–	dB	
Crystal oscillator (XTAL)						see note 1
Maximum input frequency	f_{XTAL}	4	–	–	MHz	
Crystal series resistance	R_s	–	–	150	Ω	
BUS inputs (DLEN, CLB, DATA)						
Input voltage LOW	V_{IL}	0	–	0,8	V	
Input voltage HIGH	V_{IH}	2,4	–	V_{CC1}	V	
Input current LOW	$-I_{IL}$	–	–	10	μA	V_{IL} = 0,8 V
Input current HIGH	I_{IH}	–	–	10	μA	V_{IH} = 2,4 V

* When the bus is in the active mode (see BRM in Control Information), 4,5 mA should be added to the figures given.

CHARACTERISTICS (continued)

V_{EE} = 0 V; V_{CC1} = V_{CC2} = 5 V; V_{CC3} = 30 V; T_{amb} = 25 °C; unless otherwise specified

	symbol	min.	typ.	max.		conditions
BUS inputs timing (DLEN, CLB, DATA)						see also Fig. 2 and note 2
Lead time for CLB to DLEN	$t_{CLBlead}$	1	–	–	μs	
Lead time for DATA to the first CLB pulse	t_{Tlead}	0,5	–	–	μs	
Set-up time for DLEN to CLB	$t_{CLBlag1}$	5	–	–	μs	
CLB pulse width HIGH	t_{CLBH}	5	–	–	μs	
CLB pulse width LOW	t_{CLBL}	5	–	–	μs	
Set-up time for DATA to CLB	$t_{DATAlead}$	2	–	–	μs	
Hold time for DATA to CLB	$t_{DATAhold}$	0	–	–	μs	
Hold time for DLEN to CLB	$t_{DLENhold}$	2	–	–	μs	
Set-up time for DLEN to CLB load pulse	$t_{CLBlag2}$	2	–	–	μs	
Busy time from load pulse to next start of transmission	t_{DIST}	5	–	–	μs	next transmission after word 'B' to other device
Busy time						or
asynchronous mode	t_{DIST}	0,3	–	–	ms	next transmission to SAA1057 after word 'A' (see also note 5)
synchronous mode	t_{DIST}	1,3	–	–	ms	
Sample and hold circuit (TR, TCA, TCB)						see also notes 3; 4
Minimum output voltage	V_{TCA}, V_{TCB}	–	1,3	–	V	
Maximum output voltage	V_{TCA}, V_{TCB}	–	–	V_{CC2}–0,7	V	
Capacitance at TCA (external)	C_{TCA}	–	–	2,2	nF	REFH = '1'
	C_{TCA}	–	–	2,7	nF	REFH = '0'
Discharge time at TCA	t_{dis}	–	–	5	μs	REFH = '1'
	t_{dis}	–	–	6,25	μs	REFH = '0'
Resistance at TR	R_{TR}	100	–	–	Ω	external
Voltage at TR during discharge	V_{TR}	–	0,7	–	V	
Capacitance at TCB	C_{TCB}	–	–	10	nF	external
Bias current into TCA, TCB	I_{bias}	–	–	10	nA	in-lock

CHARACTERISTICS (continued)

V_{EE} = 0 V; V_{CC1} = V_{CC2} = 5 V; V_{CC3} = 30 V; T_{amb} = 25 °C; unless otherwise specified

	symbol	min.	typ.	max.		conditions
Programmable current amplifier (PCA)						
Output current of the dig. phase detector	$\pm I_{dig}$	–	0,4	–	mA	
Current gain of PCA						
CP3 CP2 CP1 CP0						
P1 0 0 0 0	G_{P1}	–	0,023	–		$V_{CC2} \geqslant 5$ V (only for P1)
P2 0 0 0 1	G_{P2}	–	0,07	–		
P3 0 0 1 0	G_{P3}	–	0,23	–		
P4 0 1 1 0	G_{P4}	–	0,7	–		
P5 1 1 1 0	G_{P5}	–	2,3	–		
Ratio between the output current of S/H into PCA and the voltage on C_{TCB}	S_{TCB}	–	1,0	–	μA/V	
Offset voltage on TCB	ΔV_{TCB}	–	–	1	V	in-lock
Output amplifier (IN,OUT)						
Input voltage	V_{IN}	–	1,3	–	V	in-lock; equal to internal reference voltage
Output voltages						
minimum	V_{OUT}	–	–	0,5	V	$-I_{OUT}$ = 1 mA
maximum	V_{OUT}	$V_{CC3}-2$	–	–	V	I_{OUT} = 1 mA
maximum	V_{OUT}	$V_{CC3}-1$	–	–	V	I_{OUT} = 0,1 mA
Maximum output current	$\pm I_{OUT}$	5	–	–	mA	V_{OUT} = ½ V_{CC3}
Test output (TEST)*						
Output voltage LOW	V_{TL}	–	–	0,5	V	
Output voltage HIGH	V_{TH}	–	–	12	V	
Output current OFF	I_{Toff}	–	–	10	μA	V_{TH}
Output current ON	I_{Ton}	150	–	–	μA	V_{TL}
Ripple rejection**						
at f_{ripple} = 100 Hz						
$\Delta V_{CC1}/\Delta V_{OUT}$		–	77	–	dB	
$\Delta V_{CC2}/\Delta V_{OUT}$		–	70	–	dB	
$\Delta V_{CC3}/\Delta V_{OUT}$		–	60	–	dB	$V_{OUT} \leqslant V_{CC3}-3$ V

* Open collector output.

** Measured in Fig. 6.

NOTES

1. Pin 17 (XTAL) can also be used as input for an external clock.
   The circuit for that is given in Fig. 5. The values given in Fig. 5 are a typical application example.

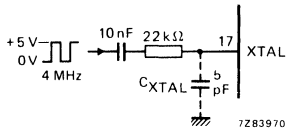


Fig. 5 Circuit configuration showing external 4 MHz clock.

2. See BUS information in section 'operation description'.
3. The output voltage at TCB and TCA is typically ½ V_{CC2}+0,3 V when the tuning system is in-lock via the sample and hold phase detector. The control voltage at TCB is defined as the difference between the actual voltage at TCB and the value calculated from the formula ½ V_{CC2}+0,3 V.
4. Crystal oscillator frequency f_{XTAL} = 4 MHz.
5. The busy-time after word "A" to another device which has more clock pulses than the SAA1057 (> 17) must be the same as the busy-time for a next transmission to the SAA1057.
   When the other device has a separate DLEN or has less clock pulses than the SAA1057 it is not necessary to keep to this busy-time, 5 μs will be sufficient.

APPLICATION INFORMATION

Initialize procedure

Either a train of at least 10 clock pulses should be applied to the clock input (CLB) or word B should be transmitted, to achieve proper initialization of the device.
For the complete initialization (defining all control bits) a transmission of word B should follow. This means that the IC is ready to accept word A.

Synchronous/asynchronous operation

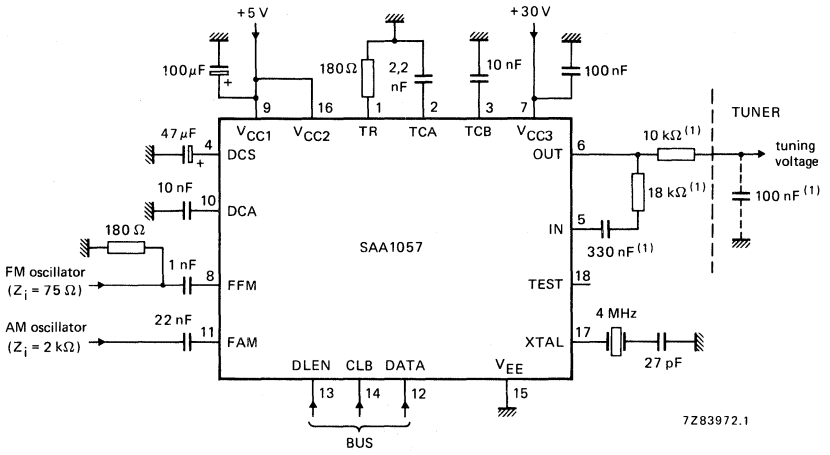
Synchronous loading of the frequency word into the programmable counter can be achieved when bit 'SLA' of word B is set to '1'. This mode should be used for small frequency steps where low tuning noise is important (e.g. search and manual tuning). This mode should not be used for frequency changes of more than 31 tuning steps. In this case asynchronous loading is necessary. This is achieved by setting bit 'SLA' to '0'. The in-lock condition will then be reached more quickly, because the frequency information is loaded immediately into the divider.

Restrictions to the use of the programmable current amplifier

The lowest current gain (0,023) must not be used in the in-lock condition when the supply voltage V_{CC2} is below 5 V (CP3, CP2, CP1 and CP0 are all set to '0'). This is to avoid possible instability of the loop due to a too small range of the sample and hold phase detector in this condition (see also section 'Characteristics').

Transient times of the bus signals

When the SAA1057 is operating in a system with continuous activity on the bus lines, the transient times at the bus inputs should not be less than 100 ns. Otherwise the signal-to-noise ratio of the tuning voltage is reduced.



(1) Values depend on the tuner diode characteristics.

Fig. 6 Application example of the SAA1057PLL frequency synthesizer module.

LED DISPLAY/INTERFACE CIRCUIT

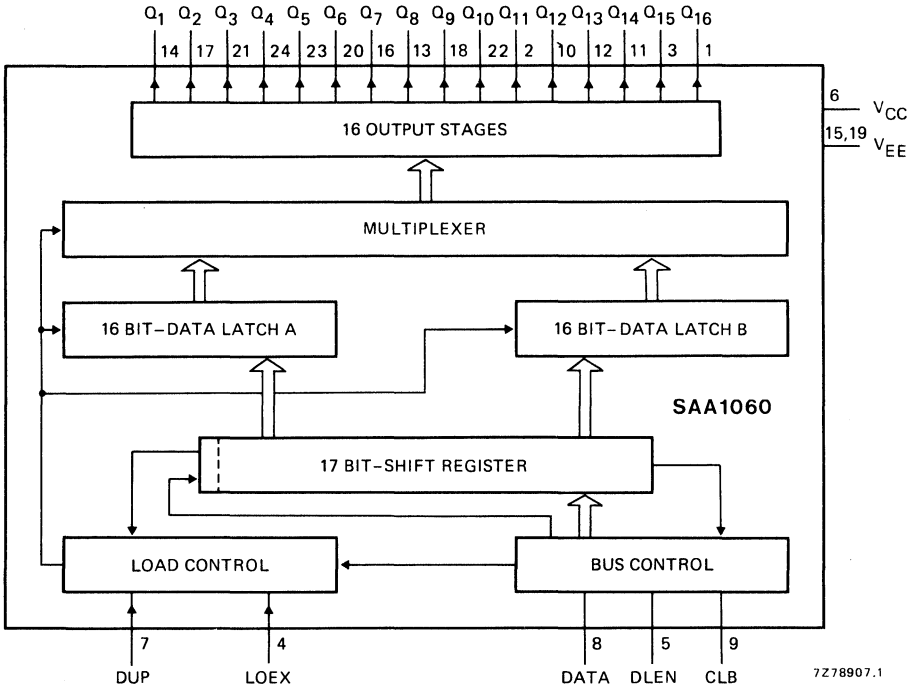


Fig. 1 Block diagram.

Features

- Driving 7, 14, 16-segment displays.
- Driving linear displays, bar graph displays for analogue functions.
- Serial to parallel decoder.
- Bus control for the selection of 18-bit words.
- 2 x 16-bit latch.
- Duplex operation for two modes of output: static (16 bit) or dynamic (2 x 16 bit).
- Data transfer control.
- 2 outputs for higher output current (80 mA).

QUICK REFERENCE DATA

Supply voltage range	V_{CC}	4 to 6	V
Operating ambient temperature range	T_{amb}	−20 to + 80	°C
Maximum input frequency	f_I	typ. 50	kHz
Supply current	I_{CC}	typ. 60	mA
Output current	I_O	< 40	mA
Output current (Q_8 and Q_{16} only)	I_O	< 80	mA

PACKAGE OUTLINE

24-lead DIL; plastic (SOT-101A).

GENERAL DESCRIPTION

The integrated circuit SAA1060 is primarily designed to drive the display unit of a digital tuning system. It can also be used as a 16-bit serial to parallel decoder. Since the device has no decoder (this is handled by a microcomputer), it has many applications:

- driving 7-segment displays
- driving 14-segment displays
- driving linear displays, e.g. pointer, bar graph
- static output of switch-functions
- digital to analogue converter, with external R-2R network
- extension of the number of outputs for microprocessors or microcomputers.

Data transmission is initiated by means of a burst of clock pulses (CLB), a data line enable signal (DLEN) and the data signal (DATA). The bus control circuit distinguishes between interference and valid data by checking word length (17 bits) and the leading zero. This allows different bus information to be supplied on the same bus lines for other circuits (e.g. SAA1056 with 16 bits).

The last bit (bit 17) of the data word contains the information which of the two internal latches will be loaded. The input LOEX determines if the latched data of selected latches is presented directly to the outputs, or synchronized with the data select signal DUP.

The output stages are n-p-n transistors with open collectors. The current capability is designed for the requirements of duplex operation. Two of the outputs (Q_8 and Q_{16}) are arranged for double current, so that 2 x 2 segments can be connected in parallel.

OPERATION DESCRIPTION

Data inputs (DLEN, DATA)

The SAA1060 processes serially the 18-bit data words synchronized with the clock burst (CLB) and applied to the data input DATA. A command will be accepted only when the data line enable input (DLEN) is HIGH (see Fig. 3).

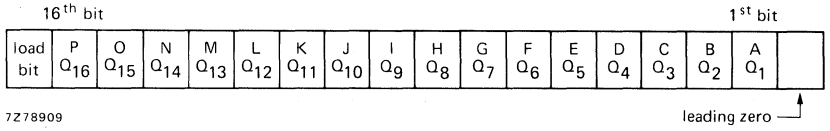


Fig. 2 Organization of a data word.

Condition for 17th bit:
0 = load data latch B
1 = load data latch A

The loading of the accepted information in one of the data latches is done by the 19th clock pulse, when DLEN is LOW.

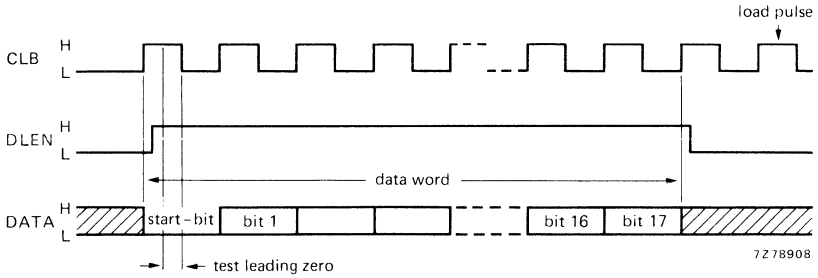


Fig. 3 Pulse diagram of the 16-bit data transmission.

Each data word must start with a leading zero. The SAA1060 checks the data word for the correct length (18 bits) and also for the leading zero.
The actual data is switched directly to the appropriate outputs. For switching on a segment, a '0' (LOW) is necessary at the appropriate data bit.

Data selection input (DUP)

The logic states at input DUP determine which of the two latch contents can be found on the output.

0 = latch A contents
1 = latch B contents

Load control input (LOEX)

Input LOEX determines the operation mode in which the device is able to work.

0 = duplex mode, i.e. output synchronized with the duplex signal
1 = d.c. mode, i.e. output direct from the by DUP selected data latch.

When operating in duplex mode at 50 Hz, the time between two data words to be transmitted must be > 21 ms.

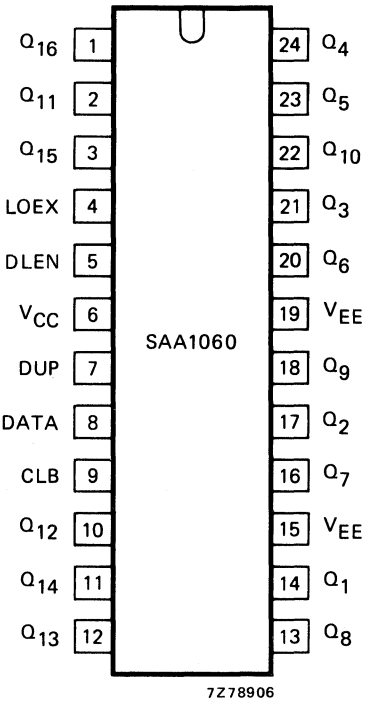


Fig. 4 Pinning diagram.

RATINGS (V_{EE} = 0)

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range	V_{CC}	−0,3 to + 7	V
Total power dissipation	P_{tot}	max. 900	mW
Operating ambient temperature range	T_{amb}	−20 to + 80	°C
Storage temperature range	T_{stg}	−25 to + 125	°C

CHARACTERISTICS

V_{EE} = 0; T_{amb} = 25 °C; unless otherwise specified

	V_{CC} V	symbol	min.	typ.	max.		conditions
Supply voltage	–	V_{CC}	4	5	6	V	
Supply current	5	I_{CC}	–	60	–	mA	
Inputs DATA, CLB, DLEN, LOEX							
input voltage HIGH	5	V_{IH}	2	–	5	V	
input voltage LOW	5	V_{IL}	–	–	1	V	
input current LOW	5	$-I_{IL}$	–	–	20	μA	V_I = 0
maximum input frequency	5	f_I	–	50	–	kHz	
Input DUP							
input voltage HIGH	5	V_{IH}	0,8	–	12	V	
input voltage LOW	5	V_{IL}	−6	–	0,4	V	
input current HIGH	5	I_{IH}	0,01	–	12	mA	
maximum input frequency	5	f_I	–	50	–	kHz	
Outputs Q_1 to Q_7, Q_9 to Q_{15}							
output voltage HIGH	5	V_{QH}	–	–	16,8	V	I_{QH} = 0
output voltage LOW	5	V_{QL}	–	–	0,5	V	I_{QL} = 40 mA
output current LOW							
duplex mode	5	I_{QL}	–	–	60	mA	peak value at sinusoidal voltage
d.c. mode	5	I_{QL}	–	20	40	mA	
Outputs Q_8 and Q_{16}							
output voltage HIGH	5	V_{QH}	–	–	16,8	V	I_{QH} = 0
output voltage LOW	5	V_{QL}	–	–	0,5	V	I_{QL} = 80 mA
output current LOW							
duplex mode	5	I_{QL}	–	–	120	mA	peak value at sinusoidal voltage
d.c. mode	5	I_{QL}	–	40	80	mA	

OUTPUT PORT EXPANDER

The SAA1061 is a MOS N-channel output port expander circuit, which converts serial input data into parallel output information. The IC is used in combination with a microcomputer.

Features

- Bus control for the selection of 18-bit words.
- 16-bit latch and low-ohmic driver outputs.
- Pin compatible with the SAA1060, except the SAA1061 has no duplex mode.
- Address selection inputs; up to four SAA1061 circuits can be operated from a common CBUS.

QUICK REFERENCE DATA

Supply voltage	V_{DD}	typ.	5 V
Operating ambient temperature range	T_{amb}		−20 to +80 °C
Supply current	I_{DD}	typ.	9 mA
Output current per output	I_O	typ.	15 mA

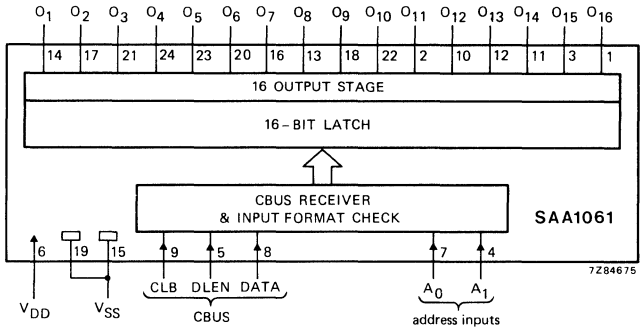


Fig. 1 Block diagram.

HANDLING

Inputs and outputs are protected against electrostatic charge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see 'Handling MOS Devices').

PACKAGE OUTLINE

24-lead DIL; plastic (SOT-101A).

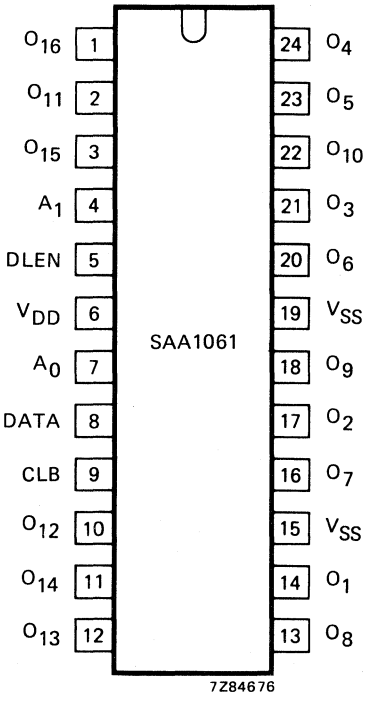


Fig. 2 Pinning diagram.

PINNING

6	V_{DD}	positive supply (+5 V)	
15, 19	V_{SS}	ground (0 V)	
Inputs			
8	DATA	data word	CBUS
9	CLB	clock burst	CBUS
5	DLEN	data line enable	CBUS
7	A_0	address bit S0	
4	A_1	address bit S1	
Outputs			
14	O_1	driver outputs O_1 to O_{16} corresponding with the data bits 1 to 16 of the data word	
17	O_2		
21	O_3		
24	O_4		
23	O_5		
20	O_6		
16	O_7		
13	O_8		
18	O_9		
22	O_{10}		
2	O_{11}		
10	O_{12}		
12	O_{13}		
11	O_{14}		
3	O_{15}		
1	O_{16}		

GENERAL DESCRIPTION

The SAA1061 is an addressable output port expander for use in microcomputer controlled systems. It converts serial input data into parallel output information. The circuit comprises a CBUS receiver, logic to check input format, a 16-bit serial/parallel converter, latches and drivers for the parallel outputs.

This universal device can be used for e.g.:

- static output of switch-functions
- extension of the number of outputs for microcomputers or microprocessors
- driving maximum 16-segment LEDs; e.g. 7, 4 or 16-segment displays
- driving linear displays (pointer, bar graph)
- digital to analogue conversion with external resistor network.

The data is transmitted via the 3-line CBUS from the microcomputer. If the data transmission is valid, the data are transferred by a load pulse via the latch to the driver output. Each data transmission is checked for word length (18-bit) by the on-chip word format control circuitry. This allows different bus information to be supplied on the same bus lines for other circuits.

The address inputs A_0 and A_1 determine four address possibilities. A data transmission only takes place if the programmed addresses correspond with the address bits S0 and S1.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range	V_{DD}	−0,3 to +7,5	V
Input voltage range	V_I	−0,3 to +15	V
Input current	$\pm I_I$	max. 10	mA
Output voltage range	V_O	−0,3 to +16,5	V
Output current per output	$\pm I_O$	max. 20	mA
Power dissipation per output	P_O	max. 7,5	mW
Total power dissipation per package	P_{tot}	max. 300	mW
Operating ambient temperature range	T_{amb}	−20 to +80	°C
Storage temperature range	T_{stg}	−20 to +125	°C

CHARACTERISTICS

V_{SS} = 0 V; V_{DD} = 5 V; T_{amb} = −20 to +80 °C; unless otherwise specified

	symbol	min.	typ.	max.		conditions
Supply voltage	V_{DD}	4,5	5	5,5	V	
Supply current	I_{DD}	–	–	20	mA	
Inputs CLB, DLEN, DATA, A_0, A_1						T_{amb} = 25 °C
Input voltage LOW	V_{IL}	−0,3	–	0,8	V	
Input voltage HIGH	V_{IH}	2,0	–	15	V	
Input leakage current	I_{IR}	–	–	1	μA	V_I = −0,3 to +15 V
Outputs O_1 to O_{16} (open drain)						
Output voltage LOW	V_{OL}	–	–	0,65	V	I_{OL} = 15 mA
Output leakage current HIGH	I_{OH}	–	–	20	μA	V_{OH} = 16,5 V
Rise and fall times	t_r, t_f	–	–	10	μs	V_{OL} = 1,5 V; V_{OH} = 13,5 V
CBUS timing						
Rise and fall times	t_r, t_f	–	–	2	μs	see Fig. 3
Data set-up time DATA → CLB	t_{SUDA}	400	–	–	ns	
Data hold time DATA → CLB	t_{HDDA}	250	–	–	ns	
Enable set-up time DLEN → CLB	t_{SUEN}	400	–	–	ns	
Disable set-up time CLB → DLEN	t_{SUDI}	600	–	–	ns	
Set-up time DLEN → CLB (load pulse)	t_{SULD}	400	–	–	ns	
CLB pulse width HIGH/LOW	t_{WH}, t_{WL}	450	–	–	ns	

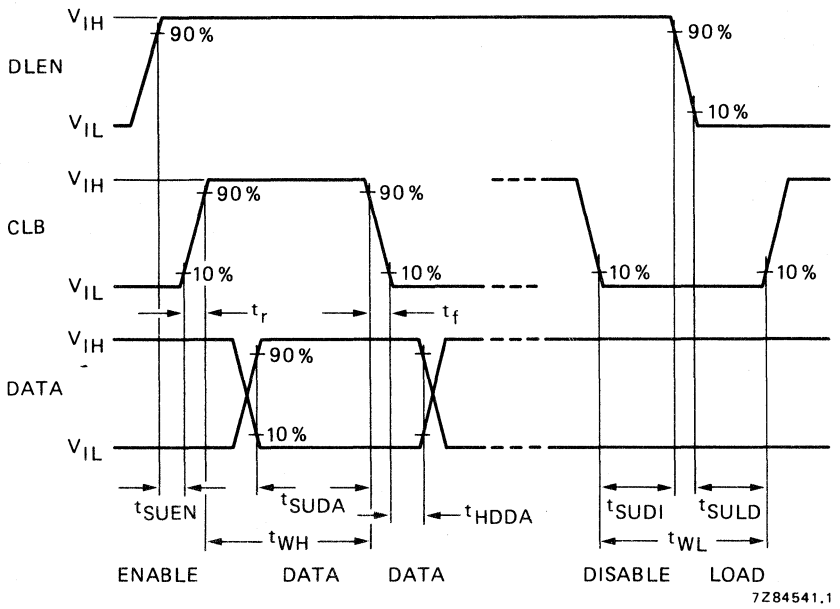


Fig. 3 CBUS timing.

OPERATION DESCRIPTION

1. CBUS transmission

The data words are entered via a serial CBUS interface. A clock burst of 18 clock periods is used to transmit the 16-bit data word, plus 2 identifier bits.

Serial data words, which are synchronized with the clock burst (CLB), are accepted if the enable input DLEN is HIGH at the same time. Each transmission is checked for word length (number of clock pulses during DLEN is HIGH) and the address bits S0 and S1.

The valid data flag is only set if:
1. Word length is correct; 2 address bits and 16 data bits.
2. Address bits S0 and S1 correspond with A_0 and A_1.

Loading the information into the selected latch register is done by the load pulse (first clock pulse after the HIGH-to-LOW transition of DLEN) if the address bits correspond with A_0 and A_1. The load pulse or a new LOW-to-HIGH transition of DLEN resets the valid data flag. Only after the valid data flag is reset, will new data be accepted.

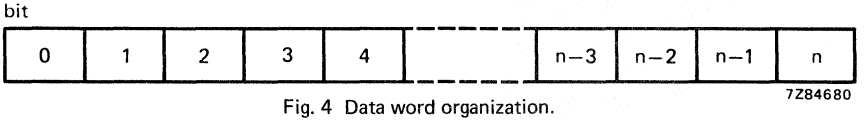


Fig. 4 Data word organization.

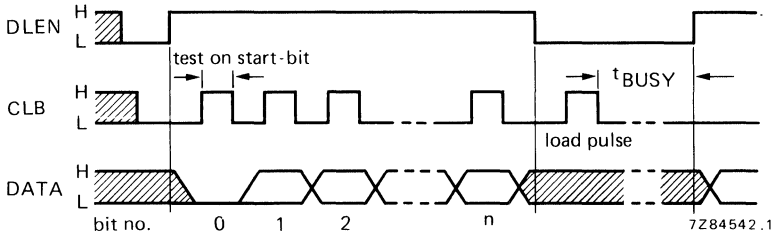


Fig. 5 CBUS data transmission.

Definitions to Figs 4 and 5:

- Word length: number of clock pulses during DLEN is active (HIGH); n + 1 bits = 18 bits.
- Bit number 0 is for the SAA1061 S0.
- Data bits: bit numbers 1 to n-1 (16-bits); bit no. n is S1.
- Load pulse: first clock pulse after DLEN returns to inactive (LOW).

2 Address inputs A_0 and A_1

The 1st bit (bit S0) and the 18th bit (bit S1) of the data word are the address bits.
Data is accepted only if the addresses correspond to the programmed addresses at inputs A_0 and A_1, that is for:

A_0 = S0 and A_1 = S1.

3 Data outputs O_1 to O_{16}

The outputs O_1 to O_{16} correspond with the data bits 1 to n-1 (16-bits). The open drain driver outputs (O_1 to O_{16}) are switched to ground (O_n = LOW), if the corresponding data bit is LOW,

4 Power-on reset

The circuit generates internally a reset-cycle after switching on the supply and the outputs become high-ohmic (HIGH).

LCD DISPLAY/INTERFACE CIRCUIT

GENERAL DESCRIPTION

The SAA1062A is designed to drive a Liquid Crystal Display (LCD) of a digital tuning system. It contains a shift register with programmable length (18 or 21 bits), latches, both synchronized or static, exclusive-OR segment drivers (17 or 20 bits), an I.f. oscillator and a backplane driver for the LCD. The circuit is designed to be driven by a 3 bus structure from a microcomputer and can also be used as a programmable 17 or 20 bits serial-to-parallel decoder. It is also capable of storing 40 bits of information.

Features

- Driving 7 to 20-segment displays.
- Driving linear displays.
- Serial to parallel decoder of digital signals.
- Bus control for the selection of 18/21-bit words.
- 17/20-bit latch.
- A.C. segment drive.
- On-chip oscillator.

QUICK REFERENCE DATA

Supply voltage range	V_{CC}	4,2 to 5,5	V
Operating ambient temperature range	T_{amb}	−20 to + 70	°C
Maximum input frequency	f_i	typ. 50	kHz
Supply current	I_{CC}	typ. 3,5	mA
Output current (Q_1 to Q_{20})	I_Q	> 60	μA

PACKAGE OUTLINES

SAA1062A : 28-lead DIL; plastic (SOT-117).
SAA1062AT: 28-lead mini-pack; plastic (SO-28; SOT-136A).

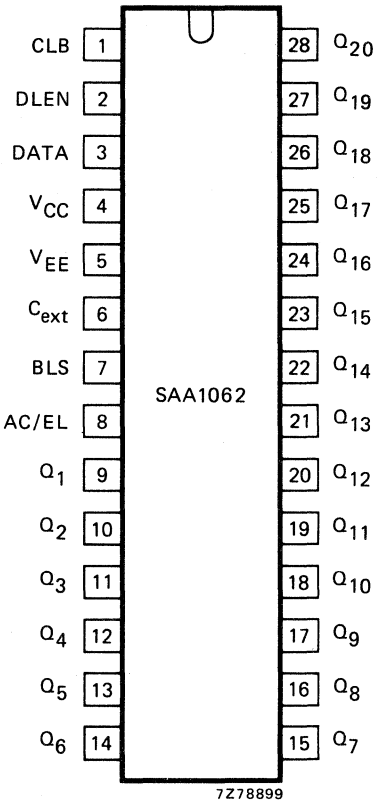


Fig. 1 Pinning diagram.

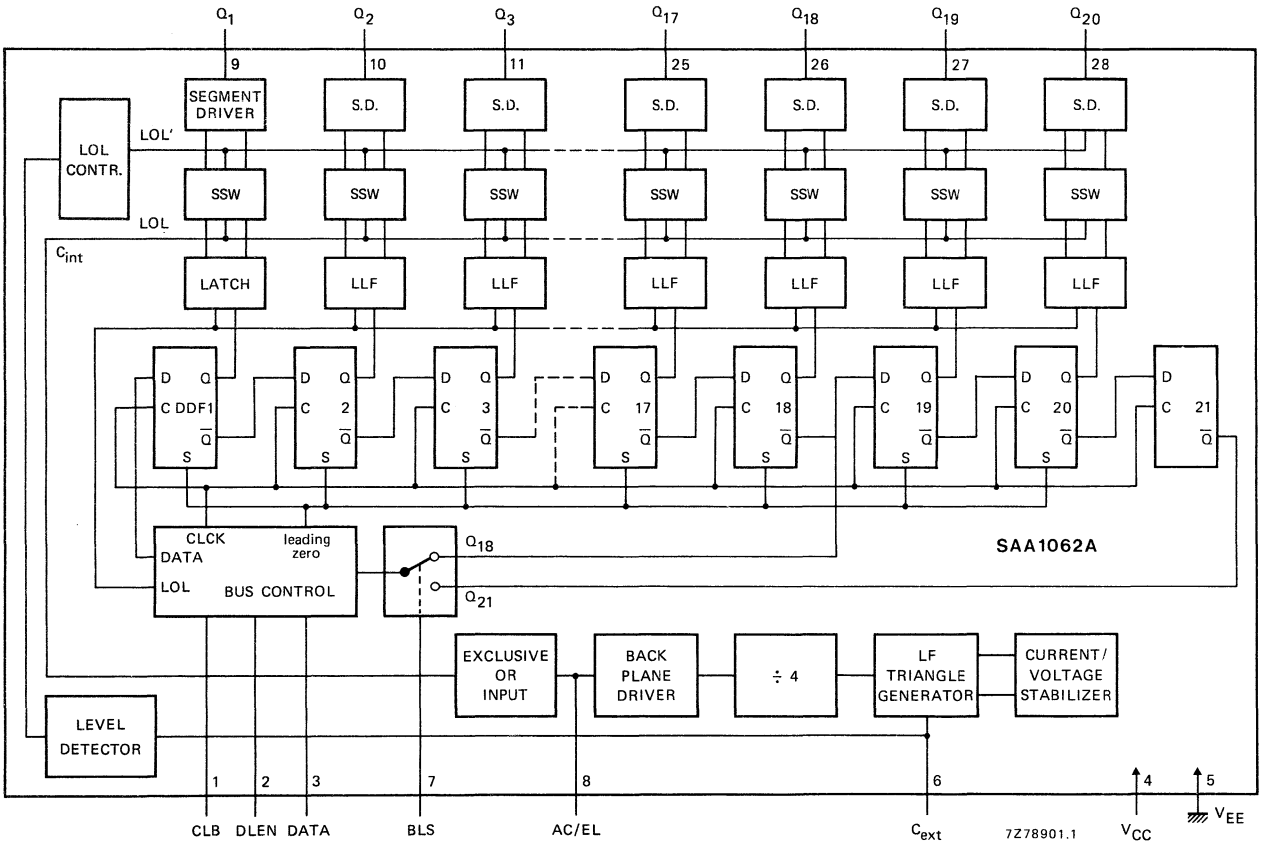


Fig. 2 Block diagram.

OPERATION DESCRIPTION

The input information for this device consists of a data bus with 18 or 21 bits words, an external clock synchronized with the data bus and an enable signal. The organization of these signals is given in Fig. 3. These signals are handled by the BUS CONTROL circuit in which the decision is made whether these signals are valid for the device. It contains a leading zero detector (start condition of reception) and a data-length control. Leading zero is detected when the data signal is LOW and the DLEN signal is HIGH, during the first HIGH period of the clock signal. During the HIGH period of DLEN, the length control determines if the clock signal consists of the programmed number of pulses (18 or 21). This last function permits the user to supply other information on the same signal lines.

Furthermore the bus control prevents the device from accepting inferferences on the signal lines. While leading zero is detected, the shift register is set and for a proper leading zero the following data is shifted into this register. The Q_n position of the first bit of the register is shifted into the last bit, if the length of the data and the clock input are correct. Incorrect length of the information is detected by checking the value of the last bit of the programmed register. If the data transmission has been accepted properly, the bus control stage generates a valid pulse (LOL).

This pulse enables the load control circuit to load the contents of the register into the output latch immediately. On the first edge of the backplane driver signal "AC out/EL in" following on this "LOL" pulse, the new information of this latch is transferred to the output driver which also contains a latch. With this ability it is possible to load the device with 20 bits and also to transfer this data to the segment outputs. Furthermore, the SR can be reloaded by a second complete load procedure without a load enable clock pulse. This causes the SR to contain 20 bits and the output latches another 20 bits of information.

The output driver also contains an EXCLUSIVE-OR which is driven by the backplane driver signal and the latch output. The segment driver output signal is in phase with the output of the backplane driver when the input data is HIGH ("1") and 180^{o} out-of-phase when the input data is LOW ("0").

In the static or slave mode, the backplane output can be used as input by connecting pin 6 to ground or V_{CC}. The IC now can operate as a static driver or as a synchronized slave.

The I.f. oscillator consists of a triangle generator of the I-2I principle. It only needs an external capacitor to fix the frequency. As both amplitude and current are temperature compensated, this frequency is more or less independent of pn temperature. An internal switching signal of this generator is divided by 4 to attain a symmetrical output for the backplane driver (pin 8) of nominal 60 Hz for an external capacitor of 22 nF.

The backplane driver is able to drive a 40 bits display.

The bit length of the shift register is programmed with BLS (Bit Length Selector) (pin 7). If BLS is kept LOW the DATA bit length is 20; for BLS open or HIGH a DATA bit length of 17 is selected.

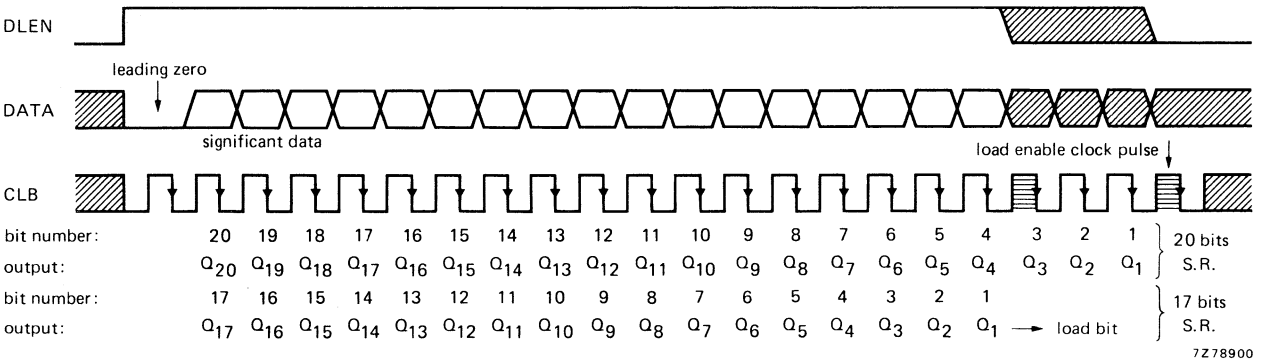


Fig. 3 Organization of 18 and 21 bit words; DATA = LOW means segment 'on'.

RATINGS (V_{EE} = 0)

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_{CC}	max.	6 V
Total power dissipation at T_{amb} = 100 °C derate linearly with 0,02 W/°C	P_{tot}	max.	500 mW
Operating ambient temperature range	T_{amb}		−25 to + 125 °C
Storage temperature range	T_{stg}		−55 to + 125 °C

CHARACTERISTICS

V_{EE} = 0; V_{CC} = 5 V; T_{amb} = 25 °C; unless otherwise specified

	symbol	min.	typ.	max.		condition
Supply voltage	V_{CC}	4,2	5	5,5	V	
Supply current	I_{CC}	–	3,5	–	mA	
Inputs CLB, DLEN, DATA, BLS						
input voltage HIGH	V_{IH}	1,6	–	V_{CC}	V	
input voltage LOW	V_{IL}	−1	–	+ 0,8	V	
maximum input frequency	f_I	–	50	–	kHz	
Input C_{ext}						
input voltage HIGH	V_{IH}	4,6	–	–	V	static mode
input voltage LOW	V_{IL}	−0,1	–	0,4	V	sync. slave mode
input current HIGH	I_{IH}	–	–	180	μA	
input current LOW	I_{IL}	–	–	−40	μA	
Input AC/EL (in slave mode)						
input voltage HIGH	V_{IH}	2,7	–	V_{CC}	V	
input voltage LOW	V_{IL}	−0,4	–	2,3	V	
Output C_{ext} (oscillator mode)						
oscillator frequency	f_{osc}	120	240	360	Hz	C = 22 nF
Output stage backplane (AC/EL)						
output current sink/source	I_O	2,4	–	–	mA	
Output Q_1 to Q_{20}						
output current sink/source	I_O	60	–	–	μA	
d.c. rest voltage between pin 8 (AC/EL) and one of the segment drivers (see Fig. 4)						
segment 'on' situation		–	–	25	mV	
segment 'off' situation		–	–	25	mV	

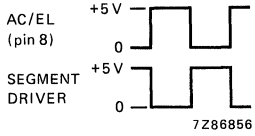


Fig. 4 AC/EL and segment driver pulses.
The d.c. voltage for segment 'on' is about 5 V.

REMOTE TRANSMITTER

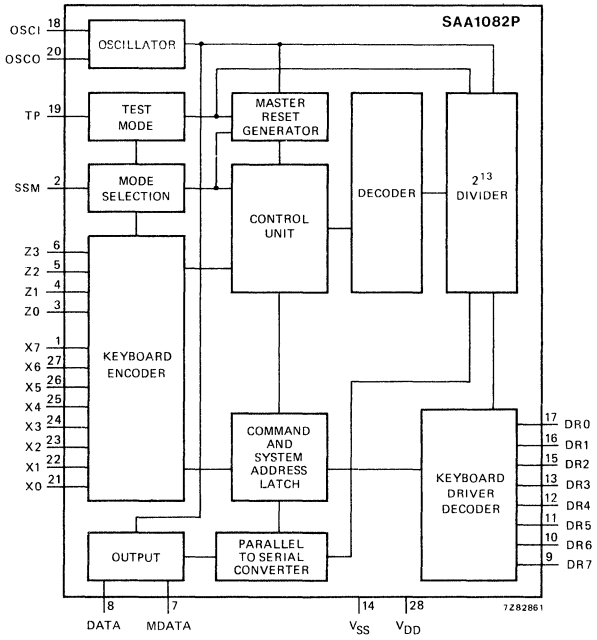


Fig. 1 Block diagram.

Features:

- Transmitter for 32 x 64 commands.
- One transmitter for the control of 32 systems.
- Very low current consumption.
- Suitable for infrared transmission link.
- Transmission by biphase technique.
- Short transmission times; speed-up of system reaction time.
- LC-controlled oscillator; no crystal required.

QUICK REFERENCE DATA

Supply voltage range	V_{DD}	4,75 to 12,6	V
Operating ambient temperature range	T_{amb}	−25 to +85	°C
Minimum oscillator input frequency	f_{OSCI}	75	kHz
Quiescent current			
V_{DD} = 12,6 V; I_Q = 0; T_{amb} = 25 °C	I_{DD}	max. 10	μA

PACKAGE OUTLINE 28-lead DIL; plastic (SOT-117).

GENERAL DESCRIPTION

The SAA1082P is intended for a general purpose infrared remote control system. The device is implemented in LOCMOS technology.
The circuit can generate 2048 different commands and utilizes a keyboard with a single-pole switch per key.
The commands are arranged such that 32 systems can be addressed, containing 64 different commands each. The keyboard interconnection is shown in Fig. 2.
The circuit response to legal (one key depressed at a time) and illegal (more than one key depressed at a time) keyboard operation is specified later in this publication (see NOTE).

OPERATION DESCRIPTION

Combined system mode (SSM = LOW)

Legal key depression either in the X-DR or Z-DR matrix starts the debounce cycle. When the contact is made for two bit times without interruption, the oscillator enable signal is latched and the key may be released. Interruption within the two bit times resets the internal action. At the end of the debounce time, the DR-outputs are switched off and two scan cycles are started, switching on the DR-outputs one by one. When a Z or X-input senses a LOW level, a latch-enable signal is fed to the system address or command latches depending on whether sensing was found in the Z or X-input matrix. After latching a system address number, the IC will generate the last command (i.e. all command bits '1') in the chosen system as long as the key is depressed. Latching of a command number causes the IC to generate this command together with the system address number stored in the system address latch. Releasing the key will reset the internal action if no data is transmitted at that time. Once the transmission is started, the signal will be finished completely.

Single system mode (SSM = HIGH)

Only legal key depression in the X-DR matrix starts the debounce cycle. When the contact is made for two bit times without interruption, the oscillator enable signal is latched and the key may be released. Interruption within the two bit times resets the internal action. At the end of the debounce time, the pull-up transistors in the X-lines are switched off, those in the Z-lines are switched on during the first scan cycle. The wired connection in the Z-matrix is then translated into a system address number and stored in the system address latch. At the end of the first scan cycle the pull-up resistors in the Z-lines are switched off and the inputs are disabled again, while the transistors in the X-lines are switched on. The second scan cycle produces the command number which, after latching, is transmitted together with the system address number.

The scan cycles are repeated before every code transmission, so that even by 'take-over' of key depression during code transmission the right system and command numbers are generated.

Inputs

The command inputs X0 to X7 carry a logical '1' in the quiescent state by means of an internal pull-up transistor. When the system mode selection input SSM is LOW, the system inputs Z0 to Z3 carry also a logical '1' in the quiescent state by means of an internal pull-up transistor.

When SSM is HIGH, the transistors are switched off. No current can than flow via the wired connection in the Z-DR matrix.

Oscillator

OSCI and OSCO are the input and the output respectively of a 2-pins LC-oscillator. The oscillator is formed externally by one inductor and two capacitors.

Key-release detection

An extra control bit is added which will be complemented after key-release. In this way the decoder gets an indication that shows if the next code is to be considered as a new command. This is very important in case of multi-digit entry (e.g. by channel numbers or Teletext/Viewdata pages). The control bit will only be complemented after finishing of at least one code transmission. The scan cycles are repeated before every code transmission, so that, even by 'take-over' of key depression during code transmission, the right system and command numbers are generated.

Outputs

The output DATA carries the generated information according to the format given in Fig. 3 and Tables 1 and 2.
The code will be transmitted in biphase; logical 'ones (1) and zeroes (0)' are given in Fig. 4.

The code consists of four parts:
- Start part formed by 2 bits (twice a logical '1'),
- Control part formed by 1 bit,
- System part formed by 5 bits,
- Command part formed by 6 bits.

The output MDATA carries the same information as output DATA, but in a modulated way. Each bit is presented as a burst of 16 oscillator periods.
In the quiescent state, both outputs are non-conducting (3-state outputs).
The scan drivers DR0 to DR7 are of the open drain N-channel type and are conducting in the quiescent state of the circuit. After a legal key depression, a scanning procedure is started so that they are switched into the conductive state one after the other.

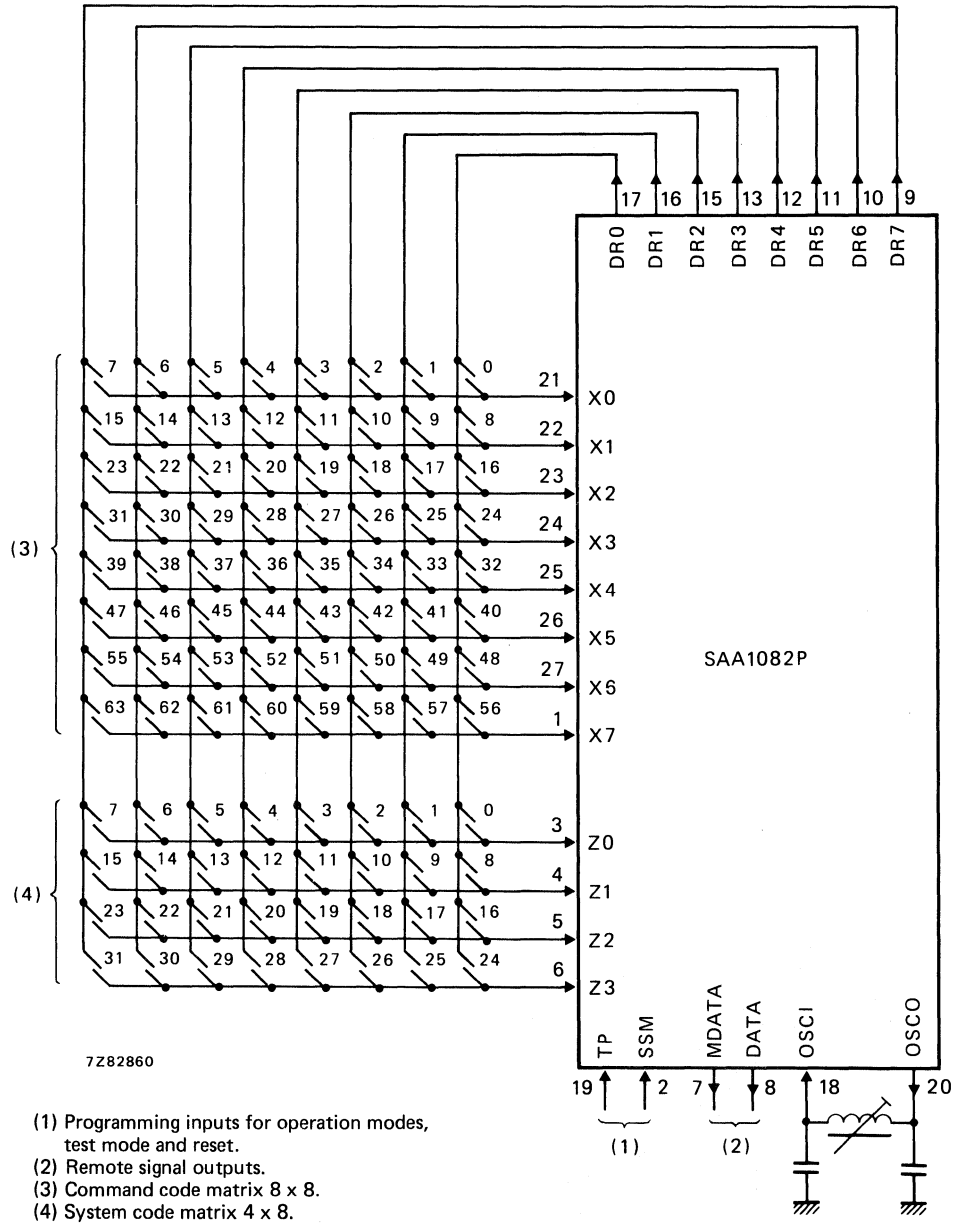
Reset action

The circuit will be reset immediately when a key release occurs during:
- debounce time,
- between two codes.

When a key release occurs during scanning of the matrix, a reset action will be accomplished if:
- key is released while one of the driver outputs is in the low-ohmic '0' state,
- key is released before detection of that key,
- there is no wired connection in the Z-DR matrix while SSM = HIGH.

Test pin

The test pin TP is an input which can be used for testing purposes.
When LOW, the circuit operates normally.
When HIGH, all pull-up transistors are switched off, the control bit is set to zero and the output data is 2^6 times faster than normal.
When Z2 = Z3 = LOW, the counter will be reset to zero.



(1) Programming inputs for operation modes, test mode and reset.
(2) Remote signal outputs.
(3) Command code matrix 8 x 8.
(4) System code matrix 4 x 8.

Fig. 2 Keyboard interconnection.

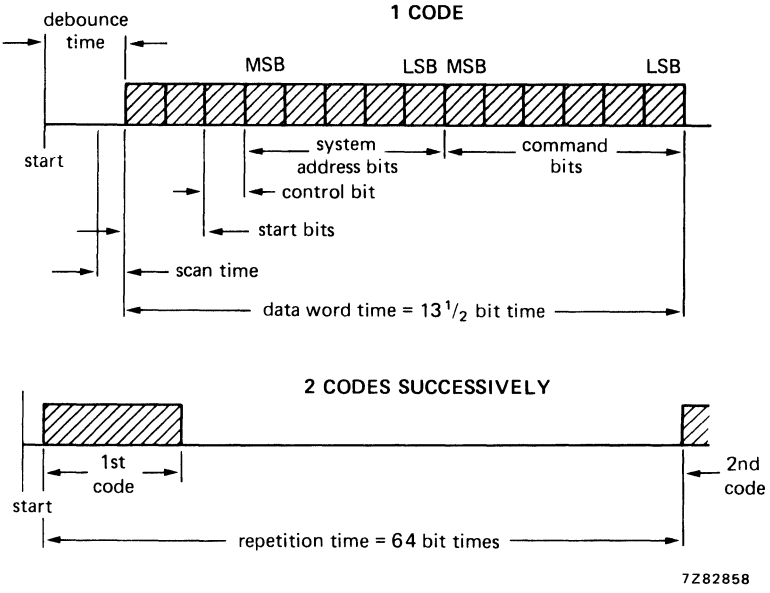


Fig. 3 Data output format.

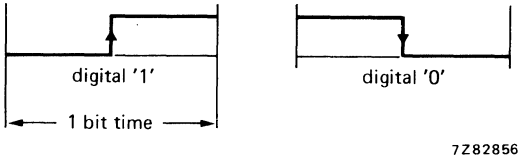


Fig. 4 Biphase transmission code; 1 bit time = $2^7 \times T_{osc}$, where T_{osc} is the oscillator period time.

NOTE

Every connection of one X-input and one DR-output will be recognized as a legal key depression and will cause the IC to generate the corresponding code. Activating more than one X-input at a time will be considered as an illegal activity and no action (oscillator does not start) will be taken.
When SSM = LOW, every connection of one Z-input and one DR-output will be recognized as a legal key depression and will cause the IC to generate the corresponding code. Activating two or more Z-inputs, or Z-inputs and X-inputs, at a time will be considered as an illegal activity and no action will be taken.
When SSM = HIGH, a wired connection must be made between a Z-input and a DR-output. If no connection is present the code will not be generated.
Z2 or Z3 must be connected to V_{DD} to avoid unwanted supply current. When one X or Z-input is connected to more than one DR-input, the last scan signal will be considered as legal.
The maximum allowable value of the contact series resistance of the keyboard switches is 10 kΩ.

Table 1 Command matrix (X-DR)

code no.	X-lines X... 0 1 2 3 4 5 6 7	DR-lines DR... 0 1 2 3 4 5 6 7	command bits C... 5 4 3 2 1 0
0	●	●	0 0 0 0 0 0
1	●	●	0 0 0 0 0 1
2	●	●	0 0 0 0 1 0
3	●	●	0 0 0 0 1 1
4	●	●	0 0 0 1 0 0
5	●	●	0 0 0 1 0 1
6	●	●	0 0 0 1 1 0
7	●	●	0 0 0 1 1 1
8	●	●	0 0 1 0 0 0
9	●	●	0 0 1 0 0 1
10	●	●	0 0 1 0 1 0
11	●	●	0 0 1 0 1 1
12	●	●	0 0 1 1 0 0
13	●	●	0 0 1 1 0 1
14	●	●	0 0 1 1 1 0
15	●	●	0 0 1 1 1 1
16	●	●	0 1 0 0 0 0
17	●	●	0 1 0 0 0 1
18	●	●	0 1 0 0 1 0
19	●	●	0 1 0 0 1 1
20	●	●	0 1 0 1 0 0
21	●	●	0 1 0 1 0 1
22	●	●	0 1 0 1 1 0
23	●	●	0 1 0 1 1 1
24	●	●	0 1 1 0 0 0
25	●	●	0 1 1 0 0 1
26	●	●	0 1 1 0 1 0
27	●	●	0 1 1 0 1 1
28	●	●	0 1 1 1 0 0
29	●	●	0 1 1 1 0 1
30	●	●	0 1 1 1 1 0
31	●	●	0 1 1 1 1 1

code no.	X-lines X... 0 1 2 3 4 5 6 7	DR-lines DR... 0 1 2 3 4 5 6 7	command bits C... 5 4 3 2 1 0
32	●	●	1 0 0 0 0 0
33	●	●	1 0 0 0 0 1
34	●	●	1 0 0 0 1 0
35	●	●	1 0 0 0 1 1
36	●	●	1 0 0 1 0 0
37	●	●	1 0 0 1 0 1
38	●	●	1 0 0 1 1 0
39	●	●	1 0 0 1 1 1
40	●	●	1 0 1 0 0 0
41	●	●	1 0 1 0 0 1
42	●	●	1 0 1 0 1 0
43	●	●	1 0 1 0 1 1
44	●	●	1 0 1 1 0 0
45	●	●	1 0 1 1 0 1
46	●	●	1 0 1 1 1 0
47	●	●	1 0 1 1 1 1
48	●	●	1 1 0 0 0 0
49	●	●	1 1 0 0 0 1
50	●	●	1 1 0 0 1 0
51	●	●	1 1 0 0 1 1
52	●	●	1 1 0 1 0 0
53	●	●	1 1 0 1 0 1
54	●	●	1 1 0 1 1 0
55	●	●	1 1 0 1 1 1
56	●	●	1 1 1 0 0 0
57	●	●	1 1 1 0 0 1
58	●	●	1 1 1 0 1 0
59	●	●	1 1 1 0 1 1
60	●	●	1 1 1 1 0 0
61	●	●	1 1 1 1 0 1
62	●	●	1 1 1 1 1 0
63	●	●	1 1 1 1 1 1

Table 2 System matrix (Z-DR)

system no.	DR-lines DR...								Z-lines Z...				system bits S...				
	0	1	2	3	4	5	6	7	0	1	2	3	4	3	2	1	0
0	●								●				0	0	0	0	0
1		●							●				0	0	0	0	1
2			●						●				0	0	0	1	0
3				●					●				0	0	0	1	1
4					●				●				0	0	1	0	0
5						●			●				0	0	1	0	1
6							●		●				0	0	1	1	0
7								●	●				0	0	1	1	1
8	●									●			0	1	0	0	0
9		●								●			0	1	0	0	1
10			●							●			0	1	0	1	0
11				●						●			0	1	0	1	1
12					●					●			0	1	1	0	0
13						●				●			0	1	1	0	1
14							●			●			0	1	1	1	0
15								●		●			0	1	1	1	1
16	●										●		1	0	0	0	0
17		●									●		1	0	0	0	1
18			●								●		1	0	0	1	0
19				●							●		1	0	0	1	1
20					●						●		1	0	1	0	0
21						●					●		1	0	1	0	1
22							●				●		1	0	1	1	0
23								●			●		1	0	1	1	1
24	●											●	1	1	0	0	0
25		●										●	1	1	0	0	1
26			●									●	1	1	0	1	0
27				●								●	1	1	0	1	1
28					●							●	1	1	1	0	0
29						●						●	1	1	1	0	1
30							●					●	1	1	1	1	0
31								●				●	1	1	1	1	1

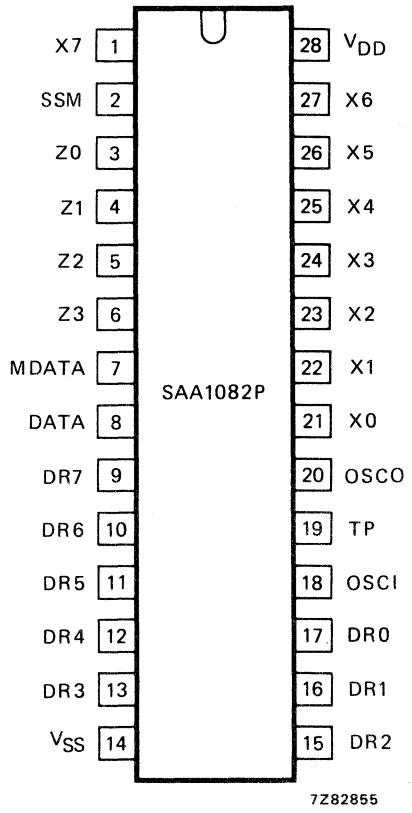


Fig. 5 Pinning diagram.

PINNING

14	V_{SS}	negative supply (0 V)
28	V_{DD}	positive supply
21	X0	keyboard command inputs with P-channel pull-up transistors
22	X1	
23	X2	
24	X3	
25	X4	
26	X5	
27	X6	
1	X7	
3	Z0	keyboard system inputs with P-channel pull-up transistors
4	Z1	
5	Z2	
6	Z3	
2	SSM	system mode selection input
19	TP	test pin
18	OSCI	oscillator input
20	OSCO	oscillator output
17	DR0	scan driver outputs with open drain N-channel transistors
16	DR1	
15	DR2	
13	DR3	
12	DR4	
11	DR5	
10	DR6	
9	DR7	
7	MDATA	remote signal outputs (3-state outputs)
8	DATA	

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range	V_{DD}	−0,5 to + 15	V
Input voltage range	V_I	−0,5 to (V_{DD} + 0,5)	V*
Input current	$\pm I_I$	max. 10	mA
Output voltage range	V_O	−0,5 to (V_{DD} + 0,5)	V*
Output current	$\pm I_O$	max. 10	mA
Power dissipation output OSCO	P_O	max. 50	mW
Power dissipation per output (all other outputs)	P_O	max. 100	mW
Total power dissipation per package	P_{tot}	max. 200	mW
Operating ambient temperature range	T_{amb}	−25 to + 85	°C
Storage temperature range	T_{stg}	−55 to + 150	°C

* V_{DD} + 0,5 V should not exceed 15 V.

CHARACTERISTICS

V_{SS} = 0; T_{amb} = −25 to +85 °C; unless otherwise specified.

	V_{DD} V	symbol	min.	typ.	max.	conditions
Supply voltage		V_{DD}	4,75	–	12,6 V	
Quiescent supply current; excluding the leakage current of the open drain N-channel outputs	12,6	I_{DD}	–	–	10 μA	I_O = mA (all outputs) X0 to X7, Z0 to Z3 at V_{DD}; all other inputs at V_{DD} or V_{SS}; T_{amb} = 25 °C
Inputs						
Keyboard inputs X and Z with P-channel pull-up transistors						
Input current at each input	4,75 to 12,6	$-I_I$	12	–	700 μA	V_I = 0 V; TP = SSM = LOW
Input voltage HIGH	4,75 to 12,6	V_{IH}	0,7V_{DD}	–	V_{DD} V	
Input voltage LOW	4,75 to 12,6	V_{IL}	0	–	0,3V_{DD} V	
Input leakage current						
V_I = 12,6 V	12,6	I_{IR}	–	–	1 μA	TP = HIGH; T_{amb} = 25 °C
V_I = 0 V	12,6	$-I_{IR}$	–	–	1 μA	TP = HIGH; T_{amb} = 25 °C
SSM, TP, OSCI inputs						
Input voltage HIGH	4,75 to 12,6	V_{IH}	0,7V_{DD}	–	V_{DD} V	
Input voltage LOW	4,75 to 12,6	V_{IL}	0	–	0,3V_{DD} V	
Input leakage current						
V_I = 12,6 V	12,6	I_{IR}	–	–	1 μA	T_{amb} = 25 °C
V_I = 0 V	12,6	$-I_{IR}$	–	–	1 μA	T_{amb} = 25 °C
Outputs						
DATA, MDATA outputs						
Output voltage HIGH	4,75 to 12,6	V_{OH}	V_{DD}−0,5	–	– V	$-I_{OH}$ = 0,7 mA*
Output voltage LOW	4,75 to 12,6	V_{OL}	–	–	0,4 V	I_{OL} = 0,7 mA*
Output leakage current						
V_O = 12,6 V	12,6	I_{OR}	–	–	10 μA	
V_O = 12,6 V	12,6	I_{OR}	–	–	1 μA	T_{amb} = 25 °C
V_O = 0 V	12,6	$-I_{OR}$	–	–	20 μA	
V_O = 0 V	12,6	$-I_{OR}$	–	–	2 μA	T_{amb} = 25 °C
DR0 to DR7 outputs						
Output voltage LOW	4,75 to 12,6	V_{OL}	–	–	0,4 V	I_{OL} = 0,7 mA*
Output leakage current						
V_O = 12,6 V	12,6	I_{OR}	–	–	10 μA	
V_O = 12,6 V	12,6	I_{OR}	–	–	1 μA	T_{amb} = 25 °C

* See next page.

CHARACTERISTICS (continued)

V_{SS} = 0; T_{amb} = −25 to + 85 °C; unless otherwise specified

	V_{DD} V	symbol	min.	typ.	max.	conditions
Outputs (continued)						
OSCO output						
Output voltage HIGH	4,75 to 12,6	V_{QH}	V_{DD}−0,5	–	– V	$-I_{QH}$ = 0,15 mA* OSCI at V_{SS}
Output voltage LOW	4,75 to 12,6	V_{QL}	–	–	0,5 V	$-I_{QL}$ = 0,4 mA* OSCI at V_{DD}
Maximum input frequency; C_L = 40 pF see also Fig. 6						
	4,75	f_{OSCI}	75	–	– kHz	
	6	f_{OSCI}	120	–	– kHz	
	12,6	f_{OSCI}	300	–	– kHz	

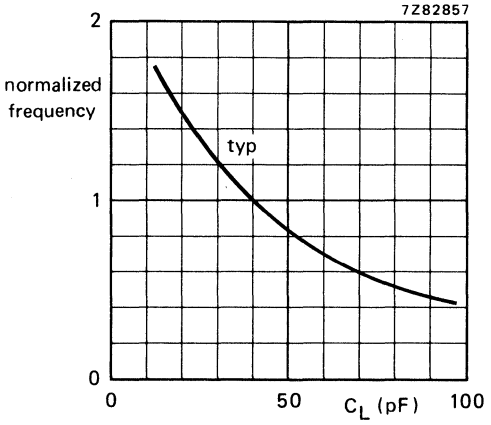


Fig. 6 Typical normalized input frequency as a function of the load capacitance.

* This d.c. test condition protects the a.c. performance of the output. The d.c. current requirement is lower in the actual application.

APPLICATION INFORMATION

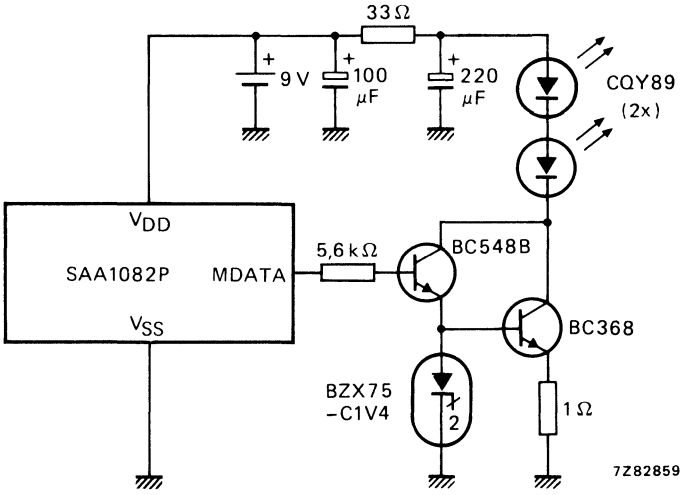


Fig. 7 A typical transmitter output stage.

MICROPROCESSOR CONTROLLED STEREO SOUND GENERATOR FOR SOUND EFFECTS AND MUSIC SYNTHESIS

GENERAL DESCRIPTION

The SAA1099 is a monolithic integrated circuit designed for generation of stereo sound effects and music synthesis.

Features

- Six frequency generators
  - eight octaves per generator
  - 256 tones per octave
- Two noise generators
- Six noise/frequency mixers
- Twelve amplitude controllers
- Two envelope controllers
- Two 6-channel mixers/current sink analogue output stages
- TTL input compatible
- Readily interfaces to 8-bit microcontroller
- Minimal peripheral components
- Simple output filtering

Applications

- Consumer games systems
- Home computers
- Electronic organs
- Arcade games
- Toys
- Chimes/alarm clocks

QUICK REFERENCE DATA

Supply voltage (pin 18)	V_{DD}	typ.	5 V
Supply current (pin 18)	I_{DD}	typ.	55 mA
Reference current (pin 6)	I_{ref}	typ.	250 μA
Total power dissipation	P_{tot}		450 mW
Operating ambient temperature range	T_{amb}		0 to + 70 °C

PACKAGE OUTLINE

18-lead DIL; plastic (SOT-102CS).

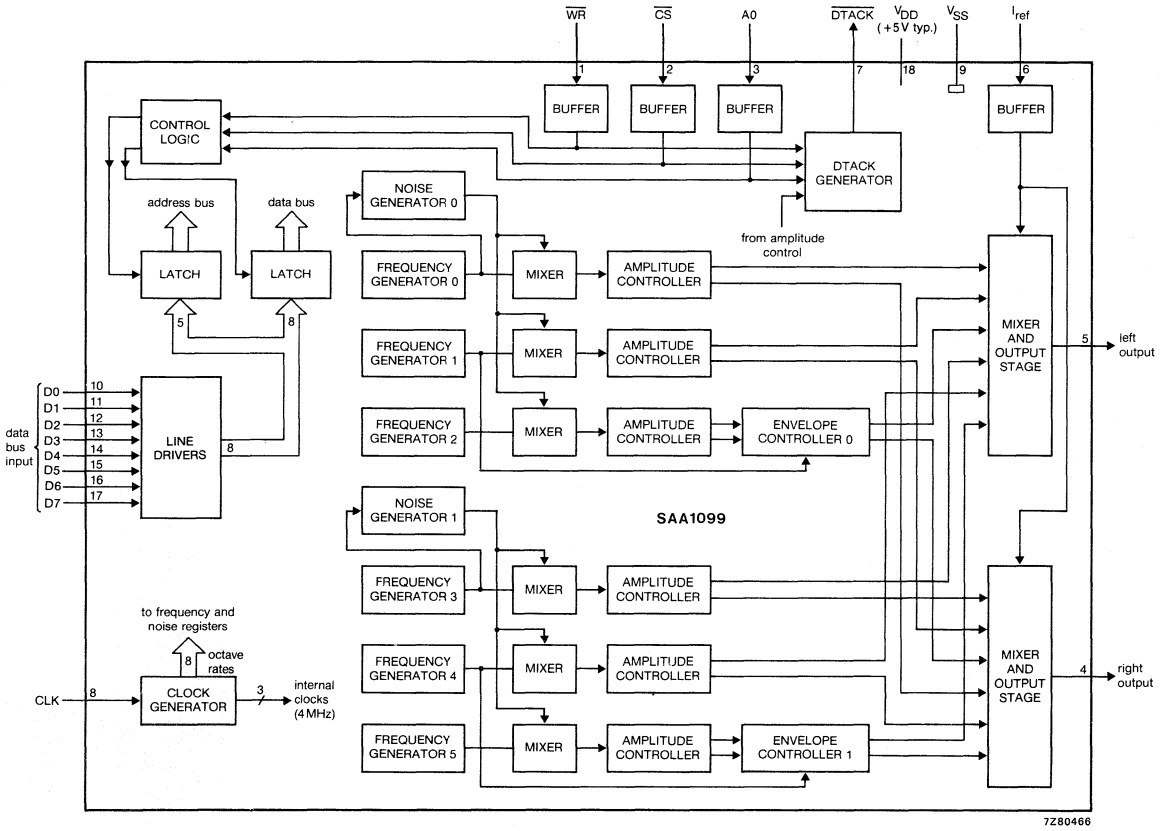


Fig. 1 Block diagram.

PINNING

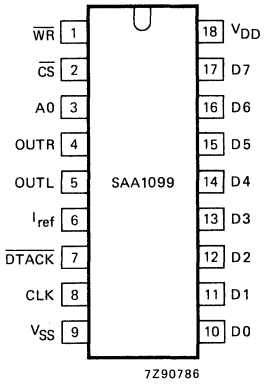


Fig. 2 Pinning diagram.

PIN DESIGNATION

1	$\overline{WR}$	**Write Enable**: active LOW input which operates in conjunction with $\overline{CS}$ and A0 to allow writing to the internal registers.
2	$\overline{CS}$	**Chip Select**: active LOW input to identify valid $\overline{WR}$ inputs to the chip. This input also operates in conjunction with $\overline{WR}$ and A0 to allow writing to the internal registers.
3	A0	**Control/Address select**: input used in conjunction with $\overline{WR}$ and $\overline{CS}$ to load data to the control register (A0 = 0) or the address buffer (A0 = 1).
4	OUTR	**Right channel output**: a 7-level current sink analogue output for the 'right' component. This pin requires an external load resistor.
5	OUTL	**Left channel output**: a 7-level current sink analogue output for the 'left' component. This pin requires an external load resistor.
6	I_{ref}	**Reference current supply**: used to bias the current sink outputs.
7	$\overline{DTACK}$	**Data Transfer Acknowledge**: open drain output, active LOW to acknowledge successful data transfer. On completion of the cycle $\overline{DTACK}$ is set to inactive.
8	CLK	**Clock**: input for an externally generated clock at a nominal frequency of 8 MHz.
9	V_{SS}	**Ground**: 0 V.
10-17	D0-D7	**Data**: Data bus input.
18	V_{DD}	**Power supply**: + 5 V typical.

FUNCTIONAL DESCRIPTION

The following sections provide a detailed functional description of the SAA1099 as shown in the block diagram, Fig. 1.

Frequency generators

Six frequency generators can each select one of 8 octaves and one of 256 tones within an octave. A total frequency range of 30 Hz to 7,74 kHz is available. The outputs may also control noise or envelope generators. All frequency generators have an enable bit which switches them on and off, making it possible to preselect a tone tone and to make it inaudible when required.

The frequency ranges per octave are:

Octave	Frequency range
0	30 Hz to 60 Hz
1	60 Hz to 122 Hz
2	122 Hz to 244 Hz
3	244 Hz to 488 Hz
4	489 Hz to 976 Hz
5	978 Hz to 1,95 kHz
6	1,95 kHz to 3,90 kHz
7	3,91 kHz to 7,81 kHz

Noise generators

The two noise generators both have a programmable output. This may be a software controlled noise via one of the frequency controlled generators or one of three pre-defined noises. There is no tone produced by the frequency generator when it is controlling the noise generator. The noise produced is based on double the frequency generator output, i.e. a range of 61 Hz to 15,6 kHz.
In the event of a pre-defined noise being chosen, the output of noise generator 0 can be mixed with frequency generator 0, 1 and 2; and the output of noise generator 1 can be mixed with frequency generator 3, 4 and 5. In order to produce an equal level of noise and tone outputs (when both are mixed) the amplitude of the tone is increased. The three pre-defined noises are based on a clock frequency of 7,8 kHz, 15,6 kHz or 31,25 kHz.

Noise/frequency mixers

Six noise/frequency mixers each with four selections

- Channel off
- Frequency only
- Noise only
- Noise and frequency

Each mixer channel has one of the frequency generator outputs fed to it, three channels use noise generator 0 and the other three use noise generator 1.

Amplitude controllers

Each of the six channel outputs from the mixer is split up into a right and left component giving effectively twelve amplitude controllers. An amplitude of 16 possible levels is assigned to each of the twelve signals. With this configuration a stereo effect can be achieved by varying only the amplitude component. The moving of a sound from one channel to the other requires, per tone, only one update of the amplitude register contents.
When an envelope generator is used, the amplitude levels are restricted. The number of levels available is then reduced to eight. This is achieved by disabling the least significant bit (LSB) of the amplitude control.

Envelope controllers

Two of the six tone generators are under envelope control. This applies to both the left and right outputs from the tone generator.
The envelope has the following eight possible modes:

- Amplitude is zero
- Single attack
- Single decay
- Single attack-decay (triangular)
- Maximum amplitude
- Continuous attack
- Continuous decay
- Continuous attack-decay

The timing of the envelope controllers is programmable using one of the frequency generators (see Fig. 1). When the envelope mode is selected for a channel its control resolution is halved for that channel from 16 levels to 8 levels by rounding down to the nearest even level.
There is also the capability of controlling the 'right' component of the channel with inverse of the 'left' component, which remains as programmed.

A direct enable permits the start of an envelope to be defined, and also allows termination of an envelope at any time. The envelope rate may be controlled by a frequency channel (see Fig. 1), or by the microprocessor writing to the address buffer register. If the frequency channel controlled is OFF (NE = FE = 0) the envelope will appear at the output, which provides an alternative 'non-square' tone capability. In this event the frequency will be the envelope rate, which provided the rate is from the frequency channel, will be a maximum of 1 kHz. Higher frequencies of up to 2 kHz can be obtained by the envelope resolution being halved from 16 levels to 8 levels. Rates quoted are based on the input of a 8 MHz clock.

Six-channel mixers/current sink analogue output stages

Six channels are mixed together by the two mixers allowing each one to control one of six equally weighted current sinks, to provide a seven level analogue output.

Command/control select

In order to simplify the microprocessor interface the command and control information is multiplexed. To select a register in order to control frequencies, amplitudes, etc. the command-register has to be loaded. The contents of this register determines to which register the data is written in the next control-cycle. If a continuous update of the control-register is necessary, only the control-information has to be written (the command-information does not change).
If the command/control select (A0) is logic 0, the byte transfer is control; if A0 is logic 1, the byte transfer is command.

Interface to microprocessor

The SAA1099 is a data bus based I/O peripheral. Depending on the value of the command/control signal (A0) the $\overline{CS}$ and $\overline{WR}$ signals control the data transfer from the microprocessor to the SAA1099. The data-transfer-acknowledge ($\overline{DTACK}$) indicates that the data transfer is completed. When, during the write cycle, the microprocessor recognizes the $\overline{DTACK}$, the bus cycle will be completed by the processor.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 18)	V_{DD}	−0,3 to + 7,5	V
Maximum input voltage	V_I	−0,3 to + 7,5	V
at V_{DD} = 4,5 to 5,5 V	V_I	−0,5 to + 7,5	V
Maximum output current	I_O	max. 10	mA
Total power dissipation	P_{tot}	450	mW
Storage temperature range	T_{stg}	−55 to + 125	°C
Operating ambient temperature range	T_{amb}	0 to + 70	°C
Electrostatic handling*	V_{es}	−1000 to + 1000	V

* Equivalent to discharging a 250 μF capacitor through a 1 kΩ series resistor.

D.C. CHARACTERISTICS

V_{DD} = 5 V; T_{amb} = 0 to 70 °C; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply					
Supply voltage	V_{DD}	4,5	5,0	5,5	V
Supply current	I_{DD}	–	55	90	mA
Reference current (note 1)	I_{ref}	100	250	400	μA
INPUTS					
Input voltage HIGH	V_{IH}	2,0	–	6,0	V
Input voltage LOW	V_{IL}	−0,5	–	0,8	V
Input leakage current	$\pm I_{LI}$	–	–	10	μA
Input capacitance	C_I	–	–	10	pF
OUTPUTS					
$\overline{DTACK}$ (open drain; note 2)					
Output voltage LOW at I_{OL} = 3,2 mA	V_{OL}	0	–	0,4	V
Voltage on pin 7 (OFF state)	V_{7-9}	−0,3	–	6,0	V
Output capacitance (OFF state)	C_O	–	–	10	pF
Load capacitance	C_L	–	–	150	pF
Output leakage current (OFF state)	$-I_{LO}$	–	–	10	μA
Audio outputs (pins 4 and 5)					
With fixed I_{ref} (note 3)					
One channel on	I_{01}/I_{ref}	90	–	125	%
Six channels on	$I_{06}/6xI_{ref}$	85	–	120	%
With I_{ref} = 250 μA; R_L = 1,1 kΩ (± 5%)					
One channel on	I_{01}/I_{ref}	95	–	115	%
Six channels on	$I_{06}/6xI_{ref}$	90	–	110	%
Output current one channel on	I_{01}	238	–	288	μA
Output current six channels on	I_{06}	1,38	–	1,65	mA
With resistor supplying I_{ref} (note 4)					
Output current one channel on	I_{01}	155	–	270	μA
Output current six channels on	I_{06}	0,94	–	1,65	mA
Load resistance	R_L	600	–	–	Ω
D.C. leakage current all channels off	$-I_{LO}$	–	–	10	μA
Maximum current difference between left and right current sinks (note 5)	$\pm I_{Omax}$	–	–	15	%
Signal-to-noise ratio (note 6)	S/N	–	tbf	–	dB

A.C. CHARACTERISTICS

V_{DD} = 5 V; T_{amb} = 0 to 70 °C; timing measurements taken at 2,0 V for a logic 1 and 0,8 V for a logic 0 unless otherwise specified (see waveforms Figs 3 and 4)

parameter	symbol	min.	typ.	max.	unit
Bus interface timing (see Fig. 3)					
A0 set-up time to $\overline{CS}$ fall	t_{ASC}	0	–	–	ns
$\overline{CS}$ LOW to $\overline{WR}$ fall	t_{CSW}	30	–	–	ns
A0 set-up time to $\overline{WR}$ fall	t_{ASW}	50	–	–	ns
$\overline{WR}$ LOW time	t_{WL}	100	–	–	ns
Data bus valid to $\overline{WR}$ rise	t_{BSW}	100	–	–	ns
$\overline{DTACK}$ fall delay from $\overline{WR}$ fall (note 7)	t_{DFW}	0	–	85	ns
A0 hold time from $\overline{WR}$ HIGH	t_{AHW}	0	–	–	ns
$\overline{CS}$ hold time from $\overline{WR}$ HIGH	t_{CHW}	0	–	–	ns
Data bus hold time from $\overline{WR}$ HIGH	t_{DHW}	0	–	–	ns
$\overline{DTACK}$ rise delay from $\overline{WR}$ HIGH	t_{DRW}	0	–	100	ns
Bus cycle time (note 8)	t_{CY}	2CP	–	–	
Bus cycle time (note 9)	t_{CY}	8CP	–	–	
Clock input timing (see Fig. 4)					
Clock period	t_{CLK}	120	125	255	ns
Clock LOW time	t_{HIGH}	55	–	–	ns
Clock HIGH time	t_{LOW}	55	–	–	ns

Notes to the characteristics

1. Using an external constant current generator to provide a nominal I_{ref} or external resistor connected to V_{DD}.
2. This output is short-circuit protected to V_{DD} and V_{SS}.
3. Measured with I_{ref} a constant value between 100 and 400 μA; load resistance (R_L) allowed to match E24 (5%) in all applications via:

$$R_L = \frac{0{,}27775 \pm 0{,}03611}{I_{ref}}.$$

4. Measured with R_{ref} = 10 kΩ (± 5%) connected between I_{ref} and V_{DD}; R_L = 820 Ω (± 5%); OUTR and OUTL short-circuit protected to V_{SS}.
5. Left and right outputs must be driven with identical configuration.
6. Sample tested value only.
7. This timing parameter only applies when no wait states are required; otherwise parameter is invalid.
8. The minimum bus cycle time of two clock periods is for loading all registers except the amplitude registers.
9. The minimum bus cycle time of eight clock periods is for loading the amplitude registers. In a system using $\overline{DTACK}$ it is possible to achieve minimum times of 500 ns. Without $\overline{DTACK}$ the parameter given must be used.

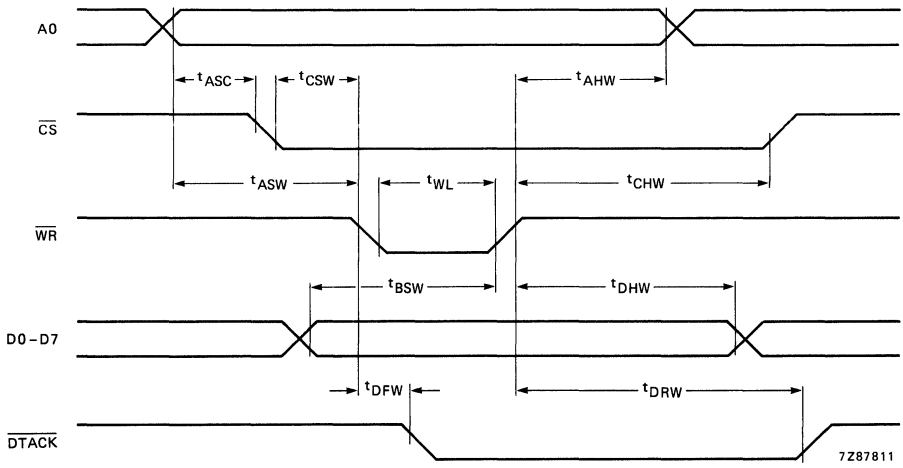


Fig. 3 Bus interface waveforms.

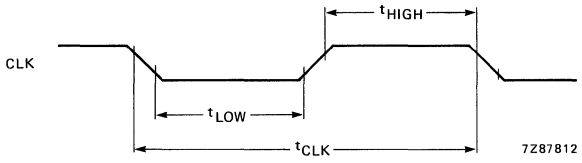


Fig. 4 Clock input waveform.

DEVELOPMENT DATA

APPLICATION INFORMATION

Device operation

The SAA1099 uses pulse width modulation to achieve amplitude and envelope levels. The twelve signals are mixed in an analogue format (6 'left' and 6 'right') before leaving the chip. The amplitude and envelope signals chop the output at a minimum rate of 62,5 kHz, compared with the highest tone output of 7,74 kHz. Simple external low-pass filtering is used to remove the high frequency components.

Rates quoted are based on the input of a 8 MHz clock.

A data bus based write only structure is used to load the on-board registers. The data bus is used to load the address for a register, and subsequently the data to that register. Once the address is loaded multiple data loads to that register can be performed.

The selection of address or data is made by the single address bit A0, as shown in register maps Table 1 and Table 2.

The bus control signals $\overline{WR}$ and $\overline{CS}$ are designed to be compatible with a wide range of microprocessors, a $\overline{DTACK}$ output is included to optimise the interface with an S68000 series microprocessor. In most bus cycles $\overline{DTACK}$ will be returned immediately, this applies to all register address load cycles and all except amplitude data load cycles. With respect to amplitude data, a number of wait cycles may need to be performed, depending on the time since the previous amplitude load. $\overline{DTACK}$ will indicate the number of required waits.

Register description (see Tables 2 and 3)

The amplitudes are assigned with 'left' and 'right' components in the same byte, on a channel by channel basis. The spare locations that are left between blocks of registers is to allow for future expansion, and should be written as zero's. The tone within an octave is defined by eight bits and the octave by three bits. Note that octaves are paired (0/1, 2/3 etc.). The frequency and noise enables are grouped together for ease of programming. The controls for noise 'colour' (clock rate) are grouped in one byte.

The envelope registers are positioned in adjacent locations. There are two types of envelope controls, direct acting controls and buffered controls. The direct acting controls always take immediate effect, and are:

- Envelope enable (reset)
- Envelope resolution (16/8 level)

The buffered controls are acted upon only at the times shown in Fig. 5 and control selection of:

- Envelope clock source
- Waveform type
- Inverted/non-inverted 'right' component

Table 1 External memory map

select	data bus inputs								operations
A0	D7	D6	D5	D4	D3	D2	D1	D0	
0	D7	D6	D5	D4	D3	D2	D1	D0	data for internal registers
1	X	X	X	A4	A3	A2	A1	A0	internal register address

Where X = don't care state.

Table 2 Internal register map.

register address	data bus inputs D7	D6	D5	D4	D3	D2	D1	D0	operations
00	AR03	AR02	AR01	AR00	AL03	AL02	AL01	AL00	amplitude 0 right channel; left channel
01	1	1	1	1	1	1	1	1	amplitude 1 right/left
02	2	2	2	2	2	2	2	2	amplitude 2 right/left
03	3	3	3	3	3	3	3	3	amplitude 3 right/left
04	4	4	4	4	4	4	4	4	amplitude 4 right/left
05	5	5	5	5	5	5	5	5	amplitude 5 right/left
06	X	X	X	X	X	X	X	X	
07	X	X	X	X	X	X	X	X	
08	F07	F06	F05	F04	F03	F02	F01	F00	frequency of tone 0
09	1	1	1	1	1	1	1	1	frequency of tone 1
0A	2	2	2	2	2	2	2	2	frequency of tone 2
0B	3	3	3	3	3	3	3	3	frequency of tone 3
0C	4	4	4	4	4	4	4	4	frequency of tone 4
0D	F57	F56	F55	F54	F53	F52	F51	F50	frequency of tone 5
0E	X	X	X	X	X	X	X	X	
0F	X	X	X	X	X	X	X	X	
10	X	012	011	010	X	002	001	000	octave 1; octave 0
11	X	032	031	030	X	022	021	020	octave 3; octave 2
12	X	052	051	050	X	042	041	040	octave 5; octave 4
13	X	X	X	X	X	X	X	X	
14	X	X	FE5	FE4	FE3	FE2	FE1	FE0	frequency enable
15	X	X	NE5	NE4	NE3	NE2	NE1	NE0	noise enable
16	X	X	N11	N10	X	X	N01	N00	noise generator 1; noise generator 0
17	X	X	X	X	X	X	X	X	
18	E07	X	E05	E04	E03	E02	E01	E00	envelope generator 0
19	E17	X	E15	E14	E13	E12	E11	E10	envelope generator 1
1A	X	X	X	X	X	X	X	X	
1B	X	X	X	X	X	X	X	X	
1C	X	X	X	X	X	X	X	SE	sound enable (all channels)
1D	X	X	X	X	X	X	X	X	
1E	X	X	X	X	X	X	X	X	
1F	X	X	X	X	X	X	X	X	

Where:
All don't cares (X) should be written as zero's.
00 to 1F block of registers repeats eight times in the block between addresses 00 to FF (full internal memory map).

APPLICATION INFORMATION (continued)

Table 3 Register description

bit	description
ARn3; ARn2; ARn1; ARn0 (n = 0,5)	4 bits for amplitude control of right channel 0 0 0 0 minimum amplitude (off) 1 1 1 1 maximum amplitude
ALn3; ALn2; ALn1; ALn0 (n = 0,5)	4 bits for amplitude control of left channel 0 0 0 0 minimum amplitude (off) 1 1 1 1 maximum amplitude
Fn7 to Fn0 (n = 0,5)	8 bits for frequency control of the six frequency generators 0 0 0 0 0 0 0 0 lowest frequency 1 1 1 1 1 1 1 1 highest frequency
On2; On1; On0 (n = 0,5)	3 bits for octave control 0 0 0 lowest octave (30 Hz to 60 Hz) 0 0 1 (60 Hz to 122 Hz) 0 1 0 (122 Hz to 244 Hz) 0 1 1 (244 Hz to 488 Hz) 1 0 0 (489 Hz to 976 Hz) 1 0 1 (978 Hz to 1,95 kHz) 1 1 0 (1,95 kHz to 3,90 kHz) 1 1 1 highest octave (3,91 kHz to 7,81 kHz)
FEn (n = 0,5)	frequency enable bit (one tone per generator) FEn = 0 indicates that frequency 'n' is off
NEn (n = 0,5)	noise enable bit (one tone per generator) NEn = 0 indicates that noise 'n' is off
Nn1; Nn0 (n = 0,1)	2 bits for noise generator control. These bits select the noise generator rate (noise 'colour') Nn1 Nn0 clock frequency (kHz) 0 0 31,3 0 1 15,6 1 0 7,6 1 1 61 to 15,6 (frequency generator 0/2)

bit	description
En7; En5 to En0 (n = 0,1)	7 bits for envelope control En0 0 left and right component have the same envelope 1 right component has inverse of envelope that is applied to left component En3 En2 En1 0 0 0 zero amplitude 0 0 1 maximum amplitude 0 1 0 single decay 0 1 1 repetitive decay 1 0 0 single triangular 1 0 1 repetitive triangular 1 1 0 single attack 1 1 1 repetitive attack En4 0 4 bits for envelope control (maximum frequency = 976 Hz) 1 3 bits for envelope control (maximum frequency = 1,95 kHz) En5 0 internal envelope clock (frequency generator 1 or 4) 1 external envelope clock (address write pulse) En7 0 reset (no envelope control) 1 envelope control enabled
SE	SE sound enable for all channels (reset on power-up to 0) 0 all channels disabled 1 all channels enabled

Note

All rates given are based on the input of a 8 MHz clock.

APPLICATION INFORMATION (continued)

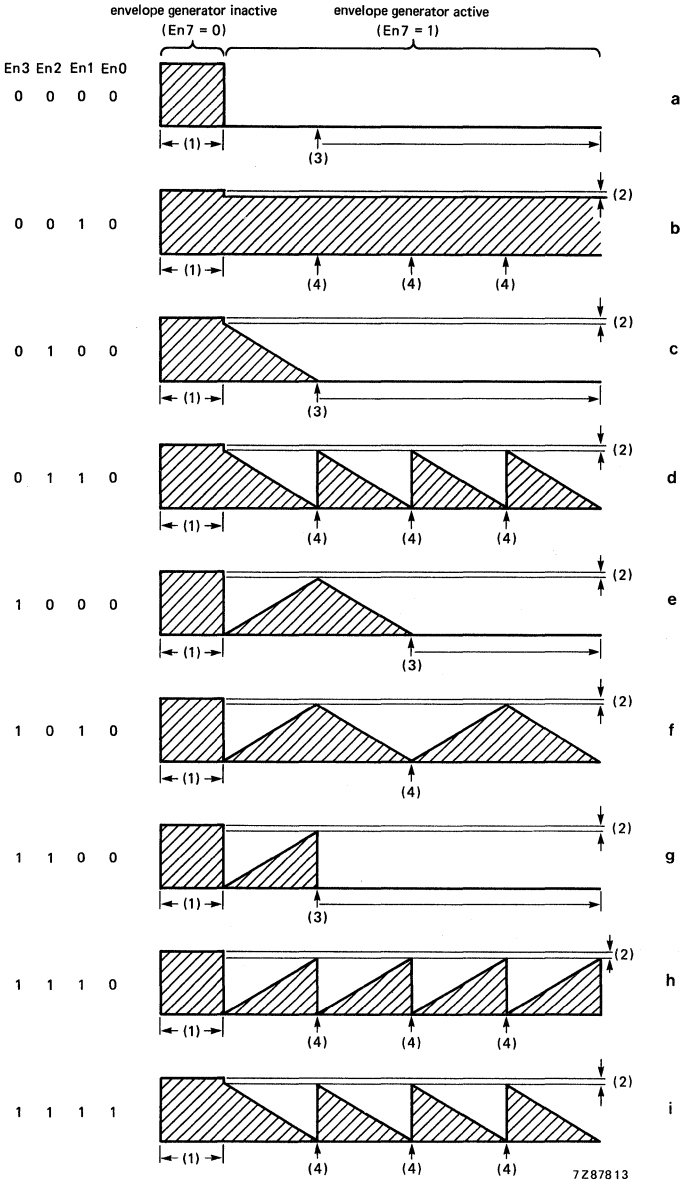


Fig. 5 Envelope waveforms.

Notes to Fig. 5

(1) The level at this time is under amplitude control only (En7 = 0; no envelope).

(2) When the generator is active (En7 = 1) the maximum level possible is 15/16ths of the amplitude level, rounded down to the nearest eight. When the generator is inactive (En7 = 0) the level will be 16/16ths of the amplitude level.

(3) After position (3) the buffered controls will be acted upon when loaded.

(4) At positions (4) the buffered controls will be acted upon if already loaded.

(5) Waveforms 'a' to 'h' show the left channel (En0 = 0; left and right components have the same envelope).
Waveform 'i' shows the right channel (En0 = 1; right component inverse of envelope applied to left).

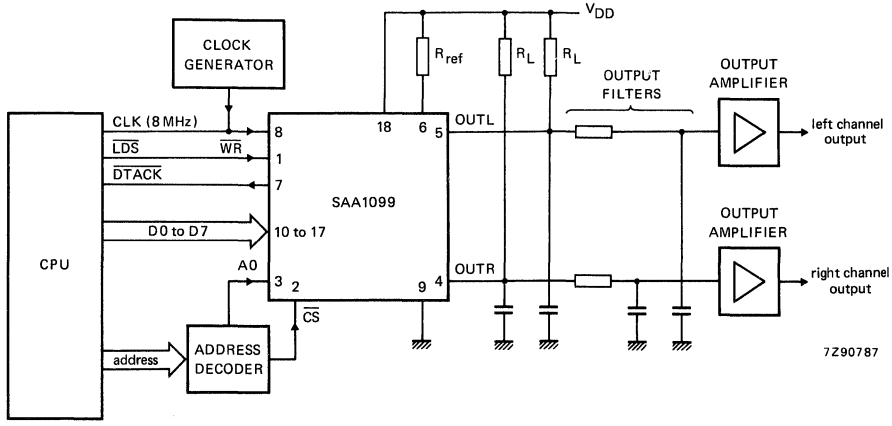


Fig. 6 Typical application circuit diagram.

TUNER SWITCHING CIRCUIT

The SAA1300 is for switching on and off the supply lines of various circuit parts via an I²C bus signal. Furthermore, it can be used to supply current for switching diodes in radio and television tuners. It contains 5 output stages, which are capable of supplying up to 100 mA in the ON state or sinking up to −100 μA in the OFF state.

Current limiting and short-circuit protection are included. The output stages are driven by a shift register/latch combination which is loaded via data from the I²C bus. A power-on reset of the latches ensures the OFF state of the output stages (OUT 2 to OUT 5) without data reception from the I²C bus. A subaddressing system allows the connection of up to three circuits on the same I²C bus lines; one of the outputs (OUT 1, pin 7) can also be used as an input to select the device via a simple internal A/D converter.

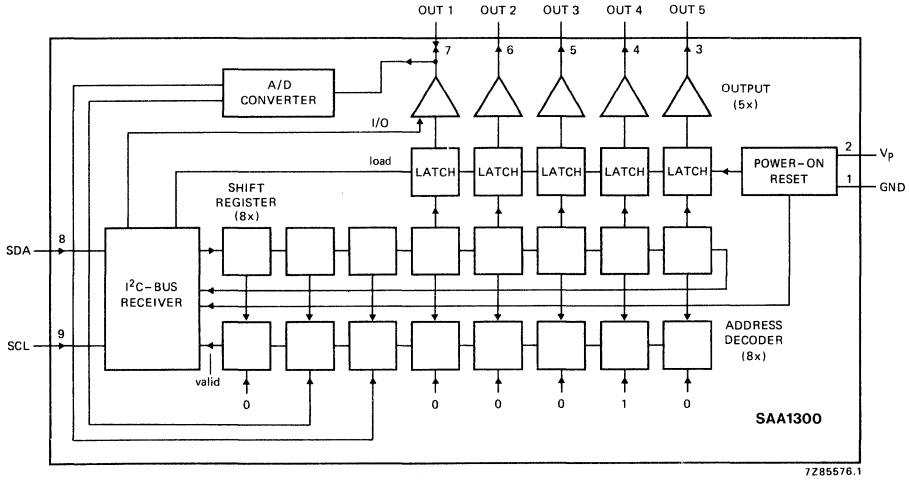


Fig. 1 Block diagram.

PACKAGE OUTLINE

9-lead SIL; plastic (SOT-142B).

PINNING

pin no.	symbol	function
1	GND	ground
2	V_P	positive supply
3	OUT 5	outputs
4	OUT 4	
5	OUT 3	
6	OUT 2	
7	OUT 1	output and subaddressing input
8	SDA	serial data line (I^2C bus)
9	SCL	serial clock line (I^2C bus)

I^2C BUS INFORMATION*

Address, first byte

0 1 0 0 0 A B 0 where,

A	B	function	condition
0	0	general address	OUT 1 = output
0	1	OUT 1 = input	address accepted if $V_{OUT\,1} = V_{OUT\,L}$ (LOW)
1	0	OUT 1 = input	address accepted if $V_{OUT\,1} = V_{OUT\,H}$ (HIGH)
1	1	OUT 1 = input	address accepted if $V_{OUT\,1} = V_{OUT\,M}$ (MEDIUM)

Data, second byte

OUT 5, OUT 4, OUT 3, OUT 2, OUT 1, X, X, X

The I/O output stage (OUT 1) is switched as an input stage after a power-on reset. It depends on the contents of the first data transmission whether the output stage is switched as an output or remains as an input.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	13,2 V
Input voltage range at SDA, SCL	V_I		−0,5 to + 13,7 V
Input voltage range at OUT 1	V_I		−0,5 to + 12,5 V
Output voltage range at OUT 1 to OUT 5	V_O		−0,5 to + 12,5 V
Input current at SDA, SCL	I_I	max.	20 mA
Input current at OUT 1	I_I	max.	20 mA
Total power dissipation	P_{tot}	max.	650 mW
Storage temperature range	T_{stg}		−40 to + 125 °C
Operating ambient temperature range	T_{amb}		−20 to + 80 °C

* Detailed information is given in a separate data sheet.

CHARACTERISTICS

V_P = 8 V; T_{amb} = 25 °C; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply (pin 2)					
Supply voltage range	V_P	4	–	12	V
Supply current	I_P	–	10	–	mA
Power-on reset level output stage in "OFF" condition	V_{PR}	–	–	3,5	V
Maximum power dissipation*	P_{max}	–	650	–	mW
Inputs SDA, SCL (pins 8 and 9)					
Input voltage HIGH	V_{IH}	2,8	–	V_P + 0,5	V
Input voltage LOW	V_{IL}	0	–	1,8	V
Input current HIGH	$-I_{IH}$	–	–	50	μA
Input current LOW	I_{IH}	–	–	0,1	μA
Acknowledge sink current	I_{ACK}	2,5	–	–	mA
Maximum input frequency	$f_{i\,max}$	100	–	–	kHz
Outputs OUT 1 to OUT 5 (pins 3 to 7)					
Maximum output current; source : "ON"	I_{Oso}	+ 100	–	+ 150	mA
Maximum output current; source : "ON" T_{amb} = 80 °C	I_{Oso}	60	–	–	mA
Output voltage HIGH at I_{Oso}	V_{OH}	–	–	V_P –2	V
Output current; sink: "OFF"	I_{Osi}	–100	–300	–	μA
Output voltage LOW at I_{Osi}	V_{OL}	–	–	100	mV
Output voltage MEDIUM at I_O = 12,5 mA	V_{OM}	–	–	V_P –0,5	V
OUT 1 used as subaddressing input					
Input voltage HIGH (code 1 0)	$V_{OUT\,1H}$	0,72 V_P	–	V_P	V
Input voltage MEDIUM (code 1 1)	$V_{OUT\,1M}$	0,39 V_P	–	0,61 V_P	V
Input voltage LOW (code 0 1)	$V_{OUT\,1L}$	0	–	0,28 V_P	V

* Outputs must not be driven simultaneously at maximum source current.

REMOTE CONTROL TRANSMITTER

GENERAL DESCRIPTION

The SAA3004 transmitter IC is designed for infrared remote control systems. It has a total of 448 commands which are divided into 7 sub-system groups with 64 commands each. The sub-system code may be selected by a press button, a slider switch or hard wired.

The SAA3004 generates the pattern for driving the output stage. These patterns are pulse distance coded. The pulses are infrared flashes or modulated. The transmission mode is defined in conjunction with the sub-system address. Modulated pulses allow receivers with narrow-band preamplifiers for improved noise rejection to be used. Flashed pulses require a wide-band preamplifier within the receiver.

The SAA3004 has the following features:

- Flashed or modulated transmission
- 7 sub-system addresses
- Up to 64 commands per sub-system address
- High-current remote output at V_{DD} = 6 V ($-I_{OH}$ = 40 mA)
- Low number of additional components
- Key release detection by toggle bits
- Very low stand-by current ($< 2\ \mu A$)
- Operational current < 2 mA at 6 V supply
- Wide supply voltage range (4 to 11 V)
- Ceramic resonator controlled frequency (typ. 450 kHz)
- Encapsulation: 20-lead plastic DIL or 20-lead plastic mini-pack (SO-20)

PACKAGE OUTLINES

20-lead DIL; plastic (SOT-146C1).
20-lead mini-pack; plastic (SO-20; SOT-163AC3).

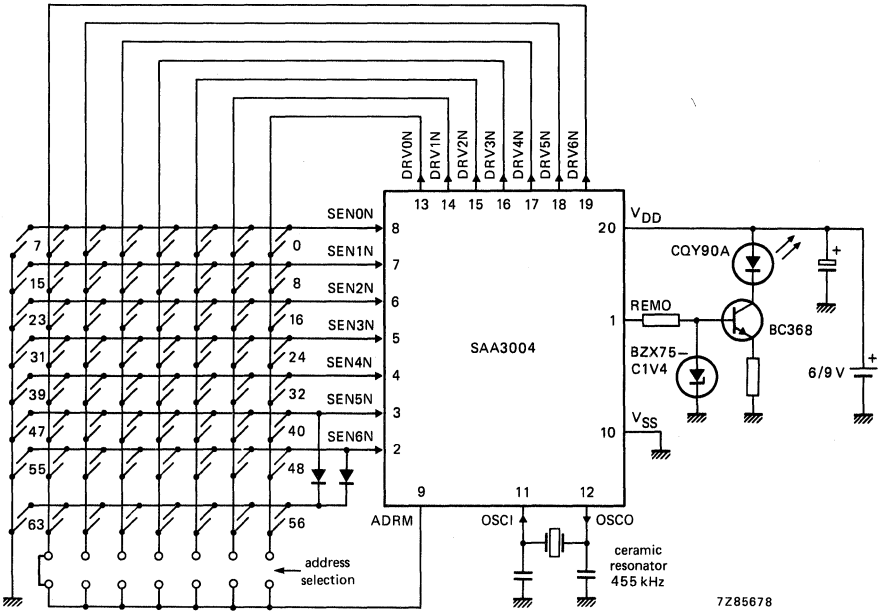


Fig. 1 Transmitter with SAA3004.

INPUTS AND OUTPUTS

Key matrix inputs and outputs (DRV0N to DRV6N and SEN0N to SEN6N)

The transmitter keyboard is arranged as a scanned matrix. The matrix consists of 7 driver outputs and 7 sense inputs as shown in Fig. 1. The driver outputs DRV0N to DRV6N are open drain N-channel transistors and they are conductive in the stand-by mode. The 7 sense inputs (SEN0N to SEN6N) enable the generation of 56 command codes. With 2 external diodes all 64 commands are addressable.The sense inputs have P-channel pull-up transistors, so that they are HIGH until they are pulled LOW by connecting them to an output via a key depression to initiate a code transmission.

Address mode input (ADRM)

The sub-system address and the transmission mode are defined by connecting the ADRM input to one or more driver outputs (DRV0N to DRV6N) of the key matrix. If more than one driver is connected to ADRM, they must be decoupled by a diode. This allows the definition of seven sub-system addresses as shown in Table 3. If driver DRV6N is connected to ADRM the data output format of REMO is modulated or if not connected, flashed.

The ADRM input has switched pull-up and pull-down loads. In the stand-by mode only the pull-down device is active. Whether ADRM is open (sub-system address 0, flashed mode) or connected to the driver outputs, this input is LOW and will not cause unwanted dissipation. When the transmitter becomes active by presssing a key, the pull-down device is switched off and the pull-up device is switched on, so that the applied driver signals are sensed for the decoding of the sub-system address and the mode of transmission.

The arrangement of the sub-system address coding is such that only the driver DRVnN with the highest number (n) defines the sub-system address, e.g. if driver DRV2N and DRV4N are connected to ADRM, only DRV4N will define the sub-system address. This option can be used in transmitters for more than one sub-system address. The transmitter may be hard-wired for sub-system address 2 by connecting DRV1N to ADRM. If now DRV3N is added to ADRM by a key or a switch, the transmitted sub-system address changes to 4.

A change of the sub-system address will not start a transmission.

Remote control signal output (REMO)

The REMO signal output stage is a push-pull type. In the HIGH state a bipolar emitter-follower allows a high output current. The timing of the data output format is listed in Tables 1 and 2.

The information is defined by the distance t_b between the leading edges of the flashed pulses or the first edge of the modulated pulses (see Fig. 3).

The format of the output data is given in Figs 2 and 3. In the flashed transmission mode the data word starts with two toggle bits T1 and T0, followed by three bits for defining the sub-system address S2, S1 and S0, and six bits F, E, D, C, B and A, which are defined by the selected key.

In the modulated transmission mode the first toggle bit T1 is replaced by a constant reference time bit (REF). This can be used as a reference time for the decoding sequence.

The toggle bits function as an indication for the decoder that the next instruction has to be considered as a new command.

The codes for the sub-system address and the selected key are given in Tables 3 and 4.

Oscillator input/output (OSCI and OSCO)

The external components must be connected to these pins when using an oscillator with a ceramic resonator. The oscillator frequency may vary between 400 kHz and 500 kHz as defined by the resonator.

DEVELOPMENT DATA

FUNCTIONAL DESCRIPTION

Keyboard operation

In the stand-by mode all drivers (DRV0N to DRV6N) are on. Whenever a key is pressed, one or more of the sense inputs (SENnN) are tied to ground. This will start the power-up sequence. First the oscillator is activated and after the debounce time t_{DB} (see Fig. 4) the output drivers (DRV0N to DRV6N) become active successively.

Within the first scan cycle the transmission mode, the applied sub-system address and the selected command code are sensed and loaded into an internal data latch. In contradiction to the command code the sub-system address is sensed only within the *first* scan cycle. If the applied sub-system address is changed while the command key is pressed, the transmitted sub-system address is not altered.

In a multiple key-stroke sequence (see Fig. 5) the command code is always altered in accordance with the sensed key.

Multiple key-stroke protection

The keyboard is protected against multiple key-strokes. If more than one key is pressed at the same time, the circuit will not generate a new output at REMO (see Fig. 5). In case of a multiple key-stroke the scan repetition rate is increased to detect the release of a key as soon as possible.

There are two restrictions caused by the special structure of the keyboard matrix:

FUNCTIONAL DESCRIPTION (continued)

- The keys switching to ground (code numbers 7, 15, 23, 31, 39, 47, 55 and 63) and the keys connected to SEN5N and SEN6N are not covered completely by the multiple key protection. If one sense input is switched to ground, further keys on the same sense line are ignored.
- SEN5N and SEN6N are not protected against multiple key-stroke on the same driver line, because this condition has been used for the definition of additional codes (code numbers 56 to 63).

Output sequence (data format)

The output operation will start when the selected code is found. A burst of pulses, including the latched address and command codes, is generated at the output REMO as long as a key is pressed. The format of the output pulse train is given in Figs 2 and 3. The operation is terminated by releasing the key or if more than one key is pressed at the same time. Once a sequence is started, the transmitted words will always be completed after the key is released.

The toggle bits T0 and T1 are incremented if the key is released for a minimum time t_{REL} (see Fig. 4). The toggle bits remain unchanged within a multiple key-stroke sequence.

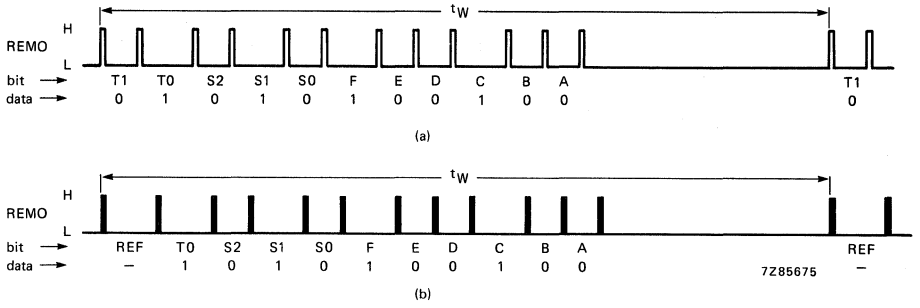
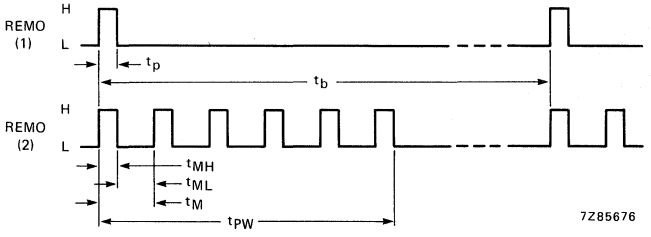


Fig. 2 Data format of REMO output; REF = reference time; T0 and T1 = toggle bits; S0, S1 and S2 = system address; A, B, C, D, E and F = command bits.
(a) flashed mode: transmission with 2 toggle bits and 3 address bits, followed by 6 command bits (pulses are flashed).
(b) modulated mode: transmission with reference time, 1 toggle bit and 3 address bits, followed by 6 command bits (pulses are modulated).



(1) Flashed pulse.
(2) Modulated pulse ($t_{PW} = (5 \times t_M) + t_{MH}$.

Fig. 3 REMO output waveform.

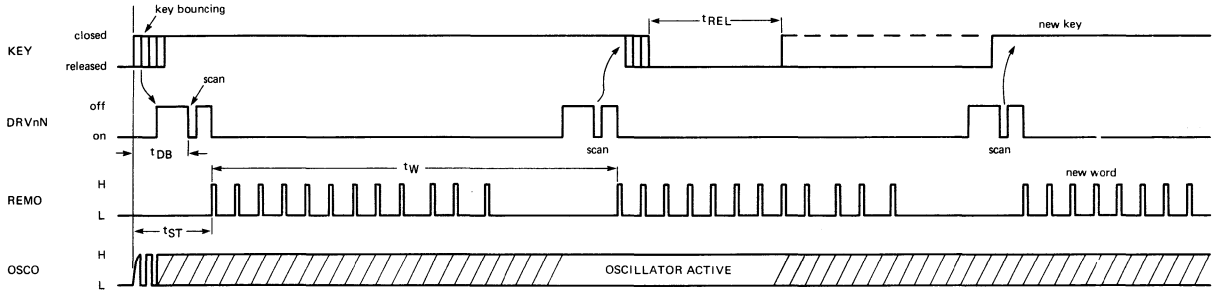


Fig. 4 Single key-stroke sequence.
Debounce time: $t_{DB} = 4$ to $9 \times T_o$.
Start time: $t_{ST} = 5$ to $10 \times T_o$.
Minimum release time: $t_{REL} = T_o$.
Word distance: t_W.

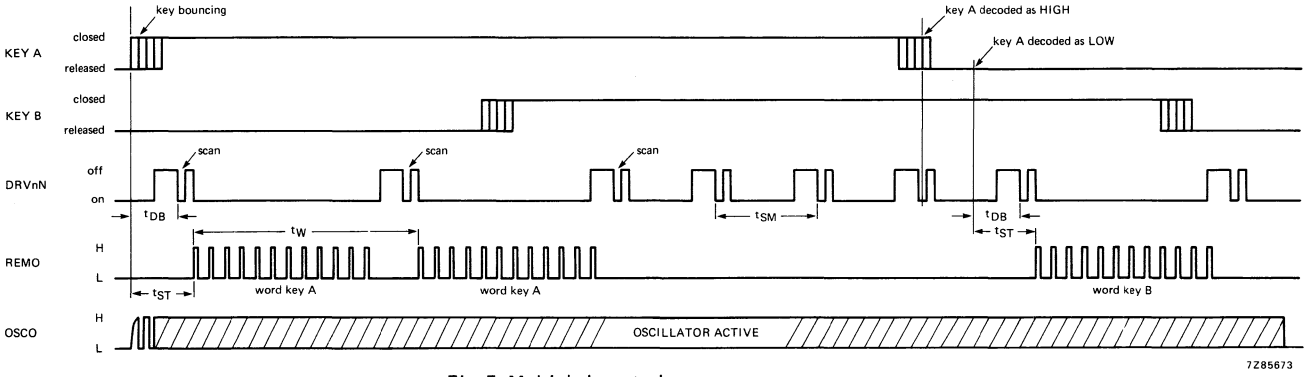


Fig. 5 Multiple key-stroke sequence.
Scan rate multiple key-stroke: $t_{SM} = 6$ to $10 \times T_o$.
For t_{DB}, t_{ST} and t_W see Fig. 4.

Table 1 Pulse train timing

mode	T_o ms	t_p μs	t_M μs	t_{ML} μs	t_{MH} μs	t_W ms
flashed	2,53	8,8	–	–	–	121
modulated	2,53	–	26,4	17,6	8,8	121

f_{osc}	455 kHz	$t_{osc} = 2{,}2\ \mu s$
t_p	$4 \times t_{osc}$	flashed pulse width
t_M	$12 \times t_{osc}$	modulation period
t_{ML}	$8 \times t_{osc}$	modulation period LOW
t_{MH}	$4 \times t_{osc}$	modulation period HIGH
T_o	$1152 \times t_{osc}$	basic unit of pulse distance
t_W	$55\,296 \times t_{osc}$	word distance

Table 2 Pulse train separation (t_b)

code	t_b
logic "0"	$2 \times T_o$
logic "1"	$3 \times T_o$
reference time	$3 \times T_o$
toggle bit time	$2 \times T_o$ or $3 \times T_o$

Table 3 Transmission mode and sub-system address selection

The sub-system address and the transmission mode are defined by connecting the ADRM input to one or more driver outputs (DRV0N to DRV6N) of the key matrix. If more than one driver is connected to ADRM, they must be decoupled by a diode.

mode	sub-system address				driver DRVnN for n =						
	#	S2	S1	S0	0	1	2	3	4	5	6
F	0	1	1	1							
L	1	0	0	0	o						
A	2	0	0	1	X	o					
S	3	0	1	0	X	X	o				
H	4	0	1	1	X	X	X	o			
E	5	1	0	0	X	X	X	X	o		
D	6	1	0	1	X	X	X	X	X	o	
M											
O	0	1	1	1							o
D	1	0	0	0	o						o
U	2	0	0	1	X	o					o
L	3	0	1	0	X	X	o				o
A	4	0	1	1	X	X	X	o			o
T	5	1	0	0	X	X	X	X	o		o
E	6	1	0	1	X	X	X	X	X	o	o
D											

o = connected to ADRM
blank = not connected to ADRM
X = don't care

Table 4 Key codes

matrix drive	matrix sense	code F	E	D	C	B	A	matrix position
DRV0N	SEN0N	0	0	0	0	0	0	0
DRV1N	SEN0N	0	0	0	0	0	1	1
DRV2N	SEN0N	0	0	0	0	1	0	2
DRV3N	SEN0N	0	0	0	0	1	1	3
DRV4N	SEN0N	0	0	0	1	0	0	4
DRV5N	SEN0N	0	0	0	1	0	1	5
DRV6N	SEN0N	0	0	0	1	1	0	6
V_{SS}	SEN0N	0	0	0	1	1	1	7
*	SEN1N	0	0	1		**		8 to 15
*	SEN2N	0	1	0		**		16 to 23
*	SEN3N	0	1	1		**		24 to 31
*	SEN4N	1	0	0		**		32 to 39
*	SEN5N	1	0	1		**		40 to 47
*	SEN6N	1	1	0		**		48 to 55
*	SEN5N and SEN6N	1	1	1		**		56 to 63

* The complete matrix drive as shown above for SEN0N is also applicable for the matrix sense inputs SEN1N to SEN6N and the combined SEN5N/SEN6N.

** The C, B and A codes are identical to SEN0N as given above.

DEVELOPMENT DATA

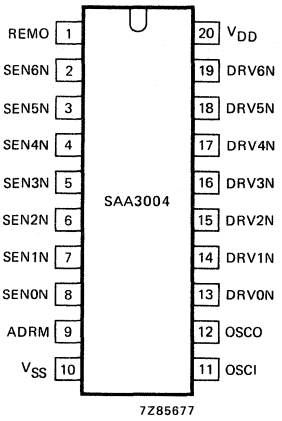


Fig. 6 Pinning diagram.

PINNING

1	REMO	remote data output
2	SEN6N	key matrix sense inputs
3	SEN5N	
4	SEN4N	
5	SEN3N	
6	SEN2N	
7	SEN1N	
8	SEN0N	
9	ADRM	address mode control input
10	V_{SS}	ground
11	OSCI	oscillator input
12	OSCO	oscillator output
13	DRV0N	key matrix drive outputs
14	DRV1N	
15	DRV2N	
16	DRV3N	
17	DRV4N	
18	DRV5N	
19	DRV6N	
20	V_{DD}	positive supply

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range	V_{DD}	−0,5 to +15		V
Input voltage range	V_I	−0,5 to V_{DD} +0,5		V
Output voltage range	V_O	−0,5 to V_{DD} +0,5		V
D.C. current into any input or output	±I	max.	10	mA
Peak REMO output current during 10 μs; duty factor = 1%	$-I_{(REMO)M}$	max.	300	mA
Power dissipation per package for T_{amb} = −20 to +70 °C	P_{tot}	max.	200	mW
Storage temperature range	T_{stg}	−55 to +150		°C
Operating ambient temperature range	T_{amb}	−20 to +70		°C

DEVELOPMENT DATA

CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; unless otherwise specified

parameter	V_{DD} (V)	symbol	min.	typ.	max.	unit
Supply voltage						
T_{amb} = 0 to +70 °C	–	V_{DD}	4	–	11	V
Supply current; active						
f_{osc} = 455 kHz;	6	I_{DD}	–	1	–	mA
REMO output unloaded	9	I_{DD}	–	3	–	mA
Supply current; inactive						
(stand-by mode)	6	I_{DD}	–	–	2	μA
T_{amb} = 25 °C	9	I_{DD}	–	–	2	μA
Oscillator frequency						
(ceramic resonator)	4 to 11	f_{osc}	400	–	500	kHz
Keyboard matrix						
Inputs SEN0N to SEN6N						
Input voltage LOW	4 to 11	V_{IL}	–	–	0,2 x V_{DD}	V
Input voltage HIGH	4 to 11	V_{IH}	0,8 x V_{DD}	–	–	V
Input current	4	$-I_I$	10	–	100	μA
V_I = 0 V	11	$-I_I$	30	–	300	μA
Input leakage current						
V_I = V_{DD}	11	I_I	–	–	1	μA
Outputs DRV0N to DRV6N						
Output voltage "ON"						
I_O = 0,1 mA	4	V_{OL}	–	–	0,3	V
I_O = 1,0 mA	11	V_{OL}	–	–	0,5	V
Output current "OFF"						
V_O = 11 V	11	I_O	–	–	10	μA
Control input ADRM						
Input voltage LOW	–	V_{IL}	–	–	0,8 x V_{DD}	V
Input voltage HIGH	–	V_{IH}	0,2 x V_{DD}	–	–	V
Input current (switched P- and N-channel pull-up/ pull-down)						
Pull-up active	4	I_{IL}	10	–	100	μA
stand-by voltage: 0 V	11	I_{IL}	30	–	300	μA
Pull-down active	4	I_{IH}	10	–	100	μA
stand-by voltage: V_{DD}	11	I_{IH}	30	–	300	μA

CHARACTERISTICS (continued)

V_{SS} = 0 V; T_{amb} = 25 °C; unless otherwise specified

parameter	V_{DD} (V)	symbol	min.	typ.	max.	unit
Data output REMO						
Output voltage HIGH	6	V_{OH}	3	–	–	V
$-I_{OH}$ = 40 mA	9	V_{OH}	6	–	–	V
Output voltage LOW	6	V_{OL}	–	–	0,2	V
I_{OL} = 0,3 mA	9	V_{OL}	–	–	0,1	V
Oscillator						
Input current OSCI at V_{DD}	6	I_I	0,8	–	2,7	μA
Output voltage HIGH $-I_{OL}$ = 0,1 mA	6	V_{OH}	–	–	V_{DD}–0,6	V
Output voltage LOW I_{OH} = 0,1 mA	6	V_{OL}	–	–	0,6	V

LOW VOLTAGE INFRARED REMOTE CONTROL TRANSMITTER (RC-5)

GENERAL DESCRIPTION

The SAA3006 is intended as a general purpose (RC-5) infrared remote control system for use where only low supply voltages are available. The device can generate 2048 different commands and utilizes a keyboard with a single-pole switch per key. The commands are arranged so that 32 systems can be addressed, each system containing 64 different commands.

The circuit response to legal (one key pressed at a time) and illegal (more than one key pressed at a time) keyboard operation is specified later in this publication (see KEY ACTIVITIES).

Features

- Low supply voltage requirements
- Very low current consumption
- For infrared transmission link
- Transmitter for 32 x 64 commands
- One transmitter controls 32 systems
- Transmission biphase technique
- Short transmission times; speed-up of system reaction time
- Single-pin oscillator input
- Input protection
- Test mode facility

QUICK REFERENCE DATA

Supply voltage range	V_{DD}	2 to 7	V
Input voltage range	V_I	0,5 to (V_{DD} + 0,5)	V*
Input current	$\pm I_I$	max. 10	mA
Output voltage range	V_O	−0,5 to (V_{DD} + 0,5)	V*
Output current	$\pm I_O$	max. 10	mA
Operating ambient temperature range	T_{amb}	−25 to +85	°C

* V_{DD} + 0,5 V not to exceed 9 V.

PACKAGE OUTLINE

28-lead DIL; plastic (SOT-117).

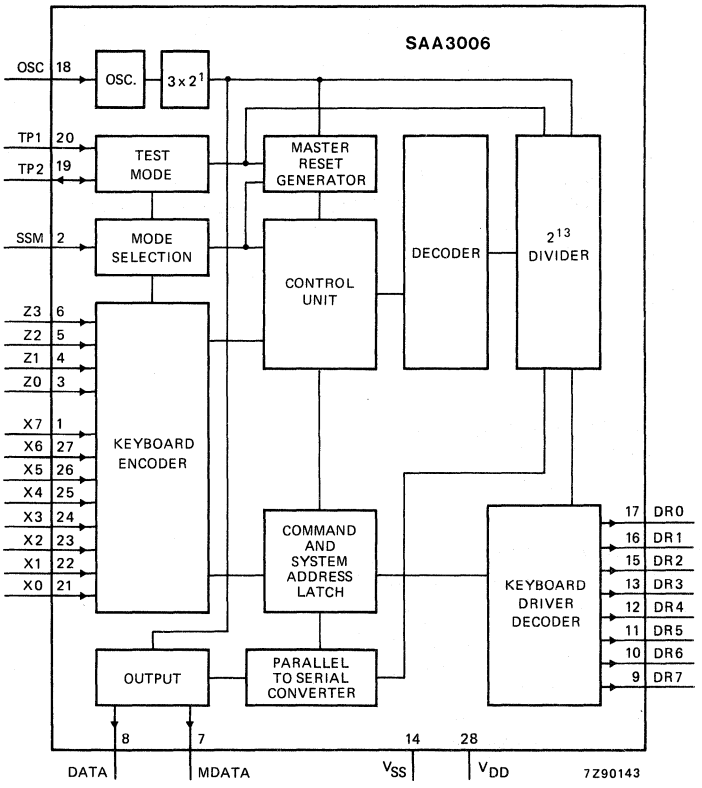


Fig. 1 Block diagram.

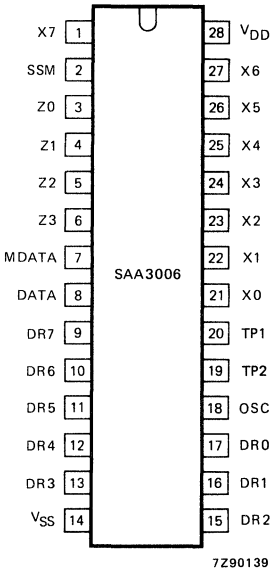
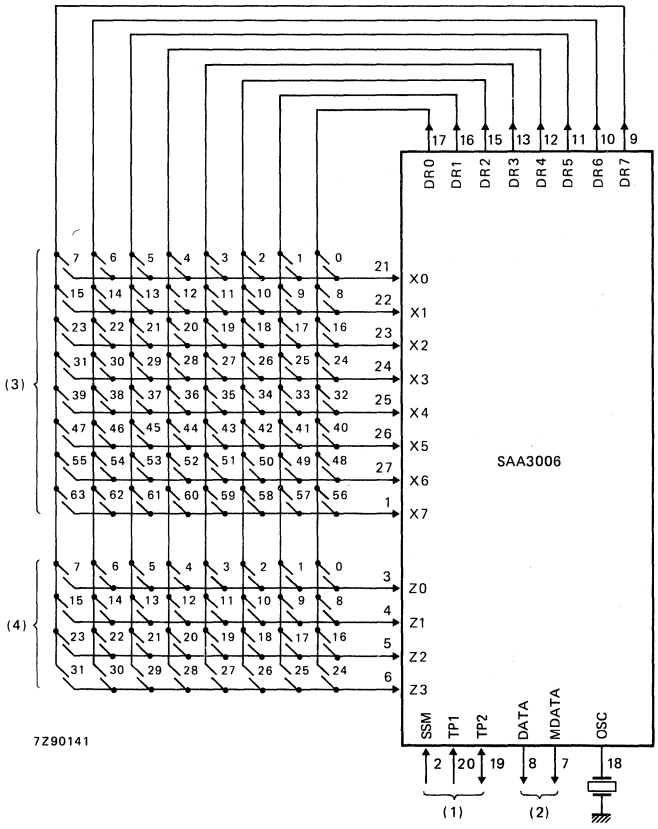


Fig. 2 Pinning diagram.

PINNING

14	V_{SS}	negative supply (ground)
28	V_{DD}	positive supply
21	X0	keyboard command inputs with P-channel pull-up transistors
22	X1	
23	X2	
24	X3	
25	X4	
26	X5	
27	X6	
1	X7	
3	Z0	keyboard system inputs with P-channel pull-up transistors
4	Z1	
5	Z2	
6	Z3	
2	SSM	system mode selection input
20	TP1	test input
19	TP2	test input/output
18	OSC	oscillator input
17	DR0	scan driver output with open drain N-channel transistors
16	DR1	
15	DR2	
13	DR3	
12	DR4	
11	DR5	
10	DR6	
9	DR7	
7	MDATA	remote signal outputs (3-state outputs)
8	DATA	

DEVELOPMENT DATA



(1) Control inputs for operating modes, test modes and reset.
(2) Remote signal outputs.
(3) Keyboard command code matrix 8 x 8.
(4) Keyboard system code matrix 4 x 8.

Fig. 3 Keyboard interconnection.

FUNCTIONAL DESCRIPTION

Combined system mode (SSM = LOW)

The X and Z-lines are active HIGH in the quiescent state. Legal key operation either in the X-DR or Z-DR matrix starts the debounce cycle. When the contact is made for two bit times without interruption, the oscillator-enable signal is latched and the key may be released. Interruption within the two bit times resets the internal action. At the end of the debounce time, the DR-outputs are switched off and two scan cycles are started, switching on the DR-outputs one by one. When a Z- or X-input senses a LOW level, a latch-enable signal is fed to the system address or command latches, depending on whether sensing was found in the Z- or X-input matrix. After latching a system address number, the device will generate the last command (i.e. all command bits '1') in the chosen system as long as the key is pressed. Latching of a command number causes the device to generate this command together with the system address number stored in the system address latch. Releasing the key will reset the internal action if no data is transmitted at that time. Once the transmission is started, the signal will be finished completely.

Single system mode (SSM = HIGH)

The X-lines are active HIGH in the quiescent state; the pull-up transistors of the Z-lines are switched off and the inputs are disabled. Only legal key operation in the X-DR matrix starts the debounce cycle. When the contact is made for two bit times without interruption, the oscillator-enable signal is latched and the key may be released. Interruption within the two bit times resets the internal action. At the end of the debounce time, the pull-up transistors in the X-lines are switched off, those in the Z-lines are switched on during the first scan cycle. The wired connection in the Z-matrix is then translated into a system address number and stored in the system address latch. At the end of the first scan cycle the pull-up transistors in the Z-lines are switched off and the inputs are disabled again, while the transistors in the X-lines are switched on. The second scan cycle produces the command number which, after latching, is transmitted together with the system address number.

DEVELOPMENT DATA

Inputs

The command inputs X0 to X7 carry a logical '1' in the quiescent state by means of an internal pull-up transistor. When SSM is LOW, the system inputs Z0 to Z3 also carry a logical '1' in the quiescent state by means of an internal pull-up transistor.

When SSM is HIGH, the transistors are switched off and no current flows via the wired connection in the Z-DR matrix.

Oscillator

The oscillator is formed by a ceramic resonator (catalogue number 2422 540 98021 or equivalent) feeding the single-pin input OSC. Direct connection is made for supply voltages in the range 2 to 5,25 V but it is necessary to fit a 10 kΩ resistor in series with the resonator when using supply voltages in the range 2,6 to 7 V.

Key-release detection

An extra control bit is added which will be complemented after key-release. In this way the decoder gets an indication that shows if the next code is to be considered as a new command. This is very important for multi-digit entry (e.g. by channel numbers or Teletext/Viewdata pages). The control bit will only be complemented after finishing at least one code transmission. The scan cycles are repeated before every code transmission, so that, even by 'take-over' of key operation during code transmission, the correct system and command numbers are generated.

FUNCTIONAL DESCRIPTION (continued)

Outputs

The output DATA carries the generated information according to the format given in Fig. 4 and Tables 2 and 3. The code is transmitted in biphase; definitions of logical '1' and '0' are given in Fig. 5.

The code consists of four parts:

- Start part formed by 2 bits (two times a logical '1');
- Control part formed by 1 bit;
- System part formed by 5 bits;
- Command part formed by 6 bits.

The output MDATA carries the same information as output DATA but is modulated on a carrier frequency of 1/12 of the oscillator frequency, so that each bit is presented as a burst of 32 pulses. To reduce power consumption, the carrier frequency has a 25% duty cycle.

In the quiescent state, both outputs are non-conducting (3-state outputs). The scan drivers DR0 to DR7 are of the open drain N-channel type and are conducting in the quiescent state of the circuit. After a legal key operation all the driver outputs go into the high ohmic state; a scanning procedure is then started so that the outputs are switched into the conducting state one after the other.

Reset action

The circuit will be reset immediately when a key release occurs during:

- debounce time;
- between two codes.

When a key release occurs during scanning of the matrix, a reset action will be accomplished if:

- the key is released while one of the driver outputs is in the low-ohmic '0' state;
- the key is released before detection of that key;
- there is no wired connection in the Z-DR matrix while SSM is HIGH.

Test pin

The test pins TP1 and TP2 are used for testing in conjunction with inputs Z2 and Z3 as shown in Table 1.

Table 1 Test functions

TP1	TP2	Z2	Z3	function
LOW	LOW	matrix input	matrix input	normal
LOW	HIGH	matrix input	matrix input	scan + output frequency six times faster than normal
HIGH	output $f_{OSC}{}^{6}$	LOW	LOW	reset
HIGH	output $f_{OSC}{}^{6}$	HIGH	HIGH	output frequency 3×2^{7} faster than normal

KEY ACTIVITIES

Every connection of one X-input and one DR-output is recognized as a legal keyboard operation and causes the device to generate the corresponding code.

Activating more than one X-input at a time is an illegal keyboard operation and no circuit action is taken (oscillator does not start).

When SSM is LOW, every connection of one Z-input and one DR-output is recognized as a legal keyboard operation and causes the device to generate the corresponding code.

Activating two or more Z-inputs, or Z-inputs and X-inputs, at one time is an illegal keyboard operation and no circuit action is taken.

When SSM is HIGH, a wired connection must be made between a Z-input and a DR-output. If no connection is made, the code is not generated.

When one X or Z-input is connected to more than one DR-output, the last scan signal is considered legal.

The maximum allowable value of the contact series resistance of the keyboard switches is 7 kΩ.

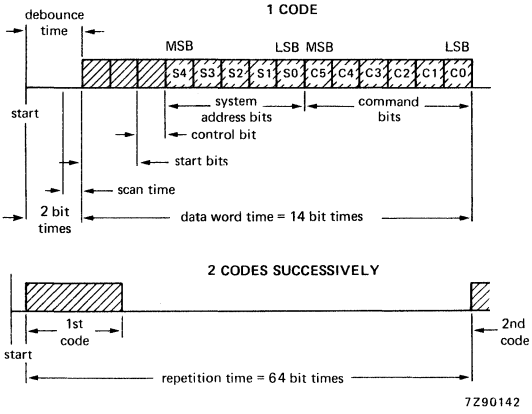


Fig. 4 DATA output format (RC-5).

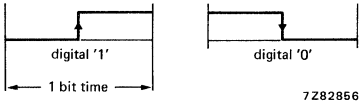


Fig. 5 Biphase transmission code; 1 bit time = $3 \times 2^8 \times T_{OSC}$ (typically 1,778 ms) where T_{OSC} is the oscillator period time.

Table 2 Command matrix X-DR

code no.	X-lines X.. 0	1	2	3	4	5	6	7	DR-lines DR.. 0	1	2	3	4	5	6	7	command bits C.. 5	4	3	2	1	0
0	●								●								0	0	0	0	0	0
1	●									●							0	0	0	0	0	1
2	●										●						0	0	0	0	1	0
3	●											●					0	0	0	0	1	1
4	●												●				0	0	0	1	0	0
5	●													●			0	0	0	1	0	1
6	●														●		0	0	0	1	1	0
7	●															●	0	0	0	1	1	1
8		●							●								0	0	1	0	0	0
9		●								●							0	0	1	0	0	1
10		●									●						0	0	1	0	1	0
11		●										●					0	0	1	0	1	1
12		●											●				0	0	1	1	0	0
13		●												●			0	0	1	1	0	1
14		●													●		0	0	1	1	1	0
15		●														●	0	0	1	1	1	1
16			●						●								0	1	0	0	0	0
17			●							●							0	1	0	0	0	1
18			●								●						0	1	0	0	1	0
19			●									●					0	1	0	0	1	1
20			●										●				0	1	0	1	0	0
21			●											●			0	1	0	1	0	1
22			●												●		0	1	0	1	1	0
23			●													●	0	1	0	1	1	1
24				●					●								0	1	1	0	0	0
25				●						●							0	1	1	0	0	1
26				●							●						0	1	1	0	1	0
27				●								●					0	1	1	0	1	1
28				●									●				0	1	1	1	0	0
29				●										●			0	1	1	1	0	1
30				●											●		0	1	1	1	1	0
31				●												●	0	1	1	1	1	1

DEVELOPMENT DATA

code no.	X-lines X.. 0	1	2	3	4	5	6	7	DR-lines DR.. 0	1	2	3	4	5	6	7	command bits C.. 5	4	3	2	1	0
32					●				●								1	0	0	0	0	0
33					●					●							1	0	0	0	0	1
34					●						●						1	0	0	0	1	0
35					●							●					1	0	0	0	1	1
36					●								●				1	0	0	1	0	0
37					●									●			1	0	0	1	0	1
38					●										●		1	0	0	1	1	0
39					●											●	1	0	0	1	1	1
40						●			●								1	0	1	0	0	0
41						●				●							1	0	1	0	0	1
42						●					●						1	0	1	0	1	0
43						●						●					1	0	1	0	1	1
44						●							●				1	0	1	1	0	0
45						●								●			1	0	1	1	0	1
46						●									●		1	0	1	1	1	0
47						●										●	1	0	1	1	1	1
48							●		●								1	1	0	0	0	0
49							●			●							1	1	0	0	0	1
50							●				●						1	1	0	0	1	0
51							●					●					1	1	0	0	1	1
52							●						●				1	1	0	1	0	0
53							●							●			1	1	0	1	0	1
54							●								●		1	1	0	1	1	0
55							●									●	1	1	0	1	1	1
56								●	●								1	1	1	0	0	0
57								●		●							1	1	1	0	0	1
58								●			●						1	1	1	0	1	0
59								●				●					1	1	1	0	1	1
60								●					●				1	1	1	1	0	0
61								●						●			1	1	1	1	0	1
62								●							●		1	1	1	1	1	0
63								●								●	1	1	1	1	1	1

Table 3 System matrix Z-DR

system no.	Z-lines Z..				DR-lines DR..								system bits S..				
	0	1	2	3	0	1	2	3	4	5	6	7	4	3	2	1	0
0	●				●								0	0	0	0	0
1	●					●							0	0	0	0	1
2	●						●						0	0	0	1	0
3	●							●					0	0	0	1	1
4	●								●				0	0	1	0	0
5	●									●			0	0	1	0	1
6	●										●		0	0	1	1	0
7	●											●	0	0	1	1	1
8		●			●								0	1	0	0	0
9		●				●							0	1	0	0	1
10		●					●						0	1	0	1	0
11		●						●					0	1	0	1	1
12		●							●				0	1	1	0	0
13		●								●			0	1	1	0	1
14		●									●		0	1	1	1	0
15		●										●	0	1	1	1	1
16			●		●								1	0	0	0	0
17			●			●							1	0	0	0	1
18			●				●						1	0	0	1	0
19			●					●					1	0	0	1	1
20			●						●				1	0	1	0	0
21			●							●			1	0	1	0	1
22			●								●		1	0	1	1	0
23			●									●	1	0	1	1	1
24				●	●								1	1	0	0	0
25				●		●							1	1	0	0	1
26				●			●						1	1	0	1	0
27				●				●					1	1	0	1	1
28				●					●				1	1	1	0	0
29				●						●			1	1	1	0	1
30				●							●		1	1	1	1	0
31				●								●	1	1	1	1	1

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range with respect to V_{SS}	V_{DD}	−0,5	to	8,5	V
Input voltage range	V_I	−0,5	to	$(V_{DD}+0,5)$	V*
Input current	$+I_I$	max.		10	mA
Output voltage range	V_O	−0,5	to	$(V_{DD}+0,5)$	V*
Output current	$+I_O$	max.		10	mA
Power dissipation output OSC	P_O	max.		50	mW
Power dissipation per output (all other outputs)	P_O	max.		100	mW
Total power dissipation per package	P_{tot}	max.		200	mW
Operating ambient temperature range	T_{amb}	−25	to	+85	°C
Storage temperature range	T_{stg}	−55	to	+150	°C

HANDLING

Inputs and outputs are protected against electrostatic charge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see "Handling MOS Devices").

DEVELOPMENT DATA

* V_{DD} + 0,5 V not to exceed 9 V.

CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = −25 to 85 °C unless otherwise specified

parameter	V_{DD} (V)	symbol	min.	typ.	max.	unit
Supply voltage	–	V_{DD}	2	–	7	V
Supply current at I_O = 0 mA for all outputs; X0 to X7 and Z3 at V_{DD}; all other inputs at V_{DD} or V_{SS}; excluding leakage current from open drain N-channel outputs; T_{amb} = 25 °C	7	I_{DD}	–	–	10	μA
Inputs						
Keyboard inputs X and Z with P-channel pull-up transistors						
Input current (each input) at V_I = 0 V; TP = SSM = LOW	2 to 7	$-I_I$	10	–	600	μA
Input voltage HIGH	2 to 7	V_{IH}	0,7 x V_{DD}	–	V_{DD}	V
Input voltage LOW	2 to 7	V_{IL}	0	–	0,3 x V_{DD}	V
Input leakage current at T_{amb} = 25 °C; TP = HIGH; V_I = 7 V		I_{IR}	–	–	1	μA
V_I = 0 V		$-I_{IR}$	–	–	1	μA
SSM, TP1 and TP2						
Input voltage HIGH	2 to 7	V_{IH}	0,7 x V_{DD}	–	V_{DD}	V
Input voltage LOW	2 to 7	V_{IL}	0	–	0,3 x V_{DD}	V
Input leakage current at T_{amb} = 25 °C; V_I = 7 V		I_{IR}	–	–	1	μA
V_I = 0 V		$-I_{IR}$	–	–	1	μA
OSC						
Input leakage current at T_{amb} = 25 °C; V_I = 0 V; TP1 = HIGH; Z2 = Z3 = LOW	2 to 7	$-I_I$	–	–	2	μA

DEVELOPMENT DATA

parameter	V_{DD} (V)	symbol	min.	typ.	max.	unit
Outputs						
DATA and MDATA						
Output voltage HIGH at $-I_{OH}$ = 0,4 mA	2 to 7	V_{OH}	V_{DD} −0,3	–	–	V
Output voltage LOW at I_{OL} = 0,6 mA	2 to 7	V_{OL}	–	–	0,3	V
Output leakage current at:						
V_O = 7 V		I_{OR}	–	–	10	μA
V_O = 0 V		$-I_{OR}$	–	–	20	μA
T_{amb} = 25 °C;						
V_O = 7 V		I_{OR}	–	–	1	μA
V_O = 0 V		$-I_{OR}$	–	–	2	μA
DR0 to DR7, TP2						
Output voltage LOW at I_{OL} = 0,3 mA	2 to 7	V_{OL}	–	–	0,3	V
Output leakage current at V_O = 7 V	7	I_{OR}	–	–	10	μA
at V_O = 7 V						
T_{amb} = 25 °C		I_{OR}	–	–	1	μA
OSC						
Oscillator current at OSC = V_{DD}	7	I_{OSC}	4,5	–	30	μA
Oscillator						
Maximum oscillator frequency at C_L = 40 pF (Figs 6 and 7)	2	f_{OSC}	–	–	450	kHz
Free-running oscillator frequency at T_{amb} = 25 °C	2	f_{OSC}	10	–	120	kHz

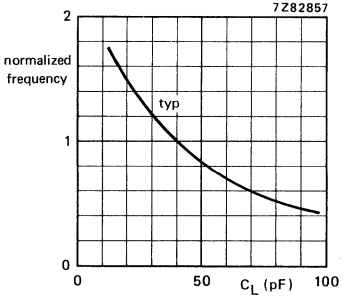


Fig. 6 Typical normalized input frequency as a function of the load (keyboard) capacitance.

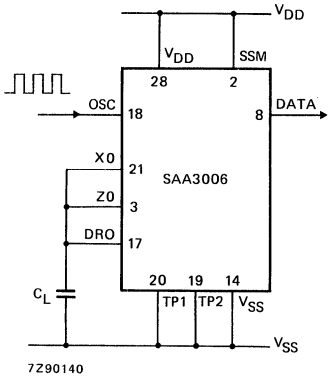


Fig. 7 Test circuit for measurement of maximum oscillator frequency.

INFRARED REMOTE CONTROL TRANSMITTER (RC-5)

GENERAL DESCRIPTION

The SAA3027 is intended for a general purpose (RC-5) infrared remote control system. The device can generate 2048 different commands and utilizes a keyboard with a single-pole switch per key. The commands are arranged so that 32 systems can be addressed, each system containing 64 different commands.

The circuit response to legal (one key pressed at a time) and illegal (more than one key pressed at a time) keyboard operation is specified later in this publication (see KEY ACTIVITIES).

Features

- Transmitter for 32 x 64 commands
- One transmitter controls 32 systems
- Very low current consumption
- For infrared transmission link
- Transmission by biphase technique
- Short transmission times; speed-up of system reaction time
- LC oscillator; no crystal required
- Input protection
- Test mode facility

QUICK REFERENCE DATA

Supply voltage range	V_{DD}	4,75 to 12,6	V
Input voltage range	V_I	−0,5 to (V_{DD}+0,5)	V*
Input current	$\pm I_I$	max. 10	mA
Output voltage range	V_O	−0,5 to (V_{DD}+0,5)	V*
Output current	$\pm I_O$	max. 10	mA
Operating ambient temperature range	T_{amb}	−25 to +85	°C

* V_{DD} + 0,5 V not to exceed 15 V.

PACKAGE OUTLINE

28-lead DIL; plastic (SOT-117).

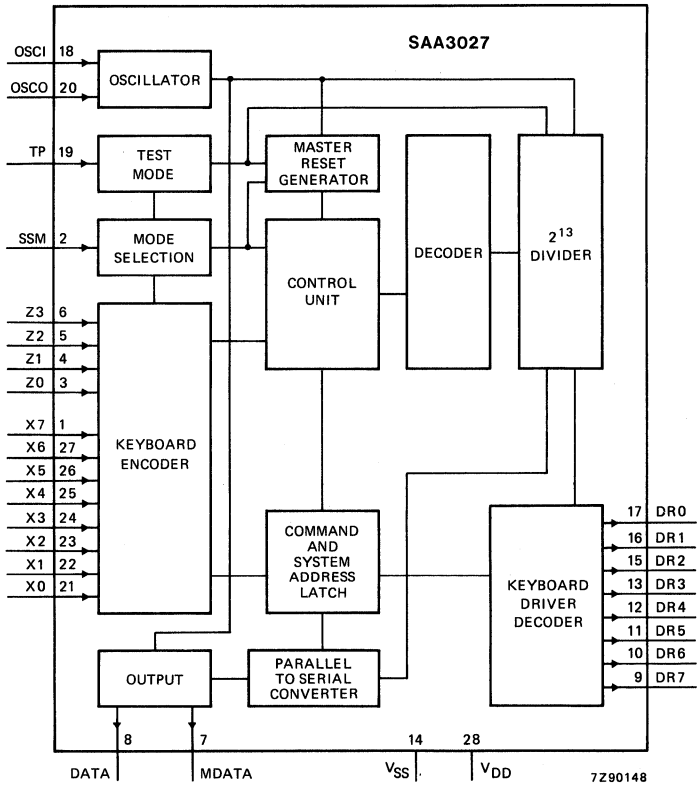


Fig. 1 Block diagram.

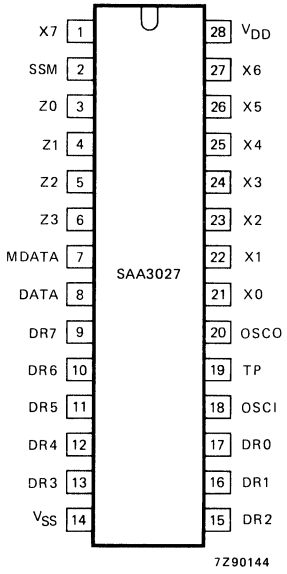
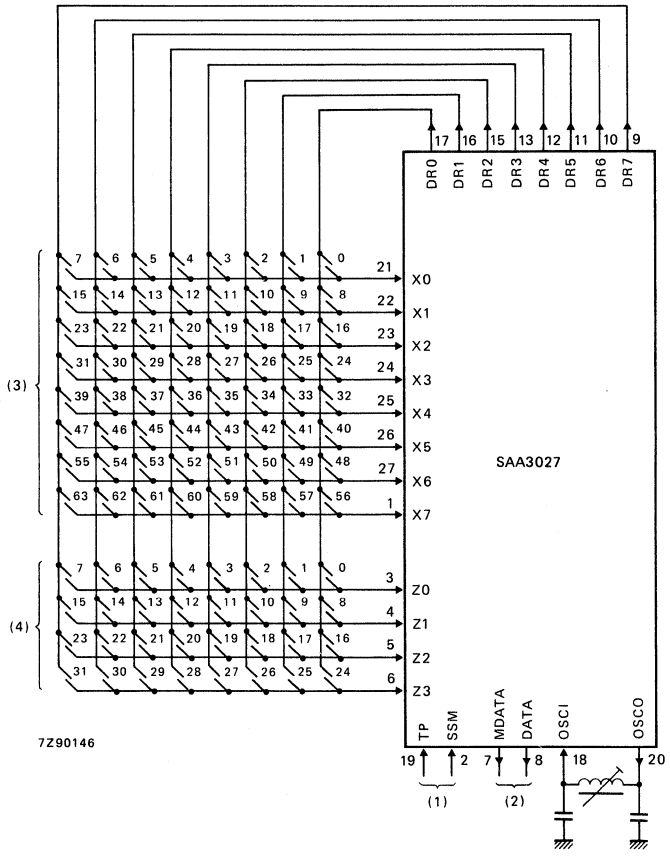


Fig. 2 Pinning diagram.

PINNING

14	V_{SS}	negative supply (ground)
28	V_{DD}	positive supply
21	X0	keyboard command inputs with P-channel pull-up transistors
22	X1	
23	X2	
24	X3	
25	X4	
26	X5	
27	X6	
1	X7	
3	Z0	keyboard system inputs with P-channel pull-up transistors
4	Z1	
5	Z2	
6	Z3	
2	SSM	system mode selection input
19	TP	test pin
18	OSC1	oscillator input
20	OSC0	oscillator output
17	DR0	scan driver outputs with open drain N-channel transistors
16	DR1	
15	DR2	
13	DR3	
12	DR4	
11	DR5	
10	DR6	
9	DR7	
7	MDATA	remote signal outputs (3-state outputs)
8	DATA	

DEVELOPMENT DATA



(1) Programming inputs for operating modes, test mode and reset.
(2) Remote signal outputs.
(3) Keyboard command code matrix 8 x 8.
(4) Keyboard system code matrix 4 x 8.

Fig. 3 Keyboard interconnection.

FUNCTIONAL DECRIPTION

Combined system mode (SSM = LOW)

The X and Z-lines are active HIGH in the quiescent state. Legal key operation either in the X-DR or Z-DR matrix starts the debounce cycle. When the contact is made for two bit times without interruption, the oscillator-enable signal is latched and the key may be released. Interruption within the two bit times resets the internal action. At the end of the debounce time, the DR-outputs are switched off and two scan cycles are started, switching on the DR-outputs one by one. When a Z or X-input senses a LOW level, a latch-enable signal is fed to the system address or command latches, depending on whether sensing was found in the Z or X-input matrix. After latching a system address number, the device will generate the last command (i.e. all command bits '1') in the chosen system as long as the key is pressed. Latching of a command number causes the device to generate this command together with the system address number stored in the system address latch. Releasing the key will reset the internal action if no data is transmitted at that time. Once the transmission is started, the signal will be finished completely.

Single system mode (SSM = HIGH)

The X-lines are active HIGH in the quiescent state; the pull-up transistors of the Z-lines are switched off and the inputs are disabled. Only legal key operation in the X-DR matrix starts the debounce cycle. When the contact is made for two bit times without interruption, the oscillator-enable signal is latched and the key may be released. Interruption within the two bit times resets the internal action. At the end of the debounce time, the pull-up transistors in the X-lines are switched off, those in the Z-lines are switched on during the first scan cycle. The wired connection in the Z-matrix is then translated into a system address number and stored in the system address latch. At the end of the first scan cycle the pull-up transistors in the Z-lines are switched off and the inputs are disabled again, while the transistors in the X-lines are switched on. The second scan cycle produces the command number which, after latching, is transmitted together with the system address number.

DEVELOPMENT DATA

Inputs

The command inputs X0 to X7 carry a logical '1' in the quiescent state by means of an internal pull-up transistor. When SSM is LOW, the system inputs Z0 to Z3 also carry a logical '1' in the quiescent state by means of an internal pull-up transistor.

When SSM is HIGH, the transistors are switched off and no current flows via the wired connection in the Z-DR matrix.

Oscillator

OSCI and OSCO are the input/output respectively of a two-pin oscillator. The oscillator is formed externally by one inductor and two capacitors and operates at 72 kHz (typical).

Key-release detection

An extra control bit is added which will be complemented after key-release. In this way the decoder gets an indication that shows if the next code is to be considered as a new command. This is very important for multi-digit entry (e.g. by channel numbers or Teletext/Viewdata pages). The control bit will only be complemented after finishing at least one code transmission. The scan cycles are repeated before every code transmission, so that, even by 'take-over' of key operation during code transmission, the correct system and command numbers are generated.

FUNCTIONAL DESCRIPTION (continued)

Outputs

The output DATA carries the generated information according to the format given in Fig. 4 and Tables 1 and 2. The code is transmitted in biphase; definitions of logical '1' and '0' are given in Fig. 5.

The code consists of four parts:

- Start part formed by 2 bits (two times a logical '1');
- Control part formed by 1 bit;
- System part formed by 5 bits;
- Command part formed by 6 bits.

The output MDATA carries the same information as output DATA but is modulated on a carrier frequency of half the oscillator frequency, so that each bit is presented as a burst of 32 oscillator periods. To reduce power consumption, the carrier frequency has a 25% duty cycle.

In the quiescent state, both outputs are non-conducting (3-state outputs). The scan drivers DR0 to DR7 are of the open drain N-channel type and are conducting in the quiescent state of the circuit. After a legal key operation, a scanning procedure is started so that they are switched into the conducting state one after the other.

Reset action

The circuit will be reset immediately when a key release occurs during:

- debounce time;
- between two codes.

When a key release occurs during scanning of the matrix, a reset action will be accomplished if:

- the key is released while one of the driver outputs is in the low-ohmic '0' state;
- the key is released before detection of that key;
- there is no wired connection in the Z-DR matrix while SSM is HIGH.

Test pin

The test pin TP is an input which can be used for testing purposes.

When LOW, the circuit operates normally.

When HIGH, all pull-up transistors are switched off, the control bit is set to zero and the output data is 2^6 times faster than normal.

When Z2 = Z3 = LOW, the counter will be reset to zero.

KEY ACTIVITIES

Every connection of one X-input and one DR-output is recognized as a legal keyboard operation and causes the device to generate the corresponding code.

Activating more than one X-input at a time is an illegal keyboard operation and no circuit action is taken (oscillator does not start).

When SSM is LOW, every connection of one Z-input and one DR-output is recognized as a legal keyboard operation and causes the device to generate the corresponding code.

Activating two or more Z-inputs, or Z-inputs and X-inputs, at one time is an illegal keyboard operation and no circuit action is taken.

When SSM is HIGH, a wired connection must be made between a Z-input and a DR-output. If no connection is made, the code is not generated.

When one X or Z-input is connected to more than one DR-output, the last scan signal is considered legal.

The maximum allowable value of the contact series resistance of the keyboard switches is 10 kΩ.

Z2 or Z3 must be connected to V_{DD} to avoid unwanted supply current.

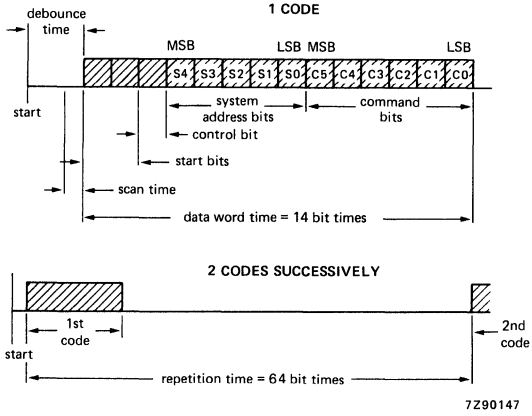


Fig. 4 DATA output format (RC-5).

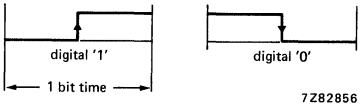


Fig. 5 Biphase transmission code; 1 bit time = $2^7 \times T_{OSC}$ = 1,778 ms (typical), where T_{OSC} is the oscillator period time.

Table 1 Command matrix X-DR

code no.	X-lines X..								DR-lines DR..								command bits C..					
	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	5	4	3	2	1	0
0	●								●								0	0	0	0	0	0
1	●									●							0	0	0	0	0	1
2	●										●						0	0	0	0	1	0
3	●											●					0	0	0	0	1	1
4	●												●				0	0	0	1	0	0
5	●													●			0	0	0	1	0	1
6	●														●		0	0	0	1	1	0
7	●															●	0	0	0	1	1	1
8		●							●								0	0	1	0	0	0
9		●								●							0	0	1	0	0	1
10		●									●						0	0	1	0	1	0
11		●										●					0	0	1	0	1	1
12		●											●				0	0	1	1	0	0
13		●												●			0	0	1	1	0	1
14		●													●		0	0	1	1	1	0
15		●														●	0	0	1	1	1	1
16			●						●								0	1	0	0	0	0
17			●							●							0	1	0	0	0	1
18			●								●						0	1	0	0	1	0
19			●									●					0	1	0	0	1	1
20			●										●				0	1	0	1	0	0
21			●											●			0	1	0	1	0	1
22			●												●		0	1	0	1	1	0
23			●													●	0	1	0	1	1	1
24				●					●								0	1	1	0	0	0
25				●						●							0	1	1	0	0	1
26				●							●						0	1	1	0	1	0
27				●								●					0	1	1	0	1	1
28				●									●				0	1	1	1	0	0
29				●										●			0	1	1	1	0	1
30				●											●		0	1	1	1	1	0
31				●												●	0	1	1	1	1	1

DEVELOPMENT DATA

code no.	X-lines X..								DR-lines DR..								command bits C..					
	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	5	4	3	2	1	0
32					●				●								1	0	0	0	0	0
33					●					●							1	0	0	0	0	1
34					●						●						1	0	0	0	1	0
35					●							●					1	0	0	0	1	1
36					●								●				1	0	0	1	0	0
37					●									●			1	0	0	1	0	1
38					●										●		1	0	0	1	1	0
39					●											●	1	0	0	1	1	1
40						●			●								1	0	1	0	0	0
41						●				●							1	0	1	0	0	1
42						●					●						1	0	1	0	1	0
43						●						●					1	0	1	0	1	1
44						●							●				1	0	1	1	0	0
45						●								●			1	0	1	1	0	1
46						●									●		1	0	1	1	1	0
47						●										●	1	0	1	1	1	1
48							●		●								1	1	0	0	0	0
49							●			●							1	1	0	0	0	1
50							●				●						1	1	0	0	1	0
51							●					●					1	1	0	0	1	1
52							●						●				1	1	0	1	0	0
53							●							●			1	1	0	1	0	1
54							●								●		1	1	0	1	1	0
55							●									●	1	1	0	1	1	1
56								●	●								1	1	1	0	0	0
57								●		●							1	1	1	0	0	1
58								●			●						1	1	1	0	1	0
59								●				●					1	1	1	0	1	1
60								●					●				1	1	1	1	0	0
61								●						●			1	1	1	1	0	1
62								●							●		1	1	1	1	1	0
63								●								●	1	1	1	1	1	1

Table 2 System matrix Z-DR

system no.	Z-lines Z..				DR-lines DR..								system bits S..				
	0	1	2	3	0	1	2	3	4	5	6	7	4	3	2	1	0
0	●				●								0	0	0	0	0
1	●					●							0	0	0	0	1
2	●						●						0	0	0	1	0
3	●							●					0	0	0	1	1
4	●								●				0	0	1	0	0
5	●									●			0	0	1	0	1
6	●										●		0	0	1	1	0
7	●											●	0	0	1	1	1
8		●			●								0	1	0	0	0
9		●				●							0	1	0	0	1
10		●					●						0	1	0	1	0
11		●						●					0	1	0	1	1
12		●							●				0	1	1	0	0
13		●								●			0	1	1	0	1
14		●									●		0	1	1	1	0
15		●										●	0	1	1	1	1
16			●		●								1	0	0	0	0
17			●			●							1	0	0	0	1
18			●				●						1	0	0	1	0
19			●					●					1	0	0	1	1
20			●						●				1	0	1	0	0
21			●							●			1	0	1	0	1
22			●								●		1	0	1	1	0
23			●									●	1	0	1	1	1
24				●	●								1	1	0	0	0
25				●		●							1	1	0	0	1
26				●			●						1	1	0	1	0
27				●				●					1	1	0	1	1
28				●					●				1	1	1	0	0
29				●						●			1	1	1	0	1
30				●							●		1	1	1	1	0
31				●								●	1	1	1	1	1

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range with respect to V_{SS}	V_{DD}	−0,5 to +15	V
Input voltage range	V_I	−0,5 to (V_{DD} + 0,5)	V*
Input current	$\pm I_I$	max. 10	mA
Output voltage range	V_O	−0,5 to (V_{DD} + 0,5)	V*
Output current	$\pm I_O$	max. 10	mA
Power dissipation output OSCO	P_O	max. 50	mW
Power dissipation per output (all other outputs)	P_O	max. 100	mW
Total power dissipation per package	P_{tot}	max. 200	mW
Operating ambient temperature range	T_{amb}	−25 to +85	°C
Storage temperature range	T_{stg}	−55 to +150	°C

HANDLING

Inputs and outputs are protected against electrostatic charge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see "Handling MOS Devices").

DEVELOPMENT DATA

* V_{DD} + 0,5 V not to exceed 15 V.

CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = −25 to 85 °C unless otherwise specified

parameter	V_{DD} (V)	symbol	min.	typ.	max.	unit
Supply voltage	–	V_{DD}	4,75	–	12,6	V
Supply current at I_O = 0 mA for all outputs; X0 to X7 and Z3 at V_{DD}; all other inputs at V_{DD} or V_{SS}; excluding leakage current from open drain N-channel outputs; T_{amb} = 25 °C	12,6	I_{DD}	–	–	10	μA
Inputs						
Keyboard inputs X and Z with P-channel pull-up transistors						
Input current (each input) at V_I = 0 V; TP = SSM = LOW	4,75 to 12,6	$-I_I$	10	–	300	μA
Input voltage HIGH	4,75 to 12,6	V_{IH}	0,7 x V_{DD}	–	V_{DD}	V
Input voltage LOW	4,75 to 12,6	V_{IL}	0	–	0,3 x V_{DD}	V
Input leakage current at T_{amb} = 25 °C; TP = HIGH;						
V_I = 12,6 V	12,6	I_{IR}	–	–	1	μA
V_I = 0 V	12,6	$-I_{IR}$	–	–	1	μA
SSM, TP and OSCI inputs						
Input voltage HIGH	4,75 to 12,6	V_{IH}	0,7 x V_{DD}	–	V_{DD}	V
Input voltage LOW	4,75 to 12,6	V_{IL}	0	–	0,3 x V_{DD}	V
Input leakage current at T_{amb} = 25 °C;						
V_I = 12,6 V	12,6	I_{IR}	–	–	1	μA
V_I = 0 V	12,6	$-I_{IR}$	–	–	1	μA
Outputs						
DATA, MDATA outputs						
Output voltage HIGH at $-I_{OH}$ = 0,8 mA	4,75 to 12,6	V_{OH}	$V_{DD}-0,6$	–	–	V
Output voltage LOW at I_{OL} = 0,8 mA	4,75 to 12,6	V_{OL}	–	–	0,4	V
Output leakage current at:						
V_O = 12,6 V	12,6	I_{OR}	–	–	10	μA
V_O = 0 V	12,6	$-I_{OR}$	–	–	20	μA
T_{amb} = 25 °C;						
V_O = 12,6 V	12,6	I_{OR}	–	–	1	μA
V_O = 0 V	12,6	$-I_{OR}$	–	–	2	μA

parameter	V_{DD} (V)	symbol	min.	typ.	max.	unit
DR0 to DR7 outputs						
Output voltage LOW; at I_{OL} = 0,35 mA	4,75 to 12,6	V_{OL}	–	–	0,4	V
Output leakage current at V_O = 12,6 V	12,6	I_{OR}	–	–	10	μA
at V_O = 12,6 V; T_{amb} = 25 °C	12,6	I_{OR}	–	–	1	μA
OSCO output						
Output voltage HIGH at $-I_{OH}$ = 0,2 mA; OSCI = V_{SS}	4,75 to 12,6	V_{OH}	$V_{DD}-0,6$	–	–	V
Output voltage LOW at $-I_{OL}$ = 0,45 mA; OSCI = V_{DD}	4,75 to 12,6	V_{OL}	–	–	0,5	V
Oscillator						
Maximum oscillator frequency at C_L = 40 pF (Figs 6 and 7)	4,75	f_{OSCI}	75	72	–	kHz
	6	f_{OSCI}	120	72	–	kHz
	12,6	f_{OSCI}	300	72	–	kHz

DEVELOPMENT DATA

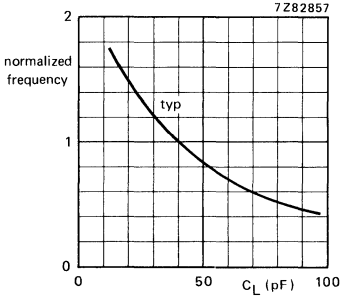


Fig. 6 Typical normalized input frequency as a function of the load (keyboard) capacitance.

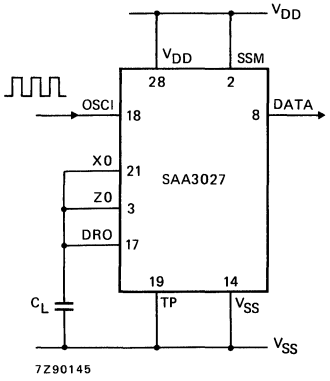


Fig. 7 Test circuit for measurement of maximum oscillator frequency.

INFRARED REMOTE CONTROL TRANSCODER (RC-5)

GENERAL DESCRIPTION

The SAA3028 is intended for use in general purpose (RC-5) remote control systems. The main function of this integrated circuit is to convert RC-5 biphase coded signals into equivalent binary values. Two input circuits are available: one for RC-5 coded signals only; the other is selectable to accept (1) RC-5 coded signals only, or (2) RC-5 (extended) coded signals only. The input used is that at which an active code is first detected. Coded signals not in RC-5/RC-5(ext) format are rejected. Data input and output is by serial transfer, the output interface being compatible for I^2C bus operation.

Features

- Converts RC-5 or RC-5(ext) biphase coded signals into binary equivalents
- Two data inputs, one fixed (RC-5), one selectable (RC-5/RC-5(ext))
- Rejects all codes not in RC-5/RC-5(ext) format
- I^2C output interface capability
- Power-off facility
- Master/slave addressable for multi-transmitter/receiver applications in RC-5(ext) mode
- Power-on-reset for defined start-up

QUICK REFERENCE DATA

Supply voltage range	V_{DD}	4,5 to	5,5 V
Supply current (quiescent) at V_{DD} = 5,5 V; T_{amb} = 25 °C	I_{DD}	max.	200 μA
Operating ambient temperature range	T_{amb}	−25 to	+85 °C

PACKAGE OUTLINE

16-lead DIL; plastic (SOT-38Z).

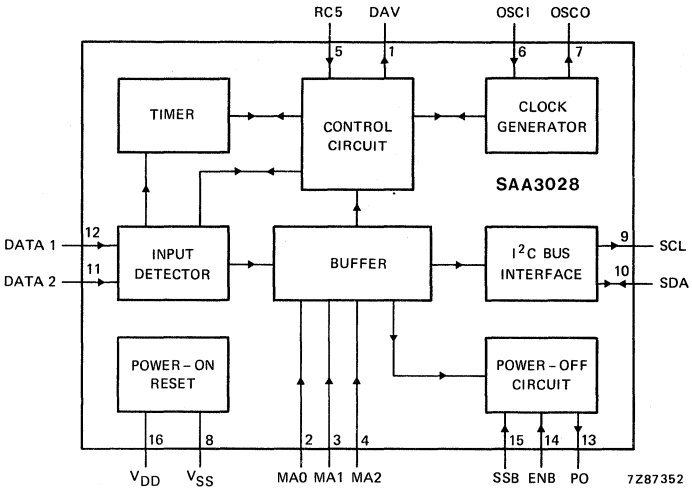


Fig. 1 Block diagram.

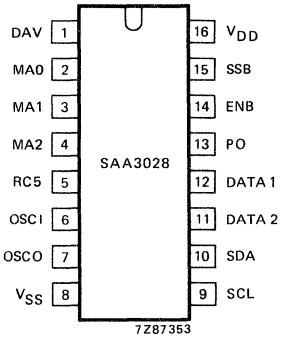


Fig. 2 Pinning diagram.

PINNING

1	DAV	data valid output with open drain N-channel transistor
2	MA0	master address inputs
3	MA1	master address inputs
4	MA2	master address inputs
5	RC5	data 2 input select
6	OSCI	oscillator input
7	OSCO	oscillator output
8	V_{SS}	negative supply (ground)
9	SCL	serial clock line (I^2C bus)
10	SDA	serial data line (I^2C bus)
11	DATA 2	data 2 input
12	DATA 1	data 1 input
13	PO	power-off signal output with open drain N-channel transistor
14	ENB	enable input
15	SSB	set standby input
16	V_{DD}	positive supply (+5 V)

FUNCTIONAL DESCRIPTION

Input function

The two data inputs are accepted into the buffer as follows:

- DATA 1. Only biphase coded signals which conform to the RC-5 format are accepted at this input.
- DATA 2. This input performs according to the logic state of the select input RC5. When RC5 = HIGH, DATA 2 input will accept only RC-5 coded signals. When RC5 = LOW, DATA 2 input will accept only RC-5(ext) coded signals.

The input detector selects the input, DATA 1 or DATA 2, in which a HIGH to LOW transition is first detected. The selected input is then accepted by the buffer for code conversion. All signals received that are not in the RC-5 or RC-5(ext) format are rejected.

Formats of RC-5 and RC-5(ext) biphase coded signals are shown in Figs 3 and 4 respectively; the codes commence from the left of the formats shown. The bit-times of the biphase codes are defined in Fig. 5.

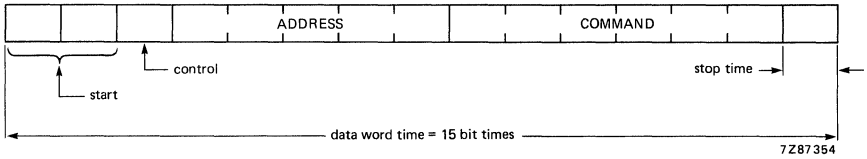


Fig. 3 RC-5 code format: the first start bit is used only for detection and input gain-setting; stop time = 1,5 bit-times (nominal).

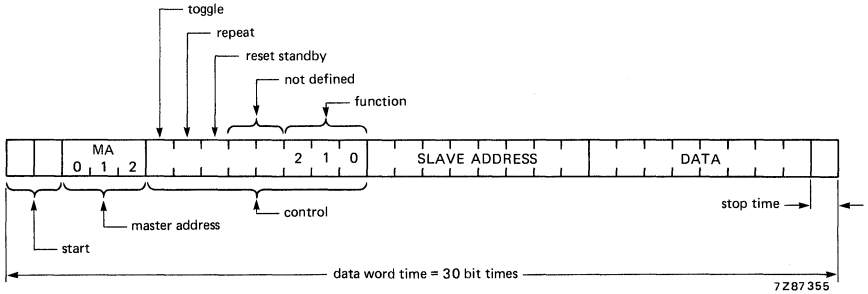


Fig. 4 RC-5(extended) code format: the first start bit is used only for detection and input gain-setting; stop time = 1,5 bit-times (nominal).

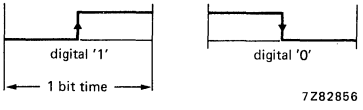


Fig. 5 Biphase code definition: RC-5 bit-time = $2^7 \times T_{OSC}$ = 1,778 ms (typical); RC-5(ext) bit-time = $2^6 \times T_{OSC}$ = 0,89 ms (typical), where T_{OSC} = the oscillator period time.

FUNCTIONAL DESCRIPTION (continued)

More information is added to the input data held in the buffer in order to make it suitable for transmission via the I^2C interface. The information now held in the buffer is as follows:

RC-5 buffer contents		RC-5(ext) buffer contents	
• data valid indicator	1 bit	• data valid indicator	1 bit
• format indicator	1 bit	• format indicator	1 bit
• input indicator	1 bit	• input indicator	1 bit
• control	1 bit	• master address	3 bits
• address data	5 bits	• control	8 bits
• command data	6 bits	• slave address	8 bits
		• data	8 bits

The information assembled in the buffer is subjected to the following controls before being made available at the I^2C interface:

ENB = HIGH — Enables the set standby input SSB.

SSB = LOW — Causes power-off output PO to go HIGH.

PO = HIGH — This occurs when the set standby input SSB = LOW and allows the existing values in the buffer to be overwritten by the new binary equivalent values. After ENB = LOW, SSB is don't care.

PO = LOW — This occurs according to the type of code being processed, as follows:

RC-5. When the binary equivalent value is transferred to the buffer.

RC-5(ext). When the reset standby bit is active and the master address bits are equal in value to the MA0, MA1, MA2 inputs.

At power-on, PO is reset to LOW.

DAV = HIGH — This occurs when the buffer contents are valid. If the buffer is not empty, or an output transfer is taking place, then the new binary values are discarded.

Output function

The data is assembled in the buffer in the format shown in Fig. 6 for RC-5 binary equivalent values, or in the format shown in Fig. 7 for RC-5(ext) binary equivalent values. The data is output serially, starting from the left of the formats shown in Figs 6 and 7.

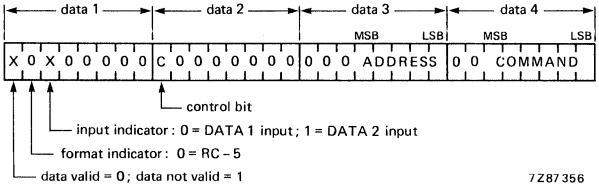


Fig. 6 RC-5 binary equivalent value format.

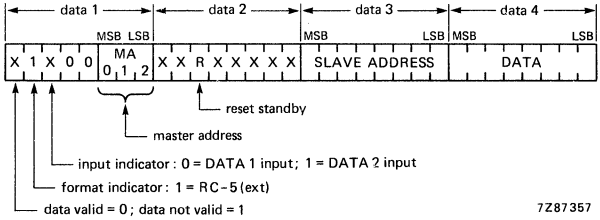


Fig. 7 RC-5(ext) binary equivalent value format.

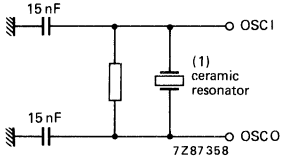
DEVELOPMENT DATA

The output signal DAV, derived in the buffer from the data valid bit, is provided to facilitate use of the transcoder on an interrupt basis. This output is reset to LOW during power-on.

The I^2C interface allows transmission on a bidirectional, two-wire I^2C bus. The interface is a slave transmitter with a built-in slave address, having a fixed 7-bit binary value of 0100110. Serial output of the slave address onto the I^2C bus starts from the left-hand bit.

Oscillator

The oscillator can comprise a ceramic resonator circuit as shown in Fig. 8. The typical frequency of oscillation is 455 kHz.



(1) Catalogue number of ceramic resonator: 2422 540 98008.

Fig. 8 Oscillator circuit.

FUNCTIONAL DESCRIPTION (continued)

I^2C bus transmission

Formats for I^2C transmission in low and high speed modes are shown respectively in Figs 9 and 10.

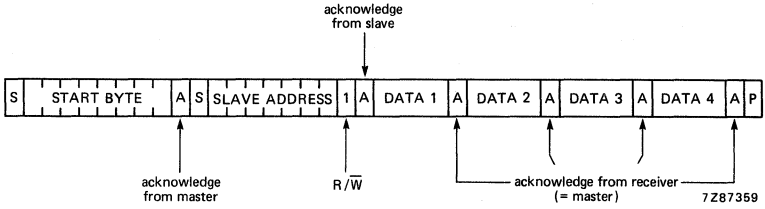


Fig. 9 Format for transmission in I^2C low speed mode.

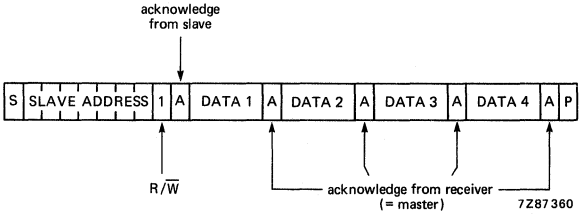


Fig. 10 Format for transmission in I^2C high speed mode.

Note to Figures 9 and 10

When R/$\overline{W}$ bit = 0; the slave generates a NACK (negative acknowledge), leaves the data line HIGH and waits for a stop (P) condition.

When the receiver generates a NACK; the slave leaves the data line HIGH and waits for P (the slave acting as if all data has been transmitted).

When all data has been transmitted, the data line remains HIGH and the slave waits for P.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range with respect to V_{SS}	V_{DD}	−0,5 to	+15	V
Input voltage range	V_I	−0,5 to	(V_{DD}+0,5)	V*
Input current	$\pm I_I$	max.	10	mA
Output voltage range	V_O	−0,5 to	(V_{DD}+0,5)	V*
Output current	$\pm I_O$	max.	10	mA
Power dissipation output OSCO	P_O	max.	50	mW
Power dissipation per output (all other outputs)	P_O	max.	100	mW
Total power dissipation per package	P_{tot}	max.	200	mW
Operating ambient temperature range	T_{amb}	−25 to	+85	°C
Storage temperature range	T_{stg}	−55 to	+150	°C

HANDLING

Inputs and outputs are protected against electrostatic charge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see "Handling MOS Devices").

DEVELOPMENT DATA

Purchase of Philips I²C components conveys a licence under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

* V_{DD} + 0,5 V not to exceed 15 V.

CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = −25 to 85 °C unless otherwise specified

parameter	V_{DD} (V)	symbol	min.	typ.	max.	unit
Supply voltage	–	V_{DD}	4,5	–	5,5	V
Supply current; quiescent at T_{amb} = 25 °C	5,5	I_{DD}	–	–	200	μA
Inputs						
MA0, MA1, MA2, DATA 1, DATA 2, RC5, SCL, ENB, SSB, OSCI						
Input voltage HIGH	4,5 to 5,5	V_{IH}	0,7 x V_{DD}	–	V_{DD}	V
Input voltage LOW	4,5 to 5,5	V_{IL}	0	–	0,3 x V_{DD}	V
Input leakage current at V_I = 5,5 V; T_{amb} = 25 °C	5,5	I_I	–	–	1	μA
Input leakage current at V_I = 0 V; T_{amb} = 25 °C;	5,5	$-I_I$	–	–	1	μA
Outputs						
DAV, PO						
Output voltage LOW at I_{OL} = 1,6 mA	4,5 to 5,5	V_{OL}	–	–	0,4	V
Output leakage current at V_O = 5,5 V; T_{amb} = 25 °C	5,5	I_{OR}	–	–	1	μA
OSCO						
Output voltage HIGH at $-I_{OH}$ = 0,2 mA	4,5 to 5,5	V_{OH}	V_{DD} − 0,5	–	–	V
Output voltage LOW at I_{OL} = 0,3 mA	4,5 to 5,5	V_{OL}	–	–	0,4	V
Output leakage current at T_{amb} = 25 °C; V_O = 5,5 V	5,5	I_{OR}	–	–	1	μA
V_O = 0 V	5,5	I_{OR}	–	–	1	μA
SDO						
Output voltage LOW at I_{OL} = 2 mA	4,5 to 5,5	V_{OL}	–	–	0,4	V
Output leakage current at V_O = 5,5 V; T_{amb} = 25 °C	5,5	I_{OR}	–	–	1	μA
Oscillator						
Max. oscillator frequency (Fig. 8)	4,75	f_{OSCI}	500	–	–	kHz

TELETEXT TIMING CHAIN

The SAA5020 is an MOS N-channel integrated circuit which performs the timing functions for a teletext system.
The SAA5020 is a 24-lead device which provides the necessary timing signals to the teletext page memory and to the Character Generator (SAA5050 series). It works in conjunction with the Video Processor Circuit (SAA5030) and the Teletext Acquisition and Control Circuit (SAA5040 series). The operation of the SAA5020 maintains the synchronisation between the teletext system and the incoming video signal.

QUICK REFERENCE DATA

Supply voltage	V_{DD}	nom. 5	V
Supply current	I_{DD}	typ. 20	mA
Operating ambient temperature range	T_{amb}	−20 to +70	°C

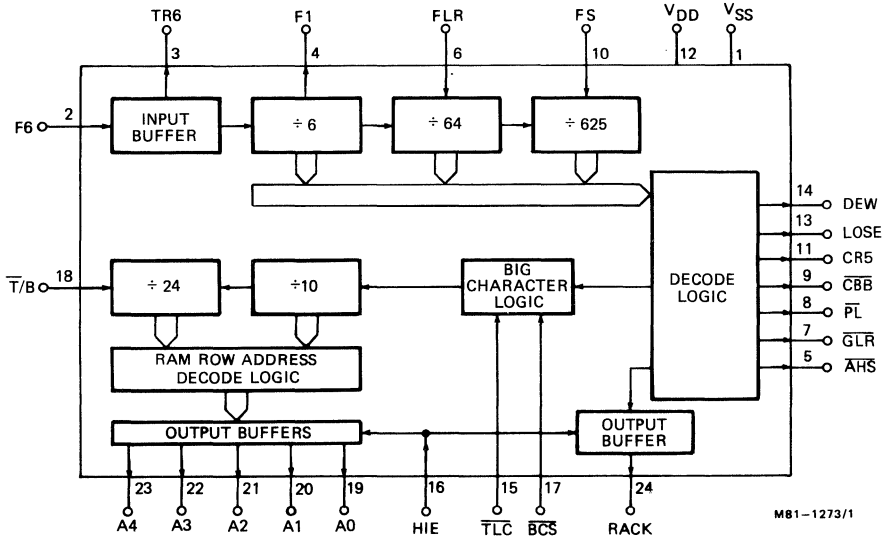


Fig.1 Block diagram

PACKAGE OUTLINE

24-lead DIL; plastic (SOT-101A)

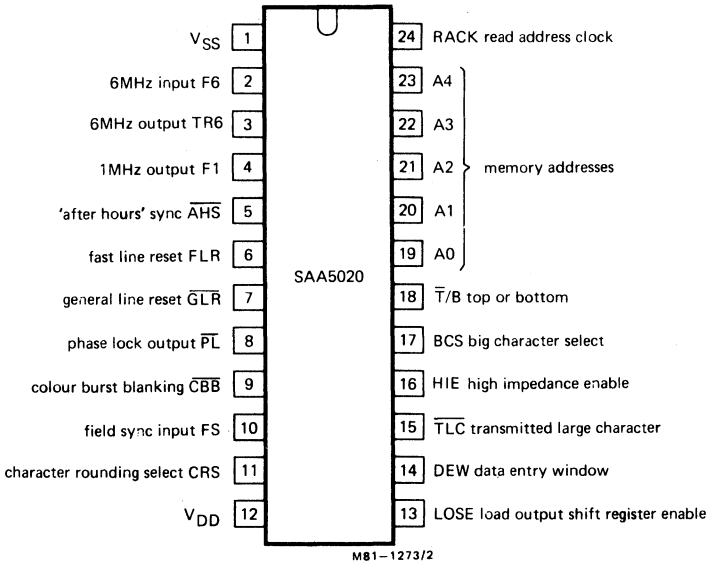


Fig.2 Pinning diagram

DESCRIPTION

The basic input to the SAA5020 is a 6 MHz clock signal from the Video Processor Circuit (SAA5030). This clock signal is buffered and is available as an output. A divide-by-six counter produces the character rate of 1 MHz. This is followed by a divide-by-64 to produce the line rate and a further divide by 312/313 to derive the field rate.

The line rate is also divided by 10 to clock a divide-by-24 counter for the teletext memory row addresses. Logic is incorporated to enable the selection of big character display, and to enable the display of transmitted large characters. An output is provided to enable character rounding for normal height characters. A composite sync. signal ($\overline{AHS}$) is available as an output which can be used to synchronise the display time bases.

HANDLING

Inputs and outputs are protected against electrostatic charge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices. (See Handling MOS Devices).

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134).

Voltages (with respect to pin 1)

			min.	max.	
Supply voltage	(pin 12)	V_{DD}	−0.3	7.5	V
Input voltage	All inputs (pins 2, 6, 10, 15, 16, 17, 18)	V_I	−0.3	7.5	V

RATINGS (continued)

		min.	typ.	max.	
Output voltage (pins 3, 4, 5, 7, 11, 13, 14)	V_O	−0.3		7.5	V
(pins 16, 19, 20, 21, 23, 24)	V_O	−0.3		7.5	V
(pins 8, 9)	V_O	−0.3		13.2	V

Temperatures

Storage temperature range	T_{stg}		−20 to +125		°C
Operating ambient temperature range	T_{amb}		−20 to +70		°C

CHARACTERISTICS

Supply voltage (pin 12)	V_{DD}	4.5	–	5.5	V
The following characteristics apply at T_{amb} = 25 °C and V_{DD} = 5 V unless otherwise stated.					
Supply current	I_{DD}	–	20	50	mA
Inputs					
6 MHz - F6 (pin 2)					
Input voltage; HIGH	V_{IH}	3.5	–	6.5	V
Input voltage; LOW	V_{IL}	Note 1	–	0	V
Rise time (between 0 V and 3.5 V levels)	t_r	–	–	25	ns
Fall time (between 0 V and 3.5 V levels)	t_f	–	–	20	ns
Mark/space ratio (measured at 1.5 V level)		40:60	–	56:44	
Input leakage current (V_I = 5.5 V)	I_{IR}	0.2	–	2	μA
All other inputs FLR (pin 6), FS (pin 10), $\overline{TLC}$ (pin 15), HIE (pin 16), $\overline{BCS}$ (pin 17), $\overline{T}$/B (pin 18)					
Input voltage; HIGH	V_{IH}	2.0	–	V_{DD}	V
Input voltage; LOW	V_{IL}	0	–	0.8	V
Input leakage current (V_I = 5.5 V)	I_{IR}	–	–	10	μA
Input capacitance	C_I	–	–	7	pF
Outputs					
TR6 (pin 3)					
Output voltage; LOW (I_{OL} = 100 μA)	V_{OL}	0	–	0.4	V
Output voltage; HIGH ($-I_{OH}$ = 100 μA)	V_{OH}	2.75	–	V_{DD}	V
Output load capacitance	C_L	–	–	15	pF
Output rise time (Note 2)	t_r	–	–	30	ns
Output fall time (Note 2)	t_f	–	–	30	ns
Mark/space ratio		40:60	–	–	

		min.	typ.	max.	
F1 (pin 4)					
Output voltage; LOW (I_{OL} = 100 μA) Note 4	V_{OL}	0	–	0.4	V
Output voltage; HIGH ($-I_{OH}$ = 100 μA)	V_{OH}	2.75	–	V_{DD}	V
Output load capacitance	C_L	–	–	35	pF
Output rise time } Note 2	t_r	–	–	50	ns
Output fall time } Note 2	t_f	–	–	30	ns
Mark/space ratio		–	–	60:40	
Delay time (measured from rising edge of TR6) Note 3	t_d	7	–	60	ns
$\overline{\text{AHS}}$ (pin 5)					
Output voltage; LOW (I_{OL} = 100 μA) Note 5	V_{OL}	0	–	0.4	V
Output voltage; HIGH ($-I_{OH}$ = 200 μA)	V_{OH}	2.4	–	V_{DD}	V
Output load capacitance	C_L	–	–	30	pF
Output rise time } Note 2	t_r	–	–	100	ns
Output fall time } Note 2	t_f	–	–	100	ns
Delay time (falling edge measured from F1 rising edge) Note 3		0	–	300	ns
$\overline{\text{GLR}}$ (pin 7)					
Output voltage; LOW (I_{OL} = 0.9 mA)	V_{OL}	0	–	0.4	V
Output voltage; HIGH ($-I_{OH}$ = 100 μA)	V_{OH}	2.4	–	V_{DD}	V
Output load capacitance	C_L	–	–	40	pF
Output rise time } Note 2	t_r	–	–	60	ns
Output fall time } Note 2	t_f	–	–	50	ns
Delay time Note 3	t_d	0	–	200	ns
$\overline{\text{PL}}$ (pin 8) (Open drain)					
Output voltage; LOW (I_{OL} = 2 mA)	V_{OL}	–	–	1.0	V
Output current in off state (V_O = 6 V)	I_O	–	–	10	μA
Output load capacitance	C_L	–	–	30	pF
Output fall time Note 2	t_f	–	–	100	ns
Delay time Note 3	t_d	0	–	250	ns
$\overline{\text{CBB}}$ (pin 9) (Open drain)					
Output voltage; LOW (I_{OL} = 1 mA)	V_{OL}	0	–	1.0	V
Output current in off state (V_O = 6 V)	I_O	–	–	10	μA
Output load capacitance	C_L	–	–	30	pF
Output fall time Note 2	t_f	–	–	200	ns
Delay time Note 3	t_d	0	–	250	ns
CRS (pin 11)					
Output voltage; LOW (I_{OL} = 100 μA)	V_{OL}	0	–	0.4	V
Output voltage; HIGH ($-I_{OH}$ = 100 μA)	V_{OH}	2.4	–	V_{DD}	V
Output load capacitance	C_L	–	–	30	pF
Output rise time } Note 2	t_r	–	–	1	μs
Output fall time } Note 2	t_f	–	–	1	μs

		min.	typ.	max.	
LOSE (pin 13)					
Output voltage; LOW (I_{OL} = 100 μA)	V_{OL}	0	–	0.4	V
Output voltage; HIGH ($-I_{OH}$ = 100 μA	V_{OH}	2.4	–	V_{DD}	V
Output load capacitance	C_L	–	–	30	pF
Output rise time (Note 2)	t_r	–	–	50	ns
Output fall time (Note 2)	t_f	–	–	50	ns
Delay time (measured from F1 falling edge) Note 3	t_d	0	–	250	ns
DEW (pin 14)					
Output voltage; LOW (I_{OL} = 100 μA)	V_{OL}	0	–	0.4	V
Output voltage; HIGH ($-I_{OH}$ = 100 μA)	V_{OH}	2.4	–	VDD	V
Output load capacitance	C_L	–	–	42	pF
Output rise time (Note 2)	t_r	–	–	200	ns
Output fall time (Note 2)	t_f	–	–	200	ns
Delay time (measured from falling edge of $\overline{CBB}$) Note 3	t_d	7.5		8.5	μs
A0,A1,A2 (pins 19, 20 and 21) 3-state					
Output voltage; LOW (I_{OL} = 100 μA)	V_{OL}	0	–	0.4	V
Output voltage; HIGH ($-I_{OH}$ = 100 μA)	V_{OH}	2.4	–	V_{DD}	V
Output load capacitance	C_L	–	–	85	pF
Output rise time (Note 2)	t_r	–	–	1	μs
Output fall time (Note 2)	t_f	–	–	1	μs
Delay time (measured from falling edge of $\overline{CBB}$) Note 3	t_d	–	–	10	μs
Leakage current in 'off' state (V_O = 5.5 V)	I_{IR}	–	–	10	μA
High impedance switching time					
Into high impedance state		0	–	0.9	μs
From high impedance state		1	–	2.9	μs
A3,A4 (pin 22 and 23) 3-state					
Output voltage; LOW (I_{OL} = 1.6 mA)	V_{OL}	0	–	0.4	V
All other parameters are as for A_0 to A_2					
RACK (pin 24) 3-state					
Output voltage; LOW (I_{OL} = 1.6 mA)	V_{OL}	0	–	0.4	V
Output voltage; HIGH ($-I_{OH}$ = 100 μA)	V_{OH}	2.4	–	V_{DD}	V
Output load capacitance	C_L	–	–	40	pF
Output rise time (Note 2)	t_r	–	–	60	ns
Output fall time (Note 2)	t_f	–	–	300	ns
Delay time (measured from dalling edge of F1) Note 3	t_d	150	–	280	ns
Leakage current in 'off' state (V_O = 5.5 V)	I_{IR}	–	–	10	μA
High impedance switching time					
Into high impedance state		1	–	2.9	μs
From high impedance state		0	–	0.9	μs

CHARACTERISTICS (continued)

Notes

1. This input incorporates an internal clamping diode, nominal $V_{IL(min)} = -0.5$ V.

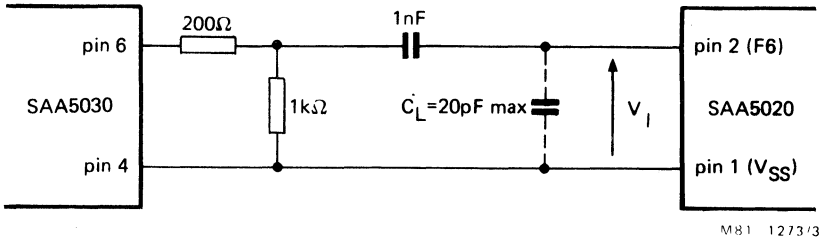


Fig.3 Capacitive coupling network for F6

2. Rise and fall times are measured between the 0.8 V and 2.0 V levels unless otherwise stated.
3. All delay times are measured from the rising edge of F1 unless otherwise stated.
   All delay times are measured at the 1.5 V level on the input to either the 2.0 V level on the rising edge of the output of the 0.8 V level on the falling edge of the output.
4. I_{OL} may be increased to 1 mA if load capacitance is less than 10 pF.
5. I_{OL} may be increased to 1.6 mA. Delay time will be increased to 350 ns max.

APPLICATION DATA

The function is quoted against the corresponding pin number.

For details of output waveforms see Fig.5

Pin No.

1. **V_{SS} Ground – 0 V.**
2. **F6**

   This input is the 6 MHz master clock signal and is used to derive the basic timings for the teletext display. It contains an internal diode clamp.

3. **TR6**

   This output is the 6 MHz character dot rate clock signal for the SAA5050 Teletext Character Generator.

4. **F1**

   This output is a 1 MHz character repetition rate clock signal for the SAA5040 Teletext Acquisition and Control device and the SAA5050 Teletext Character Generator.
   This output is synchronous with TR6, with a positive-going edge occuring at time zero of the line.

5. **$\overline{\text{AHS}}$ After hours sync**

   This output signal is an internally generated TV compound sync signal which may be used to synchronise the display (Fig.4).

6. **FLR Fast line reset**

   This input from the SAA5030 Video Processor is used to reset the internal TV line rate counter. It is a positive-going pulse of approximately 4.6 μs duration, and occurs during initial set-up of the phase-locked system.

7. $\overline{\text{GLR}}$ **General line reset**

   This output is a TV line frequency signal used for reset and clock functions in the SAA5040 Teletext Acquisition and Control device, and the SAA5050 Teletext Character Generator. It is a 1 μs negative-going pulse commencing 5 μs from the start of each line.

8. $\overline{\text{PL}}$ **Phase lock**

   This line frequency output signal to the SAA5030 Video Processor is used to phase lock the 6 MHz display system clock to the incoming television video signal. It is a 4 μs negative-going pulse commencing at 62 μs into line.

9. $\overline{\text{CBB}}$ **Colour burst blanking**

   This output signal is used to reset internal data processing and sync circuits within the SAA5030 Video Processor. It is an 8 μs negative-going pulse starting at time zero of the line.

10. **FS Field sync**

    This input signal from the SAA5030 Video Processor is used to reset the field rate counter, to maintain correct field sync with incoming video.

11. **CRS Character rounding select**

    This output signal to the SAA5050 Teletext Character Generator is required for correct character rounding of small characters within the character generator. The output is HIGH for even fields (0-313 lines) and LOW for odd fields (314-625 lines).

12. V_{DD} **+ 5 V Supply**

    This is the power supply input to the circuit.

13. **LOSE Load output shift register enable**

    This output signal to the SAA5050 Teletext Character Generator is used to reset internal control character flip-flops prior to the start of each display line. This signal also defines the character display period. It is a positive-going pulse of duration 40 μs after the start of the line and occurs on lines 49 to 288 and 362 to 601 only.

14. **DEW Data entry window**

    This output defines the period during which data may be extracted from the incoming television signal and written into the page memory. This signal is required by the SAA5040 Teletext Acquisition and Control device and the SAA5050 Teletext Character Generator. This is a positive-going pulse commencing at the end of line 5 and finishing at end of line 22 and similarly for lines 318 and 335.

15. $\overline{\text{TLC}}$ **Transmitted large character**

    This input from the SAA5050 Teletext Character Generator is to enable the correct display of large characters under broadcast control. It is HIGH for normal character display and must be taken LOW for large character display.

16. **HIE High impedance enable**

    This input when taken HIGH will switch the address and address clock (RACK) outputs to their high impedance state. For normal teletext operation this input should be connected to the DEW output (pin 14).

APPLICATION DATA (continued)

17. **$\overline{\text{BCS}}$ Big character select**

This input from the SAA5040 Teletext Acquisition and Control circuit is used to enable the correct display of large characters. It must be HIGH for normal character display and taken LOW for large character display.

18. **$\overline{\text{T}}$/B Top or bottom select**

This input from the SAA5040 Teletext Acquisition and Control device controls the RAM row address logic for correct operation of page display when large character display has been selected under user control. It must be LOW for the top half to be displayed, and HIGH for the bottom half.

19, 20
21, 22
23 **A0 to A4 Memory addresses**

These 3-state outputs to the teletext memory provide the RAM row addresses during the display period (i.e. TV lines 49 to 288 - 362 to 601 inclusive). These outputs switch to the high impedance state when HIE (pin 16) is taken HIGH. All address outputs are LOW during line 40.
During display period the outputs provide a binary count sequence which is increased every ten lines in small character mode and every twenty lines in large character mode. If any row contains transmitted large characters the address is incremented by two after 20 lines.

24. **RACK Read address clock**

This 3-state output is a 1 MHz clock occuring during the display period of the line only. This output is used to clock the external RAM address counter during the display period. The output will switch to the high impedance state when HIE (pin 16) is taken HIGH. The clock starts with a positive edge 14.65 μs from the start of a line and finishes with a negative-going edge at 53.15 μs.

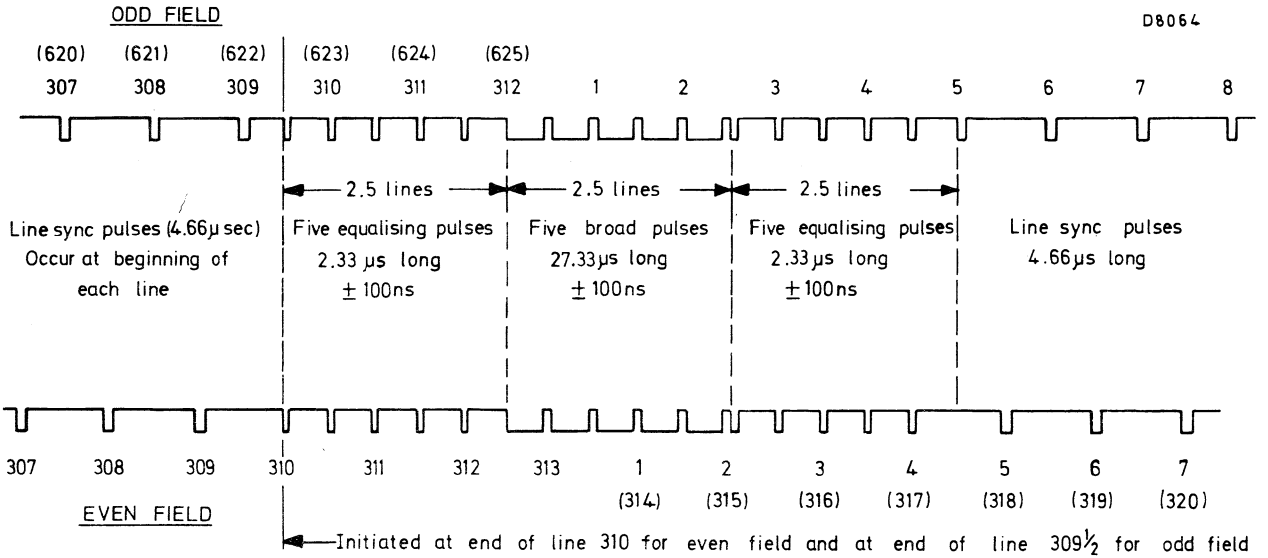


Fig.4 After hours sync waveforms ($\overline{\text{AHS}}$)

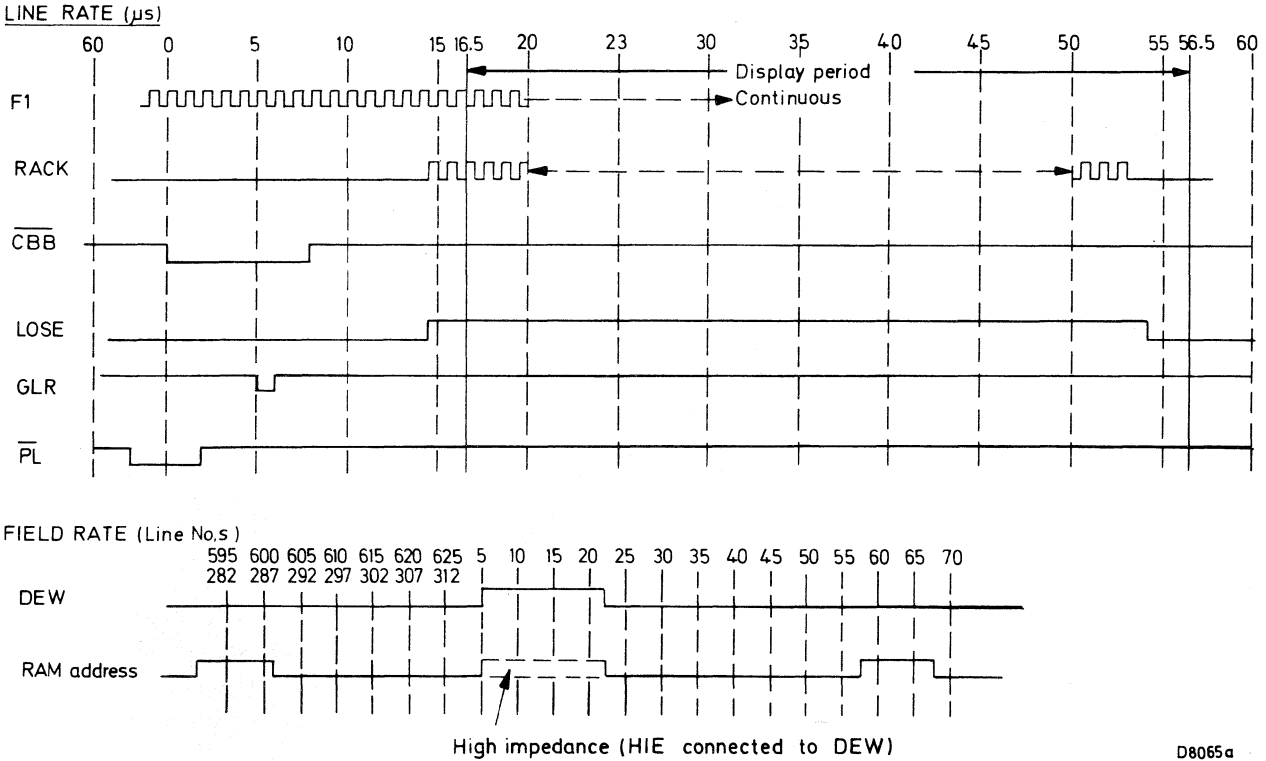


Fig.5 SAA5020 Output waveforms

TELETEXT TIMING CHAIN FOR USA 525 LINE SYSTEM

GENERAL DESCRIPTION

The SAA5025D is a MOS N-channel integrated circuit which performs the timing functions for a Teletext system. It provides the necessary timing signals to extract data from a memory and produce a display according to the USA 525 line television standard (system M).
The SAA5025D may be used in conjunction with the SAA5030 (Teletext video processor; VIP) the SAA5050 (Teletext character generator; TROM), the SAA5040B (Teletext acquisition control; TAC) and the SAA5045 (Gearing and Address Logic Array; GALA).

Features

- Designed to operate with USA 525 line television standard (system M)
- For 24 row (8 TV lines per row) x 40 character display
- Big character select input for double height characters
- Composite sync signal output for display time-base synchronization

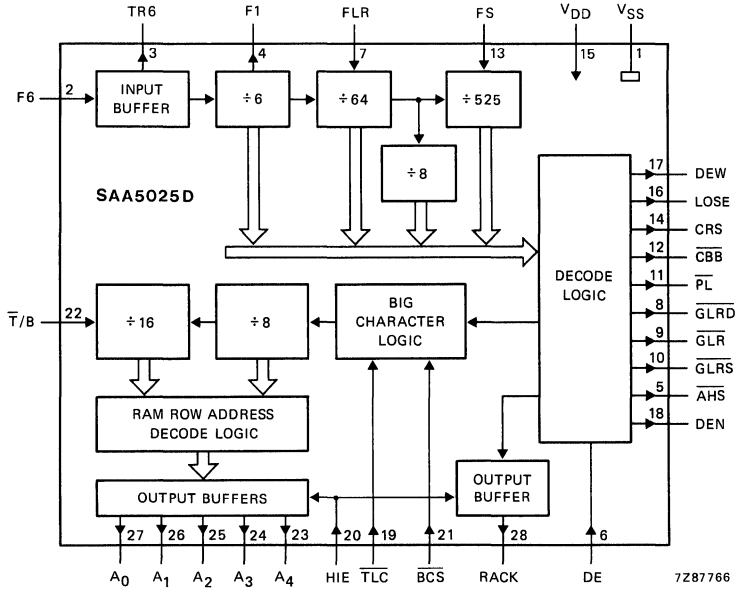


Fig. 1 Block diagram.

PACKAGE OUTLINE

28-lead DIL; plastic (SOT-117D).

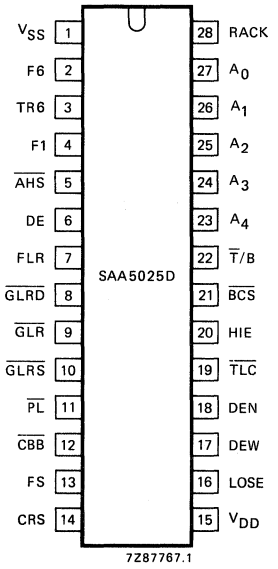


Fig. 2 Pinning diagram.

PINNING

1	V_{SS}	ground
2	F6	6,0419 MHz clock input
3	TR6	6,0419 MHz clock output
4	F1	1,007 MHz clock output
5	$\overline{AHS}$	after hours sync output
6	DE	display enable input
7	FLR	fast line reset input
8	$\overline{GLRD}$	general line reset delay output
9	$\overline{GLR}$	general line reset output
10	$\overline{GLRS}$	general line reset starting output
11	$\overline{PL}$	phase lock open drain output
12	$\overline{CBB}$	colour burst blanking output
13	FS	field (picture) sync input
14	CRS	character rounding select output
15	V_{DD}	positive supply (+ 5 V)
16	LOSE	load output shift register enable output
17	DEW	data entry window output
18	DEN	display enable output (negative-going)
19	$\overline{TLC}$	transmitted large characters input
20	HIE	high impedance enable input
21	$\overline{BCS}$	big character select input
22	$\overline{T}/B$	top/bottom select input
23	A_4	memory row address outputs (3-state)
24	A_3	
25	A_2	
26	A_1	
27	A_0	
28	RACK	read address clock output

FUNCTIONAL DESCRIPTION

The basic input to the SAB5025D is a 6,0419 MHz clock signal (e.g. from SAA5030). The clock input (F6) is buffered and also available as an output at TR6 to provide a dot rate clock. The signal at F6 is divided by 6 to produce the 1,007 MHz character rate clock at output F1, which is in turn divided by 64 to produce the line period of 63,556 μs. A divide-by-262 or 263 counter, clocked at line rate, produces a field (picture) period of 16,683 ms (average) i.e. 33,366 ms for divide-by-525. The display format is 40 characters per row for 24 rows (1 row is 8 TV lines).

A big character select ($\overline{BSC}$) input is provided and it enables double-height characters (16 TV lines per row) to be displayed. The top or bottom select ($\overline{T}/B$) input must be used in conjunction with $\overline{BCS}$ to select either the top half or bottom half of the page to be displayed on the television screen.

A composite sync ($\overline{AHS}$) output is available for synchronizing the display timebase. A high-impedance enable (HIE) input is included to switch the read address clock (RACK) and the memory row address (A_0 to A_4) outputs into their high-impedance states.

HANDLING

Inputs and outputs are protected against electrostatic charge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see "Handling MOS Devices").

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage range	V_{DD}	−0,3	+ 7,5	V
Input voltage range (note 1)	V_I	−0,3	+ 7,5	V
High-impedance state output voltage	V_{OHZ}	−0,3	+ 7,5	V
Open drain output voltage	V_{ODD}	−0,3	+ 13,2	V
Electrostatic charge protection on all inputs and outputs (notes 2 and 3)		1000	—	V
Total power dissipation per package	P_{tot}	—	275	mW
Operating ambient temperature range	T_{amb}	−20	+ 70	°C
Storage temperature range	T_{stg}	−20	+ 125	°C

Notes to ratings

1. See also characteristics on F6 input and Fig. 10.
2. Equivalent to discharging a 250 pF capacitor through a 1 kΩ series resistor.
3. N.B.: the SAA5025D is not protected against TV tube flash-over.
4. All outputs are TTL compatible.

DEVELOPMENT DATA

CHARACTERISTICS

T_{amb} = 25 °C; F6 input frequency = 6,041957 MHz; unless otherwise specified

parameter	V_{DD} V	symbol	min.	typ.	max.	unit
Supply						
Supply voltage		V_{DD}	4,5	5,0	5,5	V
Supply current	5	I_{DD}	5	–	50	mA
Inputs						
Input leakage currents						
F6	5,5	I_I	0,2	–	10	μA
	0	$-I_I$	–	–	10	μA
FLR, $\overline{TLC}$, FS, HIE, $\overline{BCS}$, $\overline{T}$/B, DE	0 to 5,5	$\pm I_I$	–	–	10	μA
Input capacitance; all inputs	5	C_I	–	–	7	pF
HIGH level input voltages						
F6; see Fig. 10	5	V_{IH}	2,7	–	6,5	V
FLR, $\overline{TLC}$, FS, HIE, $\overline{BCS}$, $\overline{T}$/B, DE	5	V_{IH}	2,0*	–	5,5	V
LOW level input voltage all inputs; see Fig. 10	5	V_{IL}	–	–	0,8*	V
Input rise and fall time F6; see Fig. 6	0 and 2,7	t_r; t_f	–	–	30	ns
Input F6 duty factor (see Fig. 10)	5	δ	40	50	56	%

* These values give no noise immunity.

DEVELOPMENT DATA

parameter	V_{DD} V	symbol	min.	typ.	max.	unit
Outputs						
Output node capacitance all outputs	5	C_O	–	–	7	pF
Output leakage current high-impedance state; A_0 to A_4, RACK	0 to 5,5	$\pm I_O$	–	–	10	μA
Output leakage current open drain; $\overline{PL}$, $\overline{CBB}$	6	I_O	–	–	10	μA
Output TR6 6,041957 MHz clock						
HIGH level output voltage $-I_{OH}$ = 100 μA	5	V_{OH}	2,75	–	V_{DD}	V
LOW level output voltage I_{OL} = 100 μA	5	V_{OL}	0	–	0,4	V
Output load capacitance	5	C_L	–	–	15	pF
Output rise and fall times see Fig. 7	5	t_r; t_f	–	–	30	ns
Duty factor at 1,5 V level depends on input F6 see F6 data and Fig. 10	5	δ	40	–	60	%
Output F1 1,007 MHz clock						
HIGH level output voltage $-I_{OH}$ = 100 μA	5	V_{OH}	2,75	–	V_{DD}	V
LOW level output voltage I_{OL} = 400 μA	5	V_{OL}	0	–	0,4	V
Output load capacitance	5	C_L	–	–	40	pF
Output rise and fall times see Fig. 7	5	t_r; t_r	–	–	50	ns
Propagation delays from rising edge of TR6; see Fig. 8; HIGH-to-LOW and LOW-to-HIGH	5	t_{PHL}; t_{PLH}	7	–	60	ns
Duty factor at 1,5 V level	5	δ	45	50	52	%

CHARACTERISTICS (continued)

parameter	V_{DD} V	symbol	min.	typ.	max.	unit
Output $\overline{\text{AHS}}$ see Fig. 6						
HIGH level output voltage $-I_{OH} = 200\ \mu A$	5	V_{OH}	2,4	–	V_{DD}	V
LOW level output voltage $I_{OL} = 1{,}6$ mA	5	V_{OL}	0	–	0,4	V
Output load capacitance	5	C_L	–	–	30	pF
Output rise and fall times see Fig. 7	5	t_r; t_f	–	–	100	ns
Propagation delay from rising edge of F1; see Fig. 8; LOW-to-HIGH	5	t_{PLH}	0	–	350	ns
Outputs $\overline{\text{GLR}}$, $\overline{\text{GLRD}}$, $\overline{\text{GLRS}}$ see Fig. 3						
HIGH level output voltage $-I_{OH} = 100\ \mu A$	5	V_{OH}	2,4	–	V_{DD}	V
LOW level output voltage $I_{OL} = 0{,}8$ mA	5	V_{OL}	0	–	0,4	V
Output load capacitance	5	C_L	–	–	40	pF
Output rise and fall times see Fig. 7	5	t_r t_f	– –	– –	70 50	ns ns
Propagation delay from rising edge of F1; see Fig. 8; HIGH-to-LOW and LOW-to-HIGH	5	t_{PHL}; t_{PLH}	0	–	300	ns
Output $\overline{\text{PL}}$ see Fig. 3						
LOW level output voltage $I_{OL} = 2$ mA	5	V_{OL}	0	–	1,0	V
Output load capacitance	5	C_L	–	–	30	pF
Output fall time; see Fig. 7	5	t_f	–	–	100	ns
Propagation delay from rising edge of F1; see Fig. 8; LOW-to-HIGH	5	t_{PLH}	0	–	250	ns

parameter	V_{DD} V	symbol	min.	typ.	max.	unit
Output $\overline{CBB}$ see Fig. 3						
LOW level output voltage I_{OL} = 2 mA	5	V_{OL}	0	–	1,0	V
Output load capacitance	5	C_L	–	–	30	pF
Output fall time; see Fig. 7	5	t_f	–	–	200	ns
Propagation delay from rising edge of F1; see Fig. 8; LOW-to-HIGH	5	t_{PLH}	0	–	250	ns
Output CRS						
HIGH level output voltage $-I_{OH}$ = 100 μA	5	V_{OH}	2,4	–	V_{DD}	V
LOW level output voltage I_{OL} = 100 μA	5	V_{OL}	0	–	0,4	V
Output load capacitance	5	C_L	–	–	30	pF
Output rise and fall times see Fig. 7	5	t_r; t_f	–	–	1	μs
Output LOSE see Fig. 3						
HIGH level output voltage $-I_{OH}$ = 100 μA	5	V_{OH}	2,4	–	V_{DD}	V
LOW level output voltage I_{OL} = 100 μA	5	V_{OL}	0	–	0,4	V
Output load capacitance	5	C_L	–	–	30	pF
Output rise and fall times; see Fig. 7	5	t_r; t_f	–	–	50	ns
Propagation delay from rising edge of F1; see Fig. 8; HIGH-to-LOW and LOW-to-HIGH	5	t_{PHL}; t_{PLH}	0	–	1	μs

DEVELOPMENT DATA

CHARACTERISTICS (continued)

parameter	V_{DD} V	symbol	min.	typ.	max.	unit
Output DEN						
HIGH level output voltage $-I_{OH} = 200\ \mu A$	5	V_{OH}	2,4	–	–	V
LOW level output voltage $I_{OL} = 100\ \mu A$	5	V_{OL}	–	–	0,4	V
Output load capacitance	5	C_L	–	–	30	pF
Output rise and fall times	5	t_r; t_f	–	–	50	ns
Propagation delay from rising edge of F1; HIGH-to-LOW and LOW-to-HIGH	5	t_{PHL}; t_{PLH}	–	–	250	ns
Output DEW see Fig. 4						
HIGH level output voltage $-I_{OH} = 200\ \mu A$	5	V_{OH}	2,4	–	V_{DD}	V
LOW level output voltage $I_{OL} = 1,6$ mA	5	V_{OL}	0	–	0,4	V
Output load capacitance	5	C_L	–	–	50	pF
Output rise and fall times	5	t_r; t_f	–	–	200	ns
Propagation delay from rising edge of $\overline{CBB}$; see Fig. 8; HIGH-to-LOW and LOW-to-HIGH	5	t_{PHL}; t_{PLH}	6,5	6,96	7,5	μs

parameter	V_{DD} V	symbol	min.	typ.	max.	unit
Outputs A_0 to A_4 see Fig. 4						
HIGH level output voltage $-I_{OH} = 100\ \mu A$	5	V_{OH}	2,4	–	V_{DD}	V
LOW level output voltage $I_{OL} = 1{,}6$ mA	5	V_{OL}	0	–	0,4	V
Output load capacitance	5	C_L	–	–	85	pF
Output rise and fall times	5	t_r; t_f	–	–	1	μs
Propagation delay from falling edge of $\overline{CBB}$; see Fig. 8; HIGH-to-LOW and LOW-to-HIGH	5	t_{PHL}; t_{PLH}	6,5	–	9,0	μs
Propagation delay from rising edge of HIE to high-impedance state; see Fig. 9	5	t_{PHZ}; t_{PLZ}	0	–	0,9	μs
Propagation delay from falling edge of HIE to normal active state; see Fig. 9	5	t_{PZH}; t_{PZL}	1	–	2,9	μs
Output RACK see Figs 3 and 4						
HIGH level output voltage $-I_{OH} = 100\ \mu A$	5	V_{OH}	2,4	–	V_{DD}	V
LOW level output voltage $I_{OL} = 1{,}6$ mA	5	V_{OL}	0	–	0,4	V
Output load capacitance	5	C_L	–	–	40	pF
Output rise and fall times see Fig. 7	5	t_r t_f	– –	– –	60 300	ns ns
Propagation delay from falling edge of F1; see Fig. 8; HIGH-to-LOW	5	t_{PHL}	150	–	280	ns
Propagation delay from rising edge of HIE to high-impedance state; see Fig. 9	5	t_{PHZ}; t_{PLZ}	1	–	2,9	μs
Propagation delay from falling edge of HIE to normal active state; see Fig. 9	5	t_{PZH}; t_{PZL}	0	–	0,9	μs

DEVELOPMENT DATA

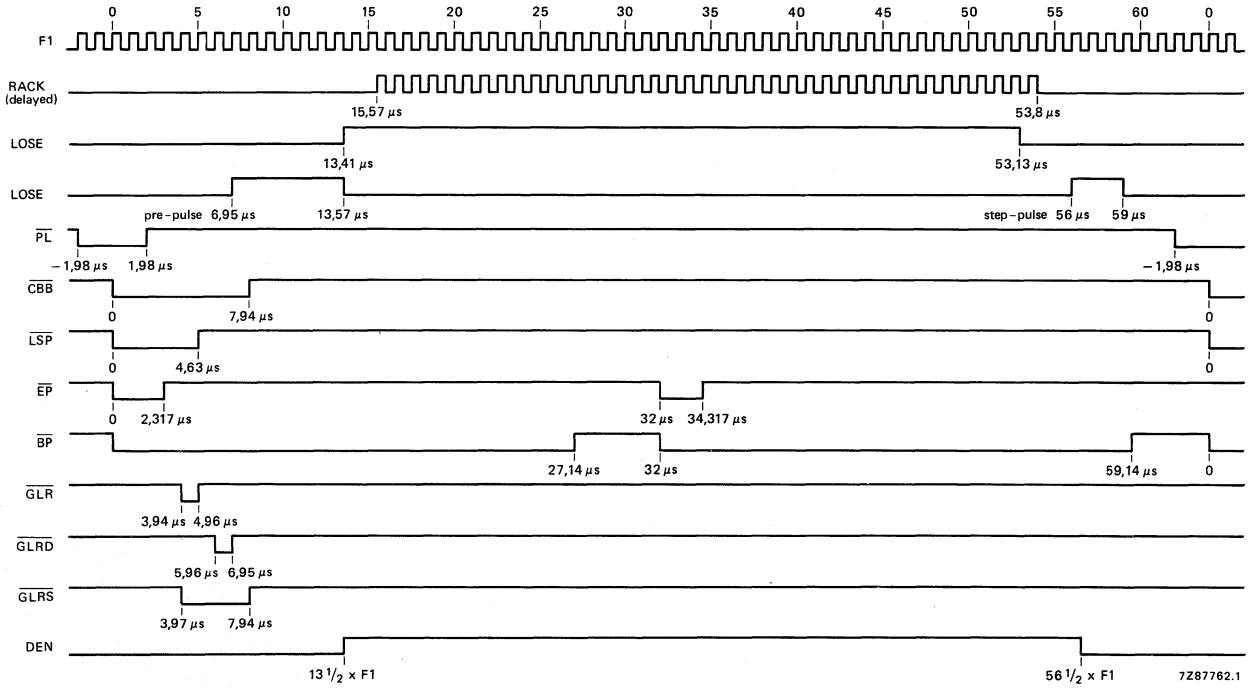


Fig. 3 Timing diagram showing the line-rate signals.

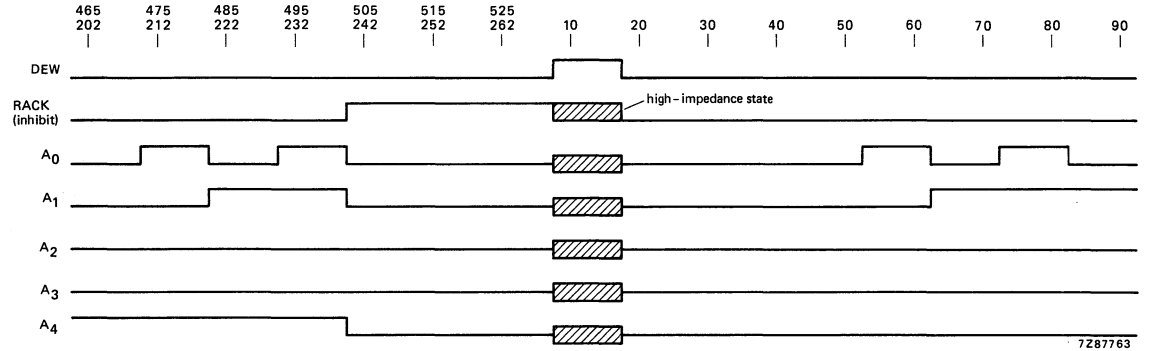


Fig. 4 Timing diagram showing the decoded signals from the field (picture) counters.

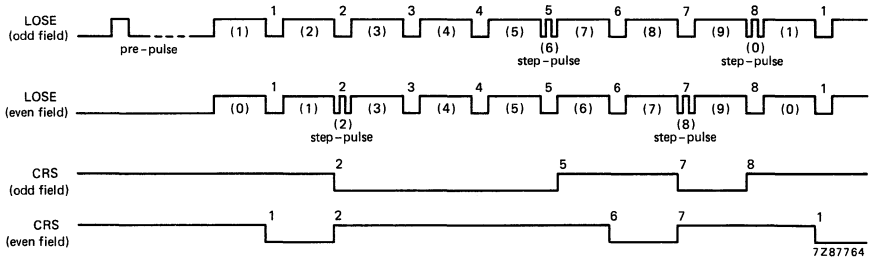


Fig. 5 Timing diagram showing the field-rate signals.

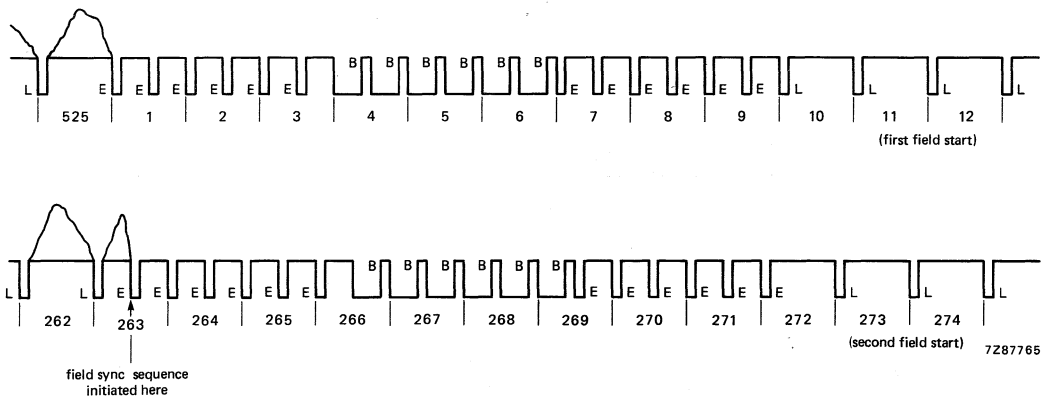
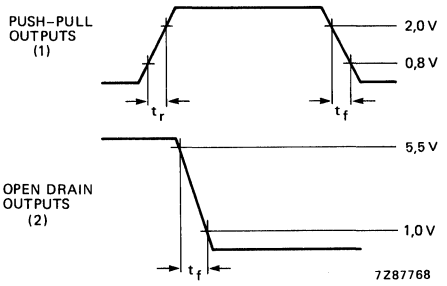


Fig. 6 After hours sync waveforms.

L = line sync pulses (4,2 to 5,1 μs)
E = equalizing pulses (2,29 μs ± 10%)
B = broad pulses (26,4 to 28 μs)



(1) These outputs will be tested with simulated TTL loads and with the load resistors adjusted such that the correct current conditions are obtained.

(2) These outputs will be tested with 3 kΩ resistors to the +6 V line for outputs $\overline{PL}$ and $\overline{CBB}$.

Fig. 7 Definition of the rise and fall times for the output stages.

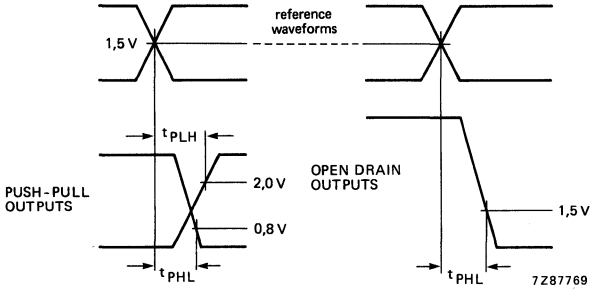


Fig. 8 Definition of the propagation delays for the output stages.

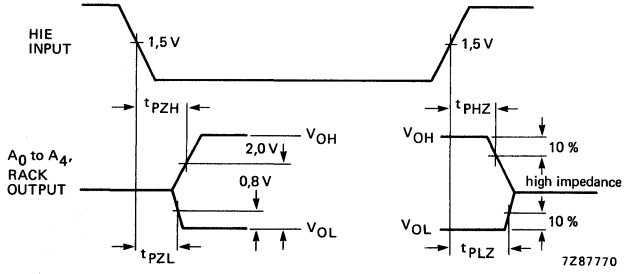


Fig. 9 Definitions of the high-impedance state propagation delay times.

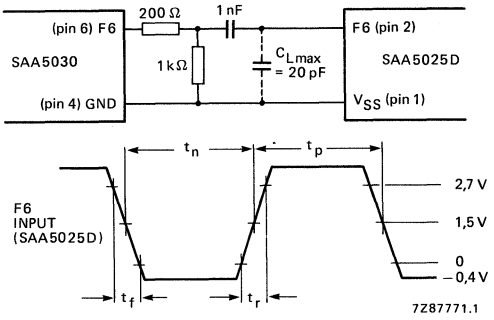


Fig. 10 Recommended 6 MHz interface circuitry between the SAA5025D and the SAA5030 (input F6). With this circuitry the F6 input will be set to a level of approximately −0,4 V in the LOW state. This is acceptable as the internal clamping diode in the F6 input of the SAA5025D provides an adequate current clamp; also shown is the F6 input waveform with the appropriate definitions.

The duty factor is defined as: $\frac{t_p}{t_p + t_n} \times 100\%$

APPLICATION INFORMATION

The function is described against the corresponding pin number.

1. **V_{SS} – ground (0 V)**

2. **F6 – 6,041957 MHz clock input**

   Obtained from video processor (SAA5030) or other source. The permissible mark/space ratio is in the range from 56:44 to 40:60 (see also Fig. 10).

3. **TR6 – 6,041957 MHz clock output**

   Dot-rate clock for Teletext character generator SAA5050 series.

4. **F1 – 1,007 MHz clock output**

   Character-rate clock for Teletext character generator SAA5050 series.

5. **$\overline{\text{AHS}}$ – after hours sync output**

   A composite sync waveform consisting of a successive sequence of line sync pulses ($\overline{\text{LSP}}$) followed by six equalizing pulses ($\overline{\text{EP}}$), six broad pulses ($\overline{\text{BP}}$) and six equalizing pulses ($\overline{\text{EP}}$), and is followed by another sequence of $\overline{\text{LSP}}$. This composite sync waveform occurs at the end and beginning of each field/picture (see also Fig. 6).

6. **DE – display enable input**

   A LOW level signal from the Teletext acquisition and control circuit (SAA5040 series) to this input switches output DEN to the LOW state.

7. **FLR – fast line reset input**

   This is the input for a positive-going pulse with a duration of 0,5 μs to 63 μs which resets the line rate counter ($\div$ 64).
   After accepting an FLR pulse, further resets are inhibited for one line period of approximately 63,5 μs.

8. **$\overline{\text{GLRD}}$ – general line reset delay output**

   A negative-going pulse with a duration of 993 ns which commences 5,96 μs from the start of each line (see also Fig. 3).

9. **$\overline{\text{GLR}}$ – general line reset output**

   A negative-going pulse with a duration of 993 ns which commences 3,97 μs from the start of each line (see also Fig. 3).

10. **$\overline{\text{GLRS}}$ – general line reset starting output**

    A negative-going pulse with starting 3,97 μs and ending 7,94 μs from the start of each line (see also Fig. 3).

11. **$\overline{\text{PL}}$ – phase lock open drain output**

    This open drain output is used to lock the oscillator in the SAA5030 to the line rate. It is a negative-going pulse with a duration of 3,96 μs which starts at 61,58 μs on one line and it ends at 1,98 μs after the start of the following line (see also Fig. 3).

DEVELOPMENT DATA

APPLICATION INFORMATION (continued)

12. $\overline{CBB}$ – colour burst blanking output

This open-drain output blanks the colour burst in the SAA5030. It is a 7,94 μs negative-going pulse which starts at the beginning of each line (t = 0; see also Fig. 3).

13. FS – field (picture) sync input

This input accepts a positive-going pulse of approximately 160 μs duration. Its leading edge occurs during the second half of line one on even fields (half picture) and correspondingly in odd fields (other half picture). It is ignored during the odd field.

14. CRS – character rounding select output

The output signal starts HIGH during the even field (lines 1 to 263), goes LOW after the 1st LOSE pulse, again HIGH after the 2nd LOSE pulse, then LOW after the 6th LOSE pulse and finally HIGH at the end of the 7th LOSE pulse. This sequence repeats every 8 lines (every row) for the entire display period (see also Fig. 5). For the odd field (lines 264 to 525) CRS starts HIGH, goes LOW after the 2nd LOSE pulse, again HIGH after the 5th LOSE pulse, then LOW after the 7th LOSE pulse and finally HIGH at the end of the 8th LOSE pulse. This sequence repeats every 8 lines (every row) for the entire display period (see also Fig. 5).

15. V_{DD} – positive supply (+ 5 V)

16. LOSE – load output shift register enable output

This is a positive-going output pulse of 39,72 μs duration commencing 13,41 μs from start of line valid during line 47 to 238 inclusive, for the even field. A step-pulse starting at the count of 3 characterrate clock pulses (F1) after the 2nd and 7th LOSE pulses and of the count of 3 character-rate clock pulses repeated every row is included. For the odd field, the LOSE pulse is preceded by a pre-pulse of 7 μs duration commencing 7,41 μs in line 20 and has a step-pulse after the 5th and 8th pulse, repeated every row (see also Fig. 5).

17. DEW – data entry window output

This output defines the period during which data may be extracted from the incoming television signal. It is HIGH during line 7 to 18 inclusive for the even fields and line 270 to 281 inclusive for the odd fields. The positive-going pulse has a duration of 762,67 μs and commences at 6,95 μs from the start of the line (see also Fig. 4).

18. DEN – display enable output

The output pulse is positive-going at 13,5 μs from the start of a line to 56,5 μs and is active during line 47 to 238 inclusive if the DE input is HIGH. If the DE input is LOW, the DEN is held in the LOW state.

19. $\overline{TLC}$ – transmitted large characters input

When this input is LOW, it enables rows of double-height characters to be displayed as required. Large characters descend into the next memory row address location. $\overline{TLC}$ is always HIGH (i.e. small) for the first line of a row, even if it contains large characters.

20. HIE – high impedance enable input

When this input is in the HIGH state it will force the RACK and memory row address output into the high-impedance state. For normal Teletext operation this input should be connected to the DEW output (pin 17).

21. $\overline{BCS}$ – big character select input

For normal size character display this input signal must be HIGH while a LOW gives double-height characters.

22. $\overline{T}$/B – top/bottom select input

When both $\overline{BCS}$ and $\overline{T}$/B are LOW the top half of a page is displayed with double-height characters. If $\overline{T}$/B is HIGH and $\overline{BCS}$ is LOW the bottom half of the page is displayed also with double-height characters.

23 to 27. A_0 to A_4 – memory row address outputs (3-state)

These binary count outputs sequencing from 00000 (count 0) to address 10111 (count 23) for the 40 x 24 format.
The binary count changes every 8 TV lines per row in the display period of line 47 to 238 inclusive for the 24 row display. The count changes between 6,5 μs and 9,0 μs during the line period.

28. RACK – read address clock output

This is the read address clock output to the SAA5045 (GALA) column address counter during the display period. It consists of 39 positive pulses at the 1,007 MHz rate starting at 13,57 μs from the start of the line period with the last negative edge occuring at 51,8 μs. This sequence is active on line 45 to 238 inclusive. RACK is delayed by two F1 clock periods for the whole of the field when input DE is LOW for the whole of line 39. On line 19 to 44 inclusive output RACK is permanently delayed by two F1 clock periods, unaffected by DE.

Note

In the big character top mode the memory row address count is 0 to 11 and in the big character bottom mode the count is 12 to 23.
Each big character row is equal to 16 television lines.

The memory row addresses are held LOW for one line period starting 6,5 μs to 9 μs from the beginning of line 36 which is only valid in the big character bottom mode.

TELETEXT VIDEO PROCESSOR

The SAA5030 is a monolithic bipolar integrated circuit used for teletext video processing. It is one of a package of four circuits to be used in teletext tv data systems. The SAA5030 extracts data and data clock information from the television composite video signal and feeds this to the Acquisition and Control circuit SAA5040. A 6 MHz crystal controlled phase locked oscillator is incorporated which drives the Timing Chain circuit SAA5020. An adaptive sync separator is also provided which derives line and field sync pulses from the input video in order to synchronise the timing chain.

QUICK REFERENCE DATA

Supply voltage	V_{CC}	nom.	12	V
Supply current (V_{CC} = 12 V)	I_{CC}	typ.	110	mA
Video input amplitude (sync-white)	$V_{16video(p-p)}$	nom.	2.4	V
Teletext data input amplitude	$V_{16teletext(p-p)}$	nom.	1.1	V
Sync amplitude	$V_{16sync(p-p)}$	nom.	0.7	V
Operating ambient temperature range	T_{amb}		−20 to +70	°C

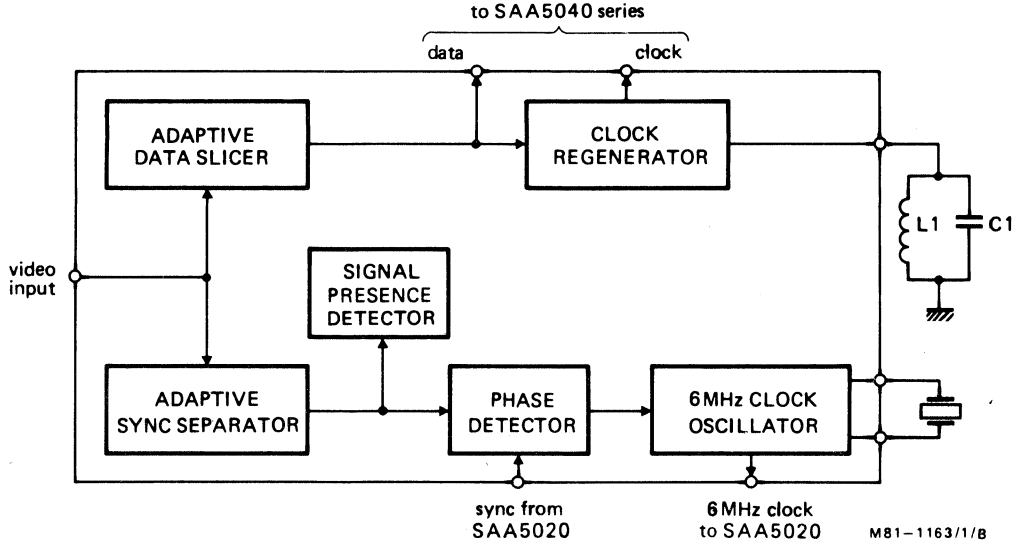


Fig.1 Block diagram

PACKAGE OUTLINE

24-lead DIL; plastic (SOT−101A with internal heat spreader).

PINNING

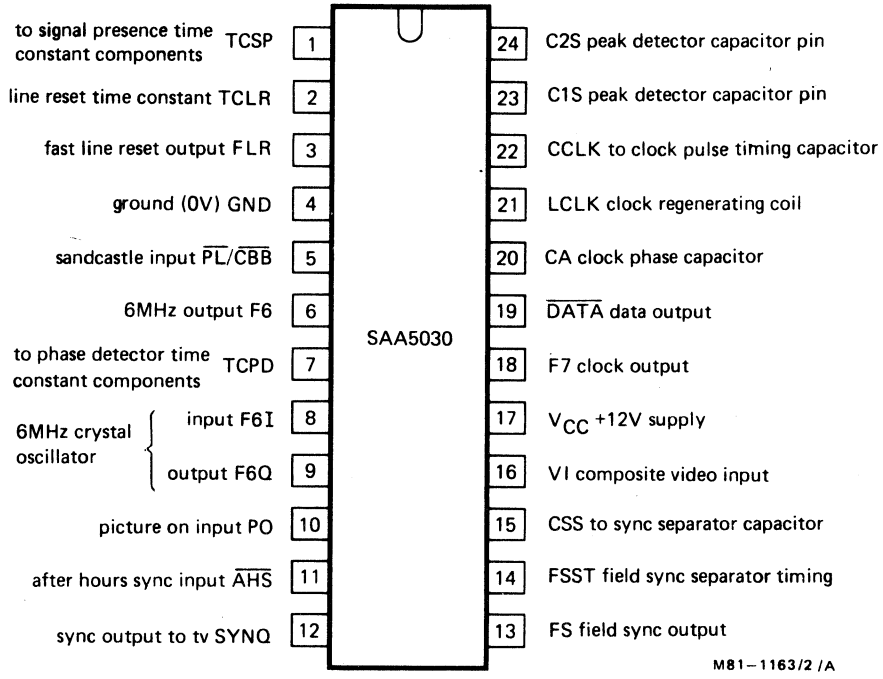


Fig.2 Pinning diagram

RATINGS Limiting values in accordance with the Absolute Maximum System. (IEC134)

Voltages					
Supply voltage	V_{17-4}	V_{CC}	max.	13.2	V
Input voltages	V_{5-4}	V_I	max.	9.0	V
	V_{10-4}	V_I	max.	V_{CC}	V
	V_{11-4}	V_I	max.	7.5	V
Temperatures					
Storage temperature range		T_{stg}		−20 to +125	°C
Operating ambient temperature range		T_{amb}		−20 to +70	°C

CHARACTERISTICS (At T_{amb} = 25 °C, V_{CC} = 12 V and with external components as shown in Fig.3 unless otherwise stated).

		min.	typ.	max.	
Supply voltage	V_{CC}	10.8	12.0	13.2	V
Supply current (V_{CC} = 12.0 V)	I_{CC}	–	110	–	mA
Video input and sync separator					
Video input amplitude (sync to white) Fig.4	$V_{16video(p-p)}$	2.0	1.4	3.0	V
Source impedance, f = 100 kHz	$\lvert Z_s \rvert$	–	–	250	Ω
Sync amplitude	$V_{16sync(p-p)}$	0.07	0.7	1.0	V
Delay through sync separator	t_d	–	0.5	–	μs
Delay between field sync datum at pin 12 and the leading edge of separated field sync at pin 13 (Note 1, Fig.4)	t_d	32	48	62	μs
Field sync output					
V_O (LOW) (I_{13} = 20 μA)	V_{OL}	–	–	0.5	V
V_O (HIGH) ($-I_{13}$ = 100 μA)	V_{OH}	2.4	–	–	V

Crystal controlled phase-locked oscillator

Measured using a crystal with the following specification e.g. catalogue number 4322 143 03241

C_1 = 27.5 fF (typ.)

C_0 = 6.8 pF (typ.)

C_L = 20 pF

Trimability (C_L increased to 30 pF) > 750 Hz

Fundamental ESR < 50 Ω

		min.	typ.	max.	
Frequency	f_{F6}	–	6.0	–	MHz
Holding range		1.5	3.0	–	kHz
Catching range		1.5	3.0	–	kHz
Control sensitivity of phase detector measured as voltage at pin 7 with respect to phase difference between separated syncs and phase lock pulse $\overline{PL}$		–	0.3	–	mV/ns
Control sensitivity of oscillator measured as change in 6 MHz phase shift from pin 8 to pin 9 with respect to voltage at pin 7		–	2	–	deg/mV
Gain of sustaining amplifier, $V_{9\text{-}8}$ measured with input voltage of 100 $mV_{p\text{-}p}$ and phase detector immobilised		2.5	–	–	V/V
Output voltage of 6 MHz signal at pin 6, measured into 20 pF load capacitance; peak-to-peak value		–	5.5	–	V
Output rise and fall times at pin 6 into 20 pF load	t_r; t_f	–	–	30	ns
Data slicer and clock regenerator					
Teletext data input amplitude, pin 16 (Note 2, Fig.4); peak-to-peak value		–	1.1	–	V
Data input amplitude at pin 16 required to enable amplitude gate flip-flop; peak-to-peak value		–	0.46	–	V
Attack rate, measured at pins 23 and 24 with a step to pin 16 (positive)		–	15	–	V/μs
(negative)		–	9	–	V/μs

		min.	typ.	max.	
Data slicer and clock regenerator (continued)					
Decay rate, measured at pins 23 and 24 with a step input to pin 16		48	100	144	mV/μs
Width of clock coil drive pulses from pin 21 when clock amplitude is not being controlled (Note 3)		–	40	–	ns
Clock hangover measured at pin 18 as the time the clock coil continues ringing after the end of data (Note 4)		20	–	–	Clock Periods
Clock and data output voltages at pins 18 and 19 measured with 20 pF load capacitance; peak-to-peak value		–	5.5	–	V
Output rise and fall times at pins 18 and 19 into 20 pF loads	t_r; t_f	–	–	30	ns
Sandcastle input					
Sandcastle detector thresholds, pin 5					
Phase lock pulse (PL) on		2	–	–	V
Phase lock pulse off		–	–	3	V
Blanking pulse ($\overline{CBB}$) on		4.5	–	–	V
Blanking pulse off		–	–	5.5	V
Dual polarity sync buffer					
After hours sync ($\overline{AHS}$) pulse input pin 11		–			
Threshold for $\overline{AHS}$ active			–	1.0	V ←
Threshold for $\overline{AHS}$ off		2.0	–	–	V ←
Picture On (PO) input, pin 10					
Threshold for PO active		2.0	–	–	V ←
Threshold for PO off		–	–	1.0	V ←
Sync output, pin 12					
$\overline{AHS}$ output with pin 10 < 1 V (Note 5) peak-to-peak value		–	0.7	–	V
Composite sync output with pin 10 > 2 V (Notes 5 and 6); peak-to-peak value		–	0.7	1.0	V
Output current		–	–	3	mA
Line reset and signal presence detectors					
Schmitt trigger threshold on pin 2 to inhibit line reset output at pin 3 (syncs coincident)		–	6.2	–	V
Schmitt trigger threshold on pin 2 to permit line reset output at pin 3 (syncs non-coincident)		–	7.8	–	V
Line reset output V_{OL} (I_3 = 20 μA)		–	–	0.5	V
Line reset output V_{OH} ($-I_3$ = 100 μA)		2.4	–	–	V
Signal presence Schmitt trigger threshold on pin 2 below which the circuit accepts the input signal		–	6.0	–	V
Signal presence Schmitt trigger threshold on pin 2 above which the input signal is rejected.		–	6.3	–	V

Notes

1. This is measured with the dual polarity buffer external resistor connected to give negative-going syncs. The measurement is made after adjustment of the potential divider at pin 14 for optimum delay.
2. The teletext data input contains binary elements as a two level NRZ signal shaped by a raised cosine filter. The bit rate is 6.9375 M bit/s. The use of odd parity for the 8-bit bytes ensures that there are never more than 14-bit periods between each data transition.
3. This is measured by replacing the clock coil with a small value resistor.
4. This must be measured with the clock coil tuned and using a clock-cracker signal into pin 16. The clock-cracker is a teletext waveform consisting of only one data transition in each byte.
5. With the external resistor connected to the ground rail, syncs are positive-going centred on +2.3 V. With the resistor connected to the supply rail, syncs are negative-going centred on +9.7 V.
6. When the composite sync is being delivered, the level is substantially the same as that at the video input.

APPLICATION DATA

The function is quoted against the corresponding pin number

Pin No.

1. **Signal presence time constant**

   A capacitor and a resistor connected in parallel between this pin and supply determine the delay in operation of the signal presence detector.

2. **Line reset time constant**

   A capacitor between this pin and supply integrates current pulses from the coincidence detector; the resultant level is used to determine whether to allow FLR pulses (see pin 3).

3. **Fast line reset output (FLR)**

   Positive-going sync pulses are produced at this output if the coincidence detector shows no coincidence between the syncs separated from the incoming video and the $\overline{CBB}$ waveform from the timing chain circuit SAA5020. These pulses are sent to the timing chain circuit and are used to reset its counters, so as to effect rapid lock-up of the phase locked loop.

4. **Ground** (0 V)

5. **Sandcastle input ($\overline{PL}$ and $\overline{CBB}$)**

   This input accepts a sandcastle waveform which is formed from $\overline{PL}$ and $\overline{CBB}$ from the timing chain SAA5020. $\overline{PL}$ is obtained by slicing the waveform at 2.5 V, and this, together with separated sync, are inputs to the phase detector which forms part of the phase locked loop. When the loop has locked up, the edges of $\overline{PL}$ are nominally 2 μs before and 2 μs after the leading edge of separated line syncs.
   CBB is obtained by slicing the waveform at 5 V, and is used to prevent the data slicer being offset by the colour burst.

6. **6 MHz output (F6)**

   This is the output of the crystal oscillator (see pins 8 and 9), and is taken to the timing chain circuit SAA5020 via a series capacitor.

7. **Phase detector time constant**

   The integrating components for the phase detector of the phase locked loop are connected between this pin and supply.

APPLICATION DATA (continued)

8, 9. **6 MHz crystal**

A 6 MHz crystal in series with a trimmer capacitor is connected between these pins. It forms part of an oscillator whose frequency is controlled by the voltage on pin 7, which forms part of the phase locked loop.

10. **Picture On input (PO)**

The PO signal from the acquisition and control circuits SAA5040 Series is fed to this input and is used to determine whether the input video (pin 16) or the $\overline{\text{AHS}}$ waveform (pin 11) appears at pin 12.

11. **After hours sync ($\overline{\text{AHS}}$)**

A composite sync waveform $\overline{\text{AHS}}$ is generated in the timing chain circuit SAA5020 and is used to synchronise the tv (see pin 10).

12. **Sync output to tv**

Either the input video of $\overline{\text{AHS}}$ is available at this output dependent on whether the PO signal is HIGH or LOW. In addition either signal may be positive-going or negative-going, dependent on whether the load resistor at this output is connected to ground or supply.

13. **Field sync output (FS)**

A pulse, derived from the input video by the field sync separator, which is used to reset the line counter in the timing chain circuit SAA5020.

14. **Field sync separator timing**

A capacitor and adjusting network is connected to this pin and forms the integrator of the field sync separator.

15. **Sync separator capacitor**

A capacitor connected to this pin forms part of the adaptive sync separator.

16. **Composite video input (VI)**

The composite video is fed to this input via a coupling capacitor.

17. **Supply voltage (+12 V)**

18. **Clock output**

The regenerated clock, after extraction from the teletext data, is fed out to the acquisition and control circuits SAA5040 Series via a series capacitor.

19. **Data output**

The teletext data is sliced off the video waveform, squared up and latched within the SAA5030. The latched output is fed to the acquisition and control circuits SAA5040 Series via a series capacitor.

20. **Clock decoupling**

A 1 nF capacitor between pin 20 and ground is required for clock decoupling.

21. **Clock regenerator coil**

A high-Q parallel tuned circuit is connected between this pin and an external potential divider. The coil is part of the clock regeneration circuit (see pin 22).

APPLICATION DATA (continued)

22. **Clock pulse timing capacitor**

Short pulses are derived from both edges of data with the aid of a capacitor connected to this pin. The resulting pulses are fed, as a current, into the clock coil connected to pin 21. Resulting oscillations are limited and taken to the acquisition and control circuits SAA5040 Series via pin 18.

23, 24 **Peak detector capacitors**

The teletext data is sliced with an automatic data slicer whose slicing level is the mid-point of two peak detectors working on the video signal. Storage capacitors are connected to these pins for the negative and positive peak detectors.

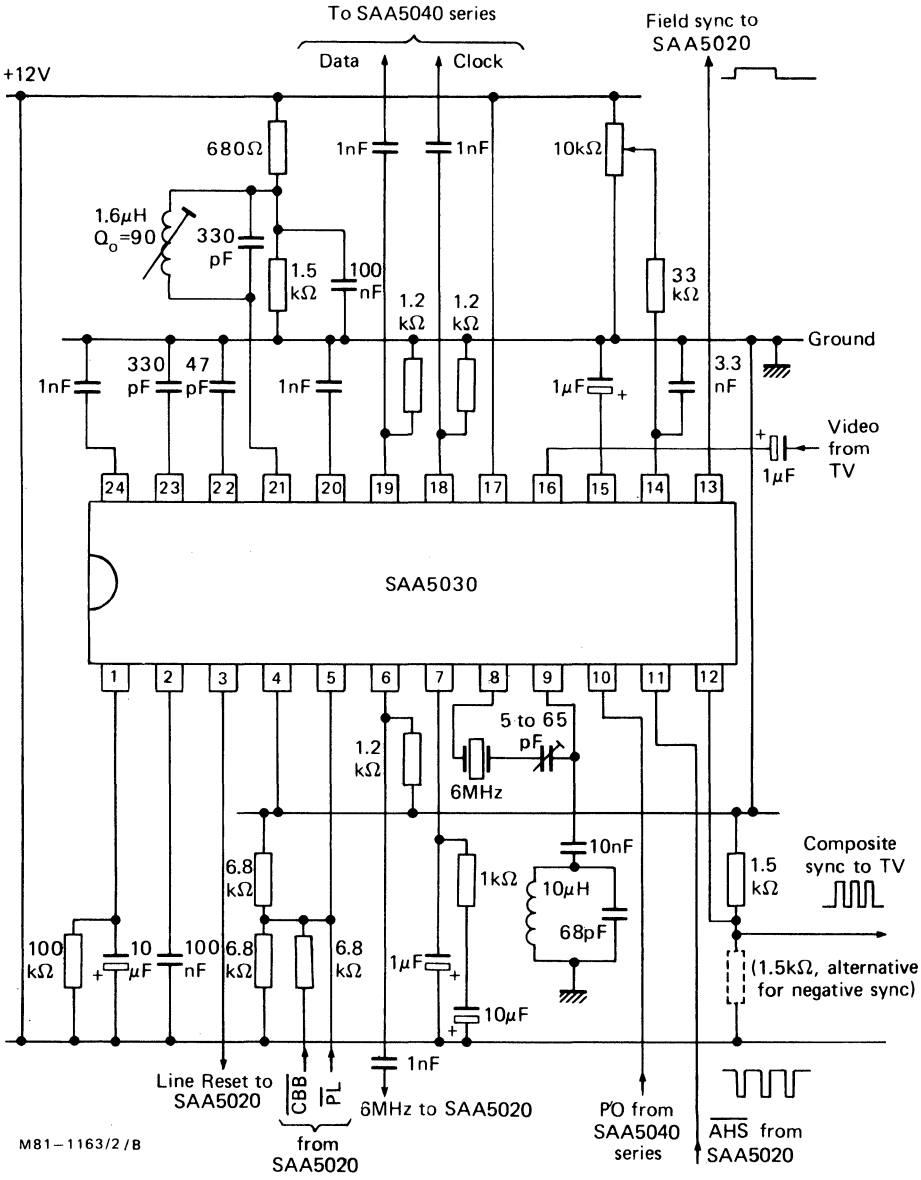


Fig.3 Peripheral circuit

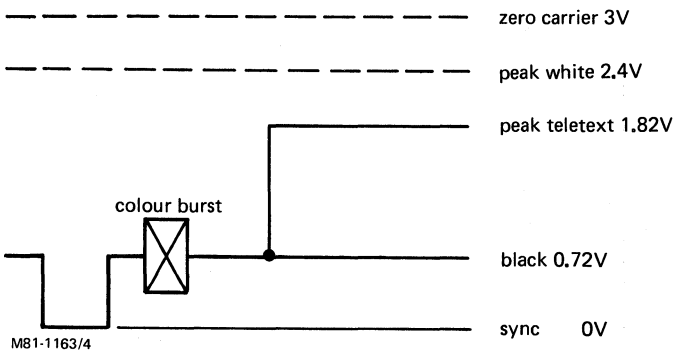


Fig.4 Part of teletext line, with burst showing nominal levels.

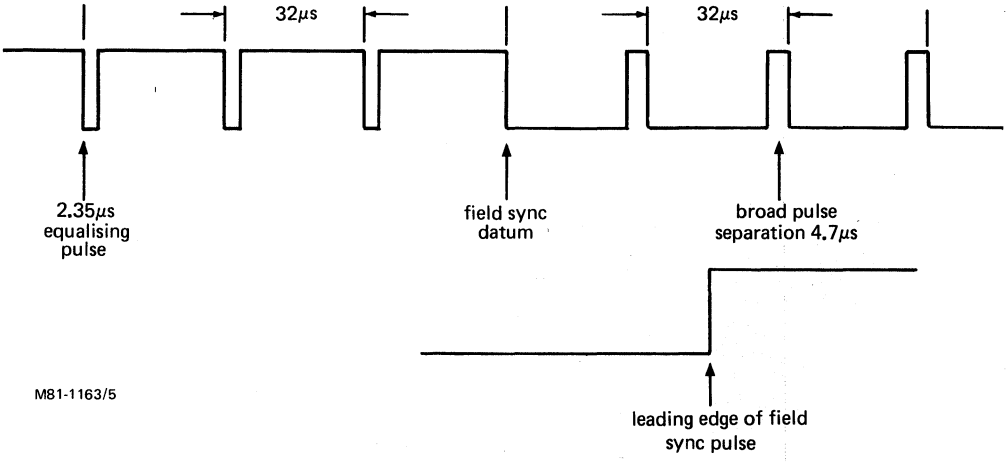


Fig.5 Detail of idealised composite sync waveform.

TELETEXT ACQUISITION AND CONTROL CIRCUIT

GENERAL

The SAA5040A, SAA5040B, SAA5040C, SAA5041, SAA5042 and form the SAA5040 series of MOS N-channel integrated circuits. They perform the control, data acquisition and data routing functions of the teletext system. The circuits differ in the on-screen display that is provided and in the decoding of the remote control commands. The functions of the circuits are detailed in Tables 1, 2 and 3; throughout the remainder of the data the SAA5040 is referred to when the complete series of the circuits is being described.

The SAA5040 is a 28-lead device which receives serial teletext data and clock signals from the remote control systems incorporating the SAA5012 or SAB3022, SAB3023 decoder circuits. The SAA5040 selects the required page information and feeds it in parallel form to the teletext page memory.

The SAA5040 works in conjunction with the SAA5020 timing chain and the SAA5050 series of character generators.

QUICK REFERENCE DATA

Supply voltage	V_{DD}	nom.	5	V
Supply current	I_{DD}	typ.	80	mA
Operating ambient temperature range	T_{amb}		−20 to +70	°C

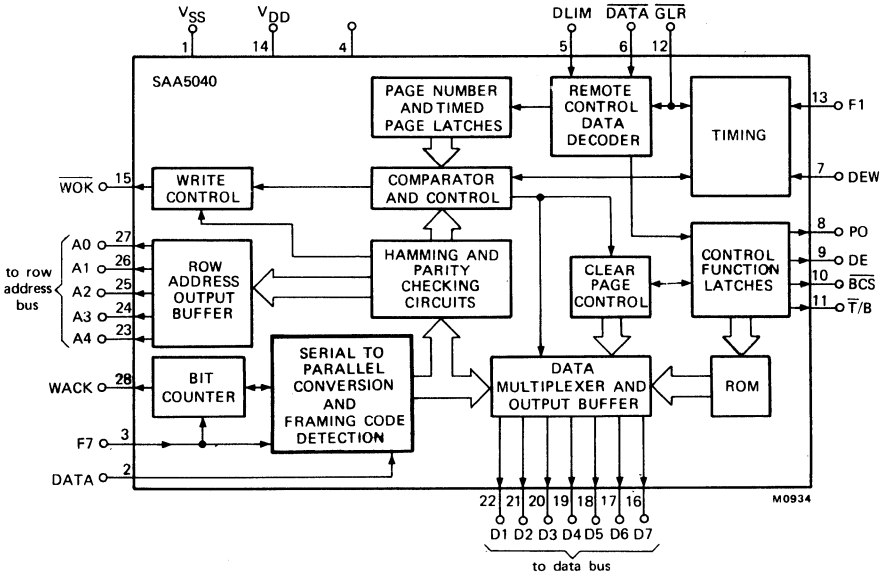


Fig.1 Block diagram.

PACKAGE OUTLINE

28-lead DIL; plastic (SOT-117)

PINNING

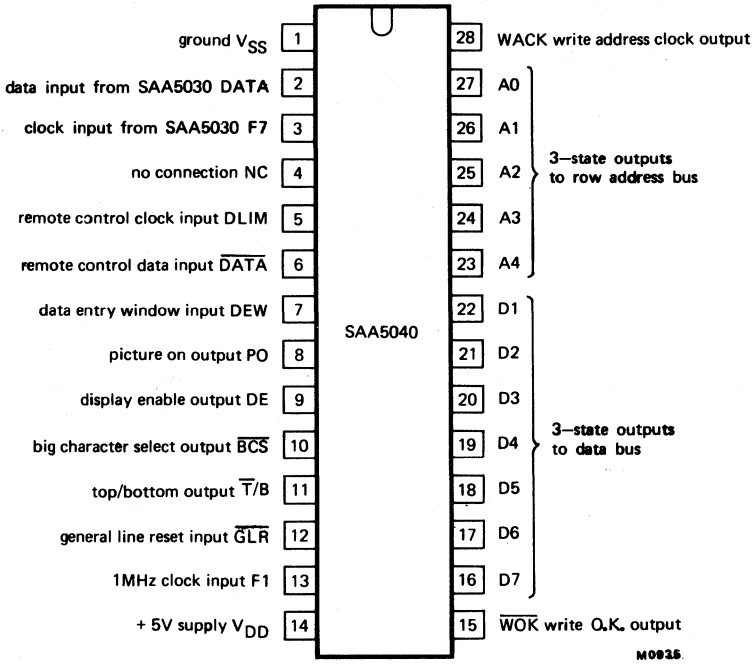


Fig.2 Pinning diagram.

DESCRIPTION

The circuit consists of two main sections.

a) Data acquisition section

The basic input to this section is the serial teletext data stream DATA from the SAA5030 video processor circuit. This data stream is clocked at a 6.9375 MHz clock rate (F7) from the SAA5030. The incoming data stream is processed and sorted so that the page of data selected by the user is written as 7-bit parallel words into the system memory. Hamming and parity checks are performed on the incoming data to reduce errors. Provision is also made to process the control bits in the page header.

b) Control section

The basic input to this section is the 7-bit serial data ($\overline{DATA}$) from the remote control decoder circuit such as the SAA5012 or SAB3012. This is clocked by the DLIM signal.
The remote control commands are decoded and the control functions are stored.
Full details of the remote control commands used in the various SAA5040 series options are given in Tables 1, 2 and 3 below. The control section also writes data into the page memory independently of the data acquisition section. This gives an on-screen display of certain user-selected functions such as page number and programme name.
The 3-state data and address outputs to the system memory are set to high impedance state if certain remote control commands are received (e.g. viewdata mode). This is to allow another circuit to access the memory using the same address and data lines. The address lines are also high impedance while the acquisition and control circuit is not writing into the memory.
Further information on the control of the complete teletext system is available.
The circuit is designed in accordance with the September 1976 Broadcast Teletext specification published by BBC/IBA/BREMA.
A typical circuit diagram of a teletext decoder is shown in Fig.7.

HANDLING

Inputs and outputs are protected against electrostatic charge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see "Handling MOS devices").

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC134).

Voltages (with respect to pin 1)

		min.	max.	
Supply voltage (pin 14)	V_{DD}	−0.3	7.5	V
Input voltage (all inputs)	V_I	−0.3	7.5	V
Output voltage (pin 8)	V_{O8}	−0.3	13.2	V
Output voltage (all other outputs)	V_O	−0.3	7.5	V
Temperatures				
Storage temperature range	T_{stg}		−20 to +125	°C
Operating ambient temperature range	T_{amb}		−20 to +70	°C

CHARACTERISTICS

		min.	typ.	max.	
Supply voltage (pin 14)	V_{DD}	4.5	–	5.5	V

The following characteristics apply at T_{amb} = 25 °C and V_{DD} = 5 V unless otherwise stated.

Supply current	I_{DD}	–	80	120	mA
Inputs					
F7 DATA (pin 2), **F7 CLOCK** (pin 3)					
Input voltage; HIGH	V_{IH}	3.5	–	5.5	V
Input voltage; LOW Note 1	V_{IL}	–	–	0.5	V
Rise time	t_r	–	–	30	ns
Fall time	t_f	–	–	30	ns
Input resistance (measured at 4 V)	R_I	2	–	18	MΩ
Input capacitance	C_I	–	–	7	pF
F1 (pin 13)					
Input voltage; HIGH	V_{IH}	2.4	–	V_{DD}	V
Input voltage; LOW	V_{IL}	0	–	0.6	V
Rise time	t_r	–	–	50	ns
Fall time	t_f	–	–	30	ns
Input capacitance	C_I	–	–	7	pF
Input leakage current (V_I = 0 to 5.5 V)	I_{IR}	–	–	10	μA
All other inputs					
DLIM (pin 5), $\overline{\textbf{DATA}}$ (pin 6), **DEW** (pin 7), $\overline{\textbf{GLR}}$ (pin 12)					
Input voltage; HIGH	V_{IH}	2.0	–	V_{DD}	V
Input voltage; LOW	V_{IL}	0	–	0.8	V
Input capacitance	C_I	–	–	7	pF
Input leakage current (V_I = 0 to 5.5 V)	I_{IR}	–	–	10	μA
Outputs					
DE (pin 9), $\overline{\textbf{BCS}}$ (pin 10), $\overline{\textbf{T}}$/**B** (pin 11) (with internal pull-up to V_{DD})					
Output voltage; LOW (I_{OL} = 400 μA)	V_{OL}	0	–	0.5	V
Output voltage; HIGH $-I_{OH}$ = 50 μA for pin 9 $-I_{OH}$ = 30 μA for pin 10 $-I_{OH}$ = 20 μA for pin 11	V_{OH}	2.4	–	V_{DD}	V
Output voltage rise time	t_r	–	–	10	
Output voltage fall time	t_f	–	–	1	μs
Output capacitance	C_O	–	–	7	pF
Output current with output in HIGH state (V_O = 0.5 V)	$-I_O$	50	–	500	μA

CHARACTERISTICS Continued

		min.	typ.	max.	
PO (pin 8) (with internal pull-up to V_{DD})					
Output voltage; LOW (I_{OL} = 140 μA)	V_{OL}	0	–	0.5	V
Output voltage; HIGH ($-I_{OH}$ = 50 μA)	V_{OH}	2.4	–	V_{DD}	V
Output rise and fall time (C_L = 40 pF) (Note 3)	t_r, t_f	–	–	10	μs
Output capacitance	C_O	–	–	7	pF
Output current with output in HIGH state (V_O = 0.5 V)	$-I_O$	50	–	500	μA
D1 to D7 (pins 16 to 22) (3-state)					
Output voltage; LOW (I_{OL} = 100 μA)	V_{OL}	0	–	0.5	V
Output voltage; HIGH (I_{OH} = −100 μA)	V_{OH}	2.4	–	V_{DD}	V
Output rise and fall time (C_L = 40 pF) (Note 3)	t_r, t_f	–	–	100	ns
Output leakage current in 'OFF' state (V_O = 0 to 5.5 V)	$\pm I_{OROff}$	–	–	10	μA
Output capacitance	C_O	–	–	7	pF
$\overline{\text{WOK}}$ (pin 15) (3-state with internal pull-up to V_{DD})					
Output voltage; LOW (I_{OL} = 400 μA)	V_{OL}	0	–	0.5	V
Output voltage; HIGH ($-I_{OH}$ = 200 μA)	V_{OH}	2.4	–	V_{DD}	V
Output voltage rise time (C_L = 80 pF) (Note 3)	t_r	–	–	50	ns
Output voltage fall time (C_L = 80 pF) (Note 3)	t_f	–	–	100	ns
Output current with 3-state 'OFF' (V_O = 0.5 V)	$-I_{OROff}$	80	–	500	μA
Output capacitance	C_O	–	–	7	pF
WACK (pin 28) (3-state)					
Output voltage; LOW (I_{OL} = 1.6 mA)	V_{OL}	0	–	0.5	V
Output voltage; HIGH ($-I_{OH}$ = 100 μA)	V_{OH}	2.4	–	V_{DD}	V
Output voltage rise time (C_L = 40 pF) (Note 3)	t_r	–	–	50	ns
Output voltage fall time (C_L = 40 pF) (Note 3)	t_f	–	–	300	ns
Output leakage current in 'OFF' state (V_O = 0 to 5.5 V)	$\pm I_{OROff}$	–	–	10	μA
Output capacitance	C_O	–	–	7	pF
A0 to A2 (pins 25 to 27) (3-state)					
Output voltage; LOW (I_{OL} = 200 μA)	V_{OL}	0	–	0.5	V
Output voltage; HIGH ($-I_{OH}$ = 200 μA)	V_{OH}	2.4	–	V_{DD}	V
Output rise and fall time (C_L = 90 pF) (Note 3)	t_r, t_f	–	–	300	ns
Output leakage current in 'OFF' state (V_O = 0 to 5.5 V)	$\pm I_{OROff}$	–	–	10	μA
Output capacitance	C_O	–	–	7	pF

CHARACTERISTICS (Continued)

Outputs

		min.	typ.	max.	
A3 and A4 (pins 23 and 24) (3-state)					
Output voltage; LOW (I_{OL} = 1.6 mA)	V_{OL}	0	–	0.5	V
Output voltage; HIGH ($-I_{OH}$ = 200 μA)	V_{OH}	2.4	–	V_{DD}	V
Output rise and fall time (C_L = 40 pF) (Note 3)	t_r, t_f	–	–	300	ns
Output leakage current in 'OFF' state (V_O = 0 to 5.5 V)	$+I_{ORoff}$	–	–	10	μA
Output capacitance	C_O	–	–	7	pF

TIMING CHARACTERISTICS

Teletext Data and Clock (F7 DATA + F7 CLOCK) (Note 2 and Fig.3)					
F7 Clock cycle time	TF_7	144	–	–	ns
F7 Clock duty cycle (HIGH to LOW)		30	–	70	%
F7 Clock to data set-up time	t_{SU}	–	60	–	ns
F7 Clock to data hold time	t_{HOLD}	–	40	–	ns
Control $\overline{\text{DATA}}$ and Clock ($\overline{\text{DATA}}$ + DLIM) (Note 3 and Fig.4)					
DLIM Clock HIGH time	t_{CH}	6.5	8	Note 4	μs
DLIM Clock LOW time	t_{CL}	3.5	8	60	μs
DLIM to DATA set-up time	t_{SU}	0	14	–	μs
DLIM to DATA hold time	t_{HOLD}	8	14	–	μs
Writing Teletext data into memory during DEW (Fig.5)					
WACK cycle time	T_{WACK}	1150	–	–	ns
WACK rising edge to $\overline{\text{WOK}}$ falling edge	t_{AWW}	250	–	450	ns
WACK rising edge to $\overline{\text{WOK}}$ rising edge	t_{WRW}	150	–	310	ns
$\overline{\text{WOK}}$ pulse width	t_{WPD}	300	–	–	ns
Data output set-up time	t_{DW}	330	–	–	ns
Data output hold time	t_{DH}	0	–	–	ns
Row address set-up time before first $\overline{\text{WOK}}$	t_{RAW}	190	–	–	ns
Row address valid time after last $\overline{\text{WOK}}$	t_{RWR}	0	–	–	ns

TIMING CHARACTERISTICS

		min.	typ.	max.	
Writing Header information into memory during tv line 40					
(Fig.6)					
This arrangement is a combined phasing of the SAA5040 and the SAA5020 and is therefore referred to F1 input. The first $\overline{WOK}$ is related to F1 No 14½ from the SAA5020					
F1 Clock cycle time		1000	–	–	ns
Time from F1 to $\overline{WOK}$ falling edge	t_{WF}	300	–	500	ns
Time from F1 to $\overline{WOK}$ rising edge	t_{FW}	0	–	120	ns
Data output set-up time	t_{DW}	330	–	–	ns
Data output hold time	t_{DH}	0	–	–	ns

Notes

1. These inputs may be a.c. coupled. Minimum rating is −0.3 V but the input may be taken more negative if a.c. coupled.
2. Transition times measured between 0.5 and 3.5 volt levels.
   Delay times are measured from 1.5 V level.
3. Transition times measured between 0.8 and 2.0 volt levels.
   Delay times are measured from 1.5 V level.
4. There is no maximum DLIM cyle time provided the DLIM duty cycle is such that $t_{CLmax.}$ requirement is not exceeded.

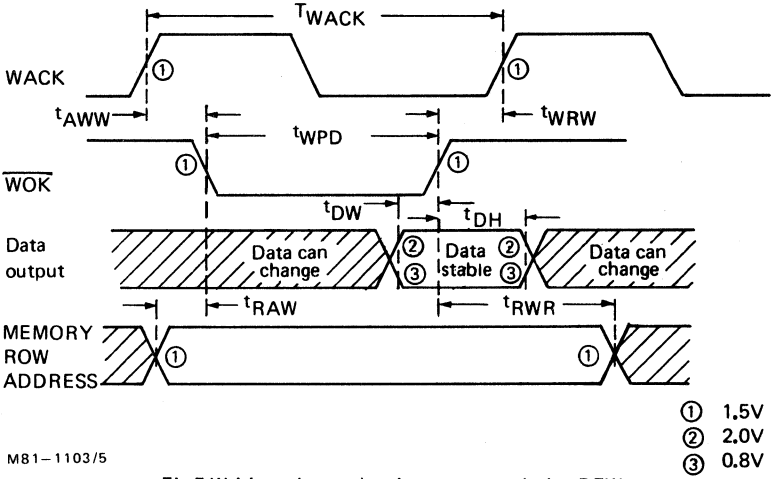


Fig.5 Writing teletext data into memory during DEW

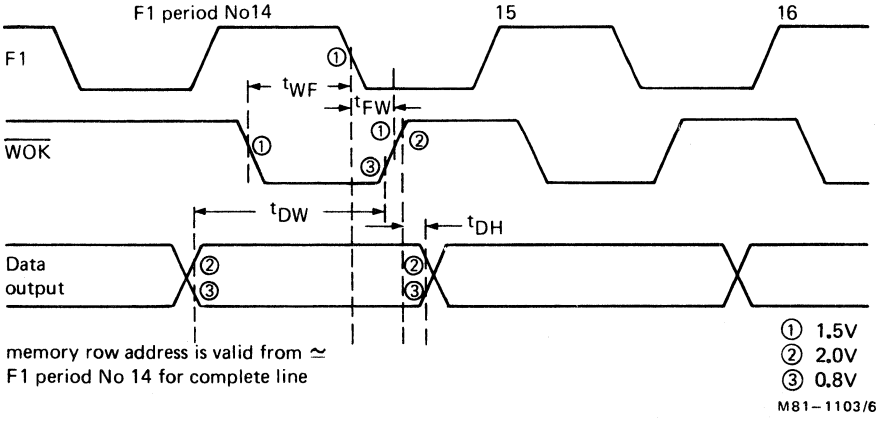


Fig.6 Writing data into memory during tv line 40

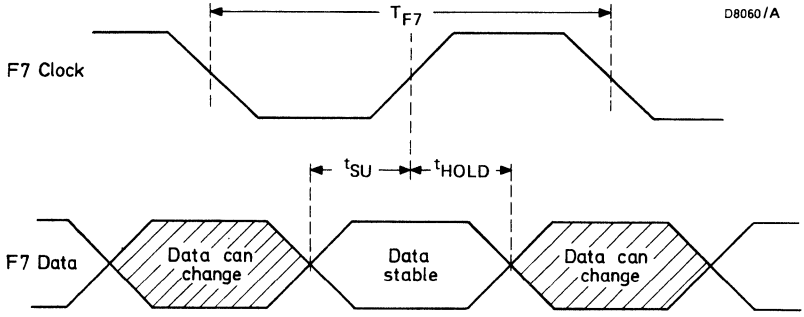


Fig.3 Teletext data timing

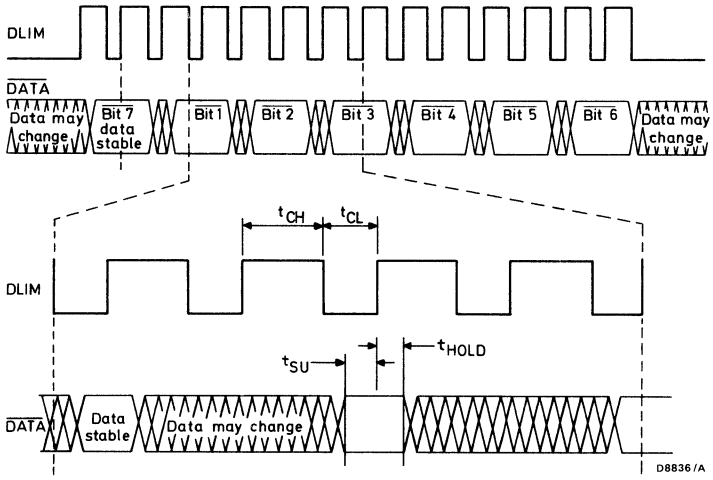


Fig.4 Remote control data input timing

APPLICATION DATA

The function is quoted against the corresponding pin number

Pin No.

1. V_{SS} Ground - 0 V
2. **DATA Data input from SAA5030**

   This input is a serial data stream of broadcast teletext data from the SAA5030 video processor, the data being at a rate of 6.9375 MHz.
   This input from the SAA5030 is a.c. coupled with internal d.c. restoration of the signal levels.
3. **F7 Clock input from SAA5030**

   This input is a 6.9375 MHz clock from the SAA5030 video processor which is used to clock the teletext data acquisition circuitry. The positive edge of this clock is nominally at the centre of each teletext data bit.
   This input from the SAA5030 is a.c. coupled with internal d.c. restoration of the signal levels.
5. **DLIM Remote control clock input**

   This input from the remote control receiver decoder is used to clock remote control data into the SAA5040. The positive-going edge of every second clock pulse is nominally in the centre of each remote control data bit.
6. **$\overline{\text{DATA}}$ Remote control data**

   This input is a 7-bit serial data stream from the remote control receiver decoder.
   This data contains the teletext and viewdata remote control user functions. The nominal data rate is 32 μs/bit. The remote control commands used in the SAA5040 series are shown in Tables 1, 2 and 3.
7. **DEW Data entry window**

   This input from the SAA5020 Timing Chain defines the period during which received teletext data may be accepted by the SAA5040. This signal is also used to enable the 5 memory address outputs (pins 23 to 27) and the 7-bit parallel data outputs (pins 16 to 22).
8. **PO Picture On**

   This output to the SAA5012, SAA5030 and SAA5050 circuits is a static level used for the selection of tv picture video 'on' or 'off'. The output is HIGH for tv picture 'ON', LOW for tv picture 'OFF'. The output has an internal pull-up to V_{DD}.
9. **DE Display enable**

   This output to the SAA5050 teletext character generator is used to enable the teletext display. The output is HIGH for display enabled, LOW for display disabled.
   The output is also forced to the LOW state during the DEW and tv line 40 periods and when a teletext page is cleared.
   The output has an internal pull-up to V_{DD}.
10. **$\overline{\text{BCS}}$ Big character select**

    This output to the SAA5020 timing chain and to the SAA5050 character generator is used to select double height character format under user control. The output is HIGH for normal height characters, LOW for double height characters. It is also forced to the HIGH state on page clear.
    The output has an internal pull-up to V_{DD}.
11. **$\overline{\text{T}}$/B Top/bottom**

    This output to the SAA5020 timing chain is used to select whether top or bottom half page is being viewed. The output is HIGH for bottom half page and LOW for top half page. It is also forced to the LOW state on page clear.
    The output has an internal pull-up to V_{DD}.

APPLICATION DATA

12. **$\overline{\text{GLR}}$ General line reset**

This input from the SAA5020 timing chain is used as a reset signal for internal control and display counter.

13. **F1**

This input is a 1 MHz clock signal from the SAA5020 timing chain used to clock internal remote control processing and encoding circuits.

14. **V_{DD} +5 V Supply**

This is the power supply input to the circuit.

15. **$\overline{\text{WOK}}$ Write O.K.**

This 3-state output signal to the system memory is used to control the writing of valid data into the system memory. The signal is LOW to write, and is in the high impedance state when viewdata is selected. The three-state buffer is enabled at the same time as the data outputs (see below). An internal pull-up device prevents the output from floating into the LOW state when the 3-state buffer is OFF.

16, 17, 18, 19, 20, 21, 22 **D7 to D1, Data outputs**

These 3-state outputs are the seven bit parallel data outputs to the system memory. The outputs are enabled at the following times:—

a) During the data entry window (DEW) to write teletext data into the memory. The data rate is 867 kbytes per second and is derived from the teletext data clock.

b) During tv line 40 for encoded status information about user commands (e.g. programme number), to be written into the memory. This period is known as EDIL (encoded data insertion line). The data rate is 1 Mbyte per second and is derived from the 1 MHz display clock F1.

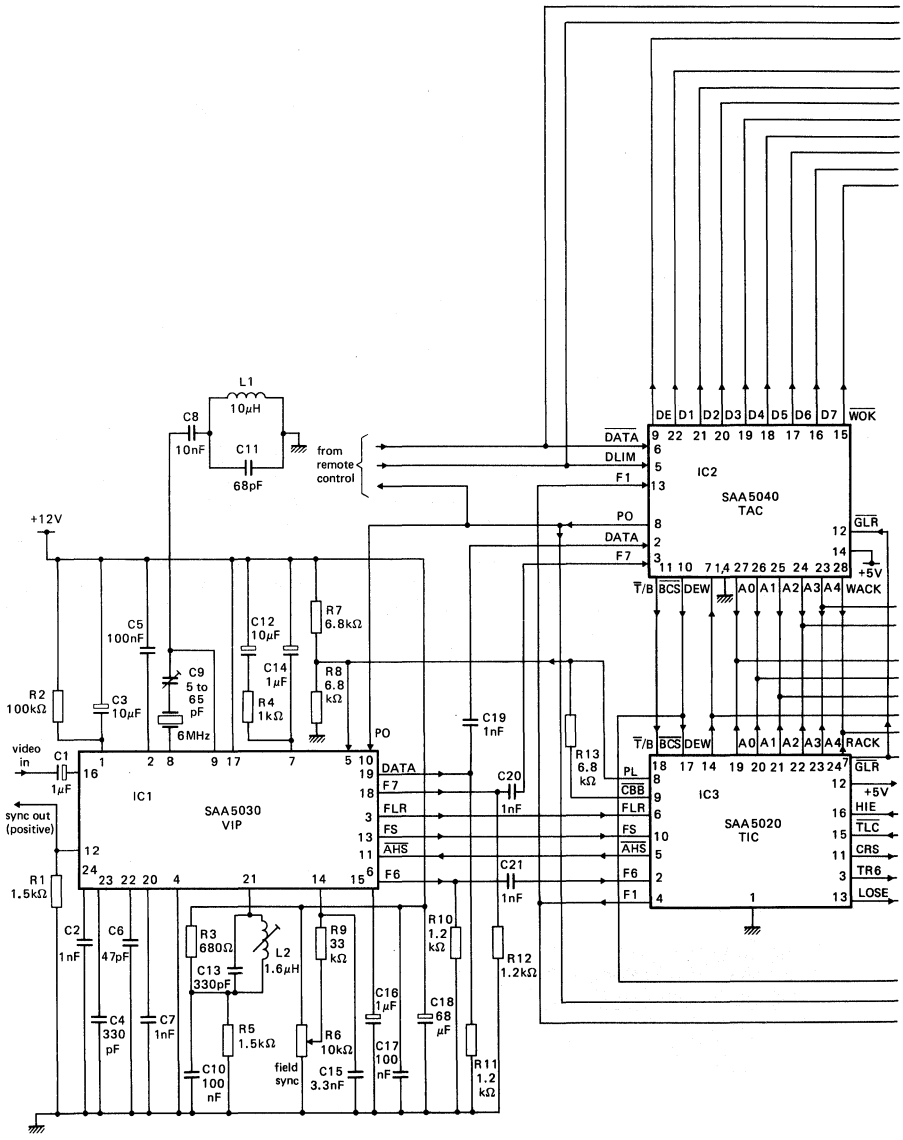
c) When the page is cleared. In this case the data output is forced to the space code (0100000) during the display period for one field. This data is held at the space code from either tv line 40 (if page clear is caused by user command), or the received teletext data line causing the clear function, until the start of the data entry window (DEW) of the next field.

23, 24, 25, 26, 27 **A4 to A0 Memory addresses**

These 3-state outputs are the 5-bit row address to the page memory. This address specifies in which of 24 rows the teletext data is to be written. The outputs are enabled during the data entry period (DEW).

28. **WACK Write address clock**

This 3-state output is used to clock the memory address counter during the data entry period (DEW). The output is enabled only during this period. The positive-going edge of WACK is used to clock the address counter.


L1
10μH
C8
10nF
C11
68pF
from
remote
control
+12V
C5
100nF
C12
10μF
C14
1μF
R7
6.8kΩ
R8
6.8
kΩ
C9
5 to
65
pF
6MHz
R2
100kΩ
C3
10μF
R4
1kΩ
video
in
C1
1μF
sync out
(positive)
R1
1.5kΩ
IC1
SAA5030
VIP
PO
DATA
F7
FLR
FS
AHS
F6
C19
1nF
C20
1nF
C21
1nF
R13
6.8
kΩ
R10
1.2
kΩ
R12
1.2kΩ
R11
1.2
kΩ
C2
1nF
C6
47pF
C4
330
pF
C7
1nF
R3
680Ω
L2
1.6μH
C13
330pF
R5
1.5kΩ
C10
100
nF
R9
33
kΩ
R6
10kΩ
field
sync
C15
3.3nF
C16
1μF
C17
100
nF
C18
68
μF
IC2
SAA5040
TAC
DE D1 D2 D3 D4 D5 D6 D7 WOK
DATA
DLIM
F1
PO
DATA
F7
GLR
+5V
T/B BCS DEW A0 A1 A2 A3 A4 WACK
IC3
SAA5020
TIC
PL
CBB
FLR
FS
AHS
F6
F1
T/B BCS DEW A0 A1 A2 A3 A4 RACK
GLR
+5V
HIE
TLC
CRS
TR6
LOSE

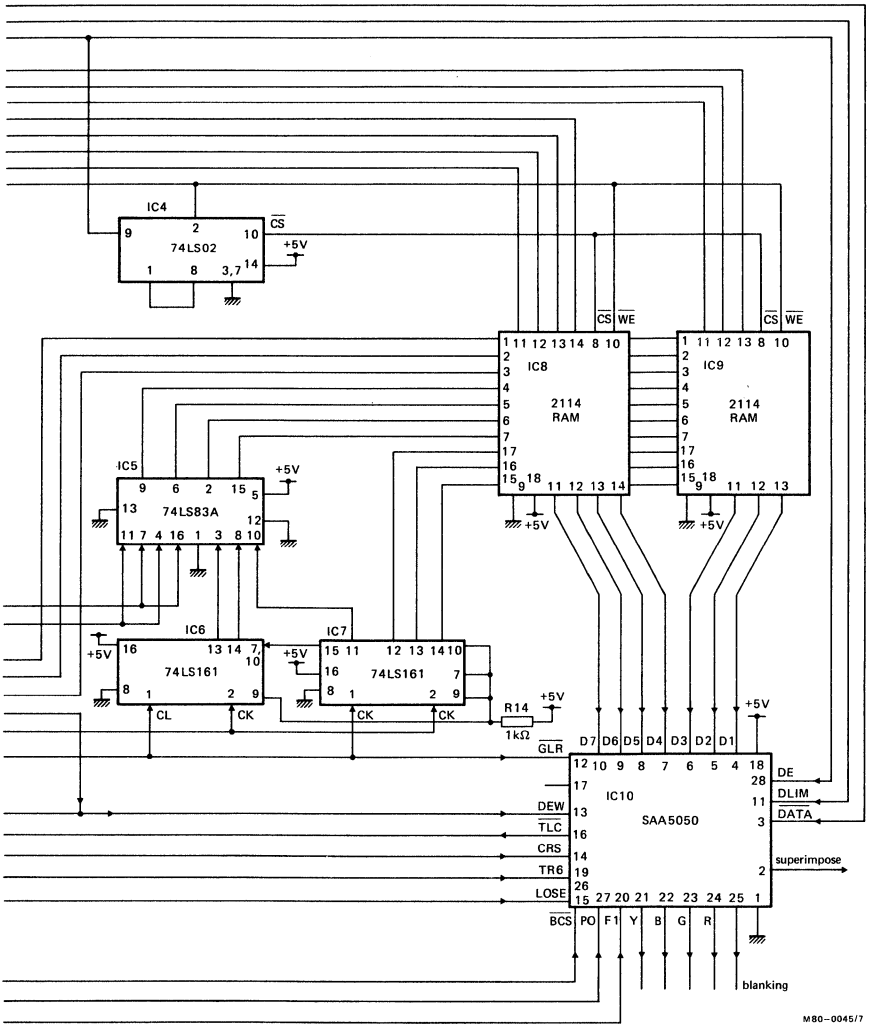


Fig.7 Typical circuit diagram of a teletext decoder.

TABLE 1 (Note 8)

Remote control commands used in the SAA5040A/SAA5040B/SAA5040C/SAA5043

CODE b_5	b_4	b_3	b_2	b_1	TELEVISION MODE ($b_7 = b_6 = 0$) (Note 7)	TELETEXT MODE ($b_7 = 1$, $b_6 = 0$) (Note 7)
0	0	0	0	0	RESET (Note 1)	
0	0	0	0	1		
0	0	0	1	0		
0	0	0	1	1	TV/ON Gives programme display.	
0	0	1	0	0	STATUS Gives programme display.	STATUS Programme/header display (Note 6)
0	0	1	0	1		HOLD Stops reception of teletext. (Note 9)
0	0	1	1	0		
0	0	1	1	1	TIME Gives time display.	DISPLAY CANCEL (Note 3)
0	1	0	0	0		
0	1	0	0	1		
0	1	0	1	0		
0	1	0	1	1		
0	1	1	0	0		TAPE Resets to small characters.
0	1	1	0	1		
0	1	1	1	0		TIMED PAGE OFF
0	1	1	1	1		TIMED PAGE ON
1	0	0	0	0	PROGRAMMES (Note 2)	NUMBERS (Notes 4 and 6) 1
1	0	0	0	1		2
1	0	0	1	0		3
1	0	0	1	1		4
1	0	1	0	0		5
1	0	1	0	1		6
1	0	1	1	0		7
1	0	1	1	1		8
1	1	0	0	0		9
1	1	0	0	1		0
1	1	0	1	0		SMALL CHARACTERS
1	1	0	1	1		LARGE CHARACTERS TOP HALF PAGE
1	1	1	0	0		LARGE CHARACTERS BOTTOM HALF PAGE
1	1	1	0	1		
1	1	1	1	0		SUPERIMPOSE (Note 6)
1	1	1	1	1		TELETEXT/ON (Note 5)

Notes for Table 1

1. Reset clears the page memory, sets page number to 100 and time code to 00.00 and resets timed page and display cancel modes.
2. Programme names are displayed for 5 s in a box at the top left of the screen in large characters. Programme commands clear the page memory except in timed page mode.

The following boxed information is displayed.

REMOTE CONTROL COMMAND b_5 b_4 b_3 b_2 b_1	SAA5040A	SAA5040B	SAA5040C	SAA5043
1 0 0 0 0	BBC1	Gives no status box	BBC1	Ch 1
1 0 0 0 1	BBC2		ITV	Ch 2
1 0 0 1 0	ITV		BBC2	Ch 3
1 0 0 1 1	4		BBC1	Ch 4
1 0 1 0 0	5		ITV	Ch 5
1 0 1 0 1	6		VTR	Ch 6
1 0 1 1 0	7		BBC1	Ch 7
1 0 1 1 1	VCR		ITV	Ch 8
1 1 0 0 0	9		BBC2	Ch 9
1 1 0 0 1	10		BBC1	Ch 0
1 1 0 1 0	11		ITV	Ch 10
1 1 0 1 1	12		VTR	Ch 11

3. Display cancel removes the text and restores the television picture. The device then reacts to any update indicator on the selected page. An updated newsflash or subtitle is displayed immediately. When an updated normal page arrives the page number only is displayed in a box at the top left of the screen. The full page of text can then be displayed when required using the teletext/on command.
4. Three number commands in sequence request a new page, and four number commands select a new time code in timed page mode. When a new page has been requested the page header turns green and the page numbers roll until the new page is captured.
5. The teletext/on command resets display cancel, hold and superimpose modes.
6. Status, timed page on, timed page off, numbers, superimpose and teletext/on commands all reset to top half page and produce a box round the header for 5 s. This allows the header to be seen if the television picture is on (e.g. newsflash or display cancel modes).
7. In viewdata mode ($b_7 = b_6 = 1$) the device is disabled and teletext cannot be received. All 3-state outputs are high impedance.
8. Table 1 shows code required for functions specified. The device requires the inverse of these codes i.e. $\overline{b_7}$ to $\overline{b_1}$. The code is transmitted serially in the following order: $\overline{b_7}$, $\overline{b_1}$, $\overline{b_2}$, $\overline{b_3}$, $\overline{b_4}$, $\overline{b_5}$, $\overline{b_6}$.
9. When hold node is selected 'HOLD' is displayed in green at the top right of the screen.
10. A 'P' is displayed before the page number at the top left of the screen (e.g. P123).

TABLE 2 (Note 9)

Remote control commands used in the SAA5041

CODE b_5 b_4 b_3 b_2 b_1	TELEVISION MODE ($b_7 = b_6 = 0$) (Note 8)	TELETEXT MODE ($b_7 = 1$, $b_6 = 0$) (Note 8)
0 0 0 0 0		
0 0 0 0 1		
0 0 0 1 0		
0 0 0 1 1		
0 0 1 0 0	TIME Gives time display.	STATUS Gives header and time display. (Note 6)
0 0 1 0 1		TIMED PAGE On/off toggle function.
0 0 1 1 0		
0 0 1 1 1		
0 1 0 0 0		
0 1 0 0 1		
0 1 0 1 0		
0 1 0 1 1		
0 1 1 0 0		
0 1 1 0 1		
0 1 1 1 0		
0 1 1 1 1		TELETEXT RESET (Note 1)
1 0 0 0 0		NUMBERS (Notes 2 and 7): 0
1 0 0 0 1		1
1 0 0 1 0		2
1 0 0 1 1		3
1 0 1 0 0		4
1 0 1 0 1	PROGRAMMES (Note 10)	5
1 0 1 1 0		6
1 0 1 1 1		7
1 1 0 0 0		8
1 1 0 0 1		9
1 1 0 1 0		SMALL CHARACTERS
1 1 0 1 1		LARGE CHARACTERS Top/bottom toggle function
1 1 1 0 0		HOLD Stops reception of teletext - toggle function (Note 3)
1 1 1 0 1		DISPLAY CANCEL (Note 4)
1 1 1 1 0		SUPERIMPOSE
1 1 1 1 1		NORMAL DISPLAY (Note 5)

Notes for Table 2

1. The teletext reset command clears the page memory, selects Page 100, goes to small characters and resets hold, timed page and display cancel modes.

2. Three number commands in sequence request a new page, and four number commands select a new time code in timed page mode. When a new page has been requested the page header turns green and the page numbers roll until the new page is captured.

3. When hold mode is selected 'HALT' is displayed in green at the top right of the screen.

4. Display cancel removes the text and restores the television picture. The SAA5041 then reacts to any update indicator on the selected page. An updated newsflash or subtitle is displayed immediately. When an updated normal page arrives the page number only is displayed in a box at the top left of the screen. The full page of text can then be displayed when required using the normal display command.

5. The normal display command resets display cancel, hold and superimpose modes.

6. Status, timed page, numbers, hold, superimpose and normal display commands all reset to top half page and produce a box round the header for five seconds. This allows the header to be seen even if the television picture is on (e.g. newsflash or display cancel modes).

7. An 'S' is displayed before the page number at the top left of the screen (e.g. S123).

8. In viewdata mode ($b_7 = b_6 = 1$) the SAA5041 is disabled and teletext cannot be received. All 3-state outputs are high impedance.

9. Table 2 shows code required for functions specified. The SAA5041 requires the inverse of these codes i.e. b_7 to b_1. The code is transmitted serially in the following order: $\overline{b_7}$, $\overline{b_1}$, $\overline{b_2}$, $\overline{b_3}$, $\overline{b_4}$, $\overline{b_5}$, $\overline{b_6}$.

10. Clear Memory occurs except in Timed Page Mode.

TABLE 3 (Note 9)

Remote control commands used in the SAA5042

CODE b_5	b_4	b_3	b_2	b_1	TELEVISION MODE ($b_7 = b_6 = 0$) (Note 8)	TELETEXT MODE ($b_7 = 1$, $b_6 = 0$) (Note 8)
0	0	0	0	0	RESET (Note 1)	
0	0	0	0	1		
0	0	0	1	0		
0	0	0	1	1		
0	0	1	0	0		STATUS Gives header and time display. (Note 6)
0	0	1	0	1		HOLD Stops reception of teletext - toggle function (Note 3)
0	0	1	1	0		
0	0	1	1	1	TIME Gives time display	
0	1	0	0	0		
0	1	0	0	1		
0	1	0	1	0		SMALL CHARACTERS
0	1	0	1	1		
0	1	1	0	0		LARGE CHARACTERS TOP HALF PAGE
0	1	1	0	1		LARGE CHARACTERS BOTTOM HALF PAGE
0	1	1	1	0		DISPLAY CANCEL/RECALL (Note 4)
0	1	1	1	1		DISPLAY RECALL
1	0	0	0	0		0
1	0	0	0	1		1
1	0	0	1	0		2
1	0	0	1	1		3
1	0	1	0	0		4
1	0	1	0	1	PROGRAMMES (Note 10)	NUMBERS (Notes 2 and 7) 5
1	0	1	1	0		6
1	0	1	1	1		7
1	1	0	0	0		8
1	1	0	0	1		9
1	1	0	1	0		TIMED PAGE On/Off toggle function
1	1	0	1	1		CLEAR MEMORY
1	1	1	0	0		LONG TERM STORE/SMALL CHARACTERS
1	1	1	0	1		
1	1	1	1	0		SUPERIMPOSE
1	1	1	1	1		TELETEXT/ON (Note 5)

Notes for Table 3

1. Reset clears the page memory, sets page number to 100 and time code to 00.00 and resets timed page and display cancel modes.

2. Three number commands in sequence request a new page, and four number commands select a new time code in timed page mode. When a new page has been requested the page header turns green and the page numbers roll until the new page is captured.

3. When hold mode is selected 'STOP' is displayed in green at the top right of the screen.

4. Display cancel/recall removes the text and restores the television picture. The SAA5042 then reacts to any update indicator on the selected page. An updated newsflash or subtitle is displayed immediately. When an updated normal page arrives the page number only is displayed in a box at the top left of the screen. The same command will then cause a normal page to be displayed, but will cancel a newsflash or subtitle page. Alternatively, text can be recalled by using the teletext/on command.

5. The teletext/on command resets display cancel, hold and superimpose modes.

6. Status, timed page, numbers, superimpose and teletext/on commands all reset to top half page and produce a box round the header for five seconds. This allows the header to be seen even if the television picture is on (e.g. newsflash or display cancel modes).

7. A 'P' is displayed before the page number at the top left of the screen (e.g. P123).

8. In viewdata mode ($b_7 = b_6 = 1$) the SAA5042 is disabled and teletext cannot be received. All 3-state outputs are high impedance.

9. Table 3 shows code required for functions specified. The SAA5042 requires the inverse of these codes i.e. $\overline{b_7}$ to $\overline{b_1}$. The code is transmitted serially in the following order: $\overline{b_7}$, $\overline{b_1}$, $\overline{b_2}$, $\overline{b_3}$, $\overline{b_4}$, $\overline{b_5}$, $\overline{b_6}$.

10. Clear Memory occurs except in Timed Page Mode.

GEARING AND ADDRESS LOGIC ARRAY FOR USA TELETEXT (GALA)

GENERAL DESCRIPTION

The SAA5045 is a PCF0700 CMOS process gate array designed to interface the SAA5040B Teletext Acquisition Control (TAC) IC to the SAA5030 Video Processor (VIP) data output for modified U.K. standard 525-line Teletext. It also provides an address interface between SAA5040B, SAA5025D Teletext Timing Chain for USA 525 line system (USTIC) and the page memory RAM. The memory interface includes read/write control compatible with the geared 32 + 8 transmission system at 5,727272 MHz data rate employed in the modified U.K. system.

For RATINGS and CHARACTERISTICS see data sheet: CMOS GATE ARRAYS (PCF0700).

SYSTEM CONTENT

Functionally the chip contains two main sections which operate during the acquisition and display periods.

Gearing control section

The data from the SAA5030 (VIP) and data clock, are processed to detect the presence of the gearing bit and convert the data for correct operation of the SAA5040B (TAC). Data and clock outputs to the TAC are internally compensated for processing delays, so that correct clocking-in of data is ensured.

Addressing section

Column counters are included, which operate from the WACK (TAC) and RACK (USTIC) column clock signals during acquisition and display respectively.

Five row-address input circuits (pins A0 to A4) are provided for (TAC) and (USTIC) address outputs. These are multiplexed with the column address from the internal counters for correct mapping of the RAM via ten output address pins (AA0 to AA9). During acquisition, the multiplexer is controlled by the gearing bit detection to give correct assembly of the 40 character per row page structure.

The address output buffers are 3-state devices controlled by the line reset signal (pin 8; $\overline{\text{GLRS}}$). During the horizontal flyback period the address pins are 3-state to allow alternative addressing for customized applications.

Read/write control to RAM

An internal counter prevents overwriting if more than 32 character WOK pulses are received from TAC due to poor transmission conditions. Two control outputs, one for read/write ($\overline{\text{WE}}$) and the other for chip select ($\overline{\text{CS}}$), are provided to eliminate conflicts on the input/output RAM bus.

PACKAGE OUTLINE

28-lead DIL; plastic (SOT-117D).

SYSTEM CURRENT (continued)

Framing code detection

When a valid data line is received and the framing code is detected in the gearing section, then flag pulses (pair of pulses) are available at output $\overline{WE}$, before the $\overline{CS}$ output is driven LOW for normal writting into the RAM. If a framing-code-present signal is required, it can be obtained by gating $\overline{WE}$ and $\overline{CS}$ outputs such, that an output from the $\overline{WE}$, when output $\overline{CS}$ is HIGH, indicates the detection of a framing code; N.B., each framing code produces a pair of pulses.

RAM ADDRESS CONTROL

Figure 2 shows that the ten RAM address outputs are controlled by a multiplexer (MUX3), which interchanges the two groups of five address lines, when a gearing bit equal to logic "1" is received during data input. During display, MUX3 is switched by bit number 6 of the column counter. MUX1, which is switched by the gearing bit, controls stepping of the row address when fill-in rows are received. MUX2 is switched by either the gearing bit or bit 6 of the column counter to access the part of RAM storing the last eight bytes of each row of data.

The mapping of the 1024-byte RAM is shown in Fig. 1. Area "A" stores data corresponding to the left-hand side (32 bytes wide) of the display whilst area "B" stores the remainder for the right-hand side.

Access to the RAM for custom operations can be made during the time that $\overline{GLRS}$ (pin 8) is LOW, which causes all ten address buffers to be in the open state. It should be noted that $\overline{GLRS}$ LOW also resets the column counters and the gearing-bit detection system to logic "0". This normally occurs during the horizontal interval (between 5 and 8 μs) after the horizontal sync pulse falling edge.

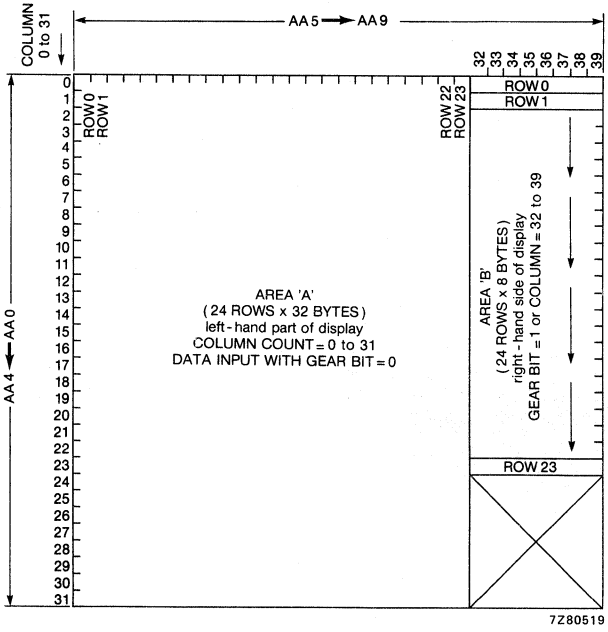


Fig. 1 Memory map for the SAA5045 address system.

DEVELOPMENT DATA

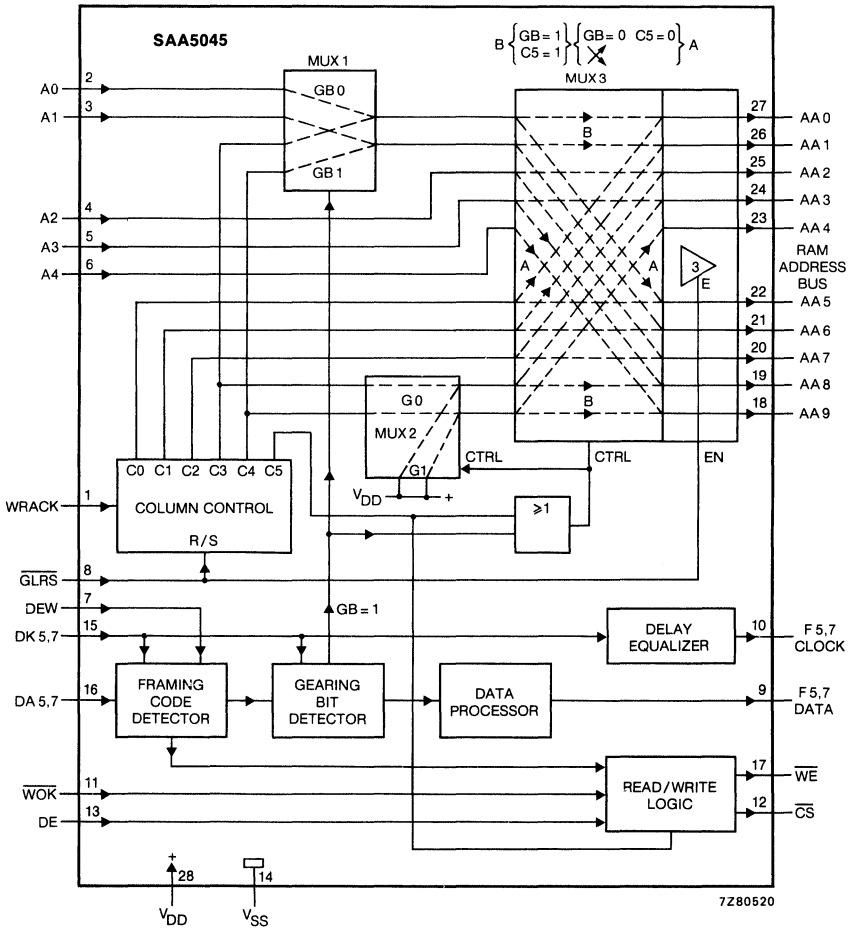


Fig. 2 Block diagram.

PIN DESCRIPTION

pin no.	symbol	name and function
1	WRACK	input clock to column counter
2	A0	row address system inputs
3	A1	
4	A2	
5	A3	
6	A4	
7	DEW	data entry window input
8	$\overline{\text{GLRS}}$	general line reset starting output
9	F5,7 DATA	5,7 MHz data output
10	F5,7 CLOCK	5,7 MHz clock output
11	$\overline{\text{WOK}}$	write enable input
12	$\overline{\text{CS}}$	chip select output
13	DE	display enable input
14	V_{SS}	ground
15	DK5,7	5,7 MHz data clock input
16	DA5,7	5,7 MHz data input
17	$\overline{\text{WE}}$	write enable output
18	AA9	memory address outputs
19	AA8	
20	AA7	
21	AA6	
22	AA5	
23	AA4	
24	AA3	
25	AA2	
26	AA1	
27	AA0	
28	V_{DD}	positive supply (+ 4,5 V to + 5,5 V)

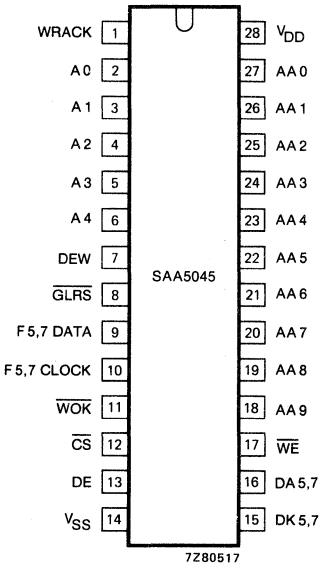


Fig. 3 Pin configuration.

APPLICATION INFORMATION

The function is described against the corresponding pin number.

1. WRACK – input clock to column counter

Input clock to column counter during data input or display; WACK from SAA5040B (TAC) or RACK from SAA5025D (USTIC).

2 to 6. A0 to A4 – row address system inputs

Inputs to row address system during data input or display. Row address numbers greater than 0 to 23 disable writing to the RAM during input.

7. DEW – data entry window input

Data entry window input enables gearing bit detection and data processing part of system.

8. $\overline{\text{GLRS}}$ – general line reset starting output

Input from the SAA5025D is a negative reset pulse at line rate for column counters and gearing system. When this input is LOW, it opens 3-state address buffers.

9. F5,7 DATA – 5,7 MHz data output

Data output at 5,7 MHz rate to SAA5040B (TAC) during the data acquisition period when DEW is HIGH.

10. F5,7 CLOCK – 5,7 MHz clock output

Data clock output at 5,7 MHz rate to SAA5040B (TAC), synchronized to data at pin 9 (F5,7 DATA).

11. $\overline{\text{WOK}}$ – write enable input

Write enable input from SAA5040B (TAC) during data acquisition, when correct data is received, for RAM write/read control (via output $\overline{\text{WE}}$; pin 17).

12. $\overline{\text{CS}}$ – chip select output

Output to drive the RAM chip enable during data input and display periods controlled by the display enable output (DE) and write O.K. ($\overline{\text{WOK}}$) output of the SAA5040B (TAC), avoiding input/output bus conflict.

13. DE – display enable input

Display enable input from SAA5040B (TAC) to control $\overline{\text{CS}}$.

14. V_{SS} – ground

15. DK5,7 – 5,7 MHz data clock input

Data clock input at 5,7 MHz rate from the SAA5030 (VIP); this pin is capacitively coupled with a d.c. restoring diode and is externally connected to V_{SS}.

16. DA5,7 – 5,7 MHz data input

Data input at 5,7 MHz rate from SAA5030 (VIP); this pin is capacitively coupled with a d.c. restoring diode and is externally connected to V_{SS}.

17. $\overline{\text{WE}}$ – write enable output

Write enable output to control RAM write/read. This output is the gated and delay version of the $\overline{\text{WOK}}$ from the SAA5040B, but limited to 32 pulses which are possible before the WACK count is equal to 32.
A pair of pulses on this output precedes the $\overline{\text{WOK}}$ pulses, whilst $\overline{\text{CS}}$ is HIGH whenever a framing code is detected.

APPLICATION INFORMATION (continued)

18 to 27. AA9 to AA0 – memory address outputs

Memory address outputs; 3-state buffered outputs, open when $\overline{\text{GLRS}}$ is LOW for auxiliary access to the RAM address bus if required.

N.B.: AA9 and AA8 are simultaneously HIGH whenever a gear bit with logic "1" is received during DEW is HIGH. This enables detection of gearing bit reception, following $\overline{\text{GLRS}}$ reset on each line, which always resets AA0 to AA9 to logic "0".

28. V_{DD} – positive supply (4,5 V to 5,5 V)

Note

Input pins other than 15 and 16 have internal 15 kΩ pull-up resistors for compatibility with SAA5025D and SAA5040B output signal ranges. Pins 15 and 16 are CMOS inputs for d.c. restored drive from the SAA5030 (VIP) clock and data output signals.

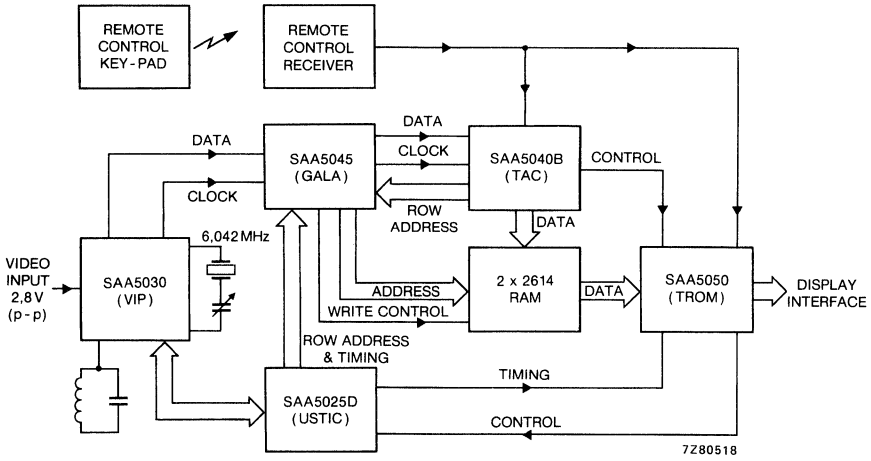


Fig. 4 Schematic diagram of the 5-chip decoder.

DEVELOPMENT DATA

TELETEXT CHARACTER GENERATOR

The SAA5050 series of MOS N-channel integrated circuits provides the video drive signals to the television receiver necessary to produce the teletext/viewdata display. The variants are described in the Quick Reference Data and full details of the characters sets are given in Figs. 11 to 18.

QUICK REFERENCE DATA

Supply voltage	V_{DD}	nom.	5	V
Supply current	I_{DD}	typ.	85	mA
Operating ambient temperature range	T_{amb}		−20 to +70	°C

Variant	Character set	Variant	Character set
5050	English	5054	Belgian
5051	German	5055	US ASCII
5052	Swedish	5056	Hebrew
5053	Italian	5057	Cyrillic

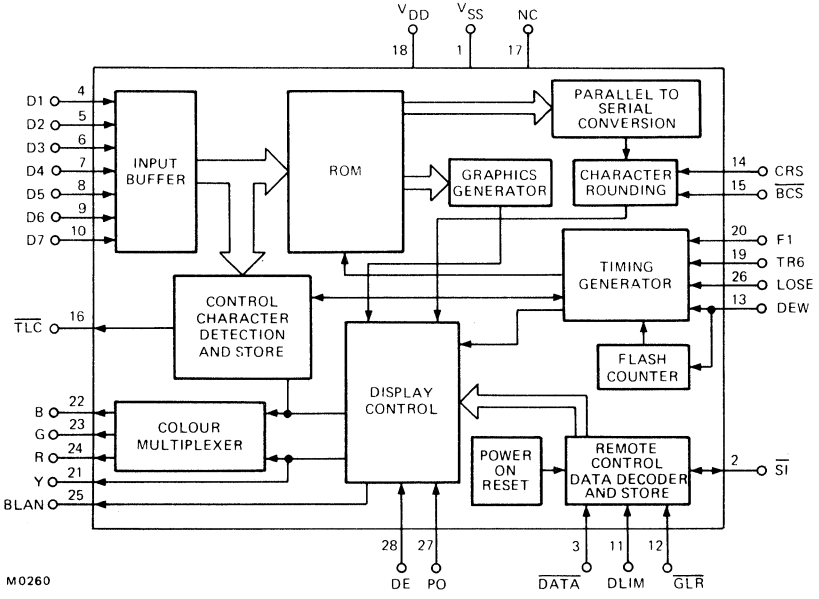


Fig.1 Block diagram

PACKAGE OUTLINE

28-lead DIL; plastic (SOT-117).

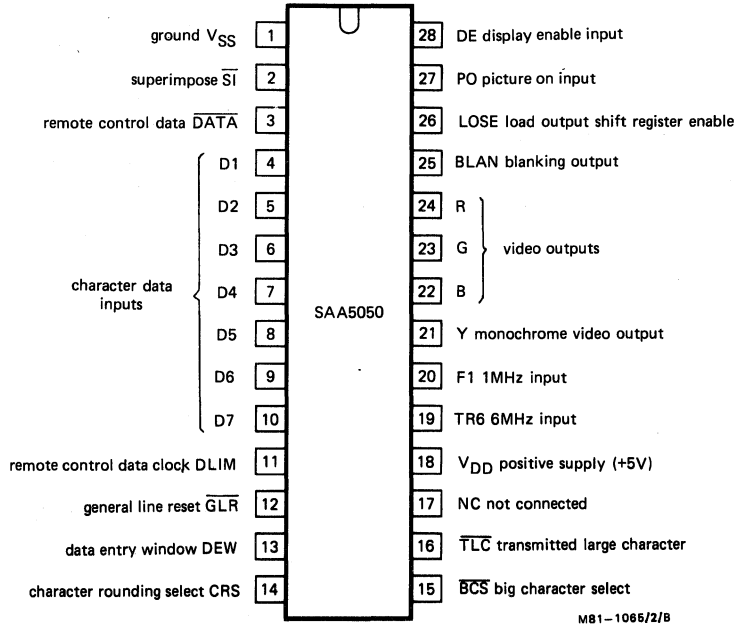


Fig.2 Pinning diagram

DESCRIPTION

The SAA5050 is a 28 pin device which incorporates a fast access character generator ROM (4.3 k bits), the logic decoding for all the teletext control characters and decoding for some of the remote control functions. The circuit generates 96 alphanumeric and 64 graphic characters. In addition there are 32 control characters which determine the nature of the display.

The SAA5050 is suitable for direct connection to the SAA5010, SAA5012, SAA5020 and SAA5040 Series integrated circuits.

The basic input to the SAA5050 is the character data from the teletext page memory. This is a 7 bit code. Each character code defines a dot matrix pattern. The character period is 1 μs and the character dot rate is 6 MHz. The timings are derived from the two external input clocks F1 (1 MHz) and TR6 (6 MHz) which are amplified and re-synchronised internally. Each character rectangle is 6 dots wide by 10 TV lines high. One dot space is left between adjacent characters, and there is one line space left between rows. Alphanumeric characters are generated on a 5 x 9 matrix, allowing space for descending characters. Each of the 64 graphic characters is decoded to form a 2 x 3 block arrangement which occupies the complete 6 x 10 dot matrix (Fig.9). Graphics characters may be either contiguous or separated (Fig.10). The alphanumeric characters are character rounded, i.e. a half dot is inserted before or after a whole dot in the presence of a diagonal in a character matrix.

The character video output signals comprise a monochrome signal and RGB signals for a colour receiver. A blanking output signal is provided to blank out the television video signal under the control of the PO and DE inputs and the box control characters (see Table 3).

The monochrome data signal can be used to inlay characters into the television video. The use of the 32 control characters provides information on the nature of the display, e.g. colour. These are also used to provide other facilities such as 'concealed display' and flashing words etc. The full character set is given in Table 1.

HANDLING

Inputs and outputs are protected against electrostatic charge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (See 'Handling MOS Devices').

RATINGS Limiting values in accordance with the Absolute Maximum System, (IEC134)

		min.	typ.	max.	
Voltages (with respect to pin 1)					
Supply voltage (pin 18)	V_{DD}	−0.3	–	7.5	V
Input voltages (all inputs + input/output)	V_I	−0.3	–	7.5	V
Output voltage (pin 16)	V_{O16}	−0.3	–	7.5	V
(all other outputs)	V_O	−0.3	–	14.0	V
Temperature					
Storage temperature range	T_{stg}		−20 to +125		°C
Operating ambient temperature range	T_{amb}		−20 to +70		°C

CHARACTERISTICS

		min.	typ.	max.	
Supply voltage (pin 18)	V_{DD}	4.5	–	5.5	V
The following parameters apply at T_{amb} = 25 °C and V_{DD} = 5 V unless otherwise stated.					
Supply current	I_{DD}	–	85	160	mA
Inputs					
Character data D1 to D7 (pins 4 to 10)					
Input voltage; HIGH	V_{IH}	2.65	–	V_{DD}	V
Input voltage; LOW	V_{IL}	0	–	0.6	V
Clock inputs F1 (pin 20) **TR6** (pin 19)					
Input voltage; HIGH	V_{IH}	2.65	–	V_{DD}	V
Input voltage; LOW	V_{IL}	0	–	0.6	V
Logic inputs					
$\overline{\text{DATA}}$ (pin 3) DEW (pin 13) LOSE (pin 26) DLIM (pin 11) CRS (pin 14) PO (pin 27) $\overline{\text{GLR}}$ (pin 12) $\overline{\text{BCS}}$ (pin 15) DE (pin 28)					
Input voltage; HIGH	V_{IH}	2.0	–	V_{DD}	V
Input voltage; LOW	V_{IL}	0	–	0.8	V
All inputs					
Input leakage current (V_I = 5.5 V)	I_{IR}	–	–	10	μA
Input capacitance	C_I	–	–	7	pF

CHARACTERISTICS (continued)

			min.	typ.	max.	
Outputs						
Character video outputs + Blanking output (open drain) (note 3)						
B – (pin 22), G – (pin 23), R – (pin 24), Y – (pin 21), Blanking (pin 25)						
Output voltage; LOW (I_{OL} = 2 mA)		V_{OL}	–	–	0.5	V
Output voltage; LOW (I_{OL} = 4 mA)		V_{OL}	–	–	1.0	V
→ Output voltage; HIGH (note 5)		V_{OH}	V_{DD}	–	13.2	V
Output load capacitance		C_L	–	–	15	pF
Output fall time	note 1	t_f	–	–	30	ns
Variation of fall time between any outputs	note 1	Δt_f	0	–	20	ns
$\overline{\text{TLC}}$ (pin 16)						
Output voltage; LOW (I_{OL} = 100 μA)		V_{OL}	0	–	0.5	V
Output voltage; HIGH ($-I_{OH}$ = 100 μA)		V_{OH}	2.4	–	V_{DD}	V
Output load capacitance		C_L	–	–	30	pF
Output rise time	Measured between 0.8 V and 2.0 V levels	t_r	–	–	1.0	μs
Output fall time	Measured between 0.8 V and 2.0 V levels	t_f	–	–	1.0	μs
Input/output						
$\overline{\text{SI}}$ (pin 2) (open drain)						
Input voltage; HIGH		V_{IH}	2.0	–	6.5	V
Input voltage; LOW		V_{IL}	0	–	0.8	V
Input leakage current (V_I = 5.5 V)		I_{IR}	–	–	10	μA
Input capacitance		C_I	–	–	7	pF
Output voltage; LOW (I_{OL} = 0.4 mA)		V_{OL}	0	–	0.5	V
Output voltage; LOW (I_{OL} = 1.3 mA)		V_{OL}	0	–	1.0	V
Output load capacitance		C_L	–	–	45	pF
Output voltage; HIGH state (note 2)		V_{OH}	–	–	6.5	V

Timing characteristics

For typical display of 40 characters per line. Line rate = 64 μs. Field rate = 20 ms.

Character data timing (Fig.4)

			min.	typ.	max.	
TR6 rising edge to F1 falling edge		t_D	6	–	60	ns
TR6 frequency		f_{TR6}	–	6	–	MHz
TR6 mark/space ratio			40:60	–	60:40	
F1 frequency		f_{F1}	–	1	–	MHz
F1 mark/space ratio			40:60	–	60:40	
Data set-up time		t_{CDS}	80	–	–	ns
Data hold time		t_{CDH}	100	–	–	ns
Delay time – character in/ character data at outputs	Graphics	t_{CDG}	–	2.6	–	μs
	Alphanumerics	t_{CDA}	–	2.767	–	μs

Display period timing (Fig.5)

F1 falling edge to LOSE rising edge	t_{LDH}	0	–	250	ns
F1 falling edge to LOSE falling edge	t_{LDL}	0	–	250	ns
LOSE rising edge to 'Display on'	t_{DON}	–	2.6	–	μs
LOSE falling edge to 'Display off'	t_{DOFF}	–	2.6	–	μs
'Display period'	t_{DP}	–	40	–	μs

Line rate timing (Fig.6)

F1 rising edge to GLR falling edge	t_{DGL}	0	–	200	ns
F1 rising edge to GLR rising edge	t_{DGH}	0	–	200	ns
GLR LOW time	t_{GLP}	–	1	–	μs
Line start* to GLR falling edge	t_{GLR}	–	5	–	μs
Line start* to LOSE rising edge	t_{LSL}	–	14.5	–	μs
LOSE falling edge to Line start*	t_{LLS}	–	9.5	–	μs
Line period	t_{LNP}	–	64	–	μs
LOSE HIGH time	t_{LHP}	–	40	–	μs

Remote data input timing (Fig.8)

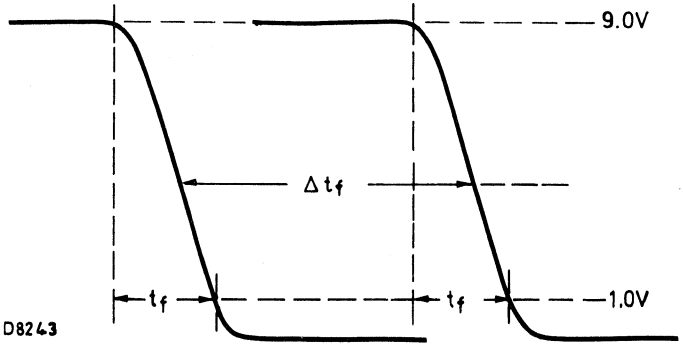
Assuming F1 period = 1 μs and GLR period = 64 μs

DLIM clock HIGH time	t_{CH}	6.5	8	(note 4)	μs
$\overline{\text{DLIM}}$ clock LOW time	t_{CL}	3.5	8	60	μs
DATA to $\overline{\text{DLIM}}$ set-up time	t_{DS}	0	14	–	μs
$\overline{\text{DLIM}}$ to $\overline{\text{DATA}}$ hold time	t_{DH}	8	14	–	μs

*Taken as falling edge of 'line sync' pulse.

Notes to characteristics

1. Fall time, t_f and Δt_f, are defined as shown and are measured using the circuit shown below:
   t_f is measured between the 9 V and 1 V levels.
   Δt_f is the maximum time difference between outputs.



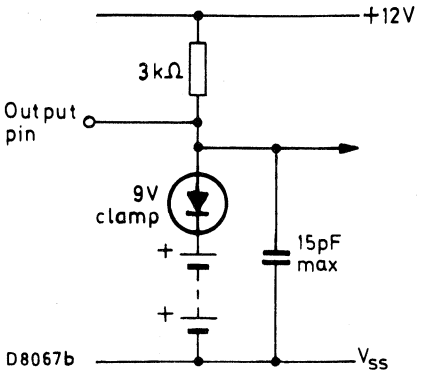


Fig.3

2. Recommended pull-up resistor for $\overline{SI}$ is 18 kΩ.
3. The R, G, B, Y and blanking outputs are protected against short circuit to supply rails.
4. There is no maximum DLIM cycle time, provided the DLIM duty cycle is such that the $t_{CL\,max}$ requirement is not exceeded.
5. With maximum pull-up voltage applied to R, G, B and BLAN outputs the leakage current will not exceed 20 μA with the outputs in the OFF state.

SPECIAL FEATURES

Flash oscillator

The circuit generates a 0.75 Hz signal with a 3:1 ON/OFF ratio to provide the flashing character facility.

Power-on-reset

When the supply voltage is switched on, the character generator will reset to tv, conceal, and not superimpose modes.

Character rounding

The character rounding function is different for the small and double height characters. In both cases the ROM is accessed twice during the character period of 1 μs. The dot information of two rows is then compared to detect the presence of any diagonal in the character matrix and to determine the positioning of the character rounding half dots.
For small characters rounding is always referenced in the same direction (i.e. row before in even fields and row after in odd fields as determined by the CRS signal).
For double height characters rounding is always referenced alternately up and down changing every line using an internally generated signal. (The CRS signal is '0' for the odd field and '1' for the even field of an interlaced tv picture).

Graphics decoder

The 64 graphics characters are decoded directly from the character data inputs and they appear on a 2 x 3 matrix. Figure 9 gives details of the graphics decoding.

APPLICATION DATA

The function is quoted against the corresponding pin numbers

Pin No.

1. **V_{SS} Ground** - 0 V

2. **$\overline{SI}$ Superimpose**

   This is a dual purpose input/output pin. The output is an open drain transistor (capable of sinking current to V_{SS}), which is in the conducting state when superimpose mode is selected. This allows contrast reduction of the tv picture in superimpose mode if required. If the pin is held LOW, the internal 'tv mode' flip-flop is held in the 'text' state. This is for VDU applications when the remote control is not used.

3. **$\overline{DATA}$ Remote control data**

   This input accepts a 7-bit serial data stream from the remote control decoder. This data contains the teletext and viewdata remote control functions. The nominal data rate is 32 μs/bit. The command codes used in the SAA5050 are shown in Table 2.

4,5,6 7,8,9, 10 **D1 to D7 Character data**

These inputs accept a 7-bit parallel data code from the page memory. This data selects the alphanumeric characters, the graphics characters and the control characters. The alphanumeric addresses are ROM column addresses, the graphics and control data are decoded internally.

11. **DLIM**

   This input receives a clock signal from the remote control decoder and this signal is used to clock remote control data into the SAA5050. The positive-going edge of every second clock pulse is nominally in the centre of each remote control data bit (Fig.8).

12 **GLR General line reset**

   This input signal from the SAA5020 Timing Chain is required for internal synchronisation of remote control data signals.

13. **DEW Data entry window**

   This input signal from the SAA5020 Timing Chain is required to reset the internal ROM row address counter prior to the display period. It is also used internally to derive the 'flash' period.

APPLICATION DATA (continued)

14. **CRS Character rounding select**

This input signal from the SAA5020 Timing Chain is required for correct character rounding of displayed characters. (Normal height characters only).

15. **$\overline{BCS}$ Big character select**

This input from the SAA5040 Teletext Acquisition and Control device allows selection of large characters by remote control.

16. **$\overline{TLC}$ Transmitted large characters**

This output to the SAA5020 Timing Chain enables double height characters to be displayed as a result of control characters stored in the page memory.

18. **V_{DD} + 5 V supply**

This is the power supply input to the circuit.

19. **TR6**

This input is a 6 MHz signal from the SAA5020 Timing Chain used as a character dot rate clock.

20. **F1**

This input is a 1 MHz equal mark/space ratio signal from the SAA5020 Timing Chain. It is used to latch the 7-bit parallel character data into the input latches. It is also used to synchronise an internal divide-by 6 counter. The F1 signal is internally synchronised with TR6.

21. **Y Output**

This is a video output signal which is active in the HIGH state containing character dot information for tv display.
The output is an open drain transistor capable of sinking current to V_{SS}

22,23, 24. **B,G,R outputs**

These are the Blue, Green and Red Character video outputs to the tv display circuits. They are active HIGH and contain both character and background colour information.
The outputs are open drain transistors capable of sinking current to V_{SS}.

25. **BLAN Blanking**

This active HIGH output signal provides tv picture video blanking. It is active for the duration of a box when Picture On and Display Enable are HIGH. It is also activated permanently for normal teletext display when no tv picture is required (PO LOW). The output is an open drain transistor capable of sinking current to V_{SS}. Full details given in Table 3.

26. **LOSE Load output shift register enable**

This input signal from the SAA5020 Timing Chain resets the internal control character flip-flops prior to the start of each display line.
This signal also defines the character display period.

27. **PO Picture On**

This input signal from the SAA5040 Teletext Acquisition and Control device is used to control the character video and blanking outputs. When PO is HIGH, only text in boxes is displayed unless in superimpose mode. The input is HIGH for tv picture video on, LOW for picture off. See Table 3.

28. **DE Display enable**

This input signal from the SAA5040 Teletext Acquisition and Control device is used to enable the teletext display. The input is HIGH for teletext display enabled. LOW for display cancelled. See Table 3.

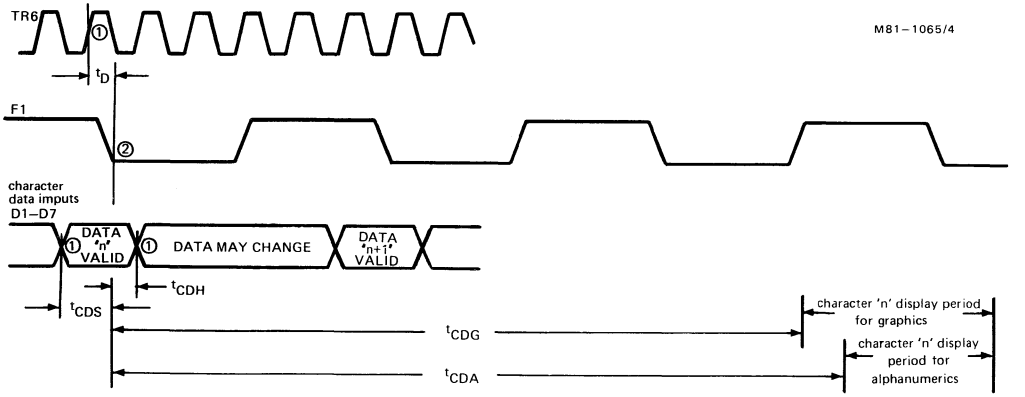


Fig.4 Character data timing (for typical 40 character display)

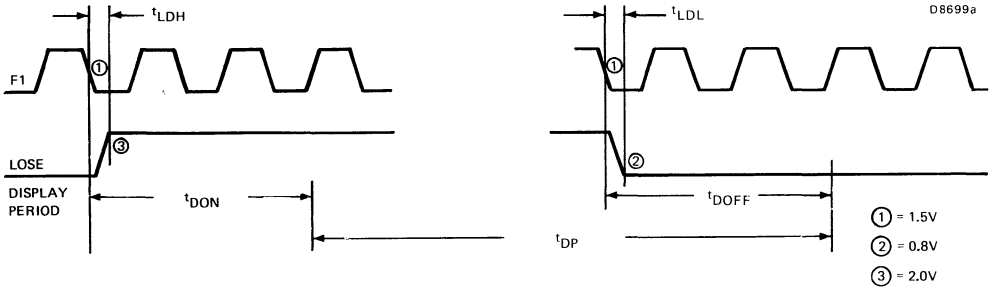


Fig.5 Display period timing (for typical 40 character display)

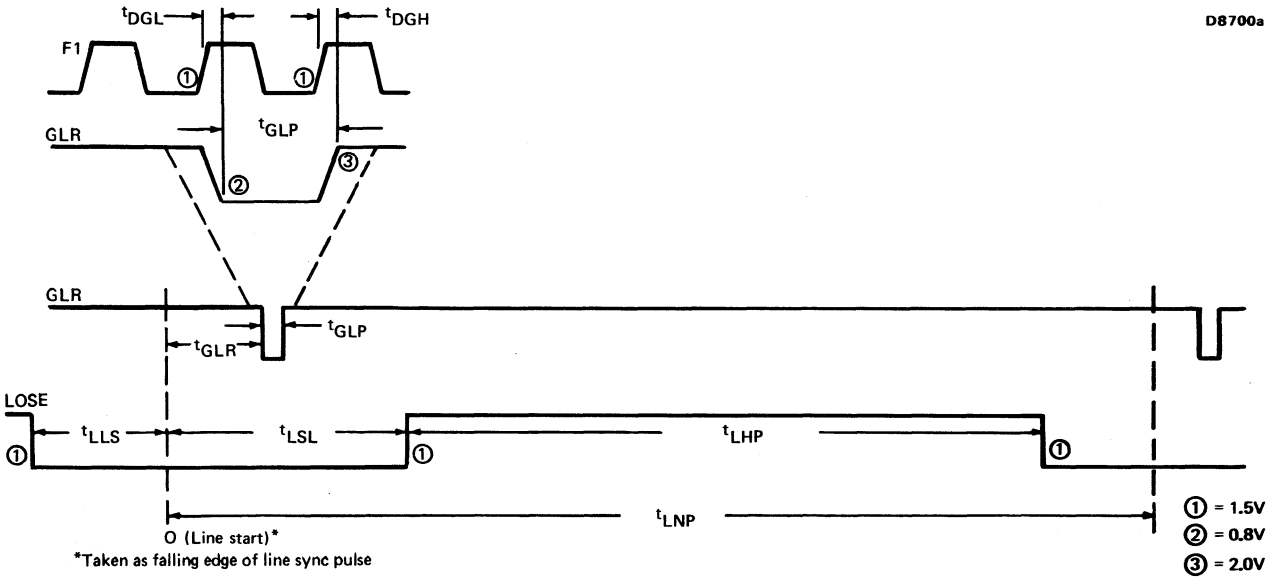


Fig.6 Line rate clocks (for line period of 64 μs)

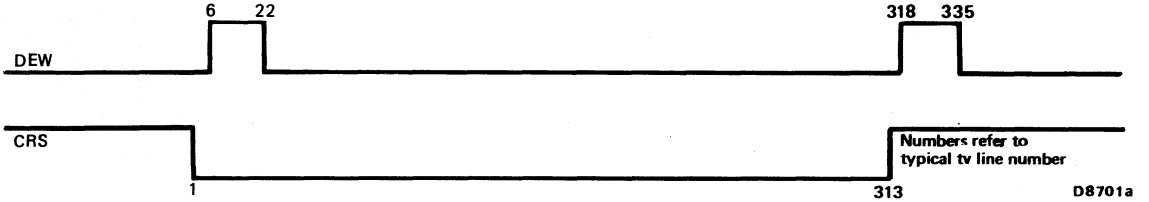


Fig.7 Field rate clocks (for field period of 20 ms, 312½ lines per field)

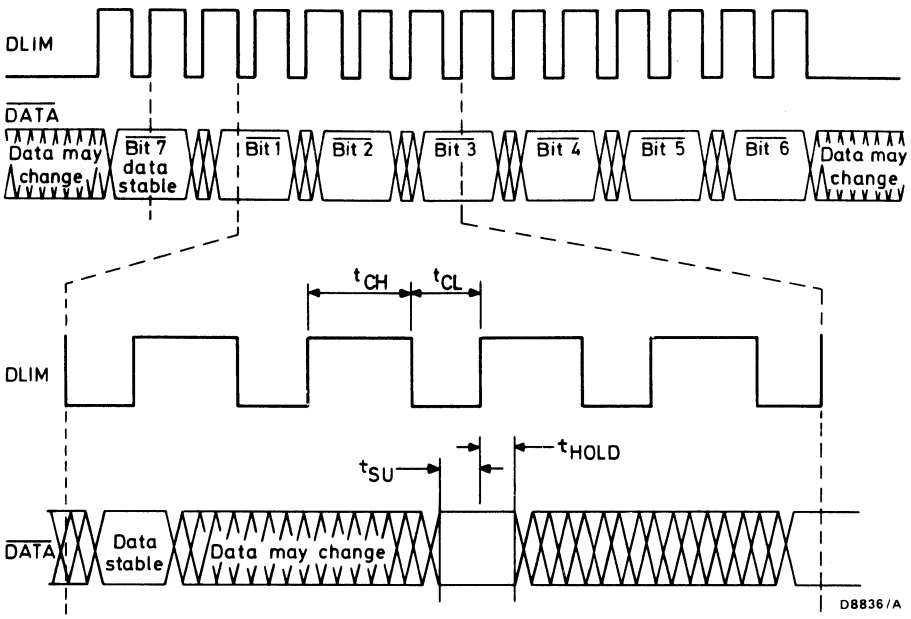
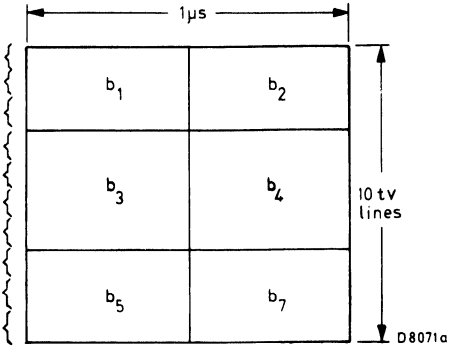


Fig.8 Remote control input timing



Each cell is illuminated if particular 'bit' (b_1, b_2, b_3, b_4, b_5, or b_7) is a '1'.
For graphics characters b_6 is always a '1' – See Table 1.

Fig.9 Graphics Character

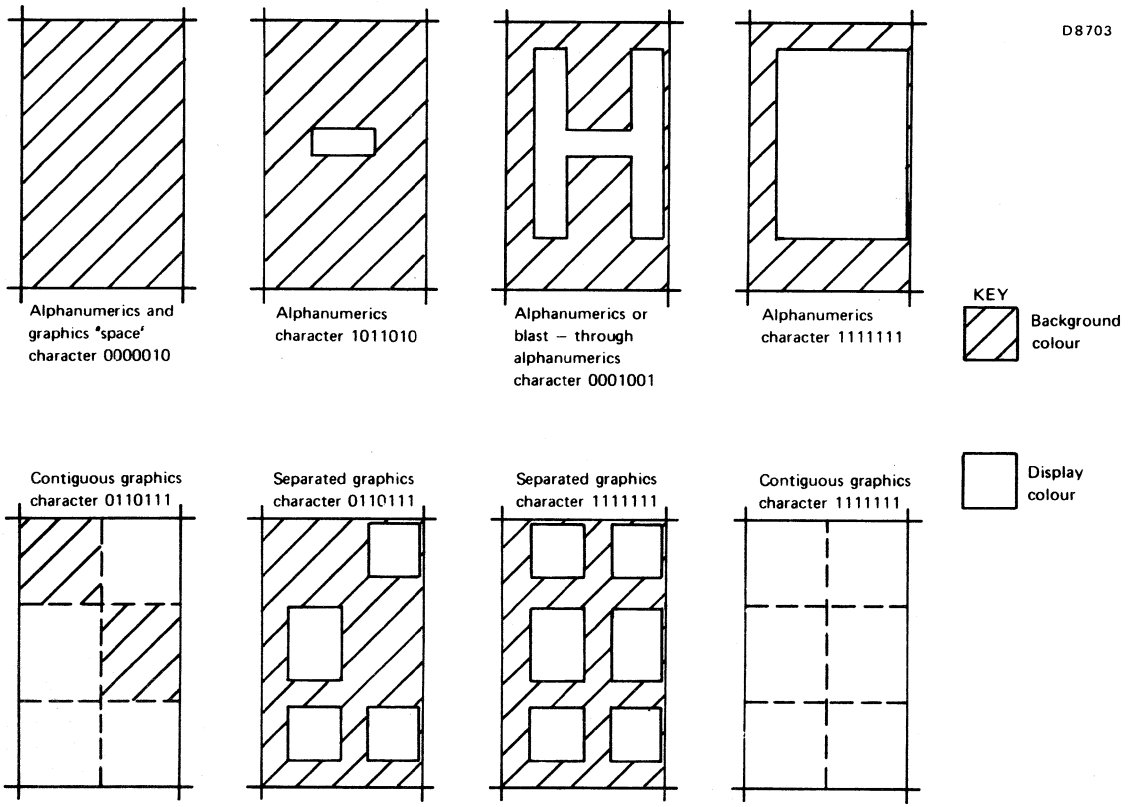


Fig.10 Character format

TABLE 1

Character data input decoding

D8068a

Bits b_7 b_6 b_5 / Col →	0_0	0_1	1_0	1_1	0_0	0_1	1_0	1_1	0_0	0_1	1_0	1_1	0_0	0_1	1_0	1_1
b_4 b_3 b_2 b_1 / Row ↓	0	1	2	2a	3	3a	4	5	6	6a	7	7a				
0 0 0 0	0	NUL *	DLE *			0		@	P			p				
0 0 0 1	1	Alpha^n Red	Graphics Red	!		1		A	Q	a		q				
0 0 1 0	2	Alpha^n Green	Graphics Green	"		2		B	R	b		r				
0 0 1 1	3	Alpha^n Yellow	Graphics Yellow	£		3		C	S	c		s				
0 1 0 0	4	Alpha^n Blue	Graphics Blue	$		4		D	T	d		t				
0 1 0 1	5	Alpha^n Magenta	Graphics Magenta	%		5		E	U	e		u				
0 1 1 0	6	Alpha^n Cyan	Graphics Cyan	&		6		F	V	f		v				
0 1 1 1	7	Alpha^n ** White	Graphics White	'		7		G	W	g		w				
1 0 0 0	8	Flash	Conceal Display	(		8		H	X	h		x				
1 0 0 1	9	** Steady	** Contiguous Graphics	)		9		I	Y	i		y				
1 0 1 0	10	** End Box	Separated Graphics	*		:		J	Z	j		z				
1 0 1 1	11	Start Box	* ESC	+		;		K	←	k		¼				
1 1 0 0	12	** Normal Height	** Black Background	,		<		L	½	l		‖				
1 1 0 1	13	Double Height	New Background	-		=		M	→	m		¾				
1 1 1 0	14	* SO	Hold Graphics	.		>		N	↑	n		÷				
1 1 1 1	15	* S1	** Release Graphics	/		?		O	#	o		■				

Control characters shown in columns 0 and 1 are normally displayed as spaces.
The SAA5050 character set is shown as example. Details of character sets are given in Figs. 11 to 18.

* These control characters are reserved for compatability with other data codes.

** These control characters are presumed before each row begins.

Codes may be refered to by their column and row e.g. 2/5 refers to %

Character rectangle

Black represents display colour.

White represents background.

TABLE 2

Remote control command codes used in the SAA5050

CODE b_7	b_6	b_5	b_4	b_3	b_2	b_1	COMMAND	FUNCTION
0	X	X	X	X	X	X	'tv' mode	Allows text on top row of display only.
1	X	X	X	X	X	X	'Text' mode	Allows text throughout display period.
1	0	1	1	1	1	0	Superimpose	Sets Superimpose mode.
1	0	1	1	1	1	1	teletext	Resets Superimpose mode.
0	X	X	X	X	X	X	'tv' mode	Resets Superimpose mode.
1	1	X	X	X	X	X	viewdata mode	Resets Superimpose mode;
1	X	0	0	1	1	0	Reveal	Reveals for time-out (notes 3, 4).
1	X	0	1	0	1	1	Reveal set	Sets Reveal mode (note 3).
Any command apart from reveal set.								Resets Reveal mode (note 3)

X = Don't care.

Notes

1. When the power is applied the SAA5050 is set into the 'tv' mode and reset out of Superimpose and Reveal modes.
2. 'Text' mode is selected when $\overline{SI}$ (pin 2) is held LOW
3. Reveal mode allows display of text previously concealed by 'conceal display' control characters.
4. This code is sent from the SAA5010 or the SAA5012 Series as a repeated command. Thus Reveal mode is set for as long as the Reveal key is depressed. The SAA5050 reverts to normal 'not Reveal' mode 160 ms after the last Reveal command.
5. The Superimpose output is LOW only if Superimpose mode is set and the DE (display enable) input is HIGH.
6. The above table shows code required for functions specified.
   The SAA5010 or the SAA5012 Series transmits and the SAA5050 requires the inverse of these codes i.e. $\overline{b_7}$ to $\overline{b_1}$. The code is transmitted serially in the following order: $\overline{b_7}$ $\overline{b_1}$ $\overline{b_2}$ $\overline{b_3}$ $\overline{b_4}$ $\overline{b_5}$ $\overline{b_6}$.
   For full details of remote control data coding see the SAA5010 or the SAA5012 data sheets.

TABLE 3

Conditions affecting display (see note 3)

	Inputs		Control data		Outputs	
	Picture On (PO)	Display Enable (DE)	Superimpose Mode	Box	Text Display Enabled (i.e. R,G,B,Y outputs)	Blanking
(a)	1	0	1 or 0	1 or 0	0	0
(b)	0	1	1 or 0	1 or 0	1	1
(c)	0	0	1 or 0	1 or 0	0 (note 2)	1
(d)	1	1	0	0	0	0
(e)	1	1	1	0	1	0
(f)	1	1	1	1	1	1
(g)	1	1	0	1	1	1

Notes

1. For tv mode (Picture On = '1', Superimpose mode not allowed) rows (a), (d) and (g) of Table 3 refer to display row 0 only. For all other rows text display is disabled and Blanking = '0'.
2. The R, G, B outputs may contain character and background colour information. The only exception is that background colours are inhibited when Blanking = '0'.
3. Valid during display period only (see Fig.5) otherwise no character or background information is displayed as blanking is determined by the Picture On. (No blanking if PO = '1').

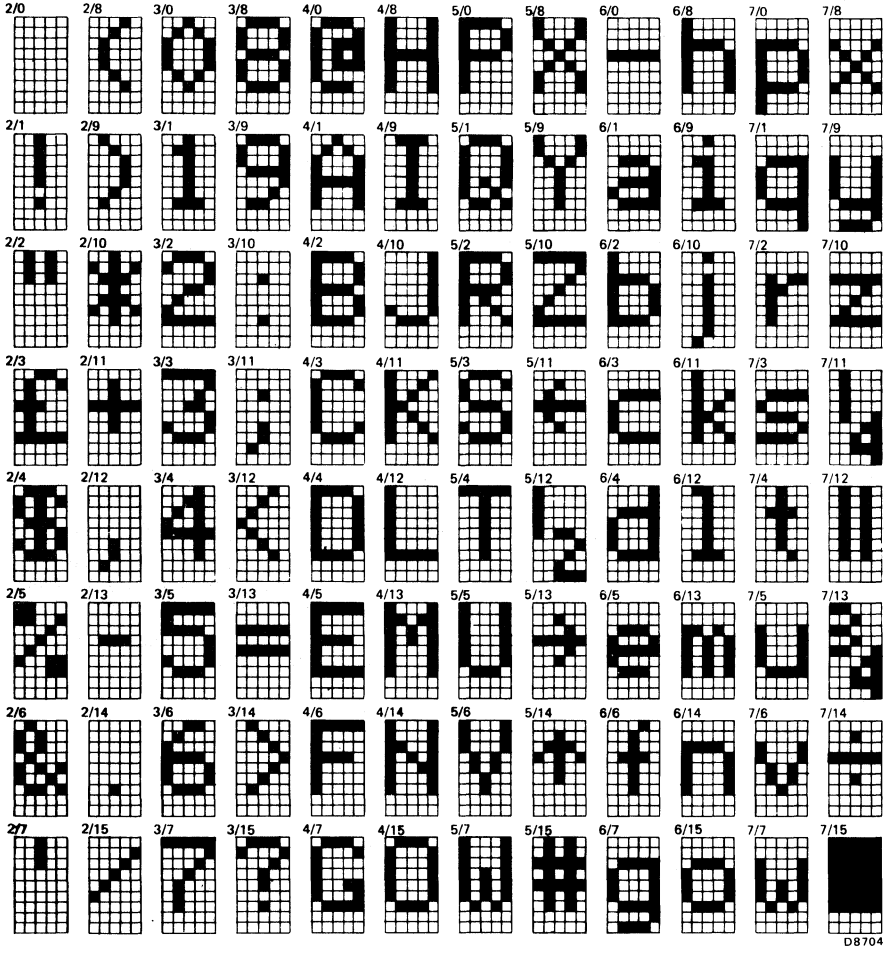


Fig. 11 SAA5050 character set (English).

Fig.12 SAA5051 character set (German).

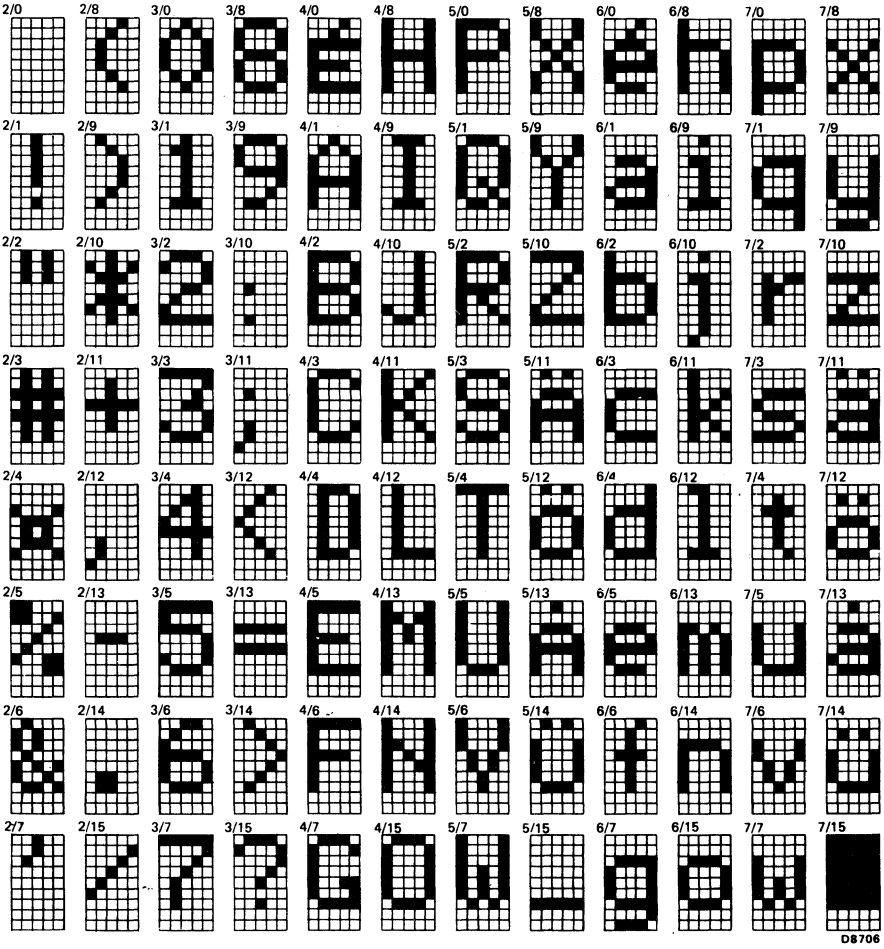


Fig. 13 SAA5052 character set (Swedish).

Fig.14 SAA5053 character set (Italian).

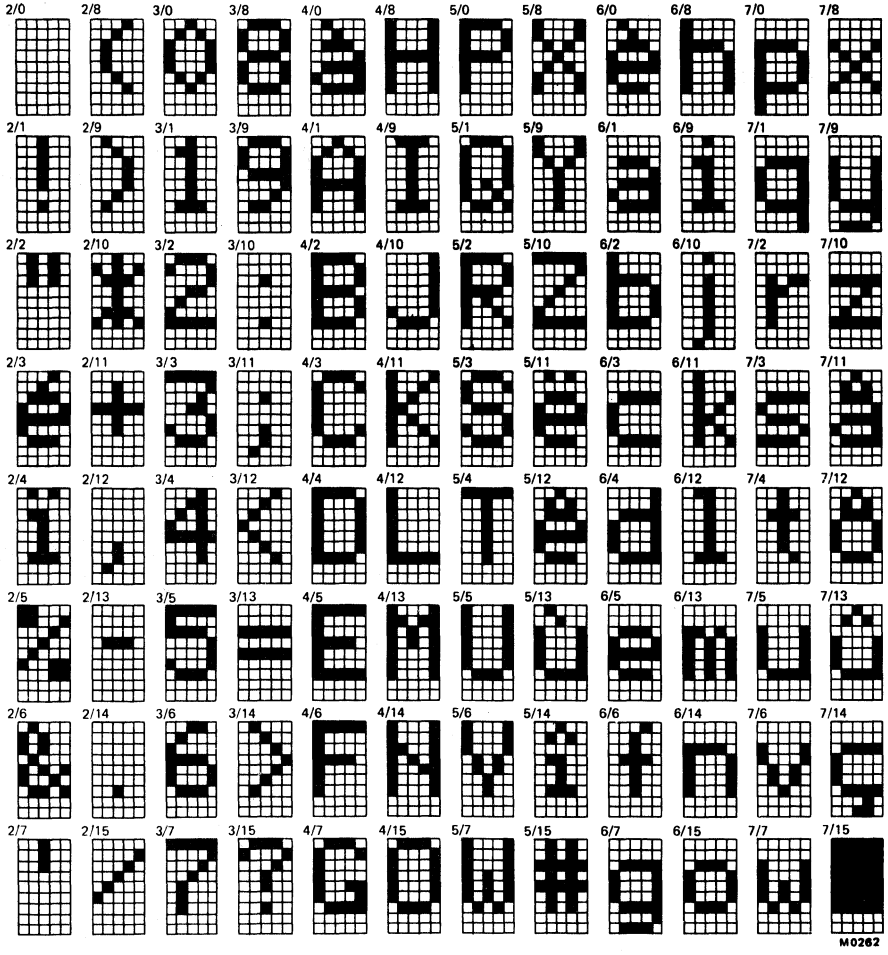


Fig. 15 SAA5054 character set (Belgian)

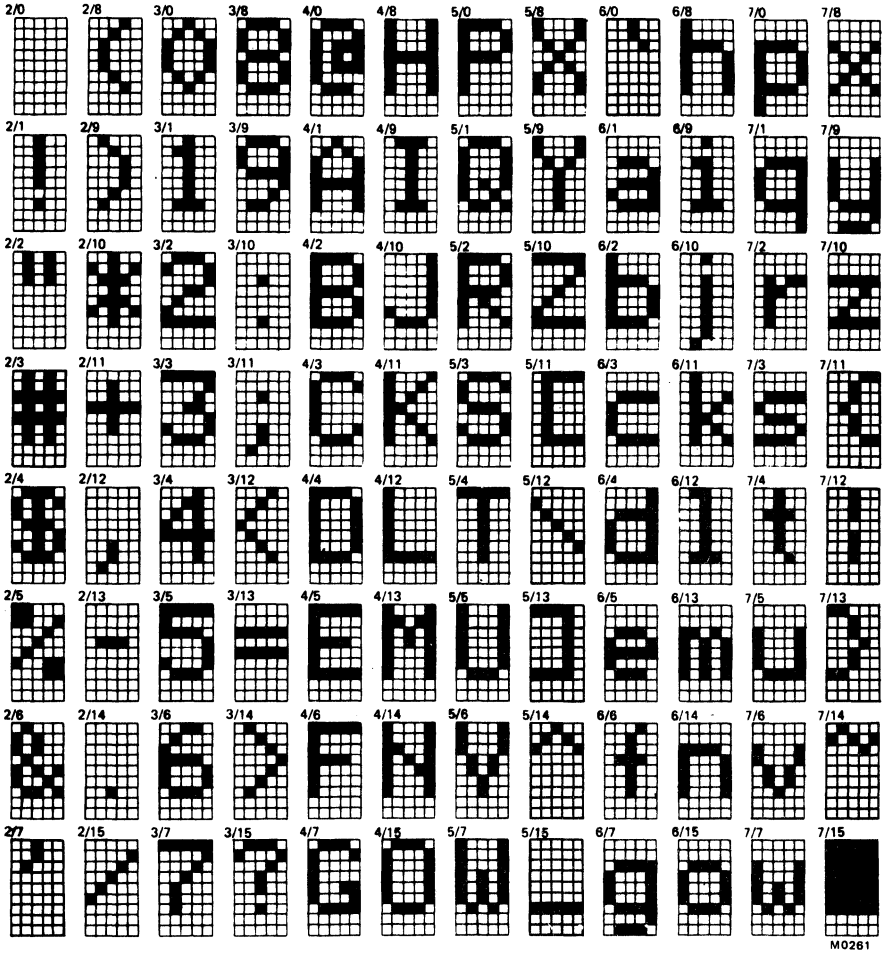


Fig.16 SAA5055 character set (US ASCII).

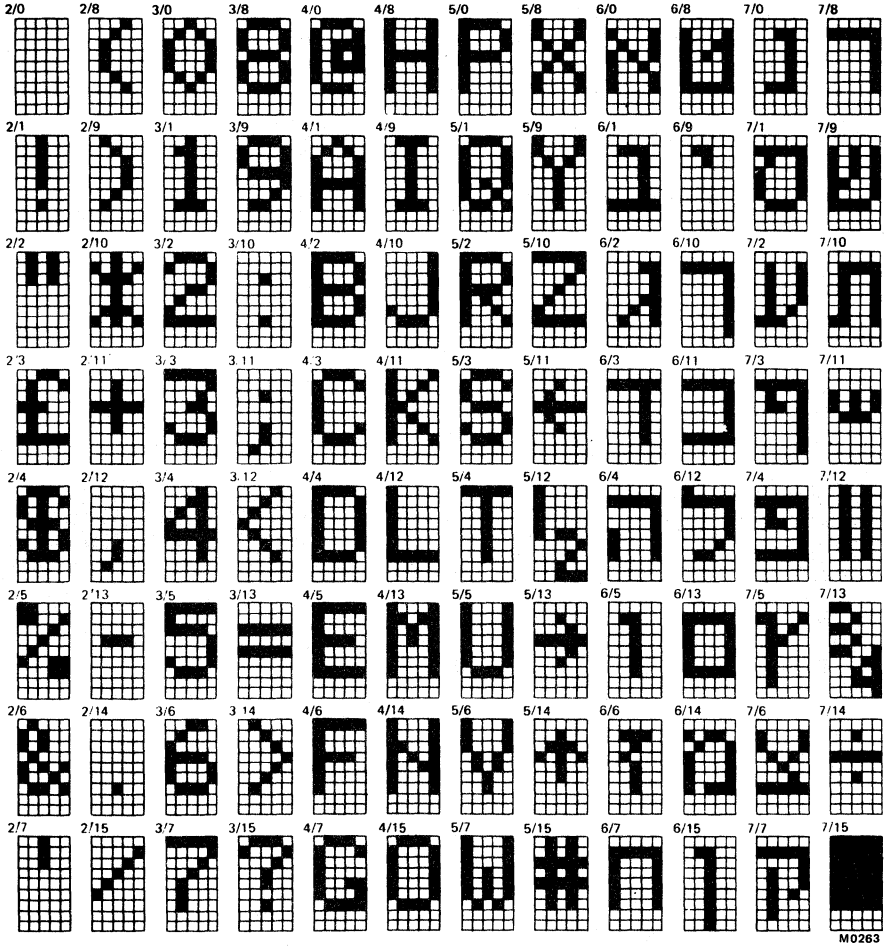


Fig.17 SAA5056 character set (Hebrew).

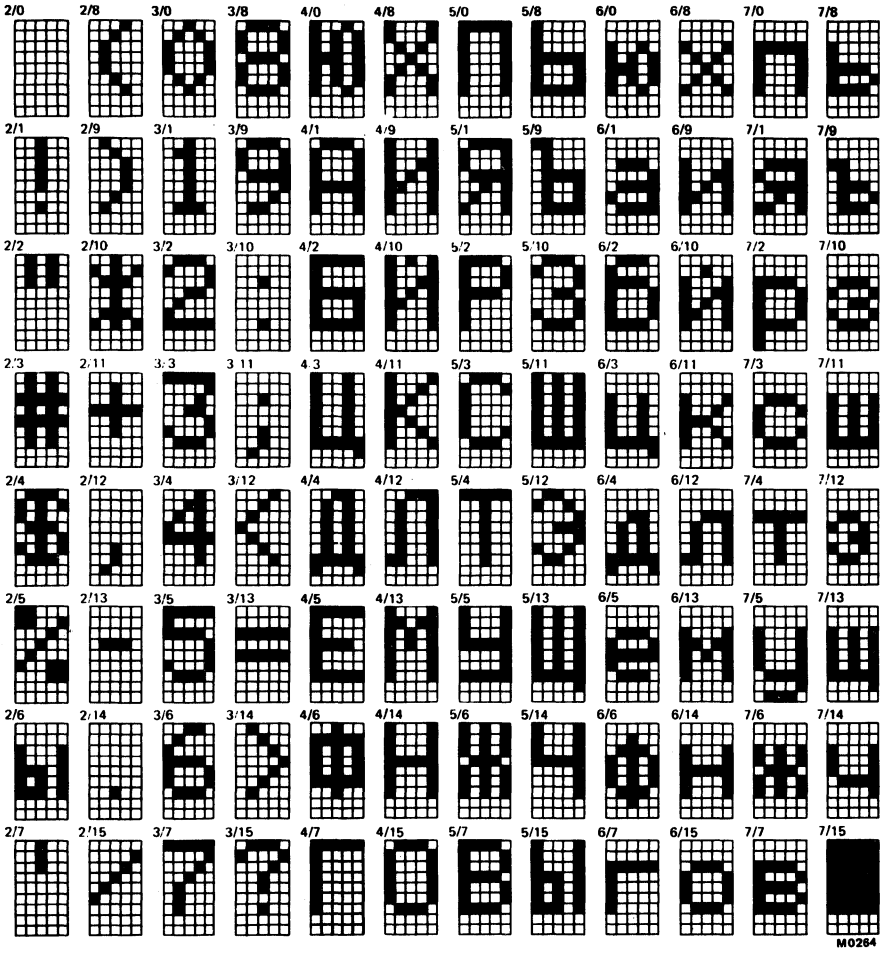


Fig.18 SAA5057 character set (Cyrillic).

MICROCOMPUTER/MICROPROCESSOR PERIPHERAL IC FOR VIEWDATA (LUCY)

The SAA5070 is a complex microcomputer/microprocessor peripheral integrated circuit in N-channel MOS technology intended for use in wired data communication systems, notably viewdata.

Features

- Microcomputer/microprocessor interface. • Modem – both 1200/75 and 1200/1200 baud.
- Line "UART" and tape recorder "UART", both with software parity control (or 8-bit without parity).
- Tape recorder modem (modified 'Kansas City' standard 1300 baud).
- Autodialler for British Post Office and Continental requirements.
- IBUS receivers and transmitters. • Timer circuits (60 s and 1.5 s time-outs).
- General input/output ports.
- Provision for connection of any external modem through V24 interface.

QUICK REFERENCE DATA

Supply voltage	V_{DD}	nom.	5	V
Supply current	I_{DD}	typ.	75	mA
Operating ambient temperature range	T_{amb}		−20 to +70	°C

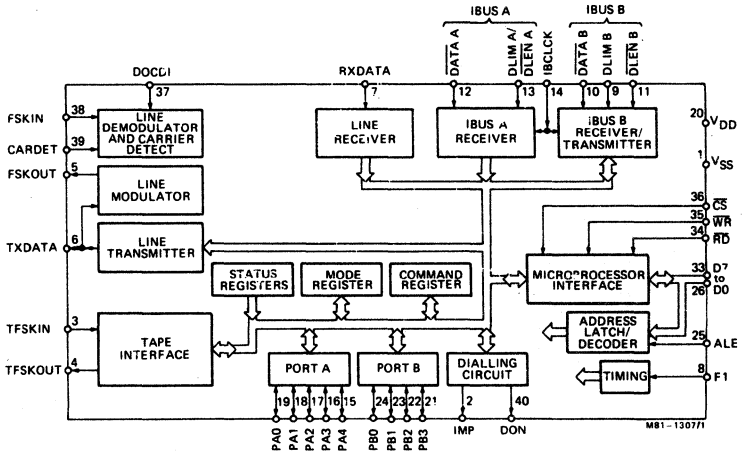
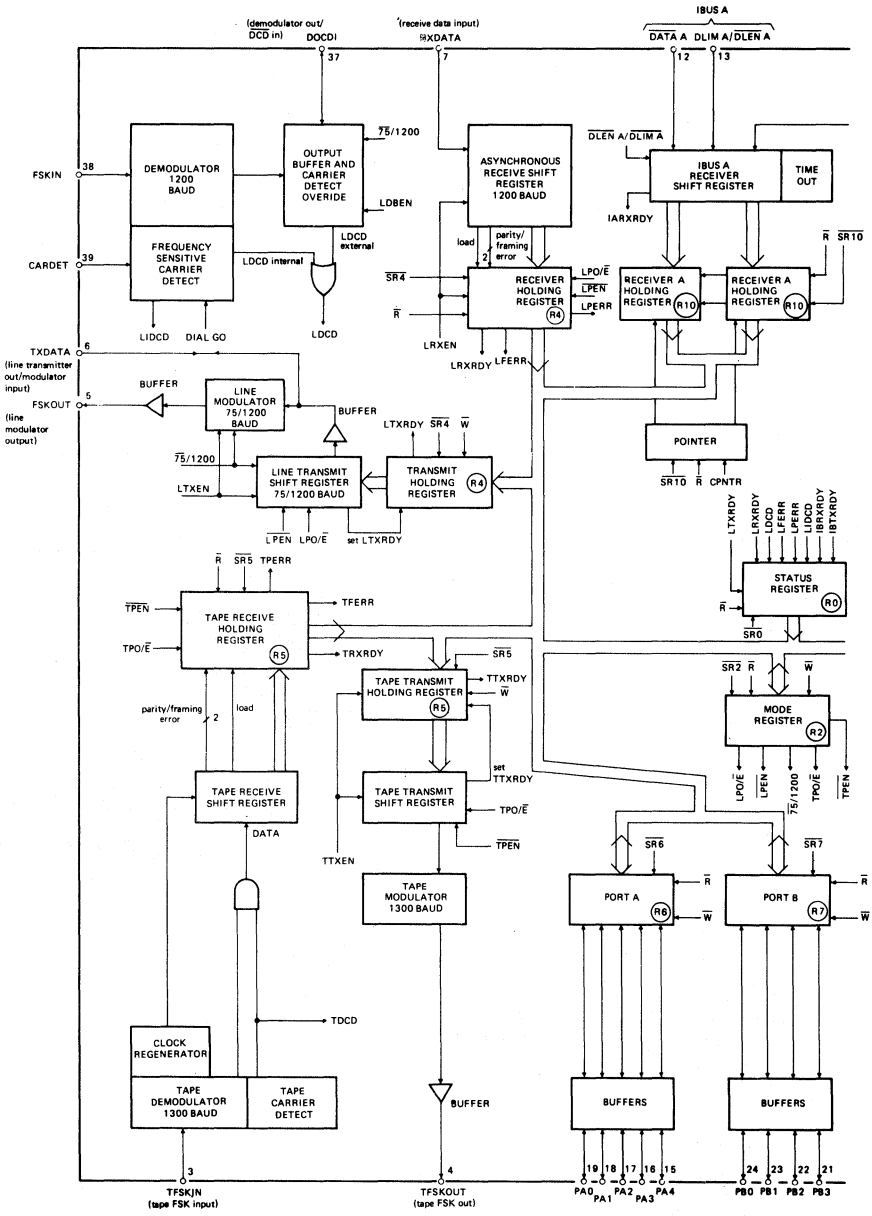


Fig.1a Simplified block diagram

PACKAGE OUTLINE

40-lead DIL; plastic (SOT–129).


(demodulator out/ DCD in)
DOCDI
37
(receive data input)
RXDATA
7
IBUS A
DATA A
DLIM A/DLEN A
12
13
FSKIN
38
DEMODULATOR 1200 BAUD
OUTPUT BUFFER AND CARRIER DETECT OVERIDE
75/1200
LDBEN
ASYNCHRONOUS RECEIVE SHIFT REGISTER 1200 BAUD
DLEN A/DLIM A
IBUS A RECEIVER SHIFT REGISTER
TIME OUT
IARXRDY
CARDET
39
FREQUENCY SENSITIVE CARRIER DETECT
LDCD internal
LDCD external
load
parity/ framing error
2
SR4
RECEIVER HOLDING REGISTER
R4
LPO/E
LPEN
LPERR
RECEIVER A HOLDING REGISTER
R10
R
SR10
LIDCD
DIAL GO
LDCD
LRXEN
LRXRDY
LFERR
TXDATA
6
(line transmitter out/modulator input)
FSKOUT
5
(line modulator output)
BUFFER
LINE MODULATOR 75/1200 BAUD
LTXRDY
SR4
W
POINTER
SR10
R
CPNTR
75/1200
LTXEN
LINE TRANSMIT SHIFT REGISTER 75/1200 BAUD
TRANSMIT HOLDING REGISTER
R4
LPEN
LPO/E
set LTXRDY
LTXRDY
LRXRDY
LDCD
LFERR
LPERR
LIDCD
IBRXRDY
IBTXRDY
STATUS REGISTER
R0
SR0
SR5
TPERR
TPEN
TAPE RECEIVE HOLDING REGISTER
R5
TFERR
TPO/E
TRXRDY
SR5
TAPE TRANSMIT HOLDING REGISTER
R5
TTXRDY
W
SR2
MODE REGISTER
R2
parity/framing error
2
load
set TTXRDY
TAPE RECEIVE SHIFT REGISTER
TAPE TRANSMIT SHIFT REGISTER
TPO/E
TPEN
DATA
TTXEN
SR6
SR7
PORT A
R6
PORT B
R7
TAPE MODULATOR 1300 BAUD
TDCD
CLOCK REGENERATOR
TAPE DEMODULATOR 1300 BAUD
TAPE CARRIER DETECT
BUFFER
BUFFERS
BUFFERS
3
TFSKIN
(tape FSK input)
4
TFSKOUT
(tape FSK out)
19
18
17
16
15
PA0
PA1
PA2
PA3
PA4
24
23
22
21
PB0
PB1
PB2
PB3

DEVELOPMENT DATA

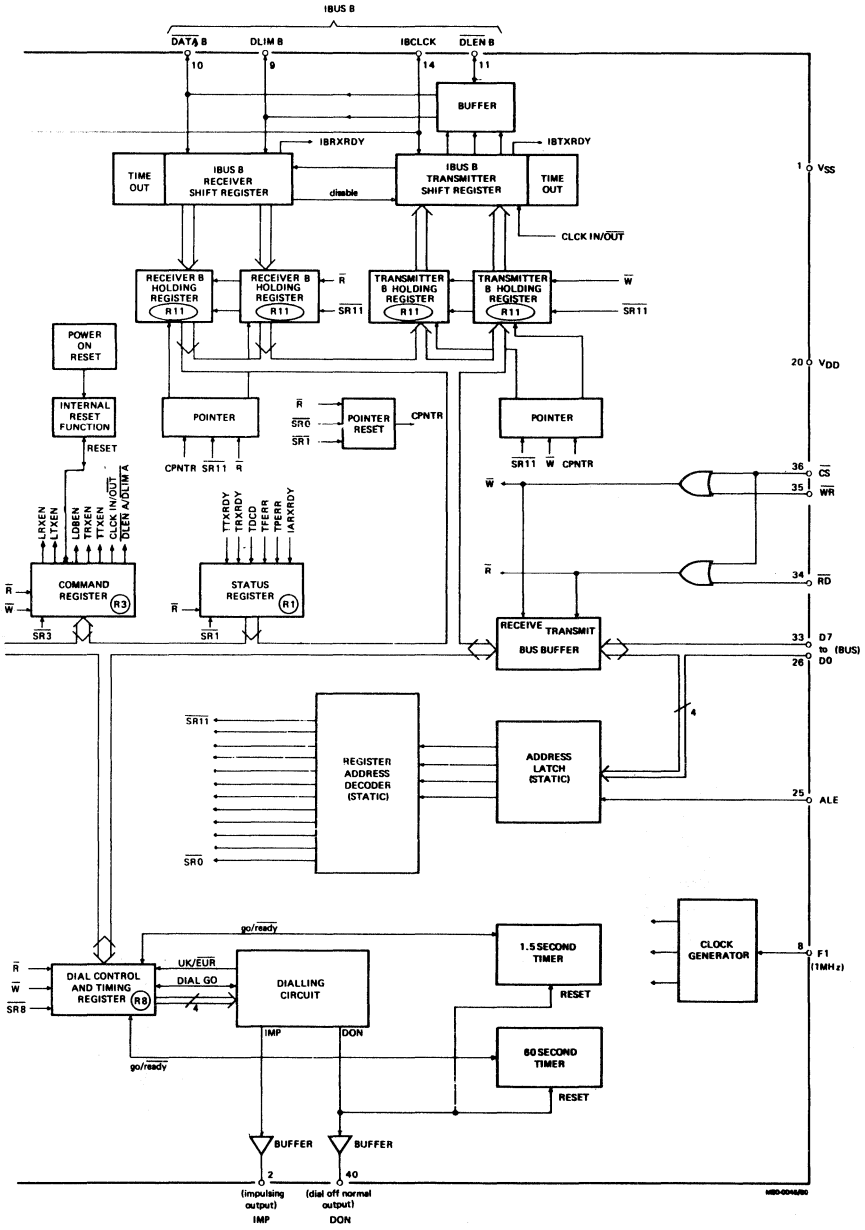


Fig. 1b. Detailed block diagram

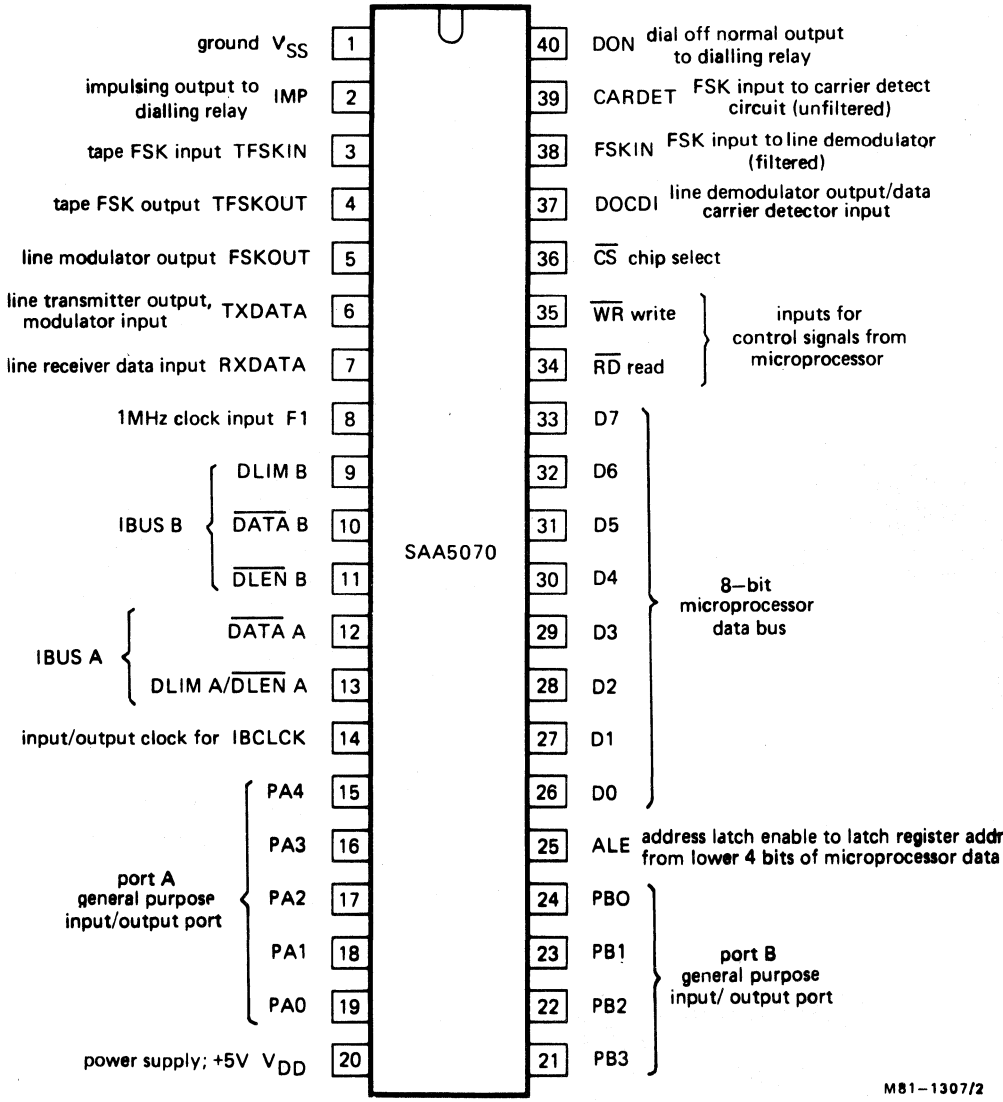


Fig.2 Pinning diagram

DESCRIPTION

The SAA5070 is a 40 pin integrated circuit in N-channel MOS with a 1 MHz clock supplying all the operating frequencies. It performs most of the hardware functions of a viewdata terminal including an autodialling circuit, a 1200 baud demodulator and asynchronous receiver, and a 75/1200 baud modulator and asynchronous transmitter.

The device also includes a tape interface circuit suitable for the recording of character codes of pages of text on a standard audio cassette recorder, and an IBUS receiver and receiver/transmitter on separate ports enabling the software recoding of IBUS transmissions. The 75 baud modulator and asynchronous transmitter can be switched to operate at 1200 baud for private telecommunications systems.

There are also two general purpose input/output ports. Port A could, for example, be used as an interface to a non volatile RAM which can store telephone numbers for autodialling and user passwords and Port B could be used for display control.

The SAA5070 has been partitioned for flexibility of use, e.g. an external modem can be used, if required, in conjunction with the internal asynchronous receiver and transmitter, or the internal modem can be used independently of the internal receiver and transmitter. Also the tape interface can work independently of, and simultaneously with, the line receiver.

HANDLING

Inputs and outputs are protected against electrostatic charge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices. (See 'HANDLING MOS DEVICES').

DEVELOPMENT DATA

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC134).

Voltages (with respect to pin 1)		min.	typ.	max.	
Supply voltage (pin 20)	V_{DD}	−0.3	–	7.5	V
Input voltage:					
PORT A (pins 15 to 10) and PB0 (pin 24)	V_I	−0.3	–	14.0	V
Input voltage (all other pins)	V_I	−0.3	–	7.5	V
Temperatures					
Storage temperature range	T_{stg}			−20 to +125	°C
Operating ambient temperature range	T_{amb}			−20 to +70	°C

CHARACTERISTICS

Supply voltage (pin 20)	V_{DD}	4.5	–	5.5	V

The following characteristics apply at T_{amb} = 25 °C and V_{DD} = 5 V unless otherwise stated.

Supply current	I_{DD}	–	75	150	mA
Inputs					
All inputs (except F1 clock)					
Input voltage; LOW	V_{IL}	−0.3	–	0.8	V
Input voltage; HIGH	V_{IH}	2.0	–	5.5	V
Input leakage current (V_I = 0 to 5.5 V)	I_{IR}	–	–	10	μA
Input capacitance	C_I	–	–	7	pF

Data specific to certain inputs

		min.	typ.	max.	
F1 (1 MHz) Clock					
Input voltage; LOW	V_{IL}	−0.3	–	0.6	V
Input voltage; HIGH	V_{IH}	2.2	–	5.5	V
Input leakage current (V_I = 0 to 5.5 V)	I_{IR}	–	–	10	μA
Input capacitance	C_I	–	–	7	pF
Mark/space ratio (measured at 1.5 V level)		40:60	–	60:40	
$\overline{\text{DATA}}$ A, DLIM A/$\overline{\text{DLEN}}$ A (IBUS A)					
Data set up time (Fig.14)	t_{DS}	3	–	–	μs
Data hold time (Fig.14)	t_{DH}	3	–	–	μs
DLIM clock; HIGH (Fig.14)	t_{CH}	4	–	–	μs
DLIM clock; LOW (Fig.14)	t_{CL}	4	–	62	μs
Time between commands	t_{BC}	140	–	∞	μs
DLIM frequency	f_{DLIM}	16	–	160	kHz
ALE (Address Latch Enable) (Figs. 3 and 4)					
Pulse width (HIGH)	t_{ALEH}	400	–	–	ns
Cycle time	T_{ALE}	–	2500	–	ns
$\overline{\text{RD}}$, $\overline{\text{WR}}$ and $\overline{\text{CS}}$ (Figs. 3 and 4)					
Control pulse width	t_{WL}	–	700	–	ns
Address hold time	t_{LA}	80	–	–	ns
Address set-up time	t_{AL}	120	–	–	ns
Read cycle timings (Fig.3)					
ALE to read pulse delay time	t_{ALR}	80	–	–	ns
Read pulse (falling edge) to data bus delay time	t_{RD}	–	–	500	ns
Data hold time	t_{DR}	0	–	200	ns
Write cycle timings (Fig.4)					
ALE to write pulse delay time	t_{ALW}	80	–	–	ns
Address set-up time to $\overline{\text{WR}}$	t_{AW}	230	–	–	ns
Data set up time before $\overline{\text{WR}}$	t_{DW}	500	–	–	ns
Data hold time after $\overline{\text{WR}}$	t_{WD}	120	–	–	ns

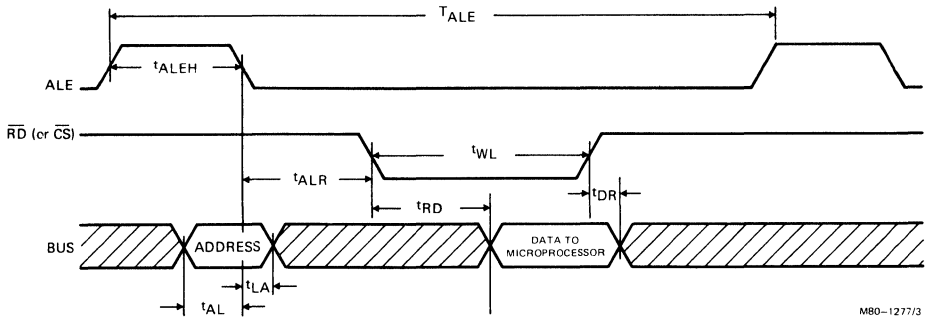


Fig.3 Read cycle timing

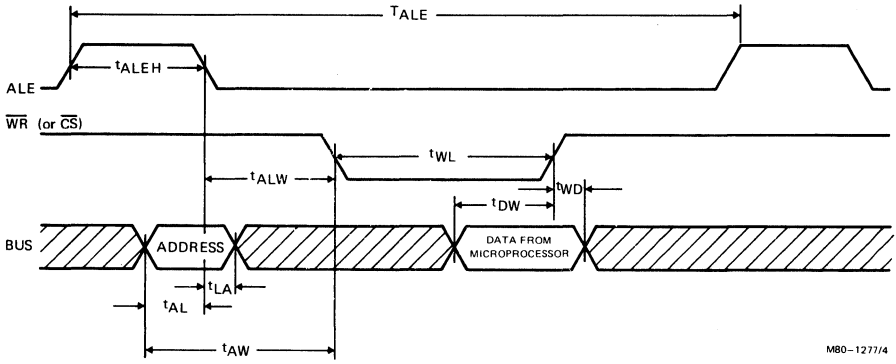


Fig.4 Write cycle timing

Inputs/Outputs

These are protected against connection to V_{SS} or V_{DD}

$\overline{\text{DATA}}$ B, DLIM B, $\overline{\text{DLEN}}$ B, IBCLCK (IBUS B)			min.	typ.	max.	
Input voltage; LOW	Fig.14	V_{IL}	−0.3	–	0.8	V
Input voltage; HIGH		V_{IH}	2.0	–	5.5	V
Input leakage current (V_I = 0 to 5.5 V) (3 state buffers off)		I_{IR}	–	–	10	μA
Input capacitance		C_I	–	–	7	pF
Output voltage; LOW (I_{OL} = 1.6 mA)		V_{OL}	–	–	0.4	V
Output voltage; HIGH ($-I_{OH}$ = 200 μA)		V_{OH}	2.4	–	–	V
Output rise and fall times (C_L = 300 pF)		t_r | t_f	–	–	1	μs

other timings as IBUS A

DOCDI (open drain output)					
Input voltage; LOW	V_{IL}	−0.3	–	0.8	V
Input voltage; HIGH	V_{IH}	2.0	–	5.5	V
Input leakage current; (V_I = 0 to 5.5 V) (output transistor off)	I_{IR}	–	0.4	10	μA
Input capacitance	C_I	–	–	7	pF
Output voltage; LOW (I_{OL} = 1.6 mA)	V_{OL}	–	0.4	–	V

TXDATA

(Internal resistive pull-up, permitting wired - AND connection)

Input voltage; LOW	V_{IL}	−0.3	–	0.8	V
Input voltage; HIGH	V_{IH}	2.0	–	5.5	V
Input current; LOW (V_I = 0.4 V)	$-I_{IL}$	–	–	500	μA
Input capacitance	C_I	–	–	7	pF
Output voltage; LOW (I_{OL} = 1.6 mA)	V_{OL}	–	–	0.4	V
Output voltage; HIGH ($-I_{OH}$ = 50 μA)	V_{OH}	2.4	–	–	V
Load capacitance	C_L	–	–	40	pF
Output rise time (C_L = 40 pF)	t_r	–	3	–	μs

PA0 to PA4 (PORT A) (open drain output)					
Input voltage; LOW	V_{IL}	−0.3	–	0.8	V
Input voltage; HIGH	V_{IH}	2.0	–	13.2	V
Input capacitance	C_I	–	–	7	pF
Output voltage; LOW (I_{OL} = 1.6 mA)	V_{OL}	–	–	0.4	V
Off state leakage current (V_I = 0 to 13.2 V)	I_{OR}	–	–	10	μA
Load capacitance	C_L	–	–	40	pF
Fall time	t_f	–	–	1	μs

Inputs/Outputs (continued)		min.	typ.	max.	
PBO (PORT B) (open drain output) as PORT A except					
Output voltage; LOW (I_{OL} = 1.6 mA)	V_{OL}	–	–	0.4	V
Output voltage; HIGH	V_{OH}	–	–	13.2	V
Load capacitance	C_L	–	–	100	pF
PB1 to PB3 (PORT B)					
Input voltage; LOW	V_{IL}	−0.3	–	0.8	V
Input voltage; HIGH	V_{IH}	2.0	–	5.5	V
Input capacitance	C_I	–	–	7	pF
Load capacitance	C_L	–	–	100	pF
Output voltage; LOW (I_{OL} = 1.6 mA)	V_{OL}	–	–	0.4	V
Off state leakage current (V_I = 0 to 5.5 V)	I_{OR}	–	–	10	μA
D0 to D7 (8-bit Data bus)					
Input voltage; LOW	V_{IL}	−0.3	–	0.8	V
Input voltage; HIGH	V_{IH}	2.0	–	5.5	V
Output voltage; LOW (I_{OL} = 1.6 mA)	V_{OL}	–	–	0.4	V
Output voltage; HIGH ($-I_{OH}$ = 200 μA)	V_{OH}	2.4	–	–	V
Input leakage current (V_I = 0 to 5.5 V) (3-state buffers off)	I_{IR}	–	–	10	μA
Input capacitance	C_I	–	–	7	pF
Output rise and fall times (C_L = 150 pF)	t_r | t_f	–	–	150	ns
Outputs					
These are protected against connection to V_{SS} or V_{DD}.					
FSKOUT and TFSKOUT					
Output voltage; LOW (I_{OL} = 1.6 mA)	V_{OL}	–	–	0.4	V
Output voltage; HIGH ($-I_{OH}$ = 200 μA)	V_{OH}	2.4	–	–	V
Rise and fall times (C_L = 100 pF)	t_r | t_f	–	–	500	ns
DON and IMP					
Output voltage; LOW (I_{OL} = 50 μA)	V_{OL}	–	–	0.2	V
Output current; HIGH (V_{OH} = 0.8 V clamped)*	I_{OH}	200	–	2000	μA
Output voltage; HIGH ($-I_{OH}$ = 200 μA)	V_{OH}	2.4	–	–	V

Autodialling timings are given in Fig.6

*These outputs are normally intended to drive the base-emitter junction of a bipolar transistor and so in normal use the V_{OH} may be clamped to V_{be}.

DEVELOPMENT DATA

RESET FUNCTION

It is possible to reset the SAA5070 to its nominal state either automatically on power-on by means of an internal power-on reset circuit, or by setting D5 in command register (R3) to '1', which returns to '0' on completion of the reset sequence. The device resets to viewdata mode, i.e. 75 baud transmit rate, even parity, etc, as shown by the all zero's state in registers R0 to R3, R6, R7 and R8 except for LTXRDY, IBTXRDY, and TTXRDY (in the status registers R0 and R1) which will come up as '1' after the transmitters have been reset, showing that they are ready to accept new data.

APPLICATION DATA

Chip organisation

Each section of the SAA5070 may be accessed by the microprocessor via a register (of up to 8-bits) connected to an internal data bus. There are 15 registers on chip accessed by 11 addresses. Some of the registers are two-level, i.e. two bytes of data are transferred by two successive read (or write) sequences to the same address, also some read only registers have the same address as a write only register.
An appendix lists the registers, their contents, and their use.

Section descriptions

The description of each section includes associated registers, flags, and pins, as well as the method of operation. On the following block diagrams external pins are shown boxed and internal flags are shown underlined.

Microprocessor Interface

D0 to D7 — I/O — 8-bit input/output port

Associated pins:	ALE	input	address latch enable from microprocessor
	$\overline{WR}$	input	write pulse from microprocessor
	$\overline{RD}$	input	read pulse from microprocessor
	$\overline{CS}$	input	chip select

Operation

The control microprocessor communicates with the SAA5070 via an 8-bit data I/O port D0 to D7. An internal read or write pulse is produced by gating $\overline{RD}$ and $\overline{WR}$ with $\overline{CS}$. A single register is enabled onto the internal bus by gating the read or write lines with the address decoder outputs. The register address is taken from the 4 least significant data bits latched on the falling edge of ALE. (See timing diagrams Figs. 3, 4). The address (D3 most significant, D0 least significant) relates directly to the register numbers shown in the register map, detailed in the appendix, and referred to in other section descriptions.

Four registers not specifically related to any one section are included. These are the status registers R0 and R1, the mode register R2, and the command register R3. These registers are used to determine the current status of the device, to dictate the mode of operation or to initiate a specific operation. The status registers are read only, the mode and command registers are read/write. When writing to these registers, it is recommended that the unallocated bits are set to '0'. On reading the registers the state of the unallocated bits should be assumed to be random. The exact functions of the flags contained in these registers are described in the section description to which they relate.

Autodial section (see Fig.5)

Associated Register: — R8 — D0 to D3 write only
D4 to D7 read/write

Associated flags in other registers: None

Associated pins: DON output, IMP output } to drive dialling relays

Operation

The autodial section includes a clock divider, a digit impulse counter, a sequence controller and an impulse generator (see block diagram Fig.5). A sequence to generate the impulses for one digit is initiated by setting D5 (DIAL GO) to '1', D3 to D0 to the binary code of the required digit, and D7 to the required mode. This initiates the sequence controller which loads the binary code into the digit impulse counter. The counter then generates the correct number of impulses at the rate of 10 per second, together with a DON pulse which overlaps the impulses by about 7 ms at the start and end (see Figs.6, 7); the interdigit pause period is also added by the sequence controller. D5 is reset to '0' at the end of a dialling sequence and may be read by the microprocessor to determine when the dial circuit is free to accept the next digit.

D7 (UK/$\overline{\text{EUR}}$) determines the mark/space ratio of the IMP pulses

UK = 2 off to 1 on
$\overline{\text{EUR}}$ = 1.5 off to 1 on
} both one pulse per 100 ms

There is a timer in the dial circuit which can be used to time out 1.5 seconds or 60 seconds by setting D4 or D6 respectively. These bits are read/write and are reset after the relevant time out period. In addition the 60 second timer can be reset by writing a '0' to D6. The 60 second timer may be used typically by the microprocessor to release the telephone line if connection has not been made within 60 seconds. The DON pulse resets the counter so that the time out is taken from the end of the last digit dialled. Once a dialling sequence for one digit has been initiated, R8 should be used only in read mode until D5 has been reset internally to '0' indicating the end of the dial sequence for that digit.

When D5 (DIAL GO) is set to '1' the carrier detect circuit (see the next section and Fig.8) is disabled.

DEVELOPMENT DATA

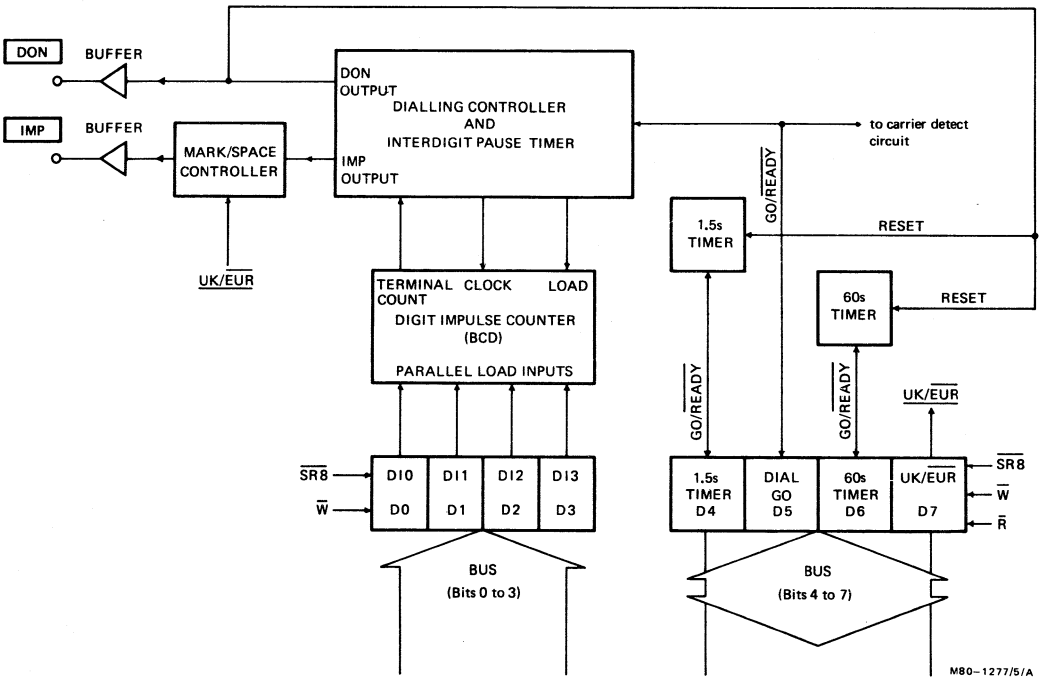
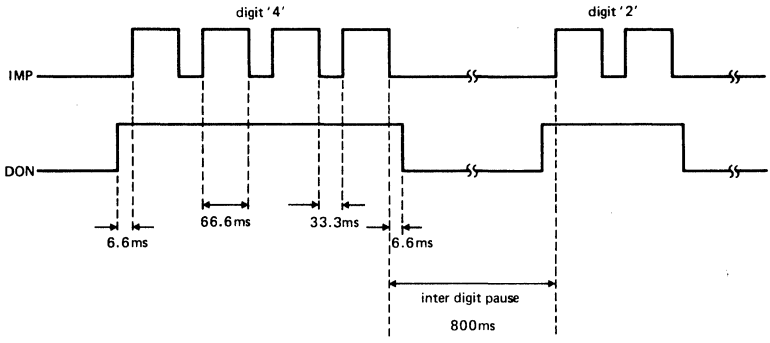


Fig.5 Autodial block diagram



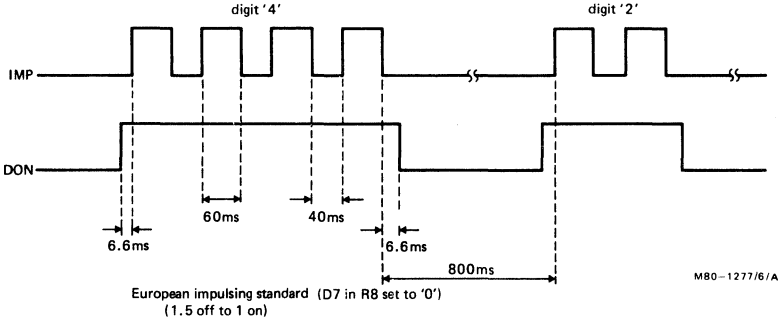


Fig.6 Autodialling timing

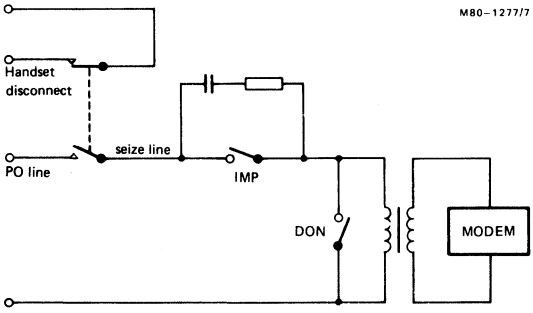


Fig.7 Simplified relay diagram

DEVELOPMENT DATA

Line Demodulator and Carrier Detect (see Fig.8)

Associated Register:– None

Associated flags in other registers:

LIDCD	–	D2	–	R0 (Status)	–	instantaneous carrier detect flag
LDCD	–	D5	–	R0 (Status)	–	carrier detect flag
$\overline{75}$/1200	–	D5	–	R2 (Mode)	–	transmit frequency baud rate (used in demodulator carrier detect circuit)
LDBEN	–	D4	–	R3 (Command)	–	line demodulator output buffer and carrier detect enable
DIAL GO	–	D5	–	R8 (Dial control)	–	used to disable carrier detect circuit during dialling sequence

Associated pins:	FSKIN	–	input	–	filtered, squared F.S.K. signal
	CARDET	–	input	–	unfiltered (squared) F.S.K. signal.
	DOCDI	–	input/output	–	demodulator output, external LDCD in

Operation

The input to the demodulator is the previously filtered and squared up F.S.K. signal from the telephone line. Its output is a pseudo analogue signal which must be externally filtered and squared to produce the demodulated data. The carrier detect circuit functions in the following modes:

a) Viewdata mode (1200 baud receive, 75 baud transmit). Initially, a narrow frequency band 'window' around 1300 Hz is accepted as carrier, this must be applied to the CARDET input. If a frequency in this range is present, the 'instantaneous carrier detected' flag will be HIGH (LIDCD), after about 2 seconds the 'line carrier detected' flag will be set HIGH (LDCD). When this occurs, the frequency window is widened to include 2100 Hz and the circuit no longer takes its input from the CARDET pin, but from the FSKIN pin.
If carrier is then removed LIDCD immediately goes LOW, and after about 1 second LDCD is reset, the frequency window again becomes narrow and around 1300 Hz and the CARDET input again becomes active. Reappearance of carrier in the 1300 Hz range will cause a repeat of the above.

b) 1200 baud each way mode
Only the instantaneous carrier detect is active in this mode. LDCD is forced LOW and the CARDET input inhibited (only FSKIN should be used in this mode).

c) External carrier detect input
If an external modem is used its (active LOW) carrier detect output is connected to DOCDI. Provided that the demodulator is not enabled, LDCD will be set if DOCDI is LOW and reset if it is HIGH.

Demodulator enable

LDCD is produced by the carrier detect circuit, which is enabled by LDBEN and disabled by DIAL GO, In the viewdata mode the demodulator is enabled by LDCD.
In the 1200 baud each way mode the demodulator is enabled directly by LDBEN.

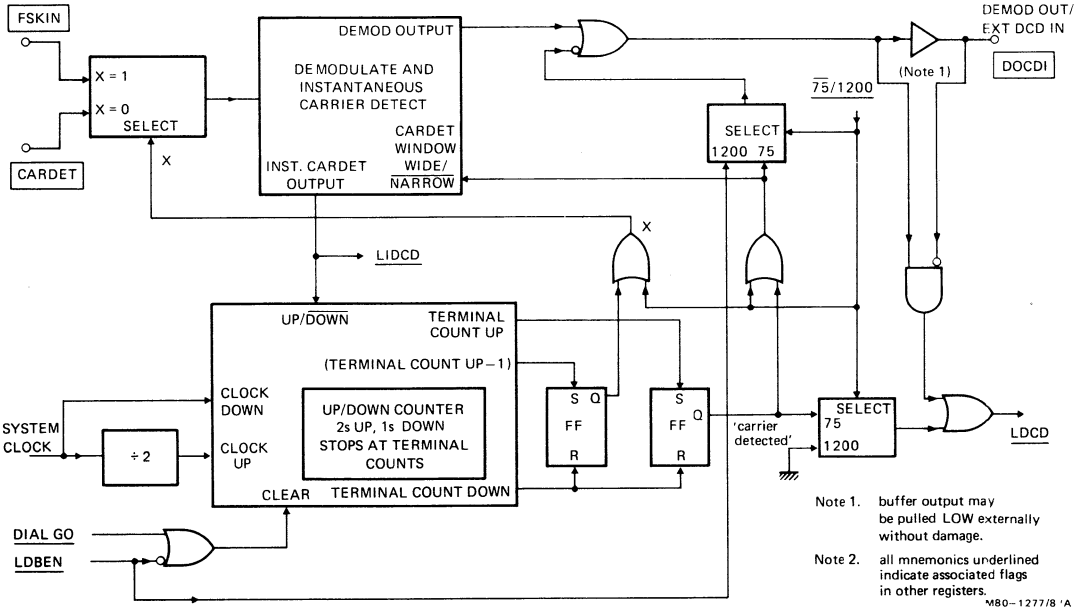


Fig.8 Line demodulator and carrier detect block diagram

Line Receiver (see Fig.9)

Associated Register: – R4 read only

Associated flags in other registers:

LRXRDY	–	D6	–	R0 (status)	–	valid data available in receive holding register
LFERR	–	D4	–	R0 (status)	–	line framing error (derived from STOP bit of message).
LPERR	–	D3	–	R0 (status)	–	line parity error.
LPO/$\overline{E}$	–	D7	–	R2 (mode)	–	odd or even parity detection mode select
$\overline{\text{LPEN}}$	–	D6	–	R2 (mode)	–	8 bit data or 7 bit plus parity mode select
LRXEN	–	D7	–	R3 (command)	–	line receiver enable.

Associated pins: RXDATA – input – received data input

Operation

The receiver may be configured to work with either 7 data bits and 1 parity, or with 8 data bits and no parity. Odd or even parity can be detected on chip, the LPERR flag being set when an error is detected. The required mode of operation should be selected by setting $\overline{\text{LPEN}}$ and LPO/$\overline{E}$ to the required states by writing to mode register (R2) before enabling the receiver by setting LRXEN to '1' in command register (R3). The data format is 10 bits per data word. The data word is made up of a start bit (LOW), 8 data bits, the 8th being an optional parity bit, and a stop bit (HIGH). The receive data will remain HIGH after the stop bit until the next data word. When the receiver has been enabled a negative transition is looked for on the RXDATA input indicating a possible start bit. After half a bit rate period the data is sampled again and if it is still LOW it is interpreted as a start bit, initiating a sequence which clocks the data into a shift register. When the full ten bit message has been received, the 8 data bits are parallel loaded into the receiver holding register (R4), the LRXRDY flag is set to '1'. The complement of the stop bit is loaded into the LFERR latch and the result of the parity check is loaded into LPERR latch. If line parity is not enabled i.e. $\overline{\text{LPEN}}$ = '1', then LPERR is held at '0'. The LRXRDY flag is reset to '0' after the microprocessor has read the receiver holding register (R4). The receiver has a 52 times baud rate factor to allow for maximum isochronous distortion.

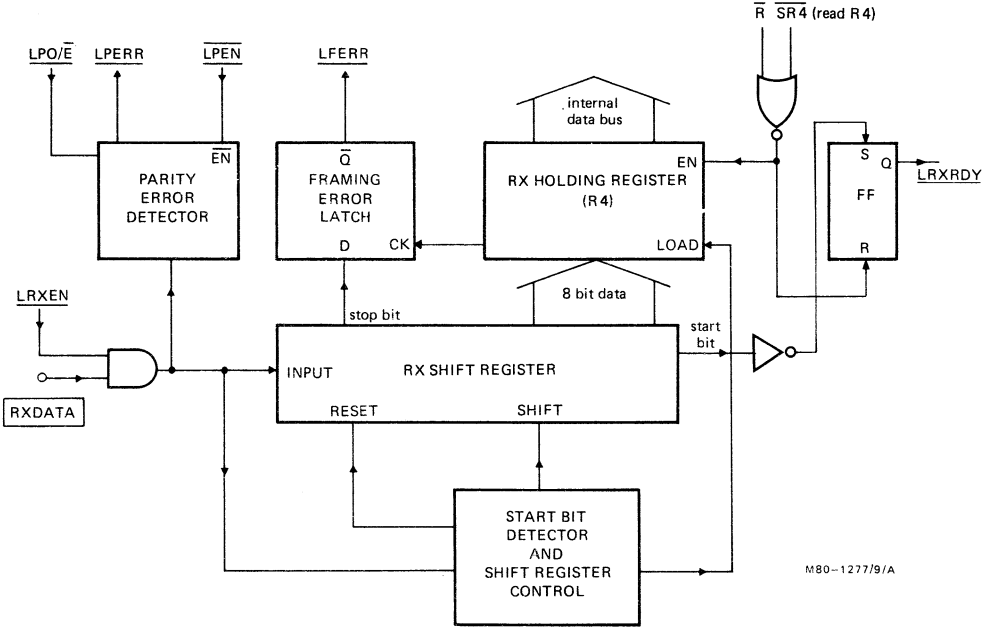


Fig.9 Line receiver block diagram

Line Transmitter (see Fig.10)

Associated Register: – R4 write only

Associated flags in other registers:

LTXRDY	–	D7	–	R0 (status)	–	transmit holding register ready to accept new data
LPO/$\overline{E}$	–	D7	–	R2 (mode)	–	odd or even parity mode select
$\overline{LPEN}$	–	D6	–	R2 (mode)	–	8 bit data or 7 bit data with parity mode select
$\overline{75}$/1200	–	D5	–	R2 (mode)	–	select transmit baud rate
LTXEN	–	D6	–	R3 (command)	–	line transmitter/modulator output enable

Associated pins: TXDATA – I/O – transmitter output (and also modulator input)

Operation

The data format of the transmitter is the same as that of the line receiver i.e. 10-bits, a start bit (LOW) followed by 8-data bits, the 8th bit being an optional parity (selected by LPEN), odd or even parity being selectable (by LPO/$\overline{E}$) ending with a STOP bit (HIGH) the output remaining HIGH until the next data word is written.

The transmitter and modulator may be used together or separately. The transmitter output is brought to the TXDATA pin (if LTXEN = 1) which is connected internally to the modulator input. The TXDATA pin has an internal resistive pull up permitting wire - AND connection. If the modulator is used with an off chip data source (e.g. UART) then data should not be written to the internal transmit holding register (R4). The STOP bit (HIGH) will then be continuously output when LTXEN = 1 (required to enable modulator output) allowing the external UART to control the TXDATA (pin 6).

To operate the transmitter the required mode should be set-up initially by writing to the mode register (R2) the required states of $\overline{75}$/1200, $\overline{LPEN}$, LPO/$\overline{E}$. The transmitter can then be enabled by setting LTXEN to '1' in the command register (R3). The 8-bit data word can then be written to the transmit holding register (R4). If parity is enabled then the 8th bit is ignored and the value of the parity bit calculated from the first 7-data bits and LPO/$\overline{E}$. The LTXRDY flag is set to zero when the holding register is written into. If the transmit output shift register is not currently in use the contents of the holding register are transferred to the output shift register and LTXRDY returns to '1'. This means that new data may now be written to the holding register but will not be transferred to the output shift register until the 10-bits of the current message have been clocked out. The start, stop, and parity bit (if selected) are written into the output shift register with the data word automatically.

Two transmit baud rates are selectable, 75 baud for viewdata transmissions or 1200 baud for private data communication systems.

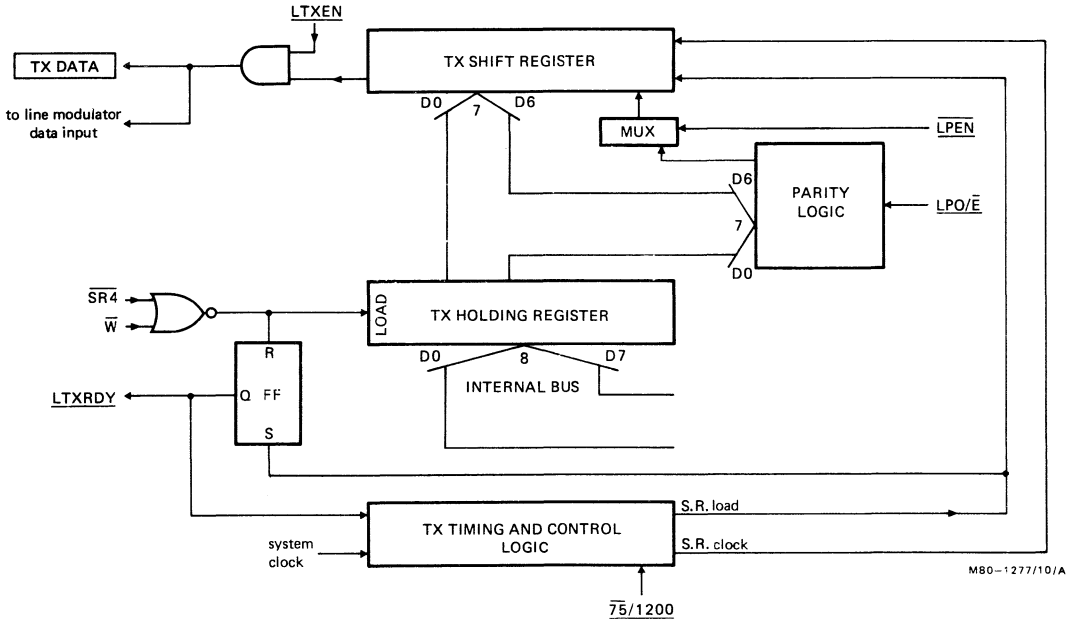


Fig.10 Line transmitter block diagram

Line Modulator (see Fig.11)

Associated Register: – None

Associated flags in other registers:

$\overline{75}$/1200	–	D5	–	R2 (mode)	–	transmit baud rate select.
LTXEN	–	D6	–	R3 (command)	–	line transmitter/modulator output enable.

Associated Pins:	TXDATA	–	I/O	–	modulator input (also (on chip) transmitter output).
	FSKOUT	–	output	–	line modulator output

Operation

The modulator generates a pseudo analogue signal from a serial shift register which is parallel loaded with patterns from an internal ROM. The frequency of the sine wave is determined by the selected baud rate $\overline{75}$/1200, and the value of the data on TXDATA (pin 6).

data	'1'	'0'
1200 baud	1300 Hz	2100 Hz
75 baud	390 Hz	450 Hz

One sine wave cycle is comprised of a 92-bit pattern which after minimal external low pass filtering provides a suitable F.S.K. signal out (see Fig.11)

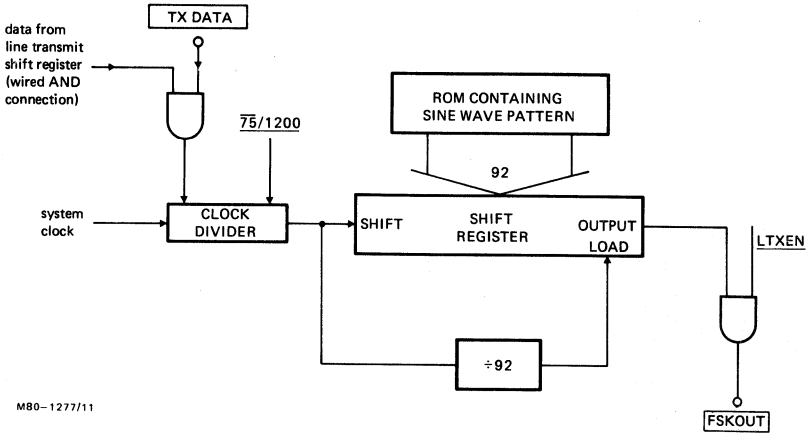


Fig.11 Line modulator block diagram

Tape section (see Fig.12)

Associated registers: – R5 – Consists of two registers with the same address:
transmit holding register write only
receive holding register read only

Associated flags in other registers:

TTXRDY	–	D7	–	R1 (status)	–	transmit holding register ready to accept new data
TRXRDY	–	D6	–	R1 (status)	–	valid data available in receive holding register
TDCD	–	D5	–	R1 (status)	–	tape data carrier detect flag
TFERR	–	D4	–	R1 (status)	–	tape framing error (derived from STOP bit of message)
TPERR	–	D3	–	R1 (status)	–	tape parity error
TPO/$\overline{E}$	–	D3	–	R2 (mode)	–	odd or even parity mode select.
$\overline{TPEN}$	–	D2	–	R2 (mode)	–	8-bit data or 7-bit plus parity mode select
TRXEN	–	D3	–	R3 (command)	–	tape receiver enable
TTXEN	–	D2	–	R3 (command)	–	tape transmitter enable

Associated pins:	TFSKIN	– input	–	F.S.K. input to tape sections
	TFSKOUT	– output	–	F.S.K. modulated data out

DEVELOPMENT DATA

Operation of tape section (see Fig.12)

The tape data modulation system is a modified form of the 'Kansas City' standard. A logic '1' is represented by one cycle of 1300 Hz, and a logic '0' by two cycles of 2600 Hz, the data rate being 1300 baud. The data format is the same as that for viewdata, i.e. 10-bit words consisting of a START bit (LOW), followed by 8-data bits, the 8th being an optional parity bit, ending with a STOP bit (HIGH) which is continuous until the next data word.

To operate the tape section the required parity mode should first be set up by writing the required states of TPEN and TPO/$\overline{E}$ to the mode register (R2). The TTXEN command enables the output of the transmit shift register into the modulator, and should be set before data is written to the transmit holding register. (With TTXEN = '0' the modulator outputs a continuous 1300 Hz signal '1'). When a data word is written to the transmit holding register the TTXRDY flag is reset to '0'. If the transmit shift register is not currently active the contents of the holding register, along with valid parity bit (if enabled) and the START and STOP bits are transferred to the transmit shift register, at the same time TTXRDY is set to '1'. The holding register is then free to accept new data but this will not be transferred to the shift register until the current data has been clocked out. Data should be written to the tape transmit holding register, therefore, only when TTXRDY = '1'.

The modulator produces 1300 Hz and 2600 Hz signals which occur synchronously with the data from the transmitter. Hence a '1' is one complete 1300 Hz cycle, and a '0' two complete 2600 Hz cycles. The modulator output, TFSKOUT, requires minimal external low pass filtering to produce data suitable for audio cassette tape recorders.

To overcome the tendency of cassette recorders to attenuate high frequencies, the 1300 Hz signal contains 2 μs wide attenuating pulses every 12 μs. This reduces the 1300 Hz signal by approximately 3 dB relative to the 2600 Hz signal after external filtering.

The data rate of 1300 baud is slightly faster than the 1200 baud line receive rate, allowing incoming data from the line to be transferred simultaneously (via the microprocessor) to tape.

The TFSKIN input accepts the previously filtered and squared data from the tape recorder. The demodulator uses the fact that the modulated data is in phase with clock to regenerate the clock from the data. This permits a wide tolerance on replay speeds. A carrier detect circuit is included which sets the TDCD flag to '1' if carrier (1300 Hz or 2600 Hz) is valid for 100 ms. If carrier is lost for 100 ms the TDCD flag is reset to '0'. This flag may be read by the microprocessor to determine when to enable the tape receiver by setting TRXEN to '1'.

If TRXEN is set, then on detection of a start bit (LOW) data is shifted into the tape receive shift register by the clock which has been extracted from the data. After ten clocks, the contents of the shift register are transferred to the receive holding register. At the same time the complement of the STOP bit is loaded into the TFERR latch, the results of the parity calculation loaded into the TPERR latch, and TRXRDY is set to '1'. The TRXRDY flag is read by the microprocessor to identify when valid data is in the holding register and is reset to '0' when the holding register (R5) is read.

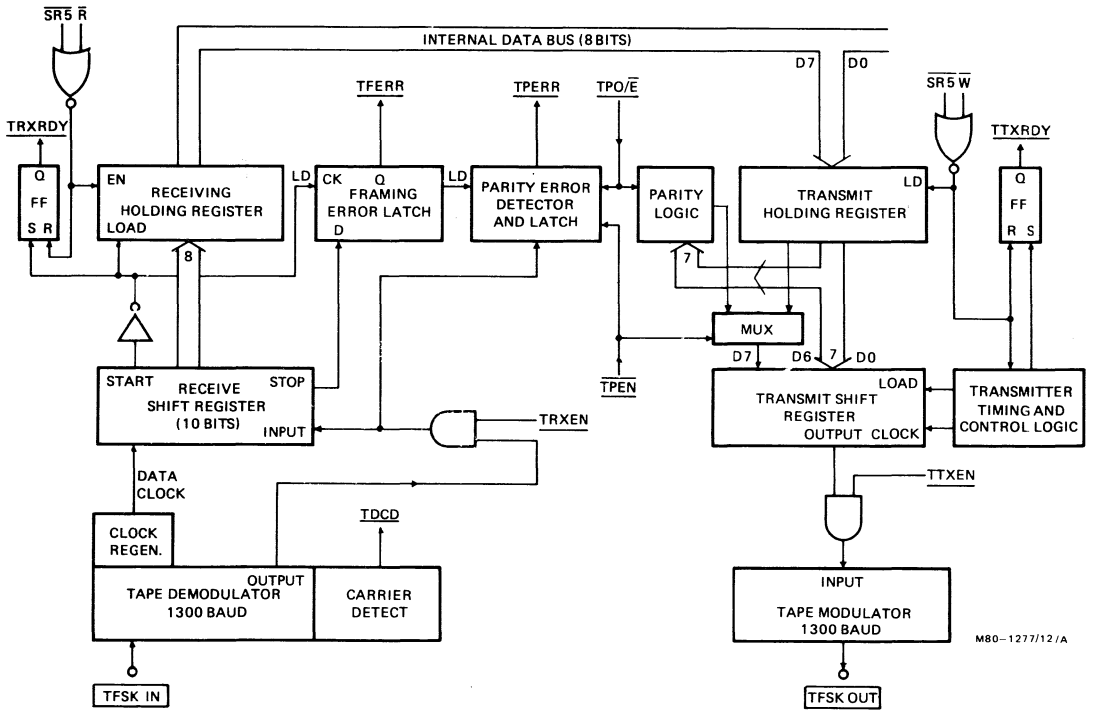


Fig.12 Tape section block diagram

IBUS A receiver and IBUS B receiver/transmitter (see Fig.13)

Associated registers:

Receiver A (2 bytes)	–	R10	–	read only
Receiver B (2 bytes)	–	R11	–	read only
Transmitter B (2 bytes)	–	R11	–	write only

Associated flags in other registers:

IBRXRDY	–	D1	–	R0 (status)	–	valid data available in receiver B holding register
IBTXRDY	–	D0	–	R0 (status)	–	transmitter B holding register ready to accept new data
IARXRDY	–	D1	–	R1 (status)	–	valid data available in receiver A holding register
CLCK IN/$\overline{\text{OUT}}$	–	D1	–	R3 (command)	–	input/output control for 62.5 kHz pin
$\overline{\text{DLEN}}$ A/$\overline{\text{DLIM}}$ A	–	D0	–	R3 (command)	–	3-line/2-line control for IBUS A receiver.

Associated pins:

$\overline{\text{DATA}}$ A	– input	–	receiver A data input
DLIM A/$\overline{\text{DLEN}}$ A	– input	–	receiver A data clock or bus enable signal
$\overline{\text{DATA}}$ B	– I/O	–	receiver B data input/transmitter B data output
DLIM B	– I/O	–	receiver B data clock input/transmitter B data clock output
$\overline{\text{DLEN}}$ B	– I/O	–	receiver B bus enable input/transmitter B bus enable output
IBCLCK	– I/O	–	62.5 kHz clock input/output

Operation

All three IBUS circuits (receiver A, receiver B, and transmitter B) are capable of handling variable length codes from 1 to 12 bits. (In fact 15 bits can be transmitted 12 being data the rest being trailing zero's, and 15 bits may be received but only the last 12 being retained). Each of the three circuits have two 8-bit registers which are accessed by two successive read or write operations to the same address. There is a pointer for each pair of registers which selects the first or second byte. The pointers act in a bistable fashion with each access and are reset to point to the first byte with power on, D5 set in R3, or by reading either of the status registers R0 and R1. The two bytes of data in each holding register contain 12 bits of message, and 4-bits which specify the word length of message. For the transmitter the word length is used to generate the correct number of data clocks, for the receivers it may be used to identify the source of the message, or to establish that the message was a valid length.

The contents of each receiver register pair is organised as:

1st byte	D7	D6	D5	D4	D3	D2	D1	D0
RXA – R10A RXB – R11A	L – 4	L – 5	L – 6	L – 7	L – 8	L – 9	L – 10	L – 11

2nd byte	D7	D6	D5	D4	D3	D2	D1	D0
RXA – R10B RXB – R11B	Word length MSB	Word length	Word length	Word length LSB	L	L – 1	L – 2	L – 3

Where L, L – 1 etc. means last data bit received, last minus one etc.

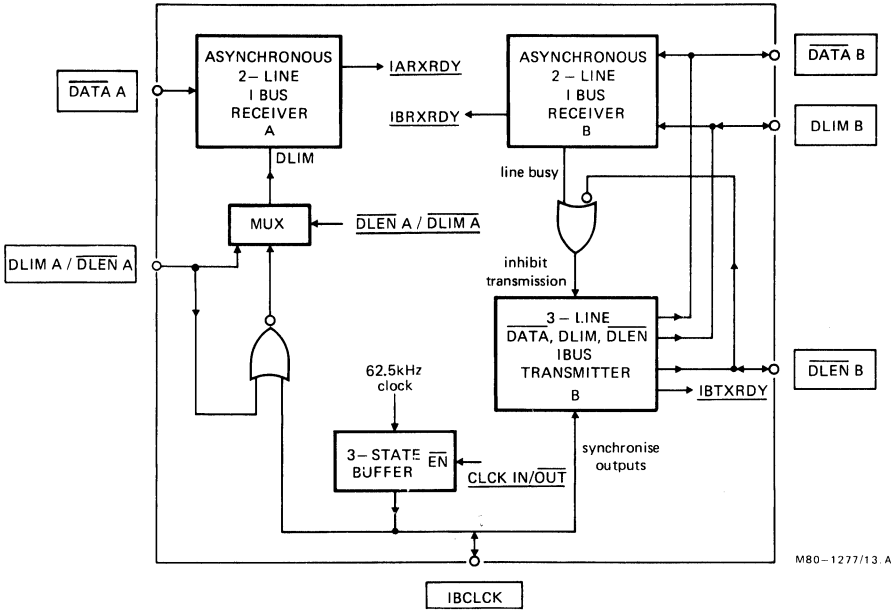


Fig.13 IBUS block diagram

For the transmitter the register pair is organised as:

	D7	D6	D5	D4	D3	D2	D1	D0
1st byte TXB – R11A	8	7	6	5	4	3	2	1

	D7	D6	D5	D4	D3	D2	D1	D0
2nd byte TXB – R11B	Word length MSB	Word length	Word length	Word length LSB	12	11	10	9

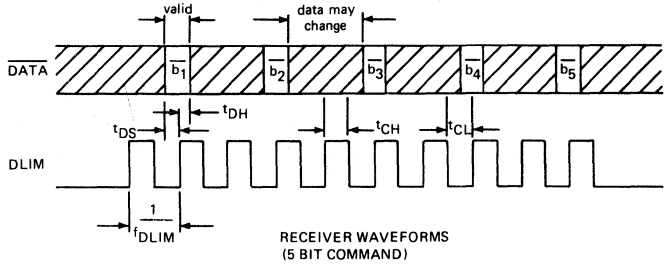
Where 1, 2, etc. means first data bit transmitted, second data bit transmitted, etc.

IARXRDY or IBRXRDY (D1 in status registers R1 and R0) are set when a message has been received by RXA or RXB respectively. These flags also inhibit the receive holding registers from being overwritten by subsequent messages until the holding registers have been read. Reading a holding register pair will reset the relevant IARXRDY or IBRXRDY flags.

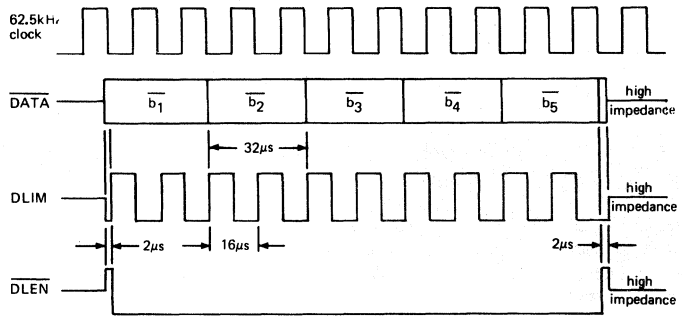
Transmitter B is initiated by writing two bytes to the transmit holding register (R11). This sets IBTXRDY to '0'. The DLIM line is sampled to detect the line busy state, and when the line is free a time out starts. If further DLIM's are detected before the end of the time out period the time out is reset and the sequence will begin again. When the time out has been completed the contents of the holding register are transferred to the output shift register and word length counter. The data and correct number of data clocks are then transmitted, at the completion of which IBTXRDY is returned to a '1'. New data should not be written to the transmit holding register (R11) while IBTXRDY = '0'. If the line is busy when a transmission is requested, the transmission will not start until 300 – 330 μs after the line becomes free (last DLIM). Receiver B is inhibited from receiving data transmitted by transmitter B.

Receiver A may operated either as a two line receiver with $\overline{\text{DATA}}$ and DLIM, or as a three line $\overline{\text{DATA}}$, $\overline{\text{DLEN}}$ and CLK receiver. DLIM A/$\overline{\text{DLEN}}$ A use the same pin, the function of which is selected by the $\overline{\text{DLEN}}$ A/$\overline{\text{DLIM}}$ A command D0, register R3 (command).

The 62.5 kHz clock (pin IBCLCK) may be used either as an input for receiver A (as described above), or to synchronise transmitter B outputs, or as an output synchronous with transmitter B. The function is selected by CLCK IN/$\overline{\text{OUT}}$ command D1 in R3



RECEIVER WAVEFORMS
(5 BIT COMMAND)



TRANSMITTER WAVEFORMS
(5 BIT COMMAND)

MBO-0045/65

Fig. 14 IBUS waveforms

PORT A

Associated register: R6 – bits 0 to 4 – read/write

Associated pins: PA0 to PA4

Operation

This is a 5-bit general purpose input/output port. The outputs are latched and are open drain up to nominal 12 V.

The latches may be accessed by the microprocessor via BUS D0 to D7 by a read or write sequence to register R6. If any pin of the port is used as an input then its output latch must first be written with a '1'. This allows the external circuit to control the pin. The state of the pins may be read by the microprocessor by reading R6. If the supply to the open drain outputs is turned on before the V_{DD} supply to the IC, then the PORT must first be cleared by writing 1's to the output latch before operation.

PORT A might typically be used in viewdata mode as an interface to a non-volatile memory in which telephone and password numbers may be stored.

PORT B

Associated register: R7 – bits 0 to 3 – read/write

Associated pins: PB0 to PB3

Operation

This is a 4-bit general purpose input/output port. It behaves in exactly the same way as PORT A except that access is by addressing R7, and that outputs PB1 to PB3 are open drain to nominal 5 V. PB0 is open drain to nominal 12 V, and might typically be used in combined teletext/viewdata applications to control the Picture On function.

APPENDIX
Register map

	D7	D6	D5	D4	D3	D2	D1	D0	
R0	LTXRDY R	LRXRDY R	LDCD R	LFERR R	LPERR R	LIDCD R	IBRXRDY R	IBTXRDY R	STATUS REGISTER 0
R1	TTXRDY R	TRXRDY R	TDCD R	TFERR R	TPERR R		IARXRDY R		STATUS REGISTER 1
R2	LPO/$\overline{E}$ R/W	$\overline{\text{LPEN}}$ R/W	$\overline{75}$/1200 R/W		TPO/$\overline{E}$ R/W	$\overline{\text{TPEN}}$ R/W			MODE REGISTER
R3	LRXEN R/W	LTXEN R/W	RESET R/W	LDBEN R/W	TRXEN R/W	TTXEN R/W	CLCK IN/$\overline{\text{OUT}}$ R/W	$\overline{\text{DLEN}}$ A/$\overline{\text{DLIM}}$ A R/W	COMMAND REGISTER
R4 R	PARITY OR B8 (R)	B7 R	B6 R	B5 R	B4 R	B3 R	B2 R	B1 R	LINE RECEIVE HOLDING REGISTER
R4 W	PARITY OR B8 (W)	B7 W	B6 W	B5 W	B4 W	B3 W	B2 W	B1 W	LINE TRANSMIT HOLDING REGISTER
R5 R	PARITY OR B8 (R)	B7 R	B6 R	B5 R	B4 R	B3 R	B2 R	B1 R	TAPE RECEIVE HOLDING REGISTER
R5 W	PARITY OR B8 (W)	B7 W	B6 W	B5 W	B4 W	B3 W	B2 W	B1 W	TAPE TRANSMIT HOLDING REGISTER
R6				PA4 R/W	PA3 R/W	PA2 R/W	PA1 R/W	PA0 R/W	PORT A
R7					PB3 R/W	PB2 R/W	PB1 R/W	PB0 R/W	PORT B
R8	UK/$\overline{\text{EUR}}$ R/W	60s TIMER R/W	DIAL GO R/W	1.5s TIMER R/W	DI 3 W	DI 2 W	DI 1 W	DI 0 W	DIAL CONTROL AND TIMING REGISTER
R10 A	B8 R	B7 R	B6 R	B5 R	B4 R	B3 R	B2 R	B1 R	IBUS A REGISTERS
R10 B	– WL3 R	– WL2 R	– WL1 R	– WL0 R	– B12 R	– B11 R	– B10 R	– B9 R	

APPENDIX

Register map (continued)

	D7	D6	D5	D4	D3	D2	D1	D0	
R11 A	B8 R/W	B7 R/W	B6 R/W	B5 R/W	B4 R/W	B3 R/W	B2 R/W	B1 R/W	IBUS B REGISTERS
	—	—	—	—	—	—	—	—	
R11 B	WL3 R/W	WL2 R/W	WL1 R/W	WL0 R/W	B12 R/W	B11 R/W	B10 R/W	B9 R/W	

NOTE R9 is unused.

For details of bit movement in R10 and R11 see discussion of IBUS operation. A mnemonic list for use with this register map and Fig.1b is given on the next page.

MNEMONIC LIST

ALE	address latch enable from microprocessor
CLCK IN/$\overline{\text{OUT}}$	input/output control for 62.5 kHz clock pin
CPNTR	pointer signal for two byte registers
$\overline{\text{DLEN}}$ A/$\overline{\text{DLIM}}$ A	three line/two line control for IBUS A receiver
DON	dial off normal relay control for dialling
IMP	impulsing relay control for dialling
IARXRDY	IBUS A receiver ready – data available
IBRXRDY	IBUS B receiver ready – data available
IBTXRDY	IBUS B transmitter ready – previous transmission complete
LDBEN	line demodulator output buffer enable
LDCD	line data carrier detected
LFERR	line receiver framing error – received stop bit not HIGH
LIDCD	line instantaneous data carrier detect
$\overline{\text{LPEN}}$	line parity enable command
LPERR	line receiver parity error flag
LPO/$\overline{\text{E}}$	line parity odd/even command
LRXEN	line receiver enable
LRXRDY	line receiver ready – data available
LTXEN	line transmitter and modulator enable
LTXRDY	line transmitter ready – transmit holding register empty
$\overline{\text{SR}}$n	select register 'n'
TDCD	tape data carrier detected
TFERR	tape receiver framing error – received stop bit not HIGH
$\overline{\text{TPEN}}$	tape parity enable command
TPERR	tape receiver parity error flag
TPO/$\overline{\text{E}}$	tape parity odd/even command
TRXEN	tape receiver enable
TRXRDY	tape receiver ready – data available
TTXEN	tape transmitter enable
TTXRDY	tape transmitter ready – transmit holding register empty
UK/$\overline{\text{EUR}}$	impulsing ratio control for UK and European standards
$\overline{75}$/1200	baud rate selection command for line modulator and line transmit shift register

TELETEXT VIDEO PROCESSOR

GENERAL DESCRIPTION

The SAA5230 is a bipolar integrated circuit intended as a successor to the SAA5030. It extracts Teletext Data from the video signal, regenerates Teletext Clock and synchronizes the text display to the television syncs. The integrated circuit is intended to work in conjunction with CCT (Computer Controlled Teletext), EUROM or other compatible devices.

Features

- Adaptive data slicer
- Data clock regenerator
- Adaptive sync separator, horizontal phase detector and 6 MHz VCO forming display phase locked loop (PLL)

QUICK REFERENCE DATA

Supply voltage (pin 16)	V_{CC}	typ.	12 V
Supply current (pin 16)	I_{CC}	typ.	70 mA
Video input amplitude (pin 27) (peak-to-peak value)			
pin 2 LOW	$V_{27\text{-}13(p\text{-}p)}$	typ.	1 V
pin 2 HIGH	$V_{27\text{-}13(p\text{-}p)}$	typ.	2,5 V
Storage temperature range	T_{stg}		−20 to + 125 °C
Operating ambient temperature range	T_{amb}		−20 to + 70 °C

PACKAGE OUTLINE

28-lead DIL; plastic (SOT-117).

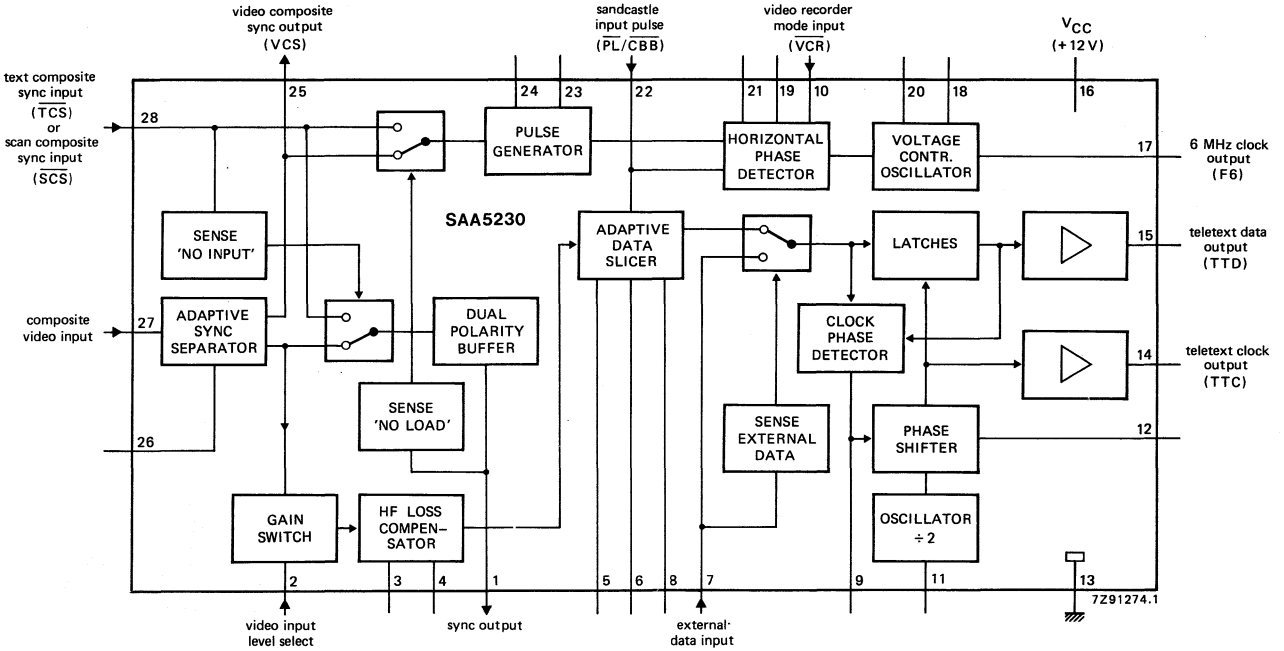


Fig. 1 Block diagram.

PINNING

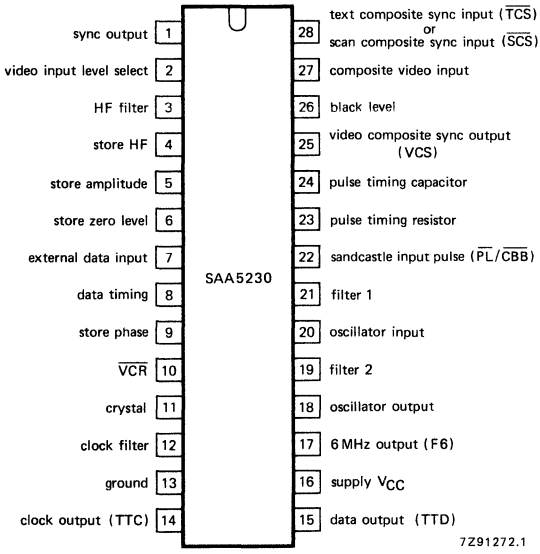


Fig. 2 Pinning diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 16)	V_{CC}	max.	13,2 V
Storage temperature range	T_{stg}		−20 to + 125 °C
Operating ambient temperature	T_{amb}		−20 to + 70 °C

CHARACTERISTICS

V_{CC} = 12 V; T_{amb} = 25 °C with external components as shown in Fig. 3a or Fig. 3b unless otherwise stated.

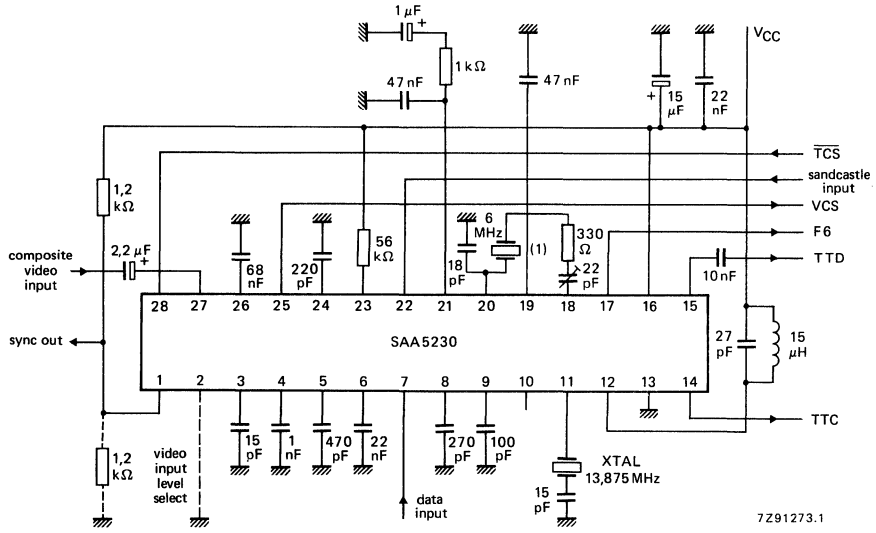
parameter	symbol	min.	typ.	max.	unit
Supply (pin 16)					
Supply voltage	V_{CC}	10,8	12,0	13,2	V
Supply current	I_{CC}	–	70	–	mA
Video input and sync separator					
Video input amplitude (sync to white) (peak-to-peak value)					
video input select level LOW (pin 2)	$V_{27\text{-}13(p\text{-}p)}$	0,7	1	1,4	V
video input select level HIGH (pin 2)	$V_{27\text{-}13(p\text{-}p)}$	1,75	2,5	3,5	V
Source impedance	$\lvert Z_s \rvert$	–	–	250	Ω
Sync amplitude (peak-to-peak value)	$V_{27\text{-}13(p\text{-}p)}$	0,1	–	1	V
Video input level select					
Input voltage LOW	$V_{2\text{-}13}$	0	–	0,8	V
Input voltage HIGH	$V_{2\text{-}13}$	2,0	–	5,5	V
Input current LOW	I_2	0	–	−150	μA
Input current HIGH	I_2	0	–	1	mA
Text composite sync input ($\overline{TCS}$)					
Input voltage LOW	$V_{28\text{-}13}$	0	–	0,8	V
Input voltage HIGH	$V_{28\text{-}13}$	2,0	–	7,0	V
Scan composite sync input ($\overline{SCS}$)					
Input voltage LOW	$V_{28\text{-}13}$	0	–	1,5	V
Input voltage HIGH	$V_{28\text{-}13}$	3,5	–	7,0	V
Select video sync from pin 1					
Input current (pin 28)					
at V_I = 0 to 7 V	I_{28}	−40	−70	−100	μA
at V_I = 10 V to V_{CC}	I_{28}	−5	–	+ 5	μA
Video composite sync output (VCS)					
Output voltage LOW	$V_{25\text{-}13}$	0	–	0,4	V
Output voltage HIGH	$V_{25\text{-}13}$	2,4	–	5,5	V
D.C. output current LOW	I_{25}	–	–	0,5	mA
D.C. output current HIGH	I_{25}	–	–	−1,5	mA
Sync separator delay time	t_d	–	0,35	–	μs

parameter	symbol	min.	typ.	max.	unit
Dual polarity buffer output					
$\overline{TCS}$ amplitude (peak-to-peak value)	$V_{1\text{-}13(p\text{-}p)}$	–	0,45	–	V
Video sync amplitude (peak-to-peak value)	$V_{1\text{-}13(p\text{-}p)}$	–	–	1	V
Output current	I_1	−3	–	+ 3	mA
D.C. output voltage					
R_L to ground (0 V)	$V_{1\text{-}13}$	–	1,4	–	V
R_L to V_{CC} (12 V)	$V_{1\text{-}13}$	–	10,1	–	V
Sandcastle input pulse ($\overline{PL}$/$\overline{CBB}$)					
Phase lock pulse (PL)					
PL on (LOW)	$V_{22\text{-}13}$	0	–	3	V
PL off (HIGH)	$V_{22\text{-}13}$	3,9	–	5,5	V
Blanking pulse (CBB)					
CBB on (LOW)	$V_{22\text{-}13}$	0	–	0,5	V
CBB off (HIGH)	$V_{22\text{-}13}$	1,0	–	5,5	V
Input current	I_{22}	−10	–	+ 10	μA
Phase locked loop (PLL)					
Phase detector timing					
Pulse duration using composite video	t_p	–	2	–	μs
using scan composite sync	t_p	–	3	–	μs
time PL must be LOW to make VCO run-free	t_L	100	–	–	μs
6 MHz clock output (F6)					
A.C. output voltage (peak-to-peak value)	$V_{17\text{-}13(p\text{-}p)}$	1	2	3	V
A.C. and d.c. output voltage range	$V_{17\text{-}13(max)}$	4	–	8,5	V
Rise and fall time	t_r; t_f	20	–	40	ns
Load capacitance	$C_{17\text{-}13}$	–	–	40	pF
Video recorder mode input ($\overline{VCR}$)					
VCR-mode on (LOW)	$V_{10\text{-}13}$	0	–	0,8	V
VCR-mode off (HIGH)	$V_{10\text{-}13}$	2,0	–	V_{CC}	V
Input current	I_{10}	−10	–	+ 10	μA

CHARACTERISTICS (continued)

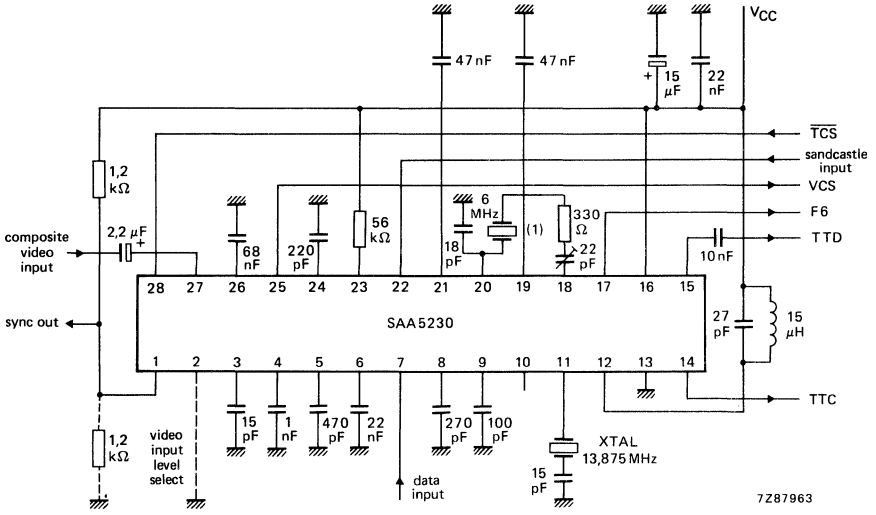
parameter	symbol	min.	typ.	max.	unit
Data slicer					
Data amplitude of video input (pin 27)					
video input level select LOW (pin 2)	$V_{27\text{-}13}$	0,30	0,46	0,70	V
video input level select HIGH (pin 2)	$V_{27\text{-}13}$	0,75	1,15	1,75	V
Teletext clock output					
A.C. output voltage (peak-to-peak value)	$V_{14\text{-}13(p\text{-}p)}$	2,5	3,5	4,5	V
D.C. output voltage (centre)	$V_{14\text{-}13}$	–	4	–	V
Load capacitance	C_L	–	–	40	pF
Rise and fall times	$t_r; t_f$	20	30	45	ns
Delay of falling edge relative to other edges of TTD	t_d	−20	0	+ 20	ns
Teletext data output					
A.C. output voltage (peak-to-peak value)	$V_{15\text{-}13(p\text{-}p)}$	2,5	3,5	4,5	V
D.C. output voltage (centre)	$V_{15\text{-}13}$	–	4	–	V
Load capacitance	C_L	–	–	40	pF
Rise and fall times	$t_r; t_f$	20	30	45	ns

APPLICATION INFORMATION



(1) Ceramic resonator e.g. Kyocera KBR 6,0M. Adjust the free-running frequency to 6010 kHz ± 5 kHz.

Fig. 3a Application circuit using ceramic resonator in PLL.



(1) Quartz crystal e.g. catalogue number 4322 143 04101. Adjust the free-running frequency to 6000,2 kHz ± 0,2 kHz.

Fig. 3b Application circuit using quartz crystal in PLL.

APPLICATION INFORMATION (continued)

Component specifications

Specifications of some external components in Fig. 3a and Fig. 3b.

Ceramic resonator (preferred type KBR 6,0 M, Kyocera; Fig. 3a)

Load resonance frequency (f) 6 MHz; adjustment tolerance ± 0,5%
Load capacitance (C_L) 20 pF
Temperature range (T) −20 to + 70 °C; frequency tolerance ± 0,3% max.
Resonance resistance (R_r) 6 Ω typ.
Motional capacitance (C_1) 9 pF typ.
Static parallel capacitance (C_o) 60 pF typ.
Ageing (10 years) f ± 0,3% max.

Quartz crystal

Load resonance frequency (f) 13,875 MHz; adjustment tolerance ± $40 \cdot 10^{-6}$
Load capacitance (C_L) 20 pF
Temperature range (T) −20 to + 70 °C; frequency tolerance ± $30 \cdot 10^{-6}$ max.
Resonance resistance (R_r) 10 Ω typ. 60 Ω max.
Motional capacitance (C_1) 19 fF typ.
Static parallel capacitance (C_o) 5 pF typ.

Fixed inductance

Inductance (L) 15 μH ± 20%
Quality factor (Q) 20 min.

Quartz crystal (preferred type catalogue number 4322 143 04101; Fig. 3b)

Load resonance frequency (f) 6 MHz; adjustment tolerance ± $40 \cdot 10^{-6}$
Load capacitance (C_L) 20 pF
Temperature range (T) −20 to + 70 °C; frequency tolerance ± $30 \cdot 10^{-6}$ max.
Resonance resistance (R_r) 60 Ω
Motional capacitance (C_1) 28 fF typ.
Static parallel capacitance (C_o) 7 pF typ.

The function is quoted against the corresponding pin number.

1. **Synch output to TV**

   Output with dual polarity buffer, a load resistor to 0 V or + 12 V selects positive-going or negative-going syncs.

2. **Video input level select**

   When this pin is LOW a 1 V video input level is selected. When the pin is not connected it floats HIGH selecting a 2,5 V video input level.

3. **HF filter**

   The video signal for the h.f.-loss compensator is filtered by a 15 pF capacitor connected to this pin.

4. **Store h.f.**

   The h.f. amplitude is stored by a 1 nF capacitor connected to this pin.

5. **Store amplitude**

   The amplitude for the adaptive data slicer is stored by a 470 pF capacitor connected to this pin.

6. **Store zero level**

   The zero level for the adaptive data slicer is stored by a 22 nF capacitor connected to this pin.

7. **External data input**

   Current input for sliced teletext data from external device.
   Active HIGH level (current), low impedance input.

8. **Data timing**

   A 270 pF capacitor is connected to this pin for timing of the adaptive data slicer.

9. **Store phase**

   The output signal from the clock phase detector is stored by a 100 pF capacitor connected to this pin.

10. **Video tape recorder mode ($\overline{\text{VCR}}$)**

    Signal input to command PLL into short time constant mode. Not used in application circuit Fig. 3a or Fig. 3b.

11. **Crystal**

    A 13,875 MHz crystal, 2 x data rate, connected in series with a 15 pF capacitor is applied via this pin to the oscillator and divide-by-two to provide the 6,9375 MHz clock signal.

12. **Clock filter**

    A filter for the 6,9375 MHz clock signal is connected to this pin.

13. **Ground (0 V)**

14. **Teletext clock output (TTC)**

    Clock output for CCT (Computer Controlled Teletext).

APPLICATION INFORMATION (continued)

15. **Teletext data output (TTD)**

Data output for CCT.

16. **Supply voltage V_{CC} (+ 12 V typ.)**

17. **Clock output (F6)**

6 MHz clock output for timing and sandcastle generation in CCT.

18. **Oscillator output (6 MHz)**

A series resonant circuit is connected between this pin and pin 20 to control the nominal frequency of the VCO.

19. **Filter 2**

A filter with a short time constant is connected to this pin for the horizontal phase detector. It is used in the video recorder mode and while the loop is locking up.

20. **Oscillator input (6 MHz)**

See pin 18.

21. **Filter 1**

A filter with a long time constant is connected to this pin for the horizontal phase detector.

22. **Sandcastle input pulse ($\overline{PL}/\overline{CBB}$)**

This input accepts a sandcastle waveform, which is formed from PL and CBB from the CCT. Signal timing is shown in Fig. 4.

23. **Pulse timing resistor**

The current for the pulse generator is defined by a 56 kΩ resistor connected to this pin.

24. **Pulse timing capacitor**

The timing of the pulse generator is determined by a 220 pF capacitor connected to this pin.

25. **Video composite sync output (VCS)**

This output signal is for CCT.

26. **Black level**

The black level for the adaptive sync separator is stored by a 68 nF capacitor connected to this pin.

27. **Composite video input (CVS)**

The composite video signal is input via a 2,2 μF clamping capacitor to the adaptive sync separator.

28. **Text composite sync input ($\overline{\text{TCS}}$)/Scan composite sync input ($\overline{\text{SCS}}$)**

$\overline{\text{TCS}}$ is input from CCT or $\overline{\text{SCS}}$ from external sync circuit. $\overline{\text{SCS}}$ is expected when there is no load resistor at pin 1. If pin 28 is not connected the sync output on pin 1 will be the composite video input at pin 27, internally buffered.

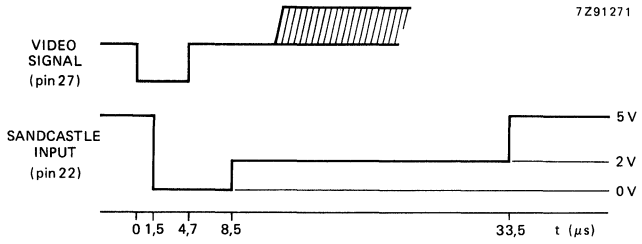


Fig. 4 Sandcastle waveform and timing.

EUROPEAN COMPUTER CONTROLLED TELETEXT CIRCUIT (EURO CCT)

GENERAL DESCRIPTION

The SAA5240 is a MOS N-channel integrated circuit which performs all the digital logic functions of a 625-line World System Teletext decoder. It operates in conjunction with the teletext video processor SAA5230, standard static RAM's and is controlled via the 2-wire I²C bus. The device can be used to provide videotex display conforming to a serial character attribute protocol.

Features

- Microcomputer controlled for flexibility
- High quality flicker-free display using a 12 x 10 character matrix
- Field flyback (lines 6 to 22), or full channel (all lines) data acquisition
- Up to four simultaneous page requests enabling acquisition during one magazine cycle
- Direct interface up to 8 K bytes static RAM
- Automatic language selection of up to three different languages
- 25th display row for software generated status messages
- Cursor control for videotex/telesoftware
- 7-bits parity or 8-bit data acquisition
- Ghost row reception option (extension packets)
- Standard I²C bus slave transceiver (slave address 0010001)
- Single 5 volt power supply
- Mask programmable character sets:
  SAA5240A; English, German, Swedish
  SAA5240B; Italian , German, French

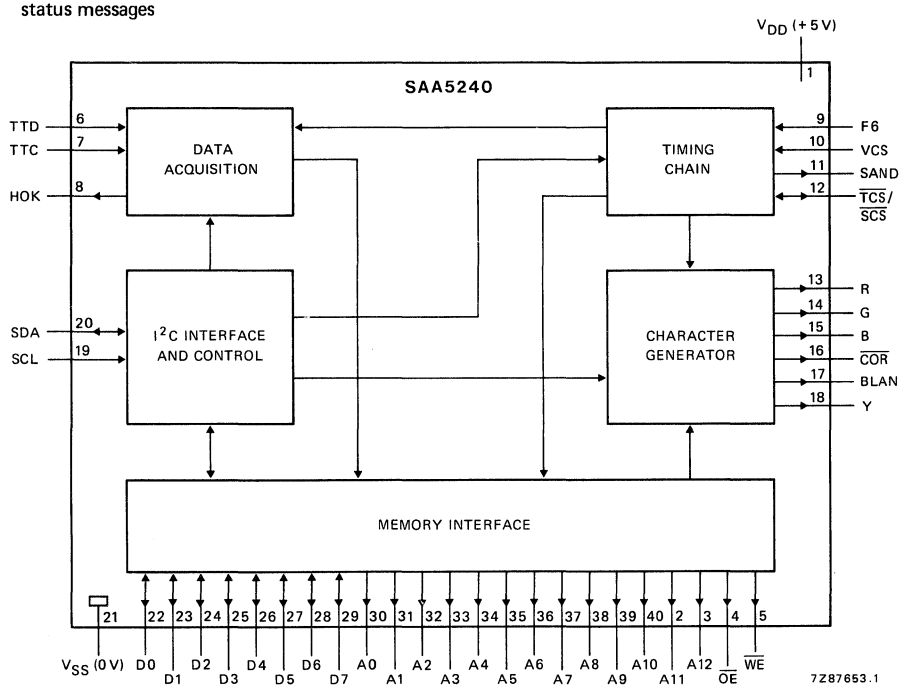


Fig. 1 Block diagram.

PACKAGE OUTLINES 40-lead DIL; plastic (SOT-129).

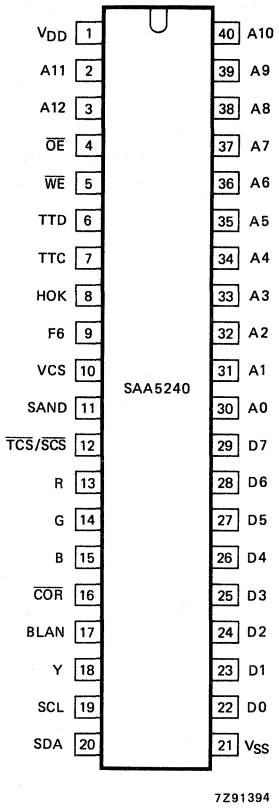


Fig. 2 Pinning diagram.

PINNING

1	V_{DD}	**Power supply**: + 5 V power supply pin.
2, 3, 40	A11, A12, A10	**Chapter Address**: three outputs that select which 1 K byte chapter of external RAM is being accessed for any read or write cycle.
4	$\overline{OE}$	**Output Enable**: active low output signal used to control the reading of the external RAM. It occurs continuously at a 1 MHz rate.
5	$\overline{WE}$	**Write Enable**: active low output signal used to control the writing of data to the external RAM. It occurs for a valid write cycle only and is interleaved with the read cycles.
6	TTD	**Teletext Data**: input from the SAA5230 Video Input Processor (VIP2). It is clamped to V_{SS} for 4 to 8 μs of each television line to maintain the correct d.c. level following the external a.c. coupling.

7	TTC	**Teletext Clock**: 6,9375 MHz clock input from the SAA5230. It is internally a.c. coupled to an active clamp input buffer.
8	HOK	**Hamming O.K.**: an active high output signal indicating reception of a valid teletext data line with no Hamming errors in the magazine or row bytes. It is reset at line rate.
9	F6	**Character display clock**: 6 MHz clock input from the SAA5230. It is internally a.c. coupled to an active clamp input buffer.
10	VCS	**Video Composite Sync**: input from the SAA5230 derived from the incoming video signal. Sync pulses are active high.
11	SAND	**Sandcastle**: 3-level sandcastle output to the SAA5230 containing the phase locking and colour burst blanking information.
12	$\overline{TCS}/\overline{SCS}$	**Text Composite Sync/Scan Composite Sync**: as an output an active low composite sync waveform (TCS) with interlaced or non-interlaced format (see Fig. 6) which is fed to the SAA5230 to drive the display timebases. Alternatively this pin can act as an input for an active low composite sync waveform (SCS) to 'slave' the display timing circuits.
13, 14, 15	R, G, B	**Red, Blue, Green**: these 3 open drain outputs are the character video signals to the television display circuits. They are active high and contain character and background information.
16	$\overline{COR}$	**Contrast Reduction**: open drain, active low output which allows selective contrast reduction of the television picture to enhance a mixed mode display.
17	BLAN	**Blanking**: open drain, active high output which controls the blanking of the television picture for a normal text display and for a mixed display.
18	Y	**Character foreground**: open drain, active high video output signal containing all the foreground information displayed on the television screen (e.g. for driving a display printer).
19	SCL	**Serial Clock**: input signal which is the I^2C bus clock from the microcontroller.
20	SDA	**Serial Data**: is the I^2C bus data line. It is an input/output function with an open drain output.
21	V_{SS}	**Ground**: 0 volts.
22-29	DO-D7	**8 RAM data lines**: 3-state input/output pins which carry the data bytes to and from the external RAM.
30-39	A0-A9	**RAM address**: 10 output signals that determine which byte location within a 1 K byte chapter of external RAM is accessed for any read or write cycle.

DEVELOPMENT DATA

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range (pin 1)	V_{DD}	−0,3 to + 7,5	V
Input voltage range			
VCS, SDA, SCL, D0-D7	V_I	−0,3 to + 7,5	V
→ TTC, TTD, F6, $\overline{TCS}/\overline{SCS}$	V_I	−0,3 to + 10,0	V
Output voltage range			
→ SAND, A0-A12, $\overline{OE}$, $\overline{WE}$, D0-D7, SDA, HOK, R, G, B, BLAN, $\overline{COR}$, Y	V_O	−0,3 to + 7,5	V
→ $\overline{TCS}/\overline{SCS}$	V_O	−0,3 to + 10,0	V
Storage temperature range	T_{stg}	−20 to + 125	°C
Operating ambient temperature range	T_{amb}	−20 to + 70	°C

CHARACTERISTICS

V_{DD} = 5 V; V_{SS} = 0 V; T_{amb} = 25 °C unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
SUPPLY					
Supply voltage (pin 1)	V_{DD}	4,5	5,0	5,5	V
Supply current (pin 1)	I_{DD}	–	160	–	mA
INPUTS (note 1)					
TTD (note 2)					
External coupling capacitor	C_{ext}	–	–	50	nF
Input voltage (peak-to-peak value)	$V_{I(p-p)}$	2,0	–	7,0	V
Input data rise and fall times (note 3)	t_r, t_f	10	–	80	ns
Input data set-up time (note 4)	t_{DS}	40	–	–	ns
Input data hold time (note 4)	t_{DH}	40	–	–	ns
Input leakage current at V_I = 0 to 10 V	I_{LI}	–	–	20	μA
Input capacitance	C_I	–	–	7	pF
TTC; F6 (note 5)					
D.C. input voltage range	V_I	–0,3	–	+ 10,0	V
A.C. input voltage (peak-to-peak value)	$V_{I(p-p)}$	1,0	–	7,0	V
Input peaks relative to 50% duty cycle	± V_P	0,2	–	3,5	V
TTC clock frequency	f_{TTC}	–	6,9375	–	MHz
F6 clock frequency	f_{F6}	–	6,0	–	MHz
Clock rise and fall times (note 3)	t_r, t_f	10	–	80	ns
Input leakage current at V_I = 0 to 10 V	I_{LI}	–	–	20	μA
Input capacitance	C_I	–	–	7	pF
VCS					
Input voltage LOW	V_{IL}	0	–	0,8	V
Input voltage HIGH	V_{IH}	2,0	–	V_{DD}	V
Input rise and fall times (note 3)	t_r, t_f	–	–	500	ns
Input leakage current at V_I = 5,5 V	I_{LI}	–	–	10	μA
Input capacitance	C_I	–	–	7	pF

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
SCL					
Input voltage LOW	V_{IL}	0	–	1,5	V
Input voltage HIGH	V_{IH}	3,0	–	V_{DD}	V
SCL clock frequency	f_{SCL}	0	–	100	kHz
Input rise and fall times (note 3)	t_r, t_f	–	–	2	μs
Input leakage current at V_I = 5,5 V	I_{LI}	–	–	10	μA
Input capacitance	C_I	–	–	7	pF
INPUT/OUTPUTS (note 6)					
$\overline{TCS}$ (output)/$\overline{SCS}$ (input)					
Input voltage LOW	V_{IL}	0	–	1,5	V
Input voltage HIGH	V_{IH}	3,5	–	10,0	V
Input rise and fall times (note 3)	t_r, t_f	–	–	500	ns
Input leakage current at V_I = 0 to 10 V and output in high impedance state	$\pm I_{LI}$	–	–	10	μA
Input capacitance	C_I	–	–	7	pF
Output voltage LOW at I_{OL} = 1,6 mA	V_{OL}	0	–	0,4	V
Output voltage HIGH at $-I_{OH}$ = 0,2 mA	V_{OH}	2,4	–	V_{DD}	V
at I_{OH} = 0,1 mA	V_{OH}	2,4	–	6,0	V
Output rise and fall times between 0,6 V and 2,2 V levels	t_r, t_f	–	–	100	ns
Load capacitance	C_L	–	–	50	pF
SDA (note 7)					
Input voltage LOW	V_{IL}	0	–	1,5	V
Input voltage HIGH	V_{IH}	3,0	–	V_{DD}	V
Input rise and fall times (note 3)	t_r, t_f	–	–	2	μs
Input leakage current at V_I = 5,5 V with output off	I_{LI}	–	–	10	μA
Input capacitance	C_I	–	–	7	pF
Output voltage LOW at I_{OL} = 3 mA	V_{OL}	0	–	0,5	V
Output fall time between 3,0 V and 1,0 V levels	t_f	–	–	200	ns
Load capacitance	C_L	–	–	400	pF

parameter	symbol	min.	typ.	max.	unit
INPUT/OUTPUTS (continued)					
D0-D7 (note 8)					
Input voltage LOW	V_{IL}	0	–	0,8	V
Input voltage HIGH	V_{IH}	2,0	–	V_{DD}	V
Input leakage current at V_I = 0 V to 5,5 V and output in high impedance state	$\pm I_{LI}$	–	–	10	μA
Input capacitance	C_I	–	–	7	pF
Output voltage LOW at I_{OL} = 1,6 mA	V_{OL}	0	–	0,4	V
Output voltage HIGH at $-I_{OH}$ = 0,2 mA	V_{OH}	2,4	–	V_{DD}	V
Output rise and fall times between 0,6 V and 2,2 V levels	t_r, t_f	–	–	50	ns
Load capacitance	C_L	–	–	120	pF
OUTPUTS (note 6)					
A0-A12; $\overline{OE}$; $\overline{WE}$ (note 8)					
Output voltage LOW at I_{OL} = 1,6 mA	V_{OL}	0	–	0,4	V
Output voltage HIGH at $-I_{OH}$ = 0,2 mA	V_{OH}	2,4	–	V_{DD}	V
Output rise and fall times between 0,6 V and 2,2 V levels	t_r, t_f	–	–	50	ns
Load capacitance	C_L	–	–	120	pF
HOK (note 9)					
Output voltage LOW at I_{OL} = 1,6 mA	V_{OL}	0	–	0,4	V
Output voltage HIGH at $-I_{OH}$ = 0,2 mA	V_{OH}	2,4	–	V_{DD}	V
Output rise and fall times between 0,6 V and 2,2 V levels	t_r, t_f	–	–	100	ns
Load capacitance	C_L	–	–	50	pF
SAND (note 9)					
Output voltage LOW at I_{OL} = 0,2 mA	V_{OL}	0	–	0,2	V
Output voltage INTERMEDIATE at I_{OL} = ± 30 μA	V_{OI}	1,3	–	2,7	V

DEVELOPMENT DATA

CHARACTERISTICS (continued)

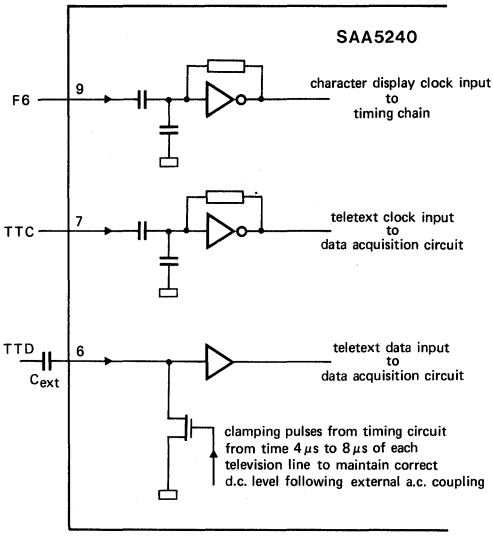
parameter	symbol	min.	typ.	max.	unit
SAND (continued)					
Output voltage HIGH at I_{OH} = 0 to −30 μA	V_{OH}	4,2	–	V_{DD}	V
Output rise time V_{OL} to V_{OI} between 0,4 V and 1,1 V levels	t_{r1}	–	–	400	ns
Output rise time V_{OI} to V_{OH} between 2,9 V and 4,0 V levels	t_{r2}	–	–	200	ns
Output fall time V_{OH} to V_{OL} between 4,0 V and 0,4 V levels	t_f	–	–	50	ns
Load capacitance	C_L	–	–	30	pF
R; G; B; $\overline{\text{COR}}$; BLAN; Y (note 10)					
Output voltage LOW at I_{OL} = 2 mA	V_{OL}	0	–	0,4	V
Output voltage LOW at I_{OL} = 5 mA	V_{OL}	0	–	1,0	V
Pull-up voltage as seen at pin	V_{PU}	–	–	6,0	V
Output fall time with a load resistor of 1,2 kΩ to 6 V and measured between 5,5 V and 1,5 V	t_f	–	–	20	ns
Skew delay between outputs with a load resistor of 1,2 kΩ to 6 V and measured on the falling edges at 3,5 V	t_{SK}	–	–	20	ns
Load capacitance	C_L	–	–	25	pF
Output leakage current at V_{PU} = 0 to 6 V with output off	I_{LO}	–	–	10	μA
TIMING					
I²C bus (note 11)					
Clock low period	t_{LOW}	4	–	–	μs
Clock high period	t_{HIGH}	4	–	–	μs
Data set-up time	$t_{SU;DAT}$	250	–	–	ns
→ Data hold time	$t_{HD;DAT}$	170	–	–	ns
Stop set-up time from clock high	$t_{SU;STO}$	4	–	–	μs
Start set-up time following a stop	t_{BUF}	4	–	–	μs
Start hold time	$t_{HD;STA}$	4	–	–	μs
Start set-up time following clock low to high transition	$t_{SU;STA}$	4	–	–	μs

parameter	symbol	min.	typ.	max.	unit
TIMING (continued)					
Memory interface (note 12)					
Cycle time	t_{CY}	–	500	–	ns
Address change to $\overline{OE}$ LOW	t_{OE}	60	–	–	ns
Address active time	t_{ADDR}	450	500	–	ns
$\overline{OE}$ pulse duration	t_{OEW}	320	–	–	ns
Access time from $\overline{OE}$ to data valid	t_{ACC}	–	–	200	ns
Data hold time from $\overline{OE}$ HIGH or address change	t_{DH}	0	–	–	ns
Address change to $\overline{WE}$ LOW	t_{WE}	40	–	–	ns
$\overline{WE}$ pulse duration	t_{WEW}	200	–	–	ns
Data set-up time to $\overline{WE}$ HIGH	t_{DS}	100	–	–	ns
Data hold time from $\overline{WE}$ HIGH	t_{DHWE}	20	–	–	ns
Write recovery time	t_{WR}	25	–	–	ns

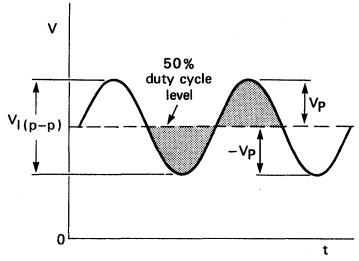
DEVELOPMENT DATA

Notes to the characteristics

1. All inputs are protected against static charge under normal handling.
2. The TTD input incorporates an internal clamping diode in addition to the active clamping transistor (see Fig. 3).
3. Rise and fall times between 10% and 90% levels.
4. Teletext input data set-up and hold times are with respect to a 50% duty cycle level of the rising edge of the teletext clock input (TTC). Data stable 1 $\geqslant$ 2,0 V; data stable 0 $\leqslant$ 0,8 V (see Fig. 4).
5. The TTC and F6 inputs have internal clamping diodes and are a.c. coupled (see Fig. 3).
6. All outputs and input/outputs are protected against static charge under normal handling and connection to V_{DD} and V_{SS}.
7. For details of I^2C bus timing see Fig. 8.
8. For details of RAM timing see Fig. 9.
9. For details of synchronization and HOK timing see Fig. 5.
10. For details of display output timing see Fig. 7.
11. The I^2C bus timings are referred to V_{IH} = 3 V and V_{IL} = 1,5 V. For waveforms see Fig. 8.
12. The memory interface timings are referred to V_{IL} = 1,5 V. For waveforms see Fig. 9.



(a)

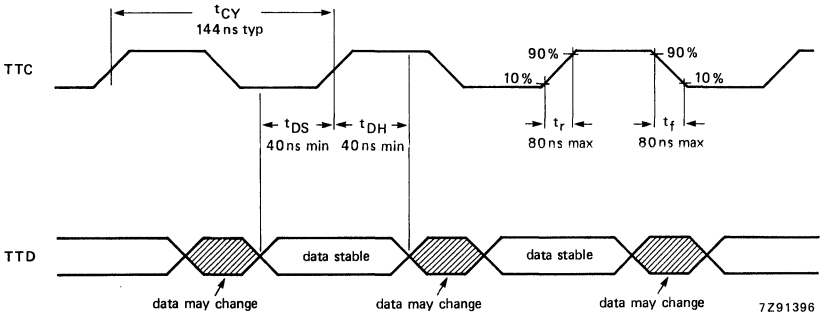


shaded regions equal in area

7Z91395

(b)

Fig. 3 (a) F6, TTC and TTD input circuitry (b) input waveform parameters.



Data stable: 1 is $\geqslant$ 2,0 V; 0 is $\leqslant$ 0,8 V.

Fig. 4 Teletext data input timing.

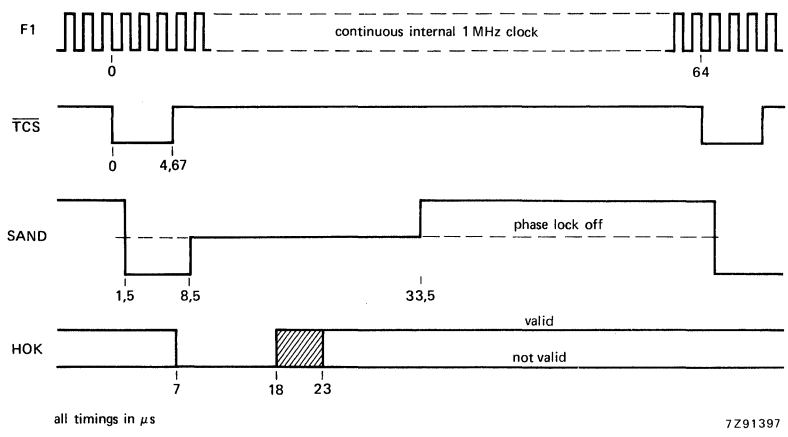
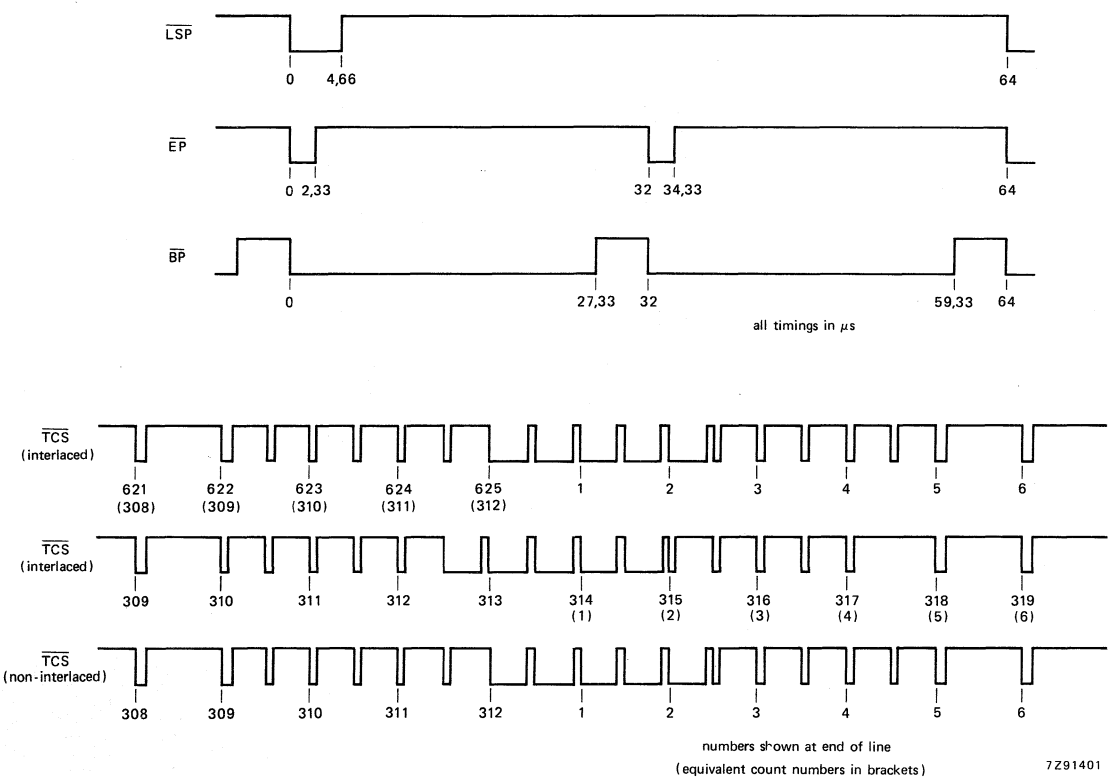


Fig. 5 Synchronization and HOK timing.



Line sync pulses ($\overline{LSP}$), equalizing pulses ($\overline{EP}$) and broad pulses ($\overline{BP}$) are combined to provide the text composite sync waveform ($\overline{TCS}$) as shown. All timings measured from falling edge of $\overline{LSP}$ with a tolerance of ± 100 ns.

Fig. 6 Composite sync waveforms.

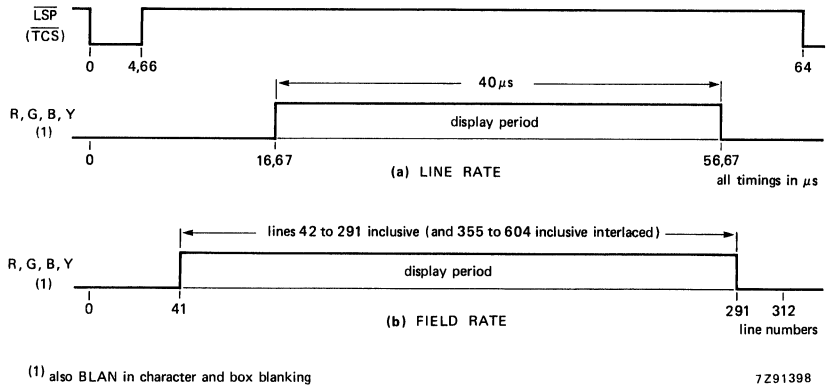


Fig. 7 Display output timing (a) line rate (b) field rate.

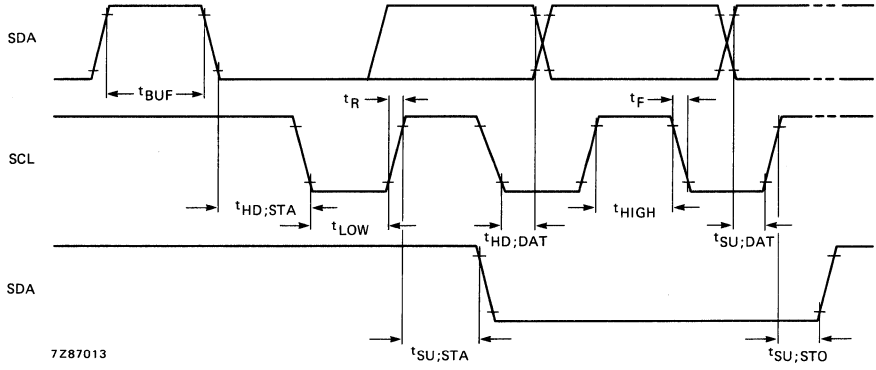


Fig. 8 I²C bus timing.

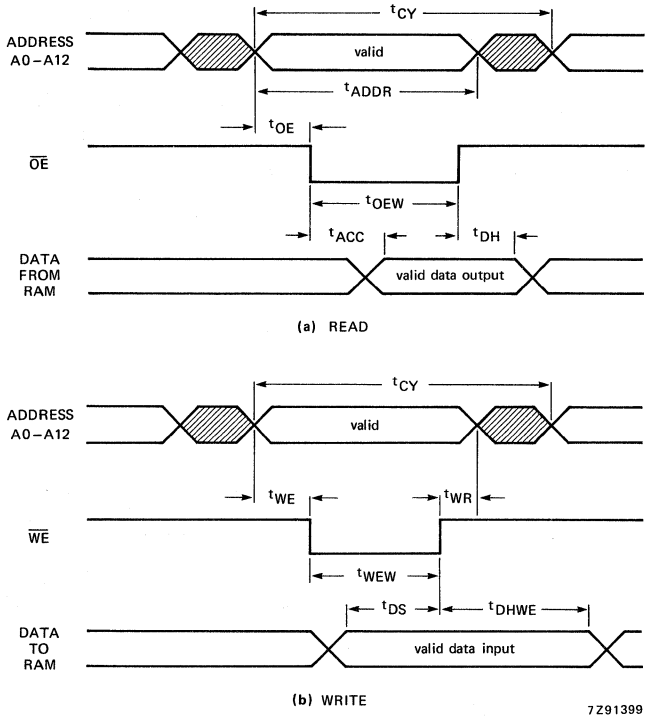


Fig. 9 Memory interface timing (a) read (b) write.

APPLICATION INFORMATION

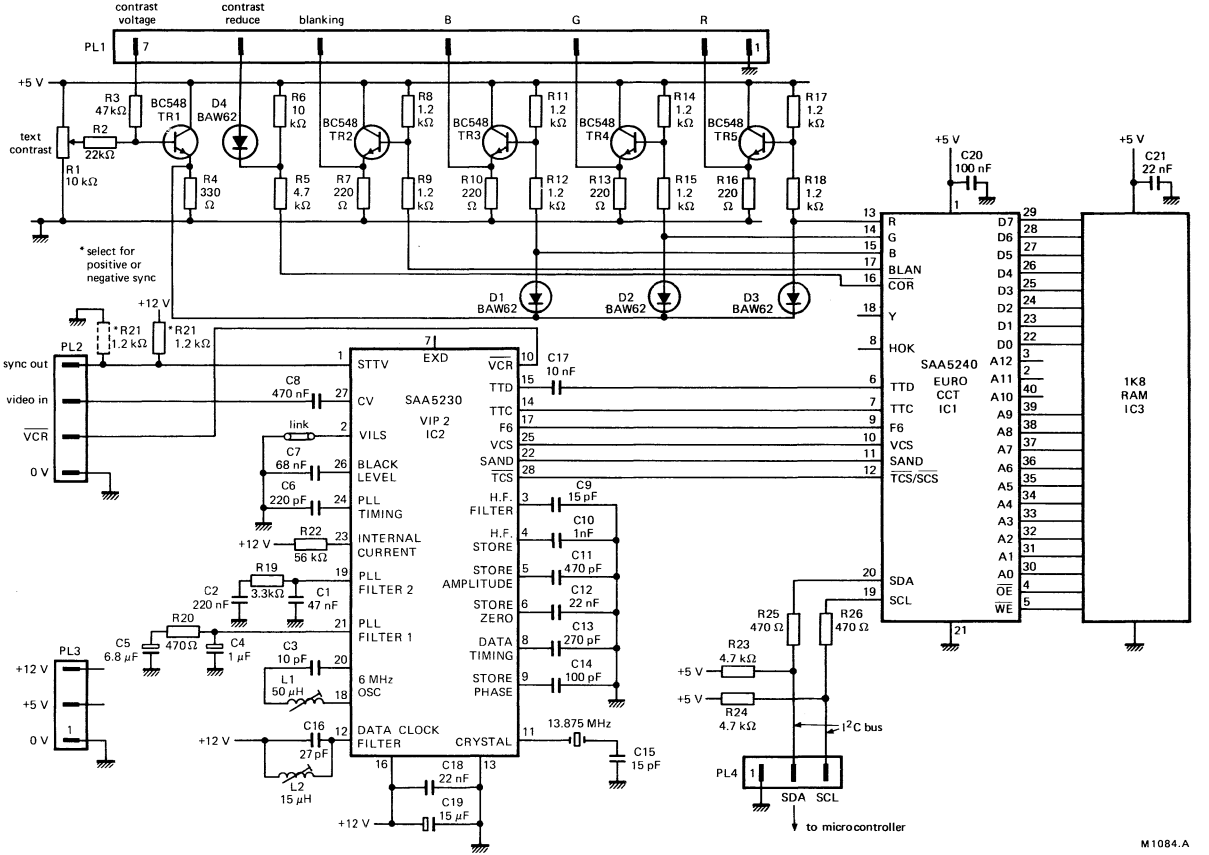


Fig. 10 EURO CCT based single-page decoder circuit diagram.

APPLICATION INFORMATION (continued)

EURO CCT page memory organization

The organization of a page memory is shown in Fig. 11. The EURO CCT provides an additional row compared with first generation decoders bringing the display format up to 40 characters by 25 rows. Rows 0 to 23 form the teletext page as broadcast and row 24 is the extra row available for user-generated status messages.

A MORE DETAILED DESCRIPTION OF CCT OPERATION AND APPLICATION IS AVAILABLE ON REQUEST.

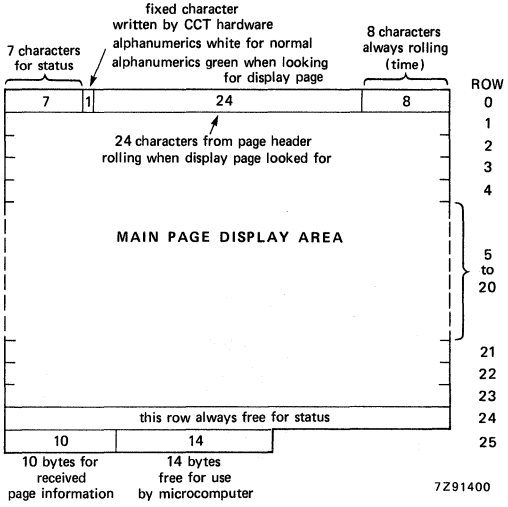


Fig. 11 Page memory organization.

Table 1 Row 25 received control data format

D0	PU0	PT0	MU0	MT0	HU0	HT0	C7	C11	MAG0	0
D1	PU1	PT1	MU1	MT1	HU1	HT1	C8	C12	MAG1	0
D2	PU2	PT2	MU2	MT2	HU2	C5	C9	C13	MAG2	0
D3	PU3	PT3	MU3	C4	HU3	C6	C10	C14	0	0
D4	HAM.ER	HAM.ER	HAM.ER	HAM.ER	HAM.ER	HAM.ER	HAM.ER	HAM.ER	$\overline{\text{FOUND}}$	0
D5	0	0	0	0	0	0	0	0	0	PBLF
D6	0	0	0	0	0	0	0	0	0	0
D7	0	0	0	0	0	0	0	0	0	0
Column	0	1	2	3	4	5	6	7	8	9

Where:

MAG	magazine	page number	MU	minutes units	page sub-code
PU	page units		MT	minutes tens	
PT	page tens		HU	hours units	
$\overline{\text{PBLF}}$	page being looked for		HT	hours tens	
$\overline{\text{FOUND}}$	LOW for page has been found		C4-C14	transmitted control bits	
HAM.ER	Hamming error in corresponding byte				

Row 0

Row 0 is for the page header. The first seven columns (0 to 6) are free for status messages. The eighth is an alphanumeric white or green control character, written automatically by EURO CCT to give a green rolling header when a page is being looked for. The last eight characters are for rolling time.

Row 25

The first 10 bytes of row 25 contain control data relating to the received page. Seven digits are used to identify a page as shown in Table 1. The remaining 14 bytes are free for use by the microcomputer.

Register maps

EURO CCT mode registers R1 to R11 are shown in Table 2. R1 to R10 are WRITE only; R11 is READ/WRITE.
Register map (R3), for page requests, is shown in detail in Table 3.

Table 2 EURO CCT register map

D7	D6	D5	D4	D3	D2	D1	D0		
TA	$\overline{7+P}$/ 8 BIT	ACQ. $\overline{ON}$/OFF	GHOST ROW ENABLE	$\overline{DEW}$/ FULL FIELD	TCS ON	T1	T0	R1	Mode
–	BANK SELECT A2	ACQ. CCT A1	ACQ. CCT A0	TB	START COLUMN SC2	START COLUMN SC1	START COLUMN SC0	R2	Page request address
–	–	–	PRD4	PRD3	PRD2	PRD1	PRD0	R3	Page request data
–	–	–	–	–	A2	A1	A0	R4	Display chapter
BKGND OUT	BKGND IN	COR OUT	COR IN	TEXT OUT	TEXT IN	PON OUT	PON IN	R5	Display control (normal)
BKGND OUT	BKGND IN	COR OUT	COR IN	TEXT OUT	TEXT IN	PON OUT	PON IN	R6	Display control (newsflash/subtitle)
STATUS ROW $\overline{BTM}$/TOP	CURSOR ON	$\overline{CONCEAL}$/ REVEAL	$\overline{TOP}$/ BOTTOM	$\overline{SINGLE}$/ DOUBLE HEIGHT	BOX ON 24	BOX ON 1-23	BOX ON 0	R7	Display mode
–	–	–	–	CLEAR MEM.	A2	A1	A0	R8	Active chapter
–	–	–	R4	R3	R2	R1	R0	R9	Active row
–	–	C5	C4	C3	C2	C1	C0	R10	Active column
D7 (R/W)	D6 (R/W)	D5 (R/W)	D4 (R/W)	D3 (R/W)	D2 (R/W)	D1 (R/W)	D0 (R/W)	R11	Active data

– bit does not exist

Notes to Table 2

The arrows shown on the right of the register map indicate that the register auto-increments to the next one on the following I^2C transmission byte. TA and TB must be logic 0 for normal operation.
All bits in registers R1 to R10 are cleared to logic 0 on power-up except bits D0 and D1 of registers R5 and R6 which are set to logic 1.
All memory is cleared to 'space' (00100000) on power-up, except row 0 column 7 chapter 0, which is 'alpha white' (00000111) as the acquisition circuit is enabled but all pages are on hold.

APPLICATION INFORMATION (continued)

Table 2 (continued)

Where:

R1 Mode	
T0, T1	interlace/non interlace 312/313 line control
TCS ON	text composite sync or direct sync select
$\overline{\text{DEW}}$/FULL FIELD	field-flyback or full channel mode
$\overline{7+P}$/8 BIT	7 bits with parity checking or 8-bit mode
TA, TB	test bits; 0 for normal operation
R2 Page request address	
START COLUMN	start column for page request data
ACQ CCT	selects one of four acquisition circuits
BANK SELECT	selects bank of four pages being addressed for acquisition
R3 Page request data	see Table 3
R4 Display chapter	determines which of the 8 pages is displayed
R5, R6 Display control	for normal and newsflash/subtitle
PON	picture on
TEXT	text on
COR	contrast reduction on
BKGND	background colour on

These functions have IN and OUT referring to inside and outside the boxing function respectively.

R7 Display mode	
BOX ON 0 (1-23, 24)	boxing function allowed on row 0 (row 1-23, 24)
STATUS ROW $\overline{\text{BTM}}$/TOP	row 25 displayed above or below the main text
R8 to R11	active chapter, row, column and data information written to or read from page memory via the I^2C bus.

Table 3 Register map for page requests (R3)

Start Column	PRD4	PRD3	PRD2	PRD1	PRD0
0	Do care Magazine	$\overline{\text{HOLD}}$	MAG2	MAG1	MAG0
1	Do care Page tens	PT3	PT2	PT1	PT0
2	Do care Page units	PU3	PU2	PU1	PU0
3	Do care Hours tens	X	X	HT1	HT0
4	Do care Hours units	HU3	HU2	HU1	HU0
5	Do care Minutes tens	X	MT2	MT1	MT0
6	Do care Minutes units	MU3	MU2	MU1	MU0

Notes to Table 3

Abbreviations are as for Table 1 except for D0 CARE bits.
When the D0 CARE bit is set to logic 1 this means the corresponding digit is to be taken into account for page requests. If the D0 CARE bit is set to logic 0 the digit is ignored. This allows, for example, 'normal' or 'timed page' selection.
If $\overline{\text{HOLD}}$ is set LOW, the page is held and not updated.
There are four groups of data shown in Table 3, one for each acquisition circuit (four simultaneous page requests).
Columns auto-increment on successive I^2C transmission bytes.

APPLICATION INFORMATION (continued)

CHARACTER SETS

The UK teletext specification allows the selection of national character sets via the page header transmission bits, C12 to C14 as shown in Table 4. The basic 96 character sets differ only in the 13 national option characters as indicated in Tables 8 and 9 with reference to their table position in the basic character matrix shown in Table 7. EURO CCT automatically decodes control bits C12 to C14. Other combinations of C12 to C14 are defaulted to SAA5240A (English); SAA5240B (German). With 8-bit decoding the character matrices are shown in Tables 5 and 6.

Table 4 Selection of national character sets

PHCB	ENGLISH	GERMAN	SWEDISH	ITALIAN	FRENCH
C12	0	0	0	0	1
C13	0	0	1	1	0
C14	0	1	0	1	0

Where:

PHCB page header control bits.

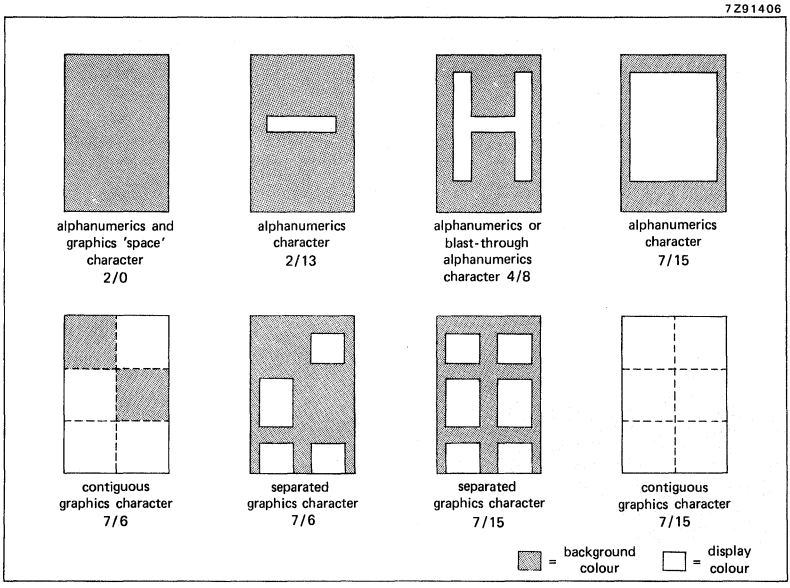
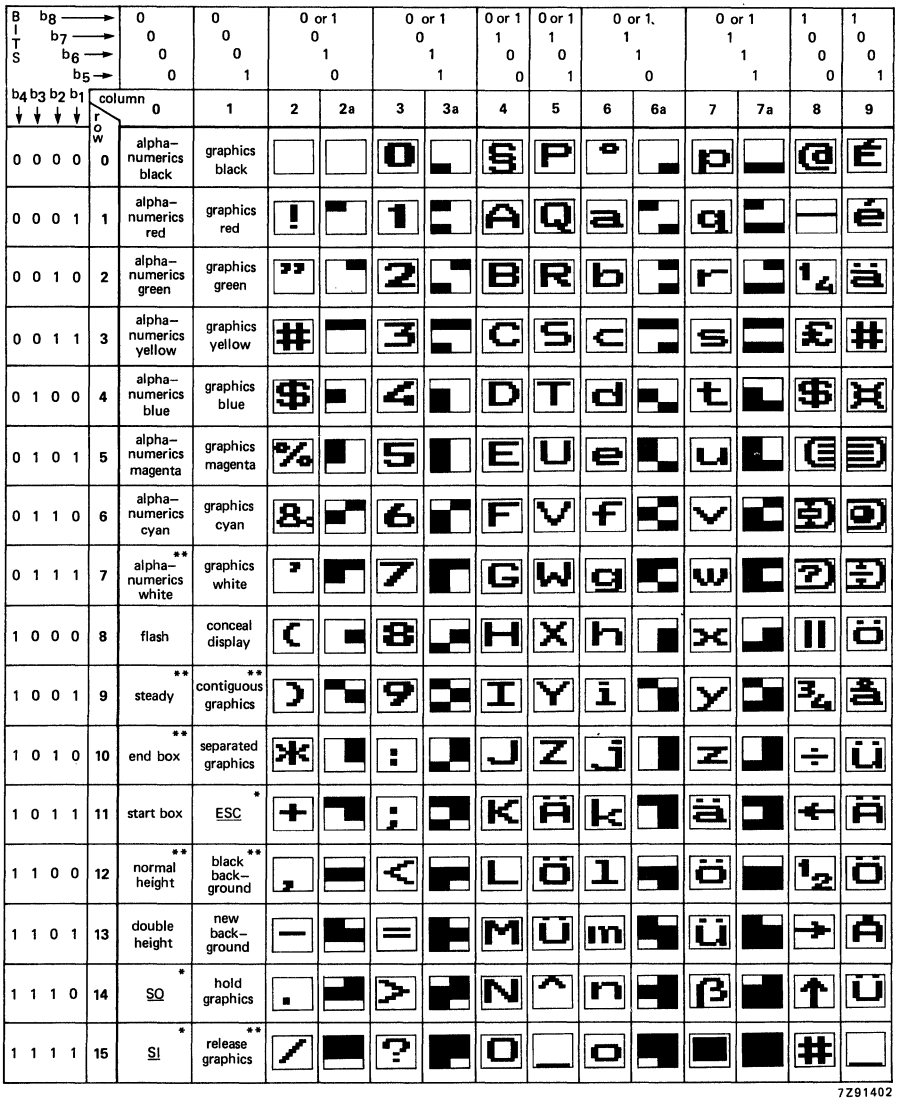


Fig. 12 Character format.

Table 5 Character data input decoding (SAA5240A)



7Z91402

* These control characters are reserved for compatibility with other data codes.

** These control characters are presumed before each row begins.

APPLICATION INFORMATION (continued)

Table 6 Character data input decoding (SAA5240B)

BITS b_8	0	0	0 or 1		0 or 1		0 or 1	0 or 1	0 or 1		0 or 1		1	1
b_7	0	0	0		0		1	1	1		1		0	0
b_6	0	0	1		1		0	0	1		1		0	0
b_5	0	1	0		1		0	1	0		1		0	1
b_4 b_3 b_2 b_1 ↓ ↓ ↓ ↓	column 0	1	2	2a	3	3a	4	5	6	6a	7	7a	8	9
0 0 0 0	0	alpha–numerics black	graphics black											
0 0 0 1	1	alpha–numerics red	graphics red											
0 0 1 0	2	alpha–numerics green	graphics green											
0 0 1 1	3	alpha–numerics yellow	graphics yellow											
0 1 0 0	4	alpha–numerics blue	graphics blue											
0 1 0 1	5	alpha–numerics magenta	graphics magenta											
0 1 1 0	6	alpha–numerics cyan	graphics cyan											
0 1 1 1	7	alpha–numerics white **	graphics white											
1 0 0 0	8	flash	conceal display											
1 0 0 1	9	steady **	contiguous graphics **											
1 0 1 0	10	end box **	separated graphics											
1 0 1 1	11	start box	ESC *											
1 1 0 0	12	normal height **	black back–ground **											
1 1 0 1	13	double height	new back–ground											
1 1 1 0	14	SO *	hold graphics											
1 1 1 1	15	SI *	release graphics **											

7Z91484

* These control characters are reserved for compatibity with other data codes.

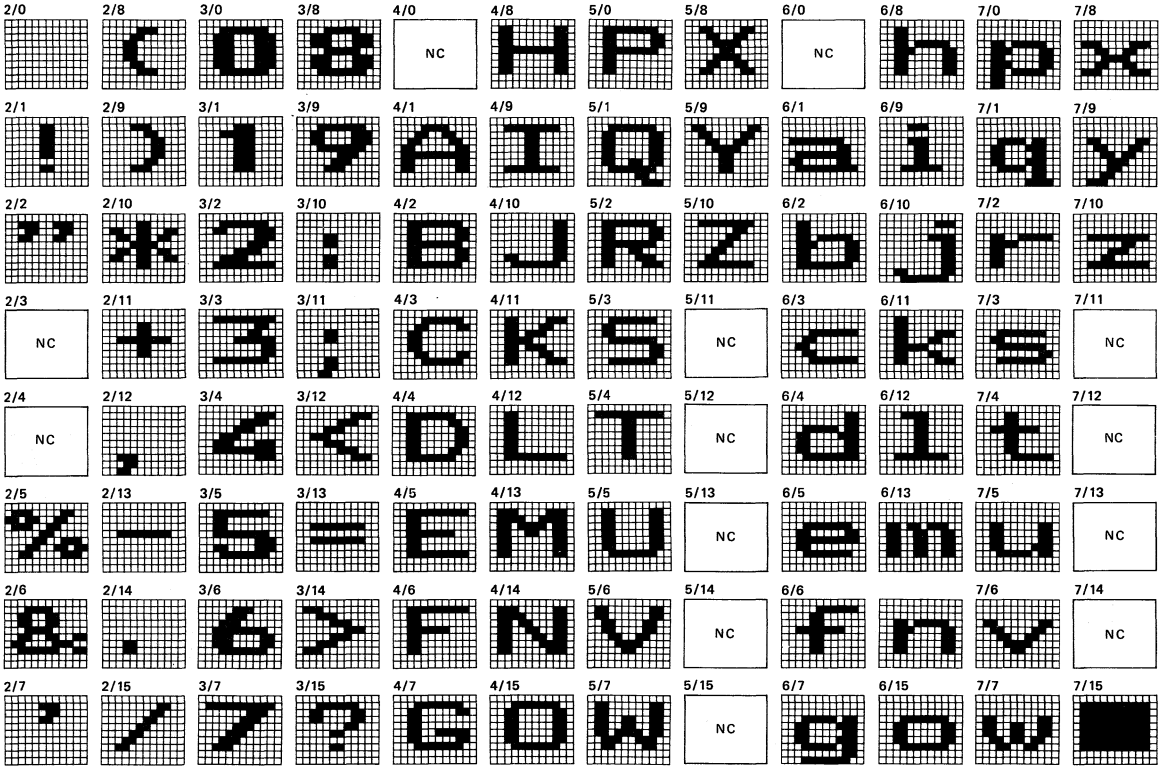
** These control characters are presumed before each row begins.

Notes to Tables 5 and 6

1. Control characters shown in columns 0 and 1 are normally displayed as spaces.
2. Codes may be referred to by column and row. For example 2/5 refers to %.
3. Black represents displayed colour. White represents background.
4. Character rectangle shown as follows: □
5. The SAA5240A national option characters are shown in Table 8.
6. The SAA5240B national option characters are shown in Table 9.
7. Characters 8/6, 8/7, 9/5, 9/6 and 9/7 are special characters to combine with character 8/5.
8. With bit 8 = 0 national option characters will be decoded according to the setting of control bits C12 to C14 (see Table 4).

APPLICATION INFORMATION (continued)

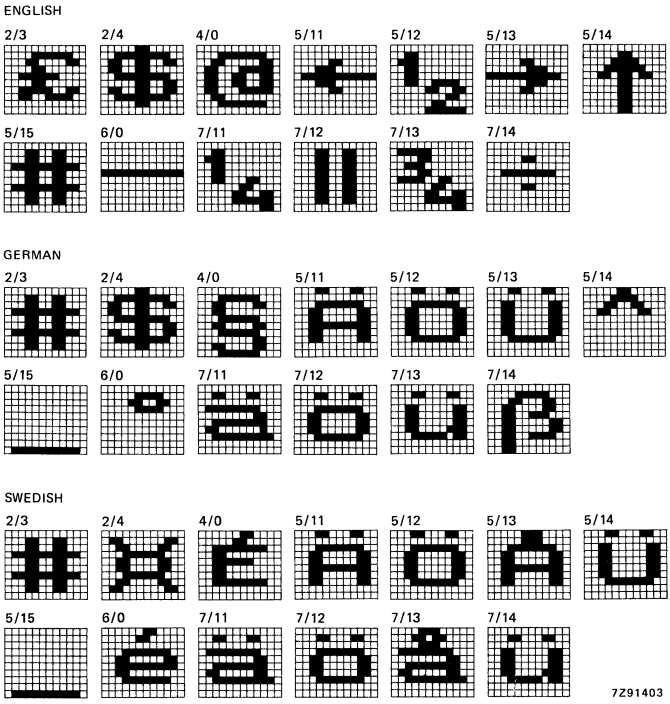
Table 7 SAA5240 basic character matrix



7Z91405

Where: NC national option character position.

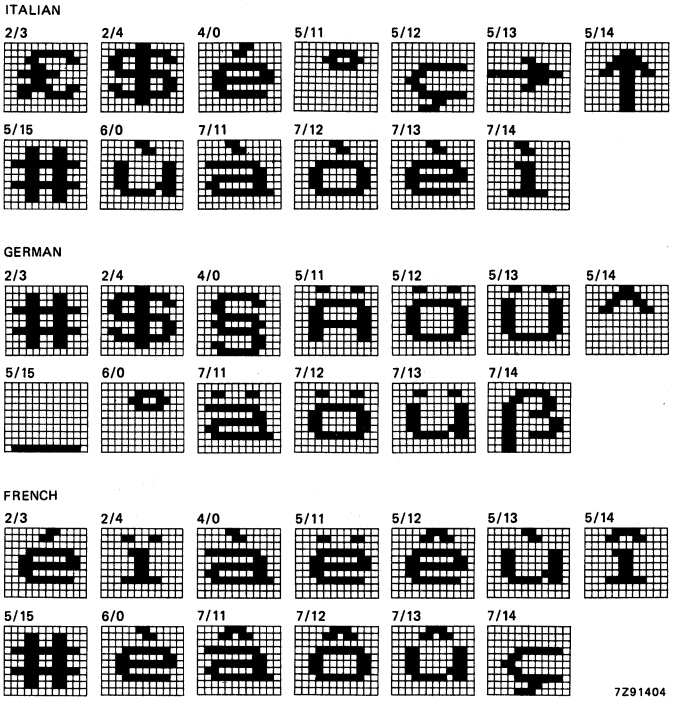
Table 8 SAA5240A character set (national option characters)



DEVELOPMENT DATA

APPLICATION INFORMATION (continued)

Table 9 SAA5240B character set (national option characters)



SINGLE-CHIP COLOUR CRT CONTROLLER (EUROM)

GENERAL DESCRIPTION

The SAA5350 EUROM is a single-chip VLSI NMOS crt controller capable of handling all display functions required by the CEPT videotex terminal, model A4. Only minimal hardware is required to produce a videotex terminal using EUROM – the simplest configuration needs just a microcontroller and 4 Kbytes of display memory.

Features

- Minimal additional hardware required
- Screen formats of 40/80 character by 1-to-25 row display
- 512 alphanumeric or graphical characters on-chip or extendable off-chip
- Serial attribute storage (STACK) and parallel attribute storage
- Dynamically redefinable character (DRCS) capability over full field
- Interfaces with 8/16-bit microprocessors with optional direct memory access
- On-chip scroll map minimizes data to be transferred when scrolling
- On-chip colour map RAM (4096 locations) and three on-chip digital-to-analogue converters allow 32 colours on-screen
- On-chip digital-to-analogue converters are non-linear to compensate for crt non-linearity
- Memory interface capable of supporting multi-page terminals. EUROM can access up to 128 Kbytes of display memory
- Programmable cursor
- Programmable local status row
- Three synchronization modes:

stand-alone	built-in oscillator operating with an external 6 MHz crystal
simple slave	directly synchronized from the source of text composite sync
phase-locked slave	indirect synchronization allows picture-in-text displays (e.g. VCR/VLP video with text overlay)

- On-chip timing composite sync output
- Zoom feature which allows the height of any group of rows to be increased to enhance legibility

PACKAGE OUTLINE

40-lead DIL; plastic (SOT-129).

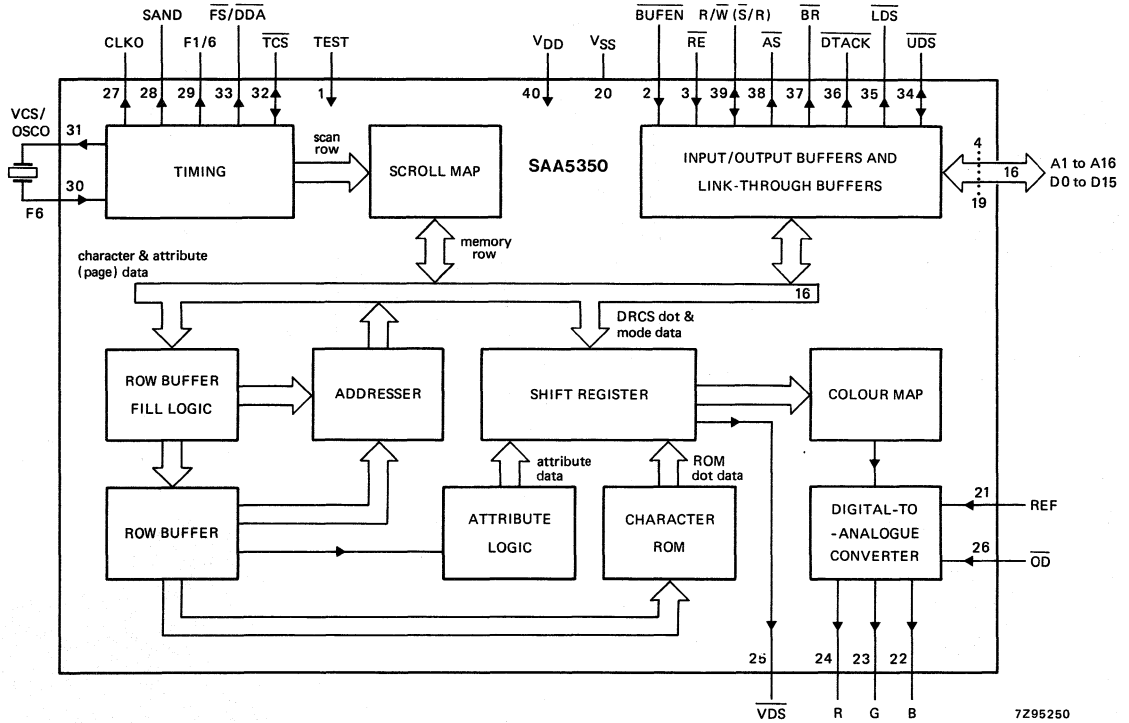


Fig. 1 Block diagram.

PINNING

1	TEST	Input to be connected to V_{SS}.
2	$\overline{\text{BUFEN}}$	Buffer enable input to the 8-bit link-through buffer.
3	$\overline{\text{RE}}$	Register enable input. This enables A1 to A6 and $\overline{\text{UDS}}$ as inputs, and D8 to D15 as input/outputs.
4 to 19	A16 to A1/ D15 to D0	Multiplexed address and data bus input/outputs. These pins also function as the 8-bit link-through buffer.
20	V_{SS}	Ground (0 V).
21	REF	Analogue reference input.
22	B	Analogue outputs (signals are gamma-corrected).
23	G	
24	R	
25	$\overline{\text{VDS}}$	Switching output for dot, screen (row), box and window video data; for use when video signal is present (e.g. from tv, VLP, alpha + photographic layer). This output is LOW for tv display and HIGH for text and will interface directly with a number of colour decoder ICs (e.g. TDA3560, TDA3505).
26	$\overline{\text{OD}}$	Output disable causing R, G, B and $\overline{\text{VDS}}$ outputs to go to high-impedance state. Can be used at dot-rate.
27	CLKO	12 MHz clock output for hard-copy dot synchronization (referenced to output dots).
28	SAND	Sandcastle feedback output for SAA5230 teletext video processor or other circuit. Used when the display must be locked to the video source (e.g. VLP). The phase-lock part of the sandcastle waveform can be disabled to allow free-running of the SAA5230 phase-locked loop.
29	F1/6	1 MHz or 6 MHz output.
30	F6	6 MHz clock input (e.g. from SAA5230). Internal a.c. coupling is provided.
31	VCS/OSCO	Video composite sync input (e.g. from SAA5230) for phase reference of vertical display timing when locking to a video source (e.g. VLP) or, in stand-alone sync mode, output from internal oscillator circuit (fixed frequency).
32	$\overline{\text{TCS}}$	Text composite sync input/output depending on master/slave status.
33	$\overline{\text{FS}}/\overline{\text{DDA}}$	Field sync pulse output or defined-display-area flag output (both referenced to output dots).
34	$\overline{\text{UDS}}$	Upper data strobe input/output.
35	$\overline{\text{LDS}}$	Lower data strobe output.
36	$\overline{\text{DTACK}}$	Data transfer acknowledge (open drain output).
37	$\overline{\text{BR}}$	Bus request to microprocessor (open drain output).
38	$\overline{\text{AS}}$	Address strobe output to external address latches.
39	R/$\overline{\text{W}}$ ($\overline{\text{S}}$/R)	Read/write input/output. Also serves as send/receive for the link-through buffer.
40	V_{DD}	Positive supply voltage (+ 5 V).

DEVELOPMENT DATA

PINNING (continued)

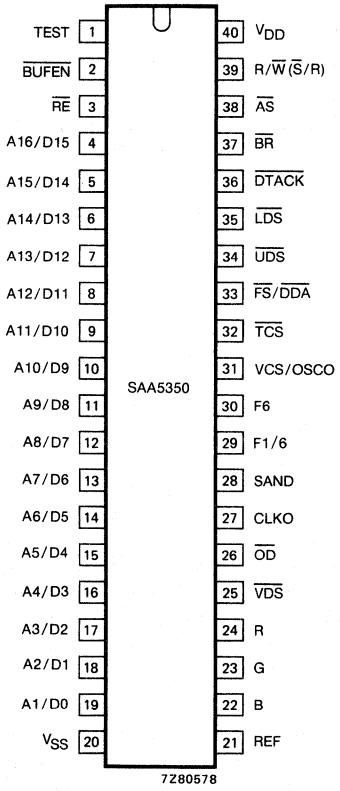


Fig. 2 Pinning diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range (pin 40)	V_{DD}	−0,3 to + 7,5 V
Maximum input voltage (except F6, $\overline{TCS}$, REF)	V_{Imax}	−0,3 to + 7,5 V
Maximum input voltage (F6, $\overline{TCS}$)	V_{Imax}	−0,3 to + 10,0 V
Maximum input voltage (REF)	V_{REF}	−0,3 to + 3,0 V
Maximum output voltage	V_{Omax}	−0,3 to + 7,5 V
Maximum output current	I_{Omax}	10 mA
Operating ambient temperature range	T_{amb}	−20 to + 70 °C
Storage temperature range	T_{stg}	−55 to + 125 °C

Outputs other than CLKO, OSCO, R, G, B, and $\overline{VDS}$ are short-circuit protected.

DEVELOPMENT DATA

CHARACTERISTICS

V_{DD} = 5 V ± 10%; V_{SS} = 0 V; T_{amb} = −20 to + 70 °C; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
SUPPLY					
Supply voltage (pin 40)	V_{DD}	4,5	5,0	5,5	V
Supply current (pin 40)	I_{DD}	–	–	350	mA
INPUTS					
F6 (note 1)					
Slave modes (Fig. 3)					
Input voltage (peak-to-peak value)	$V_{I(p-p)}$	1,0	–	7,0	V
Input peaks relative to 50% duty factor	$\pm V_P$	0,2	–	3,5	V
Input leakage current at V_I = 0 to 10 V; T_{amb} = 25 °C	I_{LI}	–	–	20	μA
Input capacitance	C_I	–	–	12	pF
Stand-alone mode (Fig. 4)					
Series capacitance of crystal	C_1	–	28	–	fF
Parallel capacitance of crystal	C_0	–	7,1	–	pF
Resonance resistance of crystal	R_r	–	–	60	Ω
Gain of circuit	G	–	–	tbf	V/V
$\overline{\text{BUFEN}}$, $\overline{\text{RE}}$, $\overline{\text{OD}}$					
Input voltage LOW	V_{IL}	0	–	0,8	V
Input voltage HIGH	V_{IH}	2,0	–	6,5	V
Input current at V_I = 0 to V_{DD}+ 0,3 V; T_{amb} = 25 °C	I_I	−10	–	+ 10	μA
Input capacitance	C_I	–	–	7	pF
REF (Fig. 5)					
Input voltage	V_{REF}	0	1 to 2	2,7	V
Resistance (pin 21 to pin 20) with REF supply and R, G, B outputs OFF	R_{REF}	–	125	–	Ω

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
OUTPUTS					
SAND					
Output voltage high level at I_O = 0 to −30 μA	V_{OH}	4,2	–	V_{DD}	V
Output voltage intermediate level at I_O = −30 to + 30 μA	V_{OI}	1,3	2,0	2,7	V
Output voltage low level at I_O = 0,2 mA	V_{OL}	0	–	0,2	V
Load capacitance	C_L	–	–	30	pF
F1/6, CLKO, $\overline{\text{DDA}}$/$\overline{\text{FS}}$					
Output voltage HIGH at I_{OH} = −200 μA	V_{OH}	2,4	–	V_{DD}	V
Output voltage LOW at I_{OL} = 3,2 mA	V_{OL}	0	–	0,4	V
Load capacitance	C_L	–	–	50	pF
$\overline{\text{LDS}}$, $\overline{\text{AS}}$					
Output voltage HIGH at I_{OH} = −200 μA	V_{OH}	2,4	–	V_{DD}	V
Output voltage LOW at I_{OL} = 3,2 mA	V_{OL}	0	–	0,4	V
Load capacitance	C_L	–	–	200	pF
$\overline{\text{DTACK}}$, $\overline{\text{BR}}$ (open drain outputs)					
Output voltage LOW at I_{OL} = 3,2 mA	V_{OL}	0	–	0,4	V
Load capacitance	C_L	–	–	150	pF
Capacitance (OFF state)	C_{OFF}	–	–	7	pF
R, G, B (note 2)					
Output voltage HIGH (note 3) at I_{OH} = −100 μA; V_{REF} = 2,7 V	V_{OH}	2,4	–	–	V
Output voltage LOW at I_{OL} = 2 mA	V_{OL}	–	–	0,4	V
Output resistance during line blanking	R_{OBL}	–	–	150	Ω
Output capacitance (OFF state)	C_{OFF}	–	–	12	pF
Output leakage current (OFF state) at V_I = 0 to V_{DD}+0,3 V; T_{amb} = 25 °C	I_{OFF}	−10	–	+ 10	μA

parameter	symbol	min.	typ.	max.	unit
$\overline{VDS}$					
Output voltage HIGH at $I_{OH} = -250\ \mu A$	V_{OH}	2,4	–	V_{DD}	V
Output voltage LOW at $I_{OL} = 2$ mA	V_{OL}	0	–	0,4	V
Output voltage LOW at $I_{OL} = 1$ mA	V_{OL}	0	–	0,2	V
Output leakage current (OFF state) at $V_I = 0$ to $V_{DD}+0,3$ V; $T_{amb} = 25\ ^oC$	I_{OFF}	−10	–	+ 10	μA
INPUT/OUTPUTS					
VCS/OSCO					
Input voltage HIGH	V_{IH}	2,0	–	6,0	V
Input voltage LOW	V_{IL}	0	–	0,8	V
Input current (output OFF) at $V_I = 0$ to $V_{DD}+0,3$ V; $T_{amb} = 25\ ^oC$	I_I	−10	–	+ 10	μA
Input capacitance	C_I	–	–	10	pF
$\overline{TCS}$					
Input voltage HIGH	V_{IH}	3,5	–	10,0	V
Input voltage LOW	V_{IL}	0	–	1,5	V
Input current at $V_I = 0$ to $V_{DD}+0,3$ V; $T_{amb} = 25\ ^oC$	I_I	−10	–	+ 10	μA
Input capacitance	C_I	–	–	10	pF
Output voltage HIGH at $I_{OH} = -200$ to $100\ \mu A$	V_{OH}	2,4	–	6,0	V
Output voltage LOW at $V_{OL} = 3,2$ mA	V_{OL}	0	–	0,4	V
Load capacitance	C_L	–	–	50	pF
A1/D0 to A16/D15, $\overline{UDS}$, R/$\overline{W}$					
Input voltage LOW	V_{IL}	0	–	0,8	V
Input voltage HIGH	V_{IH}	2,0	–	6,0	V
Input current at $V_I = 0$ to $V_{DD}+0,3$ V; $T_{amb} = 25\ ^oC$	I_I	−10	–	+ 10	μA
Input capacitance	C_I	–	–	10	pF
Output voltage HIGH at $I_{OH} = -200\ \mu A$	V_{OH}	2,4	–	V_{DD}	V
Output voltage LOW at $I_{OL} = 3,2$ mA	V_{OL}	0	–	0,4	V
Load capacitance	C_L	–	–	200	pF

DEVELOPMENT DATA

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
TIMING					
F6 (Fig. 3)					
Rise and fall times	t_r, t_f	10	–	80	ns
Frequency	f_{F6}	5,9	–	6,1	MHz
CLKO, F1/6, R, G, B, $\overline{VDS}$, $\overline{FS}$/$\overline{DDA}$, $\overline{OD}$ (notes 4, 5 and Fig. 6)					
CLKO HIGH time	t_{CLKH}	30	–	–	ns
CLKO LOW time	t_{CLKL}	20	–	–	ns
CLKO rise and fall times	t_{CLKr} t_{CLKf}	–	–	10	ns
CLKO HIGH to R, G, B, $\overline{VDS}$ change	t_{VCH}	10	–	–	ns
R, G, B, $\overline{VDS}$ valid to CLKO rise	t_{VOC}	10	–	–	ns
CLKO HIGH to R, G, B, $\overline{VDS}$ valid	t_{COV}	–	–	60	ns
CLKO HIGH to R, G, B, $\overline{VDS}$ floating after $\overline{OD}$ fall	t_{FOD}	–	–	30	ns
Skew between outputs R, G, B, $\overline{VDS}$	t_{VS}	–	–	20	ns
R, G, B, $\overline{VDS}$ rise and fall times	t_{Vr}, t_{Vf}	–	–	30	ns
CLKO HIGH to R, G, B, $\overline{VDS}$ active after $\overline{OD}$ rise	t_{AOD}	0	–	–	ns
CLKO HIGH to $\overline{FS}$/$\overline{DDA}$ change	t_{COD}	–	–	55	ns
$\overline{FS}$/$\overline{DDA}$ valid to CLKO rise	t_{DOC}	5	–	–	ns
F1 HIGH time (note 6)	t_{F1H}	–	500	–	ns
F1 LOW time (note 6)	t_{F1L}	–	500	–	ns
F6 HIGH time	t_{F6H}	–	83	–	ns
F6 LOW time	t_{F6L}	–	83	–	ns
$\overline{OD}$ to CLKO rise set-up	t_{ODS}	–	–	45	ns
$\overline{OD}$ to CLKO HIGH hold	t_{ODH}	–	–	0	ns
MEMORY ACCESS TIMING (notes 7, 8, 9 and Fig. 7)					
$\overline{UDS}$, $\overline{LDS}$, $\overline{AS}$					
Cycle time	t_{cyc}	–	500	–	ns
$\overline{UDS}$ HIGH to bus-active for address output	t_{SAA}	75	–	–	ns
Address valid set-up to $\overline{AS}$ fall	t_{ASU}	20	–	–	ns
Address valid hold from $\overline{AS}$ LOW	t_{ASH}	20	–	–	ns
Address float to $\overline{UDS}$ fall	t_{AFS}	0	–	–	ns

parameter	symbol	min.	typ.	max.	unit
$\overline{AS}$ LOW to $\overline{UDS}$ fall delay	t_{ATD}	50	–	–	ns
$\overline{UDS}$, $\overline{LDS}$ HIGH time	t_{HDS}	220	–	–	ns
$\overline{UDS}$, $\overline{LDS}$ LOW time	t_{LDS}	200	–	–	ns
$\overline{AS}$ HIGH time	t_{HAS}	125	–	–	ns
$\overline{AS}$ LOW time	t_{LAS}	320	–	–	ns
$\overline{AS}$ LOW to $\overline{UDS}$ HIGH	t_{AUH}	305	–	–	ns
Data valid set-up to $\overline{UDS}$ rise	t_{DSU}	30	–	–	ns
Data valid hold from $\overline{UDS}$ HIGH	t_{DSH}	0	–	–	ns
$\overline{UDS}$ HIGH to $\overline{AS}$ rise delay	t_{UAS}	0	–	–	ns
$\overline{AS}$ LOW to data valid	t_{AFA}	–	–	270	ns
Link-through buffers					
(notes 7, 8 and Fig. 8)					
$\overline{BUFEN}$ LOW to output valid	t_{BEA}	–	–	100	ns
Link-through delay time	t_{LTD}	–	–	85	ns
Input data float prior to direction change	t_{IFR}	0	–	–	ns
Output float after direction change	t_{OFR}	–	–	60	ns
Output float after $\overline{BUFEN}$ HIGH	t_{BED}	–	–	60	ns
Microprocessor READ from EUROM					
(Fig. 9)					
R/$\overline{W}$ HIGH set-up to $\overline{UDS}$ fall	t_{RUD}	0	–	–	ns
$\overline{UDS}$ LOW to returned-data access time	t_{UDA}	–	–	210	ns
$\overline{RE}$ LOW to returned data access time	t_{REA}	–	–	210	ns
Data valid to $\overline{DTACK}$ LOW delay	t_{DTL}	−20	–	–	ns
$\overline{DTACK}$ LOW to $\overline{UDS}$ rise	t_{DLU}	0	–	–	ns
$\overline{UDS}$ HIGH to $\overline{DTACK}$ rise	t_{DTR}	0	–	50	ns
$\overline{UDS}$ HIGH to address hold	t_{DSA}	0	–	–	ns
$\overline{UDS}$ HIGH to data hold	t_{DSH}	10	–	–	ns
$\overline{UDS}$ HIGH to $\overline{RE}$ rise	t_{SRE}	10	–	–	ns
$\overline{UDS}$ HIGH to R/$\overline{W}$ fall	t_{UDR}	0	–	–	ns
$\overline{UDS}$ LOW to $\overline{DTACK}$ LOW	t_{DSD}	190	–	260	ns
Address valid to $\overline{UDS}$ fall	t_{AUL}	0	–	–	ns

DEVELOPMENT DATA

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
MEMORY ACCESS TIMING (continued)					
Microprocessor WRITE to EUROM (Fig. 10)					
Write cycle time (note 10)	t_{WCY}	500	–	–	ns
R/$\overline{W}$ LOW set-up to $\overline{UDS}$ fall	t_{WUD}	0	–	–	ns
$\overline{RE}$ LOW to $\overline{UDS}$ fall	t_{RES}	30	–	–	ns
Address valid to $\overline{UDS}$ fall	t_{ASS}	30	–	–	ns
$\overline{UDS}$ LOW time	t_{LUS}	100	–	–	ns
Data valid to $\overline{UDS}$ rise	t_{DSS}	80	–	–	ns
$\overline{UDS}$ LOW to $\overline{DTACK}$ LOW	t_{DTA}	0	–	60	ns
$\overline{DTACK}$ LOW to $\overline{UDS}$ rise	t_{DLU}	0	–	–	ns
$\overline{UDS}$ HIGH to $\overline{DTACK}$ rise	t_{DTR}	0	–	50	ns
$\overline{UDS}$ HIGH to data hold	t_{DSH}	0	–	–	ns
$\overline{UDS}$ HIGH to address hold	t_{DSA}	0	–	–	ns
$\overline{UDS}$ HIGH to $\overline{RE}$ rise	t_{SRE}	10	–	–	ns
$\overline{UDS}$ HIGH to R/$\overline{W}$ rise	t_{UDW}	0	–	–	ns
F1/6 to memory access cycle (Fig. 11)					
$\overline{UDS}$ HIGH to F6 (component of F1/6) rise	t_{UF6}	20	–	–	ns
F6 (component of F1/6) HIGH to $\overline{UDS}$ rise	t_{F6U}	40	–	–	ns
SYNCHRONIZATION and BLANKING					
$\overline{TCS}$, SAND, $\overline{FS}$/$\overline{DDA}$					
See Fig. 12 for timing relationships and Fig. 13 for vertical sync and blanking waveforms.					

Notes to the characteristics

1. Pin 30 must be biased externally as it is internally a.c. coupled.
2. 16-level analogue voltage outputs.
3. Output voltage guaranteed when programmed for top level.
4. CLKO, R, G, B, F1/6, $\overline{VDS}$: C_L = 25 pF
   $\overline{FS}$/$\overline{DDA}$: C_L = 50 pF
5. CLKO, F1/6, $\overline{VDS}$, $\overline{FS}$/$\overline{DDA}$: reference levels = 0,8 to 2,0 V
   R, G, B: reference levels = 0,8 to 2,0 V with V_{REF} = 2,7 V
6. These times may momentarily be reduced to a nominal 83 ns in slave-sync mode at the moment of re-synchronization.
7. C_L = 150 pF.
8. Reference levels = 0,8 to 2,0 V.
9. F6 input at 6 MHz.
10. Microprocessor write cycle times of less than 500 ns are permitted but often result in Wait States being generated, the precise timing of $\overline{DTACK}$ will then depend on the internal synchronization time.

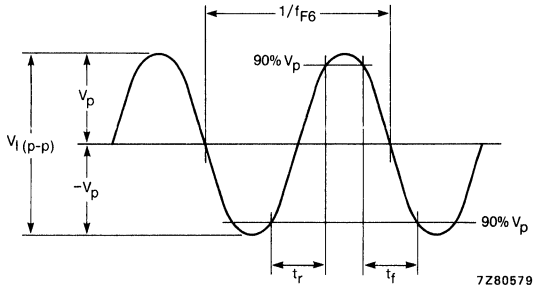
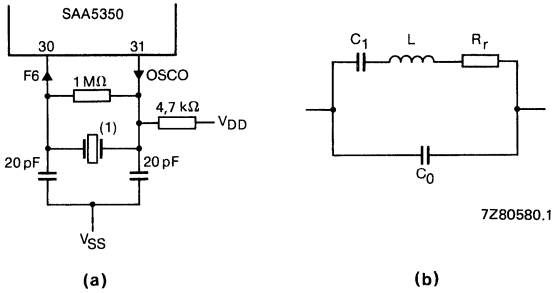


Fig. 3 F6 input waveform.



(1) Catalogue number of crystal: 4322 143 04101

Fig. 4(a) Oscillator circuit for SAA5350 stand-alone sync mode and (b) equivalent circuit of crystal at resonance (see **characteristics** for values).

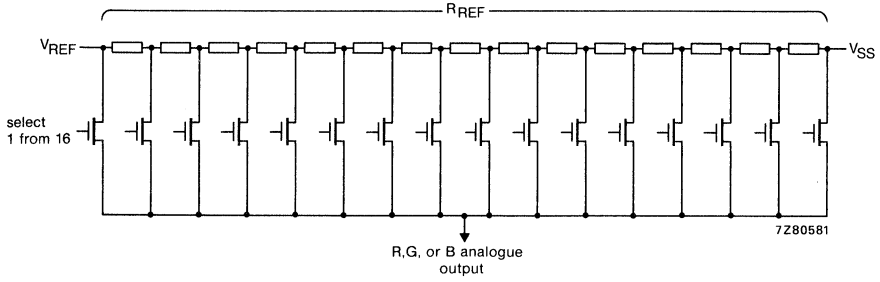


Fig. 5 Circuit arrangement giving one-of-sixteen reference voltage levels for the R, G or B analogue outputs.

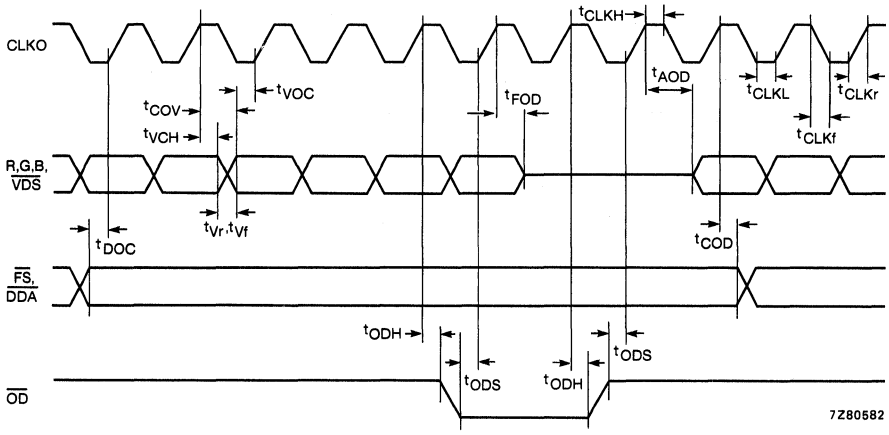


Fig. 6 Video timing.

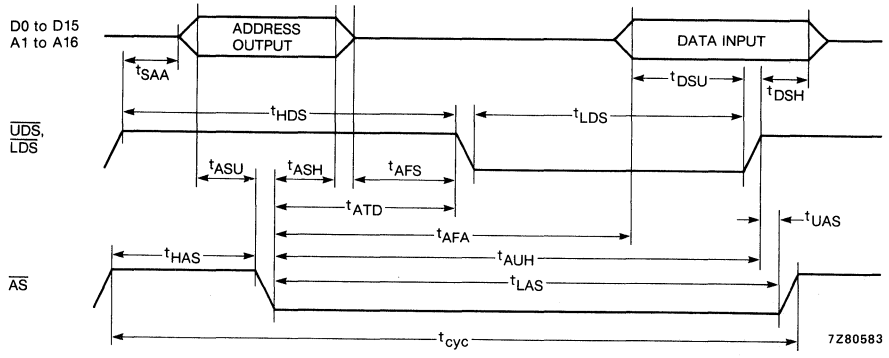


Fig. 7 Memory access timing.

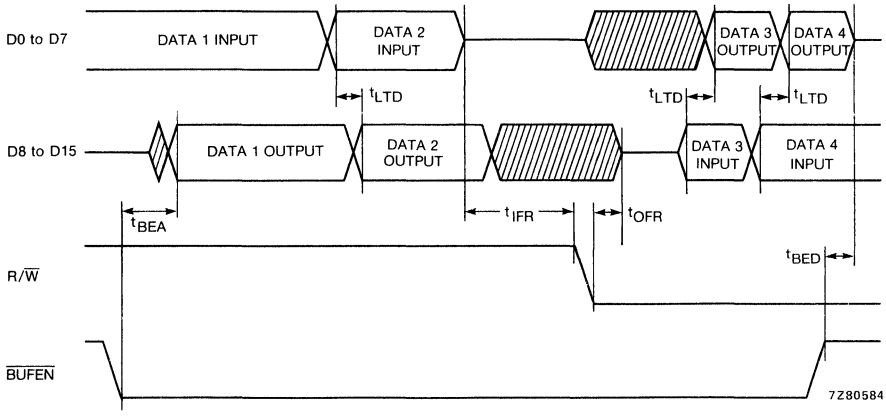


Fig. 8 Timing of link-through buffers.

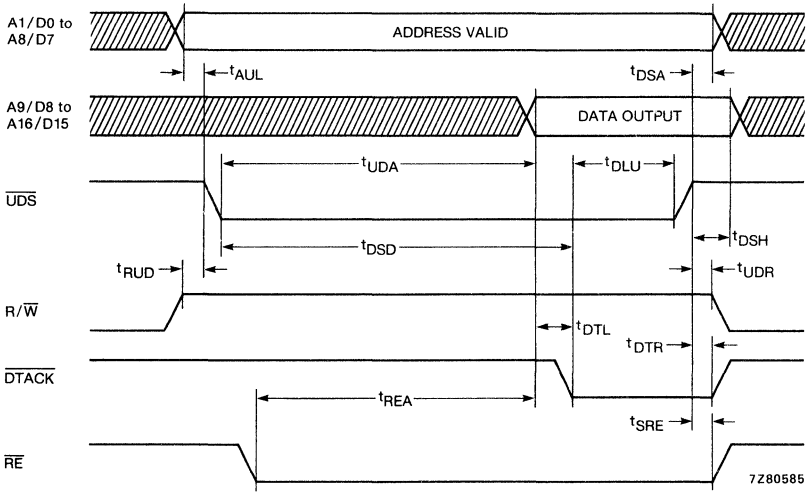


Fig. 9 Timing of microprocessor read from EUROM.

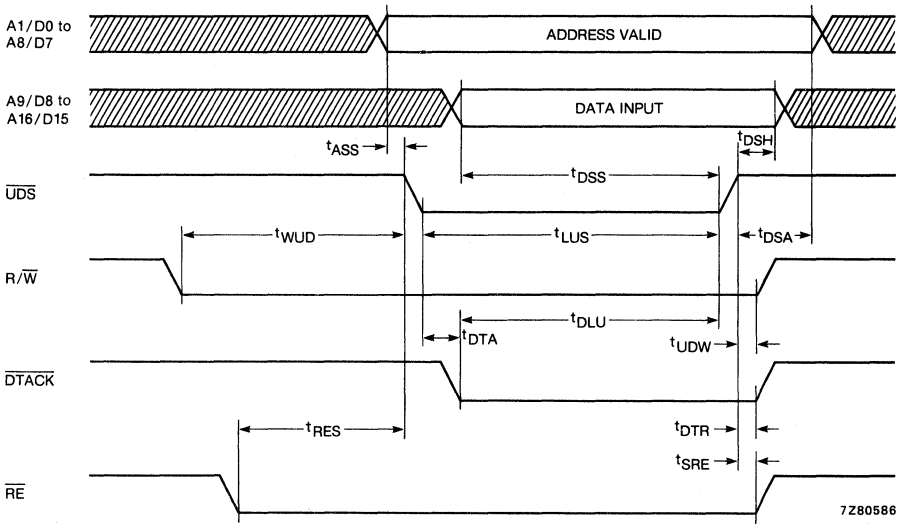


Fig. 10 Timing of microprocessor write to EUROM.

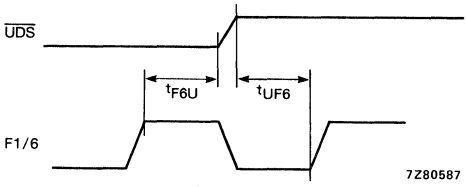


Fig. 11 Timing of F1/6 to memory access cycle.

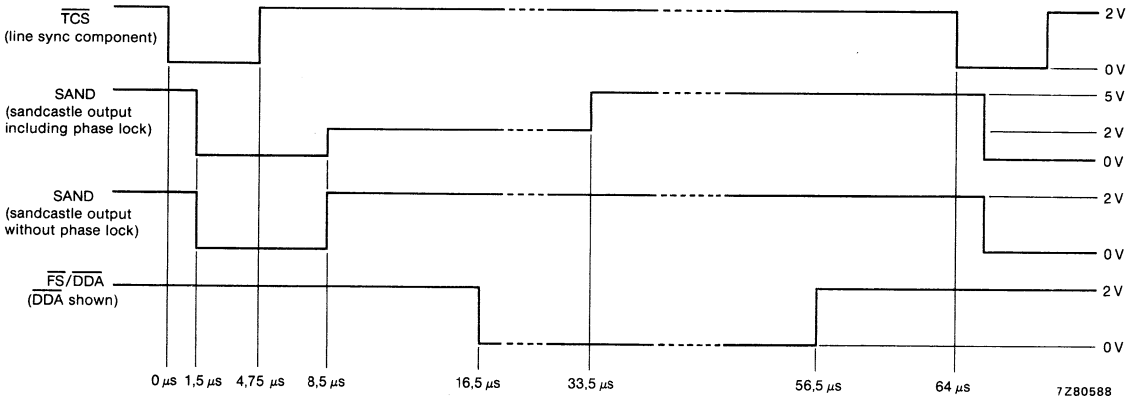


Fig. 12 Timing of synchronization and blanking outputs; all timings are nominal and assume f_{F6} = 6 MHz.

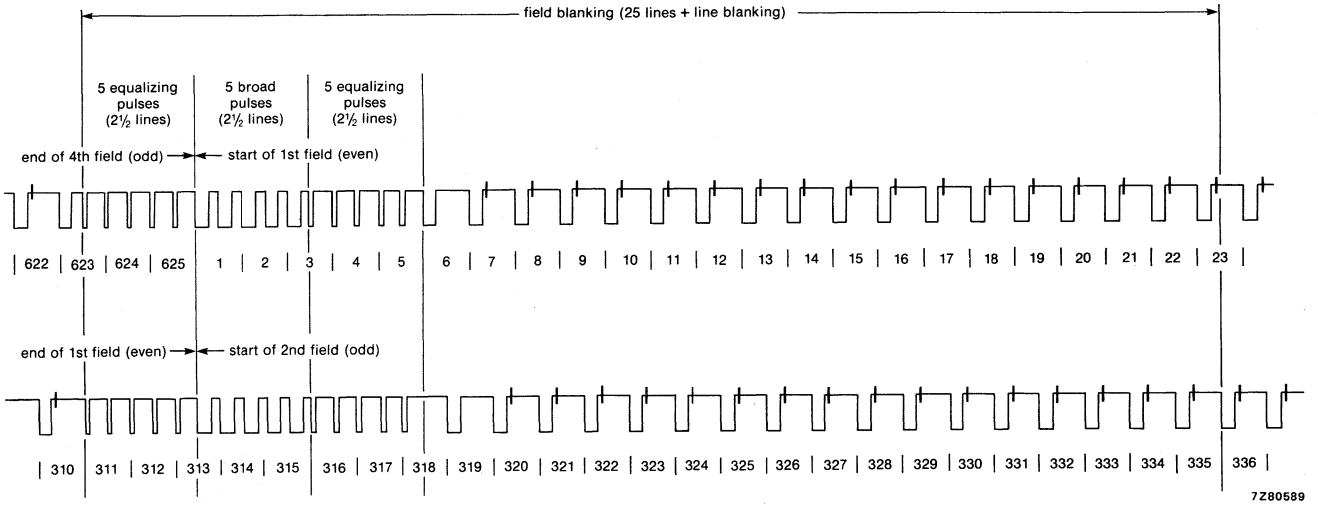


Fig. 13 Vertical synchronization and blanking waveforms; separation of broad pulses = 4,75 μs; equalizing pulse widths = 2,25 μs.

APPLICATION INFORMATION

More detailed application information is available on request

BASIC VIDEOTEX DECODER CONFIGURATION

A basic, practical decoder configuration is shown in Fig. 14, reference should also be made to the block diagram Fig. 1.

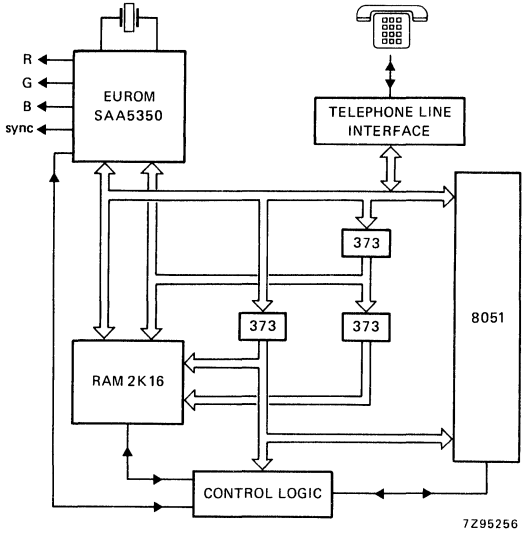


Fig. 14 Basic videotex decoder configuration.

Character and attribute data is fetched from the external memory, processed by the row buffer fill logic according to the stack coding scheme (in stack mode) and then fed into one half of the dual display row buffer. The data fetch process takes place during one line-flyback period (per row) and, since time is required to complete the fill, the other half of the dual row buffer is used for display. The row buffers exchange functions on alternate rows — each holds the 40 columns of 32 bits required to define explicitly every character in a row.

The addresser is used for row buffer filling and for fetching screen colours, and during the display time it is also used for addressing DRCS characters.

Timing

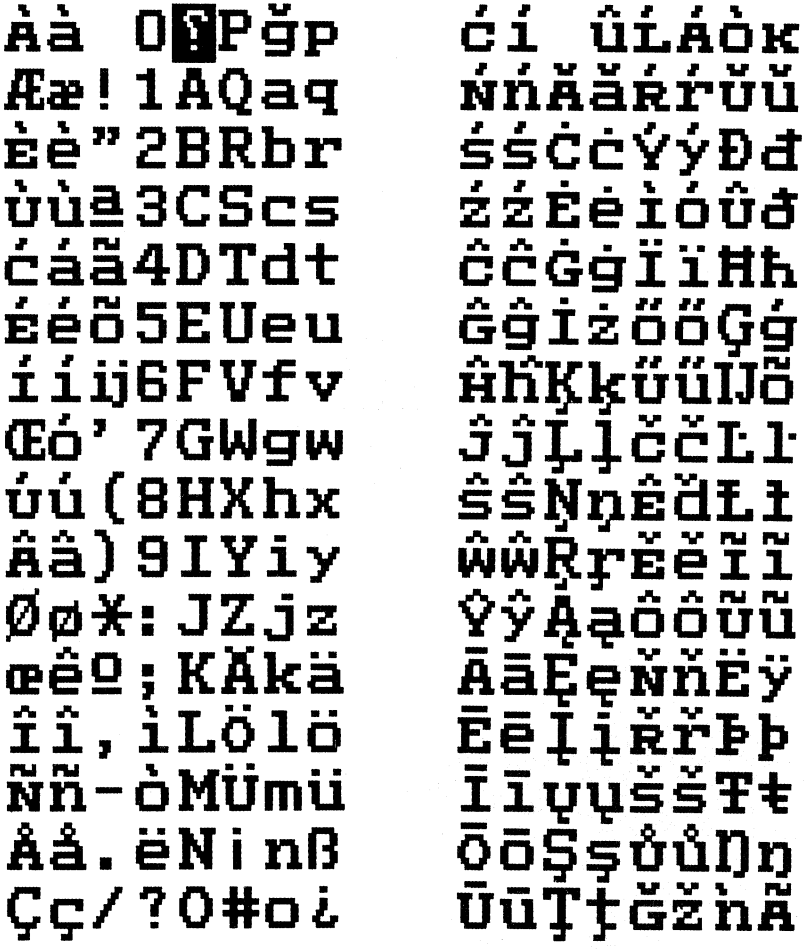
The timing chain operates from an external 6 MHz clock or an on-chip fixed-frequency crystal oscillator. The basic video format is 40 characters per row, 24/25 rows per page and 10 video lines per row. EUROM will also operate with 20/21 rows per page and 12 video lines per row. The two extra lines per row are added symmetrically and contain background colour only for ROM-based alpha-numeric characters. DRCS characters, block and smooth mosaics and line drawing characters occupy all 12 lines.

The display is generated to the normal 625-line/50 Hz scanning standard (interlaced or non-interlaced). In addition to composite sync (pin 32) for conventional timebases, a clock output at 1 MHz or 6 MHz (pin 29) is available for driving other videotex devices, and a 12 MHz clock (pin 27) is available for hard-copy dot synchronization. A defined-display-area timing signal (pin 33) simplifies the application of external peripherals such as a light pen; this signal is nominally coincident with the character dot information.

APPLICATION INFORMATION (continued)

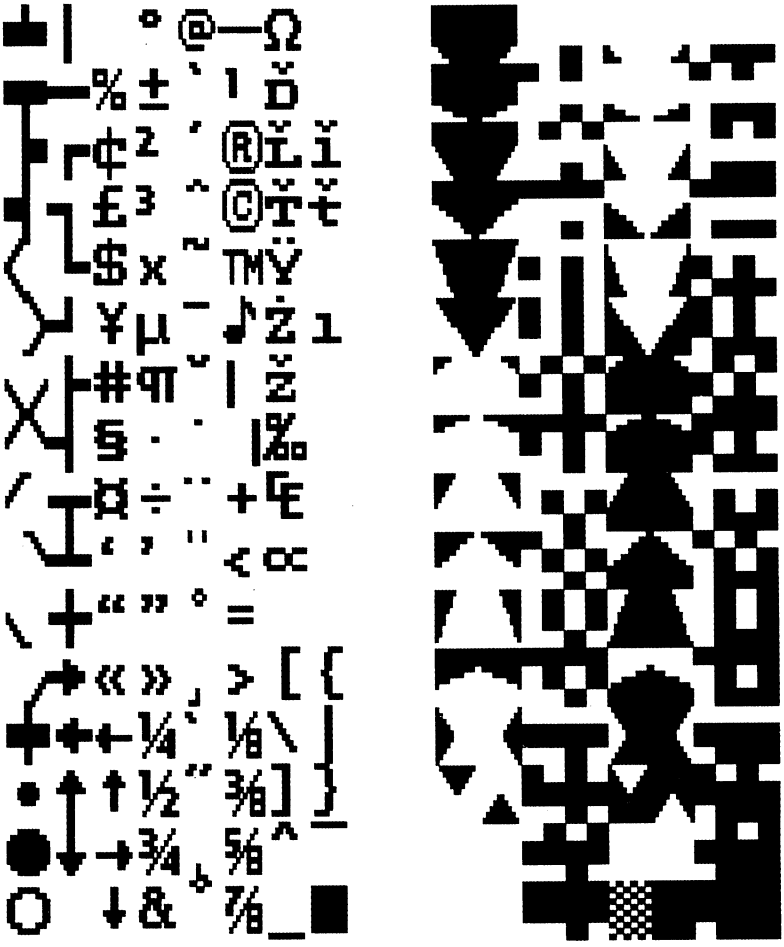
Character generation

EUROM supports eight character tables, each of (nominally) 128 characters. Four tables are in on-chip ROM and contain fixed characters and four are stored in an external RAM. The contents of the fixed character tables (Tables 0 to 3) are shown in Figs 15 and 16.



(a) (b)

Fig. 15 On-chip characters: (a) Table 0; (b) Table 1.



(a) (b)

Fig. 16 On-chip characters: (a) Table 2; (b) Table 3.

APPLICATION INFORMATION (continued)

Character generation (continued)

The 128 most commonly used characters are contained in Table 0, these are the standard upper and lower-case letters of the Roman alphabet, numerals, punctuation and the more common accented characters. In normal text transmission, Table 0 is used most of the time. Table 1 contains other accented characters. Miscellaneous characters, mathematical symbols, the line drawing character set and accents without associated symbols are contained in Table 2. Table 3 contains the block mosaics for the basic alpha-mosaic service and also the new smooth mosaics.

The four tables stored in the external RAM (Tables 4 to 7) are used for DRCS.

Scroll map

The scroll map uses a 26-byte area of on-chip RAM and functions in association with the timing chain. It maps the scan row on to the fetched memory row so allowing the stored page to be displayed in any row order. For each row, a 1-byte pointer to the display memory row is stored in the scroll map. This allows scrolling without the need for data transfer to, or from, side storage.
Additional control bits are stored, allowing 1 to 25 rows to be displayed at any location on the screen.

Colour map and digital-to-analogue converters

The colour map RAM contains thirty-two 12-bit words that are loaded by the microprocessor and read out in three 4-bit groups at pixel rate. Each group is fed to a non-linear (gamma-corrected) D-A converter. The resulting R, G and B outputs are low-impedance with peak-to-peak amplitudes controlled by the reference voltage applied at pin 21.

Cursor

The cursor is available in the stack mode. Its position, character code, character table, foreground colour, background colour, lining and flash attributes are all software programmable via internal register bits.

NON-VIDEOTEX APPLICATIONS

For non-Videotex applications, the device will also support the following operating modes:

Explicit fill mode. An alternative 40 character/rows mode which does not use the memory compression technique of stack coding. More display memory is required but there are no limitations on the number of display attribute changes per row.

80 characters/rows mode. When operating with 80 characters per row, the available display attributes are eight foreground colours, eight (potentially different) background colours (including transparent) as well as underline and blink.

Full field DRCS mode. This mode is not mutually exclusive to the explicit fill and 80 characters/rows modes but rather the available DRCS memory is expanded so that the whole screen can be covered, thus enabling a 'bit map'. All ROM-based characters and all display attributes remain available.

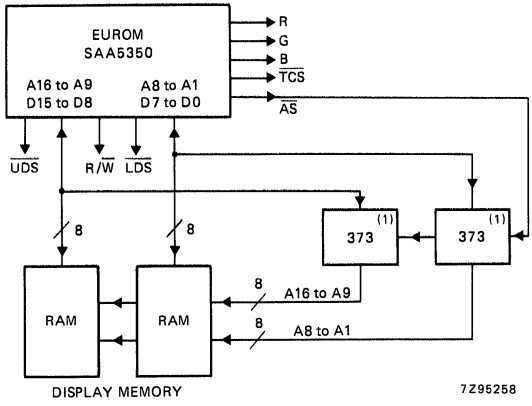
MICROPROCESSOR and RAM BUS INTERFACE

Three types of data transfer take place at the bus interface:

- EUROM fetches data from the display memory
- The microprocessor reads from, or writes to, EUROM's internal register map
- The microprocessor accesses the display memory

EUROM access to display memory (Figs 17 and 18)

EUROM accesses the external display memory via a 16-bit multiplexed address and data bus with a cycle time of 500 ns. The address strobe ($\overline{AS}$) signal from EUROM flags the bus cycle and writes the address into octal latches (74LS373). The display data is stored in bytes of upper (most-significant) and lower (least-significant) display information and is always fetched in pairs of bytes (upper + lower = 16 bits). The upper and lower display RAM sections are enabled simultaneously by the upper and lower data strobes (respectively $\overline{UDS}$ and $\overline{LDS}$) which are always asserted together to fetch a 16-bit word. The read/write control R/$\overline{W}$ is included although EUROM only reads from the display memory.



(1) 74LS373 octal transparent latch (3-state)

Fig. 17 Simple RAM interface circuit for display memory access.

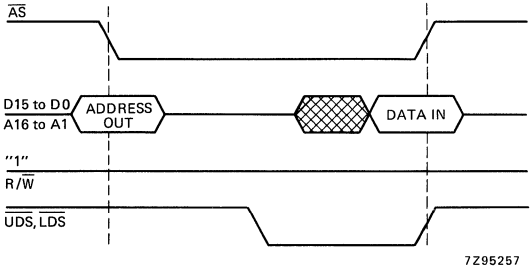


Fig. 18 Bus timing for display memory access.

APPLICATION INFORMATION (continued)

EUROM access to display memory (continued)

The display memory organization uses the word/byte addressing convention adopted for the SCN68000 microprocessor series. Data fetched on the 16-bit bus is considered in terms of bytes where the even numbered bytes use the upper (most-significant) part of the bus as shown in Fig. 19. The word addresses are numerically the same as the upper byte that they contain — there are no odd-numbered word addresses.

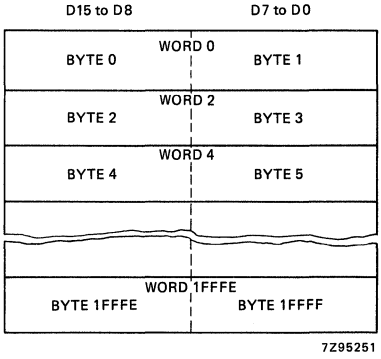


Fig. 19 Display memory word/byte organization.

Warning time

As EUROM is a real-time display device, it must have direct access to the display memory with priority over the microprocessor and other peripheral devices. This is achieved by EUROM issuing a bus request ($\overline{BR}$) signal for the duration of the memory access plus a programmable advance warning time which allows the microprocessor to complete its current bus cycle.

In systems where the buses of the microprocessor and EUROM are intimately connected (connected systems), $\overline{BR}$ may be used to suspend all microprocessor activity so that EUROM can act as a dedicated DMA controller. In systems where the two buses are separated by buffers (disconnected systems), $\overline{BR}$ may be used either to generate an interrupt or as a direct signal. To these ends, the warning time between the assertion of $\overline{BR}$ and the beginning of EUROM's bus activity is programmable to be between 0 and 23 μs.

Microprocessor access to register map

EUROM has a set of internal registers which, when memory-mapped, behave as an 8-bit wide RAM connected to the upper part of the data bus (Fig. 20). The control signals $\overline{UDS}$ and R/$\overline{W}$ are reversed to become inputs and the register map is enabled by the signal $\overline{RE}$. Addresses are input via the lower part of the bus. A data transfer acknowledge signal ($\overline{DTACK}$) indicates to the microprocessor that the data transfer is complete.

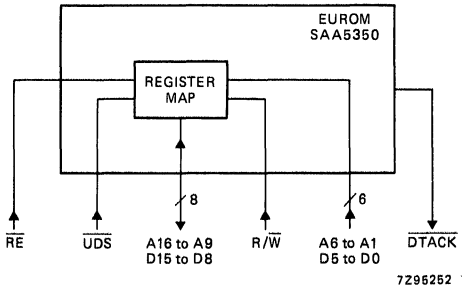


Fig. 20 Microprocessor access to register map.

The main data and address paths used in a connected 68000 interface are shown in Fig. 21. The outputs from the octal latches (74LS373) are enabled only when the 68000 has made the bus available in response to a bus request ($\overline{BR}$). When the register map is accessed data is transferred via the upper part of the bus and the microprocessor's low-order address is passed to EUROM via the octal buffers (74LS244). At the same time the bidirectional buffers (74LS245) disable the signals from the low order data bus of the 68000.

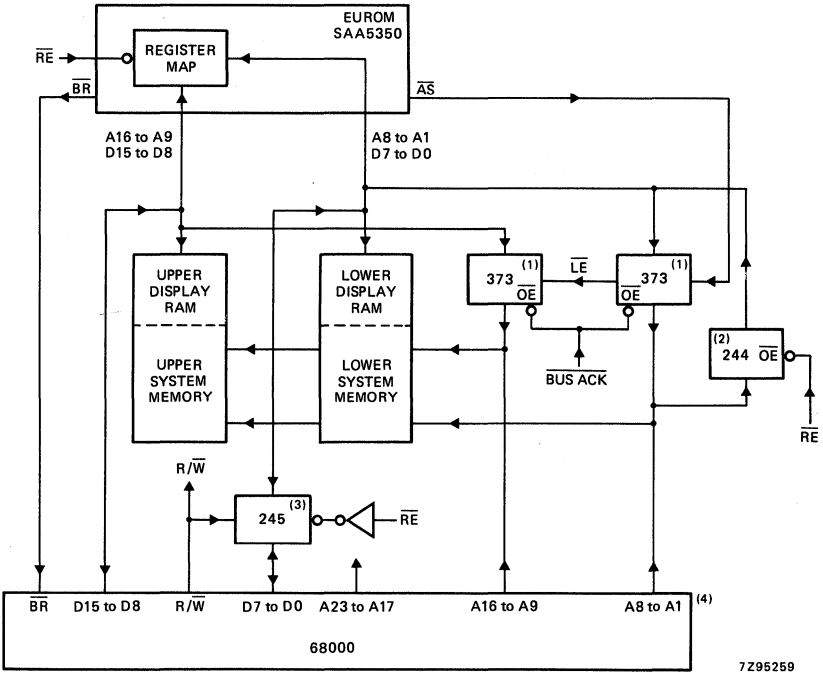
The buffers '244 and '245 may be omitted in a 16-bit write-only configuration where the least-significant data byte is interpreted by EUROM as an address. Here it will generally be necessary for the microprocessor to hold a (readable) 'master copy' of EUROM's scroll map contents at a location in its main memory.

8-bit microprocessors

Although the control bus is optimised for the SCN68000 16-bit microprocessor unit, EUROM will operate with a number of widely differing industry-standard 8, 16 or more-bit microprocessors or microcontrollers (e.g. SCN68008, MAB8051). The interfacing of 8-bit microprocessors to the 16-bit wide display memory is made simple by EUROM's on-chip link-through buffer which provides the microprocessor with bidirectional access to the lower (odd) half of the memory. The link-through buffer is enabled by the buffer-enable signal $\overline{BUFEN}$, and the send/receive direction is controlled by the signal $\overline{S}$/R.

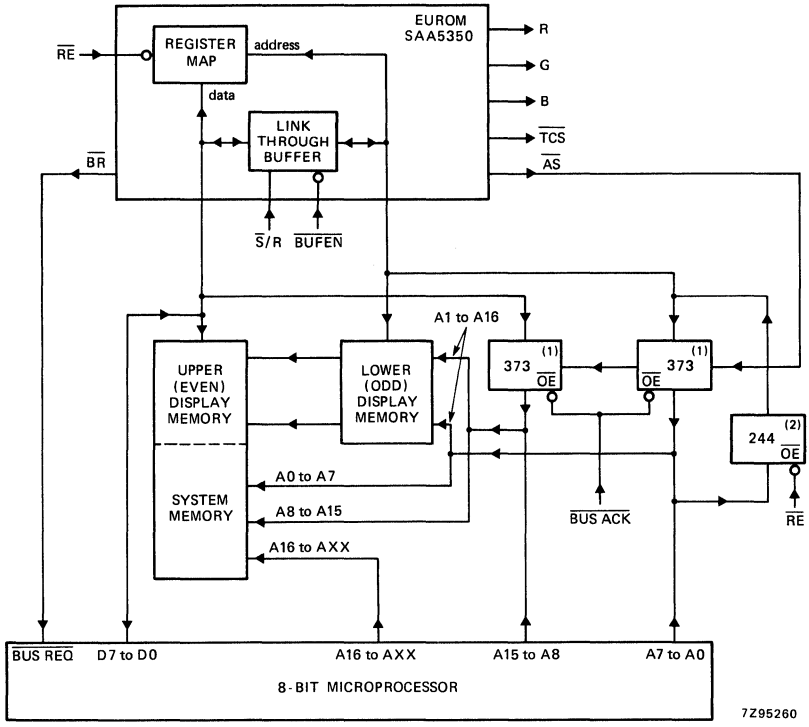
The main data and address paths used in a connected 8-bit microprocessor system are shown in Fig. 22. The interface is similar to that of the 16-bit system but here the display memory does not receive A0 as an address, rather A0 is used as the major enabling signal for $\overline{BUFEN}$ (enables when HIGH).

APPLICATION INFORMATION (continued)



(1) 74LS373 octal transparent latch (3-state)
(2) 74LS244 octal buffer (3-state)
(3) 74LS245 octal bus transceiver (3-state)
(4) SCN68000 microprocessor unit

Fig. 21 Connected 16-bit microprocessor system.



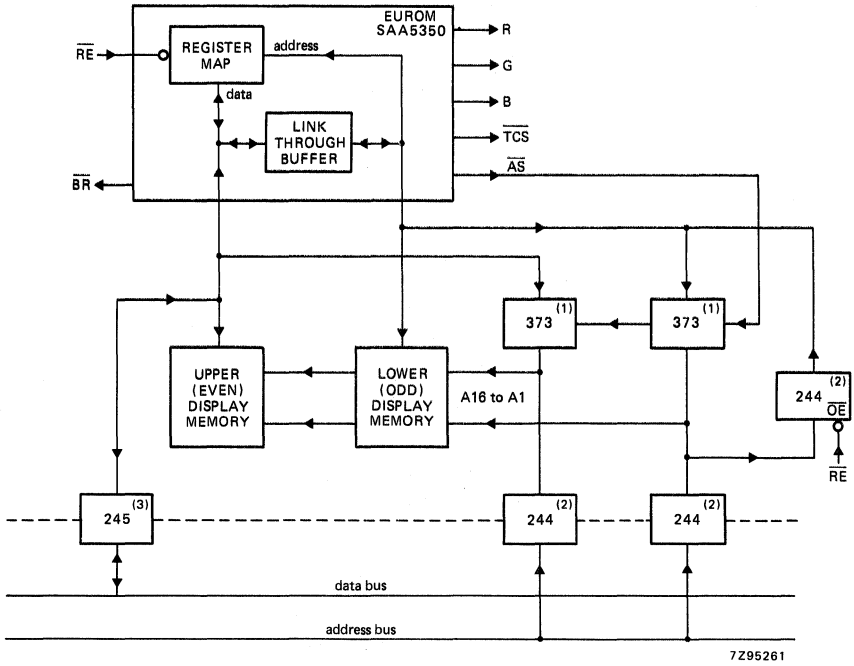
(1) 74LS373 octal transparent latch (3-state)
(2) 74LS244 octal buffer (3-state)

Fig. 22 Connected 8-bit microprocessor system.

APPLICATION INFORMATION (continued)

Disconnected systems

For many applications it may be desirable to disconnect EUROM and the display memory from the microprocessor and its ROM, RAM and other peripherals by using isolating buffers as shown in Fig. 23. The two parts of the system then operate independently and communicate only when the microprocessor accesses EUROM's register map or the display memory.



(1) 74LS373 octal transparent latch (3-state)
(2) 74LS244 octal buffer (3-state)
(3) 75LS245 octal bus transceiver (3-state)

Fig. 23 Disconnected 8-bit system.

Synchronization

Stand-alone mode

As a stand-alone device (e.g. in terminal applications) EUROM can output a composite sync signal ($\overline{TCS}$) to the display timebase IC or to a monitor. Timing is obtained from a 6 MHz on-chip oscillator using an external crystal as shown in Fig. 24.

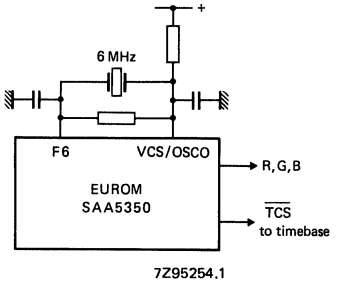


Fig. 24 Stand-alone synchronization mode.

Simple-slave

In the simple-slave mode EUROM synchronizes directly to another device, such as to the $\overline{TCS}$ signal from the SAA5240 European computer-controlled teletext circuit (CCT) or from another EUROM as shown in Fig. 25. EUROM's horizontal counter is reset by the falling edge of $\overline{TCS}$. A dead time of 250 ns is built in to avoid resetting the counter at every tv line and so prevents screen jitter.
Field synchronization is made using EUROM's internal field sync separator.

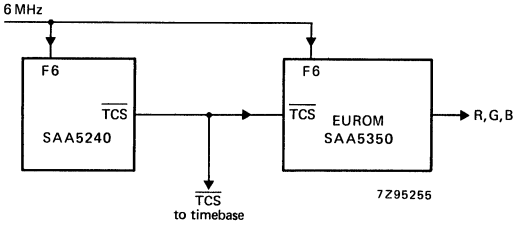


Fig. 25 Simple-slave (direct sync) mode.

APPLICATION INFORMATION (continued)

Synchronization (continued)

Phase-locked slave

The phase-locked slave (indirect sync) mode is shown in Fig. 26. A phase-locked VCO in the SAA5230 teletext video processor provides sync to the timebases. When EUROM is active, its horizontal counter forms part of the phase control loop — a horizontal reference is fed back to the SAA5230 from the SAND output and a vertical reference is generated by feeding separated composite sync to EUROM's field sync separator via the VCS input. In the phase-locked slave mode, the display derived from EUROM can sync with that from a tv source or a local VLP player, thus giving picture-in-text display possiblities.

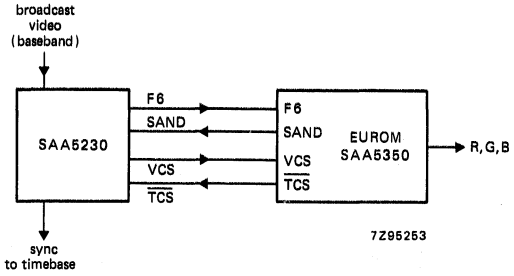


Fig. 26 Phase-locked slave (indirect sync) mode.

SENSITIVE 1 GHz DIVIDER-BY-64

This silicon monolithic integrated circuit is a prescaler in current-mode logic. It contains an amplifier, a divide-by-64 scaler and an output stage. It has been designed to be driven by a sinusoidal signal from the local oscillator of a television tuner, with frequencies from 70 MHz up to 1 GHz, for a supply voltage of 5 V ± 10% and an ambient temperature of 0 to 70 °C. It features a high sensitivity and low harmonic contents of the output signal.

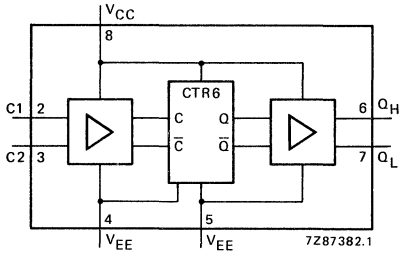


Fig. 1 Block diagram. CTR6 = 6 binary dividers = (÷ 64).

QUICK REFERENCE DATA

Supply voltage (pin 8)	V_{CC}	5 ± 10%	V
Input frequency range (pins 2 and 3)	f_i	70 to 1000	MHz
Output voltage swing (pins 6 and 7)	$V_{o(p\text{-}p)}$	typ. 1	V
Supply current; unloaded (pin 8)	I_{CC}	typ. 42	mA
Operating ambient temperature	T_{amb}	0 to + 70	°C

PACKAGE OUTLINES

SAB1164P: 8-lead DIL; plastic (SOT-97A).
SAB1165P: 8-lead DIL; plastic (SOT-97A).

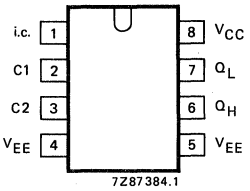


Fig. 2 Pinning diagram.

PINNING

V_{CC}	positive supply
V_{EE}	0 V; ground
C_1, C_2	differential inputs
Q_H, Q_L	complementary outputs
i.c.	internally connected

FUNCTIONAL DESCRIPTION

The circuit contains an amplifier, a divide-by-64 scaler and an output stage. It has been designed to be driven by a sinusoidal signal from the local oscillator of a TV tuner, with frequencies from 70 MHz up to 1 GHz, for a supply voltage of 5 V ± 10% and an ambient temperature of 0 to 70 °C.

The inputs are differential and are internally biased to permit capacitive coupling. For asymmetrical drive the unused input should be connected to ground via a capacitor.

The first divider stage will oscillate in the absence of an input signal; an input signal within the specified range will suppress this oscillation.

The output differential stage has two complementary outputs. The output voltage edges are slowed down internally to reduce the harmonic contents of the signal.

Wide, low-impedance ground connections and a short capacitive bypass from the V_{CC} pin to ground are recommended.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (d.c.)	V_{CC}	max.	7 V
Input voltage	V_i		0 to V_{CC} V
Storage temperature	T_{stg}		−55 to + 125 °C
Junction temperature	T_j	max.	125 °C

THERMAL RESISTANCE

From crystal to ambient	$R_{th\ c\text{-}a}$	=	120 K/W

D.C. CHARACTERISTICS

V_{EE} = 0 V (ground); V_{CC} = 5 V; T_{amb} = 25 °C unless otherwise specified.

The circuit has been designed to meet the d.c. specifications as shown below, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed-circuit board.

Output voltage				
HIGH level	V_{OH}	max.	V_{CC}	V
LOW level	V_{OL}	max.	V_{CC}−0,8	V
Supply current	I_{CC}	typ.	42	mA
		max.	50	mA

A.C. CHARACTERISTICS

V_{EE} = 0 V (ground); V_{CC} = 5 V ± 10%; T_{amb} = 0 to + 70 °C.

		min.	typ.	max.	unit
Input voltage r.m.s. value (see Fig. 4)					
input frequency 70 MHz	$V_{i(rms)}$	–	9	17,5	mV
150 MHz		–	4	10	mV
300 MHz		–	3	10	mV
500 MHz		–	3	10	mV
900 MHz		–	2	10	mV
1 GHz		–	3	17,5	mV
Input overload voltage r.m.s. value					
input frequency range 70 MHz up to 1 GHz	$V_{i(rms)}$	–	–	200	mV
Output voltage swing	$V_{o(p-p)}$	0,8	1	–	V
Output resistance					
SAB1164	R_o	–	1	–	kΩ
SAB1165	R_o	–	0,5	–	kΩ
Output unbalance	ΔV_o	–	–	0,1	V
Output rise time*					
f_i = 1 GHz	t_{TLH}	–	25	–	ns
Output fall time*					
f_i = 1 GHz	t_{THL}	–	25	–	ns

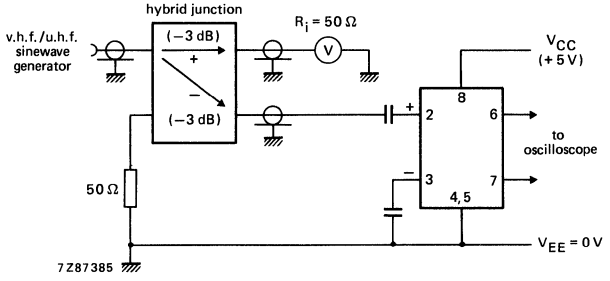


Fig. 3 Test circuit for defining input voltage.

– Cables must be 50 Ω coaxial.
– The capacitors are leadless ceramic (multilayer capacitors) of 10 nF.
– All connections to the device and to the meter must be kept short and of approximately equal lengths.
– Hybrid junction is ANZAC H-183-4 or similar.

* Between 10% and 90% of observed waveform.

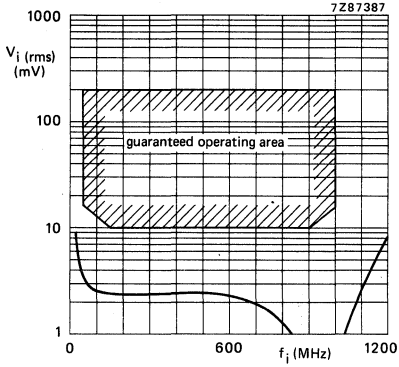


Fig. 4 Typical sensitivity curve under nominal conditions.

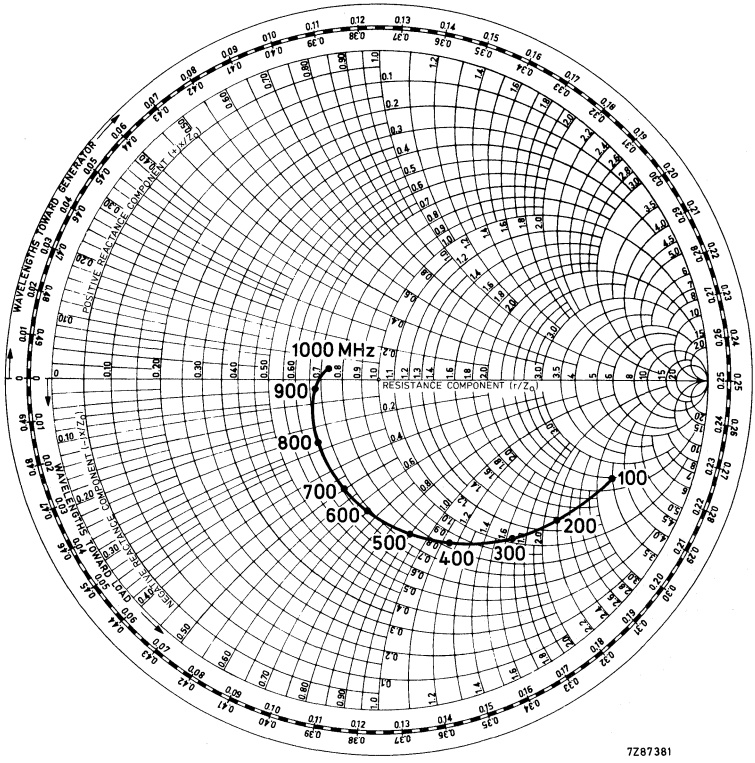


Fig. 5 Smith chart of typical input impedance.
$V_{i(rms)}$ = 25 mV; V_{CC} = 5 V; reference value = 50 Ω.

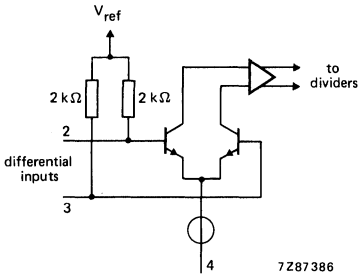


Fig. 6 Input stage.

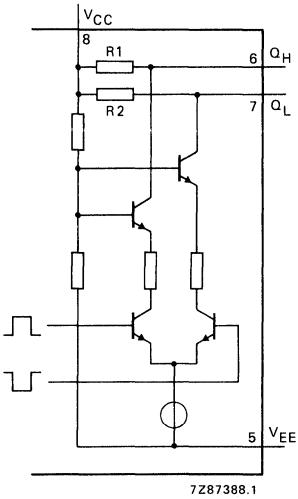


Fig. 7 Output stage. V_{CC} = 5 V.
SAB1164: R1 = R2 = 1 kΩ; I = 1 mA
SAB1165: R1 = R2 = 0,5 kΩ; I = 2 mA.

APPLICATION INFORMATION

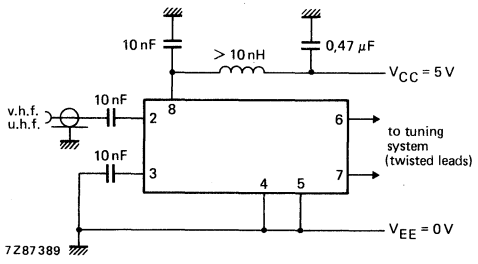


Fig. 8 Circuit diagram. Application in a television tuning system.
The output peak-to-peak voltage is about 1 V.

SENSITIVE 1 GHz DIVIDER-BY-256

This silicon monolithic integrated circuit is a prescaler in current-mode logic. It contains an amplifier, a divide-by-256 scaler and an output stage. It has been designed to be driven by a sinusoidal signal from the local oscillator of a television tuner, with frequencies from 70 MHz up to 1 GHz, for a supply voltage of 5 V ± 10% and an ambient temperature of 0 to 70 °C. It features a high sensitivity and low harmonic contents of the output signal.

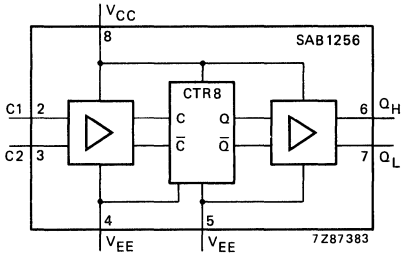


Fig. 1 Block diagram. CTR8 = 8 binary dividers = (÷ 256).

QUICK REFERENCE DATA

Supply voltage (pin 8)	V_{CC}	5 ± 10%	V
Input frequency range (pins 2 and 3)	f_i	70 to 1000	MHz
Output voltage swing (pins 6 and 7)	$V_{o(p-p)}$	typ. 1	V
Supply current, unloaded (pin 8)	I_{CC}	typ. 47	mA
Operating ambient temperature	T_{amb}	0 to + 70	°C

PACKAGE OUTLINE

SAB1256P: 8-lead DIL; plastic (SOT-97A).

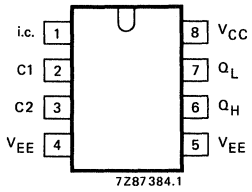


Fig. 2 Pinning diagram.

PINNING

V_{CC}	positive supply
V_{EE}	0 V; ground
C_1, C_2	differential inputs
Q_H, Q_L	complementary outputs
i.c.	internally connected

FUNCTIONAL DESCRIPTION

The circuit contains an amplifier, a divide-by-256 scaler and an output stage. It has been designed to be driven by a sinusoidal signal from the local oscillator of a TV tuner, with frequencies from 70 MHz up to 1 GHz, for a supply voltage of 5 V ± 10% and an ambient temperature of 0 to 70 °C.

The inputs are differential and are internally biased to permit capacitive coupling. For asymmetrical drive the unused input should be connected to ground via a capacitor.

The first divider stage will oscillate in the absence of an input signal; an input signal within the specified range will suppress this oscillation.

The output differential stage has two complementary outputs. The output voltage edges are slowed down internally to reduce the harmonic contents of the signal.

Wide, low-impedance ground connections and a short capacitive bypass from the V_{CC} pin to ground are recommended.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (d.c.)	V_{CC}	max.	7 V
Input voltage	V_i	0 to V_{CC}	V
Storage temperature	T_{stg}	−55 to + 125	°C
Junction temperature	T_j	max. 125	°C

THERMAL RESISTANCE

From crystal to ambient	$R_{th\ c\text{-}a}$	=	120 K/W

D.C. CHARACTERISTICS

V_{EE} = 0 V (ground); V_{CC} = 5 V; T_{amb} = 25 °C unless otherwise specified.

The circuit has been designed to meet the d.c. specifications as shown below, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed-circuit board.

Output voltage				
HIGH level	V_{OH}	max.	V_{CC}	V
LOW level	V_{OL}	max.	V_{CC}–0,8	V
Supply current	I_{CC}	typ.	47	mA
		max.	55	mA

A.C. CHARACTERISTICS

V_{EE} = 0 V (ground); V_{CC} = 5 V ± 10%; T_{amb} = 0 to + 70 °C.

		min.	typ.	max.	unit
Input voltage r.m.s. value (see Fig. 4)					
input frequency 70 MHz	$V_{i(rms)}$	–	9	17,5	mV
150 MHz		–	4	10	mV
300 MHz		–	3	10	mV
500 MHz		–	3	10	mV
900 MHz		–	2	10	mV
1 GHz		–	3	17,5	mV
Input overload voltage r.m.s. value					
input frequency range 70 MHz to 1 GHz	$V_{i(rms)}$	–	–	200	mV
Output voltage swing	$V_{o(p-p)}$	0,8	1	–	V
Output resistance	R_o	–	1	–	kΩ
Output unbalance	ΔV_o	–	–	0,1	V
Output rise time*					
f_i = 1 GHz	t_{TLH}	–	40	–	ns
Output fall time					
f_i = 1 GHz	t_{THL}	–	40	–	ns

* Between 10% and 90% of observed waveform.

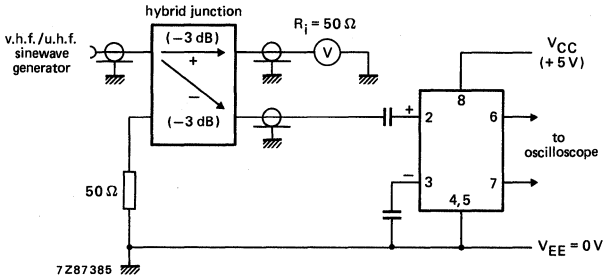


Fig. 3 Test circuit for defining input voltage.

- Cables must be 50 Ω coaxial.
- The capacitors are leadless ceramic (multilayer capacitors) of 10 nF.
- All connections to the device and to the meter must be kept short and of approximately equal lengths.
- Hybrid junction is ANZAC H-183-4 or similar.

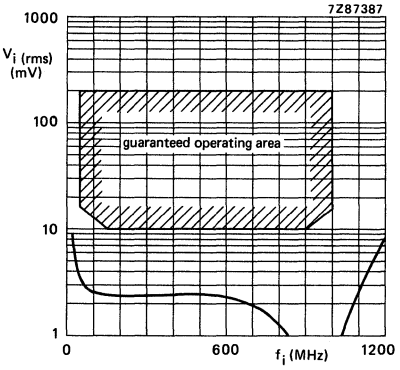


Fig. 4 Typical sensitivity curve under nominal conditions.

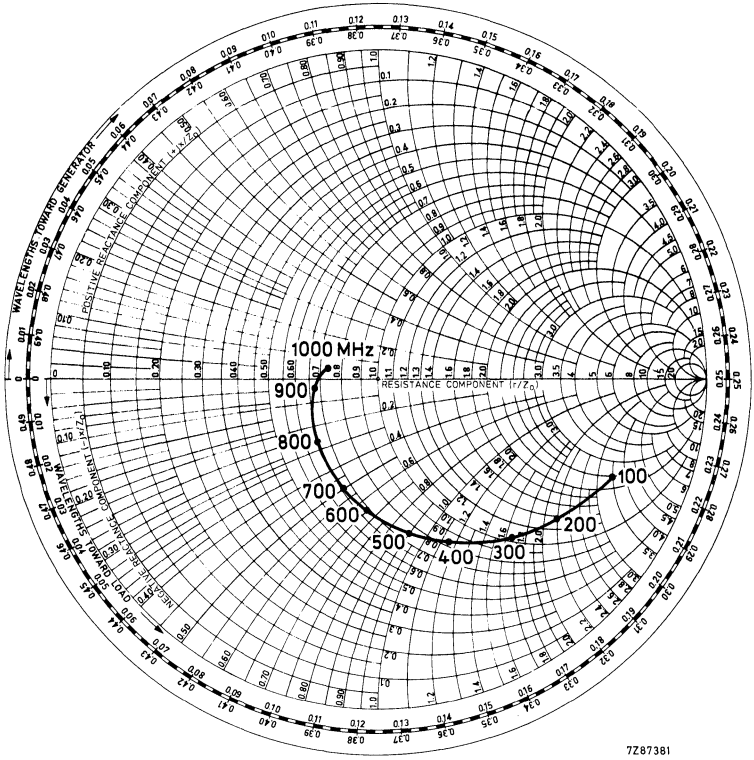


Fig. 5 Smith chart of typical input impedance.
$V_{i(rms)}$ = 25 mV; V_{CC} = 5 V; reference value = 50 Ω.

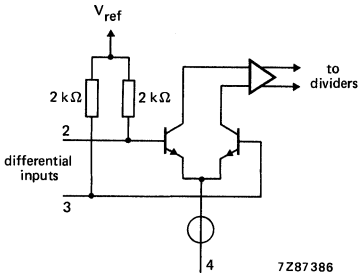


Fig. 6 Input stage.

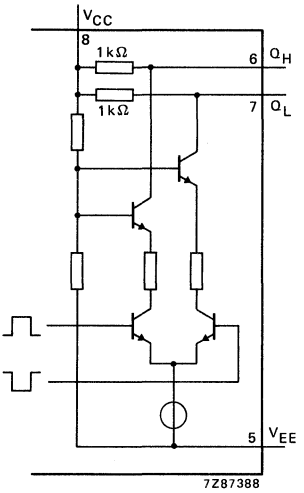


Fig. 7 Output stage.
V_{CC} = 5 V; I = 1 mA.

APPLICATION INFORMATION

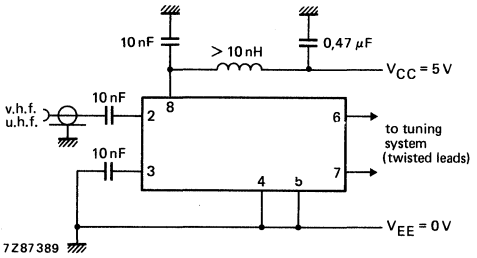


Fig. 8 Circuit diagram.
Application in a television tuning system. The output peak-to-peak voltage is about 1 V.

6-FUNCTION ANALOGUE MEMORY; MICROCOMPUTER CONTROLLED

The SAB3013 is a MOS N-channel integrated circuit which provides 6 analogue memories controlled by a microcomputer.

Features

- 6-function analogue memory; D/A converter with 6-bit resolution.
- The output of the analogue values is pulse-width modulated with adjustable repetition rate (max. 21,8 kHz).
- Microcomputer-adapted asynchronous serial interface for data input (CBUS).
- Parallel operation of up to four SAB3013 circuits is possible.

QUICK REFERENCE DATA

Supply voltage	V_{DD}	typ.	5 V
Operating ambient temperature range	T_{amb}	0 to	+70 °C
Clock frequency	f_{CLK}	<	1,4 MHz
Supply current; V_{DD} = 5 V; I_O = 0; T_{amb} = 25 °C	I_{DD}	typ.	15 mA

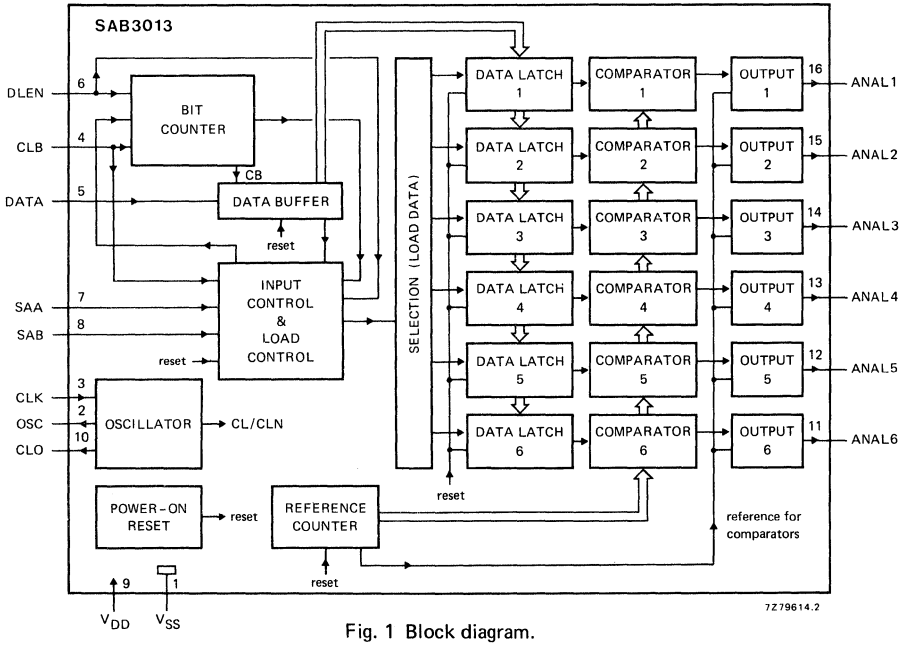


Fig. 1 Block diagram.

PACKAGE OUTLINE

16-lead DIL; plastic (SOT-38).

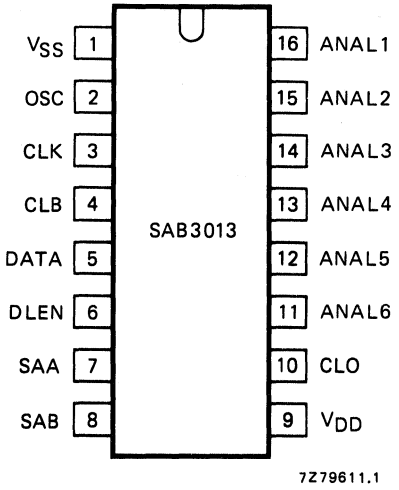


Fig. 2 Pinning diagram.

PINNING

1	V_{SS}	ground (0 V)	
9	V_{DD}	positive supply	
4	CLB	asynchronous clock pulse	CBUS
5	DATA	data input	CBUS
6	DLEN	data line enable input	CBUS
7	SAA	address inputs	
8	SAB	address inputs	
2	OSC	oscillator output	
3	CLK	oscillator input (Schmitt-trigger)	
16	ANAL1	analogue outputs	
15	ANAL2	analogue outputs	
14	ANAL3	analogue outputs	
13	ANAL4	analogue outputs	
12	ANAL5	analogue outputs	
11	ANAL6	analogue outputs	
10	CLO	buffered oscillator output	

GENERAL DESCRIPTION

The SAB3013 is designed to deliver analogue values in microcomputer-controlled television receivers and radio receivers. The circuit comprises an analogue memory and D/A converter for 6 analogue functions with a 6-bit resolution for each. The information for the analogue memory is transfered by the microcomputer via an asynchronous serial data bus.

The SAB3013 accomplishes a word format recognition, so it is able to operate one common data bus together with circuits having different word formats.

The data word of the microcomputer used for the SAB3013 consists of information for addressing the appropriate SAB3013 circuit (2-bits), for addressing the analogue memories concerned (3-bits) and processing of the wanted analogue value (6-bits). The address of the circuit is externally programmable via two inputs. It is possible to address up to four SAB3013 circuits via one common bus.

The built-in oscillator can be used for a frequency between 30 kHz and 1,4 MHz. The analogue values are generated as a pulse pattern with a repetition rate of $f_{CLK}/64$ (max. 21,8 kHz at f_{CLK} = 1,4 MHz), and the analogue values are determined by the ratio of the HIGH-time and the cycle time. A d.c. voltage proportional to the analogue value is obtained by means of an external integration network (low-pass filter).

HANDLING

Inputs and outputs are protected against electrostatic charge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see 'Handling MOS Devices').

RATINGS

Limiting values in accordance to the Absolute Maximum System (IEC 134)

Supply voltage range	V_{DD}	−0,3 to + 7,5	V
Input voltage range	V_I	−0,3 to + 15	V
Input current	$\pm I_I$	max. 100	μA
Output voltage (open drain outputs)	V_O	V_{SS} to 15	V
Output current (open drain/push-pull outputs)	$\pm I_O$	max. 10	mA
Power dissipation per output	P_O	max. 25	mW
Total power dissipation per package	P_{tot}	max. 250	mW
Operating ambient temperature range	T_{amb}	0 to + 70	°C
Storage temperature range	T_{stg}	−20 to + 125	°C

CHARACTERISTICS

V_{SS} = 0; T_{amb} = 0 to + 70 °C; V_{DD} = 4,5 to 5,5 V; unless otherwise specified

	symbol	min.	typ.	max.	conditions
Supply voltage	V_{DD}	4,5	5	5,5 V	
Supply current	I_{DD}	–	–	35 mA	V_{DD} = 5,5 V
Inputs DATA, CLB, DLEN, SAA, SAB					
Input voltage LOW	V_{IL}	0	–	12 V	
Input voltage HIGH	V_{IH}	2,0	–	12 V	
Input leakage current	I_{IR}	–	–	1 μA	V_I = –0,3 to + 12 V
Outputs ANAL1 to ANAL6 (open drain)					
Output voltage LOW	V_{OL}	–	–	0,7 V	I_O = 6 mA
Output leakage current	I_{OR}	–	–	20 μA	V_{OH} = 15 V *
Load capacitance	C_L	–	–	1000 pF	
Input CLK					
Input voltage LOW	V_{IL}	–0,3	–	0,8 V	
Input voltage HIGH	V_{IH}	3,5	–	12 V	
Input leakage current	I_{IR}	–	–	1 μA	V_I = –0,3 to 12 V
Pulse duration HIGH	t_{WH}	355	–	– ns	
Pulse duration LOW	t_{WL}	355	–	– ns	
Output CLO					
Output voltage LOW	V_{OL}	–	–	0,8 V	I_O 500 μA
Output voltage HIGH	V_{OH}	3,5	–	– V	$-I_O$ = 100 μA
Inputs DATA, CLB					
Pulse duration HIGH	t_{WH}	450	–	– ns	see Fig. 3
Pulse duration LOW	t_{WL}	450	–	– ns	see Fig. 3
Input frequency CLB	f_{CLB}	0	–	1 MHz	
Internal oscillator CLK/OSC					
External resistor	R	27	–	1000 kΩ	
External capacitor	C	27	–	1000 pF	
Clock frequency	f_{CLK}	0,7	1,0	1,4 MHz	R = 27 kΩ; C = 27 pF
Frequency for external oscillator	f_{CLK}	0,03	–	1,4 MHz	

* For correct operation: V_{OHmin} = 3 V.

CHARACTERISTICS (continued)

V_{SS} = 0; T_{amb} = 0 to +70 °C; V_{DD} = 4,5 to 5,5 V; unless otherwise specified

	symbol	min.	typ.	max.		conditions
Timing (see Fig. 3)						
Data set-up time DATA → CLB	t_{SUDA}	800	–	–	ns	measured with a voltage swing of min. V_{IH}–V_{IL}
Data hold time DATA → CLB	t_{HDDA}	300	–	–	ns	
Enable set-up time DLEN → CLB	t_{SUEN}	400	–	–	ns	
Disable set-up time CLB → DLEN	t_{SUDI}	400	–	–	ns	
Set-up time DLEN → CLB (load pulse)	t_{SULD}	1000	–	–	ns	

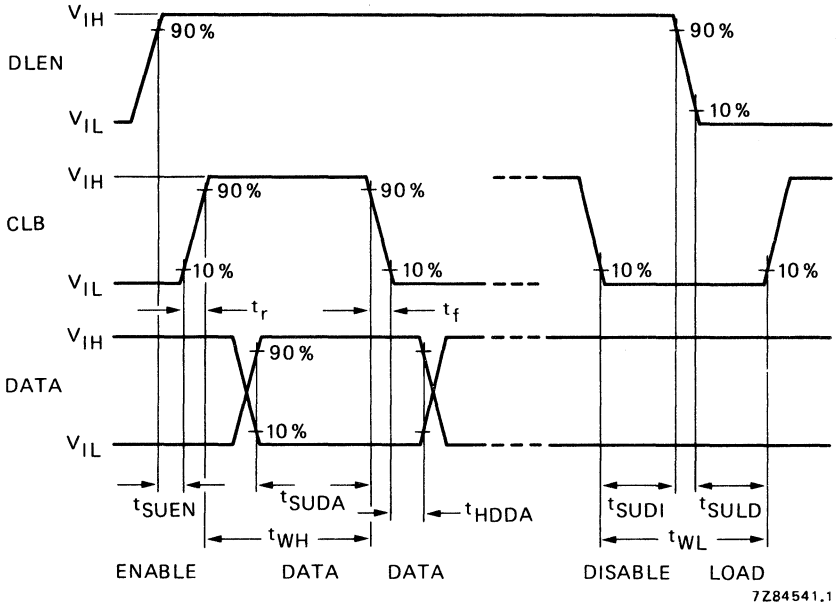


Fig. 3 CBUS timing.

OPERATION DESCRIPTION

The data input is achieved serially via the inputs DATA, DLEN and CLB. Clock pulses have to be applied at input CLB for data processing at input DATA. Data processing is only possible when DLEN = HIGH. The data from the data buffer is loaded directly into the output latch on receipt of a load pulse at input CLB (DLEN = LOW), provided the following conditions are met:

- 12 clock pulses must be received at input CLB (word format control) during transmission (DLEN = HIGH).
- The start-bit must be LOW.
- The system address bits must be A = SAA and B = SAB.
- The analogue address must be valid.

The data word for the SAB3013 consists of the following bits (see Fig. 4):

1 start-bit
2 system address bits (A and B)
3 address bits for selection of the required analogue memory
6 data bits for processing the analogue value

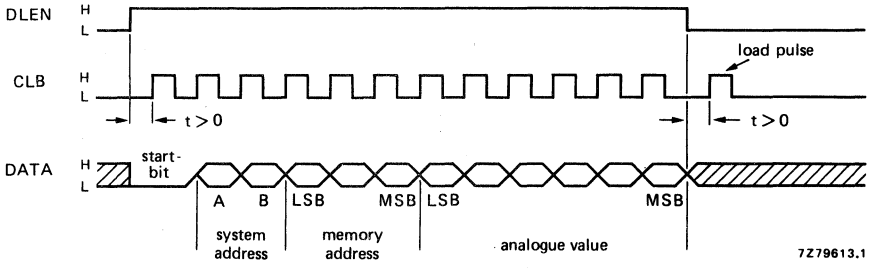


Fig. 4 Waveforms showing a CBUS transmission.

ADDRESS inputs (SAA, SAB)

The address of the SAB3013 is programmed at the inputs SAA and SAB. These inputs must be defined and not left open-circuit.

Reset

The circuit generates internally a reset-cycle with a duration of one clock cycle after switching on the supply. If a spike on the supply is likely to destroy data, a reset signal will be generated. All analogue memories are set to 50% (analogue value 32/64) after the reset cycle. The supply voltage rise dV_{DD}/dt must be max. 0,5 V/μs and min. 0,2 V/μs.

Oscillator inputs (CLK, OSC)

The oscillator frequency is determined by the external circuitry connected to the terminals CLK and OSC as shown in Fig. 5. Instead of this circuitry an externally generated oscillator signal can be connected to input CLK.

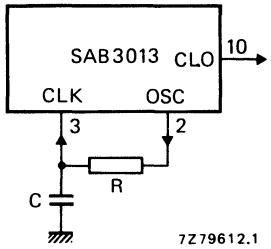


Fig. 5 Application advice for the oscillator.

At output CLO a buffered oscillator signal is available for control of other circuits.

For f_{CLK} = 0,7 to 1,4 MHz;
R = 27 kΩ; C = 27 pF.

Analogue outputs (ANAL1 to ANAL6)

The analogue values are generated as a pulse pattern with a repetition rate of $f_{CLK}/64$ at the outputs ANAL1 to ANAL6. The analogue value is determined by the ratio of the HIGH-time and the cycle time (values between 1/64 and 64/64 can be obtained).

Table 1 Addressing of the analogue data registers

R_A LSB	R_B	R_C MSB	addressing
0	0	0	not valid
1	0	0	ANAL1
0	1	0	ANAL2
1	1	0	ANAL3
0	0	1	ANAL4
1	0	1	ANAL5
0	1	1	ANAL6
1	1	1	not valid

Table 2 Correlation of analogue value to analogue output signal

analogue value	binary input data LSB					MSB	duty cycle 'low'	'high'
lowest value	0	0	0	0	0	0	63/64	1/64
	1	0	0	0	0	0	62/64	2/64
power-on reset value	1	1	1	1	1	0	32/64	32/64
highest value	0	1	1	1	1	1	1/64	63/64
	1	1	1	1	1	1	0	64/64

ANALOGUE AND TUNING CIRCUIT (A & T)

The SAB3034 is a MOS N-channel analogue and tuning (A & T) integrated circuit which provides closed loop digital tuning and control of up to six analogue functions. The IC is used in combination with a microcomputer.

Features

- Tuning by comparison of the required frequency with the actual value; digital tuning windows selectable: 250 kHz to 500 kHz.
- Tuning with a.f.c.: holding range selectable from 1 MHz to 1,5 MHz.
- 4 MHz quartz crystal oscillator or a 400 kHz synchronization from the microcomputer.
- Four tuning pulse widths selectable, so the characteristics of various tuners can be accommodated.
- Simple tuning interface.
- Digital output signal for correct tuning.
- Six 63-step digital to analogue converters.
- CBUS interface for 12-bit data words.

QUICK REFERENCE DATA

Supply voltage	V_{DD}	typ.	5 V
Operating ambient temperature range	T_{amb}		0 to + 70 °C
Supply current	I_{DD}	typ.	18 mA

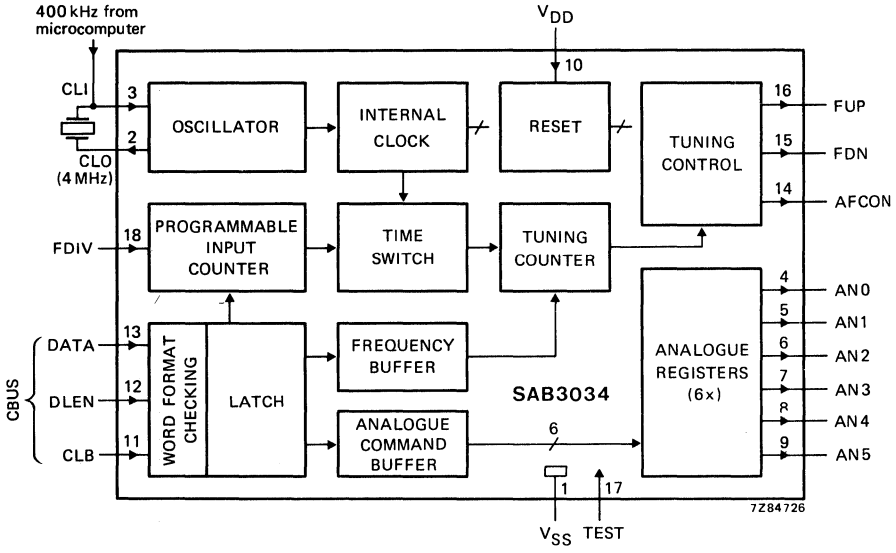


Fig. 1 Block diagram.

PACKAGE OUTLINE

18-lead DIL; plastic (SOT-102CS).

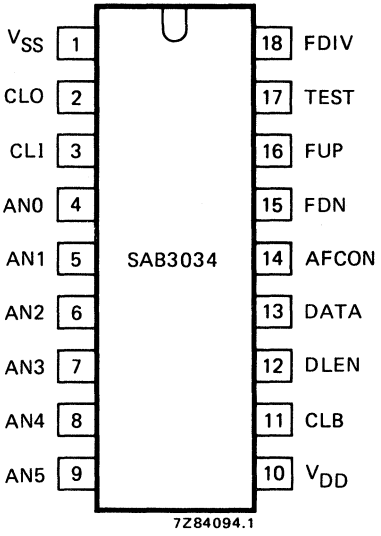


Fig. 2 Pinning diagram.

PINNING

1	V_{SS}	ground (0 V)
10	V_{DD}	positive supply (+ 5 V)
13	DATA	data word (CBUS input)
12	DLEN	data line enable (CBUS input)
11	CLB	clock burst (CBUS input)
18	FDIV	input for the divided TV tuner oscillator frequency
3	CLI	oscillator/clock input
2	CLO	quartz crystal oscillator output
16	FUP	tuning voltage control output for tuner frequency up (+)
15	FDN	tuning voltage control output for tuner frequency down (−)
14	AFCON	automatic frequency control output for indicator
17	TEST	test pin; held LOW for the circuit to operate
4	AN0	6 analogue outputs
5	AN1	
6	AN2	
7	AN3	
8	AN4	
9	AN5	

GENERAL DESCRIPTION

The SAB3034 performs frequency-locked loop digital tuning and also provides a digital-to-analogue converter for control of six analogue functions (e.g. volume control, bass/treble control etc.).
The 17 12-bit words are loaded into the data latch, if valid (12-bit data word, startbit = 0), via the CBUS interface. Six words out of the 17 define the tuning window, the a.f.c. holding range, the tuning speed and the clock oscillator frequency. Eight data words control the analogue functions. Two data words are used for internal/external clock frequency control, the remaining data word is no-operation. The clock frequency of 400 kHz can be derived directly from a microcomputer (e.g. MAB8048) and this can be used instead of the quartz crystal oscillator by applying this clock to input CLI.
The 12-bit frequency and tuning counter has an accuracy of $1024\ MHz/2^{12} = 250\ kHz$, which is within the catching range of a.f.c. circuits. The required frequency (max. 1024 MHz) can be specified in increments of 1 MHz (10-bit). While, with a second data word increments of 250 kHz, 500 kHz or 750 kHz in frequency can be specified. The counter result at the end of a measuring period generates the output of a positive or negative tuning pulse, respectively FUP or FDN. The tuning pulse duration of FUP or FDN depends on the value of the measured deviation and is approximately 2,5 ms maximum. The measuring and tuning process is repeated until the counter value has reached zero, giving the required frequency.

Six data words set the required values (0 to 63) into the 6-bit analogue registers. The contents of the registers are converted into pulse-width modulated outputs with a frequency of $f_{CLI}/64$. Only an external RC filter is needed to smooth the analogue values. Two data words enable or disable all of the analogue outputs simultaneously.

DEVELOPMENT DATA

HANDLING

Inputs and outputs are protected against electrostatic charge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see "Handling MOS Devices").

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range	V_{DD}	−0,3 to + 7,5	V
Input voltage range	V_I	−0,3 to + 7,5	V
Input current	I_I	max. 0,5	mA
Output voltage range	V_O	V_{SS} to + 15	V
Power dissipation per output	P_O	max. 20	mW
Total power dissipation per package	P_{tot}	max. 600	mW
Operating ambient temperature range	T_{amb}	0 to + 70	°C
Storage temperature range	T_{stg}	−20 to + 125	°C

D.C. CHARACTERISTICS

V_{SS} = 0 V; V_{DD} = 5 V; T_{amb} = 0 to + 70 °C; unless otherwise specified

	symbol	min.	typ.	max.		conditions
Supply voltage	V_{DD}	4,5	5	5,5	V	
Supply current	I_{DD}	–	18	40	mA	
Inputs CLB, DLEN, DATA						
Input voltage HIGH	V_{IH}	2,4	–	V_{DD}	V	
Input voltage LOW	V_{IL}	–0,3	–	0,8	V	
Input leakage current	I_{IR}	–	–	20	μA	V_I = –0,3 to + 5,5 V
Input FDIV						
Input voltage HIGH	V_{IH}	2,4	–	V_{DD}	V	
Input voltage LOW	V_{IL}	–0,3	–	0,6	V	
Input leakage current	I_{IR}	–	–	20	μA	V_I = –0,3 to + 5,5 V
Input TEST						
Should be connected to ground						
Outputs AN0 to AN5, FUP, FDN, AFCON (open drain)						
Output voltage HIGH	V_{OH}	–	–	12	V	
Output voltage LOW	V_{OL}	–	–	0,4	V	I_{OL} = 1 mA
Output current LOW	I_{OL}	–	1	10	mA	Limited by external resistor
Output leakage current	I_{OR}	–	–	10	μA	V_{OH} = 5,5 V
Clock oscillator input CLI						
Input voltage HIGH	V_{IH}	3	–	–	V	
Input voltage LOW	V_{IL}	–	–	0,8	V	
Clock oscillator output CLO						
Output voltage HIGH	V_{OH}	–	–	V_{DD}	V	
Output voltage LOW	V_{OL}	–	–	0,5	V	
Output current LOW	I_{OL}	–	–	0,1	mA	

DEVELOPMENT DATA

A.C. CHARACTERISTICS

V_{SS} = 0 V; V_{DD} = 5 V; T_{amb} = 0 to + 70 °C; unless otherwise specified

	symbol	min.	typ.	max.		conditions
Inputs DATA, DLEN, CLB						
Rise and fall times	t_r, t_f	–	–	1	µs	
Data set-up time DATA ⟶ CLB	t_{SUDA}	500	–	–	ns	
Data hold time DATA ⟶ CLB	t_{HDDA}	150	–	–	ns	
Enable set-up time DLEN ⟶ CLB	t_{SUEN}	500	–	–	ns	
Disable set-up time CLB ⟶ DLEN	t_{SUDI}	300	–	–	ns	
Set-up time DLEN ⟶ CLB (load pulse)	t_{SULD}	400	–	–	ns	
Input CLB						see Fig. 3
CLB frequency	f_{CLB}	0	–	66	kHz	
400 kHz synchronization f_o from microcomputer at CLI						
Duty factor	δ	0,5	–	0,8		
CLB pulse width HIGH (90%)	t_{WH}	$\frac{3}{f_o}$	–	–	s	
CLB pulse width LOW (10%)	t_{WL}	$\frac{1}{f_o}$	–	–	s	
Quartz crystal oscillator at pins CLI and CLO						
CLB pulse width HIGH (90%)	t_{WH}	$\frac{30}{f_{osc}}$	–	–	s	
CLB pulse width LOW (10%)	t_{WL}	$\frac{10}{f_{osc}}$	–	–	s	
Input FDIV						
Rise and fall times	t_r, t_f	–	–	65	ns	
Pulse width HIGH and LOW	t_{WH}, t_{WL}	60	–	–	ns	
Input CLI (400 kHz input)						
Rise and fall times	t_r, t_f	–	–	1	µs	
Pulse width HIGH	t_{WH}	0,4	–	5	µs	
Pulse width LOW	t_{WL}	1,7	–	5	µs	
Quartz crystal frequency	f_{osc}	1	–	4	MHz	
Switch-on reset						
Supply voltage transition rate	dV_{DD}/dt	–	0,02	4	V/ms	

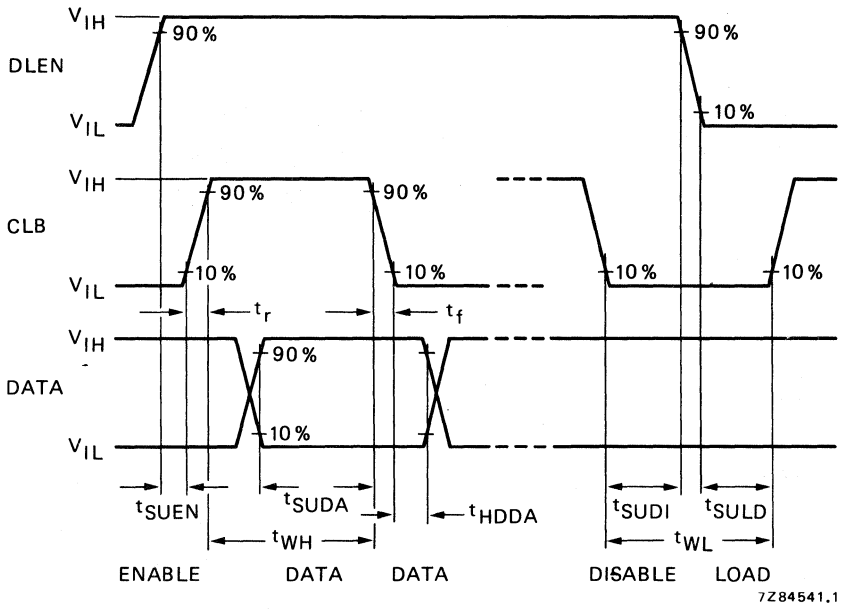


Fig. 3 CBUS timing.

OPERATION DESCRIPTION

1. Command data handling

The command data words are entered via a serial CBUS interface. Either a continuously running clock or a clock burst of 14 clock periods can be used to transmit a 12-bit data word.
Serial data, which is applied at input DATA, is shifted into the CBUS latch, with the trailing edge of the clock CLB if input DLEN is HIGH.
Each transmission is checked for word length (number of clock pulses during DLEN is HIGH) and the start-bit (first bit after start of transmission, see Fig. 5).
The valid data flag is only set if:
1. Start-bit is LOW during the first clock pulse at CLB.
2. Word length is correct; one start-bit and 11 data bits.

Loading the information into the selected latch register is done by the load pulse (first clock pulse after the HIGH-to-LOW transition of DLEN). The loading takes two pulses of the main clock and resets the valid data flag. The loading occurs only once, further CLB pulses have no effect. Only after the valid data flag is reset, will new data be accepted.

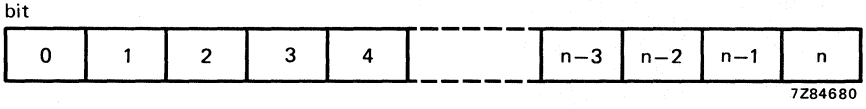


Fig. 4 Data word organization.

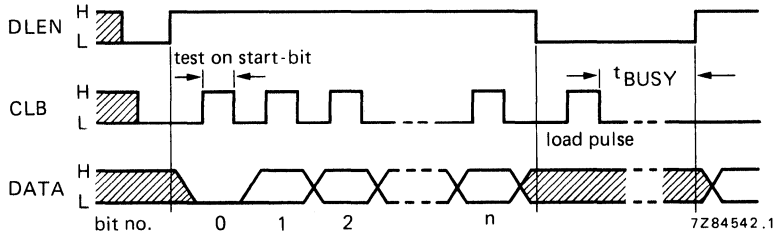


Fig. 5 CBUS data transmission.

Definitions to Figs 4 and 5:

- Word length: number of clock pulses during DLEN is active (HIGH); n + 1 bits.
- Start-bit (e.g. leading zero): bit number 0.
- Data bits: bit numbers 1 to n.
- Load pulse: first clock pulse after DLEN returns to inactive (LOW).

DEVELOPMENT DATA

1.1 Load of data

To initialize the SAB3034 after power on, either data word 1 or data word 2 must be applied first (e.g. programming of the clock oscillator mode, see Table 1). There are three different types of command data (see Table 1).

a. The first seven data words (B1 = HIGH) carry information for initialization of the operation mode, and specification of the frequency offset, tuning window, a.f.c. holding range and tuning speed (see Table 2).

b. Eight further data words (commands 9 to 16) change the contents of the analogue registers (B0 and B1 = LOW). In commands 9 to 14, bits B2, B3 and B4 form the addresses and bits B5 to B10 the 6-bit analogue values of the analogue registers. Each can be set by a binary value between 0 and 63. Enable and disable control over the six analogue outputs is achieved with data word command 15 and 16. All analogue outputs are set to logic '0' with the switch-on reset. The contents of all analogue registers are set to '0' after receiving command 1 or 2 (initialization) and the outputs are enabled.

c. The last data word (command 17) loads the 10-bit frequency data into the frequency buffer (B0 = HIGH). This 10-bit data is the binary equivalent of the required frequency in MHz. The frequency can be altered with this data word in increments of 1 MHz. If smaller steps are needed, the frequency offset can be changed in minimum steps of 250 kHz with command 3. The tuning steps are 500 kHz after the circuit is initialized by switch-on and the a.f.c. holding range is 750 kHz.

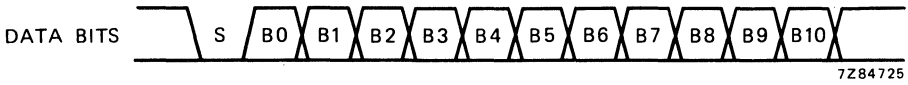


Fig. 6 Data bit organization; see also Tables 1 and 2.

Table 1. 12-bit command data words (1 to 17)

command/address	data bits B10	B9	B8	B7	B6	B5	address bits B4	B3	B2	B1	B0	start-bit S
Initialization/400 kHz clock	X	X	← DATA →				0	0	0	1	0	0
Initialization/4 MHz clock	X	X					0	0	1	1	0	0
Command according to Table 2	X	X					0	1	0	1	0	0
Tuning window Δf_t = 250 kHz	X	X	X	X	X	X	0	1	1	1	0	0
Tuning window Δf_t = 500 kHz	X	X	X	X	X	X	1	0	0	1	0	0
A.F.C. holding range Δf_a = 500 kHz	X	X	X	X	X	X	1	0	1	1	0	0
A.F.C. holding range Δf_a = 750 kHz	X	X	X	X	X	X	1	1	0	1	0	0
No operation	X	X	X	X	X	X	1	1	1	1	0	0
Analogue register 0	← DATA →						0	0	0	0	0	0
Analogue register 1							0	0	1	0	0	0
Analogue register 2							0	1	0	0	0	0
Analogue register 3							0	1	1	0	0	0
Analogue register 4							1	0	0	0	0	0
Analogue register 5							1	0	1	0	0	0
Analogue outputs enabled	X	X	X	X	X	X	1	1	0	0	0	0
Analogue outputs disabled	X	X	X	X	X	X	1	1	1	0	0	0
Data transmission of 10-bit required frequency	← DATA →										1	0

Table 2. Frequency offset and tuning speed.

frequency offset	tuning speed	B8	B7	B6	B5
0 MHz		X	X	0	0
+ 250 kHz		X	X	0	1
+ 500 kHz		X	X	1	0
+ 750 kHz		X	X	1	1
	2,5 µs/250 kHz	0	0	X	X
	5 µs/250 kHz	0	1	X	X
	10 µs/250 kHz	1	0	X	X
	20 µs/250 kHz	1	1	X	X

Note: X = state is immaterial.

2. Analogue output value (see Fig. 7)

The six analogue registers can be loaded with any binary number between 0 and 63. After the internal D to A conversion, the stored contents of each register is presented at the corresponding output by a pulse-width modulated signal. The repetition time of this output signal is $64/f_{CLI}$ (64 clock periods). External RC filters smooth the analogue outputs to obtain the d.c. control voltage levels. The commands 'analogue outputs enabled' and 'analogue outputs disabled' will simultaneously enable/disable respectively, all outputs.

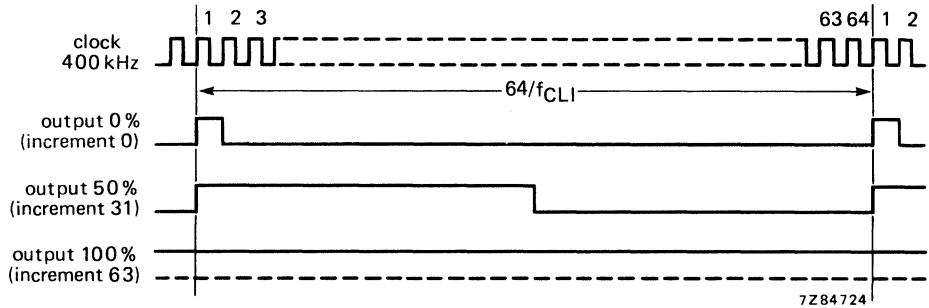


Fig. 7 Pulse-width modulated analogue outputs from SAB3034.

3. Basic tuning principle

Tuning to a transmitted frequency is controlled in the closed loop system as shown in Fig. 9. The method used is the frequency lock loop system (FLL). The tuner oscillator frequency is applied to FDIV via the divide-by-256 prescaler SAB1018. This incoming frequency $f_{osc}/256$ is once again divided by a factor N3 of the on-chip programmable prescaler, in a defined time t_m (see Fig. 8), and is then applied to the tuning counter. The tuning pulses are then compared with the required frequency. If the counter result is within the specified range (tuning window), output AFCON becomes HIGH and the a.f.c. is switched on, which enables the i.f. part to complete tuning.
At the same time, the allowed deviation in frequency is extended to the value of the a.f.c. holding range.
When the measured frequency is outside the specified limits, output AFCON will stay LOW.
Defined by the test results, frequency too high or too low, a tuning pulse is generated at respectively output FDN or FUP until the tuner is accurately tuned. The pulse duration of the FUP and FDN pulses is proportional to the measured frequency deviation and has a maximum duration of 2,5475 ms.
At the end of the tuning period the frequency counter is loaded again, just before the next frequency measurement starts.

DEVELOPMENT DATA

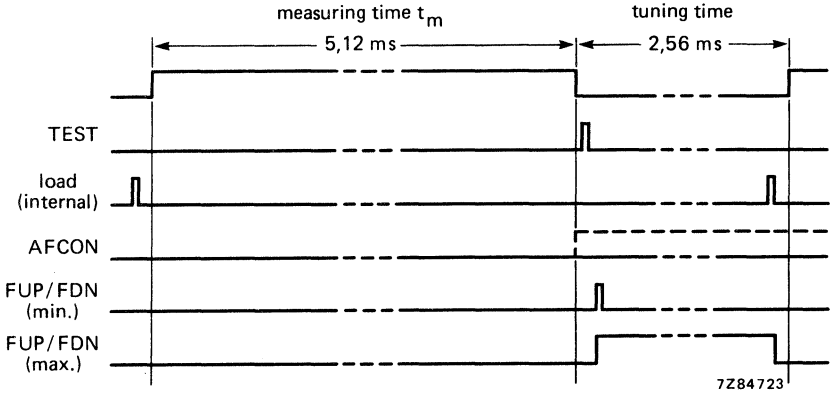


Fig. 8 Timing diagram showing the frequency measurement process.

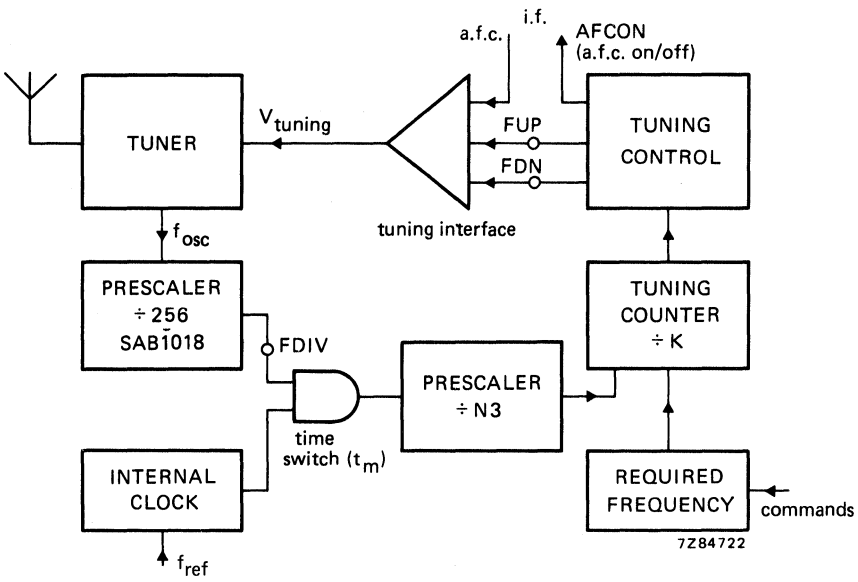


Fig. 9 The frequency lock loop system (FLL).

4. Frequency measurement

For the FLL system the following is valid:

$$f_{osc} = \frac{256 \cdot N3}{N2} \cdot f_{ref} \cdot K$$

where: f_{ref} = 400 kHz (from internal clock)
N3 = dividing factor of the internal prescaler
K = programmable factor
N2 = see below

The tuning accuracy is defined by:

$\Delta f_i = \frac{256 \cdot N3}{N2} \cdot f_{ref}$ and this is, based on the 12-bit length of the frequency counter and the maximum frequency to be measured of 1 GHz,

$\Delta f_i = \frac{1\ GHz}{2^{12}} = 250$ kHz, which is within the catching range of the a.f.c. circuit.

For practical reasons the factor 5 is chosen for N3. With f_{ref} = 400 kHz, N2 can be calculated:

$$N2 = \frac{256 \cdot N3}{250\ kHz} \cdot 400\ kHz = 2048$$

The frequency measuring time t_m is:

$$t_m = \frac{N2}{f_{ref}} = 2048 \cdot 2{,}5\ \mu s = 5{,}12\ ms$$

In the following time period of 2,56 ms, correction pulses can be generated (FUP/FDN) of which the width is proportional to the error in frequency.
The minimum width is defined as 2,5 μs for each 250 kHz deviation in frequency.
The factor of 5 for N3 implies a possible frequency error f_{er} in the measurement of:

$$f_{er} = \frac{\Delta f_i}{N3} = \frac{250}{5} = 50\ kHz$$

5. The tuning window (Δf_t)

When a tuning procedure is started, the oscillator frequency (f_{osc}) of the tuner is corrected until the measured deviation is within the tuning window Δf_t.
Width and position of Δf_t is calculated below.
The frequency applied to the i.f.-part of the TV receiver for correct tuning must be:

$f_{if} = f_{osc} - f_{Vn}$ where: f_{Vn} is the vision frequency of channel n.

At the moment the a.f.c. is switched on, the frequency to the i.f. part could be:

$f_{if} = f_{osc} \pm \Delta f_t \pm f_{er} - f_{Vn}$ (in MHz)

With the required value $f_{if} = 38{,}9$ MHz, the maximum $f_{if}(+)$ is:

$f_{if}(+) = (38{,}9 + \Delta f_t + 0{,}05)$ MHz

Given is $f_{if}(+) < 40{,}4$ MHz (the trap frequency), so $\Delta f_t + 50$ kHz = 1,5 MHz.
A practical value for $\Delta f_t(+)$: < 500 kHz.

The minimum allowed intermediate frequency $f_{if}(-)$ is defined by the sound carrier of the adjacent channel $f_{S(n-1)}$. In v.h.f.-bands with 7 MHz channel spacing applies:

$f_{S(n-1)} = (f_{Vn} - 1{,}5)$ MHz.

This results in $f_{if}(-) = f_{osc} - \Delta f_t - f_{er} - f_{V(n-1)} + 1{,}5$ MHz =

$= 40{,}4 - (\Delta f_t - 0{,}05)$

Required is $f_{if}(-) = 40{,}4$ MHz, when $\Delta f_t = 0$.

The calculations show, that the tuning window Δf_t must be positive only (see Fig. 10).

6. A.F.C. holding window (Δf_a)

When the measured frequency is specified within the tuning window Δf_t, the a.f.c. is switched on (AFCON = HIGH). The accuracy of the measurement is now set to a wider area, the a.f.c. holding window Δf_a, operational either positive or negative.
The width of Δf_a is defined by the following:

- The margin in frequency at the lower band ends of the tuners limits: $-\Delta f_a \leqslant 1$ MHz.
- Searching to unallocated frequencies with 1 MHz increments defines: $+\Delta f_a < 1$ MHz.
- To cover the complete frequency band $\pm \Delta f_a$ must have an overlap or $\pm \Delta f_a$ must be larger than the smallest frequency increment.

The SAB3034 has two different tuning windows and two a.f.c. holding windows, and are independently controllable.

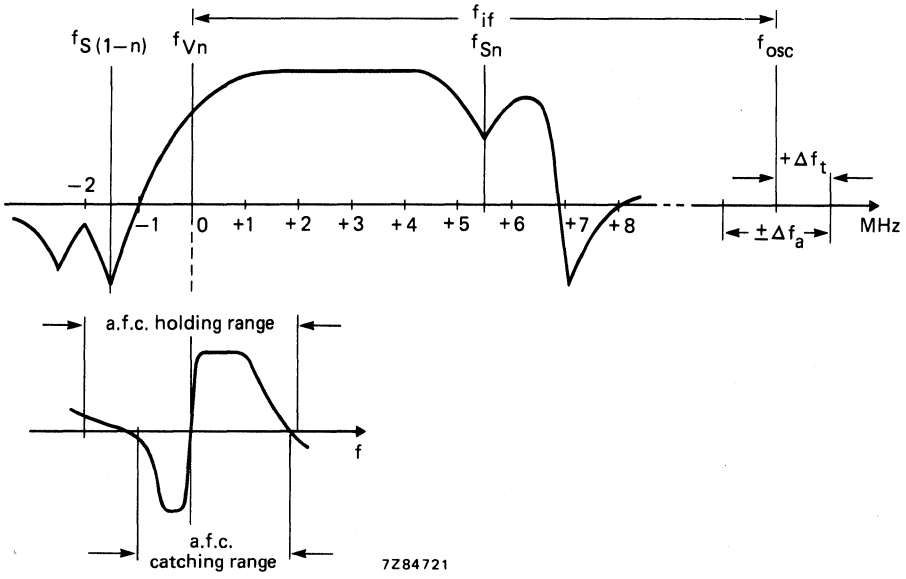


Fig. 10 Tuning example.

7. Programmable factor K

The oscillator frequency of the tuner $f_{osc} = \frac{N1 \cdot N3}{N2} \cdot f_{ref} \cdot K$.

The programmable factor is calculated from $f_{osc} = f_{Vn} + f_{if}$. For standard frequencies, CCIR norm B and G:

$f_{osc} = X, 25 + 38,9 = (X + 39), 15$ MHz where $X + 39 = K$.

The remainder of 150 kHz needs an additional offset in the frequency measurement of 150 kHz. This is done by presetting the on-chip prescaler. An example of frequency measurement is shown in Table 3, where for simplicity a measurement of 1,15 MHz is illustrated, with $a + \Delta f_t = 250$ kHz and $a^{+}/-\Delta f_a = 750$ kHz.

Table 3. Example of frequency measurement at f = 1,15 MHz

prescaler N3 = 5	frequency counter contents		
1 1 1 0 1 1 1 0 1	0 0 1 0 0 0 0 0 0 0 0 0 0	← frequency loading	150 kHz correction
0 0 1 1 1 0 0 1 0 1 0 0 0 0 0			
0 0 1 1 1 0 0 1 0 1 0 0 0 0 0	1 1 0 0 0 0 0 0 0 0 0 0 0		
0 0 1 1 1 0 0 1 0 1 0 0 0 0 0	0 1 0 0 0 0 0 0 0 0 0 0 0		
0 0 1 1 1 0 0 1 0 1 0 0 0 0 0	1 0 0 0 0 0 0 0 0 0 0 0 0	$0 < + \Delta f_t < 250$ kHz	$\Delta f_a = \pm 750$ kHz
0 0 1 1 1 0 0 1 0 1 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0		
0 0 1 1 1 0 0 1 0 1 0 0 0 0 0	1 1 1 1 1 1 1 1 1 1 1 1 1		
0 0 1 1 1 0 0 1 0 1 0 0 0 0 0	0 1 1 1 1 1 1 1 1 1 1 1 1		
0 0 1 1 1 0 0 1 0 1 0 0 0 0 0	1 0 1 1 1 1 1 1 1 1 1 1 1		
0 0 1 1 1 0 0 1 0 1 0 0 0 0 0	0 0 1 1 1 1 1 1 1 1 1 1 1		
0 0 1	1 1 0 1 1 1 1 1 1 1 1 1 1		

DEVELOPMENT DATA

8. Tuning speed

Basically the SAB3034 generates a pulse at one of the correction outputs with a width of 2,5 μs for each 250 kHz detected deviation in frequency. However, the steepness of tuner characteristics are different. To realize a more equable tuning time through the frequency bands, the correction pulse width is made programmable. A choice can be made between 2,5 μs, 5 μs, 10 μs or 20 μs for each 250 kHz deviation (see Table 2).

9. Power-on reset

The on-chip power-on reset circuits ($dV_{DD}/dt < 4$ V/ms) set the IC in the following defined states:
- analogue outputs (AN0 to AN5) = LOW,
- outputs FDN and AFCON = LOW,
- output FUP = HIGH,
- reset the CBUS latch,
- set the clock logic for f_{ref} = 400 kHz.

The IC is activated by data word 1 or 2 (see also Table 1); so the first message must be one of these and the logic will be initialized, including:
- analogue latches contents set to zero,
- enabling of all outputs,
- set Δf_t = 0,5 MHz and Δf_a = 0,75 MHz,
- load frequency offset and tuning speed control bits.
- clears all other logic.

Note

For correct power-on reset, the pull-up voltage used for the open drain outputs must have some delay in the rise time in respect to the V_{DD} = + 5 V rise time.

COMPUTER INTERFACE FOR TUNING AND CONTROL (CITAC)

GENERAL DESCRIPTION

The SAB3035 provides closed-loop digital tuning of TV receivers, with or without a.f.c., as required. It also controls up to 8 analogue functions, 4 general purpose I/O ports and 4 high-current outputs for tuner band selection.

The IC is used in conjunction with a microcomputer from the MAB8400 family and is controlled via a two-wire, bidirectional I^2C bus.

Features

- Combined analogue and digital circuitry minimizes the number of additional interfacing components required
- Frequency measurement with resolution of 50 kHz
- Selectable prescaler divisor of 64 or 256
- 32 V tuning voltage amplifier
- 4 high-current outputs for direct band selection
- 8 static digital to analogue converters (DACs) for control of analogue functions
- Four general purpose input/output (I/O) ports
- Tuning with control of speed and direction
- Tuning with or without a.f.c.
- Single-pin, 4 MHz on-chip oscillator
- I^2C bus slave transceiver

QUICK REFERENCE DATA

Supply voltages			
(pin 16)	V_{P1}	typ.	12 V
(pin 22)	V_{P2}	typ.	13 V
(pin 17)	V_{P3}	typ.	32 V
Supply currents (no outputs loaded)			
(pin 16)	I_{P1}	typ.	32 mA
(pin 22)	I_{P2}	typ.	0,1 mA
(pin 17)	I_{P3}	typ.	0,6 mA
Total power dissipation	P_{tot}	typ.	400 mW
Operating ambient temperature range	T_{amb}	−20 to +70	°C

PACKAGE OUTLINE

28-lead DIL; plastic (SOT-117).

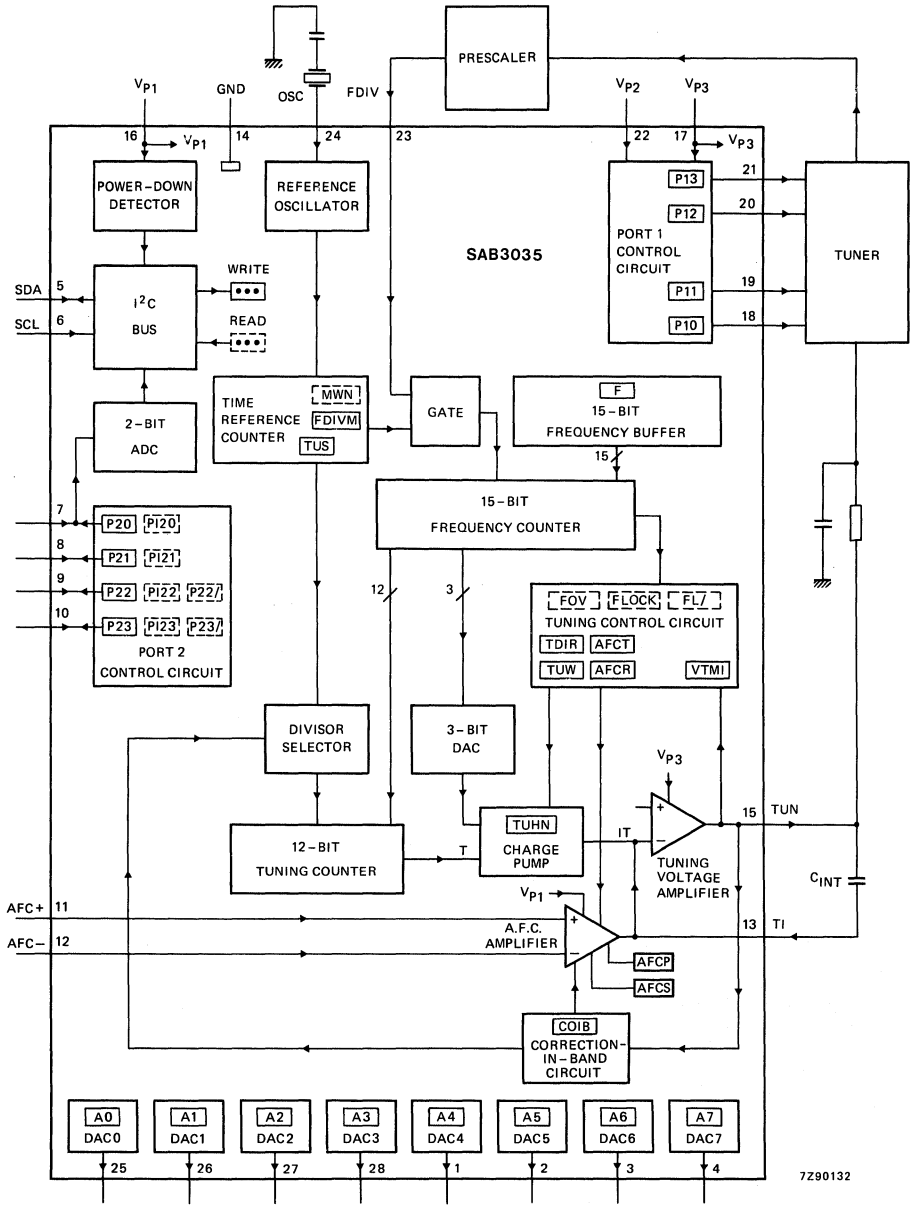


Fig. 1 Block diagram.

DEVELOPMENT DATA

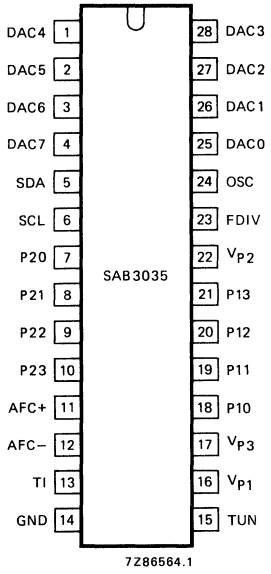


Fig. 2 Pinning diagram.

PINNING

1	DAC4	outputs of static DACs
2	DAC5	
3	DAC6	
4	DAC7	
5	SDA	serial data line (I²C bus)
6	SCL	serial clock line (I²C bus)
7	P20	general purpose input/output ports
8	P21	
9	P22	
10	P23	
11	AFC+	a.f.c. inputs
12	AFC–	
13	TI	tuning voltage amplifier inverting input
14	GND	ground
15	TUN	tuning voltage amplifier output
16	V_{P1}	+12 V supply voltage
17	V_{P3}	+32 V supply for tuning voltage amplifier
18	P10	High-current band-selection output ports
19	P11	
20	P12	
21	P13	
22	V_{P2}	positive supply for high-current band-selection output circuits
23	FDIV	input from prescaler
24	OSC	crystal oscillator input
25	DAC0	outputs of static DACs
26	DAC1	
27	DAC2	
28	DAC3	

FUNCTIONAL DESCRIPTION

The SAB3035 is a monolithic computer interface which provides tuning and control functions and operates in conjunction with a microcomputer via an I^2C bus.

Tuning

This is performed using frequency-locked loop digital control. Data corresponding to the required tuner frequency is stored in a 15-bit frequency buffer. The actual tuner frequency, divided by a factor of 256 (or by 64) by a prescaler, is applied via a gate to a 15-bit frequency counter. This input (FDIV) is measured over a period controlled by a time reference counter and is compared with the contents of the frequency buffer. The result of the comparison is used to control the tuning voltage so that the tuner frequency equals the contents of the frequency buffer multiplied by 50 kHz within a programmable tuning window (TUW).

The system cycles over a period of 6,4 ms (or 2,56 ms), controlled by the time reference counter which is clocked by an on-chip 4 MHz reference oscillator. Regulation of the tuning voltage is performed by a charge pump frequency-locked loop system. The charge IT flowing into the tuning voltage amplifier is controlled by the tuning counter, 3-bit DAC and the charge pump circuit. The charge IT is linear with the frequency deviation Δf in steps of 50 kHz. For loop gain control, the relationship $\Delta IT/\Delta f$ is programmable. In the normal mode (when control bits TUHN0 and TUHN1 are both at logic 1, see OPERATION), the minimum charge IT at Δf = 50 kHz equals 250 $\mu A\ \mu s$ (typical).

By programming the tuning sensitivity bits (TUS), the charge IT can be doubled up to 6 times. If correction-in-band (COIB) is programmed, the charge can be further doubled up to three times in relation to the tuning voltage level. From this, the maximum charge IT at Δf = 50 kHz equals $2^6 \times 2^3 \times 250\ \mu A\ \mu s$ (typical).

The maximum tuning current I is 875 μA (typical). In the tuning-hold (TUHN) mode (TUHN is active LOW), the tuning current I is reduced and as a consequence the charge into the tuning amplifier is also reduced.

An in-lock situation can be detected by reading FLOCK. When the tuner oscillator frequency is within the programmable tuning window (TUW), FLOCK is set to logic 1. If the frequency is also within the programmable a.f.c. hold range (AFCR), which always occurs if AFCR is wider than TUW, control bit AFCT can be set to logic 1. When set, digital tuning will be switched off, a.f.c. will be switched on and FLOCK will stay at logic 1 as long as the oscillator frequency is within AFCR. If the frequency of the tuning oscillator does not remain within AFCR, AFCT is cleared automatically and the system reverts to digital tuning. To be able to detect this situation, the occurrence of positive and negative transitions in the FLOCK signal can be read (FL/1N and FL/0N). AFCT can also be cleared by programming the AFCT bit to logic 0.

The a.f.c. has programmable polarity and transconductance; the latter can be doubled up to 3 times, depending on the tuning voltage level if correction-in-band is used.

The direction of tuning is programmable by using control bits TDIRD (tuning direction down) and TDIRU (tuning direction up). If a tuner enters a region in which oscillation stops, then, providing the prescaler remains stable, no FDIV signal is supplied to CITAC. In this situation the system will tune up, moving away from frequency lock-in. This situation is avoided by setting TDIRD which causes the system to tune down. In normal operation TDIRD must be cleared.

If a tuner stops oscillating and the prescaler becomes unstable by going into self-oscillation at a very high frequency, the system will react by tuning down, moving away from frequency lock-in. To overcome this, the system can be forced to tune up at the lowest sensitivity (TUS) value, by setting TDIRU.

Setting both TDIRD and TDIRU causes the digital tuning to be interrupted and a.f.c. to be switched on.

The minimum tuning voltage which can be generated during digital tuning is programmable by VTMI to prevent the tuner being driven into an unspecified low tuning voltage region.

Control

For tuner band selection there are four outputs P10 to P13 which are capable of sourcing up to 50 mA at a voltage drop of less than 600 mV with respect to the separate power supply input V_{P2}.

For additional digital control, four open collector I/O ports P20 to P23 are provided. Ports P22 and P23 are capable of detecting positive and negative transitions in their input signals. With the aid of port P20, up to three independent module addresses can be programmed.

Eight 6-bit digital-to-analogue converters DAC0 to DAC7 are provided for analogue control.

Reset

CITAC goes into the power-down-reset mode when V_{P1} is below 8,5 V (typical). In this mode all registers are set to a defined state. Reset can also be programmed.

OPERATION

Write

CITAC is controlled via a bidirectional two-wire I^2C bus; the I^2C bus is specified in our data handbook "ICs for digital systems in radio, audio, and video equipment". For programming, a module address, R/$\overline{W}$ bit (logic 0), an instruction byte and a data/control byte are written into CITAC in the format shown in Fig. 3.

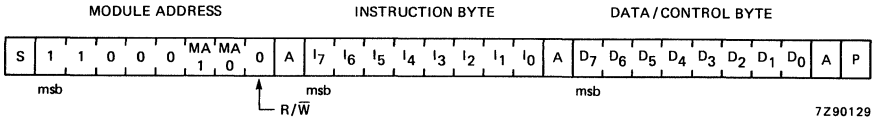


Fig. 3 I^2C bus write format.

The module address bits MA1, MA0 are used to give a 2-bit module address as a function of the voltage at port P20 as shown in Table 1.

Acknowledge (A) is generated by CITAC only when a valid address is received and the device is not in the power-down-reset mode ($V_{P1} > 8,5$ V (typical)).

Table 1 Valid module addresses

MA1	MA0	P20
0	0	don't care
0	1	GND
1	0	$\frac{1}{2}V_{P1}$
1	1	V_{P1}

OPERATION (continued)

Tuning

Tuning is controlled by the instruction and data/control bytes as shown in Fig. 4.

	INSTRUCTION BYTE								DATA/CONTROL BYTE							
	I_7	I_6	I_5	I_4	I_3	I_2	I_1	I_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
freq.	1	F14	F13	F12	F11	F10	F9	F8	F7	F6	F5	F4	F3	F2	F1	F0
TCD0	0	0	1	0	1	0	0	1	AFCT	VTMI0	AFCR1	AFCR0	TUHN1	TUHN0	TUW1	TUW0
TCD1	0	0	1	0	1	0	1	0	VTMI1	COIB1	COIB0	AFCS1	AFCS0	TUS2	TUS1	TUS0
TCD2	0	0	1	0	1	0	1	1	0	0	0	0	AFCP	FDIVM	TDIRD	TDIRU

7Z90125

Fig. 4 Tuning control format.

Frequency

Frequency is set when bit I_7 of the instruction byte is set to logic 1; the remainder of this byte together with the data/control byte are loaded into the frequency buffer. The frequency to which the tuner oscillator is regulated equals the decimal representation of the 15-bit word multiplied by 50 kHz. All frequency bits are set to logic 1 at reset.

Tuning hold

The TUHN bits are used to decrease the maximum tuning current and, as a consequence, the minimum charge IT (at Δf = 50 kHz) into the tuning amplifier.

Table 2 Tuning current control

TUHN1	TUHN0	typ. I_{max} μA	typ. IT_{min} $\mu A\ \mu s$	typ. ΔV_{TUNmin} at C_{INT} = 1 μF μV
0	0	3,5*	1*	1*
0	1	29	8	8
1	0	110	30	30
1	1	875	250	250

* Values after reset.

During tuning but before lock-in, the highest current value should be selected.
After lock-in the current may be reduced to decrease the tuning voltage ripple.

The lowest current value should not be used for tuning due to the input bias current of the tuning voltage amplifier (max. 5 nA). However it is good practice to program the lowest current value during tuner band switching.

Tuning sensitivity

To be able to program an optimum loop gain, the charge IT can be programmed by changing T using tuning sensitivity (TUS). Table 3 shows the minimum charge IT obtained by programming the TUS bits at Δf = 50 kHz; TUHN0 and TUHN1 = logic 1.

Table 3 Minimum charge IT as a function of TUS

Δf = 50 kHz; TUHN0 = logic 1; TUHN1 = logic 1

TUS2	TUS1	TUS0	typ. IT_{min} mA μs	typ. ΔV_{TUNmin} at C_{INT} = 1 μF mV
0	0	0	0,25*	0,25*
0	0	1	0,5	0,5
0	1	0	1	1
0	1	1	2	2
1	0	0	4	4
1	0	1	8	8
1	1	0	16	16

* Values after reset.

Correction-in-band

This control is used to correct the loop gain of the tuning system to reduce in-band variations due to a non-linear voltage/frequency characteristic of the tuner. Correction-in-band (COIB) controls the time T of the charge equation IT and takes into account the tuning voltage V_{TUN} to give charge multiplying factors as shown in Table 4.

DEVELOPMENT DATA

Table 4 Programming correction-in-band

COIB1	COIB0	charge multiplying factors at typical values of V_{TUN} at:			
		< 12 V	12 to 18 V	18 to 24 V	> 24 V
0	0	1*	1*	1*	1*
0	1	1	1	1	2
1	0	1	1	2	4
1	1	1	2	4	8

* Values after reset.

The transconductance multiplying factor of the a.f.c. amplifier is similar when COIB is used, except for the lowest transconductance which is not affected.

Tuning window

Digital tuning is interrupted and FLOCK is set to logic 1 (in-lock) when the absolute deviation $|\Delta f|$ between the tuner oscillator frequency and the programmed frequency is smaller than the programmed TUW value (see Table 5). If $|\Delta f|$ is up to 50 kHz above the values listed in Table 5, it is possible for the system to be locked depending on the phase relationship between FDIV and the reference counter.

Table 5 Tuning window programming

TUW1	TUW0	$\|\Delta f\|$ (kHz)	tuning window (kHz)
0	0	0*	0*
0	1	50	100
1	0	150	300

* Values after reset.

OPERATION (continued)

A.F.C.

When AFCT is set to logic 1 it will not be cleared and the a.f.c. will remain on as long as $|\Delta f|$ is less than the value programmed for the a.f.c. hold range AFCR (see Table 6). It is possible for the a.f.c. to remain on for values of up to 50 kHz more than the programmed value depending on the phase relationship between FDIV and the reference counter.

Table 6 A.F.C. hold range programming

AFCR1	AFCR0	$\|\Delta f\|$ (kHz)	a.f.c. hold range (kHz)
0	0	0*	0*
0	1	350	700
1	0	750	1500

* Values after reset.

Transconductance

The transconductance (g) of the a.f.c. amplifier is programmed via the a.f.c. sensitivity bits AFCS as shown in Table 7.

Table 7 Transconductance programming

AFCS1	AFCS0	typ. transconductance (μA/V)
0	0	0,25*
0	1	25
1	0	50
1	1	100

* Value after reset.

A.F.C. polarity

If a positive differential input voltage is applied to the (switched on) a.f.c. amplifier, the tuning voltage V_{TUN} falls when the a.f.c. polarity bit AFCP is at logic 0 (value after reset). At AFCP = logic 1, V_{TUN} rises.

Minimum tuning voltage

Both minimum tuning voltage control bits, VTMI1 and VTMI0, are at logic 0 after reset. Further details are given in CHARACTERISTICS.

Frequency measuring window

The frequency measuring window which is programmed must correspond with the division factor of the prescaler in use (see Table 8).

Table 8 Frequency measuring window programming

FDIVM	prescaler division factor	cycle period (ms)	measuring window (ms)
0	256	6,4*	5,12*
1	64	2,56	1,28

* Values after reset.

Tuning direction

Both tuning direction bits, TDIRU (up) and TDIRD (down), are at logic 0 after reset.

Control

The instruction bytes POD (port output data) and DACX (digital-to-analogue converter control) are shown in Fig. 5, together with the corresponding data/control bytes. Control is implemented as follows:

P13, P12, P11, P10 — Band select outputs. If a logic 1 is programmed on any of the POD bits D_3 to D_0, the relevant output goes HIGH. All outputs are LOW after reset.

P23, P22, P21, P20 — Open collector I/O ports. If a logic 0 is programmed on any of the POD bits D_7 to D_4, the relevant output is forced LOW. All outputs are at logic 1 after reset (high impedance state).

DACX — Digital-to-analogue converters. The digital-to-analogue converter selected corresponds to the decimal equivalent of the DACX bits X2, X1, X0. The output voltage of the selected DAC is set by programming the bits AX5 to AX0; the lowest output voltage is programmed with all data AX5 to AX0 at logic 0, or after reset has been activated.

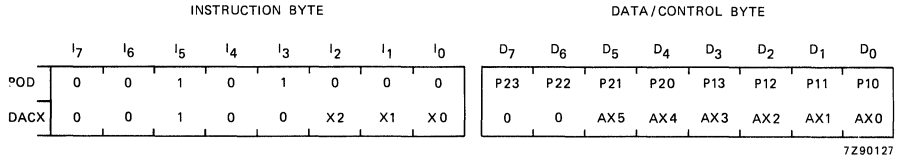


Fig. 5 Control programming.

Read

Information is read from CITAC when the R/$\overline{W}$ bit is set to logic 1. An acknowledge must be generated by the master after each data byte to allow transmission to continue. If no acknowledge is generated by the master the slave (CITAC) stops transmitting. The format of the information bytes is shown in Fig. 6.

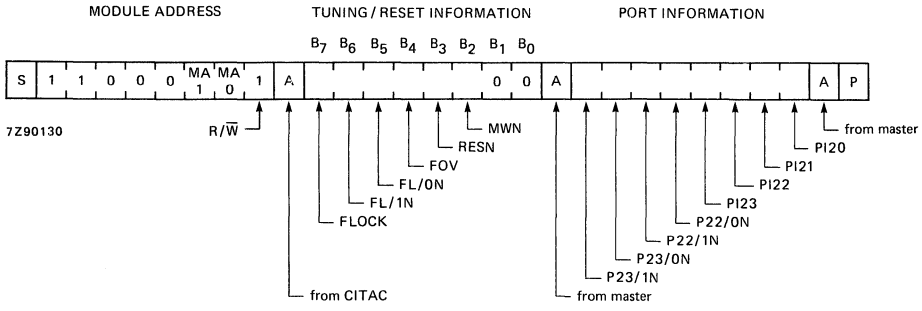


Fig. 6 Information byte format.

OPERATION (continued)

Tuning/reset information bits

FLOCK	Set to logic 1 when the tuning oscillator frequency is within the programmed tuning window.
FL/1N	Set to logic 0 (active LOW) when FLOCK changes from 0 to 1 and is reset to logic 1 automatically after tuning information has been read.
FL/0N	As for FL/1N but is set to logic 0 when FLOCK changes from 1 to 0.
FOV	Indicates frequency overflow. When the tuner oscillator frequency is too high with respect to the programmed frequency, FOV is at logic 1, and when too low, FOV is at logic 0. FOV is not valid when TDIRU and/or TDIRD are set to logic 1.
RESN	Set to logic 0 (active LOW) by a programmed reset or a power-down-reset. It is reset to logic 1 automatically after tuning/reset information has been read.
MWN	MWN (frequency measuring window, active LOW) is at logic 1 for a period of 1,28 ms, during which time the results of frequency measurement are processed. This time is independent of the cycle period. During the remaining time, MWN is at logic 0 and the received frequency is measured. When slightly different frequencies are programmed repeatedly and a.f.c. is switched on, the received frequency can be measured using FOV and FLOCK. To prevent the frequency counter and frequency buffer being loaded at the same time, frequency should be programmed only during the period of MWN = logic 0.

Port information bits

P23/1N, P22/1N	Set to logic 0 (active LOW) at a LOW-to-HIGH transition in the input voltage on P23 and P22 respectively. Both are reset to logic 1 after the port information has been read.
P23/0N, P22/0N	As for P23/1N and P22/1N but are set to logic 0 at a HIGH-to-LOW transition.
PI23, PI22, PI21, PI20	Indicate input voltage levels at P23, P22, P21 and P20 respectively. A logic 1 indicates a HIGH input level.

Reset

The programming to reset all registers is shown in Fig. 7. Reset is activated only at data byte HEX 06. Acknowledge is generated at every byte, provided that CITAC is not in the power-down-reset mode. After the general call address byte, transmission of more than one data byte is not allowed.

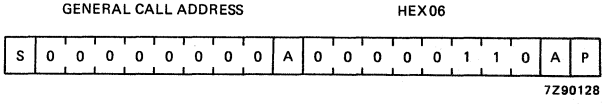


Fig. 7 Reset programming.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage ranges:			
(pin 16)	V_{P1}	−0,3 to +18	V
(pin 22)	V_{P2}	−0,3 to +18	V
(pin 17)	V_{P3}	−0,3 to +36	V
Input/output voltage ranges:			
(pin 5)	V_{SDA}	−0,3 to +18	V
(pin 6)	V_{SCL}	−0,3 to +18	V
(pins 7 to 10)	V_{P2X}	−0,3 to +18	V
(pins 11 and 12)	$V_{AFC+,AFC-}$	−0,3 to V_{P1}*	V
(pin 13)	V_{TI}	−0,3 to V_{P1}*	V
(pin 15)	V_{TUN}	−0,3 to V_{P3}*	V
(pins 18 to 21)	V_{P1X}	−0,3 to V_{P2}**	V
(pin 23)	V_{FDIV}	−0,3 to V_{P1}*	V
(pin 24)	V_{OSC}	−0,3 to +5	V
(pins 1 to 4 and 25 to 28)	V_{DACX}	−0,3 to V_{P1}*	V
Total power dissipation	P_{tot}	max. 1000	mW
Storage temperature range	T_{stg}	−55 to +125	°C
Operating ambient temperature range	T_{amb}	−20 to +70	°C

DEVELOPMENT DATA

* Pin voltage may exceed supply voltage if current is limited to 10 mA.

** Pin voltage must not exceed 18 V but may exceed V_{P2} if current is limited to 200 mA.

CHARACTERISTICS

T_{amb} = 25 °C; V_{P1}, V_{P2}, V_{P3} at typical voltages, unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply voltages	V_{P1}	10,5	12	13,5	V
	V_{P2}	4,7	13	16	V
	V_{P3}	30	32	35	V
Supply currents (no outputs loaded)	I_{P1}	20	32	50	mA
	I_{P2}	0	–	0,1	mA
	I_{P3}	0,2	0,6	2	mA
Additional supply currents (A)	I_{P2A}	–2	–	I_{OHP1X}	mA
(note 1)	I_{P3A}	0,2	–	2	mA
Total power dissipation	P_{tot}	–	400	–	mW
Operating ambient temperature	T_{amb}	–20	–	+70	°C
I²C bus inputs/outputs					
SDA input (pin 5); SCL input (pin 6)					
Input voltage HIGH (note 2)	V_{IH}	3	–	$V_{P1}-1$	V
Input voltage LOW	V_{IL}	–0,3	–	1,5	V
Input current HIGH (note 2)	I_{IH}	–	–	10	μA
Input current LOW (note 2)	I_{IL}	–	–	10	μA
SDA output (pin 5, open collector)					
Output voltage LOW at I_{OL} = 3 mA	V_{OL}	–	–	0,4	V
Maximum output sink current	I_{OL}	–	5	–	mA
Open collector I/O ports					
P20, P21, P22, P23 (pins 7 to 10, open collector)					
Input voltage HIGH	V_{IH}	2	–	16	V
Input voltage LOW	V_{IL}	–0,3	–	0,8	V
Input current HIGH	I_{IH}	–	–	25	μA
Input current LOW	$-I_{IL}$	–	–	25	μA
Output voltage LOW at I_{OL} = 2 mA	V_{OL}	–	–	0,4	V
Maximum output sink current	I_{OL}	–	4	–	mA

parameter		symbol	min.	typ.	max.	unit
A.F.C. amplifier						
Inputs AFC+, AFC– (pins 11, 12)						
Transconductance for input voltages up to 1 V differential:						
AFCS1	AFCS2					
0	0	g_{00}	100	250	800	nA/V
0	1	g_{01}	15	25	35	μA/V
1	0	g_{10}	30	50	70	μA/V
1	1	g_{11}	60	100	140	μA/V
Tolerance of transconductance multiplying factor (2, 4 or 8) when correction-in-band is used		ΔM_g	–20	–	+20	%
Input offset voltage		V_{Ioff}	–75	–	+75	mV
Common mode input voltage		V_{com}	3	–	$V_{P1}-2,5$	V
Common mode rejection ratio		CMRR	–	50	–	dB
Power supply (V_{P1}) rejection ratio		PSRR	–	50	–	dB
Input current		I_I	–	–	500	nA
Tuning voltage amplifier						
Input TI, output TUN (pins 13, 15)						
Maximum output voltage at $I_{load} = \pm 2,5$ mA		V_{TUN}	$V_{P3}-1,6$	–	$V_{P3}-0,4$	V
Minimum output voltage at $I_{load} = \pm 2,5$ mA:						
VTMI1	VTMI0					
0	0	V_{TM00}	300	–	500	mV
1	0	V_{TM10}	450	–	650	mV
1	1	V_{TM11}	650	–	900	mV
Maximum output source current		$-I_{TUNH}$	2,5	–	8	mA
Maximum output sink current		I_{TUNL}	–	40	–	mA
Input bias current		I_{TI}	–5	–	+5	nA
Power supply (V_{P3}) rejection ratio		PSRR	–	60	–	dB

DEVELOPMENT DATA

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Tuning voltage amplifier (continued)					
Minimum charge IT to tuning voltage amplifier					
TUHN1 TUHN0					
0 0	CH_{00}	0,4	1	1,7	μA μs
0 1	CH_{01}	4	8	14	μA μs
1 0	CH_{10}	15	30	48	μA μs
1 1	CH_{11}	130	250	370	μA μs
Tolerance of charge (or ΔV_{TUN}) multiplying factor when COIB and/or TUS are used	ΔCH	−20	–	+20	%
Maximum current I into tuning amplifier					
TUHN1 TUHN0					
0 0	I_{T00}	1,7	3,5	5,1	μA
0 1	I_{T01}	15	29	41	μA
1 0	I_{T10}	65	110	160	μA
1 1	I_{T11}	530	875	1220	μA
Correction-in-band					
Tolerance of correction-in-band levels 12 V, 18 V and 24 V	ΔV_{CIB}	−15	–	+15	%
Band-select output ports					
P10, P11, P12, P13 (pins 18 to 21)					
Output voltage HIGH at $-I_{OH}$ = 50 mA (note 3)	V_{OH}	V_{P2}−0,6	–	–	V
Output voltage LOW at I_{OL} = 2 mA	V_{OL}	–	–	0,4	V
Maximum output source current (note 3)	$-I_{OH}$	–	130	200	mA
Maximum output sink current	I_{OL}	–	5	–	mA
FDIV input (pin 23)					
Input voltage (peak-to-peak value) (t_{rise} and $t_{fall} \leqslant 40$ ns)	$V_{FDIV(p-p)}$	0,1	–	2	V
Duty cycle	–	40	–	60	%
→ Maximum input frequency	f_{max}	14,5	–	–	MHz
Input impedance	Z_i	–	8	–	kΩ
Input capacitance	C_i	–	5	–	pF

parameter	symbol	min.	typ.	max.	unit
OSC input (pin 24)					
Crystal resistance at resonance (4 MHz)	R_X	–	–	150	Ω
DAC outputs 0 to 7 (pins 25 to 28 and 1 to 4)					
Maximum output voltage (no load) at V_{P1} = 12 V (note 4)	V_{DH}	10	–	11,5	V
Minimum output voltage (no load) at V_{P1} = 12 V (note 4)	V_{DL}	0,1	–	1	V
Positive value of smallest step (1 least-significant bit)	ΔV_D	0	–	350	mV
Deviation from linearity	–	–	–	0,5	V
Output impedance at $I_{load} = \pm 2$ mA	Z_o	–	–	70	Ω
Maximum output source current	$-I_{DH}$	–	–	6	mA
Maximum output sink current	I_{DL}	–	8	–	mA
Power-down-reset					
Maximum supply voltage V_{P1} at which power-down-reset is active	V_{PD}	7,5	–	9,5	V
V_{P1} rise-time during power-up (up to V_{PD})	t_r	5	–	–	μs
Voltage level for valid module address					
Voltage level at P20 (pin 7) for valid module address as a function of MA1, MA0					
MA1 MA0					
0 0	V_{VA00}	−0,3	–	16	V
0 1	V_{VA01}	−0,3	–	0,8	V
1 0	V_{VA10}	2,5	–	$V_{P1}-2$	V
1 1	V_{VA11}	$V_{P1}-0,3$	–	V_{P1}	V

DEVELOPMENT DATA

Notes to the characteristics

1. For each band-select output which is programmed at logic 1, sourcing a current I_{OHP1X}, the additional supply currents (A) shown must be added to I_{P2} and I_{P3} respectively.
2. If $V_{P1} < 1$ V, the input current is limited to 10 μA at input voltages up to 16 V.
3. At continuous operation the output current should not exceed 50 mA. When the output is short-circuited to ground for several seconds the device may be damaged.
4. Values are proportional to V_{P1}.

I²C BUS TIMING (Fig. 8)

I²C bus load conditions are as follows:
4 kΩ pull-up resistor to +5 V; 200 pF capacitor to GND.

All values are referred to V_{IH} = 3 V and V_{IL} = 1,5 V.

parameter	symbol	min.	typ.	max.	unit
Bus free before start	t_{BUF}	4	–	–	μs
Start condition set-up time	$t_{SU,STA}$	4	–	–	μs
Start condition hold time	$t_{HD,STA}$	4	–	–	μs
SCL, SDA LOW period	t_{LOW}	4	–	–	μs
SCL HIGH period	t_{HIGH}	4	–	–	μs
SCL, SDA rise time	t_R	–	–	1	μs
SCL, SDA fall time	t_F	–	–	0,3	μs
Data set-up time (write)	$t_{SU,DAT}$	1	–	–	μs
Data hold time (write)	$t_{HD,DAT}$	1	–	–	μs
Acknowledge (from CITAC) set-up time	$t_{SU,CAC}$	–	–	2	μs
Acknowledge (from CITAC) hold time	$t_{HD,CAC}$	0	–	–	μs
Stop condition set-up time	$t_{SU,STO}$	4	–	–	μs
Data set-up time (read)	$t_{SU,RDA}$	–	–	2	μs
Data hold time (read)	$t_{HD,RDA}$	0	–	–	μs
Acknowledge (from master) set-up time	$t_{SU,MAC}$	1	–	–	μs
Acknowledge (from master) hold time	$t_{HD,MAC}$	2	–	–	μs

Note

Timings $t_{SU,DAT}$ and $t_{HD,DAT}$ deviate from the I²C bus specification .
After reset has been activated, transmission may only be started after a 50 μs delay.

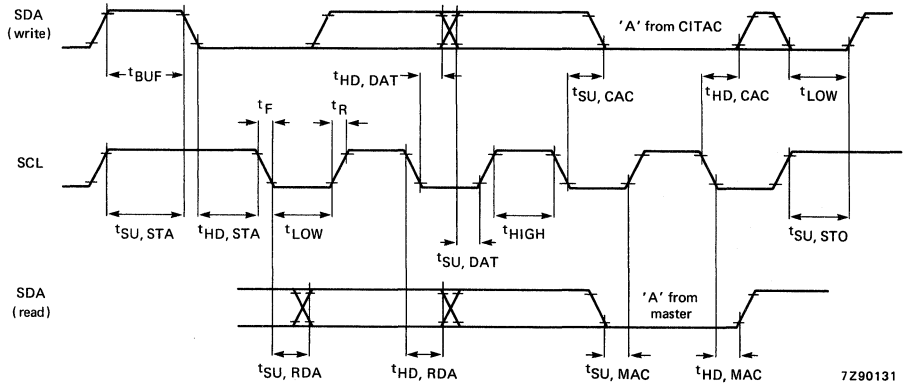


Fig. 8 I²C bus timing SAB3035.

COMPUTER INTERFACE FOR TUNING AND CONTROL (CITAC)

GENERAL DESCRIPTION

The SAB3036 provides closed-loop digital tuning of TV receivers, with or without a.f.c., as required. It also controls 4 general purpose I/O ports and 4 high-current outputs for tuner band selection.

The IC is used in conjunction with a microcomputer from the MAB8400 family and is controlled via a two-wire, bidirectional I^2C bus.

Features

- Combined analogue and digital circuitry minimizes the number of additional interfacing components required
- Frequency measurement with resolution of 50 kHz
- Selectable prescaler divisor of 64 or 256
- 32 V tuning voltage amplifier
- 4 high-current outputs for direct band selection
- Four general purpose input/output (I/O) ports
- Tuning with control of speed and direction
- Tuning with or without a.f.c.
- Single-pin, 4 MHz on-chip oscillator
- I^2C bus slave transceiver

QUICK REFERENCE DATA

Supply voltages			
(pin 5)	V_{P1}	typ.	12 V
(pin 14)	V_{P2}	typ.	13 V
(pin 9)	V_{P3}	typ.	32 V
Supply currents (no outputs loaded)			
(pin 5)	I_{P1}	typ.	23 mA
(pin 14)	I_{P2}	typ.	0,1 mA
(pin 9)	I_{P3}	typ.	0,6 mA
Total power dissipation	P_{tot}	typ.	300 mW
Operating ambient temperature range	T_{amb}		−20 to + 70 °C

PACKAGE OUTLINE

18-lead DIL; plastic (SOT-102HE).

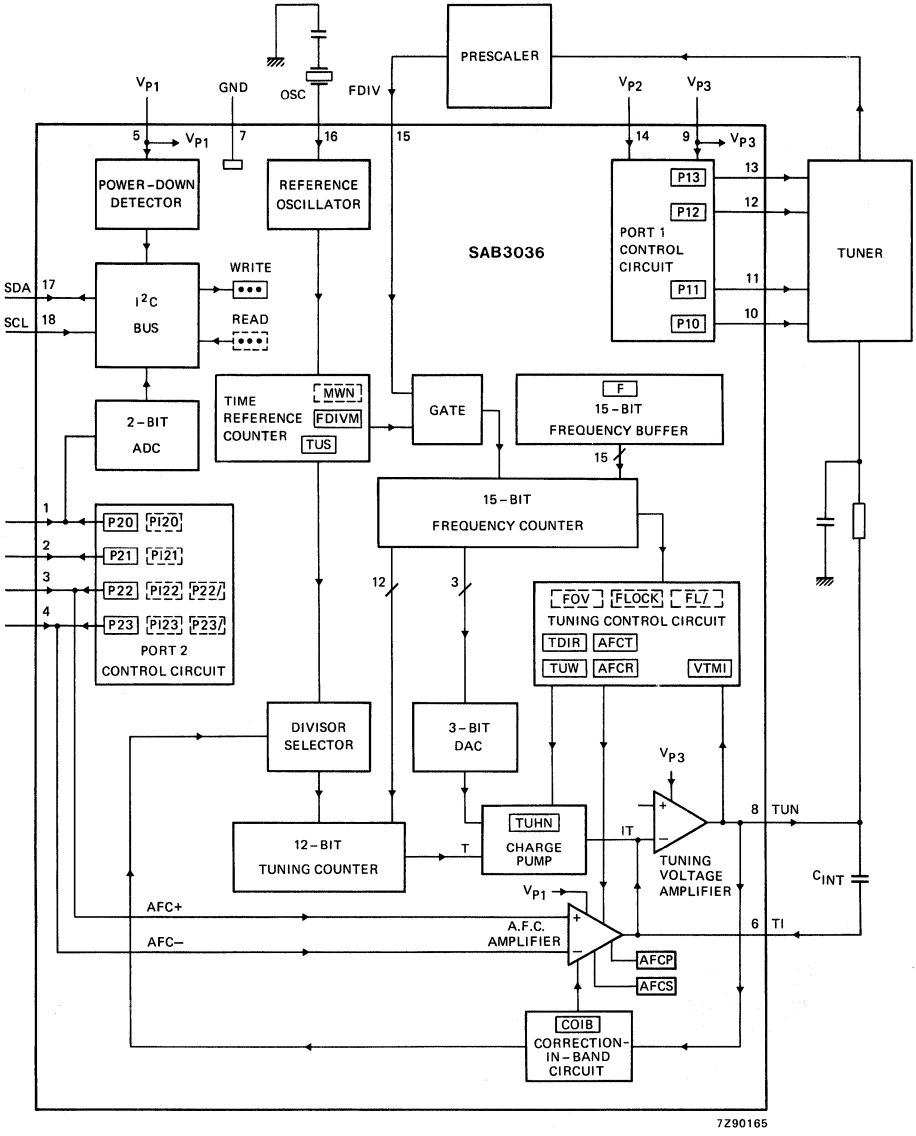


Fig. 1 Block diagram.

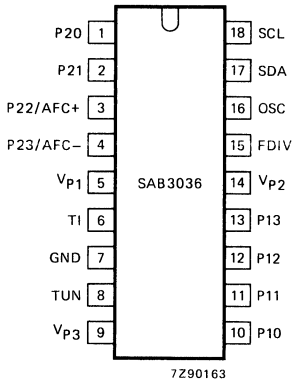


Fig. 2 Pinning diagram.

PINNING

1	P20	general purpose input/output ports
2	P21	
3	P22/AFC+	general purpose input/output ports and a.f.c. inputs
4	P23/AFC–	
5	V_{P1}	+ 12 V supply voltage
6	TI	tuning voltage amplifier inverting input
7	GND	ground
8	TUN	tuning voltage amplifier output
9	V_{P3}	+ 32 V supply for tuning voltage amplifier
10	P10	high-current band-selection output ports
11	P11	
12	P12	
13	P13	
14	V_{P2}	positive supply for high-current band-selection output circuits
15	FDIV	input from prescaler
16	OSC	crystal oscillator input
17	SDA	serial data line, I^2C bus
18	SCL	serial clock line, I^2C bus

DEVELOPMENT DATA

Purchase of Philips I^2C components conveys a licence under the Philips' I^2C patent to use the components in the I^2C system provided the system conforms to the I^2C specifications defined by Philips.

FUNCTIONAL DESCRIPTION

The SAB3036 is a monolithic computer interface which provides tuning and control functions and operates in conjunction with a microcomputer via an I^2C bus.

Tuning

This is performed using frequency-locked loop digital control. Data corresponding to the required tuner frequency is stored in a 15-bit frequency buffer. The actual tuner frequency, divided by a factor of 256 (or by 64) by a prescaler, is applied via a gate to a 15-bit frequency counter. This input (FDIV) is measured over a period controlled by a time reference counter and is compared with the contents of the frequency buffer. The result of the comparison is used to control the tuning voltage so that the tuner frequency equals the contents of the frequency buffer multiplied by 50 kHz within a programmable tuning window (TUW).

The system cycles over a period of 6,4 ms (or 2,56 ms), controlled by the time reference counter which is clocked by an on-chip 4 MHz reference oscillator. Regulation of the tuning voltage is performed by a charge pump frequency-locked loop system. The charge IT flowing into the tuning voltage amplifier is controlled by the tuning counter, 3-bit DAC and the charge pump circuit. The charge IT is linear with the frequency deviation Δf in steps of 50 kHz. For loop gain control, the relationship $\Delta IT/\Delta f$ is programmable. In the normal mode (when control bits TUHN0 and TUHN1 are both at logic 1, see OPERATION), the minimum charge IT at $\Delta f = 50$ kHz equals 250 μA μs (typical).

By programming the tuning sensitivity bits (TUS), the charge IT can be doubled up to 6 times. If correction-in-band (COIB) is programmed, the charge can be further doubled up to three times in relation to the tuning voltage level. From this, the maximum charge IT at $\Delta f = 50$ kHz equals $2^6 \times 2^3 \times 250$ μA μs (typical).

The maximum tuning current I is 875 μA (typical). In the tuning-hold (TUHN) mode (TUHN is active LOW), the tuning current I is reduced and as a consequence the charge into the tuning amplifier is also reduced.

An in-lock situation can be detected by reading FLOCK. When the tuner oscillator frequency is within the programmable tuning window (TUW), FLOCK is set to logic 1. If the frequency is also within the programmable a.f.c. hold range (AFCR), which always occurs if AFCR is wider than TUW, control bit AFCT can be set to logic 1. When set, digital tuning will be switched off, a.f.c. will be switched on and FLOCK will stay at logic 1 as long as the oscillator frequency is within AFCR. If the frequency of the tuning oscillator does not remain within AFCR, AFCT is cleared automatically and the system reverts to digital tuning. To be able to detect this situation, the occurrence of positive and negative transitions in the FLOCK signal can be read (FL/1N and FL/0N). AFCT can also be cleared by programming the AFCT bit to logic 0.

The a.f.c. has programmable polarity and transconductance; the latter can be doubled up to 3 times, depending on the tuning voltage level if correction-in-band is used.

The direction of tuning is programmable by using control bits TDIRD (tuning direction down) and TDIRU (tuning direction up). If a tuner enters a region in which oscillation stops, then, providing the prescaler remains stable, no FDIV signal is supplied to CITAC. In this situation the system will tune up, moving away from frequency lock-in. This situation is avoided by setting TDIRD which causes the system to tune down. In normal operation TDIRD must be cleared.

If a tuner stops oscillating and the prescaler becomes unstable by going into self-oscillation at a very high frequency, the system will react by tuning down, moving away from frequency lock-in. To overcome this, the system can be forced to tune up at the lowest sensitivity (TUS) value, by setting TDIRU.

Setting both TDIRD and TDIRU causes the digital tuning to be interrupted and a.f.c. to be switched on.

The minimum tuning voltage which can be generated during digital tuning is programmable by VTMI to prevent the tuner being driven into an unspecified low tuning voltage region.

Control

For tuner band selection there are four outputs P10 to P13 which are capable of sourcing up to 50 mA at a voltage drop of less than 600 mV with respect to the separate power supply input V_{P2}.

For additional digital control, four open collector I/O ports P20 to P23 are provided. Ports P22 and P23 are capable of detecting positive and negative transitions in their input signals and are connected with the AFC+ and AFC− inputs respectively. The a.f.c. amplifier must be switched off when P22 and/or P23 are used. When a.f.c. is used, P22 and P23 must be programmed HIGH (high impedance state). With the aid of port P20, up to three independent module addresses can be programmed.

Reset

CITAC goes into the power-down-reset mode when V_{P1} is below 8,5 V (typical). In this mode all registers are set to a defined state. Reset can also be programmed.

OPERATION

Write

CITAC is controlled via a bidirectional two-wire I^2C bus; the I^2C bus is specified in our data handbook "ICs for digital systems in radio, audio, and video equipment". For programming, a module address, R/$\overline{W}$ bit (logic 0), an instruction byte and a data/control byte are written into CITAC in the format shown in Fig. 3.

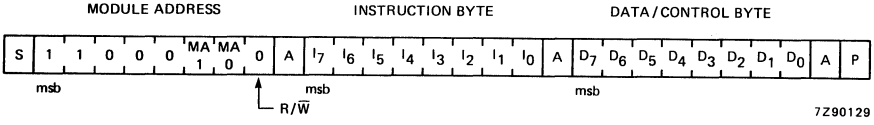


Fig. 3 I^2C bus write format.

The module address bits MA1, MA0 are used to give a 2-bit module address as a function of the voltage at port P20 as shown in Table 1.

Acknowledge (A) is generated by CITAC only when a valid address is received and the device is not in the power-down-reset mode ($V_{P1} > 8,5$ V (typical)).

OPERATION (continued)

Table 1 Valid module addresses

MA1	MA0	P20
0	0	don't care
0	1	GND
1	0	$\frac{1}{2}V_{P1}$
1	1	V_{P1}

Tuning

Tuning is controlled by the instruction and data/control bytes as shown in Fig. 4.

INSTRUCTION BYTE

	I_7	I_6	I_5	I_4	I_3	I_2	I_1	I_0
freq.	1	F14	F13	F12	F11	F10	F9	F8
TCD0	0	0	1	0	1	0	0	1
TCD1	0	0	1	0	1	0	1	0
TCD2	0	0	1	0	1	0	1	1

DATA/CONTROL BYTE

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
F7	F6	F5	F4	F3	F2	F1	F0
AFCT	VTMI0	AFCR1	AFCR0	TUHN1	TUHN0	TUW1	TUW0
VTMI1	COIB1	COIB0	AFCS1	AFCS0	TUS2	TUS1	TUS0
0	0	0	0	AFCP	FDIVM	TDIRD	TDIRU

7Z90125

Fig. 4 Tuning control format.

Frequency

Frequency is set when bit I_7 of the instruction byte is set to logic 1; the remainder of this byte together with the data/control byte are loaded into the frequency buffer. The frequency to which the tuner oscillator is regulated equals the decimal representation of the 15-bit word multiplied by 50 kHz. All frequency bits are set to logic 1 at reset.

Tuning hold

The TUHN bits are used to decrease the maximum tuning current and, as a consequence, the minimum charge IT (at $\Delta f = 50$ kHz) into the tuning amplifier.

Table 2 Tuning current control

TUHN1	TUHN0	typ. I_{max} μA	typ. IT_{min} $\mu A\ \mu s$	typ. ΔV_{TUNmin} at $C_{INT} = 1\ \mu F$ μV
0	0	3,5*	1*	1*
0	1	29	8	8
1	0	110	30	30
1	1	875	250	250

* Values after reset.

During tuning but before lock-in, the highest current value should be selected.
After lock-in the current may be reduced to decrease the tuning voltage ripple.

The lowest current value should not be used for tuning due to the input bias current of the tuning voltage amplifier (max. 5 nA). However it is good practice to program the lowest current value during tuner band switching.

Tuning sensitivity

To be able to program an optimum loop gain, the charge IT can be programmed by changing T using tuning sensitivity (TUS). Table 3 shows the minimum charge IT obtained by programming the TUS bits at $\Delta f = 50$ kHz; TUHN0 and TUHN1 = logic 1.

Table 3 Minimum charge IT as a function of TUS

$\Delta f = 50$ kHz; TUHN0 = logic 1; TUHN1 = logic 1

TUS2	TUS1	TUS0	typ. IT_{min} mA μs	typ. ΔV_{TUNmin} at $C_{INT} = 1\ \mu F$ mV
0	0	0	0,25*	0,25*
0	0	1	0,5	0,5
0	1	0	1	1
0	1	1	2	2
1	0	0	4	4
1	0	1	8	8
1	1	0	16	16

* Values after reset.

DEVELOPMENT DATA

Correction-in-band

This control is used to correct the loop gain of the tuning system to reduce in-band variations due to a non-linear voltage/frequency characteristic of the tuner. Correction-in-band (COIB) controls the time T of the charge equation IT and takes into account the tuning voltage V_{TUN} to give charge multiplying factors as shown in Table 4.

Table 4 Programming correction-in-band

COIB1	COIB0	charge multiplying factors at typical values of V_{TUN} at:			
		< 12 V	12 to 18 V	18 to 24 V	> 24 V
0	0	1*	1*	1*	1*
0	1	1	1	1	2
1	0	1	1	2	4
1	1	1	2	4	8

* Values after reset.

The transconductance multiplying factor of the a.f.c. amplifier is similar when COIB is used, except for the lowest transconductance which is not affected.

Tuning window

Digital tuning is interrupted and FLOCK is set to logic 1 (in-lock) when the absolute deviation $|\Delta f|$ between the tuner oscillator frequency and the programmed frequency is smaller than the programmed TUW value (see Table 5). If $|\Delta f|$ is up to 50 kHz above the values listed in Table 5, it is possible for the system to be locked depending on the phase relationship between FDIV and the reference counter.

OPERATION (continued)

Table 5 Tuning window programming

TUW1	TUW0	|Δf| (kHz)	tuning window (kHz)
0	0	0*	0*
0	1	50	100
1	0	150	300

* Values after reset.

A.F.C.

When AFCT is set to logic 1 it will not be cleared and the a.f.c. will remain on as long as |Δf| is less than the value programmed for the a.f.c. hold range AFCR (see Table 6). It is possible for the a.f.c. to remain on for values of up to 50 kHz more than the programmed value depending on the phase relationship between FDIV and the reference counter.

Table 6 A.F.C. hold range programming

AFCR1	AFCR0	|Δf| (kHz)	a.f.c. hold range (kHz)
0	0	0*	0*
0	1	350	700
1	0	750	1500

* Values after reset.

Transconductance

The transconductance (g) of the a.f.c. amplifier is programmed via the a.f.c. sensitivity bits AFCS as shown in Table 7.

Table 7 Transconductance programming

AFCS1	AFCS0	typ. transconductance (μA/V)
0	0	0,25*
0	1	25
1	0	50
1	1	100

* Value after reset.

A.F.C. polarity

If a positive differential input voltage is applied to the (switched on) a.f.c. amplifier, the tuning voltage V_{TUN} falls when the a.f.c. polarity bit AFCP is at logic 0 (value after reset). At AFCP = logic 1, V_{TUN} rises.

Minimum tuning voltage

Both minimum tuning voltage control bits, VTMI1 and VTMI0, are at logic 0 after reset. Further details are given in CHARACTERISTICS.

Frequency measuring window

The frequency measuring window which is programmed must correspond with the division factor of the prescaler in use (see Table 8).

Table 8 Frequency measuring window programming

FDIVM	prescaler division factor	cycle period (ms)	measuring window (ms)
0	256	6,4*	5,12*
1	64	2,56	1,28

* Values after reset.

Tuning direction

Both tuning direction bits, TDIRU (up) and TDIRD (down), are at logic 0 after reset.

Control

The instruction byte POD (port output data) is shown in Fig. 5, together with the corresponding data/control byte. Control is implemented as follows:

P13, P12, P11, P10 — Band select outputs. If a logic 1 is programmed on any of the POD bits D_3 to D_0, the relevant output goes HIGH. All outputs are LOW after reset.

P23, P22, P21, P20 — Open collector I/O ports. If a logic 0 is programmed on any of the POD bits D_7 to D_4, the relevant output is forced LOW. All outputs are at logic 1 after reset (high impedance state).

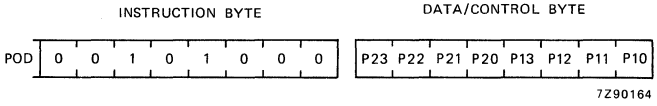


Fig. 5 Control programming.

OPERATION (continued)

Read

Information is read from CITAC when the R/$\overline{W}$ bit is set to logic 1. An acknowledge must be generated by the master after each data byte to allow transmission to continue. If no acknowledge is generated by the master the slave (CITAC) stops transmitting. The format of the information bytes is shown in Fig. 6.

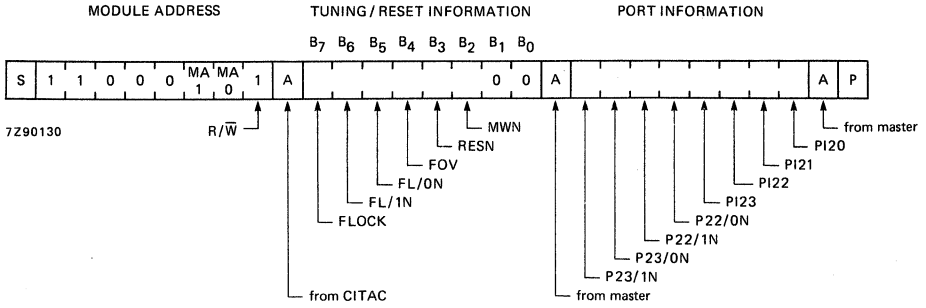


Fig. 6 Information byte format.

Tuning/reset information bits

FLOCK	Set to logic 1 when the tuning oscillator frequency is within the programmed tuning window.
FL/1N	Set to logic 0 (active LOW) when FLOCK changes from 0 to 1 and is reset to logic 1 automatically after tuning information has been read.
FL/0N	As for FL/1N but is set to logic 0 when FLOCK changes from 1 to 0.
FOV	Indicates frequency overflow. When the tuner oscillator frequency is too high with respect to the programmed frequency, FOV is at logic 1, and when too low, FOV is at logic 0. FOV is not valid when TDIRU and/or TDIRD are set to logic 1.
RESN	Set to logic 0 (active LOW) by a programmed reset or a power-down-reset. It is reset to logic 1 automatically after tuning/reset information has been read.
MWN	MWN (frequency measuring window, active LOW) is at logic 1 for a period of 1,28 ms, during which time the results of frequency measurement are processed. This time is independent of the cycle period. During the remaining time, MWN is at logic 0 and the received frequency is measured. When slightly different frequencies are programmed repeatedly and a.f.c. is switched on, the received frequency can be measured using FOV and FLOCK. To prevent the frequency counter and frequency buffer being loaded at the same time, frequency should be programmed only during the period of MWN = logic 0.

Port information bits

P23/1N, P22/1N	Set to logic 0 (active LOW) at a LOW-to-HIGH transition in the input voltage on P23 and P22 respectively. Both are reset to logic 1 after the port information has been read.
P23/0N, P22/0N	As for P23/1N and P22/1N but are set to logic 0 at a HIGH-to-LOW transition.
PI23, PI22, PI21, PI20	Indicate input voltage levels at P23, P22, P21 and P20 respectively. A logic 1 indicates a HIGH input level.

Reset

The programming to reset all registers is shown in Fig. 7. Reset is activated only at data byte HEX 06. Acknowledge is generated at every byte, provided that CITAC is not in the power-down-reset mode. After the general call address byte, transmission of more than one data byte is not allowed.

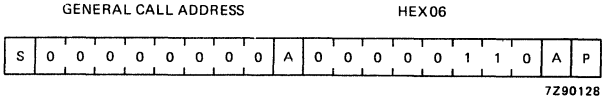


Fig. 7 Reset programming.

DEVELOPMENT DATA

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage ranges:		
(pin 5)	V_{P1}	−0,3 to + 18 V
(pin 14)	V_{P2}	−0,3 to + 18 V
(pin 9)	V_{P3}	−0,3 to + 36 V
Input/output voltage ranges:		
(pin 17)	V_{SDA}	−0,3 to + 18 V
(pin 18)	V_{SCL}	−0,3 to + 18 V
(pins 1 and 2)	$V_{P20, P21}$	−0,3 to + 18 V
(pins 3 and 4)	$V_{P22, P23, AFC}$	−0,3 to V_{P1}* V
(pin 6)	V_{TI}	−0,3 to V_{P1}* V
(pin 8)	V_{TUN}	−0,3 to V_{P3}* V
(pins 10 to 13)	V_{P1X}	−0,3 to V_{P2}** V
(pin 15)	V_{FDIV}	−0,3 to V_{P1}* V
(pin 16)	V_{OSC}	−0,3 to + 5 V
Total power dissipation	P_{tot}	max. 1000 mW
Storage temperature range	T_{stg}	−55 to + 125 °C
Operating ambient temperature	T_{amb}	−20 to + 70 °C

* Pin voltage may exceed supply voltage if current is limited to 10 mA.
** Pin voltage must not exceed 18 V but may exceed V_{P2} if current is limited to 200 mA.

CHARACTERISTICS

T_{amb} = 25 °C; V_{P1}, V_{P2}, V_{P3} at typical voltages, unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply voltages	V_{P1}	10,5	12	13,5	V
	V_{P2}	4,7	13	16	V
	V_{P3}	30	32	35	V
Supply currents (no outputs loaded)	I_{P1}	14	23	40	mA
	I_{P2}	0	–	0,1	mA
	I_{P3}	0,2	0,6	2	mA
Additional supply currents (A)	I_{P2A}	–2	–	I_{OHP1X}	mA
(note 1)	I_{P3A}	0,2	–	2	mA
Total power dissipation	P_{tot}	–	300	–	mW
Operating ambient temperature	T_{amb}	–20	–	+70	°C
I²C bus inputs/outputs					
SDA input (pin 17); SCL input (pin 18)					
Input voltage HIGH (note 2)	V_{IH}	3	–	$V_{P1}-1$	V
Input voltage LOW	V_{IL}	–0,3	–	1,5	V
Input current HIGH (note 2)	I_{IH}	–	–	10	μA
Input current LOW (note 2)	I_{IL}	–	–	10	μA
SDA output (pin 17, open collector)					
Output voltage LOW at I_{OL} = 3 mA	V_{OL}	–	–	0,4	V
Maximum output sink current	I_{OL}	–	5	–	mA
Open collector I/O ports					
P20, P21, P22, P23 (pins 1 to 4, open collector)					
Input voltage HIGH (P20, P21)	V_{IH}	2	–	16	V
Input voltage HIGH (P22, P23) AFC switched off	V_{IH}	2	–	$V_{P1}-2$	V
Input voltage LOW	V_{IL}	–0,3	–	0,8	V
Input current HIGH	I_{IH}	–	–	25	μA
Input current LOW	$-I_{IL}$	–	–	25	μA
Output voltage LOW at I_{OL} = 2 mA	V_{OL}	–	–	0,4	V
Maximum output sink current	I_{OL}	–	4	–	mA

parameter		symbol	min.	typ.	max.	unit
A.F.C. amplifier						
Inputs AFC+, AFC– (pins 3, 4)						
Transconductance for input voltages up to 1 V differential:						
AFCS1	AFCS2					
0	0	g_{00}	100	250	800	nA/V
0	1	g_{01}	15	25	35	μA/V
1	0	g_{10}	30	50	70	μA/V
1	1	g_{11}	60	100	140	μA/V
Tolerance of transconductance multiplying factor (2, 4 or 8) when correction-in-band is used		ΔM_g	–20	–	+20	%
Input offset voltage		V_{Ioff}	–75	–	+75	mV
Common mode input voltage		V_{com}	3	–	$V_{P1}-2,5$	V
Common mode rejection ratio		CMRR	–	50	–	dB
Power supply (V_{P1}) rejection ratio		PSRR	–	50	–	dB
Input current (P22 and P23 programmed HIGH)		I_I	–	–	500	nA
Tuning voltage amplifier						
Input TI, output TUN (pins 6, 8)						
Maximum output voltage at $I_{load} = \pm 2,5$ mA		V_{TUN}	$V_{P3}-1,6$	–	$V_{P3}-0,4$	V
Minimum output voltage at $I_{load} = \pm 2,5$ mA:						
VTMI1	VTMI0					
0	0	V_{TM00}	300	–	500	mV
1	0	V_{TM10}	450	–	650	mV
1	1	V_{TM11}	650	–	900	mV
Maximum output source current		$-I_{TUNH}$	2,5	–	8	mA
Maximum output sink current		I_{TUNL}	–	40	–	mA
Input bias current		I_{TI}	–5	–	+5	nA
Power supply (V_{P3}) rejection ratio		PSRR	–	60	–	dB

DEVELOPMENT DATA

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Tuning voltage amplifier (continued)					
Minimum charge IT to tuning voltage amplifier					
TUHN1 TUHN0					
0 0	CH_{00}	0,4	1	1,7	μA μs
0 1	CH_{01}	4	8	14	μA μs
1 0	CH_{10}	15	30	48	μA μs
1 1	CH_{11}	130	250	370	μA μs
Tolerance of charge (or ΔV_{TUN}) multiplying factor when COIB and/or TUS are used	ΔCH	−20	–	+20	%
Maximum current I into tuning amplifier					
TUHN1 TUHN0					
0 0	I_{T00}	1,7	3,5	5,1	μA
0 1	I_{T01}	15	29	41	μA
1 0	I_{T10}	65	110	160	μA
1 1	I_{T11}	530	875	1220	μA
Correction-in-band					
Tolerance of correction-in-band levels 12 V, 18 V and 24 V	ΔV_{CIB}	−15	–	+15	%
Band-select output ports					
P10, P11, P12, P13 (pins 10 to 13)					
Output voltage HIGH at $-I_{OH}$ = 50 mA (note 3)	V_{OH}	V_{P2}−0,6	–	–	V
Output voltage LOW at I_{OL} = 2 mA	V_{OL}	–	–	0,4	V
Maximum output source current (note 3)	$-I_{OH}$	–	130	200	mA
Maximum output sink current	I_{OL}	–	5	–	mA
FDIV input (pin 15)					
Input voltage (peak-to-peak value) (t_{rise} and $t_{fall} \leqslant 40$ ns)	$V_{FDIV(p-p)}$	0,1	–	2	V
Duty cycle	–	40	–	60	%
Maximum input frequency	f_{max}	16	–	–	MHz
Input impedance	Z_i	–	8	–	kΩ
Input capacitance	C_i	–	5	–	pF

parameter	symbol	min.	typ.	max.	unit
OSC input (pin 24)					
Crystal resistance at resonance (4 MHz)	R_X	–	–	150	Ω
Power-down-reset					
Maximum supply voltage V_{P1} at which power-down-reset is active	V_{PD}	7,5	–	9,5	V
V_{P1} rise-time during power-up (up to V_{PD})	t_r	5	–	–	μs
Voltage level for valid module address					
Voltage level at P20 (pin 1) for valid module address as a function of MA1, MA0					
MA1 MA0					
0 0	V_{VA00}	−0,3	–	16	V
0 1	V_{VA01}	−0,3	–	0,8	V
1 0	V_{VA10}	2,5	–	$V_{P1}-2$	V
1 1	V_{VA11}	$V_{P1}-0,3$	–	V_{P1}	V

DEVELOPMENT DATA

Notes to the characteristics

1. For each band-select output which is programmed at logic 1, sourcing a current I_{OHP1X}, the additional supply currents (A) shown must be added to I_{P2} and I_{P3} respectively.
2. If $V_{P1} < 1$ V, the input current is limited to 10 μA at input voltages up to 16 V.
3. At continuous operation the output current should not exceed 50 mA. When the output is short-circuited to ground for several seconds the device may be damaged.
4. Values are proportional to V_{P1}.

I²C BUS TIMING (Fig. 8)

I²C bus load conditions are as follows:
4 kΩ pull-up resistor to +5 V; 200 pF capacitor to GND.

All values are referred to V_{IH} = 3 V and V_{IL} = 1,5 V.

parameter	symbol	min.	typ.	max.	unit
Bus free before start	t_{BUF}	4	–	–	μs
Start condition set-up time	$t_{SU,STA}$	4	–	–	μs
Start condition hold time	$t_{HD,STA}$	4	–	–	μs
SCL, SDA LOW period	t_{LOW}	4	–	–	μs
SCL HIGH period	t_{HIGH}	4	–	–	μs
SCL, SDA rise time	t_R	–	–	1	μs
SCL, SDA fall time	t_F	–	–	0,3	μs
Data set-up time (write)	$t_{SU,DAT}$	1	–	–	μs
Data hold time (write)	$t_{HD,DAT}$	1	–	–	μs
Acknowledge (from CITAC) set-up time	$t_{SU,CAC}$	–	–	2	μs
Acknowledge (from CITAC) hold time	$t_{HD,CAC}$	0	–	–	μs
Stop condition set-up time	$t_{SU,STO}$	4	–	–	μs
Data set-up time (read)	$t_{SU,RDA}$	–	–	2	μs
Data hold time (read)	$t_{HD,RDA}$	0	–	–	μs
Acknowledge (from master) set-up time	$t_{SU,MAC}$	1	–	–	μs
Acknowledge (from master) hold time	$t_{HD,MAC}$	2	–	–	μs

Note

Timings $t_{SU,DAT}$ and $t_{HD,DAT}$ deviate from the I²C bus specification .
After reset has been activated, transmission may only be started after a 50 μs delay.

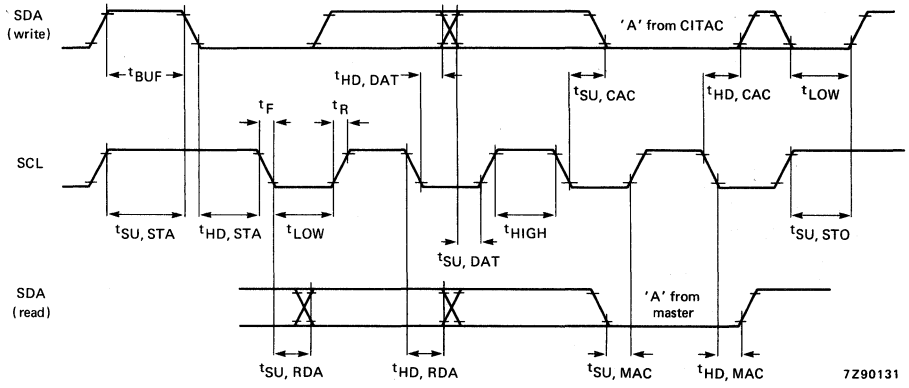


Fig. 8 I²C bus timing SAB3036.

COMPUTER INTERFACE FOR TUNING AND CONTROL (CITAC)

GENERAL DESCRIPTION

The SAB3037 provides closed-loop digital tuning of TV receivers, with or without a.f.c., as required. It also controls up to 4 analogue functions, 4 general purpose I/O ports and 4 high-current outputs for tuner band selection.

The IC is used in conjunction with a microcomputer from the MAB8400 family and is controlled via a two-wire, bidirectional I^2C bus.

Features

- Combined analogue and digital circuitry minimizes the number of additional interfacing components required
- Frequency measurement with resolution of 50 kHz
- Selectable prescaler divisor of 64 or 256
- 32 V tuning voltage amplifier
- 4 high-current outputs for direct band selection
- 4 static digital to analogue converters (DACs) for control of analogue functions
- Four general purpose input/output (I/O) ports
- Tuning with control of speed and direction
- Tuning with or without a.f.c.
- Single-pin, 4 MHz on-chip oscillator
- I^2C bus slave transceiver

QUICK REFERENCE DATA

Supply voltages				
(pin 13)	V_{P1}	typ.	12	V
(pin 19)	V_{P2}	typ.	13	V
(pin 14)	V_{P3}	typ.	32	V
Supply currents (no outputs loaded)				
(pin 13)	I_{P1}	typ.	30	mA
(pin 19)	I_{P2}	typ.	0,1	mA
(pin 14)	I_{P3}	typ.	0,6	mA
Total power dissipation	P_{tot}	typ.	380	mW
Operating ambient temperature range	T_{amb}	−20 to +70		°C

PACKAGE OUTLINE

24-lead DIL; plastic (SOT-101A).

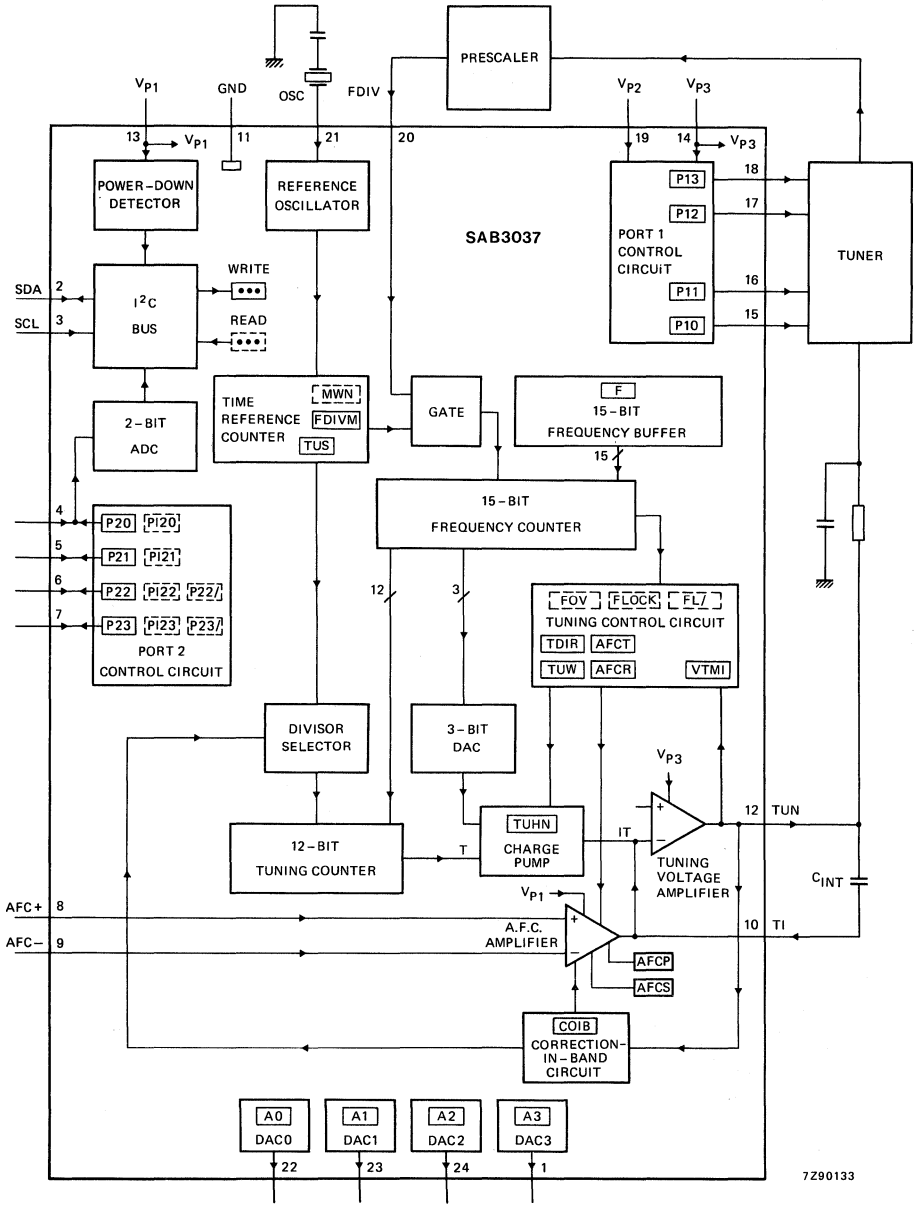


Fig. 1 Block diagram.

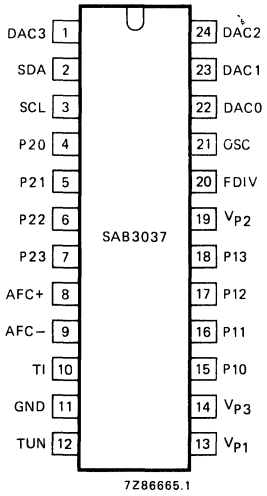


Fig. 2 Pinning diagram.

PINNING

1	DAC3	output of static DAC
2	SDA	serial data line (I²C bus)
3	SCL	serial clock line (I²C bus)
4	P20	general purpose input/output ports
5	P21	general purpose input/output ports
6	P22	general purpose input/output ports
7	P23	general purpose input/output ports
8	AFC+	a.f.c. inputs
9	AFC−	a.f.c. inputs
10	TI	tuning voltage amplifier inverting input
11	GND	ground
12	TUN	tuning voltage amplifier output
13	V_{P1}	+ 12 V supply voltage
14	V_{P3}	+ 32 V supply for tuning voltage amplifier
15	P10	high-current band-selection output ports
16	P11	high-current band-selection output ports
17	P12	high-current band-selection output ports
18	P13	high-current band-selection output ports
19	V_{P2}	positive supply for high-current band-selection output circuits
20	FDIV	input from prescaler
21	OSC	crystal oscillator input
22	DAC0	outputs of static DACs
23	DAC1	outputs of static DACs
24	DAC2	outputs of static DACs

DEVELOPMENT DATA

Purchase of Philips I²C components conveys a licence under the Philips' I²C patent to use the components in the I²C system provided the system conforms to the I²C specifications defined by Philips.

FUNCTIONAL DESCRIPTION

The SAB3037 is a monolithic computer interface which provides tuning and control functions and operates in conjunction with a microcomputer via an I^2C bus.

Tuning

This is performed using frequency-locked loop digital control. Data corresponding to the required tuner frequency is stored in a 15-bit frequency buffer. The actual tuner frequency, divided by a factor of 256 (or by 64) by a prescaler, is applied via a gate to a 15-bit frequency counter. This input (FDIV) is measured over a period controlled by a time reference counter and is compared with the contents of the frequency buffer. The result of the comparison is used to control the tuning voltage so that the tuner frequency equals the contents of the frequency buffer multiplied by 50 kHz within a programmable tuning window (TUW).

The system cycles over a period of 6,4 ms (or 2,56 ms), controlled by the time reference counter which is clocked by an on-chip 4 MHz reference oscillator. Regulation of the tuning voltage is performed by a charge pump frequency-locked loop system. The charge IT flowing into the tuning voltage amplifier is controlled by the tuning counter, 3-bit DAC and the charge pump circuit. The charge IT is linear with the frequency deviation Δf in steps of 50 kHz. For loop gain control, the relationship $\Delta IT/\Delta f$ is programmable. In the normal mode (when control bits TUHN0 and TUHN1 are both at logic 1, see OPERATION), the minimum charge IT at $\Delta f = 50$ kHz equals 250 $\mu A\ \mu s$ (typical).

By programming the tuning sensitivity bits (TUS), the charge IT can be doubled up to 6 times. If correction-in-band (COIB) is programmed, the charge can be further doubled up to three times in relation to the tuning voltage level. From this, the maximum charge IT at $\Delta f = 50$ kHz equals $2^6 \times 2^3 \times 250\ \mu A\ \mu s$ (typical).

The maximum tuning current I is 875 μA (typical). In the tuning-hold (TUHN) mode (TUHN is active LOW), the tuning current I is reduced and as a consequence the charge into the tuning amplifier is also reduced.

An in-lock situation can be detected by reading FLOCK. When the tuner oscillator frequency is within the programmable tuning window (TUW), FLOCK is set to logic 1. If the frequency is also within the programmable a.f.c. hold range (AFCR), which always occurs if AFCR is wider than TUW, control bit AFCT can be set to logic 1. When set, digital tuning will be switched off, a.f.c. will be switched on and FLOCK will stay at logic 1 as long as the oscillator frequency is within AFCR. If the frequency of the tuning oscillator does not remain within AFCR, AFCT is cleared automatically and the system reverts to digital tuning. To be able to detect this situation, the occurrence of positive and negative transitions in the FLOCK signal can be read (FL/1N and FL/0N). AFCT can also be cleared by programming the AFCT bit to logic 0.

The a.f.c. has programmable polarity and transconductance; the latter can be doubled up to 3 times, depending on the tuning voltage level if correction-in-band is used.

The direction of tuning is programmable by using control bits TDIRD (tuning direction down) and TDIRU (tuning direction up). If a tuner enters a region in which oscillation stops, then, providing the prescaler remains stable, no FDIV signal is supplied to CITAC. In this situation the system will tune up, moving away from frequency lock-in. This situation is avoided by setting TDIRD which causes the system to tune down. In normal operation TDIRD must be cleared.

If a tuner stops oscillating and the prescaler becomes unstable by going into self-oscillation at a very high frequency, the system will react by tuning down, moving away from frequency lock-in. To overcome this, the system can be forced to tune up at the lowest sensitivity (TUS) value, by setting TDIRU.

Setting both TDIRD and TDIRU causes the digital tuning to be interrupted and a.f.c. to be switched on.

The minimum tuning voltage which can be generated during digital tuning is programmable by VTMI to prevent the tuner being driven into an unspecified low tuning voltage region.

Control

For tuner band selection there are four outputs P10 to P13 which are capable of sourcing up to 50 mA at a voltage drop of less than 600 mV with respect to the separate power supply input V_{P2}.

For additional digital control, four open collector I/O ports P20 to P23 are provided. Ports P22 and P23 are capable of detecting positive and negative transitions in their input signals. With the aid of port P20, up to three independent module addresses can be programmed.

Four 6-bit digital-to-analogue converters DAC0 to DAC3 are provided for analogue control.

Reset

CITAC goes into the power-down-reset mode when V_{P1} is below 8,5 V (typical). In this mode all registers are set to a defined state. Reset can also be programmed.

OPERATION

Write

CITAC is controlled via a bidirectional two-wire I^2C bus; the I^2C bus is specified in our data handbook "ICs for digital systems in radio, audio, and video equipment". For programming, a module address, R/$\overline{W}$ bit (logic 0), an instruction byte and a data/control byte are written into CITAC in the format shown in Fig. 3.

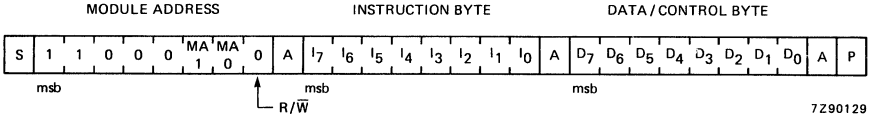


Fig. 3 I^2C bus write format.

The module address bits MA1, MA0 are used to give a 2-bit module address as a function of the voltage at port P20 as shown in Table 1.

Acknowledge (A) is generated by CITAC only when a valid address is received and the device is not in the power-down-reset mode ($V_{P1} > 8,5$ V (typical)).

Table 1 Valid module addresses

MA1	MA0	P20
0	0	don't care
0	1	GND
1	0	$\frac{1}{2}V_{P1}$
1	1	V_{P1}

OPERATION (continued)

Tuning

Tuning is controlled by the instruction and data/control bytes as shown in Fig. 4.

	INSTRUCTION BYTE								DATA/CONTROL BYTE							
	I_7	I_6	I_5	I_4	I_3	I_2	I_1	I_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
freq.	1	F14	F13	F12	F11	F10	F9	F8	F7	F6	F5	F4	F3	F2	F1	F0
TCD0	0	0	1	0	1	0	0	1	AFCT	VTMI0	AFCR1	AFCR0	TUHN1	TUHN0	TUW1	TUW0
TCD1	0	0	1	0	1	0	1	0	VTMI1	COIB1	COIB0	AFCS1	AFCS0	TUS2	TUS1	TUS0
TCD2	0	0	1	0	1	0	1	1	0	0	0	0	AFCP	FDIVM	TDIRD	TDIRU

7Z90125

Fig. 4 Tuning control format.

Frequency

Frequency is set when bit I_7 of the instruction byte is set to logic 1; the remainder of this byte together with the data/control byte are loaded into the frequency buffer. The frequency to which the tuner oscillator is regulated equals the decimal representation of the 15-bit word multiplied by 50 kHz. All frequency bits are set to logic 1 at reset.

Tuning hold

The TUHN bits are used to decrease the maximum tuning current and, as a consequence, the minimum charge IT (at Δf = 50 kHz) into the tuning amplifier.

Table 2 Tuning current control

TUHN1	TUHN0	typ. I_{max} μA	typ. IT_{min} $\mu A\ \mu s$	typ. ΔV_{TUNmin} at C_{INT} = 1 μF μV
0	0	3,5*	1*	1*
0	1	29	8	8
1	0	110	30	30
1	1	875	250	250

* Values after reset.

During tuning but before lock-in, the highest current value should be selected.
After lock-in the current may be reduced to decrease the tuning voltage ripple.

The lowest current value should not be used for tuning due to the input bias current of the tuning voltage amplifier (max. 5 nA). However it is good practice to program the lowest current value during tuner band switching.

Tuning sensitivity

To be able to program an optimum loop gain, the charge IT can be programmed by changing T using tuning sensitivity (TUS). Table 3 shows the minimum charge IT obtained by programming the TUS bits at Δf = 50 kHz; TUHN0 and TUHN1 = logic 1.

Table 3 Minimum charge IT as a function of TUS

Δf = 50 kHz; TUHN0 = logic 1; TUHN1 = logic 1

TUS2	TUS1	TUS0	typ. IT_{min} mA μs	typ. ΔV_{TUNmin} at C_{INT} = 1 μF mV
0	0	0	0,25*	0,25*
0	0	1	0,5	0,5
0	1	0	1	1
0	1	1	2	2
1	0	0	4	4
1	0	1	8	8
1	1	0	16	16

* Values after reset.

Correction-in-band

This control is used to correct the loop gain of the tuning system to reduce in-band variations due to a non-linear voltage/frequency characteristic of the tuner. Correction-in-band (COIB) controls the time T of the charge equation IT and takes into account the tuning voltage V_{TUN} to give charge multiplying factors as shown in Table 4.

DEVELOPMENT DATA

Table 4 Programming correction-in-band

COIB1	COIB0	charge multiplying factors at typical values of V_{TUN} at:			
		< 12 V	12 to 18 V	18 to 24 V	> 24 V
0	0	1*	1*	1*	1*
0	1	1	1	1	2
1	0	1	1	2	4
1	1	1	2	4	8

* Values after reset.

The transconductance multiplying factor of the a.f.c. amplifier is similar when COIB is used, except for the lowest transconductance which is not affected.

Tuning window

Digital tuning is interrupted and FLOCK is set to logic 1 (in-lock) when the absolute deviation $|\Delta f|$ between the tuner oscillator frequency and the programmed frequency is smaller than the programmed TUW value (see Table 5). If $|\Delta f|$ is up to 50 kHz above the values listed in Table 5, it is possible for the system to be locked depending on the phase relationship between FDIV and the reference counter.

Table 5 Tuning window programming

TUW1	TUW0	$\|\Delta f\|$ (kHz)	tuning window (kHz)
0	0	0*	0*
0	1	50	100
1	0	150	300

* Values after reset.

OPERATION (continued)

A.F.C.

When AFCT is set to logic 1 it will not be cleared and the a.f.c. will remain on as long as $|\Delta f|$ is less than the value programmed for the a.f.c. hold range AFCR (see Table 6). It is possible for the a.f.c. to remain on for values of up to 50 kHz more than the programmed value depending on the phase relationship between FDIV and the reference counter.

Table 6 A.F.C. hold range programming

AFCR1	AFCR0	$\|\Delta f\|$ (kHz)	a.f.c. hold range (kHz)
0	0	0*	0*
0	1	350	700
1	0	750	1500

* Values after reset.

Transconductance

The transconductance (g) of the a.f.c. amplifier is programmed via the a.f.c. sensitivity bits AFCS as shown in Table 7.

Table 7 Transconductance programming

AFCS1	AFCS0	typ. transconductance (μA/V)
0	0	0,25*
0	1	25
1	0	50
1	1	100

* Value after reset.

A.F.C. polarity

If a positive differential input voltage is applied to the (switched on) a.f.c. amplifier, the tuning voltage V_{TUN} falls when the a.f.c. polarity bit AFCP is at logic 0 (value after reset). At AFCP = logic 1, V_{TUN} rises.

Minimum tuning voltage

Both minimum tuning voltage control bits, VTMI1 and VTMI0, are at logic 0 after reset. Further details are given in CHARACTERISTICS.

Frequency measuring window

The frequency measuring window which is programmed must correspond with the division factor of the prescaler in use (see Table 8).

Table 8 Frequency measuring window programming

FDIVM	prescaler division factor	cycle period (ms)	measuring window (ms)
0	256	6,4*	5,12*
1	64	2,56	1,28

* Values after reset.

Tuning direction

Both tuning direction bits, TDIRU (up) and TDIRD (down), are at logic 0 after reset.

Control

The instruction bytes POD (port output data) and DACX (digital-to-analogue converter control) are shown in Fig. 5, together with the corresponding data/control bytes. Control is implemented as follows:

P13, P12, P11, P10 — Band select outputs. If a logic 1 is programmed on any of the POD bits D_3 to D_0, the relevant output goes HIGH. All outputs are LOW after reset.

P23, P22, P21, P20 — Open collector I/O ports. If a logic 0 is programmed on any of the POD bits D_7 to D_4, the relevant output is forced LOW. All outputs are at logic 1 after reset (high impedance state).

DACX — Digital-to-analogue converters. The digital-to-analogue converter selected corresponds to the decimal equivalent of the DACX bits X1, X0. The output voltage of the selected DAC is set by programming the bits AX5 to AX0; the lowest output voltage is programmed with all data AX5 to AX0 at logic 0, or after reset has been activated.

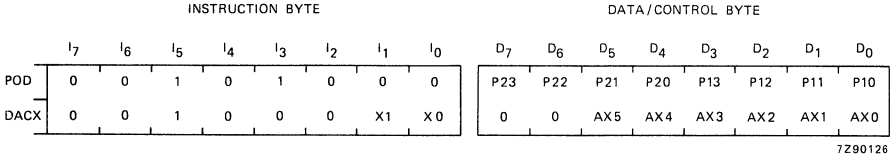


Fig. 5 Control programming.

Read

Information is read from CITAC when the R/$\overline{W}$ bit is set to logic 1. An acknowledge must be generated by the master after each data byte to allow transmission to continue. If no acknowledge is generated by the master the slave (CITAC) stops transmitting. The format of the information bytes is shown in Fig. 6.

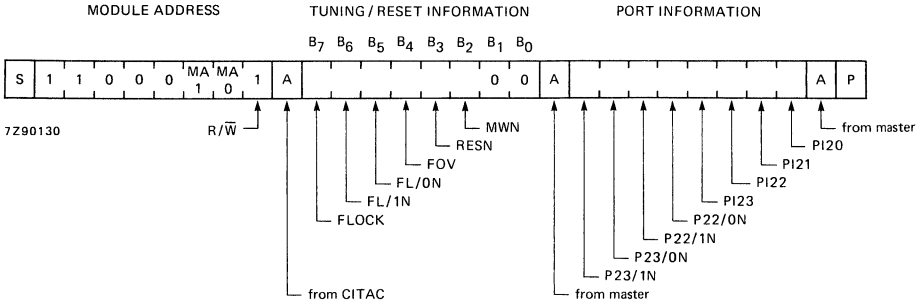


Fig. 6 Information byte format.

OPERATION (continued)

Tuning/reset information bits

FLOCK	Set to logic 1 when the tuning oscillator frequency is within the programmed tuning window.
FL/1N	Set to logic 0 (active LOW) when FLOCK changes from 0 to 1 and is reset to logic 1 automatically after tuning information has been read.
FL/0N	As for FL/1N but is set to logic 0 when FLOCK changes from 1 to 0.
FOV	Indicates frequency overflow. When the tuner oscillator frequency is too high with respect to the programmed frequency, FOV is at logic 1, and when too low, FOV is at logic 0. FOV is not valid when TDIRU and/or TDIRD are set to logic 1.
RESN	Set to logic 0 (active LOW) by a programmed reset or a power-down-reset. It is reset to logic 1 automatically after tuning/reset information has been read.
MWN	MWN (frequency measuring window, active LOW) is at logic 1 for a period of 1,28 ms, during which time the results of frequency measurement are processed. This time is independent of the cycle period. During the remaining time, MWN is at logic 0 and the received frequency is measured. When slightly different frequencies are programmed repeatedly and a.f.c. is switched on, the received frequency can be measured using FOV and FLOCK. To prevent the frequency counter and frequency buffer being loaded at the same time, frequency should be programmed only during the period of MWN = logic 0.

Port information bits

P23/1N, P22/1N	Set to logic 0 (active LOW) at a LOW-to-HIGH transition in the input voltage on P23 and P22 respectively. Both are reset to logic 1 after the port information has been read.
P23/0N, P22/0N	As for P23/1N and P22/1N but are set to logic 0 at a HIGH-to-LOW transition.
PI23, PI22, PI21, PI20	Indicate input voltage levels at P23, P22, P21 and P20 respectively. A logic 1 indicates a HIGH input level.

Reset

The programming to reset all registers is shown in Fig. 7. Reset is activated only at data byte HEX 06. Acknowledge is generated at every byte, provided that CITAC is not in the power-down-reset mode. After the general call address byte, transmission of more than one data byte is not allowed.

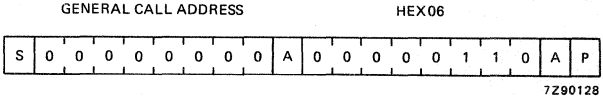


Fig. 7 Reset programming.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage ranges:			
(pin 13)	V_{P1}	−0,3 to +18	V
(pin 19)	V_{P2}	−0,3 to +18	V
(pin 14)	V_{P3}	−0,3 to +36	V
Input/output voltage ranges:			
(pin 2)	V_{SDA}	−0,3 to +18	V
(pin 3)	V_{SCL}	−0,3 to +18	V
(pins 4 to 7)	V_{P2X}	−0,3 to +18	V
(pins 8 and 9)	$V_{AFC+,AFC-}$	−0,3 to V_{P1}*	V
(pin 10)	V_{TI}	−0,3 to V_{P1}*	V
(pin 12)	V_{TUN}	−0,3 to V_{P3}*	V
(pins 15 to 18)	V_{P1X}	−0,3 to V_{P2}**	V
(pin 20)	V_{FDIV}	−0,3 to V_{P1}*	V
(pin 21)	V_{OSC}	−0,3 to +5	V
(pins 1 and 22 to 24)	V_{DACX}	−0,3 to V_{P1}*	V
Total power dissipation	P_{tot}	max. 1000	mW
Storage temperature range	T_{stg}	−55 to +125	°C
Operating ambient temperature range	T_{amb}	−20 to +70	°C

DEVELOPMENT DATA

* Pin voltage may exceed supply voltage if current is limited to 10 mA.

** Pin voltage must not exceed 18 V but may exceed V_{P2} if current is limited to 200 mA.

CHARACTERISTICS

T_{amb} = 25 °C; V_{P1}, V_{P2}, V_{P3} at typical voltages, unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply voltages	V_{P1}	10,5	12	13,5	V
	V_{P2}	4,7	13	16	V
	V_{P3}	30	32	35	V
Supply currents (no outputs loaded)	I_{P1}	18	30	45	mA
	I_{P2}	0	–	0,1	mA
	I_{P3}	0,2	0,6	2	mA
Additional supply currents (A)	I_{P2A}	–2	–	I_{OHP1X}	mA
(note 1)	I_{P3A}	0,2	–	2	mA
Total power dissipation	P_{tot}	–	380	–	mW
Operating ambient temperature	T_{amb}	–20	–	+70	°C
I²C bus inputs/outputs					
SDA input (pin 2); SCL input (pin 3)					
Input voltage HIGH (note 2)	V_{IH}	3	–	$V_{P1}-1$	V
Input voltage LOW	V_{IL}	–0,3	–	1,5	V
Input current HIGH (note 2)	I_{IH}	–	–	10	μA
Input current LOW (note 2)	I_{IL}	–	–	10	μA
SDA output (pin 2, open collector)					
Output voltage LOW at I_{OL} = 3 mA	V_{OL}	–	–	0,4	V
Maximum output sink current	I_{OL}	–	5	–	mA
Open collector I/O ports					
P20, P21, P22, P23 (pins 4 to 7, open collector)					
Input voltage HIGH	V_{IH}	2	–	16	V
Input voltage LOW	V_{IL}	–0,3	–	0,8	V
Input current HIGH	I_{IH}	–	–	25	μA
Input current LOW	$-I_{IL}$	–	–	25	μA
Output voltage LOW at I_{OL} = 2 mA	V_{OL}	–	–	0,4	V
Maximum output sink current	I_{OL}	–	4	–	mA

parameter	symbol	min.	typ.	max.	unit
A.F.C. amplifier					
Inputs AFC+, AFC– (pins 8, 9)					
Transconductance for input voltages up to 1 V differential:					
AFCS1 AFCS2					
0 0	g_{00}	100	250	800	nA/V
0 1	g_{01}	15	25	35	μA/V
1 0	g_{10}	30	50	70	μA/V
1 1	g_{11}	60	100	140	μA/V
Tolerance of transconductance multiplying factor (2, 4 or 8) when correction-in-band is used	ΔM_g	–20	–	+20	%
Input offset voltage	V_{Ioff}	–75	–	+75	mV
Common mode input voltage	V_{com}	3	–	$V_{P1}-2,5$	V
Common mode rejection ratio	CMRR	–	50	–	dB
Power supply (V_{P1}) rejection ratio	PSRR	–	50	–	dB
Input current	I_I	–	–	500	nA
Tuning voltage amplifier					
Input TI, output TUN (pins 10, 12)					
Maximum output voltage at $I_{load} = \pm 2,5$ mA	V_{TUN}	$V_{P3}-1,6$	–	$V_{P3}-0,4$	V
Minimum output voltage at $I_{load} = \pm 2,5$ mA:					
VTMI1 VTMI0					
0 0	V_{TM00}	300	–	500	mV
1 0	V_{TM10}	450	–	650	mV
1 1	V_{TM11}	650	–	900	mV
Maximum output source current	$-I_{TUNH}$	2,5	–	8	mA
Maximum output sink current	I_{TUNL}	–	40	–	mA
Input bias current	I_{TI}	–5	–	+5	nA
Power supply (V_{P3}) rejection ratio	PSRR	–	60	–	dB

DEVELOPMENT DATA

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Tuning voltage amplifier (continued)					
Minimum charge IT to tuning voltage amplifier					
TUHN1 TUHN0					
0 0	CH_{00}	0,4	1	1,7	μA μs
0 1	CH_{01}	4	8	14	μA μs
1 0	CH_{10}	15	30	48	μA μs
1 1	CH_{11}	130	250	370	μA μs
Tolerance of charge (or ΔV_{TUN}) multiplying factor when COIB and/or TUS are used	ΔCH	−20	–	+20	%
Maximum current I into tuning amplifier					
TUHN1 TUHN0					
0 0	I_{T00}	1,7	3,5	5,1	μA
0 1	I_{T01}	15	29	41	μA
1 0	I_{T10}	65	110	160	μA
1 1	I_{T11}	530	875	1220	μA
Correction-in-band					
Tolerance of correction-in-band levels 12 V, 18 V and 24 V	ΔV_{CIB}	−15	–	+15	%
Band-select output ports					
P10, P11, P12, P13 (pins 15 to 18)					
Output voltage HIGH at $-I_{OH}$ = 50 mA (note 3)	V_{OH}	V_{P2}−0,6	–	–	V
Output voltage LOW at I_{OL} = 2 mA	V_{OL}	–	–	0,4	V
Maximum output source current (note 3)	$-I_{OH}$	–	130	200	mA
Maximum output sink current	I_{OL}	–	5	–	mA
FDIV input (pin 20)					
Input voltage (peak-to-peak value) (t_{rise} and $t_{fall} \leqslant 40$ ns)	$V_{FDIV(p-p)}$	0,1	–	2	V
Duty cycle	–	40	–	60	%
Maximum input frequency	f_{max}	14,5	–	–	MHz
Input impedance	Z_i	–	8	–	kΩ
Input capacitance	C_i	–	5	–	pF

parameter	symbol	min.	typ.	max.	unit
OSC input (pin 21)					
Crystal resistance at resonance (4 MHz)	R_X	–	–	150	Ω
DAC outputs 0 to 3 (pins 22 to 24 and pin 1)					
Maximum output voltage (no load) at V_{P1} = 12 V (note 4)	V_{DH}	10	–	11,5	V
Minimum output voltage (no load) at V_{P1} = 12 V (note 4)	V_{DL}	0,1	–	1	V
Positive value of smallest step (1 least-significant bit)	ΔV_D	0	–	350	mV
Deviation from linearity	–	–	–	0,5	V
Output impedance at $I_{load} = \pm 2$ mA	Z_o	–	–	70	Ω
Maximum output source current	$-I_{DH}$	–	–	6	mA
Maximum output sink current	I_{DL}	–	8	–	mA
Power-down-reset					
Maximum supply voltage V_{P1} at which power-down-reset is active	V_{PD}	7,5	–	9,5	V
V_{P1} rise-time during power-up (up to V_{PD})	t_r	5	–	–	μs
Voltage level for valid module address					
Voltage level at P20 (pin 4) for valid module address as a function of MA1, MA0					
MA1 MA0					
0 0	V_{VA00}	−0,3	–	16	V
0 1	V_{VA01}	−0,3	–	0,8	V
1 0	V_{VA10}	2,5	–	$V_{P1}-2$	V
1 1	V_{VA11}	$V_{P1}-0,3$	–	V_{P1}	V

DEVELOPMENT DATA

Notes to the characteristics

1. For each band-select output which is programmed at logic 1, sourcing a current I_{OHP1X}, the additional supply currents (A) shown must be added to I_{P2} and I_{P3} respectively.
2. If $V_{P1} < 1$ V, the input current is limited to 10 μA at input voltages up to 16 V.
3. At continuous operation the output current should not exceed 50 mA. When the output is short-circuited to ground for several seconds the device may be damaged.
4. Values are proportional to V_{P1}.

I²C BUS TIMING (Fig. 8)

I²C bus load conditions are as follows:
4 kΩ pull-up resistor to +5 V; 200 pF capacitor to GND.

All values are referred to V_{IH} = 3 V and V_{IL} = 1,5 V.

parameter	symbol	min.	typ.	max.	unit
Bus free before start	t_{BUF}	4	–	–	μs
Start condition set-up time	$t_{SU,STA}$	4	–	–	μs
Start condition hold time	$t_{HD,STA}$	4	–	–	μs
SCL, SDA LOW period	t_{LOW}	4	–	–	μs
SCL HIGH period	t_{HIGH}	4	–	–	μs
SCL, SDA rise time	t_R	–	–	1	μs
SCL, SDA fall time	t_F	–	–	0,3	μs
Data set-up time (write)	$t_{SU,DAT}$	1	–	–	μs
Data hold time (write)	$t_{HD,DAT}$	1	–	–	μs
Acknowledge (from CITAC) set-up time	$t_{SU,CAC}$	–	–	2	μs
Acknowledge (from CITAC) hold time	$t_{HD,CAC}$	0	–	–	μs
Stop condition set-up time	$t_{SU,STO}$	4	–	–	μs
Data set-up time (read)	$t_{SU,RDA}$	–	–	2	μs
Data hold time (read)	$t_{HD,RDA}$	0	–	–	μs
Acknowledge (from master) set-up time	$t_{SU,MAC}$	1	–	–	μs
Acknowledge (from master) hold time	$t_{HD,MAC}$	2	–	–	μs

Note

Timings $t_{SU,DAT}$ and $t_{HD,DAT}$ deviate from the I²C bus specification .
After reset has been activated, transmission may only be started after a 50 μs delay.

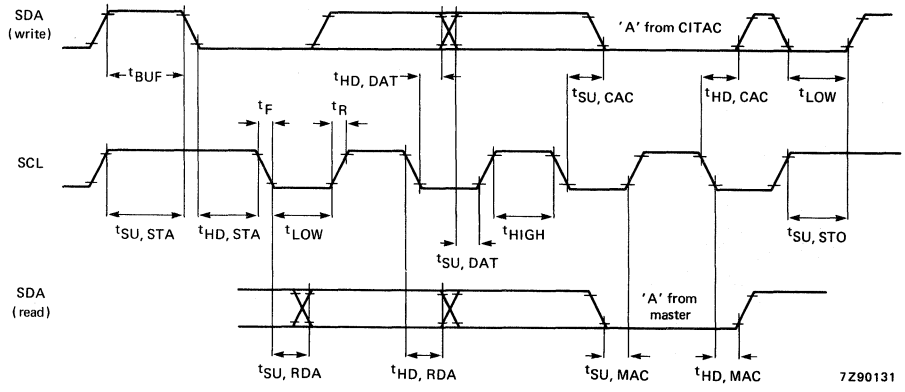


Fig. 8 I²C bus timing SAB3037.

REMOTE CONTROL SYSTEM FOR INFRARED OPERATION

The SAF1032P (receiver/decoder) and the SAF1039P (transmitter) form the basic parts of a sophisticated remote control system (pcm: pulse code modulation) for infrared operation. The ICs can be used, for example, in TV, audio, industrial equipment, etc.
Features:

SAF1032P receiver/decoder:

- 16 programme selection codes
- automatic preset to stand-by at power 'ON', including automatic analogue base settings to 50% and automatic preset of programme selection '1' code
- 3 analogue function controls, each with 63 steps
- single supply voltage
- protection against corrupt codes.

SAF1039P transmitter:

- 32 different control commands
- static keyboard matrix
- current drains from battery only during key closure time
- two transmission modes selectable.

The devices are implemented in LOCMOS (Local Oxidation Complementary MOS) technology to achieve an extremely low power consumption.
Inputs and outputs are protected against electrostatic effects in a wide variety of device-handling situations. However, to be totally safe, it is desirable to take handling precautions into account.

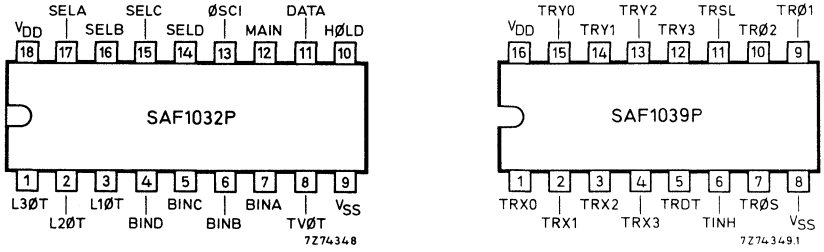


Fig. 1 Pin designations.

PACKAGE OUTLINES

SAF1032P: 18-lead DIL; plastic (SOT-102A).
SAF1039P: 16-lead DIL; plastic (SOT-38Z).

PINNING

To facilitate easy function recognition, each integrated circuit pin has been allocated a code as shown below.

SAF1032P

1	L3ØT	linear output	10	HØLD	control input
2	L2ØT	linear output	11	DATA	data input
3	L1ØT	linear output	12	MAIN	reset input
4	BIND	binary 8 output	13	ØSCI	clock input
5	BINC	binary 4 output	14	SELD	binary 8 output
6	BINB	binary 2 output	15	SELC	binary 4 output
7	BINA	binary 1 output	16	SELB	binary 2 output
8	TVØT	on/off input/output	17	SELA	binary 1 output
9	V_{SS}		18	V_{DD}	

SAF1039P

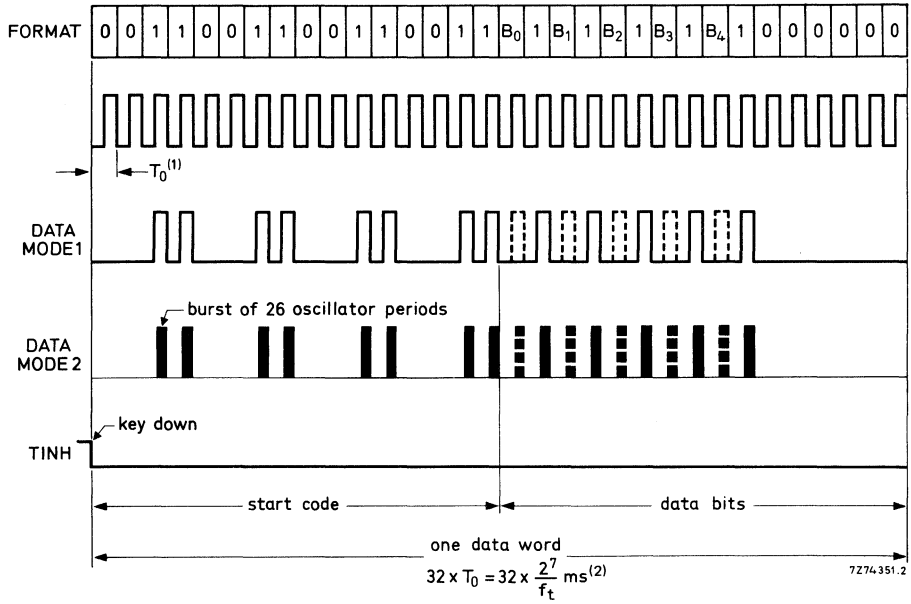
1	TRX0	keyboard input	9	TRØ1	oscillator control input
2	TRX1	keyboard input	10	TRØ2	oscillator control input
3	TRX2	keyboard input	11	TRSL	keyboard select line
4	TRX3	keyboard input	12	TRY3	keyboard input
5	TRDT	data output	13	TRY2	keyboard input
6	TINH	inhibit output/mode select input	14	TRY1	keyboard input
7	TRØS	oscillator output	15	TRY0	keyboard input
8	V_{SS}		16	V_{DD}	

BASIC OPERATING PRINCIPLES

The data to be transmitted are arranged as serial information with a fixed pattern (see Fig. 2), in which the data bit-locations B_0 to B_4 represent the generated key-command code. To cope with IR (infrared) interferences of other sources a selective data transmission is present. Each transmitted bit has a burst of 26 oscillator periods.

Before any operation will be executed in the receiver/decoder chip, the transmitted data must be accepted twice in sequence. This means the start code must be recognized each time a data word is applied and comparison must be true between the data bits of two successively received data words. If both requirements are met, one group of binary output buffers will be loaded with a code defined by the stored data bits, and an internal operation can also take place. See operating code table.

The contents of the 3 analogue function registers are available on the three outputs in a pulse code versus time modulation format after D (digital) to A (analogue) conversion. The proper analogue levels can be obtained by using simple integrated networks. For local control a second transmitter chip (SAF1039P) is used (see Fig. 7).



(1) T_0 = 1 clock period = 128 oscillator periods. (2) f_t in kHz.

Fig. 2 Pattern for data to be transmitted.

TIMING CONSIDERATIONS

The transmitter and receiver operate at different oscillator frequencies. Due to the design neither frequency is very critical, but correlation between them must exist. Calculation of these timing requirements shows the following.

With a tolerance of ±10% on the oscillator frequency (f_t) of the transmitter, the receiver oscillator frequency ($f_r = 3 \times f_t$) must be kept constant with a tolerance of ±20%.
On the other hand, the data pulse generated by the pulse stretcher circuit (at the receiver side) may vary ±25% in duration.

GENERAL DESCRIPTION OF THE SAF1039P TRANSMITTER

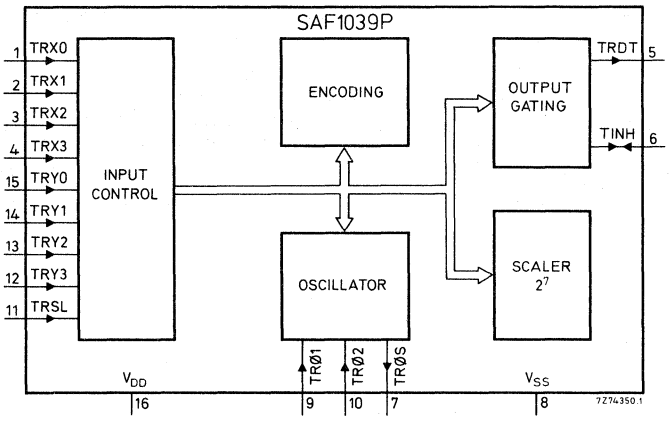


Fig. 3 Block diagram of SAF1039P transmitter.

Any keyboard activity on the inputs TRX0 to TRX3, TRY0 to TRY3 and TRSL will be detected. For a legal key depression, one key down at a time (one TRX and TRY input activated), the oscillator starts running and a data word, as shown on the previous page, is generated and supplied to the output TRDT. If none, or more than 2 inputs are activated at the same time, the input detection logic of the chip will generate an overall reset and the oscillator stops running (no legal key operation).

This means that for each key-bounce the logic will be reset, and by releasing a key the transmitted data are stopped at once.

The minimum key contact time required is the duration of two data words. The on-chip oscillator is frequency controlled with the external components R1 and C1 (see circuit Fig. 6); the addition of resistor R2 means that the oscillator frequency is practically independent of supply voltage variations. A complete data word is arranged as shown in Fig. 2, and has a length of 32 x T_0 ms, where $T_0 = 2^7/f_t$.

Operation mode

	DATA	FUNCTION OF TINH
1	unmodulated: LOCAL operation	output, external pull-up resistor to V_{DD}
2	modulated: REMOTE control	input, connected to V_{SS}

GENERAL DESCRIPTION OF THE SAF1032P RECEIVER/DECODER

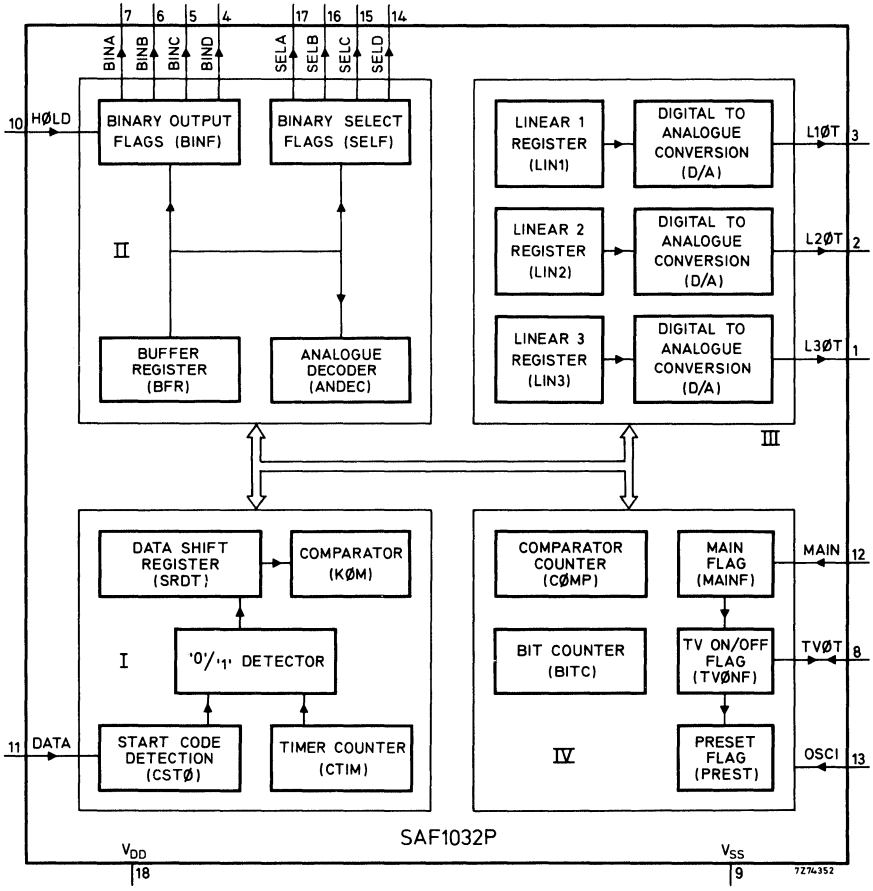


Fig. 4 Block diagram of SAF1032P receiver/decoder.

The logic circuitry of the receiver/decoder chip is divided into four main parts as shown in the block diagram above.

Part I

This part decodes the applied DATA information into logic '1' and '0'.
It also recognizes the start code and compares the stored data-bits with the new data-bits accepted.

Part II

This part stores the programme selection code in the output group (BINF) and memorizes it for condition HØLD = LOW.

It puts the functional code to output group (SELF) during data accept time, and decodes the internally used analogue commands (ANDEC).

Part III

This part controls the analogue function registers (each 6-bits long), and connects the contents of the three registers to the analogue outputs by means of D/A conversion. During sound mute, output L1ØT will be forced to HIGH level.

Part IV

This part keeps track for correct power 'ON' operation, and puts chip in 'stand-by' condition at supply voltage interruptions.

The logic design is dynamic and synchronous with the clock frequency (ØSCI), while the required control timing signals are derived from the bit counter (BITC).

Operation

Serial information applied to the DATA input will be translated into logic '1' and '0' by means of a time ratio detector.

After recognizing the start code (CSTØ) of the data word, the data bits will be loaded into the data shift register (SRDT). At the first trailing edge of the following data word a comparison (KØM) takes place between the contents of SRDT and the buffer register (BFR). If SRDT equals BFR, the required operation will be executed under control of the comparator counter (CØMP).

As shown in the operating code table on the next page, the 4-bit wide binary output buffer (BINF) will be loaded for BFR0 = '0', while for BFR0 = '1' the binary output buffer (SELF), also 4-bit wide will be activated during the data accept time.

At the same time operations involving the internal commands are executed. The contents of the analogue function registers (each 6-bits long) are controlled over 63 steps, with minimum and maximum detection, while the D/A conversion results in a pulsed output signal with a conversion period of 384 clock periods (see Fig. 5).

First power 'ON' will always put the chip in the 'stand-by' position. This results in an internal clearing of all logic circuitry and a 50% presetting of the contents of the analogue registers (analogue base value). The programme selection '1' code will also be prepared and all the outputs will be non-active (see operating output code table).

From 'stand-by' the chip can be made operational via a programme selection command, generated LOCAL or via REMOTE, or directly by forcing the TV ON/OFF output (TVØT) to zero for at least 2 clock periods of the oscillator frequency.

For POWER ON RESET a negative-going pulse should be applied to input MAIN, when V_{DD} is stabilized; pulse width LOW $\geqslant$ 100 μs.

Fig. 5 Analogue output pulses.

OPERATING CODE TABLE

key-matrix position			buffer BFR					BINF (BIN.)				SELF (SEL.)				function
TRX.	TRY.	TRSL	0	1	2	3	4	A	B	C	D	A	B	C	D	
0	0	0	0	0	1	1	0	0	0	0	0	1	1	1	1	programme select + ON
0	1	0	0	0	0	1	0	1	0	0	0	1	1	1	1	
0	2	0	0	0	1	0	0	0	1	0	0	1	1	1	1	
0	3	0	0	0	0	0	0	1	1	0	0	1	1	1	1	
1	0	0	0	1	1	1	0	0	0	1	0	1	1	1	1	
1	1	0	0	1	0	1	0	1	0	1	0	1	1	1	1	
1	2	0	0	1	1	0	0	0	1	1	0	1	1	1	1	
1	3	0	0	1	0	0	0	1	1	1	0	1	1	1	1	
2	0	0	0	0	1	1	1	0	0	0	1	1	1	1	1	programme select + ON
2	1	0	0	0	0	1	1	1	0	0	1	1	1	1	1	
2	2	0	0	0	1	0	1	0	1	0	1	1	1	1	1	
2	3	0	0	0	0	0	1	1	1	0	1	1	1	1	1	
3	0	0	0	1	1	1	1	0	0	1	1	1	1	1	1	
3	1	0	0	1	0	1	1	1	0	1	1	1	1	1	1	
3	2	0	0	1	1	0	1	0	1	1	1	1	1	1	1	
3	3	0	0	1	0	0	1	1	1	1	1	1	1	1	1	
0	0	1	1	0	1	1	0	X	X	X	X	0	1	1	1	analogue base
0	1	1	1	0	0	1	0	X	X	X	X	0	0	1	1	reg. (LIN3) + 1
0	2	1	1	0	1	0	0	X	X	X	X	0	1	0	1	reg. (LIN2) + 1
0	3	1	1	0	0	0	0	X	X	X	X	0	0	0	1	reg. (LIN1) + 1
1	0	1	1	1	1	1	0	0	0	0	0	0	0	0	0	OFF
1	1	1	1	1	0	1	0	X	X	X	X	1	0	1	1	reg. (LIN3) − 1
1	2	1	1	1	1	0	0	X	X	X	X	1	1	0	1	reg. (LIN2) − 1
1	3	1	1	1	0	0	0	X	X	X	X	1	0	0	1	reg. (LIN1) − 1
2	0	1	1	0	1	1	1	X	X	X	X	0	1	1	0	mute (set/reset)
2	1	1	1	0	0	1	1	X	X	X	X	0	0	1	0	spare functions
2	2	1	1	0	1	0	1	X	X	X	X	0	1	0	0	
2	3	1	1	0	0	0	1	X	X	X	X	0	0	0	0	
3	0	1	1	1	1	1	1	X	X	X	X	1	1	1	0	
3	1	1	1	1	0	1	1	X	X	X	X	1	0	1	0	
3	2	1	1	1	1	0	1	X	X	X	X	1	1	0	0	
3	3	1	1	1	0	0	1	X	X	X	X	1	0	0	0	

Note

Reset mute also on programme select codes, (LIN1) ± 1, and analogue base.

OPERATING OUTPUT CODE

	(BIN.)				(SEL.)				(L.ØT)			TVØT
	A	B	C	D	A	B	C	D	1	2	3	
'stand-by' OFF via remote	0	0	0	0	0	0	0	0	1	0	0	1
ON – 'not hold' condition non-operating	1	1	1	1	1	1	1	1	X	X	X	0
ON – 'hold' condition non-operating	X	X	X	X	1	1	1	1	X	X	X	0

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_{DD}-V_{SS}		−0,5 to 11	V
Input voltage	V_I	max.	11	V
Current into any terminal	$\pm I_I$	max.	10	mA
Power dissipation (per output)	P_o	max.	50	mW
Power dissipation (per package)	P_{tot}	max.	200	mW
Operating ambient temperature	T_{amb}		−40 to +85	°C
Storage temperature	T_{stg}		−65 to +150	°C

CHARACTERISTICS

T_{amb} = 0 to +85 °C (unless otherwise specified)

SAF1039P only

	symbol	min.	typ.	max.		V_{DD} V	T_{amb} °C
Recommended supply voltage	V_{DD}	7	–	10	V		
Supply current							
quiescent	I_{DD}	–	–	10	μA	10	25
		–	1	50	μA	7	65
operating; TRØ1 at V_{SS}; outputs unloaded; one keyboard switch closed	I_{DD}	–	–	1,7	mA	10	all
		–	0,8	–	mA	10	25
Inputs (note 1)							
TRØ2; TINH (note 2)							
input voltage HIGH	V_{IH}	$0,8V_{DD}$	–	V_{DD}	V	7 to 10	all
input voltage LOW	V_{IL}	0	–	$0,2V_{DD}$	V	7 to 10	all
input current	I_I	–	10^{-5}	1	μA	10	25
Outputs							
TRDT; TRØS; TRØ1							
output current HIGH at $V_{OH} = V_{DD} - 0,5$ V	$-I_{OH}$	0,4	–	–	mA	7	all
output current LOW at V_{OL} = 0,4 V	I_{OL}	0,4	–	–	mA	7	all
TRDT output leakage current when disabled $V_O = V_{SS}$ to V_{DD}	I_{OL}	–	–	1	μA	10	25
TINH							
output current LOW V_{OL} = 0,4 V	I_{OL}	0,4	–	–	mA	7	all
Oscillator							
maximum oscillator frequency	f_{osc}	120	–	–	kHz		
frequency variation with supply voltage, temperature and spread of IC properties at f_{nom} = 36 kHz (note 3)	Δf	–	–	$0,15f_{nom}$		7 to 10	all
oscillator current drain at f_{nom} = 36 kHz	I_{osc}	–	1,3	2,5	mA	10	25

Notes follow characteristics.

CHARACTERISTICS

T_{amb} = 0 to +85 °C (unless otherwise specified)

SAF1032P only

	symbol	min.	typ.	max.		V_{DD} V	T_{amb} °C
Recommended supply voltage	V_{DD}	8	–	10	V		
Supply current							
quiescent	I_{DD}	–	–	50	μA	10	25
		–	1	300	μA	10	85
operating; I_O = 0; at ØSCI frequency of 100 kHz	I_{DD}	–	–	1	mA	10	all
Inputs							
DATA; ØSCI; HØLD; TVØT (see note 4)							
input voltage HIGH	V_{IH}	$0{,}7V_{DD}$	–	V_{DD}	V	8 to 10	all
input voltage LOW	V_{IL}	0	–	$0{,}2V_{DD}$	V	8 to 10	all
MAIN; tripping levels							
input voltage increasing	V_{ti}	$0{,}4V_{DD}$	–	$0{,}9V_{DD}$	V	5 to 10	all
input voltage decreasing	V_{td}	$0{,}1V_{DD}$	–	$0{,}6V_{DD}$	V	5 to 10	all
input current; all inputs except TVØT	I_I	–	10^{-5}	1	μA	10	25
input signal rise and fall times (10% and 90% V_{DD}) all inputs except MAIN	t_r, t_f	–	–	5	μs	8 to 10	all
Outputs							
programme selection: BINA/B/C/D							
auxiliary: SELA/B/C/D							
analogue: L3ØT; L2ØT; L1ØT TVØT (note 4)							
all open drain n-channel							
output current LOW at V_{OL} = 0,4 V	I_{OL}	1,6	–	–	mA	8	all
output leakage current at $V_O = V_{SS}$ to V_{DD}	I_{OL}	–	–	10	μA	10	all

For note 4 see next page.

Notes to characteristics

1. The keyboard inputs (TRX.; TRY.; TRSL) are not voltage driven (see application information diagram Fig. 6).

   If one key is depressed, the circuit generates the corresponding code. The number of keys depressed at a time, and this being recognized by the circuit as an illegal operation, depends on the supply voltage (V_{DD}) and the leakage current (between device and printed-circuit board) externally applied to the keyboard inputs.

   If no leakage is assumed, the circuit recognizes an operation as illegal for any number of keys > 1 depressed at the same time with $V_{DD} = 7$ V. At a leakage due to a 1 MΩ resistor connected to each keyboard input and returned to either V_{DD} or V_{SS}, the circuit recognizes at least 2 keys depressed at a time with $V_{DD} \doteq 7$ V.

   The highest permissible values of the contact series resistance of the keyboard switches is 500 Ω.

2. Inhibit output transistor disabled.

3. Δf is the width of the distribution curve at 2 σ points (σ = standard deviation).

4. Terminal TVØT is input for manual 'ON'. When applying a LOW level TVØT becomes an output carrying a LOW level.

APPLICATION INFORMATION

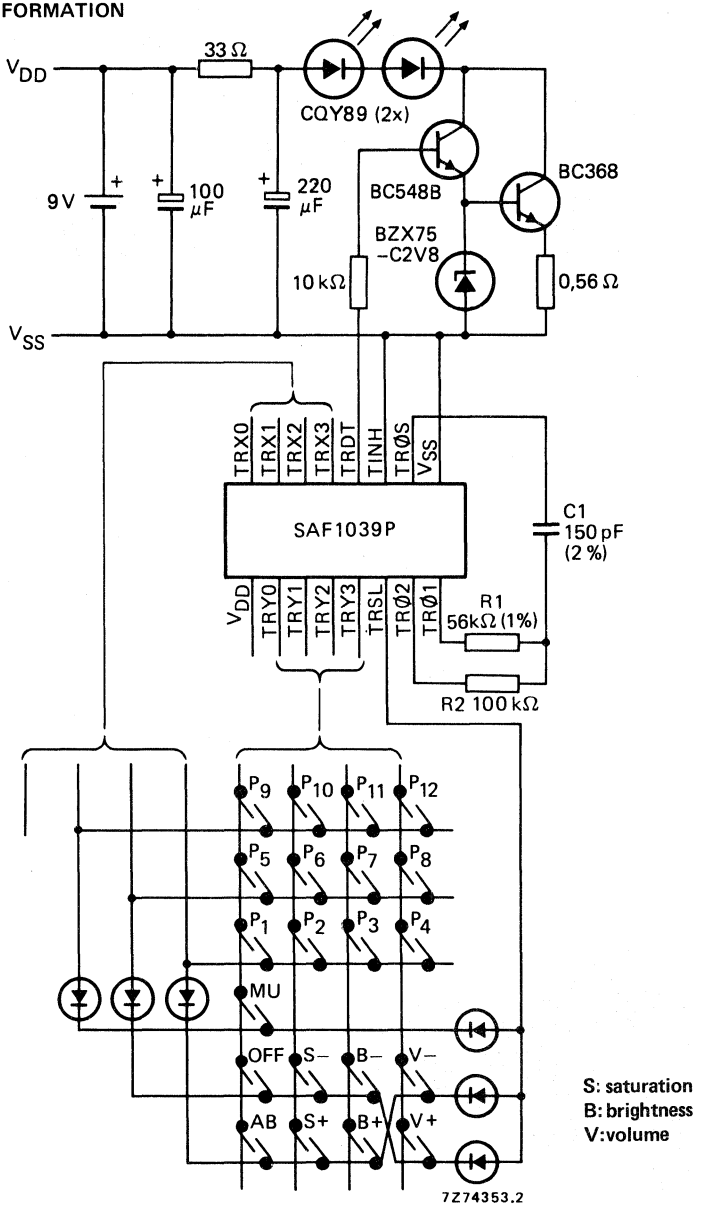


Fig. 6 Interconnection diagram of transmitter circuit SAF1039P in a remote control system, for a television receiver with 12 programmes.

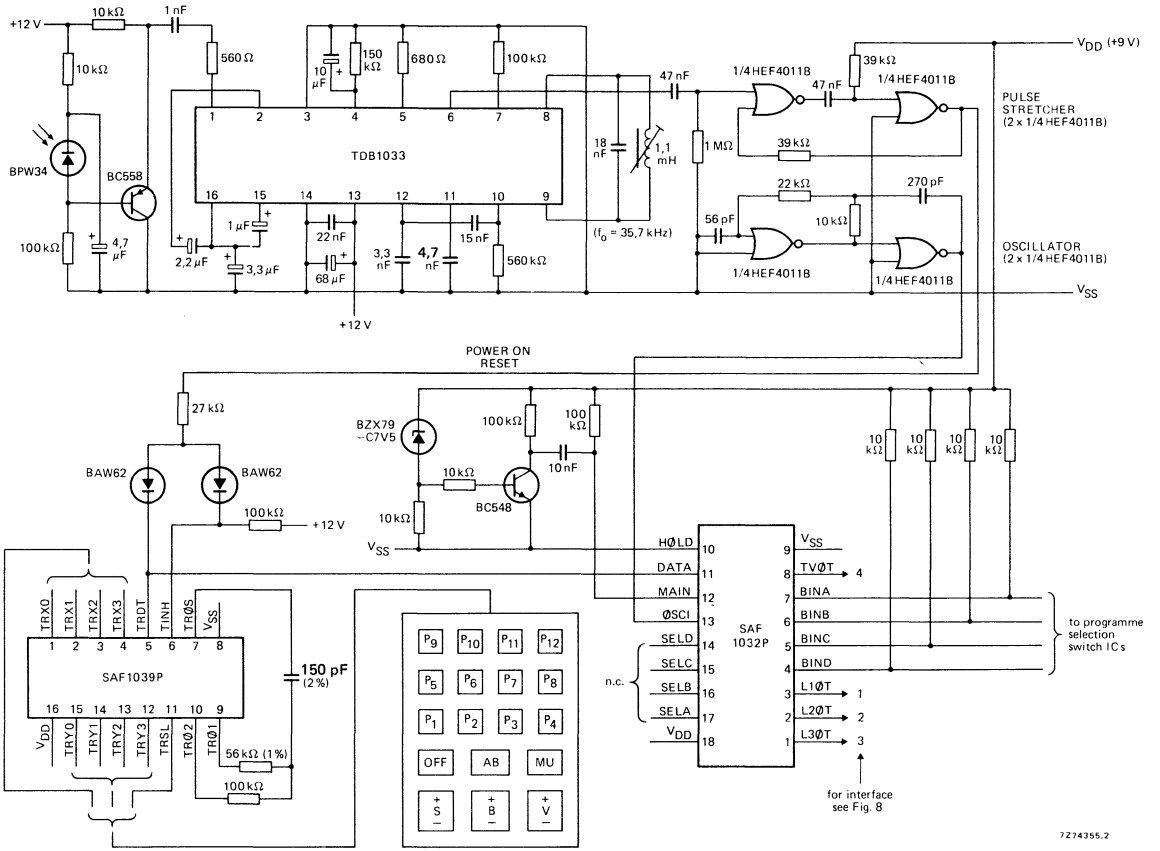


Fig. 7 Interconnection diagram showing the SAF1032P and SAF1039P used in a TV control system.

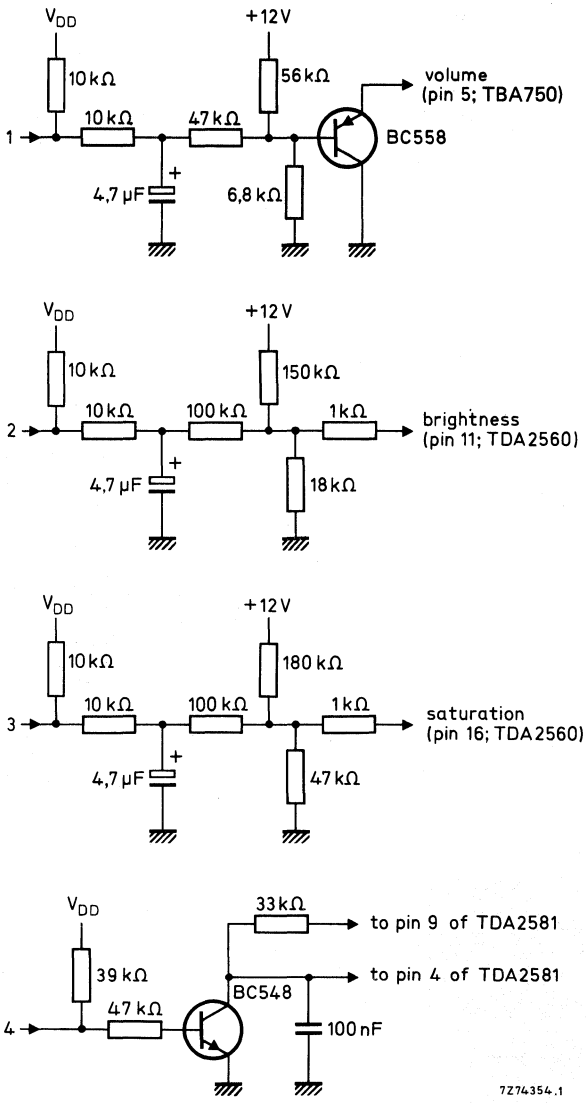


Fig. 8 Additional circuits from outputs L1ØT (1), L2ØT (2), L3ØT (3) and TVØT (4) of the SAF1032P in circuit of Fig. 7.

CLOCK/TIMER WITH SERIAL I/O

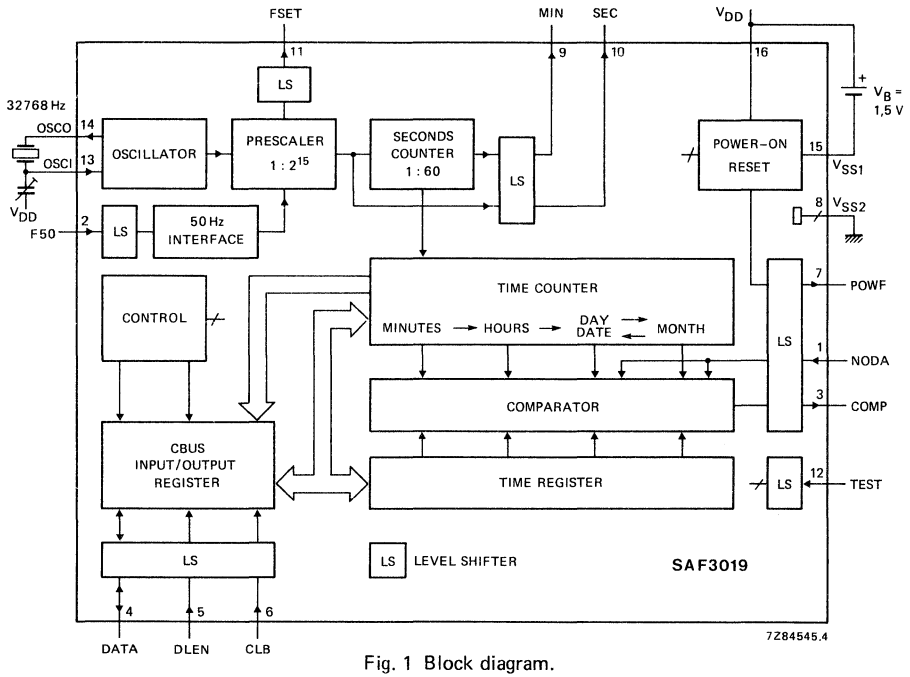


Fig. 1 Block diagram.

Features

- serial bidirectional CBUS interface for input/output of minutes, hours, day and month
- additional pulse outputs for seconds and minutes
- time register for presetting a time for alarm or remote switching functions
- battery back-up for clock function during supply interruption
- controlled either by the 50 Hz mains frequency or a crystal oscillator (automatic switch)

QUICK REFERENCE DATA

Supply voltage		V_{DD}	typ. 5 V
Battery supply voltage range	T_{amb} = −40 to + 85 °C	V_B	1,5 to 2,6 V
	T_{amb} = 0 to + 70 °C	V_B	1,3 to 2,6 V
Crystal oscillator frequency		f_{osc}	typ. 32 768 Hz
Alternative input frequency (pin 2)		f_{F50}	typ. 50 Hz
Operating ambient temperature range		T_{amb}	−40 to + 85 °C

PACKAGE OUTLINE

16-lead DIL; plastic (SOT-38DE).

GENERAL DESCRIPTION

The SAF3019 is a C-MOS integrated circuit comprising a digital clock for minutes, hours, day and month, as well as an additional register for resetting minutes, hours, day and month. The time counter provides cycles of 28, 30 or 31 days automatically, depending on the length of the month.

The time reference is the 50 Hz mains frequency or a 32 768 Hz on-chip reference oscillator with an external crystal. If the 50 Hz mains frequency is interrupted, the circuit is automatically switched to crystal oscillator operation.

The circuit can be controlled by a microcomputer. The data transmission (e.g. TIME SET and TIME READ of the time counter and time register) is achieved via the CBUS. A microcomputer then controls the data processing and the display unit drive.

The circuit uses a 5 V supply for data transmission. If this 5 V supply is interrupted, the clock function is maintained by a 1,5 V battery. The clock can then continue to function for an extended period, because the battery load current is only a few μA.

OPERATION DESCRIPTION

Oscillator and prescaler (outputs OSCO, FSET; inputs OSCI, F50)

The 32 768 Hz reference oscillator is achieved by connecting a quartz crystal between the output OSCO and the input OSCI (see also Fig. 7). The oscillator frequency of 32 768 Hz is divided by 256, and again by 128, in a prescaler. This results in a pulse once every second which controls the time counter. The divided-by-256 oscillator frequency (128 Hz) is available at FSET, which is used for fine-adjustment of the oscillator without loading it.

The circuit can also be operated by applying the 50 Hz mains frequency to input F50. This signal is divided-by-50 to obtain a pulse every second to drive the time counter. Input F50 has a Schmitt trigger characteristic which allows slowly rising pulses at this input.

If the mains frequency is interrupted, automatic quartz crystal operation is obtained (see Fig. 8). When the 50 Hz operation is not used, input F50 should be connected to ground (V_{SS2}).

Time counter (outputs SEC, MIN)

The one-second pulses are counted by a (no direct TIME READ) seconds counter and, after 60 seconds, they are transferred to successive counters for minutes, hours, day and month. This counter can be TIME SET and TIME READ by a microcomputer via the CBUS interface. The cycle length for the time counter is given in Table 1.

The seconds and minutes pulses are avilable at output SEC and MIN respectively, with a pulse ratio of 0,5.

The input/output DATA is set LOW at each transfer of seconds to the minutes counter (i.e. each minute), as long as the CBUS is not occupied by a DLEN = HIGH transmission.

DATA will be set HIGH again by a TIME ADDRESS/TIME READ or TIME SET instruction.

Table 1 Cycle lengths of time counter

unit	counting cycle	carry for following unit	content of month counter
minutes	00 59	59 → 00	1 12
hours	00 23	23 → 00	1 12
days	01 28	28 → 01	2
		or 29 → 01*	2
	01 30	30 → 01	4, 6, 9, 11
	01 31	31 → 01	1, 3, 5, 7, 8, 10, 12
months	01 12	12 → 01	

* The day counter may be set to 29.2. by a TIME SET instruction (for a leap year), then the month transfer occurs at 1.3.

Comparator (output COMP; input NODA)

The time register for a preset switching time (alarm or remote switching) is a 24-bit memory, which can also be set and read-out via the CBUS interface. If both the times of the time counter and the time register are equal, the output COMP becomes HIGH for one minute.

It is possible to choose a comparison between time counter and the time register either based upon minutes, hours, day and month (i.e. clock time *and* date) or minutes and hours (i.e. daily). It is controlled by bit 'UC' and input NODA (see also Table 3) during setting of the month register;

comparison with date: UC = 0 *and* NODA = LOW

comparison daily: UC = 1 *or* NODA = HIGH.

CBUS interface

The data transmission of the SAF3019 to the microcomputer (TIME READ) and vice versa (TIME SET) is possible via the CBUS; DATA (input/output), DLEN (input) and CLB (input).

Data and addresses are transmitted serially via the DATA line, which are synchronized with the clock burst (CLB) pulses from the microcomputer. The duration of the data transmission is determined by the number of CLB pulses when DLEN = HIGH.

The IC includes a word format checking function, which allows the CBUS to be used for controlling other circuits as well. The following word lengths are recognized as valid transmissions:

- TIME ADDRESS (3-bits and 1 start bit);
- TIME SET (10-bits and 1 start bit).

A TIME ADDRESS instruction always has to be followed by a TIME READ (7-bits) sequence. A TIME SET instruction combines address and data. With each instruction (each TIME ADDRESS and TIME READ instruction cycle) two digits of the time counter and time register can be set. The result is, that for a complete TIME READ and TIME SET transmission, 4 cycles TIME ADDRESS/TIME READ or 4 TIME SET instructions are needed.

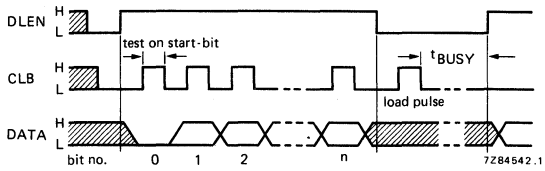


Fig. 2 CBUS data transmission.

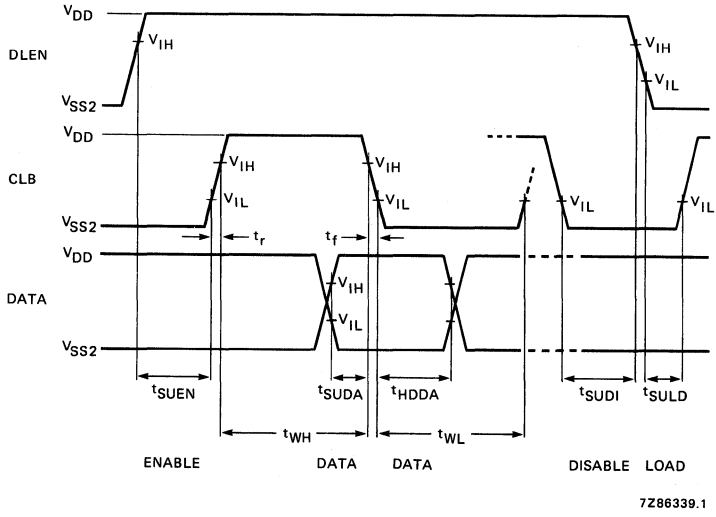


Fig. 3 CBUS timing.

TIME READ

First the bits S, A0 and A1 are transferred from the microcomputer to the SAF3019 with the TIME ADDRESS instruction. With the next instruction (TIME READ), the contents of the selected digits are transferred from the SAF3019 to the microcomputer.

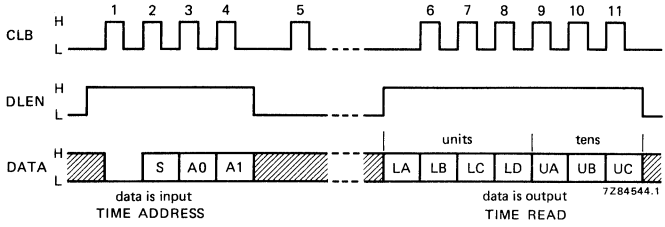


Fig. 4 TIME ADDRESS/TIME READ cycle.

Table 2 Selected digits with respect to the address bits and the TIME READ instruction function.

S	A0	A1	LA	LB	LC	LD	UA	UB	UC	instruction	
0	1	1	D	D	D	D	D	D	D	minutes	time read counter
0	0	1	D	D	D	D	D	D	0	hours	
0	1	0	D	D	D	D	D	D	0	date	
0	0	0	D	D	D	D	D	0	0	month	
1	1	1	D	D	D	D	D	D	D	minutes	time read register
1	0	1	D	D	D	D	D	D	0	hours	
1	1	0	D	D	D	D	D	D	0	date	
1	0	0	D	D	D	D	D	0	0	month	

D = data bit.

TIME SET

The TIME SET instruction transfers the address bits S, A0 and A1 as well as the selected digits of the BCD-coded incoming data from the microcomputer to the SAF3019. The last bit (UC) can control special functions. A TIME SET instruction will not stop the time counter, and also will not generate a non-selected digit for transmission.

The prescaler and seconds counter are reset with the TIME SET instruction when S = 0, A0 = 0, A1 = 0 (addressed for month) and UC = 0. If the seconds counter is between 30 and 59, this instruction generates a transfer for the minutes counter. Therefore, this instruction may be used for a very simple correction of the time counter if the deviation is within ±30 seconds.

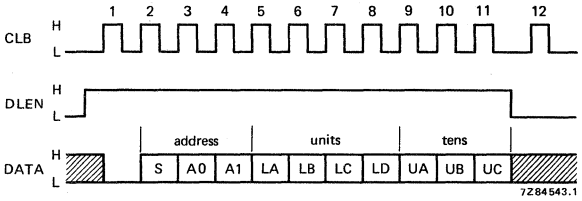


Fig. 5 Data format for TIME SET instruction.

Table 3 Selected digits with respect to the address bits and the possible TIME SET instruction function.

S	A0	A1	LA	LB	LC	LD	UA	UB	UC	instruction	
0	1	1	D	D	D	D	D	D	D	minutes	time set counter
0	0	1	D	D	D	D	D	D	X	hours	
0	1	0	D	D	D	D	D	D	X	date	
0	0	0	D	D	D	D	D	X	1	month	
0	0	0	X	X	X	X	X	X	0	seconds	reset counter
1	1	1	D	D	D	D	D	D	D	minutes	time set register
1	0	1	D	D	D	D	D	D	X	hours	
1	1	0	D	D	D	D	D	D	X	date	
1	0	0	D	D	D	D	D	X	0	month*	
1	0	0	D	D	D	D	D	X	1	month**	

D = data bit; X = 1 or 0.

* Compare *with* date. ** Compare *without* date.

Level shifters

The circuit has been designed for low-voltage operation. However, to interface with the microcomputer, most inputs and outputs have level shifters to operate with the 5 V supply voltage of the microcomputer. These level shifters only function when the 5 V supply (V_{DD}) is available. The internal clock function is independent of this supply.

Power failure (output POWF)

If the supply voltage V_{DD}-V_{SS1} is below a certain internal value (V_{POWF}), the power-failure output (POWF) is set HIGH. The threshold voltage V_{POWF} is lower than the minimum battery voltage V_{DD}-V_{SS1}. This battery is required as back-up for the logic circuitry. It is impossible to have data transmission via the CBUS when V_{DD}-$V_{SS1} < V_{POWF}$, however, the clock will continue running as long as V_{DD}-V_{SS1} does not drop to a lower value. The CBUS is released directly when V_{DD}-V_{SS1} becomes larger than V_{POWF}, but POWF stays HIGH until the next TIME SET instruction, which sets POWF LOW again.

N.B. The 5 V supply voltage (V_{DD}-V_{SS2}) must be switched off when exchanging the battery.

TEST input

The TEST input is used for testing purposes and it is connected to ground (V_{SS2}) for normal operation.

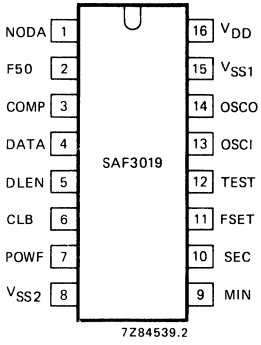


Fig. 6 Pinning diagram.

PINNING

16	V_{DD}	common positive supply (5 V; V_B = 1,5 V)
15	V_{SS1}	negative battery supply (V_B)
8	V_{SS2}	ground (V_{DD})
4	DATA	data input/output } CBUS (bidirectional)
5	DLEN	data line enable input } CBUS (bidirectional)
6	CLB	clock burst input } CBUS (bidirectional)
1	NODA	comparator mode select input
12	TEST	test mode input (normally ground)
2	F50	50 Hz mains frequency input
13	OSCI	input and output of the on-chip oscillator
14	OSCO	input and output of the on-chip oscillator
10	SEC	1 pulse per second output
9	MIN	1 pulse per minute output
3	COMP	comparator output
7	POWF	power failure output
11	FSET	frequency setting signal output (128 Hz)

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage ranges	$V_{DD} - V_{SS1}$		−0,5 to + 8	V
	$V_{DD} - V_{SS2}$		−0,5 to + 8	V
Voltage on any pin (except OSCI, OSCO)	V_I	V_{SS2}	−0,6 to V_{DD} + 0,6	V
Voltage on pins OSCI, OSCO	V_I	V_{SS1}	−0,6 to V_{DD} + 0,6	V
Input currents	$\|I_I\|$	max.	10	mA
Output currents	$\|I_O\|$	max.	10	mA
Power dissipation per output	P_O	max.	100	mW
Total power dissipation per package	P_{tot}	max.	200	mW
Operating ambient temperature range	T_{amb}		−40 to + 85	°C
Storage temperature range	T_{stg}		−65 to + 150	°C

D.C. CHARACTERISTICS

V_{SS2} = 0 V; V_{DD} = 4,5 to 5,5 V; T_{amb} = −40 to + 85 °C; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage	with respect to V_{SS2}*	V_{DD}	4,5	5	5,5	V
Battery voltage	between V_{DD} and V_{SS1}	V_B	1,5	–	2,6	V
	at T_{AMB} = 0 to 70 °C	V_B	1,3	–	2,6	V
Time keeping battery voltage		V_{BO}	1,3	–	2,6	V
Supply current	I_O = 0 mA**	$-I_{SS2}$	–	–	50	μA
Battery current	V_B = 1,5 V	$-I_{SS1}$	–	–	10	μA
Inputs DLEN, DATA, CLB, F50, NODA						
Input voltage HIGH		V_{IH}	0,7 V_{DD}	–	–	V
Input voltage LOW		V_{IL}	–	–	0,3 V_{DD}	V
Input current at $V_I = V_{SS2}$ or V_{DD}	V_{DD} = 5,5 V	$\|I_I\|$	–	–	1	μA
Input F50 hysteresis	$\Delta V = V_{IH} - V_{IL}$	ΔV	0,2	–	–	V
Outputs SEC, MIN, COMP, POWF (buffer outputs)						
Output voltage HIGH	$-I_O$ = 0,5 mA	V_{OH}	V_{DD} − 0,4	–	–	V
Output voltage LOW	I_O = 1,6 mA	V_{OL}	–	–	0,4	V
Output DATA (N-channel open drain)						
Output voltage LOW	I_O = 1,6 mA	V_{OL}	–	–	0,4	V
Output leakage current	V_O = 5,5 V (HIGH)	I_{OR}	–	–	1	μA

* All outputs are available down to $V_{SS2} = V_B$ at reduced current capability.

** $V_I = V_{SS2}$ or $V_I = V_{DD}$ at all inputs; quartz crystal oscillator operation: f = 32 768 Hz, series resistance of crystal $R_{s\,max}$ = 25 kΩ (40 kΩ for 0 to + 70 °C), C_L = 10 pF.

A.C. CHARACTERISTICS

V_{SS2} = 0 V; V_{DD} = 4,5 to 5,5 V; T_{amb} = −40 to + 85 °C; unless otherwise specified

See Figs 2 and 3 for all timing.

parameter	conditions	symbol	min.	typ.	max.	unit
Inputs DLEN, DATA, CLB, NODA						
Rise and fall times	note 1	t_r, t_f	—	—	1	μs
CLB pulse width HIGH		t_{WH}	4	—	∞	μs
CLB pulse width LOW		t_{WL}	4	—	∞	μs
Data set-up time DATA → CLB		t_{SUDA}	1	—	—	μs
Data hold time DATA → CLB		t_{HDDA}	2	—	—	μs
Enable set-up time DLEN → CLB		t_{SUEN}	2	—	—	μs
Disable set-up time CLB → DLEN		t_{SUDI}	2	—	—	μs
Set-up time DLEN → CLB (load pulse)		t_{SULD}	1	—	—	μs
Busy-time from load pulse to next start of transmission		t_{BUSY}	2	—	—	μs
CLB frequency		f_{CLB}	0	—	100	kHz
Input F50						
Rise and fall times	notes 1 and 2	t_r, t_f	—	—	10	ms
Pulse width HIGH		t_{WH}	30	—	—	μs
Pulse width LOW		t_{WL}	30	—	—	μs
Oscillator (OSCI, OSCO)						
Series resistance of crystal	f = 32 768 Hz at T_{amb} =	R_s	—	—	25	kΩ
	0 to 70 °C	R_s	—	—	40	kΩ
Load capacitance		C_L	—	10	—	pF

Notes

1. All timing values are referred to V_{IH} and V_{IL} within a voltage swing of minimum V_{SS2} to V_{DD}.
2. The supply current I_{SS2} increases at slow rise/fall times.

APPLICATION INFORMATION

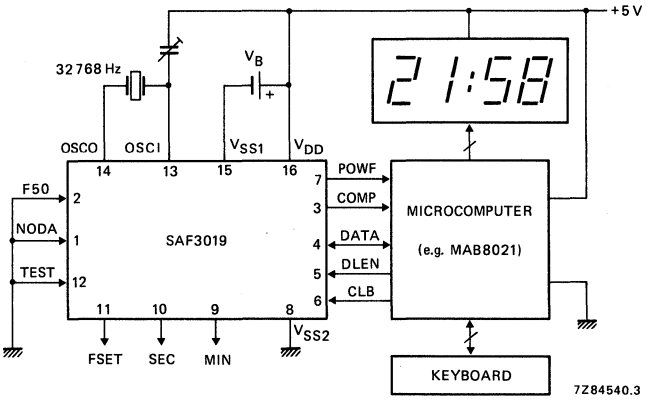


Fig. 7 Typical application of the SAF3019 in a microcomputer controlled system.

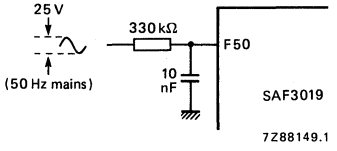


Fig. 8 Circuitry for applying the 50 Hz mains to input F50.

SOUND I.F. AMPLIFIER/DEMODULATOR FOR TV

The TBA120U is an i.f. amplifier with a symmetrical FM demodulator and an a.f. amplifier with adjustable output voltage. The a.f. amplifier is also provided with an output for volume control and an input for VCR operation.

The input and output of the TBA120U are especially designed for LC-circuits, but the input can also be used with a ceramic filter.

QUICK REFERENCE DATA

Supply voltage (pin 11)	V_P	typ.	12 V
Supply current	I_P	typ.	13,5 mA
I.F. voltage gain at f = 5,5 MHz	$G_{v\ if}$	typ.	68 dB
Input voltage starting limiting	V_i	typ.	30 μV
AM suppression at $\Delta f = \pm 50$ kHz	α	typ.	60 dB
A.F. output voltage adjustment range (pin 8)	$\Delta V_{o\ af}$	typ.	85 dB
A.F. output voltage at $\Delta f = \pm 50$ kHz (r.m.s. value)			
at pin 8	$V_{o\ af(rms)}$	typ.	1,2 V
at pin 12	$V_{o\ af(rms)}$	typ.	1,0 V

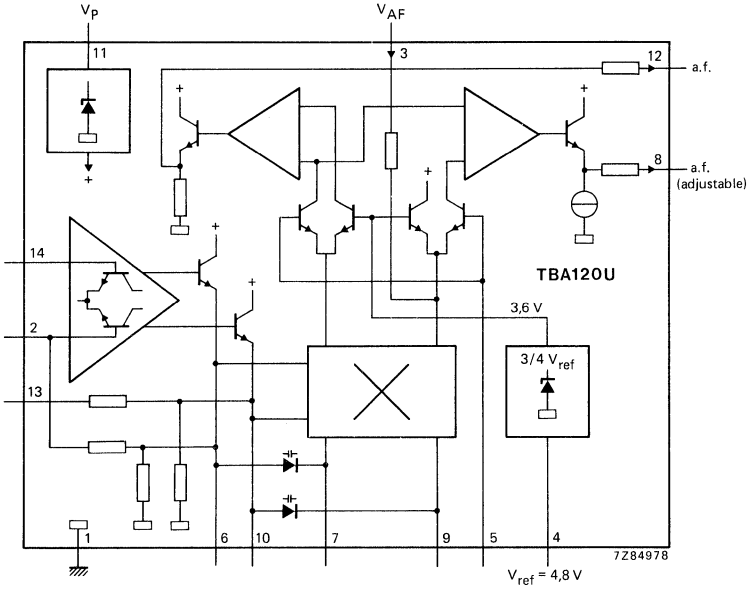


Fig. 1 Block diagram.

PACKAGE OUTLINE

14-lead DIL; plastic (SOT-27K, M, T).

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 11)	$V_P = V_{11-1}$	max.	18	V*
Adjustment voltage (pin 5)	V_{5-1}	max.	6	V
Total power dissipation	P_{tot}	max.	400	mW
By-pass resistance	R_{13-14}	max.	1	kΩ
Storage temperature range	T_{stg}		−40 to + 125	°C
Operating ambient temperature range	T_{amb}		−15 to + 70	°C

CHARACTERISTICS

V_P = 12 V; T_{amb} = 25 °C; f = 5,5 MHz

I.F. voltage gain	$G_{v\ if\ 6-14}$	typ.	68	dB
Input voltage starting limiting at Δf = ± 50 kHz; f_m = 1 kHz	V_i	typ. <	30 60	μV μV
I.F. output voltage at limiting (peak-to-peak value)	$V_{o\ if\ (p-p)}$	typ.	250	mV
AM suppression at Δf = ± 50 kHz; V_i = 500 μV; f_m = 1 kHz; m = 30%	α	> typ.	50 60	dB dB
I.F. residual voltage without de-emphasis at pin 12	$V_{if\ 12}$	typ.	30	mV
at pin 8	$V_{if\ 8}$	typ.	20	mV
A.F. voltage gain	$G_{v\ af\ 8-3}$	typ.	7,5	
A.F. adjustment at R_{4-5} = 5 kΩ; R_{5-1} = 13 kΩ	$\Delta V_{o\ af}$	 typ.	20 to 36 28	dB dB
A.F. output voltage control range	$\Delta V_{o\ af}$	> typ.	70 85	dB dB
Adjustment resistor**	R_{4-5}		1 to 10	kΩ
D.C. voltage portion at the a.f. outputs pin 12	V_{12-1}	typ.	5,6	V
pin 8	V_{8-1}	typ.	4,0	V
Output resistance of the a.f. outputs pin 12	$R_{o\ 12-1}$	typ.	1,1	kΩ
pin 8	$R_{o\ 8-1}$	typ.	1,1	kΩ
Input resistance of the a.f. input	$R_{i\ 3-1}$	typ.	2	kΩ
Stabilized reference voltage	$V_{4-1} = V_{ref}$	 typ.	4,2 to 5,3 4,8	V V
Source resistance of reference voltage source	R_{4-1}	typ.	12	Ω

* Supply voltage operating range is 10 to 18 V.

** Pin 5 must be connected to pin 4, when volume control adjustment is not applicable.

Hum suppression			
at pin 12	V_{12}/V_{11}	typ.	30 dB
at pin 8	V_8/V_{11}	typ.	35 dB
Supply current (pin 11)	$I_P = I_{11}$		9,5 to 17,5 mA
		typ.	13,5 mA
I.F. input impedance	$\|Z_i\|$	typ.	40 kΩ/4,5 pF
		>	15 kΩ/< 6 pF
A.F. output voltage at $\Delta f = \pm 50$ kHz; $f_m = 1$ kHz; $V_i = 10$ mV; $Q_o = 45$; r.m.s. value			
at pin 12	$V_{o\,af\,(rms)}$	typ.	1,0 V
at pin 8	$V_{o\,af\,(rms)}$	typ.	1,2 V
Distortion at $\Delta f = \pm 50$ kHz; $f_m = 1$ kHz; $V_i = 10$ mV; $Q_o = 20$	d_{tot}	typ.	1 %

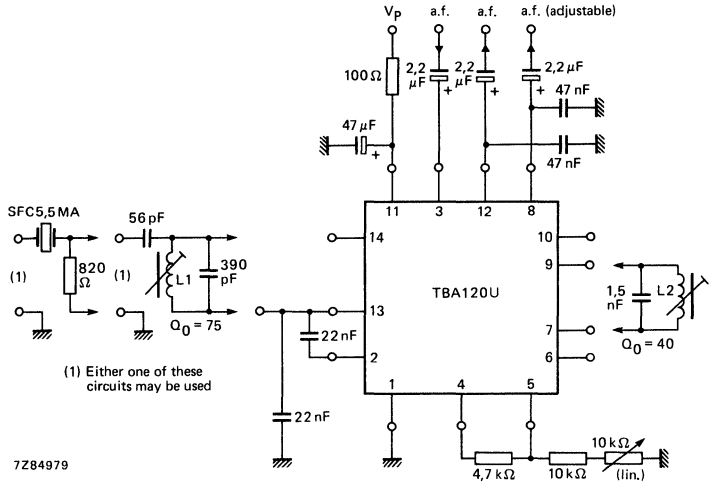


Fig. 2 Application example using TBA120U.

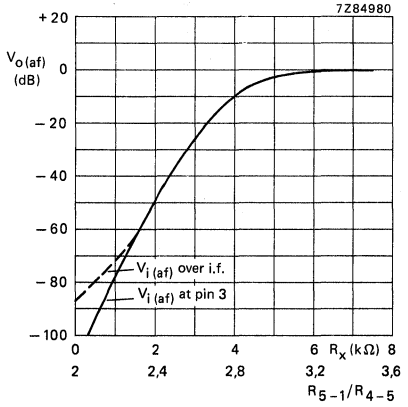


Fig. 3 The a.f. output voltage at pin 8 as a function of the resistance values as shown in Fig. 4.

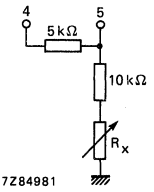
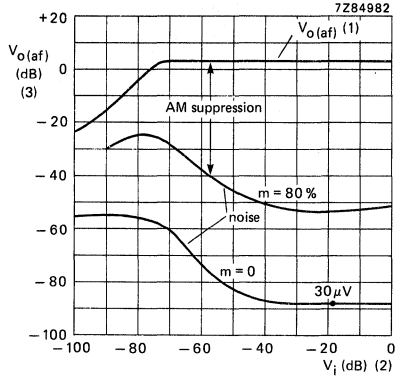


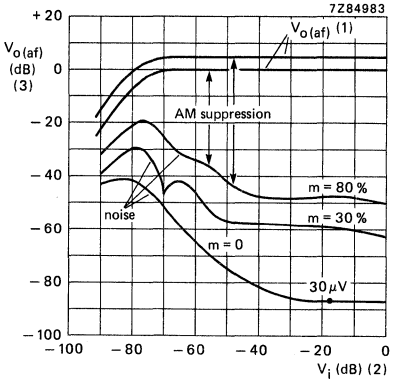
Fig. 4 Resistor conditions for curves in Fig. 3.



(1) $V_{o\,af}$ with de-emphasis at $\Delta f = \pm 50$ kHz; $f_m = 1$ kHz; $d_{tot} = 1{,}5\%$; 0 dB ≙ 770 mV.

(2) V_i: 0 dB ≙ 200 mV at 60 Ω.

Fig. 5 The a.f. output voltage at pin 8 as a function of the input voltage with SFC 5,5 MA at the input (see Fig. 2).



(1) $V_{o\,af}$ with de-emphasis at $f_m = 1$ kHz; 0 dB ≙ 770 mV;
curve a: $\Delta f = \pm 50$ kHz; $d_{tot} = 3\%$;
curve b: $\Delta f = \pm 25$ kHz; $d_{tot} = 1\%$.

(2) V_i: 0 dB ≙ 200 mV at pin 14.

Fig. 6 The a.f. output voltage at pin 8 as a function of the input voltage with broadband input (60 Ω).

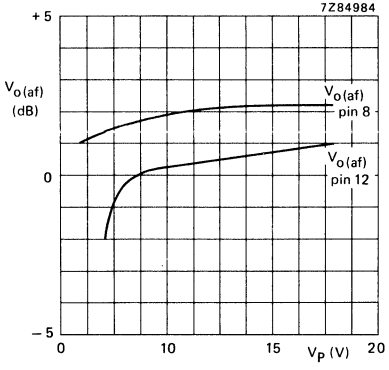


Fig. 7 The a.f. output voltages at pins 8 and 1 as a function of the supply voltage; 0 dB ≙ 770 mV.

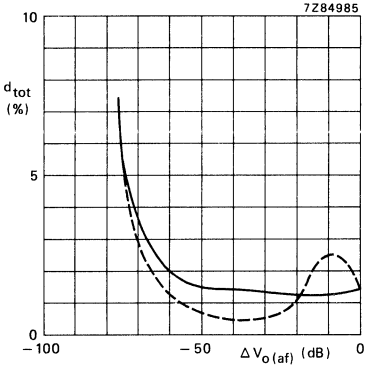


Fig. 8 Total distortion as a function of the a.f. output voltage change.
——— 0 dB ≙ 900 mV over i.f. (pin 8)
– – – – 0 dB ≙ 1,15 V (pin 8)

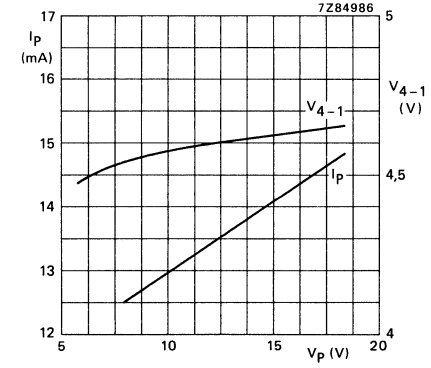


Fig. 9 Supply current and the reference voltage at pin 4 as a function of supply voltage.

REFERENCE COMBINATION

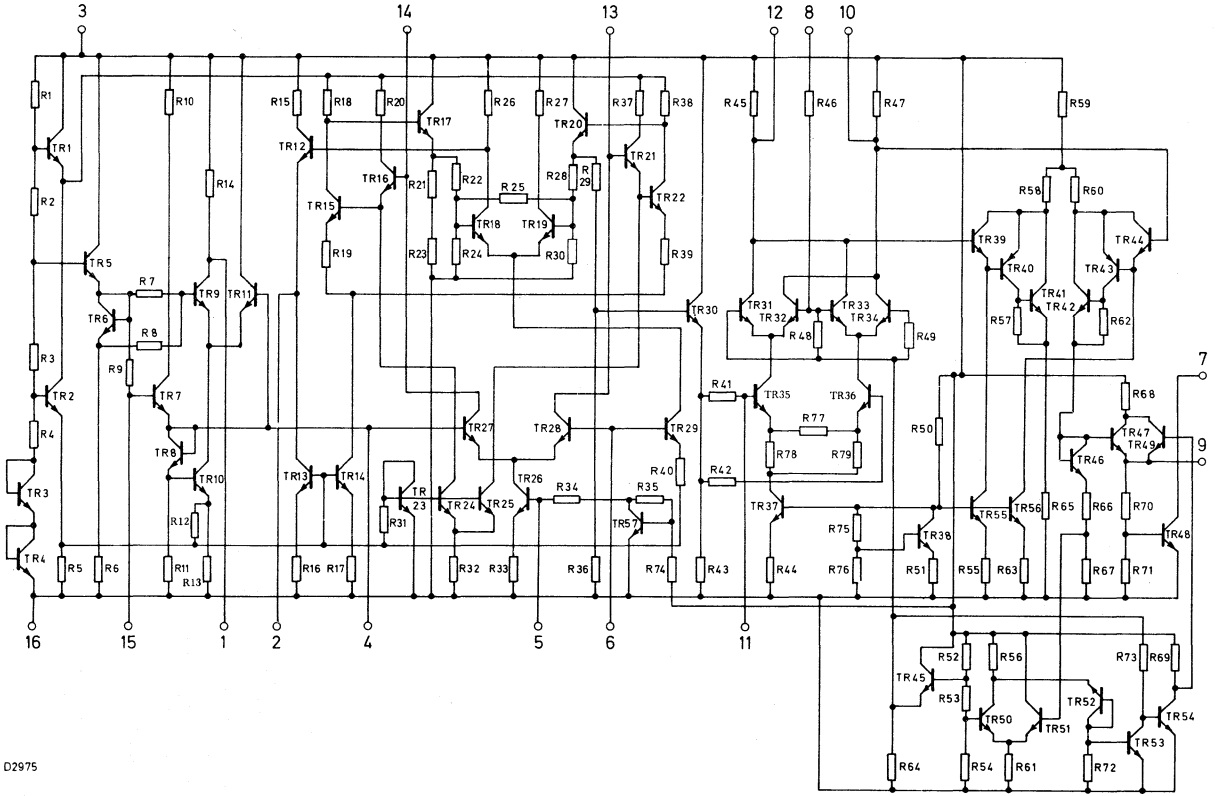
The TBA540 is an integrated reference oscillator circuit for colour television receivers incorporating an automatic phase and amplitude controlled oscillator employing a quartz crystal, together with a half-line frequency synchronous demodulator circuit. The latter compares the phases and amplitude of the swinging burst ripple and the PAL flip-flop waveform, and generates appropriate a.c.c., colour killer and identification signals. The use of synchronous demodulation for these functions permits a high standard of noise immunity.

QUICK REFERENCE DATA				
Supply voltage	V_{3-16}	nom.	12	V
Total current drain	I_3	typ.	33	mA
R-Y reference signal output peak-to-peak value	$V_{4-16(p-p)}$	typ.	1,3	V
Colour killer output: colour on	V_{7-16}	typ.	12	V
colour off	V_{7-16}	<	250	mV
A.C.C. output voltage range at correct phase of PAL switch	V_{9-16}		+4 to +0,2	V
at incorrect phase of PAL switch	V_{9-16}		+4 to +11	V

PACKAGE OUTLINES

TBA540 : 16-lead DIL; plastic (SOT-38).

CIRCUIT DIAGRAM



RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltage				
Supply voltage	V_{3-16}	max.	13.2	V
Power dissipation				
Total power dissipation at T_{amb} = 50 °C	P_{tot}	max.	680	mW
Temperatures				
Storage temperature	T_{stg}		−55 to +125	°C
Operating ambient temperature	T_{amb}		−20 to +60	°C

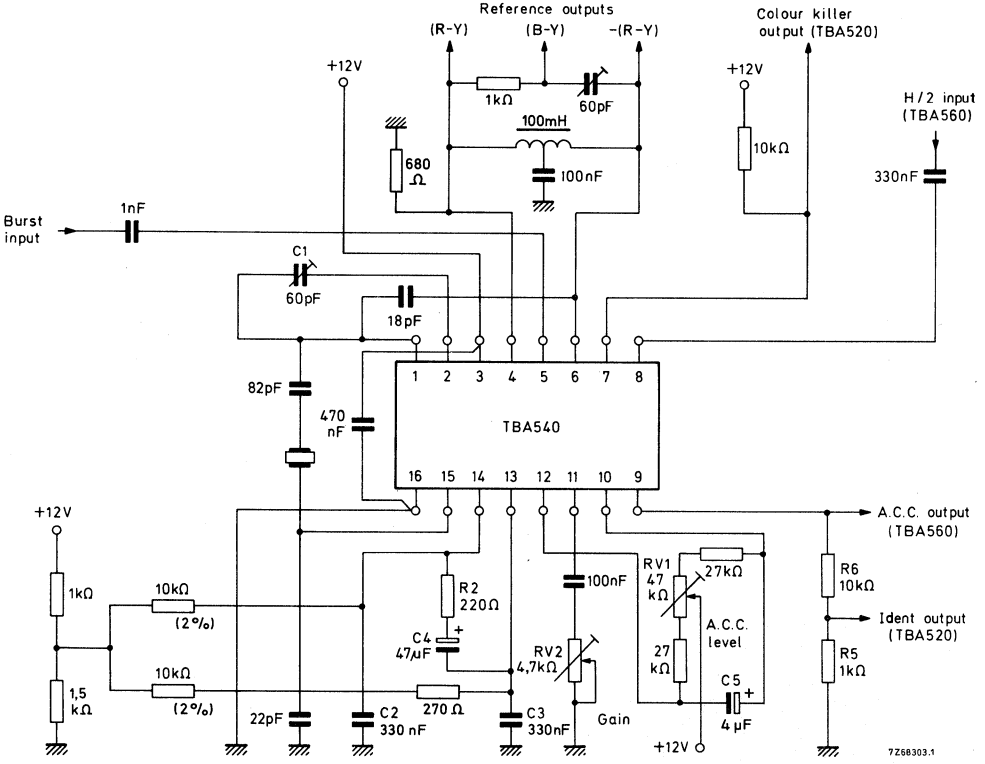
CHARACTERISTICS at V_{3-16} = 12 V; T_{amb} = 25 °C; $V_{5-16\,M}$ = 0.7 V (burst signal input); $V_{8-16(p-p)}$ = 2.5 V (P.A.L. square wave input) Measured in circuit shown on page 4.

Output signals				
R-Y reference signal output peak-to-peak value	$V_{4-16(p-p)}$	typ.	1.5	V
Colour killer output: colour on	V_{7-16}	typ.	12	V
colour off	V_{7-16}	<	250	mV
A.C.C. output signal range				
at correct phase of P.A.L. switch	V_{9-16}		+4 to +0.2	V
at incorrect phase of P.A.L. switch	V_{9-16}		+4 to +11	V
Oscillator section (amplifier)				
Input resistance	R_{15-16}	typ.	3.5	kΩ
Input capacitance	C_{15-16}	typ.	5	pF
Voltage gain	G_{15-1}	typ.	4.7	
Reactance control section				
Voltage gain with pins 13 and 14 interconnected	G_{15-2}	typ.	1.3	
Rate of change of gain G_{15-2} with phase difference between burst and reference signal	$\frac{\Delta G_{15-2}}{\Delta \varphi_{5-4}}$	typ.	5	$\frac{1}{\text{rad}}$
Supply current consumption	I_3	typ.	33	mA

PINNING

1. Oscillator feedback output
2. Reactance control stage feedback
3. Supply voltage (12 V)
4. Reference waveform output
5. Burst waveform input
6. Reference waveform input
7. Colour killer output
8. P.A.L. flip-flop square wave input
9. A.C.C. output
10. A.C.C. level setting (see also pin 12)
11. A.C.C. gain setting
12. A.C.C. level setting (see also pin 10)
13. D.C. control points for
14. oscillator phase control loop
15. Oscillator feedback input
16. Earth (negative supply)

APPLICATION INFORMATION



APPLICATION INFORMATION (continued)

The function is quoted against the corresponding pin number

1. Oscillator feedback output
   The crystal receives its energy from this pin. The input impedance is approximately 2 kΩ in parallel with 5 pF.

2. Reactance control stage feedback
   This pin is fed internally with a sinewave derived from the reference input (pin 6) and controlled in amplitude by the internal reactance control circuit. The phase of the feedback from pin 2 to the crystal via C1 is such that the value of C1 is effectively increased. Pin 2 is held internally at a very low impedance therefore the tuning of the crystal is controlled automatically by the amplitude of the feedback waveform and its influence on the effective value of C1.

3. Positive 12 V supply
   The maximum voltage must not exceed 13.2 V.

4. Reference waveform output
   This pin is driven internally by the regenerated subcarrier waveform in R-Y phase. An output amplitude of nominally 1.5 V peak-to-peak is produced at low impedance. No d.c. load to earth is required. A d.c. connection between pins 4 and 6 is, however, necessary via the bifilar coupling inductor. The function of this inductor is to produce, on pin 6, a signal of equal amplitude and opposite phase (-(R-Y)) to that on pin 4. A centre tap on the inductor, connected to earth via a d.c. blocking capacitor, is therefore necessary.

5. Burst waveform input
   A burst waveform amplitude of 1 V peak-to-peak is required to be a.c.-coupled to this pin. The amplitude of the burst will normally be controlled by the adjustment and operation of the a.c.c. circuit. The input impedance at this pin is approximately 1 kΩ and a threshold level of 0.7 V must be exceeded before the burst signal becomes effective. A d.c. bias of 400 mV is internally derived for pin 5 The absolute level of the tip of the burst at pin 5 will normally reach 1.25 V (1.5 V peak-to-peak burst amplitude). Under abnormal conditions the burst amplitude should not be allowed to exceed 3 V peak-to-peak and a limiting condition will be reached in the i.c. which inhibits the performance of the phase lock loop.

APPLICATION INFORMATION (continued)

6. Reference waveform input
This pin requires a reference waveform in the -(R-Y) phase, derived from pin 4 via a bifilar transformer (see pin 4), to drive the internal balanced reactance control stage. A d.c. connection between pins 4 and 6 must be made via the transformer.

7. Colour killer output
This pin is driven from the collector of an internal switching transistor and requires an external load resistor (typical 10 kΩ) connected to +12 V. The unkilled and killed voltages on this pin are then +12 V and < 250 mV respectively. (The voltage on pin 9 at which switching of the colour killer output on pin 7 occurs is nominally +2.5 V

8. P.A.L. flip-flop square wave input
A 2.5 V peak-to-peak square wave derived from the P.A.L. flip-flop (in the TBA520 demodulator i.c.) is required at this pin, a.c.-coupled via a capacitor. The input impedance is about 3.3 kΩ.

9. A.C.C. output
An emitter follower provides a low impedance output potential which is negative-going with a rising burst input amplitude. With zero input signal the d.c. potential produced at pin 9 is set to be +4 V (RV1). The appearance of a burst signal on pin 5 will cause the potential on pin 9 to go in a negative direction in the event that the P.A.L. flip-flop is identified to be in the correct phase. The range of potential over which full a.c.c. control is excercised at pin 9 is determined by the control characteristics of the a.c.c. amplifier i.e. for the TBA560 from 1 V to 0.2 V. The potential at pin 9 will fall to a value within this range as the burst input signal is stabilised at 1.5 V peak-to-peak. The latter condition is achieved by correct adjustment of RV2. If, however, the P.A.L. flip-flop phase is wrong the potential on pin 9 will move positively. The potential divider R5, R6 will then operate a P.A.L. switch cut-off function in the TBA520 demodulator i.c. The switching of the colour killer output at pin 7 is designed to occur as the potential on pin 9 moves past +2.5 V.

10. A.C.C. level setting
The network connected between pins 10 and 12 balances the a.c.c. circuit and RV1 is adjusted to give +4 V on pin 9 with no burst input signal to pin 5. C5 provides filtering.

11. A.C.C. gain control
RV2 is adjusted to give the correct amplitude of burst signal on pin 5 (1.5 V peak-to-peak) under a.c.c. control;

12. See pin 10.

13. See pin 14.

APPLICATION INFORMATION (continued)

14. D.C. control points in reference control loop
Pins 13 and 14 are connected to opposite sides of a differential amplifier circuit and are brought out for the purposes d.c. balancing of the reactance stage and the connection of the bandwidth-determining filter network. The conventional double time constant filter networks are R2, C2, R3, C3 and R_4, C_4. The d.c. potentials on these pins are nominally +7,2 V.

15. Oscillator feedback input
The input impedance at this pin is nominally 3.5 kΩ in parallel with 5 pF. No d.c. connection is required on this pin. The voltage in the i.c. between pin 15 and pin 1 is nominally 4.7 times.

16. Negative supply (earth)

PERFORMANCE AND COMMENTS

Initial adjustment

(a) Remove burst signal.

(b) Short-circuit pins 13-14. Adjust oscillator to correct frequency by C1. Remove short circuit.

(c) Set the a.c.c. level adjustment RV1, to give +4 V on pin 9.

(d) Apply burst signal.

(e) Adjust a.c.c. gain, RV2, to give a burst amplitude of 1.5 V peak-to-peak on pin 5.

Phase lock loop performance (with crystal type 4322 152 0110)

(a) Phase difference between reference and burst signals for ±400 Hz deviation of crystal frequency, ± 10°.

(b) Typical holding range, ± 600 Hz.

(c) Typical pull-in range, ± 300 Hz.

(d) Temperature coefficient of oscillator frequency, i.c. only, 2 Hz/°C.

LIMITER/AMPLIFIER

The TBA750C is a limiter/amplifier with f.m. detector, d.c. volume control and a.f. preamplifier. It is intended for 4,5 MHz, 5,5 MHz or 10,7 MHz. The limiter/amplifier is a four-stage differential amplifier that gives very good noise and interference suppression. The detector is of the balanced type. The d.c. volume control stage has excellent control characteristics with a control range of more than 80 dB. The a.f. preamplifier can drive a triode-pentode output stage or a class-A push-pull transistor output stage.

QUICK REFERENCE DATA

Supply voltage	V_{2-5}	typ	12 V
Total current drain	I_{tot}	typ	34 mA
Frequency	f_o		5,5 MHz
Input voltage at start of limiting	$V_{i\ lim}$	typ	130 μV
A.M. rejection at V_i = 1 mV	α	typ	45 dB
A.F. output voltage at $\Delta f = \pm 15$ kHz at pin 16	$V_{o(rms)}$	typ	2,7 V
D.C. volume control range		>	80 dB

PACKAGES OUTLINES

TBA750C: 16-lead DIL; plastic (SOT-38).
TBA750CQ: 16-lead QIL; plastic (SOT-58).

CIRCUIT DIAGRAM

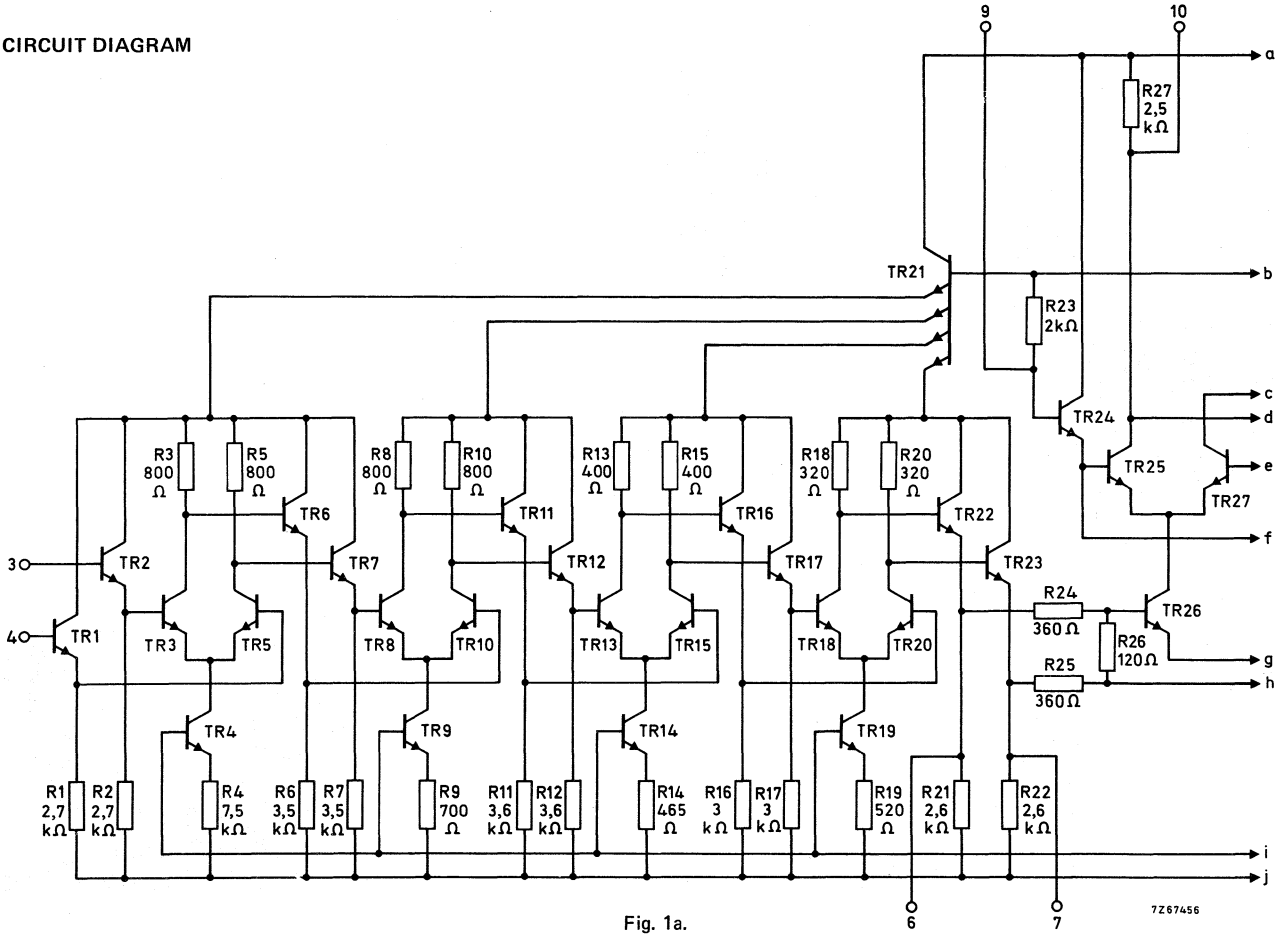


Fig. 1a.

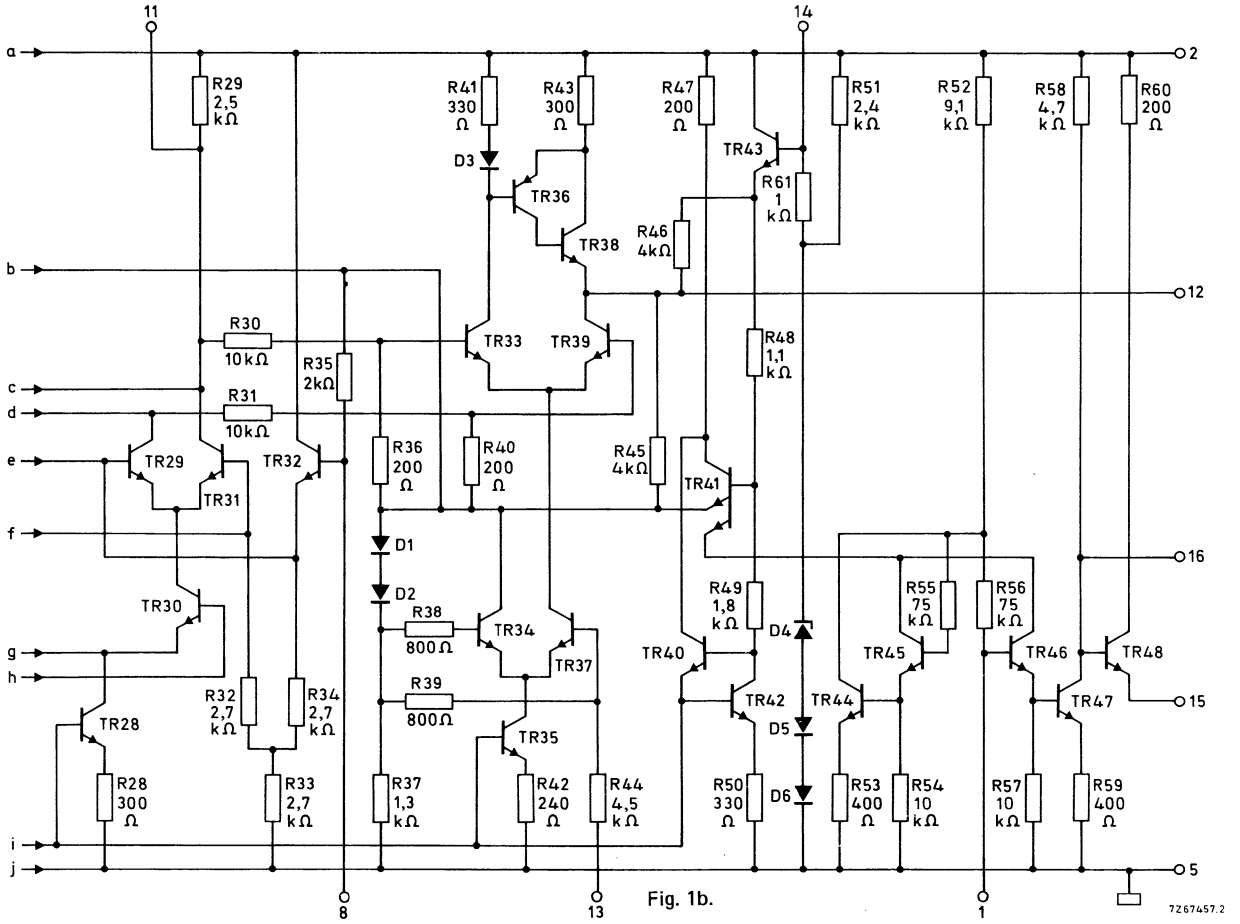

11
14
a
b
c
d
e
f
g
h
i
j
2
12
16
15
5
8
13
1
R29 2,5 kΩ
R41 330 Ω
R43 300 Ω
R47 200 Ω
R51 2,4 kΩ
R52 9,1 kΩ
R58 4,7 kΩ
R60 200 Ω
D3
TR36
TR38
TR43
R61 1 kΩ
R46 4kΩ
R30 10kΩ
R31 10kΩ
R35 2kΩ
TR33
TR39
R48 1,1 kΩ
TR29
TR31
TR32
R36 200 Ω
R40 200 Ω
R45 4kΩ
TR41
D1
D2
TR30
R38 800Ω
TR34
TR37
R49 1,8 kΩ
D4
R55 75 kΩ
R56 75 kΩ
TR40
TR45
TR46
TR48
R39 800Ω
TR42
TR44
TR47
D5
D6
TR28
R32 2,7 kΩ
R34 2,7 kΩ
TR35
R28 300 Ω
R33 2,7 kΩ
R37 1,3 kΩ
R42 240 Ω
R44 4,5 kΩ
R50 330 Ω
R53 400 Ω
R54 10 kΩ
R57 10 kΩ
R59 400 Ω
7Z67457.2

Fig. 1b.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_{2-5}	max	16 V *
Storage temperature	T_{stg}	−55 to + 125	°C
Operating ambient temperature	T_{amb}	−25 to + 55	°C
Power dissipation			

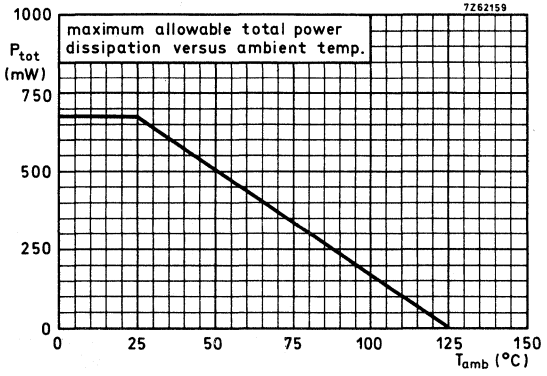


Fig. 2.

CHARACTERISTICS

Measured in test circuit Fig. 3.

Supply voltage range see also Fig. 4	V_{2-5}		10 to 25 V
Total current drain; pin 15 not connected	I_2		25 to 45 mA
Input limiting voltage at V_o = −3 dB (r.m.s. value)	$V_{i\ lim(rms)}$	typ	130 μV
I.F. output voltage at pins 6 and 7 (peak-to-peak value)	$V_{6-5(p-p)}$ / $V_{7-5(p-p)}$	typ	380 mV
A.M. rejection			
V_i = 1 mV	α	typ	45 dB
V_i = 10 mV	α	typ	50 dB
V_i = 100 mV	α	typ	55 dB
D.C. volume control range; see also Fig. 5		>	80 dB
A.F. preamplifier voltage gain pin 1 to pin 16	G_v	typ	10
Input resistance at pin 1	R_i	⩾	35 kΩ

* Allowable only if the dissipation in the IC is limited by means of a series resistor in the supply (see also Fig. 4).

CHARACTERISTICS (continued)

A.F. output voltages (r.m.s. values) $\Delta f = \pm 15$ kHz; $f_m = 1$ kHz	$V_{10-5(rms)}$ } $V_{11-5(rms)}$ }	typ	65 mV
	$V_{12-5(rms)}$	typ	250 mV
	$V_{16-5(rms)}$	typ	2,7 V
Total harmonic distortion			
at pin 12; $\Delta f = 15$ kHz	d_{tot}	typ	3 %
at pin 1 with respect to pin 16; $V_{o(rms)} = 3$ V	d_{tot}	typ	2,6 %

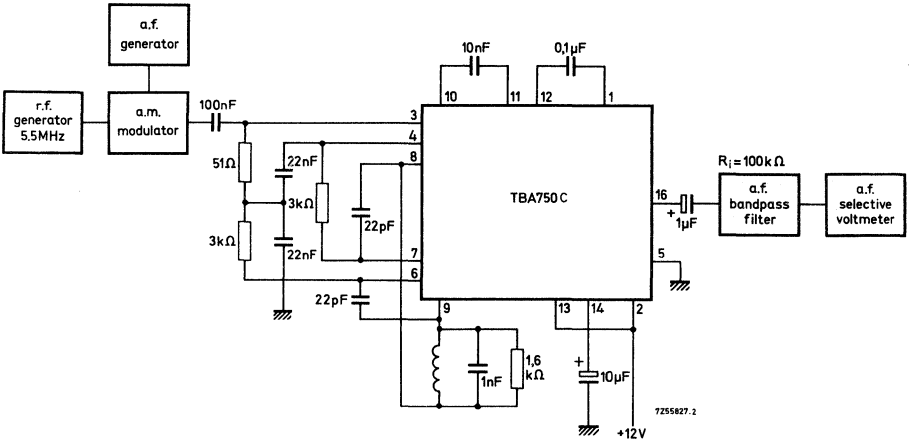


Fig.3 Test circuit; for f.m.: $f_o = 5,5$ MHz; $\Delta f = \pm 15$ kHz; $f_m = 70$ Hz.
For a.m.: $m = 0,3$; $f_m = 1$ kHz.

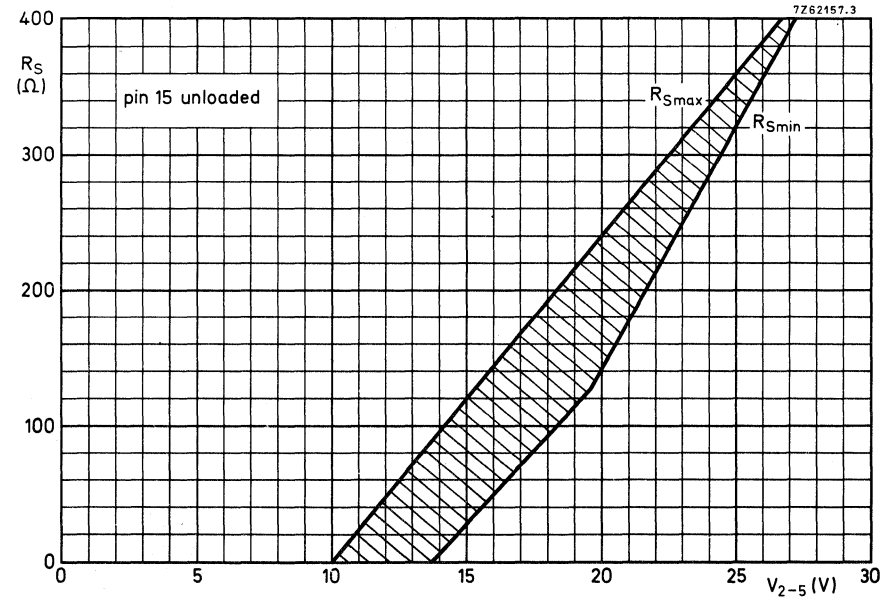


Fig. 4 Maximum and minimum values for the power supply series resistance (R_S).

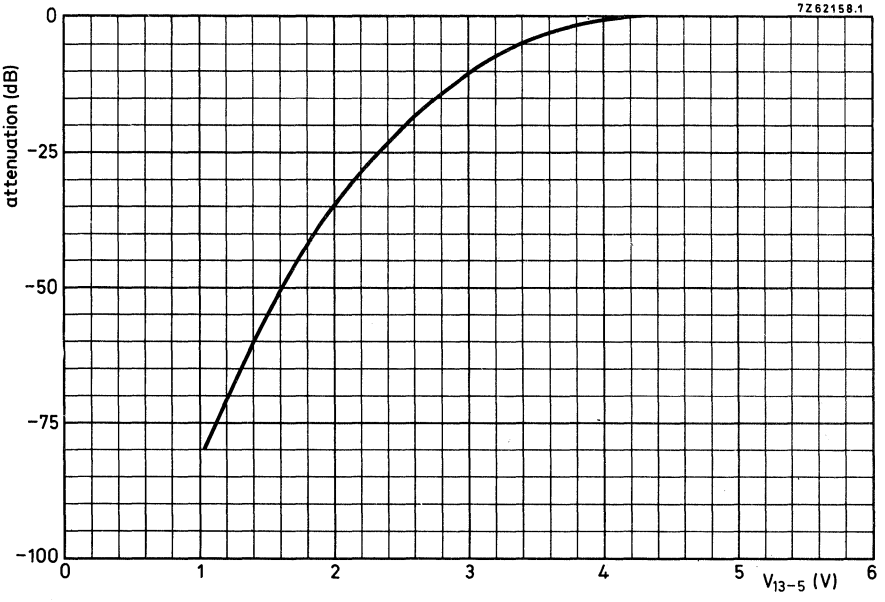


Fig. 5 Remote control characteristic.

APPLICATION INFORMATION at f = 5,5 MHz

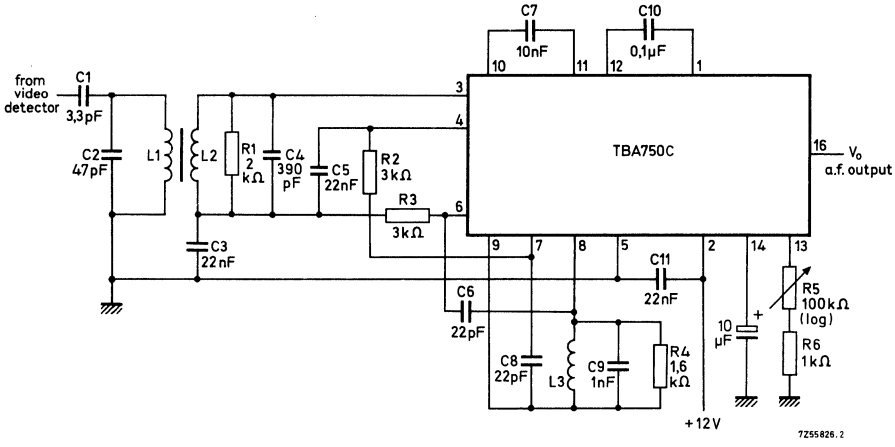


Fig. 6.

L1 = 18 μH; Q_{L1} = 36

L2 = 2,2 μH; Q_{L2} = 21

L3 = 0,84 μH; Q_{L3} = 22

Note

Q_{L1}, Q_{L2} and Q_{L3} are the loaded Q-factors.

The transfer ratio of the input bandpass filter: $\frac{V_2}{V_1} = 0{,}54$.

The peak-to-peak bandwidth of the detector S-curve is 300 kHz.

HORIZONTAL COMBINATION

The TBA920 is a monolithic integrated circuit intended for television receivers with transistor, thyristor, or tube-equipped output stages.
It combines the following functions:
- noise gated sync separator
- line oscillator
- phase comparison between sync pulse and oscillator
- loop gain and time constant switching (also for video recorder applications)
- phase comparison between line-flyback pulse and oscillator
- output stage for drive a variety of line output stages

QUICK REFERENCE DATA

Supply voltage	V_{1-16}	nom.	12 V
Ambient temperature	T_{amb}		25 °C
Input signals			
Video input voltage (positive-going sync) top sync to white value	$V_{8-16(p-p)}$	typ.	3 V 1 to 7 V
Noise gate input current (peak value)	I_{9M}	>	30 μA
Input resistance of noise gate	R_{9-16}	typ.	200 Ω
Flyback signal input voltage (peak value)	V_{5-16M}	typ.	±1 V
Flyback signal input current (peak value)	I_{5M}	typ.	1 mA
Output signals			
Line driver output voltage (peak-to-peak value)	$V_{2-16(p-p)}$	typ.	10 V
Line driver output current (average value)	$I_{2(AV)}$	max.	20 mA
Line driver output current (peak value)	I_{2M}	max.	200 mA
Composite sync output voltage (peak value)	V_{7-16M}	typ.	10 V

PACKAGE OUTLINE

16-lead dual in-line; plastic (SOT-38).

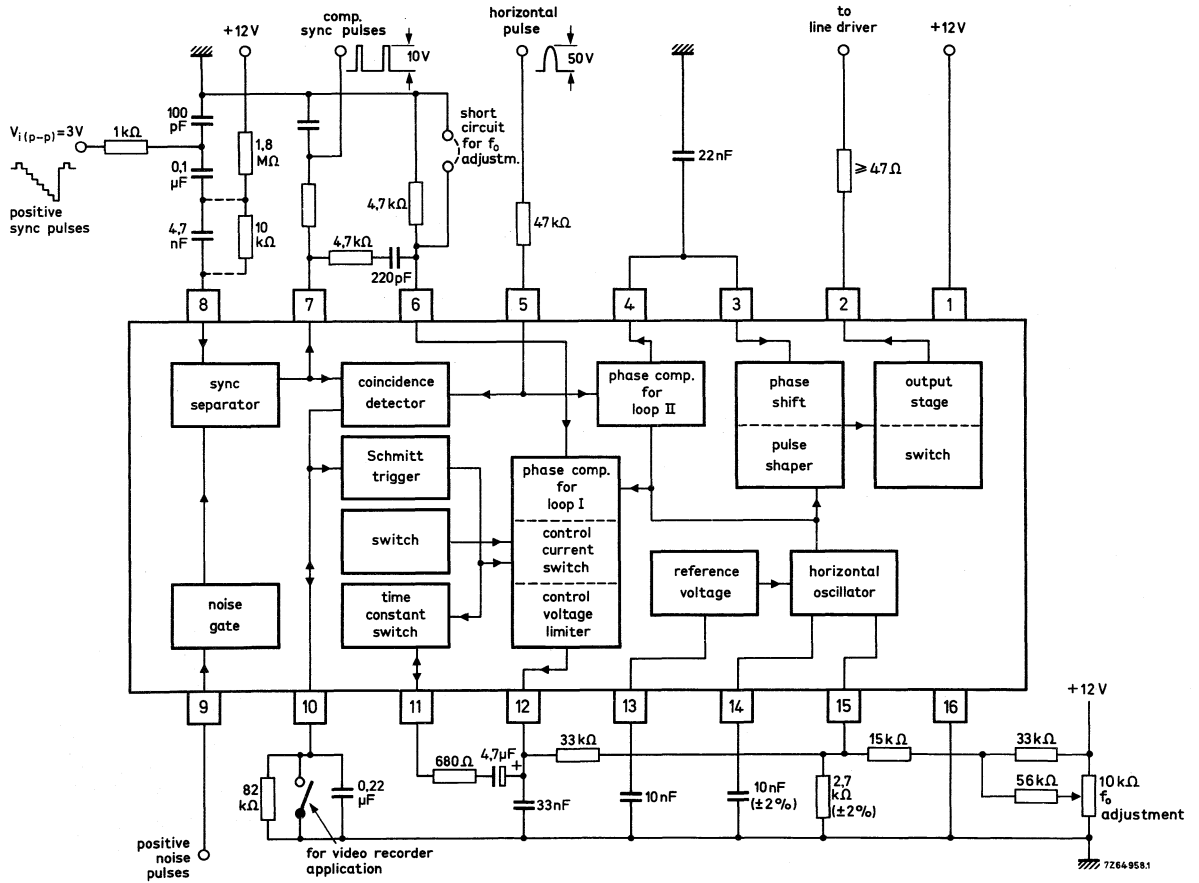


Fig. 1 Block diagram and application information.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (V_P)	$V_{1\text{-}16}$	max.	13,2	V
Phase shift voltage	$V_{3\text{-}16}$		0 to 13,2	V
Video input voltage	$-V_{8\text{-}16}$	max.	12	V
Coincidence detector voltage	$V_{10\text{-}16}$		−0,5 to +5	V
Line driver output current (average value)	$I_{2(AV)}$	max.	20	mA
(peak value)	I_{2M}	max.	200	mA
Horizontal pulse current (peak value)	I_{5M}	max.	10	mA
Composite sync current (peak value)	I_{7M}	max.	10	mA
Pos. sync pulse current (peak value)	I_{8M}	max.	10	mA
Noise gate current (peak value)	I_{9M}	max.	10	mA
Total power dissipation	P_{tot}	max.	600	mW*
Storage temperature	T_{stg}		−55 to +125	°C
Operating ambient temperature	T_{amb}		−20 to +60	°C

CHARACTERISTICS

At $V_{1\text{-}16}$ = 12 V; T_{amb} = 25 °C. Measured in circuit of Fig. 1 (CCIR standard).

Current consumption at $I_2 = 0$	I_1	typ.	36	mA
Required input signals				
Video signal				
Input voltage (positive going sync) peak-to-peak value	$V_{i(p\text{-}p)}$	typ.	3 1 to 7	V V
Input current during sync pulse (peak value)	I_{8M}	typ.	100	μA
Noise gating (pin 9)				
Input voltage (peak value)	$V_{9\text{-}16M}$	>	0,7	V
Input current (peak value)	I_{9M}	> <	30 10	μA mA
Input resistance	$R_{9\text{-}16}$	typ.	200	Ω
Flyback pulse (pin 5)				
Input voltage (peak value)	$V_{5\text{-}16M}$	typ.	±1	V
Input current (peak value)	I_{5M}	> typ.	50 1	μA mA
Input resistance	$R_{5\text{-}16}$	typ.	400	Ω
Pulse duration at 15 625 Hz	t_5	>	10	μs

* 800 mW permissible while tubes are heating up.

CHARACTERISTICS (continued)

Delivered output signals

Composite sync pulses (positive; pin 7)

Output voltage (peak-to-peak value)	$V_{7\text{-}16(p\text{-}p)}$	typ.	10 V
Output resistance			
at leading edge of pulse (emitter follower)	$R_{7\text{-}16}$	≈	50 Ω
at trailing edge	$R_{7\text{-}16}$	typ.	2,2 kΩ
Additional external load resistance	$R_{7\text{-}16(ext)}$	>	2 kΩ
Driver pulse (pin 2)			
Output voltage (peak-to-peak value)	$V_{2\text{-}16(p\text{-}p)}$	typ.	10 V
Average output current	$I_{2(AV)}$	<	20 mA
Peak output current	I_{2M}	<	200 mA
Output resistance (low ohmic)	$R_{2\text{-}16}$	typ.	2,5 or 15 Ω *
Output pulse duration when synchronized	t_2		12 to 32 μs **
Permissible delay between leading edge of output pulse and flyback pulse at t_5 = 12 μs	$t_{o\ tot}$		0 to 15 μs
Supply voltage at which output pulses are obtained	$V_{1\text{-}16}$	>	4 V

* Depends on switch position and polarity output current. $R_{2\text{-}16}$ = 2,5 Ω is valid for $V_{2\text{-}16}$ = +10,5 V and a load between pins 2 and 16 (e.g. an external resistor).

** The output pulse duration is adjusted by shifting the leading edge ($V_{3\text{-}16}$ from 6 V to 8 V). The pulse duration is a result of delay in the line output device and the action of the second control loop in the TBA920S.
For a line output stage with a BU108 high-voltage transistor the resulting duration is about 22 μs, and in such a way that the line output transistor is switched on again about 8 μs after the middle of the line-flyback pulse. This pulse duration must be taken into account when designing the driver stage and driver transformer as this way of driving the line output device differs from the usual, i.e. a driver duty cycle of about 50%.

Oscillator

Frequency; free running ($R_{15\text{-}16}$ = 3,3 kΩ)	f_o		15 625 Hz	*
Spread of frequency at $R_{15\text{-}16}$ = 3,3 kΩ; $C_{14\text{-}16}$ = 10 nF	$\frac{\Delta f_o}{f_o}$	<	1,5 %	**
Frequency change when decreasing the supply down to minimum 4 V	$\left\lvert\frac{\Delta f_o}{f_o}\right\rvert$	<	10 %	
Frequency control sensitivity	$\frac{\Delta f_o}{\Delta I_{15}}$	typ.	16,5 Hz/μA	
Adjustment range of frequency (in Fig. 2)	$\frac{\Delta f_o}{f_o}$	typ.	±5 %	
Influence of supply voltage on frequency at V_P = 12 V	$\frac{\delta f_o}{f_o} / \frac{\delta V_P}{V_{Pnom}}$	<	5 %	

Control loop 1 (between sync pulse and oscillator)

Control voltage range	$V_{12\text{-}16}$		0,8 to 5,5 V	
Control current (peak values)				
at $V_{10\text{-}16} > 4{,}5$ V; $V_{6\text{-}16} > 1{,}5$ V	I_{12M}	typ.	±2 mA	
at $V_{10\text{-}16} < 2$ V; $V_{6\text{-}16} > 1{,}5$ V	I_{12M}	typ.	±6 mA	
Loopgain of APC system				
a. Time coincidence between sync pulse and flyback pulse or $V_{10\text{-}16} > 4{,}5$ V	$\frac{\Delta f}{\Delta t}$	typ.	1 kHz/μs	
b. No time coincidence or $V_{10\text{-}16} < 2$ V	$\frac{\Delta f}{\Delta t}$	typ.	3 kHz/μs	
Catching and holding range	Δf	typ.	±1 kHz	▲

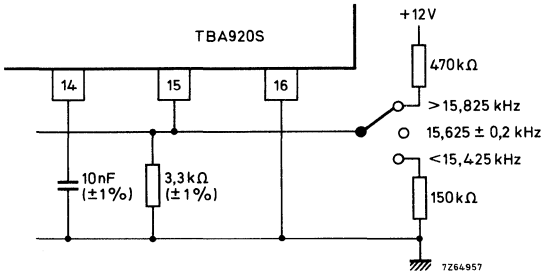


Fig. 2 Possibilities for oscillator frequency adjustment.

* The oscillator frequency can be changed for other TV standards by an appropriate value of $C_{14\text{-}16}$.

** Exclusive external components tolerances.

▲ Adjustable with $R_{12\text{-}15}$.

CHARACTERISTICS (continued)

Pull-in time for $\Delta f/f_o = \pm 3\% (\Delta f = 470$ Hz)	t	≈	20	ms	(note 1)
Switch-over from large control sensitivity to small control sensitivity after catching	t	≈	20	ms	(note 1)
Control loop II (between flyback pulse and oscillator)					
Permissible delay between leading edge of output pulse (pin 2) and leading edge of flyback pulse	$t_{d\,tot}$		0 to 15	μs	
Static control error	$\frac{\Delta t}{\Delta t_d}$	<	0,5	%	(note 2)
Output current during flyback pulse (peak value)	I_{4M}	typ.	±0,7	mA	
Overall phase relation					
Phase relation between leading edge of sync pulse and middle of flyback pulse	t	typ.	4,9	μs	(note 3)
Tolerance of phase relation	$\lvert\Delta t\rvert$	<	0,4	μs	(note 4)
Voltage for T_2 = 12 to 32 μs	$V_{3\text{-}16}$		6 to 8	V	
Adjustment sensitivity	$\frac{\Delta T_2}{\Delta V_{3\text{-}16}}$	typ.	10	μs/V	
Input current	I_3	<	2	μA	
External switch-over of parameters (loop filter and loop gain) of control loop I (e.g. for video recorder application) see note 5.					
Required switch-over voltage					
at $R_{11\text{-}16}$ = 150 Ω	$V_{10\text{-}16}$	>	4,5	V	
at $R_{11\text{-}16}$ = 2 kΩ	$V_{10\text{-}16}$	<	2	V	
Required switch-over current					
at $R_{11\text{-}16}$ = 150 Ω; $V_{10\text{-}16}$ = 4,5 V	I_{10}	typ.	80	μA	(note 5)
at $R_{11\text{-}16}$ = 2 kΩ; $V_{10\text{-}16}$ = 2 V	I_{10}	typ.	120	μA	

1. See Fig. 1.
2. The control error is the remaining error in reference to the nominal phase position between leading edge of the sync pulse and the middle of the flyback pulse caused by a variation in delay of the line output stage.
3. This phase relation assumes a luminance delay line with a delay of 500 ns between the input of the sync separator and the drive to the picuture tube. If the sync separator is inserted after the luminance delay line or if there is no delay line at all (black-and-white sets), then the phase relation is achieved at $C_{5\text{-}16}$ = 560 pF.
4. The adjustment of the overall phase relation and consequently the leading edge of the output pulse at pin 2 occurs automatically by the control loop II or by applying a d.c. voltage to pin 3.
5. With sync pulses at pin 7 and 8; without RC network at pin 10.

CHROMINANCE AMPLIFIER FOR SECAM OR PAL/SECAM DECODERS

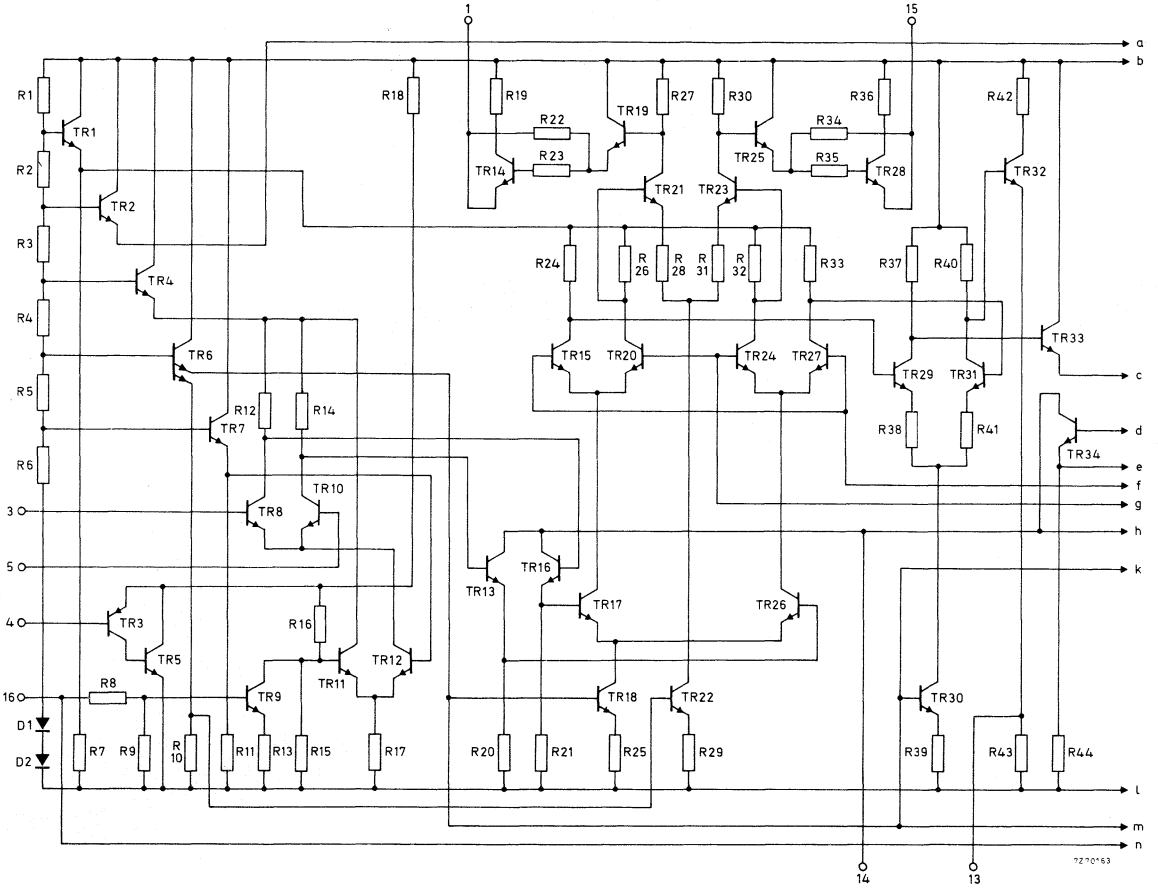
The TCA640 is an integrated chrominance amplifier for either a SECAM decoder or a double standard PAL/SECAM decoder.
Switching of the standard is performed internally, controlled by an external applied d.c. signal.
In addition to the chrominance amplifier the circuit also incorporates a 7,8 kHz flip-flop and an identification circuit for SECAM.
For PAL identification the circuit included in the TBA540 should be used.
Furthermore, the TCA640 incorporates a blanking circuit, a burst gating circuit and a colour killer detector.

QUICK REFERENCE DATA

Supply voltage	V_{14-2}	nom.	12	V	
Supply current	I_{14}	nom.	37	mA	
		PAL		SECAM	
Chrominance input signals (peak-to-peak value)	$V_{3-5(p-p)}$	>	4	7	mV
		<	80	400	mV
Chrominance output signals (peak-to-peak value)	$V_{15-2\ (p-p)}$ / $V_{1-2\ (p-p)}$	typ.	500	2000	mV
Burst output (closed a.c.c. loop) (peak-to-peak value)	$V_{13-2(p-p)}$	typ.	1	-	V
System switching signal	V_{4-2}	typ.	12	0	V
Burst blanking of chrominance signal		>	40	-	dB
Chrominance blanking at field identification		>	-	40	dB
Square-wave output (7,8 kHz) (peak-to-peak value)	$V_{12-2(p-p)}$	typ.	3	3	V

PACKAGE OUTLINE

16-lead DIL; plastic (SOT-38).


1
15
a
b
R1
R2
R3
R4
R5
R6
3
5
4
16
D1
D2
TR1
TR2
TR4
TR6
R12
TR7
R14
TR10
TR8
TR3
TR5
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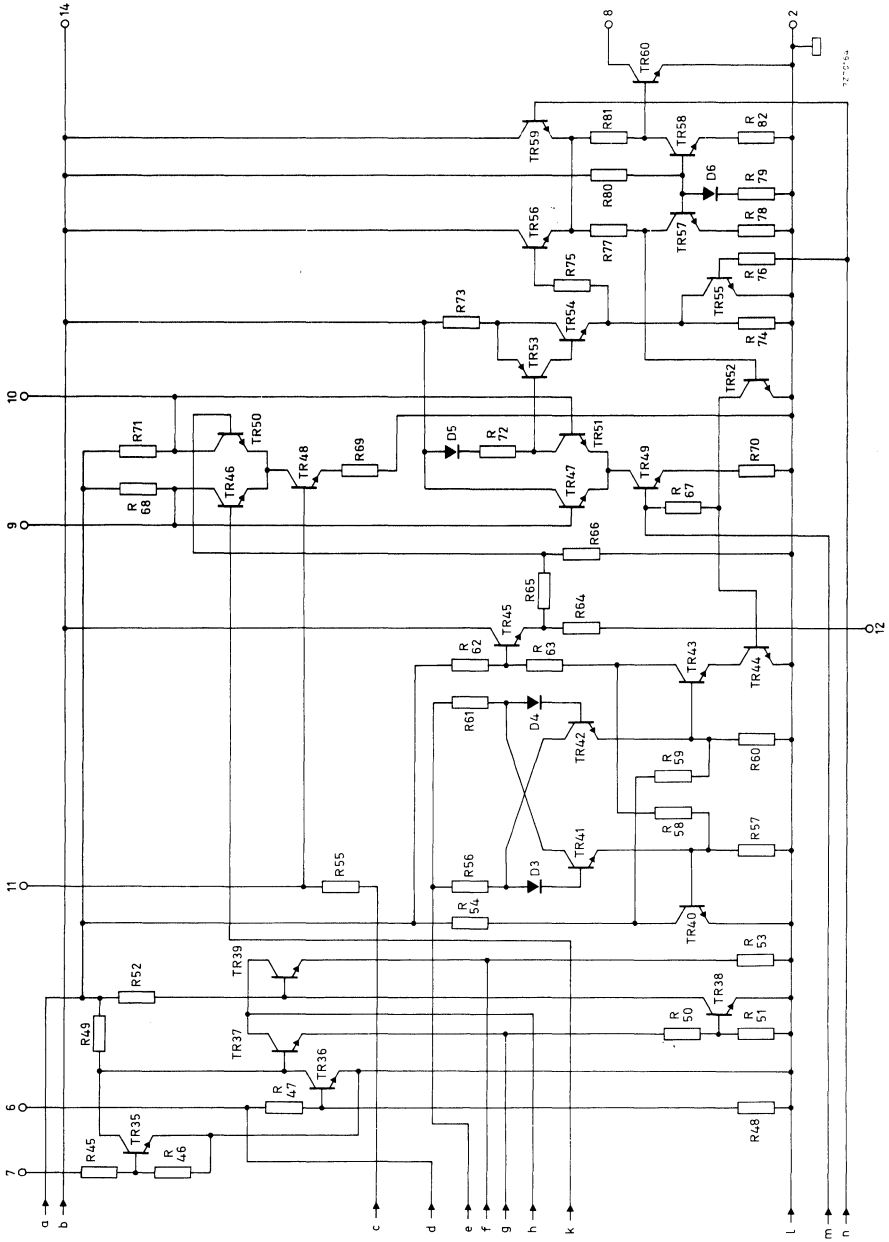
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RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltage			
Supply voltage	V_{14-2}	max.	13,2 V
Power dissipation			
Total power dissipation	P_{tot}	max.	625 mW
Temperatures			
Storage temperature	T_{stg}		−25 to +125 °C
Operating ambient temperature	T_{amb}		−25 to +65 °C [1]

CHARACTERISTICS measured in the circuit on page 6

Supply voltage	V_{14-2}	typ.	12 V
			10,2 to 13,2 V

Required input signals at V_{14-2} = 12 V and T_{amb} = 25 °C

Chrominance input signal			
peak-to-peak value	$V_{3-5(p-p)}$	PAL	4 to 80 mV
		SECAM	7 [2] to 400 mV
Automatic chrominance control starting	V_{16-2}	PAL	typ. 1,2 V [3]
Flyback pulses for blanking and burst/identification lines-keying			See note 4
Line flyback pulses (positive)			
peak-to-peak value	$V_{6-2(p-p)}$		4,5 to 12 V
Field idenfication pulses (positive)			
peak-to-peak value	$V_{7-2(p-p)}$		4 to 12 V
System switch signal	V_{4-2}	PAL	7 to V_{14-2} V
		SECAM	0 to 1 V
Colour killer threshold	V_{16-2}	PAL	typ. 2,5 V [5]

[1]) When a stabilized power supply of ⩽ 12 V is applied, T_{amb} is max. 75 °C.

[2]) Start of limiting.

[3]) A negative-going potential provides a 26 dB a.c.c. range.

[4]) The line flyback pulses also provide the clock pulses for the flip-flop.

[5]) The colour killer is operative above the quoted input voltage.

CHARACTERISTICS (continued)

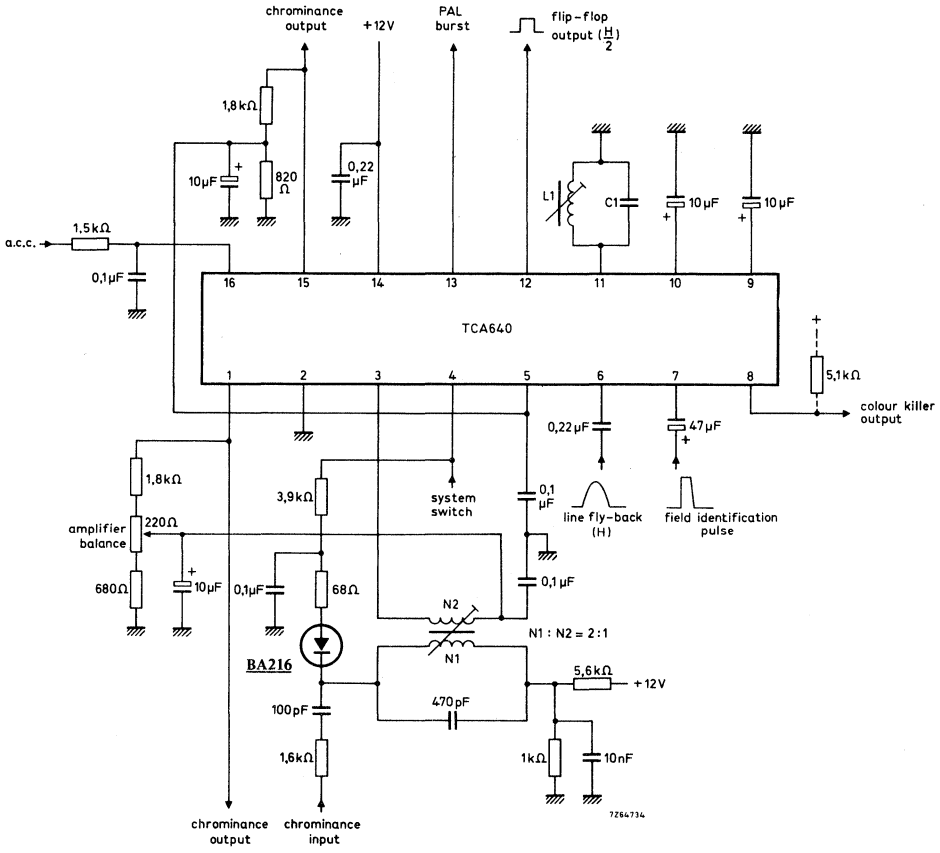
Obtainable output signals

Chrominance output signals						
peak-to-peak value		$V_{15-2(p-p)}$	PAL		425 to 575	mV
		$V_{1-2(p-p)}$	SECAM		1,8 to 2,3	V
Phase difference between output pins		$\Delta\varphi_{15-1}$	PAL		170° to 190°	[1]
Burst signal (peak-to-peak value)		$V_{13-2(p-p)}$	PAL	typ.	1	[2]
Identification signal						
peak-to-peak value		$I_{11(p-p)}$	SECAM		1,4 to 2,4	mA
Output resistance		R_{11-2}			2 to 2,9	kΩ
Flip-flop signal						
peak-to-peak value		$V_{12-2(p-p)}$			2,5 to 3,5	V
Colour killer	killed	V_{8-2}		<	0,5	V
		I_8		<	10	mA
	unkilled	V_{8-2}			V_{14-2}	V
		I_8		<	10	μA
Bandwidth of chrominance amplifier (−1 dB)						
at a carrier frequency of 4,2 MHz				>	± 1	MHz
Blanking						
burst rejection			PAL	>	40	dB
rejection identification lines with field identification			SECAM	>	40	dB

[1]) Over the a.c.c. control range the phase difference varies less than 2,5°.

[2]) The burst is kept constant at 1 V peak-to-peak by automatic gain control.

APPLICATION INFORMATION



Pinning

1. Chrominance output
2. Earth (negative supply)
3. Chrominance input
4. System switch input
5. Chrominance input
6. Line fly-back pulse input
7. Field identification pulse input
8. Colour killer output
9. Identification integrating capacitor (SECAM)
10. Identification integrating capacitor (SECAM)
11. Identification tank circuit (SECAM)
12. Flip-flop output
13. Burst output (PAL)
14. Supply voltage (12 V)
15. Chrominance output
16. A.C.C. input

APPLICATION INFORMATION (continued)

The function is quoted against the corresponding pin number

1. Chrominance output (in conjunction with pin 15)

   A balanced output is available at pins 1 and 15.
   At SECAM reception a limited signal of 2 V peak-to-peak is available, starting from an input voltage of 15 mV peak-to-peak.
   At PAL reception the output signal is 500 mV peak-to-peak for a burst signal of 1 V peak-to-peak.
   An external d.c. network is required which provides negative feedback to pin 3. The same holds for the feedback from pin 15 to pin 5.
   The figures for input and output signals are based on a 100% saturated colour bar signal.

2. Negative supply (earth)

3. Chrominance input (in conjunction with pin 5)

   The input signal is derived from a bandpass filter which provides the required "bell" shape bandpass for the SECAM signal and a flat bandpass for the PAL signal.
   The input signal can be supplied either in a balanced mode or single ended. Both inputs (pins 3 and 5) require a d.c. potential of about 2,5 V obtained from a resistive divider connected to output pins 1 and 15. The figures for the input signals are based on a 100% saturated colour bar signal and a burst-to-chrominance ratio of 1:3 of the input signal (PAL).

4. System switch input

   Between 7 V and the supply voltage, the gain of the chrominance amplifier is controlled by the a.c.c. voltage at pin 16.
   The chrominance amplifier then provides linear amplification required for the PAL signal.
   Between 0 V and 1 V the chrominance amplifier operates as a limiter for the SECAM signal.

5. Chrominance input (see pin 3)

6. Line fly-back pulse input (in conjunction with pin 11)

   Positive going pulses provide

   - blanking of the chrominance signal at the outputs (pins 1 and 15).
   - burst gating for both PAL and SECAM.
     The carrier signal present during the second half of the back porch of the SECAM signal is gated. It provides line identification when the circuit L_1C_1 (see circuit on page 6) is tuned to 4,25 MHz (at C_1 = 470 pF).
   - trigger signal for the flip-flop.

7. Field identification pulse input (in conjunction with pin 11)

   Like the line fly-back pulses, positive going identification pulses provide blanking and burst gating.
   To operate the TCA640 on the identification lines (SECAM) in the field blanking period the circuit L_1C_1 (see circuit on page 6) should be tuned to 3,9 MHz and the capacitor C_1 should be increased to 1 nF. The field fly-back pulse should be shaped so that its amplitude exceeds 4 V during the identification lines.

APPLICATION INFORMATION (continued)

8. Colour killer output

   This pin is driven from the collector of an internal switching transistor and requires an external load resistor connected to the supply voltage. The killer is operative when the a.c.c. voltage exceeds the threshold, when the SECAM chrominance signal at the input is below the limiting level or when the flip-flop operates in the wrong phase.

9. Identification integrating capacitor (SECAM)

10. Identification integrating capacitor (SECAM)

11. Identification detector tank circuit (see pins 6 and 7)

12. Flip-flop output

    A square wave of 7,8 kHz with an amplitude of 3 V is available at this pin.
    An external load resistor is not required.

13. Burst output (PAL)

    A 1 V peak-to-peak burst (kept constant by the a.c.c. system) is produced here.

14. Supply voltage (12 V)

    Correct operation occurs within the range 10,2 to 13,2 V.
    The power dissipation must not exceed 625 mW at 65 °C ambient temperature.

15. Chrominance output (see pin 1)

16. A.C.C. input

    With the system switch input (pin 4) connected for PAL operation, a negative going potential gives a 26 dB range of a.c.c. starting at + 1,2 V
    During SECAM operation, the voltage at the input should not exceed + 0,5 V, otherwise the SECAM identification circuit and the colour killer become inoperative.

CHROMINANCE DEMODULATOR FOR SECAM OR PAL/SECAM DECODERS

The TCA650 is an integrated synchronous demodulator for both the SECAM and PAL chrominance signals.
Switching of the standard is performed internally, controlled by an external applied d.c. signal.
In addition to the synchronous demodulator, which delivers colour difference signals, the circuit also incorporates:

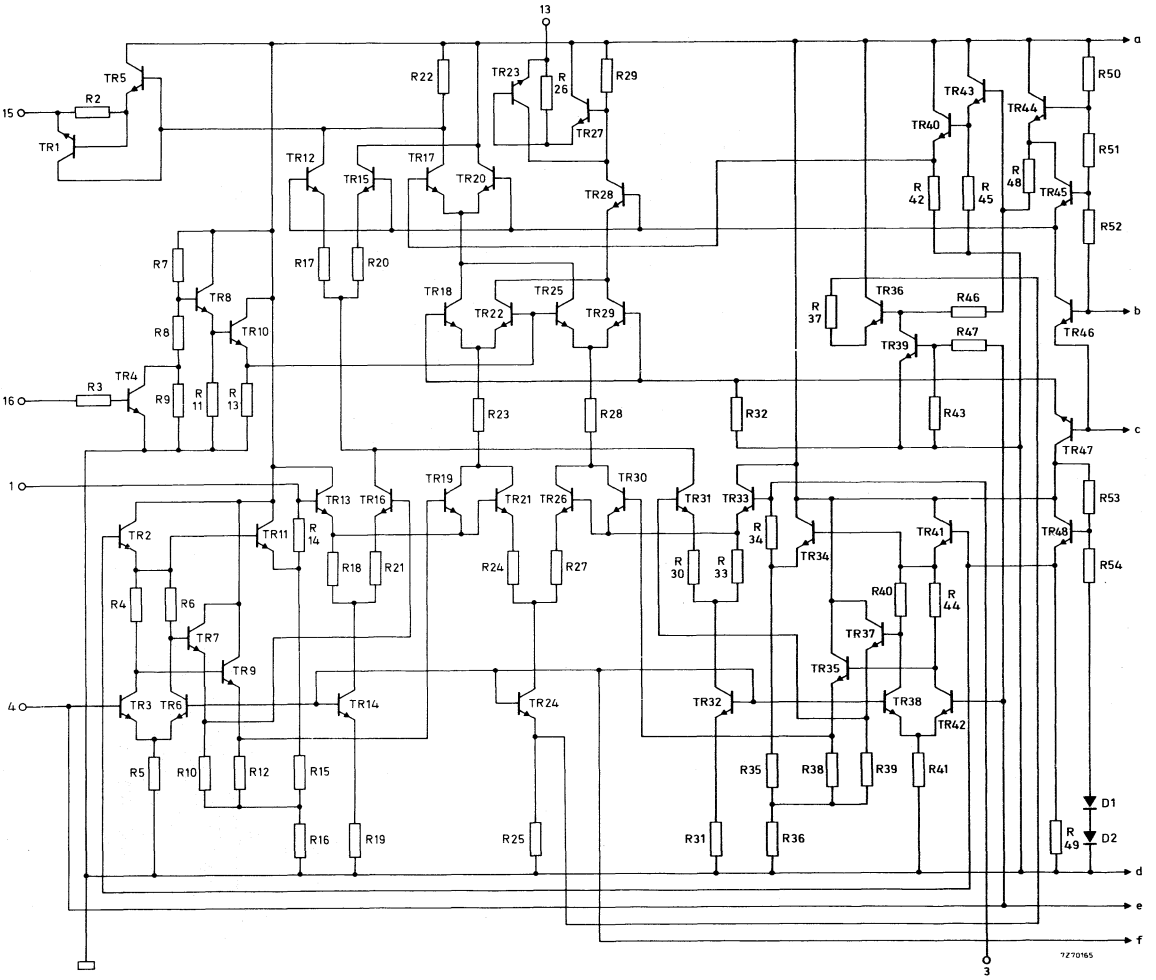
- a PAL matrix, used for adding the delayed and non-delayed signals to obtain separately the (R-Y) and (B-Y) components of the chrominance signal.
- a PAL switch, which reverses the phase of the (R-Y) component of the chrominance signal on alternating lines.
- a SECAM switch, which performs the separation of the D_R and D_B components of the chrominance signal by switching the delayed and non-delayed signals.
- a SECAM limiter.

QUICK REFERENCE DATA

				PAL	SECAM	
Supply voltage		V_{14-2}	nom.	12		V
Supply current		I_{14}	nom.	36		mA
Chrominance input signals (peak-to-peak value)	$V_{1-2(p-p)}$ / $V_{3-2(p-p)}$		typ.	50	200	mV
System switch input	V_{4-2}		typ.	12	0	V
Colour difference output signals (peak-to-peak value)	(R-Y):	$V_{12-2(p-p)}$	typ.	1,1		V
	(B-Y):	$V_{10-2(p-p)}$	typ.	1,47		V
Reference input signals (PAL) (peak-to-peak value)		$V_{6-2(p-p)}$ / $V_{7-2(p-p)}$	typ.	1		V
Square-wave input (peak-to-peak value)		$V_{16-2(p-p)}$	typ.	3		V

PACKAGE OUTLINE

16-lead DIL; plastic (SOT-38).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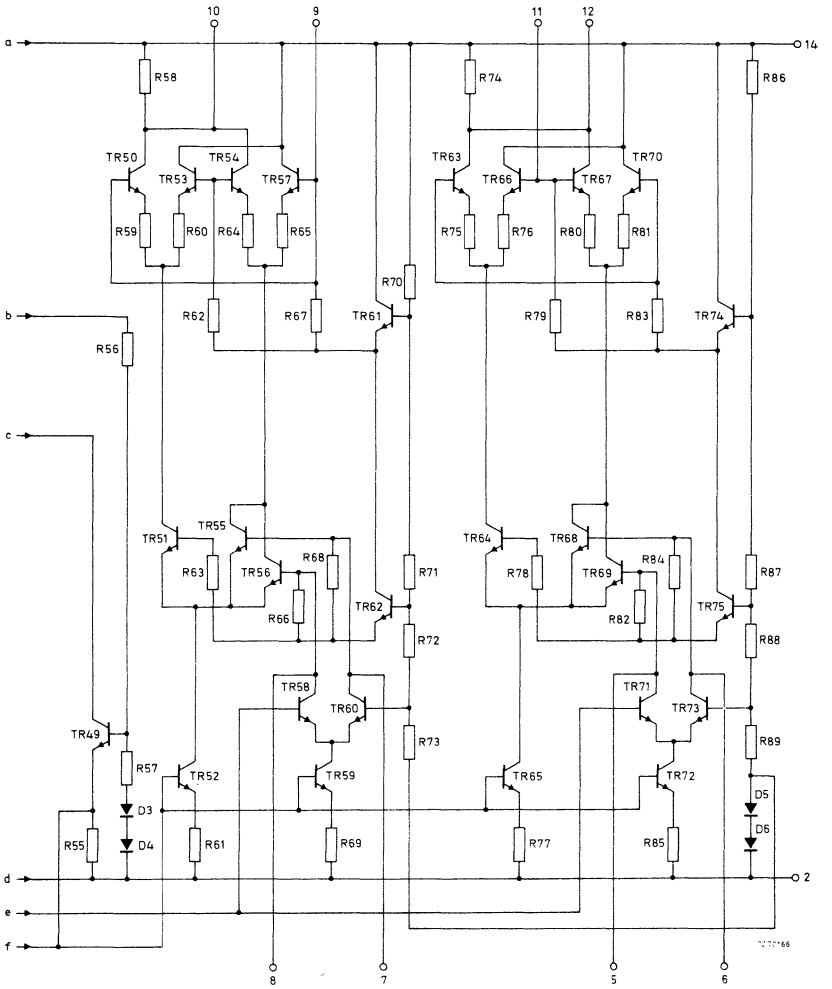
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RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltage			
Supply voltage	V_{14-2}	max. 13,2	V
Power dissipation			
Total power dissipation	P_{tot}	max. 510	mW
Temperatures			
Storage temperature	T_{stg}	−25 to +125	°C
Operating ambient temperature	T_{amb}	−25 to +65	°C [1]

CHARACTERISTICS measured in the circuit on page 6

Supply voltage	V_{14-2}	typ. 12 10,2 to 13,2	V V
Required input signals at V_{14-2} = 12 V and T_{amb} = 25 °C			
Chrominance input signal			
peak-to-peak value	$V_{1-2(p-p)}$ PAL $V_{3-2(p-p)}$ SECAM	35 to 75 150 to 400	mV mV
Input impedance	$\lvert Z_{1-2}\rvert$ $\lvert Z_{3-2}\rvert$	1,2 to 2,6	kΩ
PAL matrix			
Gain from both inputs to pin 13		2,3 to 3,3	
Gain from both inputs to pin 15		2,6 to 3,6	
Gain difference from line-to-line		< 5	%
Phase errors from line-to-line in the (R-Y) output for zero error in the (B-Y) output		< 2,5°	
Output impedance	$\lvert Z_{13-2}\rvert$ $\lvert Z_{15-2}\rvert$	< 100	Ω
SECAM permutator			
Diaphotie		< −46	dB
Output signal (peak-to-peak value)	$V_{13-2(p-p)}$ $V_{15-2(p-p)}$	1,6 [2] to 2,2	V
Output impedance	$\lvert Z_{13-2}\rvert$ $\lvert Z_{15-2}\rvert$	< 100	Ω

[1]) When a stabilized power supply of ≤ 12 V is applied, T_{amb} is max. 75 °C.

[2]) At an input voltage of 0,15 V; at an input voltage > 0,2 V the figure is 1,7 V.

CHARACTERISTICS (continued)

Demodulator

Chrominance input signal amplitude

PAL: (B-Y); peak-to-peak value	$V_{9-2(p-p)}$	typ.	0,22	V
(R-Y); peak-to-peak value	$V_{11-2(p-p)}$	typ.	0,28	V
SECAM: peak-to-peak value	$V_{9-2(p-p)}$; $V_{11-2(p-p)}$		1,5 to 3	V
Input impedance	$\lvert Z_{9-2}\rvert$; $\lvert Z_{11-2}\rvert$	>	1	kΩ

Reference input signal amplitude

PAL: peak-to-peak value	$V_{6-2(p-p)}$; $V_{7-2(p-p)}$		0,5 to 1,5	V
SECAM: peak-to-peak value	$V_{5-2(p-p)}$; $V_{8-2(p-p)}$		0,18 [1]) to 1,5	V
Input impedance	$\lvert Z_{5-2}\rvert$; $\lvert Z_{7-2}\rvert$; $\lvert Z_{6-2}\rvert$; $\lvert Z_{8-2}\rvert$		0,75 to 1,25	kΩ

Colour difference output signal

(R-Y); peak-to-peak value	$V_{12-2(p-p)}$		0,99 to 1,21	V [2])
(B-Y); peak-to-peak value	$V_{10-2(p-p)}$		1,32 to 1,62	V [2])
Output impedance	$\lvert Z_{10-2}\rvert$; $\lvert Z_{12-2}\rvert$		2,4 to 4,2	kΩ

Diaphotie at SECAM operation

Diaphotie of the total circuit at frequencies corresponding to saturated green D_R = 4,72 MHz and D_B = 4,04 MHz		<	−40	dB

Square wave input

peak-to-peak value	$V_{16-2(p-p)}$		2,5 to 3,5	V
Input impedance	$\lvert Z_{16-2}\rvert$	>	3,8	kΩ

System switch input [3])

PAL:		7 to V_{14-2}	V
SECAM:		0 to 1	V

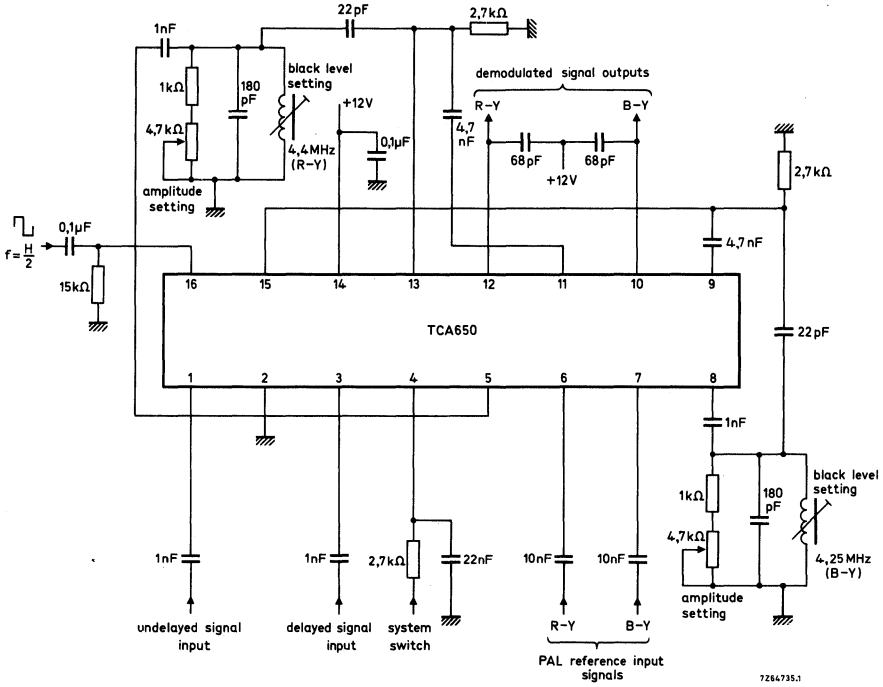
---

[1]) Limiting starts at the quoted value.

[2]) The peak-to-peak clipping level for PAL is about 4,7 V for (B-Y) and 3 V for (R-Y). The discriminator characteristic allows a maximum peak-to-peak output signal of 3,6 V for (B-Y) and 2,4 V for (R-Y) (SECAM).

[3]) The switching signal is applied to pin 4 via a resistor of 2,7 kΩ (±10%).

APPLICATION INFORMATION



Pinning

1. Chrominance input
2. Earth (negative supply)
3. Chrominance input
4. System switch input
5. Reference (R-Y) input SECAM
6. Reference (R-Y) input PAL
7. Reference (B-Y) input PAL
8. Reference (B-Y) input SECAM
9. Chrominance (B-Y), D_B input
10. Colour difference (B-Y) output
11. Chrominance (R-Y), D_R input
12. Colour difference (R-Y) output
13. Chrominance (R-Y), D_R output
14. Supply voltage (12 V)
15. Chrominance (B-Y), D_B output
16. Square wave input

APPLICATION INFORMATION (continued)

The function is quoted against the corresponding pin number

1. Chrominance input

   The blanked composite chrominance signal from pin 1 of the TCA640 is applied to this input via a resistive divider.

2. Negative supply (earth)

3. Chrominance input

   The blanked composite chrominance signal from pin 15 of the TCA640 is applied to this input via a delay-line, which has a delay time of 64 µs.

4. System switch input

   The control voltage for switching the standard is applied to this input via a resistor of 2,7 kΩ (± 10%). A decoupling capacitor of at least 10 nF is recommended. Between 7 V and the supply voltage the circuit operates in the PAL mode, whereas between 0 V and 1 V the mode SECAM is selected.

5. Reference input for the (R-Y) demodulator

   The SECAM reference signal is applied to this pin. The reference signal is obtained from pin 11 via a tank circuit. The tank circuit is tuned such that the level at the (R-Y) output (pin 12) during black (f_o = 4,4 MHz) equals the level during blanking (no signal). The output voltage amplitude at pin 12 can be adjusted by damping the tank circuit.

6. Reference input for the (R-Y) demodulator

   A PAL reference signal having (R-Y) phase is applied to this pin.

7. Reference input for the (B-Y) demodulator

   A PAL reference signal having (B-Y) phase is applied to this pin.

8. Reference input for the (B-Y) demodulator

   The SECAM reference signal is applied to this pin. The reference signal is obtained from pin 15 via a tank circuit. The tank circuit is tuned such that the level at the (B-Y) output (pin 10) during black (f_o = 4,25 MHz) equals the level during blanking (no signal). The output voltage amplitude at pin 10 can be adjusted by damping the tank circuit.

9. Chrominance input to the (B-Y), D_B demodulator

   The output signal of pin 15 is applied via a coupling capacitor of 4,7 nF.

10. Output of the (B-Y) demodulator

    The output signal of the balance demodulator contains an r.f. ripple of twice the chrominance frequency to be filtered by a π filter. At SECAM the required de-emphasis circuit should be applied.

11. Chrominance input to the (R-Y), D_R demodulator

    The output signal of pin 13 is applied via a coupling capacitor of 4,7 nF.

APPLICATION INFORMATION (continued)

12. Output of the (R-Y) demodulator

See pin 10.

13. Chrominance (R-Y), D_R output

The (R-Y) component of the chrominance signal (D_R component at SECAM) is present at this pin.
The signal is applied to the input of the (R-Y) demodulator (pin 11) and to the tank circuit for the SECAM reference signal.
The emitter follower output should be loaded with a 2,7 kΩ resistor to obtain an output impedance of <100 Ω.

14. Supply voltage (12 V)

Correct operation occurs within the range 10,2 to 13,2 V.
The power dissipation must not exceed 510 mW at 65 °C ambient temperature.

15. Chrominance (B-Y), D_B output

The (B-Y) component of the chrominance signal (D_B component at SECAM) is present at this pin.
The signal is applied to the input of the (B-Y) demodulator (pin 9) and to the tank circuit for the SECAM reference signal.
The emitter follower output should be loaded with a 2,7 kΩ resistor to obtain an output impedance of <100 Ω.

16. Square wave input

A square wave with an amplitude of 3 V drives the PAL switch or the SECAM permutator.
The square wave is available at pin 12 of the TCA640.

CONTRAST, SATURATION AND BRIGHTNESS CONTROL CIRCUIT FOR COLOUR DIFFERENCE AND LUMINANCE SIGNALS

The TCA660B is an integrated circuit performing the control functions of contrast, saturation and brightness in colour television receivers.
Contrast is controlled by three tracking electronic potentiometers; one for the luminance signal and the other two for the (R-Y) and (B-Y) colour difference signals.
In addition two tracking electronic potentiometers provide the saturation control of the colour difference signals.
Brightness is controlled by varying the black level of the luminance signal at the output.
An inverting amplifier is also included for matrixing the (G-Y) signal from the (R-Y) and (B-Y) colour difference signals.

QUICK REFERENCE DATA

Supply voltage	V_{13-4}	nom.	12	V
Supply current	I_{13}	nom.	35	mA
Luminance input current (black-to-white positive video signal)	I_{16}	typ.	0,7	mA
Luminance output voltage (black-to-white positive video signal; peak-to-peak value)	$V_{1-4(p-p)}$	typ.	3	V [1]
Black level (nominal value)	V_{1-4}	typ.	4,2	V
Brightness control (around nominal black level)	V_{1-4}		+1 to −2	V
Gain of the (R-Y) and (B-Y) amplifier		typ.	5	dB [1] [2]
Gain of the (G-Y) amplifier		typ.	1	
Contrast control range			+3 to −20	dB [3]
Saturation control range			+6 to −20	dB [3]

[1] At nominal contrast setting (max. contrast −3 dB)

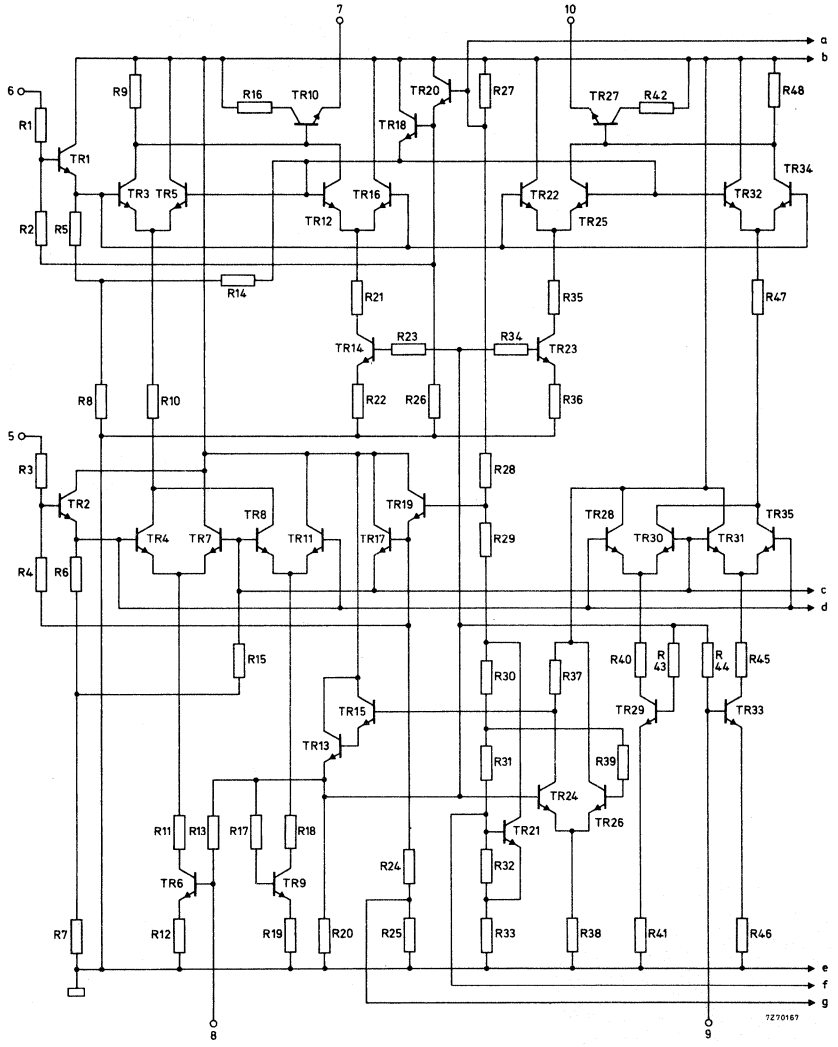
[2] At nominal saturation control setting (max. saturation −6 dB)

[3] Nominal contrast and nominal saturation are specified as 0 dB.

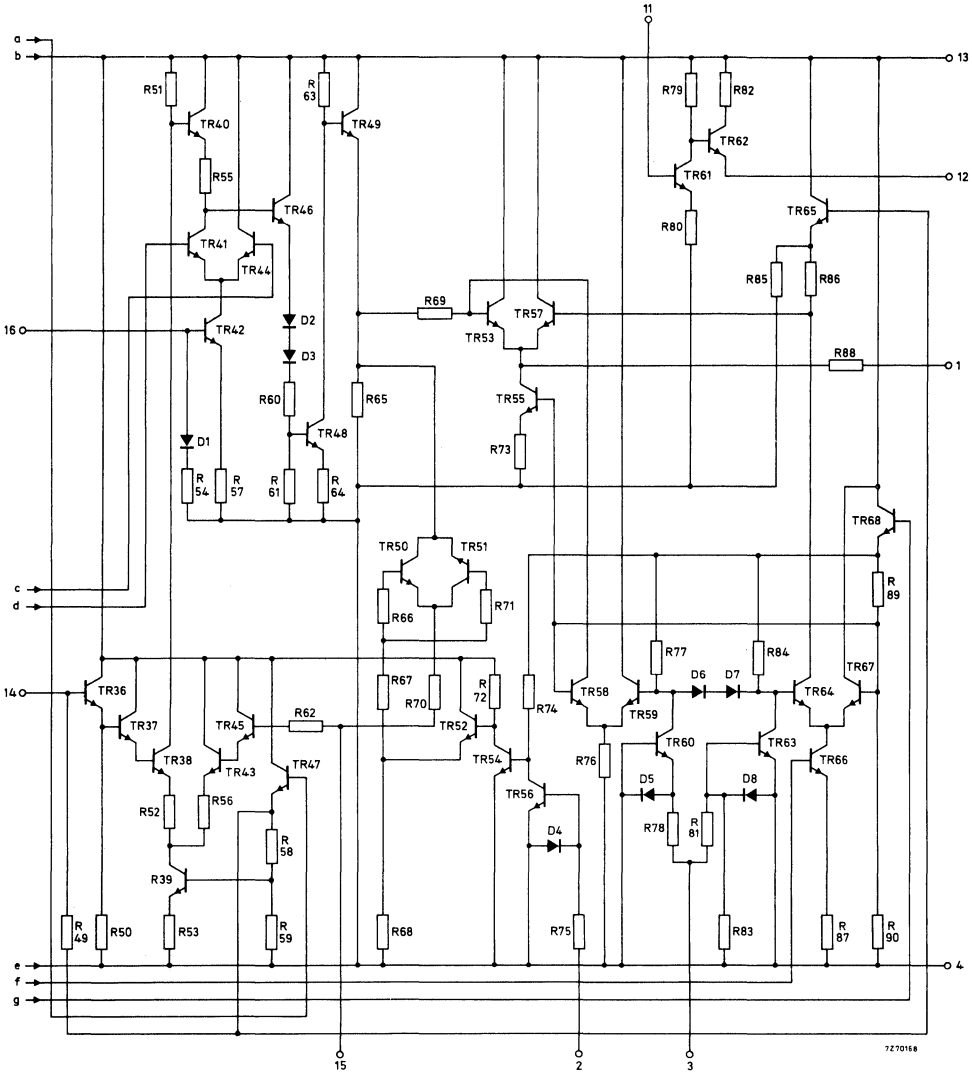
PACKAGE OUTLINE

16-lead DIL; plastic (SOT-38).

CIRCUIT DIAGRAM



CIRCUIT DIAGRAM (continued)



RATINGS Limiting values in accordance with the Absolute Maximum System (IEC134)

Voltage			
Supply voltage	V_{13-4}	max.	13,2 V
Power dissipation			
Total power dissipation	P_{tot}	max.	600 mW
Temperatures			
Storage temperature	T_{stg}		−25 to +125 °C
Operating ambient temperature	T_{amb}		−25 to +65 °C [1]

CHARACTERISTICS measured in the circuit on page 7

Supply voltage	V_{13-4}	typ.	12 V 10,2 to 13,2 V
Required input signals at V_{13-4} = 12 V and T_{amb} = 25 °C			
Luminance input current			
black-to-white positive video signal	I_{16}	typ.	0,7 mA 0 to 2,5 mA
Input impedance at I_{16} = 1 mA	$\lvert Z_{16-4}\rvert$		60 to 90 Ω
Input impedance variation for an			
input current variation ΔI_{16} = ± 0,5 mA	$\lvert \Delta Z_{16-4}\rvert$		∓25 Ω
Colour difference input voltage			
(R-Y); peak-to-peak value	$V_{9-4(p-p)}$	<	0,7 V
(B-Y); peak-to-peak value	$V_{8-4(p-p)}$	<	0,9 V
Input voltage variation before clipping			
of the output voltage occurs	ΔV_{8-4} ΔV_{9-4}	typ.	0,8 V
Input impedance	$\lvert Z_{8-4}\rvert$ $\lvert Z_{9-4}\rvert$		3,5 to 6,5 kΩ
Blanking pulse (peak value)	V_{3-4M}		−1,5 to −10 V
Black level reinsertion pulse (peak value)	V_{3-4M}		+2 to +12 V [2]
Black level clamp pulse (peak value)	V_{2-4M}		+1 to +12 V
Luminance output voltage at nominal contrast			
black-to-white positive video signal; peak-to-peak value	$V_{1-4(p-p)}$		2 to 4 V [3]

[1]) When a stabilized power supply of ≤ 12 V is applied, T_{amb} is max. 75 °C.
[2]) During scan V_{3-4} must be kept lower than 0,7 V (positive and negative) to avoid blanking of the luminance signal.
[3]) Nominal contrast is specified as maximum contrast −3 dB.

CHARACTERISTICS (continued)

Black level at nominal brightness setting	V_{1-4}	typ.	4,2	V	1)
Black level variation with brightness setting	ΔV_{1-4}		+1 to −2	V	
Contrast control voltage range	V_{5-4}	See graph on page 6			
Black level variation with contrast control	ΔV_{1-4}	<	40	mV	2)
Black level variation with video contents	ΔV_{1-4}	<	20	mV	3)
Variation between video black level and reinserted black level at ΔT_{amb} = 25 °C and ΔV_{13-4} ± 10%	V_{1-4}	<	±20	mV	
Blanking level with respect to nominal brightness	V_{1-4}		−0,8 to −1,2	V	
Bandwidth (−3 dB) of luminance signal	B	>	6	MHz	
Colour difference output signal for nominal contrast and saturation 4) 5)					
(R-Y); peak-to-peak value	$V_{10-4(p-p)}$	typ.	1,25	V	6)
(B-Y); peak-to-peak value	$V_{7-4(p-p)}$	typ.	1,6	V	6)
D.C. output level	V_{7-4} / V_{10-4}	typ.	6,1	V	
Output level variation with contrast and saturation control	ΔV_{7-4} / ΔV_{10-4}	<	500	mV	
Permissible d.c. load impedance	$\lvert Z_{7-4}\rvert$ / $\lvert Z_{10-4}\rvert$	>	4	kΩ	
Saturation control voltage range	V_{6-4}	See graph on page 6			
Saturation control at $V_{6-4} < 0,5$ V		<	−50	dB	
Bandwidth (−3 dB) of colour difference signal	B	>	2,5	MHz	

1) Nominal brightness setting V_{14-4} = 5,7 V.
2) Only valid if the input current does not exceed 0,5 mA during black.
3) For a.c. coupling only.
4) Nominal contrast is specified as maximum contrast −3 dB.
5) Nominal saturation is specified as maximum saturation −6 dB.
6) This value is obtained at the specified maximum input voltage.

CHARACTERISTICS (continued)

(G-Y) amplifier

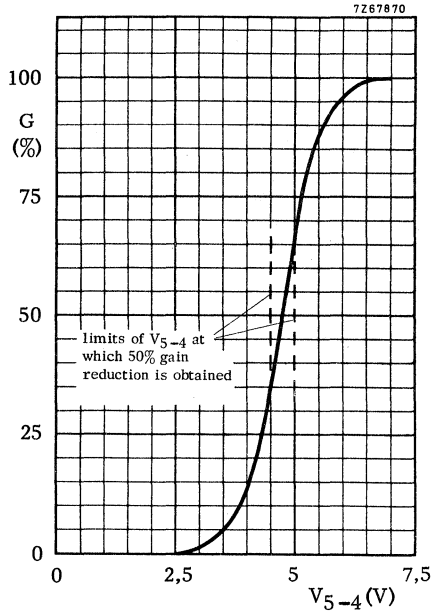
input voltage (peak-to-peak value)	$V_{11-4(p-p)}$	<	1	V
output voltage (peak-to-peak value)	$V_{12-2(p-p)}$	<	1	V
voltage gain	G_{11-12}		−1 to +0,5	dB

Tracking during contrast and saturation control

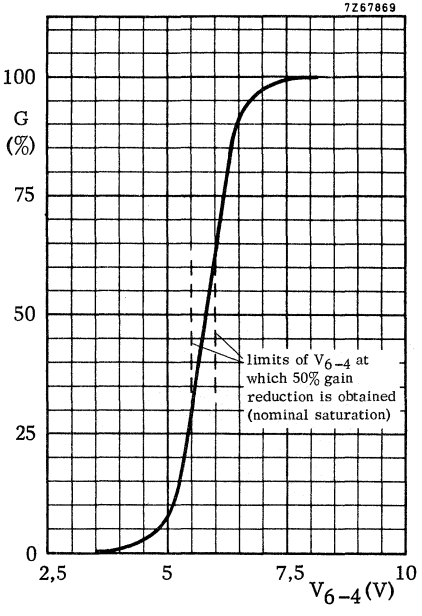
at a contrast decrease of 20 dB				
change of the ratio $\frac{(R-Y)}{(B-Y)}$		<	±1	dB
change of the ratio $\frac{Y}{(B-Y)}$			0 to 4	dB
at a saturation decrease of 20 dB				
change of the ratio $\frac{(R-Y)}{(B-Y)}$		<	±1	dB

Cross coupling

luminance signal to colour difference signal		<	−40	dB
(B-Y) signal to (R-Y) signal		<	−30	dB
colour difference signal to luminance signal		<	−40	dB

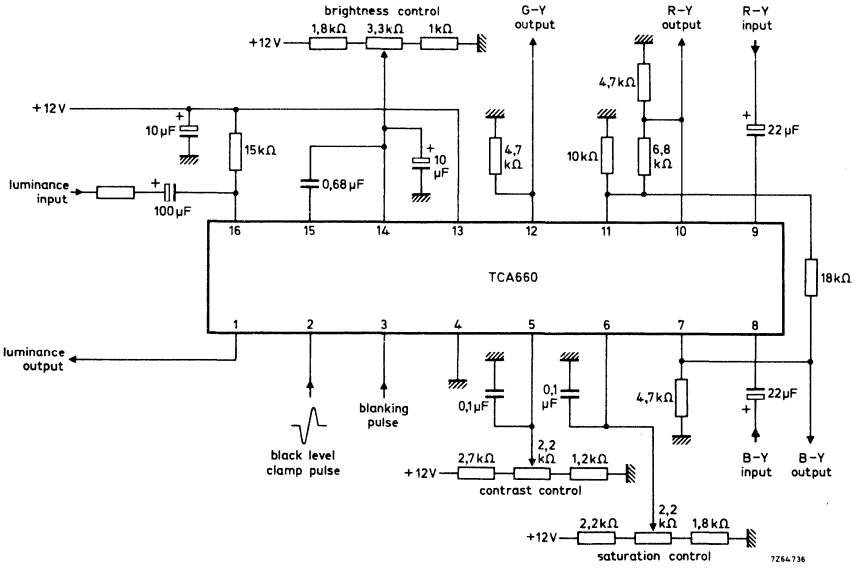


Contrast control of luminance amplifier



Saturation control of chrominance amplifier

APPLICATION INFORMATION



Pinning

1. Luminance signal output
2. Black level clamp pulse input
3. Blanking pulse input
4. Earth (negative supply)
5. Contrast control input
6. Saturation control input
7. (B-Y) signal output
8. (B-Y) signal input
9. (R-Y) signal input
10. (R-Y) signal output
11. (G-Y) signal input
12. (G-Y) signal output
13. Supply voltage (12 V)
14. Brightness control input
15. Black level clamp capacitor
16. Luminance signal input

APPLICATION INFORMATION (continued)

The function is quoted against the corresponding pin number

1. Luminance signal output

   A positive video signal of 3 V peak-to-peak is available at nominal contrast setting. The black level is clamped internally on the back porch.
   By means of the brightness control the black level can be varied between 2,2 V and 5,2 V. The blanking level of the output signal will assume a value of 3,0 to 3,4 V.

2. Black level clamp pulse input

   A positive pulse with a peak value between +1 V and +12 V will clamp the black level of the video signal to a nominal level of 4,2 V. The pulse may only be present during the back porch and should have a duration of about 3 µs.

3. Blanking pulse input

   Two modes operation can be selected by the choice of the amplitude of the pulse applied:

   - blanking

   - black level reinsertion

   Blanking of the luminance output signal is obtained when the peak value of the pulse ranges from −1,5 to −10 V. An artificial black level of nominally +4,2 V is inserted in the luminance output signal during the blanking period when the peak value of the pulse ranges from +2 to +12 V.
   During scan the amplitude at pin 3 should remain between +0,7 V and −0,7 V to avoid blanking.

4. Negative supply (earth)

5. Contrast control input

   The contrast curve is given on page 4. To avoid damaging of the circuit by flash-over pulses, picked-up by the leads, it is recommended that a capacitor of 100 nF be connected between this pin and earth.

6. Saturation control input

   The control curve is given on page 4. To avoid damaging of the circuit by flash-over pulses, picked-up by the leads, it is recommended that a capacitor of 100 nF be connected between this pin and earth.

7. (B-Y) signal output

   The amplitude of this signal is controlled by the contrast setting and the saturation setting simultaneously. At nominal contrast and nominal saturation setting an amplitude of 1,6 V peak-to-peak is obtained at an input amplitude of 0,9 V peak-to-peak. The average level is typically 6,1 V.

8. (B-Y) signal input

   The signal has to be a.c. coupled to the input.
   To cope with the variation of picture contents an input voltage margin of ± 0,8 V is provided, whereas the input signal has a typical value of ± 0,45 V for a saturated colour bar signal.

APPLICATION INFORMATION (continued)

9. (R-Y) signal input

The signal has to be a.c. coupled to the input.
To cope with the variation of picture contents an input voltage margin of ± 0, 8 V is provided, whereas the input signal has a typical value of ± 0, 35 V for a saturated colour bar input.

10. (R-Y) signal output

The amplitude of this signal is controlled by the contrast setting and saturation setting simultaneously. At nominal contrast and nominal saturation setting an amplitude of 1, 25 V peak-to-peak is obtained at an input amplitude of 0, 7 V peak to peak.
The average level is typically 6, 1 V.

11. (G-Y) signal input

The (G-Y) signal is obtained by matrixing a part of the (R-Y) and (B-Y) signals in a resistor network. The input may range from 1 to 6, 5 V.
An average level of typical 5, 9 V is required to produce an average output level of 6, 1 V.
The gain of the inverter stage is typically 1.

12. (G-Y) signal output

An inverted signal with an amplitude of maximum 1 V peak-to-peak is available at this pin.

13. Supply voltage (12 V)

Correct operation occurs within the range 10, 2 to 13, 2 V.
The power dissipation must not exceed 600 mW at 65 °C ambient temperature.

14. Brightness control input

The black level of the luminance output signal tracks the potential applied to this pin.
A typical value for setting the brightness control is 5, 7 V, for which a black level of 4, 2 V is obtained.
It is recommended that a capacitor of at least 10 μF be connected between this pin and earth.

15. Black level clamp capacitor

The level of the back porch of the luminance output signal is stored in an external capacitor of about 0, 68 μF; the latter to be connected between pins 14 and 15.

16. Luminance signal input

A positive luminance signal of 0, 7 mA peak-to-peak between black and white level drives the luminance amplifier.
A black level of about 0, 3 mA is recommended. For a.c. coupling a bias resistor to the supply line is required to bias the amplifier properly.
The resistance depends on the signal amplitude e.g.: 15 kΩ is recommended for a input signal of 0, 7 mA peak-to-peak.

DOUBLE BALANCED MODULATOR/DEMODULATOR

The TDA0820T is a monolithic integrated circuit for use at frequencies up to 650 MHz.
Typical applications are:

- modulator
- mixer
- switch/chopper
- a.m. synchronous demodulator
- f.m. quadrature demodulator
- phase comparator
- differential amplifier

The circuit is arranged to offer very flexible circuit design possibilities. The excellent matching and temperature tracking of the transistors in the circuit allow the use of circuit techniques which are not available when using discrete devices.

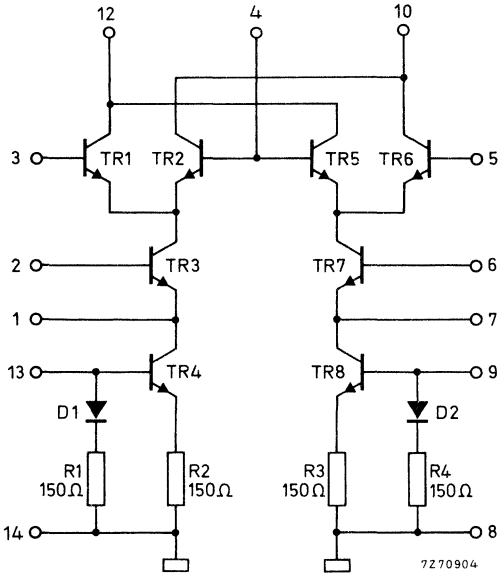


Fig. 1 Circuit diagram.

PACKAGE OUTLINE

14-lead mini-pack; plastic (SO-14; SOT-108A).

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range	V_{10-8}; V_{10-14}; V_{12-8}; V_{12-14}	0 to 13,2	V
Voltages (each transistor)			
Collector-substrate voltage (open base) and emitter)	V_{CSO}	max. 15	V
Collector-base voltage (open emitter)	V_{CBO}	max. 12	V
Collector-emitter voltage (open base)	V_{CEO}	max. 10	V
Emitter-base voltage (open collector)	V_{EBO}	max. 5	V
Currents (each transistor)			
Emitter current	I_E	max. 10	mA
Base current	I_B	max. 10	mA
Total power dissipation when mounted on a printed-circuit board	P_{tot}	max. 250	mW
Storage temperature	T_{stg}	−55 to + 125	°C
Operating ambient temperature	T_{amb}	0 to + 70	°C

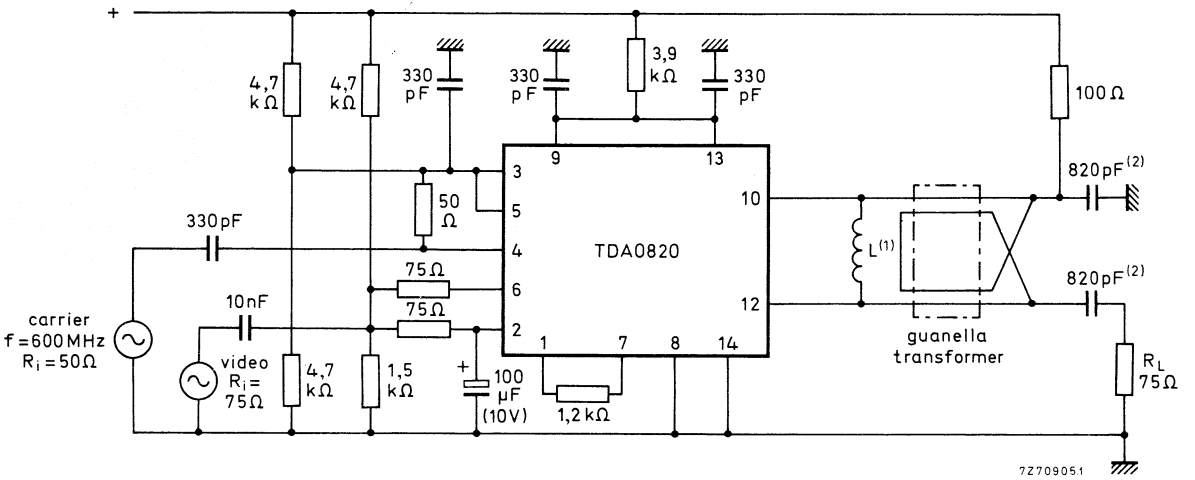
THERMAL RESISTANCE

From junction to ambient	$R_{th\ j-a}$	= 220	K/W

CHARACTERISTICS

$V_{10-8} = V_{10-14} = V_{12-8} = V_{12-14} = 12$ V; $T_{amb} = 25$ °C; measured in Fig. 2

Supply current	$I_{10} + I_{12}$	typ. 2,5 < 3	mA mA
Input signals			
carrier signal (r.m.s. value)	$V_{3-4(rms)}$; $V_{5-4(rms)}$	< 100	mV
video signal; negative modulated (peak-to-peak value)	$V_{6-2(p-p)}$	< 1,4	V
Output signal at top sync over 75 Ω (peak-to-peak value)	$V_{10-12(p-p)}$	> 22	mV
Carrier suppression in balanced condition	V_{10-12}	> 38	dB
Differential phase		< 6°	
Differential gain		< 15	%
Distortion of video signal		< −38	dB



(1) L = air coil; 3 turns; ϕ 3 mm.
(2) U.H.F. decoupling capacitor 2212 669 98003.

Fig. 2 Test circuit.

4 W AUDIO POWER AMPLIFIER WITH D.C. VOLUME CONTROL

The TDA1013A is a monolithic integrated audio amplifier circuit with d.c. volume control in a 9-lead single in-line (SIL) plastic package. The wide supply voltage range makes this circuit very suitable for applications in mains-fed apparatus such as television receivers and record players.

The d.c. volume control stage has a logarithmic control characteristic with a range of more than 80 dB; control can be obtained by means of a variable d.c. voltage between 3,5 and 8 V.

The audio amplifier has a well defined open loop gain and a fixed integrated closed loop gain. This offers an optimum in number of external components, performance and stability.

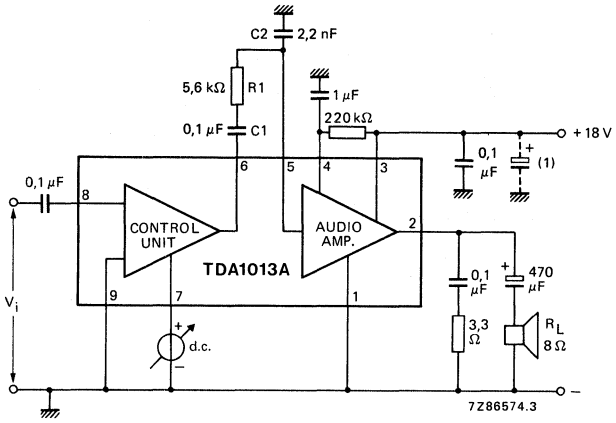
The SIL package (SOT-110B) offers a simple and low-cost heatsink connection.

QUICK REFERENCE DATA

Supply voltage range	V_P	15 to 35	V
Repetitive peak output current	I_{ORM}	max. 1,5	A
Total sensitivity (d.c. control at max. gain) for P_o = 2,5 W	V_i	typ. 55	mV
Audio amplifier			
Output power at d_{tot} = 10% V_P = 18 V; R_L = 8 Ω	P_o	typ. 4,5	W
Total harmonic distortion at P_o = 2,5 W; R_L = 8 Ω	d_{tot}	typ. 0,5	%
Sensitivity for P_o = 2,5 W	V_i	typ. 125	mV
D.C. volume control unit			
Gain control range	ϕ	> 80	dB
Signal handling at $d_{tot} < 1\%$ (d.c. control at 0 dB)	V_i	> 1,2	V
Sensitivity for V_o = 125 mV at max. voltage gain	V_i	typ. 55	mV
Input impedance (pin 8)	$\|Z_i\|$	typ. 250	kΩ

PACKAGE OUTLINE

9-lead SIL; plastic (SOT-110B).



(1) Belongs to power supply.

Fig. 1 Basic application diagram also used as test circuit with R1 = 5,1 kΩ and C1 = 22 nF.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	35 V
Non-repetitive peak output current	I_{OSM}	max.	3 A
Repetitive peak output current	I_{ORM}	max.	1,5 A
Storage temperature	T_{stg}		−55 to + 150 °C
Crystal temperature	T_j		−25 to + 150 °C
Total power dissipation	see derating curve Fig. 2		

HEATSINK DESIGN

Assume V_P = 18 V; R_L = 8 Ω; T_{amb} = 60 °C (max.); T_j = 150 °C (max); for a 4 W application into an 8 Ω load, the maximum dissipation is about 2,5 W.
The thermal resistance from junction to ambient can be expressed as:

$$R_{th\ j\text{-}a} = R_{th\ j\text{-}tab} + R_{th\ tab\text{-}h} + R_{th\ h\text{-}a} = \frac{T_{j\ max} - T_{amb\ max}}{P_{max}} = \frac{150 - 60}{2,5} = 36\ K/W.$$

Since $R_{th\ j\text{-}tab}$ = 9 K/W and $R_{th\ tab\text{-}h}$ = 1 K/W, $R_{th\ h\text{-}a}$ = 36 − (9 + 1) = 26 K/W.

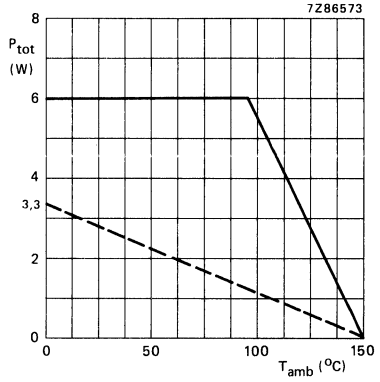


Fig. 2 Power derating curve.
——— infinite heatsink;
– – – without heatsink.

CHARACTERISTICS

V_P = 18 V; R_L = 8 Ω; f = 1 kHz; T_{amb} = 25 °C; unless otherwise specified

Supply voltage	V_P	typ.	18 V
			15 to 35 V
Total quiescent current	I_{tot}	typ.	35 mA
Noise output voltage (see also note)	V_n	<	1,4 mV
Total sensitivity (d.c. control at maximum gain) for P_o = 2,5 W	V_i		38 to 69 mV
		typ.	55 mV
Frequency response (–3 dB)	f		35 Hz to 20 kHz
Audio amplifier			
Repetitive peak output current	I_{ORM}	<	1,5 A
Output power at d_{tot} = 10%	P_o	>	4 W
		typ.	4,5 W
Total harmonic distortion at P_o = 2,5 W	d_{tot}	typ.	0,5 %
		<	1 %
Voltage gain	G_v	typ.	30 dB
Sensitivity for P_o = 2,5 W	V_i	typ.	125 mV
Input impedance (pin 5)	$\|Z_i\|$	>	100 kΩ
		typ.	250 kΩ

Note

Measured in a bandwidth according to IEC 179-curve 'A'; R_S = 5 kΩ and d.c. control at minimum gain.

CHARACTERISTICS (continued)

D.C. volume control unit

Gain control range (see also Fig. 3)	ϕ	>	80 dB
Signal handling at $d_{tot} < 1\%$ (d.c. control at 0 dB)	V_i	>	1,2 V
Sensitivity for V_o = 125 mV at max. voltage gain	V_i	typ.	55 mV
Input impedance (pin 8)	$\|Z_i\|$	>	100 kΩ
		typ.	250 kΩ
Output impedance (pin 6)	$\|Z_o\|$		100 to 400 Ω
		typ.	200 Ω

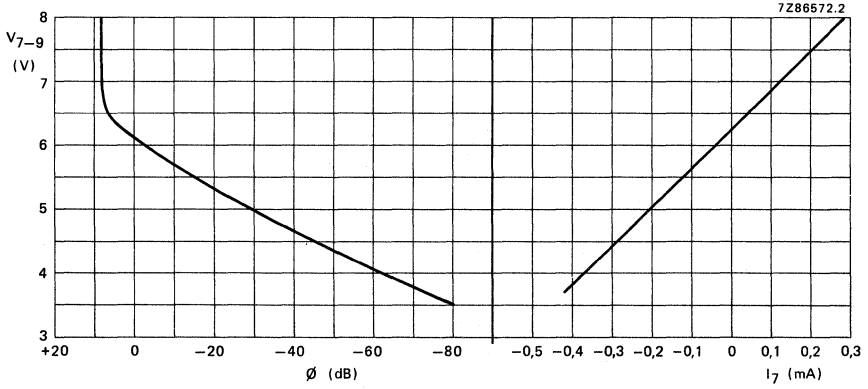


Fig. 3 Typical values gain control; V_i at pin 7.

SIGNAL-SOURCES SWITCH

The TDA1029 is a dual operational amplifier (connected as an impedance converter) each amplifier having 4 mutually switchable inputs which are protected by clamping diodes. The input currents are independent of switch position and the outputs are short-circuit protected.

The device is intended as an electronic two-channel signal-source switch in a.f. amplifiers.

QUICK REFERENCE DATA

Supply voltage range (pin 14)	V_P		6 to 23	V
Operating ambient temperature	T_{amb}		−30 to + 80	°C
Supply voltage (pin 14)	V_P	typ.	20	V
Current consumption	I_{14}	typ.	3,5	mA
Maximum input signal handling (r.m.s. value)	$V_{i(rms)}$	typ.	6	V
Voltage gain	G_v	typ.	1	
Total harmonic distortion	d_{tot}	typ.	0,01	%
Crosstalk	α	typ.	70	dB
Signal-to-noise ratio	S/N	typ.	120	dB

PACKAGE OUTLINE

16-lead DIL; plastic (SOT-38).

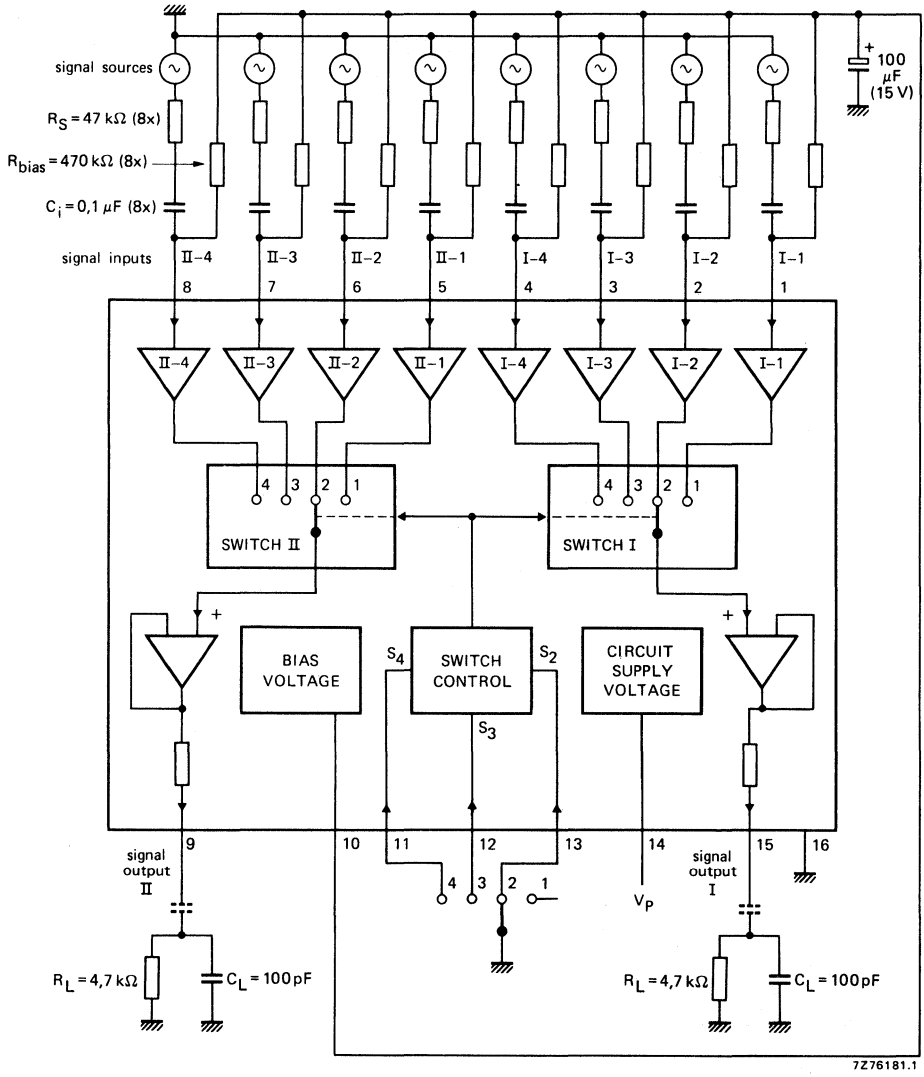


Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 14)	V_P	max.	23	V
Input voltage (pins 1 to 8)	V_I	max.	V_P	
	$-V_I$	max.	0,5	V
Switch control voltage (pins 11, 12 and 13)	V_S		0 to 23	V
Input current	$\pm I_I$	max.	20	mA
Switch control current	$-I_S$	max.	50	mA
Total power dissipation	P_{tot}	max.	800	mW
Storage temperature	T_{stg}		−55 to + 150	°C
Operating ambient temperature	T_{amb}		−30 to + 80	°C

CHARACTERISTICS

V_P = 20 V; T_{amb} = 25 °C; unless otherwise specified

Current consumption				
without load; $I_g = I_{15} = 0$	I_{14}	typ.	3,5	mA
			2 to 5	mA
Supply voltage range (pin 14)	V_P		6 to 23	V
Signal inputs				
Input offset voltage of switched-on inputs $R_S \leqslant 1$ kΩ	V_{io}	typ.	2	mV
		<	10	mV
Input offset current of switched-on inputs	I_{io}	typ.	20	nA
		<	200	nA
Input offset current of a switched-on input with respect to a non-switched-on input of a channel	I_{io}	typ.	20	nA
		<	200	nA
Input bias current independent of switch position	I_i	typ.	250	nA
		<	950	nA
Capacitance between adjacent inputs	C	typ.	0,5	pF
D.C. input voltage range	V_I		3 to 19	V
Supply voltage rejection ratio; $R_S \leqslant 10$ kΩ	SVRR	typ.	100	μV/V
Equivalent input noise voltage $R_S = 0$; f = 20 Hz to 20 kHz (r.m.s. value)	$V_{n(rms)}$	typ.	3,5	μV
Equivalent input noise current f = 20 Hz to 20 kHz (r.m.s. value)	$I_{n(rms)}$	typ.	0,05	nA
Crosstalk between a switched-on input and a non-switched-on input; measured at the output at R_S = 1 kΩ; f = 1 kHz	α	typ.	100	dB

CHARACTERISTICS (continued)

Signal amplifier

Voltage gain of a switched-on input at $I_9 = I_{15} = 0$; $R_L = \infty$	G_v	typ.	1
Current gain of a switched-on amplifier	G_i	typ.	10^5

Signal outputs

Output resistance (pins 9 and 15)	R_o	typ.	400 Ω
Output current capability at V_P = 6 to 23 V	$\pm I_9$; $\pm I_{15}$	typ.	5 mA
Frequency limit of the output voltage $V_{i(p-p)}$ = 1 V; R_S = 1 kΩ; R_L = 10 MΩ; C_L = 10 pF	f	typ.	1,3 MHz
Slew rate (unity gain); $\Delta V_{9\text{-}16}/\Delta t$; $\Delta V_{15\text{-}16}/\Delta t$ R_L = 10 MΩ; C_L = 10 pF	S	typ.	2 V/μs

Bias voltage

D.C. output voltage	$V_{10\text{-}16}$	typ. 10,2 to 11,8	11 V * V
Output resistance	$R_{10\text{-}16}$	typ.	8,2 kΩ

Switch control

switched-on inputs	interconnected pins	control voltages		
		$V_{11\text{-}16}$	$V_{12\text{-}16}$	$V_{13\text{-}16}$
I-1, II-1	1-15, 5-9	H	H	H
I-2, II-2	2-15, 6-9	H	H	L
I-3, II-3	3-15, 7-9	H	L	H
I-4, II-4	4-15, 8-9	L	H	H
I-4, II-4	4-15, 8-9	L	L	H
I-4, II-4	4-15, 8-9	L	H	L
I-4, II-4	4-15, 8-9	L	L	L
I-3, II-3	3-15, 7-9	H	L	L

In the case of offset control, an internal blocking circuit of the switch control ensures that not more than one input will be switched on at a time. In that case safe switching-through is obtained at $V_{SL} \leqslant 1{,}5$ V.

Control inputs (pins 11, 12 and 13)

Required voltage			
HIGH	V_{SH}	>	3,3 V **
LOW	V_{SL}	<	2,1 V
Input current			
HIGH (leakage current)	I_{SH}	<	1 μA
LOW (control current)	$-I_{SL}$	<	250 μA

* $V_{10\text{-}16}$ is typically $0{,}5 \cdot V_{14\text{-}16} + 1{,}5 \cdot V_{BE}$.

** Or control inputs open ($R_{11,12,13-16} > 33$ MΩ).

APPLICATION INFORMATION

V_P = 20 V; T_{amb} = 25 °C; measured in Fig. 1; R_S = 47 kΩ; C_i = 0,1 μF; R_{bias} = 470 kΩ; R_L = 4,7 kΩ; C_L = 100 pF (unless otherwise specified)

Voltage gain	G_v	typ.	−1,5 dB
Output voltage variation when switching the inputs	$\Delta V_{9\text{-}16}$; $\Delta V_{15\text{-}16}$	typ. <	10 mV 100 mV
Total harmonic distortion			
over most of signal range (see Fig. 4)	d_{tot}	typ.	0,01 %
V_i = 5 V; f = 1 kHz	d_{tot}	typ.	0,02 %
V_i = 5 V; f = 20 Hz to 20 kHz	d_{tot}	typ.	0,03 %
Output signal handling			
d_{tot} = 0,1%; f = 1 kHz (r.m.s. value)	$V_{o(rms)}$	> typ.	5,0 V 5,3 V
Noise output voltage (unweighted)			
f = 20 Hz to 20 kHz (r.m.s. value)	$V_{n(rms)}$	typ.	5 μV
Noise output voltage (weighted)			
f = 20 Hz to 20 kHz (in accordance with DIN 45405)	V_n	typ.	12 μV
Amplitude response			
V_i = 5 V; f = 20 Hz to 20 kHz; C_i = 0,22 μF	$\Delta V_{9\text{-}16}$; $\Delta V_{15\text{-}16}$	<	0,1 dB *
Crosstalk between a switched-on input and a non-switched-on input; measured at the output at f = 1 kHz	α	typ.	75 dB **
Crosstalk between switched-on inputs and the outputs of the other channels	α	typ.	90 dB **

* The lower cut-off frequency depends on values of R_{bias} and C_i.

** Depends on external circuitry and R_S. The value will be fixed mostly by capacitive crosstalk of the external components.

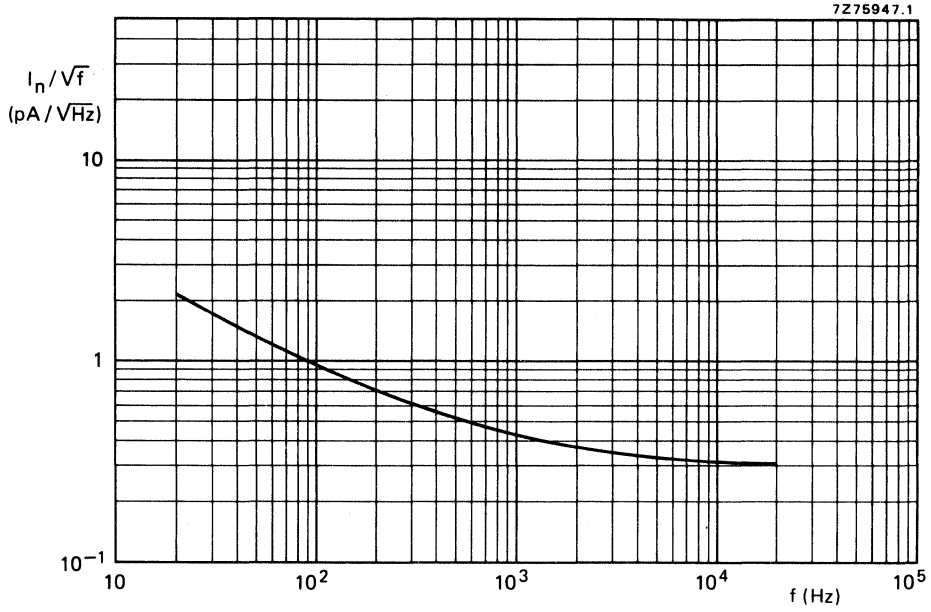


Fig. 2 Equivalent input noise current.

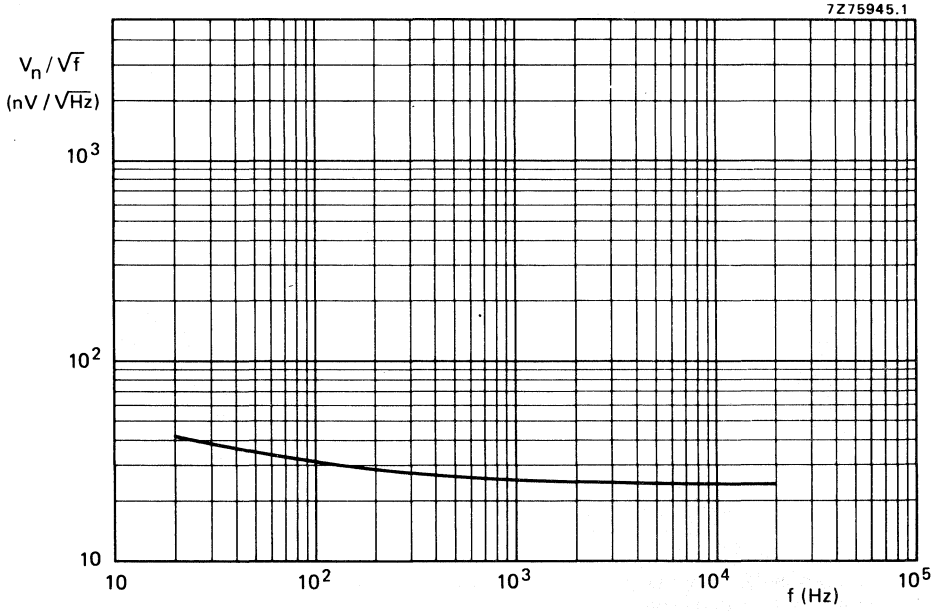


Fig. 3 Equivalent input noise voltage.

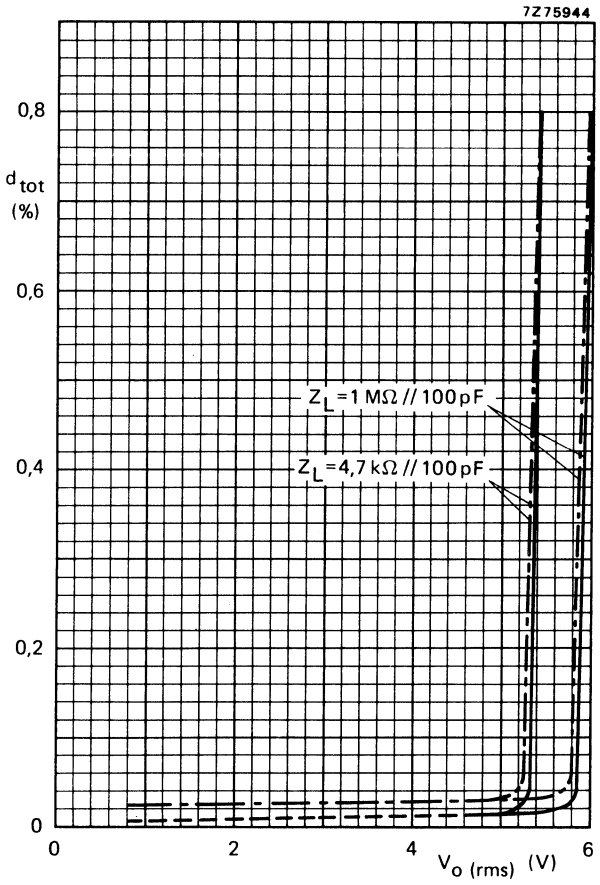


Fig. 4 Total harmonic distortion as a function of r.m.s. output voltage.
—— f = 1 kHz; — · — · f = 20 kHz.

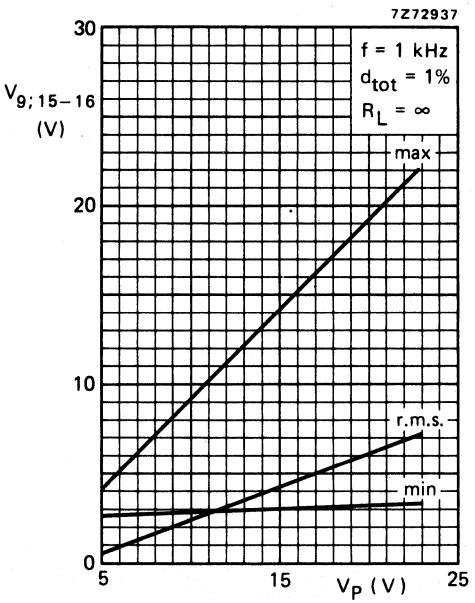


Fig. 5 Output voltage as a function of supply voltage.

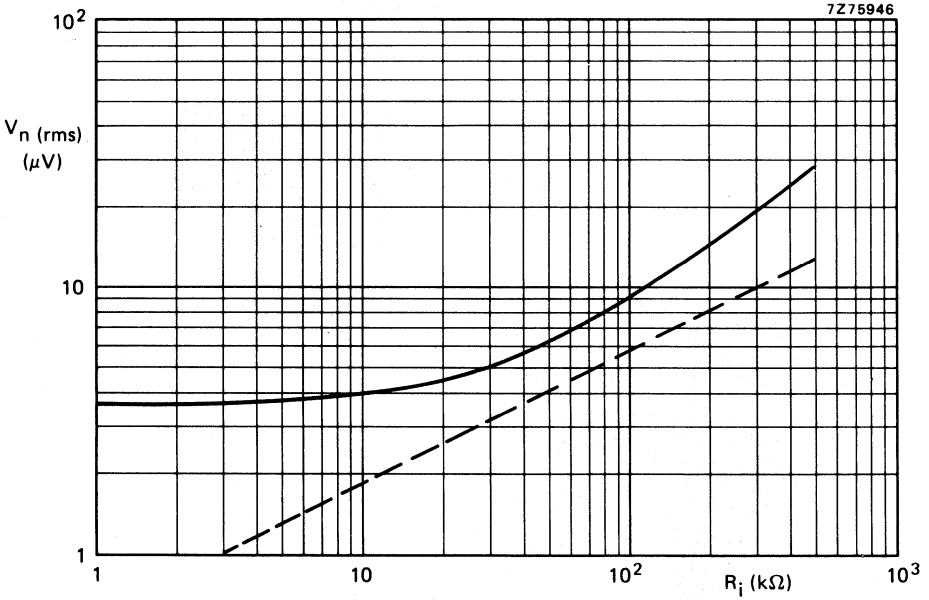


Fig. 6 Noise output voltage as a function of input resistance; G_v = 1; f = 20 Hz to 20 kHz.
—— V_n (output); – – – V_n (R_S).

APPLICATION NOTES

Input protection circuit and indication

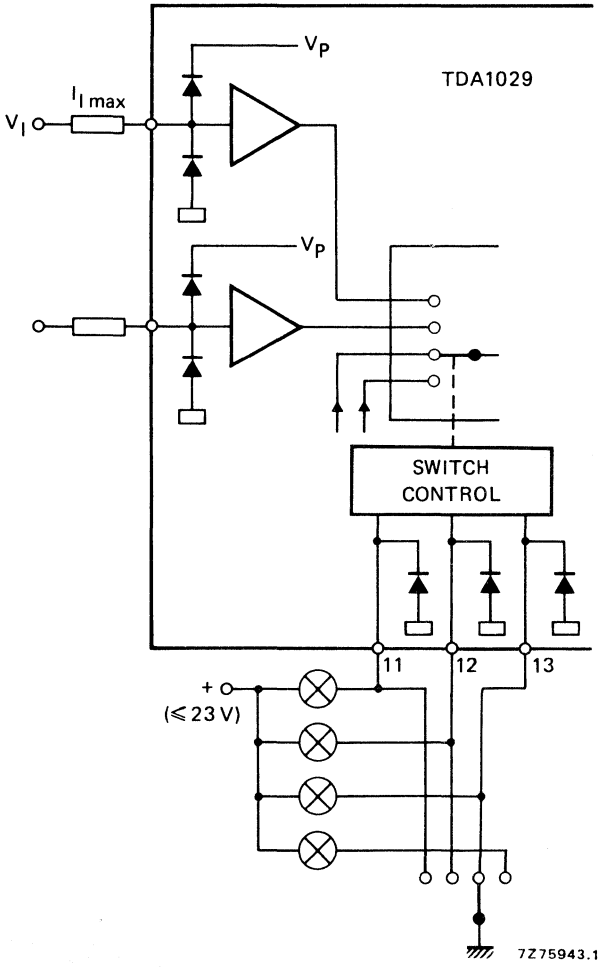


Fig. 7 Circuit diagram showing input protection and indication.

Unused signal inputs

Any unused inputs must be connected to a d.c. (bias) voltage, which is within the d.c. input voltage range; e.g. unused inputs can be connected directly to pin 10.

Circuits with standby operation

The control inputs (pins 11, 12 and 13) are high-ohmic at $V_{SH} \leqslant 20$ V ($I_{SH} \leqslant 1\ \mu A$), as well as, when the supply voltage (pin 14) is switched off.

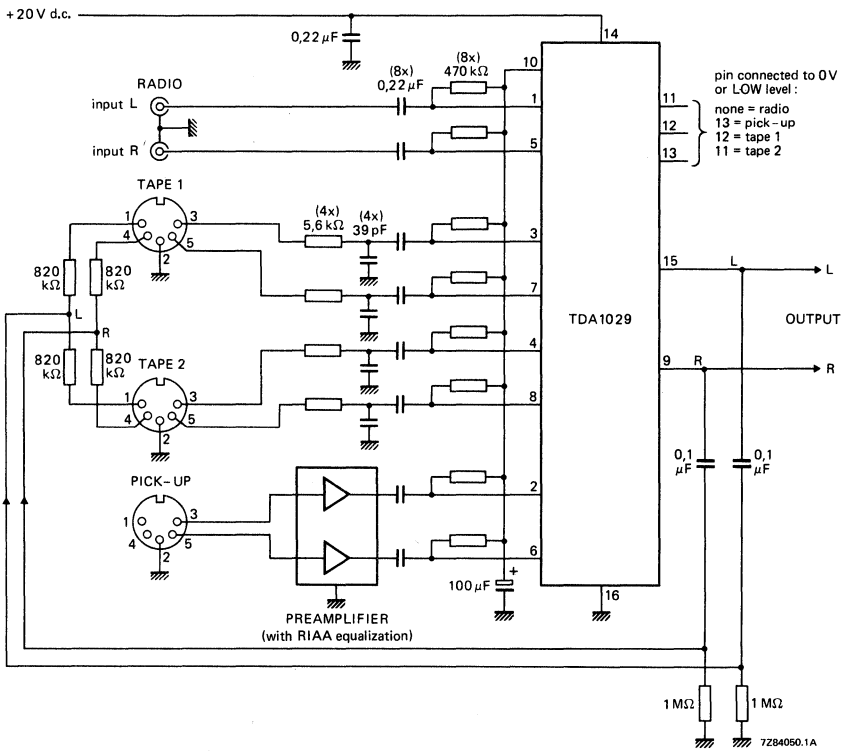


Fig. 8 TDA1029 connected as a four input stereo source selector.

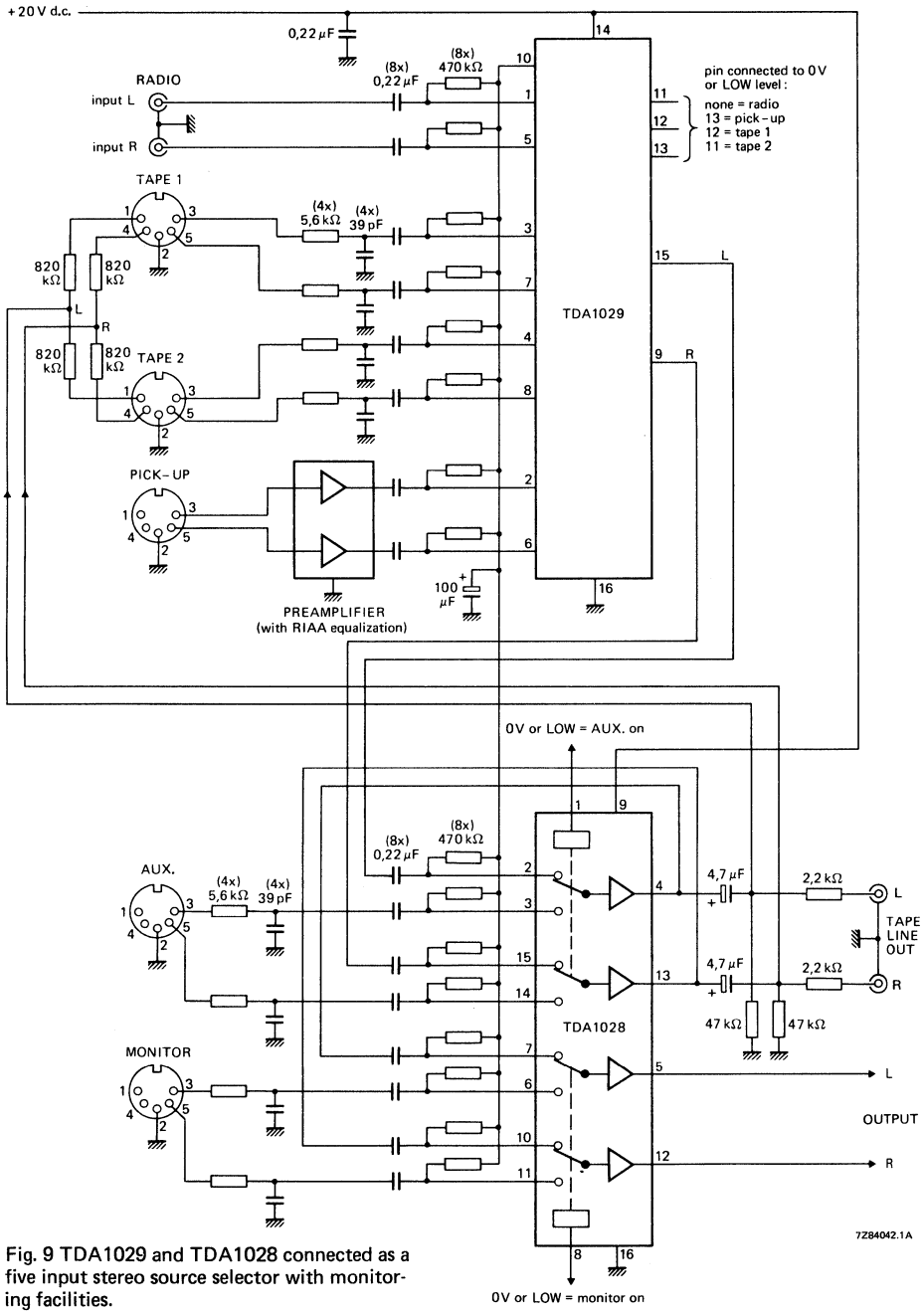


Fig. 9 TDA1029 and TDA1028 connected as a five input stereo source selector with monitoring facilities.

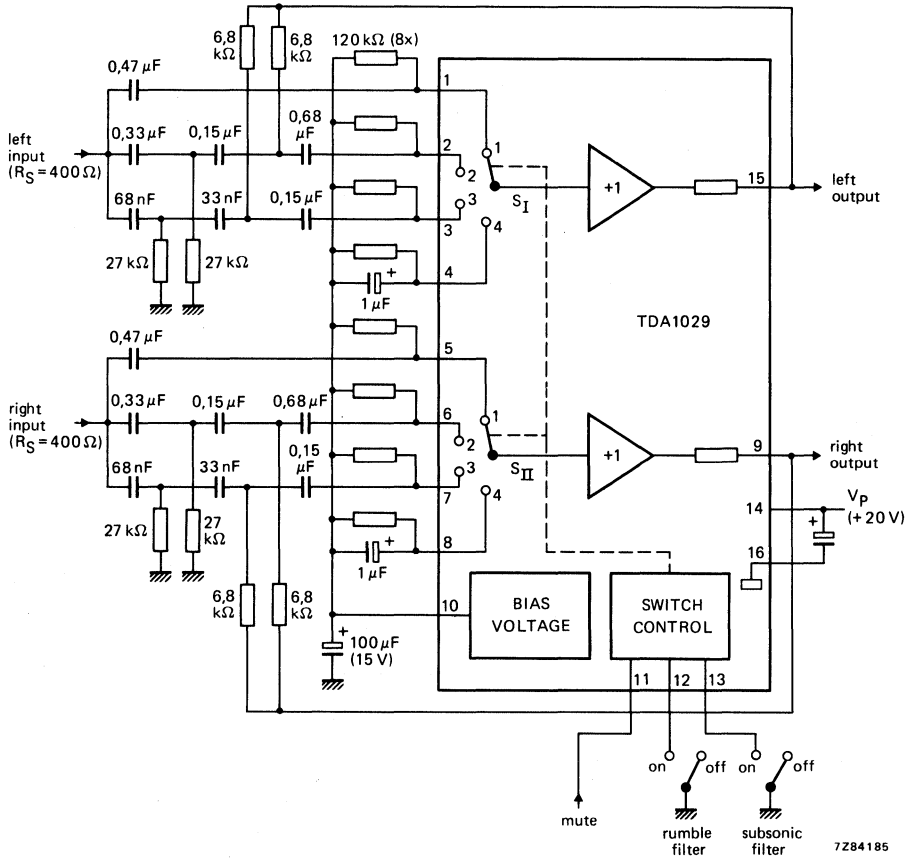


Fig. 10 TDA1029 connected as a third-order active high-pass filter with Butterworth response and component values chosen according to the method proposed by Fjällbrant. It is a four-function circuit which can select mute, rumble filter, subsonic filter and linear response.

Switch control

function	$V_{11\text{-}16}$	$V_{12\text{-}16}$	$V_{13\text{-}16}$
linear	H	H	H
subsonic filter 'on'	H	H	L
rumble filter 'on'	H	L	X
mute 'on'	L	X	X

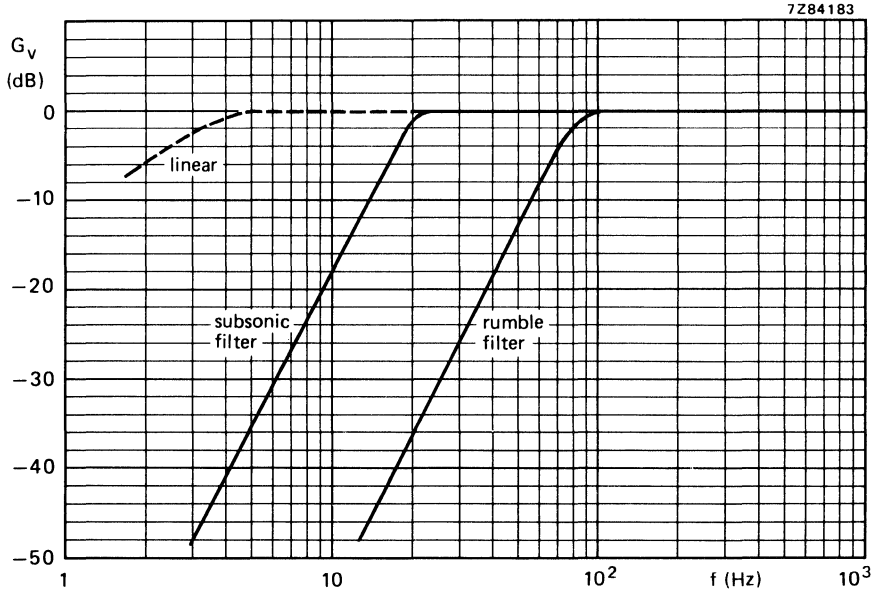


Fig. 11 Frequency response curves for the circuit of Fig. 10.

EAST-WEST CORRECTION DRIVER CIRCUIT

The TDA1082 is a monolithic integrated circuit driving east-west correction of colour tubes in television receivers. The circuit can be used for class-A and class-D operation and incorporates the following functions:

- differential input amplifier
- squaring stage
- differential output amplifier with driver stage
- protection stage with threshold
- switching off the correction during flyback
- voltage stabilizer

QUICK REFERENCE DATA

Supply voltage (pin 1)	V_P	typ.	12 V
Current consumption	I_P	typ.	17 mA
Total power dissipation	P_{tot}	max.	600 mW
Operating ambient temperature range	T_{amb}	−20 to +70	°C
Collector voltage drift external transistor	ΔV_C	typ.	0,7 V

PACKAGE OUTLINE

16-lead DIL; plastic (SOT-38).

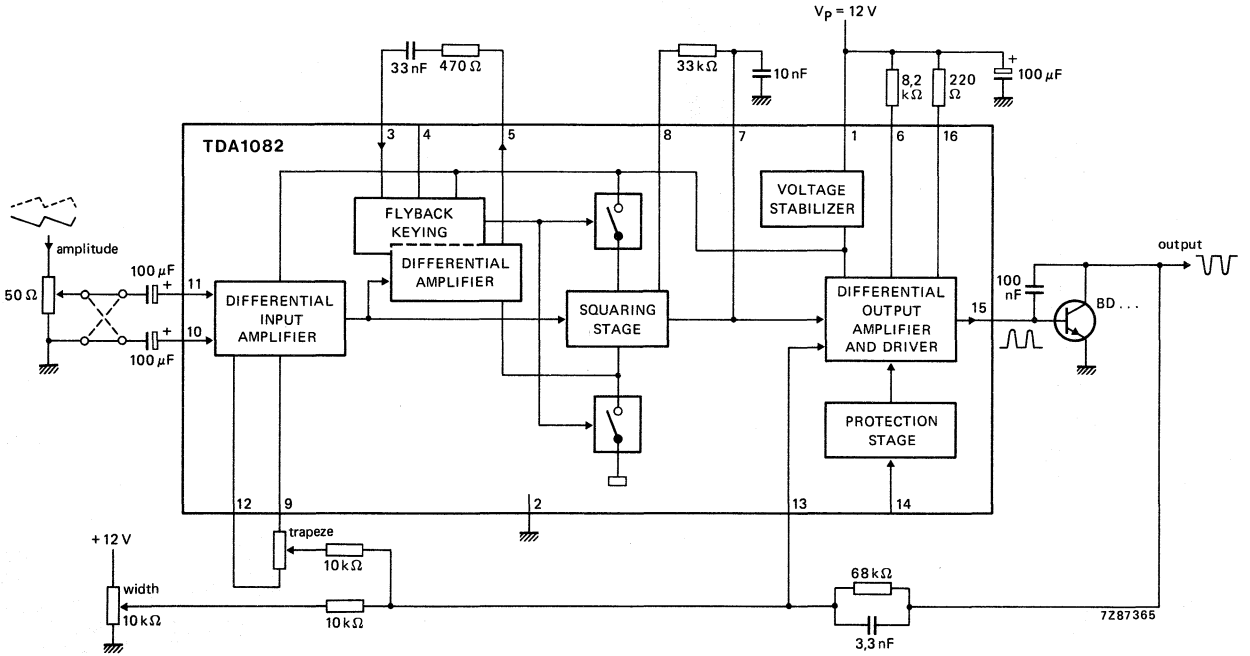


Fig. 1 Block diagram with external components (class-A operation). Also used as test circuit.

DEVELOPMENT DATA

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 1)	V_P	max.	16	V
Output current (pin 15)	$-I_O$	max.	50	mA
Total power dissipation	P_{tot}	max.	600	mW
Storage temperature range	T_{stg}	−25 to +150		°C
Operating ambient temperature range	T_{amb}	−20 to +70		°C

Voltages

with respect to ground (pin 2)	min.	max.	
Pins 1, 5, 7, 8, 9, 12, 13 and 16	0	16	V
Pins 3 and 4	0	–	V
Pins 10, 11 and 15	0	5	V

Currents

Pins 3, 4 and 6	–	5	mA
Pin 14	0	1,5	mA
Pins 15 and 16 ($-I_{15}$ and $+I_{16}$)	0	50	mA

CHARACTERISTICS

V_P = 12 V (range 10,5 to 14 V); T_{amb} = 25; measured in circuit Fig. 1 with colour tube A66-500X; unless otherwise specified

Supply

Voltage range	V_P	10,5 to	14	V
Voltage peak value	V_{PM}	max.	15	V
Current range	I_P	11 to	30	mA
Current typical value	I_P	typ.	17	mA

Sawtooth signal (pin 10 or 11)

Input voltage d.c. value	V_i	typ.	2,5	V
Input resistance	R_i	typ.	5,6	kΩ
		<	7,0	kΩ

Correcting signals (pin 13)

Input voltage d.c. value	V_{13}	typ.	0,6	V
Input current	I_{13}	typ.	0,5	mA

Flyback keying (pin 3)

Input current range	I_3	0,05 to	5	mA
Peak value, d = 5%	I_3	typ.	20	mA

Threshold (pin 14)

Input voltage at I_{14} = 200 μA for switching off the driver stage	V_i	typ.	8	V
		7,2 to	8,8	V

Output stage (pin 6)			
Generator current	I_6	typ.	1 mA
Flyback differential amplifier (pin 5)			
D.C. value output voltage	V_5	typ.	6 V
Output resistance	R_5	typ.	5,6 kΩ
Squaring stage (pin 7)			
D.C. value output voltage	V_7	typ.	6 V
Peak to peak value output voltage	$V_{7(p-p)}$	typ.	1,5 V
Output resistance	R_7	5,6 to typ.	9,4 kΩ 7,5 kΩ
Correction trapezoidal deformation (pins 9 and 12)			
D.C. voltage	$V_{9,12}$	typ.	5 V
Output resistance	$R_{9,12}$	typ.	7,5 kΩ
Driver output (pin 15)			
Output current	$-I_{15}$	<	50 mA
Drift of d.c. collector voltage			
Of external transistor in closed loop T_{amb} = 15 to 70 °C; V_{CO} = 8 V	ΔV_C	typ.	0,7 V

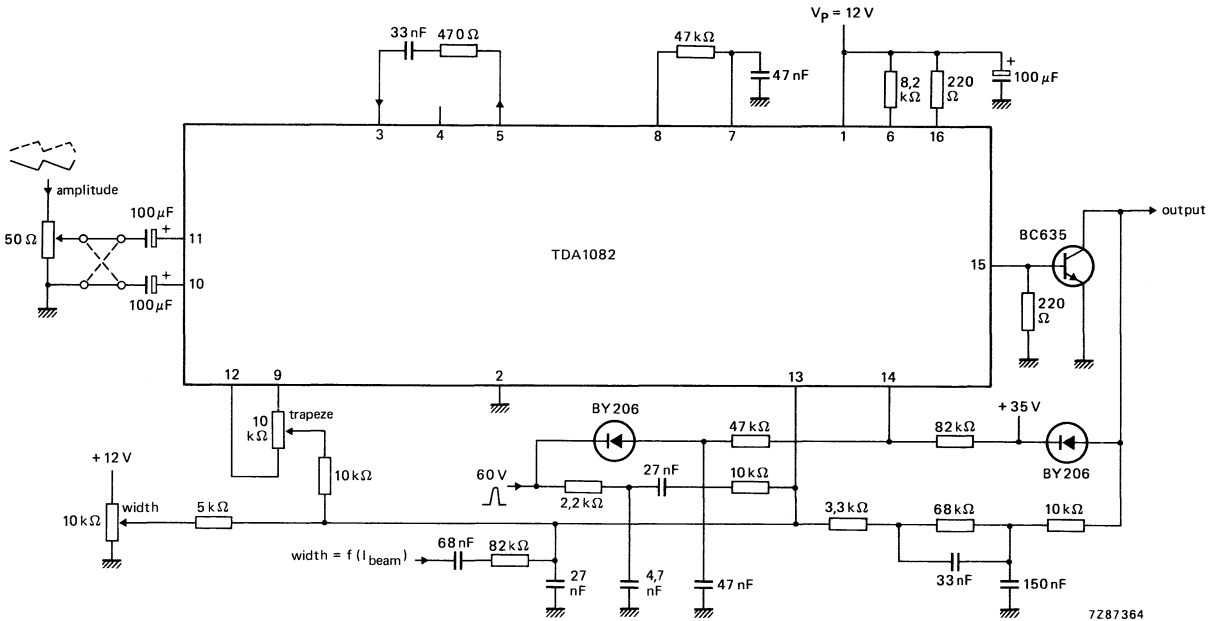


Fig. 2 Application circuit E-W-correction (class-D operation).

12 to 20 W HI-FI AUDIO POWER AMPLIFIER

The TDA1512 is a monolithic integrated hi-fi audio power amplifier designed for asymmetrical power supplies for mains-fed apparatus.
Special features are:

- Thermal protection
- Low intermodulation distortion
- Low transient intermodulation distortion
- Built-in output current limiter
- Low input offset voltage
- Output stage with low cross-over distortion
- Single in-line (SIL) power package

QUICK REFERENCE DATA

Supply voltage range	V_P		15 to 35 V
Total quiescent current at V_P = 25 V	I_{tot}	typ.	65 mA
Output power at d_{tot} = 0,7%			
sine-wave power			
V_P = 25 V; R_L = 4 Ω	P_o	typ.	13 W
V_P = 25 V; R_L = 8 Ω	P_o	typ.	7 W
music power			
V_P = 32 V; R_L = 4 Ω	P_o	typ.	21 W
V_P = 32 V; R_L = 8 Ω	P_o	typ.	12 W
Closed-loop voltage gain (externally determined)	G_c	typ.	30 dB
Input resistance (externally determined)	R_i	typ.	20 kΩ
Signal-to-noise ratio at P_o = 50 mW	S/N	typ.	72 dB
Supply voltage ripple rejection at f = 100 Hz	RR	typ.	50 dB

PACKAGE OUTLINES

TDA1512: 9-lead SIL; plastic power (SOT-131B).
TDA1512Q: 9-lead SIL-bent-to-DIL; plastic power (SOT-157B).

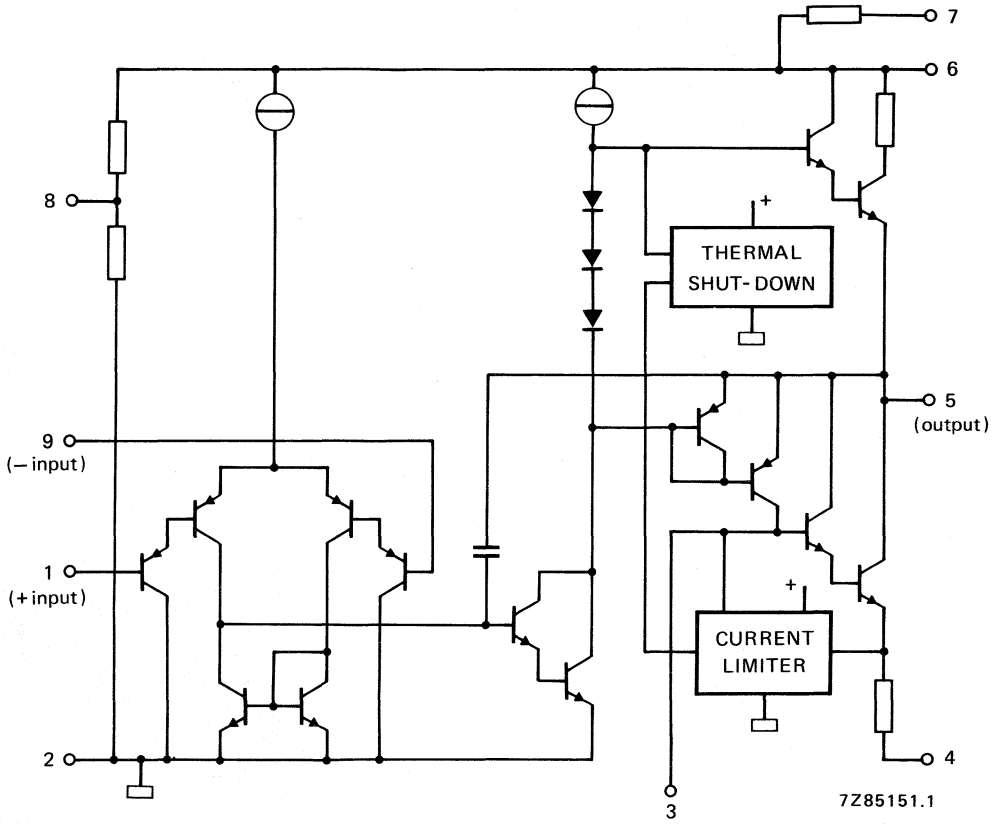


Fig. 1 Simplified internal circuit diagram.

PINNING

1. Non-inverting input
2. Input ground (substrate)
3. Compensation
4. Ground potential
5. Output
6. Positive supply (V_P)
7. Externally connected to pin 6
8. Ripple rejection
9. Inverting input (feedback)

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	35 V
Repetitive peak output current	I_{ORM}	max.	3,2 A
Non-repetitive peak output current	I_{OSM}	max.	5 A
Total power dissipation	see derating curve Fig. 2		
Storage temperature	T_{stg}		−55 to + 150 °C
Operating ambient temperature	T_{amb}		−25 to + 150 °C
A.C. short-circuit duration of load during full-load sine-wave drive $R_L = 0$; $V_P = 30$ V with $R_i = 4\ \Omega$	t_{sc}	max.	100 hours

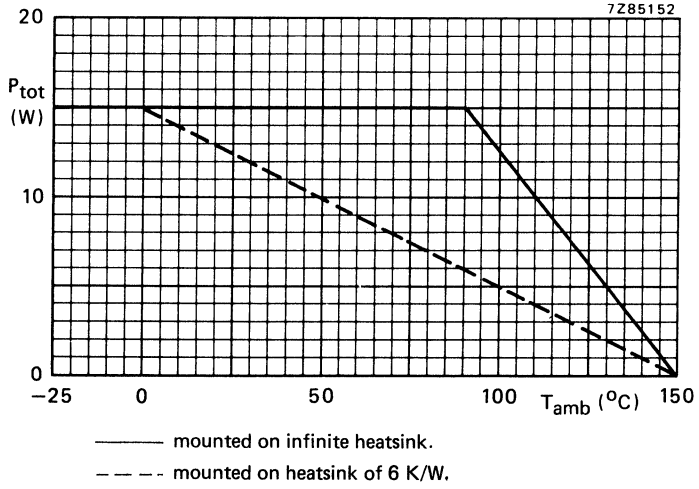


Fig. 2 Power derating curves.

THERMAL RESISTANCE

From junction to mounting base	$R_{th\ j\text{-}mb}$	typ.	3 K/W
		⩽	4 K/W

D.C. CHARACTERISTICS

Supply voltage range	V_P		15 to 35 V
Total quiescent current at V_P = 25 V	I_{tot}	typ.	65 mA

A.C. CHARACTERISTICS

V_P = 25 V; R_L = 4 Ω; f = 1 kHz; T_{amb} = 25 °C; measured in test circuit of Fig. 3; unless otherwise specified

Output power			
sine-wave power at d_{tot} = 0,7 %			
R_L = 4 Ω	P_o	typ.	13 W
R_L = 8 Ω	P_o	typ.	7 W
music power at V_P = 32 V			
R_L = 4 Ω; d_{tot} = 0,7 %	P_o	typ.	21 W
R_L = 4 Ω; d_{tot} = 10 %	P_o	typ.	25 W
R_L = 8 Ω; d_{tot} = 0,7 %	P_o	typ.	12 W
R_L = 8 Ω; d_{tot} = 10 %	P_o	typ.	15 W
Power bandwidth; −1,5 dB; d_{tot} = 0,7%	B		40 Hz to 16 kHz
Voltage gain			
open-loop	G_o	typ.	74 dB
closed-loop	G_c	typ.	30 dB
Input resistance (pin 1)	R_i	>	100 kΩ
Input resistance of test circuit (Fig. 3)	R_i	typ.	20 kΩ
Input sensitivity			
for P_o = 50 mW	V_i	typ.	16 mV
for P_o = 10 W	V_i	typ.	210 mV
Signal-to-noise ratio			
at P_o = 50 mW; R_S = 2 kΩ; f = 20 Hz to 20 kHz; unweighted	S/N	>	68 dB
weighted; measured according to IEC 173 (A-curve)	S/N	typ.	76 dB
Ripple rejection at f = 100 Hz	RR	typ.	50 dB
Total harmonic distortion at P_o = 10 W	d_{tot}	typ. <	0,1 % 0,3 %
Output resistance (pin 5)	R_o	typ.	0,1 Ω

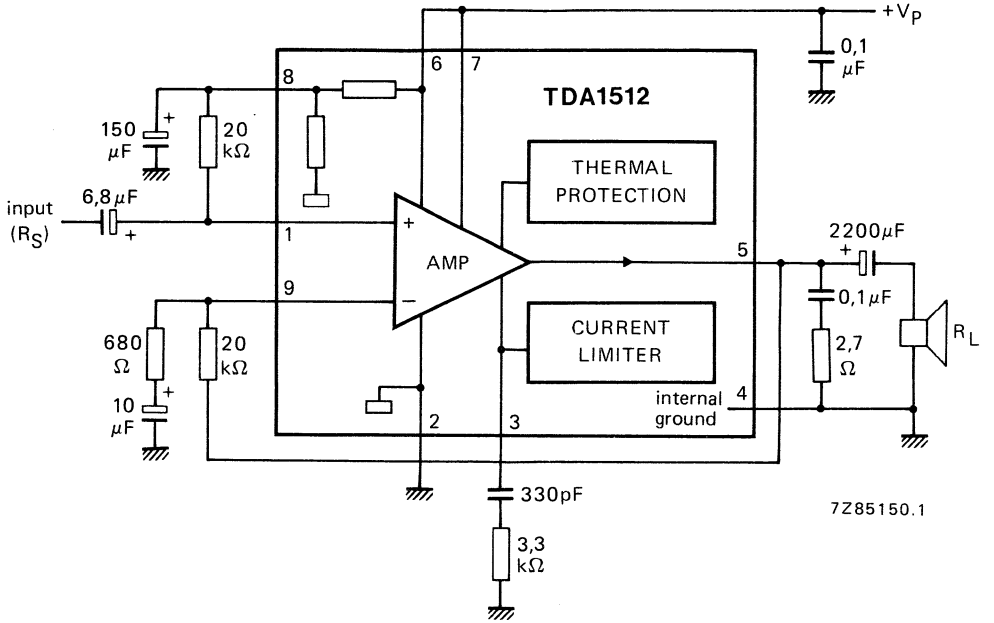


Fig. 3 Test circuit.

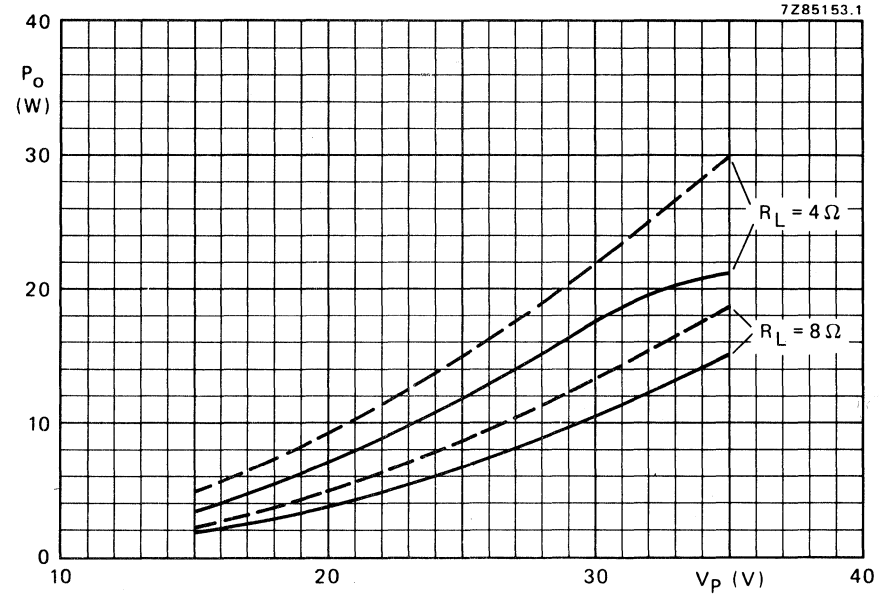


Fig. 4 Output power as a function of the supply voltage; f = 1 kHz;
——— d_{tot} = 0,7 %; – – – d_{tot} = 10 %.

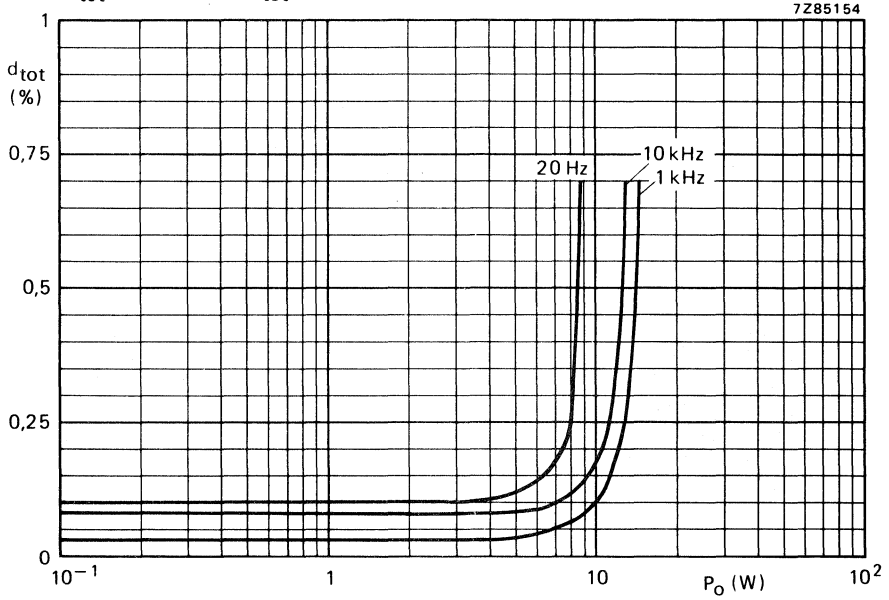


Fig. 5 Total harmonic distortion as a function of the output power.

20 W HI-FI AUDIO POWER AMPLIFIER

The TDA1520 is a monolithic integrated hi-fi audio power amplifier designed for asymmetrical or symmetrical power supplies for mains-fed apparatus.
Special features are:

- Thermal protection
- Very low intermodulation distortion
- Very low transient intermodulation distortion
- Built-in output current limiter
- Low input offset voltage
- Output stage with low cross-over distortion
- Single in-line (SIL) power package
- A.C. short-circuit protected

QUICK REFERENCE DATA

Supply voltage range	V_P		15 to 40	V
Total quiescent current at V_P = 33 V	I_{tot}	typ.	54	mA
Output power at d_{tot} = 0,5% sine-wave power				
V_P = 33 V; R_L = 4 Ω	P_o	typ.	22	W
V_P = 33 V; R_L = 4 Ω	P_o	>	16	W
V_P = 33 V; R_L = 8 Ω	P_o	typ.	11	W
Closed-loop voltage gain (externally determined)	G_c	typ.	30	dB
Input resistance (externally determined by R_{8-1})	R_i	typ.	20	kΩ
Signal-to-noise ratio at P_o = 50 mW	S/N	typ.	75	dB
Supply voltage ripple rejection at f = 100 Hz	RR	typ.	60	dB

PACKAGE OUTLINE

TDA1520 : 9-lead SIL; plastic power (SOT-131A).
TDA1520Q: 9-lead SIL-bent-to-DIL; plastic power (SOT-157A).

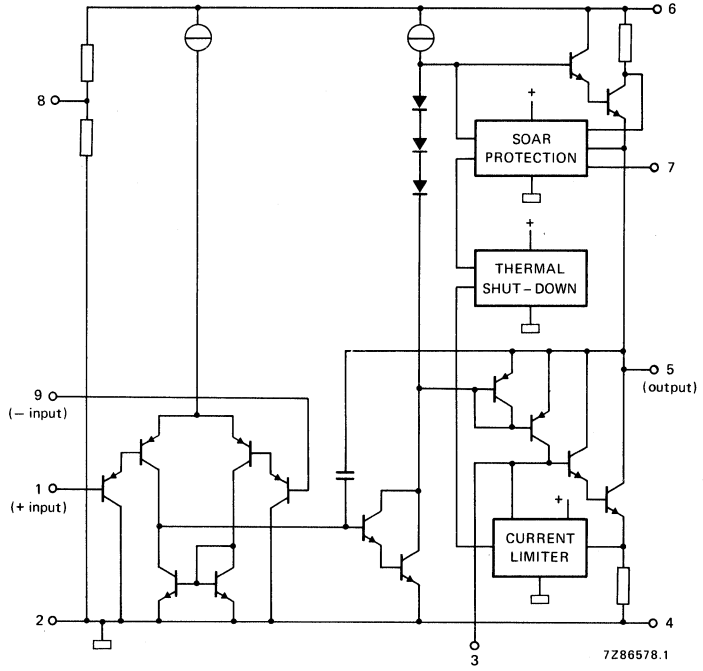


Fig. 1 Simplified internal circuit diagram.

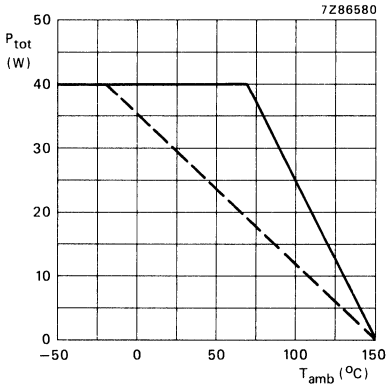
PINNING

1. Non-inverting input
2. Input ground (substrate)
3. Compensation
4. Negative supply (ground)
5. Output
6. Positive supply (V_P)
7. Internally connected
8. Ripple rejection
9. Inverting input (feedback)

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	44 V
Repetitive peak output current	I_{ORM}	max.	4 A
Non-repetitive peak output current	I_{OSM}	max.	5 A
Total power dissipation	see derating curve Fig. 2		
Storage temperature	T_{stg}	−55 to + 150	°C
Operating ambient temperature	T_{amb}	−25 to + 150	°C
A.C. short-circuit duration of load during full-load sine-wave drive $R_L = 0$; $V_P = 28$ V with $R_i = 4\ \Omega$ and $f > 20$ Hz	t_{sc}	max.	1 hour ←



——— mounted on infinite heatsink.
– – – mounted on heatsink of 2,3 K/W.

Fig. 2 Power derating curves.

THERMAL RESISTANCE

From junction to mounting base	$R_{th\ j\text{-}mb}$	⩽	2 K/W

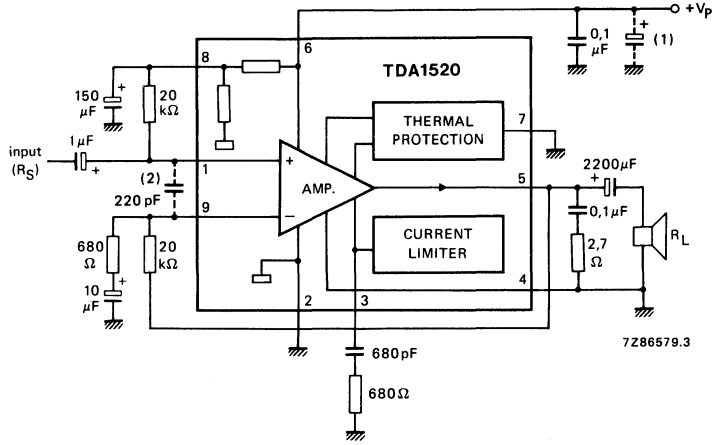
D.C. CHARACTERISTICS

Supply voltage range	V_P	15 to 40	V
Total quiescent current at V_P = 33 V	I_{tot}	22 to 105	mA
		typ. 54	mA

A.C. CHARACTERISTICS

V_P = 33 V; R_L = 4 Ω; f = 1 kHz; T_{amb} = 25 °C; measured in test circuit of Fig. 3; unless otherwise specified

Output power			
sine-wave power at d_{tot} = 0,5%			
R_L = 4 Ω	P_o	typ. 22	W
R_L = 4 Ω	P_o	> 16	W
R_L = 8 Ω	P_o	typ. 11	W
Power bandwidth; −3 dB; d_{tot} = 0,5%	B	20 Hz to 20	kHz
Voltage gain			
open-loop	G_o	typ. 74	dB
closed-loop	G_c	typ. 30	dB
Input resistance (pin 1)	R_i	> 1	MΩ
Input resistance of test circuit (Fig. 3)	R_i	typ. 20	kΩ
Input sensitivity			
for P_o = 50 mW	V_i	typ. 16	mV
for P_o = 16 W	V_i	typ. 260	mV
Signal-to-noise ratio			
at P_o = 50 mW; R_S = 2 kΩ; f = 20 Hz to 20 kHz; unweighted	S/N	typ. 75	dB
weighted; measured according to IEC 179 (A-curve)	S/N	typ. 80	dB
Supply voltage ripple rejection at f = 100 Hz	RR	typ. 65	dB
Total harmonic distortion at P_o = 16 W	d_{tot}	typ. 0,01	%
Output resistance (pin 5)	R_o	typ. 0,01	Ω
	R_o	< 0,1	Ω



(1) Belongs to power supply.
(2) In application to improve radio interference suppression.

Fig. 3 Test circuit/basic application circuit.

20 W HI-FI AUDIO POWER AMPLIFIER

GENERAL DESCRIPTION

The TDA1520A is a monolithic integrated hi-fi audio power amplifier designed for asymmetrical or symmetrical power supplies for mains-fed apparatus.

Features

- Low input offset voltage
- Output stage with low cross-over distortion
- Single in-line (SIL) power package
- A.C. short-circuit protected
- Very low internal thermal resistance
- Thermal protection
- Very low intermodulation distortion
- Very low transient intermodulation distortion
- Complete SOAR protection

QUICK REFERENCE DATA

Supply voltage range	V_P	15 to 50	V
Total quiescent current at V_P = 33 V	I_{tot}	typ. 70	mA
Output power at d_{tot} = 0,5% sine-wave power			
V_P = 33 V; R_L = 4 Ω	P_o	typ. 22	W
V_P = 33 V; R_L = 4 Ω	P_o	> 20	W
V_P = 42 V; R_L = 8 Ω	P_o	typ. 20	W
Closed-loop voltage gain (externally determined)	G_c	typ. 30	dB
Input resistance (externally determined by R_{8-1})	R_i	typ. 20	kΩ
Signal-to-noise ratio at P_o = 50 mW	S/N	typ. 76	dB
Supply voltage ripple rejection at f = 100 Hz	RR	typ. 60	dB

PACKAGE OUTLINE

TDA1520A : 9-lead SIL; plastic power (SOT-131A).
TDA1520AQ: 9-lead SIL-bent-to-DIL; plastic power (SOT-157A).

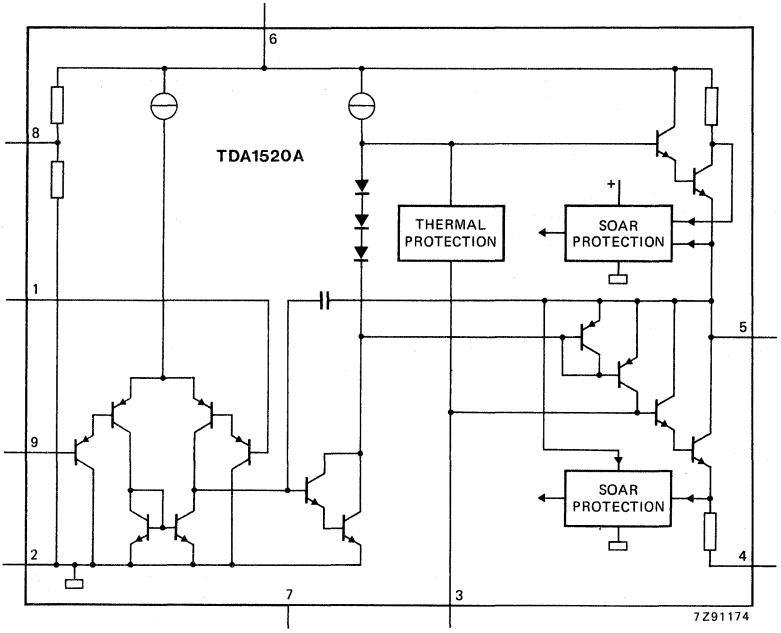


Fig. 1 Simplified internal circuit diagram.

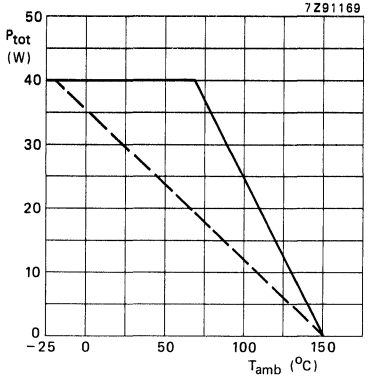
PINNING

1. Non-inverting input
2. Input ground (substrate)
3. Compensation
4. Negative supply (ground)
5. Output
6. Positive supply (V_P)
7. Not connected
8. Ripple rejection
9. Inverting input (feedback)

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	50 V
Repetitive peak output current	I_{ORM}	max.	4 A
Non-repetitive peak output current	I_{OSM}	max.	5 A
Total power dissipation	see derating curve Fig. 2		
Storage temperature	T_{stg}	−55 to + 150	°C
Operating ambient temperature	T_{amb}	−25 to + 150	°C
Duration of a.c. short-circuit of load (R_L = 0 Ω) during full-load sine-wave drive at: V_S = ± 20 V (symmetrical) and R_{supply} = 0 Ω; or V_S = 35 V (asymmetrical) and $R_{supply} \geqslant 4$ Ω	t_{sc}	max.	100 hours



——— mounted on infinite heatsink.
– – – mounted on heatsink of 2,3 K/W.

Fig. 2 Power derating curves.

THERMAL RESISTANCE

From junction to mounting base	$R_{th\ j\text{-}mb}$	⩽	2 K/W

D.C. CHARACTERISTICS

Supply voltage range	V_P	15 to 50	V
Total quiescent current at V_P = 33 V	I_{tot}	typ. 70 $\leqslant$ 105	mA mA
Minimum guaranteed output current (peak value)	I_{ORM}	$\geqslant$ 3,2	A

A.C. CHARACTERISTICS

V_P = 33 V; R_L = 4 Ω; f = 1 kHz; T_{amb} = 25 °C; measured in test circuit of Fig. 3; unless otherwise specified

Output power			
sine-wave power at d_{tot} = 0,5%			
R_L = 4 Ω } (Fig. 4)	P_o	typ. 22	W
R_L = 4 Ω } (Fig. 4)	P_o	> 20	W
R_L = 8 Ω; V_P = 42 V } (Fig. 4)	P_o	typ. 20	W
Power bandwidth at d_{tot} = 0,5% from P_o = 50 mW to 10 W	B	20 Hz to 20	kHz
Voltage gain			
open-loop	G_o	typ. 74	dB
closed-loop	G_c	typ. 30	dB
Internal resistance of pin 1 (at $R_{1-8} = \infty$)	R_i	> 1	MΩ
Input resistance of test circuit at pin 1 (Fig. 3)	R_i	typ. 20	kΩ
Input sensitivity			
for P_o = 16 W	V_i	typ. 260	mV
Signal-to-noise ratio			
at P_o = 50 mW; R_{source} = 2 kΩ			
f = 20 Hz to 20 kHz; unweighted	S/N	typ. 76	dB
weighted; measured according to IEC 179 (A-curve)	S/N	typ. 80	dB
Ripple rejection at f = 100 Hz; R_S = 0 Ω	RR	typ. 60	dB
Total harmonic distortion at P_o = 16 W	d_{tot}	typ. 0,01	%
Output resistance (pin 5)	R_o	typ. 0,01	Ω
Input offset voltage	V_{5-8}	typ. 1 < 100	mV mV
Transient intermodulation distortion			
at P_o = 10 W	d_{TIM}	typ. 0,01	%
Intermodulation distortion at P_o = 10 W	d_{IM}	typ. 0,01	%
Slew rate	SR	typ. 9	V/μs

APPLICATION INFORMATION

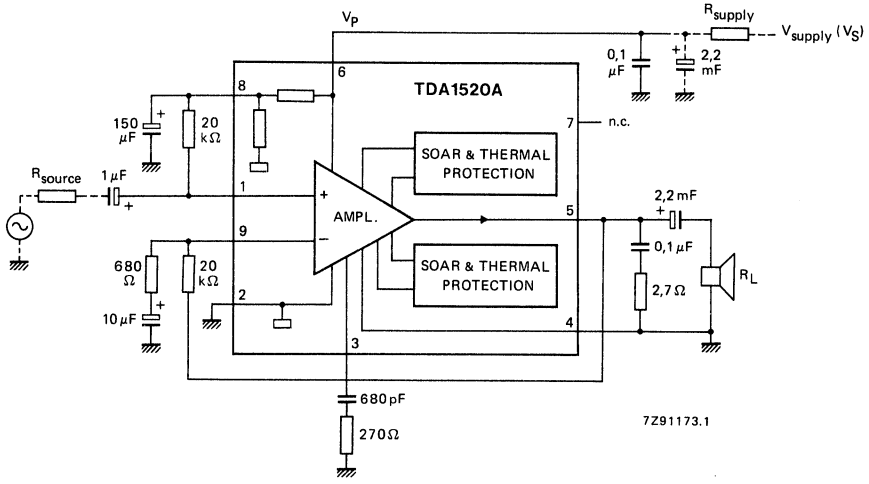


Fig. 3 Test and application circuit.

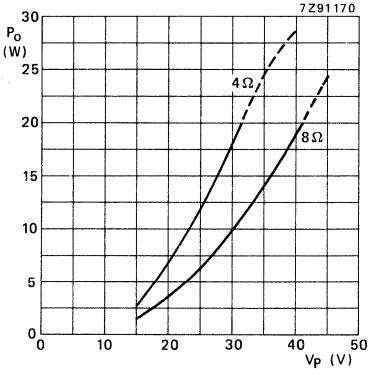


Fig. 4 Output power (P_o) versus supply voltage (V_p) at f = 1 kHz, d_{tot} = 0,5%, G_v = 30 dB.

APPLICATION INFORMATION (continued)

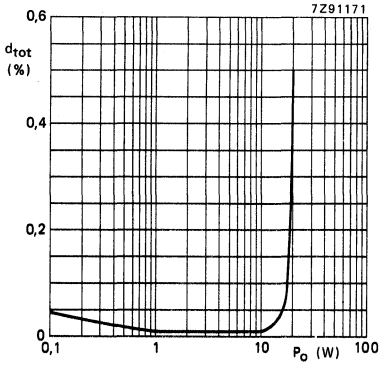


Fig. 5 Total harmonic distortion (d_{tot}) versus output power (P_o) at V_p = 33 V, R_L = 4 Ω, f = 1 kHz.

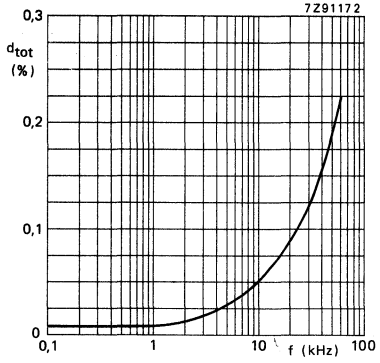


Fig. 6 Total harmonic distortion (d_{tot}) versus operating frequency (f) at V_p = 33 V, R_L = 4 Ω, P_o = 10 W (constant).

STEREO-TONE/VOLUME CONTROL CIRCUIT

GENERAL DESCRIPTION

The device is designed as an active stereo-tone/volume control for car radios, TV receivers and mains-fed equipment. It includes functions for bass and treble control, volume control with built-in contour (can be switched off) and balance. All these functions can be controlled by d.c. voltages or by single linear potentiometers.

Features

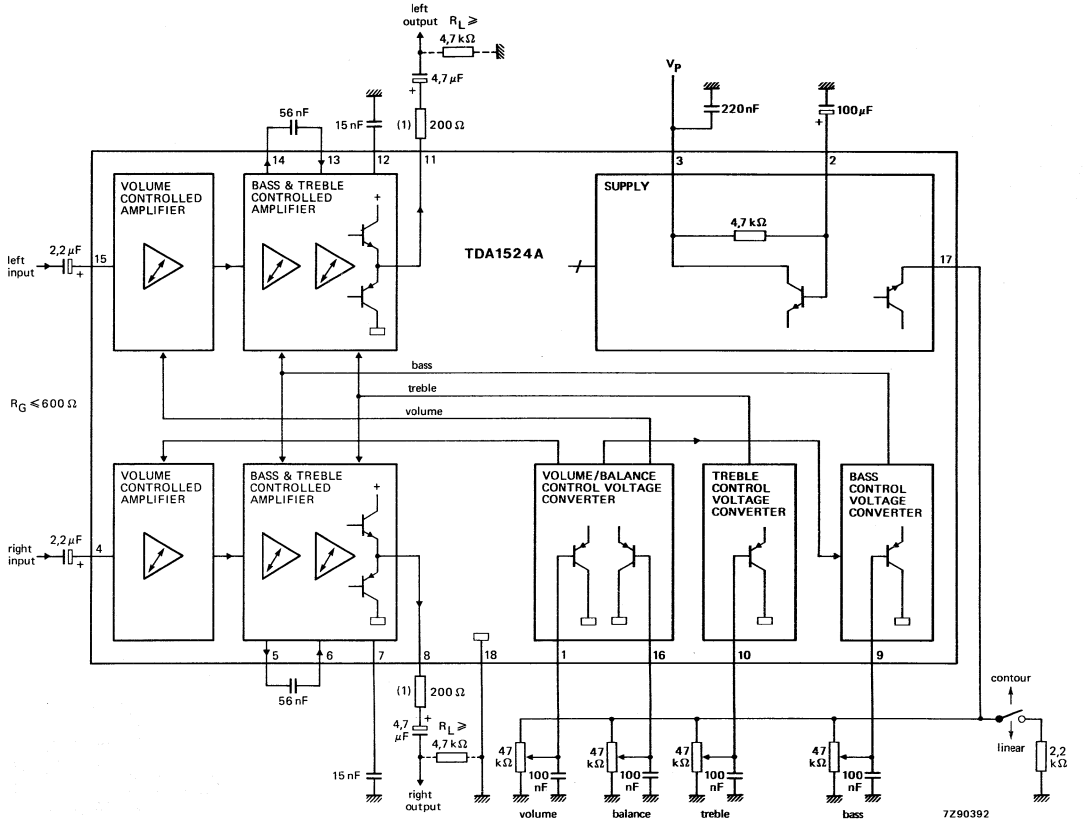
- Few external components necessary
- Low noise due to internal gain
- Bass emphasis can be increased by a double-pole low-pass filter
- Wide power supply voltage range

QUICK REFERENCE DATA

Supply voltage (pin 3)	$V_P = V_{3\text{-}18}$	typ.	12 V
Supply current (pin 3)	$I_P = I_3$	typ.	35 mA
Maximum input signal with d.c. feedback (r.m.s. value)	$V_{i(rms)}$	typ.	2,5 V
Maximum output signal with d.c. feedback (r.m.s. value)	$V_{o(rms)}$	typ.	3 V
Volume control range	G_V		−80 to + 21,5 dB
Bass control range at 40 Hz	ΔG_V	typ.	± 15 dB
Treble control range at 16 kHz	ΔG_V	typ.	± 15 dB
Total harmonic distortion	THD	typ.	0,3 %
Output noise voltage (unweighted; r.m.s. value) at f = 20 Hz to 20 kHz; V_P = 12 V;			
for max. voltage gain	$V_{no(rms)}$	typ.	310 μV
for voltage gain G_V = −40 dB	$V_{no(rms)}$	typ.	100 μV
Channel separation at G_V = −20 to + 21,5 dB	α_{cs}	typ.	60 dB
Tracking between channels at G_V = −20 to + 26 dB	ΔG_V	max.	2,5 dB
Ripple rejection at 100 Hz	RR	typ.	50 dB
Supply voltage range (pin 3)	$V_P = V_{3\text{-}18}$		7,5 to 16,5 V
Operating ambient temperature range	T_{amb}		−30 to + 80 °C

PACKAGE OUTLINE

18-lead DIL; plastic (SOT-102HE).



(1) Series resistor is recommended in the event of the capacitive loads exceeding 200 pF.

Fig. 1 Block diagram and application circuit with single-pole filter.

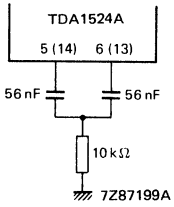


Fig. 2 Double-pole low-pass filter for improved bass-boost.

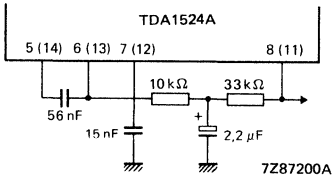


Fig. 3 D.C. feedback with filter network for improved signal handling.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 3)	$V_P = V_{3-18}$	max.	20 V
Total power dissipation	P_{tot}	max.	1200 mW
Storage temperature range	T_{stg}		−55 to + 150 °C
Operating ambient temperature range	T_{amb}		−30 to + 80 °C

D.C. CHARACTERISTICS

$V_P = V_{3-18} = 12$ V; $T_{amb} = 25$ °C; measured in Fig. 1; $R_G \leqslant 600\ \Omega$; $R_L \geqslant 4{,}7$ kΩ; $C_L \leqslant 200$ pF; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply (pin 3)					
Supply voltage	$V_P = V_{3-18}$	7,5	–	16,5	V
Supply current					
at $V_P = 8{,}5$ V	$I_P = I_3$	19	27	35	mA
at $V_P = 12$ V	$I_P = I_3$	25	35	45	mA
at $V_P = 15$ V	$I_P = I_3$	30	43	56	mA
D.C. input levels (pins 4 and 15)					
at $V_P = 8{,}5$ V	$V_{4,15-18}$	3,8	4,25	4,7	V
at $V_P = 12$ V	$V_{4,15-18}$	5,3	5,9	6,6	V
at $V_P = 15$ V	$V_{4,15-18}$	6,5	7,3	8,2	V
D.C. output levels (pins 8 and 11) under all control voltage conditions with d.c. feedback (Fig. 3)					
at $V_P = 8{,}5$ V	$V_{8,11-18}$	3,3	4,25	5,2	V
at $V_P = 12$ V	$V_{8,11-18}$	4,6	6,0	7,4	V
at $V_P = 15$ V	$V_{8,11-18}$	5,7	7,5	9,3	V
Pin 17					
Internal potentiometer supply voltage at $V_P = 8{,}5$ V	V_{17-18}	3,5	3,75	4,0	V
Contour on/off switch (control by I_{17})					
contour (switch open)	$-I_{17}$	–	–	0,5	mA
linear (switch closed)	$-I_{17}$	1,5	–	10	mA
Application without internal potentiometer supply voltage at $V_P \geqslant 10{,}8$ V (contour cannot be switched off)					
Voltage range forced to pin 17	V_{17-18}	4,5	–	$V_P/2-V_{BE}$	V
D.C. control voltage range for volume, bass, treble and balance (pins 1, 9, 10 and 16 respectively)					
at $V_{17-18} = 5$ V	$V_{1,9,10,16}$	1,0	–	4,25	V
using internal supply	$V_{1,9,10,16}$	0,25	–	3,8	V
Input current of control inputs (pins 1, 9, 10 and 16)	$-I_{1,9,10,16}$	–	–	5	μA

A.C. CHARACTERISTICS

$V_P = V_{3-18} = 8{,}5$ V; $T_{amb} = 25\ ^oC$; measured in Fig. 1; contour switch closed (linear position); volume, balance, bass, and treble controls in mid-position; $R_G \leqslant 600\ \Omega$; $R_L \geqslant 4{,}7$ kΩ; $C_L \leqslant 200$ pF; f = 1 kHz; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Control range					
Max. gain of volume (Fig. 5)	$G_{V\ max}$	20,5	21,5	23	dB
Volume control range; $G_{V\ max}/G_{V\ min}$	ΔG_V	90	100	–	dB
Balance control range; $G_V = 0$ dB (Fig. 6)	ΔG_V	–	–40	–	dB
Bass control range at 40 Hz (Fig. 7)	ΔG_V	±12	±15	–	dB
Treble control range at 16 kHz (Fig. 8)	ΔG_V	±12	±15	–	dB
Contour characteristics		see Figs 9 and 10			
Signal inputs, outputs					
Input resistance; pins 4 and 15 (note 1)					
at gain of volume control: $G_V = 20$ dB	$R_{i4,15}$	10	–	–	kΩ
$G_V = -40$ dB	$R_{i4,15}$	–	160	–	kΩ
Output resistance (pins 8 and 11)	$R_{o8,11}$	–	–	300	Ω
Signal processing					
Power supply ripple rejection					
at $V_{P(rms)} \leqslant 200$ mV; f = 100 Hz; $G_V = 0$ dB	RR	35	50	–	dB
Channel separation (250 Hz to 10 kHz)					
at $G_V = -20$ to + 21,5 dB	α_{cs}	46	60	–	dB
Spread of volume control with					
constant control voltage $V_{1-18} = 0{,}5\ V_{17-18}$	ΔG_V	–	–	±3	dB
Gain tolerance between left and right					
channel $V_{16-18} = V_{1-18} = 0{,}5\ V_{17-18}$	$\Delta G_{V,L-R}$	–	–	1,5	dB
Tracking between channels					
for $G_V = 21{,}5$ to -26 dB					
f = 250 Hz to 6,3 kHz; balance adjusted at					
$G_V = 10$ dB	ΔG_V	–	–	2,5	dB

A.C. CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Signal handling with d.c. feedback (Fig. 3)					
Input signal handling					
at V_P = 8,5 V; THD = 0,5%; f = 1 kHz (r.m.s. value)	$V_{i(rms)}$	1,4	–	–	V
at V_P = 8,5 V; THD = 0,7%; f = 1 kHz (r.m.s. value)	$V_{i(rms)}$	1,8	2,4	–	V
at V_P = 12 V; THD = 0,5%; f = 40 Hz to 16 kHz (r.m.s. value)	$V_{i(rms)}$	1,4	–	–	V
at V_P = 12 V; THD = 0,7%; f = 40 Hz to 16 kHz (r.m.s. value)	$V_{i(rms)}$	2,0	3,2	–	V
at V_P = 15 V; THD = 0,5%; f = 40 Hz to 16 kHz (r.m.s. value)	$V_{i(rms)}$	1,4	–	–	V
at V_P = 15 V; THD = 0,7%; f = 40 Hz to 16 kHz (r.m.s. value)	$V_{i(rms)}$	2,0	3,2	–	V
Output signal handling (note 2 and note 3)					
at V_P = 8,5 V; THD = 0,5%; f = 1 kHz (r.m.s. value)	$V_{o(rms)}$	1,8	2,0	–	V
at V_P = 8,5 V; THD = 10%; f = 1 kHz (r.m.s. value)	$V_{o(rms)}$	–	2,2	–	V
at V_P = 12 V; THD = 0,5%; f = 40 Hz to 16 kHz (r.m.s. value)	$V_{o(rms)}$	2,5	3,0	–	V
at V_P = 15 V; THD = 0,5%; f = 40 Hz to 16 kHz (r.m.s. value)	$V_{o(rms)}$	–	3,5	–	V
Noise performance (V_P = 8,5 V)					
Output noise voltage (unweighted; Fig. 15)					
at f = 20 Hz to 20 kHz (r.m.s. value)					
for maximum voltage gain (note 4)	$V_{no(rms)}$	–	260	–	μV
for G_v = −3 dB (note 4)	$V_{no(rms)}$	–	70	140	μV
Output noise voltage; weighted as DIN 45405 of 1981, CCIR recommendation 468-2 (peak value)					
for maximum voltage gain (note 4)	$V_{no(m)}$	–	890	–	μV
for maximum emphasis of bass and treble (contour off; G_v = −40 dB)	$V_{no(m)}$	–	360	–	μV
Noise performance (V_P = 12 V)					
Output noise voltage (unweighted; Fig. 15)					
at f = 20 Hz to 20 kHz (r.m.s. value; note 5)					
for maximum voltage gain (note 4)	$V_{no(rms)}$	–	310	–	μV
for G_v = −16 dB (note 4)	$V_{no(rms)}$	–	100	200	μV
Output noise voltage; weighted as DIN 45405 of 1981, CCIR recommendation 468-2 (peak value)					
for maximum voltage gain (note 4)	$V_{no(m)}$	–	940	–	μV
for maximum emphasis of bass and treble (contour off; G_v = −40 dB)	$V_{no(m)}$	–	400	–	μV

parameter	symbol	min.	typ.	max.	unit
Noise performance (V_P = 15 V)					
Output noise voltage (unweighted; Fig. 15) at f = 20 Hz to 20 kHz (r.m.s. value; note 5)					
for maximum voltage gain (note 4)	$V_{no(rms)}$	–	350	–	μV
for G_v = 16 dB (note 4)	$V_{no(rms)}$	–	110	220	μV
Output noise voltage; weighted as DIN 45405 of 1981, CCIR recommendation 468-2 (peak value)					
for maximum voltage gain (note 4)	$V_{no(m)}$	–	980	–	μV
for maximum emphasis of bass and treble (contour off; G_v = −40 dB)	$V_{no(m)}$	–	420	–	μV

Notes to characteristics

1. Equation for input resistance (see also Fig. 4)

$$R_i = \frac{160\ k\Omega}{1 + G_v}\ ;\ G_{v\ max} = 12.$$

2. Frequencies below 200 Hz and above 5 kHz have reduced voltage swing, the reduction at 40 Hz and at 16 kHz is 30%.
3. In the event of bass boosting the output signal handling is reduced. The reduction is 1 dB for maximum bass boost.
4. Linear frequency response.
5. For peak values add 4,5 dB to r.m.s. values.

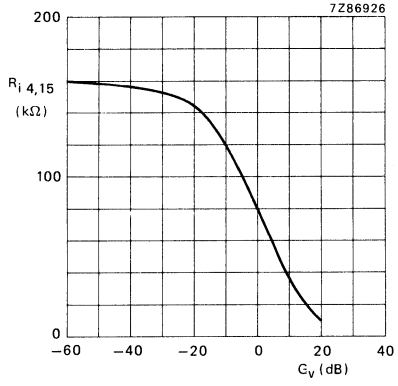


Fig. 4 Input resistance (R_i) as a function of gain of volume control (G_v). Measured in Fig. 1.

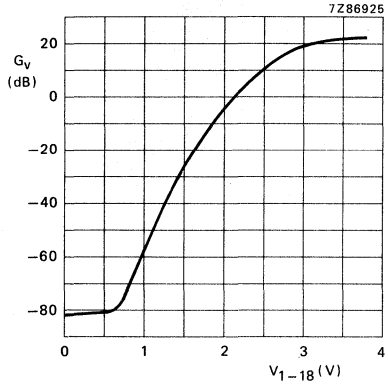


Fig. 5 Volume control curve; voltage gain (G_V) as a function of control voltage (V_{1-18}). Measured in Fig. 1 (internal potentiometer supply from pin 17 used); V_P = 8,5 V; f = 1 kHz.

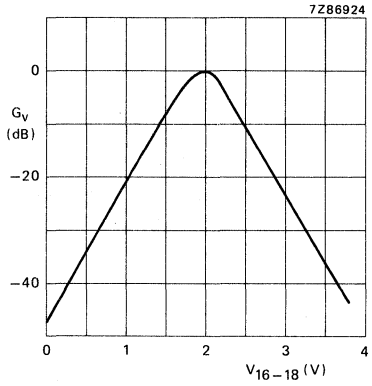


Fig. 6 Balance control curve; voltage gain (G_V) as a function of control voltage (V_{16-18}). Measured in Fig. 1 (internal potentiometer supply from pin 17 used); V_P = 8,5 V.

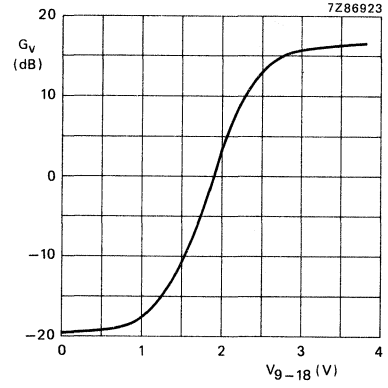


Fig. 7 Bass control curve; voltage gain (G_V) as a function of control voltage (V_{9-18}). Measured in Fig. 1 with single-pole filter (internal potentiometer supply from pin 17 used); V_P = 8,5 V; f = 40 Hz.

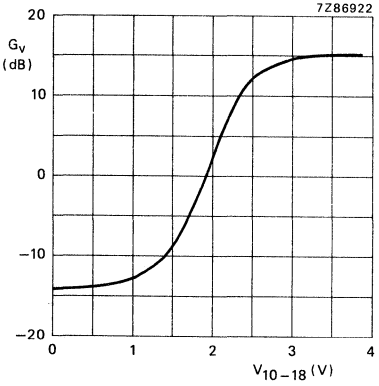


Fig. 8 Treble control curve; voltage gain (G_V) as a function of control voltage (V_{10-18}). Measured in Fig. 1 (internal potentiometer supply from pin 17 used); V_P = 8,5 V; f = 16 kHz.

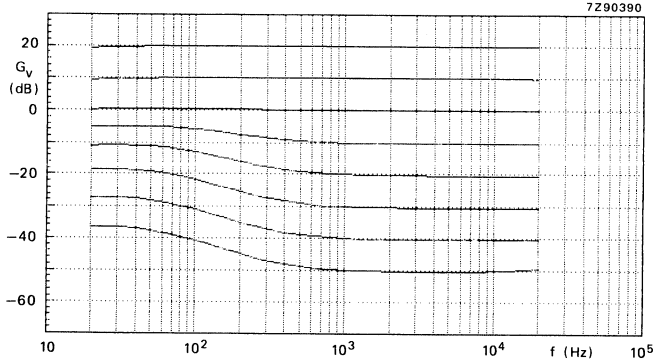


Fig. 9 Contour frequency response curves; voltage gain (G_V) as a function of audio input frequency. Measured in Fig. 1 with single-pole filter; V_P = 8,5 V.

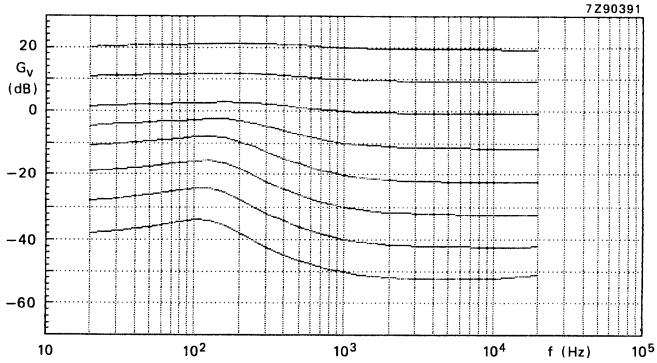


Fig. 10 Contour frequency response curves; voltage gain (G_V) as a function of audio input frequency. Measured in Fig. 1 with double-pole filter; V_P = 8,5 V.

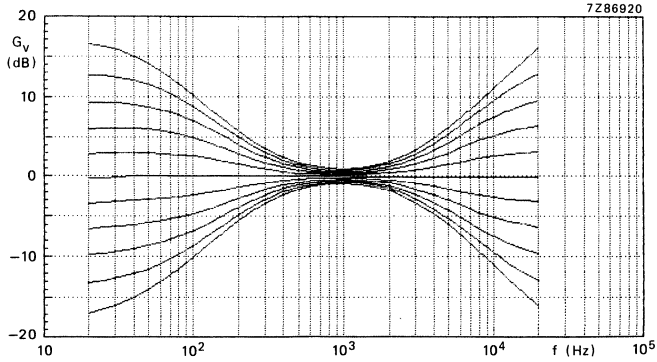


Fig. 11 Tone control frequency response curves; voltage gain (G_V) as a function of audio input frequency. Measured in Fig. 1 with single-pole filter; V_P = 8,5 V.

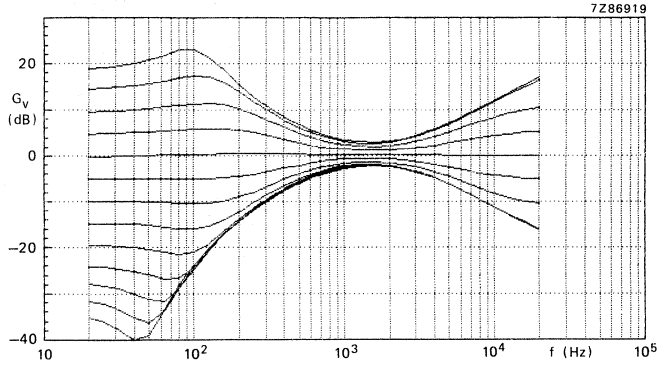


Fig. 12 Tone control frequency response curves; voltage gain (G_V) as a function of audio input frequency. Measured in Fig. 1 with double-pole filter; V_P = 8,5 V.

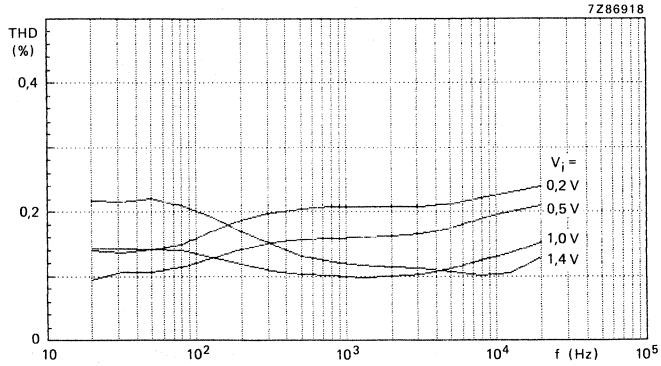


Fig. 13 Total harmonic distortion (THD); as a function of audio input frequency. Measured in Fig. 1; V_P = 8,5 V; volume control voltage gain at

$$G_V = 20 \log \frac{V_o}{V_i} = 0 \text{ dB}.$$

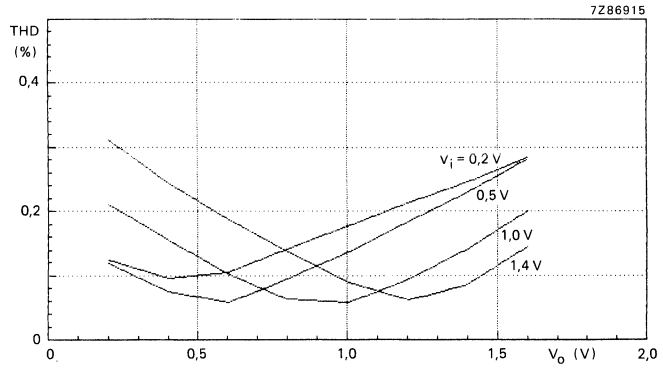
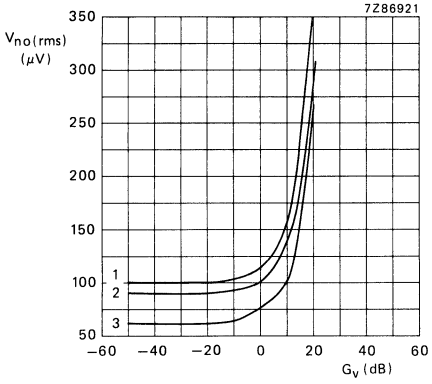


Fig. 14 Total harmonic distortion (THD); as a function of output voltage (V_o). Measured in Fig. 1; V_P = 8,5 V; f_i = 1 kHz.

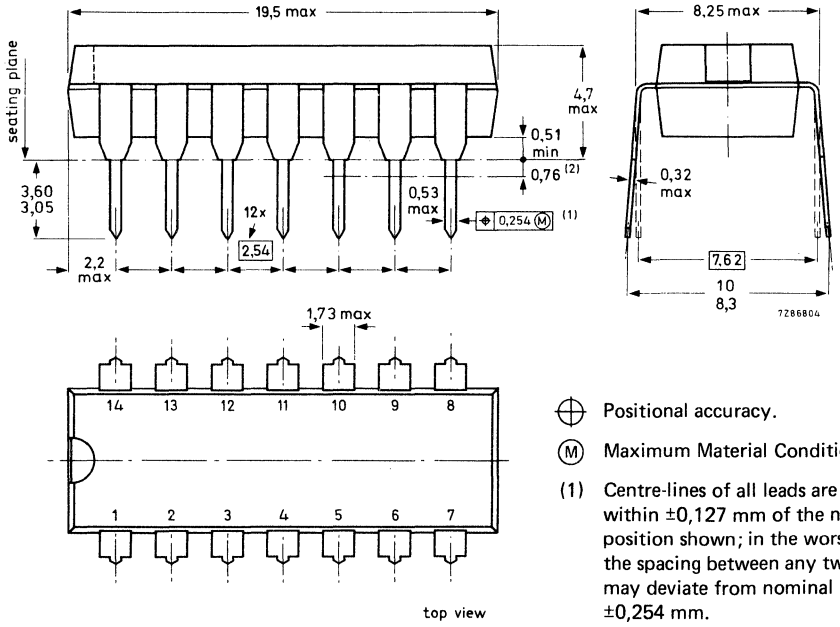


(1) V_P = 15 V.
(2) V_P = 12 V.
(3) V_P = 8,5 V.

Fig. 15 Noise output voltage ($V_{no(rms)}$; unweighted); as a function of voltage gain (G_V). Measured in Fig. 1; f = 20 Hz to 20 kHz.

PACKAGE OUTLINES

14-LEAD DUAL IN-LINE; PLASTIC (SOT-27K,M,T)



⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

Dimensions in mm

SOLDERING

1. By hand

Apply the soldering iron below the seating plane (or not more than 2 mm above it).
If its temperature is below 300 °C it must not be in contact for more than 10 seconds; if between 300 °C and 400 °C, for not more than 5 seconds.

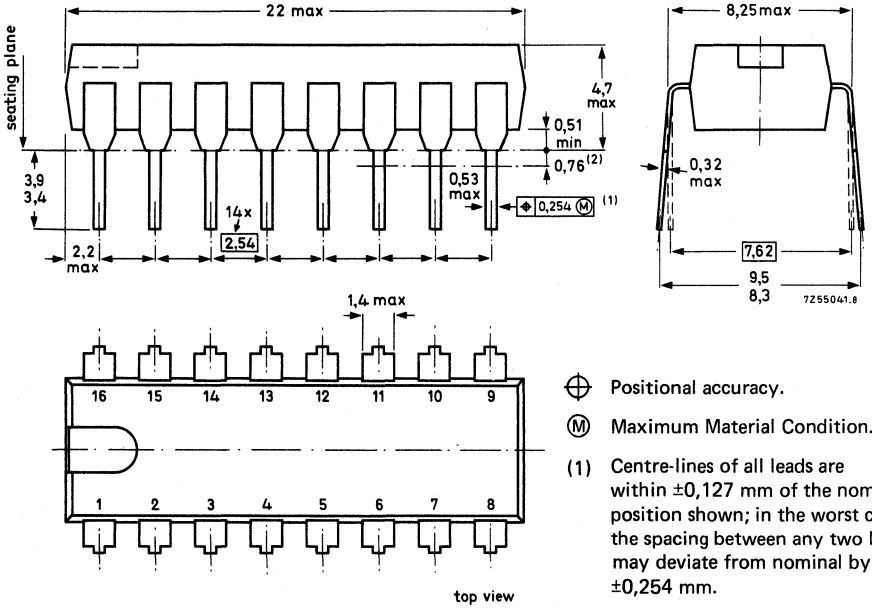
2. By dip or wave

The maximum permissible temperature of the solder is 260 °C; this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.
The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

3. Repairing soldered joints

The same precautions and limits apply as in (1) above.

16-LEAD DUAL IN-LINE; PLASTIC (SOT-38)



⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

Dimensions in mm

SOLDERING

1. By hand

Apply the soldering iron below the seating plane (or not more than 2 mm above it).
If its temperature is below 300 °C it must not be in contact for more than 10 seconds; if between 300 °C and 400 °C, for not more than 5 seconds.

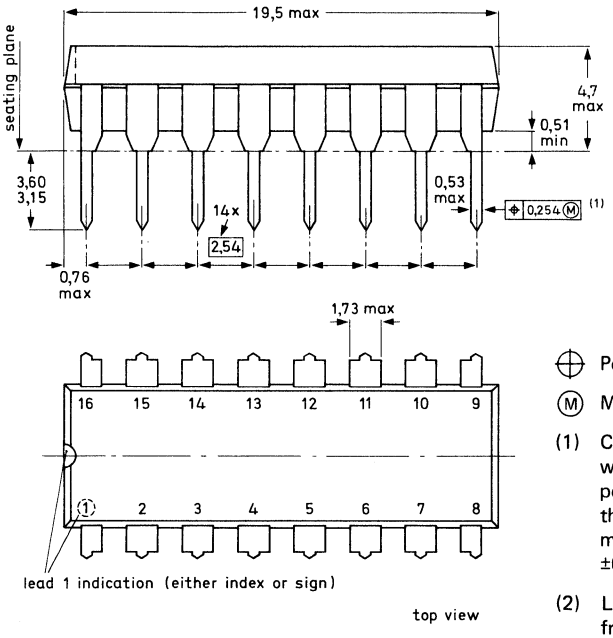
2. By dip or wave

The maximum permissible temperature of the solder is 260 °C; this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.
The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

3. Repairing soldered joints

The same precautions and limits apply as in (1) above.

16-LEAD DUAL IN-LINE; PLASTIC (SOT-38DE)



⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

Dimensions in mm

SOLDERING

1. By hand

Apply the soldering iron below the seating plane (or not more than 2 mm above it).
If its temperature is below 300 °C it must not be in contact for more than 10 seconds; if between 300 °C and 400 °C, for not more than 5 seconds.

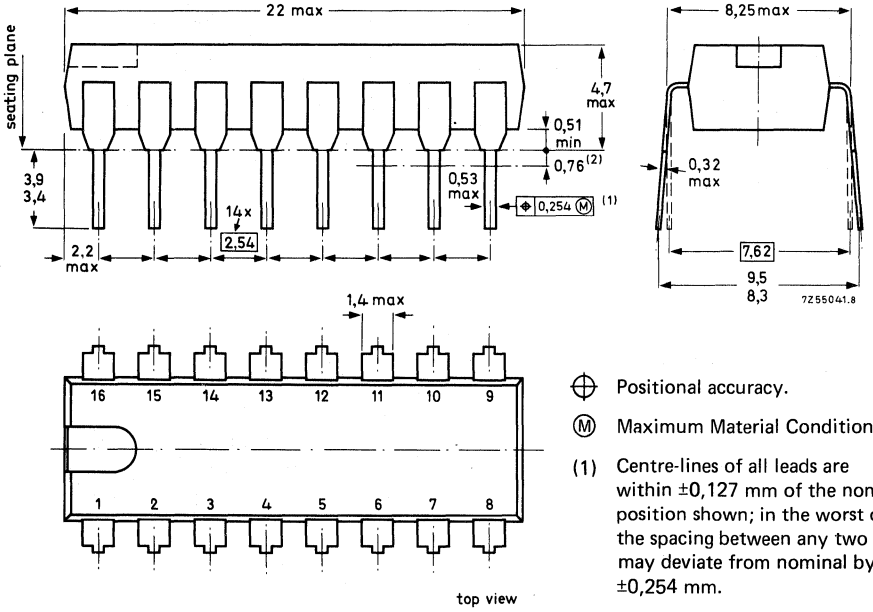
2. By dip or wave

The maximum permissible temperature of the solder is 260 °C; this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.
The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

3. Repairing soldered joints

The same precautions and limits apply as in (1) above.

16-LEAD DUAL IN-LINE; PLASTIC WITH INTERNAL HEAT SPREADER (SOT-38WE-2)



⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

Dimensions in mm

SOLDERING

1. By hand

Apply the soldering iron below the seating plane (or not more than 2 mm above it).
If its temperature is below 300 °C it must not be in contact for more than 10 seconds; if between 300 °C and 400 °C, for not more than 5 seconds.

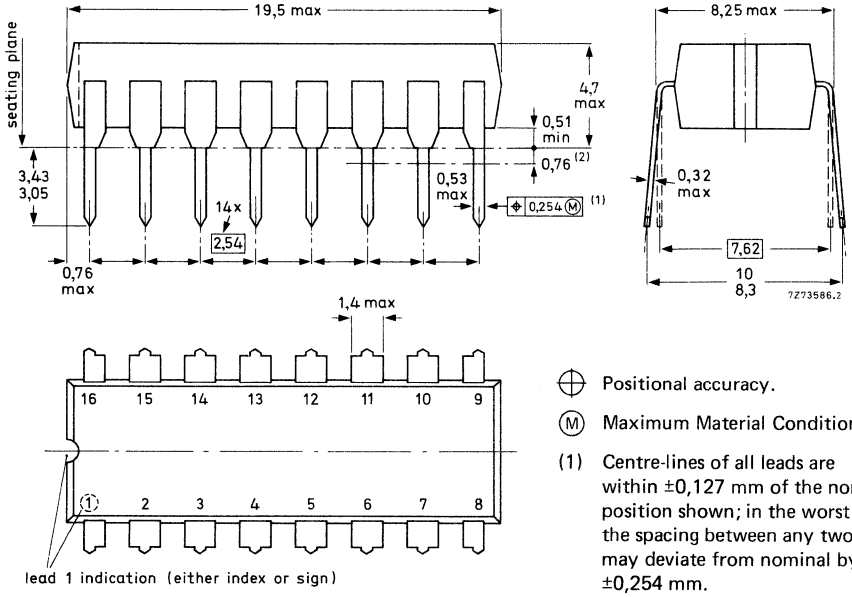
2. By dip or wave

The maximum permissible temperature of the solder is 260 °C; this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.
The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

3. Repairing soldered joints

The same precautions and limits apply as in (1) above.

16-LEAD DUAL IN-LINE; PLASTIC (SOT-38Z)



⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

Dimensions in mm

SOLDERING

1. By hand

Apply the soldering iron below the seating plane (or not more than 2 mm above it).
If its temperature is below 300 °C it must not be in contact for more than 10 seconds; if between 300 °C and 400 °C, for not more than 5 seconds.

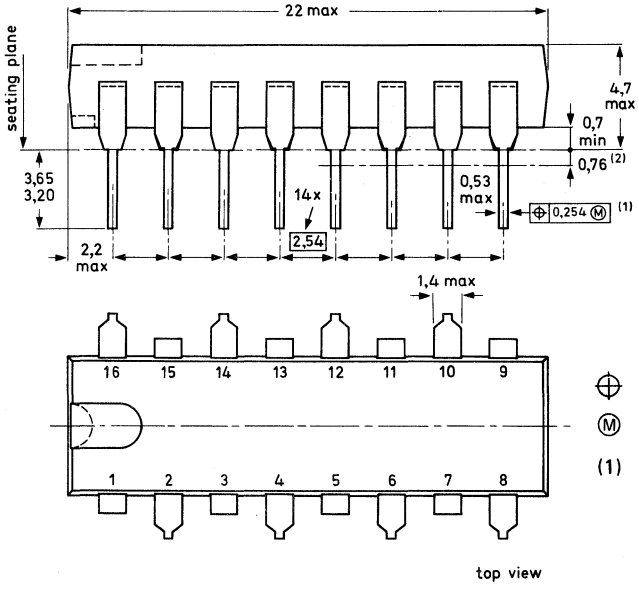
2. By dip or wave

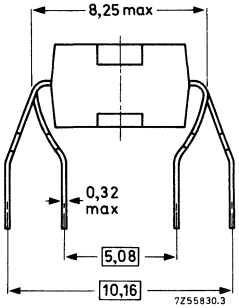
The maximum permissible temperature of the solder is 260 °C; this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.
The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

3. Repairing soldered joints

The same precautions and limits apply as in (1) above.

16-LEAD QUADRUPLE IN-LINE; PLASTIC (SOT-58)





⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

Dimensions in mm

SOLDERING

1. By hand

Apply the soldering iron below the seating plane (or not more than 2 mm above it).
If its temperature is below 300 °C it must not be in contact for more than 10 seconds; if between 300 °C and 400 °C, for not more than 5 seconds.

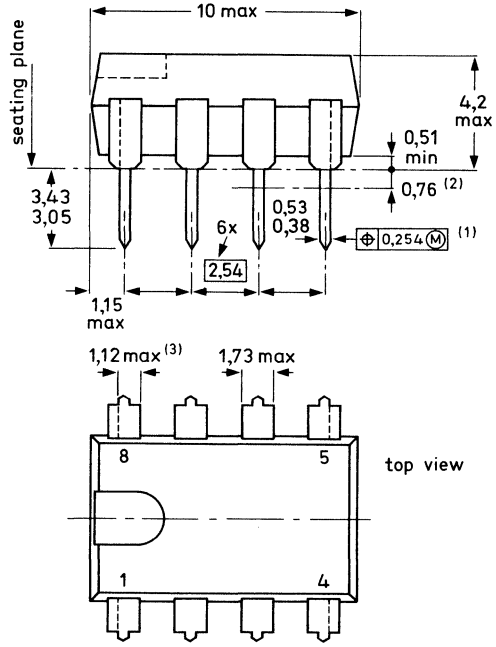
2. By dip or wave

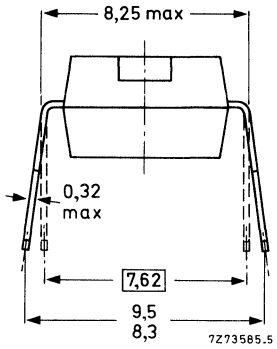
The maximum permissible temperature of the solder is 260 °C; this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.
The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

3. Repairing soldered joints

The same precautions and limits apply as in (1) above.

8-LEAD DUAL IN-LINE; PLASTIC (SOT-97A)





Dimensions in mm

⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

(3) Only for devices with asymmetrical end-leads.

SOLDERING

1. By hand

Apply the soldering iron below the seating plane (or not more than 2 mm above it).
If its temperature is below 300 °C it must not be in contact for more than 10 seconds; if between 300 °C and 400 °C, for not more than 5 seconds.

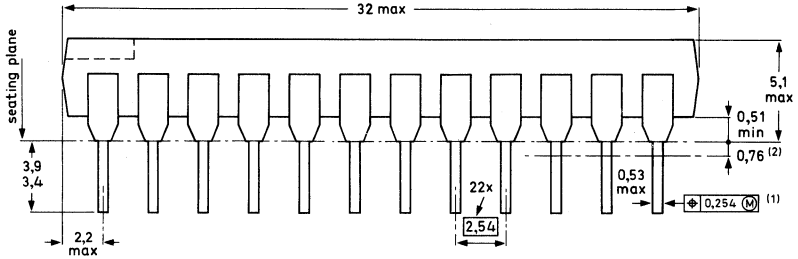
2. By dip or wave

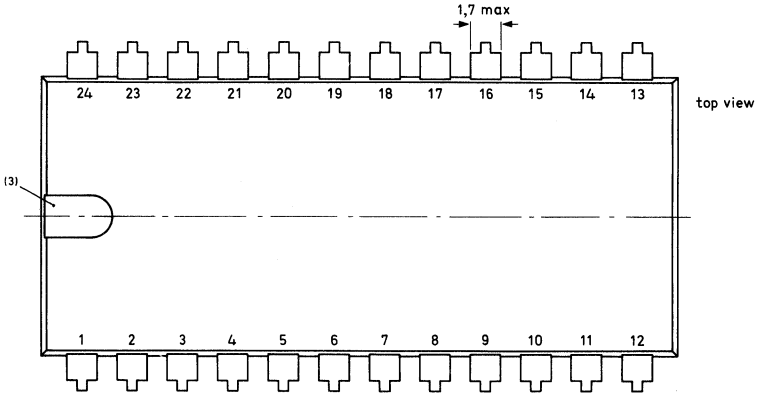
The maximum permissible temperature of the solder is 260 °C; this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.
The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

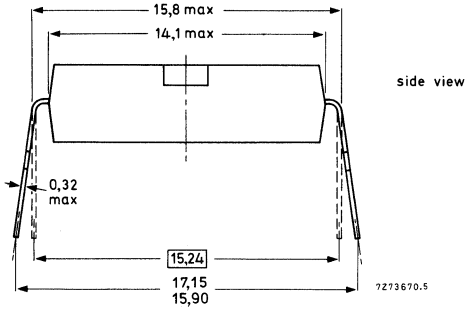
3. Repairing soldered joints

The same precautions and limits apply as in (1) above.

24-LEAD DUAL IN-LINE; PLASTIC (SOT-101A)







⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

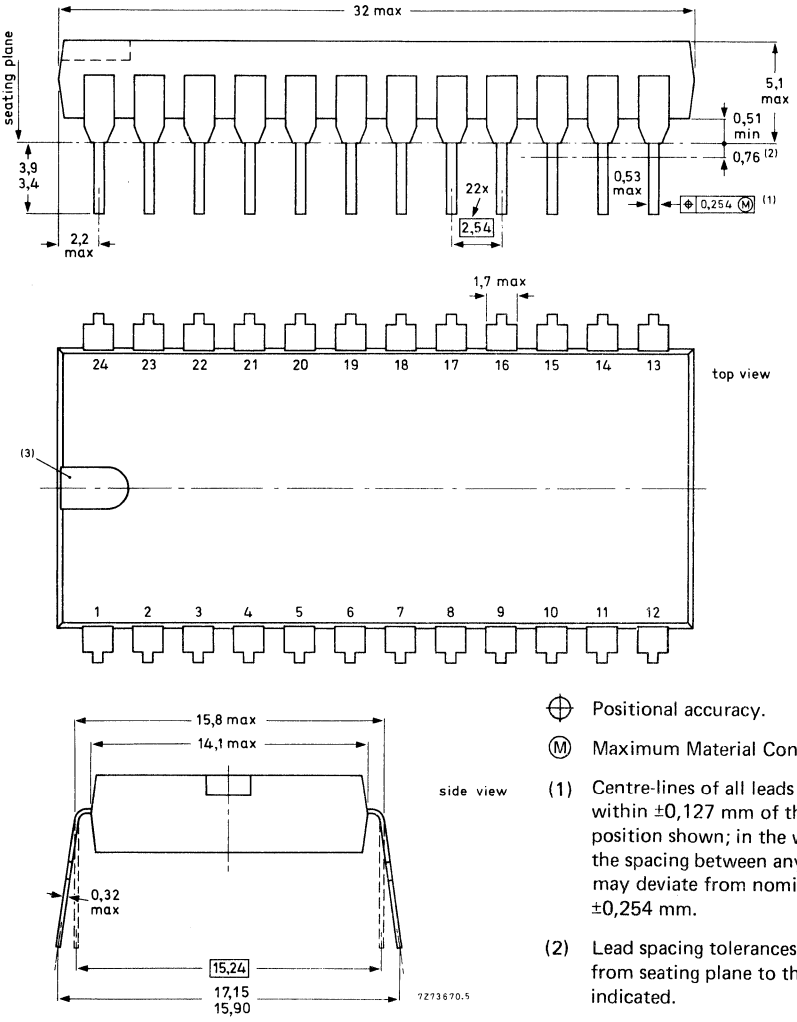
(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

(3) Index may be horizontal as shown, or vertical.

Dimensions in mm

24-LEAD DUAL IN-LINE; PLASTIC (WITH INTERNAL HEAT SPREADER) (SOT-101A, B)



⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

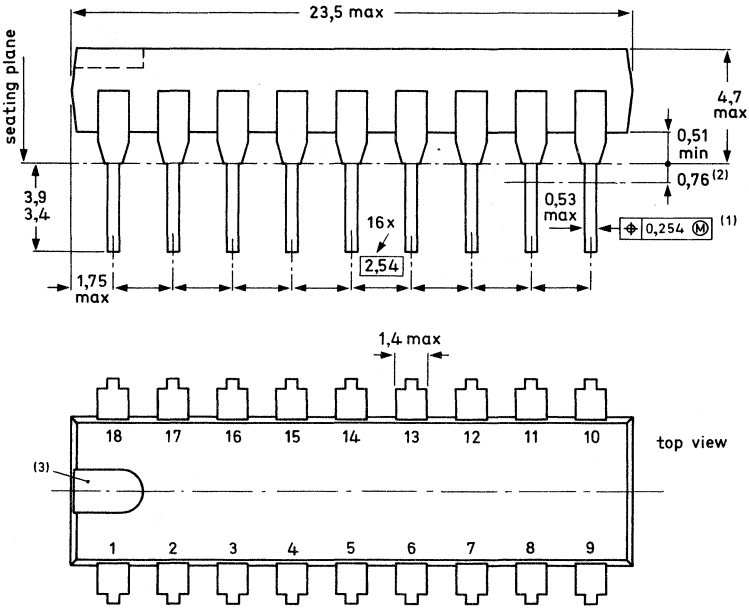
(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

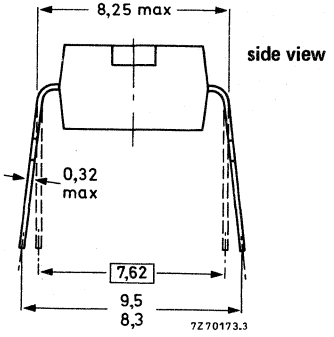
(2) Lead spacing tolerances apply from seating plane to the line indicated.

(3) Index may be horizontal as shown, or vertical.

Dimensions in mm

18-LEAD DUAL IN-LINE; PLASTIC (SOT-102A)





⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

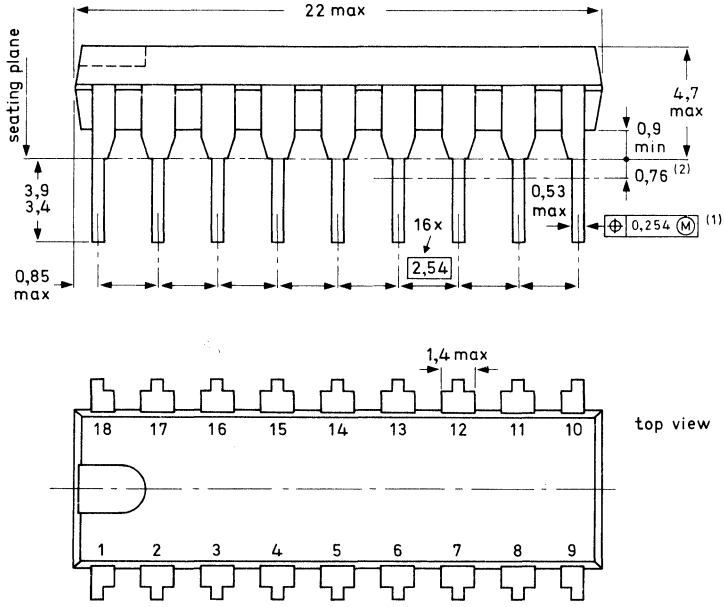
(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

(3) Index may be horizontal as shown, or vertical.

Dimensions in mm

18-LEAD DUAL IN-LINE; PLASTIC (SOT-102CS,HE,KE)



⊕ Positional accuracy.

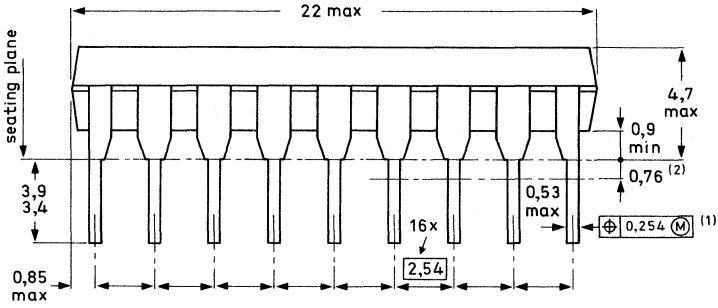
Ⓜ Maximum Material Condition.

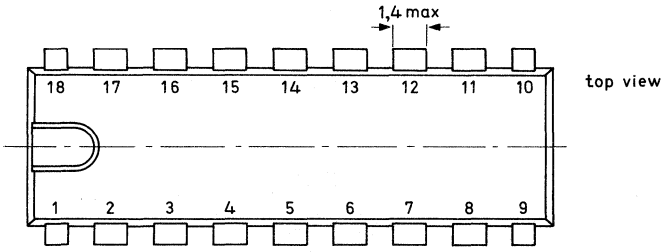
(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

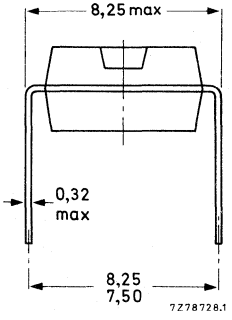
(2) Lead spacing tolerances apply from seating plane to the line indicated.

Dimensions in mm

18-LEAD DUAL IN-LINE; PLASTIC (SOT-102DS)







⊕ Positional accuracy.

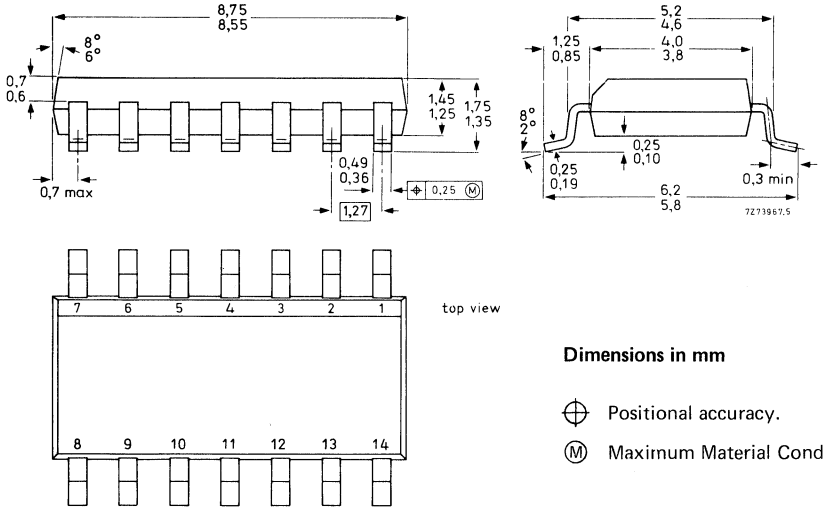
Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

Dimensions in mm

14-LEAD MINI-PACK; PLASTIC (SO-14; SOT-108A)



Dimensions in mm

⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

SOLDERING

The reflow solder technique

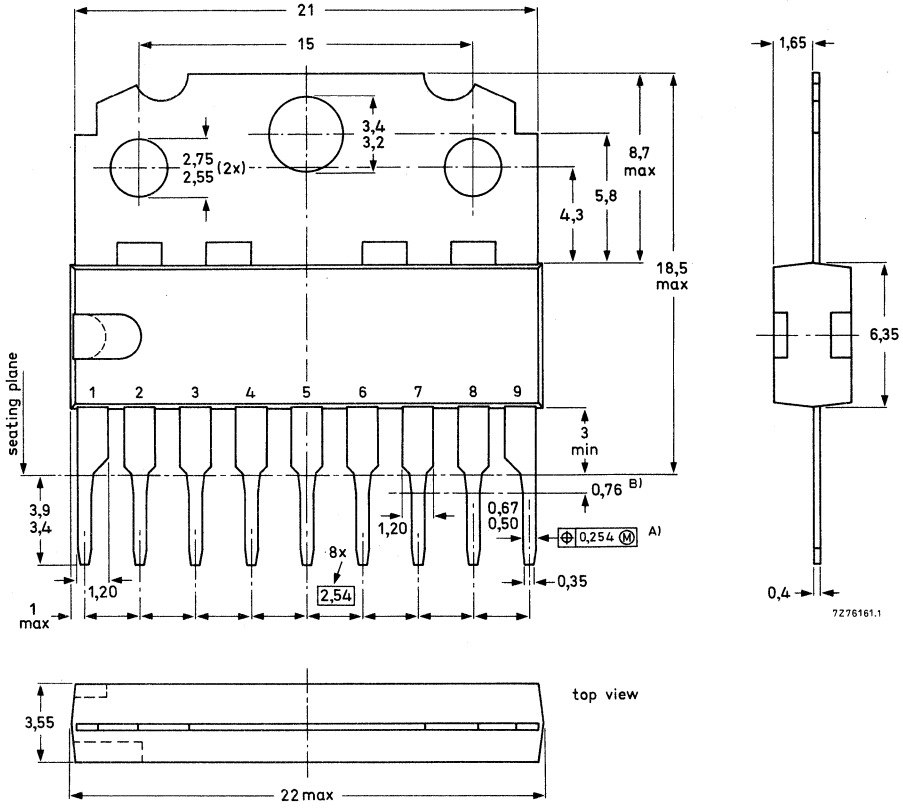
The preferred technique for mounting miniature components on hybrid thick or thin-film circuits is reflow soldering. Solder is applied to the required areas on the substrate by dipping in a solder bath or, more usually, by screen printing a solder paste. Components are put in place and the solder is reflowed by heating.

Solder pastes consist of very finely powdered solder and flux suspended in an organic liquid binder. They are available in various forms depending on the specification of the solder and the type of binder used. For hybrid circuit use, a tin-lead solder with 2 to 4% silver is recommended. The working temperature of this paste is about 220 to 230 °C when a mild flux is used.

For printing the paste onto the substrate a stainless steel screen with a mesh of 80 to 105 μm is used for which the emulsion thickness should be about 50 μm. To ensure that sufficient solder paste is applied to the substrate, the screen aperture should be slightly larger than the corresponding contact area.

The contact pins are positioned on the substrate, the slight adhesive force of the solder paste being sufficient to keep them in place. The substrate is heated to the solder working temperature preferably by means of a controlled hot plate. The soldering process should be kept as short as possible: 10 to 15 seconds is sufficient to ensure good solder joints and evaporation of the binder fluid.
After soldering, the substrate must be cleaned of any remaining flux.

9-LEAD SINGLE IN-LINE; PLASTIC (SOT-110B)



Dimensions in mm

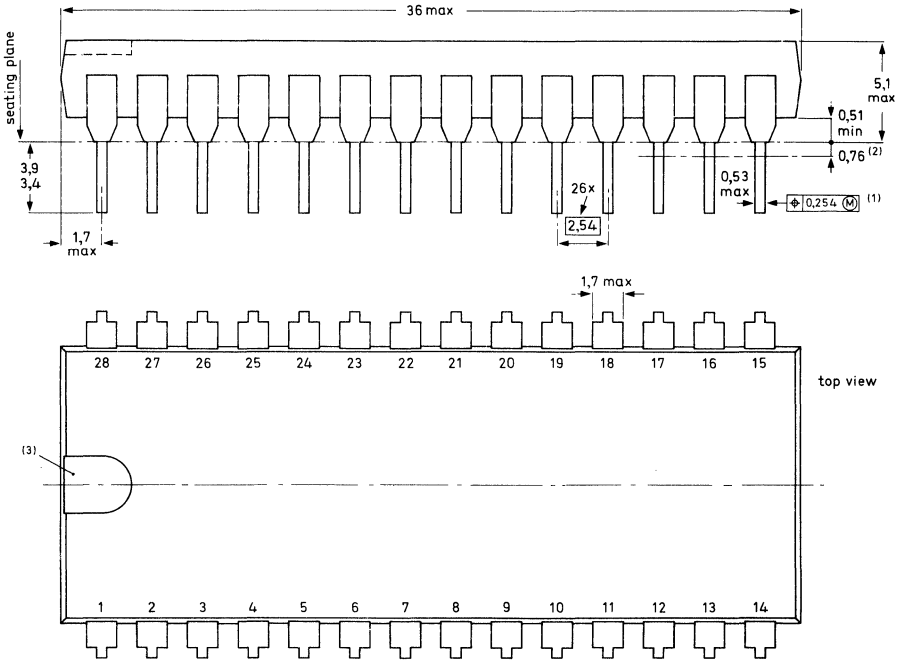
⊕ Positional accuracy.

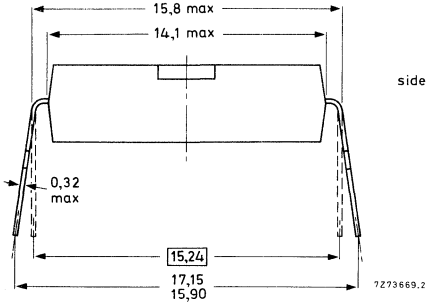
Ⓜ Maximum Material Condition.

A Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

B Lead spacing tolerances apply from seating plane to the line indicated.

28-LEAD DUAL IN-LINE; PLASTIC (SOT-117)





⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

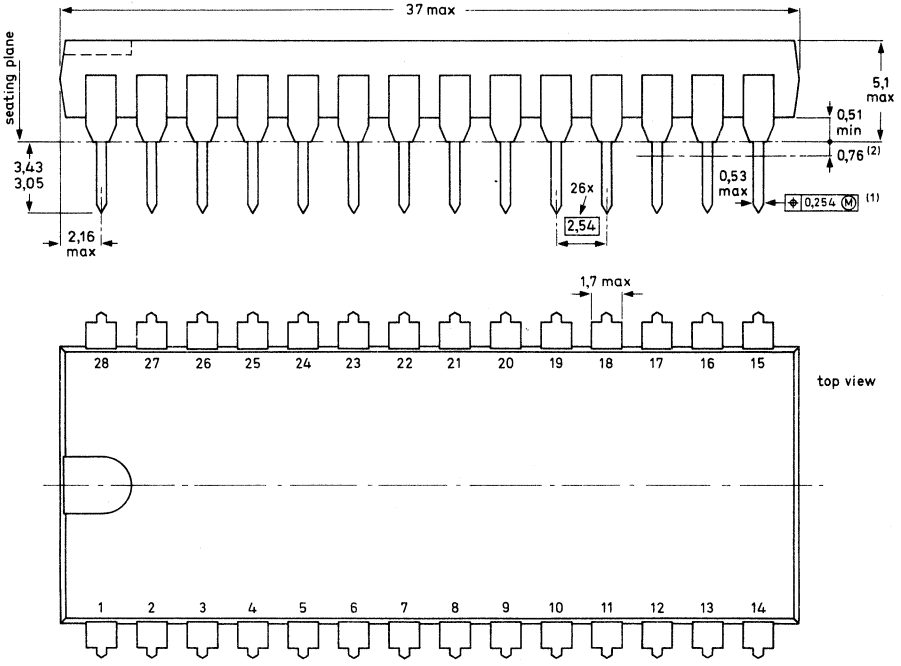
(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

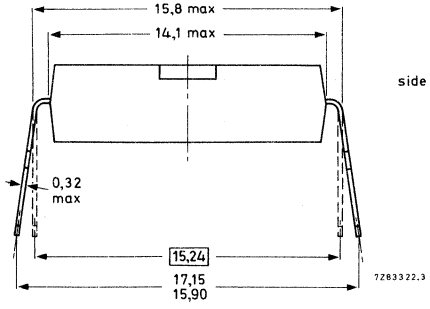
(2) Lead spacing tolerances apply from seating plane to the line indicated.

(3) Index may be horizontal as shown, or vertical.

Dimensions in mm

28-LEAD DUAL IN-LINE; PLASTIC (SOT-117A,D)





⊕ Positional accuracy.

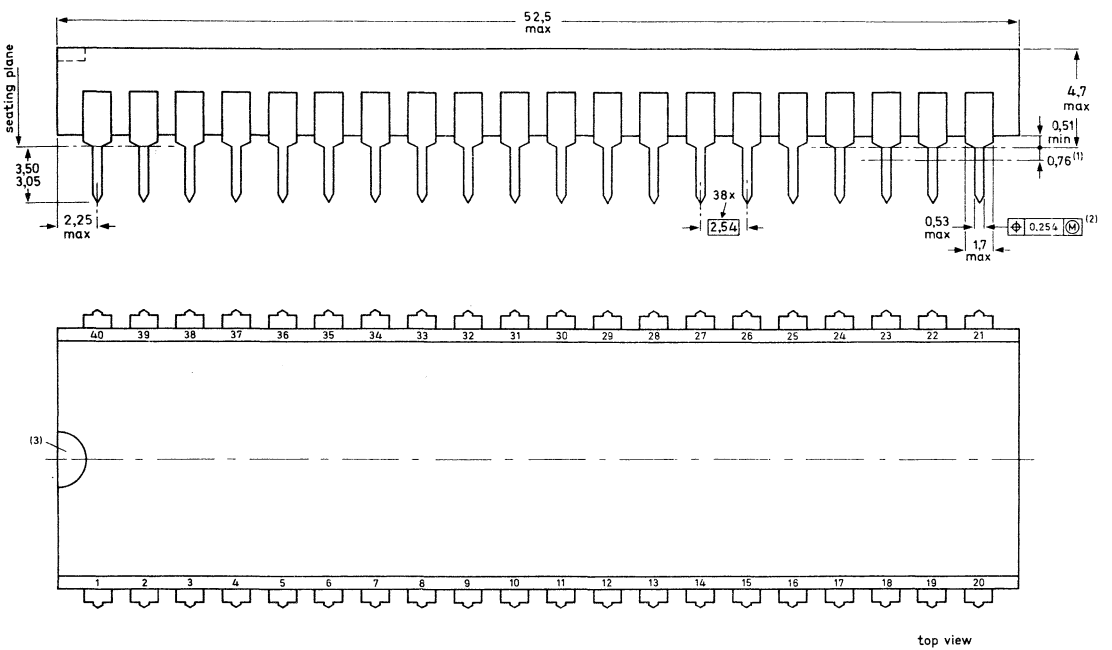
Ⓜ Maximum Material Condition.

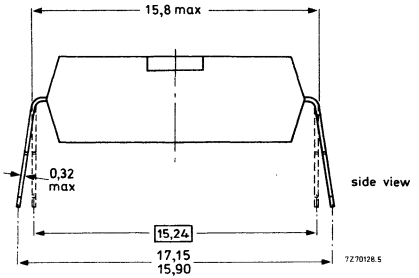
(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

Dimensions in mm

40-LEAD DUAL IN-LINE; PLASTIC (SOT-129)





⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

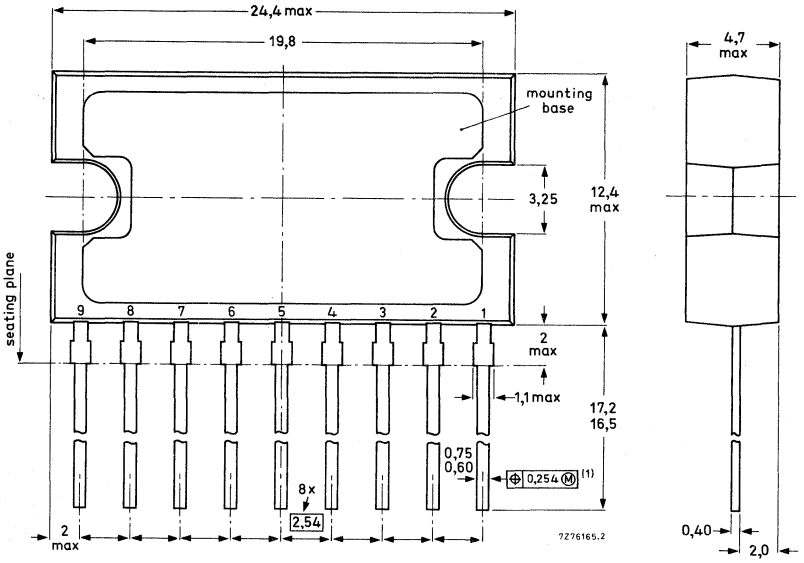
(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

(3) Index may be horizontal as shown, or vertical.

Dimensions in mm

9-LEAD SINGLE IN-LINE; PLASTIC POWER (SOT-131A, B)



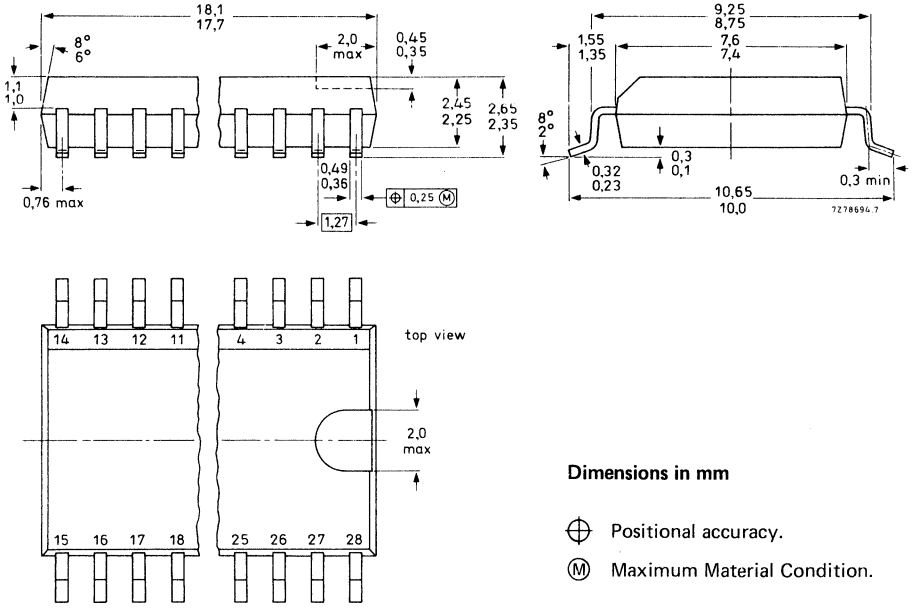
Dimensions in mm

⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

28-LEAD MINI-PACK; PLASTIC (SO-28; SOT-136A)



Dimensions in mm

⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

SOLDERING

1. Soldering iron or pulse heated solder tool

Apply the heating tool to the flat part of the pin only.
Limit the contact time to maximum 10 seconds up to 300 °C, or 5 seconds up to maximum 400 °C.
When using the proper tools, all pins can be soldered in one operation within 2 to 5 seconds and 270 to 320 °C.

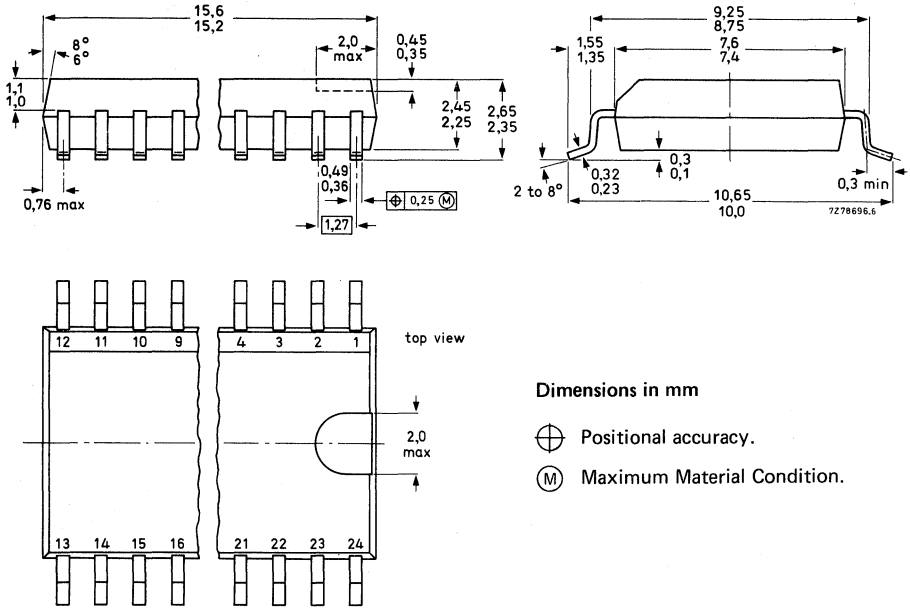
2. By dip or wave

The maximum permissible temperature of the solder is 260 °C. The permissible total time of immersing the whole package in the bath is 10 seconds, if it is allowed to cool down to less than 150 °C within 6 seconds.

3. Repairing soldered joints

The same precautions and limits apply as in (1) above.
If the vertical part of the pin needs heating, reduce the soldering iron temperature to 260 °C.

24-LEAD MINI-PACK; PLASTIC (SO-24; SOT-137A)



Dimensions in mm

⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

SOLDERING

The reflow solder technique

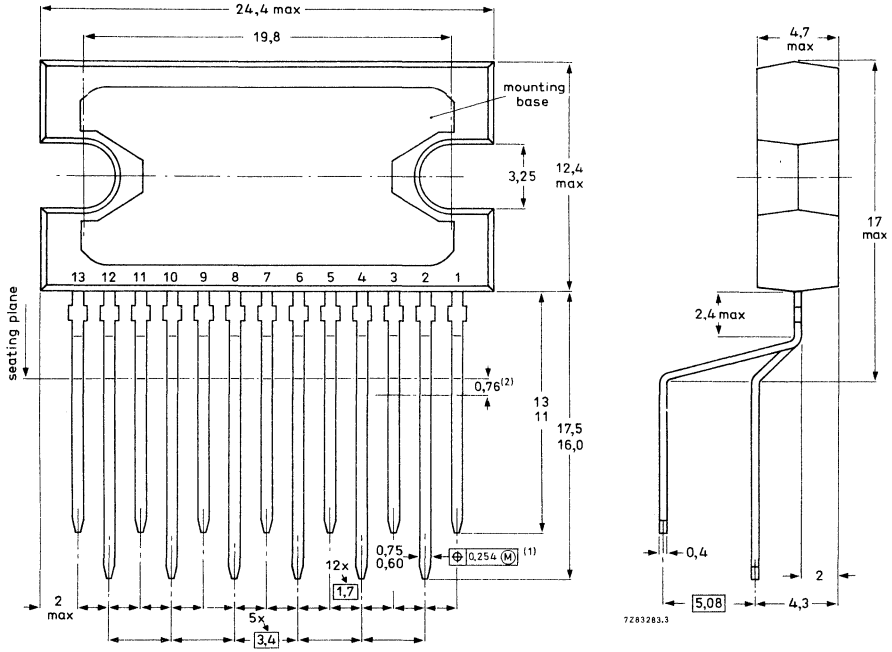
The preferred technique for mounting miniature components on hybrid thick or thin-film circuits is reflow soldering. Solder is applied to the required areas on the substrate by dipping in a solder bath or, more usually, by screen printing a solder paste. Components are put in place and the solder is reflowed by heating.

Solder pastes consist of very finely powdered solder and flux suspended in an organic liquid binder. They are available in various forms depending on the specification of the solder and the type of binder used. For hybrid circuit use, a tin-lead solder with 2 to 4% silver is recommended. The working temperature of this paste is about 220 to 230 °C when a mild flux is used.

For printing the paste onto the substrate a stainless steel screen with a mesh of 80 to 105 μm is used for which the emulsion thickness should be about 50 μm. To ensure that sufficient solder paste is applied to the substrate, the screen aperture should be slightly larger than the corresponding contact area.

The contact pins are positioned on the substrate, the slight adhesive force of the solder paste being sufficient to keep them in place. The substrate is heated to the solder working temperature preferably by means of a controlled hot plate. The soldering process should be kept as short as possible: 10 to 15 seconds is sufficient to ensure good solder joints and evaporation of the binder fluid.
After soldering, the substrate must be cleaned of any remaining flux.

13-LEAD SIL-BENT-TO-DIL; PLASTIC POWER (SOT-141B)



Dimensions in mm

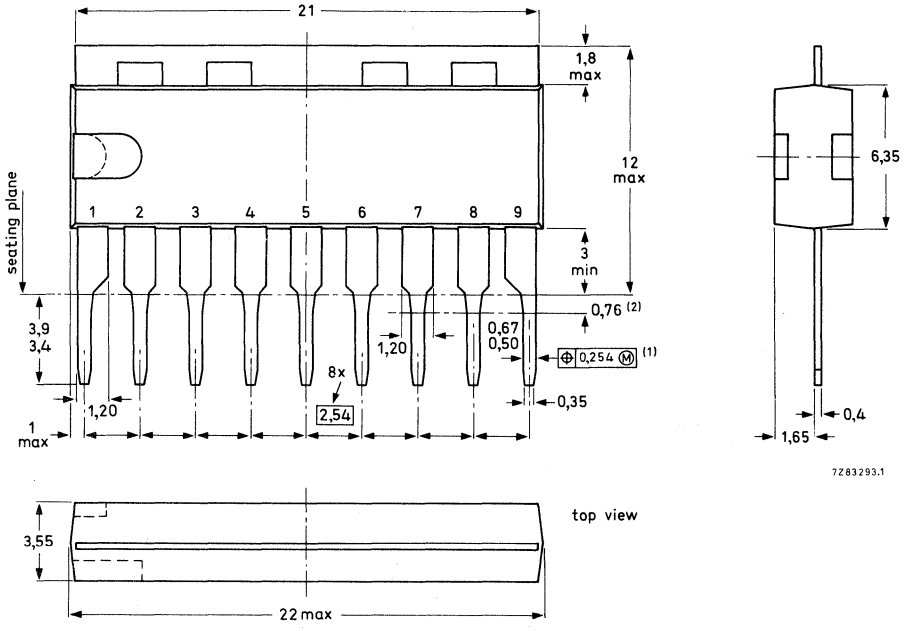
⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

9-LEAD SINGLE IN-LINE; PLASTIC (SOT-142)



Dimensions in mm

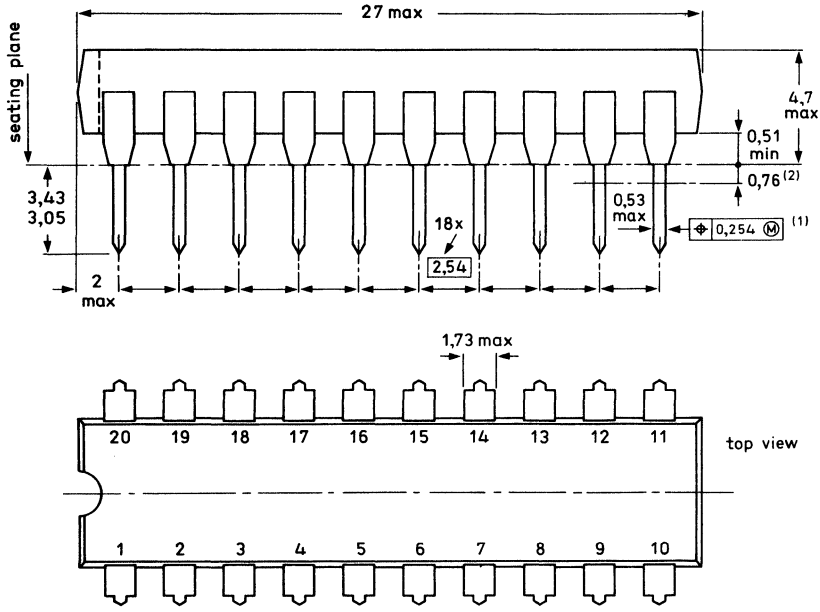
⊕ Positional accuracy.

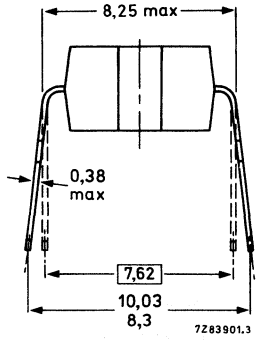
Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

20-LEAD DUAL IN-LINE; PLASTIC (SOT-146)





side view

⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

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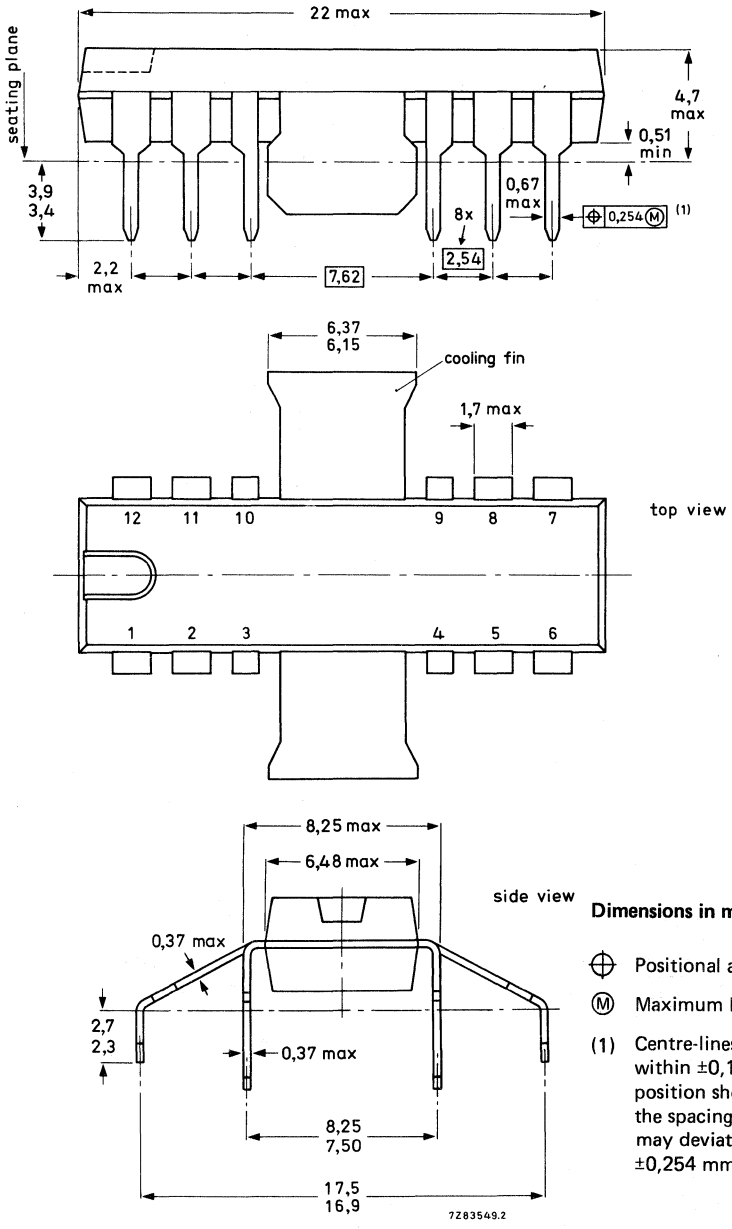
Dimensions in mm

12-LEAD DUAL IN-LINE; PLASTIC WITH METAL COOLING FIN (SOT-150)



Dimensions in mm

⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

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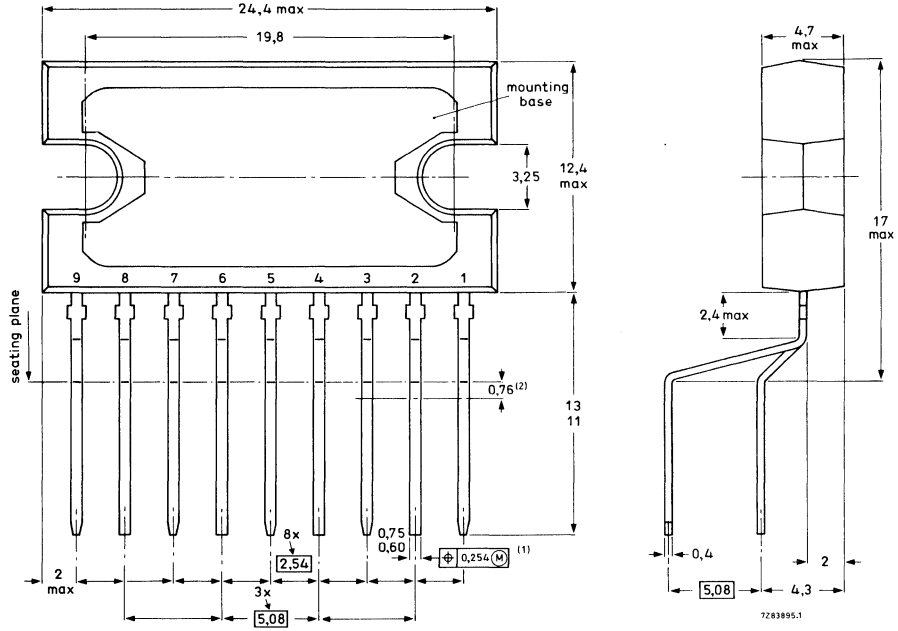
9-LEAD SIL-BENT-TO-DIL; PLASTIC POWER (SOT-157A,B)



Dimensions in mm

⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

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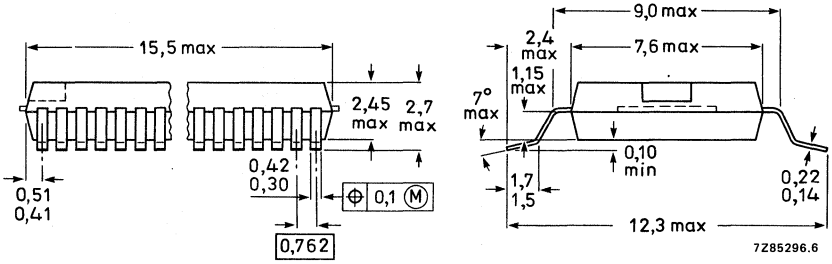
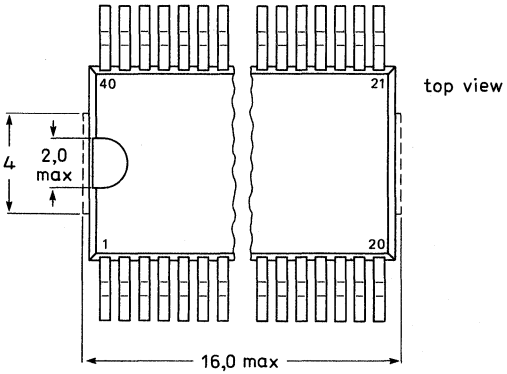
40-LEAD MINI-PACK; PLASTIC (VSO-40; SOT-158A)





Dimensions in mm

⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

SOLDERING

The reflow solder technique

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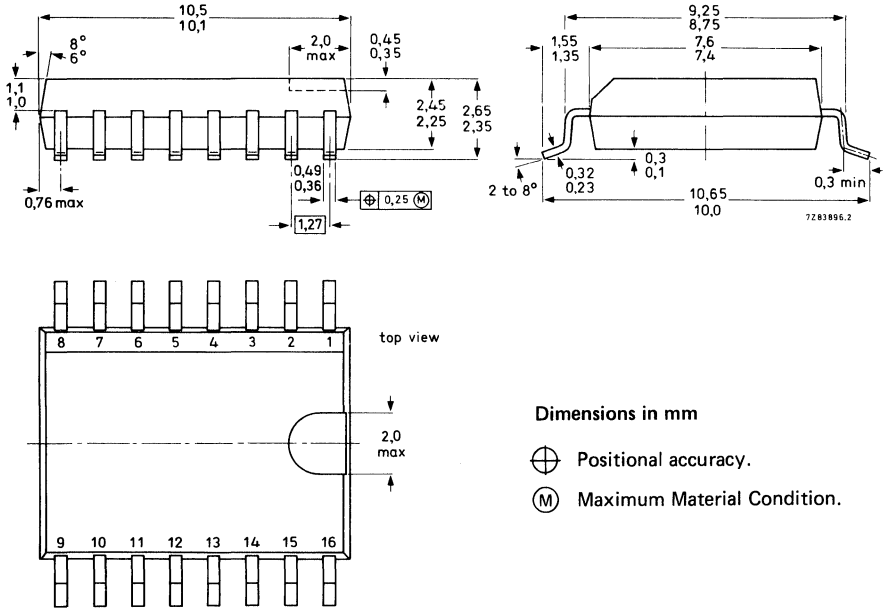
Solder pastes consist of very finely powdered solder and flux suspended in an organic liquid binder. They are available in various forms depending on the specification of the solder and the type of binder used. For hybrid circuit use, a tin-lead solder with 2 to 4% silver is recommended. The working temperature of this paste is about 220 to 230 °C when a mild flux is used.

For printing the paste onto the substrate a stainless steel screen with a mesh of 80 to 105 μm is used for which the emulsion thickness should be about 50 μm. To ensure that sufficient solder paste is applied to the substrate, the screen aperture should be slightly larger than the corresponding contact area.

The contact pins are positioned on the substrate, the slight adhesive force of the solder paste being sufficient to keep them in place. The substrate is heated to the solder working temperature preferably by means of a controlled hot plate. The soldering process should be kept as short as possible: 10 to 15 seconds is sufficient to ensure good solder joints and evaporation of the binder fluid.
After soldering, the substrate must be cleaned of any remaining flux.

16-LEAD MINI-PACK; PLASTIC (SO-16L; SOT-162A)



Dimensions in mm

⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

SOLDERING

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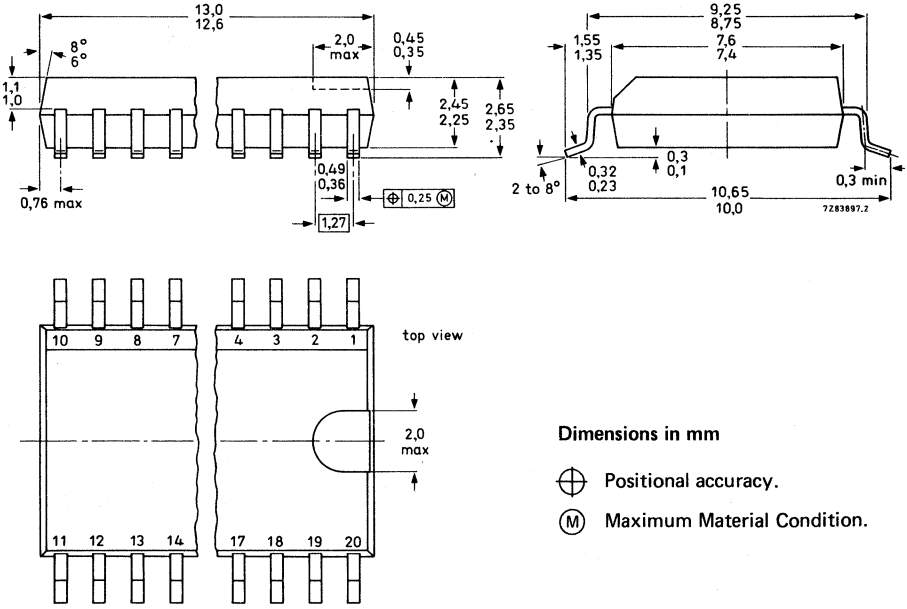
20-LEAD MINI-PACK; PLASTIC (SO-20; SOT-163A)



Dimensions in mm

⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

SOLDERING

The reflow solder technique

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