OPTi®

82C601/82C602

Buffer Devices

Data Book

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Buffer Devices

1.0 Features

• Reduces motherboard component count

• Simplifies board design

• Increased reliability

• Integral power management control (82C602)

• Integral real-time clock (82C602)

• Programmable chip select (82C602)

• 100-Pin PFP (Plastic Flat Pack)

• 1.0-micron CMOS technology

2.0 Overview

OPTi's 82C601 and 82C602 buffer devices are packaged in 100-pin PFPs (Plastic Flat Pack) and are designed to replace approximately nine TTL components normally found on PC/AT motherboards, offering significant cost savings and a substantially simplified PCB layout.

Pin-compatible with each other, the 82C602 is an upgrade from the 82C601 that adds a real-time clock (RTC) and power management functionality. (Later versions of the buffer chip will also include a keyboard controller.)

The 82C601 and 82C602 are closely coupled with OPTi's 82C801/802/802G, 82C499, and 82C495SLC/XLC chipsets to allow higher integration and lower cost.

Figure 2-1   82C601/82C602 Internal Block Diagram
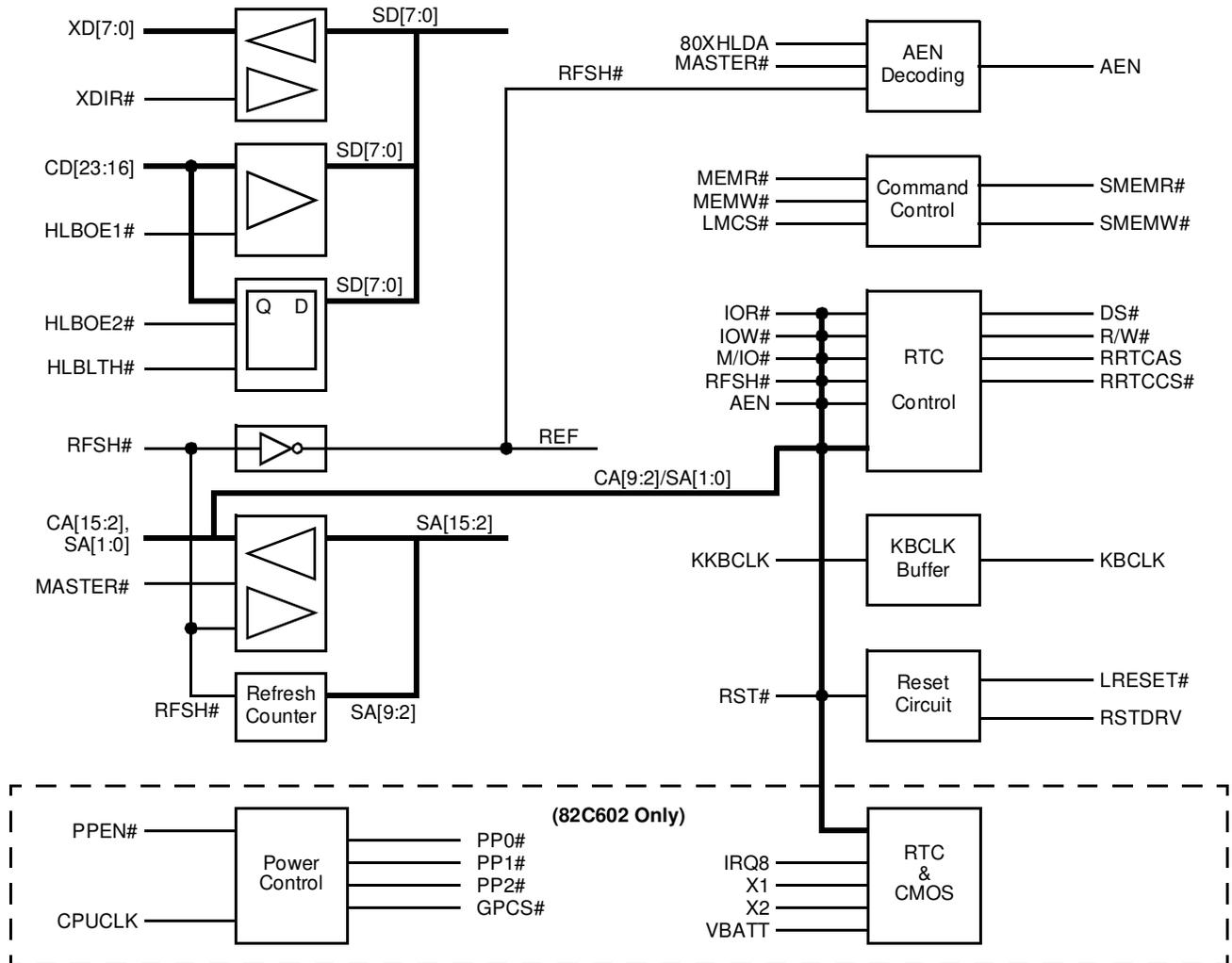
82C601/82C602

Figure 2-2   82C802G/82C601/602-Based System   Block Diagram
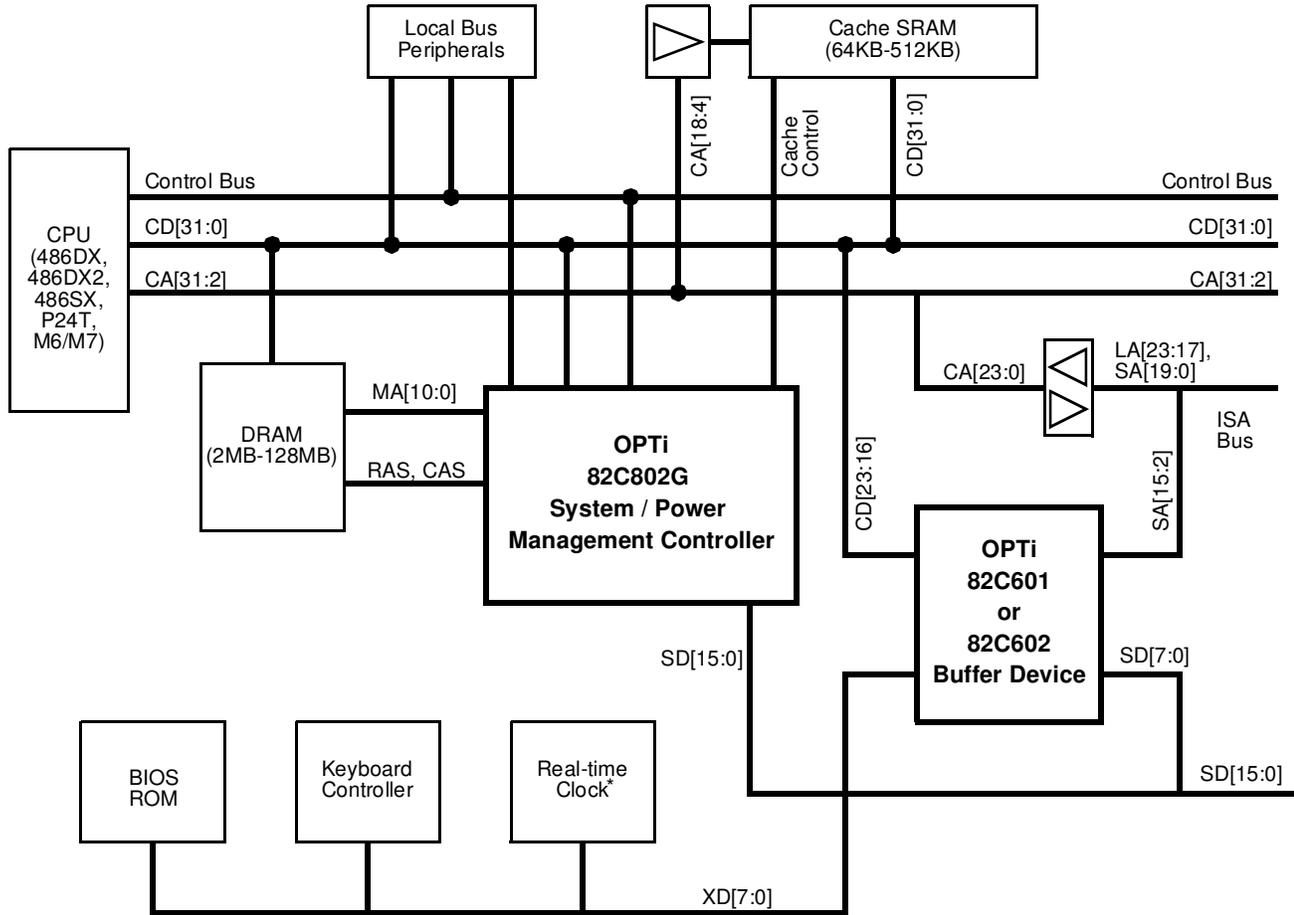
*Included as a part of 82C602.

3.0 Signal Definitions

Figure 3-1   Pin Diagram

82C601 & 82C602
Buffer Devices

Top pins (80–51): SD1, SD0, GND, AEN, RSTDRV, LRESET#, SMEMW#, SMEMR#, XDIR#, VCC, LMCS#/KBCS#, MEMW#, MEMR#, CD23, GND, CD22, CD21, CD20, CD19, CD18, CD17, CD16, MIO#, VCC, IRQ8, VBATT, X2, X1, GND, REF

Left pins (81–100): SD2, SD3, SD4, SD5, SD6, SD7, RFSH#, XD0, XD1, GND, VCC, XD2, XD3, XD4, XD5, XD6, XD7, MASTER#, SA2, SA3

Right pins (50–31): 80XHLDA, HLBOE1#/HDLEN#, HLBOE2#, HLBLTH#/HDDIR#, CA0, CA1, CA2, CA3, CA4, VCC, GND, CA5, CA6, CA7, CA8, CA9, CA10, CA11, CA12, CA13

Bottom pins (1–30): SA4, SA5, GND, SA6, SA7, SA8, SA9, SA10, SA11, SA12, SA13, SA14, SA15, VCC, GND, IOR#, IOW#, ATIOR#/DS#/PP1#, ATIOW#/RW#/GPCS#, CPUCLK, KBCLK, PPEN#, RST#, KKBCLK, RRTCCS#/PP2#, RRTCAS, PP0#, GND, CA15, CA14

Table 3-1   Numerical Pin Cross-Reference List

No.	Name	No.	Name	No.	Name	No.	Name
1	SA4	26	RRTCAS	51	REF	76	RSTDRV
2	SA5	27	PP0#	52	GND	77	AEN
3	GND	28	GND	53	X1	78	GND
4	SA6	29	CA15	54	X2	79	SD0
5	SA7	30	CA14	55	VBATT	80	SD1
6	SA8	31	CA13	56	IRQ8	81	SD2
7	SA9	32	CA12	57	VCC	82	SD3
8	SA10	33	CA11	58	MIO#	83	SD4
9	SA11	34	CA10	59	CD16	84	SD5
10	SA12	35	CA9	60	CD17	85	SD6
11	SA13	36	CA8	61	CD18	86	SD7
12	SA14	37	CA7	62	CD19	87	RFSH#
13	SA15	38	CA6	63	CD20	88	XD0
14	VCC	39	CA5	64	CD21	89	XD1
15	GND	40	GND	65	CD22	90	GND
16	IOR#	41	VCC	66	GND	91	VCC
17	IOW#	42	CA4	67	CD23	92	XD2
18	ATIOR#/DS#/PP1#	43	CA3	68	MEMR#	93	XD3
19	ATIOW#/RW#/GPCS#	44	CA2	69	MEMW#	94	XD4
20	CPUCLK	45	CA1	70	LMCS#/KBCS#	95	XD5
21	KBCLK	46	CA0	71	VCC	96	XD6
22	PPEN#	47	HLBLTH#/HDDIR#	72	XDIR#	97	XD7
23	RST#	48	HLBOE2#	73	SMEMR#	98	MASTER#
24	KKBCLK	49	HBLOE1#/HDLEN#	74	SMEMW#	99	SA2
25	RRTCCS#/PP2#	50	80XHLDA	75	LRESET#	100	SA3

Table 3-2   Alphabetical Pin Cross-Reference List

No.	Name	No.	Name	No.	Name	No.	Name
77	AEN	65	CD22	22	PPEN#	82	SD3
18	ATIOR#/DS#/PP1#	67	CD23	27	PP0#	83	SD4
19	ATIOW#/RW#/GPCS#	20	CPUCLK	51	REF	84	SD5
46	CA0	3	GND	87	RFSH#	85	SD6
45	CA1	15	GND	26	RRTCAS	86	SD7
44	CA2	28	GND	25	RRTCCS#/PP2#	73	SMEMR#
43	CA3	40	GND	23	RST#	74	SMEMW#
42	CA4	52	GND	76	RSTDRV	55	VBATT
39	CA5	66	GND	99	SA2	14	VCC
38	CA6	78	GND	100	SA3	41	VCC
37	CA7	90	GND	1	SA4	57	VCC
36	CA8	49	HBLOE1#/HDLEN#	2	SA5	71	VCC
35	CA9	47	HLBLTH#/HDDIR#	4	SA6	91	VCC
34	CA10	48	HLBOE2#	5	SA7	53	X1
33	CA11	16	IOR#	6	SA8	54	X2
32	CA12	17	IOW#	7	SA9	88	XD0
31	CA13	56	IRQ8	8	SA10	89	XD1
30	CA14	21	KBCLK	9	SA11	92	XD2
29	CA15	24	KKBCLK	10	SA12	93	XD3
59	CD16	70	LMCS#/KBCS#	11	SA13	94	XD4
60	CD17	75	LRESET#	12	SA14	95	XD5
61	CD18	98	MASTER#	13	SA15	96	XD6
62	CD19	68	MEMR#	79	SD0	97	XD7
63	CD20	69	MEMW#	80	SD1	72	XDIR#
64	CD21	58	MIO#	81	SD2	50	80XHLDA

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3.1 Signal Descriptions

3.1.1 Reset Interface

Name	No.	Type	Signal Description
RST#	23	I	Reset: PWRGD input from the power supply.
RSTDRV	76	O	Reset Drive: Active high reset to the AT bus and 82C206 IPC.
LRESET#	75	O	Local Reset: Active low reset to the VESA local bus.

3.1.2 Address Bus Direction Control Interface Signals

Name	No.	Type	Signal Description
MASTER#	98	I	Master: Master cycle indication. This signal is used to control the CA/SA buffer direction.
80XHLDA	50	I	Hold Acknowledge: HLDA from output of the 82C80x, 82C499, or 82C495SLC/XLC.
RFSH#	87	I	Refresh: Refresh cycle indication. This signal is used to: 1) Enable refresh address from internal address counter 2) Tristate CA/SA buffer
REF	51	O	Inverted Refresh#: Refresh cycle indicator.
AEN	77	O	Address Enable: When high, the DMA controller has control of the address lines, data lines, MEMR#, MEMW#, IOR#, and IOW#. This signal is connected to AEN of the AT bus.

3.1.3 Address Bus Interface Signals

Name	No.	Type	Signal Description
SA[15:2]	13:4, 2:1, 100:99	I/O	System Address AT Bus Lines 15 through 2.
CA[15:2]	29:39, 42:44	I/O	CPU Address Lines 15 through 2.
CA[1:0]	45:46	I	CPU Address Lines 1 and 0: Connected to AT bus address lines SA[1:0].

3.1.4 Data Bus And Control Interface Signals

Name	No.	Type	Signal Description
SD[7:0]	86:79	I/O	System Data AT Bus Lines 7 through 0.

3.1.4 Data Bus And Control Interface Signals (cont.)

Name	No.	Type	Signal Description
XD[7:0]	97:92, 89:88	I/O	XD Bus Data Lines 7 through 0: The XD7, XD6, and XD4 lines are internally pulled up and are sampled at reset time for strapping options. To strap these lines low during reset, the XD line should have a 2.2Kohm pull-down resistor. To strap these lines high during reset, a pull-up resistor is not necessary since an internal pull-up resistor exists in the 82C601/82C602. Do not pull down XD5 and XD[3:0], as this will cause the device to malfunction. **82C601** **XD7 XD6 Strap Option** 1 1 82C801/82C802 1 0 82C495 0 1 Reserved 0 0 Reserved **82C602** **XD7 XD6 Strap Option** 1 1 82C801/82C802 1 0 495XLC 0 1 82C802G 0 0 Reserved To enable the RTC when using the 82C602 (not available in 82C601), setting XD4 to 0 enables the RTC and affects pin 18, 24 and 25. For more information regarding these affects, refer to Table 4-1. To disable the RTC, XD4 should be set to 1.
XDIR#	72	I	XD Bus Direction: A direction control signal for the SD bus to/from the XD bus.
CD[23:16]	67, 65:59	I/O	CPU Data Bus Lines 23 through 16.
HLBOE1#/ HDLEN#	49	I	Output enable for CD[23:16] to SD[7:0]. This signal is the HD bus low byte enable control from the chipset to the 82C60x. This signal is called HLBOE1# when used with the 82C499 and 82C80x chipsets. However, it is called HDLEN# when used with the 82C495SLC/XLC.
HLBOE2#	48	I	Output enable for SD[7:0] to CD[23:16] latch from the chipset to the 82C60x.
HLBLTH#/ HDDIR	47	I	Latch control for SD[7:0] to CD[23:16] for 82C80x and 82C499. On the 82C495SLC/XLC, this signal is HD bus direction control for SD[15:0] to CD[31:16].

3.1.5 Command Interface Signals

Name	No.	Type	Signal Description
IOR#	16	I/O	AT I/O Read Command: This signal is an input when used with the 82C499 and 82C80x chipsets. It is bidirectional when used with the 82C495SLC/XLC. Normally an input, IOR# is an output only during ISA master cycles. This signal is tied to IOR# of the chipset.
IOW#	17	I/O	AT I/O Write Command: This signal is an input when used with the 82C499 and 82C80x chipsets. It is bidirectional when used with the 82C495SLC/XLC. Normally an input, IOW# is an output only during ISA master cycles. This signal is tied to IOW# of the chipset.

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3.1.5   Command Interface Signals (cont.)

Name	No.	Type	Signal Description
MEMR#	68	I/O	Memory Read Command: This signal is an input when used with the 82C499 and 82C80x chipsets. It is bidirectional when used with the 82C495SLC/XLC. Normally an input, MEMR# is an output only during ISA master cycles except during refresh. This signal is tied to MEMR# of the chipset.
MEMW#	69	I/O	Memory Write Command.: This signal is an input when used with the 82C499 and 82C80x chipsets. It is bidirectional when used with the 82C495SLC/XLC. Normally an input, MEMW# is an output only during ISA master cycles. This signal is tied to MEMW# of the chipset.
SMEMR#	73	I/O	AT Memory Read Low 1 Meg Command: This signal will follow MEMR# during a refresh cycle.
SMEMW#	74	I/O	AT Memory Write Low 1 Meg Command.
LMCS#/ KBCS#	70	I	Low 1 Meg Memory Chip Select or Keyboard Chip Select.

3.1.6   Real-time Clock Interface Signals

Name	No.	Type	Signal Description
ATIOR#/DS#/ PP1#/	18	I/O	On the 82C601, this pin is connected to the external RTC Data Strobe. On the 82C602, this pin is Power Port, bit 1. On the 82C495SLC/XLC, this a buffered IOR# for the AT bus. Refer to Table 4-1.
ATIOW#/RW#/ GPCS#/	19	I/O	On the 82C601, this pin is connected to R/W# on the external RTC chip. For the 82C602, this port is setup through Index Registers F8h and F9h. This signal is derived through the I/O read and write commands. For the 82C495SLC/XLC, this a buffered IOW# for the AT bus. Refer to Table 4-1
RRTCAS	26	O	On the82C601, this pin is connected to the address strobe of the external RTC chip. On the 82C602, this pin is reserved.
RRTCCS#/ PP2#	25	O	On the 82C601, this pin is connected to the chip select of the external RTC. On the 82C602, this pin is an output from the GREEN power control output. This pin can be accessed by either the PPEN# strobe signal or by Index Register FAh, depending on the configuration. Refer to Table 4-1

3.1.7   Keyboard Controller and GREEN Port Interface Signals

Name	No.	Type	Signal Description
KBCLK	21	O	Keyboard Clock - This is the clock signal to and from the keyboard.
KKBCLK	24	I	External Keyboard Clock: This is the clock signal from an external keyboard controller.
PPEN#	22	I	On the 82C601, this signal is reserved. On the 82C602, this pin is the GREEN power port enable, which latches the 82C802G's "AUTO_GREEN" port.
IRQ8	56	O	Interrupt Request 8: On the 82C601, this pin is reserved. On the 82C602, this signal is generated from the internal RTC.

3.1.7 Keyboard Controller and GREEN Port Interface Signals (cont.)

Name	No.	Type	Signal Description
PP0#	27	O	On the 82C601, this pin is reserved. On the 82C602, this pin is an output from the GREEN power control output. This pin can be accessed by either the PPEN# strobe signal or by Index Register FAh, depending on the configuration.

3.1.8 Miscellaneous Interface Signals

Name	No.	Type	Signal Description
MIO#	58	I	CPU Memory or I/O Status.
CPUCLK	20	I	CPU Clock: On the 82C601, this pin is reserved. On the 82C602, this pin is an input from the processor 1X clock signal.
X1	53	I	On the 82C601, this pin is reserved. On the 82C602, this pin is connected to the crystal for the internal RTC.
X2	54	O	On the 82C601, this pin is reserved. On the 82C602, this pin is connected to the crystal for the internal RTC.
VBATT	55	I	On the 82C601, this pin is reserved. On the 82C602, this pin is connected to the CMOS and RTC battery.

3.1.9 Power and Ground Pins

Name	No.	Type	Signal Description
VCC	14, 41, 57, 71, 91	I	Power Connection: +5V
GND	3, 15, 28, 40, 52, 66, 78, 90	I	Ground Connection

4.0 Functional Description

The 82C602 has all of the functionality of the 82C601 buffer chip, plus an embedded real-time clock and GREEN power port. These features are enabled through strapping options on the chip via the XD7, XD6, and XD4 signals. Table 4-1 summarizes these strapping options and explains the affects they have on pins 18, 19, and 25.

The following sub-sections will explain the differences between the 82C601 and 82C602. It will also give detailed information on various cycles and functional operations of the devices.

4.1 82C601 Functional Description

The 82C601 was designed to eliminate several buffering TTL devices typically found on motherboard designs. The 82C601 will substantially decrease the number of motherboard components and save PCB (printed circuit board) real estate. This creates higher integration which corresponds to higher reliability. The 82C601's functions are described next.

4.1.1 SD[7:0] to XD[7:0] Data Bus Control

The 82C80x, 82C495SLC/XLC, and 82C499 families drive the SD bus directly. The 82C601 provides a bidirectional buffer which controls the direction of the XD to SD bus. The XD bus is designed for devices which are not intended to drive the SD bus. These items include the RTC, keyboard controller and BIOS ROM. The direction of the internal buffer is controlled by the system logic chipset signal XDIR#.

4.1.2 CD[23:16] to SD[7:0] and/or CD[31:24] to SD[15:8] Data Bus Buffering

On the OPTi 82C80x and 82C499 chipsets, the third data byte is sourced from the CPU, hence it is not output by the chipset. In order to align the byte properly for the 16-bit ISA bus, control signals are generated by the chipset. The control for this alignment is done by HLBOE1#, HLBOE2#, and HLBTH#. On the 82C495SLC/XLC chipsets, the third and fourth byte are sourced from the CPU and not output by the chipset. This is controlled by the HLHDEN#, HDLEN#, and HDDIR# of the 82C495SLC/XLC.

4.1.3 CA[15:2] to SA[15:2] Address Buffering

The 82C601 buffers all of the local bus address lines to the ISA bus. These address lines normally drive the ISA bus and are inputs from the CPU during ISA master operations. During refresh, these buffers are disabled, allowing the refresh address to be broadcast to the ISA bus.

4.1.4 Refresh Counter and Refresh Address Logic

The 82C601 has its own built-in refresh counter. This refresh counter will broadcast the refresh address to the ISA bus during refresh cycles.

4.1.5 AEN Decode Signal

AEN is decoded by REF, MASTER#, and HLDA#. This signal is normally low and is driven high during DMA accesses.

4.1.6 AT Command Buffer Signals

The MEMR# and MEMW# signals are buffered to the ISA bus.

Table 4-1   82C601/82C602 Strapping Options

Description	XD7	XD6	XD4	Pin 18	Pin 19	Pin 25
82C602 Mode						
82C801/82C802 RTC Enabled	1	1	0	DS#	RW#	NC
82C495SLC/XLC RTC Enabled	1	0	0	ATIOR#	ATIOW#	NC
82C802G RTC Enabled	0	1	0	PP1#	GPCS#	PP2#
82C801/82C802 RTC Disabled	1	1	1	DS#	RW#	RRTCS#
82C495SLC/XLC RTC Disabled	1	0	1	DS#	RW#	RRTCS#
82C802G RTC Disabled	0	1	1	DS#	RW#	RRTCS#
82C601 Mode						
82C801/82C802	1	1	NA	DS#	RW#	RRTCS#
82C495SLC/XLC	1	0	NA	ATIOR#	ATIOW#	NC
Reserved	0	X	NA	DS#	RW#	RRTCS#

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4.1.7   Real Time Clock Control
Addresses 70h and 71h are decoded by the 82C601. These decoded addresses translate to RRTCCS# and RRTCAS strobes. This decode is needed for 82C802 designs. With 82C801 designs, the decode is done by the chipset.

4.1.8   Keyboard Clock buffer
The clock signal from the keyboard controller to the keyboard can be buffered through the 82C601. This clock is tristated through the buffer chip and sent out to the keyboard.

4.1.9   Reset Circuit
SYSRST# from the 82C801 is buffered through the 82C601. RSTDRV to the ISA bus and LRESET# to the VESA local bus are generated.

4.2   82C602 Functional Description
As previously stated, the 82C602 has all of the functionality of the 82C601 buffer chip, plus an embedded real-time clock and GREEN power port. The following sub-sections will explain these features.

4.2.1   Internal Real-Time Clock (RTC)
The internal RTC of the 82C602 is functionally compatible with the DS1285/MC146818B. The following sub-sections will give detailed functional and register features of the on-chip RTC of the 82C602.

4.2.1.1   RTC Features
- System wake-up capability -- alarm interrupt output active in battery back-up mode
- 2.7V to 3.6V operation; 4.5V to 5.5V operation
- 242 bytes of general non-volatile storage
- Direct clock/calendar replacement for IBM® AT-compatible computers and other applications
- Functionally compatible with the DS1285
  - Closely matches MC146818A pin configuration
- Less than 1.0μA load under battery operation

- 14 bytes for clock/calendar and control
- BCD or binary format for clock and calendar data
- Calendar in day of the week, day of the month, months, and years, with automatic leap-year adjustment
- Time of day in seconds, minutes, and hours
  - 12- or 24-hour format
  - Optional daylight saving adjustment
- Three individually maskable interrupt event flags:
  - Periodic rates from 122μs to 500ms
  - Time-of-day alarm once-per-second to-once-per-day
  - End-of-clock update cycle

4.2.1.2   RTC Overview
The on-chip RTC is a low-power microprocessor peripheral providing a time-of-day clock and 100 year calendar with alarm features and battery operation. The RTC supports 3.3V systems. Other RTC features include three maskable interrupt sources, square-wave output, and 242 bytes of general non-volatile storage.

Wake-up capability is provided by an alarm interrupt, which is active in battery back-up mode.

The RTC write-protects the clock, calendar, and storage registers during power failure. A back-up battery then maintains data and operates the clock and calendar.

The on-chip RTC is a fully compatible real-time clock for PC/AT-compatible computers and other applications. The only external components are a 32.768KHz crystal and a back-up battery.

4.2.1.3   RTC Address Map
The on-chip RTC provides 14 bytes of clock and control/status registers and 242 bytes of general non-volatile storage. Figure 4-1 illustrates the address map for the RTC.

Figure 4-1   RTC Address Map

14 Bytes	0	Clock and Control Status Registers	00		0	Seconds	00	
	13		00		1	Seconds Alarm	01	
114 Bytes	14	Storage Registers with EXTRAM = 0	0E		2	Minutes	02	
					3	Minutes Alarm	03	
	127		7F		4	Hours	04	BCD or Binary Format
128 Bytes	128	Storage Registers with EXTRAM = 1	80		5	Hours Alarm	05	
					6	Day of Week	06	
					7	Date of Month	07	
					8	Month	08	
					9	Year	09	
					10	Register A	0A	
					11	Register B	0B	
					12	Register C	0C	
	255		FF		13	Register D	0D	

4.2.1.4   Update Period

The update period for the RTC is one second. The RTC updates the contents of the clock and calendar locations during the update cycle at the end of each update period (see Figure 4-2). The alarm flag bit may also be set during the update cycle.

The RTC copies the local register updates into the user buffer accessed by the host processor. When a 1 is written to the update transfer inhibit bit (UTI) in Register B, the user copy of the clock and calendar bytes remains unchanged, while the local copy of the same bytes continues to be updated every second.

The update-in-progress bit (UIP) in Register A is set tBUC time before the beginning of an update cycle (see Figure 4-2). This bit is cleared and the update-complete flag (UF) is set at the end of the update cycle.

4.2.1.5   Programming the RTC

The time-of-day, alarm, and calendar bytes can be written in either the BCD or binary format (see Table 4-2).

These steps may be followed to program the time, alarm, and calendar:

1. Modify the contents of Register B:

    a. Write a 1 to the UTI bit to prevent transfers between RTC bytes and user buffer.

    b. Write the appropriate value to the data format (DF) bit to select BCD or binary format for all time, alarm, and calendar bytes.

    c. Write the appropriate value to the hour format (HF) bit.

2. Write new values to all the time, alarm, and calendar locations.

3. Clear the UTI bit to allow update transfers.

On the next update cycle, the RTC updates all ten bytes in the selected format.

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Figure 4-2   Update Period Timing and UIP
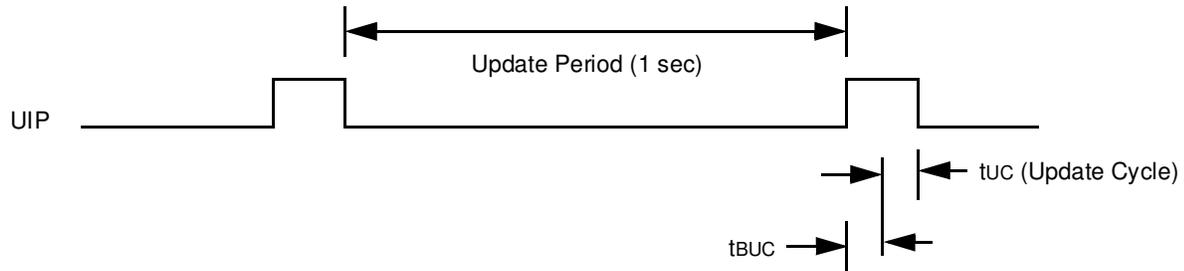
Table 4-2   Time, Alarm, and Calendar Formats

Address	RTC Bytes	Range		
		Decimal	**Binary**	**Binary-Coded Decimal**
0	Seconds	0-59	00h-3Bh	00h-59h
1	Seconds Alarm	0-59	00h-3Bh	00h-59h
2	Minutes	0-59	00h-3Bh	00h-59h
3	Minutes Alarm	0-59	00h-3Bh	00h-59h
4	Hours, 12-hour Format	1-12	01h-OCh am 81h-8Ch pm	01h-12h am 82h-92h pm
	Hours, 24-hour Format	0-23	00h-17h	00h-23h
5	Hours Alarm, 12-hour Format	1-12	01h-OCh am 81h-8Ch pm	01h-12h am 82h-92h pm
	Hours Alarm, 24-hour Format	0-23	00h-17h	00h-23h
6	Day of Week (1 = Sunday)	1-7	01h-07h	01h-07h
7	Day of Month	1-31	01h-1Fh	01h-31h
8	Month	1-12	01h-0Ch	01h-12h
9	Year	0-99	00h-63h	00h-99h

4.2.1.6 Square-wave Output
The RTC divides the 32.768KHz oscillator frequency to produce the 1Hz update frequency for the clock and calendar. Thirteen taps from the frequency divider are fed to a 16:1 multiplexor circuit. The output of this mux is fed to the SQW output and periodic interrupt generation circuitry. The four least-significant bits of Register A, RS[3:0], select among the 13 taps (see Table 4-3).

4.2.1.7 Interrupts
The RTC allows three individually selected interrupt events to generate an interrupt request. These three interrupt events are:

1. The periodic interrupt, programmable to occur once every 122µs to 500ms.

2. The alarm interrupt, programmable to occur once-per-second to once-per-day, is active in battery back-up mode, providing a "wake-up" feature.

3. The update-ended interrupt, which occurs at the end of each update cycle.

Each of the three interrupt events is enabled by an individual interrupt enable bit in Register B. When an event occurs, its event flag bit in Register C is set. If the corresponding event enable bit is also set, then an interrupt request is generated. The interrupt request flag bit (INTF) of Register C is set with every interrupt request. Reading Register C clears all flag bits, including INTF, and makes INT# high-impedance.

Two methods can be used to process RTC interrupt events:

1. Enable interrupt events and use the interrupt request output to invoke an interrupt service routine.

2. Do not enable the interrupts and use a polling routine to periodically check the status of the flag bits.

The individual interrupt sources are described in detail in the following sub-sections.

Table 4-3   Square-Wave Frequency/Periodic Interrupt Rate

Register A Bits				Square-Wave		Periodic Interrupt	
RS3	RS2	RS1	RS0	Frequency	Units	Period	Units
0	0	0	0	None		None	
0	0	0	1	256	Hz	3.90625	ms
0	0	1	0	128	Hz	7.8125	ms
0	0	1	1	8.192	KHz	122.070	µs
0	1	0	0	4.096	KHz	244.141	µs
0	1	0	1	2.048	KHz	488.281	µs
0	1	1	0	1.024	KHz	976.5625	µs
0	1	1	1	512	Hz	1.953125	ms
1	0	0	0	256	Hz	3.90625	ms
1	0	0	1	128	Hz	7.8125	ms
1	0	1	0	64	Hz	15.625	ms
1	0	1	1	32	Hz	31.25	ms
1	1	0	0	16	Hz	62.5	ms
1	1	0	1	8	Hz	125	ms
1	1	1	0	4	Hz	250	ms
1	1	1	1	2	Hz	500	ms

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4.2.1.7.1   Periodic Interrupt

The mux output used to drive the SQW output also drives the interrupt generation circuitry. If the periodic interrupt event is enabled by writing a 1 to the periodic interrupt enable bit (PIE) in Register C, an interrupt request is generated once every 122μs to 500ms. The period between interrupts is selected by the same bits in Register A that select the square-wave frequency (see Table 4-3). Setting OSC[2:0] in Register A to 011 does not affect the periodic interrupt timing.

4.2.1.7.2   Alarm Interrupt

The alarm interrupt is active in battery back-up mode, providing a "wake-up" capability. During each update cycle, the RTC compares the hours, minutes, and seconds bytes with the three corresponding alarm bytes. If a match of all bytes is found, the alarm interrupt event flag bit, AF in Register C, is set to 1. If the alarm event is enabled, an interrupt request is generated.

An alarm byte may be removed from the comparison by setting it to a "don't care" state. An alarm byte is set to a "don't care" state by writing a 1 to each of its two most significant bits. A "don't care" state may be used to select the frequency of alarm interrupt events as follows:

  A. If none of the three alarm bytes is "don't care," the frequency is once per day, when hours, minutes, and seconds match.

  B. If only the hour alarm byte is "don't care", the frequency is once per hour when minutes and seconds match.

  C. If only the hour and minute alarm bytes are "don't care", the frequency is once per minute when seconds match.

  D. If the hour, minute, and second alarm bytes are "don't care", the frequency is once per second.

## 4.2.1.7.3   Update Cycle Interrupt

The update cycle ended flag bit (UF) in Register C is set to a 1 at the end of an update cycle. If the update interrupt enable bit (UIE) of Register B is 1, and the update transfer inhibit bit (UTI) in Register B is 0, then an interrupt request is generated at the end of each update cycle.

4.2.1.8   Accessing RTC bytes

The EXTRAM pin must be low to access the RTC's registers. Time and calendar bytes read during an update cycle may be in error. Three methods to access the time and calendar bytes without ambiguity are:

  1. Enable the update interrupt event to generate interrupt requests at the end of the update cycle. The interrupt handler has a maximum of 999ms to access the clock bytes before the next update cycle begins (see Figure 4-3).

  2. Poll the update-in-progress bit (UIP) in Register A. If UIP = 0, the polling routine has a minimum of tBUC time to access the clock bytes (see Figure 4-3).

  3. Use the periodic interrupt event to generate interrupt requests every tPI time, such that UIP = 1 always occurs between the periodic interrupts. The interrupt handler has a minimum of tPI/2 + tBUC time to access the clock bytes (see Figure 4-3).

Figure 4-3   Update-Ended/Periodic Interrupt Relationship
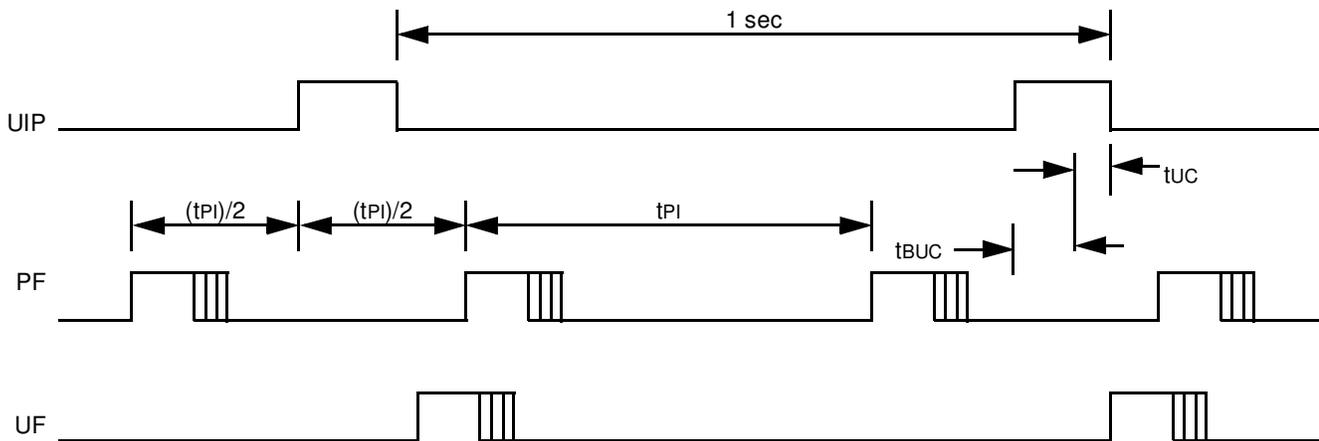
4.2.1.9 RTC Time-Base Crystal

The RTC's time-base oscillator is designed to work with an external piezoelectric 32.768KHz crystal. A crystal can be represented by its electricaL equivalent circuit and associated parameters as shown in Figure 4-4 and Table 4-4, respectively.

L1, C1, and R1 form what is known as the motional arm of the circuit. C0 is the sum of the capacitance between electrodes and the capacitance added by the leads and mounting structure of the crystal. The equivalent impedance of the crystal varies with the frequency of oscillation. Figure 4-5 shows the variation of the equivalent reactance, X , with respect to frequency.

There are two frequencies at which the crystal impedance appears purely resistive (X_E = 0). They re indicated by two points on the graph, known as the series resonant (F_S) and anti-resonant (F_A) frequencies. Oscillators operating the crystal at the resonant frequency (F_S) are termed series resonant circuits, whereas those that operate the crystal around F_A are termed parallel resonant. The on-chip RTC uses a parallel resonant oscillator circuit. The frequency of oscillation in this mode lies between F_S and F_A and is dictated by the effective load capacitance appearing across the crystal inputs, as explained next.

Table 4-4   Crystal Parameters

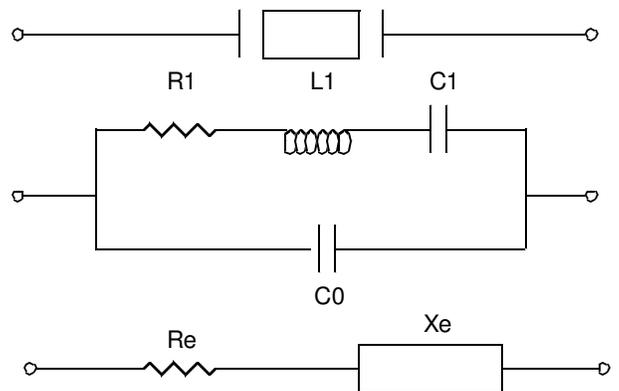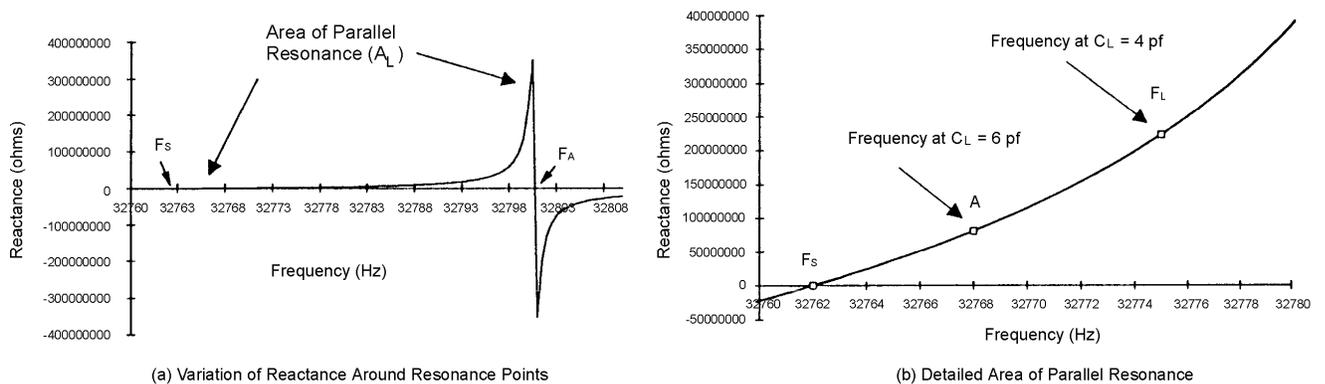| Parameter	Symbol	Value	Unit
Nominal Frequency	F	32.768	KHz
Load Capacitance	C_L	6	pF
Motional Inductance	L1	9076.66	H
Motional Capacitance	C1	2.6×10^{-3}	pF
Motional Resistance	R1	27	KΩ
Shunt Capacitance	C0	1.1	pF

Figure 4-4   Quartz Crystal Equivalent Circuit

Figure 4-5   Equivalent Reactance Versus Frequency

(a) Variation of Reactance Around Resonance Points

(b) Detailed Area of Parallel Resonance

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4.2.1.9.1   RTC Oscillator

The parallel resonant RTC oscillator circuit is comprised of an inverting micro-power amplifier with a PI-type feedback network. Figure 4-6 illustrates a block diagram of the oscillator circuit with the crystal as part of the PI-feedback network. The oscillator circuit ensures that the crystal is operating in the parallel resonance region (AL in Figure 4-5) of the impedance curve.

The actual frequency at which the circuit will oscillate depends on the load capacitance, C_L. This parameter is the dynamic capacitance of the total circuit as measured or computed across the crystal terminals. A parallel resonant crystal like the DT-26 is calibrated at this load using a parallel oscillator circuit. C_L is computed from C_{L1} and C_{L2} as given below:

$$C_L = (C_{L1} * C_{L2}) / (C_{L1} + (C_{L2})$$

The RTC's C_{L1} and C_{L2} values are trimmed to provide approximately a load capacitance (C_L) of 6pF across crystal terminals. This is to match the specified load capacitance (6pf) at which the recommended DT-26 crystal is calibrated to resonate at the nominal frequency of 32.768KHz. Referring to the impedance graph of Figure 4-5, "A" indicates the point of resonance when C_L equals the specified load capacitance of the crystal.

4.2.1.9.2   Time Keeping Accuracy

The accuracy of the frequency of oscillation depends on:

*   Crystal frequency tolerance
*   Crystal frequency stability
*   Crystal aging
*   Effective load capacitance in oscillator circuit
*   Board layout

Crystal Frequency Tolerance

The frequency tolerance parameter is the maximum frequency deviation from the nominal frequency (in this case 32.768KHz) at a specified temperature, expressed in ppm (parts per million) of nominal frequency. In the case of the Grade A DT-26 crystal, this parameter is ±20 ppm at 25°C.

Crystal Frequency Stability

This parameter, dependent on the angle and type of cut, is defined as the maximum frequency deviation from the nominal frequency over a specified temperature range, expressed in ppm or percentage of nominal frequency.

Figure 4-7 shows a typical curve of frequency variation with temperature for the KDS DT-26 crystal.

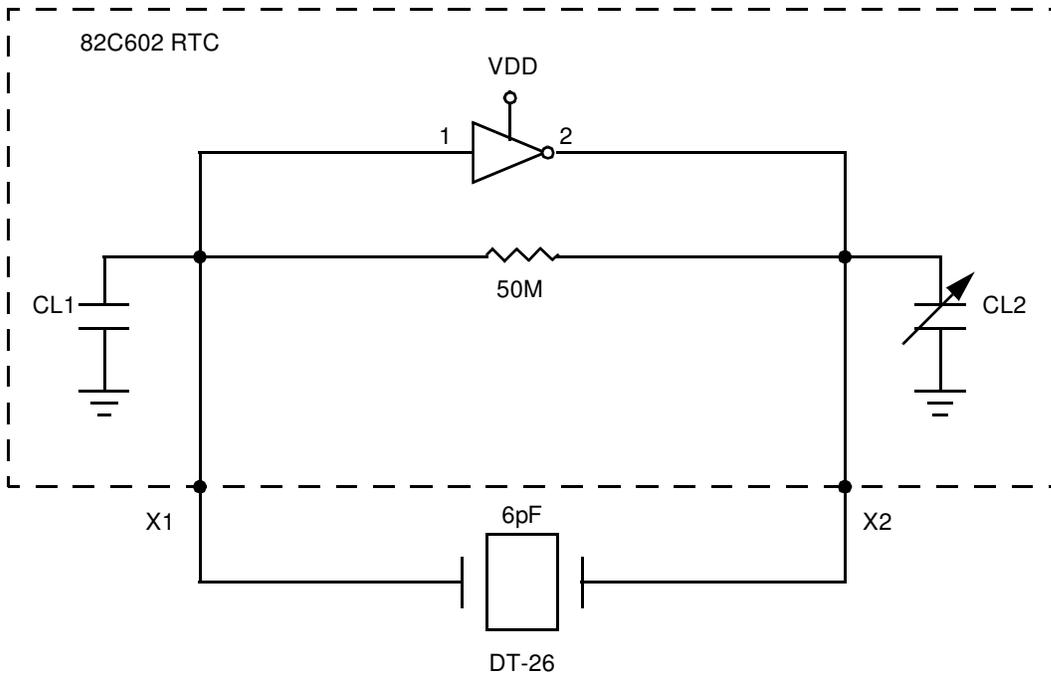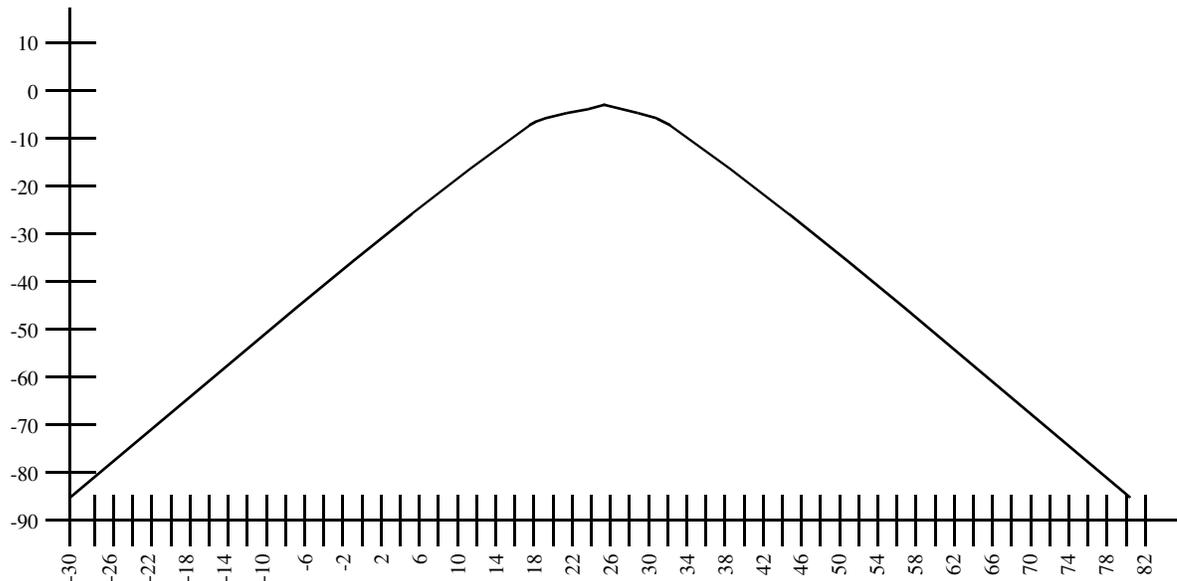**Figure 4-6   RTC Oscillator Circuit Block Diagram**

Figure 4-7   Typical Temperature Characteristics

Crystal Aging
As a crystal ages, some frequency shift may be observed. Drift with age is specified to be typically 4 ppm for the first year and 2 ppm per year for the life of the KDS DT-26 crystal.

Load Capacitance
For a parallel resonant calibrated crystal, the crystal manufacturer specifies the load capacitance at which the crystal will "parallel" resonate at the nominal frequency. From the graph of Figure 4-5, increasing the effective load capacitance by hanging additional capacitors on either of the X1 or the X2 pin will effectively lower the resonant frequency point "A" toward Fs. The deviation of the frequency Fl with load capacitance is given by:

$$F_L = F_S (1 + C1/2 (C0 + C_L))$$

where C1 is the crystal motional capacitance and C0 is the crystal shunt stray capacitance, as explained above. C_L is the effective load capacitance across the crystal inputs.

Allowing for capacitance due to board layout traces leading to the X1 and X2 pins, the RTC is trimmed internally to provide an effective load capacitance of less than 6pF. Connecting a 6pF crystal directly to the X1 and X2 pins will cause the clock to oscillate approximately 24 ppm faster than the nominal frequency of 32.768KHz, for reason explained previously.

For maximum accuracy, it is recommended that a small trim capacitor (< 8pF) be hooked to the X2 pin to move the resonant point closer to the nominal frequency. The graph of Figure 4-9 shows the variation of frequency with additional load capacitance on the X2 pin of the RTC.

Translating the data in Figure 4-9 into a practical rule of thumb: for every additional 1.54pF capacitance on the X2 pin, the frequency will decrease by 0.8Hz or a ∆F/F of -24.4 ppm around 82.768KHz.

Board Layout
Given the high input impedance of the crystal input pins X1 and X2, care should be taken to route high-speed switching signal traces away from them. Preferably a ground-plane layer should be used around the crystal area to isolate capacitive-coupling of high frequency signals. The traces from the crystal leads to the X1 and X2 pins must be kept short with minimal bends. A good rule of thumb is to keep the crystal traces within 5mm of the X1 and X2 pins.

Finally, a 0.1μF ceramic by-pass capacitor should be placed close to the VCC pin of the RTC to provide an improved supply into the clock

4.2.1.9.3   Oscillator Start-up
Barring accuracy issues, the RTC will oscillate with any 32.768KHz crystal. When hooked to the X1 and X2 pins in certain configurations, however, passive components can lead to oscillator start-up problems:

•   Excessive loading on the crystal input pins X1 and X2

•   Use of a resistive feedback element across the crystal.

Figure 4-8 shows "good" and "bad" circuit configurations for the RTC oscillator.

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Figure 4-8   Typical Crystal Hookup Circuits
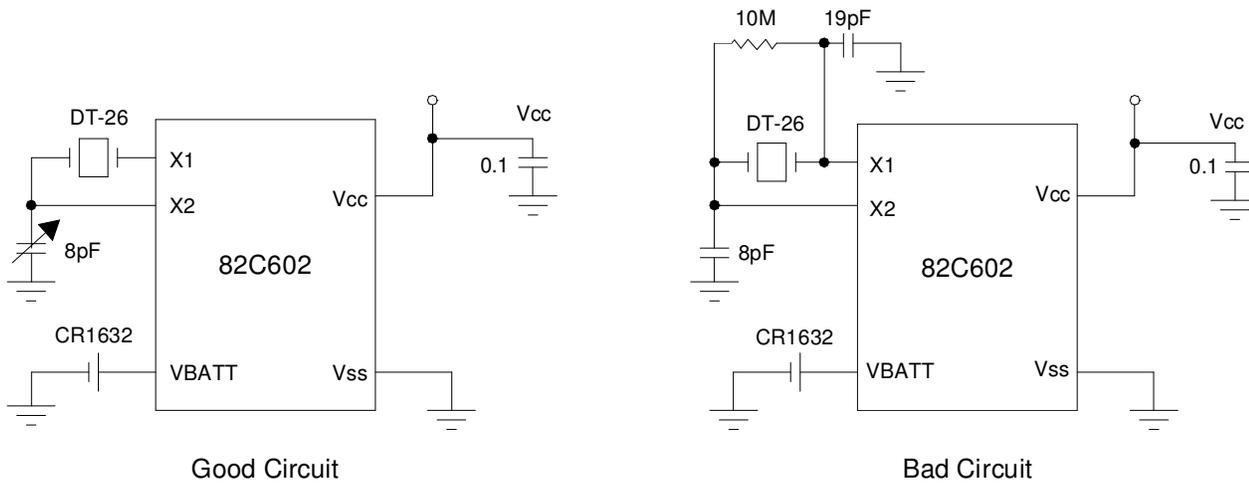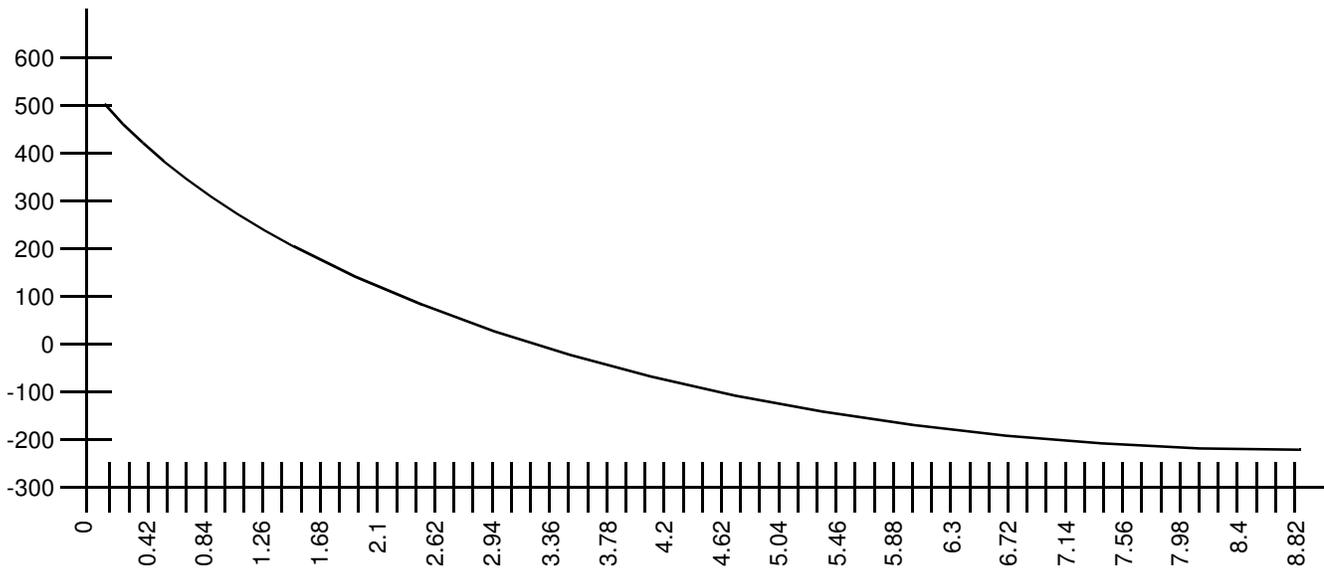

Good Circuit

Bad Circuit

Figure 4-9   Frequency Variation Versus Load Capacitance

Values above 10pF on either the X1 or X2 pin must be avoided. The feedback element is build into the RTC for start-up and no resistive feedback external to the part is required.

4.2.1.9.4   Oscillator Control
When power is first applied to the RTC and VCC is above V_{PFD}, the internal oscillator and frequency divider are turned on by writing a 010 pattern to bits 4 through 6 of Register A. A pattern of 011 behaves as 010 but additionally transforms

Register C into a read/write register. This allows the 32.768KHz output on the square-wave pin to be turned on. A pattern of 11X turns the oscillator on, but keeps the frequency divider disabled. Any other pattern to these bits keeps the oscillator off.

4.2.1.10   Power-Down/Power-Up Cycle
The RTC's power-up/power-down cycles are different. The RTC continuously monitors VCC for out-of-tolerance. During

a power failure, when VCC falls below V$_{PFD}$ (2.53V typical), the RTC write-protects the clock and storage registers. The power source is switched to BC when VCC is less than V$_{PFD}$ and BC is greater than V$_{PFD}$, or when VCC is less than V$_{BC}$ and V$_{BC}$ is less than V$_{PFD}$. RTC operation and storage data are sustained by a valid back-up energy source. When VCC is above V$_{PFD}$, the power source is VCC. Write-protection continues for t$_{CSR}$ time after VCC rises above V$_{PFD}$.

The RTC continuously monitors VCC for out-of-tolerance. During a power failure, when VCC falls below V$_{PFD}$ (4.17V typical), the RTC write-protects the clock and storage registers. When VCC is below V$_{BC}$ (3V typical), the power source is switched to BC. RTC operation and storage data are sustained by a valid back-up energy source. When VCC is above V$_{BC}$, the power source is VCC. Write-protection continues for t$_{CSR}$ time after VCC rises above V$_{PFD}$.

4.2.1.11 Recommended VBATT Input Logic
Considering the current consumption and input voltage specifications of the 82C602 VBATT pin, a 3.6V lithium cell is a recommended power source for the VBATT input pin. Due to low battery current consumption of the 82C602, the life of a 3.6V lithium battery may be as high as ten years. No additional part is needed to generate the VBATT input of the 82C602. The 82C602 incorporates circuitry to protect battery

reverse charging, which eliminates the need for the external protection diodes that are typically mounted for UL certification.

4.2.1.12 Control/Status Registers
The four control/status registers of the RTC are accessible regardless of the status of the update cycle (see Table 4-5).

4.2.1.12.1 Register A
Register A programs the frequency of the periodic event rate, and oscillator operation. Register A provides the status of the update cycle. See Table 4-6 for Register A's format.

4.2.1.12.2 Register B
Register B enables the update cycle transfer operation, square-wave output-interrupt events, and daylight saving adjustment. Register B selects the clock and calendar data formats. See Table 4-7 for Register B's format.

4.2.1.12.3 Register C
Register C is a read-only event status register. See Table 4-8 for Register C's format.

4.2.1.12.4 Register D
Register D is a read-only data integrity status register. See Table 4-9 for Register D's format.

Table 4-5   Control/Status Registers Summary

Register	Loc. (Hex)	Read	Write	Bit Name and State on Reset														
				7 (MSB)		6		5		4		3		2		1		0 (MSB)	
A	0A	Yes	Yes[1]	UIP	NA	OSC2	NA	OSC1	0	OSC0	0	RS3	NA	RS2	NA	RS1	NA	RS0	NA
B	0B	Yes	Yes	UTI	NA	PIE	0	AIE	0	UIE	0	SQWE	0	DF	NA	HF	NA	DSE	NA
C	0C	Yes	No[2]	INTF	0	PF	0	AF	0	UF	0	-	0	32KE	0	-	0	-	0
D	0D	Yes	No	VRT	NA	-	0	-	0	-	0	-	0	-	0	-	0	-	0

NOTE   Na = Not Affected
1. Except Bit 7
2. Read/write only when OSC[2:]0 in Register A is 011 (binary).

Table 4-6   Register A

Bit(s)	Type	Default	Function
7	RO		UIP - Update-In-Progress: This read-only bit is set prior to the update cycle. When UIP equals 1, an RTC update cycle may be in progress. UIP is cleared at the end of each update cycle. This bit is also cleared when the update transfer inhibit (UTI) bit in Register B is 1.
6:4			OSC[2:0] - Oscillator Control Bits 2 through 0: These three bits control the state of the oscillator and divider stages. A pattern of 010 enables RTC operation by turning on the oscillator and enabling the frequency divider. A pattern of 11X turns the oscillator on, but keeps the frequency divider disabled. When 010 is written, the RTC begins its first update after 500ms.

Bit(s)	Type	Default	Function
3:0			RS[3:0] - Rate Select Bits 3 through 0: These bits select one of the 13 frequencies for the SQW output and the periodic interrupt rate, as shown in Table 4-2.

Table 4-7   Register B

Bit(s)	Type	Default	Function
7	R/W		UTI - Update Transfer Inhibit: This bit inhibits the transfer of RTC bytes to the user buffer. 1 = Inhibits transfer and clears UIE 0 = Allows Transfer
6	R/W		PIE - Periodic Interrupt Enable: This bit enables an interrupt request due to a periodic interrupt event. 1 = Enabled 0 = Disabled
5	R/W		AIE - Alarm Interrupt Enable: This bit enables an interrupt request due to an alarm interrupt event. 1 = Enabled 0 = Disabled
4	R/W		UIE - Update Cycle Interrupt Enable: This bit enables an interrupt request due to an update ended interrupt event. 1 = Enabled 0 = Disabled The UIE bit is automatically cleared when the UTI bit equals 1.
3	R/W		SQWE - Square-wave Enable: This bit enables the square-wave output. 1 = Enabled 0 = Disabled and Held Low
2	R/W		DF - Data Format: This bit selects the numeric format in which the time, alarm, and calendar bytes are represented. 1 = Binary 0 = BCD
1	R/W		HF - Hour Format: This bit selects the time-of-day and alarm hour format. 1 = 24-Hour Format 0 = 12-Hour Format
0	R/W		DSE - Daylight Saving Enable: This bit enables daylight saving time adjustments when written to 1. On the last Sunday in October, the first time the RTC increments past 1:59:59 AM, the time falls back to 1:00:00 am. On the first Sunday in April, the time springs forward from 2:00:00 am to 3:00:00 am.

Table 4-8   Register C

Bit(s)	Type	Default	Function
7	R/W		INTF - Interrupt Request Flag: This flag is set to a 1 when any of the following is true: AIE = 1 and AF = 1 PIE = 1 and PF = 1 UIE = l and UF=1 Reading Register C clears this bit.
6	R/W		PF - Periodic Event Flag: This bit is set to a 1 every tPI time, where tPI is the time period selected by the settings of RS[3:0] in Register A. Reading Register C clears this bit.

Bit(s)	Type	Default	Function
5	R/W		AF - Alarm Event Flag: This bit is set to a 1 when an alarm event occurs. Reading Register C clears this bit.
4	R/W		UF - Update Event Flag: This bit is set to a 1 at the end of the update cycle. Reading Register C clears this bit.
3	R/W	0	NU - Not Used - This bit is always set to 0.
2			
1:0	R/W	00	NU - Not Used - These bits are always set to 0.

Table 4-9   Register D

Bit(s)	Type	Default	Function
7	RO		VRT - Valid RAM and Time: 1 = Valid backup energy source 0 = Backup energy source is depleted When the backup energy source is depleted (VRT = 0), data integrity of the RTC and storage registers is not guaranteed.
6:0	RO		NU - Not Used - These bits are always set to 0.

4.2.2   GREEN Power Port

The GREEN Port on the 82C602, when coupled with the 82C802G, provides a means of controlling devices via output pins on the device. During the power saving mode, this port can be written to by the system software or can latch data from the 82C802G's port.

This port can be written to by Index Register FAh. The lower nibble will be written to the output port on the 82C602. During the SMI handler, this port may be written to slow the CPU clock, issue a STPCLK# signal to the CPU, control video monitor syncs, and control other peripheral power states. When PPEN# is active, and bit 6 of Index F9h is set, the

GREEN Power Port will latch the data from Index EAh onto the 82C602's output pins. When this bit is cleared, the GREEN Power Port will only respond to actual writes to Index FAh.

On OPTi's reference platform, PP0# has been used as CLKCNT both to the clock synthesizer and to the CPU's STP-CLK# input. PP1# has been used to control VSYNC and PP2# has been used to control HSYNC. These outputs can have any type of configuration. If configured in this arrangement, platforms can run off of similar BIOS.   This register is write-only.

Table 4-10   GPM Port - Index: FAh

Bit(s)	Type	Default	Function
7:3	WO	0000 0	Reserved
2	WO	1	PP2#: Hsync Control
1	WO	1	PP1#: Vsync Control
0	WO	1	PP0#: Clock Control

5.0   Register Descriptions

Table 5-1   General Purpose Chip Select Registers - Index: F7h and F8h

Bit(s)	Type	Default	Function
7:0	WO	0000 0000	General Purpose Chip Select I/O Address. Register F7h holds bits A[15:8]. Register F8h holds bits A[7:0].

These ports, enabled through Index Register F9h, contain an address which will be compared during an I/O instruction to trigger a GPCS#. Optional masking bits in Index Register F9h allow a range of addresses to be selected.

Table 5-2   General Purpose Chip Select Register - Index F9h

Bit(s)	Type	Default	Function
7	WO	0	General Purpose Chip Select Polarity: 0 = Active High 1 = Active Low
6	WO	0	PPEN# Strobe: When cleared, this pin will be ignored. When set, it will latch the contents of Index EAh into Index FAh. 1 = Latch Data on the GREEN Power Port 0 = Do Not Latch Data on the GREEN Power Port
5	WO	0	Upper 128 bytes of CMOS: 1 = Enable Upper 128 bytes of CMOS (Disable Lower 114 bytes) 0 = Enable Lower 114 bytes of CMOS (Normal Mode/Disables Upper 128 bytes)
4:2	WO	000	Mask Bits: **4** **3** **2** **Description** 0 0 0 Mask No Bits 0 0 1 Mask Lowest Bit 0 1 0 Mask Lowest 2 Bits 0 1 1 Mask Lowest 3 Bits 1 0 0 Mask Lowest 4 Bits 1 0 1 Mask Lowest 5 Bits 1 1 0 Reserved (do not program) 1 1 1 Reserved (do not program)
1:0	WO	00	Qualify for General Purpose Chip Select: **1** **0** **Description** 0 0 Decoded with AEN, Address Decode and IOW# 0 1 Decoded with AEN, Address Decode and IOR# 1 0 Decoded with AEN, Address Decode only 1 1 Decoded with AEN, Address Decode, IOW#, and IOR#

This register enables/disables the general purpose chip select. It also contains which bits to mask for selecting a specific address or a range of addresses for the GPCS#. This register is write-only.

Table 5-3   GPM Port - Index: FAh

Bit(s)	Type	Default	Function
7:3	WO	0000 0	Reserved
2	WO	1	PP2#: Green power port Bit 2
1	WO	1	PP1#: Green power port Bit 1
0	WO	1	PP0#: Green power port Bit 0

6.0   Maximum Ratings

Stresses above those listed in the following tables may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification are not implied.

6.1   Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit
V_{CC}	Supply Voltage		+6.5	V
V_I	Input Voltage	-0.5	V_{CC}+0.5	V
V_O	Output Voltage	-0.5	V_{CC}+0.5	V
T_{OP}	Operating Temperature	0	+70	°C
T_{STG}	Storage Temperature	-40	+125	°C
V_{BATT}	Input Voltage, Battery Pin	-0.5	+5.5	V

6.2   DC Characteristics: T_A = 0°C to +70°C, V_{CC} = 5.0V ±5%

Symbol	Parameter	Min	Max	Unit	Condition
V_{IL}	Input Low Voltage	-0.5	0.8	V	
V_{IH}	Input High Voltage	2.0	V_{CC}+0.5	V	
V_{OL}	Output Low Voltage		0.5	V	
V_{OH}	Output High Voltage	2.4		V	
I_{IL}	Input Leakage Current		10	µA	
I_{OZ}	Tristate Leakage Current		10	µA	
C_{IN}	Input Capacitance		10	pF	
C_{OUT}	Output Capacitance		10	pF	
C_{IO}	I/O Capacitance		12	pF	
I_{CC}	Power Supply Current		TBD	mA	
V_{BATT}	Input Voltage, Battery Pin	2.5	4.0	V	For normal operation
I_{VBATT}	Power supply for RTC/CMOS RAM	-	1.0	µA	Standby

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6.3   AC Timing Characteristics - *Preliminary -* Temperature: 0°C to +70°C, VCC: 5V +/- 5%

Symbol	Parameter	Min	Max	Units	Condition
t100	HLBOE1# Active to SD[7:0] Valid	4	18	ns	
t101	HLBOE1# Inactive to SD[7:0] Invalid	4	18	ns	
t103	HLBOE2# Active to CD[23:16] Valid (HLBLTH# Inactive)	4	18	ns	
t104	HLBOE2# Inactive to CD[23:16] Invalid (HLBLTH# Active)	4	18	ns	
t105	HLBLTH# Inactive to Previous CD[23:16] Latch Invalid	4	18	ns	
t106	HLBLTH# Inactive to New CD[23:16] Valid Delay	4	18	ns	
t107	SD[7:0] Valid to CD[23:16] Valid Delay (HLBLTH# Inactive)	4	18	ns	
t108	SD[7:0] Invalid to CD[23:16] Invalid Delay (HLBLTH# Inactive)	4	18	ns	
t110	XD[7:0] Valid to SD[7:0] Valid Delay (XDIR# is Active)	4	18	ns	
t111	XD[7:0] Invalid to SD[7:0] Invalid Delay (XDIR# is Active)	4	18	ns	
t112	SD[7:0] Valid to XD[7:0] Valid Delay (XDIR# is Inactive)	4	18	ns	
t113	SD[7:0] Invalid to XD[7:0] Invalid Delay (XDIR# is Inactive)	4	18	ns	
t114	RFSH# Active to REF Active	4	18	ns	
t115	RFSH# Inactive to REF Inactive	4	18	ns	
t116	MEMR# Active to SMEMR# Active (LMCS# is Active)	4	18	ns	
t117	MEMR# Inactive to SMEMR# Inactive (LMCS# is Active)	4	18	ns	
t118	MEMW# Active to SMEMW# Active (LMCS# is Active)	4	18	ns	
t119	MEMW# Active to SMEMW# Active (LMCS# is Active)	4	18	ns	
t120	CA[15:2] Valid to SA[15:2] Valid (MASTER# is Inactive)	3	18	ns	
t121	CA[15:2] Invalid to SA[15:2] Invalid (MASTER# is Inactive)	6	20	ns	
t122	SA[15:2] Valid to CA[15:2] Valid (MASTER# is Active)	3	18	ns	
t123	SA[15:2] Invalid to CA[15:2] Invalid (MASTER# is Active)	3	18	ns	
t124	RFSH# Active to SA[9:2] Valid	4	18	ns	
t125	RFSH# Inactive to SA[9:2] Invalid	4	18	ns	
t126	RFSH# Active to SA[15:10] Tristated	4	18	ns	
t127	RFSH# Inactive to SA[15:10] Valid	4	18	ns	
t128	MASTER# Active to AEN Inactive	4	18	ns	
t129	MASTER# Inactive to AEN Active	6	18	ns	
t130	RFSH# Active to AEN Active	4	18	ns	
t131	RFSH# Inactive to AEN Inactive	6	18	ns	
t140	KBCLK↑ Delay from KKBCLK↑	4	18	ns	
t141	KBCLK↓ Delay from KKBCLK↓	3	18	ns	
t142	RST# Active to LRESET# Active	4	18	ns	

Symbol	Parameter	Min	Max	Units	Condition
t143	RST# Inactive to LRESET# Inactive	4	18	ns	
t144	RST# Active to RSTDRV Active	4	18	ns	
t145	RST# Inactive to RSTDRV Inactive	6	18	ns	
t150	IOR# Active to DS# Active Delay (RTC Address is Decoded)	9	20	ns	
t151	IOR# Inactive to DS# Inactive Delay (RTC Address is Decoded)	3	18	ns	
t152	IOW# Active to R/W# Active Delay (RTC Address is Decoded)	8	20	ns	
t153	IOW# Inactive to R/W# Inactive Delay (RTC Address is Decoded)	3	18	ns	
t154	IOW# Active to RRTCAS Active Delay (RTC Address is Decoded)	6	20	ns	
t155	IOW# Inactive to RRTCAS Inactive Delay (RTC Address is Decoded)	8	20	ns	
t156	A[9:0] Valid to RRTCCS# Active	8	20	ns	
t157	A[9:0] Invalid to RRTCCS# Inactive	5	18	ns	

NOTE   1. ↑ means rising edge
         2. ↓ means falling edge
         3. The capacitance loading is 50 pf

6.4   AC Timing Waveforms

Figure 6-1   CD[23:16] to SD[7:0] Timing
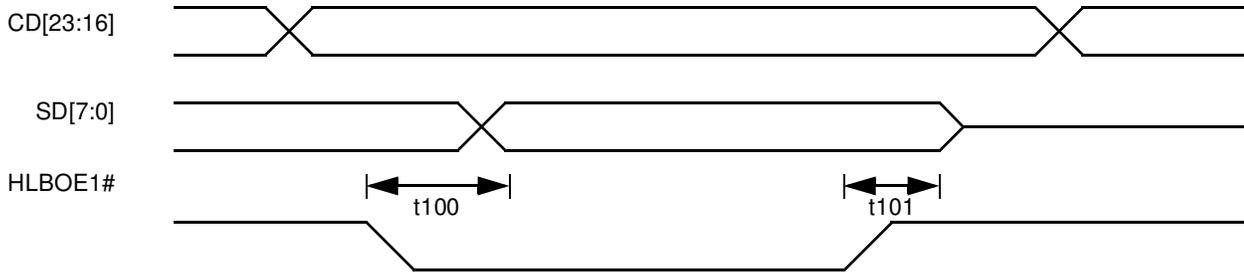
Figure 6-2   SD[7:0] to CD[23:16] Timing
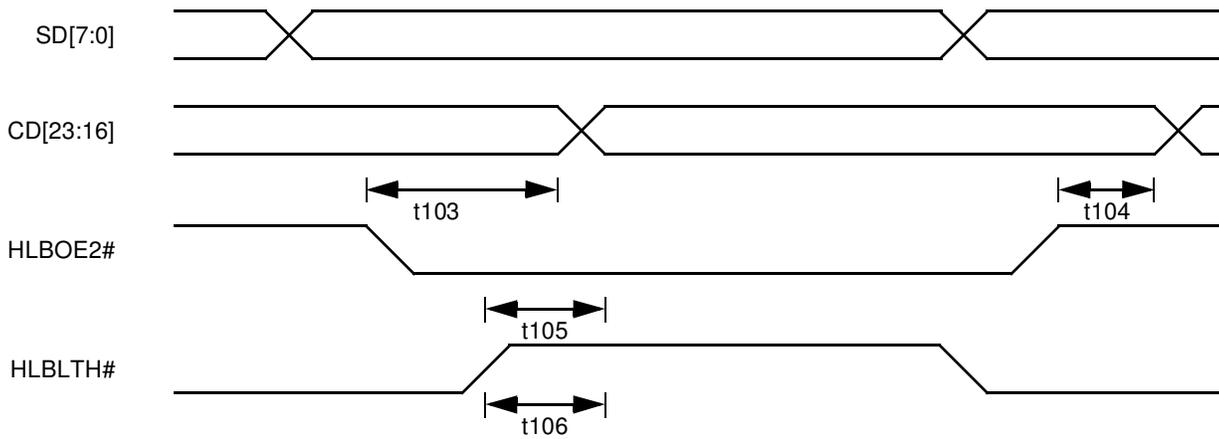
Figure 6-3   SD[7:0] to CD[23:16] Timing
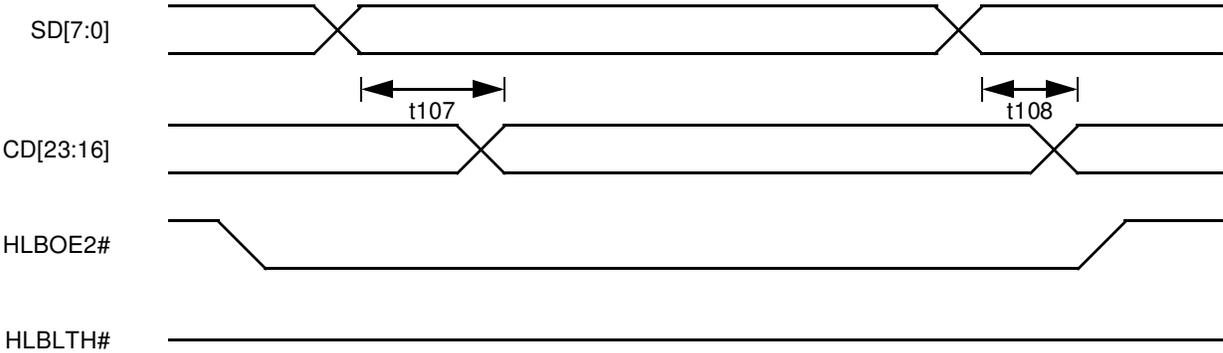
Figure 6-4   XD[7:0] to SD[7:0] Timing
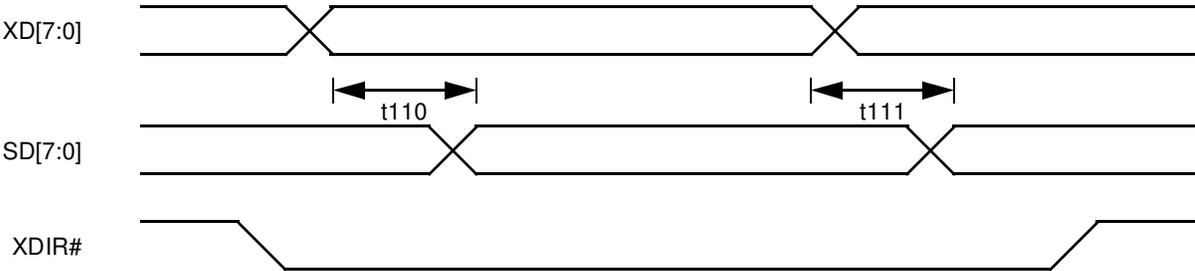
Figure 6-5   SD[7:0] to XD[7:0] Timing
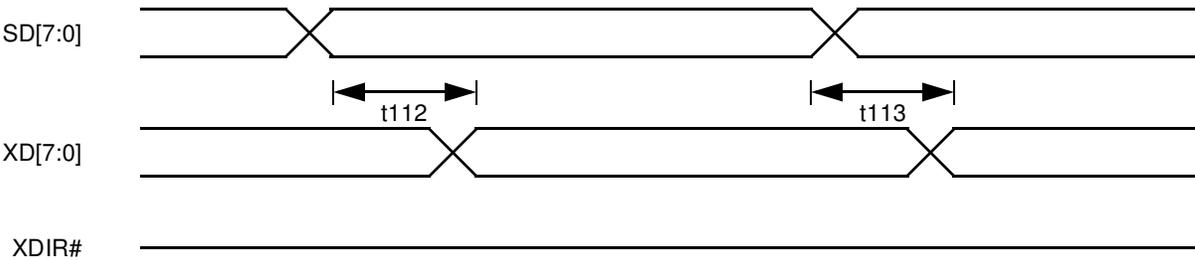
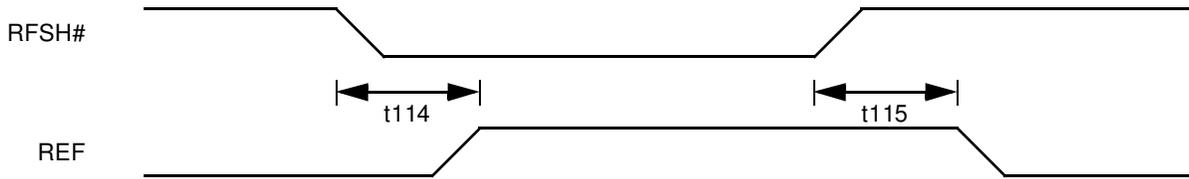# 82C601/82C602

Figure 6-6   RFSH# to REF Delay Timing

Figure 6-7   Normal Memory Strobe to Lower 1MB Memory Strobe Timing
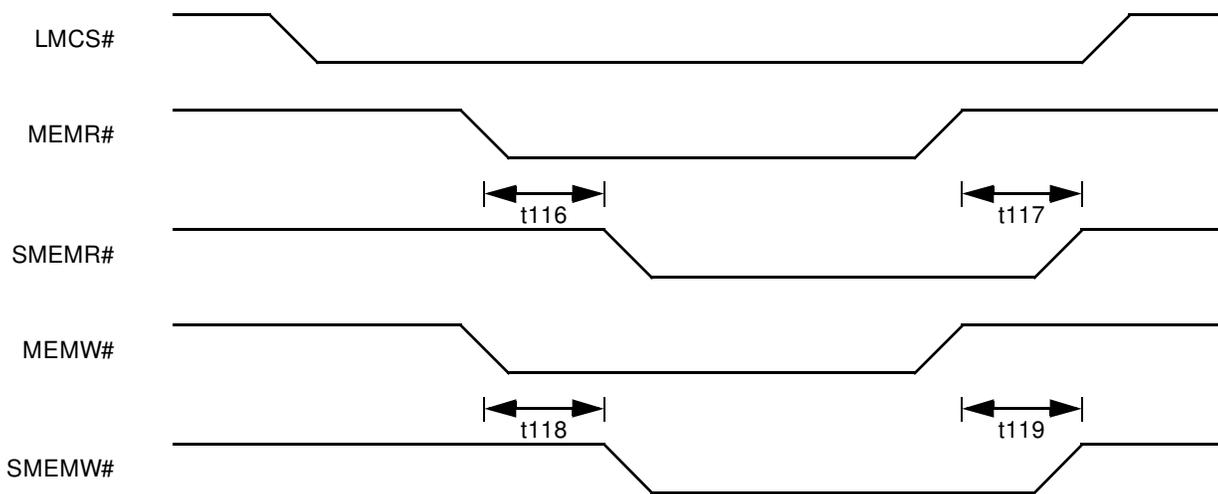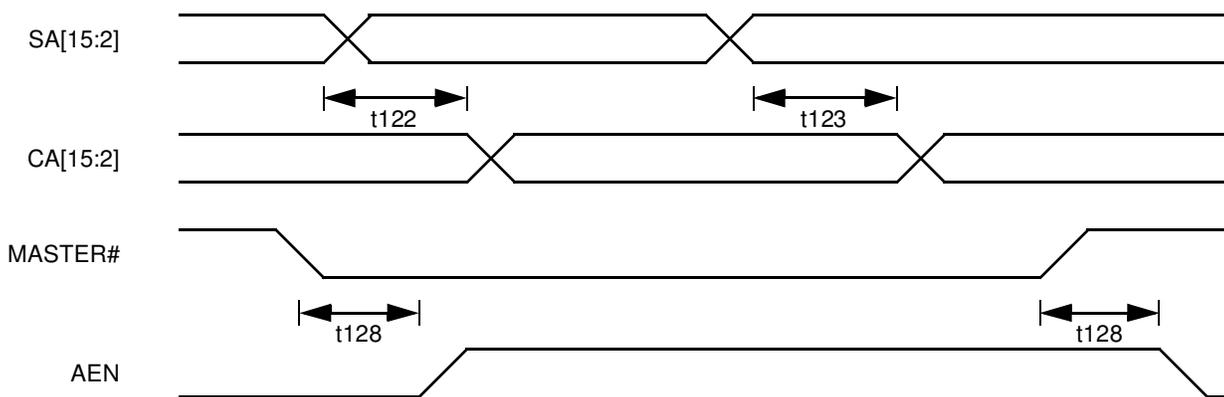

Figure 6-8   Master Mode Word SA to CA Address Timing

Figure 6-9   Normal Word CA to SA Address Timing
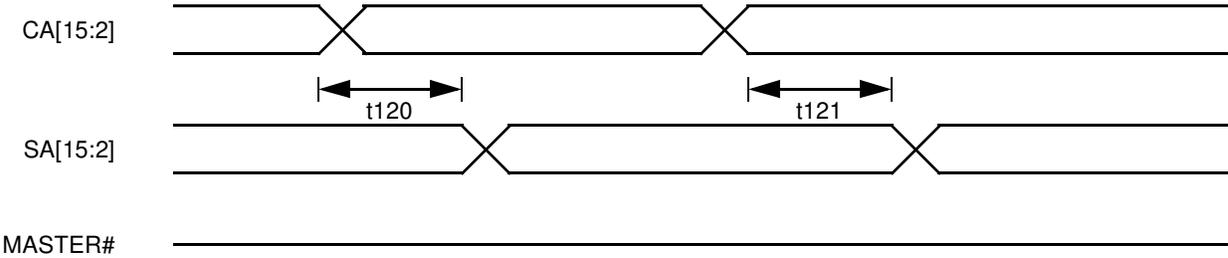
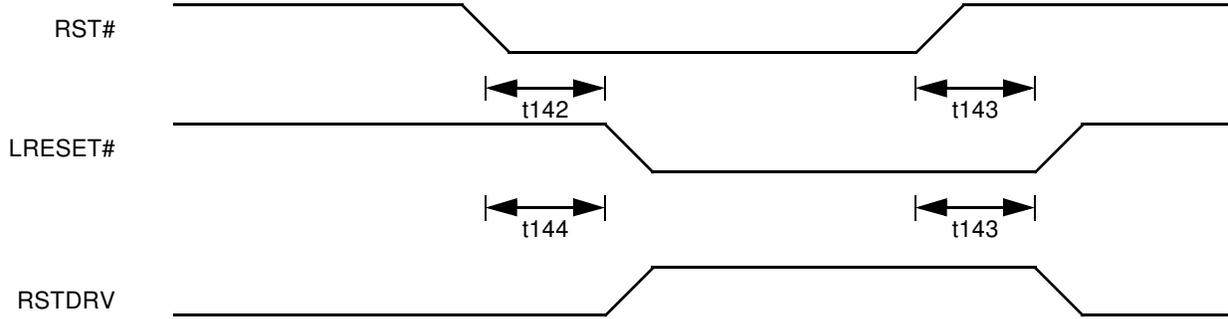**Figure 6-10   Refresh Timing**
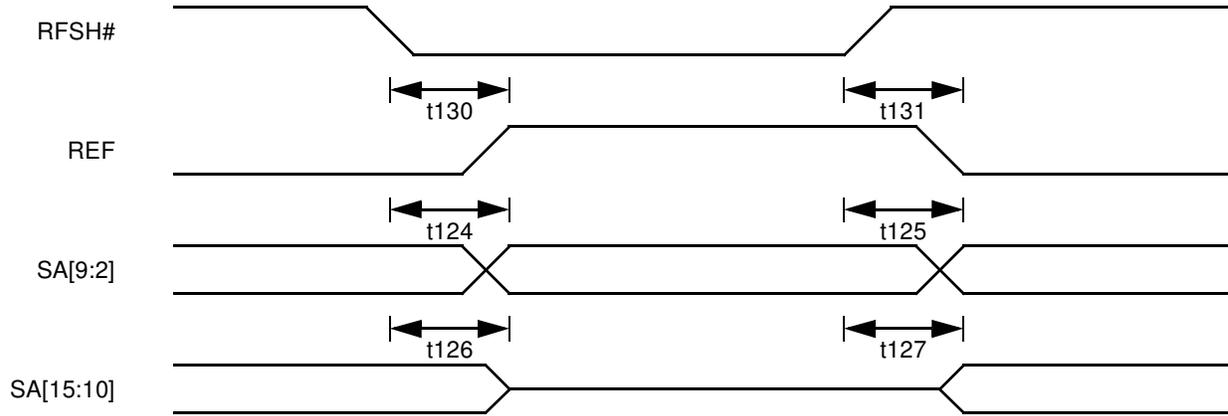
Figure 6-11   Reset Timing
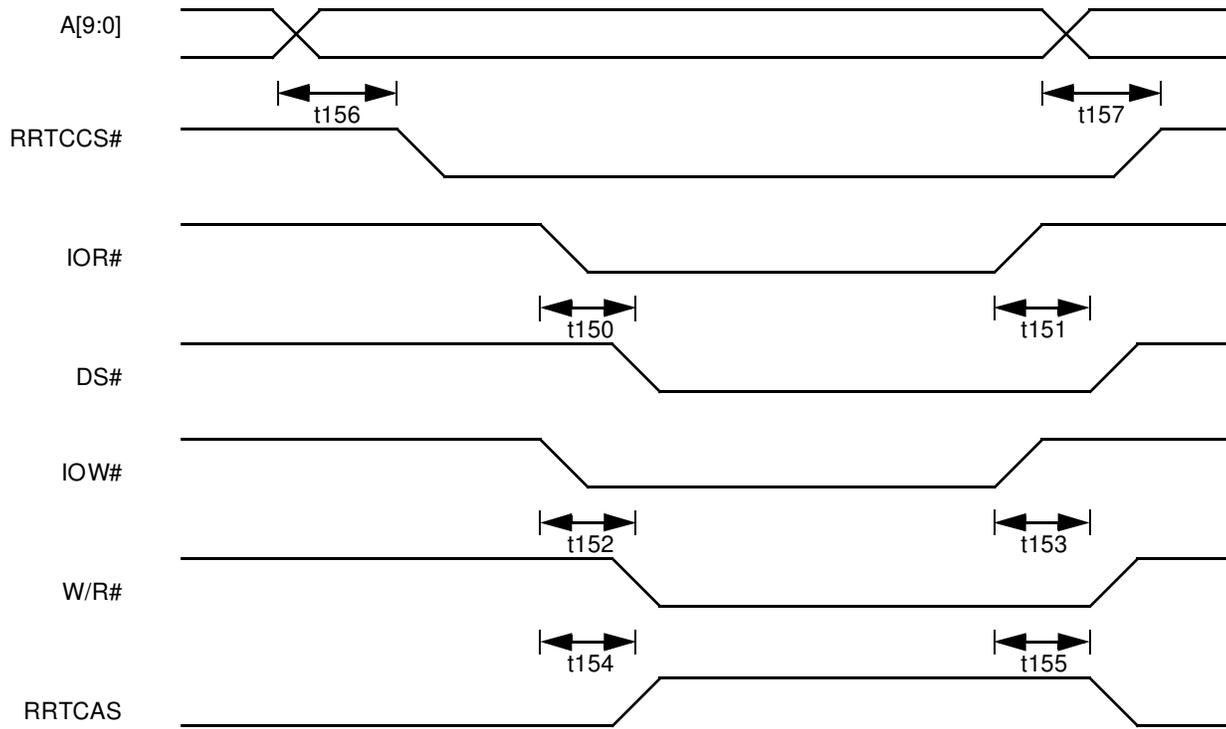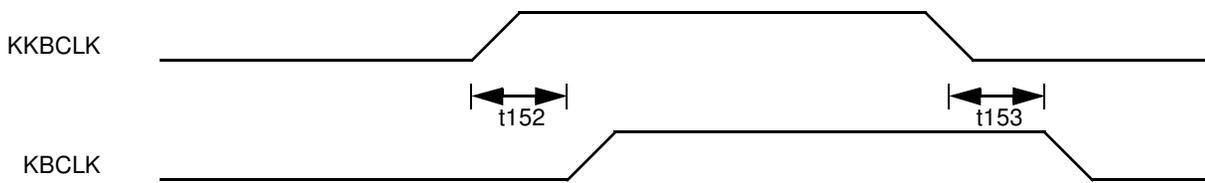
Figure 6-12   Real-time Clock Timing
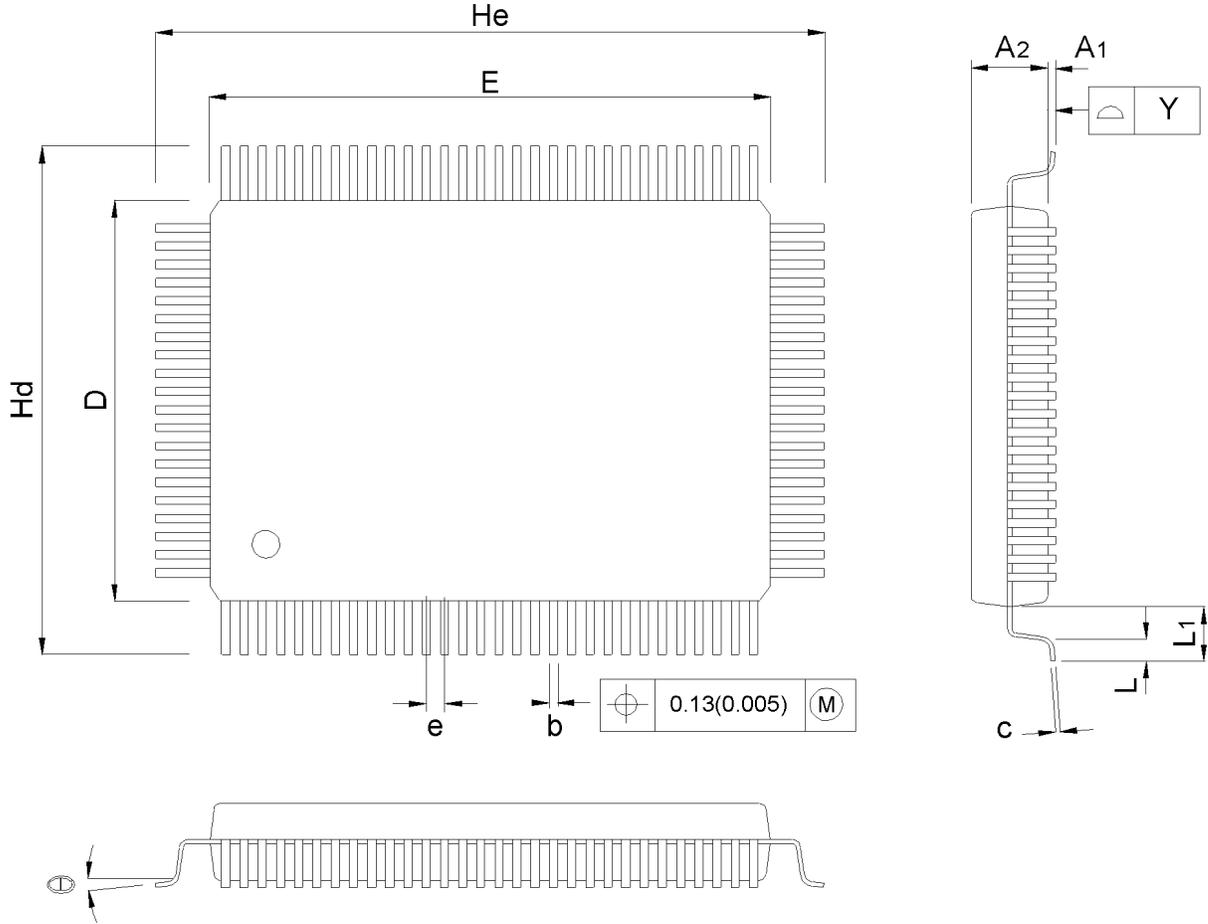

Figure 6-13   Keyboard Clock Buffer Timing

7.0 Mechanical Package Outline

Figure 7-1   100-Pin Plastic Flat Pack (PFP)

SYMBOL	MILLIMETER MIN.	MILLIMETER NOM.	MILLIMETER MAX.	INCH MIN.	INCH NOM.	INCH MAX.
A1	0.25	0.35	0.45	0.010	0.014	0.018
A2	2.57	2.72	2.87	0.101	0.107	0.113
b	0.20	0.30	0.40	0.008	0.012	0.016
c	0.10	0.15	0.20	0.004	0.006	0.008
D	13.90	14.00	14.10	0.547	0.551	0.555
E	19.90	20.00	20.10	0.783	0.787	0.791
e		0.65			0.026	
Hd	17.00	17.20	17.40	0.669	0.677	0.685
He	23.00	23.20	23.40	0.905	0.913	0.921
L	0.65	0.80	0.95	0.025	0.031	0.037
L1		1.60			0.063	
Y			0.08			0.003
⊕	0		7	0		7

Dwg. No.:	AS100PQFP-001
Dwg. Rev.: A0	Unit: MM/INCH