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Applications Note

Product Name: 82C465MV Portable Core Logic Chipset

Title: Using the Cyrix 486DX/DX2 3.3V L1 cache write-back CPU with the 82C465MV

Date:

Overview

This application note addresses hardware and software issues with using the Cyrix Cx486DX/DX2 CPUs with the 82C465MV Portable Core Logic Chipset.

Discussion

- The SMM memory space is always re-mapped by the 82C465MV to the memory segments at A0000h and B0000h. The 82C465MV can remap to this location from any memory segment 0-9; the SMM memory location in the Cyrix CPU is also programmable.
- Cyrix CPUs are static devices, which means that the clock change protocol is not needed for changing the CPU clock (slow down or stop); however, when doing the stop clock, for the sake of power consumption (Cyrix CPU consumes much less power when stop clock hand shake is implemented), it is recommended that the clock change protocol be used. Cyrix CPU uses a stop clock scheme which requires two signals, SUSP# and SUSPA#. The 82C465MV supports this scheme with some registers and straps setup described in this document.
- The Phoenix BIOS which supports the Cyrix CPU is on the OPTi BBS; the file name is CYRIX.ZIP. The BBS number is (408) 980-9774.
- 465MV(A) Rev. 3 evaluation board has full jumper settings for this Cyrix CPU; no extra wiring is needed for this evaluation board.
- Since the cache scheme in the CPU is write-back, it is not necessary to put any level-two cache on board. This application on the 465MV(A) Rev. 3 board will not have any level-two cache.

Application example on OPTi 82C465MV(A) Rev. 3 demo board

Jumper settings

Function	Jumper	State
HITM# signal routing	JP 200	close
SUSPA# signal routing	JP 201	2-3
FERR# signal routing	JP 45	close
No L2 Cache support strap	JP 40	1-2
STPCLK# CPU strap	JP 37	1-2
1X clock CPU strap	JP 30	2-3
No L2 cache routings	XJP6~ XJP21	1-2
Disconnect SDENL#, SDENH# signals	JP 42, 43	open
KBDCS# signal without L2 cache	JP 218	2-3
CPU BOFF# signal (2-3 if 82C465MV is used)	JP 210	1-2
ROMCS# signal without L2 cache	JP 216	2-3
ROMCS# signal connection without L2 cache	JP 217	1-2

Others

Do not put any jumpers on JP56, JP57, JP58, JP59, JP65, JP62, JP63, JP66.

Registers Setup

1. For CPU clock changing or CPU stop clock
   - Program Cyrix CPU register C2h[7] to 1 to enable the SUSP# and SUSPA# pins.
   - Program register 66h[3] to 1. Converts 82C465MV pin 171 to become STPGNT# signal instead of PIO3 signal, since the Cyrix CPU uses STPGNT# (SUSPA#) signal to notify the chipset that it is ready to change or stop the clock.
   - Program register 57h[3] to 0. Set pin 171 of the 465MV to input, in order to activate the input function of the signal STPGNT#.
   - Program register 61h[2] to 1. Enable the STPCLK# signal.
   - Program register 65h[6] to 1 for stopping the CPU clock. 82C465MV will latch the STPCLK# signal active while stopping the CPU clock.
   - Program register 66h[5] and 66h[0] to 1. Enable stop clock signal and enable clock change protocol.
   - Program register B0h to 80h. Setup the delay time with “no delay” since the Cyrix CPU is a static device; however, clock change protocol is going to be activated when stopping the CPU clock.
   - Refer to the data book for other general setup required.
2. For SMI function
   - Program Cyrix CPU registers CDh with 00h, CEh with 00h, and CF with 66h which is the suggested SMM code starting address.
   - Program Cyrix CPU register C1h[1] to 1 to enable the SMI pins (SMI# and SMADS#).

- Program 5Bh[4] to 1. The 82C465MV will automatically setup the default value of '76' in register AFh, and implement the Cyrix SMI signal scheme.
- Setup register 30h bit 3 and 31h bit 4 to 1, and load the SMM code to the 6000:0h to 7000:0h area. However, the starting address has to match the starting address setup in the CPU.
- Program 31h[4] to 0 to lock the SMM address space.
- Refer to the data book for other general SMI setup required.

3. For Cyrix CPU write back cache scheme support
   - Program Cyrix CPU register C2h[1] to 1 to enable WM_RST and INVAL input pins and HITM# output pin. Note that the HITM# signal will not be driven by Cyrix CPU before this bit is programmed, so a 10K pull up on the HITM# signal is recommended.
   - Program Cyrix CPU register C2h[6] to 1 to enable the burst write function for the CPU. Note that the 82C465MV supports burst write function only when an L1 write-back CPU is used.
   - Program 82C465MV register A0[1] to 1 to enable the write-back CPU support.
   - Program the 82C465MV register D1[7] for the appropriate HITM# signal sensing. Program to 0 is recommended for 33Mhz or lower CPU frequency.

If there are additional questions, please contact OPTi's Portable Applications Department at (408) 980-8178.