APPLICATION		REVISIONS			
NEXT ASSY	USED ON	APPROVED	DATE	DESCRIPTION	REV
				PCN# 32010	A
				PCN# 32043	B

Tish Morgan 2/21/84

1MB

BY G.Piorkowski	DATE 1/84	TITLE Technical Manual	
CHK		NS23S	
APPD [signature]	1-26-84	1MB Memory Module	
APPD [signature]	1-26-84		

National Semiconductor Corporation
2900 Semiconductor Drive, Santa Clara, Calif 95051

SIZE	DWG NO	REV
A	420110014-001	B

SHEET 1 OF 43

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CHAPTER I
General Description

1.0 Introduction

The NS23S Memory Card is an add-in memory for the Digital Equipment Corporation (DEC)* LSI-11 Microcomputer Systems.

The card has been designed to be mechanically and electrically compatible with the LSI-11, LSI-11/2, MICRO/PDP-11, PDP11/23 and PDP11/23-Plus systems. The NS23S is compatible with DEC MSV11-L series Semiconductor Memory Modules, and can be installed in the H9270, H9273-A, H9275(A), H9276, MICRO/PDP-11 and DDV11-B backplanes.

Note - The NS23S will not fit in the 'dual' height only H9281 backplane.

1.1 Memory Capacity

The standard memory capacity of the NS23S is 524,288 words by 18 bits (512KW x 18 bits), with optional capacities available.

The starting address of the NS23S can be assigned anywhere within the LSI-11 128KW address space in 4KW increments, or within the LSI-11 2MW address space in 4KW increments if extended addressing is implemented.

1.2 Modes of Operation

The NS23S is capable of operating within the five modes required by the LSI-11 systems:

A) Read (DATI)
B) Write (DATO, DATOB)
C) Read-Modify-Write (DATIO, DATIOB)
D) Read Block (DATBI)
E) Write Block (DATBO)

The read and block modes operate on the full 16-bit memory word. The write modes can operate on either the full word (16 bits) or on a byte (8 bits), except DATBO which can only operate on the full word. The NS23S provides its own refresh timing and addresses.

* DEC, PDP, and MICRO/PDP-11 are Digital Equipment Corporation Trademarks

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1.3 Timing

The timing characteristics of the NS23S are listed in Table 1-1.

Memory Function	Bus Cycle Type	Access Time (Max.)	Cycle Time (Max.)
Read	DATI	50NS	450NS
Write	DATO (B)	50NS	450NS
Read/Modify/Write	DATIO (B)	500NS	925NS
Read Block	DATBI	50NS	450NS
Write Block	DATBO	50NS	450NS

Table 1-1. Access and Cycle Timing

If a memory cycle is requested during a refresh operation, a delay of up to 550NS can be added to the above cycle times.

Read (DATI) access time is defined as Internal SYNC H to RPLY H with 25NS from SYNC H to DIN H. Write (DATO) access time is defined as Internal SYNC H to RPLY H with 50NS from SYNC H to DOUT H. Cycle time is defined as SYNC H to SYNC H at the maximum speed that the memory will operate. All timings are taken at bus receiver outputs and bus driver inputs.

1.4 Power Requirements

The NS23S requires only +5 volts ±5%. The current requirements are listed in Table 1-2.

	Typical	Maximum
+5 Volts	2.0A	2.5A
+5 VBB	1.5A	1.7A

Table 1-2. Power Requirements

1.5 Mechanical Description

The NS23S is a "Quad" size module and conforms to the "Quad Height" DEC backplane specification. The memory card is completely contained on one multilayer printed circuit board and is designed to plug directly into standard LSI-11 backplanes and the DDV11-B ("Hex") expansion backplane.

- CAUTION -

Do not attempt to install the NS23S in an ADAC 1000 backplane. This backplane is not compatible with newer LSI-11 systems for memory expansion.

1.6 Dimensions

Table 1-3 illustrates the dimensions of the NS23S memory module.

PCB Thickness	.056 Inches
PCB Width	10.436 Inches
PCB Length	8.575 Inches
Max. Component Height	.375 Inches
Total Thickness Max.	.490 Inches

Table 1-3. Dimensions

1.7 Environmental Specifications

The NS23S Memory Card will operate under the following environmental conditions:

Temperature = 0° to 55°C
Humidity = 10% to 90%
(no condensation)

1.8 Reliability and Maintainability

The NS23S was designed to the best commercial standards of workmanship. Reliable service is ensured by a high degree of testing conducted over the operating temperature spectrum.

The maintainability of the memory card is enhanced by the following features:

A) No timing adjustments are required. The only adjustment is the insertion of option jumpers.

B) The same card is usable over the entire LSI-11 address space.

C) All RAMs are installed in sockets for ease of field failure replacement. A spare on-board RAM is provided to assure that down-time is kept to an absolute minimum.

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CHAPTER II
Theory and Operation

2.0 General

This section describes the theory and operation of the NS23S Memory Module in DEC LSI-11 systems.

2.1 Interface Specification

Bus receiver voltage ranges from a minimum of 1.3V to a maximum of 1.7V. Maximum input current is 80uA when connected to 3.8V even with no power applied.

Bus driver output low voltage is .7V maximum when sinking 70 mA. Output high leakage current is 25uA when connected to 3.8V even if no power is applied.

2.2 Interface Signals

There are seven (7) input control signals, four (4) output control signals, and eighteen (18) bidirectional signal lines (address and data) on the NS23S Memory Card. The signals are described in the following sections.

2.2.1 Input Control Signals

Table 2-1 shows the input control signals. The NS23S presents one standard bus load to the LSI-11 system bus for each of these signals.

Signal Name	Connector Pin
BDOUT L	AE2
BDIN L	AH2
BSYNC L	AJ2
BWTBT L	AK2
BBS7 L	AP2
BDCOK H	BA1
BINIT L	AT2

Table 2-1. Input Control Signals

* BDOUT L (AE2)

This signal, when asserted, indicates that valid data is available on BDAL0-15 and that an output transfer is taking place.

* DIN L (AH2)

This signal, when asserted along with BSYNC, indicates that an input transfer is taking place and that the selected slave device is required to respond by asserting BRPLY and placing data on BDAL 0-15.

* BSYNC L (AJ2)

This signal, when asserted, indicates that a valid address is on the bus. When the address is in the operating range of the memory module, BSYNC will also initiate a memory cycle. The type of memory cycle will be determined by BDIN, BDOUT and BWTBT. BSYNC will remain asserted until the transfer is completed.

If BBS7 is asserted, then a CSR read or write cycle will occur if CSR address recognition occurred.

* BWTBT L (AK2)

This signal, when asserted during the leading edge of BSYNC, indicates a write cycle (DATO, DATBO, or DATOB) is to be executed. If asserted during the duration of BDOUT, a byte write (DATOB or DATIOB) will take place. The byte to be written is determined by the state of BDAL0 during the leading edge of BSYNC. BDAL0 = 0 indicates byte 0; BDAL0 = 1 indicates byte 1.

* BBS7 L (AP2)

This signal, when asserted during the leading edge of BSYNC indicates an I/O operation is requested. If address bits 1-12 match the CSR address, then a CSR read or write cycle will occur. During DATBI transfers, the bus master asserts this signal with the first data transfer until the last transfer to indicate to the slave that there will be subsequent transfers.

* BDCOK H (BA1)

This signal goes active (high) 3ms min. after DC voltages are in tolerance and is negated 5us min. before DC voltages are out of tolerance.

It prevents the memory card from being selected during power-up or power-down sequences or while in the battery back-up mode.

* BINIT L (AT2)

This signal is used to reset the CSR register.

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2.2.2 Output Control Signals

Table 2-2 illustrates the NS23S output control signals and a description of each signal follows.

Signal Name	Connector Pin
PARERR	AC1 (BDAL 16)
ERR ENABLE	AD1 (BDAL 17)
BRPLY L	AF2
BREF L	AR1

Table 2-2. Output Control Signals

* PARERR (AC1)

  BDAL 16 is used to indicate that a memory parity error has occurred.

* ERR ENABLE (AD1)

  BDAL 17 is the memory error enable line.

* BRPLY L (AF2)

  This signal is asserted in response to a memory cycle request. During write cycles (DATO, DATBO, DATIO), RPLY indicates acceptance of data from the bus. During read cycles (DATI, DATBI, DATIO), RPLY indicates that valid data will be on the bus within 125NS and will remain until RPLY is negated.

* BREF L (AR1)

  BREF L has two functions on the NS23S:

  1) If not using block mode transfers, BREF L is used as an external refresh input.

  2) If using block mode transfers, the NS23S will assert BREF L during BRPLY time to indicate that it is capable of accepting another block mode transfer.

2.2.3 Bi-directional Signals

The eighteen (18) bi-directional signal lines provide the memory card with address and data information. These lines are time-multiplexed between the address and data in/out during any cycle requested of the memory card. Table 2-3 lists the bi-directional signals.

Signal	Pin
BDAL 0L	AU2
BDAL 1L	AV2
BDAL 2L	BE2
BDAL 3L	BF2
BDAL 4L	BH2
BDAL 5L	BJ2
BDAL 6L	BK2
BDAL 7L	BL2
BDAL 8L	BM2
BDAL 9L	BN2
BDAL 10L	BP2
BDAL 11L	BR2
BDAL 12L	BS2
BDAL 13L	BT2
BDAL 14L	BU2
BDAL 15L	BV2
BDAL 16L	AC1
BDAL 17L	AD1

Table 2-3. Bi-directional Signals

The NS23S interprets the data on the bi-directional lines to be address information -75 to +25 nanoseconds around the leading edge of BSYNC L. At all other times the information on these lines is interpreted by the card as either data into or data out of the NS23S.

2.3 I/O Connector Pin List

The I/O connector pin list is shown in Table 2-4. Connectors C and D of the NS23S are not used for any bus connectors.

Component Side	Pin	Pin	Solder Side
A Connector			
	A1	A2	+5 Volts
	B1	B2	
BDAL16 L	C1	C2	Ground
BDAL17 L	D1	D2	
	E1	E2	BDOUT L
	F1	F2	BRPLY L
	H1	H2	BDIN L
Ground	J1	J2	BSYNC L
	K1	K2	BWTBT L
	L1	L2	
Ground	M1	M2	BIAKI L
	N1	N2	BIAKO L
	P1	P2	BBS7 L
	R1	R2	BDMGI L
BREF L	S1	S2	BDMGO L
Ground	T1	T2	BINIT L
	U1	U2	BDAL00 L
	V1	V2	BDAL01 L
B Connector			
BDCOK H	A1	A2	+5V Volts
	B1	B2	
BDAL18 L	C1	C2	Ground
BDAL19 L	D1	D2	
BDAL20 L	E1	E2	BDAL02 L
BDAL21 L	F1	F2	BDAL03 L
	H1	H2	BDAL04 L
Ground	J1	J2	BDAL05 L
	K1	K2	BDAL06 L
	L1	L2	BDAL07 L
Ground	M1	M2	BDAL08 L
	N1	N2	BDAL09 L
	P1	P2	BDAL10 L
	R1	R2	BDAL11 L
	S1	S2	BDAL12 L
Ground	T1	T2	BDAL13 L
	U1	U2	BDAL14 L
+5 Volts	V1	V2	BDAL15 L

Table 2-4. I/O Connector Pin List

2.4 Timing

The NS23S utilizes a 200NS delay line for internal timing. The delay is triggered by the read/write and refresh flip-flops.

Figures 2-1 through 2-5 illustrate the data transfer operations of the NS23S. Figure 2-6 is the NS23S Block Diagram and Figure 2-7 is the External Refresh Timing Waveform

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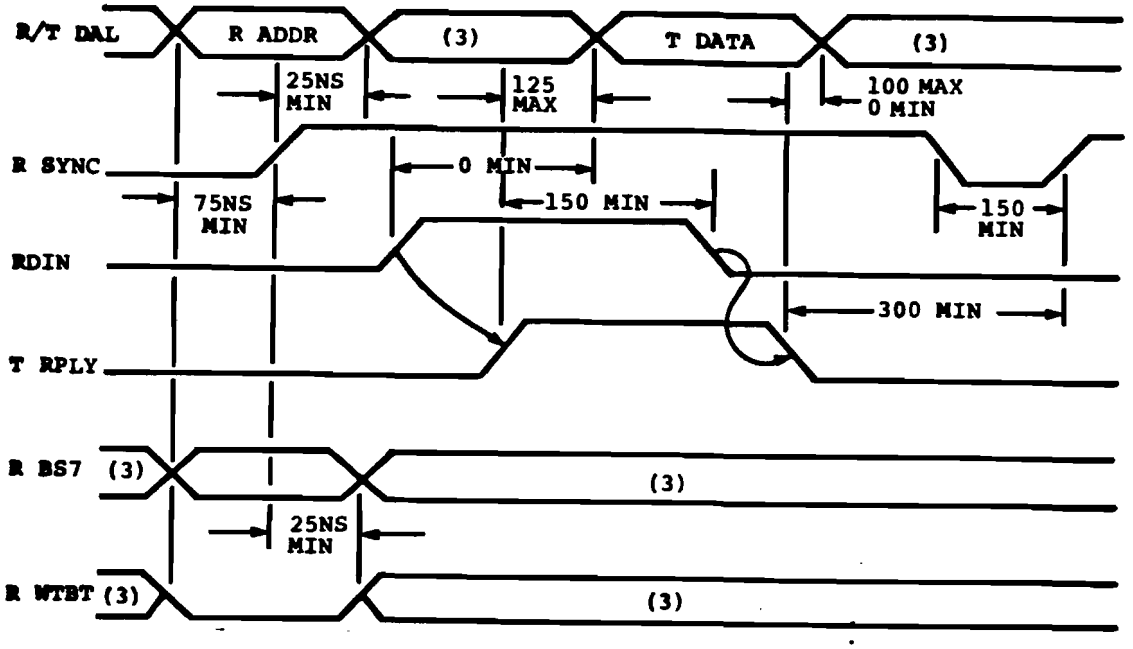

Figure 2-1. DATI Bus Cycle Timing

Notes:
1) Timing shown at Bus Driver Inputs and Bus Receiver Outputs.
2) T = Bus Driver Input
   R = Bus Receiver Output
3) Don't care condition
4) All timings given in nanoseconds

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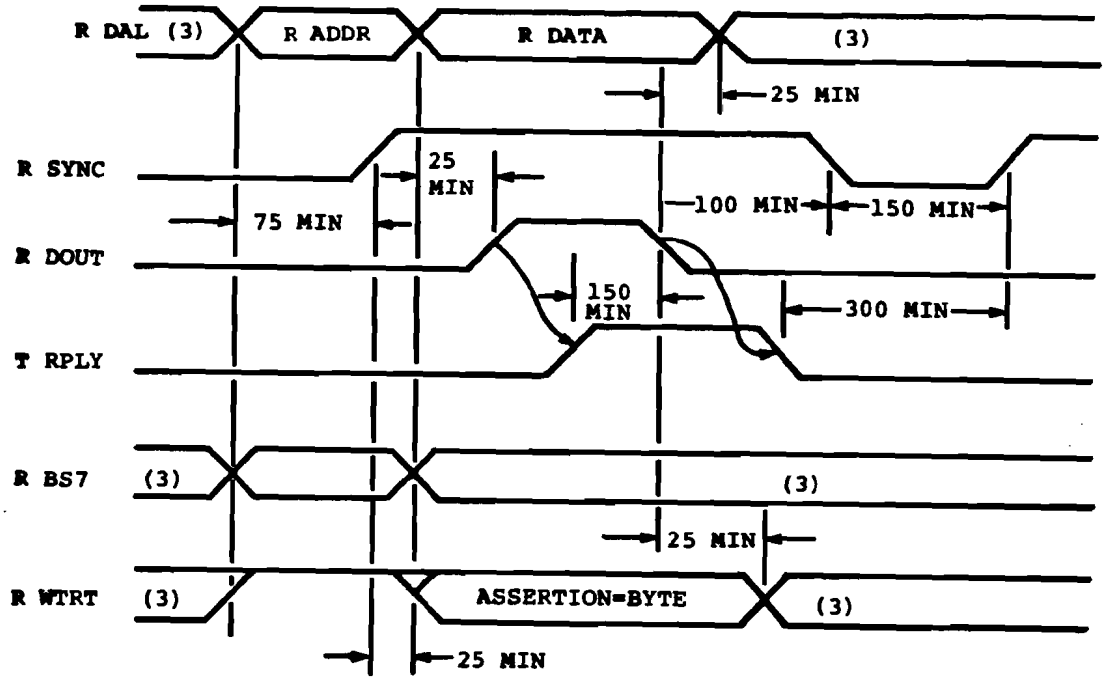

Figure 2-2. DATO, DATOB Bus Cycle Timing

Notes: 1) Timing shown at Bus Driver Inputs and Bus Receiver Outputs.
2) Signal name prefixes are defined below:
T. Bus Driver Input
R. Bus Receiver Output
3) Don't care condition

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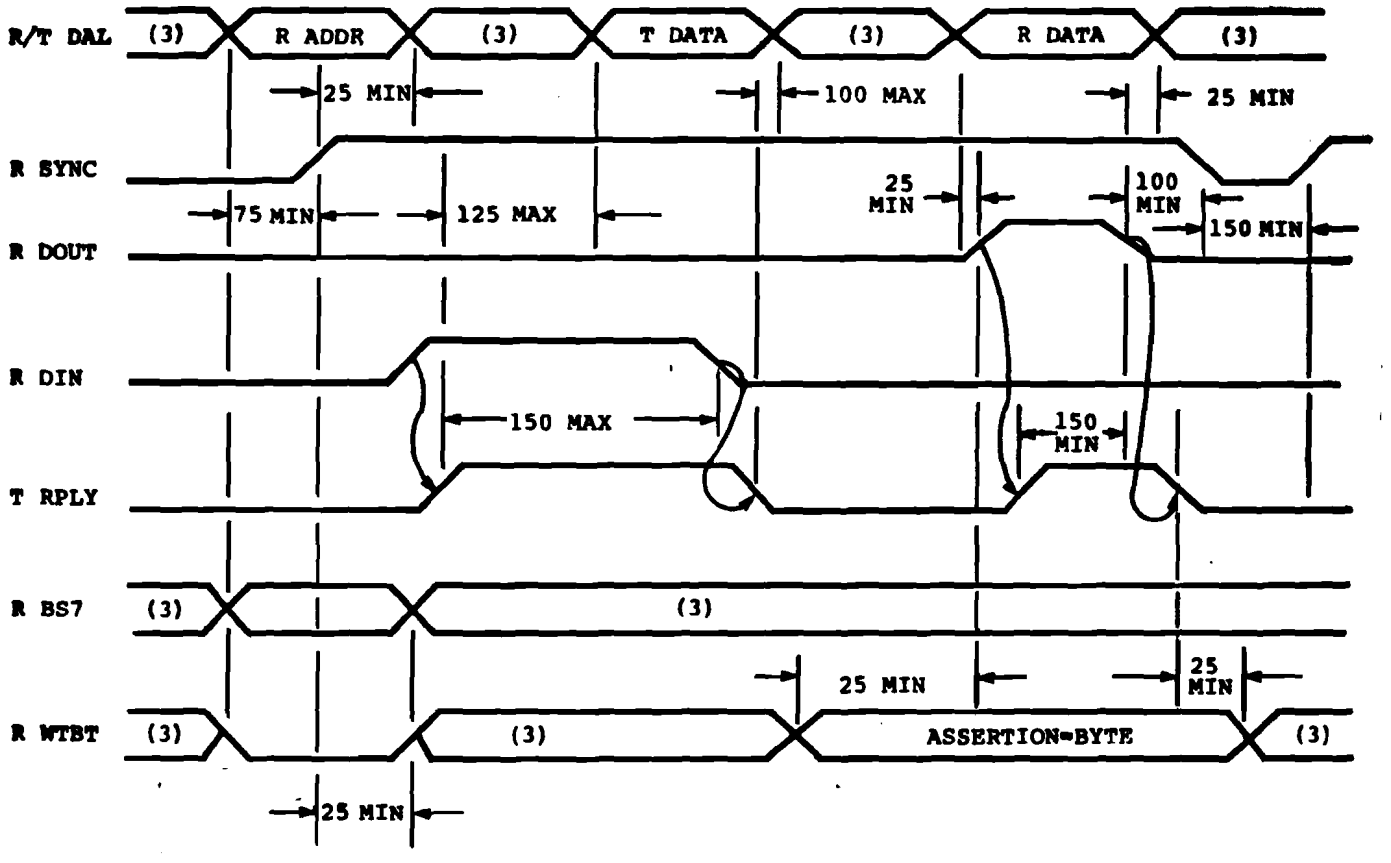
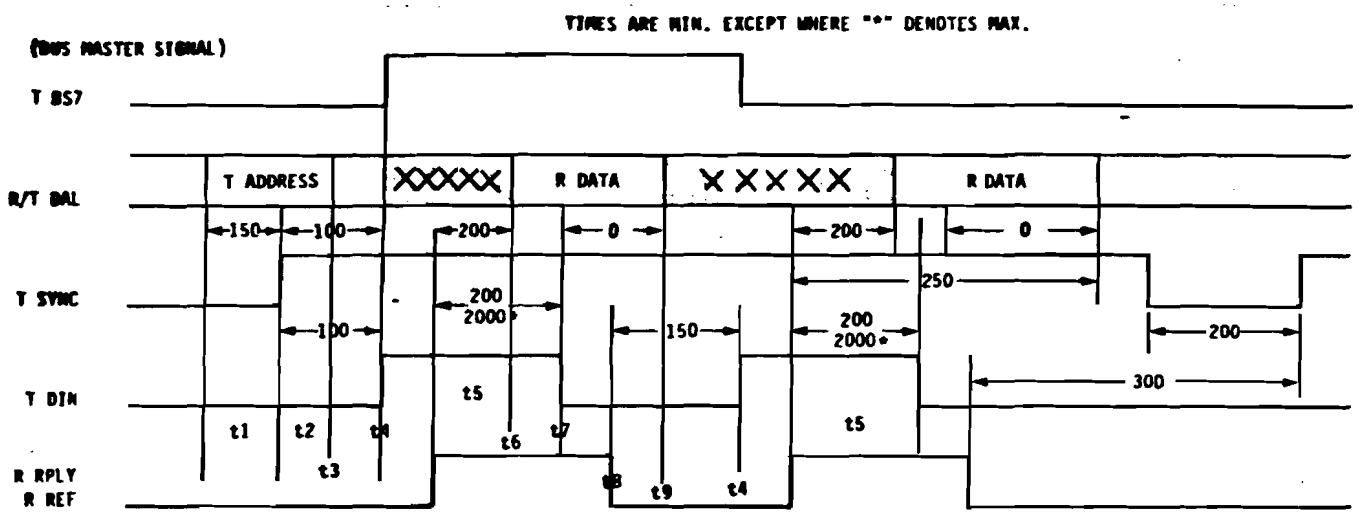


Notes:
1) Timing shown at Bus Driver Inputs and Bus Receiver Outputs
2) Signal name prefixes are defined below:
   T. Bus Driver Input
   R. Bus Receiver Output
3) Don't care condition
4) All timings are given in nanoseconds

Figure 2-3. DATIO, DATIOB Bus Cycle Timing



t1 = Address to T Sync (150ns Min.)

t2 = Address Hold (100ns Min.)

t3 = T Sync to T DIN (100ns Min.)

t4 = T DIN to R RPLY

T (Drive +T (Prop) +T (Receive) +T (Delay)

+T (drive +T (Prop) +T (Receive)

t5 = R RPLY to Data (200ns Max.)

t6 = R RPLY to T DIN (200ns Min.)

t7 = T DIN to R RPLY

T (Drive +T (Prop) +T (Receive) +T (Delay

+T (Drive) +T (Prop) +T (Receive)

t8 = R RPLY to Data (0ns Min.)

t9 = R RPLY to T DIN (150ns Min.)

T Cell = t4+t6+t7+t9 - Since t6 must be >t5 for master to have valid data and t9>t8

Figure 2-4. DATBI Bus Cycle Timing

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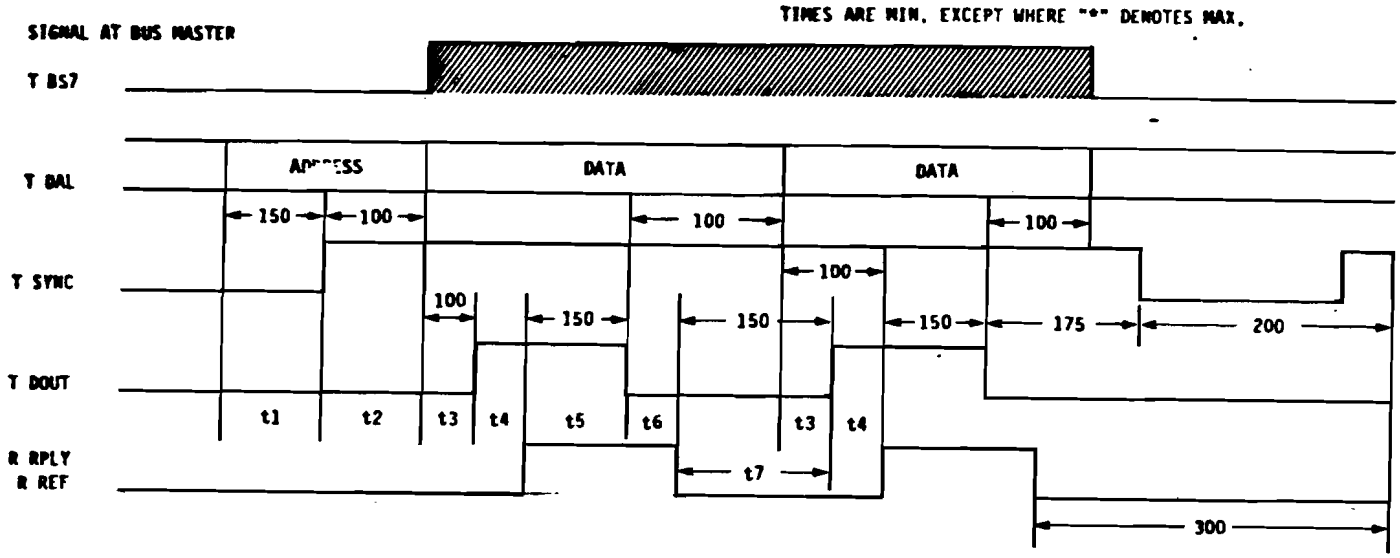

t1 = Address to T Sync (150ns Min.)

t2 = Address Hold (100ns Min.)

t3 = Data to T DOUT (100ns Min.)

t4 = T DIN to R RPLY

T (Drive) +T (Prop) +T (Receive) +T (Delay)

+T (Drive) +T (Prop) +T (Receive)

t5 = R RPLY to T DOUT (150ns Max.)

t6 = T DOUT to R RPLY

= T (Drive) +T (Prop) +T (Receive) +T (Delay)

+T (Drive) +T (Prop) +T (Receive)

t7 = R RPLY to T DOUT (150ns Min.)

T Cell = t3+t4+t5+t6+t7 - Since t3<t7

Figure 2-5. DATBO Bus Cycle Timing

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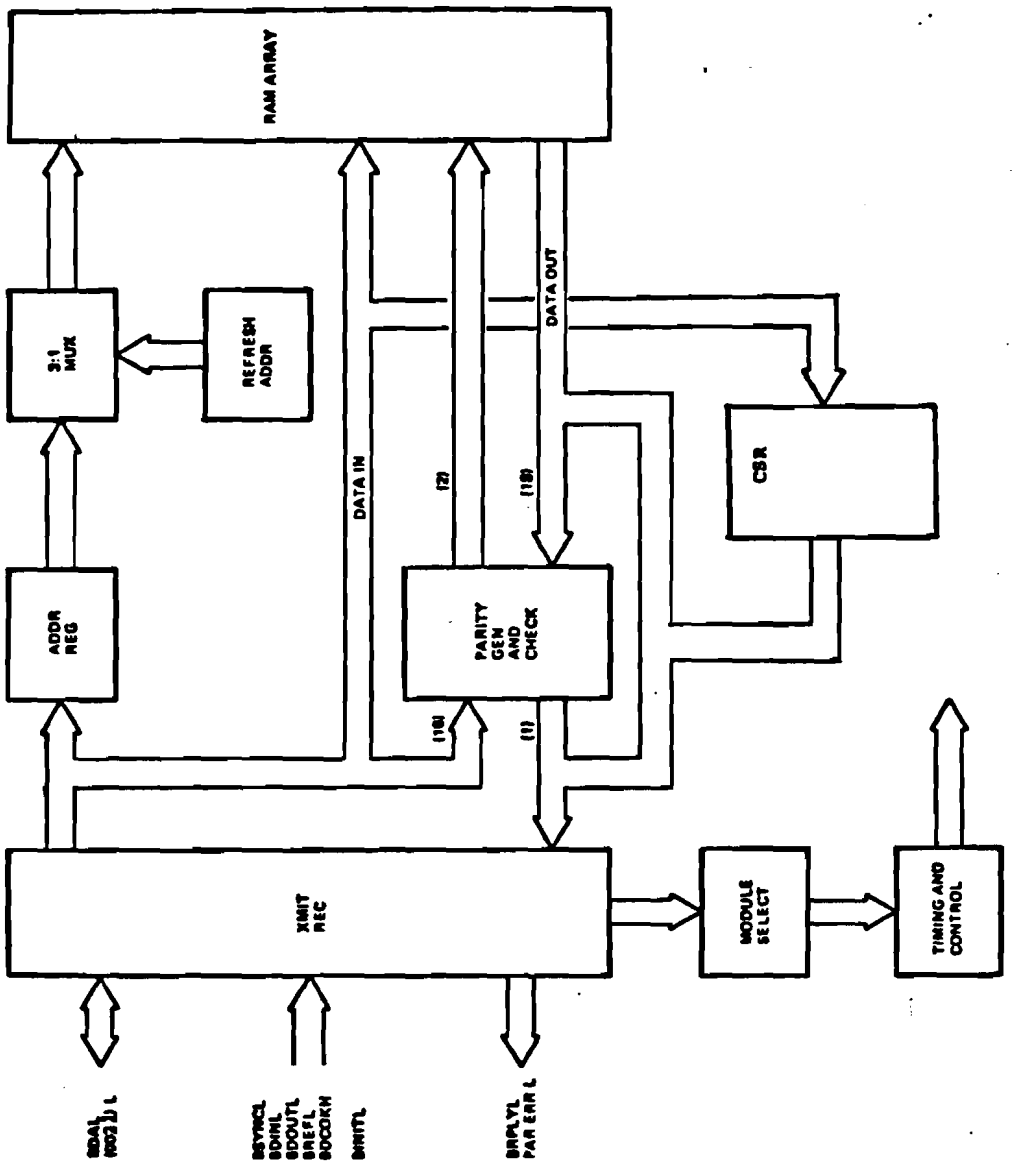

Figure 2-6. NS23S Block Diagram

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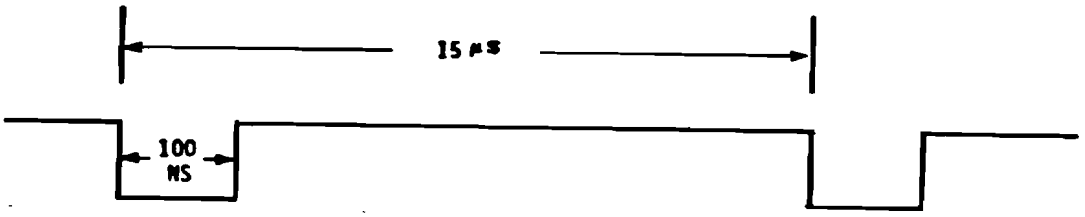

Figure 2-7. External Refresh Timing

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2.5 Memory Card Options

The NS23S memory module contains the following options:

A) On-board Parity Generation and Checking (CSR)
B) Extended Address Space Operation
C) Reserved I/O Space
D) Block Mode Transfers
E) Battery Back-up

2.5.1 Parity Generation and Checking

Provisions have been made on the card for on-board parity generation and checking. A parity bit, plus a parity generator and checker is added per byte. Parity is generated on a byte basis on all write cycles. Parity is checked on all read cycles on a byte basis.

Indication of a parity error on either byte is provided by a parity error signal gated onto the BDAL16 L and BDAL17 L bus lines, which is read by the processor during the memory read cycle.

The parity circuitry can be functionally checked by setting CSR bit 2 which causes incorrect parity during a DATO cycle and checking the resulting parity error signal during a subsequent DATI cycle at the same address.

- NOTE -
A red led on the NS23S indicates detection of a parity error.

2.5.2 Extended Address Space

The NS23S has the capability to operate with 18 to 22-bit addressing. Refer to Table 3-5 for jumper selection. Figure 3-1 is an assembly drawing of the NS23S that shows jumper locations.

2.5.3 Reserved I/O Space

On-board I/O page selection can be configured for 1KW, 2KW or 4KW. Table 3-6 shows the jumper configuration. Bus Bank Select Seven (BBS7) deselects memory during I/O operations and determines if CSR address selection occurs.

2.5.4 Block Mode Transfers

The NS23S has the ability to perform a maximum of 16 data transfers for a single address translation. The necessary block mode control circuitry is contained on the memory card. Block mode operation can only be performed on full (16-bit) words.

- Note -

The Block Mode Feature cannot be utilized on the LSI-11 and the LSI-11/2 systems.

2.5.5 Battery Back-up

The NS23S can be utilized in LSI-11 systems where battery back-up for the semiconductor memory has been implemented by the user. The +5V battery back-up voltage pins provided on the card are compatible with those that DEC provides on the MSV11-L MOS memory.

2.6 Control and Status Register

The Control and Status Register (CSR) in the NS23S allows program control of parity functions and contains diagnostic information if a parity error has occurred. The CSR is assigned an address and can be accessed by a bus master via the LSI-11 bus. The CSR bit assignments are illustrated in Figure 2-8 and are described as follows:

Bits 1,3,4,12,13 Not Used

These bits are not used and are always read as logical 0's. Writing into these bits has no effect on the CSR.

Bit 0 Parity Error Enable

If a parity error occurs during a DATI, DATBI, DATIO(B) cycle, and bit 0 is set to a1, then BDAL 16 and BDAL 17 will be asserted on the bus simultaneously with data. This is a read/write bit reset to zero by INIT L.

Bit 2 Write Wrong Parity

If this bit is set to 1 and a DATO, DATBO, DATIO, DATIOB or DATOB cycle to memory occurs, wrong parity data will be written into the parity RAMs. This bit may be used to check the parity error logic as well as failed address information in the CSR. Bit 2 is a read/write bit reset to zero by INIT L.

Bits 05-11 Error Address

If a parity error occurs on a DATI, DATBI or DATIO(B) cycle, then A11-A17 are stored in CSR bits 5-11 and bits A18-A21 are latched. CSR bit 14 = 0 allows the logic to

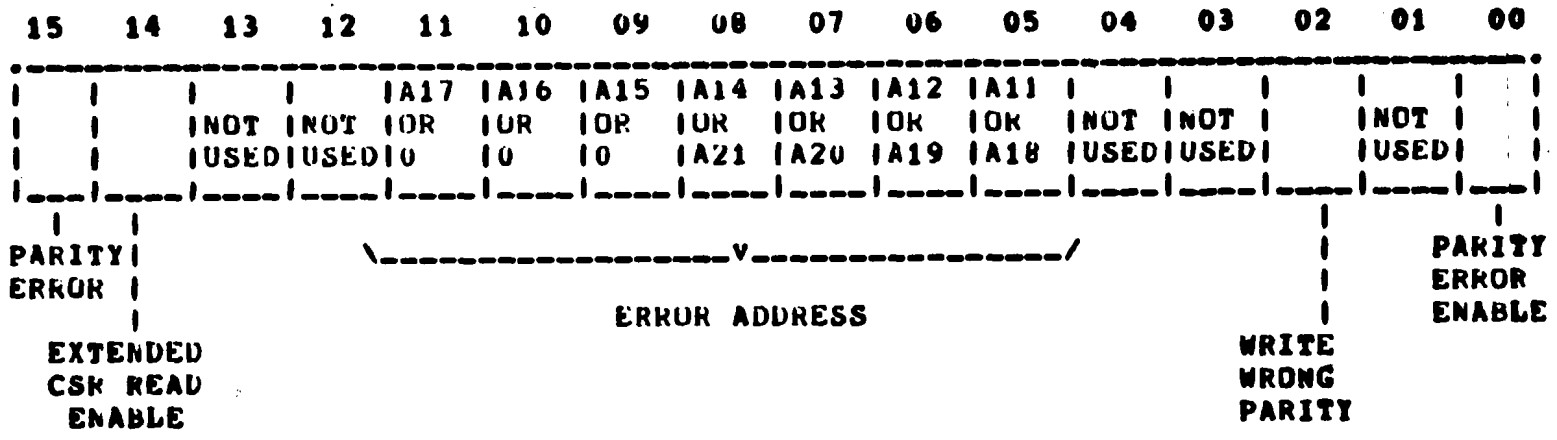

Figure 2-8. CSR Bit Assignments

pass A11-A17 to the LSI-11 bus. CSR bit 14 = 1 places A18-A21 in CSR bits 5-8.

The parity error address locates the parity error to a 1K segment of memory. These are read/write bits and are not reset by INIT L. If a second parity error is encountered, the new failed address will be stored in the CSR.

Bit 14 Extended CSR Read Enable

When bit 14 is set to a 0, either the read/write register (if no parity errors have been detected) or the contents of the primary error address register (containing A11-A17) can be read on CSR bits 05-11. When bit 14 is set to a 1, the contents of the back-up address register will be read on CSR bits 05-11.

Bit 15 Parity Error Indication

If a parity error occurs on a DATI or DATIO(B) cycle, this bit will be set to a 1. This is a read/write bit and is reset to 0 by BUS INIT.

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Chapter III
Installation

3.0 General

This chapter contains the basic information necessary for installing the NS23S Memory Card. The NS23S can be installed into and is electrically compatible with a wide range of backplanes including the H9270, H9273-A, H9275, H9276, Micro/PDP-11 and DDV11-B.

3.1 Tools Required

No special tools are required for installation of the NS23S. However, a pair of needle nose pliers will aid in installing or removing the slip-on configuration jumpers.

3.2 Unpacking and Inspection

Carefully unpack the memory module and visually examine for damage, i.e., dented, bent or broken parts.

- CAUTION -

Do not attempt to install or operate memory if any physical damage is apparent. Contact National Semiconductor for further information.

3.3 System Verification

Prior to installing the NS23S, all applicable system diagnostics should be run to verify system integrity. If a problem is detected it should be corrected before proceeding with the installation of the memory card.

3.4 Starting Address Selection

The starting address of the NS23S can be set to any 4KW boundary within either the LSI-11 128KW or 2048KW address range. Refer to Table 3-1 for starting addresses in the 128KW range. For starting addresses in the 2048KW address range, Table 3-2 must also be used. When selecting a starting address in the 2048KW range, extended addressing must be present in the host CPU, extended addressing must be selected on the NS23S, and the sum of the starting addresses listed in Tables 3-1 and 3-2 must equal the desired starting addresses. Figure 3-1 is an assembly drawing of the NS23S and depicts jumper locations.

3.5 Memory Size Selection

The memory size of the NS23S may be set from a minimum of 8KW to a maximum of 512KW in 8KW increments. Refer to Tables 3-4A and 3-4B for jumper assignments. The memory size will be the sum of the values in Tables 3-4A and 3-4B.

3.6 CSR Address Selection

The NS23S has a resident control and status register (CSR) which contains error information after occurrence of a parity error. The CSR can be assigned to one of eight addresses as dictated by the jumper settings of Table 3-3. Table 3-6 indicates the jumpers involved in enabling or disabling the CSR.

3.7 I/O Page Size Selection

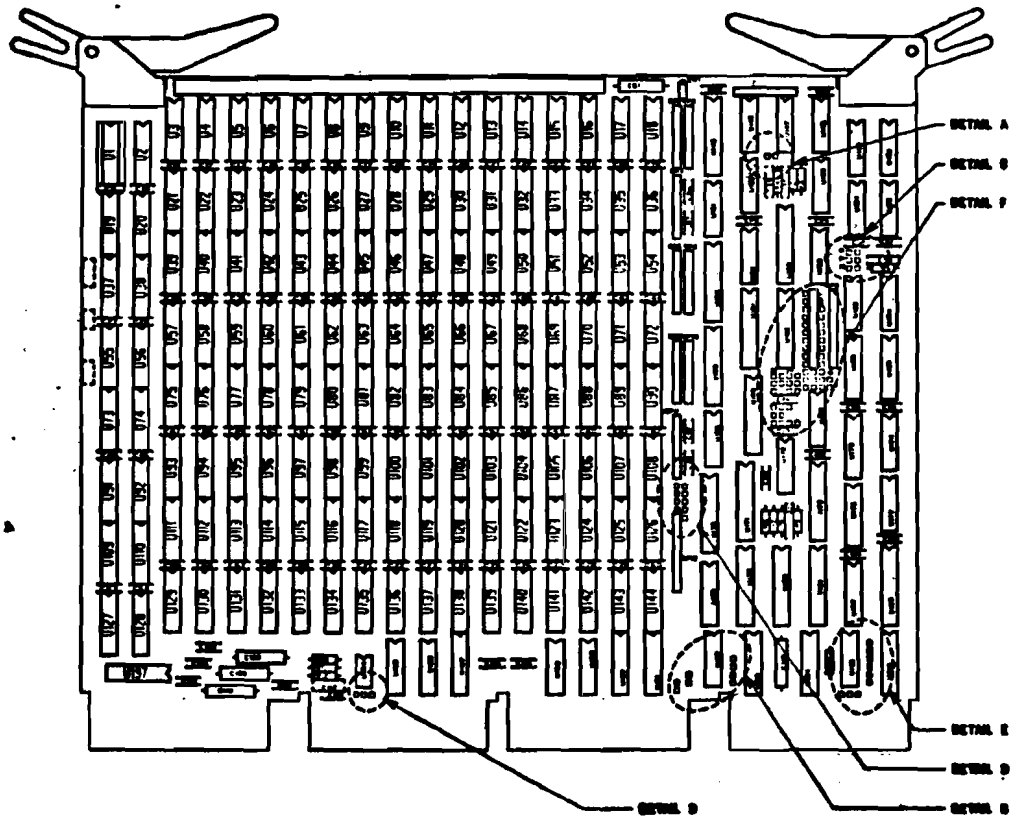
The I/O page of the NS23S is jumper selectable to 1KW, 2KW or 4KW. Table 3-6 shows the jumper settings for the I/O page.

3.8 Parity Detection

The parity detection circuitry of the NS23S can be disabled, which will inhibit parity enable (BDAL 17) from being driven active when a parity error is detected. This function is independent of the CSR parity functions and will override the CSR. Refer to Table 3-6 for jumper selection.

3.9 Internal/External Refresh

Either internal or external refresh may be selected on the NS23S. In standard LSI-11 systems, internal refresh should be selected. Refer to Table 3-6 for jumper placement.



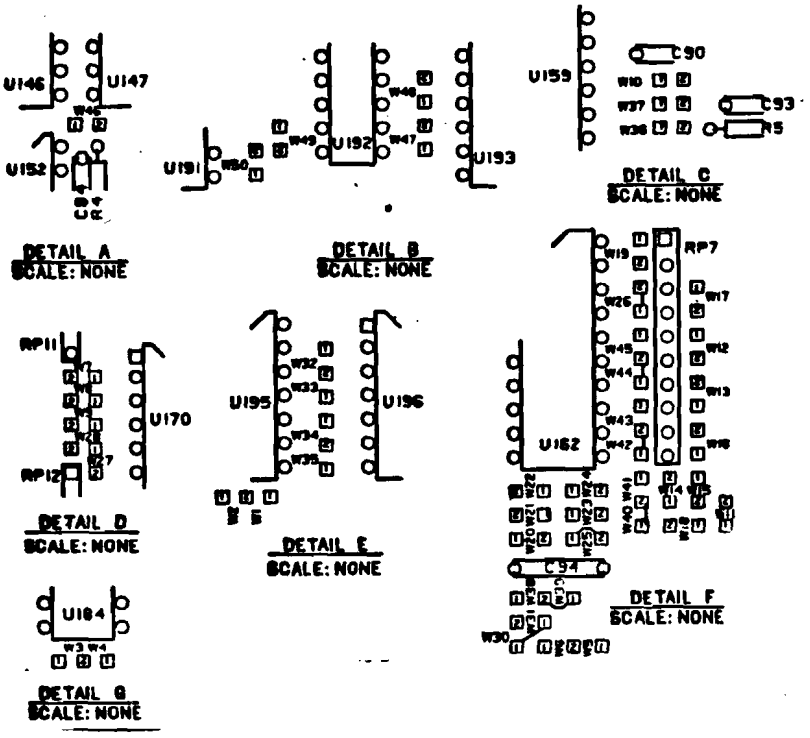


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Figure 3-1. NS23S Assembly Drawing/Jumper Locations

Table 3-1. Starting Address Selection

Starting Address*	Jumpers** W10	W11	W12	W13	W14
0K	0	0	0	0	0
4K	I	0	0	0	0
8K	0	I	0	0	0
12K	I	I	0	0	0
16K	0	0	I	0	0
20K	I	0	I	0	0
24K	0	I	I	0	0
28K	I	I	I	0	0
32K	0	0	0	I	0
36K	I	0	0	I	0
40K	0	I	0	I	0
44K	I	I	0	I	0
48K	0	0	I	I	0
52K	I	0	I	I	0
56K	0	I	I	I	0
60K	I	I	I	I	0
64K	0	0	0	0	I
68K	I	0	0	0	I
72K	0	I	0	0	I
76K	I	I	0	0	I
80K	0	0	I	0	I
84K	I	0	I	0	I
88K	0	I	I	0	I
92K	I	I	I	0	I
96K	0	0	0	I	I
100K	I	0	0	I	I
104K	0	I	0	I	I
108K	I	I	0	I	I
112K	0	0	I	I	I
116K	I	0	I	I	I
120K	0	I	I	I	I
124K	I	I	I	I	I

* 4KW Increments Within A 128K Segment
** 0 = Remove; I = Install

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Table 3-2. Address Range Selection

Address Range	Jumpers*** W15	W16	W17	W18
0K-128K	0	0	0	0
128K-256K	I	0	0	0
256K-384K	0	I	0	0
384K-512K	I	I	0	0
512K-640K	0	0	I	0
640K-768K	I	0	I	0
768K-896K	0	I	I	0
896K-1024K	I	I	I	0
1024K-1152K	0	0	0	I
1152K-1280K	I	0	0	I
1280K-1408K	0	I	0	I
1408K-1536K	I	I	0	I
1536K-1664K	0	0	I	I
1664K-1792K	I	0	I	I
1792K-1920K	0	I	I	I
1920K-2048K	I	I	I	I

*** I = Install; 0 = Remove

Table 3-3. CSR Address Selection

22-Bit CSR Address	18-Bit CSR Address	Jumpers* W9	W8	W7
17772100	772100	I	I	I
17772102	772102	0	I	I
17772104	772104	I	0	I
17772106	772106	0	0	I
17772110	772110	I	I	0
17772112	772112	0	I	0
17772114	772114	I	0	0
17772116	772116	0	0	0

* I = Install; 0 = Remove

Table 3-4A. Memory Size

Memory Size	Jumpers* W22	W21	W20	W19
8KW	I	I	I	I
16KW	I	I	I	0
24KW	I	I	0	I
32KW	I	I	0	0
40KW	I	0	I	I
48KW	I	0	I	0
56KW	I	0	0	I
64KW	I	0	0	0
72KW	0	I	I	I
80KW	0	I	I	0
88KW	0	I	0	I
96KW	0	I	0	0
104KW	0	0	I	I
112KW	0	0	I	0
120KW	0	0	0	I
128KW	0	0	0	0

* I = Install; 0 = Remove

Table 3-4B. Memory Size

Memory Size	Jumpers* W26**	W25**	W24	W23
0KW	I	I	I	I
128KW	I	I	I	0
256KW	I	I	0	I
384KW	I	I	0	0

* I = Install; 0 = Remove
** W25-26 are factory set and should not be altered

Table 3-5. Extended Address Selection

Address Type	Jumpers* W47	W48	W49	W50
18-BIT	0	0	0	0
19-BIT	I	0	0	0
20-BIT	I	I	0	0
21-BIT	I	I	0	I
22-BIT	I	I	I	I

* 0 = Remove
I = Install

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Table 3-6. Jumper Configuration

Jumper	Purpose	Configuration
W1	Battery Back-up	I = Non battery back-up R = Battery back-up
W2	Battery Back-up	I = Battery back-up R = Non battery back-up
W3	Refresh	I = Internal refresh R = External refresh
W4	Refresh	I = External refresh R = Internal refresh
W5	Refresh	I = BREF L inhibit select R = BREF L not inhibit select
W6	Refresh	I = BREF L not inhibit select R = BREF L inhibit select
W7-W9	CSR Address	See Table 3-3
W10-W18	Start Addr Select	See Table 3-1 and 3-2
W19-W24	Memory Size Select	See Table 3-4A and 3-4B
W25-W26	Factory Installed - Do Not Alter	
W27	CSR Enable	I = CSR enabled R = CSR disabled
W28	CSR Disable	I = CSR disable R = CSR enable
W29	Not Used	
W30	Block Mode Disable	I = Block Mode Disabled R = Block Mode Enabled
W31	Block Mode Enable	I = Block Mode Enabled R = Block Mode Disabled
W32	Factory Test Only	Remove
W33	Factory Test Only	Install
W34	Factory Test Only	Remove
W35	Parity	I = Parity Enable disabled R = Parity Enable enabled
W36	I/O Page	I = 2KW or 1KW I/O page R = 4KW I/O page
W37	I/O Page	I = 1KW I/O page R = 4KW or 2KW I/O page
W38-W45	Factory Configuration - Do Not Alter	
W46	Not Used	
W47-W50	Extended Address	See Table 3-5

3.10 Battery Back-up

Battery back-up may be installed on the NS23S in systems where a battery back-up option has been implemented by the user. Refer to Table 3-6 for jumper settings.

3.11 Block Mode

Block Mode operation can be enabled for those systems capable of utilizing this feature. Refer to Table 3-6 for jumper configuration.

NOTE
Block Mode operation must be DISABLED (W30 Installed/W31 Removed) for LSI-11 and LSI-11/2 Systems.

3.12 Installing the NS23S

Since the NS23S can be installed in a wide variety of LSI-11 backplanes, the configuration rules for adding options to the system must be followed. The memory module must be inserted into the backplane with the components facing in the same direction as the other modules in the LSI-11 system. The NS23S, backplane, or both can be damaged if the module is installed backwards. When the memory module is installed, diagnostics can be run to verify operation. If in doubt about which slot the NS23S is to be inserted into, contact National Semiconductor Technical Support for assistance.

CHAPTER IV
Diagnostics and Troubleshooting

4.0 General

This section describes the use of four DEC diagnostics - ZKMA, ZQMC, ZMSD and VMSA - that can be used to troubleshoot and isolate a failure on the NS23S memory module. Once the failure has been isolated, the defective RAM can easily be replaced by lifting it from the socket and replacing it with the on-board spare.

4.1 ZKMA

This diagnostic will test 0-256KB of memory on any PDP-11 family computer.

Switch Setting Summary

```
BIT 15(100000); SW15 = 1  HALT ON ERROR
BIT 14(040000); SW14 = 1  LOOP ON TEST
BIT 13(020000); SW13 = 1  INHIBIT ERROR PRINTOUTS
BIT 12(010000); SW12 = 1  ENABLE TESTING ABOVE 28K
BIT 11(004000); SW11 = 1  ENABLE PARITY TESTING
BIT 10(002000); SW10 = 1  HALT AFTER EACH TEST
BIT  9(001000); SW9  = 1  INHIBIT PROGRAM RELOCATION
BIT  8(000400); SW8  = 1  TYPE FIRST FAILURE IN 4K BANK
BIT  7(000200); SW7  = 1  LONG GALLOP TEST*
BIT  6(000100); SW6  = 1  INHIBIT MEMORY SIZING
BIT  5(000040); SW5  = 1  INHIBIT END PASS PRINTOUTS
BIT  4(000020); SW4  = 1  INHIBIT PRINTOUTS
BITS 3-0; SW3-0           BEGINNING TEST NUMBER
```

* Caution, the long gallop test will increase test times by a factor of 25!

4.2 Running ZKMA

1. Load program ZKMA?? into memory (L ZKMA?? <CR>).

2. Select options by setting bits into the switch register. Refer to the above switch settings. Note: Normal switch settings would be bits 11 and 12 set (014000).

3. Start program testing (S <CR>).

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4. A pass with no errors detected will appear similar to the following sample print-out:

```
000000-757777
PARITY
TST13 BNK 0
TST13 BNK 1
TST13 BNK 2
TST13 BNK 3
TST13 BNK 4
TST13 BNK 5
TST13 BNK 6
RELOC
TST13 BNK 0
END PASS 1
```

5. The following is an example of a typical error message print-out:

LOCATION	GOOD	BAD	PC	ERROR	PASFLG
177210	177777	177776	1625	10	[TST0]

LOCATION = FAILING MEMORY LOCATION
GOOD = GOOD DATA (DATA THAT WAS EXPECTED)
BAD = BAD DATA (DATA THAT WAS FOUND)
PC = PROGRAM COUNTER AT ERROR CALL
ERROR = FALLING ERROR NUMBER
PASFLG = CONTENTS OF ERROR PASFLG (THIS MAY NOT BE RELEVANT)

Using the above print-out as an example, the failure would be found in the address range 0-128KB (177210 is between 0 and 00377776). The failing bit would be zero; this is determined by comparing good data with bad data (177777-177776 = 000001). Using Figure 4-1, the failing RAM is found to be in the first row of RAMs (U1-U18). Since it is known that bit 0 is bad, the faulty RAM must therefore be U3. The PC, ERROR and PASFLG information are not normally needed to determine the failing RAM and are not needed in this example. If they are needed, refer to the DEC diagnostic listing for ZKMA.

4.3 ZQMC

This program has the ability to test memory from address 000000 to 757777, (0-248KB of memory), on any PDP-11 family processor.

Switch Setting Summary

BIT 15(100000); SW15 = 1 HALT ON ERROR
BIT 14(040000); SW14 = 1 LOOP ON TEST
BIT 13(020000); SW13 = 1 INHIBIT ERROR PRINT-OUTS

```
BIT 12(010000); SW12 = 1  INHIBIT MEMORY MANAGEMENT
BIT 11(004000); SW11 = 1  INHIBIT SUBTEST ITERATION
BIT 10(002000); SW10 = 1  RING BELL ON ERROR
BIT  9(001000); SW 9 = 1  LOOP ON ERROR
BIT  8(000400); SW 8 = 1  LOOP ON TEST IN SWR<4:0>
BIT  7(000200); SW 7 = 1  INHIBIT PROGRAM RELOCATION
BIT  6(000100); SW 6 = 1  INHIBIT PARITY ERROR DETECTION*
BIT  5(000040); SW 5 = 1  INHIBIT EXERCISING VECTOR AREA
BIT  4-0; SW4-0           BEGINNING TEST NUMBER
```

* With parity error detection enabled, a memory failure can cause a parity error. The error print-out on a parity error does not type the good data. Thus, a bit dropped or picked-up will not be typed as such, therefore it is best to run the program for 1 pass with parity disabled then restart the program with parity enabled.

4.4 Running ZQMC

1. Load program ZQMC?? into memory (L ZQMC?? <CR>).

2. Select options by setting bits into the switch register. Refer to the above switch settings. Note: normal switch settings would be bit 6 set for the first pass (000100), and no bits set for the second pass (000000).

3. Start program testing (S <CR>).

4. If there are no errors detected the print-out will appear similar to the following format:

```
KT11 (MEMORY MANAGEMENT) AVAILABLE
MEMORY MAP:
FROM 000000 TO 757777
PARITY MEMORY MAP:
REGISTER AT 172100 CONTROLS
FROM 000000 TO 757777
PROGRAM RELOCATED TO 720000
PROGRAM RELOCATED TO 000000
END PASS #1
```

5. There is a total of 31 types of error reports generated by this program. Some of the key column heading mnemonics are described below for clarity:

   PC = PROGRAM COUNTER OF ERROR DETECTION CODE.
   V/PC = VIRTUAL PROGRAM COUNTER. THIS IS WHERE THE ERROR DETECTION CODE CAN BE FOUND IN THE PROGRAM LISTING.

P/PC = PHYSICAL PROGRAM COUNTER. THIS IS WHERE THE ERROR DETECTION CODE IS ACTUALLY LOCATED IN MEMORY.
TRP/PC = PHYSICAL PROGRAM COUNTER OF THE CODE WHICH CAUSED A TRAP
MA = MEMORY ADDRESS
REG = PARITY REGISTER ADDRESS
PS = PROCESSOR STATUS WORD
IUT = INSTRUCTIONS UNDER TEST
S/B = WHAT CONTENTS SHOULD BE (GOOD DATA)
WAS = WHAT CONTENTS WAS (BAD DATA)

The following is an example of a typical error message print-out:

V/PC	P/PC	MA	S/B	WAS
006300	006300	473732	133732	173732

Using the above print-out as an example, the failure would be found in the address range 128KB-256KB, (473732 is between 00400000 and 00777776). The failing bit would be bit "14"; this is determined by comparing good data with bad data, (S/B with WAS), and doing an EXCLUSIVE OR of the two, (133732-173732) = 040000) and locating the bad octal bit, bit "14". Using Figure 4-1, the failing RAM is found to be in the second row of RAMs, (U19-U36).

Since it is known that bit "14" is bad, the faulty RAM must therefore be U35. For error messages that do not display the failing address and good and bad data, refer to the DEC diagnostic listing for ZQMC or call National Semiconductor Memory Systems Technical Support.

4.5 ZMSD

This diagnostic can test up to 4 megabytes of memory and can be run on any PDP-11 computer system with extended addressing (22-bit) capability, and with at least 64KW of memory. This diagnostic will not run unless the board CSR of the NS23S is enabled (W27 In, W28 Out).

Switch Register Options

BIT 15(100000); SW15 = 1 HALT ON ERROR
BIT 14(040000); SW14 = 1 LOOP ON TEST
BIT 13(020000); SW13 = 1 INHIBIT ERROR PRINT-OUTS
BIT 12(010000); SW12 = 1 INHIBIT RELOCATION
BIT 11(004000); SW11 = 1 QUICK VERIFY
BIT 10(002000); SW10 = 1 RING BELL ON ERROR
BIT 9(001000); SW 9 = 1 LOOP ON ERROR
BIT 8(000400); SW 8 = 1 HALT PROGRAM
BIT 7(000200); SW 7 = 1 DETAILED ERROR REPORT
BIT 6(000100); SW 6 = 1 INHIBIT CONFIGURATION MAP

```
BIT  5(000040); SW 5 = 1  LIMIT MAX ERRORS PER BANK
BIT  4(000020); SW 4 = 1  FAT TERMINAL (132 COLUMNS PRINTER)
BITS 3-0; SW3-0           TEST MODE
```

4.6 Running ZMSD

1. Load program ZMSD?? into memory (L ZMSD?? <CR>).

2. Select options by setting bits into the switch register. Refer to the above switch settings. Note: normal switch setting would be all bits off (000000).

3. Start program testing (S <CR>).

4. The program will start running, size memory, and print out a configuration map. Note: The diagnostic does not fully exercise the memory board whose CSR controls the memory containing the diagnostic.

- NOTE -

Earlier versions of ZMSD may note that the NS23S resident CSR "controls too many banks", but this statement has no bearing on the functionality of the diagnostic.

5. In the following example, the configuration map print-out is for a system with one NS23S memory board installed as the only memory board in the system, (the board is set for 1 megabyte of memory):

```
                  1       2       3       4       5       6       7
          01234567012345670123456701234567012345670123456701234567012345670123
ERRORS
CPU MAP   11111111111111111111111111111111
INTRLV    --------------------------------
MEMTYPE   LLLLLLLLLLLLLLLLLLLLLLLLLLLLLLLL
CSR       00000000000000000000000000000000
PROTECT   PP
```

Memory Configuration Map Explanations

BANKS = EACH BANK EQUALS 16KW OF MEMORY. EIGHT BANKS WOULD EQUAL 128KW OF MEMORY AND BE READ AS 10 OCTAL BANKS.

ERRORS = IF THE MEMORY SIZING ROUTINE COULD NOT WRITE 1'S AND 0'S IN A BANK, AN "X" WOULD BE TYPED FOLLOWING THIS HEADING UNDER THE FAILING 16K BANK.

CPU MAP = THE CPU WAS ABLE TO ACCESS THESE BANKS.

INTRLV = IF INTERLEAVED, THE CSR CONTROLLING ADDRESS BIT 1 IS TYPED.

MEMTYPE = MEMORY TYPE, L = MSV11-L; P = MSV11-P

CSR = WHICH CSR CONTROLS THAT BANK OF MEMORY.
PROTECT = PROGRAM PROTECTED SPACE, WHERE THE DIAGNOSTIC RESIDES, (INDICATED BY A "P"). NO ERRORS ARE REPORTED IN THESE BANKS.

6. A good pass will print out "END PASS 1" (for first pass).

Error information; the following is an example of a typical memory data error, error header definitions, and troubleshooting steps.

SAMPLE ERROR MESSAGE

PC	BANK	VADD	PADD	GOOD	BAD	XOR	CSR	MTYP	INT	PAT
022134	7	060060	00700060	000000	010000	010000	0	L	-	06
022134	7	060060	00700060	000000	010000	010000	0	L	-	06
022134	7	060060	00700060	000000	010000	010000	0	L	-	06
022134	7	060060	00700060	000000	010000	010000	0	L	-	06

Error Header Definitions

PC = PROGRAM COUNTER
BANK = BANK OF MEMORY UNDER TEST
VADD = VIRTUAL ADDRESS
PADD = PHYSICAL ADDRESS
GOOD = DATA EXPECTED
BAD = DATA RECEIVED
XOR = THE X-ORED VALUE OF THE GOOD AND BAD DATA
CSR = CONTROL AND STATUS REGISTER
INT = INTERLEAVED
PAT = DATA PATTERN USED

Listed below are the necessary steps used to trouble-shoot and isolate the failing RAM (refer to above example of configuration map print-out and sample error message):

1. Determine the bank in memory where the error occurred (BANK 7).

2. Locate the PADD (Physical Address) and record its contents (00700060).

3. Determine the failing bit(s) by comparing the good data with the bad data and doing an EXCLUSIVE OR (Xor) of the two, or examining the XOR value (010000) and locating the bad octal bit. This indicates that the failing bit is bit "12". In this example, knowing the physical address (PADD) 00700060 and the Xor value 010000 (Data Bit 12), Table 4.1 will indicate the failing RAM. U33 is the RAM in question.

4.7 VMSA

This program is an LSI-11 based memory diagnostic with the ability to exercise up to 4MB of memory, and can be run with or without a CSR register in the system. A minimum of 16KW of memory is needed.

Switch Register Options

```
BIT 15(100000); SW15 = 1  HALT ON ERROR
BIT 14(040000); SW14 = 1  LOOP ON TEST
BIT 13(020000); SW13 = 1  INHIBIT ERROR TYPEOUT
BIT 12(010000); SW12 = 1  INHIBIT MEMORY MANAGEMENT
BIT 11                    <NOT USED>
BIT 10(002000); SW10 = 1  RING BELL ON ERROR
BIT  9(001000); SW 9 = 1  LOOP ON ERROR
BIT  8(000400); SW 8 = 1  LOOP ON TEST IN SWR <4:0>
BIT  7(000200); SW 7 = 1  INHIBIT PROGRAM RELOCATION
BIT  6(000100); SW 6 = 1  INHIBIT PARITY ERROR DETECTION
BIT  5(000040); SW 5 = 1  INHIBIT EXERCISING VECTOR AREA
BITS 4-0                  <NOT USED>
```

4.8 Running VMSA

1. Start execution of VMSA by typing (R VMSA?? <CR>).

2. The program will identify itself, give the present contents of the switch register, and ask for the new contents of the switch register. The normal setting of the register is all bits off (000000). If the user types <CR> at this point, no bits in the switch register will be changed. To change a bit setting, the octal pattern corresponding to the bit or bits to be set is entered followed by <CR>.

3. The following example illustrates a printout of VMSA for a system with one NS23S memory board installed as the only memory in the system (the card is set for 1 megabyte of memory):

```
CVMSAA

SWR = 000000    New = 000000

KT11 (Memory Management) Available
Memory Map:
From 00000000 To 03777776

Parity Memory Map:
Parity Register at 17772100 Controls
From 00000000 To 03777776
```

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```
Program Relocated to 00700000
Program Relocated to 00000000

End Pass #1
```

4. A good pass will print out "END PASS # " after each pass.

Error Information

If an error is detected during the execution of VMSA, an error print-out similar to the following example will occur:

SAMPLE ERROR MESSAGE

```
Random Data Error (TST 14)
 V/PC         P/PC          MA          S/B         WAS
011160      00011160      00400120      000742      000342
```

Error Header Definitions

V/PC = VIRTUAL PROGRAM COUNTER ADDRESS
P/PC = PHYSICAL PROGRAM COUNTER ADDRESS
MA = ACTUAL MEMORY ADDRESS WHERE ERROR OCCURRED
S/B = GOOD DATA
WAS = BAD DATA

The steps necessary to troubleshoot and isolate the failing RAM using the above error message printout are as follows:

1. Using the 'should be' (S/B) and 'was' information, determine the bit that was in error.

2. After determining the failing bit, note the 'memory address' (MA) where the error occurred.

3. In this example, the failing bit is found to be bit 8 and the memory address is 400120. By using this information in conjunction with Table 4-1, address 400120 falls into the range covered by row 1 of the NS23S. The RAM associated with bit 8 in row 1 is U29. The faulty RAM can now be replaced with the on-board spare and the diagnostic should be rerun to verify that no other errors exist. If problems still exist after RAM replacement, or if other errors occur which cannot be isolated, contact National Semiconductor Technical Support.

4.9 11/23-Plus Diagnostic/Bootstrap

If the NS23S is installed in an 11/23-Plus system, a diagnostic/bootstrap function will be performed for power up or init sequences. This

ROW 0	U1	U2	U3	U4	U5	U6	U7	U8	U9	U10	U11	U12	U13	U14	U15	U16	U17	U18
ROW 1	U19	U20	U21	U22	U23	U24	U25	U26	U27	U28	U29	U30	U31	U32	U33	U34	U35	U36
ROW 2	U37	U38	U39	U40	U41	U42	U43	U44	U45	U46	U47	U48	U49	U50	U51	U52	U53	U54
ROW 3	U55	U56	U57	U58	U59	U60	U61	U62	U63	U64	U65	U66	U67	U68	U69	U70	U71	U72
ROW 4	U73	U74	U75	U76	U77	U78	U79	U80	U81	U82	U83	U84	U85	U86	U87	U88	U89	U90
ROW 5	U91	U92	U93	U94	U95	U96	U97	U98	U99	U100	U101	U102	U103	U104	U105	U106	U107	U108
ROW 6	U109	U110	U111	U112	U113	U114	U115	U116	U117	U118	U119	U120	U121	U122	U123	U124	U125	U126
ROW 7	U127	U128	U129	U130	U131	U132	U133	U134	U135	U136	U137	U138	U139	U140	U141	U142	U143	U144
DATA/ PARITY BIT	P1	P0	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15

ROW 0 = 0 - 64KW (0-00377776)
ROW 1 = 64KW - 128KW (00400000-00777776)
ROW 2 = 128KW - 192KW (01000000-01377776)
ROW 3 = 192KW - 256KW (01400000-01777776)
ROW 4 = 256KW - 320KW (02000000-02377776)
ROW 5 = 320KW - 384KW (02400000-02777776)
ROW 6 = 384KW - 448KW (03000000-03377776)
ROW 7 = 448KW - 512KW (03400000-03777776)

Table 4-1. NS23S RAM Locator Chart

diagnostic/bootstrap will test memory and, if no errors occur, will identify the amount of memory in the system. Table 4-2 shows the error messages and other descriptive information related to this microdiagnostic.

Address of Error	Display (octal)	Cause of Error and Comment
173232	02	Memory Error 2. Write address to itself.
173262	02	Memory Error 3. Byte addressing error.
173302	02	Memory error in pre-memory test. R2 = failing data R3 = expected data R5 = failing address
173316	02	Memory error Bit 15 set in one of the parity CSR's (172100-172136). Failing memory should have the parity LED on.
173660	02	Memory error in 0-2044KW. 22 bit memory test. Common error halt for six different tests. If R3 = 0, then error in Test 1-5. Then R4 determines failing test. R4 = expected data R5 = failing data

Table 4-2. 11/23-Plus Error Messages

Contents of R4	Test #	Test Description
20000-27776	1	Address Test, Bit 11-0
177777	2	Data Test
000000	3	Data Test
072524	4	Odd Parity Pattern Test
125125	5	Byte Addressing Test

For Test 1-5 (R3=0) determine 22 bit failing address as follows:

R1 bits 11-0 failing address Bits 11-0
R2 bits 15-6 failing address Bits 22-12

Errors in address uniqueness test. Test checks address Bits 21-6 Test #6. If R3 is not equal to 0 then error is in this test.

R4 = expected data
R5 = failing data
R2 = 22 bit failing address Bits 21-6 failing address.
Bits 5-0 are always 0

Address of Error	Display (octal)	Cause of Error and Comment
173664	02	Memory error in pre-memory address test for locations 0-776. R2 = failing data R5 = failing address and expected data
173736	02	Memory error 1, Data test failed. Test 0-30 with MMU off if present R1 = failing address R4 = expected data (either 000000 or 177777) R5 = failing data

Table 4-2 (continued). 11/23-Plus Error Messages