MEMORY APPLICATIONS HANDBOOK

NATIONAL SEMICONDUCTOR

MEMORY APPLICATIONS HANDBOOK

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Table of Contents

DESIGN AID

APPLICATION NOTE

BACKGROUND INFORMATION

TECHNICAL DESCRIPTION

Table of Contents

DESIGN AID

APPLICATION NOTE

BACKGROUND INFORMATION

TECHNICAL DESCRIPTION

Page Index of Devices Discussed

Page Index of Devices Discussed

Section 1

Introduction

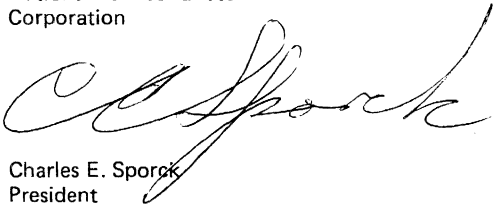
President's Message

Dear Customer:

The exciting future of memory applications is limited only by our collective abilities to make use of the continuing stream of rapid technological advances. Annual consumption of semiconductor memory components has already surpassed a half billion dollars per year and will cross the one billion dollar level within the next three years. Years ago National established the reputation as a high volume supplier of high quality, cost-effective components for the complete range of discretes, linears, optoelectronics, transducers, A/D and D/A, hybrids and large scale integrated memory, microprocessor, and logic arrays. We are pleased to continue our expansion of this broad product line to include the memories you will require in the future. Our world-wide network of factory representatives, local stocking distributors, and field applications engineers is at your service to help meet your needs – just give any of them a call.

We appreciate your interest in National's products and services, and look forward to supplying your present and future requirements.

National Semiconductor
Corporation



Charles E. Sporck
President

Preface

The application of today's memory components can present either another day-to-day engineering problem or an immense task involving a full team of design and components specialists. This does not mean that designing an add-on memory for a large mainframe computer is more difficult than producing a memory system based on a two-chip microprocessor (it most likely is not). The difference in complexity may well depend on how your organization is structured. In some organizations the memory designer concerns himself strictly with memory proper. In other organizations, a given engineer may be directly involved in designing the entire system, from the screws that hold the enclosure together to the choice of memory components. But whether your interest in this book is solely to obtain the MM5290 bit map or because you want help with your first dynamic RAM design, we hope the end result will be the same: optimization of your design engineering effort.

It would be impossible to make a memory applications handbook comprehensive. However, we have tried to make the scope of this book broad with respect to application as well as product type (made possible by the broad range of product National produces). In order to relate to the real-life problems of the design engineer, we have attempted to present actual systems as examples. To do this we have enlisted the aid of National's systems' divisions and their personnel. *To provide full credit to these contributors, we have included their names with the applications; but we ask that, should questions arise, you do not initially contact these perple directly.* We ask instead that you contact your local National sales representative or this Memory Applications group.

If you find any errors or omissions or have other contributions to make, please contact us. We welcome your suggestions and will try to include them in future editions.

We would like to express our appreciation to the authors of the applications and support material whose names are listed at the head of their work. We also express our appreciation to the people listed below who helped in data gathering and preparation.

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Memory Component Applications
National Semiconductor Corporation
Santa Clara, California

Future Memory Technology Development

National Semiconductor
Thomas Klein*
January 1978

ABSTRACT: Semiconductor integrated circuit based memory devices became the dominant Random Access Memory technology in less than 8 years. They were able to achieve this because their batch manufacturing process allowed a very rapid reduction of cost per bit of storage through technological changes to increase batch density. Continued progress in density improvement at essentially unchanged rates is still feasible. It will, however, require major changes in manufacturing, device and material technology.

Since the beginning of the 70's, semiconductor integrated circuits used as digital storage elements have become a very significant factor in the total spectrum of information storage technology. They became the dominant technology for random access memories and are beginning to make inroads into the slower serial access memory market, presently dominated by magnetic discs and drums.

The ability of integrated circuit technology to continue to offer digital data storage at very rapidly decreasing cost per bit of storage is a consequence of the batch manufacturing process. It allows introductions of new products which are cost effective even at very low manufacturing efficiency level, obtain very steep cost reduction during product life by rapid increase of manufacturing efficiency and continue to stay on the steep cost reduction curve by going to a higher level of integration when cost improvements through improved manufacturing efficiencies are starting to flatten out.

However, to go to a higher level of integration, which in case of Random Access Memory circuits, usually means a four-fold increase in number of bits on the chip, a significant improvement in batch density is required, otherwise no benefit is derived *(Figure 1)*.

This batch density (i.e., number of potentially good storage elements processed together as a single unit (i.e., a silicon wafer) has shown an even higher rate of growth than the much more visible increase in the number storage bits/memory circuit.

During the past eight years the number of potentially good storage elements contained on a single silicon wafer has risen from about 50,000 to over 6 million, with the cost of processing a wafer rising only very slowly and manufacturing efficiency expressed as the percentage of good units staying level or improving slightly.

Future progress in memory technology can be examined in terms of this single variable common to all present and future solid state memory technologies.

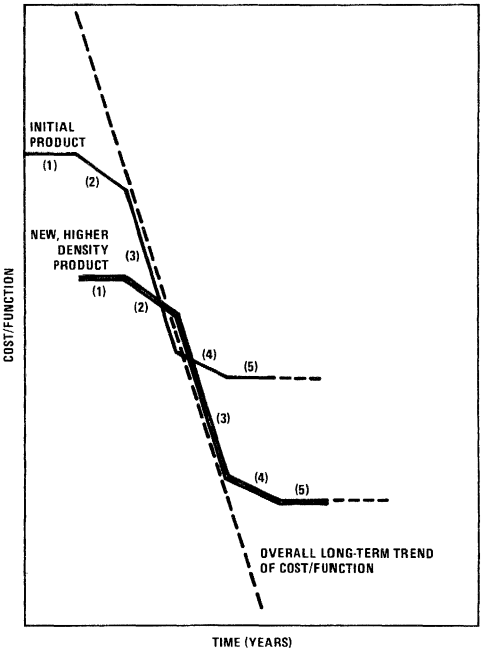
There are several technological trends that are unfolding right now which are likely to impact future memory technology developments.

These trends can be classified under the following categories:

a. Continued evolutionary process of memory cost reduction through more advanced circuit and device design techniques and improved process and manufacturing efficiencies.

b. A significant change in device and circuit sizes through major changes in pattern definition technology and an electrical scaling of devices to take advantage of the size reduction.

c. Charge Coupled Device and Magnetic Bubble Domain device based memory technologies.



NOTES:

(1) Product is introduced, very little or no competition.

(2) Product is multiple sourced but prices still hold up as production is limited.

(3) Production expands dramatically as yields improve, competition is fierce, prices tumble, marginal suppliers are beginning to drop out.

(4) Significant yield improvements are no longer available, new product is beginning to compete for the same market, competition is still intense, suppliers still drop out.

(5) Major market share is taken by new generation of product, market shrinks but prices hold up as competition is minimal.

FIGURE 1. Typical Decrease of Memory Products' Prices/Costs During Product Life

*Refer to Introduction. This paper presented at COMPCON 1977

a. EVOLUTIONARY PROCESS

This approach has so far been the most successful and continued improvements may still be expected. In fact, as long as this is a viable path for future development, it is likely to be the most vigorously pursued approach.

In terms of its future potential, we might examine past contributions to batch density improvements.

The total batch density improvement of 120-fold in eight years was contributed by:

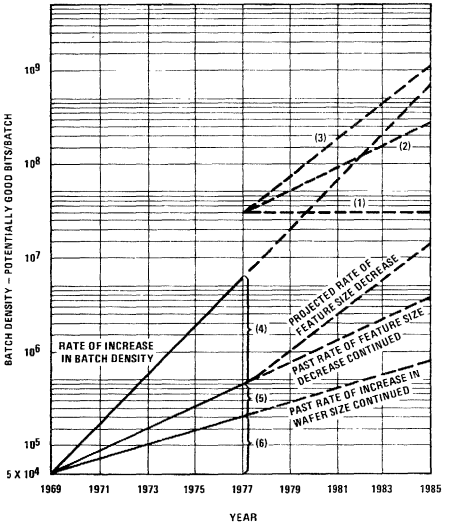
1. Higher bit density through design and process innovation: 13.5x
2. Larger wafer area: 4x
3. Smaller feature sizes and tighter alignment tolerances: 2.2x

Continued improvement based on comparable contributions from the same sources is no longer feasible for the following reasons:

Design and process improvements, the most profitable source of past batch density improvement, is getting sufficiently close to its theoretical limits so that progress in it is likely to slow down *(Figure 2)*. It is clear that regardless of whatever technique we use to design or build a memory cell, it must have at least 2 features in both x and y directions, one to store the information and one to separate it from the adjacent cell. This defines a theoretical minimum cell size of 4 f^2 where f is the minimum feature size determined by the limits of pattern definition technology.

Cell size eight years ago was a rich 200 f^2 leaving plenty of room for improvement. Today's cell size of 20 f^2 or less is sufficiently close to the theoretical limit of 4 f^2 that we can no longer project a rate of improvement comparable to past norms. We will do extremely well if we can extract a further 3-fold improvement.

Wafer size improvement will continue at an essentially constant rate. Wafer size increases are important not only for increased productivity, but wafer size is strongly correlated to maximum economically manufacturable die size *(Figure 3)*. Wafer diameter has been increasing at a rate of about 1.4 times every four years. This rate of increase is tied not only to the rate at which equipment manufacturers can develop new tooling to handle the larger wafer size, but also to the rate at which capital is invested in the semiconductor industry.



NOTES:

(1) Theoretical limit, current wafer and feature sizes.

(2) Theoretical limit, assuming continued improvements in wafer size increase and feature size reduction.

(3) Theoretical limit, assuming constant rate of wafer size increase and an *increasing* rate of feature size reduction.

(4) Increase due to design and process innovations.

(5) Increase due to feature size improvement.

(6) Increase due to wafer size.

FIGURE 2. Past and Projected Contributions to Batch Density Improvements

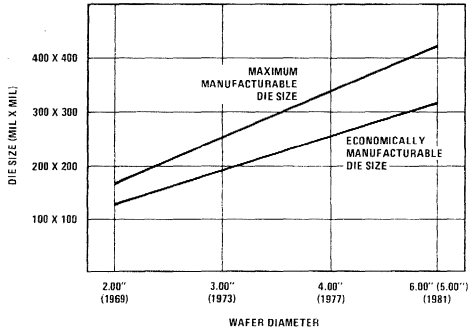


FIGURE 3. Maximum and Economic Die Size as a Function of Wafer Diameter (Time)

Feature size reduction. While we expect significant progress in this area, little of it can be considered evolutionary. In the past, progress in this area was completely evolutionary; contributing relatively little to density improvement. In the next 5 to 10 years we expect major changes in the technology and we will discuss those changes in detail later.

We also expect that manufacturing yields will increase in the next 5 to 10 years. This will be a factor in cost reduction but not in density.

The reason for yield improvement is the expected reduction in the rate of density improvement due to design and process improvements. Present manufacturing yields which include losses in wafer manufacturing, die sort, assembly and final test vary from under 5% for a leading edge product to about 25% for a mature product.

In the past, as long as significant density improvements were available from design and process innovations, engineering effort and talent was better utilized in trying to improve a new high density product's yield from 5% to 25%. Trying to extract the yield improvement available between 25% and 50%–60% which is

probably the practical upper limit for any semiconductor product, was both harder and less rewarding. With less potential improvement available from design and process innovations, we can probably expect higher overall yields for mature products.

In summary, the evolutionary trend, while it will still contribute significantly to future cost reductions, its contribution will be proportionately less than it has been in the past.

b. FEATURE SIZE IMPROVEMENT

Minimum feature size has been remarkably stable over the past 20 years of integrated circuit technology development. This was probably due to the fact that there was very little change in pattern definition technology. Up to 1975 the pattern definition technology, at least at wafer level, was basically unchanged from what it was in the late 50's and progress was obtained by better engineering, controlling and understanding the process and using improved photochemical materials.

Maskmaking technology made much more consistent progress, converting from an essentially manual drafting to a completely computerized pattern definition process.

Since the mid-70's, very significant changes are beginning to occur at wafer level too. Availability and acceptance of *projection aligners* is the first and probably the most significant of these changes.

Their introduction did not lead to an immediate reduction in feature size, but the control, reproducibility and accuracy of mask dimensions that they allow, makes feature size reduction a much more realistic task.

Improved high resolution photoresists are also becoming available.

Dry etching techniques are important technological achievements and will also be contributing to feature size reduction.

Electron beam and X-ray lithography are the most frequently mentioned technologies to achieve significant reductions in feature size.

There is undoubtedly significant progress being made in these areas and some of the results are impressive. However, they have to overcome some very significant technical and economic hurdles before they can make an impact on memory technology *(Figure 4)*.

Electron beam writing techniques are already available for maskmaking purposes where they offer some very real advantages. For direct writing on wafers, however, they still have to improve significantly and come down in price before they can make an impact on memory technology. Presently, projected machine costs and throughput times are such that processing wafers with electron beam writing instead of conventional masking—assuming no other technical problems—would raise wafer processing cost by a factor of 5. This cost increase would take care of all cost reduction achieved by the smaller feature size at *equal yield*. Since the smaller feature size means more densely built circuits sensitive to much smaller defect sizes the most immediate consequence of feature size reduction is yield reduction.

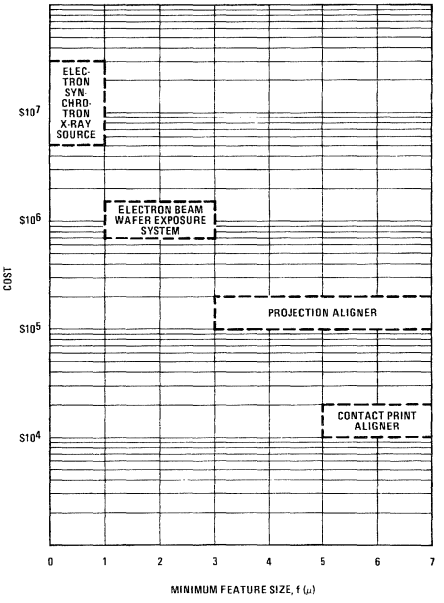


FIGURE 4. Cost of Key Equipment for Various Pattern Definition Technologies and Minimum Feature Sizes

X-ray lithography techniques have still to resolve three basic problems.

a. Maskmaking technology

b. Sufficiently intensive X-ray sources

c. Pattern registration

If they can solve these problems, they can be potentially very powerful as they can use a fixed mask and do not have to regenerate the entire pattern at every exposure.

Summarizing present status of pattern definition technologies, we can project improvements in optical pattern definition technology to yield a 5 to 8-fold increase in batch density over the next 5 to 8 years. This will represent a 2.5 to 4-fold increase in the rate of progress compared to past experience. Even higher rates of progress are possible if electron beam and/or X-ray lithography matures sufficiently to become cost effective, over the next 5 to 8 years.

Electrical Scaling of Devices

In the previous discussion, we have made the implicit assumption that feature size reduction is equivalent to circuit area reduction.

This is most certainly not the case. Feature size reduction will merely define limits to circuit size reduction. The actual reduction available will be determined by how closely the electrical device and circuit characteristics allow us to approach the limits imposed by pattern definition technology.

All three presently used major memory technologies (i.e., MOS dynamic, MOS static and bipolar static) are more limited by device and circuit design considerations, rather than optical pattern resolution.

In case of MOS devices, their performance is a function of the operating voltages and their ability to handle high operating voltages decreases very rapidly with reduced device sizes. Consequently, if denser memory circuits were to be built by taking advantage of feature size reduction, the operating voltages will have to be reduced. The resulting device and circuit performance reduction can be regained by re-engineering the entire device, reducing oxide thickness, junction depth and increasing substrate doping to make the device deliver an equivalent performance at lower operating voltages.

This total re-engineering of device structure, processing and manufacturing technology is called "scaling" and it is obviously a major engineering and manufacturing task, involving all aspects of wafer technology.

Bipolar memory circuits do not appear to suffer from this limitation; their's is, however, a different one. Device sizes can be reduced but their density cannot be significantly increased, because current drain of a bipolar device does not scale with size. Consequently, any attempt to take advantage of reduced device size by increasing number of bits/chip will run into severe power dissipation limits. Again the problem is technically solvable at an expense of major circuit design/process re-engineering efforts to "current scale" bipolar device/process technology.

I^2L technology appears technically attractive from this point of view (i.e., it would be able to take advantage of feature size reduction with the least amount of device and/or process engineering changes). Its problem is that it has so far not been able to establish a sufficiently attractive price/performance combination to gain a significant position in the memory market.

Feature size reduction and the required electrical scaling of devices will have some very important consequences in terms of relative impact on various memory technologies. When we scale devices, we adjust some basic device parameters and operating voltages so as to obtain as nearly identical device and circuit characteristics as possible. This can be achieved quite successfully for the type of circuits whose design is by and large based on the device characteristics that we have scaled (i.e., MOS static devices). For these devices, reduction of supply voltage also brings about a reduction in power dissipation, so one limitation to higher density, characteristic of static devices has also been removed.

MOS dynamic circuits which have traditionally enjoyed a 4:1 density advantage over static devices, rely more on second order effects like leakage currents, subthreshold conduction and signal to noise ratio in their sense amplifier designs, do not benefit quite as readily from scaling.

Leakage current, whose relation to stored charge is vitally important to the successful operation of MOS dynamic random access memory circuits, does not scale proportionately with voltage, due the point defect nature of the leakage current. Typically any junction's leakage current represents a spatial averaging over a relatively large number of defects. Reducing junction area will increase fluctuation in number of defect sites from one storage area to the next. Since dynamic RAM design imposes requirement that *all* storage areas have less than certain pre-determined amount of leakage current, scaling will typically reduce ratio of stored charge to leakage current. Since the signal available is already reduced by both scaling and the resulting increase in density, designers of future generation of dynamic RAM's face some formidable challenges. It is possible that the only way they will be able to overcome these challenges is to impose very strict environmental limitations on the finished product, namely cooling or even refrigeration of memory systems.

Feature size reduction and electrical scaling will impose some very stringent demands on process engineering in terms of both control and the degree of perfection required for good yields from the scaled structures. We are assuming that these problems are solvable by evolutionary improvements in processing techniques. We should not be surprised, however, if progress in those areas from time to time fails to keep up with the more visible improvements available from pattern definition technology.

c. NEW TECHNOLOGIES

Success in semiconductor integrated circuit based random access memory technology prompted considerable interest in solid state replacements for serial memories. The two most often considered candidates are Charge Coupled Devices and Bubble Domain Memory devices.

Charge Coupled Devices represent the densest silicon based technology we know. However, their speed and ease of use is considerably inferior to random access memories and as long as random access memories can be made with comparable circuit density, C.C.D. is hard pressed to carve out a market position. Typically, for a C.C.D. circuit to be competitive with RAMs, it has to offer a 4:1 density advantage over a comparably sized RAM circuit. So far it has not been able to do it, partly because RAM technology very quickly adopted all process improvements made for C.C.D. circuits and used them to make competitively sized RAMs.

However, C.C.D. technology is expected to establish a 4:1 density advantage over RAMs in the reasonably near future because its technology and organization permits:

a. Approaching the theoretical minimum storage area of 4 f^2 both more easily and more closely than RAMs.

b. Meeting the challenges of feature size reduction and device scaling more easily than dynamic RAM's.

Several features of C.C.D. technology contribute to these advantages. Absence of P-N junctions allows storage and transfer functions to be very similar structurally and either very closely spaced, or used interchangeably for both functions.

Although charge is stored dynamically, it is not held at any location for longer than a clock cycle so effect of

defect density fluctuation is averaged out over a large area. Signal strength is comparable to RAM's but there is more flexibility in sense amplifier design. Absence of contacts and P-N junctions allows more efficient layout and easier scaling of devices.

Bubble Memory Technology

Although both its device and material technology is significantly different from silicon integrated circuits, it is also based on a batch manufacturing process with the cost of a function very strongly dependent of the functional density per batch and manufacturing yields.

Examined from this point of view, it has some very major disadvantages coupled with some even greater potential long-term benefits.

First of all, as a device it is very well suited to serial storage of data. Although it is slower than any silicon I.C. based storage circuit, it is non-volatile—or at least it can be designed to be—and it can also be used to perform very simple logic functions which allow data to be stored and retrieved efficiently. Also, it can be used to pre-amplify the otherwise very small signal magnetically so it can be used to design a reasonably self-contained memory chip.

Its known major disadvantages are:

1. Very high material cost, caused by both very high initial substrate cost and a very costly, difficult and low productivity liquid phase epitaxy deposition process. Material cost is 30—50 times higher than silicon.
2. Very high packaging cost. Every circuit has to have an individually adjusted bias field and a rotating magnetic field built into the package.
3. A batch density which is presently not significantly higher than what is achievable with silicon.

Set against these disadvantages we can consider the potential long-term benefits which motivate the ever increasing activity in the field:

1. Processing typically requires only 3 masking steps, only one of which is critical, compared to 6+ for silicon.
2. Although present bit density is not impressive, it is based on a relatively simple design with bit area being in the 200 f^2 region for a T bar configuration, indicating very much room for improvement, some of which has already been implemented experimentally.
3. Because it has only one critical masking step and no critical alignment requirements, it is the technology best positioned to take advantage of improvements in pattern definition techniques.

It is difficult today to determine the point both in time and in level of complexity at which Bubble Memory Devices will be able to enter the market and compete successfully. But once they do, they will enjoy a very rapid growth comparable to silicon integrated circuit based memory circuits for exactly the same reasons.

Summarizing these trends, there is sufficient visibility for the continued technical progress of memory technology at essentially unchanged rates for the next 5 to 8 years.

One word of caution, however, is worth mentioning here. The key to past success and the continued objective of memory technology development is *cost reduction*.

Technical developments to continue to increase density of memory circuits are worthwhile only if they can make a significant contribution to this overall objective. They cannot do it if the cost of improvement is so high that it swallows up all future cost benefits.

Even if their cost is less than potential cost reduction benefit, they still represent a very significant investment in design, process development, production and testing facilities and product start-up costs for the component manufacturer.

Such an investment will only be economically attractive if the market for memory products continues to expand at a fast rate.

Static or Dynamic — The Selection Process for a Memory System

National Semiconductor
Memory Systems Division
J.C. Blackie†
November 1977

INTRODUCTION

Today's memory system designer is faced with a bewildering number of technology choices for his memory devices. He is offered overlapping performances from different technologies, different cell structures, and different packages. In addition, he is told of new developments daily that will obsolete all of the information he has already gathered. He is placed in the position where he must choose a technology, not on today's price, but on a projected price based on estimated minimum costs from vendors who are not yet in production with the devices they are offering.

There are many charts available showing the relationship between cost per bit, and learning experience, and the relationship between die size, and cost, on devices sharing the same learning experience; yet the driving reasons behind the costs are not always discussed. In addition, the device costs given do not reflect any additional expense that the user must incur in additional test costs. This additional testing can require significant capital expenditure and additional processing cost if the memory system is to achieve the reliability levels possible from semiconductor memories.

In an attempt to identify these costs more clearly, this paper will outline the decision processes and qualification testing to be followed by a design team choosing devices to be used in a line of standard memory systems that are to be competitive with existing core systems.

The systems were required to be single-card products utilizing power available in the user's system. They cover memory ranges from 16k x 18 to 128k x 18, in increments of 16k. The fact that the systems are to compete directly with well-established core modules, places a high emphasis on low cost and reliability. In addition, it dictates that static memory devices have to be seriously considered for potential applications where dynamic memories can not meet existing interface restrictions. In order to be cost effective with core systems, a volume selling price goal of 0.3¢/bit for the lowest density system, dropping to 0.18¢/bit at the highest density, was required. An analysis of the manufacturing costs of a wide range of semiconductor memory systems currently in production provided a set of non-storage cost constants. These constants define price goals for the memory devices. The systems analyzed had complexities ranging from cards with transparent error correction and power-down modes for battery back-up operation, to those offering high-storage densities with minimal overhead logic.

Figure 1 shows total non-storage costs in cents per bit of memory system versus memory system size. Although this data was compiled from dynamic memories, static figures were obtained by deducting the cost of all elements whose sole purpose is to support the need to refresh the system. Using the numbers shown in the table, one is able to establish maximum prices for memory devices that allow the design of semiconductor systems that are cost effective against core modules. Using a composite of predicted pricing from many vendors, the lowest cost per bit anticipated in mid-1978 for dynamic memory is 0.06¢/bit for both a 4k x 1 configuration and a 16k x 1 configuration. The lowest cost per bit anticipated for static devices is 0.15¢/bit for a 1k x 1 configuration or a 4k x 1 configuration. In each type, pricing per bit of the higher density configurations are projected to be on a significant downward trend while the lower densities are flat. Another fact that emerges is that static devices can be cost effective with core at low densities, but do not yield the lowest cost per bit solution in applications that can accept dynamic devices. Static devices greatest application appears to lie in areas where:

a. System performance is severely impacted by cycle stealing for refresh of dynamic memory.
b. Board space limitations do not allow space for additional logic required for dynamic interface
c. Memory requirements are small and can share a board with other system components.

As the system design goal is to replace core systems, there are many situations where the requirement to interrupt system usage for refresh cycles is impractical, thus there is a requirement for static versions of all modules.

Figure 1 shows that even with devices currently in production (1k x 1 static and 4k x 1 dynamic) semiconductor memory can be cost effective up to 32k x 18; the choice becomes marginal at 128k x 18. However, with the advent of the higher density devices in 1978 (16k x 1 dynamic), semiconductor systems establish a clear price advantage over the entire range (16k — 128k). Having established that cost effective devices are available, the designer is now faced with the task of choosing which device and which vendor should be selected. Since the goal is core replacement, the designer can restrict his choices to MOS devices that provide access times in the 150 ns to 200 ns range. These speeds allow him to provide systems to match or exceed typical core performance, even if a transparent ECC scheme is used to enhance reliability.

MEMORY SYSTEM CAPACITY	*TYPICAL NON-STORAGE COST TO BUILD/BIT	
	DYNAMIC	STATIC
16k x 18	0.046¢	0.032¢
32k x 18	0.04¢	0.027¢
64k x 18	0.039¢	0.027¢
128k x 18	0.039¢	**

*Includes PC board, peripheral circuitry and assembly
**Single card product not available

FIGURE 1

†Refer to Introduction. This paper presented at COMPCON 1977

Because it is uncertain when the higher density parts will be available at a lower cost per bit than established product, careful consideration should be given to a design approach that will allow a single board to use both high and low density devices. However, this approach should only be followed if an analysis of the devices and vendors shows that the compatible devices offered meet all of the performance and cost goals. The cost of designing a card for each type is not great enough to warrant compromising performance or reliability with a single card design. Thus, the designer should feel free to make an unbiased choice of device for high and low density products as he starts the device selection phase of his design.

DEVICE SELECTION

A survey of product available shows several choices of 4k x 1 dynamic configurations, an 8k x 1 dynamic device, and a couple of 16k x 1 dynamic configurations. In addition, there are several choices of 4k x 1 static configurations. (In order to reduce the choices to a more manageable number, the designer must compile a list of factors that will impact the potential cost of a device).

The first and major factor is pressure of competition. The availability of several qualified vendors committing to volume production ensures a long-lived product with an industry-wide commitment to maximize yields. Because volume production commitments from several vendors is dependent on large users choosing a particular configuration, a knowledge of who is committing to use the device types selected, and when, is significant in the selection of a device.

The second factor is die size. This is more difficult to evaluate because the smallest die sizes might be obtained with special processing technology that has not been optimized and therefore will take longer to reach an optimum yield. This would have a serious impact on a product that must be introduced into an established market place as soon as possible. It is necessary to weigh projected die cost by a process learning factor. (Learning experience on a product typically leads to a 3:1 improvement in yield over a one-year period of volume production). Thus, the *means* employed to reach a small die size is more important than the actual size. A small die achieved by unique chip design without resorting to especially tight masking tolerances or critical processing techniques certainly would give a vendor a definite cost advantage which would be available to a system designer. The variation in die size offered by the vendors who scored high on the other factors outlined in this paper was not significant enough to influence the potential die cost.

The third factor is the type of package that will be offered. Several considerations can create package limitations that may not be obvious from the initial evaluation samples which are usually supplied in a hermetic side-brazed ceramic package which, although expensive, places the fewest restrictions on the device's performance. The lowest cost product will be one that can be packaged in CERDIP and plastic. CERDIP can put a restraint on the die size, and plastic can restrict its operating speed. Thus, the choice of a high-performance part with a wide die may be a poor choice from a low-cost standpoint, because its die may not fit in CERDIP and a high performance device may suffer degraded performance in plastic.

The fourth factor really concerns the choice of vendor rather than a specific product or process, but it is a key consideration from a cost viewpoint. An evaluation of the component supplier's process control program and his level of quality and reliability activity is important. Absence of a meaningful program will affect the level of yield improvement that can be expected within a certain time frame, and will raise the cost of administering product through the system designer's facility. Troublesome vendors with marginal product create extra costs.

Application of the above factors to the devices, in our case, allowed the device selection to be narrowed down to a 16k x 1 RAM from 4 viable vendors, and a 4k x 1 static from 4 viable vendors. These 2 parts offered the lowest potential cost per bit through 1979. This choice did not take into account the high performance static product announced at the Solid State Conference in Philadelphia in February 1977 because that level of performance was not needed. In addition, the technologies outlined, although very significant in terms of superior performance at a lower bit cost, will not be cost effective in lower performance applications in the near future.

Having chosen the devices and vendors, the designer must develop a detailed specification for the parts he needs to procure. This leads him to the next phase of his device selection.

CHARACTERIZATION

The error-free performance of any memory device is a function of the stability of the memory element and its ability to function correctly in the presence of electrical noise and temperature variation. In order to ensure that a system design does not exceed the tolerance of the memory device, a designer must have these limitations defined so he can structure his design correctly. The purpose of the characterization phase of the system design is to define these optimum operating conditions.

Each potential vendor chosen during the device selection stage submitted a small quantity of his devices for initial evaluation. This evaluation merely allows one to gain a familiarity with the device and is used as a vehicle to set up a characterization program. Any potential problems that would eliminate further consideration are noted, but this sample cannot be considered as suitable for final characterization. This device characterization must be performed on a group of devices comprised of samples from each speed range offered by the vendor. Each vendor's composite group is split into 2 groups. One is scheduled for a 1000-hour life test and the other for board characterization. This characterization and life test evaluation is the first and most critical phase of any memory system design. It must establish, as much as possible, each vendor's distribution. This will allow the designer to optimize his system around the chip design. Observing parts from the entire distribution allows him to identify operating region limitations with temperature, patterns, and voltage levels without

regard to specific data sheets. Potential pattern problems can often be identified by investigating anomalies in the device operating regions that are far outside the range specified in the data sheet using fairly simple test patterns. Once identified, these same anomolies can often be seen to move within the specified operating range when subjected to more complex patterns.

During the earlier selection phase every vendor supplies some level of characterization and life test data. Unfortunately in the early stages of new devices, the vendor has very little to offer. The most meaningful data is generated by device users and is not available for review. This is especially true for life test evaluations where it is very difficult to measure the need for extended burn-in from vendor's data. Most vendors offer some level of burn-in as part of their standard process flow, but do not define the level of infant mortality that might remain in the product shipped. This criteria is very critical to systems planned for high reliability. Therefore, the system designer must structure a life test evaluation that monitors infant mortality as well as long-term shifts in operating parameters. Infant mortality problems in semiconductor devices are shipping-lot dependent, thus lots should be continuously sampled for evidence of infant mortality problems remaining after the vendor's standard burn-in. This problem can be avoided by providing 100% extended burn-in, but this is prohibitively expensive for a low-cost product. An incoming program that required a sample burn-in of all lots can effectively identify lots requiring extended burn-in. In addition, it gives valuable information on the control levels implemented by each vendor. So armed with the data collected from the characterization phase the system designer can proceed to the design of his peripheral logic, and the structuring of his system. He can weigh the impact of interface logic design against chip performance and arrive at the most cost effective and reliable memory system. His system test plan can be designed to effectively catch marginal devices that could create field problems, and achieve the highest levels of reliable operation.

CONCLUSIONS

The rapid development of the semiconductor memory market has made available a wide range of products, offering potential performance and cost advantages. However, the market place is limited and not all of the devices offered will reach their cost goals. Thus, the system designer's task is to first select a device that has wide acceptance, and has several viable vendors. Device performance must be obtained without resorting to state-of-the-art technologies. He must then accept the fact that to obtain the optimum cost device it is necessary to precisely specify the performance needed and he must assure himself that each vendor's device comfortably meets that performance. He must accept the fact that he will be required to perform a significant amount of device characterization so that his design can be optimized to meet the twin goals of low cost and high reliability. Finally, his system test plan must be structured to thoroughly exercise all discovered pattern sensitivities in the basic devices. The choice of static or dynamic is one of system interfacing and not cost, and the use of static devices does not eliminate the need for careful device evaluation.

With the advent of the 16k x 1 dynamic device, the semiconductor industry is moving toward a standard configuration which will remove a significant amount of the present confusion of choice. The industry is also starting to extend the life of MOS products with cost reductions obtained by optimizing and shrinking existing designs. This will further simplify the designer's choice, as cell designs and chip structures will remain the same. However, it appears that the user of memory devices will still be faced with a need to carefully evaluate the devices he intends to use and perform some device screening if semiconductor memory systems are to reach the highest levels of reliability.

Section 2

Dynamic Read/Write Memory

2

Worldwide consumption of dynamic MOS read/write memory today exceeds that of any other type of semiconductor memory component. This has resulted in volume costs of devices such as the 4kx1 at under 50 millicents ($0.0005) per bit. Despite the low cost and extreme widespread usage, there still exists some concern and even mistrust regarding dynamic memory even among professionals. This is usually reflected in an effort to "avoid the hassle" at resulting higher costs. If you have experienced doubts regarding the application of dynamic RAM to your needs, this section should prove helpful. It is intended to reduce "problem pollution" and to eliminate the "hassle."

Dynamic RAM Board Design Made Easy

National Semiconductor
Memory Application
Stephen Calebotta*
November 1977

INTRODUCTION

Many new memory system designs are being done with dynamic RAMs. This is especially true as the new 16k RAM chips become more readily available. This application note is aimed at those engineers who are doing their first dynamic RAM designs. Its intent is to give some direction in how to design a RAM board so that it will give the greatest production yield with the least amount of difficulty.

We shall not talk about specific RAMs or interface to a specific processor. Most engineers can design control and interface logic for RAMs and most board designers can lay out a PC board for that design. However, the quality of that design will become apparent only after the RAM board is built and phased into production. Does it come up easily? Does it go through testing with little or no RAM chip fallout? Is it reliable in the field?

The key to success in a dynamic RAM system, or any other system for that matter, is margin. A system designed to maximize power supply and timing margins will be reliable and easy to manufacture. One that doesn't will be a manufacturing and field service nightmare.

In this application note we shall discuss RAM chip characteristics, power supply and control signal distribution on PC boards, and control logic implementation suggestions. As successful examples, in the appendix we shall provide the schematics and foils for some memory boards that are in production.

RAM CHIP CHARACTERISTICS

For reference we shall compare dynamic and static RAMs at the chip level. Then we shall describe the unique characteristics of dynamic RAMs which must be considered in a memory system design.

Dynamic RAMs versus Static RAMs

The basic difference between dynamic and static RAMs is the way they store data. The static RAM uses a flip-flop to store a bit, while the dynamic RAM uses a capacitor to store a bit. (See figure 1.)

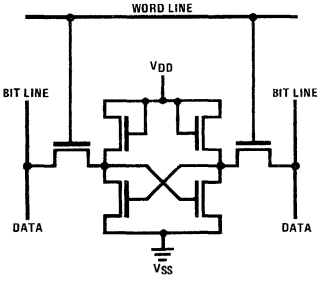
It is their respective cell designs that give each RAM its advantages over the other. Let's compare the RAMs for ease of use, power dissipation, die size, and price.

Ease of Use: The static RAM is easier to use because no refresh logic is required. In addition, static RAM control signals tend to be easier to generate because cycling is usually unnecessary.

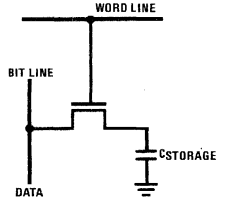
Power Dissipation: The dynamic RAM draws less power. The static RAM draws power continuously to sustain its flip-flops, while the dynamic RAM draws minimal power (1 to 2mA) between cycles. With continuous cycling, the dynamic RAM draws about as much power as the static. However, in a large memory system, dynamic RAMs save total system power since only one bank of RAMs is ever accessed during a memory cycle. All other banks draw minimal current except during refresh cycles. The duty cycle for refresh is approximately 1½ to 3%.

Die Size: Dynamic RAMs tend to be smaller. Due to the difference in cell designs, the die size of the dynamic RAM is often at least 20% smaller than that of a comparable static RAM from the same manufacturer.

Price: Because of smaller die sizes and much larger production runs, dynamic RAMs should always remain considerably cheaper than comparable static RAMs. In addition, dynamic RAMs save money in larger systems. Less chip power means smaller and cheaper power supplies. Smaller supplies mean a further saving in reduced cooling requirements. In general, the larger the memory system, the greater the savings by using dynamics.



Static RAM Cell



Dynamic RAM Cell

Figure 1.

Dynamic RAMs

Refresh: Since charge leaks off the storage capacitors, it must be replenished periodically in order for a dynamic RAM chip to retain its data. The charge in any one cell is replenished, or refreshed, every time that cell is accessed for a read or a write, At the same time, all the other cells in the same row are also refreshed. For that reason the entire RAM chip can be refreshed by doing only 64 cycles (for 4k RAM; a 16k RAM needs 128

*Refer to Introduction.

cycles) in 2 ms while sequencing through all the row addresses. The bit pattern presented to the column addresses does not matter. However, the setup and hold times must still be met. Unstable column addresses during refresh will cause data loss.

The hardware required for refresh amounts to a 6- or 7-bit counter for the refresh addresses, some way to multiplex the counter onto the RAM row address lines, a timer to signal when a refresh should be done, and the miscellaneous gating needed to couple into the usual read/write logic.

In some systems no extra refresh logic is needed. For example, in CRT systems normal operation sequences through all the row addresses in less than a 2 ms refresh period. This will be true only if the row address bits on the RAM chip are driven from the least significant address bits of the system. As a rule, this is good practice in all systems. By placing the most active system address bits on the RAM row addresses, normal system operation will automatically refresh the bulk of the RAM.

Cycling: One of the key functional differences between static and dynamic RAMs is the fact that dynamic RAMs must run through a cycle in order to read or write. Aborting the cycle by removing the chip enable too early or by trying to start a second cycle too soon after the first will probably cause data loss. Minimum chip enable on and off times must be observed.

Summary

Static RAMs are easier to use. Dynamic RAMs are cheaper, use less power, must be refreshed, and must be cycled.

MEMORY SUBSYSTEM DESIGN CONSIDERATIONS

Some memory board designs are easy to manufacture, while others, functionally identical, have low manufacturing yields seemingly due to the many "bad" chips. The difference between them is usually the amount of margin designed into each system. Power supply and timing margins are both critical, and as the margins go to zero or negative, the amount of "soft" errors goes up. (A chip has a "hard" error if a location consistently cannot be written and read back properly. It has a "soft" error if it only occasionally fails.)

On careful analysis, "soft" errors usually occur during a memory cycle in which some system parameter has gone out of spec. Since the RAM chips themselves have variations in their margins, replacing the offending RAM with one that has a greater margin in the out-of-spec parameter seems to cure the problem. This results in a large pile of "bad" RAMs. However, the real solution to this type of problem is in a careful system design and board layout in the beginning.

Power Distribution

By far the single most important aspect of a successful RAM system is good power distribution consisting of carefully designed decoupling and power gridding. The importance of good power distribution cannot be overemphasized.

Let's examine the problem. All dynamic RAMs have at least two supplies (V_{DD} and V_{BB}; V_{SS} is the RAM internal ground). Most also have a third called V_{CC}. We will discuss only V_{DD} since the other supplies have similar characteristics. Figure 2 shows the I_{DD} current waveform for a typical dynamic RAM chip during a memory cycle.

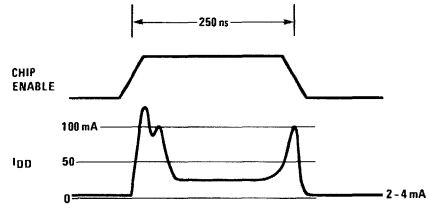


Figure 2.

At the beginning and end of chip enable, each RAM chip draws 50 to 100 mA current spikes with rise times of 20 ns. In addition, each RAM package draws a 20 to 40 mA DC current lasting for the duration of chip enable. The power distribution system must supply these currents while the voltages at the RAMs remain constant. Figure 3 is a schematic of the V_{DD} supply for a row of eight RAMs. The inductors are due to PC trace inductance which is about 10 nH per inch for a 13 mil trace. If the RAMs are on ½-inch centers there is 10 nH total between RAMs.

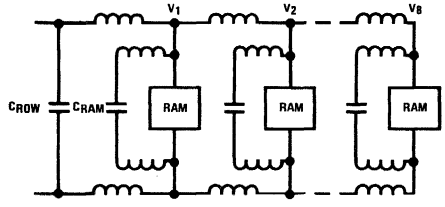


Figure 3.

If there is only one capacitor per row, and if that row capacitor, C_{row}, were infinite, the voltage spikes at the first, second, and last RAMs would be:

$$V_1 \text{ spike} = L \times 8\frac{di}{dt} = 10\,nH \times 8 \times \frac{100\,mA}{20\,ns}$$

$$= 400\,mV$$

$$V_2 \text{ spike} = L \times 15\frac{di}{dt} = 750\,mV$$

$$V_8 \text{ spike} = L \times 36\frac{di}{dt} = 1800\,mV$$

These spikes, especially the last two, are unacceptable.

If each RAM had its own decoupling capacitor, C_{RAM}, in series with 10 nH of trace inductance, the voltage spikes would be:

$$V_{spike} = L\frac{di}{dt} = 10\,nH \times \frac{100\,mA}{20\,ns} = 50\,mV$$

which is very good. Local decoupling should be used to overcome the spiking problem.

The ability of the power distribution system to supply the 20 to 40 mA per chip during a RAM cycle is also a function of the series inductance. For example, see figure 4.

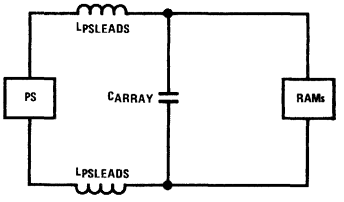


Figure 4.

Let the total power supply lead inductance be 50 nH. (We are ignoring the PC trace inductance within the RAM array itself.) What would the voltage step have to be at the RAMs to get 40 mA x 8 flowing in 20 ns? The equation is:

$$E = L\frac{di}{dt} = 50\,nH \times 8 \times \frac{40\,mA}{20\,ns} = 800\,mV$$

which is a large step which should not occur with adequately designed decoupling. Therefore, the bulk of the DC current for cycling the RAMs comes from decoupling caps themselves, and therefore they should be large enough to supply these currents with little droop. They should also be close enough to the RAMs to minimize the effect of the spikes. If we use a 0.1 μF cap, the droop for a 250 ns cycle would be:

$$V_{droop} = V = \frac{I}{C}t = \frac{40\,mA}{0.1\,\mu F} \times 250\,ns = 100\,mV$$

which is acceptable. Obviously, a larger capacitor will do an even better job of handling the droop. In addition, to help keep the droop to a minimum, the board should have about 50 to 200 μF of bulk decoupling on the +12 V supply. The other supplies can have less. Half should be placed near the point where the supplies enter the board. The other half should be placed at the far side of the RAMs so that the array lies between the bulk decoupling capacitors.

Alternatively, half of the bulk capacitors can be spread throughout the array. If this is done, use approximately 5 to 10 μF per eight RAM chips for V_{DD} and V_{BB}. For V_{CC}, 5 to 10 μF for 32 chips should be adequate.

Intuitively, this second approach seems better. However, the first technique works fine and is probably more cost effective.

The choice of capacitor types is very important. In all of the above decoupling calculations we have ignored the effective series resistance (ESR) of the capacitors. The effect of the ESR of real capacitors is probably at least as large as the effect of PC trace inductance and is a function of the capacitor type.

For best results, use ceramic capacitors for the local decoupling. The Memory Systems Group at National Semiconductor has had good results with ceramic capacitors of Z5U material from AVX and Sprague. To illustrate how important the Memory Systems Group feels these capacitors are to good memory board performance, every lot is subjected to an incoming inspection which includes, among other things, a transient response test.

For bulk decoupling, solid tantalum capacitors are recommended. They have better transient response than most other large value capacitors and they put a lot of capacitance into a small package which simplifies board layout.

A word about power gridding. If there are a number of rows of RAMs, all power supply traces to all RAMs should be run both vertically and horizontally throughout the array. Providing multiple paths through the array reduces the effective inductance of the power distribution system.

To summarize power distribution, we can say the following:

1. It is the single most important aspect of a good RAM board layout.
2. Use plenty of decoupling. The decoupling caps not only reduce voltage spikes, but also provide most of the RAM power during the cycling. Lay out the board for a 0.1 μF capacitor per power supply per RAM chip (up to three capacitors per chip). As production history accumulates, it may be possible to omit half the capacitors. However, lay out the board for one per supply per chip. Use 50 to 200 μF of bulk decoupling on +12 V. On +5 V and −5 V use 25 to 100 μF.
3. The decoupling capacitors should have the shortest possible traces back to their respective RAM power supply and ground pins. To reduce inductance further, these traces should be as wide as room will allow.
4. Traces running the power supply voltages throughout the array should be as wide as possible. However, with good decoupling design, even minimum trace widths will probably be acceptable. If some power supply traces can be wider than others, make V_{SS} (Ground) wider first, V_{DD} next, V_{BB} next, and finally V_{CC}. Ground is the key. Grid the supplies even if the traces are heavy in one direction and light in the other.
5. We have purposely omitted any discussion of multilayer boards. They tend to simplify power distribution problems, but the types of problems that must be solved are the same. Only the magnitudes have been somewhat reduced. Almost everything that has been said up to now is still applicable to multilayer boards.

Data and Control Signal Distribution

The second most important aspect of the successful RAM system is address, data, and control signal distribution.

Let's discuss the chip enables first. This is the most important signal to the RAM and all timing is referenced to it. There are two types of chip enables in common use today: 12 volt and TTL level swings. Running chip enable lines through an array tends to be less of a problem than one would think. There are only two things to keep in mind. First, place the actual driver chip near the RAM array it is driving, making the chip enable run short and direct. Second, put a damping resistor near the driver. Do this for either TTL level or 12 volt chip enables. Select the value of this resistor to

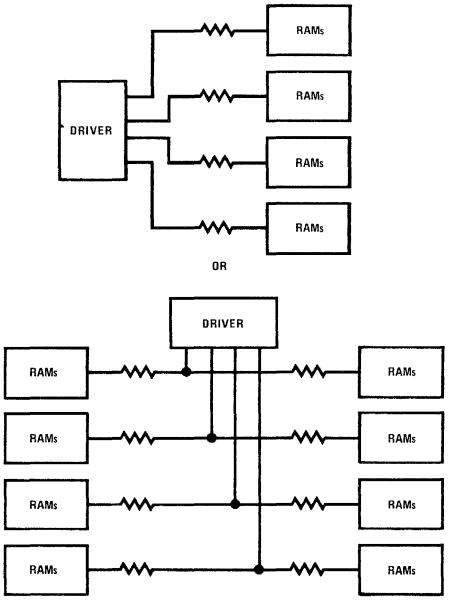


Figure 5.

give the best clock waveform at the RAM chips. Its value will probably be between 10 and 51 Ω. Figure 5 shows the commonly used arrangements.

The reasons for these two recommendations stem from the fact that, at the frequencies encountered here, the clock lines are, in fact, transmission lines. The impedance of the line is determined by:

$$Z_O = \sqrt{L/C}$$

where the impedance of the clock line within the array of chips is in the range of 10 to 15 Ω while the unloaded line between the clock driver and the chip array is in the range of 30 to 50 Ω.

In order to drive the clock line cleanly, some attempt must be made to match the clock driver's output impedance to that of the line. The actual output impedance of most monolithic clock drivers varies as much as 3 to 1 and so we choose a fast clock driver with low output impedance and put a damping resistor in series to empirically set the effective output impedance to match the line (with only about 10% variation).

Long clock lines or long lengths of unloaded clock lines can cause problems. In the case of the long clock line, the open circuit at the far end of the line causes the reflection from the end of the line to return to the driver after the end of the rise time, resulting in ringing. In the case of the long unloaded length of line, the reflection from the junction of the unloaded and loaded sections of the line (due to the mismatch) causes glitches in the clock transitions.

To minimize crosstalk from chip enable to other signals, try to run chip enable at 90° to other signals. This is usually hard to do in an actual layout. As an alternative, leave as much room as possible between chip enable and adjacent traces as it runs through the array. Typically, signals in the array are on 50 mil centers. Moving the two adjacent signals more than 50 mils away from chip enable will help some in reducing crosstalk. However, as stated earlier, there seem to be very few problems associated with chip enable. Neither CE itself nor crosstalk to other signals will be troublesome if the above guidelines are observed.

Address, data, and control signals such as read/write (or equivalent) should be run as directly as possible. Their layouts tend to be non-critical. The critical thing is timing. The control logic should be designed to maximize setup and hold times with respect to chip enable. Again, high production yield is related to margins. As an example, consider a RAM board that was built for an 8080 system. The chip used was MM5271 4k RAM which has a low true TTL level clock input. The signal that controls read, write, and refresh is called TSP. The MM5271 data sheet says that the setup time for TSP is zero ns with respect to the leading edge of chip enable. When doing a refresh, TSP must be low at the beginning of chip enable. The original timing brought TSP down at the same time as chip enable. The system seemed to work. However, it would make an error once every half hour or so. With an oscilloscope everything appeared to be within specification. When TSP and chip enable were superimposed on the scope, their leading edges were absolutely coincident in both time and waveshape. The TSP/chip enable relationship was examined very, very carefully and pronounced okay. Finally, in an attempt to cure the problem, the TSP timing was changed to give about 50 ns of setup time and the problem disappeared.

The point was that the original design was done to the limit of the memory data sheet even though there was no need to do so. The success of the operation depended on the shape of the two waveforms to keep the system in spec. Once margin was designed in, with no hardship at all in the design, the system operated flawlessly.

In high-speed systems where it is hard to design in extra margin, use damping resistors in address, data, and control lines to help control their waveshapes. A resistor in every address, data, and control line allows these waveforms to be optimized, which gives the system improved margin over an undamped design. Use damping resistors only where necessary. Leave them out of signals that have time to settle down before they are needed.

Summarizing the use of damping resistors: always put them in chip enable lines, whether they are TTL levels or 12 V levels. Use them as necessary in those address, data, and control lines whose timings are approaching the limits of the RAM chip data sheet. Design in margin first. Tune it in when it can't be designed in.

LOGIC CONSIDERATIONS

These also affect yield. For example, a RAM cycle must never be aborted before its normal completion. The control logic must be designed to never permit a shortened cycle. At this point we shall briefly discuss some techniques for timing and control.

Timing Generation

The actual phasing of control signals can be done a number of ways. Existing system level control signals can be used. This is easy in some 8080 and PACE systems. When the available system control signals aren't quite up to the job, another technique that works

quite well is to use a high frequency oscillator and a shift register connected as a Johnson counter. Any timing signal that is necessary can be generated from a Johnson counter using a 2 input gate. This technique has a minor drawback if the high frequency oscillator is asynchronous with respect to the main system timing. The RAM cycle timing will always have a finite uncertainty with respect to the system cycle timing. This uncertainty is equal to the clock period of the high frequency oscillator. To apply the same technique but to avoid the timing uncertainty, use a gated delay line oscillator instead of a crystal or RC oscillator. Delay line oscillators can be started and stopped reliably. Crystal and RC oscillators take a few cycles to settle down and therefore are not reliable in a start-stop mode. How about one-shots? Do not, under any circumstances, use one-shots in critical timing applications!

Refresh Timeouts

A counter and oscillator are best. An astable oscillator is acceptable but must be carefully designed for worst case minimum frequency with respect to temperature to ensure the RAM gets refreshed often enough. At the end of the timeout a flip-flop should be set. When the refresh cycle is finally completed, that flip-flop should be reset. The timing should be such that it doesn't matter when the RAM gets refreshed within the refresh timer period.

Transparent versus Non-Transparent Refresh

Most microprocessors have predictable periods of time when they will not access the RAM board. Usually it takes little effort to insert refresh cycles in these times, thereby making refresh transparent to the CPU. When the CPU is very fast and is using the bus almost continuously, the refresh will have to hold up the processor. Even then, some clever design will minimize the time spent doing non-transparent refresh.

Single Step

Some systems need the capability of single stepping through programs. Since dynamic RAMs must be refreshed continuously, the output data from RAM should be latched. This permits single stepping because every time the address changes, the RAM is read and the data is latched. Then the refresh proceeds behind the latches, never disturbing the data. The RAM appears static.

DMA

DMA should be little different from normal cycles. One thing that must be considered is how to handle refresh. Three techniques immediately come to mind. First, have the DMAing device permit refresh periodically. Second, limit the DMA frequency. Make the period between DMA cycles equal to a normal RAM cycle plus a refresh cycle. This way the refresh can be handled transparently to the DMA. The third technique would be to limit the DMA time to something under 2 ms and at the end of the DMA do a burst refresh of the entire memory. There are a number of other ways to handle refresh and DMA. Performance of the system will determine which technique is most appropriate.

From a system standpoint, the most important aspect of DMA and dynamic RAMs is the polarity of the system level control signals. In a TTL system where bus control can change hands, the control signals must be *low true*. The reason for this is that, as control transfers from the CPU to the DMA device and back again, there will be short periods of time when the control lines are floating since neither device is driving the lines. In a TTL system, floating lines look high. If control signals have been defined as high true, then as the lines momentarily float, devices such as our RAM board will think that a command has been issued and will start an unintended cycle. Then the problem gets compounded. During the unintended cycle comes the command for a real cycle. Either the unintended cycle will be aborted, which destroys some RAM contents, or the intended cycle will start too late, causing other problems in the external system. An example of a bus with this problem is the S100, or hobby standard bus. It mixes signal polarities and, therefore, makes dynamic RAM control logic unnecessarily complex. If there is only one controlling device, signal polarities are academic. But if control can transfer, make the control lines low true.

SUMMARY

Refresh requirements make dynamic RAMs slightly harder to use than static RAMs. However, they pay the designer back for his efforts by reducing overall system cost in three ways. First, dynamic RAMs tend to be cheaper than static RAMs of the same size. This is primarily due to smaller chip sizes and higher production volumes than comparable static RAMs. Second, dynamic RAMs use less power. When a dynamic RAM is not being accessed it draws much less current than a static RAM. During access, dynamic and static RAMs draw similar amounts of power. However, in a large array, only that bank being accessed draws full power. All others still draw standby currents so that the total system power is lower than for a comparable static system. Because of the reduced power requirements, power supplies are cheaper. And, third, due to lower power dissipation, cooling requirements are reduced, allowing a further saving.

There are three things the system designer can do to maximize RAM board yields during manufacture. First, design proper power supply decoupling. This is probably the single most important consideration for the designer. A good high frequency 0.1 μF capacitor per supply per memory chip is recommended. A capacitor per supply per two chips is probably okay, but the board should be laid out for one capacitor per supply per chip and then capacitors can be left out as yield data becomes available. For bulk decoupling use about 50 to 200 μF per board on +12 V, less on +5 V and −5 V.

Second, design in as much margin as possible in all control signal timing. Use damping resistors where necessary. If timing is designed right to the minimum specs, periodically the right combination of data pattern, power supply noise, temperature, cosmic radiation, etc., causes the system to fail. The combined worst case parameters push a signal beyond specification and the memory fails.

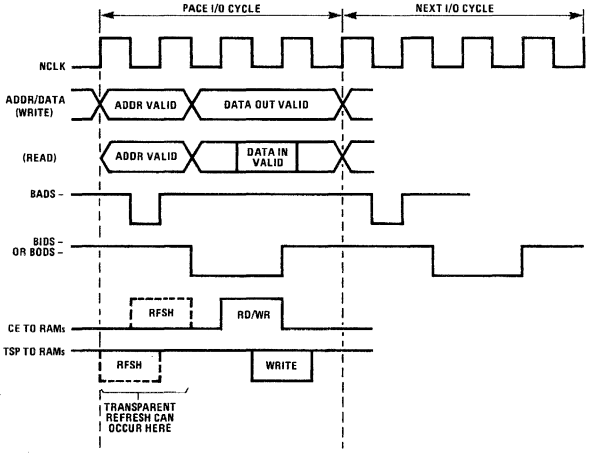
Third, never allow spurious, shortened memory cycles to occur. Shortened or aborted memory cycles are guaranteed to destroy data in the row that was addressed during the aborted cycle.

Any designer who uses reasonable care can successfully design dynamic memory systems which will be easy to manufacture and very reliable in the field.

APPENDIX A

Appendix A shows a simplified timing diagram and schematics for a 16kx8 RAM board used by a PACE microprocessor for byte mode data storage.

RAMs are MM5270 4k RAMs with 12 V chip enables. All timing is generated from existing system signals. DMA is not now in use, but is possible in the future. Control signals from the bus are low true. Refresh is transparent, done at any time in the absence of any address, data in, or data out strobes, coincident with the rising edge of clock.



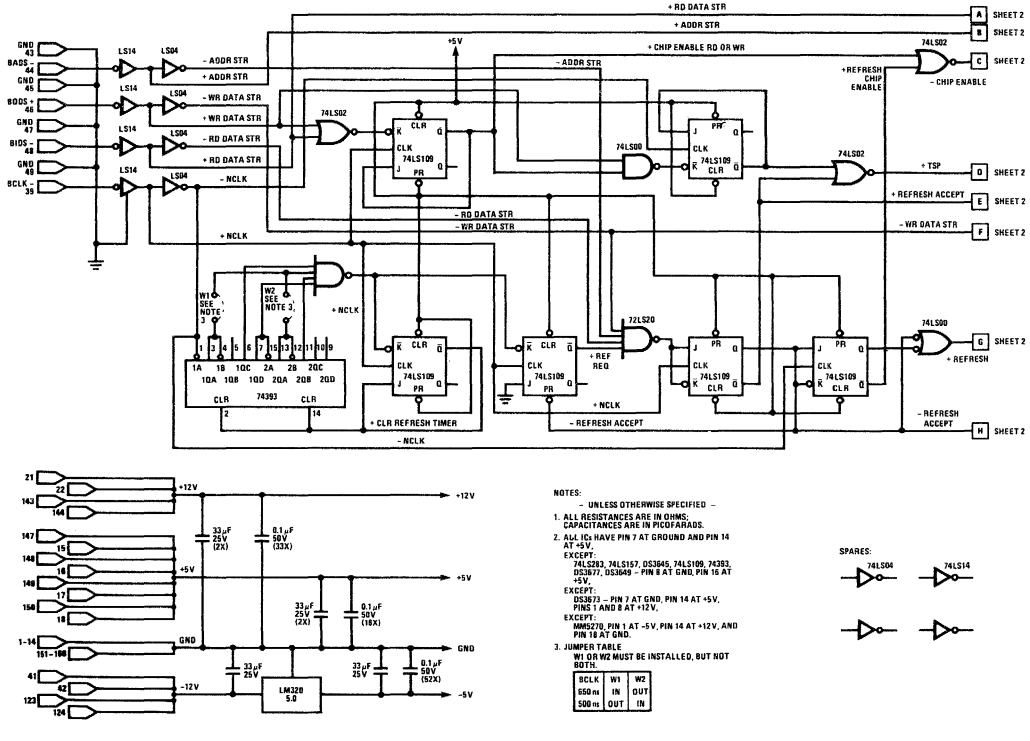


Figure 6. Control Logic, 16 x 8 R/W Memory Board

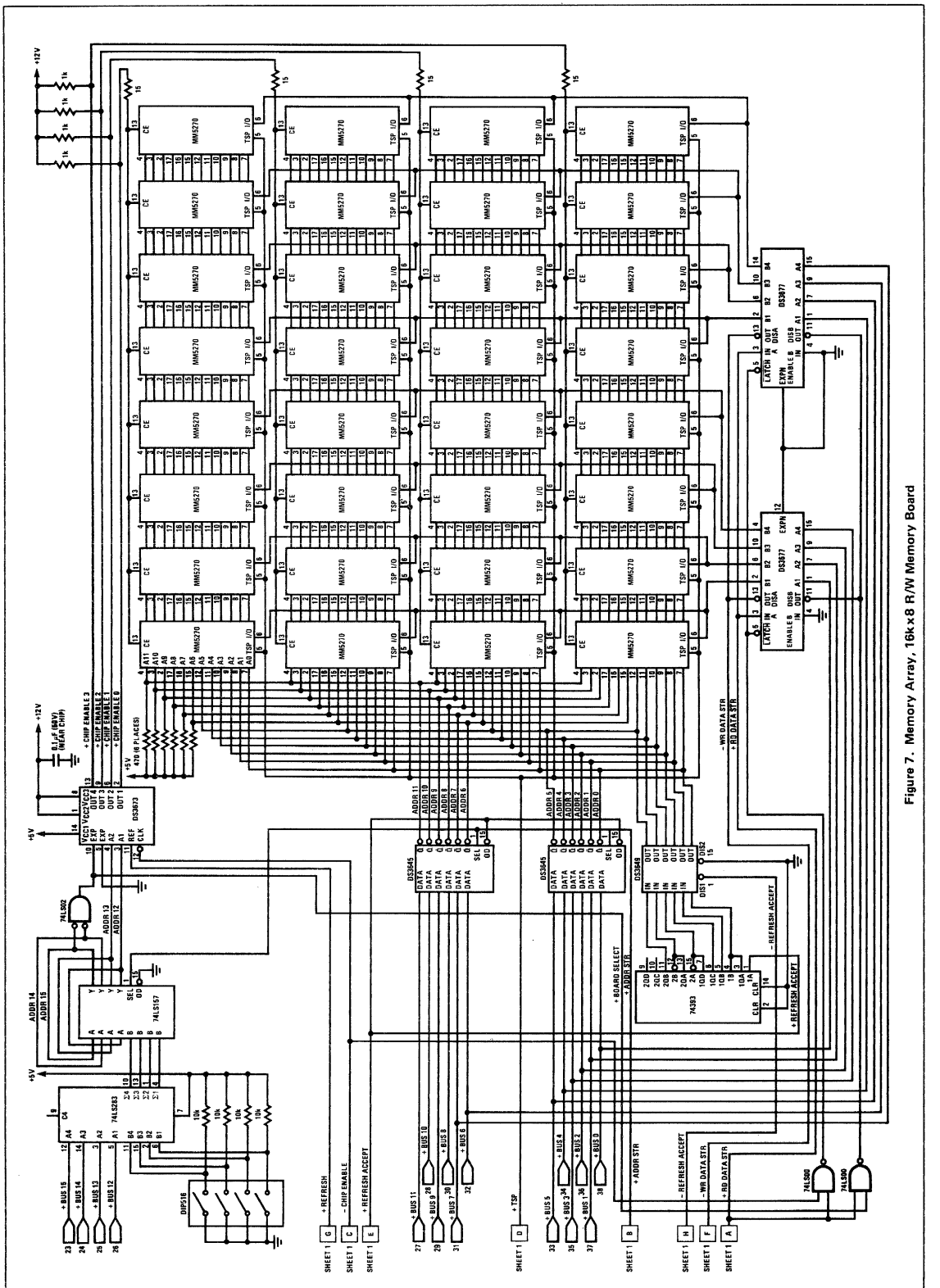
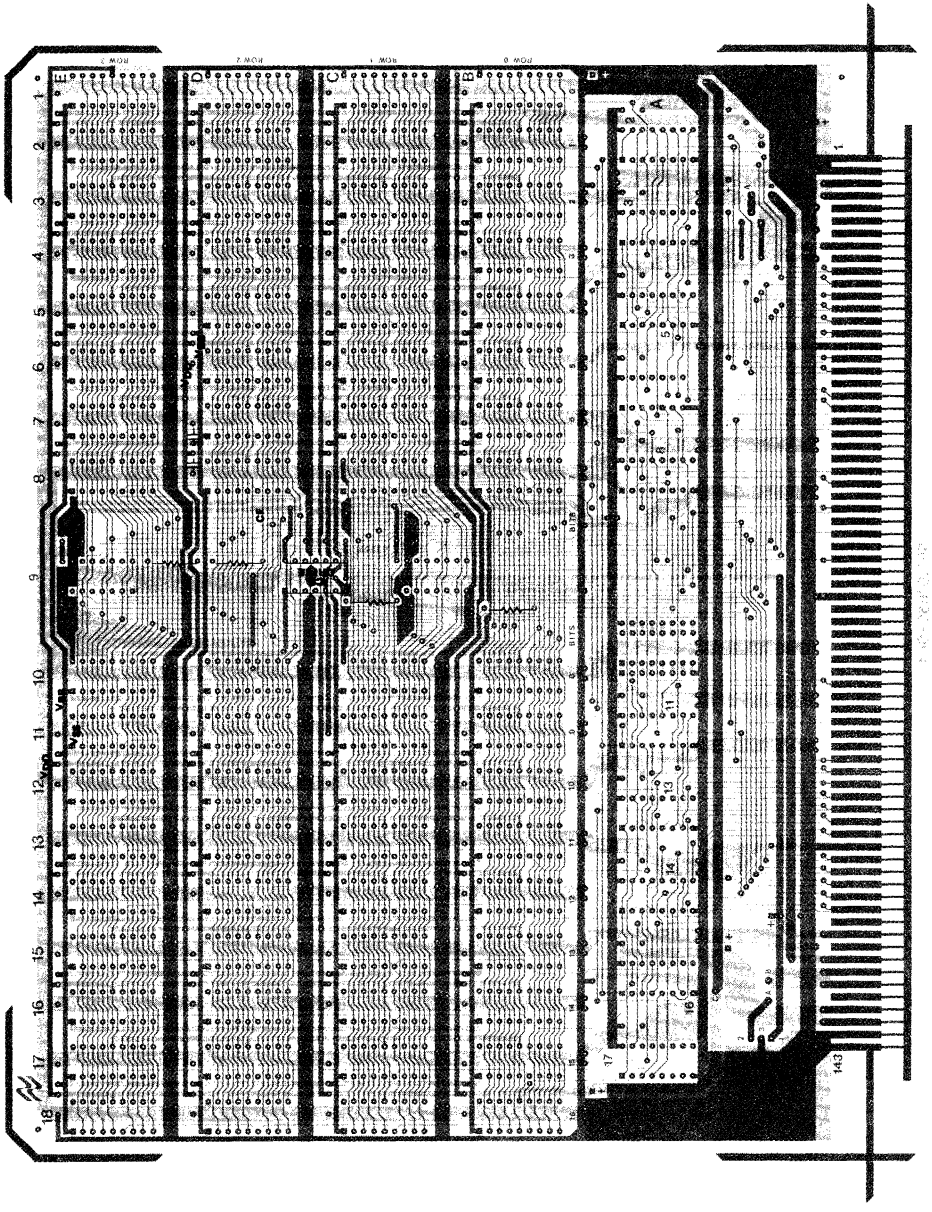


Figure 7. Memory Array, 16k x 8 R/W Memory Board

APPENDIX B

In Appendix B we show the printed circuit board layout for a 16k x 16 RAM board which uses MM5270 18-pin 4k RAMs. It is an excellent example of the proper way to grid and decouple the power supplies on a two-sided board. Also shown are the centrally located chip enable drivers with their series damping resistors.



A Memory Design for an 8080A-Based Microprocessor System

National Semiconductor
Memory Application
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INTRODUCTION

This technical note describes a memory design for a system which can provide up to 64 kilobytes of R/W memory in 16k-byte increments. Provision is made for further address decoding (up to a megabyte). Multiple refresh modes are described, along with handshake signals to and from the CPU. Power supply estimates and parts count are included to allow the reader to get an idea of his own system requirements. Circuit diagrams are also provided.

THEORY OF OPERATION

The design of the memory system can be studied by several blocks in detail. The blocks are identified as follows: (a) the four 16-kilobyte memory banks, the RAM address multiplexer, and the data latch-bus driver/receiver, (b) the timing sequencer section, and (c) the address decoding.

Memory Banks, Address Multiplexer, and Data Bus Element

Memory Banks: There are four memory banks of 16 kilobytes each, made up of eight MM5290 16k-by-1 dynamic memories. The dynamic RAMs require 14 address bits to address any unique location. These addresses are multiplexed over 7 address pins during memory access. Two strobe inputs on the RAMs indicate which 7 bits are on the internal data bus — the 7 row addresses or 7 column addresses. The strobes are Row Address Strobe (RAS) and Column Address Strobe (CAS). A third control input is the write enable signal, WE. There are two data lines: D_{IN} for input and D_{OUT} for output. In this system they are tied together for common I/O, since gating of CAS and WE determines whether data is latched in on D_{IN} or will appear at D_{OUT}. Finally, a ground and three supplies (+12, +5, −5) occupy the other 4 pins.

To provide bank selection within the memory array, 4 different CAS signals are provided, to give effective chip selects.

Address Multiplexer: The addresses to the memory array are selected by the 3242 multiplexer. The 3242 allows the row address (ADR 0 through ADR 6), the column address (ADR 7 through ADR D), or the refresh row address (output of a 7-bit counter internal to the 3242) to be placed on the RAM address bus. The 3242 select controls are derived from the sequencer outputs. In addition, the 3242 has an input to increment its internal refresh row counter. 33 Ω series resistors in the address (WE and CAS) lines serve to limit undershoot on the heavy capacitance lines. This is because MOS RAMs cannot withstand inputs less than −1 volt.

*Refer to Introduction

Data Bus Elements: A pair of quad TRI-STATE® MOS memory I/O registers (DS3647) latch the D_{OUT} outputs from the RAMs for read operations and drive the D_{IN} lines for write operations. They also drive the data bus of the system. The 3647s have TRI-STATE outputs and are inverting in both directions. Control of the 3647s comes from the sequencer. The 3647s are fast (20 ns on memory reads, 15 ns on memory writes), medium power (95 mA), and can source −5.2 mA at 2.4 V_{OUT} and sink 30 mA at 0.4 V_{OUT} when driving the bus. When receiving from the bus, 3647s source 100 μA and sink −500 μA. For 16-bit wide memory systems, one card supplies the lower data byte. A second RAM card handles the upper data byte by jumpering the data lines to edge pins DATA 8/ through DATA F/.

Timing Sequencer

The timing sequencer provides all the appropriate signals for the memory banks for system read/write cycles, refresh cycles to maintain data, and acknowledge handshake signals to bus masters.

An 8224 clock generator supplies a 45.2 ns period clock pulse to drive the sequencer. The 45.2 ns clock, CLK, is divided by 2 by a DM74LS74 flip-flop, which drives two DM74LS161A 4-bit counters. One counter divides CLK by 16 to produce a clock with a 13.02 μs period and 814 ns width. This is the on-card distributed refresh request clock, used to refresh a new row of the memory every 13 μs. The other DM74LS161A driven by CLK÷2 is used for the 8 cycles of refresh required immediately after system power-up. Actually, 9 cycles of refresh are performed. The first one is used to get the sequencer out of any illegal states. When this counter counts up to "1111," the carry output goes high, is inverted, and stops the counter by making Ep (parallel enable) low, inhibiting further counts. During the power-up burst refresh, bus master memory accesses are blocked until the burst refresh is finished.

The sequencer itself is comprised of a pair of J-K flip-flops (DM74S112) and a quad D flip-flop (DM74S175), which form a 14-state ring counter. When START CYCLE (J input to first DM74S112) goes high, ones are clocked through the sequencer in 45.2 ns intervals. The DM74S175 is wired in shift register fashion (Q_1 to D_2, Q_2 to D_3, etc.) to propagate the timing pulses. When T4 goes high (DM74S175 Q_3), the K input of the first DM74S112 goes high. On the next rising edge of CLK, this will cause the sequencer to begin shifting in 0s (count down) until all outputs are 0, at which point the cycle is over. During refresh cycles, the sequencer counts for 450 ns (495 ns max — one clock period uncertainty).

However, during system memory cycles, the sequencer begins to count down 0s immediately after T4 goes high because DT4 (delayed T4) NANDed with RAMREQ (system cycle request) clears the first DM74S112. This allows us to spec memory cycle times of 405 ns (450 ns max).

Outputs of the sequencer drive the CAS/, WE/, CAS0/ through CAS3/, BUSY/, and acknowledge circuitry.

Acknowledge Circuitry

Advanced acknowledge AACK/ is produced by clocking REF/ (high during non-refresh cycles) on a selected edge of the sequencer (T1 for default). A low on RAMREQ/ brings the AACK/ gate out of TRI-STATE.

XACK, Transfer Acknowledge, is the result of REF/ clocked on the T4/ rising edge (the end of T4). It is also gated with AACK to ensure AACK has occurred. To synchronize a pair of memory cards for a 16-bit wide memory word, MACK/ (Memory Acknowledge) is used. The master card sends out MACK/ on the bus to the slave card which uses MACK/ to enable its TRI-STATE XACK/ gate. The slave card is the only card of the pair to send out XACK/. (The bus master does not test for MACK/.)

Request Arbitration Circuitry

This section, consisting of two D flip-flops (DM74S74) and several gates, handles the different cycle requests (bus master, power-up burst refresh, hidden refresh, or 13 μs distributed refresh) and starts the sequencer in its cycles. The circuit handles the five cases of requests and decides which requests will be honored and which will be queued until the system is ready for a new cycle. However, at power-up, 9 cycles of refresh are performed in rapid succession (approximately once every 812 ns) and no bus master requests will be accepted. The total power-up burst refresh time is approximately 9 x 812 + 450 ns, or 7.76 μs.

Another feature of this memory card is to provide true hidden refresh with the INS8080A system. Provisions have been made to indicate M1 cycles of the CPU machine cycles on an auxiliary connector pin. M1 clocked on the rising edge of memory read MRDS/ indicates the 8080 is decoding the current instruction and it will not use the bus for approximately 500 ns to 600 ns. The memory card will then use this time to perform a refresh of its RAM and will be ready for the next bus master memory request. The impact is to eliminate refresh entirely from the picture and the memory will appear static — no refresh delays at all. In the case of bus masters without this M1 output (e.g., DMA cards) the memory still can be refreshed by its on-card requestor circuit.

As mentioned before, two cards can be paired together to produce a 16-bit wide data word memory. The signal MACK/ (memory acknowledge) is used to synchronize the XACK/ (transfer acknowledge) signals between the two cards. To synchronize the refresh of the two cards, three signals are used and brought out to the P2 connector. Through these signals the master card supplies the power-up refresh and distributed refresh to both cards, ensuring a minimum number of wait states to a bus master's request.

Address Decoding

Address bits ADRF/ and ADRE/ are decoded by a DM74S139 2-to-4 decoder and the four outputs are supplied to four wire wrap pin matrices. The matrices assign a base address on 16k boundaries (0000, 4000, 8000, C000) to the CAS/ of each of the four 16k memory banks. (For smaller memory cards, the number of matrices is reduced to the number of memory banks installed; e.g., for 48k, or 3 banks, matrices for banks 1, 2, and 3 would be installed.)

To assign a base address to the bank, the user installs a jumper at the bank and address desired.

The OR of the bank selection is fed to a 4-input NAND gate with the RAM-inhibit signal INH1/, the OR of the memory commands MRDS/ and MWTC/, and a signal from the optional megabyte decoder. This NAND output is called RAMREQ/ and generates Board Write and Board Read with the memory commands. RAMREQ/ is also inverted and applied to the memory cycle request arbitration circuit described earlier.

Table I. Memory Request Arbitration Conditions

Request	Current Cycle	Action
Bus Master Cycle	None	Begin Bus Master Cycle
Bus Master Cycle	Refresh	Complete Refresh Cycle, then begin Bus Master Cycle
Refresh Cycle	None	Begin Refresh Cycle
Refresh Cycle	Bus Master Cycle	Complete Bus Master Cycle, then begin Refresh Cycle
Refresh Cycle and Bus Master Cycle	None	Accept Bus Master Cycle, begin Refresh Cycle after Bus Master Cycle goes to completion

Table II. Power Supply Requirements (estimate)

Card Size	I_{CC} (+5)	I_{BB} (−5)	I_{DD} (+12)
64k RAM	1.5 A	0.0064 A	0.94 A
48k RAM	0.82 A	0.0048 A	0.73 A
32k RAM	0.74 A	0.0032 A	0.51 A
16k RAM	0.66 A	0.0016 A	0.29 A

Table III. Parts Count

Card Size	Memory Chips	Support	Total
64k	32	30	62
48k	24	28	52
32k	16	28	44
16k	8	28	36

Megabyte Decoder

This circuit decodes four more address bits – ADR13/ through ADR10/ – via an 8-bit data selector. These address bits are derived from the P1 spares (main connector) and the P2 (auxiliary connector). This decoder output is true if the lower 3 bits (10 through 12) match the switch array (one switch is opened) and if the highest bit (13) or its complement causes the DM74LS151 STROBE to go low. The decoder output goes to the RAMREQ/ gate.

Parts Count and Power Supply Requirements

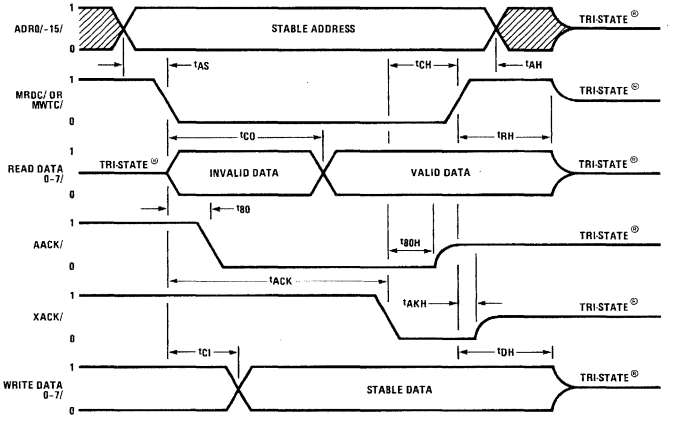
The parts count (estimated) is shown in table III. Power supply requirements are shown in table II.

DC Specifications

Signal		Parameter	Conditions		Min	Max	Units
DATA0/-DATA7/	$V_{IN(1)}$	Input Voltage Logic 1			2.0		V
	$V_{IN(0)}$	Input Voltage Logic 0				0.8	V
	$I_{IN(1)}$	Input Current Logic 1				100	μA
	$I_{IN(0)}$	Input Current Logic 0				-500	μA
	$V_{OUT(1)}$	Output Voltage Logic 1	V_{CC} = 5V	$I_{OUT(1)}$ = -5.2mA	3.0		V
	$V_{OUT(0)}$	Output Voltage Logic 0	V_{CC} = 4.5V	$I_{OUT(0)}$ = 30mA		0.4	V
	$I_{OUT(1)}$	Output Current Logic 1	V_{CC} = 5V	$V_{OUT(1)}$ = 3.0V		-5.2	mA
	$I_{OUT(0)}$	Output Current Logic 0	V_{CC} = 4.5V	$V_{OUT(0)}$ = 0.4V		30	mA
ADR0/-ADRF/, MWTC/, MRDC/, ADR10/-ADR13/	$V_{IN(1)}$	Input Voltage Logic 1			-2.0		V
	$V_{IN(0)}$	Input Voltage Logic 0				0.8	V
	$I_{IN(1)}$	Input Current Logic 1	V_{CC} = max	$V_{IN(1)}$ = 2.7V		50	μA
	$I_{IN(0)}$	Input Current Logic 0	V_{CC} = max	$V_{IN(0)}$ = 0.5V		-2	mA
AACK/, XACK/	$V_{OUT(1)}$	Output Voltage Logic 1	V_{CC} = min	$I_{OUT(1)}$ = -5.2mA	2.4		V
	$V_{OUT(0)}$	Output Voltage Logic 0	V_{CC} = min	$I_{OUT(0)}$ = 16mA		0.4	V
	$I_{OUT(1)}$	Output Current Logic 1				-5.2	mA
	$I_{OUT(0)}$	Output Current Logic 0	V_{CC} = min	$V_{OUT(0)}$ = 0.4V		16	mA
MACK/ W17 B-D	$V_{IN(1)}$	Input Voltage Logic 1			2		V
	$V_{IN(0)}$	Input Voltage Logic 0				0.8	V
	$I_{IN(1)}$	Input Current Logic 1	V_{CC} = max	$V_{IN(1)}$ = 2.4V		40	μA
	$I_{IN(0)}$	Input Current Logic 0	V_{CC} = max	$V_{IN(0)}$ = 0.4V		-1.6	mA
MACK/ W17 A-C	$V_{OUT(1)}$	Output Voltage Logic 1	V_{CC} = min	$I_{OUT(1)}$ = -400μA	2.7		V
	$V_{OUT(0)}$	Output Voltage Logic 0	V_{CC} = min	$I_{OUT(0)}$ = 8mA		0.5	V
	$I_{OUT(1)}$	Output Current Logic 1	V_{CC} = min	$V_{OUT(1)}$ = 2.7V		-400	μA
	$I_{OUT(0)}$	Output Current Logic 0	V_{CC} = min	$V_{OUT(0)}$ = 0.5V		8	mA
INH1/	$V_{IN(1)}$	Input Voltage Logic 1			2.0		V
	$V_{IN(0)}$	Input Voltage Logic 0				0.8	V
	$I_{IN(1)}$	Output Voltage Logic 1	V_{CC} = 5.5V	$V_{IN(1)}$ = 2.7V*		50	μA
	$I_{IN(0)}$	Output Volgage Logic 0	V_{CC} = 5.5V	$V_{IN(0)}$ = 0.5V*		-2.58	μA

*includes 10k pull-up

Timing Waveforms

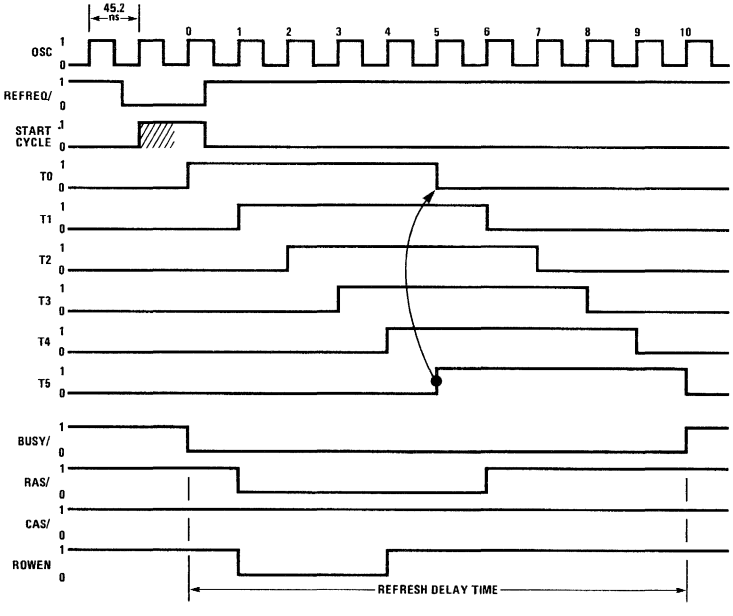


Bus Characteristics (AC)

AC Specifications (refer to figure 1)

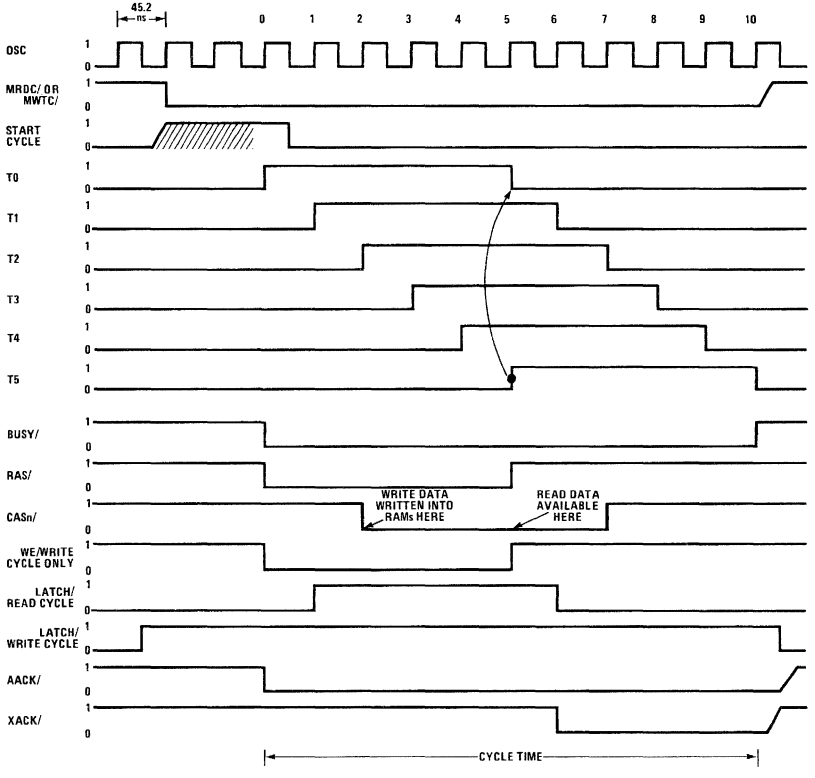
Parameter	Min (ns)	Max (ns)	Description	Remarks
t_{AS}	50		Address Setup to Command	
t_{AH}	0		Address Hold from Command	
t_{CH}	0		Command Hold from XACK/	
t_{CO}		375	Command to Read Data Access Time	
t_{RCY}, t_{WCY}	455	565	Read Cycle Time	
t_{80}	50	210	Command to AACK/	for W18 B-H
t_{ACK}	280	440	Command to XACK/	for W17 A-B
t_{CI}		90	Command to Write Data Setup Time	
t_{DH}	0		Write Data Hold Time from Command	
t_{AKH}	0	85	End of Command to Hi-Z on XACK/	
t_{80H}	0	36	End of Command to Hi-Z on AACK/	
t_{RD}	0	550	Refresh Delay Time	Since Refresh is asynchronous, t_{RD} may be added to t_{CO}, t_{RCY}, t_{AAK}, t_{ACK}.
t_{RH}	0	55	End of Command to Data Buffers go Hi-Z	
t_{A80}	0	30	AACK/ Off Time from Bus Ack	

Timing Waveforms (Continued)

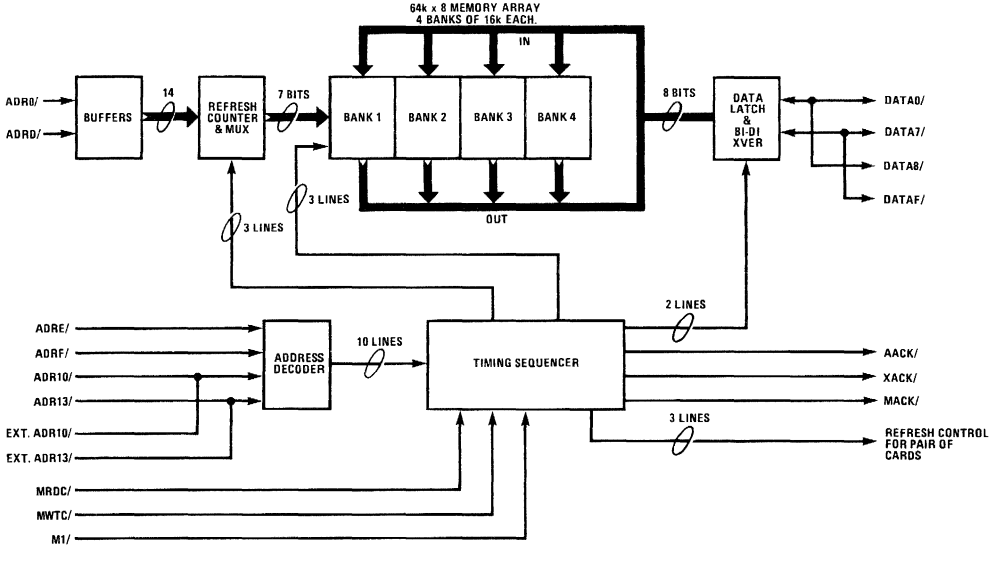


Sequence of Events, Refresh Cycle

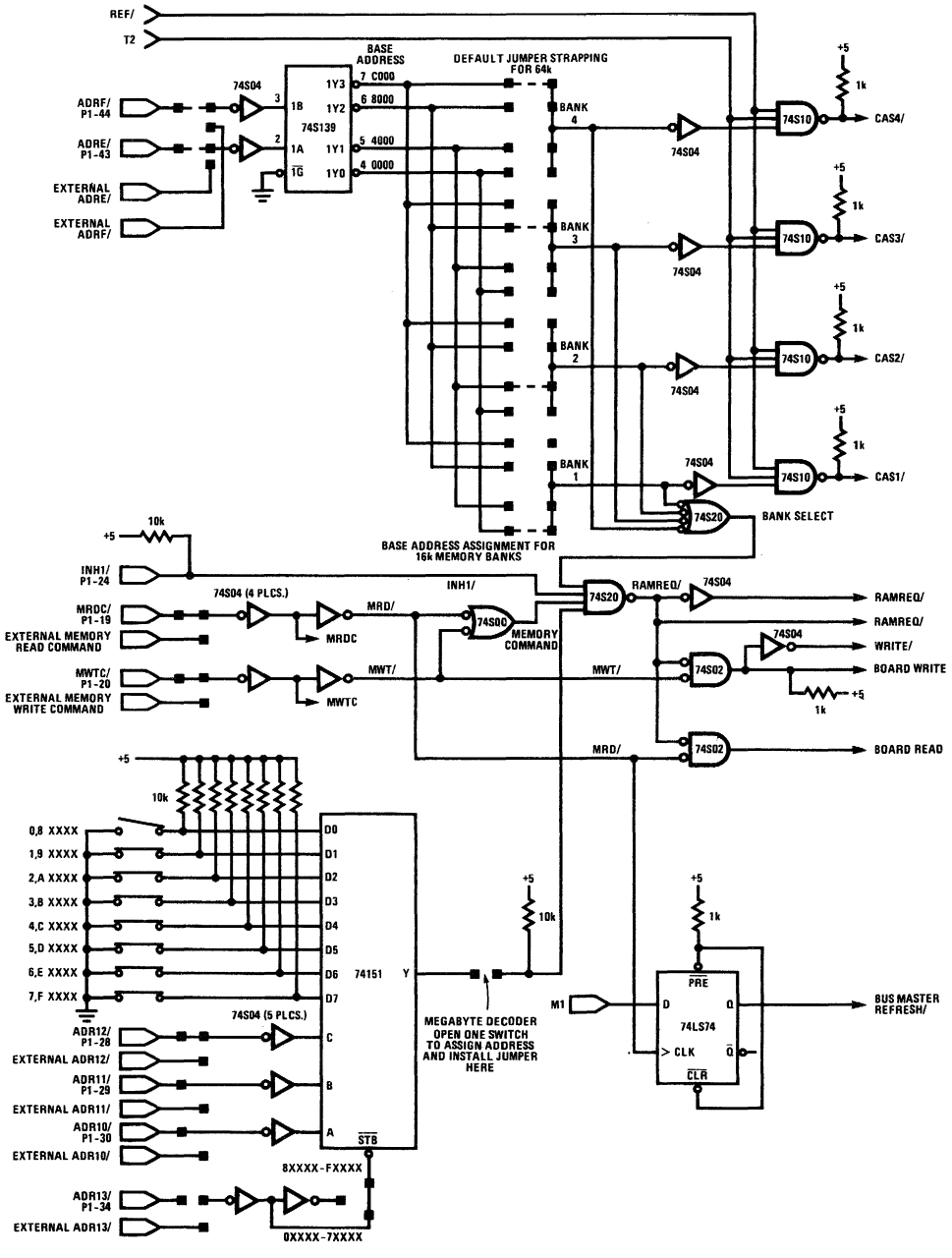
Timing Waveforms (Continued)



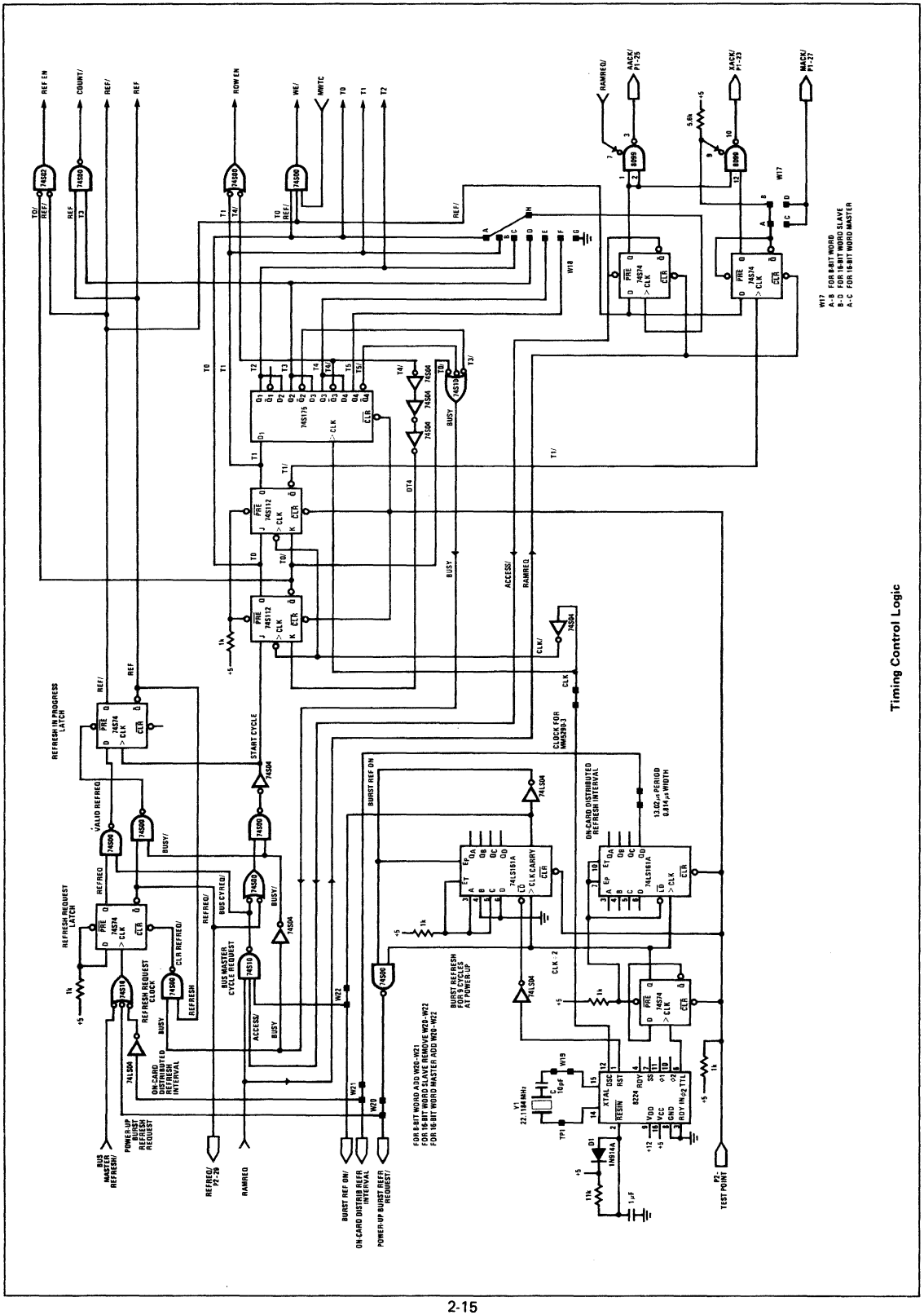
Sequence of Events, Read or Write Cycle



Block Diagram

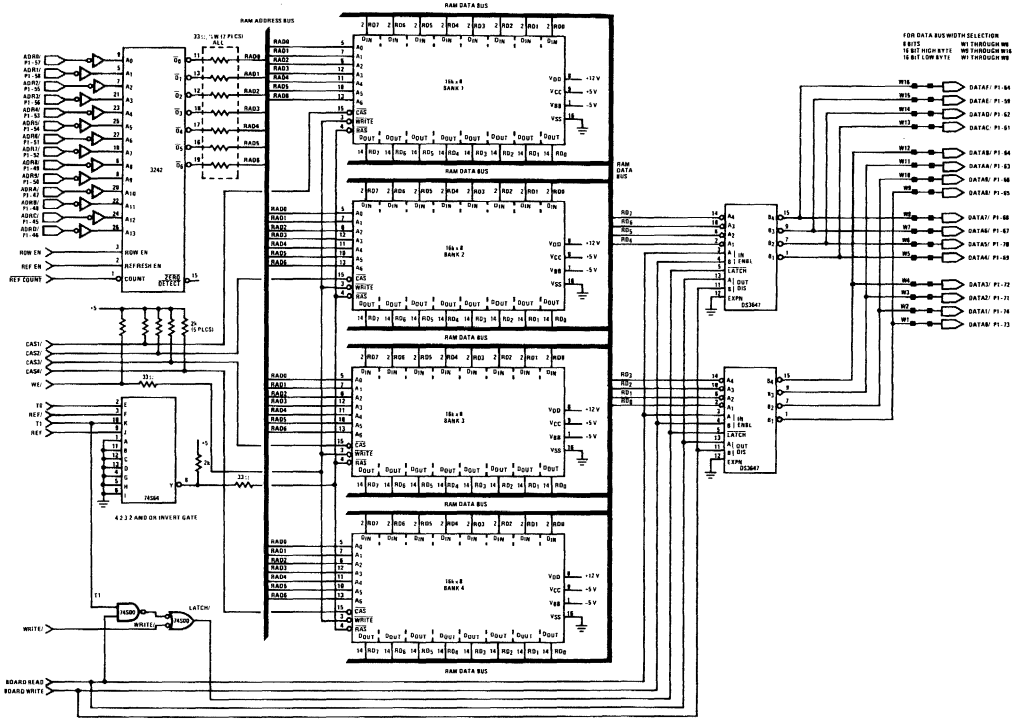


Memory Select Logic



Timing Control Logic

2



Memory Array

MM5290 16K RAM Functional Description

National Semiconductor
B. Johnston

INTRODUCTION

This functional description covers the operation of the MM5290 16k dynamic RAM currently manufactured by National Semiconductor. This device is directly interchangeable with the MK4116. The National design has some internal differences, but these are transparent to the user, making the MM5290 a direct replacement for the MK4116.

Block Diagram

The block diagram shown in *Figure 1* shows the functional relationship between major blocks of circuitry in the MM5290. The multiplexed address, unlatched output and gated $\overline{CAS}$ features are shown. The row decoder column decoders and two 64 x 128 memory arrays with sense amplifiers between them are drawn in blocks that indicate their actual physical relationship on the die. This arrangement, with sense amplifiers in the middle and column decoders duplicated along each side, reduces cross talk (coupled noise) between address and column lines. Noise margin is improved because column line length is minimized.

Clock Generation

The MM5290 has multiplexed addressing necessitating separate row (Row Address Strobe, $\overline{RAS}$) and column (Column Address Strobe, $\overline{CAS}$) strobes. The timing relationship between these two strobes is made non-critical by gating $\overline{CAS}$ with the internal $\overline{RAS}$ clock. This is shown in *Figure 1*, along with the fact that $\overline{CAS}$ gates the write enable ($\overline{WE}$) control. These three signals are the source of the internal clocks (row, column and write clocks). Another way to describe this is: 1) the row clocks are referenced to $\overline{RAS}$; 2) the column clocks are referenced to either $\overline{RAS}$ or $\overline{CAS}$, depending on the $\overline{RAS}$ to $\overline{CAS}$ delay; and 3) the write clocks are referenced to $\overline{CAS}$ or $\overline{WE}$, depending on which occurs later. The block diagram in *Figure 1* indicates which blocks of circuitry the internal clocks control.

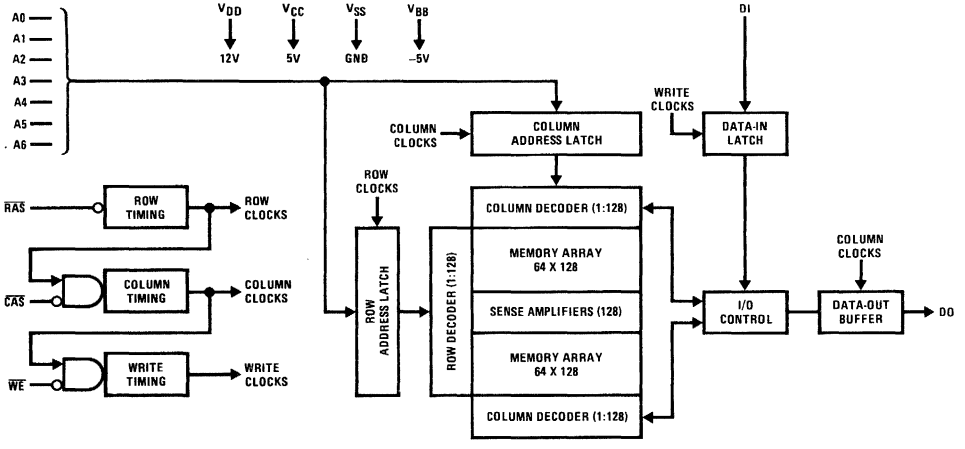


FIGURE 1. MM5290 Block Diagram

Memory Cell

The basic memory cell consists of a transistor and capacitor as shown in *Figure 2*. Data is stored by selecting a cell and charging or discharging the storage capacitor C_S through transistor Q1. Q1 is then turned OFF (cell deselected) and data is retained until charge is lost through leakage current or the cell is refreshed. Each memory cell must be refreshed every 2 ms to guarantee data retention.

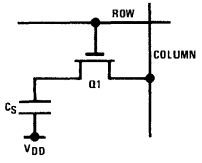


FIGURE 2. Basic Memory Cell

Cell Selection

Figure 3 shows a block diagram indicating how an individual memory cell is selected (addressed). First, the row address is latched in by $\overline{RAS}$. This is decoded to select 1 out of the 128 rows. Actually, there are 128 cells tied to each row so that 128 cell transistors (Q1 in *Figure 3*) are turned ON. Second, the column address is latched in. This is decoded to select 1 of the 128 columns. The row and column coincidence selects an individual cell for either reading or writing data.

Read Operation

Figure 4 shows a simplified version of the array of cells with the read/write circuitry. The array consists of 16,384 memory cells plus 2 rows of 128 reference cells. These are separated into 2 arrays by 128 sense amplifiers as shown. If row address AX5 is a logic "0", a row in the top half of the memory is being selected while the reference cells on the other side of the sense amplifier are also selected. Data is stored in complementary form in this half (top) of the array. The other half (bottom) of the array stores the data in true form when row address AX5 is a logic "1". A logic "0" in the array is defined as 0V stored in the cell and a logic "1" as +V.

Although the usual time reference in a cycle of operation is the high-to-low transition of $\overline{RAS}$, the prior events of discharging all row lines (to 0V) and precharging all column lines (to V_{DD}) must occur before a cycle of operation can be successfully completed. The starting point then is all row lines discharged and all column lines precharged. Then a row address is latched and the 128 cells connected to the selected row line are "read" by the 128 sense amplifiers. This also refreshes them. When a column address is latched, 1 of the 128 columns is connected to the I/O bus and the data of the selected cell becomes available on the DO pin.

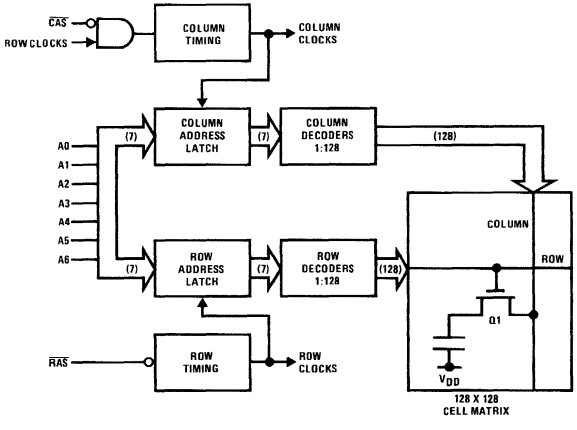


FIGURE 3. Block Diagram of Cell Selection

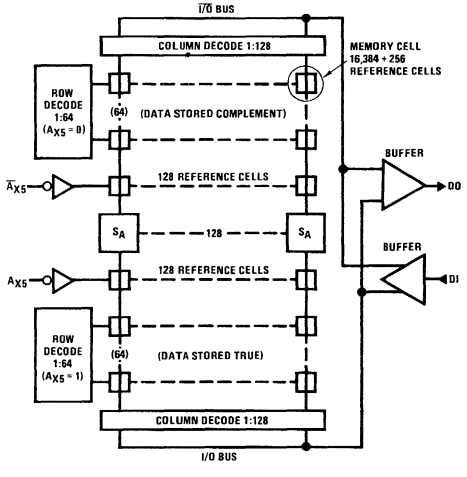


FIGURE 4. Simplified Read-Write Circuitry

Sense Amplifier Operation

Figure 5 shows a simplified version of a sense amplifier together with a selected memory cell and the reference cell associated with "reading" the cell. When the cell is selected by the row address, a reference cell on the opposite side of the differential sense amplifier is also selected. (In fact, the entire row of 128 reference cells is selected.) If the selected memory cell contains a "1", then the storage capacitor C_S has the same potential as the left column line and no charge is transferred through Q1. If the selected cell contains a "0", then charge will be transferred through Q1 and shared between C_S and C_{CL}. The voltage of the column line will be reduced by ΔV where ΔV is a function of the ratio of C_S to C_{CL}.

Simultaneously with the events happening with the memory cell and the left column line, the right column line will always be reduced by 1/2 ΔV because charge will be transferred through Q2 between the capacitor of the reference cell labeled 1/2 C_S and C_{CL}. (All reference cells begin the cycle with a "0" stored on the storage capacitor.) This means that the sense amplifier will have a voltage difference of $\pm 1/2\ \Delta V$ across it with the polarity depending on the data stored in the memory cell. The sense amplifier regeneratively amplifies the difference and restores the data in the memory cell. This signal is also amplified by the output buffer and made available at the output pin (DO).

Write Operation

Figure 6 shows a block diagram of the write circuitry. The Data In buffer drives the column line of the selected cell either low (to ground) or high (to V_{DD}) depending on the logic level of DI. Transistor Q1 is ON because the cell has been selected and the storage capacitor C_S is written to the voltage of the column line. Then Q1 is turned OFF and C_S retains the data.

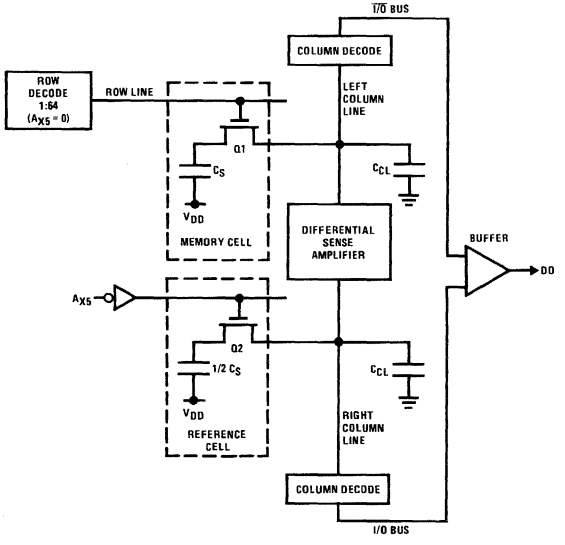


FIGURE 5. Simplified Read Circuitry

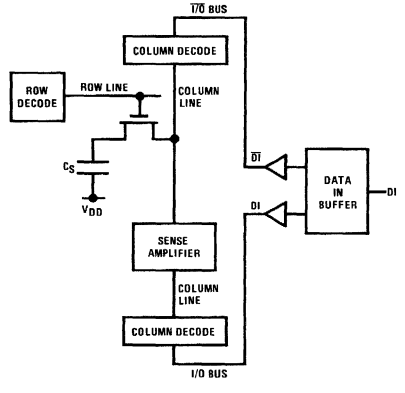


FIGURE 6. Simplified Write Circuitry

Refresh

One side of the storage capacitor of the memory cell is a polysilicon V_{DD} line. The other side is a diffused junction (the drain of a transistor). The leakage of this junction normally increases with temperature and limits the data retention. This "dynamic" nature of the data storage requires that the cells be refreshed periodically (every 2 ms with today's technology) to retain data. A row of cells (128) is refreshed whenever any valid $\overline{RAS}$ cycle occurs. This means it takes 128 cycles to refresh the MM5290. Operating power is reduced and the output kept in the high impedance state when $\overline{CAS}$ is kept high and $\overline{RAS}$ is cycled for each of the 128 row addresses ($\overline{RAS}$ Only Refresh) to refresh the memory.

Most of the circuitry used in the MM5290 is dynamic and must also be "refreshed" for the memory to function properly. This is accomplished automatically when the dynamic cells are refreshed. This dynamic circuitry requires several cycles after power-up or after the refresh limit has been exceeded before proper device operation can be assured.

Read Timing

The read cycle timing is indicated in *Figure 7*. The cycle begins with $\overline{RAS}$ going low. This latches the row address. The address bus must be stable at this time: $\overline{CAS}$ then switches low sometime later. Again the address bus must be stable at the time $\overline{CAS}$ goes low because the column address is latched at that time. $\overline{WE}$ must be high coincidentally with $\overline{CAS}$ low during the read cycle. Data Out (DO) will be valid before t_{CAC} (access time from $\overline{CAS}$) or t_{RAC} (access time from $\overline{RAS}$) whichever is limiting. The output will return to TRI-STATE® in t_{OFF} time when $\overline{CAS}$ switches high. The valid data can be maintained to the end of the cycle (in fact, into the next cycle) because t_{CRP} minimum ($\overline{CAS}$ to $\overline{RAS}$ precharge time) is specified as a negative quantity in the data sheet.

Write Timing

There are 3 types of write cycles specified in the data sheet. These are called an Early Write, a Read-Write and a Read-Modify-Write cycle.

The Early Write cycle is characterized by $\overline{WE}$ going low no later than t_{WCS} minimum ($\overline{WE}$ to $\overline{CAS}$ set-up time) before $\overline{CAS}$. This could be called a "write only" cycle. The output remains in the high impedance state throughout the cycle while data is written into the desired location *(Figure 8a)*. D_{IN} is latched when $\overline{CAS}$ goes low and must be stable then rather than being referenced to $\overline{WE}$. The $\overline{WE}$ pulse width must be a minimum of t_{WP} and both the leading and trailing edges of $\overline{WE}$ have several timing constraints with respect to $\overline{RAS}$ and $\overline{CAS}$. Refer to the data sheet for these specifications.

The Read-Write cycle *(Figure 8b)* occurs when $\overline{WE}$ is delayed for at least t_{RWD} minimum ($\overline{RAS}$ to $\overline{WE}$ Delay) from $\overline{RAS}$ and the t_{CWD} minimum ($\overline{CAS}$ to $\overline{WE}$ Delay) from $\overline{CAS}$. The data in the selected location is first read; then new data is written into the location. The read portion of the cycle is explained in the section on Read Cycle Timing. The write portion of the cycle begins with data being latched in when $\overline{WE}$ falls and ends with the end of the cycle. The detailed timing is shown in the data sheet.

The Read-Modify-Write cycle *(Figure 8c)* is the Read-Write cycle extended in time so that the data in a particular location can be read, modified if necessary, and then written back into the same location. This requires that the $\overline{WE}$ pulse be delayed the minimum time of t_{RWD} from $\overline{RAS}$ and t_{CWD} from $\overline{CAS}$ plus an additional time shown as t_{MOD}. The additional time is the time required by the system to check the data, modify it as necessary and place it on the input data bus consistent with the required set-up time before $\overline{WE}$ goes low. Note that t_{MOD} is a system parameter. Detailed timing is given in the data sheet.

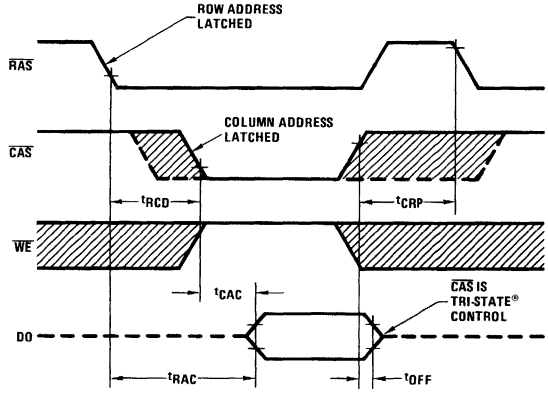


FIGURE 7. Read Cycle

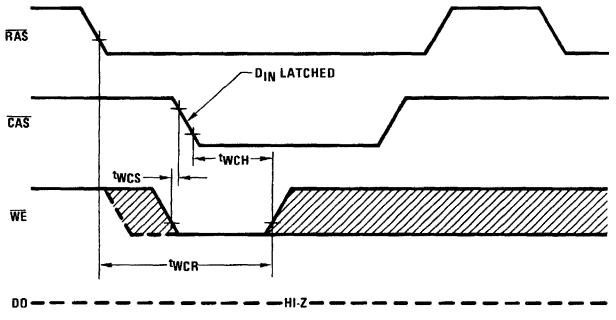


FIGURE 8a. Early Write

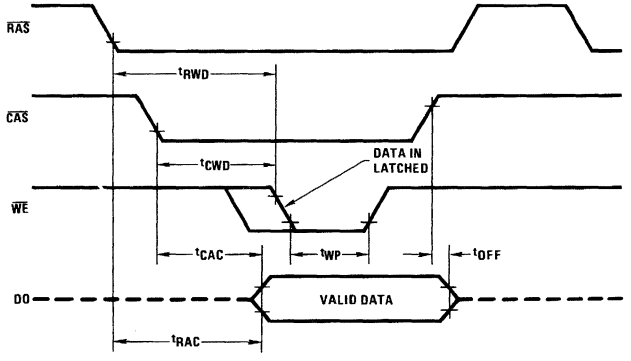


FIGURE 8b. Read-Write

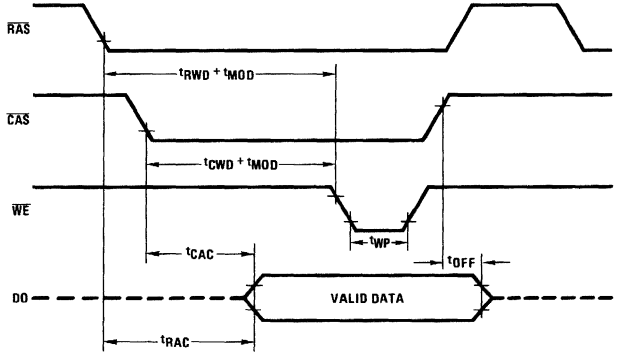


FIGURE 8c. Read-Modify-Write

Page Mode Timing

The MM5290 functions in a page mode operation with up to 128 bits (1 row) per page. Data may be read or written in this mode of operation.

Figure 9 shows the timing for a page mode Read cycle. The cycle starts like a normal read cycle with the access time of the first bit (bit 0) either t_{RAC} or t_{CAC} whichever is limiting. The rest of the page mode read is accomplished by keeping $\overline{RAS}$ low and cycling $\overline{CAS}$ an additional 127 times while changing to a new column address each time. $\overline{WE}$ may be held high continuously or cycled. If $\overline{WE}$ is cycled, it must meet the timing constraints shown in the data sheet. $\overline{RAS}$ cannot be held low for more than 32 μs so that the maximum $\overline{CAS}$ cycle time is approximately 250 ns to read the full 128 bits of data in a page (row).

Figure 10a shows the timing for a page mode Early Write cycle. The cycle begins as a normal early write cycle. The rest of this mode of operation is accomplished by keeping $\overline{RAS}$ low and cycling $\overline{CAS}$ an additional 127 times while changing to a new column address each time. The input data (D_{IN}) must be referenced to the falling edge of $\overline{CAS}$ and not $\overline{WE}$. $\overline{WE}$ may be held low or pulsed. The output will remain in the high impedance state throughout the cycle.

Figure 10b shows the timing for a page mode Read-Write cycle. The cycle begins as a normal read-write cycle. Then $\overline{RAS}$ is held low and $\overline{CAS}$ is cycled an additional 127 times while a new column address is selected each time. $\overline{WE}$ must be kept high for the t_{CWD} time (to guarantee the data is read) and then switched low for t_{WP} time to accomplish writing the new data. The data to be entered (D_{IN}) must be referenced to $\overline{WE}$ with the appropriate set-up and hold times shown in the data sheet. Extending the t_{CWD} time to allow for modifying data and then writing it back into the same location would make this a Read-Modify-Write page mode cycle.

Refresh Timing

The MM5290 must be refreshed every 2 ms. Any valid cycle of $\overline{RAS}$ will refresh a row of 128 bits. It requires 128 cycles, (1 for each row of the matrix) to refresh the entire memory. *Figure 11* shows $\overline{RAS}$ only refresh. Only $\overline{RAS}$ switches. $\overline{CAS}$ is held high which reduces I_{DD} and TRI-STATES the output.

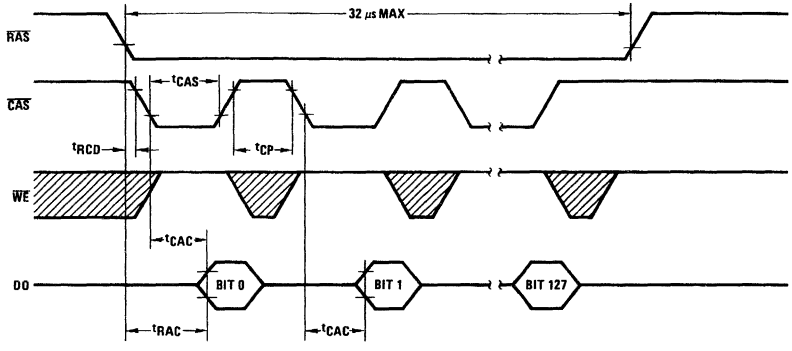


FIGURE 9. Page Mode Read Cycle

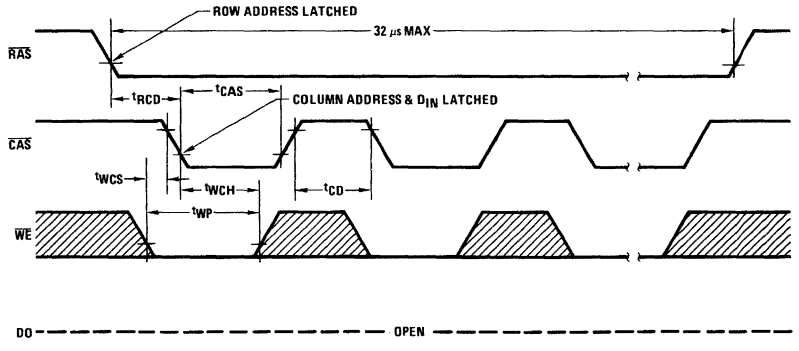


FIGURE 10a. Page Mode Early Write Cycle

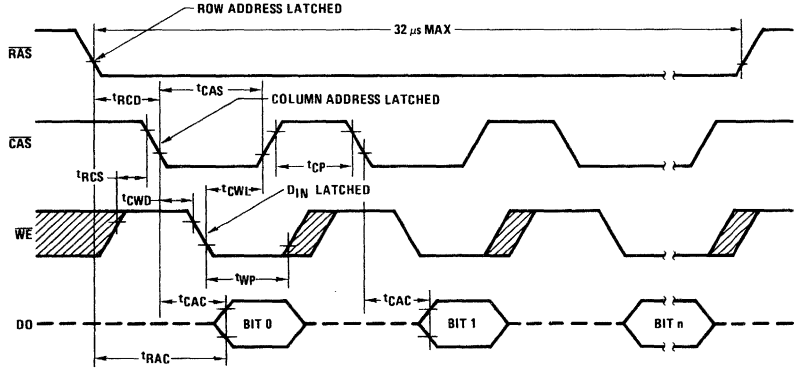


FIGURE 10b. Page Mode Read-Write Cycle

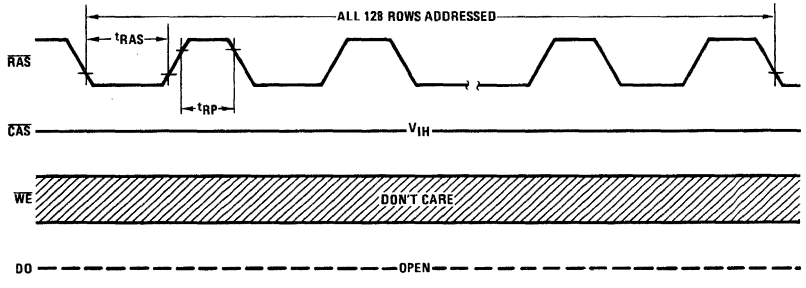
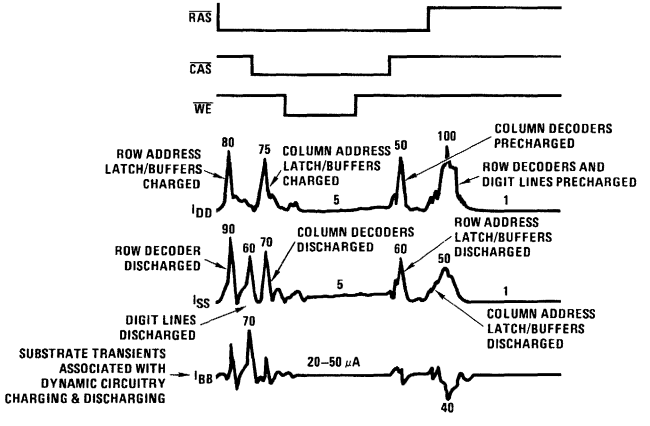


FIGURE 11. $\overline{RAS}$ Only Refresh Cycle

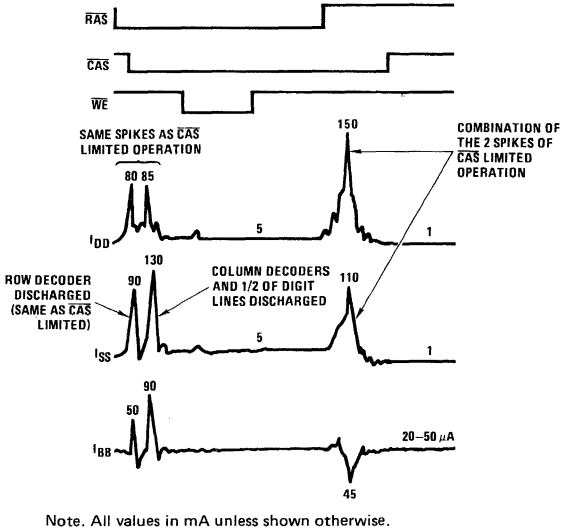
Current Transients

Figures 12 and 13 show the current waveforms for I_{DD}, I_{SS} and I_{BB}. When the MM5290 is operated with $\overline{CAS}$ limited timing, the transients associated with the row and column clocks are separated in time. The major events causing the transients are indicated in *Figure 12*. When the operation is $\overline{RAS}$ limited, some of the transients overlap. This is shown in *Figure 13*. The transients are then additive and maximum transient peaks occur. Adequate capacitive decoupling* at the board level is necessary to maintain power supply voltage transients within the data sheet specification of ±10%.



Note. All values in mA unless shown otherwise.

FIGURE 12. $\overline{CAS}$ Limited Timing Transients



Note. All values in mA unless shown otherwise.

FIGURE 13. $\overline{RAS}$ Limited Timing Transients

*Refer to "Dynamic RAM Board Design Made Easy"

Trouble Shooting Check List For Memory Systems Using the MM5290

1. Are all power supplies within spec, including spikes, at all points on the card?
   - V_{DD} = 12.0V ± 10%? ☐ Properly decoupled? ☐
   - V_{CC} = 5.0V ± 10%? ☐ Properly decoupled? ☐
   - V_{BB} = −5.0V ± 10%? ☐ Properly decoupled? ☐

2. Are there at least 8 legal RAS cycles after power-up before the memory is used? ☐

3. Are the input high and low levels within spec?
   - $V_{IHC} \geq 2.7V$ for $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$? ☐
   - $V_{IH} \geq 2.4V$ for A_0-A_6, DI? ☐
   - $V_{IL} \leq 0.8V$ for all inputs? ☐

4. Are the transition times for the input signals within spec? ☐
   Has the ringing been damped by a series resistor where necessary? ☐

5. Is DO load within spec (I_{OH} = −5.0 mA max., I_{OL} = 4.2 mA max.)? ☐

6. Are clock pulse widths and precharge times OK?
   - $\overline{RAS}$ pulse width? ☐ $\overline{RAS}$ precharge time? ☐
   - $\overline{CAS}$ pulse width? ☐ $\overline{CAS}$ precharge time? ☐
   - $\overline{WE}$ pulse width? ☐

7. Is timing $\overline{RAS}$-limited ($t_{RCD} \leq t_{RCD}$ max.)? ☐
   or $\overline{CAS}$-limited ($t_{RCD} > t_{RCD}$ max.)? ☐

8. Are all address set-up and hold times within spec?
   - t_{ASR} and t_{RAH} for the row address? ☐
   - t_{ASC} and t_{CAH} ($\overline{CAS}$ limited timing) or t_{AR} ($\overline{RAS}$ limited timing) } for the column address? ☐

9. Are the $\overline{WE}$ set-up and hold times within spec?
   - t_{RCS} and t_{RCH} for a read cycle? ☐
   - t_{RWL} and t_{CWL}, t_{WCH} ($\overline{CAS}$ limited timing) or t_{WCR} ($\overline{RAS}$ limited timing) } for a write cycle? ☐
   - t_{WCS} for an early-write cycle? ☐
   - t_{CWD} ($\overline{CAS}$ limited timing) or t_{RWD} ($\overline{RAS}$ limited timing) } for a read-write or a read-modify-write cycle? ☐

10. Are the DI set-up and hold times within spec?
    - t_{DS} and t_{DH} relative to later of $\overline{CAS}$ or $\overline{WE}$ or t_{DHR} relative to $\overline{RAS}$ for $\overline{RAS}$ limited timing. } ☐

MM5290 Bit Map and Address Decoding

INTRODUCTION

Disturb testing requires a detailed knowledge of the topology and address decoding of a dynamic RAM. The MM5290 has its own unique topology and address decoding which is described in this write-up.

Figure 1 shows the MM5290 cell array diagram. It is oriented with a top view, as if a die were in a dual-in-line package, with pin 1 in the upper left hand corner. In this orientation the row decoders are across the bottom and the column decoders are along the sides. (Actually the column decoders are duplicated on each side.)

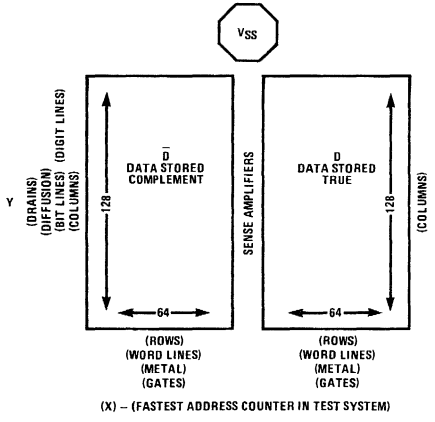


Figure 1. MM5290 Cell Array Diagram

Terminology is listed for those of us who may be confused by vertical rows, horizontal columns, bit lines, word lines, etc., so that definitions are clear. The terms "row" and "column" will be used from now on in this paper. X and Y address counter definitions are shown also. Note that even though the data out is not inverted from a user's point of view, the data is stored in complementary form in the left cell array.

Figure 2 shows the address decoding. This is shown with the cells indicated in a regular array. This is not the case and the actual topology will be discussed later. The assumptions are:

1. This is the same orientation as in figure 1.
2. One chooses the lower left hand corner of the array as the starting reference.
3. The row address counter is the faster of the two address counters providing the binary addresses.
4. The leads are translated on the test fixture as shown in figure 3.
5. The cells may be numbered in decimal from 0 to 16,383 and the numbers of the cell correspond to the binary format as shown in figure 4.

Based on these assumptions, figure 2 shows the position of the cells addressed by stepping through the binary addresses in sequence, rows fast. Several cells are numbered in figure 2 to indicate the sequence. Another way to show the address decoder translation is shown in figure 5. The row address counter counts 4 left to right (arrow a); then during the next 4 counts the

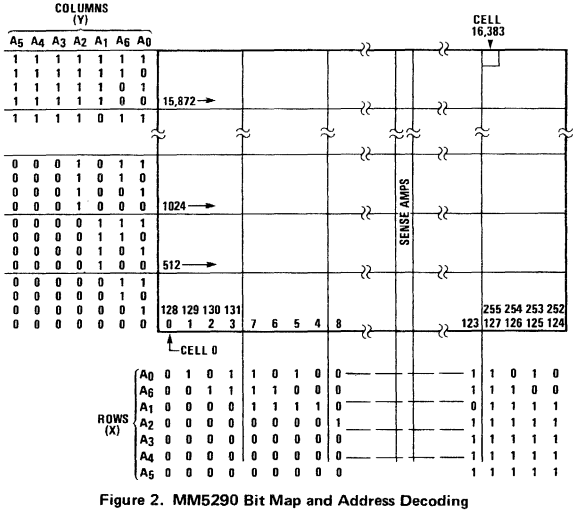


Figure 2. MM5290 Bit Map and Address Decoding

physical connections make it address cells from right to left (arrow b). This left-to-right, right-to-left sequence (in groups of 4) is repeated for 128 rows. The column address counters count in normal sequence starting with 0 at the bottom and up through 127 at the top. If the column address counter increments once for each 128 row count, then all cells of the array are addressed as follows: Column 0 is addressed (in the 4 left-to-right, then 4 right-to-left sequence), then column 1 and on to column 127, where the number of the column corresponds to the decimal equivalent of the binary column address.

Now that we can "follow the map" to any cell location, there is one more step to determine which cells are physically adjacent (as opposed to having sequential or "adjacent" address). Figure 6 shows a simplified sketch of the topology of the MM5290. The orientation (vertical rows, horizontal columns and lower left corner reference) is the same as in the other figures. The decimal numbering of the rows and columns, corresponding to figure 5, are shown. The shaded lines are metal rows. The clear lines are diffused column lines.

Examining the sequencing of the rows shows that rows 3 and 6, 4 and 9, etc., have physically adjacent cells. A test program using sequential binary addressing to assure reading adjacent cells in rows would require reading ±5 rows from the row of interest. Similarly, a column can have diagonally adjacent cells 2 column addresses away so that it requires ±2 columns to assure addressing all physically adjacent cells.

Further analysis indicates that the diffused column lines electrically isolate the cells between them from the rest of the array. Also, one of the adjacent cells (on the left or right) is always connected to the row line of the cell being investigated. This adjacent cell cannot be exercised without refreshing the cell of interest and all other cells in that row. The most practical and efficient disturb testing would exercise only the adjacent cell (on the left or right) not connected to the row line of the cell of interest and the two diffused column lines that isolate the cell in question from the rest of the array.

SUMMARY

The purist will exercise all 8 physically adjacent cells. A pragmatist will exercise the one adjacent cell not connected to the same row and the diffused column lines which isolate the cell. The efficient pragmatist will *not* use sequential binary addressing to exercise only one cell and two column lines when doing a disturb test on a cell.

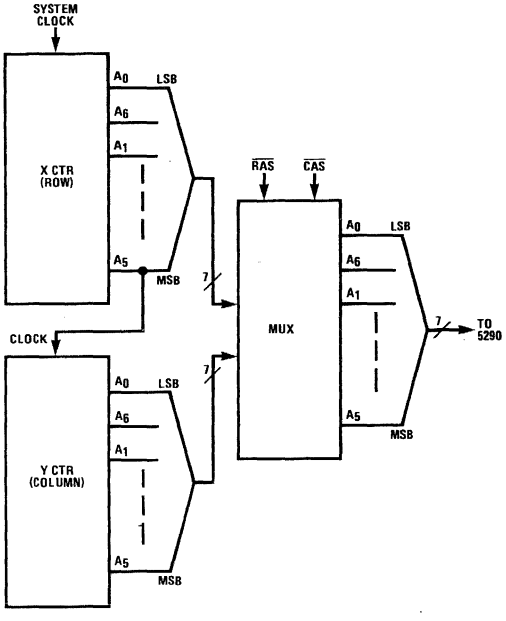


Figure 3. Test System Address Counters Showing X Counter as the "Fastest" Changing Address Counter

CELL NO.	COLUMN (MSB) A_5	A_4	A_3	A_2	A_1	A_6	A_0 (LSB)	ROW (MSB) A_5	A_4	A_3	A_2	A_1	A_6	A_0 (LSB)
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	0	0	0	0	0	0	1
•				•							•			
•				•							•			
•				•							•			
•				•							•			
•				•							•			
•				•							•			
512	0	0	0	0	1	0	0	0	0	0	0	0	0	0
•				•							•			
•				•							•			
•				•							•			
•				•							•			
•				•							•			
•				•							•			
16,383	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Figure 4. MM5290 Address Coding

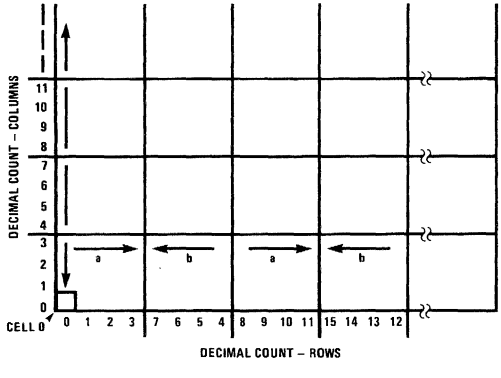


Figure 5. Addressing Bit Location

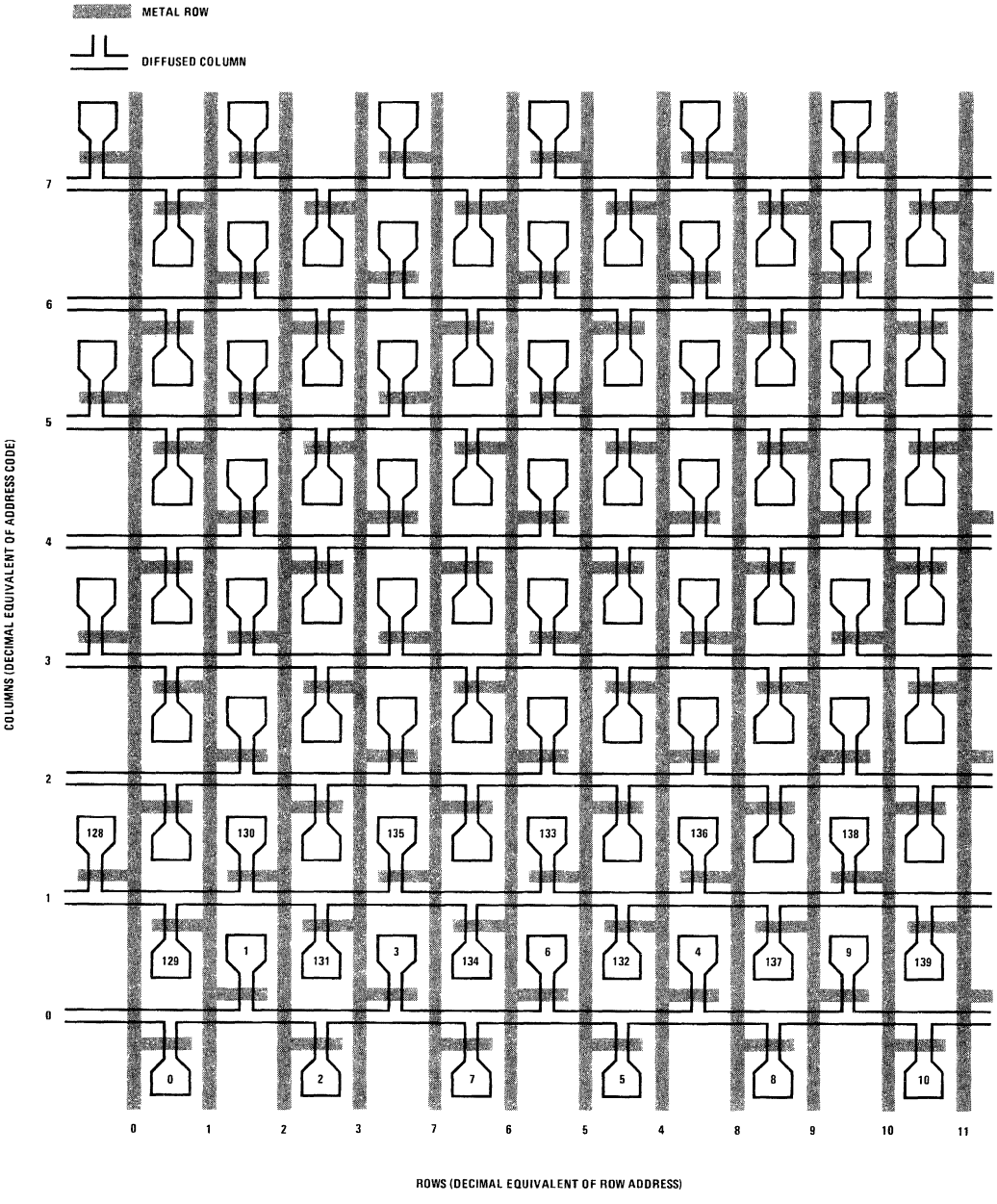


Figure 6. Simplified Topology (lower left corner of array)

MM5290 RAM
Test Description

INTRODUCTION

National Semiconductor's 16k dynamic RAM is done with sophisticated computer controlled RAM test systems.

This test description covers the general flow of the MM5290 done to insure a high quality product.

Wafer sort and quality assurance programs generally follow the described parametric and pattern testing and these are not included.

The following points are important to successful testing of the MM5290.

The following V_{BB} rule should be observed to prevent possible damage to a unit under test:

a. Power-up: V_{BB} must be brought up prior to any power supply or input signal.
b. Power-down: V_{BB} must be maintained until all other supplies and inputs have been brought to zero.

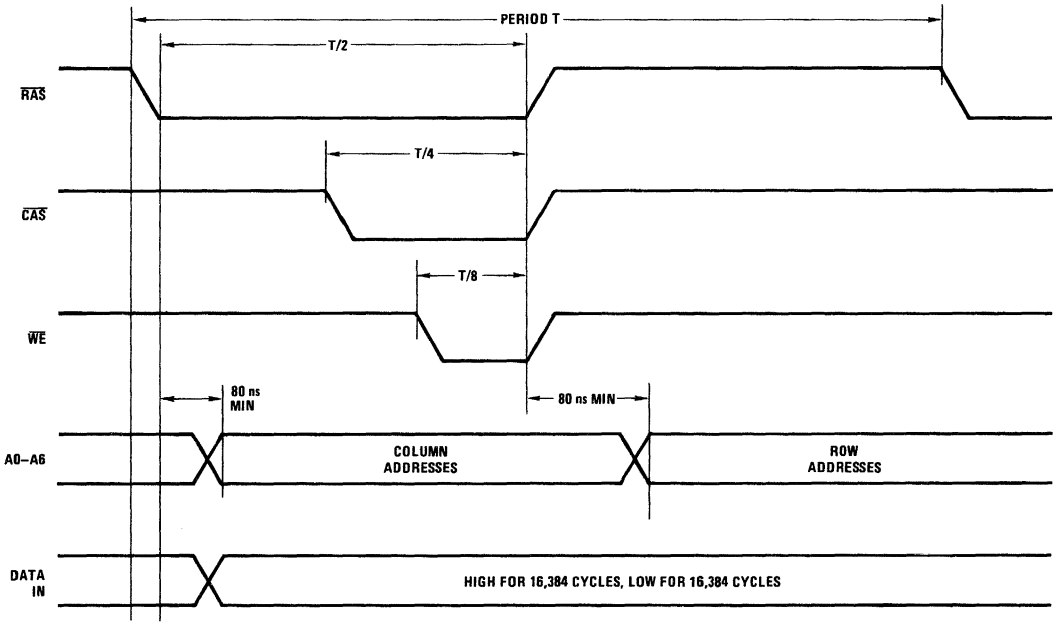
Several cycles are required after power-up *or after the maximum refresh period has been exceeded* before proper device operation is achieved. Any 8 cycles which perform refresh are sufficient.

No input signal (including transients) can be more negative than V_{BB} by 0.5V. This can forward bias the substrate and may cause damage to the device. This should be especially considered in burn-in ovens in which signals may not be well controlled.

Capacitive decoupling at the test fixture should maintain the peak-to-peak transients on V_{DD}, V_{BB} and V_{CC} lines at equal to or less than 400 mV *as measured between the appropriate voltage pin and ground pin on the device under test* (not open socket or the backside of the fixture).

This MM5290 final test description is in a preliminary form. It indicates the flow, the burn-in and the basic intent. It will be several months before the testing of this complex RAM is firmly established. The patterns, correlated limits and timing are all subject to shifts to guarantee a quality part. Notice also that no page mode testing is shown. This will probably only be done if the customer requires it. National currently has test capability in place on the Teradyne J387 test system.

Burn-In Timing

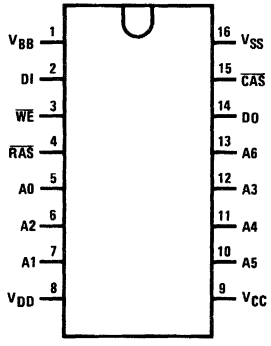


2.8 μs $\leq$ Period T $\leq$ 5.6 μs

Note 1: Input timing points: V_{IH} = 2.2V, V_{IL} = 0.6V.
Note 2: Address lines: $T_R \leq 250$ ns, $T_F \leq 250$ ns.
Note 3: $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$: $T_R \leq 150$ ns, $T_F \leq 150$ ns.

Burn-In Connection Diagram

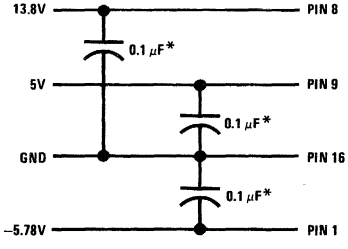
Dual-In-Line Package



TOP VIEW

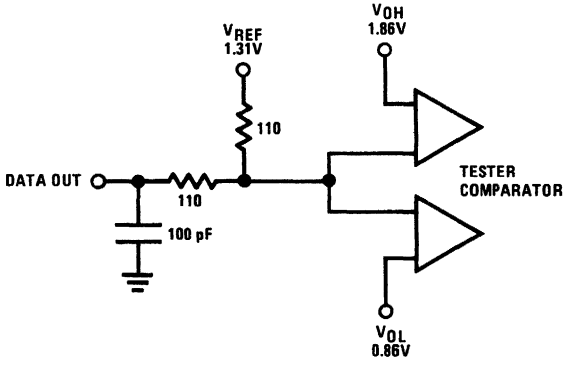
Pin Names

$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Write Enable
A0–A6	Address Inputs
DI	Data Input
DO	Data Output
V_{DD}	Power (12V)
V_{CC}	Power (5V)
V_{SS}	Ground
V_{BB}	Power (–5V)



*0.1 μF capacitors between 5V and GND, –5V and GND alternate every other socket in each column, 0.1 μF capacitors between 12V and GND every socket.

OUTPUT LOADING

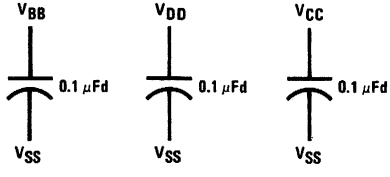


$$I_{SOURCE} = \frac{2.4 - 1.31}{220} = 4.95\ mA$$

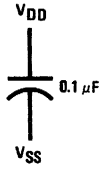
$$I_{SINK} = \frac{1.31 - 0.40}{220} = 4.14\ mA$$

BYPASS CAPACITANCE

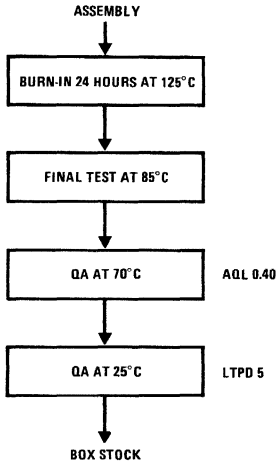
On Handler Backplate



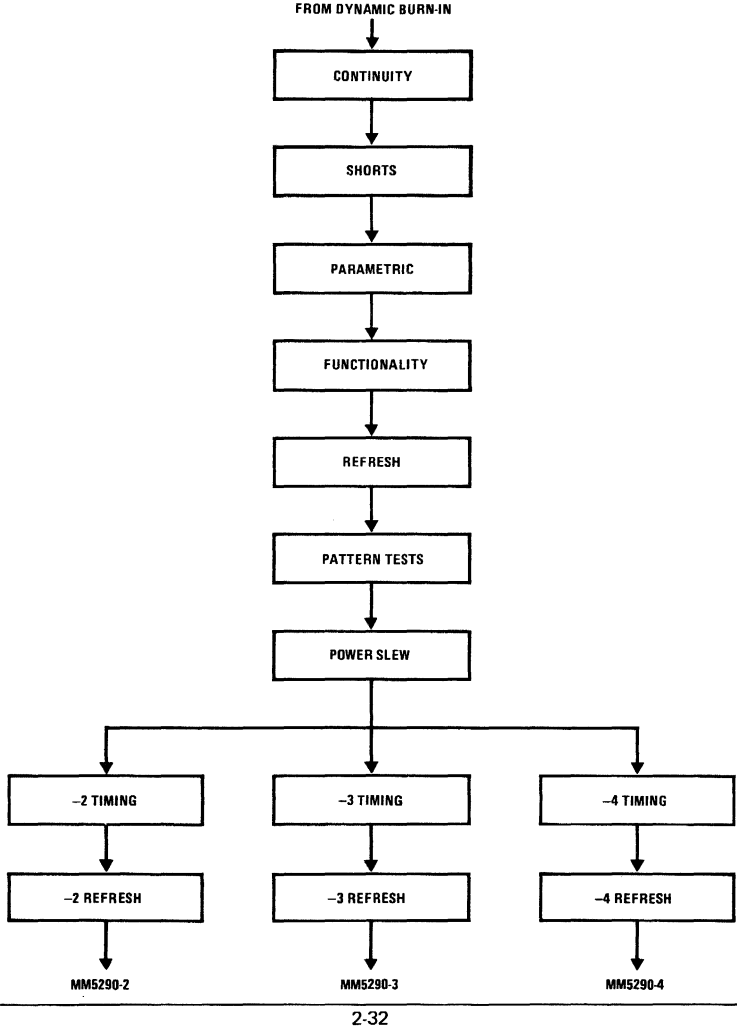
On Siemens Handler Teeth



GENERAL TEST FLOW



FINAL TEST FLOW



Trouble Shooting Check List For Memory Systems Using the MM5280

1. Is CE rise time greater than 10 ns and less than 40 ns? ☐
   Is this true at all points on the board? ☐
2. Does CE meet the min-max V_{IHC} and V_{ILC} spec including ringing at all points on the board? ☐
3. Are the CE on and off time specs being observed? ☐
4. Are the bypass capacitors big enough and close enough so that the power supply variation plus the peak-to-peak noise on the supplies does not exceed the ±5% specifications? ☐
5. Do all TTL level signals reach their respective V_{IH} and V_{IL} levels before CE reaches 2 V? ☐
6. Is the output loaded properly? ☐
   No more than one TTL load and no more than 50 pF. Is the V_{CC} bypassed properly? ☐
7. Is the memory being refreshed properly? ☐
   Are all rows (A0 through A5) being refreshed every 2 ms? ☐
8. Are address setup and hold time specs being observed (including CS)? ☐
9. Are address setup and hold times being observed during refresh, including column addresses and CS? ☐
10. Is timing of output data strobe meeting access time spec? Is it being strobed at a time when noise from other signals is at a minimum? ☐
11. Is WE input at V_{IH} level for entire read cycle? ☐
12. Is minimum WE width (t_{WP}) spec being observed? ☐
13. Are the write timing specs (t_{CW} and t_{WI}) with respect to CE being observed? ☐
14. Is the D_{IN} stable early enough before the end of CE in order to meet the t_D spec (150 ns)? ☐
15. Does the data on D_{IN} remain stable until CE has reached 2 V at the end of CE? ☐
16. Are the clock drivers bypassed with high frequency capacitors close to the clock driver package? ☐
17. Do the clock drivers have damping resistors? Are they large enough value for the lower CE capacitance of the MM5280? ☐
18. Are the clock lines short to reduce ringing? ☐
19. Are the clock drivers close to the memory array to avoid the impedance mismatch between loaded and unloaded lines? ☐
20. Are data input and output lines running perpendicular to clock lines or at least far away to minimize coupling? ☐
21. Is part being conditioned (refreshed) after power-up? ☐

Section 3

Static Read/Write Memory

3

The growth in usage of static RAMs, particularly 1k, and more recently 4k, has been phenomenal. Primary factors in this growth are low cost, ease of use, TTL signal and power supply compatibility, standard DIP packaging, and multiple sourcing. National supplies a broad line of MOS and bipolar static RAMs for the spectrum of today's applications. This section is intended to assist you in matching industry standard static RAMs to your particular needs.

Static RAM Applications

Figure 1 illustrates the ease of designing a static RAM support memory for a microprocessor, in this case the 16-bit INS8900. Full buffering has been included to a system bus which carries common input/output data and address. Operation may be from a 5-volt power supply or on-board regulation may be used. Decoupling should follow the same practices as used for TTL boards.

Figures 2 and 3 depict possible configurations for power down of the MM5257, while figure 4 shows allowable input conditions. These power down techniques apply to others of National's static RAM family including the MM2114, MM2101A, MM2102A, MM2111A, and MM2112A series.

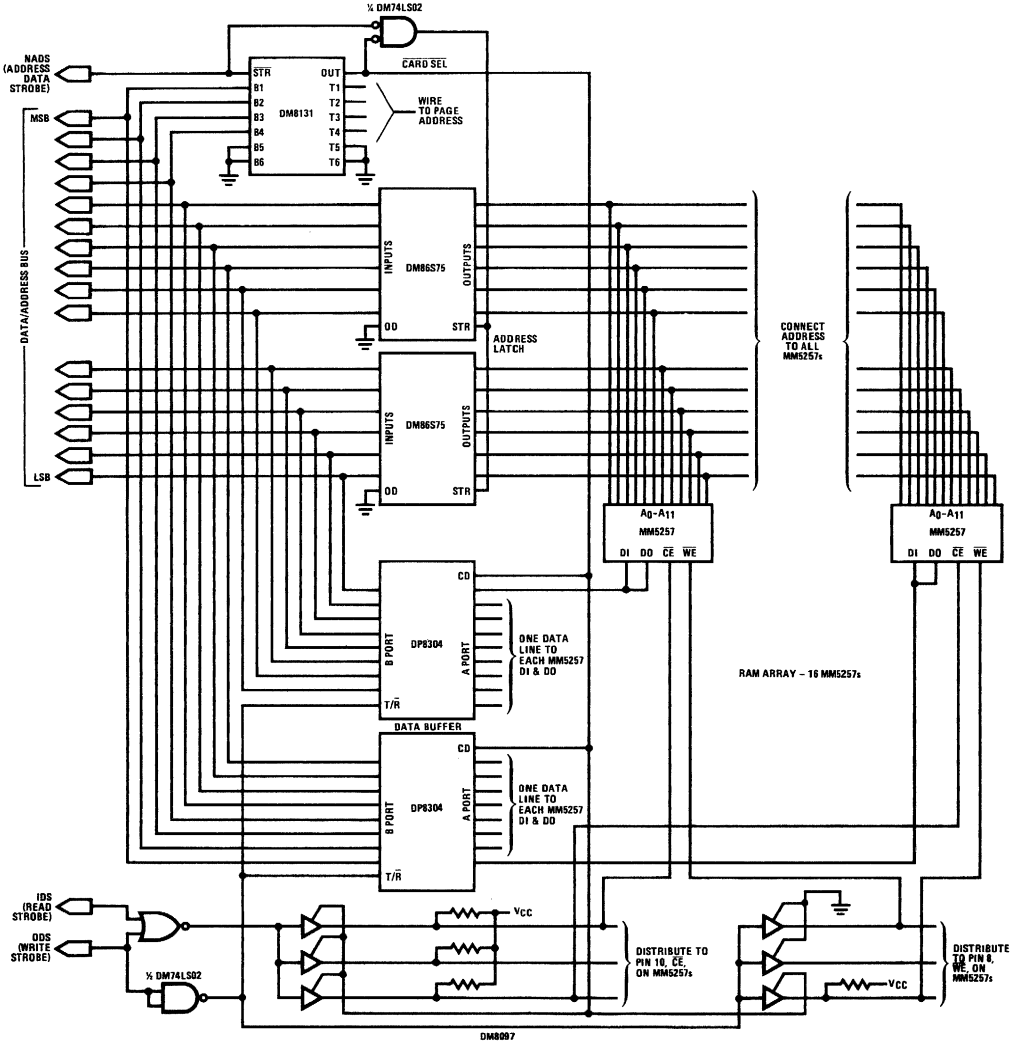


Figure 1. Example Application of MM5257 4k x 1 Static RAM: 4k x 16 Memory Card for 16-Bit Microprocessor System

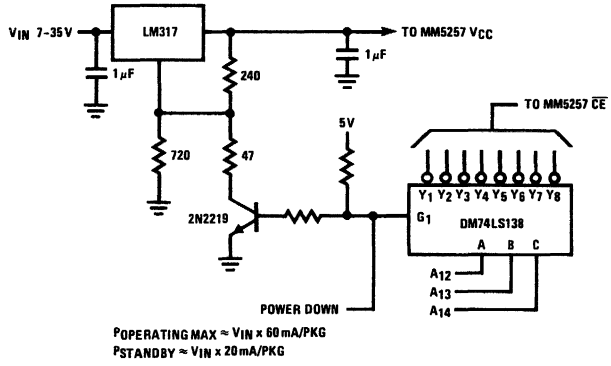


Figure 2. 4k Static Power Down 1

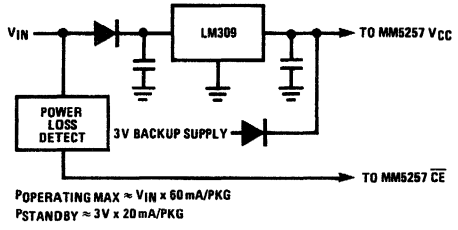


Figure 3. 4k Static Power Down 2

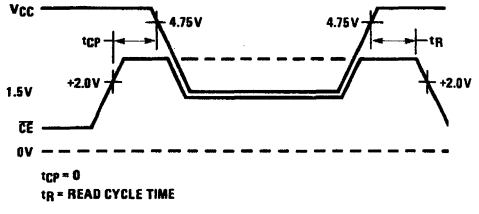


Figure 4. 4k Static Power Down Mode

Interfacing Static R/W Memories to the 8080A

Addressing Techniques

The INS8080A has a 16-bit address bus that is capable of addressing up to 65k bytes of memory and up to 256 input and 256 output devices. In small systems with minimum memory and input/output requirements, buffering of the A_{15}-A_0 Address Bus may not be required. However, as memory and input/output device requirements increase, buffering is required for the bus. This address buffering function can be implemented by using two National Semiconductor DM81LS95 TRI-STATE Octal Buffers as shown in figure 1. Note that the system Bus Enable (BUSEN) signal is connected to the buffers so that they are forced into their high-impedance state during a DMA data transfer (BUSEN = logic 1) or any other time that bus access is desired, thereby allowing other devices to gain access of the address bus. As mentioned above, up to 65k bytes of memory and up to 256 input and 256 output devices can be directly addressed via the A_{15}-A_0 Address Bus of the INS8080A. The INS8080A microcomputer system can be configured so that memory and input/output devices are either treated separately (isolated input/output) or as a single memory array (memory mapped input/output) as described below. The mapping for the isolated input/output and memory mapped input/output addressing techniques is shown in figure 2. With both of these addressing techniques, the most common method of addressing memory or input/output devices is to decode some of the address bus bits as "chip selects" (using a device such as the National Semiconductor 74LS138) to enable the addressed memory or the input/output device. The linear select method is another way of addressing the input/output devices using either of the addressing techniques. In linear select, a singular address bus bit is assigned as the exclusive enable for a specified input/output device. Using this method limits the number of input/output devices that can be addressed but eliminates the need for extra decoders. In small system design this is an important consideration.

When the INS8080A system is configured for isolated input/output addressing, the memory address space is separated from the Input/output device's address space by using system control signals for the input/output architecture as shown in figure 3. Also, with isolated input/output addressing, the input/output devices communicate only with the Accumulator using the IN and OUT Instructions. Thus, since the memory address space is not affected by input/output device addressing, the full address space of 65k bytes is available for memory.

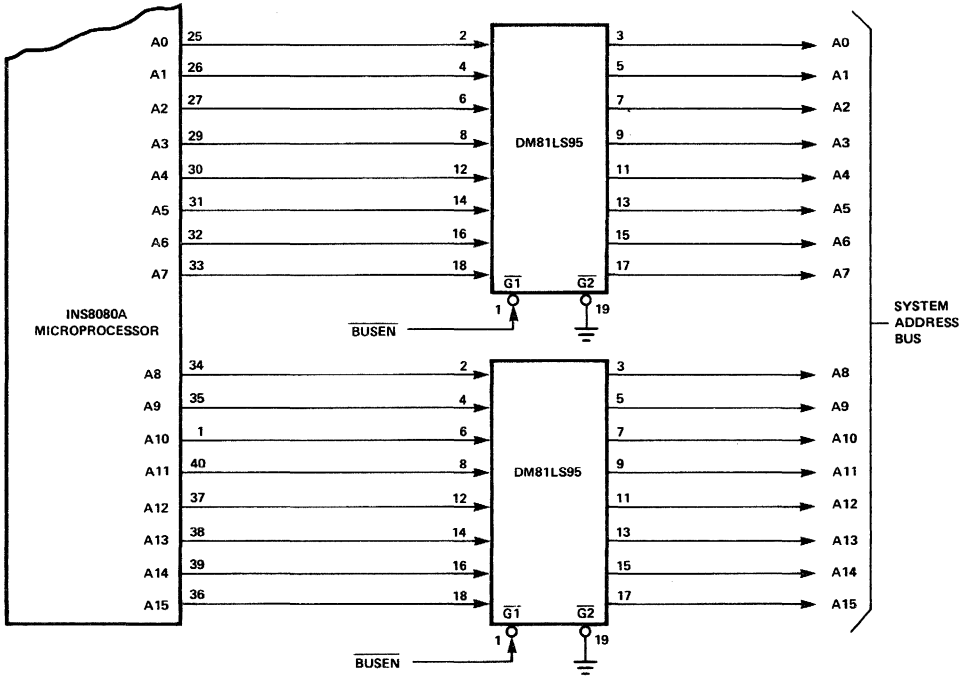


Figure 1. Address Buffer Design Using DM81LS95 Devices

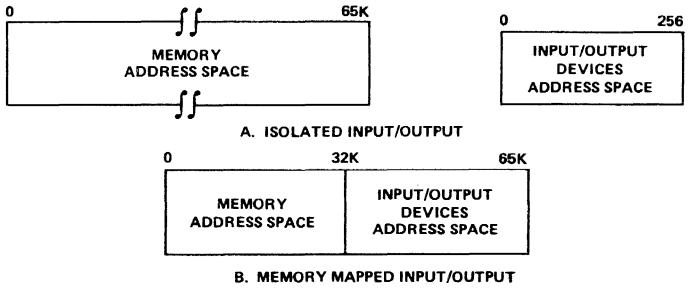


Figure 2. Mapping for Isolated Input/Output and Memory Mapped Input/Output Techniques

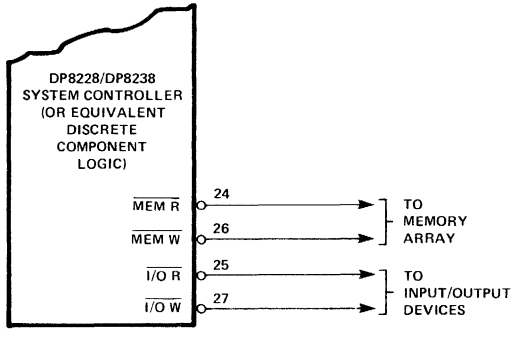


Figure 3. System Control Signals for Isolated Input/Output Addressing

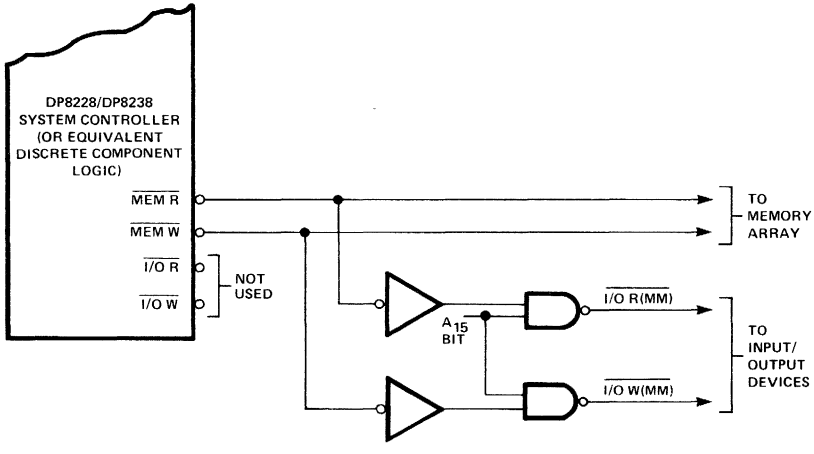


Figure 4. System Control Signals for Memory Mapped Input/Output Addressing

When the INS8080A system is configured for memory mapped input/output addressing, an area of the memory array is assigned to the input/output devices by using system control signals for the input/output architecture as shown in figure 4. In this configuration, new input/output control signals [I/O R (MM) and I/O W (MM)] are generated by gating the MEM R and MEM W signals with most significant address bit A_{15}. (Since these new input/output signals connect in exactly the same manner as the corresponding signals of the isolated input/output configuration, the system bus characteristics are unaltered.) Address bit A_{15} is used because it allows up to 32k bytes of memory addressing, and because it is easier to control with software. However, any other address bit may be used for this gating function. When bit A_{15} is low, the memory address space is active and when bit A_{15} is high, the input/output device's address space is active.

With memory mapped input/output addressing, all of the instructions that can be used to manipulate memory locations (for example, MOV M, r; LDA; STA; LHLD; et cetera) can also be used for the input/output devices. These devices are still considered addressed "PORTS" but instead of the Accumulator being the only data transfer medium for the peripherals, any of the internal registers of the INS8080A can also be used for this purpose. Thus, memory mapped input/output addressing is suited for small systems that require high throughput and have less than 32k bytes of memory.

Memory Interfacing

The CPU group of the N8080 microcomputer family interfaces with standard semiconductor memory components (and input/output devices) via a 3-bus architecture that includes an 8-bit bidirectional External Data Bus, a 6-bit Control Bus, and a 16-bit Address Bus. A typical interface to a memory array having 8k bytes of ROM storage and 512 bytes of RAM storage is shown in figure 5. This typical memory interface is suitable for almost any size of memory array. However, in larger systems, buffers may be required for driving the three buses and decoders may be required for generating the chip select signals for the memory array (and input/output devices).

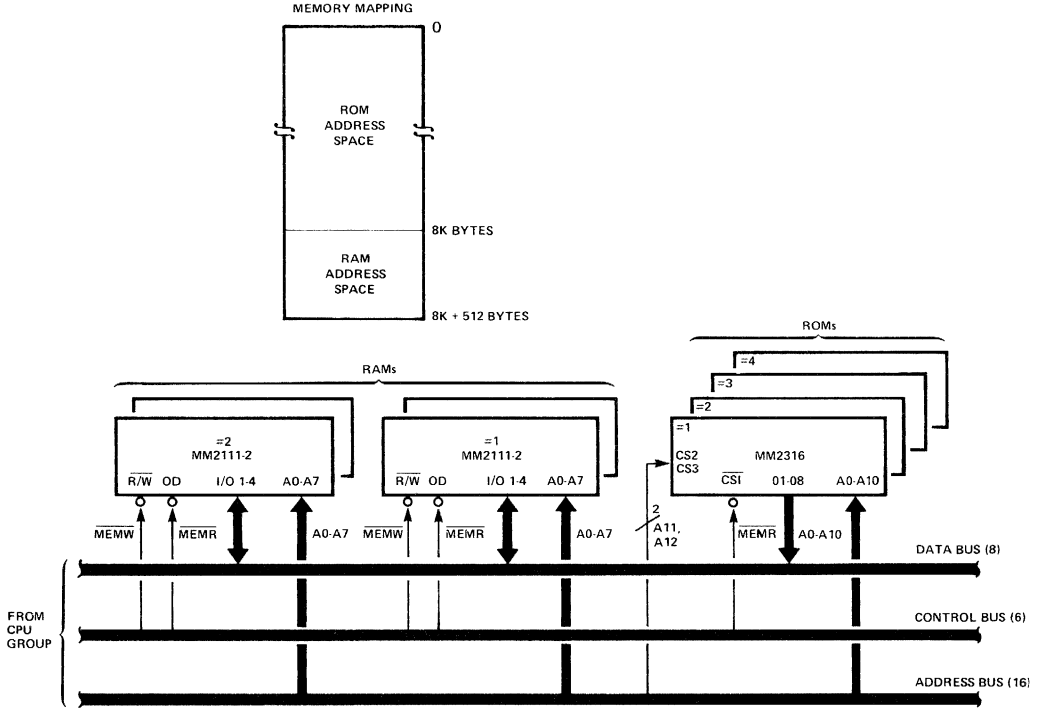


Figure 5. Typical Memory Interface

As shown in figure 5, the interfacing to the National Semiconductor MM2316 static ROMs is quite straightforward. The D_0-D_7 output lines of the ROMs are connected to the bidirectional External Data Bus; the A_0-A_{10} address inputs are connected to corresponding bits of the Address Bus; the CS2 and CS3 chip select inputs are connected to the A_{11} and A_{12} bits (most significant) of the Address Bus; and the CS1 chip select input of the ROMs is connected to the MEM R signal of the Control Bus. During a FETCH or MEMORY READ machine cycle, the CPU group may output an address in the ROM address space of the memory array. When this occurs, the data stored at the addressed ROM location are then gated onto the External Data Bus with a low-level MEM R signal. In this way, data are read from the ROMs in the INS8080A.

The interfacing to the four National Semiconductor MM2111-2 static RAMs is also straightforward. The I/O_1-I/O_4 common input/output lines of the RAMs are connected to corresponding bits of the bidirectional Data Bus; the A_0-A_7 address bits are connected to corresponding bits of the Address Bus; and the R/W and OD inputs of the RAMs are connected to the MEM W and MEM R (or DBIN) signals, respectively, of the Control Bus. During a FETCH, MEMORY READ, or STACK READ machine cycle, the CPU group reads data from the RAMs in exactly the same manner as described above for the ROMs. During a MEMORY WRITE or STACK WRITE machine cycle, the CPU group outputs an address in the RAM address space of the memory array. When this occurs, the data to be written into memory are then strobed into the addressed RAM location with a low-level MEM W signal. In these ways, data are read from and written into RAMs in the INS8080A microcomputer system.

The memory array of figure 5 includes ROMs (MM2316) and RAMs (MM2111-2) that have an access time of 850 nanoseconds (maximum). When the INS8080A microprocessor is operated from a clock generator with a t_{CY} of 500 nanoseconds, the required memory access time is from 450 to 550 nanoseconds. Therefore, to use the slower memory components in the system, the INS8080A microprocessor must contain a synchronization provision to allow the memory components to request the wait state (t_W). (The actual number of t_W states to be inserted is determined by external logic that is user designed.) This provision can be implemented for any slow memory (RAM or ROM) by a simple logic control of the READY input of the INS8080A as follows. When the addressed slower memory receives a MEM R or MEM W signal, it places a low-level on the READY line of the microprocessor, causing the INS8080A to enter the WAIT sequence. After the slower memory has had time to respond, it places a high-level on the READY line, thereby allowing completion of the instruction cycle.

Interfacing the 6800 Microprocessor to National CMOS MM74C910 Memory

National Semiconductor
Bill Kopek*
October 1977

INTRODUCTION

The applications of solid state non-volatile memory are numerous. One such application involves an Area Navigation System used on aircraft. Waypoint information can be conveniently stored upon engine shutdown and becomes readily available at power-up. This is especially useful for cross-country flying so that the same waypoint data does not have to be entered into the Area Navigation System at each aircraft takeoff.

6800 AND MM74C910 INTERFACE

A 6800 is utilized in the Area Navigation System for processing and computations. Figure 1 shows a block diagram of the system which includes 2k x 8 ROM and 64 x 4 RAM.

Non-volatile memory for waypoint storage is obtained by usage of the MM74C910. This device is a 64-word by 4-bit RAM consisting of six address lines, four data input lines, four data output lines, a Write Enable ($\overline{WE}$) and a Memory Enable ($\overline{ME}$). Typical supply current for the device is 0.05 μA.

Interface of the 6800 and MM74C910 is accomplished via the DS8T28 Bus Transceiver. However, additional hardware and software are required to extend the data time on the bus to read and write 4-bit data. (Two MM74C910 CMOS RAMs organized by 8-bit words would simplify software.)

Figure 2 shows the clock circuit hardware required to extend the data time during Write. Clock phase 2 is extended from 500 ns to 550 ns by increasing the time constant of the Monostable generator. The output is passed through one NAND and two INVERTER circuits to the Data Bus Enable input of the microprocessor. A data extension of approximately three gate delays is thereby accomplished, allowing Data Input Hold Time t_{HD} (min) of 30 ns to be met before $\overline{WE}$ from the 6800 goes high. When the MM74C910 is not being accessed the Data Bus Enable input of the 6800 is high and the clock 1 and clock 2 monostable generators are a symmetrical 500 ns.

CONCLUSION

National CMOS RAMs are competitive in solid-state non-volatile memory applications. Projections for battery life of 10 years have been made using lithium batteries with average current drains of 10 μA.

One other approach using MOS technology for Electrically Alterable ROMs can be competitive in larger systems, although the Read Cycle of approximately 20 ms and the Write Cycle of approximately 60 ms are prohibitively long compared to those of CMOS RAMs.

*Refer to Introduction.

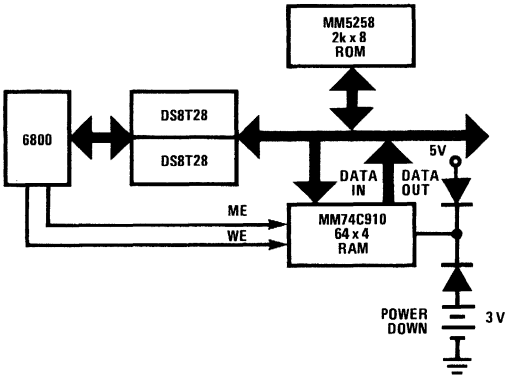


Figure 1.

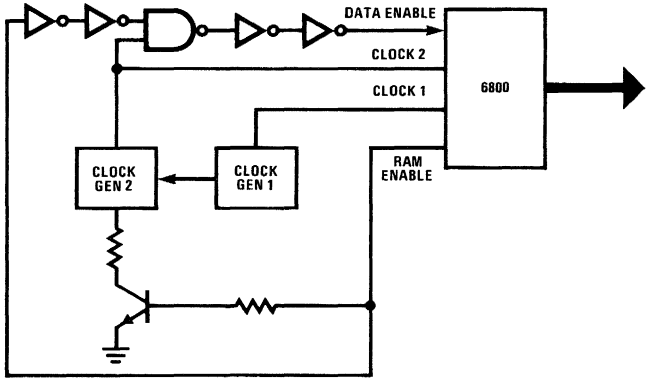


Figure 2.

1k CMOS RAMs

National Semiconductor
Karl Rapp
March 1977

1. INTRODUCTION

Static CMOS memory with typical access time of only 120 ns—such performance has been made possible by the combination of an advanced silicon-gate CMOS process and contemporary circuit-design performance.

Four different products comprise National Semiconductor's 1024-bit silicon-gate CMOS RAM family. Characteristics and differences of these memories are summarized in Table I. The MM54C921/MM74C921 is identical to the MM54C920/MM74C920, except that inputs and outputs are internally connected and share package pins. The MM54C929/MM74C929 is identical to the MM54C930/MM74C930, except that the 3 chip selects are internally connected and brought to a single pin. All 4 memories use the same basic logic design and sub-system components. All are *synchronous* static memories.

2. SYNCHRONOUS VS ASYNCHRONOUS STATIC MEMORY

Memory Cell

Static memory cells almost invariably are constructed using 6 devices connected as a pair of cross-coupled inverters, with pass devices (also called transmission gates) for selection control. *(Figure 1)*. If the pass transistors are N-channel, data stored in the flip-flop can more readily be affected by pulling *down* on a column line; the pass transistor then conducts in common-source mode. Pulling up has significantly less effect because of the weaker source-follower behavior of the pass device. Writing into the cell, therefore, consists predominantly of pulling down the required side of the flip-flop. Internal cell regeneration causes most of the rising-voltage action on the other side. It thus follows that both DATA and $\overline{\text{DATA}}$ column lines must be held high during ROW address change or data can be destroyed.

Data Protection During Address Change

Two basic techniques are available for protecting stored data as the selected ROW is changed: (1) asynchronous memory using passive column pull-up devices or (2) synchronous memory using active (strobed) column pull-up devices.

With (1) passive pull-ups, cell pass transistors must be designed to have relatively high impedance to prevent cell-to-cell interaction, should overlap occur in row selection. Alternatively, row-address decoders must be designed to ensure turn-off of a selected row before turn-on of a new row—with sufficient interim delay to achieve column pull-up. Moreover, cell sense current must be kept relatively small since sense current from every cell in a selected row goes into the column pull-ups—causing power dissipation. The net result is sacrifice of potentially smaller access time and the dissipation of power in selected chips.

National Semiconductor's CMOS memories are type (2), synchronous devices. A chip strobe is used to control column pull-ups. Pull-up transistors precharge column lines high while the strobe is absent; address decoders are inhibited during this time. When the strobe is applied, column pull-ups turn OFF, thereby avoiding any DC path for sense current; address decoders are enabled. Availability of the strobe makes possible important design advantages including high-speed sense amplifiers and on-chip registers for address and output data.

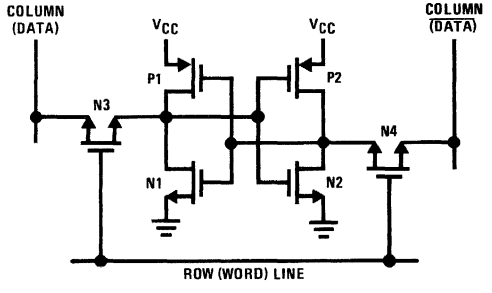


FIGURE 1

TABLE I

	ORGANIZATION	NO. OF PINS	I/O	NO. OF CHIP SELECTS (INCL. STROBE)	STROBED CHIP SELECT?
MM54C920/MM74C920	256 x 4	22	Separate	3	Yes
MM54C921/MM74C921	256 x 4	18	Common	3	Yes
MM54C929/MM74C929	1024 x 1	16	Separate	1	No
MM54C930/MM74C930	1024 x 1	18	Separate	3	No

3. MEMORY STRUCTURE

General organizations of the 256 x 4-bit and 1024 x 1-bit memories are shown in *Figures 2 and 3*, respectively. The basic structures of the 2 designs are identical.

Each of the designs has address registers controlled by the strobe terminal ($\overline{ST}$ for the 256 x 4-bit memories, $\overline{CS1}$ for the 1024 x 1-bit memories). *The general term $\overline{STROBE}$ used throughout this application note refers to $\overline{ST}$ for the MM54C920/MM74C920 and MM54C921/MM74C921 and to $\overline{CS1}$ for the MM54C929/MM74C929 and MM54C930/MM74C930.* A HIGH level at the strobe terminal allows the external address code to fall through the address-register latches and reach the decoder inputs; the decoders, however, are inhibited from selecting any row or column while the strobe input is HIGH. When $\overline{STROBE}$ falls, the address code then contained by the address registers is latched and external code changes have no further effect. $\overline{STROBE}$ LOW simultaneously enables the decoders, causing the selected location(s) to be read, and sends the data to the output latch(es).

While $\overline{STROBE}$ is LOW, the data falls through the data-out latch to the TRI-STATE® buffer input. When $\overline{STROBE}$ next goes HIGH, the data-out latch locks and stores the data. Note from the diagrams, *Figures 2 and 3*, that $\overline{STROBE}$ has no control over the TRI-STATE buffer.* Only the other 2-chip selects and the write-enable terminal control TRI-STATE. In WRITE mode (write-enable LOW), the output is disabled even though the 2-chip selects are active (LOW).

Writing into either of the memory types requires that $\overline{STROBE}$, the other 2 chip selects, and write enable all be LOW, i.e., the chip must be selected and write enable be LOW. In read mode (write enable HIGH), however, a chip need not be selected completely for new data to be stored in the data-out latch. Each chip in a system will react as its strobe terminal is brought LOW, independent of the status of its other chip-select terminals. New

*Except for the MM54C929/MM74C929 which has the strobe and other 2 chip selects connected together.

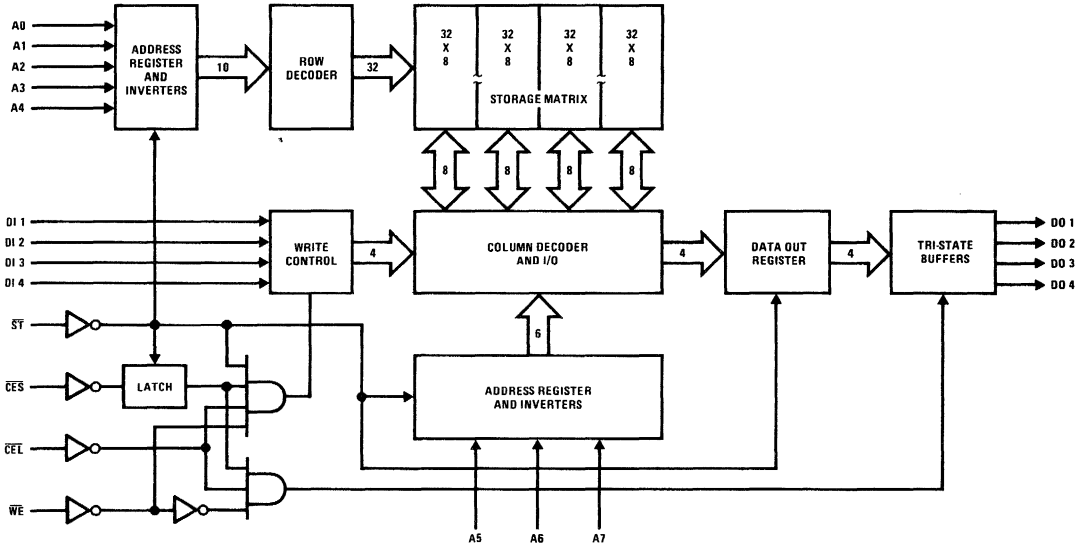


FIGURE 2. MM54C920/MM74C920 Logic Diagram

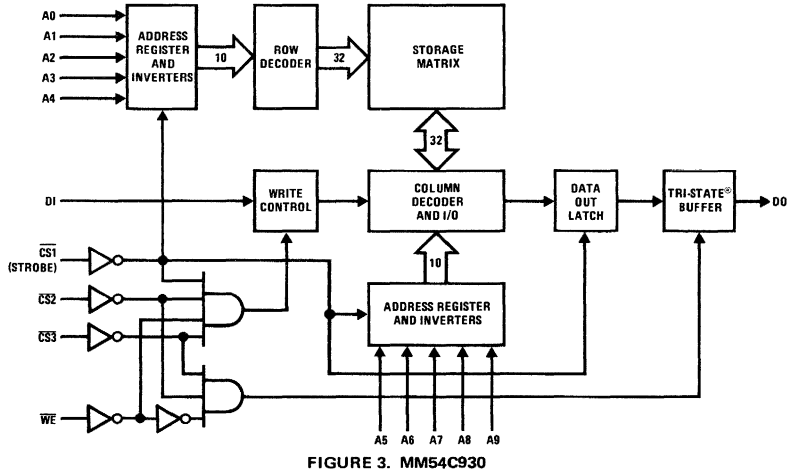


FIGURE 3. MM54C930

data corresponding to the buss address code will be fetched and stored in the data-out latches. The other chip selects choose which chip delivers its data to the data buss. Page-mode memory organization thus is available.**

The only difference between the 2 memory types, *Figures 2 and 3*, aside from the word organization, lies in the chip-select input circuits. One-chip select of the 256 x 4-bit RAMs is latched by $\overline{\text{STROBE}}$ exactly as addresses are latched. $\overline{\text{CES}}$ (Chip Enable, Strobed) thus must be established at the proper level prior to the fall of $\overline{\text{STROBE}}$. As with address inputs, set up and hold time requirements must be met by $\overline{\text{CES}}$ with respect to the negative-going edge of $\overline{\text{STROBE}}$. Once latched by $\overline{\text{STROBE}}$, the captured $\overline{\text{CES}}$ level remains constant until the end of the cycle, i.e., until $\overline{\text{STROBE}}$ again falls at the beginning of the next cycle. The $\overline{\text{CEL}}$ (Chip Enable, Level) control is not latchable. It functions completely independently of $\overline{\text{STROBE}}$. Chip selects $\overline{\text{CS2}}$ and $\overline{\text{CS3}}$ on the 1024 x 1-bit RAMs both are level actuated and operate independently of $\overline{\text{STROBE}}$ $\overline{\text{CS1}}$.

4. MEMORY TIMING

AC specifications for the memories are given in Tables II and III, timing diagrams in *Figures 4 and 5*. Typical values of the parameter as a function of temperature are given in *Figure 6*.

** For description of a page-mode application, see Section 7, paragraph 5.

TABLE II. MM54C920/MM74C920, MM54C921/MM74C921 AC Electrical Characteristics

V_{CC} = 5V ±10%, T_A = Operating Range

PARAMETER		MM54C920, MM54C921			MM74C920, MM74C921			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
TTL Interface ($V_{IH} = V_{CC} - 2V$, V_{IL} = 0.8V, Input $t_{RISE} = t_{FALL}$ = 5 ns, Load = 1 TTL Gate + 50 pF)								
t_C	Cycle Time	290	120		255	120		ns
t_{ACC}	Access Time From Address		120	275		120	250	ns
t_{ACS}	Access Time From Strobe		110	250		110	225	ns
t_{AS}	Address Setup Time	25	10		25	10		ns
t_{AH}	Address Hold Time	25	15		25	15		ns
t_{OE}	Output Enable Time		60	150		60	130	ns
t_{OD}	Output Disable Time		60	150		60	130	ns
$t_{\overline{ST}}$	$\overline{ST}$ Pulse Width (Negative)	150	60		130	60		ns
t_{ST}	ST Pulse Width (Positive)	140	60		125	60		ns
t_{WP}	Write Pulse Width (Negative)	150	80		130	80		ns
t_{DS}	Data Setup Time	100	40		90	40		ns
t_{DH}	Data Hold Time	60	25		60	25		ns

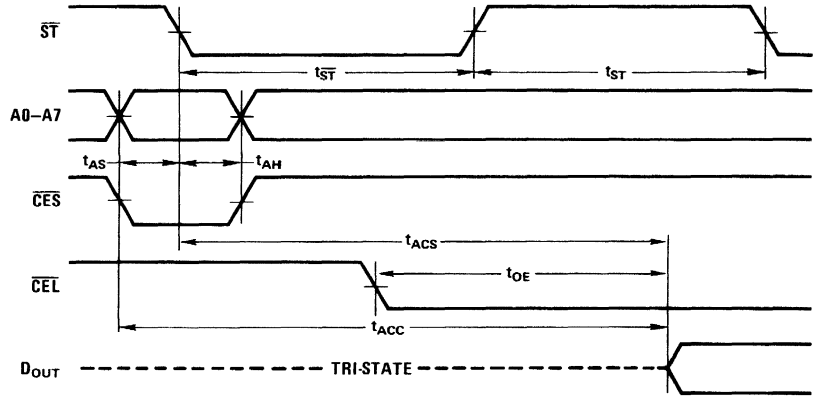
TABLE III. MM54C929/MM74C929, MM54C930/MM74C930 AC Electrical Characteristics

V_{CC} = 5V ±10%, T_A = Operating Range

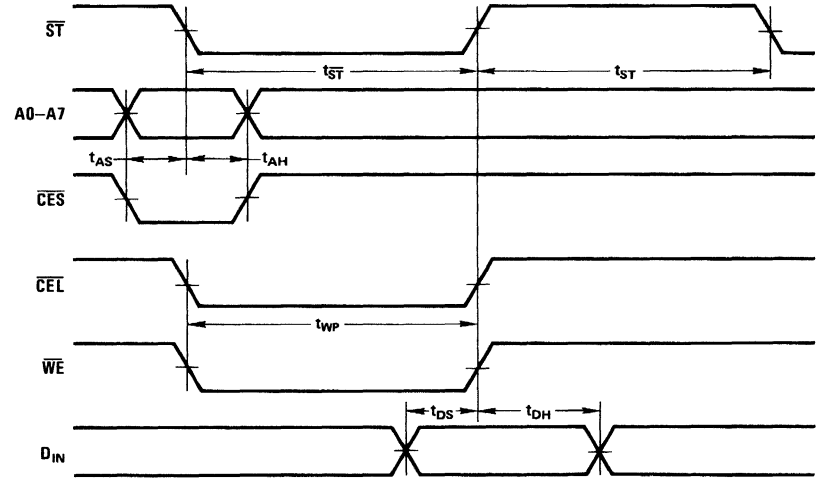
PARAMETER		MM54C929, MM54C930			MM74C929, MM74C930			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
TTL Interface ($V_{IH} = V_{CC} - 2V$, V_{IL} = 0.8V, Input $t_{RISE} = t_{FALL}$ = 5 ns, Load = 1 TTL Gate + 50 pF)								
t_C	Cycle Time	290	135		255	135		ns
t_{ACC}	Access Time From Address		105	265		105	240	ns
t_{ACS1}	Access Time From $\overline{CS1}$		100	250		100	225	ns
t_{AS}	Address Set-Up Time	15	5		15	5		ns
t_{AH}	Address Hold Time	50	20		50	20		ns
t_{OE}	Output Enable Time		60	150		60	130	ns
t_{OD}	Output Disable Time		60	150		80	130	ns
$t_{\overline{CS1}}$, (Note 3)	$\overline{CS1}$ Pulse Width (Negative)	150	75		130	75		ns
t_{CS1}	$\overline{CS1}$ Pulse Width (Positive)	140	60		125	60		ns
t_{WP}	Write Pulse Width (Negative)	150	80		130	80		ns
t_{DS}	Data Set-Up Time	150	75		140	75		ns
t_{DH}	Data Hold Time	0	−30		0	−30		ns

Typical = Nominal at 25°C

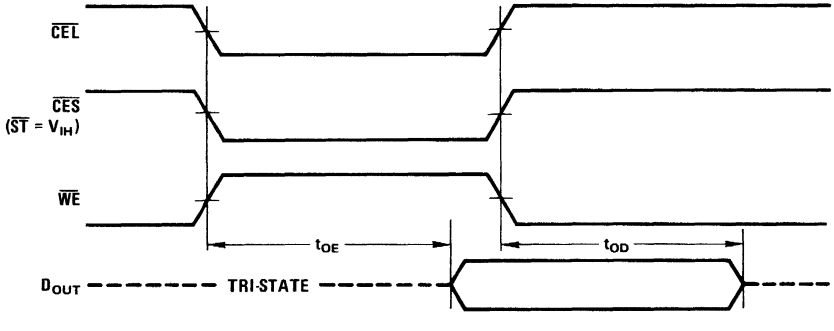
Note 3: Greater than minimum $\overline{CS1}$ pulse width must be used when reading data from the MM54C929/MM74C929 to ensure that output TRI-STATING does not occur before data becomes valid. Writing has no such limitation.



(a) Read Cycle ($\overline{WE}$ = V_{IH})

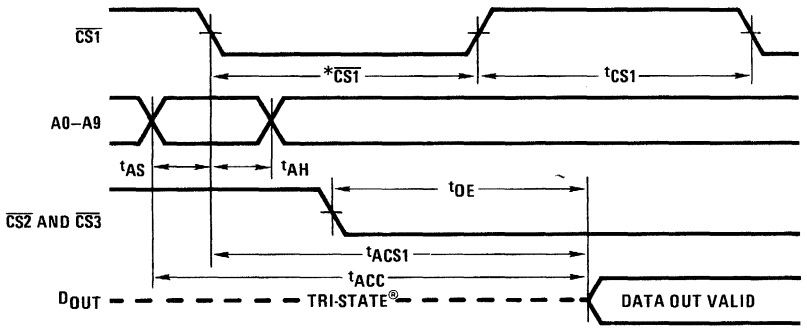


(b) Write Cycle

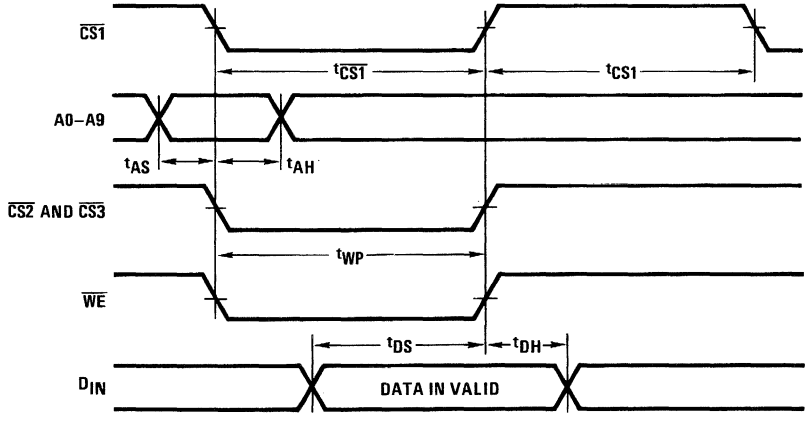


(c) Output Enable/Disable

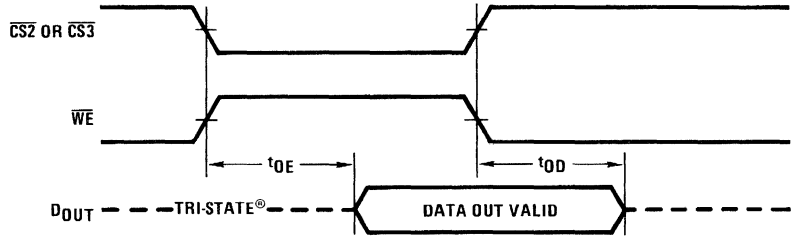
FIGURE 4. MM54C920/MM74C920, MM54C921/MM74C921 Switching Time Waveforms



(a) Read Cycle ($\overline{WE}$ = V_{IH})

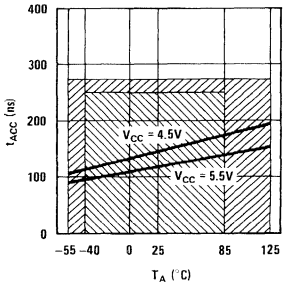


(b) Write Cycle

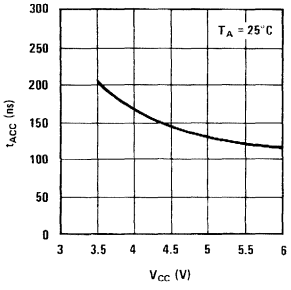


(c) Output Enable/Disable

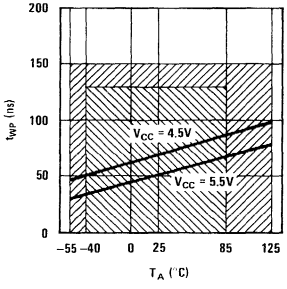
FIGURE 5. MM54C929/MM74C929, MM54C930/MM74C930 Switching Time Waveforms



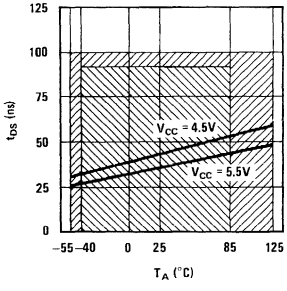
(a) Access Time vs Ambient Temperature



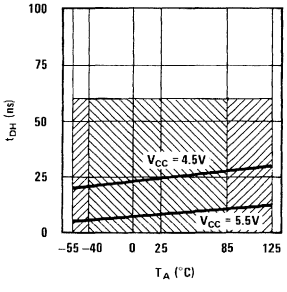
(b) Access Time vs Power Supply Voltage



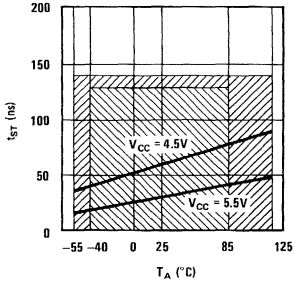
(c) Minimum Write Pulse Width vs Ambient Temperature



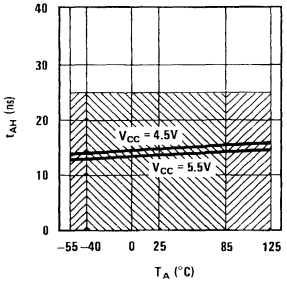
(d) Data-In Setup Time vs Ambient Temperature



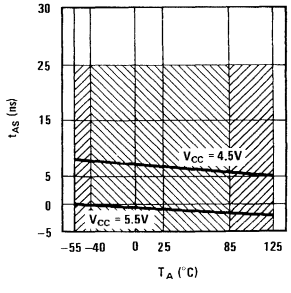
(e) Data-In Hold Time vs Ambient Temperature



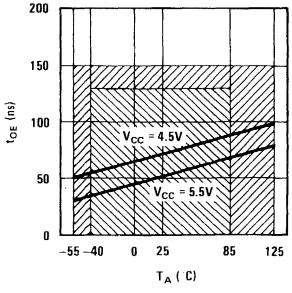
(f) Minimum $\overline{ST}$ Pulse Width (Positive) vs Ambient Temperature



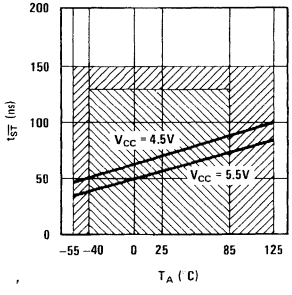
(g) Address Hold Time vs Ambient Temperature



(h) Address Setup Time vs Ambient Temperature



(i) Output Enable Time vs Ambient Temperature



(j) Minimum $\overline{ST}$ Pulse Width (Negative) vs Ambient Temperature

Test Limit MM54C920, MM54C921

Test Limit MM74C920, MM74C921

FIGURE 6. Typical Performance Characteristics

General

Set-up and hold time requirements, with respect to STROBE, must be met by all address inputs and by CES (MM54C920/MM74C920 and MM54C921/MM74C921 only). A minimum down time is specified for STROBE to ensure that new data reach the output latch during READ and to provide sufficient time to reliably enter new data during WRITE. A minimum STROBE up time is specified to allow for pulling up columns and for precharging sense amplifiers. The sum of these 2 STROBE time specifications establishes minimum cycle time.

READ Cycle

Access time is specified both from address change and from the falling edge of STROBE. Access from address change is the more meaningful measure of the speed with which new data can be fetched. It is important, however, to recognize that access from STROBE will limit if more than minimum address set-up time is provided.

Note that the asynchronous character of all auxiliary chip-select controls except CES (MM54C920/MM74C920 and MM54C921/MM74C921) permits them to fall after STROBE. Provided that the selection occurs at least t_{OE} (output-buffer enable time) before new data are made internally available by STROBE, no effect on access time occurs.

The MM54C929/MM74C929 is different from the other 3 parts in that all 3 of its chip selects are internally tied together. Data-access control and output-buffer control, therefore, are no longer isolated. Consequently, STROBE should be kept LOW the full access time to prevent turn-off of the TRI-STATE buffer before new data are available.

WRITE Cycle

WRITE circuits on a chip are activated only when STROBE, the other chip selects, and WRITE ENABLE all are LOW. To satisfy the specified minimum write-pulse width, then, these signals must be jointly LOW for at least the specified t_{WP}.

The first of the above control signals to move HIGH ends the write operation. Input data must be valid a minimum set-up time, t_{DS}, before the first positive-moving control-signal edge and be maintained a minimum hold time, t_{DH}, beyond that edge. For successive WRITE cycles, note that WE and/or the auxiliary chip selects may be kept LOW. STROBE alone then would establish the write period.

Disabling of the output buffer when write-enable, WE, is LOW is useful for common-data-I/O applications. These CMOS memories have been designed to keep their outputs disabled when WE and the auxiliary chip selects simultaneously go LOW. Note, however, that if the chip selects fall prior to WE, outputs can become briefly enabled until the falling WE signal takes control. Conflict between external data drivers and the on-chip data buffers could occur during this interval, causing unexpected data-buss transients. No damage to the CMOS RAM's will occur, however.

5. DC CHARACTERISTICS

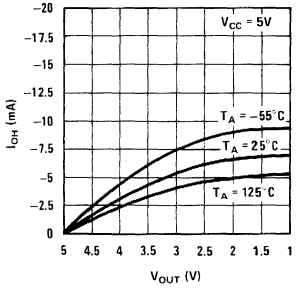
DC Specifications for the memories are contained in Tables IV and V. Over their operating voltage and temperature ranges, the memories easily can drive a TTL load. Current sinking capability is guaranteed to be at least 2 mA at 0.4V, while an mA source current is the minimum available at 2.4V. Typical output current-voltage characteristics are given as a function of temperature in *Figure 7*.

For battery-backup applications where low power is extemely important, these RAMs will retain data with V_{CC} supply voltage as low as 2V. Supply current, guaranteed to be no more than 10 μA at full V_{CC}, typically is only a few nanoamperes.

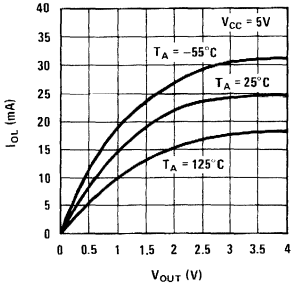
Typical operating supply current is shown as a function of supply voltage in *Figure 8*. These current values are for 1 MHz operating rate. Operating current is linear with frequency, however, and can be directly scaled for other frequencies.

6. MEMORY LOGIC AND CIRCUIT DETAILS

Logic symbols and their circuit equivalents are defined for this section in *Figure 9*.



(a) Output Source Current vs Output Voltage



(b) Output Sink Current vs Output Voltage

FIGURE 7

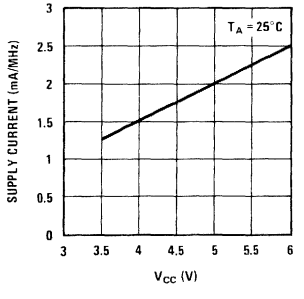


FIGURE 8. Dynamic Current vs Power Supply Voltage ($V_{IH} = V_{CC}$, V_{IL} = 0V)

TABLE IV. MM54C920/MM74C920, MM54C921/MM74C921 Absolute Maximum Ratings and DC Electrical Characteristics

Supply Voltage, V_{CC}	7V	Operating Temperature Range	
Voltage at Any Pin	−0.3V to V_{CC} + 0.3V	MM54C920, MM54C921	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C	MM74C920, MM74C921	−40°C to +85°C

V_{CC} = 5V ±10%, T_A = Operating Range

PARAMETER		CONDITIONS	MM54C920, MM54C921			MM74C920, MM74C921			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{IH}	Logical "1" Input Voltage		V_{CC}−2.0		V_{CC}	V_{CC}−2.0		V_{CC}	V
V_{IL}	Logical "0" Input Voltage		0		0.8	0		0.8	V
V_{OH1}	Logical "1" Output Voltage	I_{OH} = −1.0 mA	2.4			2.4			V
V_{OH2}	Logical "1" Output Voltage	I_{OUT} = 0	V_{CC}−0.01			V_{CC}−0.01			V
V_{OL1}	Logical "0" Output Voltage	I_{OL} = 2.0 mA			0.4			0.4	V
V_{OL2}	Logical "0" Output Voltage	I_{OUT} = 0			0.01			0.01	V
I_{IL}	Input Leakage	$0V \leq V_{IN} \leq V_{CC}$	−1.0	0.001	1.0	−1.0	0.001	1.0	μA
I_O	Output Leakage	$0V \leq V_O \leq V_{CC}$, $\overline{CEL}$ = V_{CC}	−1.0	0.001	1.0	−1.0	0.001	1.0	μA
I_{CC}	Supply Current	V_{IN} = V_{CC}, V_O = 0V		0.1	10		0.1	10	μA
C_{IN}	Input Capacitance	(Note 1)		4	7		4	7	pF
C_O	Output Capacitance	(Note 1)		6	9		6	9	pF
$C_{I/O}$	Data Input/Output Capacitance	MM54C921/MM74C921 Only		8	12		8	12	pF
V_{DR}	V_{CC} for Data Retention	$\overline{CEL}$ = V_{CC}	2.0			2.0			V

Note 1: Capacitance is guaranteed by periodic testing.

TABLE V. MM54C929/MM74C929, MM54C930/MM74C930 Absolute Maximum Ratings and DC Electrical Characteristics

Supply Voltage, V_{CC}	7V	Operating Temperature Range	
Voltage at Any Pin	−0.3V to V_{CC} +0.3V	MM54C929, MM54C930	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C	MM74C929, MM74C930	−40°C to +85°C

V_{CC} = 5V ±10%, T_A = Operating Range

PARAMETER		CONDITIONS	MM54C929, MM54C930			MM74C929, MM74C930			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{IH}	Logical "1" Input Voltage		V_{CC}−2.0		V_{CC}	V_{CC}−2.0		V_{CC}	V
V_{IL}	Logical "0" Input Voltage		0		0.8	0		0.8	V
V_{OH1}	Logical "1" Output Voltage	I_{OH} = −1 mA	2.4			2.4			V
V_{OH2}	Logical "1" Output Voltage	I_{OUT} = 0	V_{CC}−0.01			V_{CC}−0.01			V
V_{OL1}	Logical "0" Output Voltage	I_{OL} = 2 mA			0.4			0.4	V
V_{OL2}	Logical "0" Output Voltage	I_{OUT} = 0			0.01			0.01	V
I_{IL}	Input Leakage	$0V \leq V_{IN} \leq V_{CC}$	−1.0	0.001	1.0	−1.0	0.001	1.0	μA
I_C	Output Leakage	$0V \leq V_O \leq V_{CC}$, $\overline{CS2}$ or $\overline{CS3}$ = V_{CC}	−1.0	0.001	1.0	−1.0	0.001	1.0	μA
I_{CC}	Supply Current	V_{IN} = V_{CC}, V_O = 0V		0.5	100		0.5	10	μA
		V_{IN} = V_{CC} = 2V, V_O = 0V, at 25°C		0.25			0.25		μA
		V_{IN} = V_{CC} = 2V, V_O = 0V, at 125°C					4		μA
C_{IN}	Input Capacitance	(Note 1)		4	7		4	7	pF
C_O	Output Capacitance	(Note 1)		6	9		6	9	pF
$C_{\overline{CS}}$	Chip Select Capacitance	(Notes 1 and 2)		7	10		7	10	pF
V_{DR}	V_{CC} for Data Retention	$\overline{CS2}$ or $\overline{CS3}$ = $\overline{CS1}$ = V_{CC}	2.0			2.0			V

Note 1: Capacitance maximum is guaranteed by periodic testing.
Note 2: MM54C929/MM74C929.

Memory Cell and Selection Structure

The basic 6-transistor memory cell has already been described in Section III and *Figure 1. Figure 10* illustrates how each cell fits into the ROW/COLUMN and READ/WRITE selection structure. The memory cells are laid out in a 32-by-32 matrix. Hence, the ROW-SELECT signals have a 1-of-32 code; the selected row goes HIGH; the other rows remain LOW. The pass transistors N1 and N2 of all cells on the selected row then conduct. Similarly, selected COLUMN lines go high. The select code is 4-of-32 for the 256-by-4-bit memories and 1-of-32 for the 1024-by-1-bit memories. A HIGH COLUMN-SELECT signal turns ON both the WRITE access transistors N3 and N4 and the column sense amplifier. If the chip is in WRITE mode, the WRITE circuits pull either the WRITE "1" or the WRITE "0" buss LOW; the other one floats. In READ mode, both busses float. During selection, column-pull-up transistors P1 and P2 are turned OFF (STROBE is HIGH).

Address Decoders

ROW and COLUMN address decoders are logically as shown in *Figure 11*. Note that $\overline{\text{STROBE}}$ must be LOW for the output of either decoder type to go HIGH. Address bits A8 and A9 are used only for the 1024-by-1 memories.

Address Latches

Address registers comprise fall-through latches of the type shown in *Figure 12*. When $\overline{\text{STROBE}}$ is HIGH, the external address code is transmitted directly through to $\overline{A_K}$ and A_K. $\overline{\text{STROBE}}$ latches the code by going LOW.

$\overline{\text{CES}}$ Latch

The $\overline{\text{CES}}$ latchable chip select on the 256-by-4 RAM's is implemented using 2 latches of the type shown by *Figure 12*, to produce a dual-rank D flip-flop. Positive $\overline{\text{STROBE}}$ transitions thus do not disturb the stored state for $\overline{\text{CES}}$.*

*Early prototypes of the 256-by-4 memories used only a single latch stage. The external level on $\overline{\text{CES}}$ then would fall through when $\overline{\text{STROBE}}$ went HIGH.

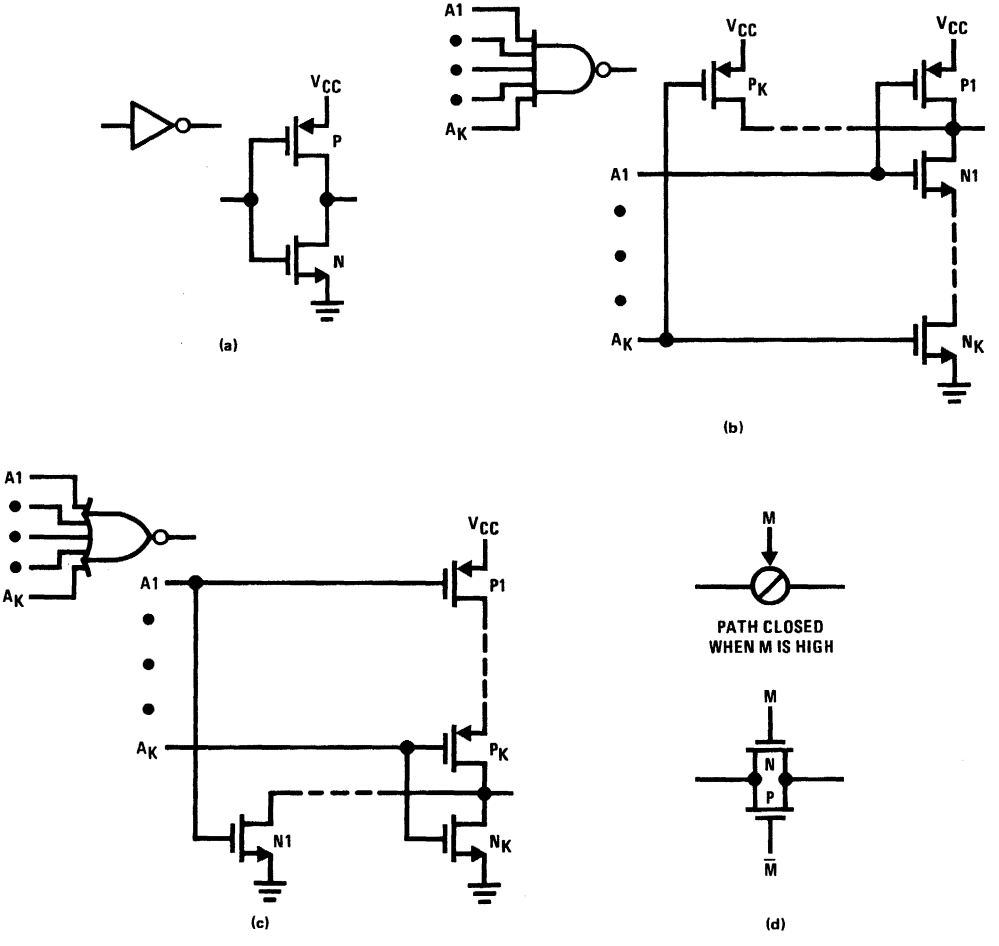


FIGURE 9

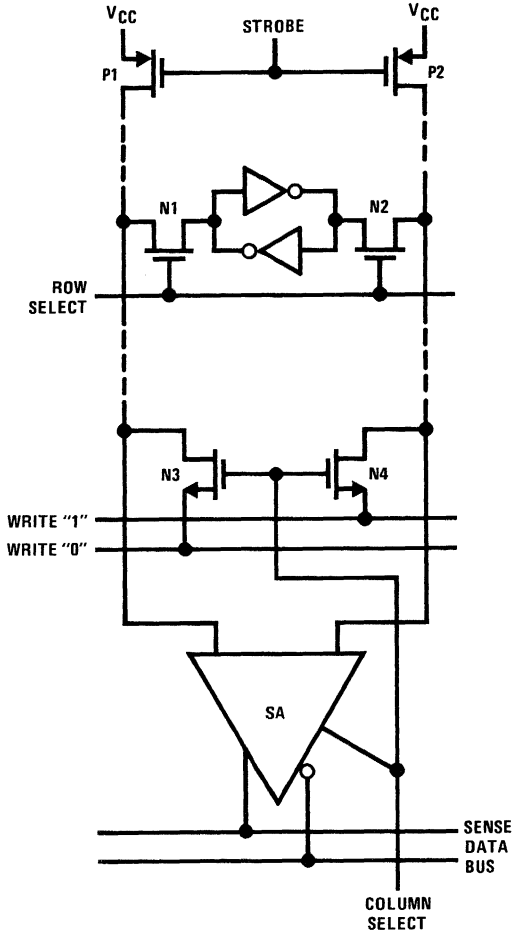


FIGURE 10

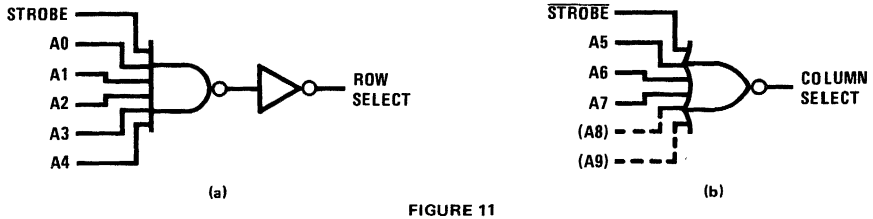


FIGURE 11

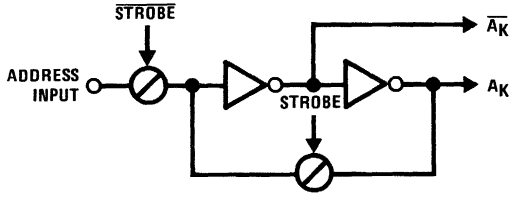


FIGURE 12

WRITE Control Logic

Figure 13 presents the logic used to control writing. Note that pass transistors N1 and N2 conduct only when all input controls are LOW, thus placing the chip in WRITE mode.

Sense Amplifier

The high-speed sense amplifier, shown in *Figure 14*, consists of differential-amplifier pairs at the end of each column, all connected via the sense-data buss to a single pair of load devices, L1 and L2. When $\overline{\text{STROBE}}$ falls, current flows in the selected-column differential amplifier, causing an amplified voltage differential between the 2 lines of the sense-data buss.

Data Latch and Output Buffer

Figure 15 diagrams the fall-through output-data latch and the TRI-STATE buffer. When the TRI-STATE control is LOW, both P1 and N1 turn OFF and the output floats.

7. APPLICATION CONSIDERATIONS

Latch-Up Precautions

The structure of CMOS IC's *(Figure 16)* intrinsically is similar to the PNPN structure of SCR's. If a junction becomes sufficiently forward-biased, the resulting minority-carrier injection can set off regenerative PNPN firing and thus cause large supply currents (100's of

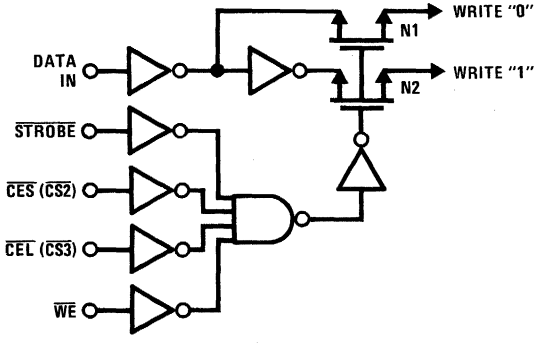


FIGURE 13

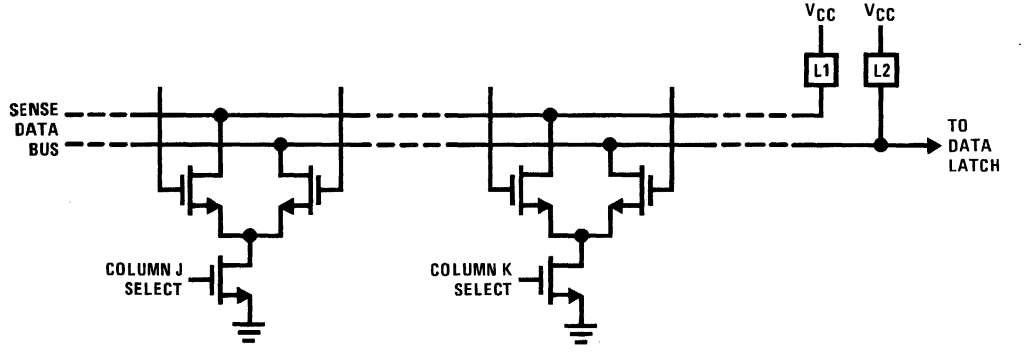


FIGURE 14

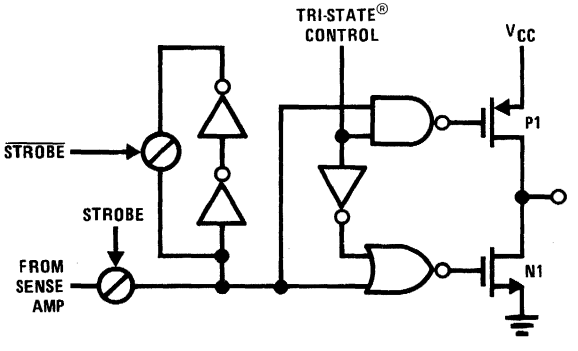


FIGURE 15

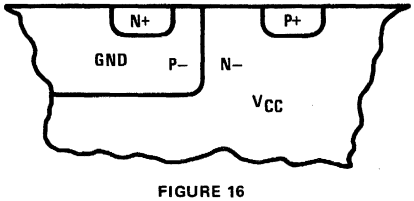


FIGURE 16

milliamperes) which pull down V_{CC}. It is important, therefore, to prevent input or output terminals from being driven more than 0.5V beyond the supply-voltage range.

Input Stages and I_{CC}

Input inverter stages are designed to accept TTL levels. It should be recognized, however, that some I_{CC} will be drawn by an inverter if the input-voltage level causes both P and N-channel transistors to conduct. Since the threshold voltage for both transistor types is about 0.7V, an input more positive than 0.7V and more negative than V_{CC}–0.7V will cause conduction. A curve showing typical I_{CC} versus temperature is given in *Figure 17* for the case where all inputs are at the TTL V_{IH} level. Not only the worst-case TTL level was used, but worst-case supply voltage of 5.5V also, to provide the highest typical currents one might expect.

To produce minimum power dissipation during standby, it is necessary to bring input levels to either 0V or a full V_{CC}.

Reduced-Voltage Data Retention

These CMOS RAM's will retain data with the supply voltage reduced to as low as 2V. They consequently find useful application in battery-backup data storage. In such applications, as V_{CC} is reduced, 3 precautions must be observed: (1) input voltages must not be left at higher values than V_{CC} as the supply is reduced or supply latchup can occur, (2) inputs should be maintained during reduced-voltage standby at either GROUND or the present V_{CC}—and not some intermediate voltage—to prevent input inverters from drawing I_{CC}, (3) control signal levels must be arranged to stay out of WRITE mode to avoid affecting stored data.

During recovery of V_{CC} to its full value, the $\overline{\text{STROBE}}$ logic state must be maintained constant (either HIGH or LOW) until address-line logic levels stabilize. This precaution on $\overline{\text{STROBE}}$ is necessary to avoid data destruction should $\overline{\text{STROBE}}$ experience a brief LOW-HIGH-LOW transition as signals stabilize. Such a brief transition could permit the fast-acting address-latch circuits to enter a new code, but might not allow sufficient time for data columns to be pulled up.

One useful method for providing battery back-up, consistent with the preceding precautions, is shown in *Figure 18*. The proper action for calling in the back-up battery is the following: (1) when removing V_{MAIN} or sensing that it is being lost, bring CS LOW. $\overline{\text{CS}}$ then assumes the moving V_{CC} potential and keeps the chip de-selected, (2) bring all other input signals to GROUND potential. (Actually, address inputs need not be controlled if $\overline{\text{STROBE}}$ is grounded since external signals then are locked out. See Section7, paragraph 2).

As V_{MAIN} is re-established, hold $\overline{\text{STROBE}}$ LOW until address inputs stabilize.

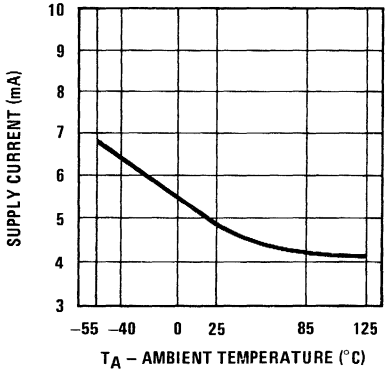
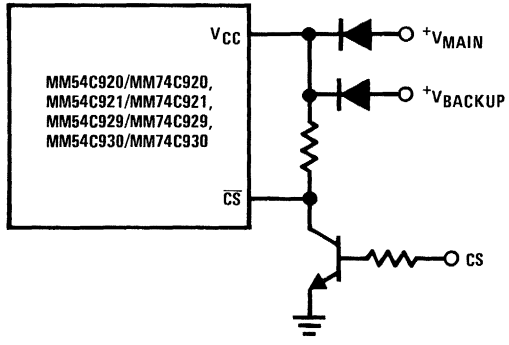


FIGURE 17. Typical DC Supply Current with TTL Input Levels vs Ambient Temperature V_{CC} = 5.5V, V_{IH} = 3.5V



For MM54C920/MM74C920, MM54C921/MM74C921: $\overline{\text{CS}} = \overline{\text{CEL}}$

For MM54C929/MM74C929, MM54C930/MM74C930: $\overline{\text{CS}} = \overline{\text{CS2}}$ or $\overline{\text{CS3}}$

FIGURE 18

Designing with Slower Transition Times

AC performance (Tables II and III) is specified and measured from 50% points of signal transitions. In applications where system-signal transition times are a significant fraction of specified times, V_{IH} and V_{IL} levels should be used as the measurement points. For example, to ensure adequate address set-up time, measurement as defined in *Figure 19a* should be used. For hold time, define as in *Figure 19b.*

Page-Read Memory

Because new data are latched into all chips in which $\overline{\text{STROBE}}$ is pulsed LOW—regardless of chip-selection status—page-organized memory can be implemented. *Figure 20* shows an example. Here, all chips are connected in parallel to $\overline{\text{STROBE}}$ and to the address lines. One cycle of $\overline{\text{STROBE}}$ brings data, corresponding to the address code, to all chip data-out latches. The M words of N data bits then can be scanned by successively selecting chip selects $\overline{CS}_0$ through $\overline{CS}_M$. Since output-enable time typically is only 50 ns, such a block of data can be read much more quickly than the 120 ns typical a full access would require.

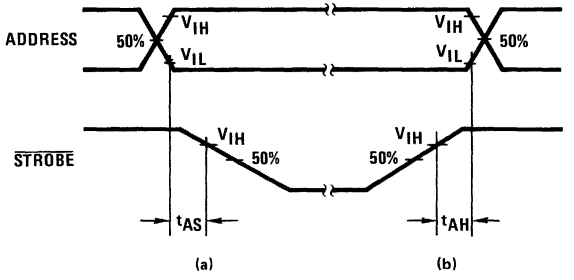
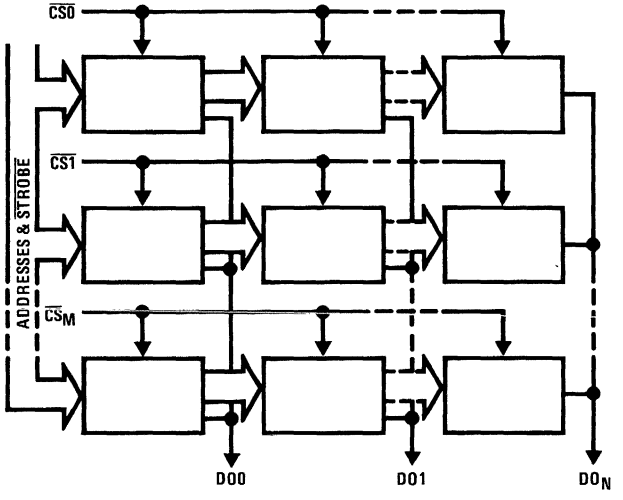


FIGURE 19



For MM54C920/MM74C920, MM54C921/MM74C921: $\overline{CS} = \overline{CE1}$

For MM54C930/MM74C930: $\overline{CS} = \overline{CS2}$ or $\overline{CS3}$

FIGURE 20

IDM2901A File Expansion Using the DM85S68

File Expansion

In certain applications the number of registers must be expanded beyond the 16 which are contained within the IDM2901A. The expansion is quite easily obtained with the use of the DM85S68 addressable D register file element. This array of registers is structured the same as the IDM2901A in that there are 16 words of 4 bits each. This component is clock edge senstivie when writing. Figure 1 shows the two components (IDM2901A and DM85S68) connected together so the effective size of the file is 32 words deep. It is easy to see how further expansion can be obtained if desired. There are several possibilities which could be used for address decode of this 32 word file. The most versatile usage would be to have separate address selection for each of the files. The IDM2901A would have an A address input and a B address input and the DM85S68 would have a distinct address input. If this cannot be obtained because of the system requirements then common address decoding for the 32 registers into two five bit fields can be obtained as in figure 2. In this schematic the external file is now limited in function to that of the internal portion of the file with the exception of shifting.

Register File Expansion

What can you do with this file extension?

Assume the following:

file locations R_0 through R_{15} are in 29015
R_{16} through R_{31} are in DM85S68

Then:

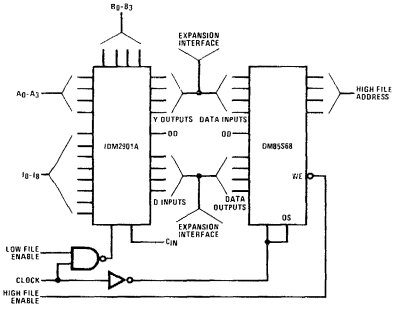
I $R_{0\text{-}15} + B_{0\text{-}15} \rightarrow B_{0\text{-}15}$
$\rightarrow R_{16\text{-}31}$

II $R_{16\text{-}31} + B_{0\text{-}15} \rightarrow B_{0\text{-}15}$
$\rightarrow R_{16\text{-}31}$
$R_{16\text{-}31} + R_{0\text{-}15} \rightarrow B_{0\text{-}15}$
$\rightarrow R_{16\text{-}31}$
$R_{16\text{-}31} + R_{0\text{-}15} \rightarrow Q$

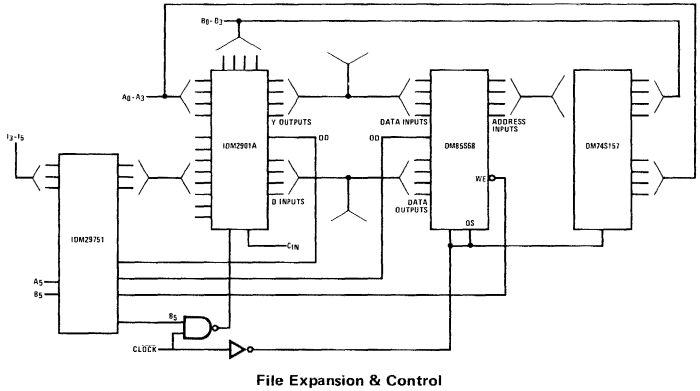
What does this schematic not do well?

I Single cycle shifts do not work, except $R_{0\text{-}15}$ Shift Right or Left is OK.

Shifts can be performed by making a transfer to the Q register, then shifting, and then transferring back to the $R_{15\text{-}31}$ register.



Register File Expansion



File Expansion & Control

Section 4

Read Only Memory

4

Program storage for microprocessors has become the fastest growing area of ROM application. As the performance of microprocessors and the sophistication of users increase, so will the requirements for large amounts of program storage. Also influencing larger ROM sizes is the trend toward higher level languages for microcomputers. The MAXI-ROM™ is a perfect vehicle for "Silicon Software™" – which is National's name for putting high level languages such as INS8080A BASIC, PACE BASIC, and NIBL (National Industrial Basic Language) for the INS8060 (SC/MP) into mask-encoded ROM – at a reasonable cost. Refer to National's Memory Data Book for the pin-compatible series of MAXI-ROM data sheets and current Silicon Software. Refer to this section for applications.

PROM Patches for the MAXI-ROM

National Semiconductor
C. Mitchell
October 1977

The introduction of the MM5235 8kx8 MAXI-ROM™* by National Semiconductor provides the system designer with cost-effective ROM to increase system capability with reduced package count and cost.

This 65,536-bit mask programmable ROM creates an understandable reluctance to commit such a large bit pattern to mask without extensive field testing.

This extensive field testing has associated costs in terms of EPROM programming overhead, parts count, component costs, and time which provide strong incentive to achieve an early masked ROM solution. One way to an early MAXI-ROM solution with minimal field testing is presented here.

The fundamental concept is to provide the capability of correcting errors in the MAXI-ROM program with system design/hardware (rather than by regenerating the masks). This also would provide for future changes to extend the market life of the system or to create additional capability.

This PROM Patch consists of providing a decode for the address location(s) of the MAXI-ROM which are to be altered, disabling the ROM and providing the corrected data to the data bus. The most cost-effective solution is through the use of a coincidence gate and a bipolar PROM as shown in figure 1.

This configuration allows correction of a single block of 32 bytes (one page). This block must start at a MAXI-ROM address divisible by 32. This is dictated by the requirement that A_5 through A_{12} must remain unchanged for the 32 combinations of A_0 through A_4 in order to get all 32 bytes. The substituted 32 bytes of the DM74S288 must contain the correct data originally stored in that page of the MAXI-ROM as well as provide altered data for those locations requiring correction.

More sophisticated techniques involving the use of adders to set initial starting addresses can be visualized. The primary drawback to such visualizations and the realization in figure 1 is the same. They are restricted by the requirement to hardwire page addresses. A technique not requiring jumpers or wired addresses utilizes a minimum of 2 PROMs. This approach is shown in figure 2 using 3 PROMs.

Here the first level PROM (DM74S287) provides address decode and the more significant address bits to the second level PROM(s) (DM74S288). These in turn provide substitute data to the bus. Note that use is made of the maskable chip selects on the MM5235. Conservative system design should allow for the possibility of patches. Board layout should follow the same philosophy providing for the patch circuitry.

Use of this dual rank approach allows greater adaptability as well as tighter packing density. Notice that data must (again) be replaced in blocks starting at location (binary) aaaA AAAA AAA0 0000 where the page address (represented by As) is programmed into the first level PROM. This allows block size to be a function of first level PROM output width and to be altered to provide less program redundancy between MAXI-ROM and the second level PROM. Regardless of block size the second level devices must copy the MAXI-ROM from start address to the ending location, correcting the erroneous locations in between.

The only timing restriction imposed upon the circuit in figure 2 is that the time between settling of the address lines and the leading edge of $\overline{CE}$ must exceed the access time of the DM74S287 (50 ns). This is most easily accomplished in most systems by making $\overline{CE}$ a function of the Read Strobe.

The ultimate in efficiency and flexibility for a PROM patch could be provided by a field programmable logic array (FPLA). Unfortunately the present high cost of these devices precludes their use in any but the most demanding parts count minimization.

Reviewing briefly, we have seen that there are a number of configurations which allow alteration of masked ROM configurations in a production system. The ultimate decision concerning the amount and type of patch provided for a MAXI-ROM can only lie with those software and/or hardware designers knowledgeable of the system, and must be based on experience and confidence. If this is done correctly enormous advantages in system capability can be realized through the use of large fixed program devices, i.e., MAXI-ROM.

*A trademark of National Semiconductor Corporation

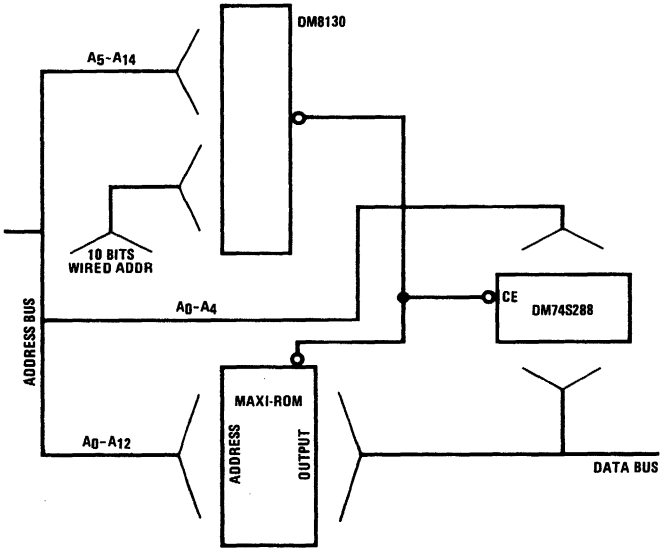


Figure 1. PROM Patch for MAXI-ROM (1)

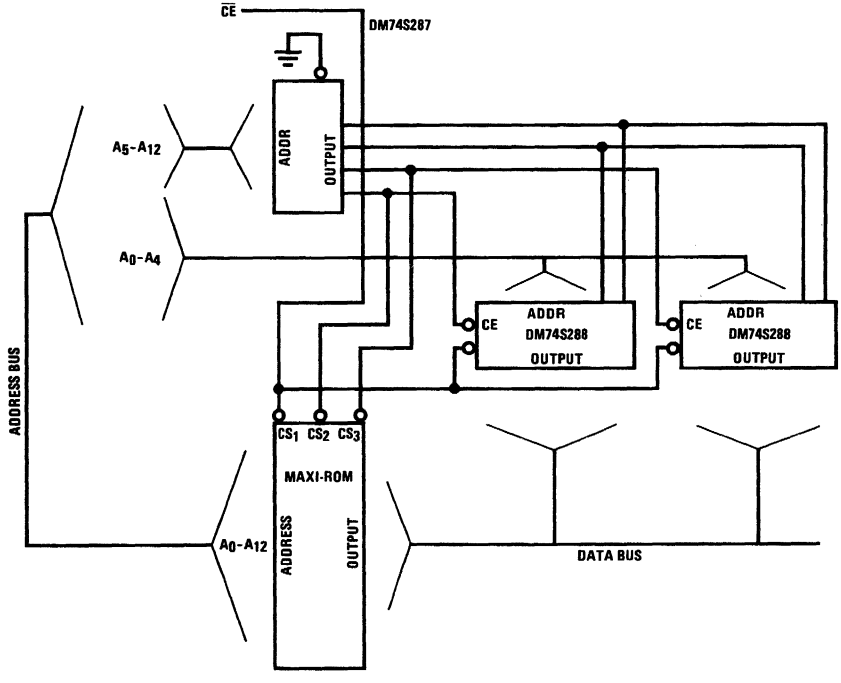


Figure 2. PROM Patch for MAXI-ROM (2)

ROM Emulator Using a Non Volatile RAM

National Semiconductor
Memory Application
Manfred Schwarztrauber*
November 1977

INTRODUCTION

The purpose of this article is to show how a read-write memory with battery backup can be implemented in order to use it as emulator for PROMs or ROMs in microprocessor systems.

Fixed, dedicated, unchangeable program portions are stored in read only memories (ROMs) or in programmable read only memories (PROMs) in microprocessor systems. These application programs are often created on a microcomputer or on a prototyping system with the aid of assembler or cross-assembler programs. One cannot assume that the programs, which are error-free assembled, function perfectly for a specific application the first time around.

In most cases, several corrections are necessary involving a learning curve until a program functions optimally and error-free.

The above considerations show:

1. It is necessary that program parts can be changed easily.
2. The memory must be non-volatile so as to not lose data in case of power failure or work interruption.

Both requirements can be easily realized with a read-write memory (RAM) that is provided with a battery backup to ensure data retention. In addition, there should be an easy way to store cross-assembled programs in the RAM and to test them in their specific applications environment.

In this manner the battery powered RAM becomes a ROM replacement in the particular machine or application. From this comes the choice of the name ROM emulator.

ROM EMULATOR HARDWARE

Figure 1 shows an example of a ROM emulator. With regard to hardware there are certain conditions in treating the RAM card as a ROM emulator:

It is advantageous to install the ROM emulator (battery powered transportable RAM) as a plug-in daughter board on a prototyping card. The prototyping card itself serves solely as a mechanical interface in the card cage of the microcomputer to its bus. In addition, the wiring of the daughter board (connector 1) is made to correspond to the wiring of the microcomputer bus, for example the SC/MP Low Cost Development System bus.

Likewise, special software must be created which permits the program to be stored in the ROM emulator. This software is basically a data loader.

In order to facilitate the use of the ROM emulator in a specific application, a further hardware requirement must be fulfilled. Parallel to the backplane a second cable to all connecting points of the ROM emulator should be provided. This is a flexible cable harness, terminated with a plug (connector 2) that is pin compatible with the PROM MM5204Q (or any other PROM). In this method, the possibility exists of plugging the ROM emulator through its cable directly in a corresponding socket of the ROM or PROM in a field application. Addresses, data, and control signals of the ROM emulator will then be connected to the bus of the desired application. A separate, smaller cable is used to supply the external read-write signals (connector 3).

In the example described here, a 512-byte RAM with 4 chips of MM2112N was built. Naturally, any other configuration with other RAM chips (for example CMOS) can be used, according to requirements. It is essential always to have compatibility between the emulator card and the corresponding ROM or PROM.

The supply of power to the memory board is buffered by 4 rechargeable batteries, so that the retention of data in the RAM is assured while providing portability (transport from prototyping machine to application). If power is required from batteries a switch should be placed in Position B (see figure 1). All 4 batteries are then in series and deliver the required operating voltage.

During the operation with the main power supply, Switch 1 should be in Position L. This allows the batteries to be charged in pairs, permitting a higher charging current (power) per battery. With the help of Switch S2, the batteries can be separated entirely from the power supply and board.

Figure 1 shows the principal construction of transportable RAMs with the buffered battery, the wiring configuration to the backplane, as well as to the PROM/ROM compatible flexible cable.

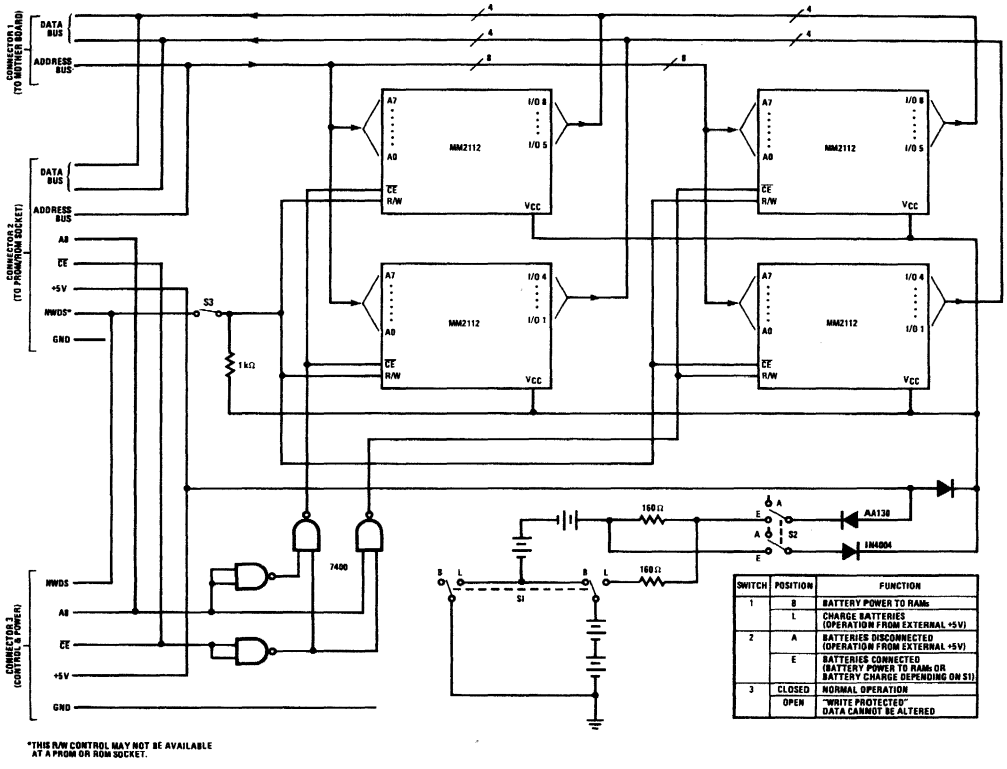
LOADING THE EMULATOR

The transportable RAM (the ROM emulator) can be loaded with data in different ways. Two basic possibilities will now be discussed:

The first possibility concerns the SC/MP Introkit, a microprocessor kit with teletype interface from National. The other refers to a prototyping machine. In both cases the ROM emulator serves as an extension of the RAM of the system.

Figure 2 shows the memory configuration of the SC/MP Introkit. Here the only practical way is to use the ROM emulator via its flexible cable as RAM extension. On the Introkit there is a provision through a corresponding socket to connect its addresses, data, and control signals easily to the ROM/PROM pin combatible plug of the emulator. After this connection is completed, it is possible to load the ROM emulator with data over the teletype interface of the Introkit.

*Refer to Introduction.



SWITCH	POSITION	FUNCTION
1	B	BATTERY POWER TO RAMs
	L	CHARGE BATTERIES (OPERATION FROM EXTERNAL +5V)
2	A	BATTERIES DISCONNECTED (OPERATION FROM EXTERNAL +5V)
	E	BATTERIES CONNECTED (BATTERY POWER TO RAMs OR BATTERY CHARGE DEPENDING ON S1)
3	CLOSED	NORMAL OPERATION
	OPEN	"WRITE PROTECTED" DATA CANNOT BE ALTERED

Figure 1. Portable PROM/ROM Emulator

The second possibility concerns a prototyping system. As already mentioned, the ROM emulator is plugged into the daughter board on a prototyping card, and this is installed into a prototyping system. The data is loaded via the microcomputer bus and the backplane into the ROM emulator. With the help of software it is now possible to load data directly – that means the creation of the program itself can occur at the assembler level.

A program must be generated to allow the loading of modules, as they are produced, from the prototyping machine directly into the ROM emulator. Naturally, the wiring of the ROM emulator's address field must be determined and established.

With the help of this program it is possible to load "load modules" in the ROM emulator as they are generated. The program which is stored directly in the ROM emulator in machine code can now be directly tested in the desired application.

After testing, debugging, and verifying an application program, it can be loaded into a corresponding PROM. The programmed PROM can now be plugged into the desired application, and substitutes for the ROM emulator.

CONCLUSION

The principle, as explained here utilizing the MM2112, MM5204Q, Introkit, and prototyping system, can be applied through enlargement of the RAM and change of the PROM-ROM compatible plug to any presently available PROMs or ROMs of any size. For bigger memories it is advantageous to install CMOS in order to keep the battery power necessary for the retention as small as possible. The emulator principle described here can be used on another microcomputer machine with another processor in the desired application. In this case, the load program must, of course, be created in the respective assembler mnemonic of the microcomputer being used and also in the corresponding cross-assembler (if necessary) for the processor in the desired application at hand.

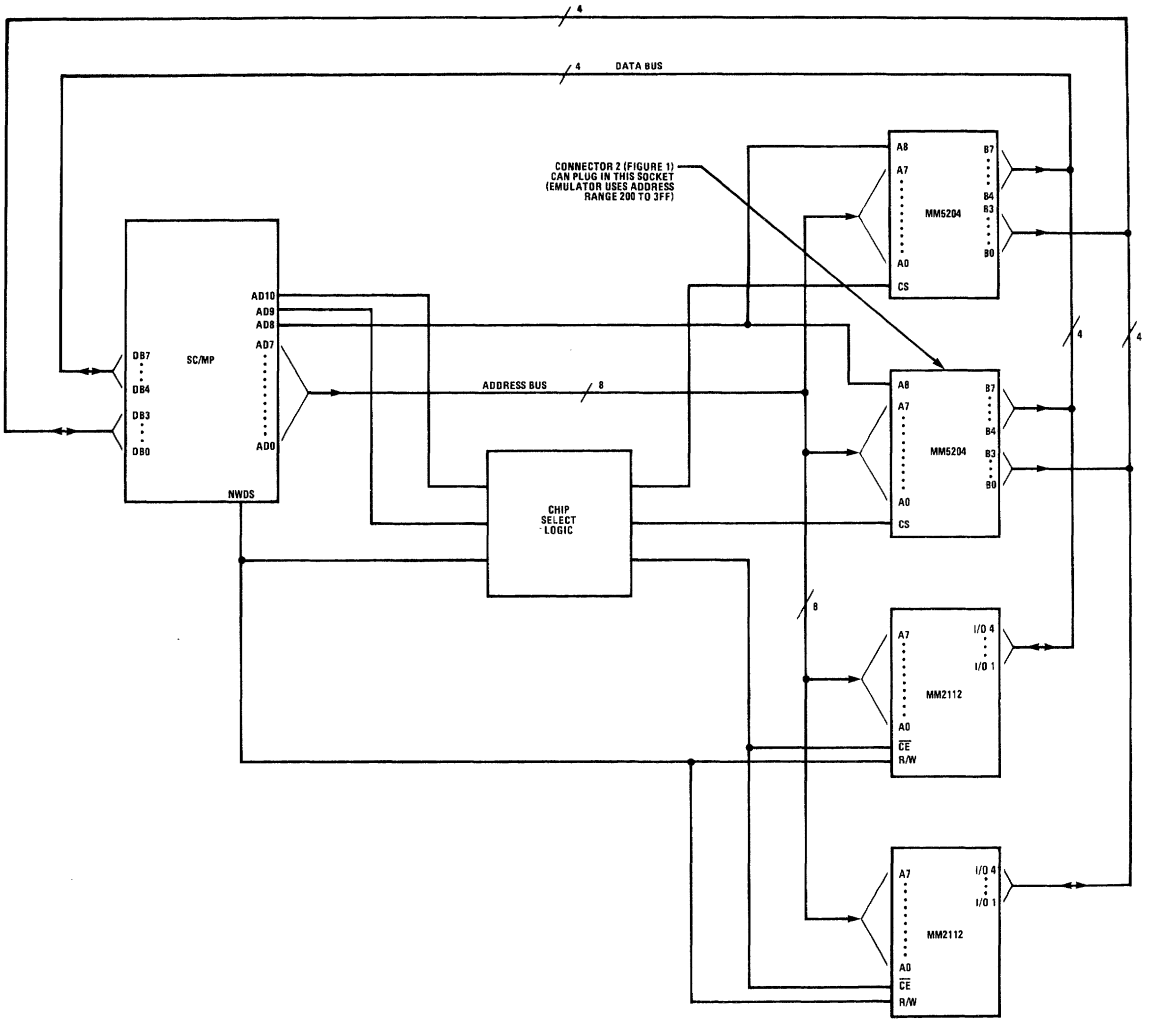


Figure 2. Memory Configuration of SC/MP Introkit Showing PROM/ROM Emulator Connection

Custom ROM Programming

National Semiconductor
Application Note
Bill Johnston

INTRODUCTION

National Semiconductor Corporation uses a computerized system to service customers with accurate, fast-turnaround processing of custom ROM orders. This system is called the Mask Programming System (MPS). It provides (1) easy customer interface, (2) fast turnaround, (3) automatic error checking, and (4) pattern verification. The following discussion describes the MPS input formats and procedures allowing the customer to utilize the system efficiently.

This application note applies specifically to ROMs. The general approach is the same for the many other types of circuits produced by NSC which utilize the MPS, but their unique requirements are not covered here.

MPS FORMATS

GENERAL

The MPS is designed to convert custom ROM programs into machine language, accomplish error checking and data processing, and then output magnetic tapes and a verification listing. The magnetic tapes are used for mask production and test tape generation. Technically, the MPS includes the CALMA and DAVID MANN systems used in generating "masters" and "working plates." These "working plates" are the masks used in fabricating the wafers with a custom ROM pattern.

The MPS will accept several formats, but using the standard MPS format will eliminate preprocessing steps. This will reduce turnaround time and decrease the possibility of error.

DEFINITIONS

Logic Definitions

Negative Logic:
A logical "1" is the more negative logical voltage level.

Positive Logic:
A logical "1" is the more positive logical voltage level.

Usually bipolar ROMs and N-channel MOS ROMs are electrically specified in positive logic. This means their data sheets will indicate a logical "1" is the more positive logical voltage level for inputs (addresses and chip selects/enables) and for outputs. Conversely P-channel MOS ROMs are often electrically specified in negative logic. This means their data sheets will indicate a logical "1" is the more negative logical voltage level for inputs and outputs. The MPS is designed to generate programs consistent with the *electrical specifications* of the "1" and "0" logic voltage levels of each device type. ROM program data may be submitted with either logic definition *but* the MPS will automatically complement the data (addresses, outputs, and chip selects/enables) when the logic definition of the submitted data does not match that of the data sheet. *The customer must specify which definition has been used when submitting a program.* Mixed definitions, positive for inputs and negative for outputs, or vice versa, cannot be used.

I/O Definitions

Addresses:
A_0 is the least significant address bit. (Some earlier types have no A_0 and start with A_1 as the least significant address bit.) L_0 is the least significant line address bit and A_0 is the least significant character address bit in character generators. The highest address subscript indicates the most significant address bit. (Some control pins have been labeled like address pins, e.g., A_8 on the MM4221; these should not be treated as addresses.)

Outputs:
O_1 or B_1 is the least significant output bit. The highest output subscript is the most significant output bit.

CAUTION

The most frequent cause of programming errors in masked ROMs when they are chosen from a second source results from failure to describe the truth table in terms of pin numbers. Two vendors may use different names for a particular pin. For example, on a 2k x 8 ROM one might find:

	Vendor 1	Vendor 2
Pin 1	A_0	A_2
Pin 2	A_1	A_1
Pin 3	A_2	A_0

It is imperative that a one-to-one correspondence of pin numbers, not names, be used. This requires that the customer "map" (translate based on pin numbers) and "order" (put in the sequence required by the MPS) the program.

Programmable Chip Select/Enable Functions

Chip Selects (MOS ROMs):
Some device types have programmable chip selection. The one-zero pattern, which selects the chip, must be specified with the same logic definition as the addresses and the outputs.

Chip Enable Options (Bipolar ROMs):
Some device types have programmable chip enable options. The customer must select the desired option from the data sheet.

Terms

TB:
The total number of "1" bits in a column expressed in decimal.

SUM:
The total number of "1" bits in a row (output word) expressed in decimal.

ORDER INFORMATION

The following information must be submitted with each custom ROM program. An order will not be processed unless it is accompanied by this information.

		NATIONAL PART NUMBER
		ROM LETTER CODE (NATIONAL USE ONLY)
NAME		DATE
ADDRESS		CUSTOMER PRINT OR I.D. NO.
CITY	STATE ZIP	PURCHASE ORDER NO.
TELEPHONE		NAME OF PERSON NATIONAL CAN CONTACT (PRINT)
AUTHORIZED SIGNATURE		DATE

LOGIC DEFINITION:

☐ POS (positive logic on addresses, outputs, and chip select/enable)

☐ NEG (negative logic on addresses, outputs, and chip select/enable)

CHIP SELECT ONE-ZERO PATTERN (MOS ROMs):

Show the one-zero pattern that selects the chip (use the same logic as specified above). Write N/A in each space where this is not applicable. (Chip enables should be treated as chip selects, e.g., CE1 = CS1, CE2 = CS2, etc.)

CS1 =

CS2 =

CS3 =

CHIP ENABLE OPTION (BIPOLAR ROMs):

Choose the desired option from data sheet and enter the option number here. Write N/A if not applicable.

OPTION NO. _____

PAPER TAPE DEFINITION
(BINARY COMPLEMENT OR BINARY ONLY):

A punch equals

☐ "1"

☐ "0"

☐ N/A (Check N/A if not used.)

Figure 1. Order Information Form

STANDARD FORMATS FOR ⩽ 1k WORDS

Cards

Cards are the first preference for data entry for ROMs with up to 1024 addresses (words). Data entered on cards in the MPS format can be directly processed by the MPS with no additional processing and all information can be checked for errors/omissions automatically. Should a correction be necessary, only a single card (or a few) need be changed.

The following coding forms show the MPS card format with its minor variations depending on the number of outputs. See figures 2, 3, and 4.

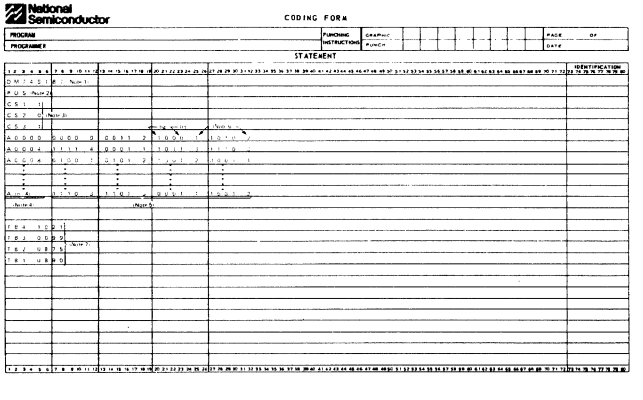


Figure 2. MPS Card Format for ROMs with 4 Outputs

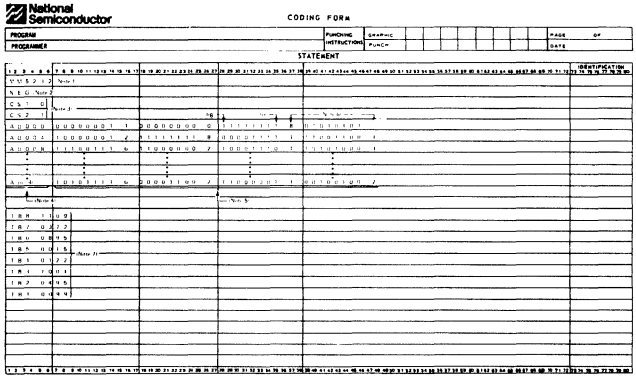


Figure 3. MPS Card Format for ROMs with 8 Outputs

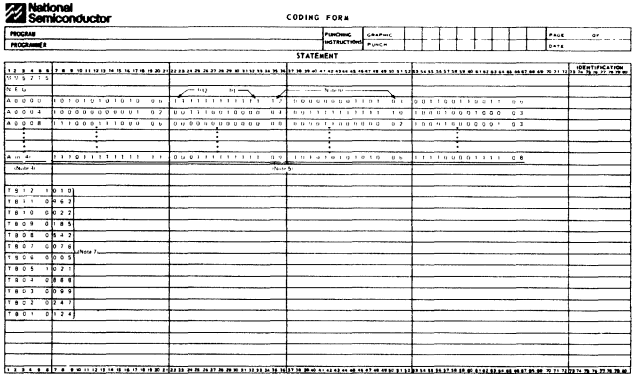


Figure 4. MPS Card Format for ROMs with 12 Outputs

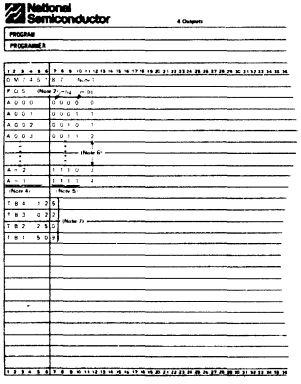
Notes:

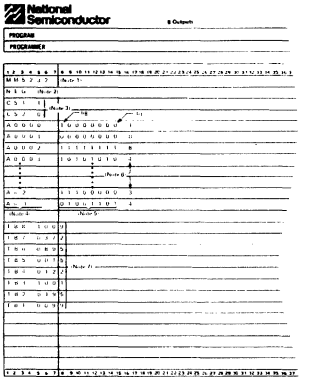
1. Specify product type including the two-letter prefix — DM for bipolar ROMs or MM for MOS ROMs.
2. Specify the type of logic — either positive (use POS) or negative (use NEG). See the "Definitions" section for further explanation.
3. Some MOS ROMs have programmable "chip select" codes. Show the logic level for each chip select that will select the ROM. Use the same logic definition (NEG or POS) as chosen for the addresses and outputs. If no programmable chip selects are involved, make no entry. Chip selects are numbered from 1 up; they do not start with zero.
4. The first ROM input address *per line* (per card) is entered in decimal form and preceded by the letter A. The first address is zero. Leading zeroes must be shown (punched).
   Use:
   AXX for 0 to 63 addresses
   AXXX for 0 to 511 addresses
   AXXXX for 0 to 1023 addresses
   The last address shown will be n - 4 where n = number of addresses (output words) of the ROM.
5. *All addresses must be programmed.* Four output "words" (addresses) are entered per line (punched per card).
   The number of "data" cards is equal to the total number of addresses divided by 4.
   Use the same logic definition (NEG or POS) for outputs, addresses, and chip selects.
   The least significant output bit (b_1) is entered on the right. This is the logic state of output 1 for a given address. The most significant output bit (b_4, b_8, or b_{12}) is entered on the left. This corresponds to the logic state of the highest order output for the corresponding address. Outputs are numbered from 1 up; they do not start with zero.
6. The total number of "1" bits in the output word is entered one space after the output word. This is for error checking. Leading zeros must be entered for ROMs with 12-bit output words.
7. The total number of "1" bits in each output bit position (column) is entered. Leading zeros must be entered (punched). Four digits are shown for 1024 addresses, but only 3 are necessary for 512 addresses, and only 2 are necessary for 64 addresses. The last 4, 8, or 12 cards, depending on the number of outputs, will show these sums for error checking.

Paper Tape

The second preference for data entry is paper tape using the MPS format. Using the 7-bit ASCII code on 8-punch tape allows customers to utilize more readily available equipment. This also allows direct entry into the MPS complete with automatic error checking. The disadvantages are the length of tape required with larger ROMs and the requirement of making a complete new tape to correct errors.

The format is essentially the same as for cards except that each address is punched together with the output word. The following coding forms (figure 5) show the MPS paper tape format.





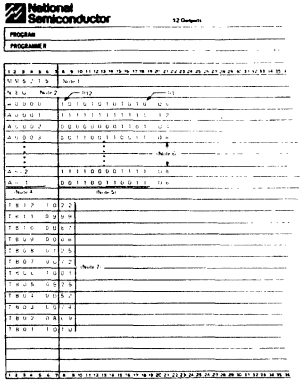


Figure 5. MPS Paper Tape Format

Notes:

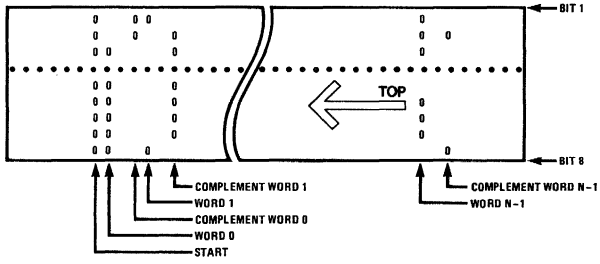
1. Specify product type including the two-letter prefix – DM for bipolar ROMs or MM for MOS ROMs.
2. Specify the type of logic – either positive (use POS) or negative (use NEG). See the "Definitions" section for further explanations.
3. Some MOS ROMs have programmable "chip select" codes. Show the logic level for each chip select that will select the ROM. Use the same logic definition (NEG or POS) as chosen for the addresses and outputs. If no programmable chip selects are involved, make no entry. Chip selects are numbered from 1 up; they do not start with zero.
4. Each ROM address is entered in decimal form together with the output word in binary form starting at Address zero and ending at Address n – 1, where n is the total number of addresses (output words). Leading zeros must be entered.
   Use:
   AXX for 0 to 63 addresses
   AXXX for 0 to 511 addresses
   AXXXX for 0 to 1023 addresses
   All addresses must be programmed.
5. Begin the output word 2 spaces after the address. The least significant output bit (b_1) is entered on the right. This is the logic state of output 1 for a given address. The most significant output bit (b_4, b_8, or b_{12}) is entered on the left corresponding to the logic state of the highest order output. The same logic definition must be used for outputs as with address and chip selects (enables).
6. The total number of "1" bits in the output word is entered one space after the output word. Leading zeros must be entered for ROMs with 12 outputs. This is for error checking.
7. The total number of "1" bits in each output bit position (column) is entered. Leading zeros must be entered. Four digits are shown for 1024 addresses, but only 3 are necessary for 512 addresses, and only 2 are necessary for 64 addresses.

STANDARD FORMAT FOR > 1k WORDS

The binary complement paper tape format shown in figure 6 is the only standard format used with ROMs having more than 1024 addresses (output words). The preparation and handling burden of long paper tapes and large quantities of punched cards is reduced with this format as compared to the standard MPS format. It is imperative that complete order information be submitted with the paper tape! In addition, the following information should be written on the tape as a safety precaution to avoid the problem of the tape getting separated from the order information.

Company Name
NSC Part No.
A punch = ("1" or "0")
This is logic (POS or NEG)
Chip select information if applicable

As shown in figure 6, the tape has nothing on it except a RUBOUT character to indicate the start and the data. There are two words of data per address: first the actual data followed immediately by the complement of the data. For example, the figure shows word 0 as 11111100 (LSB on the right, a punch equals a "1") and its complement immediately following it as 00000011.



Note 1: Tape must be all blank except for the data words.
Note 2: Tape must start with a rubout character.
Note 3: Data is comprised of two words, the first being the actual Data and the second being the complement of the data.

Figure 6. Binary Complement Format

NON-STANDARD FORMATS FOR MPS DATA ENTRY

General

The definition of a non-standard MPS format is one which requires additional processing (preprocessing) to translate it into the MPS format. This additional processing increases the possibility of error and has the undesirable side effect of increasing the turnaround time. *Whenever possible, use the standard format.*

The order information described in the "Order Information" section and the definitions in the "Definitions" section apply to all of the following non-standard formats. See figures 7, 8, and 9.

Address	Output Code MSB b_4	b_3	b_2	b_1 LSB	Sum
A000					
A001					
A002					
A003					
A n-2					
A n-1					
TB					

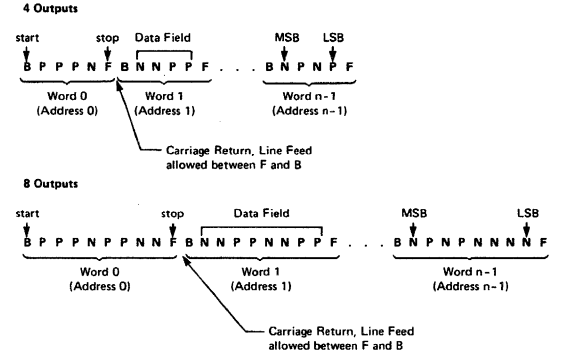
Address	Output Code MSB b_8	b_7	b_6	b_5	b_4	b_3	b_2	b_1 LSB	Sum
A0000									
A0001									
A0002									
A0003									
A n-2									
A n-1									
TB									

Address	Output Code MSB b_{12}	b_{11}	b_{10}	b_9	b_8	b_7	b_6	b_5	b_4	b_3	b_2	b_1 LSB	Sum
A0000													
A0001													
A0002													
A0003													
A n-2													
A n-1													
TB													

Figure 7. Truth Table Formats

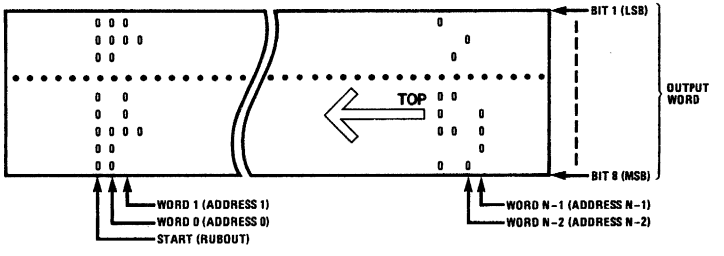
Paper Tape Formats

Figure 8 shows the BPNF paper tape formats. Here the data field must have only Ps or Ns between B and F. No other characters (no NULLs or RUBOUTs) are allowable between B and F. There must be exactly 4 or 8 P and N characters per word. Except for B and F, characters between an F stop character and a B start character will be ignored, including RUBOUTs. Errors may be corrected by rubbing out Bs and Fs of the word in error and entering the corrected word. Data for the entire n output words (0 to n-1 addresses) must be entered. Figure 9 shows the BINARY paper tape format. The order information must indicate whether a punch equals "0" or "1." THIS IS THE LEAST RELIABLE FORMAT. IT HAS NO ERROR CHECKING AND SHOULD BE AVOIDED IF AT ALL POSSIBLE.



Note: P="1", N="0"

Figure 8. BPNF Paper Tape Formats



Note: Start with a RUBOUT and enter the output words in sequence from word 0 (address 0) to word N-1 (address N-1). There must not be *any* other characters on the tape. THIS FORMAT IS THE LEAST RELIABLE.

Figure 9. Binary Paper Tape Format (8 Outputs Only)

Hardware (Firmware) Format

Often a system is prototyped and checked out with PROMs or EPROMs prior to committing to a mask programmable ROM. NSC can accept the program resident in a PROM or EPROM or multiples of these for very large ROMs like the MM2316E and the Maxi-ROM™ (MM5235) provided the following conditions are met:

1. Customer Service must give advance concurrence.
2. Patterns submitted in bipolar PROMs must be in a PROM "mate" of the desired ROM. For example, an order for a 74S97 custom ROM would require the pattern to be submitted in a 74S287.
3. Only EPROMs in current production at NSC may be used to submit custom patterns for MOS ROMs.
4. Only ROMs equivalent in electrical characteristics and with the same pinout may be used to submit custom patterns for NSC ROMs.

The verification procedure is covered in the last ("Verification") section of this note. The following discussion of MM2316E data entry using 2708 EPROMs illustrates this hardware format.

MM2316E Custom Program Data Entry Using MM2708 EPROMs

NSC has developed a system allowing customers to submit MM2316E custom programs in MM2708 EPROMs. The following definitions and serialization must be followed to eliminate delays and errors in the data entry phase of the generation of custom programs.

Positive Logic is Preferred: Positive logic is defined as follows: a logic "1" is the most positive logic level and a logic "0" is the most negative logic level. When this definition is applied to the MM2316E and the MM2708, the following definitions result:

A "1" = V_{IH} for addresses and chip selects.

A "1" = V_{OH} for outputs.

A "0" = V_{IL} for addresses and chip selects.

A "0" = V_{OL} for outputs.

This logic definition must be used for all pins on both device types. Any other logic definition (or combination of definitions) will result in delays and additional data processing steps and should be avoided.

Serialization-Identification (A Must): Two MM2708 EPROMs are required to store a custom program for a MM2316E ROM. Several custom programs may be included in a single order. The following method of serializing, identifying, and labeling is required to keep everything clearly defined:

a. Each custom program (pattern) is numerically serialized 1, 2, 3, . . . n.

b. The two MM2708s storing a custom program are designated "A" for the first block of 1024 output words and "B" for the second block of 1024 output words. Stated another way: output words corresponding to address 0000 through 1023 are in an MM2708 designated "A;" output words corresponding to addresses 1024 through 2047 are in an MM2708 designated "B."

c. The pair of MM2708s containing a custom program *must be labeled* (stickers, paint, etc.) with a number corresponding to the program and a letter designating which block of output words it contains. For example, assume three MM2316E custom programs. There would be six MM2708s sent to NSC. They would have labels on them of:

1A	2A	3A
1B	2B	3B

Verification

The customer can use software (the listing) or hardware (EPROMs) to verify the program. He will receive a verification listing and a set of EPROMs programmed and tested with tapes generated by the NSC Mask Programming System (MPS). He will be asked for a GO/NO GO response within a week after receipt of the listing and EPROMs.

The following information must be submitted with each custom ROM program. An order will not be processed unless it is accompanied by this information.

		NATIONAL PART NUMBER
		ROM LETTER CODE (NATIONAL USE ONLY)
NAME		DATE
ADDRESS		CUSTOMER PRINT OR I.D. NO.
CITY	STATE ZIP	PURCHASE ORDER NO.
TELEPHONE		NAME OF PERSON NATIONAL CAN CONTACT (PRINT)
AUTHORIZED SIGNATURE		DATE

LOGIC DEFINITION:

☐ POSITIVE (positive logic on addresses, outputs, and chip selects)

☐ OTHER (call customer service before proceeding with this order)

EPROM LABELING:

☐ Standard Format ☐ See Attached

Total No. of Programs _____ Total No. of EPROMs _____

(No. of EPROMs = 2 times No. of Programs when MM2708s are used for MM2316E custom programs.)

CHIP SELECT PATTERN:

Show the one-zero ("1" - "0") pattern that selects the chip. Use the same logic as specified above.

Program No.	(Add more if necessary.)		
1	CS1____	CS2____	CS3____
2	CS1____	CS2____	CS3____
3	CS1____	CS2____	CS3____

Figure 10. Order Information Form

VERIFICATION LISTING

The verification listing has five sections:

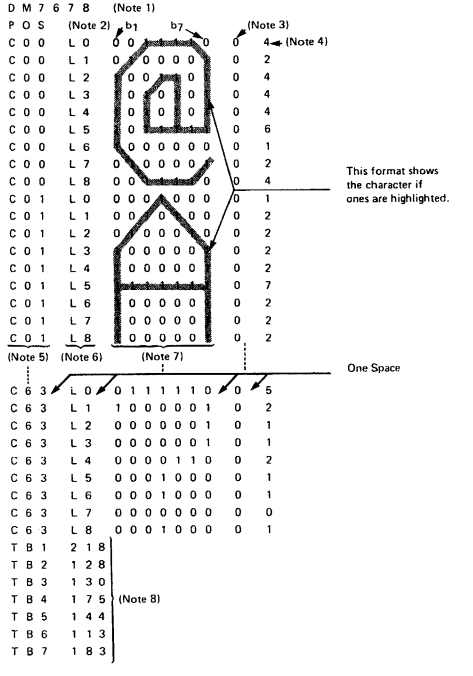
1. A cover sheet with provision for "STOP, DO NOT PROCEED" or "VERIFICATION CERTIFIED" signatures.
2. A description of the logic designations and assumptions used to process the data.
3. A listing of the data submitted by the customer.
4. An error summary.
5. A definition of the standard logic definitions for the ROM and the reduced form of the data. This list shows the output word corresponding to each address coded three ways — binary, octal, and hexadecimal.

HARDWARE VERIFICATION

When the custom program is submitted to NSC in a PROM or EPROM, the customer will receive both a verification listing and a duplicate of the original unit(s). This duplicate will have been programmed from the tapes generated by the MPS and may be verified in an operating system.

CHARACTER GENERATOR FORMAT

Character generators represent a special case of ROM custom programming. They are normally described in terms of the character address, the line address (number), and the row (dot) data. The MPS has a special program for this case. The format in figure 11 may be used with cards, paper tape, or truth table.



Notes:

1. Specify product type including the two-letter prefix — DM for bipolar and MM for MOS.
2. Specify the type of logic — either positive (use POS) or negative (use NEG). See the "Definitions" section for further explanation. Using the same definition as the electrical specification in the data sheet will result in displaying the character directly in the listing as shown in the example.
3. A tag bit is shown separately if the character generator has character shifting capability. Omit this if the shifted character feature is not available.
4. The total number of "1" bits in the line (row of the dot matrix) including the tag bit.
5. The decimal character address is shown preceded by a "C." Leading zeros are used.
6. Each decimal line address of the character is listed. This repeats for each character. All must be programmed.
7. Row data representing one horizontal row of dots at the specified line and character address. The first dot is on the left labeled b_1 and the last dot of the row is on the right. (This allows display of the character as shown in the example.)
8. The total number of "1" bits in each output bit position (column) is entered. Leading zeros must be shown.

Figure 11. Character Generator Format

How to Design with Programmable Logic Arrays

National Semiconductor
Dale Mrazek*
Mel Morris*

INTRODUCTION

A new and exciting IC device, the PLA (Programmable Logic Array), is heralding a new era of circuit compression comparable to the introduction of medium scale integration devices in the days when gates and flops were the only digital building blocks available.

As the name suggests, a PLA is an array of logic elements such that a given input function produces a known output function. In this sense, the device could be as simple as a gate or as complex as a Read Only Memory (ROM). Applications range from the slowest and smallest systems, such as traffic light controllers, to fast, high performance and complex large digital processors. In the following sections, the PLA will be described and its advantages over alternate logic forms demonstrated.

WHAT IS A PLA?

Since there is a difference between a Programmable Logic Array (PLA) and a rectangularly structured Read Only Memory (ROM), the PLA should be described. Even though any input code can be decoded to any output code in the PLA, not all possible input combinations are possible within the same package. The numbers of inputs to a PLA are much more than would be available with ROMs (Figure 1). In the case of the DM8575/DM8576 there are 14 inputs and 8 outputs. This would relate to ROM with 2^{14} or 16,384 words. This PLA (DM8575/DM8576) has 96 equivalent words. These terms are called partial product terms. Each product term can be described as a logical AND function which relates to a protion of the total output terminal solution. Each product term can be programmed to any complexity up to the input limit of the PLA. The DM8575/DM8576 PLA may have 14 variables in its product term or it may only have one input which establishes the product term. The PLA logically can be described as a collection of "ANDs" which may be "ORed" at any of its outputs. Figure 2 shows the logical data flow from the 14 address input terminals through the "AND" gate to the "OR" gate and to the output terminal.

The large variation in the partial product terms possibilities of the 14 input variables are shown below:

$$P_1 = I_1\, I_6\, I_7\, \overline{I_{10}}\, I_{14}$$

$$P_2 = I_4\, I_5\, I_7\, I_{12}\, \overline{I_{13}}\, I_{14}$$

$$P_3 = I_6\, I_{12}$$

$$P_4 = I_8\, I_9\, I_{10}\, I_{11}$$

$$\vdots$$

$$P_{96} = I_1\, I_2\, I_3\, I_{13}\, I_{14}$$

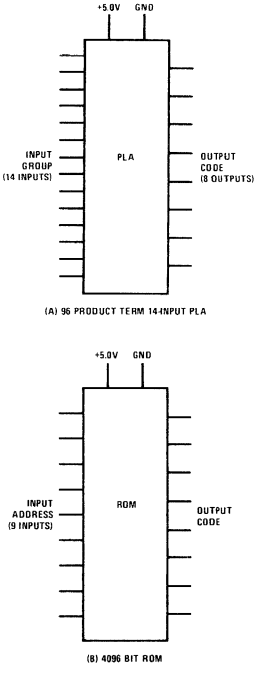


FIGURE 1.

*Refer to Preface.

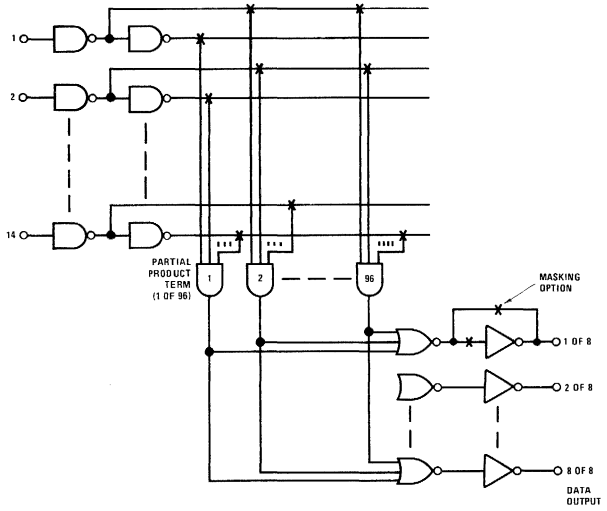


FIGURE 2.

It is possible to combine or collect by mask option any of the product terms for any of the several outputs to establish the output code combinations desired. Logically any or all of the partial product terms (AND terms) can be combined (ORed) at each output.

The equations for the output group have the following form:

$$O_1 = P_1 + P_{16} = P_{20} + P_{42} + \ldots P_{92}$$

$$O_2 = P_6 + P_{16} + P_{17} + P_{42} + \ldots P_{52}$$

$$O_3 = P_1 + P_{20} + P_{36} + \ldots P_{96}$$

Each of the partial product terms labeled P_1 through P_{96} are shown as they appear at each output. Note that the same product term may be used in as many output equation groups as required. It can be seen that P_1, the first product term, is used in both outputs one and three and P_{16} and P_{42} are used in outputs one and two.

A PLA need not have more than one output but it is generally more efficient to build the PLA or ROM with more than one output. The PLA in this discussion has eight output terminals which reflect the silicon efficiencies of today's technology. This product has the ability to be masked with outputs in either a positive true state or a negative true state. (Figure 2) These capabilities enhance the elements value when applied to the system solution since the inverter at the output terminal is not required.

To use this memory storage device, the memory storage equations must be written or tabulated so they can be stored within the mask programmed element. A large number of possible choices exist when the equations or product terms are collected at the outputs. The system designer must test the possible choices to be used within the PLA. He should combine all mutual terms within the same package. Commonly grouped product term adds to the efficiency of the PLA or PLA array as indicated in the previously mentioned equations.

WHY A PLA?

The application of the PLA in a digital solution is a natural evolution in system design. Several years ago digital systems were designed with gates and dual D memory elements. The system at that time, was conceived and implemented in its best possible way. A later development in system design utilized ROM's to provide the complex decoding for the control necessary to satisfy the same system design objective. Now we are in a new era. The design of the same system control function can be achieved by utilizing the desirable characteristics of the PLA (Programmable Logic Array). The reason for this evolution of design is based upon one or more of three possibilities. First, the new design will yield a higher performance solution. This generally relates to an improvement in system dynamic performance because fewer levels of logic are required to provide the same control function. Second, the design will result in a lower parts cost. This is due to the more efficient use of the memory array as compared with the normal rectangular array ROM. The third possible advantage comes from the reduction in system manufacturing cost brought about because of the reduction in component assembly cost, the reduction in printed circuit board cost or possibly connector cost within the system. Each time a system's physical size can be reduced by the use of more complex elements such as a PLA (Programmable Logic Array) the cost of that system decreases also because fewer cards and connectors are required.

THE PLA AS A CODE CONVERTER

Being a device, which from its input terminals produces outputs in accordance with a predefined set of rules, a PLA can be viewed as a memory storage device (i.e., a limited capability ROM). Hence, if all the partial product terms for a particular code conversion can be limited to the 96 available, then the PLA could be used in this application.

Recall that a product term consists of a combination of input variables which can represent a characters code, then the code conversion is possible for a 96 character set. Take the case of 12-line Hollerith to 8-line ASCII conversion as an example. Theoretically, 12-line input represents the possibility of 4k words. Actually, seven of the 12 Hollerith lines are not binary coded lines, they are ordinary decimally coded lines. So that a ROM structure with 12 input lines are not used, these seven lines must first be encoded to 3 binary lines using additional logic elements prior to being presented into a common 8-input ROM (Figure 3A). In addition, the 12-input ROM would have to decode all the non-existent input possibilities into don't care (or error) output states.

The PLA solves this problem efficiently. All 12 inputs are presented to the PLA. Since selective decoding is a feature of the PLA no provision need be made for pre-encoding of the inputs (Figure 3B).

An invalid input is designed to produce an all-high output state by virtue of the fact that it is not a recognizable product term.

THE PLA AS A DECODE ELEMENT IN A DIGITAL PROCESSOR

Why does it naturally follow that the PLA lends itself to the control function of a digital processor or other simularly organized system? Many processor oriented systems have control instruction codes which are much wider (a large number of inputs bits) than that which can be easily satisfied with ROM's.

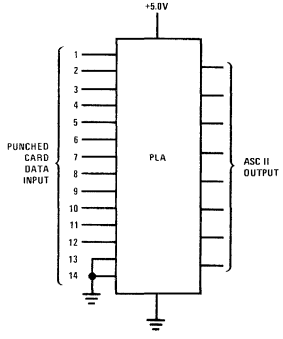


FIGURE 3B.

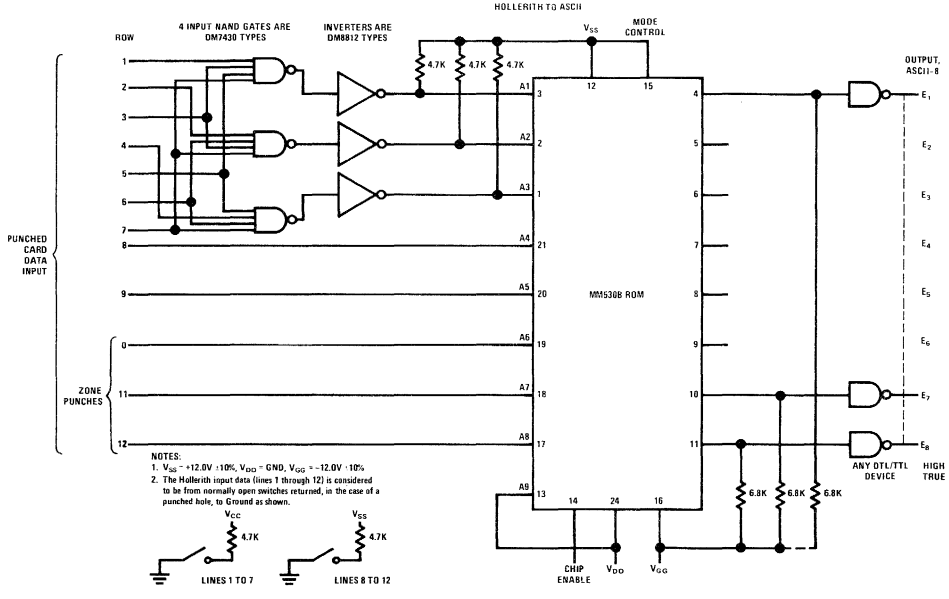


FIGURE 3A.

These types of applications have nine to eleven logical control code inputs. The timing code is also significant since the input instruction code must be logically "ANDed" with timing to form the output control signals. This results in a total input control group of eleven to thirteen bits to effect output control. Standard ROM's can be used to solve the the design problem. They have been used in the past but at the expense of system in component expense and generally in dynamic performance. If a complete input to output decode is solved, the cost of the complete ROM array is quite expensive. Two levels of logic are required to decode the proper ROM element group and enable the input data word to propagate to the output terminals (Figure 4). The technique is generally quite expensive since the quantity of ROM elements can be large.

In actual system use, not all combinations of codes of instruction data and timing data are used therefore, it is possible at times to use data compression techniques to reduce the number of ROM's necessary to store the output data. The technique normally used is to multiplex the required codes into the ROM elements as required by timing or a particular section of the input code group.

An example of such a multiplexer data decoder solution using ROM's is shown in Figure 5. Note that this solution technique uses two levels of multiplexers (DM74153's) to route the proper data to the ROM group. The use of these multiplexers significantly reduces the number of ROM's required but adds to the delay time to achieve the proper output levels. This technique also requires many engineering hours to first achieve a solution and even more to effect a change.

All five multiplexers and a ROM element are used to precode the inputs V of A PDP-8 system control ROM set.

A PLA solution would simply involve generating the logic equations for the outputs, isolating the common product terms, and implementing it in a masked PLA. Figure 6 illustrated how a PLA solution might look for the same 20-bit output word structure. The advantages of this approach are obvious.

First, the PLA design yields a higher performance solution. System dynamic performance will improve due to the reduction of signal paths interconnections and signal skewing. Secondly, a ROM solution is inefficient, requiring more silicon than is necessary to do the job and hence higher cost. Lastly, a reduction is effected in manufacturing costs due to the reduction in component assembly cost, P.C. Board cost, and interconnection cost.

THE PLA AS A SEQUENTIAL CONTROLLER

Another system application of the PLA is in sequential controllers. A sequential controller usually requires that a random set of input variables occur simultaneously to satisfy the condition of a particular state. This condition then allows advancing to the next controller state of the sequencer. An illustration of the use of the PLA in a sequencer application is that of a traffic controller. Referring to Figure 7, it is assumed that traffic can flow at high rates in any of four directions. It is also assumed that each direction has a left turn internal and that there is also provision for manual inputs to the system. It is also required to modify the timing interval depending upon the detected flow rate in any direction. The PLA is used as the controller for this adaptive sequence timer.

It would be possible to start the sequence within any of its possible status. While in each state, the other possible states are scanned to determine if the present state should be shortened or made longer in the example case, states B, C and D are checked as to the traffic status while the sequencer is in state A.

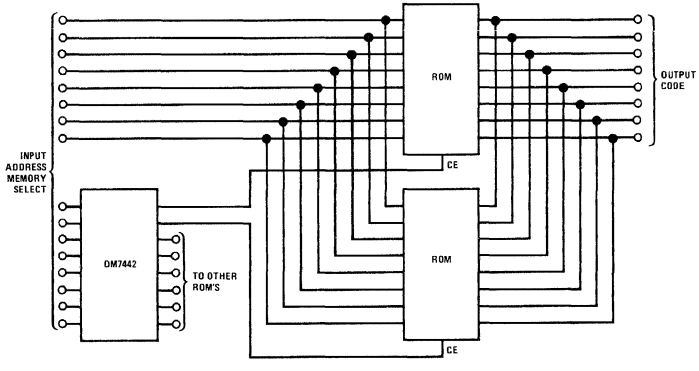


FIGURE 4.

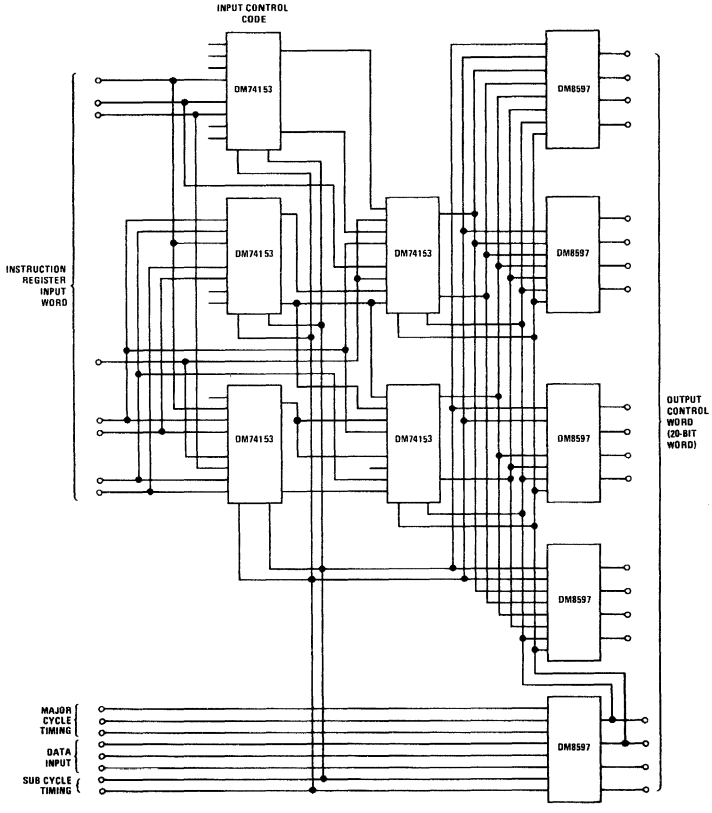


FIGURE 5.

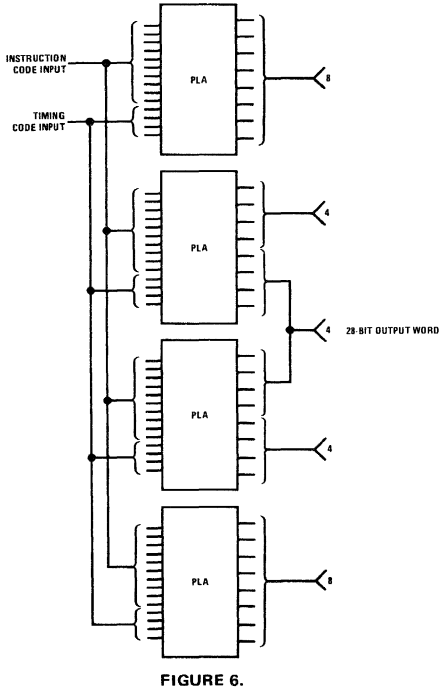


FIGURE 6.

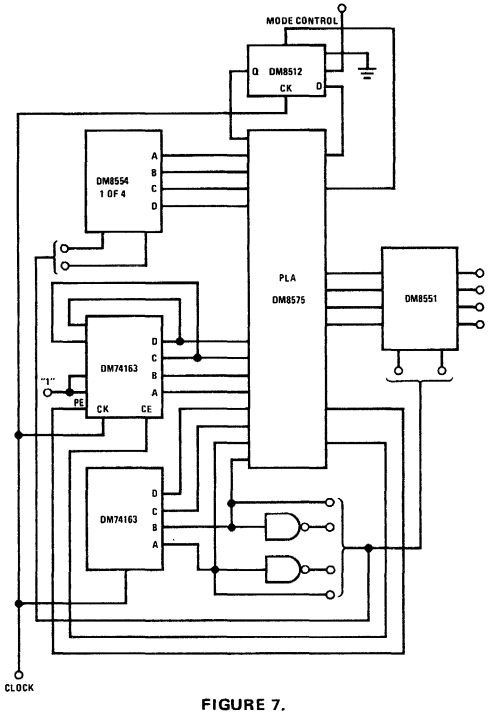


FIGURE 7.

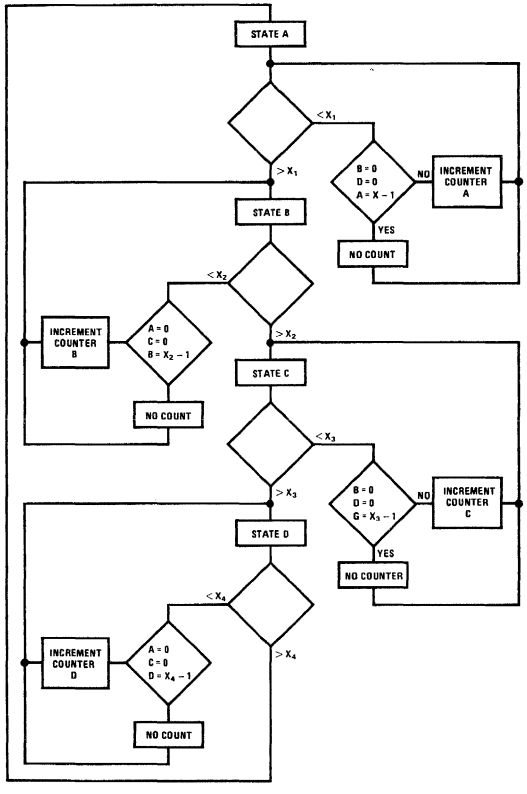


FIGURE 8.

Note that the state diagram Figure 8 shows that the maximum time interval X is checked to be greater than the present value of the A elapsed time counter. If this is true, the state counter indexes to the next machine state (state B). The output data transmitted to the holding memory (DM8551's in Figure 7) will be changed with every state step in the system. The four packages of holding memories are used to store the control information for the traffic indicators. The memories (DM8551's) are sequentially updated by using the same scan decoder which is used as a multiplex decode of remote traffic counters (DM85L54's).

The control coding developed allows a state interval to be shortened because one of the cross streets has detected on coming traffic. Also, the state interval can be lengthened if no cross or left turn traffic is detected. As the sequencer steps from state to state the other state conditions are tested. In other words, while in state B state conditions for A, C and D are tested for the necessary conditions which might modify the timing of state B. The four traffic counters which are shown in Figure 7 as DM8554 elements are multiplexed sequentially into the PLA sequencer controller where they are logically "ANDed" with present state timing. Using this information the sequencer period is modulated per the equations defined by the state equations.

It should be noted that the sequence order need not be orderly. The sequence of states through a complete cycle may have repeat intervals or jump commands in any step within the vastly variable complete sequence loop. There is no special requirement that the sequencer be designed with order in mind if some sort of disorder will yield an improvement in performance. The performance advantage may relate to a dynamic performance improvement or it may relate to a cost performance improvement. Generally a cost improvement results when fewer parts are required in the overall solution.

DESIGNING WITH A PLA

How should a PLA solution be developed? An orderly approach to the solution is necessary when the control word is wide and complex in form. The following techniques may be of some help in determining the decode combinations when using a PLA solution.

1. List all input control codes which are required for each output.
2. Reduce this list logically to minimize the number of partial product terms.
3. Combine similar terms which may be used on more than one output terminals.
4. Group outputs which can share the largest percentage of the same partial product terms.

There are some additional considerations with the general solution. Let's assume the following problem. The input control code is 14-bits wide and the output control word is 28-bits wide, Figure 9. This means that we would use four PLA's to generate the decoder solution if none of the packages required more than 96 partial product terms. In our example assume that there are four output codes which have 90 partial product solutions without considering the terms required by the four other output terminals of the PLA under question.

The initial thought about solving this problem, would suggest the use of an additional PLA with inputs and outputs connected together to obtain the extra product terms. Since the four PLA's have a total of 32 outputs and only 28 are required, the 4 unused additional outputs may be coupled from a second PLA to the PLA which first contained the 4 high usage partial product groups of terms (Figure 9).

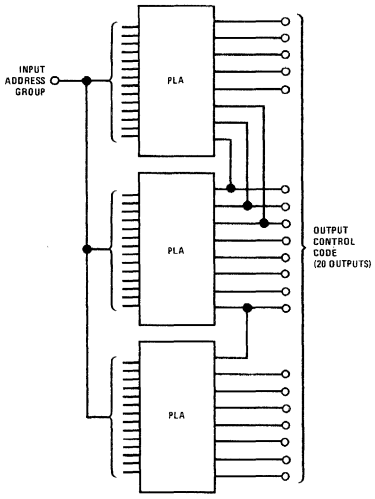


FIGURE 9.

Doing this allows half of the partial product terms to be placed in each of two separate PLA's. PLA's can be connected with common inputs and common outputs. It should be noted that the output code for the common terms must be programmed using a negative true logic for, since this permits "wire-OR'ing" the outputs. This very significant design possibility would not be allowed if standard ROM techniques are used.

This interesting observation shows that memory expansion for this product (PLA) is different than other memory elements. The normal Read Only Memory (ROM) or Random Access Memory (RAM) elements have chip select inputs which must be decoded and selected before the package is activated. When these types of memories are expanded, additional decoder logic elements are required to select the proper memory array Figure 4. In case where there are more than one output terminal,

it is necessary to activate the entire package group and therefore an entire memory word must be used for the address.

Neither of these conditions are necessary for the PLA. If the partial product does not exist as a decoder or programmed condition, the outputs do not change but if that product term does exist the outputs respond to the solution. In the PLA case it is possible for any one or combination of outputs to be selected from different but mutually connected packages (Figure 9). This element technique of grouping common control codes can simplify the solution. The technique may be used with multiple outputs to any degree which can prove economically efficient to the system design.

This last technique is a variation of items 3 and 4 in the design suggestions listed earlier. Utilization of this technique can result in significant improvements in memory storage efficiencies when compared different PLA solutions.

CONCLUSION

The two example applications, that of the control decoder within the digital processor and the traffic light sequencer, show the economic advantages of using the PLA because a reduction in circuit complexity and quantity results. The processor example application results also in an improvement in dynamic performance. Additionally both of these examples have a convenience of design which allows the system's work function to be modified without changing the overall system. Only a change of PLA programming need be accomplished to change the function of the decoder or controller system.

There are many more design ideas which will become apparent within your system when the PLA is applied to the system design. More design flexibility than that available with the ROM or random logic design can be achieved with the application of PLA elements to the system. The overall result will be more logic function per system dollar.

Section 5

PROMs and EPROMs

5

Field Programmable Read Only Memory has made a remarkable impact upon the art of logic design. Not many years ago the instruction sets of minicomputers were defined in combinatorial logic; today such definition is accomplished with PROM in microcode. The practical application of microprocessors could not be possible without EPROM. Because the in-circuit function, aside from speed considerations, is exactly the same for PROM and EPROM, the two are combined in this section. It may pay to occasionally remind oneself that MOS EPROM can do logic functions and that bipolar PROM is quite usable as microprocessor instruction store.

A Guide to Implementing Logic Functions Using PROMS

National Semiconductor
Application Note
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"The cost per bit of read only memory has declined to the point where ROMs or PROMs are competitive with gates." Most of us have heard this statement accompanied by estimates of the number of bits equivalent to a gate. These statements and estimates are only valid if efficient use is made of the memory. Efficiency of use is defined as the number of memory bits used to realize a function compared to the number of bits available. This application note intends to illustrate some techniques which allow the designer to achieve this efficiency.

No attempt will be made to derive relative costs of package counts using gates versus read only devices based on testing, insertion, and printed circuit board area overhead. Current costs of PROMs, disregarding these factors, can be directly compared to those of gates. Such a comparison shows that bipolar PROMs can be used at very low efficiencies and can be extremely competitive. The following table reflects efficiencies required based solely on purchase price.

Table I. Efficiency[1] Required in PROM Use to Effect Cost-Effective Replacement of Gate Solutions

PROM Size	Efficiency
256 bits	10 - 15 %
1024 bits	4 - 6 %
2048 bits	3 - 5 %
4096 bits	4 - 6 %[2]

Notes:

1. Percent efficiency has been calculated based on gate equivalencies of PROMs.
2. As production experience is gained, efficiencies required for replacement will decrease.

Efficiencies may drop dramatically if MSI replacement occurs. An analysis shows that if the circuit depicted in figure 10, using a 1k PROM, replaces the conventional MSI/gate solution with equal component cost, the PROM need only be used at 1.56% efficiency or better.

A PROM can be considered as an array of gates. Figure 1 depicts a 2^N x M PROM as such an array. Using a 1024 x 4 device as an example, there are N(10) inputs to the array. Each of these is routed to 2^N (1024) AND gates with selectable true or false inputs. All of the AND gates provide inputs to each of M(4) OR gates with selectable true or false inputs. Other visualizations include diode arrays driven by decoders and sensed through multiplexers (figure 2).

Regardless of the technique of description, the end result is the same: *for any specific combination of inputs each of the outputs may be assigned a logic state.*

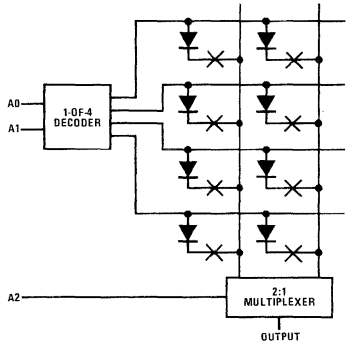


Figure 2. Read Only Device Portrayed as a Diode Array

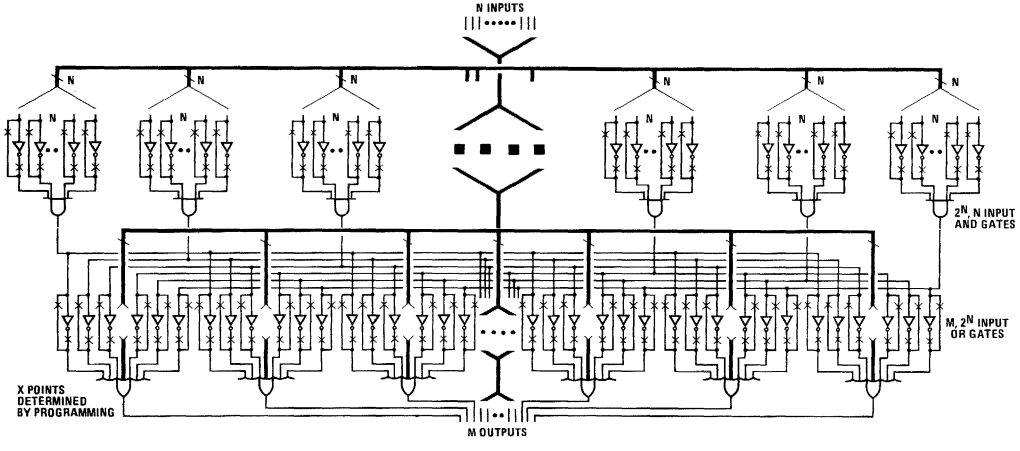
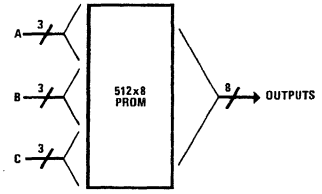


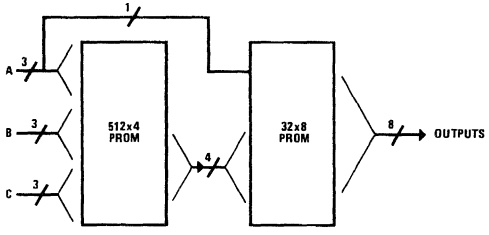
Figure 1. Visualization of a 2^N-Word by M-Bit PROM

Combinatorial Logic

When replacing combinatorial logic with PROM, two factors must be kept in mind. First, recognize the prime implicants of the equation. Too often an original design has been accomplished with a gate solution and a hasty retrofit is attempted. Unnecessary complexity may be added because the entire system has not been considered. The signals, which in a gate realization must be present, may not be important or even advisable when using a PROM. In a gate design, for example, logic signals $A \cdot B$, $A \cdot \overline{B}$, and $A+B$ may be present; only A and B are required with a PROM. Second, recognize "don't care" situations. "Don't care" states often exist in machines with multiple operating modes. For example, mode one may require signals A and B, and mode 2 may require A and C. In many systems, it is possible to pack these various states using two levels of PROM and thereby reduce end cost (figure 3).



a. Single Level Implementation



b. Two Level "Packing"

Figure 3. Reducing Memory Size by Recognizing Don't Care States

The outputs of the 512x4 PROM in figure 3b may be a packed code which does not contain the specific desired output signals, but due to the encription allows a significant reduction of the number of memory cells required. Generally, the more complex the system, the more cost-effective this technique becomes.

Synchronous Logic

In most clocked systems it is preferred that clocked devices be edge sensitive and fully synchronous. Note that in figures 4a and 4b the asynchronously cleared counter (DM74LS161) required an extra gate and flip-flop over the fully synchronous part (DM74LS163).

The need for synchronous components is basic. PROM outputs are the result of possible non-simultaneous arrival of address bits and unequal propagation delays through the PROM. This can result in output glitching. When (as in most synchronous parts) the input data need be valid for only a short interval prior to the rising clock edge, glitches following the clock transition are an allowable condition. Level sensitive components are avoided for two reasons: first, many level sensitive devices are "ones catching" (i.e., they will assume a one state should the input glitch high during the active state of the clock); second, in a system with feedback the clock strobe must be of shorter duration than the quickest propagation delay of the system. In an edge triggered design clock pulse width is not a critical parameter.

Figure 4b depicts a divide-by-N sequencer/counter. PROM output O1 determines N. O1 is normally high, allowing the counter to count successively. At address (counter output) N−1, O1 is programmed to be a zero. On the next rising clock edge the counter is cleared, O1 goes high, and the sequence repeats. The other outputs

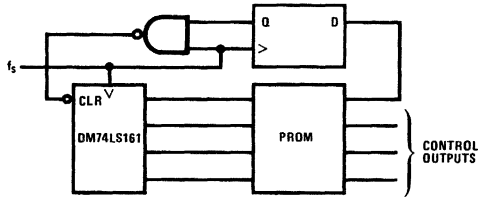


Figure 4a. Controller Using Asynchronous Device

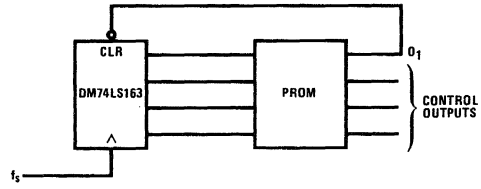


Figure 4b. Controller Using Synchronous Device

are used to drive the control inputs to logic devices. If these control inputs are synchronous or "gated D" inputs (similar to the clear input on the DM74LS163), the system clock (f_s) need never be gated through other devices. *This is a feature greatly desired.* An ungated clock is one without slivers and also one without clock-derived races. Figure 5 shows a circuit using a gated D component and the sequencer/counter of the previous diagram.

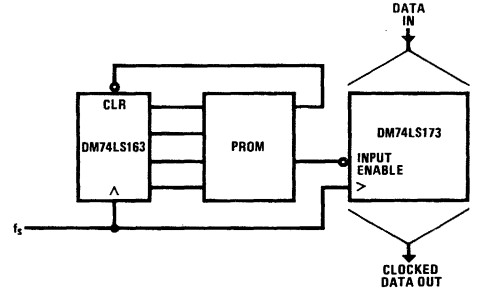


Figure 5. Gated D Control

Notice that although the clock is ungated the DM74LS173 need capture data only during the state(s) determined by the contents of the PROM and retains the data until next enabled.

Naturally, the inputs of an unclocked device may be controlled through the PROM outputs. Figure 6 depicts a multiplexer in the data path.

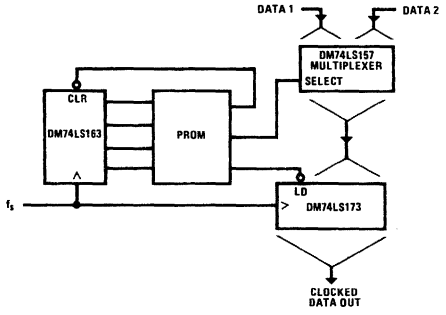


Figure 6. Sequencer Controlling Clocked & Unclocked Devices

So far the PROM has done little more than could be accomplished through the use of a gate package or two. Suppose, however, we provide the PROM with the capability to sense external conditions and allow it to determine the starting point in the count sequence by controlling the preset and data inputs of the DM74LS163 (figure 7).

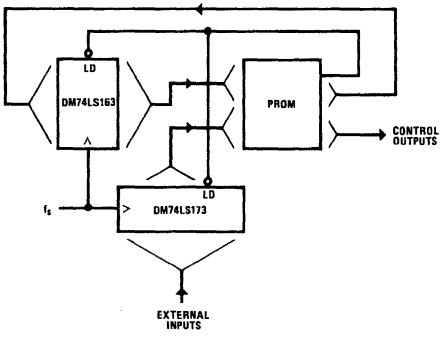


Figure 7. Determination of Next State Using External Inputs

At this point we may eliminate the count function, as the next state in the sequence may be determined by the PROM through a register (figure 8).

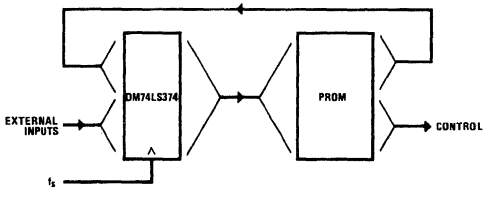


Figure 8. Elimination of the Counter

Obvious variations exist in the preceding concepts. Some examples are shown in figures 9 through 11.

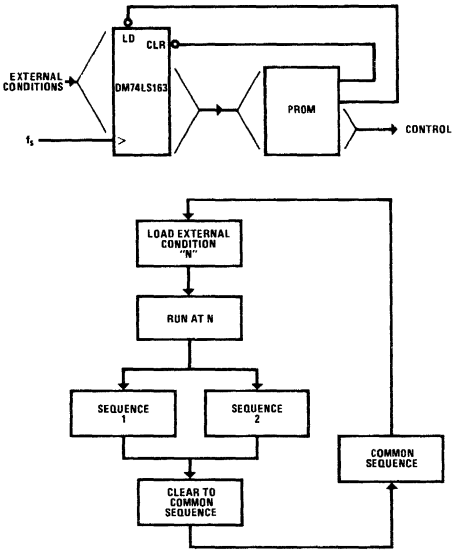
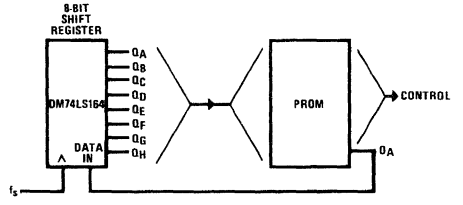
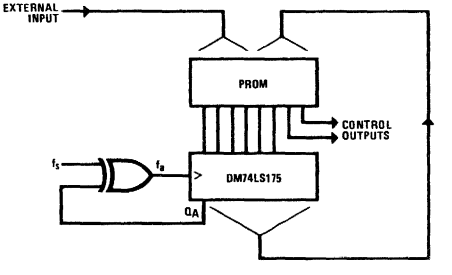


Figure 9. Control Sequence Determined by External Conditions



$$Q_A = [Q_A \oplus Q_F \oplus Q_G \oplus Q_H] + Q_A Q_B Q_C Q_D Q_E Q_F Q_G Q_H$$

Figure 10. 256-State Controller Using Shift Register & PROM



TOGGLING Q_A AT ADDRESS N ALLOWS OPERATION ON CLOCK EDGE N + ½

Figure 11. Operation on Either Clock Edge

Speed Considerations

The maximum clock speed at which these examples can operate is easily determined. The minimum allowable clock period is equal to the sum of the worst case propagation delays around the feedback loop or through the path under control, whichever is greater. Consider figure 10 as an example. The loop delay is equal to the sum of the clock-to-output delay of the shift register, the propagation delay of the PROM, and the setup time of the DM74LS164 data input. For this case,

$$\frac{1}{f_s} = t_{PHL(164)} + t_{AA} + t_{SETUP(164)},$$

where t_{AA} is the address access time of the PROM. Using a DM74S387 256x4 PROM, f_{smax} becomes more than 9 MHz. Careful attention should be paid to all AC electrical characteristics when designing for maximum speed. One parameter of special importance (in addition to those already mentioned) is data hold time. This should seldom, if ever, be a problem, but the designer should make sure that the hold time of the clocked component is significantly less than the typical propagation delay of the PROM.

In some systems the apparent speed of a PROM can be enhanced by using a technique known as pipelining. Pipelining is generally achieved through the use of a memory data latch. (Edge triggered registers are occasionally used here, but the fast fall-through time of a latch is generally preferred.) PROM output data is loaded into the latch which in turn drives the control output. While the functions under the control of the latch are being performed, a new address is accessing the PROM. Address information is changed at the same time data is loaded to the latch; therefore, system operation overlaps in time with PROM access. Obviously, care must be taken if next state information is to be provided. Two possible pipelined configurations are shown in figures 12a and 12b.

Further advantages in speed may be achieved by paralleling PROMs through a multiplexing arrangement.

Conclusion

The use of PROMs to realize logic functions can be beneficial to the system designer from a number of points of view. Some of these are:

- component count reduction
- design flexibility
- power budget economy
- device standardization

The limit of logic implementation with PROMs has, by no means, been explored to great lengths in this note. Thousands of useful, cost-effective designs have yet to be uncovered. Hopefully, this discourse will provide some impetus to the reader's own creativity.

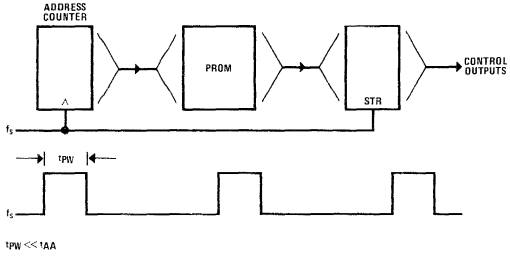


Figure 12a. PROM Pipelining Configuration #1

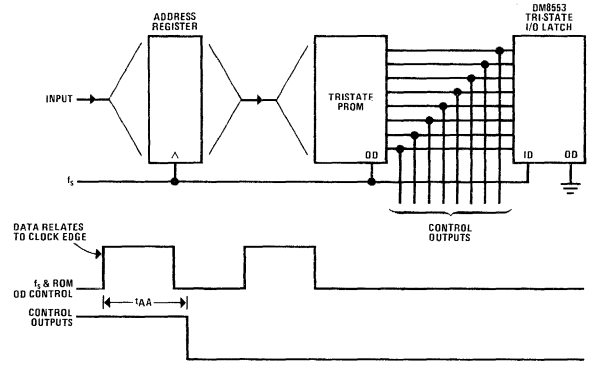


Figure 12b. PROM Pipelining Configuration #2

MOS Encoder Plus PROM Yield Quick Turnaround Keyboard Systems*

National Semiconductor
Dom Richiuso**

INTRODUCTION

Most modern keyboard designs employ MOS/LSI keyboard encoder IC's to implement all the necessary electronic functions. The key codes specified by the customer are programmed into a read only memory which is an inherent part of the encoder. Although some common encoder formats are available off the shelf, such as ASR33 teletype (MM5740AAE or MM5740AAF), there are many instances where variations of common formats are needed. Since these formats are mask programmed into the keyboard encoder, there is a certain amount of lead time (approximately 12 weeks) before a customer receives his final circuit.

By using a binary coded keyboard encoder in conjunction with a programmable read only memory, customers can build prototype keyboard systems or fill small volume orders in minimum time. This approach keeps all the encoding electronics and timing the same as in the final system, so that a minimum of redesign is necessary to configure the actual final version. This is done when the keyboard encoder with the final mask programmed key codes is received. In addition, the usefulness of being able to reassign key codes quickly in the PROM makes system debugging and alteration an easy task.

The basic configuration for this implementation is shown in the simplified block diagram of *Figure 1.* The key switches and all timing signals are configured in the normal manner. The keyboard encoder chip will emit binary codes for each valid keyswitch closure. These binary outputs are used as addresses for the PROM which is programmed with the desired actual code for each keyswitch. Each key closure is transformed first to an address by the encoder and then to the final code by the PROM. In this manner, a general design is possible, with the only variable being the contents of the PROM which is easily and quickly programmed. When changes are necessary, the PROM may be erased and reprogrammed quickly making it an easy task to finalize design alterations.

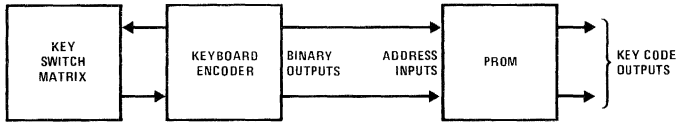


FIGURE 1. Simplified Block Diagram

***REFERENCE:** AN-80 MOS Keyboard Encoding by Dom Richiuso

**Refer to Introduction.

KEYBOARD IMPLEMENTATION

A typical implementation of this approach is shown in *Figure 2.* The encoder employs a dynamic scanning technique to identify key closures. Each keyswitch is defined by a particular X drive line and Y sense line of the encoder. In addition to the basic operation of translating a switch closure to a coded output, the MM5740

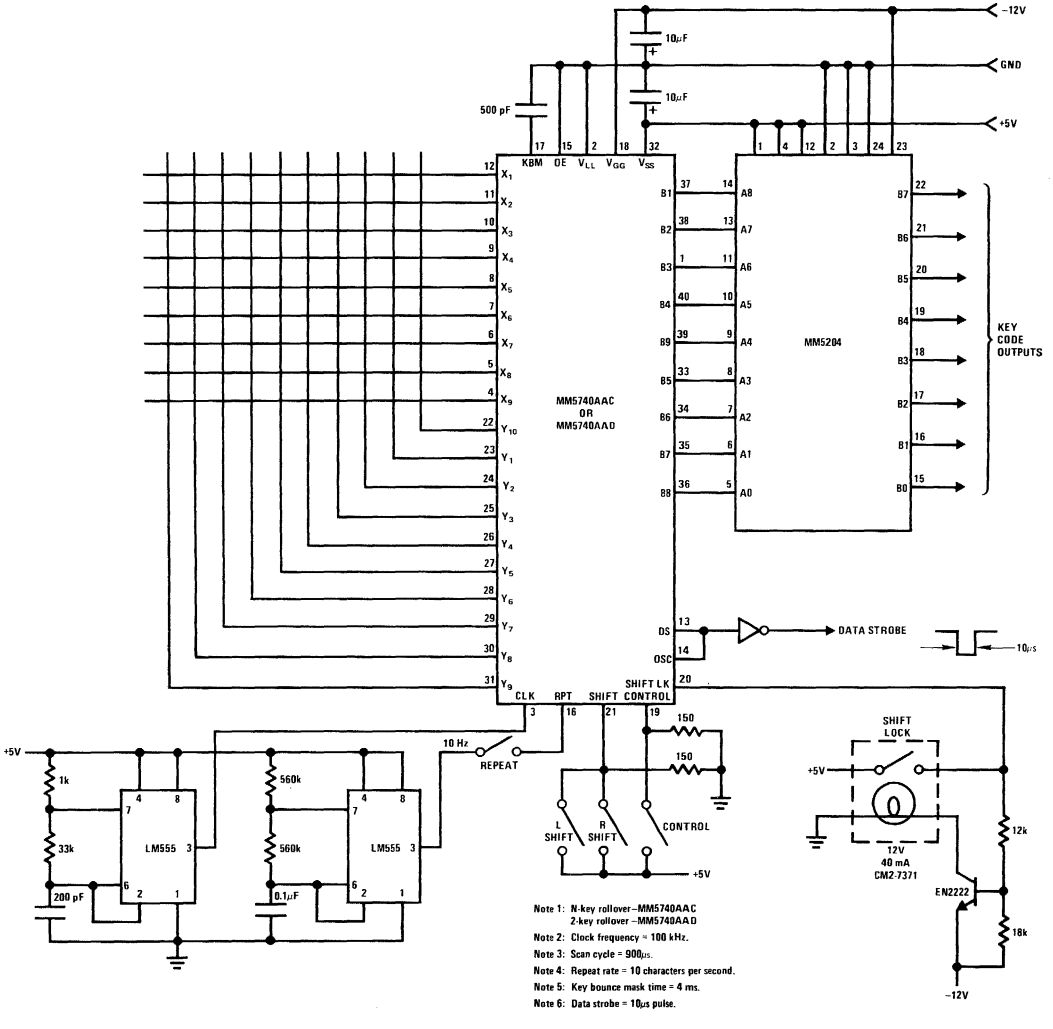


FIGURE 2. Typical Keyboard System

provides all the functions necessary for modern keyboard system design. This includes all the logic necessary for key validation, 2-key or N-key rollover, bounce masking, mode selection and strobe generation. Table I illustrates the relationship between keyswitch matrix position, key mode and the binary coded outputs of the MM5740 AAC or AAD encoder. The AAC version provides for N-key rollover while the AAD is a 2-key rollover encoder. Since there are nine X lines, ten Y lines and four modes, 360 nine-bit codes are possible.

In the general application using 90 four mode keys, a 4k PROM (MM5204) should be used. If less than 64 four-mode keys are all that is required, a 2k PROM (MM5203) may be substituted. In this case, the most significant bit (B1) from the encoder is dropped and Table I addresses would go from 0—255. When programming the PROM, it should be noted that the MM5740 uses a bit paired coding system. Any particular key will have 5 common bits (B1, B2, B3, B4, B9) and 4 variable bits (B5, B6, B7, B8) which may change when going from one mode to another. In addition, encoder coding is specified in terms of negative logic so that it may be necessary to complement positive logic PROM contents when ordering encoder masks.

By careful PC board layout, the encoder/PROM prototyping system can utilize the same PC board as the final system with the PROM removed. This can be accomplished by arranging the traces so that it is possible to provide jumpers from the encoder outputs to the PROM outputs. Utilizing this approach allows for a minimum of tooling, parts counts and quick turnaround time for new designs.

TABLE I. Encoder/PROM Mapping

	KEY POSITION		MODE	ADDRESSES (ENCODER OUTPUT)									KEY CODE OUTPUTS (PROM CONTENTS)							
	X	Y		B1	B2	B3	B4	B9	B5	B6	B7	B8	B7	B6	B5	B4	B3	B2	B1	B0
KEY 1	1	1	Unshift	0	0	0	0	0	0	0	0	0	USER DEFINED KEY CODES							
	1	1	Shift	0	0	0	0	0	0	0	0	1								
	1	1	Control	0	0	0	0	0	0	0	1	0								
	1	1	Shift Control	0	0	0	0	0	0	0	1	1								
	1	2	Unshift	0	0	0	0	0	0	1	0	0								
	1	2	Shift	0	0	0	0	0	0	1	0	1								
	1	2	Control	0	0	0	0	0	0	1	1	0								
	1	2	Shift Control	0	0	0	0	0	0	1	1	1								
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KEY 90	9	10	Unshift	1	0	1	1	0	0	1	0	0								
	9	10	Shift	1	0	1	1	0	0	1	0	1								
	9	10	Control	1	0	1	1	0	0	1	1	0								
	9	10	Shift Control	1	0	1	1	0	0	1	1	1								

*Encoder outputs are listed in positive true logic notation.

TABLE II. Truth Table
MM5740/AAC or MM5740/AAD

MATRIX ADDRESS		COMMON					UNSHIFT				SHIFT				CONTROL				SHIFT CONTROL			
		B1	B2	B3	B4	B9	B5	B6	B7	B8	B5	B6	B7	B8	B5	B6	B7	B8	B5	B6	B7	B8
1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	0	1	1	1	0	0
1	2	1	1	1	1	1	1	0	1	1	1	0	1	0	1	0	0	1	1	0	0	0
1	3	1	1	1	1	1	0	1	1	1	0	1	1	0	0	1	0	1	0	1	0	0
1	4	1	1	1	1	1	0	0	1	1	0	0	1	0	0	0	0	1	0	0	0	0
1	5	1	1	1	1	0	1	1	1	1	1	1	1	0	1	1	0	1	1	1	0	0
1	6	1	1	1	1	0	1	0	1	1	1	0	1	0	1	0	0	1	1	0	0	0
1	7	1	1	1	1	0	0	1	1	1	0	1	1	0	0	1	0	1	0	1	0	0
1	8	1	1	1	1	0	0	0	1	1	0	0	1	0	0	0	0	1	0	0	0	0
1	9	1	1	1	0	1	1	1	1	1	1	1	1	0	1	1	0	1	1	1	0	0
1	10	1	1	1	0	1	1	0	1	1	1	0	1	0	1	0	0	1	1	0	0	0
2	1	1	1	1	0	1	0	1	1	1	0	1	1	0	0	1	0	1	0	1	0	0
2	2	1	1	1	0	1	0	0	1	1	0	0	1	0	0	0	0	1	0	0	0	0
2	3	1	1	1	0	0	1	1	1	1	1	1	1	0	1	1	0	1	1	1	0	0
2	4	1	1	1	0	0	1	0	1	1	1	0	1	0	1	0	0	1	1	0	0	0
2	5	1	1	1	0	0	0	1	1	1	0	1	1	0	0	1	0	1	0	1	0	0
2	6	1	1	1	0	0	0	0	1	1	0	0	1	0	0	0	0	1	0	0	0	0
2	7	1	1	0	1	1	1	1	1	1	1	1	1	0	1	1	0	1	1	1	0	0
2	8	1	1	0	1	1	1	0	1	1	1	0	1	0	1	0	0	1	1	0	0	0
2	9	1	1	0	1	1	0	1	1	1	0	1	1	0	0	1	0	1	0	1	0	0
2	10	1	1	0	1	1	0	0	1	1	0	0	1	0	0	0	0	1	0	0	0	0
3	1	1	1	0	1	0	1	1	1	1	1	1	1	0	1	1	0	1	1	1	0	0
3	2	1	1	0	1	0	1	0	1	1	1	0	1	0	1	0	0	1	1	0	0	0
3	3	1	1	0	1	0	0	1	1	1	0	1	1	0	0	1	0	1	0	1	0	0
3	4	1	1	0	1	0	0	0	1	1	0	0	1	0	0	0	0	1	0	0	0	0
3	5	1	1	0	0	1	1	1	1	1	1	1	1	0	1	1	0	1	1	1	0	0
3	6	1	1	0	0	1	1	0	1	1	1	0	1	0	1	0	0	1	1	0	0	0
3	7	1	1	0	0	1	0	1	1	1	0	1	1	0	0	1	0	1	0	1	0	0
3	8	1	1	0	0	1	0	0	1	1	0	0	1	0	0	0	0	1	0	0	0	0
3	9	1	1	0	0	0	1	1	1	1	1	1	1	0	1	1	0	1	1	1	0	0
3	10	1	1	0	0	0	1	0	1	1	1	0	1	0	1	0	0	1	1	0	0	0
4	1	1	1	0	0	0	0	1	1	1	0	1	1	0	0	1	0	1	0	1	0	0
4	2	1	1	0	0	0	0	0	1	1	0	0	1	0	0	0	0	1	0	0	0	0
4	3	1	0	1	1	1	1	1	1	1	1	1	1	0	1	1	0	1	1	1	0	0
4	4	1	0	1	1	1	1	0	1	1	1	0	1	0	1	0	0	1	1	0	0	0
4	5	1	0	1	1	1	0	1	1	1	0	1	1	0	0	1	0	1	0	1	0	0
4	6	1	0	1	1	1	0	0	1	1	0	0	1	0	0	0	0	1	0	0	0	0
4	7	1	0	1	1	0	1	1	1	1	1	1	1	0	1	1	0	1	1	1	0	0
4	8	1	0	1	1	0	1	0	1	1	1	0	1	0	1	0	0	1	1	0	0	0
4	9	1	0	1	1	0	0	1	1	1	0	1	1	0	0	1	0	1	0	1	0	0
4	10	1	0	1	1	0	0	0	1	1	0	0	1	0	0	0	0	1	0	0	0	0
5	1	1	0	1	0	1	1	1	1	1	1	1	1	0	1	1	0	1	1	1	0	0
5	2	1	0	1	0	1	1	0	1	1	1	0	1	0	1	0	0	1	1	0	0	0
5	3	1	0	1	0	1	0	1	1	1	0	1	1	0	0	1	0	1	0	1	0	0
5	4	1	0	1	0	1	0	0	1	1	0	0	1	0	0	0	0	1	0	0	0	0
5	5	1	0	1	0	0	1	1	1	1	1	1	1	0	1	1	0	1	1	1	0	0
5	6	1	0	1	0	0	1	0	1	1	1	0	1	0	1	0	0	1	1	0	0	0
5	7	1	0	1	0	0	0	1	1	1	0	1	1	0	0	1	0	1	0	1	0	0
5	8	1	0	1	0	0	0	0	1	1	0	0	1	0	0	0	0	1	0	0	0	0
5	9	1	0	0	1	1	1	1	1	1	1	1	1	0	1	1	0	1	1	1	0	0
5	10	1	0	0	1	1	1	0	1	1	1	0	1	0	1	0	0	1	1	0	0	0
6	1	1	0	0	1	1	0	1	1	1	0	1	1	0	0	1	0	1	0	1	0	0
6	2	1	0	0	1	1	0	0	1	1	0	0	1	0	0	0	0	1	0	0	0	0
6	3	1	0	0	1	0	1	1	1	1	1	1	1	0	1	1	0	1	1	1	0	0
6	4	1	0	0	1	0	1	0	1	1	1	0	1	0	1	0	0	1	1	0	0	0
6	5	1	0	0	1	0	0	1	1	1	0	1	1	0	0	1	0	1	0	1	0	0
6	6	1	0	0	1	0	0	0	1	1	0	0	1	0	0	0	0	1	0	0	0	0
6	7	1	0	0	0	1	1	1	1	1	1	1	1	0	1	1	0	1	1	1	0	0
6	8	1	0	0	0	1	1	0	1	1	1	0	1	0	1	0	0	1	1	0	0	0
6	9	1	0	0	0	1	0	1	1	1	0	1	1	0	0	1	0	1	0	1	0	0
6	10	1	0	0	0	1	0	0	1	1	0	0	1	0	0	0	0	1	0	0	0	0
7	1	1	0	0	0	0	1	1	1	1	1	1	1	0	1	1	0	1	1	1	0	0
7	2	1	0	0	0	0	1	0	1	1	1	0	1	0	1	0	0	1	1	0	0	0
7	3	1	0	0	0	0	0	1	1	1	0	1	1	0	0	1	0	1	0	1	0	0
7	4	1	0	0	0	0	0	0	1	1	0	0	1	0	0	0	0	1	0	0	0	0
7	5	0	1	1	1	1	1	1	1	1	1	1	1	0	1	1	0	1	1	1	0	0
7	6	0	1	1	1	1	1	0	1	1	1	0	1	0	1	0	0	1	1	0	0	0
7	7	0	1	1	1	1	0	1	1	1	1	1	1	0	0	1	0	1	0	1	0	0
7	8	0	1	1	1	1	0	0	1	1	1	0	1	0	0	0	0	1	0	0	0	0
7	9	0	1	1	1	0	1	1	1	1	1	1	1	0	1	1	0	1	1	1	0	0
7	10	0	1	1	1	0	1	0	1	1	1	0	1	0	1	0	0	1	1	0	0	0
8	1	0	1	1	1	0	0	1	1	1	1	1	1	0	0	1	0	1	0	1	0	0
8	2	0	1	1	1	0	0	0	1	1	1	0	1	0	0	0	0	1	0	0	0	0
8	3	0	1	1	0	1	1	1	1	1	1	1	1	0	1	1	0	1	1	1	0	0
8	4	0	1	1	0	1	1	0	1	1	1	0	1	0	1	0	0	1	1	0	0	0
8	5	0	1	1	0	1	0	1	1	1	1	1	1	0	0	1	0	1	0	1	0	0
8	6	0	1	1	0	1	0	0	1	1	1	0	1	0	0	0	0	1	0	0	0	0
8	7	0	1	1	0	0	1	1	1	1	1	1	1	0	1	1	0	1	1	1	0	0
8	8	0	1	1	0	0	1	0	1	1	1	0	1	0	1	0	0	1	1	0	0	0
8	9	0	1	1	0	0	0	1	1	1	0	1	1	0	0	1	0	1	0	1	0	0
8	10	0	1	1	0	0	0	0	1	1	0	0	1	0	0	0	0	1	0	0	0	0
9	1	0	1	0	1	1	1	1	1	1	1	1	1	0	1	1	0	1	1	1	0	0
9	2	0	1	0	1	1	1	0	1	1	1	0	1	0	1	0	0	1	1	0	0	0
9	3	0	1	0	1	1	0	1	1	1	0	1	1	0	0	1	0	1	0	1	0	0
9	4	0	1	0	1	1	0	0	1	1	0	0	1	0	0	0	0	1	0	0	0	0
9	5	0	1	0	1	0	1	1	1	1	1	1	1	0	1	1	0	1	1	1	0	0
9	6	0	1	0	1	0	1	0	1	1	1	0	1	0	1	0	0	1	1	0	0	0
9	7	0	1	0	1	0	0	1	1	1	1	1	1	0	0	1	0	1	0	1	0	0
9	8	0	1	0	1	0	0	0	1	1	1	0	1	0	0	0	0	1	0	0	0	0
9	9	0	1	0	0	1	1	1	1	1	1	1	1	0	1	1	0	1	1	1	0	0
9	10	0	1	0	0	1	1	0	1	1	1	0	1	0	1	0	0	1	1	0	0	0

*NEGATIVE LOGIC NOTATION "1" = –, "0" = +

PROM Power-Down Circuits

National Semiconductor
Jonathan Stinehelfer*

description

Inexpensive bipolar PROMs can be used in high performance, low power applications if powered down when they are not being accessed. Since the access time of the circuit of Figure 1 is less than 80 nanoseconds, the power saving can be greater than 10 to 1 if cycled every microsecond. Longer cycle times, or decoding of the power switching to multiple packages, can yield even more impressive ratios.

Bipolar PROMs with on-chip power-down have power-up to power-down ratios of 3:1. Using the PROM power-down technique illustrated in Figure 1, ratios considerably higher than 3:1 can be obtained. National's PROMs perform well in this application. With power removed, the Tri-State® parts revert quickly to the third (open high Z) state. Because there are no clamp diodes from the outputs to V_{CC}, the powered down device presents only leakage to the output bus.

PROMs do not need to be continuously powered in many applications. Often data is required from a PROM on system power up or for a small percentage of a system cycle. Turning the PROM off when it is not needed saves power and the access time is increased by only the delay of the power down circuit.

The basic power down circuit is illustrated in Figure 2. A TTL level input signal drives the TTL logic input of the power down circuit. The logic input is drawn as a noninverting buffer; however, circuit operation is not limited to noninverting buffers. Logic Table 1 illustrates several logic implementations of both inverting and noninverting inputs with different speed-power tradeoffs.

Circuit operation is as follows. When the logic input to R_2 goes low, base drive is supplied to the PNP switch, turning the switch on. C_1 is a speed-up capacitor which decreases the switching time of the PNP switch. In applications where high speed is not important C_1 is not necessary. When the PNP saturating switch is on V_{CC} (+5 V) is applied to the PROM. The time delay from power up command to power up on the PROM ranges from about 10 ns to 100 ns, depending upon the PNP switch and the TTL logic driving the switch.

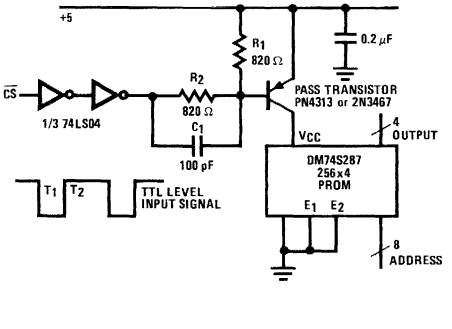


Figure 1. PROM Power Down Circuit

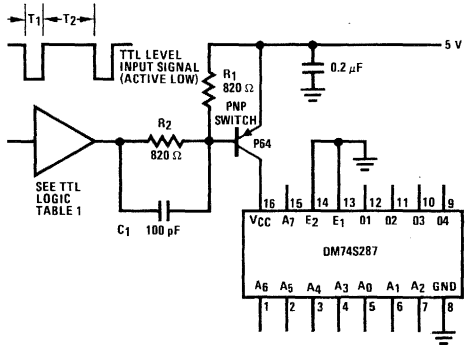


Figure 2. PROM Power Down Circuit

*Refer to Introduction.

logic table

TTL LOGIC	
CS — 74S00 74LS00	• Fast • Active High Selects 74S00 Speed 74LS00 Speed and Low Power
$\overline{CS}$ — 74S04 74LS04	• Fast • Active Low Selects 74S04 Speed Only 74LS04 Speed and Low Power
$\overline{CS}$ — MM74C902	• Very Low Power • Active Low Selects Buffers can be connected in parallel for additional current
1/10 DECODER (4, 10) MM74C42	• Very Low Power • Memory Expansion • No Resistors Required R_1 and R_2, Figure 2, not required

design example

Design a minimum power memory that has a 200 ns access time, a 1000 ns cycle time, and a 256x8 memory.

Two DM74S287 PROMs will be used for the 256x8 memory. DM74S287s have a ±5% power supply tolerance. Since there will be about a 0.2 V drop across the PNP switch we need to ensure that the V_{CC} requirement of the PROM is met.

Since speed is not of prime importance in this application we will select "slow" low power parts in the power down circuit. The 74C902 noninverting buffer will be used as the logic input device. This device is selected for its low power. 2N3467 PNP switch will be used as the pass transistor.

From the data sheets:

2N3467 PNP Saturating Switch

$V_{CE(SAT)}$	I_C = 150 mA	typ = 0.165	max	= 0.3
h_{fe}	I_C = 150 mA	typ = 120	min	= 40
$V_{BE(SAT)}$	I_C = 150 mA	typ = 0.8	max	= 1 V

DM74S287 PROM

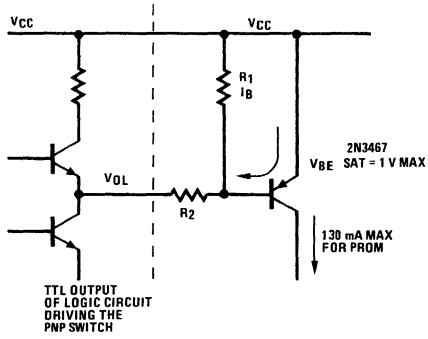
I_{CC} = 80 mA typ, 130 mA max

74C902 Buffer

I_{CC} = 15 μA max

We are now ready to calculate the value of resistor R_2. Resistor R_2 is used to limit the base drive current of the PNP 2N3467 transistor. The value of R_2 is calculated from the voltage across R_2 and the base current required to supply the I_{CC} current required for the PROM.

Resistor calculation:



$$I_B = \frac{130\text{ mA} = I_{CC}}{h_{fe} = 40} = 3.25\text{ mA}$$

min

Base current calculation:

$$R_2 = \frac{V_{CC} - (V_{BE(SAT)} + V_{OL(MAX)})}{I_B + \frac{V_{BE(SAT)}}{R_1 = 820}}$$

$$R_2 = \frac{5 - (1 + 0.5)\text{ V}}{(3.25 + 1.0)\text{ mA}}$$

$$R_2 = \frac{3.5\text{ V}}{4.25\text{ mA}} = 823\ \Omega$$

R_2 = 820 Ω, rounding to the nearest standard value.

R_1 is chosen to be equal to the R_2 to simplify the parts list and this allows resistor packs (8 identical resistors in a 16-pin package) to be used when appropriate.

Figure 3A is the final circuit for the 256 x 8 memory.

Performance of the 256x8 power down memory is:

Power when selected 1345 mW max
Power when deselected 0 mW with 74C902 buffer
Access time 180 ns max

Average power is a function of duty cycle, and for our 256x8 power down example average power is:

$$P_{ave(max)} = \frac{\text{on time}}{\text{off time}}.\quad \text{Power max} = \frac{200\text{ ns}}{1000\text{ ns}}.\ (665)\ (2)$$

$$P_{ave(max)} = \frac{1}{5}(1330) = 265\text{ mW max}$$

The 265 mW assumes that all parts are maximum at the same time. The more likely situation is that parts will be at or near their typical value.

For our example:

$$P_{ave(typ)} = \frac{1}{5}(830) = 166\text{ mW ave}_{typ}$$

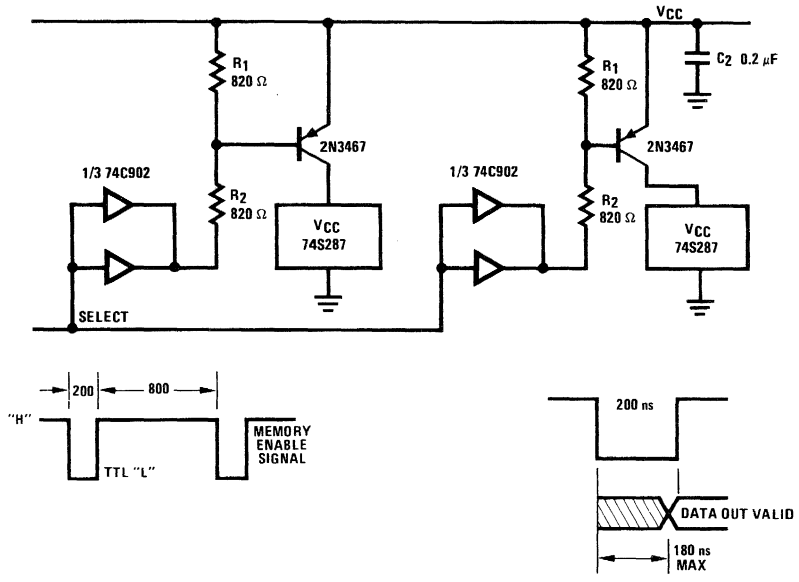


Figure 3A. 256x8 Power Down Memory

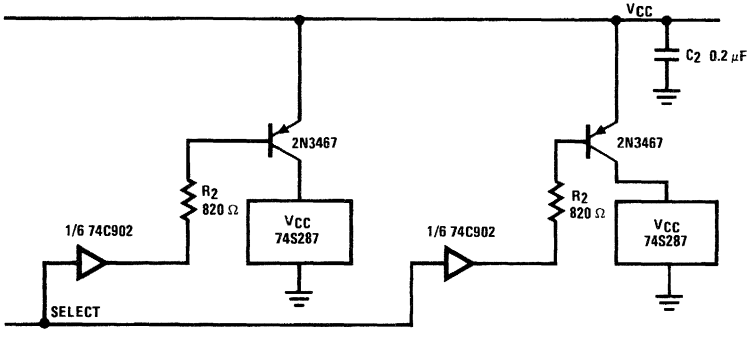


Figure 3B.

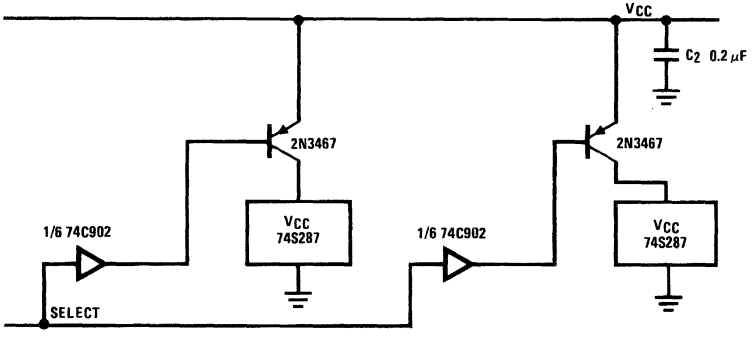


Figure 3C.

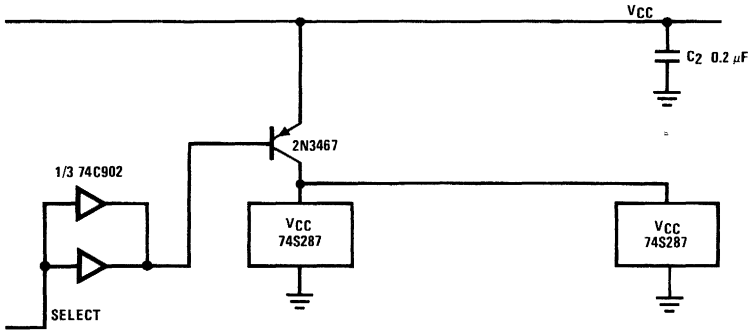
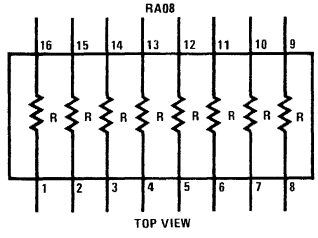


Figure 3D.

performance table

	Typ	Max
Access Time Max		
74C902 Buffer	54 ns	90 ns
2N3467 PNP Switch	20 ns	40 ns
74S287 PROM	35 ns	50 ns
	109 ns	180 ns
Power Selected		
I_B 2N3467		15 mW
74C902		—
74S287 at 5 V, 6.65 mW each		1330 mW
		1345 mW
Power Unselected		
I_B 2N3467		0 (leakage)
74C902		0 (75 μW)
74S287		0
		0 mW

resistor



buffer

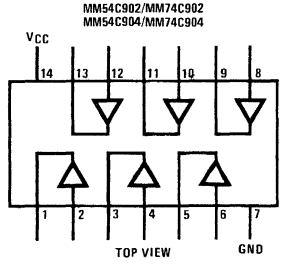


Figure 3B illustrates a circuit simplification of removing R_1 (the I_{b2} resistor). Eliminating R_1 saves a resistor and the power dissipated by the resistor. R_2 still determines the base drive current which is V/R. This circuit will be slightly slower than the circuits in figures 3A or 3C.

Figure 3C illustrates a further reduction in the number of resistors. Neither R_1 nor R_2 is used. Speed will be good and power will be higher than in figures 3A or 3B since the base current for the 2N3467 will be at least 9 mA, and typically will be higher. This adds some power dissipation when the PROMs are powered up.

Figure 3D represents a minimum part count circuit for the 256 x 8 PROM memory.

This application note illustrates several ways to power down National's Schottky TRI-STATE® PROMs. Powering down PROMs is a cost-effective method for obtaining low power and fast access time.

A PROM Programmer for the SC/MP LCDS

National Semiconductor
Application Note AN-189
Fran Terry*
Keith Winter
July 1977

ABSTRACT

This application note describes for the user of the SC/MP Low Cost Development System (LCDS) a method of programming MM5204 or MM4204 Programmable Read Only Memories (PROMs) that is both inexpensive and highly efficient.

INTRODUCTION

In the development cycle, there is a point in software development between read/write memory program debug and commitment to mask programmed ROMs. This is generally filled by using erasable PROMs; this allows the user to test the program in the end application, and then to correct any errors that occur. Also, for the small quantity user, in the end application PROMs may be more practical to use instead of ROMs. This can be inconvenient, however, if a PROM programmer is not readily available.

With the method described in this application note, the LCDS user can construct, using wire-wrap techniques, an inexpensive PROM programmer that plugs into the SC/MP LCDS backplane and programs a 512-by-8 PROM in less than 10 seconds. The only additional item required is a 65 V power supply capable of delivering 500 mA.

CAPABILITIES

The driver software has the ability to copy a PROM into memory for subsequent duplication, to verify a PROM against memory, to program a PROM from any memory area, and to verify that a PROM is erased.

An added feature of the PROM programmer is an LED that is active when the high voltage is being applied to the PROM socket.

NOTE

Damage to the PROM and/or the programmer may result if the PROM is inserted or removed when the LED is turned on.

Listed in Appendix 1 are two versions of the driver software. If the user has a Teletype, the first program can be used. If no Teletype is available, the second program uses the LCDS control panel for all entries.

EXAMPLES OF TELETYPE OPERATION

The Teletype® (TTY) program works in conjunction with the TTY DEBUG package contained on the LCDS Motherboard. The following are some examples of TTY operational routines; the user's read/write memory is assumed to be located from X'1000 to X'17FF.

NOTE

The 65 V power supply should be turned on throughout all of the following operations.

(A dash [-] denotes a debug prompt, a question mark [?] denotes a programmer prompt.)

*Refer to Introduction.

Loading an LM Tape and Programming

-L1000 CR (CR = carriage return)	Load tape into memory starting at address X'1000.
-G0 CR	After tape loads, the user transfers to programmer software.
?P1000 CR	Check PROM for erased condition, then program from X'1000.
?V1000 CR	Verify PROM against memory.
?	Ready for next command.

NOTE

The PROM is now programmed. Pressing the HALT button returns to the DEBUG monitor if desired. The following examples show the initial system state to be in DEBUG.

Duplicating a PROM

-G0 CR	Transfer to programmer routines.
	Put PROM to be duplicated in socket on programmer card.
?C1000 CR	Copy PROM data into memory starting at X'1000.
	Put blank PROM in socket.
?P1000 CR	Program PROM.
?V1000 CR	Verify PROM.
?	Ready for next command.

Program PROM Without Check for Erased Condition

-G0 CR	Transfer to programmer routines.
	Put PROM in socket.
?Y1000 CR	Program PROM from X'1000 without check for erased.
?V1000 CR	Verify PROM.
?	Ready for next command.

Checking PROM for Erased Condition

-G0 CR	Transfer to programmer routines.
	Put PROM in socket.
?E	PROM is checked.
?	Ready for next command.

Listing Contents of a PROM

-G0 CR	Transfer to programmer routines.
	Put PROM in socket.
?C1000 CR	Copy PROM contents into memory.
	Press HALT button to transfer to DEBUG routines.
-T1000:11FF CR	Type contents of buffer area.

Error Messages

If PROM cannot be programmed:

?P1000 CR
BAD PROM @0XXX where 0XXX denotes the address of the PROM that cannot be programmed

If PROM is not erased:

?P1000 CR
NOT ERASED

or

?E
NOT ERASED

If PROM does not verify against memory:

?V1000 CR
NO VERIFY

EXAMPLES OF PANEL OPERATION

For panel operation, the user enters the starting address of the routine to be executed into the Program Counter and the address to be used for copying, verifying against, or programming from into Pointer 1. After placing the PROM in the socket, the RUN button is pressed. The system halts when the operation is completed or if an error is detected. The error halts and their explanations follow:

X'0035	PROM is not erased.
X'0085	PROM cannot be programmed.
X'015A	PROM does not verify.

The following are entry points:

X'0001	Check PROM for erased condition.
X'0035	Program PROM without check for erased.
X'0048	Program PROM with check for erased.
X'0101	Copy PROM into memory.
X'012C	Verify PROM against memory.

When using the panel program, the HALT INST switch on the LCDS Motherboard must be in the DEBUG position before execution. Other than the method of inputting commands and parameters, the TTY program and PANEL program are functionally identical.

Appendix 2 contains generalized flowcharts of the PROM programmer software routines.

These programs are intended to be assembled at X'0000 so they can be placed in PROM on the SC/MP CPU card. For the P-channel card, an MM5204 is used. On the N-channel card, an 87S296 bipolar PROM must be used. If N-channel is used, the delay constants in the programming routines must be doubled to allow the correct timing for the programming pulses.

BOARD CONSTRUCTION

Referring to the schematic diagram, figures 1 and 2, standard wire-wrap techniques are used in the construction of the board. Refer to photo 1 for a suggested placement layout. This placement should be followed as closely as possible, as the transistor drivers and their associated passive components should be near the PROM socket to reduce line inductance. The decoding and control circuits are placed near the board edge connector for access to the data and address buses.

It is suggested that a low or zero insertion force socket be used for the PROM to make insertion and removal easier. This also reduces the possibility of bent pins which can cause errors in programming or damage to the part.

Three waveform photos are included to aid in verification and debug of the circuit. Photo 2 shows the programming pulse from the DM9334 addressable latch and at pin 4 of the PROM. Photo 3 shows the voltage levels of input data for both the logic "0" and logic "1" states. Photo 4 shows the levels of V_{BB} and V_{DD}. All these values are shown during the time of the programming pulse.

PARTS LIST

Type	Description	Quantity
DH3725CN	Quad Core Drivers	6
MM74C173	Quad Latch	2
DM80C95N	Hex Tri-State Buffer	2
CD4040N	12-Stage Binary Counter	1
DM8223N	1-of-8 Decoder	1
DM8131N	6-Bit Bus Comparator	1
DM8090N	Miscellaneous Gates	1
DM9334N	Addressable Latch	1
NSL5026	LED	1
2N4250	PNP Transistor	2
2N2905	PNP Transistor	1
1N93	Germanium Diode	4
LM317T	Voltage Regulator	2
RESISTORS	May be Resistor Arrays	62

A suggested board for construction is National Semiconductor part no. IPC-16C/801 prototyping board. However, any prototype board that has a 72-pin edge connector on 0.100 inch centers (plug compatible with the SC/MP LCDS bus) and room for at least 32 16-pin IC sockets can be substituted.

Each TTL and CMOS circuit should be bypassed by a 0.1 μF capacitor across V_{CC} and GND as well as bulk capacitors across V_{CC} and GND and −12 V and GND at the input to the board. These capacitors should be tantalum and should be in the 20 μF to 30 μF range.

CONCLUSIONS

This PROM programmer greatly extends the use of the SC/MP LCDS as a prototyping/development system by giving the user the ability to program PROMs for debug and test purposes while remaining much less expensive than commercially available PROM programmers. Also, since it is to be used in the LCDS, no special formats for the data are required. Load modules created by the SC/MP LCDS can be loaded by the firmware provided without conversion to binary, complemented binary, or BPNF formats.

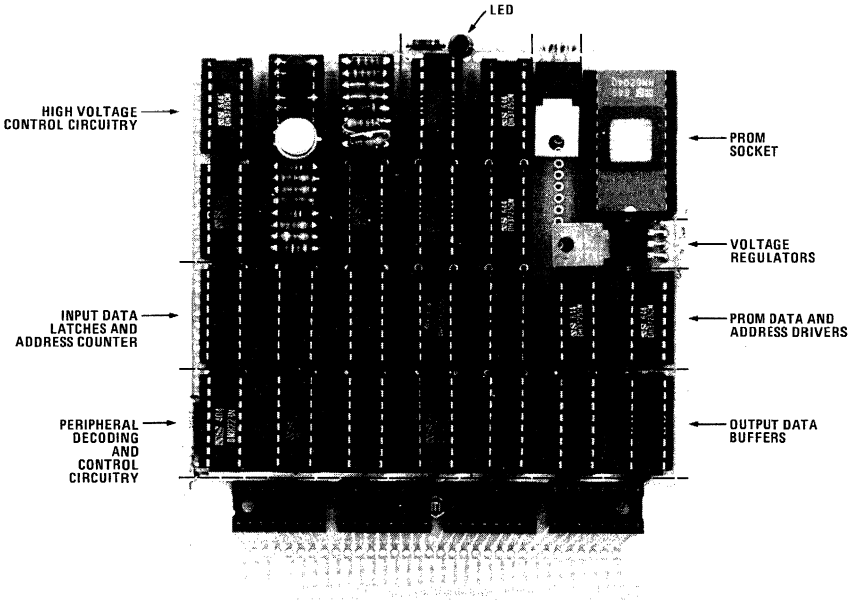


Photo 1.

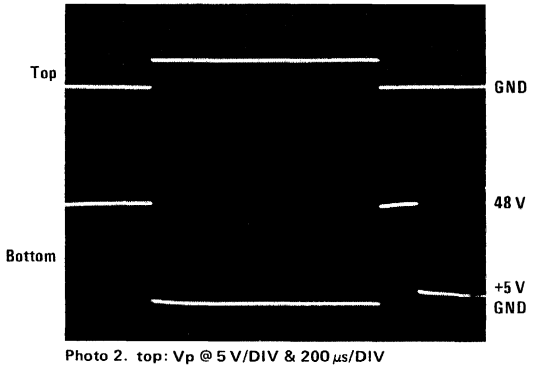


Photo 2. top: Vp @ 5 V/DIV & 200 μs/DIV
bottom: Vp (PROM) @ 20 V/DIV & 200 μs/DIV

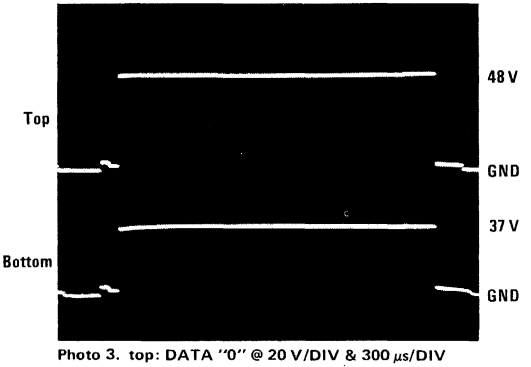


Photo 3. top: DATA "0" @ 20 V/DIV & 300 μs/DIV
bottom: DATA "1" @ 20 V/DIV & 300 μs/DIV

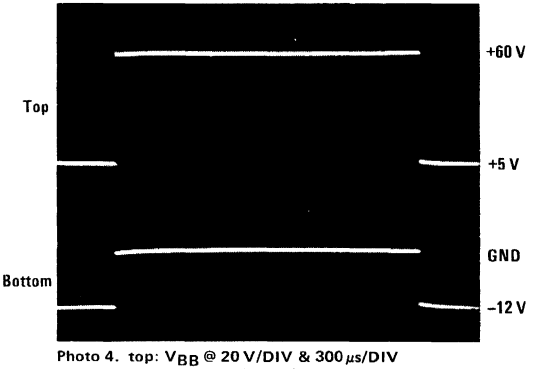


Photo 4. top: V_{BB} @ 20 V/DIV & 300 μs/DIV
bottom: V_{DD} @ 10 V/DIV & 300 μs/DIV

ABSOLUTE DEVICE ADDRESS:
X'8000 - X'83FF

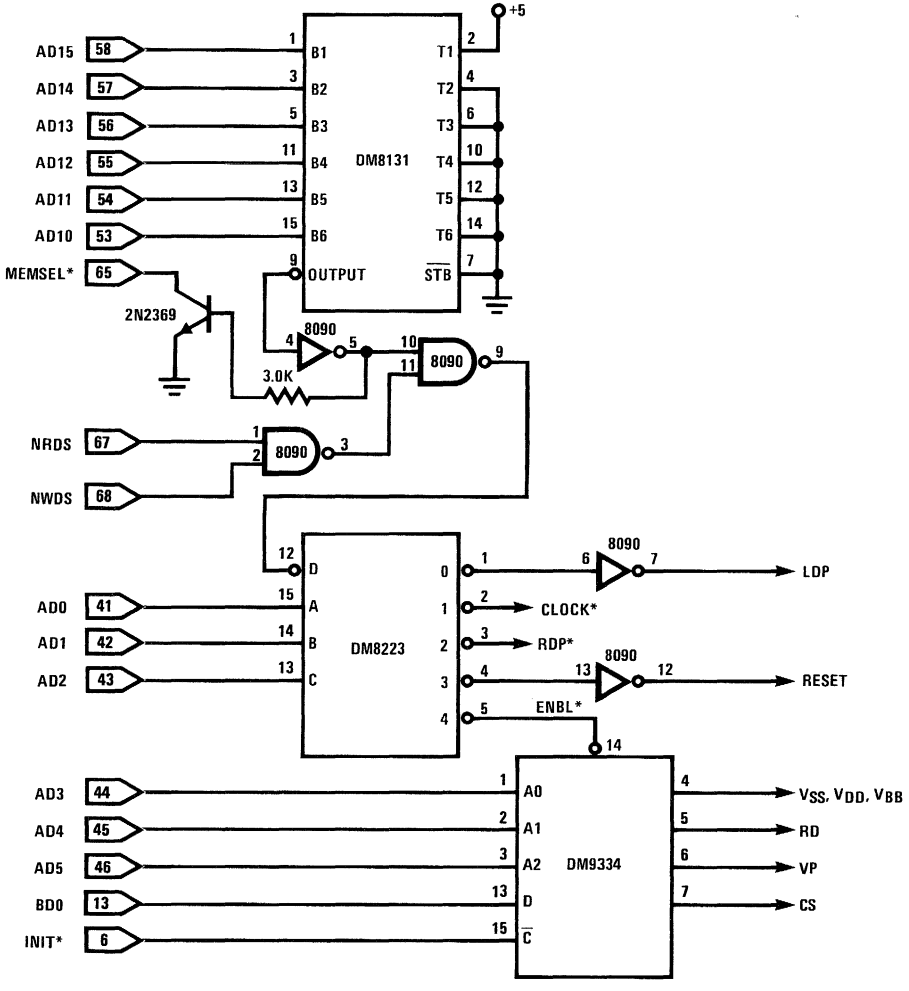


Figure 1.

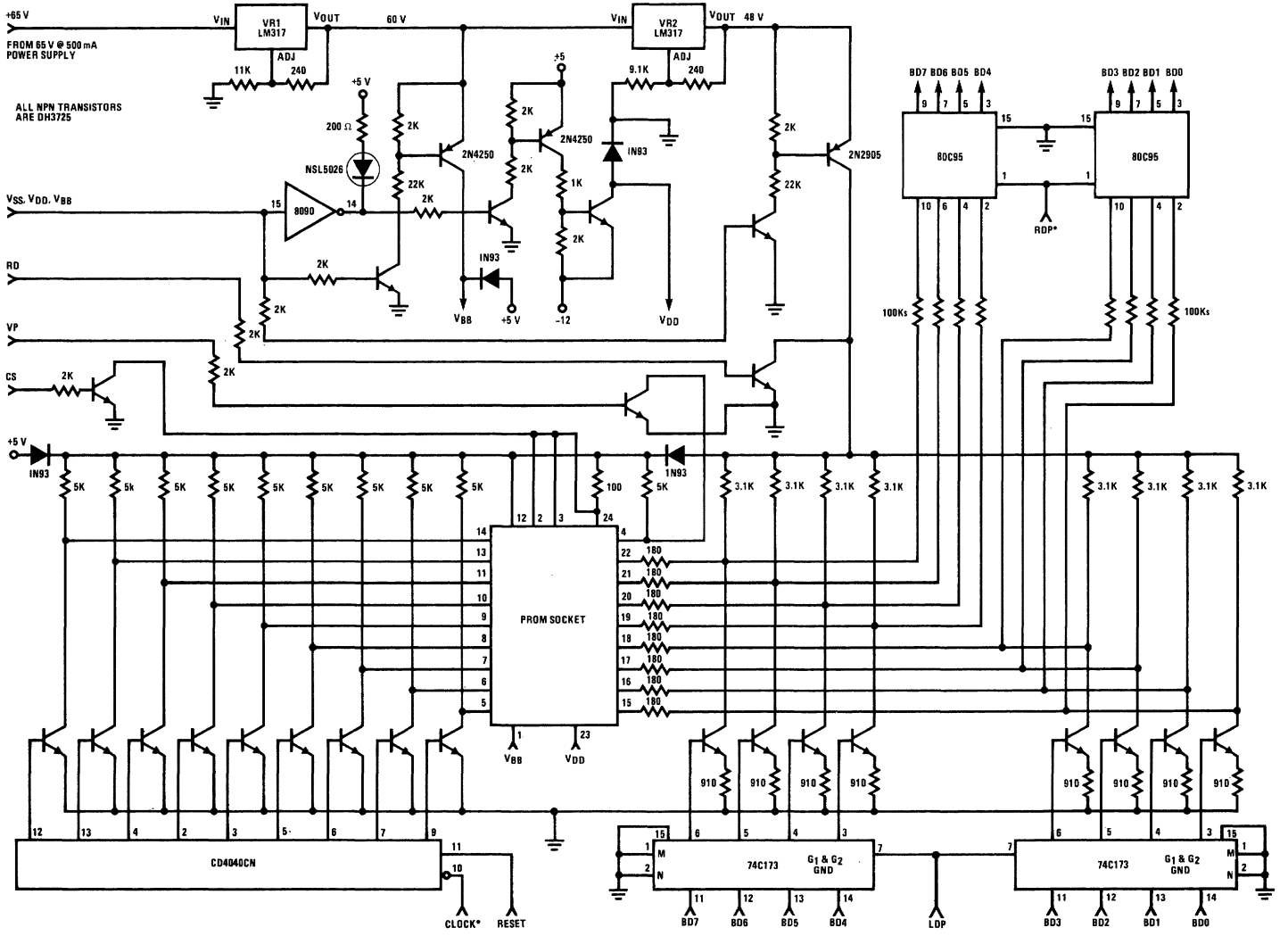

+65 V
FROM 65 V @ 500 mA POWER SUPPLY
VIN
VR1 LM317
VOUT
60 V
ADJ
11K
240
VIN
VR2 LM317
VOUT
48 V
ADJ
9.1K
240
ALL NPN TRANSISTORS ARE DH3725
+5 V
200 Ω
NSL5026
2K
22K
2N4250
1K
IN93
2N2905
VSS, VDD, VBB
8090
RD
VP
CS
VBB
-12
VDD
BD7 BD6 BD5 BD4
BD3 BD2 BD1 BD0
80C95
ROP*
100Ks
5K
100
PROM SOCKET
180
3.1K
910
CD4040CN
CLOCK*
RESET
74C173
G1 & G2
GND
LDP

Figure 2.

Appendix 1

```
SC/MP ASSEMBLER REV-A
TTYPGM SC/MP PROM PROGRAMMER


    1                       .TITLE  TTYPGM, ' SC/MP PROM PROGRAMMER'
    2
    3               ; "TTYPGM" IS A PROGRAM THAT ALLOWS THE SC/MP LCDS TO
    4               ; PROGRAM MM5204 OR MM4204 PROMS.
    5
    6               ; THE COMMANDS AND THEIR FORMATS ARE:
    7
    8               ;       CXXXX                       COPY PROM INTO MEMORY
    9
   10               ;       VXXXX                       VERIFY PROM AGAINST MEMORY
   11
   12               ;       E                           VERIFY PROM IS ERASED
   13
   14               ;       PXXXX                       PROGRAM PROM FROM MEMORY
   15               ;                                   WITH CHECK FOR ERASED
   16
   17               ;       YXXXX                       PROGRAM PROM FROM MEMORY
   18               ;                                   WITHOUT CHECK FOR ERASED
   19
   20               ; WHERE XXXX IS THE HEX STARTING ADDRESS TO BE USED.
   21
   22               ; THE PROGRAM REQUIRES THAT THERE ARE 512 CONTINUOUS MEMORY
   23               ; LOCATIONS UPWARDS FROM XXXX.
   24
   25               ; "TTYPGM" USES MEMORY ON THE LCDS MOTHERBOARD FOR TEMPORARY
   26               ; STORAGE.   THEREFORE, USER R/W MEMORY CAN BE ANYWHERE,
   27               ; EXCEPT AS SHOWN BELOW.
   28
   29               ; "TTYPGM" CAN BE ASSEMBLED ANYWHERE THE USER HAS MEMORY
   30               ; SPACE EXCEPT IN THE FOLLOWING LOCATIONS:
   31
   32               ;       X'8000 -- X'83FF        LOCATIONS OCCUPIED BY
   33               ;                               PROGRAMMER HARDWARE
   34               ;       X'7000 -- X'7FFF        LOCATIONS USED BY LCDS
   35
   36               ; A TELETYPE IS REQUIRED FOR EXECUTION.
   37
```

```
SC/MP ASSEMBLER REV-A
TTYPGM SC/MP PROM PROGRAMMER
POINTERS AND CONSTANTS


   38                       .PAGE   'POINTERS AND CONSTANTS'
   39
   40 0000                  .=0
   41
   42       0001    P1      =       1
   43       0002    P2      =       2
   44       0003    P3      =       3
   45
   46       8000    PPRGMR  =       08000           ;PERIPHERAL ADDR.  OF PROM
   47                                               ;  PROGRAMMER BOARD
   48       0014    VP      =       014             ;ORDER CODE FOR PROG.  VOLTAGE
   49       000C    RD      =       0C              ;ORDER CODE FOR READ
   50       0004    VSS     =       04              ;ORDER CODE FOR VSS, VBB, VDD
   51       001C    CS      =       01C             ;ORDER CODE FOR CHIP SELECT
   52       0000    LOAD    =       0               ;ORDER CODE TO LOAD DATA
   53       0001    CLK     =       1               ;ORDER CODE TO CLOCK COUNTER
   54       0002    RDPRM   =       2               ;ORDER CODE TO READ PROM
   55                                               ;  DATA
   56       0003    CLR     =       3               ;ORDER CODE TO CLEAR COUNTER
   57       0004    ENBL    =       4               ;ORDER CODE TO ENABLE CONTROL
   58                                               ;  LATCH
   59       7AE2    PUTC    =       07AE2           ;PUT CHARACTER POINTER
   60       7A91    GECHO   =       07A91           ;GET CHARACTER W/ECHO POINTER
   61       7B50    GHEX    =       07B50           ;POINTER TO GET 4 HEX DIGITS
   62       7B17    MESG    =       07B17           ;POINTER TO MESSAGE ROUTINE
   63       7BB3    PHEX    =       07BB3           ;POINTER TO PUT HEX ROUTINE
   64       77D0    STACK   =       077D0           ;STACK POINTER TO MOTHERBOARD
   65                                               ;  R/W MEMORY
   66       FFEF    HI      =       -17             ;TEMPORARY LOCATIONS OFFSET
   67       FFEE    LO      =       -18             ;  FROM STACK POINTER
   68       FFED    SAVLO   =       -19
   69       FFEC    SAVHI   =       -20
   70       FFEB    HCNT    =       -21
   71       FFEA    DPLO    =       -22
   72       FFE9    DPHI    =       -23
   73
```

5

```
SC/MP ASSEMBLER REV-A
TTYPGM SC/MP PROM PROGRAMMER
COMMAND INPUT PROCESSING


  74                        .PAGE   'COMMAND INPUT PROCESSING'
  75
  76                ; *** COMMAND ENTRY ROUTINE ***
  77
  78 0000 08                NOP
  79                ENTRY:
  80 0001 C477              LDI     H(STACK)          ;INITIALIZE STACK PTR.
  81 0003 36                XPAH    P2
  82 0004 C4D0              LDI     L(STACK)
  83 0006 32                XPAL    P2
  84                PROMPT:
  85 0007 C47B              JS      P3,MESG           ;PROMPT FOR COMMAND
     0009 37C4
     000B 1633
     000D 3F
  86 000E 01EC              .DBYTE  PRMPT
  87 0010 C47A              JS      P3,GECHO          ;GO TO GET CHAR. W/ECHO
     0012 37C4
     0014 9033
     0016 3F
  88 0017 D47F              ANI     07F               ;MASK OUT PARITY, IF ANY
  89 0019 01                XAE                       ;SAVE CHAR. IN E. REG.
  90 001A C401              LDI     H(CMDTBL)         ;SET PTR. TO COMMAND TABLE
  91 001C 35                XPAH    P1
  92 001D C4F0              LDI     L(CMDTBL)
  93 001F 31                XPAL    P1
  94 0020 02                CCL
  95                CLOOP:
  96 0021 C503              LD      @3(P1)            ;GET COMMAND CHAR.
  97 0023 980E              JZ      ERROR             ;END OF TABLE, ERROR ON INPUT
  98 0025 60                XRE                       ;CHECK FOR CORRECT COMMAND
  99 0026 9CF9              JNZ     CLOOP             ;NOT RIGHT, TRY NEXT
 100 0028 C5FF              LD      @-1(P1)           ;FOUND COMMAND, GET ADDR.
 101 002A 01                XAE                       ;SAVE TEMPORARILY IN E. REG.
 102 002B C5FF              LD      @-1(P1)
 103 002D 35                XPAH    P1
 104 002E 40                LDE
 105 002F 31                XPAL    P1
 106 0030 3D                XPPC    P1                ;EXECUTE COMMAND
 107 0031 90D4              JMP     PROMPT
 108                ERROR:
 109 0033 C4E1              LDI     L(PUTC)-1
 110 0035 33                XPAL    P3
 111 0036 C43F              LDI     '?'
 112 0038 3F                XPPC    P3
 113 0039 90CC              JMP     PROMPT
 114
```

```
                        .PAGE   'PROM ACCESS AND PROGRAMMING ROUTINES'

                ; *** ROUTINE TO CHECK PROM FOR ERASED CONDITION ***

                ; THIS SUBROUTINE IS ALSO CALLED BY "PROG:" TO VERIFY THAT
                ; THE PROM IS ERASED.

                ERASED:
003B C480               LDI     H(PPRGMR)       ;SET ADDR. OF PROGRAMMER
003D 37                 XPAH    P3
003E C400               LDI     L(PPRGMR)
0040 33                 XPAL    P3
0041 C401               LDI     1               ;SET UPPER COUNT
0043 CAEF               ST      HI(P2)          ;STACK IS EMPTY, USE AS PTR.
0045 CB0C               ST      RD(P3)          ;SET READ MODE
0047 CB1C               ST      CS(P3)          ;SELECT PROM SOCKET
0049 C400               LDI     0               ;SET LOWER COUNT
004B CAEE               ST      LO(P2)
004D CB03               ST      CLR(P3)         ;CLEAR PROM COUNTER
004F CB00               ST      LOAD(P3)        ;CLEAR DATA LATCHES FOR READ
                ELOOP:
0051 C302               LD      RDPRM(P3)       ;READ DATA OUT OF PROM
0053 9C0B               JNZ     NOT             ;DATA NOT ZERO? NOT ERASED
0055 CB01               ST      CLK(P3)         ;DATA OK, BUMP COUNTER
0057 BAEE               DLD     LO(P2)          ;DECREMENT LOWER COUNT
0059 9CF6               JNZ     ELOOP           ;NOT DONE YET
005B BAEF               DLD     HI(P2)          ;DECREMENT UPPER COUNT
005D 94F2               JP      ELOOP           ;NOT DONE YET
005F 3D                 XPPC    P1              ;PROM IS ERASED
                NOT:
0060 C47B               JS      P3,MESG         ;GO TO MESSAGE RTN
0062 37C4
0064 1633
0066 3F
0067 01C4               .DBYTE  NOTMSG          ;PTR TO MESSAGE
                RETN2:
0069 909C               JMP     PROMPT          ;RETURN TO COMMAND PROCESSING

                ; *** ENTRY POINT TO PROGRAM PROM W/O CHECK FOR ERASED ***

                WOCHK:
006B C47B               JS      P3,GHEX         ;GET ADDR. TO PROG. FROM
006D 37C4
006F 4F33
0071 3F
0072 C480               LDI     H(PPRGMR)
0074 37                 XPAH    P3
0075 C400               LDI     L(PPRGMR)
0077 33                 XPAL    P3
0078 C601               LD      @1(P2)          ;GET UPPER BYTE OF ADDR.
007A F402               ADI     2               ;ADD 512 OFFSET
007C 35                 XPAH    P1
007D C601               LD      @1(P2)          ;GET LOWER BYTE
007F 31                 XPAL    P1
```

```
SC/MP ASSEMBLER REV-A
TTYPGM SC/MP PROM PROGRAMMER
PROM ACCESS AND PROGRAMMING ROUTINES


  163 0080 901D            JMP     SET
  164
  165                ; *** ENTRY POINT TO PROGRAM PROM W/CHECK FOR ERASED ***
  166
  167                ;     PROM IS PROGRAMMED FROM MOST SIGNIFICANT ADDRESS TO
  168                ;     LEAST SIGNIFICANT ADDRESS DUE TO INVERSION OF COUNTER.
  169
  170                PROG:
  171 0082 C47B            JS      P3,GHEX         ;GET ADDR.  TO PROGRAM FROM
      0084 37C4
      0086 4F33
      0088 3F
  172 0089 C601            LD      @1(P2)          ;RETRIEVE ADDR.  FROM STACK
  173 008B 01              XAE
  174 008C C601            LD      @1(P2)
  175 008E CAED            ST      SAVLO(P2)       ;SAVE  IN R/W MEMORY
  176 0090 40              LDE
  177 0091 CAEC            ST      SAVHI(P2)
  178 0093 C43A            LDI     L(ERASED)-1     ;CHECK PROM FOR ERASED
  179 0095 31              XPAL    P1
  180 0096 3D              XPPC    P1
  181 0097 C2ED            LD      SAVLO(P2)
  182 0099 31              XPAL    P1
  183 009A C2EC            LD      SAVHI(P2)
  184 009C F402            ADI     2               ;ADD 512 OFFSET
  185 009E 35              XPAH    P1
  186 009F C401    SET:    LDI     1
  187 00A1 CAEF            ST      HI(P2)          ;SET UPPER LOC COUNT
  188 00A3 C400            LDI     0
  189 00A5 CAEE            ST      LO(P2)          ;SET LOWER LOC COUNT
  190 00A7 CB03            ST      CLR(P3)         ;CLEAR PROM COUNTER
  191                NXTLOC:
  192 00A9 C5FF            LD      @-1(P1)         ;GET DATA TO PROGRAM
  193 00AB 01              XAE                     ;SAVE IN EXTENSION REG.
  194                THSLOC:
  195 00AC C401            LDI     H(PPROM)        ;SET ADDR.  OF PROGRAMMING RTN
  196 00AE 35              XPAH    P1
  197 00AF CAEC            ST      SAVHI(P2)       ;SAVE PTR ADDR.
  198 00B1 C421            LDI     L(PPROM)-1
  199 00B3 31              XPAL    P1
  200 00B4 CAED            ST      SAVLO(P2)
  201 00B6 C4FE            LDI     -2              ;SET COUNT
  202 00B8 CAEB            ST      HCNT(P2)        ;SAVE HIT COUNT IN RAM
  203                GO:
  204 00BA 3D              XPPC    P1
  205 00BB 60              XRE                     ;CHECK PROM DATA
  206 00BC 981B            JZ      OK              ;PROM DATA CORRECT,  DO X+5X
  207 00BE BAEB            DLD     HCNT(P2)        ;DECREMENT HIT COUNT
  208 00C0 9CF8            JNZ     GO              ;CHECK FOR MAX.  HIT
  209                NPROG:
  210 00C2 C47B            JS      P3,MESG         ;HIT COUNT OVER MAX,  BAD PROM
      00C4 37C4
      00C6 1633
      00C8 3F
```

```
  211 00C9 01DD            .DBYTE  BADPRM
  212              LOC:
  213 00CB C4B2            LDI     L(PHEX)-1
  214 00CD 33              XPAL    P3
  215 00CE C2EF            LD      HI(P2)
  216 00D0 3F              XPPC    P3
  217 00D1 C2EE            LD      LO(P2)
  218 00D3 02              CCL                         ;CLEAR CARRY/LINK FLAG
  219 00D4 F4FF            ADI     -1                  ;CORRECT COUNT
  220 00D6 3F              XPPC    P3
  221 00D7 9090            JMP     RETN2
  222              OK:
  223 00D9 02              CCL
  224 00DA C400            LDI     0
  225 00DC CAE9            ST      DPHI(P2)            ;CLEAR UPPER D.P.  COUNT
  226 00DE FAEB            CAD     HCNT(P2)            ;COMPLEMENT HIT COUNT
  227 00E0 CAEB            ST      HCNT(P2)
  228 00E2 02              CCL                         ;CLEAR CARRY/LINK FLAG
  229 00E3 F2EB            ADD     HCNT(P2)            ;COMPUTE 5X
  230 00E5 CAEA            ST      DPLO(P2)
  231 00E7 C400            LDI     0
  232 00E9 F2E9            ADD     DPHI(P2)
  233 00EB CAE9            ST      DPHI(P2)            ;2X
  234 00ED 02              CCL
  235 00EE C2EA            LD      DPLO(P2)
  236 00F0 F2EA            ADD     DPLO(P2)
  237 00F2 CAEA            ST      DPLO(P2)
  238 00F4 C2E9            LD      DPHI(P2)
  239 00F6 F2E9            ADD     DPHI(P2)
  240 00F8 CAE9            ST      DPHI(P2)            ;4X
  241 00FA 02              CCL
  242 00FB C2EB            LD      HCNT(P2)
  243 00FD F2EA            ADD     DPLO(P2)
  244 00FF CAEA            ST      DPLO(P2)
  245 0101 C400            LDI     0
  246 0103 F2E9            ADD     DPHI(P2)
  247 0105 CAE9            ST      DPHI(P2)            ;5X
  248              PRLP:
  249 0107 3D              XPPC    P1                  ;PROGRAM PROM
  250 0108 BAEA            DLD     DPLO(P2)            ;DECREMENT LOWER COUNT
  251 010A 9CFB            JNZ     PRLP                ;NOT DONE
  252 010C BAE9            DLD     DPHI(P2)            ;DECREMENT UPPER COUNT
  253 010E 94F7            JP      PRLP                ;NOT DONE
  254 0110 C2ED            LD      SAVLO(P2)           ;RESTORE P1
  255 0112 31              XPAL    P1
  256 0113 C2EC            LD      SAVHI(P2)
  257 0115 35              XPAH    P1
  258              UPDATE:
  259 0116 CB01            ST      CLK(P3)             ;BUMP PROM COUNTER
  260 0118 BAEE            DLD     LO(P2)              ;DECREMENT LOWER LOC COUNT
  261 011A 9C8D            JNZ     NXTLOC              ;NOT DONE
  262 011C BAEF            DLD     HI(P2)              ;DECREMENT UPPER LOC COUNT
  263 011E 9489            JP      NXTLOC              ;NOT DONE
  264 0120 9051            JMP     RETN1               ;PROGRAMMING DONE
```

```
SC/MP ASSEMBLER REV-A
TTYPGM SC/MP PROM PROGRAMMER
PROM ACCESS AND PROGRAMMING ROUTINES


  265                   PPROM:
  266 0122 C400                 LDI     0
  267 0124 CB0C                 ST      RD(P3)          ;TURN OFF READ MODE AND
  268 0126 CB1C                 ST      CS(P3)          ;  CHIP SELECT
  269 0128 40                   LDE
  270 0129 CB00                 ST      LOAD(P3)        ;SEND DATA TO PROGRAMMER
  271 012B C401                 LDI     1
  272 012D CB04                 ST      VSS(P3)         ;TURN ON VSS VOLTAGE
  273 012F C47F                 LDI     07F             ;WAIT 500 MICROSECONDS
  274 0131 8F00                 DLY     0
  275 0133 CB14                 ST      VP(P3)          ;TURN ON PROGRAM PULSE
  276 0135 C4FF                 LDI     0FF
  277 0137 8F00                 DLY     0               ;DELAY 1 MS
  278 0139 C400                 LDI     0
  279 013B CB14                 ST      VP(P3)          ;TURN OFF VP
  280 013D C414                 LDI     20              ;WAIT 100 MICROSECONDS
  281 013F 8F00                 DLY     0
  282 0141 C400                 LDI     0
  283 0143 CB04                 ST      VSS(P3)         ;TURN OFF VSS VOLTAGE
  284 0145 C414                 LDI     20              ;WAIT 100 MICROSECONDS
  285 0147 8F00                 DLY     0
  286 0149 CB0C                 ST      RD(P3)          ;SET UP READ MODE
  287 014B CB1C                 ST      CS(P3)          ;SELECT PROM SOCKET
  288 014D C400                 LDI     0
  289 014F CB00                 ST      LOAD(P3)        ;CLEAR DATA LATCHES
  290 0151 C302                 LD      RDPRM(P3)       ;READ DATA FROM PROM
  291 0153 3D                   XPPC    P1
  292 0154 90CC                 JMP     PPROM
  293
  294                   ; *** COPY PROM TO RANGE IN MEMORY ***
  295
  296                   COPY:
  297 0156 C401                 JS      P1,SETRD        ;SET READ MODE
      0158 35C4
      015A A531
      015C 3D
  298 015D C601                 LD      @1(P2)          ;RETRIEVE ADDR.  FROM STACK
  299 015F F402                 ADI     2               ;ADD 512 OFFSET
  300 0161 35                   XPAH    P1
  301 0162 C601                 LD      @1(P2)
  302 0164 31                   XPAL    P1
  303                   CPLOOP:
  304 0165 C302                 LD      RDPRM(P3)       ;GET PROM DATA
  305 0167 CDFF                 ST      @-1(P1)         ;STORE INTO MEMORY
  306 0169 CB01                 ST      CLK(P3)         ;BUMP PROM COUNTER
  307 016B BAEE                 DLD     LO(P2)          ;DECREMENT LOC COUNTER LOW
  308 016D 9CF6                 JNZ     CPLOOP
  309 016F BAEF                 DLD     HI(P2)          ;DECREMENT LOC COUNTER HIGH
  310 0171 94F2                 JP      CPLOOP          ;NOT DONE
  311                   RETN1:
  312 0173 C400                 LDI     H(PROMPT)
  313 0175 35                   XPAH    P1
  314 0176 C406                 LDI     L(PROMPT)-1
  315 0178 31                   XPAL    P1
```

```
SC/MP ASSEMBLER REV-A
TTYPGM SC/MP PROM PROGRAMMER
PROM ACCESS AND PROGRAMMING ROUTINES


  316 0179 3D              XPPC    P1
  317
  318                ; *** VERIFY PROM AGAINST RANGE IN MEMORY ***
  319
  320                VERIFY:
  321 017A C401            JS      P1,SETRD        ;SET READ MODE
      017C 35C4
      017E A531
      0180 3D
  322 0181 C601            LD      @1(P2)
  323 0183 F402            ADI     2               ;ADD 512 OFFSET
  324 0185 35              XPAH    P1
  325 0186 C601            LD      @1(P2)
  326 0188 31              XPAL    P1
  327                VLOOP:
  328 0189 C302            LD      RDPRM(P3)       ;GET DATA FROM PROM
  329 018B E5FF            XOR     @-1(P1)         ;COMPARE AGAINST MEMORY DATA
  330 018D 9C0C            JNZ     NOVFY           ;DOES NOT VERIFY
  331 018F CB01            ST      CLK(P3)         ;BUMP PROM COUNTER
  332 0191 BAEE            DLD     LO(P2)          ;DECREMENT LOC COUNTER LOW
  333 0193 9CF4            JNZ     VLOOP           ;NOT DONE
  334 0195 BAEF            DLD     HI(P2)          ;DECREMENT LOC COUNTER HIGH
  335 0197 94F0            JP      VLOOP           ;NOT DONE
  336 0199 90D8            JMP     RETN1
  337                NOVFY:
  338 019B C47B            JS      P3,MESG         ;GO TO MESSAGE ROUTINE
      019D 37C4
      019F 1633
      01A1 3F
  339 01A2 01D1            .DBYTE  NVRFY
  340 01A4 90CD            JMP     RETN1
  341                SETRD:
  342 01A6 C47B            JS      P3,GHEX         ;GET ADDR.  TO COPY TO
      01A8 37C4
      01AA 4F33
      01AC 3F
  343 01AD C480            LDI     H(PPRGMR)       ;PUT ADDR.  OF PROGRAMMER
  344 01AF 37              XPAH    P3              ;  IN P3
  345 01B0 C400            LDI     L(PPRGMR)
  346 01B2 33              XPAL    P3
  347 01B3 C401            LDI     1               ;SET UPPER LOC COUNTER
  348 01B5 CAF1            ST      HI+2(P2)
  349 01B7 CB0C            ST      RD(P3)          ;SET READ MODE
  350 01B9 CB1C            ST      CS(P3)          ;SELECT PROM SOCKET
  351 01BB C400            LDI     0
  352 01BD CAF0            ST      LO+2(P2)
  353 01BF CB03            ST      CLR(P3)         ;CLEAR PROM COUNTER
  354 01C1 CB00            ST      LOAD(P3)        ;CLEAR PROM DATA LATCHES
  355 01C3 3D              XPPC    P1
  356
```

5

```
  357                           .PAGE   'MESSAGES AND COMMAND TABLE'
  358
  359                   ; *** MESSAGES ***
  360
  361                   NOTMSG:
  362 01C4 0D0A                 .DBYTE  0D0A
  363 01C6 4E4F                 .ASCII  'NOT ERASED'
      01C8 5420
      01CA 4552
      01CC 4153
      01CE 4544
  364 01D0 00                   .BYTE   0
  365                   NVRFY:
  366 01D1 0D0A                 .DBYTE  0D0A
  367 01D3 4E4F                 .ASCII  'NO VERIFY'
      01D5 2056
      01D7 4552
      01D9 4946
      01DB 59
  368 01DC 00                   .BYTE   0
  369                   BADPRM:
  370 01DD 0D0A                 .DBYTE  0D0A
  371 01DF 4241                 .ASCII  'BAD PROM AT '
      01E1 4420
      01E3 5052
      01E5 4F4D
      01E7 2041
      01E9 5420
  372 01EB 00                   .BYTE   0
  373                   PRMPT:
  374 01EC 0D0A                 .DBYTE  0D0A
  375 01EE 3F                   .BYTE   '?',0
      01EF 00
  376
  377                   ; *** COMMAND TABLE ***
  378
  379                   CMDTBL:
  380 01F0 50                   .BYTE   'P'
  381 01F1 0081                 .DBYTE  PROG-1
  382 01F3 59                   :BYTE   'Y'
  383 01F4 006A                 .DBYTE  WOCHK-1
  384 01F6 45                   .BYTE   'E'
  385 01F7 003A                 .DBYTE  ERASED-1
  386 01F9 56                   .BYTE   'V'
  387 01FA 0179                 .DBYTE  VERIFY-1
  388 01FC 43                   .BYTE   'C'
  389 01FD 0155                 .DBYTE  COPY-1
  390 01FF 00                   .BYTE   0
  391
  392       0000                .END
```

```
SC/MP ASSEMBLER REV-A
PNLPGM SC/MP PROM PROGRAMMER


    1                       TITLE  PNLPGM, ' SC/MP PROM PROGRAMMER'
    2
    3               ; "PNLPGM" IS A PROGRAM THAT ALLOWS THE SC/MP LCDS TO
    4               ; PROGRAM MM5204 OR MM4204 PROMS USING THE PANEL FOR ALL
    5               ; INPUTS FROM THE USER.
    6
    7               ; THE USER MUST ENTER THE STARTING HEX ADDRESS TO BE
    8               ; PROGRAMMED FROM OR COPIED TO INTO POINTER #1 BEFORE
    9               ; EXECUTING EACH ROUTINE.
   10
   11               ; THE PROGRAM REQUIRES THAT THERE ARE 512 CONTINUOUS MEMORY
   12               ; LOCATIONS UPWARDS FROM THE CONTENTS OF POINTER #1.
   13
   14               ; "PNLPGM" USES MEMORY ON THE LCDS MOTHERBOARD FOR TEMPORARY
   15               ; STORAGE.  THEREFORE, USER R/W MEMORY CAN BE ANYWHERE,
   16               ; EXCEPT AS SHOWN BELOW.
   17
   18               ; "PNLPGM" CAN BE ASSEMBLED ANYWHERE THE USER HAS MEMORY
   19               ; SPACE EXCEPT IN THE FOLLOWING LOCATIONS:
   20
   21               ;       X'8000 -- X'83FF      LOCATIONS OCCUPIED BY
   22               ;                             PROGRAMMER HARDWARE
   23               ;       X'7000 -- X'7FFF      LOCATIONS USED BY LCDS
   24
   25               ; THE ENTRY POINTS ARE:
   26
   27               ;  NAME          ADDRESS
   28               ;  ----          -------
   29
   30               ; CKERSD         X'0001          CHECK PROM FOR ERASED
   31               ; WOCHK          X'0035          PRORGAM PROM WITHOUT CHECK
   32               ;                                FOR ERASED
   33               ; PROG           X'0048          PROGRAM PROM WITH CHECK FOR
   34               ;                                ERASED
   35               ; COPY           X'0101          COPY PROM INTO MEMORY
   36               ; VERIFY         X'012C          VERIFY PROM AGAINST MEMORY
   37
   38               ; "PNLPGM" HALTS WHEN FINISHED OR ON ERRORS.  THE ERROR
   39               ; HALTS ARE:
   40
   41               ;  X'0035        PROM NOT ERASED
   42               ;  X'0085        PROM CANNOT BE PROGRAMMED
   43               ;  X'015A        PROM DOES NOT VERIFY
   44
   45               ; THE "HALT INST" SWITCH ON THE LCDS MOTHERBOARD MUST BE
   46               ; IN THE "DEBUG" POSITION BEFORE EXECUTION.
   47
```

```
SC/MP ASSEMBLER REV-A
PNLPGM SC/MP PROM PROGRAMMER
POINTERS AND CONSTANTS

                        .PAGE   'POINTERS AND CONSTANTS'

0000                    .=0

        0001    P1      =       1
        0002    P2      =       2
        0003    P3      =       3

        8000    PPRGMR  =       08000           ;PERIPHERAL ADDR  OF PROM
                                                ;  PROGRAMMER BOARD
        0014    VP      =       014             ;ORDER CODE FOR PROG.  VOLTAGE
        000C    RD      =       0C              ;ORDER CODE FOR READ
        0004    VSS     =       04              ;ORDER CODE FOR VSS,VBB,VDD
        001C    CS      =       01C             ;ORDER CODE FOR CHIP SELECT
        0000    LOAD    =       0               ;ORDER CODE TO LOAD DATA
        0001    CLK     =       1               ;ORDER CODE TO CLOCK COUNTER
        0002    RDPRM   =       2               ;ORDER CODE TO READ PROM
                                                ;  DATA
        0003    CLR     =       3               ;ORDER CODE TO CLEAR COUNTER
        0004    ENBL    =       4               ;ORDER CODE TO ENABLE CONTROL
                                                ;  LATCH
        77D0    RAM     =       077D0           ;RAM POINTER TO MOTHERBOARD
                                                ;  R/W MEMORY
        0000    HI      =       0               ;TEMPORARY LOCATIONS IN RAM
        FFFF    LO      =       -1
        FFFE    SAVLO   =       -2
        FFFD    SAVHI   =       -3
        FFFC    HCNT    =       -4
        FFFB    DPLO    =       -5
        FFFA    DPHI    =       -6
```

```
SC/MP ASSEMBLER REV-A
PNLPGM SC/MP PROM PROGRAMMER
PROM ACCESS AND PROGRAMMING ROUTINES


   79                       .PAGE   'PROM ACCESS AND PROGRAMMING ROUTINES'
   80
   81                ; *** ROUTINE TO CHECK PROM FOR ERASED CONDITION ***
   82
   83 0000 08                NOP
   84                CKERSD:
   85 0001 C408              LDI     L(ERASED)-1
   86 0003 31                XPAL    P1
   87 0004 C400              LDI     H(ERASED)
   88 0006 35                XPAH    P1
   89 0007 3D                XPPC    P1
   90 0008 00                HALT                        ;HALT IF ERASED
   91
   92                ; THIS SUBROUTINE IS ALSO CALLED BY "PROG:" TO VERIFY THAT
   93                ; THE PROM IS ERASED.
   94
   95                ERASED:
   96 0009 C4D0              LDI     L(RAM)              ;INIT RAM POINTER
   97 000B 32                XPAL    P2
   98 000C C477              LDI     H(RAM)
   99 000E 36                XPAH    P2
  100                ERAS2:
  101 000F C480              LDI     H(PPRGMR)           ;SET ADDR. OF PROGRAMMER
  102 0011 37                XPAH    P3
  103 0012 C400              LDI     L(PPRGMR)
  104 0014 33                XPAL    P3
  105 0015 C401              LDI     1                   ;SET UPPER COUNT
  106 0017 CA00              ST      HI(P2)              ;STACK IS EMPTY, USE AS PTR.
  107 0019 CB0C              ST      RD(P3)              ;SET READ MODE
  108 001B CB1C              ST      CS(P3)              ;SELECT PROM SOCKET
  109 001D C400              LDI     0                   ;SET LOWER COUNT
  110 001F CAFF              ST      LO(P2)
  111 0021 CB03              ST      CLR(P3)             ;CLEAR PROM COUNTER
  112 0023 CB00              ST      LOAD(P3)            ;CLEAR DATA LATCHES FOR READ
  113                ELOOP:
  114 0025 C302              LD      RDPRM(P3)           ;READ DATA OUT OF PROM
  115 0027 9C0B              JNZ     NOT                 ;DATA NOT ZERO? NOT ERASED
  116 0029 CB01              ST      CLK(P3)             ;DATA OK, BUMP COUNTER
  117 002B BAFF              DLD     LO(P2)              ;DECREMENT LOWER COUNT
  118 002D 9CF6              JNZ     ELOOP               ;NOT DONE YET
  119 002F BA00              DLD     HI(P2)              ;DECREMENT UPPER COUNT
  120 0031 94F2              JP      ELOOP               ;NOT DONE YET
  121 0033 3D                XPPC    P1                  ;PROM IS ERASED
  122                NOT:
  123 0034 00                HALT                        ;HALT IF PROM NOT ERASED
  124
  125                ; *** ENTRY POINT TO PROGRAM PROM W/O CHECK FOR ERASED ***
  126
  127                WOCHK:
  128 0035 02                CCL
  129 0036 C477              LDI     H(RAM)              ;INIT RAM POINTER
  130 0038 36                XPAH    P2
  131 0039 C4D0              LDI     L(RAM)
  132 003B 32                XPAL    P2
```

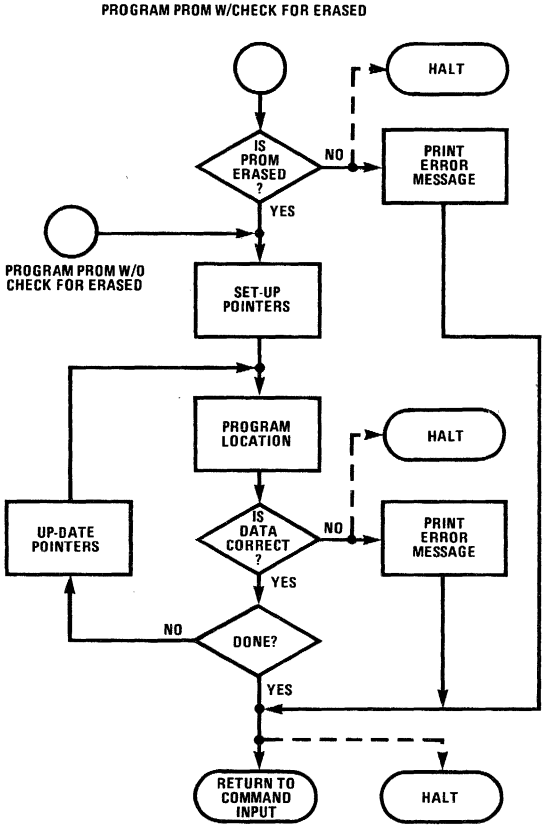
```
SC/MP ASSEMBLER REV-A
PNLPGM SC/MP PROM PROGRAMMER
PROM ACCESS AND PROGRAMMING ROUTINES


  133 003C C480           LDI     H(PPRGMR)
  134 003E 37             XPAH    P3
  135 003F C400           LDI     L(PPRGMR)
  136 0041 33             XPAL    P3
  137 0042 35             XPAH    P1
  138 0043 F402           ADI     2               ;ADD 512 OFFSET
  139 0045 35             XPAH    P1
  140 0046 9019           JMP     SET
  141
  142             ; *** ENTRY POINT TO PROGRAM PROM W/CHECK FOR ERASED ***
  143
  144             ;       PROM IS PROGRAMMED FROM MOST SIGNIFICANT ADDRESS TO
  145             ;       LEAST SIGNIFICANT ADDRESS DUE TO INVERSION OF COUNTER.
  146
  147             PROG:
  148 0048 02             CCL
  149 0049 C4D0           LDI     L(RAM)
  150 004B 32             XPAL    P2
  151 004C C477           LDI     H(RAM)
  152 004E 36             XPAH    P2
  153 004F 31             XPAL    P1              ;SAVE ADDRESS.
  154 0050 CAFE           ST      SAVLO(P2)
  155 0052 35             XPAH    P1
  156 0053 CAFD           ST      SAVHI(P2)
  157 0055 C40E           LDI     L(ERAS2)-1      ;CHECK PROM FOR ERASED
  158 0057 31             XPAL    P1
  159 0058 3D             XPPC    P1
  160 0059 C2FE           LD      SAVLO(P2)
  161 005B 31             XPAL    P1
  162 005C C2FD           LD      SAVHI(P2)
  163 005E F402           ADI     2               ;ADD 512 OFFSET
  164 0060 35             XPAH    P1
  165 0061 C401   SET:    LDI     1
  166 0063 CA00           ST      HI(P2)          ;SET UPPER LOC COUNT
  167 0065 C400           LDI     0
  168 0067 CAFF           ST      LO(P2)          ;SET LOWER LOC COUNT
  169 0069 CB03           ST      CLR(P3)         ;CLEAR PROM COUNTER
  170             NXTLOC:
  171 006B C5FF           LD      @-1(P1)         ;GET DATA TO PROGRAM
  172 006D 01             XAE                     ;SAVE IN EXTENSION REG.
  173             THSLOC:
  174 006E C400           LDI     H(PPROM)        ;SET ADDR.  OF PROGRAMMING RTN
  175 0070 35             XPAH    P1
  176 0071 CAFD           ST      SAVHI(P2)       ;SAVE PTR ADDR.
  177 0073 C4CC           LDI     L(PPROM)-1
  178 0075 31             XPAL    P1
  179 0076 CAFE           ST      SAVLO(P2)
  180 0078 C4FE           LDI     -2              ;SET COUNT
  181 007A CAFC           ST      HCNT(P2)        ;SAVE HIT COUNT IN RAM
  182             GO:
  183 007C 3D             XPPC    P1
  184 007D 60             XRE                     ;CHECK PROM DATA
  185 007E 9805           JZ      OK              ;PROM DATA CORRECT, DO X+5X
  186 0080 BAFC           DLD     HCNT(P2)        ;DECREMENT HIT COUNT
```

```
SC/MP ASSEMBLER REV-A
PNLPGM SC/MP PROM PROGRAMMER
PROM ACCESS AND PROGRAMMING ROUTINES


 187 0082 9CF8            JNZ     GO              ;CHECK FOR MAX. HIT
 188              NPROG:
 189 0084 00              HALT                    ;HIT COUNT OVER MAX, BAD PROM
 190              OK:
 191 0085 02              CCL
 192 0086 C400            LDI     0
 193 0088 CAFA            ST      DPHI(P2)        ;CLEAR UPPER D.P. COUNT
 194 008A FAFC            CAD     HCNT(P2)        ;COMPLEMENT HIT COUNT
 195 008C CAFC            ST      HCNT(P2)
 196 008E 02              CCL                     ;CLEAR CARRY/LINK FLAG
 197 008F F2FC            ADD     HCNT(P2)        ;COMPUTE 5X
 198 0091 CAFB            ST      DPLO(P2)
 199 0093 C400            LDI     0
 200 0095 F2FA            ADD     DPHI(P2)
 201 0097 CAFA            ST      DPHI(P2)        ;2X
 202 0099 02              CCL
 203 009A C2FB            LD      DPLO(P2)
 204 009C F2FB            ADD     DPLO(P2)
 205 009E CAFB            ST      DPLO(P2)
 206 00A0 C2FA            LD      DPHI(P2)
 207 00A2 F2FA            ADD     DPHI(P2)
 208 00A4 CAFA            ST      DPHI(P2)        ;4X
 209 00A6 02              CCL
 210 00A7 C2FC            LD      HCNT(P2)
 211 00A9 F2FB            ADD     DPLO(P2)
 212 00AB CAFB            ST      DPLO(P2)
 213 00AD C400            LDI     0
 214 00AF F2FA            ADD     DPHI(P2)
 215 00B1 CAFA            ST      DPHI(P2)        ;5X
 216              PRLP:
 217 00B3 3D              XPPC    P1              ;PROGRAM PROM
 218 00B4 BAFB            DLD     DPLO(P2)        ;DECREMENT LOWER COUNT
 219 00B6 9CFB            JNZ     PRLP            ;NOT DONE
 220 00B8 BAFA            DLD     DPHI(P2)        ;DECREMENT UPPER COUNT
 221 00BA 94F7            JP      PRLP            ;NOT DONE
 222 00BC C2FE            LD      SAVLO(P2)       ;RESTORE P1
 223 00BE 31              XPAL    P1
 224 00BF C2FD            LD      SAVHI(P2)
 225 00C1 35              XPAH    P1
 226              UPDATE:
 227 00C2 CB01            ST      CLK(P3)         ;BUMP PROM COUNTER
 228 00C4 BAFF            DLD     LO(P2)          ;DECREMENT LOWER LOC COUNT
 229 00C6 9CA3            JNZ     NXTLOC          ;NOT DONE
 230 00C8 BA00            DLD     HI(P2)          ;DECREMENT UPPER LOC COUNT
 231 00CA 949F            JP      NXTLOC          ;NOT DONE
 232 00CC 00              HALT                    ;HALT WHEN DONE
 233              PPROM:
 234 00CD C400            LDI     0
 235 00CF CB0C            ST      RD(P3)          ;TURN OFF READ MODE AND
 236 00D1 CB1C            ST      CS(P3)          ;  CHIP SELECT
 237 00D3 40              LDE
 238 00D4 CB00            ST      LOAD(P3)        ;SEND DATA TO PROGRAMMER
 239 00D6 C401            LDI     1
 240 00D8 CB04            ST      VSS(P3)         ;TURN ON VSS VOLTAGE
```

```
 241 00DA C47F            LDI     07F             ;WAIT 500 MICROSECONDS
 242 00DC 8F00            DLY     0
 243 00DE CB14            ST      VP(P3)          ;TURN ON PROGRAM PULSE
 244 00E0 C4FF            LDI     0FF
 245 00E2 8F00            DLY     0               ;DELAY 1 MS
 246 00E4 C400            LDI     0
 247 00E6 CB14            ST      VP(P3)          ;TURN OFF VP
 248 00E8 C414            LDI     20              ;WAIT 100 MICROSECONDS
 249 00EA 8F00            DLY     0
 250 00EC C400            LDI     0
 251 00EE CB04            ST      VSS(P3)         ;TURN OFF VSS VOLTAGE
 252 00F0 C414            LDI     20              ;WAIT 100 MICROSECONDS
 253 00F2 8F00            DLY     0
 254 00F4 CB0C            ST      RD(P3)          ;SET UP READ MODE
 255 00F6 CB1C            ST      CS(P3)          ;SELECT PROM SOCKET
 256 00F8 C400            LDI     0
 257 00FA CB00            ST      LOAD(P3)        ;CLEAR DATA LATCHES
 258 00FC C302            LD      RDPRM(P3)       ;READ DATA FROM PROM
 259 00FE 3D              XPPC    P1
 260 00FF 90CC            JMP     PPROM
 261
 262             ; *** COPY PROM TO RANGE IN MEMORY ***
 263
 264             COPY:
 265 0101 02              CCL
 266 0102 C477            LDI     H(RAM)
 267 0104 36              XPAH    P2
 268 0105 C4D0            LDI     L(RAM)
 269 0107 32              XPAL    P2              ;INIT RAM POINTER
 270 0108 31              XPAL    P1
 271 0109 CAFE            ST      SAVLO(P2)
 272 010B 35              XPAH    P1
 273 010C F402            ADI     2               ;ADD 512 OFFSET
 274 010E CAFD            ST      SAVHI(P2)
 275 0110 C401            JS      P1,SETRD        ;SET READ MODE
     0112 35C4
     0114 5931
     0116 3D
 276 0117 C2FD            LD      SAVHI(P2)       ;RETRIEVE ADDRESS
 277 0119 35              XPAH    P1
 278 011A C2FE            LD      SAVLO(P2)
 279 011C 31              XPAL    P1
 280             CPLOOP:
 281 011D C302            LD      RDPRM(P3)       ;GET PROM DATA
 282 011F CDFF            ST      @-1(P1)         ;STORE INTO MEMORY
 283 0121 CB01            ST      CLK(P3)         ;BUMP PROM COUNTER
 284 0123 BAFF            DLD     LO(P2)          ;DECREMENT LOC COUNTER LOW
 285 0125 9CF6            JNZ     CPLOOP
 286 0127 BA00            DLD     HI(P2)          ;DECREMENT LOC COUNTER HIGH
 287 0129 94F2            JP      CPLOOP          ;NOT DONE
 288 012B 00              HALT                    ;HALT WHEN DONE
 289
 290             ; *** VERIFY PROM AGAINST RANGE IN MEMORY ***
 291
```

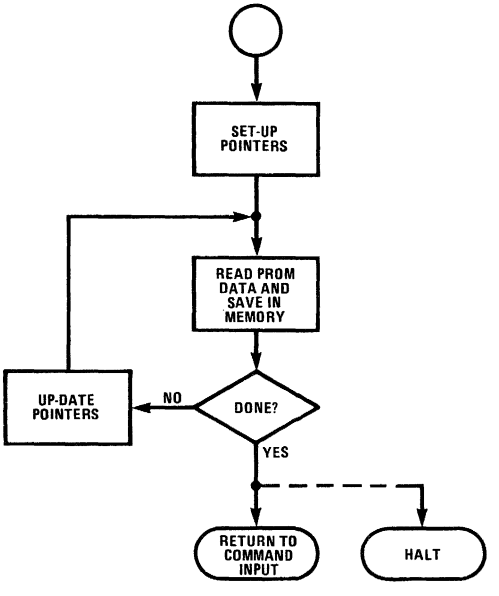
```
SC/MP ASSEMBLER REV-A
PNLPGM SC/MP PROM PROGRAMMER
PROM ACCESS AND PROGRAMMING ROUTINES


 292                VERIFY:
 293 012C 02                CCL
 294 012D C477              LDI     H(RAM)
 295 012F 36                XPAH    P2
 296 0130 C4D0              LDI     L(RAM)
 297 0132 32                XPAL    P2              ;INIT RAM POINTER
 298 0133 31                XPAL    P1
 299 0134 CAFE              ST      SAVLO(P2)
 300 0136 35                XPAH    P1
 301 0137 F402              ADI     2               ;ADD 512 OFFSET
 302 0139 CAFD              ST      SAVHI(P2)
 303 013B C401              JS      P1,SETRD        ;SET READ MODE
     013D 35C4
     013F 5931
     0141 3D
 304 0142 C2FD              LD      SAVHI(P2)       ;RETRIEVE ADDRESS
 305 0144 35                XPAH    P1
 306 0145 C2FE              LD      SAVLO(P2)
 307 0147 31                XPAL    P1
 308                VLOOP:
 309 0148 C302              LD      RDPRM(P3)       ;GET DATA FROM PROM
 310 014A E5FF              XOR     @-1(P1)         ;COMPARE AGAINST MEMORY DATA
 311 014C 9C0B              JNZ     NOVFY           ;DOES NOT VERIFY
 312 014E CB01              ST      CLK(P3)         ;BUMP PROM COUNTER
 313 0150 BAFF              DLD     LO(P2)          ;DECREMENT LOC COUNTER LOW
 314 0152 9CF4              JNZ     VLOOP           ;NOT DONE
 315 0154 BA00              DLD     HI(P2)          ;DECREMENT LOC COUNTER HIGH
 316 0156 94F0              JP      VLOOP           ;NOT DONE
 317 0158 00                HALT                    ;HALT WHEN DONE
 318                NOVFY:
 319 0159 00                HALT                    ;HALT ON ERROR
 320                SETRD:
 321 015A C480              LDI     H(PPRGMR)       ;PUT ADDR. OF PROGRAMMER
 322 015C 37                XPAH    P3              ;  IN P3
 323 015D C400              LDI     L(PPRGMR)
 324 015F 33                XPAL    P3
 325 0160 C401              LDI     1               ;SET UPPER LOC COUNTER
 326 0162 CA00              ST      HI(P2)
 327 0164 CB0C              ST      RD(P3)          ;SET READ MODE
 328 0166 CB1C              ST      CS(P3)          ;SELECT PROM SOCKET
 329 0168 C400              LDI     0
 330 016A CAFF              ST      LO(P2)
 331 016C CB03              ST      CLR(P3)         ;CLEAR PROM COUNTER
 332 016E CB00              ST      LOAD(P3)        ;CLEAR PROM DATA LATCHES
 333 0170 3D                XPPC    P1
 334
 335      0000              .END
```

Appendix 2



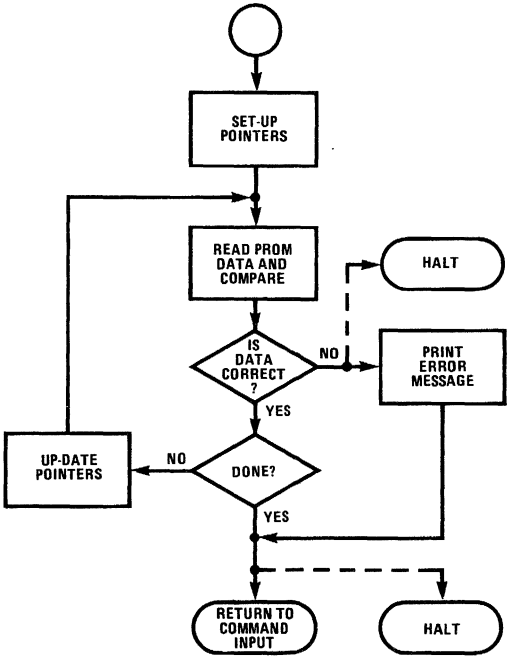
NOTE: DASHED LINES INDICATE PANEL PROGRAM ERRORS & EXITS.

COPY PROM INTO MEMORY



5

VERIFY PROM AGAINST MEMORY



Bipolar PROM Programming Procedure

These parts are shipped from the factory with all fuses intact. As a result, the outputs will be low (logical "0") for all addresses. In order to generate a high level on the outputs, the part must be programmed. Information on available programming equipment may be obtained from National. However, if it is desired to build your own programmer, the following conditions must be observed.

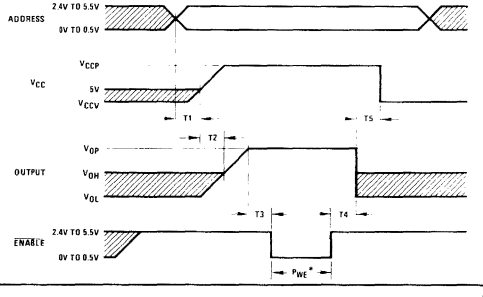
1. Programming should be attempted only at temperatures between 15°C and 30°C.
2. Addresses and chip enable pins must be driven from normal TTL logic levels during both programming and verification.
3. Programming will occur at a selected address when V_{CC} is held at 10.5V, the appropriate output is held at 10.5V and the chip is subsequently enabled. To achieve these conditions in the appropriate sequence, the following procedure must be followed:
   a) Select the desired word by applying a high or low level to the appropriate address inputs. Disable the chip by applying a high level to one or both enable inputs.
   b) Increase V_{CC} to 10.5V ±0.5V with the rate of increase being between 1.0 and 10.0V/μs. Since V_{CC} supplies the current to program the fuse as well as the I_{CC} of the device at programming voltage, it must be capable of supplying 750 mA at 11.0V.
   c) Select the output where a high level is desired by raising that output voltage to 10.5V ±0.5V. Limit the rate of increase to a value between 1.0 and 10.0V/μs. This voltage change may occur simultaneously with the increase in V_{CC} but must not precede it. It is critical that only one output at a time be programmed since the internal circuits can only supply programming current to one bit at a time. Outputs not being programmed must be left open or tied to a high impedance source of at least 20 kΩ. (Remember that the outputs of the device are still disabled at this time because the chip enables are high.)
   d) Enable the device by taking both chip enables to a low level. This is done with a pulse of 10μs. The 10μs duration refers to the time that the circuit is enabled. Normal input levels are used and rise and fall times are not critical.
   e) Verify that the bit has been programmed by first removing the programming voltage from the output and then reducing V_{CC} to 4.0V ±0.2V. Verification at a V_{CC} level of 4.0V will guarantee proper output states over the V_{CC} and temperature range of the programmed part. The chip must be enabled to sense the state of the outputs. During verification, the loading of the output must be within specified I_{OL} and I_{OH} limits. Steps b, c and d must be repeated 10 times or until verification that the bit has programmed.
   f) Following verification, apply five additional programming pulses to the bit being programmed. The programming procedure is now complete for the selected bit.
   g) Repeat steps a through f for each bit to be programmed to a high level. If the procedure is performed on an automatic programmer, the duty cycle of V_{CC} at programming voltage must be limited to a maximum of 25%. This is necessary to minimize chip junction temperatures. After all selected bits are programmed, the entire contents of the memory should be verified.

Note: Since only an enabled chip is programmed, it is possible to program these parts at the board level if all programming parameters are complied with.

Programming Parameters Do not test or you may program the device.

PARAMETERS		CONDITIONS	MIN	RECOMMENDED VALUE	MAX	UNITS
V_{CCP}	Required V_{CC} for Programming		10.0	10.5	11.0	V
I_{CCP}	I_{CC} During Programming	V_{CC} = 11V			750	mA
V_{OP}	Required Output Voltage for Programming		10.0	10.5	11.0	V
I_{OP}	Output Current while Programming	V_{OUT} = 11V			20	mA
t_{RR}	Rate of Voltage Change of V_{CC} or Output		1.0		10.0	V/μs
P_{WE}	Programming Pulse Width (Enabled)		9	10	11	μs
V_{CCV}	Required V_{CC} for Verification		3.8	4.0	4.2	V
M_{DC}	Maximum Duty Cycle for V_{CC} at V_{CCP}			25	25	%

Programming Waveforms

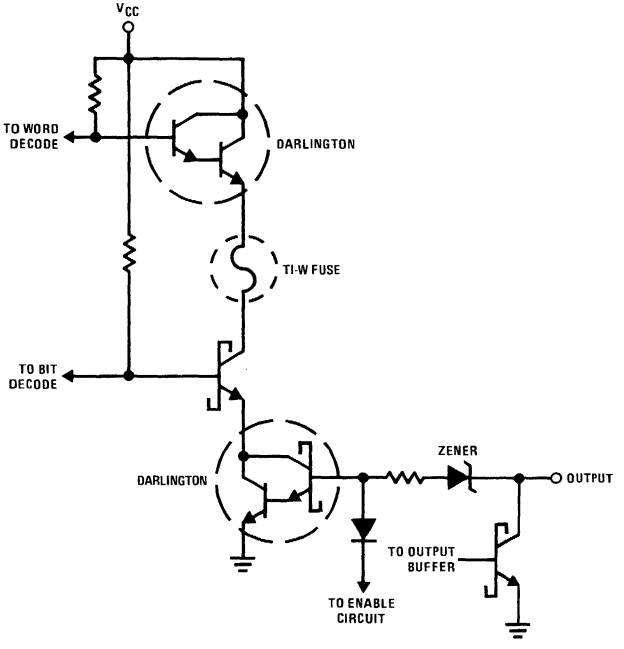


T1 = 100 ns min
T2 = 5μs min (T2 may be ≥ 0 if V_{CCP} rises at the same rate or faster than V_{OP})
T3 = 100 ns min
T4 = 100 ns min
T5 = 100 ns min

*P_{WE} is repeated for 5 additional pulses after verification of V_{OH} indicates a bit has programmed

Equivalent Circuit

Programming Equivalent Circuit for One Memory Output
(Applies to All NSC Generic Schottky PROMs)



5

Programming Equipment for National PROMs

National Semiconductor manufactures both Schottky TTL and MOS PROMs in the industry standard pinouts and organizations. See the table below for available device types.

The 2k and 4k MOS PROMs are fabricated using a silicon gate, p-channel process. The MM2708 is fabricated using a silicon gate, n-channel process. Different personality modules are required for each device type.

The bipolar PROMs are all fabricated using a Schottky TTL process. The fuses are of Ti-W material. A single, generic module is used for all bipolar PROMs. All bipolar PROMs are also supplied with all outputs low in the initial state. Positive logic is used to "program" logic 1s where desired.

National's Tri-Safe™ programming procedure ensures fast, reliable programming. After the proper address location is selected and the output and V_{CC} pins have been raised to 10.5 V_{DC}, the devices are programmed when the enable pin is taken low. Since only an enabled device is programmed, it is possible to program these devices at the board level.

For complete programming procedures and specifications, consult National Semiconductor.

Commercially Available Authorized Programming Equipment

Device	Size	Data I/O Module	Data I/O Adapter	Pro Log Module	Pro Log Configuration	Pro Log Adapter
BIPOLAR PROMs						
DM54/74S188/288	32x8	909-1063-5	715-1037	PM9047	32x8 (L)	PA16-2
DM54/74S387/287	256x4	909-1063-5	715-1035-1	PM9047	256x4 (L)	PA16-1
DM54/74S570/571	512x4	909-1063-5	715-1035-2	PM9047	512x4 (L)	PA16-1
DM54/74S572/573	1024x4	909-1063-5	715-1039-3	PM9047	1024x4 (L)	PA18-2
DM54/74S574	1024x4	909-1063-5	715-1406	PM9047	1024x4 (L)	PA18-4
DM77/87S295/296	512x8	909-1063-5	715-1033-2	PM9047	512x8 (L)	PA24-1
MOS EPROMs						
MM1702A	256x8	909-1183-1	715-1047	PM9001A		
MM5203	256x8	909-1178-1	715-1047	PM9002A		
MM5204	512x8	909-1177-1	715-1033	PM9006A		
MM2708	1024x8	909-1174-1	715-1033-3	PM9005A		

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EPROM Notes

Although EPROMs are in widespread use there are continuing problems associated with erasure and programming. The following indicates some of the pitfalls:

Erasure

Erasure seems so simple that it is often not considered when a problem arises. Under-erasure can be a direct cause of under-programming when an inter-active programmer is used. Periodic calibration of the erase system is all that is necessary to provide proper erasure. Changing bulbs (and aging bulbs), changing manufacturers, changing distance from the lamp and changing package type, especially the quartz lid, should be a stimulus for recalibrating the erase system. Over-erasure has so far not been a proven problem, but erasing more than 10 times longer than the time needed to erase a part should be avoided. Then there will be no question of over-erasure. Lamps with short wavelength (< 1800 Å) and high intensity are believed to ionize oxide with long exposure. The theory is that this will shift the threshold until the part will not function correctly. This is not a permanent shift and an overnight bake at 225°C for gold plated parts or a 24-hour bake at 150°C for tin plated parts should correct the problem.

Some EPROMs exhibit a sensitivity to ambient light. This does not erase them, but they may not function properly when minute photoelectric currents (leakage) are being generated. This is a common phenomenon with most semiconductors. Covering the lid with some opaque material is a prudent practice.

Programming

Programming seems to be the assumed cause of all EPROM problems. As noted in the section on erasure, if a part is not fully erased, an interactive (intelligent) programmer will under-program the part. This would really be an erasure problem.

If the part is slow, or the system requires a faster access time than the part provides, intermittent operation sometimes occurs and the designer often assumes the parts aren't programmed correctly. This is a system/component specification problem.

Often the operating voltages of an EPROM are shifted to ease interface design in the system. This results in the parts being programmed to operate with the data sheet voltages and then operated with a different set of voltages in the system. This may lead to some of the parts not functioning correctly in the system even though they are properly programmed. This is especially true for the MM5204 which has the trip point of the internal sense amplifier altered if V_{LL} does not meet the conditions $V_{LL} = V_{SS} - (5.0V \pm 5\%)$.

Bootstrap circuitry in some EPROMs is slow to respond when the component is powered down (to save power) and then powered up to be accessed. The first cycle of operation can have a significantly longer access time *and* can be a function of the rise time of the power supply, if power is being switched.

If the part was not under-erased, has no system/component access time problem, is not operating under voltages different from the program (really the read conditions of programming) set, and provision for the longer access time of power-up has been made, perhaps the part was programmed improperly. Unfortunately, the symptoms can look the same in a system. If may appear to be access time, output levels, sensitivity to voltage and temperature variations, or just intermittent operation.

There are three basic problems encountered in programming EPROMs. The one most often encountered is improper voltage levels. The voltage applied to any pin must be maintained between the specified min and max levels for proper programming. This statement sounds reasonable but frequently this is not done. The high voltage levels required by some EPROMs are provided by designs with resistive pullups on the address inputs. The drop across the resistor during the program time causes the input voltage to be out of tolerance; active pullups eliminate this problem. Similarly, the power supplies must be able to supply sufficient current so that they maintain the specified voltage level. The FAMOS memory cells in EPROM must have sufficient voltage developed across them or they do not program! A second cause of programming malfunction may be incorrect timing. A third programmer problem occurs when not adhering to the duty cycle limitations. If the junction temperatures are raised too high due to power dissipation, a part may not program.

Section 6

CRT Display Applications

6

The introduction of microprocessors into the design of CRT terminal systems has greatly reduced component count. With this reduction has come an even further emphasis on cutting the number of parts in the video display portion of the system. National Semiconductor has addressed this problem with the introduction of the DP8350 series of CRT controllers and the DM8678 family of character generators. Together with LSI memory and microprocessors these devices allow construction of a low end terminal consisting of less than 20 components, while retaining wide flexibility for use in more sophisticated terminal designs. Additional component types are being developed for terminal applications and will be announced in the near future.

Simplify CRT Terminal Design with the DP8350

National Semiconductor
Application Note 198
Helge H. Mortensen*
March 1978

INTRODUCTION

This application note is a description of a "low cost" CRT data terminal card design, based upon National's CRT Controller (DP8350) and 8-bit N-channel microprocessor (SC/MP). The terminal has a minimum parts count and implements all TTY functions. Even with this minimum number of parts, the terminal provides some "smart" features by efficiently utilizing the available hardware. Screen scroll, RS-232C interface and adjustable baud-rate (up to 1200-baud) are featured on the card. Higher baud-rates are available on a word-by-word basis if the RS-232-handshake signal is used. The design also demonstrates use of 2 new microprocessor-interface parts: the Asynchronous Communications Element (ACE), for serial I/O; and the RAM Input/Output (RAM I/O), for keyboard scanning and scratch pad memory. A 2-kilobyte video RAM is implemented with four 1024 x 4-bit, static RAM chips (MM2114), and dot generation uses the DM8678 5 x 7 Character Generator.

The card is self-contained except for the CRT monitor and power supply. It holds a keyboard and monitor-interface circuitry. Monitors requiring separate video and sync signals (Ball Brothers), and those requiring composite video (Motorola) are accommodated.

System Architecture

Since system cost is typically somewhat proportional to parts count, arriving at a minimum parts count solution has been a goal throughout this design effort.

A full-blown CRT terminal is shown in *Figure 1* and its low cost counterpart in *Figure 2*. Address decoding details are omitted in both cases.

Removing overhead circuitry shown in *Figure 1*, and making use of the TRI-STATE® concept greatly facilitated the parts reduction effort.

Obviously, extreme time conflicts for communicating on the system busses are created because all essential parts require access. Let us investigate this problem a little further.

Because the CRT Controller does the CRT display refresh function, it must have access to a memory containing current data for display. This memory may be a shift register (octal, 80-bit line buffer in *Figure 1*) which is loaded at the first video line in a character row and then recirculated for the number of video lines in that character row. Using such a line buffer allows the microprocessor access to the system busses for more than 90% of the video time (screen time). On the other hand, by removing the buffer, the refresh circuit needs direct memory access (DMA) during video display time.

However, with the bidirectional data buffer and the TRI-STATE address buffer in the system, the situation is not yet too serious. (We are only preventing the SC/MP microprocessor from updating video RAM data or using the scratch pad during character display time.) Instruction fetch (ROM) and keyboard scanning are still not affected. However, with the saving of the data buffer and the address buffer, a well-organized "time share" of the busses is required. How does this limited bus access affect the time-critical features such as scroll and high baud rate?

Scroll

Several scrolling methods may be implemented with the CRT Controller. The most straightforward is a rewrite of memory. This requires long processing time and bus access and is not feasible with the minimum hardware indicated in *Figure 2*. Sensing when the CRT is scanning character-row 24 and then loading a new "row start" requires additional overhead circuitry. An alternative approach is to load a new "top of page" address for each scroll and have the video RAM "wrapped-around" when it is accessed by the CRT!

In the latter approach, the processor only has to clear a row in video RAM and load a register in the CRT Controller to perform a total-screen scroll. The only problem remaining is handling the location of the scratch pad in the video RAM address space. By using the RAM I/O chip for a keyboard scanning and scratch pad RAM, the problem is solved. An additional feature for the software programmer is that the keyboard and RAM are addressable within the reach of one 8-bit index register.

Maximizing Communication Baud Rate

Assuming that the processor has bus access only during the vertical blanking period and the ACE interrupt service subroutine is executed in less than this time, only one received data word could be processed per frame! The processor's task is to transfer the word from ACE to scratch pad memory, check for terminal or system control functions, write into the proper locations in video RAM and check the keyboard for "Break" (BRK). A quick calculation reveals 60 bits/second as the maximum baud rate! To improve communication speed, the processor must have bus access during the video frame scan time. Three of the 10 scan lines making up a character row are blanked except during cursor time. Using these three lines (minimum decoding required) for processor bus access during video time allows us to communicate at 1200 baud.

Note that the baud rate is limited by the frame rate in the first approach; in the second approach, the limitation is the real time required to execute the service routine. The calculation is performed as follows. Estimated execution time for service routine with 100% availability of the bus is 2 ms. However, bus access is only granted during 3 video lines in each character row which is worth 192 μs. In terms of video time, we need 10 character rows to finish the routine and be ready for the next interrupt. Display time for 10 character rows is 6.4 ms, which in turn is the time interval for one 10-bit word. This translates into a 1600-baud maximum capability if scroll is not included in the service routine.

*Refer to Introduction.

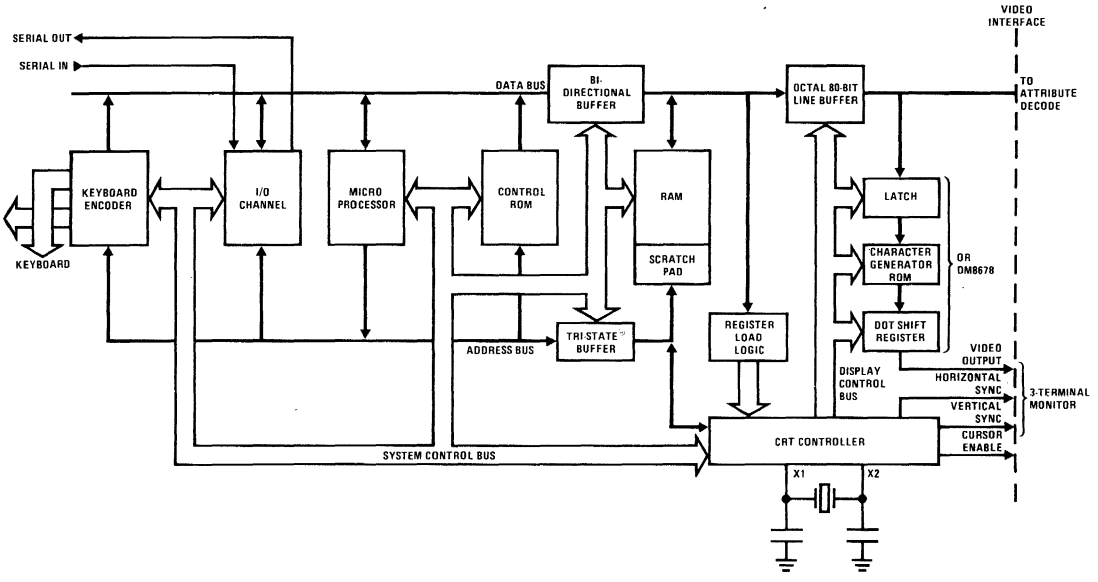


FIGURE 1. System Block Schematic Using Line Buffer, Address and Data Buffer

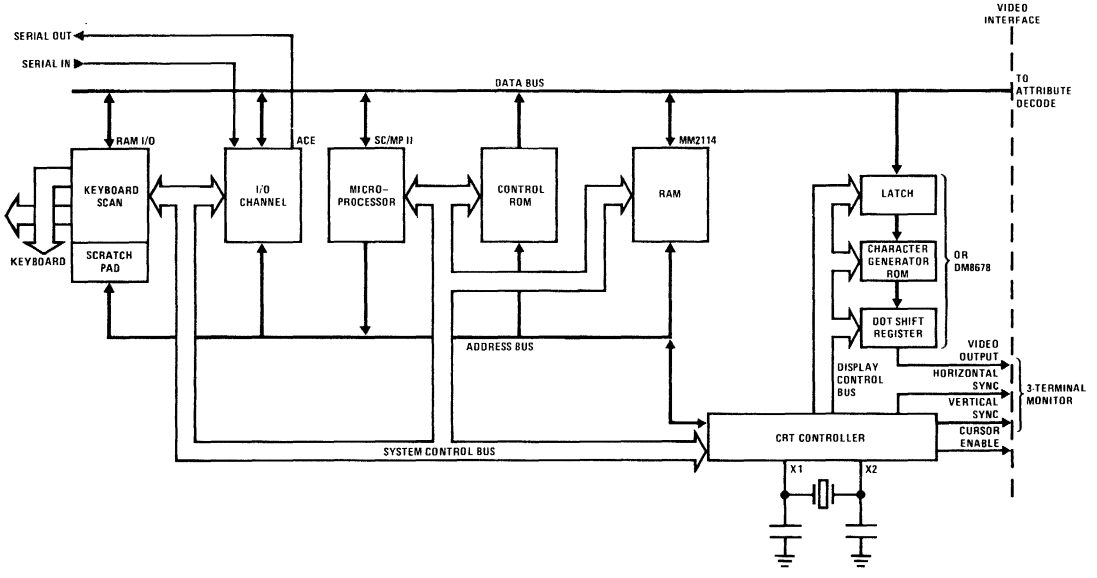


FIGURE 2. System Block Schematic for the Low Cost Terminal

Address Decoding

Holding parts to a minimum leads to a one ROM address decoding scheme. However, this does not coincide with minimum cost. Instead, 2 low-power Schottky MSI devices replace the ROM in the final design.

Memory Address Space Utilization

A very simple decoding scheme is facilitated by partitioning the processor memory space into 500-byte pages. The detailed memory map is shown in *Figure 3*. In addition, address bits 12 and 13 (multiplexed on the data bus), are used to map four 4-kilobyte pages, with the first page dedicated to processor peripherals and the following 3 pages dedicated to register loading of the CRT Controller. The 3 CRT Controller registers to be loaded are "top of page", "row start" and "cursor".

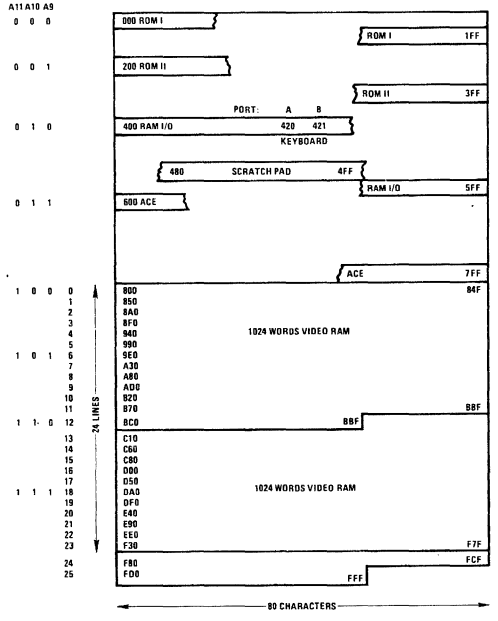


FIGURE 3. Memory Map

DISCUSSION OF SPECIFICATIONS

A device used to communicate with a computer is called interactive if it has the following properties:

a. Data may be entered on a keyboard and sent to the computer, which in turn echoes it back to the display.

b. Data may be received from the computer and displayed; keyboard is scanned for "Break" (BRK) entry by the operator of the system.

The concept of an interactive terminal is illustrated by the block diagram shown in *Figure 4*. To understand this, follow the data from the keyboard to the display and list the specifications for each block. An overall terminal specification is depicted in Table I.

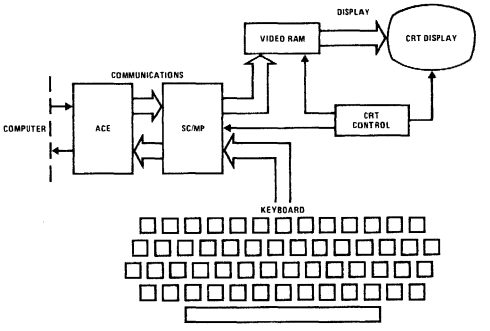


FIGURE 4. Block Diagram of an Interactive Terminal

TABLE 1. TERMINAL SPECIFICATIONS

Keyboard	
Style	Typewriter
Characters/code set	64/ASC II
Cursor controls	6
Keyboard encoder	Software
Communication	
Mode	Full duplex, half duplex option
Technique	Asynchronous
Communications protocol	ASC II
Code	ASC II
Bits/character	10/11
Speed, bits/second	110 to 1200 (19,200 word-by-word)
Operator selectable speeds	4
Format	Character
Terminal interface	RS-232, 20 mA current loop
Display	
Display positions, characters/display	1920
Display arrangement (line x characters)	24 x 80
Total display symbols	64
Symbol formation	5 x 7 dot matrix
Reverse video	Cursor and whole screen
Scrolling	Yes
Cursor type	Block, reverse video
Cursor position	Down, left, right, home and return, back space.

Keyboard

The keyboard is a copy of a standard teletypewriter with two-key rollover. The 54 keys can be broken into alphanumeric, punctuation, symbols, cursor control, and system control keys. The processor scans the keys at all times and translates any key closure into a unique code (ASC II), which is sent to the input/output channel for serial transmission to the computer. It should be noted that the RAM I/O chip has the capability of scanning 64 keys (8 x 8).

Communications

The input/output channel is based upon the Asynchronous Communication Element (ACE). This integrated circuit performs parallel-to-serial conversion of the data received from the keyboard, and serial-to-parallel conversion of data sent from the computer for display on the screen. When the system is initiated (power-up), the on-chip programmable baud generator is loaded with the desired baud rate (switch selectable). Start, stop, and parity bits are appended or deleted in this block of the system, depending on the direction of data flow. All control signals for the standard RS-232C interface are likewise generated here. Standard electrical specifications for RS-232C and 20 mA current loop are met by adding dedicated interface parts.

Display

After the data is received from the computer, it is stored in the video RAM. The CRT Controller chip refreshes the display at 60 Hz by sequentially addressing the video RAM; 1920 addresses are generated to fetch data for 24 lines of 80 characters. The standard 64-character ASC II set is displayed using a 5 x 7 dot-matrix block for each character. Data is entered from left to right and from top to bottom, until the screen is full. After that, upward scrolling with top-line overflow and newly cleared bottom line takes place automatically with line feed.

Software

A detailed flow chart of the software is shown in *Figure 5.* It is set up to service 3 major functions: a) initialize the system; b) scan the keyboard and c) service the ACE upon interrupt request.

a. Initialization
   The video RAM is cleared and the cursor is loaded at the upper left corner of the screen. ACE is set up with the desired baud rate and the interrupt enable flag is armed.

b. Keyboard Scan
   The keyboard is first checked for "Any Key Down" status. If positive, the keyboard is scanned and the binary code (ASC II) is computed by the program and read to ACE.

c. ACE Interrupt Service Routine
   When its receiver buffer is full, the ACE puts out an interrupt request. The SC/MP immediately suspends keyboard scanning and reads the buffer register. The main portion of this routine is checking incoming data for control functions and updating the video RAM and the CRT Controller registers. It should be noted that the need for executing this routine is the limiting factor for high baud rate communications.

Hardware

The detailed hardware implementation is shown in *Figure 6.* The CRT Controller grants the SC/MP microprocessor bus access during blanked scanlines and vertical blanking interval by logically OR-ing line counter outputs with the vertical blanking pulse and using this signal as a bus-available signal. The CRT Controller is held off the bus by disabling the TRI-STATE address output. This is done by applying logical "0" to the RAM address enable pin of the CRT Controller, the SC/MP then takes the bus as needed.

Sense-A of SC/MP is used as an interrupt request input whenever received data is available in the receiver buffer register of the ACE. The interrupt service routine is executed during vertical blanking and "inactive" video time as indicated above.

The keyboard is sensed for "Any Key Down" (under program control) by reading Port-B of the RAM I/O chip. Upon a positive result, the keys are scanned by a special sequence for key identification and encoding.

Mechanical

A PC board layout and its assembly is shown in *Figure 7.* Note that the keyboard is mounted directly on the card.

Acknowledgment

The development of the terminal involved significant contribution by a large number of people. The author would particularly like to express his appreciation to Len Bryson for software development and Dana Knight for invaluable suggestions and ideas during the hardware design phase.

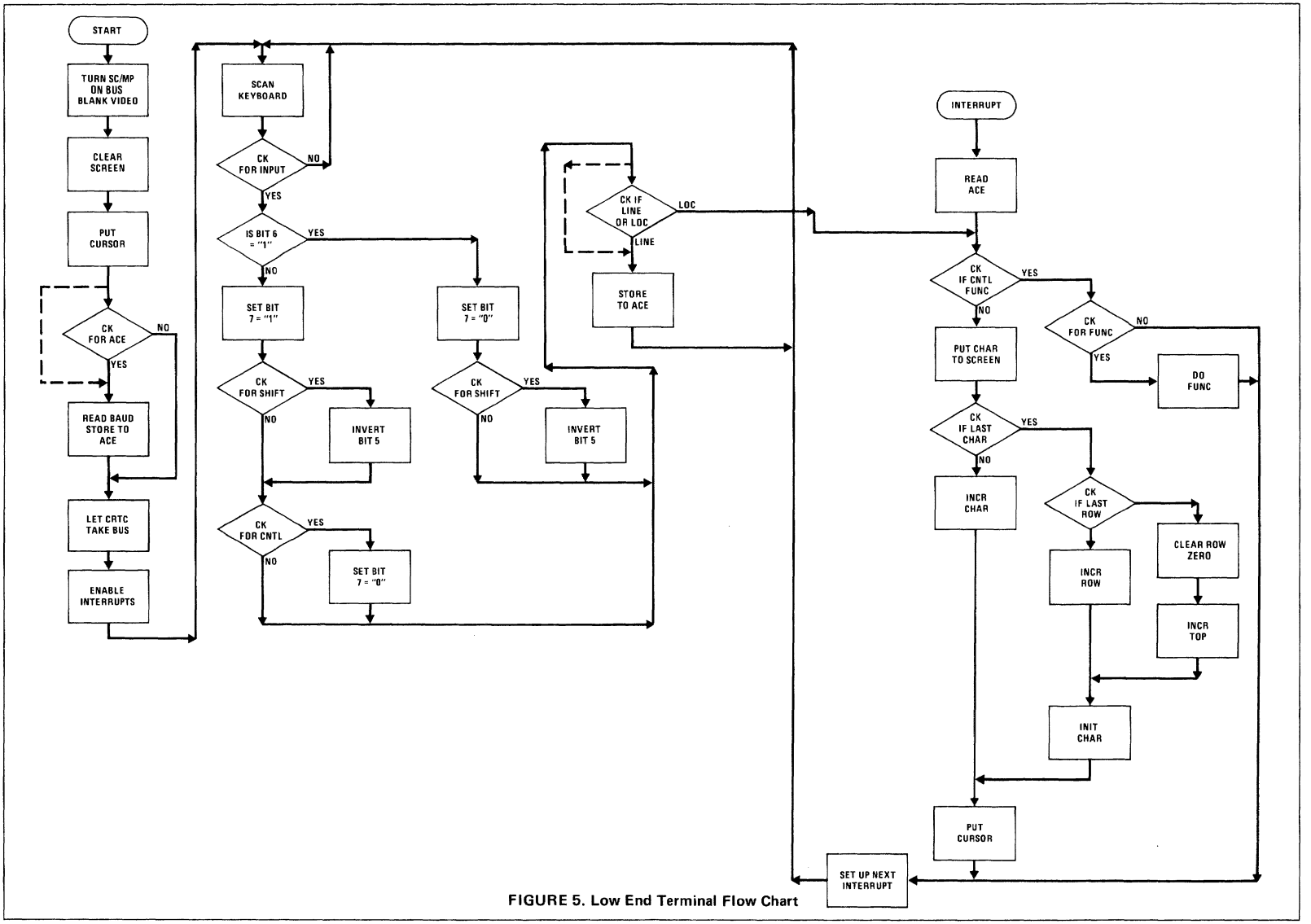


FIGURE 5. Low End Terminal Flow Chart

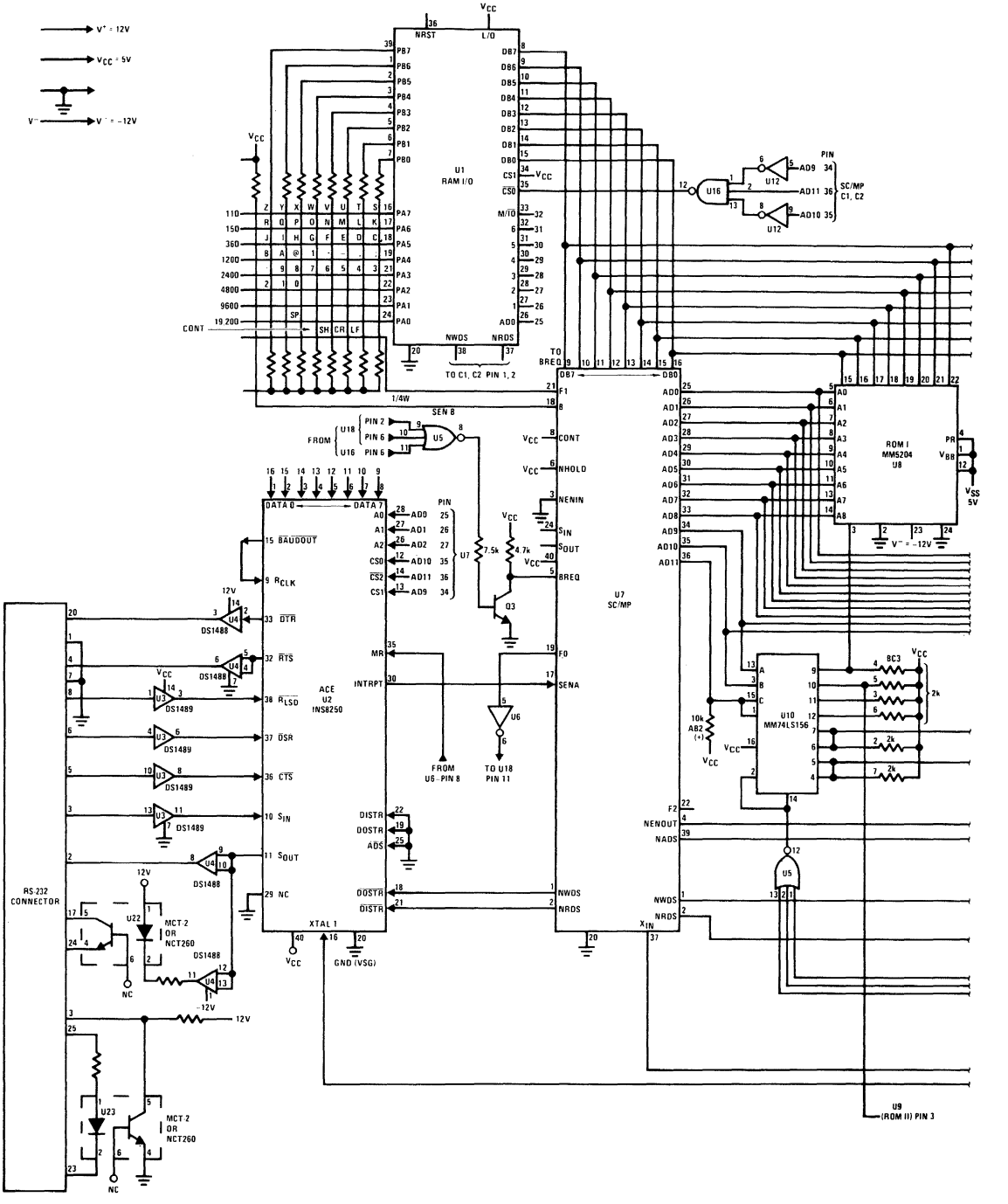


FIGURE 6. Low Cost CRT Terminal

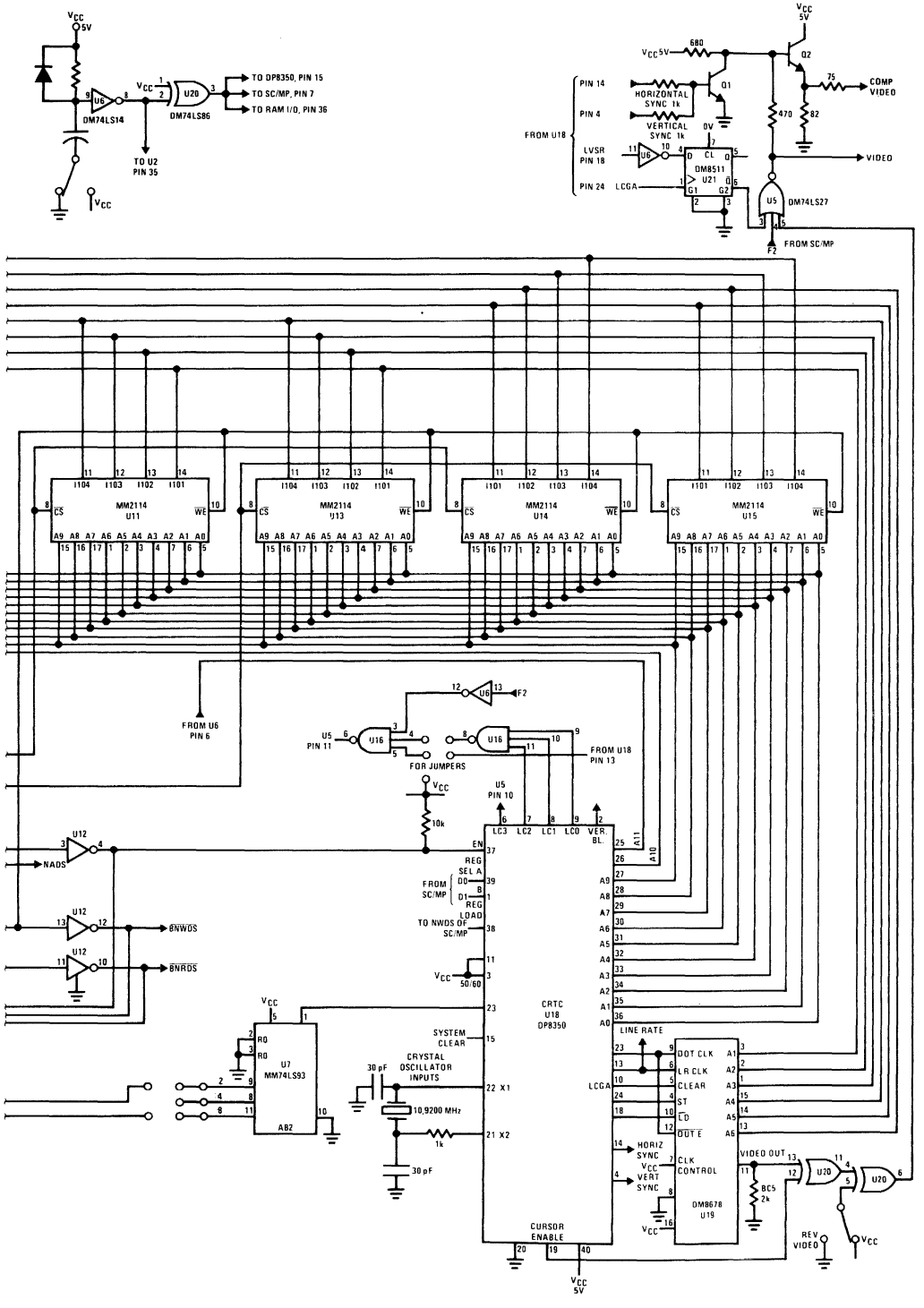


FIGURE 6. Low Cost CRT Terminal (Continued)

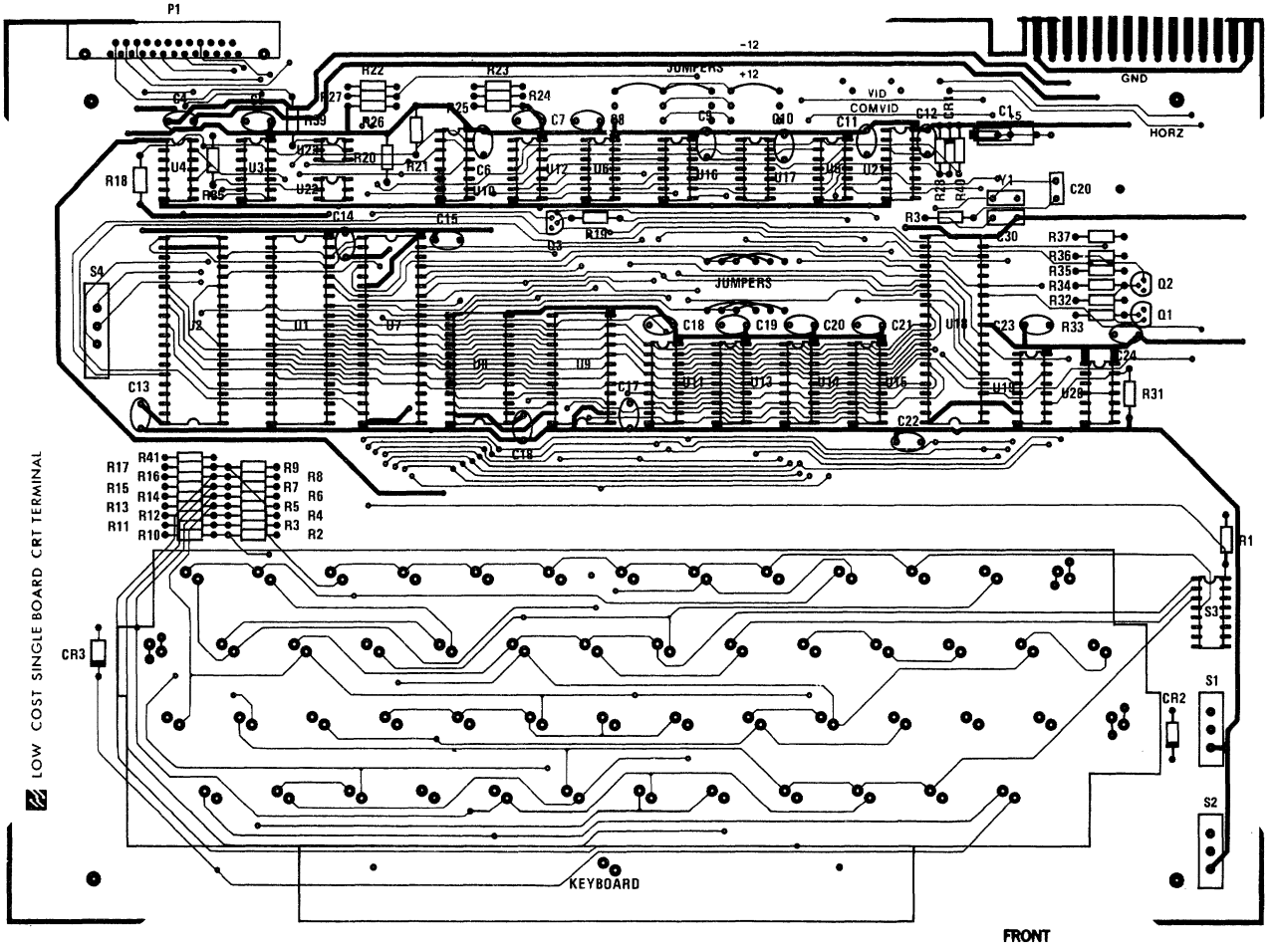


FIGURE 7A. PC Board Layout Assembly (Shown Half Size)

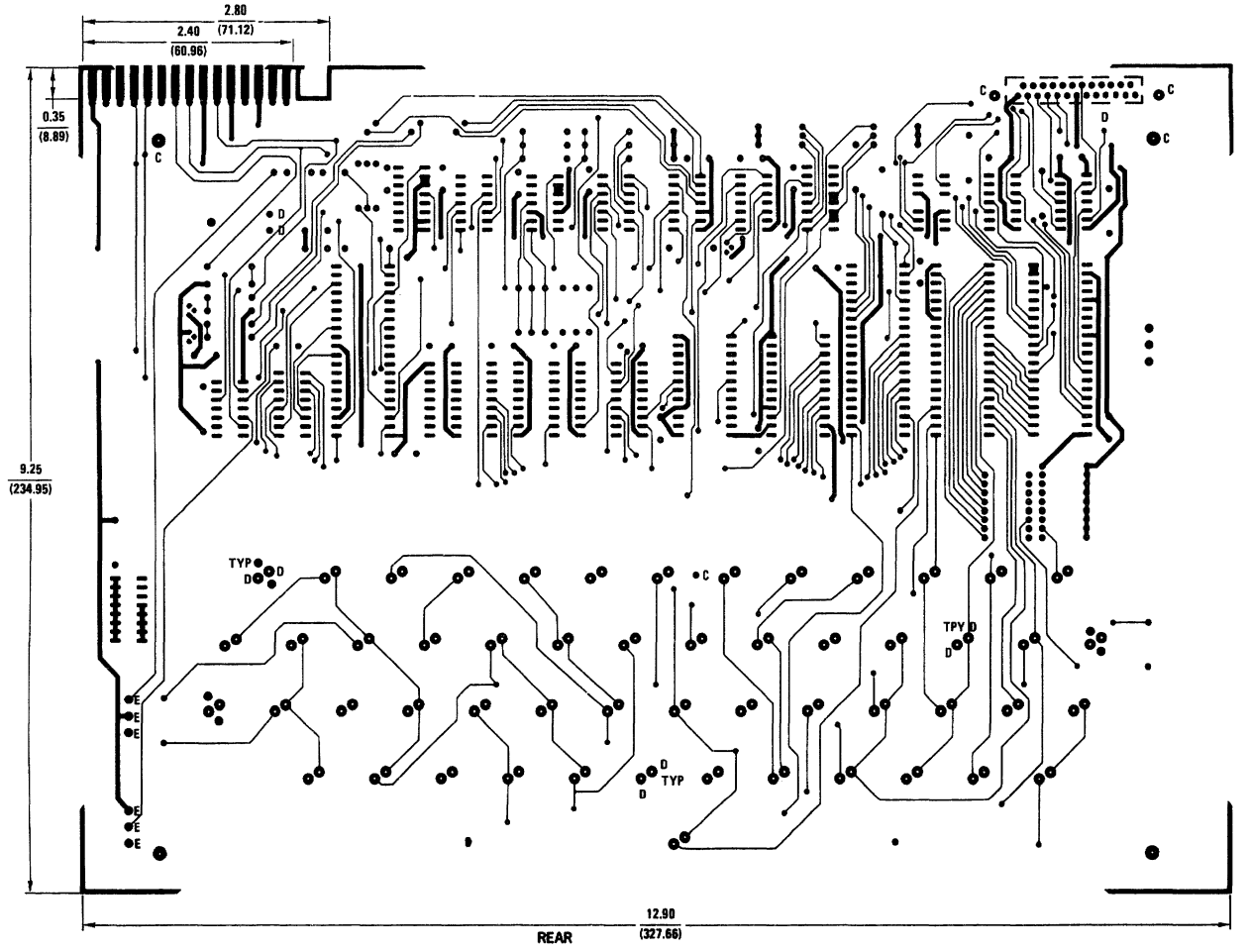


FIGURE 7B. PC Board Layout Fabrication (Shown Half Size)

National Semiconductor

Preliminary
FEBRUARY 1978

DP8350 Series Programmable CRT Controllers

General Description

The DP8350 Series of CRT Controllers are single-chip bipolar (I^2L technology) circuits in a 40-pin package. They are designed to be dedicated CRT display refresh circuits.

The CRT Controller (CRTC) provides an internal dot rate crystal controlled oscillator for ease of system design. For systems where a dot rate clock is already provided, an external clock input may be used by the CRTC. In either case system synchronization is made possible with the use of the buffered Dot Rate Clock Output.

The DP8350 Series has 11 character generation related timing outputs. These outputs are compatible for systems with or without line buffers, using character ROMS, or DM8678-type latch/ROM/shift register circuits.

12 bits (4k) of bidirectional TRI-STATE® character memory addresses are provided by the CRTC for direct interface to character memory.

Three on-chip registers provide for external loading of the row starting address, cursor address, and top-of-page address.

A complete set of video outputs is available including cursor enable, programmable vertical blanking, programmable horizontal sync, and programmable vertical sync.

The DP8350 Series CRTC provides for a wide range of programmability using internal mask programmable ROMs:

- Character Field (both number of dots/character and number of scan lines/character)
- Characters per Row
- Character Rows per Video Frame

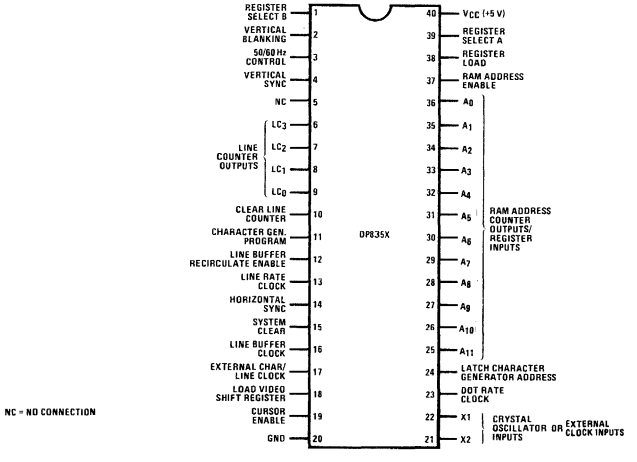
The CRTC also provides system sync and program inputs including 50/60 Hz control, system clear, external character/line rate clock, and character generator program.

The DP8350 Series operates on a single +5 V power supply. Outputs and inputs are TTL compatible.

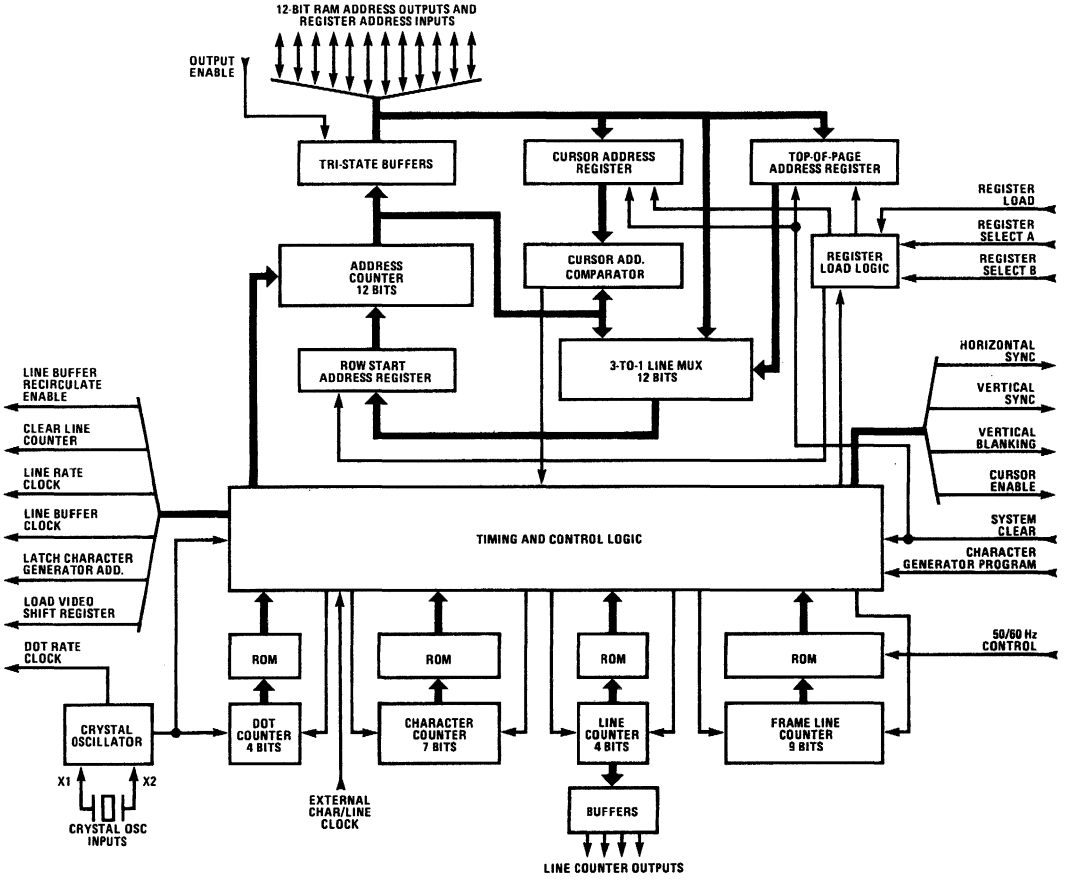
Features

- Internal crystal controlled dot rate oscillator
- External dot rate clock input
- Buffered dot rate clock output
- Timing pulses for character generation
- Character memory address outputs (12 bits)
- Internal cursor address register
- Internal row starting address register
- Top-of-page address register (for scrolling)
- Programmable horizontal and vertical sync outputs
- Programmable cursor enable output
- Programmable vertical blanking output
- 50/60 Hz refresh rate
- Programmable characters/row (5 to 110)
- Programmable character field size (up to 16 dots x 16 scan line field size)
- Programmable character rows/frame (1 to 64)
- Single +5 V power supply
- Inputs and outputs TTL compatible
- Ease of system design/application

DP8350 Series Connnnection Diagram



DP8350 Block Diagram



CHARACTER GENERATION/TIMING OUTPUTS

The CRTC provides 11 interface timing outputs for line buffers, character generator ROM, DM8678-type latch/ROM/shift register combination character generators, and system status timing. All outputs are TTL compatible and directly interface to popular system circuits, including:

- DM8678 Series Character Generators
- MM52157, MM52179 Character ROMs
- DM74166 Dot Shift Register
- MK1007P, 33571/2, 2532 80-Bit Shift Registers (Line Buffers)

Dot Rate Clock: This output is buffered for use in system synchronization and interface to dot shift register. Positive edge clock at crystal oscillator frequency.

Load Video Shift Register: Buffered output at character rate frequency. Used for direct interface to dot shift register. This output is active only during video time and therefore performs both the horizontal and vertical blanking functions. Low level active.

Latch Character Generator Address: Buffered output at character rate frequency. Active at all times. Positive edge clock.

Line Buffer Clock: This output directly interfaces to line buffers. Output operates at character rate. Negative edge clock. Not active during horizontal blanking. The number of clocks per scan line is equivalent to the number of video characters per row.

Line Rate Clock: Line rate frequency output for use with DM8678-type character generator.

Line Counter Outputs (LC_0 to LC_3): Buffered outputs at line rate frequency for use with character ROMs without internal line counter. These outputs are also useful for system decode of present line position in character row. Outputs clock in sync with Line Rate Clock at start of horizontal blanking. Outputs are always active.

Clear Line Counter: Row rate clock – occurs in sync with Line Rate Clock during horizontal blanking between last line of any row and first line of a new row. This output is always active and is a negative edge clock – direct interface to the DM8678.

Line Buffer Recirculate Enable: This output interfaces to a line buffer and becomes inactive (logic "0" state) during the last line or the first line of a character row, depending on the state of the character generator program input. A low level on this output indicates (in line buffer applications) the time during which the line buffer is loaded with the next row of character codes.

Table 1. Character Generator Program Truth Table

Character Generator Program Input	Recirculate Enable Output Low Level and New Row Address at Address Outputs
"0"	Last line of character row
"1"	First line of character row

The pulse appears at the start of horizontal blanking prior to when the memory address bus must be transferred to the CRTC, then returns to the high state at the next horizontal blanking interval.

MEMORY ADDRESS OUTPUTS/INPUTS AND REGISTERS

CRT Character Address Outputs (TRI-STATE) – A_0 to A_{11}: 12 bits of bidirectional CRT character address counter outputs are provided by the CRTC. These outputs directly interface to the system RAM memory address bus.

Within a scan line the counter is pre-set to the address contained within the Row Start Register (RSR) three character times before the start of video time. The counter is then advanced sequentially at character rate to the max video character address plus 1 for the present scan line. This address is then held during the horizontal blanking interval up to three character times before video start for the next scan line. At this point the counter is again pre-set to the contents of the RSR and the above sequence is repeated. This sequence provides scan line address repetition for every scan line of a character location within a row. Row-to-row start address modifications are accomplished by updating the contents of the RSR.

During vertical blanking the address counter operation is modified by stopping the pre-set load of the contents of the RSR into the address counter, thereby allowing the address outputs to free run during vertical blanking. This allows minimum access time to the CRTC when the CRTC address counter outputs are being used for dynamic RAM refresh.

RAM Address Enable Input: At all times the status of the address counter outputs is controlled externally by the Enable Input. Logic "0" = TRI-STATE, Logic "1" = Active.

Internal Top-of-Page, Row Start, and Cursor Registers: Control pins are provided for loading the top-of-page, row start, and cursor address into three 12-bit CRTC registers from the bidirectional memory address pins.

The Top-of-Page Register (TOPR) holds the address of the first character of the first video row. This register allows display scroll with the CRTC without the use of external memory address adders. If the TOPR is not loaded after a system clear its contents will be zero and the address outputs will be sequential from zero at the top-of-page.

The Cursor Register (CR) holds the present address of the cursor and is cleared to zero after a system clear. Once the TOPR and CR registers have been loaded they need not be accessed again until modification of their contents is required. These registers may be loaded at any time, but to cause minimum display distortion it is recommended that they be loaded only during blanking intervals.

The Row Start Register (RSR) is the working register for the CRTC address counter. It determines the first video character address on a scan line to scan line basis.

Modification of this register after the start of video in a scan line will modify the address counter outputs at the start of video on the next scan line. (See address output description.) If the RSR is never externally loaded, the CRTC address outputs will be sequential on a row-to-row basis from the TOPR contents at the start of the video page. With external loading, row-to-row non-sequential operation of the CRTC address outputs is possible, thus row-to-row edit capability. When used in this mode the RSR should be loaded after the start of video time of the last scan line of the previous row. A load to the RSR during vertical blanking will also load the TOPR.

Table 2. Register Load Truth Table

Register Select A	Register Select B	Register Load Input	Register Access
0	0	0	No Select
0	1	0	Top-of-Page
1	0	0	Row Start*
1	1	0	Cursor
X	X	1	No Select

*During vertical blanking a load to this register will also load the top-of-page register.

VIDEO RELATED OUTPUTS

Horizontal Sync: This output provides the necessary line (scan) rate sync to either three-terminal or composite sync monitors. The pulse is programmable in position and width at character time increments. This output may also be programmed to have RS-170 compatible serration pulses during the vertical sync interval. The active logic state of this output is also programmable.

Vertical Sync: This output provides the necessary frame rate sync consistent with either three-terminal or composite type monitors. The pulse is programmable in position and width at line (scan) time increments. The active logic state of this output is also programmable.

Cursor Enable: When a match with the CRTC cursor address register and address counter occurs a pulse will appear at this output at that video character time (character field width) for every line in that row. This output may also be programmed to appear on only one line of a character row. With the character generator program pin in a logic "0" position the cursor enable output will not be valid on the last line of a character row for that row. Like the Load Video Shift Register Output, this output is not active during horizontal or vertical blanking. High level active output.

CRT SYSTEM CONTROL FUNCTIONS

50/60 Hz Control Input: This input controls the CRT system refresh rate. The CRTC may also be programmed for refresh rates other than 50 and 60 Hz.

50/60 Hz Control	Refresh Rate
1	60 Hz (f_1)
0	50 Hz (f_0)

Vertical Blanking Output: This output becomes active (logic "1") at the start of vertical blanking and may be programmed to stop at the end of any line of the character row before the start of the first video row. This output is useful for flag applications to other elements in the CRT system. Its active level is also programmable.

System Clear Input: This input when low sets and holds the CRTC at the start of vertical blanking for system sync and test. It also clears to zero the cursor and top-of-page registers. The input has hysteresis and may be connected to a resistor to V_{CC} and a capacitor to ground to provide power-up system clear.

Character Generator Program Input: This input modifies both the position of the recirculate enable output low level and the time at which the address outputs change to a new row address. It is intended to provide optimum use of the CRTC with character generator/ROMs programmed with or without active video on the first or last line of a character row. (See Recirculate Enable for truth table.)

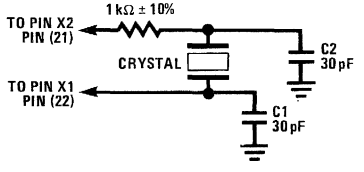
External Character/Line Rate Clock: This input is intended to aid testing of the CRTC and is not meant to be used as an active input in a CRT system. When this input is left open it is guaranteed not to interfere with normal operation.

Crystal Inputs X1 and X2: The oscillator is controlled by an external, parallel resonant crystal connected between the X1 and X2 pins. Normally, a fundamental mode crystal is used to determine the operating frequency of the oscillator; however, overtone mode crystals may be used.

Crystal Specifications (parallel resonant):

Type . . . . . AT-Cut Crystal
Tolerance . . . . . 0.005% at 25°C
Stability . . . . . 0.01% from 0°C to +70°C
Resonance . . . . . Fundamental (parallel)
Maximum Series Resistance . . . . . Dependent on frequency (for 10.92 MHz, 50 Ω)
Load Capacitance . . . . . 20 pF

Connection Diagram



If the DP8350 series is clocked at dot rate by a system clock, pin 22 (X1 input) should be clocked directly using a Schottky series circuit. Pin 21 (X2 input) may be left open.

6

Timing Waveforms

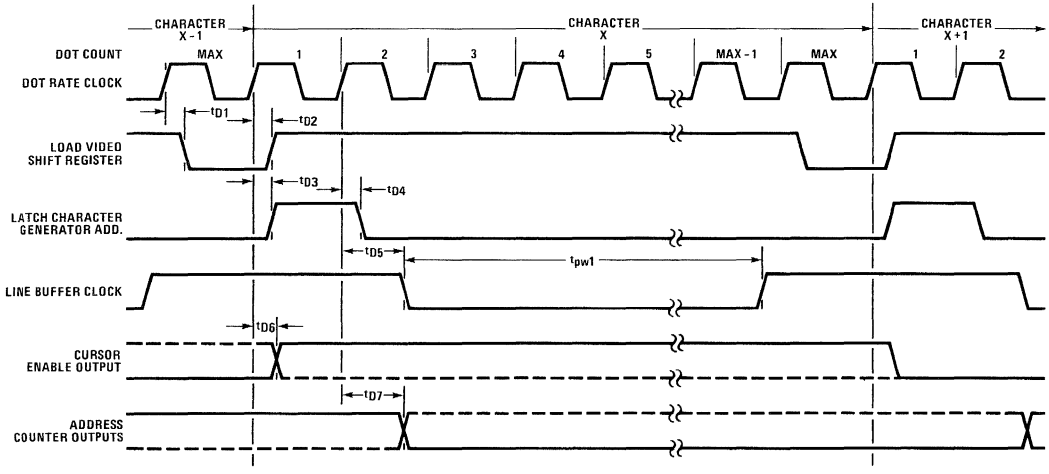
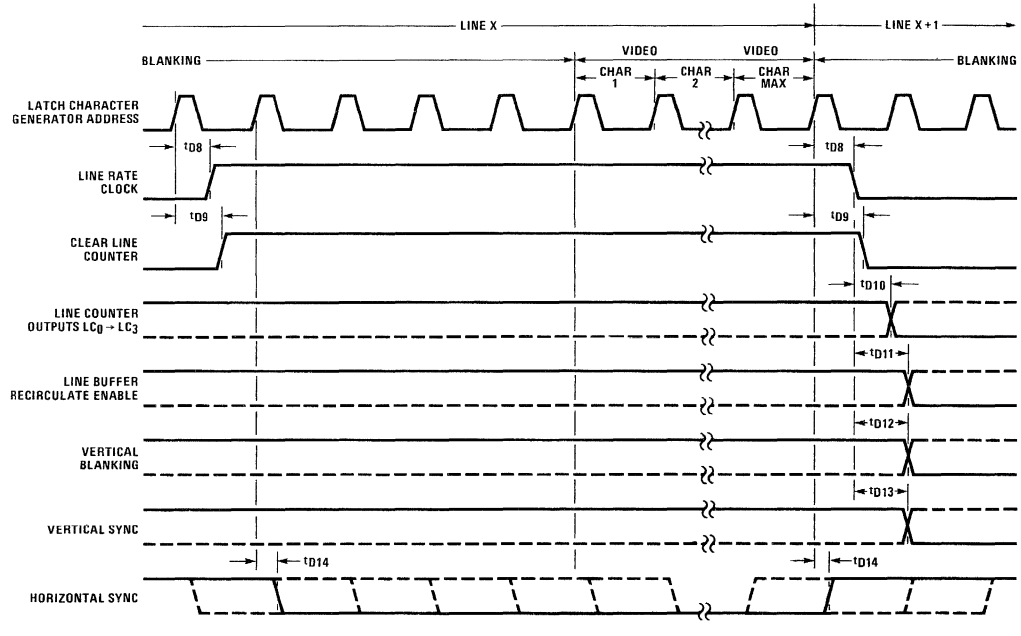


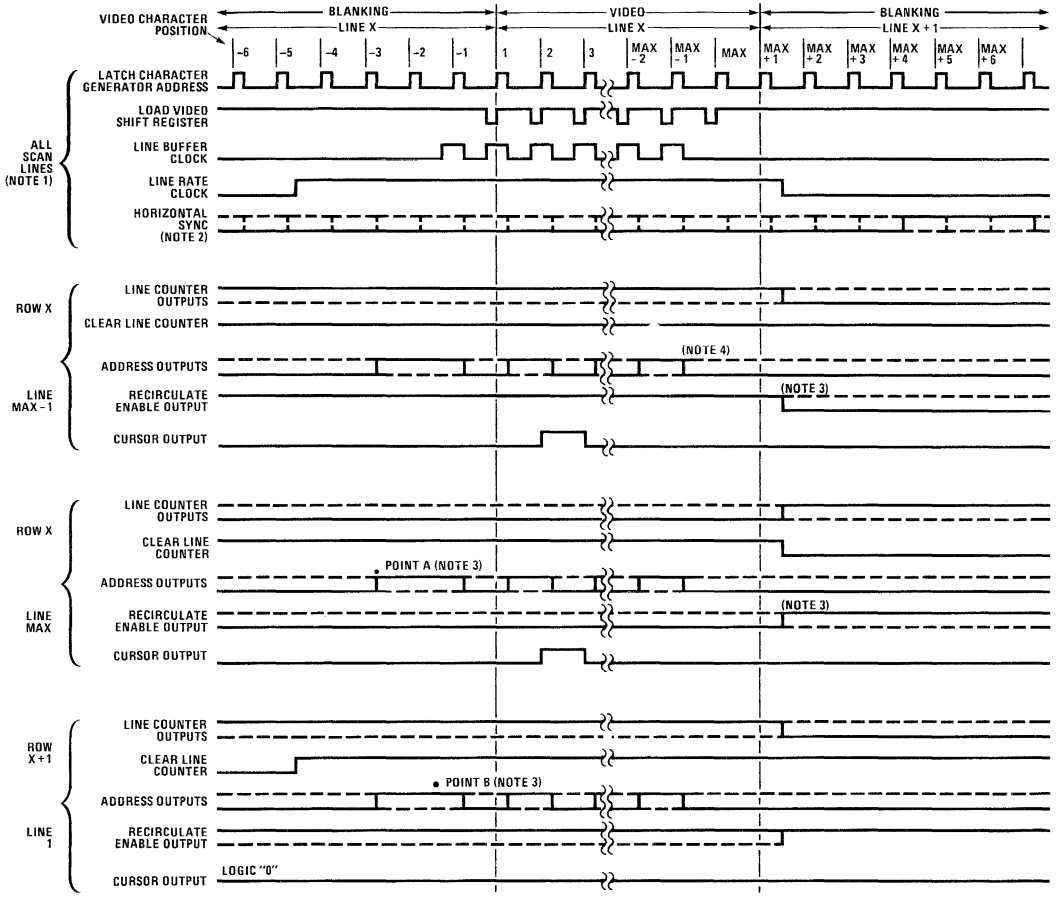
Figure 1. Dot/Character Rate Timing



*THE POSITION OF THE START AND STOP POINTS OF THE HORIZONTAL SYNC PULSE ARE PROGRAMMABLE BY CHARACTER TIME – WITHIN ONE CHARACTER TIME THE POINTS WILL HAVE THE t_{D14} TIME RELATIONSHIP.

Figure 2. Character/Line Rate Timing

Timing Waveforms (cont'd.)



Note 1: The load video shift register output is not active during vertical or horizontal blanking (remains in the logic "1" state during these intervals.

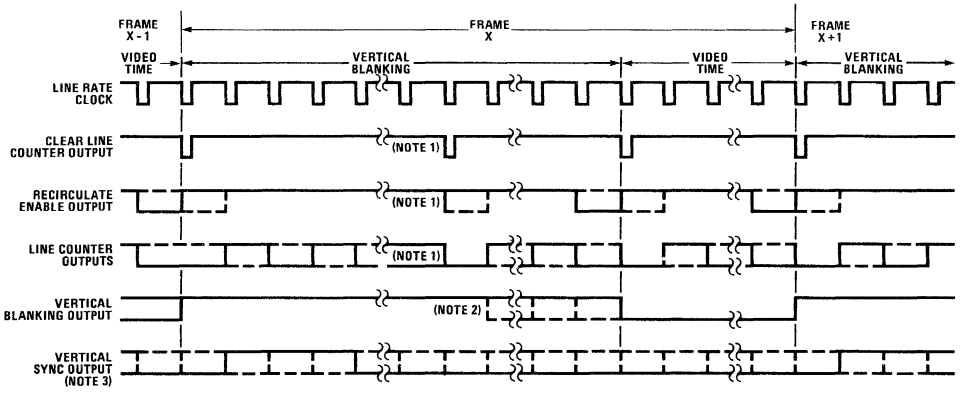
Note 2: The horizontal sync output start and stop point positions are user-programmable at character width intervals.

Note 3: The position of the recirculate enable output logic "0" level is dependent on the state of the character generator program input (CGPI). With CGPI = "0," recirculate enable occurs on the max line of a character row (solid line) and the address counter outputs roll over to the new row address at point A. With CGPI = "1," recirculate enable occurs on the first line of a character row (dashed line) and the address counter outputs roll over to the new row address at point B.

Note 4: The address counter outputs clock to the address of the last character of a video row plus 1. This address is then held during the horizontal blanking interval until video minus three character times. At this point the outputs are modified to the contents of the Row Start Register (RSR). With no external loading of the RSR the contents will be either the character address of the first character in the present row or the character address of the first character of the next video row (depending on the state of the Character Generator Program input) which will be sequential from the last character address of the last row. If the RSR was loaded, then the address outputs will be modified to the contents of the register.

Figure 3. Character/Line Rate Functional Diagram

Timing Waveforms (cont'd.)

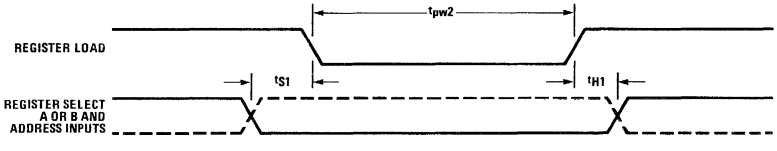


Note 1: One full row before start of video the line counter is set to zero state – this provides line counter synchronization in cases where the number of lines in vertical blanking are not even multiples of the number of lines per row.

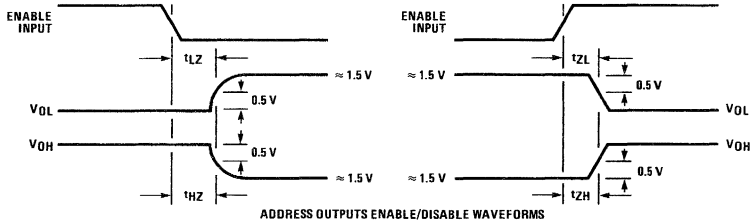
Note 2: The stop point of vertical blanking is programmable at line intervals within the last character row before start of video.

Note 3: The Vertical Sync Output start and stop points are programmable at line rate increments.

Figure 4. Line/Frame Rate Functional Diagram

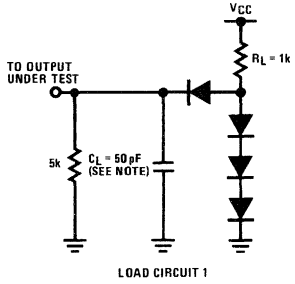


REGISTER LOAD WAVEFORMS

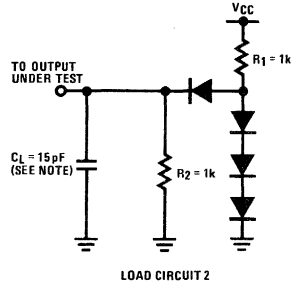


ADDRESS OUTPUTS ENABLE/DISABLE WAVEFORMS

Test Load Circuits



LOAD CIRCUIT 1



LOAD CIRCUIT 2

NOTE: C_L INCLUDES PROBE AND JIG CAPACITANCE
ALL DIODES ARE 1N914 OR EQUIVALENT.

Absolute Maximum Ratings (Note 1)

Supply Voltage, V_{CC}	7.0 V
Input Voltage	−1 V to +5.5 V
Output Voltage	5.5 V
Storage Temperature Range	−65°C to +150°C
Lead Temperature (soldering, 10 seconds)	300°C

Operating Conditions

	Min	Max	Units
V_{CC}, Supply Voltage	4.75	5.25	V
T_A, Ambient Temperature	0	+70	°C

Electrical Characteristics V_{CC} = 5 V ± 5%, T_A = 0°C to +70°C (Notes 2 and 3)

Parameter		Conditions	Min	Typ	Max	Units
V_{IH}	Logic "1" Input Voltage					
	(System Clear)		2.6			V
	(All Other Inputs Except X1, X2)		2.0			V
V_{IL}	Logic "0" Input Voltage					
	(System Clear)				0.8	V
	(All Other Inputs Except X1, X2)				0.8	V
$V_{IH}-V_{IL}$	System Clear Input Hysteresis			0.4		V
V_{clamp}	Input Clamp Voltage (All Inputs Except X1, X2, & Char/Line Rate Clock)	I_{IN} = −12 mA		−0.8		V
I_{IH}	Logic "1" Input Current					
	(Address Outputs)	Enable Input = 0 V, V_{CC} = 5.25 V, V_R = 5.25 V		10		μA
	(All Other Inputs Except X1, X2)	V_{CC} = 5.25 V, V_R = 5.25 V		2		μA
I_{IL}	Input Current					
	(Address Outputs)	Enable Input = 0 V, V_{CC} = 5.25 V, V_{IN} = 0.5 V		−20		μA
	(All Other Inputs Except X1, X2)	V_{CC} = 5.25 V, V_{IN} = 0.5 V		−20		μA
V_{OH}	Logic "1" Output Voltage	I_{OH} = −100 μA	3.2	4.1		V
		I_{OH} = −1 mA	2.5	3.3		V
V_{OL}	Logic "0" Output Voltage	I_{OL} = 5 mA		0.35	0.5	V
I_{OS}	Output Short Circuit Current	V_{CC} = 5 V, V_{OUT} = 0 V, (Note 4)		−40		mA
I_{CC}	Power Supply Current	V_{CC} = 5.25 V		170		mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified, min/max limits apply across the 0°C to +70°C temperature range and the 4.75 V to 5.25 V power supply range. All typical values are for T_A = 25°C and V_{CC} = 5.0 V.

Note 3: All currents into device pins are shown as positive; all currents out of device pins are shown as negative; all voltages are referenced to ground, unless otherwise specified. All values shown as max or min are so classified on absolute value basis.

Note 4: Only one output at a time should be shorted.

Switching Characteristics V_{CC} = 5.0 V, T_A = 25°C (Notes 1 and 2)

	Parameter	Conditions	Min	Typ	Max	Unit
t_{D1}	Dot Clock to Load Video Shift Register Negative Edge	C_L = 50 pF, R_L = 1 kΩ, Load Circuit 1		5		ns
t_{D2}	Dot Clock to Load Video Shift Register Positive Edge	C_L = 50 pF, R_L = 1 kΩ, Load Circuit 1		11		ns
t_{D3}	Dot Clock to Latch Character Generator Positive Edge	C_L = 50 pF, R_L = 1 kΩ, Load Circuit 1		11		ns
t_{D4}	Dot Clock to Latch Character Generator Negative Edge	C_L = 50 pF, R_L = 1 kΩ, Load Circuit 1		4		ns
t_{D5}	Dot Clock to Line Buffer Clock Negative Edge	C_L = 50 pF, R_L = 1 kΩ, Load Circuit 1		20		ns
t_{PW1}	Line Buffer Clock Pulse Width	C_L = 50 pF, R_L = 1 kΩ, Load Circuit 1		N(DT)*		ns
t_{D6}	Dot Clock to Cursor Enable Output Transition	C_L = 50 pF, R_L = 1 kΩ, Load Circuit 1		25		ns
t_{D7}	Dot Clock to Valid Address Output	C_L = 50 pF, R_L = 1 kΩ, Load Circuit 1		20		ns
t_{D8}	Latch Character Generator to Line Rate Clock Transition	C_L = 50 pF, R_L = 1 kΩ, Load Circuit 1		300+2DT		ns
t_{D9}	Latch Character Generator to Clear Line Counter Transition	C_L = 50 pF, R_L = 1 kΩ, Load Circuit 1		400+2DT		ns
t_{D10}	Line Rate Clock to Line Counter Output Transition	C_L = 50 pF, R_L = 1 kΩ, Load Circuit 1		180		ns
t_{D11}	Line Rate Clock to Line Buffer Recirculate Enable Transition	C_L = 50 pF, R_L = 1 kΩ, Load Circuit 1		200		ns
t_{D12}	Line Rate Clock to Vertical Blanking Transition	C_L = 50 pF, R_L = 1 kΩ, Load Circuit 1		200		ns
t_{D13}	Line Rate Clock to Vertical Sync Transition	C_L = 50 pF, R_L = 1 kΩ, Load Circuit 1		200		ns
t_{D14}	Latch Character Generator to Horizontal Sync Transition	C_L = 50 pF, R_L = 1 kΩ, Load Circuit 1		100		ns
t_{SI}	Register Select/Memory Address Setup Time Prior to Register Load Negative Edge			100		ns
t_{HI}	Register Select Memory Hold Time After Register Load Positive Edge			0		ns
t_{PW2}	Register Load Pulse Width			150		ns
f_{MAXdot}	Maximum Dot Rate Frequency			25		MHz
$f_{MAXchar}$	Maximum Character Rate Frequency			2.5		MHz
t_{LZ}, t_{HZ}	Delay from Enable Input to High Impedance State from Logic "0" and Logic "1"	C_L = 15 pF, Load Circuit 2		25		ns
t_{ZL}, t_{ZH}	Delay from Enable Input to Logic "0" and Logic "1" from High Impedance State	C_L = 15 pF, Load Circuit 2		25		ns

Note 1: Unless otherwise specified, all AC measurements are referenced to the 1.5 V level of the input to 1.5 V of the output.

Note 2: When external clock inputs are used, the input characteristics are Z_{OUT} = 50 Ω and $t_R \leq 10$ ns, $t_F \leq 10$ ns.

*"DT" is defined as the duration (in ns) of one full cycle of the Dot Rate Clock (Item 20 of the ROM Program Table). "N" denotes the number of DTs per definition in Item 24 of the ROM Program Table.

DP8350 Series Option Program Table (Notes 1, 2, and 3)

Item No.	Parameter		Value	
1	Character (Font Size)	Dots per Character		
2		Scan Lines per Character		
3	Character Field (Block Size)	Dots per Character		
4		Scan Lines per Character		
5	Number of Video Characters per Row			
6	Number of Video Character Rows per Frame			
7	Number of Video Scan Lines (Item 4 x Item 6)			
8	Frame Refresh Rate (Hz) (two frequencies allowed)		f1 =	f0 =
9	Delay after/before Vertical Blank start to start of Vertical Sync (+/– Number of Scan Lines)			
10	Vertical Sync Width (Number of Scan Lines)			
11	Delay after Vertical Blank start to start of Video (Number of Scan Lines)			
12	Total Scan Lines per Frame (Item 7 + Item 11 = Item 13 ÷ Item 8)			
13	Horizontal Scan Frequency (Line Rate) (kHz) Item 8 x Item 12)			
14	Number of Character Times per Scan Line			
15	Character Clock Rate (MHz) Item 13 x Item 14)			
16	Character Time (ns) (1 ÷ Item 15)			
17	Delay after/before Horizontal Blank start to Horizontal Sync Start (+/– Character Times)			
18	Horizontal Sync Width (Character Times)			
19	Dot Frequency (MHz) (Item 3 x Item 15)			
20	Dot Time (ns) (1 ÷ Item 19)			
21	Vertical Blanking Stop before start of Video (Number of Scan Lines) (Range = Item 4 – 1 line to 0 lines)			
22	Cursor Enable on all Scan Lines of a Row? (Yes or No) If not, which Line?			
23	Does the Horizontal Sync Pulse have Serrations during Vertical Sync? (Yes or No)			
24	Width of Line Buffer Clock logic "0" state within a Character Time (Number of Dot Time increments)			
25	Serration Pulse Width, if used (Character Times)			
26	Horizontal Sync Pulse Active state logic level (1 or 0)			
27	Vertical Sync Pulse Active state logic level (1 or 0)			
28	Vertical Blanking Pulse Active state logic level (1 or 0)			

Note 1: If the Cursor Enable, Item 22, is active on only one line of a character row, then Item 21 must be either "1" or "0" unless it is the same as the line selected for Cursor Enable.

Note 2: Item 24 x Item 20 should be > 250 ns.

Note 3: Item 11 must be greater than Item 4 + 1.

DP8350 Series Option Program Table

DP8350 Option: 80 Characters x 24 Rows, 5 x 7 Character Font, 7 x 10 Character Field

Item No.	Parameter		Value	
1	Character (Font Size)	Dots per Character	5	
2		Scan Lines per Character	7	
3	Character Field (Block Size)	Dots per Character	7	
4		Scan Lines per Character	10	
5	Number of Video Characters per Row		80	
6	Number of Video Character Rows per Frame		24	
7	Number of Video Scan Lines (Item 4 x Item 6)		240	
8	Frame Refresh Rate (Hz) (two frequencies allowed)		f1 = 60 Hz	f0 = 50 Hz
9	Delay after/before Vertical Blank start to start of Vertical Sync (+/– Number of Scan Lines)		4	30
10	Vertical Sync Width (Number of Scan Lines)		10	10
11	Delay after Vertical Blank start to start of Video (Number of Scan Lines)		20	72
12	Total Scan Lines per Frame (Item 7 + Item 11 = Item 13 ÷ Item 8)		260	312
13	Horizontal Scan Frequency (Line Rate) (kHz) Item 8 x Item 12)		15.6 kHz	
14	Number of Character Times per Scan Line		100	
15	Character Clock Rate (MHz) Item 13 x Item 14)		1.56 MHz	
16	Character Time (ns) (1 ÷ Item 15)		641 ns	
17	Delay after/before Horizontal Blank start to Horizontal Sync Start (+/– Character Times)		0	
18	Horizontal Sync Width (Character Times)		43	
19	Dot Frequency (MHz) (Item 3 x Item 15)		10.920 MHz	
20	Dot Time (ns) (1 ÷ Item 19)		91.6 ns	
21	Vertical Blanking Stop before start of Video (Number of Scan Lines) (Range = Item 4 – 1 line to 0 lines)		1	
22	Cursor Enable on all Scan Lines of a Row? (Yes or No) If not, which Line?		Yes	
23	Does the Horizontal Sync Pulse have Serrations during Vertical Sync? (Yes or No)		No	
24	Width of Line Buffer Clock logic "0" state within a Character Time (Number of Dot Time increments)		4	
25	Serration Pulse Width, if used (Character Times)		–	
26	Horizontal Sync Pulse Active state logic level (1 or 0)		1	
27	Vertical Sync Pulse Active state logic level (1 or 0)		0	
28	Vertical Blanking Pulse Active state logic level (1 or 0)		1	

FULL/HALF ROW CONTROL (PIN 5)

Device pin 5 converts the DP8350 programmed display from 80 characters by 24 rows to 80 characters by 12 rows.

Full/Half Row (Pin 5) Logic State	Display Size
1	80 by 24
0	80 by 12

With pin 5 in logic "0" state, the 12 character rows are equally spaced vertically on the CRT. Each row is spaced by one full row of blanked video.

Also in this mode the address counter outputs address the same memory space for two rows — the video row and the blanked row. Thus one half of the CRT memory space is addressed with pin 5 in logic "0" state as compared to pin 5 in logic "1" state.

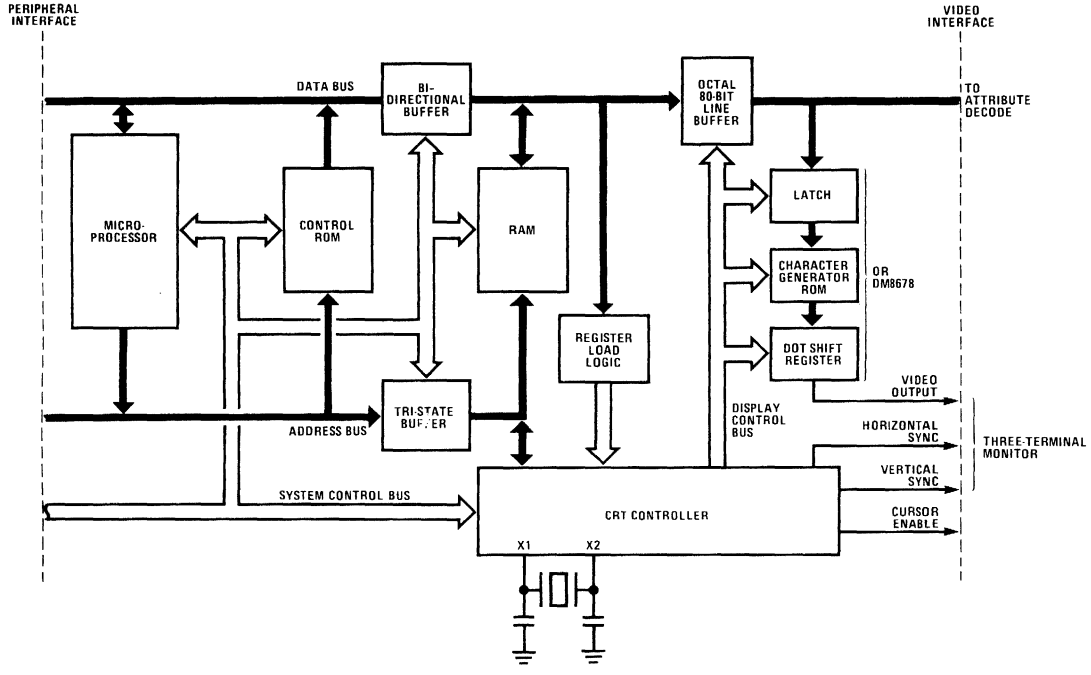


Figure 6. System Diagram Using a Line Buffer

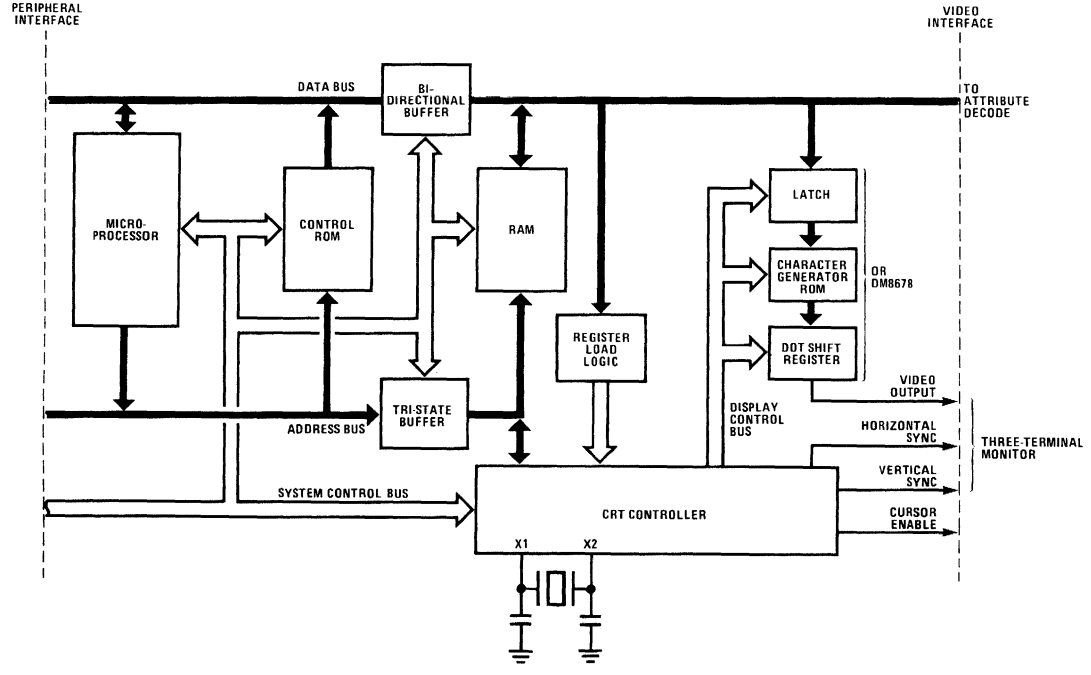


Figure 7. System Diagram with no Line Buffer

Note 1: If the Cursor Enable, Item 22, is active on only one line of a character row, then Item 21 must be either "1" or "0" unless it is the same as the line selected for Cursor Enable.

Note 2: Item 24 x Item 20 should be > 250 ns.

Note 3: Item 11 must be greater than Item 4 + 1.

DM8678 Bipolar Character Generator

The DM8678 is a 64 character bipolar character generator with serial output, and packaged in a standard 16-pin DIP designed primarily for the CRT display marketplace. The DM8678 incorporates several CRT system level functions, as well as a 7 x 9 row scan character font. The DM8678 performs the system functions of parallel to serial shifting, character address latching, character spacing, and character line spacing which are normally done with extra packages. *Figure 1* is a block diagram of the DM8678.

Address Latch

The address latches are "Fall Through" or "Feed Through" latches. The address latches are illustrated in *Figure 2*. When the address latch control signal is high, the character addresses "Fall Through" the latch. And when the address latch control signal goes low, the character addresses are latched. A 40 ns address set-up time is required.

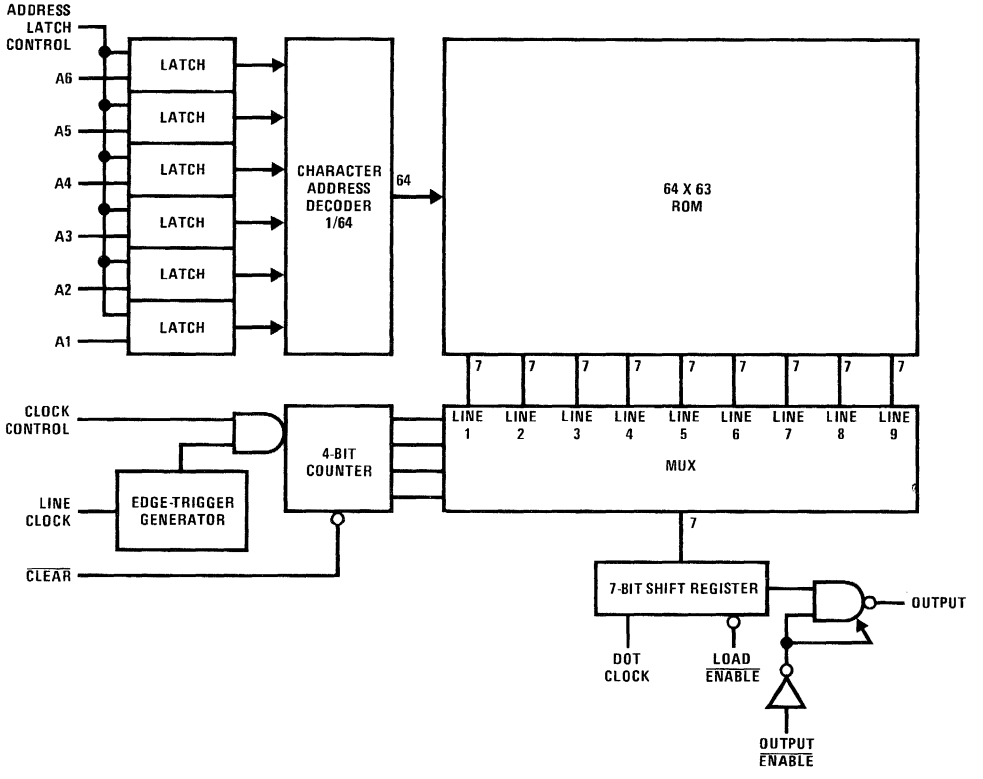
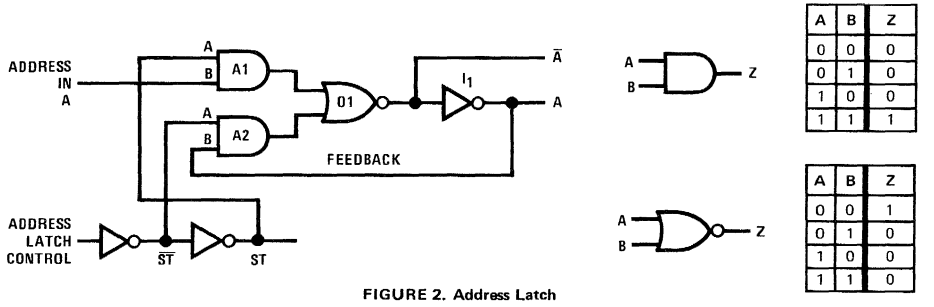


FIGURE 1. Block Diagram



A	B	Z
0	0	0
0	1	0
1	0	0
1	1	1

A	B	Z
0	0	1
0	1	0
1	0	0
1	1	0

FIGURE 2. Address Latch

Logic operation is as follows: When the address latch control signal is high, "AND" Gate A1 is enabled and "AND" gate A2 is disabled. In this mode, data "falls through" the latch. When the address latches control signal goes low, Gate A1 is disabled, blocking any new address inputs. Gate A2 is enabled by a high on input "A" which allows the feedback to determine the output of gate A2. If the feedback is low, the output of A2 will be low. If the feedback is high, the output of gate A2 will be high. Note that there are two inversions from the output of gate A2 (O1 and I_1) to the feedback loop. Thus the feedback maintains the level that was present on inverter I_1 when the address latch control goes low.

ROM

The ROM is 64 x 7 x 9 = 4032 bits. The ROM comes with a standard upper case character set. And, it is possible to have custom fonts. A coding sheet is included with the data sheet. Obviously it is possible to make smaller characters by not using all of the ROM. For example, a 5 x 7 character set could be made. Also, it is possible to use two chips to obtain a larger character set.

Line Counter

The line counter consists of a 4-bit ripple counter with an asynchronous $\overline{\text{clear}}$ input. The input clock is shaped by an edge-triggered clock generator. The clock generator's output clock pulse is enabled by the clock control signal. The output pulse from the clock generator goes to one input of a two input "AND" gate and the clock control signal goes to the other input of the "AND" gate. When the clock control signal is low the clock pulse is blocked by the "AND" gate. The line counter is illustrated in *Figure 3*.

The line counter is a mod 16 counter and its count can be shortened by $\overline{\text{clear}}$, which resets the counter to its first state, when it goes to low state.

7-Bit Shift Register

A 7-bit parallel-in serial-out shift register is used to serialize the output data. Seven "D" flip-flops and seven 2-line-to-1-line multiplexers are used to perform the parallel to serial conversion. *(Figure 4)*

Operation of the parallel to serial converter is as follows: the cycle begins with load $\overline{\text{enable}}$ going low. This routes data from the ROM via the MUX to the "D" inputs of the 7 flip-flops. The data at the "D" inputs is clocked into the flip-flops on the next low-to-high transition of the dot clock. Next, the load $\overline{\text{enable}}$, goes high switching the mux. Now data at the "D" input comes from the "Q" output of the preceding flip-flop stage.

The first stage in the shift register is an exception and the mux routes a low to its "D" input, with the first stages "D" input low. After 7 clocks, all stages are low and any additional clocks will produce a low output. This feature is used for horizontal spacing between characters.

Output Buffer

The output buffer is a standard TTL TRI-STATE® output circuit. The output enable is the TRI-STATE control and when the $\overline{\text{enable}}$ is high, the output is in the Hi-Z state. The output can sink 16 mA at 0.45V for a low signal out, and, will source 2 mA at 2.4V for a high signal out.

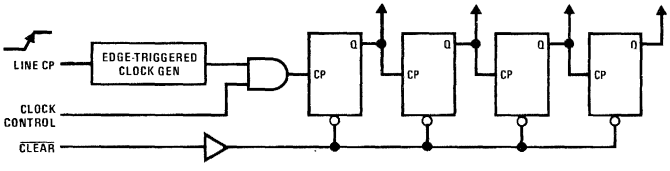


FIGURE 3. Line Counter

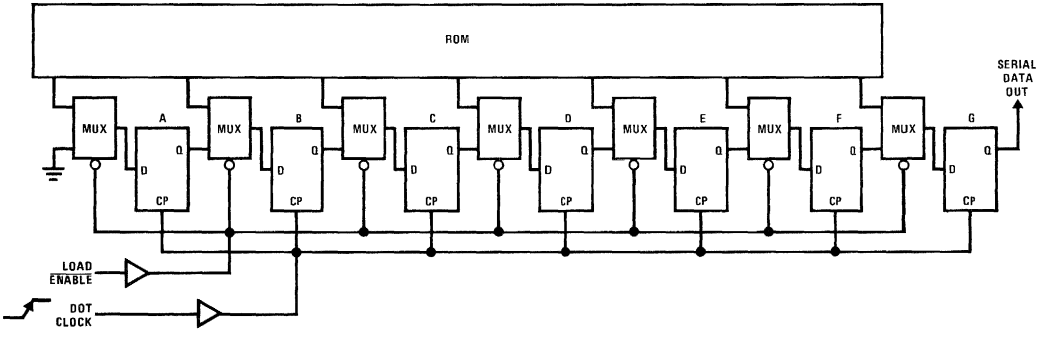


FIGURE 4. 7-Bit Parallel-In Serial-Out Shift Register with Synchronous Load

OPERATION OF THE DM8678 CHARACTER GENERATOR

To illustrate operation of the DM8678, an example is given tracing the sequence of events involved in generating a character. The character "N" is used in this example. *(Figures 1 and 5)*.

Generation of the character "N" begins with the appropriate 6-bit character address becoming valid on the address inputs A1 to A6. This address can be latched by bringing the address latch control signal low. There are address set-up and hold times of 50 ns and 40 ns respectively.

The output of the address latch is decoded in the character address decoder. This is a 1/64 active high decoder. The word line which contains the code would go high.

The ROM contains the code required for generating the 64 7 x 9 characters. The ROM is organized 64 words each, 63 bits long (7 x 9 = 63). In the ROM, the first 7 bits of 63 are line 1 of the character, the next 7 bits store line 2 of the character and so on. Note that 1 bit = 1 dot. The lines and dots for our example "N" are illustrated in *Figure 5*. The code for "N" would be:

1000001	1000001	1100001	-----
Line 1	Line 2	Line 3	
1000011	1000001	1000001	
Line 7	Line 8	Line 9	

After the access time has elapsed (tasl = 350 ns), the output of the ROM for Line 1 of the character (N for this example) can be loaded into the shift register. When load enable is brought low, the shift register is loaded on the next low-to-high transition of the dot clock with Line 1 of the character "N." The next 6 dot clocks will shift out the rest of the first line of character "N." If only a single character in a row was generated, the line clock would go from low-to-high advancing the line counter which in turn switches the multiplexer to Line 2 of the character. Line 2 contains the next 7 bits required for generating "N." This would continue until the 9th line has been clocked out. Any additional line clocks will put a vertical space between characters. This is illustrated in *Figure 5*.

In a typical application, more than one character is displayed in a row. *(Figure 6)* The sequence is as follows: Line 1 of the first character is clocked out. Note that 7 dot clocks are required to shift out one line in a character. Additional dot clocks will add lows to the end of the line. This provides a horizontal space between characters. There is no limit to the number of clocks which can be used to generate horizontal spacing. The address is changed to select the second character. Then the first line of the second character is clocked out, next, the first line of the third character is clocked out, continuing until the first line of the last character in the row has been clocked out. At this time, the line counter of the DM8678 is clocked, advancing the line counter to Line 2. The first character is addressed again, and the process of the scanning continues until the 9th line of the last character in the first row has been shifted out.

Then the line clock is again clocked, incrementing the line counter to Line 10. All characters in the row are scanned. *(Figure 6)* The output of the character generator for lines 10 to 16 is all lows. This provides a vertical space between rows. The number of lines used to space can be controlled by clear going low after the desired number of lines of vertical space have been generated.

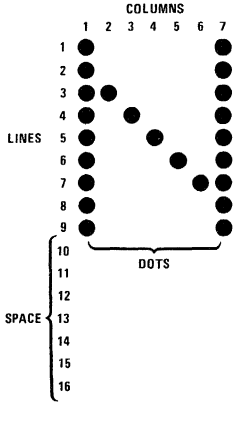


FIGURE 5. Character Example

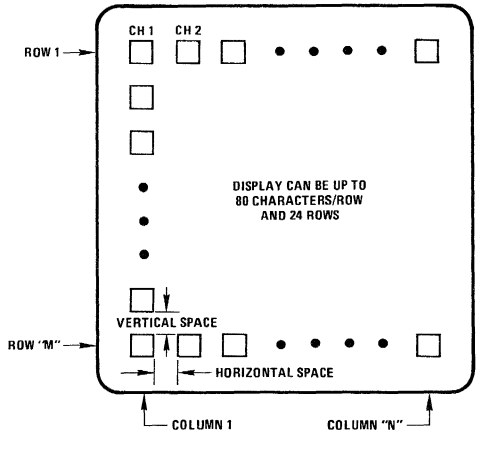


FIGURE 6. Display Example

Next, the first line of the first character of the second row is addressed and scanned. This continues until the 9th line plus lines for vertical spacing of the last character in the last row has been scanned. At this time the display field has been written. For a CRT Display, it is necessary to refresh the display. Displays are typically refreshed 30 to 60 times each second. Memory is required to store the character address so that they may be called up when required for refresh.

Figure 7 is the connection diagram and logic symbol.

DEFINITIONS

A1–A6: Character address. A 6-bit code which selects 1 of the 64 characters in the font.

$\overline{\text{Clear}}$: Active low clear for mod 16 row counter, (can be used to truncate mod 16 counter).

Line Clock: Clock that advances the line counter. Advances counter on the low-to-high transition.

Clock Control: Enables line clock when high and disables line clock when low.

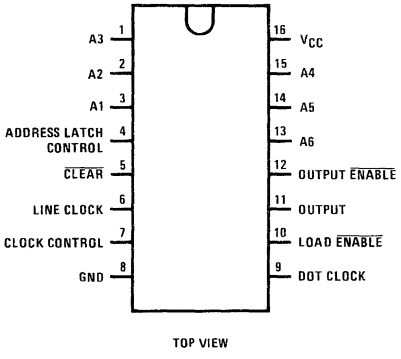
Load $\overline{\text{Enable}}$: Active low load command which routes data from the character ROM to the "D" inputs of the 7-bit shift register.

Dot Clock: A low-to-high transition of the dot clock loads the shift register if $\overline{\text{load}}$ is low or shifts data if $\overline{\text{load}}$ is high.

Output $\overline{\text{Enable}}$: An active low output enable. When high the output is in the Hi-Z state.

Output: A TTL TRI-STATE output buffer.

Dual-In-Line Package



TOP VIEW

FIGURE 7(a). Connection Diagram

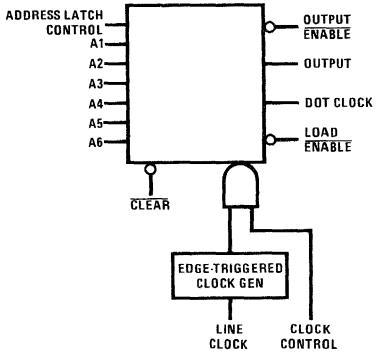


FIGURE 7(b). Logic Symbol DM8678

6

128 Characters with the DM8678

National Semiconductor
W. Johnston
C. Mitchell

The purpose of this brief is to describe the control logic necessary to generate 128 characters and attributes. The example used is for the upper and lower case set of characters from the DM8678BWF and DM8678CAE with cursor (underline) and blanking.

There are 2 important factors to consider when using 2 DM8678's. First, the character set of each ROM pattern is based on a 6-bit ASCII format. A seventh bit must be added for selection of upper or lower case. Second, the standard ASCII format requires that bits 6 and 7 be exclusive-ORed to select upper and lower case characters. Pipelining this altered most significant bit (bit 6 and bit 7) synchronizes the signal to control the OUTPUT ENABLE of the appropriate character generator. This either enables or TRI-STATES® the DM8678 outputs. *Figure 1* shows an implementation using the DM7486—exclusive-OR gate and the DM8511—gated D flip-flop.

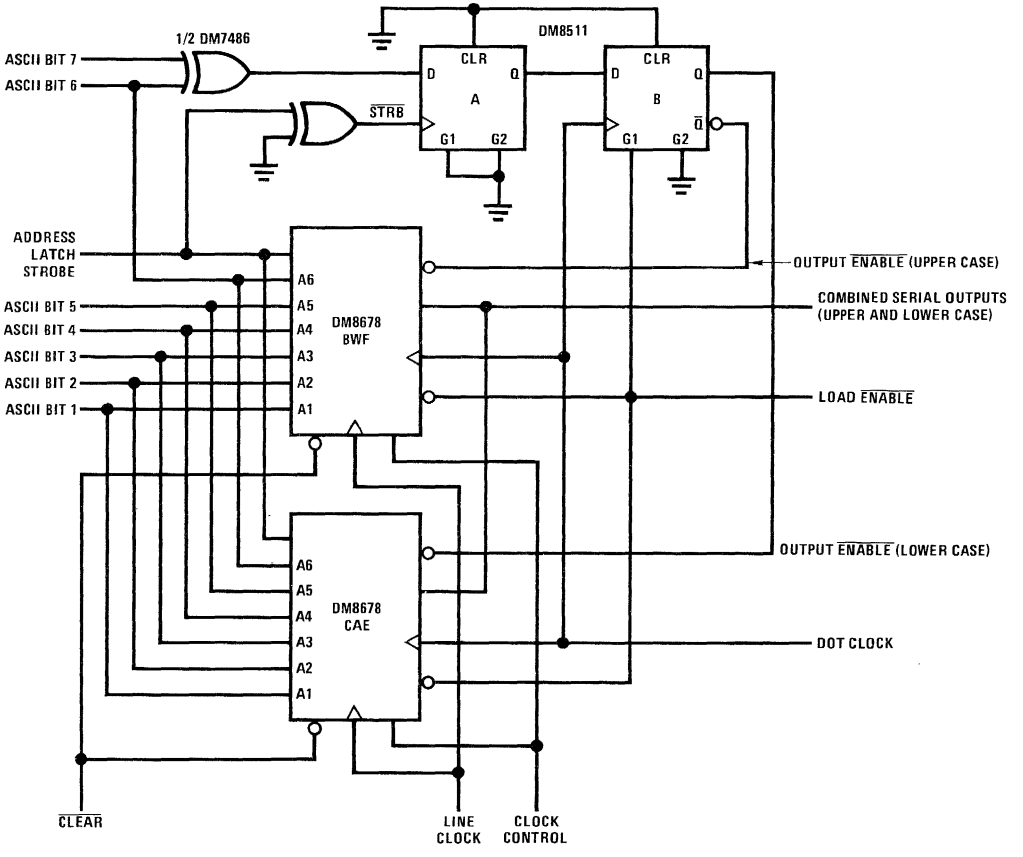


FIGURE 1. Upper and Lower Case Character Generator

The selection bit is latched into the first flip-flop on the trailing edge of the address latch strobe. If the strobe of the DM8678 is not in use (as in low character rate systems), then this first flip-flop (A) may be eliminated. The second flip-flop (B) is gated on by the same signal that drives LOAD $\overline{\text{ENABLE}}$ on the character generator. Clocking of both the DM8678's and flip-flop (B) occurs on the positive edge of the dot clock. Q and $\overline{\text{Q}}$ drive the OUTPUT $\overline{\text{ENABLE}}$ inputs of the lower and upper case generators, respectively.

Figure 2 indicates how attribute bits can be inserted into the combined serial output of *Figure 1* to produce character blanking or underlining. Here the attribute bits are pipelined using DM8511's and DM7474's.

In *Figure 2*, a cursor (which occurs on the video display as an underline) is gated on only during the eleventh scan line of a character. Apart from this gating the attributes are pipelined in the same manner as the OUTPUT $\overline{\text{ENABLE}}$'s in *Figure 1*, except that the outputs of the DM8511's are logically combined with the video.

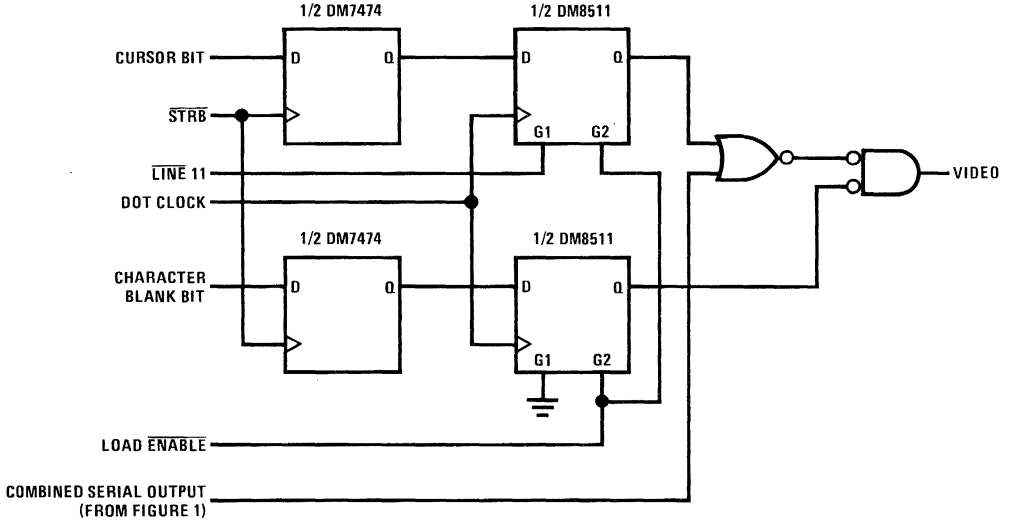


FIGURE 2. Pipelining Attribute Bits

DM8678 Character Generator Emulator

National Semiconductor
C. Mitchell

When developing new character fonts or graphic symbol sets for the DM8678 character generator, it is desirable to have a field programmable emulator. The purpose of this brief is to describe such a circuit.

Working from the DM8678 block diagram, the device can be partitioned into MSI logic components and bipolar PROMs.

A DM86S75 hex latch will serve as a functional replacement for the address input latch. Address decoding and output multiplexing are included in modern memories; therefore, the 3 blocks depicting the memory function are realized with PROM. DM74S574 1024 x 4 PROMs are used here, but any 4-bit or 8-bit wide bipolar PROM will suffice, depending on programming and partitioning preferences.*

The line count may be emulated with a DM74161 counter and DM74LS283 adder. Inclusion of the adder is required if descending characters (i.e., y, g, j, etc.) are desired.

For a 4-line descent, the B inputs of the adder should be driven to 1100 by a PROM Tag Bit (for a 2-line descent, B inputs should be 1110, etc.)**. The Tag Bit (active high) should be programmed into the PROM for each descending character. Locations addressed by line counts 1100–1111 should be programmed (except for Tag Bits) as all zeros.

The counter/adder combination provides an altered line count to the memory when the B inputs are activated. In this way, the address representing line location is shifted by an amount equal to the 2's complement of the input *(Figure 2)*. Another way to accomplish this would be to offset the PROM location of the descended character (in other words, the starting location of a y, for example, would be at line count 4 instead of 0, as in a normally placed character). However, use of an adder in conjunction with the counter provides a closer approximation to operation of the DM8678.

Note that the DM86S75 latch is inverting; therefore, address inputs as programmed into PROM should be complemented.

Alternatively, an inverter may follow the latch, or 2 DM7475 latches may replace the DM86S75.

The output stage may be implemented with a DM74166 shift register and a TRI-STATE® buffer completes the circuit *(Figure 3)*.

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*Note that the DM74S574 is pin compatible with the MM2114 1k x 4 read/write memory. Use of the MM2114 would be attractive in emulations where a more exhaustive study of symbols is desired.

**4-line descent is generally used in 7 x 9 character fonts, 2-line descent is used with 5 x 7 characters.

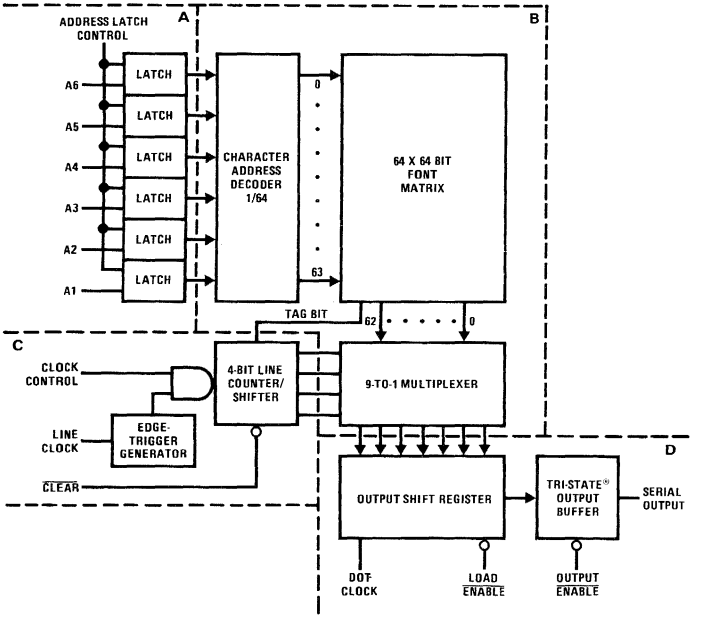
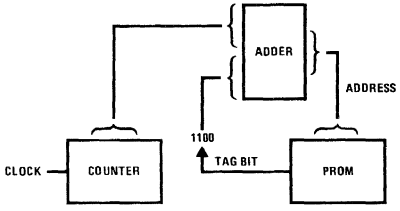


FIGURE 1. Block Diagram



TAG BIT	COUNT	ADDRESS	LINE NO.
0	n	n	n
1	0	1100	1
1	1	1101	2
1	2	1110	3
1	3	1111	4
	4	0000	5
	↓		
	9	1001	10
	↓		

FIGURE 2

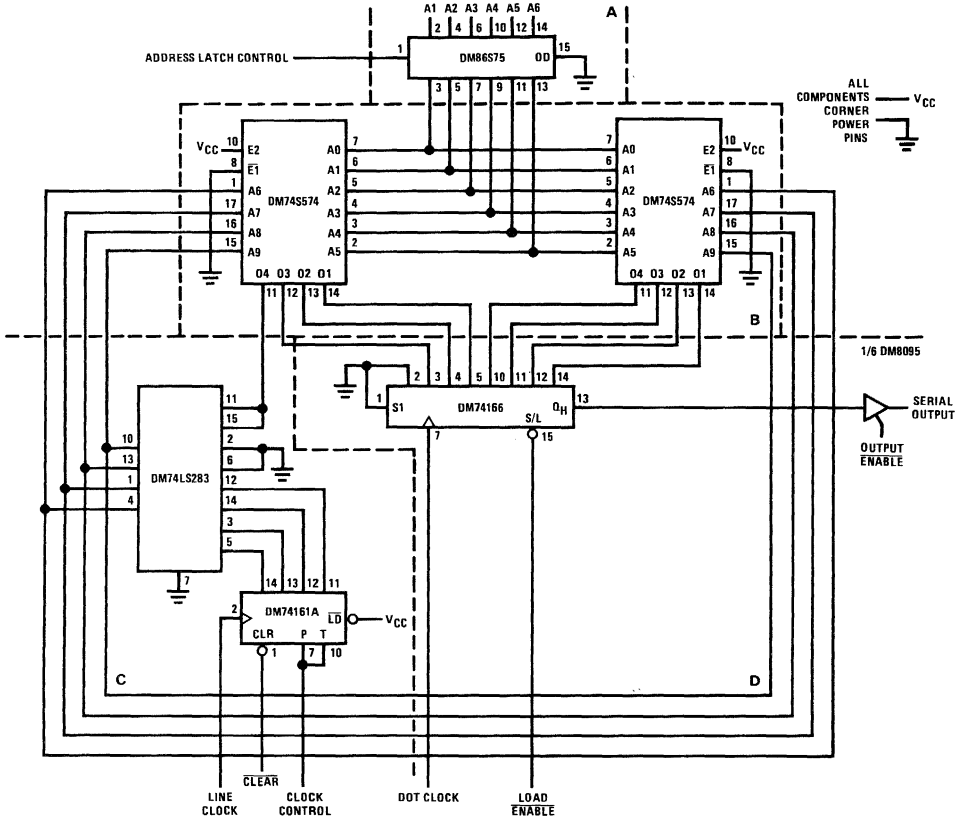


FIGURE 3

Section 7

Charge Coupled Devices

7

Recent breakthroughs in n-channel MOS technology have made possible the implementation of single chips containing 64k bits of storage, based on memory cells called charge coupled devices. Anticipated CCD yields in volume production will be much higher than more conventional dynamic RAM of the same density, because the basic CCD cell itself contains no contacts, no metal, and no diffusions. Thus, bit cost is expected to be a factor of three or more lower than that of dynamic RAM as CCD production grows in the early 1980s. As a result, much innovation is occurring in equipment designs now on the drawing boards. This section is intended to help you in the development of new architectures for your next generation systems.

The MM2464: A Practical Charge Coupled Device for Digital Memory Applications

National Semiconductor
Memory Application Note
C. B. Mitchell

PRELIMINARY*

INTRODUCTION

Charge-coupled devices (CCDs) exhibit the highest density silicon based memory capacity available. Because storage and transfer are achieved by multiphase clocking of closely packed MOS capacitors, significant amounts of circuit detail may be eliminated from a memory cell. The resulting increase in density may exceed four times that of a dynamic RAM using similar processing technology. Thus, the recent introduction of a number of very dense, sequentially accessed memory components, including the MM2464 64k-bit CCD from National Semiconductor. CCDs provide a practical answer to a need in memory technology. This need becomes apparent upon examination of current memory products with respect to access time and density. On one hand are high speed medium density devices such as semiconductor RAM and magnetic core, on the other are techniques typified by high density and low speed. These include tape and disk storage. The gap in access time runs from the one or two microsecond upper boundary of RAM and core based systems to a lower bound on disk systems of tens of milliseconds. CCDs fall within this gap providing a significant density increase over RAM and latency times of hundreds of microseconds. Therefore, the CCD provides a powerful tool in the system design engineer's effort to increase memory size and bandwidth.

What are the basic facts concerning CCDs?

- As mentioned, information is stored in the form of charge on a capacitor; therefore, the CCD must be refreshed, as in MOS dynamic RAM.
- CCDs are constructed using MOS processes very similar to those used for dynamic RAMs; therefore, power supply voltages and interface requirements are familiar.
- The CCD is a serial device; therefore, the architecture will reflect this sequential nature.
- As CCDs are a natural result of the growth of MOS technology, it is reasonable to expect products to mature in much the same way as MOS dynamic RAMs and microprocessors have grown (i.e., cost, size, speed, interfacing, etc.).

There are currently two major design philosophies in CCDs intended for digital storage which are reflected in the architecture of the devices available. These two architectures are referred to as "long loop" and "short loop." In both cases, the devices resemble a number of recirculating shift registers arranged in parallel (figure 1). Each S/R input and output is then addressed to provide a path to the package I/O pins.

The terms long loop and short loop relate to the shift register length, N. Long loops seem to have reached a de facto standard of N = 4096 bits, while for short loops N = 256 bits. Long loop CCDs are generally constructed with a buried or bulk CCD channel while short loop parts are built with surface channels. Buried channel techniques tend to result in devices with lower signal levels than those of surface channel parts, hence refresh

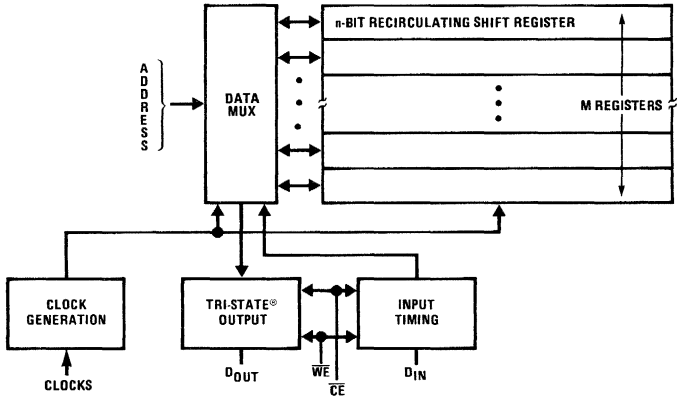


Figure 1. Block Diagram

*Due to publishing deadlines, some of the circuit diagrams contained in this note have not yet been fully tested.

requirements of long loop parts may be more demanding than those of the short loop configuration. Charge biasing (fat zero) is generally done in surface channel devices to increase noise immunity and may or may not be done in bulk devices. Surface channel CCD designs produce a less complex manufacturing sequence, as well as more efficient sense amplifier realizations.

While long loop CCDs may be clocked faster than short loop components, clock rate is not usually the most important speed parameter in a CCD. Latency time, or the amount of time it takes to get to any given word, is generally a more critical requirement. Due to the relatively few clock cycles required both the average and maximum latency times of a short loop CCD are much less than those of a long loop CCD. When applying long loop CCDs it is normal to use them in a serial mode, in other words, treating the device as 16 (in a 64k-bit part) dynamic shift registers. Another mode becomes available with a short loop CCD. A page (each position in the shift registers is known as a page) in a short loop part is 256 bits wide, a size practical for treatment as read/write memory. With this treatment comes high data rate and greatly reduced power dissipation. Because National Semiconductor is interested in bringing viable memory components with a wide range of applications to the market place, the MM2464 is configured as a 64k short loop device.

MM2464 TTL COMPATIBLE 65,536-BIT CCD

The single most significant improvement achieved by the MM2464 over existing 64k CCDs is its ease of interface. Previous CCDs have required multiple (3 or more) high level clocks and exhibited very large clock and clock-to-clock capacitance. Many system designs constrained by such high capacitance have required as many as one clock driver package for every three CCD packages. Even more devastating than the parts count requirement has been the effect of these clock drivers on system power levels. Although the CCD itself is inherently a low power device at lower clock speeds, addition of clock drivers has raised system power requirements significantly. This is not true of the MM2464, where a single DS3628 5-volt clock driver can easily service a megabyte or more of memory. Alternatively, TTL or CMOS can be used to provide clock signals. The MM2464 requires only 2 TTL level clock signals, SENSE ENABLE (SE) and SYNCHRONIZE (SYNC). SYNC occurs once for every four SE cycles. To the user it appears as if SE is clocking the 256-bit shift registers, and indeed, the device may be viewed in this manner. By examining the diagram (figure 2) below one can see this is not actually the case.

Each of the 256-bit shift registers is composed of four 63-bit CCDs and a decoding/sense amplifier/multiplexing circuit, with SYNC providing the stimulus for clocking the array. The arrangement provides a major advantage over a continuous 256-bit register while maintaining a single sense amplifier. As power dissipation in a CCD is directly dependent upon clock rate (CV^2f), higher speeds are made possible for a given power dissipation as SYNC occurs at one fourth the rate of SE. SE provides the clocking signal for the multiplexion, selecting each of the four register outputs for amplification. Upon completion of this refresh operation for the four bits in the holding register, SYNC clocks four new data bits into the register and the sequence is repeated. This one bit delay in the holding register provides the extra four bits to produce the 256-bit register ($63 \times 4 + 4 = 256$).

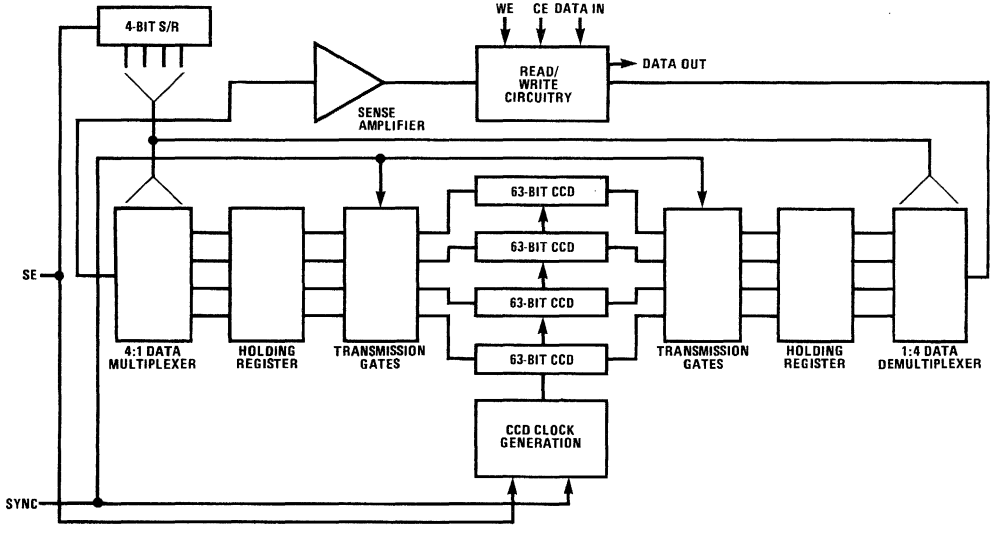


Figure 2. Block Diagram of One 256-Bit Recirculating Shift Register

257 of these registers are provided on the MM2464. The odd (or 257th) register provides a reference level for the sense amplifiers, thus the requirement for a number of clock cycles immediately following power-up to stabilize the reference voltages. This technique of providing power supply and temperature stable reference voltages reveals another advantage of the short loop configuration. Addition of a 256-bit reference loop requires only 1/256 of the device die area to accomplish. In a 4096-bit oriented device 1/16 of the die area would be necessary to construct a similar reference loop. Through comparison and feedback techniques utilizing the reference loop, noise immunity is significantly enhanced. The remaining 256 registers are available as storage.

Each register I/O in the memory array is accessible through a data steering multiplexer controlled by an eight-bit address port. A TRI-STATE® Data output and a Data input are provided which may be tied together in common bus systems provided the Write Enable (WE) signal is lowered prior to or simultaneously with Chip Enable (CE) when writing data into the part. The 256-bit page may be utilized as RAM within the restraints imposed by the timing limitations expressed in the AC electrical characteristics in the MM2464 data sheet.

A refresh cycle in the MM2464 is defined as a single passage of all data bits through the sense amplifier for regeneration. Thus, refresh takes place every 256 SE cycles. It is worthwhile to recall that refresh in a CCD is required because of charge degradation due to thermally generated "dark current" and transfer inefficiency between cells. Therefore, in systems with controlled environments, refresh, or maximum page time requirements, may be adapted to temperature conditions (for refresh, $2\,t_{REF}$ for every 10°C decrease in temperature).

SYSTEM DESIGN CONSIDERATIONS

Power Supply Considerations

Power supply voltage requirements of the MM2464 are 12V, -5V and ground. Power supply current may vary widely according to system design and clock speed. This variation is reflected in the equation below.

$$I_{DD\,AVE} = \frac{t_{CE}}{t} I_{DD1} + \frac{N}{t} I_{DD2} + \frac{t_{SSY1}}{t} I_{DD3} + I_{DD4}$$

I_{DD1} - I_{DD4} are parameters listed in the data sheet and t should be a span of time covering all modes of use of the component (i.e., t will be the period of a cyclic wave form which reflects the system operation). In most systems, the first two terms of the I_{DD} equation will be first order effects and the latter two of second order. t_{CE} is the amount of time (during t) in which the chip enable line is active; therefore, some attention should be given to generating a minimum chip enable "on time" (t_{CE}) in power critical systems. Likewise, as "N" is the number of SE cycles during t, clock frequencies should not exceed those needed for required system performance. Adaptive clocking (i.e., minimum clock rate during periods when the system is not in use) may also be attractive. Although not so critical, the third portion of the current may be minimized, as can the first, by careful control circuitry design. This term reflects the period of time between the rise of SE and the rise of SYNC. I_{DD4} is a constant term for each device. A brief study of the equation and the values for the I_{DDi} in the data sheet indicate the page mode of operation can be extremely attractive. Figure 3 reflects the V_{DD} power supply current versus the modes and frequencies of operation.

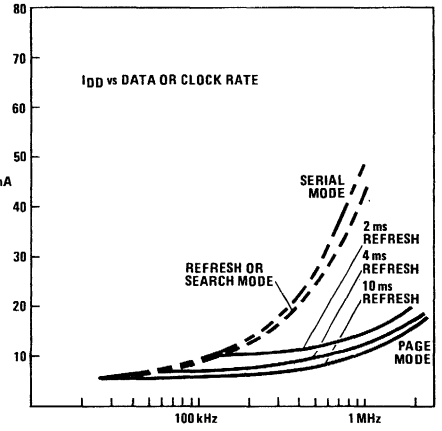


Figure 3. I_{DD} vs Clock or Data Rate @ +70°C

The reduced number of clock cycles permits far lower power supply drain in page mode than that in serial mode even though data rates are higher. The page mode current characteristics shown are plotted versus data rate and reflect the use of a burst refresh scheme where the burst frequency is either the maximum clock frequency of the CCD or a frequency,

$$f = \frac{1}{\frac{t_{REF} - N \cdot t_{CYC}}{256}}$$

where t_{CYC} is the read or write cycle time in page mode and N is the number of memory access cycles required during the refresh period t_{REF} to achieve a given data rate.

Obviously, under the condition of current drain described above, current variations will exist on system power supply lines. It is advisable to provide bypass capacitors to ground, located in close proximity to the V_{DD} pin, for each MM2464 in the system. It is further recommended to make these capacitors relatively large (0.1 μF) in the early development stages and adjust the size for acceptable noise levels after printed circuit board layout is implemented. Similar precautions should be made with respect to V_{BB} transient currents. Power supply layout and distribution should follow the same rules as those utilized in dynamic RAM design.* Clock and data distribution will be far less critical than in CCD or RAM designs with high voltage and/or high capacitance clocks; however, good practices will always provide more margin for noise immunity and device variation.

*Dynamic RAM Board Design Made Easy, *Memory Applications Handbook.*

7

Clock Generation

Ease of clock implementation will be a function of desired system requirements. Figure 4 depicts one logic realization for SE and SYNC at a 1 MHz clock rate; figure 5 shows the waveforms. Several clock generation circuits are depicted; selection of one of these will depend upon design preferences. The circuit schematic of figure 6 presents alteration of the 1 MHz generator to allow maximum clock rates. (Refer to section on Serial Mode Techniques.) Figure 7 presents a less complex circuit which may be realized with CMOS logic. Each of these implementations has been achieved with a clock enable input to allow page or search mode operation. Note that if clock rates exceeding 770 kHz are not required a simple 50% duty cycle SE clock may be utilized as in figure 8.

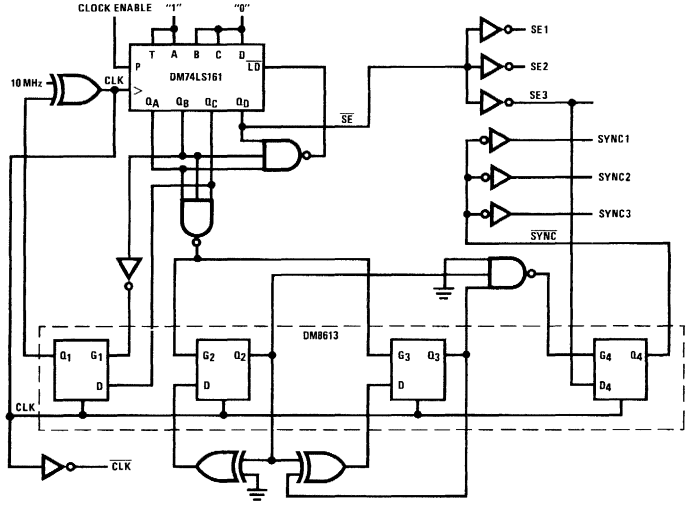


Figure 4. 1 MHz Clock Generator

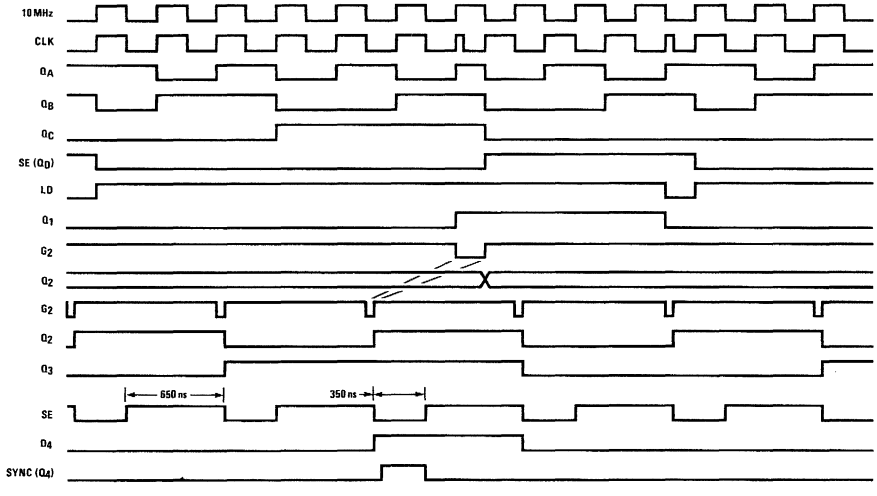


Figure 5. Waveforms for 1 MHz Clock Generator

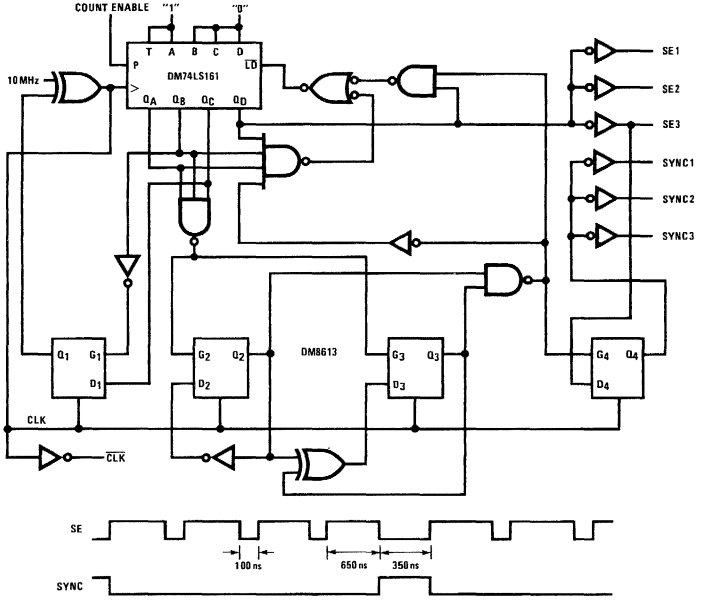


Figure 6. 1.23 MHz Clock Generator

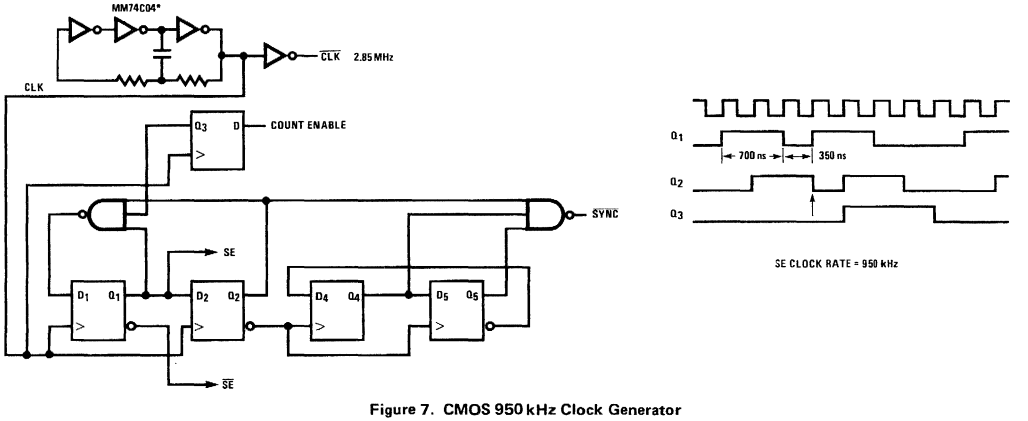


Figure 7. CMOS 950 kHz Clock Generator

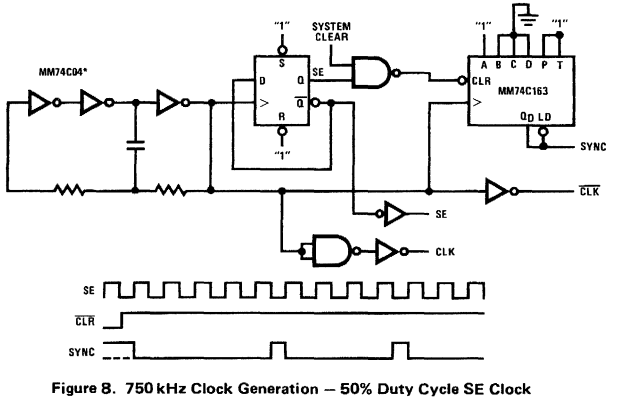


Figure 8. 750 kHz Clock Generation – 50% Duty Cycle SE Clock

*Refer to AN-118, CMOS Oscillators, CMOS Databook.

Refresh Techniques

Several techniques of achieving refresh are available to the system designer. Among these are burst refresh (where a burst consists of 256/b clock cycles at maximum clock frequency and b is the number of bursts during $t_{REF} - b = t_{REF}/t_{PTM}$†), distributed refresh (one clock cycle each $t_{REF}/256$ microseconds) and adaptive refresh. An adaptive refresh circuit monitors system utilization of the CCDs and the various timing restrictions placed upon the memory, assuming command of the system to provide clocking when those restrictions are exceeded. In the case of the adaptive refresh sub-system shown in figures 9 and 10, temperature has been added as a parameter in determining the maximum page times and t_{REF}, the refresh time.

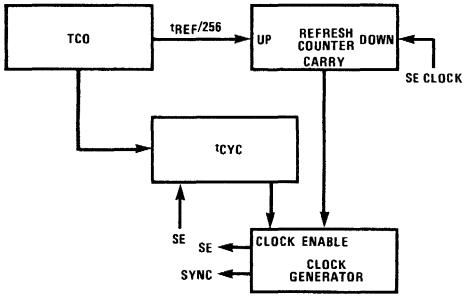


Figure 9. Block Diagram of Adaptive Refresh Circuit

The temperature controlled oscillator generates the clocks for two counters. The refresh counter is counted up by the TCO and down by the SE clock; if a carry is generated a clock cycle is required. A counter determines page time and is reset each time SE occurs; if a carry is generated a clock cycle is enabled. Although this type of refresh control is the most flexible method, many applications such as CRT display and other serial data systems will not need refresh control or may use much less complex techniques requiring fewer components.

Search Techniques

Search mode differs from refresh mode only in speed. While refresh mode implies clocking at very low rates to maintain data integrity, search mode is intended to advance the shift registers to a desired page as quickly as feasible. To achieve this, a counter must keep track of the present page location. In order to access a particular page, the controlling system loads the corresponding address into a register, the output of which is compared to the count state. When the proper page is reached, the clock is stopped and the system is signaled that it may access the requested page. Figure 11 depicts a block diagram of the circuit.

†$t_{PTM} = t_{SCY1\,MAX}$ or $t_{SSY1\,MAX}$, whichever is less.

Page Mode

As mentioned previously, the MM2464 may be treated as read/write memory, and the same design techniques may be used for the CCD as are used for static RAM. An address latch or register may be desirable at the card edge for buffering and to meet address hold time requirements. Chip enable and READ/WRITE input specifications should be noted. A ready or busy signal should be sent to the main system to prevent short cycling of the system or the MM2464. This signal may be the "page change required" signal of figure 10 in faster systems or a decoded output of the page time counter in those with slower reaction times.

Serial Mode

Serial mode consists of treating the MM2464 as a series of addressable parallel shift registers, a worthwhile configuration in display and scanner applications. However, because of the power and speed considerations and because there is no penalty in support parts count, use of the CCD in page mode with addressing being performed by a counter is advisable in the majority of cases. One exception to this will occur in systems where data may be accepted with a random starting location. In this case there is no latency time; the shift register desired is immediately selected and data manipulation commenced at once. When using the MM2464 in this mode, care should be exercised with respect to clocking schemes such as the one shown in figure 6. Here the SE off time with no SYNC pulse (t_{SC1}) has been reduced to data sheet minimum; this time is less than the minimum chip enable time (t_{CE}). Regardless of mode of operation, attention should be paid to the parameters describing the relationship of SE and SYNC to CE. One way of doing this is to assure that chip enable is active (low) only when both SE and SYNC are in the low state.

MM2464 APPLICATIONS

The MM2464 may be considered as an alternate choice to either read/write memory or rotating magnetic memory in a wide variety of applications. And, as is the case with most innovative products, heretofore unconsidered applications will arise. Several factors can be indicative of applicability.

- Bulk Store — wherever large amounts of data must be processed, analyzed or maintained.
- Serial Formats — where sequential ordering of information is inherent in the system philosophy.
- Low Latency — where rotating memories must be replaced or augmented to achieve greater bandwidth.
- Human Interface — where dense random access storage is required and lower speed than conventional RAM is not detrimental.

Examples of each of these will be examined in varying depth.

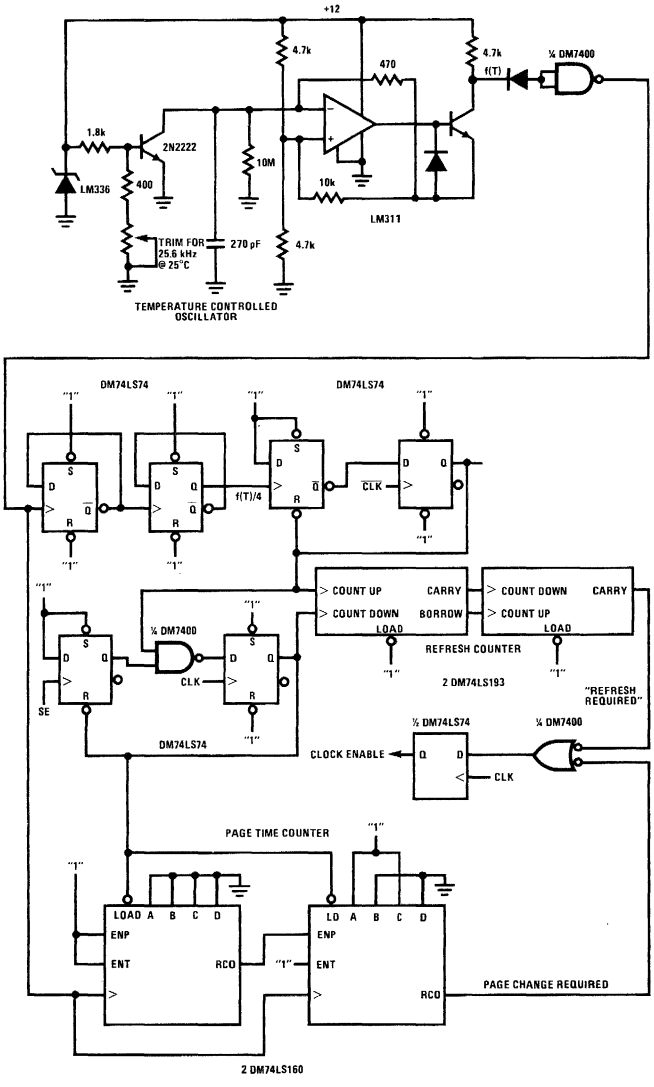


Figure 10. Adaptive Refresh Circuit

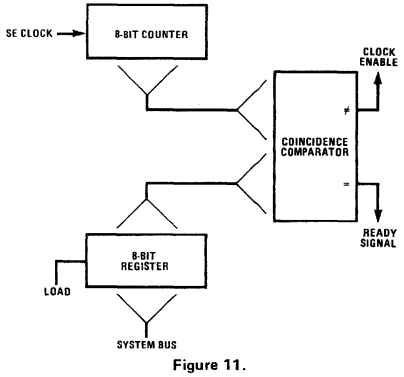


Figure 11.

Bulk Store

Obviously, the CCD may be used, as indicated previously, in page mode by a processor. However, the limitations of maximum page-time may impose restrictions which are unacceptable to the system designer. In such a case, the addition of a R/W memory buffer may resolve the dilemma. Figure 12 blocks out a memory configuration consisting of a page mode driven array of MM2464s which supplies data to, and accepts data from, a buffer consisting of MM5257 4k static RAM. A one-half megabit memory consisting of sixteen memory devices and associated logic will fit on a reasonably small printed circuit board and consume far less power than a system consisting of RAM alone.

This type of system is expandable in many ways. Additional CCD storage is easily added to form multiple megabyte capability. A second RAM page may be added for increased throughput. Loading or storing one page while utilizing the other could result in effectively a zero latency time. An expansion of utility can be achieved by switching from the absolute addressing of figure 12 to a scheme in which the processor assigns a label to each 4k page by writing the label in the first location in the page. To find that page the control system compares an inputted label to data in the shift register in location zero while operating in serial mode. When the label is found a switch is made to page mode and data is transferred to or from the buffer. In large systems, this content addressable technique may be realized by the implementation of wide word lengths and searching with masked "don't care" states using either page/serial or serial/page techniques. Information retrieval of the type accomplished in large data processing systems thus may be realized with minimal CPU time. Bulk memory formats may consist of these techniques or others, but in any case recognition of both the strengths and weaknesses of CCDs can result in high performance architectures.

Serial Formats

Sequentially formatted data obviously lends itself to CCD application and especially to the "square" arrangement of the MM2464. The block diagram of figure 13 depicts a possible configuration for a CRT graphics system. Four MM2464s are arranged in parallel. The resulting 1024-bit word contains the video data for two 512-bit horizontal scan lines of the CRT. The scan lines are arranged one above the other on the screen in an interlaced display; therefore, one of the 512-bit words is accessed during each vertical scan. The CCDs are read via page mode (during the horizontal sweep) at a rate of 2.4 MHz, allowing for 10 microseconds of horizontal retrace time. Clocking the CCD once during horizontal

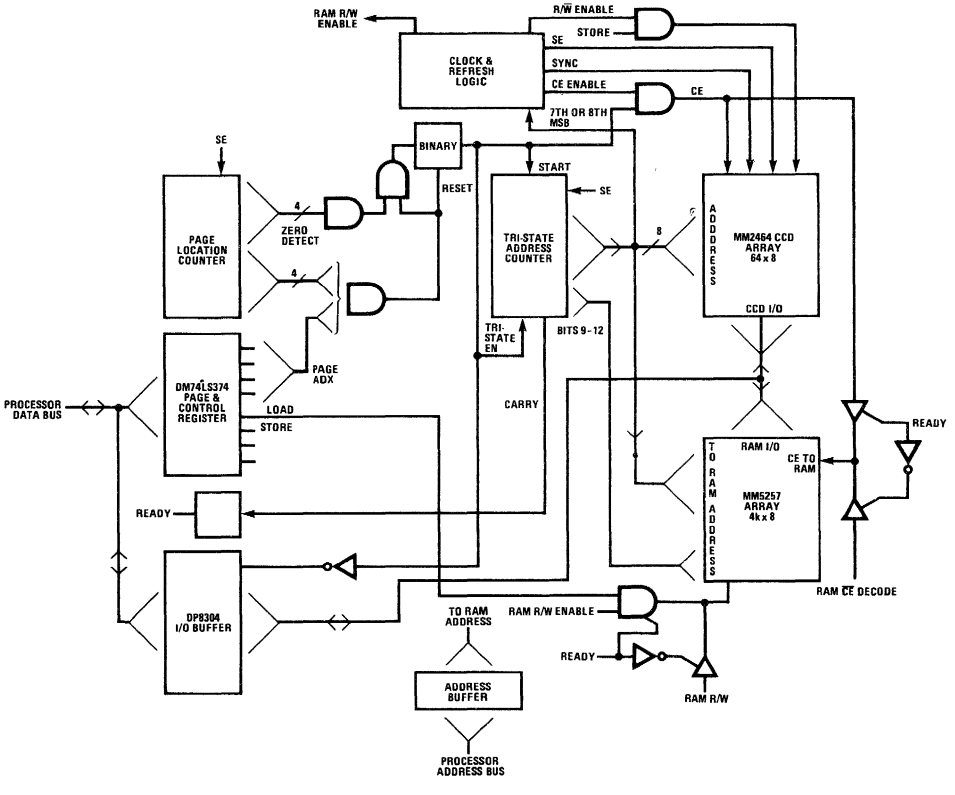


Figure 12.

retrace will not maintain data at extended temperature ranges. In light of this, the clocking scheme shown in figure 14 is proposed. Here the MM2464 is clocked eight times during the first 31 horizontal retrace periods; on the 32nd retrace the device is clocked nine times. Using this method, the CCD page sequence is 0, 7, 15, . . . , 223, 231, 239, 248, 1, ... Figure 11 depicts a 512 x 512 interlaced black and white or two-tone display. Figure 15 shows four of these 512 x 512 blocks combined to produce sixteen gray levels or color tones. The D/A function may be implemented with two National integrated circuits, LM1889 and LM1886. Techniques similar to the ones described here may be used in other types of scanning devices.

Low Latency Applications

Multi-task or multiple user processing systems are often limited in their performance by the latency time of disk and tape memories. This performance can be improved by addition of a buffer or swapping memory into which the contents of the rotating memory may be loaded. The lower latency time (orders of magnitude) and density of the MM2464 make it an obvious choice for the swapping memory, thus providing greatly increased computer bandwidth at a fraction of the cost of other techniques. The configuration of the MM2464 allows construction of a disk-like sector oriented architecture which permits the use of the same software drivers utilized for the rotating device. Thus, the costly penalties of software revision are avoided in addition to accomplishing increased user capacity.

HUMAN INTERFACE APPLICATIONS

Moving from the macro world of the mainframe computer to the micro world of calculators, consider a single-chip microprocessor or calculator oriented device such as an INS8030 or COP420 coupled to a single MM2464. The combination of low power operation and ease of interface of the MM2464 and the programmability of the processing device results in a programmable calculator with 8192 possible (8-bit) program steps or memory locations. The processor can easily drive the two CCD clocks, data input and chip enable with flag and data lines as well as the address port with its own address lines or latched data port.

Further application of CCDs may be found in distributed systems such as point-of-sale terminals which reload data each day from a central processing or storage unit and require only human interface speed for random access.

SUMMARY

CCD memory technology has progressed to the point where a practical device for bulk memory storage has evolved. This device, the MM2464, is a TTL compatible 65,536-bit CCD organized as 256 pages of 256-bit memory. The CCD fulfills a requirement for a dense memory with access times far less than those of rotating magnetic media. A wide variety of applications exist for charge coupled devices in many differing types of systems.

A debt of gratitude is owed to Bob Pease of National's Advanced Linear Integrated Circuit design group and Nello Sevastopoulos and his staff in the Linear Applications section for their contribution of time and effort in conceiving and testing the temperature controlled oscillator.

RECOMMENDED READING

Charge Coupled Devices: Technology and Applications, Edited by R. Melen and D. Buss, IEEE Press, NY, 1977.

Charge Transfer Devices, Sequin and Thompson, Academic Press, NY, 1975.

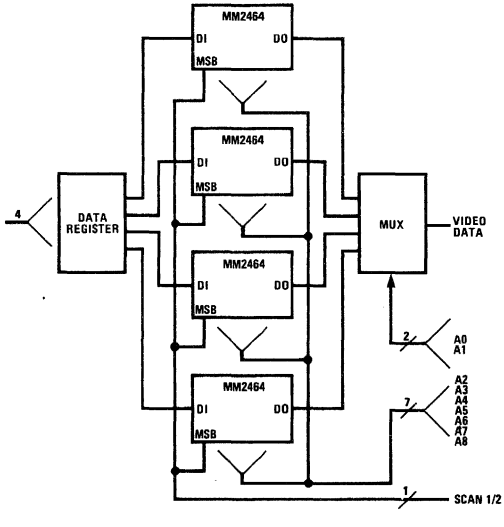


Figure 13. ¼-Megabit CRT Display Memory Using CCDs

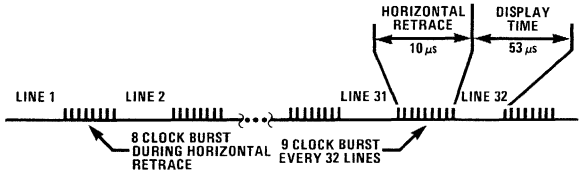


Figure 14. CCD Clock Timing During Display

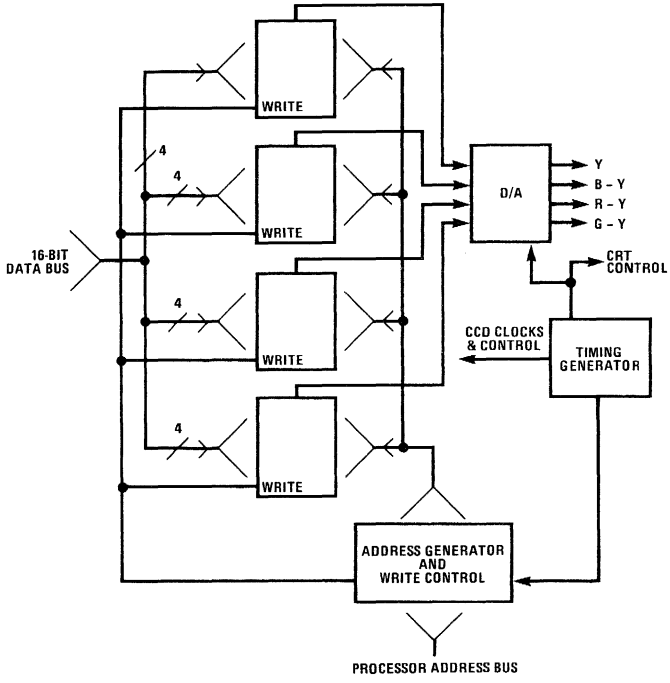


Figure 15. CCD-Based Color Graphics CRT Display

Section 8

Memory Support Components

8

Memory support components are unlike ladies' support garments. Memory support circuits don't merely enhance the appearance of memories; memories *must* have the support circuits to work at all. A memory system does not have the option of going braless; it must have the necessary voltage regulators, clock drivers, and registers to be functional. A few concepts are presented here. For further, in-depth applications information, consult the National Voltage Regulator Handbook and the Interface Integrated Circuits Data Book.

Memory Support Circuits

National offers a selection of memory support circuits to facilitate the interface of memory components in systems architecture. The memory support circuits were developed specifically to accommodate the addressing, clocking, data I/O, and control signals associated with memory systems application as shown in figure 1. Additional circuits are available to interface with data bus structured computers and microprocessors. For additional information contact National's Interface Product Marketing Manager.

FEATURES OF THE TTL LEVEL MOS DRIVERS

Figure 2 compares the switching response of the DS3628 with a 74S TTL gate. Two features can be observed from the switching waveforms: 1) the DS3628 is as fast as the 74S TTL driving TTL loads, and 2) the output high level (V_{OH}) of the DS3628 is higher than that of the 74S TTL.

In a memory system composed of MOS RAMs the load is capacitive and not resistive. Figure 3 compares the switching response of the DS3628 with a 74S TTL gate driving capacitive loads of 50 pF, 150 pF, and 300 pF. The switching waveforms show that the fall time of the DS3628 is as fast as or faster than those of the 74S TTL, but most obvious is the rise time of the DS3628 — much faster than that of the 74S TTL. In addition, the 74S has an objectionable glitch in its rise time. The output high (V_{OH}) level of the DS3628 is higher driving capacitance due to a bootstrap effect in the circuit.

The switching response of the circuits interfacing with a memory array is important since any delay subtracts from the overall memory access time. The switching response driving a capacitive load is more important; as an example, the address drivers might be expected to drive 420 pF in a memory containing 64 MOS RAMs with 5 pF input capacitance each plus 100 pF of board capacitance. The same is typical of clock signals, select signals, and read/write signals.

The input logic levels of MOS RAMs are generally higher than TTL gate levels (typically 400 mV higher). Therefore, the higher output high level (V_{OH}) of the DS3628 is preferable for noise immunity and switching overdrive.

The features of the DS3628 are typical of the other TTL level memory support circuits shown in the Selection Guide.

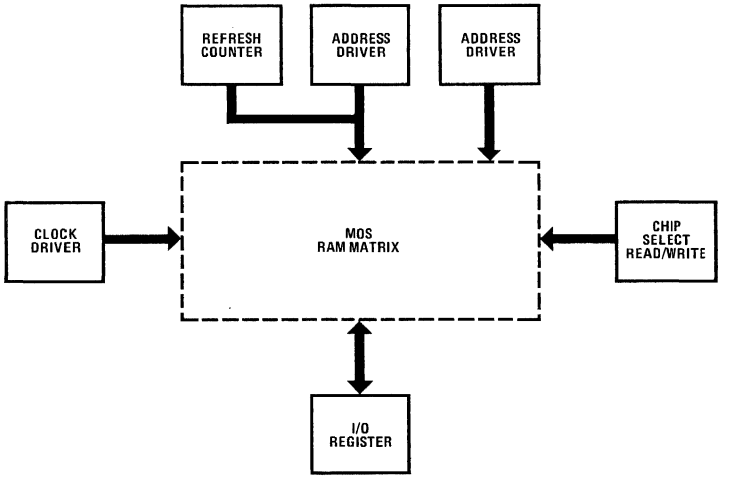


Figure 1. Memory System Block Diagram

DAMPING RINGING OF CLOCK SIGNALS

Ringing of clock signals in a system where the logic fan-out is less than 10 is not generally a big problem, but with higher fan-out the increased capacitive load associated with even a small amount of wiring inductance is a problem. When the capacitance is small the switching currents are small, but as the load increases the increased current through the inductance makes the effect of the inductance increase.

To reduce the associated ringing on the clock signals a resistor may be placed in series with the output of the clock driver to critically dampen the signal response. Many of the memory support circuits are available with this resistor in the output, such as the DS3649 which has a 15 Ω dampening resistor, or the DS3679 which is functionally the same without a dampening resistor.

FALL-THROUGH LATCH

In many memory applications a holding register is required either for address or data I/O. Most commercially available registers have an objectionable propagation delay since the circuit's response is the sum of many gate delays. The address and data I/O paths are critical to the memory system access time and a faster register is preferred. The memory support circuits provide a selection of faster latches. These circuits are the DS3645/75 and the DS3647/77/147/177 series. These registers are faster since the latch function is in parallel instead of series with the signal path.

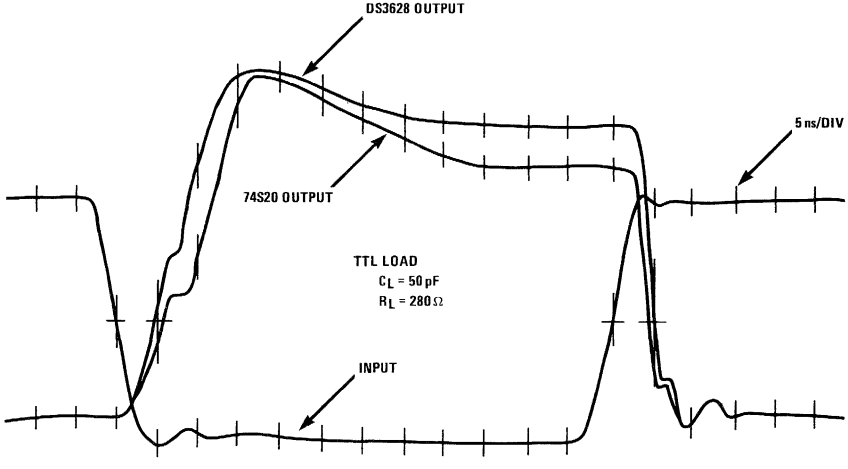


Figure 2. Switching Response with TTL Load

Memory Support Circuit Selection Guide

Device Number & Name	Available Second Source	5 Volt Clock Drivers	12 Volt Clock Drivers	4k RAM Address Drivers	16k RAM Address Drivers	Data I/O	Timing & Control Drivers
DS3628 Octal TRI-STATE™* MOS Driver		X			X		X
DS3640/70 Quad TRI-SHARE™* Port Driver							X
DS3642/72 Dual Bootstrapped MOS Clock Driver			X				
DS3643/73 Quad Decoded MOS Clock Driver			X				
DS3644/74 (3235, MC3460) Quad MOS Clock Driver	X		X				
DS3245 Quad MOS Clock Driver	X		X				
DS3645/75 Hex TRI-STATE MOS Driver Latch	X			X			
DS3646/76 6-Bit TRI-STATE MOS Refresh Counter/Driver				X			
DS3647/77/147/177 Quad TRI-STATE MOS Memory I/O Register	X					X	
DS3648/78 TRI-STATE MOS Multiplexer/Driver		X		X	X		X
DS3649/79 Hex TRI-STATE MOS Driver		X		X			X
DS36149/179 Hex MOS Driver		X		X			X
DS75322/DS3622 Dual TTL-to-MOS Driver	X		X				
DS75361 Dual TTL-to-MOS Driver	X		X				
DS75362 Dual TTL-to-MOS Driver	X		X				
DS75364 Dual TTL-to-MOS Driver	X		X				
DS75365 Quad TTL-to-MOS Driver	X		X				
DP8304 8-Bit Bidirectional Transceiver	X					X	
DP8216/26 4-Bit Bidirectional Transceiver	X					X	
DS8T26/28 Quad TRI-STATE Bus Driver	X					X	
DP8212 8-Bit Input/Output Port	X					X	
CD4024B 7-Stage Ripple-Carry Binary Counter/Divider	X				X		

*A trademark of National Semiconductor Corporation.

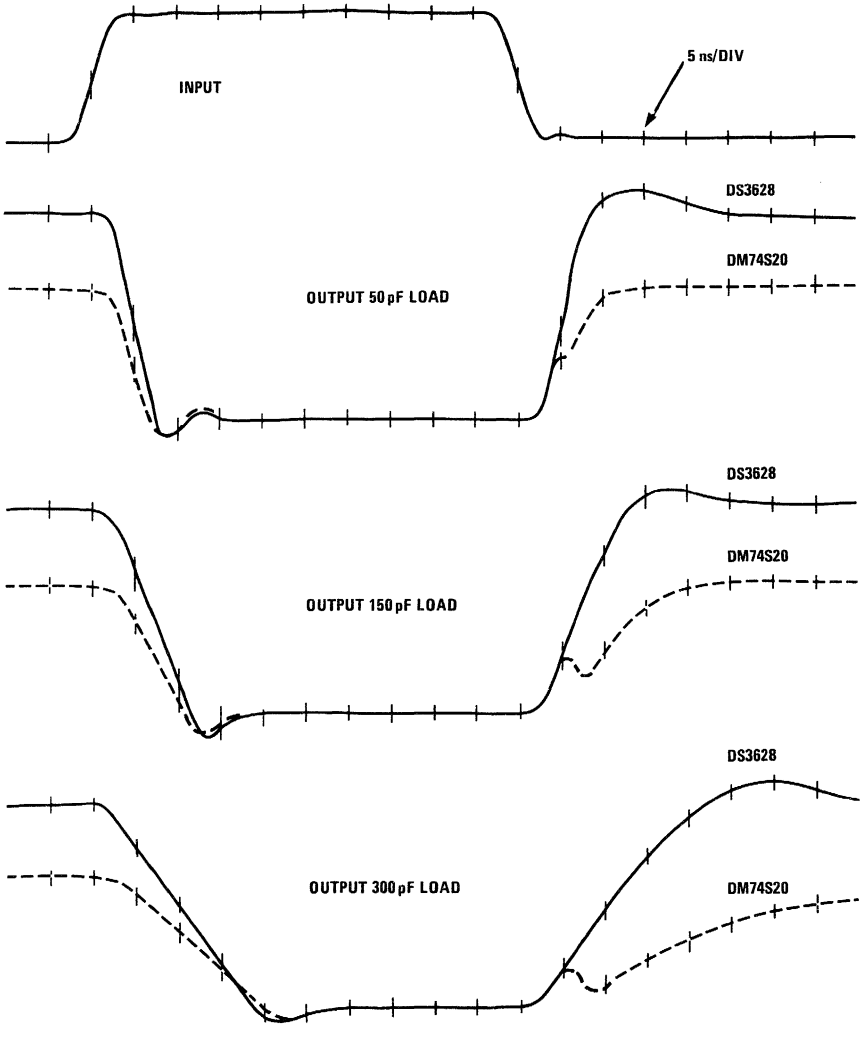


Figure 3. Switching Response with Capacitive Load

Improving Power Supply Reliability with IC Power Regulators

National Semiconductor
Application Note 182
Robert Dobkin
April 1977

Three-terminal IC power regulators include on-chip overload protection against virtually any normal fault condition. Current limiting protects against short circuits fusing the aluminum interconnects on the chip. Safe-area protection decreases the available output current at high input voltages to insure that the internal power transistor operates within its safe area. Finally, thermal overload protection turns off the regulator at chip temperatures of about 170°C, preventing destruction due to excessive heating. Even though the IC is fully protected against normal overloads, careful design must be used to insure reliable operation in the system.

SHORT CIRCUITS CAN OVERLOAD THE INPUT

The IC is protected against short circuits, but the value of the on-chip current limit can overload the input rectifiers or transformer. The on-chip current limit is usually set by the manufacturer so that with worst-case production variations and operating temperature the device will still provide rated output current. Older types of regulators, such as the LM309, LM340 or LM7800 can have current limits of 3 times their rated output current.

The current limit circuitry in these devices uses the turn-on voltage of an emitter-base junction of a transistor to set the current limit. The temperature coefficient of this junction combined with the temperature coefficient of the internal resistors gives the current limit a −0.5%/°C temperature coefficient. Since devices must operate and provide rated current at 150°C, the 25°C current limit is 120% higher than typical. Production variations will add another ±20% to initial current limit tolerance so a typical 1A part may have a 3A current limit at 25°C. This magnitude of overload current can blow the input transformer or rectifiers if not considered in the initial design—even though it does not damage the IC.

One way around this problem (other than fuses) is by the use of minimum size heat sinks. The heat sink is designed for only normal operation. Under overload conditions, the device (and heat sink) are allowed to heat up to the thermal shut-down temperature. When the device shuts down, loading on the input is reduced.

Newer regulators have improved current limiting circuitry. Devices like the LM117 adjustable regulator, LM123 3A, 5V logic regulator or the LM120 negative regulators have a relatively temperature-stable current limit. Typically these devices hold the current limit within ±10% over the full −55°C to +150°C operating range. A device rated for 1.5A output will typically have a 2.2A current limit, greatly easing the problem of input overloads.

Many of the older IC regulators can oscillate when in current limit. This does not hurt the regulator and is mostly dependent upon input bypassing capacitors. Since there is a large variability between regulator types and manufacturers, there is no single solution to eliminating oscillations. Generally, if oscillations cause other circuit problems, either a solid tantalum input capacitor or a solid tantalum in series with 5Ω to 10Ω will cure the problem. If one doesn't work, try the other.

Start-up problems can occur from the current limit circuitry too. At high input-output differentials, the current limit is decreased by the safe-area protection. In most regulators the decrease is linear, and at input-output voltages of about 30V the output current can decrease to zero. Normally this causes no problem since, when the regulator is initially powered, the output increases as the input increases. If such a regulator is running with, for example, 30V input and 15V output and the output is momentarily shorted, the input-output differential increases to 30V and available output current is zero. Then the output of the regulator stays at zero even if the short is removed. Of course, if the input is turned OFF, then ON, the regulator will come up to operating voltage again. The LM117 is the only regulator which is designed with a new safe-area protection circuit so output current does not decrease to zero, even at 40V differential.

This type of start-up problem is particularly load dependent. Loads to a separate negative supply or constant-current devices are among the worst. Another, usually overlooked, load is pilot lights. Incandescent bulbs draw 8 times as much current when cold as when operating. This severely adds to the load on a regulator,

and may prevent turn-on. About the only solutions are to use an LM117 type device, or bypass the regulator with a resistor from input to output to supply some start-up current to the load. Resistor bypassing will not degrade regulation if, under worst-case conditions of maximum input voltage and minimum load current, the regulator is still delivering output current rather than absorbing current from the resistor. *Figure 1* shows the output current of several different regulators as a function of output voltage and temperature.

When a positive regulator (except for the LM117) is loaded to a negative supply, the problem of start-up can be doubly bad. First, there is the problem of the safe-area protection as mentioned earlier. Secondly, the internal circuitry cannot supply much output current when the output pin is driven more negative than the ground pin of the regulator. Even with low input voltages, some positive regulators will not start when loaded by 50 mA to a negative supply. Clamping the output to ground with a germanium or Schottky diode usually solves this problem. Negative regulators, because of different internal circuitry, do not suffer from this problem.

DIODES PROTECT AGAINST CAPACITOR DISCHARGE

It is well recognized that improper connections to a 3-terminal regulator will cause its destruction. Wrong polarity inputs or driving current into the output (such as a short between a 5V and 15V supply) can force high currents through small area junctions in the IC, destroying them. However, improper polarities can be applied accidently under many normal operating conditions, and the transient condition is often gone before it is recognized.

Perhaps the most likely sources of transients are external capacitors used with regulators. *Figure 2* shows the discharge path for different capacitors used with a positive regulator. Input capacitance, C1, will not cause a problem under any conditions. Capacitance on the ground pin (or adjustment pin in the case of the LM117) can discharge through 2 paths which have low current junctions.

If the output is shorted, C2 will discharge through the ground pin, possibly damaging the regulator. A reverse-biased diode, D2, diverts the current around the regulator, protecting it. If the input is shorted, C3 can discharge through the output pin, again damaging the regulator. Diode D1 protects against C3, preventing damage. Also, with both D1 and D2 in the circuit, when the input is shorted, C2 is discharged through both diodes, rather than the ground pin.

In general, these protective diodes are a good idea on all positive regulators. At higher output voltages, they become more important since the energy stored in the capacitors is larger. With negative regulators and the LM117, there is an internal diode in parallel with D1 from output-to-input, eliminating the need for an external diode if the output capacitor is less than 25 μF.

Another transient condition which has been shown to cause problems is momentary loss of the ground connection. This charges the output capacitor to the unregulated input voltage minus a 1–2V drop across the regulator. If the ground is then connected, the output capacitor, C3, discharges through the regulator output to the ground pin, destroying it. In most cases, this problem occurs when a regulator (or card) is plugged into a powered system and the input pin is connected

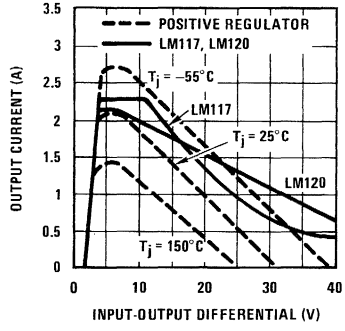


FIGURE 1. Comparison of LM117 Current Limit with Older Positive Regulator

before the ground. Control of the connector configuration, such as using 2 ground pins to insure ground is connected first, is the best way of preventing this problem. Electrical protection is cumbersome. About the only way to protect the regulator electrically is to make D2 a power zener 1V to 2V above the regulator voltage and include 10Ω to 50Ω in the ground lead to limit the current.

LOW OPERATING TEMPERATURE INCREASES LIFE

Like any semiconductor circuit, lower operating temperature improves reliability. Operating life decreases at high junction temperatures. Although many regulators are rated to meet specifications at 150°C, it is not a good idea to design for continuous operation at that temperature. A reasonable maximum operating temperature would be 100°C for epoxy packaged devices and 125°C for hermetically sealed (TO-3) devices. Of course, the lower the better, and decreasing the above temperatures by 25°C for normal operation is still reasonable.

Another benefit of lowered operating temperatures is improved power cycle life for low cost soft soldered packages. Many of today's power devices (transistors included) are assembled using a TO-220 or TO-3 aluminum soft solder system. With temperature excursions, the solder work-hardens and with enough cycles the solder will ultimately fail. The larger the temperature change, the sooner failure will occur. Failures can start at about 5000 cycles with a 100°C temperature excursion. This necessitates, for example, either a large heat sink or a regulator assembled with a hard solder, such as steel packages, for equipment that is continuously cycled ON and OFF.

THERMAL LIMITING GIVES ABSOLUTE PROTECTION

Without thermal overload protection, the other protection circuitry will only protect against short term overloads. With thermal limiting, a regulator is not destroyed by long time short circuits, overloads at high temperatures or inadequate heat sinking. In fact, this overload protection makes the IC regulator tolerant of virtually any abuse, with the possible exception of high-voltage transients, which are usually filtered by the capacitors in most power supplies.

One problem with thermal limiting is testing. With a 3-terminal regulator, short-circuit protection and safe-area protection are easily measured electrically. For thermal limiting to operate properly, the electrical circuitry on the IC must function and the IC chip must be well die-attached to the package so there are no hot spots. About the only way to insure that thermal limiting works is to power the regulator, short the output, and let it cook. If the regulator still works after 5 minutes (or more) the thermal limit has protected the regulator.

This type of testing is time consuming and expensive for the manufacturer so it is not always done. Some regulators, such as the LM117, LM137, LM120 and LM123, do receive an electrical burn-in in thermal shutdown as part of their testing. This insures that the thermal limiting works as well as reducing infant mortality. If it is probable that a power supply will have overloads which cause the IC to thermally limit, testing the regulator is in order.

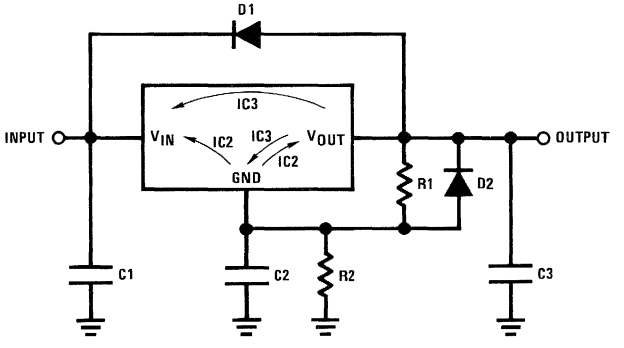


FIGURE 2. Positive Regulator with Diode Protection Against Transient Capacitor Discharge

A Cheap and Easy DC-DC Converter

National Semiconductor
Application Note 183
Paul Brown
May 1977

Many circuits do not live on a positive supply voltage alone; they also require a negative supply voltage. A separate transformer power supply can provide the negative voltage, but this is not always a practical solution. If only a 5V logic supply exists, for example, or if the system is battery powered, an alternate method of obtaining the negative supply voltage must be found.

A DC–DC converter does the job well. Converters are small and can be put on the circuit board that requires the negative voltage. This enables the circuit board to operate from a single positive supply and simplifies power distribution. This application note describes a simple and inexpensive do-it-yourself DC–DC converter for obtaining a negative supply voltage from a positive one.

The DC–DC converter *(Figure 1)* consists of a variable duty cycle pulse generator that controls a transistor switch which in turn drives a flyback circuit. The regulator controls the duty cycle of the pulse generator according to load requirements.

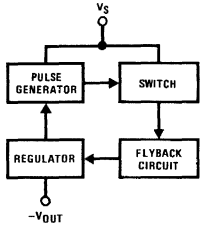


FIGURE 1. Block Diagram

The flyback circuit *(Figure 2)* develops the negative output voltage. When Q1 is ON, current flows through the inductor from Q1 to ground. When Q1 turns OFF, the polarity of the voltage across the inductor reverses, the diode becomes forward biased and a negative voltage appears across the load and filter capacitor C1. When Q1 turns ON again, the voltage across the inductor immediately returns to its original polarity, the diode becomes reverse biased and the filter capacitor discharges through the load maintaining the load current.

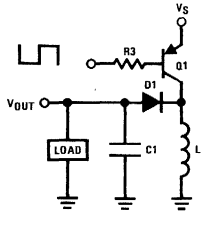


FIGURE 2. Flyback Circuit

The pulse generator *(Figure 3)* is a standard astable LM555 circuit with a diode in parallel with the discharge resistor to enable the $t_{ON}/(t_{ON} + t_{OFF})$ of the switching transistor Q1 to be more than 50%.

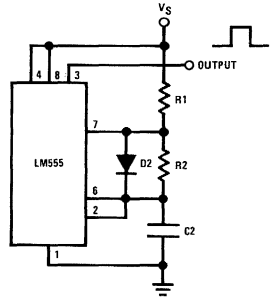


FIGURE 3. Pulse Generator

The output voltage of the converter can be controlled by varying the duty cycle of the pulse generator. This is done by the regulator shown in *Figure 4*. When $V_{BEQ2} + V_{Z1}$ is developed across R5, Q2 turns ON and steals current from the timing capacitor C2, thus controlling the duty cycle of the pulse generator.

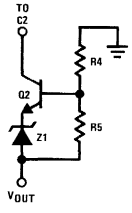
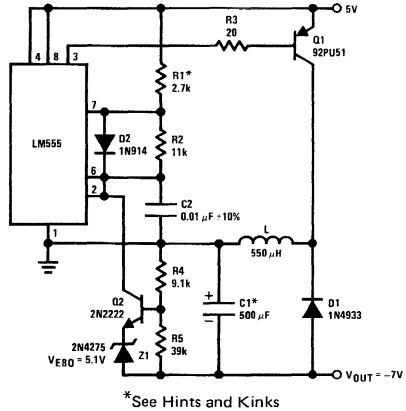


FIGURE 4. Regulator Circuit

Figure 5 shows the complete circuit for the DC–DC converter. For this circuit, with I_{LOAD} = 200 mA and V_S = 5V, efficiency is about 60%, load regulation is 1.3% and supply rejection is 30 dB.



*See Hints and Kinks

FIGURE 5. Complete Circuit

DESIGN EQUATIONS

$$t_{ON} = (L)\,(I_{LOAD})\,\frac{(V_S - V_{SAT}) + |V_{OUT} - \phi 1|}{(V_S - V_{SAT})^2}$$

$$* \quad t_{OFF} = \frac{(V_S - V_{SAT})}{|V_{OUT} - \phi 1|}\,t_{ON}$$

$$* \quad C1 = \frac{I_{LOAD}}{\Delta V_{OUT}}\,t_{ON}$$

$$* \quad R1 = -\frac{t_{OFF}}{C2 \ln \dfrac{3\phi 2 - V_S}{3\phi 2 - 2V_S}}$$

$$R2 = \frac{t_{ON}}{(0.693)\,C2}$$

$$|V_{OUT}| = (V_{BEQ2} + V_{Z1})\left(1 + \frac{R4}{R5}\right)$$

Where: t_{ON} = Time Q1 is ON
t_{OFF} = Time Q1 is OFF
V_S = Supply voltage
V_{SAT} = Saturation voltage of Q1
ΔV_{OUT} = Peak-Peak output ripple
$\phi 1 = V_{BE}$ D1
$\phi 2 = V_{BE}$ D2

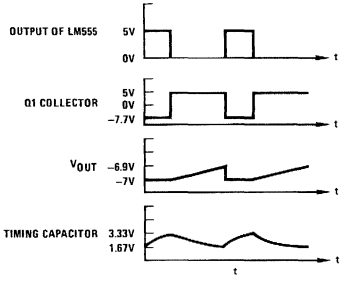


FIGURE 6. Ideal Waveforms

SAMPLE CALCULATIONS

Given:

$L = 550\ \mu H$, $I_{LOAD(MAX)} = 200$ mA, $C2 = 0.01\ \mu F$,
$\phi 2 \simeq 0.60V$
$V_S = 5V$, $V_{SAT} = 1V$, $\phi 1 = 0.7V$,
$V_{OUT} = -7V$, $\Delta V_{OUT} = 100$ mVp-p

Calculate t_{ON}, t_{OFF} and C1:

$$t_{ON} = \frac{(550\ \mu H)\,(0.2)\,(4 + 7.7)}{(4)^2} = 80\ \mu s$$

$$* \quad t_{OFF} = \frac{(550\ \mu H)\,(0.2)\,(4 + 7.7)}{(4)\,(7.7)} = 42\ \mu s$$

*See Hints and Kinks

$$* \quad C1 = \frac{0.2}{0.1}\,80\ \mu s = 160\ \mu F$$

Now calculate R1, R2:

$$* \quad R1 = \frac{-42\ \mu s}{(0.01\ \mu F)\ \ln \dfrac{1.8 - 5}{1.8 - 10}} = 4.5k$$

$$R2 = \frac{80\ \mu s}{(0.01\ \mu F)\,(0.693)} = 11.5k$$

Resistors R3, R4 and R5 can be calculated from the following considerations:

For $\beta_{Q1(MIN)} = 20$, V_{OUT} low from the LM555 = 1V
$V_{BE(Q1)(MAX)} = 1.2V$

For $I_{C(MAX)} = 800$ mA

$I_{B(MAX)} = 40$ mA

$$R3 = \frac{(5 - 1 - 1.2)}{40\ mA} = 70\Omega$$

Allow for an overdrive factor of 3.5

$R3 = 20\Omega$

Given:

$$\frac{V_{OUT}}{R4 + R5} = 150\ \mu A,\ V_{Z1} = 5.1V,\ V_{OUT} = -7V$$

Calculate R4, R5:

$$R5 = \frac{V_{BEQ2} + V_{Z1}}{\dfrac{V_{OUT}}{R4 + R5}} = \frac{5.7}{150\ \mu A} = 38k$$

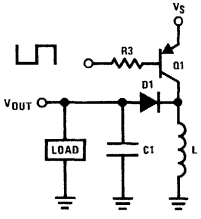
$$R4 = \frac{V_{OUT}}{150\ \mu A} - R5 = \frac{7}{150\ \mu A} - 38k = 8.7k$$

DERIVATION OF DESIGN EQUATIONS

Flyback Circuit *(Figure 7)*

For the inductor

$$V = L\,\frac{d_i}{d_t} \approx L\,\frac{\Delta I}{\Delta t}$$



$t_{ON} = Q1_{SAT}$
$t_{OFF} = Q1_{OFF}$

FIGURE 7. Flyback Circuit

8

For $\Delta t = t_{ON}$

$$\Delta I_{INDUCTOR} = \frac{V_S - V_{SAT}}{L} t_{ON} \quad (1)$$

For $\Delta t = t_{OFF}$

$$\Delta I_{INDUCTOR} = \frac{|V_{OUT} - \phi_1|}{L} t_{OFF} \quad (2)$$

For the capacitor

$$IC1 = C1 \frac{d_v}{d_t} \approx C1 \frac{\Delta V}{\Delta t}$$

For $\Delta t = t_{ON}$

$$IC1\ t_{ON} = I_{LOAD}$$

$$\Delta V_{OUT} = \frac{I_{LOAD}}{C1} t_{ON} \quad (3)$$

Since the change in the energy stored in the inductor during t_{ON} equals the energy lost by the inductor during t_{OFF}, $\Delta I_{INDUCTOR}$ (1) = $\Delta I_{INDUCTOR}$ (2).

Combining (1) and (2)

$$t_{OFF} = \frac{V_S - V_{SAT}}{|V_{OUT} - \phi_1|} t_{ON} \quad (4)$$

During t_{OFF} the capacitor voltage will be restored with an average current $\overline{IC1}$.

$$\overline{IC1} = C1 \frac{\Delta V_{OUT}}{\Delta t_{OFF}}$$

Combining with (3)

$$\overline{IC1} = \frac{t_{ON}}{t_{OFF}} I_{LOAD}$$

Combining with (4)

$$\overline{IC1} = \frac{I_{LOAD} |V_{OUT} - \phi_1|}{(V_S - V_{SAT})} \quad (5)$$

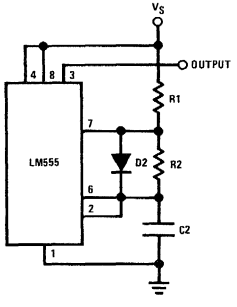


FIGURE 8. Pulse Generator--Astable LM555

During t_{OFF} $\Delta I_{INDUCTOR} = I_{LOAD} + \overline{IC1}$

From (5)

$$\Delta I_{INDUCTOR} = \frac{I_{LOAD} [(V_S - V_{SAT}) + |V_{OUT} - \phi_1|]}{(V_S - V_{SAT})} \quad (6)$$

From (1) and (6)

$$t_{ON} = \frac{(L)(I_{LOAD})[(V_S - V_{SAT}) + |V_{OUT} - \phi_1|]}{(V_S - V_{SAT})^2} \quad (7)$$

From (2) and (6)

$$t_{OFF} = \frac{(L)(I_{LOAD})[(V_S - V_{SAT}) + |V_{OUT} - \phi_1|]}{(V_S - V_{SAT})(|V_{OUT} - \phi_1|)} \quad (8)$$

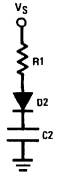


FIGURE 9. Charge Circuit

Pulse Generator *(Figures 8–10)*

For the LM555

$$\frac{2V_S}{3} \geq V_T \geq \frac{V_S}{3}$$

From circuit theory:

$$V_T = V_F + (V_i - V_F)e^{-t/\tau} \quad (9)$$

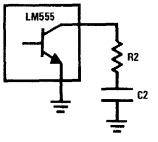


FIGURE 10. Discharge Circuit

Where V_F = Final voltage on capacitor
V_i = Initial voltage on capacitor
V_T = Threshold voltage

For charge time:

$$V_F = V_S - \phi_2$$

$$V_T = \frac{2V_S}{3}$$

$$V_i = \frac{V_S}{3}$$

$$\tau \approx R1C2$$

After substitution in (9)

$$t_{OFF}\ (\text{output high}) = -R1C2\ \ln \frac{3\phi_2 - V_S}{3\phi_2 - 2V_S} \qquad (10)$$

For discharge time:

$V_F = 0.04$ (saturation voltage of discharge transistor)

$$V_T = \frac{V_S}{3}$$

$$V_i = \frac{2V_S}{3}$$

$\tau \approx R2C2$

After substitution in (9)

$$t_{ON}\ (\text{output low}) = -R2C2\ \ln \frac{V_S - 0.12}{2V_S - 0.12}$$

$$\approx (0.693)\ R2C2 \qquad (11)$$

Regulator Circuit *(Figure 11)*

$$\left(\frac{V_{OUT}}{R4 + R5}\right) R5 = V_{BEQ2} + V_{Z1}$$

Rearranging

$$V_{OUT} = (V_{BEQ2} + V_{Z1}) \left(1 + \frac{R4}{R5}\right) \qquad (12)$$

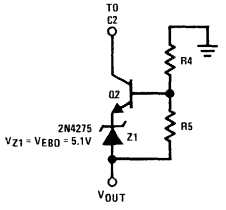


FIGURE 11. Regulator Circuit

HINTS AND KINKS

The output voltage has more than the predicted amount of ripple as well as some fast high amplitude spikes. These anomalies are due to the reverse recovery time of the rectifier diode and the pulse response of the filter capacitor. The ripple can be reduced to the desired level by increasing the size of the filter capacitor. The spikes, however, are a bit more troublesome. The filter circuit shown in *Figure 12* eliminated the spikes on the prototype. The ferrite beads in conjunction with the ceramic capacitor filter out the fast rising spikes. Paralleling the 2 halves of the filter capacitor has the effect of reducing the ESR (Effective Series Resistance) of the filter capacitor.

The full load regulation can be improved by decreasing R1 to compensate for circuit losses.

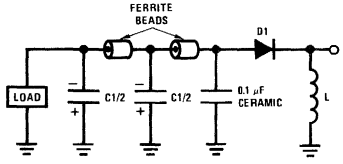


FIGURE 12. Filter Circuit for Removing Glitches

Figure 13 shows a simple scheme for short circuit protection and *Figure 14* shows a scheme for electronic shutdown.

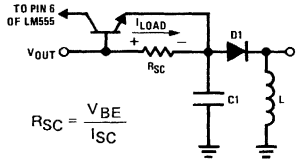


FIGURE 13. Short Circuit Protection

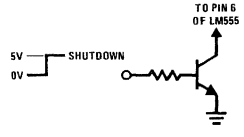


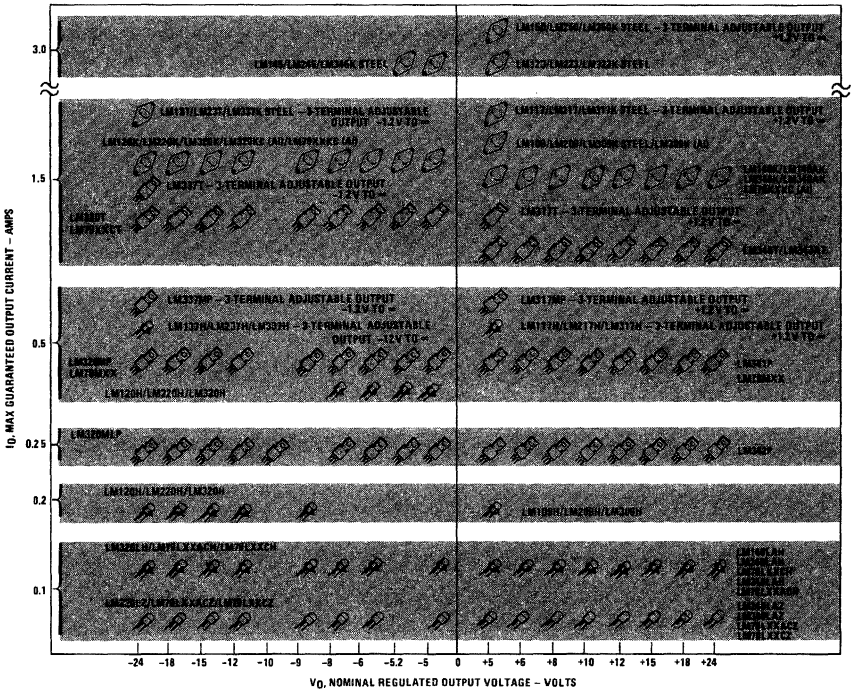
FIGURE 14. Electronic Shutdown

REFERENCES

Mortensen, Helge H., "+5 to −15 Volts DC Converter" LB-18, National Semiconductor Corporation.

Widlar, R.J., "Designing Switching Regulators" AN-2, National Semiconductor Corporation.

National's Voltage Regulator Guide



Note: All devices with TO-3 package designation (K and K STEEL) are supplied in steel TO-3 packages unless otherwise designated as (Al) aluminum TO-3 package.

THREE-TERMINAL VOLTAGE REGULATORS

Output Current		Positive Output Voltage		Negative Output Voltage	
		Fixed Output Voltage	Adjustable [2] Output Voltage	Fixed Output Voltage	Adjustable [2] Output Voltage
3 Amp	Device	LM323	LM350	LM345	
	Output Voltage	+5.0V	+1.2V to +33V	-5.0V, -5.2V	
	Package	TO-3	TO-3	TO-3	
1.5 Amp	Device	LM340-XX, LM78XX	LM317	LM320-XX, LM79XX	LM337
	Output Voltage	+5V, +6V, +8V, +10V, +12V, +15V, +18V, +24V	+1.2V to +37V High Voltage (HV) +1.2V to +57V	-5.0V, -5.2V, -6.0V, -8.0V, -9.0V, -12V, -15V, -18V, -24V	-1.2V to -37V High Voltage (HV) -1.2V to -47V
	Package	TO-3, TO-220	TO-3, TO-220	TO-3, TO-220	TO-3, TO-220
0.5 Amp	Device	LM341-XX, LM78MXX	LM317M	LM320M, LM79MXX	LM337M
	Output Voltage	+5V, +6V, +8V, +10V, +12V, +15V, +18V, +24V	+1.2V to +37V	-5.0V, -5.2V, -6.0V, -8.0V, -9.0V, -12V, -15V, -18V, -24V	-1.2V to -37V
	Package	TO-202	TO-202, TO-39	TO-202, TO-39 [1]	TO-202, TO-39
0.25 Amp	Device	LM342-XX		LM320ML	
	Output Voltage	+5V, +6V, +8V, +10V, +12V, +15V, +18V, +24V		-5.0V, -6.0V, -8.0V, -10V, -12V, -15V, -18V, -24V	
	Package	TO-202		TO-202	
0.10 Amp	Device	LM340LA-XX, LM78L-XX		LM320L-XX, LM79L-XX	
	Output Voltage	+5V, +6V, +8V, +10V, +12V, +15V, +18V, +24V		-5V, -6V, -8V, -9V, -12V, -15V, -18V, -24V	
	Package	TO-39, TO-92		TO-92, TO-39	

Note 1: Some voltage options are rated only to 200 mA.
Note 2: Adjustable voltage regulators can regulate voltages to infinity.

Section 9

Microprocessor Guide

9

Microprocessors, or digital computers for $4 to $200, are more than simply the well-publicized "in" things of today's technical press and the electronic industry. These "microcomputers" have caused a major upheaval — *computers are free* — or *nearly* free. In the past, computers used to occupy large air conditioned rooms, consumed large amounts of power, and were so expensive that even small amounts of rental time kept them out of reach of the average application. Revolutions in high-density digital silicon MOS fabrication have created new low-cost IC components which allow single board computers which can be economically applied in both simple industrial controls and even consumer products. National offers a full range of microprocessors and support circuits for the full range of applications.

National's Full Spectrum of Microprocessors

National Semiconductor offers the broadest line of microprocessors of any semiconductor manufacturer in the world. With 4-bit, 8-bit, 16-bit and bit-slice devices, this selection offers the designer an intelligent choice in capabilities, speeds and costs. Some of the benefits of dealing with National are:

- Cost effectiveness — because of our variety of microprocessors for a full range of applications
- 16-bit COMPUTATION microprocessors for precision control functions
- 8-bit BYTE HANDLING microprocessors for terminals 4/8-bit LOW-COST CONTROL microprocessors for industrial controllers
- Second sourced families
- Ready, off-the-shelf availability
- MICRO+ — special reliability and quality program
- Full development system support — all the way from the high-powered Universal Development System (a disk operating system with numerous software packages) to low-cost development systems.

National Semiconductor also offers the most extensive line of CPU-to-peripheral support products — for digital input/output, communications, peripheral control, and memory. And National is constantly expanding these support lines.

National's INS8080A Family

Positioned between the cost-effective SC/MP and the highly versatile 8900, National's 8080A can be used in systems which range from a few family components to designs which utilize its full capabilities. National offers the broadest line of peripheral circuits and memories to complement the basic 8080A CPU. National's 8080A features:

- Family approach to system design
- Complete CPU group
- Programmable input/output concepts
- Multiple source availability
- Complete line of support components

National's INS2650 Family

The 2650 Family consists of a series of memory and peripheral components built around the 2650A 8-bit microprocessor. This second-sourced processor family offers excellent byte and bit manipulation for a variety of applications.

Seventy five variable-length instructions — one, two, and three bytes — comprise the instruction set, thus minimizing memory requirements. Some of National's INS2650 family features are:

- Single-phase clock
- Single 5-volt power supply
- TRI-STATE data and address signals
- Single-level, address-vectoring interrupt mechanism.

National's INS8900 Family

The 8900 is a complete, 16-bit "minicomputer on a chip." Its wide word length, hardware-vectored interrupt structure, and sophisticated addressing modes make it ideal for laboratory instrumentation, data acquisition and process control application, where number handling and fast response are most important.

Among the outstanding features of the 8900 are its 8-bit or 16-bit data handling, exceptional data-processing throughput, compatibility with National's IMP-16 microprocessors, and large variety of support chips.

National's SC/MP Family

SC/MP is National's simple, cost-effective microprocessor. It is the lowest-cost replacement for electrical, mechanical and hydraulic control systems.

The growing family of SC/MP devices includes an NMOS CPU (INS8060), a RAM-I/O chip with 16 I/O lines, and a variety of bus-oriented interface and memory devices. The SC/MP CPU itself incorporates unique multiprocessor control logic to facilitate distributed processing systems with the lowest number of components. The INS8060 also has a built-in Clock, Parallel and Serial I/O; it uses low power; and it can interface to standard memory and peripheral products. Also available is a BASIC-type high-level language called NIBL, which is available in a MAXI-ROM form for fast software development.

National's INS4004 Family

INS4004 is National's second source to the MCS-4 family. This was the first production microprocessor system, and it is still a popular 4-bit microprocessor because of its simplicity and low cost. Some of National's INS4004 features are:

- Four-bit parallel CPU
- Applicable for use in test systems, terminals, billing machines, process control, and random logic replacement
- Readily interfaces with keyboards, switches, displays, A/D converters, and various peripheral equipment
- Ability of CPU to address 4k 8-bit instruction words, 5,120 bits of RAM, up to 16 4-bit input ports, and 16 4-bit output ports

National's IDM2900 Family

The IDM2900 Bipolar Slice Family uses very fast, unique, low-power SCL (Schottky/ECL) technology. The heart of the 2900 family is the 2901A 4-Bit Slice CPU, which has become the industry standard in slice architecture. The IDM2900 family may be used in sundry combinations to emulate a multitude of CPU architectures — in contrast to fixed-instruction microprocessors. The word length of a 2900-based microprocessor may be any multiple of 4 bits. Each 2900 device performs a basic function, which is controlled by an appropriate microinstruction of a microprogrammed system.

National's Fast IDM2900 Bit-slice Microprocessor Family

No matter how you slice it, the 60 nanosecond IDM2900 bipolar microprocessor family of components from National Semiconductor is the best bit-slice solution to your system design problems.

Until now, computer system designers had to choose between high speed and low power. They couldn't have both. It was a choice between power-draining emitter coupled logic on the one hand, and low power Schottky designs, such as previous 2900 bit-slice architectures, on the other.

With National's IDM2900 series, systems designers can have both – ECL speeds and LS bipolar power consumption. We call this new technology "SCL."

The 60 ns Slice

Centerpiece of the industry's new bipolar bit-slice standard is National's IDM2901A, a 4-bit microprocessor slice with an on-chip 16-word by 4-bit two-port RAM, a high speed eight function arithmetic logic unit, as well as the associated shifting, decoding and multiplexing circuitry.

The IDM2901A features a typical microcycle time of only 60 nanoseconds, a 30 to 50 percent improvement over LS bipolar implementations of previous generations. But power consumption is no more than that for low power Schottky versions – only 800 milliwatts.

In addition, National's IDM2901A has significantly improved almost every timing parameter. The read-modify-write cycle and the minimum clock period, for example, are 43 percent less; and the maximum clock frequency is 68 percent greater. Moreover, the IDM2901A provides higher drive current capability, with attendant IOS increase.

And also available is an even higher performance speed selected version – the IDM2901A-1.

A Full Family

There's more to National's bit-slice bipolar microprocessor story. In addition to the IDM2901A, twelve of the industry standard components in the IDM2900 family are being introduced, most with equivalent performance and power consumption improvements. The new SCL bipolar parts:

- IDM2902, a high speed carry lookahead generator capable of anticipatory carry across four binary adders or groups of adders. This part is frequently used to propagate carry terms to the most significant package when multiple 2901A parts are required.
- IDM2909A/2911A, four-bit-wide address controllers used to sequence through a series of microinstructions contained in ROM or PROM. The 2911A is functionally adequate for most applications; however, the input word cannot be masked, as can be done with the 2909A.
- IDM29702, a 64-bit RAM with TRI-STATE™* outputs, organized as sixteen 4-bit words and fully decoded with chip enable input. This part can be used as a file extension register, a memory stack or for other similar applications.
- IDM29703, a 64-bit RAM with open collector outputs, organized as sixteen 4-bit words, and fully decoded with chip-enable input. It is useful in systems that use data bus lines with a defined pull-up impedance.
- IDM29750, a 256-bit field programmable read only memory with open collector outputs, organized as thirty two 8-bit words, with on-chip decoding and 5-bit binary addressing. It is useful for logic replacement, logic extension and as an external multiplexer.
- IDM29751, TRI-STATE counterpart of the IDM29750.
- IDM29760/61, field programmable 1024-bit PROMs with open collector and TRI-STATE outputs, respectively. These parts are frequently used for logic replacement, gate matrices, multiplexers and so on.
- IDM29803, a branch controller with 16 separate instructions that is capable of performing a 2-, 4-, 8-, or 16-way branch in one microprogram execution cycle. Useful in complex processor/controller systems for address controller systems for address modification and as a variable input mask for systems using the 2909A/2911A address controllers.
- IDM29811, a next state controller unit that is used with the 2909A/2911A for microprogram control.
- IDM29902, an eight-line to three-line priority encoder that is useful in interrupt-driven systems.

All these parts are plug- and function-compatible with LS bipolar components of the previous generation of 2900 parts. And both commercial and military applications can be served by National's IDM series of parts.

Increased Efficiency

To improve the efficiency and throughput of the 2900 architecture, National is also introducing new proprietary bit-slice components that take advantage of the basic process-related speed improvements. These include:

- IDM29901, an octal, edge-triggered flip-flop with TRI-STATE outputs designed to drive high capacitance loads or those of relatively low impedance. This part is useful as a utility register or for temporary data storage.
- IDM29903, a 16-word by 4-bit clocked RAM organized as an addressable "D" register file. Any word can be asynchronously read out of or written into on the next clock transition. The data is not complemented; thus, this part is an ideal choice for file extension.

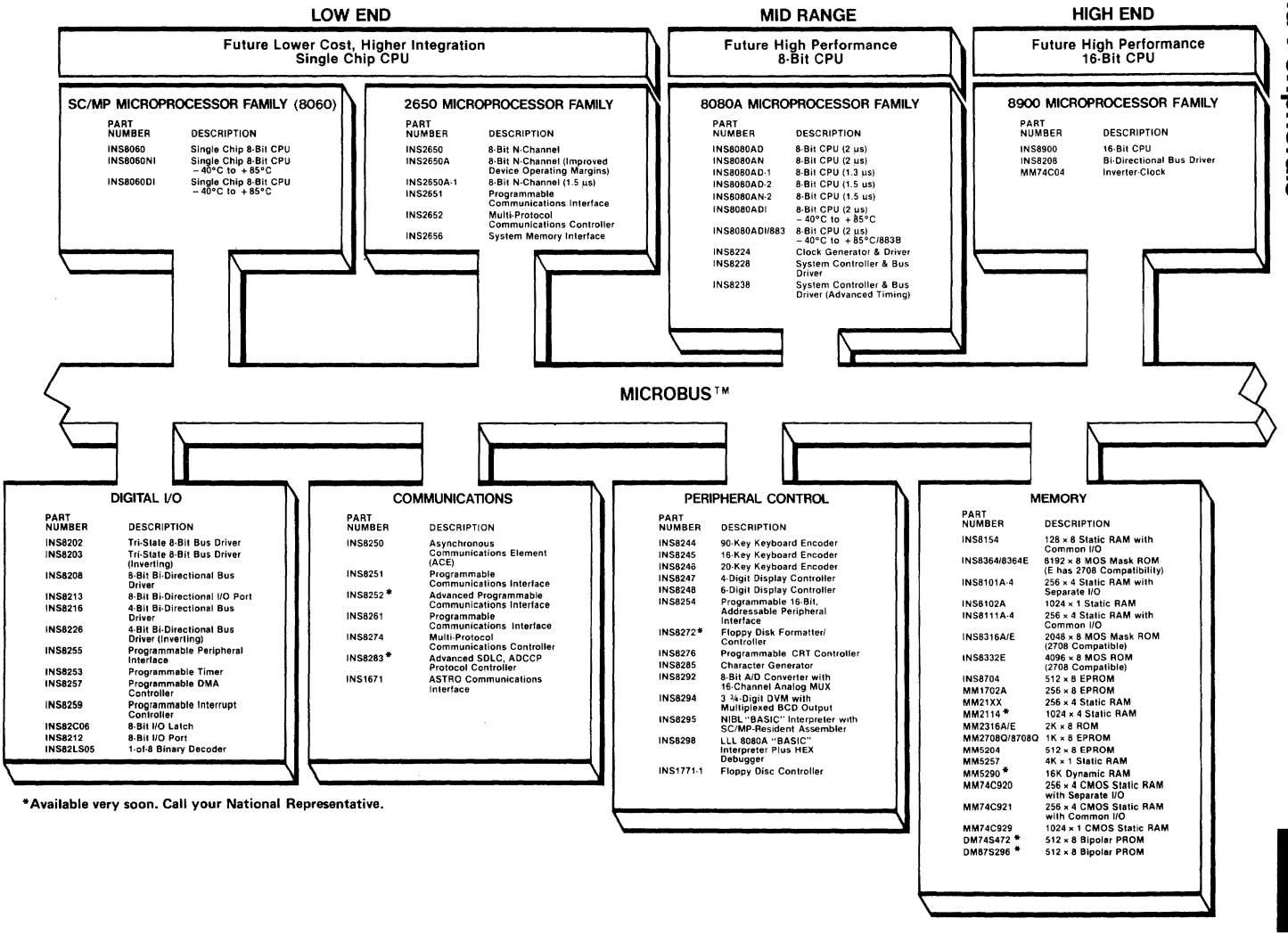
With National's family of standard IDM2900 components, system designers can have both ECL-type throughputs and LS bipolar power consumption and interface capability.

Used in a typical design, system microcycle time is in the 100 to 150 ns range, about one half to two thirds that of previous LS bipolar parts.

Execution time for a typical operation, such as an add and shift (multiply) is 95 ns maximum and 60 ns typical; again, a significant gain over previous 2900 implementations.

National Semiconductor chose the 2900 four-bit bipolar bit-slice architecture because, as the industry standard, it is the most popular and widely understood. And, except for speed, it has been the most versatile bit-slice around. Now, with the IDM2900 family from National, users get ECL high speeds, too.

*A trademark of National Semiconductor Corporation.



*Available very soon. Call your National Representative.

National's Spectrum of Microprocessors and Peripherals

Section 10

Systems Applications

Memory system applications range from a chip used in a microprocessor system to an add-on memory for a large mainframe computer. Today's memory components allow the memory for many systems to be implemented on a single card (or multiples of a single card). Examples of this type of system are presented here.

Systems Application of MM5270 4k Dynamic RAM

DESCRIPTION – STORAGE BOARD

This document describes the general features of the 1617 Storage Card. It includes a description of the functional capabilities and the physical and electrical specifications.

The 1617 Storage Board is a memory array capable of storing up to 16,384 17-bit words. 17-bit words are always stored or read and can be accessed in any sequence. The storage element on the board is the National Semiconductor MM5270 4k Dynamic RAM.

The memory capacity is 16k x 17 bits. The storage card is organized as 4 rows of 4k RAMs with 17 memory elements in each row.

MODES OF OPERATION

1. Read 2. Write 3. Refresh

ACCESS AND CYCLE TIMES

Read Access from Address . . . . . 340 ns
Read Access from CE . . . . . 320 ns
Read, Write, and Refresh . . . . . 460 ns

MEMORY – INTERFACE

MEASUREMENTS

All input/output signals are measured at the memory board input/output connector. Times shown in the Timing Diagrams (figures 1, 2, and 3) are measured at the 1.5V point of the signal transition.

LOGIC LEVELS & LOADING

All of the interface signals are standard TTL levels. Logic 0 = 0V to +0.5V; logic 1 = +2.4V to +5.0V. Input loading on all input signals is one standard TTL load. Output drivers on all output signals are capable of driving 10 standard TTL loads.

SIGNAL DESCRIPTION

This describes all input/output signals of the 1617. Refer to the Timing Diagrams (figures 1, 2, and 3) in the Appendix.

Chip Enable (CE)

CE initiates all cycles. This signal is active HIGH and becomes the chip enable signal for the 4k RAMs. It has a minimum HIGH time of 260 ns and a minimum LOW time of 200 ns. Output data is latched on the storage card coincident with the trailing (negative-going) edge of Chip Enable.

Read/Write ($\overline{R}$/W)

$\overline{R}$/W is a control signal which is LOW for a Read cycle and HIGH for a Write cycle. It must be valid at the leading edge of CE and remain so for a minimum of 20 ns after the trailing edge of CE. During a Refresh cycle, $\overline{R}$/W may assume either logic level.

Memory Select ($\overline{MS}$)

$\overline{MS}$ is a control signal which selects the storage board. During Read and Write cycles it must be LOW a minimum of 24 ns before the leading edge of CE and remain so for a minimum of 20 ns after the trailing edge of CE. During a Refresh cycle, $\overline{MS}$ may assume either logic level.

Tri-Share Port ($\overline{TSP}$)

$\overline{TSP}$ is a signal that controls Read, Write, or Refresh operations for the 4k RAMs. During a Read cycle it must be LOW for a minimum of 20 ns before the leading edge of CE and remain so for a minimum of 30 ns after the trailing edge of CE. During a Write cycle $\overline{TSP}$ must be LOW for a minimum of 20 ns before the leading edge of CE and remain so for a minimum of 80 ns before returning HIGH. A LOW-to-HIGH transition of $\overline{TSP}$ (after leading edge of CE) must occur a minimum of 150 ns before the trailing edge of CE and remain HIGH for at least 100 ns. During a Refresh cycle $\overline{TSP}$ must be HIGH for a minimum of 20 ns before the leading edge of CE and remain so for a minimum of 80 ns after the leading edge of CE.

Output Enable (DA)

DA is a control signal which enables the data out bus (DO0 - DO16) and allows the Read data to be latched into the TRI-STATE® registers (DM8123). During a Read cycle DA must be HIGH for a minimum of 180 ns before the trailing edge of CE and remain so until the trailing edge of CE or later. Data will remain on the bus for a minimum of 10 ns after DA goes LOW or $\overline{MS}$ goes HIGH. During Write and Refresh cycles it must remain LOW.

Refresh (REFH)

REFH is the memory Refresh signal. During a Refresh cycle REFH must be HIGH for a minimum of 12 ns before the leading edge of CE and remain so for a minimum of 20 ns after the trailing edge of CE. During Read and Write cycles REFH must be LOW.

Address In 0-11 (A0-A11)

A0-A11 are the 12 address lines which are the inputs to the address drivers (DS3679) which drive the address lines of the 4k RAMs. During all cycles, all address (A0-A11) lines must be stable for a minimum of 20 ns before the leading edge of CE and remain so for a minimum of 20 ns after the trailing edge of CE.

Address In 12-13 (A12, A13)

A12 and A13 are the two high-order address lines which are decoded by the clock driver (DS3673) to select one of the 4 rows of RAMs during Read and Write cycles. During Read and Write cycles A12 and A13 must be stable for a minimum of 20 ns before the leading edge of CE and remain so for a minimum of 20 ns after the trailing edge of CE. During Refresh cycles A12 and A13 may assume either logic level.

Data In 0-16 (DI0-DI16)

DI0-DI16 are the 17 data input lines to the board. During a Write cycle Data In must be stable for a minimum of 150 ns before the trailing edge of CE and remain so for a minimum of 50 ns after the trailing edge of CE. During Read and Refresh cycles, DI0-DI16 may assume either logic level.

Data Out 0-16 (DO0-DO16)

DO0-DO16 are the 17 data output lines of the board. During a Read cycle Data Out will be valid a maximum of 320 ns after the leading edge of CE. Data will remain valid on the bus for a minimum of 10 ns after DA goes LOW or $\overline{MS}$ goes HIGH. During Write and Refresh cycles DO0-DO16 will be in a high-impedance state.

REFRESH REQUIREMENTS

The 4k RAM is organized as 64 rows by 64 columns of memory cells. The 64 rows correspond to the 64 binary combinations of the 6 lower address (A0-A5) bits. Each row (corresponding to one of the 64 combinations of A0-A5) must be accessed (Refresh cycles) during any 2 ms period. The logic states of A6-A11 must be stable during a Refresh cycle but may assume either level.

POWER REQUIREMENTS

The DC voltages may be turned on or off in any sequence.

	+15 V ± 5%	−15 V ± 10%	+5 V ± 5%
Normal (Read, Write, Refresh)	850 mA*	8 mA	725 mA
Standby (Refresh only)	90 mA*	8 mA	725 mA

*Based on a 2 ms refresh rate.

DESCRIPTION — MECHANICAL

SIZE

The board size is 8.5 x 11.0 inches. It is a 2-layer (no internal layers) PC board with a maximum component height of 0.45 inch. This allows card mounting on 5/8 inch centers. Power and ground and all signals enter and exit the board via the 144-pin card edge connector.

I/O CONNECTOR

There is one I/O connector interface on each board, a 144-pin interface that supplies power and ground and all signals. The pin spacing is 0.125 inch. Mating connector assemblies are manufactured by Dyna-Tech Inc., Santa Ana, California.

DESCRIPTION — ENVIRONMENTAL

OPERATING CONDITIONS

The 1617 Storage Card is capable of operating continuously and reliably under any practical combination of the following environmental stresses:

Cooling Required: Adequate cooling of the memory card operating in its worst case power dissipation mode will require a minimum air flow of 10 CFM.

Temperature: The range of ambient air temperature is +10°C to +50°C.

Thermal Shock: The equipment is capable of operating reliably through a thermal shock with a maximum rate of ±10°C per hour.

Humidity: The system is designed to operate reliably in a relative humidity of up to 95% (without condensation).

Altitude: The system is designed to operate reliably at altitudes from −1,000 feet MSL to +10,000 feet MSL.

SHIPPING AND STORAGE SPECIFICATION

When packaged for shipment, the 1617 withstands stresses as normally encountered during shipment by common carrier. In addition, the following specific criteria are applicable:

Temperature: The card is capable of withstanding a shipping temperature range of −40°C to +85°C.

Thermal Shock: The card is capable of withstanding a shipping thermal shock of as high as +40°C in a period of 2 minutes.

Altitude: The card is capable of withstanding a shipping altitude of 40,000 feet.

RELIABILITY

The 1617 is designed for high reliability and maintainability.

SERVICE LIFE

The 1617 is designed for a service life of ten years at 24 hours per day exclusive of time required for periodic routine maintenance.

Quality and Workmanship: Workmanship, manufacture, and testing are consistent with best commercial practices of the computer industry.

Protective Features: The 1617 provides protection features to minimize the risk of catastrophic failure propagation.

MAINTENANCE AND MAINTAINABILITY

The 1617 is designed with sufficient tolerances that no adjustments are required to insure proper operation; therefore, the only unscheduled maintenance required in the field would be that necessitated by a component failure.

Interchangeability: Maintenance is enhanced by reduction of the types of spares required. Since the memory system is completely contained on one PC card and all PC cards are interchangeable without adjustment, only one type of spare is required.

Mean Time to Repair: The 1617 is designed with the objective of rapid fault isolation and repair. Through use of the manual trouble-shooting chart, it is possible to localize a fault to the defective component quickly and easily. Replacement of the defective component does not require any special tools or fixtures beyond a soldering iron and normal hand tools.

Spare Parts: The 1617 is designed to minimize the variety of unique components. Components readily available from distributors and multiple sources are used wherever possible.

APPENDIX

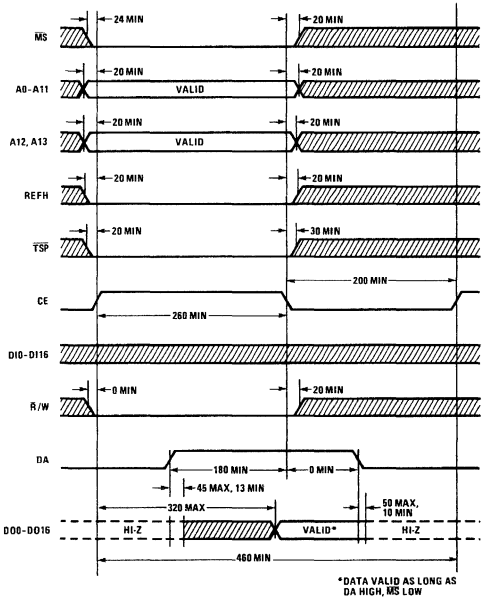


Figure 1. Read Cycle Timing

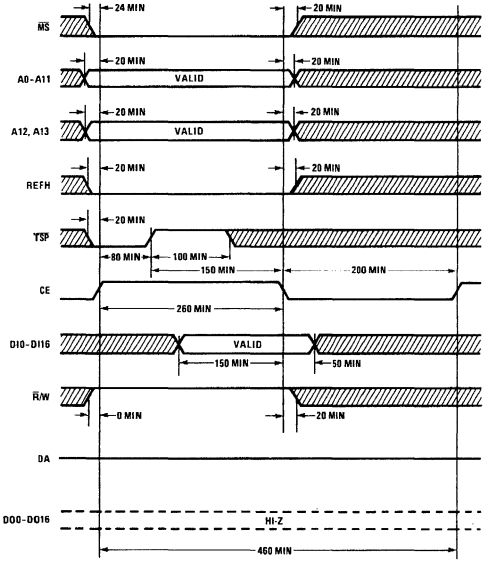


Figure 2. Write Cycle Timing

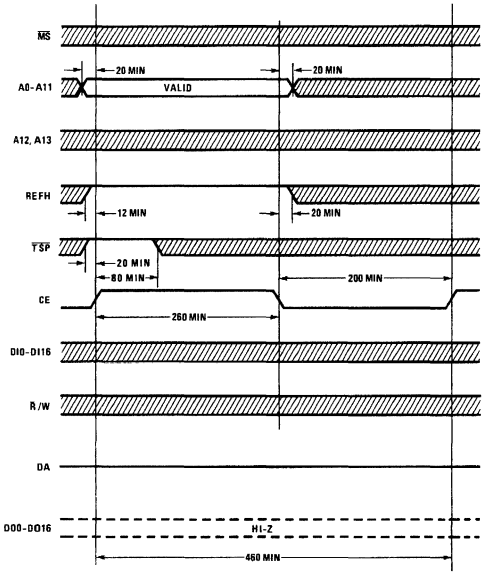


Figure 3. Refresh Cycle Timing

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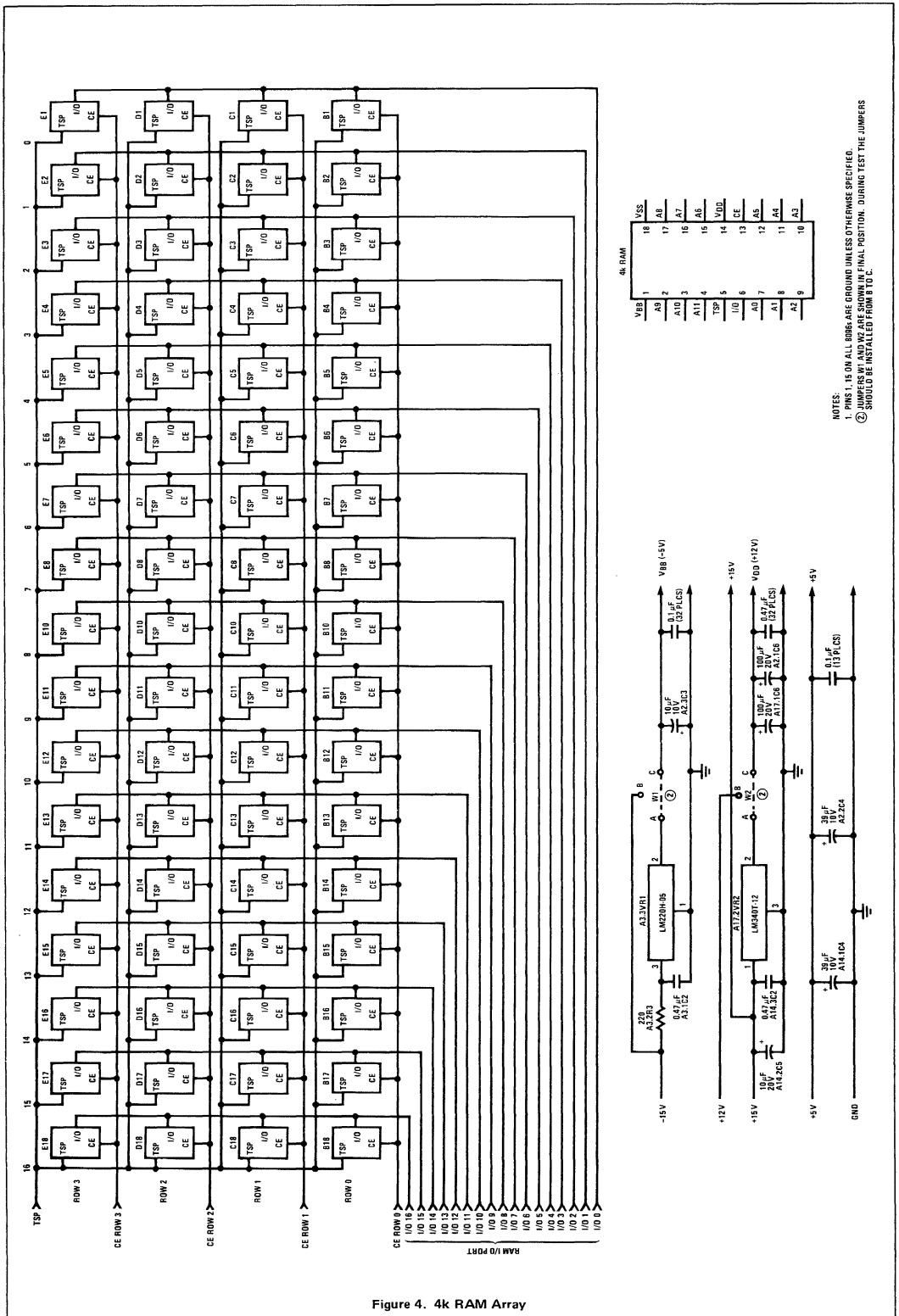

Figure 4. 4k RAM Array

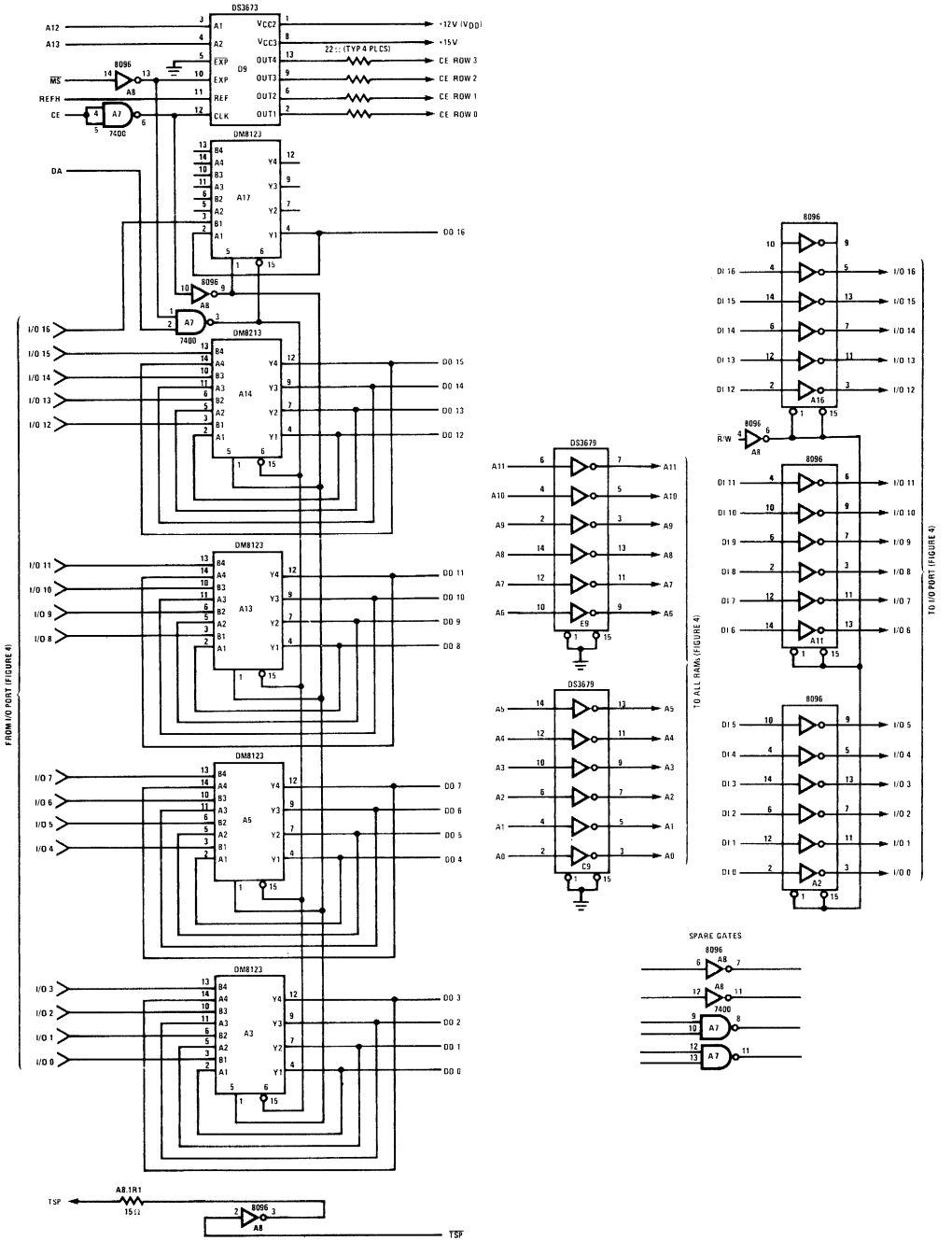

Figure 5. Interface Circuitry

Systems Application of MM5290 16K Dynamic RAM

SYSTEM DESCRIPTION

This section defines the functional capabilities of the NS340 Storage Card. The NS340 Storage Card contains a random-access semiconductor memory array utilizing the MM5290 16k dynamic RAM and appropriate drivers and receivers to permit data storage and retrieval. Proper DC power and I/O connections are required to operate the card.

Memory Configurations

The NS340 Storage Card has a maximum storage capacity of 131,072 (128k) words, each 22 bits long. Other permissible memory configurations are shown in table 1.

Table 1. Memory Configurations

Single Byte	Double Byte
256k x 8	128k x 16
256k x 9	128k x 18
256k x 10	128k x 20
256k x 11	128k x 22

Modes of Operation

The NS340 Storage Card has four basic modes of operation:

READ
WRITE
READ/DELAYED WRITE
REFRESH

The first three modes are concerned with data storage and retrieval. The last mode, REFRESH, is necessary to prevent loss of the data stored in the NMOS storage chips. NMOS Random Access Memory (RAM) devices store data as an electrical charge on the gate capacitance of a field-effect transistor. The stored charge tends to deteriorate and must be renewed at least every two milliseconds. Therefore, 1/128 of the memory (1/128 of each memory chip) is recharged (refreshed) every 15 microseconds. The seven low-order address bits determine the portion of memory to be refreshed.

Access and Cycle Times

The access and cycle times are listed below.

READ, WRITE, REFRESH cycles:
- Access Time 250 ns max
- Cycle Time 450 ns min

READ/DELAYED WRITE cycle:
- Access Time 250 ns max
- Cycle Time 500 ns min
  3450 ns max*

*READ/DELAYED WRITE timing includes processor modification if the READ/DELAYED WRITE is actually a READ/MODIFY/WRITE. A maximum modification time of 2.8 microseconds is allowed.

NOTE

Prior to performing any valid memory operations, the card must be initialized by executing a REFRESH cycle at each valid REFRESH address (128 cycles).

INTERFACE DESCRIPTION

Measurements

All timing measurements given above and in figures 1 through 4 are taken at the edge connectors of the NS340 Storage Card. Proper line termination, on both input and output lines, is assumed and signal timing measurements are referenced to the +1.5V level of the signal transition.

Input Definitions

Logic levels are defined as follows:

Logic HIGH +2.5V to +5V
Logic LOW 0V to +0.5V

SELECT (–SELECT 0, 1): The –SELECT 0 and –SELECT 1 signals enable the current memory operation to be performed on either or both of bytes 0 and 1. The –SELECT signals must be true 20 ns before t_0* and must remain true a minimum of 275 ns and a maximum of 10 μs after t_0 for a READ or WRITE cycle, and a minimum of 300 ns and a maximum of 10 μs after t_0 for a READ/DELAYED WRITE cycle.

*t_0 is defined as the starting time of the memory or REFRESH cycle at the NS340 Storage Card itself (i.e., the leading edge of –ADSTB).

ADDRESS (–ADD 00-16): All seventeen ADD lines are used to select the desired memory word during READ, WRITE, and READ/DELAYED WRITE cycles. The –ADD 00-06 lines select 1/128 of the memory during REFRESH cycles (see Refresh Control). The ADD lines must be stable a minimum of 20 ns before the leading edge of –ADSTB and must remain stable a minimum of 0 ns after the trailing edge of –ADSTB. However, it is desirable to keep the ADD lines stable until the trailing edge of –SELECT, as this helps reduce card noise to a minimum.

ADDRESS STROBE (–ADSTB): The ADDRESS STROBE signal is used to generate the internal row-address and column-address strobes for the 16k storage chips. The signal must be true at the start of the cycle (time t_0) and must remain true a minimum of 275 ns

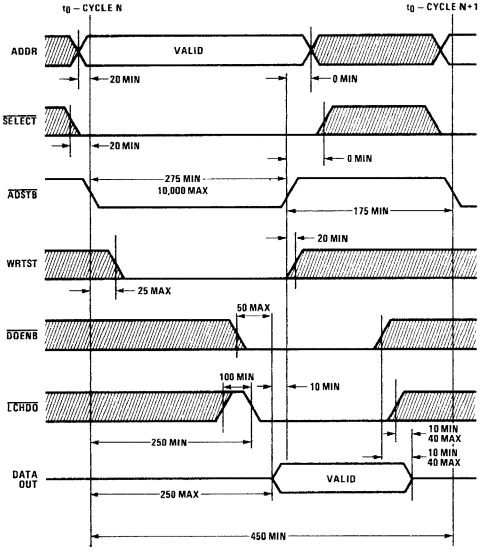

Figure 1. READ Cycle Timing
(times given in nanoseconds)

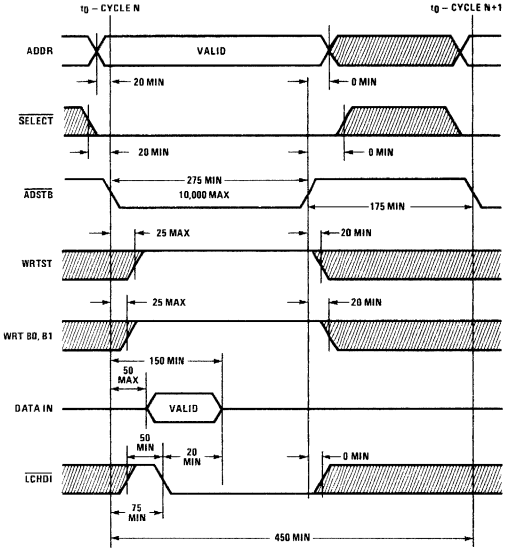

Figure 2. WRITE Cycle Timing
(times given in nanoseconds)

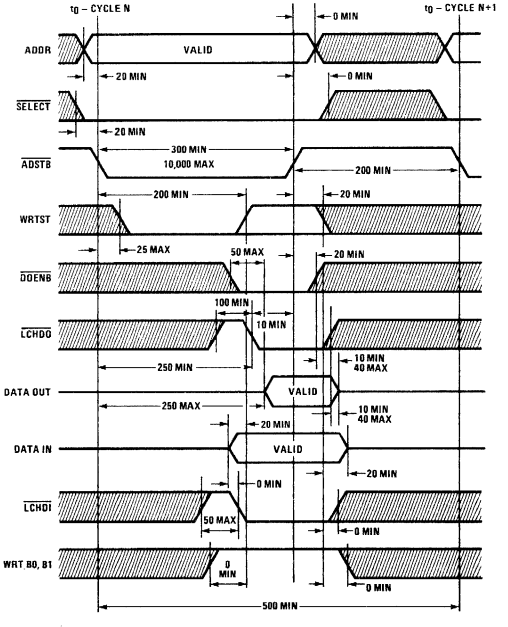

Figure 3. READ/DELAYED WRITE Cycle Timing
(times given in nanoseconds)

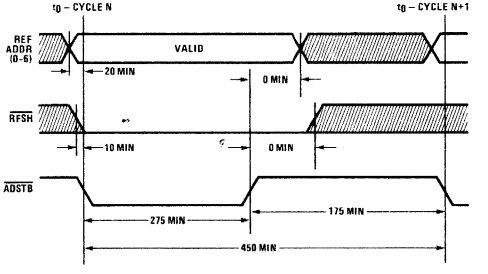

Figure 4. REFRESH Cycle Timing
(times given in nanoseconds)

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and a maximum of 10 μs for a READ or WRITE cycle, and a minimum of 300 ns and a maximum of 10 μs for a READ/DELAYED WRITE cycle.

DATA OUTPUT ENABLE (-DOENB): The 3647 TRI-STATE® I/O register chips receive data that is read from the memory chips, latch it, and send it to the host system. Since these chips may provide either a unidirectional or a bidirectional data interface, the -DOENB signal enables the chips to function in the proper direction (A-to-B) for output of data. -DOENB must go true 50 ns minimum before data out is to be valid.

LATCH DATA OUT (-LCHDO): Data read from the memory chips is latched into the 3647 output data register chips by -LCHDO. -LCHDO must be high for a minimum of 100 ns before its leading edge. The leading edge of -LCHDO occurs a minimum of 10 ns before the trailing edge of -ADSTB, and a minimum of 250 ns after t_0.

WRITE BYTE 0, 1 (+WRTB0, 1): The +WRTB0 and +WRTB1 signals control whether data is written into the byte 0 and/or byte 1 memory chips. Both of these signals are gated by +WRTST. Data is written into byte 0 (1) only if +WRTB0 (1) and -SELECT 0 (1) are both true.

WRITE STROBE (+WRTST): The +WRTST signal gates the +WRTB0 and +WRTB1 signals to the WRT inputs of all 16k memory chips. During a WRITE cycle +WRTST goes true a maximum of 25 ns after t_0 and remains true until a minimum of 20 ns after the trailing edge of -ADSTB. During a READ/DELAYED WRITE cycle, this signal must go low a maximum of 25 ns after t_0 and remain low a minimum of 200 ns after t_0. After this, the signal is allowed to go high for 100 ns minimum to gate the +WRT B0, B1 signals to the chips to perform the WRITE portion of the cycle.

DATA IN (-DIBY000-10, -DIBY100-10): Data to be stored into the memory is input via the DATA IN lines. During a WRITE cycle, input data must be valid no more than 50 ns after t_0 and remain valid at least until 150 ns after t_0. During a READ/DELAYED WRITE cycle, input data must be valid at least 20 ns before the positive-going edge of WRTST and remain valid at least until 20 ns after the trailing edge of -ADSTB.

LATCH DATA IN (-LCHDI): Data to be stored into the memory chips is latched into the input data register (3675 chips) by the -LCHDI signal. -LCHDI must be high for a minimum of 50 ns before its leading edge. The -LCHDI signal occurs a minimum of 75 ns after the leading edge of -ADSTB. -LCHDI cannot occur later than 20 ns before the input data is to be off of the bus.

REFRESH (-RFSH): The -RFSH signal performs the function of both -SELECT signals during a REFRESH cycle. -RFSH gates -ADD 00-06 to the memory chips, disables the column-address strobe, and provides a row-address strobe to each chip so that -ADD 00-06 may be latched into each chip's address register. -RFSH goes true a minimum of 10 ns before t_0 and must remain true a minimum of 275 ns and a maximum of 10 μs after t_0.

Output Definitions

The only output from the NS340 Storage Card is via the -DOBY0 and -DOBY1 (DATA OUT) lines. These lines are driven by 3647 TRI-STATE drivers, which can drive up to -5.2 mA in the high level and 100 mA in the low level. Data will be output from the -DOBY0 (byte 0) lines if -SELECT 0 and -DOENB are both true, and from the -DOBY1 (byte 1) lines if -SELECT 1 and -DOENB are both true.

OPTIONS

The NS340 Storage Card contains optional features that may be implemented by proper I/O connector wiring. The options are listed below.

External Column Address Strobe
Refresh Control:
  Burst Mode
  Distributed

These options are discussed in the following paragraphs.

External Column Address Strobe

A jumper option is provided on the card that allows the storage chips to use either the internal column address strobe signal generated from the -ADSTB signal (from the host system), or an external column address strobe supplied from the host system. If the external strobe (-CASTB) is used, it must go true a minimum of 75 ns after -ADSTB. -CASTB must be true for 180 ns minimum and 270 ns maximum.

The -CASTB signal *must* be used if it is desired to perform page-mode memory operations. A memory "page" consists of 1/128 of the memory as addressed by one row address (-ADD 00-06). If -ADD 00-06 are held constant, -ADD 07-13 may be cycled to perform the *same* type of memory operation at any or all locations of the memory "page." After the initial memory operation is performed, -CASTB goes high at 220 ns after the leading edge of -ADSTB. -CASTB then remains high for 60 ns, after which -CASTB again goes low for the next cycle. 20 ns before -CASTB goes low, the next column address must be stable on the -ADD 07-13 lines. This procedure may be repeated to cycle all address locations in the same memory "page."

Refresh Control

REFRESH cycles may be performed in either of two modes as described in the following paragraphs.

Burst Mode: Burst mode is intended for use in battery backup mode, but may also be implemented in normal mode. When this option is used, an external oscillator with a period of 2 ms must be used. At the start of every 2 ms period, a seven-bit REFRESH counter is initialized to zero. These 7 bits are used as address bits 0-6 to address 1/128 of the memory for refreshing. At the conclusion of each REFRESH cycle (450 ns), this counter is incremented and another REFRESH is *immediately* performed. This continues until 128 REFRESH cycles have been performed, and all of the memory is thus refreshed with a *burst* of 128 REFRESH cycles. Total time to refresh the entire memory is approximately 60 microseconds.

Distributed: This option is similar to burst mode, except that *one* REFRESH cycle is performed every 15 microseconds instead of 128 REFRESH cycles being performed consecutively at the start of a 2 ms period. This option requires an external oscillator with a period of 15 microseconds, and utilizes a seven-bit REFRESH

address counter as does burst mode. Now however, the REFRESH address counter is incremented at the end of each 15 microsecond oscillator period instead of at the end of each 450 ns REFRESH cycle.

POWER REQUIREMENTS

Parameters and Conditions

Three DC voltages are required to operate the NS340 Storage Card. These voltages and the current requirements are listed in this section.

Table 5 identifies the worst case power requirements of the NS340 Storage Card. The conditions and parameters used are defined as follows:

Standby	Quiescent mode with one REFRESH cycle every 15 μs.
Operating	450 ns cycle – continuous READ/WRITE memory operation, including REFRESH.
Typical	Nominal supply voltages.
Maximum	Worst case supply voltages.

Power Consumption

Table 5. Standard Power Consumption

Voltage	Operating		Standby (REFRESH only)	
	Typ	Max	Typ	Max
+12V	0.65 A	0.92 A	0.26 A	0.39 A
+5V	1.53 A	2.52 A	1.4 A	2.3 A
-5V	0.01 A	0.02 A	0.01 A	0.02 A

MECHANICAL DESCRIPTION

The physical and mechanical details of the NS340 are described in this section.

General

The NS340 Storage Card is completely contained on one multilayer printed circuit board (internal voltage and ground planes are used), which requires only the application of DC power to become functional.

Dimensions

Thickness	0.0625	inches
Height	11.75	inches
Length	15.40	inches

The NS340 Storage Card is designed to mount on a minimum center-to-center board spacing of 0.625". Two card ejectors (BIRTCHER 83-1-2 or equivalent) permit easy removal of the card.

Systems Application of MM74C929 CMOS RAM

SYSTEM DESCRIPTION

This section defines the functional capabilities of the NS400-CL and NS400-CC Storage Cards. The NS400-CL and NS400-CC Storage Cards each contain a static random-access semiconductor memory array and appropriate drivers and receivers to permit data storage and retrieval. Proper DC power and I/O connections are required to operate the cards.

The NS400-CL and NS400-CC Storage Cards both utilize the MM74C929 CMOS storage device to form 4kx8, 4kx9, or 4kx10 memory arrays. However, the NS400-CL Storage Card uses CMOS logic for its array and TTL for its I/O interface, whereas the NS400-CC Storage Card uses CMOS logic for its array and I/O interface. The NS400-CL Storage Card requires a supply voltage of +5.0V ± 5%. The NS400-CC, however, can operate with any V_{CC} voltage within the range of 3.5V through 5.5V. An increase in V_{CC} will result in a decrease in access time. Figure 2 shows a graph of access time versus V_{CC} voltage for the NS400-CC Storage Card.

Because the NS400-CC can operate at a lower V_{CC} voltage, the card is more suitable in applications where V_{CC} is supplied from a battery. This is discussed later.

MODES OF OPERATION

The NS400-C Storage Cards have two basic modes of operation: READ and WRITE. These two modes of operation permit data storage into and data retrieval from the memory array. Although the Storage Cards are not designed to perform a dedicated READ/MODIFY/WRITE cycle, such a cycle may be performed under user control as a separate READ cycle and WRITE cycle, with time allowed between the two cycles to allow data modification.

ACCESS AND CYCLE TIMES

The access and cycle times are as follows:

Storage Card Type	Read Access Time	Read or Write Cycle Time
NS400-CL (V_{CC} = +5.0V ± 5%)	400 ns max	500 ns
NS-410-CC (V_{CC} = +5.0V ± 5%)	575 ns max (25 pF data bus) 700 ns max (150pF data bus)	700 ns
NS400-CC (V_{CC} = +3.5V - +5.5V)	500 ns - 900 ns* (25 pF data bus) 600 ns - 1100 ns* (150pF data bus)	1100 ns

*For access time for any given supply voltage on the NS400-CC Storage Card, consult figure 2.

INTERFACE DESCRIPTION

The following paragraphs describe the interface to the NS400-C Storage Cards.

MEASUREMENTS

All timing measurements are taken at the edge connectors of the Storage Card. Proper line termination, on both input and output lines, is assumed. Signal timing measurements for the TTL logic are referenced to the +1.5V level of the signal transition.

INPUT DEFINITIONS

Logic Levels are defined as follows:

	NS400-CL	NS400-CC (+5V)	NS400-CC (3.5V)
Logic 1 = HIGH	+2.5V to +5.0V	+3.5V to +5.0V	+3.0V to +3.5V
Logic 0 = LOW	0V to +0.5V	0V to +1.5V	0V to +0.5V

Table I. Input Loading by Component Type

Component	NS400-CL		NS400-CC	
	Logic 1	Logic 0	Logic 1	Logic 0
8097/80C97	40 μA	1.6 mA	0.005 μA	0.005 μA
74LS42/74C42	20 μA	0.4 mA	1 μA	1 μA
74L86/74C86	20 μA	0.36 mA	0.005 μA	0.005 μA
74L20/74C20	20 μA	0.36 mA	0.005 μA	0.005 μA

Table 2. Input Loading by Signal Name

Signal	NS400-CL		NS400-CC	
	Logic 1	Logic 0	Logic 1	Logic 0
A0-A9	40 μA	1.6 mA	0.005 μA	0.005 μA
DI0-DI9	40 μA	1.6 mA	0.005 μA	0.005 μA
A10, A11	20 μA	0.4 mA	1 μA	1 μA
MEM EN	20 μA	0.36 mA	0.005 μA	0.005 μA
A12, A13, A14	20 μA	0.36 mA	0.005 μA	0.005 μA
S12, S13, S14	20 μA	0.36 mA	0.005 μA	0.005 μA
R/W	20 μA	0.36 mA	0.005 μA	0.005 μA

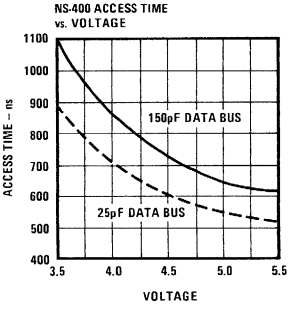


Figure 1. NS400 Access Time vs Voltage

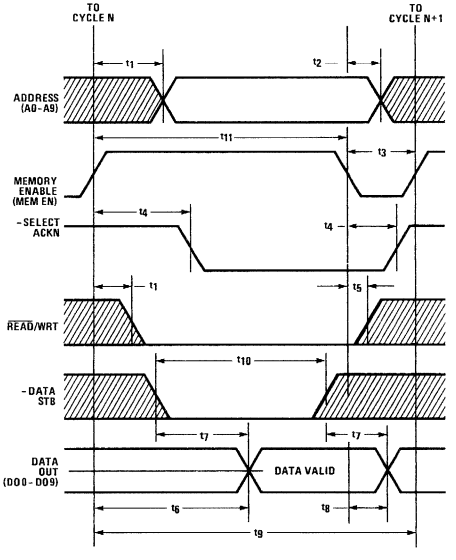


Figure 2. Read Cycle Timing

Table for Figure 2
Card Types

Time	NS400-CL	NS400-CC Fixed	NS400-CC Variable
t_1	0 ns max	70 ns max	70 ns max
t_2	0 ns min	0 ns min	100 ns min
t_3	250 ns min	350 ns min	500 ns min
t_4	62 ns min	130 ns min	130 ns min
t_5	100 ns min	350 ns min	600 ns min
t_6	400 ns max	575 ns max (25 pF) 700 ns max (150 pF)	consult figure 2
t_7	25 ns min	50 ns min	100 ns min
t_8	50 ns max	2 μs max	2 μs max
t_9	500 ns max	700 ns max	1100 ns max
t_{10}	200 ns min	300 ns min	400 ns min
t_{11}	250 ns min	350 ns min	600 ns min

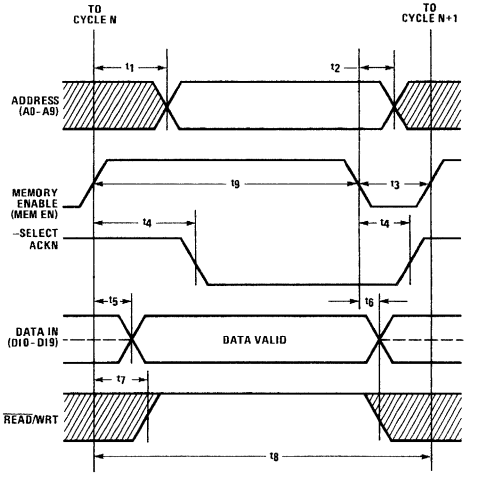


Figure 3. Write Cycle Timing

Table for Figure 3
Card Types

Time	NS400-CL	NS400-CC Fixed	NS400-CC Variable
t_1	0 ns max	70 ns max	70 ns max
t_2	0 ns min	0 ns min	100 ns min
t_3	250 ns min	350 ns min	500 ns min
t_4	60 ns min	130 ns min	130 ns min
t_5	75 ns max	100 ns max	100 ns max
t_6	100 ns min	350 ns min	600 ns min
t_7	0 ns max	100 ns max	100 ns max
t_8	500 ns max	700 ns max	1100 ns max
t_9	250 ns min	350 ns min	600 ns min

MEMORY ENABLE (MEM EN)

MEMORY ENABLE, in conjunction with ADDRESS IN lines A12-A14 and SELECT ADDRESS IN lines S12-S14, enables selection of the memory devices on the Storage Card. When the card is selected, - SELECT ACKN is driven active. MEMORY ENABLE must be activated at t_0 and remain active for a minimum of 250 ns for the NS400-CL version, 350 ns for the fixed V_{CC} NS400-CC version, and 600 ns for the variable V_{CC} NS400-CC version.

ADDRESS IN (A0-A14)

The fifteen ADDRESS IN lines are used as follows during both READ and WRITE memory cycles:

A12-A14 select 1 of up to 8 Storage Cards.

A10, A11 select one of the four 1k columns of memory devices on the Storage Card.

A0-A9 select one of the 8-, 9-, or 10-bit words in the selected memory device column of the selected Storage Card.

On the NS400-CL Storage Card, the ADDRESS IN lines must be stable no later than t_0 and remain stable for the duration of MEM EN (memory enable). On the NS400-CC Storage Card, the ADDRESS IN lines must be stable not later than 100 ns after t_0. The ADDRESS lines must remain stable for the duration of MEM EN for fixed V_{CC} operation, or for a minimum of 100 ns after the trailing edge of MEM EN for variable V_{CC} operation.

SELECT ADDRESS IN (S12-S14)

The three SELECT ADDRESS IN lines assign the Storage Card to one of eight address ranges (one of 000_2-111_2). If ADDRESS IN lines A12-A14 respectively mismatch the SELECT ADDRESS IN lines, the Storage Card is selected if MEM EN is active. The address range assignment and card selection are explained in detail later.

DATA IN (DI0-DI9)

Data to be stored into the memory array enters via the DI0-DI9 lines, and must be stable not later than 75 ns after t_0 for the NS400-CL card or 100 ns after t_0 for the NS400-CC card. For the NS400-CL card, data must be stable for at least 100 ns after the trailing edge of MEM EN. For the NS400-CC card, data must be stable for at least 350 ns after the trailing edge of MEM EN for fixed V_{CC} (+5.0 V) operation, or for at least 600 ns after the trailing edge of MEM EN for variable V_{CC} (+3.5 V-+5.5 V) operation.

READ/WRITE (R/W)

The R/W signal controls the type of cycle to be performed. R/W must be LOW for a READ cycle and HIGH for a WRITE cycle. R/W must be stable at t_0 for the NS400-CL card and be stable at a maximum of 100 ns after t_0 for the NS400-CC card.

The R/W signal must remain stable until after the trailing edge of MEM EN: 100 ns minimum after the trailing edge of MEM EN for the NS400-CL card, 350 ns minimum after MEM EN for the NS400-CC card with fixed V_{CC} operation, and 600 ns minimum after MEM EN for the NS400-CC card with variable V_{CC} operation.

DATA STROBE (- DATA STB)

The DATA STROBE signal gates data read from the memory array onto the DO (data out) lines. It must be activated a minimum of 100 ns before it is desired for data to be valid on the DO lines.

OUTPUT DEFINITIONS

The NS400-CL and NS400-CC Storage Cards output - SELECT ACKN during a WRITE cycle and Data Out during a READ cycle. The output lines are defined in the following paragraphs, and output drive is shown in tables 3 and 4.

Table 3. Output Drive by Component Type

Component	NS400-CL		NS400-CC	
	Logic 1	Logic 0	Logic 1	Logic 0
8097/80C97	5.2 mA	32 mA	4.35 mA	4.35 mA
74L20/74C20	200 μA	3.6 mA	1.75 mA	1.75 mA

Table 4. Output Drive by Signal Name

Signal	NS400-CL		NS400-CC	
	Logic 1	Logic 0	Logic 1	Logic 0
DO0-DO9	5.2 mA	32 mA	4.35 mA	4.35 mA
SELECT ACKN	200 μA	3.6 mA	1.75 mA	1.75 mA

ACKNOWLEDGE (- SELECT ACKN)

The selected Storage Card generates - SELECT ACKN in response to the correct ADDRESS IN (A12-A14) and MEM EN. On the NS400-CL card, - SELECT ACKN goes active a minimum of 60 ns after t_0 and remains active until 60 ns after the trailing edge of both the ADDRESS IN lines and MEM EN. On the NS400-CC card, the minimum time is 130 ns in both cases instead of 60 ns. - SELECT ACKN may be jumpered to - DATA STB to provide an instantaneous data strobe. Loading and capacitance should be kept to a minimum on the - SELECT ACKN line.

DATA OUT (DO0-DO9)

Data read from the memory array during a READ cycle is placed on the DO lines when - DATA STB is active. Data is valid on the DO lines a maximum of 400 ns after t_0 (NS400-CL) or 575 ns to 700 ns after t_0 (NS400-CC card with fixed V_{CC} operation). The time when data is valid for an NS-400-CC card with variable V_{CC} operation may be determined by consulting figure 1.

INTERFACE SIGNAL LIST

Table 5 lists the I/O connector signal pin assignments. The table lists by pin number, signal function (including options available), and a mnemonic of each signal.

OPTIONS

The NS400-CL and NS400-CC Storage Cards contain optional features that enable the cards to be used in a variety of applications. The options are listed below:

- TTL or CMOS interface
- Variable Access — NS400-CC Storage Card
- Delayed Data Strobe
- Address Range Assignment
- Storage Card Depopulation

These options are discussed in the following paragraphs.

TTL OR CMOS INTERFACE

As mentioned throughout this specification, there are two types of NS400-C Storage Cards: the NS400-CL and the NS400-CC. Each card utilizes the MM74C929 storage device for its memory array. However, the NS400-CL card uses TTL drivers and receivers and a TTL card-selection logic network, while the NS400-CC card uses CMOS drivers and receivers and a CMOS card-selection logic network. The NS400-CL card, although low power, requires a fixed V_{CC} of +5.0 V. The NS400-CC card can operate with any V_{CC} from +3.5 V to +5.5 V. This is useful in applications where V_{CC} must be obtained from a low voltage battery, or when operating the card in certain heavy industrial areas where brown-outs are quite common and a +5.0 V supply operating from the AC line may put out a substantially lower voltage than +5.0 V due to the reduced AC input voltage.

VARIABLE ACCESS – NS400-CC CARD

The NS400-CC Storage Card, as discussed previously, operates with any V_{CC} from +3.5V to +5.5V. Figure 1 shows V_{CC} voltage versus access time. Note that a higher V_{CC} results in a shorter access time and hence a shorter cycle time, whereas a lower V_{CC} results in a longer access time and hence a longer cycle time. Varying V_{CC} from 3.5V to 5.5V changes the access time from a low of 500ns to a high of 900ns with a 25pF data bus, or from a low of 600ns to a high of 1100ns with a 150pF data bus.

DELAYED DATA STROBE

Both Storage Cards allow instantaneous or delayed strobing out of data read from the memory array. In many applications, – SELECT ACKN is jumpered to – DATA STB. As soon as the card is selected, – SELECT ACKN becomes active, and in turn activates – DATA STB to permit instantaneous strobing of data to the interface.

Data strobe can, however, be controlled externally after the receipt of an acknowledge or the strobe can be tied LOW for a constant enable.

ADDRESS RANGE ASSIGNMENT

Several Storage Cards may be used to form a memory system. Cards may be connected in series to increase word length and/or cards may be connected in parallel to increase storage capacity.

When connecting cards in parallel, only *one* card must output a particular 10-bit word, while all other cards remain disabled. For this reason the card provides three normally HIGH address-bit-select lines, called S12, S13, and S14. S12, S13, and S14 can specify any one of eight binary numbers.

A card is assigned a binary number by jumpering the correct ones of S12, S13, and S14 to ground. When an address enters the card, S12, S13, and S14 are compared on a respective one-to-one basis with address input bits A12, A13, and A14. If all corresponding bits of both sets of address bits mismatch, the card will be selected if MEM EN is active.

Table 6 shows the jumpering required for S12, S13, and S14 to assign a card to one of the eight address ranges:

Table 6. Address Range Assignment

Address Range Assignment	S14	S13	S12
28k-32k	X	X	X
24k-28k	X	X	
20k-24k	X		X
16k-20k	X		
12k-16k		X	X
8k-12k		X	
4k-8k			X
0-4k			

Note: X indicates a jumper to ground.

STORAGE CARD DEPOPULATION

The NS400-C Storage Cards may each provide 4kx8, 4kx9, or 4kx10 storage. The card must be fully populated to provide 4kx10 storage. To provide 4kx8 or 4kx9 storage, chips need not be present in rows K and L, or row L, respectively.

POWER REQUIREMENTS

Proper V_{CC} voltage levels and current requirements for the NS400-C Storage Cards are listed in tables 7 and 8, which identify the worst case power requirements of each Storage Card. The conditions and parameters are defined as follows:

Standby	Quiescent mode – memory enable low I/O. Pins 14, 17, 22, and 27 HIGH.
Operating	Continuous READ and WRITE cycle memory operation.
Typical	Nominal supply voltages.
Max	Worst case supply voltages.

POWER REQUIREMENTS FOR NS400-CL

One +5V supply is required to operate the NS400-CL Storage Card. Table 7 identifies the worst case power requirements of this card.

Table 7. NS400-CL Power Consumption

Voltage/Mode	Typical	Maximum
+4.75V Standby/ Operating	250mA 310mA	300mA 370mA
+5.25V Standby/ Operating	280mA 350mA	345mA 420mA

POWER REQUIREMENTS FOR NS400-CC

The NS400-CC Storage Card may be operated with any V_{CC} voltage from 3.5V to 5.5V, including a low voltage battery. Table 8 identifies the worst case power requirements of this card.

Table 8. NS400-CC Power Consumption

V_{CC} Voltage/Mode	Typical	Maximum
3.5V Standby 1100ns Operating	23μA 34mA	28μA 41mA
4.75V Standby 1100ns Operating 700ns Operating	30μA 54mA 72mA	36μA 65mA 87mA
5.25V Standby 1100ns Operating 700ns Operating	55μA 62mA 84mA	66μA 74mA 101mA
5.5V Standby 1100ns Operating	200μA 67mA	240μA 80mA

POWER-UP CONSIDERATIONS

Memory enable (MEM EN) must be held LOW during power-up to prevent memory device latch-up.

MECHANICAL DESCRIPTION

Both NS400-C Storage Cards are fabricated with two-sided printed circuit boards and require only the application of DC power to become functional.

DIMENSIONS

Thickness. . . . . 0.062"
Height. . . . . 3.93"
Length . . . . . 6.3"

The cards are designed to mount on a minimum center-to-center board spacing of 0.0625". No ejectors are present on the card.

I/O CONNECTORS

One 60-pin edge-type I/O connector provides an interface to the NS400-CL or NS400-CC Storage Card. The spacing of these connector fingers is 0.125", center-to-center. The material is gold over copper. The recommended mating connector is an ELCO 00-6307-060-309-001 or equivalent.

ENVIRONMENTAL DESCRIPTION

The Storage Cards are designed to operate over a variety of environmental conditions.

Operational environmental limits are defined below:

Temperature

Ambient air temperature range is 10°C to 50°C.

Thermal Shock

Both NS400-C Storage Cards can withstand a thermal shock with a maximum rate of change of 30°C per hour during operation.

Humidity

The Storage Cards have been designed to operate in a relative humidity of up to 95% (without condensation).

Altitude

This system is capable of operation at altitudes from -1,000 feet MSL to +10,000 feet MSL.

Cooling

Suggested minimum air flow for the NS400-CL and NS400-CC Storage Cards is 15 cfm and 10 cfm respectively.

SHIPPING AND STORAGE CONDITIONS

Non-operational environmental limits are detailed as follows:

Temperature

The NS400-C Storage Cards can withstand a temperature range of −40°C to +85°C during shipment or storage.

Thermal Shock

A thermal rate of change as high as 10°C per minute can be tolerated.

Altitude

The maximum shipping altitude is 40,000 feet.

Mechanical Shock

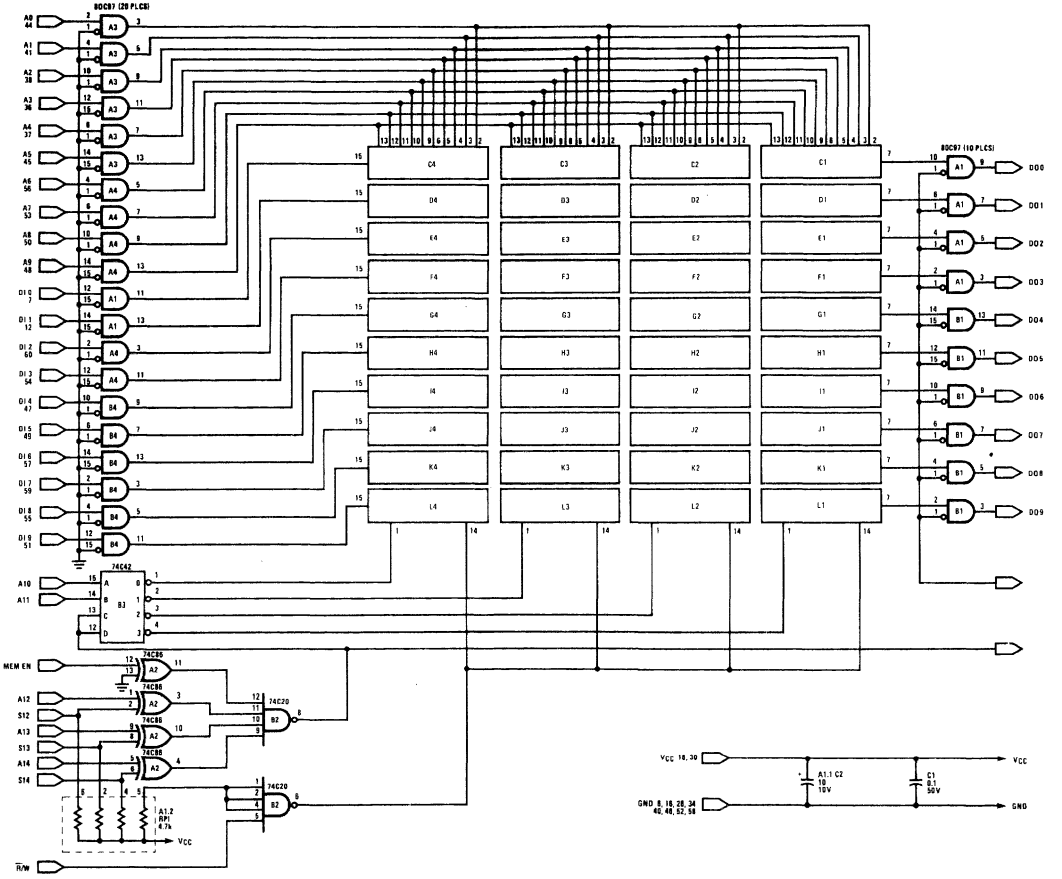
The Storage Cards, each housed in its shipping container, can tolerate mechanical shock resulting from drop tests performed in accordance with MIL-STD-810B, Method 516, Procedure V, without exhibiting damage or degradation.

RELIABILITY AND MAINTENANCE

The Storage Cards were designed to provide high reliability of operation and rapid corrective maintenance in case of component failure.

RELIABILITY

The cards were designed to the best commercial standards of workmanship, and a high degree of testing was conducted (including tests over operating temperature range) to insure a reliable service of ten years at twenty-four hours a day usage (exclusive of routine maintenance time). The design is such that catastrophic failure occurrence is minimized and minimal propagation of such failure will be experienced.



NOTES:

1. ALL RESISTOR PACKS ARE IN OHMS, ±5%, 1/8 W.
2. ALL CAPACITOR VALUES ARE IN MICROFARADS.
3. ICs DESIGNATED C1-C4, D1-D4, E1-E4, F1-F4, G1-G4, H1-H4, I1-I4, J1-J4, K1-K4, L1-L4 ARE ALL TYPE MM74C929. TYPICAL PINOUT CONFIGURATION IS AS SHOWN BELOW.

TYPICAL MM74C929
PINOUT CONFIGURATION

1	$\overline{CS}$	V_{CC}	16
2	A0	DI	15
3	A1	$\overline{WE}$	14
4	A2	A9	13
5	A3	A8	12
6	A4	A7	11
7	DO	A6	10
8	GND	A5	9

4. IC VOLTAGE AND GND PINS ARE AS FOLLOWS:
   A1, A3, A4, B1, B3, AND B4
   GROUND PIN 8, V_{CC} PIN 16. A2, B2
   GROUND PIN 7, V_{CC} PIN 14.
5. IC LOCATION DESIGNATION USED:

Figure 6. NS400-CC Logic Diagram

Section 11

Reliability

11

National consistently maintains tighter quality levels than the industry for standard commercial products. If you should decide that you need extraordinary reliability levels, still tighter guarantees are available from National through the B+, the A+, and the MICRO+ programs which are explained in brochures available through your local National Field Sales Representative.

National's Reliability Programs

OVERVIEW

The Microcircuits Reliability Assurance Department routinely conducts a number of large-scale programs which generate reliability data on National's products. These programs include:

- Product reliability audits
- New-product qualification tests
- New-process qualification tests
- Customer-funded qualification programs
- Engineering investigations

Our Product Reliability Engineers and Failure Analysis Engineers also work directly with many customers in assisting their Component Reliability people in the performance of reliability studies.

LIFE TEST DATA

Most of the reports generated by these reliability programs are proprietary to National or National's customers. However, we frequently do extract data for uncontrolled circulation. Copies of these "declassified" reports are maintained on file in Reliability Assurance. On special request, we can assemble generic life test data on virtually every device manufactured by National.

RELIABILITY BRIEFS

Reliability Assurance regularly publishes brief items of current interest. These Reliability Briefs are distributed to all National sales offices when they are first issued. Additional copies are available upon request.

SPECIAL REPORTS

From time to time, Reliability Assurance also publishes "tutorial" reports. These reports are intended to give users of National's microcircuits better insight into the subject of IC reliability.

PACKAGE RELIABILITY

Package integrity remains the single largest stumbling block to IC reliability. National has achieved a position of leadership in package reliability. We maintain this position with a heavy commitment to package-oriented reliability studies. Much of this data has been "declassified" and compiled into reports suitable for general circulation.

HOW TO OBTAIN REPORTS

The following lists those reports and other literature currently available from the Microcircuit Reliability Assurance Department. To obtain copies, call (408) 737-6686 or write to:

Reliability Assurance, M/S 320
National Semiconductor Corporation
2900 Semiconductor Drive
Santa Clara, CA 95051

NATIONAL RELIABILITY REPORT LISTING

• Reliability Briefs	Brief No.
Anti-Static Rails	2
Ultrasonic Cleaning	5
All That Glitters Is Not Gold	18
Epoxy B Flammability	23
Microcircuit Failure Analysis Requests	24

• Other General Reliability Publications	Report No.
The A+ Reliability Program brochure	
The B+ Reliability Program brochure	
The MICRO+ Reliability Program brochure	
Semiconductor Device Reliability and the Arrhenius Model (A primer on reliability nomenclature and temperature acceleration factor)	G-11
Microcircuit Failure Analysis Program	G-19
Epoxy B and the Quiet Revolution	G-21
National Epoxy B (The Epoxy B Story)	———
The Automotive Environment: The Ultimate Challenge (A cost effective approach to reliability)	G-22

NATIONAL RELIABILITY REPORT LISTING (continued)

Device		Package	Report No.
• **Life Test Reports on Linear ICs**			
ALIC			
LF311H	Voltage Comparator	H	L-117
LM104	Voltage Regulator	H	L-98A
LM104H	Voltage Regulator	H	L-100
LM108	Op Amp	H	L-96A
LM109	Voltage Regulator	K	L-92A
LM118	Op Amp	H	L-105
LM121H	Precision Preamplifier	H	L-115
LM308	Op Amp	N	L-102
LM308	Op Amp	H	L-86A
LM311D	Voltage Comparator/Buffer	D	L-91A
LM318	Op Amp	N	L-106
CLIC			
LM239D	Voltage Comparator	D	L-104
LM324J	Quad Op Amp	J	L-111
LM324N	Quad Op Amp	N	L-109
LM324N	Quad Op Amp	N	L-110
LM339N	Quad Comparator	N	L-128
LM358	Quad Op Amp	H	L-101
LM373	Amplifier/Detector	N	L-136
LM380	Audio Power Amplifier	N	L-119
LM381N	Low Noise Dual Preamplifier	N	L-125
LM390	Audio Power Amplifier	N	L-134
LM1821	TV Video Detector	N	L-123
LM1887N	Chroma Subcarrier Regenerator	N	L-116
LM1901D	Quad Comparator	N	L-112
LM2887	Chroma Subcarrier Regenerator	N	L-130
LM2900, LM3900	Quad Amplifier	N	L-118
SLIC			
LF356	Op Amp	H, N, J	L-127
LM78L05	Three-Terminal Positive Voltage Regulator	P	L-122
LM105	Voltage Regulator	P	L-90
LM105H	Voltage Regulator	H	L-99
LM301A	Op Amp	N	L-88
LM301A (E)	Op Amp	H	L-93
LM301AH, LM741H	Op Amp	H	L-114
LM307	Op Amp	N	L-87
LM340T	Voltage Regulator	T	L-103
LM340T	Three-Terminal Positive Voltage Regulator	T	L-126
LM341-5	Three-Terminal Voltage Regulator	P	L-131
LM375N	Oscillator and Buffer	N	L-133
LM555H	Timer	H	L-129
LM723	Voltage Regulator	D	L-97
LM723	Voltage Regulator	H	L-137
LM741	Op Amp	H	L-107
LM741J	Op Amp	J	L-124
LM741C	Op Amp	N	L-85
LM741C	Op Amp	N	L-89
LM1496N	Modulator-Demodulator	N	L-132
LM3046	Transistor Array	N	L-120
LM4250	Programmable Op Amp	N	L-121

(continued)

Device		Package	Report No.
• Life Test Reports on Memories			
DM74S287, DM74S387	Titanium-Tungsten Schottky Bipolar PROMs	N	M-4
DM7588N	256-Bit Programmable ROM	N	D-72
MM1702A	Electrically Reprogrammable ROM	Q	M-1
MM2102	N-Channel Silicon Gate 1024-Bit Static RAM	J, D, N	M-2
MM2708	8k UV Erasable PROM	Q	M-5
MM5203Q	2k Static EPROM	Q	M-41
MM5280D	N-Channel Silicon Gate 4096-Bit Dynamic RAM	D	M-3
MM5280J	N-Channel Silicon Gate 4096-Bit Dynamic RAM in CERDIP	J	M-6
MM5270, MM5280	Reliability Report on the 4k Dynamic RAM		———
• Life Test Reports on CMOS Logic ICs			
74C and 4000 series — CMOS Logic in CERDIP		J	C-9
54C and 4000 series — CMOS Logic in Hermetic DIP		D	C-10
74C and 4000 series — CMOS Logic in Epoxy B Package		N	C-11
• Life Test Reports on TTL ICs			
DM74L95N	Shift Register	N	D-80
DM74S30	Eight-Input Positive NAND Gate	N	D-74
DM5400J	Quad Two-Input NAND Gate	D	D-76
DM7400	Quad Two-Input NAND Gate	N	D-82
DM54LS00J, DM74LS00N	Quad Two-Input NAND Gate	N, J	D-73
DM7093N	TRI-STATE Quad Buffer	N	D-78
DM7406	Hex-Inverter Buffer/Driver	N	D-81
DM7563	Counter	N	D-83
• Life Test Reports on Interface ICs			
DM7880	Decoder/Driver	J, N	D-79
• Life Test Reports on Microprocessor ICs			
INS8080A, SC/MP	N-Channel Microprocessor	D, N	RM-14

- **Package Reliability Reports**

Package	Subject	Report No.
CERDIP	National Semiconductor Ceramic Dual-In-Line Package Reliability Report	G-17
EPOXY B	The Reliability of Epoxy B in Accelerated Temperature and Humidity Environments	G-18
Hermetic DIP	The Effects of High Humidity and Bias on Hermetic Dual-In-Line Package	G-20
Epoxy B (TO-220)	Power Cycle	L-103
Epoxy B	Temperature and Humidity, Pressure Pot, Temperature Cycle, Thermal Shock	L-108
TO-5	Temperature Cycle, Thermal Shock	L-114
Epoxy B	Temperature and Humidity	L-116
Epoxy B	Temperature Cycle	L-118
Epoxy B	Temperature Cycle	L-119
Epoxy B (TO-92)	Power Cycle	L-122
Epoxy B	Thermal Shock, Temperature Cycle, Pressure Pot	L-123
CERDIP	Thermal Shock, Temperature Cycle	L-124
Epoxy B (TO-220)	Thermal Shock, Pressure Pot, Power Cycle	L-126
TO-5, CERDIP, Epoxy B	Thermal Shock, Temperature and Humidity	L-127
Epoxy B	Temperature Cycle	L-128
Epoxy B (TO-126)	Temperature and Humidity, Pressure Pot, Power Cycle, Temperature Cycle, Thermal Shock, Solderability	L-131
Epoxy B	Temperature and Humidity	L-132
Epoxy B	Temperature and Humidity	L-133
Epoxy B	Temperature and Humidity	L-134
Epoxy B	Temperature and Humidity	L-136
Quartz-Lid DIP	Temperature Cycle, Thermal Shock	M-1
Epoxy B Hermetic	Temperature Cycle, Temperature and Humidity, Thermal Shock, Solderability, Lead Integrity	M-2
Hermetic	Thermal Shock, Temperature Cycle	M-3
Epoxy B Hermetic	Temperature Cycle, Thermal Shock, Solderability, Lead Integrity	M-4
CERDIP	Thermal Shock, Temperature Cycle, Mechanical Shock, Vibration	M-6
Hermetic Epoxy B	Temperature Cycle	RM-14
CERDIP	Temperature Cycle, Thermal Chock, Acceleration, Mechanical Shock, Solderability, Moisture Resistance, High Temperature Storage	C-9
Epoxy B	Temperature Cycle, Thermal Shock, Pressure Pot, Moisture Resistance	C-11
CERDIP Epoxy B	Temperature and Humidity, Pressure Pot, Temperature Cycle, Power Cycle	D-73
Epoxy B	Pressure Pot, Temperature Cycle, Power Cycle	D-74
CERDIP Epoxy B	Temperature and Humidity	D-79
Epoxy B	Temperature and Humidity, Temperature Cycle	D-80
Epoxy B	Temperature and Humidity, Pressure Pot, Temperature Cycle	D-81
Epoxy B	Temperature and Humidity, Pressure Pot, Temperature Cycle	D-82
Epoxy B	Temperature and Humidity, Temperature Cycle, Pressure Pot	D-83

Section 12

Definitions and Standards

12

Standardization of terms used in memory specifications is essential. Excerpts of IEEE proposed standards are presented here for future reference. A short list of acronyms is also included in this section.

Definitions of Frequently-Used Acronyms

ACE	Asynchronous Communications Element (INS8250)
ASCII	American Standard Code for Information Interchange
BCD	Binary Coded Decimal
BPNF	Begin/Positive/Negative/Finish
BRK	Break
CAS	Column Address Strobe
CCD	Charge Coupled Device
CE	Chip Enable
CERDIP	Ceramic Dual-In-Line Package
CFM	Cubic Feet per Minute
CMOS	Complementary Metal Oxide Semiconductor
CPU	Central Processing Unit
CRT	Cathode Ray Tube
CRTC	CRT Controller (DP8350)
CS	Chip Select
DED	Darkness Emitting Diode
DI	Data Input
DMA	Direct Memory Access
DO	Data Output
EPROM	Erasable Programmable Read Only Memory
I^2L	Integrated Injection Logic
I/O	Input/Output
LCDS	Low Cost Development System
LED	Light Emitting Diode
LSB	Least Significant Bit
LSI	Large Scale Integration
MOS	Metal Oxide Semiconductor
MPS	Mask Programming System
MSB	Most Significant Bit
MSI	Medium Scale Integration
MSL	Mean Sea Level
NSC	Memory Support for you
OE	Output Enable
PC	Printed Circuit
PROM	Programmable Read Only Memory
RAM	Random Access Memory
RAS	Row Address Strobe
RMW	Read/Modify/Write
ROM	Read Only Memory
R/W	Read/Write
RWM	Read/Write Memory
SE	Sense Enable
TSP	Tri-Share Port
TTL	Transistor - Transistor - Logic
WE	Write Enable

Excerpts from the Proposed IEEE Standard for Semiconductor Memory Data Sheet Generation*

Table of Contents

*The material in this section was excerpted from a document prepared by the IEEE Task Force, P662, on Semiconductor Memory Terminology and Specifications in cooperation with JEDEC JC-42 committee on Semiconductor Memories 11/16/77.

Introduction

The purpose of this standard is to provide guidelines under which data sheets for new semiconductor memories are to be generated. Following these standards should produce data sheets that are concise and that consistently define the operation and characteristics of semiconductor memory devices.

Product Description

Product description consists of information typically (but not necessarily) contained on the front pages of a memory data sheet. It should include all of the following information:

- Product name and number
- Manufacturer's name
- Summary of product features and advantages
- Description of product
- Identification of technology used
- Logical block diagram
- Pin assignments
- Function tables
- Logic symbol
- Input/output definitions
- Description of device operation

1. Logic Definitions

Care should be taken in all definitions and descriptive information to consistently define logic states, particularly in the use of the terms TRUE/FALSE, HIGH/LOW, Active/Inactive, and ONE/ZERO. A logic TRUE is by definition a logic ONE and is logically Active; it may be electrically a HIGH or a LOW. Conversely, a logic FALSE is by definition a logic ZERO and is logically Inactive and may be an electrical HIGH or LOW. For positive logic a logic TRUE is a HIGH and a logic FALSE is a LOW while the opposite is true for negative logic. For positive logic, a non-barred signal is TRUE (Active) when HIGH, a barred signal is TRUE (Active) when LOW. Positive logic is assumed unless otherwise stated. This can be represented as:

Logical Terms	Electrical Terms	
	Positive Logic	Negative Logic
Active ≡ True ≡ 1	HIGH	LOW
Inactive ≡ False ≡ 0	LOW	HIGH

HIGH is defined as the most positive and LOW as the most negative electrical level.

Since it is very common to mix active HIGH and active LOW inputs/outputs on a single memory device, care should be taken not to confuse HIGH with logic ONE. It is recommended that input and output levels be referred to as HIGH and LOW. When it becomes necessary to describe the logical operation of a device, the preferred terms are TRUE and FALSE. The use of ONE (1) and ZERO (0) should be avoided on the data sheet.

2. Logic Diagrams

The logic diagram should logically and functionally define the operation of the memory device. Drawings should adhere to IEEE Standard 91-1973/ANSI Y32.14-1973.

3. Input/Output Definitions (Pin Names)

Where multiple symbols of a single type are required, such as for multiple addresses and/or data inputs/outputs, numbering should begin at 0 and go to N–1. Unlike address and data inputs, multiple control inputs which perform the identical function, such as multiple chip selects, etc., should be numbered from 1 to N. Control inputs which do not perform identical functions should be given separate names.

A logical bar should be used over I/O names and symbols to designate negative TRUE (i.e., active LOW, low TRUE). In cases where the use of a logical bar is not practical a letter B may be appended to the pin name to indicate that the signal is negative TRUE (i.e., RE would be REB). The logical bar should be omitted when forming symbols for timing intervals.

4. Absolute Maximum Ratings

The absolute maximum ratings define the range of conditions to which the device can be submitted without affecting the operation of the device after it is subsequently returned to the specified operating range. All conditions which might impair the operation of the device such as signal and power supply sequencing, time limits on stress conditions, or static discharge conditions, should be clearly stated. Since the absolute maximum ratings are outside the operating range, device operation is not implied.

5. Operating Conditions

The range of conditions under which the product specifications are warranted should be clearly stated at the beginning of the product specification section of the data sheet or at each location in the data sheet where device parameters are given. These conditions should always include temperature and voltage range. If operation of the device also depended on transient conditions on the power supplies or other inputs, these constraints should be clearly stated in the operating conditions. Additionally, timing measurement reference points and output load conditions should be given. Where additional conditions are not specified, the parameter limits shall be assumed to apply over the full operating range of the device.

6. Electrical Parameter Nomenclature

Electrical parameters are specified with an initial symbol that specifies the type of the parameter and subsequent symbols that further define the type of measurement.

Initial symbols include:

V = Voltage
I = Current
P = Power
C = Capacitance

Although electrical parameters have traditionally been written as subscripted symbols, they may be used in the non-subscripted format.

Subscripted	Non-Subscripted
V_{IH}	VIH
I_{OL}	IOL
V_{CC}	VCC

7. Power Supply Nomenclature

Power supplies should be designated as a three-letter symbol:

VCC = principal collector bias voltage
VEE = principal emitter bias voltage
VBB = principal base or substrate bias voltage
VDD = principal drain bias voltage
VGG = principal gate bias voltage
VSS = principal source bias voltage

If other designators are used, they should follow the same format and should be defined in the data sheet. The second and third letter in a power supply symbol shall always be the same. In some systems, a single power supply will be used for multiple purposes such as a collector bias supply for some devices and a drain bias supply for other devices. On devices commonly used with other logic families, the generic power supply name can be substituted.

In all cases substitution of I or P for V in the above list will define the current or power, respectively, associated with that power supply. PD shall be the symbol for the total power dissipation in the device with no external load.

8. Other Electrical Parameter Nomenclature

The second letter of a non-power supply symbol designates the type of Input/Output pins to which the measurement applies:

I = Input
O = Output

The third symbol designates the state applied to an input or to the state of an output (or the state the output would be in if not externally forced to some other state) of this/these I/O pin(s) during the measurement.

H = HIGH
L = LOW
Z = OFF (High Impedance state)

A fourth symbol may designate an external condition forced on an output.

S = Short circuit (connected to ground unless otherwise specified)

H = HIGH

L = LOW

Z = OFF (High Impedance state)

Examples:

VOH = Voltage on an output in the HIGH state.

IIL = Current through an input in the LOW state.

IOHS = Output short circuit (to ground unless otherwise stated) current with the device output driving HIGH.

IOZH = Output current with the output in the high-impedance state (OFF) and driven HIGH.

Although the symbols may be used in a subscripted form, they may also be listed as a single, uppercase, non-subscripted line in data sheets and related material. Conventional current (not electron current) flowing into the device is defined as positive; current flowing out of the device is defined as negative.

9. Timing Parameters

The timing parameters section of the data sheet defines the time dependent performance of the device. The timing parameters should be divided into two groups: timing requirements of the device and timing responses of the device. Timing requirements define the requirements on the input signals required for correct (specified) device operation and are always measured from one timing transition on an input or output to a timing transition on a device *input*. Timing responses specify device performance and are measured from an input or output timing transition to a device *output* timing transition. Timing requirements should be clearly separated from timing responses by grouping in a separate table or a separate section of a single table and by appropriate labeling.

10. Logic States (Levels)

Logic states (levels) are defined as a condition on an input or output. The states are:

1) HIGH ≡ ⩾ Minimum VIH or VOH

2) LOW ≡ ⩽ Maximum VIL or VOL

3) VALID ≡ Defined data satisfying one of the two above conditions, 1) or 2)

4) INVALID ≡ Data either not satisfying 1) or 2) above or undefined or don't care

5) OFF ≡ In the high impedance third state or OFF state

11. Transition Definitions

There are five kinds of transitions which are used as beginnings and ends of time interval measurements. The transitions are defined in reference to the final state to which the change is made.

The five symbols and their definitions are:

H = A transition from any level to a HIGH logic level.

L = A transition from any level to a LOW logic level.

V = A transition from any level to a valid steady-state level.

X = A transition from any level to an unknown, changing, or don't care level.

Z = A transition from any level to a high-impedance "OFF" state.

12. Nomenclature for Timing Parameters

Timing parameters are the measurement of the time elapsing between a transition on one pin and a transition on the same or another pin. These timing intervals can be written as:

TABCD or t_{ABCD}

where:

T or t — indicates time.

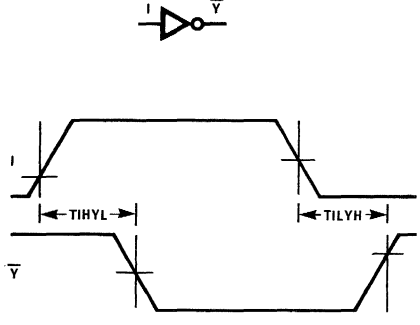
A — is the name of a signal or the terminal at which a transition occurs marking the beginning of the time interval being specified.

B — designates the direction (and possibly the measurement point) for the transition at terminal A.

C — is the name of a signal or the terminal at which a transition occurs marking the end of the time interval being specified.

D — designates the direction (and possibly the measurement point) of the transition at terminal C.

An inverter provides a simple example. If the input is labeled I and the output is labeled Y, then the two delay parameters for the inverter become TIHYL and TILYH.



The first interval is the delay from I HIGH to Y LOW and the second from I LOW to Y HIGH.

All types of timing parameters can be described in this format. Examples of timing intervals are:

1) Combinational Delays — *from* input transition *to* output transition.
2) Set-up and Hold Times — *from* input transition *to* another input transition.
3) Pulse Widths (Duration) — *from* input going LOW (or HIGH) *to* the same input going HIGH (or LOW).
4) Cycle Times — *from* an input transition *to* the next occurrence of the same transition.
5) Transition Times — *from* the beginning of an input or output transition *to* the end of the same transition.

13. Transition Measurement Points

Transitions should be measured from fixed, clearly defined voltage points. These voltage points should be expressed as fixed voltages referenced to one of the power supply pins.

Examples:

1.5 Volts
VDD - 2.0 Volts
2.0 Volts

It is recommended that timing points not be expressed as a percentage, i.e., do not use 10% and 90%. Do use, for example, 1.2 Volts and VDD - 1.2V.

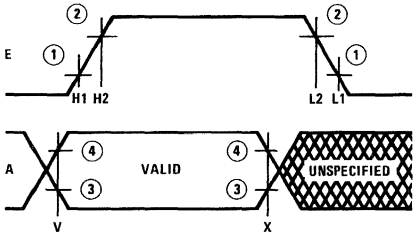
Data sheets should clearly define both the beginning and the ending voltage levels and the transition measuring points for all transitions.

14. Incorporation of Transition Measurement Points in Timing Parameter Nomenclature

In some cases, it is desirable to define more than one timing point in a transition. Particularly in MOS circuits it is desirable to define for a single LOW to HIGH transition:

1) a point at or near VIL
2) a point at or near VIH

Likewise, when making a HIGH to LOW transition, two similar timing points can be defined.

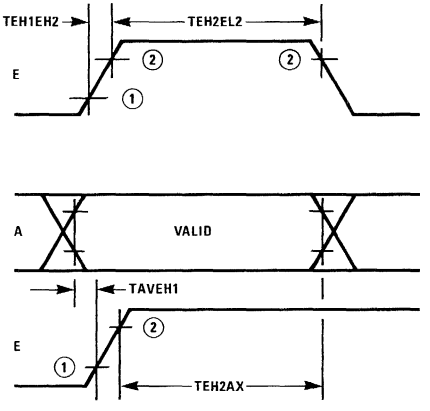


Multiple Timing Points in a Transition

Where it is necessary to define more than one timing point on a single transition, these timing points should be followed by a number. For example, transition H1 would represent timing point 1 on that transition to a HIGH level. Transition H2 would represent timing point 2 in the transition to a HIGH level. Similarly, transition L2 would be timing point 2 in a transition to a LOW level and transition point L1 would be timing point 1 during a transition to a LOW level.

Measurement points associated with high impedance OFF state are dependent on external loads applied to the device. Therefore, the data sheet should clearly show the external load and the specific voltage measurement points used to define the Z level.

The use of numbered timing points is illustrated below:



15. Refresh Time

Refresh is the operation of restoring charge in a dynamic memory cell. Refresh time is the time between successive refresh operations.

Since refresh is a complex operation to define logically it is suggested that R be used as the symbol to define the refresh operation. The symbol for refresh time is therefore written as TRVRV. TREF or t_{REF} may also be used to designate the refresh interval. A logical definition of the meaning of refresh should be given in the data sheet (e.g., cyclic, charge pump, planar, etc.).

16. Alternate Forms of Commonly Used Terms

Certain terms such as access, cycle, hold, set-up, pulse duration, and transition times are commonly used to define certain classes of timing intervals. An alternate format for naming these intervals is desirable for reasons of tradition and efficiency. These timing intervals can be written as:

TX(Y) or $t_{X(Y)}$

where:

T or t	indicates time.
X	is the type of timing interval as shown in section 17.
Y	is a pin name as defined in section 3 and tells something about the timing interval X. See section 17.

12

17. Symbols for Alternate Form

Symbol	Interval	Significance of Y
A	Access Time	Beginning measurement point
C	Cycle Time	Measurement point
H	Hold Time	Ending measurement point
S	Set-up Time	Beginning measurement point
W	Width (duration) Time	Signal name
T	Transition Time	Signal name
REF	Refresh Time	(not used)

18. Examples of Alternate Forms

TA (A)	= TAVQV	Address access
TA (E)	= TEHQV	Chip Enable access
TA (G)	= TGHQV	Output Enable access
TC (E)	= TEHEH or TELEL	Cycle time of Chip Enable
TC (EH1)	= TEH1EH1	Same as above with specified measuring point
TH (A)	= TEHAX	Address hold time
TH (D)	= TWHDX	Data hold time from Write
TH (D)	= TELDX	Data hold time from Chip Enable
TS (A)	= TAVEH	Address set-up time
TS (D)	= TDVWL	Data set-up time with respect to Write Enable
TW (E)	= TEHEL or TELEH	Chip Enable pulse width (duration)
TW (W)	= TWHWL or TWLWH	Write Enable pulse width (duration)
TT (E)	= TEH1EH2 or TEL2EL1	Chip Enable transition time
TREF	= TRVRV	Refresh time

Notice that in several cases the alternate form is ambiguous. Care should be taken to precisely define the interval by reference to the precise symbol in the TABCD format. When the TX(Y) format is used, the TABCD equivalent symbol should be included in the timing parameter specification table to define the alternate symbol. Either or both forms can be used in the timing diagram and other sections of the data sheet once the TX(Y) symbols have been defined by equating them to a TABCD symbol.

Whenever the timing interval cannot be defined as one of the seven types of intervals defined in the TX(Y) format, it must be defined in the TABCD format. Use of the TX(Y) format is optional since all intervals can be defined in the TABCD format.

19. Additional Descriptive Information

In some cases it is desirable to include additional descriptive information to further define a symbol. This information sometimes limits the definition to a certain mode of operation such as read or write or program mode. This information can be included in the TX(Y) format by adding it after the information in parentheses and can be included in the TABCD format by including it in parentheses after the normal symbol as shown below.

Examples:

TC (E) RD TEHEH (RD)	Read cycle time
TW (E) WR TEHEL (WR)	Chip Enable duration for Write Cycle
TS (A) P TAVEH (P)	Address set-up time in programming mode for a PROM

In each case, any additional descriptive information such as RD for READ or P for PROGRAM should be defined in words or table form.

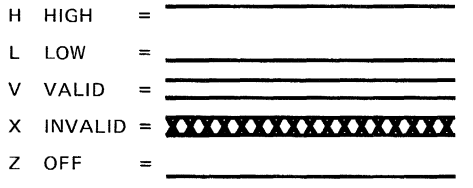
20. Definition of Maximum and Minimum

In all tables in the product specification section, it is important to define wherever possible values for maximum, typical, and minimum specifications. Typical specifications can be especially important when using statistical design techniques. Whether a parameter is specified as a minimum or maximum depends on whether it is considered from the system standpoint (what must be done to the device) or from the device standpoint (how the device responds to inputs). Timing *requirements* should be specified from the *system* standpoint. Therefore, set-up time is specified as a *minimum* since the system must provide this set-up time to the device. Timing *responses* are specified from a *device* standpoint. Access time is specified as a *maximum,* since it is the *maximum* response time of the device. The typical values are measured under the nominal operating conditions (voltage, temperature, etc.) and are defined as the median value taken over a wide number of samples which span the normal variations for that parameter which are found in the production situation. It is particularly important in capacitance measurements and current levels that typical as well as maximum levels be given.

Care should be taken in defining three-state outputs to always specify the minimum time to the output turning ON and the maximum time to the output turning OFF such that the user can insure that an overlap condition does not occur.

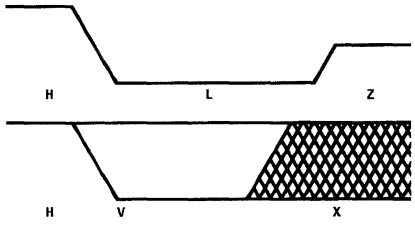
21. Timing Diagrams

As described in section 10, five discrete logic levels exist. These five logic states are shown graphically below as used in timing diagrams.



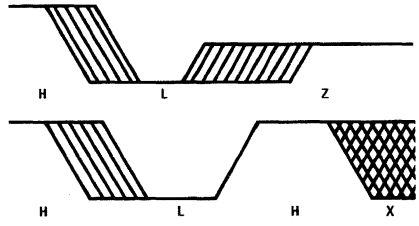
22. Transitions

Transitions from one state to another are shown by connecting the symbol for one state with that of the final state with a sloped line. The slope of the line represents a non-zero transition time.



23. Uncertainties

In cases where the exact time of the transition may vary or be unimportant, the transition should be drawn as a series of parallel transition lines. This series of transition lines should span the region in which the transition may occur.



Definition of Input/Output (Pin) Names

Recommended Symbol	Name	Definition
A	Address	Those input(s) whose logic states select a particular cell or group of cells.
D	Data Input	The input(s) whose logic state(s) determine(s) the data to be written into the memory.
Q	Data Output	The output(s) whose logic state(s) represent(s) the data read from the memory.
DQ	Data Input/Output	The port(s) that function as data input during write operations and as data output during read operations.
C	Shift Clock	The input(s) that when operated in a prescribed manner shift internal data in a serial memory.
W	Write Enable	The input(s) that when true enable(s) writing data into the memory. The data sheet must define the effect of both states of this input on the reading of data and the condition of the output.
P	Program	The input(s) that when true enable(s) programming, or writing into, a programmable read only memory (PROM).
G*	Output Enable	The input(s) that when false cause(s) the output to be in the OFF or high impedance state. This pin must be true for the output to be in any other state.
NC	Not Connected	The input(s)/output(s) that are not connected to any active part of the circuit or any other pin or any conductive surface of the package.
E	Chip Enable	The input(s) that when true permit(s) input, internal transfer, manipulation, refreshing, and output of data and when false causes the memory to be in a reduced power standby mode.
S	Chip Select	The input(s) that when false prohibit(s) writing into the memory and disables the output of the memory.

NOTE:
Chip Enable is a clock or strobe that significantly affects the power dissipation of the memory. Chip Select is a logical function that gates the inputs and outputs. For example, Chip Enable may be the cycle control of a dynamic memory or a power reduction input on a static memory.

RE	Row Enable (RAS)	The input which is used to strobe in the row address in multiplexed address RAMs.
CE	Column Enable (CAS)	The input which is used to strobe in the column address in multiplexed address RAMs.

*National will continue to use OD — Output Disable on selected parts — Ed.

Section 13

National's Literature Index

13

National Semiconductor's Data Bookshelf is a compendium of information about a product line unmatched in its breadth in the industry. The sixteen independent volumes that comprise the Bookshelf — over 5000 pages — describe in excess of 10,000 solid-state devices; devices that span the entire spectrum of semiconductor processes, and that range from the simplest of discrete transistors to microprocessors.

Active and passive devices and circuits; hybrid and monolithic structures; discrete and integrated components . . . complete electrical and mechanical specifications; charts, graphs, and tables; test circuits and waveforms; design and application information . . . Whatever you need you'll find in the designer's ultimate reference source — National Semiconductor's Data Bookshelf.

The Data Bookshelf: Tools For The Design Engineer

CMOS DATABOOK

National's Series 54C/74C logic is pin-for-pin, function-for-function equivalent to standard 7400 TTL. As such, you can take full advantage of your knowledge of 7400 when you use 54C/74C; all the design tricks of the one work with the other. Further, 54C/74C logic follows strict, consistent design rules set-up to simplify system design by giving you realistic, workable parameters with which to work.

The *CMOS Databook* completely specifies our 54C/74C logic products, as well as Series-4000 CMOS. Functions described include gates, buffers, flip-flops, counters, shift registers, decoders/demultiplexers, arithmetic functions, and more. For those who may be unfamiliar with CMOS logic, the text incorporates a series of application notes that define 54C/74C logic and show how to use it.

Mar. 1977, 560 pages, $4.00

INTERFACE DATABOOK

Peripheral/power drivers, level translators/buffers, line drivers and receivers, memory and clock drivers, sense amplifiers, display drivers, opto-couplers . . . you'll find them all in the *Interface Databook;* page after page of specifications that describe one of the industry's broadest line of interface products.

And to help you get the most from the circuitry, the text includes application notes that discuss such topics as transmission lines, data transmission in high-noise environments, driving gas-discharge and LED displays, and more. There are also product guides — listings that help you pick just the right circuit for your job from the many available; and even a cross-reference guide that lists product type numbers from other makers and gives the exact-replacement National part number.

The *Interface Databook* concludes with discussions of MIL-STD-883 and MIL-M-38510, and three pages of dimensioned package-outline drawings.

1977, 560 pages, $4.00

LINEAR APPLICATIONS HANDBOOK, VOL. I

This handbook provides you a fully-indexed, cross-referenced collection of linear integrated-circuit applications for National's monolithic and hybrid circuits.

Individual application notes are normally written to explain the operation and use of one particular device, or to detail various methods of accomplishing a given function. The organization of the *Linear Applications Handbook* takes advantage of this innate coherence: it keeps each application note intact, arranges them in numerical order, and provides detailed subject indices. The indices are composed of more than a thousand references to the main body of each text, and are the key to efficient access to the linear-applications experience garnered by National Semiconductor during the past eight years.

Feb. 1973, 432 pages, $4.00

LINEAR APPLICATIONS, VOL. II

The second volume of National's *Linear Applications Handbook* picks up where Volume I left off. Applications, notes and briefs, and pertinent articles published in the 3 years since Volume I was printed are included in this handbook. Volume II retains the same format as Volume I, to facilitate its use.

In this volume, as in Volume I, application schematics call out the generic family, which, by coincidence, is the military temperature range version of the device. Generally, any device in the generic family will work in the circuit. For example, an amplifier marked LM108 refers to the generic 108 family, and does not imply that only military-grade devices will work. Military (or industrial) grade devices need only be considered when their tighter electrical limits or wider temperature range warrant their use. As a reminder to our users, our numbering system is:

Device No.	Grade	Specified Temperature Range
LM1XX	Military	$-55°C \leq T_A \leq +125°C$
LM2XX	Industrial	$-25°C \leq T_A \leq +85°C$
LM3XX	Commercial	$0°C \leq T_A \leq +70°C$

Because commercial parts are less expensive than military or industrial, these points should be kept in mind when trying to determine the most cost-effective approach to a given design.

July 1976, 256 pages, $4.00

LINEAR DATABOOK

This edition of National's *Linear Databook* has been reformatted to make it more useful. Several new sections have been added which reflect National's larger and more diverse Linear product line. Added are Voltage References, Instrumentation Amplifiers, Sample and Hold circuits, and A/D and D/A converters. What was formerly the Consumer section is now Audio, Radio and TV, and the old Functional Blocks are now Industrial/Automotive/Functional Blocks.

The BI-FET process is a technological breakthrough pioneered by National, integrating implanted JFETs on the same chip with standard bipolar transistors.

The dramatic results are order-of-magnitude improvements in input characteristics, slew rates, and noise specifications. Products include LF156 series op amps, LF198 sample and hold, LF152 instrumentation amplifier, and LF11331/LF11201 series quad analog switches.

Guides pertinent to a particular section are now found at the beginnning of that section. Included are section contents, selection guides and/or definition of terms. This now allows the user to find all information concerning any particular product in one section without looking through the entire catalog. Ordering information, table of

contents, reliability programs, and any other information common to all sections is located in the front or back of the catalog.

National's Linear line is moving in new directions, summarized by looking at several developments which have taken place in the past year.

A family of 15 D/A and A/D products are being manufactured including 8-, 10- and 12-bit D/A and A/D converters, successive approximation registers, dual slope A/D's for panel meters, and precision voltage references. We have the distinct advantage of using any one of our many processing technologies to optimize the D/A, A/D design.

A low noise, ultra stable subsurface zener pioneered at National, is combined with a temperature stabilizer on a single chip to make the LM199 series precision voltage references. The LM199 features 1 ppm/°C guaranteed drift, 20 ppm long term stability, and 0.5Ω dynamic impedance at highly competitive prices. An LM129 series unheated version is also available.

New directions in Linear are aimed at development of building block circuits. Quad devices such as the LM124, LM139 and LM1900 series are finding wide acceptance as cost-saving alternatives to single and dual devices. The new LM148, LM149 quad 741 family is a versatile addition to this group which provides class AB outputs and wideband operation. The building block trend also includes timers (LM556), audio, radio and TV circuits, and in particular, automotive circuits (LM2907, LM2917 frequency to voltage converter).

June 1976, 968 pages, $4.00

MEMORY DATABOOK

Most of National's memory and memory-related products, regardless of their technology, are grouped together in the *Memory Databook:* a convenient, single-volume source of information and specifications about bipolar, MOS, and CMOS RAMs, field- and mask-programmable ROMs (bipolar and MOS), MOS shift registers, and PLAs.

In addition, the *Memory Databook* describes interface/support circuits for memory operation, and National's line of complete memory systems. Nor is how-to-use information neglected: there is a selection of memory-oriented application notes, including one on designing with PLAs. To aid you further, there are RAM, ROM, and PROM cross-reference guides, and even a production-status guide to National memories.

1977, 544 pages, $4.00

MICROPROCESSOR APPLICATIONS IN BUSINESS, SCIENCE AND INDUSTRY

For years National's microprocessors have impacted every facet of the application spectrum – from consumer games and point-of-sale terminals to scientific instruments and heavy industrial controls. Their use is growing rapidly. Today, those who are not actually using or considering microprocessors in their products stand to lose the competitive edge. And, that's why we have prepared this booklet of articles reprinted from industrial publications.

Starting with fundamentals, it details National's microprocessor technology – the devices, the support equipment, and the technical considerations. Equally important, it describes the spectra of successful applications from successful companies. By examining the technology and the applications you can see the microprocessor solution to your problems.

1977, 128 pages, $3.00

MOS/LSI DATABOOK

This Databook presents National's broad capability in the MOS/LSI areas – the fastest growing segment of the integrated circuit industry.

This 14 chapter, 750 page catalog covers a wide spectrum of product categories such as: Digital Electronic Clock circuits, Counter/Timers, Electronic Organ circuits, TV circuits, Analog-to-Digital (A/D) Converters, Communications/CB Radio circuits, Digital Watch circuits, Calculator circuits, and Keyboard Encoder circuits, all of which are described in complete electrical and mechanical specifications.

Custom MOS/LSI capabilities are also described for six MOS technologies. In addition, National's new family of Controller Oriented Processor Systems (COPS) is presented. This family addresses a wide variety of low-cost controller applications such as: Appliance Timers, Photo Timers, Lawn Sprinkler Controllers, Electronic Scales, Electronic Cash Registers and Traffic Controllers.

Two support circuit sections are also included. These are Display circuits and Interface Drivers. A separate section also covers Clock Modules, which describes completed modules employing National's electronic digital clock circuits and LED displays.

The *MOS/LSI Databook* presents state-of-the-art semiconductor products with LSI complexity for all MOS products except for MOS Memories and Microprocessors which are represented in separate Databooks.

1977, 720 pages, $4.00

PRESSURE TRANSDUCER HANDBOOK

This is the new catalog and handbook of integrated-circuit pressure transducers from National Semiconductor. In addition to complete specifications and a quick selection guide for National's IC transducer products, this edition includes comprehensive discussions of transducer theory, device structure, reliability and in-depth application data including circuits for the new easy-to-use autoreference compensation technique for improving accuracy in any application.

Because IC transducers are finding use in many and diverse disciplines, the breadth of application information includes traditional, non-traditional and state-of-the-art fields as well. National hopes this catalog/handbook provides the requisite insight and data for your own special applications.

1977, 142 pages, $3.00

SC/MP MICROPROCESSOR APPLICATIONS HANDBOOK

In conjunction with other SC/MP support documents, this Applications Handbook provides the user with sufficient information to build, checkout, and utilize a wide variety of SC/MP based systems. The information is organized in capsule form; thus, the designer can, with minimum effort, expand, modify, or customize a given application.

The applications are organized by class – Analog-to-Digital/Digital-to-Analog Systems, Keyboard/Display Systems, Multiprocessor Systems, and so on. Chapter I and the appendices provide general design data as regards the instruction set, addressing modes, input/output capabilities, interrupt structures, and other applications related features.

1977, 160 pages, $5.00

SPECIAL FUNCTION DATABOOK

This collection of circuits contains detailed information for the specification and application of a large number and variety of products, which are grouped together because most of them are hybrid modules with unusual characteristics.

In the Sample-and-Hold Amplifiers section, for example, you'll find precision sample-and-holds, fast S/H, very-fast S/H, and a compact, complete-with-everything S/H module. Under the Analog Switch heading are DPDT and DPST MOS/FET and JFET switches, quads, duals, low-cost switches, high-speed switches, multiplexers, commutators, etc. And under Amplifiers you'll find micropower and low-power op amps, high-voltage types, wideband types, high-slew-rate amps, and so on. Besides the product categories just mentioned, the *Special Function Databook* also describes AD/DA converters, buffers, comparators, MOS clock drivers, digital drivers, resistor arrays, and active filters; there are three op amp selection guides, and FET op amp and analog switch cross-reference listings as well.

Apr. 1976, 308 pages, $3.00

DISCRETE DATABOOK

National's discrete semiconductors are described and specified in the *Discrete Databook*. In addition to bipolar and JFET small-signal transistors, the text covers multiple-bipolars, multiple JFETs, and power transistors, including commercial, industrial, and JAN/JANTX/JANTXV types.

Besides specification sheets and package outline drawings, the book includes Process Characteristics sheets. These sheets describe and illustrate the many chip types used in National's discretes, and fully specify (via tables and curves) the performance of any device built with given process. Thus, a relatively-limited number of Process Characteristics sheets describes thousands of devices; a Standard Transistor Parts List refers each transistor type to a particular Process Characteristics sheet that determines the specifications for the device.

The *Discrete Databook* includes a great deal of helpful information apart from the specifications themselves: MIL-STD qualification data; bipolar and FET dice availability; a bipolar-transistor equivalents list; how to choose the proper JFET; a JFET applications guide; and a JFET cross-reference listing. There is also an extensive glossary of JFET terms and symbols.

Feb. 1978, 480 pages, $4.00

TTL DATABOOK

This volume of the Data Bookshelf has become one of the industry's best-known sources of DTL/TTL/ECL product information. It fully specifies National's extremely-broad line of bipolar logic; standard 54/74TTL; low-power 54L/74L; high-speed 54H/74H; ultrahigh-speed Schottky 54S/74S; low-power Schottky 71LS/81LS; Series 9000 TTL; Series 10,000 ECL; and Series 930 DTL.

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Feb. 1976, 592 pages, $4.00

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Section 14

Memory Databook Referral Index

14

Virtually no data sheets have been included in this handbook. National's Memory Databook contains a complete collection of the specifications of your favorite components. Be our guest and use this section to list part numbers and Memory Databook page numbers for future reference.

Referral Index to National's Memory Databook

This section provides a convenient place for you to make note of your favorite components from National's Memory Databook.

Just jot down the part number and page for easy reference in the future. Space has been left for several editions of the Memory Databook.

Part Number	Page in '77 Edition	Page in '78 Edition	Edge Index
MOS RAMs			1
Bipolar RAMs			2
CMOS RAMs			3
Charge Coupled Devices			4
MOS EPROMs			5

Referral Index to National's Memory Databook

Part Number	Page in '77 Edition	Page in '78 Edition	Edge Index
Bipolar PROMs			6
Bipolar ROMs			7
MOS ROMs			8
Character Generators			9
Code Converters			10

Referral Index to National's Memory Databook

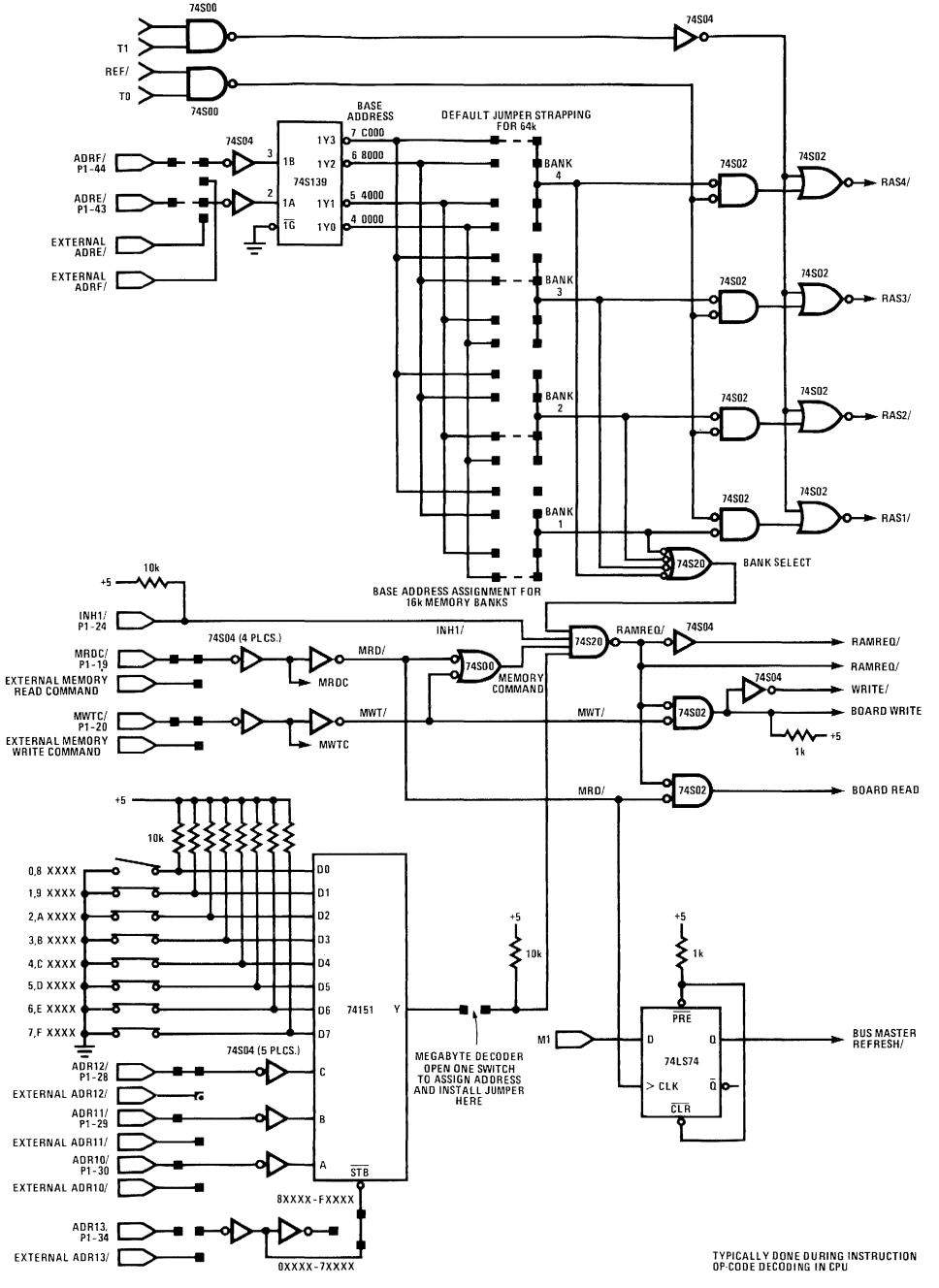
Part Number	Page in '77 Edition	Page in '78 Edition	Edge Index
Shift Registers			11
Interface			12

Notes

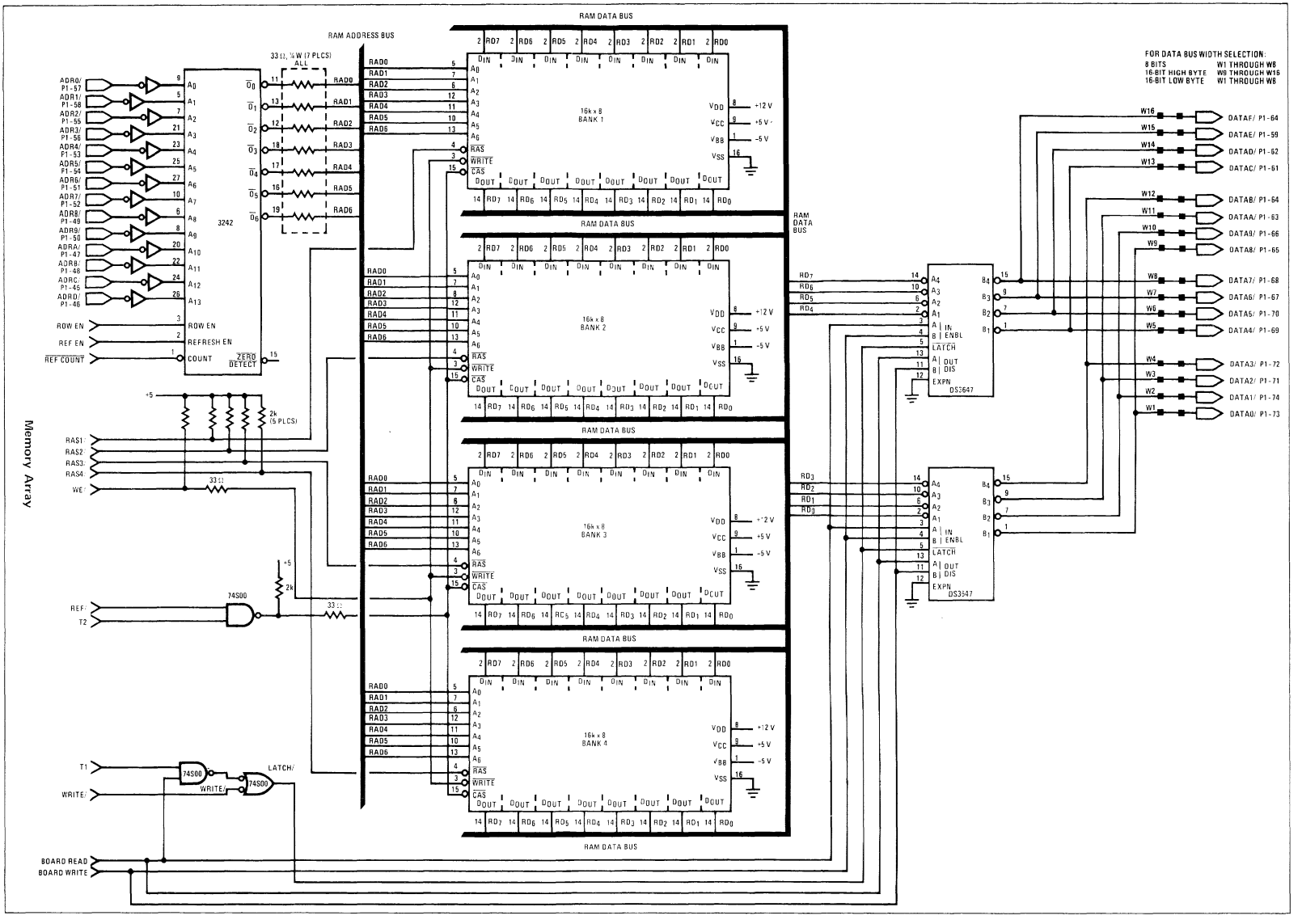
National Semiconductor

ERRATA

The following two diagrams represent improved methods for implementing the memory design beginning on page 2-9. This approach, implementing "RAS/only refresh," will result in significant power savings. These diagrams can replace pages 2-14 and 2-16.



Memory Select Logic


RAM ADDRESS BUS
RAM DATA BUS
33Ω, ¼W (7 PLCS)
ALL
3242
ADR0/ P1-57
ADR1/ P1-58
ADR2/ P1-55
ADR3/ P1-56
ADR4/ P1-53
ADR5/ P1-54
ADR6/ P1-51
ADR7/ P1-52
ADR8/ P1-49
ADR9/ P1-50
ADRA/ P1-47
ADRB/ P1-48
ADRC/ P1-45
ADRD/ P1-46
ROW EN
REFRESH EN
REF COUNT
COUNT
ZERO DETECT
RAD0
RAD1
RAD2
RAD3
RAD4
RAD5
RAD6
16k x 8 BANK 1
16k x 8 BANK 2
16k x 8 BANK 3
16k x 8 BANK 4
RAS
WRITE
CAS
+12 V
+5 V
-5 V
RD7
RD6
RD5
RD4
RD3
RD2
RD1
RD0
DS3647
IN ENBL
LATCH
OUT DIS
EXPN
FOR DATA BUS WIDTH SELECTION:
8 BITS W1 THROUGH W8
16-BIT HIGH BYTE W9 THROUGH W16
16-BIT LOW BYTE W1 THROUGH W8
DATAF/ P1-64
DATAE/ P1-59
DATAD/ P1-62
DATAC/ P1-61
DATAB/ P1-64
DATAA/ P1-63
DATA9/ P1-66
DATA8/ P1-65
DATA7/ P1-68
DATA6/ P1-67
DATA5/ P1-70
DATA4/ P1-69
DATA3/ P1-72
DATA2/ P1-71
DATA1/ P1-74
DATA0/ P1-73
2k (5 PLCS)
RAS1
RAS2
RAS3
RAS4
WE
74S00
REF T2
T1
WRITE
LATCH/
BOARD READ
BOARD WRITE

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