Designer's Encyclopedia of Bipolar One-Shots

National Semiconductor
Application Note 372
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INTRODUCTION

National Semiconductor manufacturers a broad variety of industrial bipolar monostable multivibrators (one-shots) in TTL and LS-TTL technologies to meet the stringent needs of systems designers for applications in the areas of pulse generation, pulse shaping, time delay, demodulation, and edge detection of waveforms. Features of the various device types include single and dual monostable parts, retriggerable and non-retriggerable devices, direct clearing input, and DC or pulse-triggered inputs. Furthermore, to provide the designer with complete flexibility in controlling the pulse width, some devices also have Schmitt trigger input, and/or contain internal timing components for added design convenience.

DESCRIPTION

One-shots are versatile devices in digital circuit design. They are actually quite easy to use and are best suited for applications to generate or to modify short timings ranging from several tens of nanoseconds to a few microseconds. However, difficulties are constantly being experienced by design and test engineers, and basically fall into the categories of either pulse width problems or triggering difficulties.

The purpose of this note is to present an overall view of what one-shots are, how they work, and how to use them properly. It is intended to give the reader comprehensive information which will serve as a designer's guide to bipolar one-shots.

Nearly all malfunctions and failures on one-shots are caused by misuse or misunderstanding of their fundamental operating rules, characteristic design equations, parameters, or more frequently by poor circuit layout, improper bypassing, and improper triggering signal.

In the following sections all bipolar one-shots manufactured by National Semiconductor are presented with features tables and design charts for comparisons. Operating rules are outlined for devices in general and for specific device types. Notes on unique differences per device and on special operating considerations are detailed. Finally, truth tables and connection diagrams are included for reference.

DEFINITION

A one-shot integrated circuit is a device that, when triggered, produces an output pulse width that is independent of the input pulse width, and can be programmed by an external Resistor-Capacitor network. The output pulse width will be a function of the RC time constant. There are various one-shots manufactured by National Semiconductor that have diverse features, although, all one-shots have the basic property of producing a programmable output pulse width. All National one-shots have True and Complementary outputs, and both positive and negative edge-triggered inputs.

OPERATING RULES

In all cases, R and C represented by the timing equations are the external resistor and capacitor, called R_{EXT} and C_{EXT}, respectively, in the data book. All the foregoing timing equations use C in pF, R in KΩ, and yield t_W in nanoseconds. For those one-shots that are not retriggerable, there is a duty cycle specification associated with them that

TTL AND LS-TTL ONE-SHOT FEATURES

Device Number	# Per IC Package	Re-trigger	Reset	Capacitor Min	Capacitor Max	Resistor Min	Resistor Max	Timing Equation* for $C_{EXT} > 1000$ pF
				in μF		in KΩ		
DM54121	One	No	No	0	1000	1.4	30	$t_W = KRC\bullet(1 + 0.7/R)$
DM74121	One	No	No	0	1000	1.4	40	$K = 0.55$
DM54LS122	One	Yes	Yes	None		5	180	$t_W = KRC$
DM74LS122	One	Yes	Yes	None		5	260	$K = 0.45$
DM54123	Two	Yes	Yes	None		5	25	$t_W = KRC\bullet(1 + 0.7/R)$
DM74123	Two	Yes	Yes	None		5	50	$K = 0.34$
DM54LS123	Two	Yes	Yes	None		5	180	$t_W = KRC$
DM74LS123	Two	Yes	Yes	None		5	260	$K = 0.45$
DM54LS221	Two	No	Yes	0	1000	1.4	70	$t_W = KRC$
DM74LS221	Two	No	Yes	0	1000	1.4	100	$K = 0.7$
DM8601	One	Yes	No	None		5	25	$t_W = KRC\bullet(1 + 0.7/R)$
DM9601	One	Yes	No	None		5	50	$K = 0.32$
DM8602	Two	Yes	Yes	None		5	25	$t_W = KRC\bullet(1 + 1/R)$
DM9602	Two	Yes	Yes	None		5	50	$K = 0.31$

*The above timing equations hold for all combinations of R_{EXT} and C_{EXT} for all cases of $C_{EXT} > 1000$ pF within specified limits on the R_{EXT} and C_{EXT}.

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defines the maximum trigger frequency as a function of the external resistor, R_{EXT}.

In all cases, an external (or internal) timing resistor (R_{EXT}) connects from V_{CC} or another voltage source to the "R_{EXT}/C_{EXT}" pin, and an external timing capacitor (C_{EXT}) connects between the "R_{EXT}/C_{EXT}", and "C_{EXT}" pins are required for proper operation. There are no other elements needed to program the output pulse width, though the value of the timing capacitor may vary from 0.0 to any necessary value.

When connecting the R_{EXT} and C_{EXT} timing elements, care must be taken to put these components absolutely as close to the device pins as possible, electrically and physically. Any distance between the timing components and the device will cause time-out errors in the resulting pulse width, because the series impedance (both resistive and inductive) will result in a voltage difference between the capacitor and the one-shot. Since the one-shot is designed to discharge the capacitor to a specific fixed voltage, the series voltage will "fool" the one-shot into releasing the capacitor before the capacitor is fully discharged. This will result in a pulse width that appears much shorter than the programmed value. We have encountered users who have been frustrated by pulse width problems and had difficulty to perform correlations with commercial test equipment. The nature of such problems are usually related to the improper layout of the DUT adapter boards. (See *Figure 6* for a PC layout of an AC test adapter board.) It has been demonstrated that lead length greater than 3 cm from the timing component to the device pins can cause pulse width problems on some devices.

For precise timing, precision resistors with good temperature coefficient should be used. Similarly, the timing capacitor must have low leakage, good dielectric absorption characteristics, and a low temperature coefficient for stability. Please consult manufacturers to obtain the proper type of component for the application.

For small time constants, high-grade mica glass, polystyrene, polypropylene, or polycarbonate capacitor may be used. For large time constants, use a solid tantalum or special aluminum capacitor.

In general, if a small timing capacitor is used that has leakage approaching 100 nA or if the stray capacitance from either terminal to ground is greater than 50 pF, then the timing equations or design curves which predict the pulse width would not represent the programmed pulse width which the device generates.

When an electrolytic capacitor is used for C_{EXT}, a switching diode is often suggested for standard TTL one-shots to prevent high inverse leakage current *(Figure 1)*. In general, this switching diode is not required for LS-TTL devices; it is also not recommended with retriggerable applications.

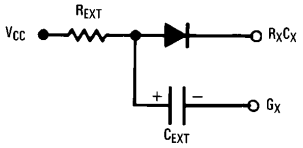

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FIGURE 1

It is never a good practice to leave any unused inputs of a logic integrated circuit "floating". This is particularly true for one-shots. Floating uncommitted inputs or attempts to establish a logic HIGH level in this manner will result in malfunction of some devices.

Operating one-shots with values of the R_{EXT} outside the recommended limits is at the risk of the user. For some devices it will lead to complete inoperation, while for other devices it may result in either output pulse widths different from those values predicted by design charts or equations, or with modes of operation and performance quite different from known standard characterizations.

To obtain variable pulse width by remote trimmiing, the following circuit is recommended *(Figure 2)*. "R_{REMOTE}" should be placed as close to the one-shot as possible.

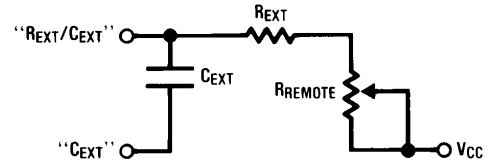

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FIGURE 2

V_{CC} and ground wiring should conform to good high frequency standards and practices so that switching transients on the V_{CC} and ground return leads do not cause interaction between one-shots. A 0.001 μF to 0.1 μF bypass capacitor (disk or monolithic type) from the V_{CC} pin to ground is necessary on each device. Furthermore, the bypass capacitor shoud be located so as to provide as short an electrical path as possible between the V_{CC} and ground pins. In severe cases of supply-line noise, decoupling in the form of a local power supply voltage regulator is necessary.

For retriggerable devices the retrigger pulse width is calculated as follows for positive-edge triggering:

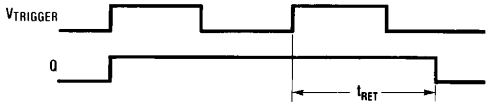

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FIGURE 3

$$t_{RET} = t_W + t_{PLH} = K \bullet (R_{EXT})(C_{EXT}) + t_{PHL}$$

(See tables for exact expressions for K and t_W; K is unity on most HCMOS devices.)

SPECIAL CONSIDERATIONS AND NOTES:

The 9601 is the single version of the dual 9602 one-shot. With the exception of an internal timing resistor, R_{INT}, the 'LS122 has performance characteristics virtually identical to the 'LS123. The design and characteristic curves for equivalent devices are not depicted individually, as they can be referenced from their parent device.

National's TTL-'123 dual retriggerable one-shot features a unique logic realization not implemented by other manufacturers. The "CLEAR" input does not trigger the device, a design tailored for applications where it is desired only to terminate or to reduce the timing pulse width.

The 'LS221, even though it has pin-outs identical to the 'LS123, is not functionally identical. It should be remembered that the 'LS221 is a non-retriggerable one-shot, while the 'LS123 is a retriggerable one. For the 'LS123 device, it is sometimes recommended to externally ground its "C_{EXT}" pin for improved system performance. The "C_{EXT}" pin on the 'LS221, however, is not an internal connection to the device ground. Hence, grounding this pin on the 'LS221 device will render the device inoperative.

Furthermore, if a polarized timing capacitor is used on the 'LS221, the positive side of the capacitor should be connected to the "C_{EXT}" pin. For the 'LS123 part, it is the contrary, the negative terminal of the capacitor should be connected to the "C_{EXT}" pin of the device *(Figure 4)*.

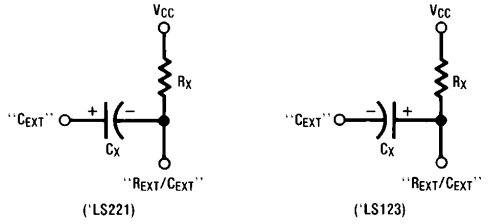

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FIGURE 4

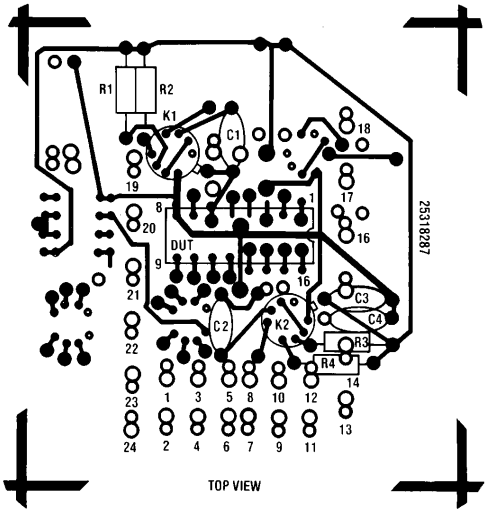

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FIGURE 6a. AC Test Adapter

The 'LS221 trigger on "CLEAR": This mode of trigger requires first the "B-Input" be set from a Low-to-High level while the "CLEAR" input is maintained at logic Low level. Then, with the "B" Input at logic High level, the "CLEAR" input, whose positive transition from LOW-to-HIGH will trigger an output pulse ("A input" is LOW).

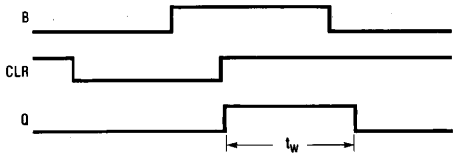

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FIGURE 5

AC Test Adapter Board

The compact PC layout below is a universal one-shot test adapter board. By wiring different jumpers, it can be configured to accept all one-shots made by National Semiconductor. The configuration shown below is dedicated for the '123 device. It has been used successfully for functional and pulse width testing on all the '123 families of one-shots on the MCT AC test system.

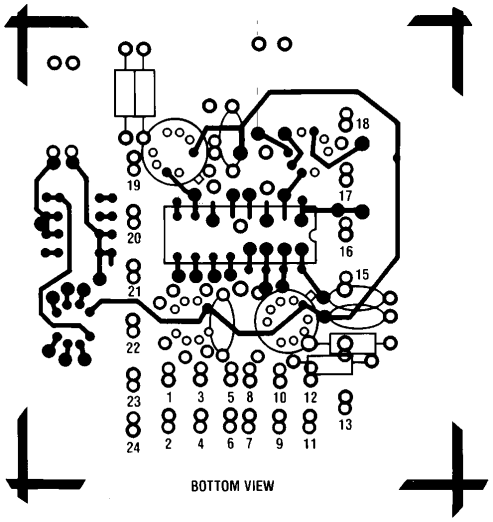

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FIGURE 6b. AC Test Adapter

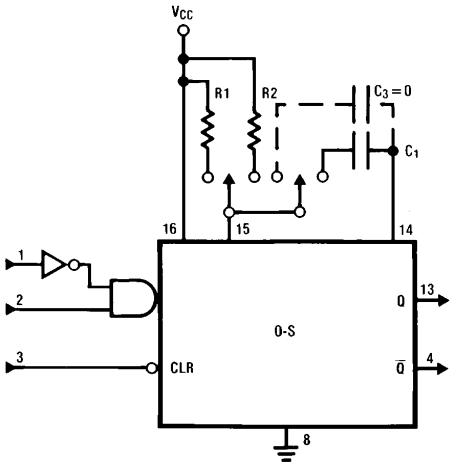

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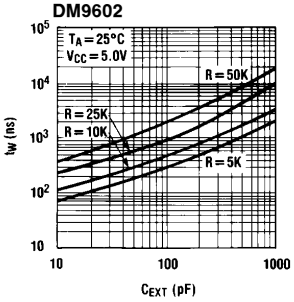
FIGURE 7a. Timing Components and I/O connections to D.U.T.

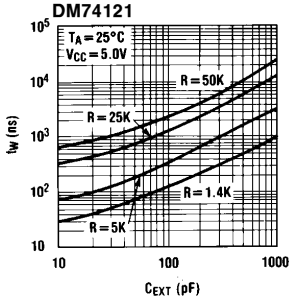
Typical Output Pulse Width vs Timing Components

Timing equations listed in the features tables hold all combinations of R_{EXT} and C_{EXT} for all cases of $C_{EXT} >$ 1000 pF. For cases where the $C_{EXT} <$ 1000 pF, use graphs shown below.

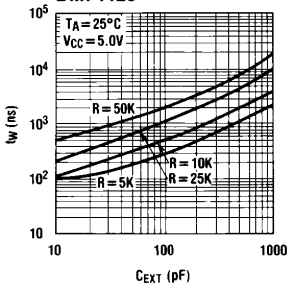
DM9602



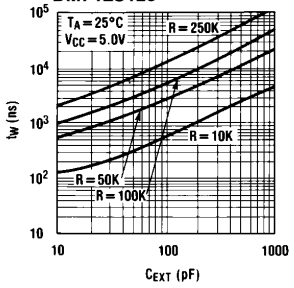
DM74121



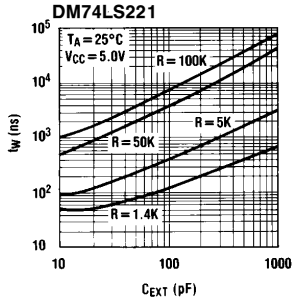
DM74123



DM74LS123



DM74LS221



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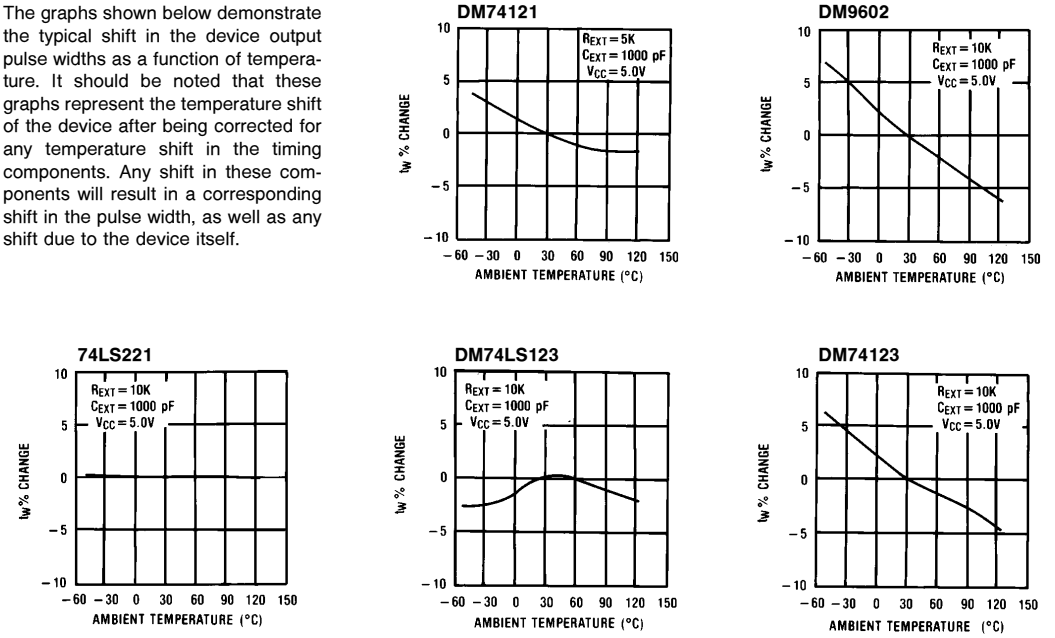
Typical Output Pulse Width Variation vs Ambient Temperature

The graphs shown below demonstrate the typical shift in the device output pulse widths as a function of temperature. It should be noted that these graphs represent the temperature shift of the device after being corrected for any temperature shift in the timing components. Any shift in these components will result in a corresponding shift in the pulse width, as well as any shift due to the device itself.



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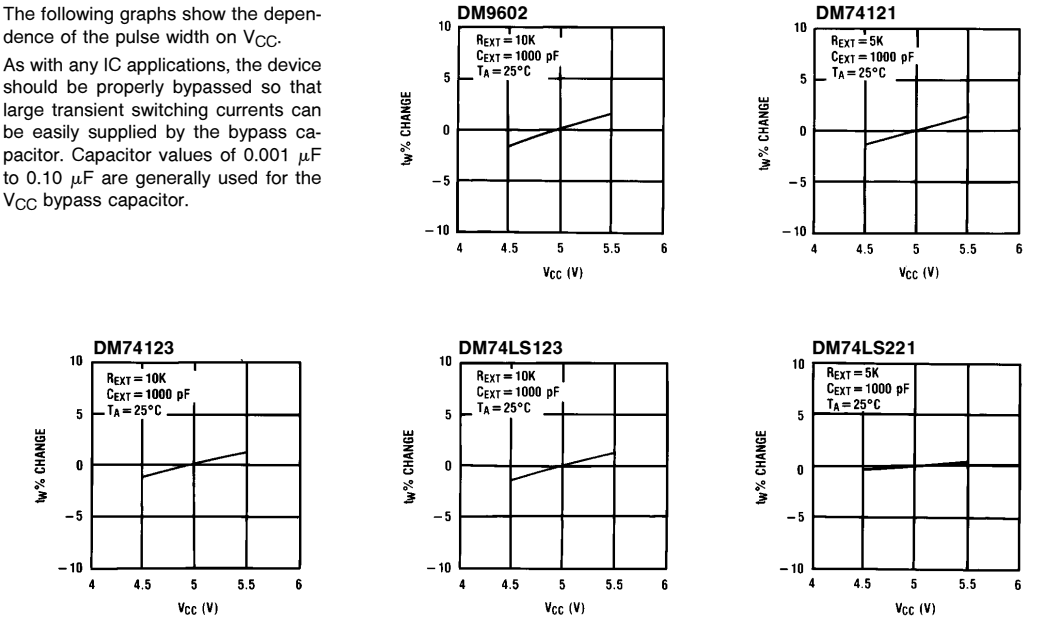
Typical Output Pulse Width Variation vs Supply Voltage

The following graphs show the dependence of the pulse width on V_{CC}.

As with any IC applications, the device should be properly bypassed so that large transient switching currents can be easily supplied by the bypass capacitor. Capacitor values of 0.001 μF to 0.10 μF are generally used for the V_{CC} bypass capacitor.



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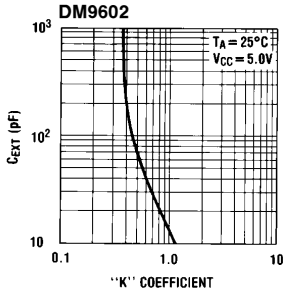
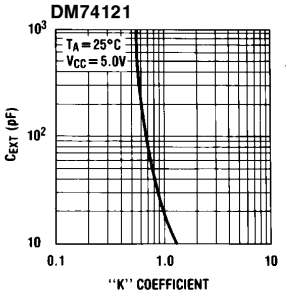
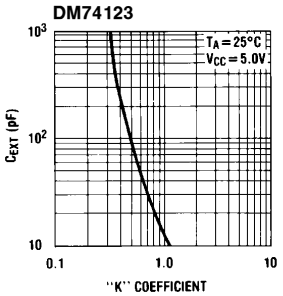
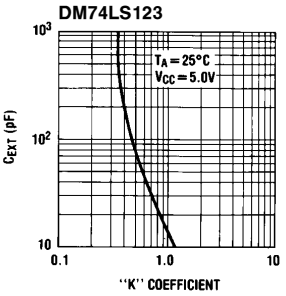
Typical "K" Coefficient Variation vs Timing Capacitance

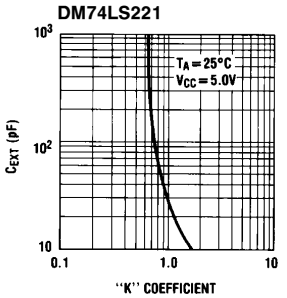
For certain one-shots, the "K" coefficient is not a constant, but varies as a function of the timing capacitor C_{EXT}. The graphs below detail this characteristic.











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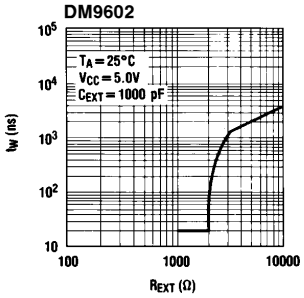
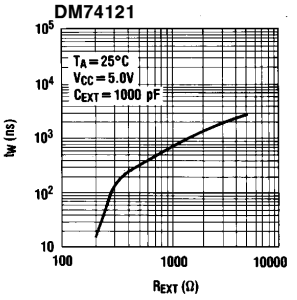
Typical Output Pulse Width vs Minimum Timing Resistance

The plots shown below demonstrate typical pulse widths and limiting values of the true output as a function of the external timing resistor, R_{EXT}. This information should evaporate those years of mysterious notions and numerous concerns about operating one-shots with lower that recommended minimum R_{EXT} values.





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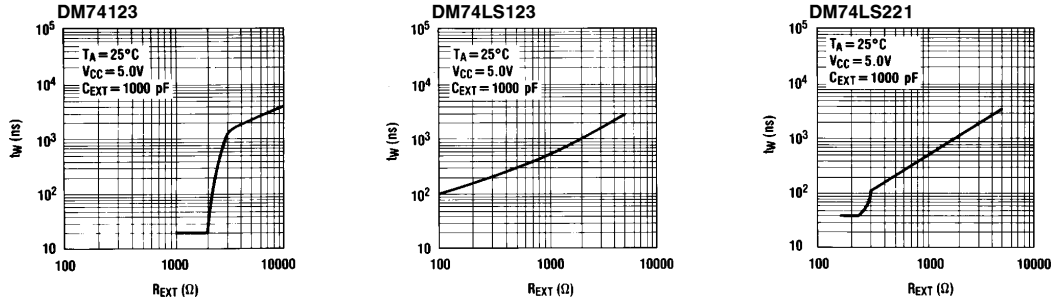
Typical Output Pulse Width vs Minimum Timing Resistance (Continued)



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Function Tables

'121 One-Shots

Inputs			Outputs	
A1	A2	B	Q	$\overline{Q}$
L	X	H	L	H
X	L	H	L	H
X	X	L	L	H
H	H	X	L	H
H	↓	H	⎍	⎎
↓	H	H	⎍	⎎
↓	↓	H	⎍	⎎
L	X	↑	⎍	⎎
X	L	↑	⎍	⎎

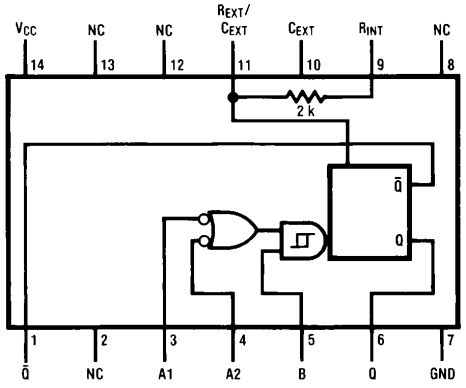
'122 Retriggerable One-Shots with Clear

Inputs					Outputs	
Clear	A1	A2	B1	B2	Q	$\overline{Q}$
L	X	X	X	X	L	H
X	H	H	X	X	L	H
X	X	X	L	X	L	H
X	X	X	X	L	L	H
X	L	X	H	H	L	H
H	L	X	↑	H	⎍	⎎
H	L	X	H	↑	⎍	⎎
H	X	L	H	H	L	H
H	X	L	↑	H	⎍	⎎
H	X	L	H	↑	⎍	⎎
H	H	↓	H	H	⎍	⎎
H	↓	↓	H	H	⎍	⎎
H	↓	H	H	H	⎍	⎎
↑	L	X	H	H	⎍	⎎
↑	X	L	H	H	⎍	⎎

H = HIGH Level
L = LOW Level
↑ = Transition from LOW-to-HIGH
↓ = Transition from HIGH-to-LOW
⎍ = One HIGH Level Pulse
⎎ = One LOW Level Pulse
X = Don't Care

Connection Diagrams

54121 (J, W); 74121 (N)



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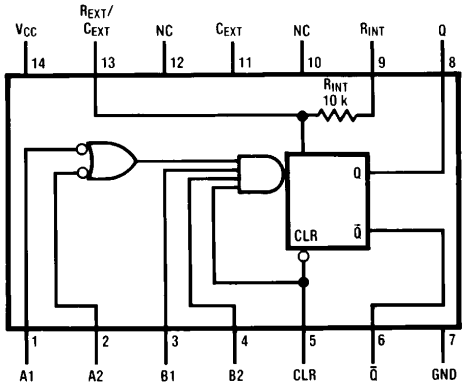
Top View

54LS122 (J, W); 74LS122 (N)



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Top View

Function Tables (Continued)

'123 Dual Retriggerable One-Shots with Clear
'123

Inputs			Outputs	
A	**A**	**Clear**	**Q**	**$\overline{Q}$**
H	X	H	L	H
X	L	H	L	H
L	↑	H	⎍	⎎
↓	H	H	⎍	⎎
X	X	L	L	H

'LS123

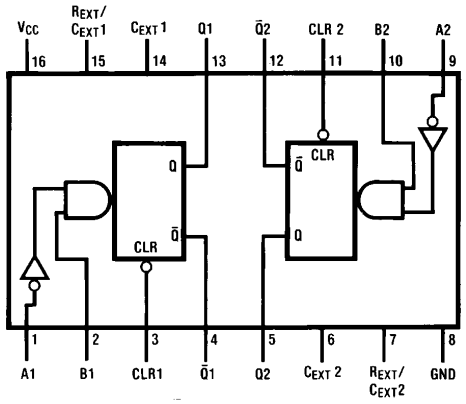
Inputs			Outputs	
Clear	**A**	**B**	**Q**	**$\overline{Q}$**
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	↑	⎍	⎎
H	↓	H	⎍	⎎
↑	L	H	⎍	⎎

8602

Pin Numbers			Operation
A	**B**	**CLEAR**	
↓	L	H	Trigger
H	↑	H	Trigger
X	X	L	Reset

H = HIGH Level
L = LOW Level
↑ = Transition from LOW-to-HIGH
↓ = Transition from HIGH-to-LOW
⎍ = One HIGH Level Pulse
⎎ = One LOW Level Pulse
X = Don't Care

Connection Diagrams (Continued)



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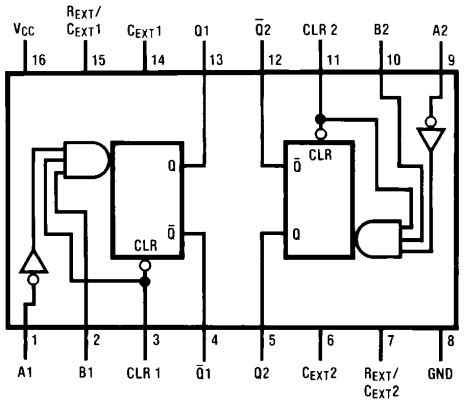
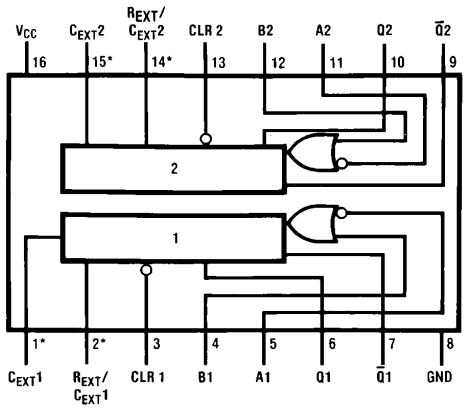
Top View
54LS123 (J, W); 74LS123 (N)



TL/F/7508–18

Top View
9602 (J, W); 8602 (N)



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Top View

*Pins for external timing.

Function Tables (Continued)

'221 Dual One-Shots with Schmitt Trigger Inputs

Inputs			Outputs	
Clear	**A**	**B**	**Q**	$\overline{Q}$
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	↑	⎍	⎎
H	↓	H	⎍	⎎
↑	L	H	⎍	⎎

8601

Inputs				Outputs	
A1	**A2**	**B1**	**B2**	**Q**	$\overline{Q}$
H	H	X	X	L	H
X	X	L	X	L	H
X	X	X	L	L	H
L	X	H	H	L	H
L	X	↑	H	⎍	⎎
L	X	H	↑	⎍	⎎
X	L	H	H	L	H
X	L	↑	H	⎍	⎎
X	L	H	↑	⎍	⎎
H	↓	H	H	⎍	⎎
↓	↓	H	H	⎍	⎎
↓	H	H	H	⎍	⎎

H = HIGH Level
L = LOW Level
↑ = Transition from LOW-to-HIGH
↓ = Transition from HIGH-to-LOW
⎍ = One HIGH Level Pulse
⎎ = One LOW Level Pulse
X = Don't Care

Applications

The following circuits are shown with generalized one-shot connection diagram.

NOISE DISCRIMINATOR *(Figure 8)*

The time constant of the one-shot (O-S) can be adjusted so that an input pulse width narrower than that determined by the time constant will be rejected by the circuit. Output at Q_2 will follow the desired input pulse, with the leading edge delayed by the predetermined time constant. The output pulse width is also reduced by the amount of the time constant from R_X and C_X.

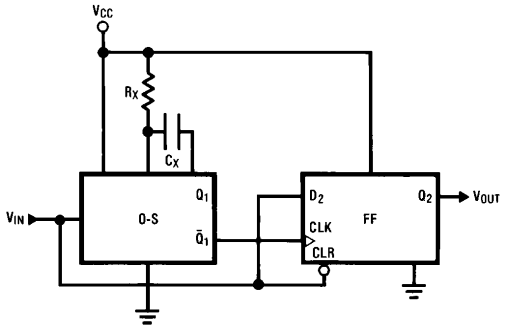

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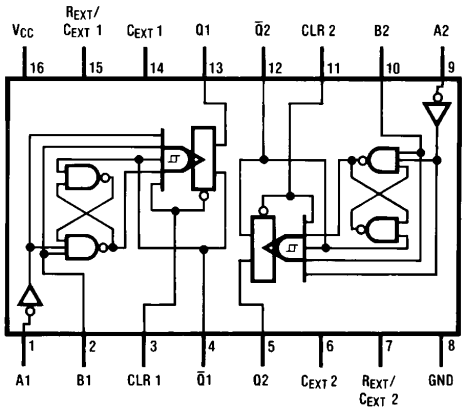
FIGURE 8. Noise Discriminator

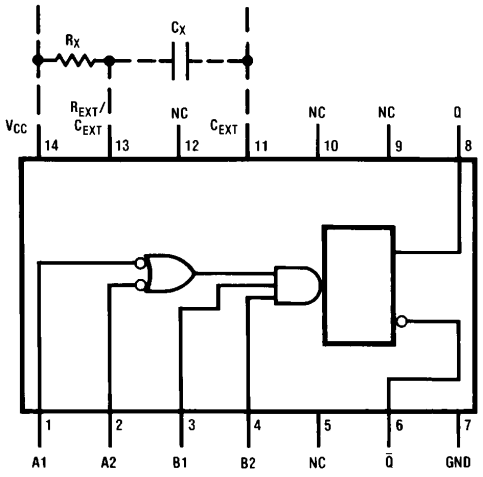
Connection Diagrams (Continued)

54LS221 (J, W); 74LS221 (N)



Top View TL/F/7508–20

9601 (J, W); 8601 (N)



Top View TL/F/7508–21

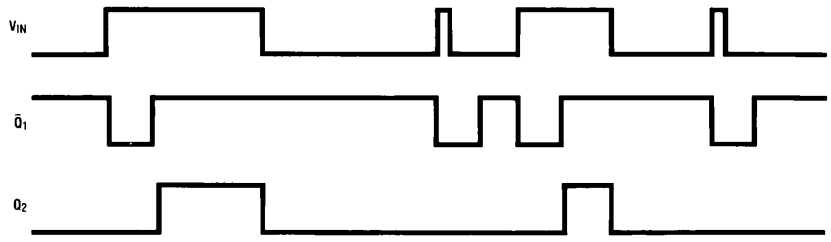


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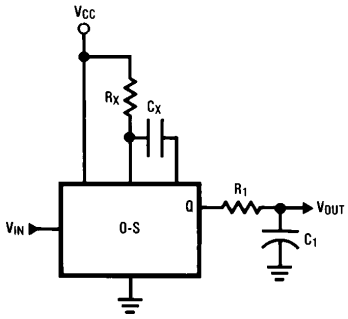
FIGURE 8. Noise Discriminator (Continued)

FREQUENCY DISCRIMINATOR *(Figure 9)*

The circuit shown in *Figure 9* can be used as a frequency-to-voltage converter. For a pulse train of varying frequency applied to the input, the one-shot will produce a pulse constant width for each triggering transition on its input. The output pulse train is integrated by R_1 and C_1 to yield a waveform whose amplitude is proportional to the input frequency. (Retriggerable device required.)



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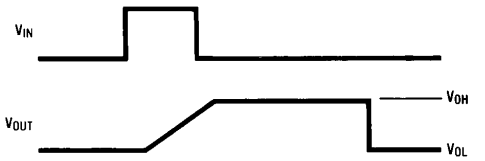

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FIGURE 9. Frequency Discriminator

ENVELOPE DETECTOR *(Figures 10a and 10b)*

An envelope detector can be made by using the one-shot's retrigger mode. The time constant of the device is selected to be slightly longer than the period of each cycle within the input pulse burst. Two distinct DC levels are present at the output for the duration of the input pulse burst and for its absence (see *Figure 10a*). The same circuit can also be employed for a specific frequency input as a Schmitt trigger to obviate input trigger problems associated with hysteresis and slow varying, noisy waveforms (see *Figure 10b*). (Retriggerable device required.)

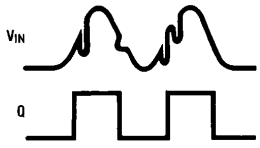

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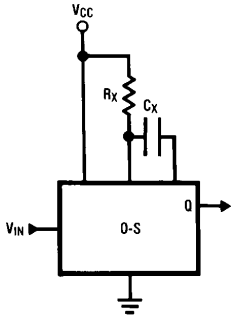
FIGURE 10b. Schmitt Trigger



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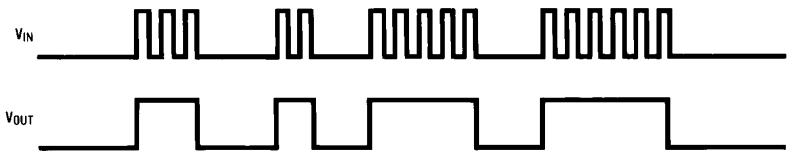

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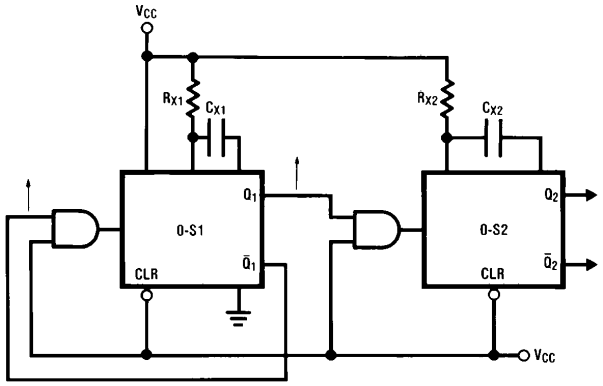
FIGURE 10a. Envelope Detector (Retriggerable Device Required)

PULSE GENERATOR *(Figure 11)*

Two one-shots can be connected together to form a pulse generator capable of variable frequency and independent duty cycle control. The R_{X1} and C_{X1} of O–S1 determine the frequency developed at output Q_1. R_{X2} and C_{X2} of O–S2 determine the output pulse width at Q_2. (Retriggerable device required.)



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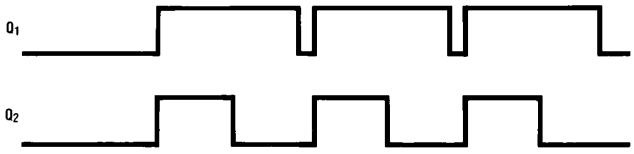

$$\text{DUTY CYCLE} = \frac{R_{X2}\,C_{X2}}{R_{X1}\,C_{X1}}$$

$$\text{FREQ} = \frac{1}{K\,R_{X1}\,C_{X1}}$$

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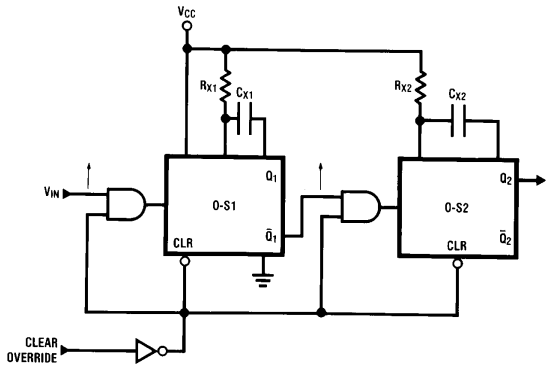
FIGURE 11. Pulse Generator (Retriggerable Device Required)

Note: K is the multiplication factor dependent of the device. Arrow indicates edge-trigger mode.

DELAYED PULSE GENERATOR WITH OVERRIDE TO TERMINATE OUTPUT PULSE *(Figure 12)*

An input pulse of a particular width can be delayed with the circuit shown in *Figure 12*. Preselected values of R_{X1} and C_{X1} determine the delay time via O–S1, while preselected values of R_{X2} and C_{X2} determine the output pulse width through O–S2. The override input can additionally serve to modify the output pulse width.



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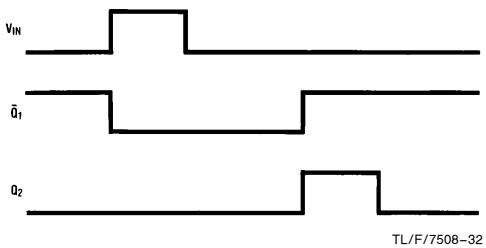

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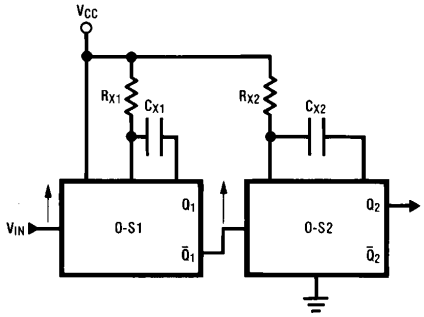
FIGURE 12. Delayed Pulse Generator with Override to Terminate Output Pulse

MISSING PULSE DETECTOR ***(Figure 13)***

By setting the time constant of O–S1 through R_{X1} and C_{X1} to be the least one full period of the incoming pulse period, the one-shot will be continuously retriggered as long as no missing pulse occurs. Hence, $\overline{Q}_1$ remains LOW until a pulse is missing in the incoming pulse train, which then triggers O–S2 and produces an indicating pulse at Q_2. (Retriggerable device required.)



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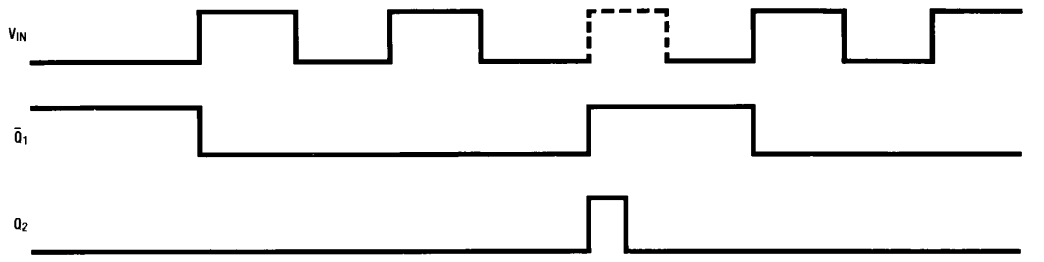

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FIGURE 13. Missing Pulse Detector (Retriggerable Device Required)

PULSE WIDTH DETECTOR ***(Figure 14)***

The circuit of *Figure 14* produces an output pulse at V_{OUT} if the pulse width at V_{IN} is wider than the predetermined pulse width set by R_X and C_X.

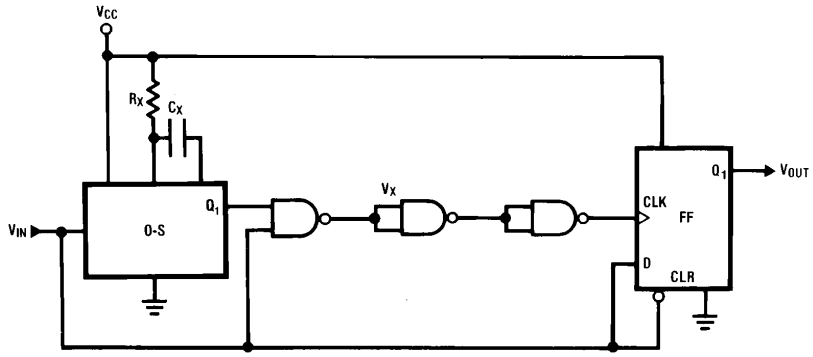

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FIGURE 14. Pulse Width Detector

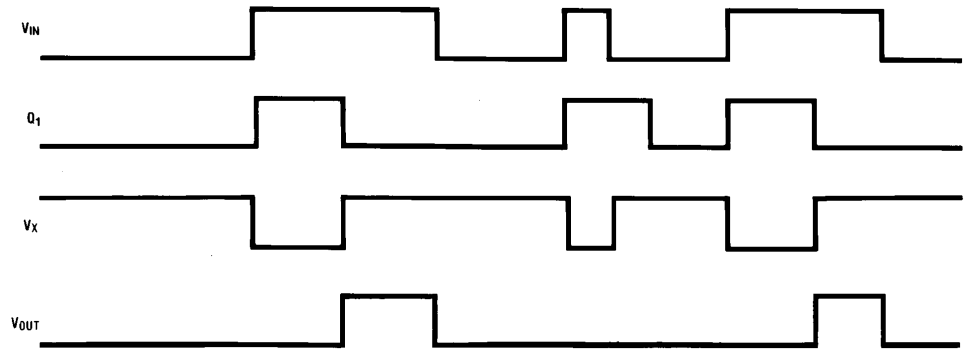

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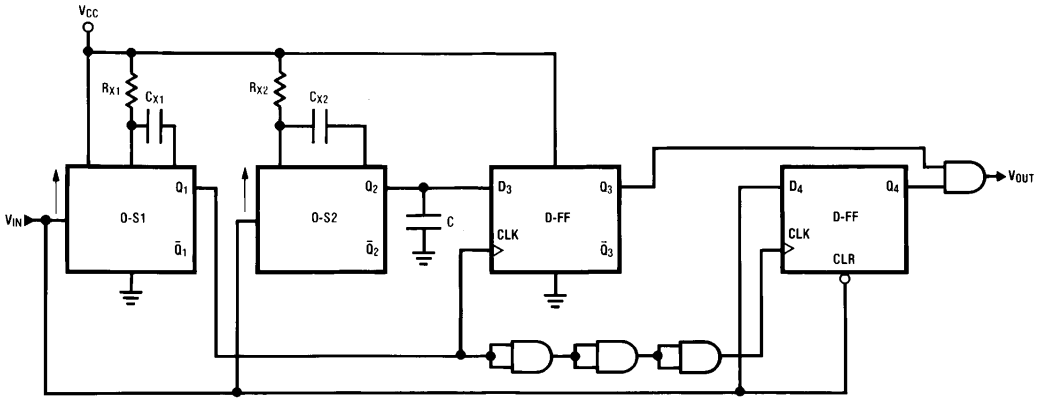
FIGURE 14. Pulse Width Detector (Continued)

BAND PASS FILTER ***(Figure 15)***

The band pass of the circuit is determined by the time constants of the two low-pass filters represented by O-S1 and O-S2. With the output at Q_2 delayed by C, the D-flip flop (D-FF) clocks HIGH only when the cutoff frequency of O-S2 has been exceeded. The output at Q_3 is gated with the delayed input pulse train at Q_4 to produce the desired output. (Retriggerable device required.)



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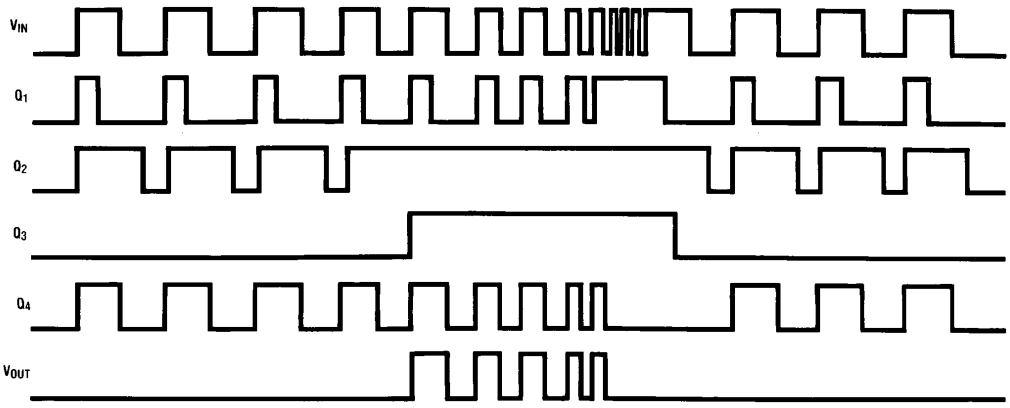

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FIGURE 15. Band Pass Filter (Retriggerable Device Required)

FM DATA SEPARATOR *(Figure 16)*

The data separator shown in *Figure 16* is a two-time constant separator that can be used on tape and disc drive memory storage systems. The clock and data pulses must fall within prespecified time windows. Both the clock and data windows are generated in this circuit. There are two data windows; the short window is used when the previous bit cell had a data pulse in it, while the long window is used when the previous bit cell had no data pulse.

If the data pulse initially falls into the data window, the —SEP DATA output returns to the NAND gate that generates the data window, to assure that the full data is allowed through before the window times out. The clock windows will take up the remainder of the bit cell time.

Assume all one-shots and flip-flops are reset initially and the +READ DATA has the data stream as indicated. With O–S1 and O–S2 inactive, +CLK WINDOW is active. The first +READ DATA pulse will be gated through the second AND gate, which becomes —SEP CLK for triggering of the R–S FF and the one-shots. With the D–FF off, O–S1 will remain reset. The —SEP CLK pulse will trigger O–S2, whose output is sent to the OR gate, and its output becomes +DATA WINDOW to enable the first AND gate. The next pulse on +READ DATA wil be allowed through the first AND gate to become —SEP DATA. This pulse sets the R–S FF, whose HIGH output becomes the data to the D–FF. The D–FF is clocked on by O–S2 timing out and +CLK WINDOW becoming active. $\overline{Q}_4$ will hold O–S2 reset and allow O–S1 to trigger on the next clock pulse.

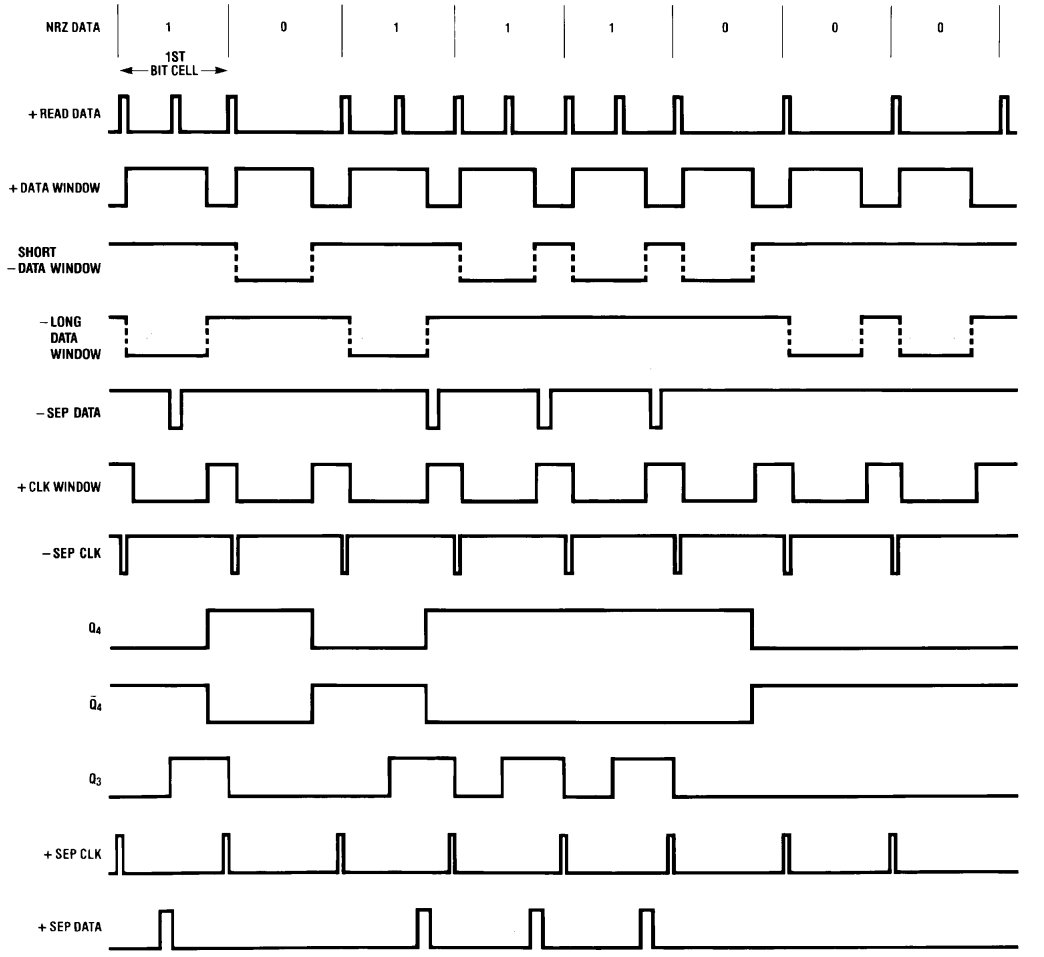

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FIGURE 16. FM Data Separator

The next clock pulse (the second bit cell) is ANDed with +CLK WINDOW and becomes the next —SEP CLK, which will reset the R–S FF and trigger O–S1. As O–S1 becomes active, the +DATA WINDOW becomes active, enabling the first AND gate. With no data bit in the second bit cell, the R–S FF will remain reset, enabling the D–FF to be clocked off when +DATA WINDOW falls. When the D–FF is clocked off, Q_4 will hold O–S1 reset and allow O–S2 to be triggered.

The third clock pulse (bit cell 3) is ANDed with +CLK WINDOW and becomes —SEP CLK, which continues resetting the R–S FF and triggers O–S2. When O–S2 becomes active, +DATA WINDOW enables the first AND gate, allowing the data pulse in bit cell 3 to become —SEP DATA. This —SEP DATA will set the R–S FF, which enables the D–FF to be clocked on when +DATA WINDOW falls. When this happens, Q_4 will hold O–S2 reset and allow O–S1 to trigger. This procedure continues as long as there is clock and data pulse stream present on the +READ DATA line.

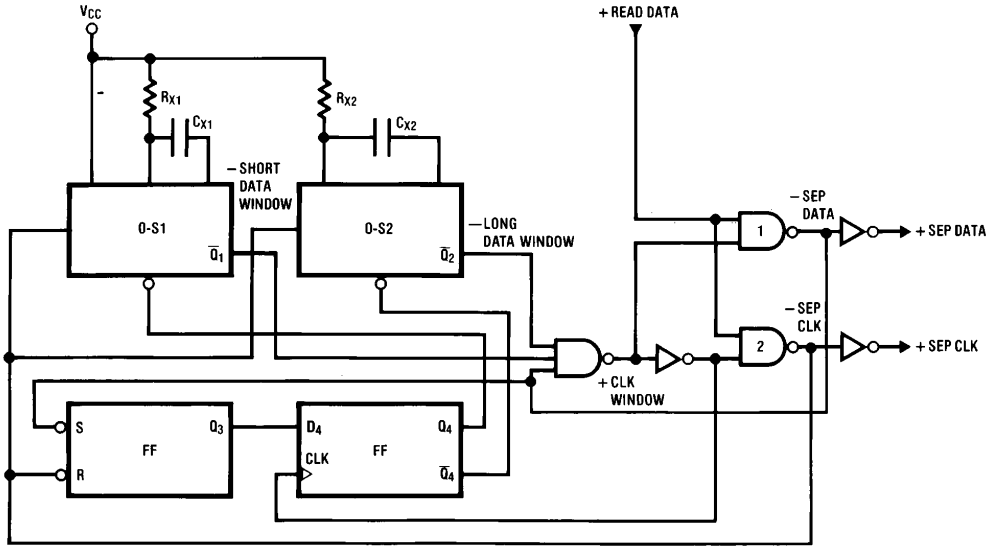

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FIGURE 16. FM Data Separator (Continued)

PHASE-LOCKED LOOP VCO *(Figure 17)*

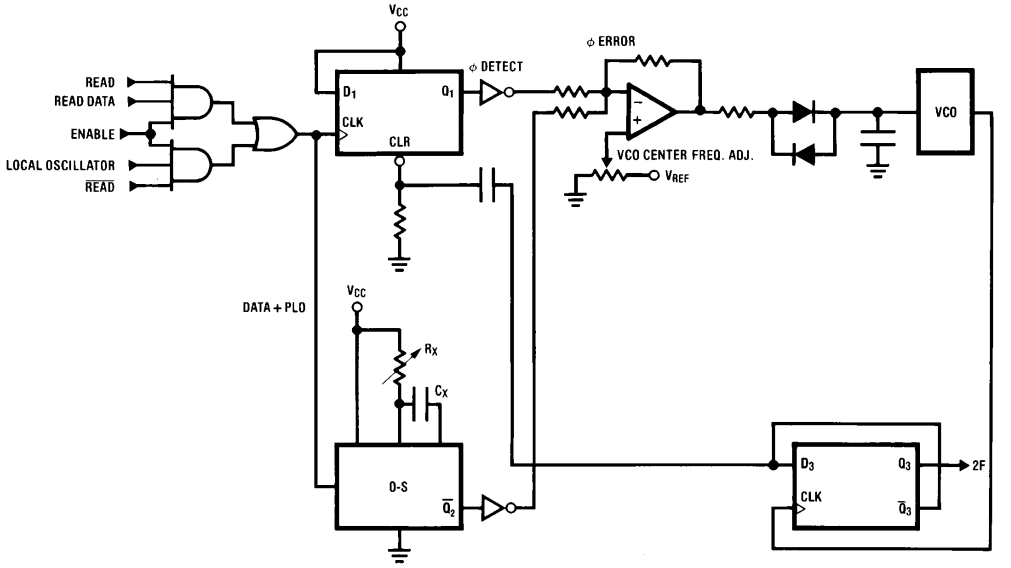
The circuit shown in *Figure 17* represents the VCO in the data separation part of a rotational memory storage system which generates the bit rate synchronous clocks for write data timing and for establishing the read data windows.

The op-amp that performs the phase-lock control operates by having its inverting input be driven by two sources that normally buck one another. One source is the one-shot, the other source is the phase detector flip-flop. When set, the one-shot, through an inverter, supplies a HIGH-level voltage to the summing node of the op-amp and the phase detector FF, also through an inverter, supplies a canceling LOW-level input.

It is only when the two sources are out of phase with each other, that is one HIGH and the other LOW, that a positive- or negative-going phase error will be applied to the op-amp to effect a change in the VCO frequency. *Figure 17* illustrates the process of phase-error detection and correction when synchronizing to a data bit pattern. The rising edge of each pulse at DATA+PLO clocks the one-shot LOW and the phase detector FF HIGH. Since both outputs are still bucking each other, no change will be observed at the phase-error summing node. When the one-shot times out, if this occurs after the 2F clock has reset the phase detector FF to a LOW output, a positive pulse will be seen at the summing node until both the one-shot and the FF are reset. Any positive pulse will be reflected by a negative change in the op-amp output, which is integrated and reduces the positive control voltage at the VCO input in direct proportion to the duration of the phase-error pulse. A negative phase-error pulse occurs when the phase detector FF remains set longer than the one-shot.

Negative phase-error pulse causes the integrated control voltage to swing positive in direct proportion to the duration of the phase-error pulse. It is recommended that a clamping circuit be connected to the output of the op-amp to prevent the VCO control voltage from going negative or more positive than necessary. A back-to-back diode pair connected between the op-amp and the VCO is highly recommended, for it will present a high impedance to the VCO input during locked mode. This way, stable and smooth operation of the PLO circuit is assured.

2F Bit Rate Synchronous Read/Write Clock



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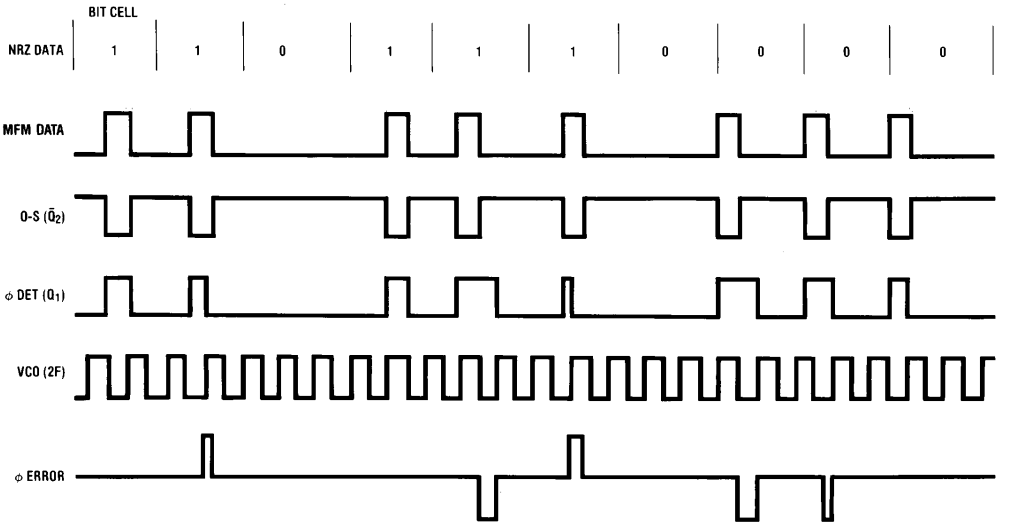

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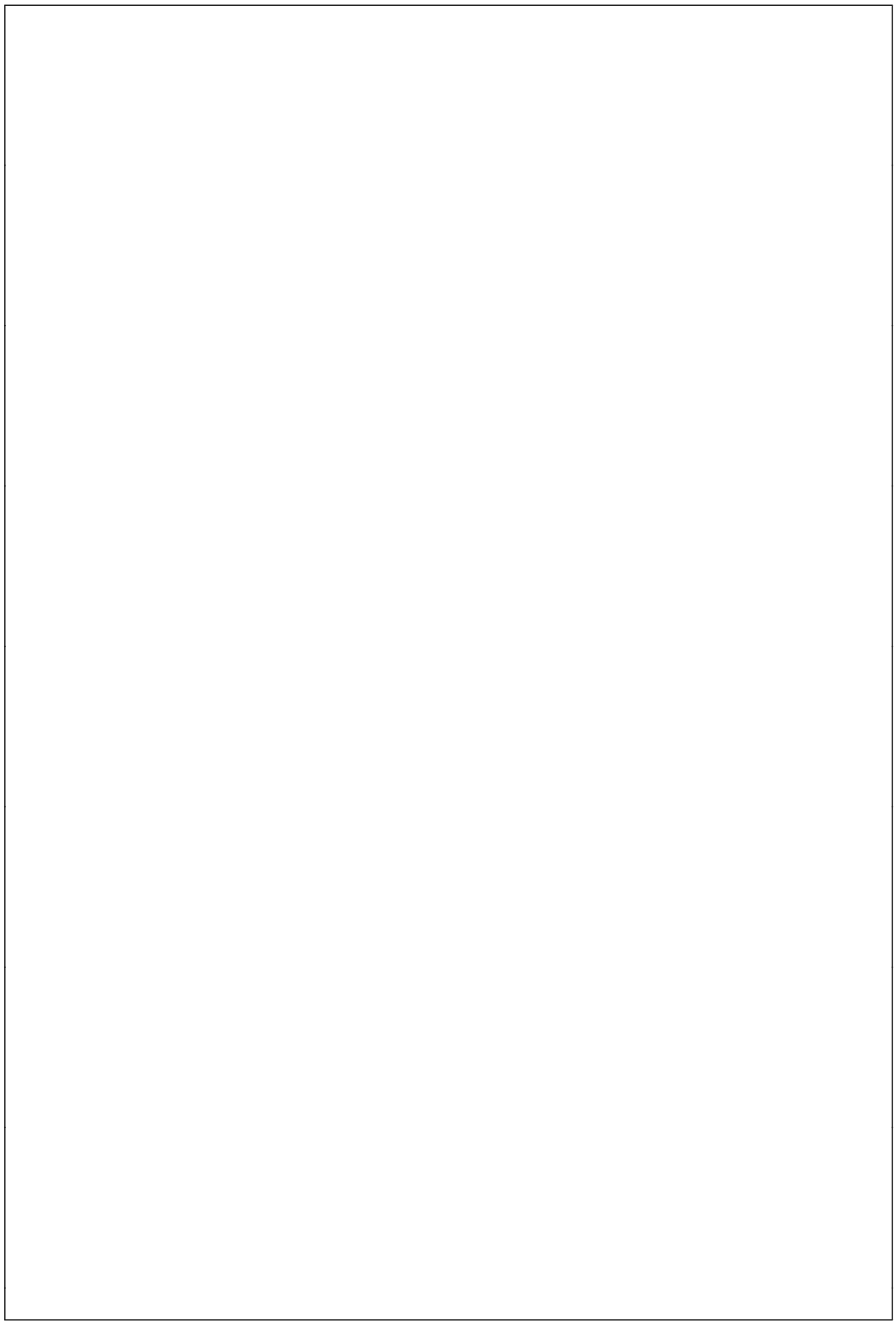
FIGURE 17. Phase-Locked Loop Voltage Controlled Oscillator

A FINAL NOTE

It is hoped that this brief note will clarify many pertinent and subtle points on the use and testing of one-shots. We invite your comments to this application note and solicit your constructive criticism to help us improve our service to you.

ACKNOWLEDGEMENT

The author wishes to thank Stephen Wong, Bill Llewellyn, Walt Sirovy, Dennis Worden, Stephen Yuen, Weber Lau, Chris Henry and Michelle Fong for their help and guidance.



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