M6800 Microcomputer

System Design Data

MOTOROLA

THE M6800 MICROCOMPUTER SYSTEM

The Motorola approach to practical microprocessor system implementation consists of:

- An interactive family of LSI semiconductor components with which to build microcomputer-based systems;
- A pervasive complement of design and evaluation tools;
- A growing line of peripheral equipment;
- An extensive library of functional and diagnostic software.

This comprehensive combination of hardware and software is augmented by a series of technical information manuals, a continuing program of customer training courses, and a team of systems application engineers that facilitate design and implementation of M6800-based systems.

M6800 SEMICONDUCTOR COMPONENTS

The semiconductor components for the M6800 System are described in the following pages. Specific features of an M6800-based microcomputer design include:

- Single +5 volt power supply for system design simplicity and low cost
- Easily expandable architecture
- Repertoire of 72 powerful, variable-length instructions
- Three-state bus controls for maximum system flexibility
- Microcomputer family concept employing dynamically programmable/bus compatible I/O functions
- 65K bytes of address capability
- High throughput, with clock rates to 1 MHz

M6800 DESIGN AND EVALUATION TOOLS

EXORciser

The EXORciser is a hardware/software design, evaluation and diagnostic instrument. With its three basic modules, plus one or more of a series of optionally available plug-in accessory modules, it permits rapid emulation of any M6800-based microcomputer design. Built-in firmware (EXbug) allows the user to evaluate the performance of his software, the M6800 components, or the user's random logic designs. The EXORciser also provides the nucleus of a cost-effective system for development and debugging of M6800 software.

Evaluation Module

The Evaluation Module provides a basic microcomputer built from M6800 components and board-mounted for convenient utilization. Each card contains all necessary components, except power supply, for the functional evaluation of M6800 components and permits running of user test programs via the bootstrap firmware designed into the unit.

M6800 Design Evaluation Kit II

The MEK6800D2 Kit provides a useful and expandable tool for those who wish to develop systems with the MC6800 microprocessor without investing in expensive terminals. All parts needed to complete the system and get on the air are provided in the kit with the exception of the power supply. In addition to the expansion available on the basic microcomputer module, additional RAM, ROM, and I/O parts can be accommodated at a later date to implement more complex systems. Machine language programs can be entered through the system keyboard or via a built-in audio cassette interface system. Hexadecimal LED displays are provided for monitoring data and address information. A crystal-controlled clock generator is used to eliminate timing adjustments.

M6800 PERIPHERAL EQUIPMENT

Trademarked EXORdisk and EXORtape, these two powerful peripherals are designed specifically for use in conjunction with the M6800 EXORciser. The versatile floppy disk (EXORdisk) is available with one to four disk drives and contains 256,256 bytes per diskette. The high-speed paper-tape reader (EXORtape) loads up to 250 characters per second into the EXORciser. This is 25 times faster than a standard ASR-33 teletype.

M6800 SUPPORT SOFTWARE

Support Software for the M6800 is available in three forms to assist the user in generating the specific programs he ultimately wishes to implement with his M6800 system design:

Resident Software — designed to work in conjunction with the EXORciser to permit real-time development of system software in an emulated final microcomputer system. Provides the lowest program development cost where several M6800 microcomputer designs are contemplated over a period of time.

Time-Sharing System — provides a software package that permits immediate utilization of a variety of national and international time-share computers for development of the M6800 program. Recommended where maximum capability at low initial cost is required.

In-House Computer System — basic programs that permit M6800 system program development on in-house computers having FORTRAN IV capability and upward of 25K words of memory. Recommended for companies which are simultaneously running many large M6800 projects.

M6800 SUPPORT LITERATURE

Key support documents which supplement the integrated circuit data sheets in this brochure include :

M6800 Microprocessor Applications Manual — a comprehensive 714-page manual describing in detail the operation and applications of the M6800 Family of microcomputer building blocks. Included are system organization, programming techniques, I/O and peripheral control techniques, family hardware characteristics, and system design and development. ($25.00)

M6800 Programming Manual — a detailed 300-page guide defining the specific hardware and software properties of the MC6800 Microprocessor, and showing how to control the execution of its programmable instructions. Actual program examples are used to show how to build sequences and subroutines that perform useful (and often complex) functions. ($10.00)

M6800 Support Products Brochure — description and data on the design and evaluation hardware, the peripheral equipment, and the software and firmware used with the M6800 Microprocessor system.

Support Software Brochures — a series of 6-page documents providing sample programs and editing features for use with the following support hardware and timesharing systems:

M6800 EXORciser
GE (General Electric Information Services International Network)
GE Background (Remote batch processing)
UCS (United Computing's Multiple Access Remote Computing Service)

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Second Printing

THE M6800 MICROCOMPUTER FAMILY

INTRODUCTION

The M6800 family of parts has been designed to set the standard for microcomputer system architectures. One of the initial goals was to minimize the number of required components and support packages. This was accomplished by designing the MC6800 Microprocessor with the total system problem in mind. All microprocessor systems require some form of static or dynamic memory. This re-requirement was fulfilled by the 1024 x 8-bit ROM (MCM6830AL) and the 128 x 8-bit RAM (MCM6810AL). The need for specialized data transfer functions was realized early, which lead to the Peripheral Interface Adapter (MC6820) as well as several others which are in various design stages. The M6800 system is attractive to the system user because these peripheral parts appear to the microprocessor as simply memory locations on the address and data bus. They are completely programmable from the bus and their real time status is available through the bus. This architecture accomplished several things at the system level. First, it simplified the interface between memory and peripheral parts and, second, it eliminated the use for I/O instructions; both of these features increase system throughput.

Other attractive features of the M6800 family are that the output buffers are capable of driving standard TTL and only one power supply is required (+5 volts). The V_{CC} power supply required by most MOS designs has been eliminated. This means the M6800 family can directly interface with standard TTL logic without the need for additional power supplies.

The intent of this specification is to define in detail the M6800 system architecture. This includes defining a minimum system and discussing requirements of complex systems. It also includes a discussion of the static and dynamic interaction between the microprocessor, memories and peripherals. This leads to static and dynamic specifications on the M6800 data bus and address bus. Further, it includes a discussion and specification of the microprocessor clocks and how they interact with the system and a definition of the microprocessor control lines such as Three-State Control, Halt, Normal Interrupt, Non-Maskable Interrupt and how they are implemented in a system environment. And finally, it includes a description of what occurs on the circuit interfaces during instruction execution.

SYSTEM COMPONENT DESCRIPTIONS

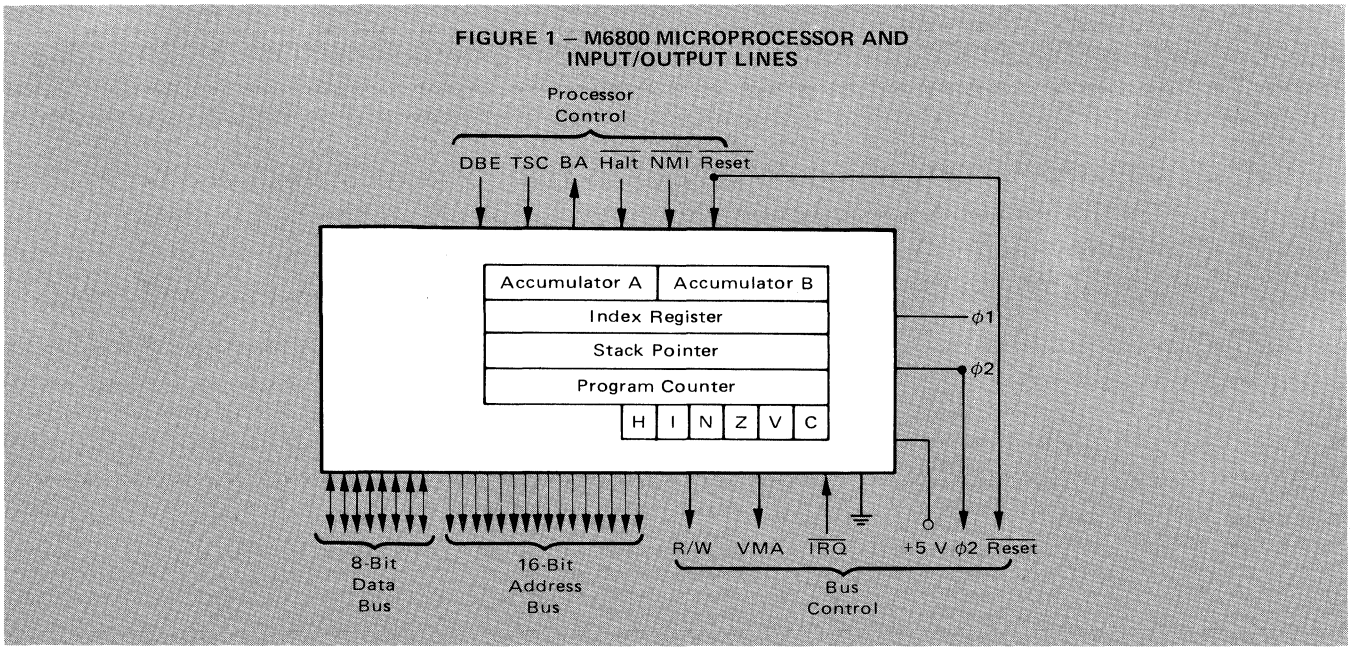
Before discussing the M6800 system, a general description of the MC6800 microprocessor, the 1024 x 8-bit ROM, the 128 x 8-bit RAM, the PIA and the ACIA is needed, as well as a detailed description of the microprocessor and peripheral input/output lines.

MC6800 Microprocessor General Description

A symbolic diagram of the microprocessor and its input/output is shown in Figure 1. The processor is a bi-directional, bus-oriented, 8-bit parallel machine with 16 bits of address. For most systems, depending on interconnection capacitance, the processor is capable of directly interfacing with eight peripheral parts and one TTL load on the same bus at a 1 MHz minor cycle clock rate. For systems requiring additional peripheral parts, a Data Bus Extender (BEX) is available.

The processor has two 8-bit accumulators which are used to hold operands and results from the Arithmetic

FIGURE 1 – M6800 MICROPROCESSOR AND INPUT/OUTPUT LINES



Logic Unit (ALU). The 16-bit index register stores 16 bits of memory address for the index mode of memory addressing. The stack pointer is a two byte (8 bits/byte) register that contains the address of the next available location in an external push-down/pop-up stack. This stack is normally a random access read/write memory that may have any location (address) that is convenient. In those applications that require storage of information in the stack when power is lost, the stack must be non-volatile. The program counter is a 16-bit register that contains the program address. And finally, a condition code register (flag register) contains six bits of condition codes. The condition codes indicate the results of an ALU operation: Negative (N), Zero (Z), Overflow (V), Carry from bit 7 (C), and Half carry from bit 3 (H). These bits of the Condition Code Register are used as testable conditions for the conditional branch instructions. Bit 4 is the interrupt mask bit (I). The unused bits of the Condition Code Register (B6, B7) are always ones.

The minimum instruction execution time is 2 microseconds. Processor control lines include Reset, which automatically restarts the processor, as well as Interrupt Request and Non-Maskable Interrupt to monitor peripheral status. Finally, there is a Three-State Control, Data Bus Enable and a Halt control line which can be used for Direct Memory Access (DMA) or multiprocessing.

MCM6810A 128 x 8-Bit RAM General Description

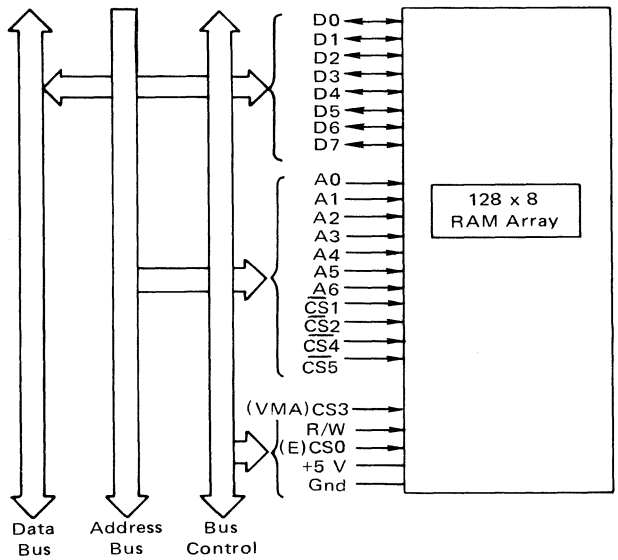
The RAM is a static memory which interfaces directly to the MC6800 microprocessor. The RAM is organized in an 8-bit byte fashion.

The RAM has six Chip Select inputs, four active low and two active high, which interface directly to the address bus.

The RAM bus interface shown in Figure 2 demonstrates the simplicity of interface in the M6800 system. Since all M6800 components operate at the same TTL levels and with the same drive capability, the data, address, and control lines can be interconnected without adding external TTL buffers. Memory timing specifications have been set to permit simple operation at full speed with the microprocessor.

Four of the Chip Selects of the MCM6810A are used to decode the system address lines. In small and medium sized systems, this address decoding will be sufficient to distinguish all packages in the system without using any additional address decoding packages.

FIGURE 2 – MCM6810A RAM BUS INTERFACE



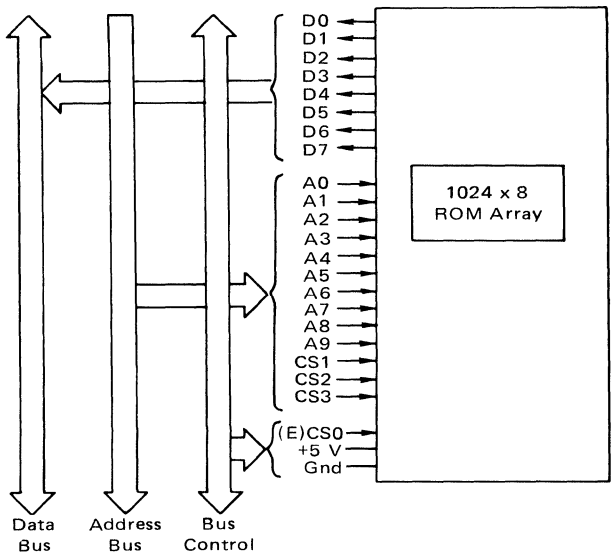
MCM6830A 1024 x 8-Bit ROM General Description

The 8K ROM is a static memory which also interfaces directly to the MC6800 microprocessor. The output drivers are level compatible with the MC6800 family. The ROM is organized in an 8-bit byte fashion similar to the RAM. It has ten Address lines and four Chip Selects.

The ROM bus interface (Figure 3) is as straightforward as that of the RAM. All outputs may be connected directly to the data bus without drivers.

Three Chip Selects (mask programmable) on the MCM6830A are used to provide address decoding in the system. In many systems, the decoding possible with these lines will be sufficient to distinguish the ROM.

FIGURE 3 – MCM6830A ROM BUS INTERFACE



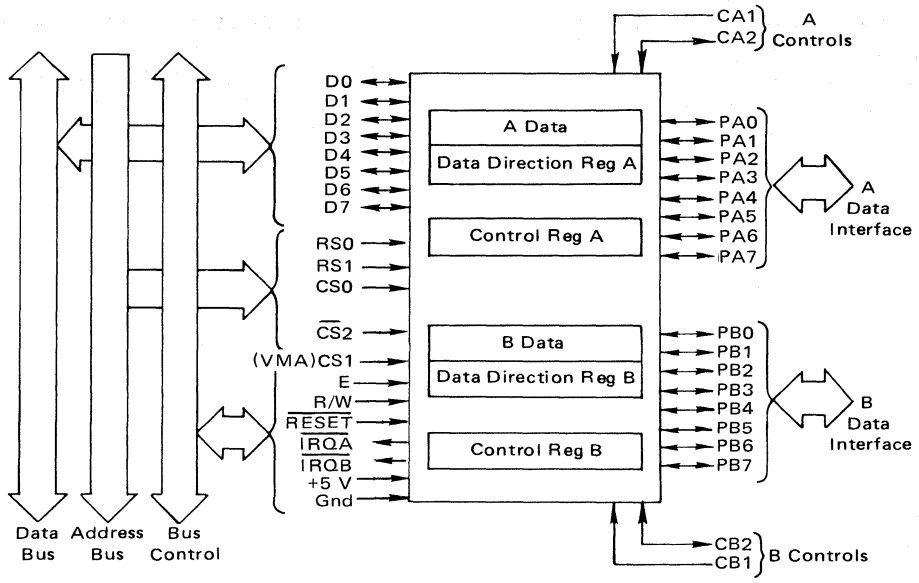
MC6820 Peripheral Interface Adapter (PIA) General Description

The MC6820 Peripheral Interface Adapter provides a universal means of interfacing peripheral equipment to the MC6800 Microprocessor through two 8-bit bi-directional peripheral data buses and four control lines. No external logic is required for interfacing to many peripheral devices.

The functional configuration of the PIA is programmed by the microprocessor during system initialization. Each of the peripheral data lines can be programmed to act as an input or output, and each of the four control/interrupt lines may be programmed for one of several control modes. This allows a high degree of flexibility in the overall operation of the interface.

Figure 4 shows the PIA system interface lines — the Data Bus lines D0–D7, Chip Selects CS0, CS1 and $\overline{CS2}$, R/W, Enable E, the Register Selects RS0 and RS1, Reset, and the Interrupt Request lines $\overline{IRQA}$ and $\overline{IRQB}$. The Data Bus lines, Chip Selects, Read/Write and Enable have the same static and dynamic characteristics as the other peripherals in the M6800 system.

FIGURE 4 – MC6820 PIA BUS INTERFACE



The Reset line is used to initialize the PIA. The Register Select lines RS0 and RS1 serve the same purpose in the PIA as address lines do in memory. They address the control and status registers, thereby making the PIA look like memory to the microprocessor.

MC6850 Asynchronous Communications Interface Adapter (ACIA) General Description

The MC6850 Asynchronous Communications Interface Adapter provides the data formatting and control to interface serial asynchronous data communications information to the MC6800 Microprocessor.

The parallel data of the bus system is serially transmitted and received (full-duplex) by the asynchronous data interface, with proper formatting and error checking. The functional configuration of the ACIA is programmed via the data bus during system initialization. A programmable Control Register provides variable word lengths, clock division ratios, transmit control, receive control, and interrupt control. Three I/O lines are provided to control external peripherals or modems. A Status Register is available to the processor, and reflects the current status of the transmitter and receiver.

Figure 5 shows the ACIA system interface lines — the Data Bus lines D0–D7, Chip Selects CS0, CS1 and $\overline{CS2}$, Read/Write, the Enable E, the Register Select RS, and the interrupt request output $\overline{IRQ}$.

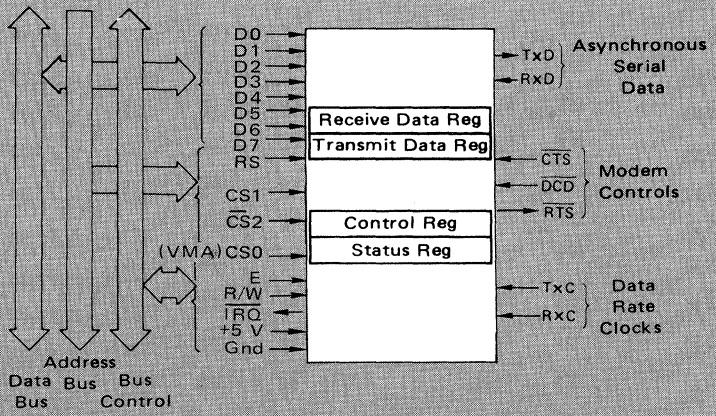
Other Peripherals

Other peripheral functions are at various stages of definition and design. All of these peripherals will be designed with the M6800 system concept in mind so that the same high degree of flexibility and compatibility is maintained.

MICROPROCESSOR INTERFACE LINES

The microprocessor input/output is broken into three groups: the bus interface lines, the bus control lines and the processor control lines. Description of bus interface and bus control lines are covered here. A description of the MPU control lines such as Halt and Data Bus Enable are covered later.

FIGURE 5 – MC6850 ACIA BUS INTERFACE



Microprocessor Address Bus Lines (A0–A15)

Sixteen pins are used for the address bus. The outputs are three-state bus drivers. When the output is turned off, it is essentially an open circuit. This permits the MPU to be used in DMA applications. Putting TSC in its high state forces the address bus and R/W lines to go into the three-state mode.

Microprocessor Data Bus Lines (D0–D7)

Eight pins are used for the data bus. It is bi-directional, transferring data to and from the memory and peripheral devices. The three-state drivers can be put into the three-state mode by forcing DBE low.

Microprocessor Clock Inputs
Phase One and Phase Two (ϕ1, ϕ2)

Two pins are used for a two-phase non-overlapping clock.

Microprocessor Read/Write Line (R/W)

The Read/Write line is an output which signals the peripheral and memory devices whether the MPU is in a Read (high) or Write (low) state. The normal standby state of this signal is Read (high). Three-State Control going high will turn Read/Write to the high impedance state. Also, when the processor is halted, it will be in the high impedance state.

Microprocessor Valid Memory Address Line (VMA)

This output indicates to peripheral devices that there is a valid address on the address bus. In normal operation, this signal should be utilized for enabling the RAM and peripheral interfaces such as the PIA and ACIA. This signal is active high. The output buffer is not three-state.

Microprocessor Interrupt Request Line ($\overline{IRQ}$)

This level-sensitive input requests that an interrupt sequence be generated within the machine when $\overline{IRQ}$ is low (Figure 13). The processor will wait until it completes the current instruction that is being executed before it recognizes the request. At that time, if the interrupt mask bit in the Condition Code Register is not set, the machine will begin an interrupt sequence. The contents of the Index Register, Program Counter, Accumulators, and Condition Code Register are stored away on the stack and the interrupt mask bit is set so no further interrupts may occur. At the end of the cycle, a 16-bit address will be placed on the address bus that points to a vectoring address which is located in memory locations FFF8 and FFF9. An address loaded at these locations causes the MPU to jump to an interrupt routine in memory.

The $\overline{Halt}$ line must be in the high state for interrupts to be serviced; interrupts will be latched internally while $\overline{Halt}$ is low. The wire-OR capability of the $\overline{IRQ}$ input requires a 3 k ohm minimum external resistor to V_{CC}.

PERIPHERAL AND MEMORY INTERFACE LINES

The peripheral and memory interface lines are the Data Bus D0–D7, the Address inputs, the Register Selects $\overline{RS0}$–$\overline{RS1}$, Chip Selects, R/W, the Enable E and Interrupt Request ($\overline{IRQ}$). A description of these follows.

Data Bus (D0–D7)

The peripheral Data Bus lines are bi-directional and capable of transferring data to and from the processor and peripheral devices. The drivers are three-state input-output buffers.

Address Inputs (A0–A15)

Sixteen Address lines are available for addressing peripherals and memories. Seven are used for addressing the internal locations of the RAM and ten are used for addressing internal locations of the ROM. The address inputs are high impedance.

Register Selects (RS0–RS1)

Register Select inputs on the peripherals such as the PIA and the ACIA are analogous to the Address inputs of the RAM and ROM. Bus address lines are tied directly to the Register Select inputs, in a minimum system configuration.

There are six locations within the PIA accessible to the microprocessor data bus: two Peripheral Registers, two Data Direction Registers, and two Control Registers. Selection of these locations is controlled by the RS0 and RS1 inputs together with CRA-2/CRB-2 in the Control Register, as shown in Table 1.

TABLE 1 – PIA INTERNAL ADDRESSING

		Control Register Bit		
RS1	RS0	CRA-2	CRB-2	Location Selected
0	0	1	X	Peripheral Register A
0	0	0	X	Data Direction Register A
0	1	X	X	Control Register A
1	0	X	1	Peripheral Register B
1	0	X	0	Data Direction Register B
1	1	X	X	Control Register B

X = Don't Care

For a functional description of these registers, see the MC6820 PIA data sheet.

The Register Select input (RS) performs a somewhat different function in the ACIA than in the PIA. The state of RS in the ACIA in conjunction with R/ W determines which of four registers will be read by the microprocessor or written into by the microprocessor, as shown in Table 2:

TABLE 2 – ACIA INTERNAL ADDRESSING

RS	R/W	Register
0	0	Control Register
0	1	Status Register
1	1	Receive Data Register
1	0	Transmit Data Register

For a functional description of these registers, see the MC6850 ACIA data sheet.

Chip Selects (CS0–CS5)

Chip Selects on the peripheral and memory devices are used to distinguish one device from another. The number of Chip Selects available varies from three on the PIA to six on the RAM. The Chip Selects may tie directly to the microprocessor address bus and VMA line in a minimum system configuration. They are high impedance inputs. The peripheral devices are enabled by various combinations of "true" and "not true" Chip Selects.

Read/Write (R/W)

The Read/ Write is a high impedance input which is used to control the direction of data flow through the processor data bus interface. When R/ W is high (MPU read cycle)

the peripheral data bus drivers are turned on and the selected location is read. When R/W is low the data bus drivers are turned off and the MPU writes into the selected location.

Enable (E)

The Enable input E is the peripheral enable signal. The E input is a high impedance input which enables the peripheral output data buffers. One of the Chip Selects is used for the E enable on the RAM and ROM.

Peripheral Interrupt Request ($\overline{IRQA}$ and $\overline{IRQB}$)

The only difference between the special function peripherals (the ACIA and PIA) and memories from a system input/output pin consideration is that the peripheral parts have interrupt outputs which are used as a request for servicing.

$\overline{IRQA}$ and $\overline{IRQB}$ from the PIA are OR tied to the system $\overline{IRQ}$ line. Since the PIA may be used to detect incoming interrupt signals on any of its control lines, this connection must be made in order to initiate the interrupt sequence at the processor. The $\overline{IRQ}$ will be pulled down by the PIA following detection of an active transition on any control line which has been enabled as a system interrupt. $\overline{IRQ}$ will be held low until the interrupt is serviced. Thus no interrupts will be lost to the system even if the interrupt mask is set at the processor.

The ACIA interrupts the microprocessor under conditions that differ from those described for the PIA. Assuming the ACIA transmitter and receiver interrupts are enabled by bits in the control register, the ACIA will interrupt the MPU if the transmitter data register is empty, the receiver data register is full or if the Data Carrier Detect input goes high indicating a loss of the Modem carrier.

STATIC AND DYNAMIC CHARACTERISTICS

Now that the microprocessor family interface has been defined, it is necessary to define the static and dynamic characteristics. Also, the microprocessor clocks, maximum ratings, power supply tolerances, temperature ranges, and test conditions will be defined. After these definitions are complete one will be able to put together a system and discuss interaction.

Static Specifications

Table 3 shows the static specifications covering the microprocessor and peripherals. The table specifies clock levels, output levels, leakages, and capacitance in one table, making all the static information available for easy use.

Dynamic Properties of the Data and Address Bus

Figure 6 and Table 4 show the dynamic characteristics of the Data and Address Bus interface. Address, Chip Selects R/W and VMA are all valid at t_{AS} (address setup time). The microprocessor then puts the address out at t_{AD} (address delay time).

The read access time $t_{ACC} = t_{AS} + t_{DDR}$, with t_{DDR} being the read data delay time. The peripheral data setup time is specified by t_{DSW}. The processor then puts data out at t_{DDW} (write data delay time). Hold time for Data Bus transfers is specified by t_H.

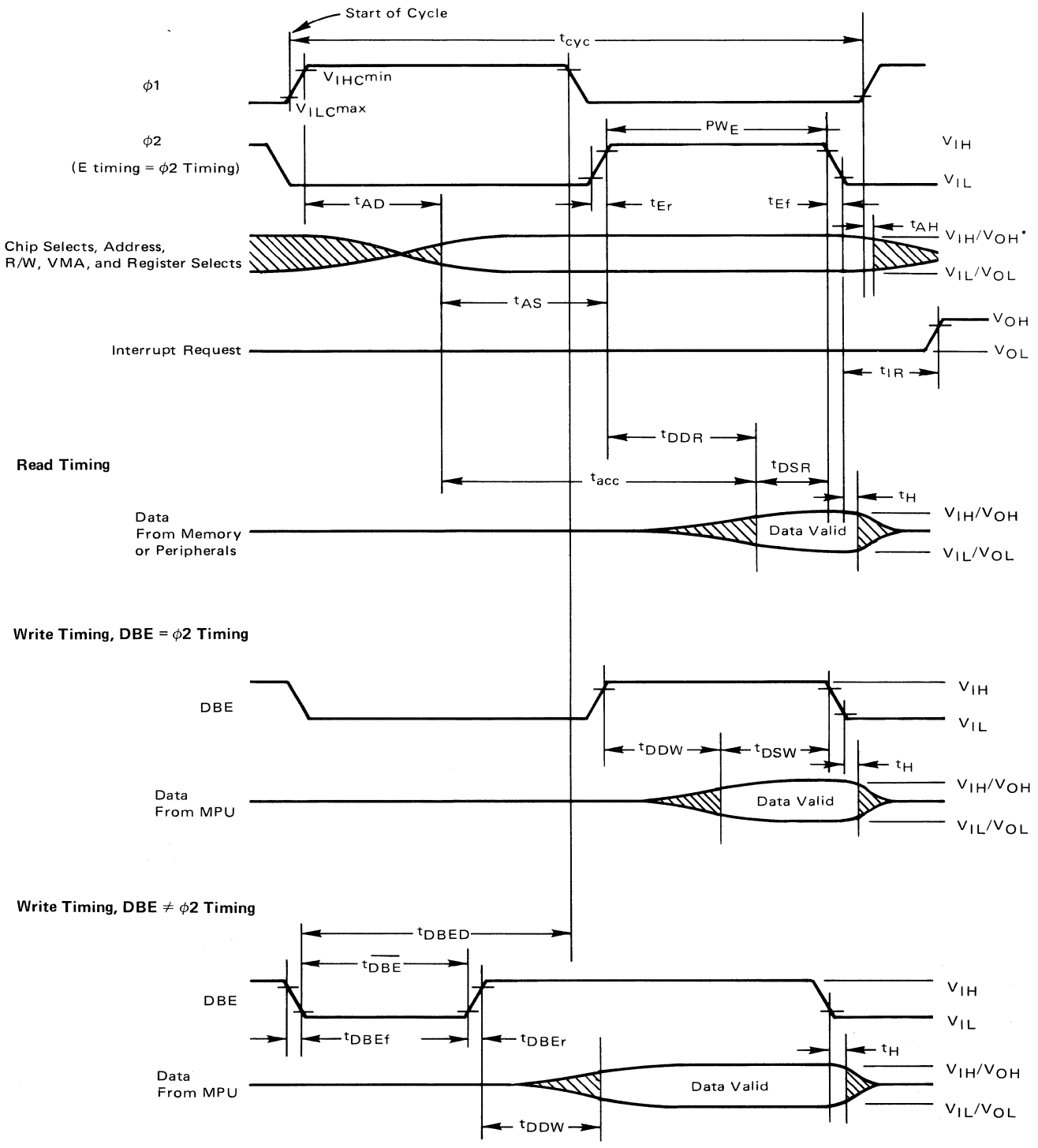
The interrupt request release time is t_{IR}. The $\overline{Interrupt\ Request}$ output driver in the peripheral parts is an open drain device. A pull up resistor is required on the $\overline{IRQ}$ line. In a minimum system, the open drain devices are all tied together and then tied to the $\overline{IRQ}$ input of the microprocessor. An interrupt is sensed by the microprocessor when $\overline{IRQ}$ is low.

TABLE 3 – STATIC CHARACTERISTICS (V_{CC} = 5.0 V ± 5%, V_{SS} = 0, T_A = 0 to 70°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Input High Voltage — All Inputs except MPU $\phi1$ and $\phi2$	V_{IH}	V_{SS} + 2.0	—	V_{CC}	Vdc
MPU $\phi1$ and $\phi2$	V_{IHC}	V_{CC} - 0.3	—	V_{CC} + 0.1	
Input Low Voltage — All Inputs except MPU $\phi1$ and $\phi2$	V_{IL}	V_{SS} - 0.3	—	V_{SS} + 0.8	Vdc
MPU $\phi1$ and $\phi2$	V_{ILC}	V_{SS} - 0.1	—	V_{SS} + 0.3	
Input Leakage Current (V_{in} = 0 to 5.25 Vdc)	I_{in}				μAdc
(V_{CC} = 5.25 Vdc) All Inputs except MPU $\phi1$ and $\phi2$		—	1.0	2.5	
(V_{CC} = 0) MPU $\phi1$ and $\phi2$		—	—	100	
Three-State (Off State) Input Current	I_{TSI}				μAdc
(V_{in} = 0.4 to 2.4 V, V_{CC} = 5.25 Vdc) D0-D7		—	2.0	10	
A0-A15, R/W		—	—	100	
Output High Voltage (V_{CC} = 4.75 Vdc)	V_{OH}	V_{SS} + 2.4	—	—	Vdc
Output Low Voltage (V_{CC} = 4.75 Vdc)	V_{OL}	—	—	V_{SS} + 0.4	Vdc
Output Leakage Current, IRQ of Peripherals (V_{in} = 2.4 Vdc)	I_{LOH}	—	1.0	10	μAdc
Capacitance* (V_{in} = 0, T_A = 25°C, f = 1.0 MHz) — MPU $\phi1$ and $\phi2$	C	80	120	160	pF
MPU TSC		—	—	15	
MPU DBE		—	7.0	10	
MPU Logic Inputs		—	6.5	8.5	
All Other Inputs		—	6.0	7.5	
D0-D7, A0-A15, R/W, VMA		—	10	12.5	
IRQ Output		—	3.0	5.0	
All Other Outputs		—	6.0	10	
$\phi1$ and $\phi2$ Overshoot/Undershoot — Input High Level	V_{OS}	V_{CC} - 0.5	—	V_{CC} + 0.5	Vdc
— Input Low Level		V_{SS} - 0.5	—	V_{SS} + 0.5	
Clock Overlap Voltage (Figure 7)	V_{OV}	—	—	0.5	Vdc

*Capacitances are periodically sampled rather than 100% tested.

FIGURE 6 – BUS INTERFACE TIMING



*Output levels of 0.4 V and 2.4 V with input levels of 0.8 V and 2.0 V guarantee a minimum 0.4 V dynamic noise immunity at "1" and "0" levels.

Data Not Valid

TABLE 4 – DYNAMIC CHARACTERISTICS (V_{CC} = 5.0 V ± 5%, V_{SS} = 0, T_A = 0 to 70°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Address Setup Time	t_{AS}	190	–	–	ns
Allowable Data Delay Time (Read)	t_{DDR}	–	200	350	ns
Memory Read Access Time	t_{acc}	–	–	540	ns
Data Setup Time (Read)	t_{DSR}	100	–	–	ns
Available Data Setup Time (Write)	t_{DSW}	225	–	–	ns
Input Data Hold Time	t_H	10	–	–	ns
Output Data Hold Time	t_H	10	30	–	ns
Address Hold Time	t_{AH}	50	75	–	ns
Address Delay	t_{AD}	–	220	300	ns
Data Delay (Write)	t_{DDW}	–	165	225	ns
Interrupt Request Release Time	t_{IR}	–	0.7	1.2	µs
Frequency of Operation	f	0.1	–	1.0	MHz
Clock Timing (ϕ1 and ϕ2)					
Cycle Time	t_{cyc}	1.0	–	10	µs
Clock Pulse Width	$PW_{\phi H}$				
(Measured at V_{CC} - 0.3 V) ϕ1		430	–	4500	ns
ϕ2		450	–	4500	ns
Clock Up Time	t_{ut}	940	–	–	ns
Rise and Fall Times ϕ1, ϕ2 (Measured between V_{SS} + 0.3 V and V_{CC} - 0.3 V)	$t_{\phi r}$, $t_{\phi f}$	5.0	–	50	ns
Delay Time or Clock Separation (Measured at V_{SS} + 0.5 V)	t_d	0	–	9100	ns
Overshoot Duration	t_{OS}	0	–	40	ns
E Enable Pulse Width	PW_E	0.45	–	25	µs
E Enable Rise and Fall Time	t_{Er}, t_{Ef}	–	–	25	ns
Processor Controls					
Processor Control Setup Time (Figure 12, 13, 14, 15)	t_{PCS}	200	–	–	ns
Processor Control Rise and Fall Time (Figures 12, 13, 14, 15)	t_{PCr}, t_{PCf}	–	–	100	ns
Bus Available Delay (Figure 15)	t_{BA}	–	–	300	ns
Three State Enable (Figure 16)	t_{TSE}	–	–	40	ns
Three State Delay (Figure 16)	t_{TSD}	–	–	700	ns
Data Bus Enable Down Time During ϕ1 Up Time (Figure 6)	$t_{\overline{DBE}}$	150	–	–	ns
Data Bus Enable Delay (Figure 6)	t_{DBED}	300	–	–	ns
Data Bus Enable Rise and Fall Times (Figure 6)	t_{DBEr}, t_{DBEf}	–	–	25	ns

Note: Dynamic properties of most of the M6800 peripheral and memory parts exceed the requirements specified above, allowing for system flexibility.

Notice the logic levels specified in Figure 6. All parts are tested to output levels of 0.4 and 2.4 V with input levels of 0.8 and 2.0 V at the specified times. This will guarantee a minimum of 0.4 V dynamic noise immunity on the "1" and "0" levels.

Microprocessor Clocks ϕ1 and ϕ2

Figure 7 shows the microprocessor clocks, and Tables 3 and 4 show the static and dynamic clock specifications. The high level is specified at V_{IHC} and the low level is specified at V_{ILC}. The allowable clock frequency is specified by f (frequency). The clock overshoot is specified by V_{OS} (overshoot voltage) for a maximum duration of t_{OS} (overshoot time). The minimum ϕ1 and ϕ2 high level pulse widths are specified by $PW_{\phi H}$ (pulse width high time). To guarantee the required access time for the peripherals, the clock up time, t_{ut}, is specified. Clock separation, t_d, is measured at a maximum voltage of V_{OV} (overlap voltage). This allows for a multitude of clock variations at the system frequency rate.

Maximum Ratings

Table 5 shows the maximum ratings. The most important specifications in the table from a user's standpoint are the operating power supply range of +4.75 V to +5.25 V and the operating temperature range of 0°C to 70°C ambient.

Test Conditions

The dynamic test load for the Data Bus, as shown in Figure 8, is 130 pF and one standard TTL load. The 11.7 kΩ resistor accounts for 205 µA of 2.4 V level leakage current. The Address, R/W and VMA processor outputs have a dynamic test load of 90 pF and one TTL load as shown in Figure 8. The 16.5 kΩ resistor accounts for 145 µA of 2.4 V level leakage current. The $\overline{\text{Interrupt Request}}$ test load is also shown in Figure 8. The load consists of a 3 kΩ resistor to V_{CC} and 100 pF of capacitance. Notice that the Data Bus lines, the Address lines, the $\overline{\text{Interrupt Request}}$ line and the E enable line are all specified and tested to guarantee 0.4 V of dynamic noise immunity on the "1" and "0" logic levels.

FIGURE 7 – MICROPROCESSOR $\phi 1$ AND $\phi 2$ CLOCKS

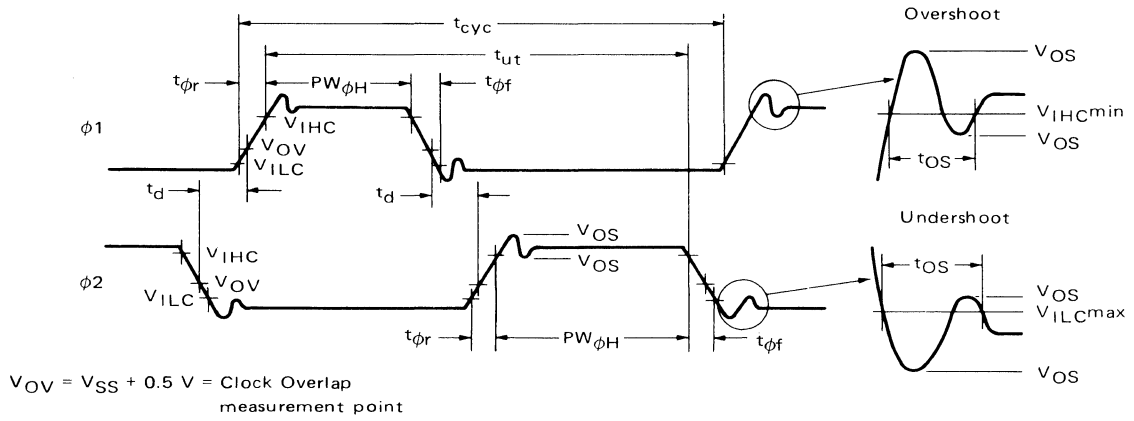
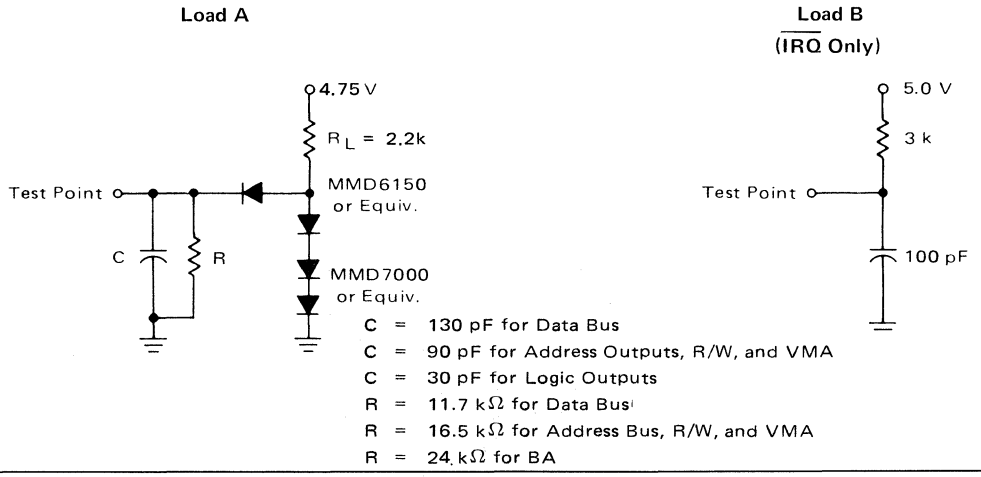


TABLE 5 – MAXIMUM RATINGS

Ratings	Symbol	Value	Unit
Supply Voltage	V_{CC}	-0.3 to +7.0	Vdc
Input Voltage	V_{in}	-0.3 to +7.0	Vdc
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	-55 to +150	°C

FIGURE 8 – TEST LOADS



A MINIMUM SYSTEM

A minimum M6800 system is defined as any size system within the basic load limitation of the MPU. Figure 9 shows a minimum system consisting of the microprocessor, three RAMs, two ROMs, two PIAs, and one ACIA. A maximum of eight peripherals are allowed on the bus in this configuration. This limitation is due to the capacitive loading specification of 130 pF on the microprocessor and peripheral data bus buffers — that is 30 pF of interconnect capacitance and 100 pF of data bus buffer capacitance.

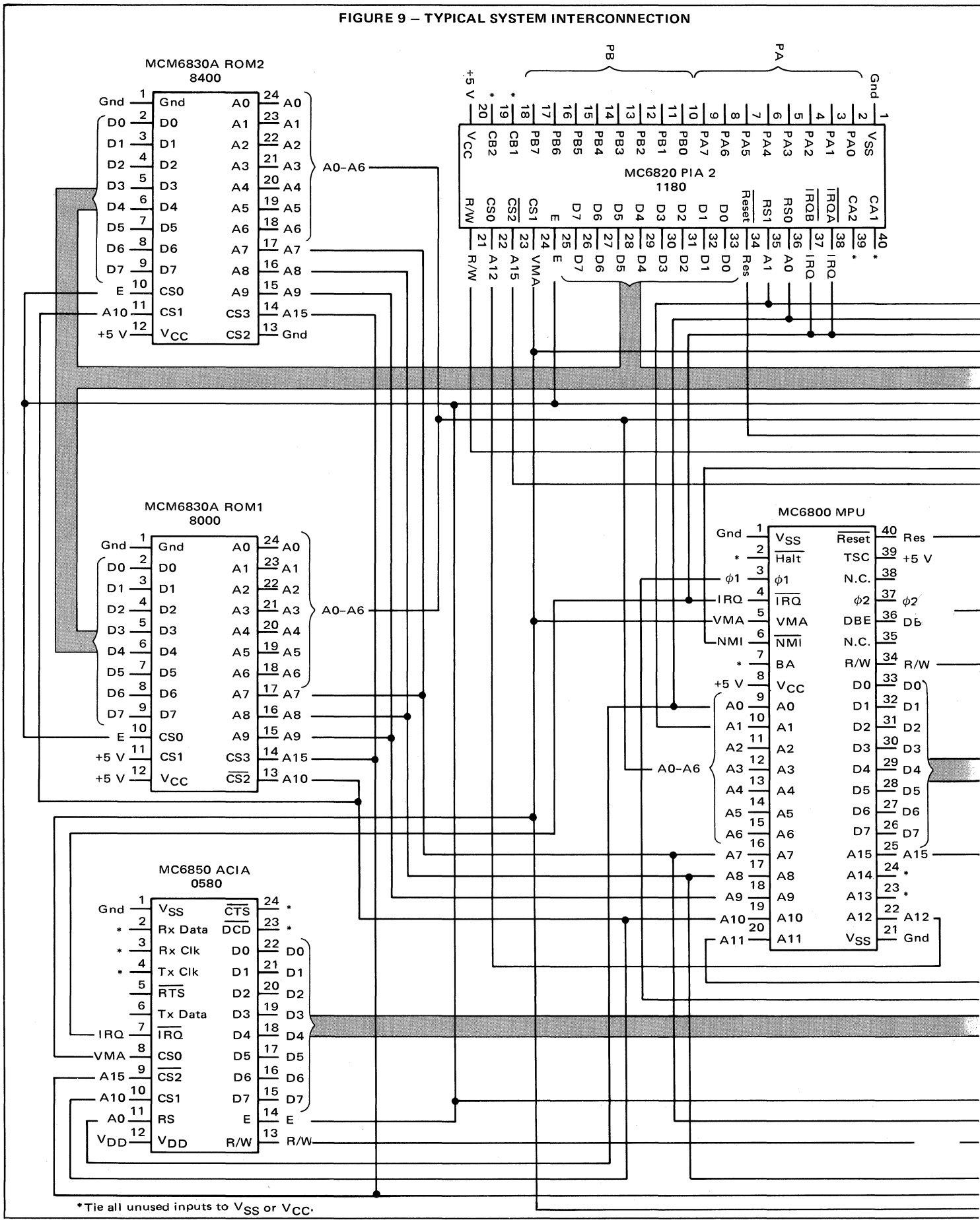
Systems having more than eight peripherals can be implemented by using the Bus Extender (BEX), additional TTL gates and the microprocessor control lines. A useful curve showing the Data Bus and Address Bus drive capability with respect to Bus loading for typical conditions is shown in Figure 10. Data Bus buffer and Address Bus buffer delays typically increase at a rate of 0.5 ns/pF for pure capacitive loading.

System Clock

The microprocessor requires two clocks, $\phi 1$ and $\phi 2$, as shown in Figure 9. A third clock, the E enable, which is in phase with $\phi 2$, is needed to transfer data to peripherals. Data transfers to the processor are made during the $\phi 2$ time. The $\phi 2$ clock is also tied to the microprocessor Data Bus Enable (DBE) which enables the Data Bus output buffers.

The write timing for this condition is shown in Figure 6 (DBE = $\phi 2$) and Table 4. If additional data setup or hold time is required on an MPU write, the DBE down-time can be decreased as shown in Figure 6 (DBE $\neq \phi 2$). The minimum down-time for DBE is $t_{\overline{DBE}}$ as shown in Table 4,

FIGURE 9 – TYPICAL SYSTEM INTERCONNECTION



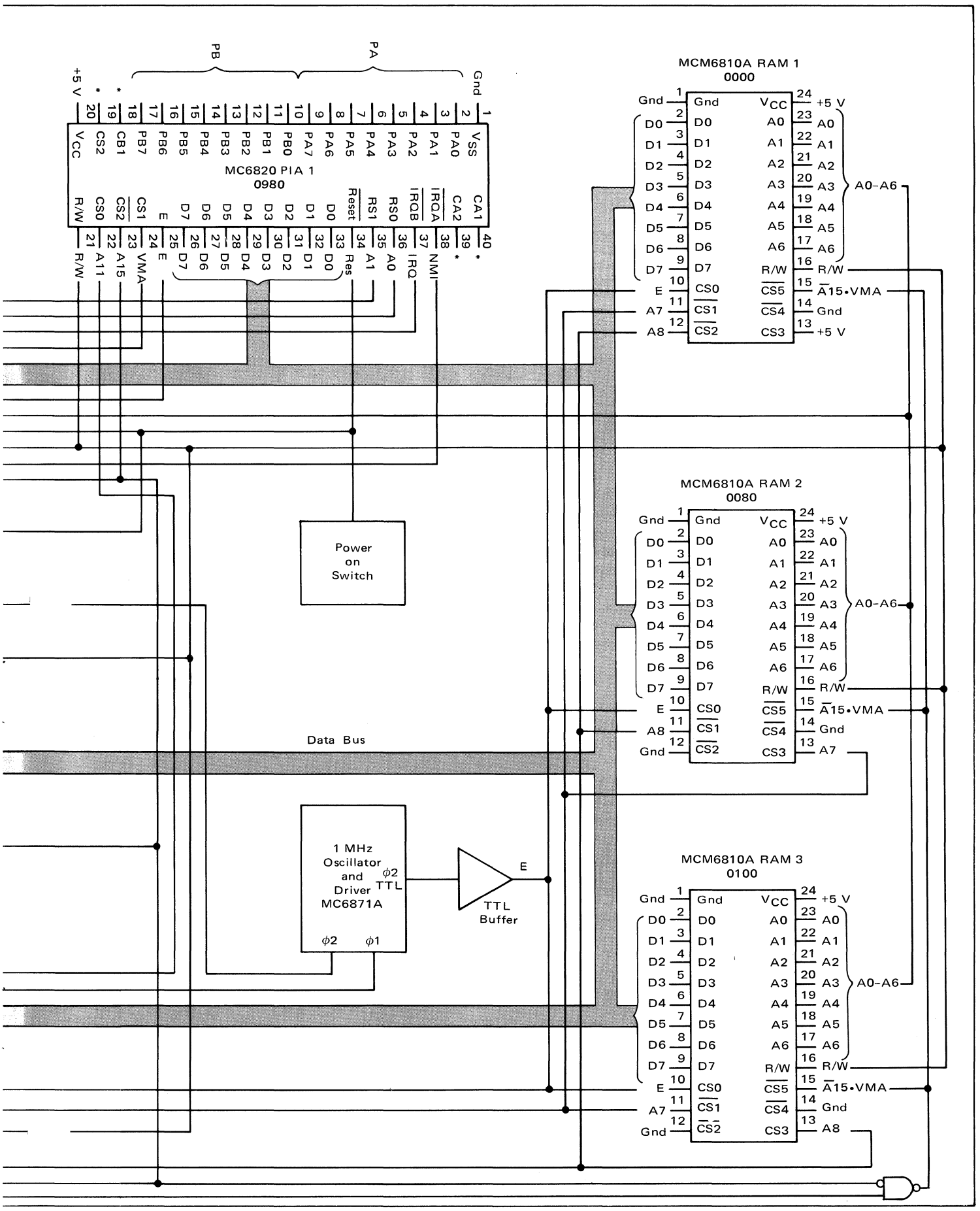
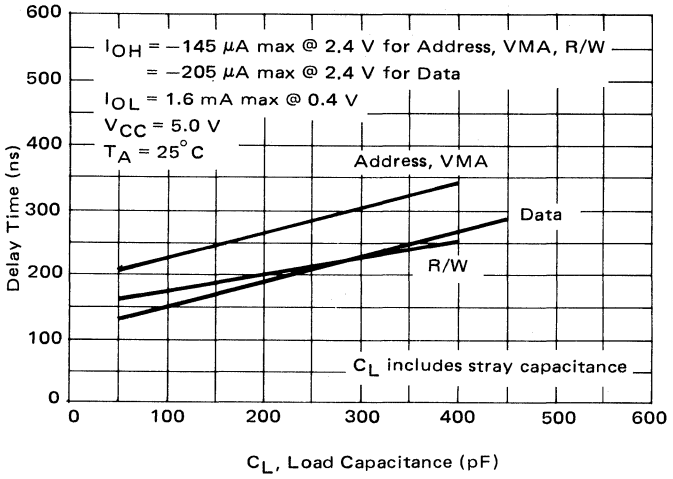

MC6820 PIA 1
0980
PB
PA
MCM6810A RAM 1
0000
MCM6810A RAM 2
0080
MCM6810A RAM 3
0100
A0-A6
R/W
A15•VMA
Power
on
Switch
Data Bus
1 MHz
Oscillator
and
Driver
MC6871A
TTL
Buffer

FIGURE 10 – TYPICAL BUS DELAY TIMES versus CAPACITIVE LOADING



and must occur within $\phi 1$ up-time. The minimum delay from the trailing edge of DBE to the trailing edge of $\phi 1$ is t_{DBED}. By skewing DBE with respect to E in this manner, data setup or hold time can be increased.

The capacitive drive requirement for the E enable line for this system is 90 pF — 60 pF for peripheral E input capacitance and 30 pF for interconnections. The MC6871A clock circuit provides $\phi 1$ and $\phi 2$ signals which meet the MPU requirements. It also provides a TTL compatible E enable output ($\phi 2$, TTL) which leads $\phi 2$ by approximately one TTL driver circuit stage delay. In the system shown, the Data Bus buffers go to their three-state mode with the trailing edge of $\phi 2$ and E allowing for sufficient hold time ($\approx$ 300 ns). In systems having TTL loads on the Data Bus, E can be tied to DBE. Variations between E and $\phi 2$ do not affect the processor or peripheral Data Bus hold time requirements providing the trailing edge of E occurs after the trailing edge of $\phi 2$.

Addressing Peripherals and Memory

As shown in Figure 6, all Address lines are valid by address setup time t_{AS}. The Address lines, Chip Selects and the E enable are tied to the ROM as shown in Figure 9. The Address lines required for addressing the ROMs are shown in Table 6. A true Address bit selects a true Chip Select, and an $\overline{\text{Address bit}}$ selects a $\overline{\text{Chip Select}}$. Figure 9 also shows the Address, Chip Select, E enable and R/$\overline{W}$ interconnection for the RAMs, the PIAs, and the ACIA, with Table 6 showing the Address lines required.

Notice that VMA is used as a Chip Select to the peripherals. VMA is needed because interrupts on these parts are cleared on a read of data from the peripherals. The microprocessor requires from 2 to 12 cycles to do an instruction. During those portions of an instruction in which the Data Bus is not active, the R/$\overline{W}$ line is held high, the Address lines are in an indeterminate state and the Data Bus buffers are in an indeterminate state. Thus a false read of a peripheral could occur, and if that peripheral was interrupting the microprocessor, the interrupt would be cleared. Tying VMA into one of the Chip Selects solves this problem since VMA is high only when there is a valid memory address on the Address Bus. If the $\overline{\text{Halt}}$ control line, the Wait for Interrupt (WAI) instruction, or the TSC control line is used, Address and R/$\overline{W}$ lines float, which could result in a false write into memory. If $\overline{\text{Halt}}$, TSC and WAI are required in a minimum system, a TTL AND gate is used to AND one of the chip selects with VMA as shown.

Address space was chosen as shown in Table 6 for the following reasons: When the microprocessor power comes up, the address FFFE goes out on the Address lines, followed by FFFF (the address of the start up program is stored at FFFE and FFFF). Thus, A15 was chosen to select the ROMs. The ROM Address bits are A0 thru A9. A10 was chosen as the other Chip Select so that ROM addressing would be contiguous. The ROM Chip Selects are programmable; for this example $\overline{\text{CS1}}$ and CS3 are defined as true and CS2 as not true ($\overline{\text{Chip Select}}$).

$\overline{\text{A15}}$ can be used to select all peripherals except the ROMs. The RAM Address bits are A0 thru A6. A7 and A8 make the address space for the RAMs contiguous.

When using direct addressing, the Address Bus high bits (A8 thru A15) are all zeros. Then RAM 1 and RAM 2 in Table 6 form 256 contiguous locations for direct addressing. When selecting the ACIA and PIAs, the RAMs are deselected by keeping A7 and A8 high.

The ACIA is selected with $\overline{\text{A15}}$, VMA, and A10. A10 can be reused since the state of A15 determines whether A10 is used as a ROM Address line or the ACIA Address line. The PIAs are selected with $\overline{\text{A15}}$, VMA and two of the remaining unused address lines — A11 and A12.

TABLE 6 – ADDRESS LINES FOR SYSTEM OF FIGURE 9

Device	Address	Chip Selects	Select Code
ROM1	A0-A9	$\overline{\text{A10}}$ A15	8000
ROM 2	A0-A9	A10 A15	8400
RAM 1	A0-A6	$\overline{\text{A7}}$ $\overline{\text{A8}}$ $\overline{\text{A15}}$ VMA	0000
RAM 2	A0-A6	A7 $\overline{\text{A8}}$ $\overline{\text{A15}}$ VMA	0080
RAM 3	A0-A6	$\overline{\text{A7}}$ A8 $\overline{\text{A15}}$ VMA	0100
ACIA 1	A0	A10 VMA $\overline{\text{A15}}$ *	0580
PIA 1	A0 A1	A11 VMA $\overline{\text{A15}}$ *	0980
PIA 2	A0 A1	A12 VMA $\overline{\text{A15}}$ *	1180

*When addressing the ACIA and PIAs, A7 and A8 must be high to disable the RAMs. When addressing the RAMs, A10, A11 and A12 are held low.

MPU ADDRESS MODES

The MC6800 has a set of 72 different instructions. Included are binary and decimal arithmetic, logical, shift, rotate, load, store, conditional or unconditional branch, interrupt and stack manipulation instructions.

Table 7 shows the microprocessor instruction set. Table 8 shows the instruction addressing modes and associated execution times.

The MPU address modes are:

1. Immediate
2. Direct
3. Indexed
4. Extended
5. Implied
6. Relative
7. Accumulator (ACCX)

TABLE 7 – MICROPROCESSOR INSTRUCTION SET – ALPHABETIC SEQUENCE

ABA	Add Accumulators	CLR	Clear	PUL	Pull Data
ADC	Add with Carry	CLV	Clear Overflow	ROL	Rotate Left
ADD	Add	CMP	Compare	ROR	Rotate Right
AND	Logical And	COM	Complement	RTI	Return from Interrupt
ASL	Arithmetic Shift Left	CPX	Compare Index Register	RTS	Return from Subroutine
ASR	Arithmetic Shift Right	DAA	Decimal Adjust	SBA	Subtract Accumulators
BCC	Branch if Carry Clear	DEC	Decrement	SBC	Subtract with Carry
BCS	Branch if Carry Set	DES	Decrement Stack Pointer	SEC	Set Carry
BEQ	Branch if Equal to Zero	DEX	Decrement Index Register	SEI	Set Interrupt Mask
BGE	Branch if Greater or Equal Zero	EOR	Exclusive OR	SEV	Set Overflow
BGT	Branch if Greater than Zero	INC	Increment	STA	Store Accumulator
BHI	Branch if Higher	INS	Increment Stack Pointer	STS	Store Stack Register
BIT	Bit Test	INX	Increment Index Register	STX	Store Index Register
BLE	Branch if Less or Equal	JMP	Jump	SUB	Subtract
BLS	Branch if Lower or Same	JSR	Jump to Subroutine	SWI	Software Interrupt
BLT	Branch if Less than Zero	LDA	Load Accumulator	TAB	Transfer Accumulators
BMI	Branch if Minus	LDS	Load Stack Pointer	TAP	Transfer Accumulators to Condition Code Reg.
BNE	Branch if Not Equal to Zero	LDX	Load Index Register	TBA	Transfer Accumulators
BPL	Branch if Plus	LSR	Logical Shift Right	TPA	Transfer Condition Code Reg. to Accumulator
BRA	Branch Always	NEG	Negate	TST	Test
BSR	Branch to Subroutine	NOP	No Operation	TSX	Transfer Stack Pointer to Index Register
BVC	Branch if Overflow Clear	ORA	Inclusive OR Accumulator	TXS	Transfer Index Register to Stack Pointer
BVS	Branch if Overflow Set	PSH	Push Data	WAI	Wait for Interrupt
CBA	Compare Accumulators				
CLC	Clear Carry				
CLI	Clear Interrupt Mask				

A description of these address modes follows, with emphasis on what is occurring in each machine cycle on the Address Bus, Data Bus, R/W line and the VMA line. A cycle-by-cycle representation is shown in Figure 11. When VMA is low the Data Bus and Address Bus are in an indeterminate state. (See MC6800 data sheet for a cycle-by-cycle description of the entire instruction set.)

Immediate Addressing

Immediate addressing is an addressing technique in which the first byte of the instruction contains the operator and the second byte contains the operand. Exceptions to this are the LDS and LDX instructions which have the operand in the second and third bytes of the instruction.

Referring to Figure 11, during the first half of cycle #1 the Program Counter (PC) current address is put on the line, R/W goes high designating a read operation and VMA goes high designating the current address is a valid memory address. During the second half of cycle #1, the LDA operator code is put on the Data Bus from memory and loaded into the MPU. The MPU Program Counter is incremented and the operand, which is usually data, is loaded into the MPU on cycle #2. The operator of the next instruction follows on the next cycle.

Direct Addressing

In direct addressing, the address of the operand is contained in the second byte of the instruction. Direct addressing allows the user to directly address the lowest 256 bytes in the machine, i.e., locations zero through 255. Enhanced execution times are achieved by storing data in these locations. In most configurations, it should be a Random Access Memory.

Referring to Figure 11, the address in the Program Counter is put on the address bus and the LDA operator code is loaded into the MPU during cycle #1. The Program Counter is incremented and during cycle #2, 8 bits of address are loaded into the Address Bus Low (ABL) register which contains the lower 8 bits of the 16-bit address register of the MPU. The upper 8 bits , which are contained in the Address Bus High (ABH) register, are forced to all zeros. In the third cycle the new address is put on the Address Bus and the operand is loaded into the MPU.

A STA instruction is handled in the same manner as an LDA instruction except there is an additional cycle required, which is cycle #6 in the diagram. Due to the MPU architecture this additional cycle is required to move the accumulator internally in the machine. During this cycle the Data Bus is in an indeterminate state and VMA goes low. The actual storing of data then occurs on cycle #7. The next instruction follows as shown.

Indexed Addressing

In indexed addressing, the address contained in the second byte of the instruction is added to the index register's lowest 8 bits in the MPU. The carry is then added to the higher order 8 bits of the index register. This result is then used to address memory. The modified address is held in a temporary address register so there is no change to the index register. These are two byte instructions.

In the first two cycles of an indexed address instruction, the LDA operator code is loaded into the MPU followed by the index offset. In the third cycle the low order byte of the index register is loaded into the adder and added to the offset; the carry propagates during cycle #4. The VMA goes low during these two cycles while the MPU is preparing the indexed address. The new address then goes on the line during cycle #5.

The STA indexed instruction is handled in the same manner as the LDA instruction, again with the exception that an additional cycle is required due to the MPU architecture. VMA is held low then for three cycles for the STA instruction instead of two for the LDA instruction.

TABLE 8 – INSTRUCTION ADDRESSING MODES AND ASSOCIATED EXECUTION TIMES
(Times in Machine Cycles)

	(Dual Operand)	ACCX	Immediate	Direct	Extended	Indexed	Implied	Relative
ABA		•	•	•	•	•	2	•
ADC	x	•	2	3	4	5	•	•
ADD	x	•	2	3	4	5	•	•
AND	x	•	2	3	4	5	•	•
ASL		2	•	•	6	7	•	•
ASR		2	•	•	6	7	•	•
BCC		•	•	•	•	•	•	4
BCS		•	•	•	•	•	•	4
BEA		•	•	•	•	•	•	4
BGE		•	•	•	•	•	•	4
BGT		•	•	•	•	•	•	4
BHI		•	•	•	•	•	•	4
BIT	x	•	2	3	4	5	•	•
BLE		•	•	•	•	•	•	4
BLS		•	•	•	•	•	•	4
BLT		•	•	•	•	•	•	4
BMI		•	•	•	•	•	•	4
BNE		•	•	•	•	•	•	4
BPL		•	•	•	•	•	•	4
BRA		•	•	•	•	•	•	4
BSR		•	•	•	•	•	•	8
BVC		•	•	•	•	•	•	4
BVS		•	•	•	•	•	•	4
CBA		•	•	•	•	•	2	•
CLC		•	•	•	•	•	2	•
CLI		•	•	•	•	•	2	•
CLR		2	•	•	6	7	•	•
CLV		•	•	•	•	•	2	•
CMP	x	•	2	3	4	5	•	•
COM		2	•	•	6	7	•	•
CPX		•	3	4	5	6	•	•
DAA		•	•	•	•	•	2	•
DEC		2	•	•	6	7	•	•
DES		•	•	•	•	•	4	•
DEX		•	•	•	•	•	4	•
EOR	x	•	2	3	4	5	•	•

	(Dual Operand)	ACCX	Immediate	Direct	Extended	Indexed	Implied
INC		2	•	•	6	7	•
INS		•	•	•	•	•	4
INX		•	•	•	•	•	4
JMP		•	•	•	3	4	•
JSR		•	•	•	9	8	•
LDA	x	•	2	3	4	5	•
LDS		•	3	4	5	6	•
LDX		•	3	4	5	6	•
LSR		2	•	•	6	7	•
NEG		2	•	•	6	7	•
NOP		•	•	•	•	•	2
ORA	x	•	2	3	4	5	•
PSH		•	•	•	•	•	4
PUL		•	•	•	•	•	4
ROL		2	•	•	6	7	•
ROR		2	•	•	6	7	•
RTI		•	•	•	•	•	10
RTS		•	•	•	•	•	5
SBA		•	•	•	•	•	2
SBC	x	•	2	3	4	5	•
SEC		•	•	•	•	•	2
SEI		•	•	•	•	•	2
SEV		•	•	•	•	•	2
STA	x	•	•	4	5	6	•
STS		•	•	5	6	7	•
STX		•	•	5	6	7	•
SUB	x	•	2	3	4	5	•
SWI		•	•	•	•	•	12
TAB		•	•	•	•	•	2
TAP		•	•	•	•	•	2
TBA		•	•	•	•	•	2
TPA		•	•	•	•	•	2
TST		2	•	•	6	7	•
TSX		•	•	•	•	•	4
TSX		•	•	•	•	•	4
WAI		•	•	•	•	•	9

Note: Interrupt time is 12 cycles from the end of the instruction being executed, except following a WAI instruction. Then it is 4 cycles.

Extended Addressing

In extended addressing, the address contained in the second byte of the instruction is the 8 higher order address bits of the operand. The third byte of the instruction contains the lower 8 bits of the address. This is an absolute address in memory and these are 3 byte instructions. Extended addressing is the same as direct addressing except the address field is a full 16 bits. This means the LDA and STA instructions require an additional cycle (cycles #2 and #6) to fetch the high order 8 bits of the address. Notice that in cycle #8 VMA is low signifying the Data Bus is in an indeterminate state. This is again due to the internal architecture of the MPU.

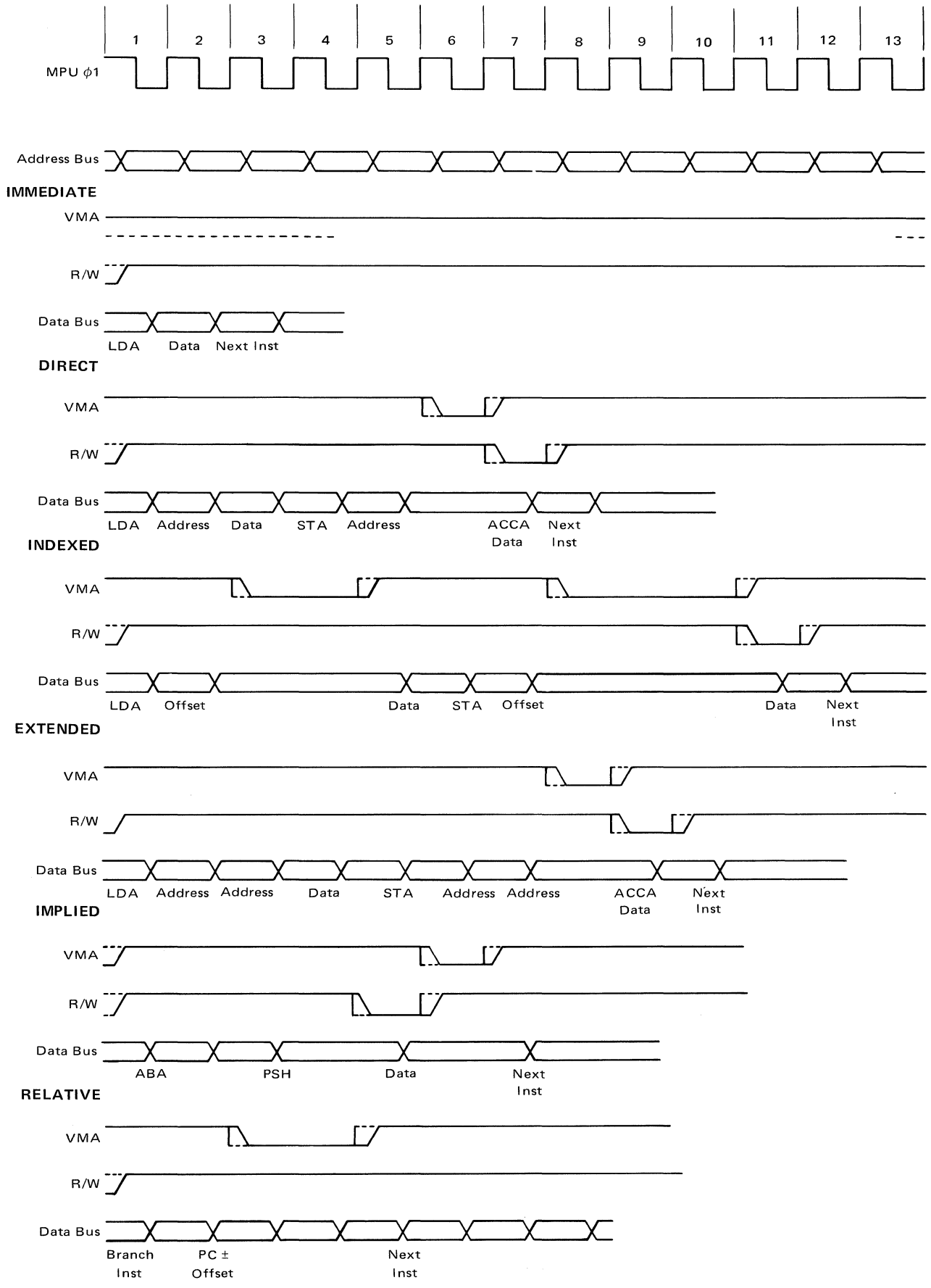
Implied Addressing

There are two types of implied addressing instructions: those which do not require an address and those which do require an address. These are one byte instructions. An example of an instruction which does not require an address is ABA. Here the contents of accumulator A is added to accumulator B and the result put in accumulator A. The Data Bus and Address Bus are valid only on the first cycle of the instruction as shown in Figure 11.

For those instructions which do require an address, the address is held by an internal MPU register such as the stack pointer. Thus no data is required to develop an address. An example of this type of instruction is PSH.

Looking again at Figure 11, the Data Bus and Address Bus are valid on cycle #3 to fetch the PSH operator. In cycle #4 the MPU is moving data internally and VMA does not go low. During this time the Address bus contains the address of the next instruction in ROM and the MPU is doing an invalid Read. In cycle #5 the stack pointer is loaded into Address Bus buffers and data is written into the stack. On the next cycle VMA goes low and the stack pointer is decremented. The next instruction then follows.

FIGURE 11 – ADDRESS MODES



Relative Addressing

In relative addressing, the address contained in the second byte of the instruction is added to the program counter's lowest 8 bits plus two. The carry or borrow is then added to the high 8 bits. This allows the user to address data within a range of −126 to +129 bytes of the present instruction. These are two byte instructions which perform branch functions.

Referring again to Figure 11, the operator code is fetched from the memory location stored in the instruction register during cycle #1. The Program Counter offset is loaded into the MPU during cycle #2. The offset is added to the low order bits of the Program Counter in cycle #3 and the carry is propagated during cycle #4. During these two cycles VMA goes low while the MPU is operating on the offset data. The next instruction is loaded during cycle #5.

Accumulator (ACCX) Addresssing

In accumulator only addressing, either accumulator A or accumulator B is specified.

An example is ASLA (Arithmetic Shift Left, on the A accumulator). These are one byte, two cycle instructions and the Address Bus and Data Bus are active only during the first cycle of the instruction when the operator is being loaded from memory. During the second cycle the machine performs the operation and VMA is high.

PROCESSOR CONTROLS

The microprocessor has six Processor Control Lines (Figure 1) which are:

$\overline{\text{Reset}}$	
$\overline{\text{NMI}}$	(Non-Maskable Interrupt)
$\overline{\text{Halt}}$	
BA	(Bus Available)
TSC	(Three-State Control)
DBE	(Data Bus Enable)

Two of the control lines, $\overline{\text{Reset}}$ and DBE are required for all systems. The remaining control lines can be utilized to enhance throughput and flexibility depending on the system application. The simplicity of the processor control lines results directly from the simplicity of the M6800 system architecture.

Along with the discussion on $\overline{\text{NMI}}$ will be a discussion of the Wait For Interrupt (WAI) instruction and the $\overline{\text{Interrupt Request}}$ ($\overline{\text{IRQ}}$) line since the three interrupt types are closely aligned.

$\overline{\text{Reset}}$

The $\overline{\text{Reset}}$ input is used to reset and start the MPU from a power down condition resulting from a power failure or initial start-up of the processor. This input can also be used to reinitialize the machine at any time after start up.

If a high level is detected in this input, this will signal the MPU to begin the reset sequence. During the reset sequence, the contents of the last two locations (FFFE, FFFF) in memory will be loaded into the Program Counter to point to the beginning of the reset routine. During the reset routine, the interrupt mask bit is set and must be cleared under program control before the MPU can be interrupted by $\overline{\text{IRQ}}$. While $\overline{\text{Reset}}$ is low (assuming a minimum of 8 clock cycles have occurred) the MPU output signals will be in the following states: VMA = low, BA = low, Data Bus = high impedance, R/W = high (read state), and the Address Bus will contain the reset address FFFE. Figure 12 illustrates a power up sequence using the $\overline{\text{Reset}}$ control line. After the power supply reaches 4.75 V a minimum of eight clock cycles are required for the processor to stabilize in preparation for restarting. During these eight cycles, VMA will be in an indeterminate state so any devices that are enabled by VMA which could accept a false write during this time (such as a battery-backed RAM) must be disabled until VMA is forced low after eight cycles. $\overline{\text{Reset}}$ can go high asynchronously with the system clock any time after the eighth cycle.

$\overline{\text{Reset}}$ timing is shown in Figure 12 and Table 4. The maximum rise and fall transition times are specified by t_{PCr} and t_{PCf}. If $\overline{\text{Reset}}$ is high at t_{PCS} (processor control setup time) as shown in Figure 12 in any given cycle, then the restart sequence will begin on the next cycle as shown. The $\overline{\text{Reset}}$ control line may also be used to reinitialize the MPU system at any time during its operation. This is accomplished by pulsing $\overline{\text{Reset}}$ low for the duration of a minimum of three complete $\phi 2$ cycles. The $\overline{\text{Reset}}$ pulse can be completely asynchronous with the MPU system clock and will be recognized during $\phi 2$ if setup time t_{PCS} is met.

$\overline{\text{Non-Maskable Interrupt}}$ ($\overline{\text{NMI}}$) and Wait for Interrupt (WAI)

The MC6800 is capable of handling two types of interrupts: maskable ($\overline{\text{IRQ}}$) as described earlier, and non-maskable ($\overline{\text{NMI}}$). $\overline{\text{IRQ}}$ is maskable by the interrupt mask in the condition code register while $\overline{\text{NMI}}$ is not maskable. The handling of these interrupts by the MPU is the same except that each has its own vector address. The behavior of the MPU when interrupted is shown in Figure 13, which details the MPU response to an interrupt while the MPU is executing the control program. The interrupt shown could be either $\overline{\text{IRQ}}$ or $\overline{\text{NMI}}$ and can be asynchronous with respect to $\phi 2$. The interrupt is shown going low at time t_{PCS} in cycle #1 which precedes the first cycle of an instruction (OP code fetch). This instruction is not executed but instead the Program Counter (PC), Index Register (IX), Accumulators (ACCX), and the Condition Code Register (CCR) are pushed onto the stack.

The Interrupt Mask bit is set to prevent further interrupts. The address of the interrupt service routine is then fetched from FFFC, FFFD for an NMI interrupt and from FFF8, FFF9 for an $\overline{\text{IRQ}}$ interrupt. Upon completion of the interrupt service routine, the execution of RTI will pull the PC, IX, ACCX, and CCR off of the stack; the Interrupt Mask bit is restored to its condition prior to Interrupts.

Figure 14 is a similar interrupt sequence, except in this case, a WAIT instruction has been executed in preparation for the interrupt. This technique speeds up the MPU's response to the interrupt because the stacking of the PC, IX, ACCX, and the CCR is already done. While the MPU is waiting for the interrupt, Bus Available will go high indicating the following states of the control lines: VMA is low, and the Address Bus, R/W and Data Bus are all in the high impedance state. After the interrupt occurs, it is serviced as previously described.

$\overline{\text{Halt}}$ and Single Instruction Execution

The $\overline{\text{Halt}}$ line provides an input to the MPU to allow control of program execution by an outside source. If $\overline{\text{Halt}}$ is high,the MPU will execute the instructions; if it is low, the MPU will go to a halted or idle mode. A response signal, Bus Available (BA) provides an indication of the current

FIGURE 12 – $\overline{\text{RESET}}$ TIMING

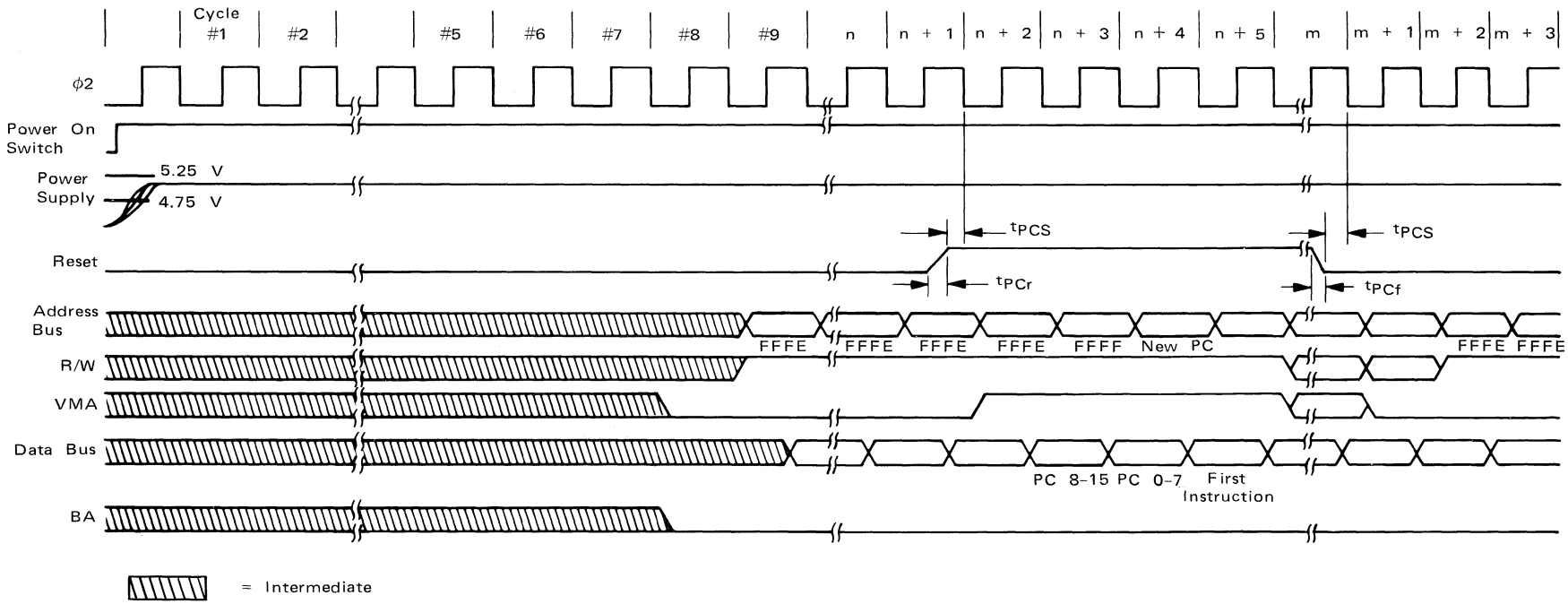


FIGURE 13 – INTERRUPT TIMING

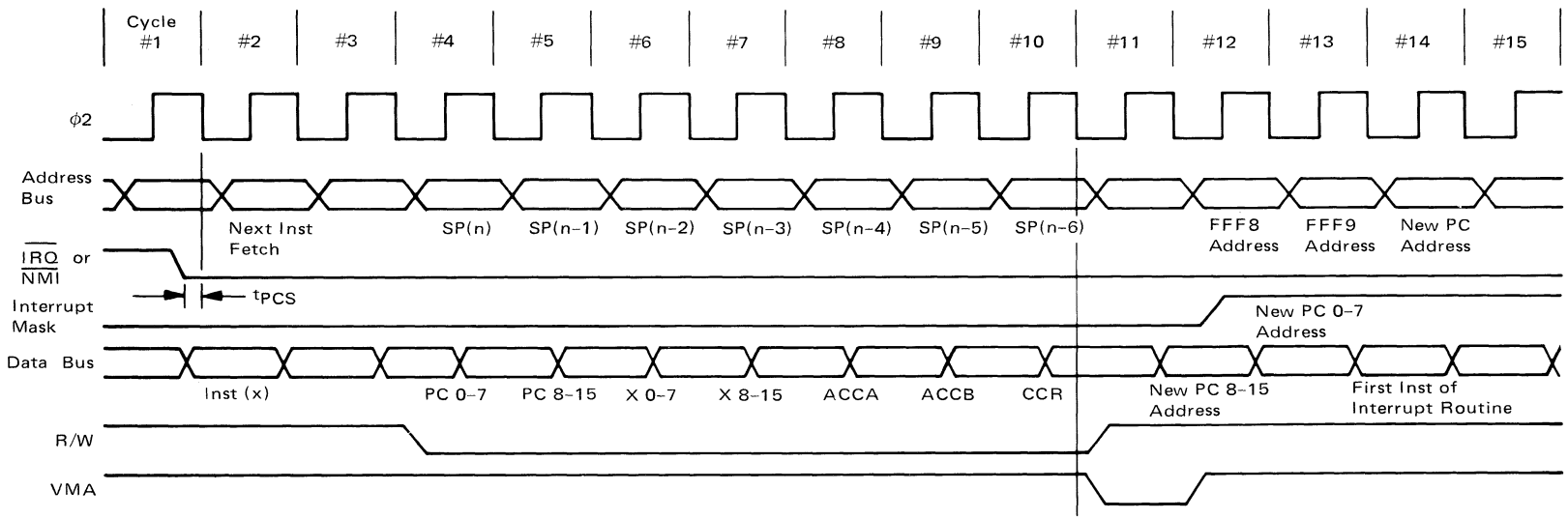
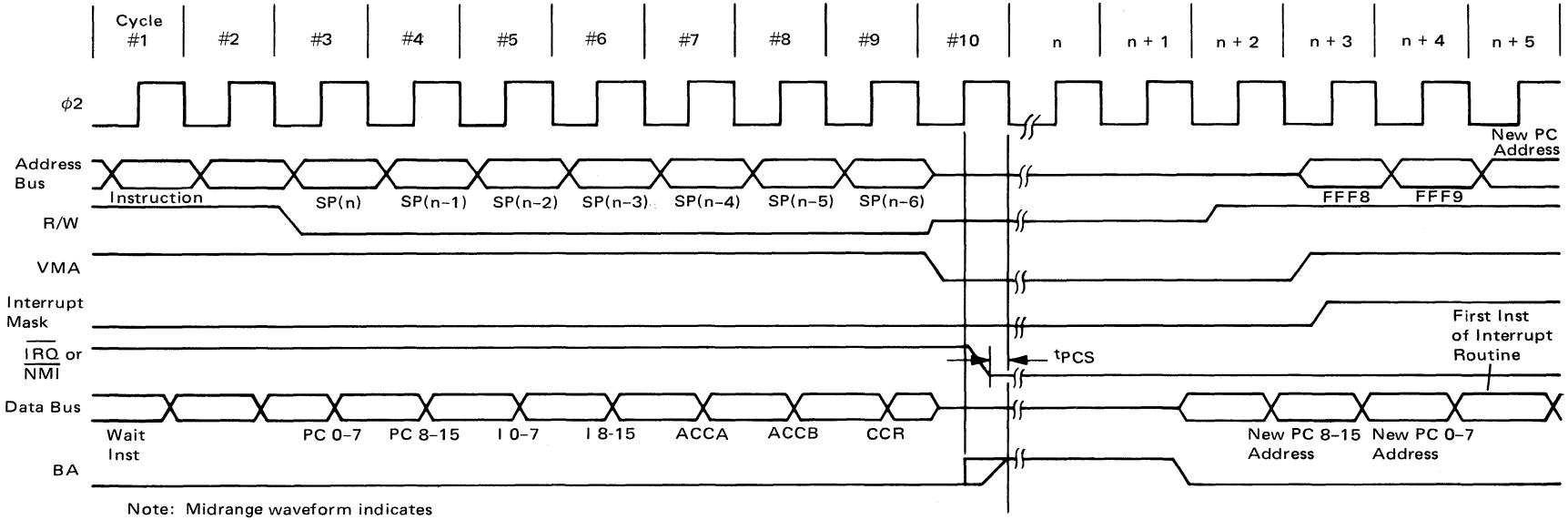


FIGURE 14 – WAIT INSTRUCTION TIMING



Note: Midrange waveform indicates high impedance state.

MPU status. When BA is low, the MPU is in the process of executing the control program; if BA is high, the MPU has halted and all internal activity has stopped.

When BA is high, the Address Bus, Data Bus, and R/W line will be in a high impedance state, effectively removing the MPU from the system bus. VMA is forced low so that the floating system bus will not activate any device on the bus that is enabled by VMA.

While the MPU is halted, all program activity is stopped, and if either an $\overline{NMI}$ or $\overline{IRQ}$ interrupt occurs, it will be latched into the MPU and acted on as soon as the MPU is taken out of the halted mode. If a $\overline{Reset}$ command occurs while the MPU is halted, the following states occur: VMA = low, BA = low, Data Bus = high impedance, R/W = high (read state), and the Address Bus will contain address FFFE as long as $\overline{Reset}$ is low. As soon as the $\overline{Halt}$ line goes high, the MPU will go to locations FFFE and FFFF for the address of the reset routine.

Figure 15 shows the timing relationships involved when halting the MPU. The instruction illustrated is a one byte, 2 cycle instruction such as CLRA. When $\overline{Halt}$ goes low, the MPU will halt after completing execution of the current instruction. The transition of $\overline{Halt}$ must occur t_{PCS} before the trailing edge of $\phi 1$ of the last cycle of an instruction (point A of Figure 15). $\overline{Halt}$ must not go low any time later than the minimum t_{PCS} specified.

The fetch of the OP code by the MPU is the first cycle of the instruction. If $\overline{Halt}$ had not been low at Point A but went low during $\phi 2$ of that cycle, the MPU would have halted after completion of the following instruction. BA will go high by time t_{BA} (bus available delay time) after the last instruction cycle. At this point in time, VMA is low and R/W, Address Bus, and the Data Bus are in the high impedance state.

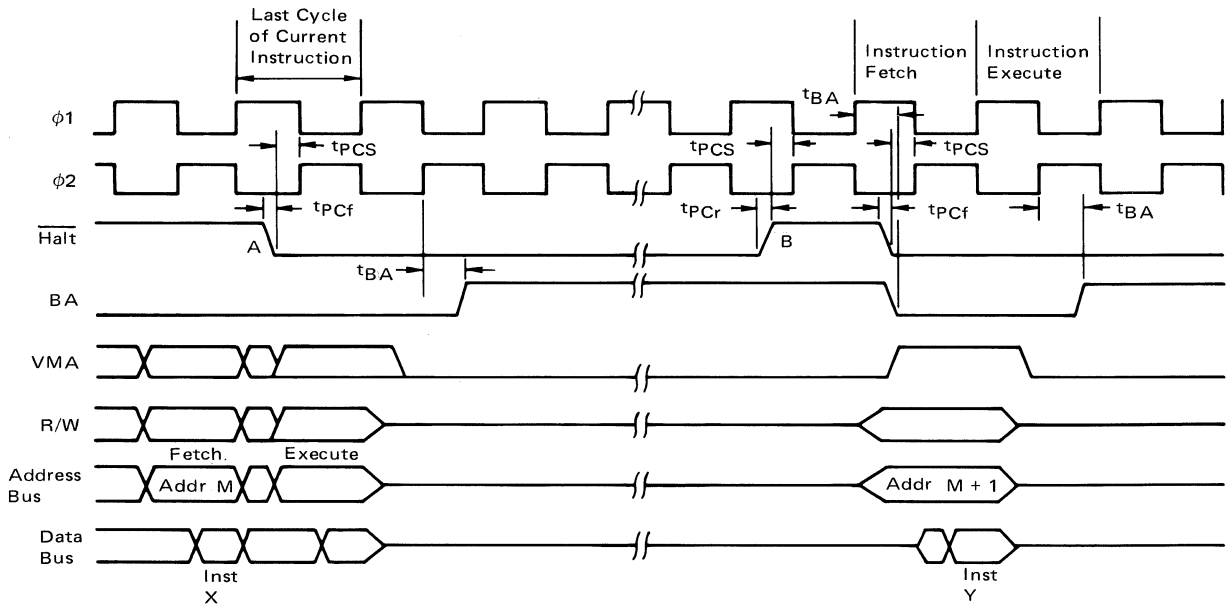
To debug programs it is advantageous to step through programs instruction by instruction. To do this, $\overline{Halt}$ must be brought high for one MPU cycle and then returned low as shown at point B of Figure 15. Again, the transitions of $\overline{Halt}$ must occur t_{PCS} before the trailing edge of $\phi 1$. BA will go low at t_{BA} after the leading edge of the next $\phi 1$, indicating that the Address Bus, Data Bus, VMA and R/W lines are back on the bus. A single byte, 2 cycle instruction such as LSR is used for this example also. During the first cycle, the instruction Y is fetched from address M + 1. BA returns high at t_{BA} on the last cycle of the instruction indicating the MPU is off the bus. If instruction Y had been three cycles, the width of the BA low time would have been increased by one cycle.

Three State Control (TSC)

When the Three-State Control (TSC) line is a logic "1", the Address Bus and the R/W line are placed in a high impedance state. VMA and BA are forced low whenever TSC = "1" to prevent false reads or writes on any device enabled by VMA. While TSC is held high, the $\phi 1$ and $\phi 2$ clocks must be held high and low, respectively, in order to delay program execution (this is required because of the bus lines being in an indeterminate state). Since the MPU is a dynamic device, the $\phi 1$ clock can be stopped for a maximum time $PW_{\phi H}$ without destroying data within the MPU. TSC then can be used in a short Direct Memory Access (DMA) application.

Figure 16 shows the effect of TSC on the MPU. TSC must have its transitions at t_{TSE} (three-state enable) while holding $\phi 1$ high and $\phi 2$ low as shown. The Address Bus and R/W line will reach the high impedance state at t_{TSD} (three-state delay), with VMA being forced low. In this example, the Data Bus is also in the high impedance state while $\phi 2$ is being held low since DBE = $\phi 2$. At this point in

FIGURE 15 – $\overline{HALT}$ AND SINGLE INSTRUCTION EXECUTION FOR SYSTEM DEBUG



Note: Midrange waveform indicates high impedance state.

time, a DMA transfer could occur on cycles #3 and #4. When TSC is returned low, the MPU Address and R/W lines return to the bus. Because it is too late in cycle #5 to access memory, this cycle is dead and used for synchronization. Program execution resumes in cycle #6.

Bus Available (BA)

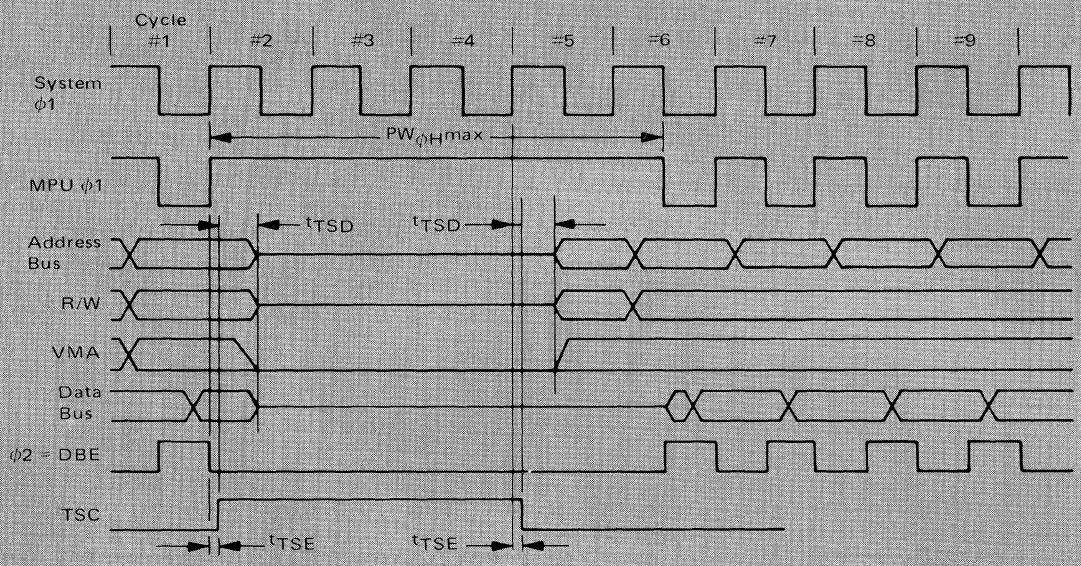
The Bus Available signal will normally be in the low state; when activated, it will go to the high state indicating that the microprocessor has stopped and that the address bus is available. This will occur if the $\overline{\text{Halt}}$ line is in the low state (Figure 15), or if the processor is in the WAIT state (Figure 14) as a result of the execution of a WAIT instruction. At such time, all three-state output drivers will go to their off state and other outputs to their normally inactive level. The processor is removed from the WAIT state by the occurrence of a maskable (mask bit I = 0) or non-maskable interrupt. Note that if TSC is in the high state, Bus Available will be low.

Data Bus Enable (DBE)

DBE is the three-state control signal for the MPU data bus and will enable the bus drivers when in the high state. This input is TTL compatible; however in normal operation, it would be driven by the $\phi 2$ clock. During an MPU read cycle, the data bus drivers will be disabled internally. When it is desired that another device control the data bus such as in DMA applications, DBE should be held low

If additional data setup or hold time is required on an MPU write, the DBE down time can be decreased as shown in Figure 6 (DBE $\neq \phi 2$). The minimum down time for DBE is $t_{\overline{DBE}}$ as shown in Table 4, and must occur within $\phi 1$ up time. The minimum delay from the trailing edge of DBE to the trailing edge of $\phi 1$ is t_{DBED}. By skewing DBE with respect to E in this manner, data setup or hold time can be increased.

FIGURE 16 – THREE STATE CONTROL TIMING



MOTOROLA Semiconductors
BOX 20912 • PHOENIX, ARIZONA 85036

MC6800

(0 to 70°C; L or P Suffix)

MC6800C

(-40 to 85°C; L Suffix only)

MICROPROCESSING UNIT (MPU)

The MC6800 is a monolithic 8-bit microprocessor forming the central control function for Motorola's M6800 family. Compatible with TTL, the MC6800, as with all M6800 system parts, requires only one +5.0-volt power supply, and no external TTL devices for bus interface.

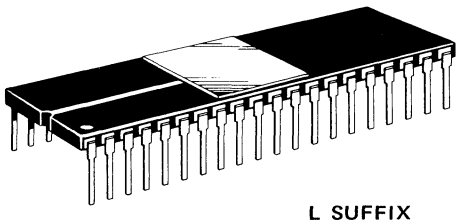
The MC6800 is capable of addressing 65K bytes of memory with its 16-bit address lines. The 8-bit data bus is bidirectional as well as 3-state, making direct memory addressing and multiprocessing applications realizable.

- Eight-Bit Parallel Processing
- Bi-Directional Data Bus
- Sixteen-Bit Address Bus — 65K Bytes of Addressing
- 72 Instructions — Variable Length
- Seven Addressing Modes — Direct, Relative, Immediate, Indexed, Extended, Implied and Accumulator
- Variable Length Stack
- Vectored Restart
- Maskable Interrupt Vector
- Separate Non-Maskable Interrupt — Internal Registers Saved In Stack
- Six Internal Registers — Two Accumulators, Index Register, Program Counter, Stack Pointer and Condition Code Register
- Direct Memory Addressing (DMA) and Multiple Processor Capability
- Clock Rates as High as 1 MHz
- Simple Bus Interface Without TTL
- Halt and Single Instruction Execution Capability

MOS

(N-CHANNEL, SILICON-GATE)

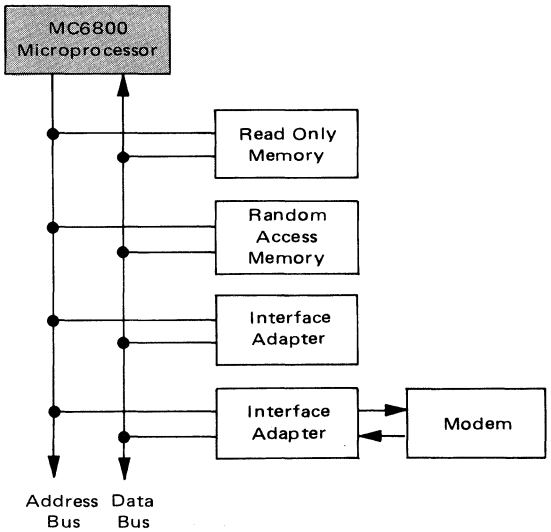
MICROPROCESSOR



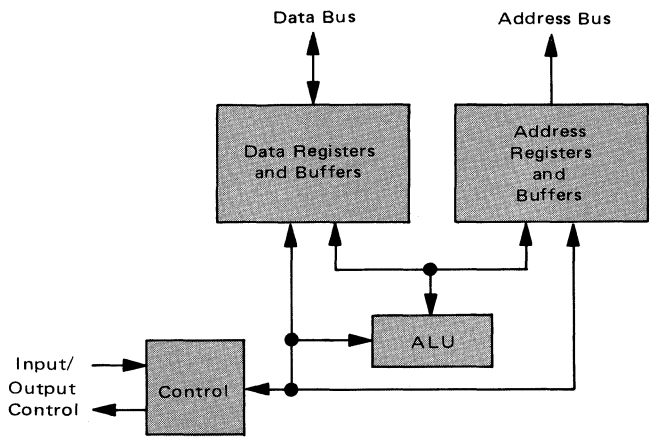
L SUFFIX
CERAMIC PACKAGE
CASE 715

NOT SHOWN: **P SUFFIX**
PLASTIC PACKAGE
CASE 711

M6800 MICROCOMPUTER FAMILY BLOCK DIAGRAM



MC6800 MICROPROCESSOR BLOCK DIAGRAM

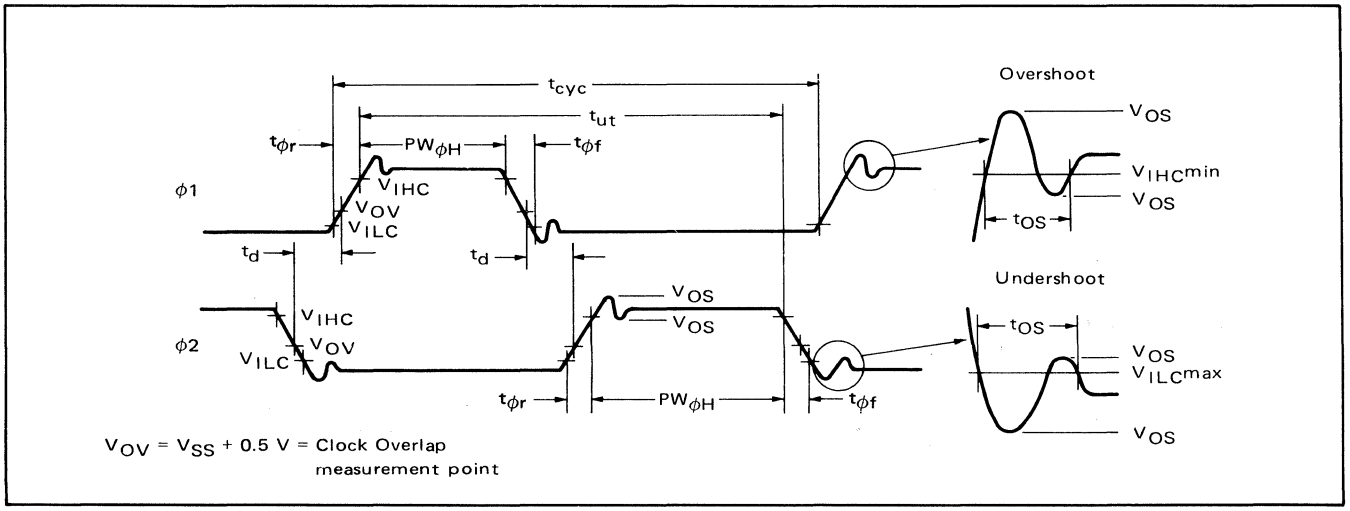


ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V ± 5%, V_{SS} = 0, T_A = 0 to 70°C unless otherwise noted.)

Characteristic		Symbol	Min	Typ	Max	Unit
Input High Voltage	Logic	V_{IH}	V_{SS} + 2.0	–	V_{CC}	Vdc
	$\phi1,\phi2$	V_{IHC}	V_{CC} – 0.3	–	V_{CC} + 0.1	
Input Low Voltage	Logic	V_{IL}	V_{SS} – 0.3	–	V_{SS} + 0.8	Vdc
	$\phi1,\phi2$	V_{ILC}	V_{SS} – 0.1	–	V_{SS} + 0.3	
Clock Overshoot/Undershoot – Input High Level		V_{OS}	V_{CC} – 0.5	–	V_{CC} + 0.5	Vdc
– Input Low Level			V_{SS} – 0.5	–	V_{SS} + 0.5	
Input Leakage Current		I_{in}				μAdc
(V_{in} = 0 to 5.25 V, V_{CC} = max)	Logic*		–	1.0	2.5	
(V_{in} = 0 to 5.25 V, V_{CC} = 0.0 V)	$\phi1,\phi2$		–	–	100	
Three-State (Off State) Input Current	D0-D7	I_{TSI}	–	2.0	10	μAdc
(V_{in} 0.4 to 2.4 V, V_{CC} = max)	A0-A15,R/W		–	–	100	
Output High Voltage		V_{OH}				Vdc
(I_{Load} = –205 μAdc, V_{CC} = min)	D0-D7		V_{SS} + 2.4	–	–	
(I_{Load} = –145 μAdc, V_{CC} = min)	A0-A15,R/W,VMA		V_{SS} + 2.4	–	–	
(I_{Load} = –100 μAdc, V_{CC} = min)	BA		V_{SS} + 2.4	–	–	
Output Low Voltage (I_{Load} = 1.6 mAdc, V_{CC} = min)		V_{OL}	–	–	V_{SS} + 0.4	Vdc
Power Dissipation		P_D	–	0.600	1.2	W
Capacitance #	$\phi1,\phi2$	C_{in}	80	120	160	pF
(V_{in} = 0, T_A = 25°C, f = 1.0 MHz)	TSC		–	–	15	
	DBE		–	7.0	10	
	D0-D7		–	10	12.5	
	Logic Inputs		–	6.5	8.5	
	A0-A15,R/W,VMA	C_{out}	–	–	12	pF
Frequency of Operation		f	0.1	–	1.0	MHz
Clock Timing (Figure 1)						
Cycle Time		t_{cyc}	1.0	–	10	μs
Clock Pulse Width		$PW_{\phi H}$				ns
(Measured at V_{CC} – 0.3 V)	$\phi1$		430	–	4500	
	$\phi2$		450	–	4500	
Total $\phi1$ and $\phi2$ Up Time		t_{ut}	940	–	–	ns
Rise and Fall Times	$\phi1,\phi2$	$t_{\phi r}$, $t_{\phi f}$	5.0	–	50	ns
(Measured between V_{SS} + 0.3 V and V_{CC} – 0.3 V)						
Delay Time or Clock Separation		t_d	0	–	9100	ns
(Measured at V_{OV} = V_{SS} + 0.5 V)						
Overshoot Duration		t_{OS}	0	–	40	ns

*Except $\overline{IRQ}$ and $\overline{NMI}$, which require 3 kΩ pullup load resistors for wire-OR capability at optimum operation.
#Capacitances are periodically sampled rather than 100% tested.

FIGURE 1 – CLOCK TIMING WAVEFORM



MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.3 to +7.0	Vdc
Input Voltage	V_{in}	−0.3 to +7.0	Vdc
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	−55 to +150	°C
Thermal Resistance	θ_{JA}	70	°C/W

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

READ/WRITE TIMING Figures 2 and 3, f = 1.0 MHz, Load Circuit of Figure 6.

Characteristic	Symbol	Min	Typ	Max	Unit
Address Delay	t_{AD}	–	220	300	ns
Peripheral Read Access Time $t_{acc} = t_{ut} - (t_{AD} + t_{DSR})$	t_{acc}	–	–	540	ns
Data Setup Time (Read)	t_{DSR}	100	–	–	ns
Input Data Hold Time	t_H	10	–	–	ns
Output Data Hold Time	t_H	10	25	–	ns
Address Hold Time (Address, R/W, VMA)	t_{AH}	50	75	–	ns
Enable High Time for DBE Input	t_{EH}	450	–	–	ns
Data Delay Time (Write)	t_{DDW}	–	165	225	ns
Processor Controls*					
Processor Control Setup Time	t_{PCS}	200	–	–	ns
Processor Control Rise and Fall Time	t_{PCr}, t_{PCf}	–	–	100	ns
Bus Available Delay	t_{BA}	–	–	300	ns
Three State Enable	t_{TSE}	–	–	40	ns
Three State Delay	t_{TSD}	–	–	700	ns
Data Bus Enable Down Time During $\phi 1$ Up Time (Figure 3)	$t_{\overline{DBE}}$	150	–	–	ns
Data Bus Enable Delay (Figure 3)	t_{DBED}	300	–	–	ns
Data Bus Enable Rise and Fall Times (Figure 3)	t_{DBEr}, t_{DBEf}	–	–	25	ns

*Additional information is given in Figures 12 through 16 of the Family Characteristics – see pages 17 through 20.

FIGURE 2 – READ DATA FROM MEMORY OR PERIPHERALS

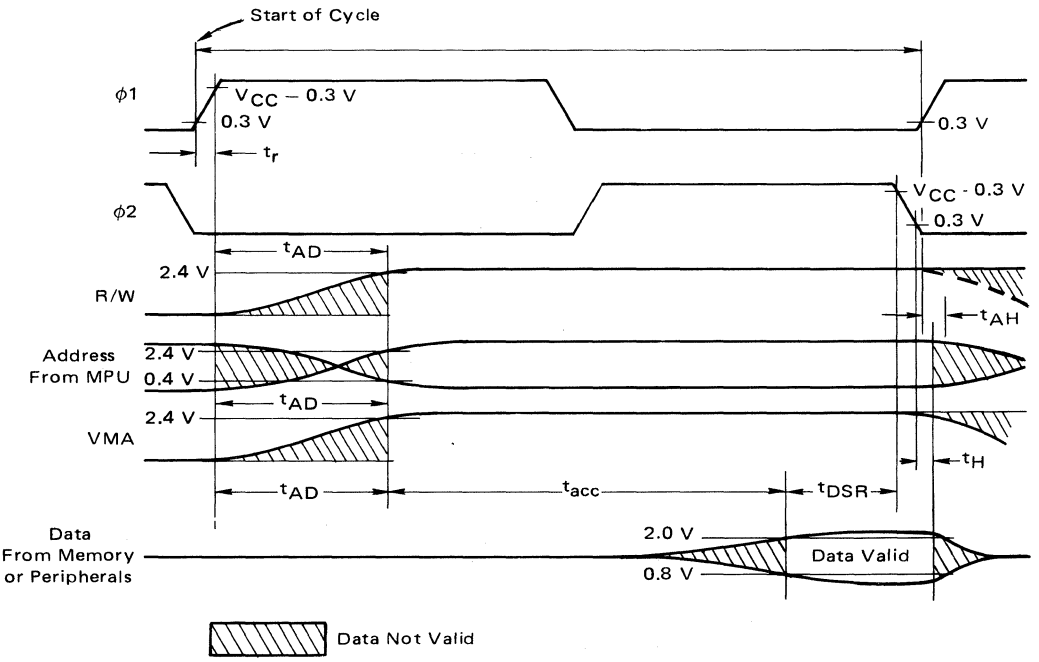


FIGURE 3 – WRITE IN MEMORY OR PERIPHERALS

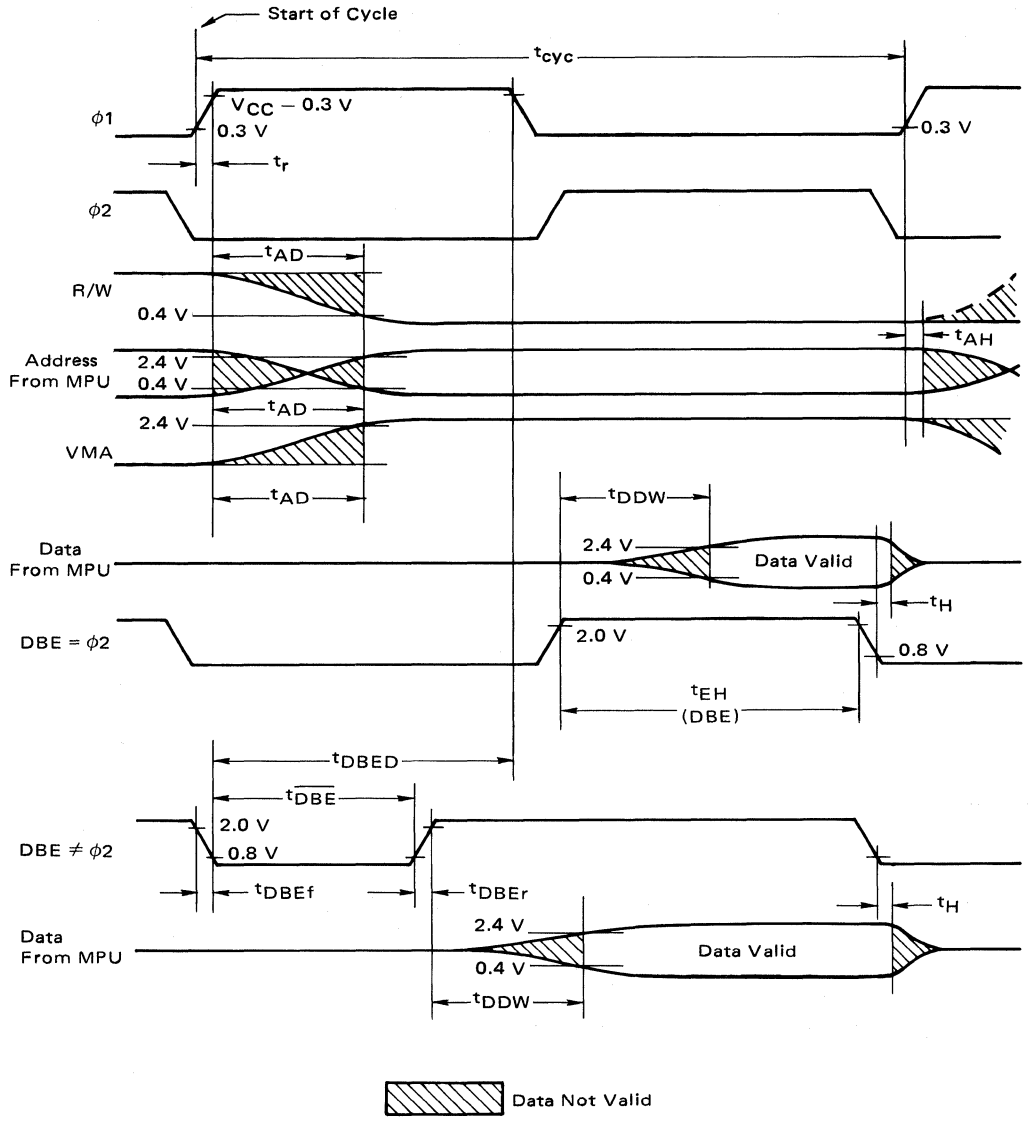


FIGURE 4 – TYPICAL DATA BUS OUTPUT DELAY versus CAPACITIVE LOADING

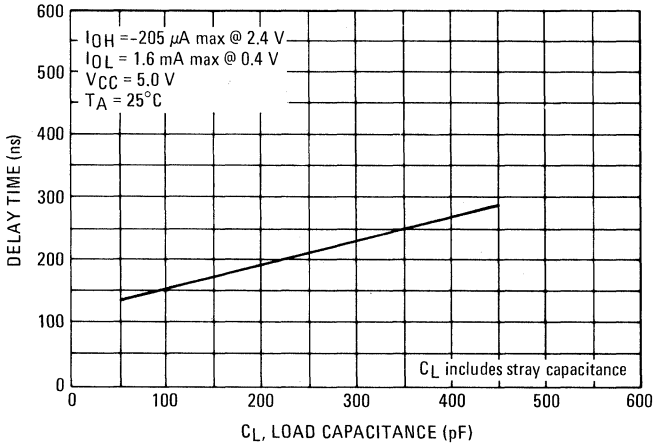


FIGURE 5 – TYPICAL READ/WRITE, VMA, AND ADDRESS OUTPUT DELAY versus CAPACITIVE LOADING

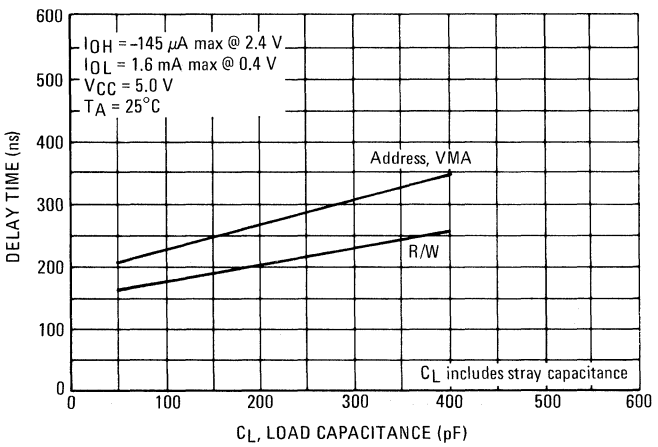
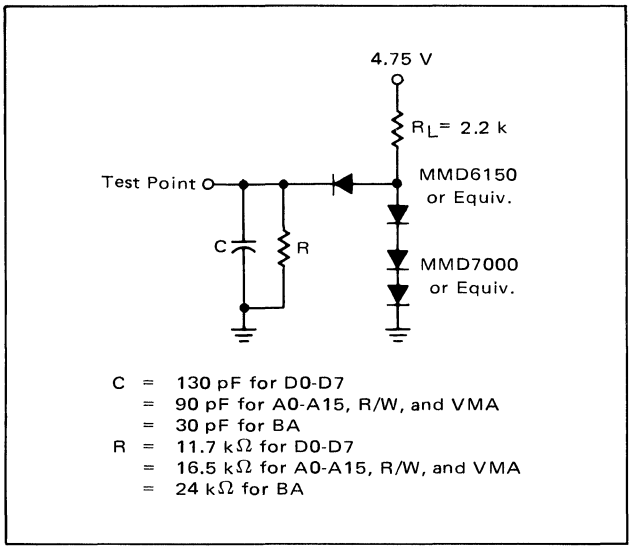


FIGURE 6 – BUS TIMING TEST LOAD



C = 130 pF for D0-D7
= 90 pF for A0-A15, R/W, and VMA
= 30 pF for BA
R = 11.7 kΩ for D0-D7
= 16.5 kΩ for A0-A15, R/W, and VMA
= 24 kΩ for BA

TYPICAL POWER SUPPLY CURRENT

FIGURE 7 – VARIATIONS WITH FREQUENCY

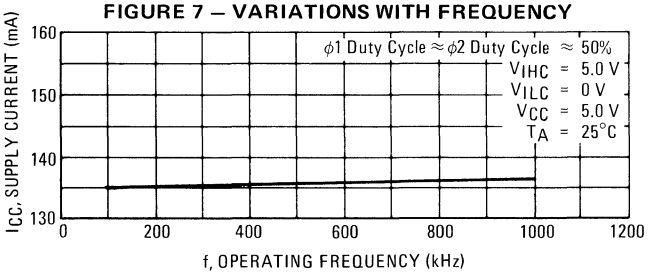
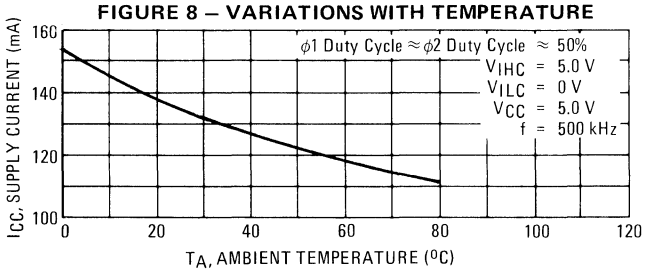
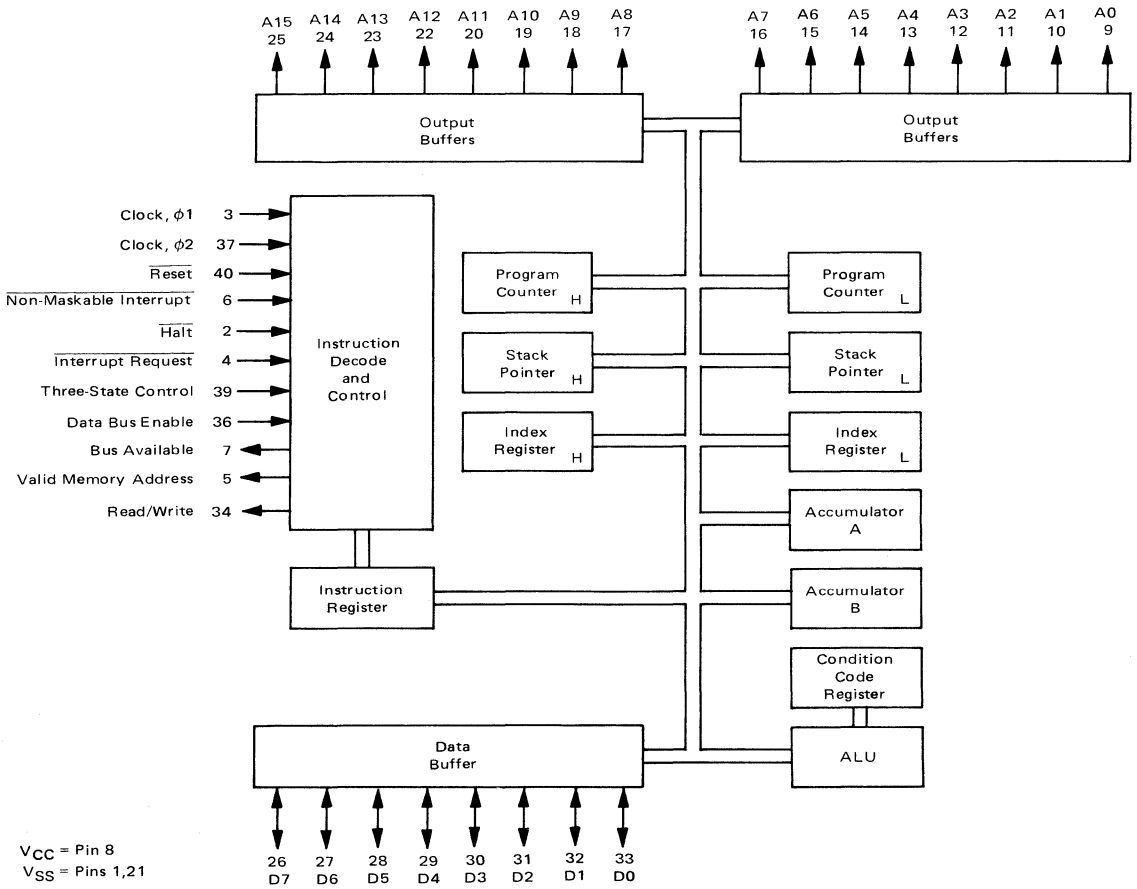


FIGURE 8 – VARIATIONS WITH TEMPERATURE



EXPANDED BLOCK DIAGRAM



MPU SIGNAL DESCRIPTION

Proper operation of the MPU requires that certain control and timing signals be provided to accomplish specific functions and that other signal lines be monitored to determine the state of the processor.

Clocks Phase One and Phase Two ($\phi 1, \phi 2$) — Two pins are used for a two-phase non-overlapping clock that runs at the V_{CC} voltage level.

Address Bus (A0-A15) — Sixteen pins are used for the address bus. The outputs are three-state bus drivers capable of driving one standard TTL load and 130 pF. When the output is turned off, it is essentially an open circuit. This permits the MPU to be used in DMA applications.

Data Bus (D0-D7) — Eight pins are used for the data bus. It is bi-directional, transferring data to and from the memory and peripheral devices. It also has three-state output buffers capable of driving one standard TTL load and 130 pF.

$\overline{\text{Halt}}$ — When this input is in the low state, all activity in the machine will be halted. This input is level sensitive. In the halt mode, the machine will stop at the end of an instruction, Bus Available will be at a one level, Valid Memory Address will be at a zero, and all other three-state lines will be in the three-state mode.

Transition of the $\overline{\text{Halt}}$ line must not occur during the last 250 ns of phase one. To insure single instruction operation, the $\overline{\text{Halt}}$ line must go high for one Clock cycle.

Three-State Control (TSC) — This input causes all of the address lines and the Read/Write line to go into the off or high impedance state. This state will occur 700 ns after TSC = 2.0 V. The Valid Memory Address and Bus Available signals will be forced low. The data bus is not affected by TSC and has its own enable (Data Bus Enable). In DMA applications, the Three-State Control line should be brought high on the leading edge of the Phase One Clock. The $\phi 1$ clock must be held in the high state and the $\phi 2$ in the low state for this function to operate properly. The address bus will then be available for other devices to directly address memory. Since the MPU is a dynamic device, it can be held in this state for only 4.5 μs or destruction of data will occur in the MPU.

Read/Write (R/W) — This TTL compatible output signals the peripherals and memory devices whether the MPU is in a Read (high) or Write (low) state. The normal standby state of this signal is Read (high). Three-State Control going high will turn Read/Write to the off (high impedance) state. Also, when the processor is halted, it will be in the off state. This output is capable of driving one standard TTL load and 90 pF.

Valid Memory Address (VMA) — This output indicates to peripheral devices that there is a valid address on the address bus. In normal operation, this signal should be utilized for enabling peripheral interfaces such as the PIA and ACIA. This signal is not three-state. One standard TTL load and 90 pF may be directly driven by this active high signal.

Data Bus Enable (DBE) — This input is the three-state control signal for the MPU data bus and will enable the bus drivers when in the high state. This input is TTL compatible; however in normal operation, it would be driven by the phase two clock. During an MPU read cycle, the data bus drivers will be disabled internally. When it is desired that another device control the data bus such as in Direct Memory Access (DMA) applications, DBE should be held low.

Bus Available (BA) — The Bus Available signal will normally be in the low state; when activated, it will go to the high state indicating that the microprocessor has stopped and that the address bus is available. This will occur if the $\overline{\text{Halt}}$ line is in the low state or the processor is in the WAIT state as a result of the execution of a WAIT instruction. At such time, all three-state output drivers will go to their off state and other outputs to their normally inactive level. The processor is removed from the WAIT state by the occurrence of a maskable (mask bit I = 0) or nonmaskable interrupt. This output is capable of driving one standard TTL load and 30 pF.

Interrupt Request ($\overline{\text{IRQ}}$) — This level sensitive input requests that an interrupt sequence be generated within the machine. The processor will wait until it completes the current instruction that is being executed before it recognizes the request. At that time, if the interrupt mask bit in the Condition Code Register is not set, the machine will begin an interrupt sequence. The Index Register, Program Counter, Accumulators, and Condition Code Register are stored away on the stack. Next the MPU will respond to the interrupt request by setting the interrupt mask bit high so that no further interrupts may occur. At the end of the cycle, a 16-bit address will be loaded that points to a vectoring address which is located in memory locations FFF8 and FFF9. An address loaded at these locations causes the MPU to branch to an interrupt routine in memory.

The $\overline{\text{Halt}}$ line must be in the high state for interrupts to be serviced. Interrupts will be latched internally while $\overline{\text{Halt}}$ is low.

The $\overline{\text{IRQ}}$ has a high impedance pullup device internal to the chip; however a 3 kΩ external resistor to V_{CC} should be used for wire-OR and optimum control of interrupts.

$\overline{\text{Reset}}$ — This input is used to reset and start the MPU from a power down condition, resulting from a power failure or an initial start-up of the processor. If a high level is detected on the input, this will signal the MPU to begin the restart sequence. This will start execution of a routine to initialize the processor from its reset condition. All the higher order address lines will be forced high. For the restart, the last two (FFFE, FFFF) locations in memory will be used to load the program that is addressed by the program counter. During the restart routine, the interrupt mask bit is set and must be reset before the MPU can be interrupted by $\overline{\text{IRQ}}$.

Figure 9 shows the initialization of the microprocessor after restart. $\overline{\text{Reset}}$ must be held low for at least eight clock periods after V_{CC} reaches 4.75 volts. If $\overline{\text{Reset}}$ goes high prior to the leading edge of $\phi 2$, on the next $\phi 1$ the first restart memory vector address (FFFE) will appear on the address lines. This location should contain the higher order eight bits to be stored into the program counter. Following, the next address FFFF should contain the lower order eight bits to be stored into the program counter.

Non-Maskable Interrupt ($\overline{\text{NMI}}$) – A low-going edge on this input requests that a non-mask-interrupt sequence be generated within the processor. As with the $\overline{\text{Interrupt Request}}$ signal, the processor will complete the current instruction that is being executed before it recognizes the $\overline{\text{NMI}}$ signal. The interrupt mask bit in the Condition Code Register has no effect on $\overline{\text{NMI}}$.

The Index Register, Program Counter, Accumulators, and Condition Code Register are stored away on the stack. At the end of the cycle, a 16-bit address will be loaded that points to a vectoring address which is located in memory locations FFFC and FFFD. An address loaded at these locations causes the MPU to branch to a non-maskable interrupt routine in memory.

$\overline{\text{NMI}}$ has a high impedance pullup resistor internal to the chip; however a 3 kΩ external resistor to V_{CC} should be used for wire-OR and optimum control of interrupts.

Inputs $\overline{\text{IRQ}}$ and $\overline{\text{NMI}}$ are hardware interrupt lines that are sampled during $\phi 2$ and will start the interrupt routine on the $\phi 1$ following the completion of an instruction.

Figure 10 is a flow chart describing the major decision paths and interrupt vectors of the microprocessor. Table 1 gives the memory map for interrupt vectors.

FIGURE 9 – INITIALIZATION OF MPU AFTER RESTART

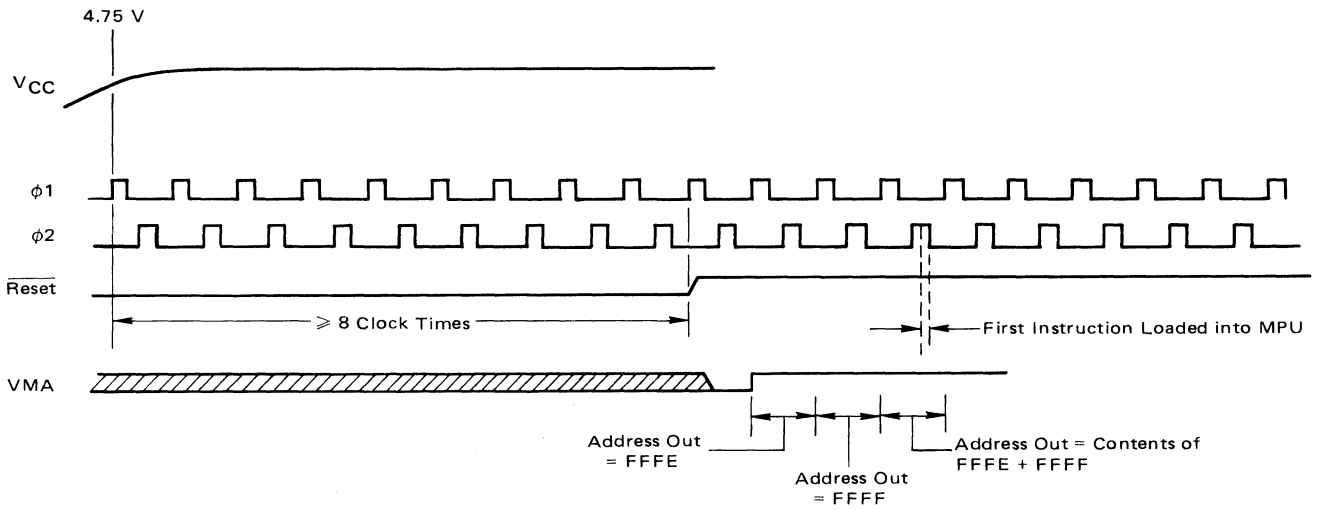
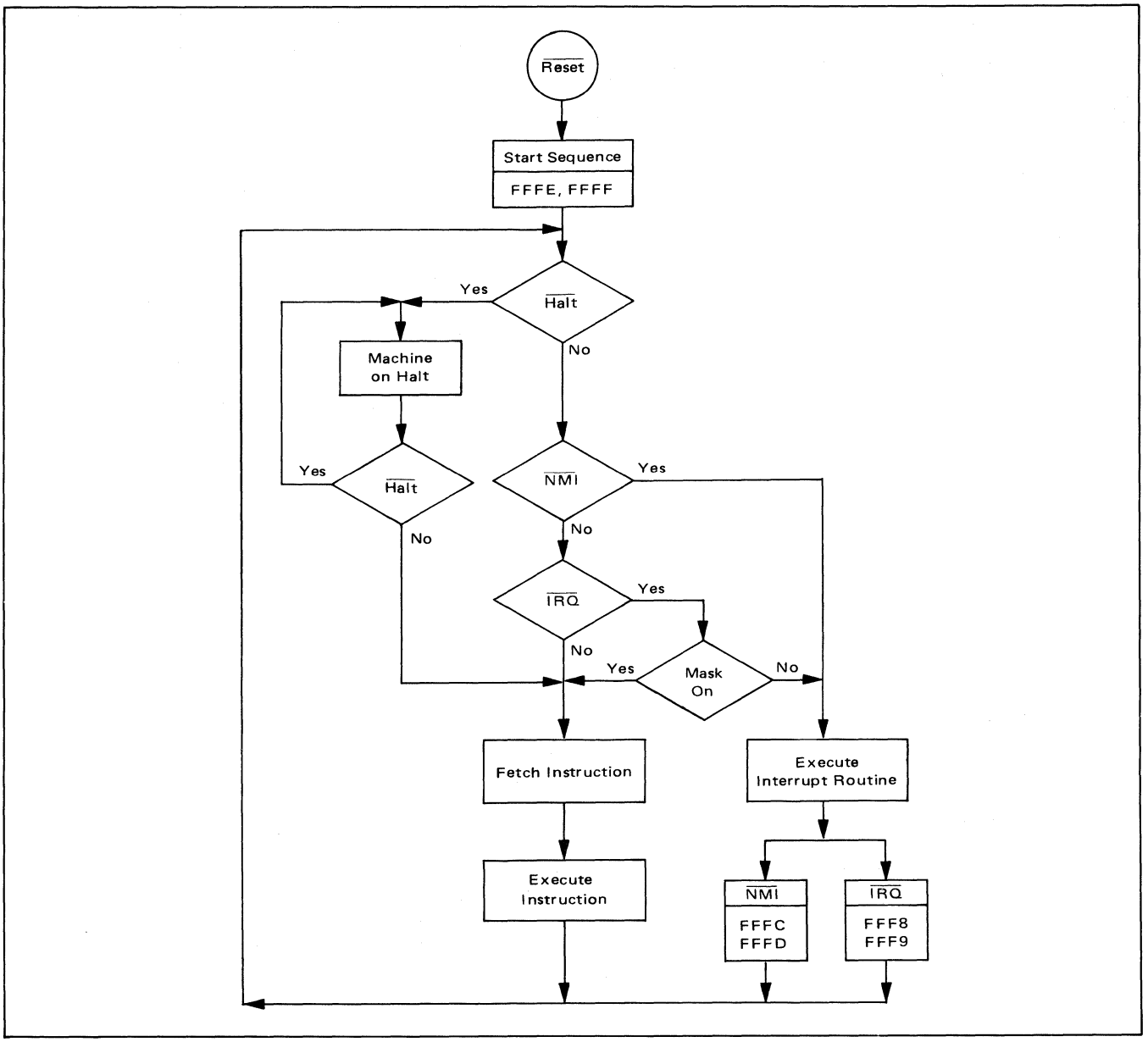


TABLE 1 – MEMORY MAP FOR INTERRUPT VECTORS

Vector MS	Vector LS	Description
FFFE	FFFF	Restart
FFFC	FFFD	Non-maskable Interrupt
FFFA	FFFB	Software Interrupt
FFF8	FFF9	Interrupt Request

FIGURE 10 – MPU FLOW CHART



MPU REGISTERS

The MPU has three 16-bit registers and three 8-bit registers available for use by the programmer (Figure 11).

Program Counter – The program counter is a two byte (16-bits) register that points to the current program address.

Stack Pointer – The stack pointer is a two byte register that contains the address of the next available location in an external push-down/pop-up stack. This stack is normally a random access Read/Write memory that may have any location (address) that is convenient. In those applications that require storage of information in the stack when power is lost, the stack must be non-volatile.

Index Register – The index register is a two byte register that is used to store data or a sixteen bit memory address for the Indexed mode of memory addressing.

Accumulators – The MPU contains two 8-bit accumulators that are used to hold operands and results from an arithmetic logic unit (ALU).

FIGURE 11 – PROGRAMMING MODEL OF THE MICROPROCESSING UNIT

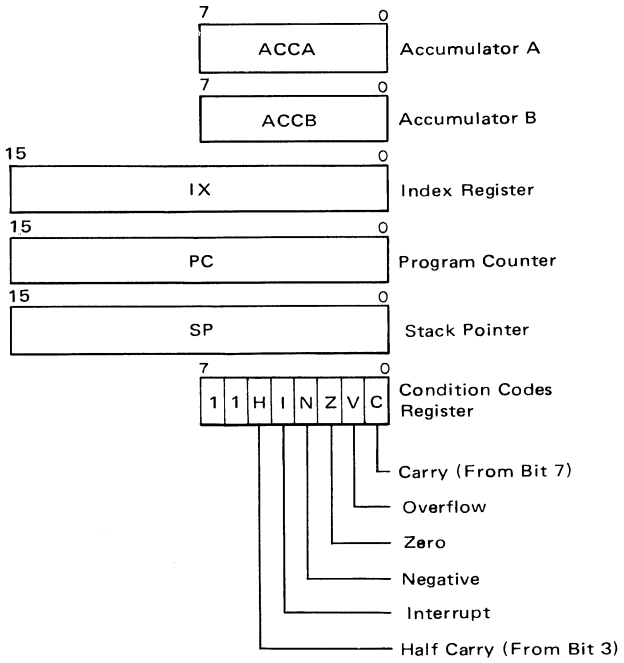
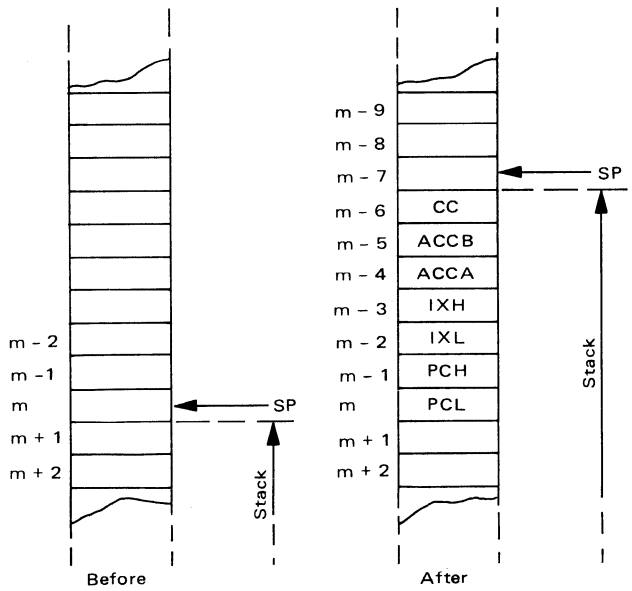


FIGURE 12 – SAVING THE STATUS OF THE MICROPROCESSOR IN THE STACK

SP = Stack Pointer
CC = Condition Codes (Also called the Processor Status Byte)
ACCB = Accumulator B
ACCA = Accumulator A
IXH = Index Register, Higher Order 8 Bits
IXL = Index Register, Lower Order 8 Bits
PCH = Program Counter, Higher Order 8 Bits
PCL = Program Counter, Lower Order 8 Bits



Condition Code Register — The condition code register indicates the results of an Arithmetic Logic Unit operation: Negative (N), Zero (Z), Overflow (V), Carry from bit 7 (C), and half carry from bit 3 (H). These bits of the Condition Code Register are used as testable conditions for the conditional branch instructions. Bit 4 is the interrupt mask bit (I). The unused bits of the Condition Code Register (b6 and b7) are ones.

Figure 12 shows the order of saving the microprocessor status within the stack.

MPU INSTRUCTION SET

The MC6800 has a set of 72 different instructions. Included are binary and decimal arithmetic, logical, shift, rotate, load, store, conditional or unconditional branch, interrupt and stack manipulation instructions (Tables 2 thru 6).

MPU ADDRESSING MODES

The MC6800 eight-bit microprocessing unit has seven address modes that can be used by a programmer, with the addressing mode a function of both the type of instruction and the coding within the instruction. A summary of the addressing modes for a particular instruction can be found in Table 7 along with the associated instruction execution time that is given in machine cycles. With a clock frequency of 1 MHz, these times would be microseconds.

Accumulator (ACCX) Addressing — In accumulator only addressing, either accumulator A or accumulator B is specified. These are one-byte instructions.

Immediate Addressing — In immediate addressing, the operand is contained in the second byte of the instruction except LDS and LDX which have the operand in the second and third bytes of the instruction. The MPU addresses this location when it fetches the immediate instruction for execution. These are two or three-byte instructions.

Direct Addressing — In direct addressing, the address of the operand is contained in the second byte of the instruction. Direct addressing allows the user to directly address the lowest 256 bytes in the machine i.e., locations zero through 255. Enhanced execution times are achieved by storing data in these locations. In most configurations, it should be a random access memory. These are two-byte instructions.

Extended Addressing — In extended addressing, the address contained in the second byte of the instruction is used as the higher eight-bits of the address of the operand. The third byte of the instruction is used as the lower eight-bits of the address for the operand. This is an absolute address in memory. These are three-byte instructions.

Indexed Addressing — In indexed addressing, the address contained in the second byte of the instruction is added to the index register's lowest eight bits in the MPU. The carry is then added to the higher order eight bits of the index register. This result is then used to address memory. The modified address is held in a temporary address register so there is no change to the index register. These are two-byte instructions.

Implied Addressing — In the implied addressing mode the instruction gives the address (i.e., stack pointer, index register, etc.). These are one-byte instructions.

Relative Addressing — In relative addressing, the address contained in the second byte of the instruction is added to the program counter's lowest eight bits plus two. The carry or borrow is then added to the high eight bits. This allows the user to address data within a range of -125 to +129 bytes of the present instruction. These are two-byte instructions.

TABLE 2 — MICROPROCESSOR INSTRUCTION SET — ALPHABETIC SEQUENCE

ABA	Add Accumulators
ADC	Add with Carry
ADD	Add
AND	Logical And
ASL	Arithmetic Shift Left
ASR	Arithmetic Shift Right
BCC	Branch if Carry Clear
BCS	Branch if Carry Set
BEQ	Branch if Equal to Zero
BGE	Branch if Greater or Equal Zero
BGT	Branch if Greater than Zero
BHI	Branch if Higher
BIT	Bit Test
BLE	Branch if Less or Equal
BLS	Branch if Lower or Same
BLT	Branch if Less than Zero
BMI	Branch if Minus
BNE	Branch if Not Equal to Zero
BPL	Branch if Plus
BRA	Branch Always
BSR	Branch to Subroutine
BVC	Branch if Overflow Clear
BVS	Branch if Overflow Set
CBA	Compare Accumulators
CLC	Clear Carry
CLI	Clear Interrupt Mask
CLR	Clear
CLV	Clear Overflow
CMP	Compare
COM	Complement
CPX	Compare Index Register
DAA	Decimal Adjust
DEC	Decrement
DES	Decrement Stack Pointer
DEX	Decrement Index Register
EOR	Exclusive OR
INC	Increment
INS	Increment Stack Pointer
INX	Increment Index Register
JMP	Jump
JSR	Jump to Subroutine
LDA	Load Accumulator
LDS	Load Stack Pointer
LDX	Load Index Register
LSR	Logical Shift Right
NEG	Negate
NOP	No Operation
ORA	Inclusive OR Accumulator
PSH	Push Data
PUL	Pull Data
ROL	Rotate Left
ROR	Rotate Right
RTI	Return from Interrupt
RTS	Return from Subroutine
SBA	Subtract Accumulators
SBC	Subtract with Carry
SEC	Set Carry
SEI	Set Interrupt Mask
SEV	Set Overflow
STA	Store Accumulator
STS	Store Stack Register
STX	Store Index Register
SUB	Subtract
SWI	Software Interrupt
TAB	Transfer Accumulators
TAP	Transfer Accumulators to Condition Code Reg.
TBA	Transfer Accumulators
TPA	Transfer Condition Code Reg. to Accumulator
TST	Test
TSX	Transfer Stack Pointer to Index Register
TXS	Transfer Index Register to Stack Pointer
WAI	Wait for Interrupt

TABLE 3 – ACCUMULATOR AND MEMORY INSTRUCTIONS

OPERATIONS	MNEMONIC	IMMED OP	IMMED ~	IMMED =	DIRECT OP	DIRECT ~	DIRECT =	INDEX OP	INDEX ~	INDEX =	EXTND OP	EXTND ~	EXTND =	IMPLIED OP	IMPLIED ~	IMPLIED =	BOOLEAN/ARITHMETIC OPERATION (All register labels refer to contents)	5 H	4 I	3 N	2 Z	1 V	0 C
Add	ADDA	8B	2	2	9B	3	2	AB	5	2	BB	4	3				A + M → A	↕	•	↕	↕	↕	↕
	ADDB	CB	2	2	DB	3	2	EB	5	2	FB	4	3				B + M → B	↕	•	↕	↕	↕	↕
Add Acmltrs	ABA													1B	2	1	A + B → A	↕	•	↕	↕	↕	↕
Add with Carry	ADCA	89	2	2	99	3	2	A9	5	2	B9	4	3				A + M + C → A	↕	•	↕	↕	↕	↕
	ADCB	C9	2	2	D9	3	2	E9	5	2	F9	4	3				B + M + C → B	↕	•	↕	↕	↕	↕
And	ANDA	84	2	2	94	3	2	A4	5	2	B4	4	3				A · M → A	•	•	↕	↕	R	•
	ANDB	C4	2	2	D4	3	2	E4	5	2	F4	4	3				B · M → B	•	•	↕	↕	R	•
Bit Test	BITA	85	2	2	95	3	2	A5	5	2	B5	4	3				A · M	•	•	↕	↕	R	•
	BITB	C5	2	2	D5	3	2	E5	5	2	F5	4	3				B · M	•	•	↕	↕	R	•
Clear	CLR							6F	7	2	7F	6	3				00 → M	•	•	R	S	R	R
	CLRA													4F	2	1	00 → A	•	•	R	S	R	R
	CLRB													5F	2	1	00 → B	•	•	R	S	R	R
Compare	CMPA	81	2	2	91	3	2	A1	5	2	B1	4	3				A − M	•	•	↕	↕	↕	↕
	CMPB	C1	2	2	D1	3	2	E1	5	2	F1	4	3				B − M	•	•	↕	↕	↕	↕
Compare Acmltrs	CBA													11	2	1	A − B	•	•	↕	↕	↕	↕
Complement, 1's	COM							63	7	2	73	6	3				$\overline{M} \rightarrow M$	•	•	↕	↕	R	S
	COMA													43	2	1	$\overline{A} \rightarrow A$	•	•	↕	↕	R	S
	COMB													53	2	1	$\overline{B} \rightarrow B$	•	•	↕	↕	R	S
Complement, 2's (Negate)	NEG							60	7	2	70	6	3				00 − M → M	•	•	↕	↕	①	②
	NEGA													40	2	1	00 − A → A	•	•	↕	↕	①	②
	NEGB													50	2	1	00 − B → B	•	•	↕	↕	①	②
Decimal Adjust, A	DAA													19	2	1	Converts Binary Add. of BCD Characters into BCD Format	•	•	↕	↕	↕	③
Decrement	DEC							6A	7	2	7A	6	3				M − 1 → M	•	•	↕	↕	4	•
	DECA													4A	2	1	A − 1 → A	•	•	↕	↕	4	•
	DECB													5A	2	1	B − 1 → B	•	•	↕	↕	4	•
Exclusive OR	EORA	88	2	2	98	3	2	A8	5	2	B8	4	3				A⊕M → A	•	•	↕	↕	R	•
	EORB	C8	2	2	D8	3	2	E8	5	2	F8	4	3				B⊕M → B	•	•	↕	↕	R	•
Increment	INC							6C	7	2	7C	6	3				M + 1 → M	•	•	↕	↕	⑤	•
	INCA													4C	2	1	A + 1 → A	•	•	↕	↕	⑤	•
	INCB													5C	2	1	B + 1 → B	•	•	↕	↕	⑤	•
Load Acmltr	LDAA	86	2	2	96	3	2	A6	5	2	B6	4	3				M → A	•	•	↕	↕	R	•
	LDAB	C6	2	2	D6	3	2	E6	5	2	F6	4	3				M → B	•	•	↕	↕	R	•
Or, Inclusive	ORAA	8A	2	2	9A	3	2	AA	5	2	BA	4	3				A + M → A	•	•	↕	↕	R	•
	ORAB	CA	2	2	DA	3	2	EA	5	2	FA	4	3				B + M → B	•	•	↕	↕	R	•
Push Data	PSHA													36	4	1	$A \rightarrow M_{SP}$, SP − 1 → SP	•	•	•	•	•	•
	PSHB													37	4	1	$B \rightarrow M_{SP}$, SP − 1 → SP	•	•	•	•	•	•
Pull Data	PULA													32	4	1	SP + 1 → SP, $M_{SP} \rightarrow A$	•	•	•	•	•	•
	PULB													33	4	1	SP + 1 → SP, $M_{SP} \rightarrow B$	•	•	•	•	•	•
Rotate Left	ROL							69	7	2	79	6	3				M	•	•	↕	↕	⑥	↕
	ROLA													49	2	1	A	•	•	↕	↕	⑥	↕
	ROLB													59	2	1	B — C b7 b0	•	•	↕	↕	⑥	↕
Rotate Right	ROR							66	7	2	76	6	3				M	•	•	↕	↕	⑥	↕
	RORA													46	2	1	A	•	•	↕	↕	⑥	↕
	RORB													56	2	1	B — C b7 b0	•	•	↕	↕	⑥	↕
Shift Left, Arithmetic	ASL							68	7	2	78	6	3				M	•	•	↕	↕	⑥	↕
	ASLA													48	2	1	A — 0	•	•	↕	↕	⑥	↕
	ASLB													58	2	1	B — C b7 b0	•	•	↕	↕	⑥	↕
Shift Right, Arithmetic	ASR							67	7	2	77	6	3				M	•	•	↕	↕	⑥	↕
	ASRA													47	2	1	A	•	•	↕	↕	⑥	↕
	ASRB													57	2	1	B — b7 b0 C	•	•	↕	↕	⑥	↕
Shift Right, Logic	LSR							64	7	2	74	6	3				M	•	•	R	↕	⑥	↕
	LSRA													44	2	1	A — 0	•	•	R	↕	⑥	↕
	LSRB													54	2	1	B — b7 b0 C	•	•	R	↕	⑥	↕
Store Acmltr.	STAA				97	4	2	A7	6	2	B7	5	3				A → M	•	•	↕	↕	R	•
	STAB				D7	4	2	E7	6	2	F7	5	3				B → M	•	•	↕	↕	R	•
Subtract	SUBA	80	2	2	90	3	2	A0	5	2	B0	4	3				A − M → A	•	•	↕	↕	↕	↕
	SUBB	C0	2	2	D0	3	2	E0	5	2	F0	4	3				B − M → B	•	•	↕	↕	↕	↕
Subtract Acmltrs.	SBA													10	2	1	A − B → A	•	•	↕	↕	↕	↕
Subtr. with Carry	SBCA	82	2	2	92	3	2	A2	5	2	B2	4	3				A − M − C → A	•	•	↕	↕	↕	↕
	SBCB	C2	2	2	D2	3	2	E2	5	2	F2	4	3				B − M − C → B	•	•	↕	↕	↕	↕
Transfer Acmltrs	TAB													16	2	1	A → B	•	•	↕	↕	R	•
	TBA													17	2	1	B → A	•	•	↕	↕	R	•
Test, Zero or Minus	TST							6D	7	2	7D	6	3				M − 00	•	•	↕	↕	R	R
	TSTA													4D	2	1	A − 00	•	•	↕	↕	R	R
	TSTB													5D	2	1	B − 00	•	•	↕	↕	R	R
																		H	I	N	Z	V	C

ADDRESSING MODES

LEGEND:

OP	Operation Code (Hexadecimal);	+	Boolean Inclusive OR;
~	Number of MPU Cycles;	⊕	Boolean Exclusive OR;
=	Number of Program Bytes;	$\overline{M}$	Complement of M;
+	Arithmetic Plus;	→	Transfer Into;
−	Arithmetic Minus;	0	Bit = Zero;
·	Boolean AND;	00	Byte = Zero;
M_{SP}	Contents of memory location pointed to be Stack Pointer;		

Note – Accumulator addressing mode instructions are included in the column for IMPLIED addressing

CONDITION CODE SYMBOLS:

H	Half-carry from bit 3;
I	Interrupt mask
N	Negative (sign bit)
Z	Zero (byte)
V	Overflow, 2's complement
C	Carry from bit 7
R	Reset Always
S	Set Always
↕	Test and set if true, cleared otherwise
•	Not Affected

TABLE 4 – INDEX REGISTER AND STACK MANIPULATION INSTRUCTIONS

		IMMED			DIRECT			INDEX			EXTND			IMPLIED				COND. CODE REG.					
																		5	4	3	2	1	0
POINTER OPERATIONS	MNEMONIC	OP	~	#	OP	~	#	OP	~	#	OP	~	#	OP	~	#	BOOLEAN/ARITHMETIC OPERATION	H	I	N	Z	V	C
Compare Index Reg	CPX	8C	3	3	9C	4	2	AC	6	2	BC	5	3				$X_H - M, X_L - (M+1)$	•	•	⑦	↕	⑧	•
Decrement Index Reg	DEX													09	4	1	$X - 1 \rightarrow X$	•	•	•	↕	•	•
Decrement Stack Pntr	DES													34	4	1	$SP - 1 \rightarrow SP$	•	•	•	•	•	•
Increment Index Reg	INX													08	4	1	$X + 1 \rightarrow X$	•	•	•	↕	•	•
Increment Stack Pntr	INS													31	4	1	$SP + 1 \rightarrow SP$	•	•	•	•	•	•
Load Index Reg	LDX	CE	3	3	DE	4	2	EE	6	2	FE	5	3				$M \rightarrow X_H, (M+1) \rightarrow X_L$	•	•	⑨	↕	R	•
Load Stack Pntr	LDS	8E	3	3	9E	4	2	AE	6	2	BE	5	3				$M \rightarrow SP_H, (M+1) \rightarrow SP_L$	•	•	⑨	↕	R	•
Store Index Reg	STX				DF	5	2	EF	7	2	FF	6	3				$X_H \rightarrow M, X_L \rightarrow (M+1)$	•	•	⑨	↕	R	•
Store Stack Pntr	STS				9F	5	2	AF	7	2	BF	6	3				$SP_H \rightarrow M, SP_L \rightarrow (M+1)$	•	•	⑨	↕	R	•
Indx Reg → Stack Pntr	TXS													35	4	1	$X - 1 \rightarrow SP$	•	•	•	•	•	•
Stack Pntr → Indx Reg	TSX													30	4	1	$SP + 1 \rightarrow X$	•	•	•	•	•	•

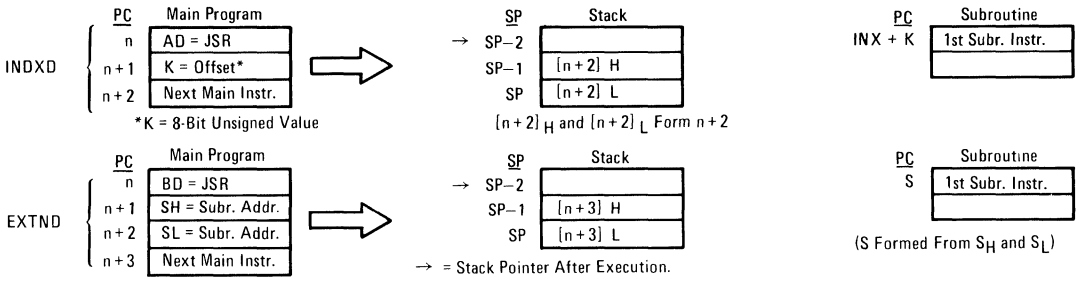
TABLE 5 – JUMP AND BRANCH INSTRUCTIONS

		RELATIVE			INDEX			EXTND			IMPLIED				COND. CODE REG.						
															5	4	3	2	1	0
OPERATIONS	MNEMONIC	OP	~	#	OP	~	#	OP	~	#	OP	~	#	BRANCH TEST	H	I	N	Z	V	C
Branch Always	BRA	20	4	2										None	•	•	•	•	•	•
Branch If Carry Clear	BCC	24	4	2										C = 0	•	•	•	•	•	•
Branch If Carry Set	BCS	25	4	2										C = 1	•	•	•	•	•	•
Branch If = Zero	BEQ	27	4	2										Z = 1	•	•	•	•	•	•
Branch If ≥ Zero	BGE	2C	4	2										$N \oplus V = 0$	•	•	•	•	•	•
Branch If > Zero	BGT	2E	4	2										$Z + (N \oplus V) = 0$	•	•	•	•	•	•
Branch If Higher	BHI	22	4	2										$C + Z = 0$	•	•	•	•	•	•
Branch If ≤ Zero	BLE	2F	4	2										$Z + (N \oplus V) = 1$	•	•	•	•	•	•
Branch If Lower Or Same	BLS	23	4	2										$C + Z = 1$	•	•	•	•	•	•
Branch If < Zero	BLT	2D	4	2										$N \oplus V = 1$	•	•	•	•	•	•
Branch If Minus	BMI	2B	4	2										N = 1	•	•	•	•	•	•
Branch If Not Equal Zero	BNE	26	4	2										Z = 0	•	•	•	•	•	•
Branch If Overflow Clear	BVC	28	4	2										V = 0	•	•	•	•	•	•
Branch If Overflow Set	BVS	29	4	2										V = 1	•	•	•	•	•	•
Branch If Plus	BPL	2A	4	2										N = 0	•	•	•	•	•	•
Branch To Subroutine	BSR	8D	8	2											•	•	•	•	•	•
Jump	JMP				6E	4	2	7E	3	3				See Special Operations	•	•	•	•	•	•
Jump To Subroutine	JSR				AD	8	2	BD	9	3					•	•	•	•	•	•
No Operation	NOP										01	2	1	Advances Prog. Cntr. Only	•	•	•	•	•	•
Return From Interrupt	RTI										3B	10	1		———			⑩		———
Return From Subroutine	RTS										39	5	1		•	•	•	•	•	•
Software Interrupt	SWI										3F	12	1	See Special Operations	•	•	•	•	•	•
Wait for Interrupt*	WAI										3E	9	1		•	⑪	•	•	•	•

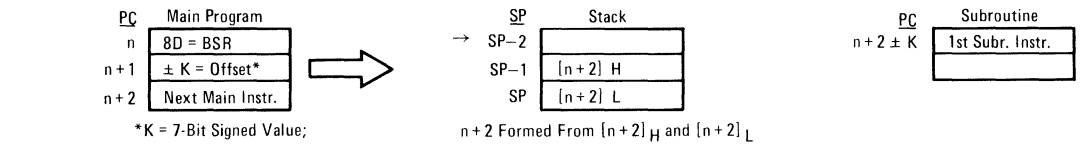
*WAI puts Address Bus, R/W, and Data Bus in the three-state mode while VMA is held low.

SPECIAL OPERATIONS

JSR, JUMP TO SUBROUTINE:

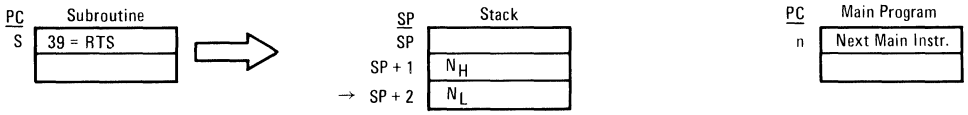


BSR, BRANCH TO SUBROUTINE:



JMP, JUMP:

RTS, RETURN FROM SUBROUTINE:



RTI, RETURN FROM INTERRUPT:

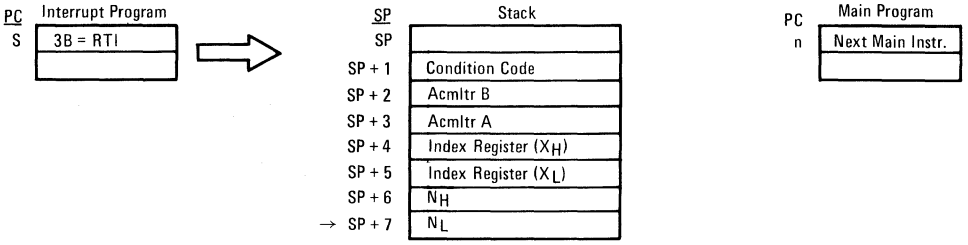


TABLE 6 – CONDITION CODE REGISTER MANIPULATION INSTRUCTIONS

OPERATIONS	MNEMONIC	IMPLIED OP	~	#	BOOLEAN OPERATION	COND. CODE REG. 5 H	4 I	3 N	2 Z	1 V	0 C
Clear Carry	CLC	0C	2	1	0 → C	•	•	•	•	•	R
Clear Interrupt Mask	CLI	0E	2	1	0 → I	•	R	•	•	•	•
Clear Overflow	CLV	0A	2	1	0 → V	•	•	•	•	R	•
Set Carry	SEC	0D	2	1	1 → C	•	•	•	•	•	S
Set Interrupt Mask	SEI	0F	2	1	1 → I	•	S	•	•	•	•
Set Overflow	SEV	0B	2	1	1 → V	•	•	•	•	S	•
Acmltr A → CCR	TAP	06	2	1	A → CCR	———			(12)		———
CCR → Acmltr A	TPA	07	2	1	CCR → A	•	•	•	•	•	•

CONDITION CODE REGISTER NOTES: (Bit set if test is true and cleared otherwise)

1 (Bit V) Test: Result = 10000000?
2 (Bit C) Test: Result = 00000000?
3 (Bit C) Test: Decimal value of most significant BCD Character greater than nine? (Not cleared if previously set.)
4 (Bit V) Test: Operand = 10000000 prior to execution?
5 (Bit V) Test: Operand = 01111111 prior to execution?
6 (Bit V) Test: Set equal to result of N⊕C after shift has occurred.
7 (Bit N) Test: Sign bit of most significant (MS) byte = 1?
8 (Bit V) Test: 2's complement overflow from subtraction of MS bytes?
9 (Bit N) Test: Result less than zero? (Bit 15 = 1)
10 (All) Load Condition Code Register from Stack. (See Special Operations)
11 (Bit I) Set when interrupt occurs. If previously set, a Non-Maskable Interrupt is required to exit the wait state.
12 (All) Set according to the contents of Accumulator A.

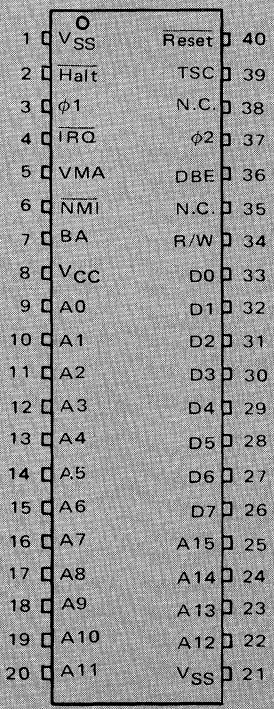
TABLE 7 – INSTRUCTION ADDRESSING MODES AND ASSOCIATED EXECUTION TIMES
(Times in Machine Cycles)

	(Dual Operand)	ACCX	Immediate	Direct	Extended	Indexed	Implied	Relative
ABA		•	•	•	•	•	2	•
ADC	x	•	2	3	4	5	•	•
ADD	x	•	2	3	4	5	•	•
AND	x	•	2	3	4	5	•	•
ASL		2	•	•	6	7	•	•
ASR		2	•	•	6	7	•	•
BCC		•	•	•	•	•	•	4
BCS		•	•	•	•	•	•	4
BEA		•	•	•	•	•	•	4
BGE		•	•	•	•	•	•	4
BGT		•	•	•	•	•	•	4
BHI		•	•	•	•	•	•	4
BIT	x	•	2	3	4	5	•	•
BLE		•	•	•	•	•	•	4
BLS		•	•	•	•	•	•	4
BLT		•	•	•	•	•	•	4
BMI		•	•	•	•	•	•	4
BNE		•	•	•	•	•	•	4
BPL		•	•	•	•	•	•	4
BRA		•	•	•	•	•	•	4
BSR		•	•	•	•	•	•	8
BVC		•	•	•	•	•	•	4
BVS		•	•	•	•	•	•	4
CBA		•	•	•	•	•	2	•
CLC		•	•	•	•	•	2	•
CLI		•	•	•	•	•	2	•
CLR		2	•	•	6	7	•	•
CLV		•	•	•	•	•	2	•
CMP	x	•	2	3	4	5	•	•
COM		2	•	•	6	7	•	•
CPX		•	3	4	5	6	•	•
DAA		•	•	•	•	•	2	•
DEC		2	•	•	6	7	•	•
DES		•	•	•	•	•	4	•
DEX		•	•	•	•	•	4	•
EOR	x	•	2	3	4	5	•	•

	(Dual Operand)	ACCX	Immediate	Direct	Extended	Indexed	Implied
INC		2	•	•	6	7	•
INS		•	•	•	•	•	4
INX		•	•	•	•	•	4
JMP		•	•	•	3	4	•
JSR		•	•	•	9	8	•
LDA	x	•	2	3	4	5	•
LDS		•	3	4	5	6	•
LDX		•	3	4	5	6	•
LSR		2	•	•	6	7	•
NEG		2	•	•	6	7	•
NOP		•	•	•	•	•	2
ORA	x	•	2	3	4	5	•
PSH		•	•	•	•	•	4
PUL		•	•	•	•	•	4
ROL		2	•	•	6	7	•
ROR		2	•	•	6	7	•
RTI		•	•	•	•	•	10
RTS		•	•	•	•	•	5
SBA		•	•	•	•	•	2
SBC	x	•	2	3	4	5	•
SEC		•	•	•	•	•	2
SEI		•	•	•	•	•	2
SEV		•	•	•	•	•	2
STA	x	•	•	4	5	6	•
STS		•	•	5	6	7	•
STX		•	•	5	6	7	•
SUB	x	•	2	3	4	5	•
SWI		•	•	•	•	•	12
TAB		•	•	•	•	•	2
TAP		•	•	•	•	•	2
TBA		•	•	•	•	•	2
TPA		•	•	•	•	•	2
TST		2	•	•	6	7	•
TSX		•	•	•	•	•	4
TSX		•	•	•	•	•	4
WAI		•	•	•	•	•	9

NOTE: Interrupt time is 12 cycles from the end of the instruction being executed, except following a WAI instruction. Then it is 4 cycles.

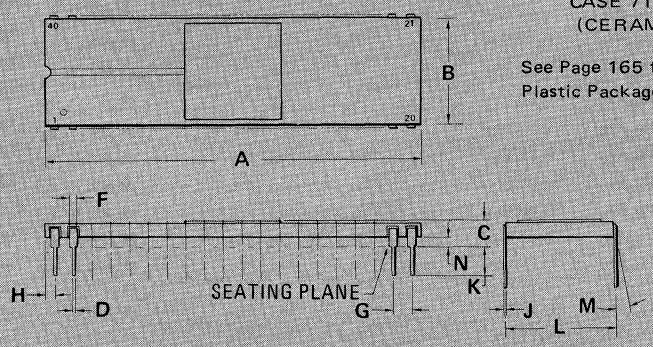
PIN ASSIGNMENT



PACKAGE DIMENSIONS

CASE 715-02
(CERAMIC)

See Page 165 for Plastic Package dimensions.



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	50.29	51.31	1.980	2.020
B	14.86	15.62	0.585	0.615
C	2.54	4.19	0.100	0.165
D	0.38	0.53	0.015	0.021
F	0.76	1.40	0.030	0.055
G	2.54 BSC		0.100 BSC	
H	0.76	1.78	0.030	0.070
J	0.20	0.33	0.008	0.013
K	2.54	4.19	0.100	0.165
L	14.60	15.37	0.575	0.605
M	–	10^0	–	10^0
N	0.51	1.52	0.020	0.060

NOTE:
1. LEADS, TRUE POSITIONED WITHIN 0.25 mm (0.010) DIA (AT SEATING PLANE), AT MAX. MAT'L CONDITION.

SUMMARY OF CYCLE BY CYCLE OPERATION

Table 8 provides a detailed description of the information present on the Address Bus, Data Bus, Valid Memory Address line (VMA), and the Read/Write line (R/W) during each cycle for each instruction.

This information is useful in comparing actual with expected results during debug of both software and hardware as the control program is executed. The information is categorized in groups according to Addressing Mode and Number of Cycles per instruction. (In general, instructions with the same Addressing Mode and Number of Cycles execute in the same manner; exceptions are indicated in the table.)

TABLE 8 – OPERATION SUMMARY

Address Mode and Instructions	Cycles	Cycle #	VMA Line	Address Bus	R/W Line	Data Bus
IMMEDIATE						
ADC EOR ADD LDA AND ORA BIT SBC CMP SUB	2	1	1	Op Code Address	1	Op Code
		2	1	Op Code Address + 1	1	Operand Data
CPX LDS LDX	3	1	1	Op Code Address	1	Op Code
		2	1	Op Code Address + 1	1	Operand Data (High Order Byte)
		3	1	Op Code Address + 2	1	Operand Data (Low Order Byte)
DIRECT						
ADC EOR ADD LDA AND ORA BIT SBC CMP SUB	3	1	1	Op Code Address	1	Op Code
		2	1	Op Code Address + 1	1	Address of Operand
		3	1	Address of Operand	1	Operand Data
CPX LDS LDX	4	1	1	Op Code Address	1	Op Code
		2	1	Op Code Address + 1	1	Address of Operand
		3	1	Address of Operand	1	Operand Data (High Order Byte)
		4	1	Operand Address + 1	1	Operand Data (Low Order Byte)
STA	4	1	1	Op Code Address	1	Op Code
		2	1	Op Code Address + 1	1	Destination Address
		3	0	Destination Address	1	Irrelevant Data (Note 1)
		4	1	Destination Address	0	Data from Accumulator
STS STX	5	1	1	Op Code Address	1	Op Code
		2	1	Op Code Address + 1	1	Address of Operand
		3	0	Address of Operand	1	Irrelevant Data (Note 1)
		4	1	Address of Operand	0	Register Data (High Order Byte)
		5	1	Address of Operand + 1	0	Register Data (Low Order Byte)
INDEXED						
JMP	4	1	1	Op Code Address	1	Op Code
		2	1	Op Code Address + 1	1	Offset
		3	0	Index Register	1	Irrelevant Data (Note 1)
		4	0	Index Register Plus Offset (w/o Carry)	1	Irrelevant Data (Note 1)
ADC EOR ADD LDA AND ORA BIT SBC CMP SUB	5	1	1	Op Code Address	1	Op Code
		2	1	Op Code Address + 1	1	Offset
		3	0	Index Register	1	Irrelevant Data (Note 1)
		4	0	Index Register Plus Offset (w/o Carry)	1	Irrelevant Data (Note 1)
		5	1	Index Register Plus Offset	1	Operand Data
CPX LDS LDX	6	1	1	Op Code Address	1	Op Code
		2	1	Op Code Address + 1	1	Offset
		3	0	Index Register	1	Irrelevant Data (Note 1)
		4	0	Index Register Plus Offset (w/o Carry)	1	Irrelevant Data (Note 1)
		5	1	Index Register Plus Offset	1	Operand Data (High Order Byte)
		6	1	Index Register Plus Offset + 1	1	Operand Data (Low Order Byte)

TABLE 8 – OPERATION SUMMARY (Continued)

Address Mode and Instructions	Cycles	Cycle #	VMA Line	Address Bus	R/W Line	Data Bus
INDEXED (Continued)						
STA	6	1	1	Op Code Address	1	Op Code
		2	1	Op Code Address + 1	1	Offset
		3	0	Index Register	1	Irrelevant Data (Note 1)
		4	0	Index Register Plus Offset (w/o Carry)	1	Irrelevant Data (Note 1)
		5	0	Index Register Plus Offset	1	Irrelevant Data (Note 1)
		6	1	Index Register Plus Offset	0	Operand Data
ASL LSR ASR NEG CLR ROL COM ROR DEC TST INC	7	1	1	Op Code Address	1	Op Code
		2	1	Op Code Address + 1	1	Offset
		3	0	Index Register	1	Irrelevant Data (Note 1)
		4	0	Index Register Plus Offset (w/o Carry)	1	Irrelevant Data (Note 1)
		5	1	Index Register Plus Offset	1	Current Operand Data
		6	0	Index Register Plus Offset	1	Irrelevant Data (Note 1)
		7	1/0 (Note 3)	Index Register Plus Offset	0	New Operand Data (Note 3)
STS STX	7	1	1	Op Code Address	1	Op Code
		2	1	Op Code Address + 1	1	Offset
		3	0	Index Register	1	Irrelevant Data (Note 1)
		4	0	Index Register Plus Offset (w/o Carry)	1	Irrelevant Data (Note 1)
		5	0	Index Register Plus Offset	1	Irrelevant Data (Note 1)
		6	1	Index Register Plus Offset	0	Operand Data (High Order Byte)
		7	1	Index Register Plus Offset + 1	0	Operand Data (Low Order Byte)
JSR	8	1	1	Op Code Address	1	Op Code
		2	1	Op Code Address + 1	1	Offset
		3	0	Index Register	1	Irrelevant Data (Note 1)
		4	1	Stack Pointer	0	Return Address (Low Order Byte)
		5	1	Stack Pointer – 1	0	Return Address (High Order Byte)
		6	0	Stack Pointer – 2	1	Irrelevant Data (Note 1)
		7	0	Index Register	1	Irrelevant Data (Note 1)
		8	0	Index Register Plus Offset (w/o Carry)	1	Irrelevant Data (Note 1)
EXTENDED						
JMP	3	1	1	Op Code Address	1	Op Code
		2	1	Op Code Address + 1	1	Jump Address (High Order Byte)
		3	1	Op Code Address + 2	1	Jump Address (Low Order Byte)
ADC EOR ADD LDA AND ORA BIT SBC CMP SUB	4	1	1	Op Code Address	1	Op Code
		2	1	Op Code Address + 1	1	Address of Operand (High Order Byte)
		3	1	Op Code Address + 2	1	Address of Operand (Low Order Byte)
		4	1	Address of Operand	1	Operand Data
CPX LDS LDX	5	1	1	Op Code Address	1	Op Code
		2	1	Op Code Address + 1	1	Address of Operand (High Order Byte)
		3	1	Op Code Address + 2	1	Address of Operand (Low Order Byte)
		4	1	Address of Operand	1	Operand Data (High Order Byte)
		5	1	Address of Operand + 1	1	Operand Data (Low Order Byte)
STA A STA B	5	1	1	Op Code Address	1	Op Code
		2	1	Op Code Address + 1	1	Destination Address (High Order Byte)
		3	1	Op Code Address + 2	1	Destination Address (Low Order Byte)
		4	0	Operand Destination Address	1	Irrelevant Data (Note 1)
		5	1	Operand Destination Address	0	Data from Accumulator
ASL LSR ASR NEG CLR ROL COM ROR DEC TST INC	6	1	1	Op Code Address	1	Op Code
		2	1	Op Code Address + 1	1	Address of Operand (High Order Byte)
		3	1	Op Code Address + 2	1	Address of Operand (Low Order Byte)
		4	1	Address of Operand	1	Current Operand Data
		5	0	Address of Operand	1	Irrelevant Data (Note 1)
		6	1/0 (Note 3)	Address of Operand	0	New Operand Data (Note 3)

TABLE 8 – OPERATION SUMMARY (Continued)

Address Mode and Instructions	Cycles	Cycle #	VMA Line	Address Bus	R/W Line	Data Bus
EXTENDED (Continued)						
STS STX	6	1	1	Op Code Address	1	Op Code
		2	1	Op Code Address + 1	1	Address of Operand (High Order Byte)
		3	1	Op Code Address + 2	1	Address of Operand (Low Order Byte)
		4	0	Address of Operand	1	Irrelevant Data (Note 1)
		5	1	Address of Operand	0	Operand Data (High Order Byte)
		6	1	Address of Operand + 1	0	Operand Data (Low Order Byte)
JSR	9	1	1	Op Code Address	1	Op Code
		2	1	Op Code Address + 1	1	Address of Subroutine (High Order Byte)
		3	1	Op Code Address + 2	1	Address of Subroutine (Low Order Byte)
		4	1	Subroutine Starting Address	1	Op Code of Next Instruction
		5	1	Stack Pointer	0	Return Address (Low Order Byte)
		6	1	Stack Pointer – 1	0	Return Address (High Order Byte)
		7	0	Stack Pointer – 2	1	Irrelevant Data (Note 1)
		8	0	Op Code Address + 2	1	Irrelevant Data (Note 1)
		9	1	Op Code Address + 2	1	Address of Subroutine (Low Order Byte)
INHERENT						
ABA DAA SEC ASL DEC SEI ASR INC SEV CBA LSR TAB CLC NEG TAP CLI NOP TBA CLR ROL TPA CLV ROR TST COM SBA	2	1	1	Op Code Address	1	Op Code
		2	1	Op Code Address + 1	1	Op Code of Next Instruction
DES DEX INS INX	4	1	1	Op Code Address	1	Op Code
		2	1	Op Code Address + 1	1	Op Code of Next Instruction
		3	0	Previous Register Contents	1	Irrelevant Data (Note 1)
		4	0	New Register Contents	1	Irrelevant Data (Note 1)
PSH	4	1	1	Op Code Address	1	Op Code
		2	1	Op Code Address + 1	1	Op Code of Next Instruction
		3	1	Stack Pointer	0	Accumulator Data
		4	0	Stack Pointer – 1	1	Accumulator Data
PUL	4	1	1	Op Code Address	1	Op Code
		2	1	Op Code Address + 1	1	Op Code of Next Instruction
		3	0	Stack Pointer	1	Irrelevant Data (Note 1)
		4	1	Stack Pointer + 1	1	Operand Data from Stack
TSX	4	1	1	Op Code Address	1	Op Code
		2	1	Op Code Address + 1	1	Op Code of Next Instruction
		3	0	Stack Pointer	1	Irrelevant Data (Note 1)
		4	0	New Index Register	1	Irrelevant Data (Note 1)
TXS	4	1	1	Op Code Address	1	Op Code
		2	1	Op Code Address + 1	1	Op Code of Next Instruction
		3	0	Index Register	1	Irrelevant Data
		4	0	New Stack Pointer	1	Irrelevant Data
RTS	5	1	1	Op Code Address	1	Op Code
		2	1	Op Code Address + 1	1	Irrelevant Data (Note 2)
		3	0	Stack Pointer	1	Irrelevant Data (Note 1)
		4	1	Stack Pointer + 1	1	Address of Next Instruction (High Order Byte)
		5	1	Stack Pointer + 2	1	Address of Next Instruction (Low Order Byte)

TABLE 8 – OPERATION SUMMARY (Continued)

Address Mode and Instructions	Cycles	Cycle #	VMA Line	Address Bus	R/W Line	Data Bus
INHERENT (Continued)						
WAI	9	1	1	Op Code Address	1	Op Code
		2	1	Op Code Address + 1	1	Op Code of Next Instruction
		3	1	Stack Pointer	0	Return Address (Low Order Byte)
		4	1	Stack Pointer – 1	0	Return Address (High Order Byte)
		5	1	Stack Pointer – 2	0	Index Register (Low Order Byte)
		6	1	Stack Pointer – 3	0	Index Register (High Order Byte)
		7	1	Stack Pointer – 4	0	Contents of Accumulator A
		8	1	Stack Pointer – 5	0	Contents of Accumulator B
		9	1	Stack Pointer – 6 (Note 4)	1	Contents of Cond. Code Register
RTI	10	1	1	Op Code Address	1	Op Code
		2	1	Op Code Address + 1	1	Irrelevant Data (Note 2)
		3	0	Stack Pointer	1	Irrelevant Data (Note 1)
		4	1	Stack Pointer + 1	1	Contents of Cond. Code Register from Stack
		5	1	Stack Pointer + 2	1	Contents of Accumulator B from Stack
		6	1	Stack Pointer + 3	1	Contents of Accumulator A from Stack
		7	1	Stack Pointer + 4	1	Index Register from Stack (High Order Byte)
		8	1	Stack Pointer + 5	1	Index Register from Stack (Low Order Byte)
		9	1	Stack Pointer + 6	1	Next Instruction Address from Stack (High Order Byte)
		10	1	Stack Pointer + 7	1	Next Instruction Address from Stack (Low Order Byte)
SWI	12	1	1	Op Code Address	1	Op Code
		2	1	Op Code Address + 1	1	Irrelevant Data (Note 1)
		3	1	Stack Pointer	0	Return Address (Low Order Byte)
		4	1	Stack Pointer – 1	0	Return Address (High Order Byte)
		5	1	Stack Pointer – 2	0	Index Register (Low Order Byte)
		6	1	Stack Pointer – 3	0	Index Register (High Order Byte)
		7	1	Stack Pointer – 4	0	Contents of Accumulator A
		8	1	Stack Pointer – 5	0	Contents of Accumulator B
		9	1	Stack Pointer – 6	0	Contents of Cond. Code Register
		10	0	Stack Pointer – 7	1	Irrelevant Data (Note 1)
		11	1	Vector Address FFFA (Hex)	1	Address of Subroutine (High Order Byte)
		12	1	Vector Address FFFB (Hex)	1	Address of Subroutine (Low Order Byte)
RELATIVE						
BCC BHI BNE BCS BLE BPL BEQ BLS BRA BGE BLT BVC BGT BMI BVS	4	1	1	Op Code Address	1	Op Code
		2	1	Op Code Address + 1	1	Branch Offset
		3	0	Op Code Address + 2	1	Irrelevant Data (Note 1)
		4	0	Branch Address	1	Irrelevant Data (Note 1)
BSR	8	1	1	Op Code Address	1	Op Code
		2	1	Op Code Address + 1	1	Branch Offset
		3	0	Return Address of Main Program	1	Irrelevant Data (Note 1)
		4	1	Stack Pointer	0	Return Address (Low Order Byte)
		5	1	Stack Pointer – 1	0	Return Address (High Order Byte)
		6	0	Stack Pointer – 2	1	Irrelevant Data (Note 1)
		7	0	Return Address of Main Program	1	Irrelevant Data (Note 1)
		8	0	Subroutine Address	1	Irrelevant Data (Note 1)

Note 1. If device which is addressed during this cycle uses VMA, then the Data Bus will go to the high impedance three-state condition. Depending on bus capacitance, data from the previous cycle may be retained on the Data Bus.
Note 2. Data is ignored by the MPU.
Note 3. For TST, VMA = 0 and Operand data does not change.
Note 4. While the MPU is waiting for the interrupt, Bus Available will go high indicating the following states of the control lines: VMA is low; Address Bus, R/W, and Data Bus are all in the high impedance state.

MOTOROLA Semiconductors
BOX 20912 • PHOENIX, ARIZONA 85036

MC6820

(0 to 70°C; L or P Suffix)

MC6820C

(-40 to 85°C; L Suffix only)

PERIPHERAL INTERFACE ADAPTER (PIA)

The MC6820 Peripheral Interface Adapter provides the universal means of interfacing peripheral equipment to the MC6800 Microprocessing Unit (MPU). This device is capable of interfacing the MPU to peripherals through two 8-bit bidirectional peripheral data buses and four control lines. No external logic is required for interfacing to most peripheral devices.

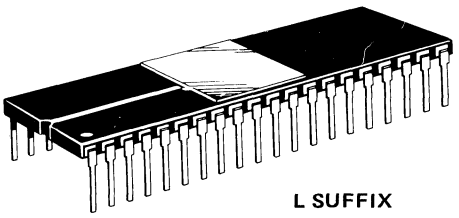
The functional configuration of the PIA is programmed by the MPU during system initialization. Each of the peripheral data lines can be programmed to act as an input or output, and each of the four control/interrupt lines may be programmed for one of several control modes. This allows a high degree of flexibility in the over-all operation of the interface.

- 8-Bit Bidirectional Data Bus for Communication with the MPU
- Two Bidirectional 8-Bit Buses for Interface to Peripherals
- Two Programmable Control Registers
- Two Programmable Data Direction Registers
- Four Individually-Controlled Interrupt Input Lines; Two Usable as Peripheral Control Outputs
- Handshake Control Logic for Input and Output Peripheral Operation
- High-Impedance 3-State and Direct Transistor Drive Peripheral Lines
- Program Controlled Interrupt and Interrupt Disable Capability
- CMOS Drive Capability on Side A Peripheral Lines

MOS

(N-CHANNEL, SILICON-GATE)

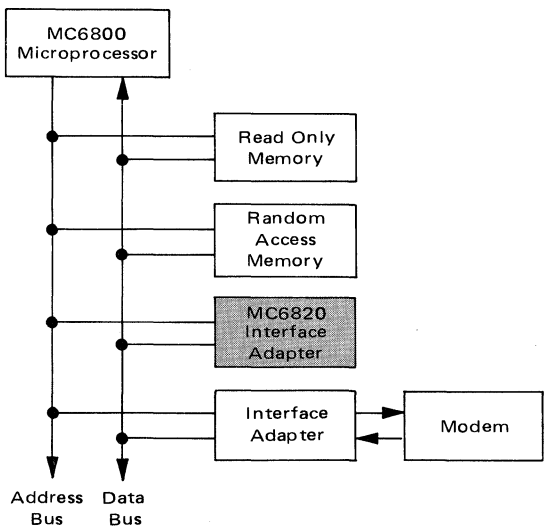
PERIPHERAL INTERFACE ADAPTER



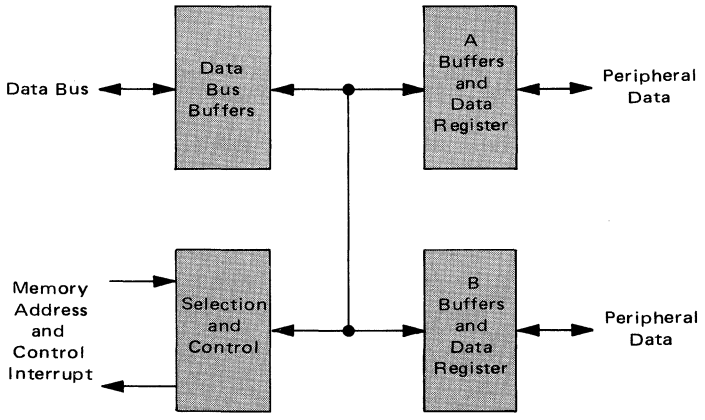
L SUFFIX
CERAMIC PACKAGE
CASE 715

NOT SHOWN: **P SUFFIX**
PLASTIC PACKAGE
CASE 711

M6800 MICROCOMPUTER FAMILY BLOCK DIAGRAM



MC6820 PERIPHERAL INTERFACE ADAPTER BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V ±5%, V_{SS} = 0, T_A = 0 to 70°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Input High Voltage — Enable	V_{IH}	V_{SS} + 2.4	–	V_{CC}	Vdc
Input High Voltage — Other Inputs		V_{SS} + 2.0	–	V_{CC}	
Input Low Voltage — Enable	V_{IL}	V_{SS} -0.3	–	V_{SS} + 0.4	Vdc
Input Low Voltage — Other Inputs		V_{SS} -0.3	–	V_{SS} + 0.8	
Input Leakage Current (R/W, $\overline{Reset}$, RS0, RS1, CS0, CS1, $\overline{CS2}$, CA1, CB1, Enable) (V_{in} = 0 to 5.25 Vdc)	I_{in}	–	1.0	2.5	μAdc
Three-State (Off State) Input Current (D0-D7, PB0-PB7, CB2) (V_{in} = 0.4 to 2.4 Vdc)	I_{TSI}	–	2.0	10	μAdc
Input High Current (PA0-PA7, CA2) (V_{IH} = 2.4 Vdc)	I_{IH}	-100	-250	–	μAdc
Input Low Current (PA0-PA7, CA2) (V_{IL} = 0.4 Vdc)	I_{IL}	–	-1.0	-1.6	mAdc
Output High Voltage	V_{OH}				Vdc
(I_{Load} = -205 μAdc, Enable Pulse Width < 25 μs) D0-D7		V_{SS} + 2.4	–	–	
(I_{Load} = -100 μAdc, Enable Pulse Width <25 μs) Other Outputs		V_{SS} + 2.4	–	–	
Output Low Voltage (I_{Load} = 1.6 mAdc, Enable Pulse Width < 25 μs)	V_{OL}	–	–	V_{SS} + 0.4	Vdc
Output High Current (Sourcing)	I_{OH}				
(V_{OH} = 2.4 Vdc) D0-D7		-205	–	–	μAdc
Other Outputs		-100	–	–	μAdc
(V_O = 1.5 Vdc, the current for driving other than TTL, e.g., Darlington Base) PB0-PB7, CB2		-1.0	-2.5	-10	mAdc
Output Low Current (Sinking) (V_{OL} = 0.4 Vdc)	I_{OL}	1.6	–	–	mAdc
Output Leakage Current (Off State) ($\overline{IRQA}$, $\overline{IRQB}$) (V_{OH} = 2.4 Vdc)	I_{LOH}	–	1.0	10	μAdc
Power Dissipation	P_D	–	–	650	mW
Input Capacitance — Enable	C_{in}	–	–	20	pF
(V_{in} = 0, T_A = 25°C, f = 1.0 MHz) D0-D7		–	–	12.5	
PA0-PA7, PB0-PB7, CA2, CB2		–	–	10	
R/W, $\overline{Reset}$, RS0, RS1, CS0, CS1, $\overline{CS2}$, CA1, CB1		–	–	7.5	
Output Capacitance ($\overline{IRQA}$, $\overline{IRQB}$)	C_{out}	–	–	5.0	pF
(V_{in} = 0, T_A = 25°C, f = 1.0 MHz) PB0-PB7		–	–	10	
Peripheral Data Setup Time (Figure 1)	t_{PDSU}	200	–	–	ns
Delay Time, Enable negative transition to CA2 negative transition (Figure 2, 3)	t_{CA2}	–	–	1.0	μs
Delay Time, Enable negative transition to CA2 positive transition (Figure 2)	t_{RS1}	–	–	1.0	μs
Rise and Fall Times for CA1 and CA2 input signals (Figure 3)	t_r,t_f	–	–	1.0	μs
Delay Time from CA1 active transition to CA2 positive transition (Figure 3)	t_{RS2}	–	–	2.0	μs
Delay Time, Enable negative transition to Peripheral Data valid (Figures 4, 5)	t_{PDW}	–	–	1.0	μs
Delay Time, Enable negative transition to Peripheral CMOS Data Valid (V_{CC} – 30% V_{CC}, Figure 4; Figure 12 Load C) PA0-PA7, CA2	t_{CMOS}	–	–	2.0	μs
Delay Time, Enable positive transition to CB2 negative transition (Figure 6, 7)	t_{CB2}	–	–	1.0	μs
Delay Time, Peripheral Data valid to CB2 negative transition (Figure 5)	t_{DC}	20	–	–	ns
Delay Time, Enable positive transition to CB2 positive transition (Figure 6)	t_{RS1}	–	–	1.0	μs
Rise and Fall Time for CB1 and CB2 input signals (Figure 7)	t_r,t_f	–	–	1.0	μs
Delay Time, CB1 active transition to CB2 positive transition (Figure 7)	t_{RS2}	–	–	2.0	μs
Interrupt Release Time, $\overline{IRQA}$ and $\overline{IRQB}$ (Figure 8)	t_{IR}	–	–	1.6	μs
Reset Low Time* (Figure 9)	t_{RL}	2.0	–	–	μs

*The Reset line must be high a minimum of 1.0 μs before addressing the PIA.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.3 to +7.0	Vdc
Input Voltage	V_{in}	−0.3 to +7.0	Vdc
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	−55 to +150	°C
Thermal Resistance	θ_{JA}	82.5	°C/W

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

BUS TIMING CHARACTERISTICS

READ (Figures 10 and 12)

Characteristic	Symbol	Min	Typ	Max	Unit
Enable Cycle Time	t_{cycE}	1.0	–	–	μs
Enable Pulse Width, High	PW_{EH}	0.45	–	25	μs
Enable Pulse Width, Low	PW_{EL}	0.43	–	–	μs
Setup Time, Address and R/W valid to Enable positive transition	t_{AS}	160	–	–	ns
Data Delay Time	t_{DDR}	–	–	320	ns
Data Hold Time	t_H	10	–	–	ns
Address Hold Time	t_{AH}	10	–	–	ns
Rise and Fall Time for Enable input	t_{Er}, t_{Ef}	–	–	25	ns

WRITE (Figures 11 and 12)

Enable Cycle Time	t_{cycE}	1.0	–	–	μs
Enable Pulse Width, High	PW_{EH}	0.45	–	25	μs
Enable Pulse Width, Low	PW_{EL}	0.43	–	–	μs
Setup Time, Address and R/W valid to Enable positive transition	t_{AS}	160	–	–	ns
Data Setup Time	t_{DSW}	195	–	–	ns
Data Hold Time	t_H	10	–	–	ns
Address Hold Time	t_{AH}	10	–	–	ns
Rise and Fall Time for Enable input	t_{Er}, t_{Ef}	–	–	25	ns

FIGURE 1 – PERIPHERAL DATA SETUP TIME
(Read Mode)

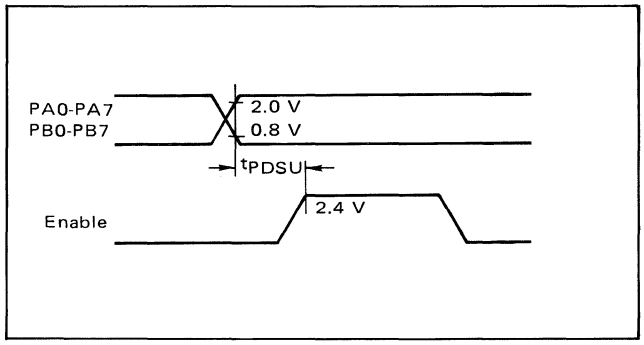
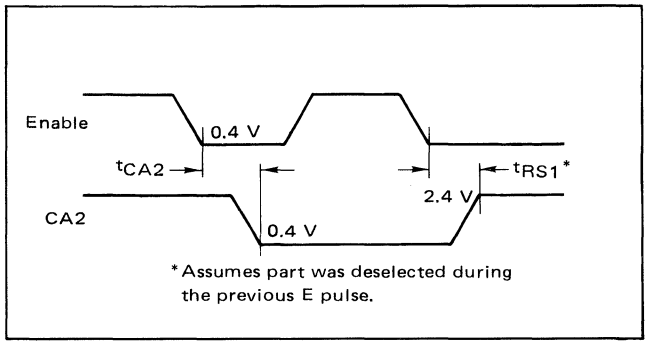


FIGURE 2 – CA2 DELAY TIME
(Read Mode; CRA-5 = CRA-3 = 1, CRA-4 = 0)



*Assumes part was deselected during the previous E pulse.

FIGURE 3 – CA2 DELAY TIME
(Read Mode; CRA-5 = 1, CRA-3 = CRA-4 = 0)

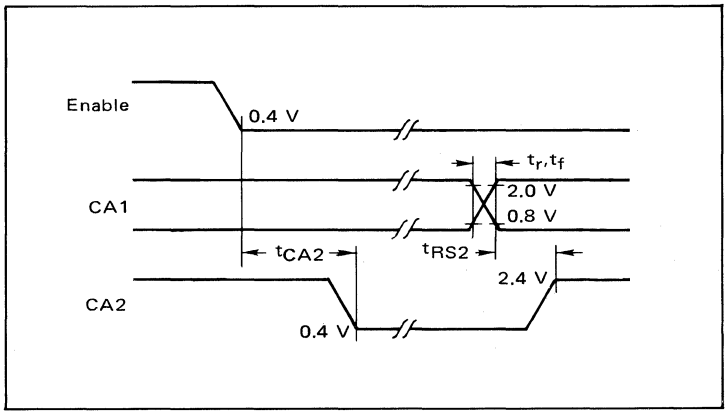


FIGURE 4 – PERIPHERAL CMOS DATA DELAY TIMES
(Write Mode; CRA-5 = CRA-3 = 1, CRA-4 = 0)

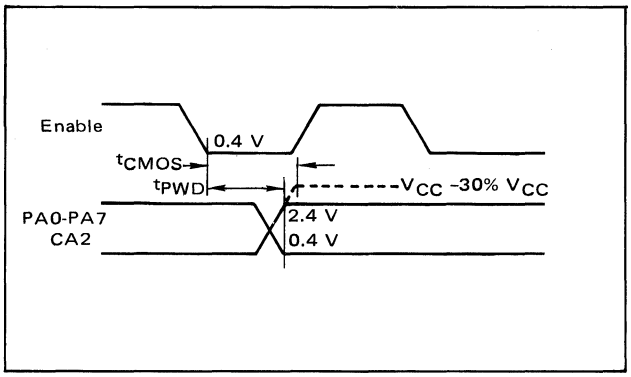
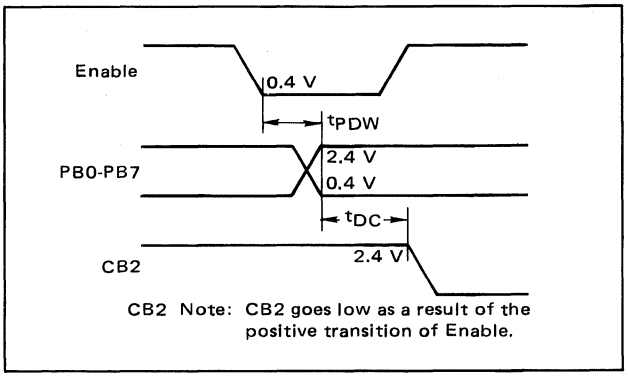
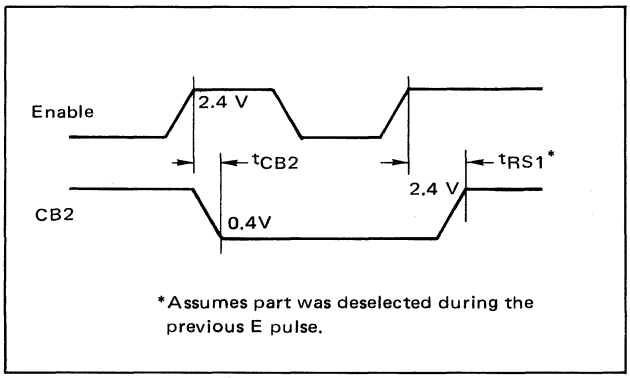


FIGURE 5 – PERIPHERAL DATA AND CB2 DELAY TIMES
(Write Mode; CRB-5 = CRB-3 = 1, CRB-4 = 0)



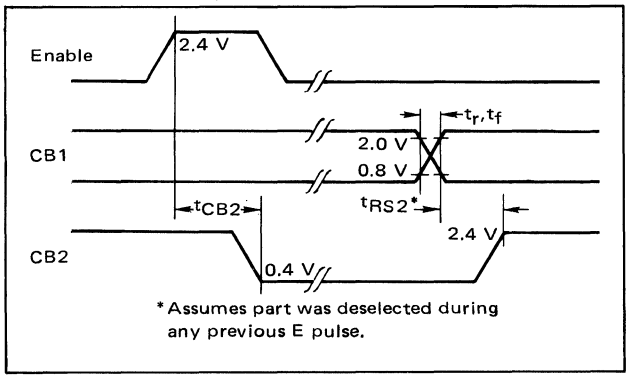
CB2 Note: CB2 goes low as a result of the positive transition of Enable.

FIGURE 6 – CB2 DELAY TIME
(Write Mode; CRB-5 = CRB-3 = 1, CRB-4 = 0)



*Assumes part was deselected during the previous E pulse.

FIGURE 7 – CB2 DELAY TIME
(Write Mode; CRB-5 = 1, CRB-3 = CRB-4 = 0)



*Assumes part was deselected during any previous E pulse.

FIGURE 8 – $\overline{IRQ}$ RELEASE TIME

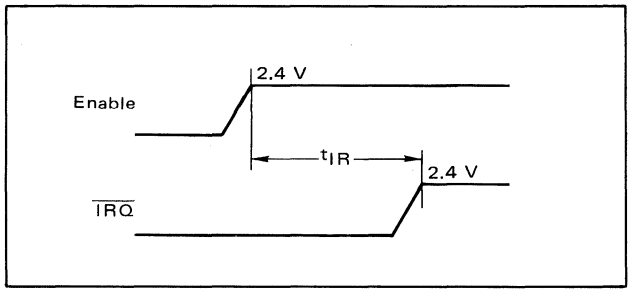
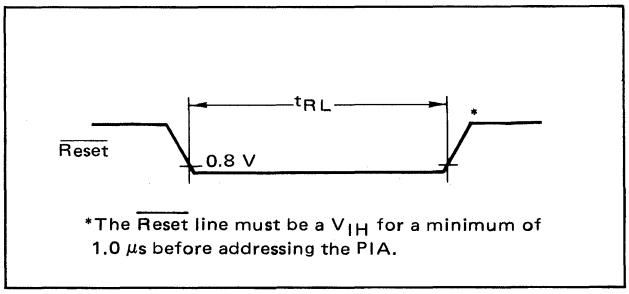


FIGURE 9 – $\overline{RESET}$ LOW TIME



*The $\overline{Reset}$ line must be a V_{IH} for a minimum of 1.0 μs before addressing the PIA.

FIGURE 10 – BUS READ TIMING CHARACTERISTICS
(Read Information from PIA)

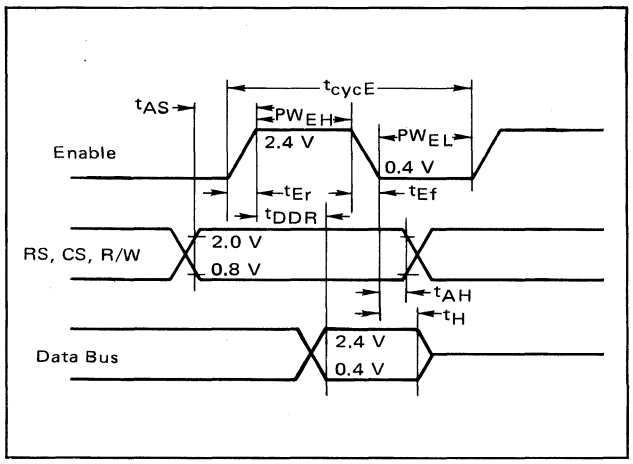


FIGURE 11 – BUS WRITE TIMING CHARACTERISTICS
(Write Information into PIA)

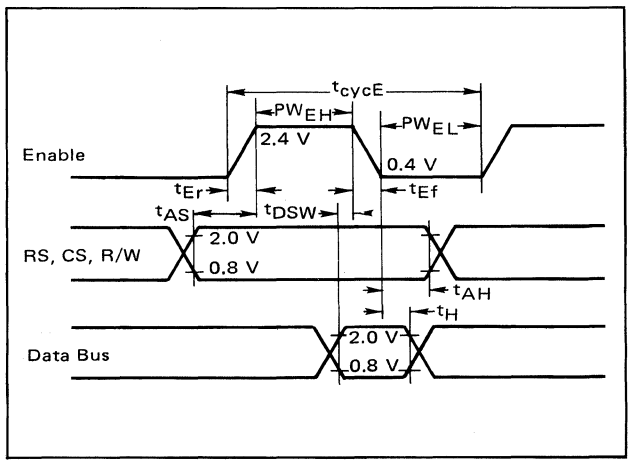
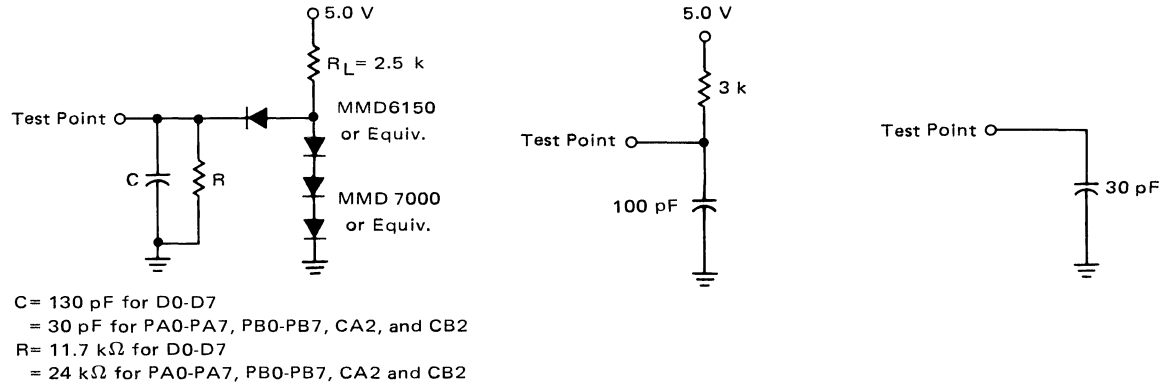


FIGURE 12 – BUS TIMING TEST LOADS



C= 130 pF for D0-D7
= 30 pF for PA0-PA7, PB0-PB7, CA2, and CB2
R= 11.7 kΩ for D0-D7
= 24 kΩ for PA0-PA7, PB0-PB7, CA2 and CB2

PIA INTERFACE SIGNALS FOR MPU

The PIA interfaces to the MC6800 MPU with an eight-bit bi-directional data bus, three chip select lines, two register select lines, two interrupt request lines, read/write line, enable line and reset line. These signals, in conjunction with the MC6800 VMA output, permit the MPU to have complete control over the PIA. VMA should be utilized in conjunction with an MPU address line into a chip select of the PIA.

PIA Bi-Directional Data (D0-D7) – The bi-directional data lines (D0-D7) allow the transfer of data between the MPU and the PIA. The data bus output drivers are three-state devices that remain in the high-impedance (off) state except when the MPU performs a PIA read operation. The Read/Write line is in the Read (high) state when the PIA is selected for a Read operation.

PIA Enable (E) – The enable pulse, E, is the only timing signal that is supplied to the PIA. Timing of all other signals is referenced to the leading and trailing edges of the E pulse. This signal will normally be a derivative of the MC6800 $\phi 2$ Clock.

PIA Read/Write (R/W) – This signal is generated by the MPU to control the direction of data transfers on the Data Bus. A low state on the PIA Read/Write line enables the input buffers and data is transferred from the MPU to the PIA on the E signal if the device has been selected. A high on the Read/Write line sets up the PIA for a transfer of data to the bus. The PIA output buffers are enabled when the proper address and the enable pulse E are present.

$\overline{\text{Reset}}$ – The active low $\overline{\text{Reset}}$ line is used to reset all register bits in the PIA to a logical zero (low). This line can be used as a power-on reset and as a master reset during system operation.

PIA Chip Select (CS0, CS1 and $\overline{\text{CS2}}$) – These three input signals are used to select the PIA. CS0 and CS1 must be high and $\overline{\text{CS2}}$ must be low for selection of the device. Data transfers are then performed under the control of the Enable and Read/Write signals. The chip select lines must be stable for the duration of the E pulse. The device is deselected when any of the chip selects are in the inactive state.

PIA Register Select (RS0 and RS1) – The two register select lines are used to select the various registers inside the PIA. These two lines are used in conjunction with internal Control Registers to select a particular register that is to be written or read.

The register and chip select lines should be stable for the duration of the E pulse while in the read or write cycle.

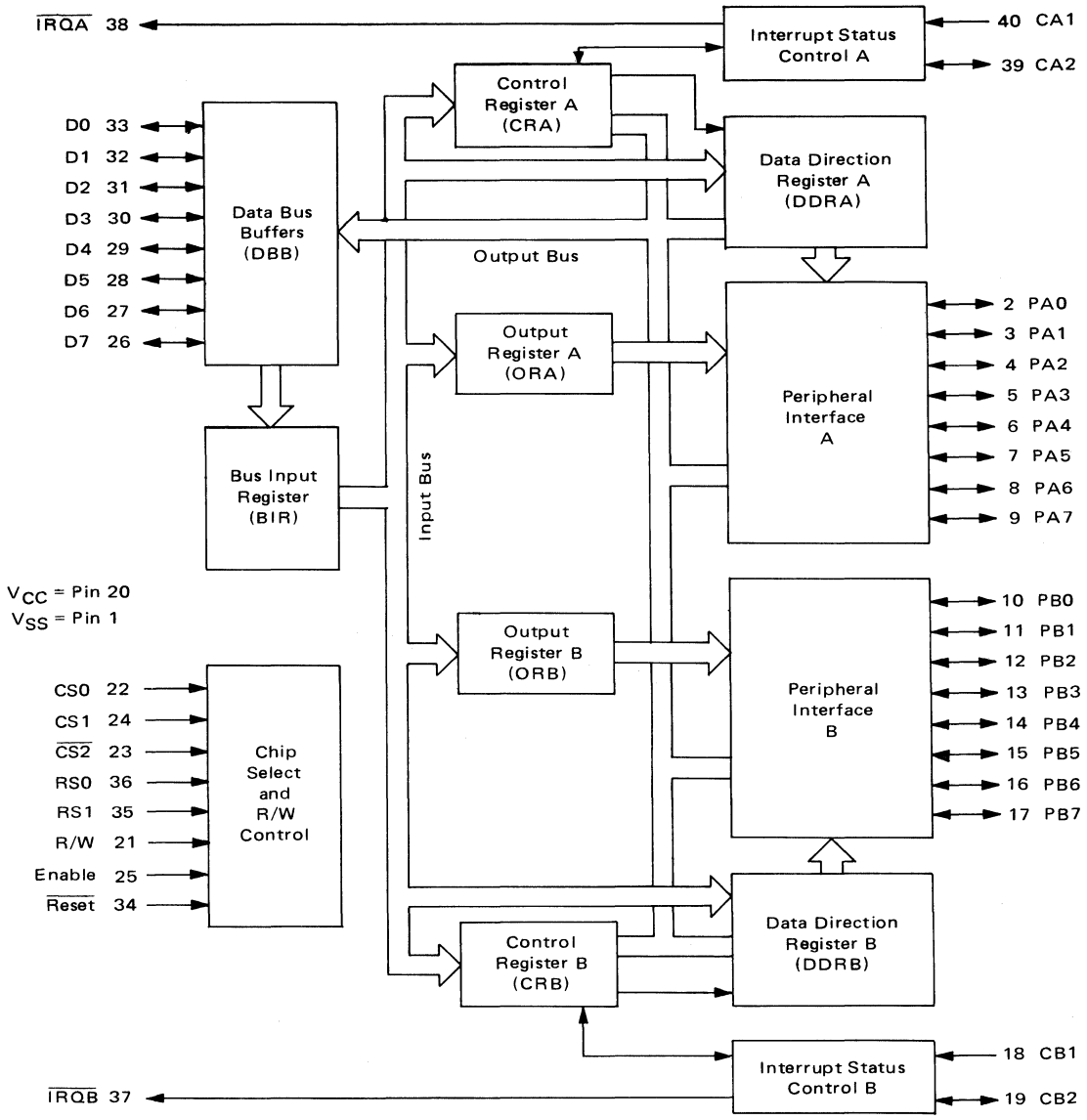
Interrupt Request ($\overline{\text{IRQA}}$ and $\overline{\text{IRQB}}$) – The active low Interrupt Request lines ($\overline{\text{IRQA}}$ and $\overline{\text{IRQB}}$) act to interrupt the MPU either directly or through interrupt priority circuitry. These lines are "open drain" (no load device on the chip). This permits all interrupt request lines to be tied together in a wire-OR configuration.

Each Interrupt Request line has two internal interrupt flag bits that can cause the Interrupt Request line to go low. Each flag bit is associated with a particular peripheral interrupt line. Also four interrupt enable bits are provided in the PIA which may be used to inhibit a particular interrupt from a peripheral device.

Servicing an interrupt by the MPU may be accomplished by a software routine that, on a prioritized basis, sequentially reads and tests the two control registers in each PIA for interrupt flag bits that are set.

The interrupt flags are cleared (zeroed) as a result of an

EXPANDED BLOCK DIAGRAM



MPU Read Peripheral Data Operation of the corresponding data register. After being cleared, the interrupt flag bit cannot be enabled to be set until the PIA is deselected during an E pulse. The E pulse is used to condition the interrupt control lines (CA1, CA2, CB1, CB2). When these lines are used as interrupt inputs at least one E pulse must occur from the inactive edge to the active edge of the interrupt input signal to condition the edge sense network. If the interrupt flag has been enabled and the edge sense circuit has been properly conditioned, the interrupt flag will be set on the next active transition of the interrupt input pin.

PIA PERIPHERAL INTERFACE LINES

The PIA provides two 8-bit bi-directional data buses and four interrupt/control lines for interfacing to peripheral devices.

Section A Peripheral Data (PA0-PA7) — Each of the peripheral data lines can be programmed to act as an input or output. This is accomplished by setting a "1" in the corresponding Data Direction Register bit for those lines which are to be outputs. A "0" in a bit of the Data Direction Register causes the corresponding peripheral data line to act as an input. During an MPU Read Peripheral Data Operation, the data on peripheral lines programmed to act as inputs appears directly on the corresponding MPU Data Bus lines. In the input mode the internal pullup resistor on these lines represents a maximum of one standard TTL load.

The data in Output Register A will appear on the data lines that are programmed to be outputs. A logical "1" written into the register will cause a "high" on the corresponding data line while a "0" results in a "low". Data in Output Register A may be read by an MPU "Read Peripheral Data A" operation when the corresponding lines are programmed as outputs. This data will be read properly if the voltage on the peripheral data lines is greater than 2.0 volts for a logic "1" output and less than 0.8 volt for a logic "0" output. Loading the output lines such that the voltage on these lines does not reach full voltage causes the data transferred into the MPU on a Read operation to differ from that contained in the respective bit of Output Register A.

Section B Peripheral Data (PB0-PB7) — The peripheral data lines in the B Section of the PIA can be programmed to act as either inputs or outputs in a similar manner to PA0-PA7. However, the output buffers driving these lines differ from those driving lines PA0-PA7. They have three-state capability, allowing them to enter a high impedance state when the peripheral data line is used as an input. In addition, data on the peripheral data lines PB0-PB7 will be read properly from those lines programmed as outputs even if the voltages are below 2.0 volts for a "high". As outputs, these lines are compatible with standard TTL and may also be used as a source of up to 1 milliampere at 1.5 volts to directly drive the base of a transistor switch.

Interrupt Input (CA1 and CB1) — Peripheral Input lines CA1 and CB1 are input only lines that set the interrupt flags of the control registers. The active transition for these signals is also programmed by the two control registers.

Peripheral Control (CA2) — The peripheral control line CA2 can be programmed to act as an interrupt input or as a peripheral control output. As an output, this line is compatible with standard TTL; as an input the internal pullup resistor on this line represents one standard TTL load. The function of this signal line is programmed with Control Register A.

Peripheral Control (CB2) — Peripheral Control line CB2 may also be programmed to act as an interrupt input or peripheral control output. As an input, this line has high input impedance and is compatible with standard TTL. As an output it is compatible with standard TTL and may also be used as a source of up to 1 milliampere at 1.5 volts to directly drive the base of a transistor switch. This line is programmed by Control Register B.

NOTE: It is recommended that the control lines (CA1, CA2, CB1, CB2) should be held in a logic 1 state when $\overline{\text{Reset}}$ is active to prevent setting of corresponding interrupt flags in the control register when $\overline{\text{Reset}}$ goes to an inactive state. Subsequent to $\overline{\text{Reset}}$ going inactive, a read of the data registers may be used to clear any undesired interrupt flags.

INTERNAL CONTROLS

There are six locations within the PIA accessible to the MPU data bus: two Peripheral Registers, two Data Direction Registers, and two Control Registers. Selection of these locations is controlled by the RS0 and RS1 inputs together with bit 2 in the Control Register, as shown in Table 1.

TABLE 1 – INTERNAL ADDRESSING

RS1	RS0	Control Register Bit CRA-2	Control Register Bit CRB-2	Location Selected
0	0	1	X	Peripheral Register A
0	0	0	X	Data Direction Register A
0	1	X	X	Control Register A
1	0	X	1	Peripheral Register B
1	0	X	0	Data Direction Register B
1	1	X	X	Control Register B

X = Don't Care

INITIALIZATION

A low reset line has the effect of zeroing all PIA registers. This will set PA0-PA7, PB0-PB7, CA2 and CB2 as inputs, and all interrupts disabled. The PIA must be configured during the restart program which follows the reset.

Details of possible configurations of the Data Direction and Control Register are as follows.

DATA DIRECTION REGISTERS (DDRA and DDRB)

The two Data Direction Registers allow the MPU to control the direction of data through each corresponding peripheral data line. A Data Direction Register bit set at "0" configures the corresponding peripheral data line as an input; a "1" results in an output.

CONTROL REGISTERS (CRA and CRB)

The two Control Registers (CRA and CRB) allow the MPU to control the operation of the four peripheral control lines CA1, CA2, CB1 and CB2. In addition they allow the MPU to enable the interrupt lines and monitor the status of the interrupt flags. Bits 0 through 5 of the two registers may be written or read by the MPU when the proper chip select and register select signals are applied. Bits 6 and 7 of the two registers are read only and are modified by external interrupts occurring on control lines CA1, CA2, CB1 or CB2. The format of the control words is shown in Table 2.

TABLE 2 – CONTROL WORD FORMAT

	7	6	5	4	3	2	1	0
CRA	IRQA1	IRQA2	CA2 Control			DDRA Access	CA1 Control	
CRB	IRQB1	IRQB2	CB2 Control			DDRB Access	CB1 Control	

Data Direction Access Control Bit (CRA-2 and CRB-2) – Bit 2 in each Control register (CRA and CRB) allows selection of either a Peripheral Interface Register or the Data Direction Register when the proper register select signals are applied to RS0 and RS1.

Interrupt Flags (CRA-6, CRA-7, CRB-6, and CRB-7) – The four interrupt flag bits are set by active transitions of signals on the four Interrupt and Peripheral Control lines when those lines are programmed to be inputs. These bits cannot be set directly from the MPU Data Bus and are reset indirectly by a Read Peripheral Data Operation on the appropriate section.

TABLE 3 – CONTROL OF INTERRUPT INPUTS CA1 AND CB1

CRA-1 (CRB-1)	CRA-0 (CRB-0)	Interrupt Input CA1 (CB1)	Interrupt Flag CRA-7 (CRB-7)	MPU Interrupt Request $\overline{IRQA}$ ($\overline{IRQB}$)
0	0	↓ Active	Set high on ↓ of CA1 (CB1)	Disabled — $\overline{IRQ}$ remains high
0	1	↓ Active	Set high on ↓ of CA1 (CB1)	Goes low when the interrupt flag bit CRA-7 (CRB-7) goes high
1	0	↑ Active	Set high on ↑ of CA1 (CB1)	Disabled — $\overline{IRQ}$ remains high
1	1	↑ Active	Set high on ↑ of CA1 (CB1)	Goes low when the interrupt flag bit CRA-7 (CRB-7) goes high

Notes:
1. ↑ indicates positive transition (low to high)
2. ↓ indicates negative transition (high to low)
3. The Interrupt flag bit CRA-7 is cleared by an MPU Read of the A Data Register, and CRB-7 is cleared by an MPU Read of the B Data Register.
4. If CRA-0 (CRB-0) is low when an interrupt occurs (Interrupt disabled) and is later brought high, $\overline{IRQA}$ ($\overline{IRQB}$) occurs after CRA-0 (CRB-0) is written to a "one".

Control of CA1 and CB1 Interrupt Input Lines (CRA-0, CRB-0, CRA-1, and CRB-1) — The two lowest order bits of the control registers are used to control the interrupt input lines CA1 and CB1. Bits CRA-0 and CRB-0 are used to enable the MPU interrupt signals $\overline{IRQA}$ and $\overline{IRQB}$, respectively. Bits CRA-1 and CRB-1 determine the active transition of the interrupt input signals CA1 and CB1 (Table 3).

TABLE 4 – CONTROL OF CA2 AND CB2 AS INTERRUPT INPUTS
CRA5 (CRB5) is low

CRA-5 (CRB-5)	CRA-4 (CRB-4)	CRA-3 (CRB-3)	Interrupt Input CA2 (CB2)	Interrupt Flag CRA-6 (CRB-6)	MPU Interrupt Request $\overline{IRQA}$ ($\overline{IRQB}$)
0	0	0	↓ Active	Set high on ↓ of CA2 (CB2)	Disabled — $\overline{IRQ}$ remains high
0	0	1	↓ Active	Set high on ↓ of CA2 (CB2)	Goes low when the interrupt flag bit CRA-6 (CRB-6) goes high
0	1	0	↑ Active	Set high on ↑ of CA2 (CB2)	Disabled — $\overline{IRQ}$ remains high
0	1	1	↑ Active	Set high on ↑ of CA2 (CB2)	Goes low when the interrupt flag bit CRA-6 (CRB-6) goes high

Notes: 1. ↑ indicates positive transition (low to high)
2. ↓ indicates negative transition (high to low)
3. The Interrupt flag bit CRA-6 is cleared by an MPU Read of the A Data Register and CRB-6 is cleared by an MPU Read of the B Data Register.
4. If CRA-3 (CRB-3) is low when an interrupt occurs (Interrupt disabled) and is later brought high, $\overline{IRQA}$ ($\overline{IRQB}$) occurs after CRA-3 (CRB-3) is written to a "one".

TABLE 5 – CONTROL OF CB2 AS AN OUTPUT
CRB-5 is high

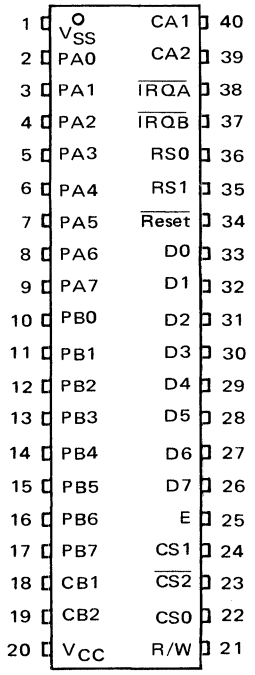
CRB-5	CRB-4	CRB-3	CB2 Cleared	CB2 Set
1	0	0	Low on the positive transition of the first E pulse following an MPU Write "B" Data Register operation.	High when the interrupt flag bit CRB-7 is set by an active transition of the CB1 signal.
1	0	1	Low on the positive transition of the first E pulse after an MPU Write "B" Data Register operation.	High on the positive edge of the first "E" pulse following an "E" pulse which occurred while the part was deselected.
1	1	0	Low when CRB-3 goes low as a result of an MPU Write in Control Register "B".	Always low as long as CRB-3 is low. Will go high on an MPU Write in Control Register "B" that changes CRB-3 to "one".
1	1	1	Always high as long as CRB-3 is high. Will be cleared when an MPU Write Control Register "B" results in clearing CRB-3 to "zero".	High when CRB-3 goes high as a result of an MPU Write into Control Register "B".

Control of CA2 and CB2 Peripheral Control Lines (CRA-3, CRA-4, CRA-5, CRB-3, CRB-4, and CRB-5) – Bits 3, 4, and 5 of the two control registers are used to control the CA2 and CB2 Peripheral Control lines. These bits determine if the control lines will be an interrupt input or an output control signal. If bit CRA-5 (CRB-5) is low, CA2 (CB2) is an interrupt input line similar to CA1 (CB1) (Table 4). When CRA-5 (CRB-5) is high, CA2 (CB2) becomes an output signal that may be used to control peripheral data transfers. When in the output mode, CA2 and CB2 have slightly different characteristics (Tables 5 and 6).

TABLE 6 – CONTROL OF CA-2 AS AN OUTPUT
CRA-5 is high

CRA-5	CRA-4	CRA-3	CA2 Cleared	CA2 Set
1	0	0	Low on negative transition of E after an MPU Read "A" Data operation.	High when the interrupt flag bit CRA-7 is set by an active transition of the CA1 signal.
1	0	1	Low on negative transition of E after an MPU Read "A" Data operation.	High on the negative edge of the first "E" pulse which occurs during a deselect.
1	1	0	Low when CRA-3 goes low as a result of an MPU Write to Control Register "A".	Always low as long as CRA-3 is low. Will go high on an MPU Write to Control Register "A" that changes CRA-3 to "one".
1	1	1	Always high as long as CRA-3 is high. Will be cleared on an MPU Write to Control Register "A" that clears CRA-3 to a "zero".	High when CRA-3 goes high as a result of an MPU Write to Control Register "A".

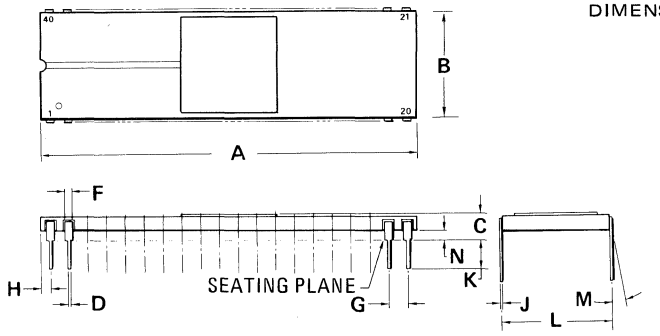
PIN ASSIGNMENT



PACKAGE DIMENSIONS

CASE 715-02
(CERAMIC)

SEE PAGE 165 FOR PLASTIC PACKAGE DIMENSIONS.



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	50.29	51.31	1.980	2.020
B	14.86	15.62	0.585	0.615
C	2.54	4.19	0.100	0.165
D	0.38	0.53	0.015	0.021
F	0.76	1.40	0.030	0.055
G	2.54 BSC		0.100 BSC	
H	0.76	1.78	0.030	0.070
J	0.20	0.33	0.008	0.013
K	2.54	4.19	0.100	0.165
L	14.60	15.37	0.575	0.605
M	–	10^0	–	10^0
N	0.51	1.52	0.020	0.060

NOTE:
1. LEADS, TRUE POSITIONED WITHIN 0.25 mm (0.010) DIA (AT SEATING PLANE), AT MAX. MAT'L CONDITION.

MOTOROLA Semiconductors
BOX 20912 • PHOENIX, ARIZONA 85036

MC6850

(0 to 70°C; L or P Suffix)

MC6850C

(-40 to 85°C; L Suffix only)

ASYNCHRONOUS COMMUNICATIONS INTERFACE ADAPTER (ACIA)

The MC6850 Asynchronous Communications Interface Adapter provides the data formatting and control to interface serial asynchronous data communications information to bus organized systems such as the MC6800 Microprocessing Unit.

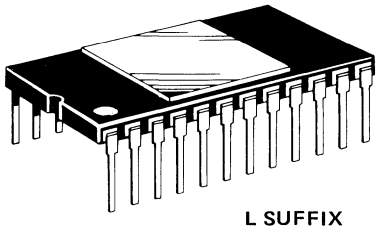
The bus interface of the MC6850 includes select, enable, read/write, interrupt and bus interface logic to allow data transfer over an 8-bit bi-directional data bus. The parallel data of the bus system is serially transmitted and received by the asynchronous data interface, with proper formatting and error checking. The functional configuration of the ACIA is programmed via the data bus during system initialization. A programmable Control Register provides variable word lengths, clock division ratios, transmit control, receive control, and interrupt control. For peripheral or modem operation three control lines are provided. These lines allow the ACIA to interface directly with the MC6860L 0-600 bps digital modem.

- Eight and Nine-Bit Transmission
- Optional Even and Odd Parity
- Parity, Overrun and Framing Error Checking
- Programmable Control Register
- Optional ÷1, ÷16, and ÷64 Clock Modes
- Up to 500 kbps Transmission
- False Start Bit Deletion
- Peripheral/Modem Control Functions
- Double Buffered
- One or Two Stop Bit Operation

MOS

(N-CHANNEL, SILICON-GATE)

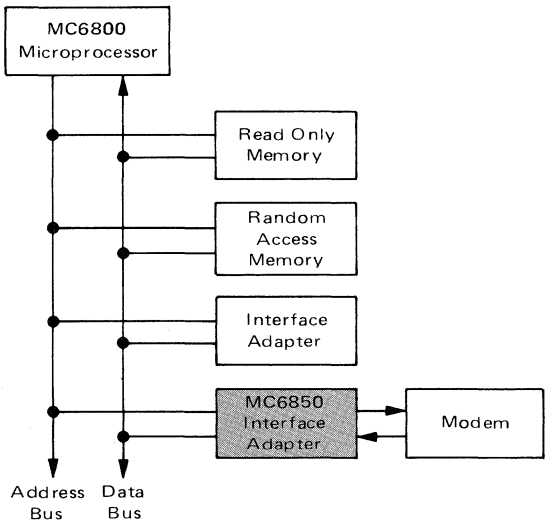
ASYNCHRONOUS COMMUNICATIONS INTERFACE ADAPTER



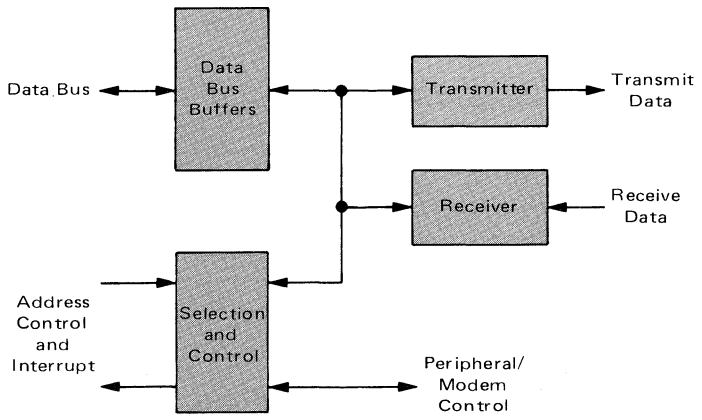
L SUFFIX
CERAMIC PACKAGE
CASE 716

NOT SHOWN: **P SUFFIX**
PLASTIC PACKAGE
CASE 709

M6800 MICROCOMPUTER FAMILY BLOCK DIAGRAM



MC6850 ASYNCHRONOUS COMMUNICATIONS INTERFACE ADAPTER BLOCK DIAGRAM



MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	-0.3 to +7.0	Vdc
Input Voltage	V_{in}	-0.3 to +7.0	Vdc
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	-55 to +150	°C
Thermal Resistance	θ_{JA}	82.5	°C/W

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V ±5%, V_{SS} = 0, T_A = 0 to 70°C unless otherwise noted.)

Characteristic		Symbol	Min	Typ	Max	Unit
Input High Voltage		V_{IH}	V_{SS} + 2.0	–	V_{CC}	Vdc
Input Low Voltage		V_{IL}	V_{SS} -0.3	–	V_{SS} + 0.8	Vdc
Input Leakage Current (V_{in} = 0 to 5.25 Vdc)	R/W,CS0,CS1,$\overline{CS2}$,Enable	I_{in}	–	1.0	2.5	μAdc
Three-State (Off State) Input Current (V_{in} = 0.4 to 2.4 Vdc)	D0-D7	I_{TSI}	–	2.0	10	μAdc
Output High Voltage	D0-D7	V_{OH}				Vdc
(I_{Load} = -205 μAdc, Enable Pulse Width <25 μs)			V_{SS} + 2.4	–	–	
(I_{Load} = -100 μAdc, Enable Pulse Width <25 μs)	Tx Data, $\overline{RTS}$		V_{SS} + 2.4	–	–	
Output Low Voltage (I_{Load} = 1.6 mAdc, Enable Pulse Width <25 μs)		V_{OL}	–	–	V_{SS} + 0.4	Vdc
Output Leakage Current (Off State) (V_{OH} = 2.4 Vdc)	$\overline{IRQ}$	I_{LOH}	–	1.0	10	μAdc
Power Dissipation		P_D	–	300	525	mW
Input Capacitance		C_{in}				pF
(V_{in} = 0, T_A = 25°C, f = 1.0 MHz)	D0-D7		–	10	12.5	
E, Tx Clk, Rx Clk, R/W, RS, Rx Data, CS0, CS1, $\overline{CS2}$, $\overline{CTS}$, $\overline{DCD}$			–	7.0	7.5	
Output Capacitance	$\overline{RTS}$, Tx Data	C_{out}	–	–	10	pF
(V_{in} = 0, T_A = 25°C, f = 1.0 MHz)	$\overline{IRQ}$		–	–	5.0	
Minimum Clock Pulse Width, Low (Figure 1)	÷16, ÷64 Modes	PW_{CL}	600	–	–	ns
Minimum Clock Pulse Width, High (Figure 2)	÷16, ÷64 Modes	PW_{CH}	600	–	–	ns
Clock Frequency	÷1 Mode	f_C	–	–	500	kHz
	÷16, ÷64 Modes		–	–	800	
Clock-to-Data Delay for Transmitter (Figure 3)		t_{TDD}	–	–	1.0	μs
Receive Data Setup Time (Figure 4)	÷1 Mode	t_{RDSU}	500	–	–	ns
Receive Data Hold Time (Figure 5)	÷1 Mode	t_{RDH}	500	–	–	ns
$\overline{Interrupt\ Request}$ Release Time (Figure 6)		t_{IR}	–	–	1.2	μs
$\overline{Request\text{-}to\text{-}Send}$ Delay Time (Figure 6)		t_{RTS}	–	–	1.0	μs
Input Transition Times (Except Enable)		t_r,t_f	–	–	1.0*	μs

*1.0 μs or 10% of the pulse width, whichever is smaller.

BUS TIMING CHARACTERISTICS

READ (Figures 7 and 9)

Characteristic	Symbol	Min	Typ	Max	Unit
Enable Cycle Time	t_{cycE}	1.0	–	–	μs
Enable Pulse Width, High	PW_{EH}	0.45	–	25	μs
Enable Pulse Width, Low	PW_{EL}	0.43	–	–	μs
Setup Time, Address and R/W valid to Enable positive transition	t_{AS}	160	–	–	ns
Data Delay Time	t_{DDR}	–	–	320	ns
Data Hold Time	t_H	10	–	–	ns
Address Hold Time	t_{AH}	10	–	–	ns
Rise and Fall Time for Enable input	t_{Er}, t_{Ef}	–	–	25	ns

WRITE (Figure 8 and 9)

Enable Cycle Time	t_{cycE}	1.0	–	–	μs
Enable Pulse Width, High	PW_{EH}	0.45	–	25	μs
Enable Pulse Width, Low	PW_{EL}	0.43	–	–	μs
Setup Time, Address and R/W valid to Enable positive transition	t_{AS}	160	–	–	ns
Data Setup Time	t_{DSW}	195	–	–	ns
Data Hold Time	t_H	10	–	–	ns
Address Hold Time	t_{AH}	10	–	–	ns
Rise and Fall Time for Enable input	t_{Er}, t_{Ef}	–	–	25	ns

FIGURE 1 – CLOCK PULSE WIDTH, LOW-STATE

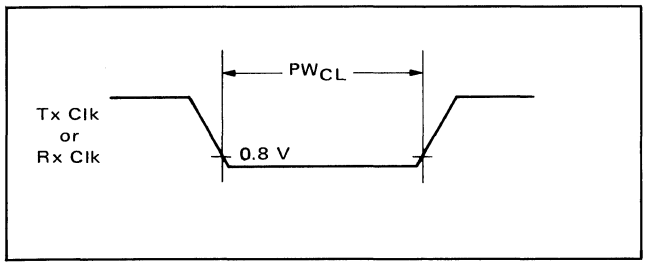


FIGURE 2 – CLOCK PULSE WIDTH, HIGH-STATE

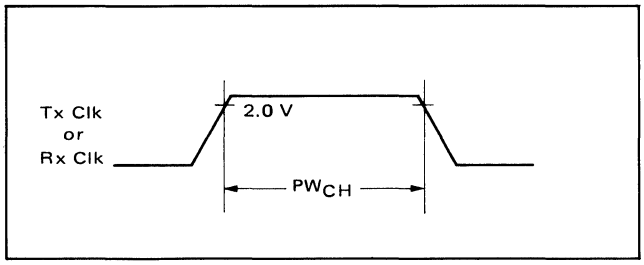


FIGURE 3 – TRANSMIT DATA OUTPUT DELAY

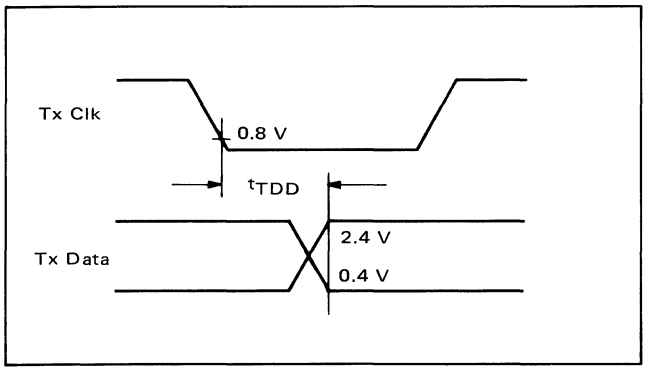


FIGURE 4 – RECEIVE DATA SETUP TIME
(÷1 Mode)

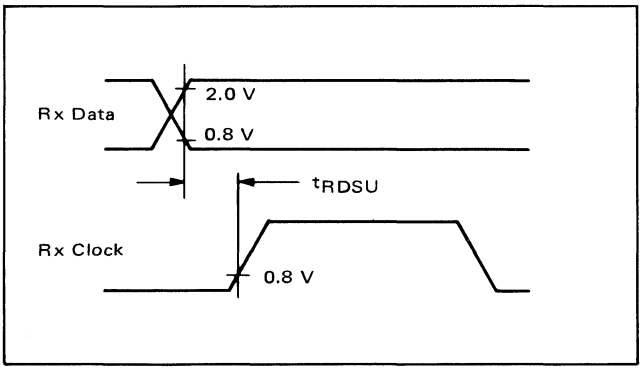


FIGURE 5 – RECEIVE DATA HOLD TIME
(÷1 Mode)

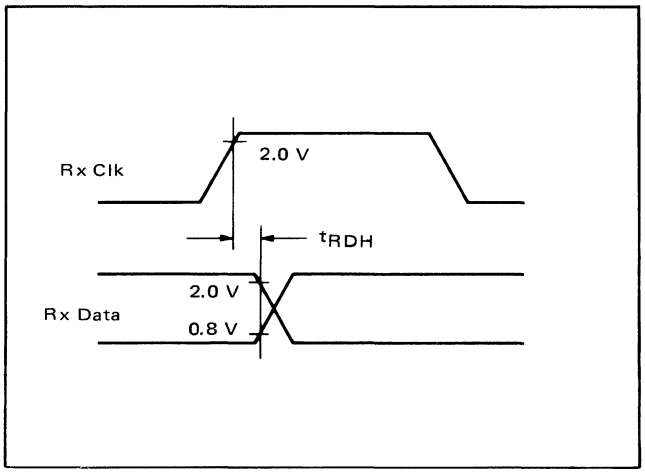


FIGURE 6 – $\overline{\text{REQUEST-TO-SEND}}$ DELAY AND $\overline{\text{INTERRUPT-REQUEST}}$ RELEASE TIMES

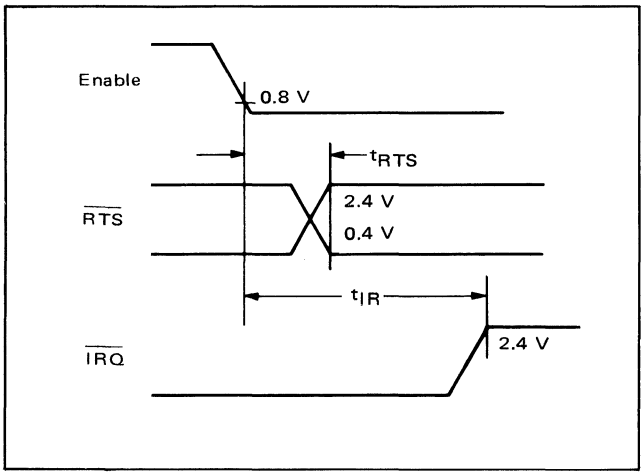


FIGURE 7 – BUS READ TIMING CHARACTERISTICS
(Read information from ACIA)

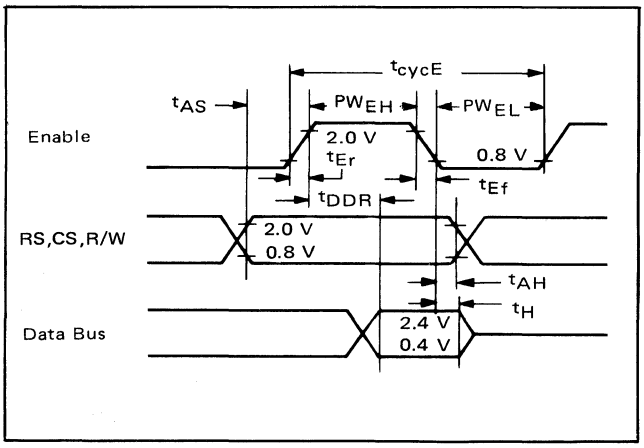


FIGURE 8 – BUS WRITE TIMING CHARACTERISTICS
(Write information into ACIA)

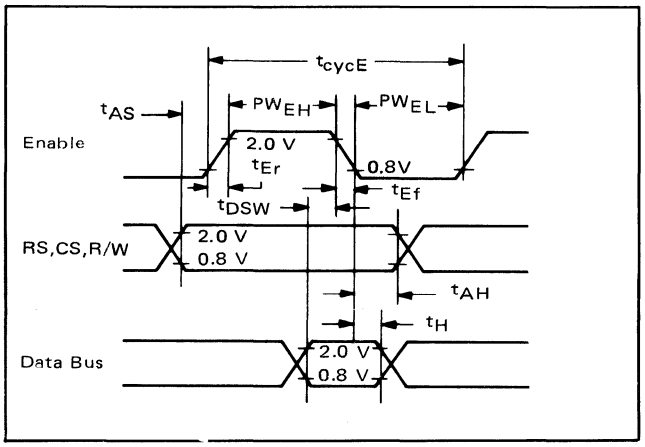
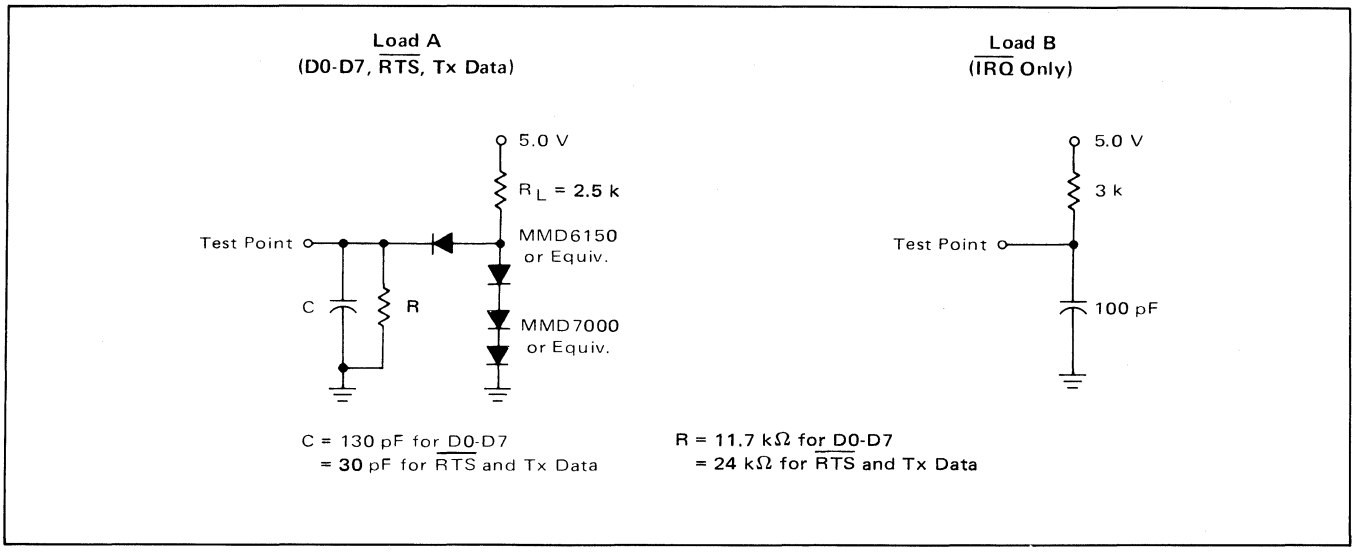
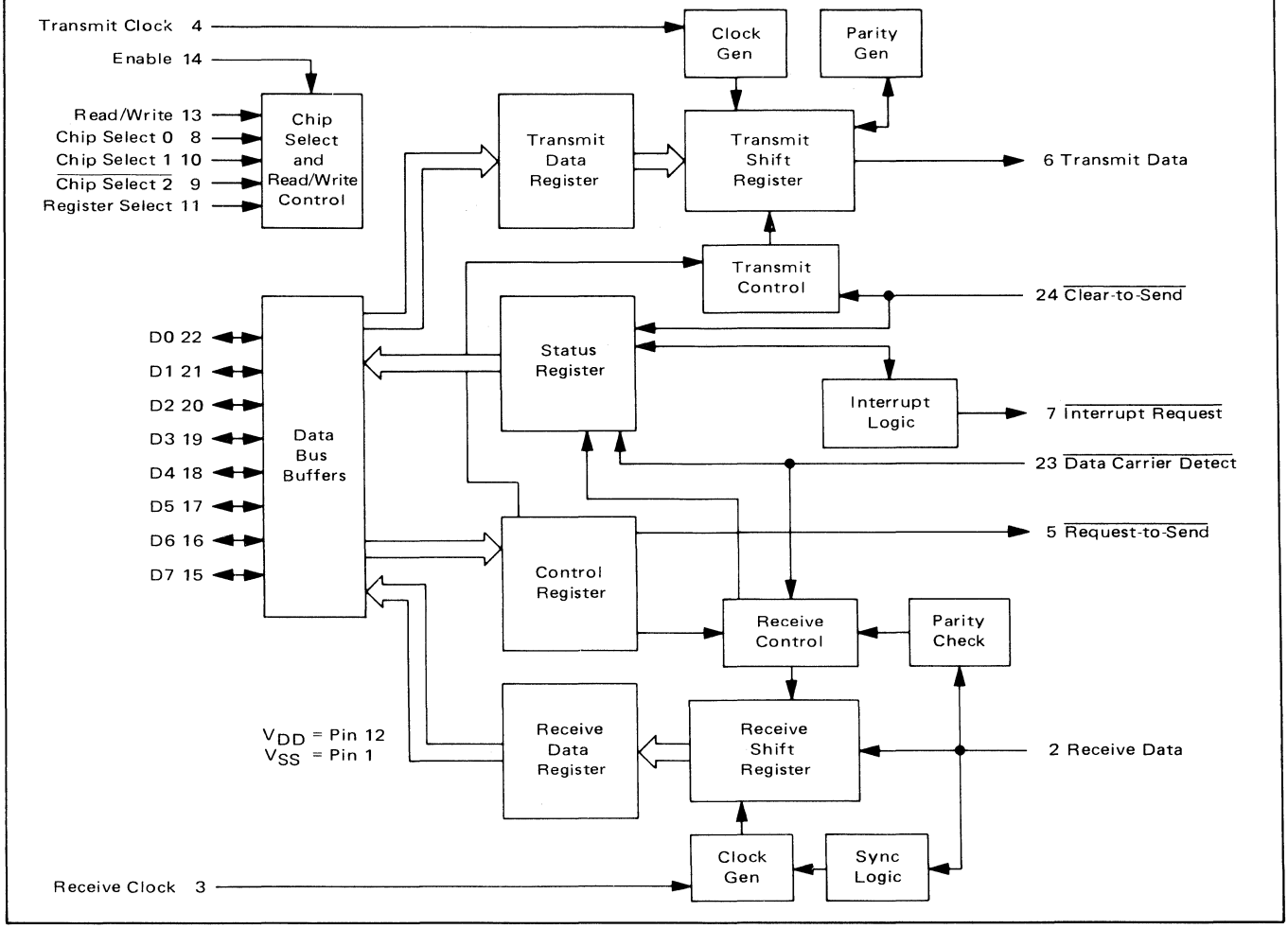


FIGURE 9 – BUS TIMING TEST LOADS



EXPANDED BLOCK DIAGRAM



DEVICE OPERATION

At the bus interface, the ACIA appears as two addressable memory locations. Internally, there are four registers: two read-only and two write-only registers. The read-only registers are Status and Receive Data; the write-only registers are Control and Transmit Data. The serial interface consists of serial input and output lines with independent clocks, and three peripheral/modem control lines.

POWER ON/MASTER RESET

The master reset (CR0, CR1) should be set during system initialization to insure the reset condition and prepare for programming the ACIA functional configuration when the communications channel is required. Control bits CR5 and CR6 should also be programmed to define the state of $\overline{RTS}$ whenever master reset is utilized. The ACIA also contains internal power-on reset logic to detect the power line turn-on transition and hold the chip in a reset state to prevent erroneous output transitions prior to initialization. This circuitry depends on clean power turn-on transitions. The power-on reset is released by means of the bus-programmed master reset which must be applied prior to operating the ACIA. After master resetting the ACIA, the programmable Control Register can be set for a number of options such as variable clock divider ratios, variable word length, one or two stop bits, parity (even, odd, or none), etc.

TRANSMIT

A typical transmitting sequence consists of reading the ACIA Status Register either as a result of an interrupt or in the ACIA's turn in a polling sequence. A character may be written into the Transmit Data Register if the status read operation has indicated that the Transmit Data Register is empty. This character is transferred to a Shift Register where it is serialized and transmitted from the Transmit Data output preceded by a start bit and followed by one or two stop bits. Internal parity (odd or even) can be optionally added to the character and will occur between the last data bit and the first stop bit. After the first character is written in the Data Register, the Status Register can be read again to check for a Transmit Data Register Empty condition and current peripheral status. If the register is empty, another character can be loaded for transmission even though the first character is in the process of being transmitted (because of double buffering). The second character will be automatically transferred into the Shift Register when the first character transmission is completed. This sequence continues until all the characters have been transmitted.

RECEIVE

Data is received from a peripheral by means of the Receive Data input. A divide-by-one clock ratio is provided for an externally synchronized clock (to its data) while the divide-by-16 and 64 ratios are provided for internal synchronization. Bit synchronization in the divide-by-16 and 64 modes is initiated by the detection of the leading mark-to-space transition of the start bit. False start bit deletion capability insures that a full half bit of a start bit has been received before the internal clock is synchronized to the bit time. As a character is being received, parity (odd or even) will be checked and the error indication will be available in the Status Register along with framing error, overrun error, and Receive Data Register full. In a typical receiving sequence, the Status Register is read to determine if a character has been received from a peripheral. If the Receiver Data Register is full, the character is placed on the 8-bit ACIA bus when a Read Data command is received from the MPU. When parity has been selected for an 8-bit word (7 bits plus parity), the receiver strips the parity bit (D7 = 0) so that data alone is transferred to the MPU. This feature reduces MPU programming. The Status Register can continue to be read again to determine when another character is available in the Receive Data Register. The receiver is also double buffered so that a character can be read from the data register as another character is being received in the shift register. The above sequence continues until all characters have been received.

INPUT/OUTPUT FUNCTIONS

ACIA INTERFACE SIGNALS FOR MPU

The ACIA interfaces to the MC6800 MPU with an 8-bit bi-directional data bus, three chip select lines, a register select line, an interrupt request line, read/write line, and enable line. These signals, in conjunction with the MC6800 VMA output, permit the MPU to have complete control over the ACIA.

ACIA Bi-Directional Data (D0-D7) — The bi-directional data lines (D0-D7) allow for data transfer between the ACIA and the MPU. The data bus output drivers are three-state devices that remain in the high-impedance (off) state except when the MPU performs an ACIA read operation.

ACIA Enable (E) — The Enable signal, E, is a high impedance TTL compatible input that enables the bus input/output data buffers and clocks data to and from the ACIA. This signal will normally be a derivative of the MC6800 $\phi 2$ Clock.

Read/Write (R/W) — The Read/Write line is a high impedance input that is TTL compatible and is used to control the direction of data flow through the ACIA's input/output data bus interface. When Read/Write is high (MPU Read cycle), ACIA output drivers are turned on and a selected register is read. When it is low, the ACIA output drivers are turned off and the MPU writes into a selected register. Therefore, the Read/Write signal is used to select read-only or write-only registers within the ACIA.

Chip Select (CS0, CS1, $\overline{CS2}$) — These three high impedance TTL compatible input lines are used to address the ACIA. The ACIA is selected when CS0 and CS1 are high and $\overline{CS2}$ is low. Transfers of data to and from the ACIA are then performed under the control of the Enable signal, Read/Write, and Register Select.

Register Select (RS) — The Register Select line is a high impedance input that is TTL compatible. A high level is used to select the Transmit/Receive Data Registers and a low level the Control/Status Registers. The Read/Write signal line is used in conjunction with Register Select to select the read-only or write-only register in each register pair.

$\overline{\text{Interrupt Request}}$ ($\overline{IRQ}$) — $\overline{\text{Interrupt Request}}$ is a TTL compatible, open-drain (no internal pullup), active low

output that is used to interrupt the MPU. The $\overline{IRQ}$ output remains low as long as the cause of the interrupt is present and the appropriate interrupt enable within the ACIA is set. The IRQ status bit, when high, indicates the $\overline{IRQ}$ output is in the active state.

Interrupts result from conditions in both the transmitter and receiver sections of the ACIA. The transmitter section causes an interrupt when the Transmitter Interrupt Enabled condition is selected (CR5 · $\overline{CR6}$), and the Transmit Data Register Empty (TDRE) status bit is high. The TDRE status bit indicates the current status of the Transmitter Data Register except when inhibited by Clear-to-Send ($\overline{CTS}$) being high or the ACIA being maintained in the Reset condition. The interrupt is cleared by writing data into the Transmit Data Register. The interrupt is masked by disabling the Transmitter Interrupt via CR5 or CR6 or by the loss of $\overline{CTS}$ which inhibits the TDRE status bit. The Receiver section causes an interrupt when the Receiver Interrupt Enable is set and the Receive Data Register Full (RDRF) status bit is high, an Overrun has occurred, or Data Carrier Detect ($\overline{DCD}$) has gone high. An interrupt resulting from the RDRF status bit can be cleared by reading data or resetting the ACIA. Interrupts caused by Overrun or loss of $\overline{DCD}$ are cleared by reading the status register after the error condition has occurred and then reading the Receive Data Register or resetting the ACIA. The receiver interrupt is masked by resetting the Receiver Interrupt Enable.

CLOCK INPUTS

Separate high impedance TTL compatible inputs are provided for clocking of transmitted and received data. Clock frequencies of 1, 16 or 64 times the data rate may be selected.

Transmit Clock (Tx Clk) – The Transmit Clock input is used for the clocking of transmitted data. The transmitter initiates data on the negative transition of the clock.

Receive Clock (Rx Clk) – The Receive Clock input is used for synchronization of received data. (In the ÷ 1 mode, the clock and data must be synchronized externally.) The receiver samples the data on the positive transiton of the clock.

SERIAL INPUT/OUTPUT LINES

Receive Data (Rx Data) – The Receive Data line is a high impedance TTL compatible input through which data is received in a serial format. Synchronization with a clock for detection of data is accomplished internally when clock rates of 16 or 64 times the bit rate are used. Data rates are in the range of 0 to 500 kbps when external synchronization is utilized.

Transmit Data (Tx Data) – The Transmit Data output line transfers serial data to a modem or other peripheral. Data rates are in the range of 0 to 500 kbps when external synchronization is utilized.

PERIPHERAL/MODEM CONTROL

The ACIA includes several functions that permit limited control of a peripheral or modem. The functions included are Clear-to-Send, Request-to-Send and Data Carrier Detect.

Clear-to-Send ($\overline{CTS}$) – This high impedance TTL compatible input provides automatic control of the transmitting end of a communications link via the modem Clear-to-Send active low output by inhibiting the Transmit Data Register Empty (TDRE) status bit.

Request-to-Send ($\overline{RTS}$) – The Request-to-Send output enables the MPU to control a peripheral or modem via the data bus. The $\overline{RTS}$ output corresponds to the state of the Control Register bits CR5 and CR6. When CR6 = 0 or both CR5 and CR6 = 1, the $\overline{RTS}$ output is low (the active state). This output can also be used for Data Terminal Ready ($\overline{DTR}$).

Data Carrier Detect ($\overline{DCD}$) – This high impedance TTL compatible input provides automatic control, such as in the receiving end of a communications link by means of a modem Data Carrier Detect output. The $\overline{DCD}$ input inhibits and initializes the receiver section of the ACIA when high. A low to high transition of the Data Carrier Detect initiates an interrupt to the MPU to indicate the occurrence of a loss of carrier when the Receive Interrupt Enable bit is set.

ACIA REGISTERS

The expanded block diagram for the ACIA indicates the internal registers on the chip that are used for the status, control, receiving, and transmitting of data. The content of each of the registers is summarized in Table 1.

TRANSMIT DATA REGISTER (TDR)

Data is written in the Transmit Data Register during the negative transition of the enable (E) when the ACIA has been addressed and RS · $\overline{R/W}$ is selected. Writing data into the register causes the Transmit Data Register Empty bit in the Status Register to go low. Data can then be transmitted. If the transmitter is idling and no character is being transmitted, then the transfer will take place within one bit time of the trailing edge of the Write command. If a character is being transmitted, the new data character will commence as soon as the previous character is complete. The transfer of data causes the Transmit Data Register Empty (TDRE) bit to indicate empty.

RECEIVE DATA REGISTER (RDR)

Data is automatically transferred to the empty Receive Data Register (RDR) from the receiver deserializer (a shift register) upon receiving a complete character. This event causes the Receive Data Register Full bit (RDRF) in the status buffer to go high (full). Data may then be read through the bus by addressing the ACIA and selecting the Receive Data Register with RS and R/W high when the ACIA is enabled. The non-destructive read cycle causes the RDRF bit to be cleared to empty although

TABLE 1 – DEFINITION OF ACIA REGISTER CONTENTS

Data Bus Line Number	Buffer Address			
	RS • R/W Transmit Data Register (Write Only)	RS • R/W Receive Data Register (Read Only)	RS • R/W Control Register (Write Only)	RS • R/W Status Register (Read Only)
0	Data Bit 0*	Data Bit 0	Counter Divide Select 1 (CR0)	Receive Data Register Full (RDRF)
1	Data Bit 1	Data Bit 1	Counter Divide Select 2 (CR1)	Transmit Data Register Empty (TDRE)
2	Data Bit 2	Data Bit 2	Word Select 1 (CR2)	Data Carrier Detect (DCD)
3	Data Bit 3	Data Bit 3	Word Select 2 (CR3)	Clear-to-Send (CTS)
4	Data Bit 4	Data Bit 4	Word Select 3 (CR4)	Framing Error (FE)
5	Data Bit 5	Data Bit 5	Transmit Control 1 (CR5)	Receiver Overrun (OVRN)
6	Data Bit 6	Data Bit 6	Transmit Control 2 (CR6)	Parity Error (PE)
7	Data Bit 7***	Data Bit 7**	Receive Interrupt Enable (CR7)	Interrupt Request (IRQ)

* Leading bit = LSB = Bit 0
** Data bit will be zero in 7-bit plus parity modes.
*** Data bit is "don't care" in 7-bit plus parity modes.

the data is retained in the RDR. The status is maintained by RDRF as to whether or not the data is current. When the Receive Data Register is full, the automatic transfer of data from the Receiver Shift Register to the Data Register is inhibited and the RDR contents remain valid with its current status stored in the Status Register.

CONTROL REGISTER

The ACIA Control Register consists of eight bits of write-only buffer that are selected when RS and R/W are low. This register controls the function of the receiver, transmitter, interrupt enables, and the Request-to-Send peripheral/modem control output.

Counter Divide Select Bits (CR0 and CR1) – The Counter Divide Select Bits (CR0 and CR1) determine the divide ratios utilized in both the transmitter and receiver sections of the ACIA. Additionally, these bits are used to provide a master reset for the ACIA which clears the Status Register (except for external conditions on $\overline{CTS}$ and $\overline{DCD}$) and initializes both the receiver and transmitter. Master reset does not affect other Control Register bits. Note that after power-on or a power fail/restart, these bits must be set high to reset the ACIA. After reseting, the clock divide ratio may be selected. These counter select bits provide for the following clock divide ratios:

CR1	CR0	Function
0	0	÷ 1
0	1	÷ 16
1	0	÷ 64
1	1	Master Reset

Word Select Bits (CR2, CR3, and CR4) – The Word Select bits are used to select word length, parity, and the number of stop bits. The encoding format is as follows:

CR4	CR3	CR2	Function
0	0	0	7 Bits + Even Parity + 2 Stop Bits
0	0	1	7 Bits + Odd Parity + 2 Stop Bits
0	1	0	7 Bits + Even Parity + 1 Stop Bit
0	1	1	7 Bits + Odd Parity + 1 Stop Bit
1	0	0	8 Bits + 2 Stop Bits
1	0	1	8 Bits + 1 Stop Bit
1	1	0	8 Bits + Even Parity + 1 Stop Bit
1	1	1	8 Bits + Odd Parity + 1 Stop Bit

Word length, Parity Select, and Stop Bit changes are not buffered and therefore become effective immediately.

Transmitter Control Bits (CR5 and CR6) – Two Transmitter Control bits provide for the control of the interrupt from the Transmit Data Register Empty condition, the Request-to-Send ($\overline{RTS}$) output, and the transmission of a Break level (space). The following encoding format is used:

CR6	CR5	Function
0	0	$\overline{RTS}$ = low, Transmitting Interrupt Disabled.
0	1	$\overline{RTS}$ = low, Transmitting Interrupt Enabled.
1	0	$\overline{RTS}$ = high, Transmitting Interrupt Disabled.
1	1	$\overline{RTS}$ = low, Transmits a Break level on the Transmit Data Output. Transmitting Interrupt Disabled.

Receive Interrupt Enable Bit (CR7) – The following interrupts will be enabled by a high level in bit position 7 of the Control Register (CR7): Receive Data Register Full, Overrun, or a low to high transistion on the Data Carrier Detect ($\overline{DCD}$) signal line.

STATUS REGISTER

Information on the status of the ACIA is available to the MPU by reading the ACIA Status Register. This read-only register is selected when RS is low and R/W is high. Information stored in this register indicates the status of the Transmit Data Register, the Receive Data Register and error logic, and the peripheral/modem status inputs of the ACIA.

Receive Data Register Full (RDRF), Bit 0 – Receive Data Register Full indicates that received data has been transferred to the Receive Data Register. RDRF is cleared after an MPU read of the Receive Data Register or by a master reset. The cleared or empty state indicates that the contents of the Receive Data Register are not current. $\overline{\text{Data Carrier Detect}}$ being high also causes RDRF to indicate empty.

Transmit Data Register Empty (TDRE), Bit 1 – The Transmit Data Register Empty bit being set high indicates that the Transmit Data Register contents have been transferred and that new data may be entered. The low state indicates that the register is full and that transmission of a new character has not begun since the last write data command.

$\overline{\text{Data Carrier Detect}}$ ($\overline{\text{DCD}}$), Bit 2 – The $\overline{\text{Data Carrier Detect}}$ bit will be high when the $\overline{\text{DCD}}$ input from a modem has gone high to indicate that a carrier is not present. This bit going high causes an Interrupt Request to be generated when the Receive Interrupt Enable is set. It remains high after the $\overline{\text{DCD}}$ input is returned low until cleared by first reading the Status Register and then the Data Register or until a master reset occurs. If the $\overline{\text{DCD}}$ input remains high after read status and read data or master reset has occurred, the interrupt is cleared, the $\overline{\text{DCD}}$ status bit remains high and will follow the $\overline{\text{DCD}}$ input.

Clear-to-Send ($\overline{\text{CTS}}$), Bit 3 – The $\overline{\text{Clear-to-Send}}$ bit indicates the state of the $\overline{\text{Clear-to-Send}}$ input from a modem. A low $\overline{\text{CTS}}$ indicates that there is a $\overline{\text{Clear-to-Send}}$ from the modem. In the high state, the Transmit Data Register Empty bit is inhibited and the $\overline{\text{Clear-to-Send}}$ status bit will be high. Master reset does not affect the $\overline{\text{Clear-to-Send}}$ Status bit.

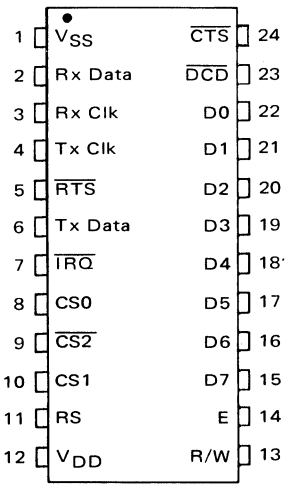
Framing Error (FE), Bit 4 – Framing error indicates that the received character is improperly framed by a start and a stop bit and is detected by the absence of the 1st stop bit. This error indicates a synchronization error, faulty transmission, or a break condition. The framing error flag is set or reset during the receive data transfer time. Therefore, this error indicator is present throughout the time that the associated character is available.

Receiver Overrun (OVRN), Bit 5 – Overrun is an error flag that indicates that one or more characters in the data stream were lost. That is, a character or a number of characters were received but not read from the Receive Data Register (RDR) prior to subsequent characters being received. The overrun condition begins at the midpoint of the last bit of the second character received in succession without a read of the RDR having occurred. The Overrun does not occur in the Status Register until the valid character prior to Overrun has been read. The RDRF bit remains set until the Overrun is reset. Character synchronization is maintained during the Overrun condition. The Overrun indication is reset after the reading of data from the Receive Data Register or by a Master Reset.

Parity Error (PE), Bit 6 – The parity error flag indicates that the number of highs (ones) in the character does not agree with the preselected odd or even parity. Odd parity is defined to be when the total number of ones is odd. The parity error indication will be present as long as the data character is in the RDR. If no parity is selected, then both the transmitter parity generator output and the receiver parity check results are inhibited.

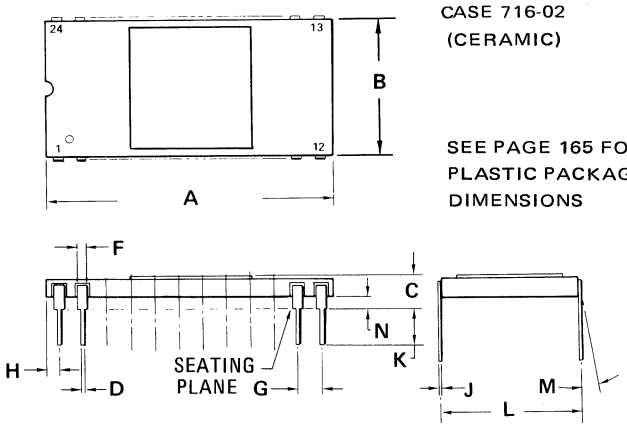
Interrupt Request ($\overline{\text{IRQ}}$), Bit 7 – The IRQ bit indicates the state of the $\overline{\text{IRQ}}$ output. Any interrupt condition with its applicable enable will be indicated in this status bit. Anytime the $\overline{\text{IRQ}}$ output is low the IRQ bit will be high to indicate the interrupt or service request status. IRQ is cleared by a read operation to the Receive Data Register or a write operation to the Transmit Data Register.

PIN ASSIGNMENT



PACKAGE DIMENSIONS

CASE 716-02
(CERAMIC)



SEE PAGE 165 FOR PLASTIC PACKAGE DIMENSIONS

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	29.97	30.99	1.180	1.220
B	14.88	15.62	0.585	0.615
C	3.05	4.19	0.120	0.165
D	0.38	0.53	0.015	0.021
F	0.76	1.40	0.030	0.055
G	2.54 BSC		0.100 BSC	
H	0.76	1.78	0.030	0.070
J	0.20	0.30	0.008	0.012
K	2.54	4.19	0.100	0.165
L	14.88	15.37	0.585	0.605
M	–	10^0	–	10^0
N	0.51	1.52	0.020	0.060

NOTE:
1. LEADS TRUE POSITIONED WITHIN 0.25mm (0.010) DIA (AT SEATING PLANE) AT MAXIMUM MATERIAL CONDITION.

MOTOROLA Semiconductors
BOX 20912 • PHOENIX, ARIZONA 85036

MC6852
(0 to 70°C; L or P Suffix)

MC6852C
(-40 to 85°C; L Suffix only)

SYNCHRONOUS SERIAL DATA ADAPTER (SSDA)

The MC6852 Synchronous Serial Data Adapter provides a bi-directional serial interface for synchronous data information interchange. It contains interface logic for simultaneously transmitting and receiving standard synchronous communications characters in bus organized systems such as the M6800 Microprocessor systems.

The bus interface of the MC6852 includes select, enable, read/write, interrupt, and bus interface logic to allow data transfer over an 8-bit bi-directional data bus. The parallel data of the bus system is serially transmitted and received by the synchronous data interface with synchronization, fill character insertion/deletion, and error checking. The functional configuration of the SSDA is programmed via the data bus during system initialization. Programmable control registers provide control for variable word lengths, transmit control, receive control, synchronization control, and interrupt control. Status, timing and control lines provide peripheral or modem control.

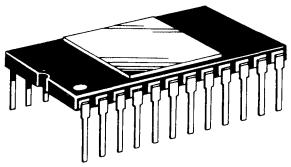
Typical applications include floppy disk controllers, cassette or cartridge tape controllers, data communications terminals, and numerical control systems.

- Programmable Interrupts from Transmitter, Receiver, and Error Detection Logic
- Character Synchronization on One or Two Sync Codes
- External Synchronization Available for Parallel-Serial Operation
- Programmable Sync Code Register
- Up to 600 kbps Transmission
- Peripheral/Modem Control Functions
- Three Bytes of FIFO Buffering on Both Transmit and Receive
- Seven, Eight, or Nine Bit Transmission
- Optional Even and Odd Parity
- Parity, Overrun, and Underflow Status

MOS

(N-CHANNEL, SILICON-GATE)

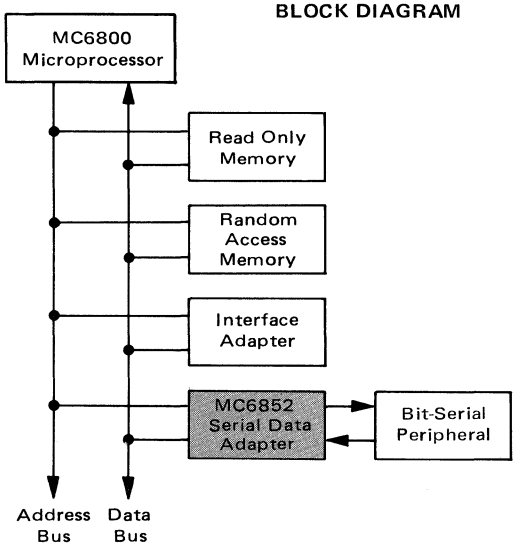
SYNCHRONOUS SERIAL DATA ADAPTER



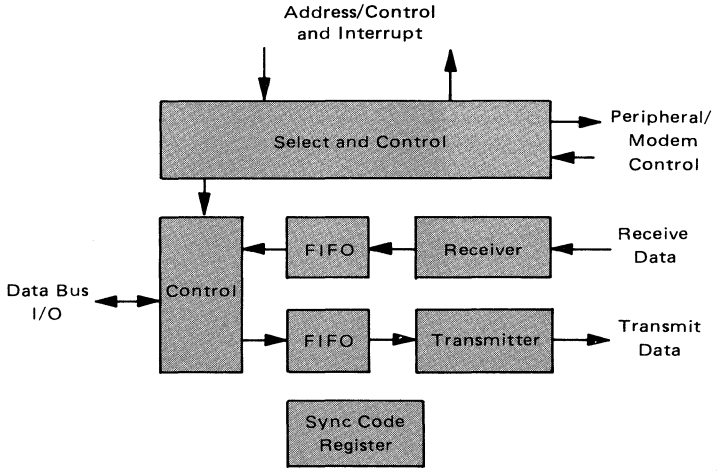
L SUFFIX
CERAMIC PACKAGE
CASE 716

NOT SHOWN: **P SUFFIX**
PLASTIC PACKAGE
CASE 709

M6800 MICROCOMPUTER FAMILY BLOCK DIAGRAM



MC6852 SYNCHRONOUS SERIAL DATA ADAPTER BLOCK DIAGRAM



MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	-0.3 to +7.0	Vdc
Input Voltage	V_{in}	-0.3 to +7.0	Vdc
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	-55 to +150	°C
Thermal Resistance	θ_{JA}	70	°C/W

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, **is is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.**

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V ±5%, V_{SS} = 0, T_A = 0 to 70°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Input High Voltage	V_{IH}	V_{SS} + 2.0	–	–	Vdc
Input Low Voltage	V_{IL}	–	–	V_{SS} + 0.8	Vdc
Input Leakage Current (Tx Clk, Rx Clk, Rx Data, Enable, Reset, RS, R/W, CS, DCD, CTS) (V_{in} = 0 to 5.25 Vdc)	I_{in}	–	1.0	2.5	μAdc
Three-State (Off State) Input Current (D0–D7) (V_{in} = 0.4 to 2.4 Vdc, V_{CC} = 5.25 Vdc)	I_{TSI}	–	2.0	10	μAdc
Output High Voltage (I_{Load} = -205 μAdc, Enable Pulse Width <25 μs) D0–D7	V_{OH}	V_{SS} + 2.4	–	–	Vdc
(I_{Load} = -100 μAdc, Enable Pulse Width <25 μs) Tx Data, DTR, TUF		V_{SS} + 2.4	–	–	
Output Low Voltage (I_{Load} = 1.6 mAdc, Enable Pulse Width <25 μs)	V_{OL}	–	–	V_{SS} + 0.4	Vdc
Output Leakage Current (Off State) (IRQ) (V_{OH} = 2.4 Vdc)	I_{LOH}	–	1.0	10	μAdc
Power Dissipation	P_D	–	300	525	mW
Input Capacitance (V_{in} = 0, T_A = 25°C, f = 1.0 MHz) D0–D7	C_{in}	–	–	12.5	pF
All Other Inputs		–	–	7.5	
Output Capacitance (Tx Data, SM/DTR, TUF) (V_{in} = 0, T_A = 25°C, f = 1.0 MHz) (IRQ)	C_{out}	–	–	10 5.0	pF
Minimum Clock Pulse Width, Low (Figure 1)	PW_{CL}	700	–	–	ns
Minimum Clock Pulse Width, High (Figure 2)	PW_{CH}	700	–	–	ns
Clock Frequency	f_C	–	–	600	kHz
Receive Data Setup Time (Figure 3, 7)	t_{RDSU}	350	–	–	ns
Receive Data Hold Time (Figure 3)	t_{RDH}	350	–	–	ns
Sync Match Delay Time (Figure 3)	t_{SM}	–	–	1.0	μs
Clock-to-Data Delay for Transmitter (Figure 4)	t_{TDD}	–	–	1.0	μs
Transmitter Underflow (Figure 4,6)	t_{TUF}	–	–	1.0	μs
DTR Delay Time (Figure 5)	t_{DTR}	–	–	1.0	μs
Interrupt Request Release Time (Figure 5)	t_{IR}	–	–	1.2	μs
Reset Minimum Pulse Width	t_{Res}	1.0	–	–	μs
CTS Setup Time (Figure 6)	t_{CTS}	–	–	200	ns
DCD Setup Time (Figure 7)	t_{DCD}	–	–	500	ns
Input Rise and Fall Times (except Enable) (0.8 V to 2.0 V)	t_r, t_f	–	–	1.0*	μs

*1.0 μs or 10% of the pulse width, whichever is smaller.

FIGURE 1 – CLOCK PULSE WIDTH, LOW-STATE

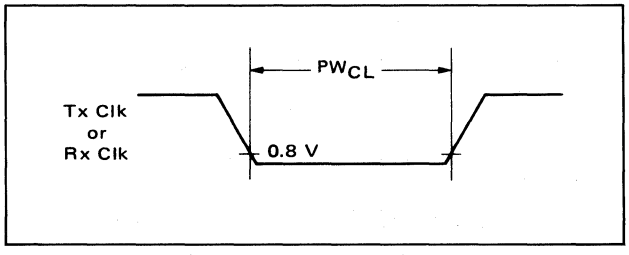
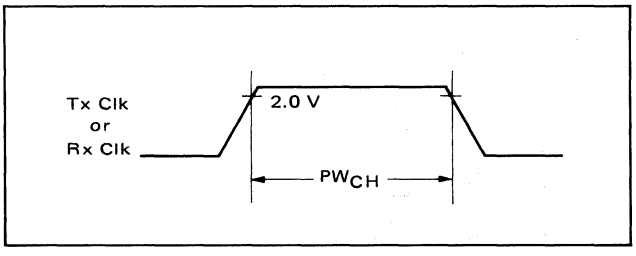


FIGURE 2 – CLOCK PULSE WIDTH, HIGH-STATE



BUS TIMING CHARACTERISTICS

READ (Figures 8 and 10)

Characteristic	Symbol	Min	Typ	Max	Unit
Enable Cycle Time	t_{cycE}	1.0	–	–	μs
Enable Pulse Width, High	PW_{EH}	0.45	–	25	μs
Enable Pulse Width, Low	PW_{EL}	0.43	–	–	μs
Setup Time, Address and R/W valid to Enable positive transition	t_{AS}	160	–	–	ns
Data Delay Time	t_{DDR}	–	–	320	ns
Data Hold Time	t_H	10	–	–	ns
Address Hold Time	t_{AH}	10	–	–	ns
Rise and Fall Time for Enable input	t_{Er}, t_{Ef}	–	–	25	ns

WRITE (Figures 9 and 10)

Enable Cycle Time	t_{cycE}	1.0	–	–	μs
Enable Pulse Width, High	PW_{EH}	0.45	–	25	μs
Enable Pulse Width, Low	PW_{EL}	0.43	–	–	μs
Setup Time, Address and R/W valid to Enable positive transition	t_{AS}	160	–	–	ns
Data Setup Time	t_{DSW}	195	–	–	ns
Data Hold Time	t_H	10	–	–	ns
Address Hold Time	t_{AH}	10	–	–	ns
Rise and Fall Time for Enable input	t_{Er}, t_{Ef}	–	–	25	ns

FIGURE 3 – RECEIVE DATA SETUP AND HOLD TIMES AND SYNC MATCH DELAY TIME

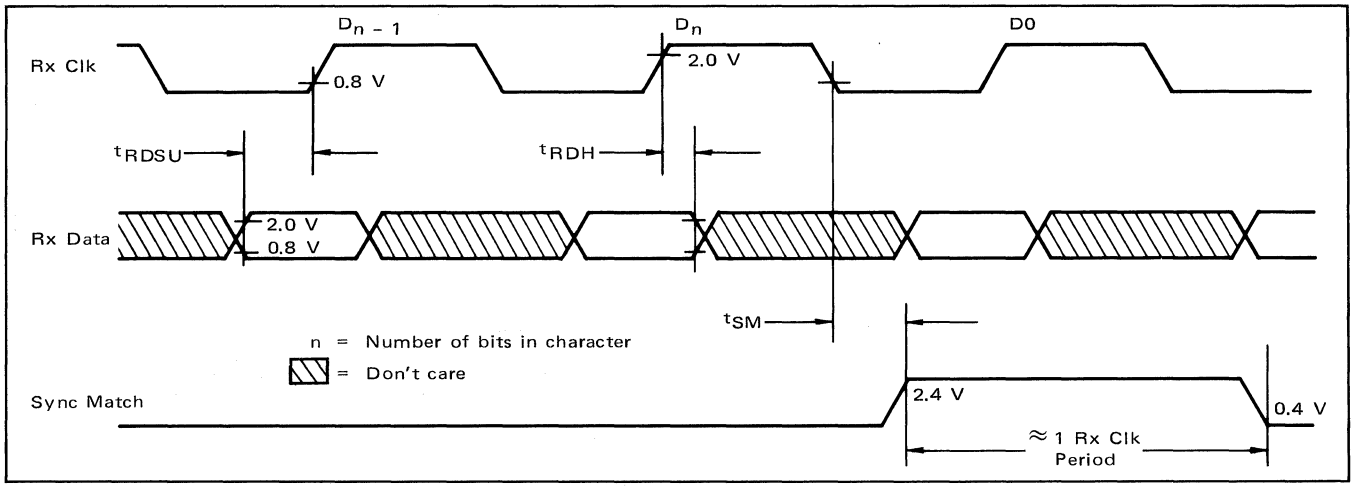


FIGURE 4 – TRANSMIT DATA OUTPUT DELAY AND TRANSMITTER UNDERFLOW DELAY TIME

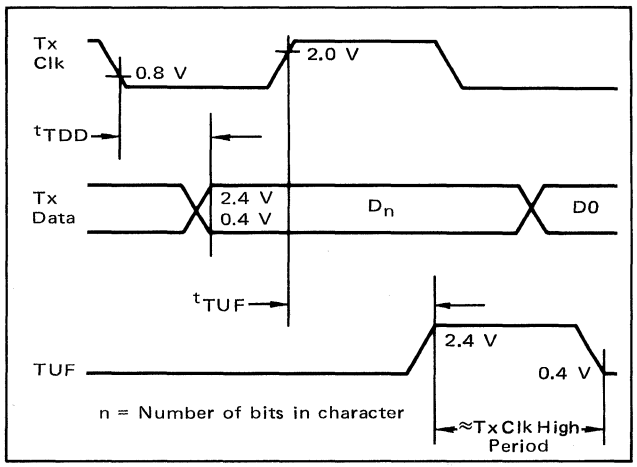


FIGURE 5 – $\overline{\text{DATA TERMINAL READY}}$ AND $\overline{\text{INTERRUPT REQUEST}}$ RELEASE TIMES

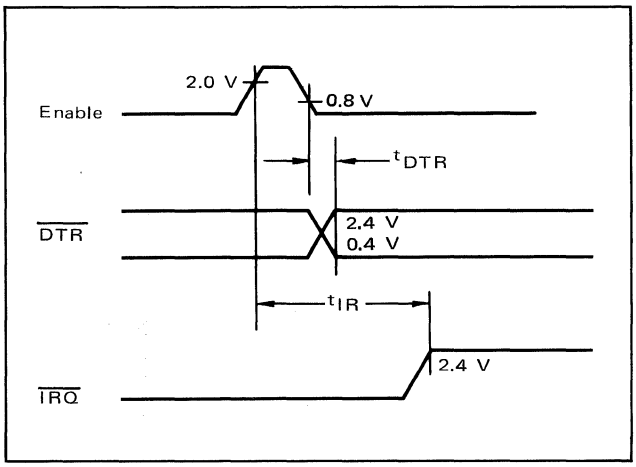


FIGURE 6 – $\overline{\text{CLEAR-TO-SEND}}$ SETUP TIME

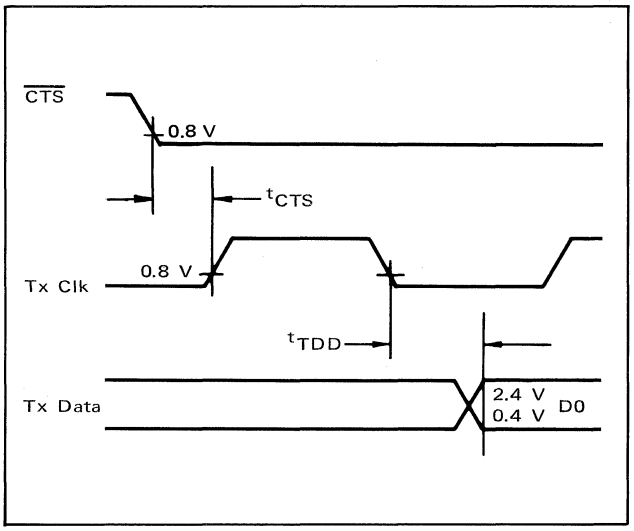


FIGURE 7 – $\overline{\text{DATA CARRIER DETECT}}$ SETUP TIME

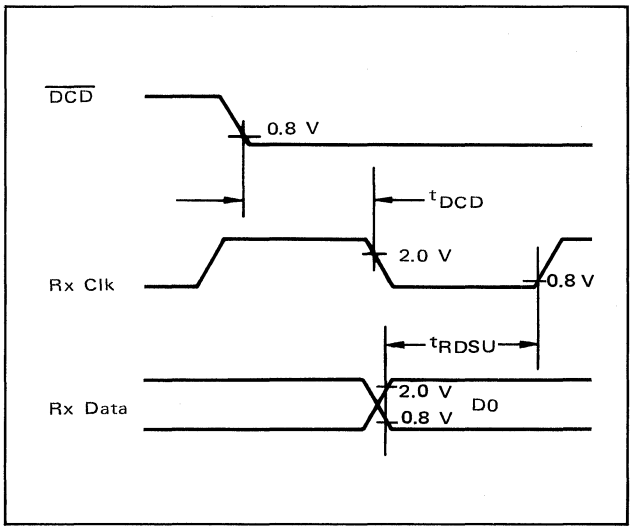


FIGURE 8 – BUS READ TIMING CHARACTERISTICS
(Read information from SSDA)

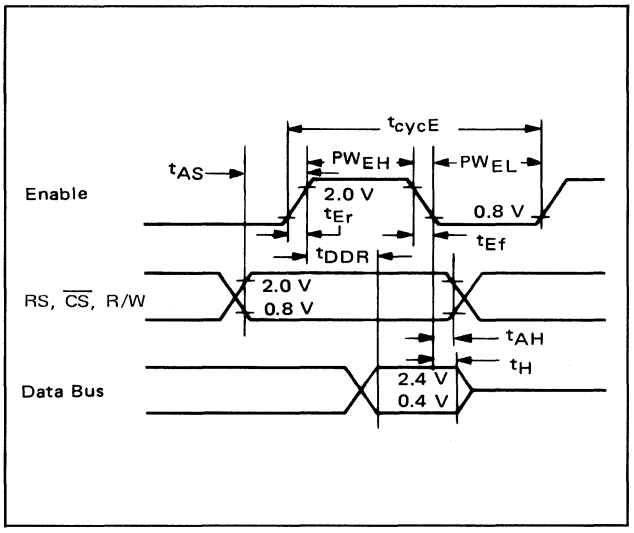


FIGURE 9 – BUS WRITE TIMING CHARACTERISTICS
(Write information into SSDA)

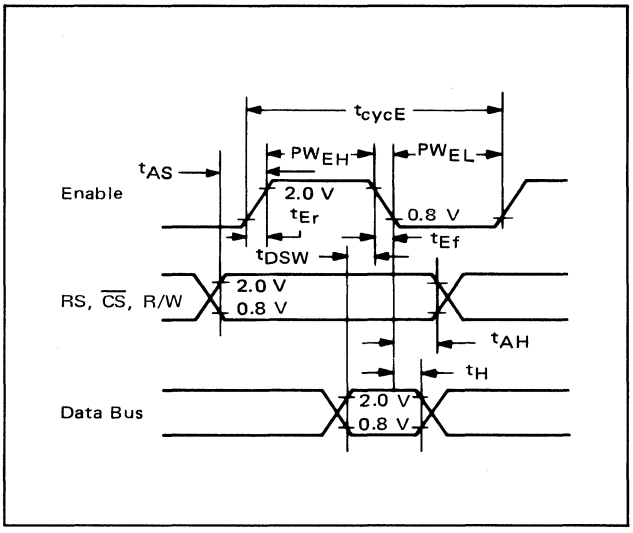
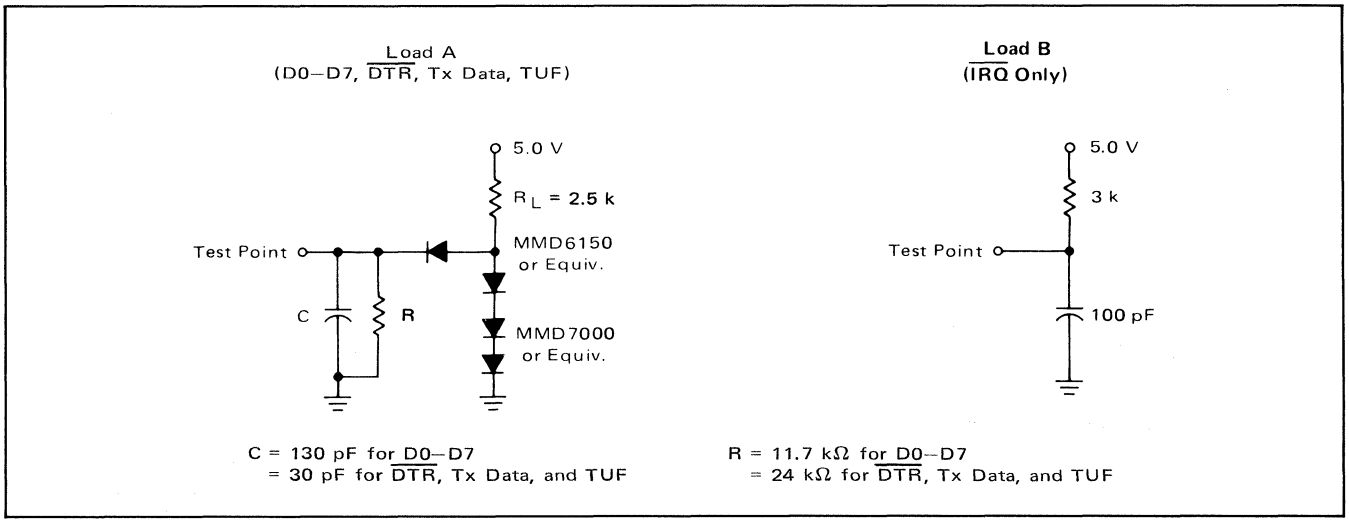
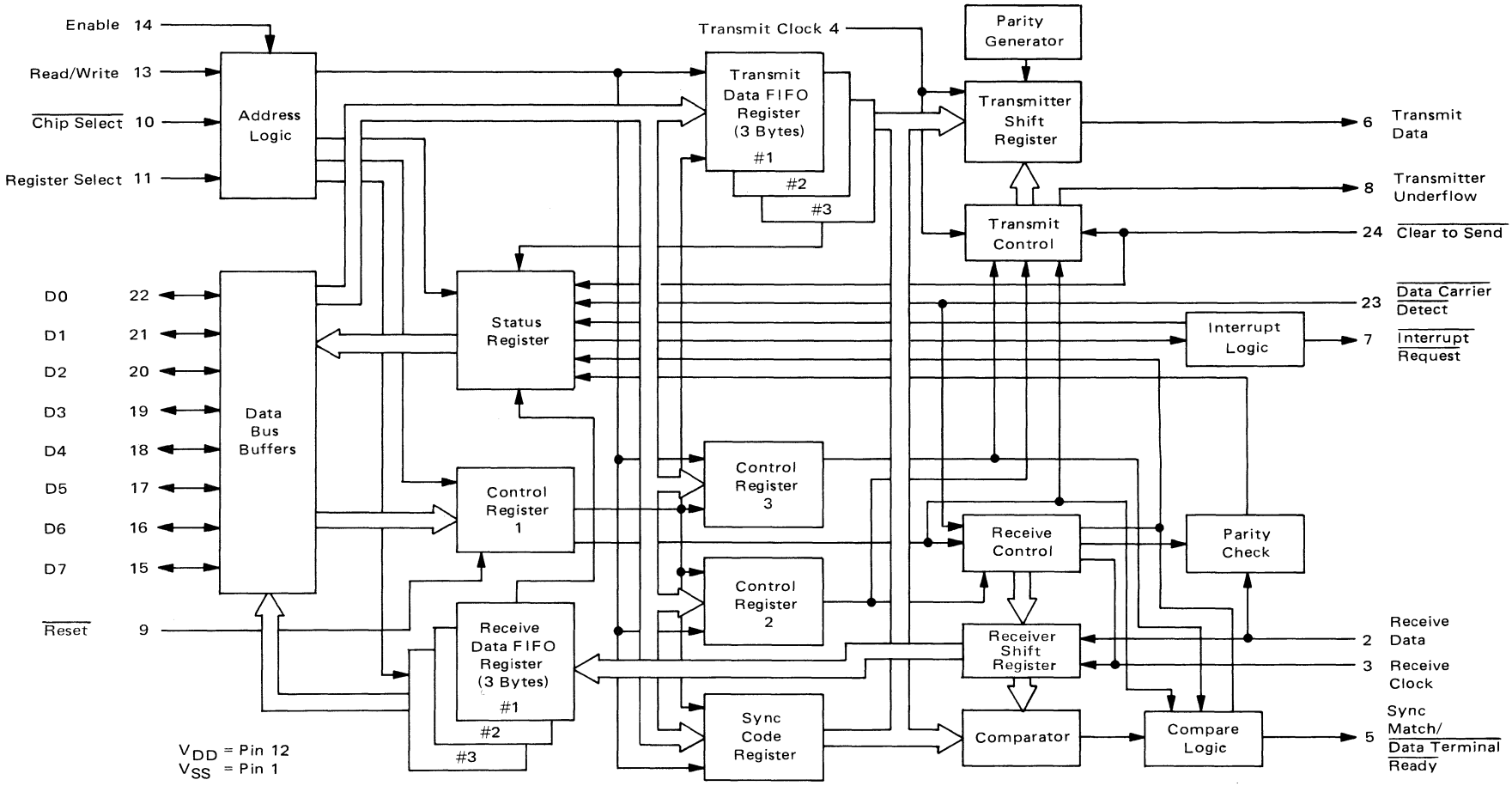


FIGURE 10 – BUS TIMING TEST LOADS



EXPANDED BLOCK DIAGRAM



DEVICE OPERATION

At the bus interface, the SSDA appears as two addressable memory locations. Internally, there are seven registers: two read-only and five write-only registers. The read-only registers are Status and Receive Data; the write-only registers are Control 1, Control 2, Control 3, Sync Code and Transmit Data. The serial interface consists of serial input and output lines with independent clocks, and four peripheral/modem control lines.

Data to be transmitted is transferred directly into the 3-byte Transmit Data First-In First-Out (FIFO) Register from the data bus. Availability of the input to the FIFO is indicated by a bit in the Status Register; once data is entered, it moves through the FIFO to the last empty location. Data at the output of the FIFO is automatically transferred from the FIFO to the Transmitter Shift Register as the shift register becomes available to transmit the next character. If data is not available from the FIFO (underflow condition), the Transmitter Shift Register is automatically loaded with either a sync code or an all "1"s character. The transmit section may be programmed to append even, odd, or no parity to the transmitted word. An external control line ($\overline{\text{Clear-to-Send}}$) is provided to inhibit the transmitter without clearing the FIFO.

Serial data is accumulated in the receiver based on the synchronization mode selected. In the external sync mode, used for parallel-serial operation, the receiver is synchronized by the $\overline{\text{DCD}}$ ($\overline{\text{Data Carrier Detect}}$) input and transfers successive bytes of data to the input of the Receiver FIFO. The single-sync-character mode requires that a match occur between the Sync Code Register and one incoming character before data transfer to the FIFO begins. The two-sync-character mode requires that two sync codes be received in sequence to establish synchronization. Subsequent to synchronization in any mode, data is accumulated in the shift register, and parity is optionally checked. An indication of parity error is carried through the Receiver FIFO with each character to the last empty location. Availability of a word at the FIFO output is indicated by a bit in the Status Register, as is a parity error.

The SSDA and its internal registers are selected by the address bus, Read/Write (R/W) and Enable control lines. To configure the SSDA, Control Registers are selected and the appropriate bits set. The Status Register is addressable for reading status.

Other I/O lines, in addition to $\overline{\text{Clear-to-Send}}$ ($\overline{\text{CTS}}$) and $\overline{\text{Data Carrier Detect}}$ ($\overline{\text{DCD}}$), include SM/$\overline{\text{DTR}}$ (Sync Match/$\overline{\text{Data Terminal Ready}}$) and Transmitter Underflow (TUF). The transmitter and receiver each have individual clock inputs allowing simultaneous operation under separate clock control. Signals to the microprocessor are the Data bus and $\overline{\text{Interrupt Request}}$ ($\overline{\text{IRQ}}$).

INITIALIZATION

During a power-on sequence, the SSDA is reset via the $\overline{\text{Reset}}$ input and internally latched in a reset condition to prevent erroneous output transitions. The Sync Code Register, Control Register 2, and Control Register 3 should be programmed prior to the programmed release of the Transmitter and/or Receiver Reset bits; these bits in Control Register 1 should be cleared after the $\overline{\text{Reset}}$ line has gone high.

TRANSMITTER OPERATION

Data is transferred to the transmitter section in parallel form by means of the data bus and Transmit Data FIFO. The Transmit Data FIFO is a 3-byte register whose status is indicated by the Transmitter Data Register Available status bit (TDRA) and its associated interrupt enable bit. Data is transferred through the FIFO on Enable (E) pulses. Two data transfer modes are provided in the SSDA. The 1-byte transfer mode provides for writing data to the transmitter section (and reading from the receiver section) one byte at a time. The 2-byte transfer mode provides for writing two data characters in succession.

Data will automatically transfer from the last register location in the Transmit Data FIFO (when it contains data) to the Transmitter Shift Register during the last half of the last bit of the previous character. A character is transferred into the Shift Register by the Transmitter Clock. Data is transmitted *LSB first,* and odd or even parity can be optionally appended. The unused bit positions in short word length characters from the data bus are "don't cares". (Note: The data bus inputs may be reversed for applications requiring the MSB to be transferred first, e.g., IBM format for floppy disks; however, care must be taken to properly program the control registers — Table 1 will have its bit positions reversed.)

When the Shift Register becomes empty, and data is *not* available for transfer from the Transmit Data FIFO, an "underflow" occurs, and a character is inserted into the transmitter data stream to maintain character synchronization. The character transmitted on underflow will be either a "Mark" (all "1"s) or the contents of the Sync Code Register, depending upon the state of the Transmit Sync Code on Underflow control bit. The underflow condition is indicated by a pulse ($\approx$1 Tx Clk high period) on the Underflow output (when in Tx Sync on underflow mode). The Underflow output occurs coincident with the transfer of the last half of the last bit preceding the underflow character. The Underflow status bit is set until cleared by means of the Clear Underflow control bit. This output may be used in floppy disk systems to synchronize write operations and for appending CRCC.

Transmission is initiated by clearing the Transmitter Reset bit in Control Register 1. When the Transmitter Reset bit is cleared, the first *full* positive half-cycle of the Transmit Clock will initiate the transmit cycle, with the transmission of data or underflow characters beginning on the negative edge of the Transmit Clock pulse which started the cycle. If the Transmit Data FIFO was not loaded, an underflow character will be transmitted (see Figure 4).

The Clear-to-Send ($\overline{CTS}$) input provides for automatic control of the transmitter by means of external system hardware; e.g., the modem $\overline{CTS}$ output provides the control in a data communications system. The $\overline{CTS}$ input resets and inhibits the transmitter section when high, but does not reset the Transmit Data FIFO. The TDRA status bit is inhibited by $\overline{CTS}$ being high in either the one-sync character or two-sync-character mode of operation. In the external sync mode, TDRA is unaffected by $\overline{CTS}$ in order to provide Transmit Data FIFO status for preloading and operating the transmitter under the control of the $\overline{CTS}$ input. When the Transmitter Reset bit (Tx Rs) is set, the Transmit Data FIFO is cleared and the TDRA status bit is cleared. After one E clock has occurred, the Transmit Data FIFO becomes available for new data with TDRA inhibited.

RECEIVER OPERATION

Data and a presynchronized clock are provided to the SSDA receiver section by means of the Receive Data (Rx Data) and Receive Clock (Rx Clk) inputs. The data is a continuous stream of binary data bits without means for identifying character boundaries within the stream. It is, therefore, necessary to achieve character synchronization for the data at the *beginning* of the data block. Once synchronization is achieved, it is assumed to be retained for all successive characters within the block.

Data communications systems utilize the detection of sync codes during the initial portion of the preamble to establish character synchronization. This requires the detection of a single code or two successive sync codes. Floppy disk and cartridge tape units require sixteen bits of defined preamble and cassettes require eight bits of preamble to establish the reference for the start of record. All three are functionally equivalent to the detection of sync codes. Systems which do not utilize code detection techniques require custom logic external to the SSDA for character synchronization and use of the parallel-to-serial (external sync) mode. (Note: The Receiver Shift Register is set to ones when reset.)

SYNCHRONIZATION

The SSDA provides three operating modes with respect to character synchronization: one-sync-character mode, two-sync-character mode, and external sync mode. The external sync mode requires synchronization and control of the receiveing section through the Data Carrier Detect ($\overline{DCD}$) input (see Figure 7). This external synchronization could consist of direct line control from the transmitting end of the serial data link or from external logic designed to detect the start of the message block. The one-sync-character mode searches on a bit-by-bit basis until a match is achieved between the data in the Shift Register and the Sync Code Register. The match indicates character synchronization is complete and will be retained for the message block. In the two-sync-character mode, the receiver searches for the first sync code match on a bit-by-bit basis and then looks for a second *successive* sync code character prior to establishing character synchronization. If the second sync code character is not received, the bit-by-bit search for the first sync code is resumed.

Sync codes received prior to the completion of synchronization (one or two character) are not transferred to the Receive Data FIFO. Redundant sync codes during the preamble or sync codes which occur as "fill characters" can automatically be stripped from the data, when the Strip Sync control bit is set, to minimize system loading. The character synchronization will be retained until cleared by means of the Clear Sync bit, which also inhibits synchronization search when set.

RECEIVING DATA

Once synchronization has been achieved, subsequent characters are automatically transferred into the Receive Data FIFO and clocked through the FIFO to the last empty location by E pulses (MPU System $\phi 2$). The Receiver Data Available status bit (RDA) indicates when data is available to be read from the last FIFO location (#3) when in the 1-byte transfer mode. The 2-byte transfer mode causes the RDA status bit to indicate data is available when the last two FIFO register locations are full. Data being available in the Receive Data FIFO causes an interrupt request if the Receiver Interrupt Enable (RIE) bit is set. The MPU will then read the SSDA Status Register, which will indicate that data is available for the MPU read from the Receive Data FIFO register. The IRQ and RDA status bits are reset by a read from the FIFO. If more than one character has been received and is resident in the Receive Data FIFO, subsequent E clocks will cause the FIFO to update and the RDA and IRQ status bits will again be set. The read data operation for the 2-byte transfer mode requires an intervening E clock between reads to allow the FIFO data to shift. Optional parity is automatically checked as data is received, and the parity status condition is maintained with each character until the data is read from the Receive Data FIFO. Parity errors will cause an interrupt request if the Error Interrupt Enable (EIE) has been set. The parity bit is not trans-

ferred to the data bus but must be checked in the Status Register. NOTE: In the 2-byte transfer mode, parity should be checked prior to reading the second byte, since a FIFO read clears the error bit.

Other status bits which pertain to the receiver section are Receiver Overrun and Data Carrier Detect ($\overline{DCD}$). The Overrun status bit is automatically set when a transfer of a character to the Receive Data FIFO occurs and the first register of the Receive Data FIFO is full. Overrun causes an interrupt if Error Interrupt Enable (EIE) has been set. The transfer of the overrunning character into the FIFO causes the previous character in the FIFO input register location to be lost. The Overrun status bit is cleared by reading the Status Register (when the overrun condition is present), followed by a Receive Data FIFO Register read. Overrun cannot occur and be cleared without providing an opportunity to detect its occurrence via the Status Register.

A positive transition on the $\overline{DCD}$ input causes an interrupt if the EIE control bit has been set. The interrupt caused by $\overline{DCD}$ is cleared by reading the Status Register when the $\overline{DCD}$ status bit is high, followed by a Receive Data FIFO read. The $\overline{DCD}$ status bit will subsequently follow the state of the $\overline{DCD}$ input when it goes low.

INPUT/OUTPUT FUNCTIONS

SSDA INTERFACE SIGNALS FOR MPU

The SSDA interfaces to the MC6800 MPU with an 8-bit bi-directional data bus, a chip select line, a register select line, an interrupt request line, read/write line, an enable line, and a reset line. These signals, in conjunction with the MC6800 VMA output, permit the MPU to have complete control over the SSDA.

SSDA Bi-Directional Data (D0-D7) — The bi-directional data lines (D0-D7) allow for data transfer between the SSDA and the MPU. The data bus output drivers are three-state devices that remain in the high-impedance (off) state except when the MPU performs an SSDA read operation.

SSDA Enable (E) — The Enable signal, E, is a high impedance TTL compatible input that enables the bus input/output data buffers, clocks data to and from the SSDA, and moves data through the FIFO Registers. This signal is normally the continuous MC6800 System $\phi 2$ clock, so that incoming data characters are shifted through the FIFO.

Read/Write (R/W) — The Read/Write line is a high impedance input that is TTL compatible and is used to control the direction of data flow through the SSDA's input/output data bus interface. When Read/Write is high (MPU read cycle), SSDA output drivers are turned on if the chip is selected and a selected register is read. When it is low, the SSDA output drivers are turned off and the MPU writes into a selected register. The Read/Write signal is also used to select read-only or write-only registers within the SSDA.

Chip Select ($\overline{CS}$) — This high impedance TTL compatible input line is used to address the SSDA. The SSDA is selected when $\overline{CS}$ is low. VMA should be used in generating the $\overline{CS}$ input to insure that false selects will not occur. Transfers of data to and from the SSDA are then performed under the control of the Enable signal, Read/Write, and Register Select.

Register Select (RS) — The Register Select line is a high impedance input that is TTL compatible. A high level is used to select Control Registers C2 and C3, the Sync Code Register, and the Transmit/Receive Data Registers. A low level selects the Control 1 and Status Registers (see Table 1).

Interrupt Request ($\overline{IRQ}$) — Interrupt Request is a TTL compatible, open-drain (no internal pullup), active low output that is used to interrupt the MPU. The Interrupt Request remains low until cleared by the MPU.

Reset Input — The Reset input provides a means of resetting the SSDA from an external source. In the low state, the Reset input causes the following:

1. Receiver Reset (Rx Rs) and Transmitter Reset (Tx Rs) bits are set causing both the receiver and transmitter sections to be held in a reset condition.
2. Peripheral Control bits PC1 and PC2 are reset to zero, causing the SM/$\overline{DTR}$ output to be high.
3. The Error Interrupt Enable (EIE) bit is reset.
4. An internal synchronization mode is selected.
5. The Transmitter Data Register Available (TDRA) status bit is cleared and inhibited.

When Reset returns high (the inactive state), the transmitter and receiver sections will remain in the reset state until the Receiver Reset and Transmitter Reset bits are cleared via the bus under software control. The control Register bits affected by Reset (Rx Rs, Tx Rs, PC1, PC2, EIE, and E/I Sync) cannot be changed when Reset is low.

CLOCK INPUTS

Separate high impedance TTL compatible inputs are provided for clocking of transmitted and received data.

Transmit Clock (Tx Clk)— The Transmit Clock input is used for the clocking of transmitted data. The transmitter shifts data on the negative transition of the clock.

Receive Clock (Rx Clk) — The Receive Clock input is used for clocking in received data. The clock and data must be synchronized externally. The receiver samples the data on the positive transition of the clock.

SERIAL INPUT/OUTPUT LINES

Receive Data (Rx Data) – The Receive Data line is a high impedance TTL compatible input through which data is received in a serial format. Data rates are from 0 to 600 kbps.

Transmit Data (Tx Data) – The Transmit Data output line transfers serial data to a modem or other peripheral. Data rates are from 0 to 600 kbps.

PERIPHERAL/MODEM CONTROL

The SSDA includes several functions that permit limited control of a peripheral or modem. The functions included are Clear-to-Send, Sync Match/Data Terminal Ready, Data Carrier Detect, and Transmitter Underflow.

Clear-to-Send ($\overline{CTS}$) – The $\overline{CTS}$ input provides a real-time inhibit to the transmitter section (the Tx Data FIFO is not disturbed). A positive $\overline{CTS}$ transition resets the Tx Shift Register and inhibits the TDRA status bit and its associated interrupt in both the one-sync-character and two-sync-character modes of operation. TDRA is not affected by the $\overline{CTS}$ input in the external sync mode.

The positive transition of $\overline{CTS}$ is stored within the SSDA to insure that its occurrence will be acknowledged by the system. The stored $\overline{CTS}$ information and its associated $\overline{IRQ}$ (if enabled) are cleared by writing a "1" in the Clear $\overline{CTS}$ bit in Control Register 3 or in the Transmitter Reset bit. The $\overline{CTS}$ status bit subsequently follows the $\overline{CTS}$ input when it goes low.

The $\overline{CTS}$ input provides character timing for transmitter data when in the external sync mode. Transmission is initiated on the negative transition of the first *full* positive clock pulse of the transmitter clock (Tx Clk) after the release of $\overline{CTS}$ (see Figure 6).

Data Carrier Detect ($\overline{DCD}$) – The $\overline{DCD}$ input provides a real-time inhibit to the receiver section (the Rx FIFO is not disturbed). A positive $\overline{DCD}$ transition resets and inhibits the receiver section except for the Receive FIFO and the RDRA status bit and its associated $\overline{IRQ}$.

The positive transition of $\overline{DCD}$ is stored within the SSDA to insure that its occurrence will be acknowledged by the system. The stored $\overline{DCD}$ information and its associated $\overline{IRQ}$ (if enabled) are cleared by reading the Status Register and then the Receiver FIFO, or by writing a "1" into the Receiver Reset bit. The $\overline{DCD}$ status bit subsequently follows the $\overline{DCD}$ input when it goes low. The $\overline{DCD}$ input provides character synchronization timing for the receiver during the external sync mode of operation. The receiver will be initialized and data will be sampled on the positive transition of the first *full* Receive Clock cycle after release of $\overline{DCD}$ (see Figure 7).

Sync Match/Data Terminal Ready (SM/$\overline{DTR}$) – The SM/$\overline{DTR}$ output provides four functions (see Table 1) depending on the state of the PC1 and PC2 control bits. When the Sync Match mode is selected (PC1 = "1", PC2 = "0"), the output provides a one-bit-wide pulse when a sync code is detected. The SM output is inhibited when PC2 = "1". The $\overline{DTR}$ mode (PC1 = "0") provides an output level corresponding to the complement of PC2 ($\overline{DTR}$ = "0" when PC2 = "1"). (See Table 1).

Transmitter Underflow (TUF) – The Underflow output indicates the occurrence of a transfer of a "fill character" to the Transmitter Shift Register when the last location (#3) in the Transmit Data FIFO is empty. The Underflow output pulse is approximately a Tx Clk high period wide and occurs during the last half of the last bit of the character preceding the "Underflow" (see Figure 4). The Underflow output does not respond to underflow conditions when the Tx Sync bit is in the reset state.

SSDA REGISTERS

Seven registers in the SSDA can be accessed by means of the bus. The registers are defined as read-only or write-only according to the direction of information flow. The Register Select input (RS) selects two registers in each state, one being read-only and the other write-only. The Read/Write input (R/W) defines which of the two selected registers will actually be accessed. Four registers (two read-only and two write-only) can be addressed via the bus at any particular time. These registers and the required addressing are defined in Table 1.

CONTROL REGISTER 1 (C1)

Control Register 1 is an 8-bit write-only register that can be directly addressed from the data bus. Control Register 1 is addressed when RS = "0" and R/W = "0".

Receiver Reset (Rx Rs), C1 Bit 0 – The Receiver Reset control bit provides both a reset and inhibit function to the receiver section. When Rx Rs is set, it clears the receiver control logic, sync logic, error logic, Rx Data FIFO, Parity Error status bit, and $\overline{DCD}$ interrupt. The Receiver Shift Register is set to ones. The Rx Rs bit must be cleared after the occurrence of a low level on $\overline{Reset}$ in order to enable the receiver section of the SSDA.

Transmitter Reset (Tx Rs), C1 Bit 1 – The Transmitter Reset control bit provides both a reset and inhibit to the transmitter section. When Tx Rs is set, it clears the transmitter control section, Transmitter Shift Register, Tx Data FIFO (which can be reloaded after one E clock pulse), the Transmitter Underflow status bit, and the $\overline{CTS}$ interrupt, and inhibits the TDRA status bit (in the one-sync-character and two-sync-character modes). The Tx Rs bit must be cleared after the occurrence of a

TABLE 1 – SSDA PROGRAMMING MODEL

Register	Control Inputs		Address Control		Register Content							
	RS	R/W	AC2	AC1	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status (S)	0	1	X	X	Interrupt Request (IRQ)	Receiver Parity Error (PE)	Receiver Overrun (Rx Ovrn)	Transmitter Underflow (TUF)	Clear-to-Send ($\overline{CTS}$)	Data Carrier Detect ($\overline{DCD}$)	Transmitter Data Register Available (TDRA)	Receiver Data Available (RDA)
Control 1 (C1)	0	0	X	X	Address Control 2 (AC2)	Address Control 1 (AC1)	Receiver Interrupt Enable (RIE)	Transmitter Interrupt Enable (TIE)	Clear Sync	Strip Sync Characters (Strip Sync)	Transmitter Reset (Tx Rs)	Receiver Reset (Rx Rs)
Receive Data FIFO	1	1	X	X	D7	D6	D5	D4	D3	D2	D1	D0
Control 2 (C2)	1	0	0	0	Error Interrupt Enable (EIE)	Transmit Sync Code on Underflow (Tx Sync)	Word Length Select 3 (WS3)	Word Length Select 2 (WS2)	Word Length Select 1 (WS1)	1-Byte/2-Byte Transfer (1-Byte/2-Byte)	Peripheral Control 2 (PC2)	Peripheral Control 1 (PC1)
Control 3 (C3)	1	0	0	1	Not Used	Not Used	Not Used	Not Used	Clear Transmitter Underflow Status (CTUF)	Clear $\overline{CTS}$ Status (Clear $\overline{CTS}$)	One-Sync-Character/ Two-Sync Character Mode Control (1 Sync/ 2 Sync)	External/ Internal Sync Mode Control (E/I Sync)
Sync Code	1	0	1	0	D7	D6	D5	D4	D3	D2	D1	D0
Transmit Data FIFO	1	0	1	1	D7	D6	D5	D4	D3	D2	D1	D0

X = Don't care

STATUS REGISTER

IRQ Bit 7 The IRQ flag is cleared when the source of the IRQ is cleared. The source is determined by the enables in the Control Registers: TIE, RIE, EIE.

Bits 6-0 indicate the SSDA status at a point in time, and can be *reset* as follows:

PE Bit 6 Read Rx Data FIFO, or a "1" into Rx Rs (C1 Bit 0).

Rx Ovrn Bit 5 Read Status and then Rx Data FIFO, or a "1" into Rx Rs (C1 Bit 0).

TUF Bit 4 A "1" into CTUF (C3 Bit 3) or into Tx Rs (C1 Bit 1).

$\overline{CTS}$ Bit 3 A "1" into Clear $\overline{CTS}$ (C3 Bit 2) or a "1" into Tx Rs (C1 Bit1)

$\overline{DCD}$ Bit 2 Read Status and then Rx Data FIFO or a "1" into Rx Rs (C1 Bit 0)

TDRA Bit 1 Write into Tx Data FIFO.

RDA Bit 0 Read Rx Data FIFO.

CONTROL REGISTER 1

AC2, AC1 Bits 7, 6 Used to access other registers, as shown above.

RIE Bit 5 When "1", enables interrupt on RDA (S Bit 0).

TIE Bit 4 When "1", enables interrupt on TDRA (S Bit 1).

Clear Sync Bit 3 When "1", clears receiver character synchronization.

Strip Sync Bit 2 When "1", strips all sync codes from the received data stream.

Tx Rs Bit 1 When "1", resets and inhibits the transmitter section.

Rx Rs Bit 0 When "1", resets and inhibits the receiver section.

CONTROL REGISTER 3

CTUF Bit 3 When "1", clears TUF (S Bit 4), and IRQ if enabled.

Clear $\overline{CTS}$ Bit 2 When "1", clears $\overline{CTS}$ (S Bit 3), and IRQ if enabled.

1 Sync/2 Sync Bit 1 When "1", selects the one-sync-character mode; when "0", selects the two-sync-character mode.

E/I Sync Bit 0 When "1", selects the external sync mode; when "0", selects the internal sync mode.

CONTROL REGISTER 2

EIE Bit 7 When "1", enables the PE, Rx Ovrn, TUF, $\overline{CTS}$, and $\overline{DCD}$ interrupt flags (S Bits 6 through 2).

Tx Sync Bit 6 When "1", allows sync code contents to be transferred on underflow, and **enables the TUF Status bit and output. When "0", an all mark character is transmitted on underflow.**

WS3, 2, 1 Bits 5-3 Word Length Select

Bit 5 WS3	Bit 4 WS2	Bit 3 WS1	Word Length
0	0	0	6 Bits + Even Parity
0	0	1	6 Bits + Odd Parity
0	1	0	7 Bits
0	1	1	8 Bits
1	0	0	7 Bits + Even Parity
1	0	1	7 Bits + Odd Parity
1	1	0	8 Bits + Even Parity
1	1	1	8 Bits + Odd Parity

1-Byte/2-Byte Bit 2 When "1", enables the TDRA and RDA bits to indicate when a 1-byte transfer can occur; when "0", the TDRA and RDA bits indicate when a 2-byte transfer can occur.

PC2, PC1 Bits 1-0 SM/$\overline{DTR}$ Output Control

Bit 1 PC2	Bit 0 PC1	SM/$\overline{DTR}$ Output at Pin 5
0	0	1
0	1	Pulse ⎍, 1-Bit Wide, on SM
1	0	0
1	1	SM Inhibited, 0

NOTE: When the SSDA is used in applications requiring the MSB of data to be received and transmitted first, the data bus inputs to the SSDA may be reversed (D0 to D7, etc.). Caution must be used when this is done since the bit positions in this table will be reversed, and the parity should not be selected.

low level on $\overline{\text{Reset}}$ in order to enable the transmitter section of the SSDA.

Strip Synchronization Characters (Strip Sync), C1 Bit 2 – If the Strip Sync bit is set, the SSDA will automatically strip all received characters which match the contents of the Sync Code Register. The characters used for synchronization (one or two characters of sync) are always stripped from the received data stream.

Clear Synchronization (Clear Sync), C1 Bit 3 – The Clear Sync control bit provides the capability of dropping receiver character synchronization and inhibiting resynchronization. The Clear Sync bit is set to clear and inhibit receiver synchronization in *all* modes and is reset to zero to enable resynchronization.

Transmitter Interrupt Enable (TIE), C1 Bit 4 – TIE enables both the Interrupt Request output ($\overline{\text{IRQ}}$) and Interrupt Request status bit to indicate a transmitter service request. When TIE is set and the TDRA status bit is high, the $\overline{\text{IRQ}}$ output will go low (the active state) and the IRQ status bit will go high.

Receiver Interrupt Enable (RIE), C1 Bit 5 – RIE enables both the Interrupt Request output ($\overline{\text{IRQ}}$) and the Interrupt Request status bit to indicate a receiver service request. When RIE is set and the RDA status bit is high, the $\overline{\text{IRQ}}$ output will go low (the active state) and the IRQ status bit will go high.

Address Control 1 (AC1) and Address Control 2 (AC2), C1 Bits 6 and 7 – AC1 and AC2 select one of the write-only registers – Control 2, Control 3, Sync Code, or Tx Data FIFO–as shown in Table 1, when RS = "1" and R/W = "0".

CONTROL REGISTER 2 (C2)

Control Register 2 is an 8-bit write-only register which can be programmed from the bus when the Address Control bits in Control Register 1 (AC1 and AC2) are reset, RS = "1" and R/W = "0".

Peripheral Control 1 (PC1) and Peripheral Control 2 (PC2), C2 Bits 0 and 1– Two control bits, PC1 and PC2, determine the operating characteristics of the Sync Match/$\overline{\text{DTR}}$ output. PC1, when high, selects the Sync Match mode. PC2 provides the inhibit/enable control for the SM/$\overline{\text{DTR}}$ output in the Sync Match mode. A one-bit-wide pulse is generated at the output when PC2 is "0", and a match occurs between the contents of the Sync Code Register and the incoming data even if sync is inhibited (Clear Sync bit = "1"). The Sync Match pulse is referenced to the negative edge of Rx Clk pulse causing the match (see Figure 3).

The Data Terminal Ready ($\overline{\text{DTR}}$) mode is selected when PC1 is low. When PC2 = "1" the SM/$\overline{\text{DTR}}$ output = "0" and vice versa. The operation of PC2 and PC1 is summarized in Table 1.

1-Byte/2-Byte Transfer (1-Byte/2-Byte), C2 Bit 2 – When 1-Byte/2-Byte is set, the TDRA and RDA status bits will indicate the availability of their respective data FIFO registers for a single byte data transfer. Alternately, if 1 Byte/2 Byte is reset, the TDRA and RDA status bits indicate when two bytes of data can be moved without a second status read. An intervening Enable pulse must occur between data transfers.

Word Length Selects (WS1, WS2, WS3), C2 Bits 3, 4, 5 – Word Length Select bits WS1, WS2, and WS3 select word length of 7, 8, or 9 bits including parity as shown in Table 1.

Transmit Sync Code on Underflow (Tx Sync), C2 Bit 6 – When Tx Sync is set, the transmitter will automatically send a sync character when data is not available for transmission. If Tx Sync is reset, the transmitter will transmit a Mark character (including the parity bit position) on underflow. When the underflow is detected, a pulse approximately a Tx Clk high period wide will occur on the underflow output if the Tx Sync bit is set. Internal parity generation is inhibited during underflow except for sync code fill character transmission in 8 bit plus parity word lengths.

Error Interrupt Enable (EIE), C2 Bit 7 – When EIE is set, the IRQ status bit will go high and the $\overline{\text{IRQ}}$ output will go low if:

1. A receiver overrun occurs. The interrupt is cleared by reading the Status Register and reading the Rx Data FIFO.
2. $\overline{\text{DCD}}$ input has gone to a "1". The interrupt is cleared by reading the Status Register and reading the Rx Data FIFO.
3. A parity error exists for the character in the last location (#3) of the Rx Data FIFO. The interrupt is cleared by reading the Rx Data FIFO.
4. The $\overline{\text{CTS}}$ input has gone to a "1". The interrupt is cleared by writing a "1" in the Clear $\overline{\text{CTS}}$ bit, C3 bit 2, or by a Tx Reset.
5. The transmitter has underflowed (in the Tx Sync on Underflow mode). The interrupt is cleared by writing a "1" into the Clear Underflow, C3 bit 3, or Tx Reset.

When EIE is a "0", the IRQ status bit and the $\overline{\text{IRQ}}$ output are disabled for the above error conditions. A low level on the $\overline{\text{Reset}}$ input resets EIE to "0".

CONTROL REGISTER 3 (C3)

Control Register 3 is a 4-bit write-only register which can be programmed from the bus when RS = "1" and R/W = "0" and Address Control bit AC1 = "1" and AC2 = "0".

External/Internal Sync Mode Control (E/I Sync), C3 Bit 0 – When the E/I Sync Mode bit is high, the SSDA is in the external sync mode and the receiver synchronization logic is disabled. Synchronization can be achieved by means of the $\overline{DCD}$ input or by starting Rx Clk at the midpoint of data bit 0 of a character with $\overline{DCD}$ low. Both the transmitter and receiver sections operate as parallel – serial converters in the External Sync mode. The Clear Sync bit in Control Register 1 acts as a receiver sync inhibit when high to provide a bus controllable inhibit. The Sync Code Register can serve as a transmitter fill character register and a receiver match register in this mode. A "low" on the $\overline{Reset}$ input resets the E/I Sync Mode bit placing the SSDA in the internal sync mode.

One-Sync-Character/Two-Sync-Character Mode Control (1 Sync/2 Sync), C3 Bit 1 – When the 1 Sync/2 Sync bit is set, the SSDA will synchronize on a single match between the received data and the contents of the Sync Code Register. When the 1 Sync/2 Sync bit is reset, two *successive* sync characters must be received prior to receiver synchronization. If the second sync character is not detected, the bit by bit search resumes from the first bit in the second character. See the description of the Sync Code Register for more details.

Clear $\overline{CTS}$ Status (Clear $\overline{CTS}$), C3 Bit 2 – When a "1" is written into the Clear $\overline{CTS}$ bit, the stored status and interrupt are cleared. Subsequently, the $\overline{CTS}$ status bit reflects the state of the $\overline{CTS}$ input. The Clear $\overline{CTS}$ control bit does not affect the $\overline{CTS}$ input nor its inhibit of the transmitter section. The Clear $\overline{CTS}$ command bit is self-clearing, and writing a "0" into this bit is a nonfunctional operation.

Clear Transmit Underflow Status (CTUF), C3 Bit 3 – When a "1" is written into the CTUF status bit, the CTUF bit and its associated interrupt are reset. The CTUF command bit is self-clearing and writing a "0" into this bit is a nonfunctional operation.

SYNC CODE REGISTER

The Sync Code Register is an 8-bit register for storing the programmable sync code required for received data character synchronization in the one-sync-character and two-sync-character modes. The Sync Code Register also provides for stripping the sync/fill characters from the received data (a programmable option) as well as automatic insertion of fill characters in the transmitted data stream. The Sync Code Register is not utilized for receiver character synchronization in the external sync mode; however, it provides storage of receiver match and transmit fill characters.

The Sync Code Register can be loaded when AC2 and AC1 are a "1" and "0", respectively, and R/W = "0" and RS = "1".

The Sync Code Register may be changed after the detection of a match with the received data (the first sync code having been detected) to synchronize with a double-word sync pattern. (This sync code change must occur prior to the completion of the second character.) The sync match (SM) output can be used to interrupt the MPU system to indicate that the first eight bits have matched. The service routine would then change the sync match register to the second half of the pattern. Alternately, the one-sync-character mode can be used for sync codes for 16 or more bits by using software to check the second and subsequent bytes after reading them from the FIFO.

The detection of the sync code can be programmed to appear on the Sync Match/$\overline{DTR}$ output by writing a "1" in PC1 (C2 bit 0) and a "0" in PC2 (C2 bit 1). The Sync Match output will go high for one bit time beginning at the character interface between the sync code and the next character (see Figure 3).

RECEIVE DATA FIRST-IN FIRST-OUT REGISTER (Rx Data FIFO)

The Receive Data FIFO Register consists of three 8-bit registers which are used for buffer storage of received data. Each 8-bit register has an internal status bit which monitors its full or empty condition. Data is always transferred from a full register to an adjacent empty register. The transfer from register to register occurs on E pulses. The RDA status bit will be high when data is available in the last location of the Rx Data FIFO.

In an Overrun condition, the overrunning character will be transferred into the full first stage of the FIFO register and will cause the loss of that data character. Successive overruns continue to overwrite the first register of the FIFO. This destruction of data is indicated by means of the Overrun status bit. The Overrun bit will be set when the overrun occurs and remains set until the Status Register is read, followed by a read of the Rx Data FIFO.

Unused data bits for short word lengths (including the parity bit) will appear as "0"s on the data bus when the Rx Data FIFO is read.

TRANSMIT DATA FIRST-IN FIRST-OUT REGISTER (Tx Data FIFO)

The Transmit Data FIFO Register consists of three 8-bit registers which are used for buffer storage of data to be transmitted. Each 8-bit register has an internal status bit which monitors its full or empty condition. Data is always transferred from a full register to an adjacent empty register. The transfer is clocked by E pulses.

The TDRA status bit will be high if the Tx Data FIFO is available for data.

Unused data bits for short word lengths will be handled as "don't cares". The parity bit is not transferred over the data bus since the SSDA generates parity at transmission.

When an Underflow occurs, the Underflow character will be either the contents of the Sync Code Register or an all "1"s character. The underflow will be stored in the Status Register until cleared and will appear on the Underflow output as a pulse approximately a Tx Clk high period wide.

STATUS REGISTER

The Status Register is an 8-bit read-only register which provides the real-time status of the SSDA and the associated serial data channel. Reading the Status Register is a non-destructive process. The method of clearing status bits depends upon the function each bit represents and is discussed for each bit in the register.

Receiver Data Available (RDA), S Bit 0 – The Receiver Data Available status bit indicates when receiver data can be read from the Rx Data FIFO. The receiver data being present in the last register (#3) of the FIFO causes RDA to be high for the 1-byte transfer mode. The RDA bit being high indicates that the last two registers (#2 and #3) are full when in the 2-byte transfer mode. The second character can be read without a second status read (to determine that the character is available). An E pulse must occur between reads of the Rx Data FIFO to allow the FIFO to shift. Status must be read on a word-by-word basis if receiver data error checking is important. The RDA status bit is reset automatically when data is not available.

Transmitter Data Register Available (TDRA), S Bit 1 – The TDRA status bit indicates that data can be loaded into the Tx Data FIFO Register. The first register (#1) of the Tx Data FIFO being empty will be indicated by a high level in the TDRA status bit in the 1-byte transfer mode. The first two registers (#1 and #2) must be empty for TDRA to be high when in the 2-byte transfer mode. The Tx Data FIFO can be loaded with two bytes without an intervening status read; however, one E pulse must occur between loads. TDRA is inhibited by the Tx Reset or $\overline{\text{Reset}}$. When Tx Reset is set, the Tx Data FIFO is cleared and then released on the next E clock pulse. The Tx Data FIFO can then be loaded with up to three characters of data, even though TDRA is inhibited. This feature allows preloading data prior to the release of Tx Reset. A high level on the $\overline{\text{CTS}}$ input inhibits the TDRA status bit in either sync mode of operation (one-sync-character or two-sync-character). $\overline{\text{CTS}}$ does not affect TDRA in the external sync mode. This enables the SSDA to operate under the control of the $\overline{\text{CTS}}$ input with TDRA indicating the status of the Tx Data FIFO. The $\overline{\text{CTS}}$ input does not clear the Tx Data FIFO in any operating mode.

Data Carrier Detect ($\overline{\text{DCD}}$), S Bit 2 – A positive transition on the $\overline{\text{DCD}}$ input is stored in the SSDA until cleared by reading both Status and Rx Data FIFO. A "1" written into Rx Rs also clears the stored $\overline{\text{DCD}}$ status. The $\overline{\text{DCD}}$ status bit, when set, indicates that the $\overline{\text{DCD}}$ input has gone high. The reading of both Status and Receive Data FIFO allows Bit 2 of subsequent Status reads to indicate the state of the $\overline{\text{DCD}}$ input until the next positive transition.

Clear-to-Send ($\overline{\text{CTS}}$), S Bit 3 – A positive transition on the $\overline{\text{CTS}}$ input is stored in the SSDA until cleared by writing a "1" into the Clear $\overline{\text{CTS}}$ control bit or the Tx Rs bit. The $\overline{\text{CTS}}$ status bit, when set, indicates that the $\overline{\text{CTS}}$ input has gone high. The Clear $\overline{\text{CTS}}$ command (a "1" into C3 Bit 2) allows Bit 3 of subsequent Status reads to indicate the state of the $\overline{\text{CTS}}$ input until the next positive transition.

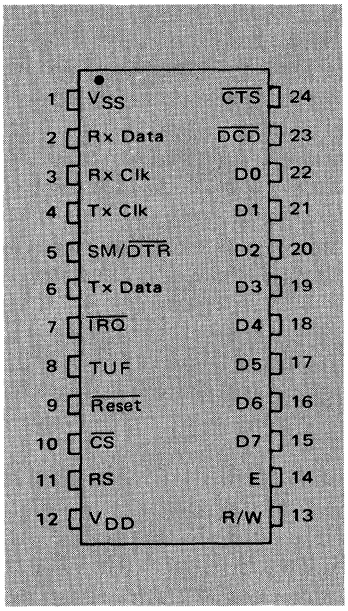
Transmitter Underflow (TUF), S Bit 4 – When data is not available for the transmitter, an underflow occurs and is so indicated in the Status Register (in the Tx Sync on underflow mode). The underflow status bit is cleared by writing a "1" into the Clear Underflow (CTUF) control bit or the Tx Rs bit. TUF indicates that a sync character will be transmitted as the next character. A TUF is indicated on the output *only* when the contents of the Sync Code Register is to be transferred (transmit sync code on underflow = "1").

Receiver Overrun (Rx Ovrn), S Bit 5 – Overrun indicates data has been received when the Rx Data FIFO is full, resulting in data loss. The Rx Ovrn status bit is set when Overrun occurs. The Rx Ovrn status bit is cleared by reading Status followed by reading the Rx Data FIFO or by setting the Rx Rs control bit.

Receiver Parity Error (PE), S Bit 6 – The parity error status bit indicates that parity for the character in the last register of the Rx Data FIFO did not agree with selected parity. The parity error is cleared when the character to which it pertains is read from the Rx Data FIFO or when Rx Rs occurs. The $\overline{\text{DCD}}$ input does not clear the Parity Error or Rx Data FIFO status bits.

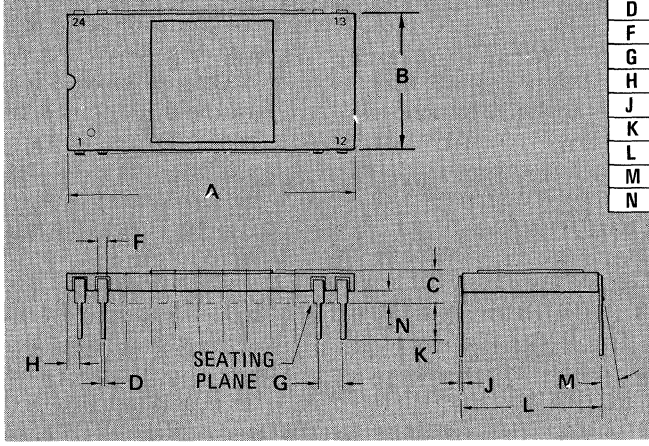
Interrupt Request ($\overline{\text{IRQ}}$), S Bit 7 – The Interrupt Request status bit indicates when the $\overline{\text{IRQ}}$ output is in the active state ($\overline{\text{IRQ}}$ output = "0"). The IRQ status bit is subject to the same interrupt enables (RIE, TIE, and EIE) as the $\overline{\text{IRQ}}$ output. The IRQ status bit simplifies status inquiries for polling systems by providing single bit indication of service requests.

PIN ASSIGNMENT



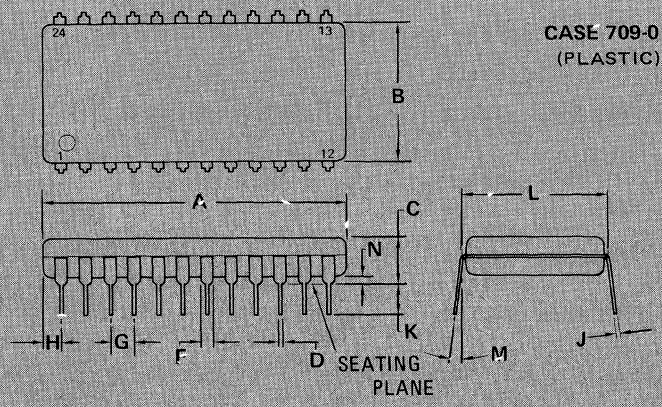
PACKAGE DIMENSIONS

NOTE:
1. LEADS TRUE POSITIONED WITHIN 0.25mm (0.010) DIA (AT SEATING PLANE) AT MAXIMUM MATERIAL CONDITION.



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	29.97	30.99	1.180	1.220
B	14.88	15.62	0.585	0.615
C	3.05	4.19	0.120	0.165
D	0.38	0.53	0.015	0.021
F	0.76	1.40	0.030	0.055
G	2.54 BSC		0.100 BSC	
H	0.76	1.78	0.030	0.070
J	0.20	0.30	0.008	0.012
K	2.54	4.19	0.100	0.165
L	14.88	15.37	0.585	0.605
M	–	10^0	–	10^0
N	0.51	1.52	0.020	0.060

CASE 716-02
(CERAMIC)



CASE 709-01
(PLASTIC)

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	31.37	32.13	1.235	1.265
B	13.72	14.22	0.540	0.560
C	4.57	5.08	0.180	0.200
D	0.36	0.51	0.014	0.020
F	1.02	1.52	0.040	0.060
G	2.41	2.67	0.095	0.105
H	1.78	2.03	0.070	0.080
J	0.20	0.30	0.008	0.012
K	3.05	3.56	0.120	0.140
L	14.73	15.24	0.580	0.600
M	0^0	10^0	0^0	10^0
N	0.51	1.02	0.020	0.040

NOTES:
1. LEADS, TRUE POSITIONED WITHIN 0.25 mm (0.010) DIA AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION. (DIM. "D")
2. DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.

MOTOROLA Semiconductors
BOX 20912 • PHOENIX, ARIZONA 85036

MC6860

(0 to 70°C; L or P Suffix)

MC6860C

(-40 to 85°C; L Suffix only)

0-600 bps DIGITAL MODEM

The MC6860 is a MOS subsystem designed to be integrated into a wide range of equipment utilizing serial data communications.

The modem provides the necessary modulation, demodulation and supervisory control functions to implement a serial data communications link, over a voice grade channel, utilizing frequency shift keying (FSK) at bit rates up to 600 bps. The MC6860 can be implemented into a wide range of data handling systems, including stand alone modems, data storage devices, remote data communication terminals and I/O interfaces for minicomputers.

N-channel silicon gate technology permits the MC6860 to operate using a single voltage supply and be fully TTL compatible.

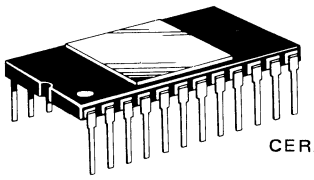
The modem is compatible with the M6800 microcomputer family, interfacing directly with the Asynchronous Communications Interface Adapter to provide low-speed data communications capability.

- Originate and Answer Mode
- Crystal or External Reference Control
- Modem Self Test
- Terminal Interfaces TTL-Compatible
- Full-Duplex or Half-Duplex Operation
- Automatic Answer and Disconnect
- Compatible Functions for 100 Series Data Sets
- Compatible Functions for 1001A/B Data Couplers

MOS

(N-CHANNEL, SILICON-GATE)

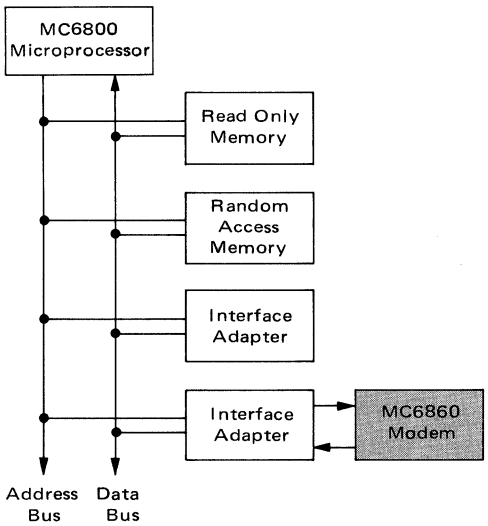
0-600 bps
DIGITAL MODEM



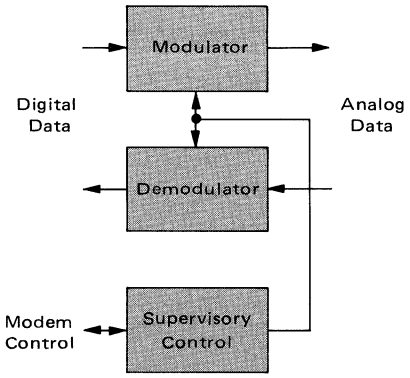
L SUFFIX
CERAMIC PACKAGE
CASE 716

NOT SHOWN: **P SUFFIX**
PLASTIC PACKAGE
CASE 709

M6800 MICROCOMPUTER FAMILY BLOCK DIAGRAM



MC6860 DIGITAL MODEM BLOCK DIAGRAM



MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.3 to +7.0	Vdc
Input Voltage	V_{in}	−0.3 to +7.0	Vdc
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	−55 to +150	°C
Thermal Resistance	θ_{JA}	82.5	°C/W

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

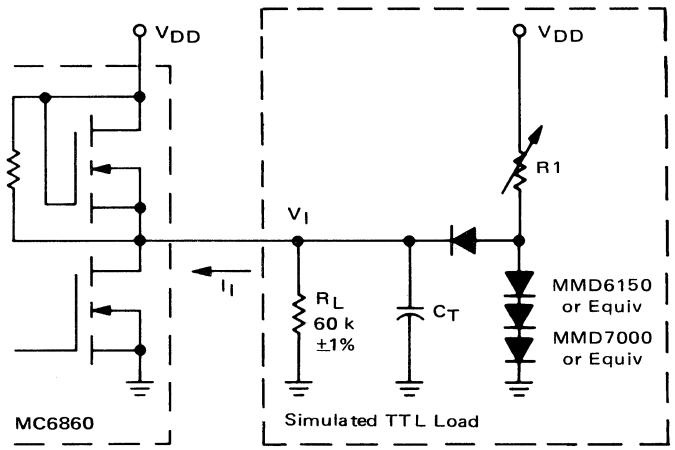
ELECTRICAL CHARACTERISTICS (V_{DD} = 5.0 ±0.25 Vdc, all voltages referenced to V_{SS} = 0, T_A = 0 to 70°C, all outputs loaded as shown in Figure 1 unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Input High Voltage, All Inputs Except Crystal	V_{IH}	2.0	–	V_{DD}	Vdc
Input Low Voltage, All Inputs Except Crystal	V_{IL}	V_{SS}	–	0.80	Vdc
Crystal Input Voltage (Crystal Input Driven from an External Reference, Input Coupling Capacitor = 200 pF, Duty Cycle = 50 ±5%)	V_{in}	1.5	–	2.0	V_{p-p}
Input Current (V_{in} = V_{SS}) All Inputs Except Rx Car, Tx Data, $\overline{TD}$, TST, $\overline{RI}$, $\overline{SH}$	I_{in}	–	–	-0.2	mAdc
$\overline{RI}$, $\overline{SH}$ Inputs		–	–	-1.6	
Input Leakage Current (V_{in} = 7.0 Vdc, V_{DD} = V_{SS}, T_A = 25°C)	I_{IL}	–	–	1.0	μAdc
Output High Voltage, All Outputs Except An Ph and Tx Car (I_{OH1} = -0.04 mAdc, Load A)	V_{OH1}	2.4	–	V_{DD}	Vdc
Output Low Voltage, All Outputs Except An Ph and Tx Car (I_{OL1} = 1.6 mAdc, Load A)	V_{OL1}	V_{SS}	–	0.40	Vdc
Output High Current, An Ph (V_{OH2} = 0.8 Vdc, Load B)	I_{OH2}	0.30	–	–	mAdc
Output Low Voltage, An Ph (I_{OL2} = 0, Load B)	V_{OL2}	V_{SS}	–	0.30	Vdc
Input Capacitance (f = 0.1 MHz, T_A = 25°C)	C_{in}	–	5.0	–	pF
Output Capacitance (f = 0.1 MHz, T_A = 25°C)	C_{out}	–	10	–	pF
Transmit Carrier Output Voltage (Load C)	V_{CO}	0.20	0.35	0.50	V(RMS)
Transmit Carrier Output 2nd Harmonic (Load C)	V_{2H}	-25	-32	–	dB
Input Transition Times, All Inputs Except Crystal	t_r	–	–	1.0*	μs
(Operating in the Crystal Input Mode; from 10% to 90% Points)	t_f	–	–	1.0*	
Input Transition Times, Crystal Input	t_r	–	–	30	ns
(Operating in External Input Reference Mode)	t_f	–	–	30	
Output Transition Times, All Outputs Except Tx Car	t_r	–	–	5.0	μs
(From 10% to 90% Points)	t_f	–	–	5.0	
V_{DD} Supply Current (All Inputs at V_{SS} and All Outputs Open)	I_{DD}	–	30	65	mAdc

*Maximum Input Transition Times are ⩽ 0.1 x Pulse Width or the specified maximum of 1.0 μs, whichever is smaller.

FIGURE 1 – OUTPUT TEST LOADS

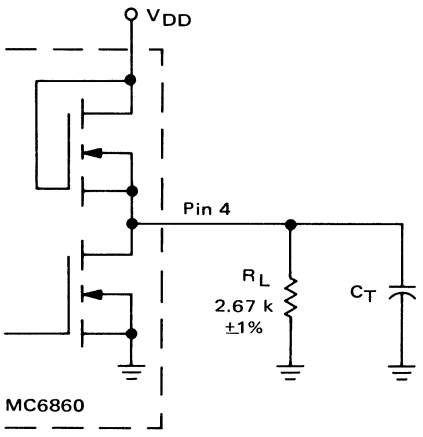
Load A – TTL Output Load for Receive Break, Digital Carrier, Mode, Clear-to-Send, and Receive Data Outputs



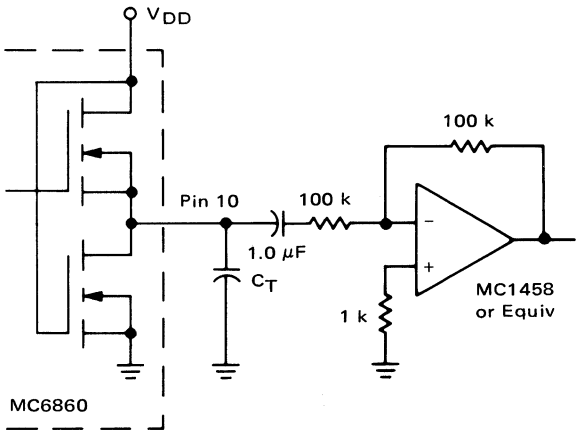
C_T = 20 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances

R1 is adjusted for I_I = 1.6 mA at V_I = 0.4 V when output node is disconnected.

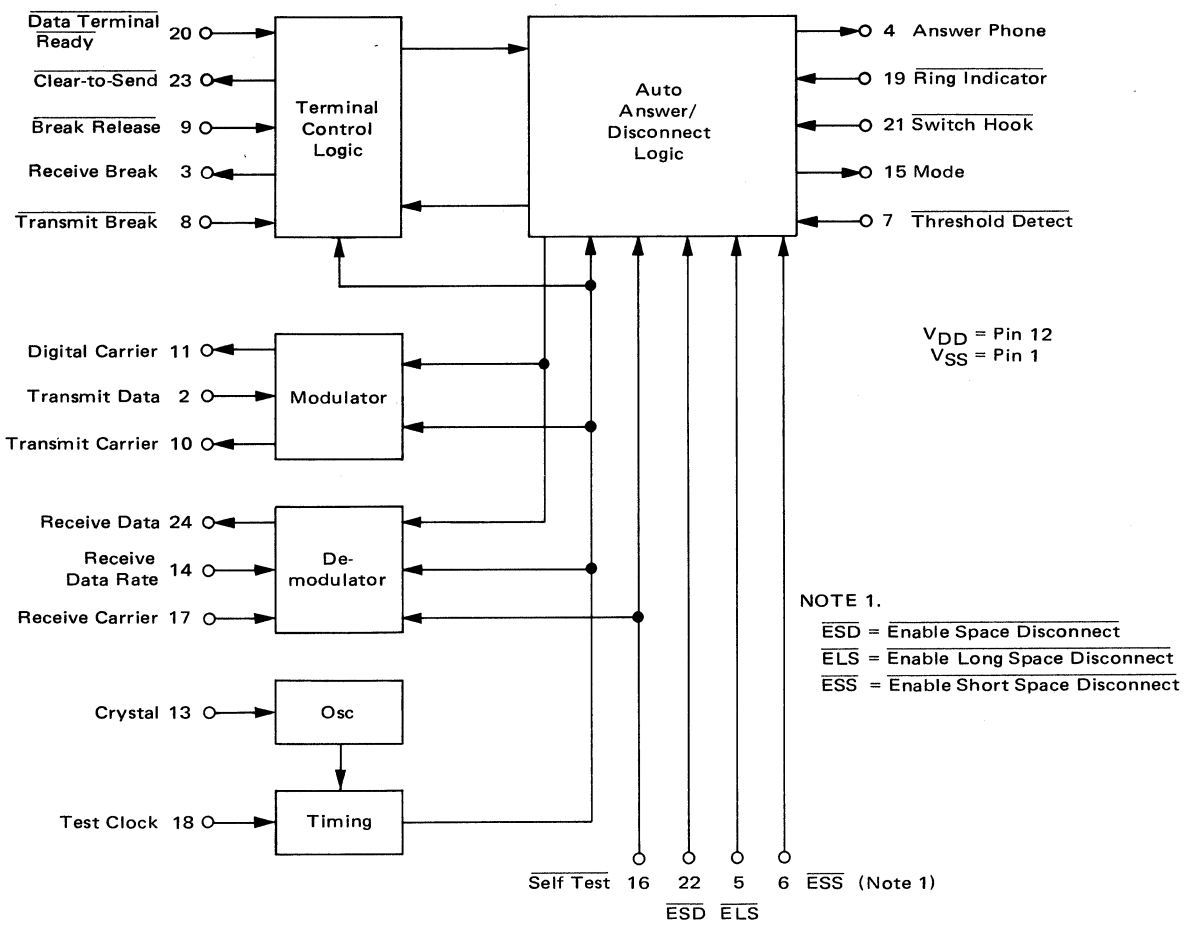
Load B – Answer Phone Load



Load C – Transmit Carrier Load



BLOCK DIAGRAM



DEVICE OPERATION*

GENERAL

Figure 2 shows the modem and its interconnections. The data to be transmitted is presented in serial format to the modulator for conversion to FSK signals for transmission on the telephone line. The modulator output is buffered before driving the line.

The FSK signal from the remote modem is received via the telephone line and filtered to remove extraneous signals such as the local Transmit Carrier. This filtering can be either a bandpass which passes only the desired band of frequencies or a notch which rejects the known interfering signal. The desired signal is then limited to preserve the axis crossings and fed to the demodulator where the data is recovered from the received FSK carrier.

The Supervisory Control provides the necessary commands and responses for handshaking with the remote modem, along with the interface signals to the data coupler and communication terminal. If the modem is a built-in unit, all input-output (I/O) logic need not be RS-232 compatible. However, if the modem is a stand-alone unit the computer-modem I/O interface must conform to the EIA specification. The use of MC1488 and MC1489A line drivers and receivers will provide the required interface.

*See Tables 1 and 2 for delay time tolerances.

Answer Mode

Automatic answering is first initiated by a receipt of a Ring Indicator ($\overline{RI}$) signal. This can be either a low level for at least 51 ms as would come from a CBS data coupler, or at least 20 cycles of a 20-47 Hz ringing signal (low level $\geqslant$ 50% of the duty cycle) as would come from a CBT data coupler. The presence of the Ring Indicator signal places the modem in the Answer Mode; if the Data Terminal Ready line is low, indicating the communication terminal is ready to send or receive data, the Answer Phone output goes high. This output is designed to drive a transistor switch which will activate the Off Hook (OH) and

Data Transmission (DA) relays in the data coupler. Upon answering the phone the 2225-Hz Transmit Carrier is turned on.

The originate modem at the other end detects this 2225-Hz signal and after a 450 ms delay (used to disable any echo suppressors in the telephone network) transmits a 1270-Hz signal which the local answering modem detects, provided the amplitude and frequency requirements are met. The amplitude threshold is set external to the modem chip. If the signal level is sufficient the $\overline{TD}$ input should be low for 20 μs at least once every 32 ms. The absence of a threshold indication for a period greater than 51 ms denotes the loss of Receive Carrier and the modem begins hang-up procedures. Hang-up will occur 17 s after $\overline{RI}$ has been released provided the handshaking routine is not re-established. The frequency tolerance during handshaking is ±100 Hz from the Mark frequency.

After the 1270-Hz signal has been received for 150 ms, the Receive Data is unclamped from a Mark condition and data can be received. The Clear-to-Send output goes low 450 ms after the receipt of carrier and data presented to the answer modem is transmitted.

Automatic Disconnect

Upon receipt of a space of 150 ms or greater duration, the modem clamps the Receive Break high. This condition exists until a Break Release command is issued at the receiving station. Upon receipt of a 0.3 s space, with Enable Short Space Disconnect at the most negative voltage (low), the modem automatically hangs up. If Enable Long Space Disconnect is low, the modem requires 1.5 s of continuous space to hang up.

Originate Mode

Upon receipt of a Switch Hook ($\overline{SH}$) command the modem function is placed in the Originate Mode. If the Data Terminal Ready input is enabled (low) the modem will provide a logic high output at Answer Phone. The modem is now ready to receive the 2225-Hz signal from the remote answering modem. It will continue to look for this signal until 17 s after $\overline{SH}$ has been released. Disconnect occurs if the handshaking routine is not established.

Upon receiving 2225 ±100 Hz for 150 ms at an acceptable amplitude, the Receive Data output is unclamped from a Mark condition and data reception can be accomplished. 450 ms after receiving a 2225-Hz signal, a 1270-Hz signal is transmitted to the remote modem. 750 ms after receiving the 2225-Hz signal, the Clear-to-Send output is taken low and data can now be transmitted as well as received.

Initiate Disconnect

In order to command the remote modem to automatically hang up, a disconnect signal is sent by the local modem. This is accomplished by pulsing the normally low Data Terminal Ready into a high state for greater than

FIGURE 2 – TYPICAL MC6860 SYSTEM CONFIGURATION

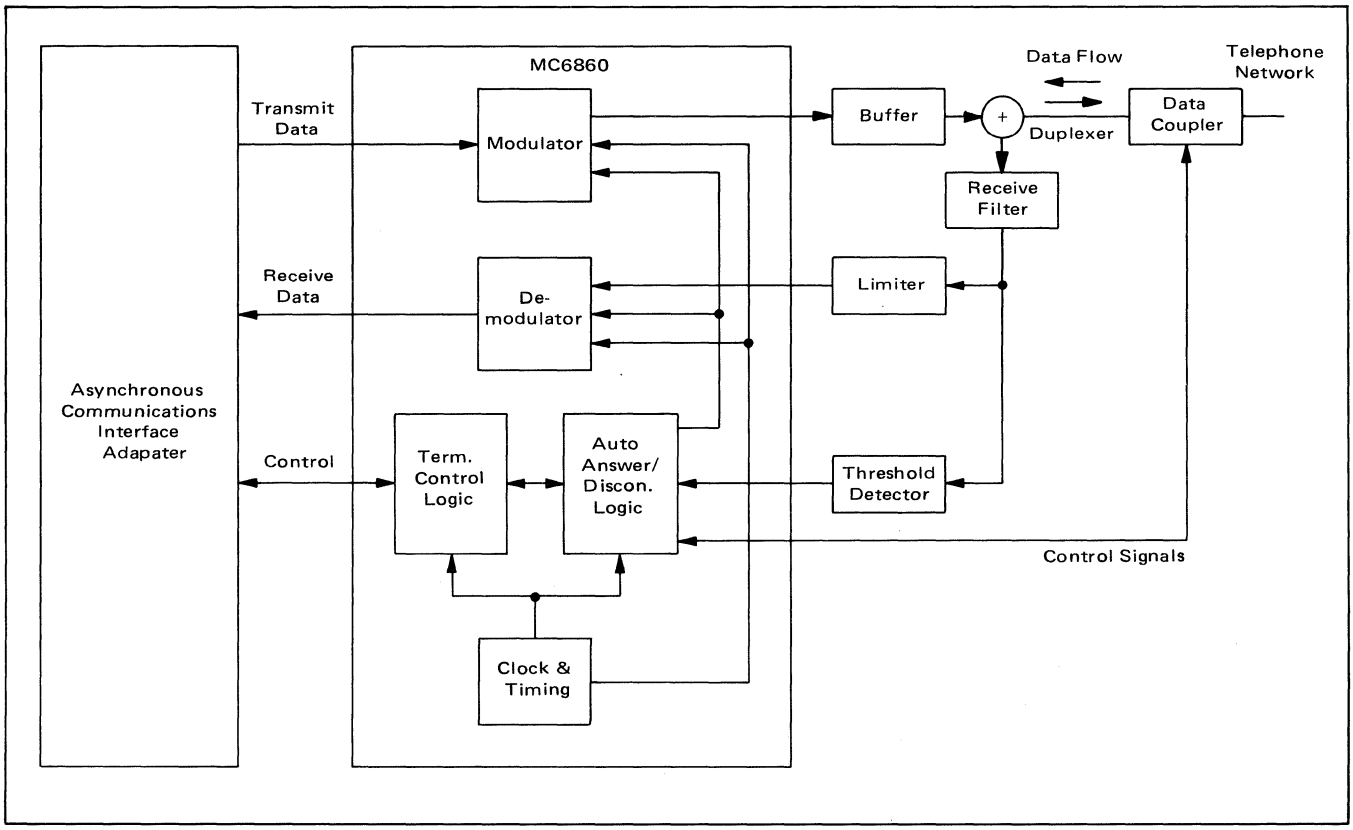
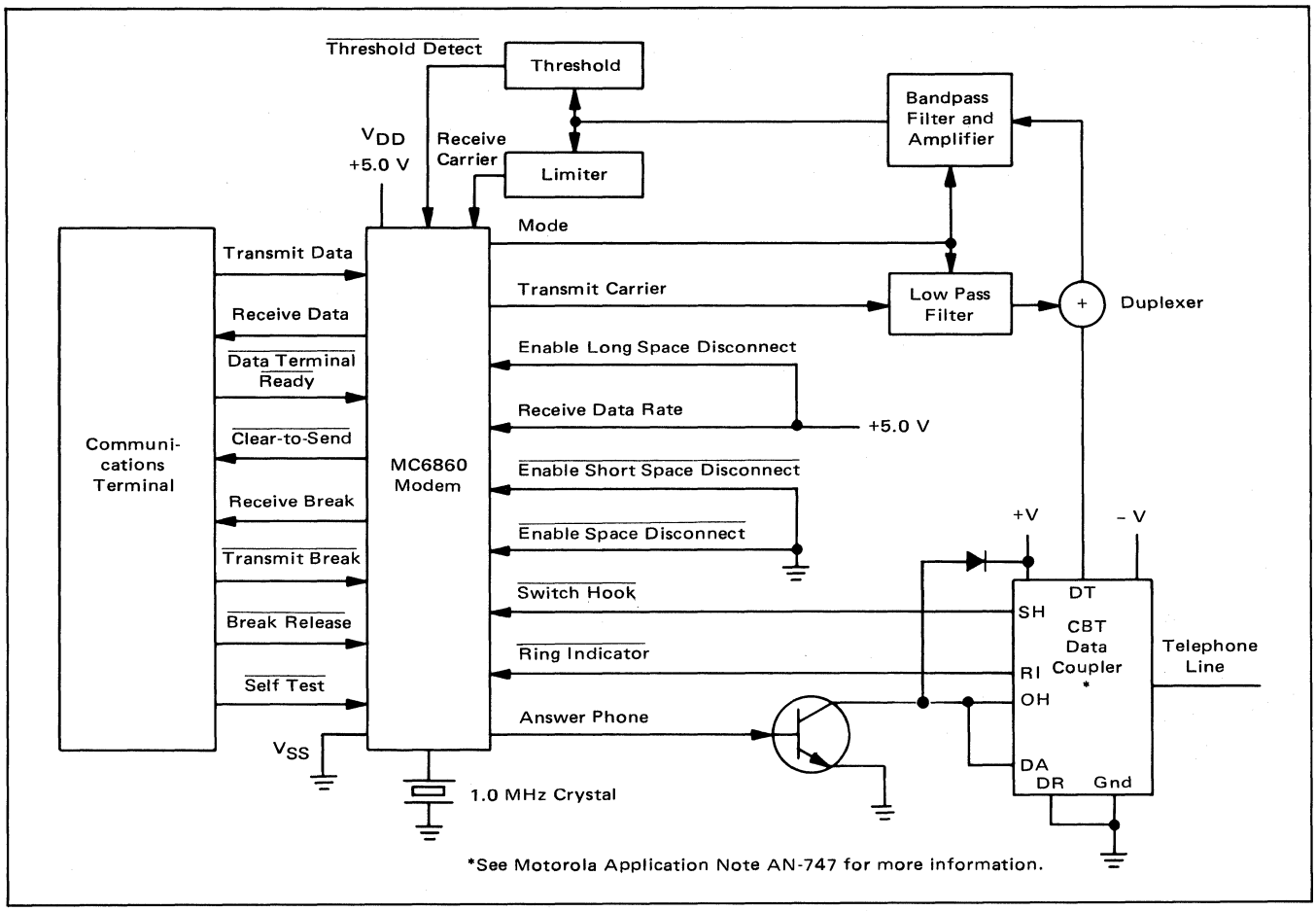


FIGURE 3 – I/O INTERFACE CONNECTIONS FOR MC6860
(ORIGINATE/ANSWER MODEM)



34 ms. The local modem then sends a 3 s continuous space and hangs up provided the Enable Space Disconnect is low. If the remote modem hangs up before 3 s, loss of Threshold Detect will cause loss of Clear-to-Send, which marks the line in Answer Mode and turns the carrier off in the Originate Mode.

If ESD is high the modem will transmit data until hang-up occurs 3 s later. Receive Break is clamped 150 ms following the Data Terminal Ready interrupt.

INPUT/OUTPUT FUNCTIONS

Figure 3 shows the I/O interface for the low speed modem. The following is a description of each individual signal:

Receive Carrier (Rx Car)

The Receive Carrier is the FSK input to the demodulator. The local Transmit Carrier must be balanced or filtered out prior to this input, leaving only the Receive Carrier in the signal. The Receive Carrier must also be hard limited. Any half-cycle period greater than or equal to 429 ± 1.0 μs for the low band or 235 ± 1.0 μs for the high band is detected as a space.

Ring Indicator (RI)

The modem function will recognize the receipt of a call from the CBT if at least 20 cycles of the 20-47 Hz ringing signal (low level ⩾ 50% of the duty cycle) are present. The CBS RI signal must be level-converted to TTL according to the EIA RS-232 specification before interfacing it with the modem function. The receipt of a call from the CBS is recognized if the RI signal is present for at least 51 ms. This input is held high except during ringing. A RI signal automatically places the modem function in the Answer Mode.

Switch Hook (SH)

SH interfaces directly with the CBT and via the EIA RS-232 level conversion for the CBS. An SH signal automatically places the modem function in the Originate Mode.

SH is low during origination of a call. The modem will automatically hang up 17 s after releasing SH if the handshaking routine has not been accomplished.

Threshold Detect (TD)

This input is derived from an external threshold detector. If the signal level is sufficient, the TD input must

be low for 20 μs at least once every 32 ms to maintain normal operation. An insufficient signal level indicates the absence of the Receive Carrier; an absence for less than 32 ms will not cause channel establishment to be lost; however, data during this interval will be invalid.

If the signal is present and the level is acceptable at all times, then the threshold input can be low permanently.

Loss of threshold for 51 ms or longer results in a loss of Clear-to-Send. The Transmit Carrier of the originate modem is clamped off and a constant Mark is transmitted from the answer modem.

Receive Data Rate (Rx Rate)

The demodulator has been optimized for signal-to-noise performance at 300 bps and 600 bps. The Receive Data Rate input must be low for 0-600 bps and should be high for 0-300 bps.

Transmit Data (Tx Data)

Transmit Data is the binary information presented to the modem function for modulation with FSK techniques. A high level represents a Mark.

Data Terminal Ready ($\overline{DTR}$)

The Data Terminal Ready signal must be low before the modem function will be enabled. To initiate a disconnect, $\overline{DTR}$ is held high for 34 ms minimum. A disconnect will occur 3 s later.

Break Release (Brk R)

After receiving a 150 ms space signal, the clamped high condition of the Receive Break output can be removed by holding Break Release low for at least 20 μs.

Transmit Break ($\overline{Tx\ Brk}$)

The Break command is used to signal the remote modem to stop sending data.

A Transmit Break (low) greater than 34 ms forces the modem to send a continuous space signal for 233 ms. Transmit Break must be initiated only after $\overline{CTS}$ has been established. This is a negative edge sense input. Prior to initiating $\overline{Tx\ Brk}$, this input must be held high for a minimum of 34 ms.

Enabled Space Disconnect ($\overline{ESD}$)

When $\overline{ESD}$ is strapped low and $\overline{DTR}$ is pulsed to initiate a disconnect, the modem transmits a space for either 3 s or until a loss of threshold is detected, whichever occurs first. If $\overline{ESD}$ is strapped high, data instead of a space is transmitted. A disconnect occurs at the end of 3 s.

Enable Short Space Disconnect ($\overline{ESS}$)

$\overline{ESS}$ is a strapping option which, when low, will automatically hang up the phone upon receipt of a continuous space for 0.3 s. *$\overline{ESS}$ and $\overline{ELS}$ must not be simultaneously strapped low.*

Enable Long Space Disconnect ($\overline{ELS}$)

$\overline{ELS}$ is a strapping option which, when low, will automatically hang up the phone upon receipt of a continuous space for 1.5 s.

Crystal (Xtal)

A 1.0-MHz crystal with the following parameters is required to utilize the on-chip oscillator. A 1.0-MHz square wave can also be fed into this input to satisfy the clock requirement.

Mode:	Parallel
Frequency:	1.0 MHz ±0.1%
Series Resistance:	750 ohms max
Shunt Capacitance:	7.0 pF max
Temperature:	0-70°C
Test Level:	1.0 mW
Load Capacitance:	13 pF

When utilizing the 1.0-MHz crystal, external parasitic capacitance, including crystal shunt capacitance, must be $\leq$ 9 pF at the crystal input. Reliable crystal oscillator start-up requires that the V_{DD} power-on transition time be $>$ 15 milliseconds.

Test Clock (TST)

A test signal input is provided to decrease the test time of the chip. In normal operation this input *must be strapped low.*

Self Test ($\overline{ST}$)

When a low voltage level is placed on this input, the demodulator is switched to the modulator frequency and demodulates the transmitted FSK signal. Channel establishment, which occurred during the initial handshake, is not lost during self test. The Mode Control output changes state during Self Test, permitting the receive filters to pass the local Transmit Carrier.

$\overline{ST}$	$\overline{SH}$	$\overline{RI}$	Mode
H	L	H	H
H	H	L	L
L	L	H	L
L	H	L	H

Answer Phone (An Ph)

Upon receipt of Ring Indicator or Switch Hook signal and Data Terminal Ready, the Answer Phone output goes high $[(\overline{SH} + \overline{RI}) \bullet \overline{DTR}]$. This signal drives the base of a transistor which activates the Off Hook and Data Transmission control lines in the data coupler. Upon call completion, the Answer Phone signal returns to a low level.

Mode

The Mode output indicates the Answer (low) or Originate (high) status of the modem. This output changes state when a Self Test command is applied.

Clear-To-Send ($\overline{CTS}$)

A low on the $\overline{CTS}$ output indicates the Transmit Data input has been unclamped from a steady Mark, thus allowing data transmission.

Receive Data (Rx Data)

The Receive Data output is the data resulting from demodulating the Receive Carrier. A Mark is a high level.

Receive Break (Rx Brk)

Upon receipt of a continuous 150 ms space, the modem automatically clamps the Receive Break output high. This output is also clamped high until Clear-to-Send is established.

Digital Carrier (FO)

A test signal output is provided to decrease the chip test time. The signal is a square wave at the transmit frequency.

Transmit Carrier (Tx Car)

The Transmit Carrier is a digitally-synthesized sine wave (Figure 4) derived from the 1.0-MHz crystal reference. The frequency characteristics are as follows:

Mode	Data	Transmit Frequency	Tolerance*
Originate	Mark	1270 Hz	-0.15 Hz
Originate	Space	1070 Hz	0.09 Hz
Answer	Mark	2225 Hz	-0.31 Hz
Answer	Space	2025 Hz	-0.71 Hz

*The reference frequency tolerance is not included.

The proper output frequency is transmitted within 3.0 μs following a data bit change with no more than 2.0 μs phase discontinuity. The typical output level is 0.35 V (RMS) into a 100 k-ohm load impedance.

The second harmonic is typically 32 dB below the fundamental (Figure 5).

POWER-ON RESET

Power-on reset is provided on-chip to insure that when power is first applied the Answer Phone output is in the low (inactive) state. This holds the modem in the inactive or idle mode until a $\overline{SH}$ or $\overline{RI}$ signal has been applied. Once power has been applied, a momentary loss of power at a later time may not be of sufficient time to guarantee a chip reset through the power-on reset circuit.

To insure initial power-on reset action, the external parasitic capacitance on $\overline{RI}$ and $\overline{SH}$ should be < 30 pF. Capacitance values > 30 pF may require the use of an external pullup resistor to V_{DD} on these inputs in addition to the pullup devices already provided on chip.

FIGURE 4 – TRANSMIT CARRIER SINE WAVE

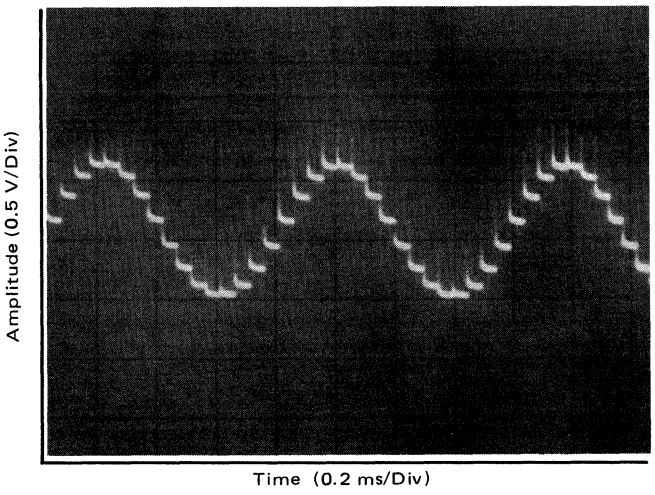
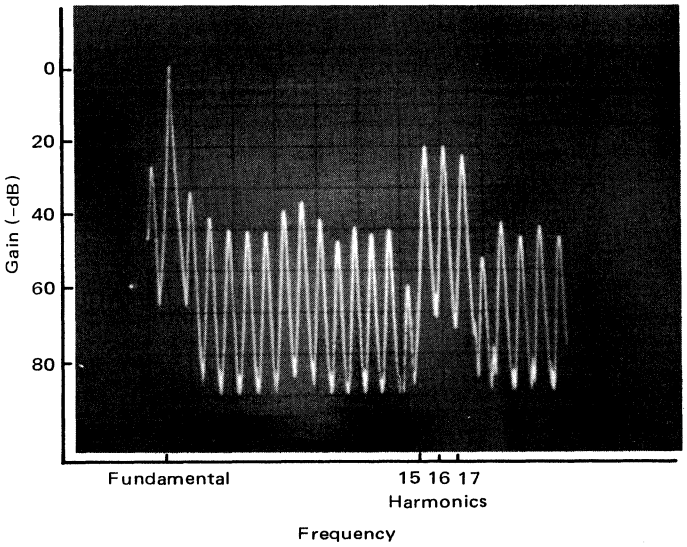


FIGURE 5 – TRANSMIT CARRIER FREQUENCY SPECTRUM



TIMING DIAGRAMS

FIGURE 6 – ANSWER MODE

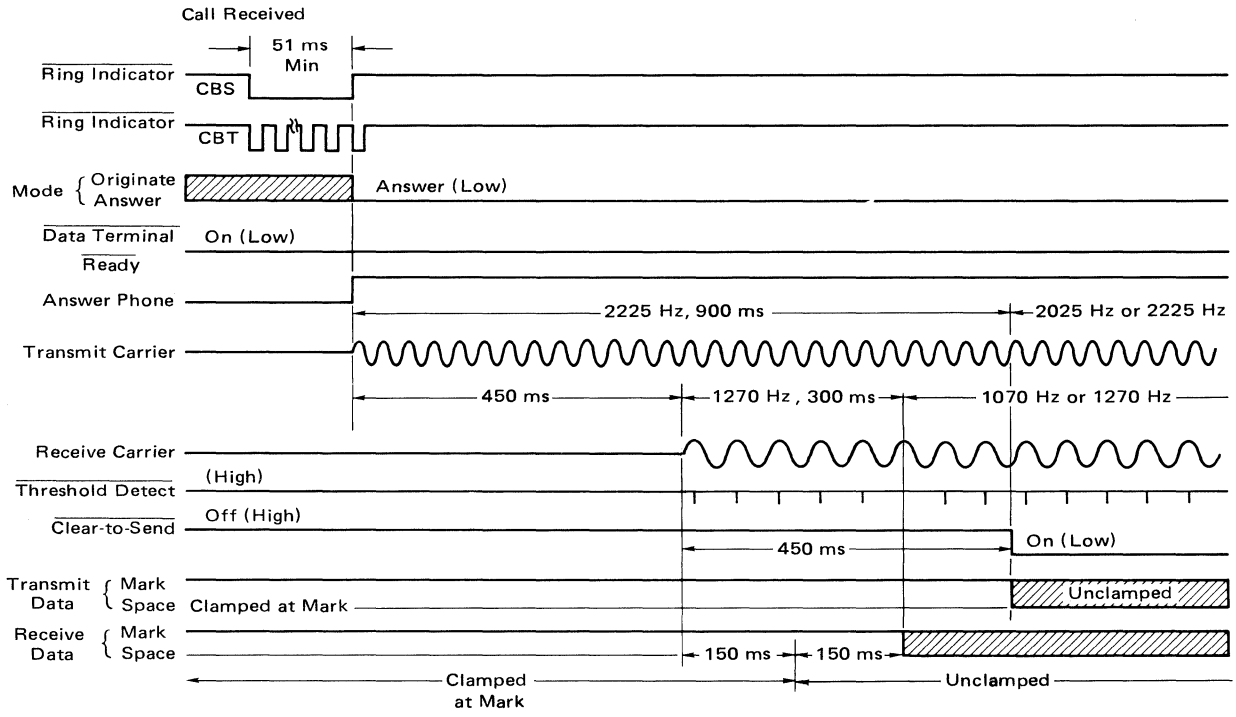


FIGURE 7 – AUTOMATIC DISCONNECT – LONG OR SHORT SPACE

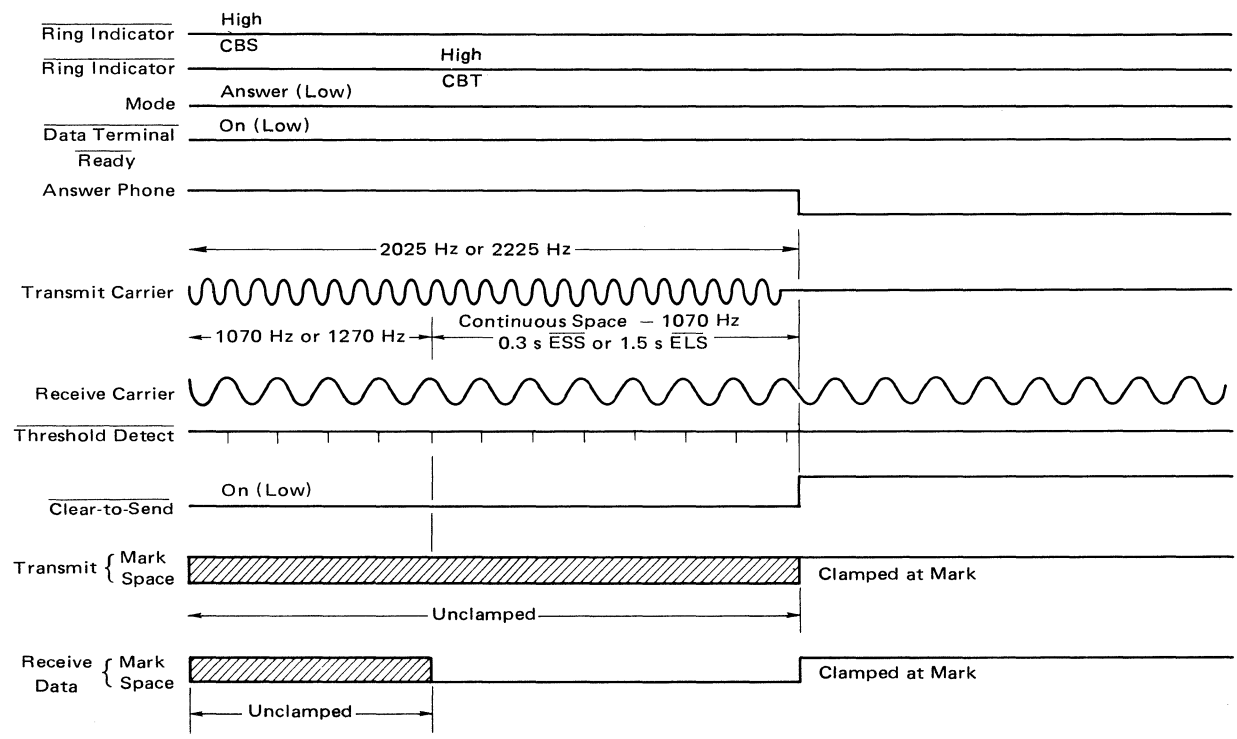


FIGURE 8 – ORIGINATE MODE

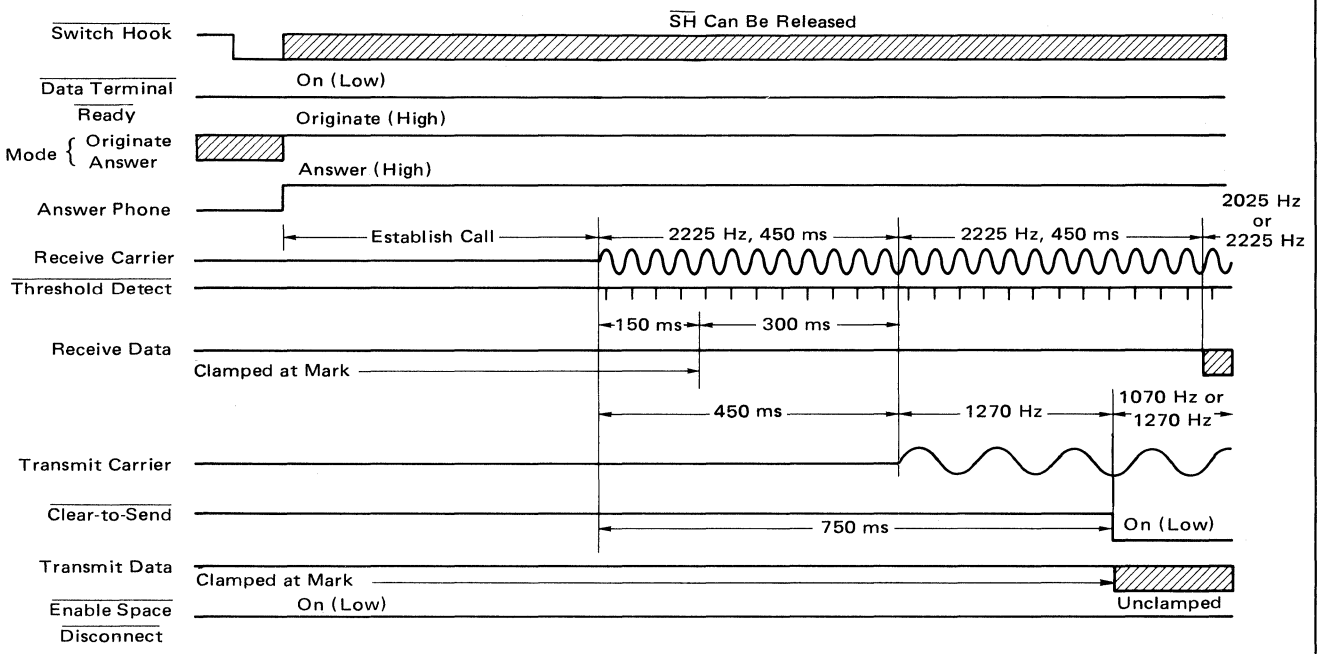


FIGURE 9 – INITIATE DISCONNECT

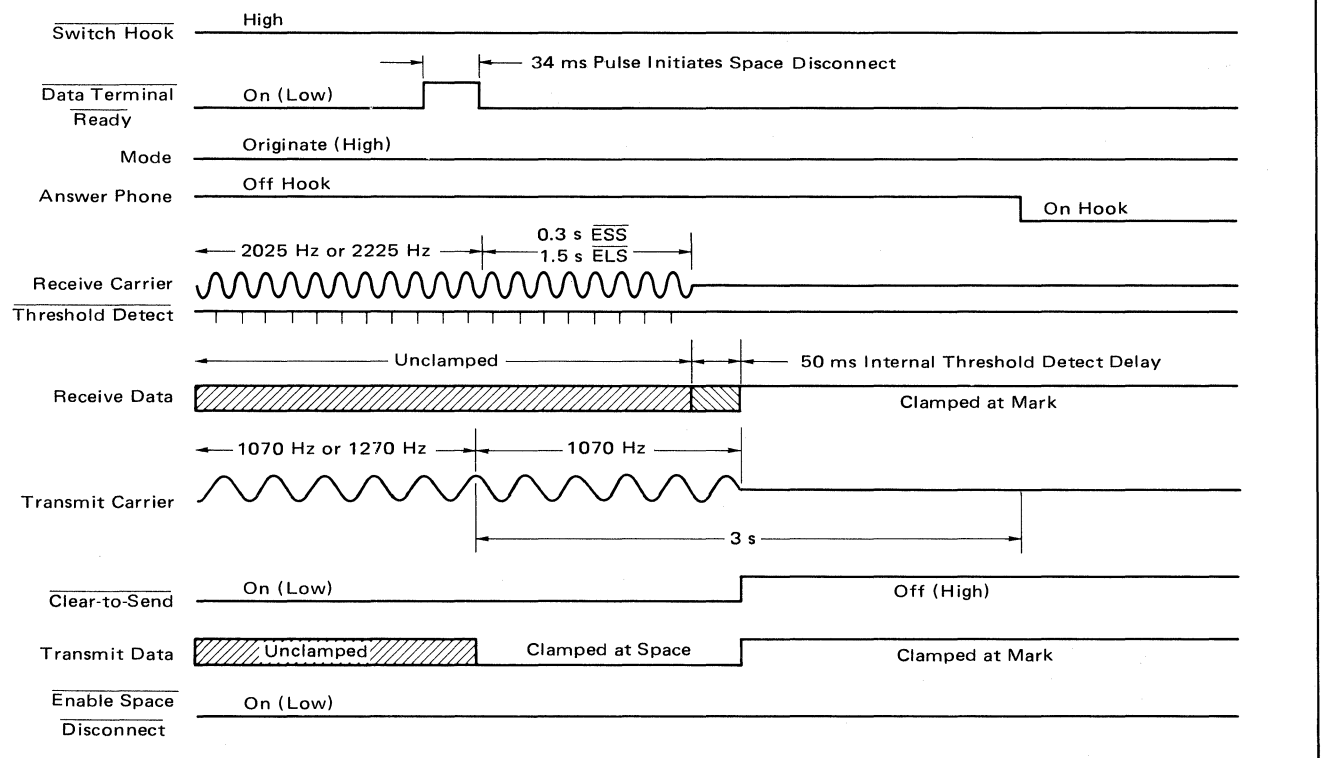
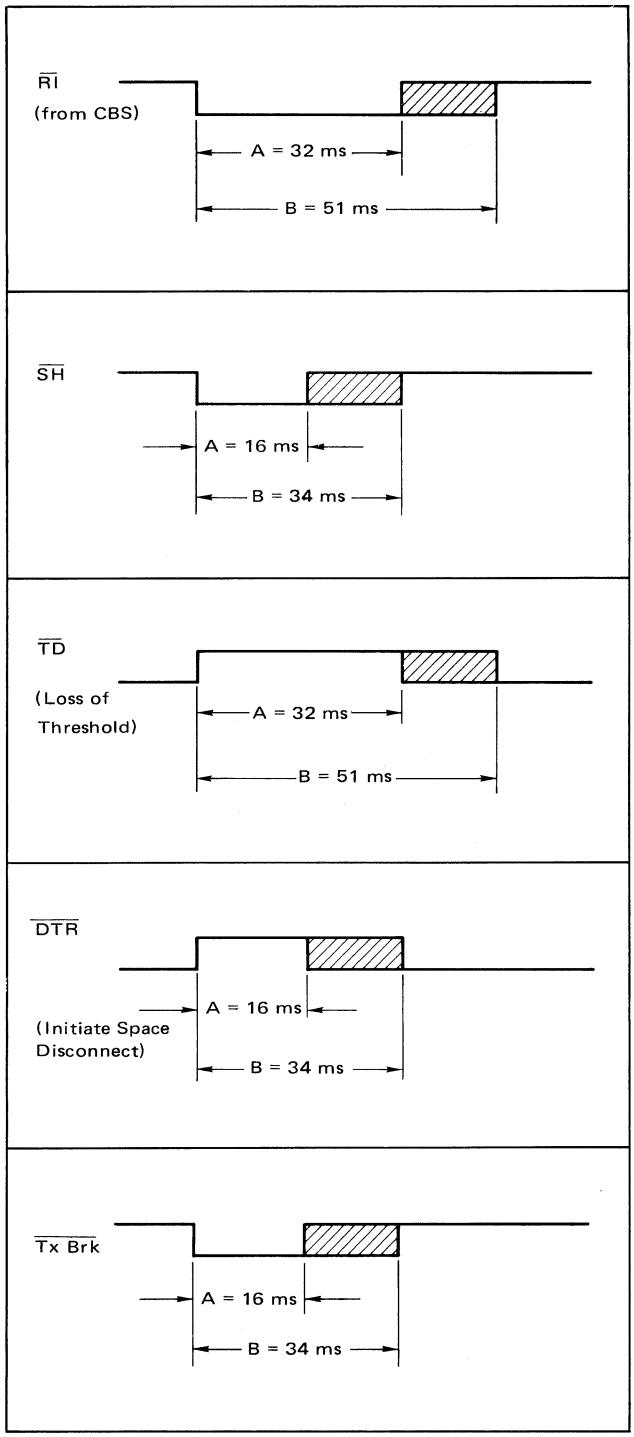


TABLE 1 – ASYNCHRONOUS INPUT PULSE WIDTH AND OUTPUT DELAY VARIATIONS
(Time delays specified do not include the 1-MHz reference tolerance.)

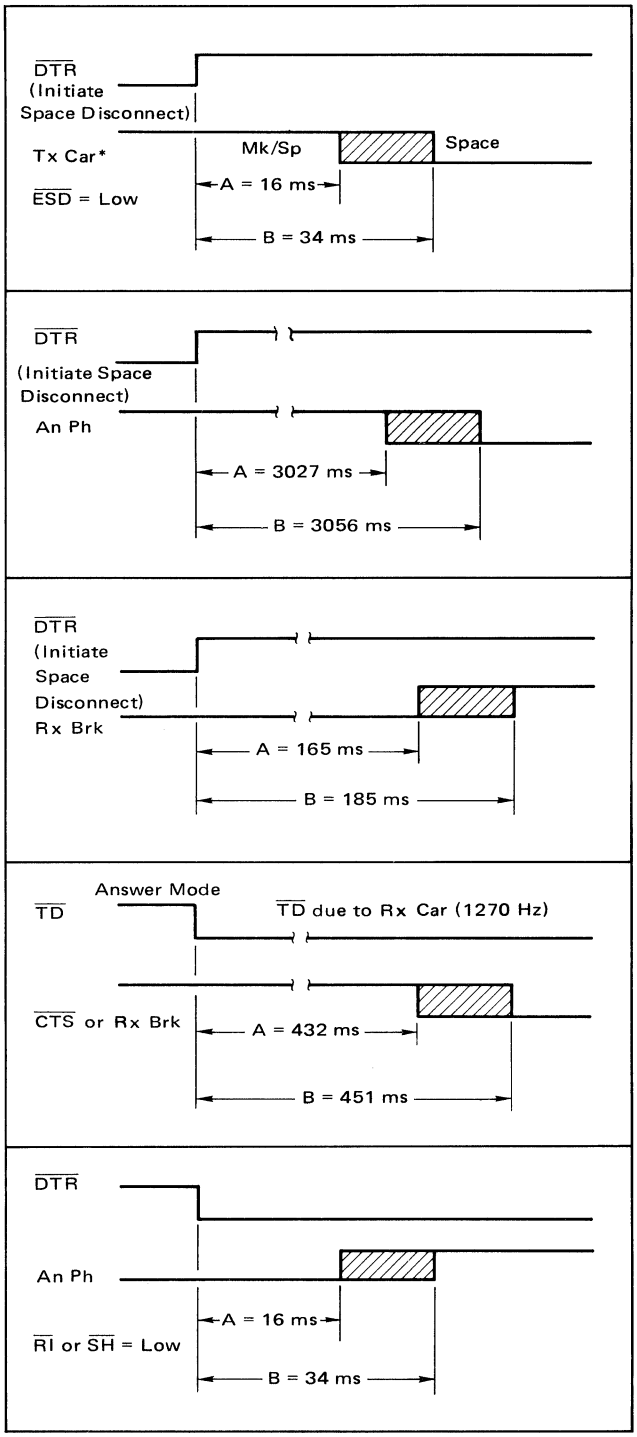
Due to the asynchronous nature of the input signals with respect to the circuit internal clock, a delay variation or input pulse width requirement will exist. Time delay A is the maximum time for which no response will occur. Time delay B is the minimum time required to guarantee an input response. Input signal widths in the cross-hatched region (i.e., greater than A but less than B) may or may not be recognized as valid.

For output delays, time A is the minimum delay before an output will respond. Time B is the maximum delay for an output to respond. Output signal response may or may not occur in the cross-hatched region (i.e., greater than A but less than B).

INPUT PULSES



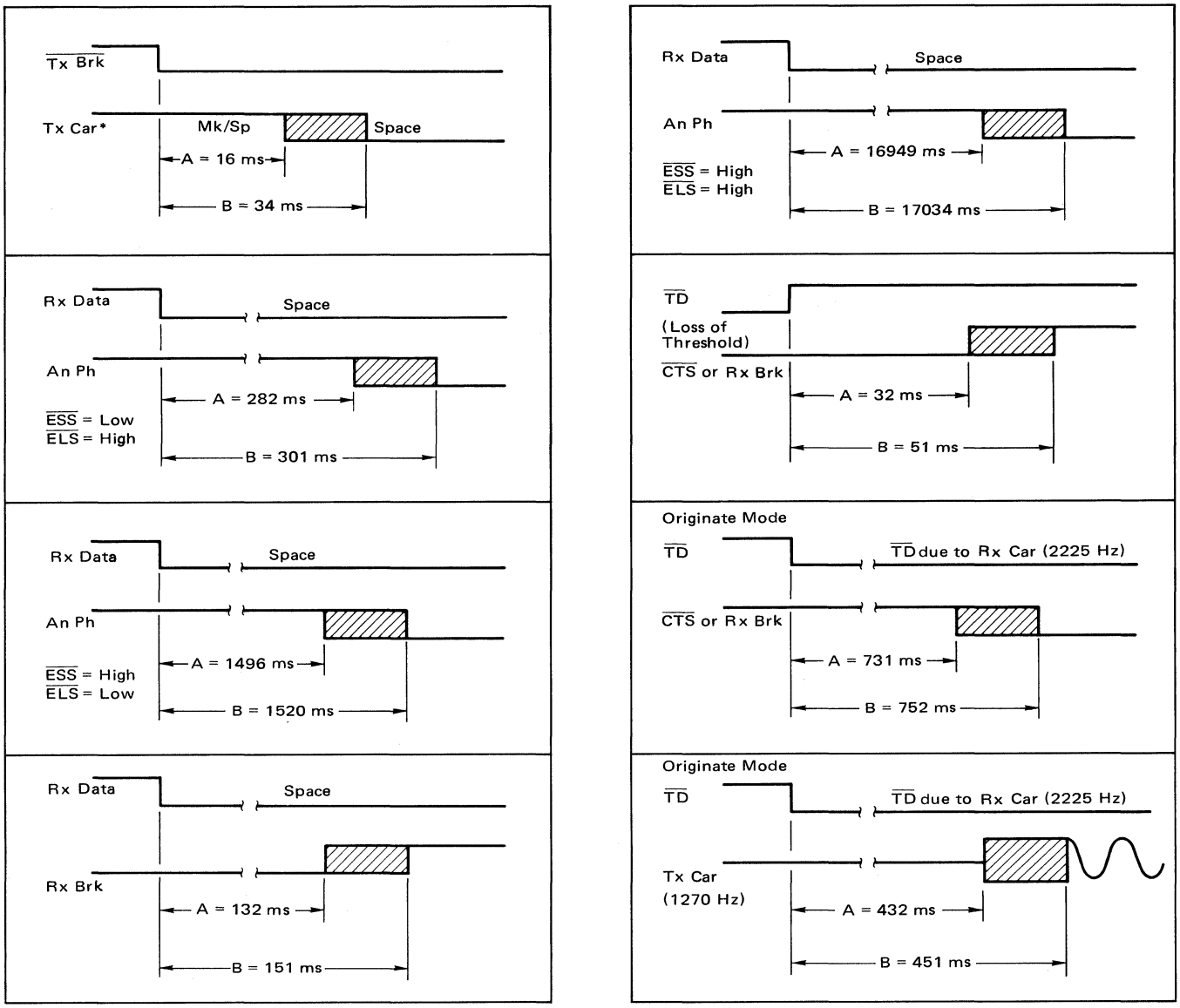
OUTPUT DELAYS



*Digital Representation.

(continued)

TABLE 1 – OUTPUT DELAY VARIATIONS (continued)

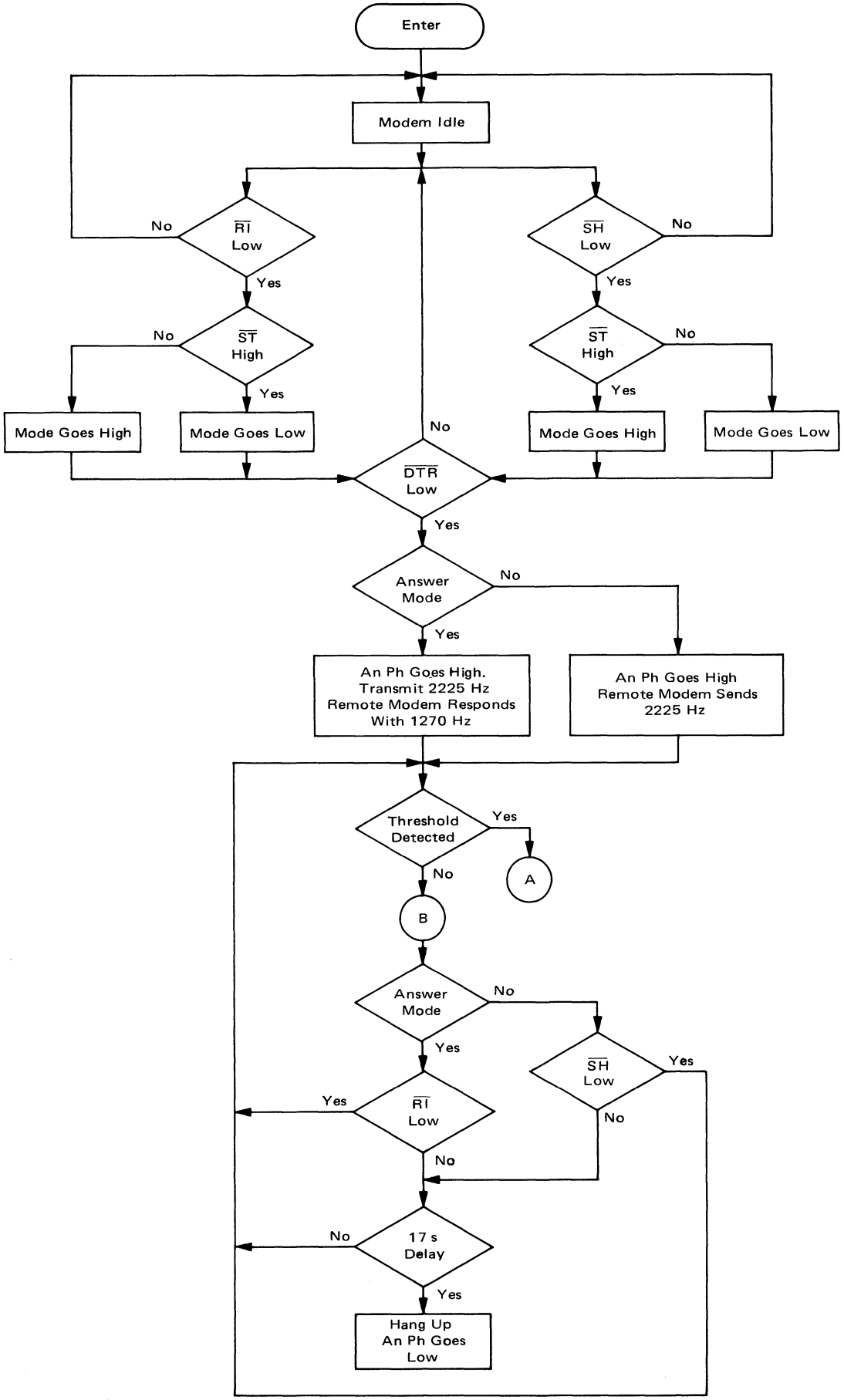


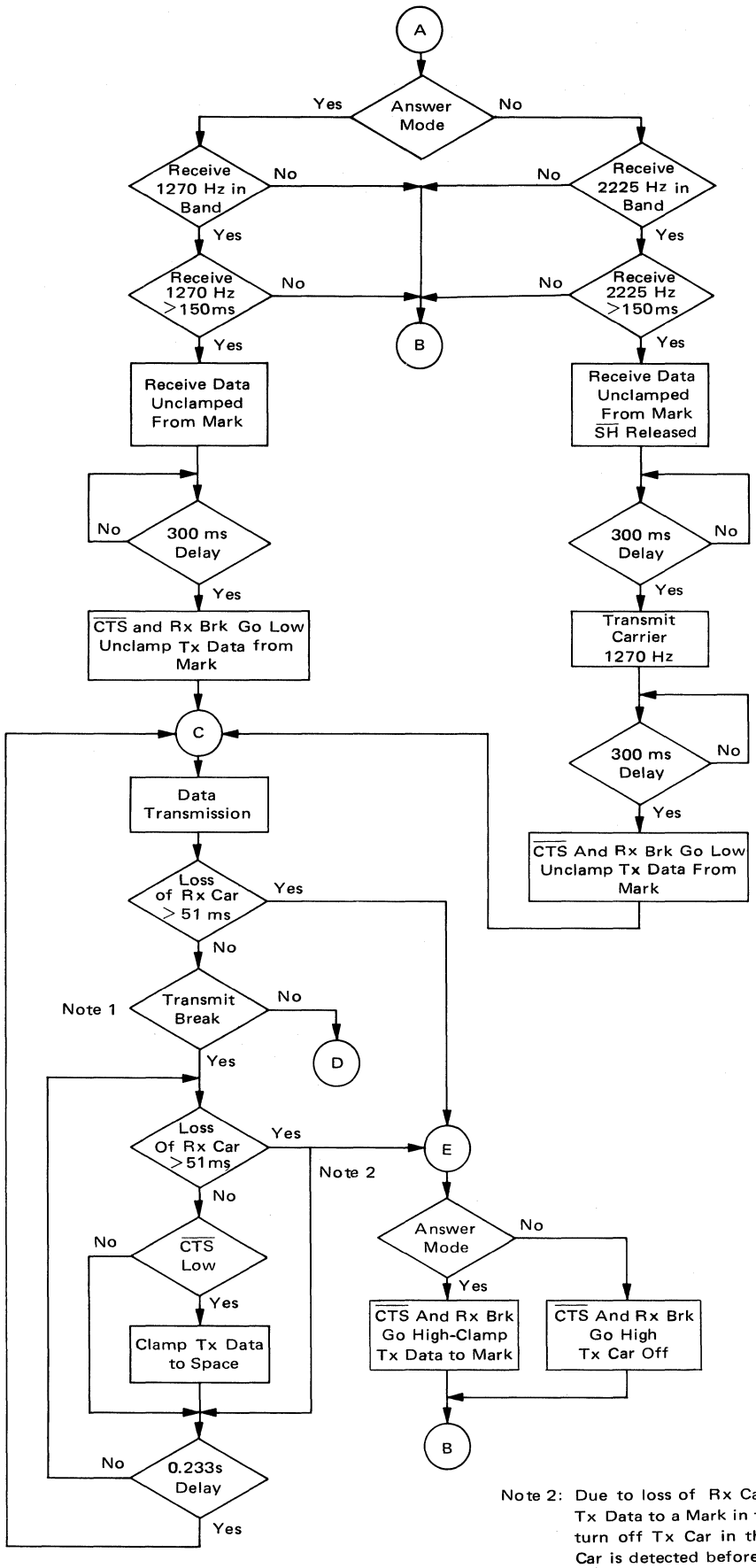
*Digital Representation

TABLE 2 – TRANSMIT BREAK AND DISCONNECT DELAYS

Function Description	Min	Max	Unit
$\overline{\text{Tx Brk}}$ (Space Duration)	232	235	ms
Space Disconnect (Space Duration) ($\overline{\text{DTR}}$ = High, $\overline{\text{ESD}}$ and $\overline{\text{TD}}$ = Low)	3010	3023	ms
Loss of Carrier Disconnect (Measured from positive edge of $\overline{\text{CTS}}$ to negative edge of An Ph, with $\overline{\text{RI}}$, $\overline{\text{SH}}$, and $\overline{\text{TD}}$ = High)	16965	17034	ms
Override Disconnect (Measured from positive edge of $\overline{\text{RI}}$ or $\overline{\text{SH}}$ to negative edge of An Ph, with $\overline{\text{TD}}$ = High)	16916	17101	ms

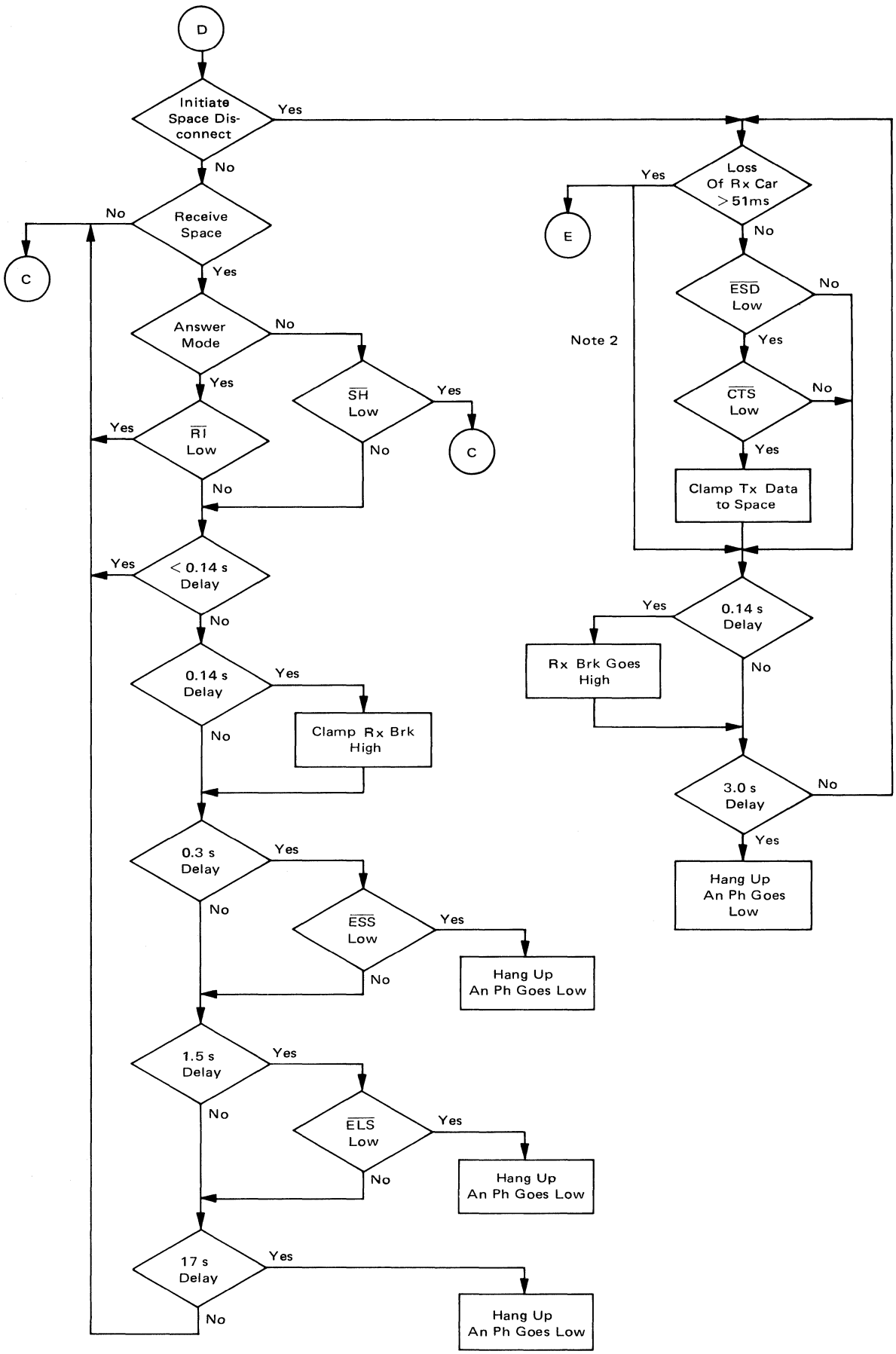
FIGURE 10 – FLOW DIAGRAM



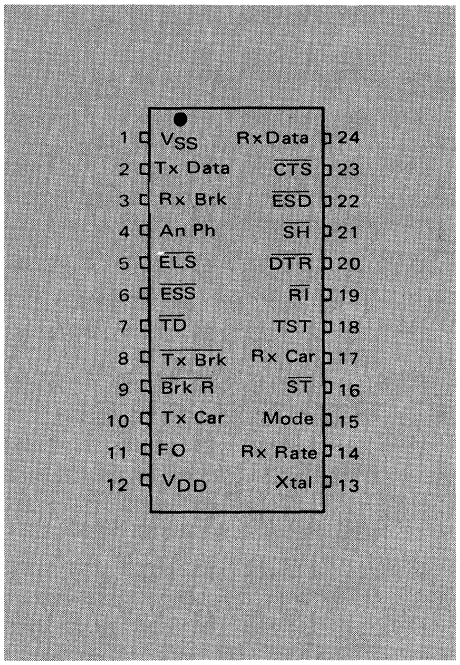


Note 1: Transmit Break, Initiate Space Disconnect, and Receive Space are mutually exclusive events.

Note 2: Due to loss of Rx Car, the modem will clamp Tx Data to a Mark in the Answer Mode and will turn off Tx Car in the Originate Mode. If Rx Car is detected before completion of Tx Brk or Initiate Space Disconnect, normal operation of Tx Brk or Initiate Space Disconnect will continue until completion of their respective time delays.


D
Initiate Space Disconnect
Yes
No
Receive Space
No
C
Yes
Answer Mode
No
Yes
SH Low
Yes
C
No
RI Low
Yes
No
< 0.14 s Delay
Yes
No
0.14 s Delay
Yes
Clamp Rx Brk High
No
0.3 s Delay
Yes
No
ESS Low
Yes
Hang Up An Ph Goes Low
No
1.5 s Delay
Yes
No
ELS Low
Yes
Hang Up An Ph Goes Low
No
17 s Delay
Yes
Hang Up An Ph Goes Low
No
Note 2
Loss Of Rx Car > 51ms
Yes
E
No
ESD Low
No
Yes
CTS Low
No
Yes
Clamp Tx Data to Space
0.14 s Delay
Yes
Rx Brk Goes High
No
3.0 s Delay
No
Yes
Hang Up An Ph Goes Low

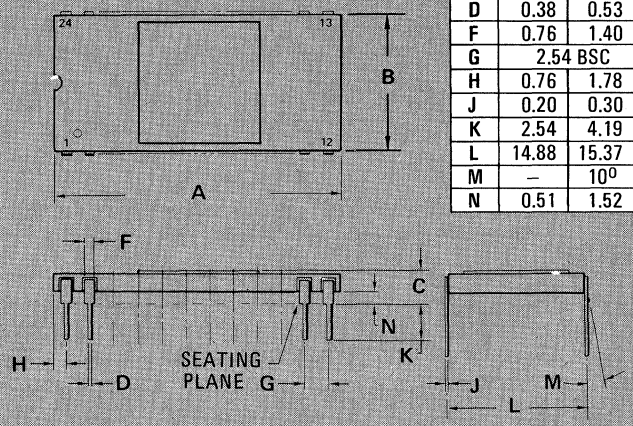
PIN ASSIGNMENT



PACKAGE DIMENSIONS

NOTE:
1. LEADS TRUE POSITIONED WITHIN 0.25mm (0.010) DIA (AT SEATING PLANE) AT MAXIMUM MATERIAL CONDITION.

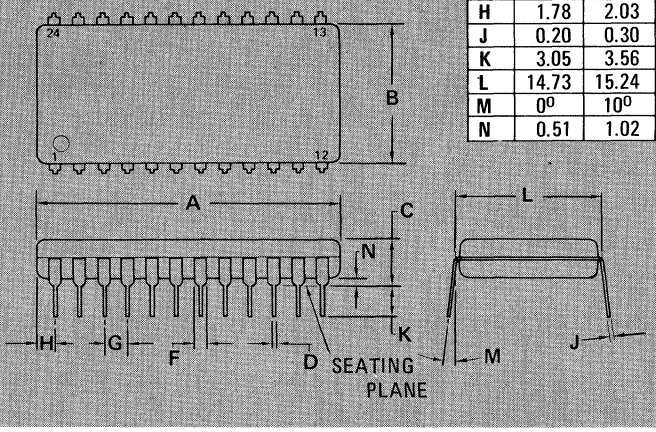
DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	29.97	30.99	1.180	1.220
B	14.88	15.62	0.585	0.615
C	3.05	4.19	0.120	0.165
D	0.38	0.53	0.015	0.021
F	0.76	1.40	0.030	0.055
G	2.54 BSC		0.100 BSC	
H	0.76	1.78	0.030	0.070
J	0.20	0.30	0.008	0.012
K	2.54	4.19	0.100	0.165
L	14.88	15.37	0.585	0.605
M	–	10^0	–	10^0
N	0.51	1.52	0.020	0.060



CASE 716-02
(CERAMIC)

NOTES:
1. LEADS, TRUE POSITIONED WITHIN 0.25 mm (0.010) DIA AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION. (DIM. "D")
2. DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	31.37	32.13	1.235	1.265
B	13.72	14.22	0.540	0.560
C	4.57	5.08	0.180	0.200
D	0.36	0.51	0.014	0.020
F	1.02	1.52	0.040	0.060
G	2.41	2.67	0.095	0.105
H	1.78	2.03	0.070	0.080
J	0.20	0.30	0.008	0.012
K	3.05	3.56	0.120	0.140
L	14.73	15.24	0.580	0.600
M	0^0	10^0	0^0	10^0
N	0.51	1.02	0.020	0.040



CASE 709-01
(PLASTIC)

MOTOROLA Semiconductors
BOX 20912 • PHOENIX, ARIZONA 85036

MC6862

(0 to 70°C; L or P Suffix)

MC6862C

(-40 to 85°C; L Suffix only)

Advance Information

MOS

(N-CHANNEL, SILICON-GATE)

2400 bps
MODULATOR

2400 bps DIGITAL MODULATOR

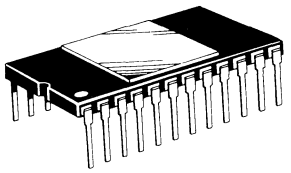
The MC6862 is a MOS subsystem designed to be integrated into a wide range of equipment utilizing serial data communication.

The modulator provides the necessary modulation and control functions to implement a serial data communication link over a voice grade channel, utilizing differential phase shift keying (DPSK) at bit rates of 1200 or 2400 bps. Phase options are provided for both the U.S. and international markets. The MC6862 can be implemented into a wide range of data handling systems, including stand-alone modems, data storage devices, remote data communication terminals, and I/O interfaces for counters.

N-channel silicon gate technology permits the MC6862 to operate using a single voltage supply and be fully TTL compatible.

The modulator is compatible with the M6800 microcomputer family, and provides medium-speed data communications capability.

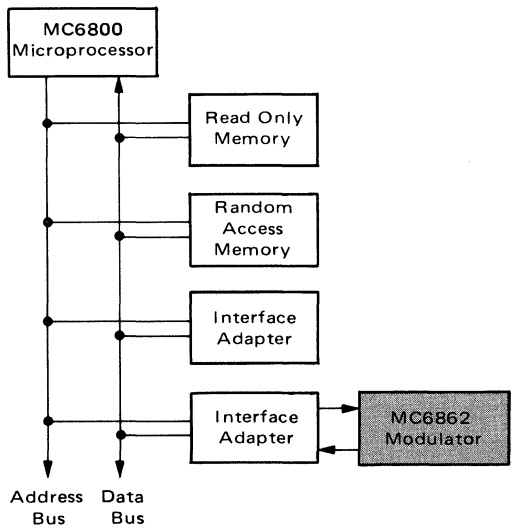
- Clear-to-Send Delay Options
- 511-Bit CCITT Test Pattern
- Terminal Interfaces Are TTL Compatible
- Compatible Functions for 201B/C Data Sets
- CCITT and U.S. Phase Options
- 1200/2400 bps Operation
- Answer Back Tone



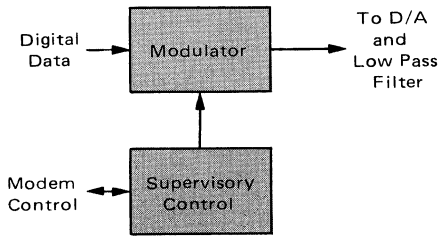
L SUFFIX
CERAMIC PACKAGE
CASE 716

NOT SHOWN: **P SUFFIX**
PLASTIC PACKAGE
CASE 709

M6800 MICROCOMPUTER FAMILY BLOCK DIAGRAM



MC6862 DIGITAL MODULATOR BLOCK DIAGRAM



MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.3 to +7.0	Vdc
Input Voltage	V_{in}	−0.3 to +7.0	Vdc
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	−55 to +150	°C
Thermal Resistance	θ_{JA}	82.5	°C/W

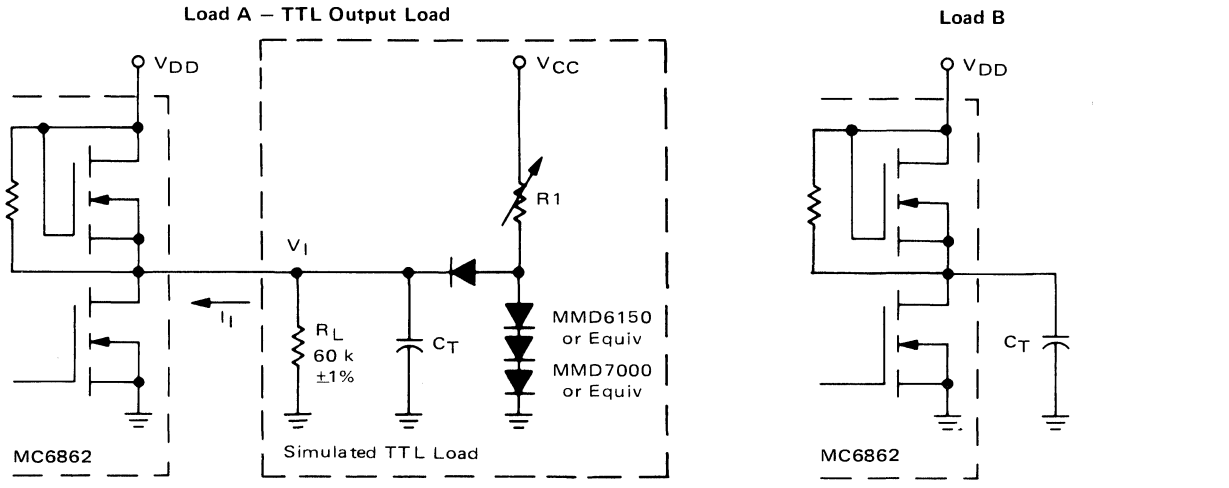
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

ELECTRICAL CHARACTERISTICS (V_{DD} = 5.0 ±0.25 Vdc, V_{SS} = 0, T_A = 0 to 70°C, all outputs loaded as shown in Figure 1 unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Input High Voltage	V_{IH}	V_{SS} + 2.0	–	V_{DD}	Vdc
Input Low Voltage	V_{IL}	V_{SS}	–	V_{SS} + 0.8	Vdc
Input Current (V_{in} = V_{SS}) CTS1, CTS2, PSS, DRS, $\overline{An\ Bk}$, and $\overline{Tx\ MK}$	I_{in}	–	–	-0.2	mAdc
$\overline{RTS}$ and $\overline{TPE}$		–	–	-1.6	
Input Leakage Current (V_{in} = 5.25 Vdc, V_{DD} = V_{SS})	I_{IL}	–	–	2.5	μAdc
Output High Voltage (I_{OH} = -0.04 mAdc, Load A)	V_{OH1}	V_{SS} + 2.4	–	V_{DD}	Vdc
(I_{OH} = 0.0 mAdc, Load B)	V_{OH2}	V_{DD}-0.5 V	–	V_{DD}	
Output Low Voltage (I_{OL} = 1.6 mAdc, Load A)	V_{OL}	V_{SS}	–	V_{SS} + 0.4	Vdc
Input Capacitance (f = 0.1 MHz, T_A = 25°C)	C_{in}	–	5.0	–	pF
V_{DD} Supply Current (All Inputs at V_{SS} except Pin 13 = 57.6 kHz and ALL Outputs Open)	I_{DD}	–	40	60	mAdc
Input Transition Times, All Inputs Except 1.8432 MHz Input (From 10% to 90% points)	t_r	–	–	1.0*	μs
	t_f	–	–	1.0*	
Input Transition Times, 1.8432 MHz Input (From 0.8 V to 2.0 V)	t_r	–	–	40	ns
	t_f	–	–	40	
Input Clock Duty Cycle, 1.8432 MHz Input (Measured at 1.5 V level)	D.C.	30	–	70	%
Tx Data Setup Time (Figure 2)	t_S	35	–	–	μs
Tx Data Hold Time (Figure 2)	t_H	35	–	–	μs
Output Transition Times (From 10% to 90% Points)	t_r	–	–	5.0	μs
	t_f	–	–	5.0	

*Maximum Input Transition Times are ≤ 0.1 x Pulse Width or the specified maximum of 1.0 μs, whichever is smaller.

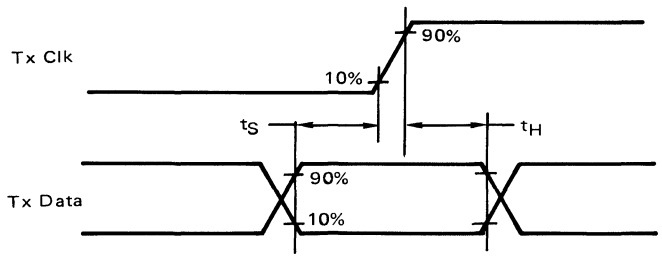
FIGURE 1 – OUTPUT TEST LOADS



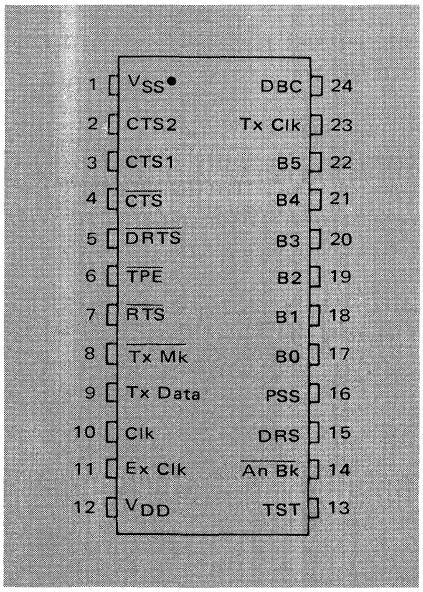
R1 is adjusted for I_I = 1.6 mA at V_I = 0.4 V when output node is disconnected.

C_T = 20 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances

FIGURE 2 – TRANSMIT DATA SETUP AND HOLD TIME

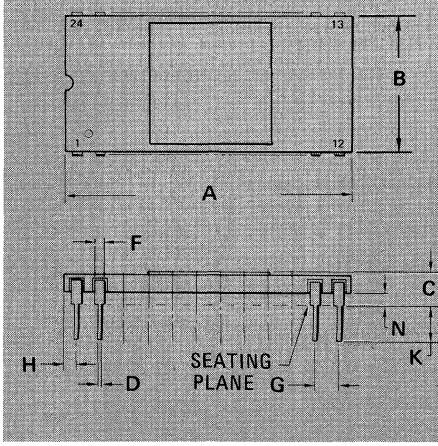


PIN ASSIGNMENT



PACKAGE DIMENSIONS

NOTE:
1. LEADS TRUE POSITIONED WITHIN 0.25mm (0.010) DIA (AT SEATING PLANE) AT MAXIMUM MATERIAL CONDITION.

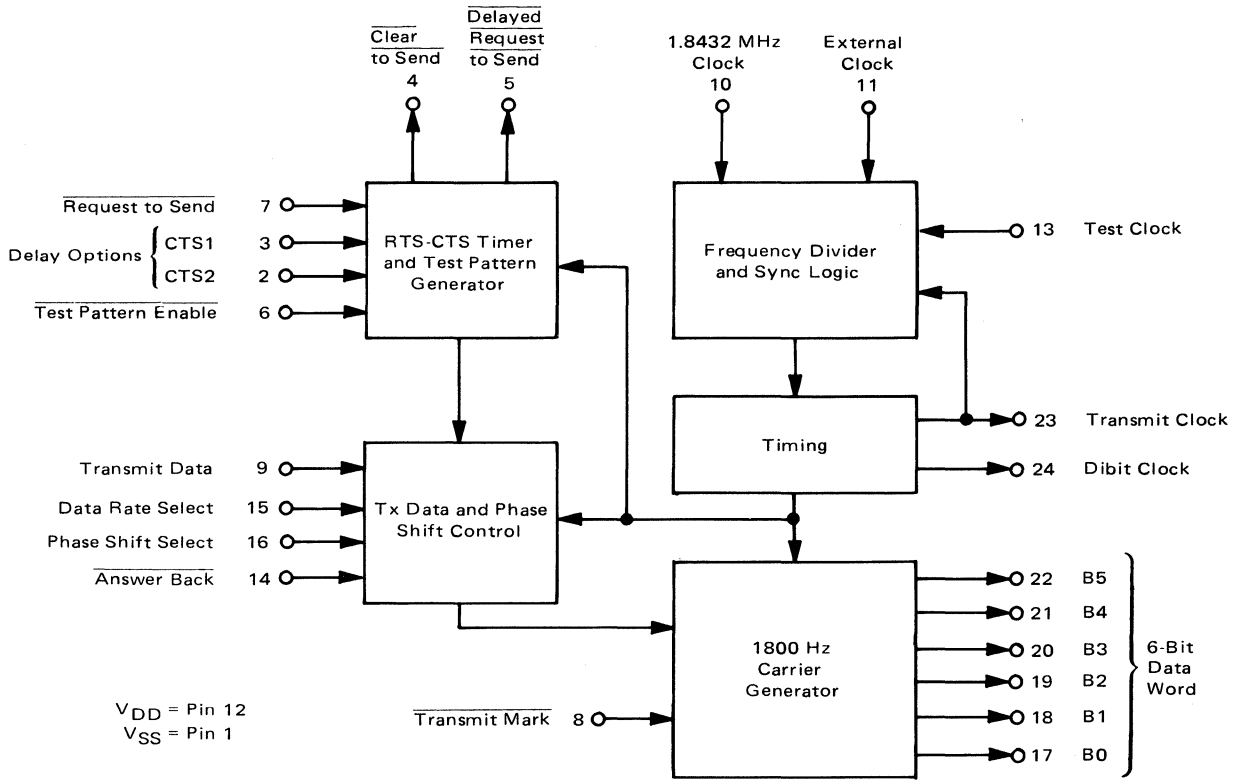


	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	29.97	30.99	1.180	1.220
B	14.88	15.62	0.585	0.615
C	3.05	4.19	0.120	0.165
D	0.38	0.53	0.015	0.021
F	0.76	1.40	0.030	0.055
G	2.54 BSC		0.100 BSC	
H	0.76	1.78	0.030	0.070
J	0.20	0.30	0.008	0.012
K	2.54	4.19	0.100	0.165
L	14.88	15.37	0.585	0.605
M	–	10^0	–	10^0
N	0.51	1.52	0.020	0.060

CASE 716-02
(CERAMIC)

SEE PAGE 165 FOR PLASTIC PACKAGE DIMENSIONS

BLOCK DIAGRAM



DEVICE OPERATION

GENERAL

Figure 3 shows the modulator and its intraconnections. The data to be transmitted is presented in synchronous serial format to the modulator for conversion to DPSK signals used in transmission. The modulator output is digital; therefore, a D/A converter and a filter transform the signal to an analog form.

The control functions provide four different Clear-to-Send delay options. An Answer Back tone is available for automatic answering applications. The modulator has a built-in 511-bit pseudorandom pattern generator for use in system diagnostic tests.

INPUT/OUTPUT FUNCTIONS

Request to Send ($\overline{RTS}$)

The $\overline{RTS}$ signal from the data terminal controls transmission from the modulator. A low level on $\overline{RTS}$ activates the modulator data output. A constant mark, for synchronization, is sent during the $\overline{RTS}$ to $\overline{CTS}$ delay interval. Termination of the transmission is accomplished by taking $\overline{RTS}$ high (see Figures 4 and 5).

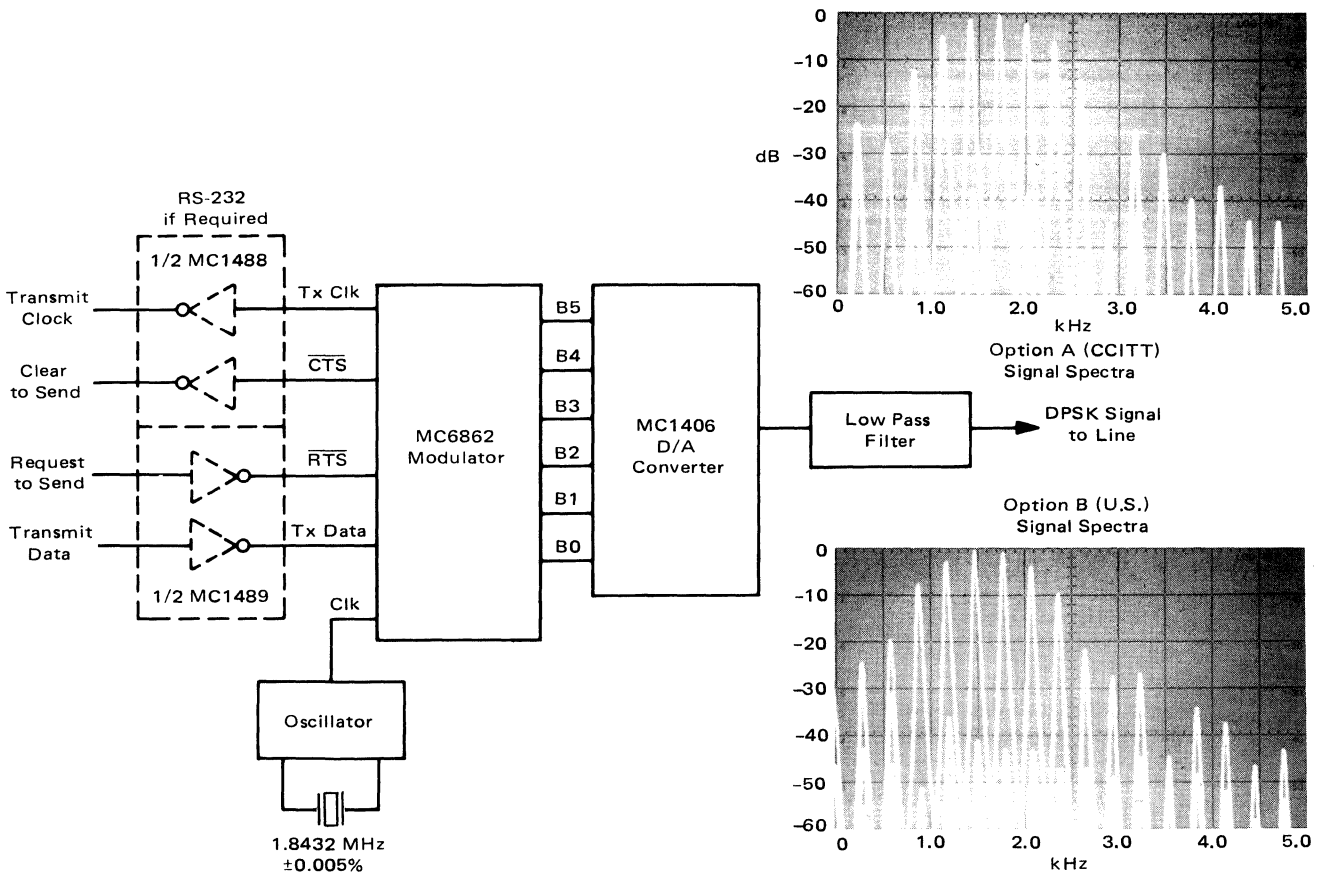
Delayed Request to Send ($\overline{DRTS}$)

This output can be used to control transmission as specified by the $\overline{Transmit\ Mark}$ control input. $\overline{DRTS}$ follows the negative transition of $\overline{RTS}$, and goes negative within the 35 μs of the negative transition of $\overline{RTS}$ (Figure 4). The delay from a positive transition of $\overline{RTS}$ to a positive transition of $\overline{DRTS}$ is shown in Figure 5. The $\overline{DRTS}$ delay allows data within the modulator to be transmitted before transmission is inhibited.

Clear to Send ($\overline{CTS}$)

$\overline{CTS}$ follows $\overline{RTS}$ to both the logic 0 and logic 1 levels. The delay from a negative transition of $\overline{RTS}$ to a negative $\overline{CTS}$ transition is selectable by external strapping of CTS1 and CTS2. The delay from a positive transition of $\overline{RTS}$ to a positive $\overline{CTS}$ transition is less than 35 μs.

FIGURE 3 – 2400 BPS MODULATOR INTERFACE



$\overline{\text{CTS}}$ will go low within 35 μs after the positive transition of the Dibit Clock (see Figure 4) except when the no-delay option is selected. For the no-delay option, $\overline{\text{CTS}}$ follows $\overline{\text{RTS}}$ within 35 μs.

$\overline{\text{RTS}}$-$\overline{\text{CTS}}$ Delay Options (CTS1,CTS2)

The $\overline{\text{RST}}$-$\overline{\text{CTS}}$ delays are selectable according to the following strapping options.

$\overline{\text{RTS}}$-$\overline{\text{CTS}}$ Delay	CTS1	CTS2
0.0 + 0.035 ms, -0.0 ms	0	1
8.55 to 9.35 ms	1	0
24.90 to 26.4 ms	1	1
147.0 to 154.0 ms	0	0

$\overline{\text{Transmit Mark}}$ ($\overline{\text{Tx Mk}}$)

The $\overline{\text{Transmit Mark}}$ control allows the system designer to select whether the $\overline{\text{Delayed Request to Send}}$ activates and deactivates the transmission on the modulator chip or off the chip in the output amplifier.

When $\overline{\text{Tx Mk}}$ is high, transmission is controlled on the modulator chip, and occurs from the chip only when $\overline{\text{DRTS}}$ or $\overline{\text{Answer Back}}$ is in the logic 0 state (see Figure 6).

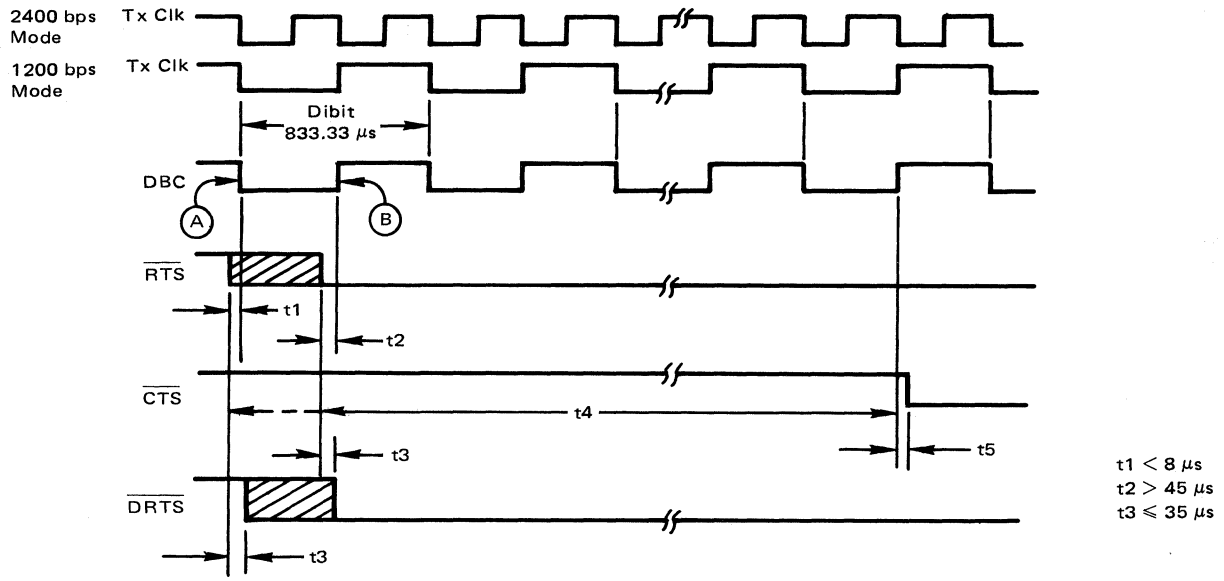
When $\overline{\text{Tx Mk}}$ is low, transmission is controlled off the modulator chip. In this mode, the modulator chip transmits marks at all times except when data or an $\overline{\text{Answer Back}}$ tone is being transmitted (see Figure 6).

$\overline{\text{Test Pattern Enable}}$ ($\overline{\text{TPE}}$)

A 511-bit test pattern generator is contained on the modulator chip. This pattern is in accord with CCITT specification V52. The pattern can be used to scramble input data, or as a test pattern.

The 511-bit test pattern is activated by applying a logic 0 to $\overline{\text{TPE}}$. A mark (logic 1) condition on the Transmit Data input with $\overline{\text{TPE}}$ activated (logic 0) causes the test pattern to appear at the data output. A space

FIGURE 4 – $\overline{RTS}$-$\overline{CTS}$ AND $\overline{RTS}$-$\overline{DRTS}$ DELAYS



CTS1	CTS2	t4*	t5
0	1	$0.0^{+0.035\ ms}_{-0.0\ ms}$	–
1	0	8.55 to 9.35 ms	< 35 μs
1	1	24.90 to 26.4 ms	< 35 μs
0	0	147.0 to 154.0 ms	< 35 μs

*The reference frequency tolerance is not included.

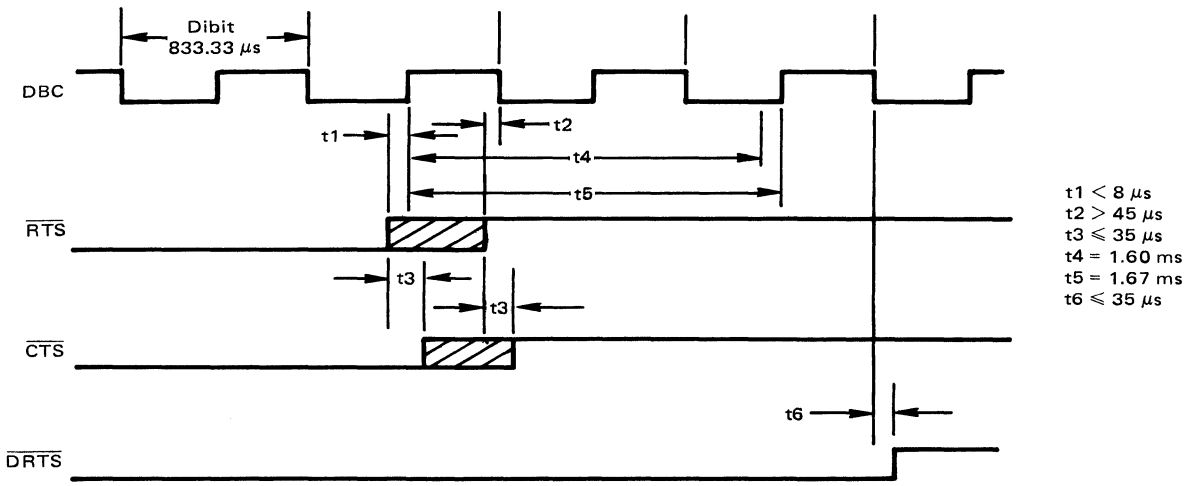
$\overline{RTS}$-$\overline{CTS}$ delay options are selected by the CTS1 and CTS2 inputs, and are stated as time delay interval t4. An $\overline{RTS}$ input signal synchronized about point A as shown and going low within the shaded region, will synchronize $\overline{CTS}$ with the positive transition of DBC (Dibit Clock), and delay t4 is measured with respect to the negative transition of $\overline{RTS}$.

$\overline{RTS}$ signals going low within the shaded region, but synchronized with the positive transition of DBC (point B), will result in the same $\overline{CTS}$ delay (t4). For this case the negative transition of $\overline{CTS}$ is synchronized with the negative transition of DBC with delay t4 measured with respect to the negative transition of $\overline{RTS}$.

$\overline{DRTS}$ will go low within 35 μs of the negative transition of $\overline{RTS}$ (shown as time t3). With the exception of the no-delay option, $\overline{CTS}$ will go low within 35 μs (t5) of the positive transition of DBC, following the t4 delay selected. This applies when $\overline{RTS}$ is synchronized to Point A as shown.

If $\overline{RTS}$ goes high and remains high $\geqslant$ 20 μs within time interval t4, a reset of the internal $\overline{RTS}$-$\overline{CTS}$ timer function will occur. If $\overline{RTS}$ goes high for less than 20 μs, the circuit may or may not respond to this momentary loss of the $\overline{RTS}$ signal.

FIGURE 5 – LOSS OF $\overline{RTS}$ TO $\overline{DRTS}$ DELAY



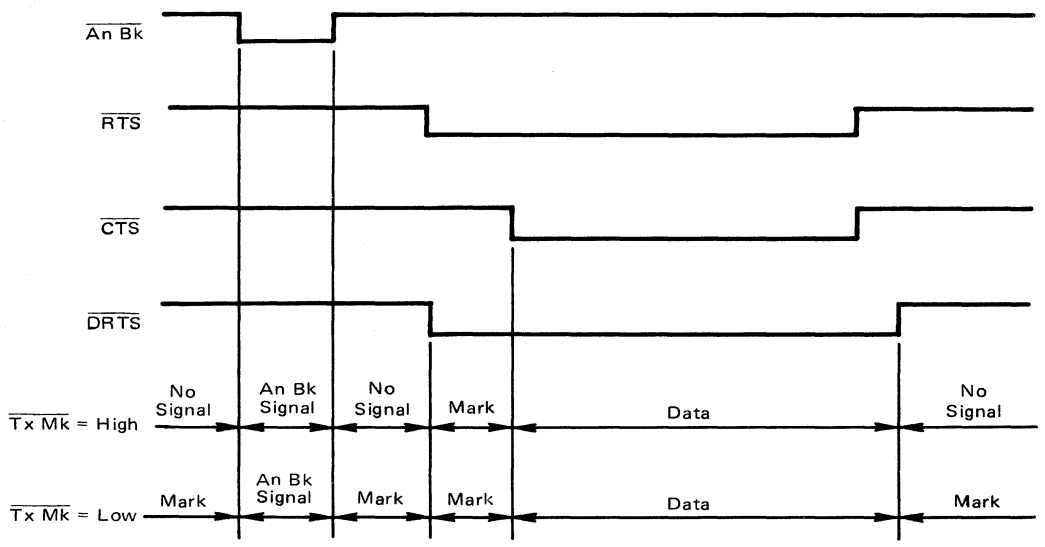
A positive transition of $\overline{RTS}$ after $\overline{CTS}$ has become active can result in different functional characteristics of the $\overline{CTS}$ and $\overline{DRTS}$ output signals, depending on the time duration that $\overline{RTS}$ remains inactive.

Under all conditions, $\overline{CTS}$ will go high within 35 µs (t3) following a positive transition of $\overline{RTS}$. If $\overline{RTS}$ goes high in the shaded region shown (i.e., synchronized to the positive transition of DBC) and remains high beyond the time interval defined as t5, then $\overline{DRTS}$ will go high within 35 µs (t6) of the next negative transition of DBC.

If $\overline{RTS}$ were to go low after t5, the $\overline{RTS}$-$\overline{CTS}$ delay times given in Figure 4 will result.

If $\overline{RTS}$ goes high in the shaded region shown, and then returns low within time interval t4, the negative transition of $\overline{CTS}$ will follow within 35 µs, and DRTS will remain in the active or low state. Under these conditions, the normal $\overline{RTS}$-$\overline{CTS}$ delay times are not encountered when $\overline{RTS}$ is reactivated. If $\overline{RTS}$ goes low for less than 20 µs, the circuit may or may not respond to this momentary $\overline{RTS}$ input signal.

FIGURE 6 – TRANSMIT MARK CONTROL



(logic 0) condition on Tx Data with $\overline{TPE}$ activated causes the test pattern data to appear inverted at the data output. Random data applied to Tx Data with $\overline{TPE}$ activated causes the test pattern data to be scrambled (exclusive NORed) with the data, and the result appears at the data output.

The test pattern generator can be enabled only when $\overline{CTS}$ and $\overline{RTS}$ are logic 0. If $\overline{TPE}$ is activated outside this time interval, the previously stated $\overline{RTS}$-$\overline{CTS}$ and $\overline{RTS}$-$\overline{DRTS}$ delays shown in Figures 4 and 5 are not valid.

Data Rate Select (DRS)

The modulator can transmit at either 2400 bps or 1200 bps. Both data rates utilize an 1800 Hz carrier signal and employ phase shifting at 1200 Hz. The 2400 bps rate is obtained by encoding two bits of data into each phase shift. The 2400 Hz rate is selected by applying a logic 1 to the Data Rate Select lead. The 1200 Hz rate is selected by applying a logic 0 to DRS.

Phase Shift Select (PSS)

Option A (CCITT) or Option B (U.S.) phase shift can be selected for 2400 bps operation. The input data format and phase shift relationship for these two options are as follows:

Data	PSS = 0 Option A	PSS = 1 Option B
00	0^o	$+45^o$
01	$+90^o$	$+135^o$
11	$+180^o$	$+225^o$
10	$+270^o$	$+315^o$

For 1200 bps operation, Option C (CCITT) or Option D (U.S.) phase shift can be selected:

Data	PSS = 0 Option C	PSS = 1 Option D
0	$+90^o$	$+45^o$
1	$+270^o$	$+225^o$

Option C is selected by applying a logic 0 to the Phase Shift Select lead when the Data Rate Select lead is strapped for 1200 bps operation (logic 0). Option D is selected by applying a logic 1 to PSS with DRS at logic 0. The phase shifts shown are the difference in phase between the signal at the end of one dibit period and the new signal at the beginning of the next dibit.

Transmit Data (Tx Data)

Transmit Data is the serial binary information presented for DPSK modulation. A high level represents a mark. For timing, see Transmit Clock (Figure 4).

Transmit Clock (Tx Clk)

A 2400/1200 Hz Transmit Clock output is provided for the communication terminal. The Transmit Data signal is sampled on the positive transition of Transmit Clock. The Transmit Data to Transmit Clock setup and hold time requirements are shown in the Electrical Characteristics table and in Figure 2.

Dibit Clock (DBC)

A 1200 Hz Dibit Clock identifies the modulation timing. This signal goes negative less than 100 μs prior to the start of dibit modulation.

External Clock (Ex Clk)

A 2400/1200 Hz clock signal applied to the External Clock lead causes Transmit Clock to be synchronized with Ex Clk. This input must have an accuracy within ±0.005%.

When no transitions occur on this input, the internal clock provides the 2400/1200 Hz transmit timing signal. Fast synchronization of Tx Clk to Ex Clk is not provided on the chip. *When Ex Clk is not used it should be tied to either the logic 0 or logic 1 state.*

1.8432 MHz (Clk)

This input must be a square wave with rise and fall times of less than 40 ns and a 50 ±20% duty cycle. The clock accuracy must be within ±0.005%.

$\overline{\text{Answer Back}}$ ($\overline{\text{An Bk}}$)

A logic 0 level applied to $\overline{\text{Answer Back}}$ causes a 2025 Hz carrier to be generated on the modulator chip instead of a phase shifted 1800 Hz carrier. A logic 1 level applied to $\overline{\text{An Bk}}$ enables the modulator to generate the normal phase shifted 1800 Hz carrier signal, as shown in Figure 6. The time delay from a transition on $\overline{\text{An Bk}}$ to the appropriate signal at the modulator chip output is less than 2 ms.

Activation of $\overline{\text{An Bk}}$ (a logic 0) will disable all other operation modes including the $\overline{\text{Tx Mk}}$ function, and will reset $\overline{CTS}$ to an inactive state along with the $\overline{RTS}$-$\overline{CTS}$ internal timer. $\overline{\text{An Bk}}$ should therefore be activated only before initiating $\overline{RTS}$ or after loss of the $\overline{DRTS}$ output signal. The combination of a logic 0 on $\overline{\text{An Bk}}$ with a logic 0 on $\overline{TPE}$ is not used in normal system operation, and hence is used as a reset input during device test.

Digital Output (B0-B5)

These outputs are designed to interface with a six-bit digital-to-analog converter. The resultant signal out of the D/A is the differential phase shift keyed signal quantized at a 14.4 kHz rate. A low pass filter can then be used to smooth the data transitions. B0 is the least significant bit, and the positive level the active state.

Test Clock (TST)

A test signal input is provided to decrease test time of the chip. *In normal operation this input must be strapped low.*

MOTOROLA INC.
COMPONENT PRODUCTS DEPT.

MC6870, MC6871 series

Two-Phase Microprocessor Clocks
Designed to drive the Motorola MC6800 MPU

The *Functional Module* approach to data communications hardware design significantly decreases the time between the "idea" stage and the marketable product.

A fundamental building block in a modular microcomputer system is the 2-phase clock oscillator used to drive the microprocessor. Motorola is uniquely qualified to provide this building block because of expertise in the three relevant fields: oscillator design, quartz crystal technology, and thick film hybrid integrated circuit manufacturing.

This one-of-a-kind expertise has created several clocks designed to drive Motorola's MC6800 Microprocessor. This plug-in unit contains the crystal, the oscillator circuit, the NMOS and TTL drivers, and the waveshaping and interface circuitry; all the components necessary to provide the critical non-overlapping 2-phase waveforms used by the MC6800 MPU.

FEATURES

Clock Module—Each clock module requires only a single 5 volt power supply. The NMOS outputs can drive highly capacitive loads ranging from 80 pf to 160 pf and meet all MPU input waveshape and timing requirements.

Each TTL output signal leads the ϕ_2 NMOS so that additional system device delays can be accommodated. All TTL outputs are buffered so they can drive 5 TTL devices and maintain all output specifications.

Each module is crystal-controlled and is compensated for variations in temperature, voltage, and load. The standard frequency of each model is 1 MHz; however, other frequencies between 250 kHz and 2.5 MHz can be ordered.

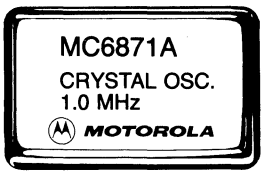
Reliability—Decreased Component Count—Thick film hybrids offer a reliability advantage that comes primarily from reduced component count and therefore reduced interconnections. Further, the single hermetic seal on the hybrid package reduces the failure rate whereas in a discrete design a separate sealing process with an associated failure rate is needed for each component.

High Density Packaging—The hybrid MPU clock allows compact microcomputer design. It takes up only 1.34″x .840″ space and has a seated height of .200″.

Ruggedized Design—Maximum reliability at minimum cost is the result of combining three of Motorola's fields of experience: quartz crystal technology, clock oscillator design, and thick film hybrid integrated circuit manufacturing. Mass automated production techniques assure volume production. Gold plating of all crystals and Class 100 clean room processing testify that no short cuts are taken that might diminish reliability. Environmental testing proves the effectiveness of the rugged design for those applications in which shock and vibration are likely hazards.

Complete Process Control—Motorola is the only totally integrated manufacturer of quartz frequency control devices; full control of all processes from growing, sawing, lapping, and finishing quartz to combining it with other components into an electronic product—the MC6870A, MC6871A, and MC6871B MPU clocks.

Volume Production—Production facilities are oriented to mass automated production techniques. And, if required, capital for expansion is available to meet even greater requirements.



actual size

environmental specifications

Temperature Cycle: ±5 ppm max., 0 to 120°C, 3 cycles, 2 hrs. max. each, 25 ±2°C ref.

Shock: 1000G's 0.35 millisec, ½ sine wave, 3 shocks each plane

Vibration: 10-55 Hz, .060″ D.A.; 55-2000Hz, 35 G's. Duration Time—12 Hours

Humidity: 85% Rel. Humidity, @ +85°C, 250 Hours

mechanical specifications

Gross Leak Test: All units 100% leak tested in de-ionized H_2O.

Hermetic Sealed Package: Mass spectrometer leak rate less than 2 x 10^{-8} atmos. cc/sec. of helium.

Seal Strengh: 20 lbs. max. force perpendicular to top and bottom.

Pin Material: Phosphor bronze, ¼ hard, Grade A .00003″ thick gold flash finish.

Bend Test: Will withstand maximum bend of 90° reference to base for 1 bend.

Marking Ink: Epoxy, heat cured.

Solvent Resistance: Isopropyl Alcohol Tricholoroethane Freon TMC. No marking or seal destruction. Dipped 1 minute @ +25°C ±5°C in solvent.

Note: (1) Unit can be cleaned by only one type solvent listed.

Note: (2) Ultrasonic degreaser not to be used unless frequency and vibration of cleaner specified.

solderability specifications

Materials:

1.1 Solder: 60% tin and 40% lead.

1.2 Flux: The flux shall be 25 percent by weight of Grade WW rosin and 75 percent by weight of 99 percent isopropyl alcohol.

Procedure:

2.1 Solder Bath: The solder bath shall be maintained at 232 ±6°C.

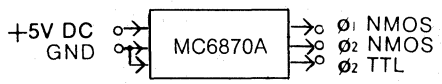
2.2 Solderability: Dip the terminals into the flux to the depth that is to be soldered or to a maximum depth of .025″ from the body of the oscillator. Keep them in the flux for at least 5 seconds. Withdraw them from the flux. Dip them immediately into the molten solder to the same depth. Keep them in the molten solder for 2 to 5 seconds. Withdraw them and allow the solder to cool in air.

Requirements:

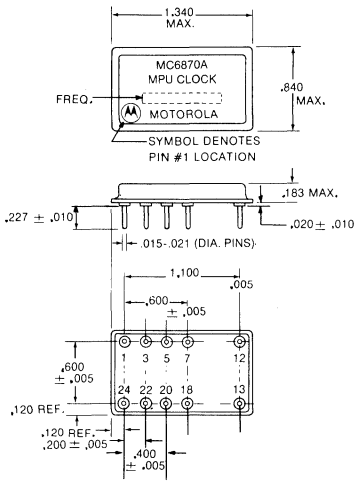
3.1 The terminals are considered solderable and acceptable for electrical connection purposes if 90 percent of the cold solder surface is uniform and free from breaks and pinholes. The other 10 percent of the cooled solder surface may show only pinholes, voids, or rough spots that are not concentrated in one area.

MC6870A

limited function microprocessor clock
250 kHz to 2.5 MHz



DIMENSIONS

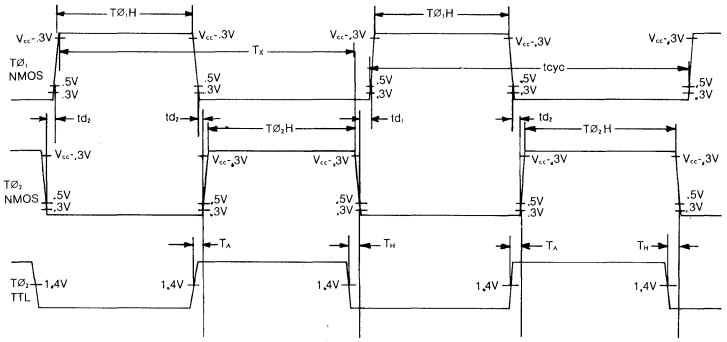


PIN	CONNECTION
1	GND
3	NC
5	$\varnothing_2$ TTL
7	V_{cc} (+5VDC)
12	$\varnothing_2$ NMOS
13	$\varnothing_1$ NMOS
18	GND
20	NC
22	NC
24	NC

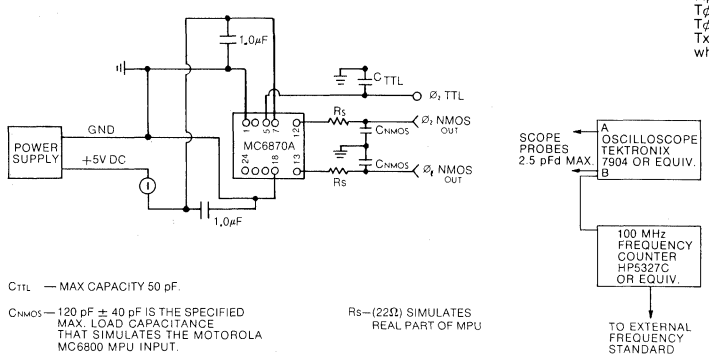
Note: All dimensions are in inches

WAVEFORM TIMING

(ALL TIME IN NANOSECONDS)



TEST CIRCUIT



CTTL — MAX CAPACITY 50 pF.

CNMOS — 120 pF ± 40 pF IS THE SPECIFIED MAX. LOAD CAPACITANCE THAT SIMULATES THE MOTOROLA MC6800 MPU INPUT.

RS — (22Ω) SIMULATES REAL PART OF MPU

specifications

Rating	Symbol	Value	Unit
Supply Voltage	V_{cc}	5.00±5%	Vdc
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C
Power Supply Drain (max.)	I_{pd}	100	mA

ELECTRICAL CHARACTERISTICS (V_{cc} = 5.0 ± 5%, V_{ss} = O, T_A = 0° to 70°C, unless otherwise noted)

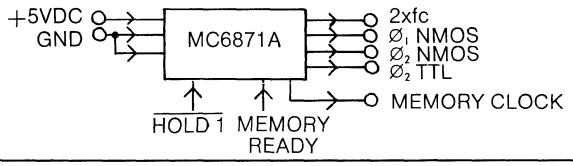
Characteristic	Symbol	Min	Typ	Max	Unit
Frequency					
Operating Frequency	f_c	.250		2.5	MHz
Frequency stability (inclusive of calibration tolerance at +25°C, operating temperature, input voltage change, load change, aging, shock and vibration)			±.01		%
NMOS Outputs at 1.0 MHz Operation**					
Pulse Width (meas. at V_{cc} = −.3V dc level)	TØ1H TØ2H	430 450			ns ns
Logic Levels	V_{OLC} V_{OHC}	V_{ss}-.1 V_{cc}-.3	— —	V_{ss}+.3 V_{cc}+.1	Vdc Vdc
Rise and Fall Times	t_r t_f	5 5	12 12	50 50	ns ns
*Overshoot/Undershoot Logic "1" Logic "0"	 V_{OS}	 V_{cc}-.5 V_{ss}-.5		 V_{cc}+.5 V_{ss}+.5	 Vdc Vdc
Pulse duration of any overshoot or undershoot	T_{OS}			40	ns
Period @ 0.3V dc Level	t_{cyc}		1.00		us
Edge Timing @ V_{cc}=0.3V dc	Tx	940			ns
NMOS Relationship @ +0.5V dc Level	t_{d1} t_{d2}	0 0		 8.0	 us
TTL Outputs					
In ref. to $\varnothing_2$ NMOS @ 0.3V dc					
$\varnothing_2$ TTL @ +1.4V dc	T_A T_H	15 10	30 25	45 40	ns ns
Logic Levels	V_{OH} V_{OL}	2.4	3.2 .3	 .4	Vdc Vdc
Rise and Fall Times .4V and 2.4V 2.4V and .4V	 t_r t_f			 15 15	 ns ns
Logic "0" Sink (/Gate)	I_{OL}			−1.6	mA
Logic "1" Source (/Gate)	I_{OH}			+40	uA
Current Output Shorted	I_{SC}	−18		−57	mA
Load					
NMOS—Load Capacity $\varnothing_1$, $\varnothing_2$	C_{NMOS}	80	120	160	pf
TTL—No. of Loads				5	ttl
TTL—Load Capacity	C_{TTL}			50	pf

*Into specified test load

**Apply the following parameters for frequencies other than 1.0 MHz:
$T\phi_1H$=0.5 (P-140) ns
$T\phi_2H$=0.5 (P-100) ns
Tx=(P-60) ns
where P=desired period of operation in nanoseconds

MC6871A

full function microprocessor clock
850 kHz to 2.5 MHz



specifications

Rating	Symbol	Value	Unit
Supply Voltage	V_{cc}	5.00±5%	Vdc
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C
Power Supply Drain (max.)	I_{pd}	100	mA

ELECTRICAL CHARACTERISTICS (V_{cc} = 5.0 ± 5%, V_{ss} = O,T_A = 0° to 70°C, unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Frequency					
Operating Frequency	f_c	.850		2.5	MHz
Frequency stability (inclusive of calibration tolerance at +25°C, operating temperature, input voltage change, load change, aging, shock and vibration)			±.01		%
NMOS Outputs at 1.0 MHz Operation* **					
Pulse Width (meas. at V_{cc}= −.3V dc level)	TØ1H TØ2H	430 450			ns ns
Logic Levels	V_{OLC} V_{OHC}	V_{ss}-.1 V_{cc}-.3	— —	V_{ss}+.3 V_{cc}+.1	Vdc Vdc
Rise and Fall Times	t_r t_f	5 5	12 12	50 50	ns ns
*Overshoot/Undershoot Logic "1" Logic "0"	 V_{OS}	 V_{cc}-.5 V_{ss}-.5		 V_{cc}+.5 V_{ss}+.5	 Vdc Vdc
Pulse duration of any overshoot or undershoot	T_{OS}			40	ns
Period @ 0.3V dc Level	t_{cyc}		1.00		us
Edge Timing @ V_{cc}=0.3V dc	Tx	940			ns
NMOS Relationship @ +0.5V dc Level	t_{d1} t_{d2}	0 0		8.0	us
TTL Outputs					
In ref. to Ø2 NMOS @ 0.3V dc					
Ø2 TTL @ 1.4V dc	T_A T_H	15 10	30 25	45 40	ns ns
Memory Clock @ 1.4V dc	T_C T_J	30 20	50 40	70 60	ns ns
2xfc @ 1.4V dc	T_B	40	80	120	ns
Logic Levels	V_{OH} V_{OL}	2.4	3.2 .3	 .4	Vdc Vdc
Rise and Fall Times .4V and 2.4V 2.4V and .4V	 t_r t_f			 15 15	 ns ns
Logic "0" Sink (/Gate)	I_{OL}			−1.6	mA
Logic "1" Source (/Gate)	I_{OH}			+40	uA
Current Output Shorted	I_{SC}	−18		−57	mA
Load					
NMOS—Load Capacity Ø1, Ø2	C_{NMOS}	80	120	160	pf
TTL—No. of Loads				5	ttl
TTL—Load Capacity	C_{TTL}			50	pf
Logic Inputs ("0" Level Applies HOLD or MEMORY READY)**					
Holds Ø1 NMOS 'High', Ø2 NMOS 'Low', Ø2 TTL 'Low'	$\overline{HOLD\ 1}$	−.2		+.4	Vdc
Holds Ø1 NMOS 'Low', Ø2 NMOS 'High', Ø2 TTL 'High', and MEMORY CLOCK 'High'	MEMORY READY	−.2		+.4	Vdc

*Into specified test load

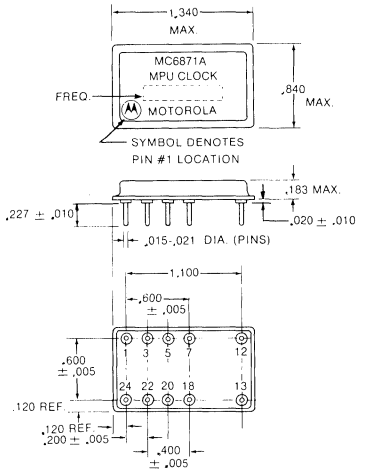
**Must be externally held at "1" level (2.4V min., 5.0V max.) if not used

***Apply the following parameters for frequencies other than 1 MHz:
TØ1H=0.5 (P-140) ns
TØ2H=0.5 (P-100) ns
Tx=(P-60) ns
where P=desired period of operation in nanoseconds

PIN	CONNECTION
1	GND
3	MEMORY CLOCK
5	Ø2 TTL
7	V_{cc} (+5VDC)
12	Ø2 NMOS
13	Ø1 NMOS
18	GND
20	$\overline{HOLD\ 1}$
22	MEMORY READY
24	2xfc

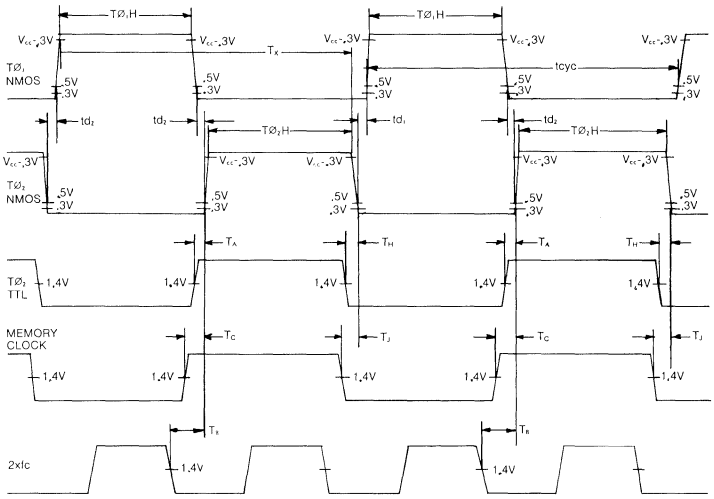
Note: All dimensions are in inches

DIMENSIONS

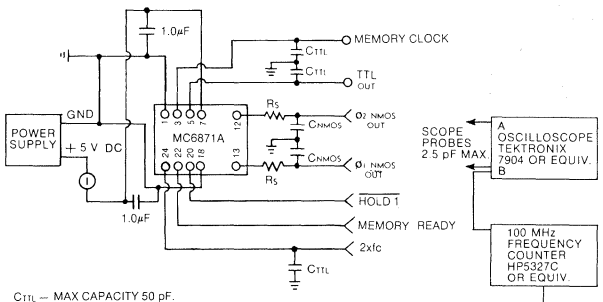


WAVEFORM TIMING

(ALL TIME IN NANOSECONDS)



TEST CIRCUIT



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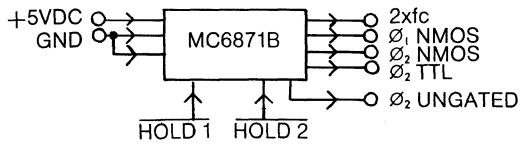
CNMOS — 120 pF ± 40 pF IS THE SPECIFIED MAX. LOAD CAPACITANCE THAT SIMULATES THE MOTOROLA MC6800 MPU INPUT.

RS—(22Ω) SIMULATES REAL PART OF MPU

*HOLD AND MEMORY READY MUST BE EXTERNALLY HELD AT "1" LEVEL (2.4VDC MIN., 5.0VDC MAX.) WHEN NOT USED

MC6871B

alternate function microprocessor clock
250 kHz to 2.5 MHz



specifications

Rating	Symbol	Value	Unit
Supply Voltage	V_{cc}	5.00±5%	Vdc
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C
Power Supply Drain (max.)	I_{pd}	100	mA

ELECTRICAL CHARACTERISTICS (V_{cc} = 5.0 ± 5%, V_{ss} = O,T_A = 0° to 70°C, unless otherwise noted)

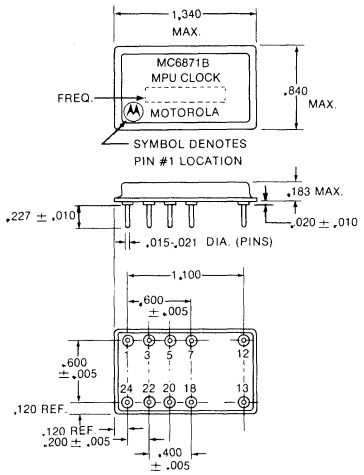
Characteristic	Symbol	Min	Typ	Max	Unit
Frequency					
Operating Frequency Frequency stability (inclusive of calibration tolerance at +25°C, operating temperature, input voltage change, load change, aging, shock and vibration)	f_c	.250	±.01	2.5	MHz %
NMOS Outputs at 1.0 MHz Operation* **					
Pulse Width (meas. at V_{cc}= −.3V dc level)	TØ1H TØ2H	430 450			ns ns
Logic Levels	V_{OLC} V_{OHC}	V_{ss}-.1 V_{cc}-.3	— —	V_{ss}+.3 V_{cc}+.1	Vdc Vdc
Rise and Fall Times	t_r t_f	5 5	12 12	50 50	ns ns
*Overshoot/Undershoot Logic "1" Logic "0"	 V_{OS}	 V_{cc}-.5 V_{ss}-.5		 V_{cc}+.5 V_{ss}+.5	 Vdc Vdc
Pulse duration of any overshoot or undershoot	T_{OS}			40	ns
Period @ 0.3V dc Level	t_{cyc}		1.00		us
Edge Timing @ V_{cc}=0.3V dc	Tx	940			ns
NMOS Relationship @ +0.5V dc	t_{d1} t_{d2}	0 0		8.0	us
TTL Outputs					
In ref. to $\varnothing_2$ NMOS @ 0.3V dc					
$Ø_2$ TTL @ 1.4V dc	T_A T_H	15 10	30 25	45 40	ns ns
$\varnothing_2$ Ungated @ 1.4V dc	T_C T_J	30 20	50 40	70 60	ns ns
2xfc @ 1.4V dc	T_B	40	80	120	ns
Logic Levels	V_{OH} V_{OL}	2.4	3.2 .3	 .4	Vdc Vdc
Rise and Fall Times .4V and 2.4V 2.4V and .4V	 t_r t_f			 15 15	 ns ns
Logic "0" Sink (/Gate)	I_{OL}			−1.6	mA
Logic "1" Source (/Gate)	I_{OH}			+40	uA
Current Output Shorted	I_{SC}	−18		−57	mA
Load					
NMOS—Load Capacity $Ø_1$, $Ø_2$	C_{NMOS}	80	120	160	pf
TTL—No. of Loads				5	ttl
TTL—Load Capacity	C_{TTL}			50	pf
Logic Inputs ("0" Level applies HOLD)**					
Holds Ø1 NMOS 'High', Ø2 NMOS 'Low', Ø2 TTL 'Low'	$\overline{HOLD\ 1}$	−.2		+.4	Vdc
Holds Ø1 NMOS 'Low', Ø2 NMOS 'High', Ø2 TTL 'High'	$\overline{HOLD\ 2}$	−.2		+.4	Vdc

*Into specified test load

**Must be externally held at "1" level (2.4V min., 5.0V max.) if not used

***Apply the following parameters for frequencies other than 1 MHz:
TØ1H=0.5 (P-140) ns
TØ2H=0.5 (P-100) ns
Tx=(P-60) ns
where P=desired period of operation in nanoseconds

DIMENSIONS



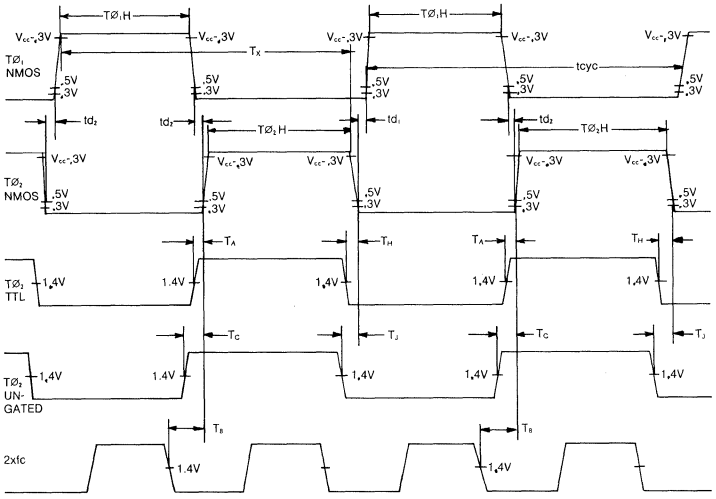
PIN	CONNECTION
1	GND
3	$\varnothing_2$ TTL UNGATED
5	$\varnothing_2$ TTL
7	V_{cc} (+5VDC)
12	$\varnothing_2$ NMOS
13	$\varnothing_1$ NMOS
18	GND
20	$\overline{HOLD\ 1}$
22	$\overline{HOLD\ 2}$
24	2xfc

Note: 4xfc available on request

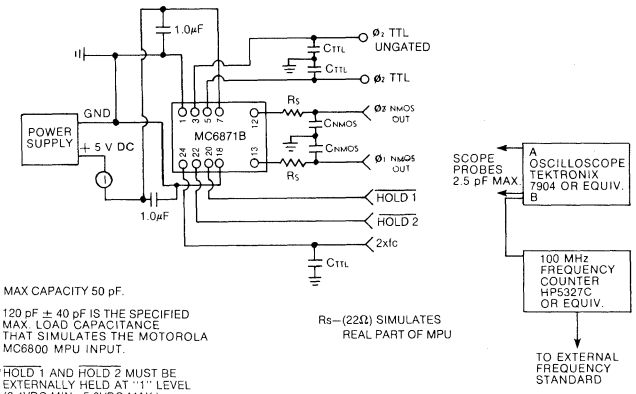
Note: All dimensions are in inches

WAVEFORM TIMING.

ALL TIME IN NANOSECONDS.



TEST DIAGRAM



C_{TTL} — MAX CAPACITY 50 pF.

C_{NMOS} — 120 pF ± 40 pF IS THE SPECIFIED MAX. LOAD CAPACITANCE THAT SIMULATES THE MOTOROLA MC6800 MPU INPUT.

*$\overline{HOLD\ 1}$ AND $\overline{HOLD\ 2}$ MUST BE EXTERNALLY HELD AT "1" LEVEL (2.4VDC MIN., 5.0VDC MAX.) WHEN NOT USED

R_S—(22Ω) SIMULATES REAL PART OF MPU

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MC6880
MC8T26

Product Preview

QUAD THREE-STATE BUS TRANSCEIVER

This quad three-state bus transceiver features both excellent MOS or MPU compatibility, due to its high impedance PNP transistor input, and high-speed operation made possible by the use of Schottky diode clamping. Both the -40 mA driver and -16 mA receiver outputs are short-circuit protected and employ three-state enabling inputs.

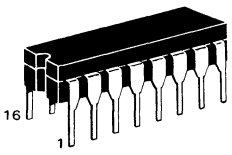
The device is useful as a bus extender in systems employing the M6800 family for other comparable MPU devices. The maximum input current of 200 μA at any of the device input pins assures proper operation despite the limited drive capability of the MPU chip. The inputs are also protected with Schottky-barrier diode clamps to suppress excessive undershoot voltages.

Propagation delay times for the driver portion are 16 ns typical while the receiver portion runs 6 ns for t_{PHL} and 13 ns for t_{PLH}. The MC8T26 is identical to the NE8T26 and it operates from a single +5 V supply.

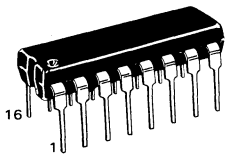
- High Impedance Inputs
- Single Power Supply
- High Speed Schottky Technology
- Three-State Drivers and Receivers
- Compatible Wtih M6800 Family Microprocessor

QUAD THREE-STATE BUS TRANSCEIVER WITH HIGH IMPEDANCE PNP INPUTS

SILICON MONOLITHIC
INTEGRATED CIRCUITS

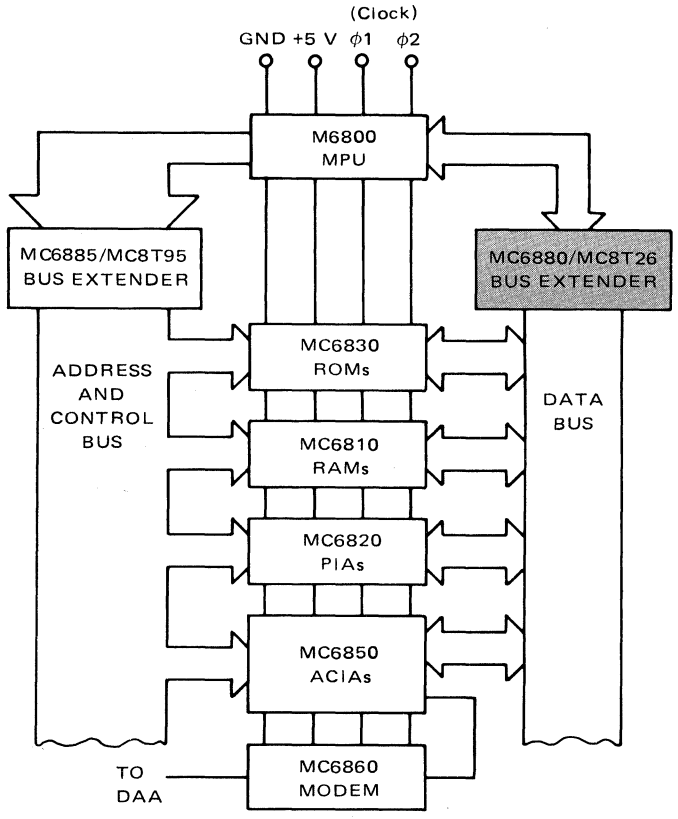


L SUFFIX
CERAMIC PACKAGE
CASE 620

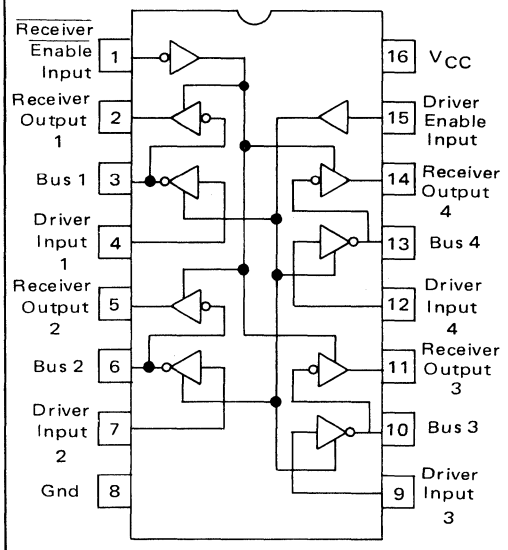


P SUFFIX
PLASTIC PACKAGE
CASE 648

MICROPROCESSOR BUS EXTENDER APPLICATION



PIN CONNECTIONS – MC6880 MC8T26



MAXIMUM RATINGS (T_A = 25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	8.0	Vdc
Input Voltage	V_I	5.5	Vdc
Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	1000 6.7	mW mW/°C
Operating Ambient Temperature Range	T_A	0 to +75	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS (Unless Otherwise Noted Specifications Apply 4.75 V ≤ V_{CC} ≤ 5.25 V and 0°C ≤ T_A ≤ 75°C)

Characteristic	Symbol	Min	Typ	Max	Unit
Input Current — Low Logic State					
($\overline{\text{Receiver Enable}}$ Input, $V_{IL(RE)}$ = 0.4 V)	$I_{IL(\overline{RE})}$	–	–	-200	μA
(Driver Enable Input, $V_{IL(DE)}$ = 0.4 V)	$I_{IL(DE)}$	–	–	-200	
(Driver Input, $V_{IL(D)}$ = 0.4 V)	$I_{IL(D)}$	–	–	-200	
(Bus (Receiver) Input, $V_{IL(B)}$ = 0.4 V)	$I_{IL(B)}$	–	–	-200	
Input Current-High Logic State					
($\overline{\text{Receiver Enable}}$ Input, $V_{IH(RE)}$ = 5.25 V)	$I_{IH(\overline{RE})}$	–	–	25	μA
(Driver Enable Input, $V_{IH(DE)}$ = 5.25 V)	$I_{IH(DE)}$	–	–	25	
(Driver Input, $V_{IH(D)}$ = 5.25 V)	$I_{IH(D)}$	–	–	25	
Input Voltage — Low Logic State					
($\overline{\text{Receiver Enable}}$ Input)	$V_{IL(\overline{RE})}$	0.85	–	–	V
(Driver Enable Input	$V_{IL(DE)}$	0.85	–	–	
(Driver Input)	$V_{IL(D)}$	0.85	–	–	
Input Voltage — High Logic State					
($\overline{\text{Receiver Enable}}$ Input)	$V_{IH(\overline{RE})}$	–	–	2.0	V
(Driver Enable Input)	$V_{IH(DE)}$	–	–	2.0	
(Driver Input)	$V_{IH(D)}$	–	–	2.0	
Output Voltage — Low Logic State					
(Bus (Driver) Output, $I_{OL(B)}$ = -10 mA)	$V_{OL(B)}$	–	–	0.5	V
(Receiver Output, $I_{OL(R)}$ = -2.0 mA)	$V_{OL(R)}$	–	–	0.5	
Output Voltage — High Logic State					
(Bus (Driver) Output, $I_{OH(B)}$ = 40 mA)	$V_{OH(B)}$	2.6	3.1	–	V
(Receiver Output, $I_{OH(R)}$ = 16 mA)	$V_{OH(R)}$	2.6	3.1	–	
Output Disabled Leakage Current — High Logic State					
(Bus (Driver) Output, $V_{OH(B)}$ = 2.6 V)	$I_{OHL(B)}$	–	–	100	μA
(Receiver Output, $V_{OH(R)}$ = 2.6 V)	$I_{OHL(R)}$	–	–	100	
Input Clamp Voltage					
(Driver Enable Input $I_{IC(DE)}$ = -5.0 mA)	$V_{IC(DE)}$	–	–	-1.0	V
(Receiver Enable Input $I_{IC(RE)}$ = -5.0 mA)	$V_{IC(RE)}$	–	–	-1.0	
(Driver Input $I_{IC(D)}$ = -5.0 mA)	$V_{IC(D)}$	–	–	-1.0	
Output Short-Circuit Current, V_{CC} = 5.25 V (1)					
(Bus (Driver) Output)	$I_{OS(B)}$	-50	–	-150	mA
(Receiver Output)	$I_{OS(R)}$	-30	–	-75	
Power Supply Current (V_{CC} = 5.25 V)	I_{CC}	–	–	87	mA

(1) Only one output may be short-circuited at a time.

SWITCHING CHARACTERISTICS (Unless otherwise noted, specifications apply at $T_A = 25^oC$ and $V_{CC} = 5.0$ V)

Characteristic	Symbol	Figure	Min	Typ	Max	Unit
Propagation Delay Time from Receiver (Bus) Input to High Logic State Receiver Output	$t_{PLH(R)}$	1	–	13	18	ns
Propagation Delay Time from Receiver (Bus) Input to Low Logic State Receiver Output	$t_{PHL(R)}$	1	–	6.0	10	ns
Propagation Delay Time from Driver Input to High Logic State Driver (Bus) Output	$t_{PLH(D)}$	2	–	16	20	ns
Propagation Delay Time from Driver Input to Low Logic State Driver (Bus) Output	$t_{PHL(D)}$	2	–	16	20	ns
Propagation Delay Time from $\overline{\text{Receiver Enable}}$ Input to High Impedance (Open) Logic State Receiver Output	$t_{PLO(\overline{RE})}$	3	–	10	17	ns
Propagation Delay Time from $\overline{\text{Receiver Enable}}$ Input to Low Logic Level Receiver Output	$t_{POL(\overline{RE})}$	3	–	20	30	ns
Propagation Delay Time from Driver Enable Input to High Impedance Logic State Driver (Bus) Output	$t_{PLO(DE)}$	4	–	35	43	ns
Propagation Delay Time from Driver Enable Input to Low Logic State Driver (Bus) Output	$t_{POL(DE)}$	4	–	29	38	ns

FIGURE 1 – TEST CIRCUIT AND WAVEFORMS FOR PROPAGATION DELAY FROM BUS (RECEIVER) INPUT TO RECEIVER OUTPUT, $t_{PLH(R)}$, $t_{PHL(R)}$

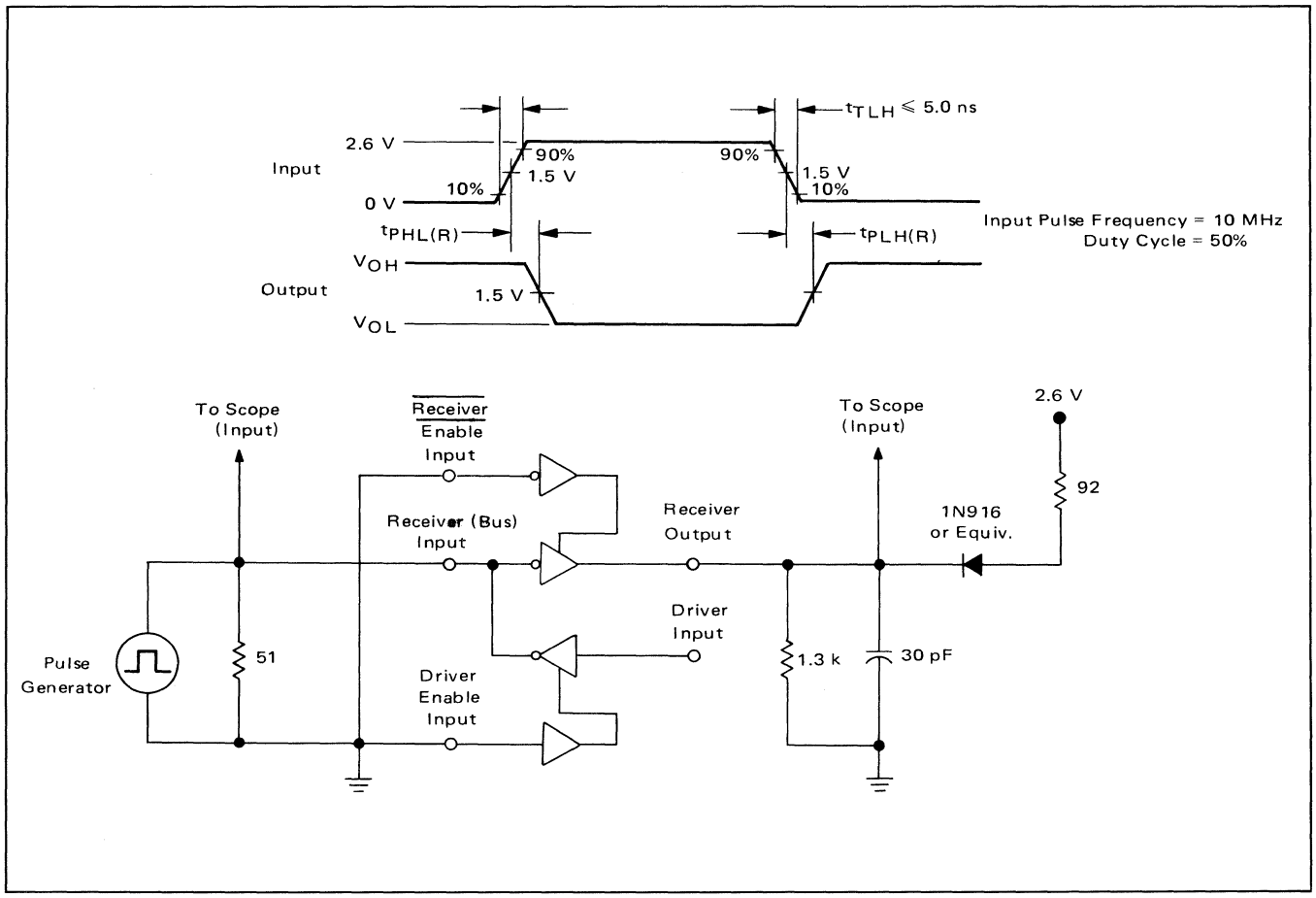


FIGURE 2 – TEST CIRCUIT AND WAVEFORMS FOR PROPAGATION DELAY TIME FROM DRIVER INPUT TO BUS (DRIVER) OUTPUT, $t_{PLH(D)}$ AND $t_{PHL(D)}$

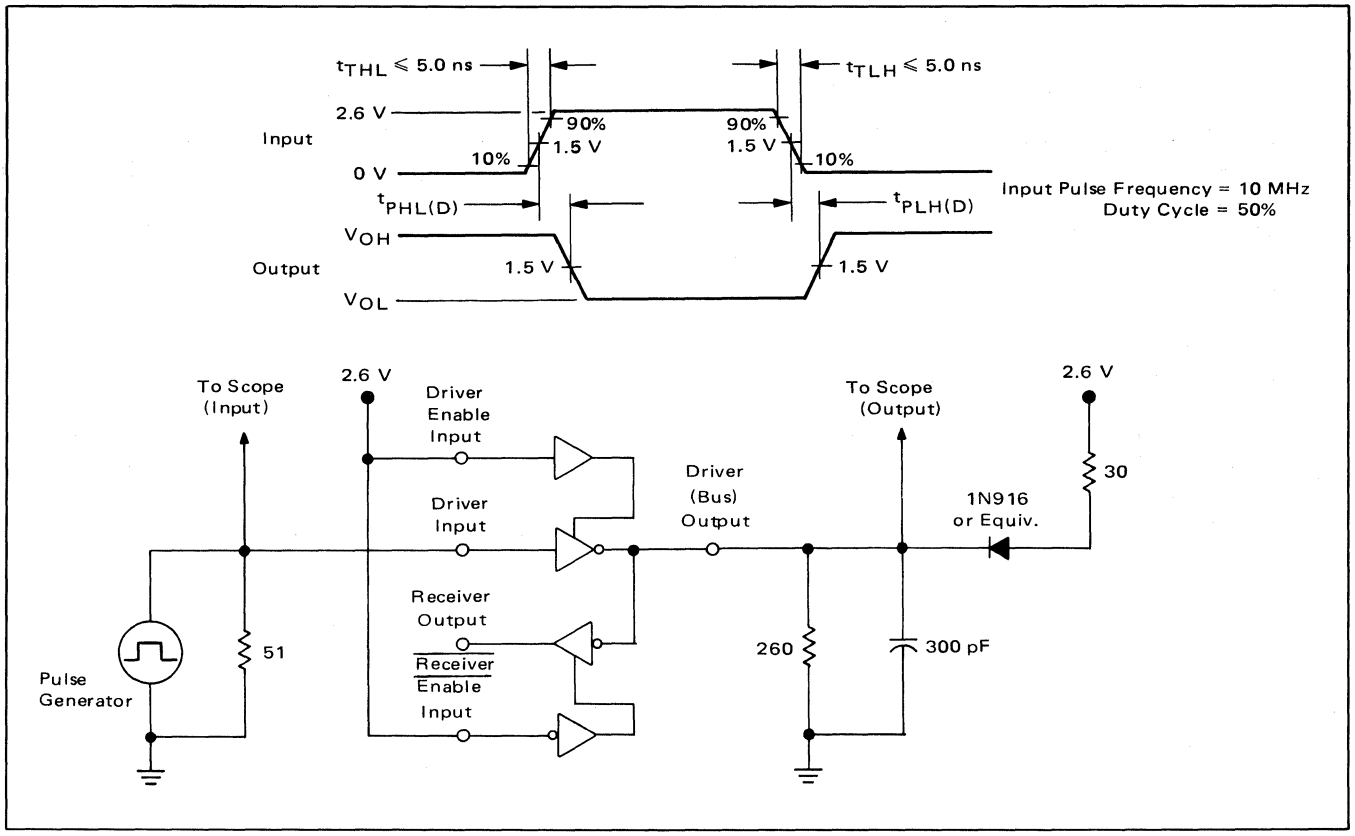


FIGURE 3 – TEST CIRCUIT AND WAVEFORMS FOR PROPAGATION DELAY TIME FROM RECEIVER ENABLE INPUT TO RECEIVER OUTPUT, $t_{PLO(RE)}$, AND $t_{POL(RE)}$

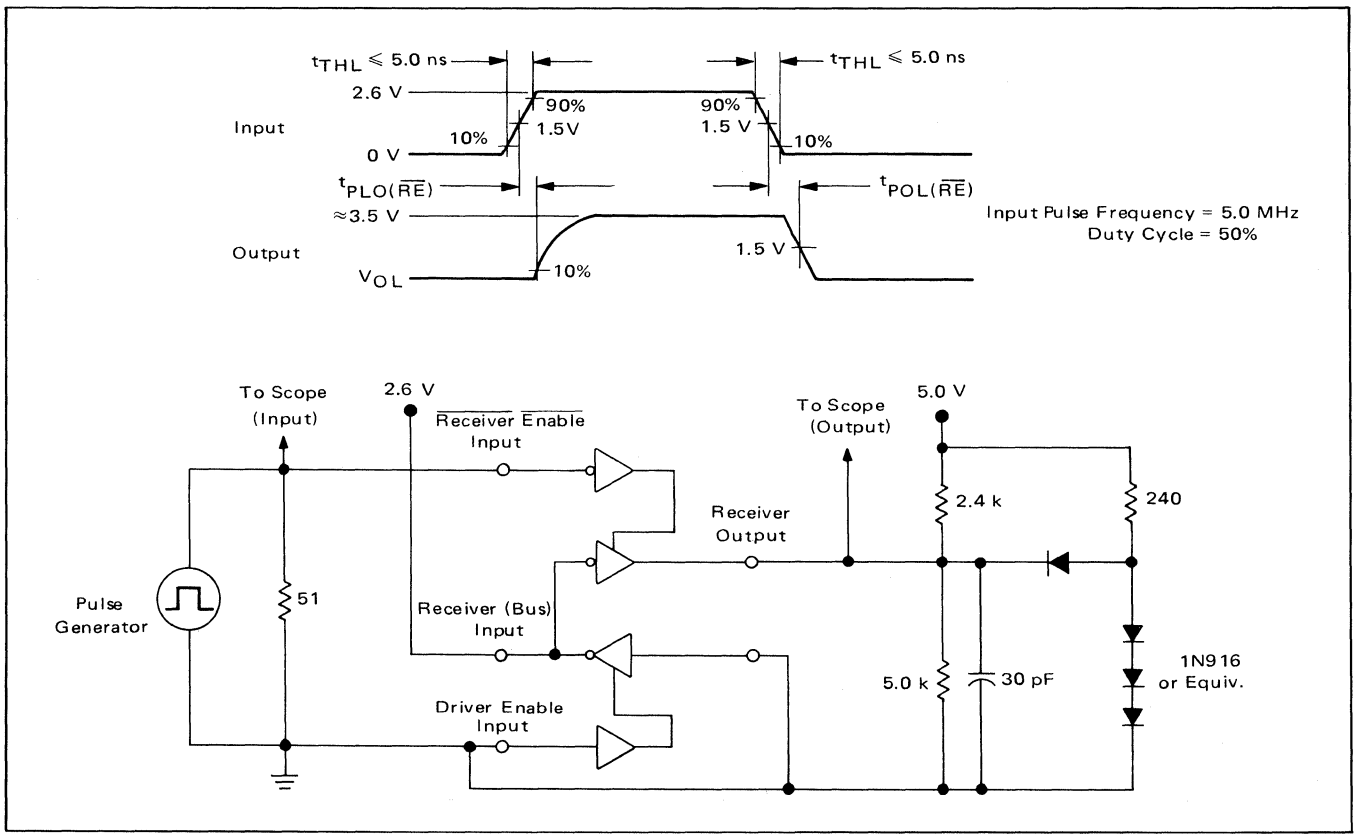


FIGURE 4 – TEST CIRCUIT AND WAVEFORMS FOR PROPAGATION DELAY TIMES FROM DRIVER ENABLE INPUT TO DRIVER (BUS) OUTPUT ,$t_{PLO(DE)}$ AND $t_{POL(DE)}$

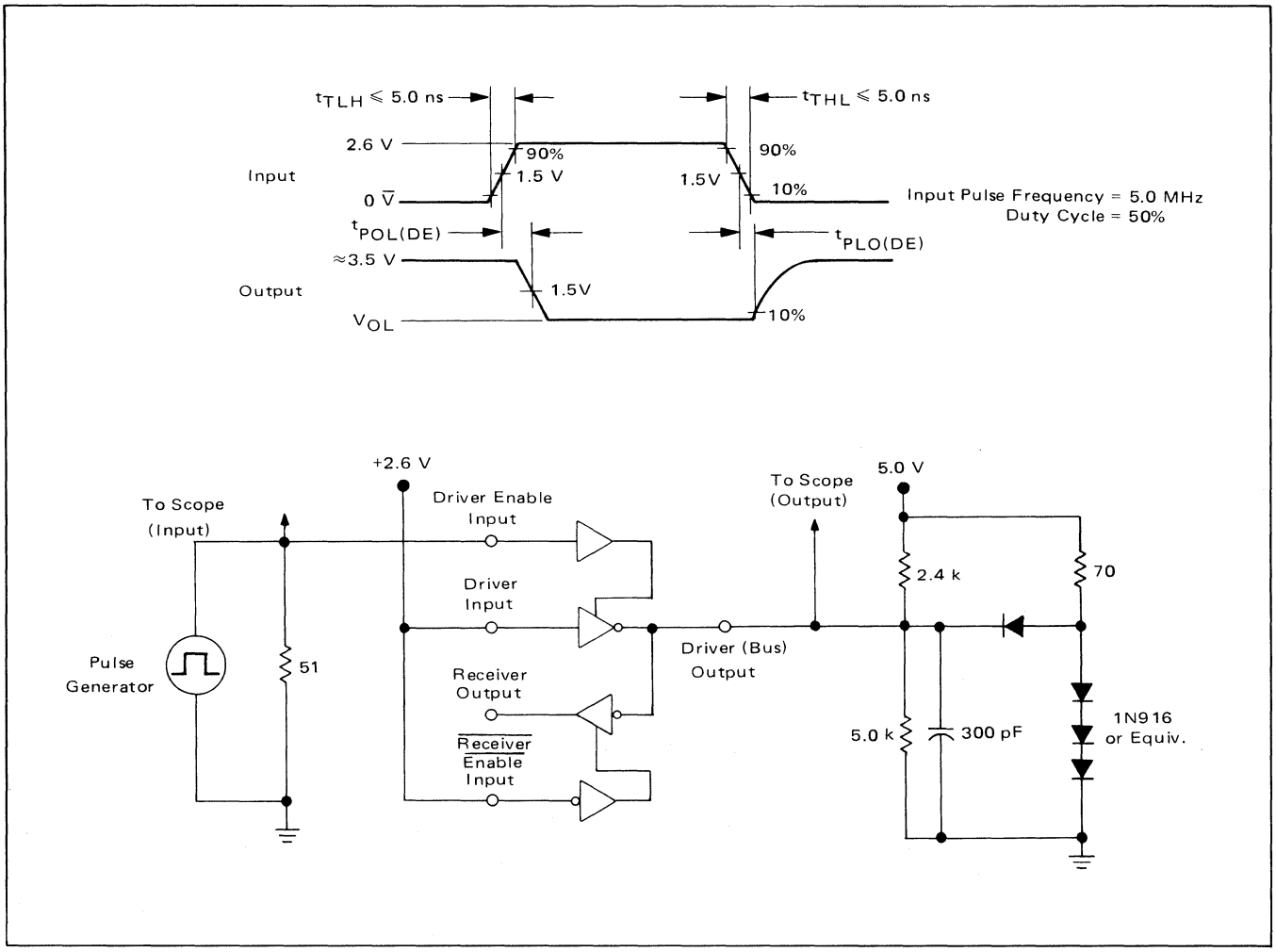
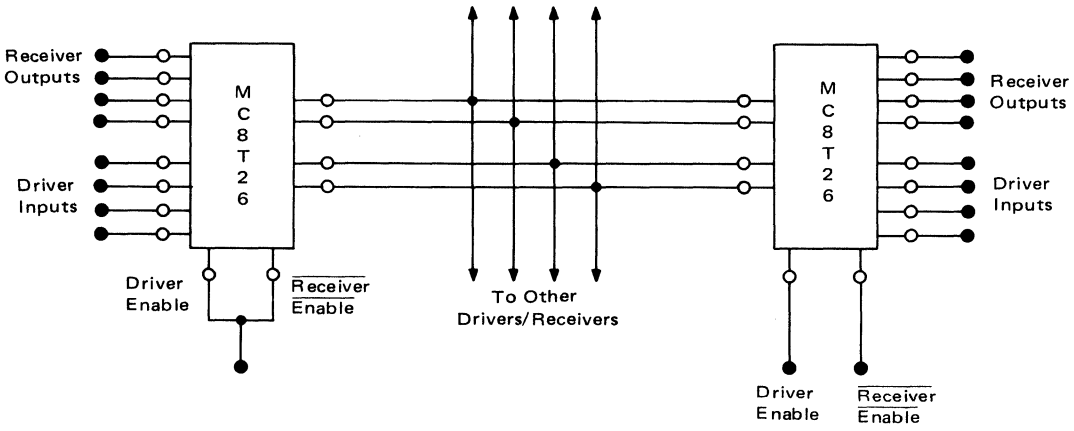
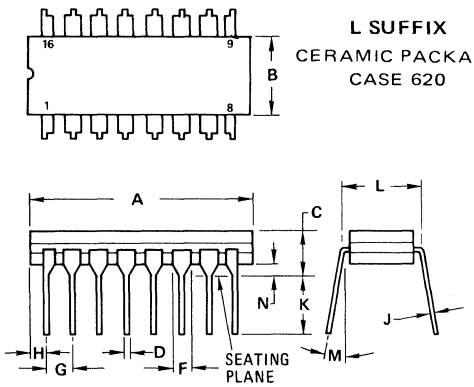


FIGURE 5 – BI-DIRECTIONAL BUS APPLICATIONS

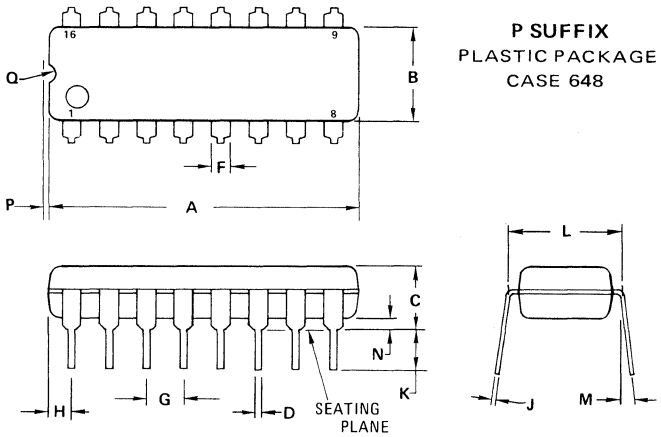




L SUFFIX
CERAMIC PACKAGE
CASE 620

NOTES:
1 LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION
2 PKG. INDEX: NOTCH IN LEAD NOTCH IN CERAMIC OR INK DOT
3 DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	19.05	19.81	0.750	0.780
B	6.22	6.98	0.245	0.275
C	4.06	5.08	0.160	0.200
D	0.38	0.51	0.015	0.020
F	1.40	1.65	0.055	0.065
G	2.54 BSC		0.100 BSC	
H	0.51	1.14	0.020	0.045
J	0.20	0.30	0.008	0.012
K	3.18	4.06	0.125	0.160
L	7.37	7.87	0.290	0.310
M	–	15°	–	15°
N	0.51	1.02	0.020	0.040



P SUFFIX
PLASTIC PACKAGE
CASE 648

NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	20.70	21.34	0.815	0.840
B	6.10	6.60	0.240	0.260
C	4.06	4.57	0.160	0.180
D	0.38	0.51	0.015	0.020
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.32	1.83	0.052	0.072
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.37	7.87	0.290	0.310
M	–	10°	–	10°
N	0.51	1.02	0.020	0.040
P	0.13	0.38	0.005	0.015
Q	0.51	0.76	0.020	0.030

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XC6881
XC3449

Product Preview

TRIPLE BI-DIRECTIONAL BUS SWITCH

The XC6881/3449 is a three channel, non-inverting, bi-directional Bus Extender. It is designed to allow the bi-directional exchange of TTL level digital information between a selected pair of ports in a three port network. All three ports of each channel may be forced to a high impedance condition through that channel's Enable input.

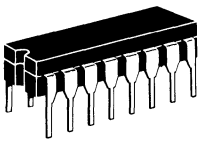
Port pair selection and listener/talker status for the three channels is determined through the Control and Select inputs. All inputs are PNP buffered and M6800 Family compatible.

A summary of XC6881/3449 features include:

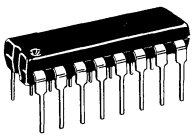
- Three Channels
- Noninverting Data Exchange
- Bi-Directional Operation
- Active Pull-Up with Three-State Capability
- High Impedance Inputs
- TTL Compatible (74LS)

BI-DIRECTIONAL BUS EXTENDER/SWITCH

SILICON MONOLITHIC INTEGRATED CIRCUITS

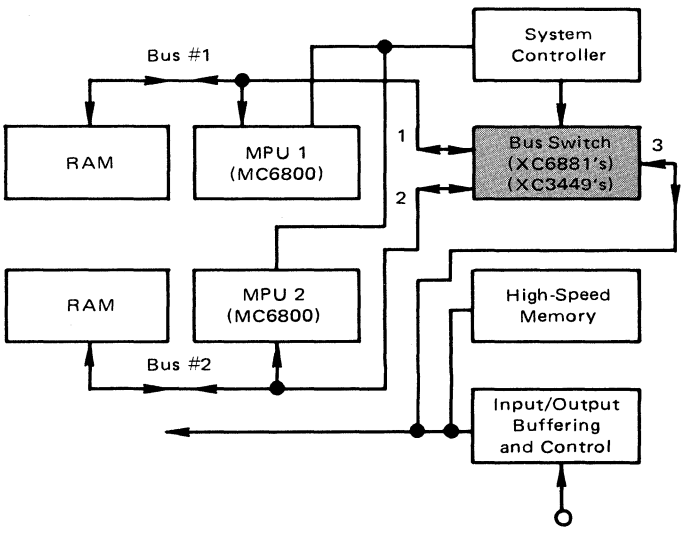


L SUFFIX
CERAMIC PACKAGE
CASE 620

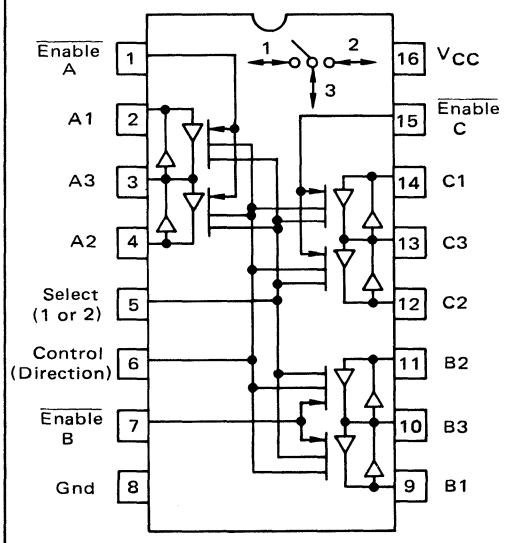


P SUFFIX
PLASTIC PACKAGE
CASE 648

MICROPROCESSOR BUS SWITCH APPLICATION



PIN CONNECTIONS

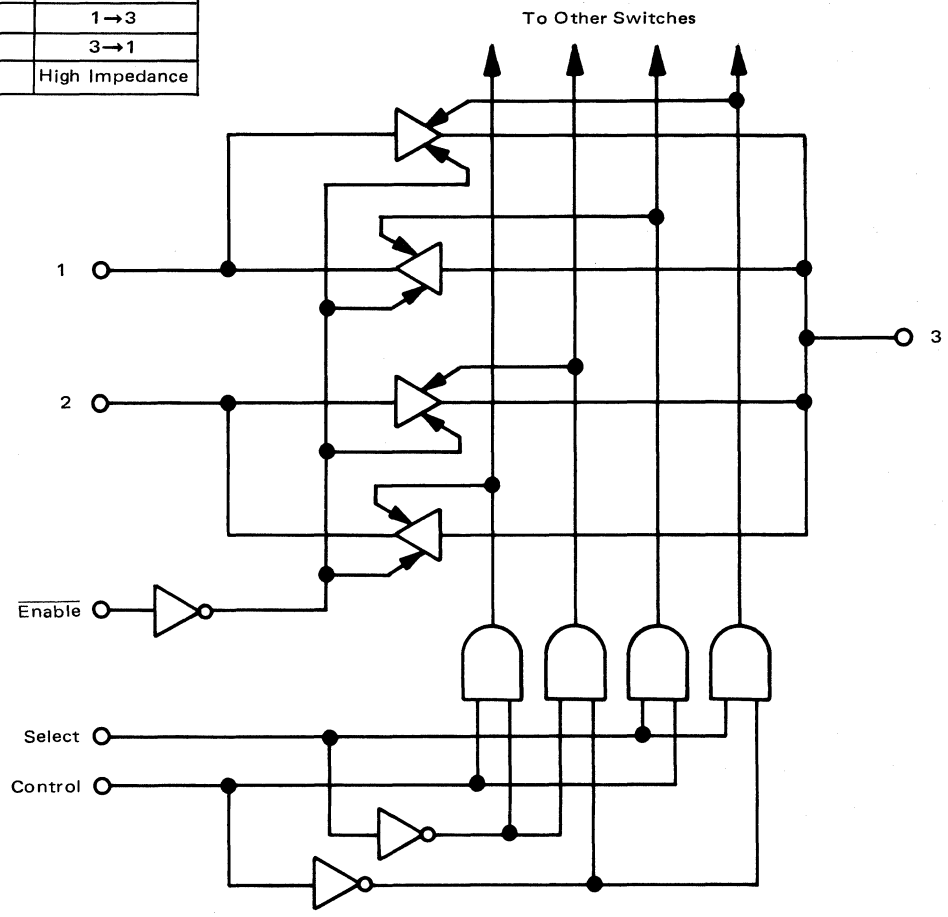


TRUTH TABLE

$\overline{\text{Enable}}$	Select	Control	Data Flow
0	0	0	2→3
0	0	1	3→2
0	1	0	1→3
0	1	1	3→1
1	X	X	High Impedance

X - Don't Care

FUNCTIONAL DIAGRAM



TARGET SPECIFICATIONS (4.75 V ≤ V_{CC} ≤ 5.25 V, 0°C ≤ T_A ≤ 70°C)

Characteristic	Symbol	Min	Max	Unit
Input Current – Low Logic State (V_{IL} = 0.4 V)	I_{IL}	–	–200	μA
Input Current – High Logic State (V_{IH} = 5.25 V)	I_{IH}	–	25	μA
Input Voltage – Low Logic State	V_{IL}	0.8	–	V
Input Voltage – High Logic State	V_{IH}	–	2.0	V
Output Voltage – Low Logic State	V_{OL}			V
(I_{OL} = 8.0 mA)		–	0.5	
(I_{OL} = 16 mA)		–	0.6	
Output Voltage – High Logic State (I_{OH} = –1.0 mA)	V_{OH}	2.4	–	V
Output Disabled Current	I_{OD}			μA
(V_{OH} = 2.4 V)		–	25	
(V_{OL} = 0.5 V)		–	-25	

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XC6885 XC8T95
XC6886 XC8T96
XC6887 XC8T97
XC6888 XC8T98

Product Preview

HEX THREE-STATE BUFFER/INVERTER

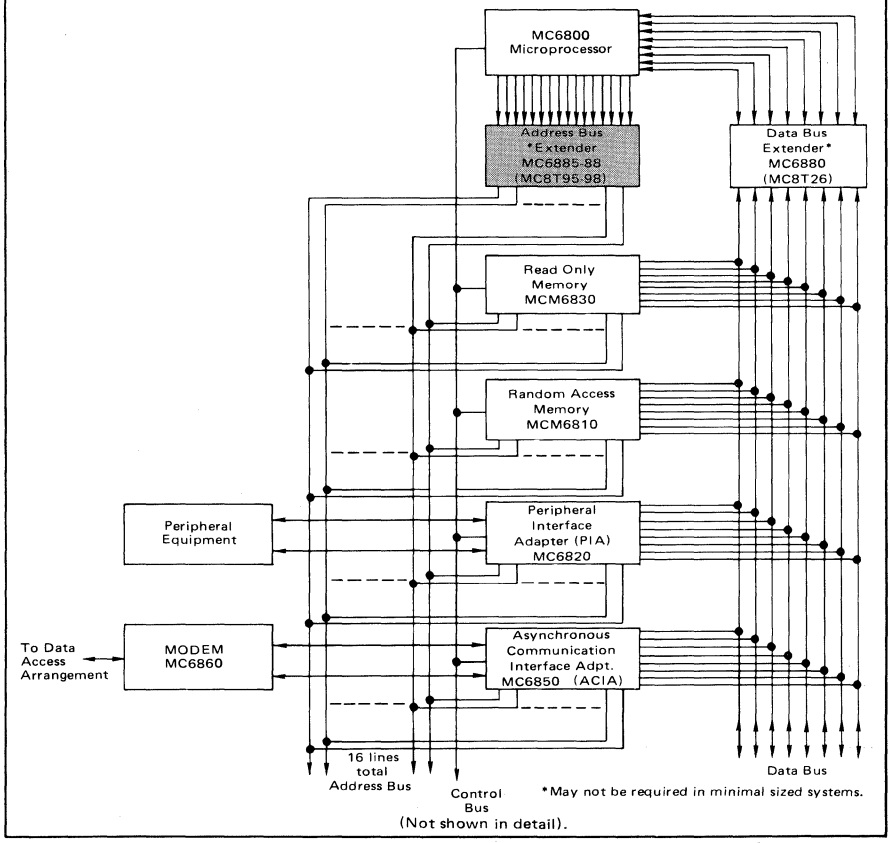
This series of devices combines four features usually found desirable in bus oriented systems. These features are: 1) – high impedance logic inputs insure that these devices do not seriously load the bus, 2) – three-state logic configuration allows buffers not being utilized to be effectively removed from the bus, 3) Schottky technology allows high-speed operation and 4) High-impedance output state maintained during power up/down. Particularly in unidirectional bus extenders and for both Address and Control functions.

The devices differ in that the non-inverting XC8T95/XC6885 and inverting XC8T96/XC6886 provide a two-input Enable which controls all six buffers, while the non-inverting XC8T97/XC6887 and inverting XC8T98/XC6888 provide two Enable inputs – one controlling four buffers and the other controlling the remaining two buffers.

The units are well-suited for Address buffers on the M6800 or similar microprocessor application.

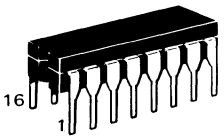
- High Speed – 8.0 ns (Typ)
- Three-State Logic Configuration
- Single +5 V Power Supply Requirement
- Compatible with 74LS Logic or M6800 Microprocessor Systems
- High Impedance PNP Inputs Assure Minimal Loading of the Bus

TYPICAL EXPANDED M6800 MPU SYSTEM

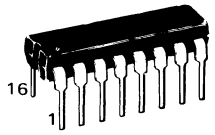


HEX THREE-STATE BUFFER/INVERTERS

MONOLITHIC SCHOTTKY INTEGRATED CIRCUITS

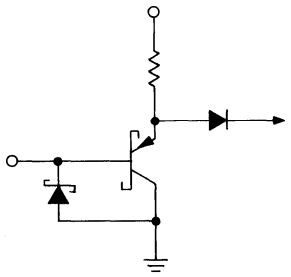


L SUFFIX
CERAMIC PACKAGE
CASE 620

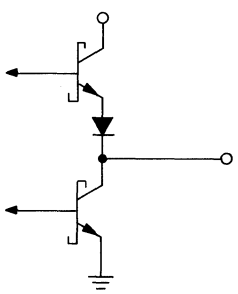


P SUFFIX
PLASTIC PACKAGE
CASE 648

INPUT EQUIVALENT CIRCUIT

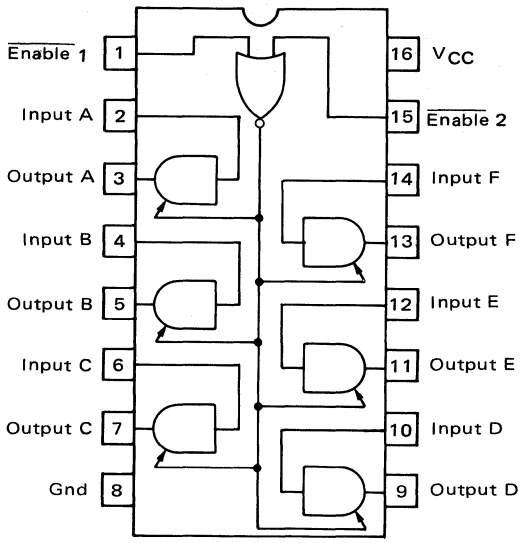


OUTPUT EQUIVALENT CIRCUIT



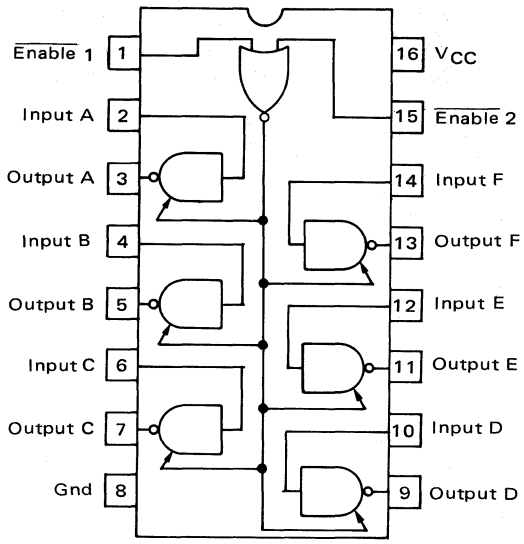
PIN CONNECTIONS AND TRUTH TABLES

XC6885/XC8T95



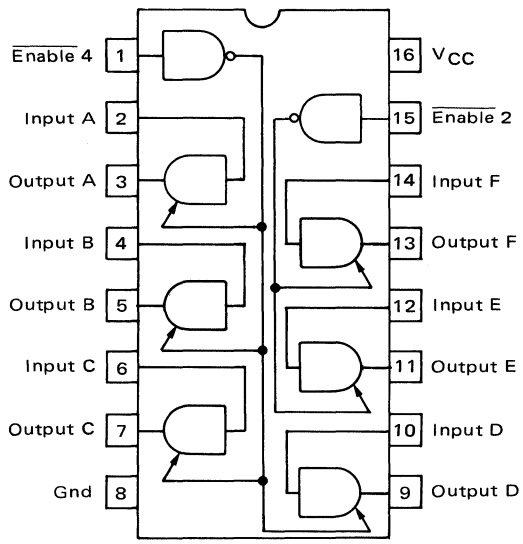
Enable 2	Enable 1	Input	Output
L	L	L	L
L	L	H	H
L	H	X	O
H	L	X	O
H	H	X	O

XC6886/XC8T96



Enable 2	Enable 1	Input	Output
L	L	L	H
L	L	H	O
L	H	X	O
H	L	X	O
H	H	X	O

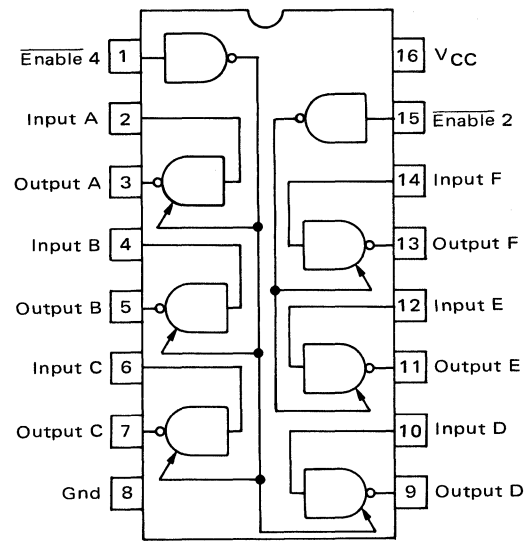
XC6887/XC8T97



Enable	Input	Output
L	L	L
L	H	H
H	X	O

L = Low Logic State
H = High Logic State
O = High Impedance State (open)
X = Irrelevant

XC6888/XC8T98



Enable	Input	Output
L	L	H
L	H	L
H	X	O

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	8.0	Vdc
Input Voltage	V_I	5.5	Vdc
Operating Ambient Temperature Range	T_A	0 to +75	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C
Operating Junction Temperature Plastic Package Ceramic Package	T_J	 150 175	°C

ELECTRICAL CHARACTERISTICS (Unless otherwise noted, $0^{o}C \leq T_A \leq 75^{o}C$ and $4.75\ V \leq V_{CC} \leq 5.25\ V$)

Characteristic	Symbol	Min	Typ	Max	Unit
Input Voltage — High Logic State (V_{CC} = 4.75 V, T_A = 25°C)	V_{IH}	2.0	–	–	V
Input Voltage — Low Logic State (V_{CC} = 4.75 V, T_A = 25°C)	V_{IL}	–	–	0.8	V
Input Current — High Logic State (V_{CC} = 5.25 V, V_{IH} = 2.4 V)	I_{IH}	–	–	40	μA
Input Current — Low Logic State (V_{CC} = 5.25 V, V_{IL} = 0.5 V, $V_{IL(\overline{E})}$ = 0.5 V)	I_{IL}	–	–	-400	μA
Input Current — High Impedance State (V_{CC} = 5.25 V, $V_{IL(I)}$ = 0.5 V, $V_{IH(\overline{E})}$ = 2.0 V)	$I_{IH(\overline{E})}$	–	–	-40	μA
Output Voltage — High Logic State (V_{CC} = 4.75 V, I_{OH} = -5.2 mA)	V_{OH}	2.4	–	–	V
Output Voltage — Low Logic State (I_{OL} = 48 mA)	V_{OL}	–	–	0.5	V
Output Current — High Impedance State (V_{CC} = 5.25 V, V_{OH} = 2.4 V) (V_{CC} = 5.25 V, V_{OL} = 0.5 V)	V_{OO}	– –	– –	40 -40	μA
Output Short-Circuit Current (V_{CC} = 5.25 V, V_O = 0) (only one output can be shorted at a time)	I_{OS}	-40	-80	-115	mA
Power Supply Current (V_{CC} = 5.25 V) XC8T95,XC8T97,XC6885,XC6887) XC8T96,XC8T98,XC6886,XC6888)	I_{CC}	– –	65 59	98 89	mA
Input Clamp Voltage (V_{CC} = 4.75 V, I_{IC} = -12 mA)	V_{IC}	–	–	-1.5	V
Output V_{CC} Clamp Voltage (V_{CC} = 0, I_{OC} = 12 mA)	V_{OC}	–	–	1.5	V
Output Gnd Clamp Voltage (V_{CC} = 0, I_{OC} = -12 mA)	V_{OC}	–	–	-1.5	V
Input Voltage (I_I = 1.0 mA)	V_I	5.5	–	–	V

SWITCHING CHARACTERISTICS (V_{CC} = 5.0 V, T_A = 25°C unless otherwise noted).

Characteristic	Symbol	Min	Typ	Max	Unit
Propagation Delay Time — Input to Output (R_L = 200 Ω, C_L = 50 pF)	t_{PLH} t_{PHL}	– –	6.0 5.0	– –	ns ns
Propagation Delay Time — $\overline{\text{Enable}}$ to Output					
(R_L = 200 Ω, C_L = 50 pF)	$t_{PHO(\overline{E})}$	–	10	–	ns
(R_L = 200 Ω, C_L = 50 pF)	$t_{PLO(\overline{E})}$	–	12	–	ns
(R_L = ∞, C_L = 50 pF)	$t_{POH(\overline{E})}$	–	10	–	ns
(R_L = 200 Ω, C_L = 50 pF)	$t_{POL(\overline{E})}$	–	12	–	ns

FIGURE 1 – TEST CIRCUIT FOR SWITCHING CHARACTERISTICS

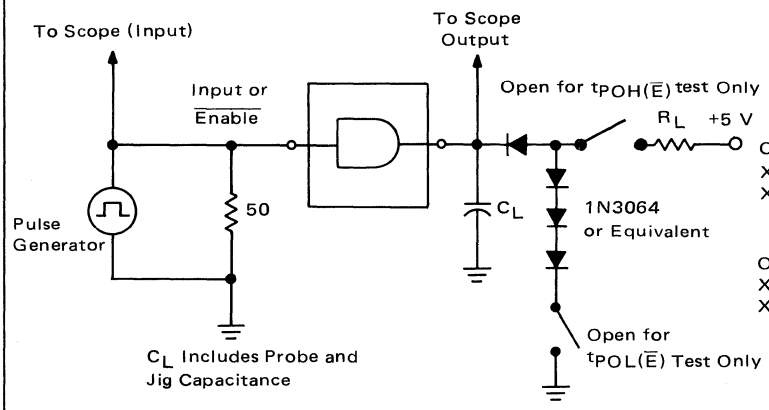


FIGURE 2 – WAVEFORMS FOR PROPAGATION DELAY TIMES INPUT TO OUTPUT

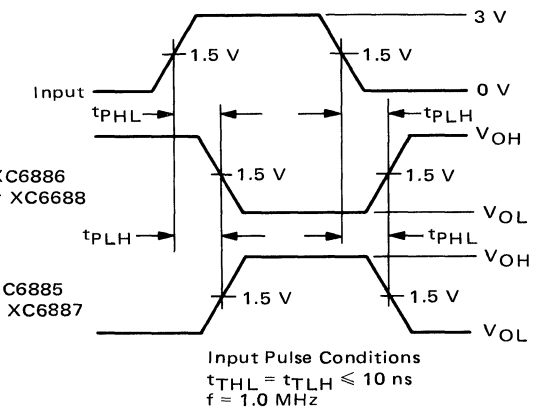


FIGURE 3 – WAVEFORMS FOR PROPAGATION DELAY TIMES – $\overline{\text{ENABLE}}$ TO OUTPUT

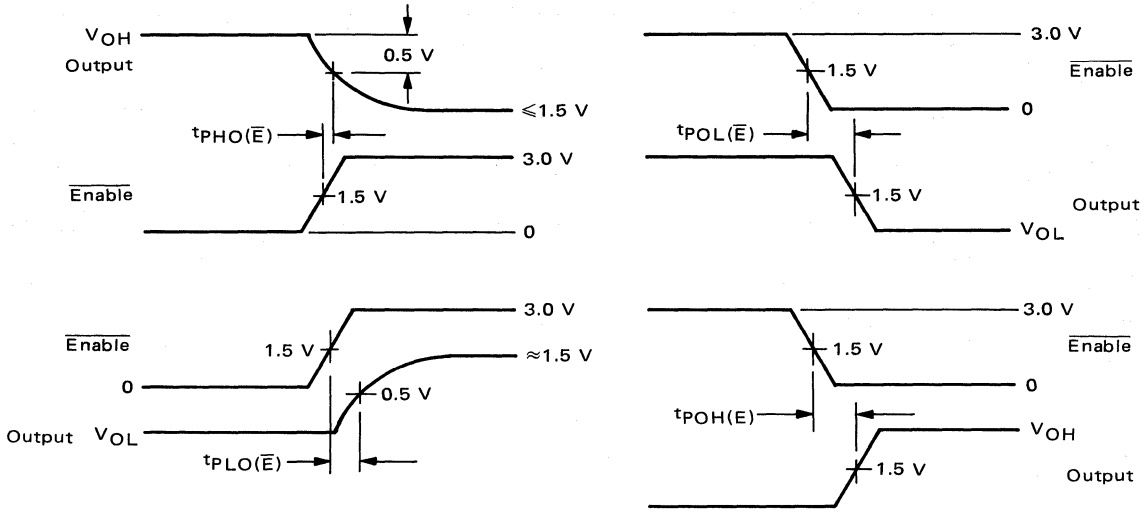
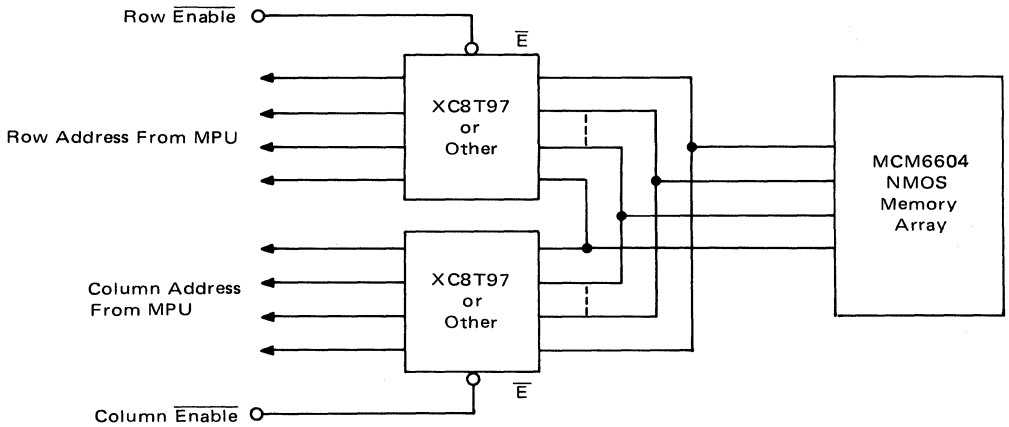
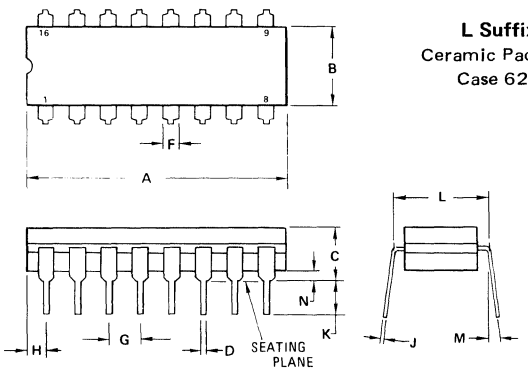


FIGURE 4 – ADDRESS MULTIPLEXER FOR 16-PIN 4K NMOS MEMORY

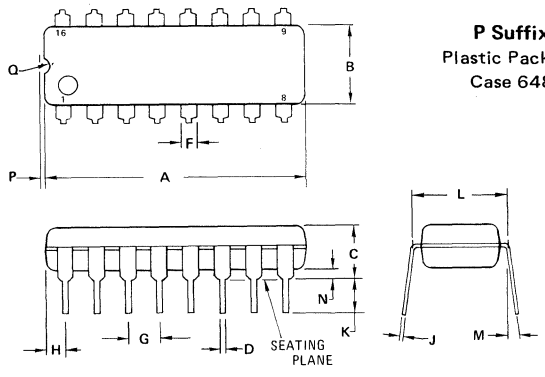




L Suffix
Ceramic Package
Case 620

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	19.05	19.81	0.750	0.780
B	6.22	6.98	0.245	0.275
C	4.06	5.08	0.160	0.200
D	0.38	0.51	0.015	0.020
F	1.40	1.65	0.055	0.065
G	2.54 BSC		0.100 BSC	
H	0.51	1.14	0.020	0.045
J	0.20	0.31	0.008	0.012
K	3.18	3.30	0.125	0.160
L	7.37	7.87	0.290	0.310
M	–	15°	–	15°
N	0.51	1.02	0.020	0.040

NOTES:
1 LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION
2 PKG. INDEX: NOTCH IN LEAD NOTCH IN CERAMIC OR INK DOT
3 DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL



P Suffix
Plastic Package
Case 648

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	20.70	21.34	0.815	0.840
B	6.10	6.60	0.240	0.260
C	4.06	4.57	0.160	0.180
D	0.38	0.51	0.015	0.020
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.32	1.83	0.052	0.072
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.37	7.87	0.290	0.310
M	–	10°	–	10°
N	0.51	1.02	0.020	0.040
P	0.13	0.38	0.005	0.015
Q	0.51	0.76	0.020	0.030

NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL

MOTOROLA Semiconductors
BOX 20912 • PHOENIX, ARIZONA 85036

MCM6810A

(0 to 70°C; L or P Suffix)

MCM6810AC

(-40 to 85°C; L Suffix only)

128 X 8-BIT STATIC RANDOM ACCESS MEMORY

The MCM6810 is a byte-organized memory designed for use in bus-organized systems. It is fabricated with N-channel silicon-gate technology. For ease of use, the device operates from a single power supply, has compatibility with TTL and DTL, and needs no clocks or refreshing because of static operation.

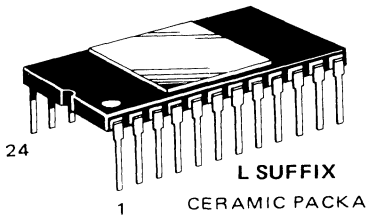
The memory is compatible with the M6800 Microcomputer Family, providing random storage in byte increments. Memory expansion is provided through multiple Chip Select inputs.

- Organized as 128 Bytes of 8 Bits
- Static Operation
- Bi-Directional Three-State Data Input/Output
- Six Chip Select Inputs (Four Active Low, Two Active High)
- Single 5-Volt Power Supply
- TTL Compatible
- Maximum Access Time = 350 ns — MCM6810AL1
  450 ns — MCM6810AL

MOS

(N-CHANNEL, SILICON-GATE)

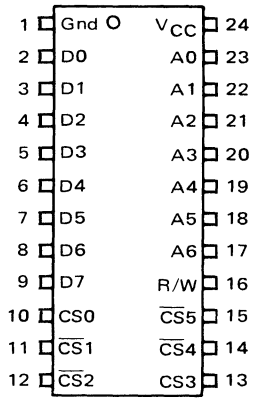
128 X 8-BIT STATIC RANDOM ACCESS MEMORY



L SUFFIX
CERAMIC PACKAGE
CASE 716

NOT SHOWN: P SUFFIX
PLASTIC PACKAGE
CASE 709

PIN ASSIGNMENT

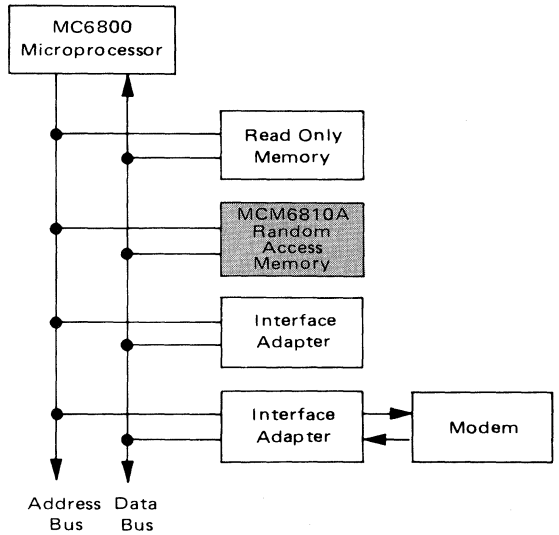


ABSOLUTE MAXIMUM RATINGS (See Note 1)

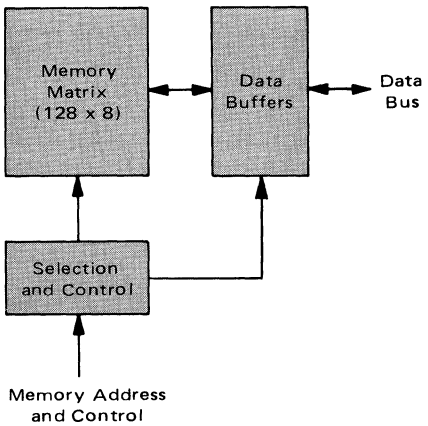
Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	-0.3 to +7.0	Vdc
Input Voltage	V_{in}	-0.3 to +7.0	Vdc
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

NOTE 1: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

M6800 MICROCOMPUTER FAMILY BLOCK DIAGRAM



MCM6810A RANDOM ACCESS MEMORY BLOCK DIAGRAM



DC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted.)

RECOMMENDED DC OPERATING CONDITIONS

Parameter	Symbol	Min	Nom	Max	Unit
Supply Voltage	V_{CC}	4.75	5.0	5.25	Vdc
Input High Voltage	V_{IH}	2.0	–	5.25	Vdc
Input Low Voltage	V_{IL}	-0.3	–	0.8	Vdc

DC CHARACTERISTICS

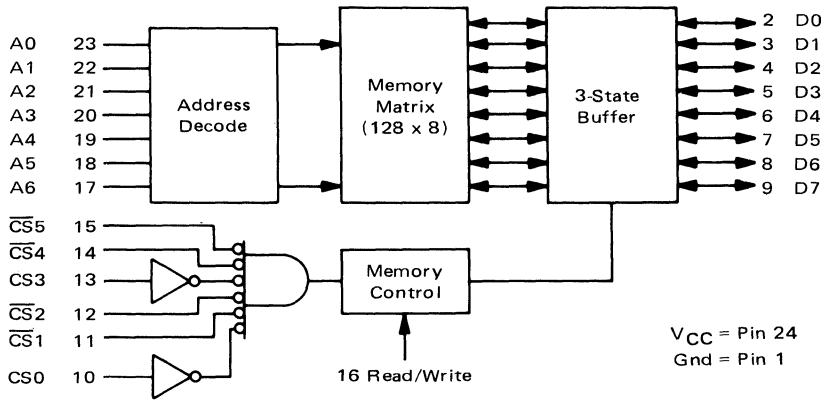
Characteristic	Symbol	Min	Typ	Max	Unit
Input Current (A_n, R/W, CS_n, $\overline{CS}_n$) (V_{in} = 0 to 5.25 V)	I_{in}	–	–	2.5	μAdc
Output High Voltage (I_{OH} = –205 μA)	V_{OH}	2.4	–	–	Vdc
Output Low Voltage (I_{OL} = 1.6 mA)	V_{OL}	–	–	0.4	Vdc
Output Leakage Current (Three-State) (CS = 0.8 V or $\overline{CS}$ = 2.0 V, V_{out} = 0.4 V to 2.4 V)	I_{LO}	–	–	10	μAdc
Supply Current (V_{CC} = 5.25 V, all other pins grounded, T_A = 0°C) MCM6810AL	I_{CC}	–	–	70	mAdc
MCM6810AL1		–	–	80	

CAPACITANCE (f = 1.0 MHz, T_A = 25°C, periodically sampled rather than 100% tested.)

Characteristic	Symbol	Max	Unit
Input Capacitance	C_{in}	7.5	pF
Output Capacitance	C_{out}	12.5	pF

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

BLOCK DIAGRAM



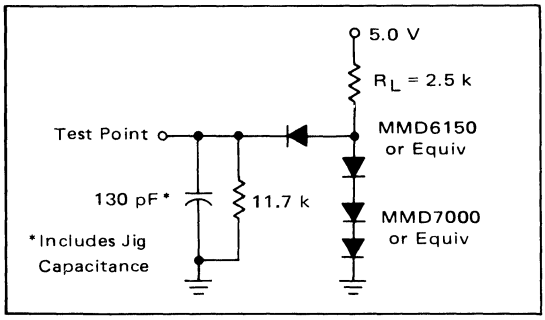
AC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature unless otherwise noted.)

AC TEST CONDITIONS

Condition	Value
Input Pulse Levels	0.8 V to 2.0 V
Input Rise and Fall Times	20 ns
Output Load	See Figure 1

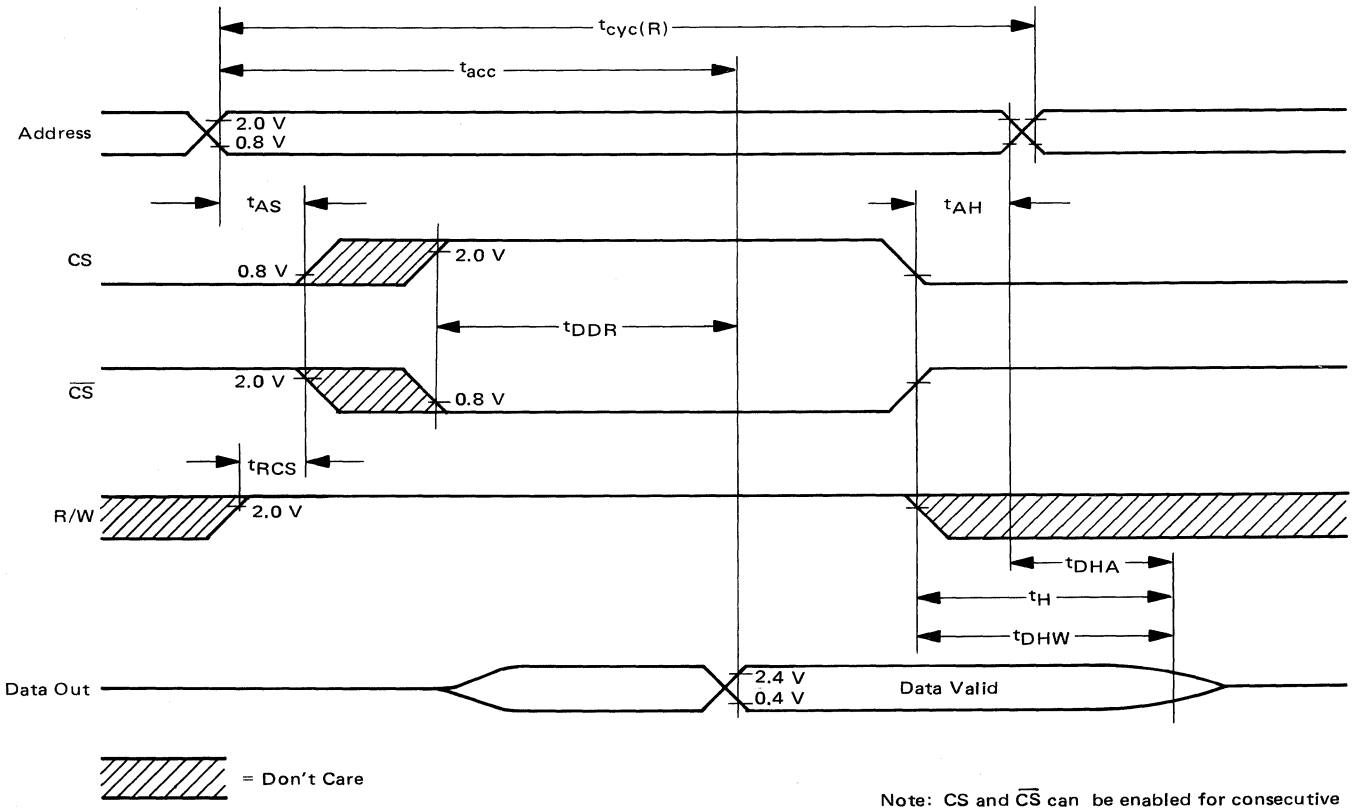
FIGURE 1 – AC TEST LOAD



READ CYCLE

Characteristic	Symbol	MCM6810AL		MCM6810AL1		Unit
		Min	Max	Min	Max	
Read Cycle Time	$t_{cyc(R)}$	450	–	350	–	ns
Access Time	t_{acc}	–	450	–	350	ns
Address Setup Time	t_{AS}	20	–	20	–	ns
Address Hold Time	t_{AH}	0	–	0	–	ns
Data Delay Time (Read)	t_{DDR}	–	230	–	180	ns
Read to Select Delay Time	t_{RCS}	0	–	0	–	ns
Data Hold from Address	t_{DHA}	10	–	10	–	ns
Output Hold Time	t_H	10	–	10	–	ns
Data Hold from Write	t_{DHW}	10	80	10	60	ns

READ CYCLE TIMING

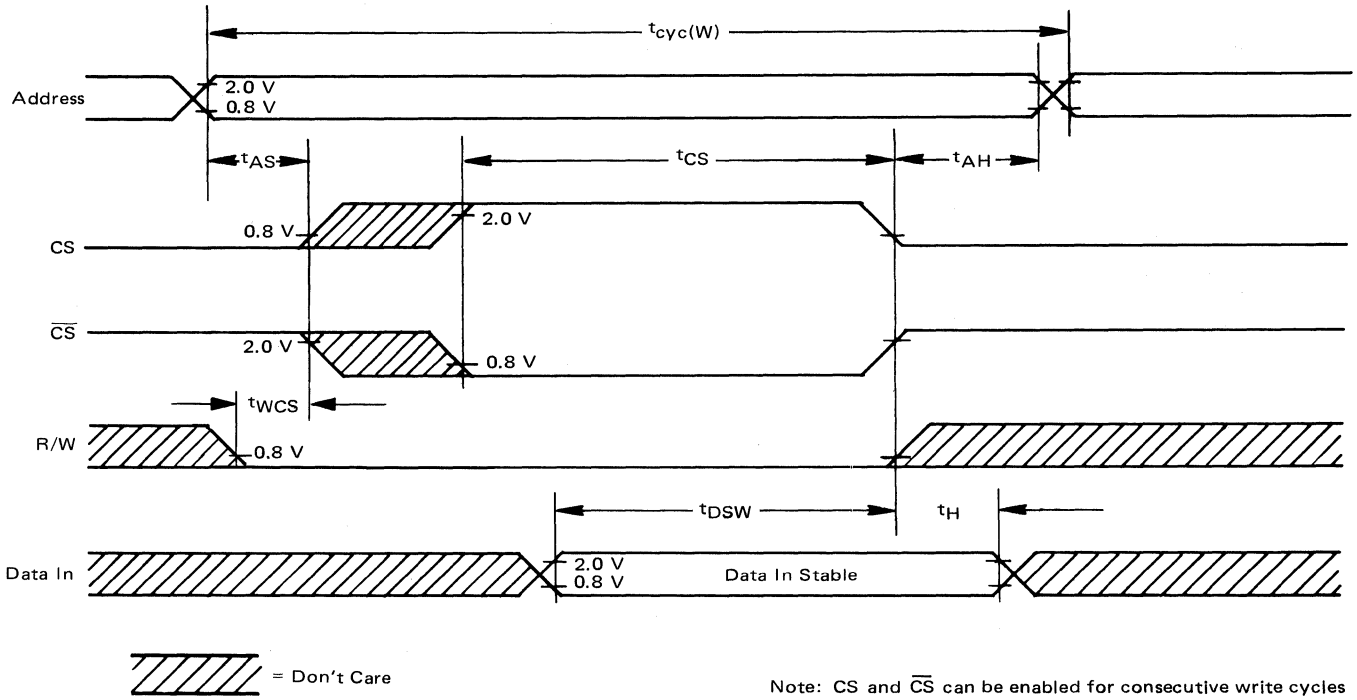


Note: CS and $\overline{CS}$ can be enabled for consecutive read cycles provided R/W remains at V_{IH}.

WRITE CYCLE

Characteristic	Symbol	MCM6810AL		MCM6810AL1		Unit
		Min	Max	Min	Max	
Write Cycle Time	$t_{cyc(W)}$	450	–	350	–	ns
Address Setup Time	t_{AS}	20	–	20	–	ns
Address Hold Time	t_{AH}	0	–	0	–	ns
Chip Select Pulse Width	t_{CS}	300	–	250	–	ns
Write to Chip Select Delay Time	t_{WCS}	0	–	0	–	ns
Data Setup Time (Write)	t_{DSW}	190	–	150	–	ns
Input Hold Time	t_H	10	–	10	–	ns

WRITE CYCLE TIMING



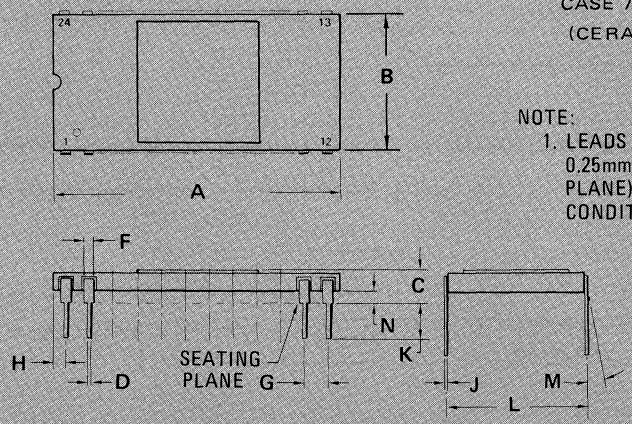
= Don't Care

Note: CS and $\overline{CS}$ can be enabled for consecutive write cycles provided R/W is strobed to V_{IH} before or coincident with the Address change, and remains high for time t_{AS}.

PACKAGE DIMENSIONS

CASE 716-02
(CERAMIC)

See Page 165 for Plastic Package dimensions.



NOTE:
1. LEADS TRUE POSITIONED WITHIN 0.25mm (0.010) DIA (AT SEATING PLANE) AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	29.97	30.99	1.180	1.220
B	14.88	15.62	0.585	0.615
C	3.05	4.19	0.120	0.165
D	0.38	0.53	0.015	0.021
F	0.76	1.40	0.030	0.055
G	2.54 BSC		0.100 BSC	
H	0.76	1.78	0.030	0.070
J	0.20	0.30	0.008	0.012
K	2.54	4.19	0.100	0.165
L	14.88	15.37	0.585	0.605
M	–	10^0	–	10^0
N	0.51	1.52	0.020	0.060

MOTOROLA Semiconductors
BOX 20912 • PHOENIX, ARIZONA 85036

MCM6830A

Advance Information

MOS

(N-CHANNEL, SILICON-GATE)

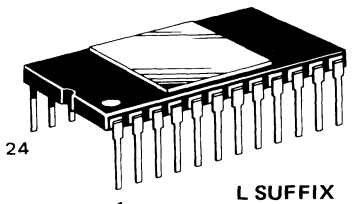
1024 X 8-BIT
READ ONLY MEMORY

1024 X 8-BIT READ ONLY MEMORY

The MCM6830A is a mask-programmable byte-organized memory designed for use in bus-organized systems. It is fabricated with N-channel silicon-gate technology. For ease of use, the device operates from a single power supply, has compatibility with TTL and DTL, and needs no clocks or refreshing because of static operation.

The memory is compatible with the M6800 Microcomputer Family, providing read only storage in byte increments. Memory expansion is provided through multiple Chip Select inputs. The active level of the Chip Select inputs and the memory content are defined by the customer.

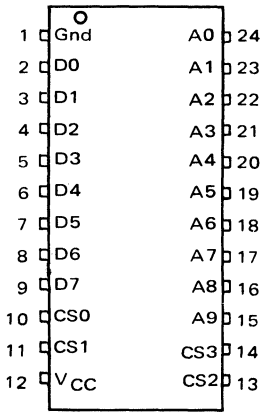
- Organized as 1024 Bytes of 8 Bits
- Static Operation
- Three-State Data Output
- Four Chip Select Inputs (Programmable)
- Single 5-Volt Power Supply
- TTL Compatible
- Maximum Access Time = 500 ns



L SUFFIX
CERAMIC PACKAGE
CASE 716

NOT SHOWN: **P SUFFIX**
PLASTIC PACKAGE
CASE 709

PIN ASSIGNMENT

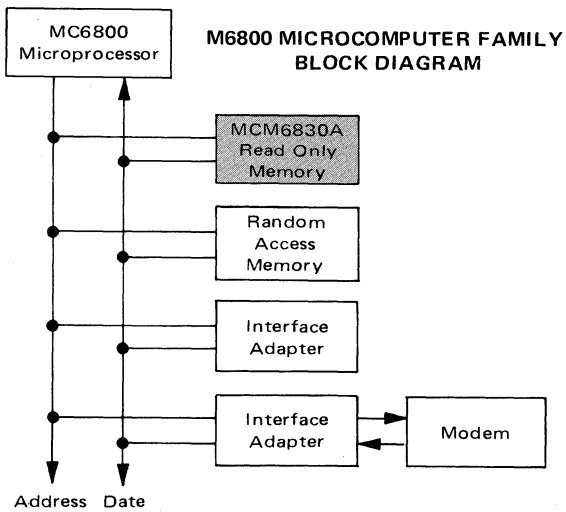


ABSOLUTE MAXIMUM RATINGS (See Note 1)

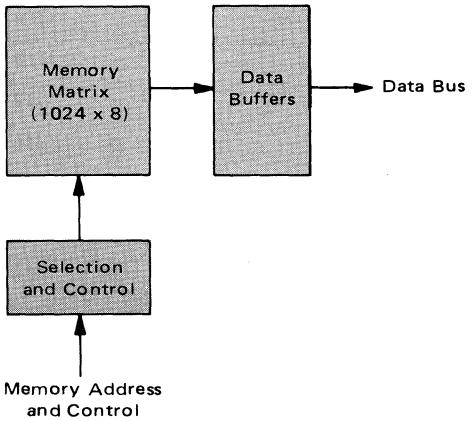
Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	-0.3 to +7.0	Vdc
Input Voltage	V_{in}	-0.3 to +7.0	Vdc
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

NOTE 1: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

M6800 MICROCOMPUTER FAMILY BLOCK DIAGRAM



MCM6830A READ ONLY MEMORY BLOCK DIAGRAM



DC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted.)

RECOMMENDED DC OPERATING CONDITIONS

Parameter	Symbol	Min	Nom	Max	Unit
Supply Voltage	V_{CC}	4.75	5.0	5.25	Vdc
Input High Voltage	V_{IH}	2.0	–	5.25	Vdc
Input Low Voltage	V_{IL}	-0.3	–	0.8	Vdc

DC CHARACTERISTICS

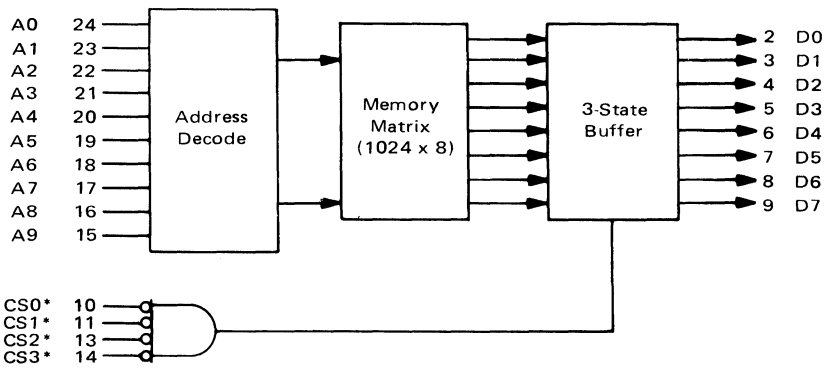
Characteristic	Symbol	Min	Typ	Max	Unit
Input Current (V_{in} = 0 to 5.25 V)	I_{in}	–	–	2.5	μAdc
Output High Voltage (I_{OH} = −205μA)	V_{OH}	2.4	–	–	Vdc
Output Low Voltage (I_{OL} = 1.6 mA)	V_{OL}	–	–	0.4	Vdc
Output Leakage Current (Three-State) (CS = 0.8 V or $\overline{CS}$ = 2.0 V, V_{out} = 0.4 V to 2.4 V)	I_{LO}	–	–	10	μAdc
Supply Current (V_{CC} = 5.25 V, T_A = 0°C)	I_{CC}	–	–	130	mAdc

CAPACITANCE (f = 1.0 MHz, T_A = 25°C, periodically sampled rather than 100% tested.)

Characteristic	Symbol	Max	Unit
Input Capacitance	C_{in}	7.5	pF
Output Capacitance	C_{out}	12.5	pF

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

BLOCK DIAGRAM



*Active level defined by the customer.

V_{CC} = Pin 12
Gnd = Pin 1

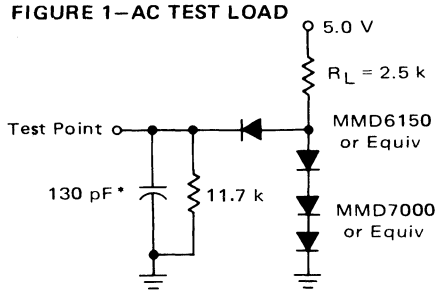
AC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature unless otherwise noted.)

(All timing with $t_r = t_f = 20$ ns, Load of Figure 1)

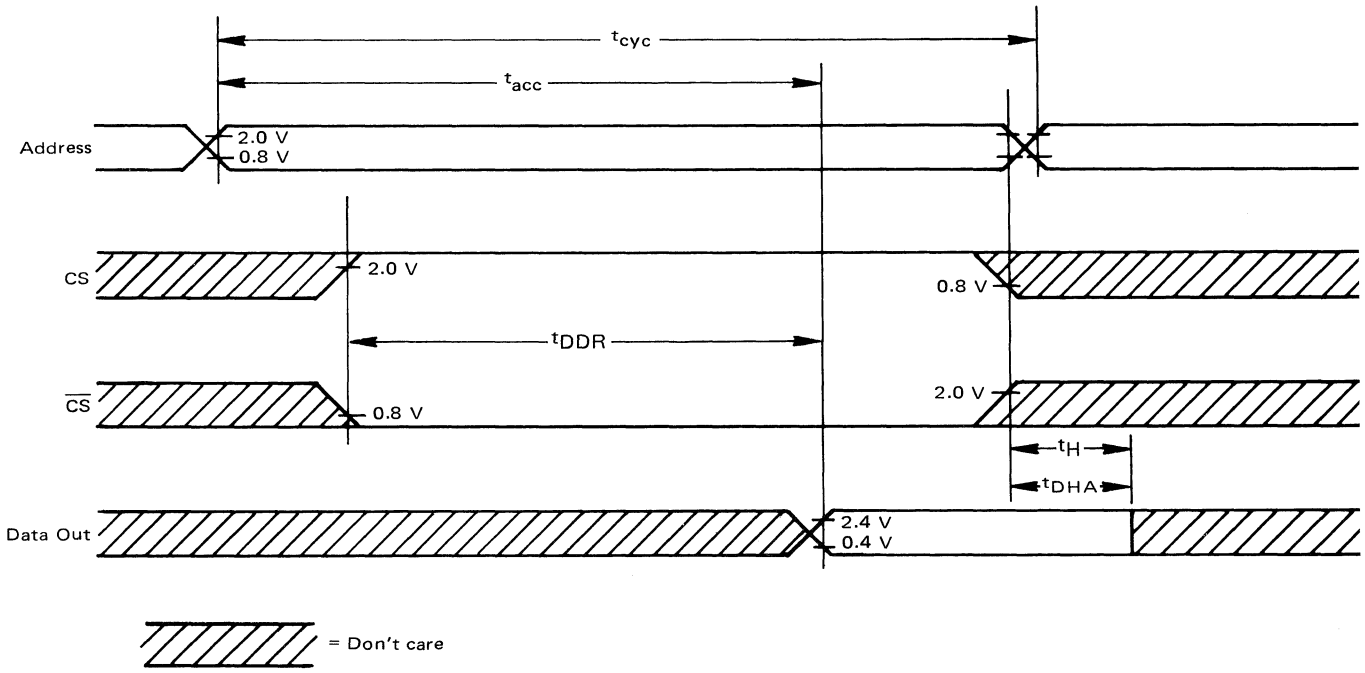
Characteristic	Symbol	Min	Max	Unit
Cycle Time	t_{cyc}	500	—	ns
Access Time	t_{acc}	—	500	ns
Data Delay Time (Read)	t_{DDR}	—	300	ns
Data Hold from Address	t_{DHA}	10	—	ns
Data Hold from Deselection	t_H	10	150	ns

FIGURE 1—AC TEST LOAD



*Includes Jig Capacitance

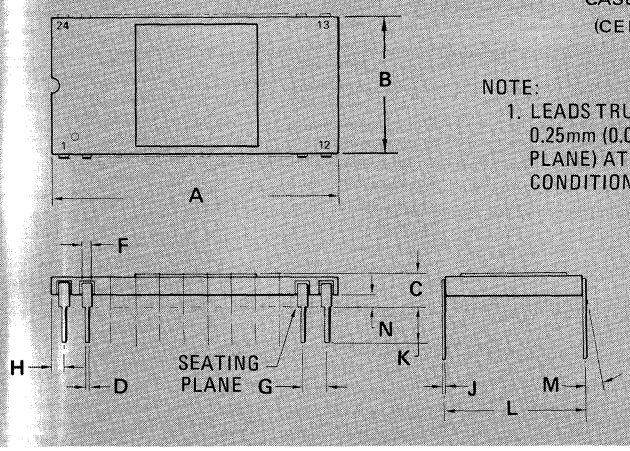
TIMING DIAGRAM



= Don't care

PACKAGE DIMENSIONS

CASE 716-02
(CERAMIC)



NOTE:
1. LEADS TRUE POSITIONED WITHIN 0.25mm (0.010) DIA (AT SEATING PLANE) AT MAXIMUM MATERIAL CONDITION.

See Page 165 for Plastic Package dimensions.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	29.97	30.99	1.180	1.220
B	14.88	15.62	0.585	0.615
C	3.05	4.19	0.120	0.165
D	0.38	0.53	0.015	0.021
F	0.76	1.40	0.030	0.055
G	2.54 BSC		0.100 BSC	
H	0.76	1.78	0.030	0.070
J	0.20	0.30	0.008	0.012
K	2.54	4.19	0.100	0.165
L	14.88	15.37	0.585	0.605
M	—	10^0	—	10^0
N	0.51	1.52	0.020	0.060

CUSTOM PROGRAMMING

By the programming of a single photomask for the MCM6830A, the customer may specify the content of the memory and the method of enabling the outputs.

Information on the general options of the MCM6830A should be submitted on an Organizational Data form such as that shown in Figure 3.

Information for custom memory content may be sent to Motorola in one of two forms (shown in order of preference):

1. Paper tape output of the Motorola M6800 Software.
2. Hexadecimal coding using IBM Punch Cards.

PAPER TAPE

Included in the software packages developed for the M6800 Micromputer Family is the ability to produce a paper tape output for computerized mask generation. The assembler directives are used to control allocation of memory, to assign values for stored data, and for controlling the assembly process. The paper tape must specify the full 1024 bytes.

Note: Motorola can accept magnetic tape and truth table table formats. For further information, contact your local Motorola sales representative.

FIGURE 2 – BINARY TO HEXADECIMAL CONVERSION

Binary Data				Hexadecimal Character
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	A
1	0	1	1	B
1	1	0	0	C
1	1	0	1	D
1	1	1	0	E
1	1	1	1	F

IBM PUNCH CARDS

The hexadecimal equivalent (from Figure 2) may be placed on 80 column IBM punch cards as follows:

Step	Column	
1	12	Byte "0" Hexadecimal equivalent for outputs D7 thru D4 (D7 = M.S.B.)
2	13	Byte "0" Hexadecimal equivalent for outputs D3 thru D0 (D3 = M.S.B.)
3	14-75	Alternate steps 1 and 2 for consecutive bytes.
4	77-78	Card number (starting 01)
5	79-80	Total number of cards (32)

FIGURE 3 – FORMAT FOR PROGRAMMING GENERAL OPTIONS

ORGANIZATIONAL DATA
MCM6830A MOS READ ONLY MEMORY

Customer:

Company _____

Part No. _____

Originator _____

Phone No. _____

Motorola Use Only:

Quote: _____

Part No.: _____

Specif. No.: _____

Enable Options:

	1	0
CS0	☐	☐
CS1	☐	☐
CS2	☐	☐
CS3	☐	☐

1 is most positive
0 is most negative

MOTOROLA Semiconductors
BOX 20912 • PHOENIX, ARIZONA 85036

MCM6832

Advance Information

MOS

(N-CHANNEL, LOW THRESHOLD)

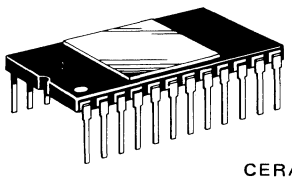
2048 x 8-BIT
READ ONLY MEMORY

2048 x 8-BIT READ ONLY MEMORY

The MCM6832 is a mask-programmable byte-organized memory designed for use in bus-organized systems. It is fabricated with N-channel metal-gate technology. For ease of use, the device is compatible with TTL and DTL, and needs no clocks or refreshing because of static operation.

The memory is compatible with the M6800 Microcomputer Family, providing read only storage in byte increments. Memory expansion is provided through a Chip Select input. The active level of the Chip Select input and the memory content are defined by the customer.

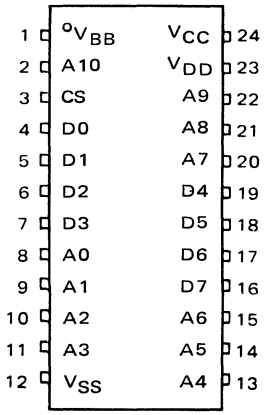
- Organized as 2048 Bytes of 8 Bits
- Static Operation
- Three-State Data Output
- Programmable Chip Select
- TTL Compatible
- Maximum Access Time = 500 ns



L SUFFIX
CERAMIC PACKAGE
CASE 716

NOT SHOWN: **P SUFFIX**
PLASTIC PACKAGE
CASE 709

PIN ASSIGNMENT

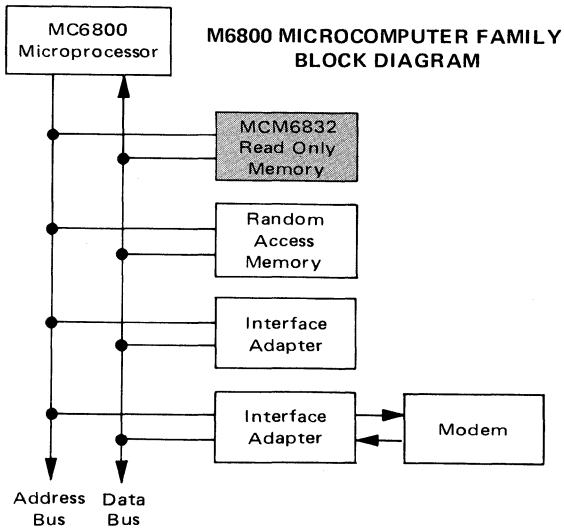


ABSOLUTE MAXIMUM RATINGS[1] (Referenced to V_{SS})

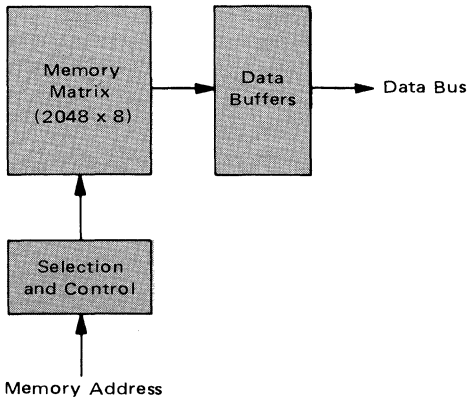
Rating	Symbol	Value	Unit
Supply Voltages	V_{DD} V_{CC} V_{BB}	-0.3 to +15 -0.3 to +6.0 -10 to +0.3	Vdc
Address/Control Input Voltage	V_{in}	-0.3 to +15	Vdc
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	-55 to +125	°C

Note 1: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

M6800 MICROCOMPUTER FAMILY
BLOCK DIAGRAM



MCM6832 READ ONLY MEMORY
BLOCK DIAGRAM



DC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted.)

RECOMMENDED DC OPERATING CONDITIONS (Referenced to V_{SS} = Ground)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{DD}	11.4	12	12.6	Vdc
	V_{CC}	4.75	5.0	5.25	Vdc
	V_{BB}	-5.25	-5.0	-4.75	Vdc
Input High Voltage (A_n, CS)	V_{IH}	3.0	–	V_{CC}	Vdc
Input Low Voltage (A_n, CS)	V_{IL}	-0.3	–	0.8	Vdc

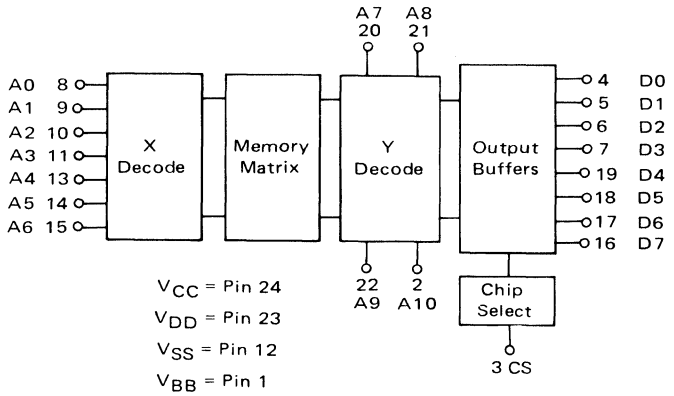
DC CHARACTERISTICS

Characteristic	Symbol	Min	Typ	Max	Unit
Input Leakage Current (A_n, CS) (V_{in} = 0 to 5.25 V)	I_{in}	–	–	10	μAdc
Output Leakage Current (Three-State) (V_O = 0.4 V to -2.4 V, CS = 0.4 V or $\overline{CS}$ = 2.4 V)	I_{LO}	–	–	10	μAdc
Output High Voltage (I_{OH} = -100 μA)	V_{OH}	3.7	–	V_{CC}	Vdc
Output Low Voltage (I_{OL} = 1.6 mA)	V_{OL}	0	–	0.4	Vdc
Supply Current (Chip Deselected or Selected)	I_{DD}	–	–	25	mAdc
	I_{CC}	–	–	45	mAdc
	I_{BB}	–	–	500	μAdc

CAPACITANCE (Periodically Sampled Rather Than 100% Tested.)

Characteristic	Symbol	Min	Typ	Max	Unit
Input Capacitance (f = 1 MHz)	C_{in}	–	5.0	7.5	pF
Output Capacitance (f = 1 MHz)	C_{out}	–	5.0	10	pF

BLOCK DIAGRAM



AC CHARACTERISTICS

(Full operating voltage and temperature unless otherwise noted. All timing with $t_r = t_f \leqslant 20$ ns; Load = 1 TTL Gate (MC7400 Series) biased to draw 1.6 mA; C_L = 130 pF.)

Characteristic	Symbol	Min	Typ*	Max	Unit
Address Access Time	t_{acc}	–	320*	500	ns
Output Select Time	t_{OS}	–	175*	300	ns
Output Deselect Time	t_{OD}	30	100*	150	ns

*Typical values measured at 25°C and nominal supply voltages.

FIGURE 1 – AC TEST LOAD

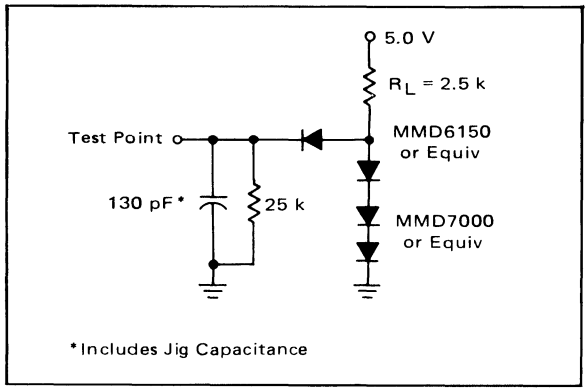
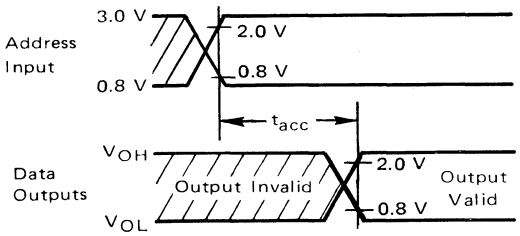
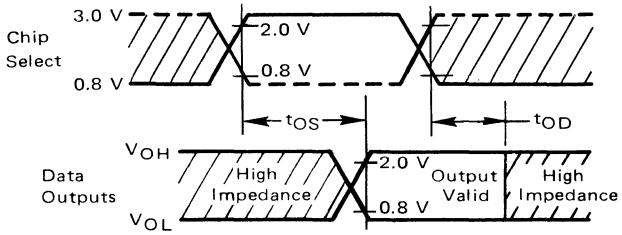


FIGURE 2 – TIMING DIAGRAM

A. ADDRESS ACCESS TIMING DIAGRAM
(Chip Selected)

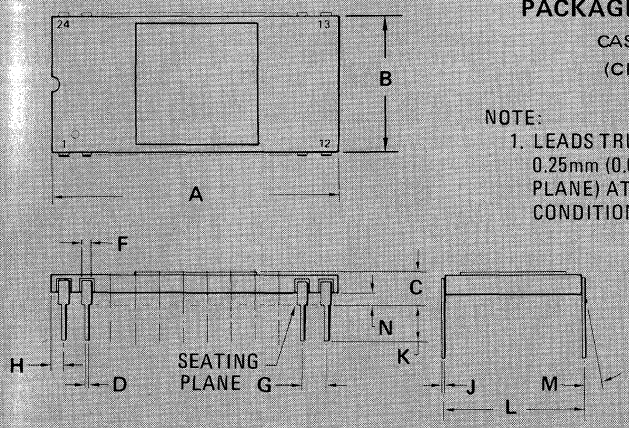


B. CHIP SELECT TIMING DIAGRAM
(Addresses Established)



PACKAGE DIMENSIONS

CASE 716-02
(CERAMIC)



NOTE:
1. LEADS TRUE POSITIONED WITHIN 0.25mm (0.010) DIA (AT SEATING PLANE) AT MAXIMUM MATERIAL CONDITION.

SEE PAGE 165 FOR PLASTIC PACKAGE DIMENSIONS.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	29.97	30.99	1.180	1.220
B	14.88	15.62	0.585	0.615
C	3.05	4.19	0.120	0.165
D	0.38	0.53	0.015	0.021
F	0.76	1.40	0.030	0.055
G	2.54 BSC		0.100 BSC	
H	0.76	1.78	0.030	0.070
J	0.20	0.30	0.008	0.012
K	2.54	4.19	0.100	0.165
L	14.88	15.37	0.585	0.605
M	–	10°	–	10°
N	0.51	1.52	0.020	0.060

CUSTOM PROGRAMMING

By the programming of a single photomask for the MCM6832, the customer may specify the content of the memory and the method of enabling the outputs.

Information on the general options of the MCM6832 should be submitted on an Organizational Data form such as that shown in Figure 4.

Information for custom memory content may be sent to Motorola in one of two forms (shown in order of preference):

1. Paper tape output of the Motorola M6800 Software.
2. Hexadecimal coding using IBM Punch Cards.

PAPER TAPE

Included in the software packages developed for the M6800 Microcomputer Family is the ability to produce a paper tape output for computerized mask generation. The assembler directives are used to control allocation of memory, to assign values for stored data, and for controlling the assembly process. The paper tape must specify the full 2048 bytes.

Note: Motorola can accept magnetic tape and truth table table formats. For further information, contact your local Motorola sales representative.

FIGURE 3 – BINARY TO HEXADECIMAL CONVERSION

MSB D7 D3	D6 D2	D5 D1	LSB D4 D0	Hexadecimal Character
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	A
1	0	1	1	B
1	1	0	0	C
1	1	0	1	D
1	1	1	0	E
1	1	1	1	F

$0 = V_{OL}$
$1 = V_{OH}$

IBM PUNCH CARDS

The hexadecimal equivalent (from Figure 3) may be placed on 80 column IBM punch cards as follows:

Step	Column	
1	12	Byte "0" Hexadecimal equivalent for outputs D7 thru D4 (D7 = M.S.B.)
2	13	Byte "0" Hexadecimal equivalent for outputs D3 thru D0 (D3 = M.S.B.)
3	14-75	Alternate steps 1 and 2 for consecutive bytes.
4	77-78	Card number (starting 01)
5	79-80	Total number of cards (64)

FIGURE 4 – FORMAT FOR PROGRAMMING GENERAL OPTIONS

ORGANIZATIONAL DATA
MCM6832 MOS READ ONLY MEMORY

Customer:

Company _____

Part No. _____

Originator _____

Phone No. _____

Motorola Use Only:

Quote: _____

Part No.: _____

Specif. No.: _____

True Chip Select Options:

I. 1 ☐

II. 0 ☐

1 is most positive
0 is most negative

MOTOROLA Semiconductors
BOX 20912 • PHOENIX, ARIZONA 85036

MCM68308

Advance Information

MOS

(N-CHANNEL, SILICON-GATE)

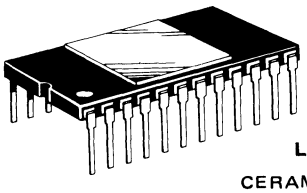
1024 X 8-BIT
READ ONLY MEMORY

1024 X 8-BIT READ ONLY MEMORY

The MCM68308 is a mask-programmable byte-organized memory designed for use in bus-organized systems. It is fabricated with N-channel silicon-gate technology. For ease of use, the device operates from a single power supply, has compatibility with TTL and DTL, and needs no clocks or refreshing because of static operation.

The memory is compatible with the M6800 Microcomputer Family, providing read only storage in byte increments. Memory expansion is provided through multiple Chip Select inputs. The active level of the Chip Select inputs and the memory content are defined by the customer.

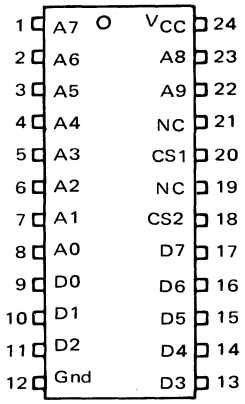
- Static Operation
- Three-State Data Output
- Mask-Programmable Chip Selects for Simplified Memory Expansion
- Single 5-Volt Power Supply
- TTL Compatible
- Maximum Access Time = 500 ns
- Pin Compatible with MCM68708 Alterable ROM
- Pin Compatible with MCM68317 2048 x 8-Bit ROM



L SUFFIX
CERAMIC PACKAGE
CASE 716

NOT SHOWN: **P SUFFIX**
PLASTIC PACKAGE
CASE 709

PIN ASSIGNMENT

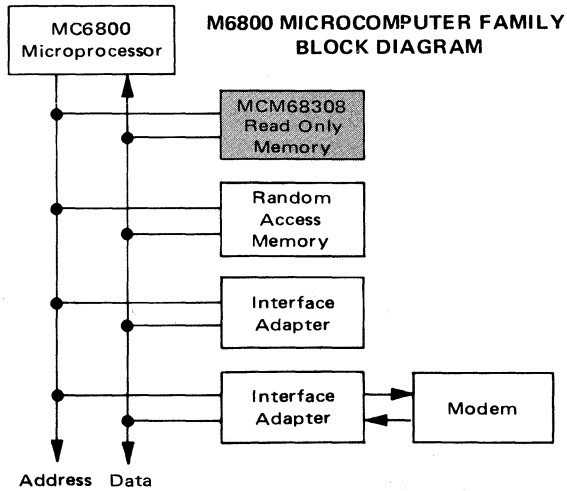


ABSOLUTE MAXIMUM RATINGS (See Note 1)

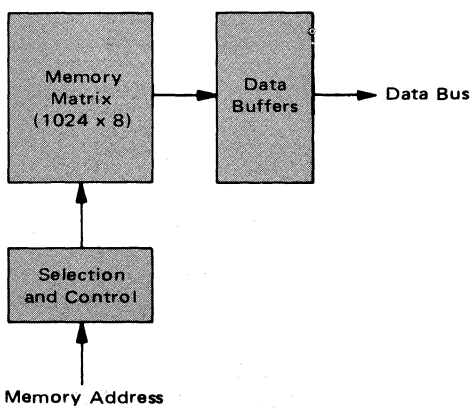
Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	-0.3 to +7.0	Vdc
Input Voltage	V_{in}	-0.3 to +7.0	Vdc
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

NOTE 1: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

M6800 MICROCOMPUTER FAMILY BLOCK DIAGRAM



MCM68308 READ ONLY MEMORY BLOCK DIAGRAM



DC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted.)

RECOMMENDED DC OPERATING CONDITIONS

Parameter	Symbol	Min	Nom	Max	Unit
Supply Voltage	V_{CC}	4.75	5.0	5.25	Vdc
Input High Voltage	V_{IH}	2.0	–	5.25	Vdc
Input Low Voltage	V_{IL}	-0.3	–	0.8	Vdc

DC CHARACTERISTICS

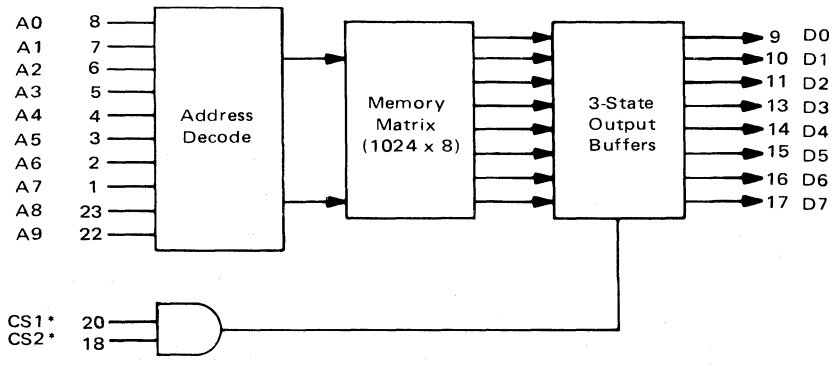
Characteristic	Symbol	Min	Typ	Max	Unit
Input Current (V_{in} = 0 to 5.25 V)	I_{in}	–	–	2.5	μAdc
Output High Voltage (I_{OH} = −205μA)	V_{OH}	2.4	–	–	Vdc
Output Low Voltage (I_{OL} = 1.6 mA)	V_{OL}	–	–	0.4	Vdc
Output Leakage Current (Three-State) (CS = 0.8 V or $\overline{CS}$ = 2.0 V, V_{out} = 0.4 V to 2.4 V)	I_{LO}	–	–	10	μAdc
Supply Current (V_{CC} = 5.25 V, T_A = 0°C)	I_{CC}	–	–	130	mAdc

CAPACITANCE (f = 1.0 MHz, T_A = 25°C, periodically sampled rather than 100% tested.)

Characteristic	Symbol	Max	Unit
Input Capacitance	C_{in}	7.5	pF
Output Capacitance	C_{out}	12.5	pF

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

BLOCK DIAGRAM



*Active level defined by the customer.

V_{CC} = Pin 24
Gnd = Pin 12

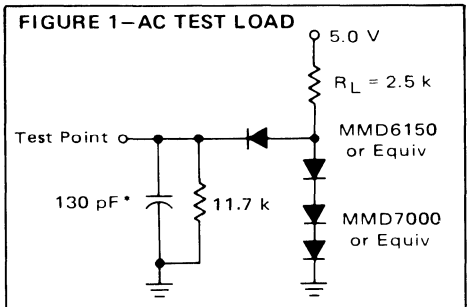
AC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature unless otherwise noted.)

(All timing with $t_r = t_f = 20$ ns, Load of Figure 1)

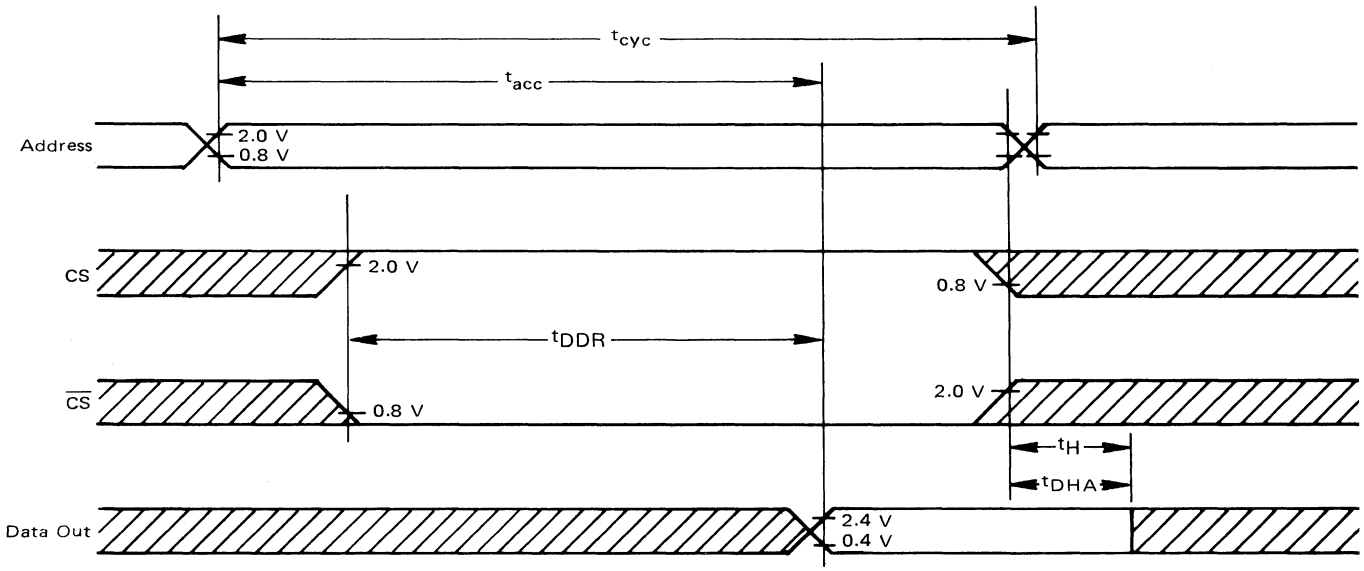
Characteristic	Symbol	Min	Max	Unit
Cycle Time	t_{cyc}	500	—	ns
Access Time	t_{acc}	—	500	ns
Data Delay Time (Read)	t_{DDR}	—	300	ns
Data Hold from Address	t_{DHA}	10	—	ns
Data Hold from Deselection	t_H	10	150	ns

FIGURE 1—AC TEST LOAD



*Includes Jig Capacitance

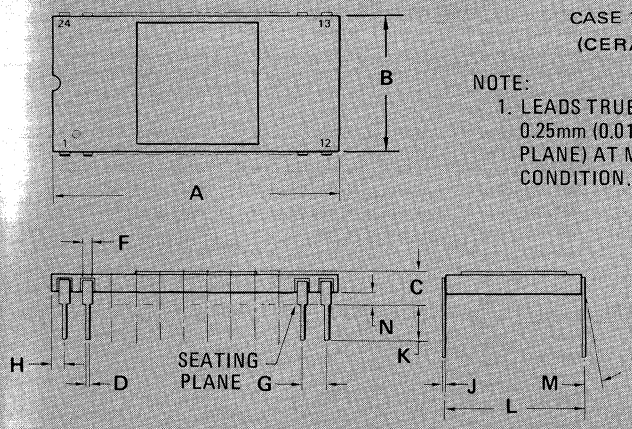
TIMING DIAGRAM



= Don't care

PACKAGE DIMENSIONS

CASE 716-02
(CERAMIC)



NOTE:
1. LEADS TRUE POSITIONED WITHIN 0.25mm (0.010) DIA (AT SEATING PLANE) AT MAXIMUM MATERIAL CONDITION.

SEE PAGE 165 FOR PLASTIC PACKAGE DIMENSIONS.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	29.97	30.99	1.180	1.220
B	14.88	15.62	0.585	0.615
C	3.05	4.19	0.120	0.165
D	0.38	0.53	0.015	0.021
F	0.76	1.40	0.030	0.055
G	2.54 BSC		0.100 BSC	
H	0.76	1.78	0.030	0.070
J	0.20	0.30	0.008	0.012
K	2.54	4.19	0.100	0.165
L	14.88	15.37	0.585	0.605
M	—	10^0	—	10^0
N	0.51	1.52	0.020	0.060

CUSTOM PROGRAMMING

By the programming of a single photomask for the MCM68308, the customer may specify the content of the memory and the method of enabling the outputs.

Information on the general options of the MCM68308 should be submitted on an Organizational Data form such as that shown in Figure 3.

Information for custom memory content may be sent to Motorola in one of two forms (shown in order of preference):

1. Paper tape output of the Motorola M6800 Software.
2. Hexadecimal coding using IBM Punch Cards.

PAPER TAPE

Included in the software packages developed for the M6800 Microcomputer Family is the ability to produce a paper tape output for computerized mask generation. The assembler directives are used to control allocation of memory, to assign values for stored data, and for controlling the assembly process. The paper tape must specify the full 1024 bytes.

Note: Motorola can accept magnetic tape and truth table table formats. For further information, contact your local Motorola sales representative.

FIGURE 2 – BINARY TO HEXADECIMAL CONVERSION

Binary Data				Hexadecimal Character
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	A
1	0	1	1	B
1	1	0	0	C
1	1	0	1	D
1	1	1	0	E
1	1	1	1	F

IBM PUNCH CARDS

The hexadecimal equivalent (from Figure 2) may be placcd on 80 column IBM punch cards as follows:

Step	Column	
1	12	Byte "0" Hexadecimal equivalent for outputs D7 thru D4 (D7 = M.S.B.)
2	13	Byte "0" Hexadecimal equivalent for outputs D3 thru D0 (D3 = M.S.B.)
3	14-75	Alternate steps 1 and 2 for consecutive bytes.
4	77-78	Card number (starting 01)
5	79-80	Total number of cards (32)

FIGURE 3 – FORMAT FOR PROGRAMMING GENERAL OPTIONS

ORGANIZATIONAL DATA
MCM68308 MOS READ ONLY MEMORY

Customer:

Company _____

Part No. _____

Originator _____

Phone No. _____

Motorola Use Only:

Quote: _____

Part No.: _____

Specif. No.: _____

Enable Options:

	1	0
CS1	☐	☐
CS2	☐	☐

1 is most positive
0 is most negative

MOTOROLA
Semiconductors
3501 ED BLUESTEIN BLVD., AUSTIN, TEXAS 78721

MCM68316E
MCM68316E1

Advance Information

MOS

(N-CHANNEL, SILICON-GATE)

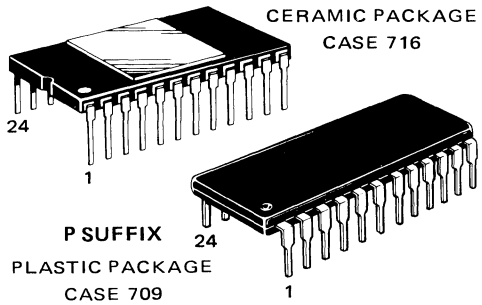
2048 X 8-BIT
READ ONLY MEMORY

2048 X 8-BIT READ ONLY MEMORY

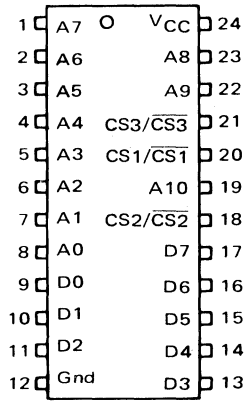
The MCM68316E is a mask-programmable byte-organized memory designed for use in bus-organized systems. It is fabricated with N-channel silicon-gate technology. For ease of use, the device operates from a single power supply, has compatibility with TTL and DTL, and needs no clocks or refreshing because of static operation.

The memory is compatible with the M6800 Microcomputer Family, providing read only storage in byte increments. Memory expansion is provided through multiple Chip Select inputs. The active level of the Chip Select inputs and the memory content are defined by the user.

- Static Operation
- Two Temperature Range Options
- Three-State Data Output
- Mask-Programmable Chip Selects for Simplified Memory Expansion
- Single 5-Volt Power Supply
- TTL Compatible
- Maximum Access Time = 500 ns
- Directly Compatible with 2316E
- Pin Compatible with 2708 PROM



PIN ASSIGNMENT

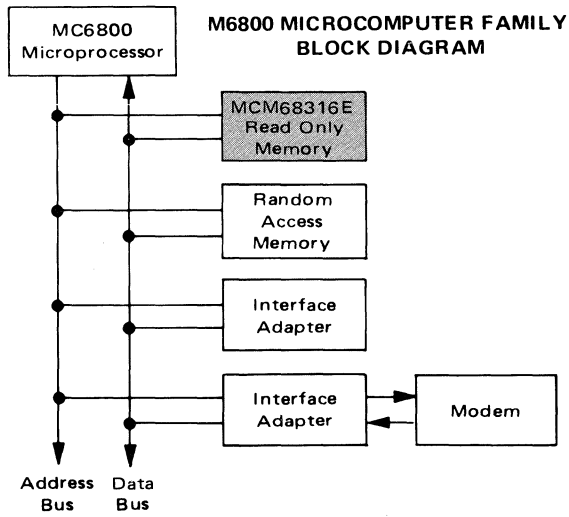


ABSOLUTE MAXIMUM RATINGS (See Note 1)

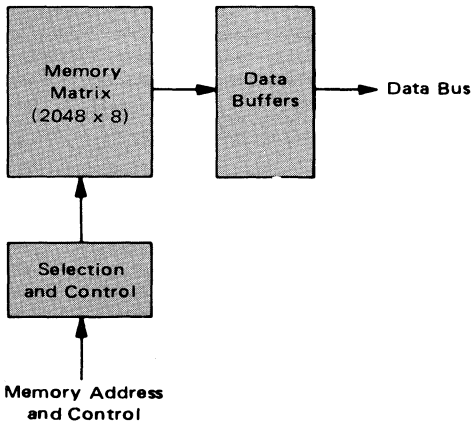
Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	-0.3 to +7.0	Vdc
Input Voltage	V_{in}	-0.3 to +7.0	Vdc
Operating Temperature Range — MCM68316E1 MCM68316E	T_A	-40 to +85 0 to +70	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

NOTE 1: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

M6800 MICROCOMPUTER FAMILY BLOCK DIAGRAM



MCM68316E READ ONLY MEMORY BLOCK DIAGRAM



DC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted.)

RECOMMENDED DC OPERATING CONDITIONS

Parameter	Symbol	Min	Nom	Max	Unit
Supply Voltage	V_{CC}	4.75	5.0	5.25	Vdc
Input High Voltage	V_{IH}	2.0	–	5.25	Vdc
Input Low Voltage	V_{IL}	-0.3	–	0.8	Vdc

DC CHARACTERISTICS

Characteristic	Symbol	Min	Typ	Max	Unit
Input Current (V_{in} = 0 to 5.25 V)	I_{in}	–	–	2.5	μAdc
Output High Voltage (I_{OH} = −205μA)	V_{OH}	2.4	–	–	Vdc
Output Low Voltage (I_{OL} = 1.6 mA)	V_{OL}	–	–	0.4	Vdc
Output Leakage Current (Three-State) (CS = 0.8 V or $\overline{CS}$ = 2.0 V, V_{out} = 0.4 V to 2.4 V)	I_{LO}	–	–	10	μAdc
Supply Current (V_{CC} = 5.25 V, T_A = 0°C)	I_{CC}	–	–	130	mAdc

CAPACITANCE (f = 1.0 MHz, T_A = 25°C, periodically sampled rather than 100% tested.)

Characteristic	Symbol	Max	Unit
Input Capacitance	C_{in}	7.5	pF
Output Capacitance	C_{out}	12.5	pF

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

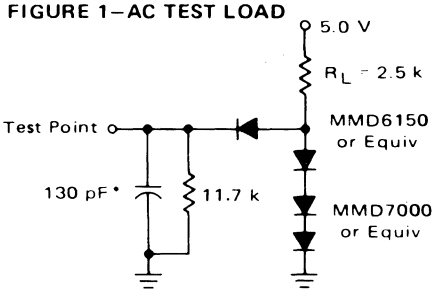
AC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature unless otherwise noted.)

(All timing with $t_r = t_f$ = 20 ns, Load of Figure 1)

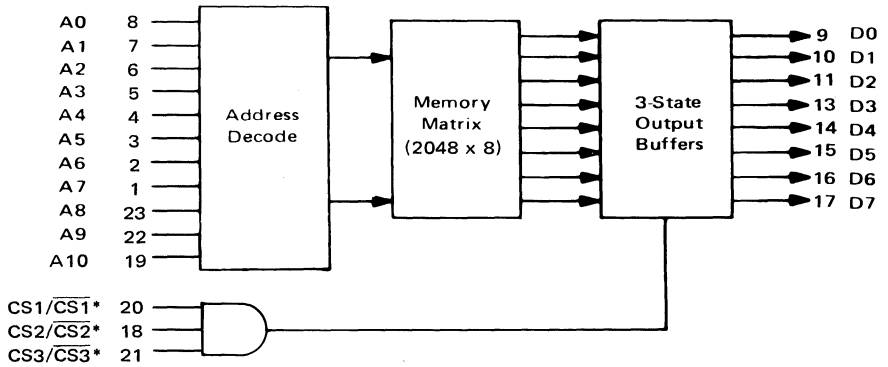
Characteristic	Symbol	Min	Max	Unit
Cycle Time	t_{cyc}	500	–	ns
Access Time	t_{acc}	–	500	ns
Chip Select to Output Delay	t_{CO}	–	300	ns
Data Hold from Address	t_{DHA}	10	–	ns
Data Hold from Deselection	t_H	10	150	ns

FIGURE 1–AC TEST LOAD



*Includes Jig Capacitance

BLOCK DIAGRAM



* Active level defined by the user.

V_{CC} = Pin 24
Gnd = Pin 12

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BOX 20912 • PHOENIX, ARIZONA 85036

MCM68708L

Product Preview

1024 X 8-BIT ALTERABLE READ ONLY MEMORY

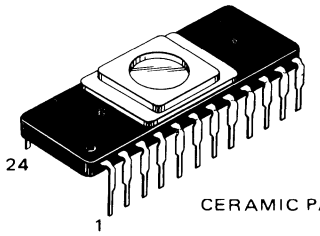
The MCM68708 is an 8192-bit Alterable Read Only Memory designed for system debug usage and similar applications requiring non-volatile memory that must be reprogrammed periodically. The transparent lid on the package allows the memory content to be erased with ultraviolet light. The memory can then be electrically reprogrammed.

- Organized as 1024 Bytes of 8-Bits
- Static Operation
- Standard Power Supplies of +12 V, +5 V, and -5 V.
- Access Time = 500 ns
- Low Power Dissipation
- Chip Select Input for Memory Expansion
- TTL Compatible
- Three-State Outputs
- Compatible with the 2708

MOS

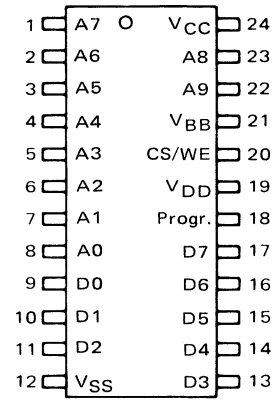
(N-CHANNEL, SILICON-GATE)

1024 X 8-BIT ALTERABLE READ ONLY MEMORY

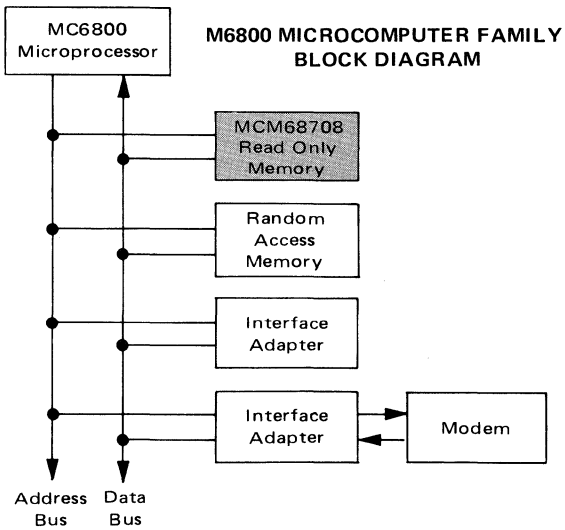


CERAMIC PACKAGE

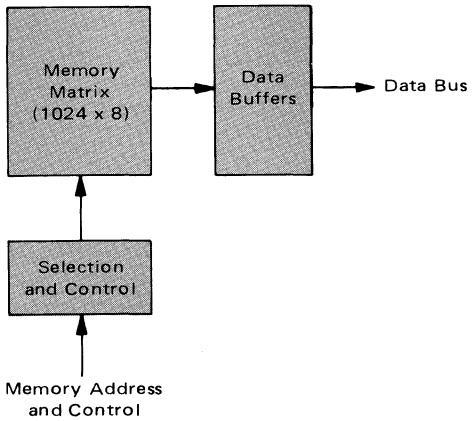
PIN ASSIGNMENT



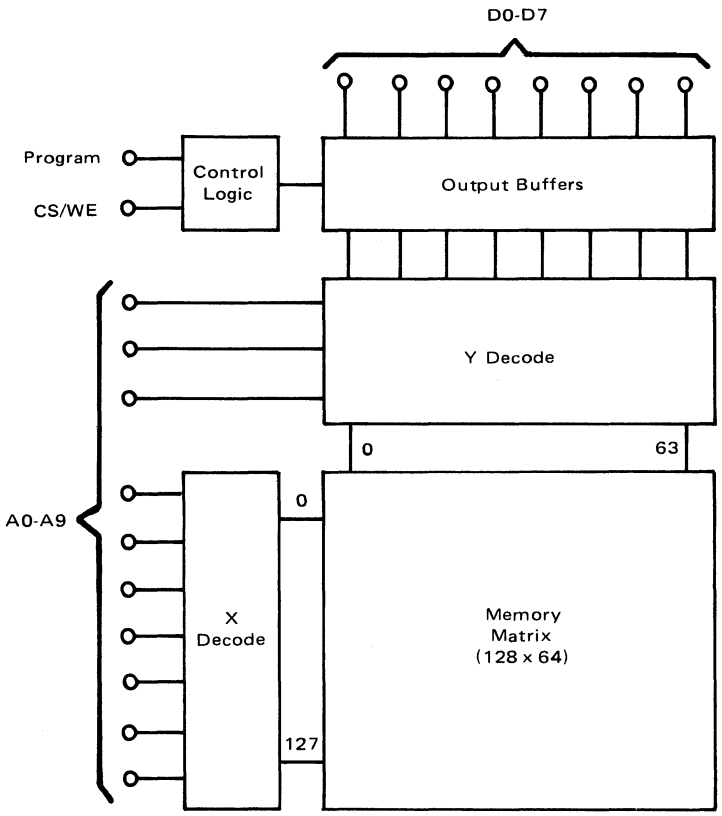
M6800 MICROCOMPUTER FAMILY BLOCK DIAGRAM



MCM68708 READ ONLY MEMORY BLOCK DIAGRAM



BLOCK DIAGRAM



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Semiconductors
BOX 20912 • PHOENIX, ARIZONA 85036

MCM6604L/L2/L4
MCM6604P/P2/P4

Advance Information

MOS
(N-CHANNEL, SILICON-GATE)

4096-BIT DYNAMIC
RANDOM ACCESS
MEMORY

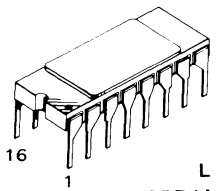
4096-BIT DYNAMIC RANDOM ACCESS MEMORY

The MCM6604 is a 4096-bit high-speed dynamic Random Access Memory designed for high-performance, low-cost applications in mainframe and buffer memories and peripheral storage. Organized as 4096 one-bit words and fabricated using Motorola's highly reliable N-channel silicon gate technology, this device optimizes speed, power, and density tradeoffs.

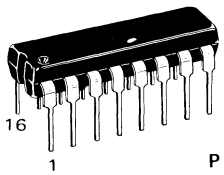
By multiplexing row and column address inputs, the MCM6604 requires only six address lines and permits packaging in Motorola's standard 16-pin dual in-line packages. Complete address decoding is done on chip with address latches incorporated.

All inputs are TTL compatible, and the output is 3-state TTL compatible. The MCM6604 incorporates a one-transistor cell design and dynamic storage techniques, with each of the 64 row addresses requiring a refresh cycle every 2.0 milliseconds.

- Organized as 4096 Words of 1 Bit
- Maximum Access Time = 250 ns (L2,P2)
  300 ns (L4,P4)
  350 ns (L,P)
- Minimum Read and Write Cycle Time =
  375 ns (L2,P2)
  425 ns (L4,P4)
  500 ns (L,P)
- Low Power Dissipation
  630 mW Maximum (Active)
  25 mW Maximum (Standby)
- TTL Compatible
- 3-State Output
- On-Chip Latches for Address, Chip Select, and Data In
- Power Supply Pins on Package Corners for Optimum Layout
- Standard 16-Pin Package
- Compatible with the Popular 2104/MK4096

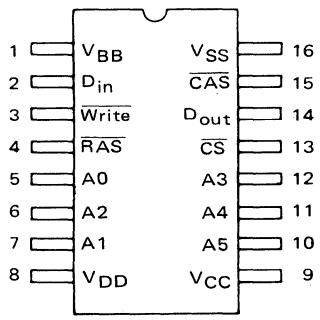


L SUFFIX
CERAMIC PACKAGE
CASE 690



P SUFFIX
PLASTIC PACKAGE
CASE 648

PIN ASSIGNMENT



ABSOLUTE MAXIMUM RATINGS (See Note 1)

Rating	Symbol	Value	Unit
Voltage on Any Pin Relative to V_{BB}	V_{in}, V_{out}	-0.3 to +20	Vdc
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

NOTE 1: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

DC OPERATING CONDITIONS AND CHARACTERISTICS
(Full operating voltage and temperature range unless otherwise noted.)

RECOMMENDED OPERATING CONDITIONS (Referenced to V_{SS} = Ground)

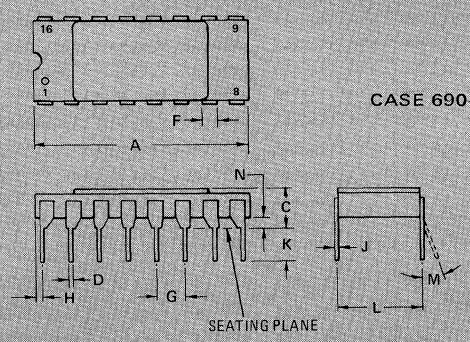
Parameter		Symbol	Min	Nom	Max	Unit
Supply Voltage		V_{DD}	11.4	12.0	12.6	Vdc
		V_{CC}	4.5	5.0	5.5	Vdc
		V_{BB}	-4.5	-5.0	-5.5	Vdc
Input High Voltage	An, $\overline{CS}$, D_{in}	V_{IH}	2.4	–	V_{CC}	Vdc
	$\overline{RAS}$, $\overline{CAS}$, Write		2.7	–	V_{CC}	
Input Low Voltage	All Inputs	V_{IL}	-1.0	–	0.8	Vdc

DC CHARACTERISTICS (V_{DD} = 12 V ±5%, V_{CC} = 5.0 V ±10%, V_{BB} = -5.0 V ±10%)

Characteristic	Symbol	Min	Typ	Max	Unit
Input Current, Any Input (V_{in} = 0 to V_{CC})	I_{in}	–	–	10	μA
Output High Voltage (I_O = -3.0 mA)	V_{OH}	2.4	–	–	Vdc
Output Low Voltage (I_O = 2.0 mA)	V_{OL}	–	–	0.4	Vdc
Output Leakage Current (Output Disabled by $\overline{CS}$ Input)	I_{LO}	–	–	10	μA
Average Supply Current, Active Mode ($T_{cyc(W)}$ = min, T_A = 70°C)	I_{DDA}	–	–	50	mA
	I_{CCA}	–	–	100	μA
	I_{BBA}	–	–	100	μA
Supply Current, Standby Mode (T_A = 70°C)	I_{DDS}	–	–	2.0	mA
	I_{CCS}	–	–	10	μA
	I_{BBS}	–	–	100	μA

PACKAGE DIMENSIONS

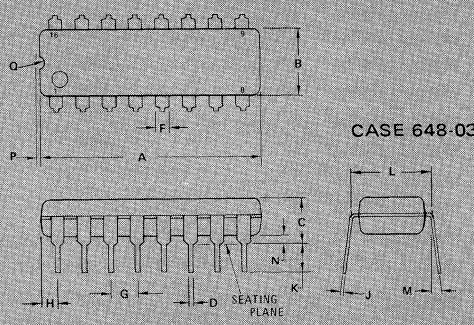
CASE 690-07



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	18.80	19.23	0.740	0.757
C	2.67	3.94	0.105	0.155
D	0.41	0.51	0.016	0.020
F	1.14	1.40	0.045	0.055
G	2.54 BSC		0.100 BSC	
H	0.51	0.71	0.020	0.028
J	0.20	0.31	0.008	0.012
K	3.56	4.83	0.140	0.190
L	7.62 BSC		0.300 BSC	
M	–	10°	–	10°
N	0.64	1.14	0.025	0.045

NOTE
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.

CASE 648-03



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	20.70	21.34	0.815	0.840
B	6.10	6.60	0.240	0.260
C	4.06	4.57	0.160	0.180
D	0.38	0.51	0.015	0.020
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.32	1.83	0.052	0.072
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.37	7.87	0.290	0.310
M	–	10°	–	10°
N	0.51	1.02	0.020	0.040
P	0.13	0.38	0.005	0.015
Q	0.51	0.76	0.020	0.030

NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL

EFFECTIVE CAPACITANCE (Full operating voltage and temperature range, periodically sampled rather than 100% tested.)

Characteristic		Symbol	Max	Unit
Input Capacitance	A_n	$C_{in(EFF)}$	10	pF
	$\overline{RAS}$, $\overline{CAS}$, D_{in}, $\overline{Write}$, $\overline{CS}$		7.0	
Output Capacitance		$C_{out(EFF)}$	8.0	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS
(Read, Write, and Read-Modify-Write Cycles)

RECOMMENDED AC OPERATING CONDITIONS (V_{DD} = 12 V ±5%, V_{CC} = 5.0 V ±10%, V_{BB} = -5.0 V ±10%, T_A = 0 to 70°C)

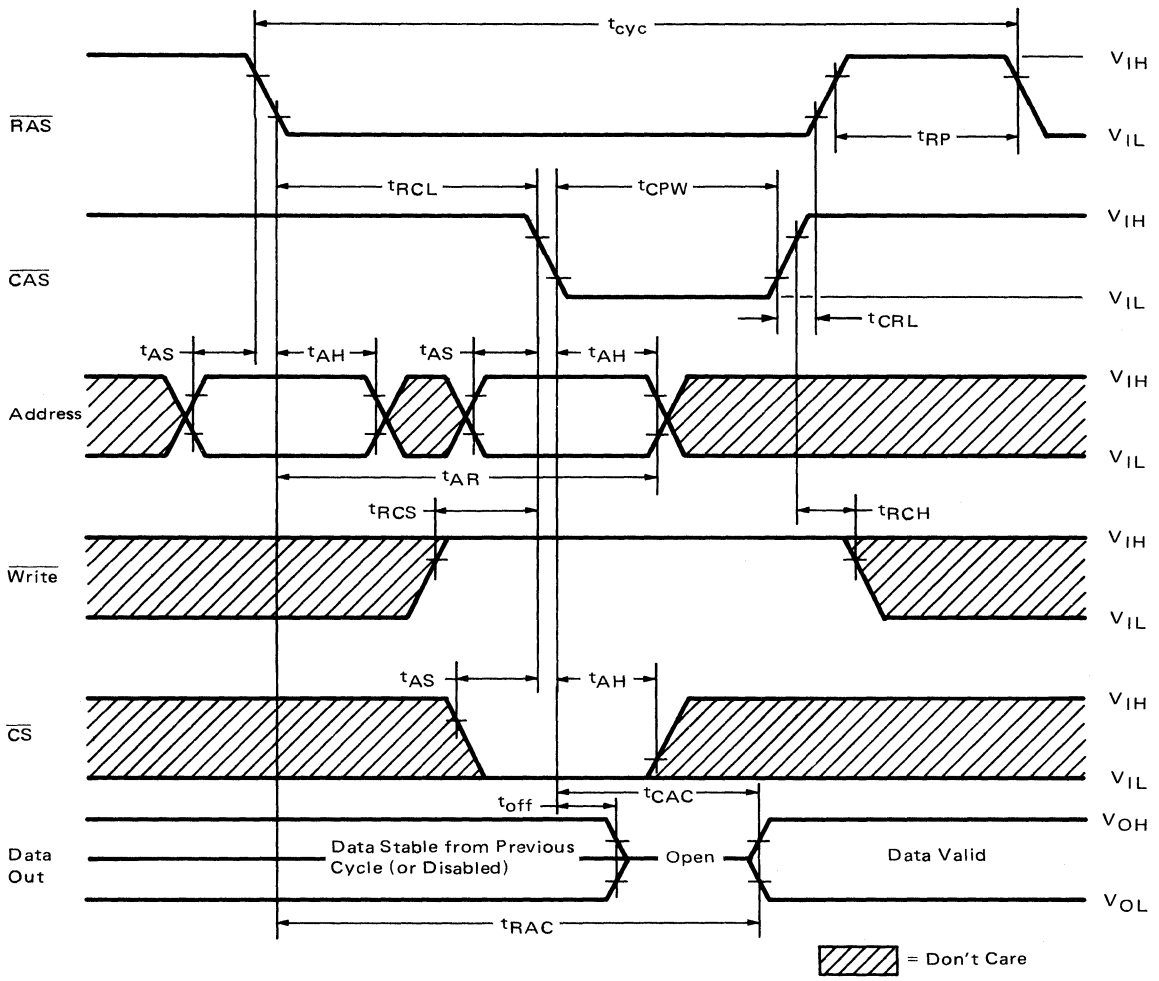
Parameter	Symbol	MCM6604L,P		MCM6604L2,P2		MCM6604L4,P4		Unit
		Min	Max	Min	Max	Min	Max	
Random Read or Write Cycle Time	t_{cyc}	500	–	375	–	425	–	ns
Read-Modify-Write Cycle Time	$t_{cyc(RMW)}$	700	–	540	–	620	–	ns
Row Address Strobe Precharge Time	t_{RP}	150	–	125	–	125	–	ns
Row to Column Strobe Lead Time (Note 1)	t_{RCL}	110	150	70	110	90	130	ns
Column Address Strobe Pulse Width	t_{CPW}	200	–	140	–	170	–	ns
Address Setup Time	t_{AS}	0	–	0	–	0	–	ns
Address Hold Time	t_{AH}	100	–	60	–	80	–	ns
$\overline{RAS}$ Address Release Time	t_{AR}	250	–	170	–	210	–	ns
Read Command Setup Time	t_{RCS}	0	–	0	–	0	–	ns
Read Command Hold Time	t_{RCH}	100	–	0	–	80	–	ns
Read Command Pulse Width	t_{RPW}	300	–	200	–	250	–	ns
Write Command Hold Time (Note 2)	t_{WCH}	150	–	110	–	130	–	ns
Write Command Pulse Width	t_{WP}	200	–	140	–	170	–	ns
Column to Row Strobe Lead Time	t_{CRL}	-50	+50	-40	+40	-45	+45	ns
Write Command to Column Strobe Lead Time	t_{CWL}	200	–	140	–	170	–	ns
Data In Setup Time	t_{DS}	0	–	0	–	0	–	ns
Data In Hold Time	t_{DH}	150	–	110	–	130	–	ns
Refresh Period	t_{REF}	–	2.0	–	2.0	–	2.0	ms
Modify Time	t_{MOD}	0	10	0	10	0	10	μs

1. If t_{RCL} is greater than the maximum recommended value shown in this table, t_{cyc} and t_{RAC} will increase by the amount that t_{RCL} exceeds the value shown.
2. The Write Command Hold Time is important only when normal random write cycles are being performed. During a read-write or a read-modify-write cycle, the limiting parameter is the Write Command Pulse Width.

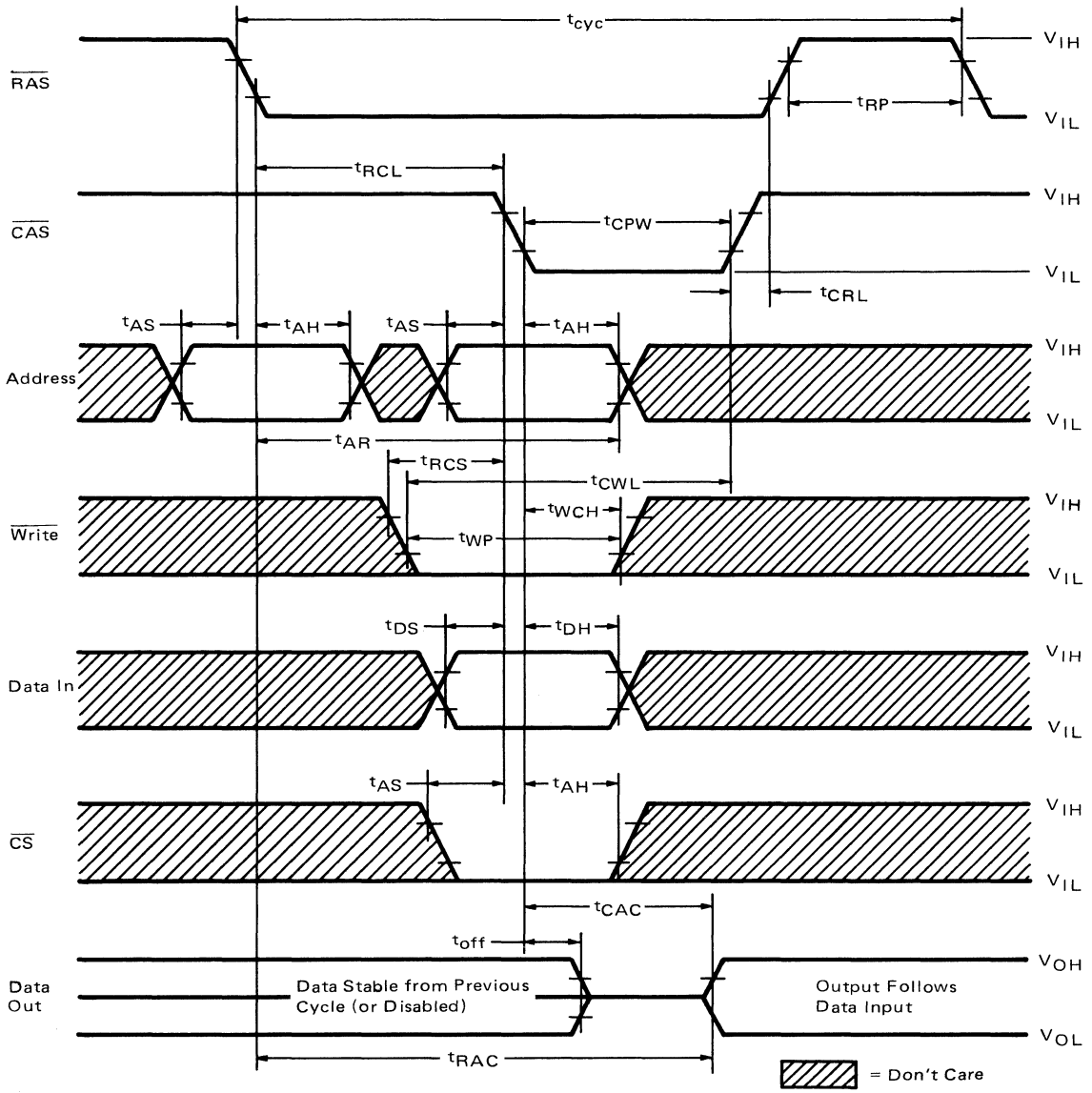
AC CHARACTERISTICS ($t_r = t_f$ = 20 ns, Load = 1 MC74H00 Series TTL Gate, $C_{L(EFF)}$ = 50 pF)

Characteristic	Symbol	MCM6604L,P	MCM6604L2,P2	MCM6604L4,P4	Unit
		Max	Max	Max	
Access Time from Row Address Strobe ($t_{RCL} \leq$ 150 ns for MCM6604L,P) ($t_{RCL} \leq$ 110 ns for MCM6604L2,P2) ($t_{RCL} \leq$ 130 ns for MCM6604L4,P4)	t_{RAC}	350	250	300	ns
Access Time from Column Address Strobe	t_{CAC}	200	150	175	ns
Output Buffer Turn-Off Delay	t_{off}	100	65	85	ns

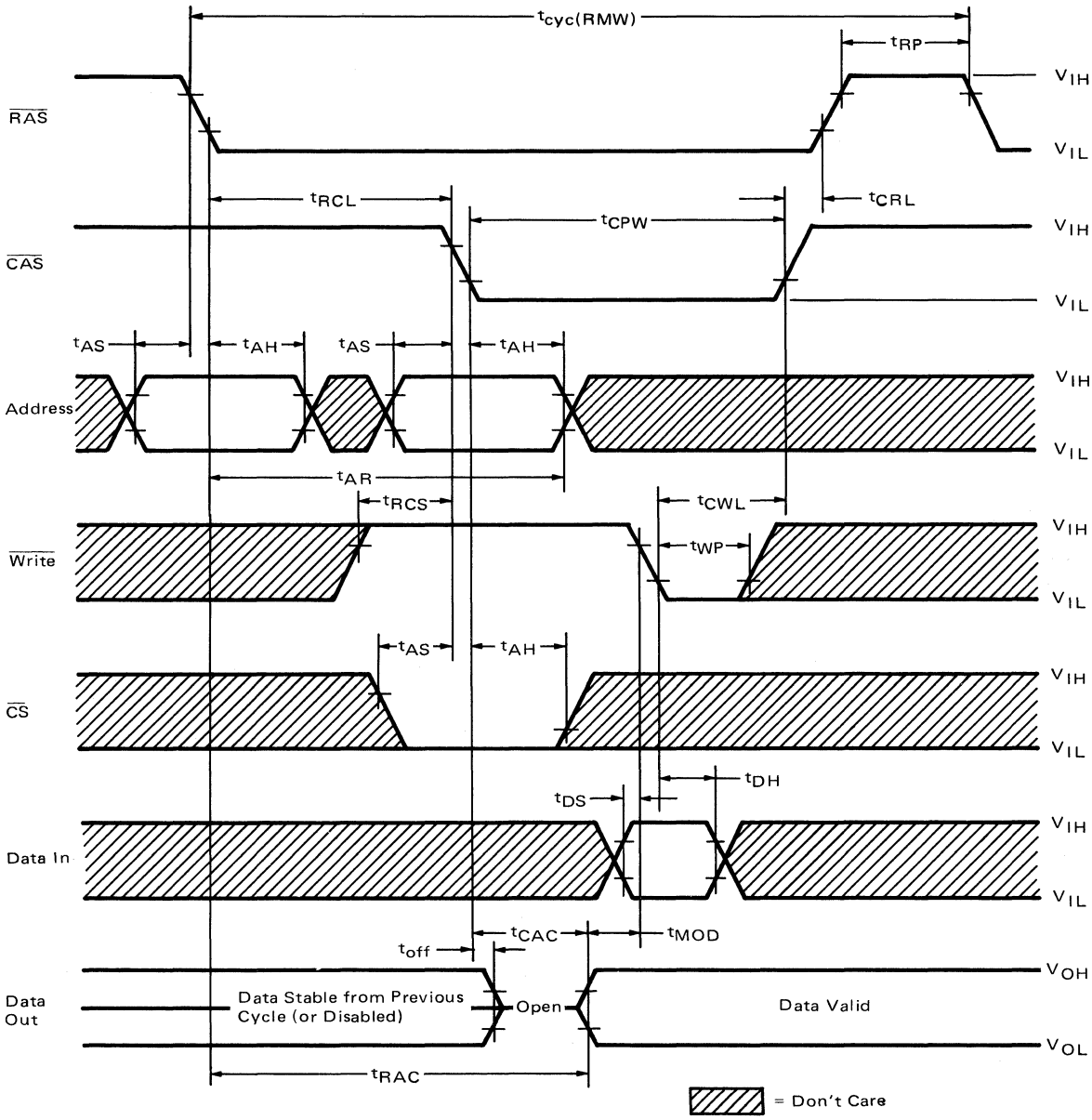
READ CYCLE TIMING



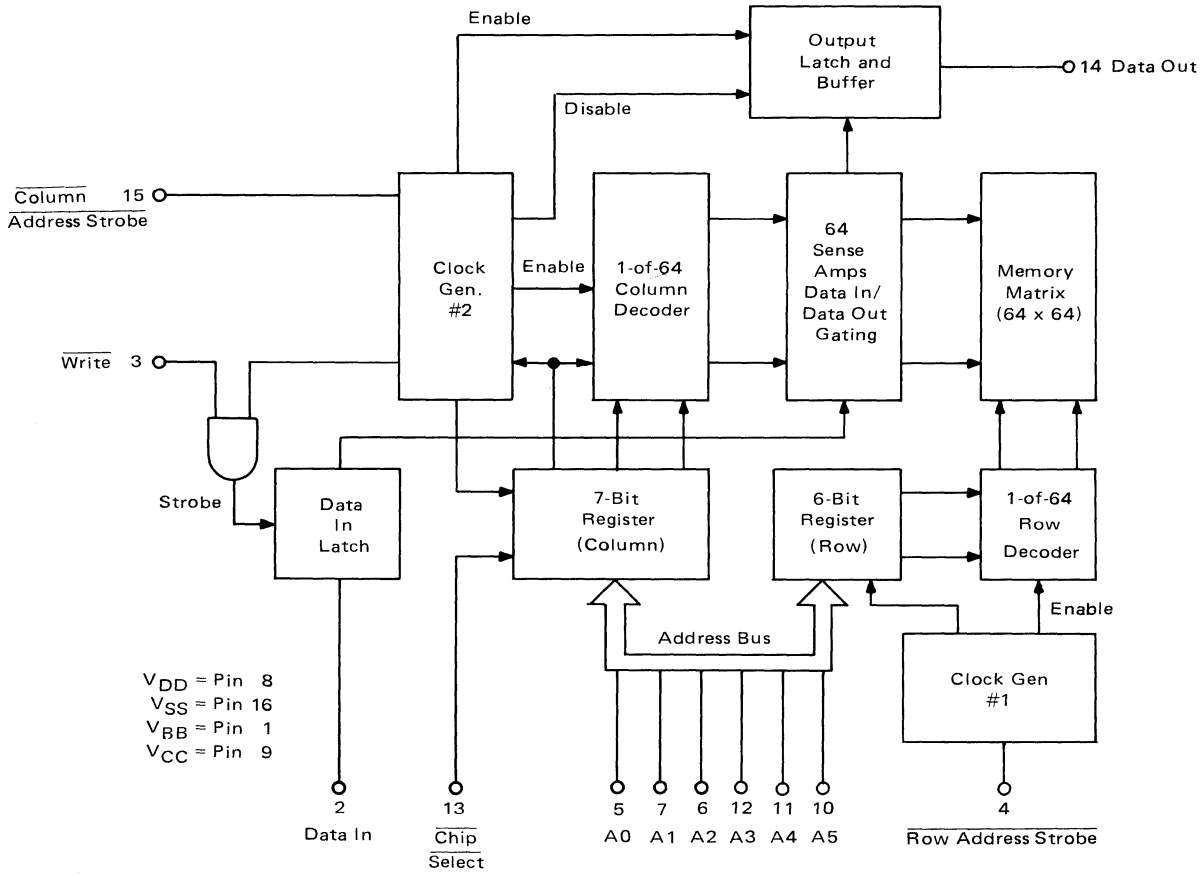
WRITE CYCLE TIMING



READ – MODIFY – WRITE TIMING



BLOCK DIAGRAM



ADDRESSING

The MCM6604 has six address inputs (A0 through A5) that are common to two address registers, one register for the row address and another for the column address. The column register has an additional latch that accommodates the Chip Select ($\overline{CS}$) signal. At the start of a memory cycle, the row address is latched into the address register with the Row Address Strobe ($\overline{RAS}$) signal. Next, the 6-bit column address is placed on the address bus along with the Chip Select signal, and they are latched into the column register with the Column Address Strobe ($\overline{CAS}$). Since the Chip Select signal is latched well into the memory cycle, its decoding time will not increase the memory system access or cycle time.

DATA OUTPUT

In order to simplify the memory system design and reduce the total package count, the MCM6604 contains an input data latch and a buffered output data latch. The state of the output latch and buffer at the end of a memory cycle will depend on the type of memory cycle performed and whether the chip is selected or unselected for that memory cycle.

A chip will be unselected during a memory cycle if:

(1) The chip receives both $\overline{RAS}$ and $\overline{CAS}$ signals, but no Chip Select signal.

(2) The chip receives a $\overline{CAS}$ signal but no $\overline{RAS}$ signal. With this condition, the chip will be unselected regardless of the state of Chip Select input.

If, during a read, write, or read-modify-write cycle, the chip is unselected, the output buffer will be in the high impedance state at the end of the memory cycle. The output buffer will remain in the high impedance state until the chip is selected for a memory cycle.

For a chip to be selected during a memory cycle, it must receive the following signals: $\overline{RAS}$, $\overline{CAS}$, and Chip Select. The state of the output latch and buffer of a selected chip during the following type of memory cycles would be:

(1) Read Cycle — On the negative edge of $\overline{CAS}$, the output buffer will unconditionally go to a high impedance state. It will remain in this state until access time. At this time, the output latch and buffer will assume the logic state of the data read from the selected cell. This output state will be maintained until the chip receives the next $\overline{CAS}$ signal.

(2) Write Cycle — If the Write input is switched to a logic 0 before the $\overline{CAS}$ transition, the output latch and buffer will be switched to

the state of the data input at the end of the access time. This logic state will be maintained until the chip receives the next $\overline{CAS}$ signal.

(3) Read-Modify-Write — Same as a read cycle.

DATA INPUT

Data to be written into a selected storage cell of the memory chip is first stored in the on-chip data latch. The gating of this latch is performed with a combination of the $\overline{Write}$ and $\overline{CAS}$ signals. The last of these signals to make a negative transition will strobe the data into the latch. If the $\overline{Write}$ input is switched to a logic 0 at the beginning of a write cycle, the falling edge of $\overline{CAS}$ strobes the data into the latch. The data setup and hold times are then referenced to the negative edge of $\overline{CAS}$.

If a read-modify-write cycle is being performed, the $\overline{Write}$ input would not make its negative transition until after the $\overline{CAS}$ signal was enabled. Thus, the data would not be strobed into the latch until the negative transition of $\overline{Write}$. The data setup and hold times would now be referenced to the negative edge of the $\overline{Write}$ signal. The only other timing constraints for a write-type cycle is that both the $\overline{CAS}$ and $\overline{Write}$ signals remain in the logic 0 state for a sufficient time to accomplish the permanent storage of the data into the selected cell.

INPUT/OUTPUT LEVELS

All of the inputs to the MCM6604 are TTL compatible. The inputs feature high impedance and low capacitance (<10 pF) characteristics which will minimize the driver requirements in a memory system. The three-state data output buffer is TTL compatible and has sufficient current sink capability (2 mA) to drive one high speed TTL load. The output buffer also has a separate V_{CC} pin so that it can be powered from the same supply as the logic being employed.

POWER DISSIPATION

Since the MCM6604 is a dynamic RAM, its power drain will be extremely small during the time the chip is unselected.

The power of the MCM6604 increases when selected and most of this increase is encountered on the address strobe edge. Hence, the power will be a function of the duty cycle.

In a memory system, the $\overline{CAS}$ signal must be supplied to all the memory chips to insure that the outputs of the unselected chips are switched to the high impedance state. Those chips that do not receive an $\overline{RAS}$ signal will not dissipate any power on the $\overline{CAS}$ edge except for that required to turn off the chip outputs. Thus, in order to insure minimum system power, the $\overline{RAS}$ signal should be decoded so that only the chips to be selected receive an $\overline{RAS}$ signal. If the $\overline{RAS}$ signal is decoded, then the chip select input of all the chips can be set to a logic 0 state.

REFRESH

The MCM6604 is refreshed by sequentially cycling through the 64 row addresses every 2 milliseconds or less. It is not necessary to supply the $\overline{CAS}$ to the chip while it is being refreshed. Any read, write, or read-modify-write cycle will refresh a selected row. However, if a write cycle is used to perform a refresh cycle the chip must be unselected.

MOTOROLA
Semiconductors
BOX 20912 • PHOENIX, ARIZONA 85036

MCM6605A L/L1/L2
MCM6605A P/P1/P2

MOS
(N-CHANNEL, SILICON-GATE)

4096-BIT DYNAMIC RANDOM ACCESS MEMORY

4096-BIT DYNAMIC RANDOM ACCESS MEMORY

The MCM6605A is a 4096-bit high-speed dynamic Random Access Memory designed for high-performance, low-cost applications in mainframe and buffer memories and peripheral storage. Organized as 4096 one-bit words, these memories are fabricated using selective oxidation N-channel silicon gate technology to optimize device speed, power and density tradeoffs.

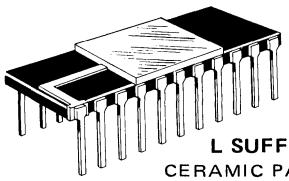
All address and control inputs are TTL compatible except for a single high-level clock (Chip Enable). Complete address decoding is done on chip and address latches are incorporated for ease of use. Refresh of the entire memory can be accomplished by sequentially cycling through addresses A0-A4 (32 cycles) a maximum of every 2.0 milliseconds.

The MCM6605A uses a three-transistor memory cell to simplify internal sense amplifier requirements. Output data is inverted with respect to input data. The outputs are 3-state TTL configuration and require no external sense amplifier. Outputs are in the high impedance (floating) state when either the Chip Enable is in the low state or the $\overline{\text{Chip Select}}$ is in the high state.

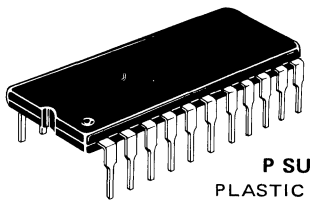
- Organized as 4096 Words of 1 Bit

	L1, P1	L2,P2	L, P
• Maximum Access Time =	150 ns	200 ns	300 ns
• Minimum Read Cycle Time =	290 ns	360 ns	470 ns
• Minimum Write Cycle Time =	390 ns	490 ns	590 ns
• Minimum Read Modify Write Cycle Time =	390 ns	490 ns	590 ns

- Low Power Dissipation
  335 mW Typical (Active)
  2.6 mW Typical (Standby with Refresh)
- Easy Refresh — Only 32 Cycles Every 2.0 ms
- TTL Compatible
- 3-State Output
- Address Latches On Chip
- Power Supply Pins on Package Corners for Layout Simplification
- Typical Applications:
  Main Memory
  Buffer Memory
  Peripheral Storage

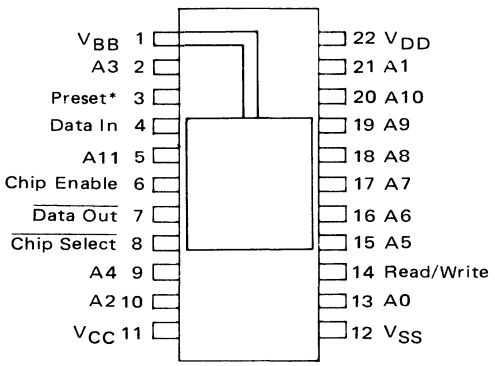


L SUFFIX
CERAMIC PACKAGE
CASE 677



P SUFFIX
PLASTIC PACKAGE
CASE 708

PIN ASSIGNMENT



*See Applications Information

ABSOLUTE MAXIMUM RATINGS (See Note 1)

Rating	Symbol	Value	Unit
Voltage on Any Pin Relative to V_{BB}	V_{in}, V_{out}	-0.3 to +20	Vdc
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

NOTE 1: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted.)

RECOMMENDED DC OPERATING CONDITIONS (Referenced to V_{SS}).

Parameter	Symbol	Min	Nom	Max	Unit
Supply Voltage	V_{DD}	11.4	12	12.6	Vdc
	V_{CC}	4.5	5.0	5.5	Vdc
	V_{SS}	0	0	0	Vdc
	V_{BB}	-5.25	-5.0	-4.75	Vdc
Logic Levels Input High Voltage (A_n, D_{in}, R/W, $\overline{CS}$)	V_{IH}	3.0	–	V_{DD} + 0.6	Vdc
Input Low Voltage (A_n, D_{in}, R/W, $\overline{CS}$)	V_{IL}	-1.0	–	0.8	Vdc
Chip Enable High Voltage	V_{CEH}	V_{DD} - 0.6	–	V_{DD} + 0.6	Vdc
Chip Enable Low Voltage	V_{CEL}	-1.0	–	0.8	Vdc

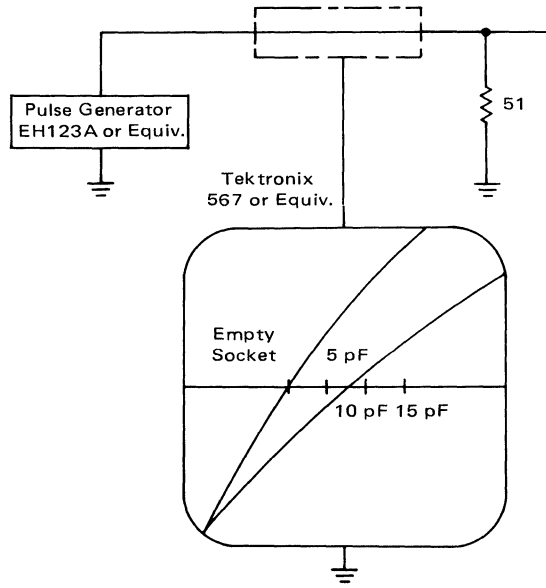
DC CHARACTERISTICS

Characteristic	Symbol	Min	Typ	Max	Unit
Input Current (A_n, D_{in}, R/W, $\overline{CS}$, Preset) (V_{in} = 0 to V_{DD} + 1.0 V)	I_{in}	–	–	10	μA
Input Chip Enable Current (V_{in} = 0 to V_{DD} + 1.0 V)	I_{ICE}	–	–	10	μA
Output High Voltage (I_O = -100 μA)	V_{OH}	2.4	–	V_{CC}	Vdc
Output Low Voltage (I_O = 2.0 mA)	V_{OL}	V_{SS}	–	0.45	Vdc
Output Leakage Current (V_O = 0.45 V to V_{CC}, CE = V_{CEL}, or $\overline{CS}$ = V_{IH})	I_{LO}	–	–	10	μA
Average Supply Current, Active Mode ($T_{cyc(W)}$ = min)	I_{DDA}	–	28	36	mA
	I_{CCA}	–	0.05	1.0	mA
	I_{BBA}	–	–	100	μA
Supply Current, Standby Mode (CE = 0.45 V)	I_{DDS}	–	1.0	20	μA
	I_{CCS}	–	–	10	μA
	I_{BBS}	–	1.0	20	μA

EFFECTIVE CAPACITANCE (Test Circuit of Figure 1, full operating voltage and temperature range, periodically sampled rather than 100% tested.)

Characteristic	Symbol	Min	Typ	Max	Unit
Input Capacitance (A_n, D_{in}, R/W, $\overline{CS}$, Preset)	$C_{in(EFF)}$	–	4.0	5.0	pF
Chip Enable Capacitance	$C_{CE(EFF)}$	–	25	30	pF
Output Capacitance	$C_{out(EFF)}$	–	4.0	5.0	pF

FIGURE 1 – MEASUREMENT OF EFFECTIVE CAPACITANCE



Effective capacitance is determined by comparing the rise time of the voltage waveform at a particular pin to that measured with known values of capacitance. Scope calibration points are determined by using the rise times obtained with the empty socket and standard capacitor values as references.

The device under test (DUT) is inserted into the test socket and normal operating power supplies applied. All input pins, except that being measured, are grounded. The effective capacitance of the desired pin can then be read directly from the scope.

Pin	R	Input Pulse	Measurement Level
CE	67 Ω	16 V	12 V
Input/Output	100 Ω	6.0 V	4.0 V

AC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature unless otherwise noted.)

OPERATING MODES

Mode	Control States		Output
	R/W	$\overline{CS}$	
Active (CE = High)			
Read Only	H	L	Valid
Read/Write	H → L	L	Valid
Write Only	L	L	Valid
Read Refresh	H → L	L → H	Valid → Floating
Refresh Only	L	H	Floating
Chip Disable (Unselected)	H	H	Floating
Standby (CE = Low)	X	X	Floating

X = Don't Care

RECOMMENDED AC OPERATING CONDITIONS (Read, Write, and Read Modify Write Cycles)

Parameter		Symbol	Min	Max	Unit
Address Setup Time		t_{AS}	0	–	ns
Address Hold Time		t_{AH}	60	–	ns
CE Pulse Transition Time		t_T	10	100	ns
CE Off Time	MCM6605AL,P/L2,P2	t_{SB}	120	–	ns
	MCM6605AL1,P1		90	–	
Chip Select Delay Time		t_{CSD}	–	70	ns
Chip Select Hold Time		t_{CSH}	0	–	ns
Read Write Delay Time		t_{RWD}	–	70	ns
Read Write Hold Time		t_{RWH}	0	–	ns
Time Between Refresh		t_{REF}	–	2.0	ms

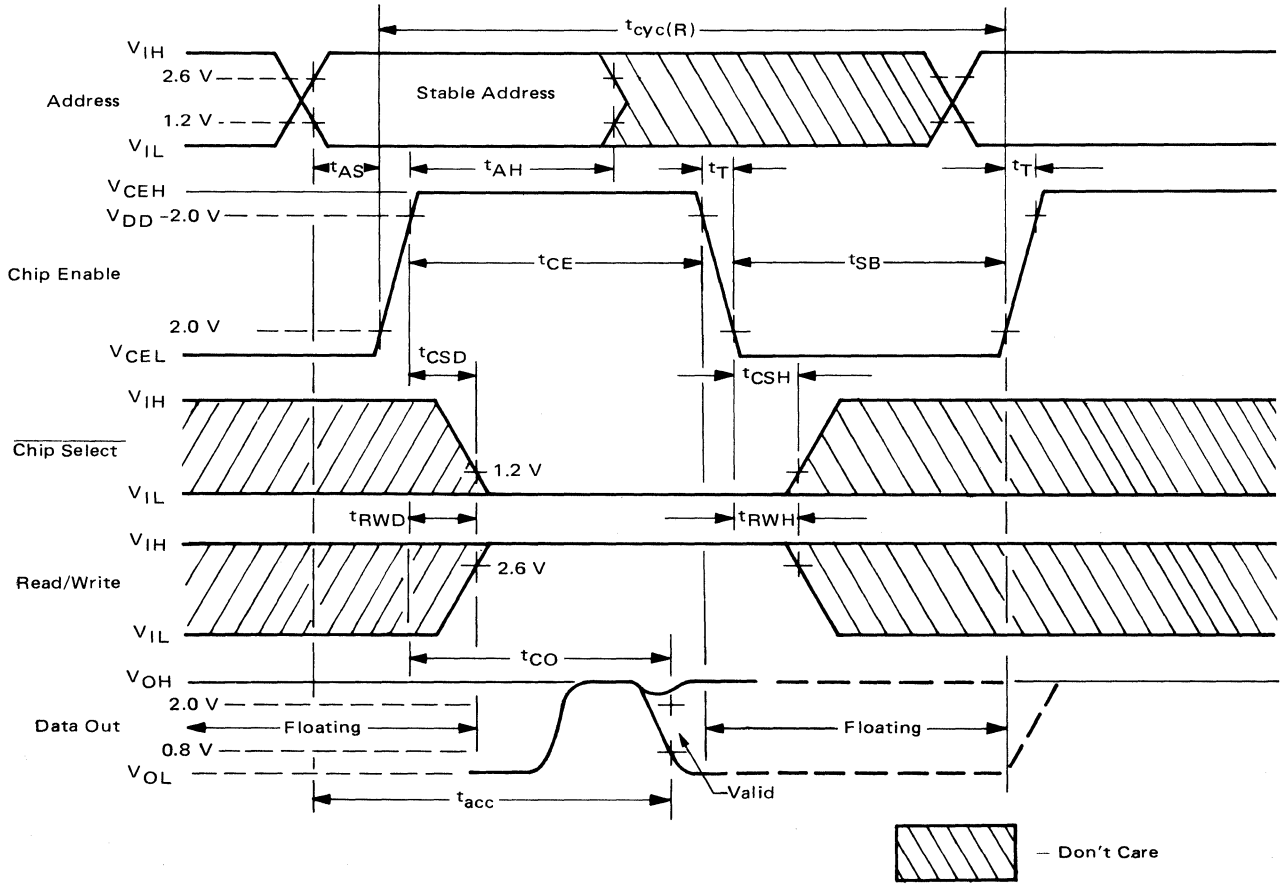
AC CHARACTERISTICS

[All timing with t_T = 20 ns; Load = 1 TTL Gate (MC74H00 Series), C_L = 50 pF (effective)]

READ CYCLE (R/W = V_{IH}, $\overline{CS}$ = V_{IL})

Characteristic	Symbol	MCM6605AL,P		MCM6605AL1,P1		MCM6605AL2,P2		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	$t_{cyc(R)}$	470	–	290	–	360	–	ns
Chip Enable On Time	t_{CE}	310	2000	160	2000	200	2000	ns
Chip Enable to Output Delay	t_{CO}	–	280	–	130	–	180	ns
Read Access Time	t_{acc}	–	300	–	150	–	200	ns

READ CYCLE TIMING

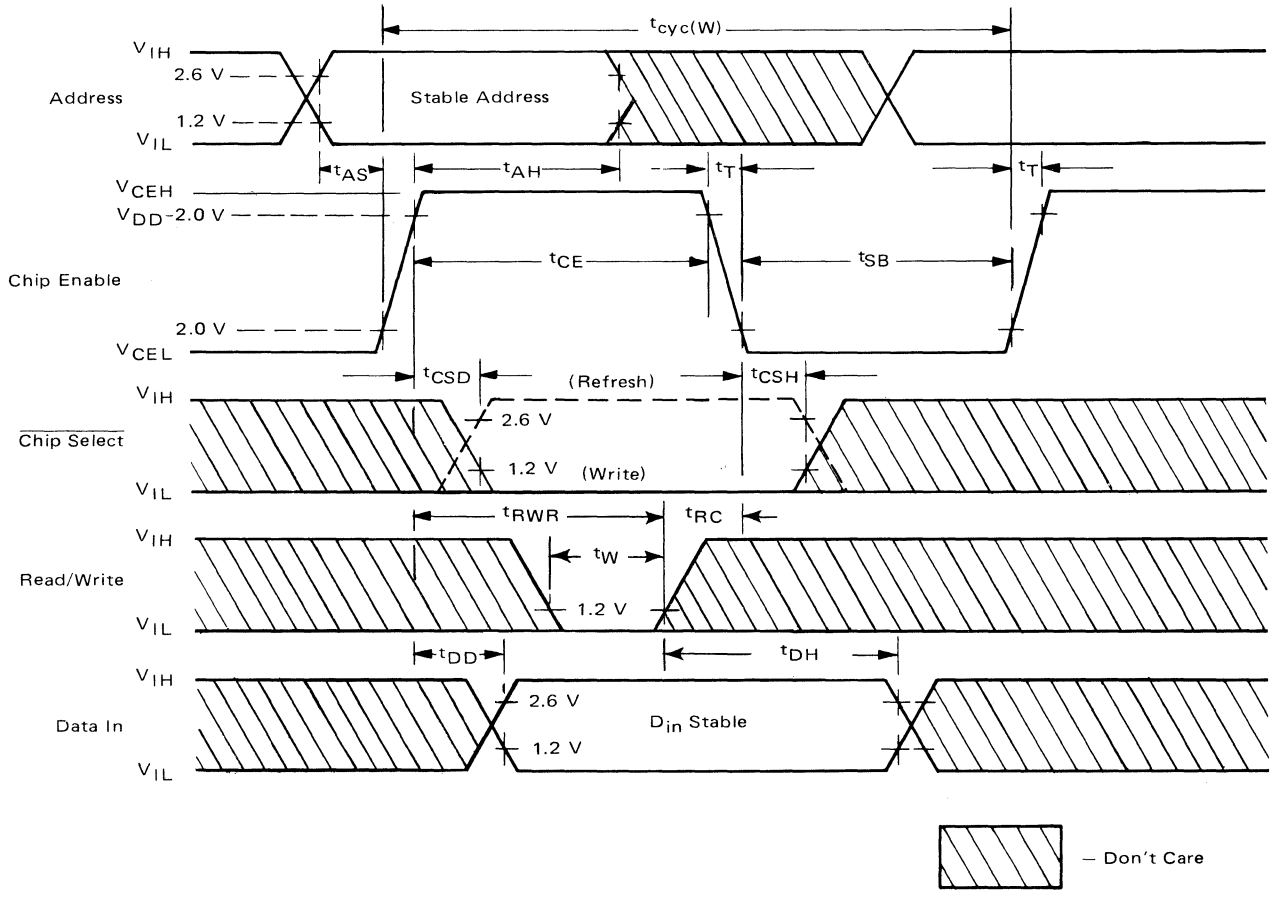


WRITE CYCLE (R/W = V_{IL}, $\overline{CS}$ = V_{IL})
REFRESH CYCLE (R/W = V_{IL}, $\overline{CS}$ = V_{IH})

Characteristic	Symbol	MCM6605AL,P		MCM6605AL1,P1		MCM6605AL2,P2		Unit
		Min	Max	Min	Max	Min	Max	
Write Cycle Time	$t_{cyc(W)}$	590	–	390	–	490	–	ns
Chip Enable On Time	t_{CE}	430	2000	260	2000	330	2000	ns
Read-Write Release Time	t_{RWR}	410	2000	240	2000	310	2000	ns
Write Pulse Width	t_W	210	–	160	–	160	–	ns
Read-Write to Chip Enable Separation Time	t_{RC}	0	–	0	–	0	–	ns
Data Delay Time*	t_{DD}	–	70	–	70	–	70	ns
Data Hold Time	t_{DH}	50	–	20	–	50	–	ns

*If a write pulse (t_W) is employed on the R/W line during a write cycle, then the input data setup time is measured from the leading edge of the write pulse. The t_{DS} time is the same as that of the read-modify-write cycle.

WRITE AND REFRESH CYCLE TIMING

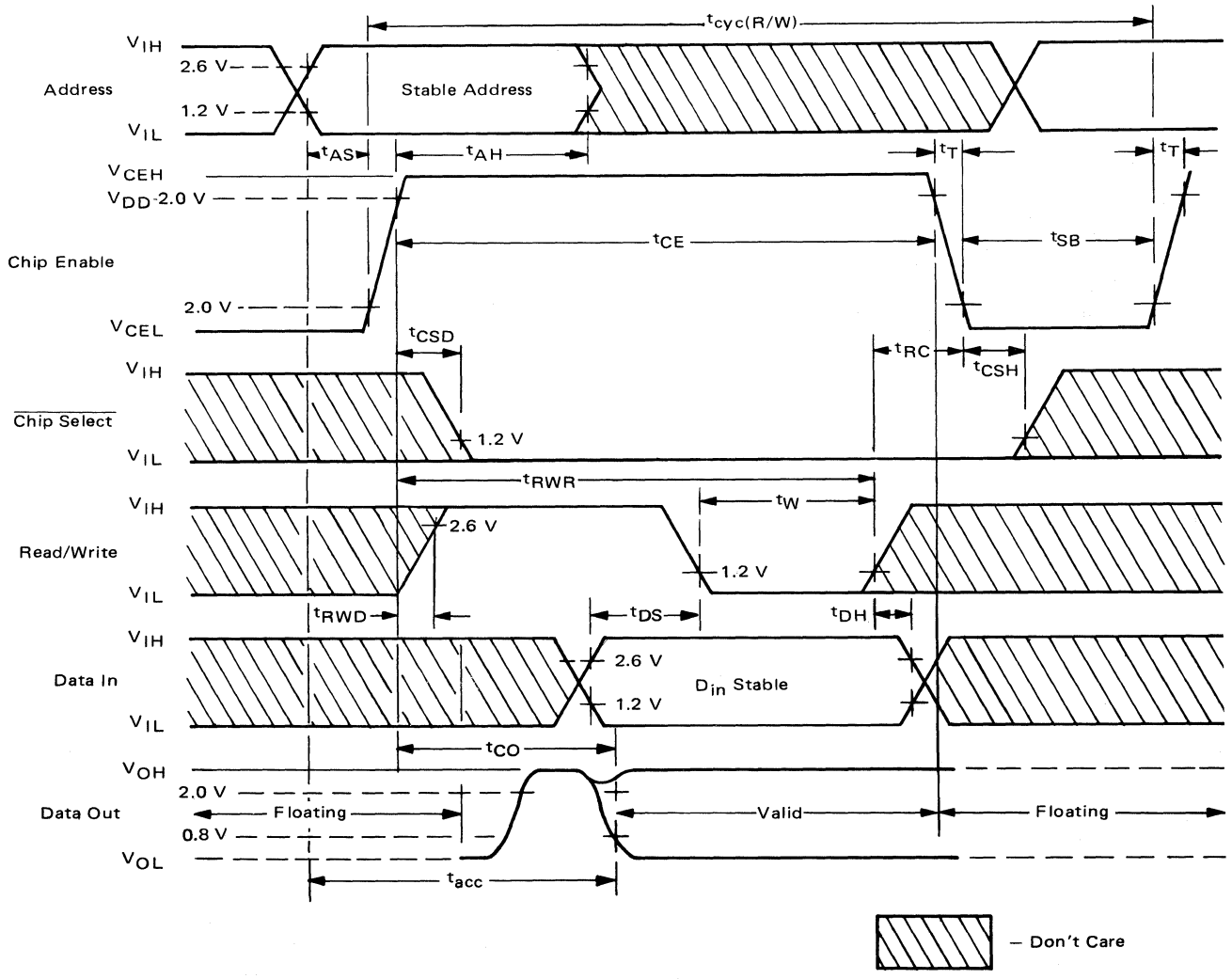


READ-MODIFY-WRITE ($R/\overline{W}$ = $V_{IH} \rightarrow V_{IL}$, $\overline{CS}$ = V_{IL})
READ REFRESH (See Note 1)

Characteristic	Symbol	MCM6605AL,P		MCM6605AL1,P1		MCM6605AL2,P2		Unit
		Min	Max	Min	Max	Min	Max	
Read-Modify-Write Cycle Time	$t_{cyc(R/W)}$	590	–	390	–	490	–	ns
Chip Enable On Time	t_{CE}	430	2000	260	2000	330	2000	ns
Read-Write Release Time	t_{RWR}	410	2000	240	2000	310	2000	ns
Write Pulse Width	t_W	210	–	160	–	160	–	ns
Data Setup Time	t_{DS}	0	–	0	–	0	–	ns
Data Hold Time	t_{DH}	50	–	20	–	50	–	ns
Read-Write to Chip Enable Separation Time	t_{RC}	0	–	0	–	0	–	ns
Chip Enable to Output Delay	t_{CO}	–	280	–	130	–	180	ns
Read Access Time	t_{acc}	–	300	–	150	–	200	ns

Note 1: A read refresh cycle is possible by bringing $\overline{CS}$ high after output data is valid and then bringing R/W low to the write position.

READ MODIFY WRITE TIMING



TYPICAL CHARACTERISTICS CURVES

FIGURE 2 – ACCESS TIME versus V_{DD}

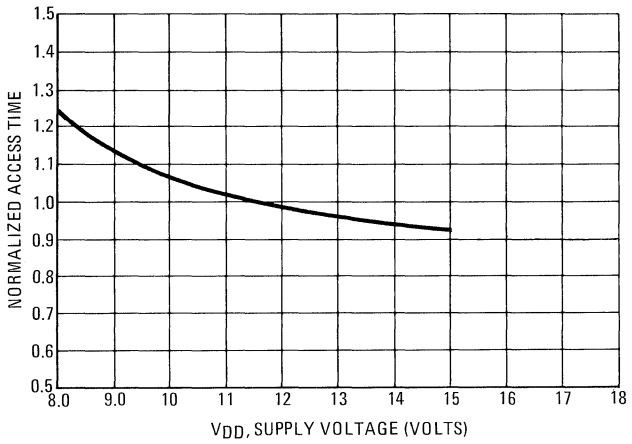


FIGURE 3 – ACCESS TIME versus AMBIENT TEMPERATURE

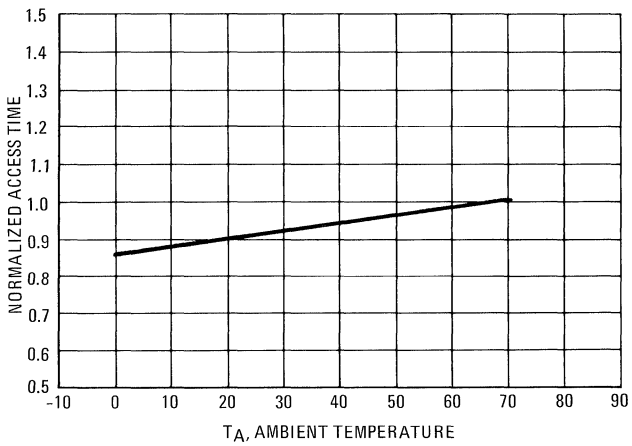


FIGURE 4 – I_{DD} SUPPLY CURRENT versus V_{DD}

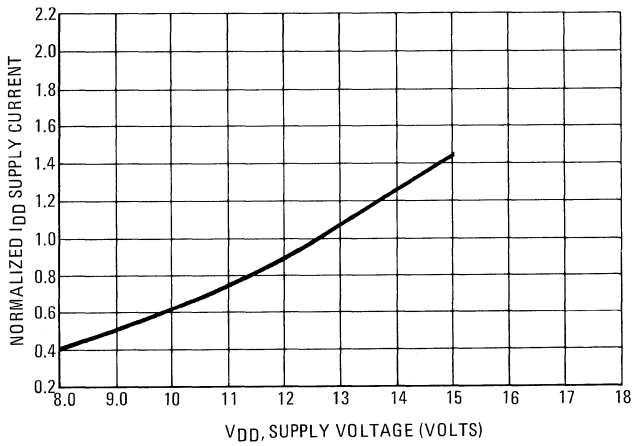


FIGURE 5 – I_{DD} SUPPLY CURRENT versus CYCLE TIME

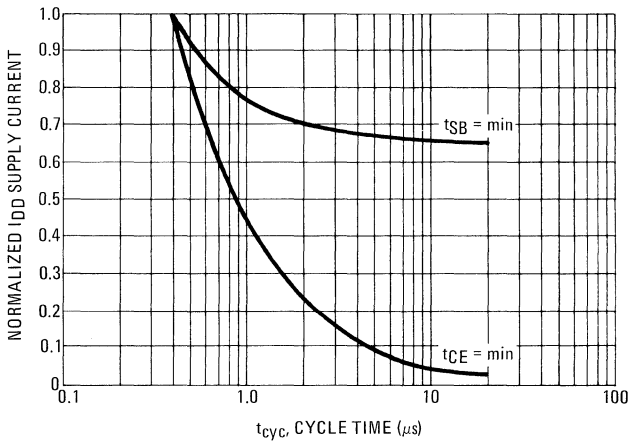


FIGURE 6 – I_{DD} SUPPLY CURRENT versus AMBIENT TEMPERATURE

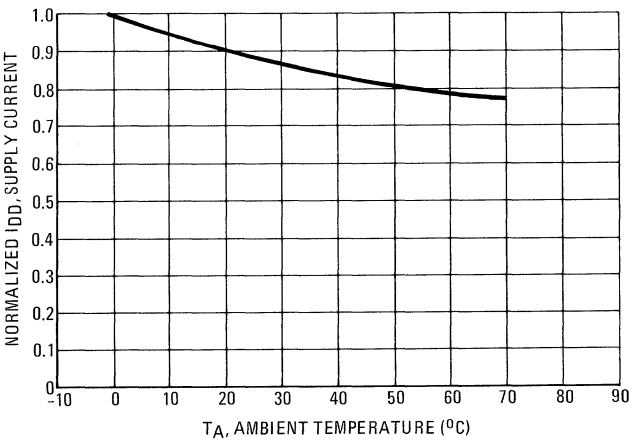
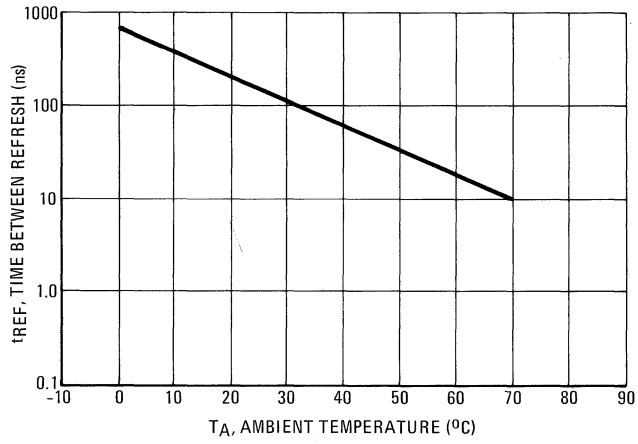


FIGURE 7 – REFRESH TIME versus AMBIENT TEMPERATURE



TYPICAL SUPPLY CURRENT TRANSIENT WAVEFORMS

FIGURE 8 – CHIP ENABLE VOLTAGE

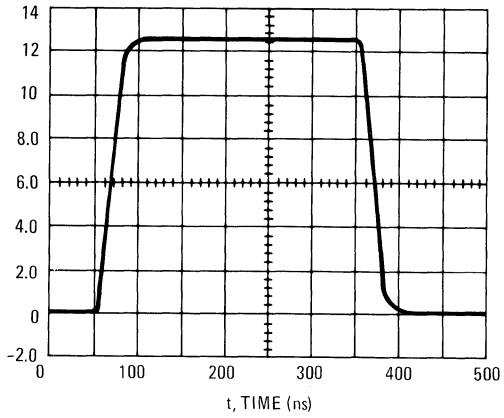


FIGURE 9 – i_{DD} SUPPLY CURRENT

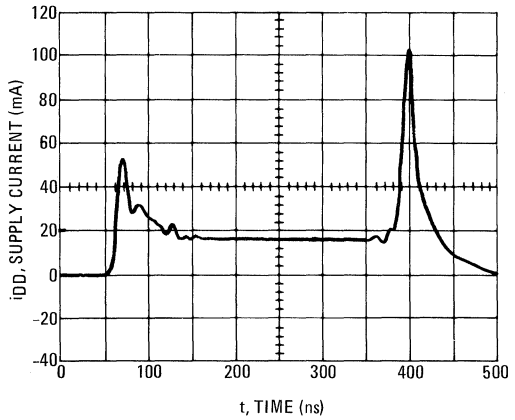


FIGURE 10 – i_{CC} SUPPLY CURRENT

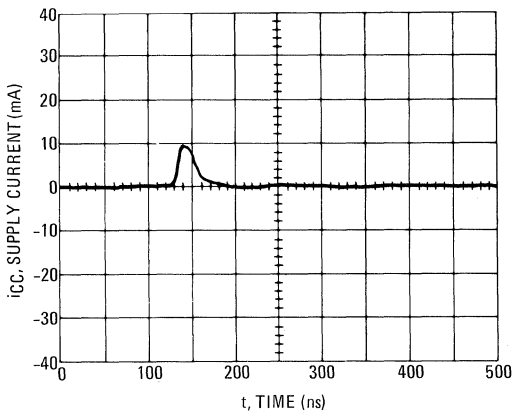


FIGURE 11 – i_{BB} SUPPLY CURRENT

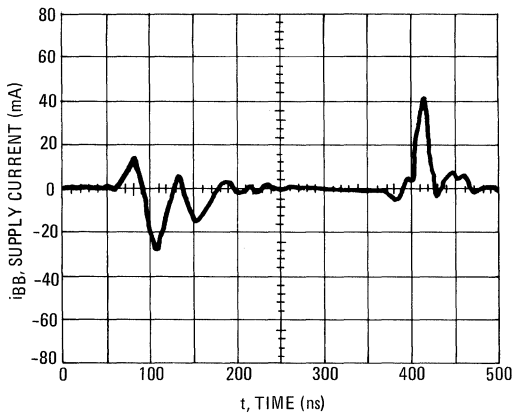
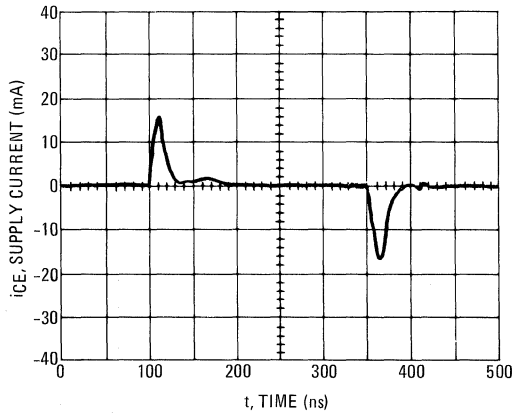
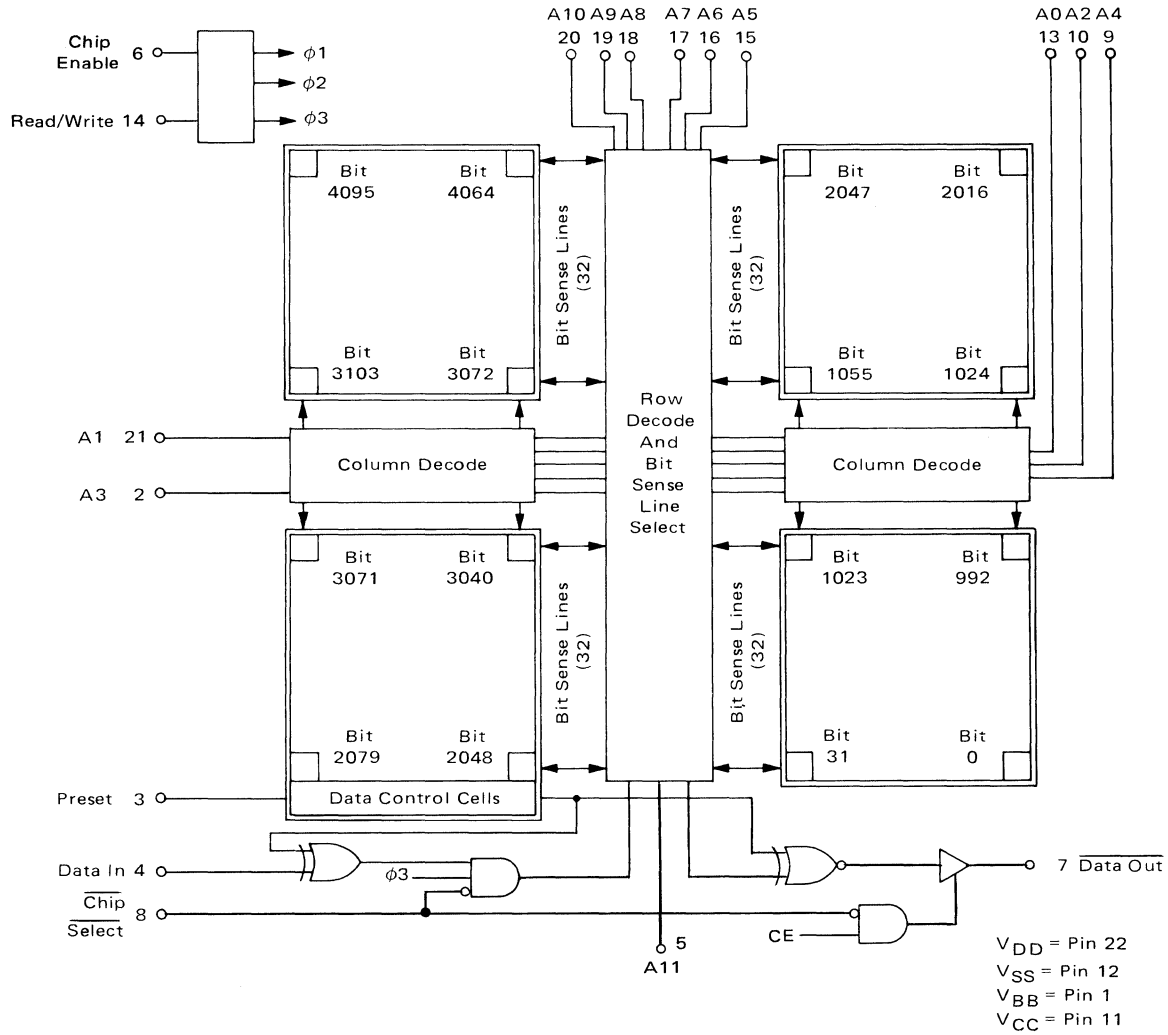


FIGURE 12 – i_{CE} SUPPLY CURRENT



BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

The MCM6605A 4096-bit dynamic RAM uses a three transistor storage cell in an inverting cell configuration. The single high-level clock (Chip Enable) starts an internal three-phase clock generator which controls the read and write functions of the device. The $\phi 1$ signal, which is high when CE is low (standby mode), preconditions the nodes in the dynamic RAM in preparation for a memory cycle. The $\phi 2$ signal, which comes on as CE goes high, is the read control and transfers data from storage onto bit sense lines. The $\phi 3$ signal, which comes after $\phi 2$ only during a write or refresh cycle, transfers data from the bit sense lines back into storage. The $\phi 3$ signal occurs only if the R/W input is low.

To perform a read cycle, CE is brought high to initiate a $\phi 2$ signal and latch the input addresses. The column decoders select one column in each of the four storage quadrants (see the block diagram) and transfers data from storage onto the 128 bit sense lines. The row decoder selects one of these 128 bit sense lines for read and write operations. During the $\phi 2$ signal, the data on this selected bit sense line is Exclusive ORed with the state of the appropriate data control cell to supply the correct output data. After this data is received by the external system, CE may be brought low to the standby position. This assumes that the R/W signal is held high to prevent an internal $\phi 3$ being generated.

To perform a write or refresh operation, CE is brought high and everything is identical to a read operation up until the 128 bit sense lines are charged with the selected columns of stored data. When R/W is brought low (if it is not already there), a $\phi 3$ signal is generated after $\phi 2$ is over. The $\phi 3$ signal takes the data from the 128 bit sense lines and returns it to the 128 storage locations it came from. Because of the design of the memory array, this $\phi 2$-$\phi 3$, read-write operation inverts the data. Therefore, one extra row of memory cells, called data control cells, is used to

keep track of the polarity of stored data in order to be able to correctly recover it. During the write operation, the input data is Exclusive ORed with these control cells before being stored in the array. A refresh cycle does not modify any of the bit sense lines, but simply returns the data (now inverted) into storage.

All timing signals for the MCM6605A are specified around these operations. The following is a brief description of the input pins and relevant timing requirements.

Chip Enable – CE is a single high level clock which initiates all memory cycles. CE can remain low as long as desired for specific applications as long as the 2.0 ms refresh requirements are met.

Chip Select – This signal controls only the I/O buffers. When $\overline{CS}$ is high, the input is disconnected and the output is in the 3-state high-impedance state. A refresh cycle is, therefore, a write cycle with $\overline{CS}$ high. $\overline{CS}$ has no critical timing with respect to any other signal except that there is a finite delay between activation and data out.

Read/Write – When high, R/W inhibits the internal $\phi 3$ signal, thereby keeping the memory from writing. When R/W is low, a $\phi 3$ will occur soon after $\phi 2$ is finished. For a read cycle, R/W should be high within t_{RWD} of CE to insure that a $\phi 3$ does not start. The only timing requirement on the R/W input for writing is a minimum write pulse defined as the overlap of $\overline{CS}$, CE, and R/W. Refresh cycles require that $\overline{CS}$ be high to inhibit the input buffer before a $\phi 3$ occurs. Thus $\overline{CS}$ should be high within t_{CSD} for a refresh cycle, or before R/W goes low for a read-refresh cycle.

Data In – The input data must be valid for a sufficient time to override the data stored on the selected bit sense line. It must remain valid for the "write pulse" defined under Read/Write. Signals on the D_{in} pin are ignored when either $\overline{CS}$ or R/W is high, or CE is low.

Data Out – Output data is inverted from input data and is valid t_{acc} after CE goes high. The data will remain valid as long as CE is high and $\overline{CS}$ remains low. With either CE low or $\overline{CS}$ high, the output is in a high-impedance state. The data output is initially precharged high when CE goes high and is then either discharged to ground or left high depending on the stored data. This precharging followed by valid data occurs regardless of the state of the R/W input, making the write cycle actually a read-write cycle. The output will also try to precharge during a refresh cycle but will be kept at high impedance by the $\overline{CS}$ being high. If $\overline{CS}$ is originally low and is then brought high (within the t_{CSD} specification) the output may start to precharge before being cut off and returned to high impedance.

Addresses – The addresses are latched when CE goes high, and may be removed after an appropriate hold time.

V_{SS} – Circuit ground.

V_{BB} – The reverse bias substrate supply. Forward biasing this supply with respect to V_{SS} will destroy the memory device.

V_{DD} – Positive supply voltage.

V_{CC} – Output buffer supply. This supply goes only to the data output buffer and draws current only when driving an output load high.

Preset – This pin should be tied to ground. During device testing Preset can be used to preset the data control cells to a logic zero. One 200 ns, 12 V pulse will set all 32 cells simultaneously. Preset has no system use; its only purpose is to ensure a good logic level in the control cells after first power up. In system use, this good logic level will come naturally after the first few refresh cycles.

APPLICATIONS INFORMATION

Power Supplies

The MCM6605A is a dynamic RAM which has essentially zero power drain when in the standby (CE low) mode. When operating, the V_{DD} supply may experience transients in the order of 100 mA for a short time (Figure 9). The V_{BB} supply, which has very low dc drain while operating, may see transients of about 40 mA during the edges of CE. Therefore, appropriate bypassing of both supplies is recommended. This bypassing has been simplified by the location of the power supply pins on the corners of the package.

The V_{CC} line supplies only the input leakage of a TTL load on Data Out and should never exceed about 100 μA, presenting little bypassing requirement.

Power dissipation for a system of N chips is much lower than N times the 335 mW typical dissipation for a full speed operating chip. This is because the unselected rows in a memory array card are operating in the standby mode of near zero dissipation. This zero standby power is actually unachievable because of the requirements for refresh. Therefore, power dissipation for an array of N X M chips operating at t_1 cycle time, t_{REF} refresh increment, and maximum CE down time between cycles is:

$$P_D \approx M\left(\frac{490\,ns}{t_1\,ns}\right)335\,mW + (N-1)\,(M)\left(\frac{15.7}{t_{REF}\,\mu s}\right)335\,mW$$

For a 550-ns-cycle-time, 64 k by 16 system (16 by 16 chip array) with refresh at 2.0 ms, the approximate power dissipation is:

$$P_D \approx 16\left(\frac{490}{550}\right)335 + (15)\,(16)\left(\frac{15.7}{2000}\right)335$$

$$\approx 4775\,mW + 630\,mW = 5.4\,W$$

A similar one megabyte system, eight bytes wide, would have a dissipation of only 24 W. If the low standby power capability were not used, over 600 W would be dissipated.

Refresh

The MCM6605A is refreshed by performing a refresh (or write) cycle on each of the 32 combinations of the least significant address bits (A0-A4) within a 2.0 ms time period. (A5-A11 must remain constant at proper logic levels.) This refresh can be done in a burst mode (32 cycles starting every 2.0 ms) or in a distributed mode where one cycle is done every 62.5 μs.

A refresh abort can be accomplished by treating a refresh cycle as a read-modify-write cycle with $\overline{CS}$ high. This type of cycle can be aborted any time until the R/W signal has been brought low to allow a $\phi 3$ clock to begin.

Non-Volatile Storage

In many digital systems, it is extremely important to retain data during emergencies such as power failure. Unfortunately, however, most random access read/write semiconductor memories such as the MCM6605A are volatile. That is, if power is removed from the semiconductor memory, stored information is lost. Therefore, non-volatility for a specified period of time becomes highly desirable — as a necessity to maintain irreplaceable information or as a convenience to avoid the time consuming and troublesome task of having to reload the memory.

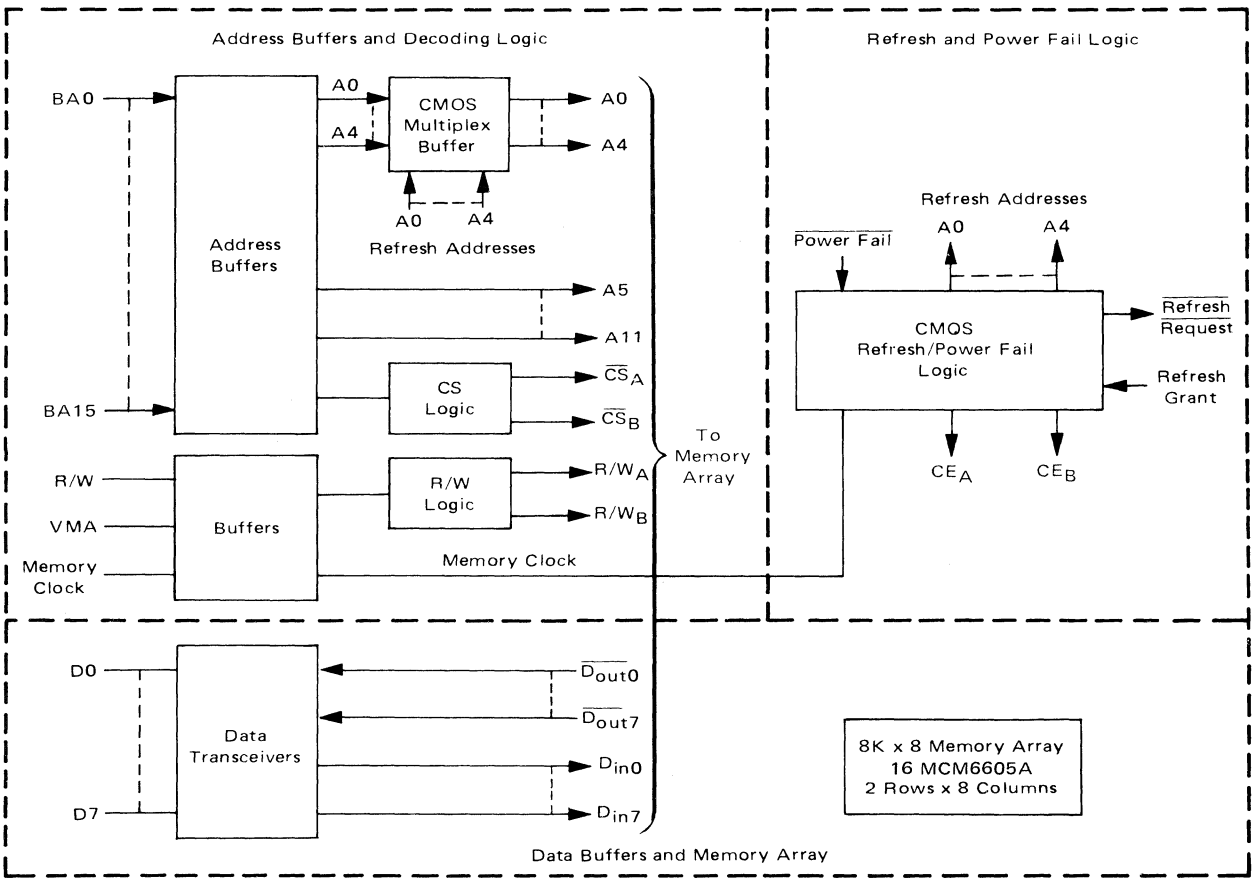
The extremely low standby power dissipation of the MCM6605A makes it ideal for main memory applications requiring battery backup for non-volatility. For example, the MCM6605A can be employed in an 8K byte non-volatile main memory system application for microprocessors. The memory system can be partitioned into three major sections as illustrated in Figure 13. The first section contains the address buffers and the Read/Write and Chip Select decoding logic. The second section consists of the data bus buffering transceivers and the memory array (which consists of 16 MCM6605As) organized into two rows of 4K bytes each.

The third section of the block diagram comprises refresh and control logic for the memory system. This logic interfaces the timing of the refresh handshaking with the microprocessor (MPU) clock circuitry. It handles requests for refresh, the generation of refresh addresses, the synchronization of a $\overline{\text{Power Fail}}$ signal, the multiplexing of the external Memory Clock with the internal clock (used during standby), and the generation of a −5 V supply on the board using a charge-pump method.

The refresh control logic is illustrated in Figure 14. It handles the refreshing of the memory during both operating and standby modes. The timing for this logic is given in Figure 15. Figure 16 gives the memory timing for the standby mode only. Decoding of the memory clock (CE_A and CE_B) and the circuitry to synchronize the $\overline{\text{Power Fail}}$ signal are shown in Figure 17, with the timing given in Figure 18.

The memory device clock (CE_A and CE_B) during standby is created by a monostable multivibrator (MC14528) and buffered from the memory array by three MC14503 buffers in parallel. This clock is multiplexed with the $\overline{\text{Memory Clock}}$ by use of the three-state feature of the

FIGURE 13 – NON-VOLATILE MEMORY SYSTEM BLOCK DIAGRAM



MC14503. The $\overline{\text{Memory Clock}}$ (used during normal operation) is translated to 12 V levels by use of an MC3460 Clock Driver. Decoding of the CE_A and CE_B signals (i.e., clocking only the memory bank addressed) to conserve power is accomplished by the logic within the MC3460.

Since the $\overline{\text{Power Fail}}$ signal will occur asynchronously with both the $\overline{\text{Memory Clock}}$ and the refreshing operation (Refresh Clock), it is necessary to synchronize the $\overline{\text{Power Fail}}$ signal to the rest of the system in order to avoid aborting a memory access cycle or a refresh cycle. An MC14027 dual flip-flop is used as the basic synchronization device. The leading edge of the Refresh Clock triggers a 3 μs monostable multivibrator which is used as a refresh pretrigger. The trailing edge of this pretrigger triggers a 500 ns monostable which creates the CE pulse during standby operation. The 3 μs pretrigger signal is used to set half of the MC14027 flip-flop, the output of which, Ⓑ, then inhibits a changeover from the standby to the operating modes (or vice versa). This logic prevents the system from aborting a refresh cycle should the $\overline{\text{Power Fail}}$ signal change states just prior to or during a refresh cycle. The trailing edge of the 500 ns monostable clears the MC14027 flip-flop, enabling the second flip-flop in the package. The state of $\overline{\text{Power Fail}}$ and Power Fail is applied to the K and J inputs of this second flip-flop and is synchronized by clocking with $\overline{\text{Memory Clock}}$. The outputs of this flip-flop, labeled Bat and $\overline{\text{Bat}}$, lock the system into the refresh mode and multiplex in the internal clock for standby operation when Bat = "1". The voltage to logic not required for the refresh only mode of operation is removed to conserve power.

By using CMOS for the refresh logic and capacitance drivers, and a low current refresh oscillator, the standby current required for the 8K byte system is extremely small, as noted in Table 1. This low standby current requirement can be easily supplied for several days with standard type +12 V batteries. For more detailed information on this sytem and a large mainframe memory system, see Application Notes AN-732 and AN-740.

FIGURE 14 – REFRESH CONTROL LOGIC

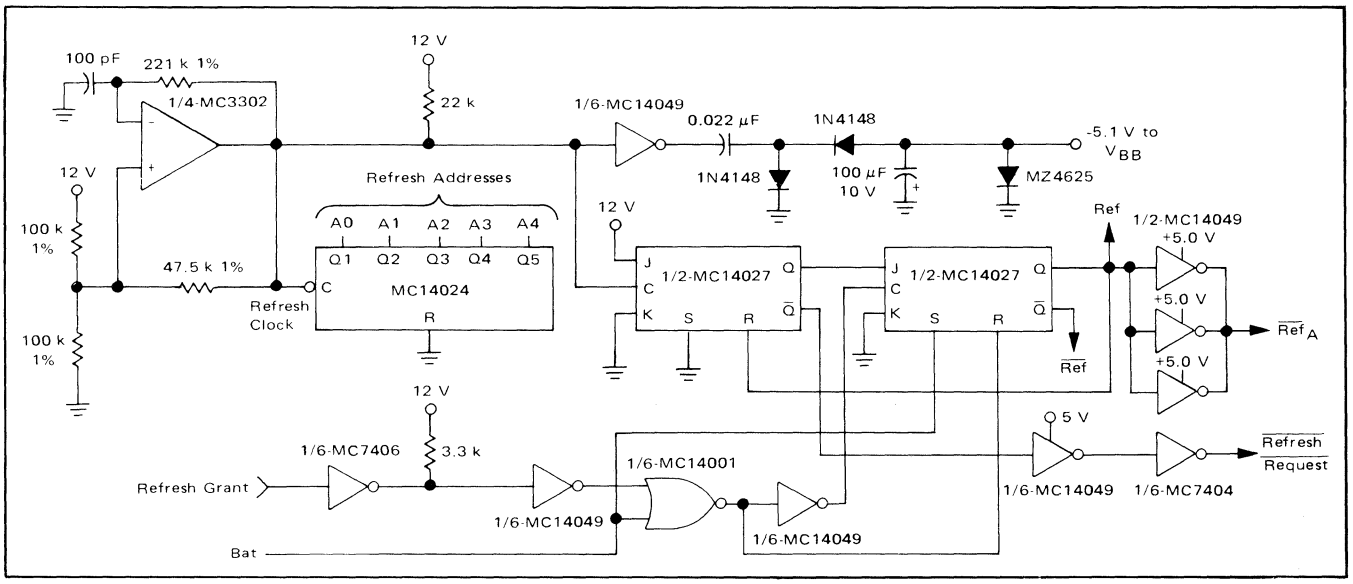


FIGURE 15 – REFRESH TIMING

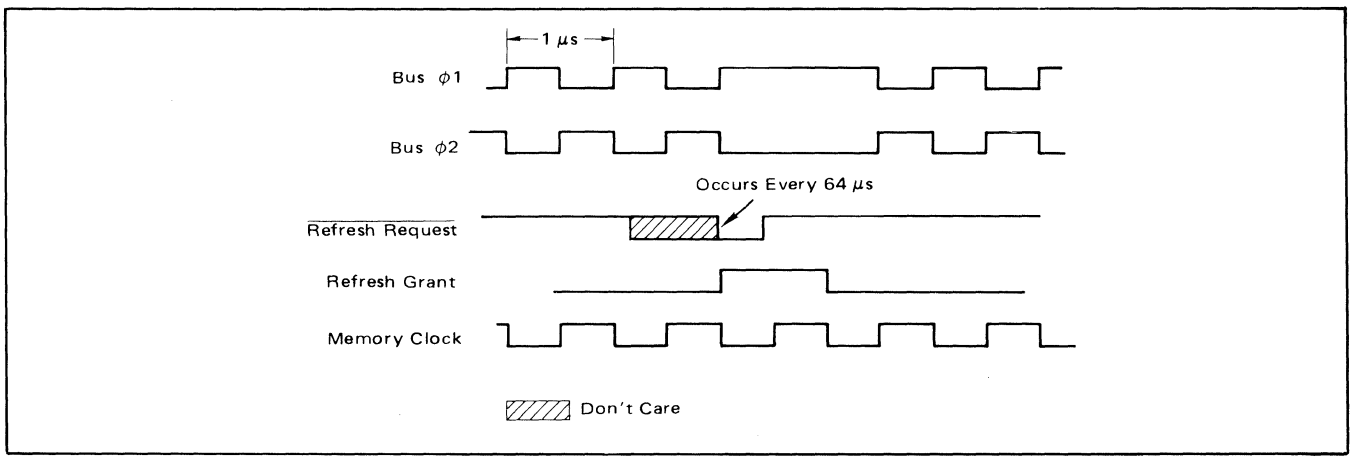


FIGURE 16 – MEMORY TIMING IN STANDBY MODE

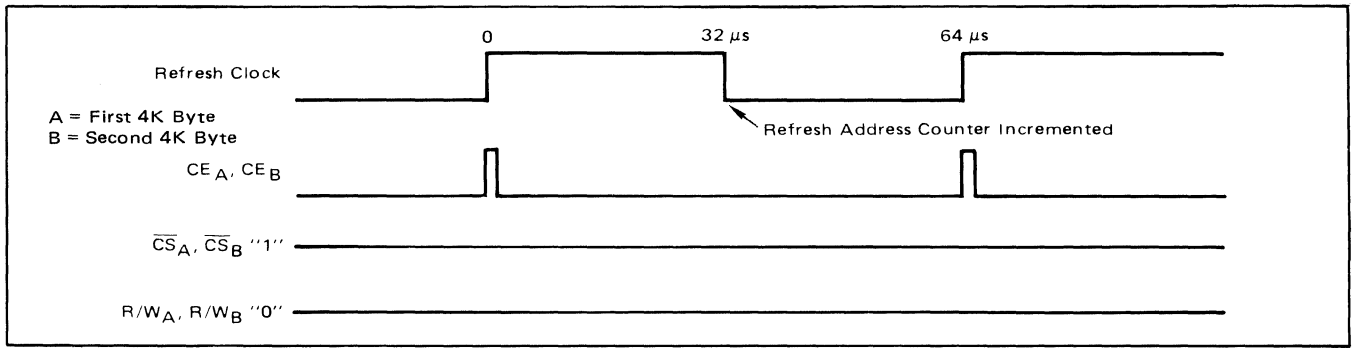


FIGURE 17 – POWER FAIL LOGIC AND CHIP ENABLE DRIVER

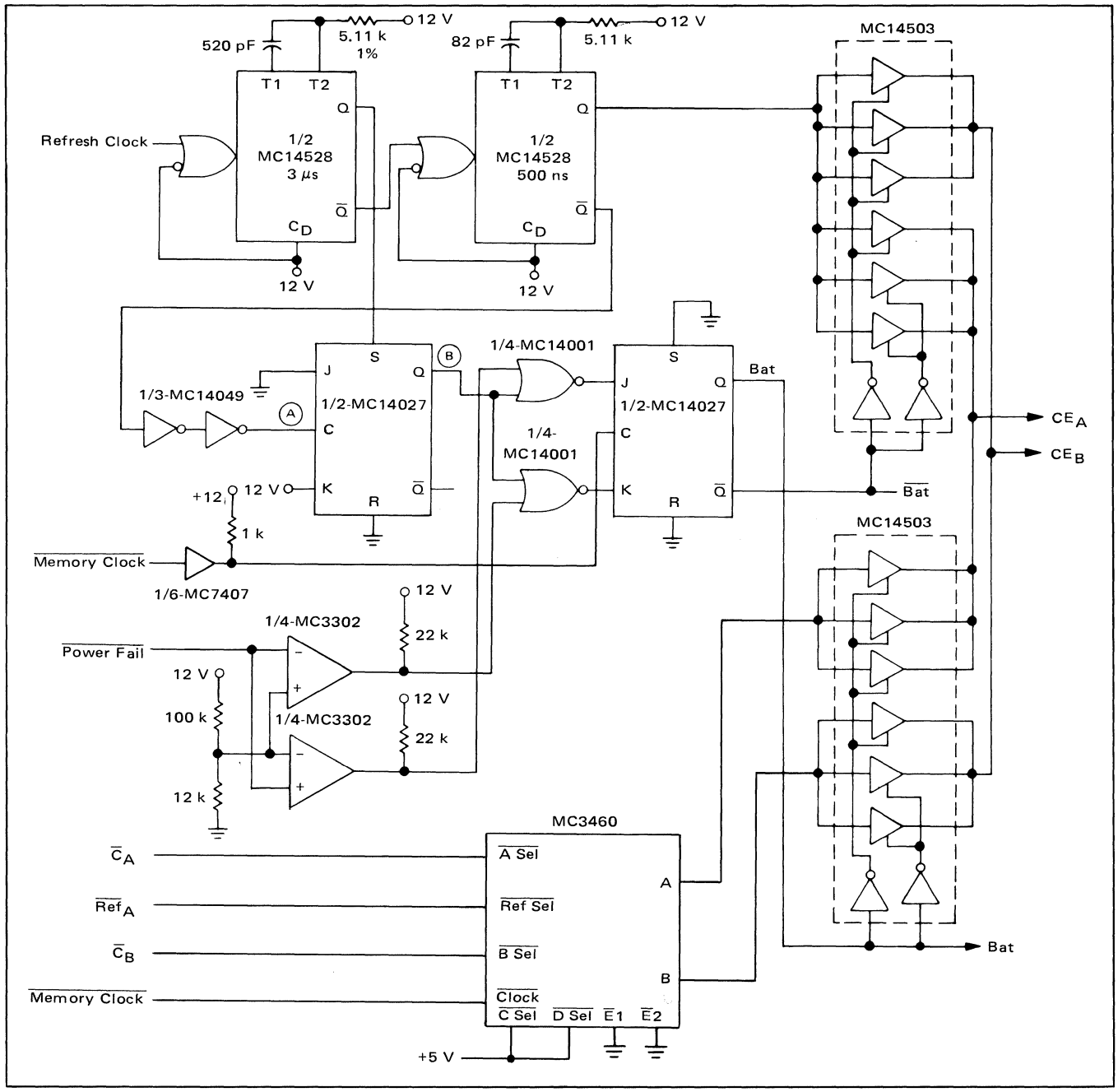


FIGURE 18 – POWER UP/DOWN SYNCHRONIZATION

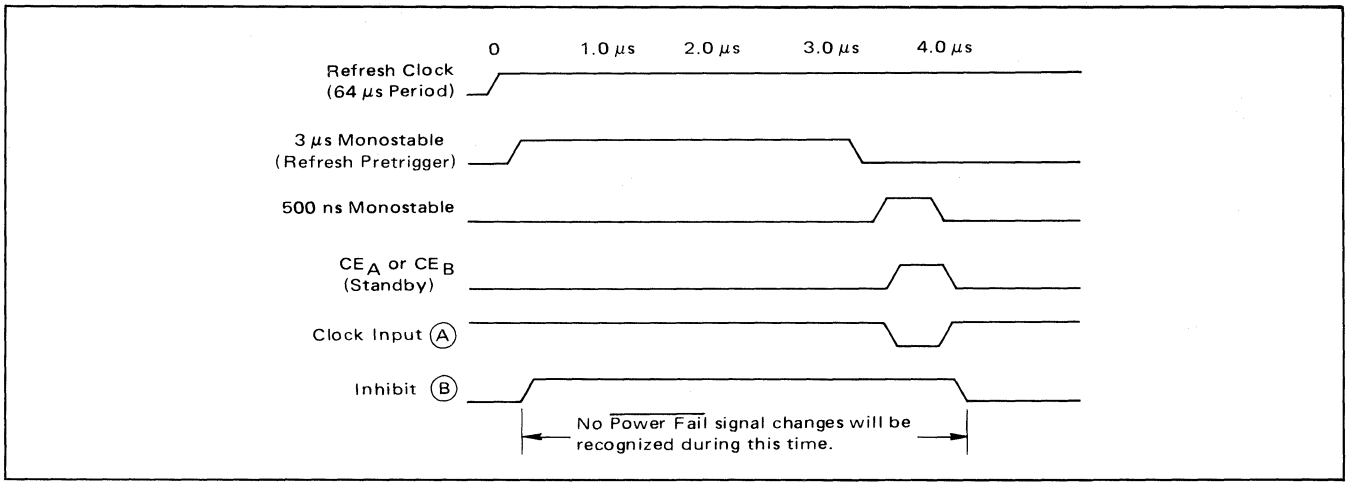
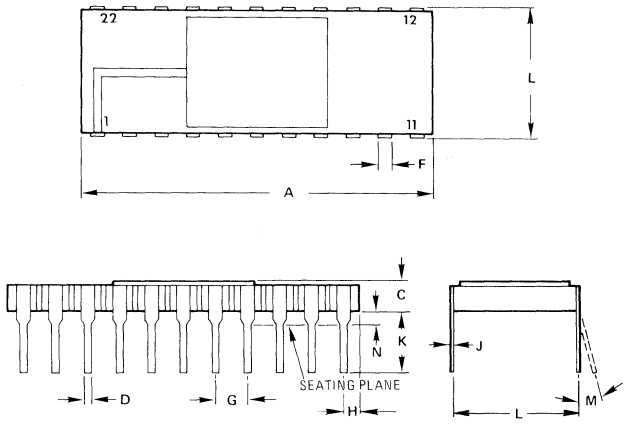


TABLE 1 – STANDBY MODE CURRENT ALLOCATION

Circuit Section	Typical Current
+12 V Current (V_{DD}) for 16 MCM6605A's	5 mA
Charge Pump	3 mA
Comparator	2 mA
Capacitance Drivers	4 mA
Total	14 mA

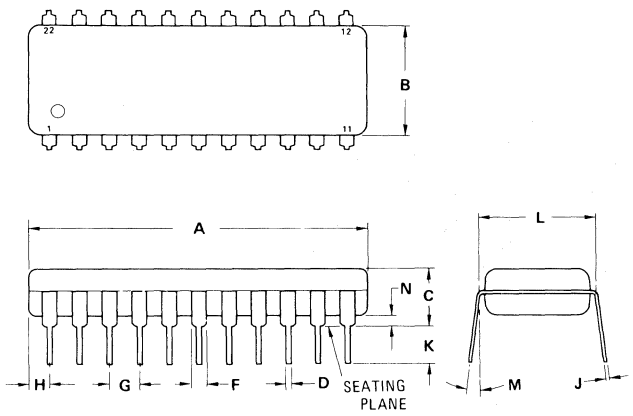
PACKAGE DIMENSIONS



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	27.05	27.94	1.065	1.100
C	2.16	3.68	0.085	0.145
D	0.43	0.58	0.017	0.023
F	1.02 REF		0.040 REF	
G	2.54 BSC		0.100 BSC	
H	0.76	1.78	0.030	0.070
J	0.20	0.30	0.008	0.012
K	3.18	4.45	0.125	0.175
L	9.65	10.67	0.380	0.420
M	–	7^0	–	7^0
N	0.64	1.27	0.025	0.050

NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.

CERAMIC PACKAGE
CASE 677-03



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	28.83	29.59	1.135	1.165
B	8.64	9.14	0.340	0.360
C	4.57	5.08	0.180	0.200
D	0.36	0.51	0.014	0.020
F	1.02	1.52	0.040	0.060
G	2.41	2.67	0.095	0.105
H	1.78	2.03	0.070	0.080
J	0.20	0.30	0.008	0.012
K	3.05	3.56	0.120	0.140
L	9.65	10.16	0.380	0.400
M	0^0	10^0	0^0	10^0
N	0.51	1.02	0.020	0.040

PLASTIC PACKAGE
CASE 708-01

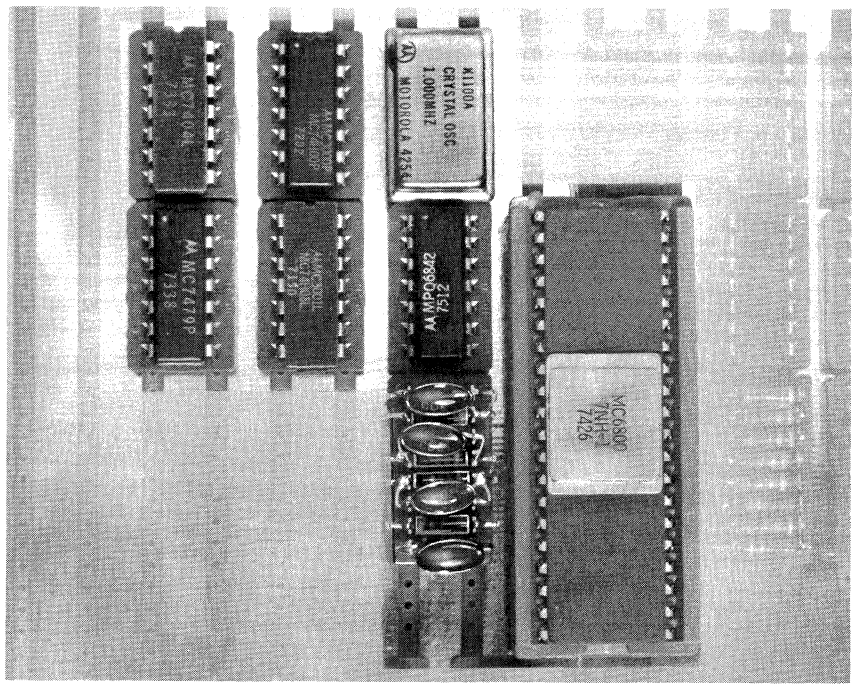
MOTOROLA
Semiconductors
BOX 20912 • PHOENIX, ARIZONA 85036

MPQ6842

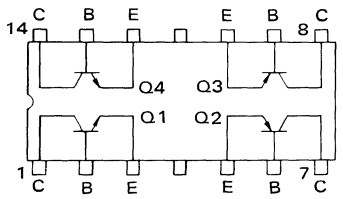
MPU CLOCK BUFFER

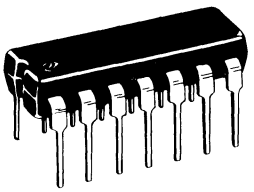
The MPQ6842 is designed to provide the switching speed and saturation voltages necessary in the clock circuit for the $\phi 1$ and $\phi 2$ inputs of the MC6800 Microprocessor.

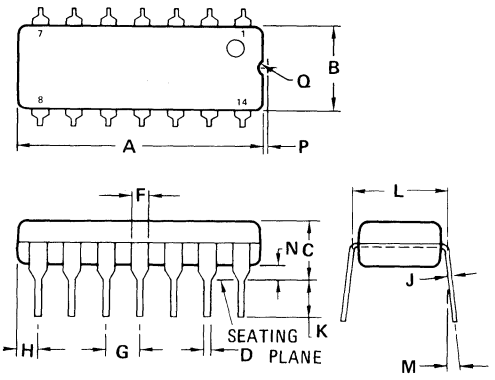
MPU CLOCK BUFFER



CONNECTION DIAGRAM







DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	18.16	18.80	0.715	0.740
B	6.10	6.60	0.240	0.260
C	4.06	4.57	0.160	0.180
D	0.38	0.51	0.015	0.020
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.32	1.83	0.052	0.072
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.37	7.87	0.290	0.310
M	–	10^0	–	10^0
N	0.51	1.02	0.020	0.040
P	0.13	0.38	0.005	0.015
Q	0.51	0.76	0.020	0.030

NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL

CASE 646
PLASTIC PACKAGE

MAXIMUM RATINGS

Rating	Symbol	Value		Unit
Collector-Emitter Voltage	V_{CEO}	30		Vdc
Collector-Base Voltage	V_{CB}	30		Vdc
Emitter-Base Voltage	V_{EB}	4.0		Vdc
Collector Current – Continuous	I_C	200		mAdc
		Each Transistor	Four Transistors Equal Power	
Total Power Dissipation @ $T_A = 25^oC$ (1) Derate above 25^oC	P_D	500 4.0	900 7.2	mW mW/^oC
Total Power Dissipation @ $T_C = 25^oC$ Derate above 25^oC	P_D	825 6.7	2400 19.2	mW mW/^oC
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−55 to +150		^oC

(1) Second Breakdown occurs at power levels greater than 3 times the power dissipation rating.

THERMAL CHARACTERISTICS

Characteristic		Junction to Case	Junction to Ambient	Unit
Thermal Resistance	Each Die	151	250	$^oC/W$
	Effective, 4 Die	52	139	$^oC/W$
Coupling Factors	Q1-Q4 or Q2-Q3	34	70	%
	Q1-Q2 or Q3-Q4	2.0	26	%

THERMAL COUPLING AND EFFECTIVE THERMAL RESISTANCE

In multiple chip devices, coupling of heat between die occurs. The junction temperature can be calculated as follows:

(1) $\Delta T_{J1} = R_{\theta 1} P_{D1} + R_{\theta 2} K_{\theta 2} P_{D2} + R_{\theta 3} K_{\theta 3} P_{D3} + R_{\theta 4} K_{\theta 4} P_{D4}$

Where ΔT_{J1} is the change in junction temperature of die 1
$R_{\theta 1}$ thru 4 is the thermal resistance of die 1 through 4
P_{D1} thru 4 is the power dissipation in die 1 through 4
$K_{\theta 2}$ thru 4 is the thermal coupling between die 1 and die 2 through 4.

An effective package thermal resistance can be defined as follows:

(2) $R_{\theta (EFF)} = \Delta T_{J1}/P_{DT}$

Where: P_{DT} is the total package power dissipation.

Assuming equal thermal resistance for each die, equation (1) simplifies to

(3) $\Delta T_{J1} = R_{\theta 1} (P_{D1} + K_{\theta 2} P_{D2} + K_{\theta 3} P_{D3} + K_{\theta 4} P_{D4})$

For the conditions where $P_{D1} = P_{D2} = P_{D3} = P_{D4}$, $P_{DT} = 4P_D$, equation (3) can be further simplified and by substituting into equation (2) results in

(4) $R_{\theta (EFF)} = R_{\theta 1} (1 + K_{\theta 2} + K_{\theta 3} + K_{\theta 4}) /4$

Values for the coupling factors when either the case or the ambient is used as a reference are given in the table on page 1. If significant power is to be dissipated in two die, die at the opposite ends of the package should be used so that lowest possible junction temperatures will result.

ELECTRICAL CHARACTERISTICS ($T_A = 25^oC$ unless otherwise noted.)

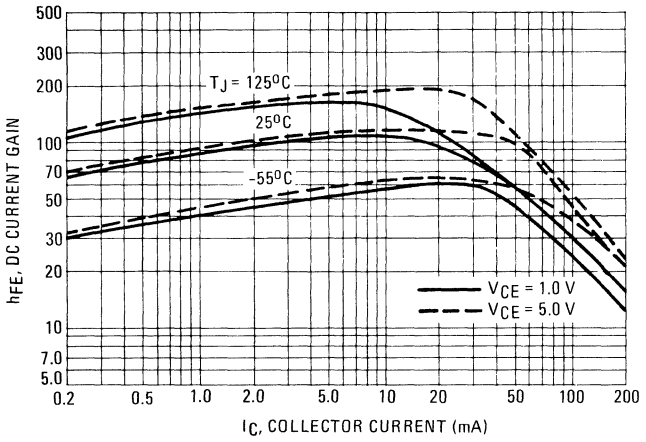
Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (1) (I_C = 10 mAdc, I_B = 0)	BV_{CEO}	30	–	–	Vdc
Collector-Base Breakdown Voltage (I_C = 10 μAdc, I_E = 0)	BV_{CBO}	30	–	–	Vdc
Emitter-Base Breakdown Voltage (I_E = 10 μAdc, I_C = 0)	BV_{EBO}	4.0	–	–	Vdc
Collector Cutoff Current (V_{CB} = 20 Vdc, I_E = 0)	I_{CBO}	–	–	50	nAdc
Emitter Cutoff Current (V_{EB} = 3.0 Vdc, I_C = 0)	I_{EBO}	–	–	50	nAdc
ON CHARACTERISTICS (1)					
DC Current Gain	h_{FE}				–
(I_C = 0.5 mAdc, V_{CE} = 1.0 Vdc)		30	–	–	
(I_C = 1.0 mAdc, V_{CE} = 1.0 Vdc)		50	–	–	
(I_C = 10 mAdc, V_{CE} = 1.0 Vdc)		70	–	–	
Collector-Emitter Saturation Voltage (I_C = 0.5 mAdc, I_B = 0.05 mAdc, $0^oC \leq T \leq 70^oC$)	$V_{CE(sat)}$	–	0.05	0.15	Vdc
Base-Emitter Saturation Voltage (I_C = 0.5 mAdc, I_B = 0.05 mAdc)	$V_{BE(sat)}$	–	0.65	0.9	Vdc
DYNAMIC CHARACTERISTICS					
Current-Gain – Bandwidth Product (1) (I_C = 10 mAdc, V_{CE} = 20 Vdc, f = 100 MHz)	f_T	200	350	–	MHz
Output Capacitance (V_{CB} = 5.0 Vdc, I_E = 0, f = 100 kHz)	C_{ob}	–	3.0	4.5	pF
Input Capacitance	C_{ib}				pF
(V_{EB} = 0.5 Vdc, I_C = 0, f = 100 kHz) PNP		–	5.0	10	
NPN		–	4.0	8.0	
SWITCHING CHARACTERISTICS ($T_A = 25^oC$, V_{CC} = 5.0 Vdc)					
Propagation Delay Time					ns
(50% Points TP1 to TP3)	t_{PLH}	–	15	25	
(50% Points TP2 to TP4)	t_{PHL}	–	6.0	15	
Rise Time (0.3 V to 4.7 V, TP3 or TP4)	t_r	5.0	25	35	ns
Fall Time (4.7 V to 0.3 V, TP3 or TP4)	t_f	5.0	10	20	ns

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

NPN

PNP

FIGURE 1 – DC CURRENT GAIN



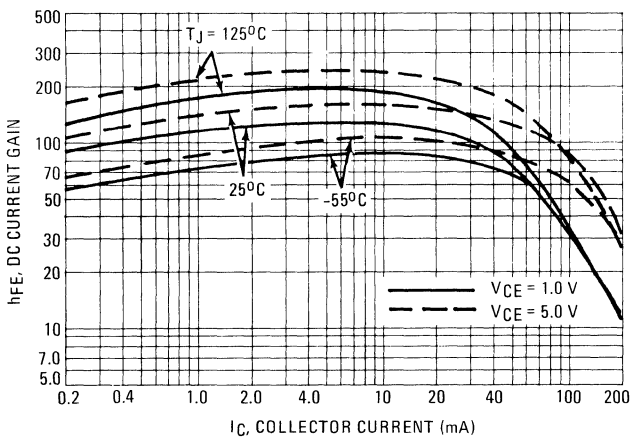
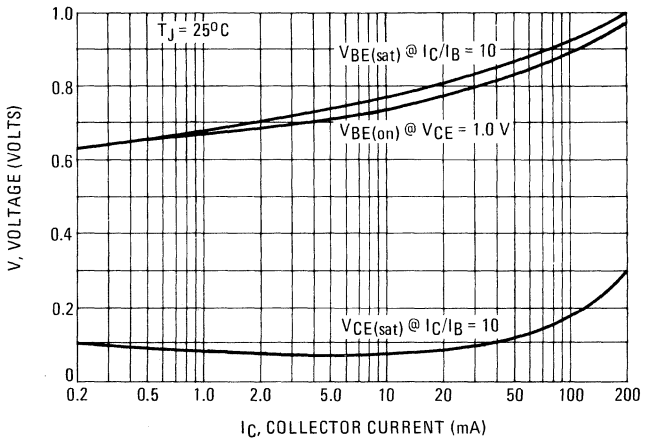


FIGURE 2 – "ON" VOLTAGE



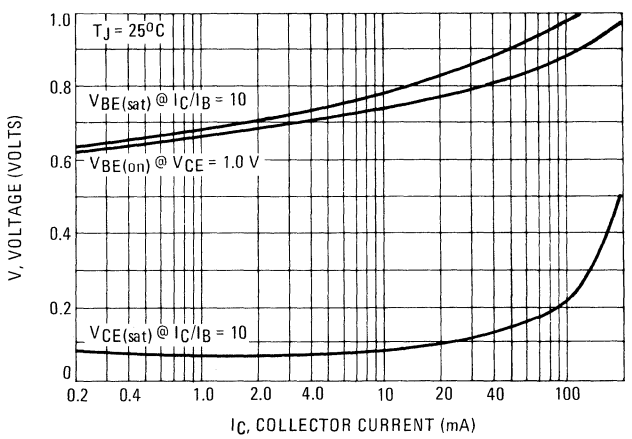
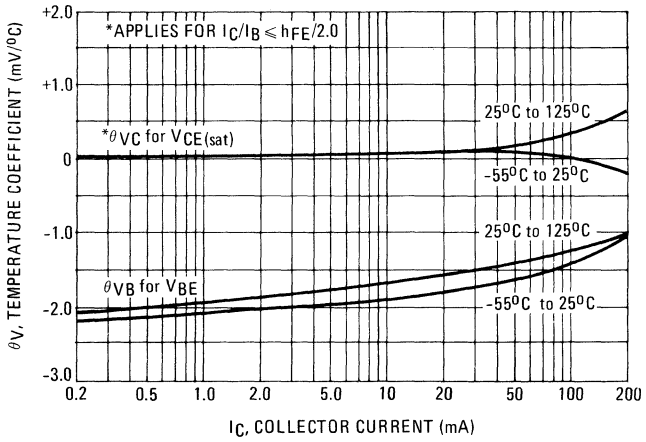
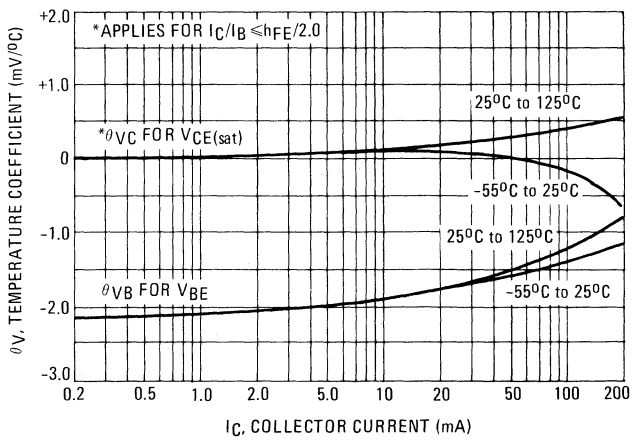


FIGURE 3 – TEMPERATURE COEFFICIENTS





NPN

PNP

FIGURE 4 – COLLECTOR SATURATION REGION

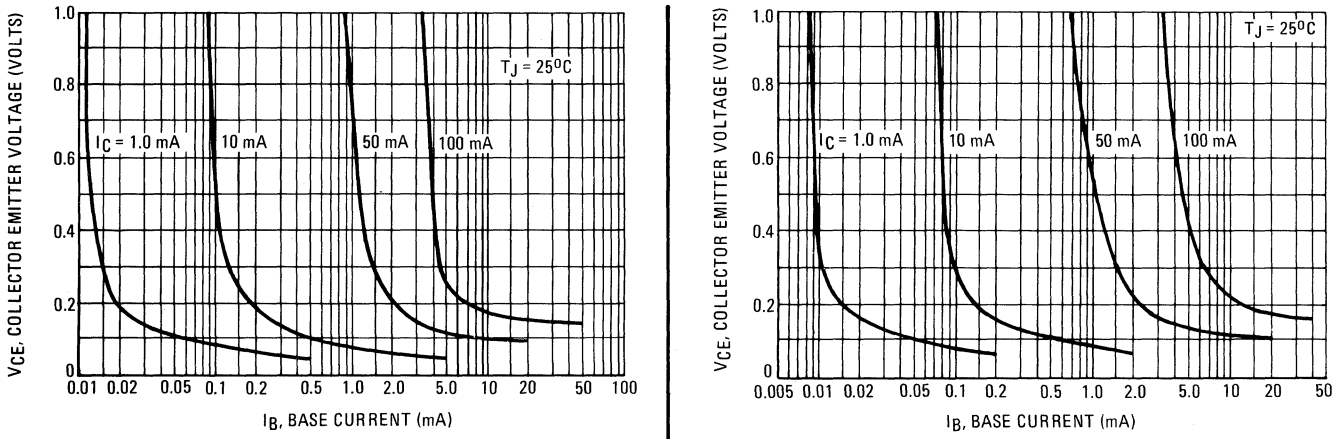
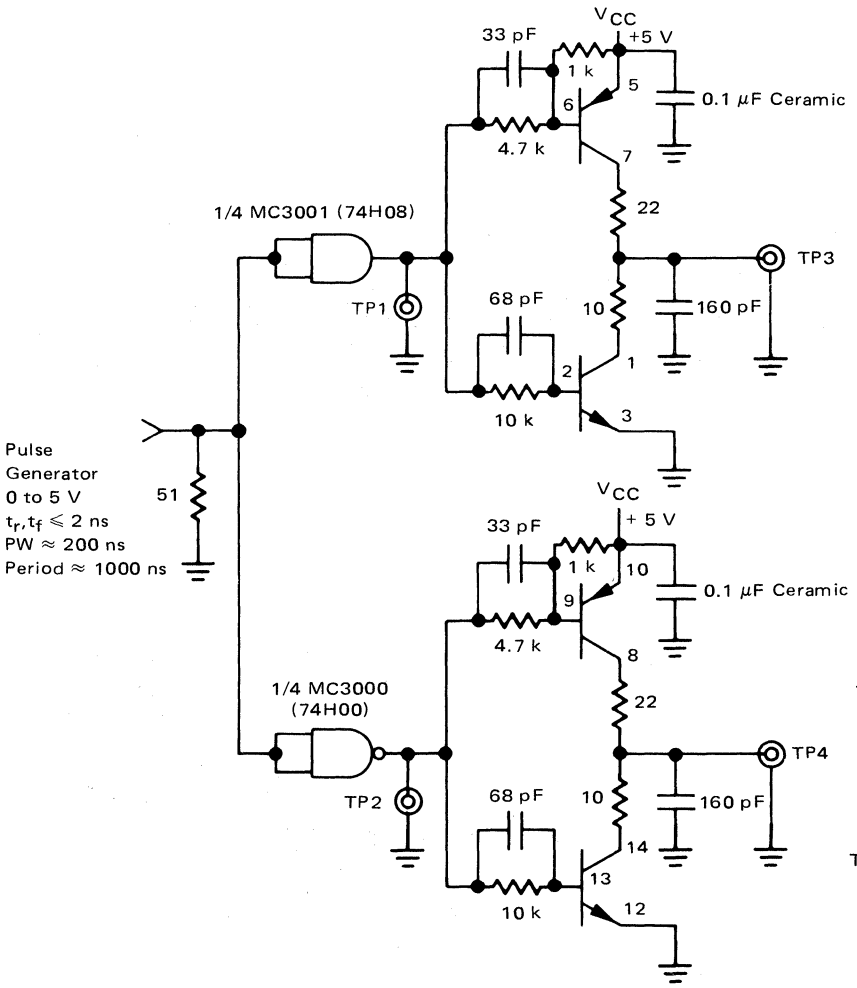
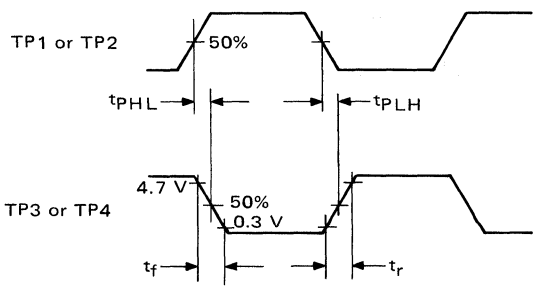


FIGURE 5 – SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS



NOTES:

1. Unless otherwise noted, all resistors carbon composition ¼ W ±5%, all capacitors dipped mica ±2%.
2. Use short interconnect wiring with good power and ground busses.
3. TP1 thru TP4 are coaxial connectors to accept scope probe tip and provide a good ground.
4. Device under test is MPQ6842.
5. 160 pF load does not include stray or scope probe capacitance.
6. Scope probe resistance > 5 kΩ. Scope probe capacitance < 10 pF.



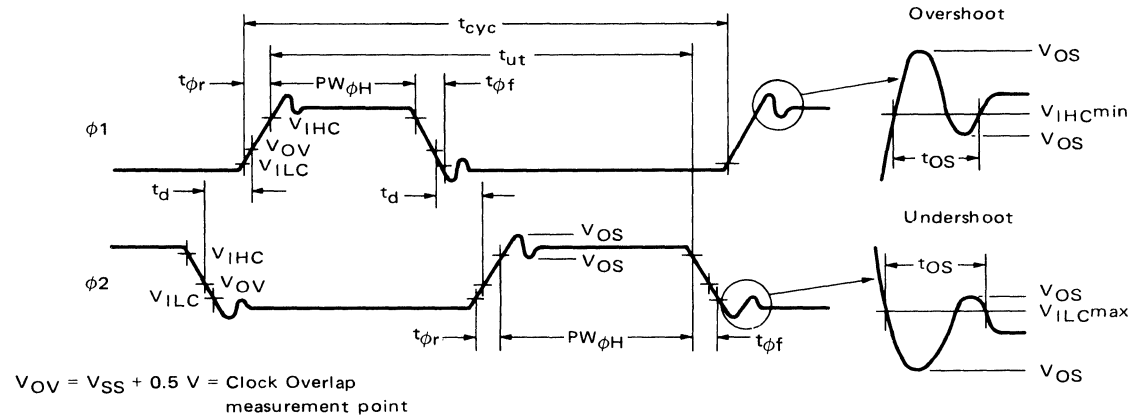
APPLICATIONS INFORMATION#

Figure 6 is a summary of the MC6800 Microprocessor clock waveform requirements. The $\phi1$ and $\phi2$ clock inputs require complementary 1 MHz, 5 volt non-overlapping clocks. The clock inputs of the MPU appear primarily capacitive, being 120 pF typical and 160 pF maximum with 100 μAdc leakage. Provision is made in the specification for the undershoot and overshoot that will result from the generation of a high speed transition into a capacitive load.

The clock specifications which constrain the clock driver are the rise and fall times required to meet the pulse widths at the maximum operating frequency of 1 MHz, the non-overlapping requirement, the logic level requirements of V_{SS} + 0.3 volt and V_{CC} - 0.3 volt, the overshoot specification, and the MPU input capacitance. The clock buffer circuit that drives the MPU clock inputs must be designed to meet the rise and fall time requirements as well as provide the proper logic levels into the load capacitance, within the overshoot constraints. The non-overlapping requirements of the clock signal can be met by the design of the control logic which drives the buffers. The MPQ6842 clock buffer can guarantee the clock designer the speed and saturation voltages necessary to design the clock circuit to meet the MPU clock requirements.

Figure 7 is a circuit designed with TTL logic devices and the MPQ6842 buffer to meet the MPU clock requirements while operating from a single +5 volt supply. The oscillator

FIGURE 6 – MPU CLOCK SPECIFICATION



$V_{OV} = V_{SS} + 0.5$ V = Clock Overlap measurement point

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V ± 5%, V_{SS} = 0, T_A = 0 to 70°C unless otherwise noted.)

Characteristic		Symbol	Min	Typ	Max	Unit
Input High Voltage	φ1,φ2	V_{IHC}	V_{CC}-0.3	–	V_{CC} + 0.1	Vdc
Input Low Voltage	φ1,φ2	V_{ILC}	V_{SS}-0.1	–	V_{SS} + 0.3	Vdc
Clock Overshoot/Undershoot – Input High Level – Input Low Level		V_{OS}	V_{CC}-0.5 V_{SS}-0.5	– –	V_{CC}+0.5 V_{SS} + 0.5	Vdc
Input Leakage Current (V_{in} = 0 to 5.25 V, V_{CC} = 0 V)	φ1,φ2	I_{in}	–	–	100	μAdc
Capacitance* (V_{in} = 0, T_A = 25°C, f = 1.0 MHz)		C_{in}	80	120	160	pF
Frequency of Operation		f	0.1	–	1.0	MHz
Clock Timing						
Cycle Time		t_{cyc}	1.0	–	10	μs
Clock Pulse Width (Measured at V_{CC} - 0.3 V)	φ1 φ2	$PW_{\phi H}$	430 450	– –	4500 4500	ns
Total φ1 and φ2 Up Time		t_{ut}	940	–	–	ns
Rise and Fall Times (Measured between V_{SS} + 0.3 V and V_{CC} - 0.3 V)	φ1,φ2	$t_{\phi r}$, $t_{\phi f}$	5.0	–	50	ns
Dealy Time or Clock Separation (Measured at $V_{OV} = V_{SS} + 0.5$ V)		t_d	0	–	9100	ns
Overshoot Duration		t_{OS}	0	–	40	ns

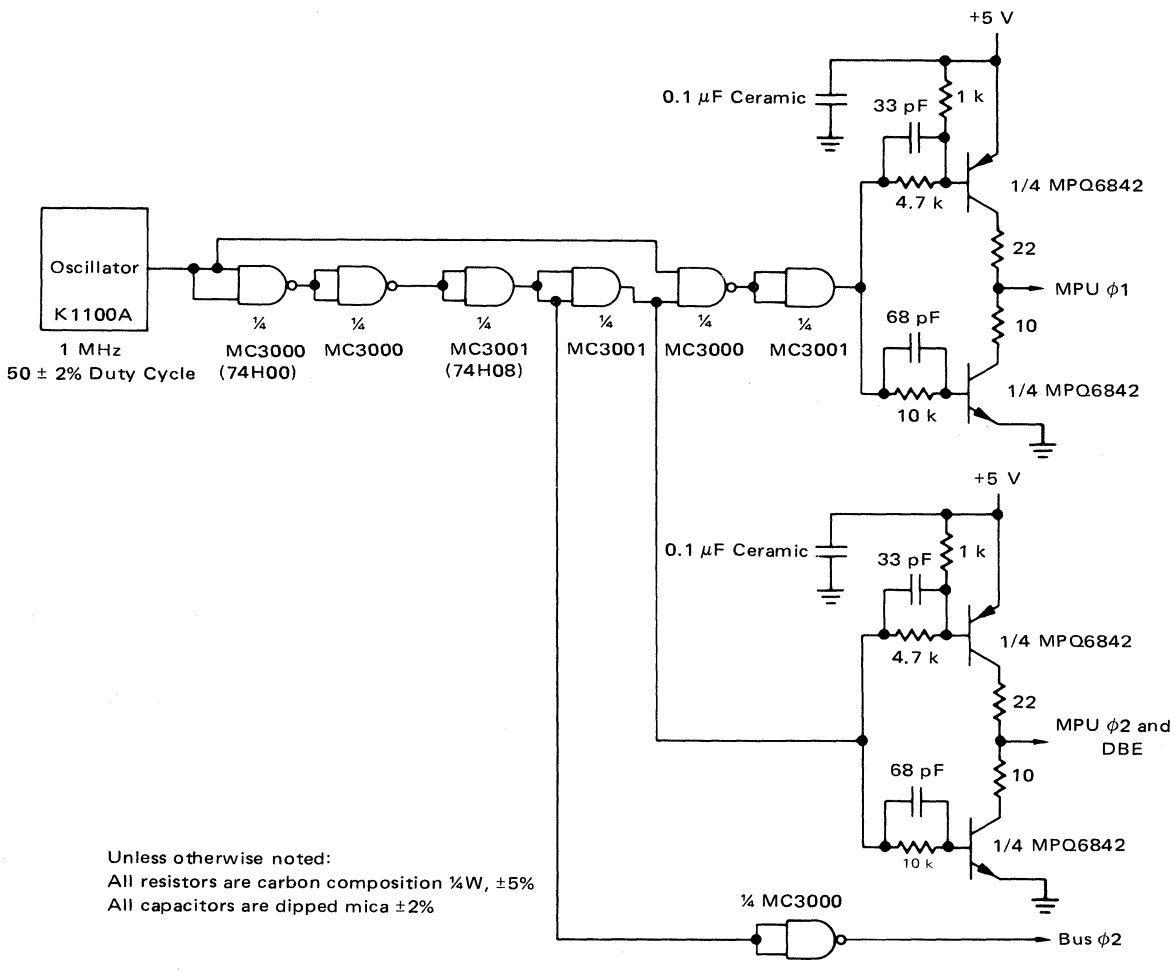
*Capacitances are periodically sampled rather than 100% tested.

#For further information on M6800 system usage, refer to the M6800 Applications Manual.

can be any source with a maximum frequency of 1 MHz, TTL logic levels and a 50% duty cycle. This oscillator signal source could vary from a commercial oscillator, such as a K1100A available from Motorola's Component Products Department,[1] to a signal derived from a higher frequency signal already available in the system. The TTL gates shown are standard MC3000 and MC3001 (74H00 and 74H08) gates which were chosen for their speed and drive characteristics. The discrete buffers require good "1" level pullup and drive capability which is provided by the MC3001. The circuit was constructed on a wirewrap board and tested on an EXORciser.[2] Good power and ground distribution practice was followed but no special care was taken in parts layout.

Waveforms typical of the circuit in Figure 7 are shown in Figures 8a and 8b, with T_A = 20°C and V_{CC} = 5.0 volts. These figures depict the logic levels and pulse widths achieved by this circuitry with V_{CC} and Ground as reference levels. Figure 8c superimposes the two clock waveforms so that their phase relationship can be seen. Figure 8d shows the phase relationship of Bus ϕ2 and MPU ϕ2. Figures 8e and 8f examine the non-overlap regions as well as rise and fall times typical of this clock driver circuit. Table 1 presents test data taken over a voltage range of 4.75 volts to 5.25 volts and over a temperature range of 0°C to 70°C. Note the stability of these measured parameters, and that the logic levels achieved will provide noise margin on the system clocks.

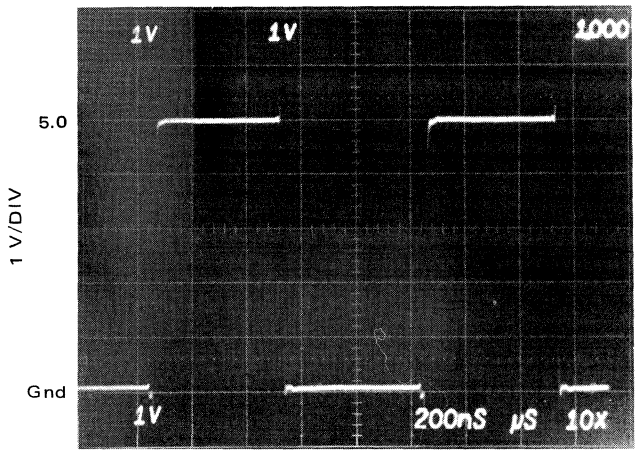
FIGURE 7 – MPU CLOCK CIRCUIT



1. 2553 N. Edgington, Franklin Park, Illinois 60131, (312) 451-1000.
2. A prototyping system for the M6800 family.

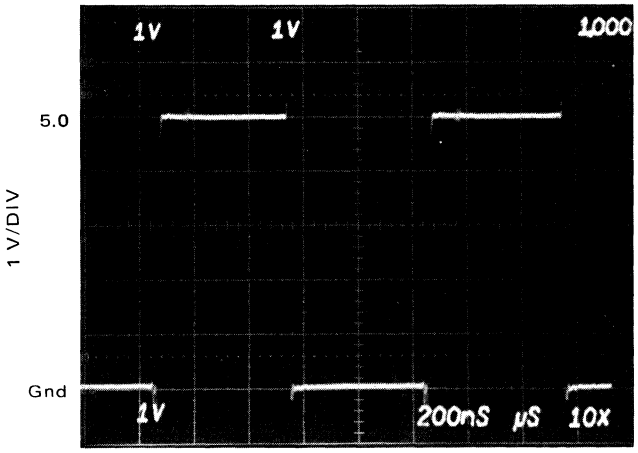
CLOCK CIRCUIT WAVEFORMS
(Using Circuit of Figure 7)

FIGURE 8a – MPU ϕ1 CLOCK



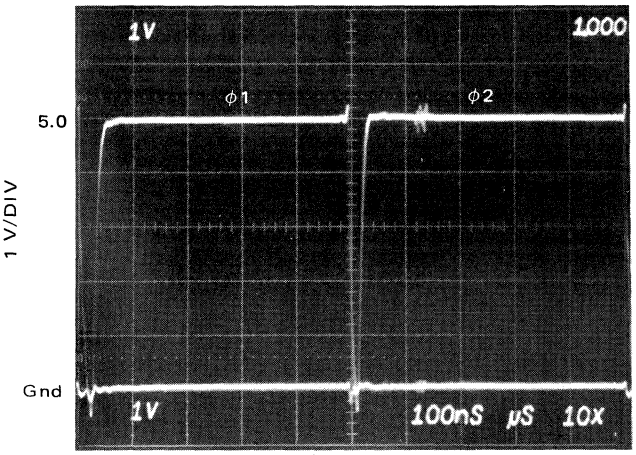
200 ns/DIV

FIGURE 8b – MPU ϕ2 CLOCK



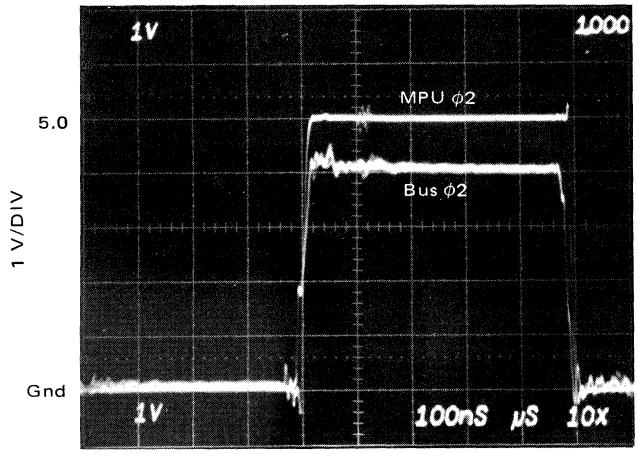
200 ns/DIV

FIGURE 8c – MPU ϕ1 AND ϕ2 CLOCKS



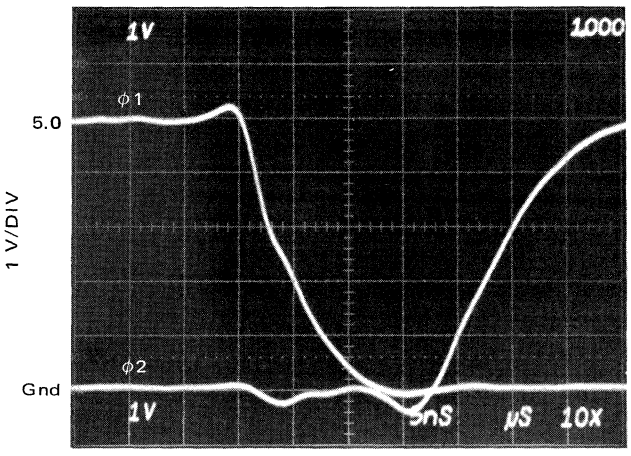
100 ns/DIV

FIGURE 8d – MPU ϕ2 CLOCK AND BUS ϕ2



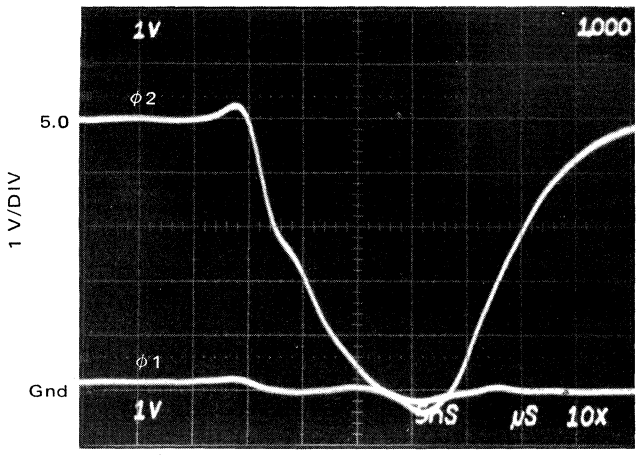
100 ns/DIV

FIGURE 8e – MPU CLOCK NON-OVERLAP REGION
ϕ1 to ϕ2



5 ns/DIV

FIGURE 8f – MPU CLOCK NON-OVERLAP REGION
ϕ2 to ϕ1



5 ns/DIV

Both $\phi 1$ and $\phi 2$ clock high times were designed to be 15-30 ns wider than the minimum required by the MPU ($\phi 1$ = 430 ns, $\phi 2$ = 450 ns) to provide system margin. Rise and fall times were minimized to provide maximum clock high times consistent with non-critical circuit layout considerations. The overlap margin shown easily meets the MPU requirement of 0 ns at 0.5 volt but will decrease as the capacitive loading increases, as shown in Table 1. The MPU tested for this data had a typical clock input capacitance of 120 pF.

In many systems, especially in the breadboard and evaluation stage, it may be desirable to have the flexibility to vary the system clock to test the effects on data throughput, real time operation with interrupts, or to help diagnose a system timing problem. In these applications, or in those not requiring crystal oscillator stability, an even simpler clock circuit can be used. A pair of cross coupled monostable multivibrators with individual pulse width adjustments can be used as the clock oscillator with the previously described clock buffer circuit. This approach is shown in Figure 9. The non-overlapping clock is generated by the propagation delays through the monostable multivibrators. Figures 10a – 10d show waveforms resulting from this circuit. Table 2 shows test data taken of this circuit over the voltage and temperature range. Note the small variations in the pulse widths.

The fast rise and fall times produced by this circuitry and the highly capacitive loads require some care in layout to avoid excessive ringing and/or pulse distortion. While no particular care was taken in the construction of the wire-wrap test boards other than placing all of the discrete devices into one header board, the following construction guidelines are recommended. Wide power and ground lines (50-100 mils) should be used to provide low impedance voltage and ground sources. The clock driver should be physically located as near the MPU as possible to avoid ringing down long lines. Close proximity of the clock circuitry to the MPU allows common power and ground connections so that any noise appears common mode rather than differential to the MPU and clock driver. Finally, it is recommended that the MPU $\phi 2$ clock signal not be used to clock any device other than the MPU so that it is not distributed all over the system with the possibility of picking up noise and causing reflections. The circuits shown provide an additional buffer for the other $\phi 2$ loads in the system to isolate MPU $\phi 2$ from all the other $\phi 2$ loads.

TABLE 1 – PERFORMANCE OF CIRCUIT OF FIGURE 7
(C_L = 120 pF unless otherwise noted.)

Test Conditions	MPU $\phi 1$					MPU $\phi 2$					Non-Overlap Region	
	PW	t_r	t_f	"1" LL*	"0" LL*	PW	t_r	t_f	"1" LL*	"0" LL*	$\phi 1\downarrow$ to $\phi 2\uparrow$	$\phi 2\downarrow$ to $\phi 1\uparrow$
T = 20°C												
V_{CC} = 4.75 V	460 ns	15 ns	10 ns	4.75 V	0.1 V	465 ns	15 ns	10.5 ns	4.75 V	0 V	10.5 ns	12 ns
V_{CC} = 5.00 V	460	16	11	5.00	0.1	465	16	10	5.00	0	10	11
V_{CC} = 5.25 V	460	16	11	5.25	0.1	465	16	11	5.25	0	9.5	10.5
V_{CC} = 5.00 V, (C_L = 210 pF)	450	21	15.5	5.00	0.1	460	22	15	5.00	0	2	5.5
T = 70°C												
V_{CC} = 4.75 V	460	15	12	4.75	0.1	465	16	12	4.75	0	9	10.5
V_{CC} = 5.00 V	460	16	12	5.00	0.1	465	17	12	4.75	0	8.5	10
V_{CC} = 5.25 V	455	17	12.5	5.25	0.1	465	17	13	5.25	0	8	9
T = 0°C												
V_{CC} = 4.75 V	460	14	10	4.75	0.1	465	15	10.5	4.75	0	11	12
V_{CC} = 5.00 V	460	15	10	5.00	0.1	465	15	10	5.00	0	10.5	11.5
V_{CC} = 5.25 V	460	15	10.5	5.25	0.1	465	15	10	5.25	0	10	10.5

*Resolution of this measurement ≈ ±50 mV

LEGEND:

PW: Pulse width measured at V_{CC} – 0.3 V
t_r: Rise time measured from 0.3 V to V_{CC} – 0.3 V
t_f: Fall time measured from V_{CC} – 0.3 V to 0.3 V
"0" LL: Zero logic level
"1" LL: One logic level
Non-Overlap: Measured from 0.5 volt levels

FIGURE 9 – MONOSTABLE CLOCK GENERATOR

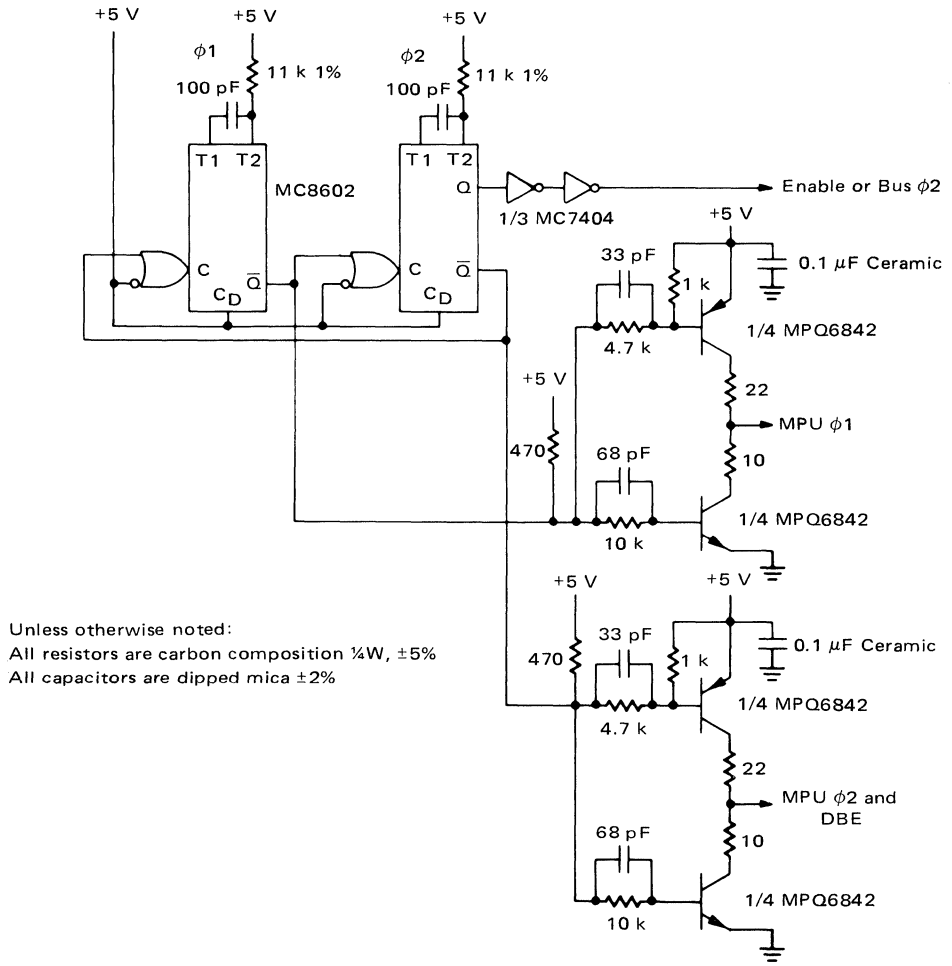


TABLE 2 – PERFORMANCE OF CIRCUIT OF FIGURE 9

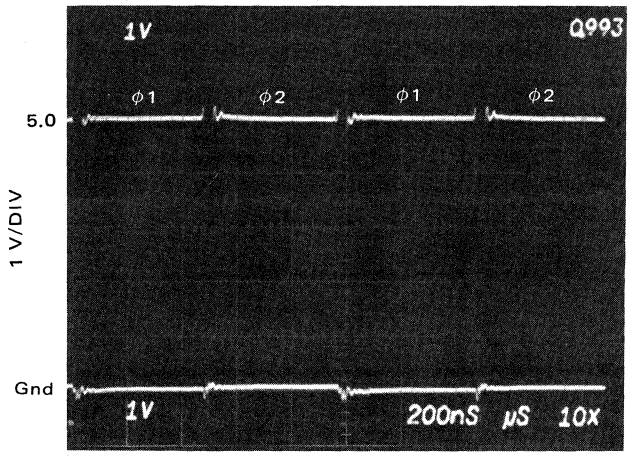
Test Conditions	MPU ϕ1					MPU ϕ2					Non-Overlap Region	
	PW	t_r	t_f	"1" LL*	"0" LL*	PW	t_r	t_f	"1" LL*	"0" LL*	ϕ1↓ to ϕ2↑	ϕ2↓ to ϕ1↑
T = 20°C												
V_{CC} = 4.75 V	470 ns	11 ns	11.5 ns	4.75 V	0.1 V	450 ns	12 ns	12 ns	4.75 V	0 V	12 ns	11 ns
V_{CC} = 5.00 V	470	12.5	13	5.00	0.1	460	13	12.5	5.00	0	11	9.5
V_{CC} = 5.25 V	470	13	12	5.25	0.1	460	13.5	12.5	5.25	0	10	9
T = 70°C												
V_{CC} = 4.75 V	455	12.5	13.5	4.75	0.1	450	13	13	4.75	0	11	10
V_{CC} = 5.00 V	455	13	14	5.00	0.1	450	14	14	5.00	0	10	9
V_{CC} = 5.25 V	455	13	14.5	5.25	0.1	450	14	14	5.25	0	8.5	7
T = 0°C												
V_{CC} = 4.75 V	473	12	12	4.75	0.1	470	12	12	4.75	0	11	11
V_{CC} = 5.00 V	475	12	12	5.00	0.1	470	12.5	12	5.00	0	9	11
V_{CC} = 5.25 V	475	12.5	12.5	5.25	0.05	473	12.5	12	5.25	0	9	8

*Resolution of this measurement ≈ ±50 mV

LEGEND: PW: Pulse width measured at V_{CC} – 0.3 V
t_r: Rise time measured from 0.3 V to V_{CC} – 0.3 V
t_f: Fall time measured from V_{CC} – 0.3 V to 0.3 V
"0" LL: Zero logic level
"1" LL: One logic level
Non-Overlap: Measured from 0.5 volt points

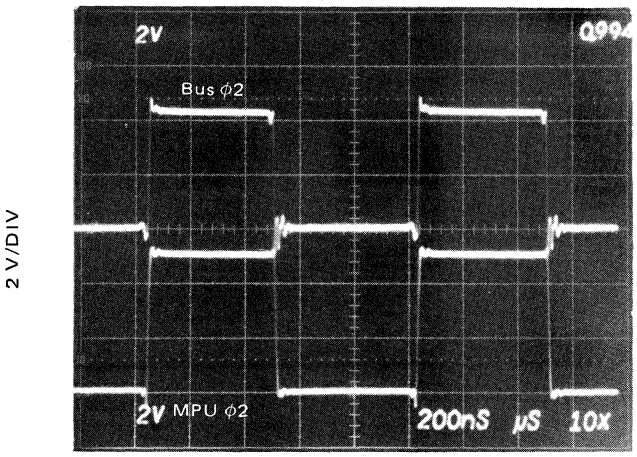
CLOCK CIRCUIT WAVEFORMS
(Using Circuit of Figure 9)

FIGURE 10a – MPU CLOCK



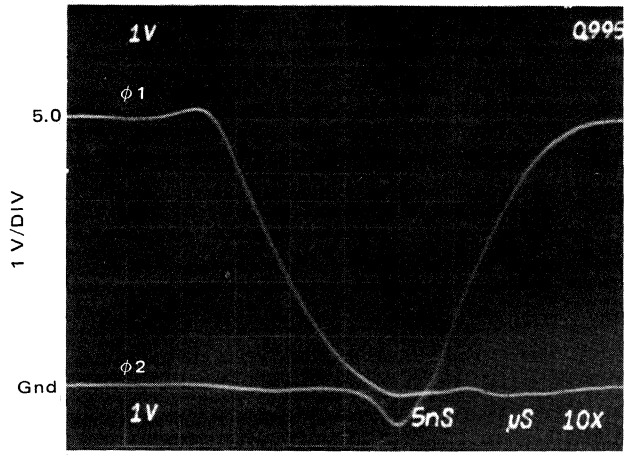
200 ns/DIV

FIGURE 10b – MPU $\phi 2$ CLOCK AND BUS $\phi 2$



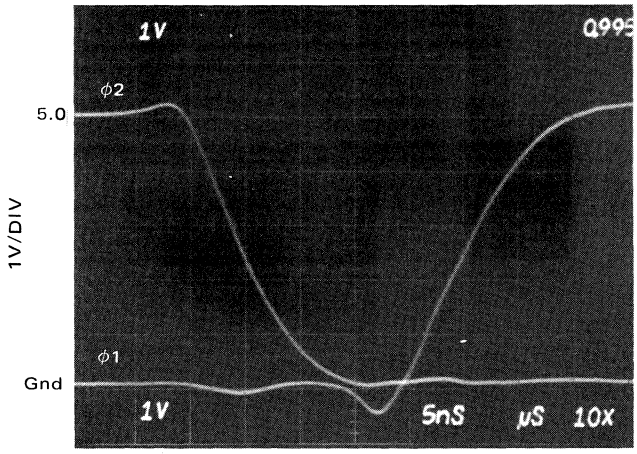
200 ns/DIV

FIGURE 10c – MPU CLOCK NON-OVERLAP REGION $\phi 1$ to $\phi 2$



5 ns/DIV

FIGURE 10d – MPU CLOCK NON-OVERLAP REGION $\phi 2$ to $\phi 1$



5 ns/DIV

CLOCK CIRCUITRY FOR SLOW AND DYNAMIC MEMORIES

The circuitry to modify the clock signals to interface the MC6800 with dynamic (e.g., MCM6605) and slow memories can be evolved from the clock circuitry described previously. Figure 11 expands the clock circuit of Figure 7 (which has a crystal stabilized source) to include interface signals for dynamic ($\overline{\text{Refresh Request}}$ and Refresh Grant) and slow memories (Memory Ready). Note that the only extra parts required are an MC7479 dual latch, an MC7404 hex inverter, and a pair of 10 k ohm pullup resistors. The state of $\overline{\text{Refresh Request}}$ is sampled during the leading edge of $\phi 1$ and, if it is low, the $\phi 1$ and $\phi 2$ clocks to the MPU are held in the high and low states respectively for at least one full clock cycle. A high Refresh Grant signal is issued to indicate to the dynamic memory system that this cycle is a refresh cycle. Upon receipt of the Refresh Grant signal, the memory system controller sets $\overline{\text{Refresh Request}}$ back high; this is clocked through on the next leading edge of $\phi 1$, thereby restoring the system to normal operation. The Memory Ready line is sampled on the leading edge of $\phi 2$ and, if low, the MPU $\phi 1$ and $\phi 2$ clocks are held in the low and high states, respectively. The clocks will be held in these states until the Memory Ready line is brought high by the slow memory controller, allowing the slow memory controller to determine the amount by which $\phi 2$ is stretched. Figures 12a and 12b show the effect of $\overline{\text{Refresh Request}}$ and Memory Ready signals on the MPU clocks. Note that the $\overline{\text{Refresh Request}}$ signal is asynchronous with the MPU clocks as it is generated by the refresh oscillator in the dynamic memory controller. Figures 13a and 13b show the phase relationship between MPU $\phi 2$, Bus $\phi 2$ and Dynamic Memory Clock. Note that Bus $\phi 2$ and MPU $\phi 2$ are in phase and that the Dynamic Memory Clock leads MPU $\phi 2$ to help offset delays added by the memory

system controller in decoding and level shifting this signal onto the memory array.

The circuit in Figure 14 shows how the Memory Ready capability can be added to the cross-coupled monostable clock generator of Figure 9. The Memory Ready feature is incorporated into this circuit by switching in or out of the $\phi 2$ pulse width generator an additional timing resistor. By selection of the timing resistors for $\phi 1$ and $\phi 2$, all combinations of $\phi 1$, $\phi 2$, and stretched $\phi 2$ pulse width can be generated.

FIGURE 11 – MPU CLOCK CIRCUITRY WITH INTERFACE FOR SLOW AND DYNAMIC MEMORY

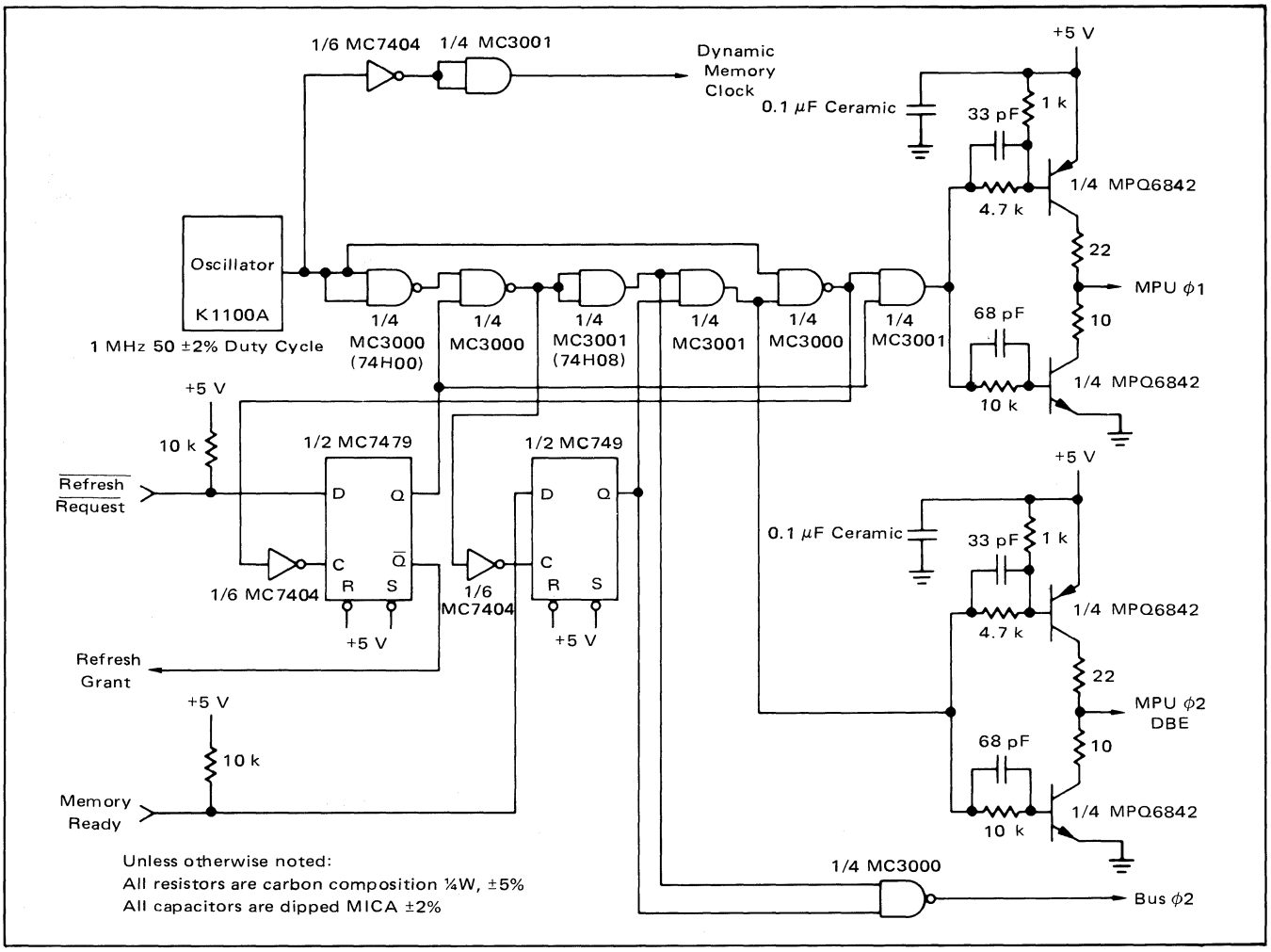
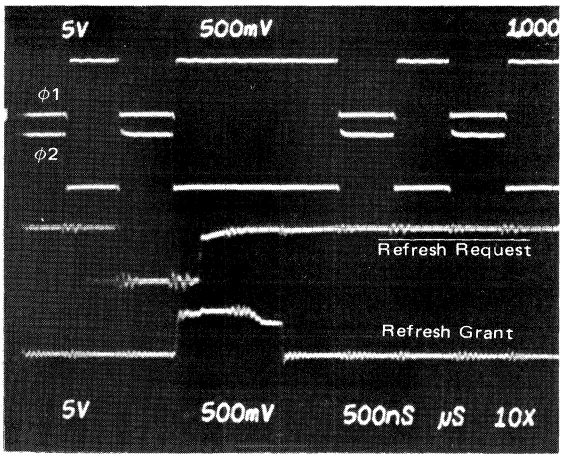


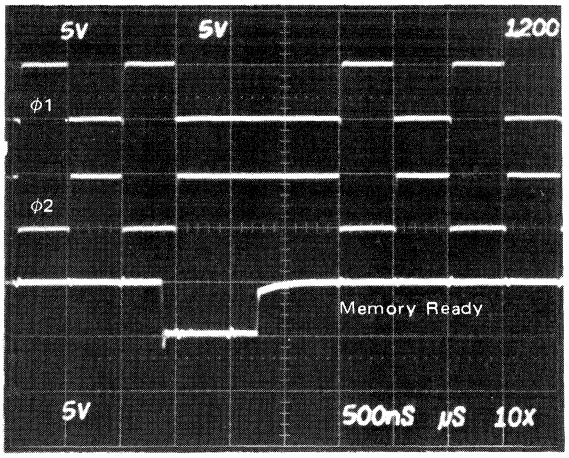
FIGURE 12a – MPU CLOCKS, $\overline{\text{REFRESH}}$ $\overline{\text{REQUEST}}$, AND REFRESH GRANT



5 V/DIV

500 ns/DIV

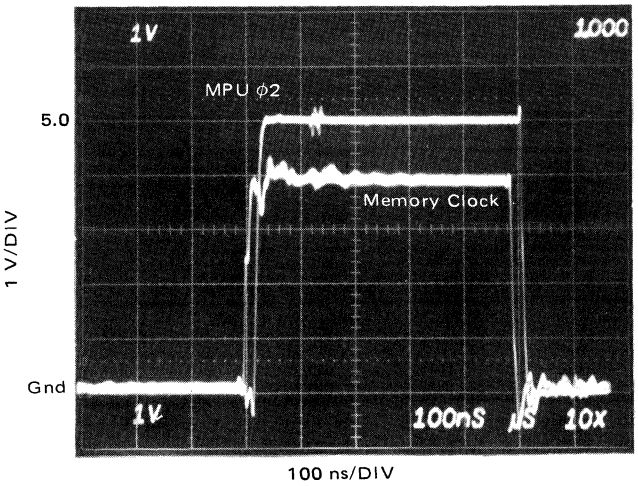
FIGURE 12b – MPU CLOCKS AND MEMORY READY



5 V/DIV

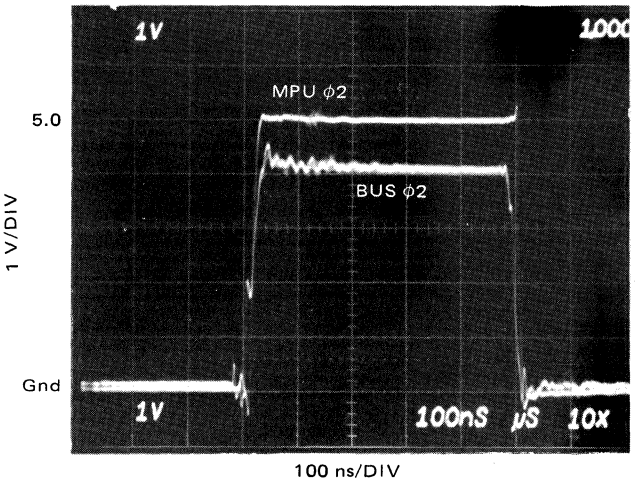
500 ns/DIV

FIGURE 13a – DYNAMIC MEMORY CLOCK AND MPU $\phi 2$



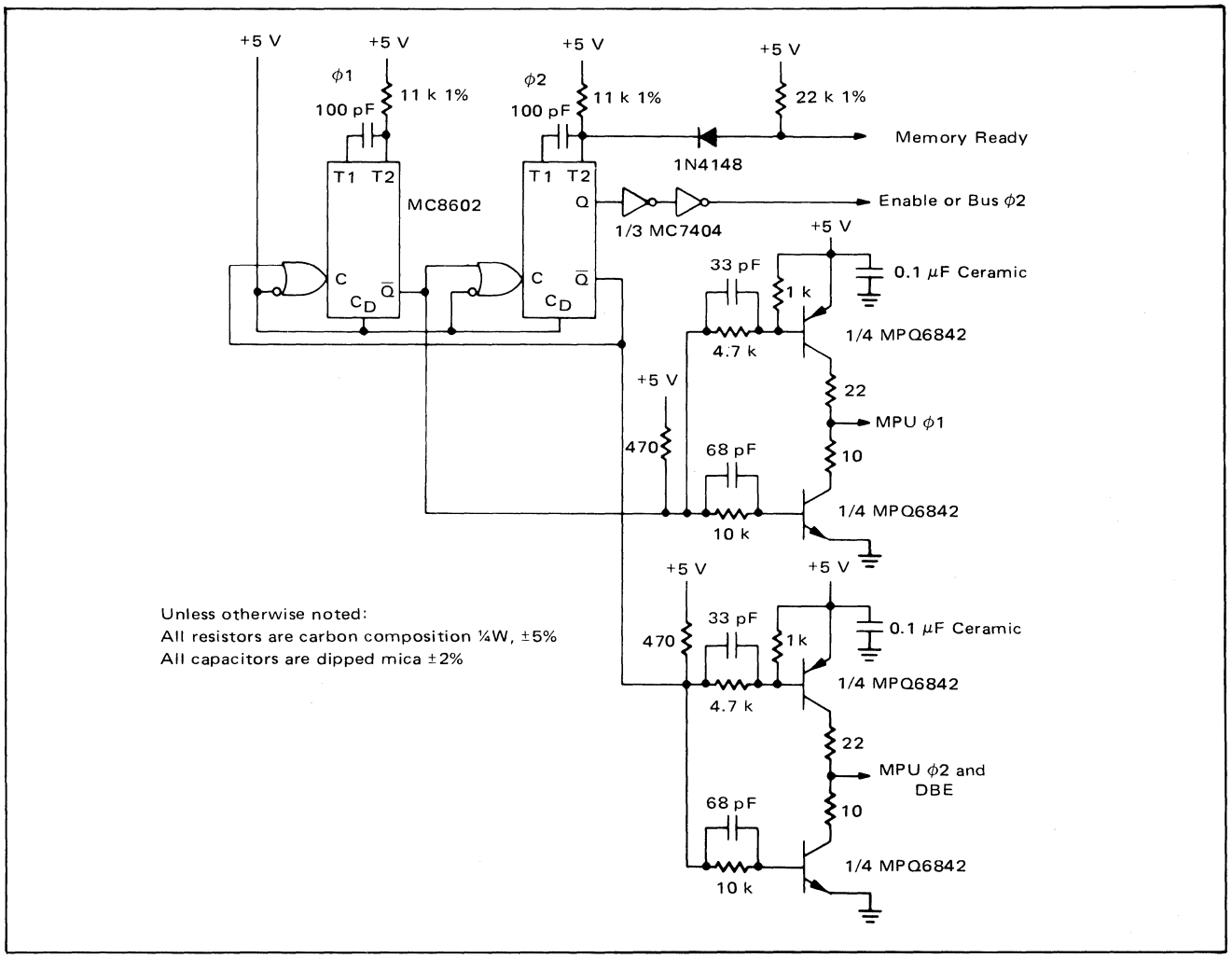
100 ns/DIV

FIGURE 13b – BUS $\phi 2$ AND MPU $\phi 2$



100 ns/DIV

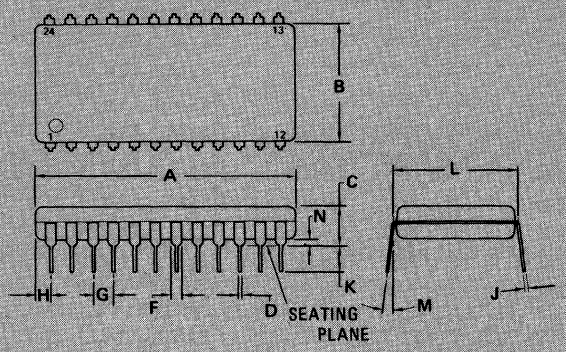
FIGURE 14 – MONOSTABLE CLOCK GENERATOR WITH MEMORY READY



Unless otherwise noted:
All resistors are carbon composition ¼W, ±5%
All capacitors are dipped mica ±2%

24 AND 40-LEAD
PLASTIC PACKAGE DIMENSIONS

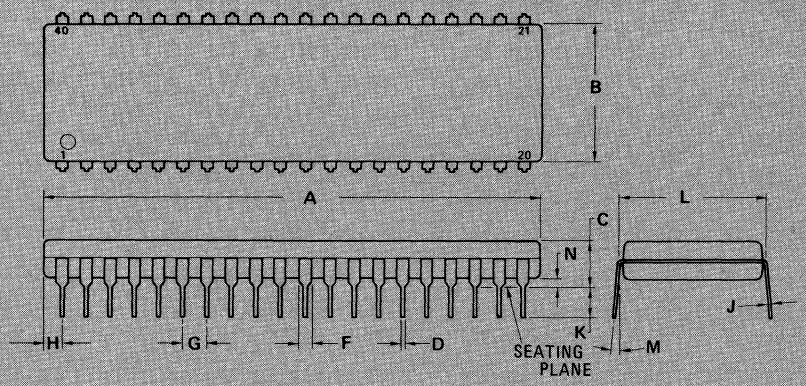
CASE 709-01



	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	31.37	32.13	1.235	1.265
B	13.72	14.22	0.540	0.560
C	4.57	5.08	0.180	0.200
D	0.36	0.51	0.014	0.020
F	1.02	1.52	0.040	0.060
G	2.41	2.67	0.095	0.105
H	1.78	2.03	0.070	0.080
J	0.20	0.30	0.008	0.012
K	3.05	3.56	0.120	0.140
L	14.73	15.24	0.580	0.600
M	0°	10°	0°	10°
N	0.51	1.02	0.020	0.040

NOTES:
1. LEADS, TRUE POSITIONED WITHIN 0.25 mm (0.010) DIA AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION. (DIM. "D")
2. DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.

CASE 711-01



	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	51.82	52.32	2.040	2.060
B	13.72	14.22	0.540	0.560
C	4.57	5.08	0.180	0.200
D	0.36	0.51	0.014	0.020
F	1.02	1.52	0.040	0.060
G	2.41	2.67	0.095	0.105
H	1.65	2.16	0.065	0.085
J	0.20	0.30	0.008	0.012
K	3.68	4.19	0.145	0.165
L	14.99	15.49	0.590	0.610
M	0°	10°	0°	10°
N	0.51	1.02	0.020	0.040

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