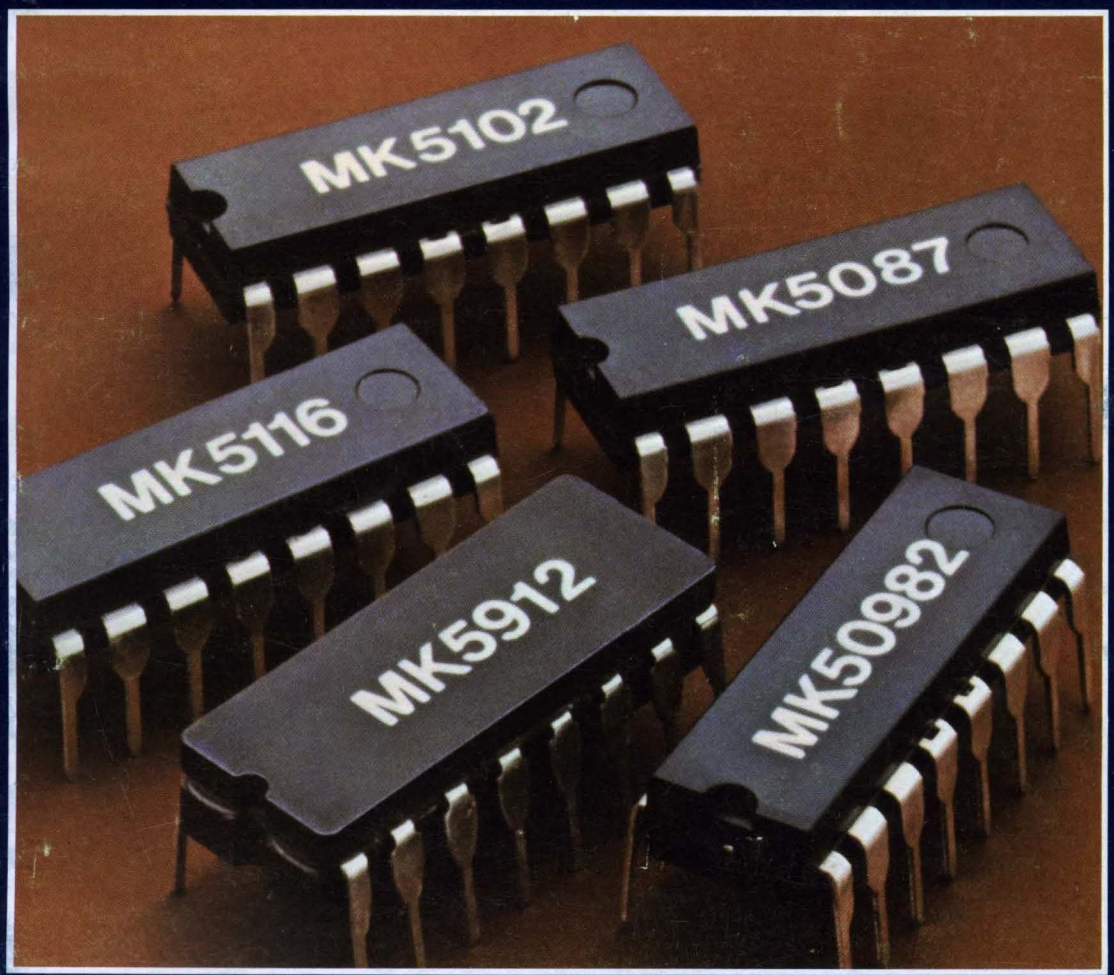
MOSTEK 1980

TELECOMMUNICATIONS DATA BOOK



MOSTEK 1980 TELECOMMUNICATIONS DATA BOOK

1980
Telecommunication Products
Data Book

PRINTED IN USA April 1980
STD No. 20004

1980 TELECOMMUNICATION PRODUCTS DATA BOOK

1980 TELECOMMUNICATION PRODUCTS DATA BOOK

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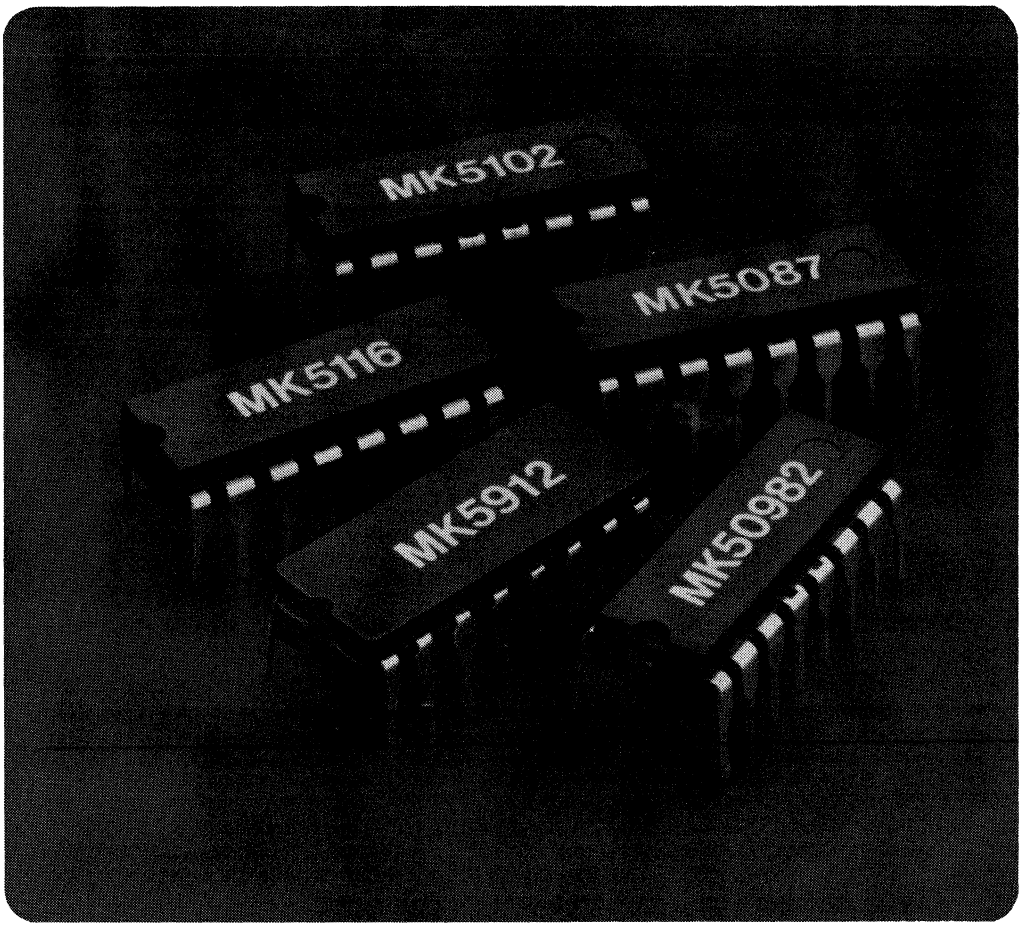


Telecommunications

Mostek has all the numbers for a totally digital system

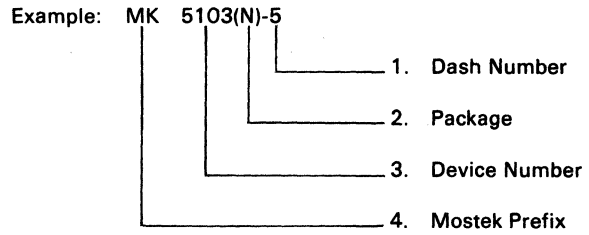
At Mostek you get a choice. Mostek is the only company with a broad line of telecommunications circuits aimed at cost-effective solutions for big systems or small. Tone dialers, pulse dialers, repertory dialers, tone decoders and codecs are available in volume now.

Mostek made its commitment to telecommunications products in 1974, the year we built our first tone dialer. Since then we've shipped over five million. So, we've earned our reputation as a dependable source for reliable products. Our extensive testing and quality control procedures all assure reliable systems in the field.

A good example of Mostek's technology leadership is the recently introduced switched capacitor PCM filter. In an application where space and power are the most critical parameters, Mostek's codec and filter offer industry's smallest packages and industry's lowest power.

ORDERING INFORMATION
TELECOMMUNICATION PRODUCTS

Factory orders for parts described in this book should include a four-part number as explained below:



1. Dash Number

   One or two numerical characters defining specific device performance characteristic.

2. Package

   P - Gold side-brazed ceramic DIP
   J - CER-DIP
   N - Epoxy DIP (Plastic)
   K - tin side-brazed ceramic DIP
   T - Ceramic DIP with transparent lid
   E - Ceramic leadless chip carrier

3. Device Number

   1XXX or 1XXXX - Shift Register, ROM
   2XXX or 2XXXX - ROM, EPROM
   3XXX or 3XXXX - ROM, EPROM
   38XX - Microcomputer Components
   4XXX or 4XXXX - RAM
   5XXX or 5XXXX - Counters, Telecommunication and Industrial
   7XXX or 7XXXX - Microcomputer Systems

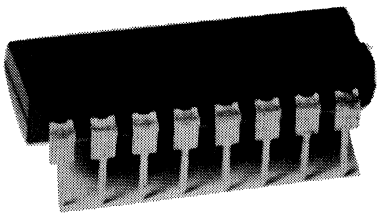
4. Mostek Prefix

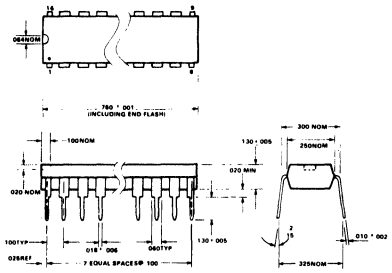
   MK-Standard Prefix

   MKB-100% 883B screening, with final electrical test at low, room and high-rated temperatures.

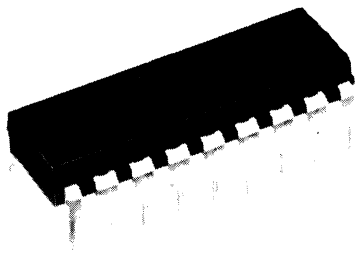
Package Descriptions

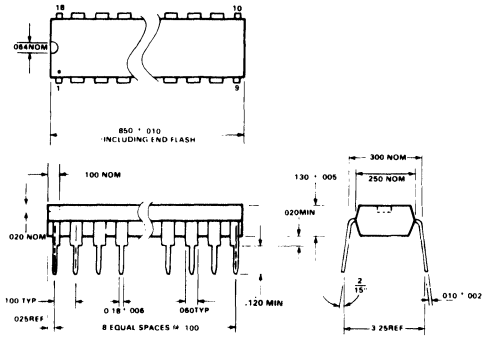
Plastic Dual-In-Line Package (N)
16 Pin



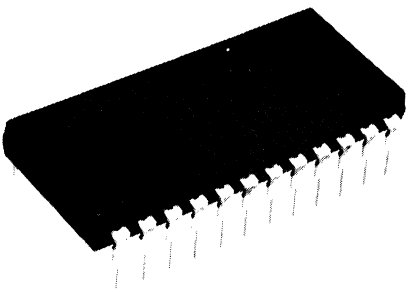


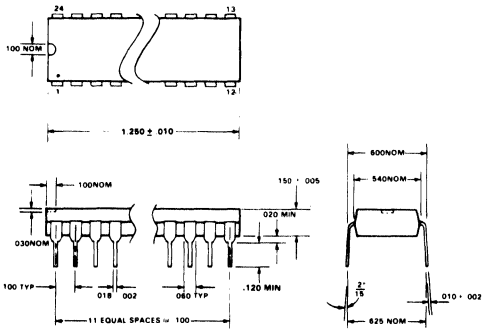
Plastic Dual-In-Line Package (N)
18 Pin



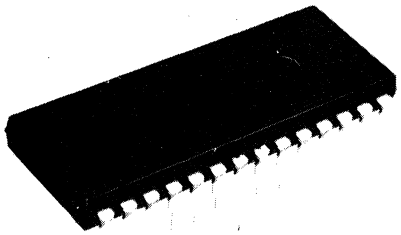


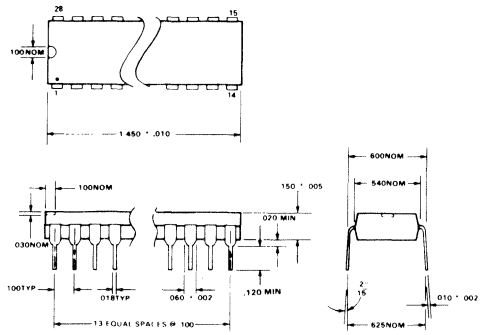
Plastic Dual-In-Line Package (N)
24 Pin



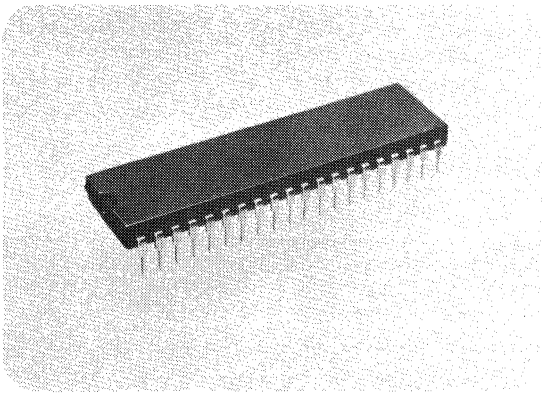


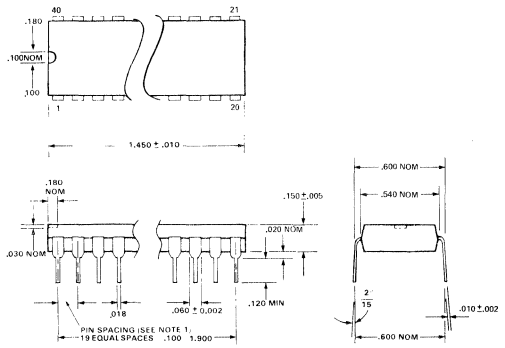
Plastic Dual-In-Line Package (N)
28 Pin





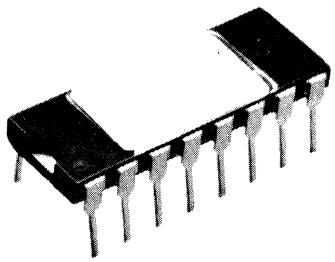
Plastic Dual-In-Line Package (N)
40 Pin

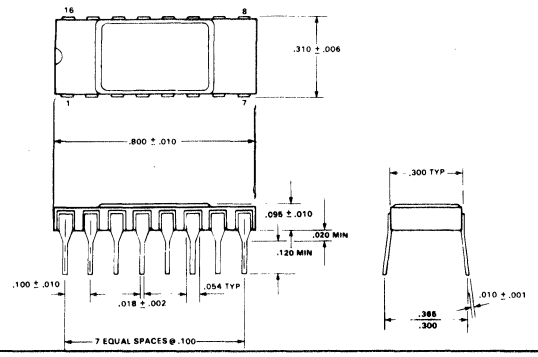




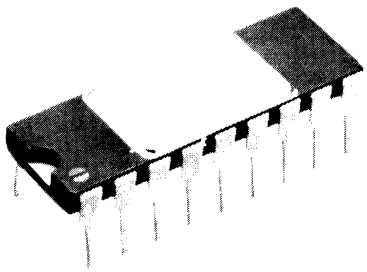
NOTES:
1. The true-position pin spacing is 0.100 between centerlines. Each pin centerline is located within ± 0.010 of its true longitudinal position relative to pins 1 and 40.

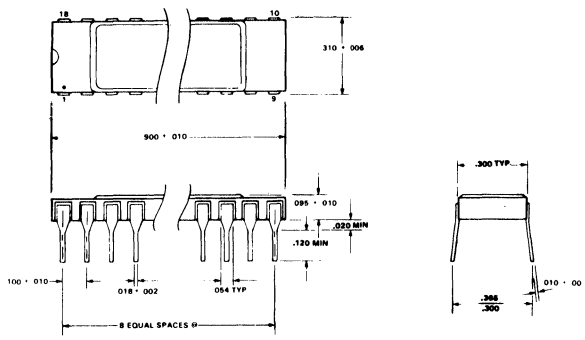
Ceramic Dual-In-Line Package (P)
16 Pin



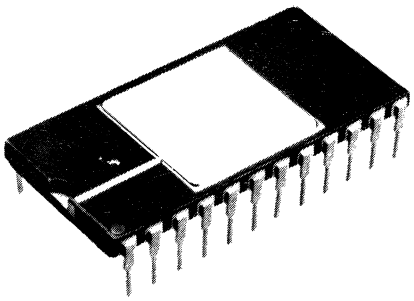


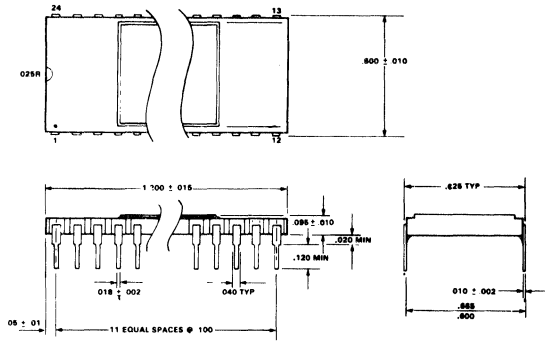
Ceramic Dual-In-Line Package (P)
18 Pin



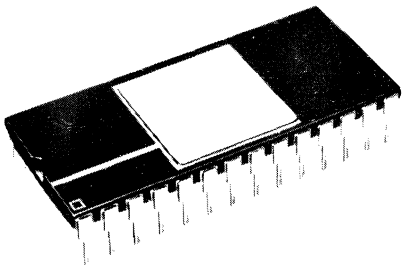


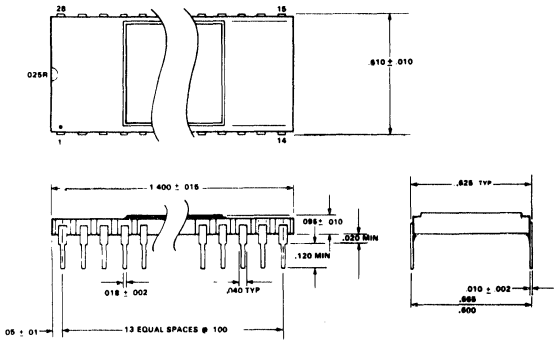
Ceramic Dual-In-Line Package (P)
24 Pin



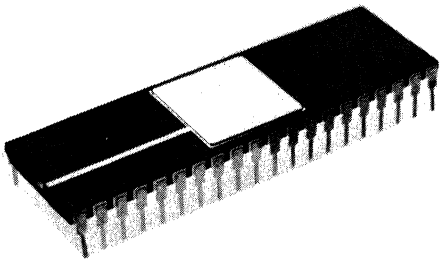


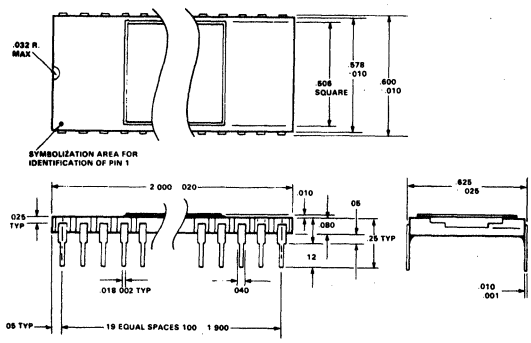
Ceramic Dual-In-Line Package (P)
28 Pin



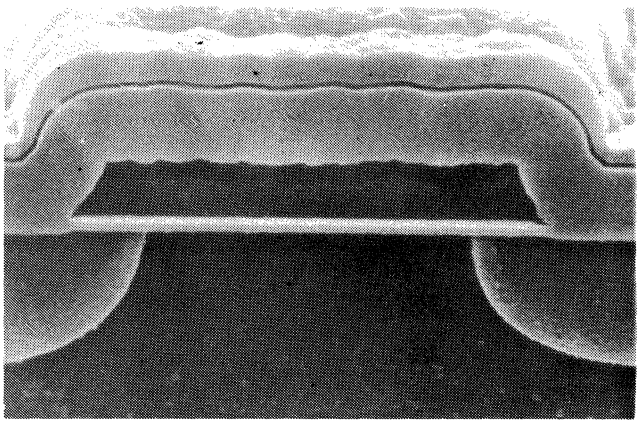


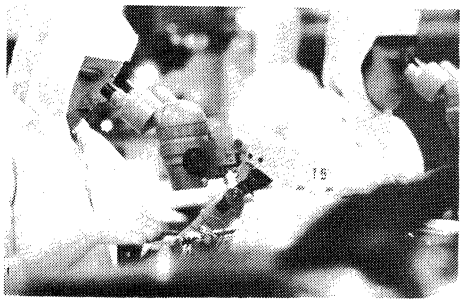
Ceramic Dual-In-Line Package (P)
40 Pin

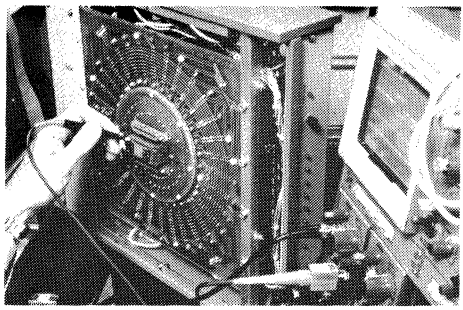




Mostek - Technology For Today And Tomorrow







TECHNOLOGY

From the beginning, Mostek has been recognized as an innovator. In 1970, Mostek developed the MK4006 1K dynamic RAM and the world's first single-chip calculator circuit, the MK6010. These technical breakthroughs proved the benefits of ion-implantation and cost-effectiveness of MOS. Now, Mostek represents one of the industry's most productive bases of MOS/LSI technology. Each innovation - in memories, microcomputers and telecommunications - adds to that technological capability.

QUALITY

The worth of a Mostek product is measured by its quality. How well it's designed, manufactured and tested. How well it works in your system.

In design, production and testing, our goal is meeting the spec every time. This goal requires a strict discipline, both from the company and from the individual. This discipline, coupled with a very personal pride, has driven Mostek to build in quality at every level, until every product we take to the market is as well-engineered as can be found in the industry.

PRODUCTION CAPABILITY

Mostek's commitment to increasing production capability has made us the world's largest manufacturer of dynamic RAMs. In 1979 we shipped 25 million 4K and 16K dynamic RAMs. We built our first telecommunication tone dialer in 1974; since then, we've shipped over 5 million telecom circuits. The MK3870 single-chip microprocessor is also a large volume product with over two million in application around the world. To meet the demand for our products, production capability must be constantly increased. To accomplish this, Mostek has been in a constant process of expanding and refining our production capabilities.

THE PRODUCTS

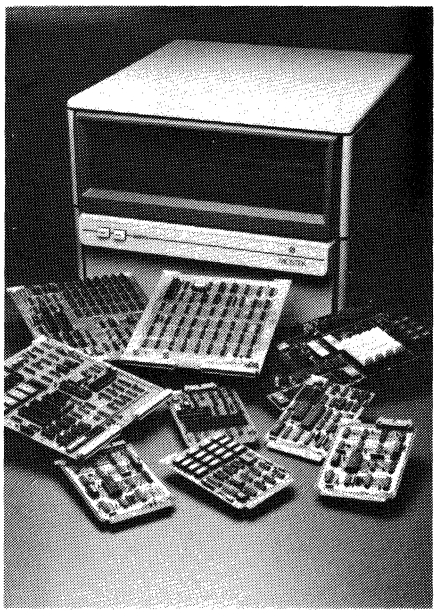
Telecommunications and Industrial Products

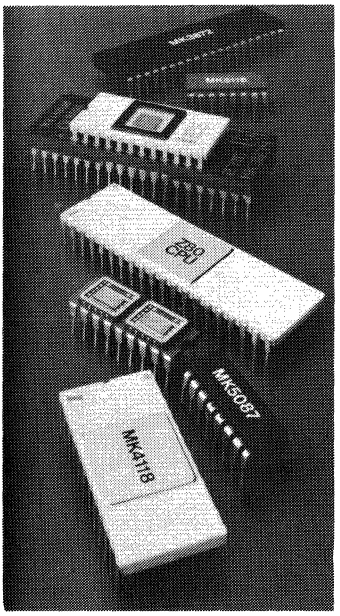
Mostek has made a solid commitment to telecommunications with a new generation of products, such as Integrated Pulse Dialers, Tone Dialers, CODECs, monolithic filters, tone receivers, A/D converters and counter time-base circuits.

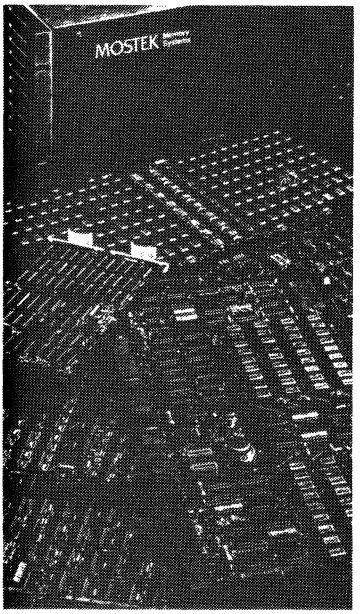
Since 1974 over five million telecom circuits have been shipped, making Mostek the leading supplier of tone/pulse dialers and CODECs.

Memory Products

Through innovations in both circuit







design, wafer processing and production, Mostek has become the industry's leading supplier of memory products.

An example of Mostek leadership is our new BYTEWYDE™ family of static RAMs, ROMs, and EPROMs. All provide high performance, N words x 8-bit organization and common pin configurations to allow easy system upgrades in density and performance. Another important product area is fast static RAMs. With major advances in technology, Mostek static RAMs now feature access times as low as 55 nanoseconds. With high density ROMs and PROMs, static RAMs, dynamic RAMs and pseudostatic RAMs, Mostek now offers one of industry's broadest and most versatile memory families.

Microcomputer Components

Mostek's microcomputer components are designed for a wide range of applications.

Our Z80 family is the highest performance 8-bit microcomputer available today. The MK3870 family is one of the industry's most popular 8-bit single-chip microcomputers, offering upgrade options in ROM, RAM, and I/O, all in the same socket. The MK3874 EPROM version supports and prototypes the entire family.

Microcomputer Systems

Supporting the entire component product line is the powerful MATRIX™ microcomputer development system, a Z80-based, dual floppy-disk system that is used to develop and debug software and hardware for all Mostek microcomputers.

A software operating system, FLP-80DOS, speeds and eases the design cycle with powerful commands. BASIC, FORTRAN, and PASCAL are also available for use on the MATRIX.

Mostek's MD Series™ features both stand-alone microcomputer boards and expandable microcomputer boards. The expandable boards are modularized by function, reducing system cost because the designer buys only the specific functional modules his system requires. All MDX boards are STD-Z80 BUS compatible.

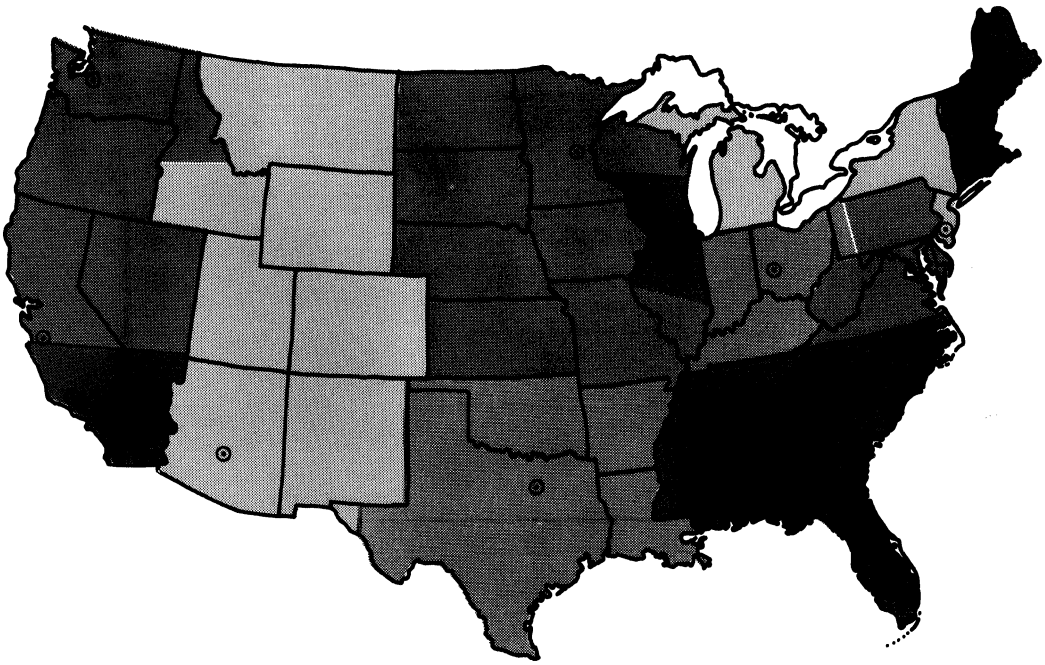
The STD-Z80 BUS is a multi-sourced motherboard interconnect system designed to handle any MDX card in any card slot.

Memory Systems

Taking full advantage of our leadership in memory components technology, Mostek Memory Systems offers a broad line of products, all with the performance and reliability to match our industry-standard circuits. Mostek Memory Systems offers add-in memory boards for popular DEC and Data General minicomputers.

Mostek also offers special purpose and custom memory boards for special applications.

U.S. AND CANADIAN SALES OFFICES



CORPORATE HEADQUARTERS

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TWX 910-950-1283

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TWX 910-749-6404

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TWX 710-332-0435

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TWX 910-563-3737

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314/394-7271

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215/627-0149 (Philadelphia Line)
TWX 710-896-0881

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Precision Sales Corp.*
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TWX 710-545-0250

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7221 Taylorsville Road
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TWX 810-427-9210

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TELEX 36-0465 (AMAPORT PTL)

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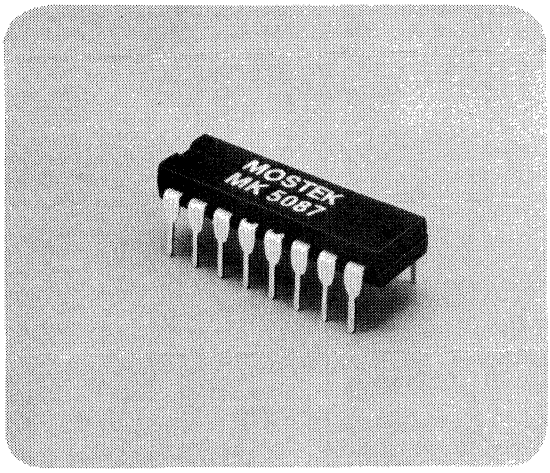
INTEGRATED TONE DIALER

MK5087(N)

FEATURES

- ☐ Pin-for-Pin compatible with MK5085N with improved performance
- ☐ Low Standby Power
- ☐ Auxiliary Switching Functions on Chip
- ☐ Minimum External Parts Count
- ☐ Uses Inexpensive 3.579545 MHz Television Color-Burst Crystal to Provide High Accuracy Tones
- ☐ On-Chip-Regulation of Dual and Single Tone Amplitudes
- ☐ Interfaces Easily in Electronic or μP Dialing Applications
- ☐ Multiple Key Entry Pin Selectable to Either Single Tone or No Tone



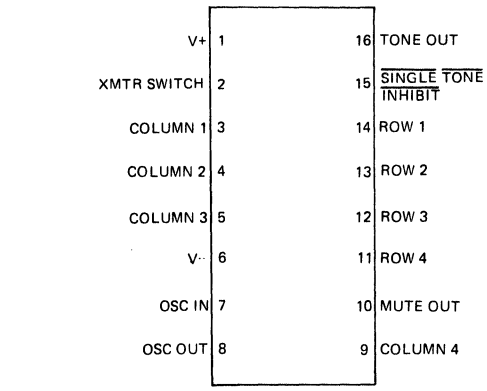
DESCRIPTION

The MK 5087 is a monolithic integrated circuit fabricated using the complementary-symmetry MOS (CMOS) process. A member of the TONE II* family of integrated tone-dialers, the MK5087 uses an inexpensive crystal reference to provide eight different audio sinusoidal frequencies, which are mixed to provide tones suitable for Dual-Tone-Multi-Frequency(DTMF) telephone dialing.

The MK 5087 was designed specifically for integrated tone-dialer applications that require the following: wide-supply operation with regulated output, opposite-polarity logic outputs,(one with push-pull output and one with open emitter output), single contact static keyboard inputs, and $\overline{\text{single}}$ $\overline{\text{tone}}$ $\overline{\text{inhibit}}$ option.

Keyboard entries to the TONE II* family of integrated tone-dialers cause the selection of the proper divide ratio to obtain the required two audio frequencies from the 3.579545 MHz reference oscillator. D-to-A conversion is accomplished on-chip by a conventional R-2R ladder network. The tone output is a stairstep approximation to a sine wave and requires little or no filtering for low-distortion applications. The same operational amplifier that accomplishes the current-to-voltage transformation necessary for the D-to-A converter also mixes the low and high-group signals. Frequency stability of this type of tone generator is such that no frequency adjustment is needed to meet standard DTMF specifications.

PIN OUT



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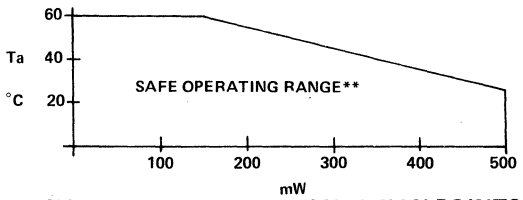
*ABSOLUTE MAXIMUM RATINGS

Supply Voltage V+	+10.5 Volts
Voltage on any pin relative to V-	-0.3 Volts
Voltage on any pin relative to V+	+0.3 Volts
Operating temperature, T_A (ambient)	-30°C to +60°C
Storage Temperature (ambient)	-55°C to +150°C
Maximum Circuit Power Dissipation	500mW @25°C. See Derating Curve



SUM OF ALL POWER DISSIPATION POINTS.

*Operation Above Absolute Maximum Ratings May Damage the Device
**Derating Curve Is Based On Device Operation Soldered Into Printed Circuit Board
DC Operating Conditions; $-30°C < T_A < +60°C$

Parameter	Symbol	Min.	Typ.	Max.	Units	Notes
Supply Voltage	V+	3.5		10.0	Volts	1
Inputs:						
$\overline{\text{Single}}$ $\overline{\text{Tone}}$ $\overline{\text{Inhibit}}$						
Input High (Logic 1)	VIH	.7V+		V+	Volts	1
Input Low (Logic 0)	VIL	0.0		.3V+	Volts	1
Columns (1-4)						
Input High (Column On)		.7V+		V+	Volts	1
Input Low (Column Off)		0.0		.1V+	Volts	1
Rows (1-4)						
Input High (Row Off)		.9V+		V+	Volts	1
Input Low (Row On)		0.0		.3V+	Volts	1

Electrical Characteristics $-30°C < T_A < +60°C; 3.5V \leq V+ \leq 10.0V$

Parameter	Symbol	Min	Typ	Max	Units	Notes
Output Voltage						
Row Tone (R_L = 1k)		317	400	504	mVRMS	1,3,6
Column Tone (R_L = 1k)		396	500	630	mVRMS	1,3,6
Tone Output External Load Impedance						
V+=3.5Vdc	R_L	620			Ω	
V+=10.0Vdc	R_L	330			Ω	

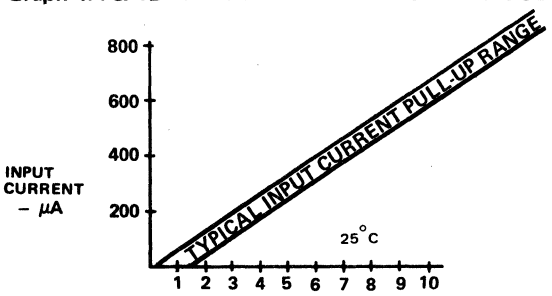
Electrical Characteristics (Cont.)

Parameter	Symbol	Min	Typ	Max	Units	Notes
Output Current Drive						
XMTR Switch (No Keyboard Entry)						
(V+=3.5, V_{OHX}=2.5V)	I_{OHX}	-15	-25		mA	
(V+=10.0V, V_{OHX}=8.0V)	I_{OHX}	-50	-100		mA	
XMTR Switch (Keyboard Entry)						
(V+=10.0V, Output=0.0V)	I_{XLEAK}		.1	10.0	μA	
Mute Out (No Keyboard Entry)						
(V+=3.5V, V_{OL}=0.5V)	I_{OL}	0.5	2.0		mA	
(V+=10.0V, V_{OL}=0.5V)	I_{OL}	1.0	4.0		mA	
Mute Out (Keyboard Entry)						
(V+=3.5V, V_{OH}=3.0V)	I_{OH}	0.5	2.0		mA	
(V+=10.0V, V_{OH}=9.5V)	I_{OH}	1.0	4.0		mA	
Standby Current (No Keyboard Entry)						
(Pin 6, V+=3.5V)	I_{STBY}		.25	100	μA	2,7
(Pin 6, V+=10.0V)	I_{STBY}		.5	200	μA	2,7
Operating Current (Keyboard Entry)						
(Pin 6, V+=3.5V)	I_{OP}		1.0	2.0	mA	2,6,8,9
(Pin 6, V+=10.V)	I_{OP}		5.0	10.0	mA	2,6,8,9
Input Current Rows and Columns - SEE GRAPH 1						
Input Resistance						
Single Tone Inhibit	R_{IN}	20		100	kΩ	
Tone Output (No Keyboard Entry)				-80	dBm	
Tone Output Rise Time t_{RISE}	t_r		3	5.0	mscs	5,9
Pre-Emphasis		1.0	2.0	3.0	dB	
Output Distortion, measured in terms of Total Out-Of-Band power Relative to Sum of Row & Column Fundamental Power				–20	dB	4

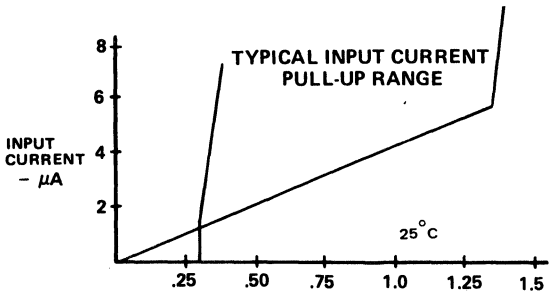
NOTES:

1. All voltages referenced to V–
2. All outputs unloaded
3. T_A = 25°C
4. Any row plus any column at V+$\geq$ 4 volts
5. Time from a valid keystroke with no bounce to allow wave to go from minimum to 90% of the final magnitude of either frequency.
6. True RMS Readings
7. Current Out Of Pin 6 No Key Depressed
8. Current Out Of Pin 6 One Key Depressed
9. Crystal parameters defined as $R_S \leq 100\Omega$ L_m =96mH, C_m =0.02pF, and C_h =5pF, F = 3.579545MHz, C_L = 18pF

Graph 1A & 1B - INPUT CURRENT VS. INPUT VOLTAGE



Graph 1A



Graph 1B

OSCILLATOR

The network contains an on-board inverter with sufficient loop-gain to provide oscillation when working with a low cost television color-burst crystal. The inverter's input is OSC IN (pin 7) and output is OSC OUT (pin 8). The circuit is designed to work with a crystal cut to 3.579545 megahertz to give the frequencies in Table 1.

Any crystal frequency deviation from 3.579545 MHz will be reflected in the tone output frequency. Most crystals don't vary more than ± .02%.

OUTPUT FREQUENCY DEVIATION
TABLE 1

		Standard DTMF (Hz)	Tone Output Frequency Using 3.579545 MHz Crystal	% Deviation From Standard	
ROW	f_1	697	701.3	+0.62	
	f_2	770	771.4	+0.19	LOW GROUP
	f_3	852	857.2	+0.61	
	f_4	941	935.1	-0.63	
COL	f_5	1209	1215.9	+0.57	
	f_6	1336	1331.7	-0.32	HIGH GROUP
	f_7	1477	1471.9	-0.35	
	f_8	1633	1645.0	+0.73	

ROW AND COLUMN INPUTS

The MK 5087N features inputs compatible with the standard 2-of-8 keyboard, the inexpensive single-contact (form A) keyboard, and electronic input. Figure 1 shows how to connect to the two keyboard types and Figure 2 shows waveforms for electronic input. The inputs are static, i.e. there is no noise generation as occurs with scanned or dynamic inputs.

The internal structure of the MK 5087N inputs is shown in Figure 3. R_{RI} and R_{CI} pull in opposite directions and hold their associated input sensing circuit turned off. When one or more row or column inputs are tied together, however, the input sensing circuits sense the "½ Level" and deliver a logic signal to the internal circuitry of the MK 5087N and cause the proper tone or tones to be generated.

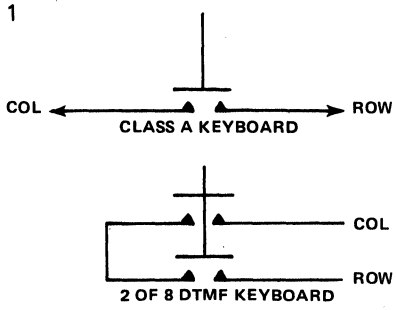
When operating with a keyboard, normal operation is for dual-tone generation when any single button is pushed, and single-tone operation when one or more buttons in the same row or column is pushed. Activation of diagonal buttons will result in no tones being generated.

When the inputs to the MK 5087N are electronically activated, per Figure 2, input to a single row and column will result in that dual tone digit's being generated. Input to a single column will result in that column tone being generated. Input to multiple columns will result in no tone being generated.

Activation of a single row is not sensed by the internal circuitry of the MK 5087N. If a single row tone is desired, two columns must be activated along with the desired row.

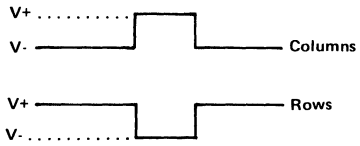
KEYBOARD CONFIGURATION

Figure 1



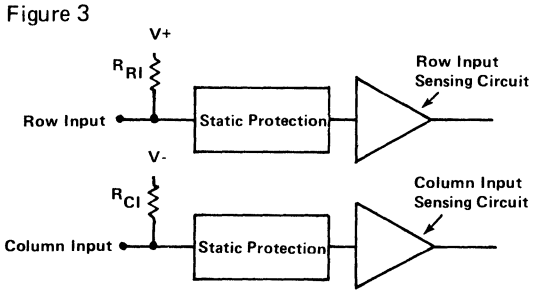
ELECTRONIC INPUT

Figure 2

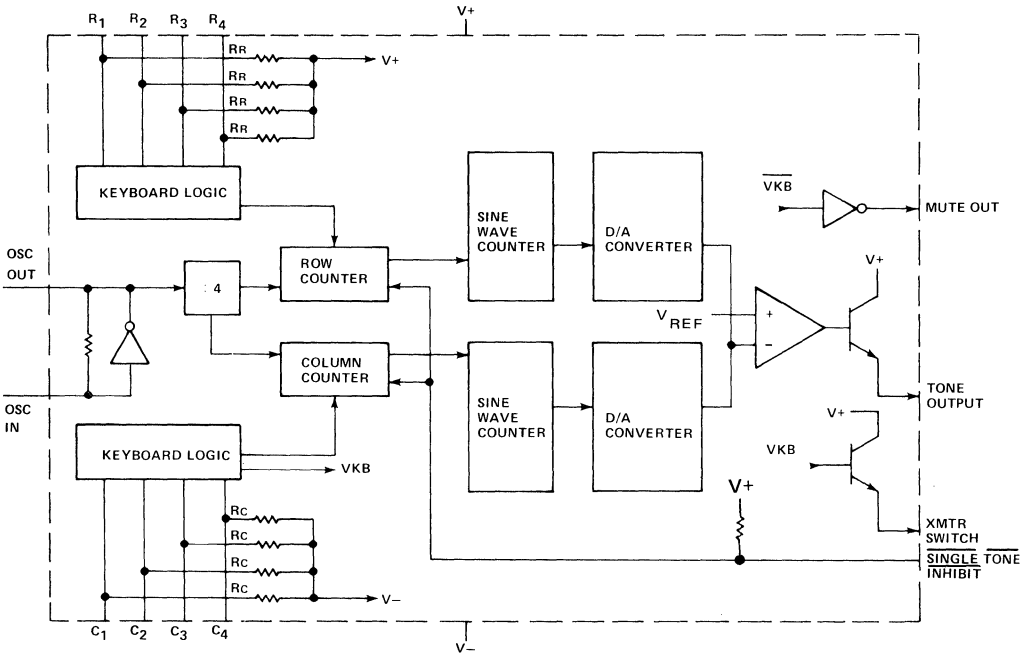


ROW AND COLUMN INPUTS

Figure 3



MK 5087 BLOCK DIAGRAM



SINGLE TONE INHIBIT (PIN 15)

The Single Tone Inhibit input is used to inhibit the generation of other than dual tones. It has a pull up to the V+ supply and, when left floating or tied to V+, single or dual-tones may be generated as described in the paragraph under row-column inputs. When forced to the V- supply, any input situation that would normally result in a single-tone will now result in no tone, with all other chip functions operating normally.

XMTR SWITCH (PIN 2)

This pin is connected to the emitter of an on-chip bipolar transistor whose collector is connected to V+. With no keyboard input, this transistor is turned on and pulls pin 2 up to the V+ supply. When a key-board entry is sensed, this output goes open-circuit (high impedance). The XMTR switch output switches regardless of the state of the single tone inhibit input.

TONE OUTPUT (PIN 16)

The tone output pin is connected internally in the MK 5087N to the emitter of an NPN transistor whose collector is tied to V+. The input to this transistor is the on-chip operational amplifier which mixes the row and column tones together and provides output level regulation.

MUTE OUT (PIN 10)

The mute output is a conventional CMOS gate that pulls to V- with no keyboard input and pulls to the V+ supply when a keyboard entry is sensed. This output is used to control auxiliary switching functions that are required to actuate upon keyboard input. The mute output switches regardless of the state of the single tone inhibit input.

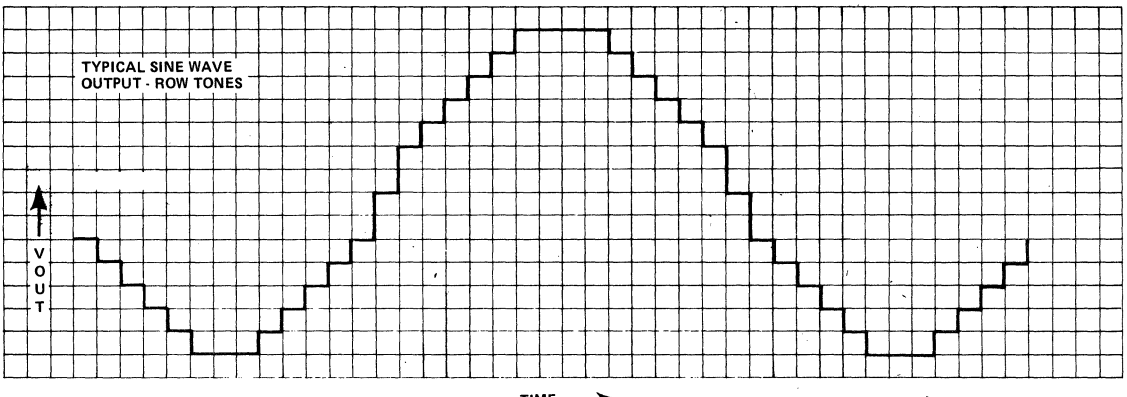


Figure 4

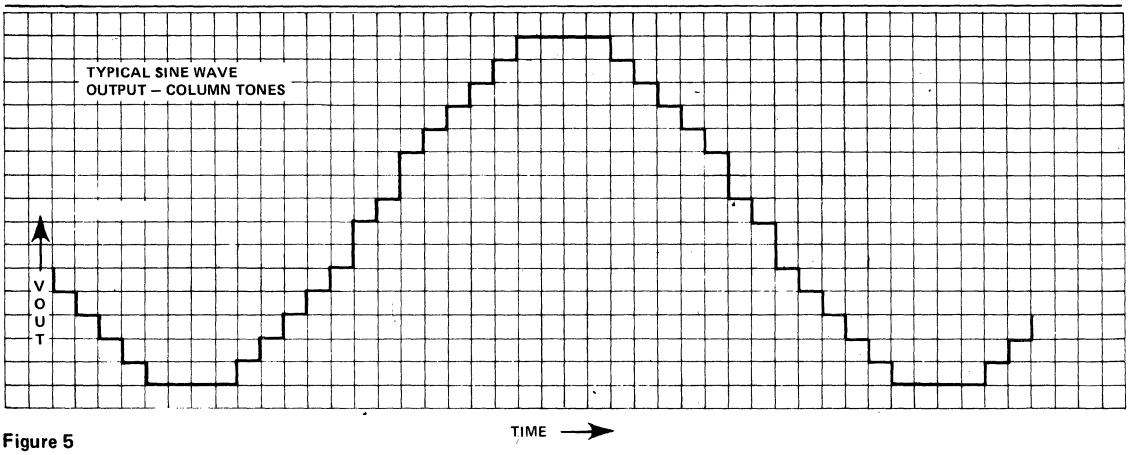


Figure 5

OUTPUT WAVEFORM

The row and column output waveforms are shown in figures 4 and 5. These waveforms are digitally-synthesized using on-chip D-to-A converters. Distortion measurement of these unfiltered waveforms will show a typical distortion of 7% or less.

The on-chip operational amplifier of the MK 5087 mixes the row and column tones to result in a dual-tone waveform. Spectral analysis of this waveform will show that typically all harmonic and inter-modulation distortion components will be -30 dB down when referenced to the strongest fundamental (column tone).

Figures 6 and 7 show a typical dual tone waveform and its spectral analysis.

DISTORTION MEASUREMENTS

Total Harmonic Distortion for the single tone case (i.e. a single row or column) is defined by the classical equation:

$$THD = \left(\frac{\sqrt{v_{2f}^2 + v_{3f}^2 + v_{4f}^2 + \ldots v_{nf}^2}}{v_{fundamental}} \right) \times 100\%$$

Where v_{2f} . . . v_{nf} are various Fourier components of the waveform being measured.

Total Harmonic Distortion for the dual tone case is defined by:

$$THD = \left(\frac{\sqrt{v_{2r}^2 + v_{3r}^2 + \ldots v_{nr}^2 + v_{2c}^2 + v_{3c}^2 + \ldots v_{nc}^2 + v_{IMD}^2}}{\sqrt{v_{row}^2 + v_{col}^2}} \right) \times 100$$

Where v_{row} is the row fundamental amplitude, v_{col} is the column fundamental amplitude, v_{2r}. . .V_{nr} are the amplitudes of all the Fourier components of the column frequencies, and v_{IMD}^2 is the sum of all the intermodulation components represented by $(V_r + c)^2 + (V_r - c)^2 + (V_{2r} + c)^2 + (V_r - 2c)^2 + (V_{2r} - c)^2 + (V_{2r} - zc)^2 + \ldots (V_{nr} + mc)^2 + (V_{nr} - mc)^2$

A commonly-quoted method of dual tone distortion measurement is the comparison of total power in the unwanted components (i.e. intermodulation and harmonic components) with the total power in the two fundamentals. For the MK 5087 dual tone waveform, THD is –20dB maximum.

A simpler measurement may be made directly from the screen of a spectrum analyzer by relating any component to one of the fundamentals. The MK 5087 dual tone spectrum will show all individual harmonic and IMD components are typically at least 30dB down with respect to the column tone.

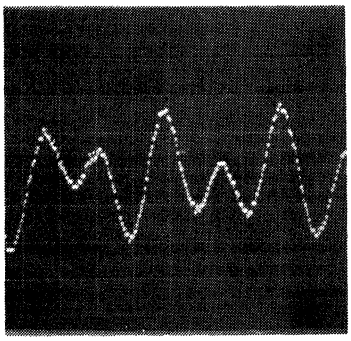


Figure 6 - TYPICAL DUAL TONE WAVEFORM (ROW 1, COL.1)

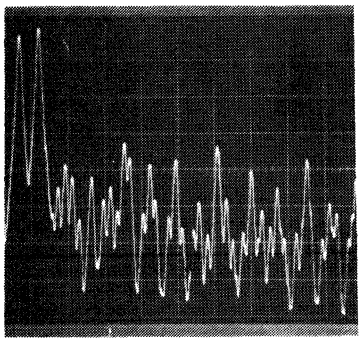


Figure 7 - SPECTRAL ANALYSIS OF WAVEFORM IN FIG. 6 (Vert-10 dB/Div, Horizontal-1 KHz/Div)

DTMF TONE GENERATOR - Fixed Supply Operation

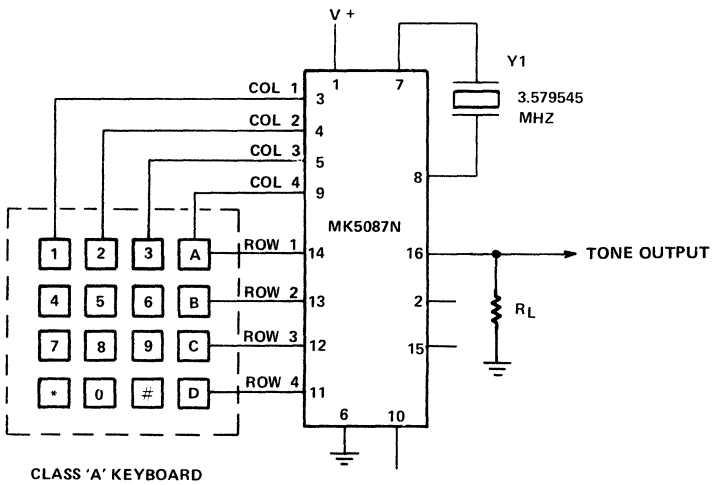


Figure 8

APPLICATION

The MK 5087 may be used for almost any application where generation of the standard DTMF frequencies is required.

Figure 8 shows the minimum parts count application for fixed supply operation.

PRELIMINARY

MOSTEK®

INTEGRATED TONE DIALER

MK 5089 N

FEATURES

- ☐ Minimum external parts count
- ☐ High-accuracy tones
- ☐ Digital divider logic, resistive ladder network and CMOS operational amplifier on single chip
- ☐ Uses inexpensive 3.579545 MHz television color-burst crystal
- ☐ Invalid key entry can result in either single tone or no tone
- ☐ · $\overline{\text{Chip}}$ $\overline{\text{Disable}}$ allows any key down output to function from keyboard input without generating tones

DESCRIPTION

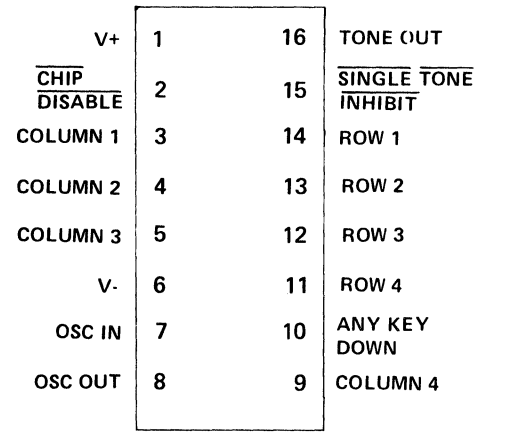
The MK 5089 is a monolithic integrated circuit fabricated using the complementary-symmetry MOS (CMOS) process. A member of the TONE II* family of integrated tone dialers, the MK 5089 uses an inexpensive crystal reference to provide eight different audio sinusoidal frequencies, which are mixed to provide tones suitable for Dual-Tone Multi-Frequency (DTMF) telephone dialing.

The MK 5089 was designed specifically for integrated tone-dialer applications that require the following: fixed supply operation, negative-true keyboard-input, chip disable input, stable-output tone level, and an Any Key Down output that is open circuit when no keyboard buttons are pushed and pulls to the V- supply when a button is pushed.

* Trademark of Mostek Corporation

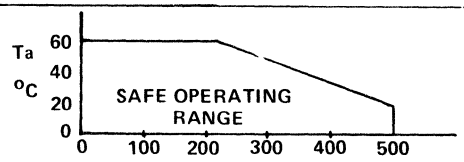
Keyboard entries to the TONE II* family of integrated tone dialers cause the selection of the proper divide ratio to obtain the required two audio frequencies from the 3.579545 MHz reference oscillator. D-to-A conversion is accomplished on-chip by a conventional R-2R ladder network. The tone output is a stairstep approximation to a sine wave and requires little filtering for low-distortion applications. The same operational amplifier that accomplishes the current-to-voltage transformation necessary for the D-to-A converter also mixes the low and high group signals. Frequency-stability of this type of tone generation is such that no frequency adjustment is needed to meet standard DTMF specifications.

PIN OUT



*ABSOLUTE MAXIMUM RATINGS

DC Supply Voltage V+	10.5 Volts
Any Input Relative to V+ (except Pin 10)	+0.30 Volts
Any Input Relative to V- (except Pin 10)	-0.30 Volts
Operating Temperature	-30°C to +60°C
Storage Temperature	-55°C to 150°C
Maximum Circuit Power Dissipation	500 mW See derating curve.



SUM OF ALL POWER DISIPATION POINTS.

*OPERATION ABOVE ABSOLUTE MAXIMUM RATINGS MAY DAMAGE THE DEVICE.

Operating Characteristics . . . . . -30°C≤ T_A ≤60°C

PARAMETER	SYM	MIN	TYP	MAX	UNITS
Supply Voltage	V+	3.0		10.0	Volts
Input "0"		V-		.3V+	Volts
Input "1"		.7V+		V+	Volts
Input Pull-Up Resistor	R_1	20		100	K OHM
$\overline{\text{Chip Disable}}$	$\overline{CD}$	V-		.3V+	Volts See Note 4
Tone Output (R_{LOAD}=100KΩ)	V_{out}	-10.0		-7.0	dBm See Note 1
Pre Emphasis, High Band		2.4	2.7	3	dB
Output distortion, measured in terms of total out-of-band power relative to RMS sum of Row and column fundamental power.				-20	dB See Note 2
Rise Time	T_{rise}		2.8	5.0	ms See Note 3
Any Key Down Sink Current to V-	I_{AKD}	500			μA@.5V
AKD Off Leakage	I_{AKDO}			2	μA @ 5V
Supply Current Operating	I_{SO}			2.0	mA@3.5V;See Note 6
Supply Current Standby	I_{SST}			200	μA@10.0V;See Note5
Tone Output - No Key Down	NKD			-80	dBm

NOTE 1: Single-tone, low-group. Any V+ = between 3.4 and 3.6 V - OdBm = .775V

NOTE 2: Any dual-tone. Any V+ = between 3.4 to 10.0V.

NOTE 3: Time from a valid keystroke with no bounce to allow the waveform to go from min. to 90% of the final magnitude of either frequency. Crystal parameters defined as R_S = 100Ω, L = 96mH, C = 0.02pF, and C_h = 5pF. V+≥3.4V F=3.579545 MHz.

NOTE 4: Only tones will be disabled when $\overline{CD}$ is taken to logical "0". Other chip functions may activate. Pull-up resistor on $\overline{CD}$ input will meet same spec as other inputs, R_1. Logic 0 = V-.

NOTE 5: Stand-by condition is defined as no keys activated, $\overline{CD}$ = Logical 1, $\overline{\text{Single Tone Disable}}$ = Logical 0.

NOTE 6: One key depressed only. Outputs unloaded.

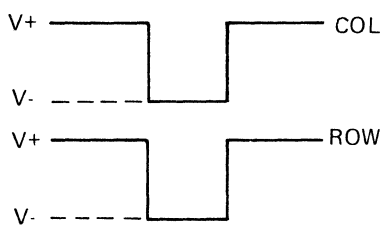
OSCILLATOR

The network contains an on-board inverter with sufficient loop gain to provide oscillation when used with a low cost television color-burst crystal. The inverter's input is OSC IN (pin 7) and output is OSC OUT (pin 8). The circuit is designed to work with a crystal cut to 3.579545 megahertz to give the frequencies in Table 1.

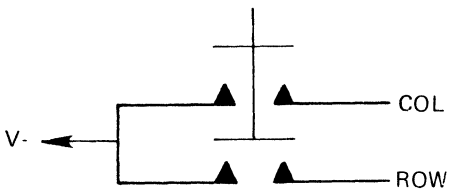
Any crystal frequency deviation from 3.579545 MHz will be reflected in the tone output frequency. Most crystals don't vary more than .02%.

CRYSTAL FREQUENCY
TABLE 1

	Standard DTMF (Hz)	Tone Output Frequency Using 3.579545 MHz Crystal	% Deviation From Standard
f_1	697	701.3	+0.62
f_2	770	771.4	+0.19
f_3	852	857.2	+0.61
f_4	941	935.1	-0.63
f_5	1209	1215.9	+0.57
f_6	1336	1331.7	-0.32
f_7	1477	1471.9	-0.35
f_8	1633	1645.0	+0.73



ELECTRONIC INPUT



2 OF 8 DTMF KEYBOARD

KEYBOARD CONFIGURATION

Each keyboard input is standard CMOS with a pull-up resistor to the V+ supply. These inputs may be controlled by a keyboard or electronic means. Open collector TTL or standard CMOS (operated off same supply as the MK 5089) may be used for electronic control.

The switch contacts used in the keyboards may be void of precious metals, due to the CMOS network's ability to recognize resistance up to 1kOHMS as a valid key closure.

ROW-COLUMN INPUTS

With $\overline{\text{single}}$ $\overline{\text{tone}}$ $\overline{\text{inhibit}}$ at V+, connection of V- to a single column will cause the generation of that column tone. Connection of V- to more than one column will result in no tones being generated. The application of V- to only a row pin or pins has no effect on the circuit. There must always be at least one column connected to V- for row tones to be generated. If a single row tone is desired, it may be generated by tying any two column pins and the desired row pin to V-. Dual tones will be generated if a single row pin and a single column pin are connected to V-

ANY KEY DOWN (PIN 10)

The any key down output is used for electronic control of receiver and/or transmitter switching and other desired functions. It switches to the V- supply when a keyboard button is pushed, and is open circuited when not. The AKD output switches regardless of the chip disable and single tone disable inputs.

$\overline{\text{CHIP}}$ $\overline{\text{DISABLE}}$ (PIN 2)

The $\overline{\text{chip}}$ $\overline{\text{disable}}$ input is used to defeat tone generation when the keyboard is used for other functions besides DTMF signaling. It has a pull-up to the V+ supply and when tied to the V- supply, tones are inhibited. All other chip functions operate normally.

$\overline{\text{SINGLE}}$ $\overline{\text{TONE}}$ $\overline{\text{INHIBIT}}$ (PIN 15)

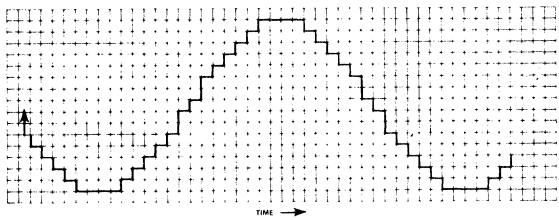
The $\overline{\text{single}}$ $\overline{\text{tone}}$ $\overline{\text{inhibit}}$ input is used to inhibit the generation of other than dual tones. It has a pull down to the V- supply and when floating or tied to V-, any input situation that would normally result in a single tone will now result in no tone, with all other chip functions operating normally.

When forced to the V+ supply, single or dual tones may be generated as described in the paragraph under Row-Column Inputs.

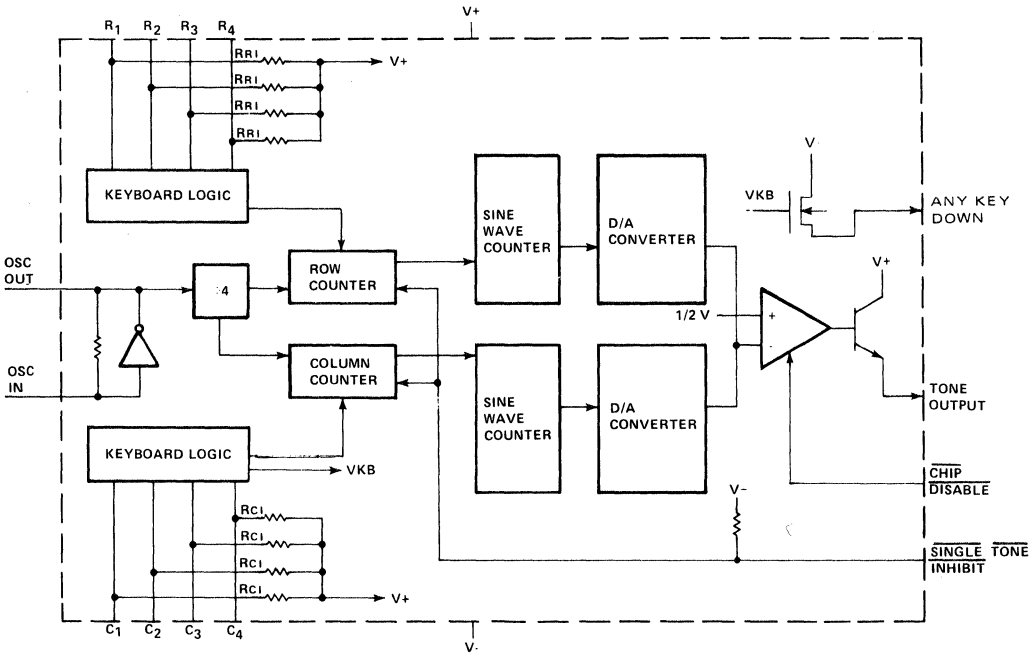
TONE OUTPUT (PIN 16)

The tone output pin is connected internally in the MK5089 to the emitter of an NPN transistor whose collector is tied to V+. The input to this transistor is the on-chip operational amplifier which mixes the row and column tones together and provides output level regulation.

TYPICAL SINE WAVE OUTPUT - SINGLE TONE, COLUMN



MK5089N BLOCK DIAGRAM



PRODUCT PROFILE

MOSTEK®

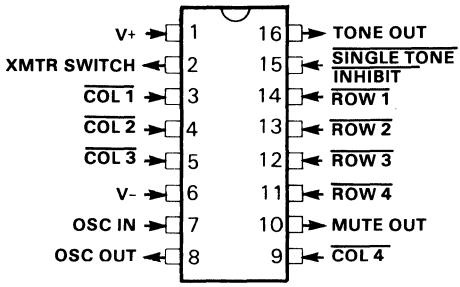
INTEGRATED TONE DIALER

MK5387

FEATURES

- Pin-for-pin compatible in keyboard applications with MK5087 with improved performance.
- Direct telephone-line operation with no external power supply
- Low standby power
- Minimum external parts count
- Uses inexpensive 3.579545 MHz television color-burst crystal to provide high-accuracy tones
- On-chip regulation of dual-and single-tone amplitudes
- Improved loop compensation
- Improved distortion
- Lower voltage operation - 2.5 volt instantaneous in loop applications
- Uses low-cost calculator-type keyboard (Form A contact) or standard 2-of-8 keyboard
- Auxiliary switching functions on chip
- Multiple key entry pin-selectable to either single tone or no tone

PIN CONNECTIONS



IV TONE DIALERS

DESCRIPTION

The MK5387 is a monolithic integrated circuit fabricated using the complementary - symmetry MOS (CMOS) process. A member of the Tone III* family of integrated tone-dialers, the MK5387 uses an inexpensive crystal reference to provide eight different audio sinusoidal frequencies, which are mixed to provide tones suitable for Dual-Tone-Multi-Frequency (DTMF) telephone dialing.

The MK5387 was designed specifically for integrated-tone-dialer applications that require the following: wide-supply operation with regulated output, scanned keyboard inputs which recognize either negative-true or Class A closures, and auxiliary switching functions. Keyboard entries to the MK5387 integrated tone-dialer cause the selection of the proper divide ratio to obtain the required two audio frequencies from the 3.579545 MHz reference oscillator.

* Trademark of Mostek Corporation

PRODUCT PROFILE

MOSTEK®

INTEGRATED TONE DIALER

MK5389

DESCRIPTION

The MK5389 is a monolithic integrated circuit fabricated using the complementary - symmetry MOS (CMOS) process. A member of the Tone III* family of integrated tone-dialers, the MK5389 uses an inexpensive crystal reference to provide eight different audio sinusoidal frequencies, which are mixed to provide tones suitable for Dual-Tone-Multi-Frequency (DTMF) telephone dialing.

The MK5389 was designed specifically for integrated tone-dialer applications that require the following: fixed - or regulated - supply operation where output is a function of supply voltage, scanned keyboard inputs which recognize either negative-true or Class A closures, $\overline{\text{Tone Disable}}$ input, and an $\overline{\text{Any Key Down}}$ output that is open circuit when no keyboard buttons are pushed and pulls to the V– supply when a button is pushed.

Keyboard entries to the MK5389 integrated tone-dialer cause the selection of the proper divide ratio to obtain the required two audio frequencies from the 3.579545 MHz reference oscillator.

* Trademark of Mostek Corporation

PRODUCT PROFILE

MOSTEK®

INTEGRATED TONE DIALER WITH REDIAL

MK5494

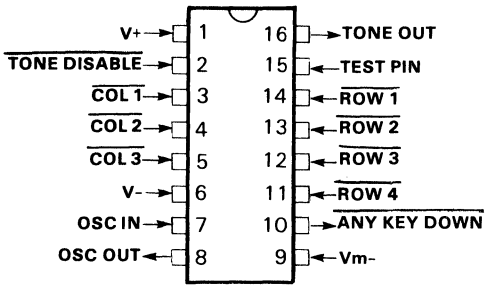
FEATURES

- Direct telephone-line operation with no external power supply
- Minimum external parts count
- Uses inexpensive 3.579545 MHz television color-burst crystal to provide high-accuracy tones
- Improved loop compensation
- Improved distortion
- Lower voltage operation - 2.5 volt instantaneous in loop applications
- Low standby power
- Uses low-cost calculator-type keyboard (Form A contact) or standard 2-of-8 keyboard with common V–
- $\overline{\text{Tone Disable}}$ allows $\overline{\text{Any Key Down}}$ output to function from keyboard input without tone generation
- On-chip regulation of dual- and single-tone amplitudes
- 13-digit last number redial
- Up to 2 PBX access digits may be dialed before using last number redial function
- Off-hook store into memory without dialing
- On-chip power-up-clear and memory-loss-detect circuitry
- Low on-hook memory retention current

DESCRIPTION

The MK5494 is a monolithic integrated circuit fabricated using the complementary - symmetry MOS (CMOS) process. A member of the Tone III* family of integrated tone-dialers, the MK5494 uses an inexpensive crystal reference to provide eight different audio sinusoidal frequencies, which are mixed to provide tones suitable for Dual-Tone-Multi-Frequency (DTMF) telephone dialing.

PIN CONNECTIONS



The MK5494 was designed specifically for integrated tone-dialer applications that require the following: wide-supply operation with regulated output, scanned keyboard inputs which recognize either negative-true or Class A closures, a $\overline{\text{Tone Disable}}$ input, and an $\overline{\text{Any Key Down}}$ output that is open circuit when no keyboard buttons are pushed and pulls to the V– supply when a button is pushed.

The MK5494 will redial up to 13 digits. The redial function may be employed immediately after going off-hook, after dialing one PBX access digit, or after dialing two PBX access digits. An "off-hook store" function allows a number to be entered into the last number dial memory for later use with no tones emitted during entry.

On-chip power-up-clear circuitry and memory-loss-detection circuitry ensure that no false numbers can be redialed due to power loss.

IV TONE DIALERS

*Trademark of Mostek Corporation

PRELIMINARY

MOSTEK®

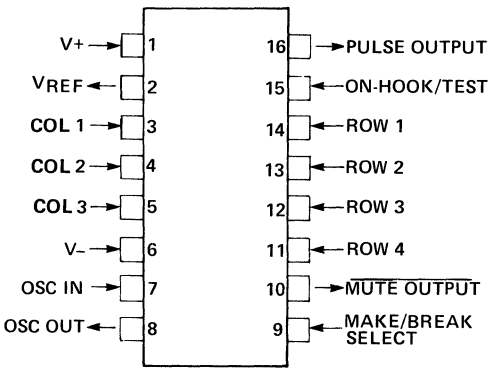
INTEGRATED PULSE DIALER WITH REDIAL

MK50981(N)

FEATURES

- Direct telephone-line operation
- CMOS technology is used for low-voltage, low-power operation
- Uses standard 2-of-7 matrix with pos. true common or the inexpensive Form A-type keyboard
- Ceramic resonator used as frequency reference for guaranteed accuracy.
- Make/Break ratio pin-selectable
- Redial with either a * or # input
- Provision for rapid testing
- On-chip voltage regulator
- Power-Up-Clear circuitry

PIN CONNECTIONS



DESCRIPTION

The MK50981 is a monolithic CMOS integrated circuit which converts keyboard inputs into pulse signal outputs simulating a rotary telephone dial. It is designed to operate directly from the telephone line and can be interfaced properly to meet telephone specifications in systems utilizing loop-disconnect signalling. Two outputs, one to pulse the telephone line and one to mute the receiver, are provided to implement the pulse dialer function. Accurate timing is accomplished by using a ceramic resonator as the frequency reference for the on-chip oscillator.

The MK50981 is in either the on-hook or off-hook mode as determined by the input to the pin designated "On-Hook/Test." In order to accept any key inputs, the MK50981 must be in the off-hook state. Upon sensing a key input, the normally static oscillator is enabled and the row and column inputs are al rnately strobed to verify that the keyboard input is valiu. The decoded input is then entered into an on-chip memory. The memory will store up to 17 digits and allows keystrokes to be entered at rates comparable to tone dialing telephones. Entering the first digit (except * or #) clears the memory buffer and starts the outpulsing sequence. As additional digits are entered, they are stored in the memory and outpulsed in turn. The memory has a FIFO-(first-in-first-out) type architecture and more than 17 digits may be dialed in any number sequence. The limitation is that there can never be more than 17 digits remaining to be outpulsed.

The MK50981 also features the redial function. Any 17-digit number sequence may be redialed with an * or # key input, providing that the circuit enters the on-hook mode for a finite time, t_{OH} (refer to discussion on the On-Hook/Test Pin).

An on-chip "Power-Up-Clear" circuit insures reliable operation of the MK50981. If the supply to the circuit should become insufficient to retain data in the memory (see electrical specifications), a "Power-Up-Clear" will occur upon regaining a proper supply level. This function will prevent the "Redial" or spontaneous outpulsing of incorrect data. A new number sequence may be entered in normal fashion.

Functions of the individual pins are described below:

V+ (Pin 1)

This is the positive supply input to the part and is measured relative to V- (pin 6). The voltage on this pin must be regulated to less than 6 volts using either the on-chip reference circuitry or an external form of regulation.

V_{REF} (Pin 2)

The V_{REF} output provides a negative reference voltage relative to the V+ supply. Its magnitude is a function of the internal parameters which define the minimum operating voltage of each part. In a typical application,

ABSOLUTE MAXIMUM RATINGS*

DC Supply Voltage, V+ ..... 6.2 Volts
Operating Temperature ..... -30°C to +60°C
Storage Temperature ..... -55°C to +150°C
Maximum Power Dissipation (25°C) 500mW
Maximum Voltage on any Pin ..... (V+) +0.3; (V−) −0.3 Volts

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

$-30°C \leq T_A \leq 60°C$
DC CHARACTERISTICS

Symbol	Parameter: Specific Conditions	Minimum	Typical*	Maximum	Units
V+	DC Supply Voltage	2.5		6.0	Volts
I_{MR}	Memory Retention Current: (Note 1)		0.7		μA
I_{OP}	DC Operating Current: (Note 2)		100	150	μA
V_{REF}	Magnitude of (V+ - V_{REF}): I_{SUPPLY} 150 μA	1.5	2.5	3.5	Volts
I_M	Mute Sink Current: V+ = 2.5, Vo = 0.5V	0.5	2.0		mA
I_P	Pulse Sink Current: V+ = 2.5V, Vo = 0.5V	1.0	4.0		mA
I_{LKG}	Mute and Pulse Leakage: V+ = 6.0V, Vo = 6.0V		0.001	1.0	μA
R_{KI}	Keyboard Contact Resistance			1.0	kΩ
C_{KI}	Keyboard Capacitance			30	pF
K_{IL}	"0" Logic Level	V-		20% of V+	Volts
K_{IH}	"1" Logic Level	80% of V+		V+	Volts
K_{RU}	Keyboard Pull-Up Resistance: (Note 3)		4.0		kΩ
K_{RD}	Keyboard Pull-Down Resistance: (Note 3)		100		kΩ
R_{OH}	On-Hook Pull-Up Resistance		100		kΩ

NOTES
*Typical values are to be used as a design aid and are not subject to production testing.
1. Current necessary for memory to be maintained. All outputs unloaded. On-Hook-mode.
2. Current required for proper circuit function. Off-Hook Mode, Valid Key input, V_{REF} tied to V-.
3. Keyboard to be scanned at 500Hz when oscillator enabled. Row and Column to alternately pull high and low.

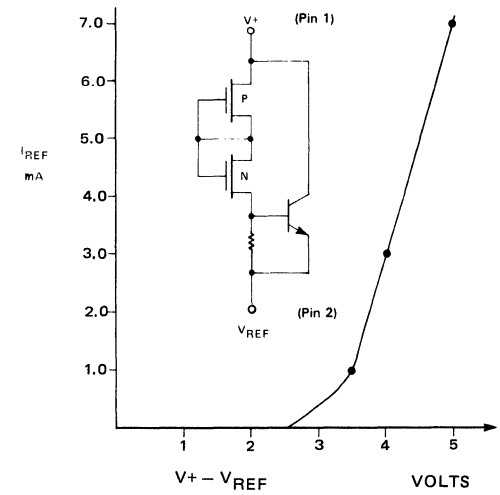
AC CHARACTERISTICS* (The Timing Relationships are shown in Figure 3)

Symbol	Parameter: Specific Conditions	Minimum	Typical	Maximum	Units
f_{OSC}	Oscillator Frequency (antiresonant mode) (Note 1)		480		kHz
t_{DB}	Keyboard debounce time		10		ms
t_{KD}	Time for Valid Key Entry	40			ms
t_{OS}	Oscillator Start-Up Time		6.0		ms
P_r	Pulse Rate		10.0		pps
t_B	Break Time: Pin 9 tied to V+/ tied to V-		61.0/67.0		ms
t_{IDP}	Interdigital Pause		800		ms

NOTES:
*Typical values are exact values with a nominal 480 kHz frequence reference (except for oscillator start-up time).
1. Ceramic resonator should have the following equivalent values: R $< 20\Omega$, $R_A \geq 70k\ \Omega$, Co $\leq$ 500pF.

as shown in Figure 4, the V_{REF} pin is simply tied to V- (Pin 6). The internal circuit with its associated I-V characteristic is shown in Figure 1.

TYPICAL I-V CHARACTERISTICS
Figure 1



KEYBOARD INPUTS (Pins 3,4,5,11,12,13,14)

The MK50981 incorporates an innovative keyboard scheme that allows either the standard 2-of-7 keyboard with positive common or the inexpensive single-contact (Form A) keyboard to be used, as shown in Figure 2.

A valid key entry is defined by either a single row being connected to a single column or V+ being simultaneously presented to both a single row and column.

When in the On-Hook mode, the row and column inputs are held high and no keyboard inputs are accepted. When Off Hook, the keyboard is completely static until the initial valid key input is sensed. The oscillator is then enabled and the rows and columns are alternately scanned (pulled high, then low) to verify the input is valid. The input must remain valid continuously for 10 ms of debounce time to be accepted.

V— (Pin 6)

This pin is the negative supply input.

OSCILLATOR IN, OUT (Pin 7,8)

The MK50981 contains an on-chip inverter with sufficient gain to provide oscillation when working with a low-cost 480kHz ceramic resonator (anti-resonant mode). In addition to the resonator, two external capacitors are required. Suggested equivalent values for the resonator are given in the timing specification section. These values will insure proper oscillator operation in the specified voltage range. The MK50981 may be driven externally with a 480kHz signal on Pin 7.

MAKE/BREAK SELECT (Pin 9)

The Make/Break ratio may be selected by connecting the pin to either the V+ or V- supply. Table 1 indicates the two popular ratios from which the user can choose.

KEYBOARD CONFIGURATION
Figure 2

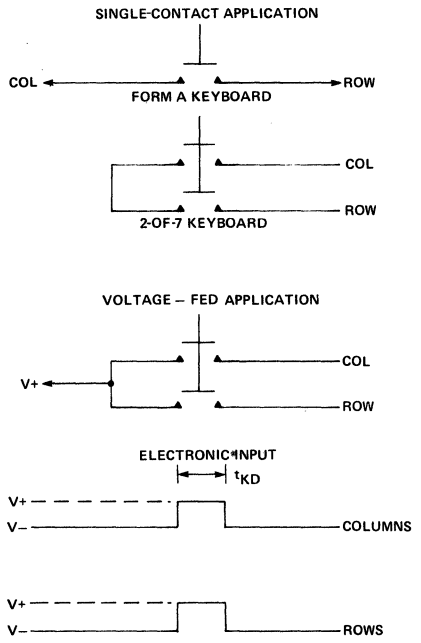


Table 1.
Make/Break Ratio Selection

Input to Make/Break Pin	Pulse Output	
	MAKE	BREAK
V+ (Pin 1)	39%	61%
V- (Pin 6)	33%	67%

MUTE OUTPUT (Pin 10)

The Mute Output consists of an open-drain N-channel transistor. It provides the logic necessary to mute the receiver while the telephone line is being pulsed. A typical way to interface this output is shown in the application diagram in Figure 4. Figure 3 shows the timing characteristics of the Mute Output.

ON-HOOK/TEST (Pin 15)

The "Test" or "On-Hook" input of the MK50981 has a 100kΩ pull-up to the positive supply. A V+ input or allowing the pin to float sets the circuit in its On-Hook or test mode, while a V- input sets it in the Off-Hook or Normal Mode.

When Off-Hook, the MK50981 will accept key inputs and outpulse the digits in normal fashion. Upon completion of the last digit, the oscillator is disabled and the circuit stands by for additional inputs.

Switching the MK50981 to On-Hook while it is outpulsing causes the remaining digits to be outpulsed at 100 x the normal rate (M/B ratio is then 50/50). This feature provides a means of rapidly testing the device and is also an efficient method by which the circuitry is reset. When the outpulsing in this mode, which can take up to 300ms, is completed, the circuit is deactivated and will require only the current necessary to sustain the memory and Power-Up-Clear detect circuitry (refer to the electrical specifications).

Upon returning Off-Hook, if the first key entry is either * or #, the number sequence stored on-chip will be outpulsed. Any other valid entries will clear the memory and outpulse the new number sequence.

PULSE OUTPUT(Pin 16)

The pulse output consists of an open-drain N-channel transistor. This output provides the logic necessary to pulse the telephone line with the correct Make/Break, pulse rate, and interdigital pause timings. The timing characteristics of the pulse output are shown in Figure 3.

TYPICAL APPLICATION

The schematic diagram in Figure 4 shows one method which can be used to interface the pulse dialer with the telephone line. In the approach shown, the pulse dialer circuitry is in parallel with the speech network.

A current source of some type is desired to present a high impedance to the telephone line while guaranteeing sufficient current to power the MK50981 ($\geq$ 150 μA). The current is sourced by the collector of transistor Q2. Its magnitude is determined by the voltage drop across R1, caused by the forward-biased diodes, D1 and D2. Transistor Q1 provides the quiescent current for the diodes and base drive for Q2.

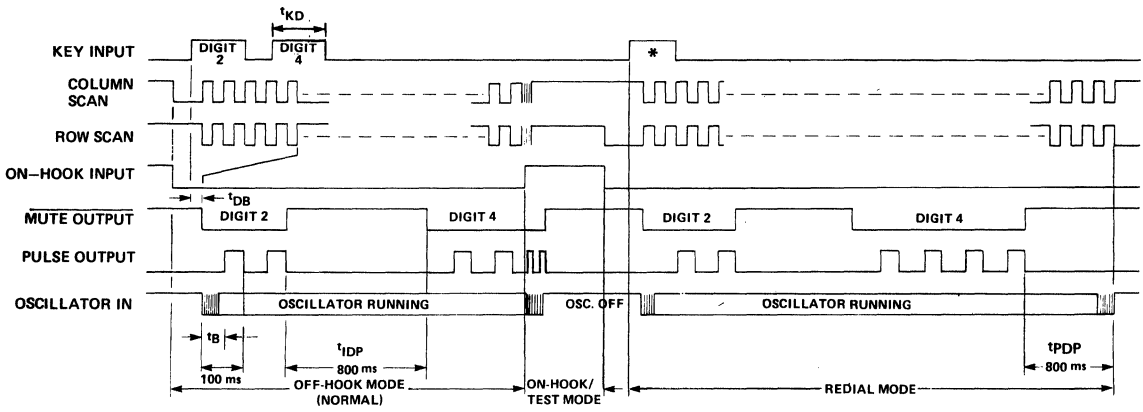
When in the On-Hook mode, S1 and S2 are open. This disables the current source and eliminates any excess current flow through the base-emitter junction of Q1 by allowing the emitter to be pulled to V+ through On-Hook. A large-value resistor, R3, allows a small amount of current to maintain the memory on the MK50981.

To return Off-Hook S1 and S2 are closed, thus tying the On-Hook pin to V-. The pulse and mute outputs drive external transistors to perform the outpulsing function. The speech network is connected through transistor Q5 to the telephone line. Mute holds this transistor on until outpulsing begins. The first break occurs when Mute switches low and the speech network is removed from the line. The pops caused by breaking the line are then isolated from the receiver. The pulse output drives darlington pair Q3 and Q4 to make and break the line until the digit has been completely pulsed. Mute then switches high, returning the speech network to the line.

Other implementations may consider a constant current diode for the current source or muting the network with a darlington. If your application requires muting the network with a relay, request information on our MK50991 outpulser.

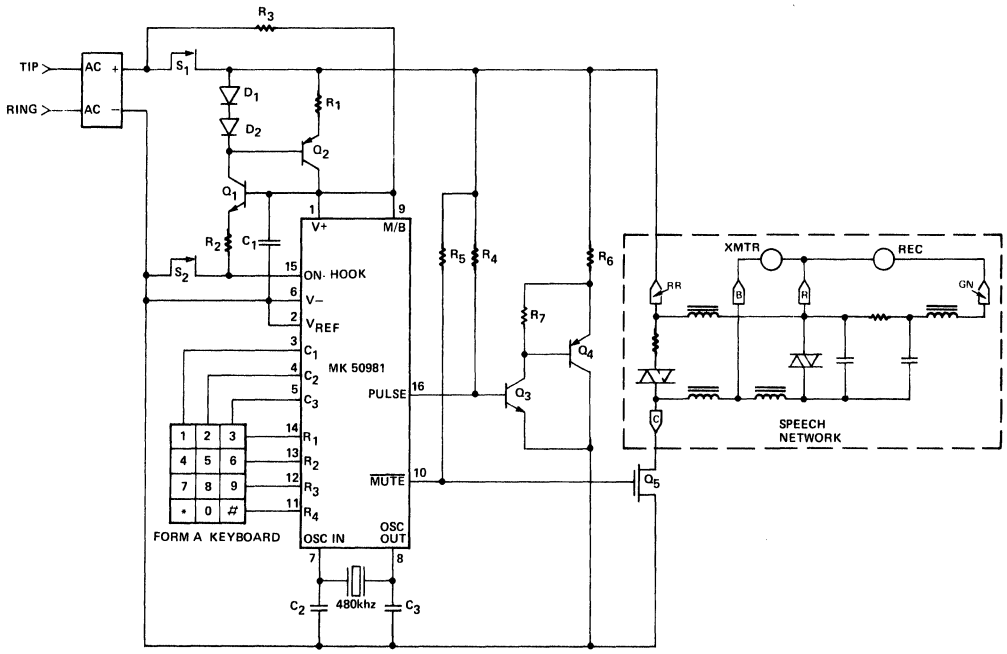
TIMING CHARACTERISTICS

Figure 3



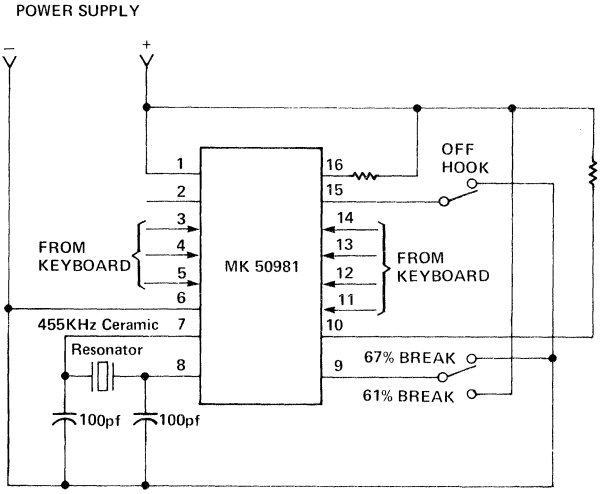
TYPICAL APPLICATION

Figure 4



Q_1 2N5550	Q_5 2N6661	C_2 100pF ±20%	R_3 22M
Q_2 2N5401	D_1 1N914	C_3 100pF ±20%	R_4 390k
Q_3 2N5550	D_2 1N914	R_1 2.7k	R_5 1M
Q_4 2N5401	C_1 20μF (LOW LEAKAGE)	R_2 75k	R_6 150Ω
			R_7 100k

TEST CIRCUIT
Figure 6



PRELIMINARY

MOSTEK®

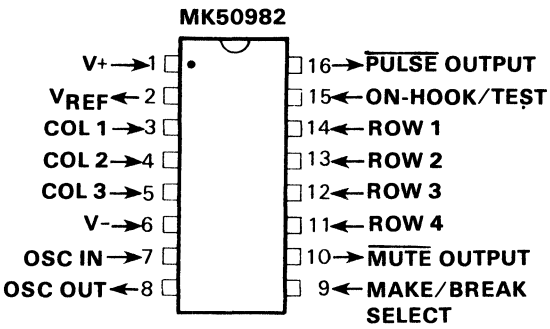
INTEGRATED PULSE DIALER WITH REDIAL

MK50982

FEATURES

- Direct telephone-line operation
- CMOS technology is used for low-voltage, low-power operation
- Uses standard 2-of-7 matrix with pos. true common or the inexpensive Form A-type keyboard
- Ceramic resonator used as frequency reference for guaranteed accuracy
- Make/Break ratio pin-selectable
- Redial with either * or #
- Provision for rapid testing
- On-chip voltage regulator
- Power-Up-Clear circuitry

PIN CONNECTIONS



DESCRIPTION

The MK50982 is a monolithic CMOS integrated circuit which converts keyboard inputs into pulse signal outputs simulating a rotary telephone dial. It is designed to operate directly from the telephone line and can be interfaced properly to meet telephone specifications in systems utilizing loop-disconnect signalling. Two outputs, one to pulse the telephone line and one to mute the receiver, are provided to implement the pulse dialer function. Accurate timing is accomplished by using a ceramic resonator as the frequency reference for the on-chip oscillator.

The MK50982 is in either the on-hook or off-hook mode as determined by the input to the pin designated, "On-Hook/Test." In order to accept any key inputs, the MK50982 must be in the off-hook state.

Refer to Figure 1 for a block diagram. Upon sensing a key input, the normally static oscillator is enabled and the row and column inputs are alternately strobed to verify that the keyboard input is valid. The decoded input is then entered into an on-chip memory. The memory will store up to 17 digits and allows keystrokes to be entered at rates comparable to tone dialing telephones. Entering the first digit (except* or #) clears the memory buffer and starts the outpulsing sequence. As additional digits are entered, they are stored in the memory and outpulsed in turn. The memory has FIFO-(first-in-first-out) type architecture and more than 17 digits may be dialed in any number sequence. The limitation is that there can never be more than 17 digits remaining to be outpulsed.

The MK50982 also features the redial function. Any 17-digit number sequence may be redialed with an * or # key input, providing that the circuit enters the on-hook mode for a finite time, t_{OH} (refer to discussion on the On-Hook/Test Pin).

An on-chip "Power-Up-Clear" circuit insures reliable operation of the MK50982. If the supply to the circuit should become insufficient to retain data in the memory (see electrical specifications), a "Power-Up-Clear" will occur upon regaining a proper supply level. This function will prevent the "Redial" or spontaneous outpulsing of incorrect data. A new number sequence may be entered in normal fashion.

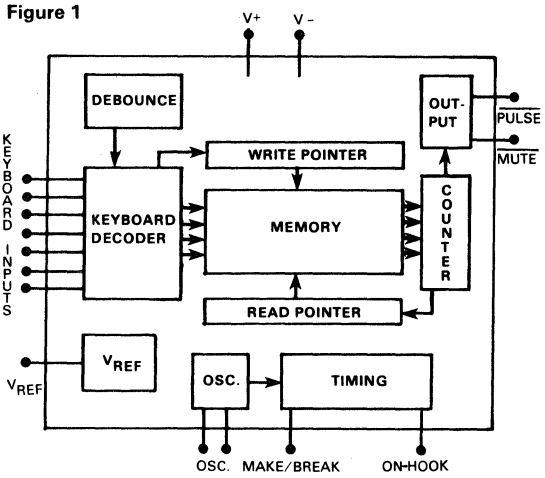
FUNCTIONAL DESCRIPTION

V+ (Pin 1)

This is the positive supply input to the part and is measured relative to V- (pin 6). The voltage on this pin must be regulated to less than 6 volts using either the on-chip reference circuitry or an external form of regulation.

BLOCK DIAGRAM

Figure 1

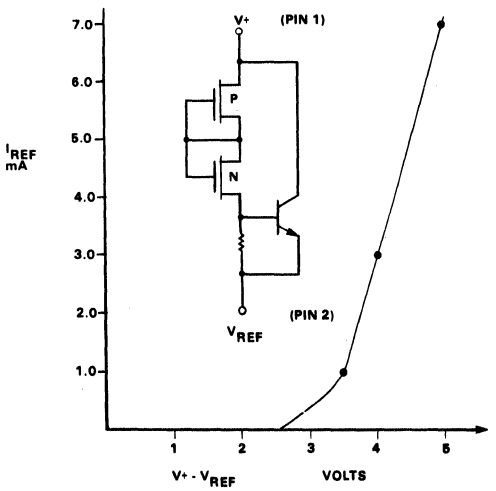


V_{REF} (Pin 2)

The V_{REF} output provides a negative reference voltage relative to the V+ supply. Its magnitude is a function of the internal parameters which define the minimum operating voltage of each part. In a typical application, as shown in Figure 5, the V_{REF} pin is simply tied to V-(Pin 6). The internal circuit with its associated I-V characteristic is shown in Figure 2.

TYPICAL I-V CHARACTERISTICS

Figure 2



V- (Pin 6)

This is the negative supply pin to which V_{REF} is normally tied (see V_{REF} paragraph).

KEYBOARD INPUTS (Pins 3,4,5,11,12,13,14)

The MK50982 incorporates an innovative keyboard scheme that allows either the standard 2-of-7 keyboard with positive common or the inexpensive single-contact (Form A) keyboard to be used, as shown in Figure 3.

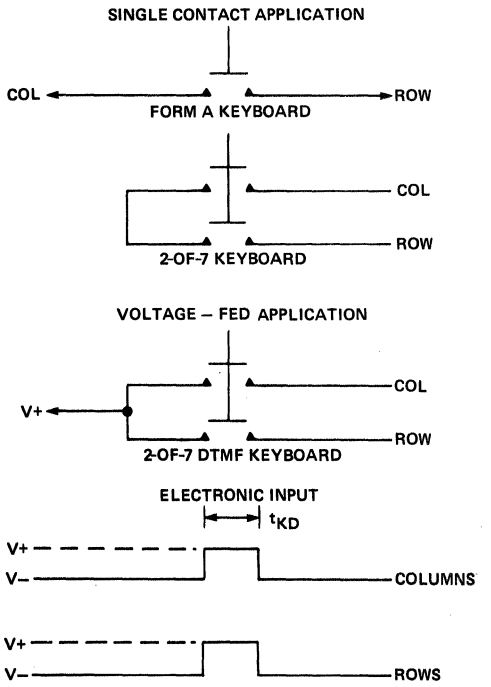
A valid key entry is defined by either a single row being connected to a single column or V+ being simultaneously presented to both a single row and column.

When in the On-Hook mode, the row and column inputs are held high and no keyboard inputs are accepted, thus preventing any accidental key contacts from causing excessive current flow.

When Off-Hook, the keyboard is completely static until the initial valid key input is sensed. The oscillator is then enabled and the row and columns are alternately scanned (pulled high, then low) to verify the input is valid. The input must remain valid continuously for 10ms of debounce time to be accepted.

KEYBOARD CONFIGURATION

Figure 3



OSCILLATOR IN, OUT (Pin 7,8)

The MK50982 contains an on-chip inverter with sufficient gain to provide oscillation when used with a low-cost 480kHz ceramic resonator (anti-resonant mode). In addition to the resonator, two external capacitors are required. Suggested equivalent values for the resonator are given in the timing specification section. These values will insure proper oscillator operation in the specified voltage range. The MK50982 may be driven externally with a 480kHz signal on Pin 7.

MAKE/BREAK SELECT (Pin 9)

The Make/Break ratio may be selected by connecting the pin to either the V+ or V- supply. Table 1 indicates the two popular ratios from which the user can choose.

MAKE/BREAK RATIO SELECTION
Table 1

Input to Make/Break Pin	Pulse Output	
	MAKE	BREAK
V+ (Pin 1)	39%	61%
V- (Pin 6)	33%	67%

$\overline{\text{MUTE}}$ OUTPUT (Pin 10)

The $\overline{\text{Mute}}$ output consists of an open-drain N-channel transistor. It provides the logic necessary to mute the receiver while the telephone line is being pulsed. A typical method of interfacing this output is shown in the application diagram in Figure 5. Figure 6 shows the timing characteristics of the $\overline{\text{Mute}}$ output.

ON-HOOK/TEST (Pin 15)

The "Test" or "On-Hook" input of the MK50982 has a 100kΩ pull-up to the positive supply. A V+ input or allowing the pin to float sets the circuit in its On-Hook or test mode, while a V- input sets it in the Off-Hook or Normal Mode. Any digits to be tested in the "On-Hook/Test" mode must be entered while "Off-Hook."

When Off-Hook, the MK50982 will accept key inputs and outpulse the digits in normal fashion. Upon completion of the last digit, the oscillator is disabled and the circuit stands by for additional inputs.

Switching the MK50982 to On-Hook while it is outpulsing causes the remaining digits to be outpulsed at 100 x the normal rate (M/B ratio is then 50/50). This feature provides a means of rapidly testing the device and is also an efficient method by which the circuitry is reset. When the outpulsing in this mode, which can take up to 300ms, is completed, the circuit is deactivated and will require only the current necessary to sustain the memory and Power-Up-Clear detect circuitry (refer to the electrical specifications).

Upon returning Off-Hook, if the first key entry is either * or #, the number sequence stored on-chip will be outpulsed. Any other valid entries will clear the memory and outpulse the new number sequence.

$\overline{\text{PULSE}}$ OUTPUT (Pin 16)

The $\overline{\text{Pulse}}$ output is an open-drain N-Channel transistor designed to drive an external bipolar transistor. These transistors would normally be used to pulse the telephone line by controlling the loop current through the network. The timing characteristics of the $\overline{\text{Pulse}}$ output are shown in Figure 6.

TEST CIRCUIT

A test circuit is shown in Figure 4. This circuit can be used to demonstrate the basic operation of the MK50982.

TYPICAL APPLICATION

The schematic diagram in Figure 5 shows one method which can be used to interface the pulse dialer with the telephone line. In the approach shown, the pulse dialer circuitry is in series with the speech network.

A current source of some type is desired to present a high impedance to the telephone line while guaranteeing sufficient current to power the MK50982 ($\geq$ 150 μA). The current source shown is constructed with two components, Q2 and R1. The current is regulated by the negative feedback provided by R1 to the gate of Q2. Several other implementations can be considered, such as a constant current diode, or a configuration using bipolar transistors.

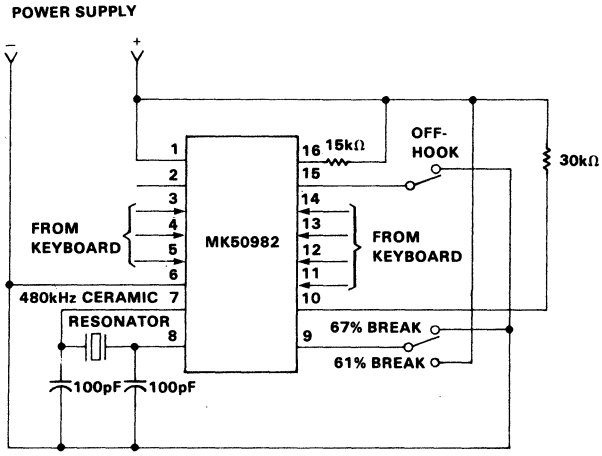
The purpose of transistor Q1 is to take the place of an additional hookswitch contact. When S1 closes, Q1 is turned on and On-Hook (pin 15) is pulled to V-. This sets the MK50982 in the normal mode, ready to accept key inputs.

When going On-Hook, S1 is opened, causing Q1 to be turned off. An on-chip resistor pulls pin 15 to V+ and the current source is disabled. The purpose of D1 is to limit any reverse current flow through the current source. A large-value resistor, R3, allows a small amount of current to maintain the memory on MK50982.

To return Off-Hook, S1 is closed, causing Q1 to be turned on thus tying the On-Hook pin to V-. The $\overline{\text{Pulse}}$ and $\overline{\text{Mute}}$ outputs drive external transistors to perform the outpulsing function. The receiver is connected through transistor Q6 to the speech network. $\overline{\text{Mute}}$ causes the transistor to be held on until outpulsing begins. When $\overline{\text{Mute}}$ switches low, the receiver is removed from the speech network. The pops caused by breaking the line are then isolated from the receiver. The $\overline{\text{Pulse}}$ output drives transistors Q3 and Q5 to make and break the line until the digit has been completely outpulsed. $\overline{\text{Mute}}$ then switches high, returning the receiver to the speech network.

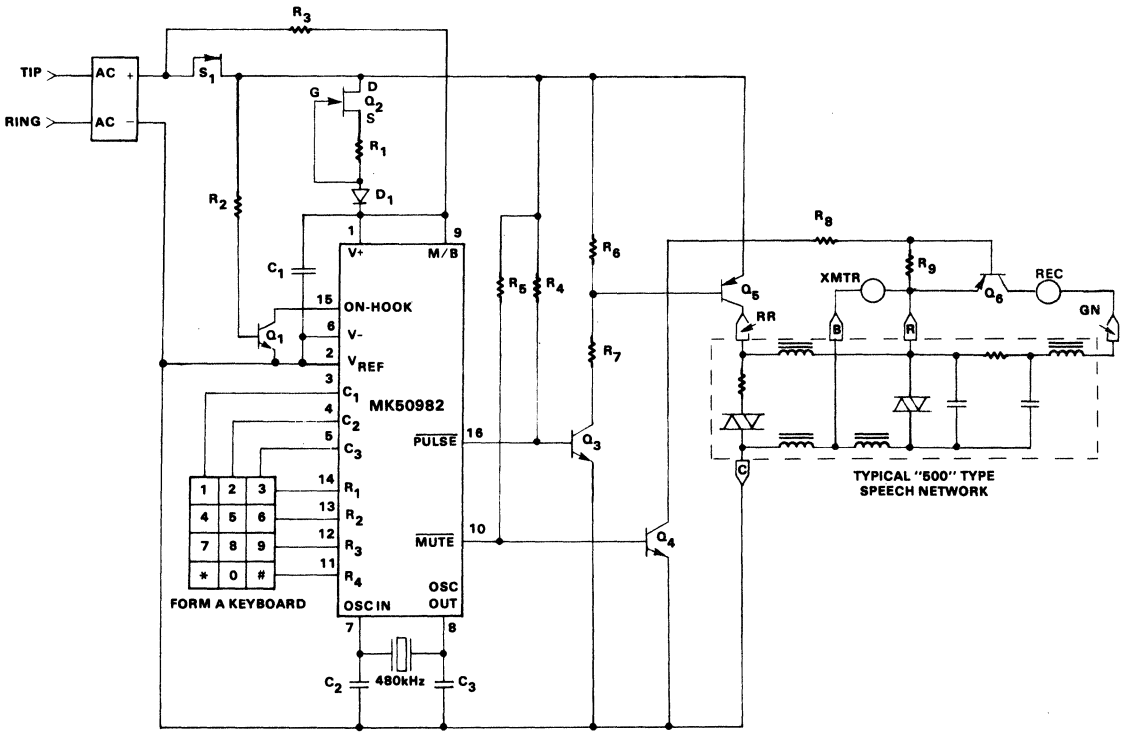
TEST CIRCUIT

Figure 4



TYPICAL APPLICATION

Figure 5



Q1, 3, 4 = 2N5550	D1 = 1N914	R1 = 8kΩ	R4, 5 = 390kΩ
Q5, 6 = 2N5401	C1 = 20μF (low leakage)	R2 = 500kΩ	R6, 9 = 100kΩ
Q2 = 2N3822	C2, 3 = 100pF ± 20%	R3 = 22MΩ	R7, 8 = 3kΩ

ABSOLUTE MAXIMUM RATINGS

DC Supply Voltage, V+ ..... 6.2 Volts
Operating Temperature ..... -30°C to +60°C
Storage Temperature ..... -55°C to +150°C
Maximum Power Dissipation (25°C) 500mW
Maximum Voltage on any Pin ..... (V+) +0.3; (V-) -0.3 Volts

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

$-30°C \leqslant T_A \leqslant 60°C$
DC CHARACTERISTICS

SYM	PARAMETER: SPECIFIC CONDITIONS	MIN	TYP*	MAX	UNITS
V+	DC Supply Voltage	2.5		6.0	V
I_{MR}	Memory Retention Current: Note 1		0.7		μA
I_{OP}	DC Operating Current: Note 2		100	150	μA
V_{REF}	Magnitude of (V+ - V_{REF}): I_{SUPPLY} = 150 μA	1.5	2.5	3.5	V
I_M	Mute Sink Current: V+ = 2.5, V_O = 0.5V	0.5	2.0		mA
I_P	Pulse Sink Current: V+ = 2.5V, Vo = 0.5V	1.0	4.0		mA
I_{LKG}	Mute and Pulse Leakage: V+ = 6.0V, Vo = 6.0V		0.001	1.0	μA
R_{KI}	Keyboard Contact Resistance			1.0	kΩ
C_{KI}	Keyboard Capacitance			30	pF
K_{IL}	"0" Logic Level	V-		20% of V+	V
K_{IH}	"1" Logic Level	80% of V+		V+	V
K_{RU}	Keyboard Pull-Up Resistance: Note 3		4.0		kΩ
K_{RD}	Keyboard Pull-Down Resistance: Note 3		100		kΩ
R_{OH}	On-Hook Pull-Up Resistance		100		kΩ

NOTES
*Typical values are to be used as a design aid and are not subject to production testing.
1. Current necessary for memory to be maintained. All outputs unloaded.On-Hook mode.
2. Current required for proper circuit function. Off-Hook mode, Valid Key input, V_{REF} tied to V-.
3. Keyboard to be scanned at 500Hz when oscillator enabled. Row and Column to alternately pull high and low.

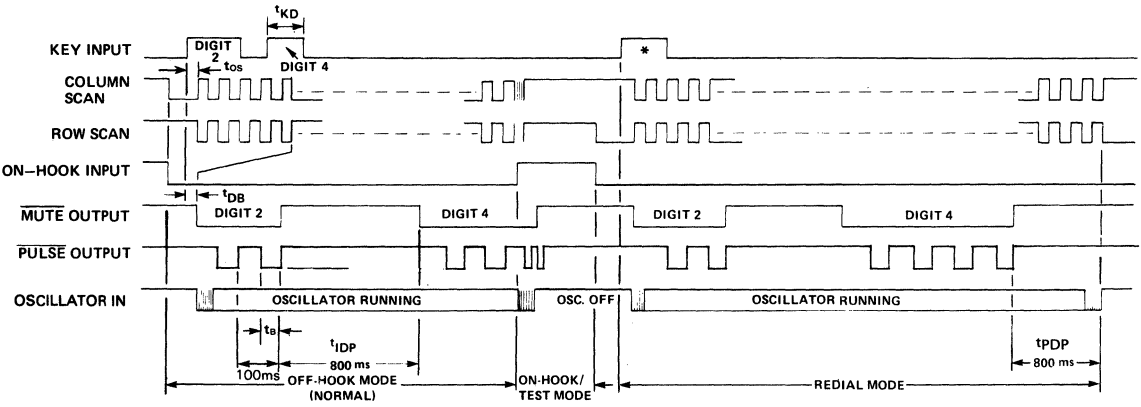
AC CHARACTERISTICS* (The timing Relationships are shown in Figure 6)

SYM	PARAMETER: SPECIFIC CONDITIONS	MIN	TYP	MAX	UNITS
f_{OSC}	Oscillator Frequency (antiresonant mode): Note 1		480		kHz
t_{DB}	Keyboard Debounce Time		10		ms
t_{KD}	Time for Valid Key Entry	40			ms
t_{OS}	Oscillator Start-Up Time		6.0		ms
P_R	Pulse Rate		10.0		pps
t_B	Break Time: Pin 9 Tied to V+/Tied to V-		61.0/67.0		ms
t_{IDP}	Interdigital Pause		800		ms

NOTES:
*Typical values are exact with a nominal 480 kHz frequence reference (except for oscillator start-up time).

Ceramic resonator should have the following equivalent values: R <20Ω, $R_A \geqslant$ 70k Ω, Co ≤ 500pF.

TIMING CHARACTERISTICS
Figure 6



PRELIMINARY

MOSTEK®

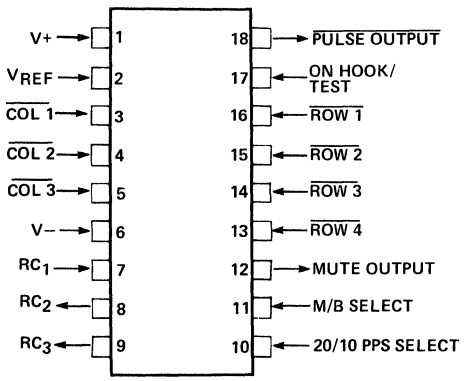
INTEGRATED PULSE DIALER WITH REDIAL

MK50991(N)

FEATURES

- Direct telephone-line operation
- CMOS technology is used for low-voltage, low-power operation
- Uses either a standard 2-of-7 matrix keyboard or the inexpensive Form A-type keyboard
- Inexpensive RC oscillator used as frequency reference
- Redial with either a * or # input
- Make/Break ratio and pulse rate are pin-selectable
- Provision for rapid testing
- On-chip voltage regulator
- Power-up-clear circuitry

PIN CONNECTIONS



V PULSE DIALERS WITH REDIAL

DESCRIPTION

The MK50991 is a monolithic CMOS integrated circuit which converts keyboard inputs into pulse signal outputs simulating a rotary telephone dial. It is designed to operate directly from the telephone line and can be interfaced properly to meet telephone specifications in systems utilizing loop-disconnect signalling. Two outputs are provided to implement the pulse dialer function, one to pulse the line and another to mute the receiver. The mute output can be interfaced with a bistable latching relay in applications with this requirement.

The MK50991 is in either the on-hook or off-hook mode as determined by the input to the pin designated "On-Hook/Test." In order to accept any key inputs, the MK50991 must be in the off-hook state. Upon sensing a key input, the normally static oscillator is enabled and the row and column inputs are alternately strobed to verify that the keyboard input is valid. The decoded input is then entered into an on-chip memory. The memory will store up to 17 digits and allows keystrokes to be entered at rates comparable to tone dialing telephones. Entering the first digit (except * or #) clears the memory buffer and starts the outpulsing sequence. As additional digits are entered, they are stored in the memory and outpulsed in turn. The memory has a FIFO—(first-in-first-out) type architecture and more than 17 digits may be dialed in any number sequence. The limitation is that there can never be more than 17 digits remaining to be outpulsed.

The MK50991 also features the redial function. Any 17-digit number sequence may be redialed with a * or # key input, providing that the circuit enters the on-hook mode for a finite time, t_{OH} (refer to discussion on the On-Hook/Test pin).

An on-chip "Power-Up-Clear" circuit insures reliable operation of the MK50991. If the supply to the circuit should become insufficient to retain data in the memory (see electrical specifications), a "Power-Up-Clear" will occur upon regaining a proper supply level. This function will prevent the "Redial" or spontaneous outpulsing of incorrect data. A new number sequence may then be entered in normal fashion.

ABSOLUTE MAXIMUM RATINGS*

DC Supply Voltage, V+ ..... 6.2 Volts
Operating Temperature ..... -30°C to +60°C
Storage Temperature ..... -55°C to +150°C
Maximum Power Dissipation 25°C 500mW
Maximum Voltage on any Pin ..... (V+) + 0.3; (V-) - 0.3 Volts

*Stresses above these listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS
-30°C < TA < 60°C

DC CHARACTERISTICS

Symbol	Parameter: Specific Conditions	Minimum	Typical*	Maximum	Units
V+	DC Operating Voltage	2.5		6.0	Volts
I_{MR}	Memory Retention Current: (Note 1)		0.7		μA
I_{OP}	DC Operating Current: (Note 2)		100	150	μA
V_{REF}	Magnitude of (V+ - Vref): I_{supply} = 150μA	1.5	2.5	3.5	Volts
I_{ML}	Mute Sink Current: V+ = 2.5V, Vo = 0.5V	0.5	2.0		mA
I_{MH}	Mute Source Current: V+ = 2.5V, Vo = 2.0V	0.5	2.0		mA
I_P	Pulse Sink Current: V+ = 2.5V, Vo = 0.5V	1.0	4.0		mA
I_{LKG}	Mute and Pulse Leakage: V+ = 6.0V, Vo = 6.0V		0.001	1.0	μA
R_{KI}	Keyboard Contact Resistance			1.0	kΩ
C_{KI}	Keyboard Capacitance			30	pF
K_{IL}	Keyboard "0" Logic Level	V-		20% of V+	Volts
K_{IH}	Keyboard "1" Logic Level	80% of V+		V+	Volts
K_{RU}	Keyboard Pull-Up Resistance: (Note 3)		100		kΩ
K_{RD}	Keyboard Pull-Down Resistance: (Note 3)		4.0		kΩ
R_{OH}	On-Hook Pull-Up Resistance		100		kΩ

Notes:
*Typical values are to be used as a design aid and are not subject to production testing.
1. Current necessary for memory to be maintained. All outputs unloaded. On-Hook mode. VREF tied to V-
2. Current required for proper circuit function. Off-Hook Mode, Valid key input, Vref tied to V-.
3. Keyboard to be scanned at 500Hz when oscillator enabled. Row and Column to alternately pull high and low.

AC CHARACTERISTICS
(The Timing Relationships are shown in Figure 4)

Symbol	Parameter: Specific Conditions	Minimum	Typical	Maximum	Units
f_{OSC}	Oscillator Frequency (Note 1)		4.0		kHz
Δf_{OSC1}	Frequency Stability: 2.5 to 3.5V (Note 2)		± 4		%
Δf_{OSC2}	Frequency Stability: 3.5 to 6.0V (Note 2)		± 4		%
Δf_{OSC3}	Frequency Stability: 150→500 μA (Note 3)		± 3		%
Pr	Pulse Rate: Pin 10 tied to V+/V-		20/10		pps
t_{DB}	Keyboard Debounce Time		10		ms
t_{KD}	Time for Valid Key Entry	40			ms
t_B	Break Time: Pin 9 tied to V+/ tied to V-		66.0/60.0		ms
t_{IDP}, t_{PDP}	Interdigital Pause, Predigital Pause (Note 4)		800+ t_M		ms
t_{MO}	Mute Overlap of Pulse		5		ms

NOTES:
"Typical" values are exact assuming a 4kHz frequency reference.
1. A change in the frequency will result in a proportional change in all circuit timing.
2. For stated voltages, the given "typical" Δfosc holds from part to part over the stated operating temperature range.
3. Using Vref in conjunction with a current source results in the given "typical" Δfosc from part to part over the stated operating temperature and current.
4. Time from last break to next break, t_M = 100ms-t_B = make time.

Functions of the individual pins are described below:

V+ (Pin 1)

This is the positive supply input to the part and is measured relative to V- (pin 6). The voltage on this pin must be regulated to less than 6 volts using either the on-chip reference circuitry or an external form of regulation.

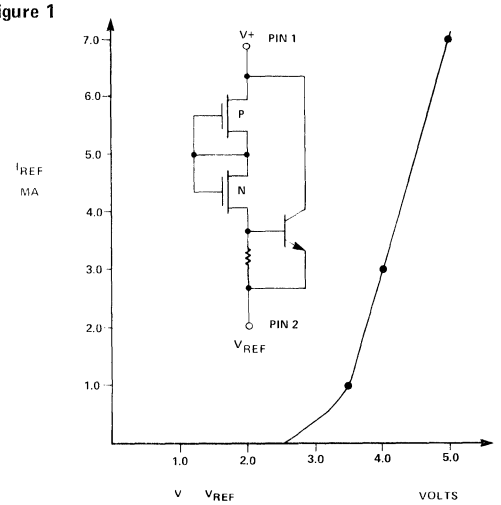
V_{REF} (Pin 2)

The V_{REF} output provides a negative reference voltage relative to the V+ supply. Its magnitude is a function of the internal parameters which define the minimum operating voltage of each part. In a typical application, as shown in Figure 5, the V_{REF} pin is simply tied to V-(Pin 6). The internal circuit with its associated I-V characteristic is shown in Figure 1.

KEYBOARD INPUTS (Pins 3,4,5,13,14,15,16)

The MK50991 incorporates an innovative keyboard

V_{REF} TYPICAL I–V CHARACTERISTICS
Figure 1



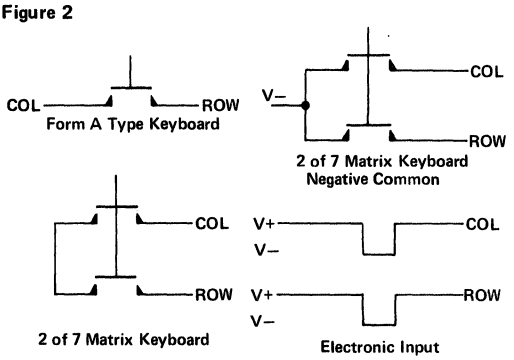
scheme that allows either the standard 2-of-7 keyboard with positive common or the inexpensive single contact (Form A) keyboard to be used.

A valid key entry is defined by either a single row being connected to a single column or V- being simultaneously presented to both a single row and column.

When in the On-Hook mode, the row and column inputs are held high and no keyboard inputs are accepted. When Off-Hook, the keyboard is completely static until the initial valid key input is sensed. The oscillator is then enabled and the rows and columns are alternately scanned (pulled high, then low) to verify the input is valid. The input must remain valid continuously for 10 ms of debounce time to be accepted.

KEYBOARD CONFIGURATIONS

Figure 2



RC OSCILLATOR (Pins 7,8,9)

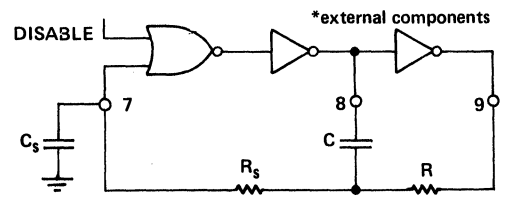
The MK50991 contains on-chip inverters to provide an oscillator which will operate with a minimum of external components. Figure 3 shows the on-chip configuration with the necessary external components. Optimum stability occurs with the ratio $K = R_S/R$ equal to 10. The oscillator period is given by:

$$T = RC \left[1.386 + \frac{3.5KCs}{C} - \frac{2K}{K+1} \ln\left(\frac{K}{1.5K + 0.5}\right) \right]$$

where C_S is the stray capacitance on Pin 7. Accuracy and stability will be enhanced with the capacitance minimized.

OSCILLATOR CONFIGURATION

Figure 3



20/10 PPS SELECT (Pin 10)

Tying this input to either V+ (Pin 1) or V- (Pin 6) will select a pulse rate of either 20 or 10 pps respectively.

MAKE/BREAK SELECT (Pin 11)

The Make/Break ratio may be selected by connecting the pin to either the V+ or V- supply. The table below indictates the two popular ratios from which the user can choose.

MAKE/BREAK RATIO SELECTION

Table 1

INPUT TO MAKE/BREAK PIN	PULSE OUTPUT	
	MAKE	BREAK
V+ (Pin 1)	34%	66%
V– (Pin 6)	40%	60%

MUTE OUTPUT (Pin 12)

The Mute output consists of a complementary pair of CMOS transistors. It provides the logic necessary to be interfaced with a bistable latching relay to Mute the speech network. Upon coming off-hook, a negative transition on Mute will insure the speech network is properly connected to the telephone line. When outpulsing begins, a positive transition will switch the relay, continuously muting the network until the entire number sequence entered is outpulsed. Figure 4 shows, in detail, the timing diagram of the Mute Output.

ON-HOOK/TEST (Pin 17)

The "Test" or "On-Hook" input of the MK50991 has a 100kΩ pull-up to the positive supply. A V+ input or allowing the pin to float sets the circuit in its On-Hook or test mode while a V- input sets it in the Off-Hook or Normal Mode.

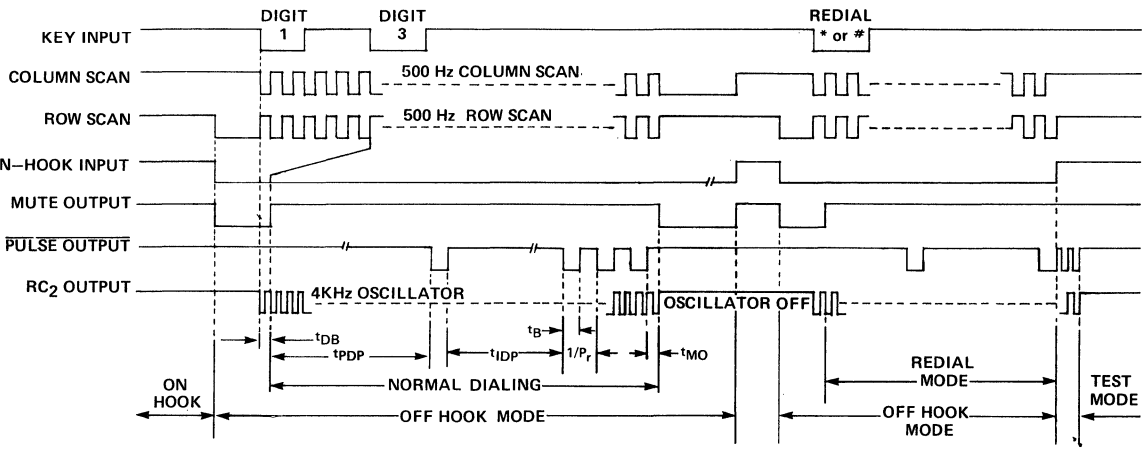
When Off-Hook, the MK50991 will accept key inputs and outpulse the digits in normal fashion. Upon completion of the last digit, the oscillator is disabled and the circuit stands by for additional inputs.

Switching the MK50991 to On-Hook while it is outpulsing causes the remainingdigits to be outpulsed at 100 x the normal rate (M/B ratio is then 50/50). This feature provides a means of rapidly testing the device and is also an efficient method by which the circuitry is reset. When the outpulsing in this mode, which can take up to 300ms, is completed, the circuit is deactivated and will require only the current necessary to sustain the memory and Power-Up-Clear detect circuitry (refer to the electrical specifications).

Upon returning Off-Hook, a negative transistion on the Mute Output will insure the speech network is connected to the line. If the first key entry is either a * or #, the number sequence stored on-chip will be outpulsed. Any other valid key entries will clear the memory and outpulse the new number sequence.

TIMING CHARACTERISTICS

Figure 4



PULSE OUTPUT (Pin 16)

The Pulse Output consists of an open-drain N-channel transistor. This output provides the logic necessary to pulse the telephone line with the correct Make/Break, pulse rate, and interdigital pause timings. The timing characteristic of the Pulse Output is shown in Figure 4 above.

TYPICAL APPLICATION

The schematic diagram in Figure 5 shows one method which can be used to interface the MK50991 with the telephone line. In this approach, the speech network is connected directly to the telephone line through a metallic relay contact. The pulse signalling circuitry is in parallel with the speech network.

A current source of some type is desired to present a high impedance to the telephone line while guaranteeing sufficient current to power the MK50991 (>150μA). Transistor Q_2 provides the source current to the device. The magnitude of this current is determined by the voltage on R_1 due to the forward-biased diodes D_1 and D_2. Transistor Q_1 provides a regulated bias current to the diodes as well as Q_2.

When in the On-Hook mode, S_1 and S_2 are open. The current source is disabled in this manner and only a small amount of current, supplied through R_3, is needed to maintain data in the memory. The relay is open, thereby disconnecting the speech network from the telephone line.

When coming Off-Hook, switches S1 and $S\bar{2}$ close, connecting the On-Hook input to V-. Immediately the output of Mute switches low. This transition pulses the relay through Q_5 and Q_6, latching it in the closed position. The speech network is now attached directly to the telephone line for normal conversation. Diode D3 will hold the pulsing darlington composed of transistors Q_3 and Q_4 off.

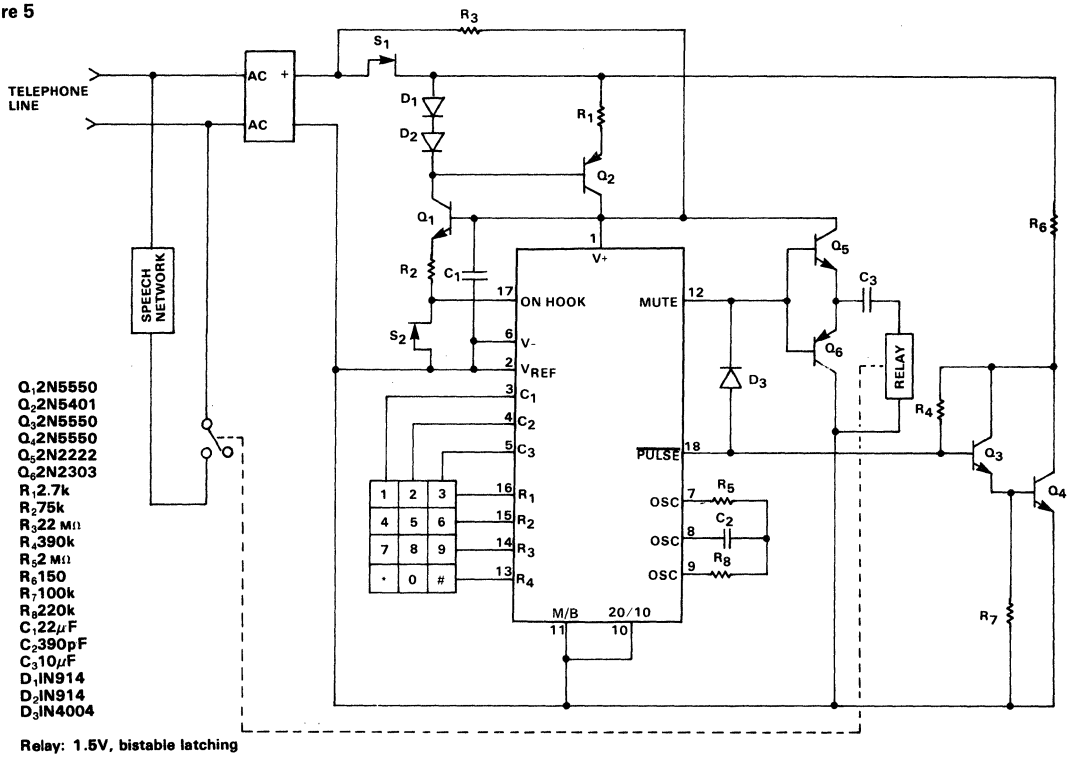
Upon receiving a valid key entry, Mute switches high. This transition pulses the relay to its open state, thereby muting the network. The loop current is still passed through the darlington pair, Q_3 and Q_4, for a predigital pause time of approximately 840ms. (t_{PDP}). Break is accomplished when the Pulse output switches low, cutting the darlington off. During break, current flow is limited to the current source and the Pulse pullup resistor $R\bar{4}$, insuring a high impedence in this interval. Pulsing of the complete digit continues in this manner. Each digit in the number sequence dialed is separated by standard interdigital pauses (t_{IDP}).

After the final digit is outpulsed, the Mute Output returns low and the speech network is connected back to the telephone line through the relay contact for normal conversation. Returning On-Hook causes Mute to switch high, removing the network from the line.

Applications which do not require operation with a bistable relay may use our MK50981 pulse dialer to better advantage.

TYPICAL APPLICATION

Figure 5

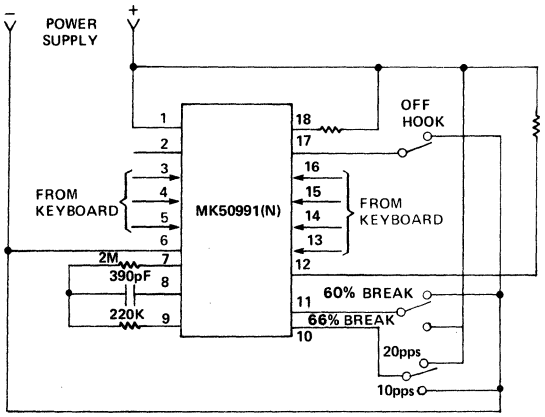


Q_1 2N5550
Q_2 2N5401
Q_3 2N5550
Q_4 2N5550
Q_5 2N2222
Q_6 2N2303
R_1 2.7k
R_2 75k
R_3 22 MΩ
R_4 390k
R_5 2 MΩ
R_6 150
R_7 100k
R_8 220k
C_1 22μF
C_2 390pF
C_3 10μF
D_1 IN914
D_2 IN914
D_3 IN4004

Relay: 1.5V, bistable latching

TEST CIRCUIT

Figure 6



PRELIMINARY

MOSTEK®

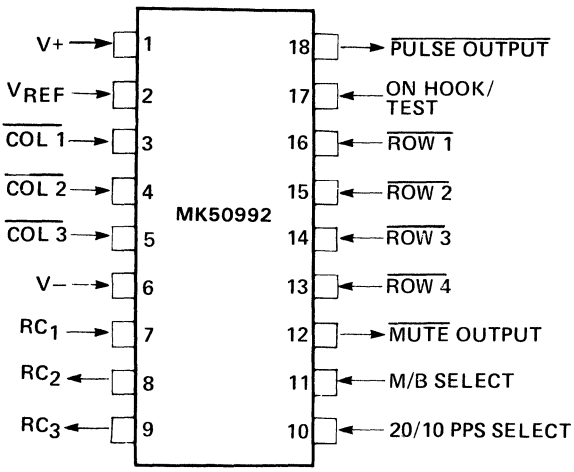
INTEGRATED PULSE DIALER WITH REDIAL

MK50992(N)

FEATURES

- Direct Telephone Line Operation
- Uses Standard 2-of-7 Keyboard board
- CMOS Technology for Low-Voltage, Low-Power Operation
- Supply Voltage Range 2.5 to 6 volts
- MAKE/BREAK Ratio Pin-Selectable
- 20/10pps Pin-Selectable
- Redial with # or *
- Continuous Mute
- Inexpensive RC Oscillator

PIN CONNECTIONS



DESCRIPTION

The MK50992 is a monolithic CMOS integrated circuit which uses an inexpensive RC oscillator for its frequency reference and provides all the features required for implementing a pulse dialer with redial. It operates directly off the telephone line supply and converts 2-of-7 keyboard inputs into pulse signals simulating a rotary telephone dial. When not outpulsing, the MK50992 consumes only microamperes of current.

Keyboard logic is totally static so that the MK50992 will not introduce noise into the telephone system. Two outputs, one to pulse the telephone line and one to mute the receiver, are provided to implement the pulse dialer function.

When off-hook, the MK50992 senses a key down condition, verifies that only one key is depressed and then enters the key's code into an on-chip memory.

The memory will store up to 17 digits, and allows keystrokes to be entered at rates comparable to tone dialing telephones. Entering the first digit starts a predigital pause counter and clears the memory buffer. At the end of the predigital pause, outpulsing begins. As digits are entered during the outpulsing period they will also be stored in the memory. Outpulsing will continue until all entered digits have been dialed. The first 17 digits entered will be stored in the on-chip redial memory and can be redialed by pressing either # or *, provided that the receiver has gone on-hook for the minimum t_{OH} (refer to the electrical specifications section).

When on-hook, key inputs will not be recognized because the oscillator is disabled. This oscillator inhibit prevents the circuit from drawing excessive current when on-hook.

ABSOLUTE MAXIMUM RATINGS*

DC Supply Voltage, V+ ..... 6.2 Volts
Operating Temperature ..... -30° to +60°C
Storage Temperature ..... -55°C to +150°C
Maximum Power Dissipation @ 25°C 500mW
Maximum Voltage on any Pin Relative to V- ..... -0.3 Volts
Maximum Voltage on any Pin Relative to V+ ..... +0.3 Volts

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS
$-30° \leqslant T_A \leqslant 60°C$

DC CHARACTERISTICS

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V+	DC Supply Voltage	2.5		6.0	V	
R_{KI} C_{KI}	Key Input (R1 - 4R, C1 - C3) Contact Resistance Keyboard Capacitance			1 30	kΩ pF	
K_{IL} K_{IH}	Key Input Level (R1 - R4, C1 - C3) 2-of-7 input mode and all electronic switching	V- 80% of V+		20% of V+ V+	V V	
K_{IRU}	Pull-Up		100		kΩ	
K_{IRD}	Pull-Down Input Resistance @ V_{IN} = 4.8V, V+ = 6.0V		100		kΩ	
I_M	Mute Sink Current @ V_O = 0.5V, V+ = 2.5V	500			μA	
I_P	Pulse Output Sink Current @ V_O = 0.5V, V+ = 2.5V	1.0			mA	
I_{MR}	Memory Retention Current		0.7		μA	7
Iop	Operating Current		100	150	μA	1
I_{LKG}	Mute or Pulse Off Leakage V+ = 6.0V V_O = 6.0V		 .001	 1	 μA	
I_{REF}	V_{REF} Output Source Current (V_{REF} = -6.0V REF to V+)	1	7		mA	8

Functions of the individual pins are described below:

V+ (Pin 1)

This is the positive supply pin. The voltage on this pin is measured relative to V- and is supplied from a 150μA current source. This voltage must be regulated to less than 6.0 volts.

V_{REF} (Pin 2)

The V_{REF} output provides a reference voltage that tracks internal paramters of the MK50992. V_{REF} provides a negative voltage reference to the V+ supply. Its magnitude will be approximately 0.6 volt greater than the minimum operating voltage of each particular MK50992.

The typical application would be to connect the V_{REF} pin to the V- pin (pin 6). The supply to the V+ pin (pin 1) should then be regulated to 150μA (Iop max). With this amount of supply current, operation of the MK50992 is guaranteed.

The internal circuit of the V_{REF} function is shown in Figure 1 with its associated I-V characteristic.

AC CHARACTERISTICS

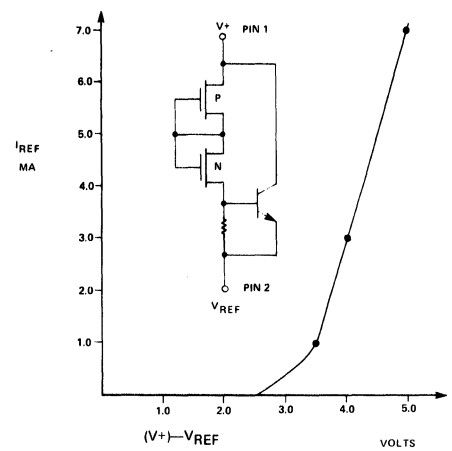
SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
F_{OSC}	Oscillator Frequency		4		kHz	4
t_{DB}	Key Input Debounce Time		10		ms	3,6
t_{KD}	Key Down Time for Valid Entry	40			ms	2,3
t_{KR}	Key Down Time During Two-Key Roll Over	5			ms	3
t_{OS}	Oscillator Start-Up Time (V+ = 2.5V)		1		ms	
t_{MO}	Mute Valid After Last Outpulse		5		ms	3,6
Pr	Pulse Output Pulse Rate		10		pps	5
t_{OH}	On-Hook Time Required to Clear Memory	300			ms	3
t_{PDP}	Pre-Digital Pause		800		ms	3,6
t_{IDP}	Inter-Digital Pause		800		ms	3,6
Δf	Frequency Stability (2.5V - 3.5V)		± 4		%	
Δf	Frequency Stability (3.5V - 6.0V)		± 4		%	
Δf	Frequency Stability (with V_{REF} used) (I_{REF} = 250μA - 500μA)		± 2.5		%	

NOTES:

1. Output and V_{REF} unloaded.
2. Debounce plus oscillator startup time ≤ 40ms.
3. These times are directly proportional to the oscillator frequency.
4. R_S = 2MΩ, R = 220KΩ, C = 390pF. See oscillator paragraph.
5. If pin 10 is tied to V+, the Pulse Output Pulse Rate will be 20pps.
6. If the 20pps option is selected, the time will be ½ these shown.
7. Current necessary for memory to be maintained. All outputs unloaded.
8. Refer to Figure 1

V_{REF} TYPICAL I-V CHARACTERISTICS

Figure 1



KEYBOARD INPUTS (Pins 3, 4, 5, 13, 14, 15, 16)

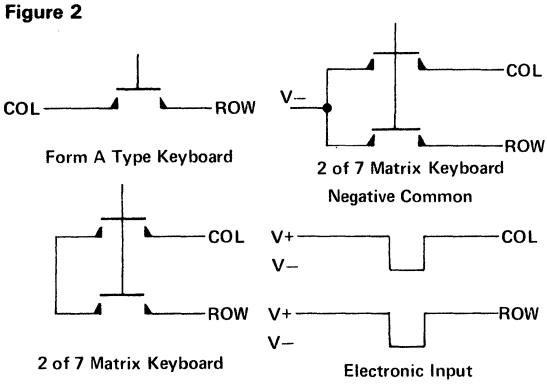
The MK50992 incorporates an innovative keyboard scheme that allows either the standard 2-of-7 keyboard with negative common or the inexpensive single contact (Form A) keyboard to be used.

A valid key entry is defined by either a single row being connected to a single column or V- being simultaneously presented to both a single row and column.

When in the On-Hook mode, the row and column inputs are held high and no keyboard inputs are accepted. When Off-Hook, the keyboard is completely static until the initial valid key input is sensed. The oscillator is then enabled and the rows and columns are alternately scanned (pulled high, then low) to verify the input is valid. The input must remain valid continuously for 10ms of debounce time to be accepted.

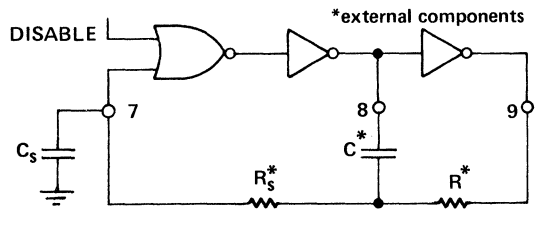
KEYBOARD CONFIGURATIONS

Figure 2



OSCILLATOR CONFIGURATION

Figure 3



OSCILLATOR (Pins 7, 8, 9)

The MK50992 contains on-chip inverters to provide an oscillator which will operate with a minimum of external components. Figure 3 shows the on-chip configuration with the necessary external components. Optimum stability occurs with the ratio $K = R_S/R$ equal to 10. The oscillator period is given by:

$$T=RC[1.386+(3.5KCs)/C-(2K/(K+1))\ln(K/(1.5K+0.5))]$$

where C_S is the stray capacitance on Pin 7. Accuracy and stability will be enhanced with this capacitance minimized.

V- (Pin 6)

This is the negative supply pin and is normally tied to V_{REF} (see V_{REF} paragraph).

20/10 PPS (Pin 10)

Tying this pin to V- will select an Output Pulse Rate of 10pps. Tying the pin to V+ will select an Output Pulse Rate of 20pps.

MAKE/BREAK (Pin 11)

The MAKE/BREAK pin controls the MAKE/BREAK ratio of the pulse output. The MAKE/BREAK ratio is controlled by connecting V+ or V- to this pin as shown in the following table.

MAKE/BREAK RATIO SELECTION

Table 1

INPUT TO MAKE/BREAK PIN	PULSE OUTPUT	
	MAKE	BREAK
V+ (Pin 1)	34%	66%
V- (Pin 6)	40%	60%

$\overline{\text{MUTE}}$ OUTPUT (Pin 12)

The $\overline{\text{Mute}}$ output is an open-drain N-channel transistor designed to drive an external bipolar transistor. This circuitry is usually used to mute the receiver during outpulsing.

As shown in Figure 4, the MK50992 $\overline{\text{Mute}}$ output turns on (pulls to the V- supply) at the beginning of the predigital pause and turns off (goes to an open circuit) following the last break. The delay from the end of the last break until the $\overline{\text{Mute}}$ output turns off is mute overlap and is specified as t_{MO}.

TEST/ON HOOK (Pin 17)

The "Test" or "On-Hook" input of the MK50992 has a 100kΩ pull-up to the positive supply. A V+ input or allowing the pin to float sets the circuit in its On-Hook or test mode while a V- input sets it in the Off-Hook or Normal Mode.

When Off-Hook, the MK50992 will accept key inputs and outpulse the digits in normal fashion. Upon completion of the last digit, the oscillator is disabled and the circuit stands by for additional inputs.

Switching the MK50992 to On-Hook while it is outpulsing causes the remaining digits to be outpulsed at 100 x the normal rate (M/B ratio is then 50/50). This feature provides a means of rapidly testing the device and is also an efficient method by which the circuitry is reset. When the outpulsing in this mode, which can take up to 300ms, is completed, the circuit is deactivated and will require only the current necessary to sustain the memory and Power-Up-Clear detect circuitry (refer to the electrical specifications).

Upon returning Off-Hook, a negative transistion on the Mute Output will insure the speech network is connected to the line. If the first key entry is either a * or #, the number sequence stored on-chip will be outpulsed. Any other valid key entries will clear the memory and outpulse the new number sequence.

$\overline{\text{PULSE}}$ OUTPUT (Pin 18)

The $\overline{\text{Pulse}}$ output is an open drain N-channel tranistor designed to drive an external bipolar transistor. These transistors would normally be used to pulse the telephone line by disconnecting and connecting the network.

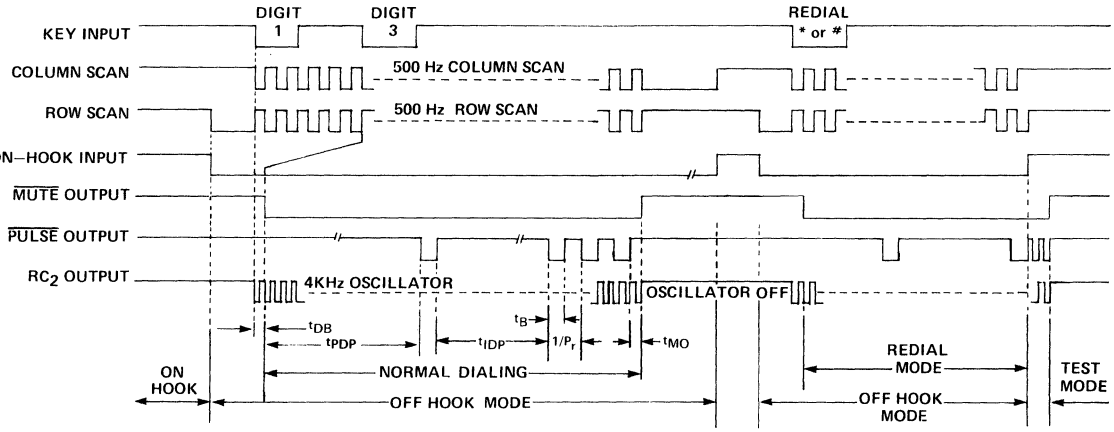
The MK50992 $\overline{\text{Pulse}}$ output is an open circuit during make and pulls to the V- supply during break.

As shown in Figure 4, outpulsing starts with a make before break.

A typical application is shown in Figure 6. This circuit will produce the timing shown in Figure 4.

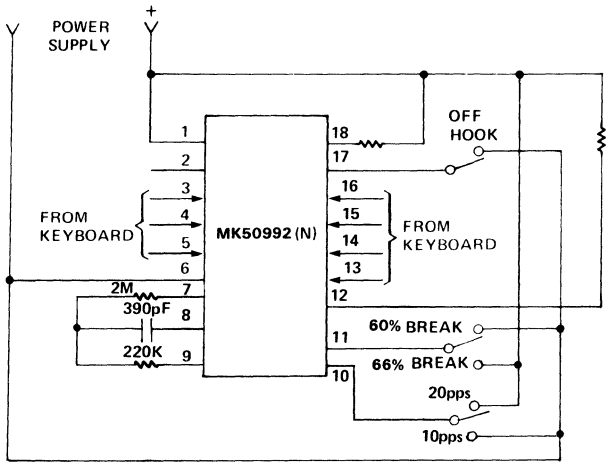
TIMING CHARACTERISTICS

Figure 4



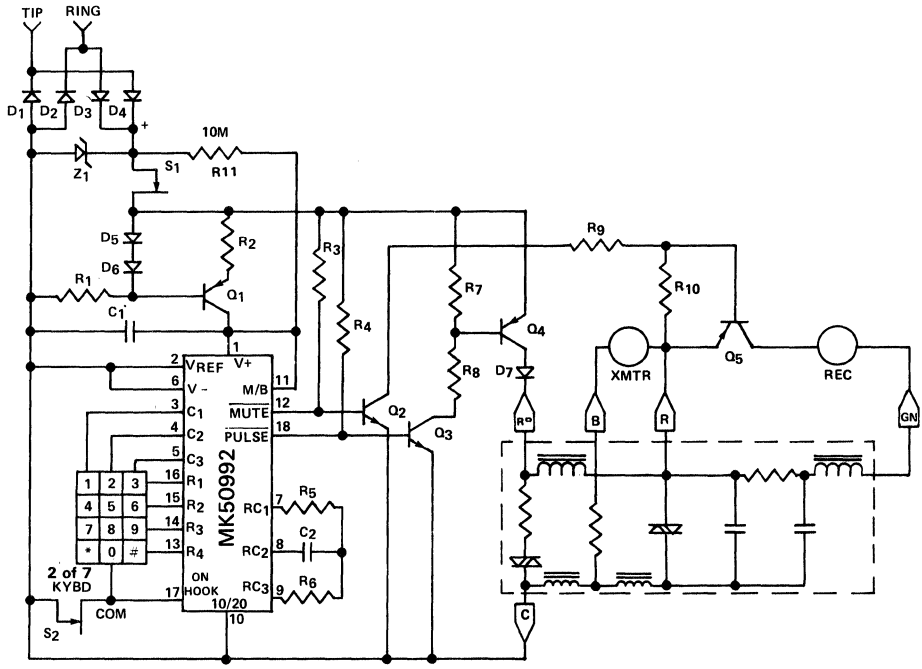
TEST CIRCUIT

Figure 5



TYPICAL APPLICATION

Figure 6



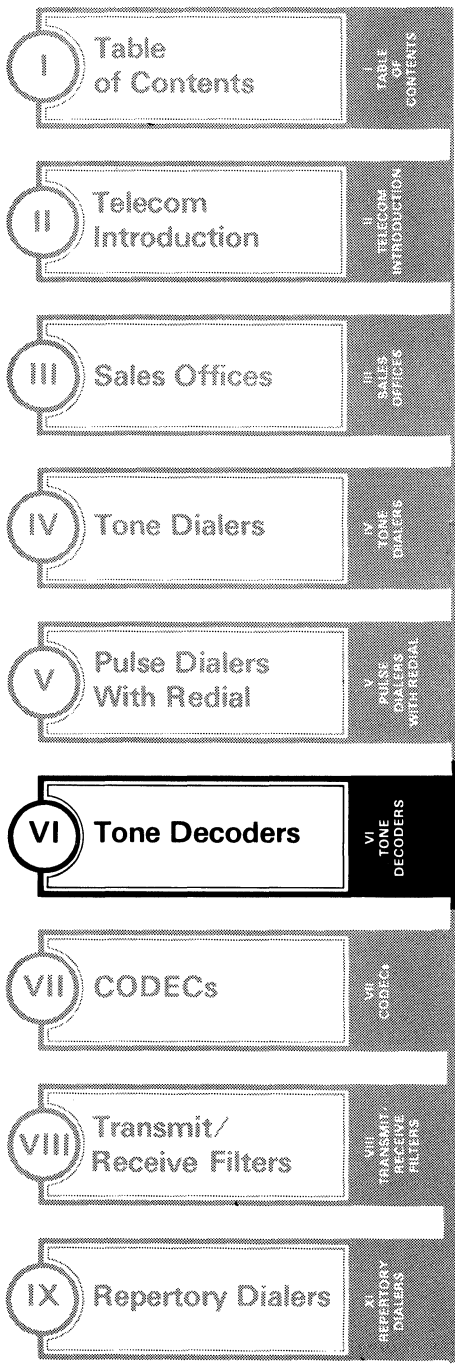
R1 = 560KΩ
R2 = 1.4KΩ
R3 = 470KΩ
R4 = 330KΩ
R5 = 2MΩ
R6 = 220KΩ

R7 = 100KΩ
R8 = 3KΩ
R9 = 3KΩ
R10 = 100KΩ
R11 = 10MΩ

Q1 = 2N5401
Q2 = 2N5550
Q3 = 2N5550
Q4 = 2N5401
Q5 = 2N5401

D1 = IN4004
D2 = IN4004
D3 = IN4004
D4 = IN4004
D5 = IN914
D6 = IN914
D7 = IN4004

C1 = 68μF
C2 = 390pF
S1 = HOOK SWITCH
S2 = HOOK SWITCH
Z1 = 120-volt, 1-watt zener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IX REPERTORY DIALERS

PRELIMINARY

MOSTEK®

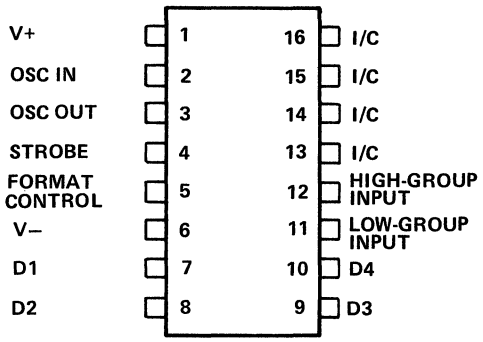
INTEGRATED TONE RECEIVER

MK5102(N)-5

FEATURES

- ☐ Detects all 16 standard DTMF digits
- ☐ Requires minimum external parts count for minimum system cost
- ☐ Uses inexpensive 3.579545 MHz crystal for reference
- ☐ Digital counter detection with period averaging insures minimum false response
- ☐ 16-pin package for high system density
- ☐ Single supply 5 Volts ± 10%
- ☐ Output in either 4-bit binary code or dual 2-bit row/column code
- ☐ Latched outputs

MK5102 PIN OUT



DESCRIPTION

The MK5102 is a monolithic integrated circuit fabricated using the complementary-symmetry MOS (CMOS) process. Using an inexpensive 3.579545 MHz television colorburst crystal for reference, the MK5102 detects and decodes the 8 standard DTMF frequencies used in telephone dialing. The requirement of only a single supply and its construction in a 16-pin package make the MK5102 ideal for applications requiring minimum size and external parts count.

The MK5102 detects the high and low group DTMF tones after band splitting using a digital counting method. The zero crossings of the incoming tones are counted over several periods and the results averaged over a longer period. When a minimum of 33 milliseconds of a valid DTMF digit is detected, the proper data is latched into the outputs and the output strobe goes high. When a valid digit is no longer detected, the strobe will return low and the data will remain latched into the outputs. Minimum interdigit time is 35 milliseconds.

The MK5102 is designed to interface with the MK5099 Integrated Pulse Dialer with only one additional DIP Package. These two parts working together form a DTMF-to-Pulse converter that meets the recognized telephone standards.

ABSOLUTE MAXIMUM RATINGS*

DC Supply Voltage V+ (Referenced to V–) ..... +6.0 Volts
Operating Temperature ..... 0°C to 70°C
Storage Temperature ..... –55°C to 100°C
Maximum Circuit Power Dissipation ..... 300 mW
Voltage on any pin, with respect to V– ..... –0.3 Volt
Voltage on any pin, with respect to V+ ..... +0.3 Volt

*Operation Above Absolute Maximum Ratings May Damage The Device

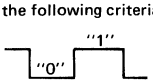
ELECTRICAL CHARACTERISTICS

$0° C \leq T_A \leq 70° C$ V– = 0 Volts

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage (V+)	(V– = 0)	4.5		5.5	Volts	
Lo Group & Hi Group Inputs	50% Duty Cycle Square Wave	0.9		V+	Volts Peak-to-Peak	1,2
STROBE D1, D2, D3, D4 OUTPUTS	"0" Level	0.0		0.4	Volt @ 1.6 mA	
	"1" Level	(V+)–1		V+	Volts @ 0.1 mA	
FORMAT CONTROL Input	"0" Level	0.0		0.5	Volt @ 700μA	
	"1" Level	(V+)–0.5		V+	Volt @ 700μA	
Frequency Detect Band Width		± 2.0	± 2.5	± 2.9	% of f_o	
Tone Coincidence Duration		33			ms	4
Interdigit Interval		35			ms	4
Signal to Noise Ratio		18			dB	3
Supply Current @ 5.5V	Inputs and Outputs Unloaded		5	10	mA	

NOTES:

1. Due to internal biasing, this input must be capacitively coupled with a low leakage .05 μF capacitor.
2. No coupling capacitor is needed if the DTMF square wave meets the following criteria:



   a. Logic "0" level = 1 Volt (max)
   b. Logic "1" level = 4 Volts (min)

3. Signal-To-Noise Ratio is defined as:
   $SN = 20 \log \frac{SA}{NA}$
   where SA = RMS Amplitude of single tone being detected.
   NA = RMS white noise in the band from 300Hz to 3.4KHz.
4. Tone coincidence duration and interdigit interval measured at High- and Low-group inputs. Filter and/or limiter or comparator characteristics will affect the overall detect time.

OSCILLATOR

The MK5102 contains an on-board inverter with sufficient gain to provide oscillation when working with a low cost television "color burst" crystal. The inverter input is OSC IN (pin 2) and output is OSC OUT (pin 3). The circuit is designed to work with a crystal cut to 3.579545 MHz to give detection of the standard DTMF frequencies.

FORMAT CONTROL (PIN 5)

The Control pin is used to control the output format of Pins D1 through D4. This three-state input selects a 4-Bit Binary Code, a Dual 2-Bit Row/Column code. or high-impedance output for use with bus-structured circuitry. This three-state input is controlled as follows:

FORMAT CONTROL INPUT	OUTPUT DATA FORMAT
V–	High Impedance
V+	4-Bit Binary
Floating	Dual 2-Bit Row/Column

FORMAT CONTROL (continued)

The following table describes the two output codes.

Table 1

	4-Bit Binary				Dual 2-Bit Row/Column			
					Row		Column	
Digit	D1	D2	D3	D4	D1	D2	D3	D4
1	0	0	0	1	0	1	0	1
2	0	0	1	0	0	1	1	0
3	0	0	1	1	0	1	1	1
4	0	1	0	0	1	0	0	1
5	0	1	0	1	1	0	1	0
6	0	1	1	0	1	0	1	1
7	0	1	1	1	1	1	0	1
8	1	0	0	0	1	1	1	0
9	1	0	0	1	1	1	1	1
0	1	0	1	0	0	0	1	0
*	1	0	1	1	0	0	0	1
#	1	1	0	0	0	0	1	1
A	1	1	0	1	0	1	0	0
B	1	1	1	0	1	0	0	0
C	1	1	1	1	1	1	0	0
D	0	0	0	0	0	0	0	0

Figure 1 shows the relationship between the data output code shown in Table 1 and the standard DTMF keyboard.

DTMF DIALING MATRIX

Figure 1

	Col 1	Col 2	Col 3	Col 4
Row 1	1	2	3	A
Row 2	4	5	6	B
Row 3	7	8	9	C
Row 4	*	0	#	D

Note: Column 4 is for special applications and is not normally used in telephone dialing.

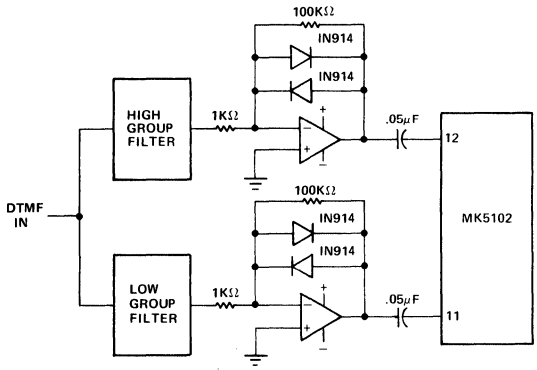
DETECTION FREQUENCY

Table 2

Low Group f_o	High Group f_o
Row 1 = 697 Hz	Column 1 = 1209 Hz
Row 2 = 770 Hz	Column 2 = 1336 Hz
Row 3 = 852 Hz	Column 3 = 1477 Hz
Row 4 = 941 Hz	Column 4 = 1633 Hz

SUGGESTED INPUT LIMITER CIRCUIT

Figure 2



OUTPUTS D1 THRU D4 (PINS 7 THRU 10)

Outputs D1 thru D4 are CMOS push-pull when enabled and open-circuited (high impedance) when disabled by the format control pin.

D1 thru D4 are the data out lines. The output data can be in two formats as described in the section about the format control pin (pin 5).

The Dual 2-Bit Row/Column code decodes with D1 and D2 indicating the row selected, and D3 and D4 indicating the column selected.

The two output codes allow the user to obtain either 1-of-16 or 2-of-8 output data by using only a single additional package.

I/C (PINS 13 THRU 16)

Pins 13 thru 16 are internally connected and are intended to be left floating.

STROBE (Pin 4)

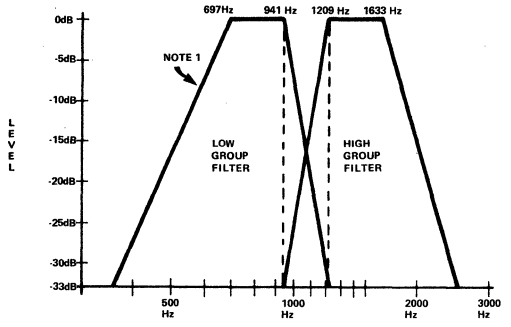
The STROBE output goes to a "1" when 33 miliseconds of a valid DTMF signal is detected and remains at a "1" until an interdigit interval has been detected. The data at D1-D4 are already valid when STROBE goes to a "1" and will remain unchanged until the next DTMF digit is detected.

LOW-GROUP INPUT (Pin 11) and HIGH-GROUP INPUT (Pin 12)

The low- and high-group inputs are comparators that can detect capacitively-coupled square-wave signals as small as 0.9 volts peak-to-peak. The circuitry driving these inputs would typically use back-to-back silicon diodes as symmetrical limiters to regulate this level.

These inputs are biased to the midpoint of the supply with a resistive divider. Nominal input impedience is 100K Ω.

INPUT BAND SPLIT REQUIREMENTS



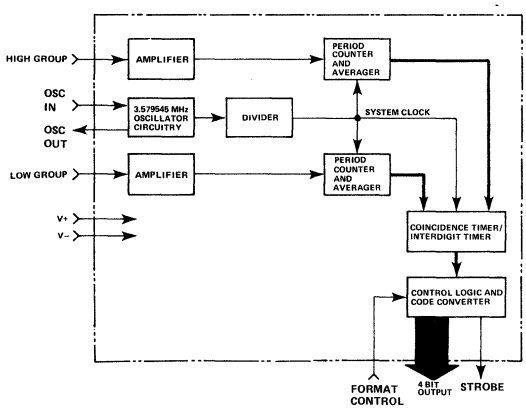
RELATIVE INPUT LEVEL VS FREQUENCY

NOTES:

1. Dial tone notch filter adequate to maintain S/N ratio of $\geqslant$ 18dB in above pass bands.

2. Filter response described above will normally result in operation to 6dB of twist with 18dB S/N.

MK5102 BLOCK DIAGRAM



MOSTEK®

DESIGN CONSIDERATIONS FOR A DTMF RECEIVER SYSTEM

Application Note

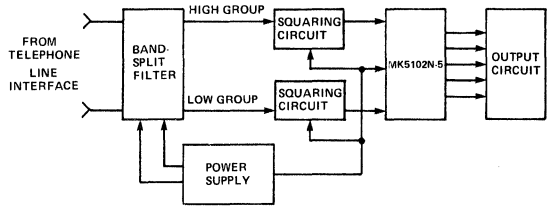
This application note will describe all of the requirements for building a high-quality DTMF receiver using the MK5102N-5 and hybrid filters. The following topics will be discussed:

1. Power supply requirements
2. Band separation filter requirements
3. Squaring circuit requirements
4. Squaring circuit-to-decoder coupling requirements
5. Receiver testing
6. Output formatting
7. Other system considerations

Since the MK5102N-5 is intended to be a portion of a tone receiver SYSTEM, SYSTEM requirements must be met before a satisfactory decoder can be constructed. A block diagram of a typical system is shown in Figure 1. Each portion of the block diagram is discussed in succeeding paragraphs.

TYPICAL DTMF RECEIVER

Figure 1



POWER SUPPLY REQUIREMENTS

For proper operation of the MK5102N-5, the V+ power supply must be between 4.5 VDC and 5.5 VDC, with V- grounded. A power supply decoupling capacitor (typically .1uF) should be connected between V+ and V- to insure that no high-frequency noise is present on the V+ supply. Typically, a 1-volt peak-to-peak signal may be applied to V+ and the MK5102N-5 will function properly.

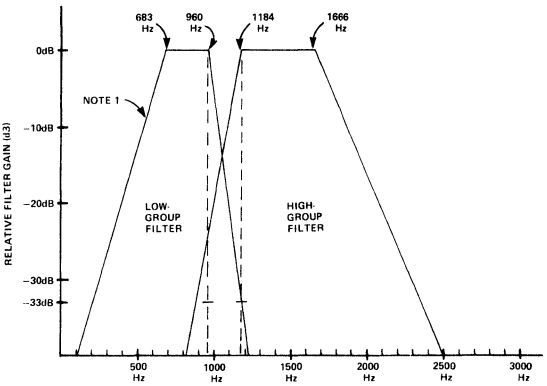
FILTER REQUIREMENTS

For proper operation of the MK5102N-5, an external band separation filter must be provided to split the DTMF signal into its high-group and low-group components. However, the band separation requirements are not as stringent for the MK5102N-5 as they are for competing designs. As shown in figure 2, the MK5102N-5 requires a band separation of only 33dB in an average application. The 33dB requirement allows for a S/N ratio of 18dB, 6dB of twist, and a detection bandwidth of at least ± 2%. A reduction of twist margin or S/N requirements will result in a corresponding lower requirement for band separation. For example, if there is not a requirement for twist margin, the band separation can be reduced to 27dB. In a system with no noise and no twist, the band separation can be 22dB.

The plot shown in Figure 2 depicts corner frequencies of 683Hz, 960Hz, 1184Hz and 1666Hz. These represent a 2% deviation from the DTMF frequencies of 697Hz, 941Hz, 1209Hz and 1633Hz, respectively. This deviation is necessary because of the requirement that a DTMF receiver must detect frequencies which are 2% higher or lower than the nominal DTMF frequency. Table 1 lists the 8 DTMF frequencies and the corresponding frequencies which a DTMF decoder is required to detect.

BAND SEPARATION FILTER REQUIREMENTS

Figure 2



NOTES:

1. Dial tone notch filter must maintain S/N ratio ≥ 18dB
2. Filter response shown will allow operation to 6dB of twist with 18dB S/N.

TABLE I

8 STANDARD DTMF FREQUENCIES AND CORRESPONDING UPPER AND LOWER REQUIRED DETECTION FREQUENCIES

DTMF FREQUENCY (HZ)	LOWER DETECTION FREQUENCY LIMIT (HZ)	UPPER DETECTION FREQUENCY LIMIT (HZ)
697	683	711
770	755	786
852	834	869
941	922	960
1209	1184	1233
1336	1309	1363
1477	1447	1507
1633	1600	1666

DETECTION ALGORITHM

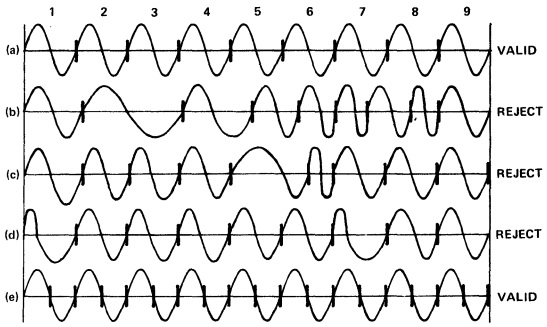
The detection approach used in the MK5102N-5 utilizes zero-crossing detection and digital period-counting. To increase the rejection of random noise and the residue from out-of-band components, an averaging scheme is used. Figure 3(a) shows nine cycles of a symmetrical sine wave. If zero-crossings were the only detection criteria, and if the average period-count obtained over nine periods were acceptable, then the signal in Figure 3(a) represents a valid tone. The jitter of the zero-crossings is integrated out by the nine-period average. However, based on the simple nine-period average, the signal shown in Figure 3(b) would be accepted as a valid tone. To improve rejection of this speech-type waveform, the nine-period detection time can be broken into three period-averaged sub-groups as indicated by the dashed lines in Figure 3(b). By combining the nine-period average and the sub-group average criteria, 200 false hits are obtained on 30 minutes of a standard speech tape. Figure 3(c) represents a type of waveform that would produce a hit based on the nine-period and sub-group average algorithm. To improve rejection of this waveform, requirements must be placed on every single period in addition to the nine-period average and the sub-group average. However, the waveform of Figure 3(d) will be detected using only these three criteria. Therefore an additional requirement must be placed on each half-period of the waveform. Figure 3(e) shows the only type of signal which will be accepted by a detection algorithm which requires the following:

1. Valid nine-period average
2. Three valid sub-group averages
3. Valid single-period
4. Valid half-period

Using these four criteria, the number of hits on a standard speech tape can be reduced to less than six.

POSSIBLE INPUT WAVEFORMS

Figure 3

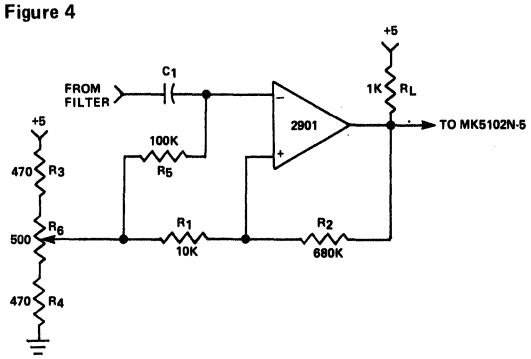


INPUT SQUARING CIRCUITS

As described above, to minimize the number of false hits, a detection algorithm must place stringent requirements on each half-period of the input waveform (high group or low group). To successfully meet these requirements, the duty cycle of the input waveform must be between 49% and 51%. The input squaring circuit must therefore provide an output which accurately tracks the input without adversely affecting the duty cycle. Such a circuit, an inverting comparator with hysteresis, is illustrated in Figure 4.

INPUT SQUARING CIRCUIT

Figure 4



C_1 is used to ac couple the filter output to the squaring circuit so that DC bias present at the filter output will not affect the performance of the squaring circuit. R_3, R_4, and R_6 establish a bias level at about 2.5 Volts, and R_5 is used to provide the same bias level at the inverting input of the comparator used in the squaring circuit. The maximum input bias current for the LM2901 is 500nA, so the DC bias level at the inverting input is effectively the same as the voltage at the wiper of R_6. R_6 must be adjusted so that, for an input signal level of -28dBm, the output duty cycle will be 50%. This adjustment compensates for

the input offset voltage of the LM2901. R_L is the pullup resistor for the open-collector output of the comparator. R_1 and R_2 set the hysteresis level. Their values are determined by the following approximate relationships:

$$V_{UT} = 2.5 + \frac{(2.5)(R_1)}{(R_1 + R_2 + R_L)}$$

where V_{UT} is the upper threshold

$$V_{LT} = \frac{(2.5 - V_{OL})(R_2)}{(R_1 + R_2)}$$

where V_{LT} is the lower threshold and V_{OL} is the output saturation voltage

In both cases, any variation due to the current in R_5 is ignored.

For central office applications, the tone receiver system must operate over an input signal level range of -26dBm to +6dBm. The squaring circuit, therefore, must respond to signal levels of -26dBm or greater but is not required to respond to lower signal levels.

To allow for signal attenuation through the band separation filter, the squaring circuit should be set to respond to signal levels of -28dBm or greater. The -28dBm cutoff point corresponds to a peak-to-peak voltage of 87.1mV. For a 50% duty-cycle output waveform, V_{UT} should be set 43.5mV above and V_{LT} should be set 43.5mV below the DC bias point. The passive components for the squaring circuit are then selected as follows:

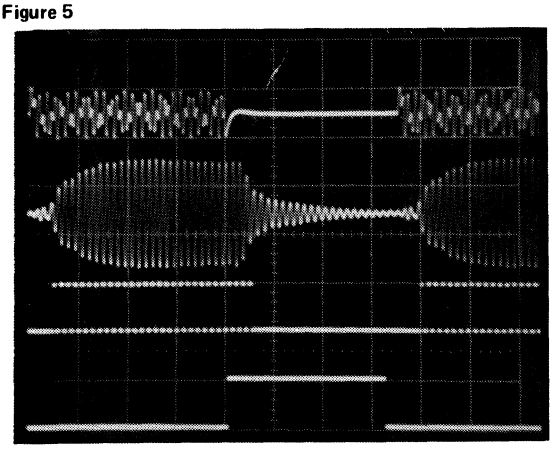
$R_L = 1k\Omega$	Chosen value.
$R_2 = 680k\Omega$	Chosen value.
$R_1 = 12k\Omega$	Calculated value.
$R_3 = R_4 = 470\Omega$	Chosen value for DC bias.
$R_5 = 100k\Omega$	Chosen value. Tradeoff effect on DC bias vs. drop across R_5 due to 2901 input bias current.
$C_1 = 1\mu F$	Chosen value. Must be low impedance over frequency range of 683Hz to 1666Hz.

To achieve proper operation at low signal levels, R_1 must be 10kΩ. The discrepancy between the calculated value and the actual required value results from component tolerances.

Since many commercially-available filters exhibit a ringing characteristic at their output, as shown in Figure 5 and Figure 6, additional circuitry is required to detect the beginning of ringing and squelch the output of the squaring circuit. The required circuitry, an envelope detector, is shown in Figure 7. The detector consists of two precision rectifiers, two sample-and-hold circuits, and a comparator. C_3 is used to couple the low-group filter output to the envelope detector. Z1a, D_1, C_1, R_2, and R_3 then rectify the incoming signal and store a peak value. The $R_2/R_3/C_1$ time constant is set for 20ms so that the voltage at the inverting input of Z_2 will represent ½ the peak value of the incoming signal. Z1b, D_2, R_1 and C_2 also rectify the incoming signal and store a peak value, but the time constant is set for 1.4ms so that the voltage at the non-inverting input of Z_2 will represent the instantaneous peak value of the incoming waveform. As long as the instantaneous value is greater than ½ of the peak value, the comparator output will be high. However, as soon as the instantaneous value decreases to less than ½ the peak value (this will occur as ringing begins), the comparator output will go low and inhibit the output of the squaring circuit. It is necessary to provide only one envelope detector since the MK5102N-5 will treat the absence of a valid low-group/high-group tone combination as interdigit time.

LOW-GROUP FILTER RESPONSE (3044)

Figure 5



DTMF INPUT TO FILTER (5V/DIV.)

LOW-GROUP FILTER OUTPUT (IV/DIV.)

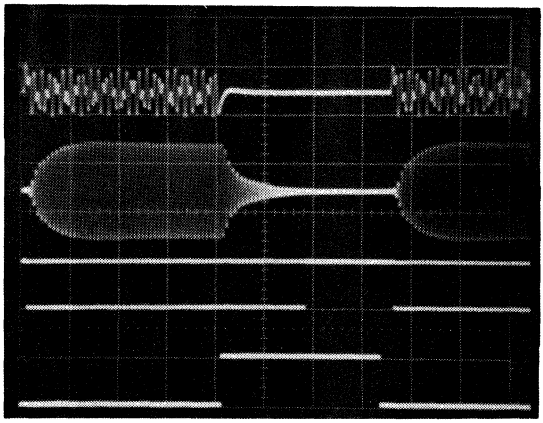
SQUARING CIRCUIT OUTPUT (5V/DIV.)

STROBE FROM MK5102N-5 (5V/DIV.)

EACH TIME DIVISION = 10 MS

HIGH–GROUP FILTER RESPONSE (3045)

Figure 6



EACH TIME DIVISION = 10 ms

DTMF INPUT TO FILTER (5V/DIV.)

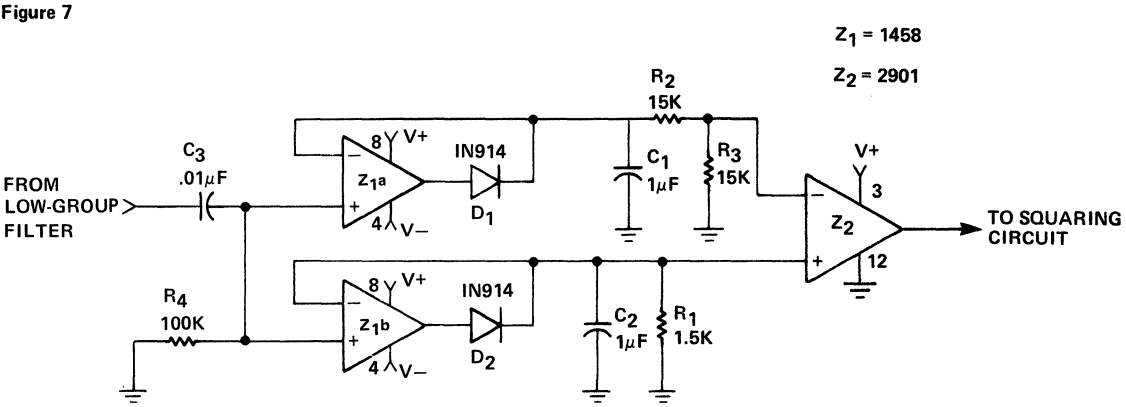
LOW-GROUP
FILTER OUTPUT (IV/DIV.)

SQUARING CIRCUIT
OUTPUT (5V/DIV.)

STROBE FROM MK5102N-5
(5V/DIV.)

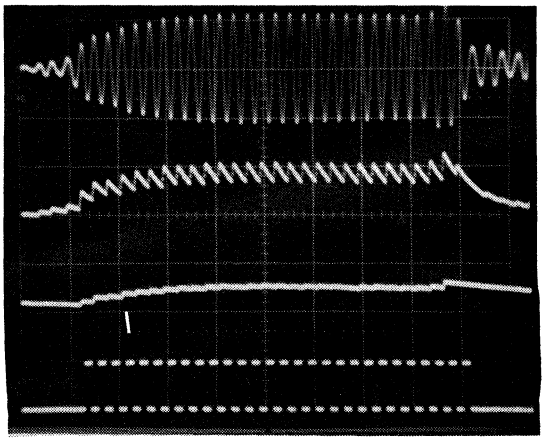
ENVELOPE DECAY DETECTOR

Figure 7



ENVELOPE DETECTOR OPERATION

Figure 8



LOW-GROUP
FILTER OUTPUT (IV/DIV.)

INSTANTANEOUS PEAK
DETECTOR (IV/DIV.)

AVERAGE PEAK
DETECTOR (IV/DIV.)

LOW-GROUP INPUT
TO 5102N-5 (5V/DIV.)

SQUARING CIRCUIT-TO-DECODER COUPLING

The output of the squaring circuit may be tied directly to the MK5102N-5 if it meets the following requirements:

Logic 1 ≥ 4 volts
Logic 0 ≤ 1 volt

A squaring circuit with an output that does not meet these requirements must be capacitively coupled to the MK5102N-5 with a 0.05μF capacitor. The value of the coupling capacitor is critical because of the impedance of the bias circuit at the high-group or low-group input. As shown in Figure 9, the sudden appearance of a tone burst causes the DC bias point to shift upward. Until the DC bias returns to its normal level, the input comparator will not switch and the input signal will be ignored, causing an increase in the dual-tone detection time. Using a 0.05μF capacitor will minimize the effect of this DC level shift. The peak-to-peak value of the coupled signal must be greater than .9 volts but less than V+ volts.

OUTPUT SIGNALS

D1, D2, D3, and D4 are the data output lines. The output format present on these pins is determined by the format control (pin 5) as shown in Table 2.

FORMAT CONTROL FUNCTIONS
TABLE 2

Format Control Input	Data Output Format
V–	High Impedance
V+	4-Bit Binary
Floating	Dual 2-Bit Row/Column

SHIFT IN DC BIAS LEVEL CAUSED BY APPLICATION OF TONE BURST
Figure 9

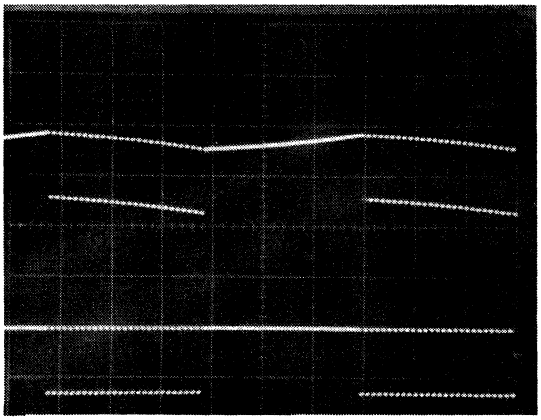


Table 3 describes the two output codes available.

TABLE 3

OUTPUT FORMAT

			4-Bit Binary				Dual 2-Bit Row/Column			
							Row		Column	
Key	Row	Col.	D1	D2	D3	D4	D1	D2	D3	D4
1	1	1	0	0	0	1	0	1	0	1
2	1	2	0	0	1	0	0	1	1	0
3	1	3	0	0	1	1	0	1	1	1
4	2	1	0	1	0	0	1	0	0	1
5	2	2	0	1	0	1	1	0	1	0
6	2	3	0	1	1	0	1	0	1	1
7	3	1	0	1	1	1	1	1	0	1
8	3	2	1	0	0	0	1	1	1	0
9	3	3	1	0	0	1	1	1	1	1
0	4	2	1	0	1	0	0	0	1	0
*	4	1	1	0	1	1	0	0	0	1
#	4	3	1	1	0	0	0	0	1	1
A	1	4	1	1	0	1	0	1	0	0
B	2	4	1	1	1	0	1	0	0	0
C	3	4	1	1	1	1	1	1	0	0
D	4	4	0	0	0	0	0	0	0	0

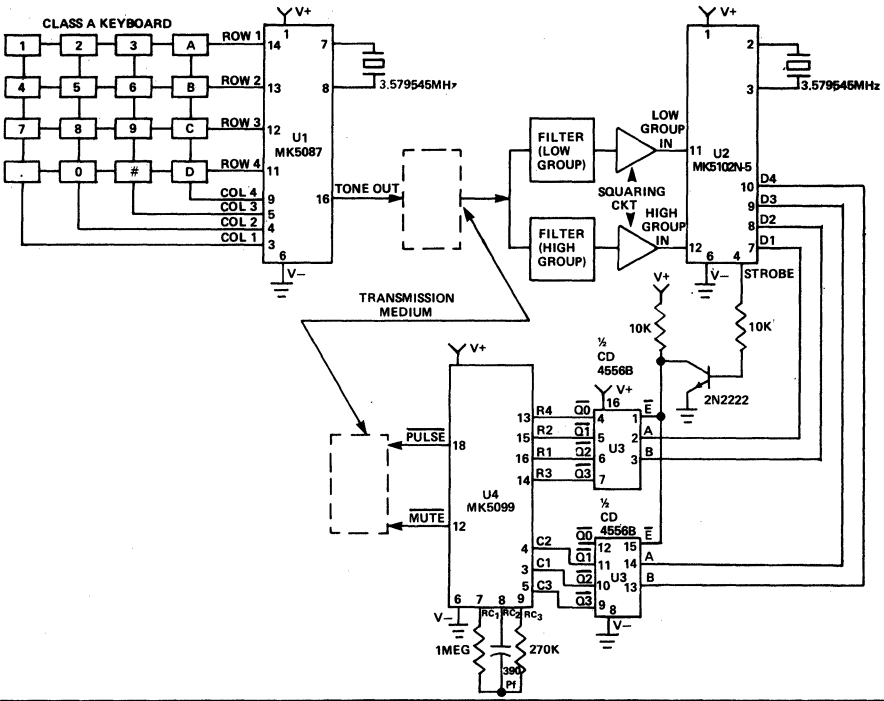
When all detection criteria are present, the MK-5102N-5 will latch the proper data into its outputs and strobe will go high. After an interdigit time has been detected, strobe will go low, but the data will remain on D1 through D4.

The dual 2-bit row/column code is useful when interfacing a key-to-pulse converter, as shown in Figure 10. On this circuit, the MK5102N-5, CD4556 and MK 5099 combine to form a tone-to-pulse converter, which allows the use of DTMF telephones in rotary exchanges. The DTMF tones are detected by the MK 5102N-5, which then generates the corresponding row/column code. Each CD4556 then uses this 2-bit code to select 1 of 4 active-low outputs. The MK5099 then interprets these signals as a valid key closure and generates a corresponding series of pulses.

For simple remote-control applications, the circuit of Figure 11 is useful. After a valid tone is detected, strobe will go high and one of the 16 outputs on the binary-to-1-of-16 encoder will go true. Thus, a DTMF transmitter and 16-key keyboard can be used to control 1 of 16 functions in a DTMF receiver. Each control pulse will have its width controlled by Strobe.

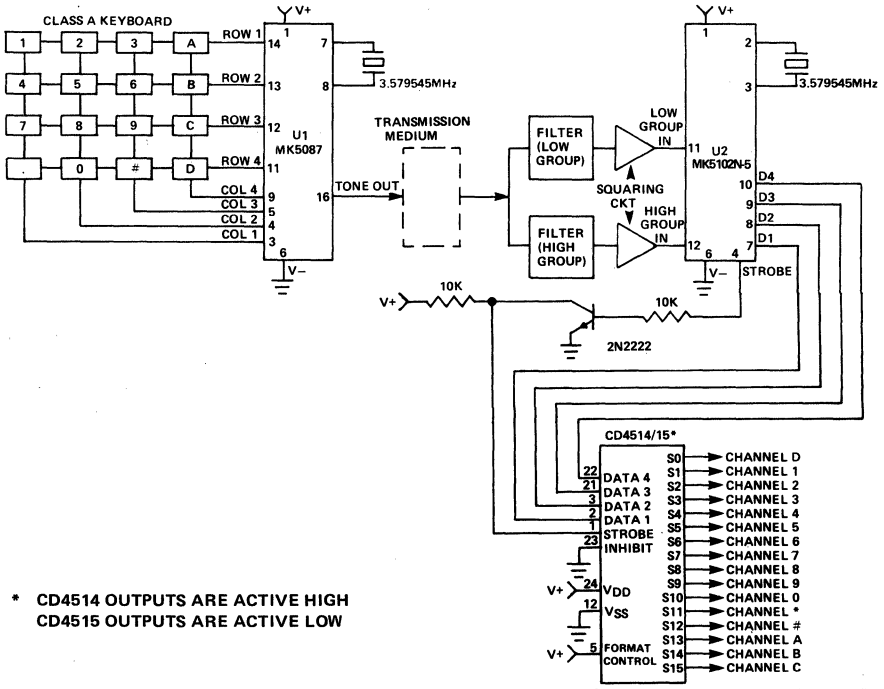
TONE-TO-PULSE CONVERTER

Figure 10



16-CHANNEL REMOTE CONTROL

Figure 11



* CD4514 OUTPUTS ARE ACTIVE HIGH
CD4515 OUTPUTS ARE ACTIVE LOW

RECEIVER TESTING

Equipment connections for testing a DTMF receiver are shown in Figure 12. The setup consists of a cassette player (ideally with a speed adjustment), a digital frequency counter, and a voltmeter. A Mitel CM7290 Tone Receiver Test Cassette was used in all the receiver tests described below. This cassette checks receiver detection bandwidth, maximum acceptable amplitude ratio (twist), receiver guard time, dynamic range and acceptable signal-to-noise ratio. It also evaluates the receiver talk-off rate with a condensed speech recording equivalent to many hours of receiver exposure. The CM7290 is available from Mitel at the locations listed.

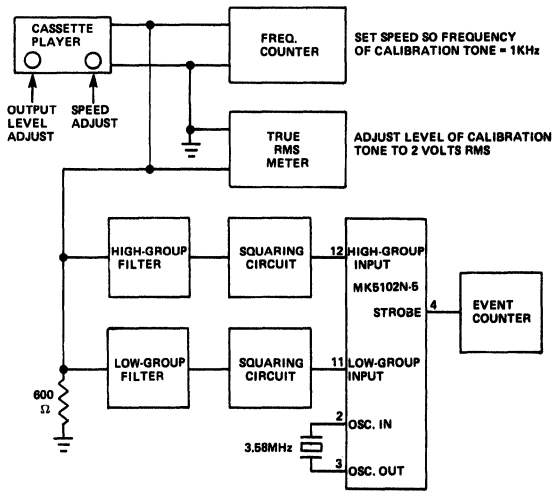
Mitel International
Shannon Industrial Estate
Shannon, Ireland
Telephone: 061-61433
Telex: 32208

Mitel Corp.
P.O. Box 13089 Kanata
Ottawa, Ontario, Canada
K2K1X3
Telephone: 613-592-2122
Telex: 053-4596
Cable Mitelcan
Twx: 610-562-8529

Mitel Inc.
St. Lawrence Industrial Park
Ogdensburg, New York 13669
Telephone: 315-393-1212
Twx: 510-259-4071

EQUIPMENT CONNECTIONS FOR RECEIVER EVALUATION

Figure 12



There are several considerations in setting up a receiver test. First, the recorder should have a speed adjustment and an output level adjustment. Each side of the CM7290 contains a 1kHz calibration tone. To set up properly for the test, the speed of the recorder should be adjusted so that the tone frequency is 1kHz and the cassette player output level should be adjusted to 2 volts RMS. The cassette player must be able to provide the 2-volt output level without clipping. If a speed adjustment is not available, printed instructions included with the CM7290 provide a formula for correcting some of the test results. Second, the strobe output of the MK5102N-5 should be tied to the input of the event counter and the counter's sensitivity input adjusted so as to prevent false triggering. This can easily be done by repeating test 2a on the CM7290 until consistent results are obtained. Third, any sources of environmental noise (electric motors, speed controls, etc) should be eliminated so that they will not introduce count errors on the event counter.

FILTER EVALUATION

Two commercially-available filters, the CH1295 and CH1296 from Cermetek and the 3044 and 3045 from ITT North Electric Microsystems, were evaluated. The addresses of these two filter vendors are listed below:

Cermetek, Inc.
660 National Avenue
Mt. View, CA 94043
Telephone: 415-969-9433
Twx: 910-379-6931

ITT North Microsystems Division
700 Hillsboro Plaza
Deerfield Beach, FL 33441
Telephone: 305-421-8450
Twx: 510-953-7523

Figure 13 and Table 5 show the test circuit and test results for the Cermetek filters. The test circuit and test results for the North Electric filters are shown in Figure 13 and Table 4. The tests were performed using the equipment setup shown in Figure 12. Figures 14 through 17 show the spectral response of the filters.

TEST CIRCUIT FOR CERMETEK AND NORTH ELECTRIC FILTERS

Figure 13

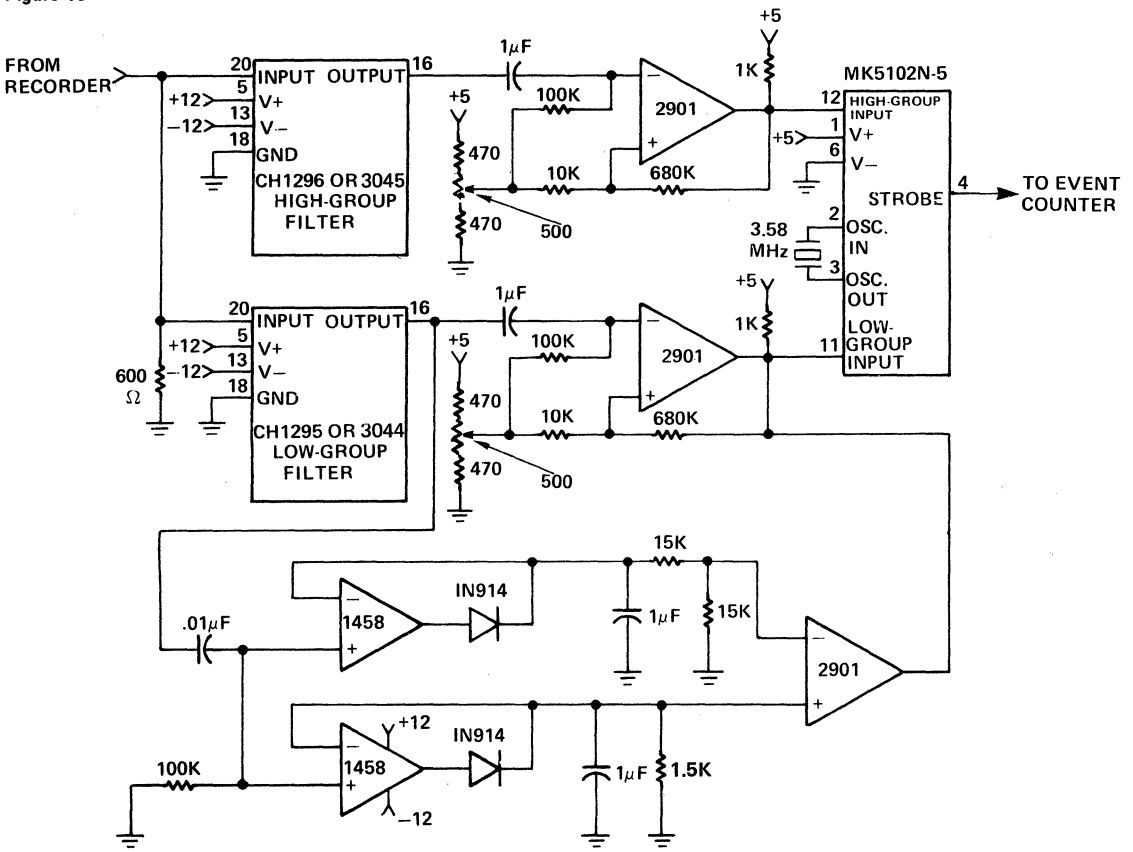


TABLE 4
MITEL TAPE TEST RESULTS FOR NORTH ELECTRIC FILTERS

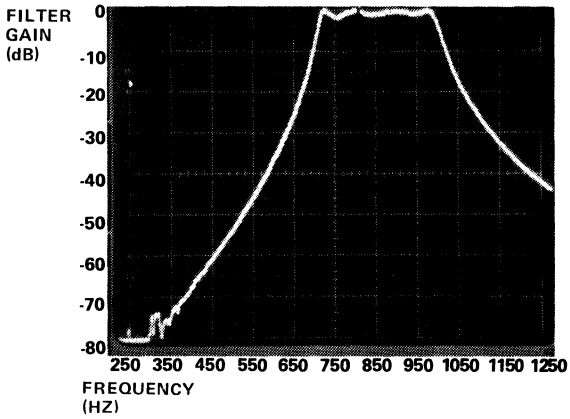
TEST#	RESULTS
2a, b	BW = 4.7 % of fo
2c, d	BW = 5.2 % of fo
2e, f	BW = 5.1 % of fo
2g, h	BW = 5.1 % of fo
2i, j	BW = 5.1 % of fo
2k, l	BW = 4.9 % of fo
2m, n	BW = 5.5 % of fo
2o, p	BW = 5.0 % of fo
3	159 decodes
4	Acceptable Amplitude Ratio = 13.1dB
5	Dynamic Range = 31.33 dB
6	Guard Time = 34.23 ms
7	99.8 % Successful Decode at N/S Ratio of -12dbV
8	3 Hits on Talk-Off Test

TABLE 5
MITEL TAPE TEST RESULTS FOR CERMETEK FILTERS

TEST#	RESULTS
2a, b	BW = 5.6 % of fo
2c, d	BW = 5.7 % of fo
2e, f	BW = 5.0 % of fo
2g, h	BW = 5.3 % of fo
2i, j	BW = 5.2 % of fo
2k, l	BW = 5.0 % of fo
2m, n	BW = 5.5 % of fo
2o, p	BW = 5.0 % of fo
3	158 decodes
4	Acceptable Amplitude Ratio = 12.6dB
5	Dynamic Range = 31.67 dB
6	Guard Time = 33.4 ms
7	98.33 % Successful Decode at N/S Ratio of -12dbV
8	3 Hits on Talk-Off Test

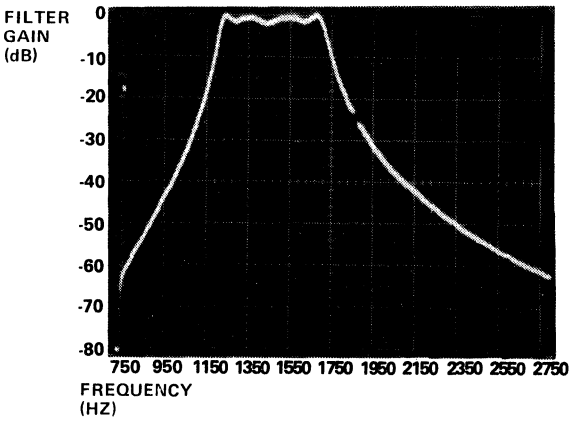
SPECTRAL RESPONSE OF CH1295 LOW-GROUP FILTER

Figure 14



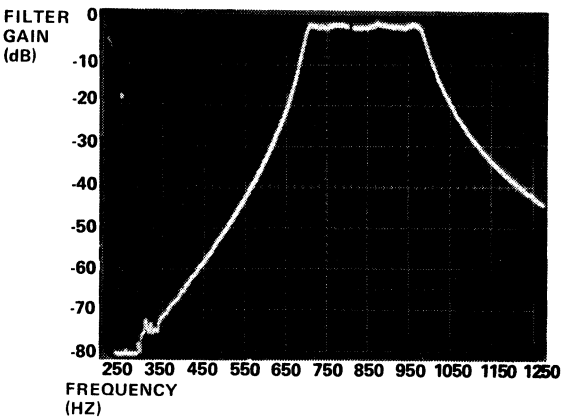
SPECTRAL RESPONSE OF CH1296 HIGH-GROUP FILTER

Figure 15



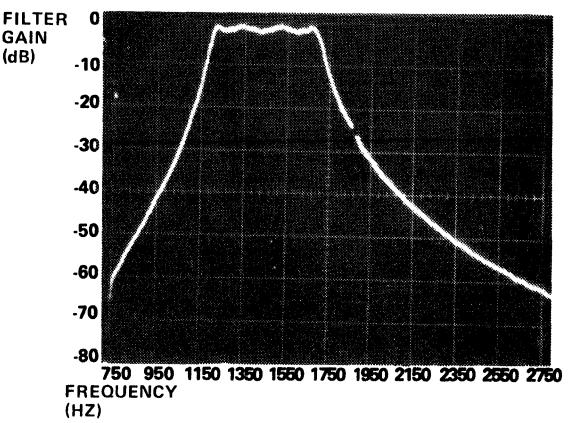
SPECTRAL RESPONSE OF 3044 LOW-GROUP FILTER

Figure 16



SPECTRAL RESPONSE OF 3045 HIGH-GROUP FILTER

Figure 17



OTHER SYSTEM CONSIDERATIONS

System noise will affect the operation of the MK5102N-5 by causing the detection bandwidth to shrink. The instantaneous value of the low-group or high-group waveform is represented by the following approximate relationship, $a = a_T \sin w_T t + a_N \sin w_N t$, where a is the instantaneous amplitude of the overall waveform, a_T is the amplitude of the high-group or low-group component, and a_N is the amplitude of the noise. If the highly-simplified noise term ($a_N \sin w_N t$) were removed, then the remaining term would represent a pure sine wave and the zero crossings of the waveform would be repeatable from cycle to cycle. All detection criteria would be present and the DTMF tone would be detected within a ± 2.0% to ± 2.9% bandwidth. However, adding the noise term introduces instantaneous amplitude variations which will effectively alter the duty cycle of the sine wave by causing the zero crossing points to jitter. If 0.5% jitter is caused by system noise, detection bandwidth will be decreased by .5%. Therefore, as the system noise level increases, the detection bandwidth will decrease.

As noted in the Filter Requirements paragraph, the 33dB band separation requirement allows for a S/N ratio of 18dB, with 6dB of twist, which means that the algorithm in the MK5102N-5 has been set up to provide a ± 2% minimum detection bandwidth in the presence of noise which is 18dB below the signal level and in the presence of high-group and low-group signals with an amplitude difference of 6dB.

SUMMARY

The MK5102N-5 provides a high-performance solution for DTMF detection at a lower cost than competing approaches. Band separation requirements for the MK5102N-5 are not as stringent as for competing designs, and, as was seen in the test results of Table 4 and Table 5, the MK5102N-5 provides excellent talk-off rejection. When used in conjunction with either the Cermetek or the North Electric filters, the MK5102N-5 will give the user a high-quality DTMF receiver which may be used in myriad applications.

PRELIMINARY

MOSTEK®

INTEGRATED TONE DECODER

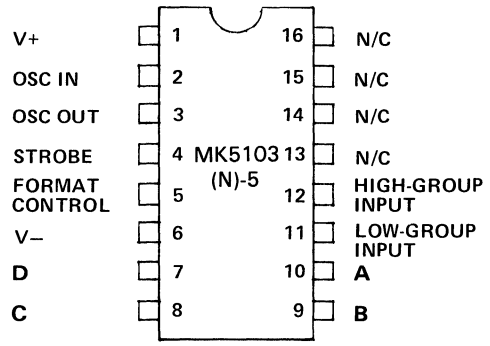
MK5103(N)-5

FEATURES

- Detects all 16 standard DTMF digits
- Requires minimum external parts count for minimum system cost
- Uses inexpensive 3.579545 MHz crystal for reference
- Digital counter detection with period averaging insures minimum false response
- 16-pin package for high system density
- Single supply: 5 volts ±10%
- Output in either 4-bit binary code or dual 2-bit row/column code
- Will operate at 14dB S/N ratio under worst-case signal conditions
- Latched outputs

PIN CONNECTIONS

Figure 1



DESCRIPTION

The MK5103 is a monolithic integrated circuit fabricated using the complementary-symmetry MOS (CMOS) process. Using an inexpensive 3.579545 MHz television color-burst crystal for reference, the MK5103 detects and decodes the 8 standard DTMF frequencies used in telephone dialing. The requirement of only a single supply and its construction in a 16-pin package make the MK5103 ideal for applications requiring minimum size and external parts count.

The MK5103 detects the high- and low-group DTMF tones after band splitting using a digital counting method. The zero crossings of the incoming tones are counted over several periods and the results averaged over a longer period. When a minimum of 30 milliseconds of a valid DTMF digit is detected, the proper data is latched into the outputs and the output strobe goes high. When a valid digit is no longer detected, the strobe will return low and the data will remain latched into the outputs. Minimum interdigit time is 35 milliseconds.

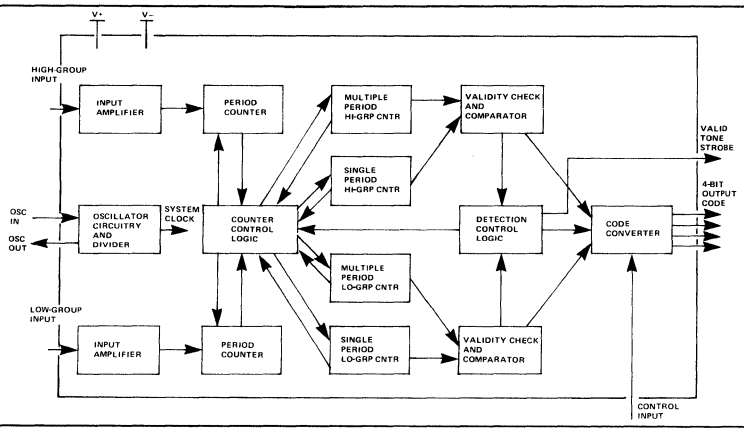
The MK5103 is designed to interface with the MK5099 Integrated Pulse Dialer with only one additional DIP package. These two parts working together form a DTMF-to-Pulse converter that meets the recognized telephone standards.

A block diagram of the MK5103 is shown in Figure 2. Functions of the individual pins are described beginning on page 2.

VI TONE DECODERS

BLOCK DIAGRAM

Figure 2



ABSOLUTE MAXIMUM RATINGS*

DC Supply Voltage V+ (Referenced to V-) ..... +6.0 Volts
Operating Temperature ..... 0°C to 70°C
Storage Temperature ..... -55°C to 100°C
Maximum Circuit Power Dissipation 300mW
Voltage on any pin, with respect to V- ..... -0.3 Volt
Voltage on any pin, with respect to V+ ..... +0.3 Volt

* **Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.**

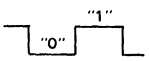
ELECTRICAL CHARACTERISTICS

$0°C \leq T_A \leq 70°C$ V- = **0 Volts**

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage (V+)	(V– = 0)	4.5		5.5	Volts	
Lo Group & Hi Group Inputs	47% - 53% Duty Cycle Rectangular Wave	0.9		V+	Volts Peak-to-Peak	1,2
STROBE, A, B, C, D OUTPUTS	"0" Level	0.0		0.4	Volt @ 1.6 mA	
	"1" Level	(V+)-1		V+	Volts @ 0.1 mA	
FORMAT CONTROL INPUT	"0" Level	0.0		0.5	Volt @ 700μA	
	"1" Level	(V+)-0.5		V+	Volt @ 700μA	
Frequency Detect Band Width		± 2.0	± 2.5	± 2.9	% of f_o	
Tone Coincidence Duration		30			ms	4
Interdigit Interval		35			ms	4
Signal-to-Noise Ratio		14			dB	3,5
Supply Current @ 5.5V	Inputs and Outputs Unloaded		2	5	mA	

NOTES:

1. Due to internal biasing, this input must be capacitively coupled with a low-leakage 0.05 μF capacitor.
2. No coupling capacitor is needed if the DTMF rectangular wave meets the following criteria:



A. Logic "0" level = 1 Volt (max)
B. Logic "1" level = 4 Volts (min)

3. Signal-To-Noise Ratio is defined as:
$$SN = 20 \log \frac{SA}{NA}$$
where SA = RMS Amplitude of single tone being detected.
NA = RMS white noise in the band from 300Hz to 3.4KHz.
4. Tone coincidence duration and interdigit interval measured at High- and Low-group inputs. Filter and/or limiter or comparator characteristics will affect the overall detect time.
5. Signal-To-Noise Ratio with 33db Filter Separation.

FUNCTIONAL DESCRIPTION

OSCILLATOR

The MK5103 contains an on-board inverter with sufficient gain to provide oscillation when working with a low-cost television "color-burst" crystal. The inverter input is OSC IN (pin 2) and output is OSC OUT (pin 3). The circuit is designed to work with a crystal cut to 3.579545 MHz to give detection of the standard DTMF frequencies.

FORMAT CONTROL (PIN 5)

The Control pin is used to control the output format of Pins 7 through 10. This three-state input selects a 4-bit Binary Code, a Dual 2-Bit Row/Column code, or high-impedance output for use with bus-structured circuitry. This three-state input is controlled as follows:

FORMAT CONTROL FUNCTIONS
Table 1

FORMAT CONTROL INPUT	OUTPUT DATA FORMAT
V-	High Impedance
V+	4-Bit Binary
Floating	Dual 2-Bit Row/Column

The following table describes the two output codes.

Table 2

	4-Bit Binary				Dual 2-Bit Row		Column	
Digit	D	C	B	A	D	C	B	A
1	0	0	0	1	0	1	0	1
2	0	0	1	0	0	1	1	0
3	0	0	1	1	0	1	1	1
4	0	1	0	0	1	0	0	1
5	0	1	0	1	1	0	1	0
6	0	1	1	0	1	0	1	1
7	0	1	1	1	1	1	0	1
8	1	0	0	0	1	1	1	0
9	1	0	0	1	1	1	1	1
0	1	0	1	0	0	0	1	0
*	1	0	1	1	0	0	0	1
#	1	1	0	0	0	0	1	1
A	1	1	0	1	0	1	0	0
B	1	1	1	0	1	0	0	0
C	1	1	1	1	1	1	0	0
D	0	0	0	0	0	0	0	0

Figure 3 shows the relationship between the data output code shown in Table 2 and the standard DTMF keyboard.

DTMF DIALING MATRIX
Figure 3

	Col 1	Col 2	Col 3	Col 4
Row 1	1	2	3	A
Row 2	4	5	6	B
Row 3	7	8	9	C
Row 4	*	0	#	D

Note: Column 4 is for special applications and is not normally used in telephone dialing.

Table 3 shows the detection frequency associated with each row or column:

DETECTION FREQUENCY
Table 3

Low Group fo	High Group fo
Row 1 = 697 Hz	Column 1 = 1209 Hz
Row 2 = 770 Hz	Column 2 = 1336 Hz
Row 3 = 852 Hz	Column 3 = 1477 Hz
Row 4 = 941 Hz	Column 4 = 1633 Hz

OUTPUTS A THRU D (PINS 7 THRU 10)

Outputs A thru D are CMOS push-pull when enabled and open-circuited (high impedance) when disabled by the format control pin.

A thru D are the data out lines. The output data can be in in two formats as described in the section about the format control pin (pin 5).

The Dual 2-Bit Row/Column code decodes with A and B indicating the column selected, and C and D indicating the row selected.

The two output codes allow the user to obtain either 1-of-16 or 2-of-8 output data by using only a single additional package.

N/C (PINS 13 THRU 16)

Pins 13 thru 16 are not internally connected and may be used as tie points.

STROBE (PIN 4)

The STROBE output goes to a "1" when 30 milliseconds of a valid DTMF signal is detected and remains at a "1" until an interdigit interval has been detected. The data at A-D are already valid when STROBE goes to a "1" and will remain unchanged until the next DTMF digit is detected.

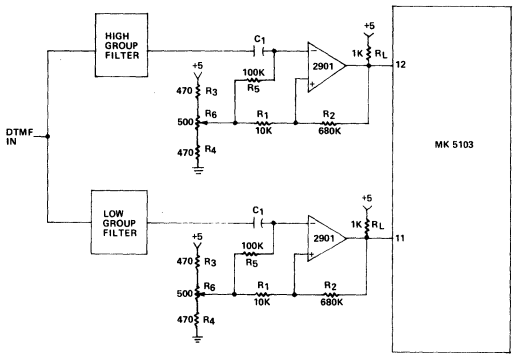
LOW-GROUP INPUT (PIN 11) AND HIGH-GROUP INPUT (PIN 12)

The circuitry driving these inputs, as shown in Figure 4, should be squaring circuits which use resistive dividers to set the output duty cycle to 50%. The squaring circuit shown was designed to provide hysteresis and allow the circuit to respond to signal levels of -28dBm or greater, where -28dBm corresponds to a peak-to-peak voltage of 87.1 mV. Any squaring circuit providing a 47% - 53% duty cycle over the receiver and dynamic range is sufficient.

The high-group and low-group signals are provided by the high-group filter and the low-group filter, as shown in Figure 4. These filters have the response characteristics shown in Figure 5 and are used to separate the DTMF signal into its high-group and low-group components.

SUGGESTED INPUT LIMITER CIRCUIT

Figure 4

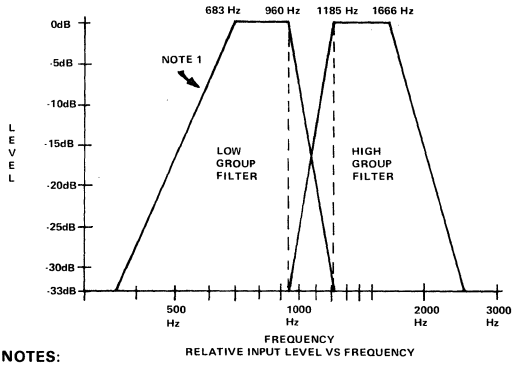


APPLICATIONS

Two possible applications of the MK5103 are shown in Figure 6 and Figure 7. The dual 2-bit row/column code is useful when interfacing a key-to-pulse converter, as shown in Figure 6. On this circuit, the MK5103N-5, CD4556 and MK5099 combine to form a tone-to-pulse converter, which allows the use of DTMF telephones in rotary exchanges. The DTMF tones are detected by the MK5103N-5, which then generates the corresponding row/column code. Each CD4556 then uses this 2-bit code to select 1 of 4 active-low outputs. The MK5099 then interprets these signals as a valid key closure and generates a corresponding series of pulses.

INPUT BAN SEPARATION FILTER

Figure 5



RELATIVE INPUT LEVEL VS FREQUENCY

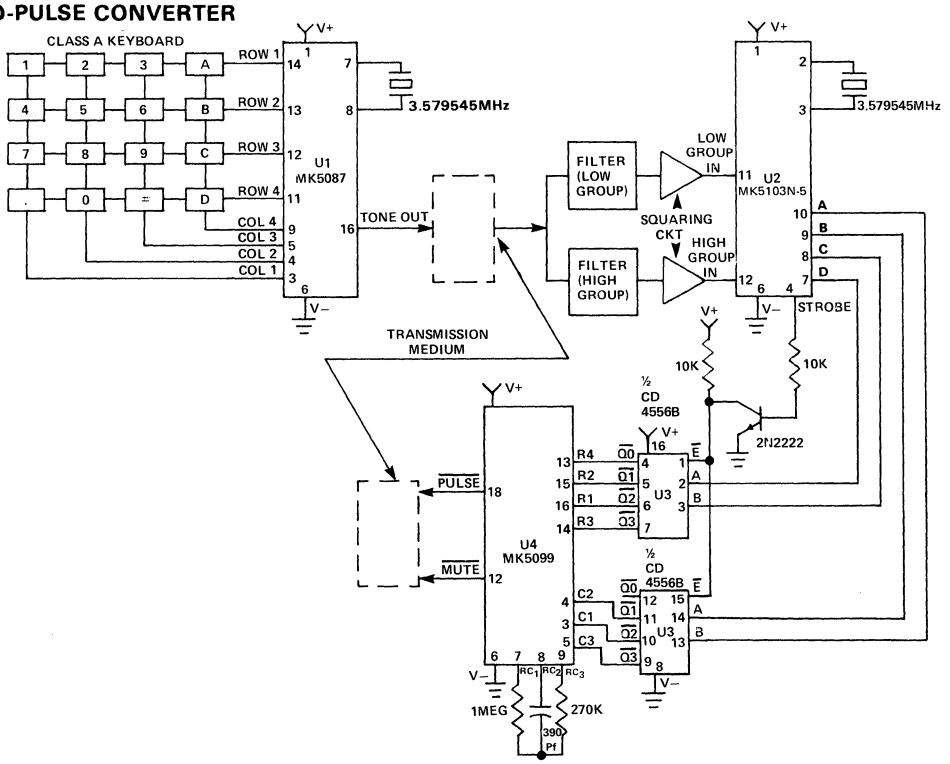
NOTES:

1. Dial tone notch filter adequate to maintain S/N ratio of ≥ 14dB in above bands.
2. Filter response described above will normally result in operation to 6dB of twist with 14dB S/N.
3. Filter separation is defined as either the rejection ratio of high group frequencies to low group frequencies, or the rejection ratio of low-group frequencies to high-group frequencies, whichever ratio is smaller.
4. Filter separation may be reduced to 28dB, resulting in operation to 6dB of twist with an 18dB S/N ratio.

For simple remote-control applications, the circuit of Figure 7 is useful. After a valid tone is detected, strobe will go high and one of the 16 outputs on the binary-to-1-of-16 encoder will go true. Thus, a DTMF transmitter and 16-key keyboard can be used to control 1 of 16 functions in a DTMF receiver.

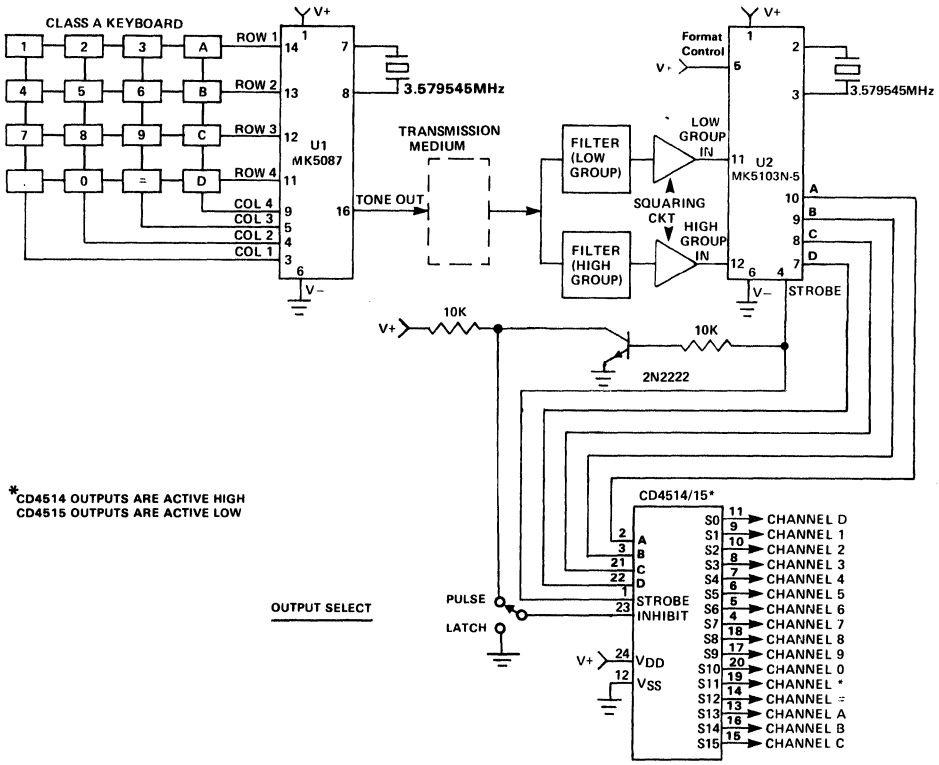
TONE-TO-PULSE CONVERTER

Figure 6



16-CHANNEL REMOTE CONTROL

Figure 7



PRELIMINARY

MOSTEK

μ-255 LAW COMPANDING CODEC

MK5116

FEATURES

- ± 5-Volt Power Supplies
- Low Power Dissipation - 30mW (Typ)
- Follows the μ-255 Companding Law
- Exceeds D3 Channel Bank Transmission Specifications
- Synchronous or Asynchronous Operation
- On-Chip Sample and Hold
- On-Chip Offset Null Circuit Eliminates Long-Term Drift Errors and Need for Trimming
- Single 16-Pin Package
- Minimal External Circuitry Required
- Serial Data Output of 64kb/s—2.1Mb/s at 8kHz Sampling Rate
- Separate Analog and Digital Grounding Pins Reduce System Noise Problems

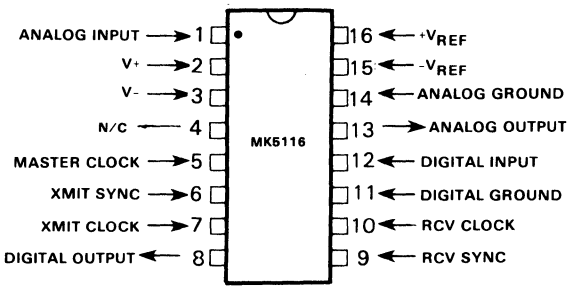
DESCRIPTION

The MK5116 is a monolithic CMOS companding CODEC which contains two sections: (1) An analog-to-digital converter which has a transfer characteristic conforming to the μ-255 companding law and (2) a digital-to-analog converter which also conforms to the μ-255 law.

These two sections form a coder-decoder which is designed to meet the needs of the telecommunications industry for per-channel voice-frequency codecs used in D3 Channel Bank and PBX systems. Digital input and output are in serial format. Actual transmission and reception of 8-bit data words containing the analog information is done at a 64kb/s-2.1Mb/s rate with analog signal sampling occuring at an 8kHz rate. A sync pulse input is provided for synchronizing transmission and reception of multi-channel information being multiplexed over a single transmission line.

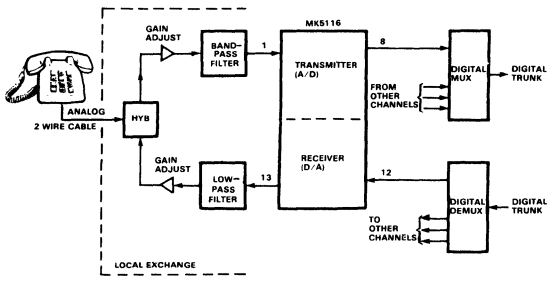
The pin configuration of the MK5116 is shown in Figure 1.

PIN CONNECTIONS
Figure 1



A block diagram of a PCM system using the MK5116 is shown in Figure 2.

PCM SYSTEM BLOCK DIAGRAM
Figure 2

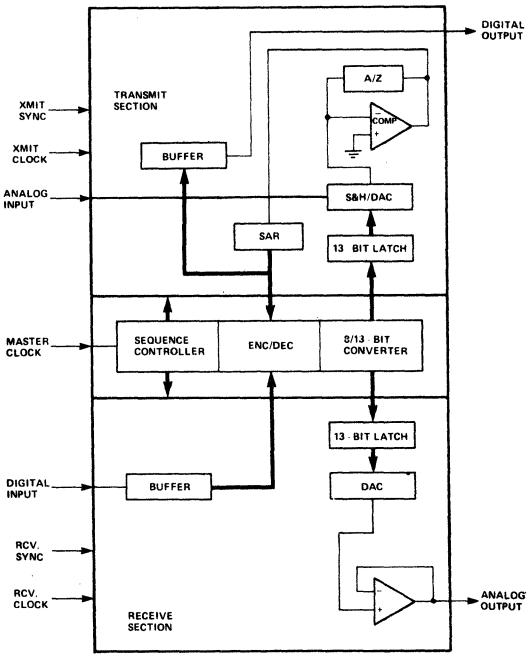


VII CODEC

FUNCTIONAL DESCRIPTION: (Refer to Figure 3 for a Block Diagram)

MK5116 BLOCK DIAGRAM

Figure 3



POSITIVE AND NEGATIVE REFERENCE VOLTAGES ($+V_{REF}$ and $-V_{REF}$) Pins 16 and 15

These inputs provide the conversion references for the digital-to-analog converters in the MK5116 $+V_{REF}$ and $-V_{REF}$ must maintain 100ppM/°C regulation over the operating temperature range. Variation of the reference directly affects system gain.

ANALOG INPUT, Pin 1

Voice-frequency analog signals which are bandwidth-limited to 4kHz are input at this pin. Typically, they are then sampled at an 8kHz rate (Refer to Figure 4.). The analog input must remain between $+V_{REF}$ and $-V_{REF}$ for accurate conversion.

MASTER CLOCK, Pin 5

This signal provides the basic timing and control signals required for all internal conversions. It does not have to be synchronized with RCV. SYNC, RCV. CLOCK, XMIT SYNC or XMIT CLOCK and is not internally related to them.

XMIT SYNC, Pin 6 (Refer to Figure 10 for the Timing Diagram)

This input is synchronized with XMIT CLOCK. When XMIT SYNC goes high, the digital output is activated and the A/D conversion begins on the next positive edge of MASTER CLOCK. The conversion by MASTER CLOCK can be asynchronous with XMIT CLOCK. The serial output data is clocked out by the positive edges of XMIT CLOCK. The negative edge of XMIT SYNC causes the digital output to become three-state. XMIT SYNC may remain high longer than 8 XMIT CLOCK cycles, but must go low for at least 1 master clock prior to the transmission of the next digital word(Refer to Figure 12).

XMIT CLOCK, Pin 7 (Refer to Figure 10 for the Timing Diagram)

The on-chip 8-bit output shift register of the MK5116 is unloaded at the clock rate present on this pin. Clock rates of 64kHz-2.1MHz can be used for XMIT CLOCK. The positive edge of the INTERNAL CLOCK transfers the data from the master to the slave of a master-slave flip-flop (Refer to Figure 5). If the positive edge of XMIT SYNC occurs after the positive edge of XMIT CLOCK, XMIT SYNC will determine when the first positive edge of INTERNAL CLOCK will occur. In this event, the hold time for the first clock pulse is measured from the positive edge of XMIT SYNC.

RCV. SYNC, Pin 9 (Refer to Figure 11 for the Timing diagram)

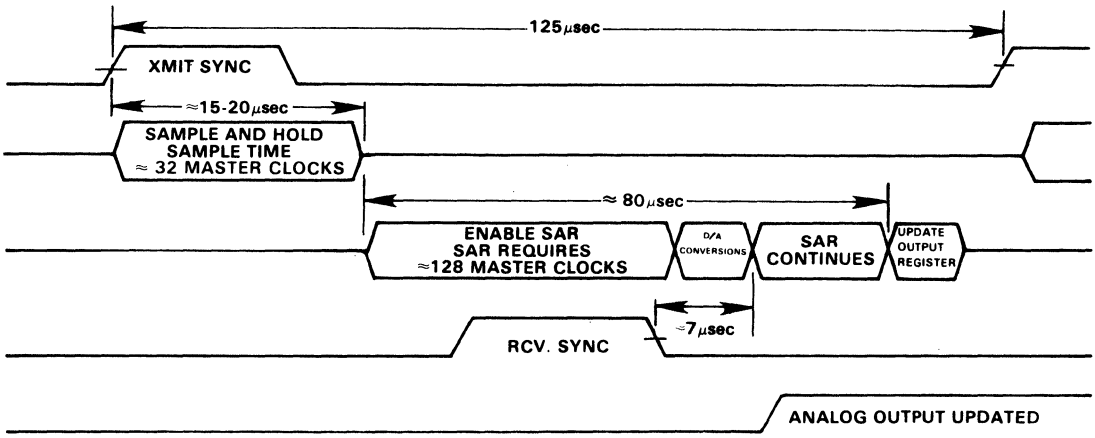
This input is synchronized with RCV. CLOCK and serial data is clocked in by RCV. CLOCK. Duration of the RCV. SYNC pulse is approximately 8 RCV. CLOCK periods. The conversion from digital-to-analog starts after the negative edge of the RCV. SYNC pulse (Refer to Figure 4). The negative edge of RCV. SYNC should occur before the 9th positive clock edge to insure that only eight bits are clocked in. RCV. SYNC must stay low for 17 MASTER CLOCKS (min.) before the next digital word is to be received (Refer to Figure 13).

RCV CLOCK, Pin 10 (Refer to Figure 11 for Timing Diagram)

The on-chip 8-bit shift register for the MK5116 is loaded at the clock rate present on this pin. Clock rates of 64kHz-2.1MHz can be used for RCV. CLOCK. Valid data should be applied to the digital input before the positive edge of the internal clock (Refer to Figure 5). This set up time, t_{RDS}, allows the data to be transferred into the MASTER of a master-slave flip-flop. The positive edge of the INTERNAL CLOCK transfers the data to the SLAVE of the master-slave flip-flop. A hold time, t_{RDH}, is required to complete this transfer. If the rising edge of RCV. SYNC occurs after the first rising edge of RCV. CLOCK, RCV. SYNC will determine when the first positive edge of INTERNAL CLOCK will occur. In this event, the set up and hold times for the first clock pulse should be measured from the positive edge of RCV. SYNC.

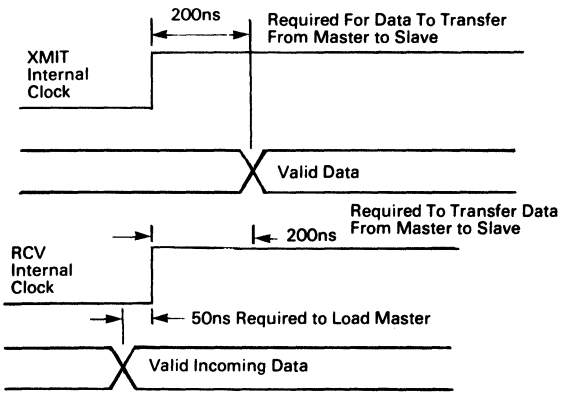
A/D, D/A CONVERSION TIMING

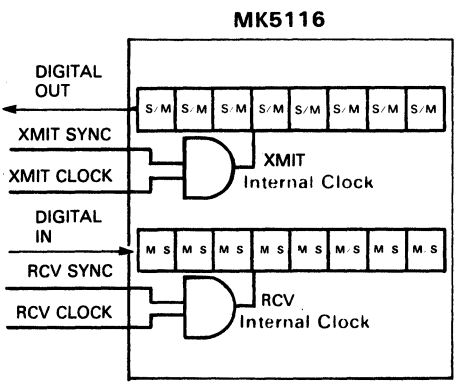
Figure 4



DATA INPUT/OUTPUT TIMING

Figure 5





DIGITAL OUTPUT, Pin 8

The MK5116 output register stores the 8-bit encoded sample of the analog input. This 8-bit word is shifted out under control of XMIT SYNC and XMIT CLOCK. When XMIT SYNC is low, the DIGITAL OUTPUT is an open circuit. When XMIT SYNC is high, the state of the DIGITAL OUTPUT is determined by the value of the output bit in the serial shift register. The output is composed of a Sign Bit, 3 Chord Bits, and 4 Step Bits. The Sign Bit indicates the polarity of the analog input while the Chord and Step Bits indicate the magnitude. In the first Chord, the Step Bit has a value of 0.6mV. In the second Chord, the Step Bit has a value of 1.2mV. This doubling of the step value continues for each of the six successive Chords.

Each Chord has a specific value and the Step Bits, 16 in each Chord, specify the displacement from that value (Refer to Table 1). Thus the output, which follows the μ-255 law, has resolution that is proportional to the input level rather than to full scale. This provides the resolution of a 12-bit A/D converter at low input levels and that of a 6-bit converter as the input approaches full scale. The transfer characteristic of the A/D converter (μ-law Encoder) is shown in Figure 6.

DIGITAL OUTPUT CODE μ-LAW

Table 1

	Chord Code	Chord Value	Step Value
1.	000	0.0mV	0.613mV
2.	001	10.11mV	1.226mV
3.	010	30.3mV	2.45mV
4.	011	70.8mV	4.90mV
5.	100	151.7mV	9.81mV
6.	101	313mV	19.61mV
7.	110	637mV	39.2mV
8.	111	1.284V	78.4mV

EXAMPLE:

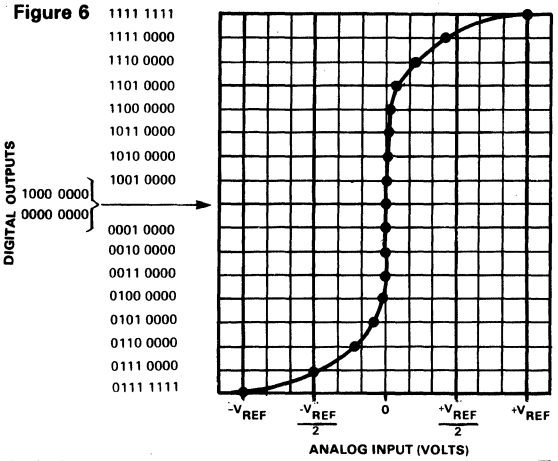
1 011 0010 = + 70.8mV + (2 x 4.90mV)

Sign Bit Chord Step Bits

If the sign bit were a zero, then both plus signs would be changed to minus signs.

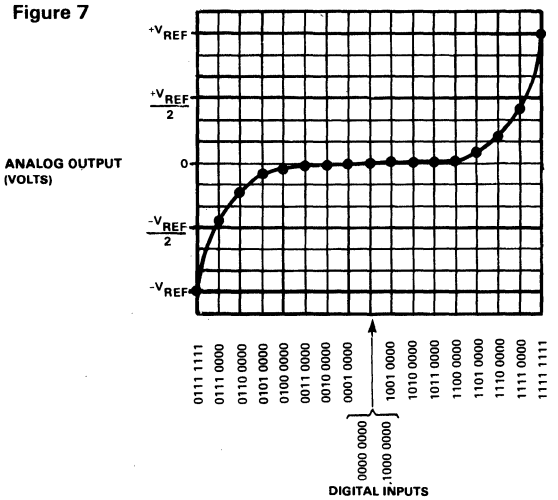
A/D CONVERTER (μ-Law Encoder) TRANSFER CHARACTERISTIC

Figure 6



D/A CONVERTER (μ-Law Decoder) TRANSFER CHARACTERISTIC

Figure 7



DIGITAL INPUT, Pin 12

The MK5116 input register accepts the 8-bit sample of an analog value and loads it under control of RCV. SYNC and RCV. CLOCK. The timing diagram is shown in Figure 11. When RCV. SYNC goes high, the MK5116 uses RCV. CLOCK to clock the serial data into its input register. RCV. SYNC goes low to indicate the end of serial input data. The 8 bits of the input data have the same functions described for the DIGITAL OUTPUT. The transfer characteristic of the D/A converter (μ-law Decoder) is shown in Figure 7.

ANALOG OUTPUT, Pin 13

The analog output is in the form of voltage steps (100% duty cycle) having amplitude equal to the analog sample which was encoded. This waveform is then filtered with an external low-pass filter with sinx/x correction to recreate the sampled voice signal.

OPERATION OF CODEC WITH 64kHz XMIT/RCV CLOCK FREQUENCIES

XMIT/RCV. SYNC must not be allowed to remain at a logic "1" state. XMIT SYNC is required to be at a logic "0" state for 1 master clock period (min.) before the next digital word is transmitted. RCV. SYNC is required to be at a logic "0" state for 17 master clock periods (min.) before the next digital word is received (Refer to Figures 12 and 13).

OFFSET NULL

The offset null feature of the MK5116 eliminates long-term drift errors and conversion errors due to temperature changes by going through an offset adjustment cycle before every conversion, thus guaranteeing accurate A/D conversion for inputs near ground. There is no offset adjust of the output amplifier because, since the output is intended to be AC - coupled to the external filter, the resultant DC error ($V_{OFFSET/O}$) will have no effect. The sign bit is not used to null the analog input. Therefore, for an analog input of 0 volts, the sign bit will be stable.

PERFORMANCE EVALUATION

The equipment connections shown in Figure 8 can be used to evaluate the performance of the MK5116. An analog signal provided by the HP3551A Transmission Test Set is connected to the Analog Input (Pin 1) of the MK5116. The Digital Output of the CODEC is tied back to the Digital Input and the Analog Output is fed through a low-pass filter to the HP3551A. Remaining pins of the MK5116 are connected as follows:

(1) RCV. SYNC is tied to XMIT SYNC

(2) XMIT CLOCK is tied to MASTER CLOCK. The signal is inverted and tied to RCV. CLOCK.

The following timing signals are required:

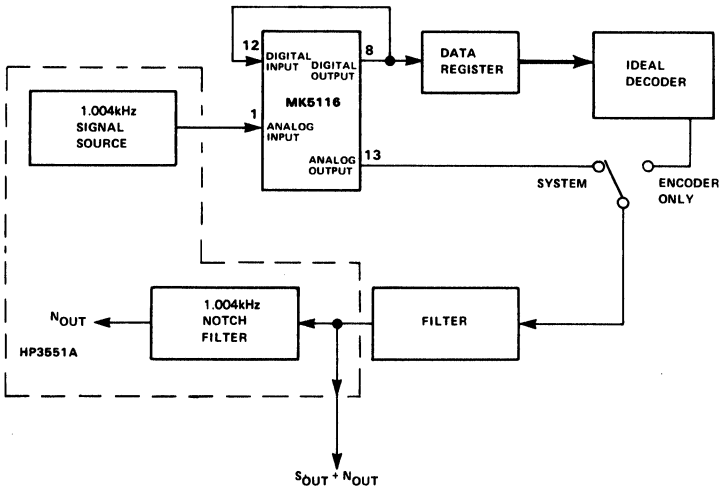
(1) MASTER CLOCK = 1.544MHz
(2) XMIT SYNC repetition rate = 8kHz
(3) XMIT SYNC width = 8 XMIT CLOCK periods

When all the above requirements are met, the setup of Figure 8 permits the measurement of synchronous system performance over a wide range of analog inputs. The data register and ideal decoder provide a means of checking the encoder portion of the MK5116 independently of the decoder section. To test the system in the asynchronous mode, MASTER CLOCK should be separated from XMIT CLOCK and MASTER CLOCK should be separated from RCV. CLOCK. XMIT and RCV. CLOCKS are separated also.

Some experimental results obtained with the MK5116 are shown in Figure 14 and Figure 15. In each case, both the measured results and the corresponding D3 Channel Bank specifications are shown. The MK5116 exceeds the requirements for Signal-to-Distortion ratio (Figure 14) and for Gain Tracking (Figure 15).

SYSTEM CHARACTERISTICS TEST CONFIGURATION

Figure 8



NOTE: The ideal decoder consists of a digital decompander and a 13-bit precision DAC.

ABSOLUTE MAXIMUM RATINGS

DC Supply Voltage, V+ ..... +6V
DC Supply Voltage, V- ..... -6V
Operating Temperature ..... 0°C to 70°C
Storage Temperature ..... -55°C to +125°C
Package Dissipation at 25°C (Derated 9mW/°C when soldered into PCB) 500mW
Digital Input ..... $-0.5V \leq V_{IN} \leq V+$
Analog Input ..... $V- \leq V_{IN} \leq V+$
$+V_{REF}$ ..... $-0.5V \leq +V_{REF} \leq V+$
$-V_{REF}$ ..... $V- \leq -V_{REF} \leq +0.5V$

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL OPERATING CHARACTERISTICS
POWER SUPPLY REQUIREMENTS

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V+	Positive Supply Voltage	4.75	5.0	5.25	V	
V-	Negative Supply Voltage	-5.25	-5.0	-4.75	V	
$+V_{REF}$	Positive Reference Voltage	2.375	2.5	2.625	V	1
$-V_{REF}$	Negative Reference Voltage	-2.625	-2.5	-2.375	V	1

TEST CONDITIONS: V+ = 5.0V, V- = -5.0V, + V_{REF} = 2.5V, -V_{REF} = -2.5V

DC CHARACTERISTICS

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
R_{INAS}	Analog Input Resistance During Sampling		2		kΩ	2
R_{INANS}	Analog Input Resistance Non-Sampling		100		MΩ	
C_{INA}	Analog Input Capacitance		150	250	pF	
$V_{OFFSET/I}$	Analog Input Offset Voltage		±1	± 8	mV	
R_{OUTA}	Analog Output Resistance		20	50	Ω	
I_{OUTA}	Analog Output Current	0.25	0.5		mA	
$V_{OFFSET/O}$	Analog Output Offset Voltage		-200	± 850	mV	
I_{INLOW}	Logic Input Low Current (V_{IN} = 0.8V) Digital Input, Clock Input, Sync Input		± 0.1	± 10	μA	3
I_{INHIGH}	Logic Input High Current (V_{IN} = 2.4V) Digital Input, Clock Input, Sync Input		-0.25	-0.8	mA	3
C_{DO}	Digital Output Capacitance		8	12	pF	
I_{DOL}	Digital Output Leakage Current		± 0.1	±10	μA	
V_{OUTLOW}	Digital Output Low Voltage			0.4	V	4
$V_{OUTHIGH}$	Digital Output High Voltage	3.9			V	4
I+	Positive Supply Current		4	10	mA	
I-	Negative Supply Current		2	6	mA	
I_{REF+}	Positive Reference Current		4	20	μA	
I_{REF-}	Negative Reference Current		4	20	μA	

AC CHARACTERISTICS (Refer to Figure 10 and Figure 11)

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
F_M	Master Clock Frequency	1.5	1.544	2.1	MHz	
F_R, F_X	XMIT, RCV. Clock Frequency	0.064	1.544	2.1	MHz	
PW_{CLK}	Clock Pulse Width (MASTER, XMIT, RCV.)	200			ns	
t_{RC},t_{FC}	Clock Rise, Fall Time(MASTER, XMIT, RCV.)			25% of PW_{CLK}	ns	
t_{RS}, t_{FS}	Sync Rise, Fall Time (XMIT, RCV.)			25% of PW_{CLK}	ns	
t_{DIR}, t_{DIF}	Data Input Rise, Fall Time			25% of PW_{CLK}	ns	
t_{WSX}, t_{WSR}	Sync Pulse Width (XMIT RCV.)		$\frac{8}{F_X(F_R)}$		μs	
t_{PS}	Sync Pulse Period (XMIT, RCV.)		125		μs	
t_{XCS}	XMIT Clock-to-XMIT Sync Delay	50% of t_{FC} (t_{RS})			ns	6

AC CHARACTERISTICS (Refer to Figure 10 and Figure 11)

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
t_{XCSN}	XMIT Clock-to-XMIT Sync (Negative Edge) Delay	200			ns	
t_{XSS}	XMIT Sync Set-Up Time	200			ns	
t_{XDD}	XMIT Data Delay	0		200	ns	4
t_{XDP}	XMIT Data Present	0		200	ns	4
t_{XDT}	XMIT Data Three State			150	ns	4
t_{DOF}	Digital Output Fall Time		50		ns	4
t_{DOR}	Digital Output Rise Time		50		ns	4
t_{SRC}	RCV. Sync-to-RCV. Clock Delay	50% of t_{RC} (t_{FS})			ns	6
t_{RDS}	RCV. Data Set-Up Time	50			ns	5
t_{RDH}	RCV. Data Hold Time	200			ns	5
t_{RCS}	RCV. Clock-to-RCV. Sync Delay	200			ns	
t_{RSS}	RCV. Sync Set-Up Time	200			ns	5
t_{SAO}	RCV. Sync-to-Analog Output Delay		7		μs	
SLEW+	Analog Output Positive Slew Rate		1		V/μs	
SLEW–	Analog Output Negative Slew Rate		1		V/μs	
DROOP	Analog Output Droop Rate		25		μV/μs	

SYSTEM CHARACTERISTICS (Refer to Figures 14 and 15)

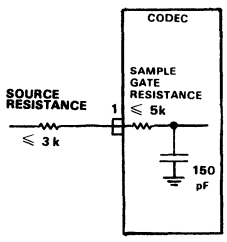
SYM	PARAMETER	MIN	TYP	MAX	UNITS	TEST COND.
S/D	Signal-to-Distortion Ratio	35 29 24	39 34 29		dB dB dB	Analog Input=0 to -30dBm0 Analog Input=-40dBm0 Analog Input=-45dm0
GT	Gain Tracking	-0.4 -0.8 -2.5	±0.1 ±0.1 ±0.2	+0.4 +0.8 +2.5	dB dB dB	Analog Input=+3 to -37dBm0 Analog Input=-37 to -50dBm0 Analog Input=-50 to -55dBm0
N_{IC}	Idle Channel Noise		10	18	dBrnc0	Analog Input=0 Volts
TLP	Transmission Level Point		+4		dB	600Ω

NOTES:

1. $+V_{REF}$ and $-V_{REF}$ must be matched within ± 1% in order to meet system requirements.
2. Sampling is accomplished by charging the internal capacitor to within ½ LSB ($\leq 300\mu V$) in 20μs. Therefore, the external source resistance must be 3k or less. The equivalent circuit during sampling is shown in Figure 9.
3. The MK5116 will source current through an internal 6kΩ resistor to help pull up the TTL output. When a transition from a "1" to a "0" takes place, the user must sink the "1" current until reaching the "0" level.
4. Driving one 74L or 74LS TTL load plus 30pF with $I_{OH} = -100\mu A$, $I_{OL} = 500\mu A$.
5. The first bit of data is loaded when the Sync and Clock are both "1" during bit time 1 as shown on RCV. timing diagram.
6. This delay is necessary to avoid overlapping CLOCK and SYNC.

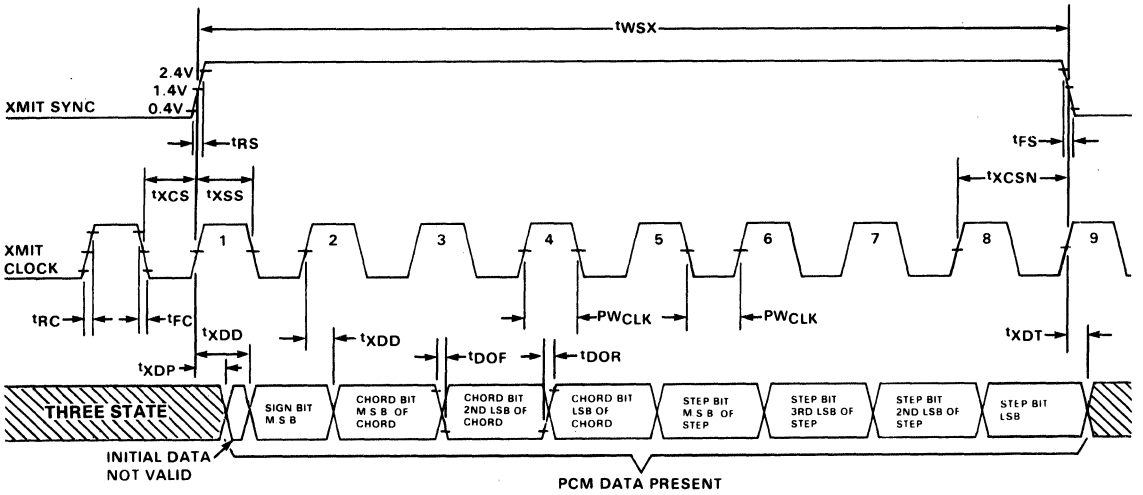
EQUIVALENT INPUT RESISTANCE CIRCUIT DURING SAMPLING

Figure 9



TRANSMITTER SECTION TIMING

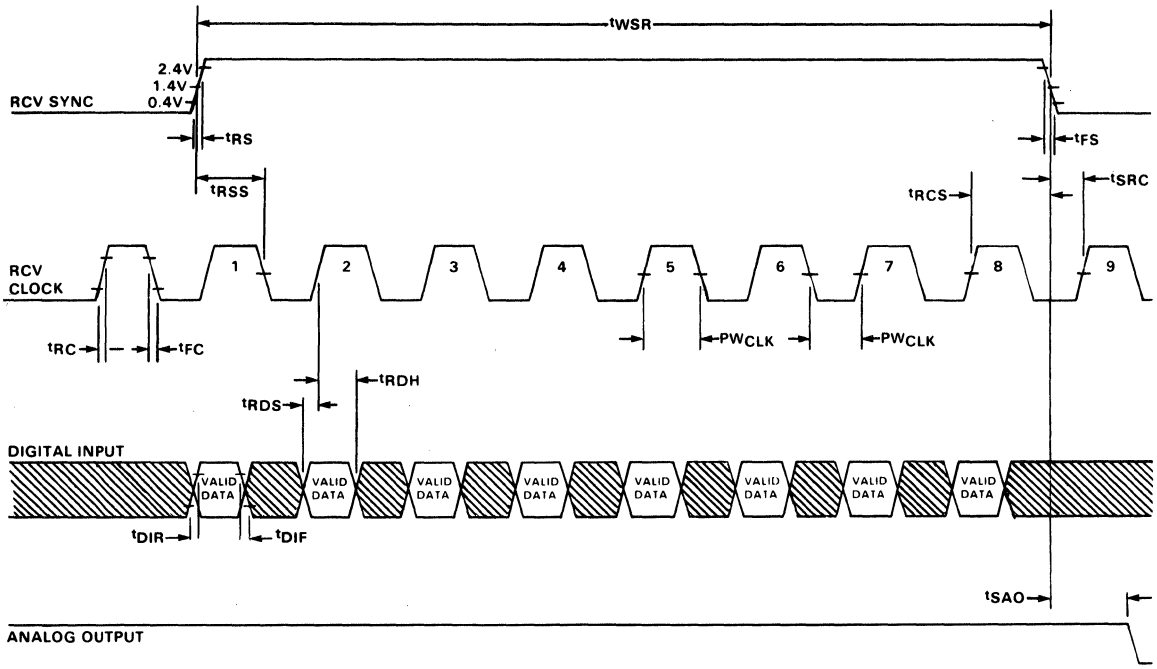
Figure 10



NOTE: All rise and fall times are measured from 0.4V and 2.4V. All delay times are measured from 1.4V.

RECEIVER SECTION TIMING

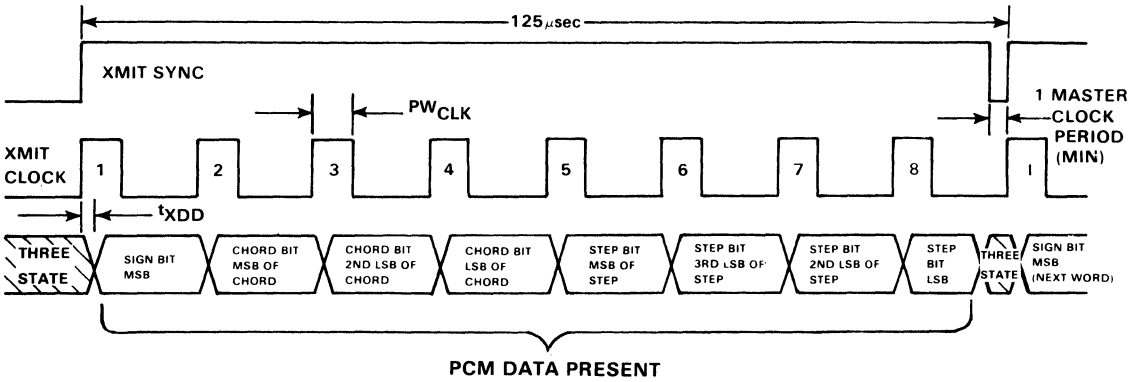
Figure 11



NOTE: All rise and fall times are measured from 0.4V and 2.4V. All delay times are measured from 1.4V.

64kHz OPERATION, TRANSMITTER SECTION TIMING

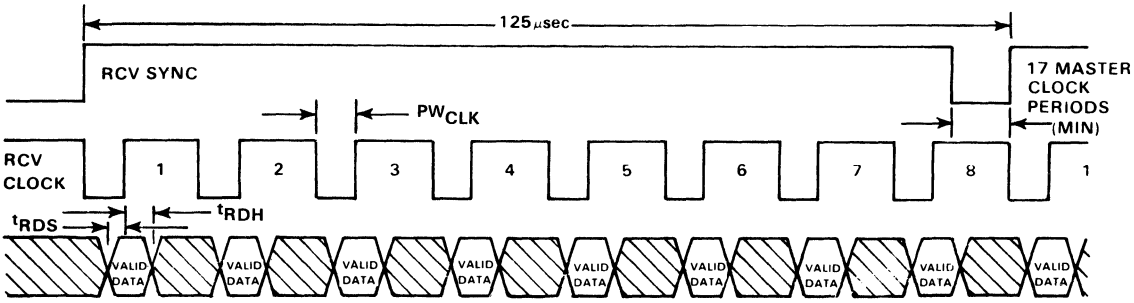
Figure 12



NOTE: All rise and fall times are measured from 0.4V and 2.4V. All delay times are measured from 1.4V.

64kHz OPERATION, RECEIVER SECTION TIMING

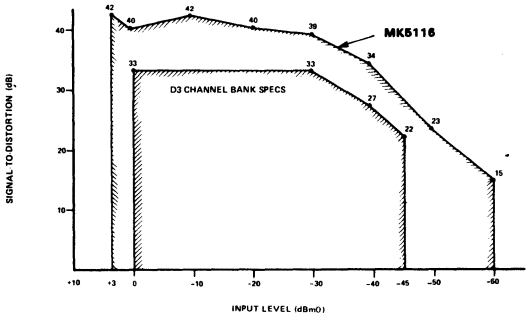
Figure 13



NOTE: All rise and fall times are measured from 0.4V and 2.4V. All delay times are measured from 1.4V.

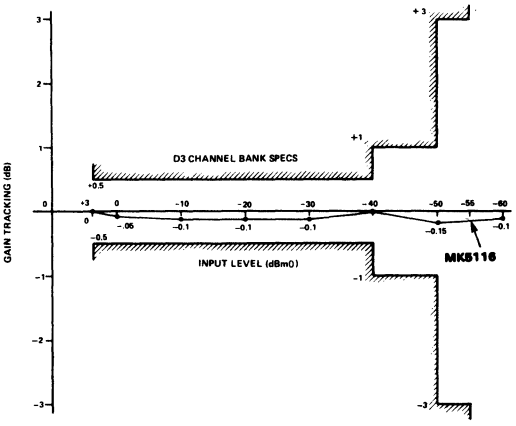
MK5116 S/D RATIO VS: INPUT LEVEL

Figure 14



MK5116 GAIN TRACKING PERFORMANCE

Figure 15



PRELIMINARY

MOSTEK®

μ-255 LAW COMPANDING CODEC

MK5151

FEATURES

- ±5-Volt Power Supplies
- Low Power Dissipation - 30mW (Typ)
- **Follows the μ-255 Companding Law**
- Exceeds D3 Specifications - Zero Code Suppression and Sign-Magnitude Data Format
- On-Chip Sample and Hold
- On-Chip Offset Null Circuit Eliminates Long-Term Drift Errors and Need for Trimming
- Single 24-Pin Package
- Minimal External Circuitry Required
- Serial Data Output of 64kb/s - 2.1Mb/s at 8kHz Sampling Rate
- Separate Analog and Digital Grounding Pins Reduce System Noise Problems

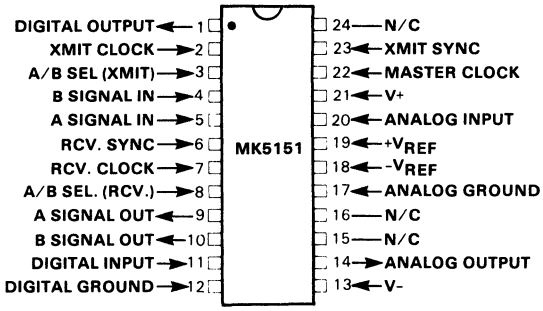
DESCRIPTION

The MK5151 is a monolithic CMOS companding CODEC which contains two sections: (1) An analog-to-digital converter which has a transfer characteristic conforming to the μ-255 companding law and (2) a digital-to-analog converter which also conforms to the μ-255 law.

These two sections form a coder-decoder which is designed to meet the needs of the telecommunications industry for per-channel voice-frequency codecs used in D3 Channel Bank and PBX systems. Digital input and output are in serial format. Actual transmission and reception of 8-bit data words containing the analog information is done at a 64kb/s-2.1Mb/s rate with analog signal sampling occuring at an 8kHz rate. A sync pulse input is provided for synchronizing transmission and reception of multi-channel information being multiplexed over a single transmission line.

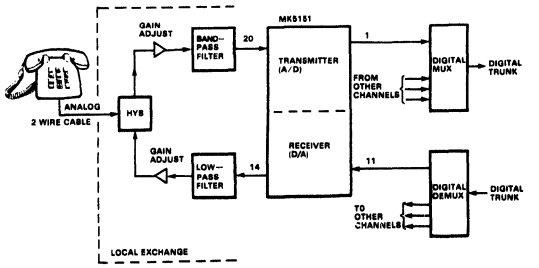
The pin configuration of the MK5151 is shown in Figure 1.

PIN CONNECTIONS
Figure 1



A block diagram of a PCM system using the MK5151 is shown in Figure 2.

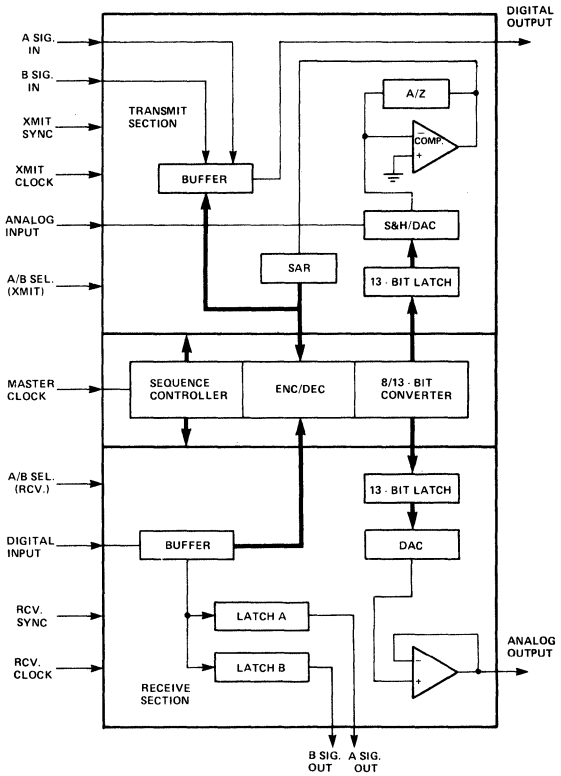
PCM SYSTEM BLOCK DIAGRAM
Figure 2



VII CODECs

FUNCTIONAL DESCRIPTION: (Refer to Figure 3 for a Block Diagram)

MK5151 BLOCK DIAGRAM
Figure 3



POSITIVE AND NEGATIVE REFERENCE VOLTAGES ($+V_{REF}$ and $-V_{REF}$) Pins 19 and 18

These inputs provide the conversion references for the digital-to-analog converters in the MK5151. $+V_{REF}$ and $-V_{REF}$ must maintain 100ppM/°C regulation over the operating temperature range. Variation of the reference directly affects system gain.

ANALOG INPUT, Pin 20

Voice-frequency analog signals which are bandwidth-limited to 4kHz are input at this pin. Typically, they are then sampled at an 8kHz rate (Refer to Figure 4.). The analog input must remain between $+V_{REF}$ and $-V_{REF}$ for accurate conversion.

MASTER CLOCK, Pin 22

This signal provides the basic timing and control signals required for all internal conversions. It does not have to be synchronized with RCV. SYNC, RCV. CLOCK, XMIT SYNC or XMIT CLOCK and is not internally related to them.

XMIT SYNC, Pin 23 (Refer to Figure 12 for the Timing Diagram)

This input is synchronized with XMIT CLOCK. When XMIT SYNC goes high, the digital output is activated and the A/D conversion begins on the next positive edge of MASTER CLOCK. The conversion by MASTER CLOCK can be asynchronous with XMIT CLOCK. The serial output data is clocked out by the positive edges of XMIT CLOCK. The negative edge of XMIT SYNC causes the digital output to become three-state. XMIT SYNC must go low for at least 1 master clock prior to the transmission of the next digital word. (Refer to Figure 14).

XMIT CLOCK, Pin 2 (Refer to Figure 12 for the Timing Diagram)

The on-chip 8-bit output shift register of the MK5151 is unloaded at the clock rate present on this pin. Clock rates of 64kHz-2.1MHz can be used for XMIT CLOCK. The positive edge of the INTERNAL CLOCK transfers the data from the master to the slave of a master-slave flip-flop (Refer to Figure 5). If the positive edge of XMIT SYNC occurs after the positive edge of XMIT CLOCK, XMIT SYNC will determine when the first positive edge of INTERNAL CLOCK will occur. In this event, the hold time for the first clock pulse is measured from the positive edge of XMIT SYNC.

RCV. SYNC, Pin 6 (Refer to Figure 13 for the timing diagram)

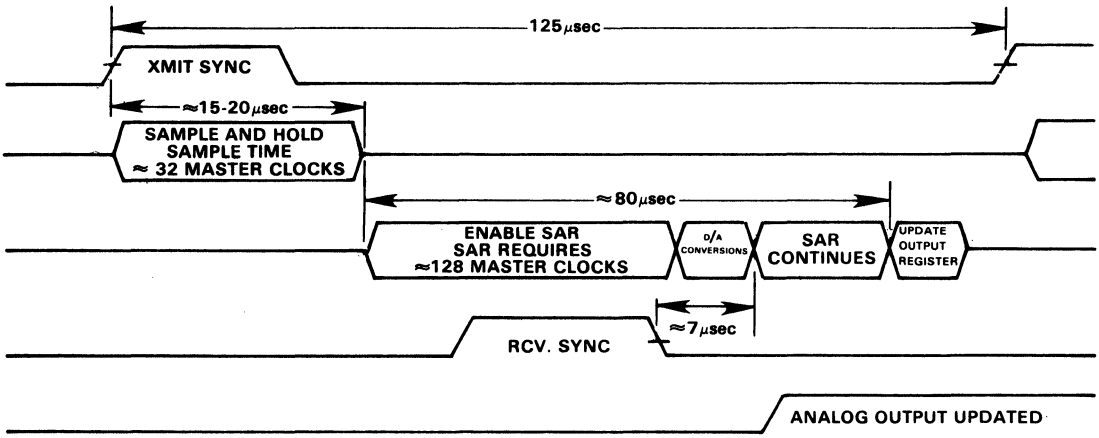
This input is synchronized with RCV. CLOCK and serial data is clocked in by RCV. CLOCK. Duration of the RCV. SYNC pulse is approximately 8 RCV. CLOCK periods. The conversion from digital-to-analog starts after the negative edge of the RCV. SYNC pulse (Refer to Figure 4). The negative edge of RCV. SYNC should occur before the 9th positive clock edge to insure that only eight bits are clocked in. RCV. SYNC must stay low for 17 MASTER CLOCKS (min.) before the next digital word is to be received (Refer to Figure 15).

RCV CLOCK, Pin 7 (Refer to Figure 13 for Timing Diagram)

The on-chip 8-bit shift register for the MK5151 is loaded at the clock rate present on this pin. Clock rates of 64kHz-2.1MHz can be used for RCV. CLOCK. Valid data should be applied to the digital input before the positive edge of the internal clock (Refer to Figure 5). This set up time, t_{RDS}, allows the data to be transferred into the MASTER of a master-slave flip-flop. The positive edge of the INTERNAL CLOCK transfers the data to the SLAVE of the master-slave flip-flop. A hold time, t_{RDH}, is required to complete this transfer. If the rising edge of RCV. SYNC occurs after the first rising edge of RCV. CLOCK, RCV. SYNC will determine when the first positive edge of INTERNAL CLOCK will occur. In this

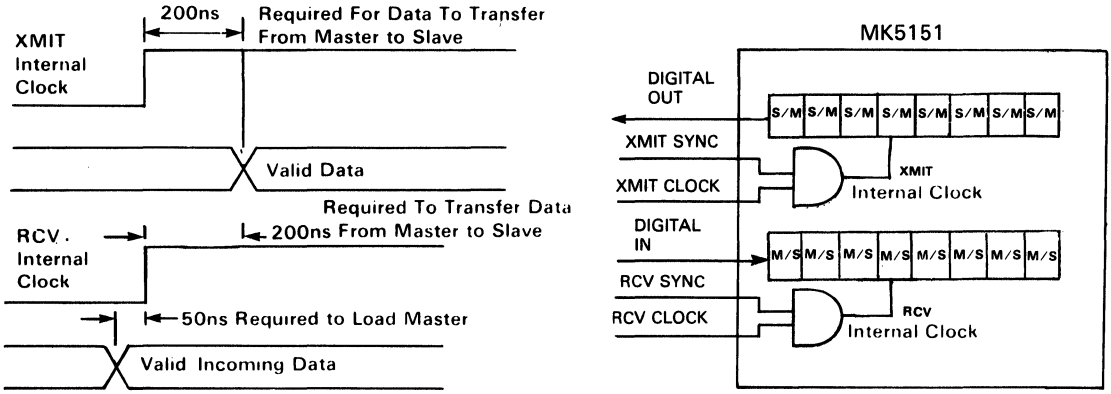
A/D, D/A CONVERSION TIMING

Figure 4



DATA INPUT/OUTPUT TIMING

Figure 5



event, the set-up and hold times for the first clock pulse should be measured from the positive edge of RCV. SYNC.

DIGITAL OUTPUT, Pin 1

The MK5151 output register stores the 8-bit encoded sample of the analog input. This 8-bit word is shifted out under control of XMIT SYNC and XMIT CLOCK. When XMIT SYNC is low, the DIGITAL OUTPUT is an open circuit. When XMIT SYNC is high, the state of the DIGITAL OUTPUT is determined by the value of the output bit in the serial shift register. The output is composed of a Sign Bit, 3 Chord Bits, and 4 Step Bits. The Sign Bit indicates the polarity of the analog input while the Chord and Step Bits indicate the magnitude. In the first Chord, the Step Bit has a value of 0.6mV. In the second Chord, the Step Bit has a value of 1.2mV. This doubling of the step value continues for each of the six successive Chords.

Each Chord has a specific value and the Step Bits, 16 in each Chord, specify the displacement from that value (Refer to Table 1). Thus the output, which follows the μ-255 law, has resolution that is proportional to the input level rather than to full scale. This provides the resolution of a 12-bit A/D converter at low input levels and that of a 6-bit converter as the input approaches full scale. The transfer characteristic of the A/D converter (μ-law Encoder) is shown in Figure 6.

DIGITAL OUTPUT CODE μ-LAW

Table 1

	Chord Code	Chord Value	Step Value
1.	111	0.0mV	0.613mV
2.	110	10.11mV	1.226mV
3.	101	30.3mV	2.45mV
4.	100	70.8mV	4.90mV
5.	011	151.7mV	9.81mV
6.	010	313mV	19.61mV
7.	001	637mV	39.2mV
8.	000	1.284V	78.4mV

EXAMPLE:

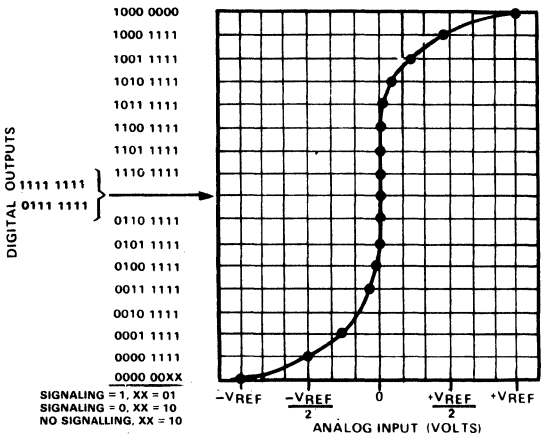
1 100 1101 = +70.8mV + (2 x 4.90mV)

Sign Bit Chord Step Bits

If the sign bit were a zero, then both plus signs would be changed to minus signs.

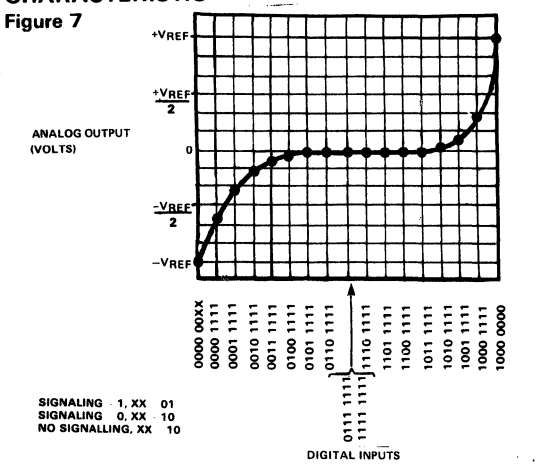
A/D CONVERTER (μ-Law Encoder) TRANSFER CHARACTERISTIC

Figure 6



D/A CONVERTER (μ-Law Decoder) TRANSFER CHARACTERISTIC

Figure 7



DIGITAL INPUT, Pin 11

The MK5151 input register accepts the 8-bit sample of an analog value and loads it under control of RCV. SYNC and RCV. CLOCK. The timing diagram is shown in Figure 13. When RCV. SYNC goes high, the MK5151 uses RCV. CLOCK to clock the serial data into its input register. RCV. SYNC goes low to indicate the end of serial input data. The 8 bits of the input data have the same functions described for the SERIAL OUTPUT. The transfer characteristic of the D/A converter (μ-law Decoder) is shown in Figure 7.

ANALOG OUTPUT, Pin 14

The analog output is in the form of voltage steps (100% duty cycle) having amplitude equal to the analog sample which was encoded. This waveform is then filtered with an external low-pass filter with sinx/x correction to recreate the sampled voice signal. When the 8th bit of the word is a signalling bit, it is assigned a value of ½ step. This results in a lower system quantization error rate than would result if the bit were arbitarily set to 0 (no step) or 1 (full step).

OPERATION OF CODEC WITH 64kHz XMIT/RCV. CLOCK FREQUENCIES

XMIT/RCV. SYNC must not be allowed to remain at a logic "1" state. XMIT SYNC is required to be at a logic "0" state for 1 master clock period (min.) before the next digital word is transmitted. RCV. SYNC is required to be at a logic "0" state for 17 master clock periods (min.) before the next digital word is received (Refer to Figures 14 and 15).

A/B SIGNAL IN, Pins 4 and 5

These two pins allow insertion of signalling information into the transmitted data stream. The inserted information occurs as the 8th bit (LSB) in the transmitted word. A positive transition occuring on A/B SEL (XMIT) selects A SIGNAL IN while a negative transition selects B SIGNAL IN.

A/B SIGNAL OUT, Pins 9 and 10

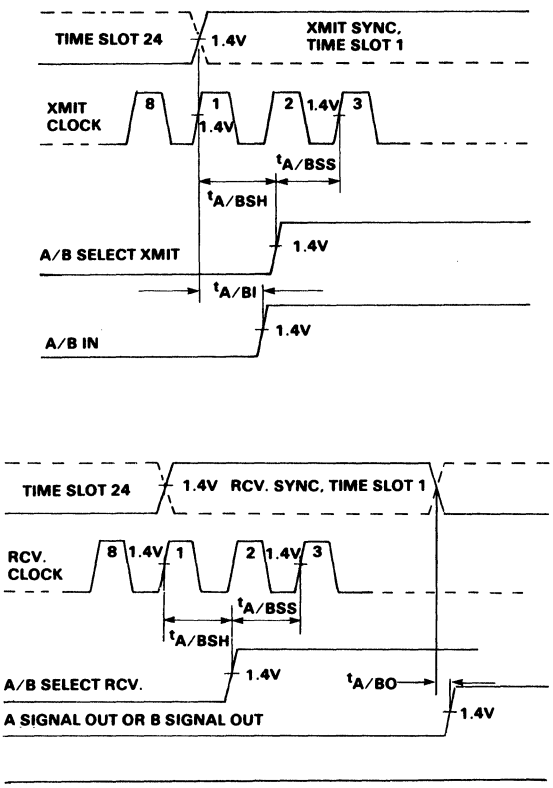
These two pins are provided to output received signalling information. A positive transition on A/B SEL (RCV.) routes the signal bit to A SIGNAL OUT while a negative transition routes the signal bit (bit 8) to B SIGNAL OUT. Refer to Figure 8.

A/B SEL (XMIT), Pin 3

This input selects either A SIGNAL IN or B SIGNAL IN as described in the A/B SIGNAL IN paragraph above, and should be changed only at the start of the 6th and 12th frames as shown in Figure 9.

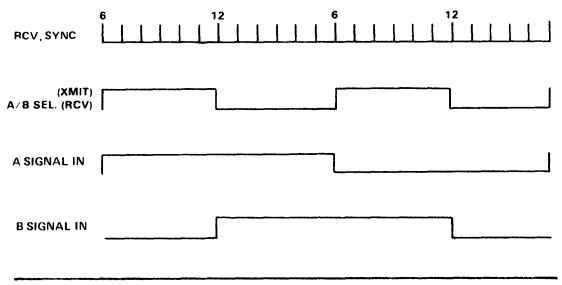
A/B SELECT TIMING

Figure 8



SIGNALLING TIMING REQUIREMENTS FOR PERFORMANCE EVALUATION

Figure 9



A/B SEL (RCV.), Pin 8

This input routes the signalling bit, bit 8, either to A SIGNAL OUT or to B SIGNAL OUT as described in the A/B SIGNAL OUT paragraph above, and should be changed only at the start of the 6th and 12th frames as shown in Figure 9.

OFFSET NULL

The offset null feature of the MK5151 eliminates long-term drift errors and conversion errors due to temperature changes by going through an offset adjustment cycle before every conversion, thus guaranteeing accurate A/D conversion for inputs near ground. There is no offset adjust of the output amplifier because, since the output is intended to be AC - coupled to the external filter, the resultant DC error ($V_{OFFSET/O}$) will have no effect. The sign bit is not used to null the analog input. Therefore, for an analog input of 0 volts, the sign bit will be stable.

PERFORMANCE EVALUATION

The equipment connections shown in Figure 10 can be used to evaluate the performance of the MK5151. An analog signal provided by the HP3551A Transmission Test Set is connected to the Analog Input (Pin 20) of the MK5151. The Digital Output of the CODEC is tied back to the Digital Input and the Analog Output is fed through a low-pass filter to the HP3551A. Remaining pins of the MK5151 are connected as follows:

(1) A/B SEL. (RCV.) is tied to A/B SEL. (XMIT).
(2) RCV. SYNC is tied to XMIT SYNC.
(3) XMIT CLOCK is tied to MASTER CLOCK. The signal is inverted and tied to RCV. CLOCK.

The following timing signals are required:

(1) MASTER CLOCK = 1.544MHz
(2) XMIT SYNC repetition rate = 8kHz
(3) XMIT SYNC width = 8 MASTER CLOCK periods

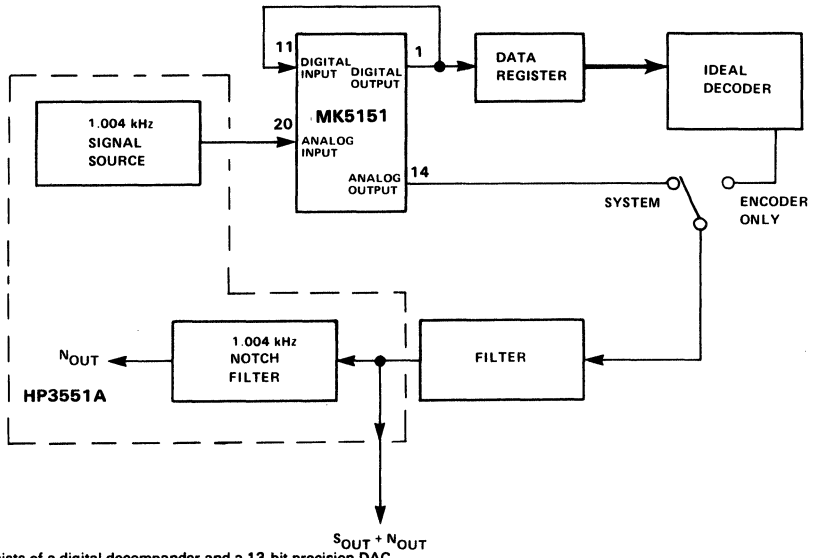
Additional timing signals are shown in Figure 9.

When all the above requirements are met, the setup of Figure 10 permits the measurement of synchronous system performance over a wide range of analog inputs. The data register and ideal decoder provide a means of checking the encoder portion of the MK5151 independently of the decoder section. To test the system in the asynchronous mode, MASTER CLOCK should be separated from XMIT CLOCK and MASTER CLOCK should be separated from RCV. CLOCK. XMIT CLOCK and RCV. CLOCK are separated also.

Some experimental results obtained with the MK5151 are shown in Figure 16 and Figure 17. In each case, both the measured results and the corresponding D3 Channel Bank specifications are shown. The MK5151 exceeds the requirements for Signal-to-Distortion ratio (Figure 17) and for Gain Tracking (Figure 16).

SYSTEM CHARACTERISTICS TEST CONFIGURATION

Figure 10



NOTE: The ideal decoder consists of a digital decompander and a 13-bit precision DAC.

ABSOLUTE MAXIMUM RATINGS

DC Supply Voltage, V+ ..... +6V
DC Supply Voltage, V– ..... -6V
Operating Temperature ..... 0°C to 70°C
Storage Temperature ..... -55°C to +125°C
Package Dissipation at 25°C (Derated 9mW/°C when soldered into PCB) 500mW
Digital Input ..... $-0.5V \leq V_{IN} \leq V+$
Analog Input ..... $V- \leq +V_{IN} \leq V+$
$+V_{REF}$ ..... $-0.5V \leq +V_{REF} \leq V+$
$-V_{REF}$ ..... $V- \leq -V_{REF} \leq 0.5V$

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL OPERATING CHARACTERISTICS
POWER SUPPLY REQUIREMENTS

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V+	Positive Supply Voltage	4.75	5.0	5.25	V	
V–	Negative Supply Voltage	-5.25	-5.0	-4.75	V	
$+V_{REF}$	Positive Reference Voltage	2.375	2.5	2.625	V	1
$-V_{REF}$	Negative Reference Voltage	-2.625	-2.5	-2.375	V	1

TEST CONDITIONS: V+ = 5.0V, V– = -5.0V, + V_{REF} = 2.5V, $-V_{REF}$ = -2.5V

DC CHARACTERISTICS

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
R_{INAS}	Analog Input Resistance During Sampling		2		kΩ	2
R_{INANS}	Analog Input Resistance Non-Sampling		100		MΩ	
C_{INA}	Analog Input Capacitance		150	250	pF	

DC CHARACTERISTICS CONTINUED

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
$V_{OFFSET/I}$	Analog Input Offset Voltage		±1	± 8	mV	
R_{OUTA}	Analog Output Resistance		20	50	Ω	
I_{OUTA}	Analog Output Current	0.25	0.5		mA	
$V_{OFFSET/O}$	Analog Output Offset Voltage		-200	± 850	mV	
I_{INLOW}	Logic Input Low Current (V_{IN} = 0.8V) Digital Input, Clock Input, Sync Input		± 0.1	±10	μA	3
I_{INHIGH}	Logic Input High Current (V_{IN} = 2.4V) Digital Input, Clock Input, Sync Input		-0.25	-0.8	mA	3
C_{DO}	Digital Output Capacitance		8	12	pF	
I_{DOL}	Digital Output Leakage Current		± 0.1	±10	μA	
V_{OUTLOW}	Logic Output Low Voltage Digital Output, A/B Signal Out			0.4	V	4
$V_{OUTHIGH}$	Logic Output High Voltage Digital Output, A/B Signal Out	3.9			V	4
I+	Positive Supply Current		4	10	mA	
I–	Negative Supply Current		2	6	mA	
I_{REF+}	Positive Reference Current		4	20	μA	
I_{REF-}	Negative Reference Current		4	20	μA	

AC CHARACTERISTICS (Refer to Figure 12 and Figure 13)

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
F_M	Master Clock Frequency	1.5	1.544	2.1	MHz	
F_R, F_X	Receive, Transmit Clock Frequency	0.064	1.544	2.1	MHz	
PW_{CLK}	Clock Pulse Width (MASTER, XMIT, RCV.)	200			ns	
t_{RC}	Clock Rise Time (MASTER, XMIT, RCV.)			25% of PW_{CLK}	ns	
t_{RS},t_{FS}	Sync Fall, Rise Time (XMIT, RCV.)			25% of PW_{CLK}	ns	
$t_{DIR}$$t_{DIF}$	Digital Input Rise, Fall Time			25% of PW_{CLK}	ns	
t_{WSX}, t_{WSR}	Sync Pulse Width (XMIT, RCV.)		$\frac{8}{F_X(F_R)}$		μs	
t_{PS}	Sync Pulse Period (XMIT, RCV.)		125		μs	
t_{XCS}	XMIT Clock-to-XMIT Sync Delay	50%of t_{FC} t_{RS})			ns	6
t_{XCSN}	XMIT Clock-to-XMIT Sync (Negative Edge) Delay	200			ns	
t_{XSS}	XMIT Sync Set-Up Time	200			ns	
t_{XDD}	XMIT Data Delay	0		200	ns	4
t_{XDP}	XMIT Data Present	0		200	ns	4
t_{XDT}	XMIT Data Three State			150	ns	4
t_{DOF}	Digital Output Fall Time		50		ns	4
t_{DOR}	Digital Output Rise Time		50		ns	4

AC CHARACTERISTICS CONTINUED (Refer to Figure 12 and Figure 13)

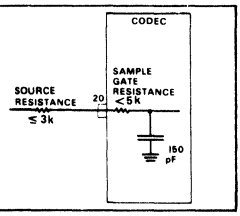
SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
t_{SRC}	RCV. Sync-to-RCV. Clock Delay	50% of t_{RC} (t_{FS})			ns	6
t_{RDS}	RCV. Data Set-Up Time	50			ns	5
t_{RDH}	RCV. Data Hold Time	200			ns	5
t_{RCS}	RCV. Clock-to-RCV. Sync Delay	200			ns	
t_{RSS}	RCV. Sync Set-Up Time	200			ns	5
t_{SAO}	RCV. Sync-to-Analog Output Delay		7		μs	
$t_{A/BI}$	A/B Signalling Input Setup Time			200	ns	
$t_{A/BSH}$	A/B Select Hold Time	200			ns	
$t_{A/BSS}$	A/B Select Setup Time	400			ns	
$t_{A/BO}$	A/B Signalling Output Delay		200	300	ns	
SLEW+	Analog Output Positive Slew Rate		1		V/μs	
SLEW-	Analog Output Negative Slew Rate		1		V/μs	
DROOP	Analog Output Droop Rate		25		μV/μs	

SYSTEM CHARACTERISTICS (Refer to Figures 16 and 17)

SYM	PARAMETER	MIN	TYP	MAX	UNITS	TEST COND.
S/D	Signal-to-Distortion Ratio	35 29 24	39 34 29		dB dB dB	Analog Input=0 to -30dBm0 Analog Input=-40dBm0 Analog Input=-45dm0
GT	Gain Tracking	-0.4 -0.8 -2.5	±0.1 ±0.1 ±0.2	+0.4 +0.8 +2.5	dB dB dB	Analog Input=+3 to -37dBm0 Analog Input=-37 to -50dBm0 Analog Input=-50 to -55dBm0
N_{IC}	Idle Channel Noise		10	18	dBrnc0	Analog Input=0 Volts
TLP	Transmission Level Point		+4		dB	600Ω

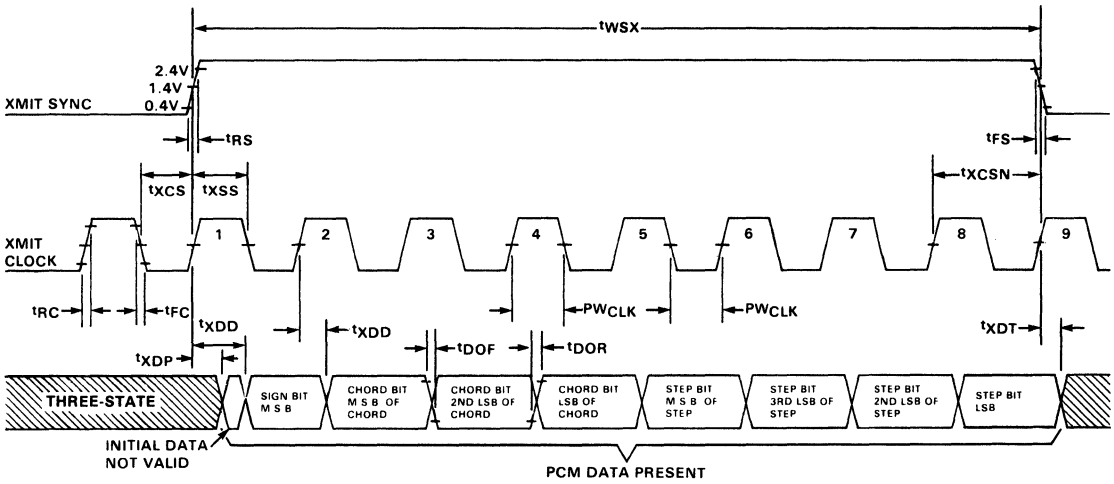
NOTES:
1. $+V_{REF}$ and $-V_{REF}$ must be matched within ± 1% in order to meet system requirements.
2. Sampling is accomplished by charging the internal capacitor to within ½ LSB (≤ 300μV) in 20μs. Therefore, the external source resistance must be 3k or less. The equivalent circuit during sampling is shown in Figure 11.
3. The MK5151 will source current through an internal 6kΩ resistor to help pull up the TTL output. When a transistion from a "1" to a "0" takes place, the user must sink the "1" current until reaching the "0" level.
4. Driving one 74L or 74LS TTL load plus 30pF with I_{OH} = -100μA, I_{OL} = 500μA.
5. The first bit of data is loaded when Sync and Clock are both "1" during bit time 1 as shown on RCV timing diagram.
6. This delay is necessary to avoid overlapping CLOCK and SYNC.

Equivalent Input Resistance Circuit During Sampling
Figure 11



TRANSMITTER SECTION TIMING

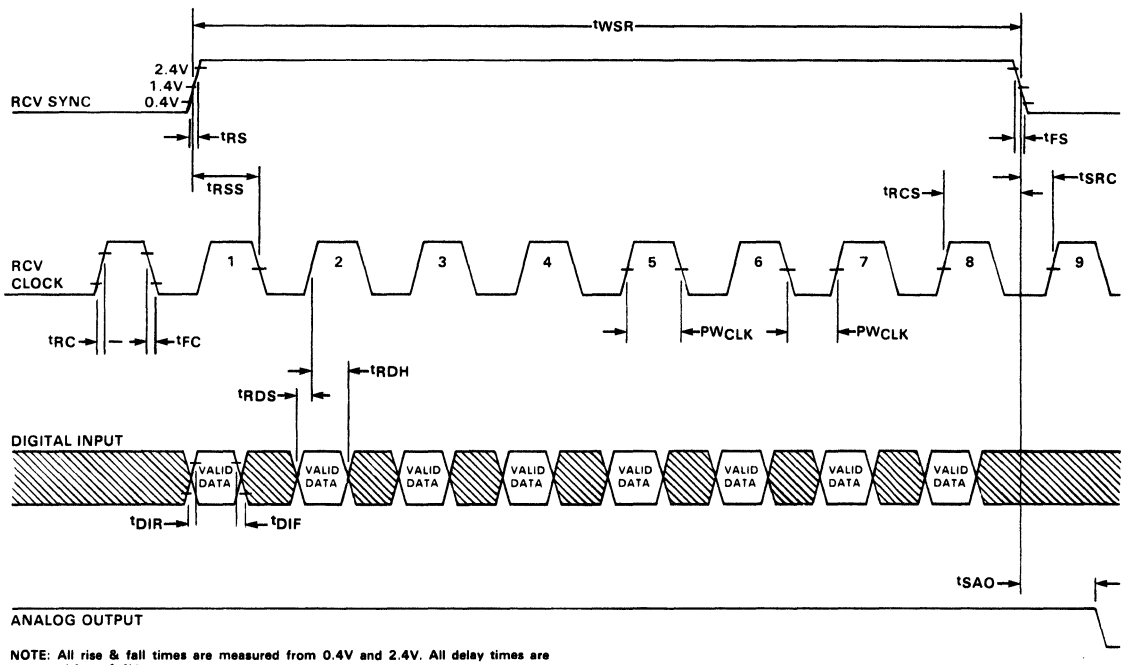
Figure 12



NOTE: All rise and fall times are measured from 0.4V and 2.4V.
All delay times are measured from 1.4V.

RECEIVER SECTION TIMING

Figure 13

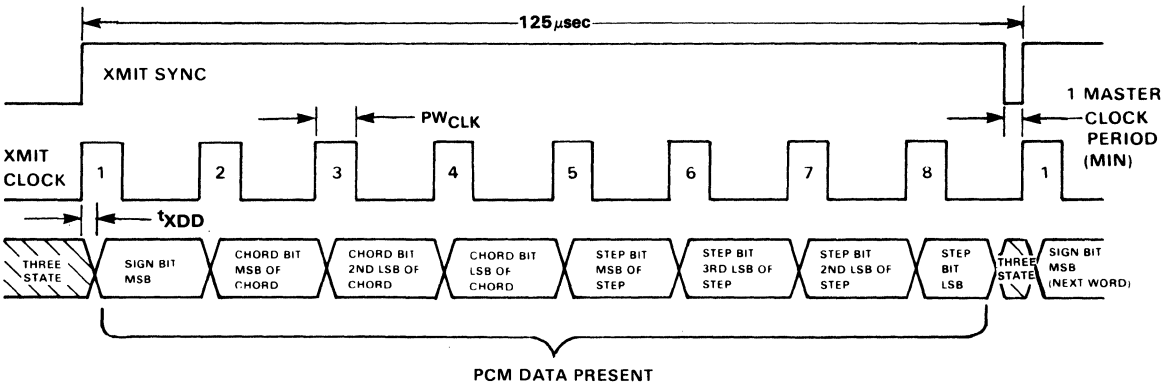


NOTE: All rise & fall times are measured from 0.4V and 2.4V. All delay times are measured from 1.4V.

VII CODECs

64kHz OPERATION, TRANSMITTER SECTION TIMING

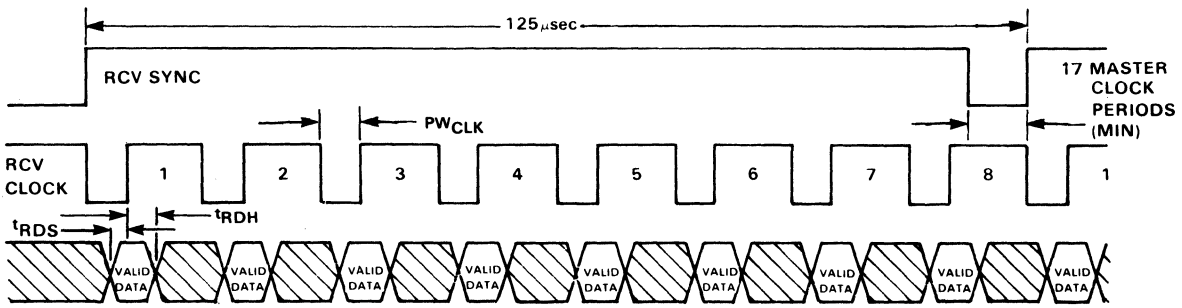
Figure 14



NOTE: All rise and fall times are measured from 0.4V and 2.4V. All delay times are measured from 1.4V.

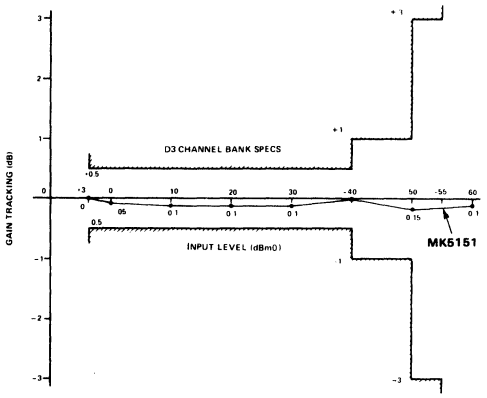
64kHz OPERATION, RECEIVER SECTION TIMING

Figure 15

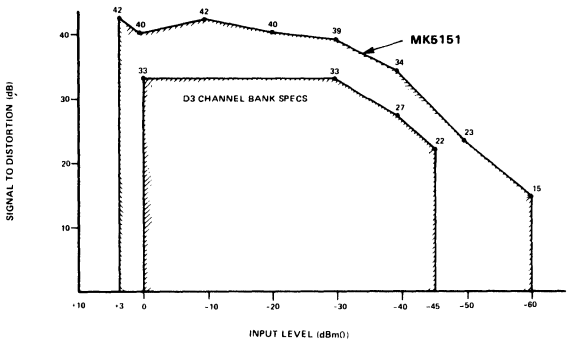


NOTE: All rise and fall times are measured from 0.4V and 2.4V. All delay times are measured from 1.4V.

MK5151 GAIN TRACKING PERFORMANCE
Figure 16



MK5151 S/D RATIO VS. INPUT LEVEL
Figure 17



PRELIMINARY

MOSTEK®

A-LAW COMPANDING CODEC

MK5156

FEATURES

- ±5-Volt Power Supplies
- Low Power Dissipation - 30mW (Typ)
- Follows the A-Law Companding Code
- Exceeds CCITT Specifications, Includes Even-Order-Bit Inversion
- Synchronous or Asynchronous Operation
- On-Chip Sample and Hold
- On-Chip Offset Null Circuit Eliminates Long-Term Drift Errors and Need for Trimming
- Single 16-Pin Package
- Minimal External Circuitry Required
- Serial Data Output of 64kb/s-2.1 Mb/s at 8kHz Sampling Rate
- Separate Analog and Digital Grounding Pins Reduce System Noise Problems

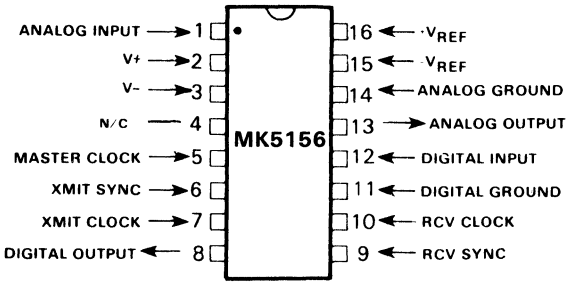
DESCRIPTION

The MK5156 is a monolithic CMOS companding CODEC which contains two sections: (1) An analog-to-digital converter which has a transfer characteristic conforming to the A-law companding code and (2) a digital-to-analog converter which also conforms to the A-law code.

These two sections form a coder-decoder which is designed to meet the needs of the telecommunications industry for per-channel voice-frequency codecs used in PCM systems. Digital input and output are in serial format. Actual transmission and reception of 8-bit data words containing the analog information is done at a 64kb/s-2.1Mb/s rate with analog signal sampling occuring at an 8kHz rate. A sync pulse input is provided for synchronizing transmission and reception of multi-channel information being multiplexed over a single transmission line.

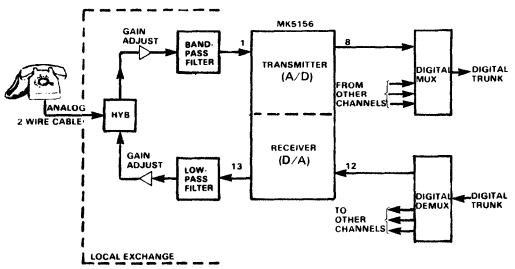
The pin configuration of the MK5156 is shown in Figure 1.

PIN CONNECTIONS
Figure 1



A block diagram of a PCM system using the MK5156 is shown in Figure 2.

PCM SYSTEM BLOCK DIAGRAM
Figure 2

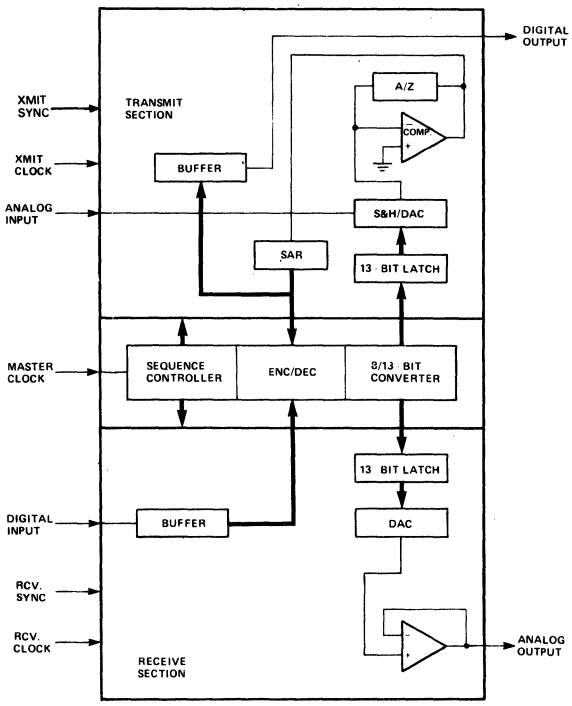


VII CODECs

FUNCTIONAL DESCRIPTION: (Refer to Figure 3 for a Block Diagram)

MK5156 BLOCK DIAGRAM

Figure 3



POSITIVE AND NEGATIVE REFERENCE VOLTAGES ($+V_{REF}$ and $-V_{REF}$) Pins 16 and 15

These inputs provide the conversion references for the digital-to-analog converters in the MK5156. $+V_{REF}$ and $-V_{REF}$ must maintain 100ppM/°C regulation over the operating temperature range. Variation of the reference directly affects system gain.

ANALOG INPUT, Pin 1

Voice-frequency analog signals which are bandwidth-limited to 4kHz are input at this pin. Typically, they are then sampled at an 8kHz rate (Refer to Figure 4.). The analog input must remain between $+V_{REF}$ and $-V_{REF}$ for accurate conversion.

MASTER CLOCK, Pin 5

This signal provides the basic timing and control signals required for all internal conversions. It does not have to be synchronized with RCV. SYNC, RCV. CLOCK, XMIT SYNC or XMIT CLOCK and is not internally related to them.

XMIT SYNC, Pin 6 (Refer to Figure 10 for the Timing Diagram)

This input is synchronized with XMIT CLOCK. When XMIT SYNC goes high, the digital output is activated and the A/D conversion begins on the next positive edge of MASTER CLOCK. The conversion by MASTER CLOCK can be asynchronous with XMIT CLOCK. The serial output data is clocked out by the positive edges of XMIT CLOCK. The negative edge of XMIT SYNC causes the digital output to become three-state. XMIT SYNC must go low for at least 1 master clock prior to the transmission of the next digital word (Refer to Figure 12).

XMIT CLOCK, Pin 7 (Refer to Figure 10 for the Timing Diagram)

The on-chip 8-bit output shift register of the MK5156 is unloaded at the clock rate present on this pin. Clock rates of 64kHz-2.1MHz can be used for XMIT CLOCK. The positive edge of the INTERNAL CLOCK transfers the data from the master to the slave of a master-slave flip-flop (Refer to Figure 5). If the positive edge of XMIT SYNC occurs after the positive edge of XMIT CLOCK, XMIT SYNC will determine when the first positive edge of INTERNAL CLOCK will occur. In this event, the hold time for the first clock pulse is measured from the positive edge of XMIT SYNC.

RCV. SYNC, Pin 9 (Refer to Figure 11 for the timing diagram)

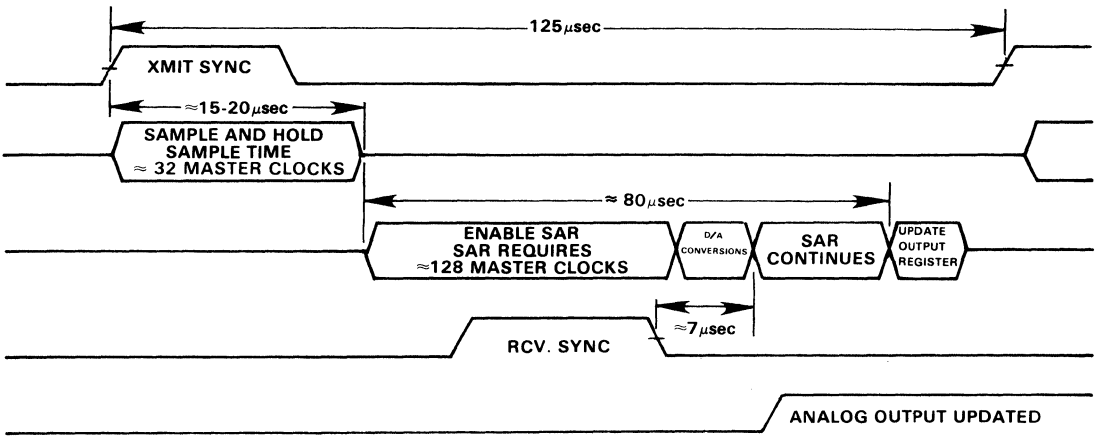
This input is synchronized with RCV. CLOCK and serial data is clocked in by RCV. CLOCK. Duration of the RCV SYNC pulse is approximately 8 RCV. CLOCK periods. The conversion from digital-to-analog starts after the negative edge of the RCV. SYNC pulse (Refer to Figure 4). The negative edge of RCV. SYNC should occur before the 9th positive clock edge to insure that only eight bits are clocked in. RCV. SYNC must stay low for 17 MASTER CLOCKS (min.) before the next digital word is to be received (Refer to Figure 13).

RCV CLOCK, Pin 10 (Refer to Figure 11 for Timing Diagram)

The on-chip 8-bit shift register for the MK5156 is loaded at the clock rate present on this pin. Clock rates of 64kHz-2.1MHz can be used for RCV. CLOCK. Valid data should be applied to the digital input before the positive edge of the internal clock (Refer to Figure 5). This set up time, t_{RDS}, allows the data to be transferred into the MASTER of a master-slave flip-flop. The positive edge of the INTERNAL CLOCK transfers the data to the SLAVE of the master-slave flip-flop. A hold time, t_{RDH}, is required to complete this transfer. If the rising edge of RCV. SYNC occurs after the first rising edge of RCV. CLOCK, RCV. SYNC will determine when the first positive edge of INTERNAL CLOCK will occur. In

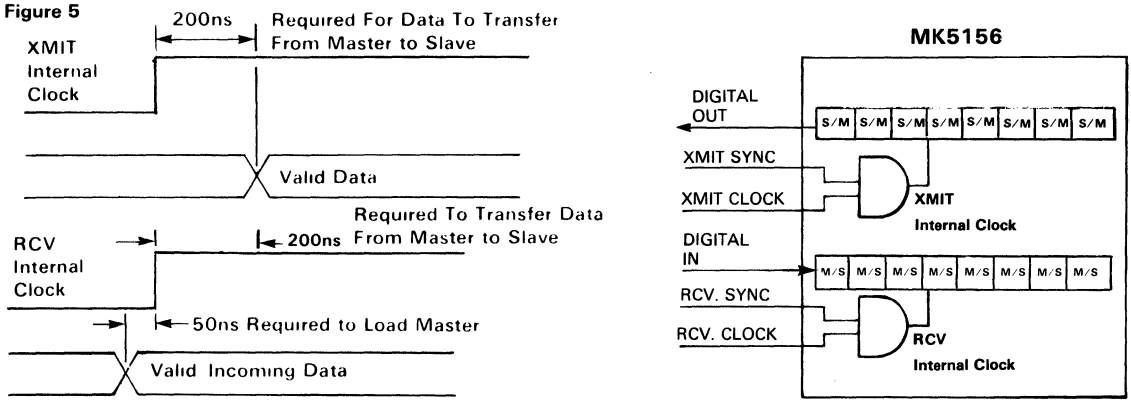
A/D, D/A CONVERSION TIMING

Figure 4



DATA INPUT/OUTPUT TIMING

Figure 5



this event, the set-up and hold times for the first clock pulse should be measured from the positive edge of RCV. SYNC.

DIGITAL OUTPUT, Pin 8

The MK5156 output register stores the 8-bit encoded sample of the analog input. This 8-bit word is shifted out under control of XMIT SYNC and XMIT CLOCK. When XMIT SYNC is low, the DIGITAL OUTPUT is an open circuit. When XMIT SYNC is high, the state of the DIGITAL OUTPUT is determined by the value of the output bit in the serial shift register. The output is composed of a Sign Bit, 3 Chord Bits, and 4 Step Bits. The Sign Bit indicates the polarity of the analog input while the Chord and Step Bits indicate the magnitude. In the first two Chords, the Step Bit has a value of 1.2mV. In the third Chord, the Step Bit has a value of 2.4mV. This doubling of the step value continues for each of the five successive Chords.

Each Chord has a specific value and the Step Bits, 16 in each Chord, specify the displacement from that value (Refer to Table 1). Thus the output, which follows the A law, has resolution that is proportional to the input level rather than to full scale. This provides the resolution of a 12-bit A/D converter at low input levels and that of a 6-bit converter as the input approaches full scale. The transfer characteristic of the A/D converter (A-law Encoder) is shown in Figure 6.

DIGITAL INPUT, Pin 12

The MK5156 input register accepts the 8-bit sample of an analog value and loads it under control of RCV. SYNC and RCV. CLOCK. The timing diagram is shown in Figure 11. When RCV. SYNC goes high, the MK5156 uses RCV. CLOCK to clock the serial data into its input register. RCV. SYNC goes low to indicate the end of serial input data. The 8 bits of the input data have the same functions described for the DIGITAL OUTPUT. The

DIGITAL OUTPUT CODE: A LAW

Table 1

	Chord Code	Chord Value	Step Value
1.	101	0.0mV	1.221mV
2.	100	20.1mV	1.221mV
3.	111	40.3mV	2.44mV
4.	110	80.6mV	4.88mV
5.	001	161.1mV	9.77mV
6.	000	332mV	19.53mV
7.	011	645mV	39.1mV
8.	010	1.289V	78.1mV

EXAMPLE:

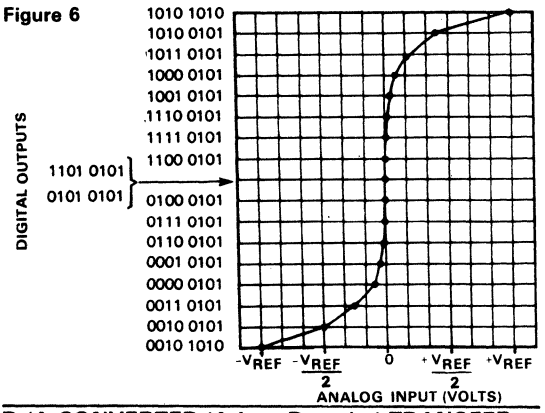
1 110 0111= +80.6mV+ (2 x 4.88mV)

Sign Bit Chord Step Bits

If the sign bit were a zero, then both plus signs would be changed to minus signs.

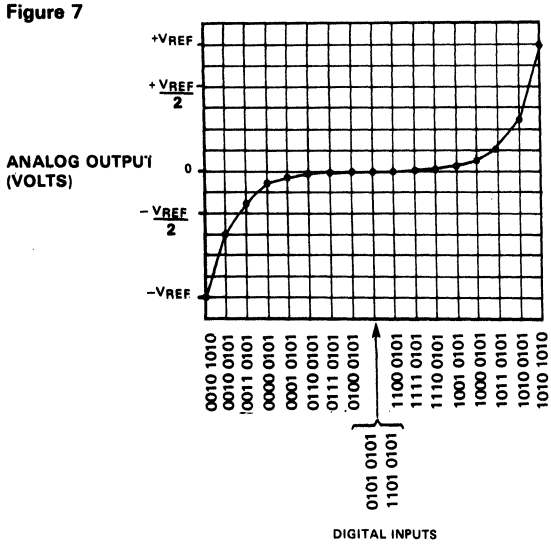
A/D CONVERTER (A-Law Encoder) TRANSFER CHARACTERISTIC

Figure 6



D/A CONVERTER (A-Law Decoder) TRANSFER CHARACTERISTIC

Figure 7



transfer characteristic of the D/A converter (A-law Decoder) is shown in Figure 7.

ANALOG OUTPUT, Pin 13

The analog output is in the form of voltage steps (100% duty cycle) having amplitude equal to the analog sample which was encoded. This waveform is then filtered with an external low-pass filter with sinx/x correction to recreate the sampled voice signal.

OPERATION OF CODEC WITH 64kHz XMIT/RCV. CLOCK FREQUENCIES

XMIT/RCV. SYNC must not be allowed to remain at a logic "1" state. XMIT SYNC is required to be at a logic "0" state for 1 master clock period (min.) before the next digital word is transmitted. RCV. SYNC is required to be at a logic "0" state for 17 master clock periods (min.) before the next digital word is received (Refer to Figures 12 and 13).

OFFSET NULL

The offset null feature of the MK5156 eliminates long-term drift errors and conversion errors due to temperature changes by going through an offset adjustment cycle before every conversion, thus guaranteeing accurate A/D conversion for inputs near ground. There is no offset adjust of the output amplifier because, since the output is intended to be AC - coupled to the external filter, the resultant DC error ($V_{OFFSET/O}$) will have no effect. The sign bit is not used to null the analog input. Therefore, for an analog input of 0 volts, the sign bit will be stable.

PERFORMANCE EVALUATION

The equipment connections shown in Figure 8 can be used to evaluate the performance of the MK5156. An analog signal provided by the HP3552A Transmission Test Set is connected to the Analog Input (Pin 1) of the MK5156. The Digital Output of the CODEC is tied back to the Digital Input and the Analog Output is fed through a low-pass filter to the HP3552A. Remaining pins of the MK5156 are connected as follows:

(1) RCV. SYNC is tied to XMIT SYNC
(2) XMIT CLOCK is tied to MASTER CLOCK. The signal is inverted and tied to RCV. CLOCK.

The following timing signals are required:

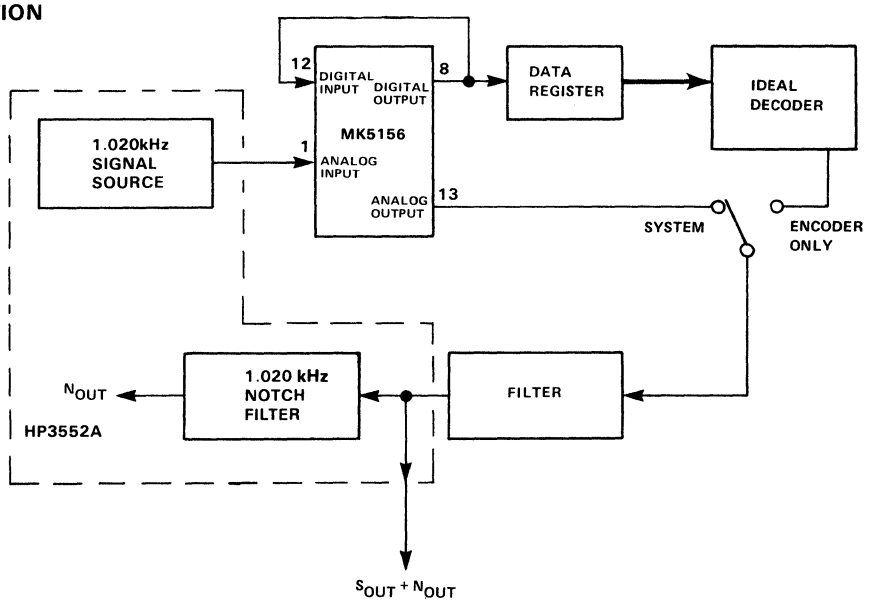
(1) MASTER CLOCK = 2.048MHz
(2) XMIT SYNC repetition rate = 8kHz
(3) XMIT SYNC width = 8 XMIT CLOCK periods

When all the above requirements are met, the setup of Figure 8 permits the measurement of synchronous system performance over a wide range of analog inputs.

The data register and ideal decoder provide a means of checking the encoder portion of the MK5156 independently of the decoder section. To test the system in the asynchronous mode, MASTER CLOCK should be separated from XMIT CLOCK and MASTER CLOCK should be separated from RCV. CLOCK. XMIT CLOCK and RCV. CLOCK are separated also. Some experimental results obtained with the MK5156 are shown in Figures 14 and 15.

SYSTEM CHARACTERISTICS TEST CONFIGURATION

Figure 8



NOTE: The ideal decoder consists of a digital decompander and a 13-bit precision DAC.

ABSOLUTE MAXIMUM RATINGS

DC Supply Voltage, V+ ..... +6V
DC Supply Voltage, V– ..... -6V
Operating Temperature ..... 0°C to 70°C
Storage Temperature ..... -55°C to +125°C
Package Dissipation at 25°C (Derated 9mW/°C when soldered into PCB) 500mW
Digital Input ..... $-0.5V \leq V_{IN} \leq V+$
Analog Input ..... $V- \leq V_{IN} \leq V+$
$+V_{REF}$ ..... $-0.5V \leq +V_{REF} \leq V+$
$-V_{REF}$ ..... $V- \leq -V_{REF} \geq +0.5V$

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL OPERATING CHARACTERISTICS
POWER SUPPLY REQUIREMENTS

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V+	Positive Supply Voltage	4.75	5.0	5.25	V	
V–	Negative Supply Voltage	-5.25	-5.0	-4.75	V	
$+V_{REF}$	Positive Reference Voltage	2.375	2.5	2.625	V	1
$-V_{REF}$	Negative Reference Voltage	-2.625	-2.5	-2.375	V	1

TEST CONDITIONS: V+ = 5.0V, V– = -5.0V,+ V_{REF} = 2.5V, $-V_{REF}$ = -2.5V

DC CHARACTERISTICS

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
R_{INAS}	Analog Input Resistance During Sampling		2		kΩ	2
R_{INANS}	Analog Input Resistance Non-Sampling		100		MΩ	
C_{INA}	Analog Input Capacitance		150	250	pF	
$V_{OFFSET/I}$	Analog Input Offset Voltage		±1	± 8	mV	
R_{OUTA}	Analog Output Resistance		20	50	Ω	
I_{OUTA}	Analog Output Current	0.25	0.5		mA	
$(V_{OFFSET/O})$	Analog Output Offset Voltage		-200	± 850	mV	
I_{INLOW}	Logic Input Low Current (V_{IN} = 0.8V) Digital Input, Clock Input, Sync Input		± 0.1	±10	μA	3
I_{INHIGH}	Logic Input High Current (V_{IN} = 2.4V) Digital Input, Clock Input, Sync Input		-0.25	-0.8	mA	3
C_{DO}	Digital Output Capacitance		8	12	pF	
I_{DOL}	Digital Output Leakage Current		± 0.1	±10	μA	
V_{OUTLOW}	Digital Output Low Voltage			0.4	V	4
$V_{OUTHIGH}$	Digital Output High Voltage	3.9			V	4
I+	Positive Supply Current		4	10	mA	
I–	Negative Supply Current		2	6	mA	
I_{REF+}	Positive Reference Current		4	20	μA	
I_{REF-}	Negative Reference Current		4	20	μA	

AC CHARACTERISTICS (Refer to Figure 10 and Figure 11)

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
F_M	Master Clock Frequency	1.5	2.048	2.1	MHz	
F_R, F_X	XMIT, RCV. Clock Frequency	0.064	2.048	2.1	MHz	
PW_{CLK}	Clock Pulse Width (MASTER, XMIT, RCV.)	200			ns	
t_{RC}, t_{FC}	Clock Rise, Fall Time (MASTER, XMIT, RCV.)			25% of PW_{CLK}	ns	
t_{RS},t_{FS}	Sync Rise, Fall Time (XMIT, RCV.)			25% of PW_{CLK}	ns	
t_{DIR},t_{DIF}	Data Input Rise, Fall Time			25% of PW_{CLK}	ns	
t_{WSX}, t_{WSR}	Sync Pulse Width (XMIT, RCV.)		$\frac{8}{F_X(F_R)}$		μs	
t_{PS}	Sync Pulse Period (XMIT, RCV.)		125		μs	
t_{XCS}	XMIT Clock-to-XMIT Sync Delay	50% of t_{FC}(t_{RS})			ns	6
t_{XCSN}	XMIT Clock-to-XMIT Sync (Negative Edge) Delay	200			ns	

AC CHARACTERISTICS CONTINUED (Refer to Figure 10 and Figure 11)

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
t_{XSS}	XMIT Sync Set-Up Time	200			ns	
t_{XDD}	XMIT Data Delay	0		200	ns	4
t_{XDP}	XMIT Data Present	0		200	ns	4
t_{XDT}	XMIT Data Three State			150	ns	4
t_{DOF}	Digital Output Fall Time		50		ns	4
t_{DOR}	Digital Output Rise Time		50		ns	4
t_{SRC}	RCV. Sync-to-RCV. Clock Delay	50% of t_{RC} (t_{FS})			ns	6
t_{RDS}	RCV. Data Set-Up Time	50			ns	5
t_{RDH}	RCV. Data Hold Time	200			ns	5
t_{RCS}	RCV. Clock-to-RCV. Sync Delay	200			ns	
t_{RSS}	RCV. Sync Set-Up Time	200			ns	5
t_{SAO}	RCV. Sync-to-Analog Output Delay		7		μs	
SLEW+	Analog Output Positive Slew Rate		1		V/μs	
SLEW–	Analog Output Negative Slew Rate		1		V/μs	
DROOP	Analog Output Droop Rate		25		μV/μs	

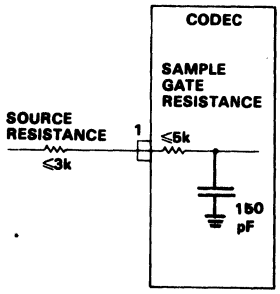
SYSTEM CHARACTERISTICS (Refer to Figures 14 and 15)

SYM	PARAMETER	MIN	TYP	MAX	UNITS	TEST COND.
S/D	Signal-to-Distortion Ratio	35 29 24	39 34 29		dB dB dB	Analog Input=0 to -30dBm0 Analog Input=-40dBm0 Analog Input=-45dm0
GT	Gain Tracking	-0.4 -0.8 -2.5	±0.1 ±0.1 ±0.2	+0.4 +0.8 +2.5	dB dB dB	Analog Input=+3 to -37dBm0 Analog Input=-37 to -50dBm0 Analog Input=-50 to -55dBm0
N_{IC}	Idle Channel Noise		-80	-72	dBm0p	Analog Input=0 Volts
TLP	Transmission Level Point		+4		dB	600Ω

NOTES:
1. $+V_{REF}$ and $-V_{REF}$ must be matched within ±1% in order to meet system requirements.
2. Sampling is accomplished by charging the internal capacitor to within ½ LSB (≤300μV) in 20μs. Therefore, the external source resistance must be 3k or less. The equivalent circuit during sampling is shown in Figure 9.
3. The MK5156 will source current through an internal 6kΩ resistor to help pull up the TTL output. When a transition from a "1" to a "0" takes place, the user must sink the "1" current until reaching the "0" level.
4. Driving one 74L or 74LS TTL load plus 30pF with I_{OH} = -100μA, I_{OL} = 500μA.
5. The first bit of data is loaded when Sync and Clock are both "1" during bit time 1 as shown on RCV. timing diagram.
6. This delay is necessary to avoid overlapping Clock and Sync.

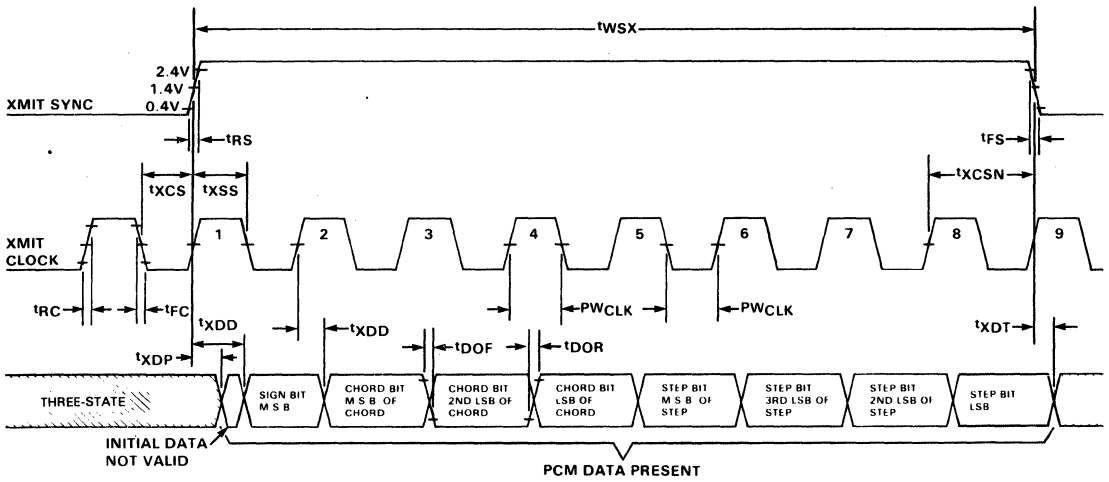
EQUIVALENT INPUT RESISTANCE CIRCUIT DURING SAMPLING

Figure 9



TRANSMITTER SECTION TIMING

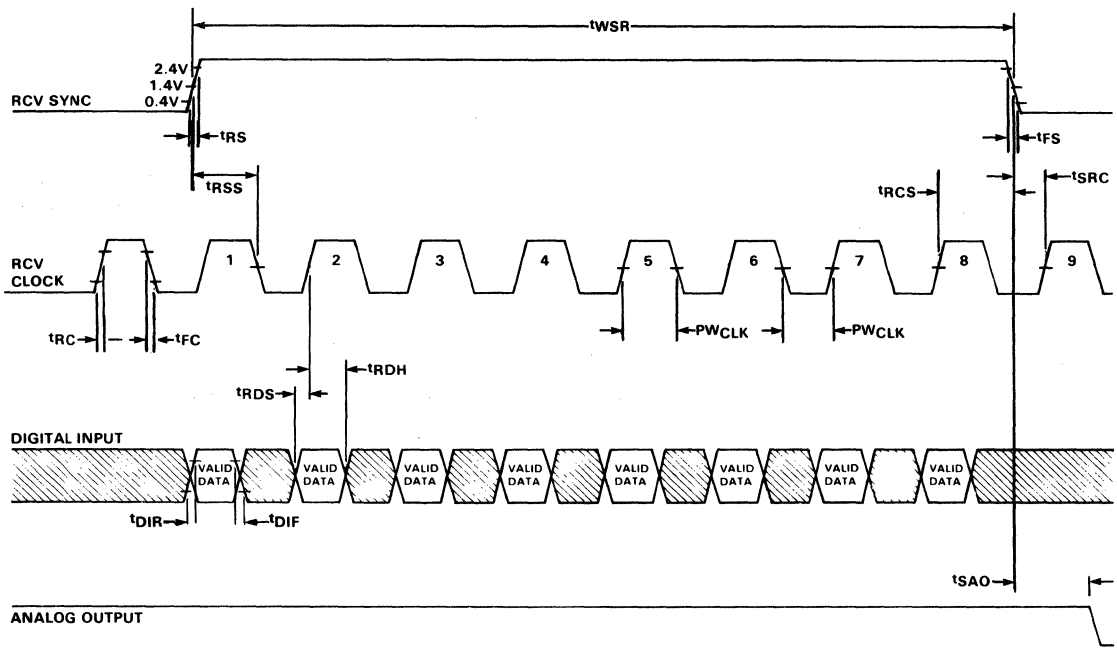
Figure 10



NOTE: All rise and fall times are measured from 0.4V and 2.4V. All delay times are measured from 1.4V.

RECEIVER SECTION TIMING

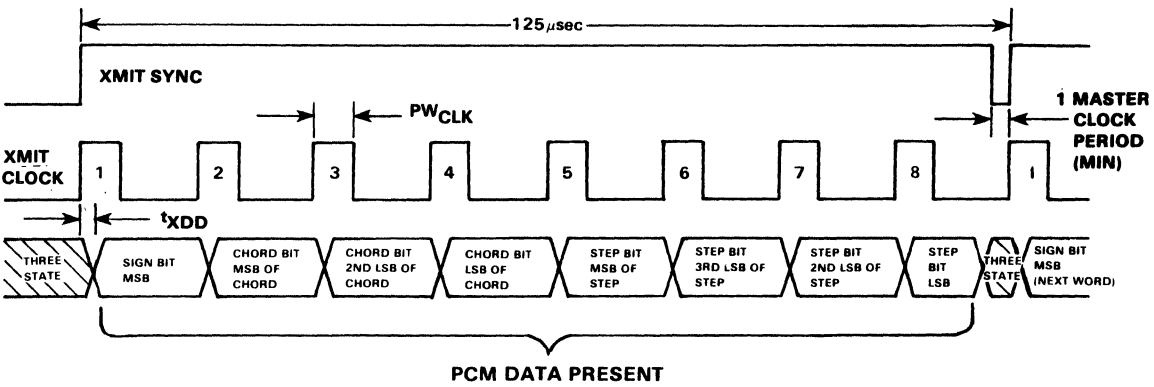
Section 11



NOTE: All rise and fall times are measured from 0.4V and 2.4V. All delay times are measured from 1.4V.

64kHz OPERATION, TRANSMITTER SECTION TIMING

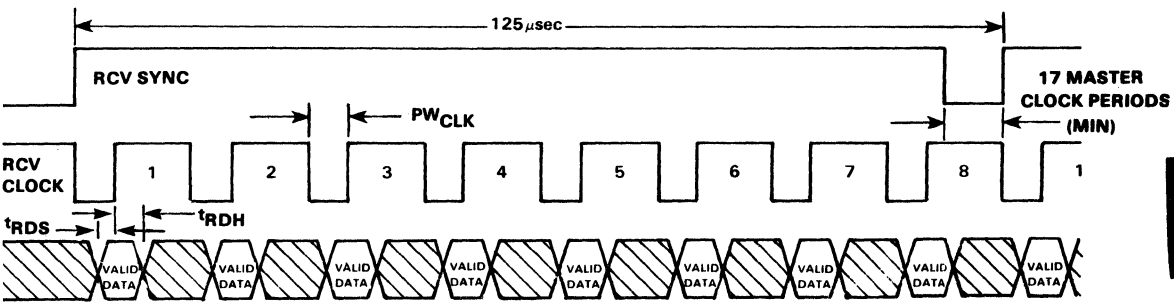
Figure 12



NOTE: All rise and fall times are measured from 0.4V and 2.4V. All delay times are measured from 1.4V.

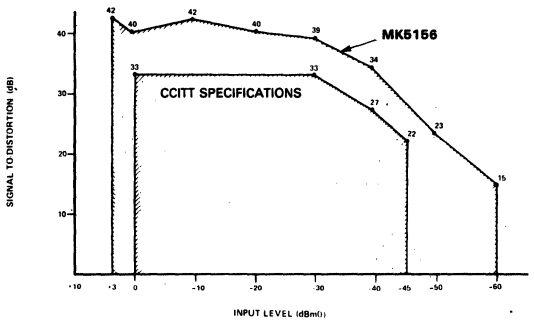
64kHz OPERATION, RECEIVER SECTION TIMING

Figure 13

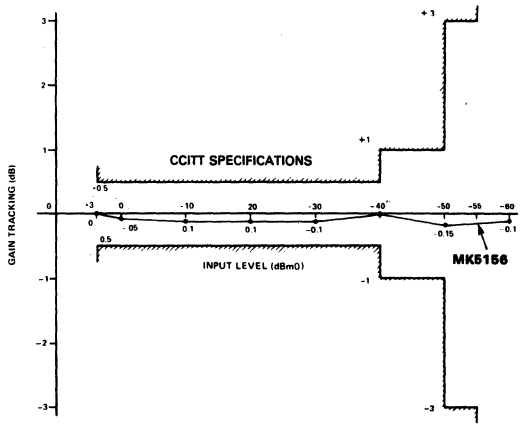


NOTE: All rise and fall times are measured from 0.4V and 2.4V. All delay times are measured from 1.4V.

MK5156 S/D RATIO VS. INPUT LEVEL
Figure 14



M5156 GAIN TRACKING PERFORMANCE
Figure 15



MOSTEK®

μ-255 LAW COMPANDING CODEC AND FILTERS

MK5300

DESCRIPTION

The MK5300 is a monolithic device containing both transmit and receive filters and a μ-255 companding CODEC on a single chip. The transmit section of the MK5300 is composed of an input op amp, a band-pass filter, and an A/D converter. The receive section of the MK5300 is composed of a D/A converter, a low-pass filter, and power driver amplifiers.

The MK5300 features a microcomputer mode which provides on-chip time slot computation. A direct mode is also provided in order to directly control the CODEC by control data input. The transmit, receive, and control sections may be operated synchronously or asynchronously. The MK5300 also features a stable on-chip voltage reference to provide accurate A/D and D/A conversions.

INTRODUCTION

A general trend towards the conversion of voice signals to digital information is currently occurring. TDM PCM is the most popular form of digital transmission.

Today there are several important applications for this TDM scheme:

1. A high speed digital data link between central offices to pass many conversations over one pair of wires.
2. The electronic connection of two different circuit paths.
3. Concentrators

Traditionally this connection had been done by electromechanical crossreed switches. Very low "on" resistance, low crosstalk, and immunity from the large ringing or transient voltages were required. Since the electromechanical technique was deemed to be of lower reliability, an all electronic approach was desired. Electronic cross point switches were designed and built, but because the electrical requirements mentioned above are extremely difficult to meet, the results were not entirely satisfying.

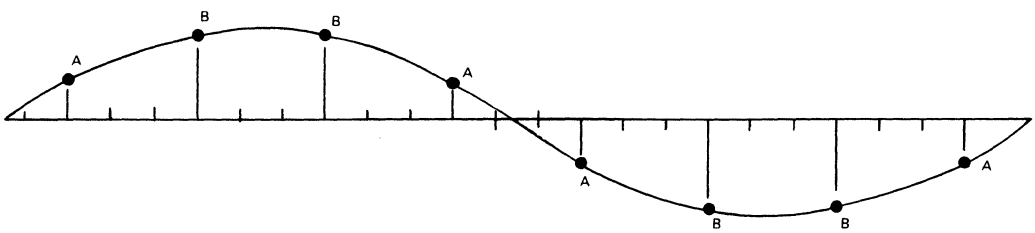
The digital approach obviates the analog switch problem by first performing an A to D conversion, then assigning a time slot for each voice channel. For the D3 channel bank, 24 channels of digital data of 8 bits per word are transmitted in a serial bit stream at 1.544 Mbits/sec. Each voice channel is sampled at an 8kHz rate so this signal must be bandlimited to less than 4kHz in order to prevent undesirable aliasing.

Figure 1 shows how a 1kHz input signal is sampled every 125 μsec. At each of these sampling times, the analog information is converted into an eight-bit digital word that is later sent out in serial format at the 1.544 Mbits/sec rate.

Figure 2 shows how the 24 voice channels are time division multiplexed onto one wire (for simplicity only simplex operation is shown).

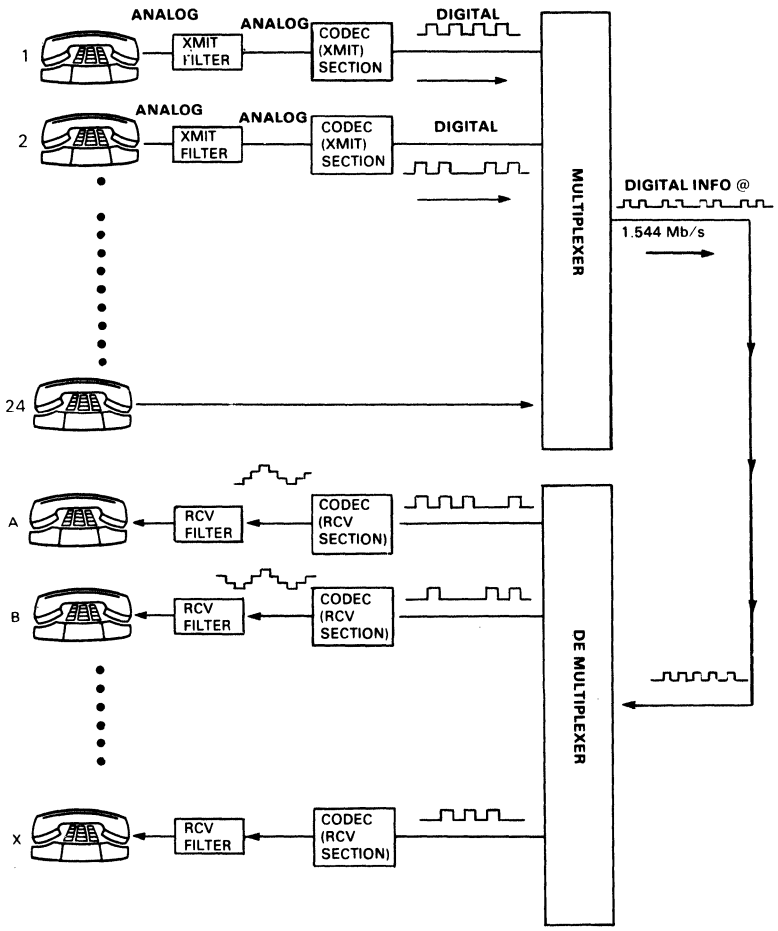
Channel 1 analog information is first bandlimited to less than 4kHz, then sampled and converted to a companded digital code. This 8 bit word is serially transmitted to a multiplexer where digital information from all the other channels are assimalated. The final bit stream of 1.544mbit/sec is sent to the demultiplexer where the appropriate alphanumeric channel is connected to numeric channel. This control (selection) is done by the main computer or processor. One may see that any numeric channel could be connected to any alphanumeric channel by means of a different time slot assignment. This completes the switching in a completely digital manner.

8kHz SAMPLING SYSTEM
Figure 1



24 CHANNEL MULTIPLEXING

Figure 2



For T1 carrier systems, the digital PCM information might be transmitted between central offices. For PBX applications, the PCM technique is used to allow the switching to be done digitally. The accuracy of the subsequent D-A conversion preserves the voice quality so that insertion loss is not a problem.

We selected the metal gate CMOS process for several reasons. First it is extremely low power, which is of great concern. Secondly, it allows for high-quality, matched capacitors in a minimum of chip size. Critical analog circuit design is done well in CMOS: for example, high gain amplifiers and comparators. Also, the metal gate CMOS process is one that is well proven in high volume production.

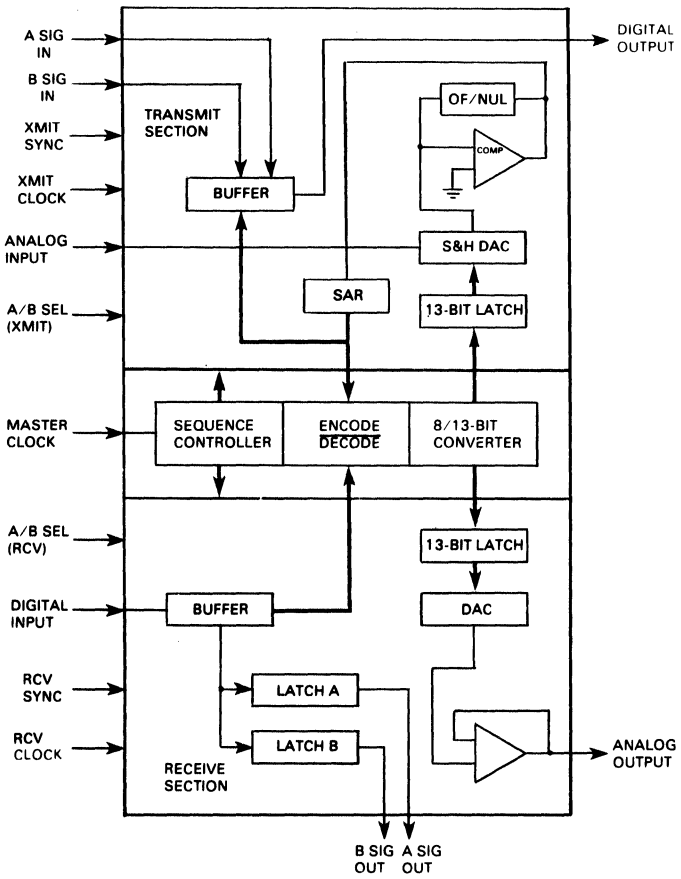
By using the CMOS process, only two supplies are necessary, plus and minus five volts. To minimize power, all the digital logic is run from the plus 5V supply to ground, and only the analog section operates from ± 5 volts.

CHIP ARCHITECTURE

Figure 3 shows the block diagram representation of the CODEC chip. The important features of the scheme used are listed below:

1. Two independent DAC's for encode and decode functions provide system isolation not achievable using shared DAC approach. The capacitive two DAC approach also eliminates external sample/hold capacitors as well as an external filter for offset which is required in the shared DAC approach. This minimizes the external components required.
2. Complete signalling compatibility with D3 channel bank requirements.
3. Since the companding law is implemented using 8 to 13 bit converter, the DAC is a linear DAC thus minimizing the number of analog components to only the minimum required for system implementation, namely two: one comparator and only one op-amp on the entire chip. Minimizing the linear

CODEC BLOCK DIAGRAM
Figure 3



components helps reduce system operating power which was the overriding consideration in chip design. Using the CMOS process, the digital portions dissipate power only during transitions. The linear sections consume power continuously.

4. The digital companding section allows easy conversion from mu-law to A-law. The CODEC allows data input/output rates from 64kHz to 2.1MHz.
5. Asynchronous or synchronous operation.

MODES OF OPERATION

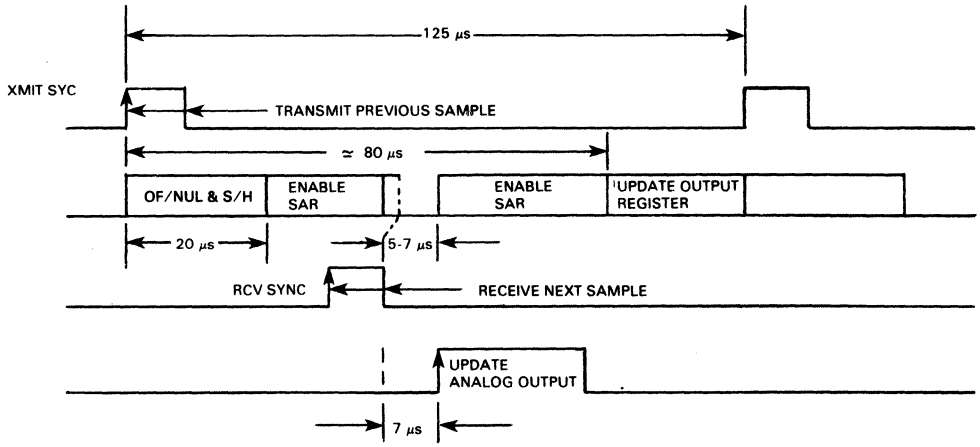
The XMIT and Receive function are completely independent of each other and of the master clock. Thus the chip can operate in synchronous/asynchronous mode at various input/output clock rates. The chip timing diagram is shown in Figure 4 and the Receive and XMIT modes of operation are described in detail below:

(a) Receive Mode of Operation
In the receive mode of operation, the serial input data is shifted into the input buffer at the receive clock rate during the period receive sync. is high. The encode process is halted after the falling edge of receive sync pulse) for about 5 to 7μs, and the translated data from 8 to 13 bit converter is latched into the 13 bit receive latch which updates the output of the receive DAC with 100% duty cycle. The receive DAC acts as a sample and hold and is buffered by the unity gain op amp to the output.
During the signalling frame a 7 bit decode is performed and the 8th data bit is latched into the SigA/SigB output latch as selected by the A/B Select (RCV) input. When the eight bit of a word is a signalling bit, it is assigned the value of ½ step. This results in a lower S/D ratio than if it were arbitrarily set to either a one or zero.

(b) Transmit Mode of Operation:
In this mode of operation the analog signal is sampled in the input sample/hold which performs the offset-null function simultaneously as described in the circuit operation section. Following the hold mode, the encoding process is completed using successive approximation technique. The operation of the XMIT DAC is similar to the operation of the receive DAC as described earlier. After the encode

A/D AND D/A CONVERSION TIMING

Figure 4



process is completed, the output of the SAR is loaded into the output buffer. The data is transmitted serially at the output clock rate during the period the XMIT SYNC is high. During the signalling frame, signalling information (SigA/SigB) is inserted into the output bit stream in place of the 8th data bit as selected by the A/B select (SMIT) input.

CIRCUIT DESCRIPTION

The system timing is controlled by the sequence controller which operates at master clock rate of 1.5 - 2.1 MHz. All necessary signals, e.g. and S&H, SAR clock Encode/Decode control, etc; are generated in this section. To insure proper encode operation, decode interrupt is allowed only when the internal SAR clock is low thus resulting in a variable (5-7 μs) decode interrupt interval.

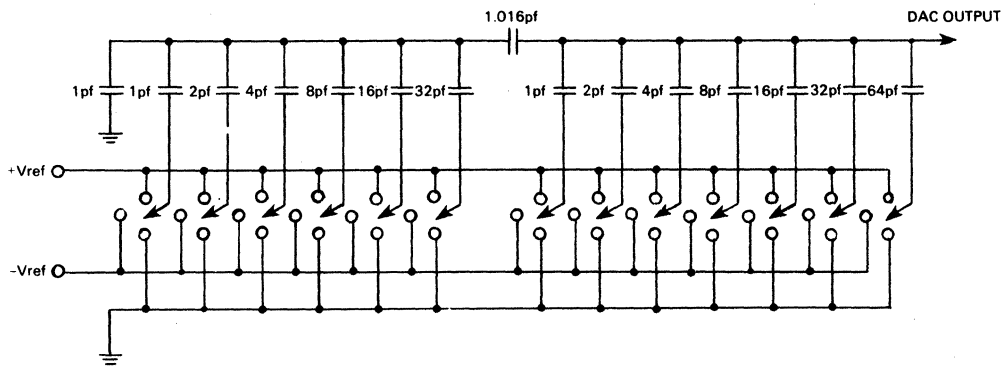
The 8 to 13 bit converter gives a one-to-one translation between 8 bit companded code at its input to a 13 bit linear code at its output thus allowing the use of a linear DAC in the digital-to-analog conversion process.

The 13-bit linear DAC operates on the charge distribution principal of a binary weighted capacitor ladder.

As shown in Figure 5, the capacitor ladder has two sections of 7 bits (7 most significant bits) and 6 bits (6 least significant bits) connected by a 64:1 capacitor divider. The equivalent circuit of the two sections can be drawn as shown in Figure 6.

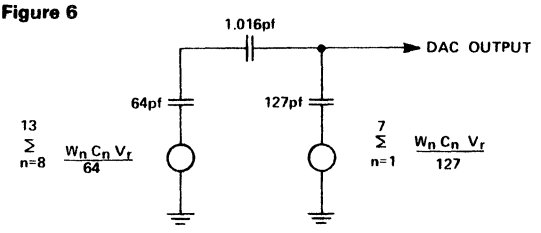
CAPACITOR LADDER

Figure 5



CAPACITOR LADDER EQUIVALENT CIRCUIT

Figure 6



WHERE W_n = 0 or 1 for the n th bit.
C_n = n th bit capacitor.
V_r = Reference Voltage ($+V_{ref}$ or $-V_{ref}$)

The output of the DAC can be written as:

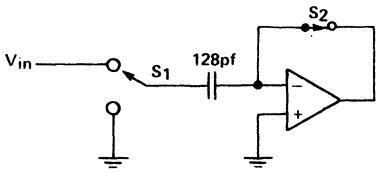
$$V_{DAC} = \frac{V_r}{128}\left[\sum_{n=1}^{7} W_n C_n + \sum_{n=8}^{13} W_n (C_n/64)\right]$$

which is equivalent to the output of a 13 bit DAC with an equivalent output capacitance of 128pF.

In the encode section this equivalent capacitor of 128pF is also employed to perform the additional function of offset-null and sample-hold as shown in Figure 7.

OFFSET NULL/SAMPLE HOLD

Figure 7



Initially S_1 is connected to V_{in} and S_2 is closed. The op. amp. is operating as a unity gain follower and its offset voltage (V_{off}), along with the analog input voltage, is stored on the capacitor.

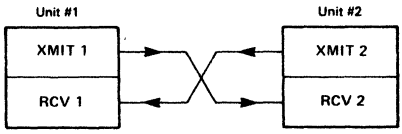
Then switch S_2 is opened and S_1 is switched to analog ground. The voltage at the inverting input of the op-amp is now V_{off}-V_{in}. Thus when the amplifier operates with S_2 open it acts as a comparator with effectively zero offset and $-V_{in}$ applied on its inverting input. The other end of the capacitor can now be operated as a DAC. Thus the capacitor ladder performs all the necessary functions of offset-null sample-hold as well as a DAC in the encode section of the chip.

EXPERIMENTAL RESULTS

The set up of Figure 8 was used to evaluate the chip performance.

CHIP PERFORMANCE

Figure 8

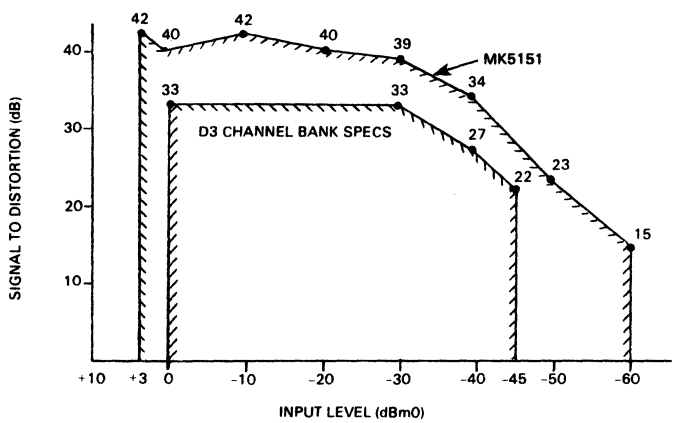


The MK5151 CODEC performance exceeds the AT&T D3 channel bank specifications. Figure 9 shows the signal-to-quantizing distortion as a function of input level.

Idle channel noise of 13-14dBrnC0 is better than the D3 spec by 9-10dB. Gain tracking is shown in Figure 10.

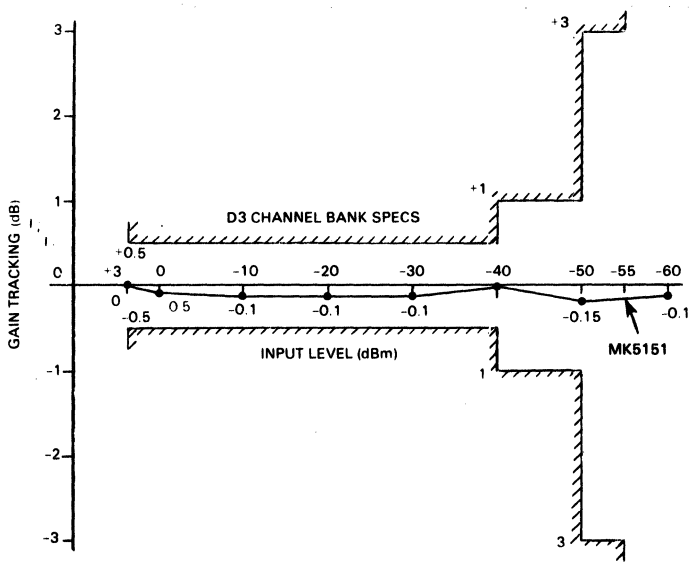
SIGNAL-TO-NOISE RATIO

Figure 9



GAIN TRACKING

Figure 10



Operating power measured at room temperature typically is 30mW. This is low enough that a stand-by mode is not deemed necessary. The European A-law version of the CODEC is also available and is simply a metal mask variation of this product. Chip size is 170 x 184 mils.

PRODUCT PROFILE

MOSTEK®

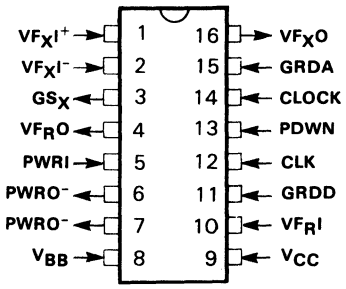
PCM TRANSMIT/RECEIVE FILTERS

MK5912

FEATURES

- Monolithic device includes both transmit and receive filters
- CCITT G712 and AT&T D3/D4 compatible
- Transmit filter includes 50/60Hz rejection
- Receive filter includes sin x/x compensation
- External gain adjustment, both transmit and receive filters
- Lower power consumption
- Direct interface with transformer or electronic telephone hybrids
- ± 5% power supplies; +5V, -5V
- Standard 16-pin package.
- Pin-for-pin compatible with the Intel 2912 PCM filter

PIN CONNECTIONS

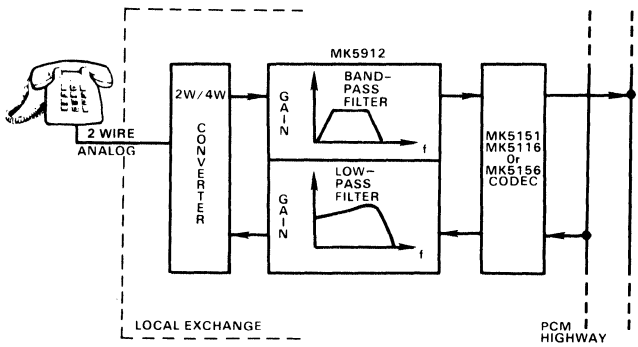


DESCRIPTION

The MK5912 is a monolithic device containing the two filters of a PCM line or trunk termination and is designed to minimize power dissipation, maximize reliability and provide a low-cost alternative to hybrid filters. The pin connections are shown above.

The device consists of two switched-capacitor filters, transmit and receive, and power amplifiers which may be used to drive a transformer hybrid (2-to-4-wire converter) or an electronic hybrid (SLIC). If an electronic hybrid is used, the power amplifiers are not needed and may be deactivated to minimize power dissipation. The transmit filter is a band-pass filter which will pass frequencies between 300Hz and 3200Hz and provides rejection of the 50/60Hz power line frequency as well as the anti-aliasing needed in an 8kHz sampling system. The receive filter is a low-pass filter which smooths the voltage steps present in the CODEC output waveform and provides the sin x/x correction necessary to give unity gain in the passband for the CODEC-decoder-and-receive-filter pair. A typical line termination is shown below.

The MK5912 is designed to be used with the Mostek family of CODECS.



PRELIMINARY

MOSTEK®

REPERTORY DIALER

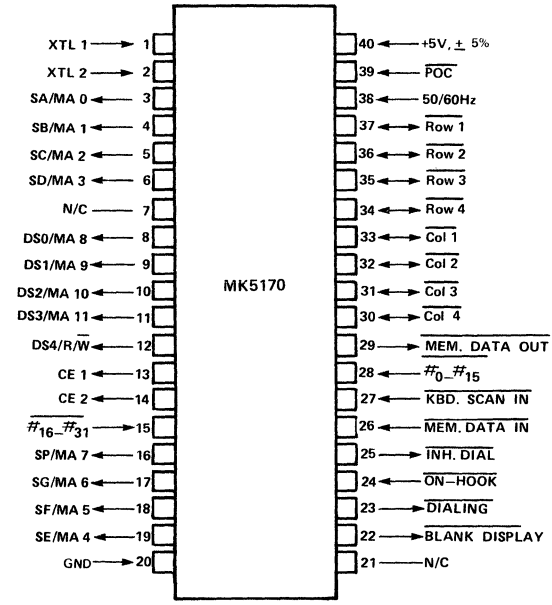
MK5170

FEATURES

- ☐ Repertory of 10, 24, 50, or 100 20-digit call numbers
- ☐ Repertory size determined automatically by the amount of memory installed
- ☐ Speed dialing of the desired call number
- ☐ Repertory easily updated by user
- ☐ Each call number has an associated address code. Display drive is provided to display the address code and the 20-digit call number
- ☐ When a phone number is manually dialed, the digits will be displayed as they are entered
- ☐ Any number in the repertory can be displayed
- ☐ The last number dialed is retained in an internal dial buffer for redialing
- ☐ Single-button dialing, with up to 32 numbers in two 16-number groups
- ☐ Controls either a tone dialer or a pulse dialer
- ☐ On-chip segment encoding
- ☐ Will interface 2102 or MK4104 static memory
- ☐ Digital real-time, 12/24-hour, 50/60 Hz clock
- ☐ 100-hour timer
- ☐ Two keyboard options
- ☐ Operates on an inexpensive TV color-burst crystal
- ☐ Single +5 volt ± 5% power supply

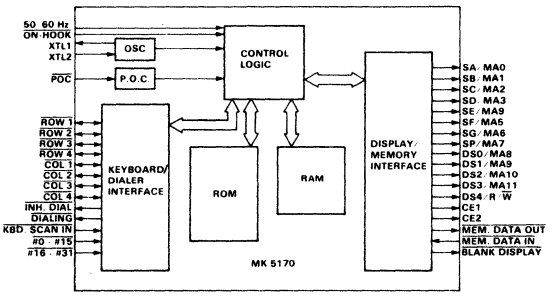
PIN CONNECTIONS

Figure 1



BLOCK DIAGRAM

Figure 2



DESCRIPTION

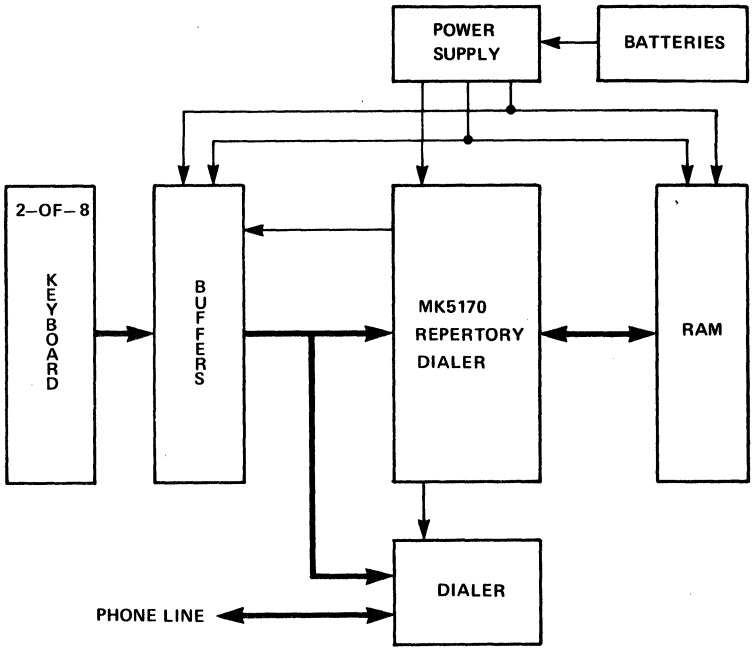
The MK5170 is a multi-function Repertory Dialer circuit utilizing ion-implanted, N-channel silicon gate technology and advanced circuit design techniques to provide maximum cost-effectiveness and flexibility. Pin connections are shown in Figure 1, and a block diagram is shown in Figure 2.

Several different modes of operation are possible. For minimal component count, the system of Figure 3 can be used with the keyboard configuration shown in Figure 4. This configuration is ideally suited to a 10-number repertory system and places the function control buttons on column 4 of a standard telephone keypad. For systems with more features, the system of Figure 5 can be used with the input matrix shown in

Figure 6. Note that the input matrix of Figure 6 permits the use of a calculator-type 1-of-N keyboard. The matrix includes both push-buttons and diode-selectable options. The options are selected by connecting a diode between the appropriate digit strobe and the keyboard scan input. Digit strobes are generated by an external decoder which is driven by the MK5170 (See Figure 7). Figure 8 provides two single-key dialing configurations. Up to 32 individual dial entry keys (#0 - #31) are possible.

BASIC REPERTORY DIALER SYSTEM

Figure 3



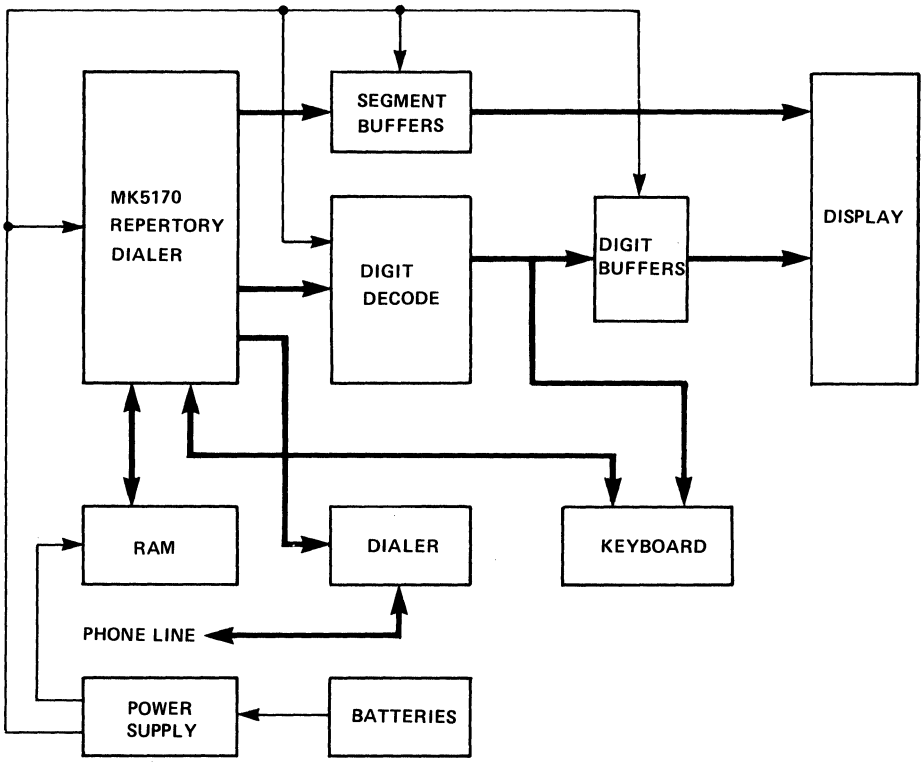
BASIC SYSTEM KEYBOARD CONFIGURATION

Figure 4

1	ABC 2	DEF 3	ENTER / DIAL	ROW 1
GHI 4	JKL 5	MNO 6	STORE	ROW 2
PRS 7	TUV 8	WXY 9	INF. PAUSE	ROW 3
*	OPER. 0	#	CLEAR	ROW 4
COL 1	COL 2	COL 3	COL 4	

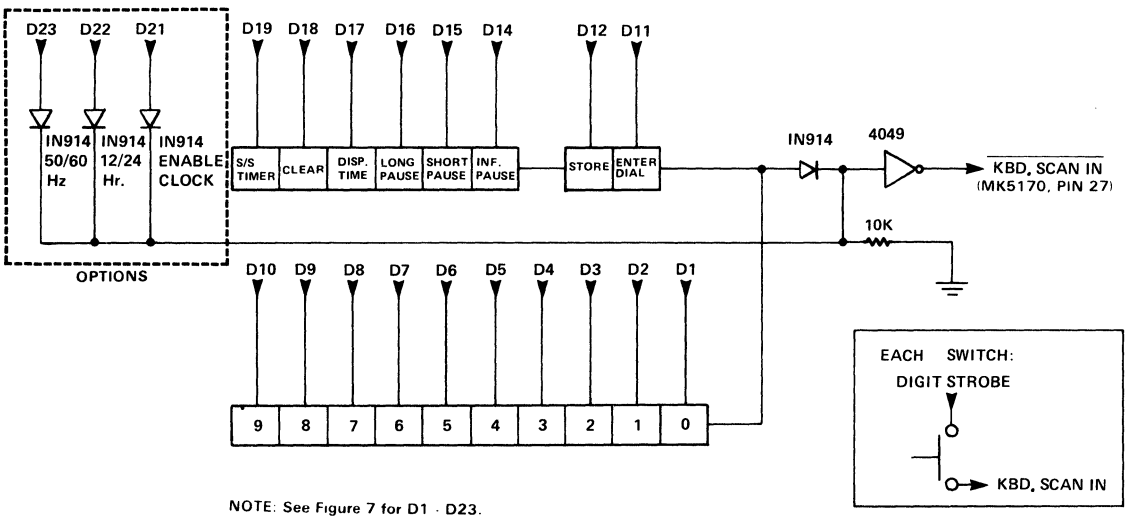
FULL FEATURE REPERTORY DIALER SYSTEM

Figure 5



FULL FEATURE KEYBOARD

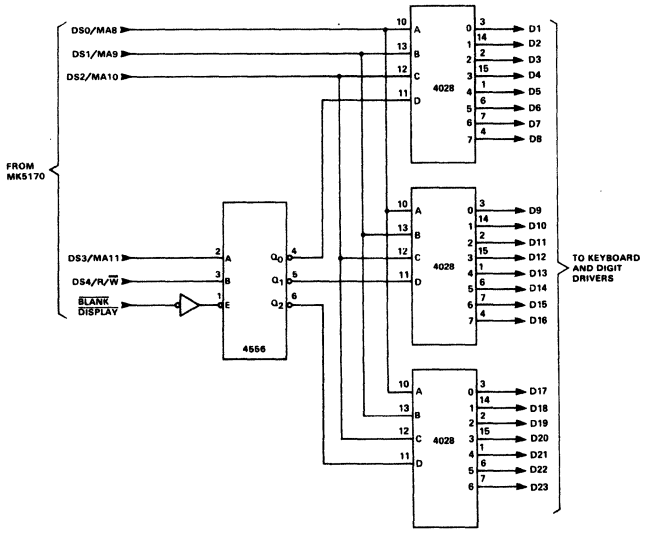
Figure 6



NOTE: See Figure 7 for D1 - D23.

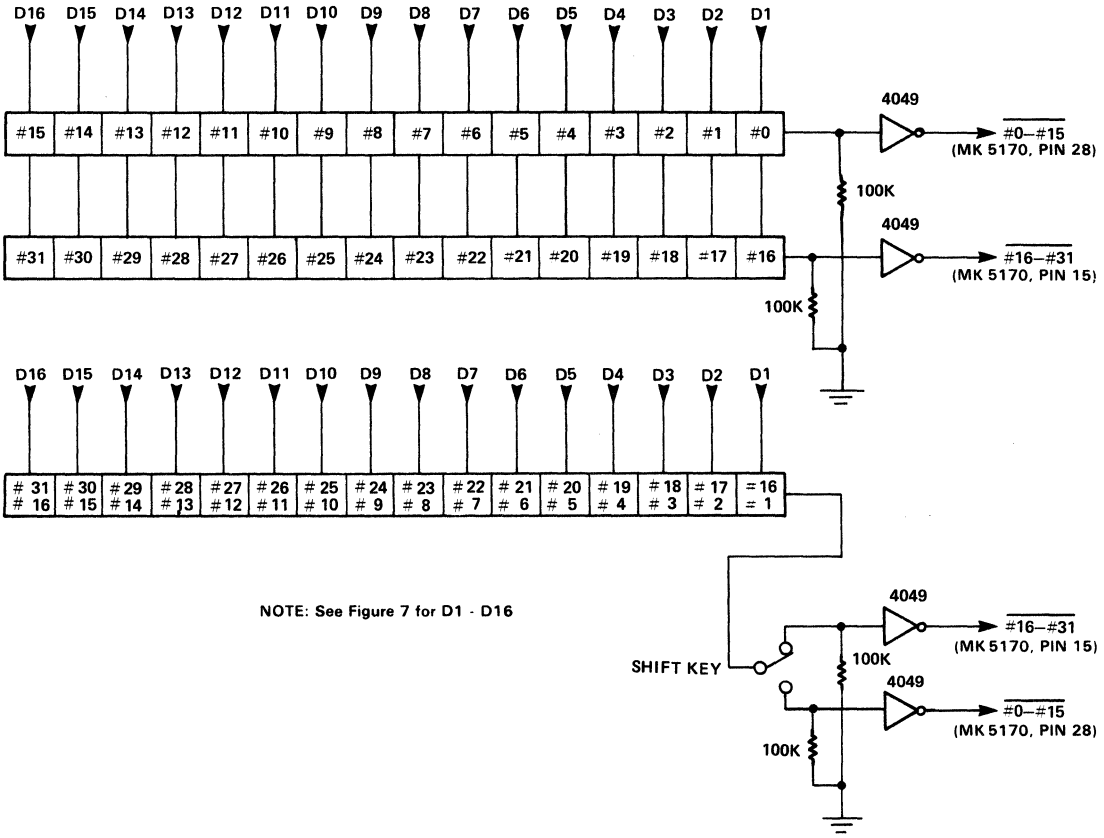
DIGIT SELECT ENCODER

Figure 7



TWO CONFIGURATIONS FOR SINGLE-KEY DIALING

Figure 8



NOTE: See Figure 7 for D1 - D16

Four types of functions are used to control the dialer: (1) ENTER/DIAL allows entry and dialing of telephone numbers, (2) STORE enables storage of entered numbers, (3) CLEAR clears erroneous entries or begins a data entry sequence and (4) PAUSE provides for inter-group pauses while dialing. Note that one of three lengths of pause may be selected:

(a.) Infinite pause which is terminated either by pressing the ENTER/DIAL button or by pressing one of the #0 through #31 keys; (b.) Short pause (1.5 seconds) which is terminated either by a 1.5-second time-out or by the means described in (a.); and (c.) Long pause (5 seconds) which is terminated either by a 5-second timeout or by the means described in (a.).

Two additional buttons are used to control the clock and the timer. DISP. TIME causes the MK5170 to display the current time. If this button is pressed and held for more than 3 seconds, then the MK5170 will enter the set time mode. During the 3-second timeout, the colons will stop flashing. At the conclusion of the timeout, the colons will resume flashing and the time can be set via the number keys. S/S TIMER provides for displaying the timer as well as starting and stopping it. If S/S TIMER is pressed and the timer is not being displayed, the display will change to show the timer count. If the timer is being displayed when S/S TIMER is pressed, the timer will start if it is not running and will stop if it is running.

An additional feature of the MK5170 is that, once a minute, the current time is stored in external RAM. The storage occurs on the minute transition. For example, as the time changes from 1:02 to 1:03, 1:02 will be stored. If AC power is then lost between 1:03:00 and 1:03:59, the clock will power up at 1:02:00 when AC power is restored. To further explain the operation of the Mk5170, a few examples are given below:

EXAMPLE 1: Storing a Number to be Dialed Later Using ENTER/DIAL

1. With the phone on-hook, press the ENTER/DIAL key. Digits 21 and 22 (See Figure 9), the address code, will show only decimal points. The remainder of the display will show the contents of the dial buffer. If the dial buffer is empty, only decimal points will be shown in digits 1 through 20.

2. Enter the address code. As the address code is entered it will be displayed in digits 21 and 22. If only 1K of memory has been installed, the first digit will be entered into digit 21 and digit 22 will be zero. Otherwise, the first entry will be displayed in digit 22 and the second entry will be displayed in digit 21. After a number has been entered in digit 21, the memory contents referenced by the address code will be shown on the display. If nothing has been stored in the referenced location, only decimal points will show in digits 1 through 20.

3. If digits 1 through 20 are not blank, press the CLEAR key. Enter the number to be dialed. As the digits are entered, they will appear on the display beginning at digit 20. If a pause is required, press the appropriate pause key. The code corresponding to the key, as shown in Figure 10, will appear on the display.

4. Press the STORE key. The telephone number shown in digits 1 through 20 will be stored in the memory location specified by the address code.

EXAMPLE 2: Dialing a Stored Number Using ENTER/DIAL

1. Lift the receiver and press the ENTER/DIAL key. Digits 21 and 22, the address code, will show only decimal points.

2. Enter the address code. Entry will be as described in Step 2 of Example 1. The dialing sequence will begin when the number is recalled from memory.

3. If the call wasn't completed, hang up the receiver. To redial the number, lift the receiver and press the ENTER/DIAL key twice.

EXAMPLE 3: Storing a Dialed Number Using ENTER/DIAL

1. Lift the receiver and dial the number. As the keys are pressed their corresponding code will appear on the display. The address code will show only decimal points. If the keyboard of Figure 4 is used, * and # can be dialed. If a pause key is pressed, its code will appear on the display but the pause will not occur. If the number is redialed or stored and recalled from memory, the pause will be executed when it is encountered.

2. Before going on-hook, press the ENTER/DIAL key followed by the desired address code. Entry will be as described in Step 2 of Example 1. After digit 21 is entered, press the STORE key. The telephone number will be stored in the location specified by the address code.

EXAMPLE 4: Storing a Number to be Dialed Later using #0 - #31

1. With the phone on-hook, press the button (#0 - #31) corresponding to the desired number. The address code will be two digits corresponding to the pressed button.

2. Proceed as described in Steps 3 and 4 of Example 1.

EXAMPLE 5: Dialing a Stored Number Using #0 - #31

1. Lift the receiver and press the button (#0 - #31) corresponding to the desired number. The address code will be two digits corresponding to the pressed button. As soon as the number is recalled from memory, the dialing sequence will begin.

2. If the call was not completed, proceed as described in Step 3 of Example 2.

EXAMPLE 6: Setting the Clock

1. Press the DISP. TIME button and hold for 3 seconds. While the key is held, the colons will not flash. After the 3-second timeout, the colons will resume flashing.

2. Press the CLEAR key. The time will be reset to 1 a.m.

3. Enter the desired time via the number keys. Illegal entries will be ignored. If an error is made, repeat step 2. Only the first 4 entries will be accepted.

4. After the correct data has been entered, press the DISP. TIME key. Clock setting will then be disabled.

EXAMPLE 7: Displaying the Clock

1. Press the DISP. TIME button. The clock will be displayed but cannot be set unless the sequence shown in Example 6 is followed.

2. If the CLOCK ENABLE diode has been installed (see Figure 6), the clock will automatically be displayed 10 seconds after dialing is completed.

EXAMPLE 8: Operating the Timer

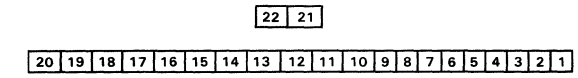
1. Whenever it is desired to display the timer, press the S/S TIMER button.

2. If the timer is being displayed when the S/S TIMER button is pressed, one of the following actions will result: a. If the timer is running, it will stop
   b. If the timer is stopped, it will start

3. If the timer is being displayed when the CLEAR button is pressed, it will be cleared to 00.00.00.

DISPLAY ORGANIZATION

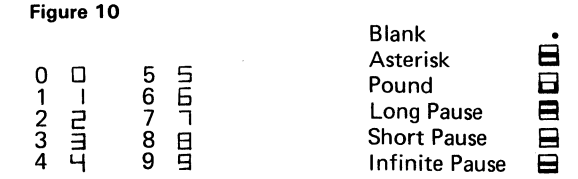
Figure 9



Digits 22 & 21 -	Address Code (Rep Dialer Mode)
Digits 20 - 1 -	Dial Buffer Contents (Rep Dialer Mode)
Digits 20 - 15 -	Real time - H.M.S. (Clock Mode)
Digits 20 - 15 -	Elapsed Time - H.M.S. (Timer Mode)
Digits 19 & 17 -	Decimal Points (Flashing in Clock Mode; Fixed in Timer Mode)

CHARACTER FONT

Figure 10



FUNCTIONAL PIN DESCRIPTION

Pin 1, XTL1 and Pin 2, XTL2

These pins are the time-base inputs. With a crystal connected between these pins, the MK5170 will provide the Row/Column timing shown in the AC characteristics section. No other oscillator components are required.

Pin 3, SA/MA0

This output normally has segment A information for the display. During memory access, this output drives the LSB of the memory address.

Pin 4, SB/MA1

This output normally has segment B information for the display. During memory access, this output drives the 2nd LSB of the memory address.

Pin 5, SC/MA2

This output normally has segment C information for the display. During memory access, this output drives the 3rd LSB of the memory address.

Pin 6, SD/MA3

This output normally has segment D information for the display. During memory access, this output drives the 4th LSB of the memory address.

Pin 7, N/C

This pin has no user-accessible function but it should not be used as a tie point.

Pin 8, DS0/MA8

This output normally has the LSB of the digit select code. During memory access, this output drives the 4th MSB of the memory address.

Pin 9, DS1/MA9

This output normally has the 2nd LSB of the digit select code. During memory access, this output drives the 3rd MSB of the memory address.

Pin 10, DS2/MA10

This output normally has the 3rd LSB of the digit select code. During memory access, this output drives the 2nd MSB of the memory address.

Pin 11, DS3/MA11

This output normally has the 2nd MSB of the digit select code. During memory access, this output drives the MSB of the memory address.

Pin 12, DS4/R/$\overline{W}$

This output normally has the MSD of the digit select code. During memory access, this output drives the memory read/write line. A low on this pin enables the write mode; a high allows the memory to be read.

Pin 13, CE1

This output enables the least significant memory chip.

Pin 14, CE2

This output enables the most significant memory chip.

Pin 15, $\overline{\#16 - \#31}$

This input is used to interrogate single-key ENTER/DIAL keys 16 through 31. As shown in Figure 8, these keys are tied to digit strobes 1 through 16, respectively.

Pin 16, SP/MA7

This output normally has segment P (decimal point) information for the display. During memory access, the output drives the 5th MSB of the memory address.

Pin 17, SG/MA6

This output normally has segment G information for the display. During memory access, this output drives the 6th MSB of the memory address.

Pin 18, SF/MA5

This output normally has segment F information for the display. During memory access, this output drives the 6th LSB of the memory address.

Pin 19, SE/MA4

This output normally has segment E information for the display. During memory access, this output drives the 5th LSB of the memory address.

Pin 20, GND

This pin is logic and circuit ground.

Pin 21, N/C

This pin has no user-accessible function but it should not be used as a tie point.

Pin 22, $\overline{\text{Blank Display}}$

This signal goes low to blank the display by inhibiting an external digit select decoder.

Pin 23, $\overline{\text{Dialing}}$

This output goes low during a dialing cycle and is used to disable the 2-of-8 keyboard.

Pin 24, $\overline{\text{On-Hook}}$

If this pin is pulled low, the telephone is on-hook and the ENTER/DIAL key functions as an ENTER key. If this input goes low during dialing, dialing is terminated and the dialer resorts to its normal scanning routine. If this pin is high, the telephone is off-hook and dialing can occur.

Pin 25, $\overline{\text{Inh. Dial}}$

This pin goes low during data entry to inhibit the MK5090 or MK5098 and prevent tones or pulses from being generated.

Pin 26, $\overline{\text{MEM. DATA IN}}$

The dialer uses this pin to read data from the external memory.

Pin 27, $\overline{\text{KBD. SCAN IN}}$

This is the input for the function keys, options and number keys. The use of the options is described below:

50/60 Hz (D23) (See Figure 6)

If a diode is not installed, the MK5170 will require a 60 Hz timebase for the clock and timer. Installing a diode indicates that a 50Hz timebase is to be used.

12/24 HR (D22) (See Figure 6)

If a diode is not installed, the MK5170 will display the clock in 12-hr format. Installing a diode will cause the clock to be displayed in 24-hr format with leading zeroes.

Enable Clock (D21) (See Figure 6)

10 seconds after the MK5170 completes a dialing cycle, one of two actions will occur: (1) If the Enable Clock diode is installed, the MK5170 will display the clock or (2) If the diode is not installed, the display will be blanked. Pressing any key will unblank the display.

The use of the remaining keys is described in Table 1. State Control Sequence for the MK5170 Repertory Dialer.

Pin 28, $\overline{\text{\#0 - \#15}}$

This input is used to interrogate single-key ENTER/DIAL keys 0 through 15. As shown in Figure 8, these keys are tied to digit strobes 1 through 16, respectively.

Pin 29, $\overline{\text{MEM. DATA OUT}}$

This output is used to transmit data to the external memory.

Pin 30 through Pin 33, $\overline{\text{COL 4}}$ through $\overline{\text{COL 1}}$

These pins are used to interrogate the keyboard columns and to drive the column inputs of the MK5090 tone dialer or MK5098 pulse dialer.

Pin 34 through Pin 37, $\overline{\text{ROW 4}}$ through $\overline{\text{ROW 1}}$

These pins are used to interrogate the keyboard rows and to drive the row inputs of the MK5090 tone dialer or MK5098 pulse dialer.

Pin 38, 50/60 Hz

This input provides the time base for the real time clock.

Pin 39, $\overline{\text{POC}}$

This input can be used to force a power-on-clear.

Pin 40, V_{CC}

+5V, ± 5%

STATE CONTROL SEQUENCE FOR THE MK5170 REPERTORY DIALER
Table 1

STATE	LAST FUNCTION ENTERED	PRESENT FUNCTION	RESULTS
Power Up	None	None	Display all decimal points; digits blanked
	None	Disp. Time	Display clock. Will show 1.00.00 if memory power has failed or if this is the first application of power. Otherwise, it will show the time at which AC power was lost.
	None	S/S Timer	Display timer. 00.00.00. Timer not running
	None	E/D	Display phone number. Display will not change.
	None	Digits, * #, Long/Short/Inf. Pause	Display the symbol for each digit or function as it is is entered. Any entries above 20 digits are ignored.
	None	Clear	No change
	None	Store	No Change
	None	#0 - #31	Show the number stored in the corresponding memory location. If nothing has been stored, display all decimal points with digits blanked, except for address code. If off-hook, dial the number.

Table 1 Continued

STATE	LAST FUNCTION ENTERED	PRESENT FUNCTION	RESULTS
Display Clock	Disp. Time	Disp. Time	No change. Colons will not flash while Disp. Time switch is held. If switch is held for more than three seconds, the colons will start flashing and the MK5170 will enter the set clock state.
		S/S Timer	Display timer. Colons not flashing.
		E/D	Blank address code, display phone number.
		Long/Short/Inf. Pause, Clear, Store	No change
		#0 - #31	Show the number stored in the corresponding memory location. If off-hook, dial the number.
		Digits, *, #	Display the digit or function when it is entered. Start manual entry sequence.
Display Timer	S/S Timer	S/S Timer	If timer was running, stop. If timer was not running, start.
		Clear	Clear timer.
		Disp. Time	Display clock.
		Long/Short/Inf. Pause, Store	No change
		Digits, #, *	Display the digit or function when it is entered. Start manual entry sequence.
		E/D	Blank address code, display phone number
		#0 - #31	Show the number stored in the corresponding memory location. If off-hook, dial the number.
Manual Entry	Digits, *, #	Digits, #, *, Long/Short/Inf. Pause	Display the symbol for each digit or function as it is entered. Entries above 20 digits are ignored.
		Clear	Clear the display
		Disp. Time	Display clock
		Store, E/D	No change
		#0 - #31	Display the number stored in the corresponding memory location. If off-hook, dial the number
Display Phone Number	E/D	None	Blank address code, display phone number.

Table 1 Continued

STATE	LAST FUNCTION ENTERED	PRESENT FUNCTION	RESULTS
Display Phone Number Continued		Digit	Enter digit into address code. If 1K of memory is installed, enter digit into LSD and recall phone number from memory. If off-hook, dial the number.
		S/S Timer	Display timer
		Disp. Time	Display clock
		Store, Long/ Short/Inf. Pause, *, #	No change
		Clear	Clear display
		#0 - #31	Display the number stored in the corresponding memory location. If off-hook, dial the number.
	Digit	Digit	If second digit and more than 1K of memory is installed, store digit in LSD of address code and recall phone number from memory. If off-hook, dial number. If second digit and 1K of memory is installed, store digit in MSD of phone number. If not second digit, store in next location in phone no.
		*, #, Long/Short/ Inf. Pause	If second digit and more than 1K of memory is installed, ignore. If not second digit, store in next location in phone number.
		Clear	If address code is incomplete, clear address code and phone number. If address code is complete, clear only the phone number.
		Store	If address code is complete, store the phone number. Otherwise, ignore.
		#0 - #31	Display the number stored in the corresponding memory location. If off-hook, dial the number.
	E/D	E/D	Dial the number in the dial buffer (redial).
	Digit	S/S Timer	Display timer
		Disp. Time	Display clock
Set Clock	Disp. Time for greater than 3 seconds	Digit	Legal digit will be entered into next location. Illegal digit will be ignored.
		Clear	Set time to 1.00.00 a.m.

Table 1 Continued

STATE	LAST FUNCTION ENTERED	PRESENT FUNCTION	RESULTS
Set Clock Continued		Store, *, #, Long/ Short/Inf. Pause	No change
		#0 - #31	Display the number stored in the corresponding memory location. If off-hook, dial the number.
		E/D	Display phone number
		S/S Timer	Display timer
		Disp. Time	Display clock, leave set clock mode.

APPLICATION INFORMATION

The Basic Repertory Dialer System of Figure 3 represents the minimum number of components required to implement a repertory dialer system using MK5170. A 2-of-8 keyboard, using the interface shown in Figure 11, provides the system control functions of number entry, Enter/Dial, Store, Inf. Pause and Clear. A quad comparator, an LM2901 or equivalent, is used as a buffer between the keyboard and the MK5170. The non-inverting input of each comparator is biased at ½ +5M and the appropriate non-inverting inputs are tied to their assigned row or column. A key closure will pull two of the non-inverting inputs within two diode drops of ground, thus causing the associated comparator outputs to go low. The MK5170 then senses these two low levels and, after identifying the key, drives the $\overline{\text{DIALING}}$ output low, which pulls the inverting inputs within one diode drop of ground and causes all of the comparator output transistors to turn off, thus isolating the keyboard from the MK5170 so that the MK5170 can apply row and column information to the dialer without interference from the keyboard.

The dialer interfaces shown in Figure 12 and Figure 13 include level conversion circuitry as well as an $\overline{\text{Inhibit Dial}}$ feature. The active - low row and column signals (ROW 1 - COL 3) are applied to the bases of NPN transistors. Because the power supply to the tone dialer can vary between 3.4 volts and 10.5 volts and the power supply to the pulse dialer can vary between 2.5 and 5 volts, level conversion is required between the 0 - to 5 - volt row and column signals and the corresponding inputs to the MK5090 or MK5098. This required level conversion is provided by the 7 NPN transistors. When the MK5170 is required to isolate the dialer from the 2-of-8 keyboard (i.e. during data entry), it does so by driving the $\overline{\text{INH. DIAL}}$ line low. The $\overline{\text{INH. DIAL}}$ signal is inverted and used to turn all of the NPN transistors on so that the signals applied to the row and column inputs of the MK5090 and MK5098 will be at their inactive level. When the MK5170 starts a dialing cycle, the $\overline{\text{INH. DIAL}}$ line will go high and the required sequence of row and column signals will be applied to the bases of the NPN level converters. The 4050 buffers and 4049 inverting buffers shown in the dialer interface schematics are powered from the phone line and provide the buffering and logic inversion necessary to meet the input requirements of the MK5090 and MK5098, as well as permitting the use of 1 megohm pull up resistors at the collectors of the NPN level converters. Using large - value pullup resistors reduces the amount of current that the buffer circuitry draws from the phone line.

The Full-Feature Repertory Dialer System of Figure 5 implements all the features provided by the MK5170 by placing all of the keys and option diodes in a 3 x 24 matrix shown in Figure 6 and Figure 8. $\overline{\text{KBD. SCAN IN}}$, #0 - #15 and #16 - #31 are scanned by the MK5170. When an active low level is detected on any of the three scan lines, the MK5170 determines which key has been pressed and takes appropriate action. Digit strobes for scanning the input matrix are generated by the circuit shown in Figure 7, which encodes the 5-bit digit select code (DS0 - DS4) into 1 of 23 digit strobes (D1 - D23). These positive pulses are then used to drive the bipolar digit drivers for the display as well as for scanning the input matrix. A $\overline{\text{BLANK DISPLAY}}$ input is provided to inhibit the generation of digit strobes during memory access, since the segment and digit encoding lines are shared by memory addresses and read/write control (See Figure 7).

The Power Supply and Timebase Reference circuit shown in Figure 14 provides two independent 5-volt power supplies: (1) +5L which powers the MK5170 and the display circuitry and (2) +5M which powers the memory, the memory protect logic and the keyboard buffers and is provided with a battery backup which consists of 6 NiCd cells and a charging circuit. The

Timebase Reference consists of a comparator with hysteresis so that power line noise will not reach the MK5170.

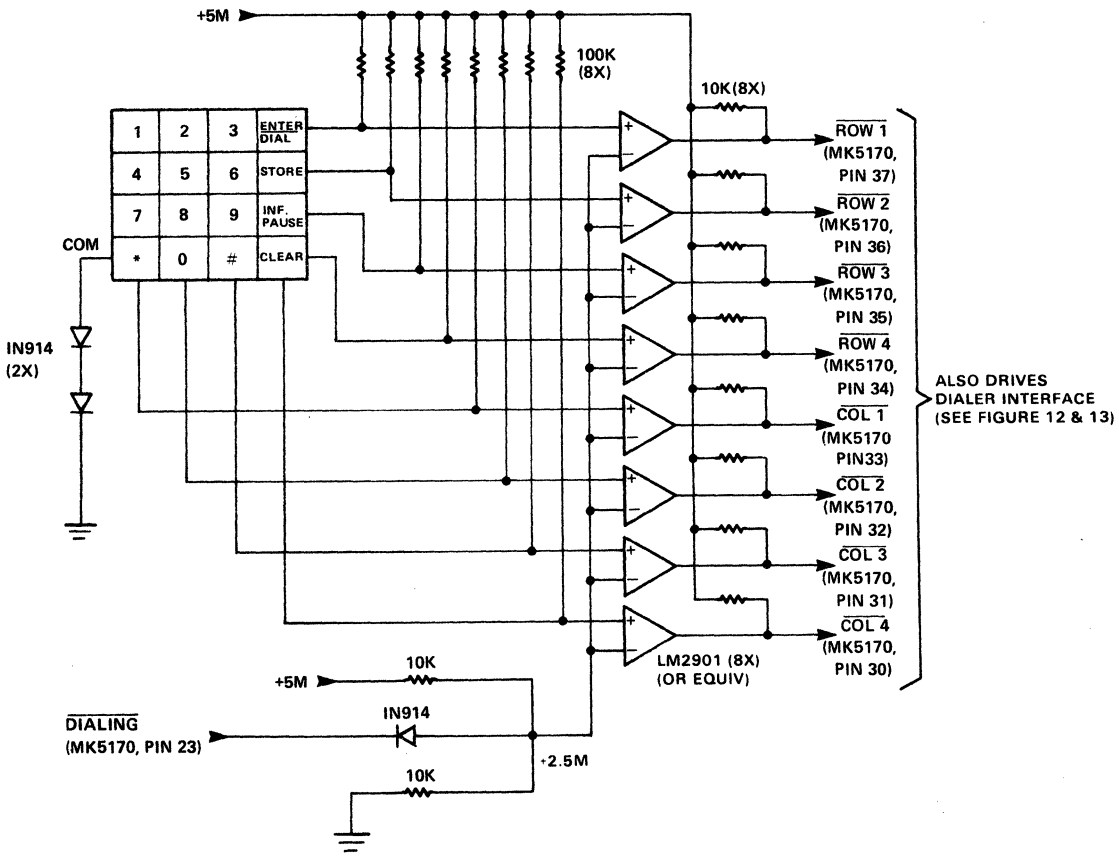
The Memory Protect Logic shown in Figure 15 provides two functions: (1) The MK5170 will be reset whenever its power supply dips to 4.75V and (2) on power up and during a power supply dip to 4.75V, $\overline{CE1}$ and $\overline{CE2}$ will be forced high so that no memory chip selects can be generated. This insures that data stored in the MK4104 will not be destroyed. If a 2102 memory is used, the memory protect latch is not required. Note, however, that CE1 and CE2 must still be inverted to enable the memory. $\overline{CE1}$ and $\overline{CE2}$ will be enabled after $\overline{POC}$ is removed from the MK5170 and CE1 goes high.

Repertory size is determined automatically by the amount of memory installed so all that is required to alter the size of the repertory is to install memory devices as shown in Figure 16.

Figure 17 shows the suggested LED drive circuitry.

A special "on-hook" circuit, Figure 18, is shown for use with PBX systems. This circuit prevents the MK5170 from seeing the momentary line-disconnect exhibited by a PBX system as it switches to out-of-plant lines.

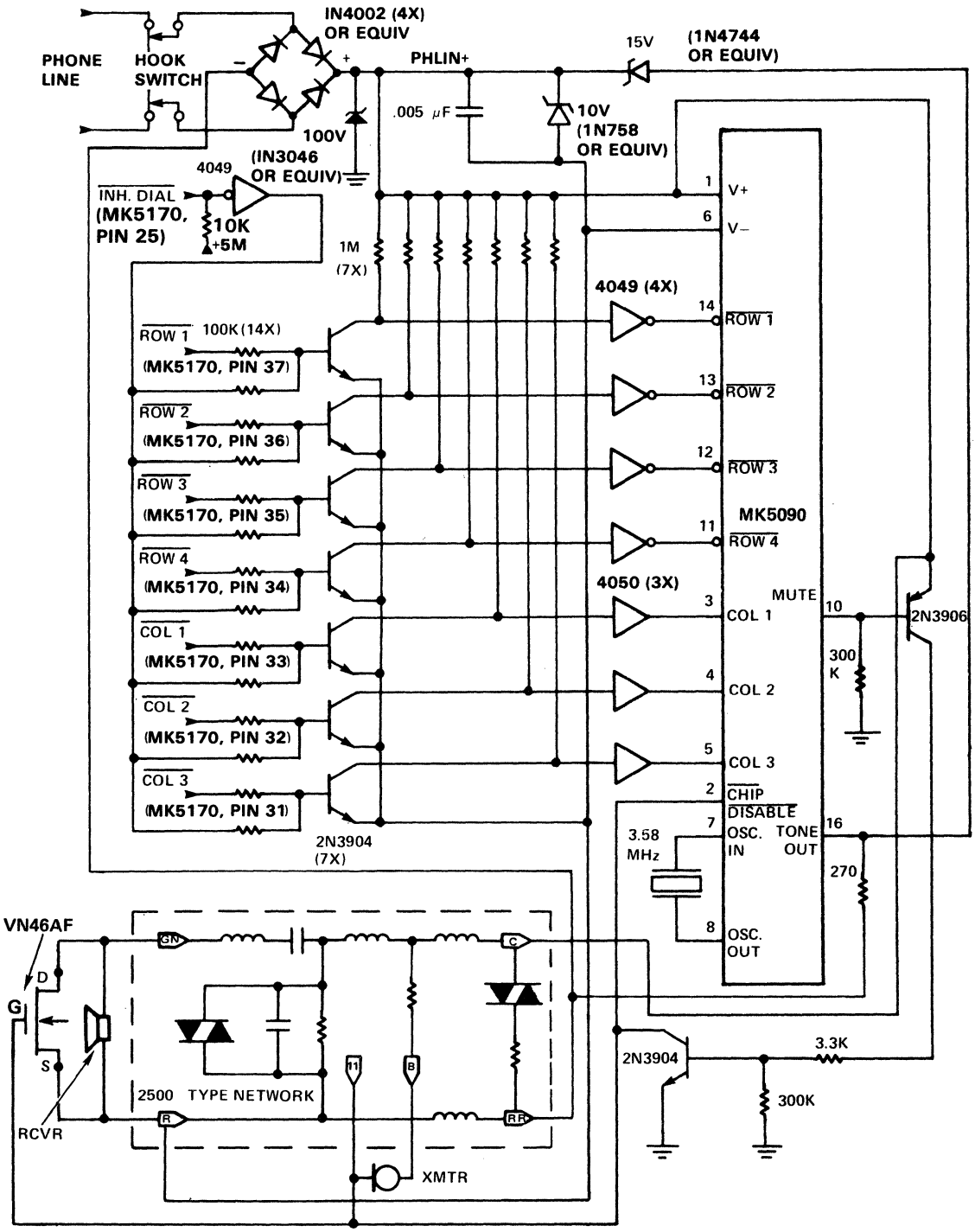
2 OF 8 KEYBOARD TERMINAL
Figure 11



NOTE: Comparator Powered From +5M

TONE DIALER INTERFACE

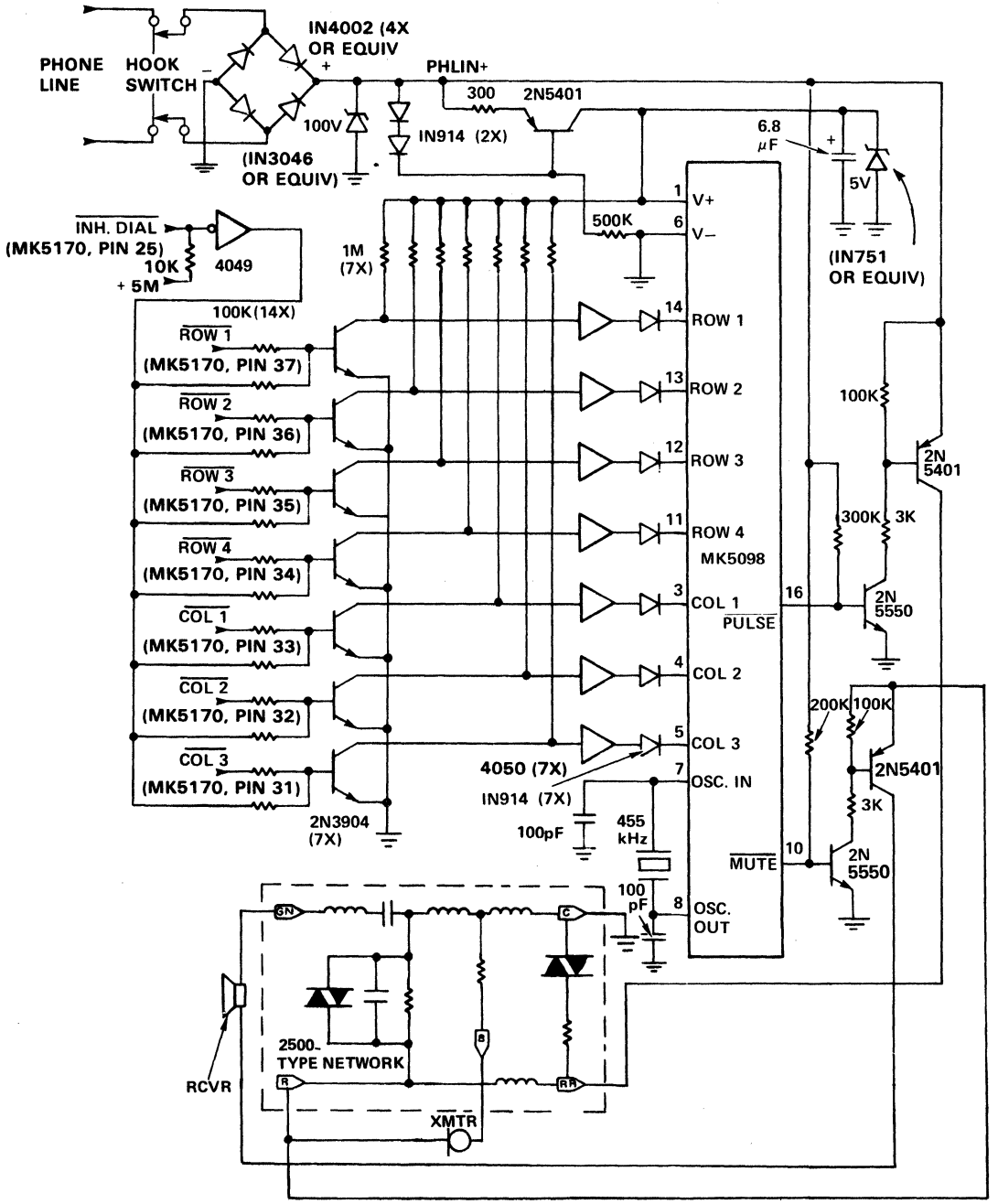
Figure 12



NOTE: 4049 and 4050 Buffers are Powered From PHLIN+

PULSE DIALER INTERFACE

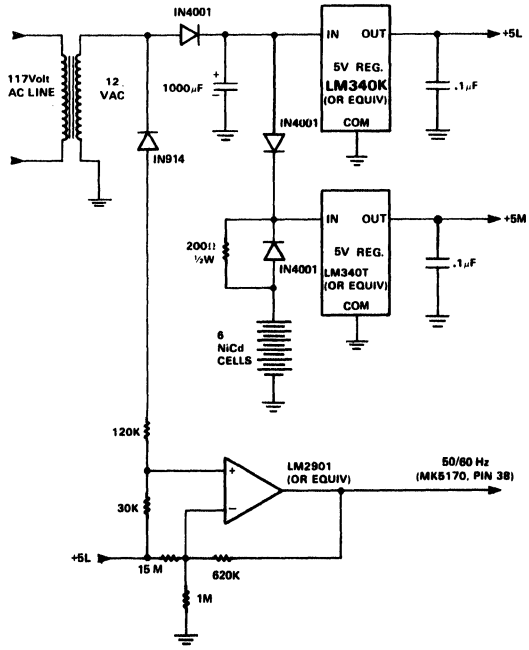
Figure 13



NOTE: 4049 and 4050 Buffers are Powered From PHLIN+

POWER SUPPLY AND TIMEBASE REFERENCE

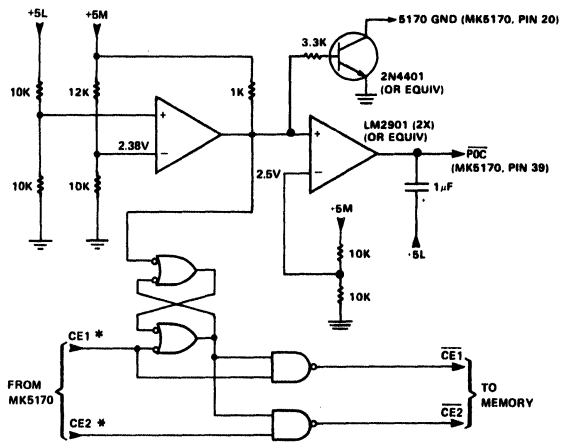
Figure 14



NOTE: COMPARATOR POWERED FROM +5M

MEMORY PROTECT LOGIC

Figure 15



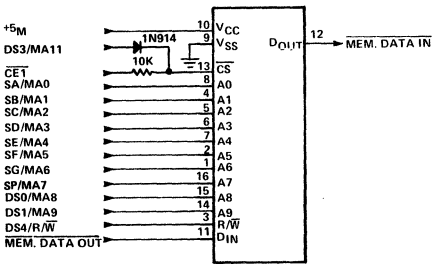
* CE1 & CE2 must be inverted to enable memory.

NOTE: ALL ACTIVE DEVICES POWERED FROM +5M

MEMORY CONNECTIONS TO MK5170

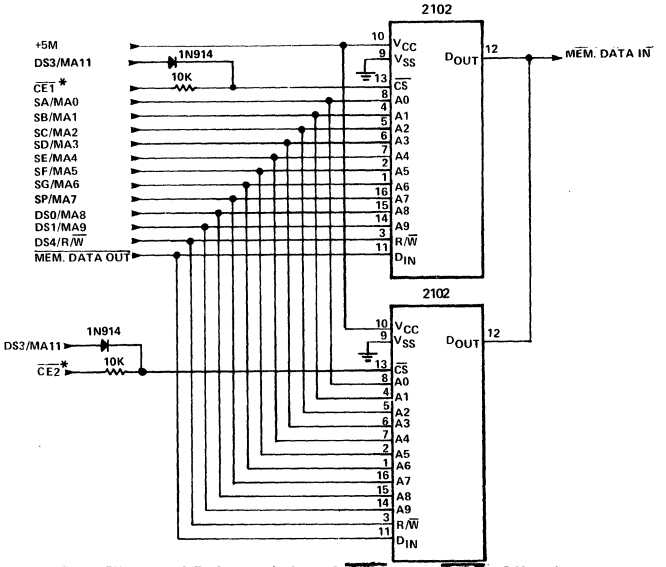
Figure 16

a. 12 - NUMBER REPERTORY



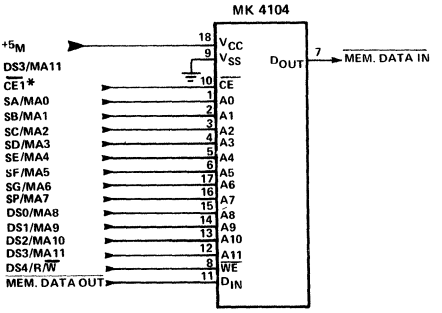
***See Figure 15 for origin of $\overline{CE1}$. All other signals interface directly with MK5170.**

b. 24 - NUMBER REPERTORY



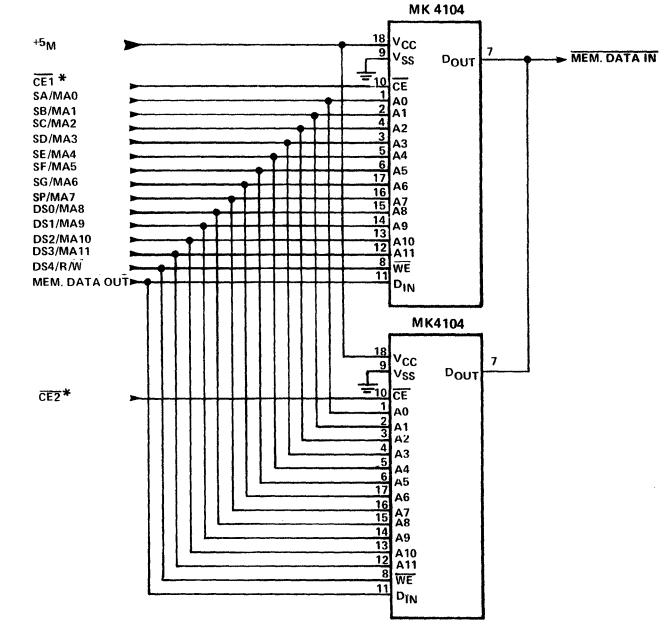
***See Figure 15 for origin of $\overline{CE1}$ and $\overline{CE2}$. All other signals interface directly with MK5170.**

c. 50 - NUMBER REPERTORY



***See Figure 15 for origin of $\overline{CE1}$. All other signals interface directly with MK5170.**

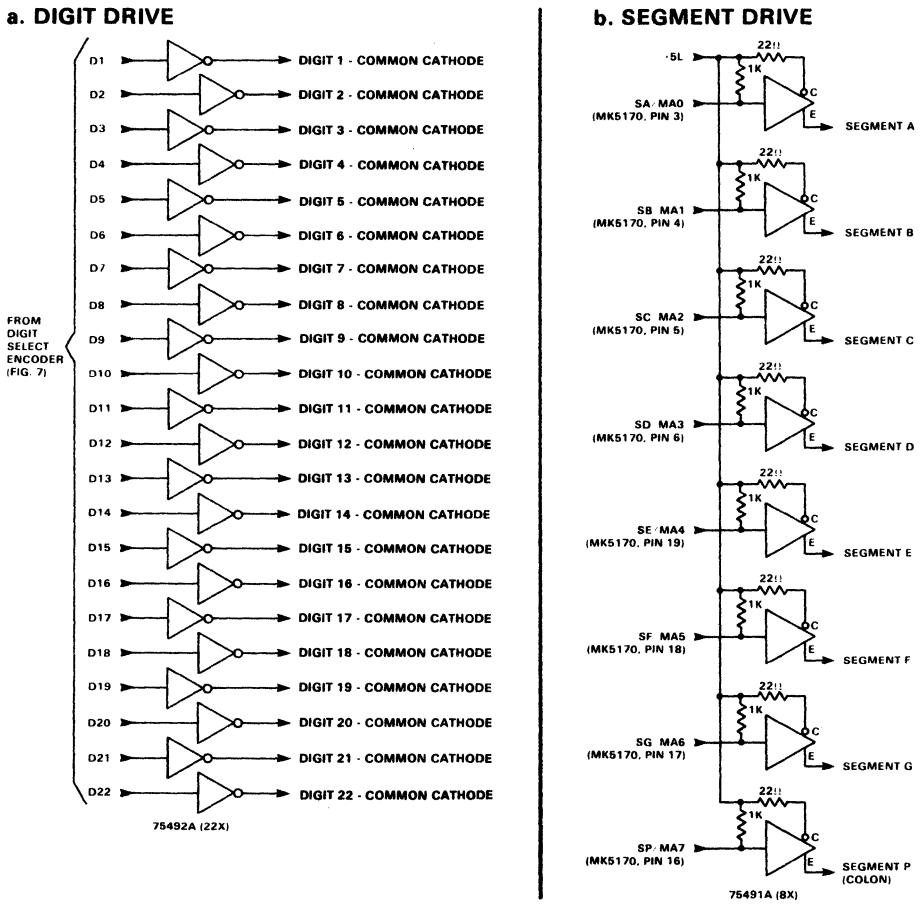
d. 100 - NUMBER REPERTORY



***See Figure 15 for origin of $\overline{CE1}$ and $\overline{CE2}$. All other signals interface directly with MK5170.**

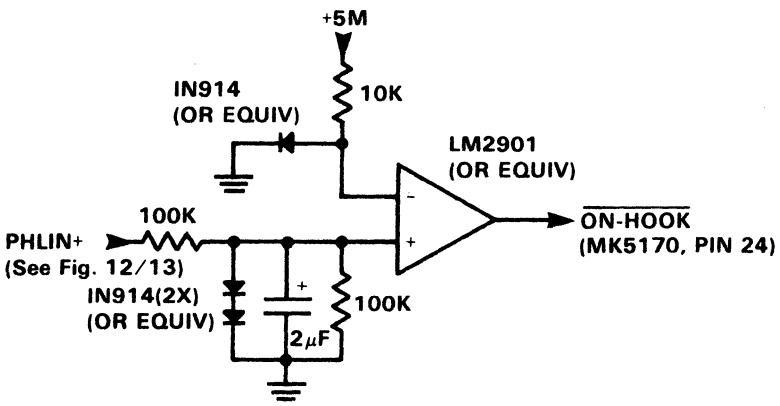
LED DRIVE CIRCUITRY

Figure 17



ON-HOOK CIRCUITRY

Figure 18



NOTE: Comparator is powered from +5M

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS*

Temperature under bias ..... 0°C to 70°C
Storage temperature ..... -65°C to 150°C
Voltage on any pin with respect to ground ..... -1.0V to +7V
Power dissipation 1.0W

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and function operation of the device at these or any other condition above these indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

T_A = 0°C to 70°C, V_{CC} = 5V ± 5%

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	TEST CONDITIONS
I_{CC}	Power Supply Current		55	77	mA	Output Open
P_D	Power Dissipation		275	385	mW	Outputs Open
V_{IH}	Input High Level	2.0		5.8	V	
V_{IL}	Input Low Level	-0.3		0.8	V	
I_{IH}	Input High Current			100	μA	V_{IH}=2.4V Internal Pull-Up
I_{IL}	Input Low Current			-1.6	mA	V_{IL}=0.4V
I_{OH}	Output High Current	-100			μA	V_{OH}=2.4V
I_{OL}	Output Low Current	1.8			mA	V_{OL}=0.4V
R_{IP}	Internal Pull-up Resistor		6		kΩ	Output transistor off

AC CHARACTERISTICS

T_A = 0°C to 70°C, V_{CC} = 5V ± 5%

SIGNAL	SYMBOL	PARAMETER	MIN	MAX	UNIT	COMMENTS
	t_0(XTL)	Time base period, Crystal mode	250	279	ns ns	4MHz crystal 3.58 MHz crystal
0	t_0	Internal 0 clock period	500	558	ns	
POC	t_{RH}	POC hold time, Low	3.75 4.10		μs μs	4MHz crystal 3.58MHz crystal
50/60Hz	t_{EH}	50/60Hz hold time, High	3.75 4.10		μs μs	4MHz crystal 3.58MHz crystal
Row/Col	t_{RC}	Row/Column output duration & off time	68	76	ms ms	4MHz crystal 3.58MHz crystal
	t_{ACC}	Memory Access Time	10		μs	
	t_{DP}	Digit Period		10.8	ms	3.58MHz crystal
	t_{DON}	Digit On Time		490	μs	3.58MHz crystal
	D.C.	Display Duty Cycle	3.2	3.2	%	

CAPACITANCE

T_A = 25°C, f_{XTL} = 4MHz

SYMBOL	PARAMETER	MIN	MAX	UNIT	TEST CONDITIONS
C_{IN}	Input capacitance, all pins except XTL1, XTL2		7	pF	Unmeasured pins returned to ground
C_{XTL}	Input capacitance, XTL1, XTL2	18	23	pF	

MOSTEK®

TEN NUMBER REPERTORY DIALER

MK5175

DESCRIPTION

The MK5175 is a monolithic integrated ten number repertory dialer manufactured using Mostek's Silicon Gate CMOS process. The circuit accepts keyboard inputs and provides the Pulse and Mute logic levels required for loop disconnect signalling. For DTMF Signalling, the MK5175 may be interfaced with Mostek's Tone Generators.

The circuit will function in either Tone or Pulse mode, dependent upon the logic level presented to pin 2, the "Mode Select" pin. The interpretation of several inputs and outputs is dependent upon the mode selected.

In Pulse mode, the time base for the circuit is a ceramic resonator which is low cost but provides a guaranteed accurate reference. In Tone mode, a single pin RC oscillator provides the frequency reference for the circuit. This provides the least expensive means to adequately control the tone output rate.

An on-chip RAM is capable of storing 10 sixteen-digit telephone numbers including the last number dialed. When used in a PABX system, a pause (# key) may be stored in the number sequence. The repertory dialer will recognize this pause when automatically dialing and stop until a "continue" (# key) input is received.

The MK5175 repertory dialer uses a standardized pinout scheme common to all Mostek Tone and Pulse Dialers. This will facilitate the design of a family of telephone products using common PC boards and circuit components.

NOTES

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