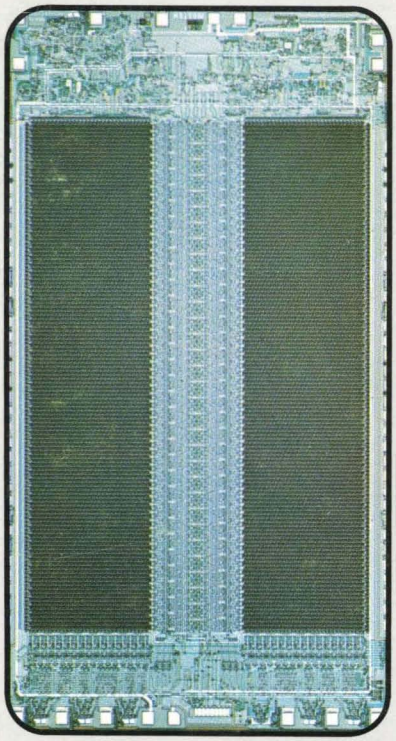
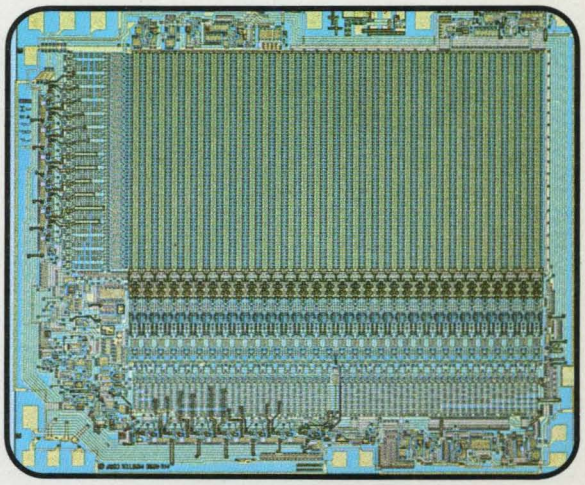
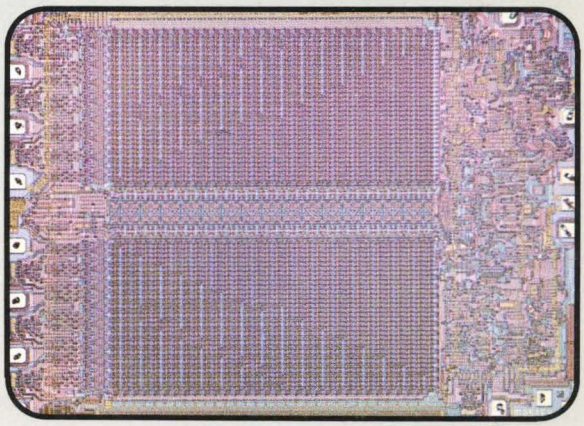
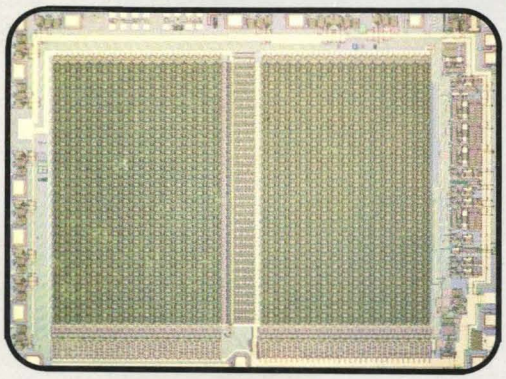
MOSTEK

1977 MEMORY PRODUCTS CATALOG









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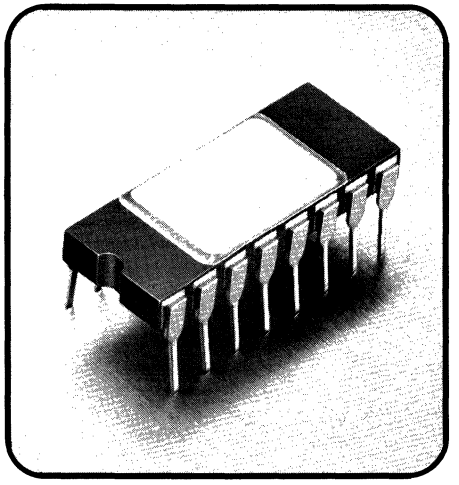


MOSTEK

DUAL 128-BIT STATIC SHIFT REGISTER

MK 1002 P/N

FEATURES

- ☐ Ion-implanted for full TTL/DTL compatibility no interface circuitry required
- ☐ Single-phase, TTL/DTL compatible clocks
- ☐ Dual 128-bit static shift registers—256 bits total
- ☐ Dual sections have independent clocks
- ☐ Recirculate logic built in
- ☐ DC to 1 MHz clock rates
- ☐ Low power dissipation—130 mW
- ☐ 16-pin dual-in-line package

DESCRIPTION

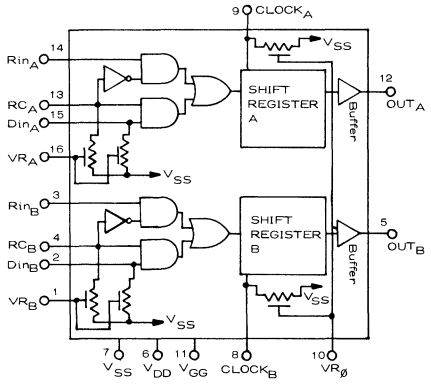
The MK 1002 is a P-channel MOS static shift register utilizing low threshold-voltage processing and ion-implantation to achieve full TTL/DTL compatibility. Each of the two independent 128 bit sections has a built-in clock generator to generate three internal clock phases from a single-phase TTL-level external input. In addition, each section has input logic for loading or recirculating data within the register. (See Functional Diagram.) The positive-logic Boolean expression for this action is:

OUT (delayed 128 bits) =
$(R_C)\ (D_{IN}) + (\overline{R_C})\ (R_{IN})$

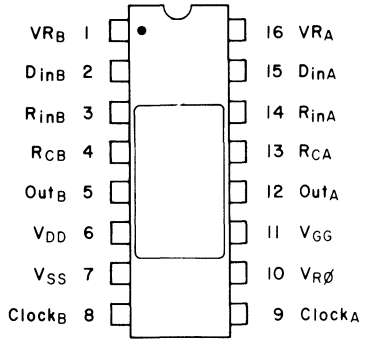
The Data, Recirculate Control, and Clock inputs are provided with internal pull-up resistors to V_{SS} (+5V) for use when driving from TTL. These resistors can be disabled when driving from circuitry with larger output-voltage swings, such as DTL. Enabling of pull-up resistors is accomplished by connecting the appropriate terminal to V_{GG}; disabling by connecting to V_{SS}. The Recirculate inputs are not provided with pull-up resistors since they are generally driven from MOS.

Shifting data into the register is accomplished while the Clock input is low. Output data appears following the positive-going Clock edge. Data in each register can be held indefinitely by maintaining the Clock input high.

FUNCTIONAL DIAGRAM



PIN CONNECTIONS



ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{DD} . . . . . V_{SS} − 10.0 V
Supply Voltage, V_{GG} . . . . . V_{SS} − 20.0 V
Voltage at any Input or Output. . . . . V_{SS} + 0.3 V to V_{SS} − 10.0 V
Operating Free-Air Temperature Range. . . . . 0°C to +75°C
Storage Temperature Range (Ceramic) . . . . . −65°C to +150°C
Storage Temperature Range (Plastic). . . . . −55°C to +125°C

RECOMMENDED OPERATING CONDITIONS ($0°C \leq T_A \leq 75°C$)

		PARAMETER	MIN	TYP	MAX	UNITS	COMMENTS
POWER	V_{SS}	Supply Voltage	4.75	5.0	5.25	V	V_{DD} = 0 V
	V_{GG}	Supply Voltage[1]	−12.6	−12.0	−11.4	V	
INPUTS	V_{IL}	Input Voltage, Logic 0[2]		0	V_{SS}−4	V	
	V_{IH}	Input Voltage, Logic 1	V_{SS}−1	5.0	V_{ss}	V	
INPUT TIMING	f	Clock Repetition Rate	DC		1	MHz	See Timing Diagram
	$t_{\phi p}$	Clock Pulse Width	0.35		10	μs	
	$t_{\phi d}$	Clock Pulse Delay	0.4			μs	
	$t_{\phi r}$	Clock Pulse Risetime	.010		0.2	μs	
	$t_{\phi f}$	Clock Pulse Falltime	.010		0.2	μs	
	t_{dld}	Data Leadtime	50			ns	
	t_{dlg}	Data Lagtime	200			ns	
	t_{rld}	Recirculate Control Leadtime	100			ns	
	t_{tlg}	Recirculate Control Lagtime	300			ns	

ELECTRICAL CHARACTERISTICS

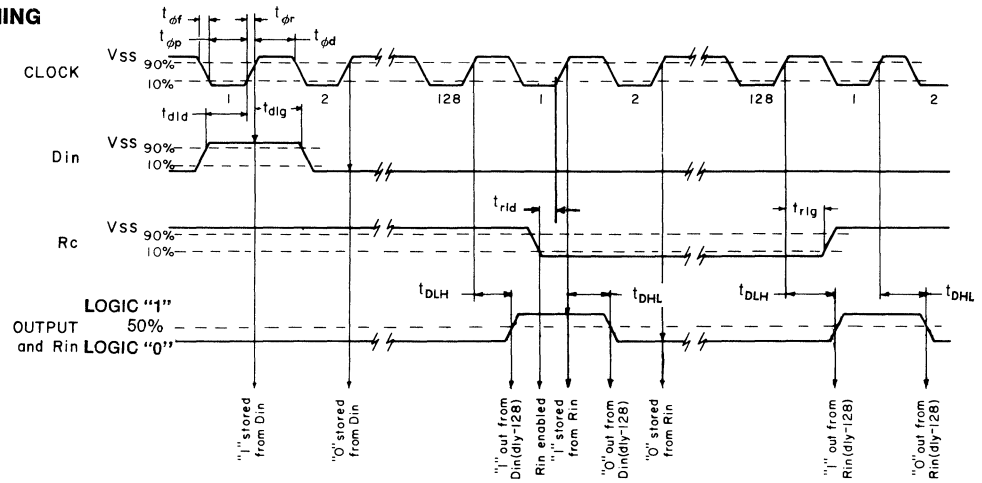
(V_{SS} = +5 ±0.25V, V_{GG} = −12 ±0.6V, V_{DD} = 0V, T_A = 0°C to +75°C, using test circuit shown, unless otherwise noted.)

		PARAMETER	MIN	TYP[3]	MAX	UNITS	CONDITIONS
POWER	I_{SS}	Power Supply Current, V_{SS}		14	25	mA	f_ϕ = 1 MHz Inputs & Outputs open
	I_{GG}	Power Supply Current, V_{GG}		5	10	mA	
INPUTS	C_i	Input Capacitance, any Input		3	10	pF	$V_I = V_{SS}$, f = 1 MHz T_A = 25°C
	I_{IL}	Input Current, Logic 0: Resistors Disabled[2]			−40	μA	$V_I = V_{SS}$ −5V
		Resistors Enabled[2]	−0.3		−1.6	mA	V_I = +0.4V
	I_{IH}	Input Current, Logic 1, Any Input			40	μA	VR_A, VR_B, $VR\phi = V_{SS}$ $V_I = V_{SS}$
	$I_{IR(on)}$	Input Current at Recirculate Inputs[2]			−40	μA	VR_A, VR_B, $VR\phi = V_{GG}$ $V_I = V_{SS}$ − 5V
OUTPUTS	V_{OL}	Output Voltage, Logic 0 (3)			0.4	V	I_L = −1.6 mA
	V_{OH}	Output Voltage, Logic 1 (3)	V_{SS} − 1			V	I_L = +100 μA
DYNAMIC CHAR.	t_{DLH}	Output Delay, Low to High (3)			450	ns	See Timing Diagram and Test Circuit
	t_{DHL}	Output Delay, High to Low (3)			450	ns	
	t_{VOR}	Output Voltage Rise Time (3)		100	150	ns	
	t_{VOF}	Output Voltage Fall Time (3)		100	150	ns	

NOTES:

1. Other supply voltages are permissible providing that supply and input voltages are adjusted to maintain the same potential relative to V_{SS}, e.g., V_{SS} = OV, V_{DD} = −5 ± 0.25V, V_{GG} = −17 ± 0.85V.
2. MOS pull-up resistors to +5V are provided internally. These MOS resistors are enabled by connecting VR_A, VR_B and $VR\phi$ to V_{GG}, and disabled by connecting VR_A, VR_B and $VR\phi$ to V_{SS}. Pull-up resistors not provided at recirculate inputs.
3. At T_A = 25°C.

TIMING



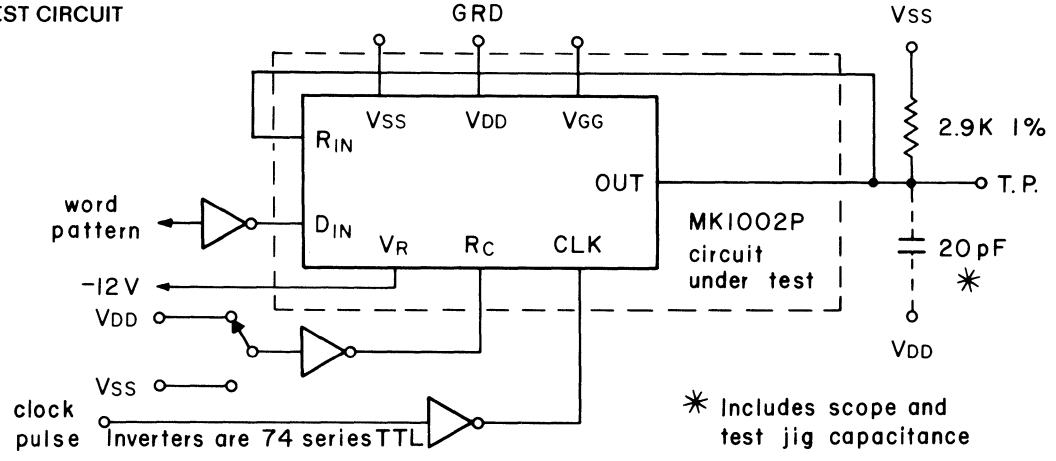
The timing diagram applies to either section of the dual shift register. The test conditions for these waveforms are illustrated below. A logic "1" is defined as +5 V and a logic "0" is defined as 0V

As long as R_C is at a "1", R_{in} is disabled and D_{in} is enabled. The data that is present at D_{in} while the clock is at "0" is shifted in and will be stored as the clock goes to a "1" This data must have been present t_{did} time prior to the clock "1" edge. The data must also remain in that same state for t_{dig} time after that edge. These times are necessary to insure proper data storage in the first register-cell.

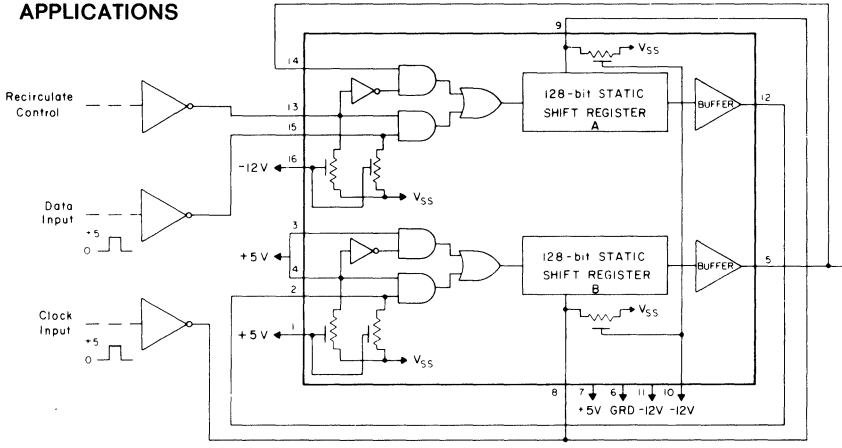
On the clock "1" edge, data is shifted through the register causing bit 127 to be shifted to position 128. This cell's output is buffered and appears at the output in the same logic polarity that appeared at the input 128 clocks prior. This data appears within t_{pd} time of the clock "1" edge.

R_{in} may be hardwired to the data output. When R_C is at a "0", R_{in} is enabled and D_{in} is disabled. Therefore, the output data will appear at the input of the first cell. When R_{in} is tied to the data output, the output delay will insure t_{dig} and t_{did} times. R_C "0" time must lead the clock "1" edge by t_{rid} time and must lag that edge by t_{rig} time to insure proper data storage when recirculate storage is desired.

TEST CIRCUIT



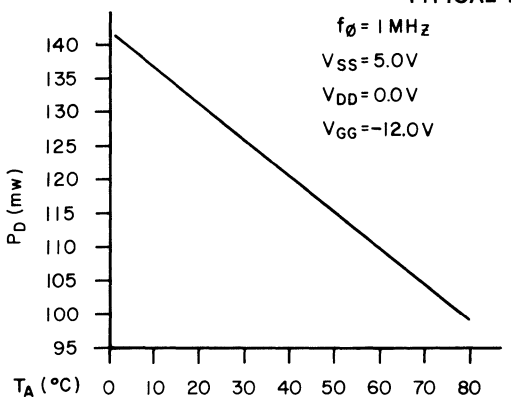
APPLICATIONS

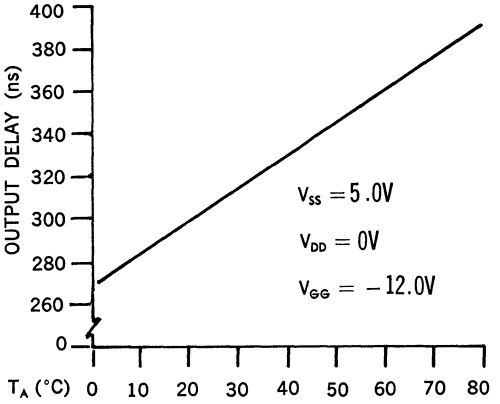


This shows the MK 1002 P connected to operate as a single, 256-bit, static shift register. Pull-up resistors are enabled at TTL driven inputs and disabled at MOS or DTL driven inputs. Any similar TTL/DTL device may be used in place of the inverters shown.

Inverters are 74-series TTL

TYPICAL PERFORMANCE





OPERATING NOTES

R_C	R_{in}	D_{in}	DATA ENTERED
1	X	1	1
1	X	0	0
0	1	X	1
0	0	X	0

"1" = V_{SS} = +5V

"0" = V_{DD} = Grd

X = No Effect

Output Logic: See Description.

MOSTEK

320-BIT DYNAMIC SHIFT REGISTER

MK 1007 P/N

FEATURES

- ☐ Ion-Implanted for full TTL/DTL compatibility
- ☐ Single-phase, TTL/DTL compatible clock
- ☐ Internal pull-up resistors
- ☐ Clock Frequency 10 kHz to 2.5 MHz
- ☐ Built-in recirculate logic for each register
- ☐ Power Supplies: +5V and −12V

DESCRIPTION

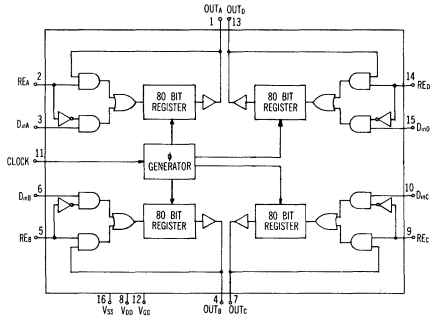
The MK 1007 P contains four separate 80-bit MOS dynamic shift registers on a single chip, using ion-implantation in conjunction with P-channel processing to achieve low threshold voltage and direct TTL/DTL compatibility. All logic inputs, including the single-phase Clock, can be driven directly from DTL or TTL logic. Pull-up resistors to +5V are provided for worst-case TTL inputs.

Each 80-bit register has independent inputs and outputs and a control input (RE) which allows external data to be shifted into the register (at logical 0) or data at the output to be recirculated into the register (at logical 1).

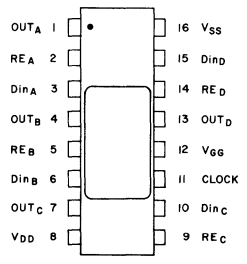
All four registers use a common (external) Clock input. With the Clock high (1), data is shifted into the registers. Following the negative-going edge of the Clock, data shifting is inhibited and output data appears. Output data is True, delayed 80 bits.

Since the MK 1007 P has zero lag-time requirements for data inputs, devices may be cascaded, i.e., the output of one device may be fed directly to the input of another device. All inputs are protected to prevent damage due to static charge accumulation.

FUNCTIONAL DIAGRAM



PIN CONNECTIONS



ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{DD} ..... V_{SS} + 0.3 V to V_{SS} − 20 V
Supply Voltage, V_{GG} ..... V_{SS} + 0.3 V to V_{SS} − 20 V
Voltage at any Input or Output ..... V_{SS} + 0.3 V to V_{SS} − 20 V
Operating Free-Air Temperature Range ..... 0°C to +75°C
Storage Temperature Range (Ceramic) ..... −65°C to +150°C
Storage Temperature Range (Plastic) ..... −55°C to +125°C

RECOMMENDED OPERATING CONDITIONS

($0°C \leq T_A \leq 75°C$)

	PARAMETER	MIN	TYP	MAX	UNITS	COMMENTS
POWER	V_{SS} Supply Voltage	4.75	5.0	5.25	V	V_{DD} = 0 V
	V_{GG} Supply Voltage[1]	−12.6	−12.0	−11.4	V	
INPUTS	V_{IL} Logic "0" Voltage, any input		0.0	0.8	V	
	V_{IH} Logic "1" Voltage, any input [2]	V_{SS} − 1.5	+5.0	V_{SS}	V	
INPUT TIMING	$f\phi$ Clock Repetition Rate	.01		2.5	MHz	NOTE: Total permitted clock times will be determined by clock frequency, $f\phi$.
	$t_{\phi p}$ Clock Pulse Width	.150		100	μs	
	$t_{\phi d}$ Clock Pulse Delay	.150		100	μs	
	$t_{\phi r}$ Clock Pulse Risetime	.010		5	μs	
	$t_{\phi f}$ Clock Pulse Falltime	.010		5	μs	
	t_{dld} Data Leadtime	150			ns	
	t_{dlg} Data Lagtime	0			ns	
	t_{rld} Recirculate Control Leadtime	200			ns	
	t_{rlg} Recirculate Control Lagtime	50			ns	

ELECTRICAL CHARACTERISTICS

(V_{SS} = +5 ±0.25 V, V_{GG} = −12 ±0.6V, V_{DD} = 0V, T_A = 0°C to +75°C, unless otherwise specified.)

	PARAMETER	MIN	TYP[3]	MAX	UNITS	CONDITIONS
POWER	I_{SS} V_{SS} Power Supply Current[4][5]		22.0	40.0	mA	$f\phi$ = 2.5 MHz;
	I_{GG} V_{GG} Power Supply Current[5]		9.0	16.0	mA	outputs open
INPUTS	C_{IN} Capacitance at Data, RE, and Clock Inputs[5]		3	6	pF	$V_I = V_{SS}$, $f\phi$ = 1 MHz
	I_{IL} Logic "0" Current, any input[5]	0.6	1.1	1.6	mA	V_I=0.4 V
	$I_{I(lk)}$ Leakage Current, any input			1	μA	$V_I=V_{SS}-5.5V$; $V_{SS}=V_{DD}=V_{GG}$
	R_{IN} Input Pullup Resistance[5]	3.0		8.4	kΩ	V_I=0.4 V
OUTPUTS	V_{OL} Logic "0" Output Voltage[5]			0.4	V	I_L = −1.6 mA
	V_{OH} Logic "1" Output Voltage[5]	V_{SS} − 1			V	I_L = +100 μA
DYN. CHAR.	t_{DLH} Output Delay, Low to High		75	200	ns	See Timing Diagrams
	t_{DHL} Output Delay, High to Low		75	200	ns	
POWER DIS.	$P_{D(1)}$ Power Dissipation[4]		220		mW	$f\phi$ = 2.5 MHz
	$P_{D(2)}$ Power Dissipation[4]		195		mW	$f\phi$ = 1 MHz
	$P_{D(3)}$ Power Dissipation[4]		170		mW	$f\phi$ = 10 kHz

NOTES:

(1) Other supply voltages are permissible providing that supply and input voltages are adjusted to maintain the same potential relative to V_{SS}, e.g., V_{SS}=0 V, V_{DD}= −5V, V_{GG}= −17 V.
(2) Pull-up resistances to +5V are provided internally.
(3) Typical values at T_A=25°C, V_{SS}=+5.0 V, V_{DD}=−12.0 V.
(4) I_{SS} will increase a maximum of 1.6 mA for each input at logic "0."
(5) At T_A=25°C.

TIMING

CONDITIONS:

1. All timing relationships apply to any of the four registers.
2. Logic 0 is defined as V_{DD} or ground; logic 1 as V_{SS} or +5V.

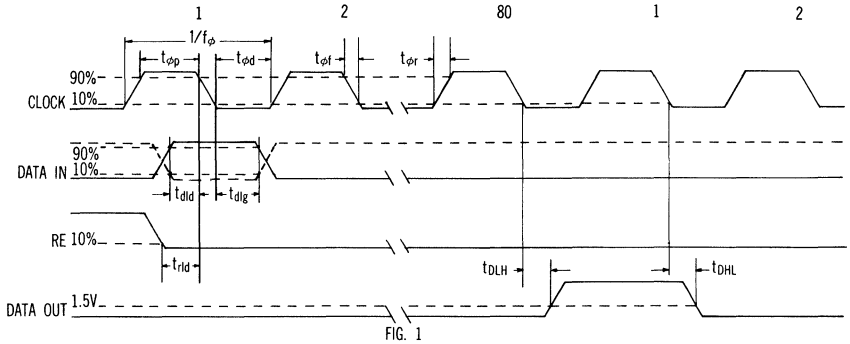


FIG. 1

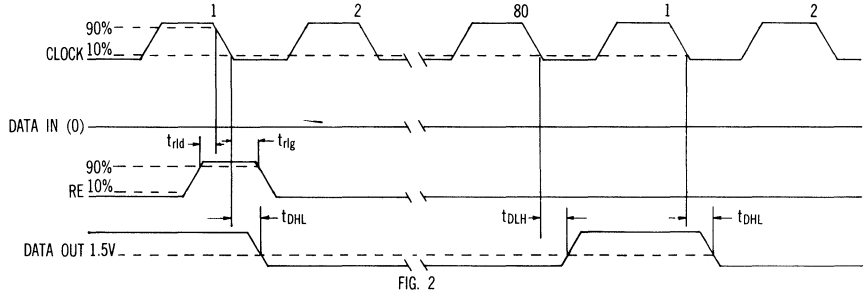
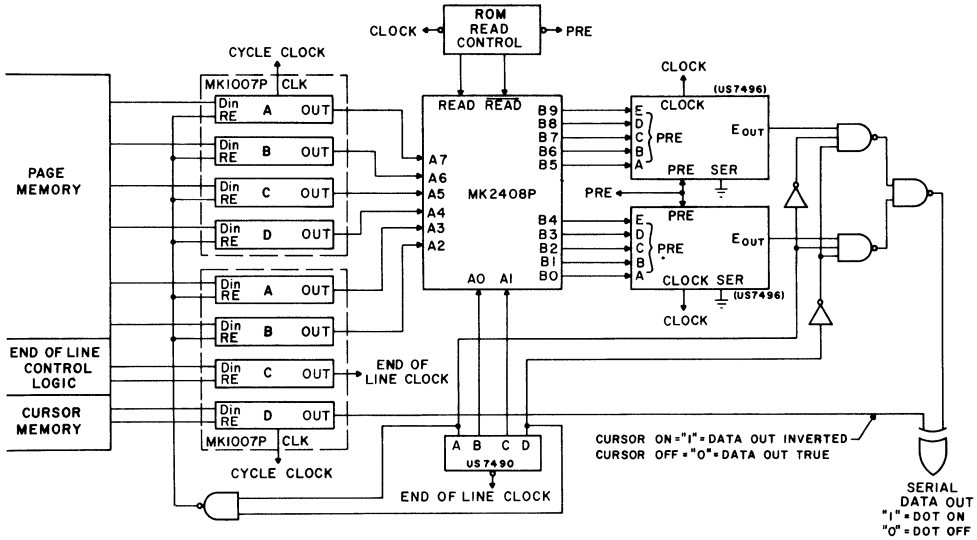


FIG. 2

SHIFT: Fig. 1 illustrates shifting a logic 1 bit from the Data Input (D_{in}) through one of the 80-bit registers. RE (Recirculate Enable) at logic 0 enables D_{in}. RE must go to logic 0 for t_{rld} time (Recirculate Control Leadtime) prior to the Clock's negative edge, and must maintain that state at least until the Clock's negative edge (t_{dlg}) to insure proper data shifting. This data bit entered will appear 80 clock pulses later within Output Delay Time (t_D) of that Clock's negative edge.

RECIRCULATE: Fig. 2 illustrates recirculating a bit present at the output back through the register. RE must attain a logic 1 for t_{rld} time (Recirculate Control Leadtime) prior to the Clock's negative edge, and must maintain that state at least until the Clock's negative edge (t_{rlg}) to insure proper data recirculation. The bit entered will appear 80 clocks later as shown.

APPLICATIONS



LINE REFRESH MEMORY FOR CRT DISPLAY

This application shows the MK 1007 P used as the Line Refresh Memory, driving MOSTEK's MK 2408 P TTL-compatible character generator. The MK 1007 P receives new data from the Page Memory (which may also consist of MK 1007 P's) on the tenth row of any character line, this being the third vertical space between rows of characters. The MK 1007 P recirculates the character-address data as these characters are scanned and displayed on a CRT screen.

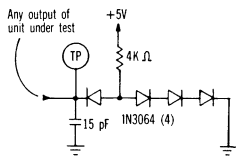
The decade counter selects the appropriate rows from the character generator which outputs two rows of the addressed character at one time (see MK 2408 P data sheet), and also controls the multiplexed output of the character generator so that only one row of the addressed characters is displayed on any CRT horizontal sweep.

One stage of the MK 1007 P may be used to shift a single data bit, which may be used to determine the end of the horizontal sweep. Another stage may be used as a cursor control and, as shown above, may blank the cursored character dots while surrounding dots are on, to give a reverse image of that particular character.

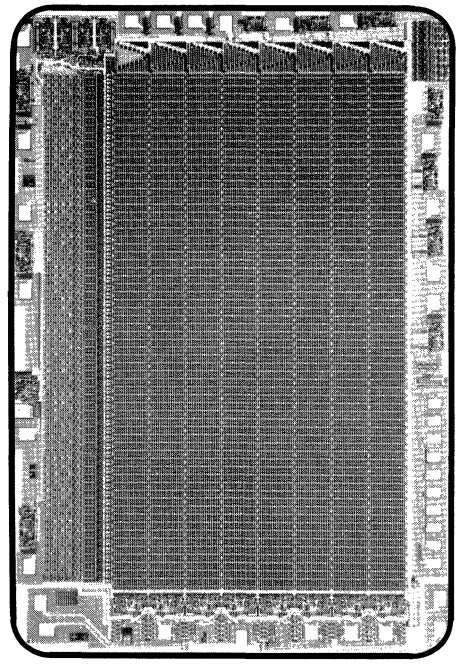
OPERATING NOTES

1. Recirculate Enable (RE) = Logic 1 = output data recirculated.
2. Output data (delayed 80 bits) maintains same logic state when RE = 1.
3. Recirculate Enable (RE) = Logic 0 = Data In (D_{in}) enabled.
4. Output data (delayed 80 bits) attains same logic state as D_{in} when RE = 0.
5. Output data follows the clock negative edge.

TEST CIRCUIT



READ ONLY MEMORIES



MOSTEK

2240-BIT ROM CHARACTER GENERATORS

MK 2300/ 2302 P/N

FEATURES

- ☐ Ion-implantation processing for full TTL/DTL compatibility
- ☐ 2240 bits of storage organized as 64 5x7 dot matrix characters with column-by-column output
- ☐ MK 2302 P is pre-programmed with ASCII encoding
- ☐ Internal counter provides clocked column selection
- ☐ Counter output for updating external character address registers
- ☐ Internal provision for one- or two-column inter-character spacing
- ☐ Output enable and blanking capability
- ☐ Operates from +5V and −12V supplies

DESCRIPTION

The MK 2300 P Series MOS, TTL/DTL-compatible read-only memories (ROMs) are designed specifically for dot-matrix character generation. Each ROM provides 2240 bits of programmable storage, organized as 64 characters each having 5 columns of 7 bits. A row output capability of 64 7x10 characters is possible, as illustrated on the back page.

Low threshold-voltage processing, utilizing ion-implantation, is used with P-channel, enhancement-mode MOS technology to provide direct input/output interface with TTL and DTL logic families. All inputs are protected to prevent damage from static charge accumulation.

The MK 2302 P is preprogrammed with ASCII-encoded characters (font shown on back page). Other ROMs in the series are programmed during manufacture to customer specifications by modification of a single mask.

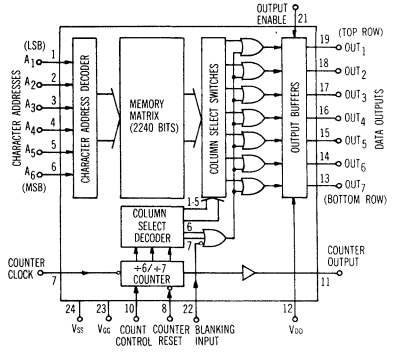
Characters are selected by a six-bit binary word at the Character Address inputs. Each character consists of five columns, the columns selected by an internal counter which is clocked by the Counter Clock input. Column information appears sequentially beginning with the left-most column. Two additional intercharacter spacing columns are available, selectable for one or two spaces by the Count Control Input. During the spacing, the Data Outputs are high (+5V), or the "dot-off" condition. After the last space, the modulo counter automatically increments to the leftmost column.

Synchronizing other system components with the ROM is possible using the Counter Reset Input to reset the counter to the last intercharacter spacing column, or using the Counter Output which occurs only on the last spacing column.

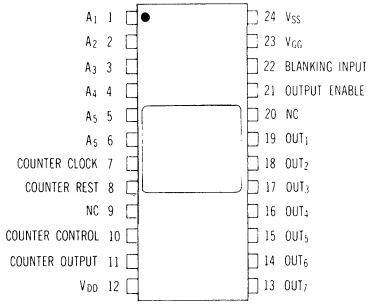
The Blanking Input allows all Data Outputs to be driven high (+5V) without affecting any other ROM functions. The Output Enable input allows the outputs to be open-circuited for wire-ORing.

Memory operation is static; refresh clocks are not required to maintain output information. The Clock input is used only to select columns and need not be pulsed continuously.

FUNCTIONAL DIAGRAM



PIN CONNECTIONS



NC = NO CONNECTION

ABSOLUTE MAXIMUM RATINGS

Voltage on any terminal relative to V_{SS} ..... +0.3V to −20V
Operating temperature range ..... 0°C to +75°C
Storage temperature (Ambient) Ceramic ..... −65°C to + 150°C
Storage temperature (Ambient) Plastic ..... −55°C to + 125°C

RECOMMENDED OPERATING CONDITIONS ($0°C \leq T_A \leq 75°C$)

		PARAMETER	MIN	TYP	MAX	UNITS	COMMENTS
POWER	V_{SS}	Supply voltage	+4.75	+5.0	+5.25	V	
	V_{DD}	Supply voltage	—	0.0	—	V	See note 1
	V_{GG}	Supply voltage	−12.6	−12.0	−11.4	V	
INPUTS	$V_{in(0)}$	Input voltage, logic "0"			+0.6	V	See note 2
	$V_{in(1)}$	Input voltage, logic "1"	$V_{SS}-1.5$			V	Count control input should be
	$V_{in(cc)}$	Count Control input voltage, ÷ 6		−12.0	−11.4	V	returned to V_{GG} for ÷ 6 oper-
		÷ 7	+4.75	+5.0		V	ation, or V_{SS} for ÷ 7 operation
COUNTER TIMING	f_{clk}	Counter Clock input frequency	0		200	kHz	
	$t_{clk(0)}$	Clock time at logic "0"	2			μs	
	$t_{clk(1)}$	Clock time at logic "1"	2			μs	See timing
	$t_{r(clk)}$	Clock rise time			0.1	μs	diagrams
	$t_{f(clk)}$	Clock fall time			0.1	μs	
	t_{rp}	Reset pulse width	1.0			μs	
	t_{crd}	Clock-to-reset pulse delay	0.4			μs	See note 4

ELECTRICAL CHARACTERISTICS

(V_{SS} = +5.0V ±0.25V, V_{GG} = −12.0V ±0.6V, 0°C ≤ T_A ≤ +75°C, unless noted otherwise)

		PARAMETER	MIN	TYP*	MAX	UNITS	CONDITIONS
POW	I_{SS}	Supply current (V_{SS})		20	40	mA	Outputs unconnected
	I_{GG}	Supply current (V_{GG})		20	40	mA	f_{clk} = 200 kHz
INPUTS	C_{in}	input capacitance			10	pF	$V_{in}=V_{SS}$, f_{meas} = 1MHz
	I_{in}	Input leakage current			10	μA	$V_{in}=V_{SS}-6V$, T_A = 25°C
							See note 2
OUTPUTS	$V_{out(0)}$	Output voltage, logical "0"		0.2	0.4	V	I_{out} = 2.0 mA (into output)
	$V_{out(1)}$	Output voltage, logical "1"	2.4			V	I_{out} = 0.6 mA (out of output)
							See note 3
	I_{out}	Data Output leakage current	−10		+10	μA	$V_{SS}-6V \leq V_{out} \leq V_{SS}$, T_A = 25°C (outputs disabled)
DYNAMIC CHARACTERISTICS	t_{AO}	Address-to-output delay time			1	μs	
	t_{CO}	Clock-to-output delay time			1	μs	
	t_{CCO}	Clock-to-counter output delay time			1	μs	Rise and fall times included in delay times
	t_{BO}	Blanking/unblanking delay time			1	μs	See timing diagrams
	t_{OEO}	Output enable/disable delay time			1	μs	
	t_{CRO}	Counter reset delay time			1	μs	R_L = 4 kΩ to V_{SS}
	t_{CRCO}	Reset-to-counter output delay time			1	μs	C_L = 15 pF to V_{DD}
	t_F	Output fall time			0.3	μs	T_A = 25°C
	t_R	Output rise time			0.3	μs	

*Typical values apply at V_{SS} = +5.0V, V_{GG} = −12.0V, T_A = 25°C

NOTES:
1. Supply voltages shown are for operation in a TTL/DTL system. Other supply voltages may be used if V_{DD} and V_{GG} maintain the same relationship to V_{SS}, e.g., V_{SS} = OV, V_{DD} = −5V, V_{GG} −17V. Input voltages would also need to be adjusted accordingly.
2. These parameters apply to the character address, counter clock, counter reset, blanking, and output enable inputs.
3. These parameters apply to both the data outputs and counter output.
4. The counter clock must not make a negative transition within the period tcrd, before or after a positive counter reset transition. The counter reset negative edge may occur any time.

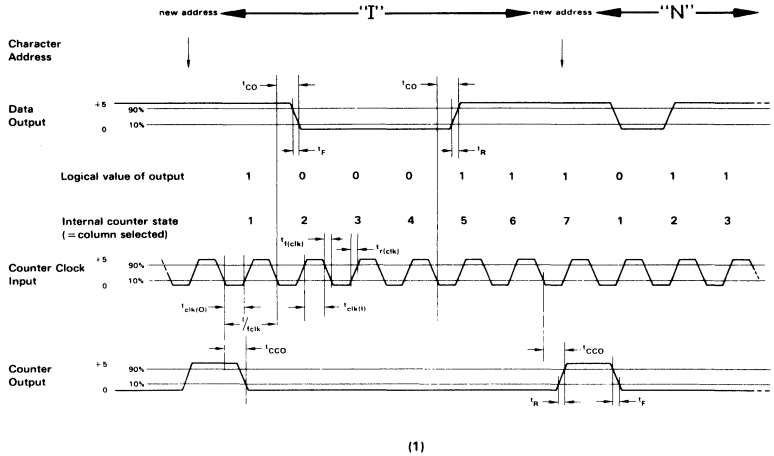
TIMING

(waveforms not to scale)

Timing diagram (1)* shows the time relationships between character address, data output, counter clock, and counter output during typical operation of an MK 2300 P Series character generator. An output sequence from the MK 2302 P is shown to help clarify operation. This sequence can be seen from the top rows (OUT_i) of the characters "I" and "N".

	"I"							"N"			
OUT_1	1	0	0	0	1	1	1	0	1	1	1
	1	1	0	1	1	1	1	0	1	1	1
	1	1	0	1	1	1	1	0	0	1	1
	1	1	0	1	1	1	1	0	1	0	1
	1	1	0	1	1	1	1	0	1	1	0
	1	1	0	1	1	1	1	0	1	1	1
OUT_7	1	0	0	0	1	1	1	0	1	1	1

COUNT OF 7



(1)

All timing relationships shown in diagram (1) apply to any other output or combination of characters as well.

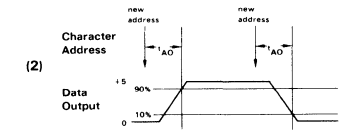
Relevant input conditions assumed but not shown in timing diagram (1) are as follows:

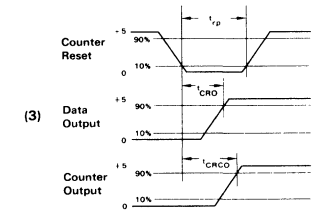
Count Control, +5V
Counter Reset, +5V
Blanking Input, +5V
Output Enable, +5V

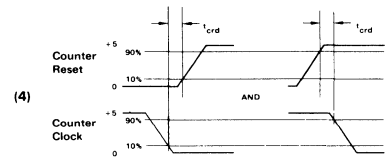
Had the Count Control input been at −12V, the counter sequence would have been six positions instead of seven and the Counter Output would have been high during the sixth position.

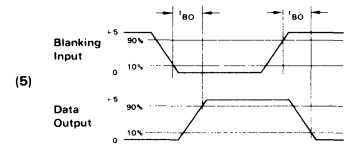
New character addresses are shown coinciding with the rising edge of the Counter Output waveform in diagram (1). This condition was selected to demonstrate use of the Counter Output to advance an external input register to a new character address. Character addresses can be changed at any other time as well. Timing diagram (2) depicts output response to a character address change when, for example, the counter is stationary in one of the five character column positions.

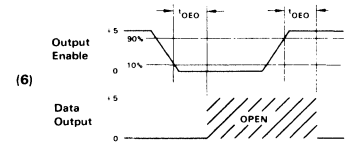
Timing diagrams (3) through (6) show timing relationships for the Counter Reset, Blanking Input, and Output Enable. The "open" condition in (6) implies that both the pull-up and pull-down devices in each data output push-pull buffer are turned off.











OPERATING NOTES

The following table summarizes the MK 2300 P Series input control states and corresponding drive levels:

Count Control	
÷6	−12V
÷7	+5V
Counter Reset	
operate	+5V
reset	0V
Blanking Input	
unblank	+5V
blank*	0V
Output Enable	
enable	+5V
disable**	0V

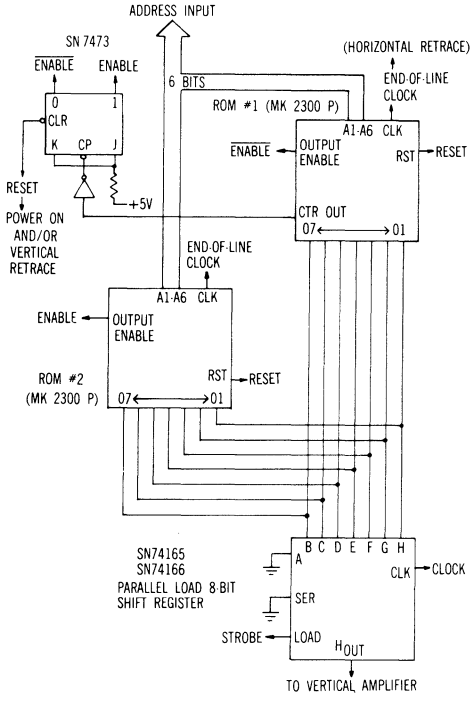
*All data outputs high (+5V)
**All data outputs open-circuited

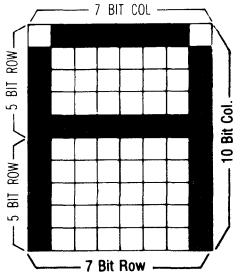
APPLICATION:
7x10 CHARACTER GENERATOR

ROM CODING

7x10 Non-Interlace Configuration: (As illustrated) For row-out (7-bit) horizontal raster-scan application, code ROM #1 for Rows 1 through 5; and ROM #2 for Rows 6 through 10.

7x10 Interlace (525-line): Code ROM #1 for Rows 1, 3, 5, 7, 9; Code ROM #2 for Rows 2, 4, 6, 8, 10. The Enable Flip-flop should be changed to clock only at vertical retrace time, thus allowing ROM #1 to be enabled for the 1st page sweep (262 ½ lines) and then allowing ROM #2 to be enabled for the interlaced 2nd page sweep of 262 ½ lines.



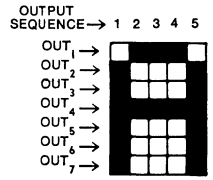


Combining two 5x7 column-output ROMs provides a 7x10 row output.

MK 2302 P

Logic 1 = input @ +5V
Logic 0 = input @ 0V

Output dot "on" = 0V
Output dot "off" = +5V



A_4	A_3	A_2	A_1	A_6 1 1 0 0 / A_5 0 1 0 1
0	0	0	0	
0	0	0	1	
0	0	1	0	
0	0	1	1	
0	1	0	0	
0	1	0	1	
0	1	1	0	
0	1	1	1	
1	0	0	0	
1	0	0	1	
1	0	1	0	
1	0	1	1	
1	1	0	0	
1	1	0	1	
1	1	1	0	
1	1	1	1	

MOSTEK ROM PUNCHED-CARD CODING FORMAT[1]

MK 2300 P

Cols.	Information Field
First Card	
1-30	Customer
31-50	Customer Part Number
60-72	Mostek Part Number[2]
Second Card	
1-30	Engineer at Customer Site
31-50	Direct Phone Number for Engineer
Third Card	
1-5	Mostek Part Number[1]
10-15	Organization[2]
Fourth Card	
1-6	Data Format[3] — "MOSTEK"
15-28	Logic[4] — "Positive Logic" or
35-57	Verification Code[5]
Data Cards [4]	
1-6	Binary Address
8-12	First row of character
14-18	Second row of character
20-24	Third row of character
26-30	Fourth row of character
32-36	Fifth row of character
38-42	Sixth row of character
44-48	Seventh row of character

Notes: 1. Assigned by Mostek Marketing Department; may be left blank.

2. Punched as 64x5x7.

3. "MOSTEK" format only is accepted on this part.

4. A dot "ON" should be coded as a "1".

5. Punched as: (a) VERIFICATION HOLD — i.e. the customer verification of the data as reproduced by MOSTEK is required prior to production of the ROM. To accomplish this MOSTEK supplies a copy of its Customer Verification Data Sheet (CVDS) to the customer.
   (b) VERIFICATION PROCESS — i.e. the customer will receive a CVDS but production will begin prior to receipt of customer verification.
   (c) VERIFICATION NOT NEEDED — i.e. the customer will not receive a CVDS and production will begin immediately.

MOSTEK

2560x1 BIT STATIC ROM

MK 2400 P

FEATURES

- ☐ Ion-implanted for full TTL/DTL compatibility
- ☐ Chip enable permits wire-ORing
- ☐ Custom-programmed memory requires single mask modification
- ☐ 550 ns cycle time ($0° \leqslant T_A \leqslant 75°C$)
- ☐ Static output storage latches
- ☐ Optional 3-bit, chip-select decoder available
- ☐ 2560 bits of storage, organized as 256 10-bit words
- ☐ Operates from +5V and −12V supplies

DESCRIPTION

The MK 2400 P Series TTL/DTL-compatible MOS Read-Only Memories (ROM's) are designed for a wide range of general-purpose memory applications where large quantity bit storage is required. Each ROM provides 2560 bits of programmable storage, organized as 256 words of 10 bits each. Low threshold-voltage processing, utilizing ion implantation with P-channel enhancement-mode MOS technology, provides direct input/output interface with TTL and DTL logic.

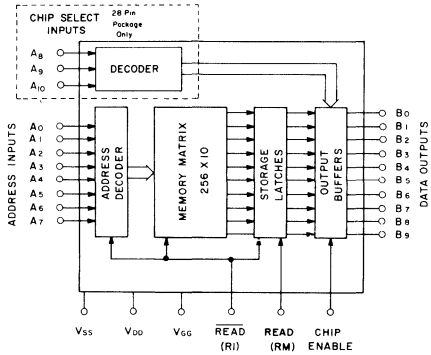
Programming is accomplished during manufacture by modification of a single mask, according to customer specifications. The MK 2400 P Series is available in either 24-lead or 28-lead ceramic dual-in-line packages. On the 28-pin ROM, an optional Chip Select Decoder may also be programmed according to customer specifications to provide a 3-bit Chip Select Code.

Operation involves transferring addressed information from the memory matrix into the storage latches using the READ and $\overline{\text{READ}}$ inputs (see Timing). Information stored in the latches will remain despite address changes or chip disabling until the READ and $\overline{\text{READ}}$ inputs are again cycled. READ and $\overline{\text{READ}}$ input signals may be generated from separate timing circuits if desired, or either may be the inverse of the other.

The Chip Enable input forces the normally push-pull output buffer stages to an open-circuit condition when disabling the chip. If desired, new data can be stored in the storage latches while the chip is disabled. When the chip is reenabled, this data would be present at the outputs.

All inputs are protected against static charge accumulation. Pull-up resistors on all inputs are available as a programmable option.

FUNCTIONAL DIAGRAM



OPERATING NOTES

CHIP ENABLE	READ	$\overline{\text{READ}}$	OUTPUT
0	X	X	A
1	0	1	B
1	1	0	C

"1" = V_{SS} (+5V): "0" = V_{DD} (0V)

X = No effect on output

A = Output open-circuited

B = Output retains data last stored in latches

C = Output assumes state of addressed cells

Voltage on any terminal relative to V_{SS} ..... +0.3V to −10V
Operating temperature range ..... 0°C to +75°C
Storage temperature range ..... −65°C to +150°C

RECOMMENDED OPERATING CONDITIONS ($0°C \leq T_A \leq 75°C$)

	PARAMETER		MIN	TYP	MAX	UNITS	COMMENTS
POWER	V_{SS}	Supply voltage	+4.75	+5.0	+5.25	V	
	V_{DD}	Supply voltage	—	0.0	—	V	See note 1
	V_{GG}	Supply voltage	−12.6	−12.0	−11.4	V	
INPUTS	$V_{in(o)}$	Input voltage, logic "0"		0	+0.8	V	Pull-up resistors (≈5KΩ) to
	$V_{in(l)}$	Input voltage, logic "1"	$V_{SS}-1.5$	V_{SS}		V	V_{SS} available as programmable option.
INPUT TIMING	t_{cyc}	Address change cycle time	550			ns	
	t_{id}	Address to $\overline{\text{Read}}$ lead time	250			ns	
	t_{lg1}	Read lag time 1	−.05		.05	μs	See
	t_{lg2}	Read lag time 2	−.05		.05	μs	Timing
	$t_{\overline{rd}}$	$\overline{\text{Read}}$ pulse width	300			ns	Section
	t_{rd}	Read pulse width	0.3		100	μs	
	t_r	Rise time, any input			100	ns	
	t_f	Fall time, any input			100	ns	

ELECTRICAL CHARACTERISTICS ($V_{SS}=+5.0V \pm 0.25V$, $V_{GG}=-12.0V \pm 0.6V$, $0°C \leq T_A \leq +75°C$, unless noted otherwise. Pull-up resistors not programmed.)

	PARAMETER		MIN	TYP*	MAX	UNITS	CONDITIONS
POWER	I_{SS}	Supply current (V_{SS})		12	25	mA	Outputs unconnected
	I_{GG}	Supply current (V_{GG})		−12	−25	mA	See Note 2 and Note 3
INPUTS	C_{in}	Input capacitance		5	10	pF	$V_{in}=V_{SS}$, $f_{meas}=1MHz$
	I_{in}	Input leakage current			10	μA	$V_{in}=V_{SS}-6V$ $T_A=25°C$
OUTPUTS	$V_{out(o)}$	Output voltage, logical "0"			0.4	V	$I_{out}=1.6$ mA (into output) — See note 3 and Figure #1
	$V_{out(l)}$	Output voltage, logical "1"	2.4			V	$I_{out}=0.4$ mA (out of output); $V_{SS}-6V \leq V_{out} \leq V_{SS}$
	I_{out}	Output leakage current	−10		+10	μA	$T_A=25°C$ (outputs disabled)
DYNAMIC CHARACTERISTICS	t_{ACC}	Address-to-output access time			600	ns	$t_{id}=250ns$, $t_{lg1}=0$, $t_{lg2}=0$, See note 4 — See timing Section and Figure #1
	t_{OD}	Output delay time			350	ns	
	t_{OEO}	Output enable/disable time		125	300	ns	
	t_{CS}	Chip Select to Output Delay			600	ns	
	t_{CD}	Chip Deselect to Output Delay			600	ns	

*Typical values apply at $V_{SS}=+5.0V$, $V_{GG}=-12.0V$, $T_A=25°C$

NOTES: 1. Supply voltages shown are for operation in a TTL/DTL system. Other supply voltages may be used if V_{DD} and V_{GG} maintain the same relationship to V_{SS}, e.g., $V_{SS}=0V$, $V_{DD}=-5V$, $V_{GG}=-17V$. Input voltages would also need to be adjusted accordingly.

2. Max measurements at 0°C. (MOS supply currents increase as temperature decreases.) I_{SS} will increase 1.6mA (max) for each input at logic 0 when pull-up resistors are programmed.

3. Unit operated at minimum specified cycle time.

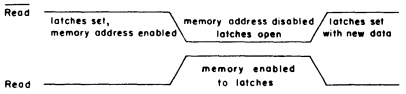
4. The outputs become open circuited when disabled or deselected. As shown in Fig. 1, an output with a "1" expected out does not transition through the 1.5V point when enabled (selected) or disabled (deselected); this is true because the TTL equivalent load pulls the open-circuited output to approximately 2 volts.

TIMING

Notes:

1. All times are referenced to the 1.5V point relative to V_{DD} (ground) except rise and fall time measurements.
2. Chip enable = V_{SS} for all measurements except when measuring T_{OEO}.
3. Logic 0 is defined as V_{DD} or ground; logic 1 as V_{SS} or +5V.

INTERNAL FUNCTION OF READ/$\overline{\text{READ}}$ SIGNALS

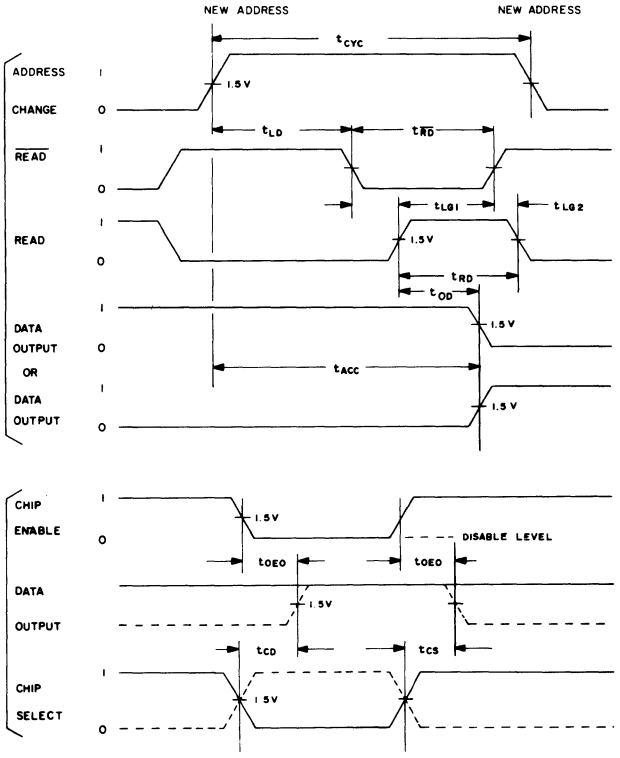


Set up time, t_{id}, allows the input address to propagate through the address decoder and memory matrix prior to $\overline{\text{READ}}$ logic 0 time. As indicated above, $\overline{\text{READ}}$ at a logic 0 internally disables the input address so that an external address change may occur without affecting the location previously selected. The latches are also readied to receive new data which is enabled from the matrix when $\overline{\text{READ}}$ is at a logic 1. Data is set in the latches when READ is allowed to rise back to its logic 1 state. In actual use, the READ rising and falling edges can precede the falling and rising edges of $\overline{\text{READ}}$, respectively, as implied by the specification of negative read lag times. This allows a very flexible timing relation between the two pulses, in that either input can be the inversion of the other or both may be generated from separate timing circuits.

Output data appears following the rise of the READ pulse but correct output data will not appear until $\overline{\text{READ}}$ has gone low. For this reason, $\overline{\text{READ}}$ is shown preceding READ even though other relationships are allowed. If READ is made to precede $\overline{\text{READ}}$, delay time, t_{OD}, should be referenced to the fall of $\overline{\text{READ}}$ rather than as shown.

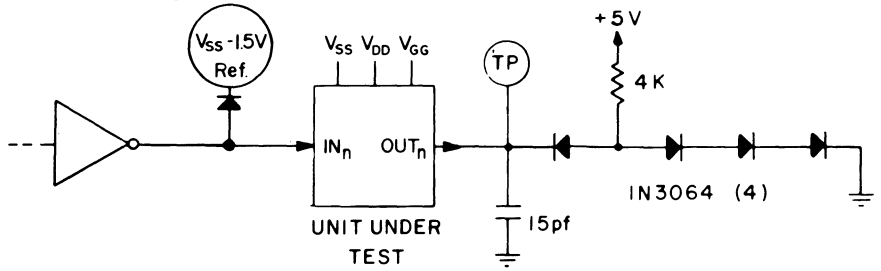
The chip is disabled by applying a logical 0 to the chip enable input, forcing the outputs to an open-circuit condition. The output data present at the time of disable will again be present upon re-enabling unless a new read cycle was initiated for a different address while the chip was disabled, in which case the new data would be present at the outputs.

The programmable 3-bit chip select timing would be the same as the address inputs.

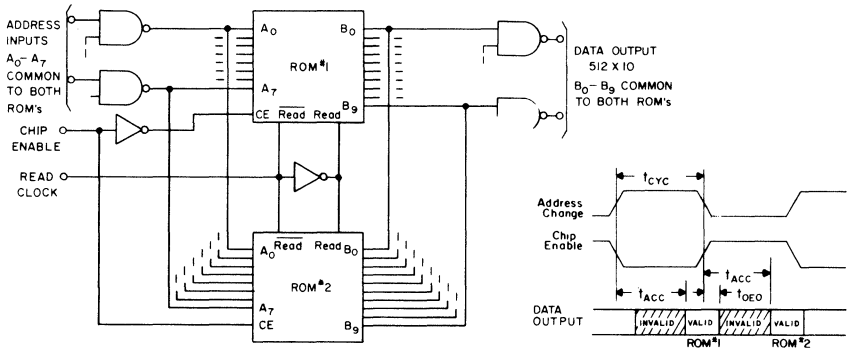


NOTE: Wave forms are not to scale.

FIGURE #1 t_{ACC} and t_{DD} test circuit



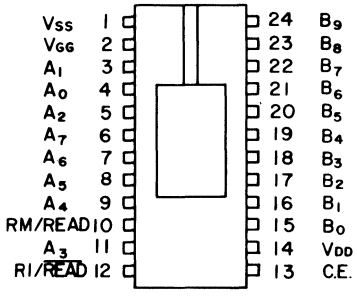
APPLICATIONS



Application shows wire-Or'ing for expansion to a 512 X 10 memory. Further expansion is possible by 1 of N decoding to the Chip Enable input (or with the optional 3-bit decoder) while maintaining the time relationships shown. t_{cyc} should include the desired data-valid time. Interface devices may be TTL or DTL.

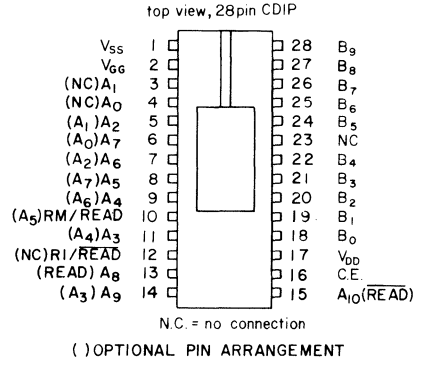
PIN CONNECTIONS

top view, 24 pin CDIP



PIN CONNECTIONS

top view, 28 pin CDIP



N.C. = no connection

( ) OPTIONAL PIN ARRANGEMENT

MOSTEK ROM PUNCHED-CARD CODING FORMAT[1]

MK 2400 P

Cols.	Information Field
First Card	
1-30	Customer
31-50	Customer Part Number
60-72	Mostek Part Number[2]
Second Card	
1-30	Engineer at Customer Site
31-50	Direct Phone Number for Engineer
Third Card	
1-5	Mostek Part Number[2]
10-16	Organization[3]
29	A8[4]
30	A9[4]
31	A10[4]
32	Pull-up Resistor[5]
Fourth Card	
0-6	Data Format[6] — "MOSTEK"
15-28	Logic — "Positive Logic" or "Negative Logic"
35-57	Verification Code[7]
60-74	Package Choice[8]
Data Cards	
1-3	Decimal Address
5	Output B9
6	Output B8
7	Output B7
8	Output B6
9	Output B5
10	Output B4
11	Output B3
12	Output B2
13	Output B1
14	Output B0
16	Octal Equivalent of: B9[9]
17	Octal Equivalent of: B8, B7, B6[9]
18	Octal Equivalent of: B5, B4, B3[9]
19	Octal Equivalent of: B2, B1, B0[9]

Notes: 1. Positive or negative logic formats are accepted as noted in the fourth card.

2. Assigned by Mostek Marketing Department; may be left blank.

3. Punched as 0256x10.

4. A "0" indicates the chip is enabled by a logic 0, a "1" indicates it is enabled by a logic 1, and a "2" indicates a "Don't Care" condition.

5. A "1" indicates pull-ups; a "0" indicates no pull-ups.

6. "MOSTEK" format only is accepted on this part.

7. Punched as:
   (a) VERIFICATION HOLD — i.e. customer verification of the data as reproduced by MOSTEK is required prior to production of the ROM. To accomplish this MOSTEK supplies a copy of its Customer Verification Data Sheet (CVDS) to the customer.
   (b) VERIFICATION PROCESS — i.e. the customer will receive a CVDS but production will begin prior to receipt of customer verification.
   (c) VERIFICATION NOT NEEDED — i.e. the customer will not receive a CVDS and production will begin immediately.

8. "24 PIN", "28 PIN STANDARD", or "28 PIN OPTIONAL" (left justified to column 60).

9. The octal parity check is created by breaking up the output word into groups of three from right to left and creating a base 8 (octal) number in place of these groups. For example the output word 1010011110 would be separated into groups 1/010/011/110 and the resulting octal equivalent number is 1236.

MOSTEK

2560x1 ROM CHARACTER GENERATOR

MK 2408 P

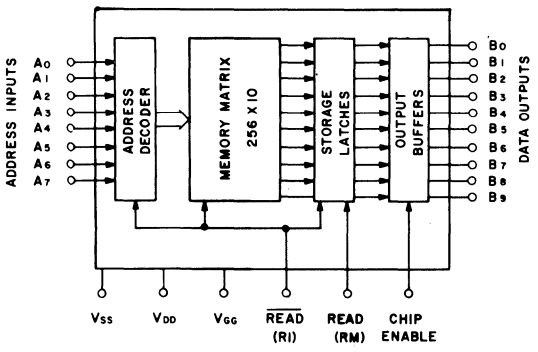
DESCRIPTION

The MK 2408 P is a pre-programmed member of the MK 2400 P Series. It is programmed as a dot-matrix character generator (64 characters) with ASCII encoded inputs and row (5-bit) outputs. The MK 2408 P outputs two rows at the same time. Row 1 is available at outputs B9 (left), B8, B7, B6, and B5 (right) while row 2 is available at outputs B4 (left), B3, B2, B1, and B0 (right). Row 3 is available at B9 through B5 while row 4 is available at B4 through B0. Row 5 and row 6 are available at B9 through B5 and B4 through B0. Row 5 and row 6 are available at B9 through B5 and B4 through B0. Row selection is determined by the address combination of bits A0 and A1.

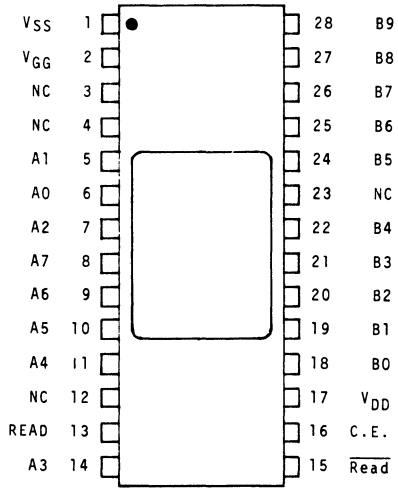
The MK 2408 P meets and operates by the specifications outlined in the MK 2400 P Series data sheet (DS-24001270-2)

The example in Figure 1 demonstrates the correspondence of the device outputs and row select sequence to the 7 x 5 dot-matrix font. The complete character font patterns (truth table) are illustrated on the back. A logic 1 or a DOT represents an input or output voltage equal to V_{SS} (+5V) and a logic 0 or a blank represents a voltage equal to V_{DD} (OV). The eighth row outputs (B4 through B0 when inputs A1 and A0 equal logic 1) are not illustrated since in each case they are equal to all 0's.

FUNCTIONAL DIAGRAM



PIN CONNECTIONS



NC= NO CONNECTION

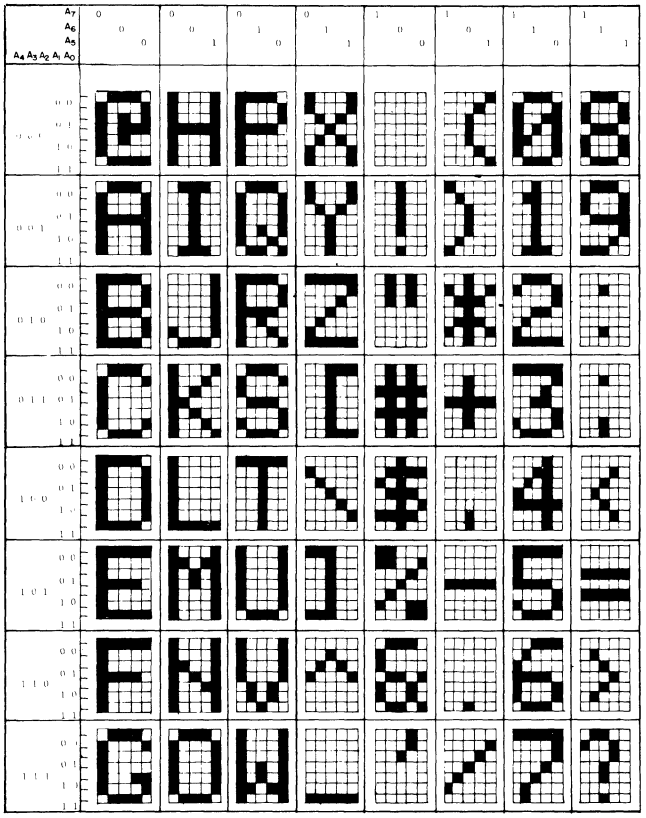
A1	A0		B9 B4	B8 B3	B7 B2	B6 B1	B5 B0		
0	0	—	1	0	0	0	1	--	B9-B5
		—	1	1	0	1	1	--	B4-B0
0	1	—	1	0	1	0	1	--	B9-B5
		—	1	0	1	0	1	--	B4-B0
1	0	—	1	0	0	0	1	--	B9-B5
		—	1	0	0	0	1	--	B4-B0
1	1	—	1	0	0	0	1	--	B9-B5
		—	0	0	0	0	0	--	B4-B0

A7 = 0
A6 = 0
A5 = 1

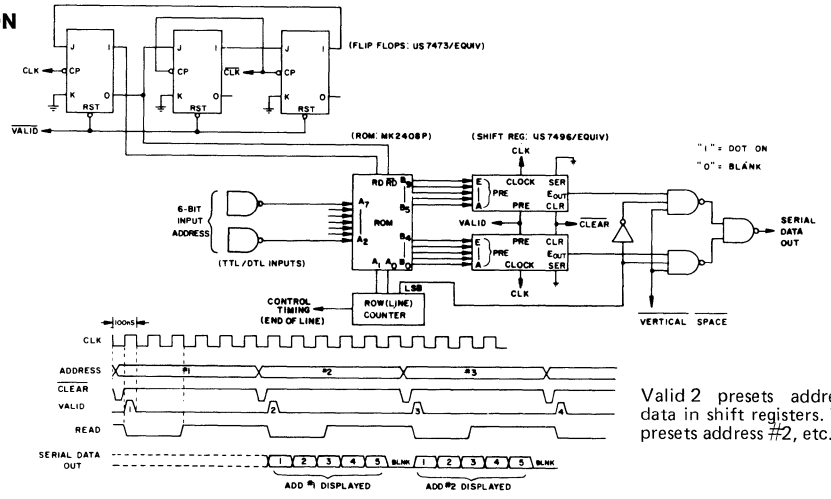
A4 = 1
A3 = 0
A2 = 1

FIGURE 1

CODING & CHARACTER FONTS



APPLICATION



Valid 2 presets address #1 data in shift registers. Valid 3 presets address #2, etc.

MOSTEK

4096x1 BIT STATIC ROM

MK 2500/2600 P

FEATURES

- ☐ High-speed, static operation — 400 nsec. typical access time
- ☐ Active input pull-ups provide worst-case TTL compatibility
- ☐ Push-pull outputs provide three output states: one, zero, and open
- ☐ Ion-implantation for constant current loads and lower power
- ☐ Standard power supplies: +5V, −12V
- ☐ MK 2500 P is pin-for-pin replacement for National 5232
- ☐ MK 2600 P is pin-for-pin replacement for Fairchild 3514

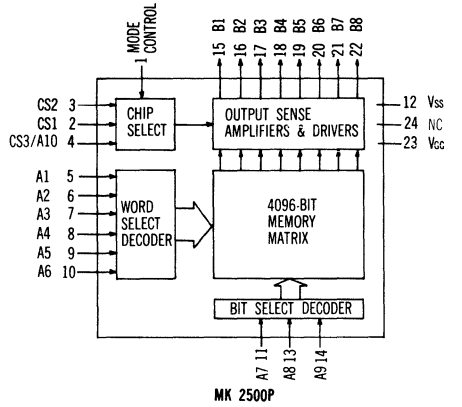
DESCRIPTION

The MK 2500 P and MK 2600 P series of TTL/DTL compatible MOS read-only memories (ROMs) are designed to store 4096 bits of information by programming one mask pattern. The word and bit organization of these ROM series is either 512W X 8B or 1024W X 4B.

The MK 2500/2600 P series has push-pull outputs that can be in one of three states: logic one, logic zero, or open or unselected state. This, plus the programmable Chip Selects, enables the use of several ROMS in parallel with no external components. Since the ROM is a static device, no clocks are required, making the MK 2500/2600 P series of ROMS very versatile and easy to use.

Low threshold-voltage processing, utilizing ion-implantation, is used with P-channel, enhancement-mode MOS technology to provide direct input/output interfacing with TTL and DTL logic families. All inputs are protected to prevent damage from static charge accumulation.

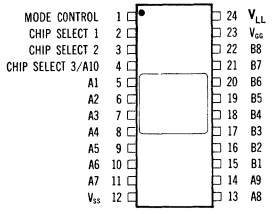
FUNCTIONAL DIAGRAMS



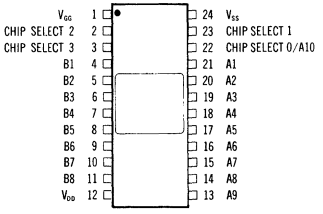
MK 2500P

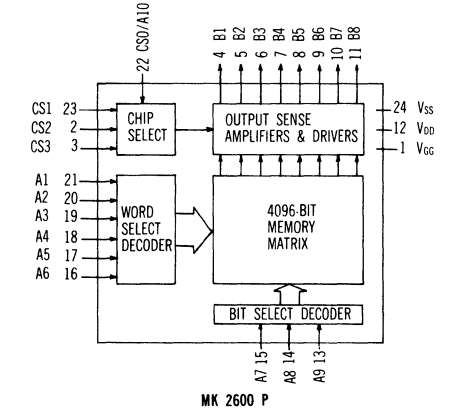
PIN CONNECTIONS

MK 2500 P



MK 2600 P





MK 2600 P

ABSOLUTE MAXIMUM RATINGS

Voltage on Any Terminal Relative to V_{SS} (except V_{GG}) ..... +0.3V to −10V
Voltage on V_{GG} Terminal Relative to V_{SS} ..... +0.3V to −20V
Operating Temperature Range (Ambient) ..... 0°C to +70°C
Storage Temperature Range (Ambient) ..... −65°C to +150°C

RECOMMENDED OPERATING CONDITIONS

($0°C \leq T_A \leq 70°C$)

	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{SS}	Supply Voltage	+4.75	+5.0	+5.25	V	
V_{DD}	Supply Voltage	——	0.0	——	V	Note 1
V_{GG}	Supply Voltage	−11.4	−12.0	−12.6	V	
V_{IL}	Input Voltage, Logic "0"			+0.8	V	
V_{IH}	Input Voltage, Logic "1"	V_{SS}−1.5			V	Note 2
V_{IH}	Input Voltage, Logic "1"	2.4			V	Note 3

ELECTRICAL CHARACTERISTICS

($V_{SS} = +5.0V \pm 5\%$; $V_{DD} = 0$ V; $V_{GG} = -12V \pm 5\%$; $0°C \leq T_A \leq 70°C$ unless noted otherwise)

	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
I_{SS}	Supply Current, V_{SS}		19.0	28.0	mA	Note 4
I_{GG}	Supply Current, V_{GG}		19.0	28.0	mA	Note 4
$I_{I(L)}$	Input Leakage Current, Any Input			10.0	μA	$V_I = V_{SS}-6.0V$. Note 2
I_{IL}	Input Current, Logic 0, Any Input			−100.0	μA	V_I=.4V. Note 3
I_{IH}	Input Current, Logic 1, Any Input			−600.0	μA	V_I=2.4V. Note 3
V_{OL}	Output Voltage, Logic "0"			0.4	V	I_{OL}=1.6mA
V_{OH}	Output Voltage, Logic "1"	2.4			V	I_{OH}=−40μA
$I_{O(L)}$	Output Leakage Current			+10	μA	Outputs disabled ($V_O = V_{SS}-6V$)
C_{IN}	Input Capacitance			10	pF	Note 5
C_O	Output Capacitance			10	pF	Note 5
t_{ACCESS}	Address to Output Access Time	100	400	700	nsec	Refer to
t_{CS}	Chip Select to Output Delay	100	250	500	nsec	Test
t_{CD}	Chip Deselect to Output Delay	100	250	800	nsec	Note 6 Circuit

Notes: 1. This is V_{LL} on MK2500P.

2. This parameter is for inputs without active pull-ups (programmable).

3. This parameter is for inputs with active pull-ups (programmable) for TTL interfaces. As the TTL driver goes to a logic 1 it must only provide 2.4V (this voltage must not be clamped) and the circuit pulls the input to V_{SS}. Refer to the Input pull-up figure for a graphical description of the active pull-up's operation.

4. Inputs at V_{SS}, outputs unloaded.

5. $V_{Bias} - V_{SS} = 0V$; $f = 1$ MHz.

6. t_{CD} is primarily dependent on the RC time constant of the load (i.e. the outputs become open circuited upon being disabled). As noted in the Timing Diagram, disabling or enabling an output with a "1" expected out does not yield a transition through the 1.5V point; this is true because the TTL equivalent load pulls the open-circuited output to approximately 2 volts.

PROGRAMMING OPTIONS

MK 2500 P

	OPTIONS	
Function	512 X 8	1024 X 4
Mode Control	1	0
Chip Select 1	1 or 0	1 or 0
Chip Select 2	1 or 0	1 or 0
Chip Select 3/A10	1 or 0	address A10

1 = Most Positive = High Level Voltage

Pin 1 in the MK 2500 P is used as a Mode Control, setting the circuit in the 1024x4 or 512x8 mode. In the 1024x4 mode a tenth address bit is required, which is provided at Pin 4. If the circuit is in the 512x8 mode, then Pin 4 may be used for a third chip select.

Additional Options: The MK 2500 P can have the address and control inputs set by the user so that:

512x8: Mode Control — High
A10 — Low

1024x4: Mode Control — Low
A10 aid as an address
See Note 9, following page

MK 2600 P

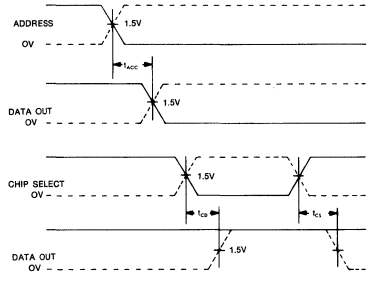
	OPTIONS	
Function	512 X 8	1024 X 4
Chip Select 0/A10	1 or 0	A10
Chip Select 1	1 or 0	1 or 0
Chip Select 2	1 or 0	1 or 0
Chip Select 3	1 or 0	1 or 0

1 = Most Positive = High Level Voltage

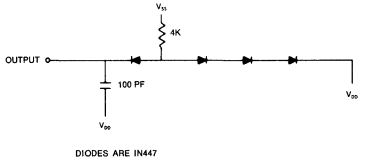
The MK 2600 P is programmed either as a 512x8 array or a 1024x4 array. In the 1024x4 arrays, Pin 22 provides the tenth address bit. When A10 is low the four bits are present at the even outputs (B2, B4, B6, and B8); when A10 is high, the bits are at the odd outputs (B1, B3, B5, and B7).

In 512x8 arrays, Pin 22 may be used to provide a fourth chip select. Thus, with four programmable chip selects, sixteen MK 2600 P ROMS in the 512x8 configuration can be arranged in an 8192x8 array requiring no external decoding.

TIMING

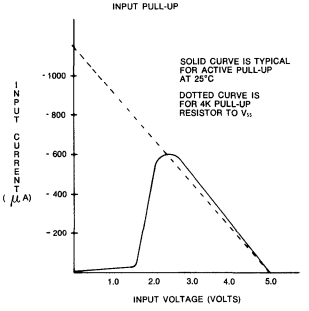


T_{ACCESS} TEST CIRCUIT



DIODES ARE IN447

INPUT



MOSTEK ROM PUNCHED-CARD CODING FORMAT[1]

MK 2500 P

First Card

Cols.	Information Field
1-30	Customer
31-50	Customer Part Number
60-72	Mostek Part Number[2]

Second Card

1-30	Engineer at Customer Site
31-50	Direct Phone Number for Engineer

Third Card

1-5	Mostek Part Number[2]
10-16	Organization[3]
29	CS3[10]
30	CS2[4]
31	CS1[4]
32	Active Pull-ups[5]

Fourth Card

1-9	Data Format[6]
15-28	Logic — "Positive Logic" or "Negative Logic"
35-57	Verification Code[7]
60-67	"A10 EVEN" or "A10 ODD" (left justified)[9]

Data Cards/512x08 Organization

1-4	Decimal Address
6-13	Output B8- B1 (MSB thru LSB)
15-17	Octal Equivalent of output data[8]

Data Cards/1024x04 Organization

1-4	Decimal Address (0-1022), even addresses
6-9	Output (MSB-LSB)
11-12	Octal Equivalent of output data[8]
50-53	Decimal Address (1-1023), odd addresses
55-58	Output (MSB-LSB)
60-61	Octal Equivalent of output data[8]

MK 2600 P

First Card

Cols.	Information Field
1-30	Customer
31-50	Customer Part Number
60-72	Mostek Part Number[2]

Second Card

1-30	Engineer at Customer Site
31-50	Direct Phone Number for Engineer

Third Card

1-5	Mostek Part Number[2]
10-16	Organization[3]
29	CS3[4]
30	CS2[4]
31	CS1[4]
32	CS0[10]
33	Active Pull-ups[5]

Fourth Card

1-9	Data Format[6]
15-28	Logic — "Positive Logic" or "Negative Logic"
35-57	Verification Code[7]

Data Cards/512x08 Organization

1-4	Decimal Address
6-13	Output B8- B1 (MSB thru LSB)
15-17	Octal Equivalent of output data[8]

Data Cards/1024x04 Organization

1-4	Decimal Address (0-1022), even addresses
6-9	Output (MSB-LSB)
11-12	Octal Equivalent of output data[8]
50-53	Decimal Address (1-1023), odd addresses
55-58	Output (MSB-LSB)
60-61	Octal Equivalent of output data[8]

Notes: 1. Positive or negative logic formats are accepted as noted in the fourtn card.

2. Assigned by Mostek Marketing Department; may be left blank.

3. Punched as "0512x08" or "1024x04".

4. A "0" indicates the chip is enabled by a logic 0, a "1" indicates it is enabled by a logic 1, and a "2" indicates a "Don't Care" condition.

5. A "1" indicates active pull-ups; a "0" indicates no pull-ups.

6. MOSTEK, Fairchild, or National Punched-Card Coding Format may be used. Specify which punched card format used by punching either "MOSTEK", "Fairchild", or "National". Start name at column one.

7. Punched as: (a) VERIFICATION HOLD — i.e. customer verification of the data as reproduced by MOSTEK is required prior to production of the ROM. To accomplish this MOSTEK supplies a copy of its Customer Verification Data Sheet (CVDS) to the customer.
   (b) VERIFICATION PROCESS — i.e. the customer will receive a CVDS but production will begin prior to receipt of customer verification.
   (c) VERIFICATION NOT NEEDED — i.e. the customer will not receive a CVDS and production will begin immediately.

8. The octal parity check is created by breaking up the output word into groups of three from right to left and creating a base 8 (octal) number in place of these groups. For example the output word 10011110 would be separated into groups 10/011/110 and the resulting octal equivalent number is 236.

9. "A10 EVEN" and "A10 ODD" applies to the 1024 x 4 mode. "A10 EVEN" means the even outputs are enabled when A10 is high. "A10 ODD" means the odd outputs are enabled when A10 is high.

10. Punched as "2" for 1024 x 4 organization.

ASCII-TO-EBCDIC CODE CONVERTER
EBCDIC-TO-ASCII CODE CONVERTER

A_1 = LSB B_1 = LSB
A_9 = MSB B_8 = MSB

MK 2503 P

Function	512 X 8
Mode Control	1
Chip Select 1	0
Chip Select 2	0
Chip Select 3/A10	0

MK 2601 P

Function	512 X 8
Chip Select 0/A10	0
Chip Select 1	0
Chip Select 2	0
Chip Select 3	0

ASCII (ADDRESS) TO EBCDIC (DATA)

0 00000000	1 00000001	2 00000010	3 00000011	128 00100000	129 00100001	130 00100010	131 00100011
4 00110111	5 00101101	6 00101110	7 00101111	132 00100100	133 00010101	134 00000110	135 00010111
8 00010110	9 00000101	10 00100101	11 00001011	136 00101000	137 00101001	138 00101010	139 00101011
12 00001100	13 00001101	14 00001110	15 00001111	140 00101100	141 00001001	142 00001010	143 00011011
16 00010000	17 00010001	18 00010010	19 00010011	144 00110000	145 00110001	146 00011010	147 00110011
20 00111100	21 00111101	22 00110010	23 00100110	148 00110100	149 00110101	150 00110110	151 00001000
24 00011000	25 00011001	26 00111111	27 00100111	152 00111000	153 00111001	154 00111010	155 00111011
28 00011100	29 00011101	30 00011110	31 00011111	156 00000100	157 00010100	158 00111110	159 11100001
32 01000000	33 01001111	34 01111111	35 01111011	160 01000001	161 01000010	162 01000011	163 01000100
36 01011011	37 01101100	38 01010000	39 01111101	164 01000101	165 01000110	166 01000111	167 01001000
40 01001101	41 01011101	42 01011100	43 01001110	168 01001001	169 01010001	170 01010010	171 01010011
44 01101011	45 01100000	46 01001011	47 01100001	172 01010100	173 01010101	174 01010110	175 01010111
48 11110000	49 11110001	50 11110010	51 11110011	176 01011000	177 01011001	178 01100010	179 01100011
52 11110100	53 11110101	54 11110110	55 11110111	180 01100100	181 01100101	182 01100110	183 01100111
56 11111000	57 11111001	58 01111010	59 01011110	184 01101000	185 01101001	186 01110000	187 01110001
60 01001100	61 01111110	62 01101110	63 01101111	188 01110010	189 01110011	190 01110100	191 01110101
64 01111100	65 11000001	66 11000010	67 11000011	192 01110110	193 01110111	194 01111000	195 10000000
68 11000100	69 11000101	70 11000110	71 11000111	196 10001010	197 10001011	198 10001100	199 10001101
72 11001000	73 11001001	74 11010001	75 11010010	200 10001110	201 10001111	202 10010000	203 10011010
76 11010011	77 11010100	78 11010101	79 11010110	204 10011011	205 10011100	206 10011101	207 10011110
80 11010111	81 11011000	82 11011001	83 11100000	208 10011111	209 10100000	210 10101010	211 10101011
84 11100011	85 11100100	86 11100101	87 11100110	212 10101100	213 10101101	214 10101110	215 10101111
88 11100111	89 11101000	90 11101001	91 01001010	216 10110000	217 10110001	218 10110010	219 10110011
92 11100000	93 01011010	94 01011111	95 01101101	220 10110100	221 10110101	222 10110110	223 10110111
96 01111001	97 10000001	98 10000010	99 10000011	224 10111000	225 10111001	226 10111010	227 10111011
100 10000100	101 10000101	102 10000110	103 10000111	228 10111100	229 10111101	230 10111110	231 10111111
104 10001000	105 10001001	106 10010001	107 10010010	232 11001010	233 11001011	234 11001100	235 11001101
108 10010011	109 10010100	110 10010101	111 10010110	236 11001110	237 11001111	238 11011010	239 11011011
112 10010111	113 10011000	114 10011001	115 10100010	240 11011100	241 11011101	242 11011110	243 11011111
116 10100011	117 10100100	118 10100101	119 10100110	244 11101010	245 11101011	246 11101100	247 11101101
120 10100111	121 10101000	122 10101001	123 11000000	248 11101110	249 11101111	250 11111010	251 11111011
124 01101010	125 11010000	126 10100001	127 00000111	252 11111100	253 11111101	254 11111110	255 11111111

EBCDIC (ADDRESS) TO ASCII (DATA)

256 00000000	257 00000001	258 00000010	259 00000011	384 11000011	385 01100001	386 01100010	387 01100011
260 10011100	261 00001001	262 10000110	263 01111111	388 01100100	389 01100101	390 01100110	391 01100111
264 10010111	265 10001101	266 10001110	267 00001011	392 01101000	393 01101001	394 11000100	395 11000101
268 00001100	269 00001101	270 00001110	271 00001111	396 11000110	397 11000111	398 11001000	399 11001001
272 00010000	273 00010001	274 00010010	275 00010011	400 11001010	401 01101010	402 01101011	403 01101100
276 10011101	277 10000101	278 00001000	279 10000111	404 01101101	405 01101110	406 01101111	407 01110000
280 00011000	281 00011001	282 10010010	283 10001111	408 01110001	409 01110010	410 11001011	411 11001100
284 00011100	285 00011101	286 00011110	287 00011111	412 11001101	413 11001110	414 11001111	415 11010000
288 10000000	289 10000001	290 10000010	291 10000011	416 11010001	417 01111110	418 01110011	419 01110100
292 10000100	293 00001010	294 00010111	295 00011011	420 01110101	421 01110110	422 01110111	423 01111000
296 10001000	297 10001001	298 10001010	299 10001011	424 01111001	425 01111010	426 11010010	427 11010011
300 10001100	301 00000101	302 00000110	303 00000111	428 11010100	429 11010101	430 11010110	431 11010111
304 10010000	305 10010001	306 00010110	307 10010011	432 11011000	433 11011001	434 11011010	435 11011011
308 10010100	309 10010101	310 10010110	311 00000100	436 11011100	437 11011101	438 11011110	439 11011111
312 10011000	313 10011001	314 10011010	315 10011011	440 11100000	441 11100001	442 11100010	443 11100011
316 00010100	317 00010101	318 10011110	319 00011010	444 11100100	445 11100101	446 11100110	447 11100111
320 00100000	321 10100000	322 10100001	323 10100010	448 01111011	449 01000001	450 01000010	451 01000011
324 10100011	325 10100100	326 10100101	327 10100110	452 01000100	453 01000101	454 01000110	455 01000111
328 10100111	329 10101000	330 01011011	331 00101110	456 01001000	457 01001001	458 11101000	459 11101001
332 00111100	333 00101000	334 00101011	335 00100001	460 11101010	461 11101011	462 11101100	463 11101101
336 00100110	337 10101001	338 10101010	339 10101011	464 01111101	465 01001010	466 01001011	467 01001100
340 10101100	341 10101101	342 10101110	343 10101111	468 01001101	469 01001110	470 01001111	471 01010000
344 10110000	345 10110001	346 01011101	347 00100100	472 01010001	473 01010010	474 11101110	475 11101111
348 00101010	349 00101001	350 00111011	351 01011110	476 11110000	477 11110001	478 11110010	479 11110011
352 00101101	353 00101111	354 10110010	355 10110011	480 01011100	481 10011111	482 01010011	483 01010100
356 10110100	357 10110101	358 10110110	359 10110111	484 01010101	485 01010110	486 01010111	487 01011000
360 10111000	361 10111001	362 01111100	363 00101100	488 01011001	489 01011010	490 11110100	491 11110101
364 00100101	365 01011111	366 00111110	367 00111111	492 11110110	493 11110111	494 11111000	495 11111001
368 10111010	369 10111011	370 10111100	371 10111101	496 00110000	497 00110001	498 00110010	499 00110011
372 10111110	373 10111111	374 11000000	375 11000001	500 00110100	501 00110101	502 00110110	503 00110111
376 11000010	377 01100000	378 00111010	379 00100011	504 00111000	505 00111001	506 11111010	507 11111011
380 01000000	381 00100111	382 00111101	383 00100010	508 11111100	509 11111101	510 11111110	511 11111111

MOSTEK

8K-BIT MOS READ ONLY MEMORY

MK30000P/N

FEATURES

- ☐ High performance replacement for Intel 2308/8308, and TI 4700
- ☐ 350ns max access time
- ☐ Single +5V ±10% power supply
- ☐ Contact programmed for fast turn-around
- ☐ Two programmable chip selects
- ☐ Inputs and three-state outputs TTL compatible
- ☐ Eight bit output for use with microprocessor systems
- ☐ Pin compatible with MK 2708 EPROM

DESCRIPTION

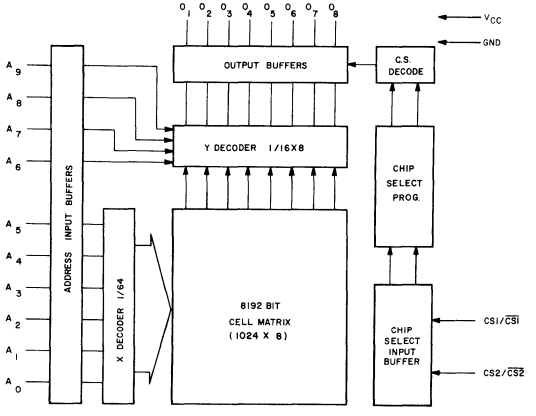
The MK 30000 is a 8,192 bit Read Only Memory designed as a high performance replacement for the Intel 2308/8308 and the TI 4700. The MK 30000 is organized as a 1K x 8 array which makes the device very attractive for use with 8-bit microprocessors such as the F8, 8080, 6800, Z-80 or any memory application requiring a high performance, high bit density ROM.

The device uses a single +5V (± 10% tolerance) power supply. The two chip select inputs can be programmed for any desired combination of active high's or low's. These programmable chip select inputs coupled with the three-state TTL compatible outputs provide a high performance memory circuit with extremely simple interface requirements.

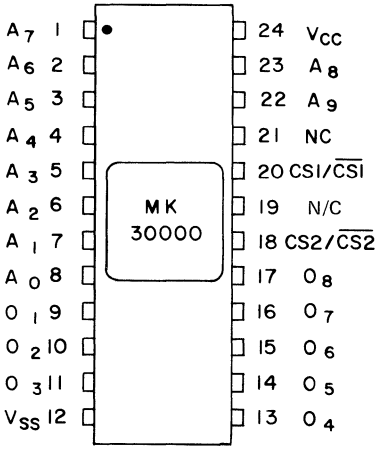
An outstanding feature of the MK 30000 is the use of contact programming instead of gate mask programming. Since the contact mask is applied at a later processing stage, wafers can be partially processed and stored. When an order is received, a contact mask, which represents the desired bit pattern, is generated and applied to the wafers. Only a few processing steps are left to complete the part. Therefore, the use of contact programming reduces the turnaround time for a custom ROM.

The MK 30000 is fabricated with N-channel silicon gate MOS technology for optimum size and circuit performance. Ion-implantation is utilized to allow full TTL compatibility at the inputs and outputs. All inputs are protected against static charge.

FUNCTIONAL DIAGRAM



PIN CONNECTIONS



ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Terminal Relative to Ground . . . . . −0.5V to + 7V
Operating Temperature T_A (Ambient) . . . . . 0°C to + 70°C
Storage Temperature — Ceramic (Ambient) . . . . . −65°C to + 150°C
Storage Temperature — Plastic (Ambient) . . . . . −55°C to +125°C
Power Dissipation . . . . . 1 Watt

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS

(V_{CC} = 5V ± 10%; 0°C ≤ T_A ≤ + 70°C)

PARAMETER		MIN	TYP	MAX	UNITS	NOTES
V_{CC}	Power Supply Voltage	4.5	5.0	5.5	Volts	6
V_{IL}	Input Logic 0 Voltage	−0.5		0.8	Volts	
V_{IH}	Input Logic 1 Voltage	2.0		V_{CC}	Volts	

D C ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ± 10%; 0°C ≤ T_A ≤ + 70°C)[6]

PARAMETER		MIN	MAX	UNITS	NOTES
I_{CC}	V_{CC} Power Supply Current		60	mA	1
$I_{I(L)}$	Input Leakage Current		10	μA	2
$I_{O(L)}$	Output Leakage Current		10	μA	3
V_{OL}	Output Logic 0 Voltage @ I_{OUT} = 3.3mA		0.4	volts	
V_{OH}	Output Logic 1 Voltage @ I_{OUT} = −220 μA	2.4	V_{CC}	volts	

A C ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ± 10%; 0°C ≤ T_A ≤ + 70°C)[6]

PARAMETER		MIN	MAX	UNITS	NOTES
t_{ACC}	Address to output delay time		350	ns	4
t_{CS}	Chip select to output delay time		175	ns	4
t_{CD}	Chip deselect to output delay time		150	ns	4

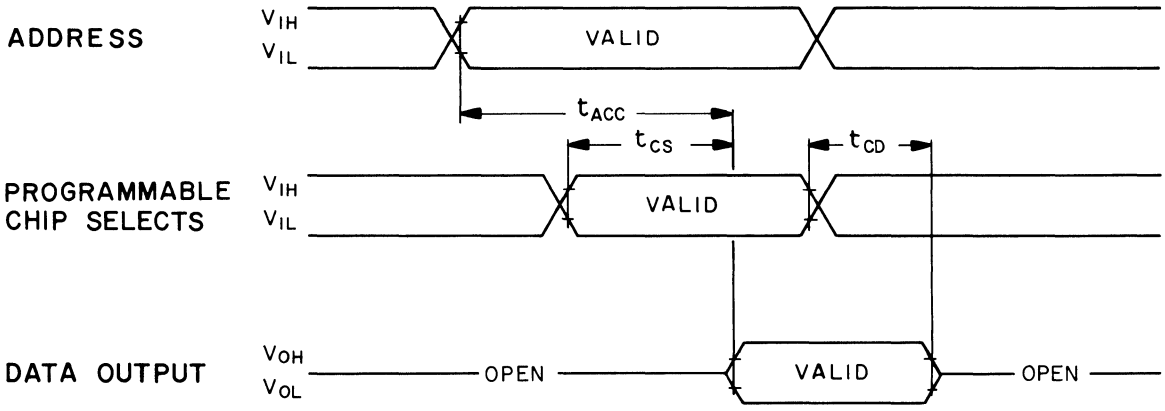
CAPACITANCE

PARAMETER		TYP	MAX	UNITS	NOTES
C_{IN}	Input Capacitance	6	8	pF	5
C_{OUT}	Output Capacitance	10	15	pF	5

NOTES:

1. All inputs 5.5V; Data Outputs open.
2. V_{IN} = 0V to 5.5V
3. Device unselected; V_{OUT} = 0V to 5.5V.
4. Measured with 2 TTL loads and 100pF, transition times = 20ns
5. Capacitance measured with Boonton Meter or effective capacitance calculated from the equation : $C = \frac{I \Delta t}{\Delta V}$ with current equal to a constant 20mA.
6. A minimum 100 μs time delay is required after the application of V_{CC} (+5) before proper device operation is achieved.

TIMING DIAGRAM



MOSTEK 30000 ROM PUNCHED CARD CODING FORMAT (1)

FIRST CARD

COLS	INFORMATION FIELD
1-30	Customer
31-50	Customer Part Number
60-72	MOSTEK Part Number (2)

SECOND CARD

1-30	Engineer at Customer Site
31-50	Direct Phone Number for Engineer

THIRD CARD

1-5	MOSTEK Part Number (2)
33	Chip Select One "1" = CS_1 or "0" = $\overline{CS}_1$
35	Chip Select Two "1" = CS_2 or "0" = $\overline{CS}_2$

FOURTH CARD

1-9	Data Format (3)
15-28	Logic - ("Positive Logic" or "Negative Logic")
35-57	Verification Code (4)

DATA FORMAT (3)

MOSTEK OR INTEL

MOSTEK FORMAT
64 data cards (16 data words/card) with the following format:

COLS	INFORMATION FIELD
1-4	Four digit octal address of first output word on card
5-7	Three digit octal output word specified by address in column 1-4
8-52	Next fifteen output words, each word consists of three octal digits.

NOTES:

1. Positive or negative logic formats are accepted as noted in the fourth card.
2. Assigned by MOSTEK; may be left blank.
3. MOSTEK or Intel Punched card coding format may be used. Specify which card format used by punching either "MOSTEK" or "Intel". Start at column one.
4. Punches as: (a) VERIFICATION HOLD - i.e. customer verification of the data as reproduced by MOSTEK is required prior to production of the ROM. To accomplish this MOSTEK supplies a copy of its Customer Verification Data Sheet (CVDS) to the customer.

   (b) VERIFICATION PROCESS - i.e. the customer will receive a CVDS but production will begin prior to receipt of customer verification; (c) VERIFICATION NOT NEEDED - i.e. the customer will not receive a CVDS and production will begin immediately.

16K ROMS

MOSTEK's new series of 16K Read Only Memories now gives the user several options on speed, operating performance and pin-out configurations. The MK 34000 is the fastest and lowest power 16K ROM available today with the added advantage of being pin-compatible with the new generation EPROM's. The MK 31000 is a high performance replacement for the 8316A type ROM and the MK 34000 is a high performance replacement for the 8316E/6831B type ROMs.

MOSTEK

16,384x1-BIT DYNAMIC ROM

MK 28000 P/N

FEATURES

- ☐ 600 ns Maximum Access Time
- ☐ Low Power Dissipation
  Active – 0.02 mW/bit Typ.
  Inactive – .007 mW/bit Typ.
- ☐ EA 4900 and EA 4800 Pin-for-pin Replacement
- ☐ 2K x 8 or 4K x 4 organization with Open Drain Outputs
- ☐ Standard Supplies +5 volts, – 12 volts
- ☐ Ion-Implanted for Full TTL/DTL Compatibility

DESCRIPTION

The MK 28000 is a mask programmable read only memory utilizing low-threshold Ion-Implant, P-Channel technology. The MK 28000 is a pin-for-pin replacement for the EA 4900. The MK 28000 may be organized as either a 2K x 8 or 4K x 4 memory.

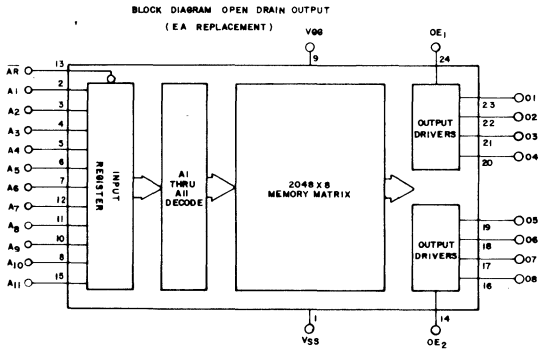
The MK 28000 open drain outputs are divided into two groups with one Output Enable line controlling each group of outputs. This feature allows the MK 28000 to be either a 2K x 8 or a 4K x 4 memory without any internal mask changes. For a 2K x 8 organization, the Output Enables (OE_1, OE_2) are tied together. For a 4K x 4 organization, the four outputs associated with OE_1 are wire-ORed to the four outputs associated with OE_2. OE_1 and OE_2 are inverted with respect to each other and used as the twelfth address input in the 4K x 4 organization.

The internal circuitry of the MK 28000 is dynamic. This features means low standby power consumption when the ROM is not being addressed.

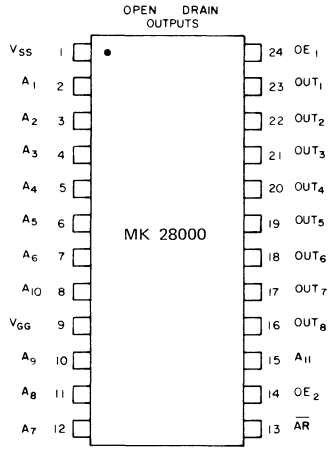
All inputs are protected against static charge accumulation. Pullup resistors on all inputs are available as a programmable option.

With no address lead time required, system design is simplified; address and $\overline{AR}$ may appear simultaneously.

FUNCTIONAL DIAGRAM



PIN CONNECTIONS



ABSOLUTE MAXIMUM RATINGS

Voltage on any terminal relative to V_{SS} ..... +0.3V to −20V
Operating temperature range (Ambient) ..... 0°C to 70°C
Storage temperature range (Ambient) Ceramic ..... −65°C to +150°C
Storage temperature range (Ambient) Plastic ..... −55°C to +125°C

	PARAMETER	MIN	TYP	MAX	COMMENTS
V_{SS}	Supply Voltage	+4.75V	+5V	+5.25V	
	TTL Reference	—	0	—	
V_{GG}	Supply Voltage	−12.6V	−12V	−11.4V	
V_{IL}	Input Voltage, Logic "0"	V_{GG}		+.8V	
V_{IH}	Input Voltage, Logic "1"	V_{SS} − 1.5V		V_{SS}	Pullup resistors to V_{SS} (≈5K) available as an option

ELECTRICAL CHARACTERISTICS

(V_{SS} = +5.0V ±5%; V_{DD} = 0V; V_{GG} = −12V ±5%; 0°C ≤ T_A ≤ 70°C)

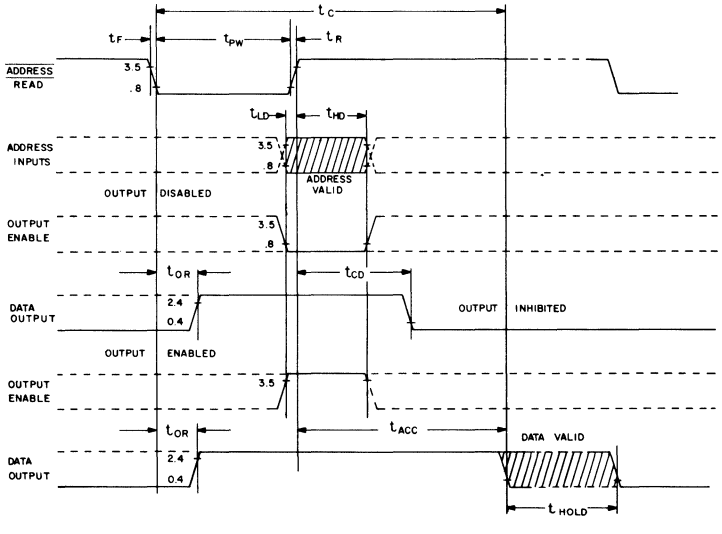
	PARAMETER	MIN	TYP	MAX	COMMENTS
I_{SS}	Supply Current		20 mA	35 mA	See Note 1
I_{GG}	Supply Current		−20 mA	−35 mA	Inputs at V_{SS}
I_{GG}	Supply Current (Standby)		7 mA	12 mA	See Note 1
C_{IN}	Input Capacitance (Address & OE's)		8 pF	10 pF	See Note 2
C_{IN}	Input Capacitance ($\overline{AR}$)		12 pF	15 pF	See Note 2
I_{IN}	Input Leakage			10 µA	See Note 3
R_{IN}	Input Pullup Resistors	3 KΩ		11 KΩ	Optional
V_{OH}	Output Voltage, Logic "1"	2.4V			See Note 4
I_{OL}	Output Leakage Current	−10 µA		+10µA	V_O = V_{SS} −6V, T_A = 25°C (outputs disabled)

	PARAMETER	MIN	TYP	MAX	COMMENTS
t_{PW}	$\overline{AR}$ Precharge Time	400 ns		∞	
t_C	Cycle Time	1 µs + t_R + t_F			t_{ACC} + t_{PW} + t_R + t_F
t_{ACC}	Access Time			600 ns	See note 4
t_{LD}	Address Lead Time	0			
t_{HD}	Address Hold Time	250 ns			
t_R	$\overline{AR}$ Rise Time			100 ns	
t_F	$\overline{AR}$ Fall Time			100 ns	
t_{HOLD}	Data Output Valid Time	2 µs			See note 5
t_{CD}	Output Disable Time			300 ns	See note 4
t_{OR}	Output Reset Time	75 ns		400 ns	See note 4

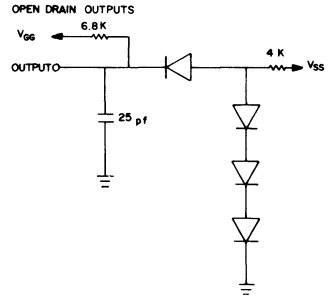
NOTES:

1. Outputs disconnected with no internal pullup resistors.
2. $V_{BIAS} - V_{SS} = 0V$; f = 1 MHz
3. This parameter is for inputs without pullups (optional)
4. With test circuit shown below
5. or, until the next precharge + T_{OR} [if AR makes a negative transition before t_{HOLD} (min) has elapsed].

TIMING



TEST CIRCUIT



MOSTEK 28000 ROM Punched Card Coding Format[1]

First Card

Cols	Information Field
1-30	Customer
31-50	Customer Part Number
60-72	MOSTEK Part Number[2]

Second Card

1-30	Engineer at Customer Site
31-50	Direct Phone Number for Engineer

Third Card

1-5	MOSTEK Part Number[2]
33	Input Pullups (0 = no, 1 = yes, 2 = Selectable Pull-up Option)[5]

Fourth Card

1-9	Data Format[3]
15-28	Logic – ("Positive Logic" or "Negative Logic")
35-57	Verification Code[4]

Data Cards

MOSTEK Format		EA Format
1-4	Decimal Address	
6-13	Output 08-01 (MSB Thru LSB)	
15-17	Octal Equivalent of Output Data	

NOTES:
1. Positive or negative logic formats are accepted as noted in the fourth card.
2. Assigned by MOSTEK; may be left blank.
3. MOSTEK or Electronic Arrays Punched card coding format may be used. Specify which card format used by punching either "MOSTEK" or "EA". Start at column one.
4. Punches as:
   (a) VERIFICATION HOLD – i.e. customer verification of the data as reproduced by MOSTEK is required prior to production of the ROM. To accomplish this MOSTEK supplies a copy of its Customer Verification Data Sheet (CVDS) to the customer.
   (b) VERIFICATION PROCESS – i.e. the customer will receive a CVDS but production will begin prior to receipt of customer verification
   (c) VERIFICATION NOT NEEDED – i.e. the customer will not receive a CVDS and production will begin immediately.
5. Columns 34-47 represent A1–A11, $\overline{AR}$, OE1, OE2 respectively. 0= No pull-up, 1 = Pull-up

MOSTEK

16 K-Bit MOS Read Only Memory

MK 31000(P/N)-3

FEATURES

- ☐ High performance replacement for Intel 2316A/ 8316A and General Instrument RO-3-8316A
- ☐ Maximum access time 550ns
- ☐ Single +5V ±10% power supply
- ☐ Contact programmed for fast turn-around
- ☐ Three programmable chip selects
- ☐ Inputs and three-state outputs TTL compatible
- ☐ Outputs drive 2 TTL loads and 100pF
- ☐ Low power
- ☐ Eight bit output for use with microprocessor systems

DESCRIPTION

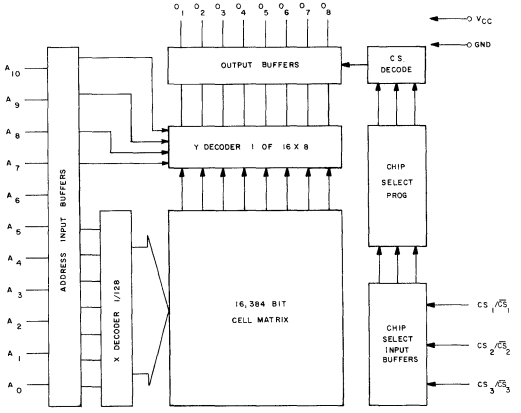
The MK 31000 is a 16,384 bit Read Only Memory designed as a high performance replacement for the Intel 2316A/8316A and the General Instrument RO-3-8316A. The MK 31000 is organized as a 2K x 8 array which makes the device very attractive for use with 8 bit microprocessors such as the F8, 8080, 6800, Z-80 or any memory application requiring a high performance, high bit density ROM.

The device uses a single +5 volt (± 10% tolerance) power supply. The three chip select inputs can be programmed for any desired combination of active high's or low's. These programmable chip select inputs coupled with the three-state TTL compatible outputs provide a high performance memory circuit with extremely simple interface requirements.

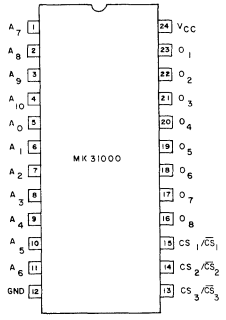
An outstanding feature of the MK 31000 is the use of contact programming instead of gate mask programming. Since the contact mask is applied at a later processing stage, wafers can be partially processed and stored. When an order is received, a contact mask, which represents the desired bit pattern, is generated and applied to the wafers. Only a few processing steps are left to complete the part. Therefore, the use of contact programming reduces the turnaround time for a custom ROM.

The MK 31000 is fabricated with N-channel silicon gate MOS technology for optimum size and circuit performance. Ion-implantation is utilized to allow full TTL compatibility at the inputs and outputs. All inputs are protected against static charge.

FUNCTIONAL DIAGRAM



PIN CONNECTIONS



ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Terminal Relative to Ground. . . . . −0.5V to +7V
Operating Temperature T_A (Ambient). . . . . 0°C to +70°C
Storage Temperature (Ambient) Ceramic . . . . . −65°C to +150°C
Storage Temperature (Ambient) Plastic. . . . . −55°C to +125°C
Power Dissipation 1W

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED D C OPERATING CONDITIONS
(V_{CC} = 5V ± 10%; 0°C ≤ T_A ≤ + 70 C)

	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{CC}	Power Supply Voltage	4.5	5.0	5.5	Volts	
V_{IL}	Input Logic 0 Voltage	−0.5		0.8	Volts	
V_{IH}	Input Logic 1 Voltage	2.0		V_{CC}	Volts	

D C ELECTRICAL CHARACTERISTICS
(V_{CC} = 5V ± 10%; 0°C ≤ T_A ≤ + 70°C)

	PARAMETER	MIN	MAX	UNITS	NOTES
I_{CC}	V_{CC} Power Supply Current		60	mA	1
$I_{I(L)}$	Input Leakage Current		10	μA	2
$I_{O(L)}$	Output Leakage Current		10	μA	3
V_{OL}	Output Logic 0 Voltage @ I_{OUT} = 3.3mA		0.4	volts	
V_{OH}	Output Logic 1 Voltage @ I_{OUT} = −220 μA	2.2	V_{CC}	volts	

A C ELECTRICAL CHARACTERISTICS
(V_{CC} = 5V ± 10%; 0°C ≤ T_A ≤ + 70°C)

	PARAMETER	MIN	MAX	UNITS	NOTES
t_{ACC}	Address to output delay time		550	ns	4
t_{CS}	Chip select to output delay time		250	ns	4
t_{CD}	Chip deselect to output delay time		150	ns	4

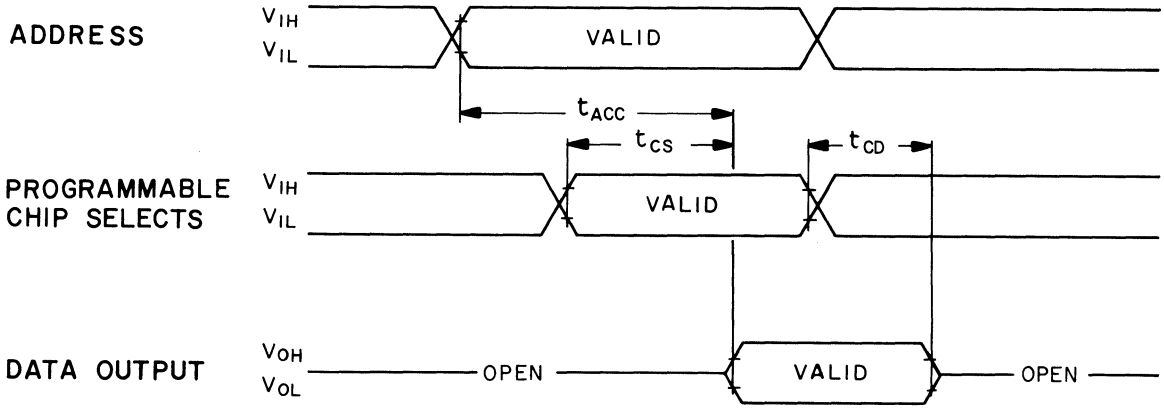
CAPACITANCE

	PARAMETER	TYP	MAX	UNITS	NOTES	
C_{IN}	Input Capacitance	6	8	pf	5	
C_{OUT}	Output Capacitance	10	15	pf	5	

NOTES:

1. All inputs 5.5V ; Data Outputs open.
2. V_{in} = 0V to 5.5V.
3. Device unselected; V_{out} = 0V to 5.5V
4. Measured with 2 TTL loads and 100pf.
5. Capacitance measured with Boonton Meter or effective capacitance calculated from the equation $C = \frac{I \Delta t}{\Delta V}$ with current equal to a constant 20mA.

TIMING DIAGRAM



MOSTEK 31000 ROM PUNCHED CARD CODING FORMAT (1)

FIRST CARD

COLS	INFORMATION FIELD
1-30	Customer
31-50	Customer Part Number
60-72	MOSTEK Part Number (2)

SECOND CARD

1-30	Engineer at Customer Site
31-50	Direct Phone Number for Engineer

THIRD CARD

1-5	MOSTEK Part Number (2)
33	Chip Select One "1" = CS_1 or "0" = $\overline{CS}_1$
35	Chip Select Two "1" = CS_2 or "0" = $\overline{CS}_2$
37	Chip Select Three "1" = CS_3 or "0" = $\overline{CS}_3$

FOURTH CARD

1-9	Data Format (3)
15-28	Logic - ("Positive Logic" or "Negative Logic")
35-57	Verification Code (4)

DATA FORMAT

MOSTEK OR INTEL

MOSTEK FORMAT
128 data cards (16 data words/card) with the following format:

COLS	INFORMATION FIELD
1-4	Four digit octal address of first output word on card
5-7	Three digit octal output word specified by address in column 1-4
8-52	Next fifteen output words, each word consists of three octal digits.

NOTES:

1. Positive or negative logic formats are accepted as noted in the fourth card.
2. Assigned by MOSTEK; may be left blank.
3. MOSTEK or Intel Punched card coding format may be used. Specify which card format used by punching either "MOSTEK" or "Intel". Start at column one.
4. Punches as: (a) VERIFICATION HOLD - i.e. customer verification of the data as reproduced by MOSTEK is required prior to production of the ROM. To accomplish this MOSTEK supplies a copy of its Customer Verification Data Sheet (CVDS) to the customer.

   (b) VERIFICATION PROCESS - i.e. the customer will receive a CVDS but production will begin prior to receipt of customer verification; (c) VERIFICATION NOT NEEDED - i.e. the customer will not receive a CVDS and production will begin immediately.

MOSTEK

16K-BIT MOS READ ONLY MEMORY

MK 34000P/N-3

FEATURES

- ☐ 2K x 8 organization with static interface
- ☐ 350ns max access time
- ☐ Single +5V ± 10% power supply
- ☐ 330mW max power dissipation
- ☐ Contact programmed for fast turn-around
- ☐ Three programmable chip selects
- ☐ Inputs and three-state outputs—TTL compatible
- ☐ Outputs drive 2 TTL loads and 100pF

DESCRIPTION

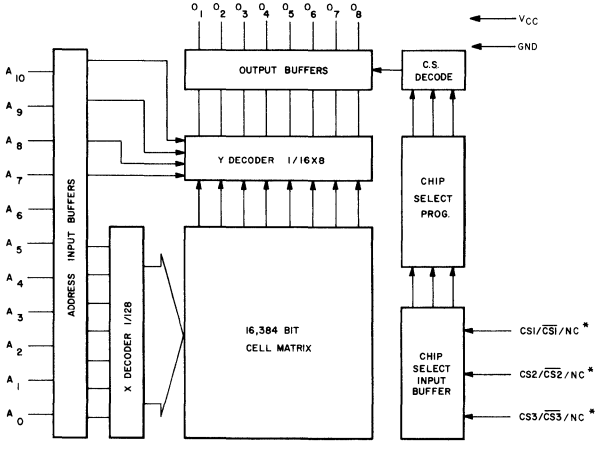
The MK 34000 is a new generation N-channel silicon gate MOS Read Only Memory circuit organized as 2048 words by 8 bits. As a state-of-the-art device, the MK 34000 incorporates advanced circuit techniques designed to provide maximum circuit density and reliability with highest possible performance, while maintaining low power dissipation and wide operating margins.

The MK 34000 requires a single +5 volt (± 10% tolerance) power supply and has complete TTL compatibility at all inputs and outputs (a feature made possible by MOSTEK's Ion-implantation technique). The three chip select inputs can be programmed for any desired combination of active high's or low's or even an optional "DON'T CARE" state. The convenient static operation of the MK 34000 coupled with the programmable chip select inputs and three-state TTL compatible outputs results in extremely simple interface requirements.

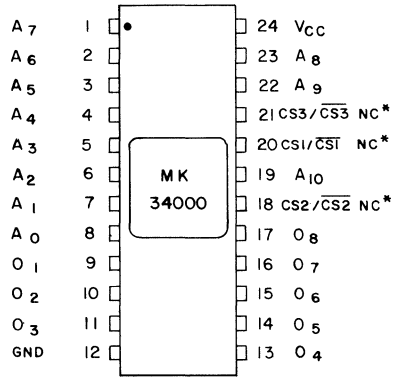
An outstanding feature of the MK 34000 is the use of contact programming over gate mask programming. Since the contact mask is applied at a later processing stage, wafers can be partially processed and stored. When an order is received, a contact mask, which represents the desired bit pattern, is generated and applied to the wafers. Only a few processing steps are left to complete the part. Therefore, the use of contact programming reduces the turnaround time for a custom ROM.

Any application requiring a high performance, high bit density ROM can be satisfied by this device. The MK 34000 is ideally suited for 8-bit microprocessor systems such as those which utilize the Z80 or F8. The MK 34000 also provides significant cost advantages over PROM.

FUNCTIONAL DIAGRAM



PIN CONNECTIONS



*Programmable Chip Selects

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Terminal Relative to Ground . . . . . −0.5V to + 7V
Operating Temperature T_A (Ambient) . . . . . 0°C to + 70°C
Storage Temperature — Ceramic (Ambient) . . . . . −65°C to + 150°C
Storage Temperature — Plastic (Ambient) . . . . . −55°C to +125°C
Power Dissipation . . . . . 1 Watt

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS

(V_{CC} = 5V ± 10%; 0°C ≤ T_A ≤ + 70°C)

	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{CC}	Power Supply Voltage	4.5	5.0	5.5	Volts	6
V_{IL}	Input Logic 0 Voltage	−0.5		0.8	Volts	
V_{IH}	Input Logic 1 Voltage	2.0		V_{CC}	Volts	

D C ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ± 10%; 0°C ≤ T_A ≤ + 70°C)[6]

	PARAMETER	MIN	MAX	UNITS	NOTES
I_{CC}	V_{CC} Power Supply Current		60	mA	1
$I_{I(L)}$	Input Leakage Current		10	μA	2
$I_{O(L)}$	Output Leakage Current		10	μA	3
V_{OL}	Output Logic 0 Voltage @ I_{OUT} = 3.3mA		0.4	volts	
V_{OH}	Output Logic 1 Voltage @ I_{OUT} = −220 μA	2.4	V_{CC}	volts	

A C ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ± 10%; 0°C ≤ T_A ≤ + 70°C)[6]

	PARAMETER	MIN	MAX	UNITS	NOTES
t_{ACC}	Address to output delay time		350	ns	4
t_{CS}	Chip select to output delay time		175	ns	4
t_{CD}	Chip deselect to output delay time		150	ns	4

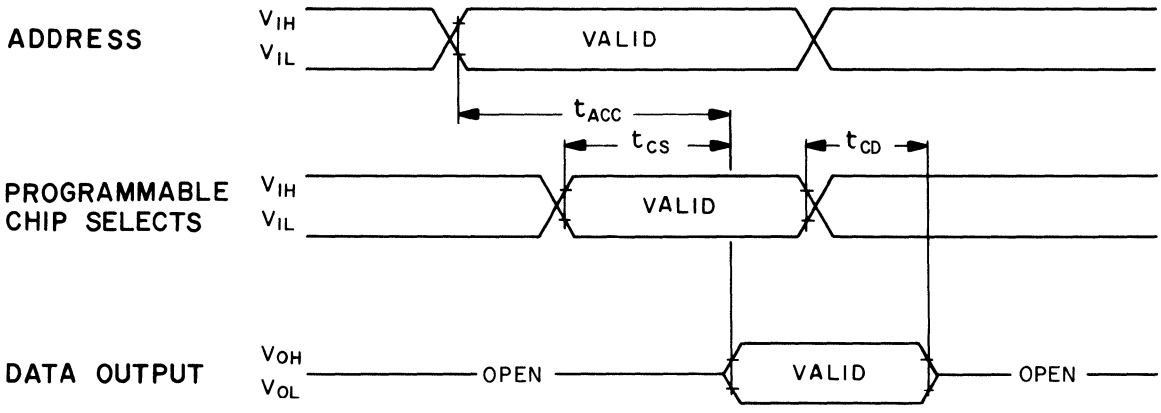
CAPACITANCE

	PARAMETER	TYP	MAX	UNITS	NOTES
C_{IN}	Input Capacitance	6	8	pF	5
C_{OUT}	Output Capacitance	10	15	pF	5

NOTES:

1. All inputs 5.5V; Data Outputs open.
2. V_{IN} = 0V to 5.5V
3. Device unselected; V_{OUT} = 0V to 5.5V.
4. Measured with 2 TTL loads and 100pF, transition times = 20ns
5. Capacitance measured with Boonton Meter or effective capacitance calculated from the equation :
   $C = \frac{I \Delta t}{\Delta V}$ with current equal to a constant 20mA.
6. A minimum 100 μs time delay is required after the application of V_{CC} (+5) before proper device operation is achieved.

TIMING DIAGRAM



* The chip select inputs can be user programmed so that either the input is enabled by a Logic 0 voltage (V_{IL}), a Logic 1 voltage (V_{IH}), or the input is always enabled (regardless of the state of the input). See chart below for programming instructions.

MOSTEK 34000 ROM PUNCHED CARD CODING FORMAT (1)

FIRST CARD

COLS	INFORMATION FIELD
1-30	Customer
31-50	Customer Part Number
60-72	MOSTEK Part Number (2)

SECOND CARD

1-30	Engineer at Customer Site
31-50	Direct Phone Number for Engineer

THIRD CARD

1-5	MOSTEK Part Number (2)
33	Chip Select One "1" = CS_1 or "0" = $\overline{CS_1}$ or "2" = Don't Care
35	Chip Select Two "1" = CS_2 or "0" = $\overline{CS_2}$ or "2" = Don't Care
37	Chip Select Three "1" = CS_3 or "0" = $\overline{CS_3}$ or "2" = Don't Care

FOURTH CARD

1-9	Data Format (3)
15-28	Logic - ("Positive Logic" or "Negative Logic")
35-57	Verification Code (4)

DATA FORMAT

128 data cards (16 data words/card) with the following format:

COLS	INFORMATION FIELD
1-4	Four digit octal address of first output word on card
5-7	Three digit octal output word specified by address in column 1-4
8-52	Next fifteen output words, each word consists of three octal digits.

NOTES:

1. Positive or negative logic formats are accepted as noted in the fourth card.
2. Assigned by MOSTEK; may be left blank.
3. MOSTEK punched card coding format should be used. Punch "MOSTEK" starting in column one.
4. Punches as: (a) VERIFICATION HOLD - i.e. customer verification of the data as reproduced by MOSTEK is required prior to production of the ROM. To accomplish this MOSTEK supplies a copy of its Customer Verification Data Sheet (CVDS) to the customer.
   (b) VERIFICATION PROCESS - i.e. the customer will receive a CVDS but production will begin prior to receipt of customer verification; (c) VERIFICATION NOT NEEDED - i.e. the customer will not receive a CVDS and production will begin immediately.

32K/64K ROMS

MOSTEK's MK 32000/MK 36000, 32K/64K bit ROMs, utilize state-of-the-art circuit and processing techniques to provide a highly reliable, low power, high performance device while maintaining a die size capable of being produced in large volume. As with other current generation MOSTEK products a 5V, ±10% tolerance power supply is combined with complete TTL compatibility to eliminate user implementation problems.

PRELIMINARY

MOSTEK

32K-BIT AND 64K-BIT MOS READ-ONLY MEMORIES

MK32000P-5/MK36000P-5

FEATURES

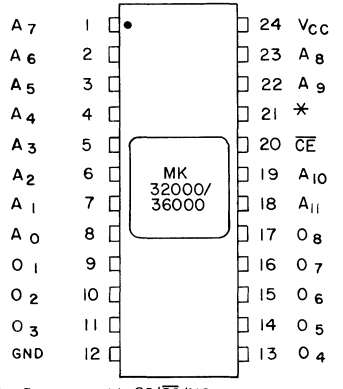
- ☐ MK 32000-4K x 8 Organization—$\overline{CE}$ activated operation
- ☐ MK 36000-8K x 8 Organization—$\overline{CE}$ activated operation
- ☐ 300ns maximum access time
- ☐ Single +5V ± 10% power supply
- ☐ Average Power Dissipation — 200mW typical
- ☐ Standby Power Dissipation—25 mW typical ($\overline{CE}$ High)
- ☐ On board latches for addresses and CS/$\overline{CS}$ (CS/$\overline{CS}$ 32000 only)
- ☐ Inputs and three-state outputs-TTL compatible
- ☐ Outputs drive 2 TTL loads and 100 pF
- ☐ Standard 24 pin DIP (EPROM Pin Out Compatible)

DESCRIPTION

The MK 32000 and MK 36000 are new generation N-channel silicon gate MOS Read Only Memories. The MK 32000 is organized as 4096 words by 8 bits and the MK 36000 is organized as 8192 words by 8 bits. As state-of-the-art devices, both ROMs incorporate advanced circuit techniques designed to provide maximum circuit density and reliability with the highest possible performance, while maintaining low power dissipation and wide operating margins.

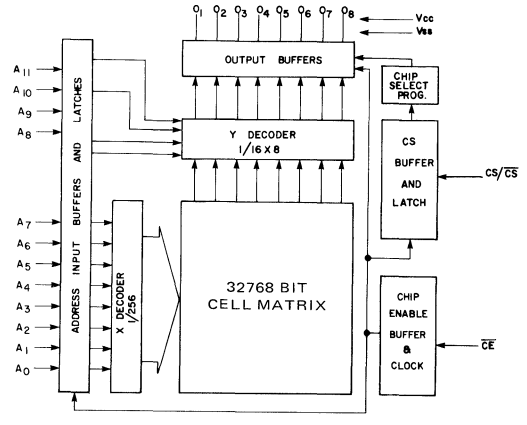
The MK 32000 and MK 36000 utilize what is fast becoming an industry standard method of device operation. Use of a static storage cell with clocked control periphery allows the circuit to be put into an automatic low power standby mode. This is accomplished by maintaining the chip enable ($\overline{CE}$) input at a TTL high level. In this mode, power dissipation is reduced to typically 25 mW, as compared to unclocked devices which draw full power continuously. In system operation, a device is

PIN CONNECTIONS

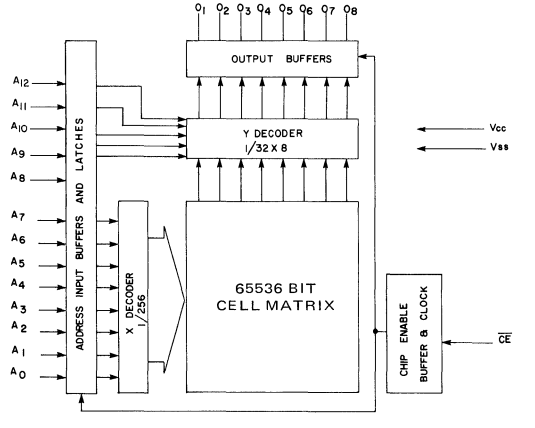


* MK 32000 = Programmable CS/$\overline{CS}$/NC
MK 36000 = A_{12}

FUNCTIONAL DIAGRAM (MK 32000)



FUNCTIONAL DIAGRAM (MK 36000)



ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Terminal Relative to Ground . . . . . −0.5V to + 7V
Operating Temperature T_A (Ambient) . . . . . 0°C to + 70°C
Storage Temperature − Ceramic (Ambient) . . . . . −65°C to + 150°C
Power Dissipation . . . . . 1 Watt

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS[6]

($0°C \leq T_A \leq +70°C$)

	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{CC}	Power Supply Voltage	4.5	5.0	5.5	Volts	6
V_{IL}	Input Logic 0 Voltage	−0.5		0.8	Volts	
V_{IH}	Input Logic 1 Voltage	2.0		V_{CC}	Volts	

D C ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ± 10%) ($0°C \leq T_A \leq +70°C$)[6]

	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
I_{CC1}	V_{CC} Power Supply Current (Active)		40		mA	1,7
I_{CC2}	V_{CC} Power Supply Current (Standby)		5		mA	1,8
$I_{I(L)}$	Input Leakage Current	−10		10	μA	2
$I_{O(L)}$	Output Leakage Current	−10		10	μA	3
V_{OL}	Output Logic "0" Voltage @ I_{OUT} = 3.3mA			0.4	volts	
V_{OH}	Output Logic "1" Voltage @ I_{OUT} = −220 μA	2.4			volts	

A C ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ± 10%) ($0°C \leq T_A \leq +70°C$)[6]

	PARAMETER	MIN	MAX	UNITS	NOTES
t_C	Cycle Time	450		ns	4
t_{CE}	$\overline{CE}$ Pulse Width	300			4
t_{AC}	$\overline{CE}$ Access Time		300	ns	4
t_{OFF}	Output Turn Off Delay		75	ns	4
t_{AH}	Address and CS Hold Time Referenced to $\overline{CE}$	100		ns	9
t_{AS}	Address and CS Setup Time Referenced to $\overline{CE}$	0		ns	9
t_P	$\overline{CE}$ Precharge Time	150		ns	

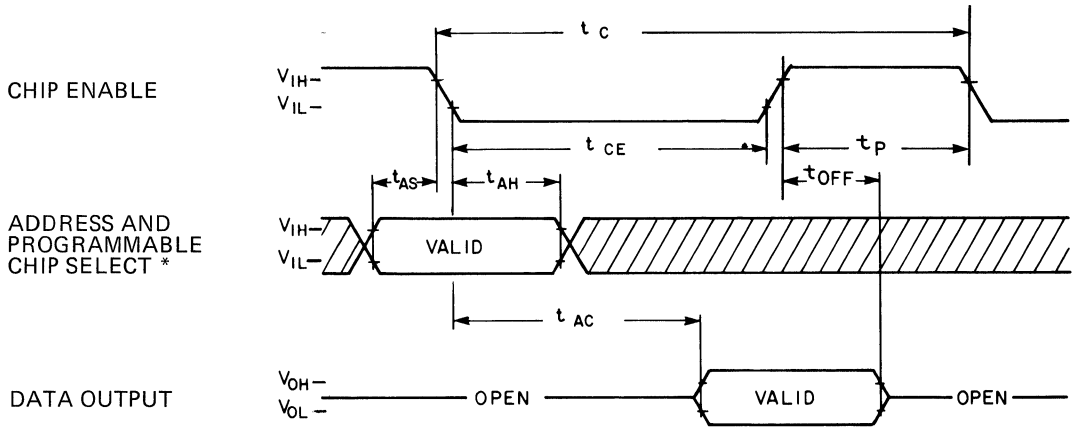
NOTES:

1. All inputs 5.5V; Data Outputs open.
2. V_{IN} = 0V to 5.5V
3. Device unselected; V_{OUT} = 0V to 5.5V
4. Measured with 2 TTL loads and 100pF, transistion times = 20ns
5. Capacitance measured with Boonton Meter or effective capacitance calculated from the equation:

   $C = \frac{I \Delta t}{\Delta V}$ with current equal to a constant 20mA.

6. A minimum 100 μs time delay is required after the application of V_{CC} (+5) before proper device operation is achieved.
7. Current is proportional to cycle rate. I_{CCI} is measured at the specified minimum cycle time.
8. $\overline{CE}$ high.
9. CS applies only to MK 32000.

TIMING DIAGRAM



* The chip select input can be user programmed so that either the input is enabled by a Logic 0 voltage (V_{IL}), a Logic 1 voltage (V_{IH}), or the input is always enabled (regardless of the state of the input). See chart below for programming instructions. This applies to the MK 32000 only.

MOSTEK 32000/36000 ROM PUNCHED CARD CODING FORMAT (1 & 6)

FIRST CARD

COLS	INFORMATION FIELD
1-30	Customer
31-50	Customer Part Number
60-72	MOSTEK Part Number (2)

SECOND CARD

1-30	Engineer at Customer Site
31-50	Direct Phone Number for Engineer

THIRD CARD

1-5	MOSTEK Part Number (2)
33	Chip Select (MK 32000 only) "1" = CS or "0" = $\overline{CS}$ or "2" = Don't Care

FOURTH CARD

1-9	Data Format (3)
15-28	Logic - ("Positive Logic" or "Negative Logic")
35-57	Verification Code (4)

DATA FORMAT

256 or 512 data cards (16 data words/card) with the following format: (Note 5)

COLS	INFORMATION FIELD
1-4	Four digit octal address of first output word on card
5-7	Three digit octal output word specified by address in column 1-4
8-52	Next fifteen output words, each word consists of three octal digits.

NOTES:

1. Positive or negative logic formats are accepted as noted in the fourth card.
2. Assigned by MOSTEK; may be left blank.
3. MOSTEK punched card coding format should be used. Punch "MOSTEK" starting in column one.
4. Punches as: (a) VERIFICATION HOLD - i.e. customer verification of the data as reproduced by MOSTEK is required prior to production of the ROM. To accomplish this MOSTEK supplies a copy of its Customer Verification Data Sheet (CVDS) to the customer.
   (b) VERIFICATION PROCESS - i.e. the customer will receive a CVDS but production will begin prior to receipt of customer verification; (c) VERIFICATION NOT NEEDED - i.e. the customer will not receive a CVDS and production will begin immediately.
5. 256 cards for MK 32000; 512 cards for MK 36000
6. Please consult MOSTEK ROM Programming Guide for further details on other formats.

DESCRIPTION (Continued)

selected by the $\overline{CE}$ input, while all others are in a low power mode, reducing the overall system power. Lower power means reduced power supply cost, less heat to dissipate and an increase in device and system reliability.

The edge activated chip enable also means greater system flexibility and an increase in system speed. The MK 32000 and MK 36000 feature onboard address latches controlled by the $\overline{CE}$ input. Once the address hold time specification has been met, new address data can be applied in anticipation of the next cycle. Outputs can be wire-'OR'ed together, and a specific device can be selected by utilizing the $\overline{CE}$ input with no bus conflict on the outputs. The MK 32000 offers added flexibility with the availability of a programmable chip select input pin, allowing another dimension of decode. The $\overline{CE}$ input allows the fastest access times yet available in 5 volt only ROM's and imposes no loss in system operating flexibility over an unclocked device.

Other system oriented features include fully TTL compatible inputs and outputs. The three state outputs, controlled by the $\overline{CE}$ input, will drive a minimum of 2 standard TTL loads. The MK 32000/ MK 36000 both operate from a single +5 volt power supply with a wide ± 10% tolerance, providing the widest operating margins available. Both the MK 32000 and MK 36000 are packaged in the industry standard 24 DIP.

Any application requiring a high performance, high bit density ROM can be satisfied by either the MK 32000 or the MK 36000 ROM. These devices are ideally suited for 8 bit microprocessor systems such as those which utilize the Z-80. Both devices offer significant cost advantages over PROM.

OPERATION

Both the MK 32000 and MK 36000 are controlled by the chip enable ($\overline{CE}$) input. A negative going edge at the $\overline{CE}$ input will activate the device as well as strobe and latch the inputs into the onboard address registers. At access time the outputs will become active and contain the data read from the selected location. On the MK 32000, the programmable chip select can be used to deselect the output. The state of the CS/$\overline{CS}$ input is latched into the chip by the $\overline{CE}$ input. The outputs will remain latched and active until $\overline{CE}$ is returned to the inactive state.

Programming Data

MOSTEK is now able to utilize a wide spectrum of data input formats and media. Those presently available are listed in the following table:

TABLE I

Acceptable Media	Acceptable Format
CARDS	MOSTEK
PAPER TAPE	INTEL CARD
PROMS	INTEL TAPE
DATA LINK	EA
	MOSTEK F-8
	MOTOROLA 6800

PROGRAMMABLE ROMS

MOSTEK's PROM family is ideally suited for applications where fast turnaround and pattern experimentation are important. These reliable products offer significant advantages over hard-wired logic in cost, system flexibility and performance.

MOSTEK

256x8 Bit Electrically Programmable/Ultraviolet Erasable ROM

MK3702T/MK3602P/MK1702A

FEATURES

- ☐ Replacement for the popular 1702A PROM
- ☐ Improved performance:

  Random access of 550 ns (−1)
  750 ns (−2)
  1 μs (−3)

- ☐ No V_{GG} power supply required
- ☐ All inputs TTL compatible
- ☐ Three-state TTL-compatible outputs —"OR-tie" capability
- ☐ High speed programming: Typically 30 seconds for all 2048 bits using standard PROM (1702A) programmers with no modifications
- ☐ Hermetically sealed package with transparent lid
- ☐ Typical Application — Microprocessor system prototyping aid

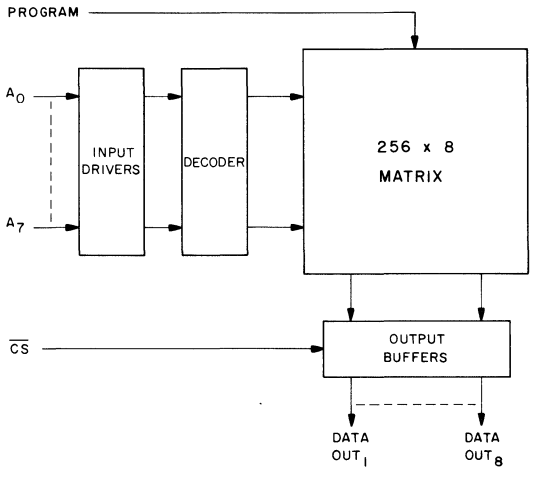
DESCRIPTION

The MK 3702 is a 256 x 8 bit electrically programmable and ultraviolet erasable Read Only Memory circuit, fabricated with MOSTEK's P-Channel Silicon-Gate technology. The MK 3702 PROM is ideally suited for applications where fast turnaround and pattern experimentation are important. The MK 3702 is a very reliable device that offers significant advantages over hard-wired logic in cost, system flexibility and performance. MOSTEK performs complete programming and functional testing on all 2048 bit locations prior to shipment to insure 100% programmability.**

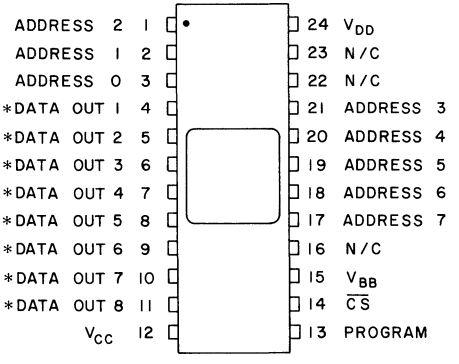
The MK 3702 is packaged in a 24-pin dual-in-line (DIP) package with a transparent, hermetically sealed lid. This allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can be written into the device by following the programming procedures outlined in this data sheet. This procedure can be repeated as many times as required.

MOSTEK also has available the MK 3602 which is identical to the MK 3702 in every respect except for the package. The MK 3602 is packaged in a 24-pin DIP with a metal lid. Therefore, the MK 3602 is not erasable by exposure to ultraviolet light.

FUNCTIONAL DIAGRAM



PIN CONNECTIONS



MODE \ PIN	12 (V_{CC})	13 (PROGRAM)	14 ($\overline{CS}$)	15 (V_{BB})
READ	V_{CC}	V_{CC}	GND	V_{CC}
PROGRAMMING	GND	PROGRAM PULSE	GND	V_{BB}

**MOSTEK's liability shall be limited to replacing any unit which fails to program as desired.

*This pin is the data input lead during programming.

ABSOLUTE MAXIMUM RATINGS*

Operating Temperature T_A (Ambient) . . . . . 0°C to + 70°C

Storage Temperature (Ambient) . . . . . –65°C to + 125°C

V_{CC} relative to V_{BB} . . . . . –12.0V

Voltage on any pin (except V_{CC}) relative to V_{BB} . . . . . –60.0V

Voltage on any pin (except V_{BB}) relative to V_{CC} . . . . . –48.0V
(V_{BB}–V_{CC} = 13.2V)

Power Dissipation 2W

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

READ OPERATION

DC Electrical Characteristics

(0°C≤T_A≤70°C) (V_{CC} = 5V ± 5%, V_{DD} = –9V ± 5%, V_{BB} = 5V ± 5%)

PARAMETER		MIN	TYP(2)	MAX	UNITS	NOTES
$I_{I(L)}$	Input Leakage, Address and Chip Select Inputs			1	μA	3
$I_{O(L)}$	Output Leakage Current			1	μA	4
I_{DD}	V_{DD} Power Supply Current			60	mA	5
V_{IL}	Input Logic "0" Voltage (all inputs)	–1.0		0.65	V	
V_{IH}	Input Logic 1 Voltage (all inputs)	V_{CC}–2		V_{CC}+0.3	V	
V_{OL}	Output Logic "0" Voltage I_{OUT} = 2.0mA			0.4	V	
V_{OH}	Output Logic 1 Voltage I_{OUT} = –100μA	3.5	4.5		V	

CAPACITANCE

Parameter		Min	Typ	Max	Units	Notes
C_{IN}	Input capacitance		7	15	pf	
C_{OUT}	Output capacitance		7	15	pf	

NOTES:

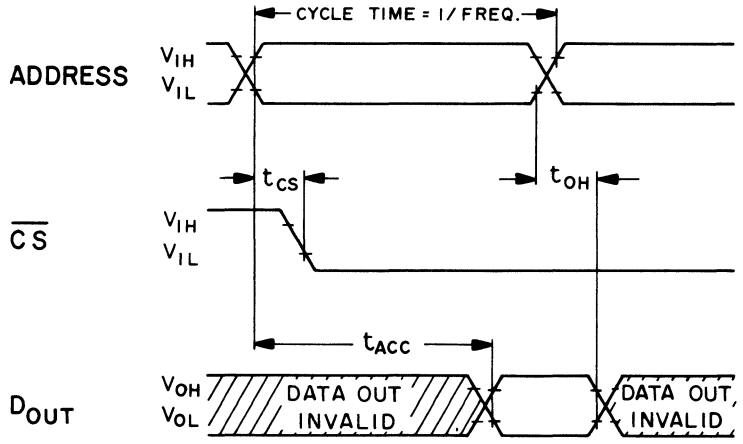
1. In the programming mode, the data inputs 1-8 are pins 4-11 respectively, $\overline{CS}$ = Ground.
2. Typical values are at nominal voltages and T_A = + 25°C.
3. V_{IN} = 0 Volts.
4. V_{OUT} = 0 Volts, $\overline{CS}$ = logic 1.
5. $\overline{CS}$ = logic 1, I_{OL} = 0mA (outputs open-circuit) T_A = 0°C.

AC Electrical Characteristics

($0°C \leq T_A \leq 70°C$) (V_{CC} = 5V ±5%, V_{DD} = –9V ±5%)

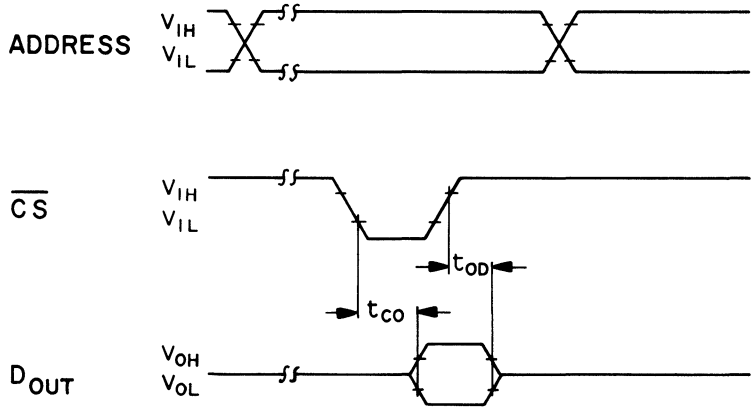
Parameter		MK 3702–1 Min	MK 3702–1 Max	MK 3702–2 Min	MK 3702–2 Max	MK 3702–3 Min	MK 3702–3 Max	Units	Notes
t_{ACC}	Address to output delay		550		750		1000	ns	
t_{CO}	Output delay from $\overline{CS}$		450		450		450	ns	
t_{CS}	Chip select delay		100		300		550	ns	
t_{OD}	Output deselect		300		300		300	ns	
t_{OH}	Previous data valid		100		100		100	ns	
Freq.	Repetition Rate		1.8		1.3		1.0	MHz	

READ OPERATION TIMING DIAGRAM



Load condition = 1 TTL gate and C_L = 50 pf.

DESELECTION OF DATA OUTPUT IN OR-TIE OPERATION



PROGRAMMING OPERATION [1]

DC Electrical Characteristics

(T_A = 25°C) (V_{CC} = 0V, V_{BB} = +12V ±10%, $\overline{CS}$ = 0V)

Parameter		Min	Typ	Max	Units	Notes
I_{LI1P}	Address and data input load current			10	mA	6
I_{LI2P}	Program load current			10	mA	6
I_{BB}	V_{BB} supply load current		10		mA	10
I_{DDP}	Peak V_{DD} supply load current			150	mA	7, 9
I_{DDPA}	Average V_{DD} supply load current		40		mA	8
V_{IHP}	Input high voltage			0.3	V	
V_{IL1P}	Pulsed data input low voltage	–46		–48	V	
V_{IL2P}	Address input low voltage	–40		–48	V	
V_{IL3P}	Pulsed input low V_{DD} and program voltage	–46		–48	V	

AC Electrical Characteristics

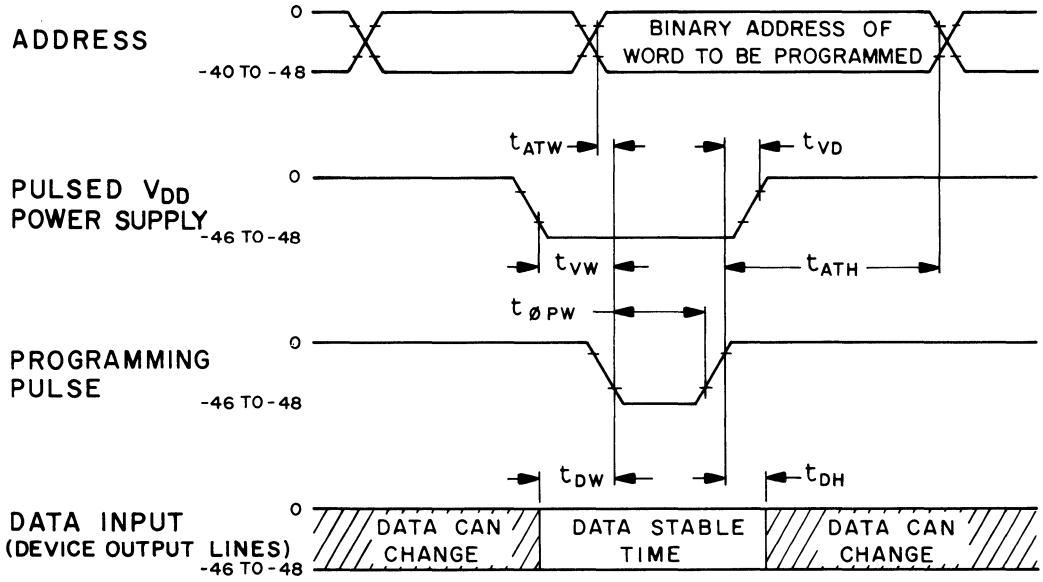
(T_A = 25°C) (V_{CC} = 0V, V_{BB} = +12V ±10%, $\overline{CS}$ = 0V)

Parameter		Min	Max	Units	Notes
	V_{DD} duty cycle		20	%	
$t_{\Phi PW}$	Program pulse width		3	ms	9
t_{DW}	Data set up time	25		μs	
t_{DH}	Data hold	10		μs	
t_{VW}	V_{DD} set up time	100		μs	
t_{VD}	V_{DD} hold time	10	100	μs	
t_{ATW}	Address set up time	10		μs	
t_{ATH}	Address hold time	10		μs	

NOTES (Continued)

6. V_{IN} = –48 Volts.
7. I_{DDP} flows only during V_{DD} on time. I_{DDP} should not be allowed to exceed 150mA for greater than 200 μsec.
8. Average power supply current is measured at 20% duty cycle.
9. V_{DD} = V_{prog} = –48V.
10. The V_{BB} supply must be limited to 100mA maximum current to prevent damage to the device.

PROGRAM OPERATION TIMING DIAGRAM



Conditions — Input pulse rise and fall times $\leq 1\mu$sec; $\overline{CS}$ = 0V.

PROGRAMMING INSTRUCTIONS

1. Operation in the Program Mode (MK 3602/MK 3702)

Initially, all 2048 bits of the ROM are in the "0" state (output low). Information is introduced by selectively programming "1s" (output high) in the proper bit locations. Word address selection is done by the same decoding circuitry used in the READ mode (see logic levels). The address should be programmed in the sequence 0 through 255 for a minimum of 32 times. The eight output terminals are used as data inputs to determine the information pattern in the eight bits of each word. A low data input level (−48V) will program a "1" and a high data input level (ground) will leave a "0". All eight bits of one word are programmed simultaneously by setting the desired bit information patterns on the data input terminals. During the programming procedure, V_{DD} and the Program Pulse are pulsed signals.

2. MK 3702 Erasing Procedure

The MK 3702 may be erased by exposure to high intensity ultraviolet light by illuminating the chip through the window. This exposure to ultraviolet light induces the flow of a photo current from the floating gate to the substrate, thereby discharging the gate to its initial state. An ultraviolet light source of 2537Å yielding a total integrated dosage of 6W−sec/cm^2 is required. Note that the MK 3702 will be completely erased, as there is no known method of selectively erasing any portion of the chip.

Examples of ultraviolet light sources which can erase the MK 3702 in 10 to 20 minutes are the Model UVS-54 and Model S-52 short-wave ultraviolet lamps manufactured by Ultra-Violet Products, Inc. (5114 Walnut Grove Avenue, San Gabriel, California). The lamps should be used without short-wave filters, and the MK 3702 to be erased should be placed about one inch away from the lamp tubes.

MK 3702 PROGRAMMING/APPLICATIONS CONSIDERATIONS

The MOSTEK MK 3702 can be programmed on commercially available equipment from the following manufacturers:

DATA I/O – Model V, 909 – 1011 – 1
PROLOG – Series 90, PM 9001
SPECTRUM DYNAMICS–Series 550 434-549

The device may also be programmed on any other equipment capable of programming any of the popular 1702A type PROMS.

Many of MOSTEK's distributor locations are also equipped to program the MK 3702. The distributors can program the parts from customer supplied paper tape in a variety of formats. The most common of these formats include:

1. ASCII P–N format
2. ASCII H–L format
3. Spectrum Dynamics – ASCII format
4. Binary or DATA I/O format

Check with the MOSTEK distributor in your area for the format(s) which is best suited to his equipment.

The MK 3702 As A Microprocessor Design Aid

The ability of the MK 3702 to be erased and reprogrammed is of great value in the development of microprocessor systems. This feature, coupled with a 256 word by 8 bit internal organization makes the MK 3702 an ideal component for use with MOSTEK's F-8 microprocessor family.

Figure 1 is a block diagram which illustrates a simple F-8 system utilizing MK 3702's as non-volatile memory storage. Basically, the system consists of one F-8 CPU (MK 3850), one static memory interface (SMI-MK 3853), and several MK 3702 PROMs. The SMI serves as a communication link between the CPU and the MK 3702 PROMs. This type of configuration can be used for production systems where there are a number of variations of the same basic machine. An example of this might be a Point of Sale (POS) terminal where local tax tables could be stored in PROM. The PROM would allow simple and inexpensive update as local tax rates change.

Another market that could be addressed with a PROM system is one where a customer might want 400 systems but needs 50 of one configuration, 10 of another, etc. In this case, it is hard to justify a mask ROM. However, if a system can be implemented with mask ROM, MOSTEK has available a Program Storage Unit (PSU – MK 3851) which is organized as 1K x 8.

If a PSU is to be used in a system it is important to have the program in correct and final form before the ROM is manufactured. To aid in the development of an F-8 system, MOSTEK has available a prototyping tool called the F-8 PSU Emulator. The Emulator board contains four MK 3702 PROMs plus the control logic required to completely simulate a PSU ROM. With this tool, the designer can now develop his program and make as many changes as required until the program is correct. Once the program has been tested using the Emulator, a mask ROM (PSU) can be developed.

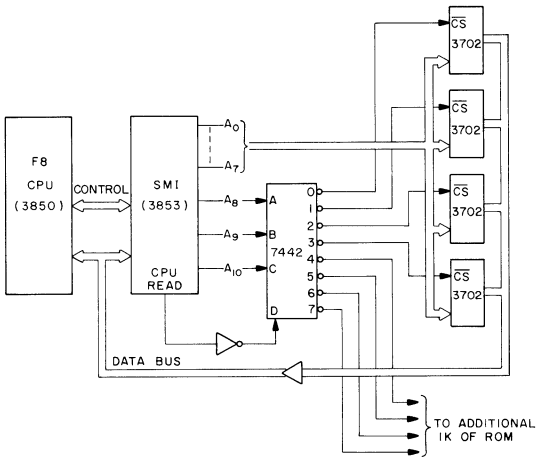


Figure 1 – Typical F8 system.

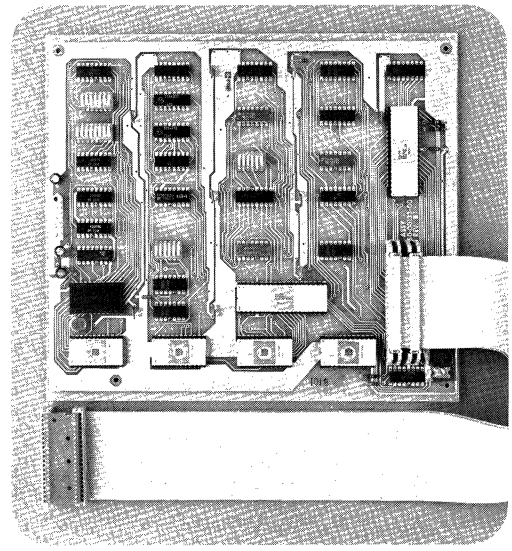


Figure 2 – MOSTEK's F8 PSU Emulator Board.

PRELIMINARY

MOSTEK

8K BIT ELECTRICALLY PROGRAMMABLE/ULTRAVIOLET ERASABLE ROM

MK 2708T

FEATURES

- ☐ Replacement for popular 2708 type EPROM
- ☐ Static operation — no clocks required
- ☐ Low power dissipation — less than 450 mW in READ mode
- ☐ 450ns maximum access time
- ☐ Inputs and outputs TTL compatible
- ☐ Standard supplies +12V, ±5V
- ☐ Three state output "OR" tie capability
- ☐ Standard 24 pin DIP with transparent lid

DESCRIPTION

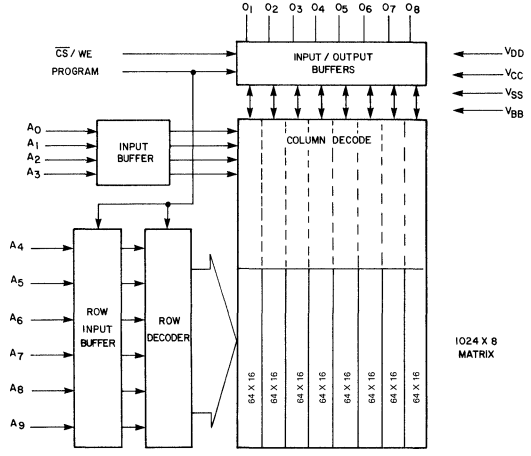
The MK 2708 is a 1024 x 8 bit Electrically Programmable/Ultraviolet Erasable Read Only Memory. The circuit is fabricated with MOSTEK's advanced N-channel silicon gate technology for the highest performance and reliability. The MK 2708 offers significant advantages over hardwired logic in cost, system flexibility, turnaround time and performance.

System oriented features include direct interfacing capability with TTL during both the READ and PROGRAM modes. The three state outputs provide "OR" tie capability for construction of larger arrays. Power requirements include +12V, +5V and −5V supplies. Power dissipation has been reduced to less than 450 mW. Complete programming and functional testing on all 8192 bit locations is performed prior to shipment to insure 100% programmability.

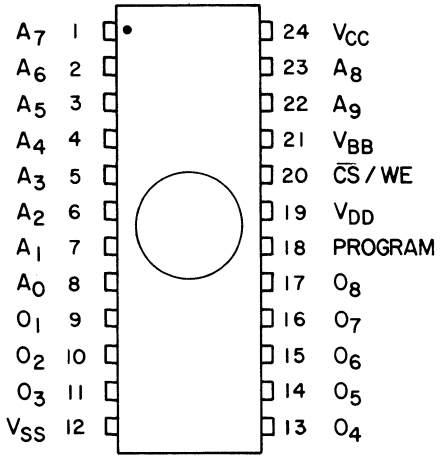
The MK 2708 is packaged in the industry standard 24 pin dual-in-line (DIP) package with a transparent hermetically sealed lid. This allows the user to expose the chip to ultraviolet light to erase the data pattern. A new pattern may then be written into the device by following the programming procedures outlined in this data sheet.

The MK 2708 is specifically designed to fit those applications where fast turnaround time and pattern experimentation are required. The 8 bit wide parallel output of the MK 2708 makes it ideally suited for use in microprocessor systems. Since data may be altered in the device (erase and reprogram) it allows for early debugging of the system program and for updating the system capabilities in the field. Once the program is fixed and the intention is to produce large numbers of systems, MOSTEK also supplies a pin compatible mask programmable ROM, the MK 30000. To transfer the program data to ROM, the user need only send the PROM along with part information to Mostek, from which the ROM with the required pattern can be generated. This means a reduction in the possibility of error when converting data to other forms (cards, tape, etc.) for this purpose. However, data may still be input by any of these traditional means, such as paper tape, card deck, etc.

FUNCTIONAL DIAGRAM



PIN CONNECTIONS



ABSOLUTE MAXIMUM RATINGS*

Operating temperature T_A (Ambient) . . . . . 0°C to + 70°C
Storage temperature T_A (Ambient) . . . . . −65°C to + 125°C
V_{DD} with respect to V_{BB} . . . . . −.3V to +20V
V_{CC} and V_{SS} with respect to V_{BB} . . . . . −.3V to +15V
All input or outputs with respect to V_{BB} during read . . . . . −.3V to +15V
$\overline{CS}$/WE input with respect to V_{BB} during programming . . . . . −.3V to +20V
PROGRAM input with respect to V_{BB} . . . . . −.3V to +35V
Power dissipation 1W

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

READ OPERATION

Recommended DC Operating Conditions

($0° C \leq T_A \leq 70° C$)

	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{DD}	Supply Voltage	11.4	12.0	12.6	Volts	1
V_{CC}	Supply Voltage	4.75	5.0	5.25	Volts	1
V_{BB}	Supply Voltage	−4.75	−5.0	−5.25	Volts	1
V_{SS}	Supply Voltage	0	0	0	Volts	1
V_{IL}	Logic '0' Voltage All Inputs	VSS		0.65	Volts	1
V_{IH}	Logic '1' Voltage All Inputs	3.0		V_{CC} + 1	Volts	1

DC Electrical Characteristics

($0°C \leq T_A \leq 70° C$) (V_{DD} = + 12V ±5%, V_{CC} = + 5V± 5%, V_{BB} = −5V± 5%, V_{SS} = OV)

	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
I_{DD}	V_{DD} Power Supply Current			20	mA	2
I_{CC}	V_{CC} Power Supply Current			10	mA	2
I_{BB}	V_{BB} Power Supply Current			24	mA	2
V_{OL}	Output Low Level (Logic '0') I_{OUT} = 3.2mA			0.40	Volts	
V_{OH1}	Output High Level (Logic '1') I_{OUT} = −100 μA	3.7			Volts	
V_{OH2}	Output High Level (Logic '1') I_{OUT} = −1mA	2.4			Volts	
$I_{I(L)}$	Input Leakage Current	−10		10	μA	3
$I_{O(L)}$	Output Leakage Current	−10		10	μA	4

NOTES:

1. All voltages referenced to V_{SS}
2. Power supply currents are specified under worst case conditions on over temperature range of 0° C to +70° C. $\overline{CS}$/WE = 0V or +5V
3. V_{IN} = 0 to 5.25V
4. V_{OUT} = 5.25V, $\overline{CS}$ = 5 volts
5. Load conditions = 1 TTL load and 100pF

AC Electrical Characteristics (5)

($0°C \leq T_A \leq 70°C$) (V_{DD} = + 12V±5%, V_{CC} = + 5V±5%, V_{BB} = −5V± 5%, V_{SS} = 0V)

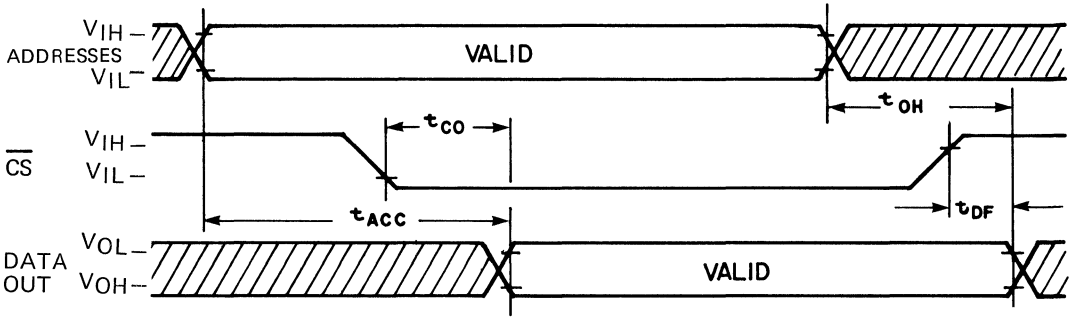
	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
t_{ACC}	Access Time Referenced to Address Valid			450	ns	5
t_{CO}	Chip Select to Output Delay			250	ns	5
t_{DF}	Chip Deselect to Output Open	0		250	ns	5
t_{OH}	Output Hold Time	0			ns	5

Capacitance

(T_A = 25° C)

	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
C_{IN}	Input Capacitance		4	6	pF	
C_{OUT}	Output Capacitance		8	12	pF	

READ OPERATION TIMING DIAGRAM



PROGRAMMING OPERATION

PROGRAMMING INSTRUCTIONS

Operation in the Program Mode

The MK 2708 as shipped from MOSTEK will be completely erased. In this initial state and after any subsequent erasure, all bits will be at a '1' level (output high). Information is introduced by selectively programming 'O's in to the proper bit locations. Once a '0' has been programmed into the chip it may be changed only by erasing the entire chip with UV light.

Word address selection is done by the same decode circuitry used in the read mode. The circuit is put into the programming mode by maintaining the $\overline{CS}$/WE input at +12V. In this mode the output pins serve as inputs (8 bits in parallel) for the required program data. Logic levels for other inputs and the supply voltages are the same as in the read mode.

Once address set-up and data set-up times have been met, one program pulse per address is applied to the program input. Each of 1024 address locations are programmed sequencially in this manner. One cycle thru all 1024 addresses constitutes a loop. The number of required loops (N) is a function of program pulse width according to the following equation:

$$N \times t_{PW} \geq 100 \text{ ms}$$

This implies that the number of loops (N) range from a minimum of 100 (t_{PW} = 1 ms) to 1000 (t_{PW} = .1 mS).

Recommended DC Operating Conditions
(T_A = 25° C)

	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{DD}	Supply Voltage	11.4	12.0	12.6	Volts	1
V_{CC}	Supply Voltage	4.75	5.0	5.25	Volts	1
V_{BB}	Supply Voltage	−4.75	−5.0	−5.25	Volts	1
V_{SS}	Supply Voltage	0	0	0	Volts	1
V_{IL}	Input Logic '0' Level Except PROGRAM	V_{SS}		0.65	Volts	1
V_{IH}	Input Logic '1' Level (Addresses and Data)	3.0		V_{CC} + 1	Volts	1
V_{IHW}	$\overline{CS}$/WE Input High Level	11.4	12.0	12.6	Volts	1, 2
V_{IHP}	PROGRAM Pulse Input High Level	25.0		27.0	Volts	1, 2
V_{ILP}	PROGRAM Pulse Input Low Level	V_{SS}		1.0	Volts	1, 2

DC Electrical Characteristics
(T_A = 25° C) (V_{DD} = 12V ±5%, V_{CC} = +5V ± 5%, V_{BB} = −5V ± 5%, V_{SS} = OV)

	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
I_{DD}	V_{DD} Supply Current			20	mA	3
I_{CC}	V_{CC} Supply Current			10	mA	3
I_{BB}	V_{BB} Supply Current			45	mA	3
$I_{I(L)}$	Input Leakage Current			10	μA	4, 5
I_{IPL}	PROGRAM Pulse Source Current			TBD	mA	
I_{IPH}	PROGRAM Pulse Sink Current			TBD	mA	

NOTES:

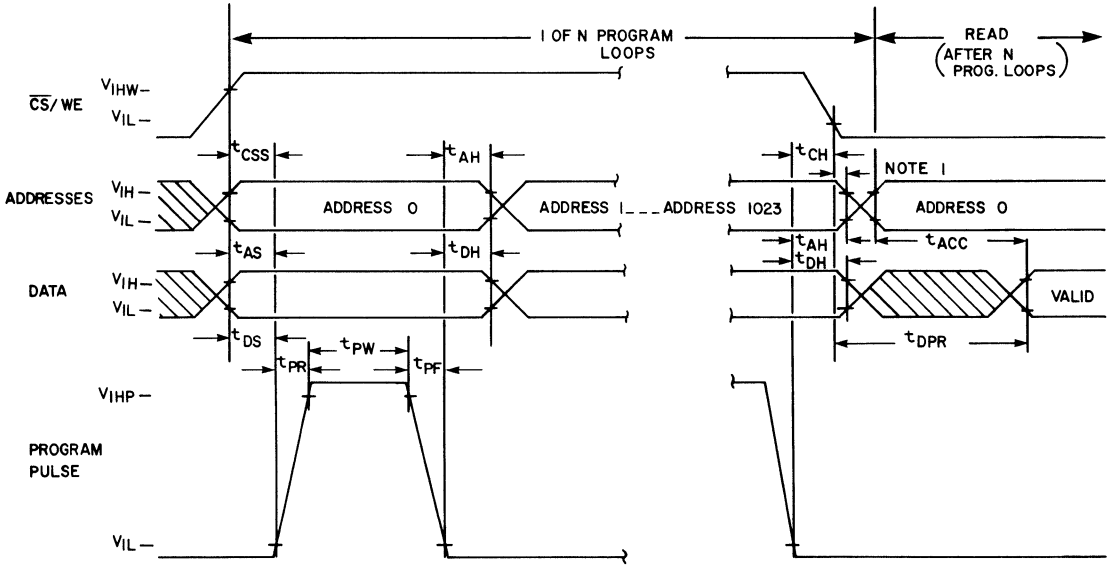
1. All voltages are referenced to V_{SS}.
2. Programming mode only.
3. Power supply currents are specified under worst case conditions at T_A = 25° C and $\overline{CS}$/WE = +12V.
4. V_{IN} = 0 to 5.25V.
5. In program mode output pins are used as inputs.

AC Electrical Characteristics

(T_A = 25°C) (V_{DD} = +12V±5%, V_{CC} = +5V±5%, V_{BB} = −5V± 5%, V_{SS} = 0V)

	PARAMETER	MIN	MAX	UNITS	NOTES
t_{AS}	Address Set-Up Time	10		μs	
t_{CSS}	$\overline{CS}$/WE Set-Up Time	10		μs	
t_{DS}	Data Set-Up Time	10		μs	
t_{AH}	Address Hold Time	1		μs	
t_{CH}	$\overline{CS}$/WE Hold Time	.5		μs	
t_{DH}	Data Hold Time	1		μs	
t_{DF}	Chip Deselect to Output Off	0	250	μs	
t_{DPR}	Program to Read Delay		10	μs	
t_{PW}	Program Pulse Width	.1	1.0	ms	
t_{PR}	Program Pulse Rise Time	.5	2.0	μs	
t_{PF}	Program Pulse Fall Time	.5	2.0	μs	

TIMING DIAGRAM



NOTE:

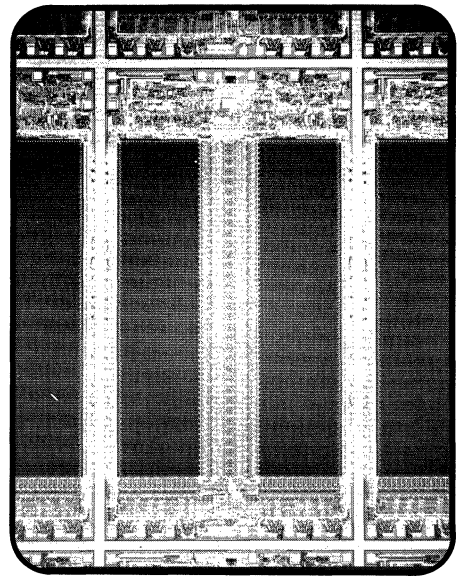
The $\overline{CS}$/WE transition must occur after the program pulse transition and before the address transition.

MK 2708 Erasing Procedure

The MK 2708 may be erased by exposure to high intensity ultraviolet light, illuminating the chip thru the transparent window. This exposure to ultraviolet light induces the flow of a photo current from the floating gate to the substrate, thereby discharging the gate to its initial state. An ultraviolet source of 2537Å yielding a total integrated dosage of 10 Watt-seconds/cm^2 is required. Note that all bits of MK 2708 will be erased.

An example of an ultraviolet light source which can erase the MK 2708 in 10 to 20 minutes is the Model S-52 short wave ultraviolet lamps manufactured by Ultra-Violet Products, Inc. (5114 Walnut Grove Avenue, San Gabriel, California). The lamp should be used without short wave filters, and the MK 2708 to be erased should be placed about one inch away from the lamp tubes. It should be noted that as the distance between the lamp and the chip is doubled, the exposure time required goes up by a factor of 4. The UV content of sunlight is insufficient to provide a practical means of erasing the MK 2708. However, it is not recommended that the MK 2708 be operated or stored in direct sunlight, as the UV content of sunlight may cause erasure of some bits in a short period of time.

RANDOM ACCESS MEMORIES



MOSTEK

1024x1 BIT DYNAMIC RAM

MK 4006 P-6/MK 4008 P-6

FEATURES

- ☐ TTL/DTL Compatible inputs
- ☐ No Clocks Required
- ☐ Access time:
  MK 4006 P-6 under 400 ns
  MK 4008 P-6 under 500 ns
- ☐ Standby Power: under 50 mW
- ☐ 16-Pin Standard CDIP
- ☐ Supply Voltage: +5V and −12V

DESCRIPTION

This is a family of MOS dynamic 1024x1 random-access memories having identical functional characteristics, differing only in speed. Access time in the MK 4006 P-6 is less than 400 ns; in the MK 4008 P-6 less than 500.

Full address decoding is provided internally. Information is read out non-destructively (NDRO) and has the same polarity as the input data.

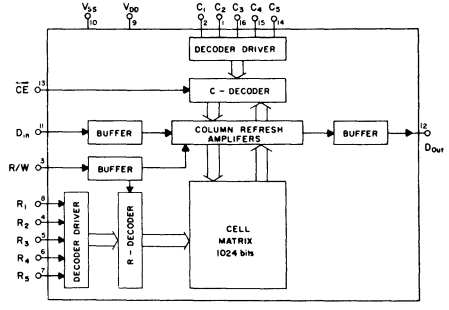
TTL/DTL compatibility at all inputs allows economical use in small systems by eliminating the need for special interface circuitry. Large main-memory applications also benefit from the low drive-voltage swings as well as the packing density afforded by the standard 16-pin dual-in-line packaging and low standby power.

The internal memory element of this RAM is a capacitance, and refreshing must be periodically initiated (see TIMING). However, all internal decoding and sensing is static, so that precharging or clocking normally associated with dynamic memories is not required. From the user's viewpoint, memory control and addressing are essentially those of a static device.

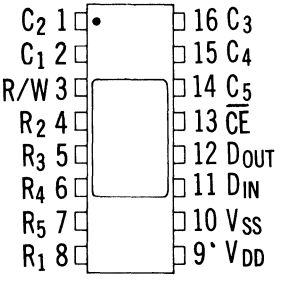
Noise suppression measures normally employed in DTL or TTL systems are sufficient. High voltage input swings and high peak-current line drivers are unnecessary for driving memory inputs and the memory itself does not exhibit large supply current transients.
Data output is single-ended to minimize propagation delay. Output current is sourced from V_{SS} (+5V), and easily sensed using readily available components. A logic 1 at the output terminal appears as a 5,000 Ohm resistor (MK 4006) to +5V; a logic 0 as an open circuit.

The performance of this RAM is made possible by Mostek's ion-implantation process. In addition to offering low threshold voltages for TTL/DTL compatibility and utilizing conventional P-channel processing, ion-implantation allows both enhancement (normally OFF) and depletion (normally ON) MOS transistors to be fabricated on the same chip. By replacing conventional MOS load resistors with constant-current depletion transistors, operational speeds and functional density are increased.

FUNCTIONAL DIAGRAM



PIN CONNECTIONS



ABSOLUTE MAXIMUM RATINGS

Voltage on any pin relative to V_{SS} ..... +0.3 to −20V

Operating Temperature ..... 0°C to +70°C

Storage Temperature Range ..... −65°C to +150°C

RECOMMENDED DC OPERATING CONDITIONS

(0° C $\leq T_A \leq$ 70°C)

	PARAMETER	MK 4006P-6 MIN	MK 4006P-6 MAX	MK 4008P-6 MIN	MK 4008P-6 MAX	UNITS	NOTES
V_{SS}	Supply Voltage		+4.75		+5.25	V	
V_{DD}	Supply Voltage		−11.4		−12.6	V	
V_{IL}	Input Voltage, Logic 0				+0.8	V	
V_{IH}	Input Voltage, Logic 1		$V_{SS}-1$		V_{SS}	V	
V_{SB}	Standby Supply Voltage (Fig. 4)		$V_{SS}-4$		$V_{SS}-6$	V	Note 1

RECOMMENDED AC OPERATING CONDITIONS[2]

(0° C $\leq T_A \leq$ 70°C)

	PARAMETER	MK 4006P-6 MIN	MK 4006P-6 MAX	MK 4008P-6 MIN	MK 4008P-6 MAX	UNITS	NOTES
t_{RC}	Read Cycle Time (Fig. 1)	400		500		ns	
t_{WC}	Write Cycle Time (Fig. 2)	650				ns	t_{WP}=250 ns
				900		ns	t_{WP}=400 ns
t_{WP}	Write Pulse Width (Fig. 2)	250				ns	t_{AW}=400 ns
				400		ns	t_{AW}=500 ns
t_{AW}	Address-to-Write Delay (Fig. 2)	400				ns	t_{WP}=250 ns
				500		ns	t_{WP}=400 ns
t_{DLD}	Data-to-Write Lead Time (Fig. 2)	300				ns	t_{WP}=250 ns
				400		ns	t_{WP}=400 ns
t_{RDLY}	Refresh Time (Fig. 3)		2		2	ms	See Note 3.
t_{CDPD}	Chip-Disable-to-Power-Down Delay (Fig. 4)	200		200		ns	See Note 1 See Note 4

DC ELECTRICAL CHARACTERISTICS

(V_{SS} = +5V ± 5%; V_{DD} = −12V ± 5%; 0°C $\leq T_A \leq$ 70°C unless otherwise noted)

	PARAMETER	MK 4006P-6 MIN	MK 4006P-6 MAX	MK 4008P-6 MIN	MK 4008P-6 MAX	UNITS	NOTES
I_{SS}, I_{DD}	Supply Current: At T_A=0°C		32		32	mA	Output
	At T_A=70°C		27		27	mA	Open
P_{SDBY}	Power Dissipation, Standby		50		50	mW	$V_{SS}-V_{DD}$ = 5V; Note 1
I_{IH}	Input Current, Logic 1. Any Input	−5	+5	−5	+5	μA	$V_I=V_{SS}-1V$
I_{IL}	Input Current, Logic 0, Any Input	−5	+5	−5	+5	μA	V_I=0.8V
I_{OH}	Output Current, Logic 1	1.0		0.8		mA	Note 5
I_{OL}	Output Current, Logic 0		5		5	μA	

AC ELECTRICAL CHARACTERISTICS

($V_{SS} = +5V \pm 5\%$; $V_{DD} = -12V \pm 5\%$; $0°C \leq T_A \leq 70°C$ unless otherwise noted)

	PARAMETER	MK 4006P-6 MIN	MK 4006P-6 MAX	MK 4008P-6 MIN	MK 4008P-6 MAX	UNITS	NOTES
t_{ACCESS}	Read Access Time (Fig. 1 & 1-A)		400		500	ns	Note 2
t_{CE}	Chip Enable Time (Fig. 1A & 5)		350		450	ns	Note 2
t_{CD}	Chip Disable Time (Fig. 1A & 5)		350		450	ns	
C_I	Input Capacitance, Any Input		5.0		5.0	pF	$T_A=25°C$; $V_I=V_{SS}$; f=1MHz
C_O	Output Capacitance		10		10	pF	$T_A=25°C$; $V_O=V_{SS}-5V$; f=1MHz
C_{DD}	V_{DD} Capacitance		75		75	pF	$T_A = 25°C$; Note 6

NOTES:

(1) Applies to MK 4006-6 and MK 4008-6 only.

(2) Measurement Criteria: Input voltage swing, all inputs: 0.8V to $V_{SS} - 1$
Input rise and fall times: 20 ns
Measurement point on input signals: +1.5V above ground
Measurement point on output signal: +60 mV above ground, using a load circuit of a 200 ohm resistor in parallel with a 100 pF capacitance connected to ground.

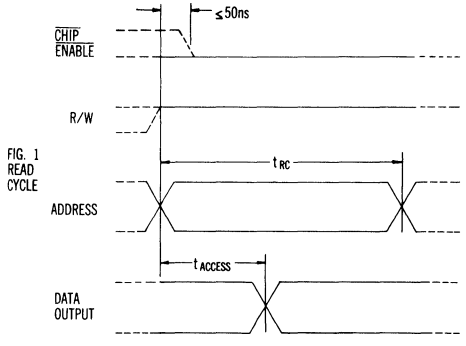
(3) t_{RDLY} is the time between refresh cycles for a given row address.

(4) The rise time of V_{DD} must not be faster than 20 ns.

(5) Steady-state values. (Refer to Fig. 1A for clarification)

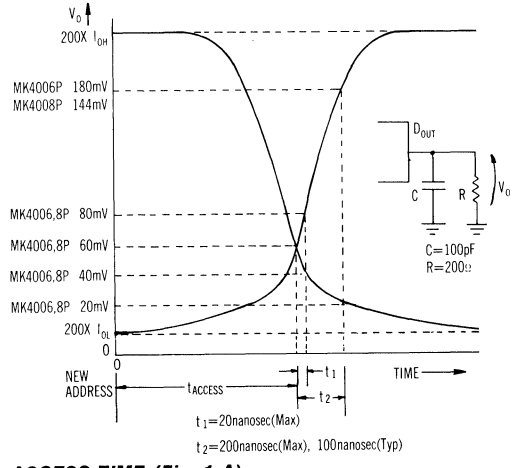
(6) Average capacitance of the V_{DD} terminal relative to the V_{SS} terminal. Measured by switching the V_{DD} terminal from OV to −12V with an applied $V_{SS} = 5V$. Peak I_{DD} is observed and the circuit replaced by a capacitance which yields the same peak current as the circuit under test.

TIMING (Note 2)



READING (Fig. 1)

Reading is accomplished with the Read/Write input held high. Data output directly follows the application of an address. As long as the address is unchanged and the chip enabled, data output will remain valid until the next refresh cycle. Input addresses can be changed as soon as output data is accessed. Any address can be applied repetitively without degrading stored data, providing that the refresh period of 2 ms is observed.



ACCESS TIME (Fig. 1-A)

Figure 1-A illustrates the measurement of access time after application of new address for the MK 4006 P and the MK 4008 P.

TIMING
(Note 2)

WRITING (Fig. 2)

Writing is accomplished by bringing the Read/Write input low with valid data present at the data input and the Chip-Enable input low (chip enabled). Following the return of the Read/Write line to a high state, new address and input data can be applied. If a read-after-write operation is desired, valid data will appear at the output within one read access time following the rising edge of the Write Pulse. Read-modify-write operation is easily achieved by delaying the Write Pulse until data has been read and modification is complete.

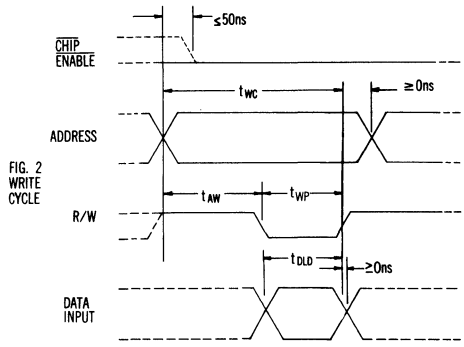


FIG. 2 WRITE CYCLE

REFRESHING (Figs. 2 & 3)

The dynamic memory cell employed in the MK 4006 P and MK 4008 P will not store data indefinitely. Stored data must be written back into the cell at least once every 2 ms. Rewriting is accomplished internally without the need to reapply external data. This rewriting operation is called *refreshing.*

Refreshing of the MK 4006 P and MK 4008 P is accomplished during both *write cycles* and *refresh cycles.* During a write cycle the state of the Row Address (R_1-R_5) determines which of the 32 memory matrix rows will be internally refreshed. An entire row (32 bits) is refreshed during one write cycle. Since it is difficult in practice to assure that each of the 32 possible R addresses is associated with a write cycle in every 2 ms period, a separate refresh cycle is normally employed.

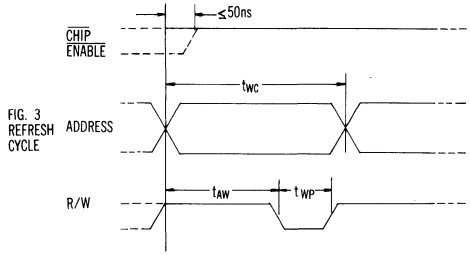


FIG. 3 REFRESH CYCLE

The refresh cycle is identical to the write cycle except that the chip is disabled while the Read/Write line is pulsed. Disabling the chip removes the data output and prevents data at the data input from being written into the memory. An entire refresh cycle consists of 32 address changes and associated write pulses, involving a total time of approximately 20 microseconds.

STANDBY MODE (Fig. 4)

Power dissipation of the MK 4006-6 P and MK 4008-6 P can be reduced below 50 mW without loss of stored data by lowering the V_{DD} supply voltage to system ground (V_{SS}-5V). Figure 4 illustrates the proper input conditions that should be observed when reducing V_{DD}. If the standby mode is maintained as long as 2 milliseconds, the V_{DD} supply should be returned to −12V and a refresh cycle initiated. Read or write cycles can commence immediately following the return of V_{DD} to −12V.

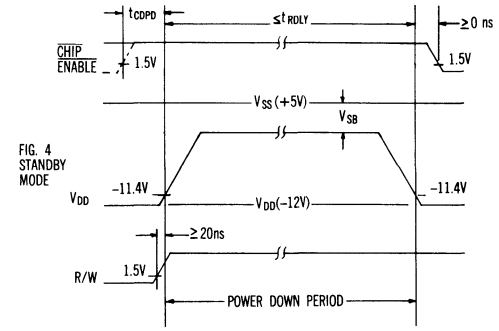


FIG. 4 STANDBY MODE

TIMING
(Note 2)

CHIP ENABLING (Fig. 5)[1]

The negative-going $\overline{CE}$ enables the chip, and output data becomes valid within t_{CE} time. Return of the $\overline{CE}$ input to logic 1 disables the chip; data out remains for t_{CD} time.

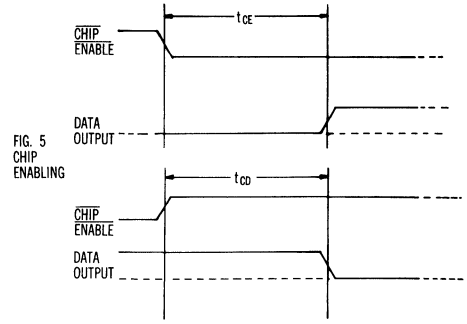


FIG. 5 CHIP ENABLING

TESTING CONSIDERATIONS

For a complete discussion of testing this memory, see Mostek's Applications Note AN-103.

The functional diagram (Fig. 6) indicates signal flow for selected row and column.

A simplified listing of functional tests is shown in Table 1. (high = Logic 1; low = Logic 0)

Tests are performed in an address sequence which requires the maximum number of changes in the row and column decoders between addresses. Addressing Rows 0 through 31 is accomplished by using the binary equivalent of the row address. The internal organization of the memory matrix requires the logic shown in Fig. 7 for column addresses; this logic provides the necessary conversion from inary equivalent to column address.

Fig. 6

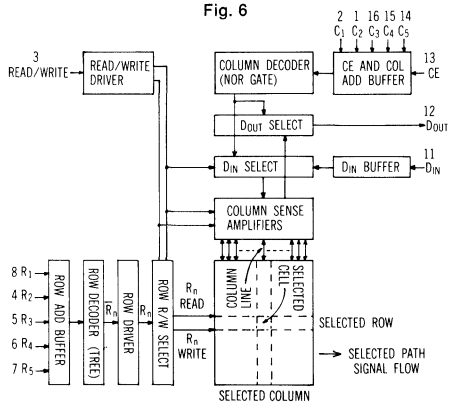


Fig. 7

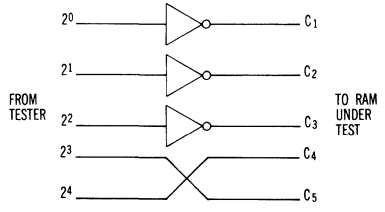


TABLE 1: FUNCTIONAL TESTS (SIMPLIFIED)

TEST DESC.	TEST SEQ.	OPER.	CHIP ENABLE	DATA INPUT	COMPARE DATA
Bit & Decoder Test[1]	First	Write	E	Parity	
	Next	Read	E		Parity
Column Shorts & No Write During Disable	First	Write	E	V-Bar	
	Next	Write	D	$\overline{\text{V-Bar}}$	
	Next	Read	E		V-Bar
Row Shorts, No Read During Disable, & Max. Power	First	Write	E	H-Bar	
	Next	Read	D	1	0
	Next	Read	E	0	H-Bar
Access Time, Refresh, Write Cycle, & Standby[1]	First	Write, Write	E	V-Bar, $\overline{\text{V-Bar}}$	
	Next	Delay	D	0	
	Next	Read	E		$\overline{\text{V-Bar}}$
Disturb Test	First	Write Row of 1's	E	1	
	Next	Write Adj. Row with 0's	E	0	
	Next	Continue Writing Same Row for Max. Refresh Delay	E	0	
	Next	Read original Row of 1's	E		1

1. Test performed as shown and repeated with complementary data.

ORDERING INFORMATION

MK 4006 P–6 1024x1 RAM/w/400 ns access time with power down
MK 4008 P–6 1024x1 RAM/w/500 ns access time with power down

APPLICATION

SENSE AMPLIFIERS FOR MK 4006/4008 RAM's

Since the interface circuitry used to convert memory signals to system logic levels strongly influences system access times, this circuitry should always be designed to meet the speed and cost requirements of the particular application.

Fig. 1-A (See "Timing") is shown to assist in the design of such amplifiers. This figure shows output voltage (across a specified load) vs. time from application of new address with several points indicated where specified voltage levels are referenced to specific times. Although all the various access times vs. output current levels cannot be shown, a few guidelines are given for interpolation between the specified points.

In Fig. 1-A, the two points at t_{access} + 20 nsec give the minimum "1" level and the maximum "0" level for this particular time (80 mV and 40 mV respectively). At t_{access} + 200 nsec, voltage levels are specified for the 90% and 10% points of the minimum "1" and maximum "0" levels.

INTERPOLATION

These interpolation guidelines are selected to give the designer a high level of confidence in his sense amplifier design.

From O to 1: This portion of the access curve can be estimated by two linear portions: (1) from the 60 mV to the 80 mV level; and (2) from the 80 mV level to 180/144 mV level.

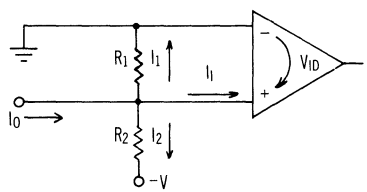
From 1 to O: This portion of the access curve can be estimated by a semi-logarithmic plot decreasing 20 mV for each decade or 10 nsec of time added to t_{access}, with the end points being 60 mV at 2 nsec and 20 mV at 200 nsec.

EXAMPLE: Let us consider how this data can be used in a sense amplifier design utilizing the 75107/108 Dual-Line-Receiver-and-Driver.

The manufacturer's data sheet for this circuit shows us that at strobe time, three conditions of the line receiver can exist: (1) the input voltage differential can be more positive than 25 mV, resulting in a logic 1 at the output (Input differential voltage is referenced to the inverting terminal); (2) the input differential can be more negative than 25 mV, resulting in a logic O at the output; (3) the input differential is less than 25 mV (absolute value), which will result in an output of an undetermined state. In other words, the line receiver has a 50 mV "window" centered around zero, and a signal must fall outside this window to provide reliable information at the output.

The standard configuration for using the 75107/108 as a sense amp is shown in Fig. 8 with the voltage and current conventions used in this analysis.

FIG. 8: Illustrating use of 75107/108 Line Receivers as sense amplifiers for the MK 4006/4008 P.



From the worst-case access at the *chip* level, one can use the interpolation technique described above to determine maximum "O" current level [I_{OLC}(MAX)] and the minimum "1" current level [I_{OH}(MIN)].

However, to use a worst-case approach to this design, in addition to the chip's characteristics, one must include in the "O" level current the effect of leakage from all outputs that are wired together. Also the input currents required by the 75107/108 (75 mA and 10 mA) must be included. Let us call this I_{OLT}(MAX):

$$I_{OLT}(MAX) = I_{OLC}(MAX) + (N\text{-}1)\ (5\ \mu A) \quad [1]$$

where N = number of outputs wired together

Using the maximum zero level at the line receiver input ($V_{ID} \leq -25mV = V_{ID}^{-}$), the following equation is derived:

$$I_{OLT}(MAX) = I_1 - I_2 + I_{IL}(MIN)$$
$$\text{and } I_{IL}(MIN) = O\ \mu A \quad [2]$$

therefore:

$$I_{OLT}(MAX) = \frac{V_{ID}^{-}}{R1} + \frac{V + V_{ID}^{-}}{R2} \quad [3]$$

Using the minimum "1" level at the line receiver input ($V_{ID} \geq +25\ mV = V_{ID}^{+}$), the equation becomes

$$I_{OH}(MIN) = I_1 - I_2 + I_{IH}(MAX) \quad [4]$$
$$\text{and } I_{IH}(MAX) = 75\ \mu A$$

$$I_{OH}(MIN) = \frac{V_{ID}^{+}}{R1} + \frac{V + V_{ID}^{+}}{R2} + 75\ \mu A \quad [5]$$

Solving these equations ([3] and [5]) simultaneously yields R1 and R2.

As an example, assume a memory system with 4 outputs wired-ORed to a sense amplifier, requiring a chip access time of 460 nsec. Then the associated current and resistor values are:

$$I_{OLT}(MAX) = 152.3\ \mu A + 3\ (5\ \mu A) = 167.3\ \mu A$$
$$I_{OH}(MIN) = 511.12\ \mu A$$

Therefore:

$$R1 = 190\ \Omega$$
$$R2 = 16.5\ K\Omega$$

Sense amplifiers vary from the very fast, low-threshold types to the slower, high-threshold kind. The ideal choice will depend on the application. Fig. 1-A and the guidelines in this note are intended to help the designer tailor his sense amplifier design to meet the speed and cost requirements of his particular application.

It should also be noted that a portion of the output current from the memory chip is used to charge the capacitance on the data output. If the output impedance differs greatly from the specified load, this current must also be calculated.

MOSTEK

256x1 BIT DYNAMIC RAM

MK 4007 P/N

FEATURES

- ☐ Versatile RAM can replace any existing 1101-type 256x1 MOS RAM pin for pin.
- ☐ Ion-implanted for superior performance.
- ☐ **Lower power dissipation:** TOTAL 370 mW max over entire temperature range.
- ☐ **Faster access time:** Typically 525 ns with V_D and V_{DD} at −9V.
- ☐ **Less temperature-sensitive:** specified over entire AMBIENT temperature range 0° to 75°C.
- ☐ **Tight control of output sink current capabilities:** made possible by use of depletion-mode transistors.
- ☐ **No restrictions** on address input sequence, skew, or rise and fall times.
- ☐ Full DTL/TTL compatibility.
- ☐ Wide power supply range: +5V; −6.5 to −15V.

APPLICATIONS

Ideal for small buffer storage requiring low cost, superior performance, and bipolar compatibility, such as:

- ☐ Scratchpad memories
- ☐ Data link buffers
- ☐ Key-to-tape buffers
- ☐ Tape-to-printer buffers
- ☐ Editing memories

DESCRIPTION

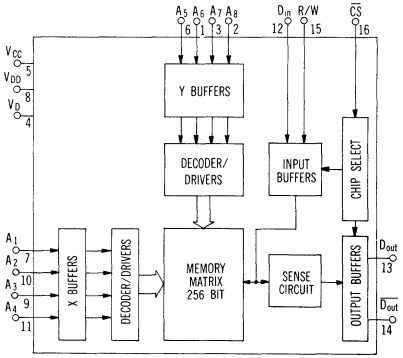
Ion-implantation processes used in manufacturing the Mostek MK 4007 P Random Access MOS Memory result in a low-cost device with performance exceeding other industry types over the entire temperature and voltage supply ranges. It may be used to replace any existing 1101 type RAM pin for pin.

The depletion-load ion-implantation technique allows the fabrication of both depletion and enhancement mode transistors on the same chip. The result is not only superior operating characteristics within the region usually specified for devices of this type, but also wider operational areas without severe performance degradation. For example, while specifications for this device are given for V_D and V_{DD} from −7 to −13.2V, V_D and V_{DD} may actually range from −6.5 to −15V (see DC Operating Conditions and Figure 1). Access times are improved (See Figure 2); power dissipation is reduced (see Figure 3) and output sink current capabilities are improved (see Figure 4). The device is less temperature-dependent (see Figures 5 and 6) and is specified over the entire ambient temperature range of 0° to 75°C.

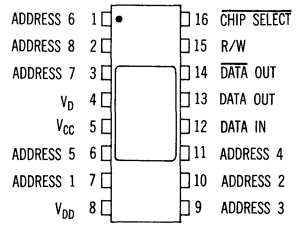
The ion-implantation process also makes the MK 4007 P RAM fully TTL/DTL compatible at all inputs and outputs.

The 4007 P is a static memory, requiring no clocks or refreshing. Data is written into the address location by applying a logic "1" to the R/W input. Addressing the desired location, with the chip enabled and R/W at logic "0", provides a nondestructive read-out (NDRO) of true and complement data. A "Chip Select" allows output buffers to be open-circuited during disable time for wire ORing. All inputs are protected against static charge accumulation.

FUNCTIONAL DIAGRAM



PIN CONNECTIONS



ABSOLUTE MAXIMUM RATINGS

Voltage on Any Terminal Relative to V_{CC} . . . . . +0.3V to −25V
Operating Temperature Range (Ambient) . . . . . 0°C to +75°C
Storage Temperature Range (Ambient) Ceramic . . . . . −65°C to +150°C
Storage Temperature Range (Ambient) Plastic . . . . . −55°C to 125°C

DC OPERATING CONDITIONS

(Ambient Temperature Range: 0°C to +75°C)

	PARAMETER		MIN	TYP	MAX	UNITS	COMMENTS
POWER	V_{CC}	Supply Voltage	4.75	5.0	5.25	V	
	V_{DD}	Supply Voltage	−6.5	−9.0	−15.0	V	See Fig. 1 for
	V_D	Supply Voltage	−6.5	−9.0	−15.0	V	V_D, V_{DD} differential
INPUTS	V_{IL}	Logic "0" Voltage, any input		0	+0.8	V	
	V_{IH}	Logic "1" Voltage, any input	V_{CC} −2.0	V_{CC}	V_{CC}+0.3	V	

ELECTRICAL CHARACTERISTICS

(Ambient Temperature Range: 0°C to +75°C. V_{CC} = +5 V ±5%;
$V_D = V_{DD}$ = −7 V to −13.2 V, unless otherwise specified.)

	PARAMETER		MIN	TYP(1)	MAX	UNITS	CONDITIONS
POWER	I_D	Supply Current. V_D		8.0	16	mA	$V_D = V_{DD}$ = −9V ± 5% Outputs open-circuited.
	I_{DD}	Supply Current, V_{DD}		4.0	9	mA	
	P_D	Power Dissipation, Total		170	370	mW	
	I_D	Supply Current. V_D			19	mA	$V_D = V_{DD}$ = −13.2 V V_{CC} = +5.25 V Outputs open-circuited.
	I_{DD}	Supply Current, V_{DD}			10	mA	
	P_D	Power Dissipation, Total			535	mW	
	P_{SDBY}	Power Dissipation, Standby		30	75	mW	$V_D = V_{CC}$; V_{DD} = −9V ±5%
INPUTS	$I_{I(L)}$	Input Leakage Current			1.0	μA	V_{IN} = 0 V, T_A = 25°C
	C_{IN}	Input Capacitance, Any Logic Input		7	10	pF	T_A = 25°C, F. meas. = 1 MHz; Tested input = V_{CC}
	$C_{V(D)}$	Capacitance, V_D Power Supply		35		pF	
OUTPUTS	I_{OL}	Output Current, Logic "0"	3.2	5.6		mA	V_O = +0.40 V
	I_{OH}	Output Current, Logic "1"	−1.0	−4.2		mA	V_O = +2.6 V
	I_{OLC}	Output Clamp Current, Logic "0"			8.0	mA	V_O = −1.0 V
	$I_{O(L)}$	Output Leakage Current			1.0	μA	$V_O = V_{CC}$ −5V; $\overline{CS}$ = Logic 1; T_A = 25°C.
	C_{OUT}	Output Capacitance		7	10	pF	T_A = 25°C; F meas. = 1 MHz; $V_O = V_{CC}$

NOTES:

(1) Typical values at V_{CC} = +5 V, $V_D = V_{DD}$ = −9.0 V*, T_A = 25°C.
(*Except Standby Power)

TIMING

(Ambient Temperature Range: 0°C to 75°C; $V_{CC} = +5$ V $\pm 5\%$; $V_D = V_{DD} = -7$V to -13.2 V, unless otherwise specified. See Notes 1 and 2.)

		PARAMETER	MIN	TYP	MAX	UNITS	
OPERATING CONDITIONS	t_{wc}	Write Cycle Time	700			ns	
	t_{wd}	Write Set-up Delay	300			ns	
	t_{wp}	Write Pulse Width	400			ns	
	t_{did}	Data Lead Time	300			ns	
	t_{dig}	Data Lag Time	0			ns	
	t_{cw}	Chip Select Pulse Width	400			ns	
DYNAMIC CHAR.	t_{ACC}	Access Time		525	900	ns	$V_D = V_{DD} = -9$V $\pm 5\%$.
	t_{RC}	Read Cycle Time			800	ns	(See Note 3.)
	t_{ACC}	Access Time			1.0	μs	$V_D = V_{DD} = -7$V to -13.2V.
	t_{RC}	Read Cycle Time			900	ns	(See Note 3.)
	t_{OH}	Data Output Hold Time	100			ns	
	t_{CSE}	Chip-Select-to-Output Enable			300	ns	
	t_{CSD}	Chip-Select-to-Output Disable			300	ns	

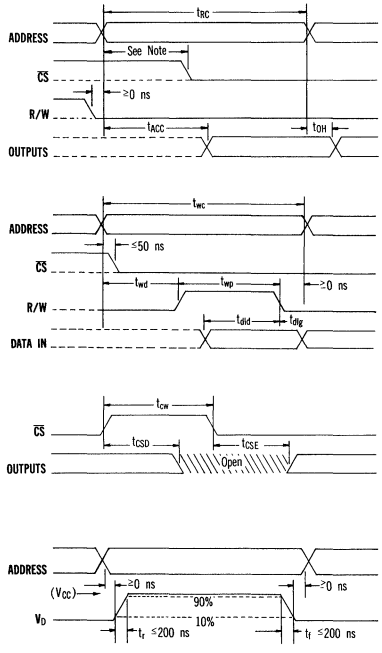
NOTES:

(1) All measurements to the 1.5 V level; inputs for test are 0 to 5 V and $\leq$10 ns rise and fall times; output is loaded with 1 TTL and approx. 20 pF.

(2) R/W should be brought to logical "0" whenever address bits are changed; however, there are no restrictions on rise and fall times of address bits, nor on the sequence (or skew) of address bit changes.

(3) Read Cycle may be "pipe-lined," i.e., the minimum hold time (t_{OH}) may be subtracted from the maximum access time (t_{ACC}).

TIMING



READ CYCLE

Reading is accomplished with R/W (Read/Write) and $\overline{CS}$ (Chip Select) at logical "0."

NOTE: $\overline{CS}$ logical "1" overlap time shown must be 300 ns (max t_{CSE}) less than the desired access time; e.g., if desired access time $t_{ACC} = 1.2$ μs, then $\overline{CS}$ should go to logical "0" no later than 900 ns following address change.

WRITE CYCLE

Writing is accomplished with R/W at logical "1" and $\overline{CS}$ at logical "0." $\overline{CS}$ at logical "1" may overlap the address change as much as 50 ns. R/W may be taken to logical "0" coincidentally with an address change, but should not overlap an address change while in the logical "1" state.

CHIP SELECT

$\overline{\text{Chip Select}}$ at logical "1" causes the normal push-pull output buffers to be open-circuited for purposes of wire-ORing. The $\overline{\text{Chip Select}}$ may be used to access the memory at a faster rate by maintaining a constant address and selecting individual chips with the $\overline{\text{Chip Select}}$ input.

POWER SWITCHING

During standby operation the MK 4007 P will dissipate only 30 mW of power (typically) if the peripheral power supply, V_D, is reduced to V_{CC}. The R/W input may be maintained at logical "0" or "1"; however, if R/W is at logical "1," $\overline{\text{Chip Select}}$ should also be logical "1" (to disable chip during standby operation). With the return of power, either read or write cycles may commence as described above.

TYPICAL PERFORMANCE CURVES

FIG. 1: POWER SUPPLY OPERATING REGION & DIFFERENTIAL

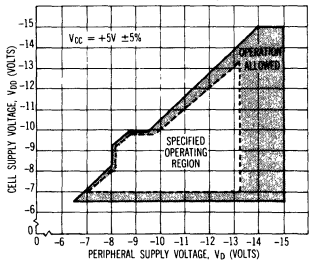


FIG. 2: ACCESS TIME VS SUPPLY VOLTAGE, (V_D)

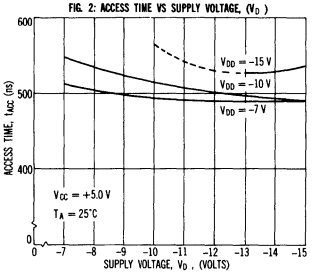


FIG. 3: TOTAL POWER DISSIPATION, (P_D), VS SUPPLY VOLTAGE, (V_D and V_{DD})

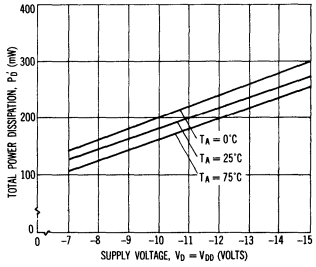


FIG. 4: OUTPUT CURRENT VS OUTPUT VOLTAGE

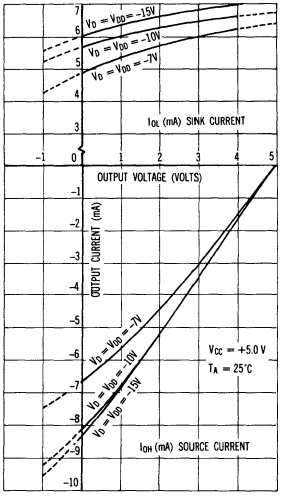


FIG. 5: OUTPUT CURRENT VS AMBIENT TEMPERATURE

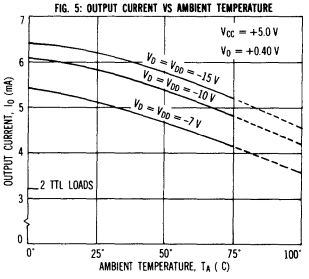


FIG. 6: WORST-CASE ACCESS TIME VS SUPPLY VOLTAGE (At Various Capacitances and Ambient Temperatures)

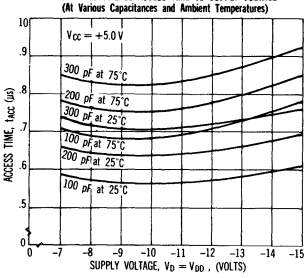


FIG. 7: SUPPLY CURRENT, (I_D and I_{DD}), VS SUPPLY VOLTAGE (V_D and V_{DD})

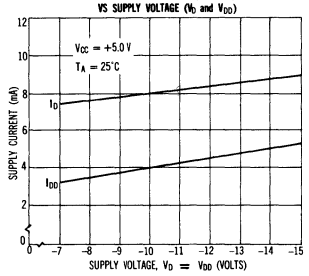
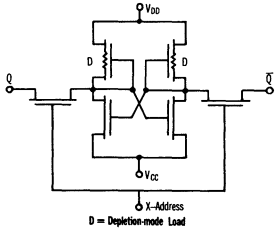


FIG. 8: MK 4007 P MEMORY CELL



D = Depletion-mode Load

MOSTEK

256x1 BIT DYNAMIC RAM

MK 4007 P/N- 4

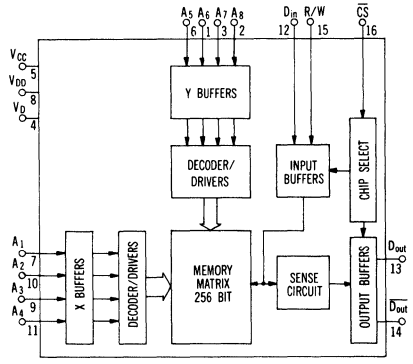
FEATURES

- Low-cost 256x1 RAM in 16-pin package.
- Identical with Mostek's MK 4007 P in all specifications except output current

DESCRIPTION

This economical version of Mostek's 256x1 bit RAM is identical with the MK 4007 P in all electrical characteristics except output current. Performance, operating conditions, timing characteristics, package, and all other specifications are identical with the MK 4007 P. See the MK 4007 P Data Sheet for additional information.

FUNCTIONAL DIAGRAM



ELECTRICAL CHARACTERISTICS

(Ambient Temperature Range: 0°C to +75°C. V_{CC} = +5 V ±5%; V_D = V_{DD} = −7 V to −13.2 V, unless otherwise specified.)

		PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
POWER	I_D I_{DD} P_D	Supply Current, V_D Supply Current, V_{DD} Power Dissipation, Total		8.0 4.0 170	16 9 370	mA mA mW	V_D = V_{DD} = −9 V ±5% Outputs open-circuited.
	I_D I_{DD} P_D	Supply Current, V_D Supply Current, V_{DD} Power Dissipation, Total			19 10 535	mA mA mW	V_D = V_{DD} = −13.2 V V_{CC} = +5.25 V Outputs open-circuited.
	P_{SDBY}	Power Dissipation, Standby		30	75	mW	V_D = V_{CC}; V_{DD} = −9V ±5%
INPUTS	$I_{I(L)}$	Input Leakage Current			1.0	µA	V_{IN} = O V, T_A = 25°C
	C_{IN} $C_{V(D)}$	Input Capacitance, Any Logic Input Capacitance, V_D Power Supply		7 35	10	pF pF	T_A = 25°C, F. Meas. = 1 MHz; Tested input = V_{CC}
OUTPUTS	I_{OL} I_{OH} I_{OLC}	Output Current, Logic "0": @ T_A = 25°C Output Current, Logic "0": @ T_A = 70°C Output Current, Logic "1" Output Clamp Current, Logic "0"	3.0 2.0 −1.0	5.6 −4.2	 8.0	mA mA mA mA	V_O = +0.40 V V_O = +0.40 V V_O = +2.6 V V_O = −1.0 V V_{CC} = 5.0 V ±5%; V_D = V_{DD} = −9.0 V ±10%
	$I_{O(L)}$	Output Leakage Current			1.0	µA	V_O = V_{CC} −5V; $\overline{CS}$ = Logic 1; T_A = 25°C.
	C_{OUT}	Output Capacitance		7	10	pF	T_A = 25°C; F meas. = 1 MHz; V_O = V_{CC}

NOTES:

(1) Typical values at V_{CC} = +5 V, V_D = V_{DD} = −9.0 V*, T_A = 25°C.
(*Except Standby Power)

MOSTEK

1024 x 1 BIT STATIC RAM

MK 4102N Series

FEATURES

- ☐ Industry standard 1024 bit static RAM
- ☐ Totally static operation:
  No clocks or refreshing required
- ☐ Cycle Time/Access Time
  MK 4102/-12 1μS max
  MK 4102-1/-11 450nS max
- ☐ All pins TTL compatible
- ☐ Single +5 volt power supply
- ☐ Power Dissipation
  MK 4102-12/-11 160 mW max
  MK 4102/-1 370 mW max
- ☐ Three-state output
- ☐ Standard 16 pin DIP

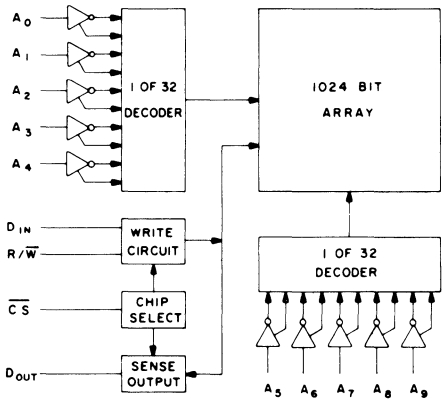
DESCRIPTION

The MOSTEK MK 4102 is a fully static 1024 x 1 bit random access memory, fabricated with MOSTEK's standard N-channel silicon gate process. This technology makes the MK 4102 a highly manufactureable MOS memory, while maintaining high performance and circuit reliability. The pin connections and functional operation are similar to MOSTEK's popular 1024 x 1 bit dynamic RAM series, the MK 4006/MK 4008.

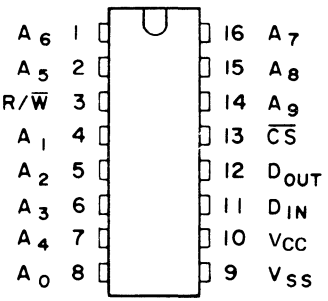
The MK 4102 has many system oriented features including TTL compatability on all pins. All inputs are specified at 2.2 volts V_{IH}, which guarantees a minimum noise margin of 200 mV when used with standard TTL logic. The three-state output, which is controlled by the Chip Select ($\overline{CS}$) input, permits the construction of large memory arrays with wire "OR"ed outputs. The device operates from a single +5 volt power supply.

The MK 4102 family of devices are pin and performance compatable with the popular industry standard types 2102A/2102AL 1K static RAMs. The static operation of the MK 4102 means no clocks or refreshing and associated external control circuitry are required.

FUNCTIONAL DIAGRAM



PIN CONNECTIONS



PIN NAMES

A0-A9	Address Inputs	D_{IN}	Data In
$\overline{R/W}$	Read/Write Input	V_{CC}	Power (+5V)
$\overline{CS}$	Chip Select	V_{SS}	Ground
D_{OUT}	Data Output		

ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to V_{SS} ..... −.5V to 7V

Operating Temperature (Ambient) T_A ..... 0°C to +70°C

Storage Temperature (Ambient) ..... −55°C to +125°C

Power Dissipation ..... 1 Watt

RECOMMENDED DC OPERATING CONDITIONS ($0°C \leq T_A \leq 70°C$)

	PARAMETER	MIN	MAX	UNITS	NOTES
V_{CC}	Supply Voltage	4.75	5.25	volts	
V_{SS}	Supply Voltage	0	0	volts	
V_{IH}	Input Voltage, Logic 1	2.2	5.25	volts	
V_{IL}	Input Voltage, Logic 0	0	.65	volts	

DC ELECTRICAL CHARACTERISTICS ($V_{CC} = +5V \pm 5\%$, $V_{SS} = OV$, $0°C \leq T_A \leq 70°C$)

	PARAMETER	MK 4102-11 MK 4102-12		MK 4102 MK 4102-1		UNITS	NOTES
		MIN	MAX	MIN	MAX		
I_{CC}	Supply Current		30		70	mA	output open
$I_{I(L)}$	Input Leakage Current		10		10	μA	V_{IN} = OV to 5.25V (2)
$I_{O(L)}$	Output Leakage Current		10		10	μA	V_O = 0.4V to 5.25V (3)
V_{OH}	Output Voltage, Logic 1	2.2		2.2		volts	$I_{OH} = -100\mu A$
V_{OL}	Output Voltage, Logic 0		.4		.4	volts	$I_{OL} = +3.2mA$

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (1) ($0°C \leq T_A \leq 70°C$)

	PARAMETER	MK 4102 MK 4102-12		MK 4102-1 MK 4102-11		UNITS	NOTES
		MIN	MAX	MIN	MAX		
t_{RC}	Read Cycle Time	1000		450		ns	
t_{WC}	Write Cycle Time	1000		450		ns	
t_{WP}	Write Pulse Width	750		200		ns	
t_{AW}	Address to Write Pulse Delay	200		20		ns	
t_{DW}	Data Set-Up Time	800		200		ns	
t_{DH}	Data Hold Time	100		0		ns	
t_{CW}	Chip Select to Write	800		300		ns	
t_{WR}	Write Recovery Time (Address Hold Time)	50		0		ns	
t_{ACC}	Access Time (Ref Add)		1000		450	ns	
t_{CO}	$\overline{CS}$ (low) Access Time		300		200	ns	4
t_{OH1}	Output Turn-Off Delay Referenced to Address	50		50		ns	5
t_{OH2}	Output Turn-off Delay Referenced to $\overline{CS}$ (high)	0		0		ns	6

* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 5%, V_{SS} = OV, 0°C ≤ T_A ≤ 70°C)

	PARAMETER	MIN	MAX	UNITS	NOTES
C_I	Input Capacitance (Any Input)		6	pF	7
C_O	Output Capacitance		10	pF	7

NOTES:

(1) AC Test Conditions: Input voltage swing = + .4 to 2.2v; V_{IH} or V_{IL} and V_{OH} or V_{OL} are used as references for timing; $t_R = t_F$ = 5ns, Output load —1 standard TTL load and C_L = 100 pF

(2) $V_{SS} = V_{CC} = OV$

(3) Output Disabled

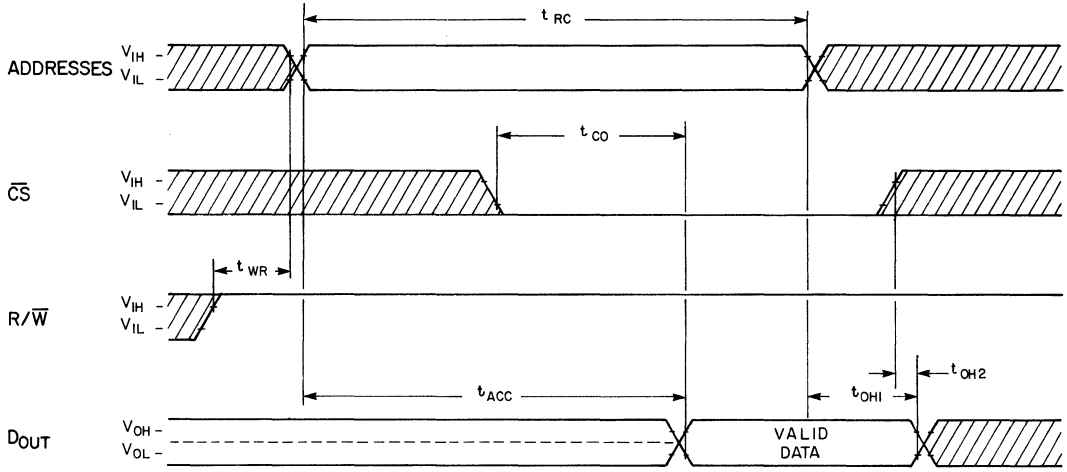
(4) Assumes that addresses have been valid for ≥ $t_{ACC} - t_{CO}$ nsec

(5) Chip Selected

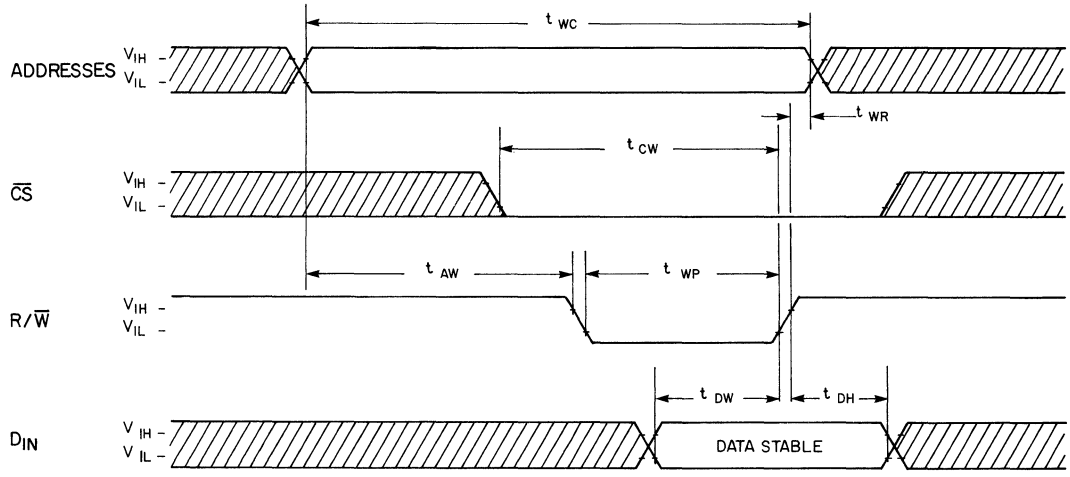
(6) Addresses valid when chip select goes active

(7) f = 1MHz V_{IN} = OV @ 25°C

READ CYCLE



WRITE CYCLE



4K DYNAMIC RAMs

MOSTEK is the recognized leader in 4096-bit Random Access Memory technology. All MOSTEK 4K dynamic RAMs are packaged in the industry standard 16-pin configuration providing high system bit densities and compatibility with widely available automated testing and insertion equipment. A wide choice of speed, power, and temperature ranges are available. New introductions include a low standby power version of the MK 4027 called MK 4227 which features 100 μA (max.) standby current, and the addition of extended temperature range MK 4096's designated MK 4096P-77/86 and 85. These are also available processed to MIL-STD-883 Class B.

MOSTEK

4096 X1-BIT DYNAMIC RAM

MK4027(P/N)-2/3/4

FEATURES

- ☐ Industry standard 16-pin DIP (MK 4096) configuration
- ☐ 150ns access time, 320ns cycle (MK 4027-2)
  200ns access time, 375ns cycle (MK 4027-3)
  250ns access time, 375ns cycle (MK 4027-4)
- ☐ ±10% tolerance on all supplies (+12V, ±5V)
- ☐ Low Power: 462mW active (max)
  27mW standby (max)
- ☐ Improved performance with "gated $\overline{CAS}$", "$\overline{RAS}$ only" refresh and page mode capability
- ☐ All inputs are low capacitance and TTL compatible
- ☐ Input latches for addresses, chip select and data in
- ☐ Three-state TTL compatible output
- ☐ Output data latched and valid into next cycle

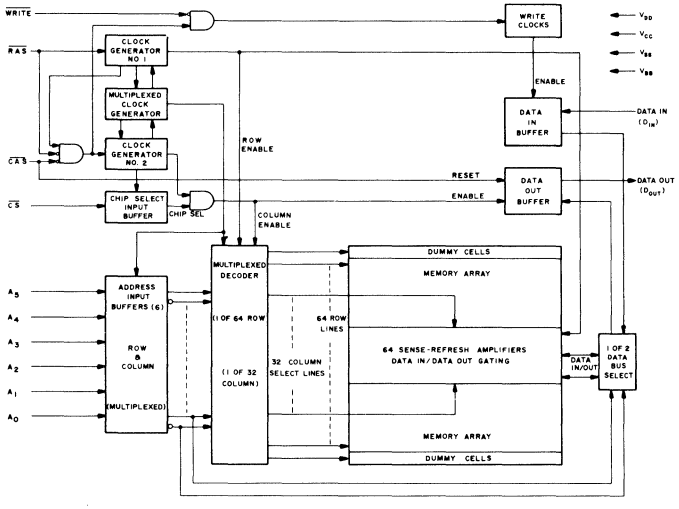
DESCRIPTION

The MK 4027 is a 4096 word by 1 bit MOS random access memory circuit fabricated with MOSTEK's N-channel silicon gate process. This process allows the MK 4027 to be a high performance state-of-the-art memory circuit that is manufacturable in high volume. The MK 4027 employs a single transistor storage cell utilizing a dynamic storage technique and dynamic control circuitry to achieve optimum performance with low power dissipation.

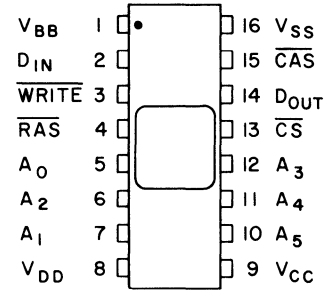
A unique multiplexing and latching technique for the address inputs permits the MK 4027 to be packaged in a standard 16-pin DIP on 0.3 in. centers. This package size provides high system-bit densities and is compatible with widely available automated testing and insertion equipment.

System oriented features include direct interfacing capability with TTL, only 6 very low capacitance address lines to drive, on-chip address and data registers which eliminates the need for interface registers, input logic levels selected to optimize noise immunity, and two chip select methods to allow the user to determine the appropriate speed/power characteristics of his memory system. The MK 4027 also incorporates several flexible operating modes. In addition to the usual read and write cycles, read-modify write, page-mode, and $\overline{RAS}$-only refresh cycles are available with the MK 4027. Page-mode timing is very useful in systems requiring Direct Memory Access (DMA) operation.

FUNCTIONAL DIAGRAM



PIN CONNECTIONS



PIN NAMES

A_0-A_5	ADDRESS INPUTS
$\overline{CAS}$	COLUMN ADDRESS STROBE
$\overline{CS}$	CHIP SELECT
D_{IN}	DATA IN
D_{OUT}	DATA OUT
$\overline{RAS}$	ROW ADDRESS STROBE
$\overline{WRITE}$	READ/WRITE INPUT
V_{BB}	POWER (−5V)
V_{CC}	POWER (+5V)
V_{DD}	POWER (+ 12V)
V_{SS}	GROUND

ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to V_{BB} ..... −0.5V to +20V
Voltage on V_{DD}, V_{CC} relative to V_{SS} ..... −1.0V to +15V
$V_{BB}-V_{SS}$ ($V_{DD}-V_{SS} > 0$) 0V
Operating temperature, T_A (Ambient) ..... 0°C to + 70°C
Storage temperature (Ambient)(Ceramic) ..... −65°C to + 150°C
Storage temperature (Ambient)(Plastic) ..... −55°C to + 125°C
Short Circuit Output Current 50mA
Power dissipation ..... 1 Watt

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS [4]

($0°C \leq T_A \leq 70°C$) [1]

	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{DD}	Supply Voltage	10.8	12.0	13.2	volts	2
V_{CC}	Supply Voltage	4.5V	5.0	5.5	volts	2,3
V_{SS}	Supply Voltage	0	0	0	volts	2
V_{BB}	Supply Voltage	−4.5	−5.0	−5.5	volts	2
V_{IHC}	Logic 1 Voltage, $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	2.4		7.0	volts	2
V_{IH}	Logic 1 Voltage, all inputs except $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	2.2		7.0	volts	2
V_{IL}	Logic 0 Voltage, all inputs	−1.0		.8	volts	2

DC ELECTRICAL CHARACTERISTICS [4]

($0°C \leq T_A \leq 70°C$)[1] (V_{DD} = 12.0V ± 10%; V_{CC} = 5.0V ± 10%; V_{SS} = 0V; V_{BB} = −5.0V ± 10%)

	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
I_{DD1}	Average V_{DD} Power Supply Current			35	mA	5
I_{DD2}	Standby V_{DD} Power Supply Current			2	mA	8
I_{DD3}	Average V_{DD} Power Supply Current during "$\overline{RAS}$ only" cycles			25	mA	
I_{CC}	V_{CC} Power Supply Current				mA	6
I_{BB}	Average V_{BB} Power Supply Current			150	μA	
$I_{I(L)}$	Input Leakage Current (any input)			10	μA	7
$I_{O(L)}$	Output Leakage Current			10	μA	8,9
V_{OH}	Output Logic 1 Voltage @ I_{OUT} = −5mA	2.4			volts	
V_{OL}	Output Logic 0 Voltage @ I_{OUT} = 3.2mA			0.4	volts	

NOTES

1. T_A is specified for operation at frequencies to $t_{RC} \geq t_{RC}$ (min). Operation at higher cycle rates with reduced ambient temperatures and higher power dissipation is permissible provided that all AC parameters are met. See figure 2 for derating curve.
2. All voltages referenced to V_{SS}.
3. Output voltage will swing from V_{SS} to V_{CC} when enabled, with no output load. For purposes of maintaining data in standby mode, V_{CC} may be reduced to V_{SS} without affecting refresh operations or data retention. However, the V_{OH} (min) specification is not guaranteed in this mode.
4. Several cycles are required after power-up before proper device operation is achieved. Any 8 cycles which perform refresh are adequate for this purpose.
5. Current is proportional to cycle rate, I_{DD1} (max) is measured at the cycle rate specified by t_{RC} (min). See figure 1 for I_{DD1} limits at other cycle rates.
6. I_{CC} depends on output loading. During readout of high level data V_{CC} is connected through a low impedance (135Ω typ) to Data Out. At all other times I_{CC} consists of leakage currents only.
7. All device pins at 0 volts except V_{BB} which is at −5 volts and the pin under test which is at +10 volts.
8. Output is disabled (high-impedance) and $\overline{RAS}$ and $\overline{CAS}$ are both at a logic 1. Transient stabilization is required prior to measurement of this parameter.
9. $0V \leq V_{OUT} \leq +10V$.
10. Effective capacitance is calculated from the equation:

$$C = \frac{\Delta Q}{\Delta V} \text{ with } \Delta V = 3 \text{ volts.}$$

11. A.C. measurements assume t_T = 5ns.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (4,11,17)

($0°C \leq T_A \leq 70°C$)[1] (V_{DD} = 12.0V ± 10%, V_{CC} = 5.0V ± 10%, V_{SS} = 0V, V_{BB} = −5.0V ± 10%)

	PARAMETER	MK 4027-2		MK 4027-3		MK 4027-4		UNITS	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX		
t_{RC}	Random read or write cycle time	320		375		375		ns	12
t_{RWC}	Read write cycle time	330		420		480		ns	12
t_{RAC}	Access time from row address strobe		150		200		250	ns	13,15
t_{CAC}	Access time from column address strobe		100		135		165	ns	14,15
t_{OFF}	Output buffer turn-off delay		40		50		60	ns	
t_{RP}	Row address strobe precharge time	100		120		120		ns	
t_{RAS}	Row address strobe pulse width	150	10,000	200	10,000	250	10,000	ns	
t_{RSH}	Row address strobe hold time	100		135		165		ns	
t_{CAS}	Column address strobe pulse width	100		135		165		ns	
t_{RCD}	Row to column strobe delay	20	50	25	65	35	85	ns	16
t_{ASR}	Row address set-up time	0		0		0		ns	
t_{RAH}	Row address hold time	20		25		35		ns	
t_{ASC}	Column address set-up time	−10		−10		−10		ns	
t_{CAH}	Column address hold time	45		55		75		ns	
t_{AR}	Column address hold time referenced to $\overline{RAS}$	95		120		160		ns	
t_{CSC}	Chip select set-up time	−10		−10		−10		ns	
t_{CH}	Chip select hold time	45		55		75		ns	
t_{CHR}	Chip select hold time referenced to $\overline{RAS}$	95		120		160		ns	
t_T	Transition time (rise and fall)	3	35	3	50	3	50	ns	17
t_{RCS}	Read command set-up time	0		0		0		ns	
t_{RCH}	Read command hold time	0		0		0		ns	
t_{WCH}	Write command hold time	45		55		75		ns	
t_{WCR}	Write command hold time referenced to $\overline{RAS}$	95		120		160		ns	
t_{WP}	Write command pulse width	45		55		75		ns	
t_{RWL}	Write command to row strobe lead time	50		70		85		ns	
t_{CWL}	Write command to column strobe lead time	50		70		85		ns	
t_{DS}	Data in set-up time	0		0		0		ns	18
t_{DH}	Data in hold time	45		55		75		ns	18
t_{DHR}	Data in hold time referenced to $\overline{RAS}$	95		120		160		ns	
t_{CRP}	Column to row strobe precharge time	0		0		0		ns	
t_{CP}	Column precharge time	60		80		110		ns	
t_{RFSH}	Refresh period		2		2		2	ms	
t_{WCS}	Write command set-up time	0		0		0			19
t_{CWD}	$\overline{CAS}$ to $\overline{WRITE}$ delay	60		80		90		ns	19
t_{RWD}	$\overline{RAS}$ to $\overline{WRITE}$ delay	110		145		175		ns	19
t_{DOH}	Data out hold time	10		10		10		μs	

Notes Continued

12. The specifications for t_{RC} (min) and t_{RWC} (min) are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \leq T_A \leq 70°C$) is assured. See figure 2 for derating curve.

13. Assumes that $t_{RCD} \leq t_{RCD}$ (max).

14. Assumes that $t_{RCD} \geq t_{RCD}$ (max).

15. Measured with a load circuit equivalent to 2 TTL loads and 100pF

16. Operation within the t_{RCD} (max) limit insures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.

17. V_{IHC} (min) or V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IHC} or V_{IH} and V_{IL}.

18. These parameters are referenced to $\overline{CAS}$ leading edge in random write cycles and to $\overline{WRITE}$ leading edge in delayed write or read-modify-write cycles.

19. t_{WCS}, t_{CWD}, and t_{RWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only: If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and Data Out will contain the data written into the selected cell. If $t_{CWD} \geq t_{CWD}$ (min) and $t_{RWD} \geq t_{RWD}$ (min), the cycle is a read-write cycle and Data Out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of Data Out (at access time) is indeterminate.

AC ELECTRICAL CHARACTERISTICS

($0°C \leq T_A \leq 70°C$) ($V_{DD} = 12.0V \pm 10\%$; $V_{SS} = 0V$; $V_{BB} = -5.0V \pm 10\%$)

	PARAMETER	TYP	MAX	UNITS	NOTES
C_{I1}	Input Capacitance (A_0-A_5), D_{IN}, $\overline{CS}$	4	5	pF	10
C_{I2}	Input Capacitance $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	8	10	pF	10
C_O	Output Capacitance (D_{OUT})	5	7	pF	8,10

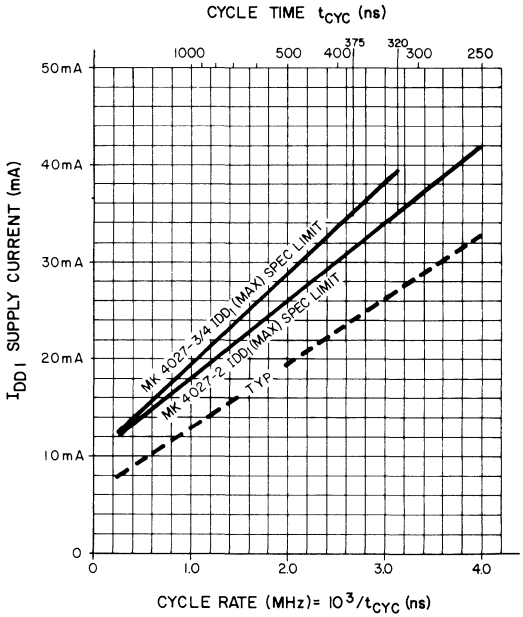


Figure 1. Maximum I_{DD1} versus cycle rate for device operation at extended frequencies.

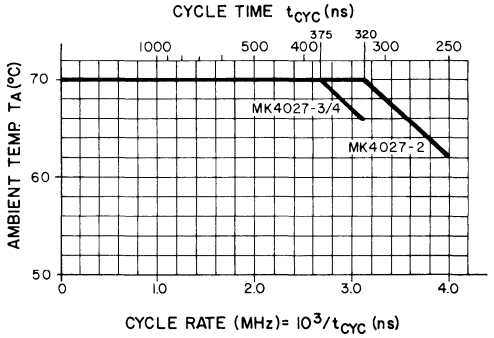
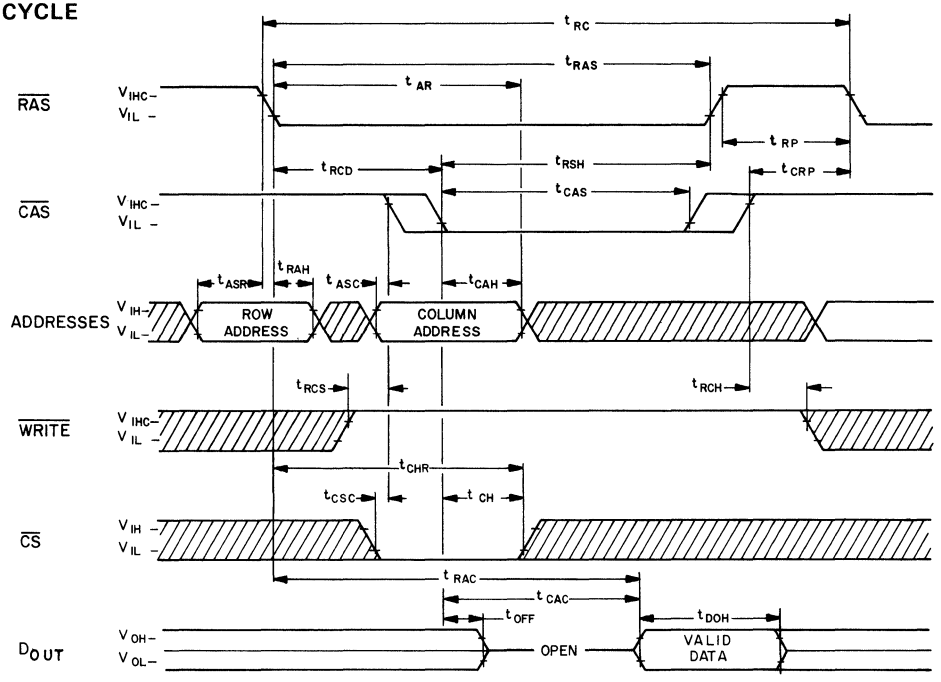
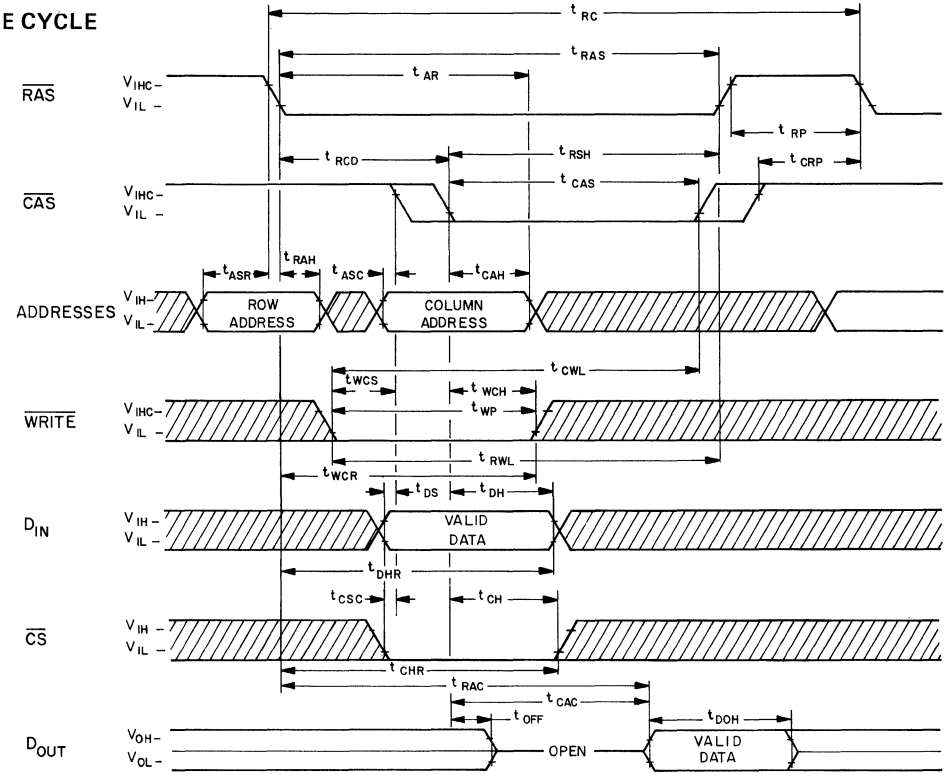


Figure 2. Maximum ambient temperature versus cycle rate for extended frequency operation.

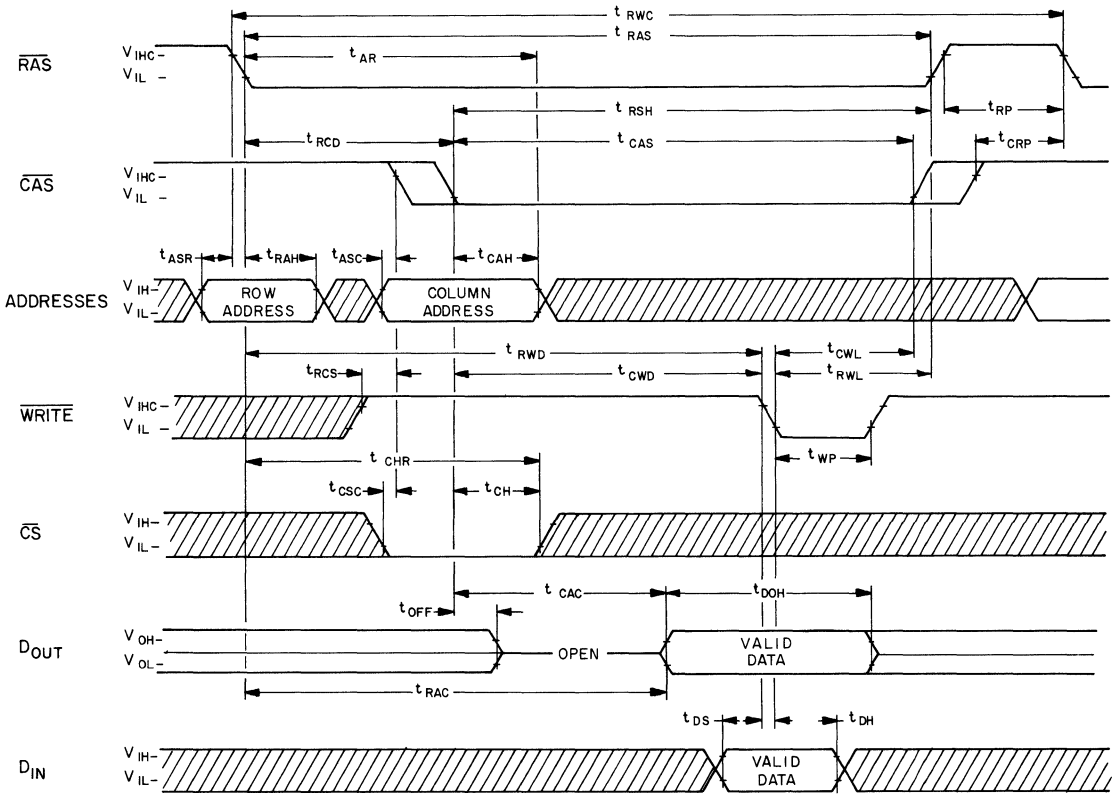
READ CYCLE



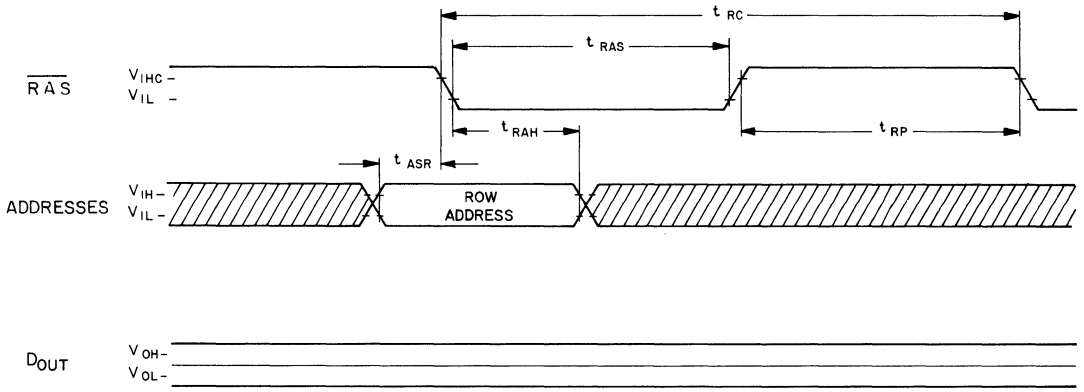
WRITE CYCLE



READ–WRITE/READ–MODIFY–WRITE CYCLE

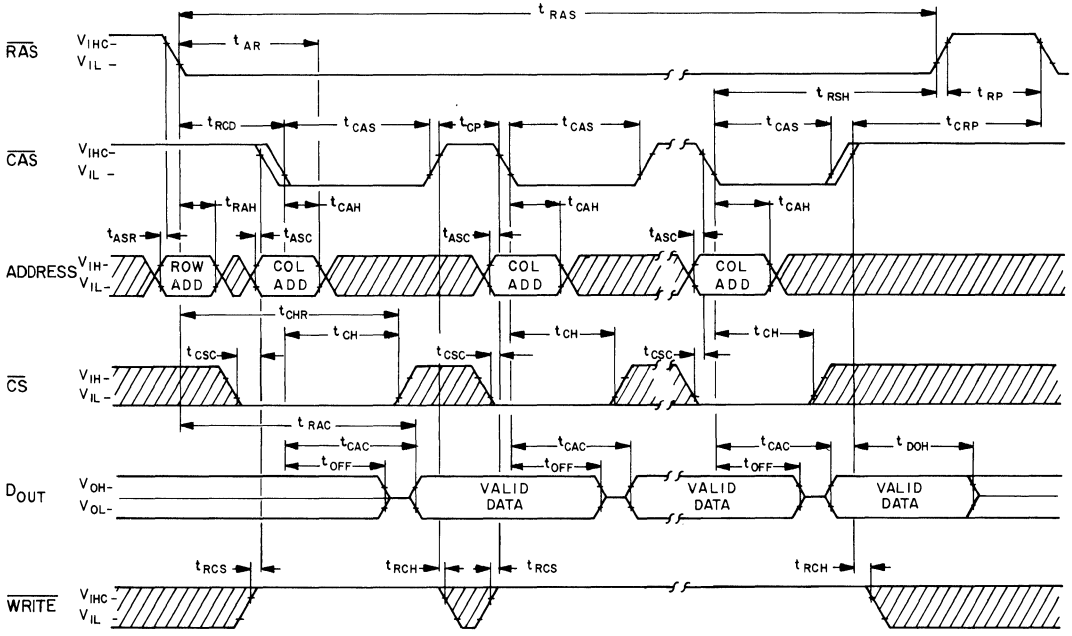


"RAS ONLY" REFRESH CYCLE

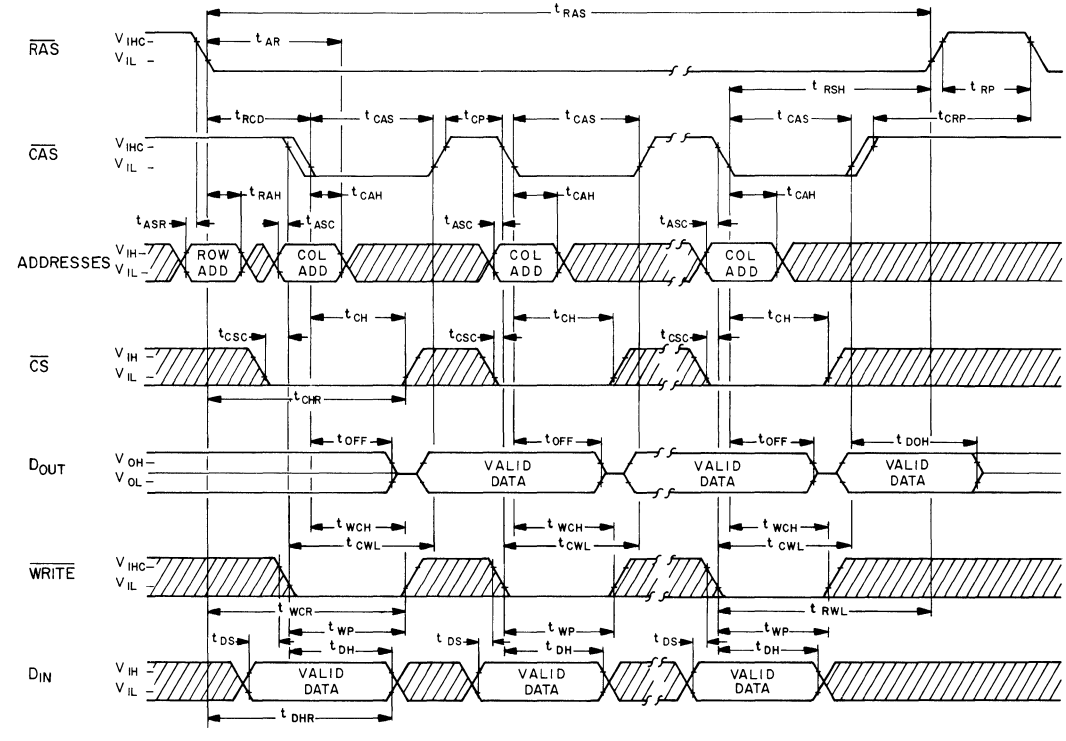


Note: D_{OUT} remains unchanged from previous cycle.

PAGE MODE READ CYCLE



PAGE MODE WRITE CYCLE



ADDRESSING

The 12 address bits required to decode1 of the 4096 cell locations within the MK 4027 are multiplexed onto the 6 address inputs and latched into the on-chip address latches by externally applying two negative going TTL level clocks. The first clock, the Row Address Strobe ($\overline{RAS}$), latches the 6 row address bits into the chip. The second clock, the Column Address Strobe ($\overline{CAS}$), subsequently latches the 6 column address bits plus Chip Select ($\overline{CS}$) into the chip. The internal circuitry of the MK 4027 is designed to allow the column information to be externally applied to the chip before it is actually required. Because of this, the hold time requirements for the input signals associated with the Column Address Strobe are also referenced to $\overline{RAS}$. However, this gated $\overline{CAS}$ feature allows the system designer to compensate for timing skews that may be encountered in the multiplexing operation. Since the Chip Select signal is not required until $\overline{CAS}$ time, which is well into the memory cycle,its decoding time does not add to system access or cycle time.

DATA INPUT/OUTPUT

Data to be written into a selected cell is latched into an on-chip register by a combination of $\overline{WRITE}$ and $\overline{CAS}$ while $\overline{RAS}$ is active. The later of the signals ($\overline{WRITE}$ or $\overline{CAS}$) to make its negative transition is the strobe for the Data In register. This permits several options in the write cycle timing. In a write cycle, if the $\overline{WRITE}$ input is brought low prior to $\overline{CAS}$, the Data In is strobed by $\overline{CAS}$, and the set-up and hold times are referenced to $\overline{CAS}$. If the data input is not available at $\overline{CAS}$ time or if it is desired that the cycle be a read-write cycle, the $\overline{WRITE}$ signal must be delayed until after $\overline{CAS}$. In this "delayed write cycle" the data input set-up and hold times are referenced to the negative edge of $\overline{WRITE}$ rather than to $\overline{CAS}$. (To illustrate this feature, Data In is referenced to $\overline{WRITE}$ in the timing diagram depicting the read-write and page mode write cycles while the "early write" cycle diagram shows Data In referenced to $\overline{CAS}$.) Note that if the chip is unselected ($\overline{CS}$ high at $\overline{CAS}$ time) $\overline{WRITE}$ commands are not executed and, consequently, data stored in the memory is unaffected.

Data is retrieved from the memory in a read cycle by maintaining $\overline{WRITE}$ in the inactive or high state throughout the portion of the memory cycle in which $\overline{CAS}$ is active. Data read from the selected cell will be available at the output within the specified access time.

DATA OUTPUT LATCH

Any change in the condition of the Data Out Latch is initiated by the $\overline{CAS}$ signal. The output buffer is not affected by memory (refresh) cycles in which only the $\overline{RAS}$ signal is applied to the MK 4027. Whenever $\overline{CAS}$ makes a negative transition, the output will go unconditionally open-circuited, independent of the state of any other input to the chip. If the cycle in progress is a read,read-modify-write, or a delayed write cycle and the chip is selected, then the output latch and buffer will again go active and at access time will contain the data read from the selected cell. This output data is the same polarity (not inverted) as the input data. If the cycle in progress is a write cycle ($\overline{WRITE}$ active low before $\overline{CAS}$ goes low) and the chip is selected, then at access time the output latch and buffer will contain the input data. Once having gone active, the output will remain valid until the MK 4027 receives the next $\overline{CAS}$ negative edge. Intervening refresh cycles in which a $\overline{RAS}$ is received (but no $\overline{CAS}$) will not cause valid data to be affected. Conversely, the output will assume the open-circuit state during any cycle in which the MK 4027 receives a $\overline{CAS}$ but no $\overline{RAS}$ signal (regardless of the state of any other inputs). The output will also assume the open circuit state in normal cycles (in which both $\overline{RAS}$ and $\overline{CAS}$ signals occur) if the chip is unselected.

The three-state data output buffer presents the data output pin with a low impedance to V_{CC} for a logic 1 and a low impedance to V_{SS} for a logic 0. The output resistance to V_{CC} (logic 1 state) is 420 Ω maximum and 135 Ω typically. The output resistance to V_{SS} (logic 0 state) is 125 Ω maximum and 35 Ω typically. The separate V_{CC} pin allows the output buffer to be powered from the supply voltage of the logic to which the chip is interfaced. During battery standby operation, the V_{CC} pin may have power removed without affecting the MK 4027 refresh operation. This allows all system logic except the $\overline{RAS}$ timing circuitry and the refresh address logic to be turned off during battery standby to conserve power.

REFRESH

Refresh of the dynamic cell matrix is accomplished by performing a memory cycle at each of the 64 row addresses within each 2 millisecond time interval. Any cycle in which a $\overline{RAS}$ signal occurs, accomplishes a refresh operation. A read cycle will refresh the selected row, regardless of the state of the Chip Select ($\overline{CS}$) input. A write or read-modify-write cycle also refreshes the selected row, but the chip should be unselected to prevent writing data into the selected cell. If, during a refresh cycle, the MK 4027 receives a $\overline{RAS}$ signal but no $\overline{CAS}$ signal, the state of the output will not be affected. However, if "$\overline{RAS}$-only" refresh cycles (where $\overline{RAS}$ is the only signal applied to the chip) are continued for extended periods, the output buffer may eventually lose proper data and go open-circuit. The output buffer will regain activity with the first cycle in which a $\overline{CAS}$ signal is applied to the chip.

POWER DISSIPATION/STANDBY MODE

Most of the circuitry used in the MK 4027 is dynamic and most of the power drawn is the result of an address strobe edge. Because the power is not drawn during the whole time the strobe is active, the dynamic power is a function of operating frequency rather than active duty cycle. Typically, the power is 170mW at 1 μsec cycle rate for the MK 4027 with a worse case power of less than 470mW at 320nsec cycle time. To minimize the overall system power, the Row Address Strobe ($\overline{RAS}$) should be decoded and supplied to only the selected chips. The $\overline{CAS}$ must be supplied to all chips (to turn off the unselected output). Those chips that did not receive a $\overline{RAS}$, however, will not dissipate any power on the $\overline{CAS}$ edges, except for that required to turn off the outputs. If the $\overline{RAS}$ signal is decoded and supplied only to the selected chips, then the Chip Select ($\overline{CS}$) input of all chips can be at a logic 0. The chips that receive a $\overline{CAS}$ but no $\overline{RAS}$ will be unselected (output open-circuited) regardless of the Chip Select input. For refresh cycles, however, either the $\overline{CS}$ input of all chips must be high or the $\overline{CAS}$ input must be held high to prevent several "wire-OR'd" outputs from turning on with opposing force. Note that the MK 4027 will dissipate considerably less power when the refresh operation is accomplished with a "$\overline{RAS}$-only" cycle as opposed to a normal $\overline{RAS}/\overline{CAS}$ memory cycle.

PAGE MODE OPERATION

The "Page Mode" feature of the MK 4027 allows for successive memory operations at multiple column locations of the same row address with increased speed without an increase in power. This is done by strobing the row address into the chip and keeping the $\overline{RAS}$ signal at a logic 0 throughout all successive memory cycles in which the row address is common. This "page mode" of operation will not dissipate the power associated with the negative going edge of $\overline{RAS}$. Also, the time required for strobing in a new row address is eliminated, thereby decreasing the access and cycle times. The chip select input ($\overline{CS}$) is operative in page mode cycles just as in normal cycles. It is not necessary that the chip be selected during the first operation in a sequence of page cycles. Likewise, the $\overline{CS}$ input can be used to select or disable any cycle(s) in a series of page cycles. This feature allows the page boundary to be extended beyond the 64 column locations in a single chip. The page boundary can be extended by applying $\overline{RAS}$ to multiple 4K memory blocks and decoding $\overline{CS}$ to select the proper block.

POWER UP

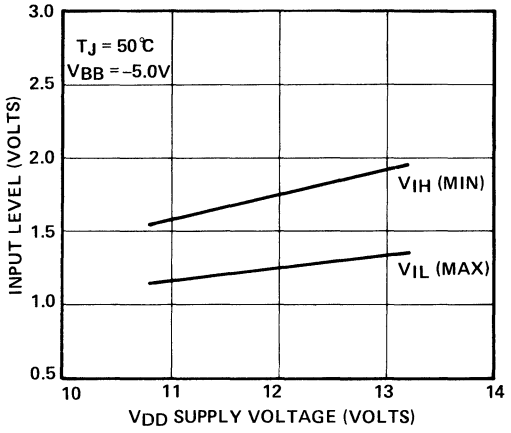
The MK 4027 requires no particular power supply sequencing so long as the Absolute Maximum Rating Conditions are observed. However, in order to insure compliance with the Absolute Maximum Ratings, MOSTEK recommends sequencing of power supplies such that V_{BB} is applied first and removed last. V_{BB} should never be more positive than V_{SS} when power is applied to V_{DD}.

Under system failure conditions in which one or more supplies exceed the specified limits significant additional margin against catastrophic device failure may be achieved by forcing $\overline{RAS}$ and Data Out to the inactive state.

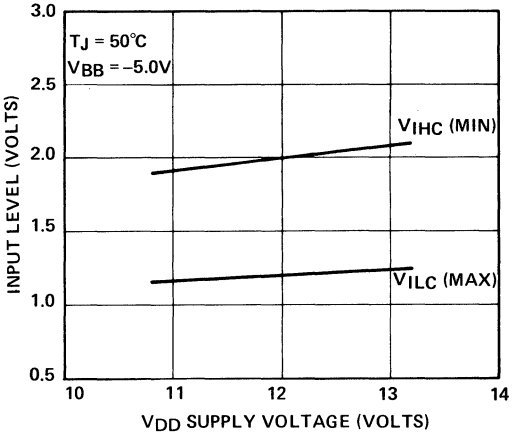
After power is applied to the device, the MK 4027 requires several cycles before proper device operation is achieved. Any 8 cycles which perform refresh are adequate for this purpose.

TYPICAL DEVICE CHARACTERISTICS

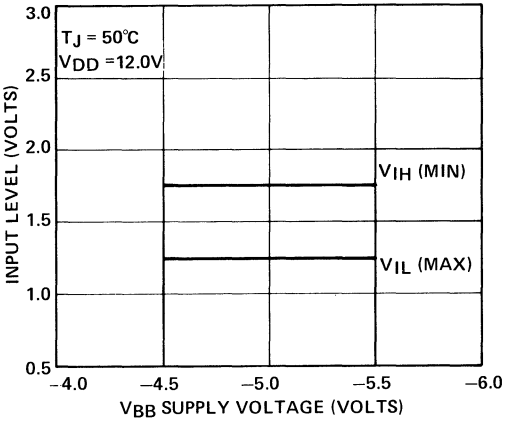
TYPICAL ADDRESS AND DATA INPUT LEVELS vs. V_{DD}



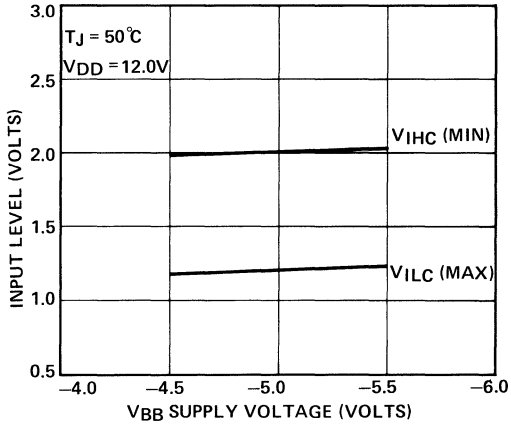
TYPICAL CLOCK INPUT LEVELS vs. V_{DD}



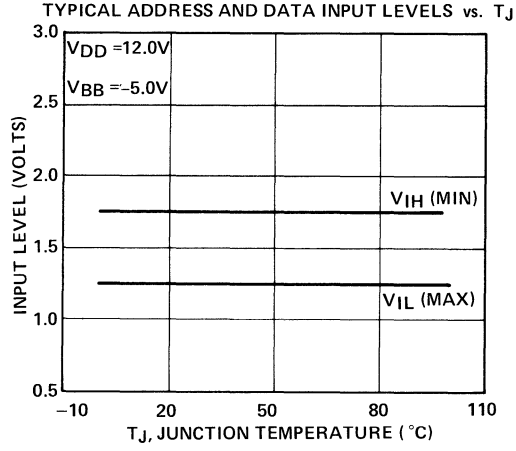
TYPICAL ADDRESS AND DATA INPUT LEVELS vs. V_{BB}



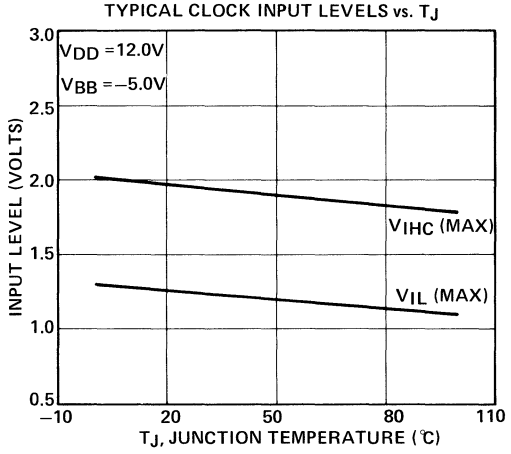
TYPICAL CLOCK INPUT LEVELS vs. V_{BB}



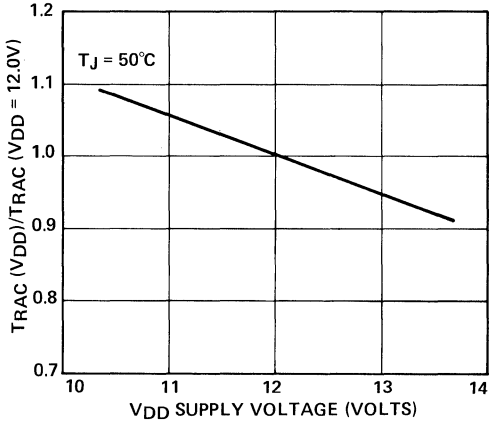
TYPICAL ADDRESS AND DATA INPUT LEVELS vs. T_J



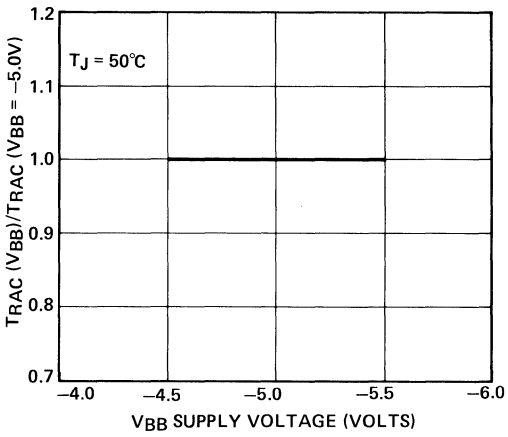
TYPICAL CLOCK INPUT LEVELS vs. T_J



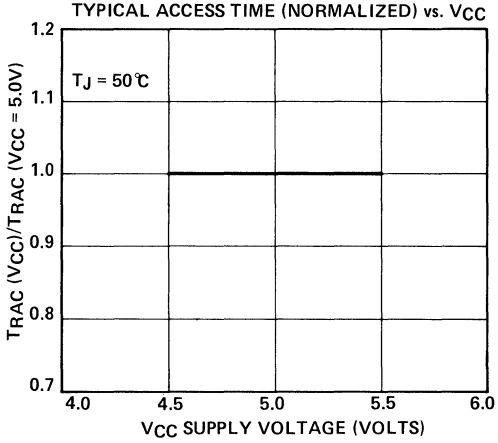
TYPICAL ACCESS TIME (NORMALIZED) vs. V_{DD}



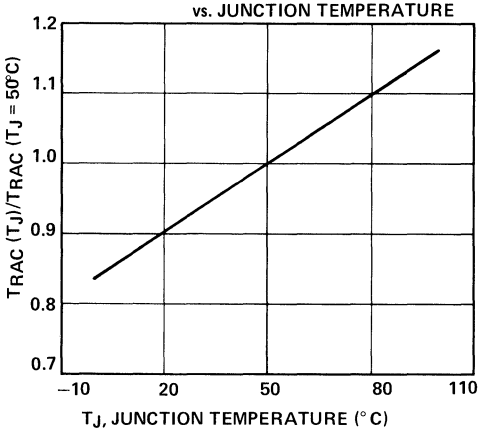
TYPICAL ACCESS TIME (NORMALIZED) vs. V_{BB}



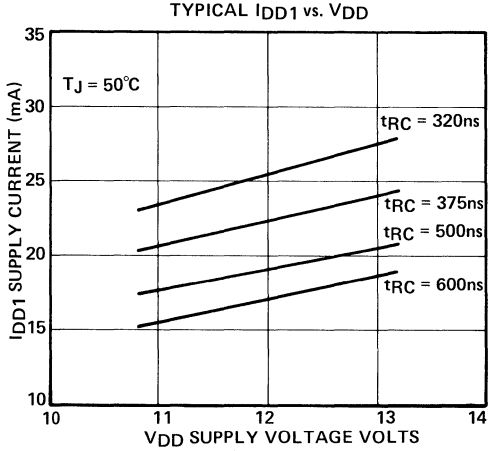
TYPICAL ACCESS TIME (NORMALIZED) vs. V_{CC}



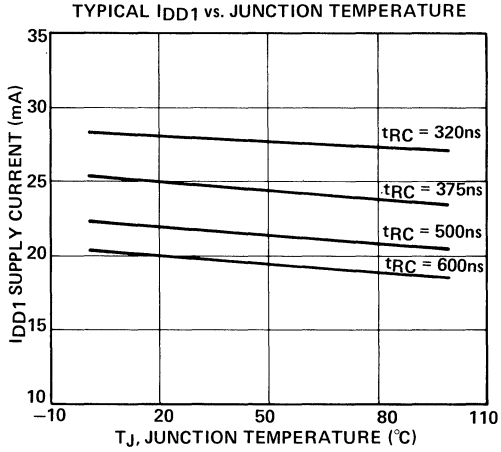
TYPICAL ACCESS TIME (NORMALIZED) vs. JUNCTION TEMPERATURE



TYPICAL I_{DD1} vs. V_{DD}



TYPICAL I_{DD1} vs. JUNCTION TEMPERATURE



MOSTEK

4096 X 1 BIT DYNAMIC RAM

MK4096 (P/N)-6/16/11

FEATURES

- ☐ Industry standard 16-pin DIP configuration (available in plastic (N) and ceramic (P) packages)
- ☐ All inputs are low capacitance and TTL compatible
- ☐ Input latches for address, chip select and data in
- ☐ Inputs protected against static charge
- ☐ Three-state TTL compatible output, latched and valid into next cycle
- ☐ Proven reliability with high performance

Part Number	Access Time	Cycle Time	Max Power*
MK 4096–6	250 ns	375 ns	450mW
MK 4096–16	300 ns	425 ns	385mW
MK 4096–11	350 ns	500 ns	320mW

*Standby power for all parts < 19mW

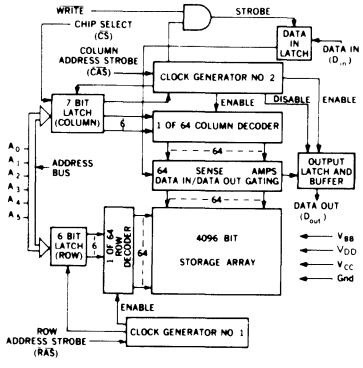
DESCRIPTION

The MK 4096 is the recognized industry standard 4096 word by 1 bit MOS Random Access Memory circuit packaged in a standard 16-pin DIP on 0.3 inch centers. This package configuration is made possible by a unique multiplexing and latching technique for the address inputs. The use of the 16-pin DIP for the MK 4096 provides high system bit densities and is compatible with widely available automated testing and insertion equipment.

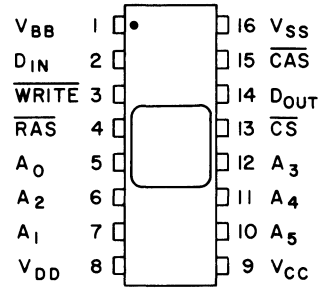
The MK 4096 is fabricated with MOSTEK's standard Self-Aligned, Poly-Interconnect, N-Channel (SPIN) process. The SPIN process allows the MK 4096 to be a highly manufacturable, state-of-the-art memory circuit that exhibits the reliability and performance standards necessary for today's (and tomorrow's) data processing applications. The MK 4096 employs a single transistor storage cell, utilizing a dynamic storage technique and dynamic control circuitry to achieve optimum performance with low power dissipation.

System oriented features incorporated within the MK 4096 include direct interfacing capability with TTL, 6 instead of 12 address lines to drive, on-chip registers which can eliminate the need for interface registers, input logic levels selected to optimize the noise immunity, and two chip select methods to allow the user to determine the speed/power characteristics of his memory system.

FUNCTIONAL DIAGRAM



PIN CONNECTIONS



PIN NAMES

A_0 - A_5	ADDRESS INPUTS	D_{IN}	DATA IN
$\overline{CAS}$	COLUMN ADDRESS STROBE	D_{OUT}	DATA OUT
$\overline{CS}$	CHIP SELECT	V_{BB}	POWER (–5V)
$\overline{RAS}$	ROW ADDRESS STROBE	V_{CC}	POWER (+5V)
$\overline{WRITE}$	READ/WRITE INPUT	V_{DD}	POWER (+12V)
		V_{SS}	GROUND

ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to V_{BB} . . . . −0.5V to + 25V
(V_{SS}−V_{BB} ⩾ 4.5V
Operating temperature T_A (Ambient) . . . . 0°C to + 70°C
Storage temperature (Ceramic) . . . . . −65°C to + 150°C
Storage temperature (Plastic) . . . . . −55°C to + 125°C
Power dissipation 1Watt
Data out current 50mA

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS (17)
(0°C ⩽ T_A ⩽+70°C)

	PARAMETER	MK 4096–6 MIN	MK 4096–6 MAX	MK 4096–16 MIN	MK 4096–16 MAX	MK 4096–11 MIN	MK 4096–11 MAX	UNITS	NOTE
V_{DD}	Supply Voltage	11.4	12.6	11.4	12.6	11.4	12.6	Volts	1
V_{CC}	Supply Voltage	V_{SS}	V_{DD}	V_{SS}	V_{DD}	V_{SS}	V_{DD}	Volts	1,2
V_{SS}	Supply Voltage	0	0	0	0	0	0	Volts	1
V_{BB}	Supply Voltage	−4.5	−5.5	−4.5	−5.5	−4.5	−5.5	Volts	1
V_{IHC}	Logic 1 Voltage – $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	2.7	7.0	2.7	7.0	3.0	7.0	Volts	1,3
V_{IH}	Logic 1 Voltage, all inputs except $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	2.4	7.0	2.4	7.0	2.4	7.0	Volts	1,3
V_{IL}	Logic 0 Voltage, all inputs	−1.0	0.8	−1.0	0.8	−1.0	0.8	Volts	1,3

DC ELECTRICAL CHARACTERISTICS (17)
(0°C ⩽ T_A ⩽ 70°C)(V_{DD} = 12.0V ± 5%; V_{CC} = 5.0V ± 10%; V_{SS} = 0V; V_{BB} = −5.0V ± 10%)

	PARAMETER	MK4096-6 MIN	MK4096-6 MAX	MK4096-16 MIN	MK4096-16 MAX	MK4096-11 MIN	MK4096-11 MAX	UNITS	NOTES
I_{DD1}	Average V_{DD} Power Supply Current		35		30		25	mA	4
I_{CC}	V_{CC} Power Supply Current							mA	5
I_{BB}	Average V_{BB} Power Supply Current		75		75		75	μA	
I_{DD2}	Standby V_{DD} Power Supply Current		1.5		1.5		1.5	mA	7
I_{DD3}	Average V_{DD} Supply Current during "$\overline{RAS}$-only" cycles		25		22		18	mA	4
$I_{I(L)}$	Input Leakage Current (any input)		5		5		5	μA	6
$I_{O(L)}$	Output Leakage Current		10		10		10	μA	7,8
V_{OH}	Output Logic 1 Voltage @ I_{OUT} = −5mA	2.4		2.4		2.4		Volts	2
V_{OL}	Output Logic 0 Voltage @ I_{OUT} = 2mA		0.4		0.4		0.4	Volts	

NOTES

1. All voltages referenced to V_{SS}. V_{BB} must be applied to and removed from the device within 5 seconds of V_{DD}.
2. Output voltage will swing from V_{SS} to V_{CC} if V_{CC} ⩽ V_{DD} −4 volts. If V_{CC} ⩾ V_{DD} −4 volts, the output will swing from V_{SS} to a voltage somewhat less than V_{DD}.
3. Device speed is not guaranteed at input voltages greater than TTL levels (0 to 5V).
4. Current is proportional to cycle rate; maximum current is measured at the fastest cycle rate.
5. I_{CC} depends upon output loading. The V_{CC} supply is connected to the output buffer only.
6. All device pins at 0 volts except V_{BB} which is at −5 volts and the pin under test which is at +10 volts.
7. Output is disabled (open-circuit) and $\overline{RAS}$ and $\overline{CAS}$ are both at a logic 1.
8. 0V ⩽ V_{OUT} ⩽ +10V.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (10, 15,17)

($0°C \leq T_A \leq 70°C$) (V_{DD} = 12.0V ± 5%, V_{CC} = 5.0V ± 10%, V_{SS} = 0V, V_{BB} = −5.0V ± 10%)

		MK 4096-6		MK 4096-16		MK 4096-11			
	PARAMETER	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
t_{RC}	Random Read or Write Cycle Time	375		425		500		nsec	11
t_{RAC}	Access time from Row Address Strobe		250		300		350		11,13
t_{CAC}	Access Time from Column Address Strobe		140		165		200		12,13
t_{OFF}	Output Buffer Turn-Off Delay	0	65	0	80	0	100		
t_{RP}	Row Address Strobe Precharge Time	115		125		150			
t_{RAS}	Row Address Strobe Pulse Width	250	10,000	300	10,000	350	10,000		
t_{RCL}	Row To Column Strobe Lead Time	60	110	80	135	100	150		14
t_{CAS}	Column Address Strobe Pulse Width	140		165		200			12
t_{AS}	Address Set-Up Time	0		0		0			
t_{AH}	Address Hold Time	60		80		100			
t_{CH}	Chip Select Hold Time	100		100		100			
t_T	Rise and Fall Times	3	50	3	50	3	50		15
t_{RCS}	Read Command Set-Up Time	0		0		0			
t_{RCH}	Read Command Hold Time	0		0		0			
t_{WCH}	Write Command Hold Time	110		130		150			
t_{WP}	Write Command Pulse Width	110		130		150			
t_{CRL}	Column to Row Strobe Lead Time	−40	+40	−50	+50	−50	+50		
t_{CWL}	Write Command to Column Strobe Lead Time	110		130		150			
t_{DS}	Data In Set-Up Time	0		0		0			16
t_{DH}	Data In Hold Time	110		130		150			16
t_{RFSH}	Refresh Period		2		2		2	msec	
t_{MOD}	Modify Time		10		10		10	µsec	
t_{DOH}	Data Out Hold Time	10		10		10		µsec	

NOTES Continued

9. Capacitance measured with Boonton Meter or effective capacitance calculated from the equation: $C = \frac{I \Delta t}{\Delta V}$ with current equal to a constant 20mA.

10. A C measurements assume t_T = 5ns.

11. Assumes that $t_{RCL} + t_T \leq t_{RCL}$ (max).

12. Assumes that $t_{RCL} + t_T \geq t_{RCL}$ (max).

13. Measured with a load circuit equivalent to 1 TTL load and C_L = 100pF.

14. Operation within the t_{RCL} (max) limit insures that t_{RAC} (max) can be met. t_{RCL} (max) is specified as a reference point only; if t_{RCL} is greater than the specified t_{RCL} (max) limit, then access time is controlled exclusively by t_{CAC} and t_{RAS}, t_{RAC} and t_{RCL} will be longer by the amount $t_{RCL} + t_T$ exceeds t_{RCL} (max).

15. V_{IHC} (min) or V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IHC} or V_{IH} and V_{IL}.

16. These parameters are referenced to $\overline{CAS}$ leading edge in random write cycles and to $\overline{WRITE}$ leading edge in delayed write or read-modify-write cycles.

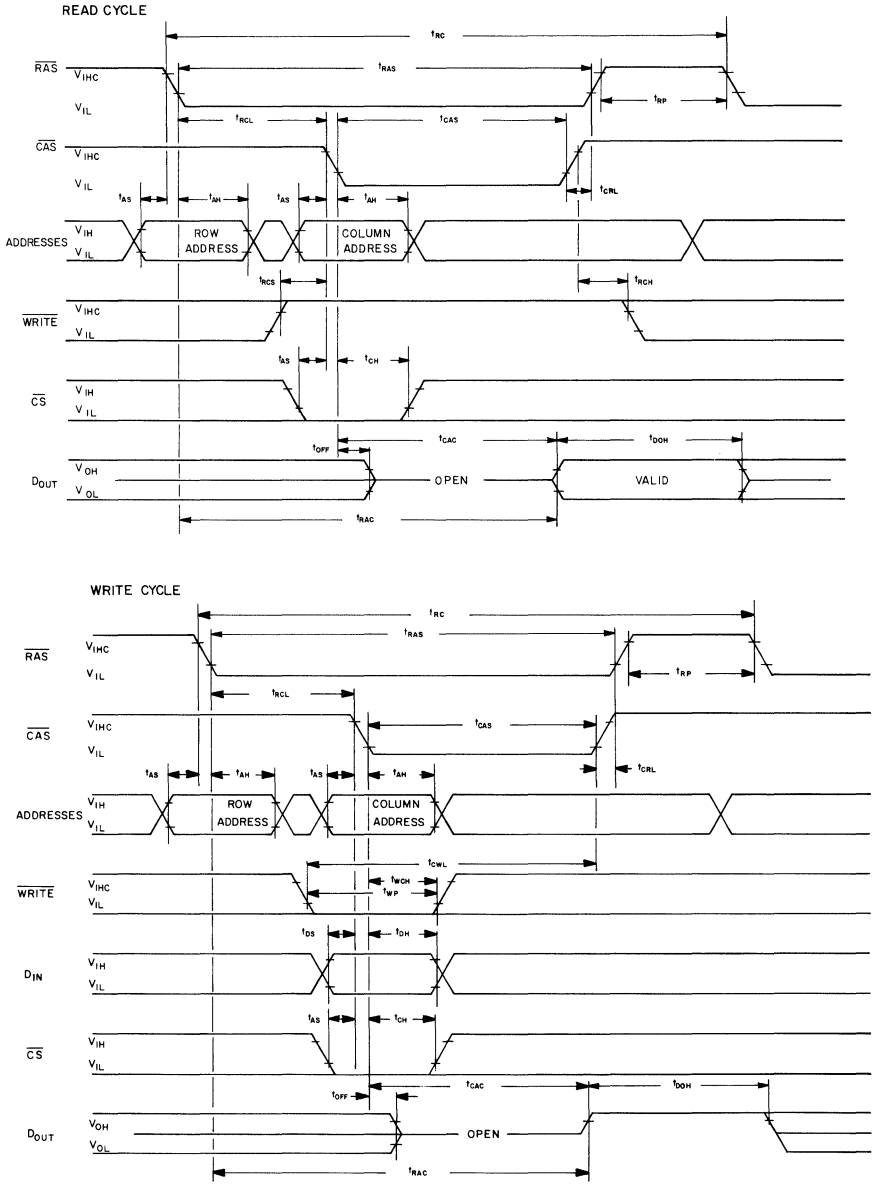
17. After the application of supply voltages or after extended periods of operation without clocks, the device must perform a minimum of one initialization cycle (any valid memory cycle containing both $\overline{RAS}$ and $\overline{CAS}$) prior to normal operation.

AC ELECTRICAL CHARACTERISTICS

(0°C $\leq T_A \leq$ + 70°C) (V_{DD} = 12.0V ± 5%, V_{CC} =5.0V ±10%, V_{SS} = 0V, V_{BB} = –5.0V ± 10%)

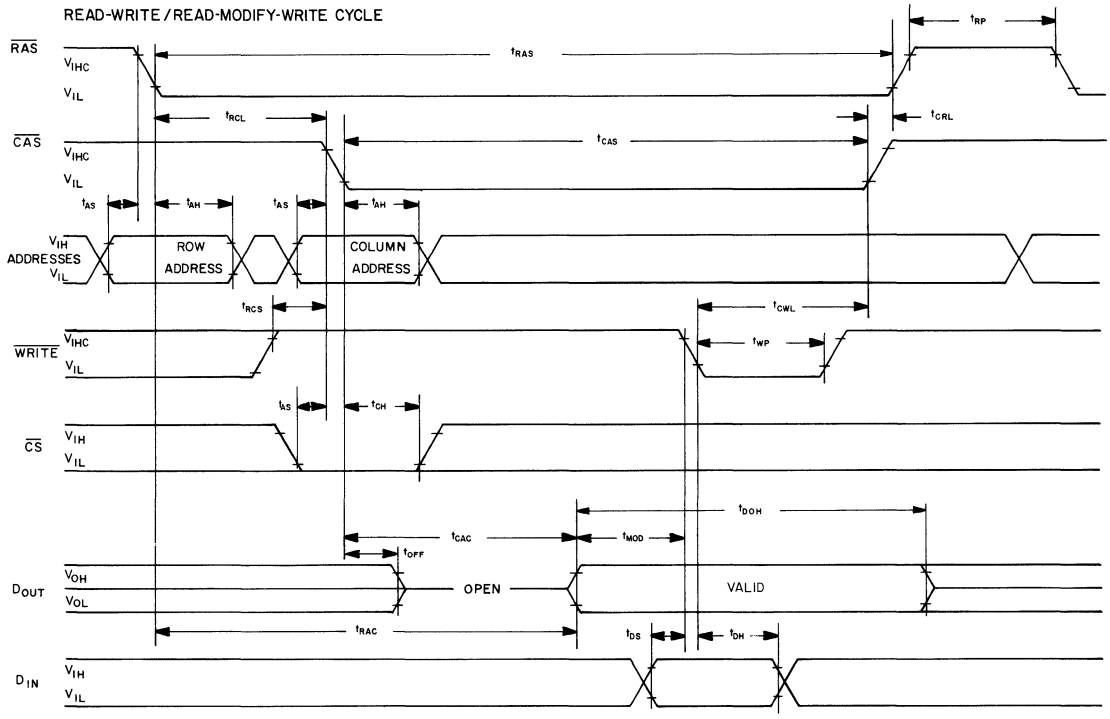
	PARAMETER	TYP	MAX	UNITS	NOTES
C_{I1}	Input Capacitance ($A_0 - A_5$)	7	10	pF	9
C_{I2}	Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, D_{IN}, $\overline{WRITE}$, $\overline{CS}$)	5	7	pF	9
C_O	Output Capacitance (D_{OUT})	5	8	pF	7,9

TIMING WAVEFORMS

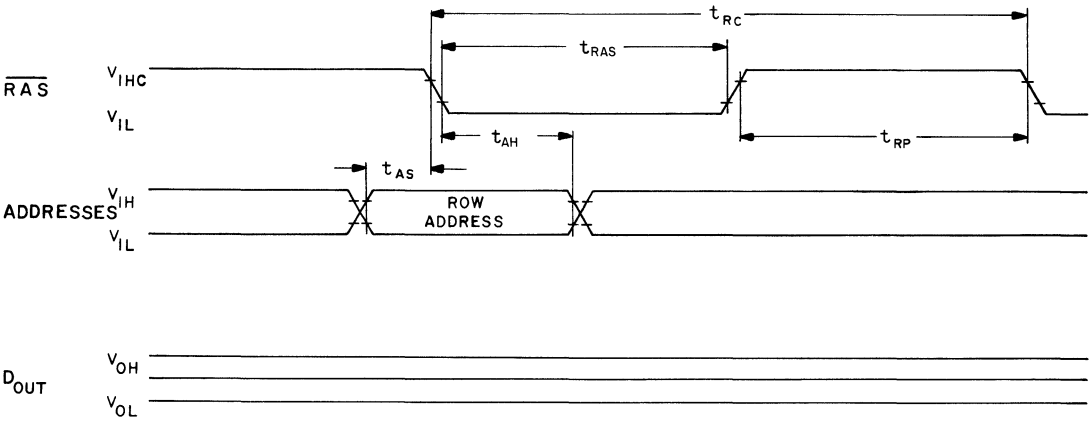


TIMING WAVEFORMS

READ-WRITE / READ-MODIFY-WRITE CYCLE



"RAS ONLY" REFRESH CYCLE



NOTE:

Prior to the first memory cycle following a period (beyond 2mS) of "RAS-only refresh, a memory-cycle employing both RAS and CAS must be performed to insure proper device operation.

ADDRESSING

The 12 address bits required to decode one of the 4096 cell locations within the MK 4096 are multiplexed onto the 6 address inputs and latched into the on-chip address latches by externally applying two negative going TTL level clocks. The first clock, the Row Address Strobe ($\overline{RAS}$), latches the 6 row address bits into the chip. The second clock, the Column Address Strobe ($\overline{CAS}$), subsequently latches the 6 column address bits plus Chip Select ($\overline{CS}$) into the chip. (Note that since the Chip Select signal is not required until $\overline{CAS}$ time, which is well into the memory cycle, its decoding time does not add to system access or cycle time). Each of these signals, $\overline{RAS}$ and $\overline{CAS}$, triggers a sequence of events which are controlled by different delayed internal clocks. The two clock chains are linked together logically in such a way that the address multiplexing operation is done outside of the critical path timing sequence for read data access. The later events in the $\overline{CAS}$ clock sequence are inhibited until the occurrence of a delayed signal derived from the $\overline{RAS}$ clock chain. This " gated $\overline{CAS}$" feature allows the $\overline{CAS}$ clock to be externally activated as soon as the Row Address Hold Time specification (t_{AH}) has been satisfied and the 6 address inputs have been changed from Row address to Column address information.

Note that $\overline{CAS}$ can be activated at any time after t_{AH} and it will have no effect on the worst case data access time (t_{RAC}) up to the point in time when the delayed row clock no longer inhibits the remaining sequence of column clocks. Two timing end points result from the internal gating of $\overline{CAS}$ which are called t_{RCL} (min) and t_{RCL} (max). No data storage or reading errors will result if $\overline{CAS}$ is applied to the MK 4096 at a point in time beyond the t_{RCL} (max) limit. However, access time will then be determined exclusively by the access time from $\overline{CAS}$ (t_{CAC}) rather than from $\overline{RAS}$ (t_{RAC}), and access time from $\overline{RAS}$ will be lengthened by the amount that t_{RCL} exceeds the t_{RCL} (max) limit.

DATA INPUT/OUTPUT

Data to be written into a selected cell is latched into an on-chip register by a combination of $\overline{WRITE}$ and $\overline{CAS}$ while $\overline{RAS}$ is active. The later of the signals ($\overline{WRITE}$ or $\overline{CAS}$) to make its negative transition is the strobe for the Data In register. This permits several options in the write cycle timing. In a write cycle, if the $\overline{WRITE}$ input is brought low prior to $\overline{CAS}$, the Data In is strobed by $\overline{CAS}$, and the set-up and hold times are referenced to $\overline{CAS}$. If the data input is not available at $\overline{CAS}$ time or if it is desired that the cycle be a read-write or read-modify-write cycle, the $\overline{WRITE}$ signal must be delayed until after $\overline{CAS}$. In this "delayed write cycle" the data input set-up and hold times are referenced to the negative edge of $\overline{WRITE}$ rather than to $\overline{CAS}$. (To illustrate this feature, Data In is referenced to $\overline{WRITE}$ in the timing diagram depicting the read-modify-write cycle while the "early write" cycle diagram shows Data In referenced to $\overline{CAS}$). Note that if the chip is unselected ($\overline{CS}$ high at $\overline{CAS}$ time) $\overline{WRITE}$ commands are not executed and, consequently, data stored in the memory is unaffected.

Data is retrieved from the memory in a read cycle by maintaining $\overline{WRITE}$ in the inactive or high state throughout the portion of the memory cyle in which $\overline{CAS}$ is active. Data read from the selected cell will be available at the output within the specified access time.

DATA OUTPUT LATCH

Any change in the condition of the Data Out Latch is initiated by the $\overline{CAS}$ signal. The output buffer is not affected by memory (refresh) cycles in which only the $\overline{RAS}$ signal is applied to the MK 4096. Whenever $\overline{CAS}$ makes a negative transition, the output will go unconditionally open-circuited, independent of the state of any other input to the chip. If the cycle in progress is a read, read-modify-write, or a delayed write cycle and the chip is selected, then the output latch and buffer will again go active and at access time will contain the data read from the selected cell. This output data is the same polarity (not inverted) as the input data. If the cycle in progress is a write cycle ($\overline{WRITE}$ active low before $\overline{CAS}$ goes low) and the chip is selected, then at access time the output latch and buffer will contain a logic 1. Once having gone active, the output will remain valid until the MK 4096 receives the next $\overline{CAS}$ negative edge. Intervening refresh cycles in which a $\overline{RAS}$ is received (but no $\overline{CAS}$) will not cause valid data to be affected. Conversely, the output will assume the open-circuit state during any cycle in which the MK 4096 receives a $\overline{CAS}$ but no $\overline{RAS}$ signal (regardless of the state of any other inputs). The output will also assume the open-circuit state in normal cycles (in which both $\overline{RAS}$ and $\overline{CAS}$ signals occur) if the chip is unselected.

The three-state data output buffer presents the data output pin with a low impedance to V_{CC} for a logic 1 and a low impedance to V_{SS} for a logic 0. The effective resistance to V_{CC} (logic 1 state) is 500Ω maximum and 150Ω typically. The resistance to V_{SS} (logic 0 state) is 200Ω maximum and 100Ω typically. The separate V_{CC} pin allows the output buffer to be powered from the supply voltage of the logic to which the chip is interfaced. During battery standby operation, the V_{CC} pin may have power removed without affecting the MK 4096 refresh operation. This allows all system logic except the $\overline{RAS}/\overline{CAS}$ timing circuitry and the refresh address logic to be turned off during battery standby to conserve power.

REFRESH

Refresh of the dynamic cell matrix is accomplished by performing a memory cycle at each of the 64 row addresses within each 2 millisecond time interval. Any cycle in which a $\overline{RAS}$ signal occurs accomplishes a refresh operation. A read cycle will refresh the selected row, regardless of the Chip Select ($\overline{CS}$) input. A write or read-modify-write cycle also refreshes the selected row, but the chip should be unselected to prevent writing data into the selected cell.

For standby operation, a "$\overline{RAS}$-only" cycle can be employed to refresh the MK 4096. However, if "$\overline{RAS}$-only" refresh cycles (where $\overline{RAS}$ is the only signal applied to the chip) are continued for extended periods, the output buffer may eventually lose proper data and go open-circuit. Prior to the first memory cycle following a period (beyond 2ms) of "$\overline{RAS}$-only" refresh, a memory cycle employing both $\overline{RAS}$ and $\overline{CAS}$ must be performed to precharge the internal circuitry. This "dummy cycle" allows the output buffer to regain activity and enables the device to perform a read or write cycle upon command.

POWER DISSIPATION/STANDBY MODE

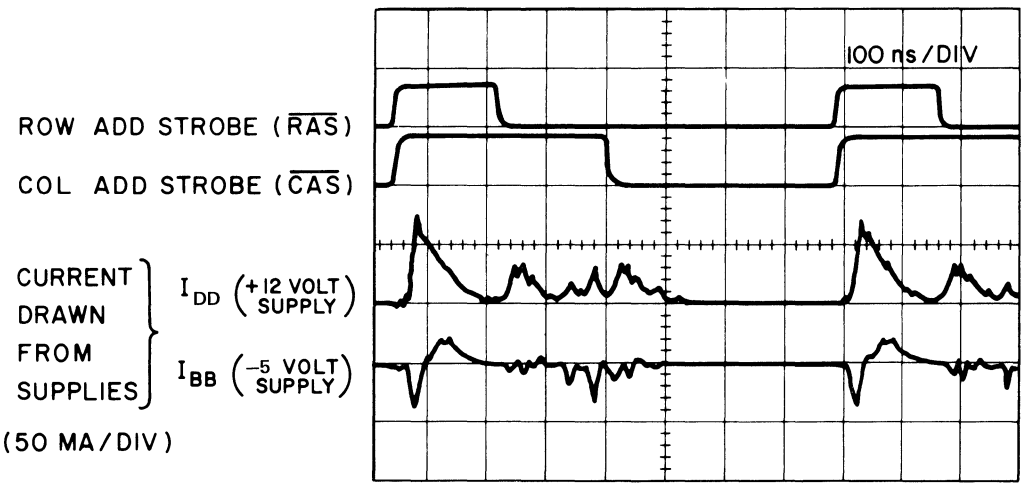
Most of the circuitry used in the MK 4096 is dynamic and most of the power drawn is the result of an address strobe edge. Because the power is not drawn during the whole time the strobe is active, the dynamic power is a function of operating frequency rather than active duty cycle. Typically, the power is 120 mW at a 1 μsec cycle rate for the MK 4096 with a maximum power of less than 450 mW at 375 nsec cycle time. To minimize the overall system power, the Row Address Strobe ($\overline{RAS}$) should be decoded and supplied to only the selected chips. The $\overline{CAS}$ must be supplied to all chips (to turn off the unselected output). Those chips that did not receive a $\overline{RAS}$, however, will not dissipate any power on the $\overline{CAS}$ edges, except for that required to turn off the outputs. If the $\overline{RAS}$ signal is decoded and supplied only to the selected chips, then the Chip Select ($\overline{CS}$) input of all chips can be at a logic 0. The chips that receive a $\overline{CAS}$ but no $\overline{RAS}$ will be unselected (output open-circuited) regardless of the Chip Select input. For refresh cycles, however, either the $\overline{CS}$ input of all chips must be high or the $\overline{CAS}$ input must be held high to prevent several "wire-ORed" outputs from turning on with opposing force.

The current waveforms for the current drawn from the V_{DD} and V_{BB} supplies are shown in Figure A. Since the current is pulsed, proper power distribution and bypassing techniques are required to maintain system power supply noise levels at an acceptable level. Low inductance supply lines for V_{DD} and V_{SS} are desirable. One 0.01 microfarad, low inductance, bypass capacitor per two MK 4096 devices and one 6.8 microfarad electrolytic capacitor per eight MK 4096 devices on each of the V_{DD} and V_{BB} supply lines is desirable.

POWER–UP

Under normal operating conditions the MK 4096 requires no particular power-up sequence. However, in order to achieve the most reliable performance from the MK 4096, proper consideration should be given to the V_{BB}/V_{DD} power supply relationship. The V_{BB} supply is an extremely important "protective voltage" since it performs two essential functions within the device. It establishes proper junction isolation and sets field-effect thresholds, both thin field and thick field. Misapplication of V_{BB} or device operation without the V_{BB} supply can affect long term device reliability. For optimum reliability performance from the MK 4096, it is suggested that measures be taken to not have V_{DD} (+12V) applied to the device for over five (5) seconds without the application of V_{BB} (–5V).

After power is applied to the device, the MK 4096 requires at least one memory cycle ($\overline{RAS}/\overline{CAS}$) before proper device operation is achieved. A normal 64 cycle refresh with both $\overline{RAS}$ and $\overline{CAS}$ is adequate for this purpose.



Power Supply Current Waveforms

MOSTEK

4096 X 1 BIT DYNAMIC RAM

MK4096 (P/N)-15

FEATURES

- ☐ Industry standard 16-pin DIP configuration
- ☐ Access time 350ns (MAX)
- ☐ Input latches for address, chip select and data in
- ☐ All inputs are low capacitance and TTL compatible
- ☐ Low cost for consumer and hobbyist microprocessor applications
- ☐ Three-state TTL compatible output, latched and valid into next cycle
- ☐ Low power dissipation
- ☐ Inputs protected against static charge

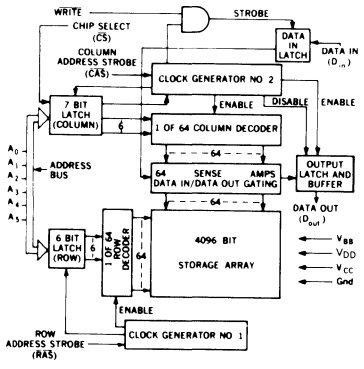
DESCRIPTION

The MK 4096 is the recognized industry standard 4096 word by 1 bit MOS Random Access Memory circuit packaged in a standard 16-pin DIP on 0.3 inch centers. This package configuration is made possible by a unique multiplexing and latching technique for the address inputs. The use of the 16-pin DIP for the MK 4096 provides high system bit densities and is compatible with widely available automated testing and insertion equipment.

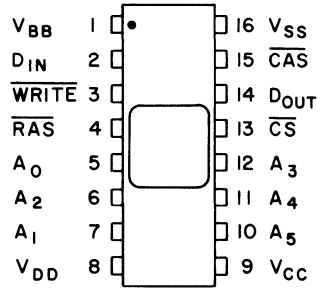
The MK 4096 is fabricated with MOSTEK's standard Self-Aligned, Poly-Interconnect, N-Channel (SPIN) process. The SPIN process allows the MK 4096 to be a highly manufacturable, state-of-the-art memory circuit that exhibits the reliability and performance standards necessary for today's (and tomorrow's) data processing applications. The MK 4096 employs a single transistor storage cell, utilizing a dynamic storage technique and dynamic control circuitry to achieve optimum performance with low power dissipation.

System oriented features incorporated within the MK 4096 include direct interfacing capability with TTL, 6 instead of 12 address lines to drive, on-chip registers which can eliminate the need for interface registers, input logic levels selected to optimize the noise immunity, and two chip select methods to allow the user to determine the speed/power characteristics of his memory system.

FUNCTIONAL DIAGRAM



PIN CONNECTIONS



PIN NAMES

$A_0 - A_5$	ADDRESS INPUTS	D_{IN}	DATA IN
$\overline{CAS}$	COLUMN ADDRESS STROBE	D_{OUT}	DATA OUT
$\overline{CS}$	CHIP SELECT	V_{BB}	POWER (–5V)
$\overline{RAS}$	ROW ADDRESS STROBE	V_{CC}	POWER (+5V)
$\overline{WRITE}$	READ/WRITE INPUT	V_{DD}	POWER (+15V)
		V_{SS}	GROUND

ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to V_{BB} . . . . −0.5V to + 25V
(V_{SS}−V_{BB} ≥ 4.5V
Operating temperature T_A (Ambient) . . . . 0°C to + 55°C
Storage temperature (Ceramic) . . . . . −65°C to + 150°C
Storage temperature (Plastic) . . . . . −55°C to + 125°C
Power dissipation . . . . . 1 Watt
Data out current 50mA

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS (17)
(0°C ≤ T_A ≤ +55°C)

	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{DD}	Supply Voltage	14.25	15.0	15.75	Volts	1
V_{CC}	Supply Voltage	V_{SS}		V_{DD}	Volts	1,2
V_{SS}	Supply Voltage	0		0	Volts	1
V_{BB}	Supply Voltage	−4.5	−5.0	−5.5	Volts	1
V_{IHC}	Logic 1 Voltage −$\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	3.5		7.0	Volts	1,3
V_{IH}	Logic 1 Voltage, all inputs except $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	3.0		7.0	Volts	1,3
V_{IL}	Logic 0 Voltage, all inputs	−1.0		0.8	Volts	1,3

DC ELECTRICAL CHARACTERISTICS (17)
(0°C ≤ T_A ≤ 55°C) (V_{DD} = 15.0V ±5%; V_{CC} = 5.0V ± 10%; V_{SS} = 0V; V_{BB} = −5.0V ± 10%)

	PARAMETER	MIN	MAX	UNITS	NOTES
I_{DD1}	Average V_{DD} Power Supply Current		35	mA	4
I_{CC}	V_{CC} Power Supply Current			mA	5
I_{BB}	Average V_{BB} Power Supply Current		75	μA	
I_{DD2}	Standby V_{DD} Power Supply Current		2	mA	7
I_{DD3}	Average V_{DD} Supply Current during "$\overline{RAS}$-only" cycles		24	mA	4
$I_{I(L)}$	Input Leakage Current (any input)		5	μA	6
$I_{O(L)}$	Output Leakage Current		10	μA	7,8
V_{OH}	Output Logic 1 Voltage @ I_{OUT}= −5mA	2.4		Volts	2
V_{OL}	Output Logic 0 Voltage @ I_{OUT} = 2mA		0.4	Volts	

NOTES

1. All voltages referenced to V_{SS}. V_{BB} must be applied to and removed from the device within 5 seconds of V_{DD}.
2. Output voltage will swing from V_{SS} to V_{CC} if $V_{CC} \leq V_{DD}$ −4 volts. If $V_{CC} \geq V_{DD}$ −4 volts, the output will swing from V_{SS} to a voltage somewhat less than V_{DD}.
3. Device speed is not guaranteed at input voltages greater than TTL levels (0 to 5V).
4. Current is proportional to cycle rate; maximum current is measured at the fastest cycle rate.
5. I_{CC} depends upon output loading. The V_{CC} supply is connected to the output buffer only.
6. All device pins at 0 volts except V_{BB} which is at −5 volts and the pin under test which is at +10 volts.
7. Output is disabled (open-circuit) and $\overline{RAS}$ and $\overline{CAS}$ are both at a logic 1.
8. 0V ≤ V_{OUT} ≤ +10V.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITONS (10,15,17)

($0°C \leq T_A \leq 55°C$) (V_{DD} = 15.0V ± 5%; V_{CC} = 5.0V ± 10%, V_{SS} = 0V, V_{BB} = −5.0V ± 10%)

	PARAMETER	MIN	MAX	UNITS	NOTES
t_{RC}	Random Read or Write Cycle Time	500		nsec	11
t_{RAC}	Access time from Row Address Strobe		350	nsec	11,13
t_{CAC}	Access Time from Column Address Strobe		200	nsec	12,13
t_{OFF}	Output Buffer Turn-Off Delay	0	100	nsec	
t_{RP}	Row Address Strobe Precharge Time	150		nsec	
t_{RAS}	Row Address Strobe Pulse Width	350	10,000	nsec	
t_{RCL}	Row To Column Strobe Lead Time	100	150	nsec	14
t_{CAS}	Column Address Strobe Pulse Width	200		nsec	12
t_{AS}	Address Set-Up Time	0		nsec	
t_{AH}	Address Hold Time	100		nsec	
t_{CH}	Chip Select Hold Time	100		nsec	
t_T	Rise and Fall Times	3	50	nsec	15
t_{RCS}	Read Command Set-Up Time	0		nsec	
t_{RCH}	Read Command Hold Time	0		nsec	
t_{WCH}	Write Command Hold Time	150		nsec	
t_{WP}	Write Command Pulse Width	150		nsec	
t_{CRL}	Column to Row Strobe Lead Time	−50	+50	nsec	
t_{CWL}	Write Command to Column Strobe Lead Time	150		nsec	
t_{DS}	Data In Set-Up Time	0		nsec	16
t_{DH}	Data In Hold Time	150		nsec	16
t_{RFSH}	Refresh Period		1	msec	
t_{MOD}	Modify Time		10	μ sec	
t_{DOH}	Data Out Hold Time	10		μ sec	

NOTES Continued

9. Capacitance measured with Boonton Meter or effective capacitance calculated from the equation: $C = \frac{I \Delta t}{\Delta V}$ with current equal to a constant 20mA.

10. A C measurements assume t_T = 5ns.

11. Assumes that $t_{RCL} + t_T \leq t_{RCL}$ (max).

12. Assumes that $t_{RCL} + t_T \geq t_{RCL}$ (max).

13. Measured with a load circuit equivalent to 1 TTL load and C_L = 100pF.

14. Operation within the t_{RCL} (max) limit insures that t_{RAC} (max) can be met. t_{RCL} (max) is specified as a reference point only; if t_{RCL} is greater than the specified t_{RCL} (max) limit, then access time is controlled exclusively by t_{CAC} and t_{RAS}, t_{RAC} and t_{RCL} will be longer by the amount $t_{RCL} + t_T$ exceeds t_{RCL} (max).

15. V_{IHC} (min) or V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IHC} or V_{IH} and V_{IL}.

16. These parameters are referenced to $\overline{CAS}$ leading edge in random write cycles and to $\overline{WRITE}$ leading edge in delayed write or read-modify-write cycles.

17. After the application of supply voltages or after extended periods of operation without clocks, the device must perform a minimum of one initialization cycle (any valid memory cycle containing both $\overline{RAS}$ and $\overline{CAS}$) prior to normal operation.

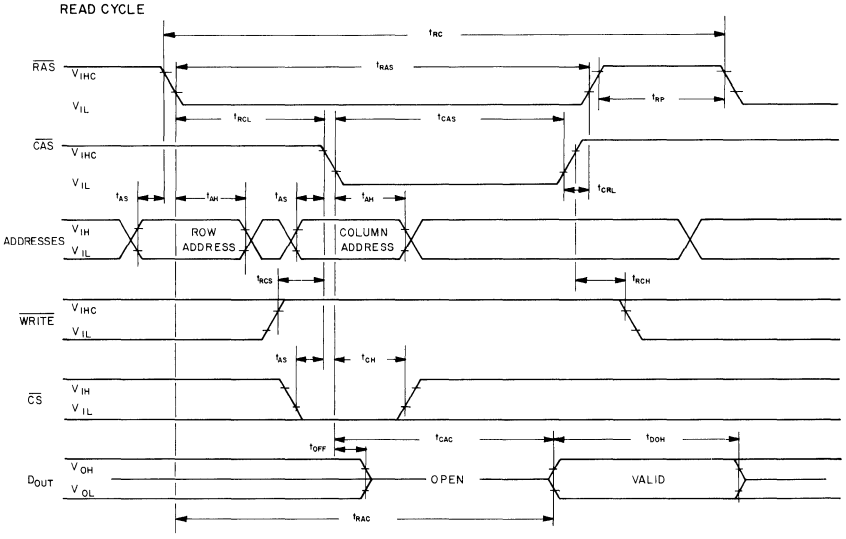
AC ELECTRICAL CHARACTERISTICS

($0℃ \leq T_A \leq +55℃$) (V_{DD} = 15.0V ± 5%, V_{CC} = 5.0V ± 10%, V_{SS} = 0V, V_{BB} = –5.0V ± 10%)

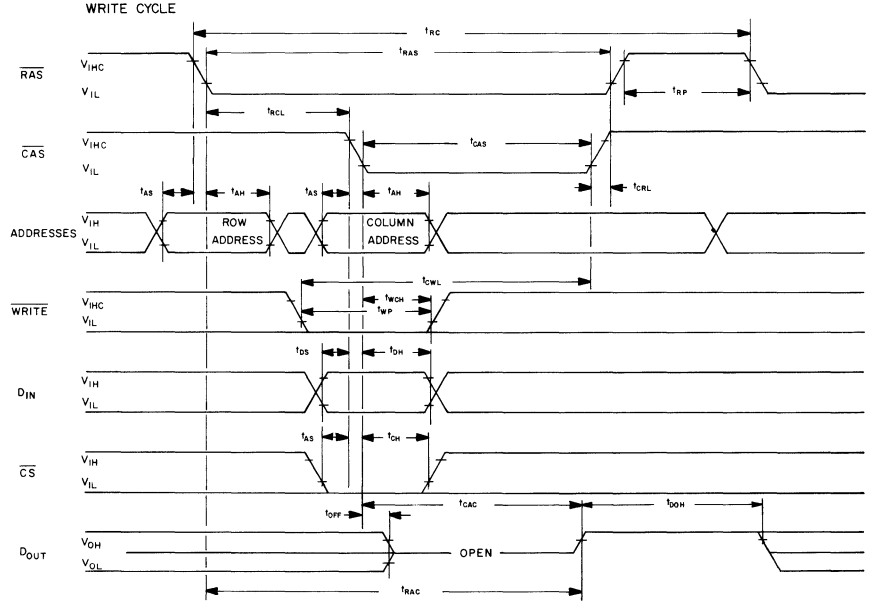
	PARAMETER	TYP	MAX	UNITS	NOTES
C_{I1}	Input Capacitance ($A_0 - A_5$)	7	10	pF	9
C_{I2}	Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, D_{IN}, $\overline{WRITE}$, $\overline{CS}$)	5	7	pF	9
C_O	Output Capacitance (D_{OUT})	5	8	pF	7,9

TIMING WAVEFORMS

READ CYCLE

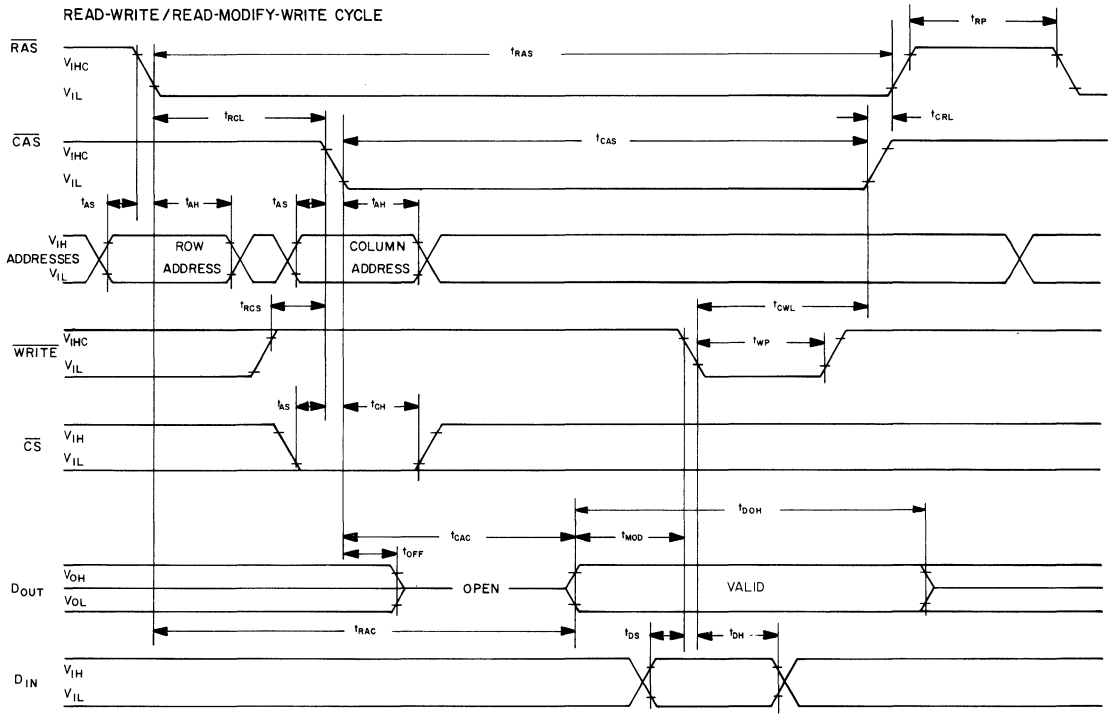


WRITE CYCLE

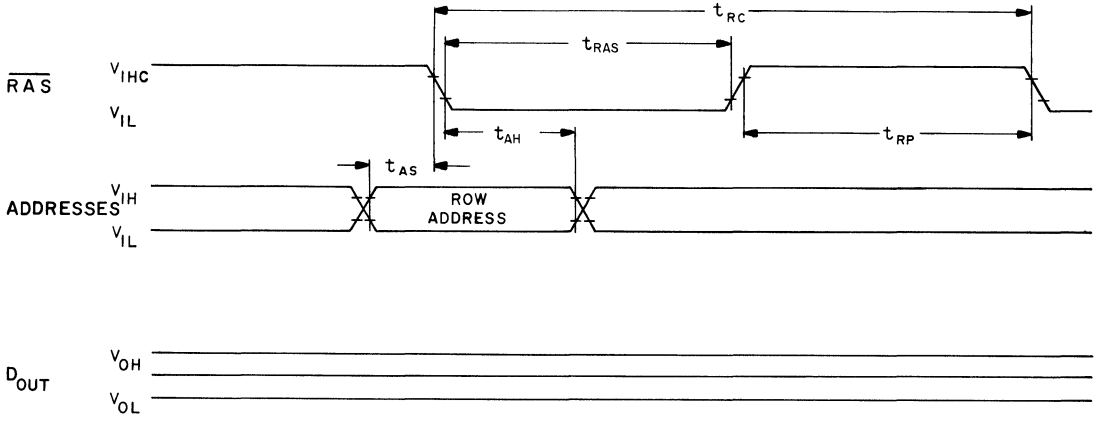


TIMING WAVEFORMS

READ-WRITE / READ-MODIFY-WRITE CYCLE



"RAS ONLY" REFRESH CYCLE (See text under Refresh)



NOTE:

Prior to the first memory cycle following a period (beyond 1mS) of "RAS-only refresh, a memory cycle employing both RAS and CAS must be performed to insure proper device operation.

ADDRESSING

The 12 address bits required to decode one of the 4096 cell locations within the MK 4096 are multiplexed onto the 6 address inputs and latched into the on-chip address latches by externally applying two negative going TTL level clocks. The first clock, the Row Address Strobe ($\overline{RAS}$), latches the 6 row address bits into the chip. The second clock, the Column Address Strobe ($\overline{CAS}$), subsequently latches the 6 column address bits plus Chip Select ($\overline{CS}$) into the chip. (Note that since the Chip Select signal is not required until $\overline{CAS}$ time, which is well into the memory cycle, its decoding time does not add to system access or cycle time). Each of these signals, $\overline{RAS}$ and $\overline{CAS}$, triggers a sequence of events which are controlled by different delayed internal clocks. The two clock chains are linked together logically in such a way that the address multiplexing operation is done outside of the critical path timing sequence for read data access. The later events in the $\overline{CAS}$ clock sequence are inhibited until the occurrence of a delayed signal derived from the $\overline{RAS}$ clock chain. This " gated $\overline{CAS}$" feature allows the $\overline{CAS}$ clock to be externally activated as soon as the Row Address Hold Time specification (t_{AH}) has been satisfied and the 6 address inputs have been changed from Row address to Column address information.

Note that $\overline{CAS}$ can be activated at any time after t_{AH} and it will have no effect on the worst case data access time (t_{RAC}) up to the point in time when the delayed row clock no longer inhibits the remaining sequence of column clocks. Two timing end points result from the internal gating of $\overline{CAS}$ which are called t_{RCL} (min) and t_{RCL} (max). No data storage or reading errors will result if $\overline{CAS}$ is applied to the MK 4096 at a point in time beyond the t_{RCL} (max) limit. However, access time will then be determined exclusively by the access time from $\overline{CAS}$ (t_{CAC}) rather than from $\overline{RAS}$ (t_{RAC}), and access time from $\overline{RAS}$ will be lengthened by the amount that t_{RCL} exceeds the t_{RCL} (max) limit.

DATA INPUT/OUTPUT

Data to be written into a selected cell is latched into an on-chip register by a combination of $\overline{WRITE}$ and $\overline{CAS}$ while $\overline{RAS}$ is active. The later of the signals ($\overline{WRITE}$ or $\overline{CAS}$) to make its negative transition is the strobe for the Data In register. This permits several options in the write cycle timing. In a write cycle, if the $\overline{WRITE}$ input is brought low prior to $\overline{CAS}$, the Data In is strobed by $\overline{CAS}$, and the set-up and hold times are referenced to $\overline{CAS}$. If the data input is not available at $\overline{CAS}$ time or if it is desired that the cycle be a read-write or read-modify-write cycle, the $\overline{WRITE}$ signal must be delayed until after $\overline{CAS}$. In this "delayed write cycle" the data input set-up and hold times are referenced to the negative edge of $\overline{WRITE}$ rather than to $\overline{CAS}$. (To illustrate this feature, Data In is referenced to $\overline{WRITE}$ in the timing diagram depicting the read-modify-write cycle while the "early write" cycle diagram shows Data In referenced to $\overline{CAS}$). Note that if the chip is unselected ($\overline{CS}$ high at $\overline{CAS}$ time) $\overline{WRITE}$ commands are not executed and, consequently, data stored in the memory is unaffected.

Data is retrieved from the memory in a read cycle by maintaining $\overline{WRITE}$ in the inactive or high state throughout the portion of the memory cyle in which $\overline{CAS}$ is active. Data read from the selected cell will be available at the output within the specified access time.

DATA OUTPUT LATCH

Any change in the condition of the Data Out Latch is initiated by the $\overline{CAS}$ signal. The output buffer is not affected by memory (refresh) cycles in which only the $\overline{RAS}$ signal is applied to the MK 4096. Whenever $\overline{CAS}$ makes a negative transition, the output will go unconditionally open-circuited, independent of the state of any other input to the chip. If the cycle in progress is a read, read-modify-write, or a delayed write cycle and the chip is selected, then the output latch and buffer will again go active and at access time will contain the data read from the selected cell. This output data is the same polarity (not inverted) as the input data. If the cycle in progress is a write cycle ($\overline{WRITE}$ active low before $\overline{CAS}$ goes low) and the chip is selected, then at access time the output latch and buffer will contain a logic 1. Once having gone active, the output will remain valid until the MK 4096 receives the next $\overline{CAS}$ negative edge. Intervening refresh cycles in which a $\overline{RAS}$ is received (but no $\overline{CAS}$) will not cause valid data to be affected. Conversely, the output will assume the open-circuit state during any cycle in which the MK 4096 receives a $\overline{CAS}$ but no $\overline{RAS}$ signal (regardless of the state of any other inputs). The output will also assume the open-circuit state in normal cycles (in which both $\overline{RAS}$ and $\overline{CAS}$ signals occur) if the chip is unselected.

The three-state data output buffer presents the data output pin with a low impedance to V_{CC} for a logic 1 and a low impedance to V_{SS} for a logic 0. The effective resistance to V_{CC} (logic 1 state) is 500Ω maximum and 150Ω typically. The resistance to V_{SS} (logic 0 state) is 200Ω maximum and 100Ω typically. The separate V_{CC} pin allows the output buffer to be powered from the supply voltage of the logic to which the chip is interfaced. During battery standby operation, the V_{CC} pin may have power removed without affecting the MK 4096 refresh operation. This allows all system logic except the $\overline{RAS}/\overline{CAS}$ timing circuitry and the refresh address logic to be turned off during battery standby to conserve power.

REFRESH

Refresh of the dynamic cell matrix is accomplished by performing a memory cycle at each of the 64 row addresses within each 1 millisecond time interval. Any cycle in which a $\overline{RAS}$ signal occurs accomplishes a refresh operation. A read cycle will refresh the selected row, regardless of the Chip Select ($\overline{CS}$) input. A write or read-modify-write cycle also refreshes the selected row, but the chip should be unselected to prevent writing data into the selected cell.

For standby operation, a "$\overline{RAS}$-only" cycle can be employed to refresh the MK 4096. However, if "$\overline{RAS}$-only" refresh cycles (where $\overline{RAS}$ is the only signal applied to the chip) are continued for extended periods, the output buffer may eventually lose proper data and go open-circuit. Prior to the first memory cycle following a period (beyond 1ms) of "$\overline{RAS}$-only" refresh, a memory cycle employing both $\overline{RAS}$ and $\overline{CAS}$ must be performed to precharge the internal circuitry. This "dummy cycle" allows the output buffer to regain activity and enables the device to perform a read or write cycle upon command.

POWER DISSIPATION/STANDBY MODE

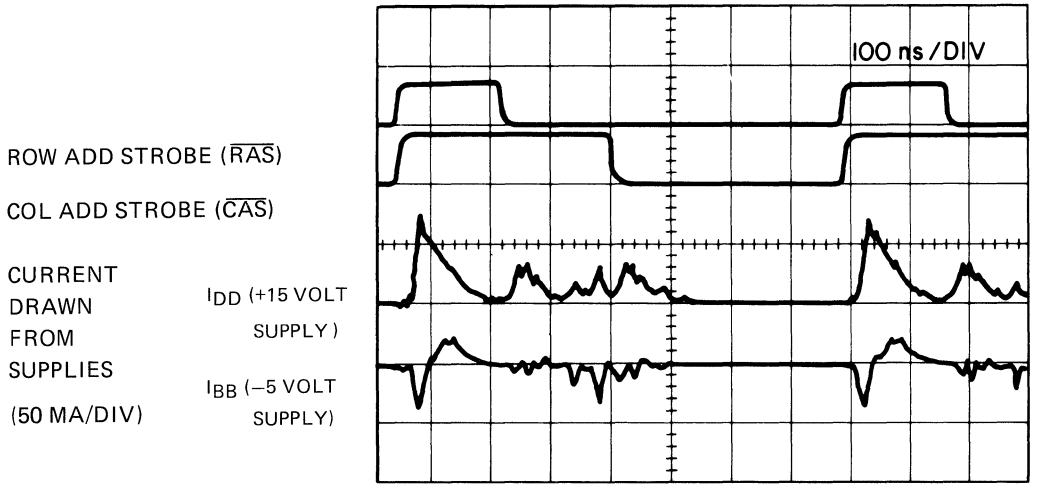
Most of the circuitry used in the MK 4096 is dynamic and most of the power drawn is the result of an address strobe edge. Because the power is not drawn during the whole time the strobe is active, the dynamic power is a function of operating frequency rather than active duty cycle. Typically, the power is 120 mW at a 1 μsec cycle rate for the MK 4096 with a maximum power of less than 550 mW at 500 nsec cycle time. To minimize the overall system power, the Row Address Strobe ($\overline{RAS}$) should be decoded and supplied to only the selected chips. The $\overline{CAS}$ must be supplied to all chips (to turn off the unselected output). Those chips that did not receive a $\overline{RAS}$, however, will not dissipate any power on the $\overline{CAS}$ edges, except for that required to turn off the outputs. If the $\overline{RAS}$ signal is decoded and supplied only to the selected chips, then the Chip Select ($\overline{CS}$) input of all chips can be at a logic 0. The chips that receive a $\overline{CAS}$ but no $\overline{RAS}$ will be unselected (output open-circuited) regardless of the Chip Select input. For refresh cycles, however, either the $\overline{CS}$ input of all chips must be high or the $\overline{CAS}$ input must be held high to prevent several "wire-ORed" outputs from turning on with opposing force.

The current waveforms for the current drawn from the V_{DD} and V_{BB} supplies are shown in Figure A. Since the current is pulsed, proper power distribution and bypassing techniques are required to maintain system power supply noise levels at an acceptable level. Low inductance supply lines for V_{DD} and V_{SS} are desirable. One 0.01 microfarad, low inductance, bypass capacitor per two MK 4096 devices and one 6.8 microfarad electrolytic capacitor per eight MK 4096 devices on each of the V_{DD} and V_{BB} supply lines is desirable.

POWER–UP

Under normal operating conditions the MK 4096 requires no particular power-up sequence. However, in order to achieve the most reliable performance from the MK 4096, proper consideration should be given to the V_{BB}/V_{DD} power supply relationship. The V_{BB} supply is an extremely important "protective voltage" since it performs two essential functions within the device. It establishes proper junction isolation and sets field-effect thresholds, both thin field and thick field. Misapplication of V_{BB} or device operation without the V_{BB} supply can affect long term device reliability. For optimum reliability performance from the MK 4096, it is suggested that measures be taken to not have V_{DD} (+15V) applied to the device for over five (5) seconds without the application of V_{BB} (–5V).

After power is applied to the device, the MK 4096 requires at least one memory cycle ($\overline{RAS}/\overline{CAS}$) before proper device operation is achieved. A normal 64 cycle refresh with both $\overline{RAS}$ and $\overline{CAS}$ is adequate for this purpose.



Power Supply Current Waveforms

SUPPLEMENT

MOSTEK

Extended Operating Temperature Range(−55°C to +85°C)

4096 × 1 Bit Dynamic RAM — MK 4096P-77/86/85

FEATURES

- ☐ Industry standard 16-pin DIP configuration (available in hermetic ceramic (P) package only)
- ☐ Extended operating temperature range (−55°C to + 85°C)
- ☐ All inputs are low capacitance and TTL compatible
- ☐ Input latches for address, chip select and data in
- ☐ Inputs protected against static charge
- ☐ Three-state TTL compatible output, latched and valid into next cycle
- ☐ Proven reliability with high performance

Part Number	Access Time	Cycle Time	Max Power*
MK 4096–77	250 ns	375 ns	570mW
MK 4096–86	300 ns	425 ns	500mW
MK 4096–85	350 ns	500 ns	450mW

*Standby power for all parts < 27mW

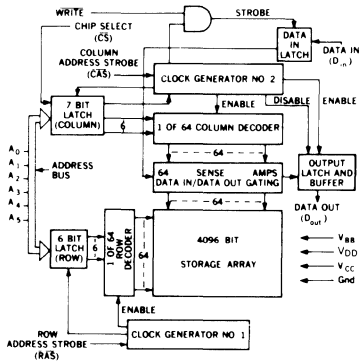
DESCRIPTION

The MK 4096 is the recognized industry standard 4096 word by 1 bit MOS Random Access Memory circuit packaged in a standard 16-pin DIP on 0.3 inch centers. This package configuration is made possible by a unique multiplexing and latching technique for the address inputs. The use of the 16-pin DIP for the MK 4096 provides high system bit densities and is compatible with widely available automated testing and insertion equipment.

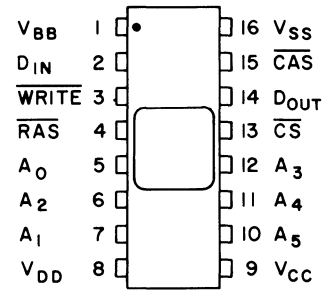
The MK 4096 is fabricated with MOSTEK's standard Self-Aligned, Poly-Interconnect, N-Channel (SPIN) process. The SPIN process allows the MK 4096 to be a highly manufacturable, state-of-the-art memory circuit that exhibits the reliability and performance standards necessary for today's (and tomorrow's) data processing applications. The MK 4096 employs a single transistor storage cell, utilizing a dynamic storage technique and dynamic control circuitry to achieve optimum performance with low power dissipation.

System oriented features incorporated within the MK 4096 include direct interfacing capability with TTL, 6 instead of 12 address lines to drive, on-chip registers which can eliminate the need for interface registers, input logic levels selected to optimize the noise immunity, and two chip select methods to allow the user to determine the speed/power characteristics of his memory system.

FUNCTIONAL DIAGRAM



PIN CONNECTIONS



PIN NAMES

A_0 - A_5	ADDRESS INPUTS	D_{IN}	DATA IN
$\overline{CAS}$	COLUMN ADDRESS STROBE	D_{OUT}	DATA OUT
$\overline{CS}$	CHIP SELECT	V_{BB}	POWER (−5V)
$\overline{RAS}$	ROW ADDRESS STROBE	V_{CC}	POWER (+5V)
$\overline{WRITE}$	READ/WRITE INPUT	V_{DD}	POWER (+12V)
		V_{SS}	GROUND

ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to V_{BB} . . . . −0.5V to + 25V
($V_{SS}-V_{BB} \geq 4.5V$
Operating temperature T_A (Ambient). . −55°C to + 85°C
Storage temperature (Ceramic) . . . . . −65°C to + 150°C
Power dissipation 1Watt
Data out current 50mA

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS (17)
($-55°C \leq T_A \leq +85°C$)

	PARAMETER	MK 4096P−77 MIN	MK 4096P−77 MAX	MK 4096P−86 MIN	MK 4096P−86 MAX	MK 4096P−85 MIN	MK 4096P−85 MAX	UNITS	NOT
V_{DD}	Supply Voltage	11.4	12.6	11.4	12.6	11.4	12.6	Volts	1
V_{CC}	Supply Voltage	V_{SS}	V_{DD}	V_{SS}	V_{DD}	V_{SS}	V_{DD}	Volts	1,2
V_{SS}	Supply Voltage	0	0	0	0	0	0	Volts	1
V_{BB}	Supply Voltage	−4.5	−5.5	−4.5	−5.5	−4.5	−5.5	Volts	1
V_{IHC}	Logic 1 Voltage − $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	2.7	7.0	2.7	7.0	3.0	7.0	Volts	1,3
V_{IH}	Logic 1 Voltage, all inputs except $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	2.4	7.0	2.4	7.0	2.4	7.0	Volts	1,3
V_{IL}	Logic 0 Voltage, all inputs	−1.0	0.8	−1.0	0.8	−1.0	0.8	Volts	1,3

DC ELECTRICAL CHARACTERISTICS (17)
($-55°C \leq T_A \leq +85°C$)($V_{DD}$ = 12.0V ± 5%; V_{CC} = 5.0V ± 10%; V_{SS} = 0V; V_{BB} = −5.0V ± 10%)

	PARAMETER	MK4096P-77 MIN	MK4096P-77 MAX	MK4096P-86 MIN	MK4096P-86 MAX	MK4096P-85 MIN	MK4096P-85 MAX	UNITS	NOTES
I_{DD1}	Average V_{DD} Power Supply Current		45		40		35	mA	4
I_{CC}	V_{CC} Power Supply Current							mA	5
I_{BB}	Average V_{BB} Power Supply Current		75		75		75	μA	
I_{DD2}	Standby V_{DD} Power Supply Current		2		2		2	mA	7
I_{DD3}	Average V_{DD} Supply Current during "$\overline{RAS}$-only" cycles		35		30		25	mA	4
$I_{I(L)}$	Input Leakage Current (any input)		5		5		5	μA	6
$I_{O(L)}$	Output Leakage Current		10		10		10	μA	7,8
V_{OH}	Output Logic 1 Voltage @ I_{OUT} = −5mA	2.4		2.4		2.4		Volts	2
V_{OL}	Output Logic 0 Voltage @ I_{OUT} = 2mA		0.4		0.4		0.4	Volts	

NOTES

1. All voltages referenced to V_{SS}. V_{BB} must be applied to and removed from the device within 5 seconds of V_{DD}.
2. Output voltage will swing from V_{SS} to V_{CC} if $V_{CC} \leq V_{DD} - 4$ volts. If $V_{CC} \geq V_{DD} - 4$ volts, the output will swing from V_{SS} to a voltage somewhat less than V_{DD}.
3. Device speed is not guaranteed at input voltages greater than TTL levels (0 to 5V).
4. Current is proportional to cycle rate; maximum current is measured at the fastest cycle rate.
5. I_{CC} depends upon output loading. The V_{CC} supply is connected to the output buffer only.
6. All device pins at 0 volts except V_{BB} which is at −5 volts and the pin under test which is at +10 volts.
7. Output is disabled (open-circuit) and $\overline{RAS}$ and $\overline{CAS}$ are both at a logic 1.
8. $0V \leq V_{OUT} \leq +10V$.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (10, 15,17)

($-55°C \leq T_A \leq +85°C$) ($V_{DD}$ = 12.0V ± 5%, V_{CC} = 5.0V ± 10%, V_{SS} = 0V, V_{BB} = −5.0V ± 10%)

		MK4096P-77		MK4096P-86		MK4096P-85			
	PARAMETER	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
t_{RC}	Random Read or Write Cycle Time	375		425		500		nsec	11
t_{RAC}	Access time from Row Address Strobe		250		300		350		11,13
t_{CAC}	Access Time from Column Address Strobe		140		165		200		12,13
t_{OFF}	Output Buffer Turn-Off Delay	0	65	0	80	0	100		
t_{RP}	Row Address Strobe Precharge Time	115		125		150			
t_{RAS}	Row Address Strobe Pulse Width	250	10,000	300	10,000	350	10,000		
t_{RCL}	Row To Column Strobe Lead Time	60	110	80	135	100	150		14
t_{CAS}	Column Address Strobe Pulse Width	140		165		200			12
t_{AS}	Address Set-Up Time	0		0		0			
t_{AH}	Address Hold Time	60		80		100			
t_{CH}	Chip Select Hold Time	100		100		100			
t_T	Rise and Fall Times	3	50	3	50	3	50		15
t_{RCS}	Read Command Set-Up Time	0		0		0			
t_{RCH}	Read Command Hold Time	0		0		0			
t_{WCH}	Write Command Hold Time	110		130		150			
t_{WP}	Write Command Pulse Width	110		130		150			
t_{CRL}	Column to Row Strobe Lead Time	−40	+40	−50	+50	−50	+50		
t_{CWL}	Write Command to Column Strobe Lead Time	110		130		150			
t_{DS}	Data In Set-Up Time	0		0		0			16
t_{DH}	Data In Hold Time	110		130		150			16
t_{RFSH}	Refresh Period		2		2		2	msec	
t_{MOD}	Modify Time		10		10		10	μsec	
t_{DOH}	Data Out Hold Time	10		10		10		μsec	

NOTES Continued

9. Capacitance measured with Boonton Meter or effective capacitance calculated from the equation: $C = \frac{I \Delta t}{\Delta V}$ with current equal to a constant 20mA.

10. A C measurements assume t_T = 5ns.

11. Assumes that $t_{RCL} + t_T \leq t_{RCL}$ (max).

12. Assumes that $t_{RCL} + t_T \geq t_{RCL}$ (max).

13. Measured with a load circuit equivalent to 1 TTL load and C_L = 100pF.

14. Operation within the t_{RCL} (max) limit insures that t_{RAC} (max) can be met. t_{RCL} (max) is specified as a reference point only; if t_{RCL} is greater than the specified t_{RCL} (max) limit, then access time is controlled exclusively by t_{CAC} and t_{RAS}, t_{RAC} and t_{RCL} will be longer by the amount $t_{RCL} + t_T$ exceeds t_{RCL} (max).

15. V_{IHC} (min) or V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IHC} or V_{IH} and V_{IL}.

16. These parameters are referenced to $\overline{CAS}$ leading edge in random write cycles and to $\overline{WRITE}$ leading edge in delayed write or read-modify-write cycles.

17. After the application of supply voltages or after extended periods of operation without clocks, the device must perform a minimum of one initialization cycle (any valid memory cycle containing both $\overline{RAS}$ and $\overline{CAS}$) prior to normal operation.

AC ELECTRICAL CHARACTERISTICS

($-55°C \leq T_A \leq +85°C$) ($V_{DD}$ = 12.0V ± 5%; V_{CC} = 5.0V ± 10%, V_{SS} = 0V, V_{BB} = −5.0V ± 10%)

	PARAMETER	TYP	MAX	UNITS	NOTES
C_{I1}	Input Capacitance ($A_0 - A_5$)	7	10	pF	9
C_{I2}	Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, D_{IN}, $\overline{WRITE}$, $\overline{CS}$)	5	7	pF	9
C_O	Output Capacitance (D_{OUT})	5	8	pF	7,9

MOSTEK

4096 X 1 BIT DYNAMIC RAM

MK 4200 (P/N)-11/16

FEATURES

- ☐ Industry standard 16-pin DIP configuration (available in plastic (N) and ceramic (P) packages)
- ☐ All inputs are low capacitance and TTL compatible, except RAS (MOS level)
- ☐ Input latches for address, chip select and data in
- ☐ Inputs protected against static charge
- ☐ Three-state TTL compatible output, latched and valid into next cycle
- ☐ Proven reliability with high performance

Part Number	Access Time	Cycle Time	Max Power*
MK 4200-16	300 ns	425 ns	380 mW
MK 4200-11	350 ns	500 ns	300 mW

*Standby power for all parts $<$.6 mW

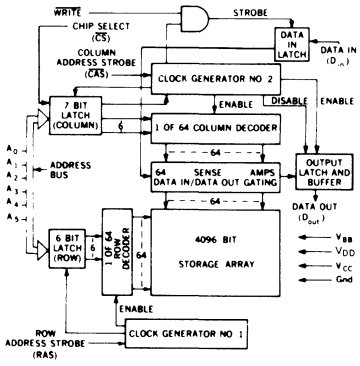
DESCRIPTION

The MK 4200 is a 4096 word by 1 bit MOS Random Access Memory circuit packaged in a standard 16-pin DIP on 0.3 inch centers. This package configuration is made possible by a unique multiplexing and latching technique for the address inputs. The use of the 16-pin DIP for the MK 4200 provides high system bit densities and is compatible with widely available automated testing and insertion equipment.

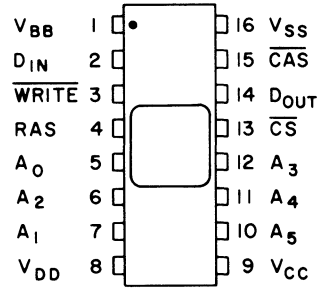
The MK 4200 is fabricated with MOSTEK's standard Self-Aligned, Poly-Interconnect, N-Channel (SPIN) process. The SPIN process allows the MK 4200 to be a highly manufacturable, state-of-the-art memory circuit that exhibits the reliability and performance standards necessary for today's (and tomorrow's) data processing applications. The MK 4200 employs a single transistor storage cell, utilizing a dynamic storage technique and dynamic control circuitry to achieve optimum performance with low power dissipation.

System oriented features incorporated within the MK 4200 include direct interfacing capability with TTL, 6 instead of 12 address lines to drive, on-chip registers which can eliminate the need for interface registers, input logic levels selected to optimize the noise immunity, and two chip select methods to allow the user to determine the speed/power characteristics of his memory system.

FUNCTIONAL DIAGRAM



PIN CONNECTIONS



PIN NAMES

A_0 - A_5	ADDRESS INPUTS	D_{IN}	DATA IN
$\overline{CAS}$	COLUMN ADDRESS STROBE	D_{OUT}	DATA OUT
$\overline{CS}$	CHIP SELECT	V_{BB}	POWER (–5V)
$\overline{RAS}$	ROW ADDRESS STROBE	V_{CC}	POWER (+5V)
$\overline{WRITE}$	READ/WRITE INPUT	V_{DD}	POWER (+12V)
		V_{SS}	GROUND

ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to V_{BB} . . . . −0.5V to + 25V
($V_{SS}-V_{BB} \geq 4.5V$)
Operating temperature T_A (Ambient) . . . . 0°C to + 70°C
Storage temperature (Ceramic) . . . . . −65°C to + 150°C
Storage temperature (Plastic) . . . . . −55°C to + 125°C
Power dissipation 1Watt
Data out current 50mA

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS (17)

($0°C \leq T_A \leq 70°C$)

	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{DD}	Supply Voltage	11.4	12.0	12.6	Volts	1
V_{CC}	Supply Voltage	V_{SS}	5.0	V_{DD}	Volts	1,2
V_{SS}	Supply Voltage	0	0	0	Volts	1
V_{BB}	Supply Voltage	−4.5	−5.0	−5.5	Volts	1
V_{IHC}	Logic 1 Voltage, $\overline{CAS}$, $\overline{WRITE}$	2.7	5.0	7.0	Volts	1,3
V_{IH}	Logic 1 Voltage, all inputs except RAS, $\overline{CAS}$, $\overline{WRITE}$	2.4	5.0	7.0	Volts	1,3
V_{IHR}	Logic 1 Voltage, RAS input	$V_{DD}-1$	12.0	$V_{DD}+1$	Volts	1
V_{IL}	Logic 0 Voltage, all inputs	−1.0	0	0.8	Volts	1,3

DC ELECTRICAL CHARACTERISTICS (17)

($0°C \leq T_A \leq 70°C$) (V_{DD} = 12.0V ± 5%; V_{CC} = 5.0V ± 10%; V_{SS} = 0V; V_{BB} = −5.0V ± 10%)

	PARAMETER	MK 4200-16 MIN	MK 4200-16 MAX	MK 4200-11 MIN	MK 4200-11 MAX	UNITS	NOTES
I_{DD1}	Average V_{DD} Power Supply Current		30		25	mA	4
I_{CC}	V_{CC} Power Supply Current					mA	5
I_{BB}	Average V_{BB} Power Supply Current		75		75	µA	
I_{DD2}	Standby V_{DD} Power Supply Current		50		50	µA	7
I_{DD3}	Average V_{DD} Supply Current during "RAS-only" cycles		22		18	mA	4
$I_{I(L)}$	Input Leakage Current (any input)		5		5	µA	6
$I_{O(L)}$	Output Leakage Current		10		10	µA	7,8
V_{OH}	Output Logic 1 Voltage @ I_{OUT} = −5mA	2.4		2.4		Volts	2
V_{OL}	Output Logic 0 Voltage @ I_{OUT} = 2mA		0.4		0.4	Volts	

NOTES

1. All voltages referenced to V_{SS}. V_{BB} must be applied to and removed from the device within 5 seconds of V_{DD}.
2. Output voltage will swing from V_{SS} to V_{CC} if $V_{CC} \leq V_{DD}-4$ volts. If $V_{CC} \geq V_{DD}-4$ volts, the output will swing from V_{SS} to a voltage somewhat less than V_{DD}.
3. Device speed is not guaranteed at input voltages greater than TTL levels (0 to 5V).
4. Current is proportional to cycle rate; maximum current is measured at the fastest cycle rate.
5. I_{CC} depends upon output loading. The V_{CC} supply is connected to the output buffer only.
6. All device pins at 0 volts except V_{BB} which is at −5 volts and the pin under test which is at +10 volts.
7. Output is disabled (open-circuit); RAS = V_{IL} and $\overline{CAS}$ = V_{IHC}.
8. $0V \leq V_{OUT} \leq +10V$.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (10, 15,17)

(0°C ≤ T_A ≤ 70°C) (V_{DD} = 12.0V ± 5%, V_{CC} = 5.0V ± 10%, V_{SS} = 0V, V_{BB} = −5.0V ± 10%)

	PARAMETER	MK 4200-16 MIN	MK 4200-16 MAX	MK 4200-11 MIN	MK 4200-11 MAX	UNITS	NOTES
t_{RC}	Random Read or Write Cycle Time	425		500		nsec	11
t_{RAC}	Access time from Row Address Strobe		300		350	nsec	11,13
t_{CAC}	Access Time from Column Address Strobe		165		200	nsec	12,13
t_{OFF}	Output Buffer Turn-Off Delay	0	80	0	100	nsec	
t_{RP}	Row Address Strobe Precharge Time	125		150		nsec	
t_{RAS}	Row Address Strobe Pulse Width	300	10,000	350	10,000	nsec	
t_{RCL}	Row To Column Strobe Lead Time	80	135	100	150	nsec	14
t_{CAS}	Column Address Strobe Pulse Width	165		200		nsec	12
t_{AS}	Address Set-Up Time	0		0		nsec	
t_{AH}	Address Hold Time	80		100		nsec	
t_{CH}	Chip Select Hold Time	100		100		nsec	
t_T	Rise and Fall Times	3	50	3	50	nsec	15
t_{RCS}	Read Command Set-Up Time	0		0		nsec	
t_{RCH}	Read Command Hold Time	0		0		nsec	
t_{WCH}	Write Command Hold Time	130		150		nsec	
t_{WP}	Write Command Pulse Width	130		150		nsec	
t_{CRL}	Column to Row Strobe Lead Time	−50	+50	−50	+50	nsec	
t_{CWL}	Write Command to Column Strobe Lead Time	130		150		nsec	
t_{DS}	Data In Set-Up Time	0		0		nsec	16
t_{DH}	Data In Hold Time	130		150		nsec	16
t_{RFSH}	Refresh Period		2		2	msec	
t_{MOD}	Modify Time		10		10	μsec	
t_{DOH}	Data Out Hold Time	10		10		μsec	

NOTES Continued

9. Capacitance measured with Boonton Meter or effective capacitance calculated from the equation: $C = I\frac{\Delta t}{\Delta V}$ with current equal to a constant 20mA.

10. A C measurements assume t_T = 5ns.

11. Assumes that $t_{RCL} + t_T \leq t_{RCL}$ (max).

12. Assumes that $t_{RCL} + t_T \geq t_{RCL}$ (max).

13. Measured with a load circuit equivalent to 1 TTL load and C_L = 100pF.

14. Operation within the t_{RCL} (max) limit insures that t_{RAC} (max) can be met. t_{RCL} (max) is specified as a reference point only; if t_{RCL} is greater than the specified t_{RCL} (max) limit, then access time is controlled exclusively by t_{CAC} and t_{RAS}, t_{RAC} and t_{RCL} will be longer by the amount $t_{RCL} + t_T$ exceeds t_{RCL} (max).

15. V_{IHC} or V_{IHR} or V_{IH} and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IHC} or V_{IHR} or V_{IH} and V_{IL}.

16. These parameters are referenced to $\overline{CAS}$ leading edge in random write cycles and to $\overline{WRITE}$ leading edge in delayed write or read-modify-write cycles.

17. After the application of supply voltages or after extended periods of operation without clocks, the device must perform a minimum of one initialization cycles (any valid memory cycle containing both RAS and $\overline{CAS}$) prior to normal operation.

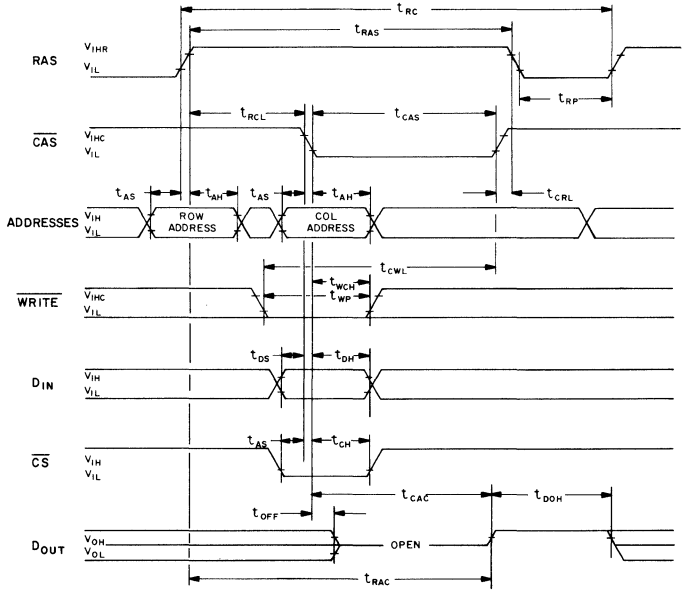
AC ELECTRICAL CHARACTERISTICS

(0℃ ≤ T_A ≤ + 70℃) (V_{DD} = 12.0V ± 5%, V_{CC} = 5.0V ±10%, V_{SS} = 0V, V_{BB} = –5.0V ± 10%)

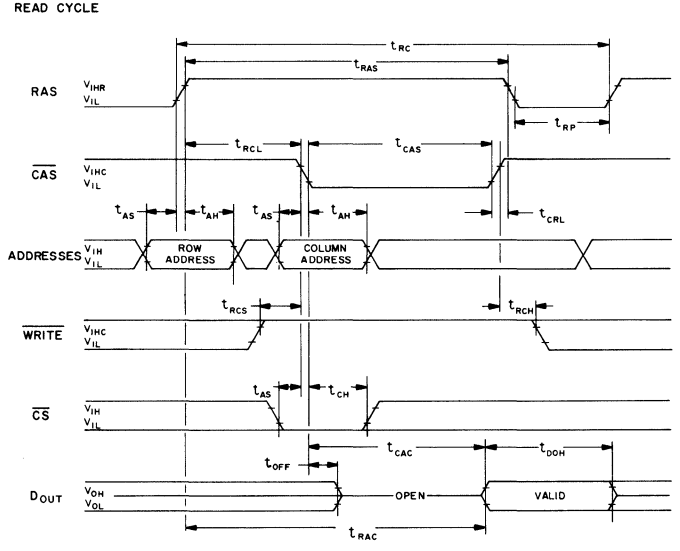
	PARAMETER	TYP	MAX	UNITS	NOTES
C_{I1}	Input Capacitance ($A_0 - A_5$)	7	10	pF	9
C_{I2}	Input Capacitance (RAS, $\overline{CAS}$, D_{IN}, $\overline{WRITE}$, $\overline{CS}$)	5	7	pF	9
C_O	Output Capacitance (D_{OUT})	5	8	pF	7,9

TIMING WAVEFORMS

WRITE CYCLE

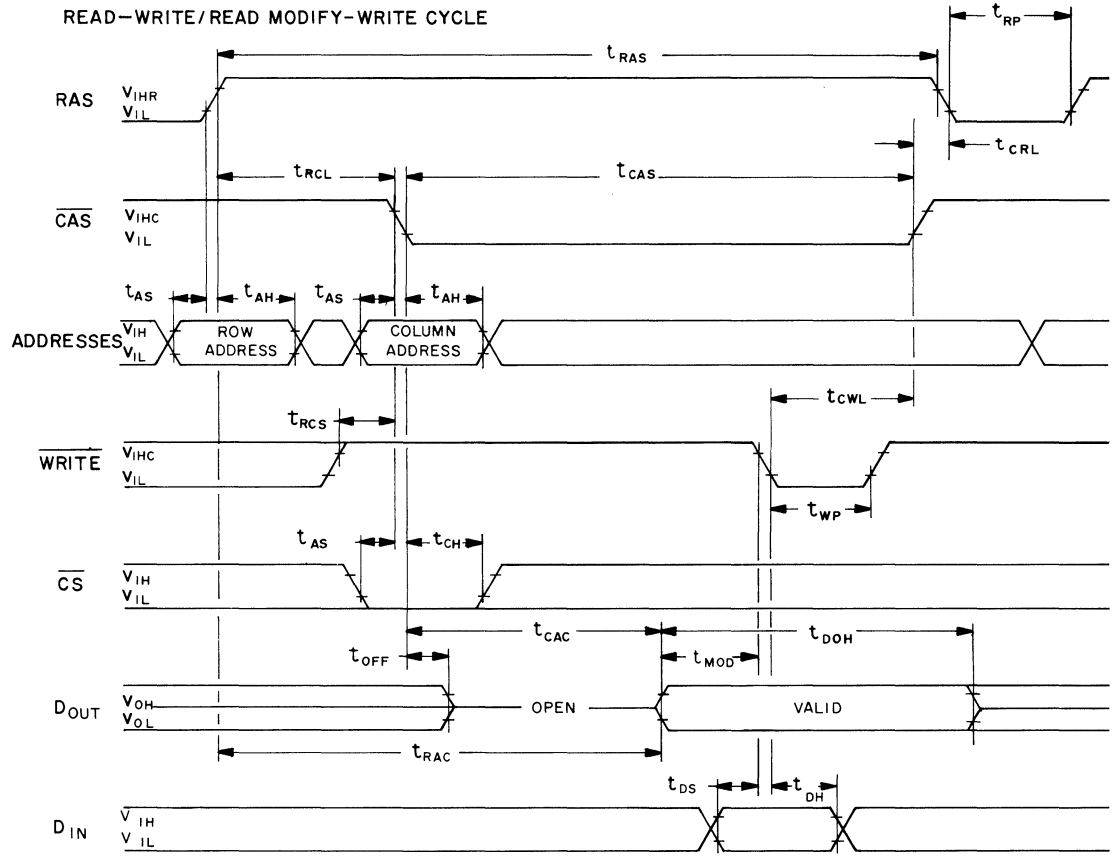


READ CYCLE

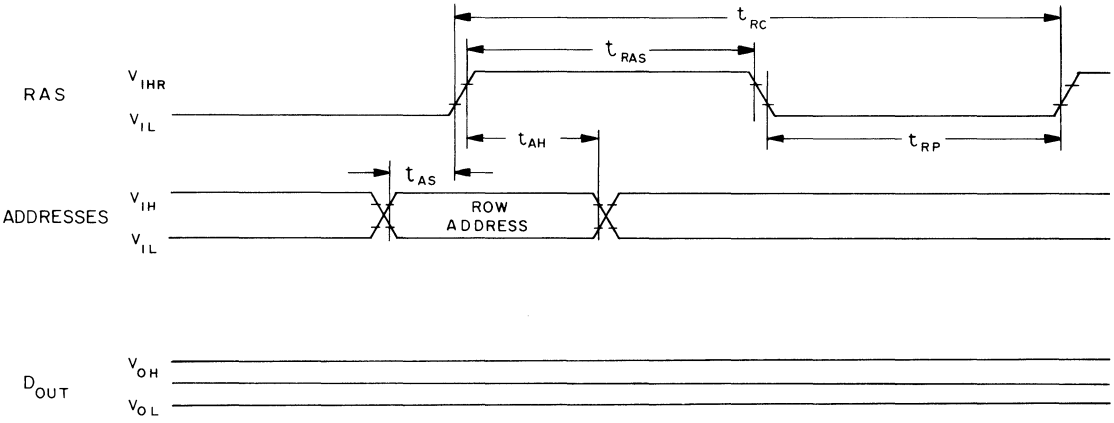


TIMING WAVEFORMS

READ–WRITE/READ MODIFY-WRITE CYCLE



"RAS ONLY" REFRESH CYCLE



NOTE:

Prior to the first memory cycle following a period (beyond 2mS) of "RAS-only refresh, a memory cycle employing both RAS and $\overline{CAS}$ must be performed to insure proper device operation.

ADDRESSING

The 12 address bits required to decode one of the 4096 cell locations within the MK 4200 are multiplexed onto the 6 address inputs and latched into the on-chip address latches by externally applying a positive going MOS level clock and a negative going TTL level clock. The first clock, the Row Address Strobe (RAS), latches the 6 row address bits into the chip. The second clock, the Column Address Strobe ($\overline{CAS}$), subsequently latches the 6 column address bits plus Chip Select ($\overline{CS}$) into the chip. (Note that since the Chip Select signal is not required until $\overline{CAS}$ time, which is well into the memory cycle its decoding time does not add to system access or cycle time). Each of these signals, RAS and $\overline{CAS}$, triggers a sequence of events which are controlled by different delayed internal clocks. The two clock chains are linked together logically in such a way that the address multiplexing operation is done outside of the critical path timing sequence for read data access. The later events in the $\overline{CAS}$ clock sequence are inhibited until the occurrence of a delayed signal derived from the RAS clock chain. This "gated $\overline{CAS}$" feature allows the $\overline{CAS}$ clock to be externally activated as soon as the Row Address Hold Time specification (t_{AH}) has been satisfied and the 6 address inputs have been changed from Row address to Column address information.

Note that $\overline{CAS}$ can be activated at any time after t_{AH} and it will have no effect on the worst case data access time (t_{RAC}) up to the point in time when the delayed row clock no longer inhibits the remaining sequence of column clocks. Two timing end points result from the internal gating of $\overline{CAS}$ which are called t_{RCL} (min) and t_{RCL} (max). No data storage or reading errors will result if $\overline{CAS}$ is applied to the MK 4200 at a point in time beyond the t_{RCL} (max) limit. However, access time will then be determined exclusively by the access time from $\overline{CAS}$ (t_{CAC}) rather than from RAS (t_{RAC}), and access time from RAS will be lengthened by the amount that t_{RCL} exceeds the t_{RCL} (max) limit.

INPUT LEVELS

All inputs to the MK 4200 except address strobe (RAS) are TTL compatible. The RAS input has been specially designed so that very little steady state (DC) power is dissipated by the MK 4200 while in standby operation. In doing this, the RAS input requires a high level signal to activate the chip. The RAS input driver must be able to change the capacitance load of the RAS input from within 8 volt at V_{SS} (0V) to within 1 volt of V_{DD} (+12).

DATA INPUT/OUTPUT

Data to be written into a selected cell is latched into an on-chip register by a combination of $\overline{WRITE}$ and $\overline{CAS}$ while RAS is active. The later of the signals ($\overline{WRITE}$ or $\overline{CAS}$) to make its negative transition is the strobe for the Data In register. This permits several options in the write cycle timing. In a write cycle, if the $\overline{WRITE}$ input is brought low prior to $\overline{CAS}$, the Data In is strobed by $\overline{CAS}$, and the set-up and hold times are referenced to $\overline{CAS}$. If the data input is not available at $\overline{CAS}$ time or if it is desired that the cycle be a read-write or read-modify-write cycle, the $\overline{WRITE}$ signal must be delayed until after $\overline{CAS}$. In this "delayed write cycle" the data input set-up and hold times are referenced to the negative edge of $\overline{WRITE}$ rather than to $\overline{CAS}$.

(To illustrate this feature, Data In is referenced to $\overline{WRITE}$ in the timing diagram depicting the read-modify-write cycle while the "early write" cycle diagram shows Data In referenced to $\overline{CAS}$). Note that if the chip is unselected ($\overline{CS}$ high at $\overline{CAS}$ time) $\overline{WRITE}$ commands are not executed and, consequently, data stored in the memory is unaffected.

Data is retrieved from the memory in a read cycle by maintaining $\overline{WRITE}$ in the inactive or high state throughout the portion of the memory cyle in which $\overline{CAS}$ is active. Data read from the selected cell will be available at the output within the specified access time.

DATA OUTPUT LATCH

Any change in the condition of the Data Out Latch is initiated by the $\overline{CAS}$ signal. The output buffer is not affected by memory (refresh) cycles in which only the RAS signal is applied to the MK 4200. Whenever $\overline{CAS}$ makes a negative transition, the output will go unconditionally open-circuited, independent of the state of any other input to the chip. If the cycle in progress is a read, read-modify-write, or a delayed write cycle and the chip is selected, then the output latch and buffer will again go active and at access time will contain the data read from the selected cell. This output data is the same polarity (not inverted) as the input data. If the cycle in progress is a write cycle ($\overline{WRITE}$ active low before $\overline{CAS}$ goes low) and the chip is selected, then at access time the output latch and buffer will contain a logic 1. Once having gone active, the output will remain valid until the MK 4200 receives the next $\overline{CAS}$ negative edge. Intervening refresh cycles in which a RAS is received (but no $\overline{CAS}$) will not cause valid data to be affected. Conversely, the output will assume the open-circuit state during any cycle in which the MK 4200 receives a $\overline{CAS}$ but no RAS signal (regardless of the state of any other inputs). The output will also assume the open-circuit state in normal cycles (in which both RAS and $\overline{CAS}$ signals occur) if the chip is unselected.

The three-state data output buffer presents the data output pin with a low impedance to V_{CC} for a logic 1 and a low impedance to V_{SS} for a logic 0. The effective resistance to V_{CC} (logic 1 state) is 500Ω maximum and 150Ω typically. The resistance to V_{SS} (logic 0 state) is 200Ω maximum and 100Ω typically. The separate V_{CC} pin allows the output buffer to be powered from the supply voltage of the logic to which the chip is interfaced. During battery standby operation, the V_{CC} pin may have power removed without affecting the MK 4200 refresh operation. This allows all system logic except the RAS/$\overline{CAS}$ timing circuitry and the refresh address logic to be turned off during battery standby to conserve power.

REFRESH

Refresh of the dynamic cell matrix is accomplished by performing a memory cycle at each of the 64 row addresses within each 2 millisecond time interval. Any cycle in which a RAS signal occurs accomplishes a refresh operation. A read cycle will refresh the selected row, regardless of the Chip Select ($\overline{CS}$) input. A write or read-modify-write cycle also refreshes the selected row, but the chip should be unselected to

prevent writing data into the selected cell.

For standby operation, a "RAS-only" cycle can be employed to refresh the MK 4200. However, if "RAS-only" refresh cycles (where RAS is the only signal applied to the chip) are continued for extended periods, the output buffer may eventually lose proper data and go open-circuit. Prior to the first memory cycle following a period (beyond 2ms) of "RAS-only" refresh, a memory cycle employing both RAS and $\overline{CAS}$ must be performed to precharge the internal circuitry. This "dummy cycle" allows the output buffer to regain activity and enables the device to perform a read or write cycle upon command.

POWER DISSIPATION/STANDBY MODE

Most of the circuitry used in the MK 4200 is dynamic and most of the power drawn is the result of an address strobe edge. Because the power is not drawn during the whole time the strobe is active, the dynamic power is a function of operating frequency rather than active duty cycle. Typically, the power is 120 mW at a 1 μsec cycle rate for the MK 4200 with a maximum power of less than 450 mW at 375 nsec cycle time. To minimize the overall system power, the Row Address Strobe (RAS) should be decoded and supplied to only the selected chips. The $\overline{CAS}$ must be supplied to all chips (to turn off the unselected output). Those chips that did not receive a RAS, however, will not dissipate any power on the $\overline{CAS}$ edges, except for that required to turn off the outputs. If the RAS signal is decoded and supplied only to the selected chips, then the Chip Select ($\overline{CS}$) input of all chips can be at a logic 0. The chips that receive a $\overline{CAS}$ but no RAS will be unselected (output open-circuited) regardless of the Chip Select input. For refresh cycles, however, either the $\overline{CS}$ input of all chips must be high or the $\overline{CAS}$ input must be held high to prevent several "wire-ORed)" outputs from turning on with opposing force.

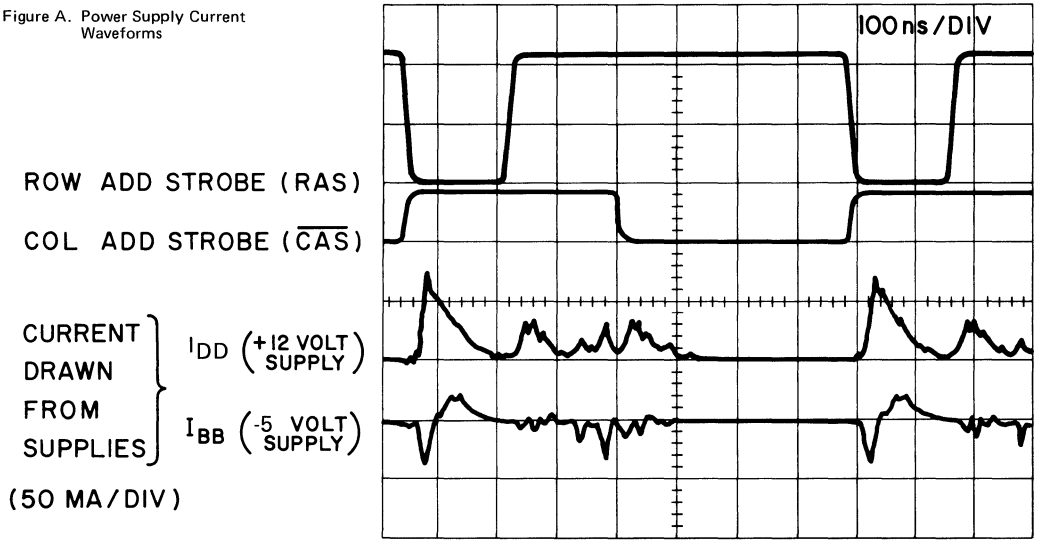
The current waveforms for the current drawn from the V_{DD} and V_{BB} supplies are shown in Figure A. Since the current is pulsed, proper power distribution and bypassing techniques are required to maintain system power supply noise levels at an acceptable level. Low inductance supply lines for V_{DD} and V_{SS} are desirable. One 0.01 microfarad, low inductance, bypass capacitor per two MK 4200 devices and one 6.8 microfarad electrolytic capacitor per eight MK 4200 devices on each of the V_{DD} and V_{BB} supply lines is desirable.

POWER–UP

Under normal operating conditions the MK 4200 requires no particular power-up sequence. However, in order to achieve the most reliable performance from the MK 4200, proper consideration should be given to the V_{BB}/V_{DD} power supply relationship. The V_{BB} supply is an extremely important "protective voltage" since it performs two essential functions within the device. It establishes proper junction isolation and sets field-effect thresholds, both thin field and thick field. Misapplication of V_{BB} or device operation without the V_{BB} supply can affect long term device reliability. For optimum reliability performance from the MK 4200, it is suggested that measures be taken to not have V_{DD} (+12V) applied to the device for over five (5) seconds without the application of V_{BB} (–5V).

After power is applied to the device, the MK 4200 requires at least one memory cycle (RAS/$\overline{CAS}$) before proper device operation is achieved. A normal 64 cycle refresh with both RAS and $\overline{CAS}$ is adequate for this purpose.

Figure A. Power Supply Current Waveforms



MOSTEK

4096 x 1-BIT DYNAMIC RAM

MK 4227 (P/N)-2/3/4

FEATURES

- ☐ Industry standard 16-pin DIP (MK 4096) configuration
- ☐ All inputs are low capacitance and TTL compatible, except RAS (MOS level)
- ☐ ±10% tolerance on all supplies (+12V, ±5V)
- ☐ Improved performance with "gated $\overline{CAS}$", "RAS only" refresh and page mode capability
- ☐ Input latches for addresses, chip select and data in
- ☐ Three-state TTL compatible output
- ☐ Output data latched and valid into next cycle
- ☐ Proven Reliability with high performance
- ☐ Standby power for all parts 1.3 mW (max).

Part Number	Access Time	Cycle Time	Max Power
MK 4227-2	150ns	320ns	462mW
MK 4227-3	200ns	375ns	462mW
MK 4227-4	250ns	375ns	462mW

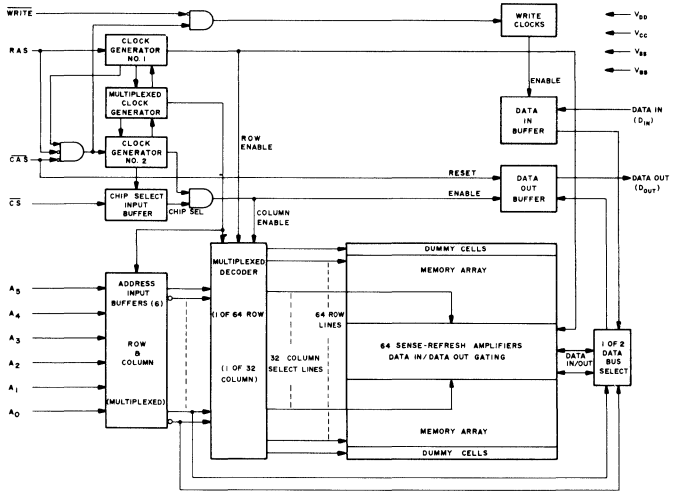
DESCRIPTION

The MK 4227 is a 4096 word by 1 bit MOS random access memory circuit fabricated with MOSTEK's N-channel silicon gate process. This process allows the MK 4227 to be a high performance state-of-the-art memory circuit that is manufacturable in high volume. The MK 4227 employs a single transistor storage cell utilizing a dynamic storage technique and dynamic control circuitry to achieve optimum performance with low power dissipation.

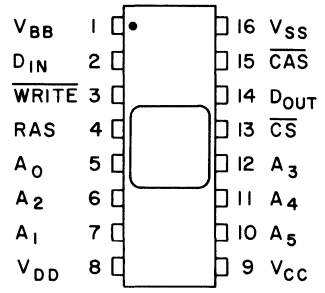
A unique multiplexing and latching technique for the address inputs permits the MK 4227 to be packaged in a standard 16-pin DIP on 0.3 in. centers. This package size provides high system-bit densities and is compatible with widely available automated testing and insertion equipment.

System oriented features include direct interfacing capability with TTL, only 6 very low capacitance address lines to drive, on-chip address and data registers which elimates the need for interface registers, input logic levels selected to optimize noise immunity, and two chip select methods to allow the user to determine the appropriate speed/power characteristics of his memory system. The MK 4227 also incorporates several flexible operating modes. In addition to the usual read and write cycles, read-modify write, page-mode, and RAS-only refresh cycles are available with the MK 4227. Page-mode timing is very useful in systems requiring Direct Memory Access (DMA) operation.

FUNCTIONAL DIAGRAM



PIN CONNECTIONS



PIN NAMES

A_0-A_5	ADDRESS INPUTS
$\overline{CAS}$	COLUMN ADDRESS STROBE
$\overline{CS}$	CHIP SELECT
D_{IN}	DATA IN
D_{OUT}	DATA OUT
$\overline{RAS}$	ROW ADDRESS STROBE
$\overline{WRITE}$	READ/WRITE INPUT
V_{BB}	POWER (−5V)
V_{CC}	POWER (+5V)
V_{DD}	POWER (+ 12V)
V_{SS}	GROUND

ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to V_{BB} ..... −0.5V to +20V
Voltage on V_{DD}, V_{CC} relative to V_{SS} ..... −1.0V to +15V
V_{BB}−V_{SS} (V_{DD}−V_{SS} > 0) 0V
Operating temperature, T_A (Ambient) ..... 0°C to + 70°C
Storage temperature (Ambient) (Ceramic) ..... −65°C to + 150°C
Storage temperature (Ambient) (Plastic) ..... −55°C to +125°C
Short Circuit Output Current 50mA
Power dissipation ..... 1 Watt

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS [4]
($0°C \leqslant T_A \leqslant 70°C$) [1]

	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{DD}	Supply Voltage	10.8	12.0	13.2	volts	2
V_{CC}	Supply Voltage	4.5V	5.0	5.5	volts	2,3
V_{SS}	Supply Voltage	0	0	0	volts	2
V_{BB}	Supply Voltage	−4.5	−5.0	−5.5	volts	2
V_{IHC}	Logic 1 Voltage, CAS, WRITE	2.4		7.0	volts	2
V_{IH}	Logic 1 Voltage, all inputs except RAS, CAS, WRITE	2.2		7.0	volts	2
V_{IL}	Logic 0 Voltage, all inputs	−1.0		.8	volts	2
V_{IHR}	Logic 1 Voltage, RAS input	V_{DD}−1.0	12.0	V_{DD} +3	volts	2

DC ELECTRICAL CHARACTERISTICS [4]
($0°C \leqslant T_A \leqslant 70°C$)[1] ($V_{DD}$ = 12.0V ± 10%; V_{CC} = 5.0V ± 10%; V_{SS} = 0V; V_{BB} = −5.0V ± 10%)

	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
I_{DD1}	Average V_{DD} Power Supply Current			35	mA	5
I_{DD2}	Standby V_{DD} Power Supply Current			100	µA	8
I_{DD3}	Average V_{DD} Power Supply Current during "RAS only" cycles			25	mA	
I_{CC}	V_{CC} Power Supply Current				mA	6
I_{BB}	Average V_{BB} Power Supply Current			100	µA	
$I_{I(L)}$	Input Leakage Current (any input)			10	µA	7
$I_{O(L)}$	Output Leakage Current			10	µA	8,9
V_{OH}	Output Logic 1 Voltage @ I_{OUT} = −5mA	2.4			volts	
V_{OL}	Output Logic 0 Voltage @ I_{OUT} = 3.2mA			0.4	volts	

NOTES

1. T_A is specified for operation at frequencies to $t_{RC} \geqslant t_{RC}$ (min). Operation at higher cycle rates with reduced ambient temperatures and higher power dissipation is permissible provided that all AC parameters are met. See figure 2 for derating curve.
2. All voltages referenced to V_{SS}.
3. Output voltage will swing from V_{SS} to V_{CC} when enabled,with no output load. For purposes of maintaining data in standby mode, V_{CC} may be reduced to V_{SS} without affecting refresh operations or data retention. However, the V_{OH} (min) specification is not guaranteed in this mode.
4. Several cycles are required after power-up before proper device operation is achieved. Any 8 cycles which perform refresh are adequate for this purpose.
5. Current is proportional to cycle rate. I_{DD1} (max) is measured at the cycle rate specified by t_{RC} (min. See figure 1 for I_{DD1} limits at other cycle rates. The following equations may be used to calculate I_{DD1} (max) at other cycle rates.
   MK 4227-3/4 I_{DD1} (max) [mA] = 10.0 + 9.30 x Cycle rate (MHz)
   MK 4227-2 I_{DD1} (max) [mA] = 10.0 + 8.0 x Cycle rate (MHz)
6. I_{CC} depends on output loading. During readout of high level data V_{CC} is connected through a low impedance (135Ω typ) to **Data Out**. At all other times I_{CC} consists of leakage currents only.
7. All device pins at 0 volts except V_{BB} which is at −5 volts and the pin under test which is at +10 volts.
8. Output is disabled (high-impedance) and RAS and $\overline{CAS}$ are both at a logic 1. Transient stabilization is required prior to measurement of this parameter.
9. $0V \leqslant V_{OUT} \leqslant +10V$.
10. Effective capacitance is calculated from the equation:
    $C = \frac{\Delta Q}{\Delta V}$ with ΔV = 3 volts.
11. A.C. measurements assume t_T = 5ns.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (4,11,17)

($0°C \leq T_A \leq 70°C$)[1] (V_{DD} = 12.0V ± 10%, V_{CC} = 5.0V ± 10%, V_{SS} = 0V, V_{BB} = −5.0V ± 10%)

		MK 4227-2		MK 4227-3		MK 4227-4			
	PARAMETER	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
t_{RC}	Random read or write cycle time	320		375		375		ns	12
t_{RWC}	Read write cycle time	330		420		480		ns	12
t_{RAC}	Access time from row address strobe		150		200		250	ns	13,15
t_{CAC}	Access time from column address strobe		100		135		165	ns	14,15
t_{OFF}	Output buffer turn-off delay		40		50		60	ns	
t_{RP}	Row address strobe precharge time	100		120		120		ns	
t_{RAS}	Row address strobe pulse width	150	10,000	200	10,000	250	10,000	ns	
t_{RSH}	Row address strobe hold time	100		135		165		ns	
t_{CAS}	Column address strobe pulse width	100		135		165		ns	
t_{RCD}	Row to column strobe delay	20	50	25	65	35	85	ns	16
t_{ASR}	Row address set-up time	0		0		0		ns	
t_{RAH}	Row address hold time	20		25		35		ns	
t_{ASC}	Column address set-up time	−10		−10		−10		ns	
t_{CAH}	Column address hold time	45		55		75		ns	
t_{AR}	Column address hold time referenced to RAS	95		120		160		ns	
t_{CSC}	Chip select set-up time	−10		−10		−10		ns	
t_{CH}	Chip select hold time	45		55		75		ns	
t_{CHR}	Chip select hold time referenced to RAS	95		120		160		ns	
t_T	Transition time (rise and fall)	3	35	3	50	3	50	ns	17
t_{RCS}	Read command set-up time	0		0		0		ns	
t_{RCH}	Read command hold time	0		0		0		ns	
t_{WCH}	Write command hold time	45		55		75		ns	
t_{WCR}	Write command hold time referenced to RAS	95		120		160		ns	
t_{WP}	Write command pulse width	45		55		75		ns	
t_{RWL}	Write command to row strobe lead time	50		70		85		ns	
t_{CWL}	Write command to column strobe lead time	50		70		85		ns	
t_{DS}	Data in set-up time	0		0		0		ns	18
t_{DH}	Data in hold time	45		55		75		ns	18
t_{DHR}	Data in hold time referenced to RAS	95		120		160		ns	
t_{CRP}	Column to row strobe precharge time	0		0		0		ns	
t_{CP}	Column precharge time	60		80		110		ns	
t_{RFSH}	Refresh period		2		2		2	ms	
t_{WCS}	Write command set-up time	0		0		0			19
t_{CWD}	$\overline{CAS}$ to $\overline{WRITE}$ delay	60		80		90		ns	19
t_{RWD}	RAS to $\overline{WRITE}$ delay	110		145		175		ns	19
t_{DOH}	Data out hold time	10		10		10		μs	

Notes Continued

12. The specifications for t_{RC} (min) and t_{RWC} (min) are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \leq T_A \leq 70°C$) is assured. See figure 2 for derating curve.

13. Assumes that $t_{RCD} \leq t_{RCD}$ (max).

14. Assumes that $t_{RCD} \geq t_{RCD}$ (max).

15. Measured with a load circuit equivalent to 2 TTL loads and 100pF

16. Operation within the t_{RCD} (max) limit insures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.

17. V_{IHC} (min), V_{IHR} (Min) or V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also transition times are measured between V_{IHC}, V_{IHR} or V_{IH} and V_{IL}.

18. These parameters are referenced to $\overline{CAS}$ leading edge in random write cycles and to $\overline{WRITE}$ leading edge in delayed write or read-modify-write cycles.

19. t_{WCS}, t_{CWD}, and t_{RWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only: If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and Data Out will contain the data written into the selected cell. If $t_{CWD} \geq t_{CWD}$ (min) and $t_{RWD} \geq t_{RWD}$ (min), the cycle is a read-write cycle and Data Out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of Data Out (at access time) is indeterminate.

AC ELECTRICAL CHARACTERISTICS

($0°C \leq T_A \leq 70°C$) ($V_{DD} = 12.0V \pm 10\%$; $V_{SS} = 0V$; $V_{BB} = -5.0V \pm 10\%$)

	PARAMETER	TYP	MAX	UNITS	NOTES
C_{I1}	Input Capacitance (A_0-A_5), D_{IN}, $\overline{CS}$	4	5	pF	10
C_{I2}	Input Capacitance RAS, $\overline{CAS}$, $\overline{WRITE}$	8	10	pF	10
C_O	Output Capacitance (D_{OUT})	5	7	pF	8,10

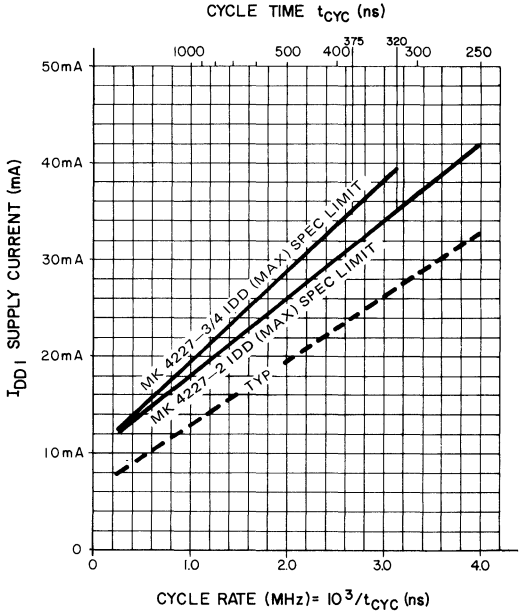


Figure 1. Maximum I_{DD1} versus cycle rate for device operation at extended frequencies.

MK 4227-3/4 I_{DD1} (max) [mA] = 10.0 + 9.30 x Cycle rate (MHz)
MK 4227-2 I_{DD1} (max) [mA] = 10.0 + 8.0 x Cycle rate (MHz)

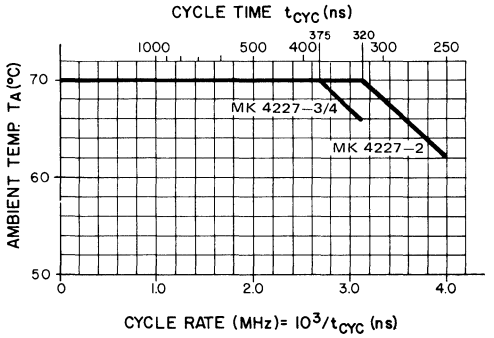
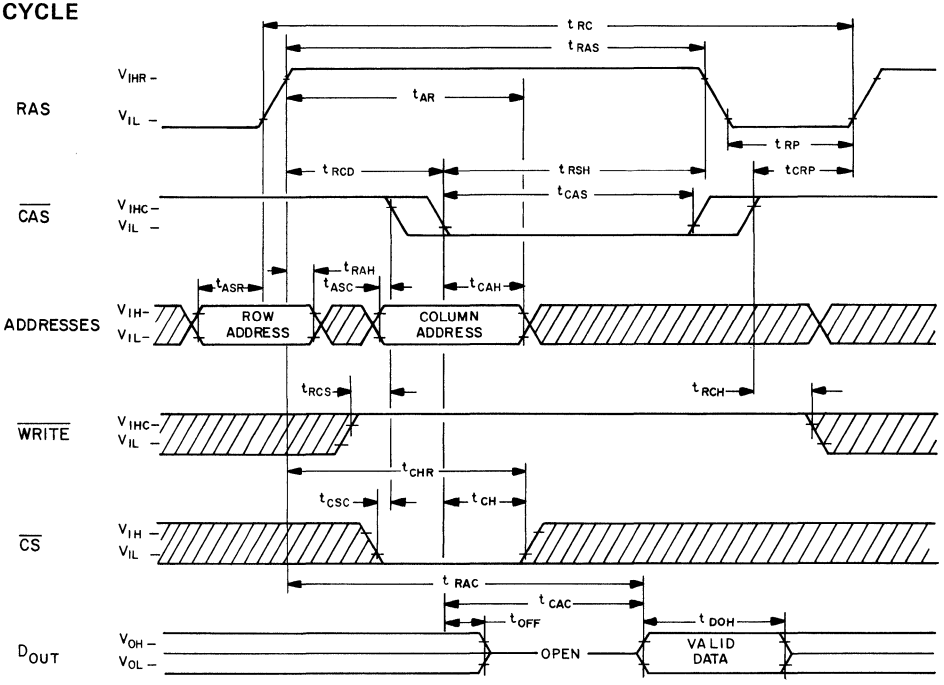
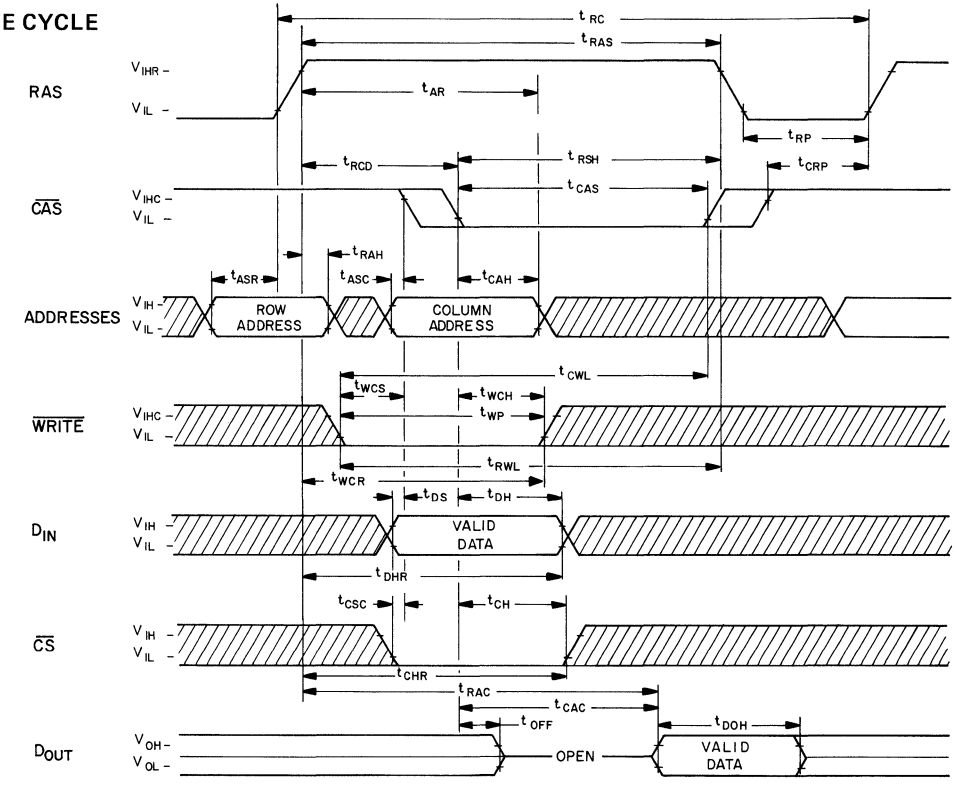


Figure 2. Maximum ambient temperature versus cycle rate for extended frequency operation.

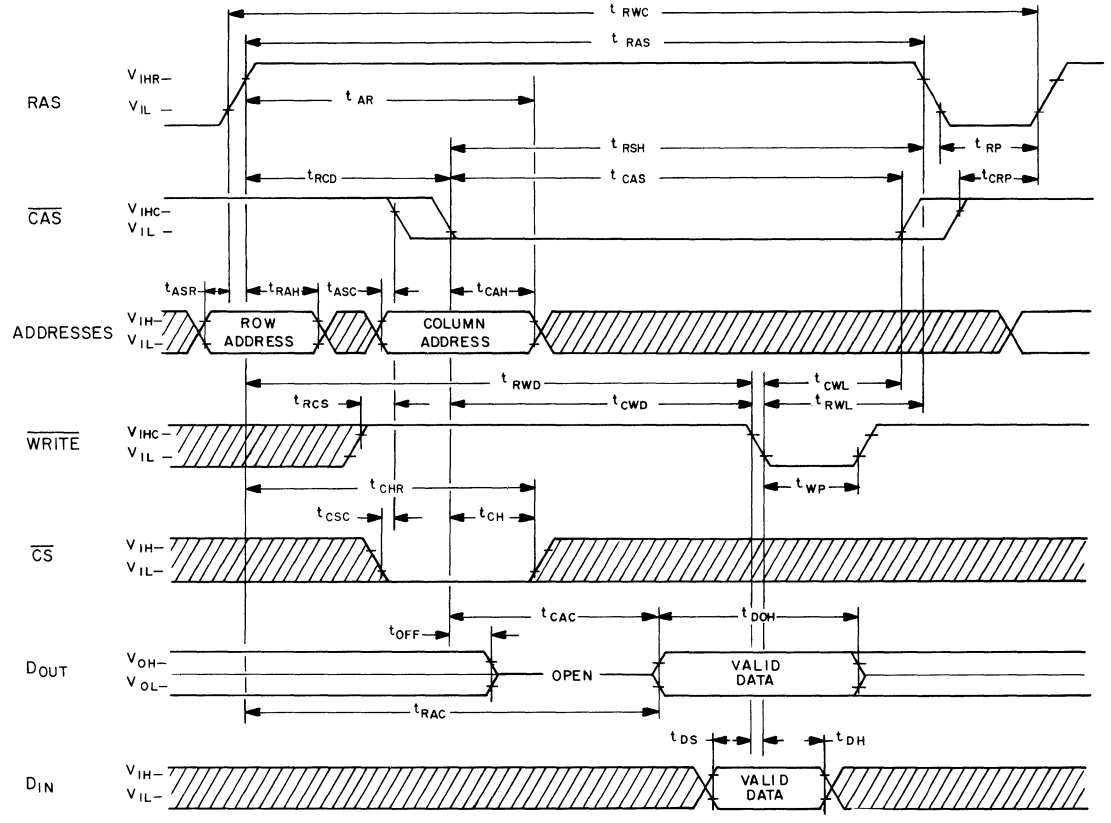
READ CYCLE



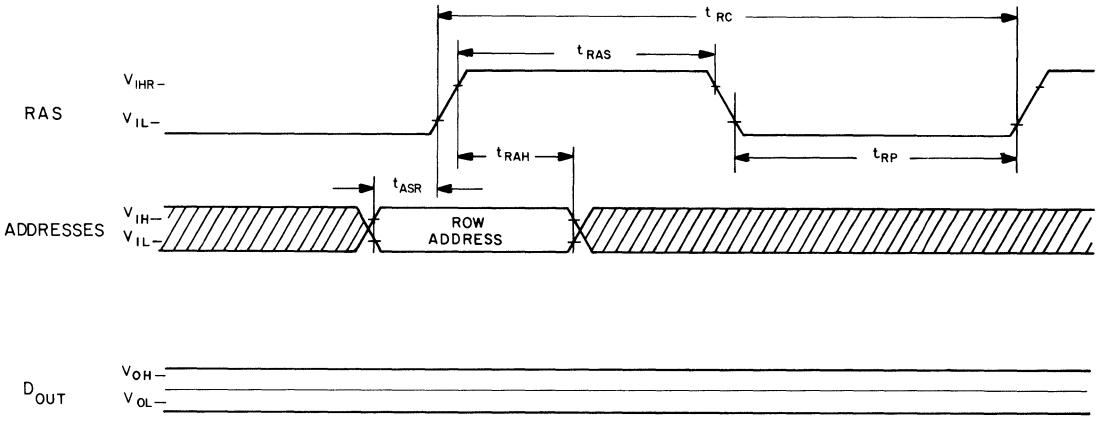
WRITE CYCLE



READ–WRITE/READ–MODIFY–WRITE CYCLE

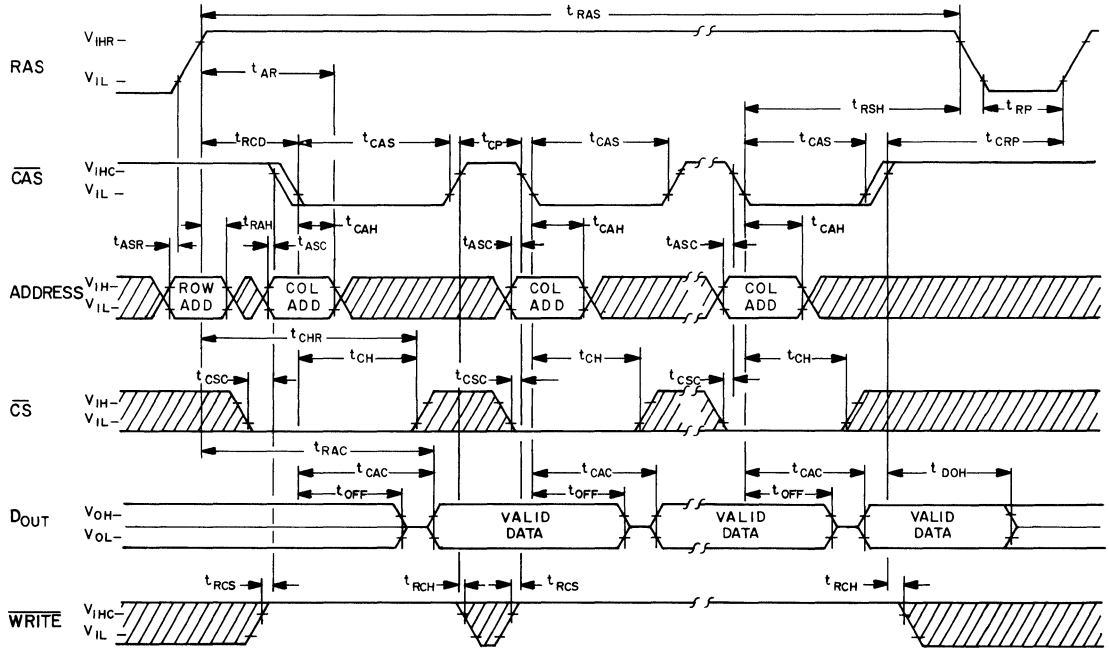


"RAS ONLY" REFRESH CYCLE

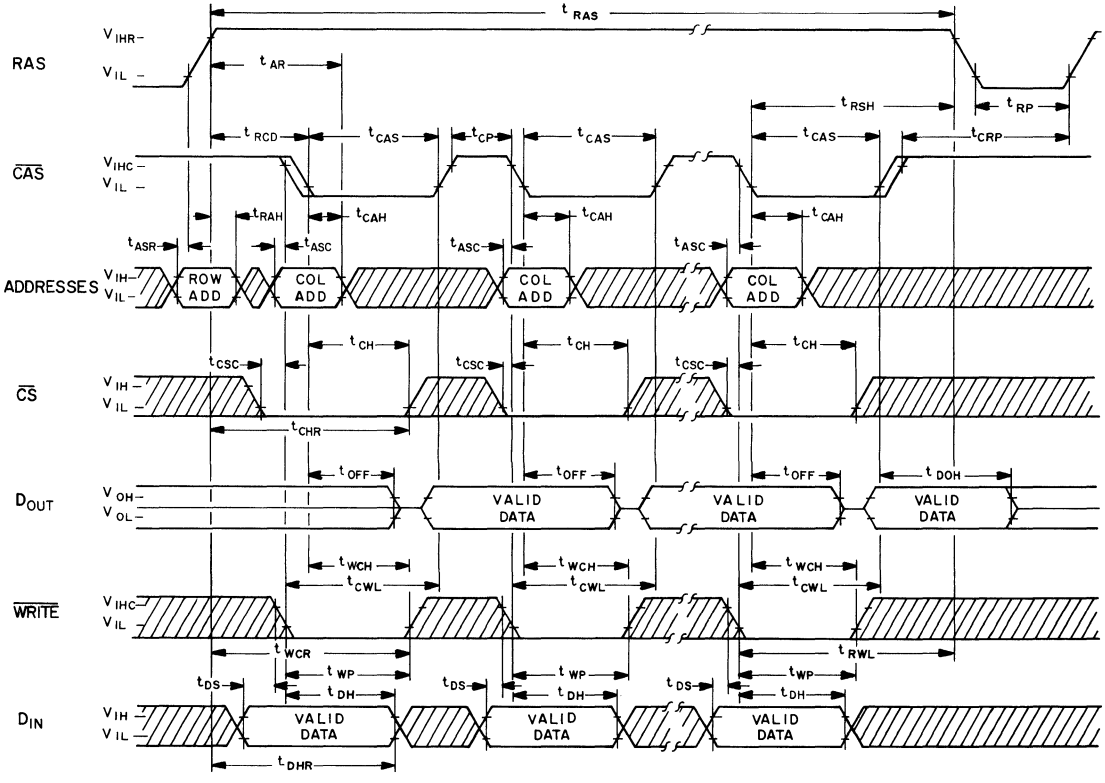


Note: D_{OUT} remains unchanged from previous cycle.

PAGE MODE READ CYCLE



PAGE MODE WRITE CYCLE



INPUT LEVELS

All inputs to the MK 4227 except row address strobe (RAS) are TTL compatible. The RAS input has been specially designed so that very little steady state (DC) power is dissipated by the MK 4227 while in standby operation. In doing this, the RAS input requires a high level signal to activate the chip. The RAS input driver must be able to change the capacitance load of the RAS input from within .8 volt at V_{SS} (0V) to within 1 volt of V_{DD} (+12).

ADDRESSING

The 12 address bits required to decode 1 of the 4096 cell locations within the MK 4227 are multiplexed onto the 6 address inputs and latched into the on-chip address latches by externally applying a positive going MOS level clock and a negative going TTL level clock. The first clock, the Row Address Strobe (RAS), latches the 6 row address bits into the chip. The second clock, the Column Address Strobe ($\overline{CAS}$), subsequently latches the 6 column address bits plus Chip Select ($\overline{CS}$) into the chip. The internal circuitry of the MK 4227 is designed to allow the column information to be externally applied to the chip before it is actually required. Because of this, the hold time requirements for the input signals associated with the Column Address Strobe are also referenced to RAS. However, this gated $\overline{CAS}$ feature allows the system designer to compensate for timing skews that may be encountered in the multiplexing operation. Since the Chip Select signal is not required until $\overline{CAS}$ time, which is well into the memory cycle, its decoding time does not add to system access or cycle time.

DATA INPUT/OUTPUT

Data to be written into a selected cell is latched into an on-chip register by a combination of $\overline{WRITE}$ and $\overline{CAS}$ while RAS is active. The later of the signals ($\overline{WRITE}$ or $\overline{CAS}$) to make its negative transition is the strobe for the Data In register. This permits several options in the write cycle timing. In a write cycle, if the $\overline{WRITE}$ input is brought low prior to $\overline{CAS}$, the Data In is strobed by $\overline{CAS}$, and the set-up and hold times are referenced to $\overline{CAS}$. If the data input is not available at $\overline{CAS}$ time or if it is desired that the cycle be a read-write cycle, the $\overline{WRITE}$ signal must be delayed until after $\overline{CAS}$. In this "delayed write cycle" the data input set-up and hold times are referenced to the negative edge of $\overline{WRITE}$ rather than to $\overline{CAS}$. (To illustrate this feature, Data In is referenced to $\overline{WRITE}$ in the timing diagram depicting the read-write and page mode write cycles while the "early write" cycle diagram shows Data In referenced to $\overline{CAS}$.) Note that if the chip is unselected ($\overline{CS}$ high at $\overline{CAS}$ time) $\overline{WRITE}$ commands are not executed and, consequently, data stored in the memory is unaffected.

Data is retrieved from the memory in a read cycle by maintaining $\overline{WRITE}$ in the inactive or high state throughout the portion of the memory cycle in which $\overline{CAS}$ is active. Data read from the selected cell will be available at the output within the specified access time.

DATA OUTPUT LATCH

Any change in the condition of the Data Out Latch is initiated by the $\overline{CAS}$ signal. The output buffer is not affected by memory (refresh) cycles in which only the RAS signal is applied to the MK 4227. Whenever $\overline{CAS}$ makes a negative transition, the output will go unconditionally open-circuited, independent of the state of any other input to the chip. If the cycle in progress is a read, read-modify-write, or a delayed write cycle and the chip is selected, then the output latch and buffer will again go active and at access time will contain the data read from the selected cell. This output data is the same polarity (not inverted) as the input data. If the cycle in progress is a write cycle ($\overline{WRITE}$ active low before $\overline{CAS}$ goes low) and the chip is selected, then at access time the output latch and buffer will contain the input data. Once having gone active, the output will remain valid until the MK 4227 receives the next $\overline{CAS}$ negative edge. Intervening refresh cycles in which a RAS is received (but no $\overline{CAS}$) will not cause valid data to be affected. Conversely, the output will assume the open-circuit state during any cycle in which the MK 4227 receives a $\overline{CAS}$ but no RAS signal (regardless of the state of any other inputs). The output will also assume the open circuit state in normal cycles (in which both RAS and $\overline{CAS}$ signals occur) if the chip is unselected.

The three-state data output buffer presents the data output pin with a low impedance to V_{CC} for a logic 1 and a low impedance to V_{SS} for a logic 0. The output resistance to V_{CC} (logic 1 state) is 420 Ω maximum and 135 Ω typically. The output resistance to V_{SS} (logic 0 state) is 125 Ω maximum and 35 Ω typically. The separate V_{CC} pin allows the output buffer to be powered from the supply voltage of the logic to which the chip is interfaced. During battery standby operation, the V_{CC} pin may have power removed without affecting the MK 4227 refresh operation. This allows all system logic except the RAS timing circuitry and the refresh address logic to be turned off during battery standby to conserve power.

REFRESH

Refresh of the dynamic cell matrix is accomplished by performing a memory cycle at each of the 64 row addresses within each 2 millisecond time interval. Any cycle in which a RAS signal occurs, accomplishes a refresh operation. A read cycle will refresh the selected row, regardless of the state of the Chip Select ($\overline{CS}$) input. A write or read-modify-write cycle also refreshes the selected row, but the chip should be unselected to prevent writing data into the selected cell. If, during a refresh cycle, the MK 4227 receives a RAS signal but no $\overline{CAS}$ signal, the state of the output will not be affected. However, if "RAS-only" refresh cycles (where RAS is the only signal applied to the chip) are continued for extended periods, the output buffer may eventually lose proper data and go open-circuit. The output buffer will regain activity with the first cycle in which a $\overline{CAS}$ signal is applied to the chip.

POWER DISSIPATION/STANDBY MODE

Most of the circuitry used in the MK 4227 is dynamic and most of the power draw is the result of an address strobe edge. Because the power is not drawn during the whole time the strobe is active, the dynamic power is a function of operating frequency rather than active duty cycle. Typically, the power is 170mW at 1 μsec cycle rate for the MK 4227 with a worse case power of less than 470mW at 320 nsec cycle time. To minimize the overall system power, the Row Address Strobe (RAS) should be decoded and supplied to only the selected chips. The $\overline{CAS}$ must be supplied to all chips (to turn off the unselected output). Those chips that did not receive a RAS, however, will not dissipate any power on the $\overline{CAS}$ edges, except for that required to turn off the outputs. If the RAS signal is decoded and supplied only to the selected chips, then the Chip Select ($\overline{CS}$) input of all chips can be at a logic 0. The chips that receive a $\overline{CAS}$ but no RAS will be unselected (output open-circuited) regardless of the Chip Select input. For refresh cylcles, however, either the $\overline{CS}$ input of all chips must be high or the $\overline{CAS}$ input must be held high to prevent several "wire-OR'd" outputs from turning on with opposing force. Note that the MK 4227 will dissipate considerably less power when the refresh operation is accomplished with a "RAS-only" cycle as opposed to a normal RAS/$\overline{CAS}$ memory cycle.

PAGE MODE OPERATION

The "Page Mode" feature of the MK 4227 allows for successive memory operations at multiple column locations of the same row address with increased speed without an increase inpower. This is done by strobing the row address into the chip and keeping the RAS signal at a logic 1 throughout all successive memory cycles in which the row address is common. This "page mode" of operation will not dissipate the power associated with the positive going edge of RAS. Also, the time required for strobing in a new row address is eliminated, thereby decreasing the access and cycle times. The chip select input ($\overline{CS}$) is operative in page mode cycles just as in normal cycles. It is not necessary that the chip be selected during the first operation in a sequence of page cycles. Likewise, the $\overline{CS}$ input can be used to select or disable any cycle(s) in a series of page cycles. This feature allows the page boundary to be extended beyond the 64 column locations in a single chip. The page boundary can be extended by applying RAS to multiple 4K memory blocks and decoding $\overline{CS}$ to select the proper block.

POWER UP

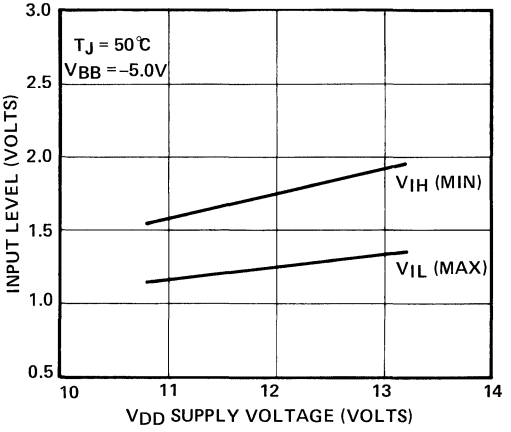
The MK 4227 requires no particular power supply sequencing so long as the Absolute Maximum Rating Conditions are observed. However, in order to insure compliance with the Absolute Maximum Ratings, MOSTEK recommends sequencing of power supplies such that V_{BB} is applied first and removed last. V_{BB} should never be more positive than V_{SS} when power is applied to V_{DD}.

Under system failure conditions in which one or more supplies exceed the specified limits significant additional margin against catastrophic device failure may be achieved by forcing RAS and Data Out to the inactive state.

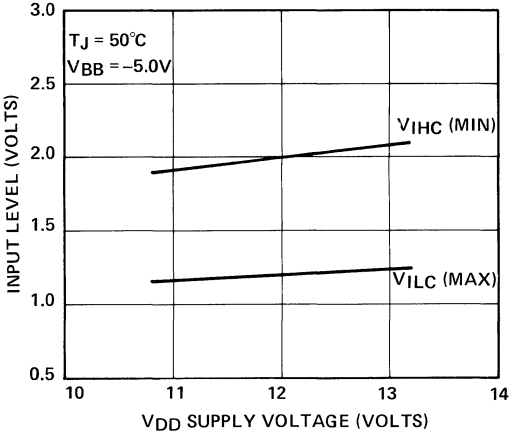
After power is applied to the device, the MK 4227 requires several cycles before proper device operation is achieved. Any 8 cycles which perform refresh are adequate for this purpose.

TYPICAL DEVICE CHARACTERISTICS

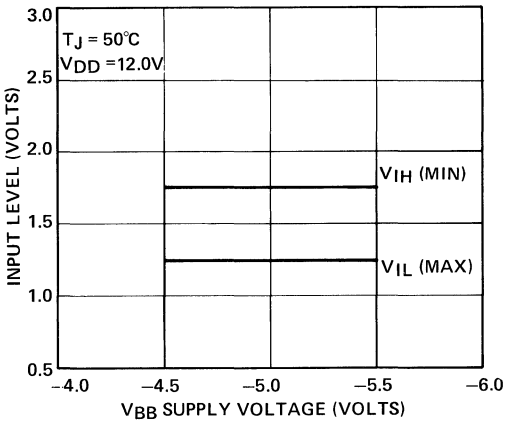
TYPICAL ADDRESS AND DATA INPUT LEVELS vs. V_{DD}



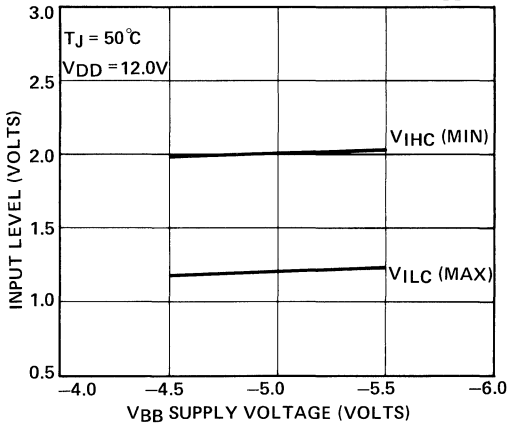
TYPICAL CLOCK INPUT LEVELS vs. V_{DD}



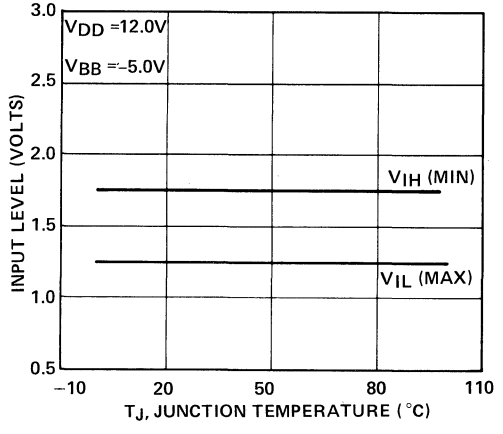
TYPICAL ADDRESS AND DATA INPUT LEVELS vs. V_{BB}



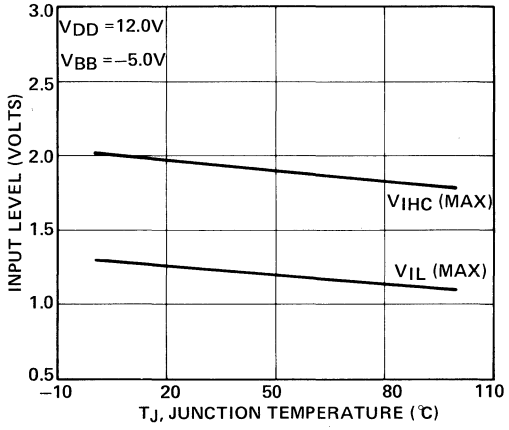
TYPICAL CLOCK INPUT LEVELS vs. V_{BB}



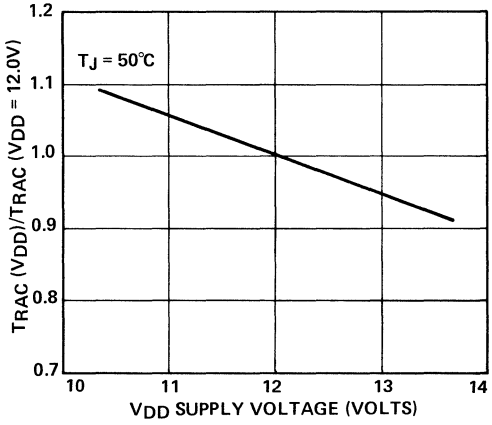
TYPICAL ADDRESS AND DATA INPUT LEVELS vs. T_J



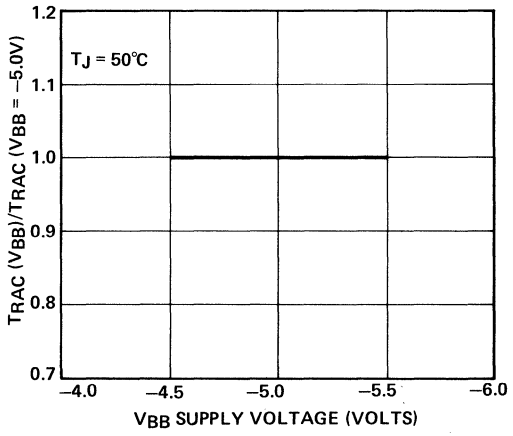
TYPICAL CLOCK INPUT LEVELS vs. T_J



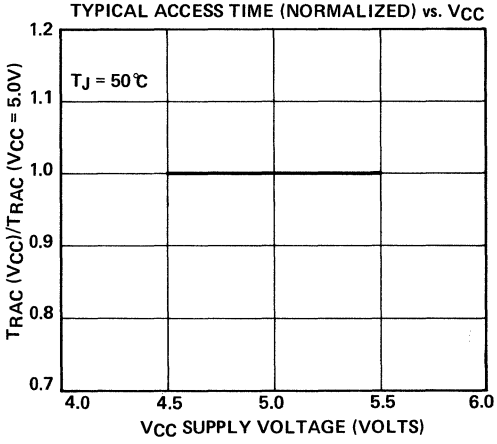
TYPICAL ACCESS TIME (NORMALIZED) vs. V_{DD}



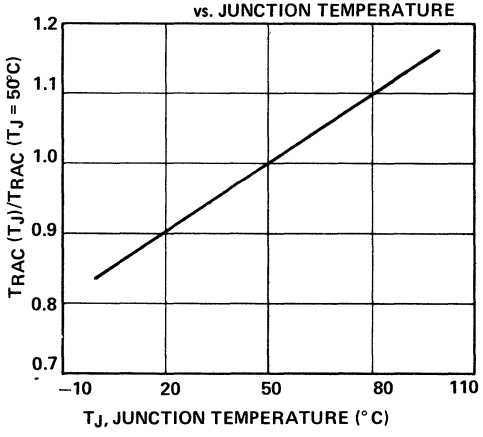
TYPICAL ACCESS TIME (NORMALIZED) vs. V_{BB}



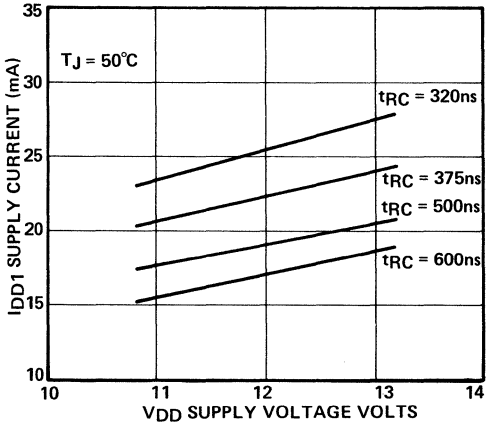
TYPICAL ACCESS TIME (NORMALIZED) vs. V_{CC}



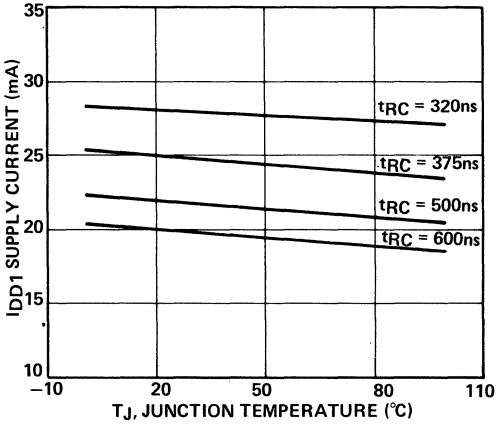
TYPICAL ACCESS TIME (NORMALIZED) vs. JUNCTION TEMPERATURE



TYPICAL I_{DD1} vs. V_{DD}



TYPICAL I_{DD1} vs. JUNCTION TEMPERATURE



16K DYNAMIC RAMS

A new generation of MOS memory devices is emerging onto the scene in the form of 16K RAMS. As the industry leader of the 16K RAM race, MOSTEK's MK 4116 serves as the "Universal Memory" for all types of system requirements. The versatility and economy of the MK 4116 allow the device to service an unusually wide spectrum of data processing applications.

MOSTEK

16,384 X 1 BIT DYNAMIC RAM

MK4116P-2/3

FEATURES

- ☐ Recognized industry standard 16-pin configuration from MOSTEK
- ☐ 150ns access time, 375ns cycle (MK 4116-2) 200ns access time, 375ns cycle (MK 4116-3)
- ☐ ± 10% tolerance on all power supplies (+12V, ±5V)
- ☐ Low power: 462mW active, 20mW standby (max)
- ☐ Output data controlled by $\overline{CAS}$ and unlatched at end of cycle to allow two dimensional chip selection and extended page boundary
- ☐ Common I/O capability using "early write" operation
- ☐ Read-Modify-Write, $\overline{RAS}$-only refresh, and Page-mode capability
- ☐ All inputs TTL compatible,low capacitance, and protected against static charge
- ☐ 128 refresh cycles

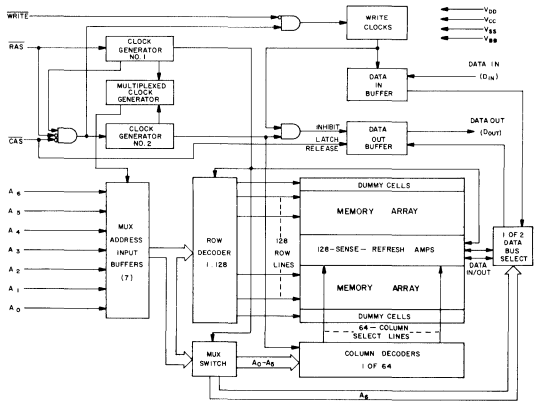
DESCRIPTION

The MK 4116 is a new generation MOS dynamic random access memory circuit organized as 16,384 words by 1 bit. As a state-of-the-art MOS memory device, the MK 4116 (16K RAM) incorporates advanced circuit techniques designed to provide wide operating margins, both internally and to the system user, while achieving performance levels in speed and power previously seen only in MOSTEK's high performance MK 4027 (4K RAM).

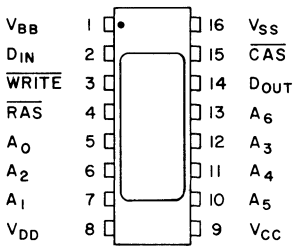
The technology used to fabricate the MK 4116 is MOSTEK's double-poly, N-channel silicon gate, POLY II ™ process. This process, coupled with the use of a single transistor dynamic storage cell, provides the maximum possible circuit density and reliability, while maintaining high performance capability. The use of dynamic circuitry throughout, including sense amplifiers, assures that power dissipation is minimized without any sacrifice in speed or operating margin. These factors combine to make the MK 4116 a truly superior RAM product.

Multiplexed address inputs (a feature pioneered by MOSTEK for its 4K RAMS) permits the MK 4116 to be packaged in a standard 16-pin DIP. This recognized industry standard package configuration, while compatible with widely available automated testing and insertion equipment, provides highest possible system bit densities and simplifies system upgrade from 4K to 16K RAMs for new generation applications. Non-critical clock timing requirements allow use of the multiplexing technique while maintaining high performance.

FUNCTIONAL DIAGRAM



PIN CONNECTIONS



PIN NAMES

A_0-A_6	ADDRESS INPUTS
$\overline{CAS}$	COLUMN ADDRESS STROBE
D_{IN}	DATA IN
D_{OUT}	DATA OUT
$\overline{RAS}$	ROW ADDRESS STROBE
$\overline{WRITE}$	READ/WRITE INPUT
V_{BB}	POWER (–5V)
V_{CC}	POWER (+5V)
V_{DD}	POWER (+12V)
V_{SS}	GROUND

ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to V_{BB} ..... −0.5V to +20V
Voltage on V_{DD}, V_{CC} supplies relative to V_{SS} ..... −1.0V to +15.0V
V_{BB}−V_{SS} (V_{DD}−V_{SS} >0V) 0V
Operating temperature, T_A (Ambient) ..... 0°C to + 70°C
Storage temperature (Ambient) ..... −65° C to + 150°C
Short circuit output current 50mA
Power dissipation ..... 1 Watt

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS
($0°C \leq T_A \leq 70°C$)[1]

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{DD} V_{CC} V_{SS} V_{BB}	10.8 4.5 0 −4.5	12.0 5.0 0 −5.0	13.2 5.5 0 −5.5	Volts Volts Volts Volts	2 2,3 2 2
Input High (Logic 1) Voltage, $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	V_{IHC}	2.7	–	7.0	Volts	2
Input High (Logic 1) Voltage, all inputs except $\overline{RAS}$, $\overline{CAS}$ $\overline{WRITE}$	V_{IH}	2.4	–	7.0	Volts	2
Input Low (Logic 0) Voltage, all inputs	V_{IL}	−1.0	–	.8	Volts	2

DC ELECTRICAL CHARACTERISTICS
($0°C \leq T_A \leq 70°C$)[1] (V_{DD} = 12.0V ±10%; V_{CC} = 5.0V ±10%; V_{BB} = −5.0V ±10%; V_{SS} = 0V)

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
OPERATING CURRENT Average power supply operating current ($\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = 375ns)	I_{DD1} I_{CC1} I_{BB1}		35 200	mA µA	4 5
STANDBY CURRENT Power supply standby current ($\overline{RAS}$ = V_{IHC}, D_{OUT} = High Impedance)	I_{DD2} I_{CC2} I_{BB2}	 −10 	1.5 10 100	mA µA µA	
REFRESH CURRENT Average power supply current, refresh mode ($\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IHC}; t_{RC} = 375ns)	I_{DD3} I_{CC3} I_{BB3}	 −10 	27 10 200	mA µA µA	4
PAGE MODE CURRENT Average power supply current, page-mode operation ($\overline{RAS}$ =V_{IL}, $\overline{CAS}$ cycling; t_{PC} = 225ns)	I_{DD4} I_{CC4} I_{BB4}		27 200	mA µA	4 5
INPUT LEAKAGE Input leakage current, any input (V_{BB} = −5V, 0V ≤ V_{IN} ≤ +7.0V, all other pins not under test = 0 volts)	$I_{I(L)}$	−10	10	µA	
OUTPUT LEAKAGE Output leakage current (D_{OUT} is disabled, 0V ≤ V_{OUT} ≤ +5.5V)	$I_{O(L)}$	−10	10	µA	
OUTPUT LEVELS Output high (Logic 1) voltage (I_{OUT} = −5mA) Output low (Logic 0) voltage (I_{OUT} = 4.2 mA)	V_{OH} V_{OL}	2.4 	 0.4	Volts Volts	3

NOTES:

1. T_A is specified here for operation at frequencies to $t_{RC} \geq t_{RC}$ (min). Operation at higher cycle rates with reduced ambient temperatures and higher power dissipation is permissible, however, provided AC operating parameters are met. See figure 1 for derating curve.
2. All voltages referenced to V_{SS}.
3. Output voltage will swing from V_{SS} to V_{CC} when activated with no current loading. For purposes of maintaining data in standby mode, V_{CC} may be reduced to V_{SS} without affecting refresh operations or data retention. However, the V_{OH} (min) specification is not guaranteed in this mode.
4. I_{DD1}, I_{DD3}, and I_{DD4} depend on cycle rate. See figures 2,3, and 4 for I_{DD} limits at other cycle rates.
5. I_{CC1} and I_{CC4} depend upon output loading. During readout of high level data V_{CC} is connected through a low impedance (135 Ω typ) to data out. At all other times I_{CC} consists of leakage currents only.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (6,7,8)

($0°C \leq T_A \leq 70°C$)[1] (V_{DD} = 12.0V ±10%; V_{CC} = 5.0V ±10%, V_{SS} = 0V, V_{BB} = −5.0V ±10%)

PARAMETER	SYMBOL	MK 4116-2 MIN	MK 4116-2 MAX	MK 4116-3 MIN	MK 4116-3 MAX	UNITS	NOTES
Random read or write cycle time	t_{RC}	375		375		ns	9
Read-write cycle time	t_{RWC}	375		375		ns	9
Page mode cycle time	t_{PC}	170		225		ns	
Access time from $\overline{RAS}$	t_{RAC}		150		200	ns	10,12
Access time from $\overline{CAS}$	t_{CAC}		100		135	ns	11,12
Output buffer turn-off delay	t_{OFF}	0	40	0	50	ns	13
Transition time (rise and fall)	t_T	3	35	3	50	ns	8
$\overline{RAS}$ precharge time	t_{RP}	100		120		ns	
$\overline{RAS}$ pulse width	t_{RAS}	150	10,000	200	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	100		135		ns	
$\overline{CAS}$ hold time	t_{CSH}	150		200			
$\overline{CAS}$ pulse width	t_{CAS}	100	10,000	135	10,000	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	50	25	65	ns	14
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	−20		−20		ns	
Row Address set-up time	t_{ASR}	0		0		ns	
Row Address hold time	t_{RAH}	20		25		ns	
Column Address set-up time	t_{ASC}	−10		−10		ns	
Column Address hold time	t_{CAH}	45		55		ns	
Column Address hold time referenced to $\overline{RAS}$	t_{AR}	95		120		ns	
Read command set-up time	t_{RCS}	0		0		ns	
Read command hold time	t_{RCH}	0		0		ns	
Write command hold time	t_{WCH}	45		55		ns	
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	95		120		ns	
Write command pulse width	t_{WP}	45		55		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	60		80		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	60		80		ns	
Data-in set-up time	t_{DS}	0		0		ns	15
Data-in hold time	t_{DH}	45		55		ns	15
Data-in hold time referenced to $\overline{RAS}$	t_{DHR}	95		120		ns	
$\overline{CAS}$ precharge time (for page-mode cycle only)	t_{CP}	60		80		ns	
Refresh period	t_{REF}		2		2	ms	
$\overline{WRITE}$ command set-up time	t_{WCS}	−20		−20		ns	16
$\overline{CAS}$ to $\overline{WRITE}$ delay	t_{CWD}	70		95		ns	16
$\overline{RAS}$ to $\overline{WRITE}$ delay	t_{RWD}	120		160		ns	16

NOTES (Continued)

6. Several cycles are required after power-up before proper device operation is achieved. Any 8 cycles which perform refresh are adequate for this purpose.
7. AC measurements assume t_T = 5ns.
8. V_{IHC} (min) or V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IHC} or V_{IH} and V_{IL}.
9. The specifications for t_{RC} (min) and t_{RWC} (min) are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \leq T_A \leq 70°C$) is assured.
10. Assumes that $t_{RCD} \leq t_{RCD}$ (max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the value shown.
11. Assumes that $t_{RCD} \geq t_{RCD}$ (max).
12. Measured with a load equivalent to 2 TTL loads and 100pF.
13. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
14. Operation within the t_{RCD} (max) limit insures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
15. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WRITE}$ leading edge in delayed write or read-modify-write cycles.
16. t_{WCS}, t_{CWD} and t_{RWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only: If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; If $t_{CWD} \geq t_{CWD}$ (min) and $t_{RWD} \geq t_{RWD}$ (min), the cycle is a read-write cycle and the data out will contain data read from the selected cell; If neither of the above sets of conditions is satisfied the condition of the data out (at access time) is indeterminate.
17. Effective capacitance calculated from the equation $C = I \frac{\Delta t}{\Delta V}$ with ΔV = 3 volts and power supplies at nominal levels.
18. $\overline{CAS}$ = V_{IHC} to disable D_{OUT}.

AC ELECTRICAL CHARACTERISTICS

($0°C \leq T_A \leq 70°C$) (V_{DD} = 12.0V ± 10%; V_{SS} = 0V; V_{BB} = –5.0V ± 10%)

PARAMETER	SYMBOL	TYP	MAX	UNITS	NOTES
Input Capacitance (A_0–A_6), D_{IN}	C_{I1}	4	5	pF	17
Input Capacitance $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	C_{I2}	8	10	pF	17
Output Capacitance (D_{OUT})	C_O	5	7	pF	17,18

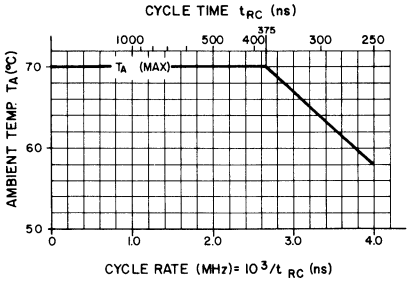


Fig. 1 Maximum ambient temperature versus cycle rate for extended frequency operation. T_A (max) for operation at cycling rates greater than 2.66 MHz (t_{CYC} < 375ns) is determined by T_A (max) [°C] =70 – 9.0 x (cycle rate [MHz] –2.66).

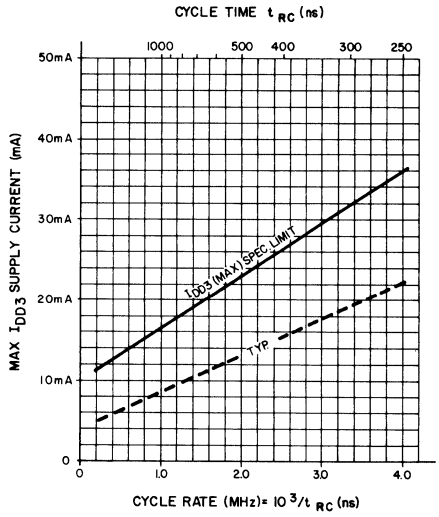


Fig. 3 Maximum I_{DD3} versus cycle rate for device operation at extended frequencies. I_{DD3} (max) curve is defined by the equation:
I_{DD3} (max) [mA]= 10 + 6.5 x cycle rate [MHz]

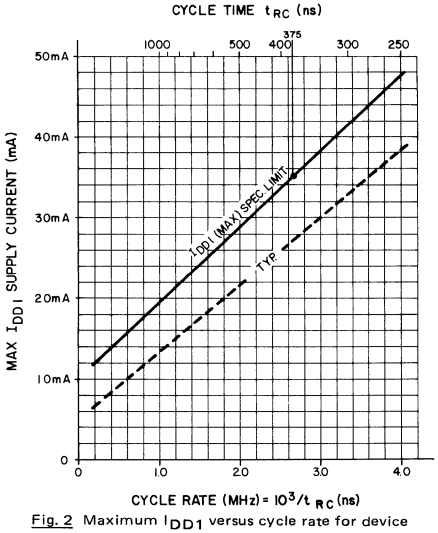


Fig. 2 Maximum I_{DD1} versus cycle rate for device operation at extended frequencies. I_{DD1} (max) curve is defined by the equation:
I_{DD1} (max) [mA] = 10 + 9.4x cycle rate [MHz] .

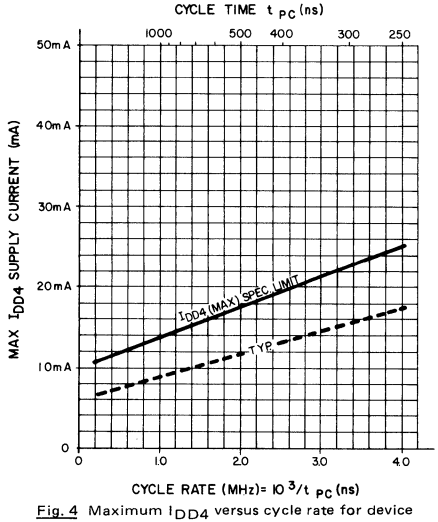
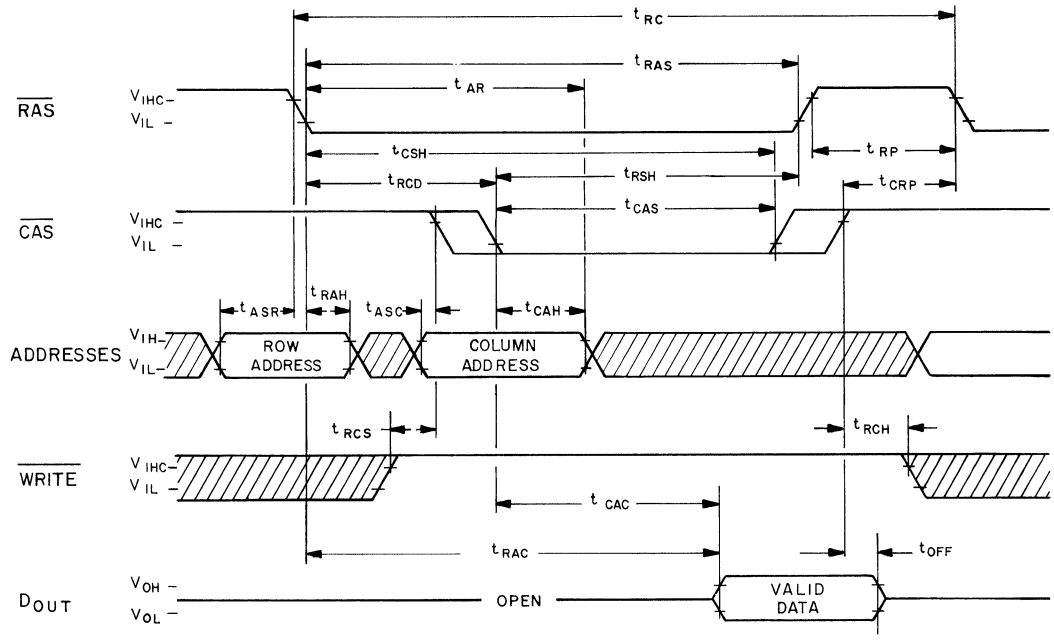
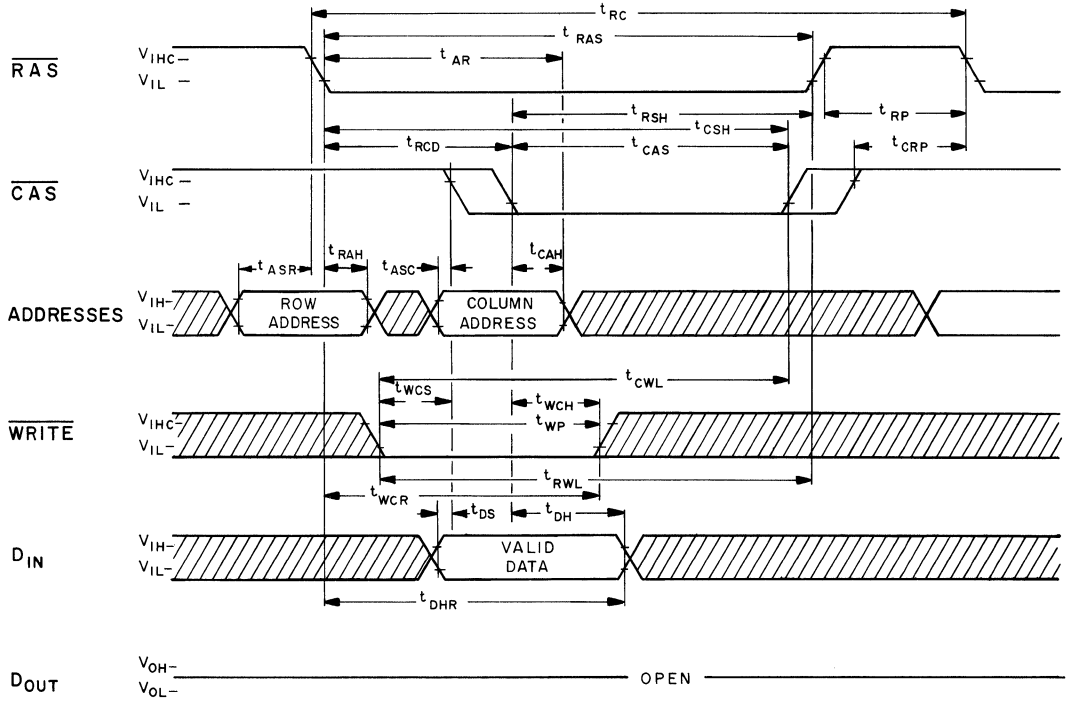


Fig. 4 Maximum I_{DD4} versus cycle rate for device operation in page mode. I_{DD4} (max) curve is defined by the equation
I_{DD4} (max) [mA] = 10 + 3.75 x cycle rate [MHz]

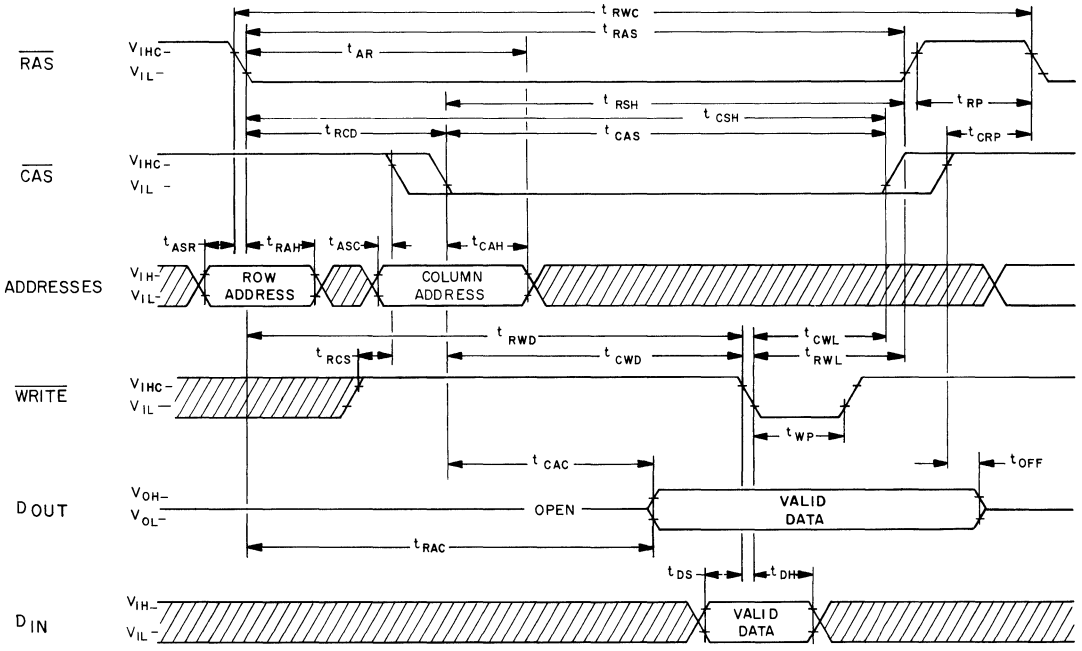
READ CYCLE



WRITE CYCLE (EARLY WRITE)

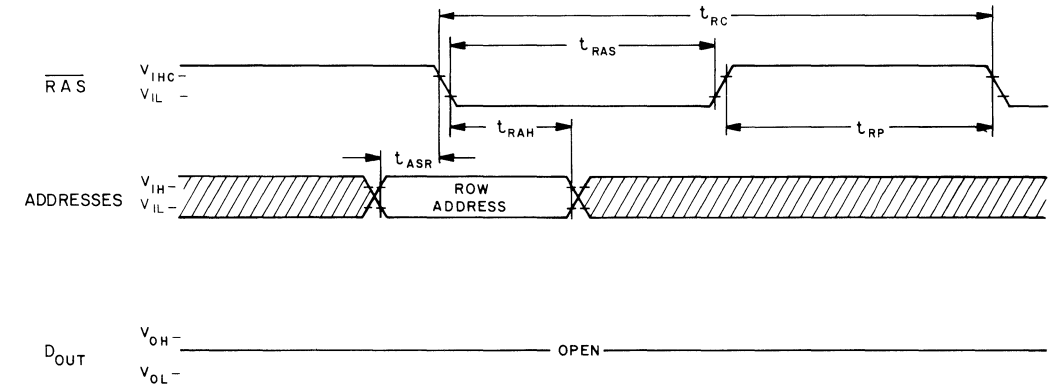


READ–WRITE/READ–MODIFY–WRITE CYCLE

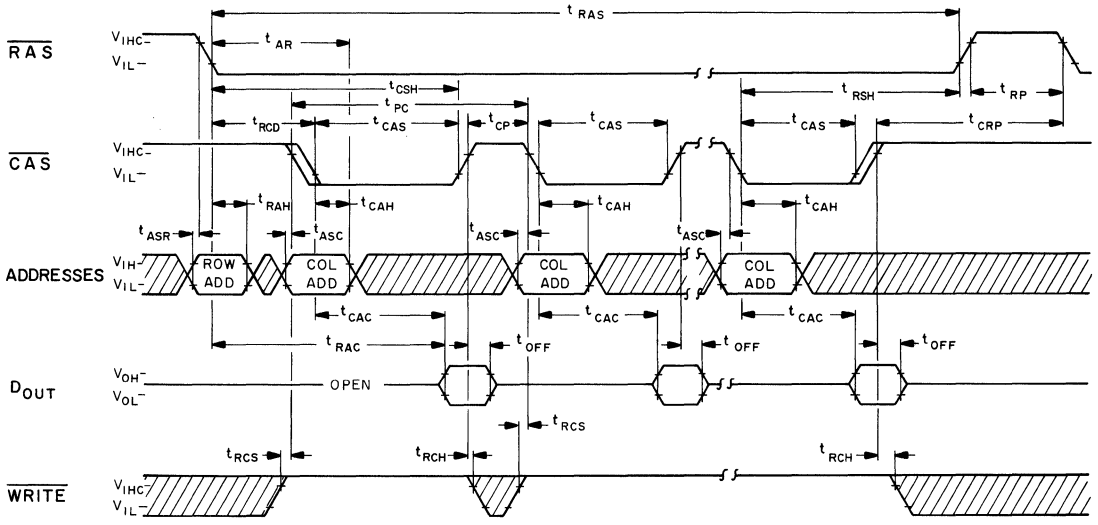


"RAS–ONLY" REFRESH CYCLE

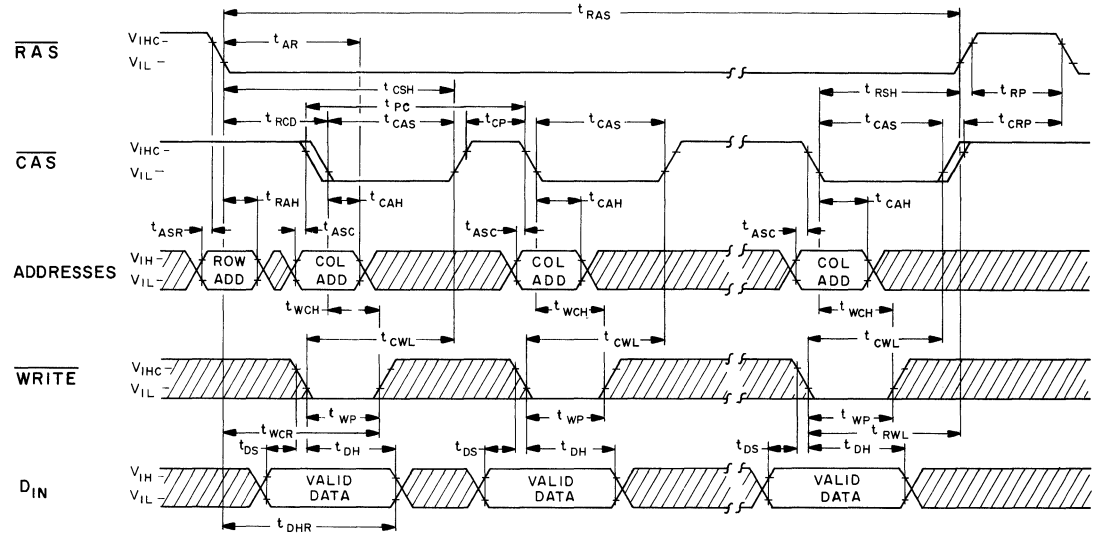
NOTE: $\overline{CAS}$ = V_{IHC}, $\overline{WRITE}$ = Don't Care



PAGE MODE READ CYCLE



PAGE MODE WRITE CYCLE



DESCRIPTION (continued)

System oriented features include ± 10% tolerance on all power supplies, direct interfacing capability with high performance logic families such as Schottky TTL, maximum input noise immunity to minimize "false triggering" of the inputs (a common cause of soft errors), on-chip address and data registers which eliminate the need for interface registers, and two chip select methods to allow the user to determine the appropriate speed/power characteristics of his memory system. The MK 4116 also incorporates several flexible timing/operating modes. In addition to the usual read, write, and read-modify-write cycles, the MK 4116 is capable of delayed write cycles, page-mode operation and $\overline{RAS}$-only refresh. Proper control of the clock inputs($\overline{RAS}$, $\overline{CAS}$ and $\overline{WRITE}$) allows common I/O capability, two dimensional chip selection, and extended page boundaries (when operating in page mode).

ADDRESSING

The 14 address bits required to decode 1 of the 16,384 cell locations within the MK 4116 are multiplexed onto the 7 address inputs and latched into the on-chip address latches by externally applying two negative going TTL-level clocks. The first clock, the Row Address Strobe ($\overline{RAS}$), latches the 7 row address bits into the chip. The second clock, the Column Address Strobe ($\overline{CAS}$), subsequently latches the 7 column address bits into the chip. Each of these signals, $\overline{RAS}$ and $\overline{CAS}$, triggers a sequence of events which are controlled by different delayed internal clocks. The two clock chains are linked together logically in such a way that the address multiplexing operation is done outside of the critical path timing sequence for read data access. The later events in the $\overline{CAS}$ clock sequence are inhibited until the occurence of a delayed signal derived from the $\overline{RAS}$ clock chain. This "gated $\overline{CAS}$" feature allows the $\overline{CAS}$ clock to be externally activated as soon as the Row Address Hold Time specification (t_{RAH}) has been satisfied and the address inputs have been changed from Row address to Column address information.

Note that $\overline{CAS}$ can be activated at any time after t_{RAH} and it will have no effect on the worst case data access time (t_{RAC}) up to the point in time when the delayed row clock no longer inhibits the remaining sequence of column clocks. Two timing endpoints result from the internal gating of $\overline{CAS}$ which are called t_{RCD} (min) and t_{RCD} (max). No data storage or reading errors will result if $\overline{CAS}$ is applied to the MK 4116 at a point in time beyond the t_{RCD} (max) limit. However, access time will then be determined exclusively by the access time from $\overline{CAS}$ (t_{CAC}) rather than from $\overline{RAS}$ (t_{RAC}), and access time from $\overline{RAS}$ will be lengthened by the amount that t_{RCD} exceeds the t_{RCD} (max) limit.

DATA INPUT/OUTPUT

Data to be written into a selected cell is latched into an on-chip register by a combination of $\overline{WRITE}$ and $\overline{CAS}$ while $\overline{RAS}$ is active. The later of the signals ($\overline{WRITE}$ or $\overline{CAS}$) to make its negative transition is the strobe for the Data In (D_{IN}) register. This permits several options in the write cycle timing. In a write cycle, if the $\overline{WRITE}$ input is brought low (active) prior to $\overline{CAS}$, the D_{IN} is strobed by $\overline{CAS}$, and the set-up and hold times are referenced to $\overline{CAS}$. If the input data is not available at $\overline{CAS}$ time or if it is desired that the cycle be a read-write cycle, the $\overline{WRITE}$ signal will be delayed until after $\overline{CAS}$ has made its negative transition. In this "delayed write cycle" the data input set-up and hold times are referenced to the negative edge of $\overline{WRITE}$ rather than $\overline{CAS}$. (To illustrate this feature, D_{IN} is referenced to $\overline{WRITE}$ in the timing diagrams depicting the read-write and page-mode write cycles while the "early write" cycle diagram shows D_{IN} referenced to $\overline{CAS}$).

Data is retrieved from the memory in a read cycle by maintaining $\overline{WRITE}$ in the inactive or high state throughout the portion of the memory cycle in which $\overline{CAS}$ is active (low). Data read from the selected cell will be available at the output within the specified access time.

DATA OUTPUT CONTROL

The normal condition of the Data Output (D_{OUT}) of the MK 4116 is the high impedance (open-circuit) state. That is to say, anytime $\overline{CAS}$ is at a high level, the D_{OUT} pin will be floating. The only time the output will turn on and contain either a logic 0 or logic 1 is at access time during a read cycle. D_{OUT} will remain valid from access time until $\overline{CAS}$ is taken back to the inactive (high level) condition.

If the memory cycle in progress is a read, read-modify write, or a delayed write cycle, then the data output will go from the high impedance state to the active condition, and at access time will contain the data read from the selected cell. This output data is the same polarity (not inverted) as the input data. Once having gone active, the output will remain valid until $\overline{CAS}$ is taken to the precharge (logic 1) state,whether or not $\overline{RAS}$ goes into precharge.

If the cycle in progress is an "early-write" cycle ($\overline{WRITE}$ active before $\overline{CAS}$ goes active), then the output pin will maintain the high impedance state throughout the entire cycle. Note that with this type of output configuration, the user is given full control of the D_{OUT} pin simply by controlling the placement of $\overline{WRITE}$ command during a write cycle, and the pulse width of the Column Address Strobe during read operations. Note also that even though data is not latched at the output, data can remain valid from access time until the beginning of a subsequent cycle without paying any penalty in overall memory cycle time (stretching the cycle).

This type of output operation results in some very significant system implications.

Common I/O Operation – If all write operations are handled in the "early write" mode,then D_{IN} can be connected directly to D_{OUT} for a common I/O data bus.

Data Output Control – D_{OUT} will remain valid during a read cycle from t_{CAC} until $\overline{CAS}$ goes back to a high level (precharge), allowing data to be valid from one cycle up until a new memory cycle begins with no penalty in cycle time. This also makes the $\overline{RAS}/\overline{CAS}$ clock timing relationship very flexible.

Two Methods of Chip Selection – Since D_{OUT} is not latched, $\overline{CAS}$ is not required to turn off the outputs of unselected memory devices in a matrix. This means that both $\overline{CAS}$ and/or $\overline{RAS}$ can be decoded for chip selection. If both $\overline{RAS}$ and $\overline{CAS}$ are decoded, then a two dimensional (X,Y) chip select array can be realized.

Extended Page Boundary – Page-mode operation allows for successive memory cycles at multiple column locations of the same row address. By decoding $\overline{CAS}$ as a page cycle select signal, the page boundary can be extended beyond the 128 column locations in a single chip. (See page-mode operation).

OUTPUT INTERFACE CHARACTERISTICS

The three state data output buffer presents the data output pin with a low impedance to V_{CC} for a logic 1 and a low impedance to V_{SS} for a logic 0. The effective resistance to V_{CC} (logic 1 state) is 420 Ω maximum and 135Ω typically. The resistance to V_{SS} (logic 0 state) is 95 Ω maximum and 35 Ω typically. The separate V_{CC} pin allows the output buffer to be powered from the supply voltage of the logic to which the chip is interfaced. During battery standby operation, the V_{CC} pin may have power removed without affecting the MK 4116 refresh operation. This allows all system logic except the $\overline{RAS}$ timing circuitry and the refresh address logic to be turned off during battery standby to conserve power.

PAGE MODE OPERATION

The "Page Mode" feature of the MK 4116 allows for successive memory operations at multiple column locations of the same row address with increased speed without an increase in power. This is done by strobing the row address into the chip and maintaining the $\overline{RAS}$ signal at a logic 0 throughout all successive memory cycles in which the row address is common. This "page-mode" of operation will not dissipate the power associated with the negative going edge of $\overline{RAS}$. Also, the time required for strobing in a new row address is eliminated, thereby decreasing the access and cycle times.

The page boundary of a single MK 4116 is limited to the 128 column locations determined by all combinations of the 7 column address bits. However, in system applications which utilize more than 16,384 data words, (more than one 16K memory block), the page boundary can be extended by using $\overline{CAS}$ rather than $\overline{RAS}$ as the chip select signal. $\overline{RAS}$ is applied to all devices to latch the row address into each device and then $\overline{CAS}$ is decoded and serves as a page cycle select signal. Only those devices which receive both $\overline{RAS}$ and $\overline{CAS}$ signals will execute a read or write cycle.

REFRESH

Refresh of the dynamic cell matrix is accomplished by performing a memory cycle at each of the 128 row addresses within each 2 millisecond time interval. Although any normal memory cycle will perform the refresh operation, this function is most easily accomplished with "$\overline{RAS}$-only" cycles. $\overline{RAS}$-only refresh results in a substantial reduction in operating power. This reduction in power is reflected in the I_{DD3} specification.

POWER CONSIDERATIONS

Most of the circuitry used in the MK 4116 is dynamic and most of the power drawn is the result of an address strobe edge. Consequently, the dynamic power is primarily a function of operating frequency rather than active duty cycle (refer to the MK 4116 current waveforms in figure 5). This current characteristic of the MK 4116 precludes inadvertent burn out of the device in the event that the clock inputs become shorted to ground due to system malfunction.

Although no particular power supply noise restriction exists other than the supply voltages remain within the specified tolerance limits, adequate decoupling should be provided to suppress high frequency noise resulting from the transient current of the device. This insures optimum system performance and reliability. Bulk capacitance requirements are minimal since the MK 4116 draws very little steady state (DC) current.

In system applications requiring lower power dissipation, the operating frequency (cycle rate) of the MK 4116 can be reduced and the (guaranteed maximum) average power dissipation of the device will be lowered in accordance with the I_{DD1} (max) spec limit curve illustrated in figure 2. NOTE: The MK 4116 family is guaranteed to have a maximum I_{DD1} requirement of 35mA @ 375ns cycle with an ambient temperature range from 0°to 70°C. A lower operating frequency, for example 1 microsecond cycle, results in a reduced maximum I_{DD1} requirement of under 20mA with an ambient temperature range from 0°to 70°C.

It is possible to operate certain versions of the MK 4116 family (the –2 and –3 speed selections for example) at frequencies higher than 2.66 MHz (375ns cycle), provided all AC operating parameters are met. Operation at shorter cycle times (< 375ns) results in higher power dissipation and, therefore, a reduction in ambient temperature is required. Refer to figure 1 for derating curve.

Fig. 5 Typical Current Waveforms

Although $\overline{RAS}$ and/or $\overline{CAS}$ can be decoded and used as a chip select signal for the MK 4116, overall system power is minimized if the Row Address Strobe ($\overline{RAS}$) is used for this purpose. All unselected devices (those which do not receive a $\overline{RAS}$) will remain in a low power (standby) mode regardless of the state of $\overline{CAS}$.

POWER UP

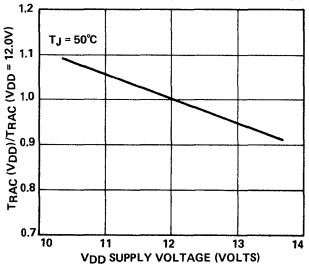
The MK 4116 requires no particular power supply sequencing so long as the Absolute Maximum Rating Conditions are observed. However, in order to insure compliance with the Absolute Maximum Ratings, MOSTEK recommends sequencing of power supplies such that V_{BB} is applied first and removed last. V_{BB} should never be more positive than V_{SS} when power is applied to V_{DD}.

Under system failure conditions in which one or more supplies exceed the specified limits significant additional margin against catastrophic device failure may be achieved by forcing $\overline{RAS}$ and $\overline{CAS}$ to the inactive state (high level).

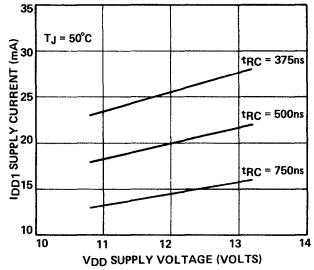
After power is applied to the device, the MK 4116 requires several cycles before proper device operation is achieved. Any 8 cycles which perform refresh are adequate for this purpose.

TYPICAL CHARACTERISTICS

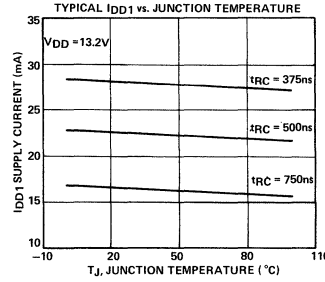
TYPICAL ACCESS TIME (NORMALIZED) vs. V_{DD}



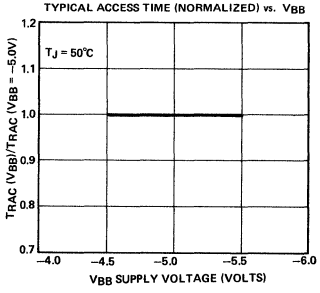
TYPICAL I_{DD1} vs. V_{DD}



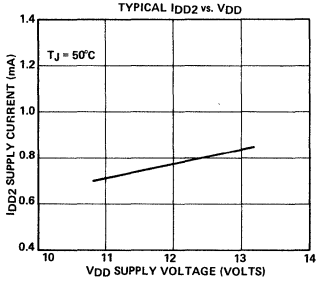
TYPICAL I_{DD1} vs. JUNCTION TEMPERATURE



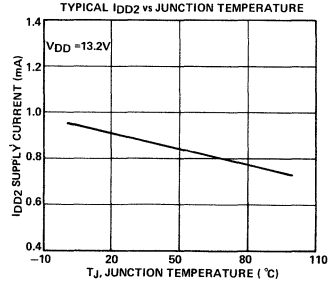
TYPICAL ACCESS TIME (NORMALIZED) vs. V_{BB}



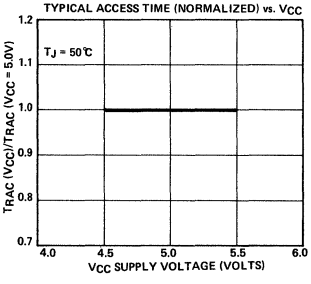
TYPICAL I_{DD2} vs. V_{DD}



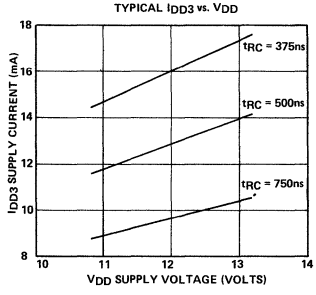
TYPICAL I_{DD2} vs JUNCTION TEMPERATURE



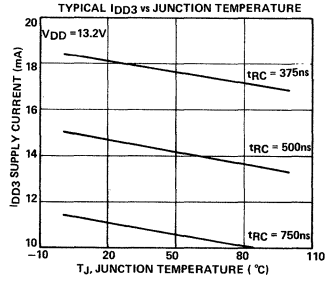
TYPICAL ACCESS TIME (NORMALIZED) vs. V_{CC}



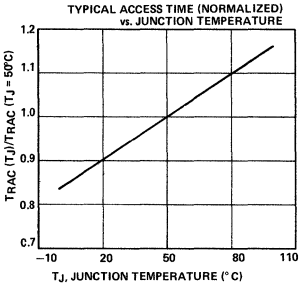
TYPICAL I_{DD3} vs. V_{DD}



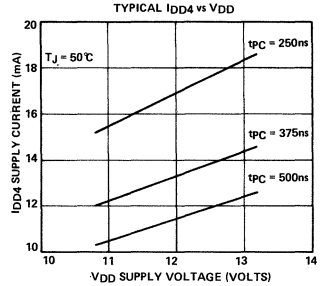
TYPICAL I_{DD3} vs JUNCTION TEMPERATURE



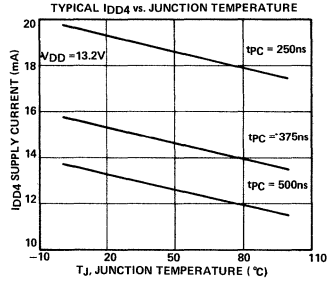
TYPICAL ACCESS TIME (NORMALIZED)
vs. JUNCTION TEMPERATURE



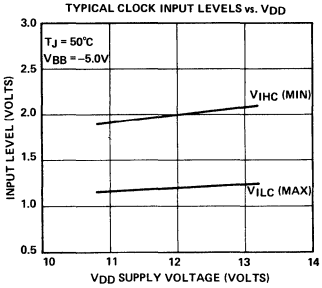
TYPICAL I_{DD4} vs V_{DD}



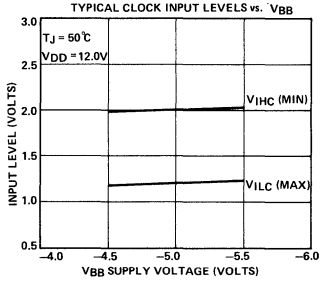
TYPICAL I_{DD4} vs. JUNCTION TEMPERATURE



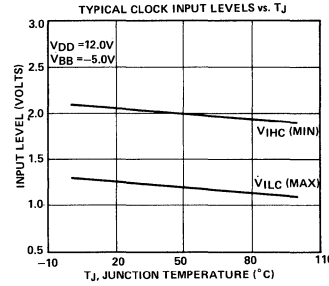
TYPICAL CLOCK INPUT LEVELS vs. V_{DD}



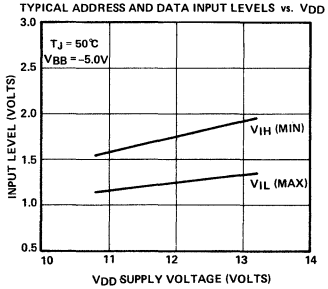
TYPICAL CLOCK INPUT LEVELS vs. V_{BB}



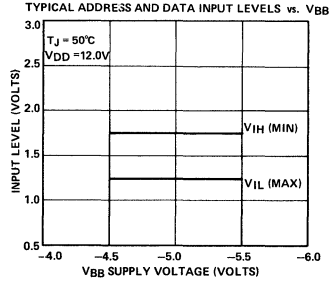
TYPICAL CLOCK INPUT LEVELS vs. T_J



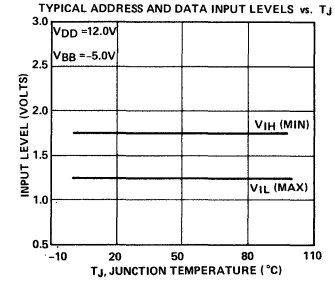
TYPICAL ADDRESS AND DATA INPUT LEVELS vs. V_{DD}



TYPICAL ADDRESS AND DATA INPUT LEVELS vs. V_{BB}



TYPICAL ADDRESS AND DATA INPUT LEVELS vs. T_J



MOSTEK

16,384 X 1 BIT DYNAMIC RAM

MK4116P-4

FEATURES

- ☐ Recognized industry standard 16-pin configuration from MOSTEK
- ☐ 250ns access time, 410ns cycle
- ☐ ± 10% tolerance on all power supplies (+12V, ±5V)
- ☐ Low power: 462mW active, 20mW standby (max)
- ☐ Output data controlled by $\overline{CAS}$ and unlatched at end of cycle to allow two dimensional chip selection and extended page boundary
- ☐ Common I/O capability using "early write" operation
- ☐ Read-Modify-Write, $\overline{RAS}$-only refresh, and Page-mode capability
- ☐ All inputs TTL compatible,low capacitance, and protected against static charge
- ☐ 128 refresh cycles

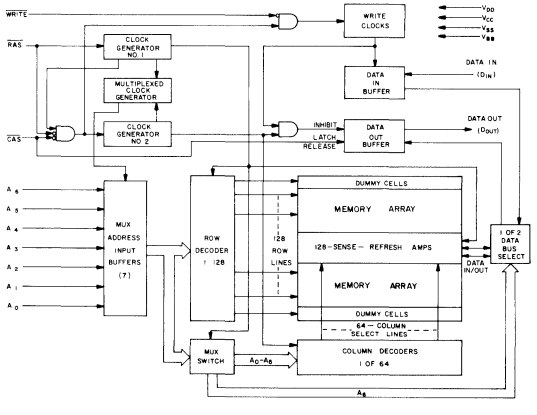
DESCRIPTION

The MK 4116 is a new generation MOS dynamic random access memory circuit organized as 16,384 words by 1 bit. As a state-of-the-art MOS memory device, the MK 4116 (16K RAM) incorporates advanced circuit techniques designed to provide wide operating margins, both internally and to the system user, while achieving performance levels in speed and power previously seen only in MOSTEK's high performance MK 4027 (4K RAM).

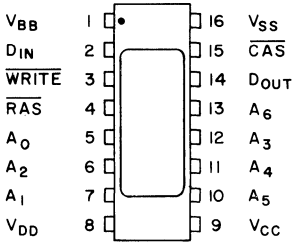
The technology used to fabricate the MK 4116 is MOSTEK's double-poly, N-channel silicon gate, POLY II™ process. This process, coupled with the use of a single transistor dynamic storage cell, provides the maximum possible circuit density and reliability, while maintaining high performance capability. The use of dynamic circuitry throughout, including sense amplifiers, assures that power dissipation is minimized without any sacrifice in speed or operating margin. These factors combine to make the MK 4116 a truly superior RAM product.

Multiplexed address inputs (a feature pioneered by MOSTEK for its 4K RAMS) permits the MK 4116 to be packaged in a standard 16-pin DIP. This recognized industry standard package configuration, while compatible with widely available automated testing and insertion equipment, provides highest possible system bit densities and simplifies system upgrade from 4K to 16K RAMs for new generation applications. Non-critical clock timing requirements allow use of the multiplexing technique while maintaining high performance.

FUNCTIONAL DIAGRAM



PIN CONNECTIONS



PIN NAMES

A_0-A_6	ADDRESS INPUTS
$\overline{CAS}$	COLUMN ADDRESS STROBE
D_{IN}	DATA IN
D_{OUT}	DATA OUT
$\overline{RAS}$	ROW ADDRESS STROBE
$\overline{WRITE}$	READ/WRITE INPUT
V_{BB}	POWER (–5V)
V_{CC}	POWER (+5V)
V_{DD}	POWER (+12V)
V_{SS}	GROUND

ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to V_{BB} ..... −0.5V to +20V
Voltage on V_{DD}, V_{CC} supplies relative to V_{SS} ..... −1.0V to +15.0V
$V_{BB}-V_{SS}$ ($V_{DD}-V_{SS}>0V$) 0V
Operating temperature, T_A (Ambient) ..... 0°C to + 70°C
Storage temperature (Ambient) ..... −65°C to + 150°C
Short circuit output current 50mA
Power dissipation ..... 1 Watt

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS
($0°C \leq T_A \leq 70°C$)[1]

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{DD} V_{CC} V_{SS} V_{BB}	10.8 4.5 0	12.0 5.0 0 −5.0	13.2 5.5 0	Volts Volts Volts Volts	1 1,2 1 1
Input High (Logic 1) Voltage, $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	V_{IHC}	2.7	–	7.0	Volts	1
Input High (Logic 1) Voltage, all inputs except $\overline{RAS}$, $\overline{CAS}$ $\overline{WRITE}$	V_{IH}	2.4	–	7.0	Volts	1
Input Low (Logic 0) Voltage, all inputs	V_{IL}	−1.0	–	.8	Volts	1

DC ELECTRICAL CHARACTERISTICS
($0°C \leq T_A \leq 70°C$)[1] (V_{DD} = 12.0V ±10%; V_{CC} = 5.0V ±10%; V_{BB} = −5.0V ±10%; V_{SS} = 0V)

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
OPERATING CURRENT Average power supply operating current ($\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = 410ns)	I_{DD1} I_{CC1} I_{BB1}		35 200	mA µA	3 4
STANDBY CURRENT Power supply standby current ($\overline{RAS}$ = V_{IHC}, D_{OUT} = High Impedance)	I_{DD2} I_{CC2} I_{BB2}	 −10 	1.5 10 	mA µA µA	
REFRESH CURRENT Average power supply current, refresh mode ($\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IHC}; t_{RC} = 410ns)	I_{DD3} I_{CC3} I_{BB3}	 −10 	27 10 	mA µA µA	3
PAGE MODE CURRENT Average power supply current, page-mode operation ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling; t_{PC} = 275ns)	I_{DD4} I_{CC4} I_{BB4}		27 	mA µA	3 4
INPUT LEAKAGE Input leakage current, any input (V_{BB} = −5V, $0V \leq V_{IN} \leq +7.0V$, all other pins not under test = 0 volts)	$I_{I(L)}$	−10	10	µA	
OUTPUT LEAKAGE Output leakage current (D_{OUT} is disabled, $0V \leq V_{OUT} \leq +5.5V$)	$I_{O(L)}$	−10	10	µA	
OUTPUT LEVELS Output high (Logic 1) voltage (I_{OUT} = −5mA) Output low (Logic 0) voltage (I_{OUT} = 4.2 mA)	V_{OH} V_{OL}	2.4 	 0.4	Volts Volts	3

NOTES:

1. All voltages referenced to V_{SS}.
2. Output voltage will swing from V_{SS} to V_{CC} when activated with no current loading. For purposes of maintaining data in standby mode, V_{CC} may be reduced to V_{SS} without affecting refresh operations or data retention. However, the V_{OH} (min) specification is not guaranteed in this mode.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (5,6,7)
($0°C \leq T_A \leq 70°C$) (V_{DD} = 12.0V ± 10%; V_{CC} = 5.0V ± 10%, V_{SS} = 0V, V_{BB} = −5.0V ± 10%)

PARAMETER	SYMBOL	MK 4116 MIN	MK 4116 MAX	UNITS	NOTES
Random read or write cycle time	t_{RC}	410		ns	
Read-write cycle time	t_{RWC}	515		ns	
Page mode cycle time	t_{PC}	275		ns	
Access time from $\overline{RAS}$	t_{RAC}		250	ns	8,10
Access time from $\overline{CAS}$	t_{CAC}		165	ns	9,10
Output buffer turn-off delay	t_{OFF}	0	60	ns	11
Transition time (rise and fall)	t_T	3	50	ns	7
$\overline{RAS}$ precharge time	t_{RP}	150		ns	
$\overline{RAS}$ pulse width	t_{RAS}	250	10000	ns	
$\overline{RAS}$ hold time	t_{RSH}	165		ns	
$\overline{CAS}$ pulse width	t_{CAS}	165	10000	ns	
$\overline{CAS}$ hold time	t_{CSH}	250		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	35	85	ns	12
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	−20		ns	
Row Address set-up time	t_{ASR}	0		ns	
Row Address hold time	t_{RAH}	35		ns	
Column Address set-up time	t_{ASC}	−10		ns	
Column Address hold time	t_{CAH}	75		ns	
Column Address hold time referenced to $\overline{RAS}$	t_{AR}	160		ns	
Read command set-up time	t_{RCS}	0		ns	
Read command hold time	t_{RCH}	0		ns	
Write command hold time	t_{WCH}	75		ns	
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	160		ns	
Write command pulse width	t_{WP}	75		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	100		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	100		ns	
Data-in set-up time	t_{DS}	0		ns	13
Data-in hold time	t_{DH}	75		ns	13
Data-in hold time referenced to $\overline{RAS}$	t_{DHR}	160		ns	
$\overline{CAS}$ precharge time (for page-mode cycle only)	t_{CP}	100		ns	
Refresh period	t_{REF}		2	ms	
$\overline{WRITE}$ command set-up time	t_{WCS}	−20		ns	14
$\overline{CAS}$ to $\overline{WRITE}$ delay	t_{CWD}	125		ns	14
$\overline{RAS}$ to $\overline{WRITE}$ delay	t_{RWD}	200		ns	14

3. I_{DD1}, I_{DD3}, and I_{DD4} depend on cycle rate. The maximum specified current values are for t_{RC}=410ns and t_{PC}=275ns. I_{DD} limit at other cycle rates are determined by the following equations:

   I_{DD1} (max) [MA] = 10 + 10.25 x cycle rate [MHz]
   I_{DD3} (max) [MA] = 10 + 7 x cycle rate [MHz]
   I_{DD4} (max) [MA] = 10 + 4.7 x cycle rate [MHz]

4. I_{CC1} and I_{CC4} depend upon output loading. During readout of high level data V_{CC} is connected through a low impedance (135 typ) to data out. At all other times I_{CC} consists of leakage currents only.

5. Several cycles are required after power-up before proper device operation is achieved. Any 8 cycles which perform refresh are adequate for this purpose.

6. AC measurements assume t_T=5ns.

7. V_{IHC} (min) or V_{IH}((min) and V_{IL}(max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IHC} or V_{IH} and V_{IL}.

8. Assumes that $t_{RCD} \leq t_{RCD}$ (max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the value shown.

9. Assumes that $t_{RCD} \geq t_{RCD}$ (max).

10. Measured with a load equivalent to 2 TTL loads and 100pF.

11. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

12. Operation within the t_{RCD} (max) limit insures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.

13. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WRITE}$ leading edge in delayed write or read-modify-write cycles.

14. t_{WCS}, t_{CWD} and t_{RWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only: If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) $\geq t_{RWD}$ (min), the cycle is a read-write cycle and the data out will contain data read from the selected cell; If neither of the above sets of conditions is satisfied the condition of the data out (at access time) is indeterminate.

15. Effective capacitance calculated from the equation $C = \frac{I \Delta t}{\Delta v}$ with Δv = 3 volts and power supplies at nominal levels.

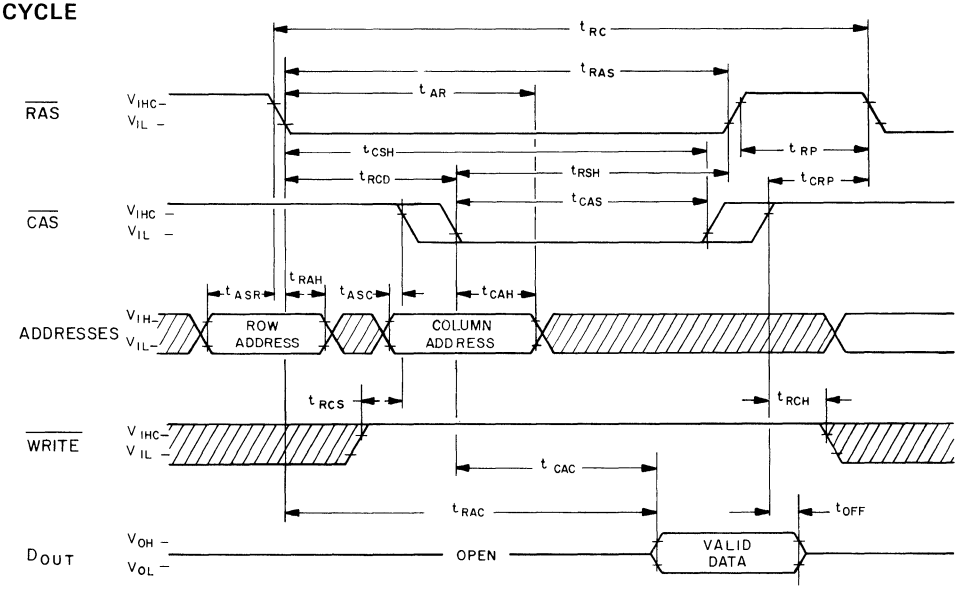
16. $\overline{CAS}$ = V_{IHC} to disable D_{OUT}.

AC ELECTRICAL CHARACTERISTICS

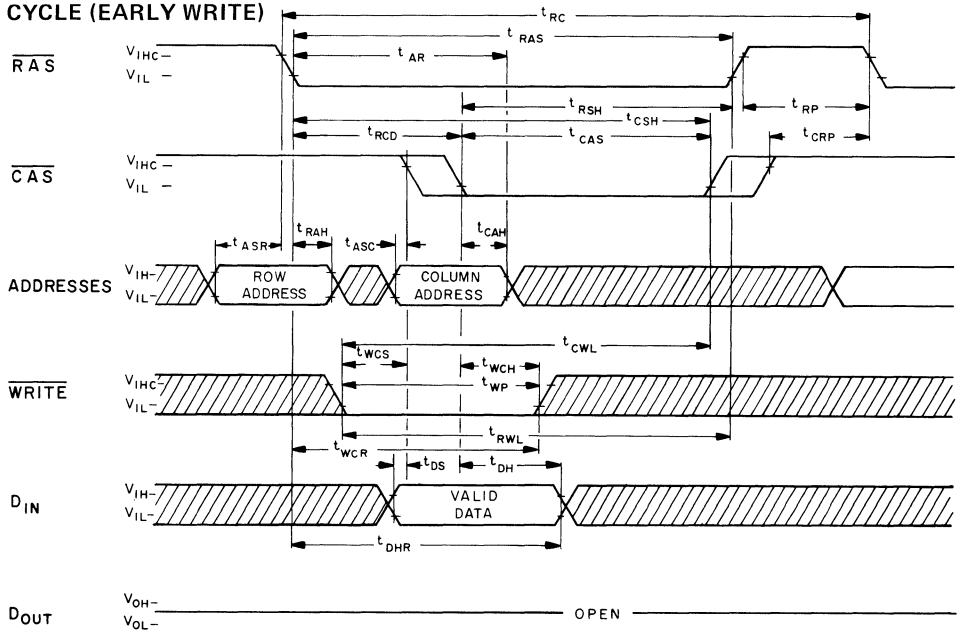
($0°C \leq T_A \leq 70°C$) ($V_{DD} = 12.0V \pm 10\%$; $V_{SS} = 0V$; $V_{BB} = -5.0V \pm 10\%$)

PARAMETER	SYMBOL	TYP	MAX	UNITS	NOTES
Input Capacitance (A_0–A_6), D_{IN}	C_{I1}	4	5	pF	17
Input Capacitance $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	C_{I2}	8	10	pF	17
Output Capacitance (D_{OUT})	C_O	5	7	pF	17,18

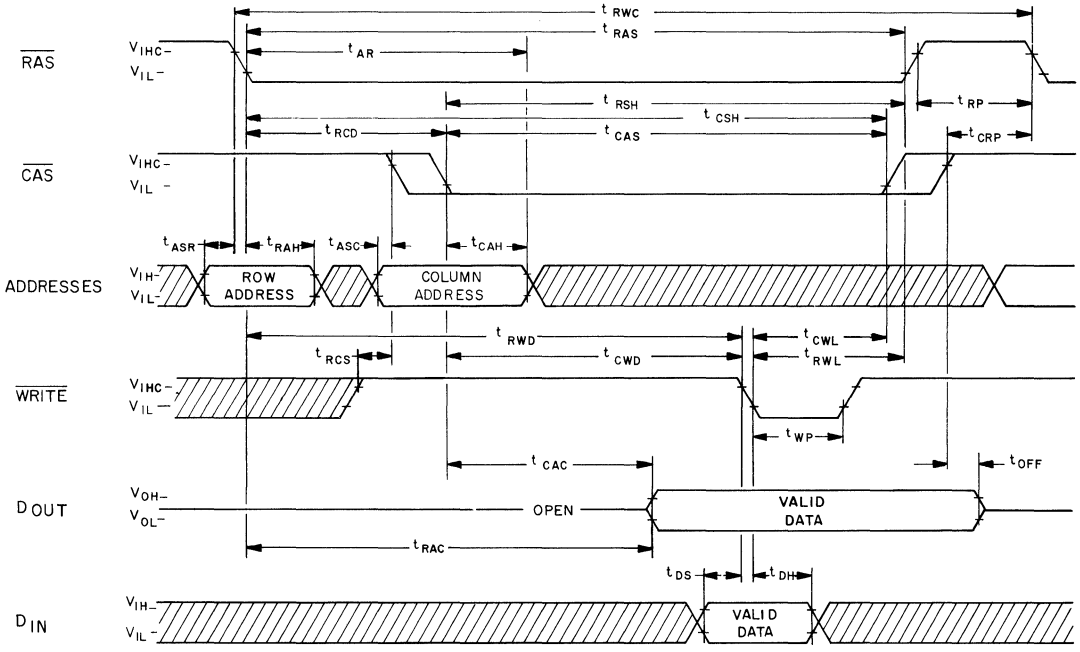
READ CYCLE



WRITE CYCLE (EARLY WRITE)

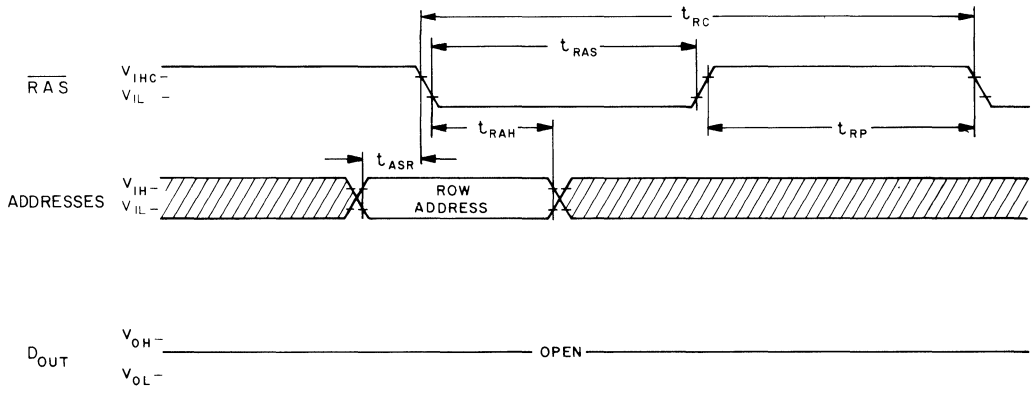


READ–WRITE/READ–MODIFY–WRITE CYCLE

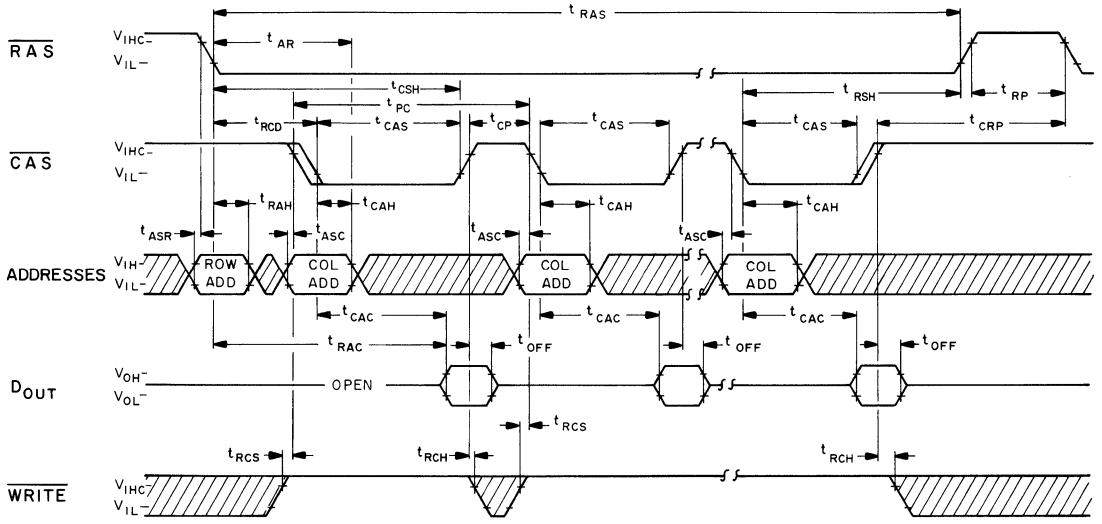


"RAS–ONLY" REFRESH CYCLE

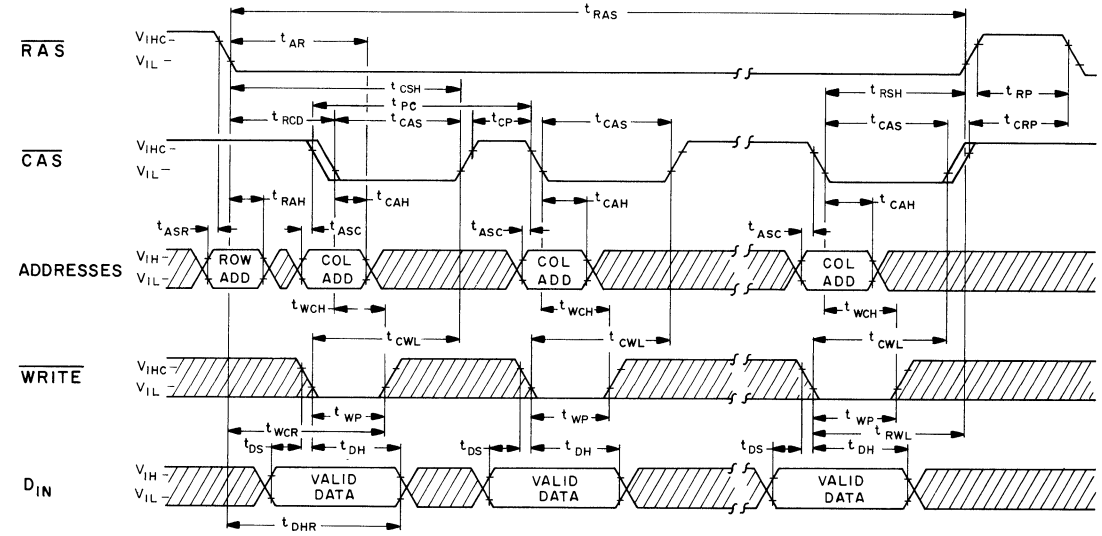
NOTE: $\overline{CAS}$ = V_{IHC}, $\overline{WRITE}$ = Don't Care



PAGE MODE READ CYCLE



PAGE MODE WRITE CYCLE



DESCRIPTION (continued)

System oriented features include ± 10% tolerance on all power supplies, direct interfacing capability with high performance logic families such as Schottky TTL, maximum input noise immunity to minimize "false triggering" of the inputs (a common cause of soft errors), on-chip address and data registers which eliminate the need for interface registers, and two chip select methods to allow the user to determine the appropriate speed/power characteristics of his memory system. The MK 4116 also incorporates several flexible timing/operating modes. In addition to the usual read, write, and read-modify-write cycles, the MK 4116 is capable of delayed write cycles, page-mode operation and RAS-only refresh. Proper control of the clock inputs($\overline{RAS}$, $\overline{CAS}$ and $\overline{WRITE}$) allows common I/O capability, two dimensional chip selection, and extended page boundaries (when operating in page mode).

ADDRESSING

The 14 address bits required to decode 1 of the 16,384 cell locations within the MK 4116 are multiplexed onto the 7 address inputs and latched into the on-chip address latches by externally applying two negative going TTL-level clocks. The first clock, the Row Address Strobe ($\overline{RAS}$), latches the 7 row address bits into the chip. The second clock, the Column Address Strobe ($\overline{CAS}$), subsequently latches the 7 column address bits into the chip. Each of these signals, $\overline{RAS}$ and $\overline{CAS}$, triggers a sequence of events which are controlled by different delayed internal clocks. The two clock chains are linked together logically in such a way that the address multiplexing operation is done outside of the critical path timing sequence for read data access. The later events in the $\overline{CAS}$ clock sequence are inhibited until the occurence of a delayed signal derived from the $\overline{RAS}$ clock chain. This "gated $\overline{CAS}$" feature allows the $\overline{CAS}$ clock to be externally activated as soon as the Row Address Hold Time specification (t_{RAH}) has been satisfied and the address inputs have been changed from Row address to Column address information.

Note that $\overline{CAS}$ can be activated at any time after t_{RAH} and it will have no effect on the worst case data access time (t_{RAC}) up to the point in time when the delayed row clock no longer inhibits the remaining sequence of column clocks. Two timing endpoints result from the internal gating of $\overline{CAS}$ which are called t_{RCD} (min) and t_{RCD} (max). No data storage or reading errors will result if $\overline{CAS}$ is applied to the MK 4116 at a point in time beyond the t_{RCD} (max) limit. However, access time will then be determined exclusively by the access time from $\overline{CAS}$ (t_{CAC}) rather than from $\overline{RAS}$ (t_{RAC}), and access time from $\overline{RAS}$ will be lengthened by the amount that t_{RCD} exceeds the t_{RCD} (max) limit.

DATA INPUT/OUTPUT

Data to be written into a selected cell is latched into an on-chip register by a combination of $\overline{WRITE}$ and $\overline{CAS}$ while $\overline{RAS}$ is active. The later of the signals ($\overline{WRITE}$ or $\overline{CAS}$) to make its negative transition is the strobe for the Data In (D_{IN}) register. This permits several options in the write cycle timing. In a write cycle, if the $\overline{WRITE}$ input is brought low (active) prior to $\overline{CAS}$, the D_{IN} is strobed by $\overline{CAS}$, and the set-up and hold times are referenced to $\overline{CAS}$. If the input data is not available at $\overline{CAS}$ time or if it is desired that the cycle be a read-write cycle, the $\overline{WRITE}$ signal will be delayed until after $\overline{CAS}$ has made its negative transition. In this "delayed write cycle" the data input set-up and hold times are referenced to the negative edge of $\overline{WRITE}$ rather than $\overline{CAS}$. (To illustrate this feature, D_{IN} is referenced to $\overline{WRITE}$ in the timing diagrams depicting the read-write and page-mode write cycles while the "early write" cycle diagram shows D_{IN} referenced to $\overline{CAS}$).

Data is retrieved from the memory in a read cycle by maintaining $\overline{WRITE}$ in the inactive or high state throughout the portion of the memory cycle in which $\overline{CAS}$ is active (low). Data read from the selected cell will be available at the output within the specified access time.

DATA OUTPUT CONTROL

The normal condition of the Data Output (D_{OUT}) of the MK 4116 is the high impedance (open-circuit) state. That is to say, anytime $\overline{CAS}$ is at a high level, the D_{OUT} pin will be floating. The only time the output will turn on and contain either a logic 0 or logic 1 is at access time during a read cycle. D_{OUT} will remain valid from access time until $\overline{CAS}$ is taken back to the inactive (high level) condition.

If the memory cycle in progress is a read, read-modify write, or a delayed write cycle, then the data output will go from the high impedance state to the active condition, and at access time will contain the data read from the selected cell. This output data is the same polarity (not inverted) as the input data. Once having gone active, the output will remain valid until $\overline{CAS}$ is taken to the precharge (logic 1) state, whether or not $\overline{RAS}$ goes into precharge.

If the cycle in progress is an "early-write" cycle ($\overline{WRITE}$ active before $\overline{CAS}$ goes active), then the output pin will maintain the high impedance state throughout the entire cycle. Note that with this type of output configuration, the user is given full control of the D_{OUT} pin simply by controlling the placement of $\overline{WRITE}$ command during a write cycle, and the pulse width of the Column Address Strobe during read operations. Note also that even though data is not latched at the output, data can remain valid from access time until the beginning of a subsequent cycle without paying any penalty in overall memory cycle time (stretching the cycle).

This type of output operation results in some very significant system implications.

Common I/O Operation – If all write operations are handled in the "early write" mode, then D_{IN} can be connected directly to D_{OUT} for a common I/O data bus.

Data Output Control – D_{OUT} will remain valid during a read cycle from t_{CAC} until $\overline{CAS}$ goes back to a high level (precharge), allowing data to be valid from one cycle up until a new memory cycle begins with no penalty in cycle time. This also makes the $\overline{RAS}/\overline{CAS}$ clock timing relationship very flexible.

Two Methods of Chip Selection – Since D_{OUT} is not latched, $\overline{CAS}$ is not required to turn off the outputs of unselected memory devices in a matrix. This means that both $\overline{CAS}$ and/or $\overline{RAS}$ can be decoded for chip selection. If both $\overline{RAS}$ and $\overline{CAS}$ are decoded, then a two dimensional (X,Y) chip select array can be realized.

Extended Page Boundary – Page-mode operation allows for successive memory cycles at multiple column locations of the same row address. By decoding $\overline{CAS}$ as a page cycle select signal, the page boundary can be extended beyond the 128 column locations in a single chip. (See page-mode operation).

OUTPUT INTERFACE CHARACTERISTICS

The three state data output buffer presents the data output pin with a low impedance to V_{CC} for a logic 1 and a low impedance to V_{SS} for a logic 0. The effective resistance to V_{CC} (logic 1 state) is 420 Ω maximum and 135Ω typically. The resistance to V_{SS} (logic 0 state) is 95 Ω maximum and 35 Ω typically. The separate V_{CC} pin allows the output buffer to be powered from the supply voltage of the logic to which the chip is interfaced. During battery standby operation, the V_{CC} pin may have power removed without affecting the MK 4116 refresh operation. This allows all system logic except the $\overline{RAS}$ timing circuitry and the refresh address logic to be turned off during battery standby to conserve power.

PAGE MODE OPERATION

The "Page Mode" feature of the MK 4116 allows for successive memory operations at multiple column locations of the same row address with increased speed without an increase in power. This is done by strobing the row address into the chip and maintaining the $\overline{RAS}$ signal at a logic 0 throughout all successive memory cycles in which the row address is common. This "page-mode" of operation will not dissipate the power associated with the negative going edge of $\overline{RAS}$. Also, the time required for strobing in a new row address is eliminated, thereby decreasing the access and cycle times.

The page boundary of a single MK 4116 is limited to the 128 column locations determined by all combinations of the 7 column address bits. However, in system applications which utilize more than 16,384 data words, (more than one 16K memory block), the page boundary can be extended by using $\overline{CAS}$ rather than $\overline{RAS}$ as the chip select signal. $\overline{RAS}$ is applied to all devices to latch the row address into each device and then $\overline{CAS}$ is decoded and serves as a page cycle select signal. Only those devices which receive both $\overline{RAS}$ and $\overline{CAS}$ signals will execute a read or write cycle.

REFRESH

Refresh of the dynamic cell matrix is accomplished by performing a memory cycle at each of the 128 row addresses within each 2 millisecond time interval. Although any normal memory cycle will perform the refresh operation, this function is most easily accomplished with "$\overline{RAS}$-only" cycles. $\overline{RAS}$-only refresh results in a substantial reduction in operating power. This reduction in power is reflected in the I_{DD3} specification.

POWER CONSIDERATIONS

Most of the circuitry used in the MK 4116 is dynamic and most of the power drawn is the result of an address strobe edge. Consequently, the dynamic power is primarily a function of operating frequency rather than active duty cycle (refer to the MK 4116 current waveforms in figure 5). This current characteristic of the MK 4116 precludes inadvertent burn out of the device in the event that the clock inputs become shorted to ground due to system malfunction.

Although no particular power supply noise restriction exists other than the supply voltages remain within the specified tolerance limits, adequate decoupling should be provided to suppress high frequency noise resulting from the transient current of the device. This insures optimum system performance and reliability. Bulk capacitance requirements are minimal since the MK 4116 draws very little steady state (DC) current.

In system applications requiring lower power dissipations, the operating frequency (cycle rate) of the MK 4116 can be reduced and the (guaranteed maximum) average power dissipation of the device will be lowered in accordance with the I_{DD1} (max) spec limit equation shown in Note 3. NOTE: The MK 4116 P-4 is guaranteed to have a maximum I_{DD1} requirement of 35mA @ 410ns cycle with an ambient temperature range from 0° to 70°C. A lower operating frequency, for example 1 microsecond cycle, results in a reduced maximum I_{DD1} requirement of under 20mA with an ambient temperature range from 0° to 70°C.

Although $\overline{RAS}$ and/or $\overline{CAS}$ can be decoded and used as a chip select signal for the MK 4116, overall system power is minimized if the Row Address Strobe ($\overline{RAS}$) is used for this purpose. All unselected devices (those which do not receive a $\overline{RAS}$) will remain in a low power (standby) mode regardless of the state of $\overline{CAS}$.

Fig. 5 Typical Current Waveforms

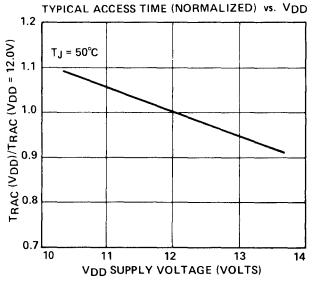
POWER UP

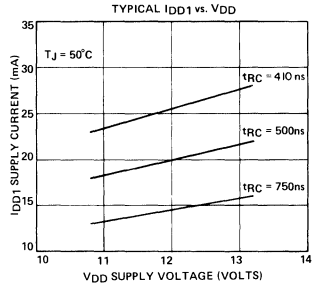
The MK 4116 requires no particular power supply sequencing so long as the Absolute Maximum Rating Conditions are observed. However, in order to insure compliance with the Absolute Maximum Ratings, MOSTEK recommends sequencing of power supplies such that V_{BB} is applied first and removed last. V_{BB} should never be more positive than V_{SS} when power is applied to V_{DD}.

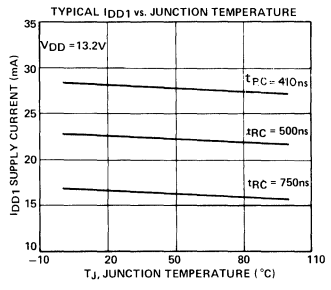
Under system failure conditions in which one or more supplies exceed the specified limits significant additional margin against catastrophic device failure may be achieved by forcing $\overline{RAS}$ and $\overline{CAS}$ to the inactive state (high level).

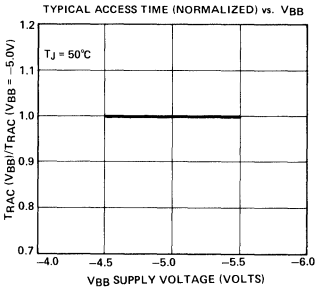
After power is applied to the device, the MK 4116 requires several cycles before proper device operation is achieved. Any 8 cycles which perform refresh are adequate for this purpose.

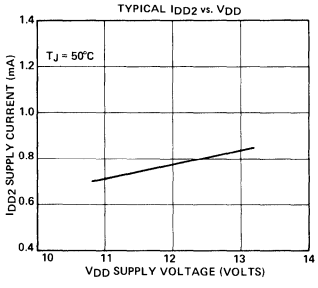
TYPICAL CHARACTERISTICS

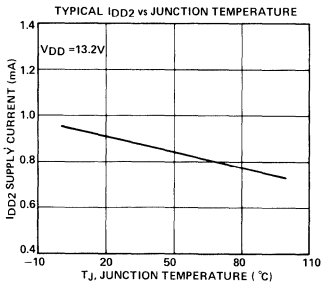


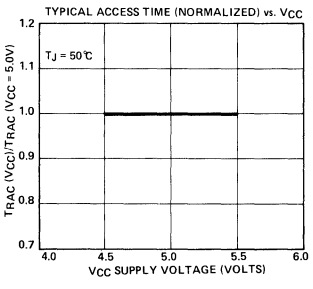


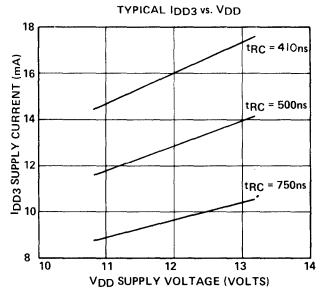


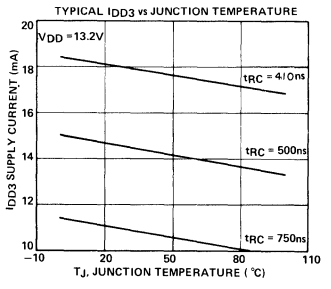


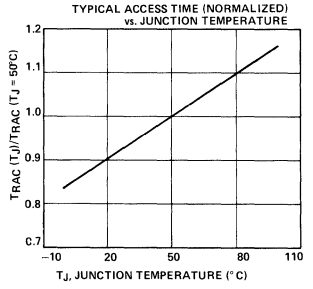


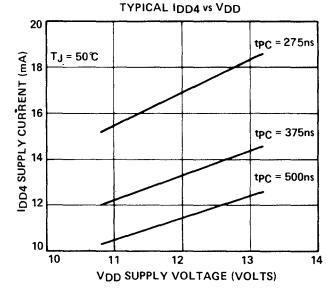


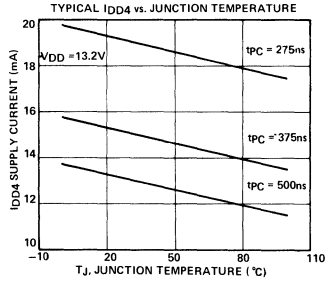




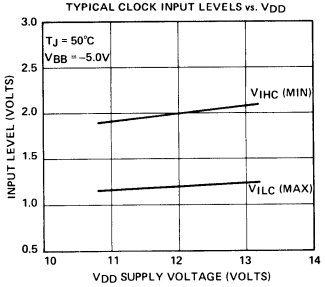




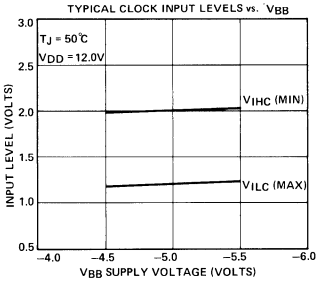




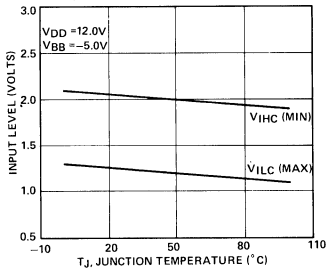
TYPICAL CLOCK INPUT LEVELS vs. V_{DD}



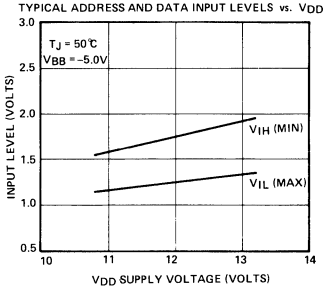
TYPICAL CLOCK INPUT LEVELS vs. V_{BB}



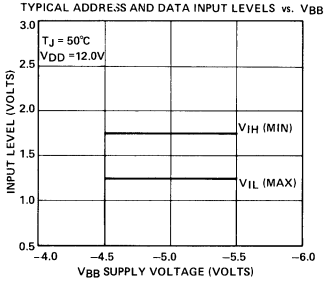
TYPICAL CLOCK INPUT LEVELS vs. T_J



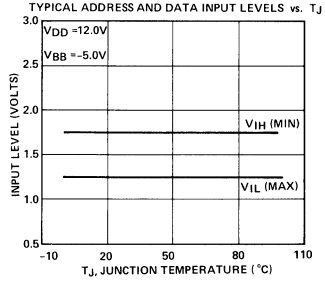
TYPICAL ADDRESS AND DATA INPUT LEVELS vs. V_{DD}



TYPICAL ADDRESS AND DATA INPUT LEVELS vs. V_{BB}



TYPICAL ADDRESS AND DATA INPUT LEVELS vs. T_J



4K STATIC

MOSTEK's 4096-bit static RAM family consists of 5V-only, TTL compatible 4K x 1 and 1K x 4 common I/O components designed to cover all static memory applications. The static RAMs combine the best characteristics of static and dynamic circuit techniques to achieve a highly reliable, low power, high performance memory device designed for ease of system implementation.

PRELIMINARY

MOSTEK

4096 x 1 BIT STATIC RAM

MK 4104 (P/N) -3/-4/-5

FEATURES

- ☐ Combination static storage cells and dynamic control circuitry for truly high performance

Part Number	Access Time	Cycle Time
MK 4104–3	200ns	310ns
MK 4104–4	250ns	385ns
MK 4104–5	300ns	460ns

- ☐ Average Power Dissipation less than 120mW
- ☐ Standby Power Dissipation less than 28 mW
- ☐ Single +5V Power Supply (± 10% tolerance)
- ☐ Fully TTL Compatible

  Fanout: 2 – Standard TTL
  2 – Schottky TTL
  12 – Low Power Schottky TTL

- ☐ Standard 18-pin DIP

DESCRIPTION

The MOSTEK MK 4104 is a high performance static random access memory organized as 4096 one bit words. The MK 4104 combines the best characteristics of static and dynamic memory techniques to achieve a TTL compatible, 5 volt only, high performance, low power memory device. It utilizes advanced circuit design concepts and an innovative state-of-the-art N-channel silicon gate process specially tailored to provide static data storage with the performance (speed and power) of dynamic RAMs. Since the storage cell is static the device may be stopped indefinitely with the $\overline{CE}$ clock in the off (Logic 1) state.

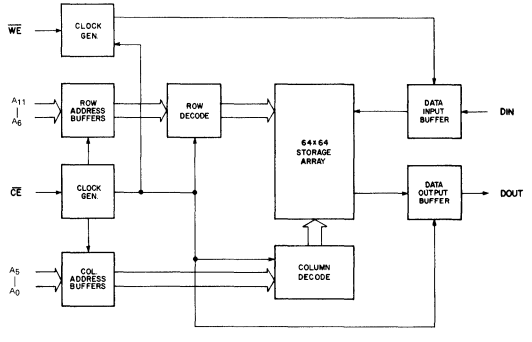
All input levels, including write enable ($\overline{WE}$) and chip enable ($\overline{CE}$) are true TTL with a one level of 2.0 volts and a zero level of 0.8 volts. This gives the system designer for a logic "1" state, at least 400mV of noise margin when driven by standard TTL and a minimum of 700 mV when used with high performance Schottky TTL. These margins are wider than on most TTL compatible MOS memories available. The push-pull output (no pull-up resistor required) delivers a one level of 2.4V minimum and a zero level of .4 volts maximum. The output has a fanout of 2 standard TTL loads or 12 low power Schottky loads.

The RAM employs an innovative static cell which occupies a mere 2.75 square mils (½ the area of previous cells) and dissipates power levels comparable to CMOS. The static cell eliminates the need for refresh cycles and associated hardware thus allowing easy system implementation.

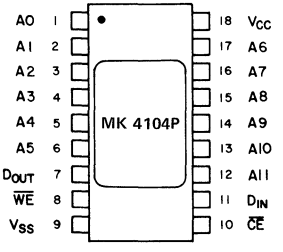
Power supply requirements of +5V ± 10% tolerance combined with TTL compatability on all I/O pins permits easy integration into large memory configurations. The single supply reduces capacitor count and permits denser packaging on printed circuit boards. The 5V only supply requirement and TTL compatible I/O makes this part an ideal choice for next generation +5V only microprocessors such as MOSTEK's Z80 and MK3870. The early write mode ($\overline{WE}$ active prior to $\overline{CE}$) permits common I/O operation, needed for Z80 interfacing, without external circuitry.

Reliability is greatly enhanced by the low power dissipation which causes a maximum junction rise of only 8°C at 3.2 Megahertz operation. The MK 4104 was designed for the system designer and user who require the highest performance available along with MOSTEK's proven reliability.

FUNCTIONAL DIAGRAM



PIN CONNECTIONS



PIN NAMES

A_0 - A_{11}	ADDRESS INPUTS	V_{SS}	GROUND
$\overline{CE}$	CHIP ENABLE	V_{CC}	POWER (+5V)
D_{IN}	DATA INPUT	$\overline{WE}$	WRITE ENABLE
D_{OUT}	DATA OUTPUT		

ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to V_{SS} . . . . . −1.0V to +7.0V
Operating Temperature T_A (Ambient) . . . . . 0° C to + 70° C
Storage Temperature (Ambient) (Ceramic) . . . . . −65° C to +150° C
Storage Temperature (Ambient) (Plastic) . . . . . −55° C to +125° C
Power Dissipation . . . . . 1 Watt
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS[6]

(0° C ≤ T_A ≤ + 70° C)

	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	Volts	1
V_{SS}	Supply Voltage	0	0	0	Volts	1
V_{IH}	Logic "1" Voltage All Inputs	2.0		7.0	Volts	1
V_{IL}	Logic "0" Voltage All Inputs	−1.0		0.8	Volts	1

DC ELECTRICAL CHARACTERISTICS

(0° C ≤ T_A ≤ + 70° C) (V_{CC} = 5.0 volts ± 10%)

	PARAMETER	MIN	MAX	UNITS	NOTES
I_{CC1}	Average V_{CC} Power Supply Current		21	mA	2
I_{CC2}	Standby V_{CC} Power Supply Current		5	mA	3
I_{IL}	Input Leakage Current (Any Input)	−10	10	μA	4
I_{OL}	Output Leakage Current	−10	10	μA	3, 5
V_{OH}	Output Logic "1" Voltage I_{OUT}=−500μA	2.4		Volts	11
V_{OL}	Output Logic "0" Voltage I_{OUT}= 5mA		0.4	Volts	11

AC ELECTRICAL CHARACTERISTICS

(0° C ≤ T_A ≤ + 70° C) (V_{CC} = + 5.0 volts ±10%)

	PARAMETER	MIN	TYP	MAX	NOTES
C_I	Input Capacitance		4pF		14
C_O	Output Capacitance		7pF		14

NOTES:

1. All voltages referenced to V_{SS}.
2. I_{CC1} is related to precharge and cycle times. Guaranteed maximum values for I_{CC1} may be calculated by
$$I_{CC1}[mA] = (5t_P + 13(t_C - t_P) + 3420) \div t_C$$
where t_P and t_C are expressed in nanoseconds.
3. Output is disabled (open circuit), $\overline{CE}$ is at logic 1.
4. All device pins at 0 volts except pin under test at 5.5 volts.
5. $0V \leq V_{OUT} \leq +5.5V$.
6. During power up, $\overline{CE}$ and $\overline{WE}$ must be at V_{IH} for minimum of 2ms after V_{CC} reaches 4.5V, before a valid memory cycle can be accomplished.
7. Measured with load circuit equivalent to 2 TTL loads and CL = 100 pF.
8. If $\overline{WE}$ follows after $\overline{CE}$ then data out may not remain open circuited.
9. Determined by user. Total cycle time cannot exceed t_{CE} max.
10. Data-in set-up time is referenced to the later of the two falling clock edges $\overline{CE}$ or $\overline{WE}$.
11. AC measurements assume t_T = 5ns. Timing points are taken as V_{IL} = 0.8V and V_{IH} = 2.0V on the inputs and V_{OL} = 0.4V and V_{OH} = 2.4V on the output waveform.
12. $T_C = t_{CE} + t_P + 2t_T$.
13. The true level of the output in the open circuit condition will be determined totally by output load conditions. The output is guaranteed to be open circuit within t_{OFF}.
14. Effective capacitance calculated from the equation $C = I\frac{\Delta t}{\Delta V}$ with ΔV equal to 3V and V_{CC} nominal.
15. For RMW, $t_{CE} = t_{AC} + t_{WPL} + t_{MOD}$.
16. $t_C = t_{AC} + t_{WPL} + t_P + 2t_T + t_{MOD}$.

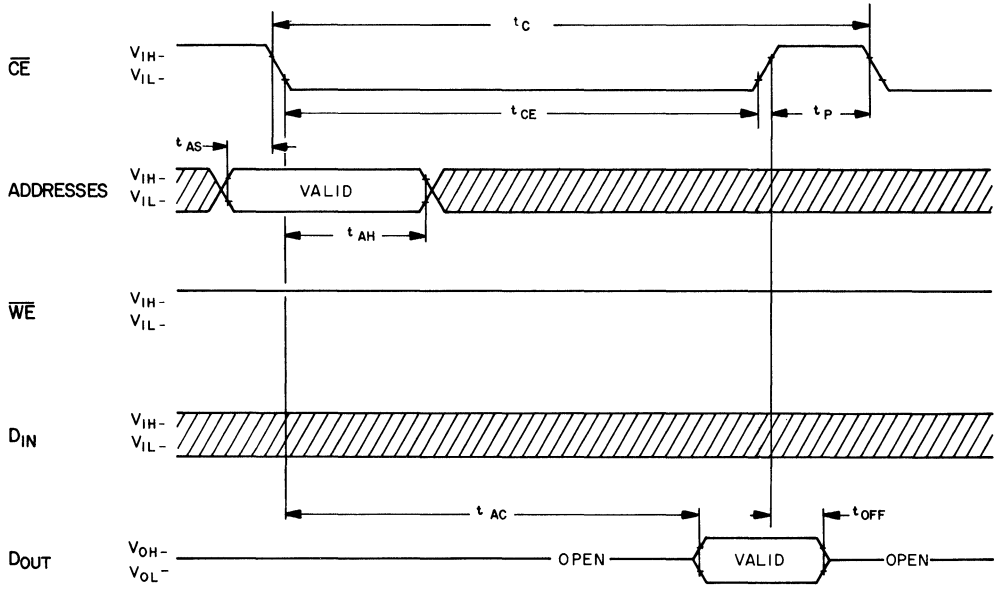
AC ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS[6, 11]

(0°C ≤ T_A ≤ +70°C) (V_{CC} = +5.0 volts ±10%)

PARAMETER		MK 4104–3		MK 4104–4		MK 4104–5		UNIT	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX		
t_C	Read or Write Cycle Time	310		385		460		ns	12
t_{AC}	Random Access		200		250		300	ns	7
t_{CE}	Chip Enable Pulse Width	200	10,000	250	10,000	300	10,000	ns	15
t_P	Chip Enable Precharge Time	100		125		150		ns	
t_{AH}	Address Hold Time	110		135		165		ns	
t_{AS}	Address Set-Up Time	0		0		0		ns	
t_{OFF}	Output Buffer Turn-Off Delay	0	50	0	65	0	75	ns	13
t_{WS}	Write Enable Set-Up Time	–20		–20		–20		ns	8
t_{DIH}	Data Input Hold Time	25		25		25		ns	
t_{WW}	Write Enabled Pulse Width	60		75		90		ns	
t_{MOD}	Modify Time	0	10,000	0	10,000	0	10,000	ns	9
t_{WPL}	$\overline{WE}$ to $\overline{CE}$ Precharge Lead Time	70		85		105		ns	10
t_{DS}	Data Input Set-Up Time	0		0		0		ns	
t_{WH}	Write Enable Hold Time	150		185		225		ns	
t_T	Transition Time	5	50	5	50	5	50	ns	
t_{RMW}	Read-Modify-Write Cycle Time	380		470		565		ns	16

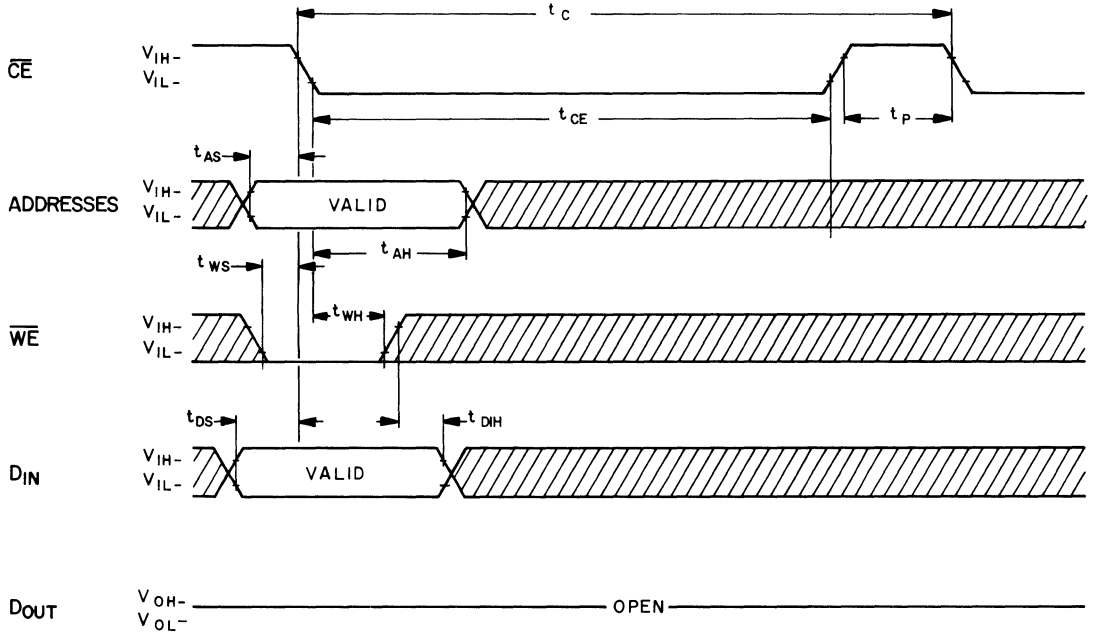
TIMING WAVEFORMS

READ CYCLE

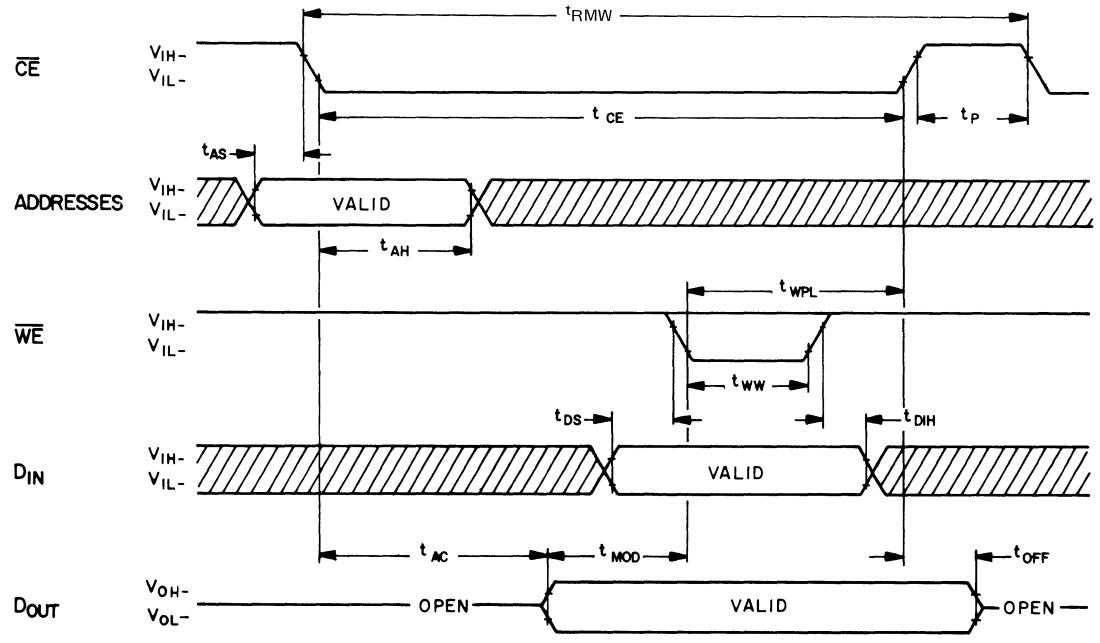


TIMING WAVEFORMS

WRITE CYCLE



READ-MODIFY-WRITE CYCLE



OPERATION

READ CYCLE

The circuit offers one bit of the possible 4096 by decoding the 12 address bits presented at the inputs. The address bits are strobed into the chip by the negative-going edge of the Chip Enable ($\overline{CE}$) clock. A read cycle is accomplished by holding the 'write enable' ($\overline{WE}$) input at a high level (V_{IH}) while clocking the $\overline{CE}$ input to a low level (V_{IL}). At access time (t_{AC}) valid data will appear at the output. The output is unlatched by a positive transition of $\overline{CE}$ and therefore will be open circuited (high impedance state) from the previous cycle to access time and will go open again at the end of the present cycle when $\overline{CE}$ goes high.

Once the address hold time has been satisfied, the addresses may be changed for the next cycle.

WRITE CYCLE

Data that is to be written into a selected cell is strobed into the chip on the later occurring negative edge of $\overline{CE}$ or $\overline{WE}$. If the negative transition of $\overline{WE}$ occurs prior to the leading edge of $\overline{CE}$ as in an "early" write cycle then the $\overline{CE}$ input serves as the strobe for data-in. If $\overline{CE}$ leading edge occurs prior to the leading edge of $\overline{WE}$ as in a read-modify-write cycle then data-in is strobed by the $\overline{WE}$ input. In either type of cycle data-in must remain valid for a minimum time period following the positive going edge of $\overline{WE}$. This time is specified by the parameter t_{DIH} (data input hold time).

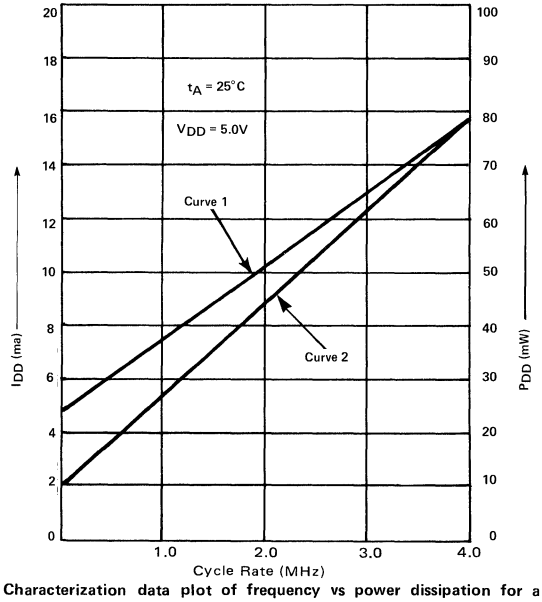
In an 'early' write cycle the output will remain in an open or high impedance state. In a read-modify write operation the output will go active (valid one/zero) at access time and remain active through the modify and write period until $\overline{CE}$ goes to precharge V_{IH}). If the cycle is such that $\overline{WE}$ goes active after $\overline{CE}$ but before valid data appears on the output (prior to t_{AC}) then the output may not remain open. However, if data-in is valid on the leading edge of $\overline{WE}$, and $\overline{WE}$ occurs prior to the positive transition of $\overline{CE}$ by the minimum lead time t_{WPL}, then valid data will be written into the selected cell.

READ-MODIFY-WRITE CYCLE

The read-modify-write (RMW) cycle is no more than an extension of the read and write cycles. Data is read at access time, modified during a period determined by the user and the same or new data written between $\overline{WE}$ active (low) and the rising edge of $\overline{CE}$ (t_{WPL}). Data out will remain valid until the rising edge of $\overline{CE}$. A minimum RMW cycle time can be approximated by the following equation (t_{RMW} = RMW cycle time and t_P = $\overline{CE}$ precharge time).

$$t_{RMW} = t_{AC} + t_{MOD} + t_{WPL} + t_P + 2t_T$$

OPERATING POWER VS CYCLE TIME



Characterization data plot of frequency vs power dissipation for a typical MK 4104 device.

Curve 1 – Clock on time (low level) is bottom scale minus 100 NSEC

Curve 2 – Clock off time (high level) is bottom scale minus 200 NSEC

PRELIMINARY

(SUBJECT TO CHANGE)

MOSTEK

1024x4 BIT STATIC RAM

MK 4114 (P/N) -3/-4/-5

FEATURES

- ☐ Combination static storage cells and dynamic control circuitry for truly high performance

Part Number	Access Time
MK 4114–3	200ns
MK 4114–4	250ns
MK 4114–5	300ns

- ☐ Average Power Dissipation less than 150mW
- ☐ Standby Power Dissipation less than 28 mW
- ☐ Single +5V Power Supply (± 10% tolerance)
- ☐ Fully TTL Compatible
  Fanout: 2 – Standard TTL
  2 – Schottky TTL
  12 – Low Power Schottky TTL
- ☐ Common Data I/O
- ☐ Standard 18-pin DIP
- ☐ 1K x 4 organization

DESCRIPTION

The MOSTEK MK 4114 is a high performance static random access memory organized as 1024 x 4 bit words. The MK 4114 combines the best characteristics of static and dynamic memory techniques to achieve a TTL compatible, 5 volt only, high performance, low power memory device. It utilizes advanced circuit design concepts and an innovative state-of-the-art N-channel silicon gate process specially tailored to provide static data storage with the performance (speed and power) of dynamic RAMs. Since the storage cell is static the device may be stopped indefinitely with the $\overline{CE}$ clock in the off (Logic 1) state.

All input levels, including write enable ($\overline{WE}$) and chip enable ($\overline{CE}$) are true TTL with a one level of 2.0 volts and a zero level of 0.8 volts. This gives the system designer for a logic "1" state, at least 400mV of noise margin when driven by standard TTL and a minimum of 700mV when used with high performance Schottky TTL. These margins are wider than on most TTL compatible MOS memories available.

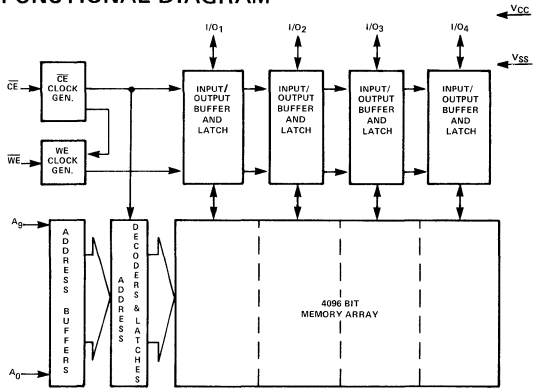
The push-pull output (no pull-up resistor required) delivers a one level of 2.4V minimum and a zero level of .4 volts maximum. The output has a fanout of 2 standard TTL loads or 12 low power Schottky loads.

The RAM employs an innovative static cell which occupies a mere 2.75 square mils (½ the area of previous cells) and dissipates power levels comparable to CMOS. The static cell eliminates the need for refresh cycles and associated hardware thus allowing easy system implementation.

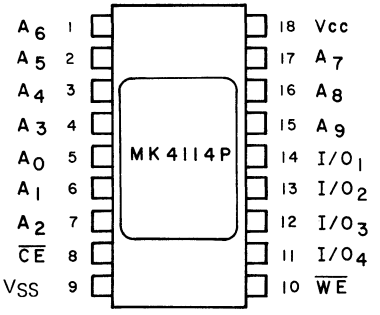
Power supply requirements of +5V ± 10% tolerance combined with TTL compatability on all I/0 pins permits easy integration into large memory configurations. The single supply reduces capacitor count and permits denser packaging on printed circuit boards. The 5V only supply requirement and TTL compatible I/0 makes this part an ideal choice for next generation +5V only microprocessors such as MOSTEK's Z80 and MK 3870. The common I/O operation permits simple interfacing to microprocessors such as the Z80.

Reliability is greatly enhanced by the low power dissipation which causes a maximum junction rise of only 8° C at 3.2 Megahertz operation. The MK 4114 was designed for the system designer and user who require the highest performance available along with MOSTEK's proven reliability.

FUNCTIONAL DIAGRAM



PIN CONNECTIONS



ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to V_{SS} . . . . . −1.0V to +7.0V
Operating Temperature T_A (Ambient) . . . . . 0° C to + 70° C
Storage Temperature (Ambient) (Ceramic) . . . . . −65° C to +150° C
Storage Temperature (Ambient) (Plastic) . . . . . −55° C to +125° C
Power Dissipation . . . . . 1 Watt
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS[6]

(0° C ≤ T_A ≤ + 70° C)

	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	Volts	1
V_{SS}	Supply Voltage	0	0	0	Volts	1
V_{IH}	Logic "1" Voltage All Inputs	2.0		7.0	Volts	1
V_{IL}	Logic "0" Voltage All Inputs	−1.0		0.8	Volts	1

DC ELECTRICAL CHARACTERISTICS

(0° C ≤ T_A ≤ + 70° C) (V_{CC} = 5.0 volts ± 10%)

	PARAMETER	MIN	MAX	UNITS	NOTES
I_{CC1}	Average V_{CC} Power Supply Current		27	mA	2
I_{CC2}	Standby V_{CC} Power Supply Current		5	mA	3
I_{IL}	Input Leakage Current (Any Input)	−10	10	μA	4
I_{OL}	Output Leakage Current	−10	10	μA	3, 5
V_{OH}	Output Logic "1" Voltage I_{OUT}= −500μA	2.4		Volts	11
V_{OL}	Output Logic "0" Voltage I_{OUT}= 5mA		0.4	Volts	11

AC ELECTRICAL CHARACTERISTICS

(0° C ≤ T_A ≤ + 70° C) (V_{CC} = + 5.0 volts ±10%)

	PARAMETER	MIN	TYP	MAX	NOTES
C_I	Input Capacitance		4pF		14
C_O	Input/Output Capacitance		12pF		14

NOTES:

1. All voltages referenced to V_{SS}.
2. I_{CC1} is related to precharge and cycle times.
3. Output is disabled (open circuit), $\overline{CE}$ is at logic 1.
4. All device pins at 0 volts except pin under test at 5.5 volts.
5. 0V ≤ V_{OUT} ≤ + 5.5V.
6. During power up, $\overline{CE}$ and $\overline{WE}$ must be at V_{IH} for minimum of 2ms after V_{CC} reaches 4.5V, before a valid memory cycle can be accomplished.
7. Measured with load circuit equivalent to 2 TTL loads and CL = 100 pF.
8. Ref to $\overline{CE}$ if $\overline{WE}$ goes to a "1" before $\overline{WE}$.
9. Determined by user. Total cycle time cannot exceed t_{CE} max.
10. Data-in set-up time is referenced to the later of the two falling clock edges $\overline{CE}$ or $\overline{WE}$ for early write. Referenced to trailing edge of $\overline{WE}$ for R-M-W.
11. AC measurements assume t_T = 5ns. Timing points are taken as V_{IL} = 0.8V and V_{IH} = 2.0V on the inputs and V_{OL} = 0.4V and V_{OH} = 2.4V on the output waveform.
12. $T_C = t_{CE} + t_P + 2t_T$.
13. The true level of the output in the open circuit condition will be determined totally by output load conditions. The output is guaranteed to be open circuit within t_{OFF}.
14. Effective capacitance calculated from the equation $C = I\frac{\Delta t}{\Delta V}$ with Δ V equal to 3V and V_{CC} nominal.
15. For RMW $t_{CE} = t_{AC} + t_{WPL} + t_{MOD}$.
16. $t_C = t_{AC} + t_{WPL} + t_P + 2t_T + t_{MOD}$.

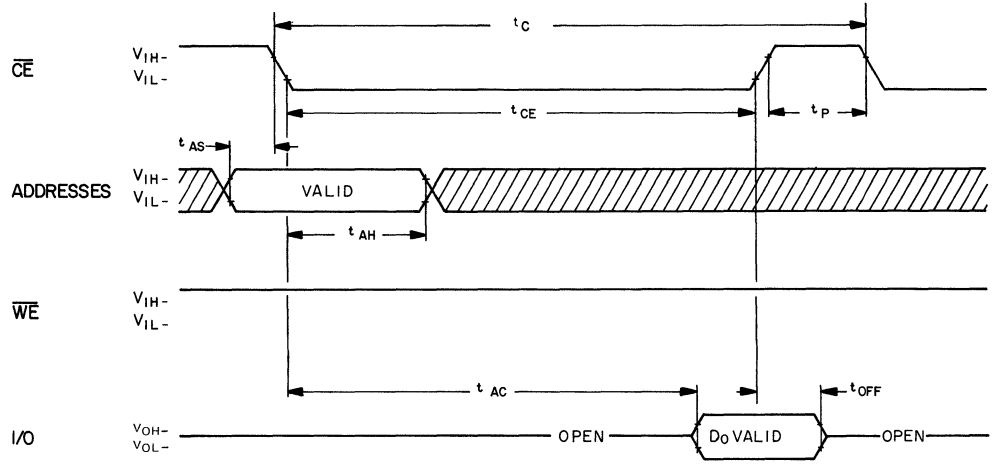
AC ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS[6, 11]

($0°C \leq T_A \leq +70°C$) ($V_{CC} = +5.0$ volts ±10%)

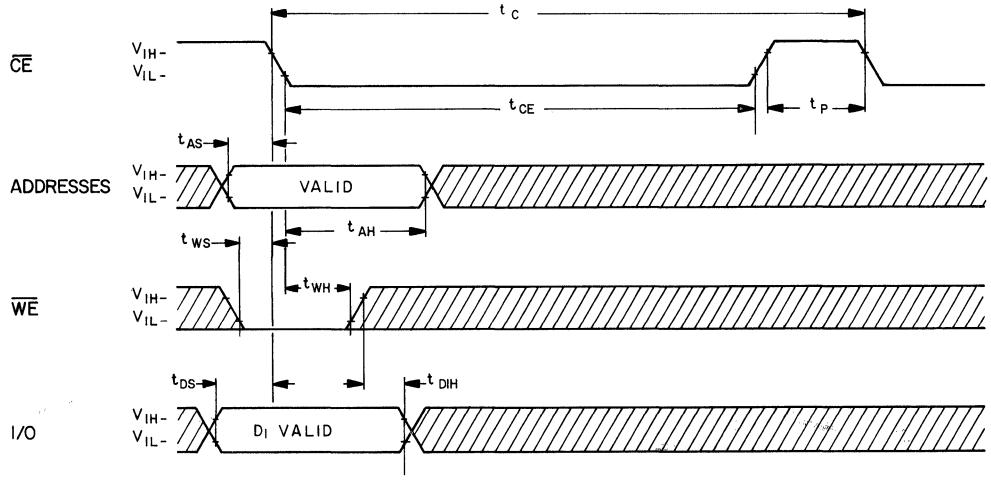
PARAMETER READ OR WRITE CYCLE		MK 4114-3		MK 4114-4		MK 4114-5		UNIT	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX		
t_C	Read or Write Cycle Time	310		385		460		ns	12
t_{AC}	Random Access		200		250		300	ns	7
t_{CE}	Chip Enable Pulse Width	200	10,000	250	10,000	300	10,000	ns	
t_P	Chip Enable Precharge Time	100		125		150		ns	
t_{AH}	Address Hold Time	110		135		165		ns	
t_{AS}	Address Set-Up Time	0		0		0		ns	
t_{OFF}	Output Buffer Turn-Off Delay	0	50	0	65	0	75	ns	13
t_{WS}	Write Enable Set-Up Time	0		0		0		ns	8
t_{DIH}	Data Input Hold Time	25		25		25		ns	
t_{WW}	Write Enabled Pulse Width	60		75		90		ns	
t_{MOD}	Modify Time	0	10,000	0	10,000	0	10,000	ns	9
t_{WPL}	$\overline{WE}$ to $\overline{CE}$ Precharge Lead Time	70		85		105		ns	
t_{DS}	Data Input Set-Up Time	0		0		0		ns	10
t_{WH}	Write Enable Hold Time	150		185		225		ns	
t_T	Transition Time	5	50	5	50	5	50	ns	

TIMING WAVEFORMS

READ CYCLE



WRITE CYCLE

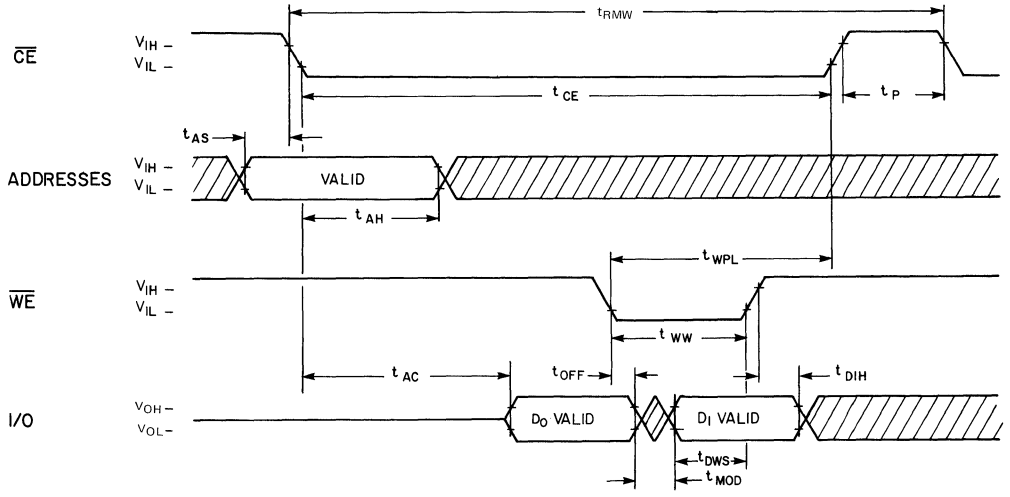


AC ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS [6, 11]

(0°C ≤ T_A ≤ +70°C) (V_{CC} = +5.0 volts ±10%)

PARAMETER READ-MODIFY-WRITE CYCLE		MK 4114-3		MK 4114-4		MK 4114-5		UNIT	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX		
t_{RMW}	Read-Modify-Write Cycle Time							ns	12
t_{AC}	Random Access		200		250		300	ns	7
t_{CE}	Chip Enable Pulse Width		10,000		10,000		10,000	ns	15
t_P	Chip Enable Precharge Time	100		125		150		ns	
t_{AH}	Address Hold Time	110		135		165		ns	
t_{AS}	Address Set-Up Time	0		0		0		ns	
t_{OFF}	Output Buffer Turn-Off Delay	0		0		0		ns	13
t_{DIH}	Data Input Hold Time	25		25		25		ns	
t_{WW}	Write Enabled Pulse Width							ns	
t_{MOD}	Modify Time	0	10,000	0	10,000	0	10,000	ns	9
t_{WPL}	$\overline{WE}$ to $\overline{CE}$ Precharge Lead Time							ns	10
t_{DWS}	Data Input Set-Up Time							ns	8
t_{WH}	Write Enable Hold Time							ns	
t_T	Transition Time	5	50	5	50	5	50	ns	

READ-MODIFY-WRITE CYCLE



OPERATION

READ CYCLE

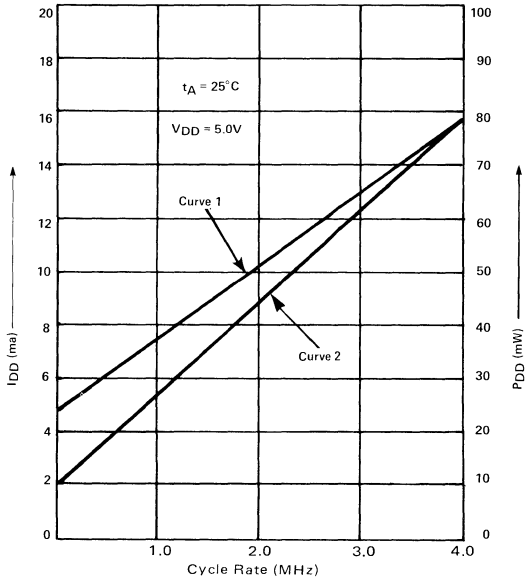
The circuit offers four bits of the possible 4096 by decoding the 10 address bits presented at the inputs. The address bits are strobed into the chip by the negative-going edge of the Chip Enable ($\overline{CE}$) clock. A read cycle is accomplished by holding the 'write enable' ($\overline{WE}$) input at a high level (V_{IH}) while clocking the $\overline{CE}$ input to a low level (V_{IL}). At access time (t_{AC}) valid data will appear at the output. The output is unlatched by a positive transition of $\overline{CE}$ and therefore will be open circuited (high impedance state) from the previous cycle to access time and will go open again at the end of the present cycle when $\overline{CE}$ goes high.

Once the address hold time has been satisfied, the addresses may be changed for the next cycle.

WRITE CYCLE

Data that is to be written into a selected cell is strobed into the chip on the latest occurring negative edge of $\overline{CE}$ or $\overline{WE}$. If the negative transition of $\overline{WE}$ occurs prior to the leading edge of $\overline{CE}$ as in an "early" write cycle then the $\overline{CE}$ input serves as the strobe for data-in. If $\overline{CE}$ leading edge occurs prior to the leading edge of $\overline{WE}$ as in a read-modify-write cycle then data-in is strobed by the $\overline{WE}$ input. If DI occurs after the later of $\overline{CE}$ or $\overline{WE}$, a ripple thru write mode will be accomplished. A minimum DI to $\overline{WE}$ positive going edge overlap is required. In either type of cycle data-in must remain valid for a minimum time period following the positive going edge of $\overline{WE}$. This time is specified by the parameter t_{DIH} (data input hold time).

OPERATING POWER VS CYCLE TIME



Characterization data plot of frequency vs power dissipation for a typical MK 4114 device.

Curve 1 – Clock on time (low level) is bottom scale minus 100 NSEC

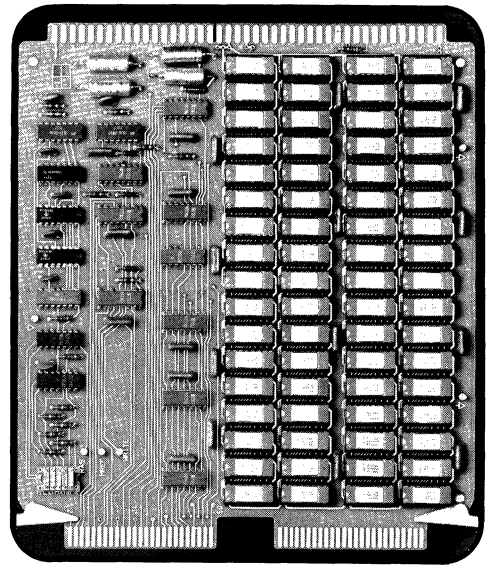
Curve 2 – Clock off time (high level) is bottom scale minus 200 NSEC

In an 'early' write cycle the output will remain in an open or high impedance state. In a read-modify write operation the output will go active (valid one/zero) at access time and remain active until $\overline{WE}$ goes active.

READ-MODIFY-WRITE CYCLE

The read-modify-write (RMW) cycle is no more than an extension of the read and write cycles. Data is read at access time, modified during a period determined by the user and the same or new data written between $\overline{WE}$ active (low) and the rising edge of $\overline{CE}$ (t_{WPL}) or $\overline{WE}$. In the R-M-W mode data-in normally will become valid after $\overline{WE}$ has been activated. In this mode a ripple thru type write will occur. A minimum data-in to $\overline{WE}$ positive going edge overlap is required.

APPLICATION INFORMATION



AN IN-DEPTH LOOK AT MOSTEK'S HIGH PERFORMANCE MK4027

INTRODUCTION

The MK 4027, like its predecessor the MK 4096, is a 4096 word by 1 bit N-Channel MOS Random Access Memory circuit that is packaged in a standard 16-pin DIP. This small package size is the result of a unique multiplexing and latching technique for the address inputs which MOSTEK pioneered for its 4K RAM family. This innovative approach to dynamic RAM design has proven to be one of the most important semiconductor memory milestones in the past few years. With more than a dozen manufacturers having announced their intentions to produce equivalent circuits with identical pin configurations, the MOSTEK 16-pin 4K RAM family has become an industry standard.

The purpose of this application note is to acquaint the user with the MK 4027, and to provide a more complete and in-depth understanding of the circuit (and its use) than can be obtained from the data sheet alone. MOSTEK realizes that most experienced memory system designers go through a process of evaluating many potential memory devices and making a judgement as to which device is best for a particular application. MOSTEK also realizes that this evaluation process can be a very tedious and time consuming endeavor, especially if several potential candidates are to be evaluated. Therefore, the information presented in this application note is divided into major sections and presented in the order that MOSTEK has found to be most desirable in the typical evaluation process used by most designers.

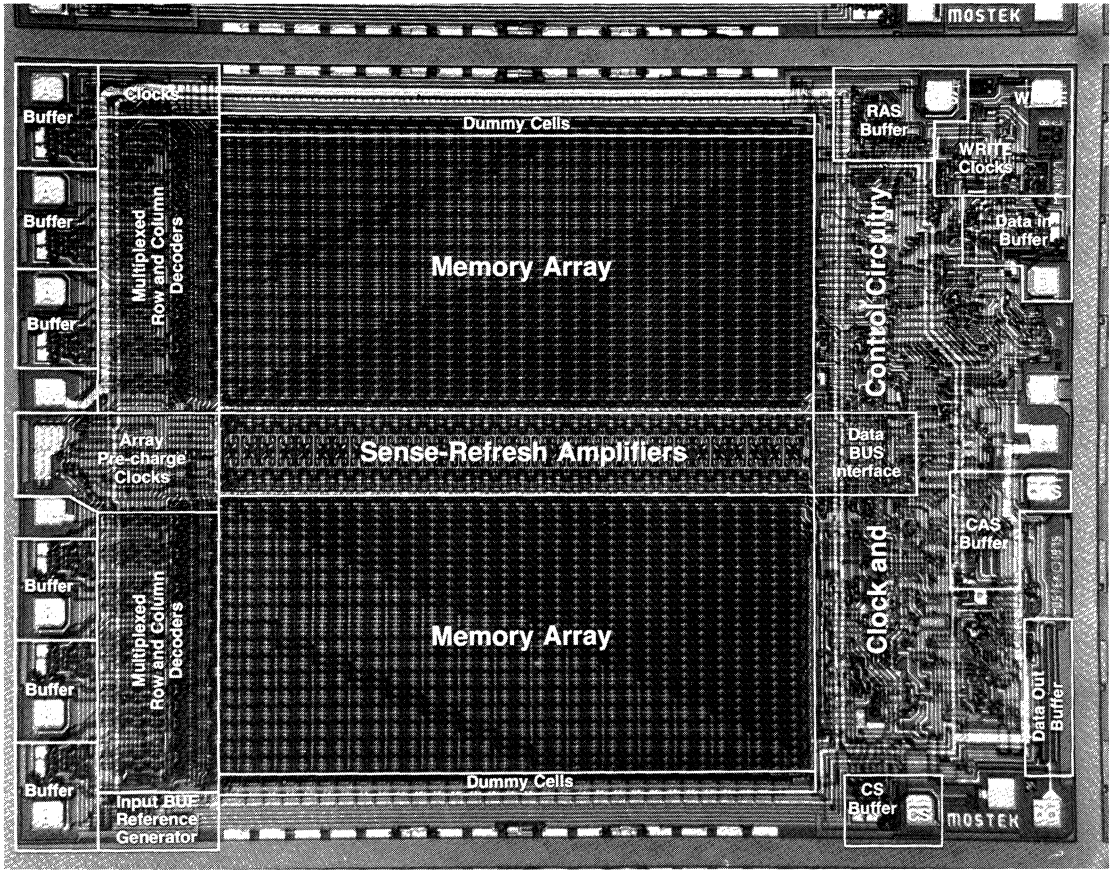


Figure 1

BACKGROUND

The pin configuration for the 16-pin 4K RAM was originated by MOSTEK Corporation when the MK 4096 was announced in 1973. Basically, the 16 pin device is made possible by eliminating six of the twelve address inputs required to select one out of 4096 bit locations in the RAM. Addressing is accomplished by the external generation of negative going Row and Column Address Strobe signals ($\overline{RAS}$ and $\overline{CAS}$) which latch incoming multiplexed addresses into the chip. This same addressing technique is carried over from the MK 4096 to the higher performance MK 4027.

PIN CONNECTIONS

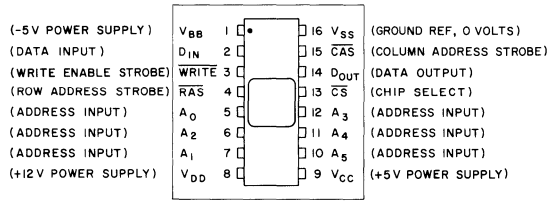


Figure 2

In addition to improved performance characteristics, the MK 4027 also incorporates several different and flexible operating modes and system-oriented features. These features include direct interfacing capability with TTL, low capacitance inputs and output, on-chip address and data registers, two methods of chip selection, simplified ($\overline{RAS}$-only) refresh operation, and flexible column address timing to compensate for system timing skews. Also, the MK 4027 offers a unique cycling operation called page-mode. Page-mode timing is very useful in systems requiring Direct Memory Access (DMA) operation.

Before delving into the more detailed aspects of the MK 4027, it is helpful to obtain a basic understanding of the internal circuit operation. Once a designer understands the fundamental operation of the MK 4027, it is much easier to see how and why the device operates with such improved performance over existing 4K dynamic RAM designs.

Much of the internal structure of the MK 4027 is made possible by state-of-the-art processing. The MK 4027 is fabricated with MOSTEK's ion-implanted N-Channel silicon gate (Poly I) process, whose basic steps are illustrated in figure 3. This process allows independent adjustment of gate and field oxide thresholds by ion-implantation (a technique introduced by MOSTEK in 1971), which maximizes performance, density, and reliability.

4027 PROCESS STEPS

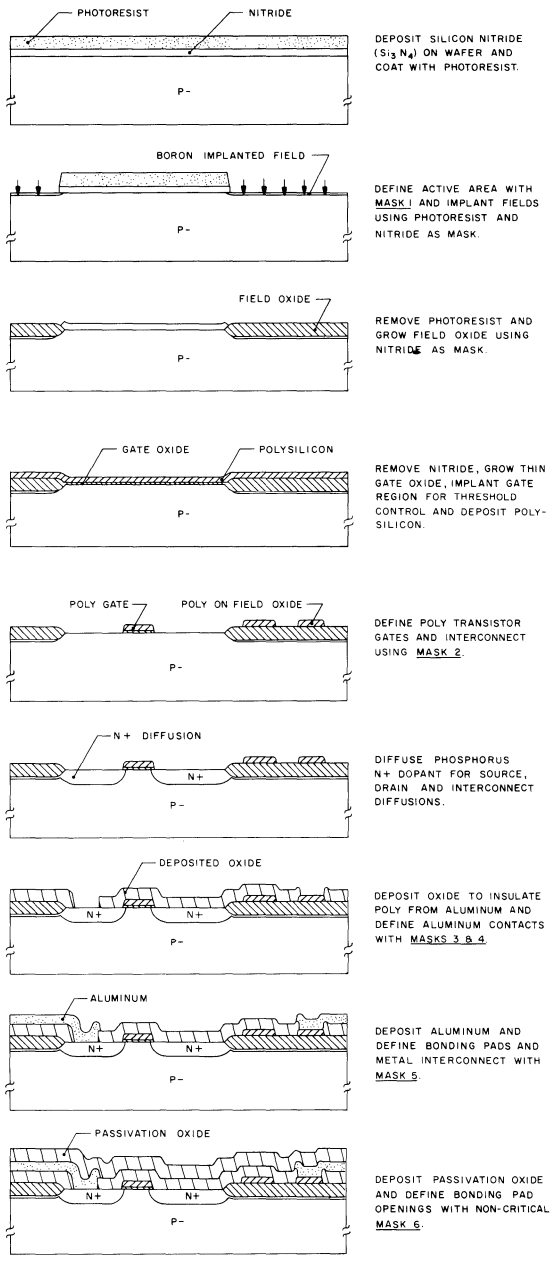


Figure 3

INTERNAL CIRCUIT OPERATION

The internal circuit operation of the MK 4027 is unlike any other 4K RAM in the industry. The MK 4027 utilizes a revolutionary new architecture for semiconductor memories. The circuit layout and design techniques incorporated within the MK 4027 are the main reasons for the increased performance capabilities and the additional system-oriented features. As an aid in understanding the operation of the MK 4027 refer to the block diagram in figure 4 .

A major difference between the MK 4027 and most conventional RAMs is that the MK 4027 has only one internal decoder and only one set of input buffers for both the Row and Column addresses. This feature greatly reduces the active silicon area and input capacitance. Note also that the internal single transistor storage cell matrix is divided into two sections with the sense amplifiers and input/output circuitry located between the two. This type of sense amp configuration causes data stored in half of the memory to be inverted from the data stored in the opposite half. However, this inversion is completely invisible at the device terminals. The sense amplifiers incorporated within the MK 4027 are dynamic, balanced, differential sense amps which dissipate no D C or steady-state power. Furthermore, virtually all of the circuitry used in the MK 4027 is a dynamic and consequently, most of the power dissipated by the MK 4027 is a function of operating frequency rather than active duty cycle.

MEMORY CYCLES

The MK 4027 will begin a memory cycle as soon as the Row Address Strobe ($\overline{RAS}$) input is activated. This is done by changing the voltage potential at the $\overline{RAS}$ input from a high level to a low level. The first internal action that takes place is the conversion of the TTL-compatible $\overline{RAS}$ signal to the MOS (12 volt) level that is required within the chip. The internal amplifier that performs this conversion is, of necessity, powered up at all times. Therefore, the $\overline{RAS}$ input buffer always dissipates some D C power. The steady-state power dissipated by the $\overline{RAS}$ input buffer is the main component of the overall standby power.

After the Row strobe reaches the proper level internally, a series of internal clock edges are generated to perform special control functions. The first of these clocks serves as a signal to "trap" the first set of six addresses into the address input buffers. These input buffers then generate the address into both true and complement form in high level, as required by the decoder. The addresses are then decoded for selection of the proper row in the memory cell matrix. Also, as the selected row is enabled, a set of dummy cells are enabled on the opposite side of the sense amplifier from the selected Row. These dummy cells serve to establish the proper trip point or reference voltage as required by the sense amps to differentiate between a one level and a zero level when the selected cell is read. As the selected Row and dummy cells are enabled, the address input buffers are already being reset and precharged so that the column addresses can be multiplexed into the chip.

MK 4027 FUNCTIONAL BLOCK DIAGRAM

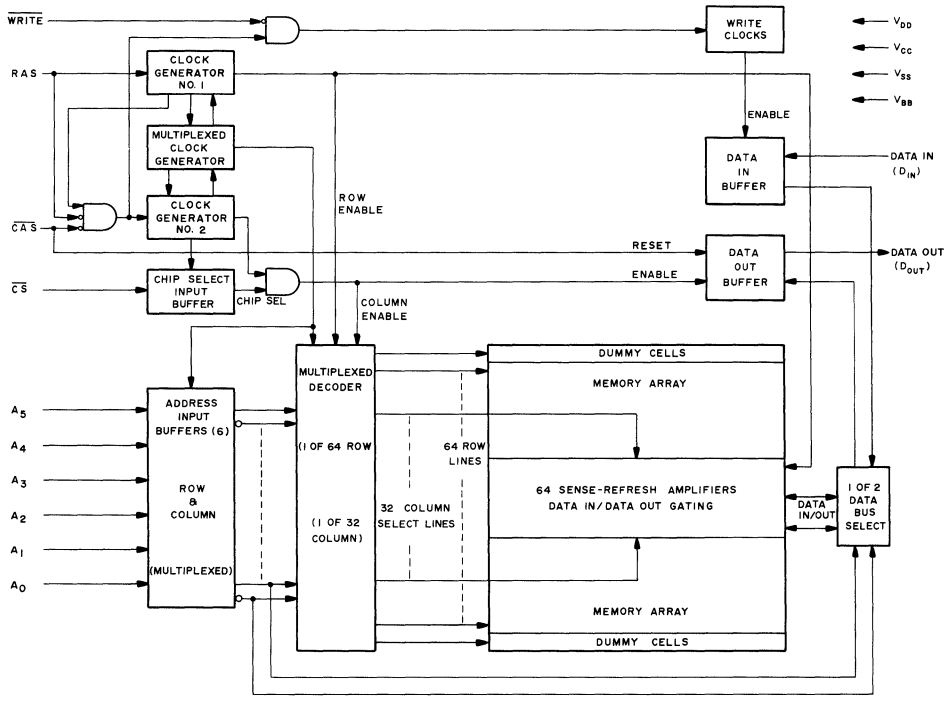


Figure 4

The last action initiated by the row clocks causes the data in all 64 cell locations in the selected Row to be latched into the sense amplifiers which , in turn, restore proper data back into the cells. (This action is known as refreshing.) The selected Row output from the decoder remains enabled as long as the Row Address Strobe ($\overline{RAS}$) is at a logic 0 level.

The second chain of events within the MK 4027 memory cycle, assuming that $\overline{RAS}$ is active, occurs when the Column Address Strobe ($\overline{CAS}$) is activated. As soon as the $\overline{CAS}$ is brought to logic 0 level, the output buffer is turned off and the output assumes the high impedance (open-circuit) state. If , at this time, the input circuitry is ready to process the column data, the low level $\overline{CAS}$ signal is converted to high level (12V) CAS. However, if the circuit is not yet ready to process column data, generation of the high level CAS signal is delayed. The internal mechanism for determining whether the MK 4027 is ready to process the column information is controlled by a signal from the row clock generator. This signal inhibits all column clocks until the sequence of row clocks has progressed to the appropriate time in the memory cycle. The internal "gating" of the RAS and CAS clocks has a very significant impact on external operation of the part. This is discussed in detail in a later section of this application note.

After CAS reaches the proper internal level, a series of clock edges are generated which operate in a similiar manner to the RAS clocks. In the case of CAS, however, the second rather than the first clock serves to "trap" the second set of six addresses into the address input buffers. These buffers again generate true and complement high level addresses as required by the decoder. Also, at this time the $\overline{WRITE}$ circuitry is enabled and the input/output data buses, which are routed through the center of the cell matrix, and the output buffer are all precharged to proper levels.

If the $\overline{WRITE}$ input is activated, a parallel series of clocks are enabled in addition to those enabled by the $\overline{CAS}$ circuitry alone. While the column addresses are trapped into the address input buffers and converted into true and complement high-level addresses, the $\overline{WRITE}$ input is converted to a high-level clock and data is latched into the data input buffer where it is also converted to true and complement, high-level information. It should be pointed out that the CAS circuitry also enables the Chip Select ($\overline{CS}$) input. The Chip Select input buffer is essentially the same type of circuit as an address input buffer, but, if the Chip Select input is not activated, the remaining series of CAS clocks are inhibited.

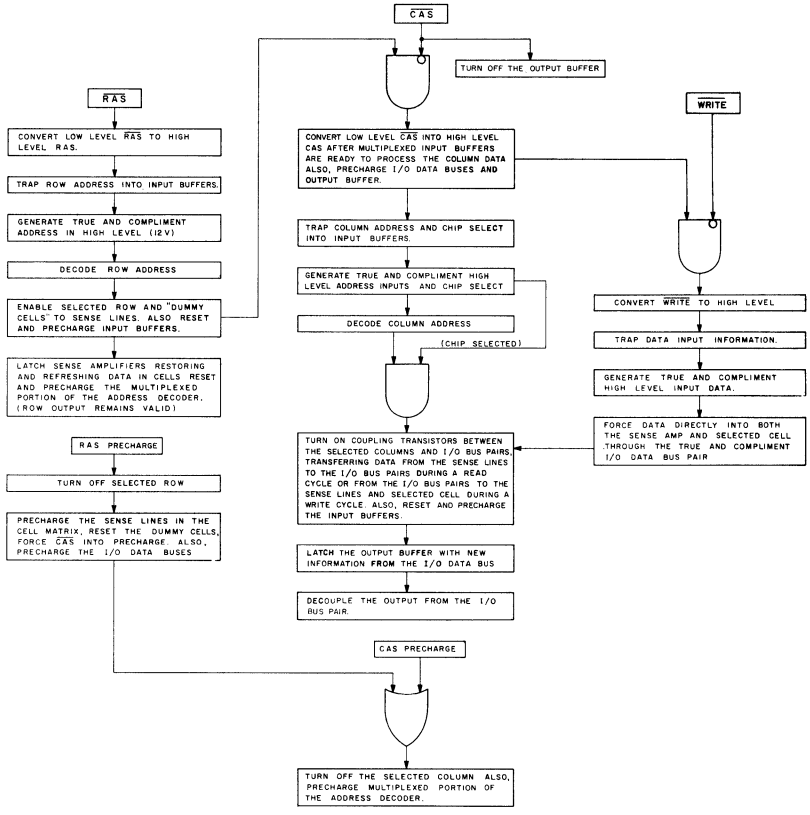
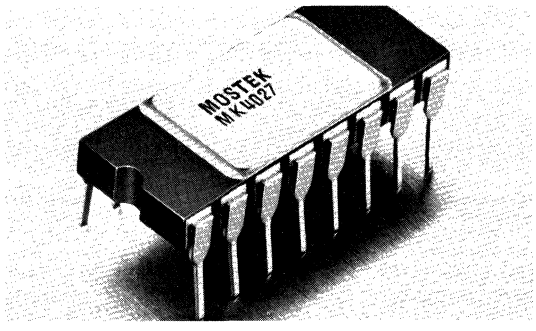


Figure 5

If, at this point in time, the chip has received a Row Address Strobe and a Column Address Strobe (with the Chip Select active), the chip will initiate either the Read or Write operation as indicated by the state of the $\overline{\text{WRITE}}$ input. The decoder selects the proper column by enabling the coupling transistors which connect the selected columns to the data input/data output differential bus pairs. During a read cycle, data is transferred from the selected sense lines to the I/O bus pairs. A write cycle will cause data to be transferred from the selected data I/O bus to the sense lines so that proper data is forced into the selected storage cell. After the correct data is present on the I/O bus, the data output buffer is latched and the correct information is presented at the output of the chip. Once the output buffer is latched, the output is decoupled from the internal I/O bus.

After the chip has performed all the functions required for a read, write or refresh operation, it remains in a quiescent state until the input control clocks ($\overline{\text{RAS}}$ and $\overline{\text{CAS}}$) are taken to the inactive (high) state. If $\overline{\text{RAS}}$ remains active and $\overline{\text{CAS}}$ is taken to the precharge (high) condition, the previously selected column will be turned off and the multiplexed portion of the address decoder will be reset and precharged, ready for a new $\overline{\text{CAS}}$ cycle. However, the previously selected row will remain enabled and the sense amps will retain the information read from that row. (This feature of the MK 4027 makes possible "page-mode" operation.) When $\overline{\text{RAS}}$ is terminated, the selected Row is turned off, the sense lines and the data I/O buses are precharged and the dummy cells are reset. Also, the input buffers and decoders are reset and precharged, ready for a new $\overline{\text{RAS}}$ cycle. Deactivating $\overline{\text{RAS}}$ also forces $\overline{\text{CAS}}$ into the precharge condition internally, even though $\overline{\text{CAS}}$ may remain active at the input.

The internal workings of the MK 4027 can be best summarized by referring to the Functional Flow Chart in figure 5. From this brief outline of the internal operation of the device it is easy to see how the MK 4027 is capable of so many different and flexible timing modes. Besides the usual read, write, and read-modify-write cycles, the MK 4027 is also capable of "page-mode" cycles (very useful in Direct Memory Access operation) and "delayed-write" cycles (very useful in shift register applications.) While keeping in mind the internal structure of the MK 4027 it is now appropriate to delve into a more detailed discussion of the external characteristics and system implications of the MK 4027 memory device.



EXTERNAL DEVICE CHARACTERISTICS

ADDRESSING

As stated earlier, the 12 address bits required to decode one of the 4096 cell locations within the MK 4027 are multiplexed onto the 6 address inputs and latched into the on-chip address latches by externally applying two negative-going, TTL-level clocks. The first clock, the Row Address Strobe ($\overline{\text{RAS}}$), latches the 6 row address bits into the chip. The second clock, the Column Address Strobe ($\overline{\text{CAS}}$), subsequently latches the 6 column address bits plus Chip Select ($\overline{\text{CS}}$) into the chip. Each of these clock signals, $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$, triggers off a sequence of events which are controlled by different delayed internal clocks. The two clock chains are linked together logically in such a way that the address multiplexing operation is done outside of the critical path timing sequence for read data access. The later events in the $\overline{\text{CAS}}$ clock sequence are inhibited until the occurence of a delayed signal derived from the $\overline{\text{RAS}}$ clock chain. This "gated $\overline{\text{CAS}}$" features allows the $\overline{\text{CAS}}$ clock to be externally activated as soon as the Row Address Hold Time specification (t_{RAH}) has been satisfied and the 6 address inputs have been changed from Row address to Column address information. This results in a system limit of $t_{RCD} = t_{RAH} + t_T + t_{ASC}$ (t_T = one transition time).

Note that $\overline{\text{CAS}}$ can be activated at any time after t_{RAH} and it will have no affect on the worst case data access time (t_{RAC}) up to the point in time when the delayed row clock no longer inhibits the remaining sequence of column clocks. Two timing end points result from the internal gating of $\overline{\text{CAS}}$ which are called t_{RCD} (min) and t_{RCD} (max). No data storage or reading errors will result if $\overline{\text{CAS}}$ is applied to MK 4027 at a point in time beyond the t_{RCD} (max) limit. However, access time will then be determined exclusively by the access time for $\overline{\text{CAS}}$ (t_{CAC}) rather than from $\overline{\text{RAS}}$ (t_{RAC}), and access time from $\overline{\text{RAS}}$ will be lengthened by the amount that t_{RCD} exceeds the t_{RCD} (max) limit.

The significance of this "gated $\overline{\text{CAS}}$" feature is that it allows a multiplexed circuit, such as the MK 4027, to be comparable in performance (access time) with non-multiplexed devices such as the 18- and 22-pin 4K RAMs. In essence, it allows the designer to compensate for system timing skews that may be encountered in the multiplexing operation when addressing the device. In the MK 4027, the "window" available for multiplexing from row address to column address information while still achieving minimum access time (t_{RAC}) is a full 25% of access time.

MEMORY CYCLES

Once the MK 4027 is properly addressed, the device is capable of performing various types of memory cycles. Selection of the various cycles, whether read, write or some combination thereof, is controlled by a combination of $\overline{\text{CAS}}$ and $\overline{\text{WRITE}}$, while $\overline{\text{RAS}}$ is active. Also, since Chip Select ($\overline{\text{CS}}$) does not have to be valid until $\overline{\text{CAS}}$, which is well into the memory cycle, it is possible to start a cycle before it is known which is the selected device.

Data is retrieved from the memory in a read-only cycle by maintaining $\overline{WRITE}$ in the inactive or high state throughout the portion of the memory cycle in which $\overline{CAS}$ is active. Data read from the selected cell will be available at the output within the specified access time.

Data to be written into a selected cell is latched into an on-chip register by a combination of $\overline{WRITE}$ and $\overline{CAS}$ while $\overline{RAS}$ is active. The later of these signals ($\overline{WRITE}$ or $\overline{CAS}$) to make its negative transition is the strobe for the Data-In register. This permits several options in the write cycle timing. In a write cycle, if the $\overline{WRITE}$ input is brought low prior to $\overline{CAS}$, the Data In is strobed in by $\overline{CAS}$, and the set-up and hold times are referenced to $\overline{CAS}$. If the data input is not available at $\overline{CAS}$ time or if it is desired that the cycle be a read-write cycle, the $\overline{WRITE}$ signal will be delayed until after $\overline{CAS}$ goes low. In this "delayed write cycle" the data input set-up and hold times are referenced to the negative edge of $\overline{WRITE}$ rather than to $\overline{CAS}$. Note that delaying $\overline{WRITE}$ until after the negative edge of $\overline{CAS}$ is termed a "read-write cycle" rather than read-modify-write. In a read-write cycle, it is not necessary to wait until data is valid at the output before the write operation is started. This feature is very useful when the MK 4027 is used in sequential memory applications or in systems that employ "interleaving techniques." However, if a true read-modify-write cycle is required (where the write operation occurs after read access), then $\overline{WRITE}$ can occur while $\overline{RAS}$ and $\overline{CAS}$ are still active and after t_{CAC}.

To take full advantage of this $\overline{CAS}/\overline{WRITE}$ signal relationship it is necessary for one to understand how the Data Out Latch is controlled. The most important fact to remember is that any change in the condition of the Data Out Latch is initiated by the $\overline{CAS}$ negative edge. The output buffer is not affected by memory cycles in which only the $\overline{RAS}$ signal is applied to the MK 4027. Whenever $\overline{CAS}$ makes a negative transition, the output will go unconditionally open-circuited, independent of the state of any other input to the chip. If the cycle in progress is a read, read-modify-write, or a delayed write cycle and the chip is selected, then the output latch and buffer will again go active, and at access time will contain the data read from the selected cell. This output data is the same polarity (not inverted) as the input data. If the cycle in progress is a write cycle ($\overline{WRITE}$ active low before $\overline{CAS}$ goes low) and the chip is selected, then at access time the output latch and buffer will contain the input data. Once having gone active, the output will remain valid until the MK 4027 receives the next $\overline{CAS}$ negative edge. Intervening refresh cycles in which $\overline{RAS}$ is received, but no $\overline{CAS}$, will not cause valid data to be affected. Conversely, the output will assume the open-circuited state during any cycle in which the MK 4027 receives a $\overline{CAS}$ but no $\overline{RAS}$ signal (regardless of the state of any other inputs). The output will also assume the open-circuit state in normal cycles if the chip is unselected. Note that if the chip is unselected ($\overline{CS}$ high at $\overline{CAS}$ time) $\overline{WRITE}$ commands are not executed and, consequently, data stored in the memory is unaffected.

The three-state data output buffer presents the data output pin with a low impedance to V_{CC} for a logic 1 and a low impedance to V_{SS} (Ground) for a logic 0. The effective resistance to V_{CC} (logic "1" state) is 420Ω maximum and $<$ 100 Ω typically. The resistance to V_{SS} (logic "0" state) is 125Ω maximum and $<$ 50Ω typically. The separate V_{CC} pin allows the output buffer to be powered from the positive supply voltage of the logic to which the chip is interfaced. During battery standby operation, the V_{CC} pin may have power removed without affecting the MK 4027 refresh operation. This allows all system logic except the $\overline{RAS}$ timing circuitry and the refresh address logic to be turned off during battery standby to conserve power.

Specified on the MK 4027 data sheet are two electrical characteristics of the device which guarantee the appropriate state of the data output during a write cycle. These two specifications, $\overline{RAS}$ to $\overline{WRITE}$ delay (t_{RWD}) and $\overline{CAS}$ to $\overline{WRITE}$ delay (t_{CWD}) are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. The values listed in the "minimum" and "maximum" columns should be inserted as terms in the following equations:

1. If $t_{CWD} + t_T \leqslant t_{CWD}$ (min), the data out latch will contain the data written into the selected cell.
2. If $t_{CWD} \geqslant t_{CWD}$ (max) + t_T and $t_{RWD} \geqslant t_{RWD}$ (max) + t_T, the data out latch will contain the data read from the selected cell.
3. If t_{CWD} does not meet the above constraints then the data out latch will contain indeterminate data at access time.

The following diagrams are representations of the MK 4027 timing waveforms for read, write and delayed-write or read-modify-write cycles. A list of the timing parameters associated with each cycle is also included.

These parameters apply to all MK 4027 memory cycles:

SYMBOL	DEFINITION
t_{RFSH}	Maximum time that the device will retain stored data without being refreshed.
t_{RP}	$\overline{RAS}$ precharge, or $\overline{RAS}$ inactive time of a cycle.
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ lead time. Operation within the t_{RCD} (max) limit insures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
t_{ASR}	Row address set-up time.
t_{RAH}	Row address hold time.
t_{ASC}	Column address set-up time.
t_{CAH}	Column address hold time.
t_{AR}	Column address hold time referenced to $\overline{RAS}$.
t_{CSC}	Chip select set-up time.
t_{CH}	Chip select hold time.
t_{CHR}	Chip select hold time referenced to $\overline{RAS}$.
t_{CRP}	$\overline{CAS}$ inactive to $\overline{RAS}$ active precharge time.
t_{OFF}	Output buffer turn-off delay.
t_{RAS}	$\overline{RAS}$ pulse width or active time.
t_{CAS}	$\overline{CAS}$ pulse width or active time.
t_{RAC}	Access time from $\overline{RAS}$ falling edge.
t_{CAC}	Access time from $\overline{CAS}$ falling edge.
t_T	Transition time (rise and fall). Transition times are measured between V_{IHC} or V_{IH} and V_{IL}. V_{IHC} (min) or V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals.

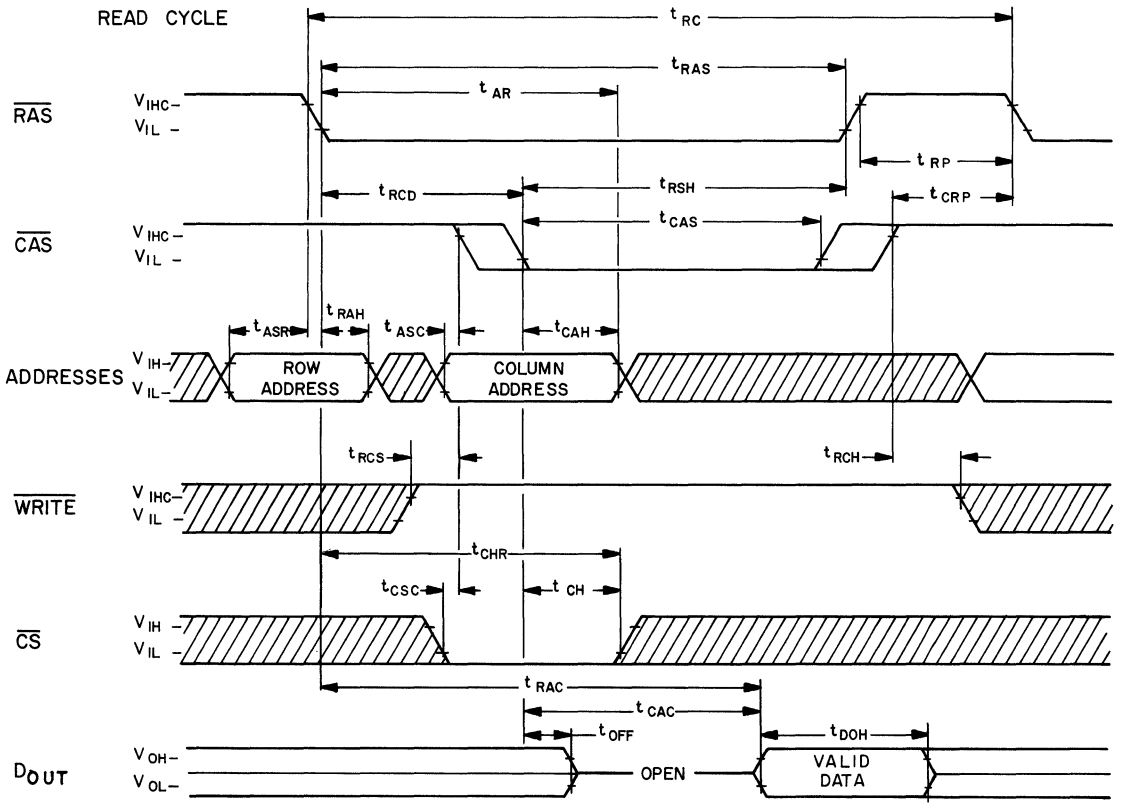


Figure 6

READ CYCLE ONLY

t_{RC}	Random read or write cycle time. t_{RC} (min) $\geq t_T + t_{RAS} + t_T + t_{RP}$.
t_{RCS}	Read command set-up time.
t_{RCH}	Read command hold time.
t_{ACC}*	Device access time, t_{ACC}, is the longer of two calculated intervals: 1. $t_{ACC} = t_{RAC}$, or 2. $t_{ACC} = t_{RCD} + t_T + t_{CAC}$ * This parameter is not shown in the timing waveforms.

WRITE CYCLE

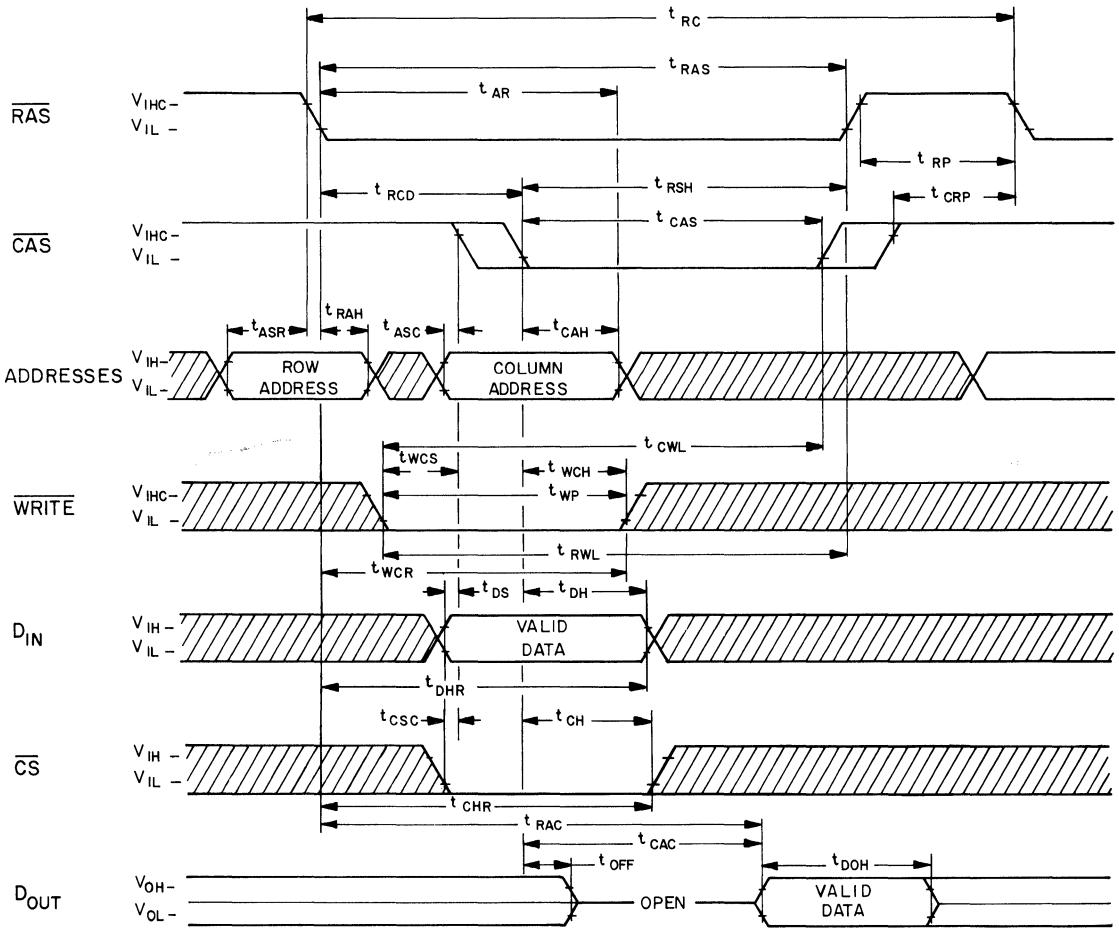


Figure 7

WRITE CYCLE ONLY

tRC	Random read or write cycle time. t_{RC} (min) $\geq t_T + t_{RAS} + t_T + t_{RP}$.
tWCH	Write command hold time referenced to $\overline{CAS}$.
tWCR	Write command hold time referenced to $\overline{RAS}$.
tWP	Write command pulse width.
tRWL	Write command to $\overline{RAS}$ lead time.
tCWL	Write command to $\overline{CAS}$ lead time.
tDS	Data In set-up time (referenced to $\overline{CAS}$).
tDH	Data In hold time (referenced to $\overline{CAS}$)
tDHR	Data In hold time (referenced to $\overline{RAS}$)

READ - WRITE / READ - MODIFY - WRITE CYCLE

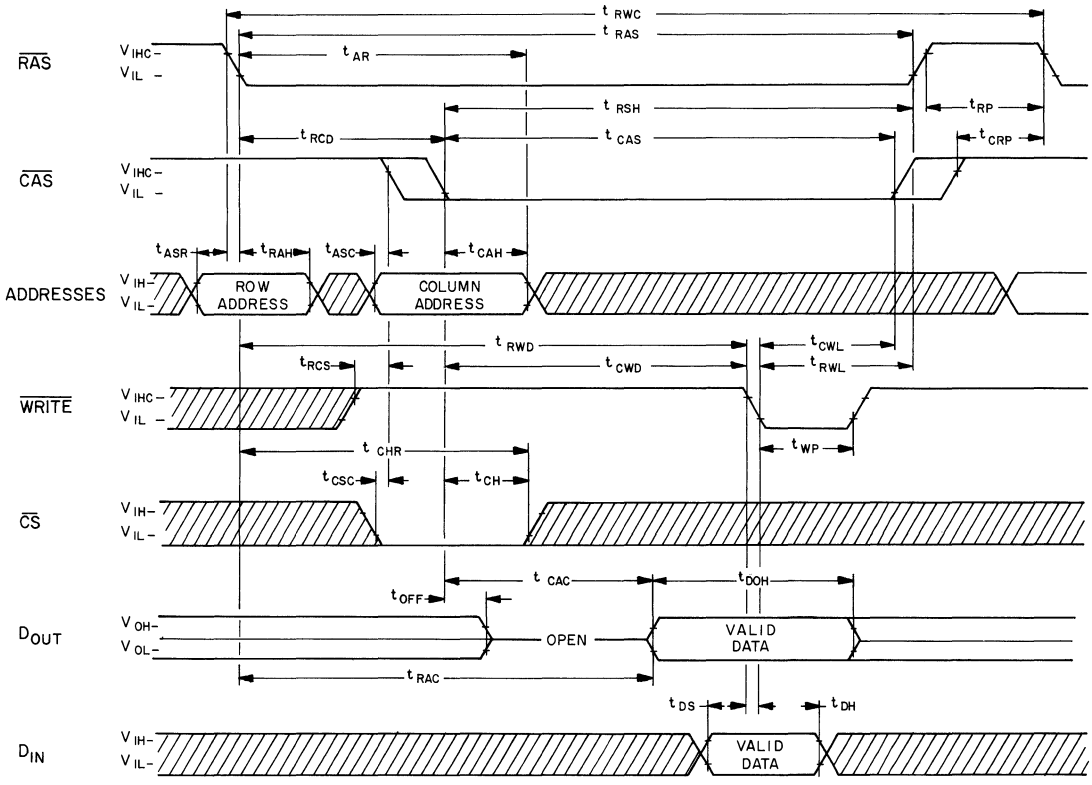


Figure 8

READ/WRITE CYCLE

t_{RWC}	Read-write or "delayed write" cycle time. t_{RWC} (min) $\geq t_T + t_{RCD} + t_T + T_{CWD} + t_{RWL} + t_T + t_{RP}$. This is the minimum time to insure that both a read and write operation will occur at the same address in a single memory cycle.
t_{RCS}	Read command set-up time.
t_{WP}	Write command pulse width.
t_{RWD}	$\overline{RAS}$ to $\overline{WRITE}$ delay.
t_{CWD}	$\overline{CAS}$ to $\overline{WRITE}$ delay.
t_{RWL}	Write command to $\overline{RAS}$ lead time.
t_{CWL}	Write command to $\overline{CAS}$ lead time.
t_{DS}	Data In set-up time (referenced to $\overline{WRITE}$).
t_{DH}	Data In hold time (referenced to $\overline{WRITE}$).

PAGE MODE

Keeping in mind the above mentioned cycle operations, it is now appropriate to introduce another category of memory cycles. The "page-mode" operation allows for successive memory operations at multiple column locations at the same row address with increased speed and with decreased power. This is done by strobing the row address into the chip and keeping the $\overline{RAS}$ signal active (at a logic 0) throughout all successive memory cycles in which the row address is common. This "page-mode" operation will not dissipate the power associated with the negative going edge of $\overline{RAS}$. Also, the time required for strobing in a new row address is eliminated, thereby decreasing the access and cycle times. Every type of cycle-read, write, read-modify-write and delayed-write cycles-can all be performed in the page mode. Also, the chip select ($\overline{CS}$) is operative in page mode just as in normal cycles. It is not necessary that the chip be selected during the first cycle for subsequent cycles to be selected properly in a page operation. Likewise, the $\overline{CS}$ input can be used to select or disable any cycle (s) in a series of "page" cycles. This feature allows the page boundary to be extended beyond the 64 column locations in a single chip. The page boundary can be extended by applying $\overline{RAS}$ to multiple 4K memory blocks and decoding $\overline{CS}$ to select the proper block.

The addition of page mode to the MK 4027's repertoire of features adds only two additional constraints to the timing parameters mentioned earlier. The first constraint is that the length of time that a single chip can remain in the page mode is limited to the maximum $\overline{RAS}$ pulse width (t_{RAS}) as specified on the data sheet. Second, the $\overline{CAS}$ precharge time (t_{CP}), or the time from the positive edge of $\overline{CAS}$ in one page cycle to the negative edge of $\overline{CAS}$ in subsequent page cycles must be obeyed.

The following timing waveforms illustrate the page mode operation. Note that the page-mode write cycle depicts the Data In set-up and hold times referenced to $\overline{WRITE}$ rather than $\overline{CAS}$. Once again, this is to illustrate the flexibility of the write cycle operation. Page-mode operation is particularly useful in transferring large blocks of data into or out of memory.

PAGE MODE READ CYCLE

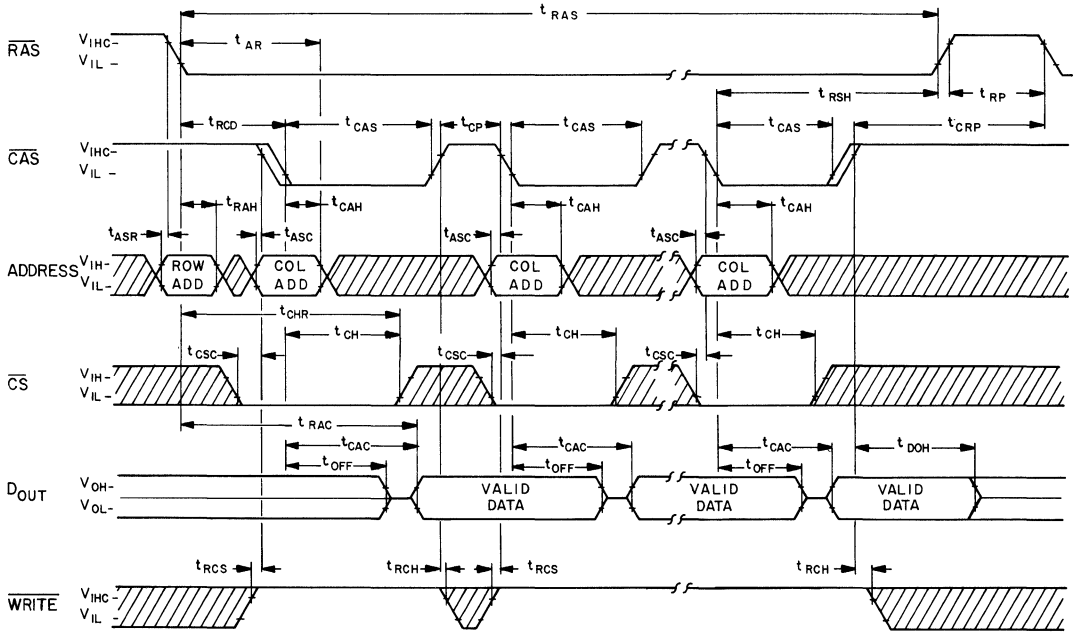


Figure 9

PAGE MODE WRITE CYCLE

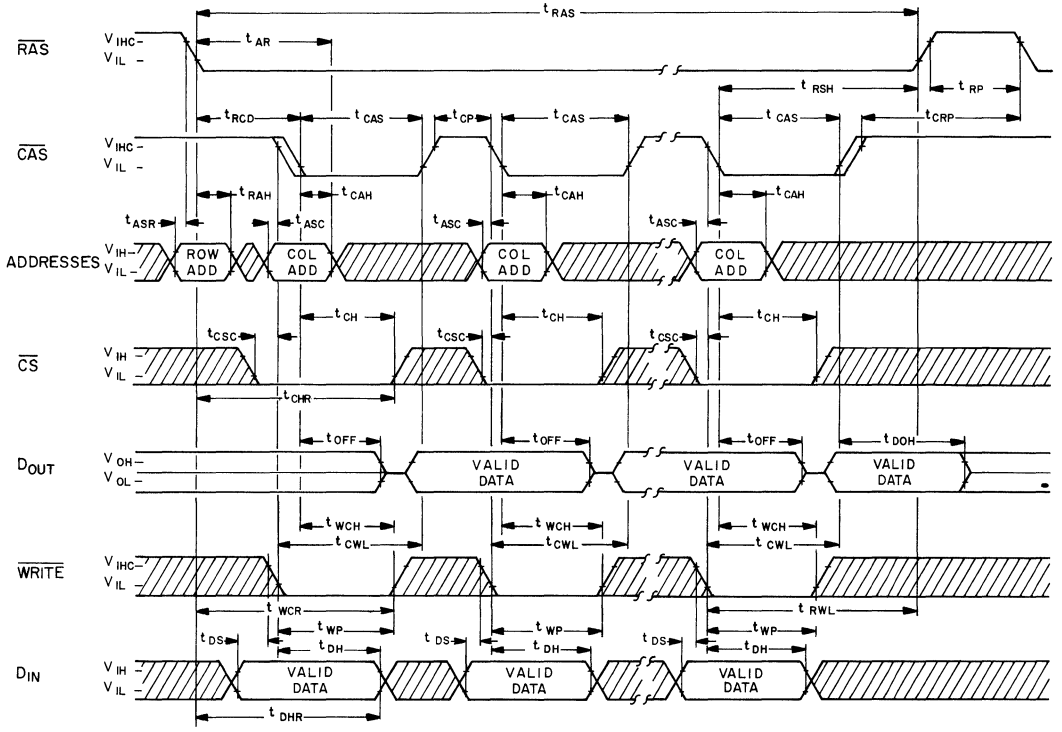


Figure 10

REFRESH

Refresh of the dynamic cell matrix is accomplished by performing a memory cycle at each of the 64 row addresses within each 2 millisecond time interval. Any cycle in which a $\overline{RAS}$ signal occurs, accomplishes a refresh operation. A read cycle will refresh the selected row, regardless of the state of the Chip Select ($\overline{CS}$) input. A write or read-modify-write cycle also refreshes the selected row, but the chip should be unselected to prevent writing data into the selected cell. If during a refresh cycle, the MK 4027 receives a $\overline{RAS}$ signal but no $\overline{CAS}$ signal, the state of the output will not be affected. Therefore, data from the previous cycle will remain valid throughout the refresh cycle. However, if "$\overline{RAS}$-only" refresh cycles (where $\overline{RAS}$ is the only signal applied to the chip) are continued for extended periods, the output buffer may eventually lose proper data and go open-circuit. The output buffer will regain activity with the first cycle in which $\overline{CAS}$ is applied to the chip.

The following diagram illustrates the "$\overline{RAS}$-only" refresh cycle:

"$\overline{RAS}$ ONLY" REFRESH CYCLE

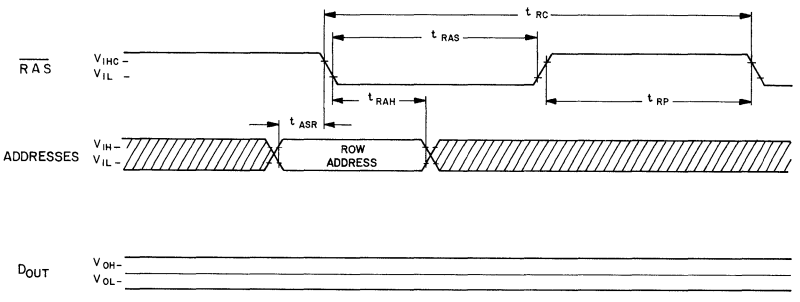


Figure 11

POWER DISSIPATION

The worst case power dissipation of the MK 4027, continuously operating at the fastest cycle rate, is the sum of [V_{DD} (max) X I_{DD} (max) plus V_{BB} (max) X I_{BB} (max)], where maximum currents are the maximum currents averaged over one memory cycle. The worst case power for the MK 4027 with a cycle rate of 375 nanoseconds is less than 470mW, while the typical power is 170 mW at a 1 μs cycle time.

Typical power supply current waveforms for various types of memory cycles are shown in figure 12. From this picture it is easy to see that most of the power drawn by the MK 4027 is the result of an address strobe charging the capacitances of various internal circuit nodes.

Note also that there is very small DC component in the current waveforms, independent of how long the address strobes remain active. This is because most of the circuitry in the MK 4027 is dynamic, with the exception of the $\overline{RAS}$ input buffer.

The first portion of the current waveforms illustrates a normal $\overline{RAS}/\overline{CAS}$ memory cycle. As expected, the I_{DD} waveform has three major current peaks above ground level. These occur when $\overline{RAS}$ goes active, then when $\overline{CAS}$ internally goes active, and finally when both $\overline{RAS}$ and $\overline{CAS}$ go back into precharge. On the other hand, both positive and negative current transients are associated with I_{BB}. This results in peak currents that can be two to four orders of magnitude higher than the average D C value.

The second cycle is representative of a page-mode cycle in which $\overline{CAS}$ is completely enveloped by $\overline{RAS}$. Note that delaying $\overline{CAS}$ until well after $\overline{RAS}$ goes negative demonstrates the relative contributions of $\overline{RAS}$ and $\overline{CAS}$ to total power. This type of cycle operation has the effect of reducing the peak current associated with $\overline{RAS}$ and $\overline{CAS}$ going into precharge simultaneously. Instead, two smaller current spikes are generated, each coinciding with the separate termination of $\overline{CAS}$ and $\overline{RAS}$. From the current waveform it is clear that approximately 60% of all active power is due to $\overline{RAS}$ and only about 40% of all active power is due to $\overline{CAS}$. Thus, even with increased frequency, the maximum power dissipated in a page-mode operation is less than that in a normal cycle.

The third cycle is a "$\overline{RAS}$-only" cycle which can be used for the refresh operation. Note that the MK 4027 will dissipate considerably less power when the refresh operation is accomplished with a "$\overline{RAS}$-only" cycle as opposed to a normal $\overline{RAS}/\overline{CAS}$ cycle.

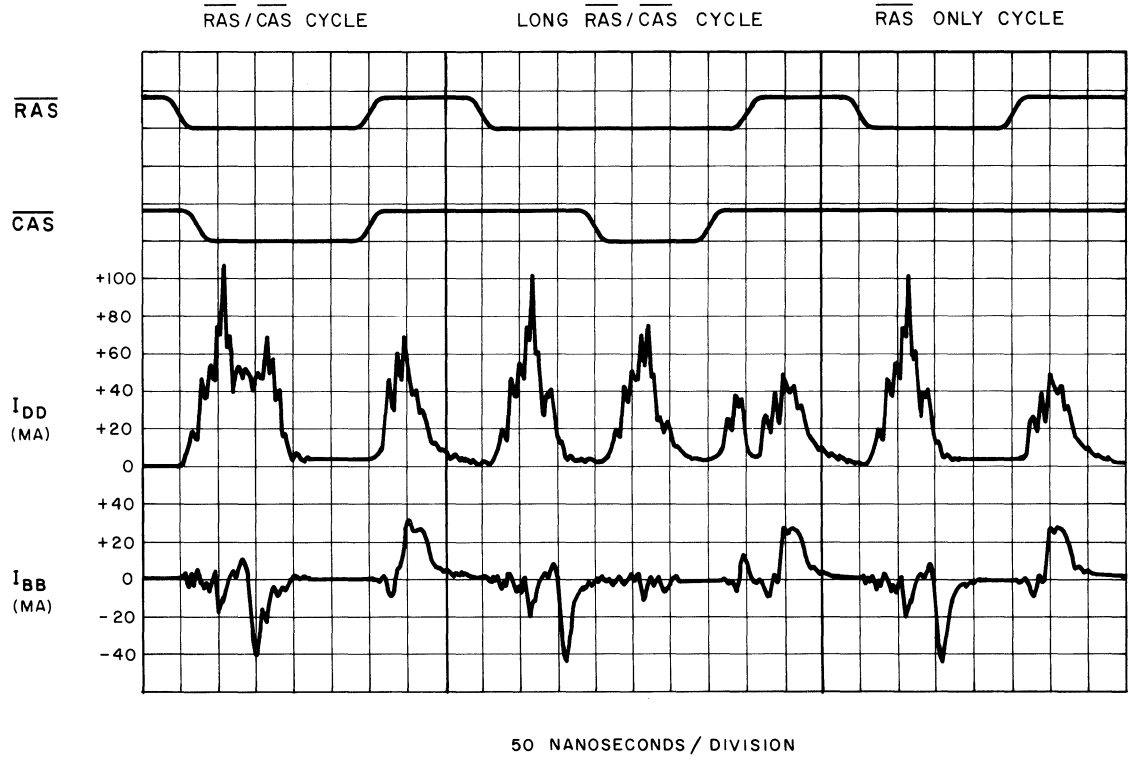


Figure 12

TESTING THE MK 4027 MEMORY DEVICE

Production testing of each MK 4027 memory device begins early in the process of every MK 4027 wafer. Once a wafer is processed, each individual die on that wafer is subjected to probe testing. This is where each die is probed and tested for functionality, leakage and continuity. All die that pass this test are then packaged and subjected to further Quality Assurance Processing.

The next barrage of tests include the following:

100% Pre-burn testing at high temperature (for function, leakage, and continuity)

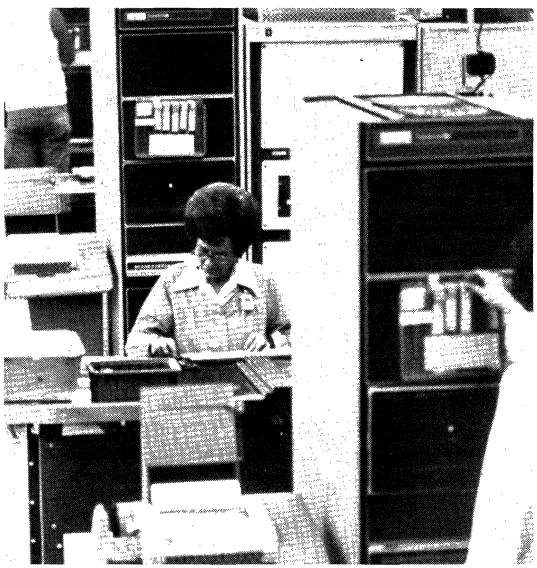
100% Temperature Cycling-screened to 10 cycles, −65°C to +150°C

100% Centrifuge - screened to insure positive die and bond attachment

100% Dynamic Burn-In - each device is operated at conditions well beyond data sheet limits for many hours to insure that only quality devices reach the end user.

All MK 4027 devices that pass the previous tests are then final tested for customer use. At final test, all devices are tested at high temperature, to all data sheet AC and DC specifications with wide guardbands. This type of Quality Assurance Processing and Testing insures that not only does every MK 4027 perform well within the established data sheet limits, but also exhibits the quality and reliability standards necessary for today's (and tomorrow's) data processing applications.

Thorough testing of every MK 4027 is performed on what MOSTEK calls "MASTER TESTERS." These machines incorporate a very versatile pattern generator made by Computest and a very sophisticated parametric measurement unit (PMU) and clock section that was conceived and constructed by MOSTEK Test Equipment design engineers. This combination of purchased and custom designed hardware is controlled by a PDP-11 minicomputer. These MASTER TESTERS are used not only in production testing but also in the engineering characterization of the MK 4027. This permits excellent correlation between characterization and production testing on the device. The test equipment is also used as an analysis tool in the "continuing engineering" phase of MK 4027 production.



MOSTEK's 4K testing area.

Establishing one's own incoming inspection and testing procedures for a device as complicated as a 4K dynamic RAM is one of the most important and critical procedures in any production program. Usually the effectiveness of the screening procedure may not be known until several assembled systems have been field tested for several months. Therefore, it is important that proper screening procedures are employed early in any production program.

Many times, in establishing electrical end-point tests, it is necessary to know the proper external addressing sequence to insure sequential addressing within a memory device. The internal address bit map of the MK 4027 is arranged in a somewhat unusual fashion to keep the chip size to a minimum. Therefore, sequentially addressing the MK 4027 cannot be done with a straight binary count without the circuitry shown below. Note that this is for testing purposes only and is certainly not required or recommended for system use.

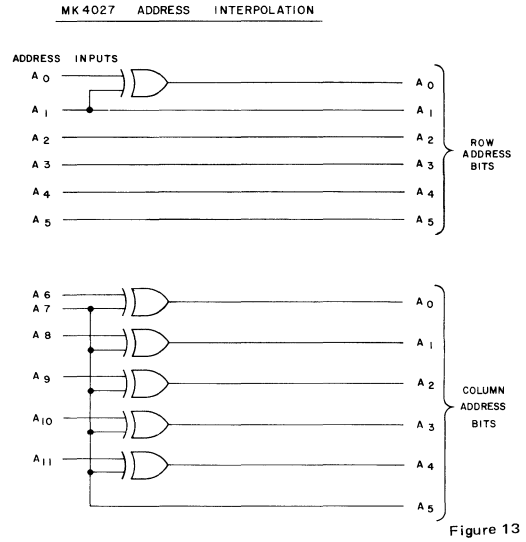


Figure 13

Also, since the sense amplifiers within the MK4027 are located in the center of the memory matrix, data stored in half of the memory will be inverted from the data presented at the input pin. Once again, this inversion is completely transparent to the user (i.e., data stored in the memory as a "1" or "0" at the input will, when subsequently accessed, appear as a "1" or "0" respectively at the output). However, if one wishes to determine the polarity of data stored in the memory, refer to the following chart.

ROW ADDRESS A_5	DATA STORED
0	inverted data
1	true data

MK4096 APPLICATION INFORMATION

INTRODUCTION

Designing a memory system involves interfacing the memory component (MK 4096) to a memory controller to form a memory system. The memory controller must interface the memory system to a processor or peripheral that may require access to the memory. For the controller to be the "go-between" for the processor and the memory, the designer must have a full knowledge of the MK 4096 and the interface requirements of the processor.

This application note is intended to extend the MK 4096 data sheet and show the details of the MK 4096 characteristics that are necessary for system design. Also, a memory controller design is included to show a technique that can be used to interface the MK 4096 to the PDP-11* processor.

FUNCTIONAL DESCRIPTION

The MOSTEK MK 4096 is a 4096x 1 bit dynamic MOS Random Access Memory (RAM). The MK 4096 is fully TTL compatible on all inputs, including strobes and the output. Multiplex addressing techniques are used to allow the chip to function in a standard 16 pin DIP. The RAM is dynamic and the data stored must be refreshed every 2 mS.

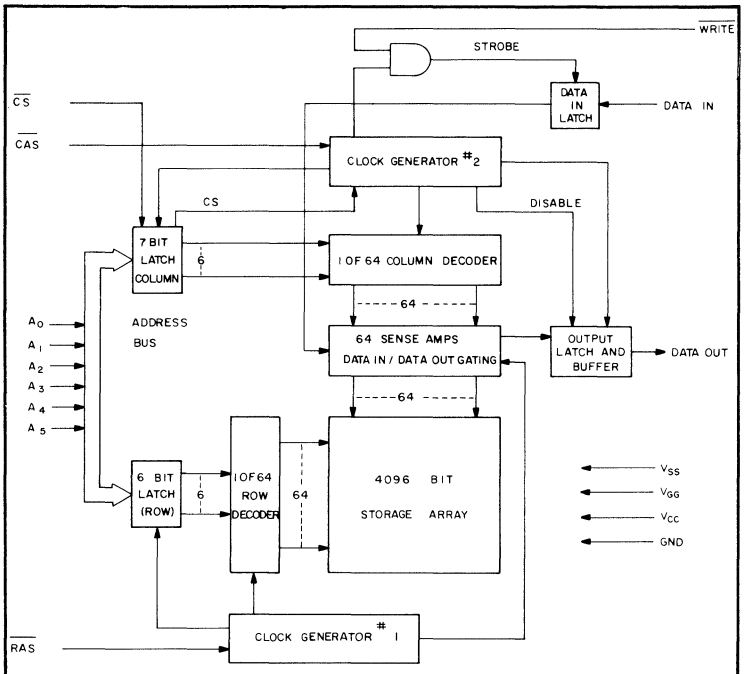


Fig. 1 MK 4096 Functional Block Diagram

Figures 1 and 2 show the functional block diagram and timing diagrams for the MK 4096. The memory is organized as a 64 x 64 bit matrix with a sense amp at the top of each column. A memory cycle is begun by supplying the row address to the six address inputs and bringing the Row Address Strobe (RAS) low. This starts operation of clock generator No. 1.

The first function the chip performs regardless of whether the cycle will be a read cycle, write cycle, or refresh cycle, is to latch and decode the 6 row address bits. One of the 64 rows will be selected. Next, the contents of all 64 cells in the selected row will be sensed by the sense amps at the top of the column and the data held for use later in the cycle.

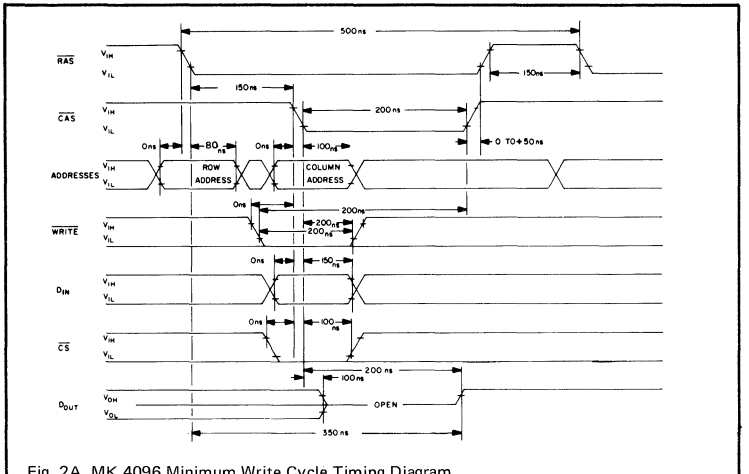


Fig. 2A MK 4096 Minimum Write Cycle Timing Diagram

*PDP – Trade mark of Digital Equipment Corp.

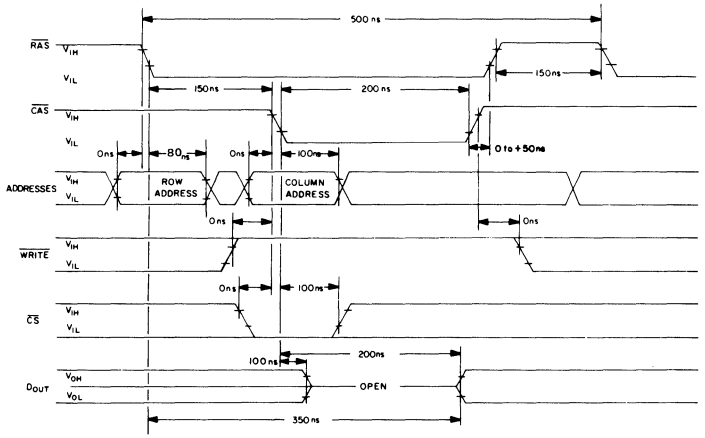


Fig. 2B MK 4096 Minimum Read Cycle Timing Diagram

Since the first function of the chip is to read the information contained in a row of cells, inputs such as column addresses, $\overline{WRITE}$, $\overline{CS}$ and Data In are not needed until the row of cells is read by the sense amps. This allows time to first strobe in the row address and later, with $\overline{CAS}$, strobe and latch the column address and $\overline{CS}$. ($\overline{WRITE}$ and DIN are not latched by CAS allowing a read-modify-write cycle as mentioned in the MK 4096 Data Sheet). Next, if CS is true and the column address is decoded, one of the 64 sense amps will be selected to output data to the output buffer latch. The $\overline{WRITE}$ line is high (READ CYCLE). Also the data is rewritten into the row from which the data was read initially. If the $\overline{WRITE}$ line is low, the data on the DIN line is latched by the "AND" of $\overline{CAS}$, $\overline{RAS}$, $\overline{WRITE}$ and $\overline{CS}$. The selected sense amp now receives the new data and the information being held by the other 63 sense amps will be rewritten into the selected row. Thus, the information in the selected row is refreshed by any cycle. Each row must receive at least one cycle to refresh it every 2 mS.

INPUTS				DATA OUT *	CYCLE PWR	ROW REFRESH	FUNCTION
$\overline{RAS}$	$\overline{CAS}$	$\overline{CS}$	$\overline{WRITE}$				
A	A	A	A	(VALID DATA) – OPEN – I	375 MW	YES	WRITE CYCLE
A	A	A	I	(VALID DATA) OPEN – (VALID DATA)	375 MW	YES	READ CYCLE
A	A	I	DC	(VALID DATA) OPEN – OPEN	375 MW	YES	REFRESH
I	A	DC	DC	(VALID DATA) OPEN – OPEN	12 MW	NO	STAND BY, OUTPUT DISABLED
I	I	DC	DC	(VALID DATA) (VALID DATA) (VALID DATA)	12MW	NO	STAND BY

* Previous Cycle - Intermediate - Present Cycle

A = Active I = Inactive DC = Don't Care

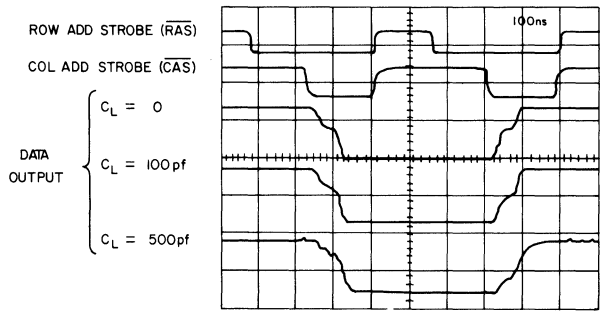
Fig. 3 MK 4096 Control Inputs Function Chart

MEMORY CYCLES

The MK 4096 has several subtle qualities that are not obvious by looking at the block diagram or timing diagram. $\overline{RAS}$, $\overline{CAS}$, $\overline{CS}$, and $\overline{WRITE}$ have 16 possible combinations with only 5 possible modes of operation. Figure 3 is a function chart describing interrelationship of the strobes and control inputs on the MK 4096. An "A" indicates an input will be active during a cycle and an "I" indicates inactive.

There are three types of cycles possible with $\overline{RAS}$ active. These cycles are: the normal read and write cycles and a refresh cycle and $\overline{RAS}$ and $\overline{CAS}$ active and $\overline{CS}$ inactive. Each of these cycles refreshes the addressed row and dissipates active power. The Dout waveform is different for each of these cycles.

Figure 4 shows the output waveform for three cycles where a "1" is latched at the output and then a "0" is read and then in the next cycle another "1" is read. The figure shows data is held from the previous cycle until $\overline{CAS}$ becomes active at which time the output goes to an open circuit, high impedance state. When the data is accessed, the output changes from the open state to true data. The Dout column in Figure 3 shows the transition that is seen on the output for each of the cycles. Note for a write cycle, the Dout goes to a "1". When Dout goes open circuit-



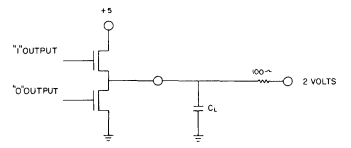


Fig. 4 Effects of Capacity loading on the MK 4096 output

ed after $\overline{CAS}$, a TTL device connected to the outputs may begin to oscillate because the input is floating. A 10K pullup resistor to +5V will keep the TTL device from oscillating.

If $\overline{RAS}$ is inactive and $\overline{CAS}$ is active, the only function that will be performed by the chip is to change the output to a high impedance state when $\overline{CAS}$ goes low. The power dissipated in this mode is negligible. This cycle allows a system operating with 8K of wire-ORed memory to decode the 13th address bit and gate $\overline{RAS}$ to only the selected 4K block while both blocks receive $\overline{CAS}$ and $\overline{CS}$. Receipt of $\overline{CAS}$ guarantees the unselected 4K output will go open circuited if true data was still available from the previous cycle. Thus only half the memory will be consuming active power for any given memory access. A refresh cycle, however, will require all 8K of the memory to be activated.

If both $\overline{RAS}$ and $\overline{CAS}$ are inactive the chip is in the standby mode and will consume a maximum power of 12 mW. The Dout will be held valid in this situation for at least 10 µS. The output latch is dynamic and the charge on the latch leaks off.

OUTPUT BUFFER

The output buffer, shown in figure 4 is a three state device. In the "1" state, the pull-up transistor has a maximum resistance of 500 ohms to +5 (V_{CC}). The transistor will source 5mA minimum at an output voltage of 2.4V. The current sourced in the output "1" state is the only current the device draws from the +5V supply. The pull down transistor has a maximum resistance of 200 ohms to ground (V_{SS}) in the "0" state. The transistor will sink 2mA at an output voltage of 0.4V maximum.

When the +12V supply (V_{GG}) is turned on, the output may "come up" in any of the three states. If two wire-ORed outputs come up in opposite conducting states, curent would be flowing from the +5V supply to ground through the two outputs. Typically this would be a 300 ohm path to go round. This occurance will not harm the devices and will last only a few hundred microseoncds until one circuit goes open circuited. This situation can be avoided by bringing up the +12V supply, and a few milliseconds later bringing up the +5V supply or immediately giving each chip a $\overline{CAS}$. Again the chip will not be harmed and it will be only an added momentary drain on the +5V supply.

Figure 4 also shows typical output buffer waveforms with a 100 ohm load to 2.0V and different capacitive loads. Note the output goes to the open state after $\overline{CAS}$ becomes active and then goes to the true data output at access time. The first waveform is loaded only with the resistive load and approximately 15 pF of stray capacitance. The second waveform shows the effects of driving a 100 pF load. The third waveform shows the output driving a 500 pf load. Less than 20 nS speed degradation occurs between essentially no load and 100 pF load, demonstrating the drive capability of the MK 4096 output buffer. The MK 4096 is tested with 100 pf of load capacitance.
If a CMOS interface is required at the output, the V_{CC} supply may be raised from +5V up to +12V. This will not effect anything except the output levels. The output levels may be calculated by using the output device resistances given previously. For standby situations, the V_{CC} may be reduced to 0V to save power.

CURRENT DRAIN

The MK 4096, when in the inactive state, (both $\overline{RAS}$ and $\overline{CAS}$ high), draws only 1 mA maximum and 0.5 mA typically from the +12V supply and 75 µA maximum from the −9V supply. The 75 µA from the −9V supply is purely a leakage current. The 1mA from the +12V supply is a D.C. path to ground through the $\overline{RAS}$ input buffers. The majority of the V_{GG} current is drawn when $\overline{RAS}$ returns to the inactive or precharge state. At this time, all the internal circuitry is precharged to an initial condition awaiting the next cycle. The current waveform that is drawn from the +12V supply is shown in figure 5. The figure shows a peak current of 80 mA at precharge. If $\overline{RAS}$ does not become active, the current drain will decrease to less than 1 mA to the standby condition. As $\overline{RAS}$ becomes active, a series of current peaks of 30 mA or less occur as the internal clocks generate the timing phases that are necessary to accomplish the cycle.

The current drain from the +12V supply will be less than 30 mA when averaged over the entire cycle. A dynamic current waveform such as this requires proper distribution and bypassing techniques to minimize noise voltages in a memory system. The current spikes passing through the inductive distribution lines can cause noise spikes of several volts

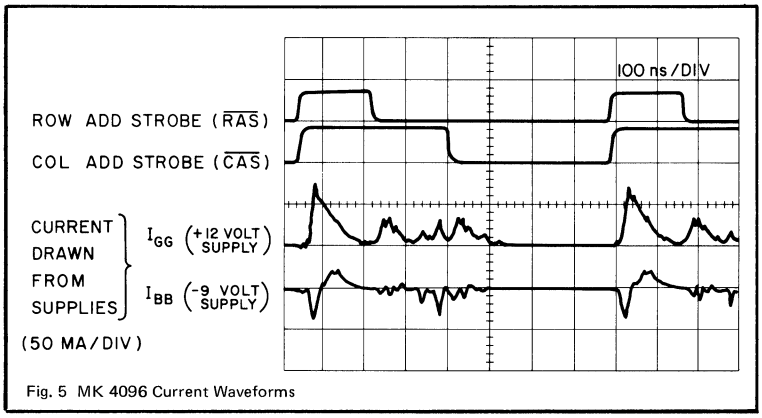


Fig. 5 MK 4096 Current Waveforms

on the supply lines unless proper bypassing is implemented.

Figure 5 also shows the current waveform on the −9V substrate supply (V_{BB}). The current has a peak value of 30 mA and the major spike is approximately 50 nS wide. This current fluxuation is present because the precharge is charging capacitance to both the ground diffussions and the substrate. Although the peak current is 30 mA, the average current is less than 75 μA. The current drawn during precharge is pumped back later in the cycle. This occurs because of the redistribution of charge between the bypass and internal substrate capacitances. The amount of bypassing needed for a system is to a large extent determined by how well the ground and power supply distribution is implemented. A multilayer board with power and ground planes is the most desirable situation. Two sided boards can be used with proper bypassing techniques if care is taken to minimize inductance in the gournd and power lines. This means maximizing the widths of the V_{SS} and V_{GG} supply lines.

The MK 4096 requires the steady state value of the supply lines to be within the limits defined by the data sheet and the noise on the +12V supply line should be less than 0.35V peak to peak. The peak to peak noise on the V_{BB} + V_{GG} supply lines must be less than 0.5V. The noise on the supply lines can be reduced through use of low inductance bypass capacitors distributed throughout the memory matrix. For most systems, a 0.01 μF ceramic capacitor per MK 4096 on the +12V line and one 0.01 μF per three MK 4096's on the −9V supply line will adequately reduce the noise.

When the +12V supply is turned on and V_{BB} is at ground, all the transistors will be depletion mode devices and approximately 150 mA will flow from the +12V supply to ground. When the V_{BB} supply is turned on to −9V, the transistors become enhancement mode and current flow decreases to the usual amount. This will not harm the MK 4096, but will load the +12V supply.

INPUTS

All MK 4096 inputs, including $\overline{RAS}$ and $\overline{CAS}$ are high impedance. The inputs require only TTL voltage levels and do not require the input source/sink currents of TTL gates. The inputs are small capacitors (less than 10 pF for address lines and less than 7 pF for $\overline{RAS}$, $\overline{CAS}$, $\overline{CS}$, and DIN) with a maximum of 10 μA leakage current.

In a memory matrix, when several address inputs are tied together, the inputs look like distributed loads along a transmission line. Since a number of MK 4096 inputs may be driven by one driver, care should be taken in choosing the driver, laying out the circuit board, and terminating the input lines to the memory matrix. The usual techniques of dealing with transmission lines can be applied here.

If a memory is to operate at its maximum speed, fast drivers must be used on the critical path signals. The drivers will have transition times between 10 nS and 30 nS and delay times of 20 nS or less. If input lines are not terminated, reflections will occur and severly degrade the quality of the input signals. Ringing on these lines can cause the input voltage specifications to be violated and memory errors may occur.

To avoid this type of problem, first the input drivers should be as close to the matrix as possible. Second, the MK 4096's should be spaced evenly along the line and discontinuities should be avoided if possible. Third, the lines should be terminated. The choice of termination will depend upon the driver that is chosen and its output drive (source/sink) characteristics.

The input buffers are designed for maximum speed with TTL input voltages. If the inputs are at a voltage greater than 7V and switch to ground, the propagation time will be increased because of internal parasitic capacitors that must be discharged. The inputs that are making a negative going transition should not go below ground more than 1V for the same reason.

Figure 6 shows the relative typical drive capabilities of several TTL drivers into four different loads. The rise and fall times in the chart also reflect the propagation time through the drivers.

PDP-11 INTERFACE

The PDP-11 minicomputer interfaces to the memory through an asynchronous bus. This asynchronous bus is common to the minicomputer, memory and peripherals such as card reader, line printer, disc., etc. The bus is bidirectional with 16 data lines, 17 address lines, and several control lines. The control lines that are important to the memory are the ones that control data in and out of the memory.

The memory discussed here is a 16K word x 16 bit memory. The controller for this memory is hardware encoded to respond to a continuous 16K block of addresses of the possible 128K addresses on the bus. Each time an address is placed on the bus the decoder checks to see if the add-

DEV	R	T_R		T_F		DEV	R	T_R		T_F	
		33pf	300pf	33pf	300pf			33pf	300pf	33pf	300pf
7437	Pull Up	16	28	17	26	7437	Pull Up	15.5	28	19.5	28
7438	180 Ω	25.5	63	17	25	7438	330 Ω	28.5	83	19	30.5
8T09*	Pull Down	16	27	16	29.5	8T09*	No Pull Down	15	27	18	29.5
8T09**	270 Ω	25	64	17	24.5	8T09**		28	78	19	30
7404		19.5	37	25	53	7404		19	41	28.5	71
74S00		14	25	12	21	74S00		13	25	13.5	24

* ENABLE LOW; PULSE GENERATOR TO DATA INPUT

** DATA INPUT HIGH; PULSE GENERATOR TO ENABLE

*** T_R AND T_F INCLUDE PROPAGATION DELAY AND ARE MEASURED FROM 10% TO 90% MINIMUM TTL LEVELS.

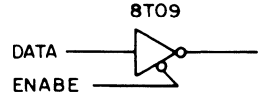


Fig. 6 Relative drive capabilities of TTL drivers.

ress is one of the 16K addresses that is assigned to the memory. If the address is one of the 16K addresses, the Address Decode input in figure 7 will be true.

The bus signals for a read and write cycle are shown in figure 8. For a write memory cycle, the processor places the address, data to be stored, and a write signal on the bus. The memory controller will decode the address to see if one of the 16K addresses is selected. Address Decode will be high for a decoded address. The memory controller then decodes the 13th and 14th addresses to select the 4K word block being addressed. Only the required 4K word section will receive a $\overline{RAS}$. Thus only one 4K word of the memory will be drawing active power (30 mA/MK 4096 max) and the remainder of the memory will be drawing standby power (75 µA/MK 4096 max).

The processor allows 150 nS for deskewing of the addresses across the bus and decoding of addresses before placing Master Sync ($\overline{MSYN}$) on the bus. ($\overline{MSYN}$ is inverted by the receiver and is shown as MSYN in figure 7.) Master Sync ($\overline{MSYN}$) is the signal that tells the memory controller to start the cycle. $\overline{MSYN}$ and the proper address decode are required to initiate the data transfer between the processor and the memory. The signals from the processor will remain on the bus until a transfer complete signal is sent from the memory controller to the processor. This signal is Slave Sync ($\overline{SSYN}$).

$\overline{SSYN}$ is placed on the bus approximately 350 nS after the write cycle is begun. At this time the MK 4096 cycle is not complete, but the inputs from the processor are no longer needed. Thus, the processor can be using the 150 nS that are necessary to finish the cycle to accomplish other tasks. The processor is inactive while waiting for $\overline{SSYN}$.

The same basic bus timing is used for a memory read cycle. The major difference is that $\overline{SSYN}$ and Data Out must be placed on the bus at the same time. The processor must allow time for deskewing on the data lines once $\overline{SSYN}$ is received. This requires 75 nS. The memory controller must keep data and $\overline{SSYN}$ on the bus until $\overline{MSYN}$ returns high. Since the data is latched at the out-

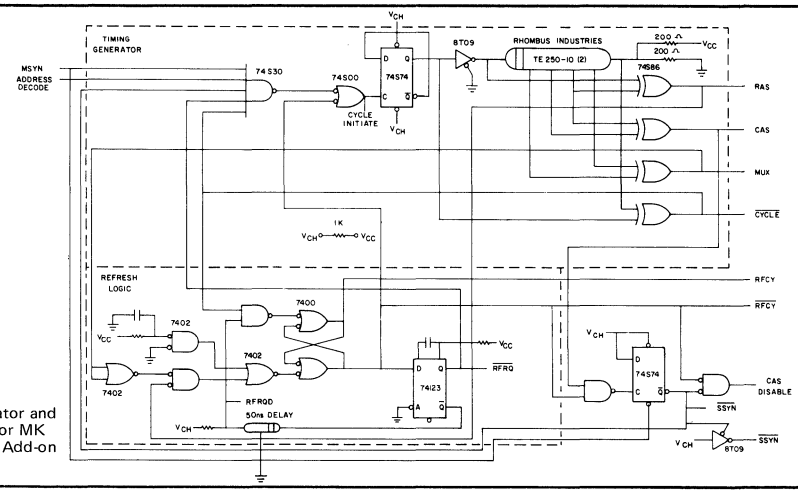


Fig. 7 Timing generator and refresh logic for MK 4096 PDP-11 Add-on memory

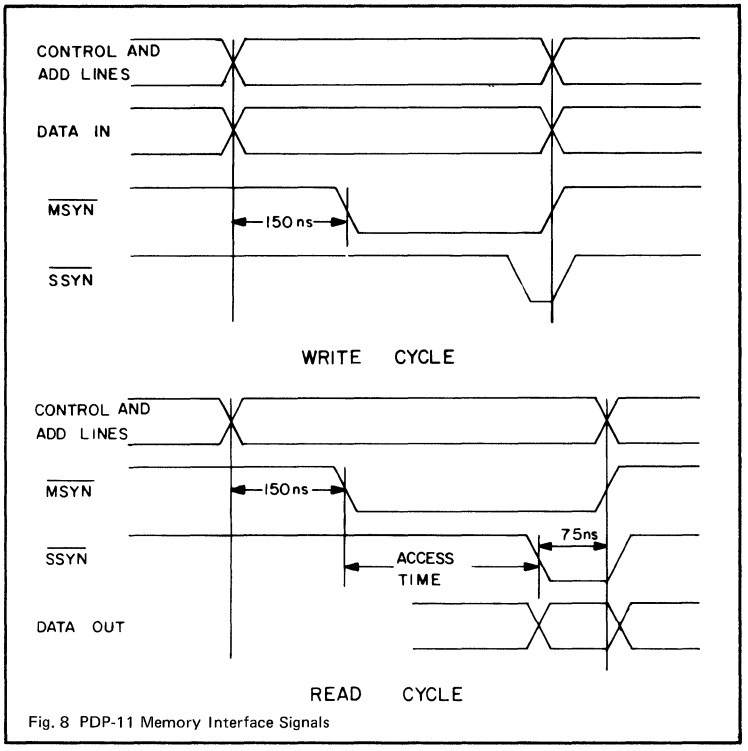


Fig. 8 PDP-11 Memory Interface Signals

put of the MK 4096, there is no need to latch data out or prolong a read cycle to keep data true, as required for the competitive 22 pin 4K RAMs. When $\overline{\text{MSYN}}$ returns high the controller removes $\overline{\text{SSYN}}$ and data from the bus.

CONTROLLER

The controller shown in figure 7 performs three functions. The controller must generate all the necessary timing signals that are necessary for the MK 4096 cycles and also generate signals that control the data bus. Since the MK 4096s are dynamic, data must be refreshed every 2 mS. The memory controller also performs this task.

The timing signal generator section of the controller generates the same signals regardless of the type of cycle being performed. The signals generated are the Row Address Strobe (RAS), Column Address Strobe (CAS), Multiplexer Control (MUX) and a signal that tells the controller that a cycle is in progress ($\overline{\text{CYCLE}}$). These signals are shown in figure 9. The timing signal generator uses two Rhombus Industries TE 250-10 delay lines. The delay lines are each 250 nS delay, tapped every 25 nS and cascaded together to give the 500 nS cycle time required by the MK 4096. The 74S74 flip flop is used as a divide-by-two circuit so only one transition edge will pass down the delay line each cycle. The exclusive-OR gates detect the transition at the appropriate tap down the delay line. The exclusive-OR gates respond with a pulse whose width is equal to the spacings of the inputs along the delay line. The pulse will be the same polarity regardless of the polarity of the transition passing through the delay line. The 74S74, delay lines, and exclusive-OR gates in the timing signal can be replaced by the "one-shot" diagram shown in figure 10. The "one-shots" may be cheaper, but are much harder to adjust and less reliable than the delay lines.

The controller gates $\overline{\text{RAS}}$ to the selected 4K word block for a read or write cycle. For a refresh cycle, the decoder gates $\overline{\text{RAS}}$ to all four 4K word blocks in the memory. MUX is needed to signal the address multiplexer to switch from the row address to the column address that the MK 4096 s requires. The multiplexers, shown in figure 11, must also switch to the refresh row address in a refresh cycle. The multiplexers are wired in such a manner that during a refresh cycle, the multiplexer will switch to the refresh row address regardless of the MUX signal.

The $\overline{\text{CYCLE}}$ signal is used to keep the refresh logic from initiating a refresh cycle while a processor initiated cycle is in progress. The same is true if a refresh cycle is in progress and the processor sends $\overline{\text{MSYN}}$ to the memory. When and only when a cycle is completed will the controller allow another cycle to start.

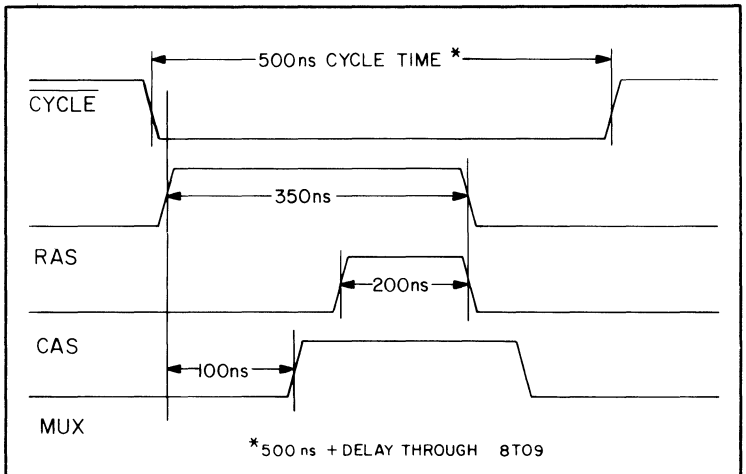


Fig. 9 Signals generated each memory cycle by the memory controller

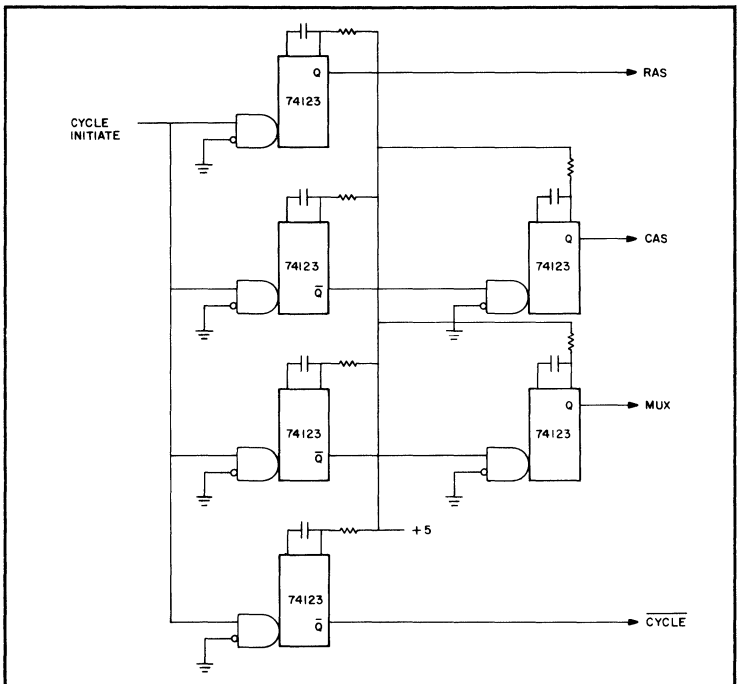


Fig. 10 "one Shot" circuit for generating timing signals

For a refresh cycle, the controller must select each of the four $\overline{RAS}$ drivers, switch the multiplexers to the refresh row address, and deselect all the chip select ($\overline{CS}$) lines to the MK 4096s. Once these tasks are accomplished, all the MK 4096s will receive $\overline{RAS}$ and $\overline{CAS}$ with the proper row refresh address to refresh one row in each MK 4096. At the end of the refresh cycle, the refresh row address counter is incremented to the next row address that will be refreshed and starts the next 30 µS interval.

The refresh logic interrupts the normal operation of the memory system once every 30 µS to refresh one row address. A refresh request (RFRQ) signal notifies the controller, at the end of the 30 µS period that it is time to refresh a row. If a read or write cycle is in progress, the controller will complete the cycle in progress and then initiate the refresh cycle. Figure 12 shows the timing diagram for a system cycle followed by a refresh cycle followed by another system cycle.

The MK 4096s have 64 rows in the memory matrix. By interrupting read and write operation once every 30 µS to refresh one row, the controller insures that each row will be refreshed once every 2 mS. The refresh row address counter is a six bit counter. The counter need not be synchronous since it has 30 µS to count from one address to the next. The counter is clocked by the trailing edge of Refresh Cycle ($\overline{RFCY}$). The refresh address counter, multiplexers, and Row Address Strobe ($\overline{RAS}$) decoder are shown in figure 11 The "one-shot" used for the 30 µS timing in the refresh logic is a 74123 since the duty cycle is greater than 95%.

An alternative method for multiplexing the addresses is shown in figure 13. The devices shown are Signetics 8T09 line drivers. These drivers are three state devices with a disable input. The drivers are wire-ORed together and the end of the address line will be terminated with a pull-up resistor. This method uses 6 packages and the method shown in figure 13 uses only 5. The 74S153s are expensive, so the wire-ORed 8T09's have a cost and speed advantage.

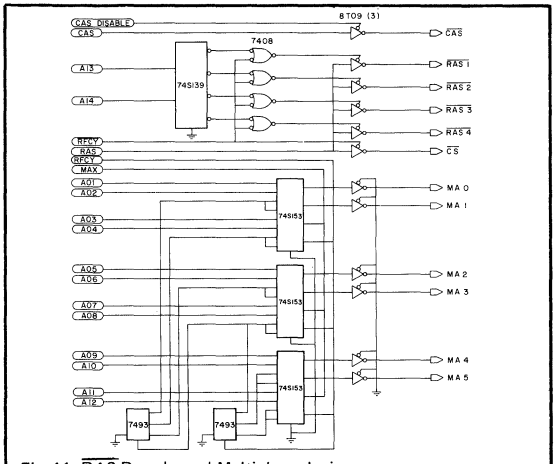


Fig. 11 $\overline{RAS}$ Decoder and Multiplexer logic

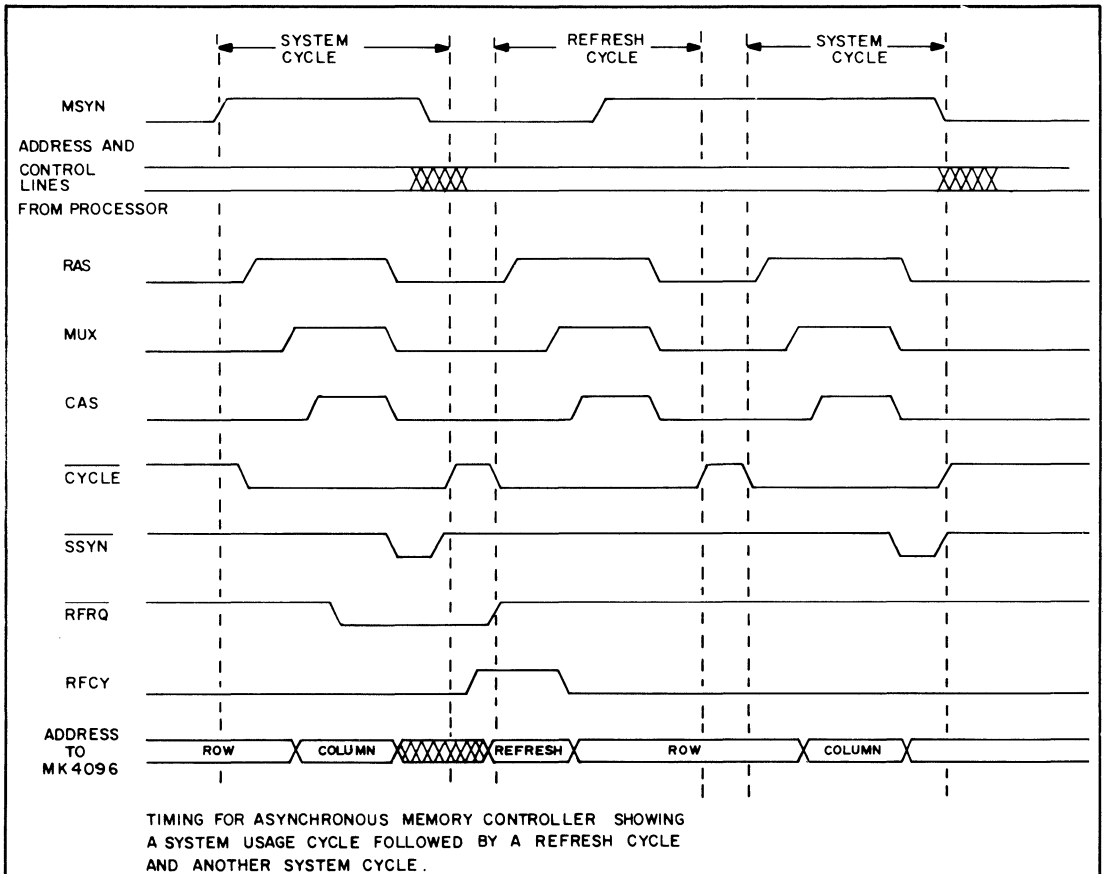


Fig. 12 Timing diagram for MK 4096 PDP-11 Add-on Memory System

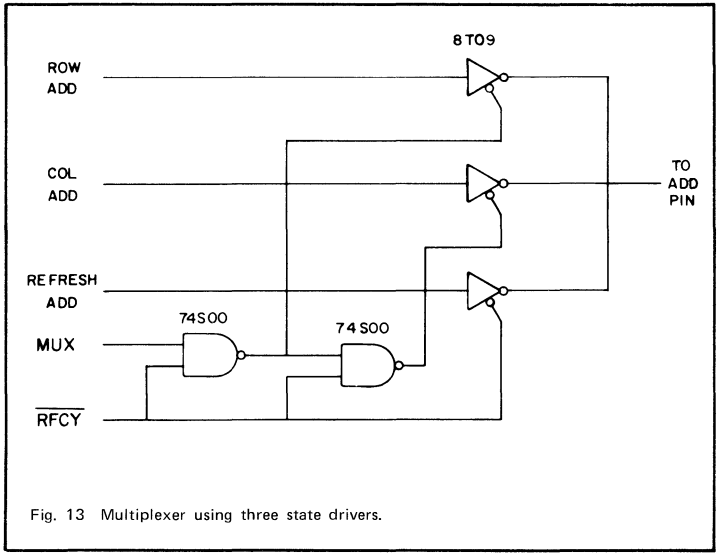


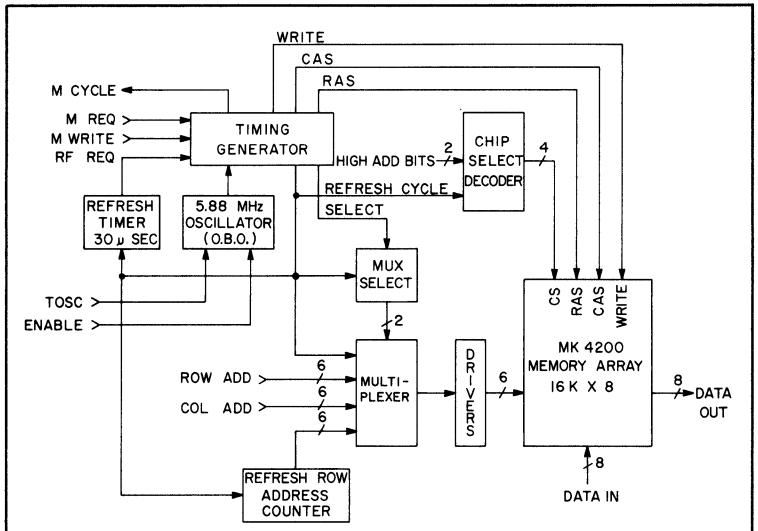
Fig. 13 Multiplexer using three state drivers.

CONCLUSION

Advantages such as full TTL compatibility, small 16-pin package, and data output latches allow the system designer to design a system without the need for high level drivers or output data latches.

The MK 4096 was developed with the user in mind.

Considerations For Designing A High Density, Low Power Memory System



FUNCTIONAL DIAGRAM

INTRODUCTION

A main concern of many semiconductor memory systems designers is deciding which memory device best meets the requirements of his particular system. Generally it is assumed that the memory device chosen for the job must be a high performance, high density, low power device. It is also desirable for the device to lend itself to a non-volatile memory system design. If one carefully examines all of the MOS RANDOM ACCESS MEMORIES on the market today, a logical choice to meet these requirements is the MOSTEK MK 4200.

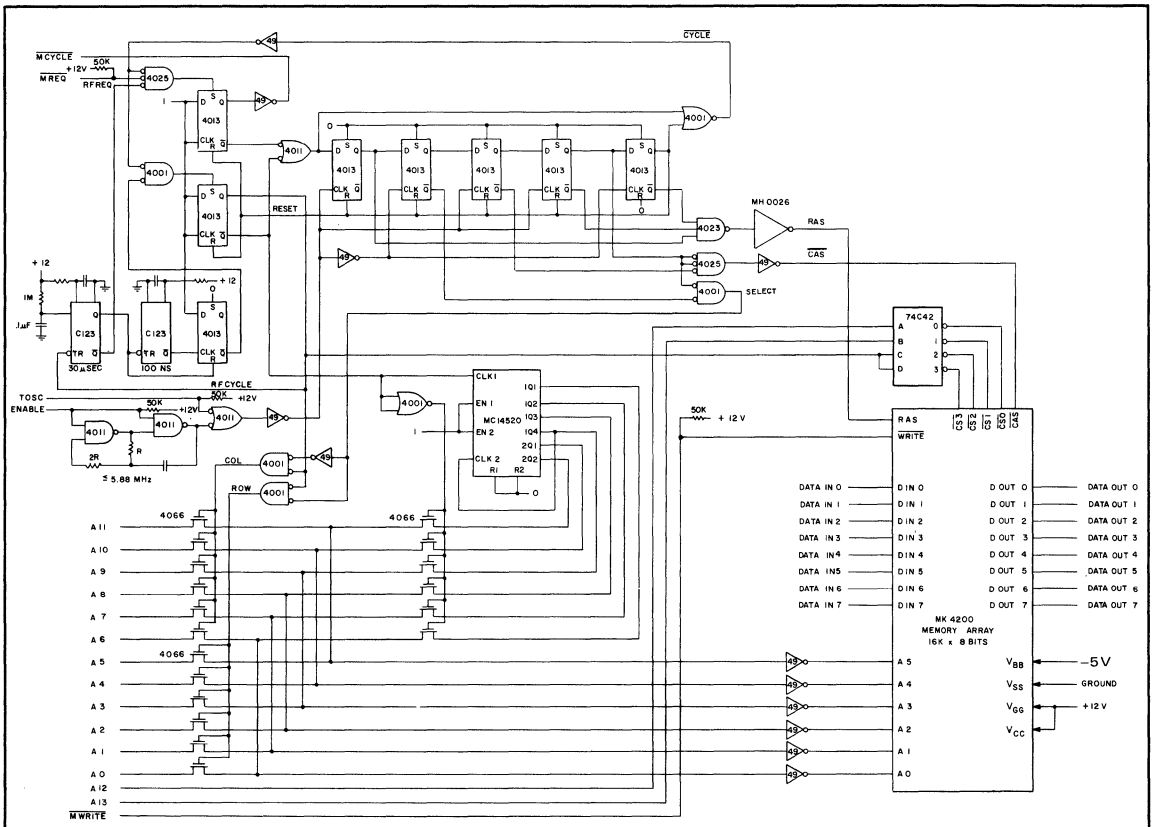
The intent of this paper is to explore some of the trade offs encountered in designing a low power memory system and to examine the features of the MK 4200. The approach taken is an asynchronous memory system implemented in CMOS logic. The controller will operate a 16K x 8 bit memory array consisting of 32 MK 4200 parts. It will also have the ability to convert to battery back-up in the case of system power failures.

MEMORY DEVICE

Like the MK 4096, the MK 4200 is a 4096 x 1 bit dynamic MOS RANDOM ACCESS MEMORY. The unique design of these parts allows them to be packaged in a standard 16-pin DIP. This results in much greater memory packing density than any other 4K RAM. To make the MK 4200 a very low power device, the first driver stage of the ROW ADDRESS STROBE input is bypassed. By doing this, the MK 4200 RAS input requires a high level (12V) signal rather than TTL. Since the conversion of TTL to MOS logic levels is done externally, the power normally dissipated by the internal circuitry required for the conversion is substantially reduced. Most of the circuitry used in the MK 4200 is dynamic and draws power from the V_{GG} (+12V) supply as a result of the clock edges. Active power is under 400 mW while standby is less than 1 mW as compared to 12 mW in the MK 4096P.

The V_{CC} supply pin applies power only to the output buffer and is not required during standby operation. Current requirements for this supply are totally dependent upon output loading. The V_{CC} voltage can range from 0 to 12 volts. This makes interfacing to TTL, DTL, CMOS, etc. directly compatible. All inputs to the MK 4200 (except RAS) are TTL compatible. The address and data inputs are designed in such a way that a logic 0 is 0.8 volts and a logic 1 is 2.4 volts. Logic 1 level for $\overline{CAS}$ and $\overline{WRITE}$ is 2.7 volts. These trip points hold true even though the inputs will accept a signal as high as V_{GG} (+12V). In most cases, such as in a CMOS system, the need for level converting circuitry is eliminated. In choosing a device to drive the input lines, one should keep in mind that the MK 4200 represents capacitance loads and not current loads like TTL. The requirement for the address and data drivers is that they provide sufficient drive capability to insure proper logic levels to the memory chips at the time that the information is required. For the ROW ADDRESS STROBE input the driver must be able to charge the capacitance load of the RAS input from within .6 volt of V_{SS} (0V) to within 1 volt of V_{GG} (+12V) in 50 nanoseconds. This can be done by means of a discrete driver or one of the many commercial MOS clock drivers on the market.

Twelve address bits are required to select one out of 4096 bit locations in a 4K RAM. In the case of the MK 4200, only 6 address inputs are required. Addressing is accomplished by the generation of Row and Column address strobe signals to latch incoming multiplexed addresses into the chip. This task is handled by the memory controller.



SCHEMATIC

MEMORY CONTROLLER

Ideally, a memory controller should be an uncomplicated circuit and yet meet all requirements of the system. The MK 4200 requires relatively few control signals but the circuitry required to generate these signals may consume more than its share of system power when implemented in TTL. In many cases low power is more critical than high speed. This is the ideal application for a CMOS controller and high density CMOS compatible dynamic RAMs.

Since standard CMOS will operate over a wide supply voltage range, the V_{CC} (+5V) normally used by TTL is not required. Instead, the CMOS will be operated from the V_{GG} (+12V) supply. Also, the V_{CC} supply for the MK 4200 will be taken to V_{GG}. This will allow direct interface with the CMOS both into and out of the RAMs and eliminates the need for an extra power supply. Also, operating CMOS at this high voltage allows for highest possible operating speeds and better noise immunity.

MEMORY CYCLES

The memory controller must be able to perform three types of cycles when controlling dynamic RAMs. These are processor requested READ or WRITE cycles and REFRESH cycles. To initiate a memory cycle, the processor sends a MEMORY REQUEST signal (MREQ) to the memory controller (see timing). If no other memory cycle is occurring the controller will acknowledge the MREQ signal and output the MCYCLE signal back to the processor. A CYCLE IN PROGRESS signal is shifted one bit at a time down a shift register and various register outputs are logically "AND" ed to form the timing signals for the memory system. The clock for the timing generator shift register is a precise frequency that originates in the processor. This clock (TOSC) controls the pulse width of the ROW and COLUMN ADDRESS STROBES required to multiplex addresses into the MK 4200. The frequency of this oscillator should not exceed 5.88 MHz tokeep the MK 4200 operating within data sheet specifications. The schematic shows an on-board oscillator that is used only in standby operation.

During a normal READ or WRITE cycle the row addresses are enabled first. After allowing ample time for these addresses to reach proper levels in the matrix, the ROW ADDRESS STROBE occurs and latches the ROW ADDRESS into the RAMs.

As the SELECT signal occurs the ROW ADDRESS is disabled and the COLUMN ADDRESS is enabled through the multiplexer. The COLUMN ADDRESS STROBE is generated to latch the COLUMN ADDRESS into the RAMs. During a REFRESH CYCLE both the row and column addresses are disabled and only the REFRESH ROW ADDRESS COUNTER is enabled.

As soon as the memory cycle is complete the MCYCLE signal is removed from the system interface. This transition, as MCYCLE goes from a high to a low logic level, is an indication to the processor that data is valid from the memory. This negative going edge can be used to clock data into the processor. Also at this time the MREQ signal should be removed from the controller. The processor has one complete cycle time of the TOSC oscillator to remove the MREQ signal. It is possible to keep the MREQ signal applied to the memory controller and only change the address to the memory to initiate a new memory cycle.

CHIP SELECT DECODE

There are two modes of chip select decoding in a MK 4200 system. The most efficient way is to decode the RAS signal and gate it as a chip select to enable only one 4K block of memory at a time. This mode is best for large memory systems because power dissipation is drastically reduced since only the selected 4K block dissipates active power. The other method is to decode the CHIP SELECT signal from the two high order address bits to select one of the 4K blocks of memory. Since the CHIP SELECT and also the WRITE signal are not required until very late in the cycle, their decode times do not add to memory access time. Also, only one high level RAS driver is required instead of four with RAS decode. The disadvantage is high system power since all RAMs are active in this mode.

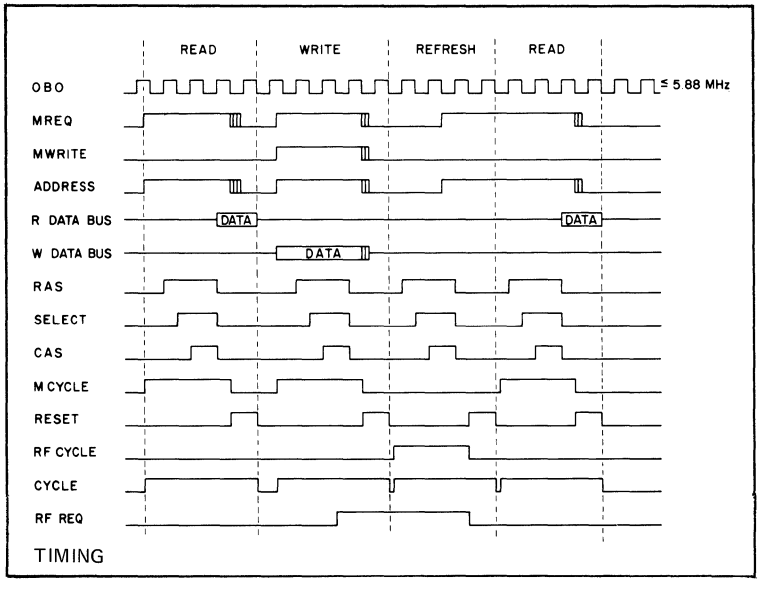
REFRESH CYCLE

The dynamic nature of the MK 4200 requires that a memory cycle be executed at each of the 64 row addresses every 2 milliseconds or less. In the memory controller, a retriggerable one shot is adjusted to have a pulse width of 30 microseconds. When the refresh timer one-shot times out, a REFRESH REQUEST (RFREQ) is output to the memory control logic. If the memory is not busy or as soon as the memory controller completes any cycle previously in progress a REFRESH CYCLE begins. The RFREQ signal also prevents any new processor requested cycles from beginning.

During a REFRESH cycle only the REFRESH ROW ADDRESS is enabled by the multiplexer. Also, the REFRESH CYCLE signal (RFCYCLE) disables the Chip Select Decoder. On the trailing edge of RFCYCLE the REFRESH ROW ADDRESS COUNTER is incremented and the REFRESH TIMER ONE-SHOT is retriggered.

STANDBY MODE

Several things happen when the memory system goes into the standby mode. First of all the TOSC oscillator becomes inactive and the on-board memory oscillator is enabled. The ENABLE input is connected to a sensing device that monitors the power supply of the processor. The ON - BOARD OSCILLATOR (OBO) is set at a very noncritical frequency. It is advised that the frequency of OBO be much slower than TOSC because the CMOS controller will require less power at lower operating speeds. The controller must be kept operative in the standby mode to execute REFRESH CYCLES for the memory every 30 microseconds. All control inputs to the memory system should be pulled up to V_{GG} (+12V) during standby.

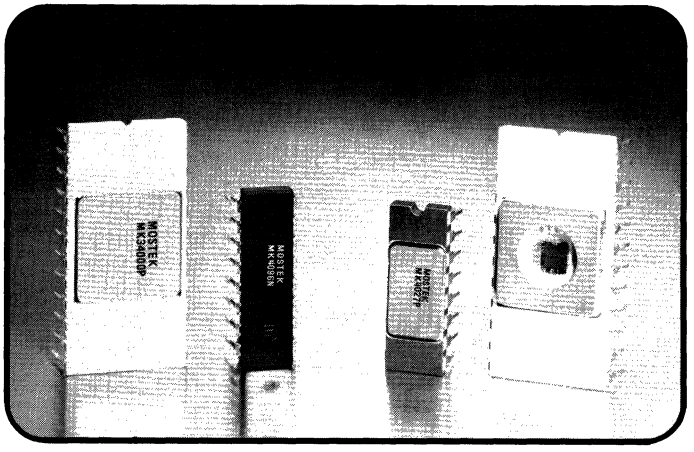


TIMING

PERFORMANCE

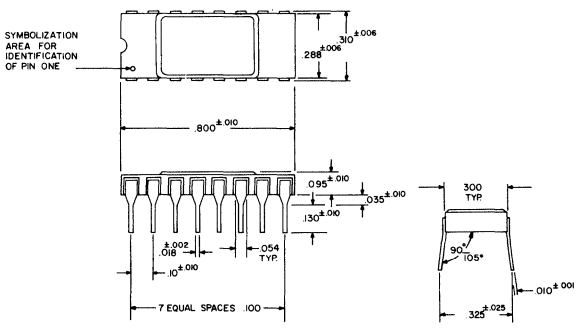
Obviously, a memory controller implemented with CMOS logic is not going to be the most efficient system in terms of speed. However, access time for this system was measured to be 775 nanoseconds and cycle time was under 1 microsecond. Active power for the CMOS controller is under 400 milliwatts. In standby with the controller operating at reduced frequency, a savings of approximately 75 milliwatts can be realized. Standby power for the complete system including the MK 4200 RAMs is under 500 milliwatts. With REFRESH CYCLES included, average standby power is less than 850 milliwatts. A TTL memory controller of similar complexity will typically dissipate 3.5 watts from the V_{CC} (+5V) supply alone.

PACKAGING

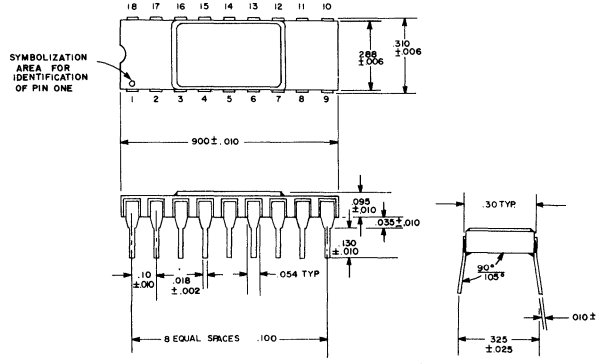


CERAMIC DUAL-IN-LINE HERMETIC PACKAGING (P)

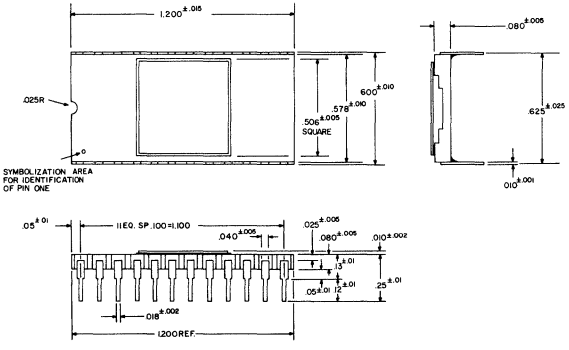
16-Lead Side-Braze Package



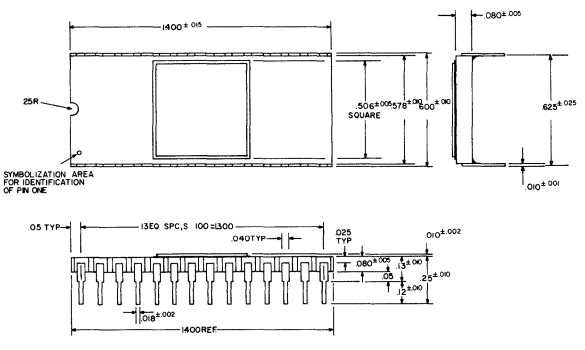
18-Lead Side-Braze Package



24-Lead Side-Braze Package

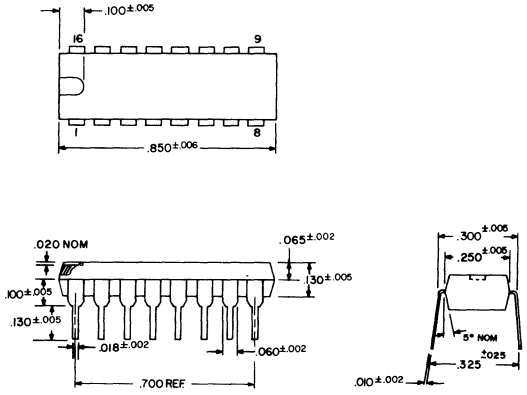


28-Lead Side-Braze Package

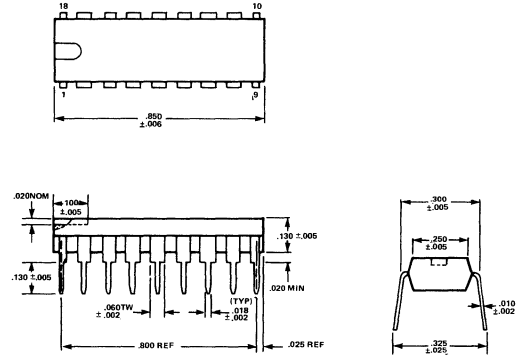


PLASTIC DUAL-IN-LINE PACKAGING (N)

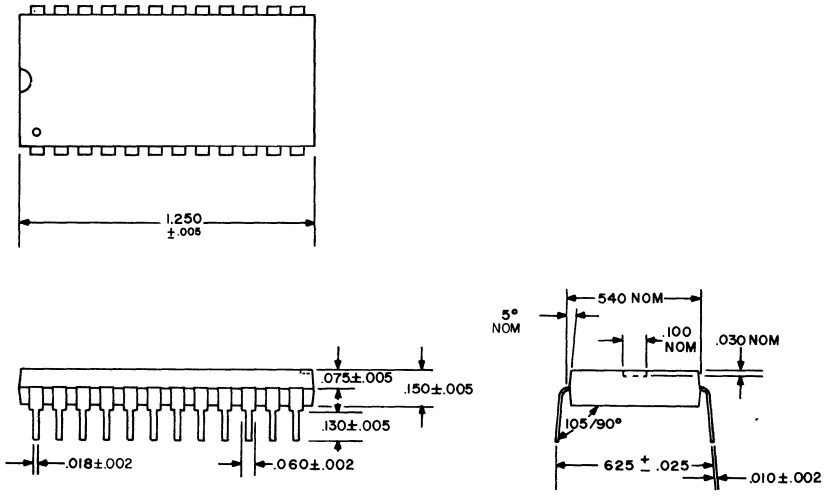
16-Lead Package



18-Lead Package

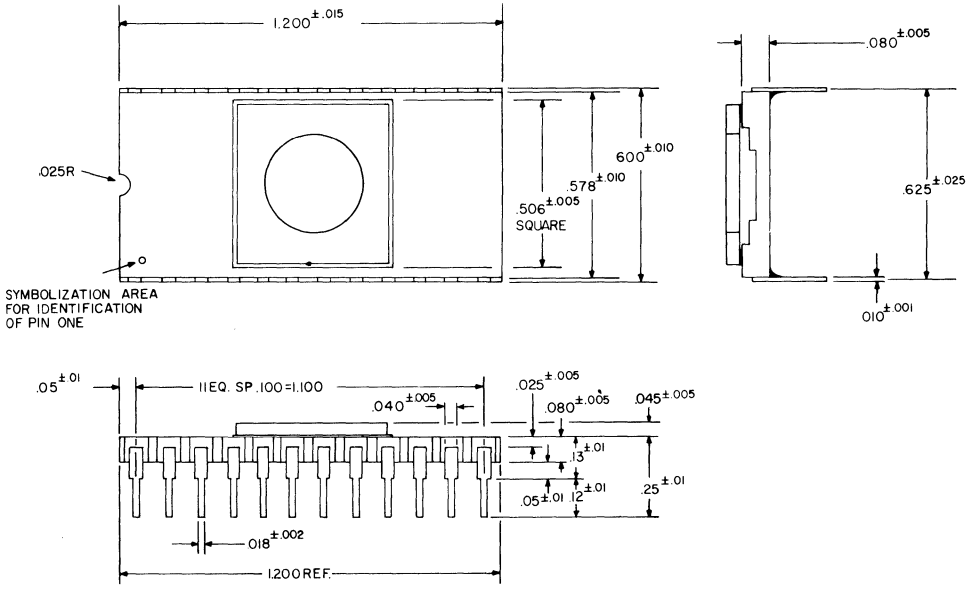


24-Lead Package

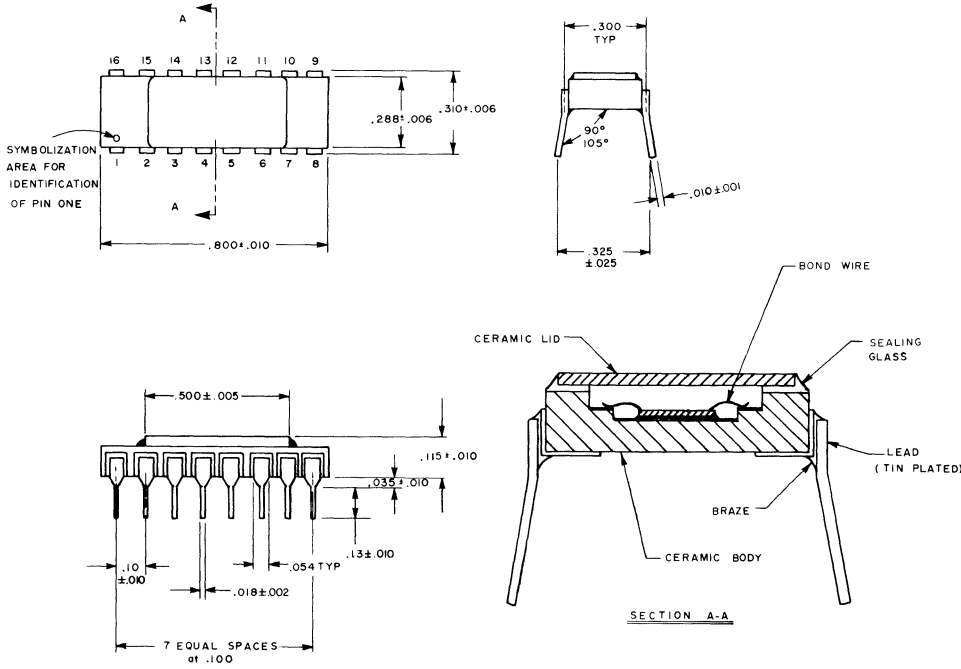


ALTERNATE HERMETIC PACKAGING (T)

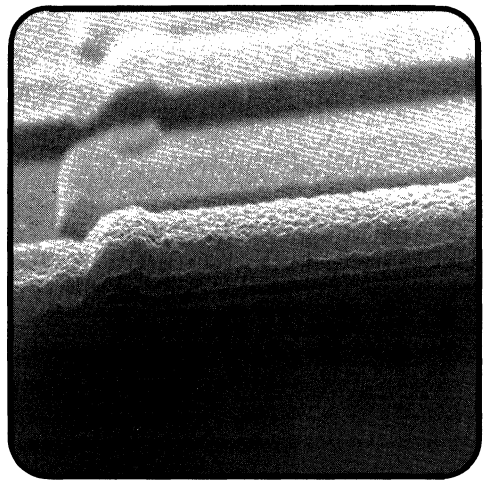
24-Lead Side-Braze Ceramic Package With Transparent Lid

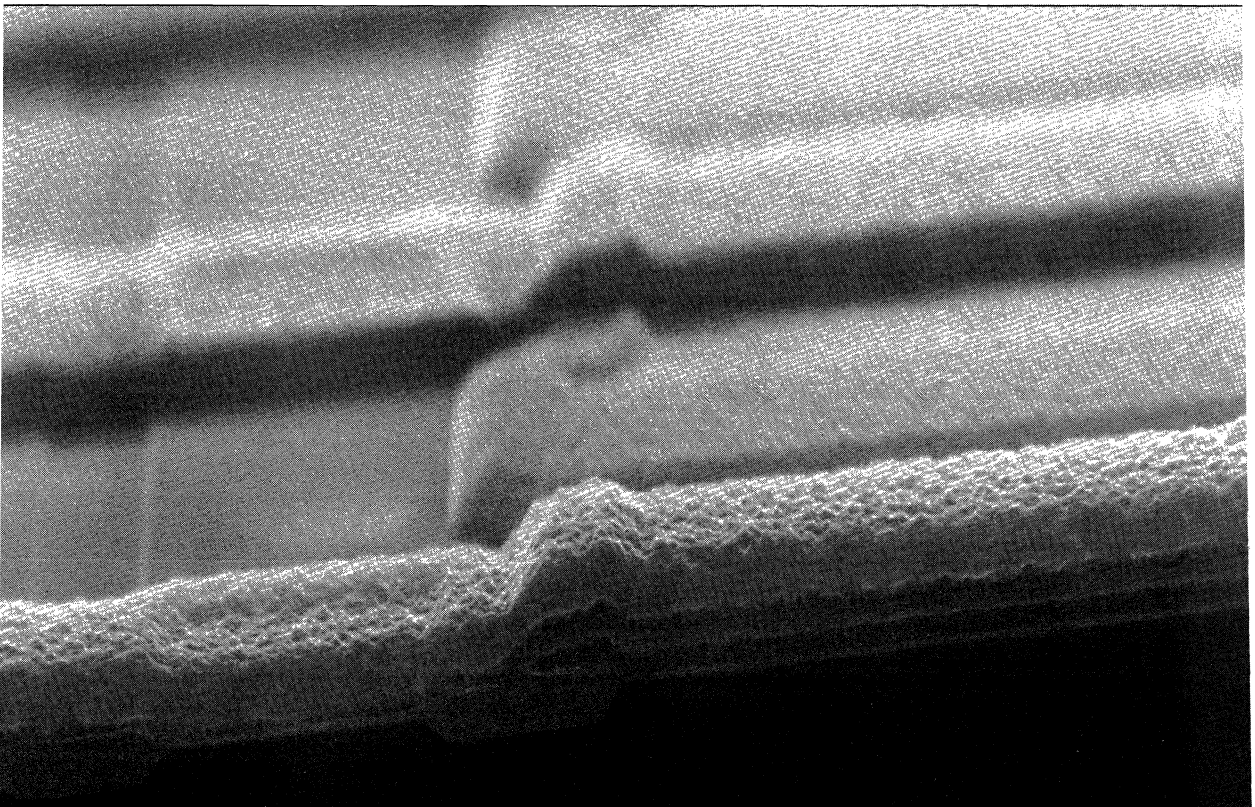


Tin-Plated, Frit-Sealed Ceramic Lid, Side-Braze Package (K)



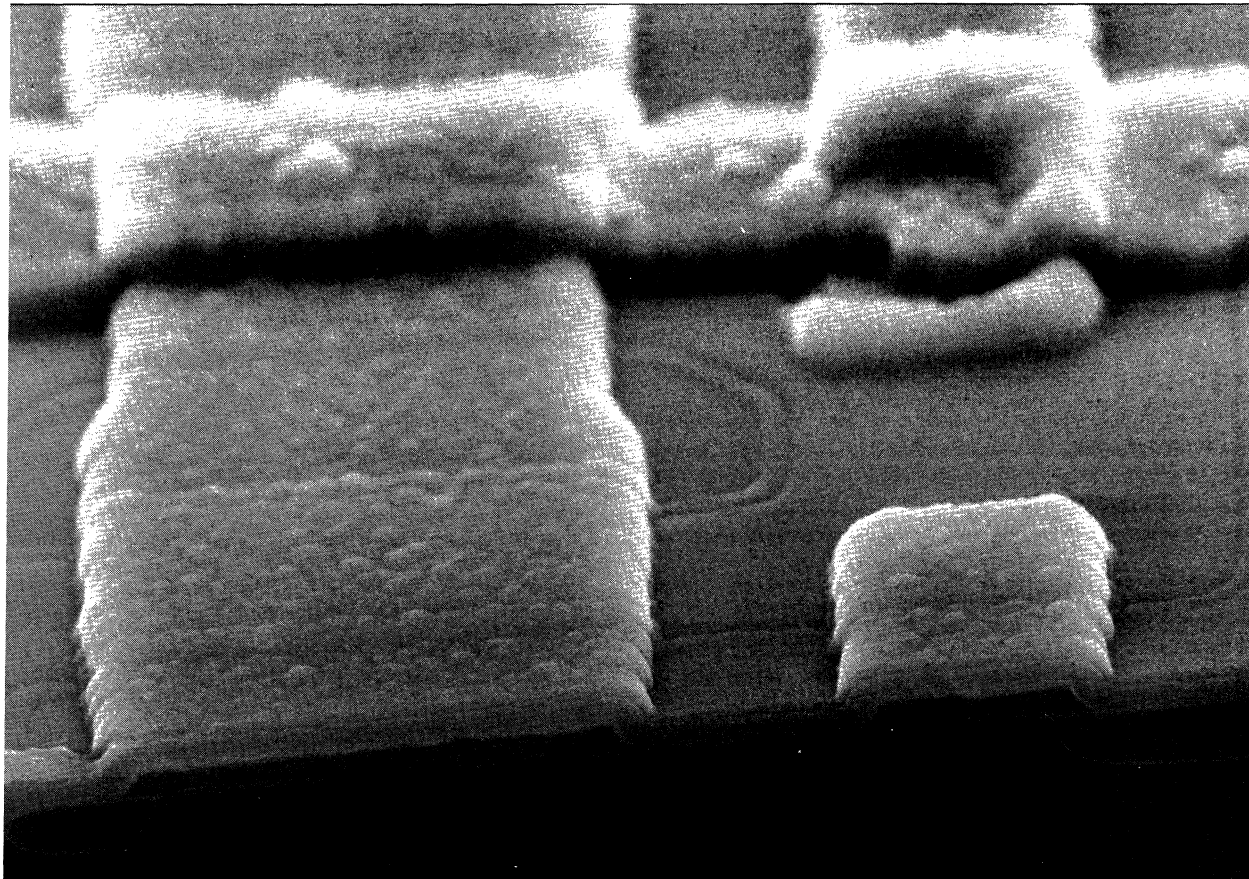
RELIABILITY INFORMATION





CONTENTS

Metal Gate Cell Typical of MK 4096



APPENDICES

Silicon Gate Cell Typical of MK 4027

1.0 INTRODUCTION

This report is designed to summarize reliability knowledge about MOSTEK'S 4K RAM products. It is an update of previously published reports, and covers the MK 4096 in both ceramic and plastic and the newer MK 4027.

The testing described herein was not initiated with this report in mind. This data is a beneficial spin-off of MOSTEK'S in-house program to control reliability.

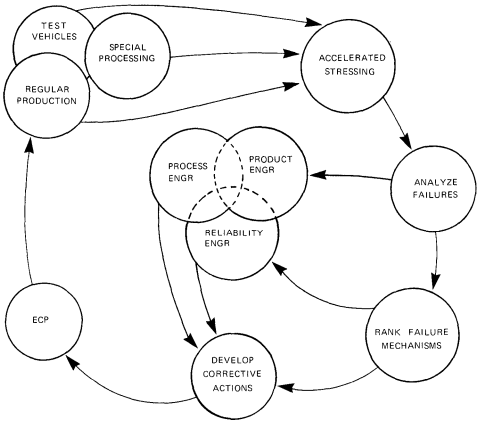
The goal of MOSTEK'S reliability test program is to continually improve reliability regardless of what that reliability may be. This is achieved by obtaining and disseminating sufficient meaningful data derived from accelerated stresses that all engineering and QRA personnel are aware of and can act on the types and causes of failure modes affecting product reliability.

Commensurate with this philosophy, MOSTEK'S approach to reliability testing takes the form of accelerated stressing of various levels of product and special test vehicles in a closed-loop corrective feedback system as indicated in the bubble-chart.

Once again, the primary intent is to continually improve reliability of the product.

At any one point in time, MOSTEK has a very large reliability test effort underway on memory devices. The chart below summarizes some recent examples of 4K test effort.

MOSTEK's RELIABILITY TESTING APPROACH



4K RELIABILITY EFFORT

Present Level of Reliability Effort = Approximately 19,500 Units on Various Tests

EXAMPLES OF TESTS

Program	Sub-Sets
P/M/P (Production Monitor Program)	• 4096P • 4096N • 4027P
Sub-Contractor Qual	• Three Sub-Contractor Facilities
Package Qual	• K-Package • "Other" Package Configurations
New Product Qual	• 16K RAM
Mil-Qual	• MKM 4096P-XX Products

Program	Sub-Sets
Assembly Process Evaluations	• Thermosonic Bonding • Ultrasonic Bonding • Step-Stress Studies • Thermal Resistance Studies
Front End Evaluations	• Numerous Proprietary Process Evaluations

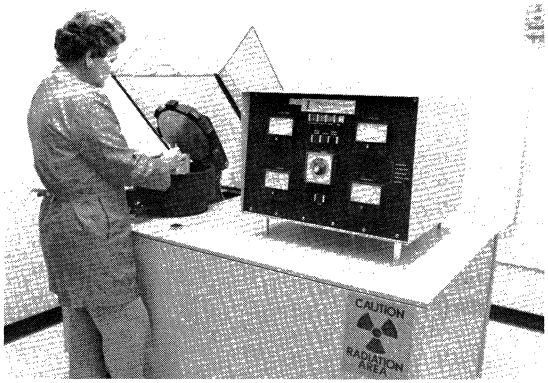
The data presented in this report is summarized from the P/M/P portion of this chart. MOSTEK'S Production Monitor Program (P/M/P) is a routine sampling of outgoing product run on various reliability tests.

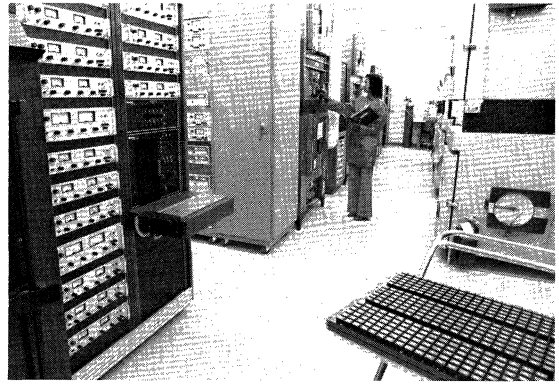
These P/M/P samples are typical of "shipped" devices all of which are subjected to standard 4K flow which includes the hi-rel processing (Right).

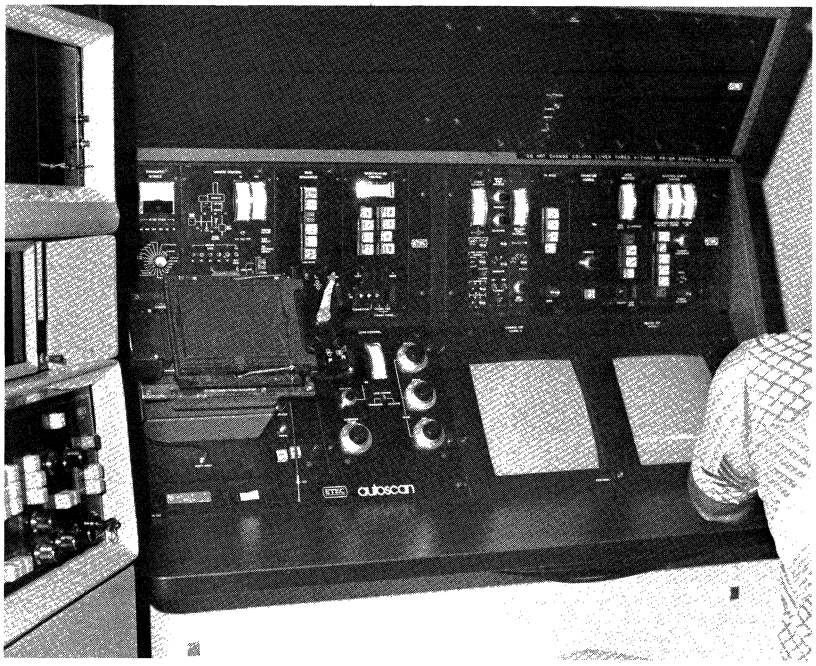
All of MOSTEK'S 4K RAM products receive the above processing *(except plastic product which does not receive hermeticity or centrifuge).* This processing is very key to obtaining the superior field reliability as discussed later in this report.

RELIABILITY ENHANCEMENT PROCESSING

- 100% Fine & Gross Leak Test
- 100% Temp Cycle
- 100% Centrifuge
- 100% Hi Voltage, Hi Temp, Dynamic Burn-In
- 100% Hi Temp, Worst-Case, Multi-Pattern Final Test
- Comprehensive QA Lot Acceptance Testing Prior To Shipment







Above left: Radioactive Tracer Flo System
Above right: Mostek burns-in well over one million devices per month.
Left: SEM (Scanning Electron Microscope) with EDS (Energy Dispersive Spectrometer) attachment.

2.0 MK 4096P RELIABILITY

MOSTEK'S oldest 4K RAM, the 4096 in ceramic, is a very high volume, mature product line. Because the closed-loop feedback system described above has been effective on this product, the failure rate is at an all time low.

The latest summary of P/M/P data on the 4096P run on longterm 125°C operating life tests is shown (Right).

As a point of reference, the previously published failure rate for the MK 4096P at +125°C was 2.5%/KHrs (January 1976). It should be noted that the data in this present report is "all new." There is no duplication of data published in the previous report. If data from the two reports is combined, it represents almost 6400 devices tested on long-term accelerated life tests . . . probably the largest 4K RAM accelerated life test data base in existence.

This failure rate is, of course, at highly accelerated conditions, the applicability of this data to in-use conditions will be discussed later in this report, but does require a knowledge of failure mechanisms. Each of the 34 failures generated in the above testing received an in-depth failure analysis and report. A summary of the categories of failures is shown (Right).

Dielectric defects occurring in the various oxide and nitride structures of the device are expected to be a primary failure in any MOS LSI device and must continually be monitored and controlled. "Foreign Material" mechanisms are also a classical area of concern in a surface sensitive technology such as MOS. This manifests itself in a variety of mechanisms as will be discussed later, but on the MK 4096 will most often result in a threshold shift, particularly affecting trip point of the sense amps. "Bulk Defects" are closely akin to, and may interact with, foreign material mechanisms and include such things as P-N junction leakage.

SUMMARY OF MK 4096P CERAMIC (C-DIP) PACKAGE
125°C LIFE TEST STUDIES

Stress	Quan.	Fail	Longest Stress Hours	Total Device Hours @ Temp.
Dynamic Operation at +125°C	4002	34	3,000	4,579,044

Point Failure Rate (λ_0) Estimate at +125°C Equals 0.74%/KHRS.

FAILURE MECHANISMS
FOR
MK 4096P +125°C LIFE TEST STUDIES

Mechanism	Percent Contribution
Dielectric Defects	23.5
Foreign Material	20.6
Bulk Defects	20.6
Bonding	11.8
Undetermined	11.8
Metalization	8.8
Package Defects	2.9
Total:	100.00

Total Population: 34 Devices

3.0 MK 4096N RELIABILITY

MOSTEK QRA department qualified the 4096 chip in a 16 pin novalac epoxy dip package in 1975, and since then over 5 million 4096's have been shipped in plastic. These 4K RAM's receive the same reliability considerations and processing as ceramic devices. The latest composite of accelerated life testing of over 1000 MK 4096N plastic devices is summarized (Right).

This failure rate is slightly higher than the MK 4096 in ceramic, but the failure mechanisms must be considered in order to put this comparison in proper perspective.

A summary of the in-depth analysis of these 25 failures are shown (Right).

Note that the vast majority of these plastic failures on 125°C operating life are associated with "Foreign Material." This predominance of foreign material as the underlying failure mechanism is certain to have a pronounced effect on derating this 125°C life test failure rate down to some lower use-type condition. Foreign material is generally conceded to have one of the highest thermal activation energies of any of the common IC failure mechanisms. It can result in acceleration factors of an order of magnitude higher than other mechanisms. As such, it is not inconceivable that plastic packaged RAM's *could* have as good reliability under use conditions as their ceramic packaged counterparts. This is not inconsistent with inputs from some users who have experience with both.

SUMMARY OF MK 4096N PLASTIC PACKAGE
+125°C LIFE TEST STUDIES

Stress	Quan.	Fail	Longest Stress Hours	Total Device Hours @ Temp.
Dynamic Operation at +125°C	1056	25	3,000	1,553,268

Point Failure Rate (λ_0) Estimate at +125°C Equals 1.6%/KHRS.

FAILURE MECHANISMS
FOR
MK 4096N +125°C LIFE TEST STUDIES

Mechanism		Percent Contribution
Foreign Material		76.0
Undetermined		12.0
Dielectric Defects		8.0
Bulk Defects		4.0
	Total:	100.0

Total Population: 25 Devices

4.0 MK 4027P RELIABILITY

In addition to the MK 4096 device which uses metal-gate "SPIN" technology, MOSTEK offers the MK 4027. The MK4027 is a high-performance, pin-compatible version of the 4K RAM, but uses N-Channel, SI-Gate, technology.

Although more recently announced than the MK 4096, a significant data base has been established on the MK 4027 in the ceramic side-brazed package. A summary of recently compiled life test data, some of which is past 5000 hours, is shown (Right).

This 125°C failure rate of 1.2% per thousand hours is superficially slightly higher than the previously presented MK 4096 data. However, the implications of this at a use condition level can be fully appreciated only with a detailed knowledge of the individual failure mechanisms.

A detailed analysis of these 45 failures shows a distribution as shown (Right).

This distribution of mechanisms is what might be expected for a SI-Gate device in the earlier phases of production. The de-rating considerations of such a data set will be discussed later in this report.

SUMMARY OF MK 4027P CERAMIC (C-DIP) PACKAGE
+125°C LIFE TEST STUDIES

Stress	Devices	Fail	Longest Stress Hours	Total Device Hours @ Temp.
Dynamic Operation at +125°C	2934	45	5,000	3,699,960

Point Failure Rate (λ_0) Estimate at +125°C Equals 1.2%/KHRS.

FAILURE MECHANISMS FOR MK 4027P LIFE TEST STUDIES

Mechanism	Percent Contribution
Dielectric Defect	26.7
Bonding	17.8
Foreign Material	15.5
Mounting	11.1
Undetermined	11.1
Awaiting Analysis	17.8
Total:	100.0

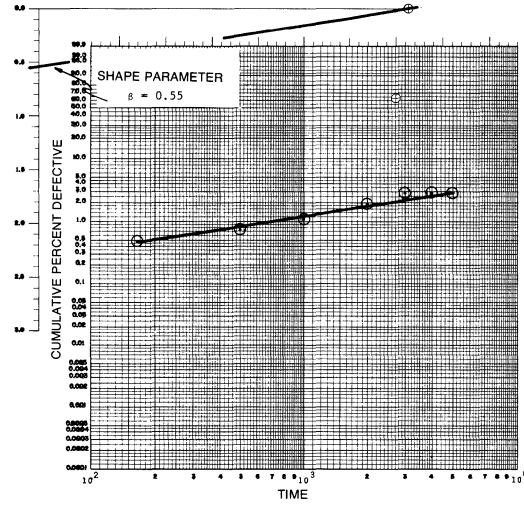
Total Population: 45 Devices

5.0 FAILURE RATE vs TIME

MOSTEK consistently measures its RAM products as having a decreasing failure rate with time. The rate of decrease varies slightly with device and package style, but ranges between 0.5 to 0.7 as the value of β *(shape factor)* in the popular Weibull distribution.

These values are obtained from plotting life test results on standard Weibull charting paper such as shown below for the MK 4027.

WEIBULL PLOT OF MK 4027P
LIFE TEST STUDIES



6.0 ENVIRONMENTAL STRESSING

Operating life test data has been emphasized in this report because of its popularity with users in attempting to obtain insight into system level failure rates. MOSTEK does, however, support a fairly large environmental test effort for controlling and definitizing package and assembly related failure mechanisms.

This environmental effort takes the form of a cross-matrix of process technologies (NMOS, CMOS, etc.) versus package configuration (ceramic/plastic, 16 pin/40 pin, etc.). A large amount of testing has been done recently on plastic 4K RAMS because of the universal interest in plastic package technology.

This section will give an indication of the types of environmental test data available.

The emphasis on ceramic packaged devices is placed on environmental test sequences such as shown (right).

The ceramic side-brazed "P" package is rugged and exhibits very low failure rates on the classical IC environmental stresses.

16 pin ceramic product is run to MIL-STD-883 in support of the MKM-series of military type devices as shown (Page 10).

SUMMARY OF 16 PIN CERAMIC (MK 4096)
ENVIRONMENTAL STRESS STUDIES

Stress	Fail/Sample
Temperature Cycling −65°C to +150°C, 10 Cycles Constant Acceleration 20KG, Y_1 Plane Only (Sequential Stressing)	Hermeticity Endpoints* 18/4825

*MIL-STD-883A, Method 1014.1, Condition A
(Limit: 1 x 10^{-7} ATM-CC/SEC)and Condition C, Step 1

Electrical Endpoints 15/4696

MIL-STD-883

Subgroup 1	Method	Condition	Class B LTPD	Sample Size	Max No. Accept	Observed Fails
Thermal Shock	1011.1	Test Condition B	15	34	2	0
Temperature Cycling	1010.1	Test Condition C				
Moisture Resistance (With Bias)	1004.1	Omit Para. 3.1 & 3.4				
Seal	1014.1					
(A) Fine		1×10^{-7} ATM CC/SEC				0
(B) Gross		C_1				0
Visual Examination						0
End Point Electrical Parameters		Per MK 4096 Data Sheet Specs @ Ta = +70°C				0

Subgroup 2	Method	Condition	Class B LTPD	Sample Size	Max No. Accept	Observed Fails
Mechanical Shock	2002.1	Test Condition B	15	34	2	0
Vibration, Variable Frequency	2007	Test Condition A				
Constant Acceleration	2001.1	Test Condition E Y_1Only				
Seal	1014.1					
(A) Fine		1×10^{-7} ATM CC/SEC				0
(B) Gross		C_1				0
Visual Examination						0
End Point Electrical Parameters		Per MK 4096 Data Sheet Specs @ Ta = +70°C				0

Again, we find the 16 pin ceramic side-brazed package (MK 4096) has no difficulties in meeting all 883 stress requirements.

The environmental testing of plastic devices takes a variety of forms. One is step stress testing such as shown (Right) for the 16 pin plastic package (MK 4096).

Some other types of tests run on 16 pin plastic packages (MK 4096) are shown in the table (below right).

The moisture resistance test clearly shows that a plastic package is, by definition, not totally hermetic. All of the failures on this 2000 hour test were judged by testing to full "data sheet specs" at elevated temperature. The failures predominantly manifest themselves as a shift in threshold voltage *(commonly in the sense amp circuitry)* long before "metal corrosion" occurs. If failures are judged strictly on the basis of DC catastrophic failures, the time to failure is extended greatly.

Stress	Condition	Step	Fails/Sample
Thermal Shock	0°C to +100°C	15 cyc.	0/220
		30 cyc.	0/220
		45 cyc.	0/220
		60 cyc.	0/220
Temp. Cycle	−40°C to +125°C	10 cyc.	0/275
		50 cyc.	0/273
		100 cyc.	0/273
		300 cyc.	0/273
Temp. Cycle	−65°C to +150°C	10 cyc.	0/220
		50 cyc.	1/220
		100 cyc.	1/218
		150 cyc.	2/217

		Fails/Sample
Thermal Shock: −55°C to +125°C, 15~		
Temperature Cycling: −65°C to +150°C, 10~		
Moisture Resistance: 25°C to +65°C @ 95% RH; 240 Hrs. ΔV = 17V		
(Sequential Stressing)		0/84
Moisture Resistance:		
25°C to +65°C @ 95% RH	240 Hrs.	3/471
ΔV = 17V	500 Hrs.	4/468
	1000 Hrs.	28/463
	2000 Hrs.	27/338
Storage Life @ +150°C	168 Hrs.	0/109
	500 Hrs.	0/109
	1000 Hrs.	1/109

7.0 PREDICTED SYSTEM FAILURE RATES

The failure rate to be expected under actual use conditions is extremely difficult to determine for any low-failure-rate component. The two classical methods used are (1) to perform very large-scale, long-term testing *at* use conditions or (2) to perform testing under accelerated conditions. Either approach has its limitations, and MOSTEK recognizes there are no universally agreed-upon techniques.

However, use-level testing of the MK 4096 by our customers has been very gratifying to date. At the MOSTEK-sponsored "Users Forum" (May 1976) users reported approximately five million device-hours at "use conditions" with only one failure. It was noted that about 1/3 of this data was on plastic 4096's.

Another user has recently reported that he is predicting a failure rate of 0.02%/Khrs based on his qual testing of the 4096.

Yet another user says the 4096 "is the most reliable dynamic RAM (both 1K and 4K) that he's using." This is based on 0.3% fall-out at "final system burn-in."

All feedback from the field indicates that the in-use failure rate of the MK 4096 will be 50 to 100 times lower than that observed on 125°C operating life tests.

Commensurate with MOSTEK's stated philosophy on reliability testing, virtually all test data is taken at highly accelerated conditions — most usually 125°C operating life. There are various ways to extrapolate data from such a life test to lower use conditions. Probably the method with most authority is the RADC-developed acceleration curve published in MIL-STD-883A. *If* one chooses to use this curve (which happens to show a thermal activation energy of approximately 1.0eV) one *could* de-rate the 125°C data shown earlier in this report to 70°C as indicated in the table (Below).

Device	**Demonstrated** λ at 125°C (%/KHRS)	**Extrapolated*** λ at 70°C (%/KHRS)
4096P	0.74	0.007
4096N	1.6	0.016
4027P	1.2	0.012

**Using the MIL-STD-883A Accelerated life test curve.*

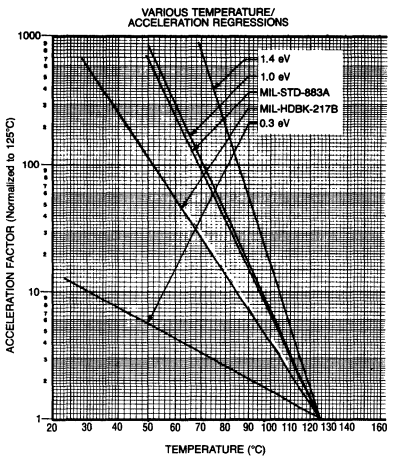
One should recognize that this is not universally accepted, and MOSTEK feels it is an over-simplification of a very complex question. However, as a "ballpark estimate," it does appear to be in "the range" of field experience.

Another, less used, acceleration factor appears in MIL-HDBK-217B. Although somewhat more complex to calculate than the 883A nomograph, this document gives generally lower acceleration factors.

MOSTEK feels that any complete analysis of accelerated life test data must give due consideration to the difference in thermal activation energies of the various failure mechanisms. It is also recognized that exact values of the activation energy of all but a very few mechanisms are not known. Still, there seems to be a general agreement on at least ranges for various mechanisms. It would appear that the more important MOS/LSI mechanisms fall in the following areas of thermal activation energies *(as measured in electron-volts as applicable to the Arrhenius or Eyring models).*

- Contamination Oriented Mechanisms .... 1.0 to 1.5eV
- Dielectric Defects ..... 0.1 to 0.5eV
- "Others" ..... 0.5 to 1.2eV

Any use of these activation energies must be with the appreciation for what a 0.1eV variation really means. The following graph can give an appreciation for the magnitude of possible error.



It can be seen that the range of activation energies being considered here result in acceleration factors over several *orders* of *magnitude.*

Unless a great deal of discretion is used in working with activation energies, one can get "caught up in the numbers game."

Still, it is obvious from the above chart that dielectric failures will de-rate at a much slower rate to use conditions than for a contamination-oriented type of failure. This is the basis for previously saying that the 4096 in plastic at normal operating temperatures *could* be as low as ceramic, due to the different distributions of failure mechanisms.

All of these acceleration factors are based on some form of the Arrhenius model which addresses thermal energy levels only. Any model for MOS devices which does not treat voltage stress considerations must, of necessity, be considered incomplete. A voltage-dependent technology such as MOS will not exhibit the same failure modes on both storage life and operating life.

Unfortunately, there are no proven MOS reliability models which do treat electrical stress levels. However, many of these variables will hopefully cancel if the electrical considerations are the same for both the accelerated life test and the use conditions. This is why MOSTEK uses the dynamic operating life test (per appendix 1) almost exclusively.

The life test failures discussed in this report have been "hard" failures. Experience to date indicates MOSTEK 4K RAM's do not have soft failure or pattern sensitivity problems. MOSTEK feels the single most effective reason has been the utilization of high temperature testing, generous guardbanding, along with multi-pattern testing which optimizes the internal stress modes to worst-case power supply corners. A summary of the MK 4096 test sequence is shown in Appendix 2.

APPENDICES

App. 1 Life Test Circuit

125°C DYNAMIC OPERATING LIFE CONDITIONS

Static Conditions	Dynamic Conditions
D_{OUT} = Open	Levels:
CS = 0 Volts	"0" Level = 0 Volts (+.8V Max)
V_{DD} = +13 Volts	"1" Level = 4 Volts (+2.4V Min)
V_{BB} = −5 Volts	Timing:
V_{CC} = 0 Volts	Cycle Time ≈ 2.6 μsec
V_{SS} = 0 Volts	
W = 0 Volts	

App. 2 Final Test Sequence

MK 4096 POST BURN-IN FUNCTIONAL TEST DESCRIPTION

TEST #	TITLE	TEST DESCRIPTION
1	Continuity (low bias)	Force −0.7 volts relative to V_{BB} on each pin in turn and check for a current of 100 μA or greater on each pin. Pins 9, 14 and 16 cannot be checked for continuity due to externally connected load resistors and decoupling capacitors. If all pins fail continuity, High Bias continuity (Test 2) is attempted.
2	Continuity (high bias)	Force −5 volts relative to V_{BB} on each pin in turn and check for a current of 100 μA or greater on each pin. If any pin passes this test the part is rejected as a "high substrate resistance" part.
3	Input Leakage	V_{BB} biased at −5 volts with respect to all other supplies, ground, and the output pin. All inputs are tied in parallel to 0 volts through the meter. A current greater than 1.5 μA magnitude is considered a leakage failure. Next the pins are similarly connected to 10 volts and again checked for 1.5 μA or less leakage current.
4	Substrate Leakage	All pins other than V_{BB} are grounded. V_{BB} is biased at −15 volts through the meter and checked for less than 50 μA leakage current.
5	I_{DD} Standby	The device is powered up with minimum V_{BB} and maximum V_{DD} conditions. The output is left floating and unused inputs are tied to 5 volts. RAS is held at 5 volts while CAS is toggled between 5 volts and 0 volts in order to deselect the output. The device is then checked for maximum I_{DD} in the standby state.
6	Checkerboard	Using a binary addressing sequence (rows fast) the data pattern is written into the entire memory followed immediately by reading the memory and checking each cell for the proper data output. Repeat sequence for data complement.
7	Ones	Same as Test 6
8	Horizontal Bar	Same as Test 6
9	Vertical Bar	Same as Test 6
10	Address Parity	Same as Test 6
11	Diagonal	Same as Test 6
12	Walking Diagonal (omitted on Rev. 3)	Using a binary addressing sequence (rows fast) a diagonal pattern is written into the memory followed by reading the memory for the same pattern. This procedure is then repeated with the diagonal data pattern shifting through all of the 64 possible positions. The entire procedure is then repeated for complement data.
13	Horizontal Bar-wide Inputs	Same as test 6 except $V_{IN(0)}$ = −1 volt and $V_{IN(1)}$ −5.5 volts.

TEST #	TITLE	TEST DESCRIPTION
14	Address complement address parity	Same as test 6 except addressing sequence is address complement instead of binary.
15	Burst refresh — ones	Using a binary addressing sequence (rows fast) the data pattern is written into the memory followed by a stall in the standby mode for the refresh interval with the CAS clock toggling. The entire memory is then read with each cell checked for proper data output. Repeat sequence for data complement.
16	Burst refresh — Horizontal bar	Same as test 15
17	Adjacent Row Disturb Refresh	Using a binary addressing sequence an all zeroes data pattern is written into the entire memory with row addresses as the fast axis. Odd numbered rows are then written with 1's with column addresses as the fast axis. The even rows are next written with O's again with column addresses as the fast axis. Finally the odd rows are read checking each bit for the proper output data. The procedure is then repeated for the opposite rows. Repeat entire procedure for complement data.
18	CAS Inactive Burst Refresh-Horizontal Bar	Same as test 15 except CAS is inactive (logic "1") during the standby refresh stall.
19	CS Disable Write — Address Parity	Using a binary addressing sequence (rows fast) the data pattern is written into the memory followed by an attempt to write a data complement pattern into the memory with CS at a logic "1". The entire memory is then read checking each cell for true data. Repeat procedure for data complement.
20	RAS Disable Write — Address parity	Using a binary addressing sequence (rows fast) the data pattern is written into the memory followed by attempting to write a data complement pattern into the memory with RAS at a logic "1". The entire memory is then read checking each cell for true data. Repeat procedure for complement data.
21	Read/Modify/Write Address Parity	Using a binary address sequence (rows fast) the data pattern is written into the memory. The entire memory is then scanned using read/modify/write cycles reading each cell and then writing data complement into the same cell. The memory is then again scanned using read/modify/writing cycles reading each cell for complement data and then rewriting true data into the cell. Finally the memory is read in a binary sequence checking each cell for true data.
22	Column Fast Address Parity	Same as Test 6 except column addresses change as the fast axis instead of row addresses.
23	Output Tristate	A chekerboard data pattern is written into the entire memory. Each cell is then read at a 1 us cycle rate with CS at a logic "1". During each chip deselected read cycle the output level is checked to be within ±.1 volt from the open circuit Voltage condition.
24	Column Disturb	Column 0 is written with an all ones data pattern an "0" is then written into row 0 of the column 100 times followed by reading all other bits of the column and checking each bit for a logic "1" output. Row 0 of the column is then rewritten to a "1" and the procedure is repeated for rows 1,2,3, . . . 63 of the column under test. The entire procedure is then repeated for columns 1-63.

TEST #	TITLE	TEST DESCRIPTION
25	Extended Cycle	With t_{MOD} = 10 μs, t_{WC} = 10.6 μs and all other timing parameters at data sheet minimum conditions a diagonal pattern is written into the entire memory followed by a pause of t_{REF} −680 μs duration in the standby mode. The entire memory is then read with t_{RC} = 10.6 μs and all other timing edges at data sheet minimum conditions. During the read cycle the output data is checked at the end of each cycle. Addressing sequence used for both read and write cycles is binary (rows fast). Repeat procedure for complement data.
26	V_{DD} Hysteresis	With V_{DD} = 5 volts a diagonal is written into the entire memory followed by reading the memory and ignoring all errors detected. V_{DD} is then restored to its test value and a diagonal complement data pattern is then written into the entire memory and then read checking each cell for proper data output. Addressing sequence is binary (rows fast).
27	V_{BB} Hysteresis	With V_{BB} = −1 volt a diagonal complement pattern is written into the entire memory followed by reading the memory and ignoring all errors detected. V_{BB} is then restored to its test value and a diagonal data pattern is then written into the entire memory and then read checking each cell for proper data output. Addressing sequence is binary (rows fast).
28	Gated CAS — Horizontal Bar	Same as test 6 except t_{RCL} = t_{RCL} (min.) t_{RCL} = t_{RCL} (max.) for all other tests.
29	Maximum Power	A "0" is repeatedly written at cell location row 0, column 0 at minimum specified write cycle time for 5 ms. The device is rejected if the I_{DD} average current exceeds I_{DD} max. during the test.
30	March	Using a binary addressing sequence (rows fast) an all ones data pattern is written into the memory. The memory is then scanned in a binary manner by first reading each cell addressed and checking for proper data and then writing the same cell with complement data on the following cycle before proceeding to the next cell location. When the entire memory has been scanned in this manner the memory is then scanned counting downward starting with cell location row 63, column 63 reading each cell addressed and checking for complement data output and then writing the same cell with true data before moving to the next cell location. Finally the entire memory is read checking each cell for true data output. Repeat procedure for complement data.
31	Pattern Sensitivity	Using a binary addressing sequence, one row is written continuously with 1's for 1 second at V_{BB} = −2.0 volts and V_{DD} = 13.2 volts. Complement data is then written into the entire matrix (rows fast) followed by reading the memory for complement data.
32	TMOD — MARCH	Using a binary addressing sequence (rows fast) the matrix is written with a 10μs time elapse interval between each bit being written. After having written the whole matrix in this fashion, each bit is read with a 1μs error strobe and written with opposite data, respectively, before the next cell is addressed. With complement data filling the whole matrix, this extended read cycle (followed by a write cycle) is executed looking for opposite data. With true data (1's) filling the matrix, the entire matrix is read using minimum "spec" access timing.

Unless otherwise specified in the test descriptions, the functional test conditions are as follows:

$V_{IN}(1)$ = min. data sheet limit − guardband Δ

$V_{IN}(0)$ = max. data sheet limit + guardband Δ

$V_{OUT}(0)$ = 0.4V @ 2 ma max. − guardband Δ

$V_{OUT}(1)$ = 2.4V @ 5 ma min. + guardband Δ

All timing edges are set to data sheet limits for minimum cycle time conditions − guardband Δ's

$T_J = T_J$ equivalent for 70C continuous still air ambient operation ($T_J = P_D X \Theta_{JX} + T_A$)

The functional tests performed at each voltage corner of V_{DD} and V_{BB} are listed below:

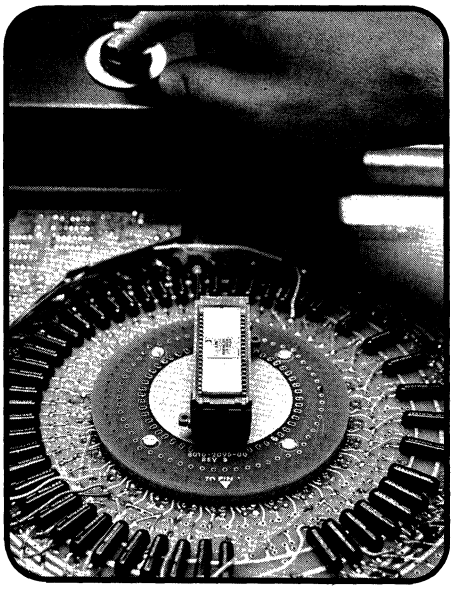
Voltage Corner	Test #'s Performed
V_{DD} min, V_{BB} max	6,7,8,10,11,13,14,15, 16,17,18,19,20,21,22, 23,25,26,28
V_{DD} max, V_{BB} min	6,8,10,12,14,19,20,21, 22,23,24,27,29,30
V_{DD} min, V_{BB} min	8,9,10,14,22,25
V_{DD} max, V_{BB} max	8,9,10,14,15,16,17,22

App. 3 Available Reliability Reports

The following reports treating of specialized reliability topics are available upon request.

Report Number	Dated	Title
74-0452	11/07/74	Plastic Package Qualification Report
RE-0106	05/03/76	MK 4096N Reliability Report
RE-0102A	09/23/76	Power Supply Considerations in the Use of 4K RAMS
RE-0103	02/20/76	Thermal Resistance Data on 16 Pin DIP's
RE-0096	08/19/75	Test Transistor Studies (4096)
RE-0097	08/19/75	Test Vehicle Studies (4096)
RE-0109/ 0110	07/20/76	Weibull Curves

MICROPROCESSORS



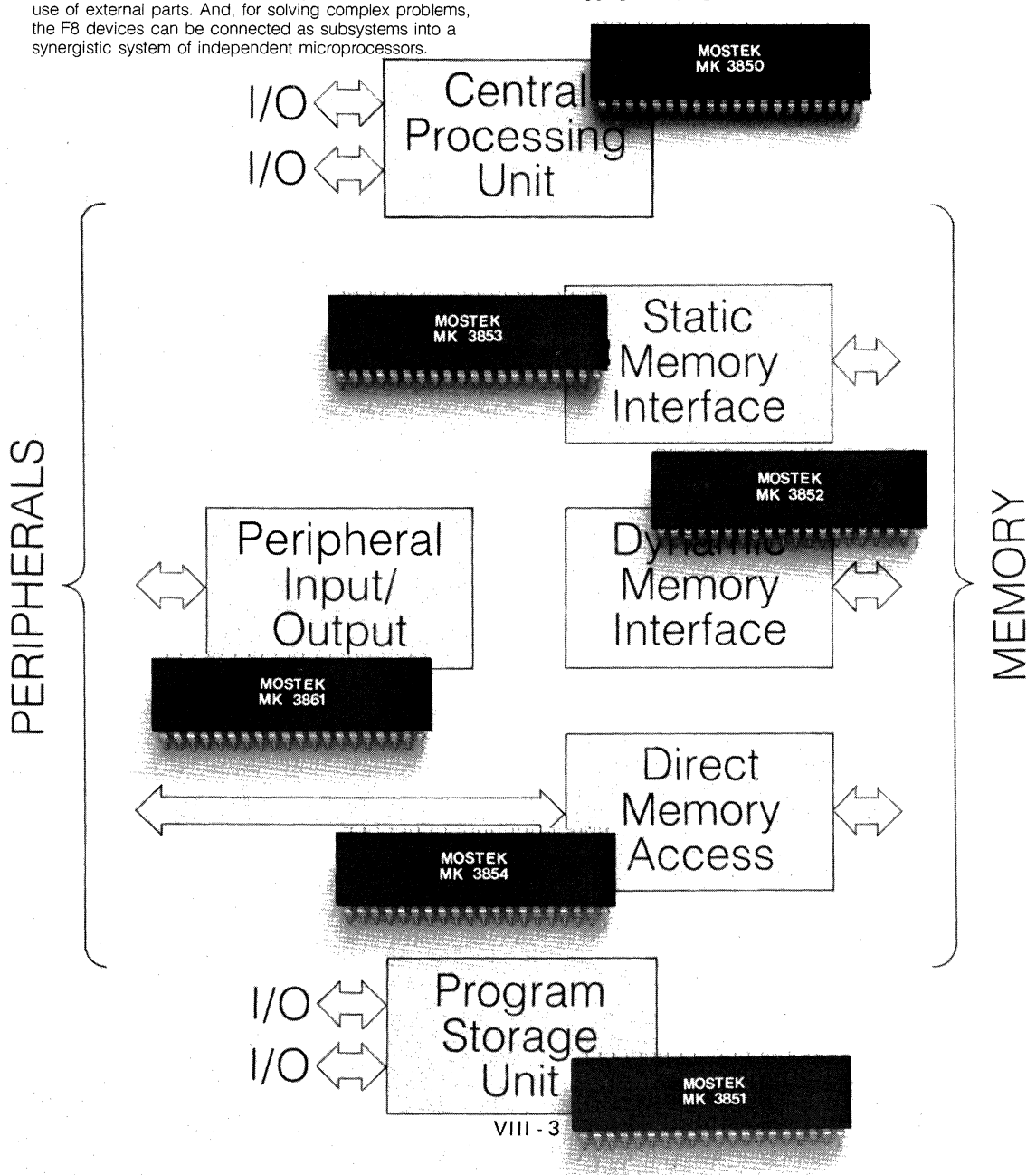
The versatile F8 Microcomputer. With low power requirements and delivered in plastic.

The F8 microprocessor from MOSTEK offers important advantages in system efficiency, system cost and versatility. Here's the F8 concept . . .

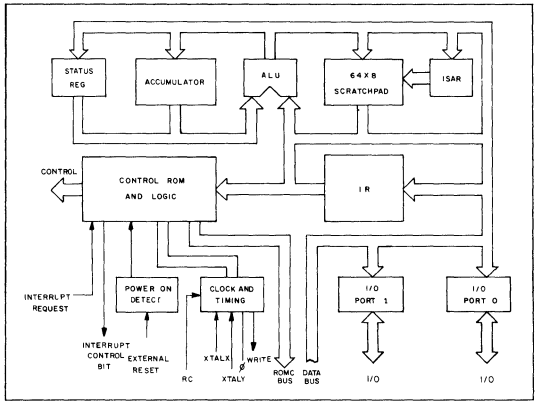
Unique partitioning of the system functions have been divided among the various circuits of the F8 family to provide sophisticated modularity. As a result, it is now possible to build a minimum microprocessor system with *only one device*. PSU, RAM and 1/O devices can be added to this system to form medium-size or memory-intensive systems with a minimum use of external parts. And, for solving complex problems, the F8 devices can be connected as subsystems into a synergistic system of independent microprocessors.

With the I/O structure incorporated on the chips, the majority (95%) of the peripheral devices can be directly controlled without the need for special circuits. This is accomplished by accommodating the characteristics of a given peripheral device in the software. The I/O hardware structure includes a programmable timer, an efficient interrupt system and bidirectional I/O ports.

Support software and hardware for generating and debugging microprograms is also available from Mostek.



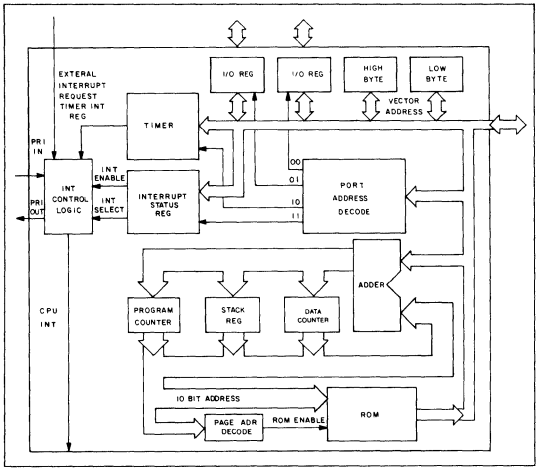
MK 3850 Central Processing Unit



FEATURES:

- Complete 8-bit central processing unit.
- 64 bytes of scratchpad RAM memory included on the F8 CPU eliminates the need for external RAM circuits in many applications.
- Clock and power-on-reset circuitry, normally requiring additional integrated circuit packages, are included on-chip.
- Contains 16 bits of fully bidirectional input/output lines internally latched (for storing output data) and capable of driving a standard TTL load.

MK 3851 Program Storage Unit

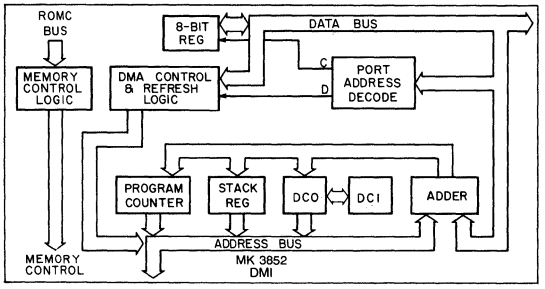


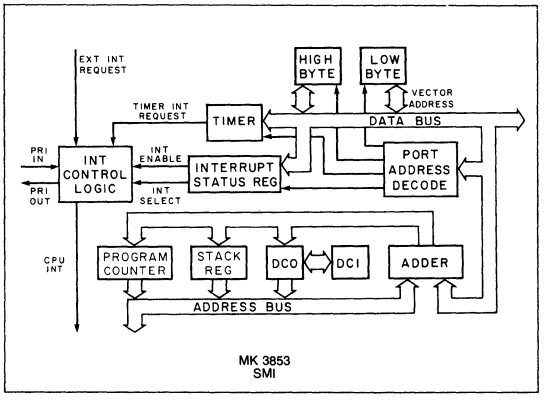
FEATURES:

- Contains 1024 bytes of mask programmable ROM for program and constant storage.
- Includes the addressing logic for memory referencing, a Program Counter, an Indirect Address Register (the Data Counter) and a Stack Register.
- Complete vectored interrupt level, including an external interrupt line to alert the central processor.
- The 8-bit Programmable Timer is especially useful for generating real time delays.
- An additional 16 bits of TTL compatible, bidirectional, fully latched I/O lines.

(Systems requiring more program storage may be expanded by adding more PSU circuits. For example, one F8 CPU and three F8 PSUs will produce a microprocessor system complete with 64 bytes of RAM, 3072 bytes of ROM, 64 I/O bits, three interrupt levels, and three programmable timers. This complete system will require only four IC packages.)

MK 3852/MK 3853 Memory Interface

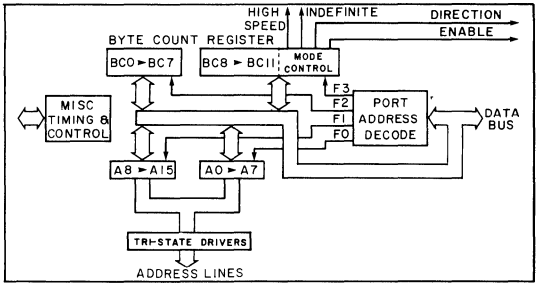




For applications requiring more than the 64 byte RAM located on the CPU, two memory interface circuits are included in the F8 set. Each device generates the 16 address lines and the signals necessary to interface with up to 65K bytes of RAM, PROM or ROM memory. Either device may be used in conjunction with standard static semiconductor memory devices.

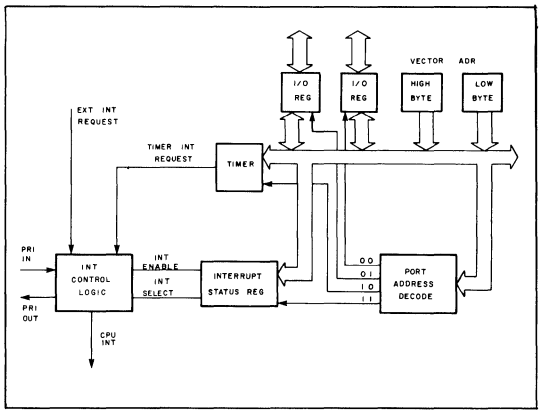
The Static Memory Interface (SMI) contains a full level of interrupt capability with a programmable interrupt vector and a programmable timer. The Dynamic Memory Interface (DMI) contains all of the logic necessary to refresh MOS dynamic memories without degrading the system throughput time. The F8 DMI can also interface with static memories when desired.

MK 3854
Direct Memory Access



MOSTEK's Direct Memory Access (DMA) device sets up a high speed data path to link F8 memory with peripheral electronics. The F8 DMA circuit, when working in conjunction with the F8 DMI, does not require overhead electronics to keep track of memory addresses, bytes transferred and handshaking signals. The data transfer is initiated by the CPU under program control. Once started, the DMA transfer will continue without CPU intervention. The CPU can sense the enable line of the DMA to determine the completion of a transfer. The DMA transfer is totally transparent to the CPU so processing throughout is not degraded.

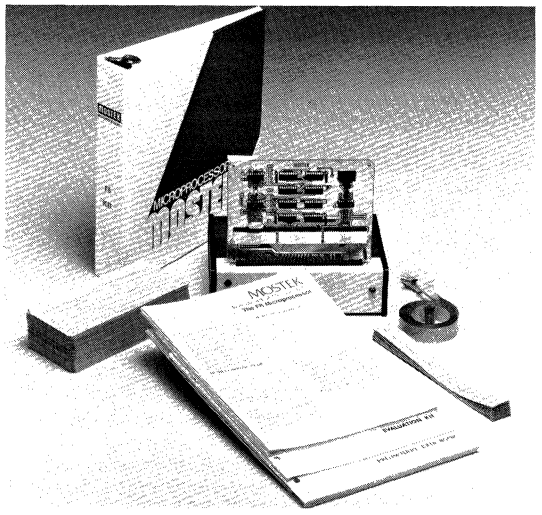
MK 3861
Peripheral Input / Output



The Peripheral I/O circuit (PIO) can be used to provide 16 bidirectional ports, an extra timer, and an extra vectored interrupt. The port address and interrupt address are preset on the PIO. Several versions with varying combinations of port and interrupt addresses are available.

Because the I/O, timer, and interrupt functions of the PIO are identical to those of the PSU, a PIO can also be used in conjunction with an MI (Memory Interface) and PROM to emulate a PSU. The MI-PROM emulates the memory function with the PIO emulating the I/O, timer and interrupt functions of a PSU.

F8 Development Systems



The Mostek Computer Kit (79002) MCK-50/70

The Mostek F8 Computer Kit contains the following parts: F8 CPU, Program Storage Unit (PSU), Static Memory Interface (SMI), 1K x 8 of random access memory, 2.0 MHz crystal, two CMOS buffers, and a 6.75" x 5.5" printed circuit board.

After assembly you then have a basic F8 evaluation/ development microcomputer with these features:

- 24 bits of I/O arranged in three 8 bit ports
- Full duplex TTY Interface (20 mA loop)
- Crystal control clock
- Automatic power on reset
- Hardware reset
- 1024 bytes of Random Access Memory
- Non-volatile operating system in PSU firmware called Designer Development Tool 1 (DDT-1)

To operate, you simply attach a 110 or 300 BAUD ASCII terminal (such as a teletype or CRT monitor system) and +5 and + 12 Vdc power supplies. Using DDT-1, you can load, debug, and modify your own software in the 1K byte of RAM provided in the kit.

DDT-1 provides these features that can be accessed from the ASCII terminal to write and execute your own software.

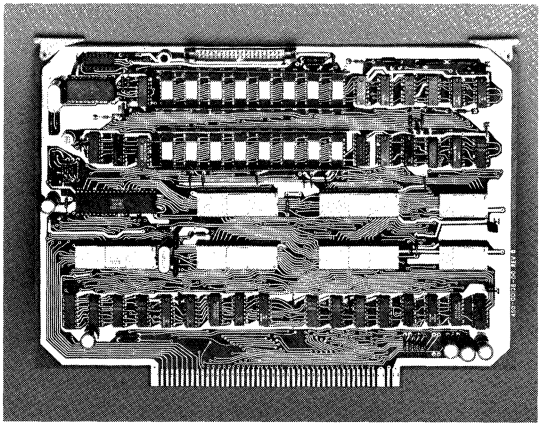
- Load command — loads memory from paper tape
- Dump command — formats data and output to paper tape punch
- Type command — examines blocks of memory
- Copy command — moves blocks of memory from one location to another
- Memory Display and Modify Command — examines and modifies memory one byte at a time
- Port commands — displays and modifies the 24 I/O lines
- Hexadecimal arithmetic commands — performs Hexidecimal arithmetic
- Execute command — directs program execution to a specific location.
- Breakpoint command — debugs users software

The Mostek F8 Computer Kit comes with complete documentation including a detailed application note, programming guide, a listing of the DDT-1 program, and Fortran IV cross assembler.

The Mostek F8 Computer Kit is available in kit form (79001) or as an assembled and tested unit (79002). A power supply box MPS-50/70 (MK 79003) that provides an edge card connector, all necessary power, switch selectable BAUD rate and a TTY cable is also available.

Software Available for the F8

- Resident Assembler
- Resident Text Editor
- Fortran IV Cross Assembler
- Designer's Debugging Tool 1 (DDT-1 included in the MCK-50/70)
- Designer's Debugging Tool 2 (DDT-2 included with the Software Development Board SDB-50/70)

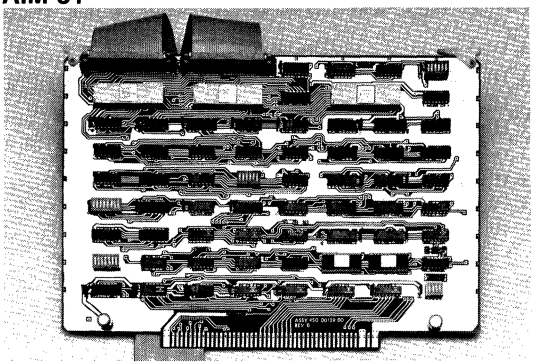


Software Development Board (79019) SDB-50/70

The Software Development Board is a complete F8 Microprocessor System designed to aid in developing software for the F8. When combined with power supply, card cage and an ASCII terminal (such as a teletype), it will enable the user to develop the software for all types of F8 applications. This not only includes the ability to execute and debug user software, but also the ability to create and edit "source" listings (using the resident text editor) and assemble them into corresponding "object" code (using the resident assembler). Its other features include 8K x 8 of RAM (expandable with additional memory boards), a variable speed ASCII interface, and resident console and debugging routines. The SDB-50/70 also includes an interface to an optional high speed paper tape reader/punch. Other peripherals such as a card reader and line printer may be added using an Auxiliary Interface Board.

The SDB-50/70 may be used in two ways. As a stand-alone microcomputer, the SDB-50/70 may be utilized to generate (edit and assemble) and debug F8 Software using the 8K bytes of RAM and 32 bits of I/O available on the board. In many F8 applications the SDB-50/70 will thus provide all the development capability the user will require. Other users, however, may prefer to emulate their application software in the circuit configuration required for their final system. This procedure can significantly reduce the development time for many types of applications. To support these users, an option is available for the SDB-50/70 called AIM (Application Interface Module). With AIM, the user may apply all of the debug capabilities of the SDB-50/70 operating system (DDT-2) directly to his final application configuration. This is accomplished without any modifications to the hardware, software or mechanical packaging of the user's final system.

Application Interface Module (79017) AIM-51

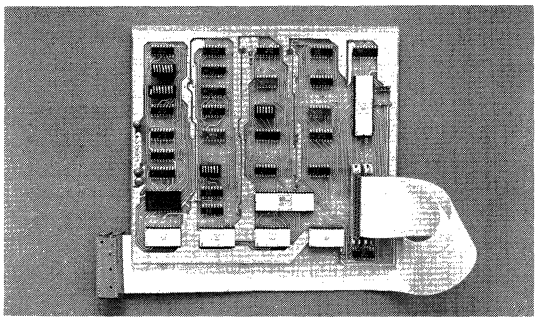


AIM-51 (Application Interface Module) is a unique development aid for debugging F8 applications in the actual hardware and software configuration of the user's final system (referred to as the 'Target'). To accomplish this, it is first necessary to emulate the Target ROM (or PROM) with RAM. This RAM must appear as ROM (or PROM) to the application while retaining the ability to be loaded, debugged and modified using peripherals independent from the Target. It is the purpose of AIM-51, used in conjunction with the Mostek Software Development Board 50/70, to provide these capabilities. With AIM-51, all of the peripheral and debugging capabilities of the SDB-50/70 may be applied directly to either the prototype or final production configuration of virtually any F8 application. No modifications to the user's hardware, software or mechanical packaging are required.

The Target may utilize either field programmable PROM or mask ROM memories. Also, since the Target can be a production version of the user's application, product revisions and enhancements may be easily implemented.

The AIM-51 Board is usually mounted in a card cage with the Software Development Board 50/70. It is the purpose of the SDB-50/70 to supply the user with the means for accessing and controlling the target system (via the AIM-51 Board) during the program development phase. This provides access to all the development software and peripherals of the SDB-50/70 without having to introduce any perturbations to the target system environment. AIM-51 does not affect the peripheral expansion capabilities of the SDB-50/70.

In microprocessor applications where the anticipated system volume is insufficient to justify the tooling charges associated with ROM, field programmable PROM may be used instead. Software for this type of system may be easily developed by using AIM-51 to emulate the PROM memory and MK 3861 PIO features of the final system. One AIM-51 Board will emulate up to 1024 bytes of PROM- and one MK 3861 PIO.



EMULATOR-51

The Emulator from Mostek (79018) EMU-51

The EMU-51 is a development aid for designing and field testing F8 microprocessor systems which utilize one or more MK 3851 program storage unit (PSU) chips. The EMU-51 is electrically equivalent to the PSU but is field programmable instead of mask programmabie. This enables a user to obtain final hardware verification of all PSU programming prior to ordering custom PSU chips. Also, since the EMU-51 even "plugs in" like a PSU chip (via a male, 40-pin connector on the end of an "umbilical cord"), prototype systems can be converted to final production status by simply unplugging the Emulator-51 and plugging in the corresponding custom PSU(s).

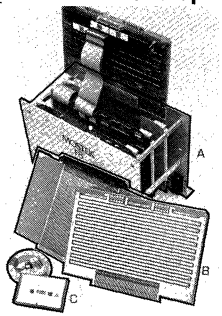
The MK 3851 is a 40-pin integrated circuit that provides 1K bytes of ROM, two 8-bit latched I/O ports, a software programmable timer and interrupt circuitry for vectored addressing and priority control. Multiple MK 3851 PSU chips can be used in a single system, providing up to 1024 bits of I/O, 64 timers, 64K bytes of ROM, and 64 interrupts.

The EMU-51 performs all the functions of the PSU — ROM, input/output ports, interrupt vector and timer.

The ROM section of the EMU-51 uses either four 256 x 8 bit ultraviolet erasable PROMs or a single 1K x 8 bit ultra-violet erasable PROM to provide non-volatile storage of the users' program. The PROM(s) should be programmed using a PROM programmer and then installed on the EMU-51. The six ROM address select switches can then be used to establish the location of the PROM in the system memory map.

Input/output ports on the EMU-51 are implemented using an actual PSU. Six I/O port address assignment switches on the EMU-51 allow the user to select the I/O port address desired for each EMU-51.

Software Development Accessories



Several accessories are available for the Software Development Board (SDB). The items shown are:

A. MK 79028 Universal Card Cage (XAID-102)

The card cage has a prewired connector assembly with power supplies bussed and a terminal strip for ease of power supply connection. The card cage will accept 3 "SDB size" cards. As shown a typical system would include an SDB, AIM and a wirewrap card for prototyping plugged into an extender card for user accessibility.

B. 79023 Wirewrap Card (XAID-103) 79024 Extender Card (XAID-104)

The wirewrap card is used for both prototyping new F8 systems and for adding peripheral interfaces and memory expansion for the SDB.

The extender card enables any card in the system to be made readily accessible to the user.

C. MK 79027 Silent 700 Accessory Package.

This package is used with the SDB to interface a Silent 700 with dual digital cassettes. The package contains a cable for the hardware interface, a digital cassette with software drivers for the silent 700 and the text editor. Instructions are included for operation.

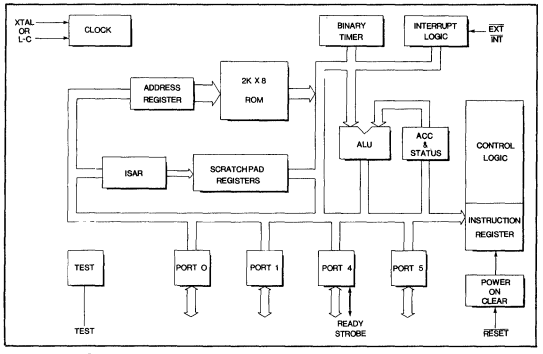
D. MK 79026 F8 Paper Tape Reader/Punch Cable Assembly. (XAID-703)

This item is not shown but is a 40-pin 3M type connector with 10 feet of flat cable. The connector mates with the parallel I/O port on the SDB.

The economical 3870. A complete system on a single chip.

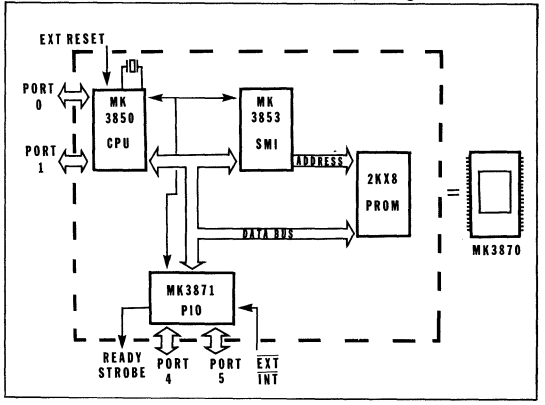
Now it is possible to build a minimum microprocessor system with only one device and still maintain upward expansion capability. This results in lower costs, fewer components and lower power. Mostek's new MK 3870 is the first single-chip microprocessor to have full software compatibility with a multichip microprocessor family, providing complete user flexibility for product enhancement. This compatibility allows new or existing systems implemented with 2Kx8 of ROM, 64x8 scratchpad RAM and four 8-bit I/O ports to be implemented with the MK 3870.

MK 3870
Single Chip F8

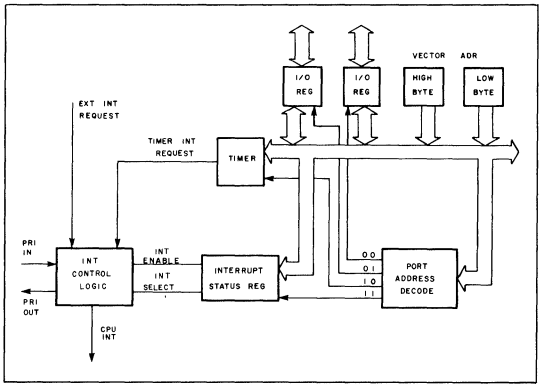


FEATURES:

- Software compatible with existing F8 family
- Single +5 volt ±10% power supply
- 2Kx8 mask programmable ROM
- 64x8 scratchpad RAM
- 32 bits (4 ports) bidirectional TTL compatible I/O
- Ready strobe provides handshake capability with Port 4
- Binary readable timer
  - Modulo "N"
  - Pulse width measurement
  - Event counter
  - Software selectable prescaler
- Vectored interrupts (4 modes)
  - External
  - Internal
  - External and internal
  - Interrupts disabled
- Versatile single phase clocks 4MHz
  - R-C
  - L-C
  - Crystal (standard 3.58 MHz may be used)
  - Internal time base (no external components)
- Low Power (Typ 300 mW)
- Standard 40-pin plastic or ceramic package



MK 3871
Peripheral Input/Output



The Peripheral I/O circuit (PIO) can be used to provide 16 bidirectional ports, an extra timer, and an extra vectored interrupt. The port address and interrupt address are preset on the PIO. Several versions with varying combinations of port and interrupt addresses are available.

Because the I/O, timer, and interrupt functions of the PIO are identical to those of the MK 3870, a PIO can also be used in conjunction with an MI and PROM to emulate an MK 3870. The MI-PROM emulates the memory function with the PIO emulating the I/O, timer and interrupt functions of an MK 3870.

Application Interface Module AIM-70 (79031)

AIM-70 is a development aid for debugging 3870 applications, similar to AIM-51. Refer to AIM-51 description for additional details of AIM-70 operation.

MK 3870 Emulator (79030)
EMU-70

The EMU-70 is a development aid for designing and field testing applications using the MK 3870 F8 compatible single chip microcomputer.

The EMU-70 is an electrical equivalent of the MK 3870 implemented with an MK 3850, MK 3853, MK 3871, two 1Kx8 UV erasable PROMs, and some additional components. The emulator allows the user to prototype, debug and field test MK 3870 systems with UV erasable PROMs. The emulator plugs into the same 40-pin socket where the MK 3870 will be in production. This system provides the user the capability of verifying his system in a field environment prior to committing to a mask programmable MK 3870.

The High Performance Z80 Microcomputer. With 8080A software compatibility and expanded system features.*

Increased system performance over the 8080A.

The Z80 outperforms the 8080A by providing more than 50% additional processor throughput with 25% to 50% less program storage space. This is accomplished using the expanded Z80 instruction set which includes all of the 78 instructions of the 8080A plus 80 additional instructions. Plus, there are 9 additional internal registers (including two 16-bit index registers) and special control circuitry for extremely fast interrupt servicing.

Reduced memory interfacing costs over the 8080A.

The Z80 CPU provides all refresh and timing signals to directly drive dynamic memories so that the Z80 LSI components can interface to standard 4K dynamic memories with minimum external logic.

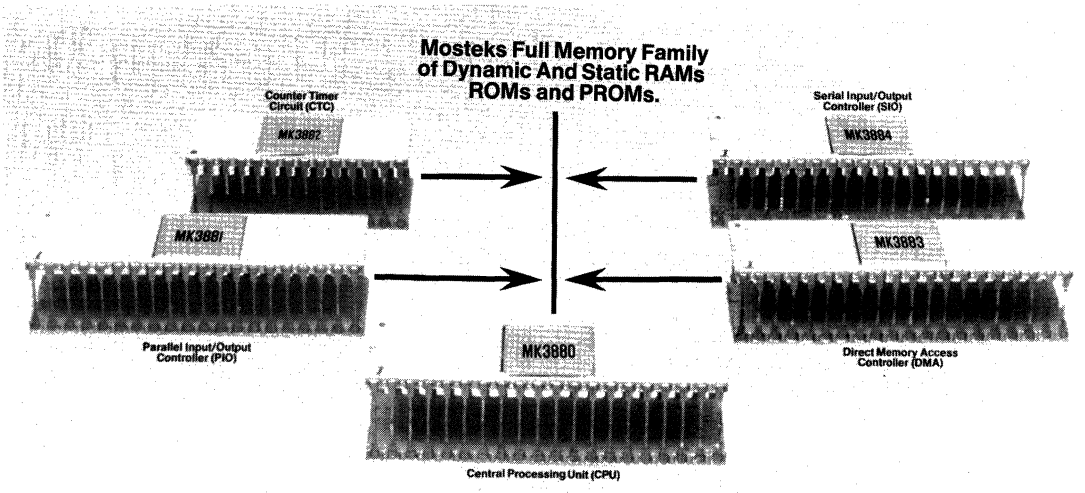
Reduced I/O costs over the 8080A.

To reduce I/O costs the Z80 LSI component set includes four general purpose programmable I/O circuits containing all of the logic required to implement fast I/O transfers with minimal CPU overhead.

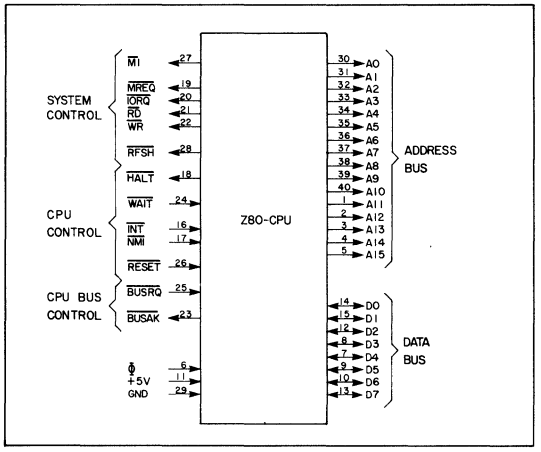
Reduced support circuitry costs over the 8080A.

All Z80 devices require a single +5 volt power supply and a single-phase TTL clock. All control signals are directly compatible with I/O and memory devices so that system control circuits are not required. External interrupt control and prioritization circuits are unnecessary since these are included in each Z80 I/O circuit. DMA circuits are usually not required due to an extremely fast interrupt response and powerful I/O block transfer capability within the CPU.

***Licensed second source to the Z80 from Zilog.**



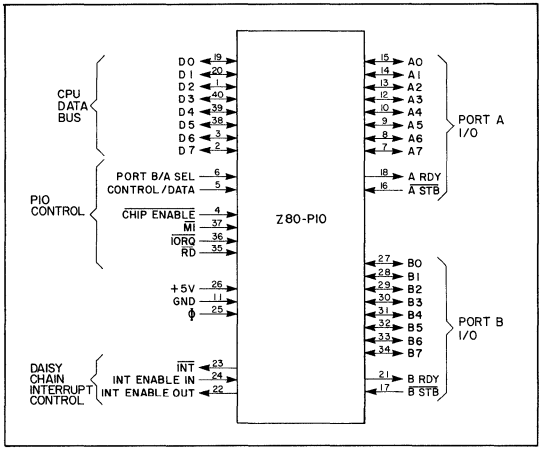
MK 3880
Central Processing Unit (CPU)



FEATURES:

- Single chip, N-channel Silicon-Gate Depletion-Load Technology in 40-pin DIP.
- 158 instructions — Includes all 78 of the 8080A instructions with total software compatibility. New instructions include 4-, 8- and 16-bit operations.
- 22 internal registers (more than twice the 8080A registers), including two 16-bit index registers.
- Three modes of fast interrupt response plus a non-maskable interrupt.
- Directly interfaces with standard static or dynamic memories with minimum external logic.
- 1.6μs instruction execution speed.
- Single 5V supply.
- Single-phase TTL-level clock.
- Requires 25% to 50% less memory space than the 8080A CPU.
- Over 50% more throughput than the 8080A.
- TTL compatible tri-state data and address busses.
- 10 addressing modes, including indexed and relative.
- Memory to memory block transfer and search instructions.
- Bit manipulation and testing in any register or memory location.
- Special I/O instructions, including I/O block transfer.
- Expanded 16-bit arithmetic capability.
- Expanded BCD arithmetic instructions.

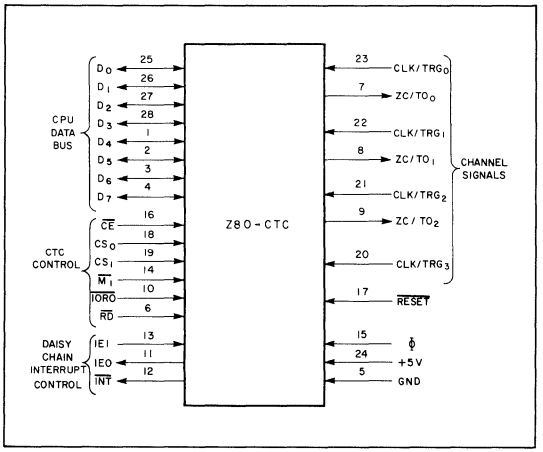
MK 3881
Parallel Input/Output Controller (PIO)



FEATURES:

- N-channel Silicon-Gate Depletion-Load Technology in 40-pin DIP.
- Two independent 8-bit ports with handshake (interrupt driven).
- Four modes of operation under program control: byte input, byte output, byte bidirectional and bit control.
- Daisy chain priority interrupt logic with programmable interrupt vectoring.
- Easy control for peripherals with a parallel interface such as line printers, paper tape reader/punches, card readers, keyboards, and displays.
- Single 5 volt supply

MK 3882
Counter Timer Circuit (CTC)



FEATURES:

- N-channel Silicon-Gate Depletion-Load Technology in 28 pin DIP.
- Single 5 volt supply.
- Single-phase TTL-level clock.
- Four independent programmable 8-bit counter/16-bit timer channels with selectable counter or timer mode.
- Readable down counters.
- Selectable 16 or 256 clock prescaler for each timer channel for resolution of 64μs to 32ms.
- Selective positive or negative trigger for counter operation.
- Capable of driving Darlington transistors.
- Daisy chain priority interrupt logic with programmable interrupt vectoring.
- All inputs and outputs are fully TTL compatible.

MK 3883
Direct Memory Access Controller (DMA)

FEATURES:

- N-Channel Silicon-Gate Depletion-Load Technology in 40-pin DIP.
- Handles bidirectional data transfers between main memory and Z80 peripherals.
- Four modes of transfer selectable: no cycle steal, byte at a time, burst, continuous.
- 1.2M byte/sec data handling rate.
- Channel status on program request.
- Two modes of operation: transfer data or search data.
- Daisy chain priority logic with programmable interrupt vectoring.
- Single 5 volt supply

MK 3884
Serial Input/Output Controller (SIO)

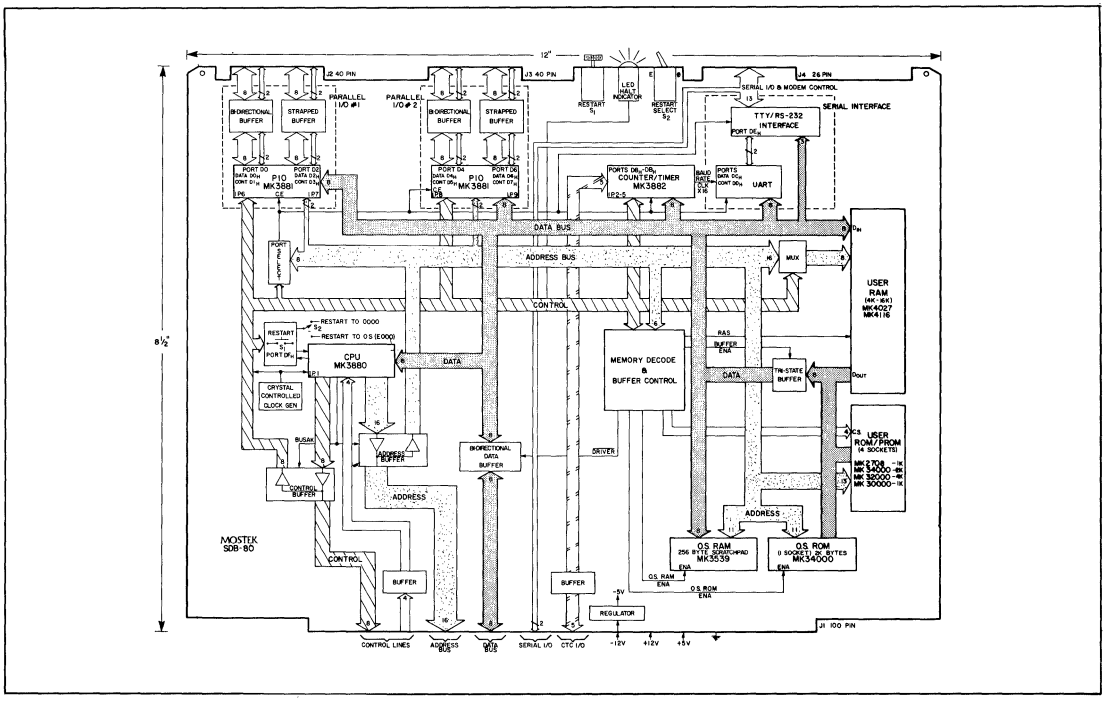
FEATURES:

- N-channel Silicon-Gate Depletion-Load Technology.
- Designed to handle peripherals with serial data interface requirements, both synchronous and asynchronous.
- Capable of full duplex serial I/O channel operation.
- Asynchronous with 5 to 8-bit data.
- Synchronous with IBM BiSync and SDLC compatibility.
- Parity checking included.
- Daisy chain priority interrupt logic with programmable interrupt vectoring.

Z80 Support Software

- XMDS-80 8080 BASED X-ASSEMBLER
- XFOR-80 FORTRAN IV BASED X-ASSEMBLER
- ASMB-80 RESIDENT Z80 ASSEMBLER
- EDIT-80 RESIDENT Z80 TEXT EDITOR
- DDT-80 RESIDENT Z80 OPERATING SYSTEM WITH DEBUG PACKAGE

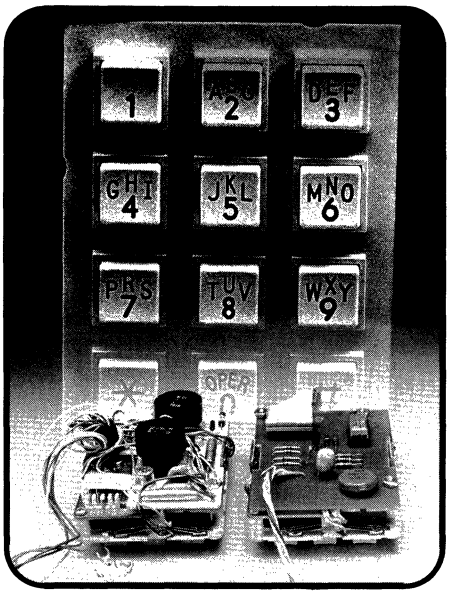
Z80 Based Development and OEM Board (78101)
SDB-80



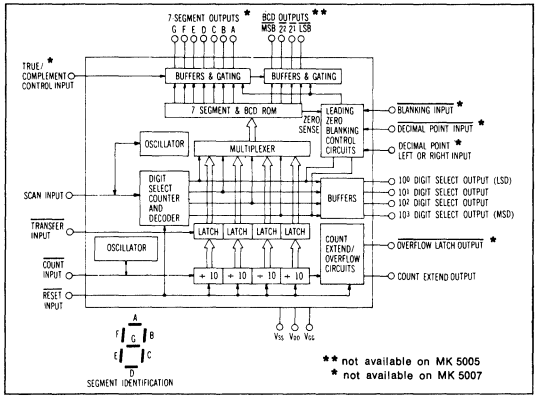
FEATURES:

- 4K RAM bytes (MK4027) expandable to 16K bytes (MK4116) on board
- System memory capability — expandable up to 65K bytes
- Versatile memory mapping — memory can be placed in any of 16-4K blocks
- ROM/PROM — 5 sockets available for up to 20K bytes of ROM
- I/O — 4 parallel ports (8 bits x 4) with handshaking (2 lines x4) capability (2 ports are bidirectional)
- I/O — 1 serial port that accepts asynchronous data (UART)
- I/O — system is expandable up to 256 parallel ports
- Ports interface directly to TTY, RS-232 (silent 700), Mostek's CRT board, paper tape reader/punch, and line printer (drivers exist in O.S.)
- BAUD rate generator on card
- Crystal controlled clock generator
- 3 software controlled digital delay/counter circuits are available to the user
- All MOS lines are TTL buffered or protected
- Data, address, and control bus lines are available for system expansion
- Card size is 12" x 8½"
- Interrupt capability from 9 sources
- Operating system available in 2K bytes of ROM (1-MK 34000)
- O.S. uses separate 256 byte scratch memory so all of the main memory user RAM is free
- Text editor available in 2K bytes of ROM (1-MK 34000)
- Resident Assembler available in 4K bytes of ROM (2-MK 34000)

INDUSTRIAL



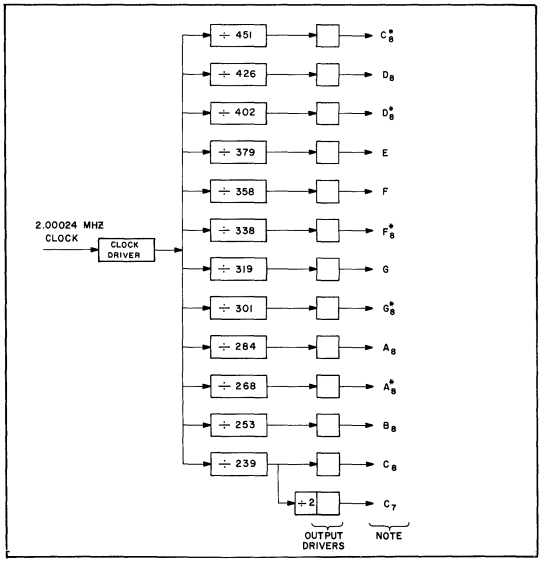
MK 5002P MK 5005P MK 5007P
MK 5002N MK 5005N MK 5007N
4-Digit Counter/Display Decoder



FEATURES:

- Ion-implanted for TTL/DTL compatibility
- Single +5V operation Low power (25 mW)
- On-chip oscillators for scan control and for counter input time base
- MK 5002P/N provides 7-segment and BCD outputs in a 28-pin dual-in-line package
- MK 5005 P/N provides 7-segment outputs in a 24-pin dual-in-line package
- MK 5007 P/N provides BCD outputs in a 16-pin dual-in-line package. Blanking Decimals, and Complement controls excluded

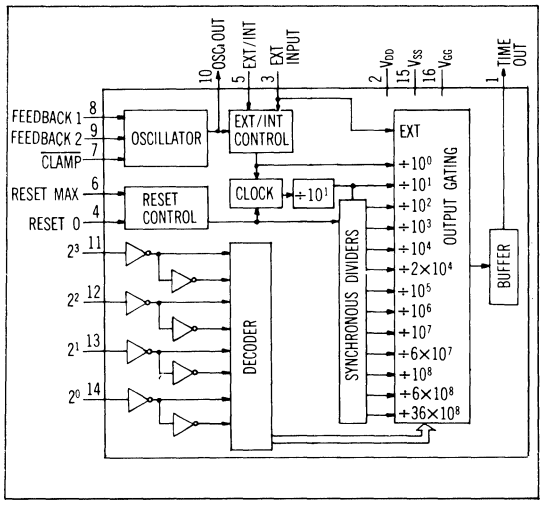
MK 50240P Series / MK 50240N Series
Top Octave Frequency Generator



FEATURES:

- Single Power supply
- Broad supply voltage operating range
- Low power dissipation
- High output drive capability
- MK 50240 — 50% Output Duty Cycle
- MK 50241 — 30% Output Duty Cycle
- MK 50242 — 50% Output Duty Cycle

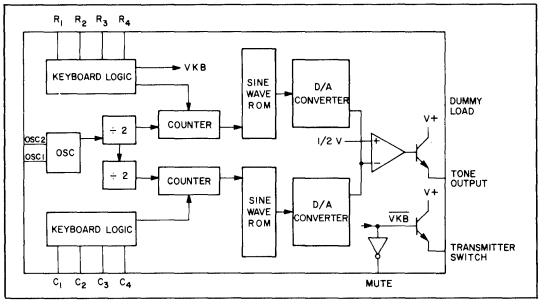
MK 5009P / MK 5009N
Counter Time Base Circuit



FEATURES:

- Ion-implanted for full TTL/DTL compatibility
- Internal clock operates from:
  External signal
  External RC network
  External crystal
- Operates DC to above 1 MHz
- Binary encoded for frequency selection

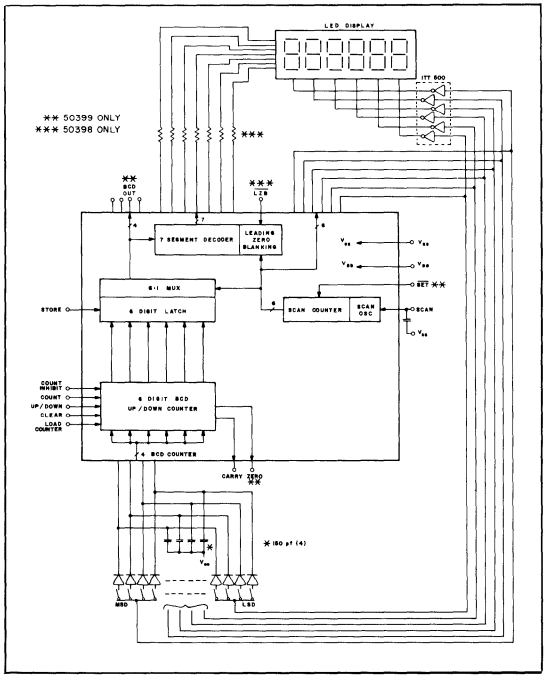
MK 5085N / MK 5086N
Integrated Tone Dialer



FEATURES

- Direct telephone line operation with no external power supply
- Requires minimal telephone line tone interfacing
- High Accuracy tones
- Digital divider logic, resistive ladder network and CMOS operational amplifier on single chip
- Uses inexpensive 3.579 MHz crystal
- Wide DC supply Voltage range
- Invalid key entry can result in either single tone or no tone
- MK 5085 designed for use with calculator type (Class A contact) keyboards
- MK 5086 designed for use in applications requiring minimal electronic interfacing
- Both parts will work in existing telephone keypads
- May use high impedance keyboard switches
- Telephone common functions on chip

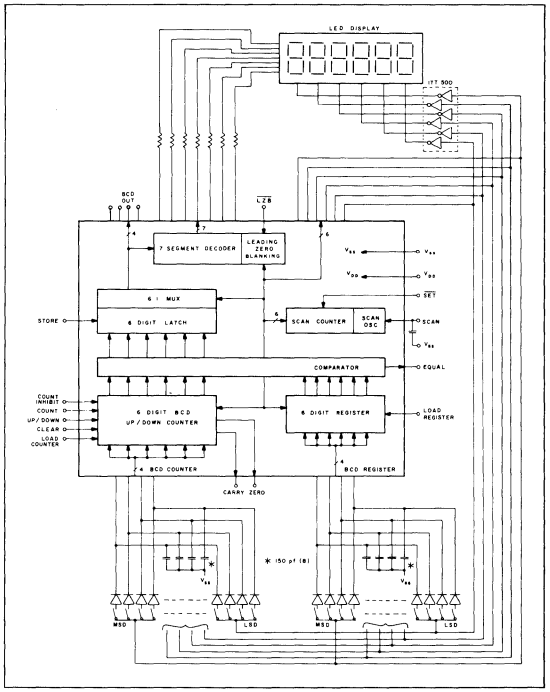
MK50398N/MK50399N
Six-Decade Counter/Display Decoder



FEATURES:

- 28-pin dual-in-line package
- Single power supply (+10V to +15V)
- Schmitt-Trigger on the count-input
- Six decades of synchronous up/down counting
- Loadable counter
- Interfaces directly with CMOS logic
- Multiplexed BCD or seven-segment outputs

MK 50395N / MK 50396N / MK 50397N
Six-Decade Counter/Display Decoder



FEATURES:

- Single power supply
- Schmitt-Trigger on the count-input
- Six decades of synchronous up/down counting
- Look-ahead carry or borrow
- Loadable counter
- Loadable compare-register with comparator output
- Multiplexed BCD and seven-segment outputs
- Internal scan oscillator
- Direct LED segment drive
- Interfaces directly with CMOS logic
- MK 50396 programmed to count time: 99 hrs. 59 min. 59 sec.
- MK 50397 programmed to count time: 59 min., 59 sec., 99/100 sec.

Industrial circuits available soon...

MK 5098N
Integrated Pulse Dialer

FEATURES:

- Direct telephone line operation with no external power supply
- Requires minimal telephone line interfacing
- Works with both calculator type keyboard (form A contact) and standard 2 of 7 keyboard
- CMOS-Silicon gate technology with on chip bipolar transistors and zener diodes
- Uses inexpensive ceramic resonator for reference
- Wide DC supply voltage range
- BCD input option
- Pin selectable interdigit delay and make/break ratio
- Standard part in 16 pin package, re-dial option will be available in 18 pin package

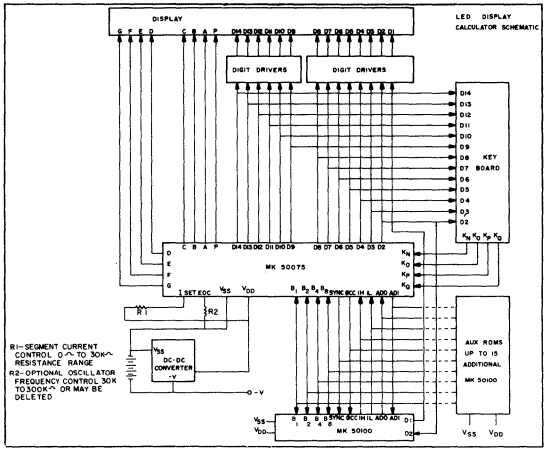
MK 5102N
Integrated Tone Receiver

FEATURES

- Detects all 16 standard DTMF digits
- Requires minimum external parts count for minimum system cost
- Uses inexpensive 3.579545 MHz crystal for reference
- Limiting is done on-chip — no off chip limiting required
- Digital counter detection with period averaging insures minimum false response
- 16-pin package for high system density
- Single supply, wide voltage range
- Includes two on-chip operational amplifiers for band split or band pass
- Output in both 4-bit binary code or dual 2-bit row/column code
- Latched outputs

CONSUMER

Expandable Calculator Set
MK 50101N / MK 50102N / MK 50075N
MK 50103N / MK 50104N / MK 50075N



FEATURES:

Financial Calculator Chip Set

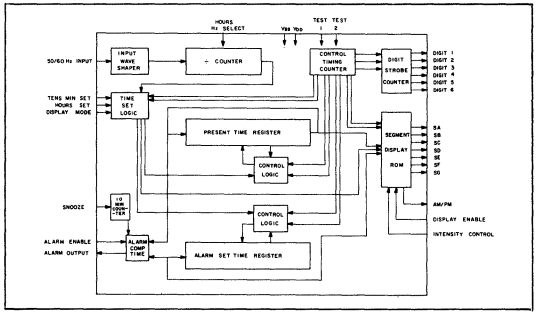
- 8 or 12 Digit Display
- 9 Memory Registers
- Gross Profit Margin
- Percentage Add On/Discount
- Financial Calculation
  - Present Value
  - Future Value
  - Interest rate (i)
  - Number of Periods (n)
  - Payment
- Floating or Fixed Point
- Algebraic Entry

FEATURES:

Scientific Calculator Chip Set

- 10 Digit Mantissa, 2 Digit Exponent
- 9 Memory Registers
- Trigonometric
- Hyperbolic
- Logarithmic
- Mean, Standard Deviation
- 8 Metric Conversion
- Percentage Calculation
- Powers and Roots
- Radian/Degrees

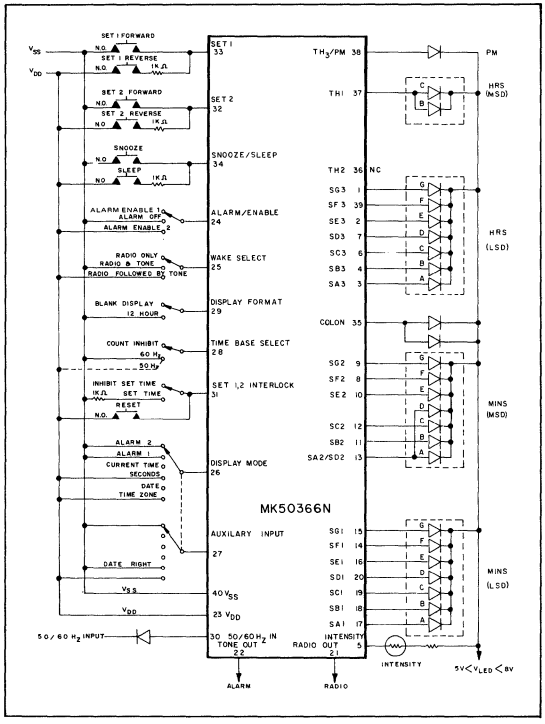
MK 50250N Series
Digital Alarm Clock



FEATURES:

- Single Voltage Power Supply
- Intensity Control
- Simple Time Setting
- 4-or 6-Digit Display
- AM/PM and Activity Indicator
- Selectable Input Frequency
- 24 hr. alarm
- Snooze Alarm
- Selectable Input Frequency and Output Mode
  - MK 50250 — 12 hr/60 Hz or 24 hr/50 Hz
  - MK 50253 — 12 hr/50 Hz or 24 hr/50 Hz
  - MK 50254 — 12 hr/60 Hz or 24 Hr/60 Hz

MK 50366N
Non-Multiplexed Clock Radio Timer



FEATURES:

- Single Chip Operation
- LED Direct Drive (10mA/Segment)
- Simple Forward or Reverse Time Setting
- Intensity Control
- 4-Digit Non-Multiplexed Display
- AM/PM and 1Hz Activity Indicator
- 12 Hr. or 24 Hr. Display Format
- 50Hz or 60Hz
- 24 Hr. Alarm
- Three Function Wake Select (Radio, Tone, Radio, Radio Followed by Tone in 8 Minutes)
- Variable Sleep (1 to 59 Minutes)
- Count Inhibit
- Seconds Display
- Brown-out Indication
- Leading Zero Suppression For Tens of Hours
- Four Year Calendar
- Month Date or Date Month Format
- One Time Zone Register
- A Second Alarm Time
- Set 1,2 interlock prevents accidental time setting
- Alarm sequence for AM/FM radio allows demonstration of alarm action quickly

MK 50460 Series
Six Digit LCD Multifunction Watch Circuits

MK50461C

- Stopwatch or time zone function bonding option
- Displays month, date, alpha day, hours, minutes, seconds
- Stopwatch displays elapsed time or accumulated time
- 12/24 hour bonding option
- 32,768 Hz oscillator

MK 50462C

- Alarm watch with snooze capability
- Displays month, date, alpha day, hour, minutes, seconds
- 12/24 hour bonding option
- 32,768 Hz oscillator

REFERENCE

MOSTEK DIRECT REPLACEMENT GUIDE*

Manufacturer	Part No.	Description	MOSTEK Replacement
AMD	Am 1002	2x128 SSR	MK1002
	Am 1101	256x1 SRAM	MK4007
	Am 2102	1024x1 SRAM	MK4102
	Am 1702A/9702A	256x8 EPROM	MK3702/ 1702A
	Am 9208	1024x8 ROM	MK30000
	Am 9214	512x8 or 1024x4ROM	MK2600
AMI	S2181	2x128 SSR	MK1002
	S3514	512x8 ROM	MK2600
	S6831A	2048x8 ROM	MK31000
	S6831B	2048x8 ROM	MK34000
	S4006	1024x1 DRAM	MK4006
	S4008	1024x1 DRAM	MK4008
	S4096	4096x1 DRAM	MK4096
	S5232	512x8 or 1024x4 ROM	MK2500
AMS	7005	4096x1 DRAM	MK 4096
EA	EA 4800/4900	2048x8 ROM	MK28000 (unlatched outputs)
	EA 2102	1024x1 SRAM	MK4102
	EA 2308	1024x8 ROM	MK30000
	EA 4096	4096x1 DRAM	MK4096
FAIRCHILD	2102	1024x1 SRAM	MK4102
	3257	ASCII Char. Gen.	MK2302
	3514	512x8 or 1024x4 ROM	MK2600
	3850	μP CPU	MK3850
	3851	μP PSU	MK3851
	3852	μP DMI	MK3852
	3853	μP SMI	MK3853
	3854	μP DMA	MK3854
	3861	μP PIO	MK3861
	4027	4096x1 DRAM	MK4027
	4096	4096x1 DRAM	MK4096
G.I.	RA 9-1101	256x1 SRAM	MK4007
	RO-3-8316A/B	2048x8 ROM	MK31000
	RO-3-9316A/B	2048x8 ROM	MK34000
	RO-5-2240S	ASCII Char. Gen.	MK2302
INTEL	1101	256x1 SRAM	MK4007
	1702A	256x8 EPROM	MK3702/ 1702A
	2102	1024x1 SRAM	MK4102
	2102AL	1024x1 SRAM	MK4102-11/ 4102-12

Manufacturer	Part No.	Description	MOSTEK Replacement
INTEL	2104	4096x1 DRAM	MK4096
	2104A	4096x1 DRAM	MK4027
	2116	16384x1 DRAM	MK4116 (unlatched outputs)
	2308/8308	1024x8 ROM	MK30000
	2316A/8316A	2048x8 ROM	MK31000
	2316E/8316E	2048x8 ROM	MK34000
	2708/8708	1024x8 EPROM	MK2708**
INTERSIL	IM 7501/11/12	256x1 SRAM	MK4007
	IM 7552	1024x1 SRAM	MK4102
	IM 7780	4x80 DSR	MK1007
MOTOROLA	MCM 2102	1024x1 SRAM	MK4102
	MCM 6604	4096x1 DRAM	MK4096
	MCM 6616	16384x1 DRAM	MK4116
	MCM 68316E	2048x8 ROM	MK34000
NATIONAL	MM 1101	256x1 SRAM	MK4007
	MM 1702A	256x8 EPROM	MK3702/ 1702A
	MM 2102	1024x1 SRAM	MK4102
	MM 4232/5232	512x8 or 1024x4 ROM	MK2500
	MM 5257	4096x1 SRAM	MK4104
NEC	μPD 414	4096x1 DRAM	MK4096
	μPD 416	16384x1 DRAM	MK4116
RCA	MW 4104	4096x1 DRAM	MK4027
SIGNETICS	2532	4x80 DSR	MK1007
	2102/2602	1024x1 SRAM	MK4102
	2501	256x1 SRAM	MK4007
	2660	4096x1 DRAM	MK4096
SYNERTEK	SY2316A	2048x8 ROM	MK31000
	SY2316B	2048x8 ROM	MK34000
T.I.	TMS 2708	1024x8 PROM	MK2708
	TMS 3409	4x80 DSR	MK1007
	TMS 4027	4096x1DRAM	MK 4027
	TMS 4033/4035	1024x1 SRAM	MK4102
	TMS 4070	16384x1 DRAM	MK4116
	TMS 4700	1024x8 ROM	MK30000
ZILOG	Z80 CPU	μP CPU	MK3880**
	Z80 PIO	μP PIO	MK3881**
	Z80 SIO	μP SIO	MK3884**
	Z80 CTC	μP CTC	MK3882**
	Z80 DMA	μP DMA	MK3883**

* User must consult data sheet to determine proper dash (—) number required when ordering

**Available soon

MOSTEK MOS MEMORY PRODUCT GUIDE

DYNAMIC RANDOM ACCESS MEMORIES

DEVICE	ORGANIZATION	ACCESS (ns)	CYCLE (ns)	SUPPLY VOLTAGES V_{DD}	V_{CC}	V_{BB}	V_{SS}	POWER DIS (max) STNBY	ACTIVE	PACKAGE TYPE	PINS
MK 4006-6	1024 x 1	400	650	−12			+5	50	450	Ceramic	16
MK 4008-6	1024 x 1	500	900	−12			+5	50	450	Ceramic	16
MK 4200-11	4096 x 1	350	500	+12	+5	−5	0	.6	300	Cer/Plas	16
MK 4200-16	4096 x 1	300	425	+12	+5	−5	0	.6	380	Cer/Plas	16
MK 4096-11	4096 x 1	350	500	+12	+5	−5	0	24	320	Cer/Plas	16
MK 4096-16	4096 x 1	300	425	+12	+5	−5	0	24	385	Cer/Plas	16
MK 4096-6	4096 x 1	250	375	+12	+5	−5	0	24	450	Cer/Plas	16
MK 4096-85	4096 x 1	350	500	+12	+5	−5	0	32	475	Cer/−55 °C to +85 °C	16
MK 4096-86	4096 x 1	300	425	+12	+5	−5	0	32	500	Cer/−55 °C to +85 °C	16
MK 4096-77	4096 x 1	250	375	+12	+5	−5	0	32	570	Cer/−55 °C to +85 °C	16
MK 4027-4	4096 x 1	250	375	+12	+5	−5	0	27	470	Cer/Plas	16
MK 4027-3	4096 x 1	200	375	+12	+5	−5	0	27	470	Cer/Plas	16
MK 4027-2	4096 x 1	150	320	+12	+5	−5	0	27	470	Cer/Plas	16
MK 4116-4	16K x 1	250	410	+12	+5	−5	0	27	465	Ceramic	16
MK 4116-3	16K x 1	200	375**	+12	+5	−5	0	27	465	Ceramic	16
MK 4116-2	16K x 1	150	375**	+12	+5	−5	0	27	465	Ceramic	16
MKM 4096 XX	4096 x 1	***	***	+12	+5	−5	0	***	***	Mil Version	16
MKB 4096XX	4096 x 1	***	***	+12	+5	−5	0	***	***	Mil Version	16
MK 4227-4*	4096 x 1	250	320	+12	+5	−5	0	1.3 mW	470	Cer/Plas	16
MK 4227-3*	4096 x 1	200	375	+12	+5	−5	0	1.3 mW	470	Cer/Plas	16
MK 4227-2*	4096 x 1	150	375	+12	+5	−5	0	1.3 mW	470	Cer/Plas	16

STATIC RANDOM ACCESS MEMORIES

MK 4007-1	256 x 1	900	900	−9	+5			75	370	Cer/Plas	16
MK 4007-4	256 x 1	900	900	−9	+5			75	370	Higher Output Current	16
MK 4102	1024 x 1	1000	1000		+5		0		350	Plastic	16
MK 4102-1	1024 x 1	450	450		+5		0		350	Plastic	16
MK 4102-12	1024 x 1	1000	1000		+5		0		170	Plastic	16
MK 4102-11	1024 x 1	450	450		+5		0		170	Plastic	16
MK 4104	4096 x 1	200	340		+5		0	25	150	Ceramic	18
MK 4114*	1024 x 4	200	340		+5		0	25	150	Ceramic	18

ULTRAVIOLET – ERASABLE PROGRAMMABLE READ ONLY MEMORIES

MK 3702-3	256 x 8	1000	1000	−9			+5		840	Ceramic	24
MK 3702-2	256 x 8	750	750	−9			+5		840	Ceramic	24
MK 3702-1	256 x 8	550	550	−9			+5		840	Ceramic	24
MK 2708*	1024 x 8	450	450	+12	+5	−5	0		TBD	Ceramic	24

READ ONLY MEMORIES

DEVICE	ORGANIZATION	LOGIC	NUMBER BITS	ACCESS (ns)	SUPPLY VOLTAGES V_{DD}	V_{GG}	V_{BB}	V_{CC}	V_{SS}	POWER DIS (MW) MAX	PACKAGE TYPE	PINS
MK 2300	64 x 7 x 5	Static	2240	1000	0	−12			+5	750	Cer/Plas	24
MK 2400	256 x 10	Static	2560	500	0	−12			+5	850	Ceramic	24
MK 2500	512 x 8 or 1024 x 4	Static	4096	700	0	−12			+5	950	Cer/Plas	24
MK 2600	512 x 8 or 1024 x 4	Static	4096	700	0	−12			+5	950	Cer/Plas	24
MK 28000	2048 x 8 or 4096 x 4	Dynamic	16384	600		−12			+5	1000	Cer/Plas	24
MK 30000	1024 x 8	Static	8192	450				+5	0	330	Cer/Plas	24
MK 31000	2048 x 8	Static	16384	550				+5	0	300	Cer/Plas	24
MK 32000*	4096 x 8	Dynamic	32768	300				+5	0	TBD	Ceramic	24
MK 34000	2048 x 8	Static	16384	350				+5	0	330	Cer/Plas	24
MK 36000*	8192 x 8	Dynamic	65536	300				+5	0	TBD	Ceramic	24

SHIFT REGISTERS

DEVICE	ORGANIZATION	LOGIC	RECIRC	SPEED (MHz)	V_{GG}	V_{SS}	NO. CLOCKS	CLOCK SWING(V)	CLOCK CAP (max)	POWER (MIN)	PACKAGE TYPE	PINS
MK 1002	Dual 128	Static	Yes	1	−12.0	+5	1	0 to 5	10	600	Cer/Plas	16
MK 1007	Quad 80	Dynamic	Yes	2.5	−12.0	+5	1	0 to 5	6	950	Cer/Plas	16

*Available Soon/**I_{DD} specified at 375 ns cycle/***Consult applicable data sheet/TBD – To Be Determined

NOTES

NOTES

PRINTED IN USA MM 2026 Rev. A/577

MOSTEK SALES OFFICES

WEST

1215 West Crosby Road
Carrollton, Texas 75006
214/242-0444

17870 Skypark Circle
Suite 107
Irvine, Calif. 92714
714/549-0397

2025 Gateway Place
Suite 268
San Jose, Ca 95110
408/287-5080

8828 North Central Avenue
Suite 201
Phoenix, Arizona 85020
602/997-7573

CENTRAL

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