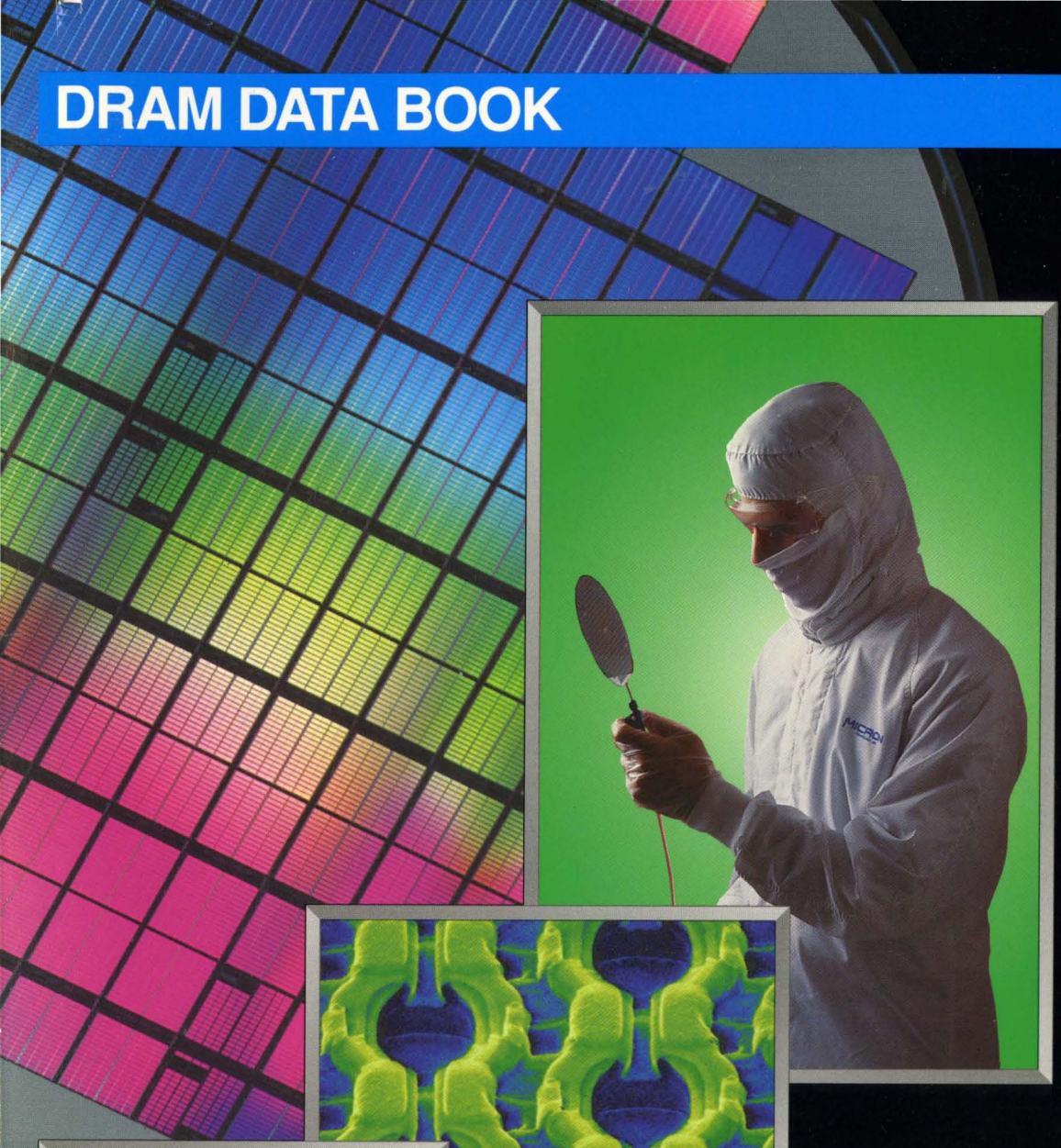
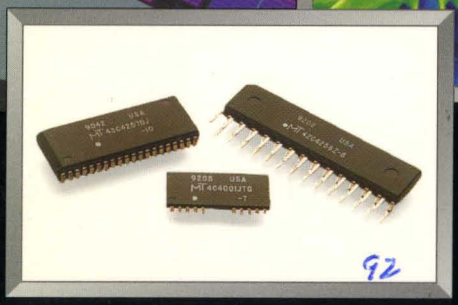
DRAM DATA BOOK





MICRON

TECHNOLOGY, INC.

MICRON TECHNOLOGY, INC.

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APPLICATION/TECHNICAL NOTES 6

PRODUCT RELIABILITY 7

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MICRON TECHNOLOGY, INC.

DRAM DATA BOOK

2805 East Columbia Road
Boise, Idaho 83706
Telephone: (208) 368-3900
FAX: (208) 368-4431
Customer Comment Line:
800-932-4992 (USA)
01-208-368-3410 (Intl.)

ABOUT THE COVER:

Front — Clockwise from left, 1) Micron's 16 Meg DRAM wafer; 2) More than 4,000 Micron team members give painstaking attention to every step of the production process; 3) Scanning electron microscope (SEM) photograph of Micron's DRAM mini-stack process; and 4) Micron's Triple Port, Dual Port and 4 Meg DRAMs in SOJ, ZIP and TSOP packages.

Back — Micron's Boise, Idaho, corporate headquarters including three fabrication facilities.

IMPORTANT NOTICE

Micron Technology, Inc., reserves the right to change products or specifications without notice. Customers are advised to obtain the latest versions of product specifications, which should be considered in evaluating a product's appropriateness for a particular use. There is no assurance that Micron's semiconductors are appropriate for any application by a customer.

MICRON TECHNOLOGY, INC., MAKES NO WARRANTIES EXPRESSED OR IMPLIED OTHER THAN COMPLIANCE WITH MICRON'S SPECIFICATION SHEET FOR THE COMPONENT AT THE TIME OF DELIVERY. ANY CLAIM AGAINST MICRON MUST BE MADE WITHIN NINETY (90) DAYS FROM THE DATE OF SHIPMENT FROM MICRON, AND MICRON HAS NO LIABILITY THEREAFTER. ANY MICRON LIABILITY IS LIMITED TO REPLACEMENT OF DEFECTIVE ITEMS OR RETURN OF AMOUNTS PAID FOR DEFECTIVE ITEMS (AT THE BUYER'S ELECTION).

MICRON'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF MICRON TECHNOLOGY, INC. AS USED HEREIN:

A. LIFE SUPPORT DEVICES OR SYSTEMS ARE DEVICES OR SYSTEMS WHICH (1) ARE INTENDED FOR SURGICAL IMPLANT INTO THE BODY, OR (2) SUPPORT OR SUSTAIN LIFE AND WHOSE FAILURE TO PERFORM WHEN PROPERLY USED IN ACCORDANCE WITH INSTRUCTIONS FOR USE PROVIDED IN THE LABELING CAN BE REASONABLY EXPECTED TO RESULT IN A SIGNIFICANT INJURY TO THE USER.

B. CRITICAL COMPONENT IS ANY COMPONENT OF A LIFE SUPPORT DEVICE OR SYSTEM WHOSE FAILURE TO PERFORM CAN BE REASONABLY EXPECTED TO CAUSE THE FAILURE OF THE LIFE SUPPORT DEVICE OR SYSTEM OR TO AFFECT ITS SAFETY OR EFFECTIVENESS.

Dear Customer:

Micron Technology, Inc., is dedicated to the design, manufacture and marketing of high quality, highly reliable memory components. Our corporate mission is

"To be a world class team developing advantages for our customers"

At Micron, we are investing time, talent and resources to bring you the finest DRAMs, SRAMs, VRAMs and other specialty memory products. We have developed a unique intelligent burn-in system, AMBYX™, which evaluates and reports the quality level of each and every component we produce.

We are dedicated to continuous improvement of all our products and services. This means continual reduction of electrical and mechanical defect levels. It also means the addition of new services such as "just-in-time" delivery and electronic data interchange programs. And, when you have a design or application question, you can get the answers you need from the source through one of Micron's applications engineers.

We're proud of our products, our progress and our performance. And we're pleased that you're choosing Micron as your memory supplier.

The Micron Team

ADVANTAGES

Micron Technology brings quality, productivity and innovation together to provide advantages for our customers. Our products feature some of the industry's fastest speeds and smallest die sizes. And we establish delivery standards based on your expectations, including JIT programs, made possible by ever-increasing product reliability.

COMPONENT INTEGRATED CIRCUITS

Micron Technology entered the memory market 14 years ago first designing, then manufacturing dynamic random access memory (DRAM). From there, we developed high-performance fast static RAM (SRAM), multiport DRAM (VRAM and Triple Port DRAM), and a variety other memory products.

As we bring progressive memory solutions to our customers, we enjoy recognition for our achievements. Micron's Triple Port DRAM was the first IC ever to incorporate a second, independent serial access port, allowing unparalleled flexibility in data manipulation. In 1990, Micron's Triple Port received the 1990 "Product of the Year" award from *Electronic Products* magazine.

SPECIALTY MEMORY PRODUCTS

Beyond our standard component memory, Micron is introducing many revolutionary products that we expect will follow the Triple Port's tradition. From FIFOs to processors, Micron continues to forge ahead into new and exciting frontiers.

We are pleased to be first to market with our compact, easy-to-install 88-pin IC DRAM Card. Ideal for laptop, notebook and other portable systems, Micron's IC DRAM Card offers both high density and low power within JEDEC and JEIDA specifications.*

MILITARY CERTIFIED PRODUCTS

As one of the few manufacturers of military-grade memory in North America, Micron is proud to provide a documented source inspection from wafer start to finished product. We've earned recognition from U.S. and European space agencies as well as Joint Army/Navy certification for both our NMOS and CMOS process technologies.

DIE SALES

In addition to our durable packaging, Micron also provides memory devices in bare die form. These are increasingly in demand for commercial and military use in highly specialized applications. Micron's bare die products are available both in 6" wafers and wafflepacks.

CUSTOM MANUFACTURING SERVICES

For total project management, Micron offers added-value services. These include both standard contract manufacturing services for system-level products including design, assembly, customer kitted assembly, comprehensive quality testing or shipping as well as complete turnkey services covering all phases of production. Our component and system-level manufacturing facilities are centrally located in Boise, Idaho, so the component products you need are readily available.

QUALITY

Without a doubt, quality is the most important thing we provide to every Micron customer with every Micron shipment. That's because we believe that quality must be internalized consistently at every level of our company. We provide every Micron team member with the training and motivation needed to make Micron's quality philosophy a reality.

One way we have measurably improved both productivity and product quality is through our own quality improvement program formed by individuals throughout the company. Micron quality teams get together to address a wide range of issues within their areas. We consistently and regularly perform a company-wide self-assessment based on the Malcolm Baldrige National Quality Award criteria. We've also implemented statistical process controls to evaluate every facet of the memory design, fabrication, assembly and shipping process. And our AMBYX™ intelligent burn-in and test system** gives Micron a unique edge in product reliability.

*See NOTE, page v.
**For more information on Micron's AMBYX™, see Section 7.

ABOUT THIS BOOK

CONTENT

The 1992 ***DRAM Data Book*** from Micron Technology provides complete specifications on all standard DRAMs and DRAM modules as well as specialty and derivative products based on our DRAM production process.

The ***DRAM Data Book*** is one of three product data books Micron currently publishes. Its two companion volumes include our ***SRAM Data Book*** and ***Military Data Book***.

SECTION ORGANIZATION

Micron's 1992 ***DRAM Data Book*** contains a detailed Table of Contents with sequential and numerical indexes of products as well as a complete product selection guide. The Data Book is organized into nine sections:

- **Sections 1–5:** Individual product families. Each contains a product selection guide followed by data sheets.
- **Section 6:** Application/technical notes.
- **Section 7:** Summary of Micron's unique quality and reliability programs and testing operation, including our AMBYX™ intelligent burn-in and test system.*
- **Section 8:** Packaging information.
- **Section 9:** Product ordering information, including a list of sales representatives and distributors worldwide.

DATA SHEET SEQUENCE

Data sheets in this book are ordered first by width and second by depth. For example, the DRAM section begins with the 1 Meg x 1 followed by 4 Meg x 1 and all other x1 configurations in order of ascending depth. Next come the x4 products, followed by x8, etc., as applicable to the specific product family.

DATA SHEET DESIGNATIONS

As detailed in the table below, each Micron product data sheet is classified as either **Advance, Preliminary** or **Final**. In addition, new product data sheets that are new additions are designated with a "New" indicator in the tab area of the front page.

SURVEY

We have included a removable, postage-paid survey form in the front of this book. Your time in completing and returning this survey will enhance our efforts to continually improve our product literature.

For more information on Micron product literature, or to order additional copies of this publication, contact

Micron Technology, Inc.
2805 East Columbia Road
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Phone: (208) 368-3900
FAX: (208) 368-4431
Customer Comment Line:
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01-208-368-3410 (Intl.)

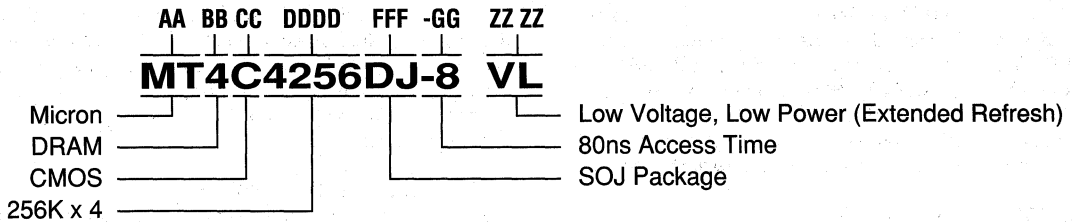
DATA SHEET DESIGNATIONS

DATA SHEET MARKING	DEFINITION
"Advance"	This data sheet contains initial descriptions of products still under development.
"Preliminary"	This data sheet contains initial characterization limits that are subject to change upon full characterization of production devices.
No Marking (Final)	This data sheet contains minimum and maximum limits specified over the complete power supply and temperature range for production devices. Although considered final, these specifications are subject to change, as further product development and data characterization sometimes occur.
"New"	This data sheet (which may be either Advance, Preliminary or Final) is a new addition to the Data Book.

NOTE: Micron's DRAM Data Book uses acronyms to refer to certain industry-standard-setting bodies. These are defined below for your reference:
EIA/JEDEC—Electronics Industry Association/Joint Electron Device Engineering Council.
JEIDA—Japanese Electronics Industry Development Association.
PCMCIA—Personal Computer Memory Card International Association.

*Micron's ***Quality/Reliability Handbook*** is available by calling (208) 368-3900.

EXPANDED COMPONENT NUMBERING SYSTEM



AA – PRODUCT LINE IDENTIFIER

Component Product	MT

BB – PRODUCT FAMILY

DRAM	4
DPDRAM	42
TPDRAM	43
SRAM	5
FIFO	52
Cache Data SRAM	56
Synchronous SRAM	58

CC – PROCESS TECHNOLOGY

CMOS	C
Low Voltage CMOS	LC

DDDD – DEVICE NUMBER

(Can be modified to indicate variations)

DRAM	Width, Density
DPDRAM	Width, Density
TPDRAM	Width, Density
SRAM	Total Bits, Width
CACHE	Density, Width
Latched SRAM	Total Bits, Width
FIFO	Width, Total Bits
Synchronous SRAM	Density, Width

E – DEVICE VERSIONS

(Alphabetic characters only; located between D and F when required)

JEDEC Test Mode (4 Meg DRAM)	J
Errata on Base Part	Q

FFF – PACKAGE CODES

PLASTIC	
DIP	Blank
DIP (Wide Body)	W
ZIP	Z
LCC	EJ
SOP/SOIC	SG

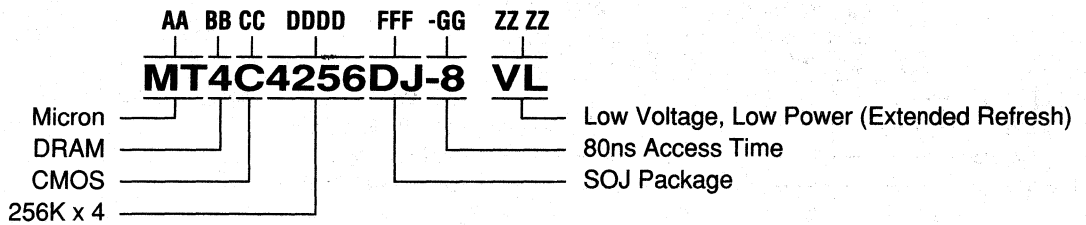
FFF – PACKAGE CODES (continued)

QFP	LG
TSOP (Type II)	TG
TSOP (Reversed)	RG
TSOP (Longer)	TL
SOJ	DJ
SOJ (Reversed)	DR
SOJ (Longer)	DL
DIE	
Die	XDC
Wafer	XWC
Military Die	XD
Military Wafer	XW
Ceramic	
DIP	C
DIP (Narrow Body)	CN
DIP (Wide Body)	CW
LCC	EC
LCC (Narrow Body)	ECN
LCC (Wide Body)	ECW
SOP/SOIC	CG
SOJ	DCJ
PGA	CA
FLAT PACK	F

GG – ACCESS TIME

-5	5ns or 50ns
-6	6ns or 60ns
-7	7ns or 70ns
-8	8ns or 80ns
-10	10ns or 100ns
-12	12ns or 120ns
-15	15ns or 150ns
-17	17ns
-20	20ns
-25	25ns
-35	35ns
-45	45ns
-50 (SRAM only)	50ns
-53	53ns

EXPANDED COMPONENT NUMBERING SYSTEM (continued)



GG – ACCESS TIME (continued)

-55 ..... 55ns
-70 (SRAM only) 70ns

ZZ ZZ – PROCESSING CODES

(Multiple processing codes are separated by a space and are listed in hierarchical order).

Example:
A DRAM supporting low power, extended refresh (L); low voltage (V) and the industrial temperature range (IT) would be indicated as:
V L IT

Interim I
Low Voltage V
DRAMS
- Low Power (Extended Refresh) L
- Low Voltage, Low Power (Extended Refresh) VL
- Low Power (Self Refresh) ..... S
- Low Voltage, Low Power (Self Refresh) ..... VS

SRAMS
- Low Volt Data Retention L
- Low Power ..... P
- Low Power, Low Volt Data Retention ..... LP
- Low Voltage, Low Power ..... VP

ZZ ZZ – PROCESSING CODES (continued)

- Low Voltage, Low Volt Data Retention VL
- Low Voltage, Low Volt Data Retention, Low Power ..... VB

EPI Wafer ..... E

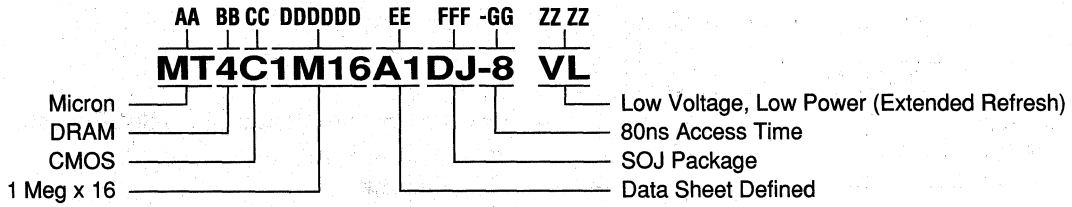
Commercial Testing
- 0°C to +70°C ..... Blank
- -40°C to +85°C ..... IT
- -40°C to +125°C ..... AT
- -55°C to +125°C ..... XT

MIL-STD-883C Testing
- -55°C to +125°C 883C
- -55°C to +110°C (DRAMs) 883C
- 0°C to +70°C M070

Special Processing
- Engineering Sample ..... ES
- Mechanical Sample ..... MS
- Sample Kit* ..... SK
- Tape and Reel* ..... TR
- Bar Code* ..... BC

* Used in device order codes; this code is not marked on device.

NEW COMPONENT NUMBERING SYSTEM



AA – PRODUCT LINE IDENTIFIER

Component Product ..... MT

BB – PRODUCT FAMILY

DRAM 4
DPDRAM 42
TPDRAM 43
Synchronous DRAM 48
SRAM 5
FIFO 52
Latched SRAM 56
Synchronous SRAM 58

CC – PROCESS TECHNOLOGY

CMOS C
Low Voltage CMOS LC

DDDDDD – DEVICE NUMBER

Depth, Width

Example:
1M16 = 1 Megabit deep by 16 bits wide = 16 Megabits of total memory

No Letter ..... Bits
K ..... Kilobits
M ..... Megabits
G ..... Gigabits

EE – DEVICE VERSIONS

(The first character is an alphabetic character only; the second character is a numeric character only.)
Specified by individual data sheet

FFF – PACKAGE CODES

Plastic
DIP ..... Blank
DIP (Wide Body) ..... W
ZIP ..... Z
LCC ..... EJ
SOP/SOIC ..... SG

FFF – PACKAGE CODES (continued)

QFP ..... LG
TSOP (Type II) ..... TG
TSOP (Reversed) ..... RG
TSOP (Longer) ..... TL
SOJ ..... DJ
SOJ (Reversed) ..... DR
SOJ (Longer) ..... DL

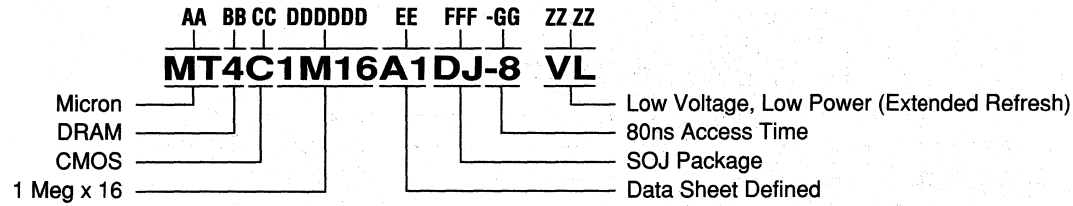
DIE
Die ..... XDC
Wafer ..... XWC
Military Die ..... XD
Military Wafer ..... XW

CERAMIC
DIP C
DIP (Narrow Body) ..... CN
DIP (Wide Body) ..... CW
LCC (Narrow Body) ..... ECN
LCC ..... EC
LCC (Wide Body) ..... ECW
SOP/SOIC ..... CG
SOJ ..... DCJ
PGA ..... CA
FLAT PACK ..... F

GG – ACCESS TIME

-5 ..... 5ns or 50ns
-6 ..... 6ns or 60ns
-7 ..... 7ns or 70ns
-8 ..... 8ns or 80ns
-10 ..... 10ns or 100ns
-12 ..... 12ns or 120ns
-15 ..... 15ns or 150ns
-17 ..... 17ns
-20 ..... 20ns
-25 ..... 25ns
-35 ..... 35ns
-45 ..... 45ns
-50 (SRAM only) 50ns

NEW COMPONENT NUMBERING SYSTEM (continued)



GG – ACCESS TIME (continued)

-53 ..... 53ns
-55 ..... 55ns
-70 (SRAM only) 70ns

ZZ ZZ – PROCESSING CODES

(Multiple processing codes are separated by a space and are listed in hierarchical order.)

Example:
A DRAM supporting low power, extended refresh (L); low voltage (V) and the industrial temperature range (IT) would be indicated as:
V L IT

Interim I
Low Voltage V
DRAMs
- Low Power (Extended Refresh) L
- Low Voltage, Low Power (Extended Refresh) VL
- Low Power (Self Refresh) ..... S
- Low Voltage, Low Power (Self Refresh) ..... VS

SRAMs
- Low Volt Data Retention L
- Low Power ..... P
- Low Power, Low Volt Data Retention ..... LP
- Low Voltage, Low Power ..... VP

ZZ ZZ – PROCESSING CODES (continued)

- Low Voltage, Low Volt Data Retention VL
- Low Voltage, Low Volt Data Retention, Low Power ..... VB

EPI Wafer ..... E

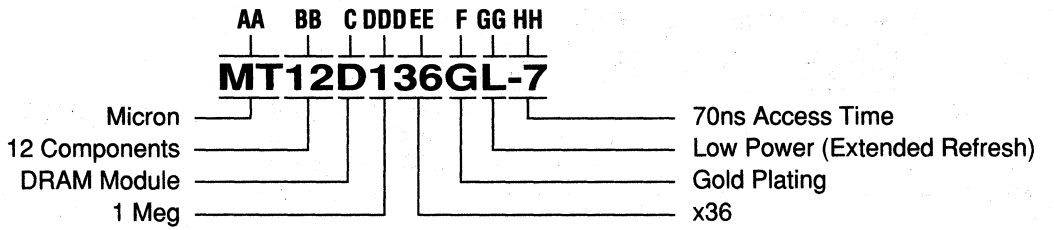
Commercial Testing
- 0°C to +70°C ..... Blank
- -40°C to +85°C ..... IT
- -40°C to +125°C ..... AT
- -55°C to +125°C ..... XT

MIL-STD-883C Testing
- -55°C to +125°C 883C
- -55°C to +110°C (DRAMs) 883C
- 0°C to +70°C M070

Special Processing
- Engineering Sample ..... ES
- Mechanical Sample ..... MS
- Sample Kit* ..... SK
- Tape and Reel* ..... TR
- Bar Code* ..... BC

* Used in device order codes; this code is not marked on device.

MODULE NUMBERING SYSTEM



AA – PRODUCT LINE IDENTIFIER
Micron Technology Component Product ..... MT

BB – NUMBER OF MEMORY COMPONENTS

C – RAM FAMILY
SRAM ..... S
DRAM ..... D

DDD – DEPTH

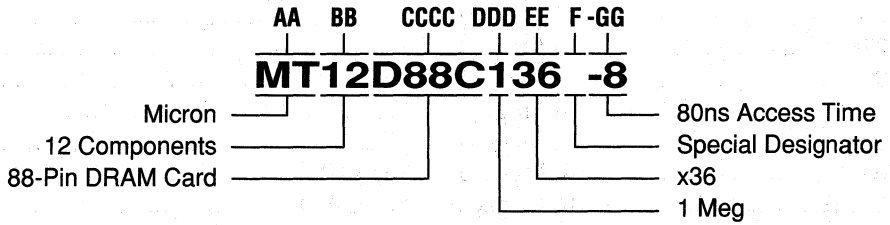
EE – WIDTH

F – PACKAGE CODE
DIP ..... D
Gold Plate ..... G
ZIP ..... Z
SIP ..... N
SIMM ..... M

GG – SPECIAL DESIGNATOR
Low Power L

HH – ACCESS TIME
-10 ..... 10ns or 100ns
-15 ..... 15ns
-20 ..... 20ns
-25 ..... 25ns
-30 ..... 30ns
-35 ..... 35ns
-45 ..... 45ns
-6 ..... 60ns
-7 ..... 70ns
-8 ..... 80ns

IC DRAM CARD NUMBERING SYSTEM



AA – PRODUCT LINE IDENTIFIER
Micron Technology Component Product ..... MT

BB – NUMBER OF MEMORY COMPONENTS

CCCC – DRAM CARD DESIGNATOR AND PIN COUNT
88-Pin DRAM Card D88C
60-Pin DRAM Card D60C

DDD – DEPTH

EE – WIDTH

F – SPECIAL DESIGNATOR
3.3 Volts V

G – ACCESS TIME
-5 ..... 50ns
-6 ..... 60ns
-7 ..... 70ns
-8 ..... 80ns

DYNAMIC RAMS

		PAGE
MT4C1024	1 Meg x 1	FP 1-1
MT4C1024 L	1 Meg x 1	FP, LP 1-13
MT4C1026	1 Meg x 1	SC 1-25
MT4C1004J	4 Meg x 1	FP 1-37
MT4C1004J L	4 Meg x 1	FP, LP 1-49
MT4C1006J	4 Meg x 1	SC 1-61
MT4C16M1A1	16 Meg x 1	FP, 4KR 1-73
MT4LC16M1A1	16 Meg x 1	FP, 4KR, LV 1-73
MT4C16M1D1	16 Meg x 1	SC, 4KR 1-85
MT4C4256	256K x 4	FP 1-87
MT4C4256 L	256K x 4	FP, LP 1-97
MT4C4256 VL	256K x 4	FP, LP, LV 1-109
MT4C4258	256K x 4	SC 1-121
MT4C4001J	1 Meg x 4	FP 1-133
MT4C4001J L	1 Meg x 4	FP, LP 1-145
MT4C4003J	1 Meg x 4	SC 1-157
MT4C4004J	1 Meg x 4	FP, QCP 1-169
MT4C4M4A1	4 Meg x 4	FP, 4KR 1-183
MT4C4M4B1	4 Meg x 4	FP, 2KR 1-183
MT4LC4M4A1	4 Meg x 4	FP, 4KR, LV 1-195
MT4LC4M4B1	4 Meg x 4	FP, 2KR, LV 1-195
MT4C4M4D1	4 Meg x 4	SC, 4KR 1-207

FP ..... FAST PAGE MODE
SC ..... STATIC COLUMN MODE
LP ..... Low Power, Extended Refresh
QCP ..... Quad CAS Parity
LV ..... Low Voltage
2KR ..... 2,048 Row Refresh
4KR ..... 4,096 Row Refresh

WIDE DRAMS

		PAGE
MT4C8512	512K x 8	FP 2-1
MT4C8513	512K x 8	FP, WPB 2-1
MT4C8512 L	512K x 8	FP, LP 2-15
MT4C8513 L	512K x 8	FP, WPB, LP 2-15
MT4(L)C2M8A1	2 Meg x 8	FP, 4KR 2-31
MT4(L)C2M8A2	2 Meg x 8	FP, 4KR, WPB 2-31
MT4(L)C2M8B1	2 Meg x 8	FP, 2KR 2-47
MT4(L)C2M8B2	2 Meg x 8	FP, 2KR, WPB 2-47
MT4(L)C2M8A1 S	2 Meg x 8	FP, 4KR, S, LP 2-63
MT4(L)C2M8A2 S	2 Meg x 8	FP, 4KR, WPB, S, LP 2-63
MT4(L)C2M8B1 S	2 Meg x 8	FP, 2KR, S, LP 2-81
MT4(L)C2M8B2 S	2 Meg x 8	FP, 2KR, WPB, S, LP 2-81
MT4C1664	64K x 16	FP, DW 2-99

WIDE DRAMS (continued)

		PAGE
MT4C1665	64K x 16	FP, WPB 2-99
MT4C1664 L	64K x 16	FP, DW, LP 2-115
MT4C1665 L	64K x 16	FP, WPB, LP 2-115
MT4C1670	64K x 16	SC, DW 2-133
MT4C1671	64K x 16	SC, WPB 2-133
MT4C1670 L	64K x 16	SC, DW, LP 2-151
MT4C1671 L	64K x 16	SC, WPB, LP 2-151
MT4C16256	256K x 16	FP, DW 2-169
MT4C16257	256K x 16	FP, DC 2-169
MT4C16258	256K x 16	FP, DW, WPB 2-169
MT4C16259	256K x 16	FP, DC, WPB 2-169
MT4C16256 L	256K x 16	FP, DW, LP 2-191
MT4C16257 L	256K x 16	FP, DC, LP 2-191
MT4C16258 L	256K x 16	FP, DW, WPB, LP 2-191
MT4C16259 L	256K x 16	FP, DC, WPB, LP 2-191
MT4C16260	256K x 16	FP, ASY, DW 2-213
MT4C16261	256K x 16	FP, WPB, ASY 2-213
MT4(L)C1M16C3	1 Meg x 16	FP, DC 2-229
MT4(L)C1M16C5	1 Meg x 16	FP, DW 2-229
MT4(L)C1M16C6	1 Meg x 16	FP, DC, WPB 2-229
MT4(L)C1M16C7	1 Meg x 16	FP, DW, WPB 2-229
MT4(L)C1M16C3 S	1 Meg x 16	FP, DC, S, LP 2-251
MT4(L)C1M16C5 S	1 Meg x 16	FP, DW, S, LP 2-251
MT4(L)C1M16C6 S	1 Meg x 16	FP, DC, WPB, S, LP 2-251
MT4(L)C1M16C7 S	1 Meg x 16	FP, DW, WPB, S, LP 2-251

FP ..... FAST PAGE MODE
LP ..... Low Power, Extended Refresh
DW ..... Dual WE
2KR ..... 2,048 Refresh
S ..... Self Refresh
SC ..... STATIC COLUMN
WPB ..... WRITE PER BIT
DC ..... Dual CAS
4KR ..... 4,096 Refresh
ASY ..... Asymmetrical Addressing

DRAM MODULES

MT2D2568	256K x 8	LP, LV* 3-1
MT2D18	1 Meg x 8	LP, LV* 3-11
MT8D18	1 Meg x 8	LP 3-21
MT2D48	4 Meg x 8	 3-31
MT8D48	4 Meg x 8	LP 3-41
MT8D168	16 Meg x 8	 3-51
MT3D2569	256K x 9	LP 3-61
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LP ..... Low Power
LV ..... Low Voltage
NOTE: All modules include FAST PAGE MODE cycle.
*Contact factory regarding availability of low voltage versions.

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FP ..... FAST PAGE MODE
LP ..... Low Power, Extended Refresh
BW ..... BLOCK WRITE

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DRAM PRODUCT SELECTION GUIDE

Memory Configuration	Optional Access Cycle	Part Number	Access Time (ns)	Typical Power Dissipation		Package and Number of Pins				Page
				Standby	Active	PDIP	ZIP	SOJ	TSOP	
1 Meg x 1	FP	MT4C1024	60, 70, 80	3mW	175mW	18	20	20	20	1-1
1 Meg x 1	FP, LP	MT4C1024 L	70, 80, 100	0.3mW	150mW	18	20	20	20	1-13
1 Meg x 1	SC	MT4C1026	70, 80	3mW	175mW	18	20	20	-	1-25
4 Meg x 1	FP	MT4C1004J	60, 70, 80	3mW	225mW	-	20	20	20	1-37
4 Meg x 1	FP, LP	MT4C1004J L	60, 70, 80	1mW	225mW	-	20	20	20	1-49
4 Meg x 1	SC	MT4C1006J	70, 80	3mW	225mW	-	20	20	-	1-61
16 Meg x 1	FP, 4KR	MT4C16M1A1	60, 70, 80	3mW	325mW	-	-	24	24	1-73
16 Meg x 1	FP, 4KR, LV	MT4LC16M1A1	60, 70, 80	1mW	125mW	-	-	24	24	1-73
16 Meg x 1	SC, 4KR	MT4C16M1D1	60, 70, 80	3mW	330mW	-	-	24	-	1-85
256K x 4	FP	MT4C4256	60, 70, 80	3mW	175mW	20	20	20	20	1-87
256K x 4	FP, LP	MT4C4256 L	70, 80, 100	0.3mW	150mW	20	20	20	20	1-97
256K x 4	FP, LP, LV	MT4C4256 VL	100, 120	0.1mW	100mW	-	20	20	20	1-109
256K x 4	SC	MT4C4258	70, 80 ,100	3mW	175mW	20	20	20	-	1-121
1 Meg x 4	FP	MT4C4001J	60, 70, 80	3mW	225mW	-	20	20	20	1-133
1 Meg x 4	FP, LP	MT4C4001J L	60, 70, 80	1mW	225mW	-	20	20	20	1-145
1 Meg x 4	SC	MT4C4003J	70, 80	3mW	225mW	-	20	20	-	1-157
1 Meg x 4	FP, QCP	MT4C4004J	70, 80, 100	3mW	225mW	-	-	24	-	1-169
4 Meg x 4	FP, 4KR	MT4C4M4A1	60, 70, 80	3mW	325mW	-	-	24	24	1-183
4 Meg x 4	FP, 2KR	MT4C4M4B1	60, 70, 80	3mW	400mW	-	-	24	24	1-183
4 Meg x 4	FP, 4KR, LV	MT4LC4M4A1	60, 70, 80	1mW	125mW	-	-	24	24	1-195
4 Meg x 4	FP, 2KR, LV	MT4LC4M4B1	60, 70, 80	1mW	175mW	-	-	24	24	1-195
4 Meg x 4	SC, 4KR	MT4C4M4D1	60, 70, 80	3mW	325mW	-	-	24	-	1-207

FP = Fast Page Mode, SC = Static Column Mode, LP = Low Power, Extended Refresh; QCP = Quad CAS Parity,
LV = Low Voltage, 2KR = 2,048 Row Refresh, 4KR = 4,096 Row Refresh

WIDE DRAM PRODUCT SELECTION GUIDE

Memory Configuration	Optional Access Cycle	Part Number*	Access Time (ns)	Typical Power Dissipation		Package/Number of Pins			Page
				Standby	Active	ZIP	SOJ	TSOP	
512K x 8	FP	MT4C8512	70, 80, 100	3mW	350mW	28	28	28	2-1
512K x 8	FP, WPB	MT4C8513	70, 80, 100	3mW	350mW	28	28	28	2-1
512K x 8	FP, LP	MT4C8512 L	70, 80, 100	1mW	350mW	28	28	28	2-15
512K x 8	FP, WPB, LP	MT4C8513 L	70, 80, 100	1mW	350mW	28	28	28	2-15
2 Meg x 8	FP, 4KR	MT4(L)C2M8A1	60, 70, 80	5mW	400mW	-	28, 32	28, 32	2-31
2 Meg x 8	FP, 4KR, WPB	MT4(L)C2M8A2	60, 70, 80	5mW	400mW	-	28, 32	28, 32	2-31
2 Meg x 8	FP, 2KR	MT4(L)C2M8B1	60, 70, 80	5mW	400mW	-	28, 32	28, 32	2-47
2 Meg x 8	FP, 2KR, WPB	MT4(L)C2M8B2	60, 70, 80	5mW	400mW	-	28, 32	28, 32	2-47
2 Meg x 8	FP, 4KR, S, LP	MT4(L)C2M8A1 S	60, 70, 80	2mW	400mW	-	28, 32	28, 32	2-63
2 Meg x 8	FP, 4KR, WPB, S, LP	MT4(L)C2M8A2 S	60, 70, 80	2mW	400mW	-	28, 32	28, 32	2-63
2 Meg x 8	FP, 2KR, S, LP	MT4(L)C2M8B1 S	60, 70, 80	2mW	400mW	-	28, 32	28, 32	2-81
2 Meg x 8	FP, 2KR, WPB, S, LP	MT4(L)C2M8B2 S	60, 70, 80	2mW	400mW	-	28, 32	28, 32	2-81
64K x 16	FP, DW	MT4C1664	70, 80, 100	3mW	225mW	40	40	40	2-99
64K x 16	FP, WPB	MT4C1665	70, 80, 100	3mW	225mW	40	40	40	2-99
64K x 16	FP, DW, LP	MT4C1664 L	70, 80, 100	1mW	225mW	40	40	40	2-115
64K x 16	FP, WPB, LP	MT4C1665 L	70, 80, 100	1mW	225mW	40	40	40	2-115
64K x 16	SC, DW	MT4C1670	70, 80, 100	3mW	225mW	40	40	40	2-133
64K x 16	SC, WPB	MT4C1671	70, 80, 100	3mW	225mW	40	40	40	2-133
64K x 16	SC, DW, LP	MT4C1670 L	70, 80, 100	1mW	225mW	40	40	40	2-151
64K x 16	SC, WPB, LP	MT4C1671 L	70, 80, 100	1mW	225mW	40	40	40	2-151
256K x 16	FP, DW	MT4C16256	70, 80, 100	3mW	500mW	40	40	40	2-169
256K x 16	FP, DC	MT4C16257	70, 80, 100	3mW	500mW	40	40	40	2-169
256K x 16	FP, DW, WPB	MT4C16258	70, 80, 100	3mW	500mW	40	40	40	2-169
256K x 16	FP, DC, WPB	MT4C16259	70, 80, 100	3mW	500mW	40	40	40	2-169
256K x 16	FP, DW, LP	MT4C16256 L	70, 80, 100	1mW	500mW	40	40	40	2-191
256K x 16	FP, DC, LP	MT4C16257 L	70, 80, 100	1mW	500mW	40	40	40	2-191
256K x 16	FP, DW, WPB, LP	MT4C16258 L	70, 80, 100	1mW	500mW	40	40	40	2-191
256K x 16	FP, DC, WPB, LP	MT4C16259 L	70, 80, 100	1mW	500mW	40	40	40	2-191
256K x 16	FP, ASY, DW	MT4C16260	70, 80, 100	1mW	500mW	40	40	40	2-213
256K x 16	FP, WPB, ASY	MT4C16261	70, 80, 100	1mW	500mW	40	40	40	2-213
1 Meg x 16	FP, DC	MT4(L)C1M16C3	60, 70, 80	5mW	500mW	-	42	44	2-229
1 Meg x 16	FP, DW	MT4(L)C1M16C5	60, 70, 80	5mW	500mW	-	42	44	2-229
1 Meg x 16	FP, DC, WPB	MT4(L)C1M16C6	60, 70, 80	5mW	500mW	-	42	44	2-229
1 Meg x 16	FP, DW, WPB	MT4(L)C1M16C7	60, 70, 80	5mW	500mW	-	42	44	2-229
1 Meg x 16	FP, DC, S, LP	MT4(L)C1M16C3 S	60, 70, 80	2mW	500mW	-	42	44	2-251
1 Meg x 16	FP, DW, S, LP	MT4(L)C1M16C5 S	60, 70, 80	2mW	500mW	-	42	44	2-251
1 Meg x 16	FP, DC, WPB, S, LP	MT4(L)C1M16C6 S	60, 70, 80	2mW	500mW	-	42	44	2-251
1 Meg x 16	FP, DW, WPB, S, LP	MT4(L)C1M16C7 S	60, 70, 80	2mW	500mW	-	42	44	2-251

FP = Fast Page Mode, SC = Static Column, LP = Low Power, Extended Refresh; WPB = Write Per Bit, DW = Dual WE, DC = Dual CAS, 2KR = 2,048 Refresh, 4KR = 4,096 Refresh, S = Self Refresh, ASY = Asymmetrical Addressing
*(L)C means device is available in both 5V Vcc (MT4CXXXXX) and 3/3.3V Vcc (MT4LCXXXXX) versions

DRAM MODULE PRODUCT SELECTION GUIDE

Memory Configuration	Part Number	Optional Access Cycle	Access Time (ns)	Power Dissipation		Package		Page
				Standby	Active	SIMM	SIP	
256K x 8	MT2D2568	LP, LV*	60, 70, 80	6mW	350mW	30	30	3-1
1 Meg x 8	MT2D18	LP, LV*	60, 70, 80	6mW	450mW	30	30	3-11
1 Meg x 8	MT8D18	LP	60, 70, 80	24mW	1,400mW	30	30	3-21
4 Meg x 8	MT2D48		60, 70, 80	10mW	550mW	30	30	3-31
4 Meg x 8	MT8D48	LP	60, 70, 80	24mW	1,800mW	30	30	3-41
16 Meg x 8	MT8D168		60, 70, 80	24mW	2,200mW	30	30	3-51
256K x 9	MT3D2569	LP	60, 70, 80	9mW	625mW	30	30	3-61
1 Meg x 9	MT3D19	LP	60, 70, 80	9mW	625mW	30	30	3-71
1 Meg x 9	MT9D19	LP	60, 70, 80	27mW	1,575mW	30	30	3-81
4 Meg x 9	MT3D49		60, 70, 80	12mW	775mW	30	30	3-91
4 Meg x 9	MT9D49	LP	60, 70, 80	27mW	2,025mW	30	30	3-101
16 Meg x 9	MT9D169		60, 70, 80	27mW	2,475mW	30	30	3-111
512K x 16	MT8D25632	LP, LV*	60, 70, 80	24mW	1,400mW	72	-	3-121
1 Meg x 16	MT16D51232	LP, LV*	60, 70, 80	48mW	2,800mW	72	-	3-133
2 Meg x 16	MT8D132	LP, LV*	60, 70, 80	24mW	1,800mW	72	-	3-145
4 Meg x 16	MT16D232	LP, LV*	60, 70, 80	48mW	1,824mW	72	-	3-157
8 Meg x 16	MT8D432		60, 70, 80	40mW	2,200mW	72	-	3-169
16 Meg x 16	MT16D832		60, 70, 80	80mW	2,240mW	72	-	3-179
512K x 18	MT10D25636		60, 70, 80	30mW	1,750mW	72	-	3-199
1 Meg x 18	MT6D118		60, 70, 80	18mW	1,250mW	72	-	3-209
1 Meg x 18	MT20D51236		60, 70, 80	60mW	1,780mW	72	-	3-229
2 Meg x 18	MT12D136	LP	60, 70, 80	36mW	2,500mW	72	-	3-249
4 Meg x 18	MT24D236	LP	60, 70, 80	72mW	2,536mW	72	-	3-271
8 Meg x 18	MT12D436		60, 70, 80	52mW	3,100mW	72	-	3-283
16 Meg x 18	MT24D836		60, 70, 80	104mW	3,152mW	72	-	3-293
256K x 32	MT8D25632	LP, LV*	60, 70, 80	24mW	1,400mW	72	-	3-121
512K x 32	MT16D51232	LP, LV*	60, 70, 80	48mW	1,424mW	72	-	3-133
1 Meg x 32	MT8D132	LP, LV*	60, 70, 80	24mW	1,800mW	72	-	3-145
2 Meg x 32	MT16D232	LP, LV*	60, 70, 80	48mW	1,824mW	72	-	3-157
4 Meg x 32	MT8D432		60, 70, 80	40mW	2,200mW	72	-	3-169
8 Meg x 32	MT16D832		60, 70, 80	80mW	2,240mW	72	-	3-179
256K x 36	MT9D25636		60, 70, 80	27mW	1,575mW	72	-	3-189
256K x 36	MT10D25636		60, 70, 80	30mW	1,750mW	72	-	3-199
512K x 36	MT18D51236		60, 70, 80	54mW	1,600mW	72	-	3-219
512K x 36	MT20D51236		60, 70, 80	60mW	1,780mW	72	-	3-229
1 Meg x 36	MT9D136		60, 70, 80	27mW	2,175mW	72	-	3-239
1 Meg x 36	MT12D136	LP	60, 70, 80	36mW	2,500mW	72	-	3-249
2 Meg x 36	MT18D236		60, 70, 80	54mW	2,052mW	72	-	3-261
2 Meg x 36	MT24D236	LP	60, 70, 80	72mW	2,536mW	72	-	3-271
4 Meg x 36	MT12D436		60, 70, 80	52mW	3,100mW	72	-	3-283
8 Meg x 36	MT24D836		60, 70, 80	104mW	3,152mW	72	-	3-293
256K x 40	MT10D25640	LP, LV*	60, 70, 80	30mW	1,750mW	72	-	3-303
512K x 40	MT20D51240	LP, LV*	60, 70, 80	60mW	1,780mW	72	-	3-315
1 Meg x 40	MT10D140	LP, LV*	60, 70, 80	30mW	2,250mW	72	-	3-327
2 Meg x 40	MT20D240	LP, LV*	60, 70, 80	60mW	2,280mW	72	-	3-339

LP = Low Power, Extended Refresh; LV = Low Voltage
NOTE: All modules include FAST PAGE MODE cycle. *Contact factory regarding availability of low voltage versions.

IC DRAM CARD SELECTION GUIDE

Memory Configuration		Part Number	Access Time (ns)	Number of Pins Card	Page
512K x 16	1 Megabyte	MT8D88C25632	60, 70, 80	88	4-1
1 Meg x 16	2 Megabytes	MT16D88C51232	60, 70, 80	88	4-17
2 Meg x 16	4 Megabytes	MT8D88C132	60, 70, 80	88	4-33
4 Meg x 16	8 Megabytes	MT16D88C232	60, 70, 80	88	4-49
512K x 18	1 Megabyte	MT12D88C25636	60, 70, 80	88	4-65
1 Meg x 18	2 Megabytes	MT24D88C51236	60, 70, 80	88	4-79
2 Meg x 18	4 Megabytes	MT12D88C136	60, 70, 80	88	4-93
4 Meg x 18	8 Megabytes	MT24D88C236	60, 70, 80	88	4-107
512K x 20	1 Megabyte	MT12D88C25640	60, 70, 80	88	4-121
1 Meg x 20	2 Megabytes	MT24D88C51240	60, 70, 80	88	4-137
2 Meg x 20	4 Megabytes	MT12D88C140	60, 70, 80	88	4-153
4 Meg x 20	8 Megabytes	MT24D88C240	60, 70, 80	88	4-169
256K x 32	1 Megabyte	MT8D88C25632	60, 70, 80	88	4-1
512K x 32	2 Megabytes	MT16D88C51232	60, 70, 80	88	4-17
1 Meg x 32	4 Megabytes	MT8D88C132	60, 70, 80	88	4-33
2 Meg x 32	8 Megabytes	MT16D88C232	60, 70, 80	88	4-49
256K x 36	1 Megabyte	MT12D88C25636	60, 70, 80	88	4-65
512K x 36	2 Megabytes	MT24D88C51236	60, 70, 80	88	4-79
1 Meg x 36	4 Megabytes	MT12D88C136	60, 70, 80	88	4-93
2 Meg x 36	8 Megabytes	MT24D88C236	60, 70, 80	88	4-107
256K x 40	1 Megabyte	MT12D88C25640	60, 70, 80	88	4-121
512K x 40	2 Megabytes	MT24D88C51240	60, 70, 80	88	4-137
1 Meg x 40	4 Megabytes	MT12D88C140	60, 70, 80	88	4-153
2 Meg x 40	8 Megabytes	MT24D88C240	60, 70, 80	88	4-169

DUAL PORT DRAM (VRAM) PRODUCT SELECTION GUIDE

Memory Configuration	Access Cycle	Part Number	Access Time (ns)	Power Dissipation		Package and Number of Pins				Page
				Standby	Active	SOJ	SOG	TSOP	ZIP	
256K x 4	FP	MT42C4255	80, 100	15mW	275mW	28	-	-	28	5-1
256K x 4	FP, BW, LP	MT42C4256	70, 80, 100	15mW	275mW	28	-	-	28	5-3
128K x 8	FP	MT42C8127	80, 100	15mW	275mW	40	-	-	-	5-39
128K x 8	FP, BW, LP	MT42C8128	70, 80, 100	15mW	275mW	40	-	40/44	-	5-41
256K x 8	FP, BW	MT42C8255	70, 80	10mW	300mW	40	-	40/44	-	5-79
256K x 8	FP, BW	MT42C8256	70, 80	10mW	300mW	40	-	40/44	-	5-111
256K x 16	FP, BW	MT42C256K16A1	60, 70, 80	10mW	350mW	-	64	-	-	5-153

FP = Fast Page Mode, BW = Block Write, LP = Low Power, Extended Refresh

TRIPLE PORT DRAM PRODUCT SELECTION GUIDE

Memory Configuration	Access Cycle	Part Number	Access Time (ns)	Power Dissipation		Package/Number of Pins				Page
				Standby	Active	SOJ	SOG	TSOP	PLCC	
256K x 4	FP, BW, QSF pin	MT43C4257	80, 100	15mW	500mW	40	-	40/44	-	5-155
256K x 4	FP, BW, SSF pin	MT43C4258	80, 100	15mW	500mW	40	-	40/44	-	5-155
128K x 8	FP, BW, QSF pin	MT43C8128	80, 100	15mW	550mW	-	-	-	52	5-201
128K x 8	FP, BW, SSF pin	MT43C8129	80, 100	15mW	550mW	-	-	-	52	5-201
256K x 8	FP, BW	MT43C256K8A1	60, 70, 80	15mW	400mW	-	64	-	-	5-247

FP = Fast Page Mode, BW = Block Write

APPLICATION/TECHNICAL NOTE SELECTION GUIDE

Technical Note	Title	Page
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MICRON TECHNOLOGY, INC

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DRAM PRODUCT SELECTION GUIDE

Memory Configuration	Optional Access Cycle	Part Number	Access Time (ns)	Typical Power Dissipation		Package and Number of Pins				Page
				Standby	Active	PDIP	ZIP	SOJ	TSOP	
1 Meg x 1	FP	MT4C1024	60, 70, 80	3mW	175mW	18	20	20	20	1-1
1 Meg x 1	FP, LP	MT4C1024 L	70, 80, 100	0.3mW	150mW	18	20	20	20	1-13
1 Meg x 1	SC	MT4C1026	70, 80	3mW	175mW	18	20	20	-	1-25
4 Meg x 1	FP	MT4C1004J	60, 70, 80	3mW	225mW	-	20	20	20	1-37
4 Meg x 1	FP, LP	MT4C1004J L	60, 70, 80	1mW	225mW	-	20	20	20	1-49
4 Meg x 1	SC	MT4C1006J	70, 80	3mW	225mW	-	20	20	-	1-61
16 Meg x 1	FP, 4KR	MT4C16M1A1	60, 70, 80	3mW	325mW	-	-	24	24	1-73
16 Meg x 1	FP, 4KR, LV	MT4LC16M1A1	60, 70, 80	1mW	125mW	-	-	24	24	1-73
16 Meg x 1	SC, 4KR	MT4C16M1D1	60, 70, 80	3mW	330mW	-	-	24	-	1-85
256K x 4	FP	MT4C4256	60, 70, 80	3mW	175mW	20	20	20	20	1-87
256K x 4	FP, LP	MT4C4256 L	70, 80, 100	0.3mW	150mW	20	20	20	20	1-97
256K x 4	FP, LP, LV	MT4C4256 VL	100, 120	0.1mW	100mW	-	20	20	20	1-109
256K x 4	SC	MT4C4258	70, 80 ,100	3mW	175mW	20	20	20	-	1-121
1 Meg x 4	FP	MT4C4001J	60, 70, 80	3mW	225mW	-	20	20	20	1-133
1 Meg x 4	FP, LP	MT4C4001J L	60, 70, 80	1mW	225mW	-	20	20	20	1-145
1 Meg x 4	SC	MT4C4003J	70, 80	3mW	225mW	-	20	20	-	1-157
1 Meg x 4	FP, QCP	MT4C4004J	70, 80, 100	3mW	225mW	-	-	24	-	1-169
4 Meg x 4	FP, 4KR	MT4C4M4A1	60, 70, 80	3mW	325mW	-	-	24	24	1-183
4 Meg x 4	FP, 2KR	MT4C4M4B1	60, 70, 80	3mW	400mW	-	-	24	24	1-183
4 Meg x 4	FP, 4KR, LV	MT4LC4M4A1	60, 70, 80	1mW	125mW	-	-	24	24	1-195
4 Meg x 4	FP, 2KR, LV	MT4LC4M4B1	60, 70, 80	1mW	175mW	-	-	24	24	1-195
4 Meg x 4	SC, 4KR	MT4C4M4D1	60, 70, 80	3mW	325mW	-	-	24	-	1-207

FP = Fast Page Mode, SC = Static Column Mode, LP = Low Power, Extended Refresh; QCP = Quad CAS Parity,
LV = Low Voltage, 2KR = 2,048 Row Refresh, 4KR = 4,096 Row Refresh

DRAM

1 MEG x 1 DRAM

FAST PAGE MODE

FEATURES

- Industry standard x1 pinout, timing, functions and packages
- High-performance, CMOS silicon-gate process
- Single +5V ±10% power supply
- Low power, 3mW standby; 175mW active, typical
- All inputs, outputs and clocks are fully TTL compatible
- 512-cycle refresh in 8ms
- Refresh modes: $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$ (CBR) and HIDDEN
- Optional FAST PAGE MODE access cycle

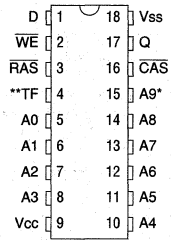
OPTIONS

	MARKING
• Timing	
60ns access	- 6
70ns access	- 7
80ns access	- 8
• Packages	
Plastic DIP (300 mil)	None
Plastic ZIP (350 mil)	Z
Plastic SOJ (300 mil)	DJ
Plastic TSOP (300 mil)***	TG
• Operating Temperature, T_A	
Commercial (0°C to +70°C)	None
Industrial (-40°C to +85°C)	IT

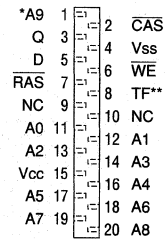
NOTE: Available in die form (commercial or military) or military ceramic packages. Please consult factory for die data sheets or refer to Micron's *Military Data Book.*

PIN ASSIGNMENT (Top View)

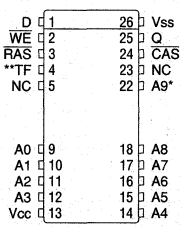
18-Pin DIP (N-1)



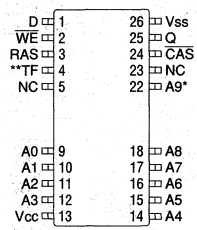
20-Pin ZIP (O-1)



20-Pin SOJ (Q-1)



20-Pin TSOP (R-1)



*Address not used for $\overline{RAS}$-ONLY refresh
**TF = Test Function, V_{IN} must not exceed Vcc+1V for normal operation
***Consult factory on availability of reverse pinout TSOP packages

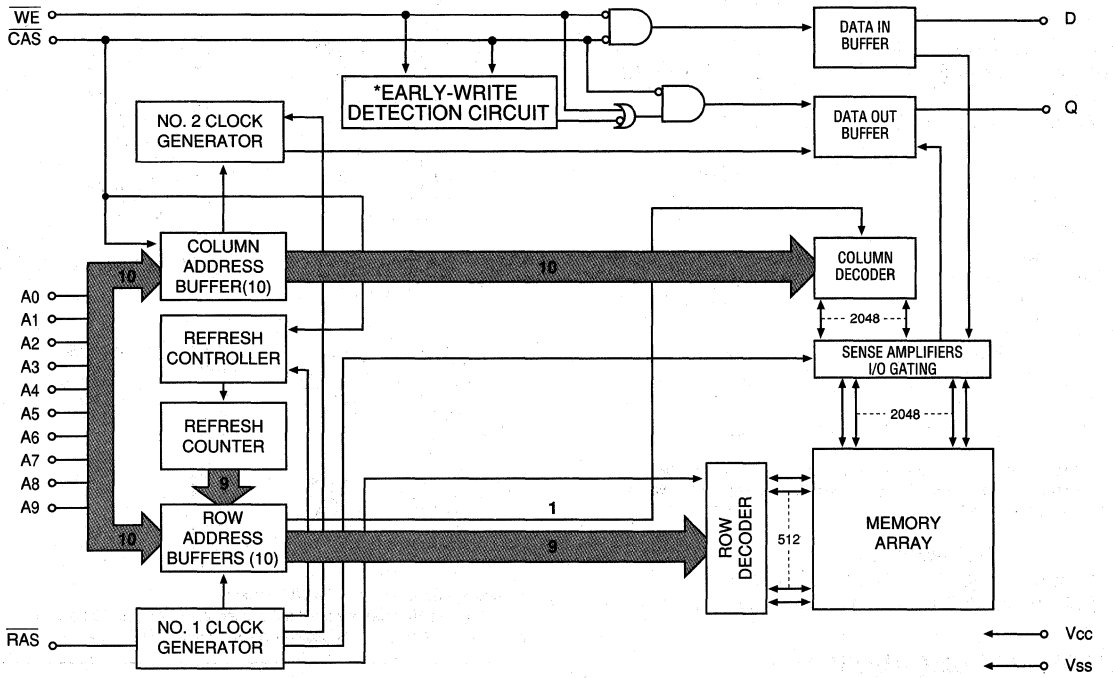
GENERAL DESCRIPTION

The MT4C1024 is a randomly accessed solid-state memory containing 1,048,576 bits organized in a x1 configuration. During READ or WRITE cycles, each bit is uniquely addressed through the 20 address bits, which are entered 10 bits (A0-A9) at a time. $\overline{RAS}$ is used to latch the first 10 bits and $\overline{CAS}$ the latter 10 bits. READ and WRITE cycles are selected with the $\overline{WE}$ input. A logic HIGH on $\overline{WE}$ dictates READ mode while a logic LOW on $\overline{WE}$ dictates WRITE mode. During a WRITE cycle, data in (D) is latched by the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. If $\overline{WE}$ goes LOW prior to $\overline{CAS}$ going LOW, the output pin, data out (Q), remains open (High-Z) until the next $\overline{CAS}$ cycle. If $\overline{WE}$ goes LOW after data reaches the output pin, Q is activated and retains the selected cell data as long as $\overline{CAS}$ remains LOW (regardless of $\overline{WE}$ or $\overline{RAS}$). This late $\overline{WE}$ pulse results in a READ-WRITE cycle.

FAST PAGE MODE operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row address (A0-A9) defined page boundary. The FAST PAGE MODE cycle is always initiated with a row address strobed-in by $\overline{RAS}$ followed by a column address strobed-in by $\overline{CAS}$. $\overline{CAS}$ may be toggled by holding $\overline{RAS}$ LOW and strobing-in different column addresses, thus executing faster memory cycles. Returning $\overline{RAS}$ HIGH terminates the FAST PAGE MODE operation.

Returning $\overline{RAS}$ and $\overline{CAS}$ HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the $\overline{RAS}$ high time. Memory cell data is retained in its correct state by maintaining power and executing any $\overline{RAS}$ cycle (READ, WRITE, $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$ (CBR), or HIDDEN refresh) so that all 512 combinations of $\overline{RAS}$ addresses (A0-A8) are executed at least every 8ms, regardless of sequence. The CBR refresh cycle will invoke the internal refresh counter for automatic $\overline{RAS}$ addressing.

FUNCTIONAL BLOCK DIAGRAM
FAST PAGE MODE



*NOTE: $\overline{WE}$ LOW prior to $\overline{CAS}$ LOW, EW detection circuit output is a HIGH (EARLY-WRITE)
$\overline{CAS}$ LOW prior to $\overline{WE}$ LOW, EW detection circuit output is a LOW (LATE-WRITE)

TRUTH TABLE

FUNCTION		$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	ADDRESSES		DATA	
					^tR	^tC	D (Data In)	Q (Data Out)
Standby		H	H→X	X	X	X	Don't Care	High-Z
READ		L	L	H	ROW	COL	Don't Care	Data Out
EARLY-WRITE		L	L	L	ROW	COL	Data In	High-Z
READ-WRITE		L	L	H→L	ROW	COL	Data In	Data Out
FAST-PAGE-MODE	1st Cycle	L	H→L	H	ROW	COL	Don't Care	Data Out
READ	2nd Cycle	L	H→L	H	n/a	COL	Don't Care	Data Out
FAST-PAGE-MODE	1st Cycle	L	H→L	L	ROW	COL	Data In	High-Z
EARLY-WRITE	2nd Cycle	L	H→L	L	n/a	COL	Data In	High-Z
FAST-PAGE-MODE	1st Cycle	L	H→L	H→L	ROW	COL	Data In	Data Out
READ-WRITE	2nd Cycle	L	H→L	H→L	n/a	COL	Data In	Data Out
$\overline{RAS}$-ONLY REFRESH		L	H	X	ROW	n/a	Don't Care	High-Z
HIDDEN	READ	L→H→L	L	H	ROW	COL	Don't Care	Data Out
REFRESH	WRITE	L→H→L	L	L	ROW	COL	Data In	High-Z
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH		H→L	L	X	X	X	Don't Care	High-Z

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to V_{SS} ..... -1V to +7V
Operating Temperature, T_A (Ambient) ..... 0°C to +70°C
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation 600mW
Soldering Temperature (Soldering 10 Seconds) ..... 260°C
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 3, 4, 6, 7) (V_{CC} = 5V ±10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.5	V	1
Input High (Logic 1) Voltage, All Inputs	V_{IH}	2.4	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, All Inputs	V_{IL}	-1.0	0.8	V	1
INPUT LEAKAGE CURRENT Any Input 0V ≤ V_{IN} ≤ 6.5V (All other pins not under test = 0V)	I_I	-2	2	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled, 0V ≤ V_{OUT} ≤ 5.5V)	I_{OZ}	-10	10	µA	
OUTPUT LEVELS Output High Voltage (I_{OUT} = -5mA)	V_{OH}	2.4		V	
Output Low Voltage (I_{OUT} = 4.2mA)	V_{OL}		0.4	V	

		MAX				
PARAMETER/CONDITION	SYMBOL	-6	-7	-8	UNITS	NOTES
STANDBY CURRENT: (TTL) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC1}	2	2	2	mA	
STANDBY CURRENT: (CMOS) ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} -0.2V)	I_{CC2}	1	1	1	mA	
OPERATING CURRENT: Random READ/WRITE Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC (MIN))	I_{CC3}	90	80	70	mA	3, 4
OPERATING CURRENT: FAST PAGE MODE Average power supply current ($\overline{RAS}$ = V_{IL}; $\overline{CAS}$, Address Cycling: ^tPC = ^tPC (MIN))	I_{CC4}	70	60	50	mA	3, 4
REFRESH CURRENT: $\overline{RAS}$-ONLY Average power supply current ($\overline{RAS}$ Cycling; $\overline{CAS}$ = V_{IH}: ^tRC = ^tRC (MIN))	I_{CC5}	90	80	70	mA	3
REFRESH CURRENT: $\overline{CAS}$-BEFORE-$\overline{RAS}$ Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC (MIN))	I_{CC6}	90	80	70	mA	3, 5

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A9, D	C_{I1}		5	pF	2
Input Capacitance: $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	C_{I2}		7	pF	2
Output Capacitance: Q	C_O		7	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (V_{CC} = 5.0V ± 10%)

AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	tRC	110		130		150		ns	
READ-WRITE cycle time	tRWC	135		155		175		ns	
FAST-PAGE-MODE READ or WRITE cycle time	tPC	40		40		45		ns	
FAST-PAGE-MODE READ-WRITE cycle time	tPRWC	60		65		70		ns	
Access time from $\overline{RAS}$	tRAC		60		70		80	ns	14
Access time from $\overline{CAS}$	tCAC		20		20		20	ns	15
Access time from column address	tAA		30		35		40	ns	
Access time from $\overline{CAS}$ precharge	tCPA		35		40		45	ns	
$\overline{RAS}$ pulse width	tRAS	60	100,000	70	100,000	80	100,000	ns	
$\overline{RAS}$ pulse width (FAST PAGE MODE)	tRASP	60	100,000	70	100,000	80	100,000	ns	
$\overline{RAS}$ hold time	tRSH	20		20		20		ns	
$\overline{RAS}$ precharge time	tRP	40		50		60		ns	
$\overline{CAS}$ pulse width	tCAS	20	100,000	20	100,000	20	100,000	ns	
$\overline{CAS}$ hold time	tCSH	60		70		80		ns	
$\overline{CAS}$ precharge time	tCPN	10		10		10		ns	16
$\overline{CAS}$ precharge time (FAST PAGE MODE)	tCP	10		10		10		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	tRCD	20	40	20	50	20	60	ns	17
$\overline{CAS}$ to $\overline{RAS}$ precharge time	tCRP	5		5		5		ns	
Row address setup time	tASR	0		0		0		ns	
Row address hold time	tRAH	10		10		10		ns	
$\overline{RAS}$ to column address delay time	tRAD	15	30	15	35	15	40	ns	18
Column address setup time	tASC	0		0		0		ns	
Column address hold time	tCAH	15		15		15		ns	
Column address hold time (referenced to $\overline{RAS}$)	tAR	45		55		60		ns	
Column address to $\overline{RAS}$ lead time	tRAL	30		35		40		ns	
Read command setup time	tRCS	0		0		0		ns	
Read command hold time (referenced to $\overline{CAS}$)	tRCH	0		0		0		ns	19
Read command hold time (referenced to $\overline{RAS}$)	tRRH	0		0		0		ns	19
$\overline{CAS}$ to output in Low-Z	tCLZ	0		0		0		ns	
Output buffer turn-off delay	tOFF	0	20	0	20	0	20	ns	20
$\overline{WE}$ command setup time	tWCS	0		0		0		ns	21

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

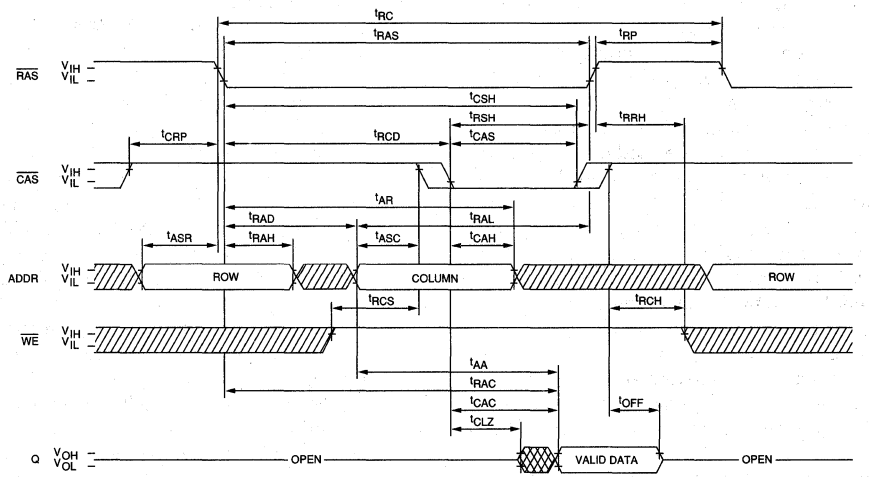
(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (V_{CC} = 5V ±10%)

AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Write command hold time	^tWCH	10		15		15		ns	
Write command hold time (referenced to $\overline{RAS}$)	^tWCR	45		55		60		ns	
Write command pulse width	^tWP	10		15		15		ns	
Write command to $\overline{RAS}$ lead time	^tRWL	20		20		20		ns	
Write command to $\overline{CAS}$ lead time	^tCWL	20		20		20		ns	
Data-in setup time	^tDS	0		0		0		ns	22
Data-in hold time	^tDH	15		15		15		ns	22
Data-in hold time (referenced to $\overline{RAS}$)	^tDHR	45		55		60		ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	^tRWD	60		70		80		ns	21
Column address to $\overline{WE}$ delay time	^tAWD	30		35		40		ns	21
$\overline{CAS}$ to $\overline{WE}$ delay time	^tCWD	15		20		20		ns	21
Transition time (rise or fall)	^tT	3	50	3	50	3	50	ns	9, 10
Refresh period (512 cycles)	^tREF		8		8		8	ms	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	^tRPC	0		0		0		ns	
$\overline{CAS}$ setup time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tCSR	10		10		10		ns	5
$\overline{CAS}$ hold time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tCHR	10		15		15		ns	5

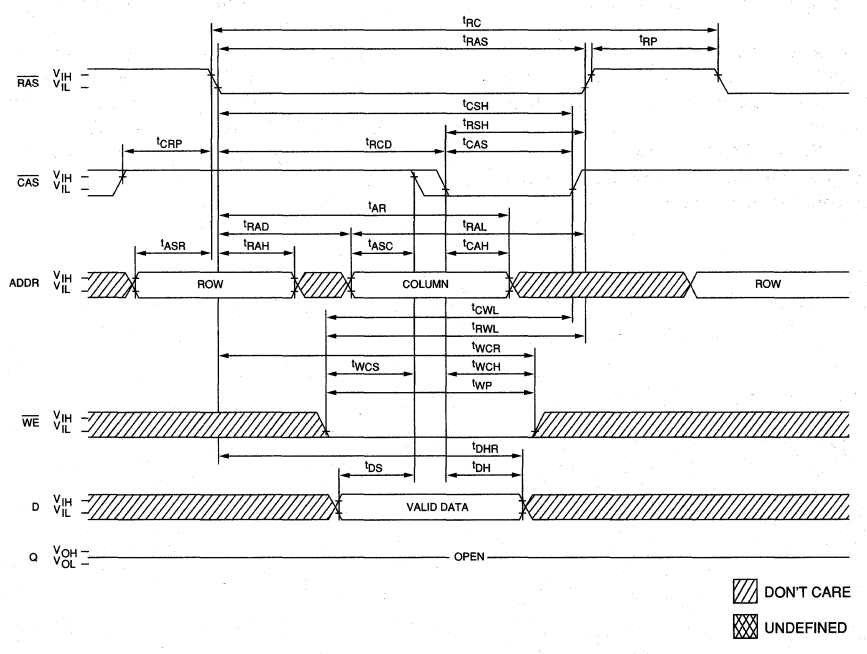
NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. V_{CC} = 5V ±10%, f = 1 MHz.
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is assured.
7. An initial pause of 100µs is required after power-up followed by any eight $\overline{RAS}$ cycles before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-up should be repeated any time the ^{t}REF refresh requirement is exceeded.
8. AC characteristics assume ^{t}T = 5ns.
9. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS}$ = V_{IH}, data output is High-Z.
12. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to 2 TTL gates and 100pF.
14. Assumes that $^{t}RCD < {}^{t}RCD$ (MAX). If ^{t}RCD is greater than the maximum recommended value shown in this table, ^{t}RAC will increase by the amount that ^{t}RCD exceeds the value shown.
15. Assumes that $^{t}RCD \geq {}^{t}RCD$ (MAX).
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer, $\overline{CAS}$ must be pulsed HIGH for ^{t}CPN.
17. Operation within the ^{t}RCD (MAX) limit ensures that ^{t}RAC (MAX) can be met. ^{t}RCD (MAX) is specified as a reference point only; if ^{t}RCD is greater than the specified ^{t}RCD (MAX) limit, then access time is controlled exclusively by ^{t}CAC.
18. Operation within the ^{t}RAD (MAX) limit ensures that ^{t}RAC (MIN) and ^{t}CAC (MIN) can be met. ^{t}RAD (MAX) is specified as a reference point only; if ^{t}RAD is greater than the specified ^{t}RAD (MAX) limit, then access time is controlled exclusively by ^{t}AA.
19. Either ^{t}RCH or ^{t}RRH must be satisfied for a READ cycle.
20. ^{t}OFF (MAX) defines the time at which the output achieves the open circuit condition, and is not referenced to V_{OH} or V_{OL}.
21. ^{t}WCS, ^{t}RWD, ^{t}AWD and ^{t}CWD are restrictive operating parameters. If $^{t}WCS \geq {}^{t}WCS$ (MIN), the cycle is an EARLY-WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If $^{t}RWD \geq {}^{t}RWD$ (MIN), $^{t}AWD \geq {}^{t}AWD$ (MIN) and $^{t}CWD \geq {}^{t}CWD$ (MIN), the cycle is a READ-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the cycle is a LATE-WRITE and the state of Q is indeterminate (at access time and until $\overline{CAS}$ goes back to V_{IH}).
22. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY-WRITE cycles and $\overline{WE}$ leading edge in LATE-WRITE or READ-MODIFY-WRITE cycles.
23. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW.

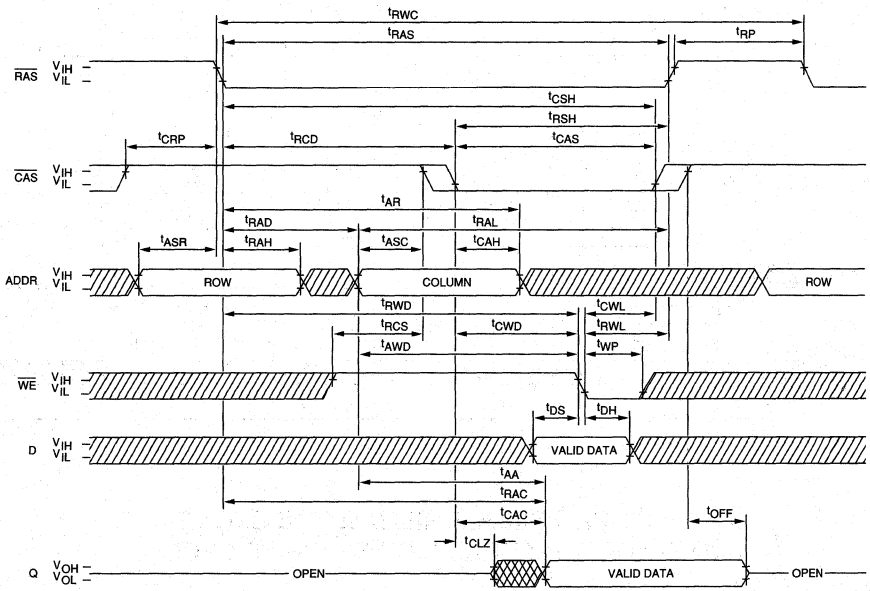
READ CYCLE



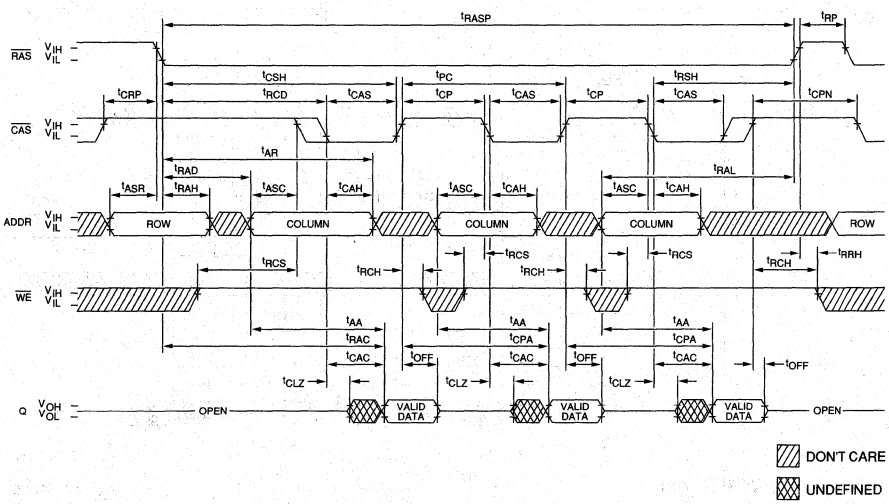
EARLY-WRITE CYCLE



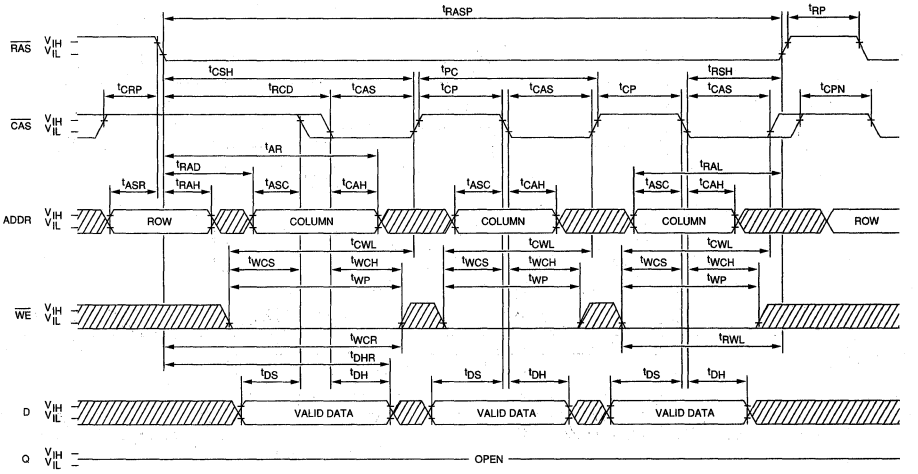
READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)



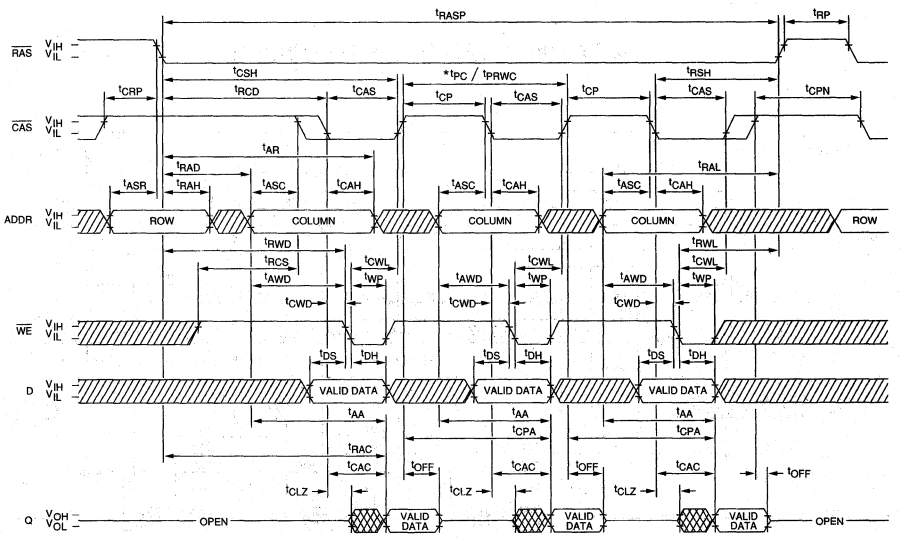
FAST-PAGE-MODE READ CYCLE



FAST-PAGE-MODE EARLY-WRITE CYCLE

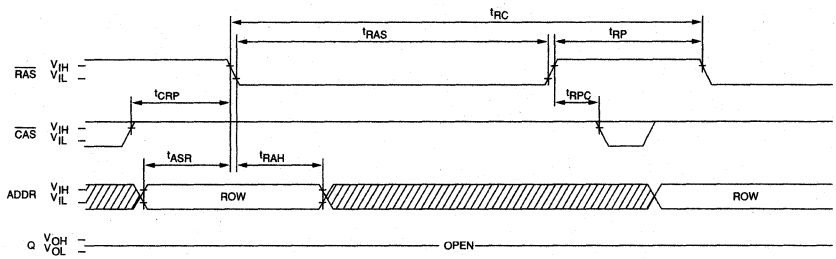


FAST-PAGE-MODE READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)

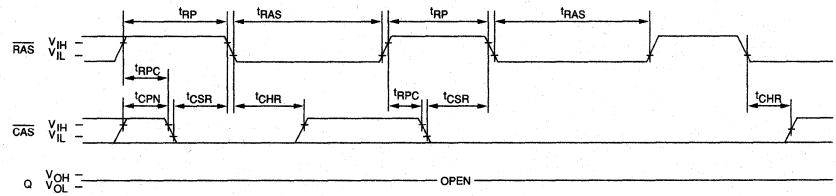


*tPC is for LATE-WRITE only.

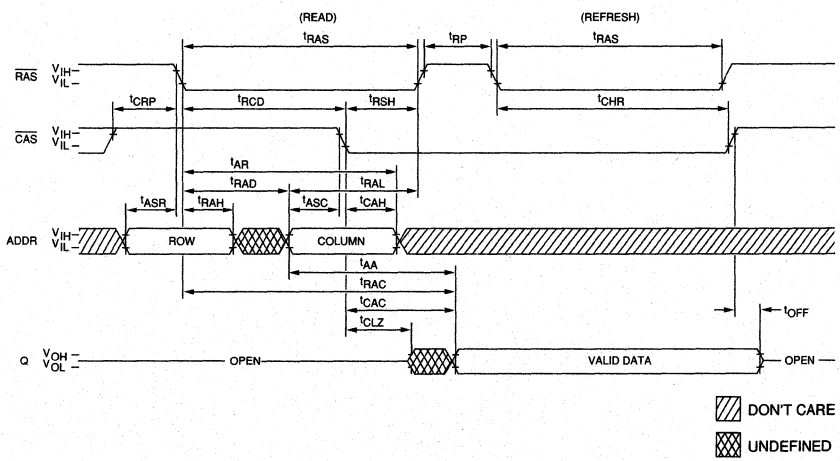
RAS-ONLY REFRESH CYCLE
(ADDR = A0-A8; A9 and WE = DON'T CARE)



CAS-BEFORE-RAS REFRESH CYCLE
(A0-A9 and WE = DON'T CARE)



HIDDEN REFRESH CYCLE [23]
(WE = HIGH)



DRAM

1 MEG x 1 DRAM

LOW POWER, EXTENDED REFRESH

FEATURES

- Industry standard x1 pinout, timing, functions and packages
- High-performance, CMOS silicon-gate process
- Single +5V ±10% power supply
- Low power, .3mW standby; 150mW active, typical
- All inputs, outputs and clocks are fully TTL compatible
- Optional FAST PAGE MODE access cycle
- Refresh modes: $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$ (CBR), HIDDEN and BATTERY BACKUP (BBU)
- 512-cycle extended refresh in 64ms
- Low CMOS STANDBY CURRENT, 200µA maximum

OPTIONS — MARKING

- Timing

70ns access	- 7
80ns access	- 8
100ns access	-10

- Packages

Plastic DIP (300 mil)	None
Plastic SOJ (300 mil)	DJ
Plastic TSOP (300 mil)***	TG
Plastic ZIP (350 mil)	Z

NOTE: Available in die form (commercial or military) or military ceramic packages. Please consult factory for die data sheets or refer to Micron's ***Military Data Book.***

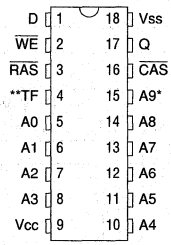
- Operating Temperature, T_A

Commercial (0°C to +70°C)	None
Industrial (-40°C to +85°C)	IT

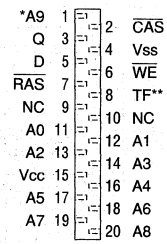
- Part Number Example: MT4C1024DJ-7 L

PIN ASSIGNMENT (Top View)

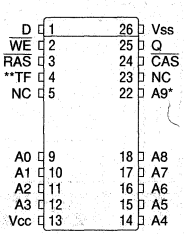
18-Pin DIP (N-1)



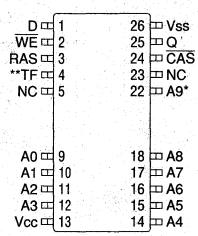
20-Pin ZIP (O-1)



20-Pin SOJ (Q-1)



20-Pin TSOP (R-1)



*Address not used for $\overline{RAS}$-ONLY refresh
**TF = Test Function, V_{IN} must not exceed Vcc+1V for normal operation
***Consult factory on availability of reverse pinout TSOP packages

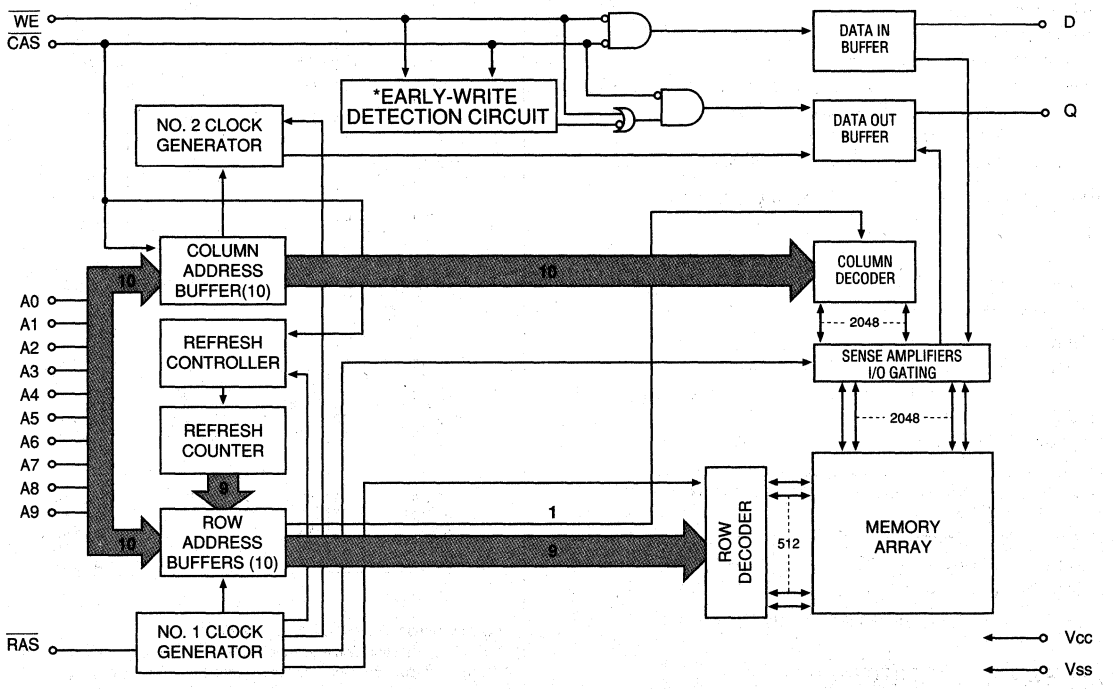
GENERAL DESCRIPTION

The MT4C1024 L is a randomly accessed solid-state memory containing 1,048,576 bits organized in a x1 configuration. During READ or WRITE cycles, each bit is uniquely addressed through the 20 address bits, which are entered 10 bits (A0-A9) at a time. $\overline{RAS}$ is used to latch the first 10 bits and $\overline{CAS}$ the latter 10 bits. READ and WRITE cycles are selected with the $\overline{WE}$ input. A logic HIGH on $\overline{WE}$ dictates READ mode while a logic LOW on $\overline{WE}$ dictates WRITE mode. During a WRITE cycle, data in (D) is latched by the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. If $\overline{WE}$ goes LOW prior to $\overline{CAS}$ going LOW, the output pin, data out (Q), remains open (High-Z) until the next $\overline{CAS}$ cycle. If $\overline{WE}$ goes LOW after data reaches the output pin, Q is activated and retains the selected cell data as long as $\overline{CAS}$ remains LOW (regardless of $\overline{WE}$ or $\overline{RAS}$). This late $\overline{WE}$ pulse results in a READ-WRITE cycle.

FAST PAGE MODE operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row address (A0-A9) defined page boundary. The FAST PAGE MODE cycle is always initiated with a row address strobed-in by $\overline{RAS}$ followed by a column address strobed-in by $\overline{CAS}$. $\overline{CAS}$ may be toggled by holding $\overline{RAS}$ LOW and strobing-in different column addresses, thus executing faster memory cycles. Returning $\overline{RAS}$ HIGH terminates the FAST PAGE MODE operation.

Returning $\overline{RAS}$ and $\overline{CAS}$ HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the $\overline{RAS}$ high time. Memory cell data is retained in its correct state by maintaining power and executing any $\overline{RAS}$ cycle (READ, WRITE, $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$ (CBR), or HIDDEN refresh) so that all 512 combinations of $\overline{RAS}$ addresses (A0-A8) are executed at least every 64ms, regardless of sequence. The CBR refresh cycle will invoke the internal refresh counter for automatic $\overline{RAS}$ addressing.

FUNCTIONAL BLOCK DIAGRAM
LOW POWER, FAST PAGE MODE



*NOTE: $\overline{WE}$ LOW prior to $\overline{CAS}$ LOW, EW detection circuit output is a HIGH (EARLY-WRITE)
$\overline{CAS}$ LOW prior to $\overline{WE}$ LOW, EW detection circuit output is a LOW (LATE-WRITE)

TRUTH TABLE

FUNCTION		RAS	CAS	WE	ADDRESSES		DATA	
					tR	tC	D (Data In)	Q (Data Out)
Standby		H	H→X	X	X	X	Don't Care	High-Z
READ		L	L	H	ROW	COL	Don't Care	Data Out
EARLY-WRITE		L	L	L	ROW	COL	Data In	High-Z
READ-WRITE		L	L	H→L	ROW	COL	Data In	Data Out
FAST-PAGE-MODE	1st Cycle	L	H→L	H	ROW	COL	Don't Care	Data Out
READ	2nd Cycle	L	H→L	H	n/a	COL	Don't Care	Data Out
FAST-PAGE-MODE	1st Cycle	L	H→L	L	ROW	COL	Data In	High-Z
EARLY-WRITE	2nd Cycle	L	H→L	L	n/a	COL	Data In	High-Z
FAST-PAGE-MODE	1st Cycle	L	H→L	H→L	ROW	COL	Data In	Data Out
READ-WRITE	2nd Cycle	L	H→L	H→L	n/a	COL	Data In	Data Out
RAS-ONLY REFRESH		L	H	X	ROW	n/a	Don't Care	High-Z
HIDDEN	READ	L→H→L	L	H	ROW	COL	Don't Care	Data Out
REFRESH	WRITE	L→H→L	L	L	ROW	COL	Data In	High-Z
CAS-BEFORE-RAS REFRESH		H→L	L	X	X	X	Don't Care	High-Z
BATTERY BACKUP REFRESH		H→L	L	X	X	X	Don't Care	High-Z

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to V_{SS} ..... -1V to +7V
Operating Temperature, T_A (Ambient) ..... 0°C to +70°C
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation 600mW
Soldering Temperature (Soldering 10 Seconds) ..... 260°C
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 3, 4, 6, 7) (V_{CC} = 5V ±10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.5	V	1
Input High (Logic 1) Voltage, All Inputs	V_{IH}	2.4	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, All Inputs	V_{IL}	-1.0	0.8	V	1
INPUT LEAKAGE CURRENT Any Input 0V ≤ V_{IN} ≤ 6.5V (All other pins not under test = 0V)	I_I	-2	2	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled; 0V ≤ V_{OUT} ≤ 5.5V)	I_{OZ}	-10	10	µA	
OUTPUT LEVELS Output High Voltage (I_{OUT} = -5mA)	V_{OH}	2.4		V	
Output Low Voltage (I_{OUT} = 4.2mA)	V_{OL}		0.4	V	

		MAX				
PARAMETER/CONDITION	SYMBOL	-7	-8	-10	UNITS	NOTES
STANDBY CURRENT: (TTL) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC1}	2	2	2	mA	
STANDBY CURRENT: (CMOS) ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} -0.2V)	I_{CC2}	200	200	200	µA	
OPERATING CURRENT: Random READ/WRITE Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Single Address Cycling: ^tRC = ^tRC (MIN))	I_{CC3}	75	65	60	mA	3, 4
OPERATING CURRENT: FAST PAGE MODE Average power supply current ($\overline{RAS}$ = V_{IL}; $\overline{CAS}$, Address Cycling: ^tPC = ^tPC (MIN))	I_{CC4}	55	45	40	mA	3, 4
REFRESH CURRENT: $\overline{RAS}$-ONLY Average power supply current ($\overline{RAS}$ Cycling; $\overline{CAS}$ = V_{IH}: ^tRC = ^tRC (MIN))	I_{CC5}	75	65	60	mA	3
REFRESH CURRENT: $\overline{CAS}$-BEFORE-$\overline{RAS}$ (CBR) Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC (MIN))	I_{CC6}	75	65	60	mA	3, 5
REFRESH CURRENT: BATTERY BACKUP (BBU) Average power supply current during BATTERY BACKUP refresh: $\overline{CAS}$ = 0.2V or $\overline{CAS}$-BEFORE-$\overline{RAS}$ cycling; $\overline{RAS}$ = ^tRAS (MIN) to 1µs; $\overline{WE}$, A0-A9 and D_{IN} = V_{CC} -0.2V or 0.2V (D_{IN} may be left OPEN), ^tRC = 125µs (512 rows at 125µs = 64ms)	I_{CC7}	200	200	200	µA	3, 5, 7, 24

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A9, D	C_{I1}		5	pF	2
Input Capacitance: $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	C_{I2}		7	pF	2
Output Capacitance: Q	C_O		7	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (V_{CC} = 5V ±10%)

AC CHARACTERISTICS		-7		-8		-10			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	^tRC	130		150		180		ns	
READ-WRITE cycle time	^tRWC	155		175		205		ns	
FAST-PAGE-MODE READ or WRITE cycle time	^tPC	40		45		55		ns	
FAST-PAGE-MODE READ-WRITE cycle time	^tPRWC	65		70		85		ns	
Access time from $\overline{RAS}$	^tRAC		70		80		100	ns	14
Access time from $\overline{CAS}$	^tCAC		20		20		25	ns	15
Access time from column address	^tAA		35		40		50	ns	
Access time from $\overline{CAS}$ precharge	^tCPA		40		45		50	ns	
$\overline{RAS}$ pulse width	^tRAS	70	100,000	80	100,000	100	100,000	ns	
$\overline{RAS}$ pulse width (FAST PAGE MODE)	^tRASP	70	100,000	80	100,000	100	100,000	ns	
$\overline{RAS}$ hold time	^tRSH	20		20		25		ns	
$\overline{RAS}$ precharge time	^tRP	50		60		70		ns	
$\overline{CAS}$ pulse width	^tCAS	20	100,000	20	100,000	25	100,000	ns	
$\overline{CAS}$ hold time	^tCSH	70		80		100		ns	
$\overline{CAS}$ precharge time	^tCPN	10		10		15		ns	16
$\overline{CAS}$ precharge time (FAST PAGE MODE)	^tCP	10		10		10		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	^tRCD	20	50	20	60	25	75	ns	17
$\overline{CAS}$ to $\overline{RAS}$ precharge time	^tCRP	5		5		5		ns	
Row address setup time	^tASR	0		0		0		ns	
Row address hold time	^tRAH	10		10		15		ns	
$\overline{RAS}$ to column-address delay time	^tRAD	15	35	15	40	20	50	ns	18
Column address setup time	^tASC	0		0		0		ns	
Column address hold time	^tCAH	15		15		20		ns	
Column address hold time (referenced to $\overline{RAS}$)	^tAR	55		60		70		ns	
Column address to $\overline{RAS}$ lead time	^tRAL	35		40		50		ns	
Read command setup time	^tRCS	0		0		0		ns	
Read command hold time (referenced to $\overline{CAS}$)	^tRCH	0		0		0		ns	19
Read command hold time (referenced to $\overline{RAS}$)	^tRRH	0		0		0		ns	19
$\overline{CAS}$ to output in Low-Z	^tCLZ	0		0		0		ns	
Output buffer turn-off delay	^tOFF	0	20	0	20	0	20	ns	20
$\overline{WE}$ command setup time	^tWCS	0		0		0		ns	21

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

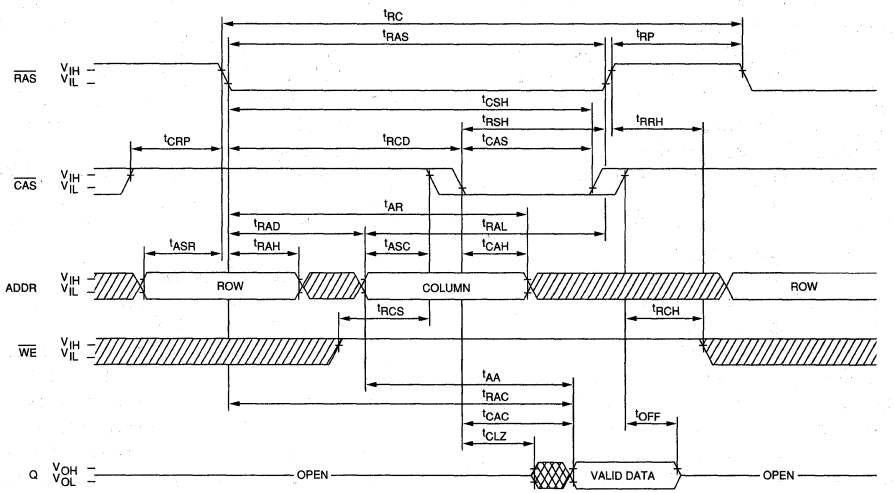
(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (Vcc = 5V ±10%)

AC CHARACTERISTICS		-7		-8		-10			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Write command hold time	^{t}WCH	15		15		20		ns	
Write command hold time (referenced to $\overline{RAS}$)	^{t}WCR	55		60		75		ns	
Write command pulse width	^{t}WP	15		15		20		ns	
Write command to $\overline{RAS}$ lead time	^{t}RWL	20		20		25		ns	
Write command to $\overline{CAS}$ lead time	^{t}CWL	20		20		25		ns	
Data-in setup time	^{t}DS	0		0		0		ns	22
Data-in hold time	^{t}DH	15		15		20		ns	22
Data-in hold time (referenced to $\overline{RAS}$)	^{t}DHR	55		60		75		ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	^{t}RWD	70		80		100		ns	21
Column address to $\overline{WE}$ delay time	^{t}AWD	35		40		50		ns	21
$\overline{CAS}$ to $\overline{WE}$ delay time	^{t}CWD	20		20		25		ns	21
Transition time (rise or fall)	^{t}T	3	50	3	50	3	50	ns	9, 10
Refresh period (512 cycles)	^{t}REF		64		64		64	ms	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	^{t}RPC	0		0		0		ns	
$\overline{CAS}$ setup time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^{t}CSR	10		10		10		ns	5
$\overline{CAS}$ hold time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^{t}CHR	15		15		15		ns	5

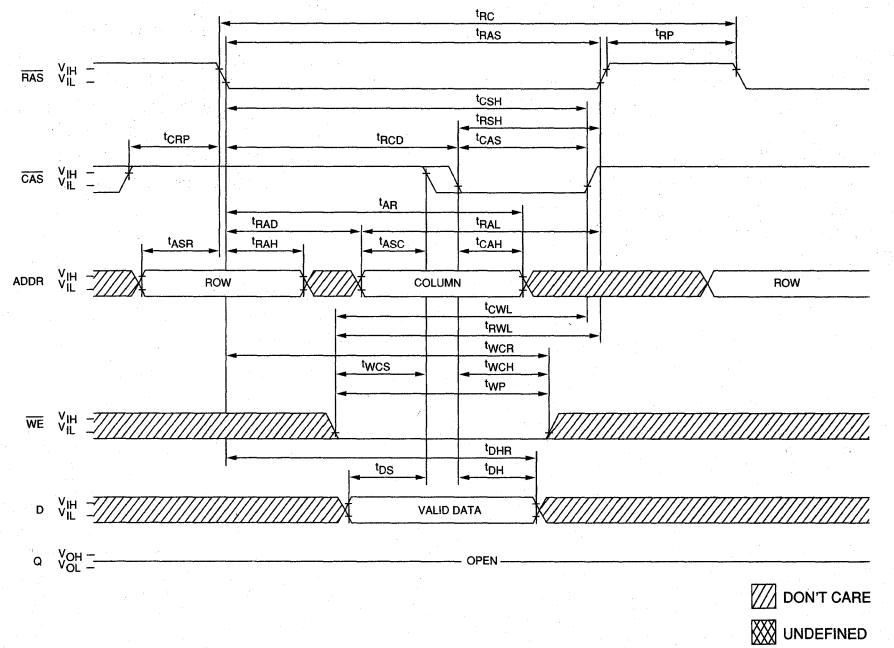
NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. V_{CC} = 5V ±10%, f = 1 MHz.
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is assured.
7. An initial pause of 100µs is required after power-up followed by any eight $\overline{RAS}$ cycles before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-up should be repeated any time the ^{t}REF refresh requirement is exceeded.
8. AC characteristics assume ^{t}T = 5ns.
9. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS}$ = V_{IH}, data output is High-Z.
12. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to 2 TTL gates and 100pF.
14. Assumes that $^{t}RCD < {}^{t}RCD$ (MAX). If ^{t}RCD is greater than the maximum recommended value shown in this table, ^{t}RAC will increase by the amount that ^{t}RCD exceeds the value shown.
15. Assumes that $^{t}RCD \geq {}^{t}RCD$ (MAX).
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer, $\overline{CAS}$ must be pulsed HIGH for ^{t}CPN.
17. Operation within the ^{t}RCD (MAX) limit ensures that ^{t}RAC (MAX) can be met. ^{t}RCD (MAX) is specified as a reference point only; if ^{t}RCD is greater than the specified ^{t}RCD (MAX) limit, then access time is controlled exclusively by ^{t}CAC.
18. Operation within the ^{t}RAD (MAX) limit ensures that ^{t}RAC (MIN) and ^{t}CAC (MIN) can be met. ^{t}RAD (MAX) is specified as a reference point only; if ^{t}RAD is greater than the specified ^{t}RAD (MAX) limit, then access time is controlled exclusively by ^{t}AA.
19. Either ^{t}RCH or ^{t}RRH must be satisfied for a READ cycle.
20. ^{t}OFF (MAX) defines the time at which the output achieves the open circuit condition, and is not referenced to V_{OH} or V_{OL}.
21. ^{t}WCS, ^{t}RWD, ^{t}AWD and ^{t}CWD are restrictive operating parameters in LATE-WRITE, and READ-MODIFY-WRITE cycles only. If $^{t}WCS \geq {}^{t}WCS$ (MIN), the cycle is an EARLY-WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If $^{t}RWD \geq {}^{t}RWD$ (MIN), $^{t}AWD \geq {}^{t}AWD$ (MIN) and $^{t}CWD \geq {}^{t}CWD$ (MIN), the cycle is a READ-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the cycle is a LATE-WRITE and the state of Q is indeterminate (at access time and until $\overline{CAS}$ goes back to V_{IH}).
22. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY-WRITE cycles and $\overline{WE}$ leading edge in LATE-WRITE or READ-MODIFY-WRITE cycles.
23. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW.
24. BBU current is reduced as ^{t}RAS is reduced from its maximum specification during the BBU cycle.

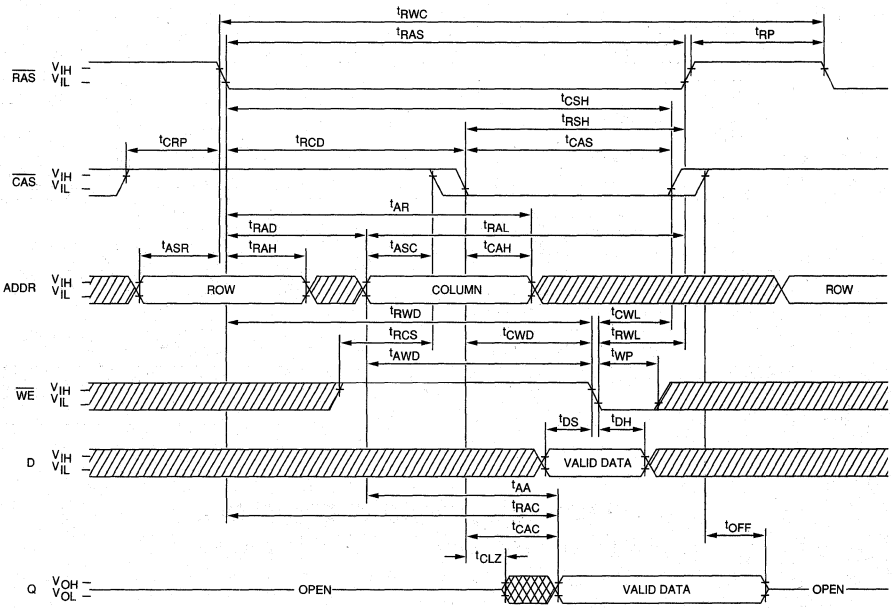
READ CYCLE



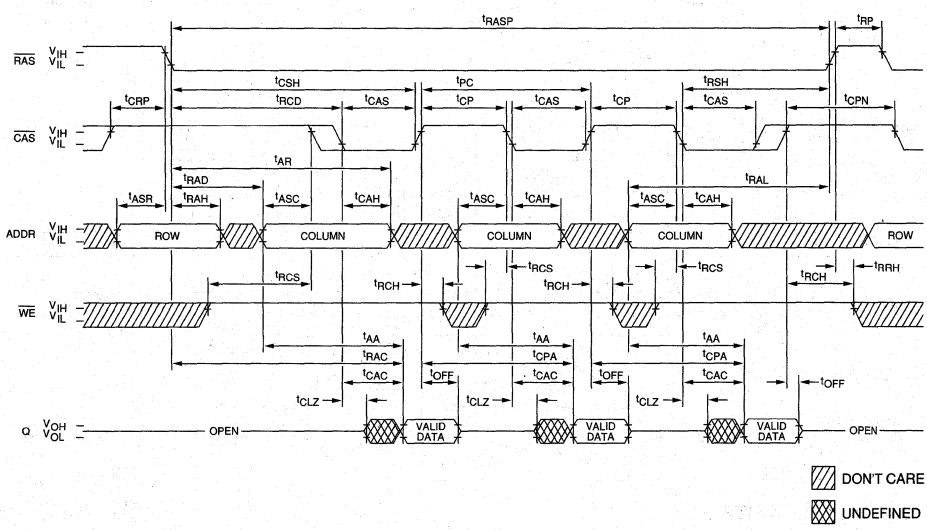
EARLY-WRITE CYCLE



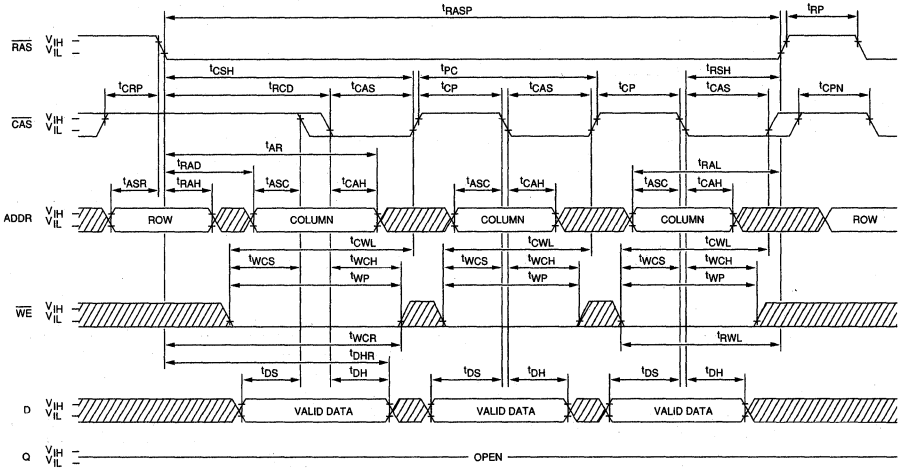
READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)



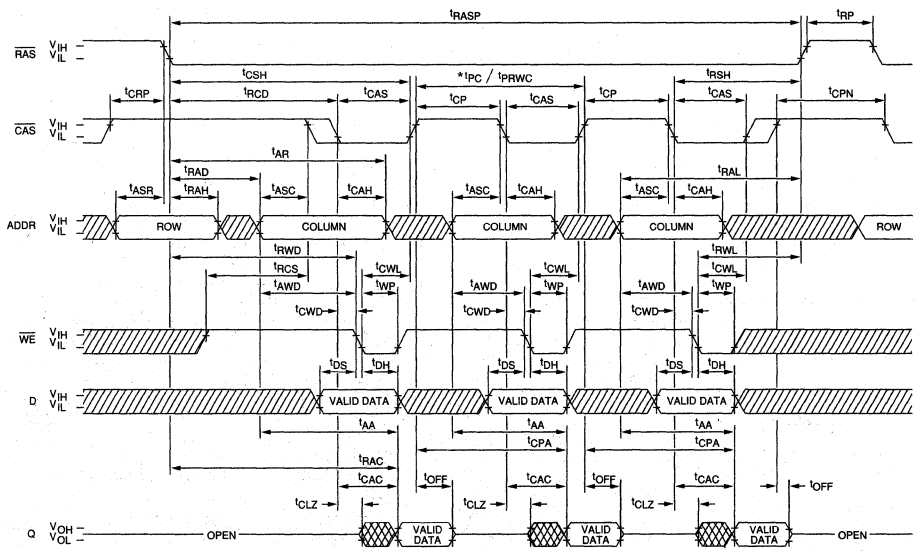
FAST-PAGE-MODE READ CYCLE



FAST-PAGE-MODE EARLY-WRITE CYCLE

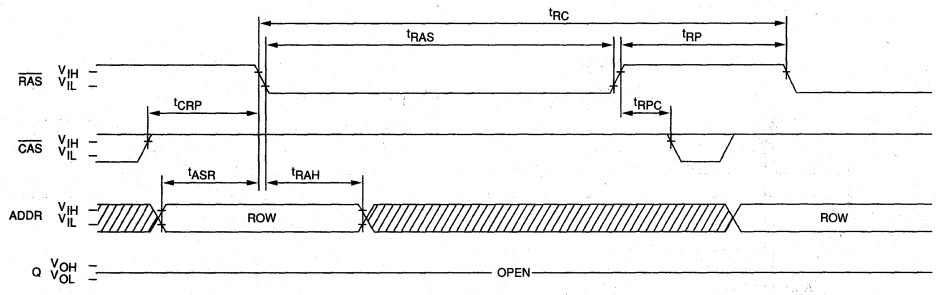


FAST-PAGE-MODE READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)

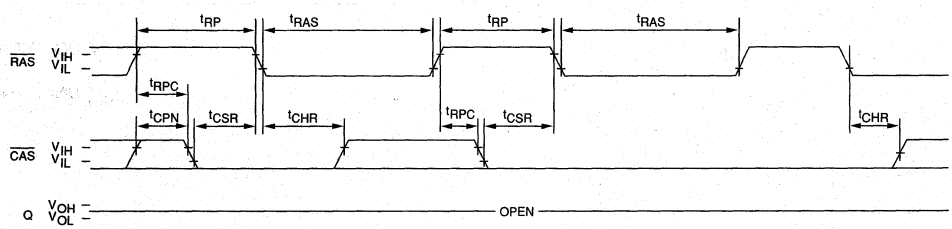


*tPC is for LATE-WRITE only.

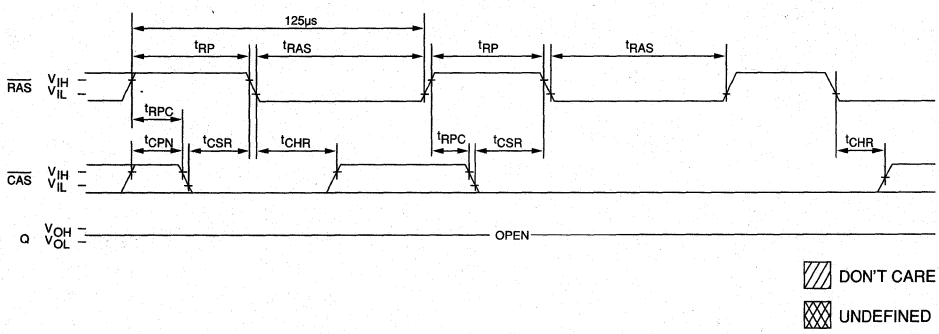
RAS-ONLY REFRESH CYCLE
(ADDR = A0-A8; A9 and WE = DON'T CARE)



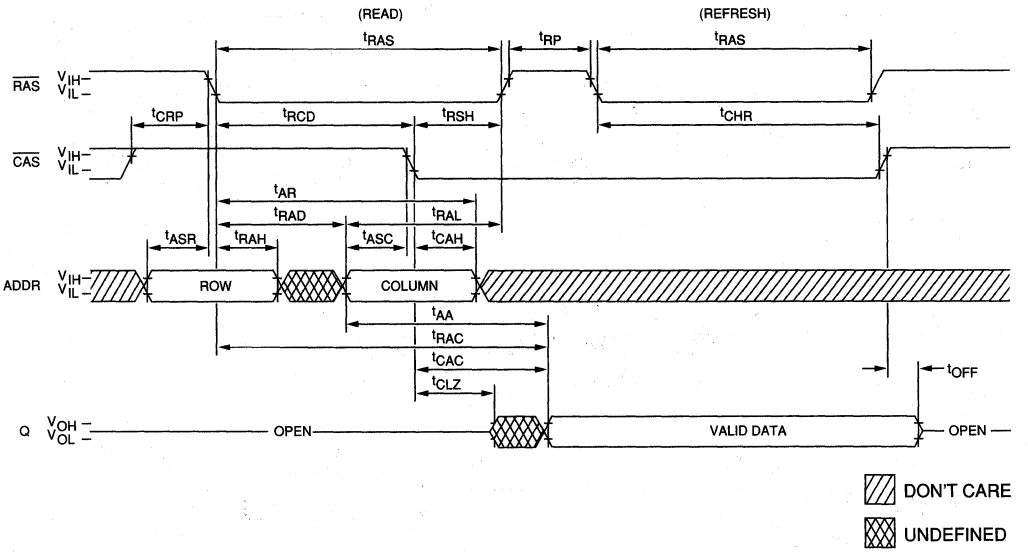
CAS-BEFORE-RAS REFRESH CYCLE
(A0-A9 and WE = DON'T CARE)



BATTERY BACKUP REFRESH CYCLE
(A0-A9 and WE = DON'T CARE)



HIDDEN REFRESH CYCLE [23]
($\overline{WE}$ = HIGH)



DRAM

1 MEG x 1 DRAM

STATIC COLUMN

FEATURES

- Industry standard x1 pinout, timing, functions and packages
- High-performance, CMOS silicon-gate process
- Single +5V ±10% power supply
- Low power, 3mW standby; 175mW active, typical
- All inputs, outputs and clocks are fully TTL compatible
- 512-cycle refresh in 8ms
- Refresh modes: $\overline{\text{RAS}}$-ONLY, $\overline{\text{CAS}}$-BEFORE-$\overline{\text{RAS}}$ (CBR), and HIDDEN
- Optional STATIC COLUMN access cycle

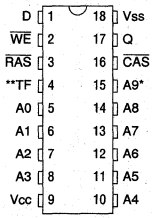
OPTIONS

	MARKING
• Timing	
70ns access	- 7
80ns access	- 8
100ns access	-10
• Packages	
Plastic DIP (300 mil)	None
Plastic SOJ (300 mil)	DJ
Plastic ZIP (350 mil)	Z

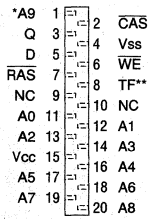
NOTE: Available in die form (commercial or military) or military ceramic packages. Please consult factory for die data sheets or refer to Micron's *Military Data Book.*

PIN ASSIGNMENT (Top View)

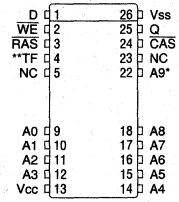
18-Pin DIP (N-1)



20-Pin ZIP (O-1)



20-Pin SOJ (Q-1)



*Address not used for $\overline{\text{RAS}}$-ONLY REFRESH
**TF = Test Function, V_{IN} must not exceed Vcc+1V for normal operation

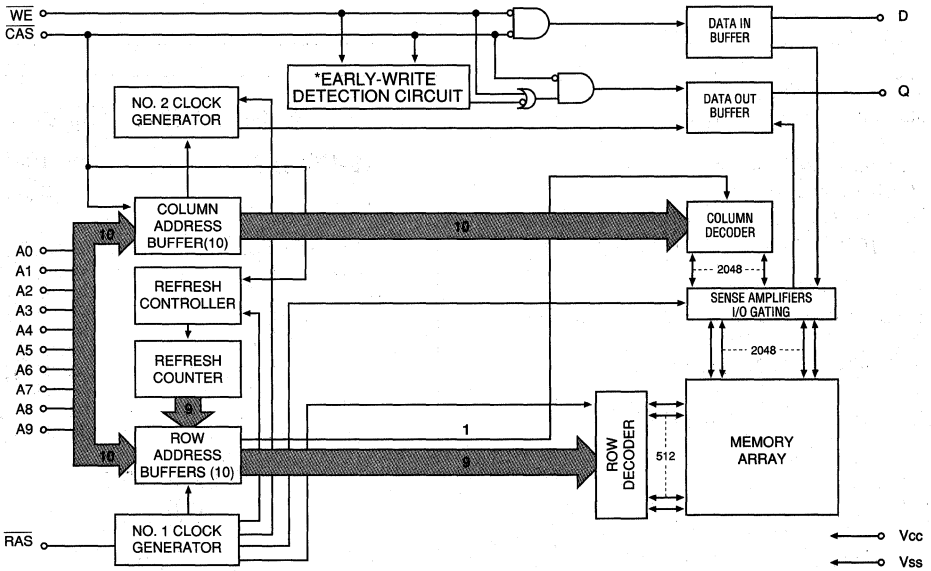
GENERAL DESCRIPTION

The MT4C1026 is a randomly accessed solid-state memory containing 1,048,576 bits organized in a x1 configuration. During READ or WRITE cycles, each bit is uniquely addressed through the 20 address bits, which are entered 10 bits (A0-A9) at a time. $\overline{\text{RAS}}$ is used to latch the first 10 bits and $\overline{\text{CAS}}$ the latter 10 bits. A READ or WRITE cycle is selected with the $\overline{\text{WE}}$ input. A logic HIGH on $\overline{\text{WE}}$ dictates READ mode while a logic LOW on $\overline{\text{WE}}$ dictates WRITE mode. During a WRITE cycle, data in (D) is latched by the falling edge of $\overline{\text{WE}}$ or $\overline{\text{CAS}}$, whichever occurs last. If $\overline{\text{WE}}$ goes LOW prior to $\overline{\text{CAS}}$ going LOW, the output pin, data out (Q), remains open (High-Z) until the next $\overline{\text{CAS}}$ cycle. If $\overline{\text{WE}}$ goes LOW after data reaches the output pin, Q is activated and retains the selected cell data as long as $\overline{\text{CAS}}$ remains LOW (regardless of $\overline{\text{WE}}$ or $\overline{\text{RAS}}$). This late $\overline{\text{WE}}$ pulse results in a READ-WRITE cycle.

STATIC COLUMN operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row address (A0-A9) defined page boundary. After the first read, any column address transition will result in new data out. Unlike the page-mode part, which requires $\overline{\text{CAS}}$ to be toggled for each successive PAGE-MODE access, the STATIC COLUMN part allows $\overline{\text{CAS}}$ to be left LOW for successive STATIC COLUMN accesses. Returning $\overline{\text{RAS}}$ HIGH terminates the STATIC COLUMN operation.

Returning $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the $\overline{\text{RAS}}$ high time. Memory cell data is retained in its correct state by maintaining power and executing any $\overline{\text{RAS}}$ cycle (READ, WRITE, $\overline{\text{RAS}}$-ONLY, $\overline{\text{CAS}}$-BEFORE-$\overline{\text{RAS}}$ (CBR) or HIDDEN refresh) so that all 512 combinations of $\overline{\text{RAS}}$ addresses (A0-A8) are executed at least every 8ms, regardless of sequence. The CBR refresh cycle will invoke the internal refresh counter for automatic $\overline{\text{RAS}}$ addressing.

FUNCTIONAL BLOCK DIAGRAM
STATIC COLUMN



*NOTE: $\overline{WE}$ LOW prior to $\overline{CAS}$ LOW, EW detection circuit output is a HIGH (EARLY-WRITE)
$\overline{CAS}$ LOW prior to $\overline{WE}$ LOW, EW detection circuit output is a LOW (LATE-WRITE)

TRUTH TABLE

FUNCTION		$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	ADDRESSES		DATA	
					^tR	^tC	D (Data In)	Q (Data Out)
Standby		H	H→X	X	X	X	Don't Care	High-Z
READ		L	L	H	ROW	COL	Don't Care	Data Out
EARLY-WRITE		L	L	L	ROW	COL	Data In	High-Z
READ-WRITE		L	L	H→L	ROW	COL	Data In	Data Out
STATIC COLUMN	1st Cycle	L	L	H	ROW	COL	Don't Care	Data Out
READ	2nd Cycle	L	L	H	n/a	COL	Don't Care	Data Out
STATIC COLUMN	1st Cycle	L	L	L	ROW	COL	Data In	High-Z
EARLY-WRITE	2nd Cycle	L	L	H→L	n/a	COL	Data In	High-Z
STATIC COLUMN	1st Cycle	L	L	H→L	ROW	COL	Data In	Data Out
READ-WRITE	2nd Cycle	L	L	H→L	n/a	COL	Data In	Data Out
$\overline{RAS}$-ONLY REFRESH		L	H	X	ROW	n/a	Don't Care	High-Z
HIDDEN	READ	L→H→L	L	H	ROW	COL	Don't Care	Data Out
REFRESH	WRITE	L→H→L	L	L	ROW	COL	Data In	High-Z
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH		H→L	L	X	X	X	Don't Care	High-Z

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Vss ..... -1V to +7V
Operating Temperature, T_A (Ambient) ..... 0°C to +70°C
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation 600mW
Soldering Temperature (Soldering 10 Seconds) ..... 260°C
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 3, 4, 6, 7) (V_{CC} = 5V ±10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.5	V	1
Input High (Logic 1) Voltage, All Inputs	V_{IH}	2.4	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, All Inputs	V_{IL}	-1.0	0.8	V	1
INPUT LEAKAGE CURRENT Any Input 0V ≤ V_{IN} ≤ 6.5V (All other pins not under test = 0V)	I_I	-2	2	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled, 0V ≤ V_{OUT} ≤ 5.5V)	I_{OZ}	-10	10	µA	
OUTPUT LEVELS Output High Voltage (I_{OUT} = -5mA)	V_{OH}	2.4		V	
Output Low Voltage (I_{OUT} = 4.2mA)	V_{OL}		0.4	V	

		MAX				
PARAMETER/CONDITION	SYMBOL	-7	-8	-10	UNITS	NOTES
STANDBY CURRENT: (TTL) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC1}	2	2	2	mA	
STANDBY CURRENT: (CMOS) ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} -0.2V)	I_{CC2}	1	1	1	mA	
OPERATING CURRENT: Random READ/WRITE Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC (MIN))	I_{CC3}	80	70	60	mA	3, 4
OPERATING CURRENT: STATIC COLUMN Average power supply current ($\overline{RAS}$ = V_{IL}; $\overline{CAS}$, Address Cycling: ^tSC = ^tSC (MIN))	I_{CC4}	60	50	40	mA	3, 4
REFRESH CURRENT: $\overline{RAS}$-ONLY Average power supply current ($\overline{RAS}$ Cycling; $\overline{CAS}$ = V_{IH}: ^tRC = ^tRC (MIN))	I_{CC5}	80	70	60	mA	3
REFRESH CURRENT: $\overline{CAS}$-BEFORE-$\overline{RAS}$ Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC (MIN))	I_{CC6}	80	70	60	mA	3, 5

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A9, D	C_{I1}		5	pF	2
Input Capacitance: $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	C_{I2}		7	pF	2
Output Capacitance: Q	C_O		7	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (V_{CC} = 5V ±10%)

AC CHARACTERISTICS		-7		-8		-10			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	t_{RC}	130		150		180		ns	
READ-WRITE cycle time	t_{RWC}	155		175		205		ns	
STATIC-COLUMN READ or WRITE cycle time	t_{SC}	40		45		55		ns	
STATIC-COLUMN READ-WRITE cycle time	t_{SRWC}	70		80		100		ns	
Access time from $\overline{RAS}$	t_{RAC}		70		80		100	ns	14
Access time from $\overline{CAS}$	t_{CAC}		20		20		25	ns	15
Access time from column address	t_{AA}		35		40		50	ns	
$\overline{RAS}$ pulse width	t_{RAS}	70	100,000	80	100,000	100	100,000	ns	
$\overline{RAS}$ pulse width (STATIC COLUMN)	t_{RASC}	70	100,000	80	100,000	100	100,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	20		20		25		ns	
$\overline{RAS}$ precharge time	t_{RP}	50		60		70		ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	100,000	20	100,000	25	100,000	ns	
$\overline{CAS}$ hold time	t_{CSH}	70		80		100		ns	
$\overline{CAS}$ precharge time	t_{CPN}	10		10		15		ns	16
$\overline{CAS}$ precharge time (STATIC COLUMN)	t_{CP}	10		10		10		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	50	20	60	25	75	ns	17
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		5		ns	
Row address setup time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	10		10		15		ns	
$\overline{RAS}$ to column address delay time	t_{RAD}	15	35	15	40	20	50	ns	18
Column address setup time	t_{ASC}	0		0		0		ns	
Column address hold time	t_{CAH}	15		15		20		ns	
Column address hold time (referenced to $\overline{RAS}$)	t_{AR}	80		90		100		ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	35		40		50		ns	
Read command setup time	t_{RCS}	0		0		0		ns	
Read command hold time (referenced to $\overline{CAS}$)	t_{RCH}	0		0		0		ns	19
Read command hold time (referenced to $\overline{RAS}$)	t_{RRH}	0		0		0		ns	19
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	0		0		0		ns	
Output buffer turn-off delay	t_{OFF}	0	20	0	20	0	20	ns	20

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

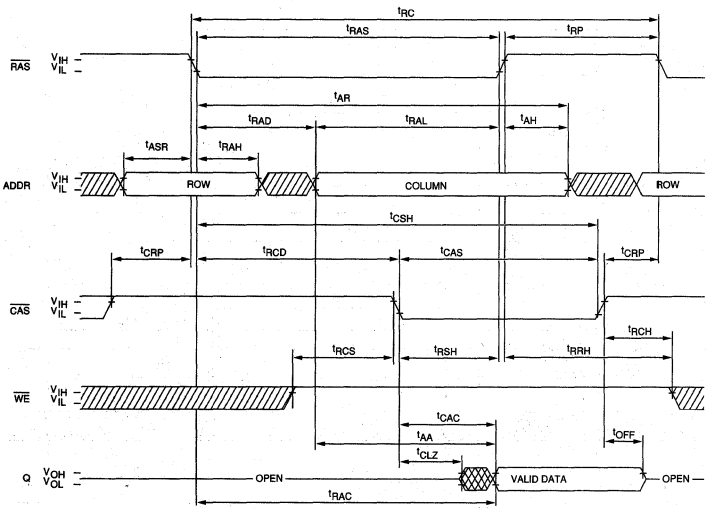
(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (V_{CC} = 5V ±10%)

AC CHARACTERISTICS		-7		-8		-10			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Column address hold time EARLY-WRITE (referenced to $\overline{RAS}$)	^tAWR	55		60		70		ns	
$\overline{WE}$ command setup time	^tWCS	0		0		0		ns	21
Write command hold time	^tWCH	15		15		20		ns	
Write command hold time (referenced to $\overline{RAS}$)	^tWCR	55		60		75		ns	
Write command pulse width	^tWP	15		15		20		ns	
Write command to $\overline{RAS}$ lead time	^tRWL	20		20		25		ns	
Write command to $\overline{CAS}$ lead time	^tCWL	20		20		25		ns	
Data-in setup time	^tDS	0		0		0		ns	22
Data-in hold time	^tDH	15		15		20		ns	22
Data-in hold time (referenced to $\overline{RAS}$)	^tDHR	55		60		75		ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	^tRWD	70		80		100		ns	21
Column address to $\overline{WE}$ delay time	^tAWD	35		40		50		ns	21
$\overline{CAS}$ to $\overline{WE}$ delay time	^tCWD	20		20		25		ns	21
Transition time (rise or fall)	^tT	3	50	3	50	3	50	ns	9, 10
Refresh period (512 cycles)	^tREF		8		8		8	ms	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	^tRPC	0		0		0		ns	
$\overline{CAS}$ setup time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tCSR	10		10		10		ns	5
$\overline{CAS}$ hold time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tCHR	15		15		15		ns	5
Write inactive time	^tWI	10		10		10		ns	
Previous WRITE to column address delay time	^tLWAD	20	30	20	35	25	45	ns	
Previous WRITE to column address hold time	^tAHLW	65		75		95		ns	
Output data hold time from column address	^tAOH	5		5		5		ns	
Output data enable from WRITE	^tOW	^tAA + 5		^tAA + 5		^tAA + 5		ns	
Access time from last WRITE	^tALW	65		75		95		ns	
Column address hold time referenced to $\overline{RAS}$ HIGH	^tAH	5		5		10		ns	
$\overline{CAS}$ pulse width in STATIC-COLUMN mode	^tCSC	^tCAS		^tCAS		^tCAS		ns	
Output data hold from WRITE	^tWOH	0		0		0		ns	

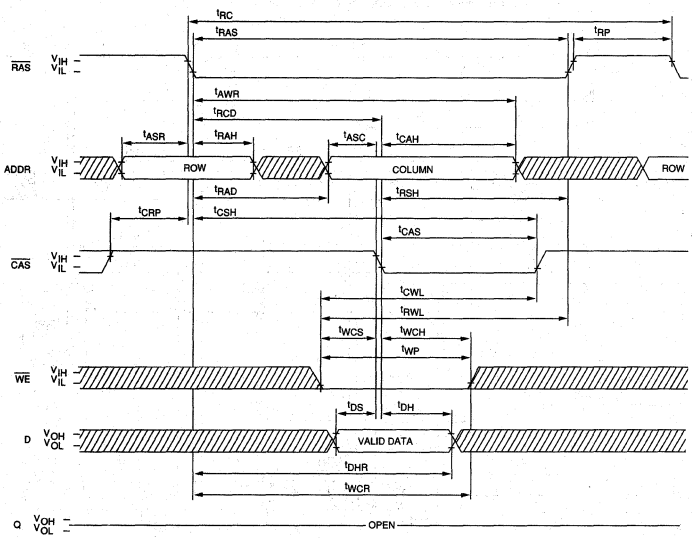
NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. V_{CC} = 5V ±10%, f = 1 MHz.
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is assured.
7. An initial pause of 100µs is required after power-up followed by any eight $\overline{RAS}$ cycles before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-up should be repeated any time the ^{t}REF refresh requirement is exceeded.
8. AC characteristics assume ^{t}T = 5ns.
9. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS}$ = V_{IH}, data output is High-Z.
12. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to 2 TTL gates and 100pF.
14. Assumes that $^{t}RCD < {}^{t}RCD$ (MAX). If ^{t}RCD is greater than the maximum recommended value shown in this table, ^{t}RAC will increase by the amount that ^{t}RCD exceeds the value shown.
15. Assumes that $^{t}RCD \geq {}^{t}RCD$ (MAX).
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer, $\overline{CAS}$ must be pulsed HIGH for ^{t}CPN.
17. Operation within the ^{t}RCD (MAX) limit ensures that ^{t}RAC (MAX) can be met. ^{t}RCD (MAX) is specified as a reference point only; if ^{t}RCD is greater than the specified ^{t}RCD (MAX) limit, then access time is controlled exclusively by ^{t}CAC.
18. Operation within the ^{t}RAD (MAX) limit ensures that ^{t}RAC (MIN) and ^{t}CAC (MIN) can be met. ^{t}RAD (MAX) is specified as a reference point only; if ^{t}RAD is greater than the specified ^{t}RAD (MAX) limit, then access time is controlled exclusively by ^{t}AA.
19. Either ^{t}RCH or ^{t}RRH must be satisfied for a READ cycle.
20. ^{t}OFF (MAX) defines the time at which the output achieves the open circuit condition, and is not referenced to V_{OH} or V_{OL}.
21. ^{t}WCS, ^{t}RWD, ^{t}AWD and ^{t}CWD are restrictive operating parameters in LATE-WRITE, and READ-MODIFY-WRITE cycles only. If $^{t}WCS \geq {}^{t}WCS$ (MIN), the cycle is an EARLY-WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If $^{t}RWD \geq {}^{t}RWD$ (MIN), $^{t}AWD \geq {}^{t}AWD$ (MIN) and $^{t}CWD \geq {}^{t}CWD$ (MIN), the cycle is a READ-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the cycle is a LATE-WRITE and the state of Q is indeterminate (at access time and until $\overline{CAS}$ goes back to V_{IH}).
22. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY-WRITE cycles and $\overline{WE}$ leading edge in LATE-WRITE or READ-MODIFY-WRITE cycles.
23. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW.

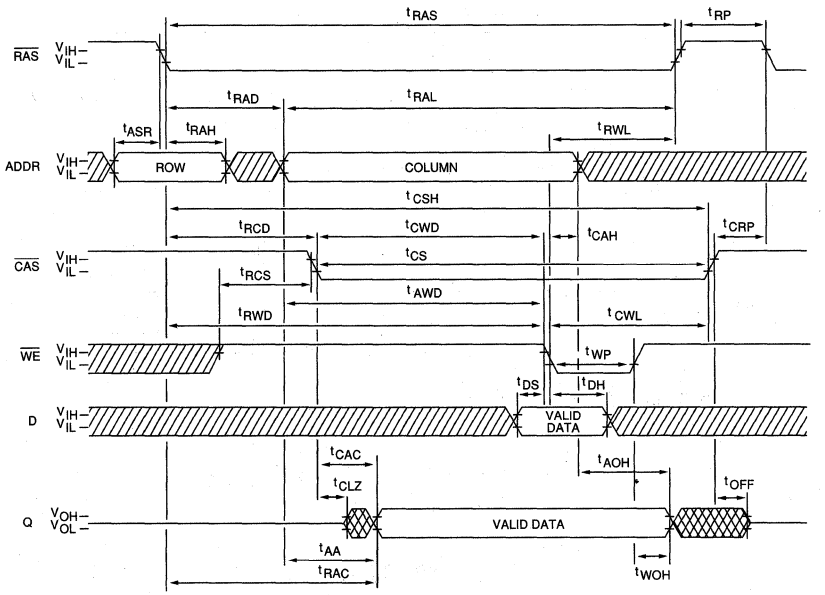
READ CYCLE



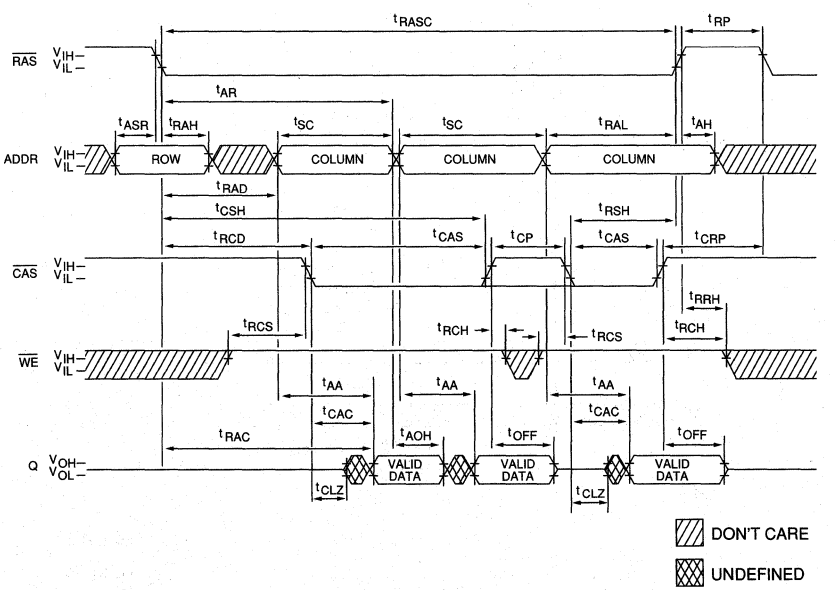
EARLY-WRITE CYCLE



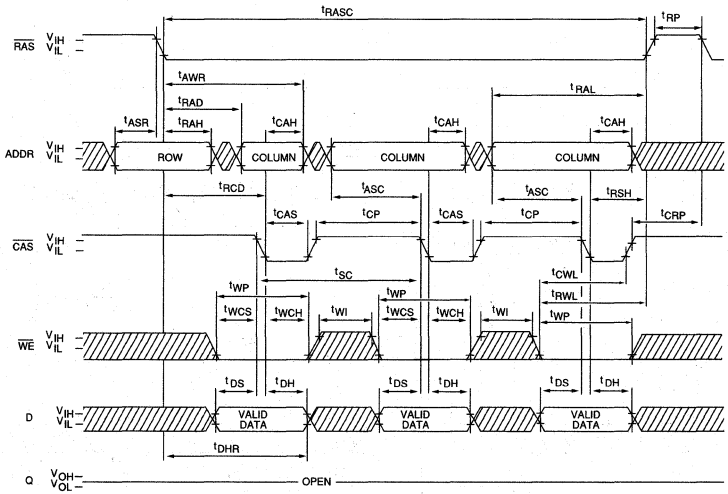
READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)



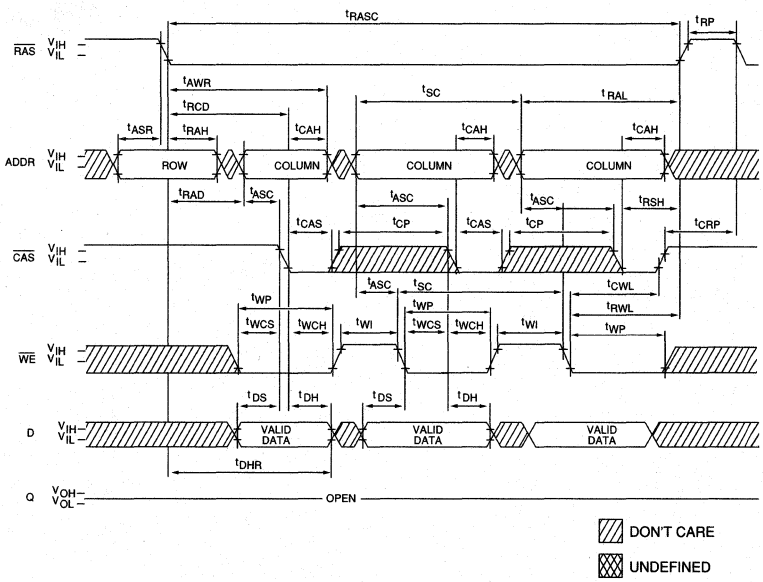
STATIC-COLUMN READ CYCLE



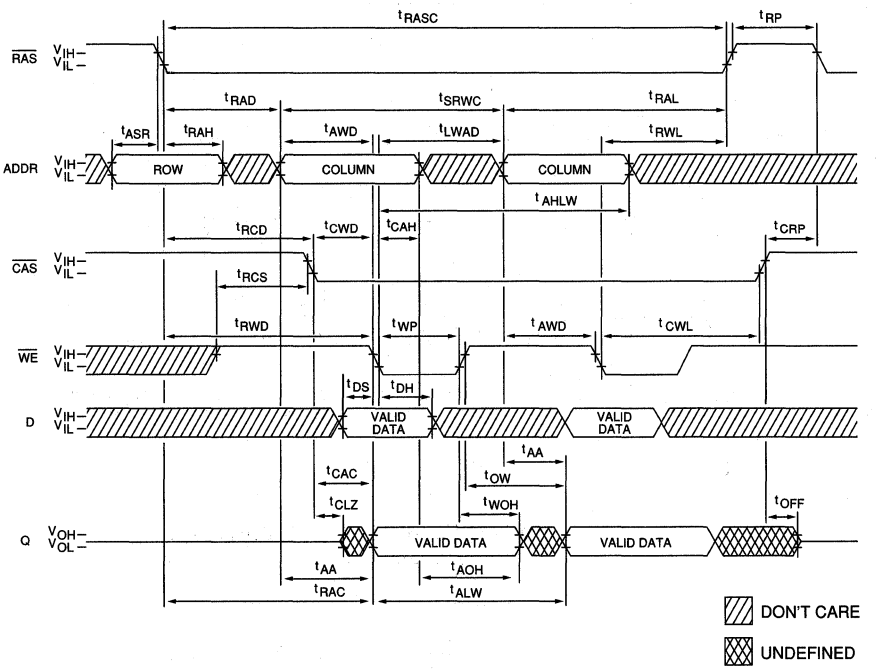
STATIC-COLUMN EARLY-WRITE CYCLE
(CAS Controlled)



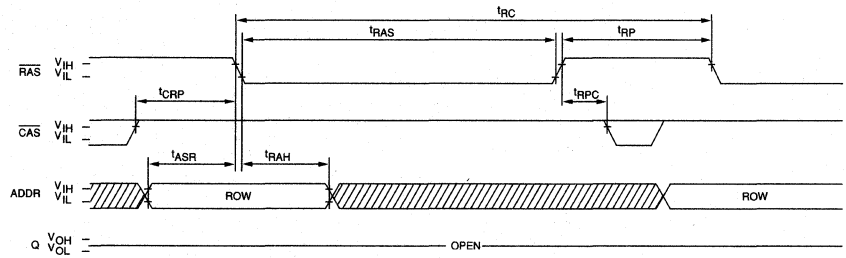
STATIC-COLUMN EARLY-WRITE CYCLE
(WE Controlled)



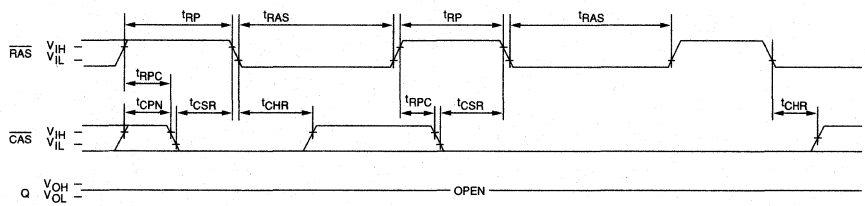
STATIC-COLUMN READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)



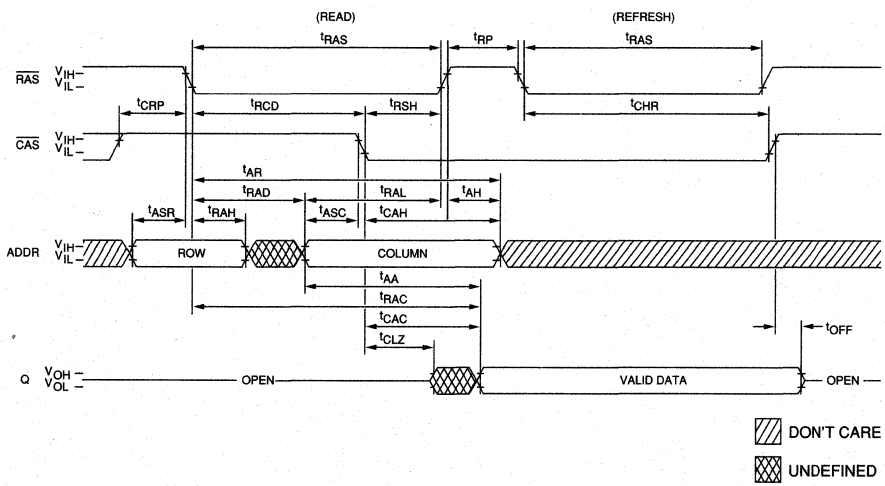
RAS-ONLY REFRESH CYCLE
(ADDR = A0-A8; A9 and WE = DON'T CARE)



CAS-BEFORE-RAS REFRESH CYCLE
(A0-A9 and WE = DON'T CARE)



HIDDEN REFRESH CYCLE [23]
(WE = HIGH)



DRAM

4 MEG x 1 DRAM

FAST PAGE MODE

FEATURES

- Industry standard x1 pinout, timing, functions and packages
- High-performance, CMOS silicon-gate process
- Single +5V ±10% power supply
- Low power, 3mW standby; 225mW active, typical
- All inputs, outputs and clocks are fully TTL compatible
- 1,024-cycle refresh distributed across 16ms
- Refresh modes: $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$ (CBR) and HIDDEN
- FAST PAGE MODE access cycle

OPTIONS — MARKING

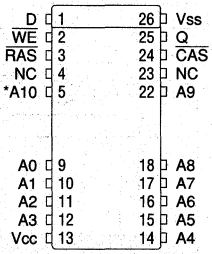
- Timing
  - 60ns access — -6
  - 70ns access — -7
  - 80ns access — -8
- Packages
  - Plastic SOJ (300 mil) — DJ
  - Plastic TSOP (300 mil)** — TG
  - Plastic ZIP (350 mil) — Z

NOTE: Available in die form (commercial or military) or military ceramic packages. Please consult factory for die data sheets or refer to Micron's *Military Data Book*.

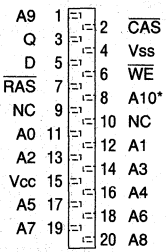
- Operating Temperature, T_A
  - Commercial (0°C to +70°C) — None
  - Industrial (-40°C to +85°C) — IT
- Part Number Example: MT4C1004JDJ-6

PIN ASSIGNMENT (Top View)

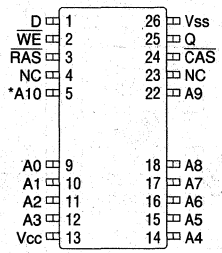
20-Pin SOJ (Q-1)



20-Pin ZIP (O-1)



20-Pin TSOP (R-1)



*Address not used for $\overline{RAS}$-ONLY REFRESH
**Consult factory on availability of reverse pinout TSOP packages

GENERAL DESCRIPTION

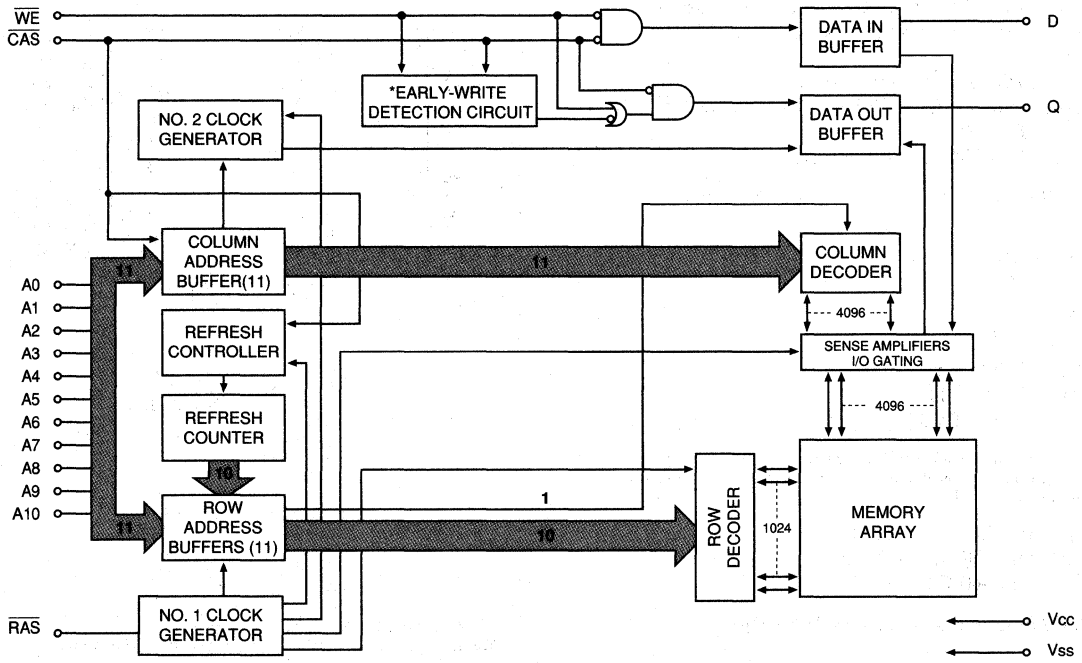
The MT4C1004J is a randomly accessed solid-state memory containing 4,194,304 bits organized in a x1 configuration. During READ or WRITE cycles, each bit is uniquely addressed through the 22 address bits, which are entered 11 bits (A0-A10) at a time. $\overline{RAS}$ is used to latch the first 11 bits and $\overline{CAS}$ the latter 11 bits. READ and WRITE cycles are selected with the $\overline{WE}$ input. A logic HIGH on $\overline{WE}$ dictates READ mode while a logic LOW on $\overline{WE}$ dictates WRITE mode. During a WRITE cycle, data in (D) is latched by the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. If $\overline{WE}$ goes LOW prior to $\overline{CAS}$ going LOW, the output pin remains open (High-Z) until the next $\overline{CAS}$ cycle. If $\overline{WE}$ goes LOW after data reaches the output pin, data out (Q) is activated and retains the selected cell data as long as $\overline{CAS}$ remains LOW (regardless of $\overline{WE}$ or $\overline{RAS}$). This late $\overline{WE}$ pulse results in a READ-WRITE cycle.

FAST PAGE MODE operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row address (A0-A10) defined page boundary. The FAST PAGE MODE cycle is always initiated with a row address strobed-in by $\overline{RAS}$ followed by a column address strobed-in by $\overline{CAS}$. $\overline{CAS}$ may be toggled-in by holding $\overline{RAS}$ LOW and strobing-in different column addresses, thus executing faster memory cycles. Returning $\overline{RAS}$ HIGH terminates the FAST PAGE MODE operation.

Returning $\overline{RAS}$ and $\overline{CAS}$ HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the

$\overline{RAS}$ high time. Memory cell data is retained in its correct state by maintaining power and executing any $\overline{RAS}$ cycle (READ, WRITE, $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$ (CBR), or HIDDEN refresh) so that all 1,024 combinations of $\overline{RAS}$ addresses (A0-A9) are executed at least every 16ms, regardless of sequence. The CBR cycle will invoke the internal refresh counter for automatic $\overline{RAS}$ addressing.

FUNCTIONAL BLOCK DIAGRAM
FAST PAGE MODE



*NOTE: $\overline{WE}$ LOW prior to $\overline{CAS}$ LOW, EW detection circuit output is a HIGH (EARLY-WRITE)
$\overline{CAS}$ LOW prior to $\overline{WE}$ LOW, EW detection circuit output is a LOW (LATE-WRITE)

TRUTH TABLE

FUNCTION		RAS	CAS	WE	ADDRESSES		DATA	
					^tR	^tC	D (Data In)	Q (Data Out)
Standby		H	H→X	X	X	X	Don't Care	High-Z
READ		L	L	H	ROW	COL	Don't Care	Data Out
EARLY-WRITE		L	L	L	ROW	COL	Data In	High-Z
READ-WRITE		L	L	H→L	ROW	COL	Data In	Data Out
FAST-PAGE-MODE	1st Cycle	L	H→L	H	ROW	COL	Don't Care	Data Out
READ	2nd Cycle	L	H→L	H	n/a	COL	Don't Care	Data Out
FAST-PAGE-MODE	1st Cycle	L	H→L	L	ROW	COL	Data In	High-Z
EARLY-WRITE	2nd Cycle	L	H→L	L	n/a	COL	Data In	High-Z
FAST-PAGE-MODE	1st Cycle	L	H→L	H→L	ROW	COL	Data In	Data Out
READ-WRITE	2nd Cycle	L	H→L	H→L	n/a	COL	Data In	Data Out
RAS-ONLY REFRESH		L	H	X	ROW	n/a	Don't Care	High-Z
HIDDEN	READ	L→H→L	L	H	ROW	COL	Don't Care	Data Out
REFRESH	WRITE	L→H→L	L	L	ROW	COL	Data In	High-Z
CAS-BEFORE-RAS REFRESH		H→L	L	H	X	X	Don't Care	High-Z

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to V_{SS} ..... -1V to +7V
Operating Temperature, T_A (Ambient) ..... 0°C to +70°C
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 3, 4, 6, 7) (0°C ≤ T_A ≤ 70°C; V_{CC} = 5V ±10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.5	V	1
Input High (Logic 1) Voltage, All Inputs	V_{IH}	2.4	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, All Inputs	V_{IL}	-1.0	0.8	V	1
INPUT LEAKAGE CURRENT Any Input 0V ≤ V_{IN} ≤ 6.5V (All other pins not under test = 0V)	I_I	-2	2	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled, 0V ≤ V_{OUT} ≤ 5.5V)	I_{OZ}	-10	10	µA	
OUTPUT LEVELS Output High Voltage (I_{OUT} = -5mA)	V_{OH}	2.4		V	
Output Low Voltage (I_{OUT} = 4.2mA)	V_{OL}		0.4	V	

		MAX				
PARAMETER/CONDITION	SYMBOL	-6	-7	-8	UNITS	NOTES
STANDBY CURRENT: (TTL) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC1}	2	2	2	mA	
STANDBY CURRENT: (CMOS) ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} -0.2V)	I_{CC2}	1	1	1	mA	
OPERATING CURRENT: Random READ/WRITE Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC (MIN))	I_{CC3}	110	100	90	mA	3, 4
OPERATING CURRENT: FAST PAGE MODE Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: ^tPC = ^tPC (MIN))	I_{CC4}	80	70	60	mA	3, 4
REFRESH CURRENT: $\overline{RAS}$-ONLY Average power supply current ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}: ^tRC = ^tRC (MIN))	I_{CC5}	110	100	90	mA	3
REFRESH CURRENT: $\overline{CAS}$-BEFORE-$\overline{RAS}$ Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC (MIN))	I_{CC6}	110	100	90	mA	3, 5

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A10, D	C_{I1}		5	pF	2
Input Capacitance: $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	C_{I2}		7	pF	2
Output Capacitance: Q	C_O		7	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (V_{CC} = 5V ±10%)

AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	^tRC	110		130		150		ns	
READ-WRITE cycle time	^tRWC	135		155		175		ns	
FAST-PAGE-MODE READ or WRITE cycle time	^tPC	40		40		45		ns	
FAST-PAGE-MODE READ-WRITE cycle time	^tPRWC	60		65		70		ns	
Access time from $\overline{RAS}$	^tRAC		60		70		80	ns	14
Access time from $\overline{CAS}$	^tCAC		15		20		20	ns	15
Access time from column address	^tAA		30		35		40	ns	
Access time from $\overline{CAS}$ precharge	^tCPA		35		40		45	ns	
$\overline{RAS}$ pulse width	^tRAS	60	100,000	70	100,000	80	100,000	ns	
$\overline{RAS}$ pulse width (FAST PAGE MODE)	^tRASP	60	100,000	70	100,000	80	100,000	ns	
$\overline{RAS}$ hold time	^tRSH	15		20		20		ns	
$\overline{RAS}$ precharge time	^tRP	40		50		60		ns	
$\overline{CAS}$ pulse width	^tCAS	15	100,000	20	100,000	20	100,000	ns	
$\overline{CAS}$ hold time	^tCSH	60		70		80		ns	
$\overline{CAS}$ precharge time	^tCPN	10		10		10		ns	16
$\overline{CAS}$ precharge time (FAST PAGE MODE)	^tCP	10		10		10		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	^tRCD	20	45	20	50	20	60	ns	17
$\overline{CAS}$ to $\overline{RAS}$ precharge time	^tCRP	10		10		10		ns	
Row address setup time	^tASR	0		0		0		ns	
Row address hold time	^tRAH	10		10		10		ns	
$\overline{RAS}$ to column address delay time	^tRAD	15	30	15	35	15	40	ns	18
Column address setup time	^tASC	0		0		0		ns	
Column address hold time	^tCAH	10		15		15		ns	
Column address hold time (referenced to $\overline{RAS}$)	^tAR	50		55		60		ns	
Column address to $\overline{RAS}$ lead time	^tRAL	30		35		40		ns	
Read command setup time	^tRCS	0		0		0		ns	
Read command hold time (referenced to $\overline{CAS}$)	^tRCH	0		0		0		ns	19
Read command hold time (referenced to $\overline{RAS}$)	^tRRH	0		0		0		ns	19
$\overline{CAS}$ to output in Low-Z	^tCLZ	0		0		0		ns	
Output buffer turn-off delay	^tOFF	0	15	0	20	0	20	ns	20
$\overline{WE}$ command setup time	^tWCS	0		0		0		ns	21

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

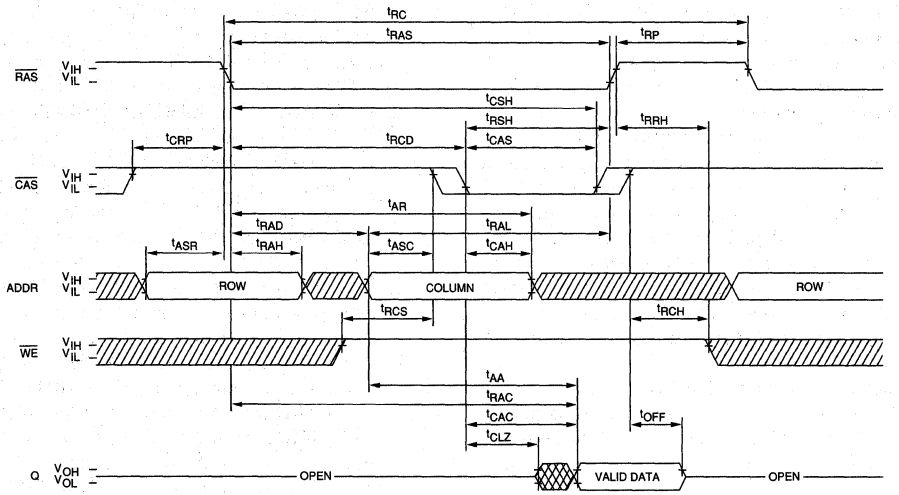
(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (V_{CC} = 5V ±10%)

AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Write command hold time	^tWCH	10		15		15		ns	
Write command hold time (referenced to $\overline{RAS}$)	^tWCR	45		55		60		ns	
Write command pulse width	^tWP	10		15		15		ns	
Write command to $\overline{RAS}$ lead time	^tRWL	15		20		20		ns	
Write command to $\overline{CAS}$ lead time	^tCWL	15		20		20		ns	
Data-in setup time	^tDS	0		0		0		ns	22
Data-in hold time	^tDH	10		15		15		ns	22
Data-in hold time (referenced to $\overline{RAS}$)	^tDHR	45		55		60		ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	^tRWD	60		70		80		ns	21
Column address to $\overline{WE}$ delay time	^tAWD	30		35		40		ns	21
$\overline{CAS}$ to $\overline{WE}$ delay time	^tCWD	15		15		20		ns	21
Transition time (rise or fall)	^tT	3	50	3	50	3	50	ns	9, 10
Refresh period (1024 cycles)	^tREF		16		16		16	ms	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	^tRPC	0		0		0		ns	
$\overline{CAS}$ setup time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tCSR	10		10		10		ns	5
$\overline{CAS}$ hold time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tCHR	15		15		15		ns	5
$\overline{WE}$ hold time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tWRH	10		10		10		ns	24, 25
$\overline{WE}$ setup time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tWRP	10		10		10		ns	24, 25
$\overline{WE}$ hold time (WCBR test cycle)	^tWTH	10		10		10		ns	24, 25
$\overline{WE}$ setup time (WCBR test cycle)	^tWTS	10		10		10		ns	24, 25

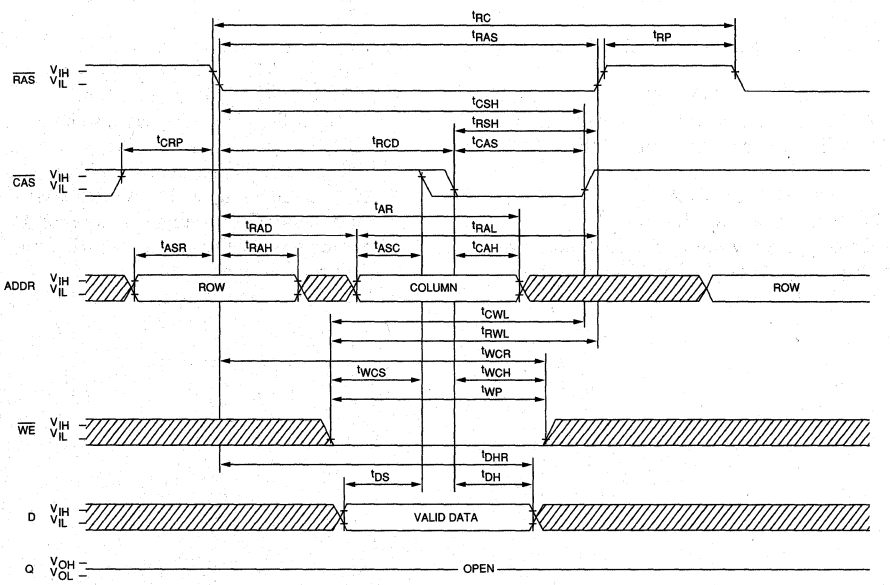
NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. V_{CC} = 5V ±10%, f = 1 MHz.
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \le T_A \le 70°C$) is assured.
7. An initial pause of 100µs is required after power-up followed by eight $\overline{RAS}$ refresh cycles ($\overline{RAS}$-ONLY or CBR with $\overline{WE}$ HIGH) before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-up should be repeated any time the ^tREF refresh requirement is exceeded.
8. AC characteristics assume ^tT = 5ns.
9. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS}$ = V_{IH}, data output is High-Z.
12. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to 2 TTL gates and 100pF.
14. Assumes that $^tRCD < {}^tRCD$ (MAX). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
15. Assumes that $^tRCD \ge {}^tRCD$ (MAX).
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer, $\overline{CAS}$ must be pulsed HIGH for ^tCPN.
17. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (MAX) limit, then access time is controlled exclusively by ^tCAC.
18. Operation within the ^tRAD (MAX) limit ensures that ^tRAC (MIN) and ^tCAC (MIN) can be met. ^tRAD (MAX) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (MAX) limit, then access time is controlled exclusively by ^tAA.
19. Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
20. ^tOFF (MAX) defines the time at which the output achieves the open circuit condition, and is not referenced to V_{OH} or V_{OL}.
21. ^tWCS, ^tRWD, ^tAWD and ^tCWD are restrictive operating parameters in LATE-WRITE, READ-WRITE and READ-MODIFY-WRITE cycles only. If $^tWCS \ge {}^tWCS$ (MIN), the cycle is an EARLY-WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If $^tRWD \ge {}^tRWD$ (MIN), $^tAWD \ge {}^tAWD$ (MIN) and $^tCWD \ge {}^tCWD$ (MIN), the cycle is a READ-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the cycle is a LATE-WRITE and the state of Q is indeterminate (at access time and until $\overline{CAS}$ goes back to V_{IH}).
22. These parameters are referenced to $\overline{CAS}$ leading edge in early WRITE cycles and $\overline{WE}$ leading edge in late WRITE or READ-WRITE cycles.
23. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW.
24. ^tWTS and ^tWTH are set up and hold specifications for the $\overline{WE}$ pin being held LOW to enable the JEDEC test mode (with CBR timing constraints). These two parameters are the inverts of ^tWRP and ^tWRH in the CBR refresh cycle.
25. JEDEC test mode only.

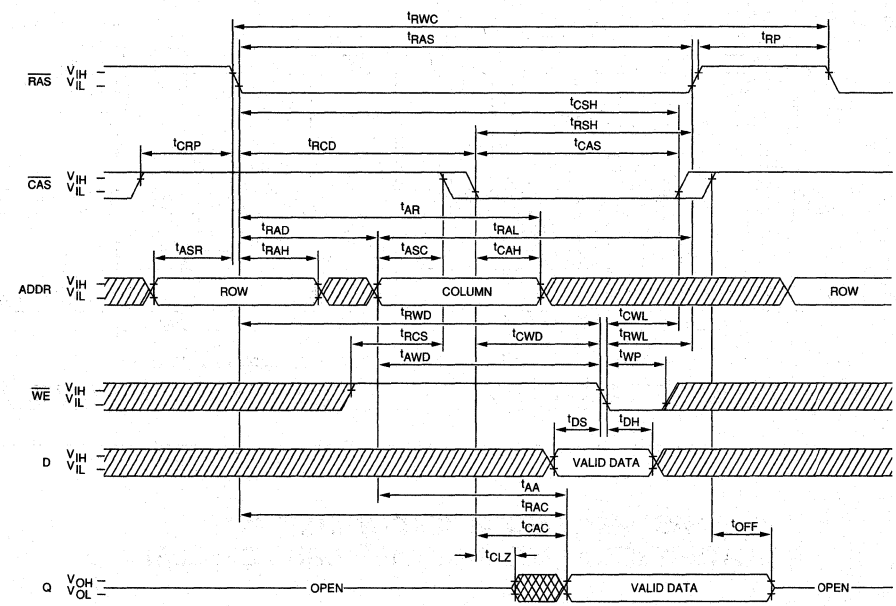
READ CYCLE



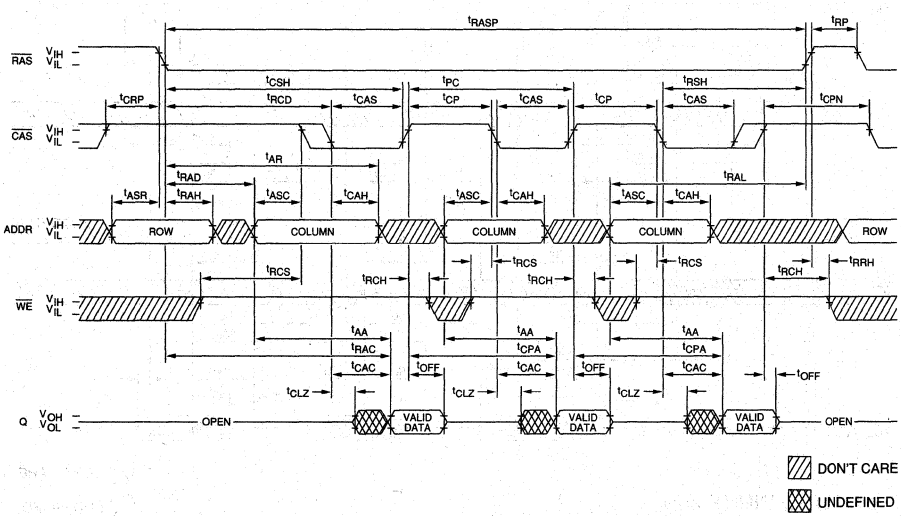
EARLY-WRITE CYCLE



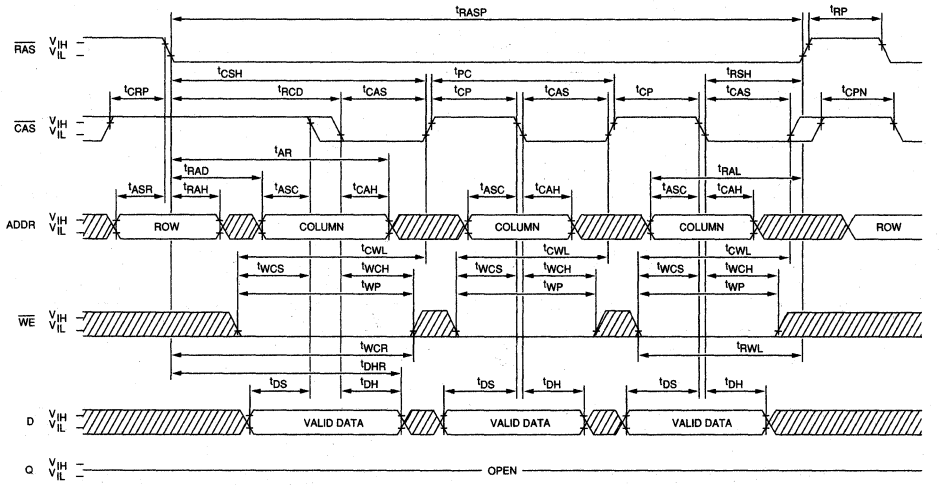
READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)



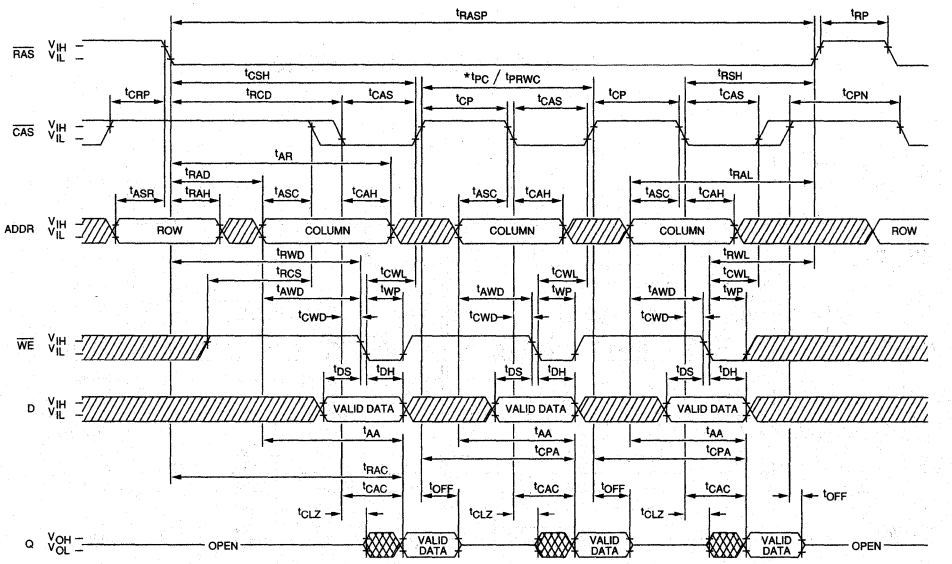
FAST-PAGE-MODE READ CYCLE



FAST-PAGE-MODE EARLY-WRITE CYCLE

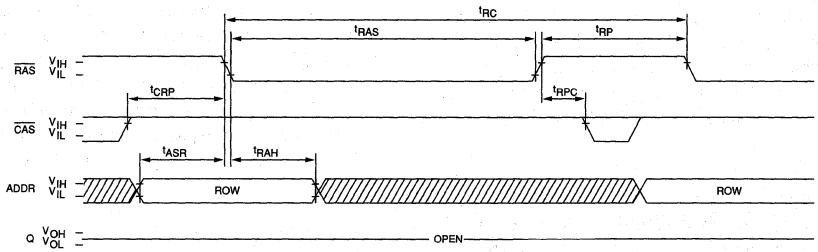


FAST-PAGE-MODE READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)

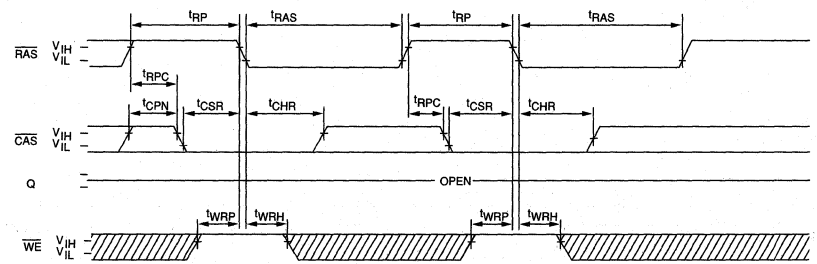


*tPC is for LATE-WRITE only.

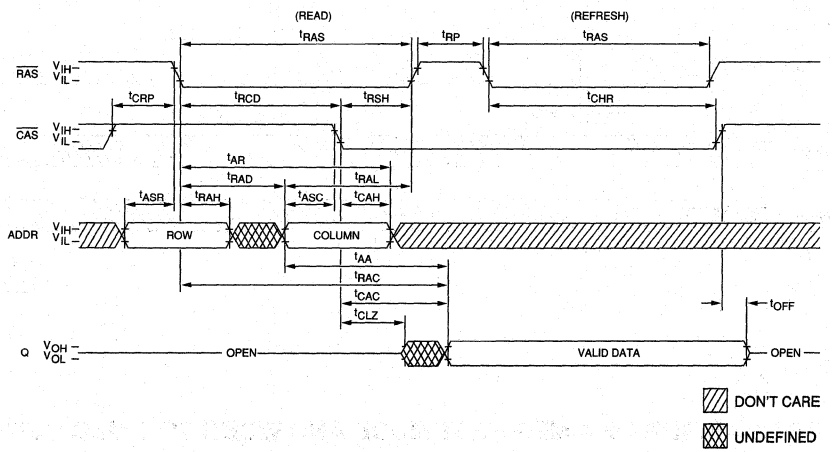
$\overline{RAS}$-ONLY REFRESH CYCLE
(ADDR = A0-A9; A10 and $\overline{WE}$ = DON'T CARE)



$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE
(A0-A10 = DON'T CARE)



HIDDEN REFRESH CYCLE [23]
($\overline{WE}$ = HIGH)



4 MEG POWER-UP AND REFRESH CONSTRAINTS

The EIA/JEDEC 4 Meg DRAM introduces two potential incompatibilities compared to the previous generation 1 Meg DRAM. The incompatibilities involve refresh and power-up. Understanding these incompatibilities and providing for them will offer the designer and system user greater compatibility between the 1 Meg and 4 Meg.

REFRESH

The most commonly used refresh mode of the 1 Meg is the CBR ($\overline{CAS}$-BEFORE-$\overline{RAS}$) REFRESH cycle. The CBR for the 1 Meg specifies the $\overline{WE}$ pin as a "don't care." The 4 Meg, on the other hand, specifies the CBR REFRESH mode with the $\overline{WE}$ pin held at a voltage HIGH level.

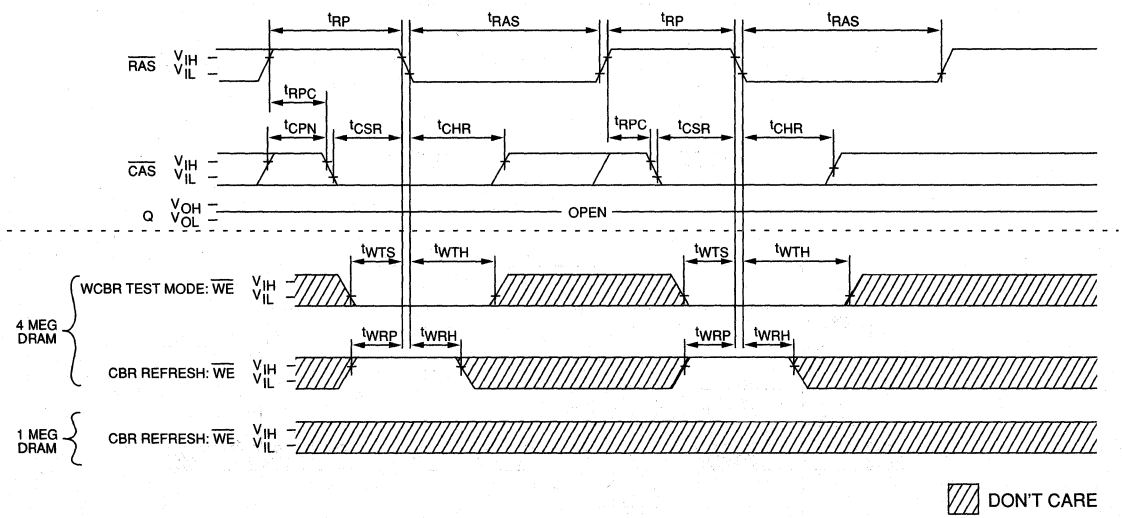
A CBR cycle with $\overline{WE}$ LOW will put the 4 Meg into the JEDEC specified test mode (WCBR).

POWER-UP

The 4 Meg JEDEC test mode constraint may introduce another problem. The 1 Meg POWER-UP cycle requires a 100µs delay followed by any eight $\overline{RAS}$ cycles. The 4 Meg POWER-UP is more restrictive in that eight $\overline{RAS}$-ONLY or CBR REFRESH ($\overline{WE}$ held HIGH) cycles must be used. The restriction is needed since the 4 Meg may power-up in the JEDEC specified test mode and must exit out of the test mode. The only way to exit the 4 Meg JEDEC test mode is with either a $\overline{RAS}$-ONLY or a CBR REFRESH cycle ($\overline{WE}$ held HIGH).

SUMMARY

1. The 1 Meg CBR REFRESH allows the $\overline{WE}$ pin to be "don't care" while the 4 Meg CBR requires $\overline{WE}$ to be HIGH.
2. The eight $\overline{RAS}$ wake-up cycles on the 1 Meg may be any valid $\overline{RAS}$ cycle while the 4 Meg may only use $\overline{RAS}$-ONLY or CBR REFRESH cycles ($\overline{WE}$ held HIGH).



COMPARISON OF 4 MEG TEST MODE AND WCBR TO 1 MEG CBR

NEW ■ DRAM

DRAM

4 MEG x 1 DRAM

LOW POWER, EXTENDED REFRESH

FEATURES

- Industry standard x1 pinout, timing, functions and packages
- High-performance, CMOS silicon-gate process
- Single +5V ±10% power supply
- All inputs, outputs and clocks are fully TTL compatible
- Refresh modes: $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$ (CBR), BATTERY BACKUP (BBU) and HIDDEN
- FAST PAGE MODE access cycle
- 1,024-cycle extended refresh distributed across 128ms
- Low power, 1mW standby; 225mW active, typical

OPTIONS — MARKING

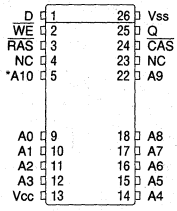
- Timing
  - 60ns access — -6
  - 70ns access — -7
  - 80ns access — -8
- Packages
  - Plastic SOJ (300 mil) — DJ
  - Plastic TSOP (300 mil)** — TG
  - Plastic ZIP (350 mil) — Z

NOTE: Available in die form (commercial or military) or military ceramic packages. Please consult factory for die data sheets or refer to Micron's *Military Data Book*.

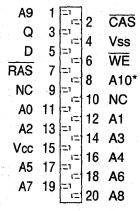
- Part Number Example: MT4C1004JDJ-6 L

PIN ASSIGNMENT (Top View)

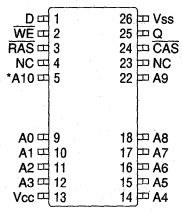
20-Pin SOJ (Q-1)



20-Pin ZIP (O-1)



20-Pin TSOP (R-1)



*Address not used for $\overline{RAS}$-ONLY REFRESH
**Consult factory on availability of reverse pinout TSOP packages

GENERAL DESCRIPTION

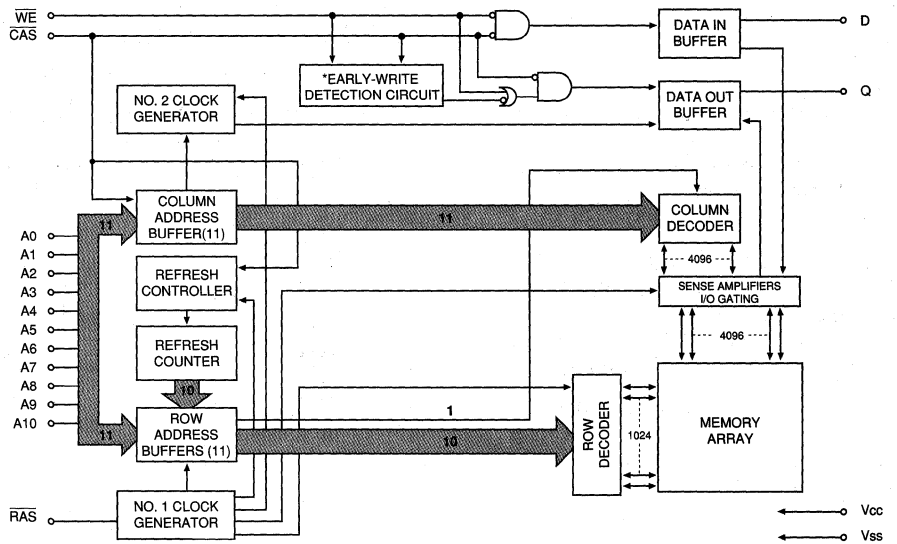
The MT4C1004J L is a randomly accessed solid-state memory containing 4,194,304 bits organized in a x1 configuration. During READ or WRITE cycles, each bit is uniquely addressed through the 22 address bits, which are entered 11 bits (A0-A10) at a time. $\overline{RAS}$ is used to latch the first 11 bits and $\overline{CAS}$ the latter 11 bits. READ and WRITE cycles are selected with the $\overline{WE}$ input. A logic HIGH on $\overline{WE}$ dictates READ mode while a logic LOW on $\overline{WE}$ dictates WRITE mode. During a WRITE cycle, data in (D) is latched by the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. If $\overline{WE}$ goes LOW prior to $\overline{CAS}$ going LOW, the output pin remains open (High-Z) until the next $\overline{CAS}$ cycle. If $\overline{WE}$ goes LOW after data reaches the output pin, data out (Q) is activated and retains the selected cell data as long as $\overline{CAS}$ remains LOW regardless of $\overline{WE}$ or $\overline{RAS}$). This late $\overline{WE}$ pulse results in a READ-WRITE cycle.

FAST PAGE MODE operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row address (A0-A10) defined page boundary. The FAST PAGE MODE cycle is always initiated with a row address strobed-in by $\overline{RAS}$ followed by a column address strobed-in by $\overline{CAS}$. $\overline{CAS}$ may be toggled-in by holding $\overline{RAS}$ LOW and strobing-in different column addresses, thus executing faster memory cycles. Returning $\overline{RAS}$ HIGH terminates the FAST PAGE MODE operation.

Returning $\overline{RAS}$ and $\overline{CAS}$ HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the $\overline{RAS}$ high time. Memory cell data is retained in its correct state by maintaining power and executing any $\overline{RAS}$ cycle (READ, WRITE, $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$ (CBR), BATTERY BACKUP or HIDDEN refresh) so that all 1,024 combinations of $\overline{RAS}$ addresses (A0-A9) are executed at least every 128ms, regardless of sequence. The CBR and BATTERY BACKUP cycles will invoke the internal refresh counter for automatic $\overline{RAS}$ addressing.

The MT4C1004J L contains the EIA/JEDEC defined test mode.

FUNCTIONAL BLOCK DIAGRAM
FAST PAGE MODE



*NOTE: $\overline{WE}$ LOW prior to $\overline{CAS}$ LOW, EW detection circuit output is a HIGH (EARLY-WRITE)
$\overline{CAS}$ LOW prior to $\overline{WE}$ LOW, EW detection circuit output is a LOW (LATE-WRITE)

TRUTH TABLE

FUNCTION		$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	ADDRESSES		DATA	
					^tR	^tC	D (Data In)	Q (Data Out)
Standby		H	H→X	X	X	X	Don't Care	High-Z
READ		L	L	H	ROW	COL	Don't Care	Data Out
EARLY-WRITE		L	L	L	ROW	COL	Data In	High-Z
READ-WRITE		L	L	H→L	ROW	COL	Data In	Data Out
FAST-PAGE-MODE	1st Cycle	L	H→L	H	ROW	COL	Don't Care	Data Out
READ	2nd Cycle	L	H→L	H	n/a	COL	Don't Care	Data Out
FAST-PAGE-MODE	1st Cycle	L	H→L	L	ROW	COL	Data In	High-Z
EARLY-WRITE	2nd Cycle	L	H→L	L	n/a	COL	Data In	High-Z
FAST-PAGE-MODE	1st Cycle	L	H→L	H→L	ROW	COL	Data In	Data Out
READ-WRITE	2nd Cycle	L	H→L	H→L	n/a	COL	Data In	Data Out
$\overline{RAS}$-ONLY REFRESH		L	H	X	ROW	n/a	Don't Care	High-Z
HIDDEN	READ	L→H→L	L	H	ROW	COL	Don't Care	Data Out
REFRESH	WRITE	L→H→L	L	L	ROW	COL	Data In	High-Z
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH		H→L	L	H	X	X	Don't Care	High-Z
BATTERY BACKUP REFRESH		H→L	L	H	X	X	Don't Care	High-Z

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to V_{SS} ..... -1V to +7V
Operating Temperature, T_A (Ambient) ..... 0°C to +70°C
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 3, 4, 6, 7) (0°C ≤ T_A ≤ 70°C; V_{CC} = 5V ±10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.5	V	1
Input High (Logic 1) Voltage, All Inputs	V_{IH}	2.4	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, All Inputs	V_{IL}	-1.0	0.8	V	1
INPUT LEAKAGE CURRENT Any Input 0V ≤ V_{IN} ≤ 6.5V (All other pins not under test = 0V)	I_I	-2	2	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled, 0V ≤ V_{OUT} ≤ 5.5V)	I_{OZ}	-10	10	µA	
OUTPUT LEVELS Output High Voltage (I_{OUT} = -5mA)	V_{OH}	2.4		V	
Output Low Voltage (I_{OUT} = 4.2mA)	V_{OL}		0.4	V	

		MAX				
PARAMETER/CONDITION	SYMBOL	-6	-7	-8	UNITS	NOTES
STANDBY CURRENT: (TTL) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC1}	2	2	2	mA	
STANDBY CURRENT: (CMOS) ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} -0.2V)	I_{CC2}	200	200	200	µA	
OPERATING CURRENT: Random READ/WRITE Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC (MIN))	I_{CC3}	110	100	90	mA	3, 4
OPERATING CURRENT: FAST PAGE MODE Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: ^tPC = ^tPC (MIN))	I_{CC4}	80	70	60	mA	3, 4
REFRESH CURRENT: $\overline{RAS}$-ONLY Average power supply current ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}: ^tRC = ^tRC (MIN))	I_{CC5}	110	100	90	mA	3
REFRESH CURRENT: $\overline{CAS}$-BEFORE-$\overline{RAS}$ Average power supply current ($\overline{WE}$ = V_{IH}, $\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC (MIN))	I_{CC6}	110	100	90	mA	3, 5
REFRESH CURRENT: BATTERY BACKUP (BBU) Average power supply current during BATTERY BACKUP refresh: $\overline{CAS}$ = 0.2V or $\overline{CAS}$-BEFORE-$\overline{RAS}$ cycling; $\overline{RAS}$ = ^tRAS (MIN) to 300ns; $\overline{WE}$ = V_{CC} -0.2V, A0-A9 and D_{IN} = V_{CC} - 0.2V or 0.2V (D_{IN} may be left open), ^tRC = 125µs (1,024 rows at 125µs = 128ms)	I_{CC7}	300	300	300	µA	3, 5, 7, 25

CAPACITANCE

PARAMETER	SYMBOL	MAX	UNITS	NOTES
Input Capacitance: A0-A10, D	C_{I1}	5	pF	2
Input Capacitance: $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	C_{I2}	7	pF	2
Output Capacitance: Q	C_O	7	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (V_{CC} = 5V ±10%)

AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	t_{RC}	110		130		150		ns	
READ-WRITE cycle time	t_{RWC}	135		155		175		ns	
FAST-PAGE-MODE READ or WRITE cycle time	t_{PC}	40		40		45		ns	
FAST-PAGE-MODE READ-WRITE cycle time	t_{PRWC}	60		65		70		ns	
Access time from $\overline{RAS}$	t_{RAC}		60		70		80	ns	14
Access time from $\overline{CAS}$	t_{CAC}		15		20		20	ns	15
Access time from column address	t_{AA}		30		35		40	ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		35		40		45	ns	
$\overline{RAS}$ pulse width	t_{RAS}	60	100,000	70	100,000	80	100,000	ns	25
$\overline{RAS}$ pulse width (FAST PAGE MODE)	t_{RASP}	60	100,000	70	100,000	80	100,000	ns	25
$\overline{RAS}$ hold time	t_{RSH}	15		20		20		ns	
$\overline{RAS}$ precharge time	t_{RP}	40		50		60		ns	
$\overline{CAS}$ pulse width	t_{CAS}	15	100,000	20	100,000	20	100,000	ns	
$\overline{CAS}$ hold time	t_{CSH}	60		70		80		ns	
$\overline{CAS}$ precharge time	t_{CPN}	10		10		10		ns	16
$\overline{CAS}$ precharge time (FAST PAGE MODE)	t_{CP}	10		10		10		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	45	20	50	20	60	ns	17
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		10		10		ns	
Row address setup time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	10		10		10		ns	
$\overline{RAS}$ to column address delay time	t_{RAD}	15	30	15	35	15	40	ns	18
Column address setup time	t_{ASC}	0		0		0		ns	
Column address hold time	t_{CAH}	10		15		15		ns	
Column address hold time (referenced to $\overline{RAS}$)	t_{AR}	50		55		60		ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	30		35		40		ns	
Read command setup time	t_{RCS}	0		0		0		ns	
Read command hold time (referenced to $\overline{CAS}$)	t_{RCH}	0		0		0		ns	19
Read command hold time (referenced to $\overline{RAS}$)	t_{RRH}	0		0		0		ns	19
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	0		0		0		ns	
Output buffer turn-off delay	t_{OFF}	0	15	0	20	0	20	ns	20
$\overline{WE}$ command setup time	t_{WCS}	0		0		0		ns	21

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

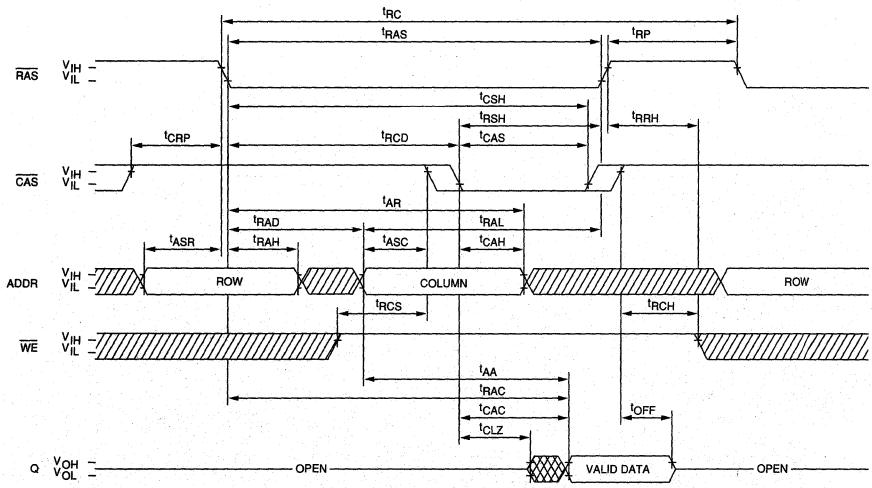
(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (V_{CC} = 5V ±10%)

AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Write command hold time	^tWCH	10		15		15		ns	
Write command hold time (referenced to $\overline{RAS}$)	^tWCR	45		55		60		ns	
Write command pulse width	^tWP	10		15		15		ns	
Write command to $\overline{RAS}$ lead time	^tRWL	15		20		20		ns	
Write command to $\overline{CAS}$ lead time	^tCWL	15		20		20		ns	
Data-in setup time	^tDS	0		0		0		ns	22
Data-in hold time	^tDH	10		15		15		ns	22
Data-in hold time (referenced to $\overline{RAS}$)	^tDHR	45		55		60		ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	^tRWD	60		70		80		ns	21
Column address to $\overline{WE}$ delay time	^tAWD	30		35		40		ns	21
$\overline{CAS}$ to $\overline{WE}$ delay time	^tCWD	15		15		20		ns	21
Transition time (rise or fall)	^tT	3	50	3	50	3	50	ns	9, 10
Refresh period (1,024 cycles)	^tREF		128		128		128	ms	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	^tRPC	0		0		0		ns	
$\overline{CAS}$ setup time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tCSR	10		10		10		ns	5
$\overline{CAS}$ hold time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tCHR	15		15		15		ns	5
$\overline{WE}$ hold time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tWRH	10		10		10		ns	24
$\overline{WE}$ setup time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tWRP	10		10		10		ns	24
$\overline{WE}$ hold time (WCBR test cycle)	^tWTH	10		10		10		ns	24
$\overline{WE}$ setup time (WCBR test cycle)	^tWTS	10		10		10		ns	24

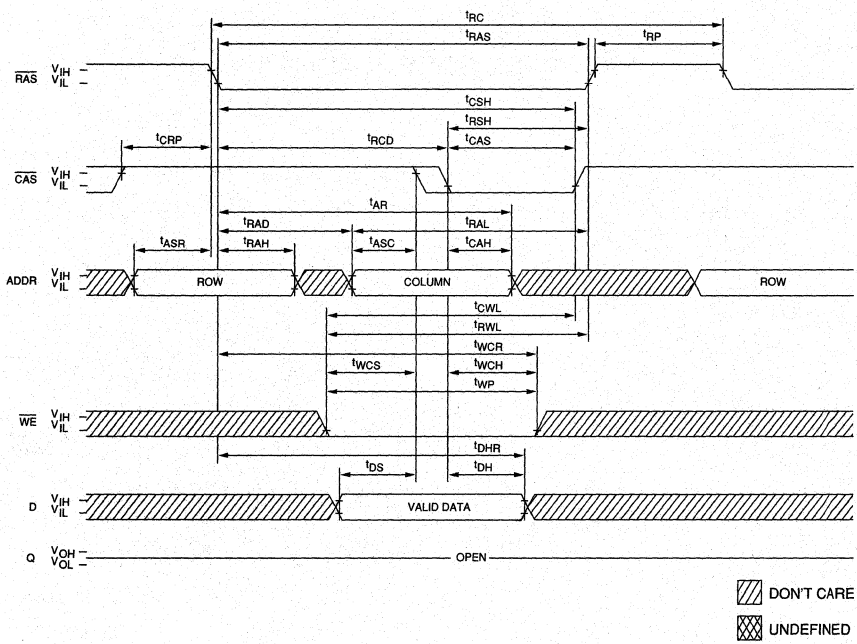
NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. V_{CC} = 5V ±10%, f = 1 MHz.
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is assured.
7. An initial pause of 100µs is required after power-up followed by eight $\overline{RAS}$ refresh cycles ($\overline{RAS}$-ONLY or CBR with $\overline{WE}$ HIGH) before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-up should be repeated any time the ^tREF refresh requirement is exceeded.
8. AC characteristics assume ^tT = 5ns.
9. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS}$ = V_{IH}, data output is High-Z.
12. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to 2 TTL gates and 100pF.
14. Assumes that $^tRCD < ^tRCD$ (MAX). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
15. Assumes that $^tRCD \geq ^tRCD$ (MAX).
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer, $\overline{CAS}$ must be pulsed HIGH for ^tCPN.
17. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (MAX) limit, then access time is controlled exclusively by ^tCAC.
18. Operation within the ^tRAD (MAX) limit ensures that ^tRAC (MIN) and ^tCAC (MIN) can be met. ^tRAD (MAX) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (MAX) limit, then access time is controlled exclusively by ^tAA.
19. Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
20. ^tOFF (MAX) defines the time at which the output achieves the open circuit condition, and is not referenced to V_{OH} or V_{OL}.
21. ^tWCS, ^tRWD, ^tAWD and ^tCWD are restrictive operating parameters in late WRITE, READ-WRITE and READ-MODIFY-WRITE cycles only. If $^tWCS \geq ^tWCS$ (MIN), the cycle is an EARLY-WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If $^tRWD \geq ^tRWD$ (MIN), $^tAWD \geq ^tAWD$ (MIN) and $^tCWD \geq ^tCWD$ (MIN), the cycle is a READ-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the cycle is a LATE-WRITE and the state of data out is indeterminate (at access time and until $\overline{CAS}$ goes back to V_{IH}).
22. These parameters are referenced to $\overline{CAS}$ leading edge in early WRITE cycles and $\overline{WE}$ leading edge in late WRITE or READ-WRITE cycles.
23. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW.
24. ^tWTS and ^tWTH are set up and hold specifications for the $\overline{WE}$ pin being held LOW to enable the JEDEC test mode (with CBR timing constraints). These two parameters are the inverts of ^tWRP and ^tWRH in the CBR refresh cycle.
25. BBU current is reduced as ^tRAS is reduced from its maximum specification during the BBU cycle.

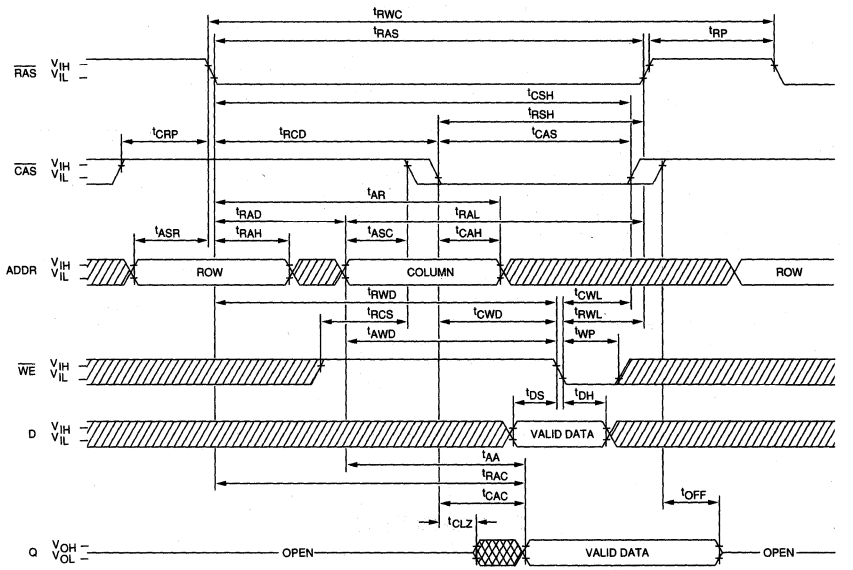
READ CYCLE



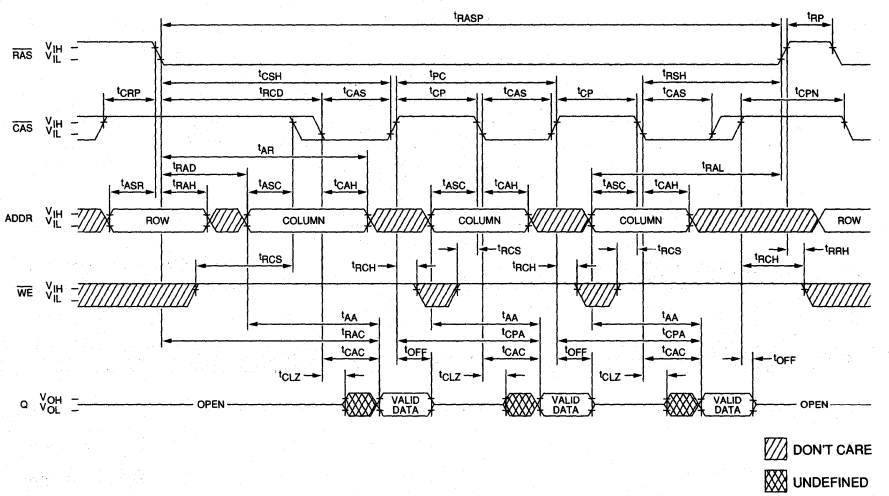
EARLY-WRITE CYCLE



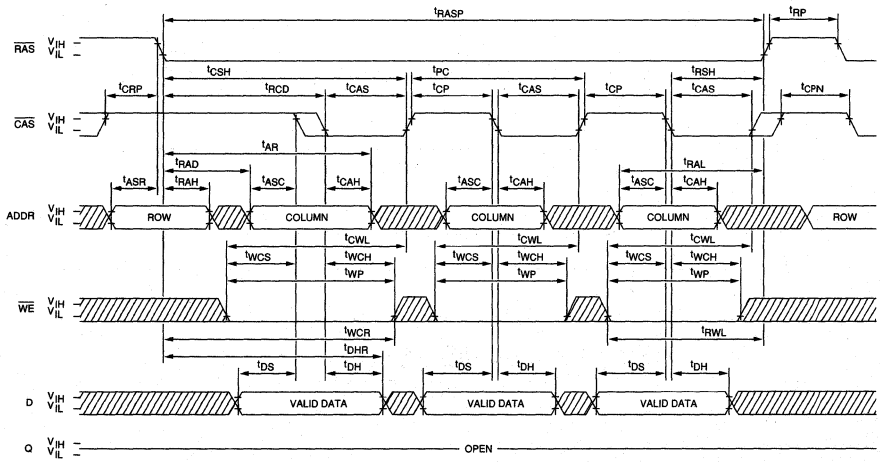
READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)



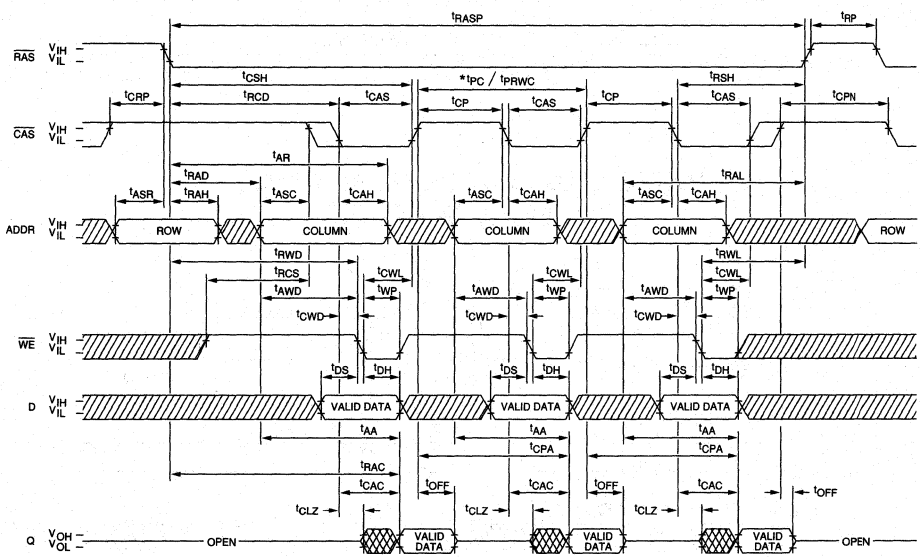
FAST-PAGE-MODE READ CYCLE



FAST-PAGE-MODE EARLY-WRITE CYCLE

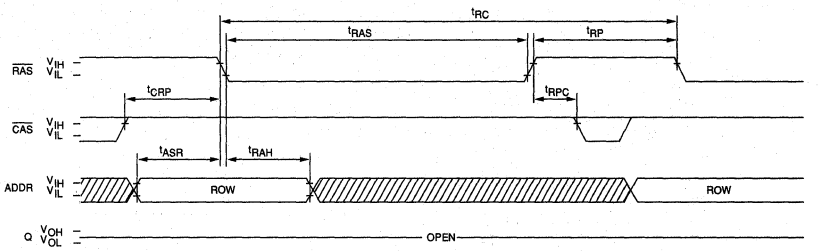


FAST-PAGE-MODE READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)

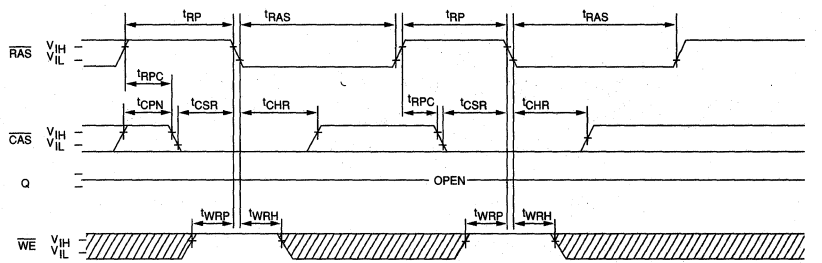


*tPC is for LATE-WRITE only.

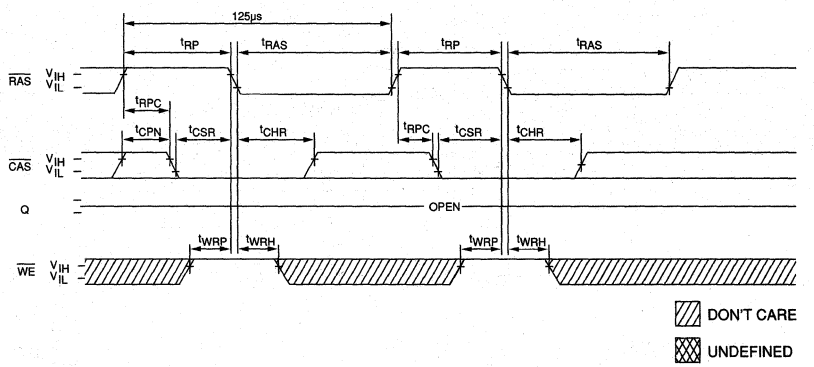
RAS-ONLY REFRESH CYCLE
(ADDR = A0-A9; A10 and WE = DON'T CARE)



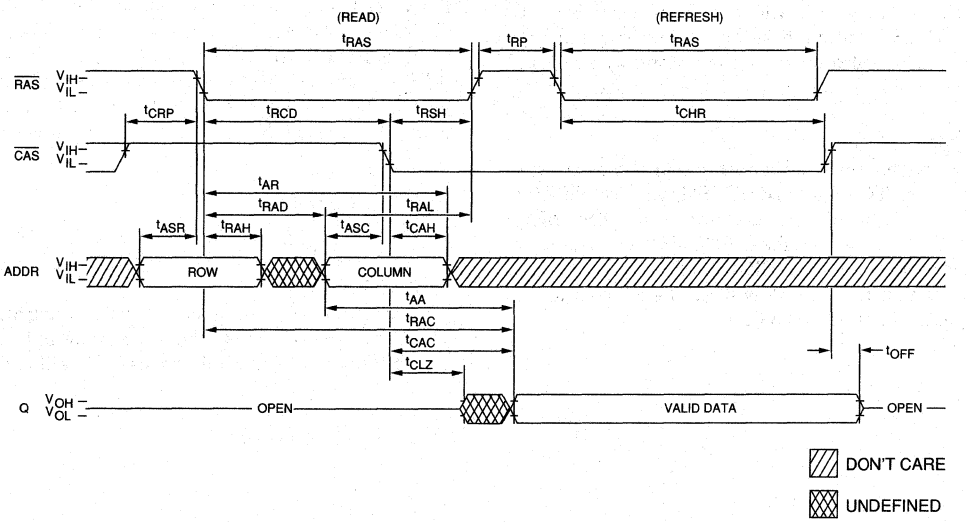
CAS-BEFORE-RAS REFRESH CYCLE
(A0-A10 = DON'T CARE)



BATTERY BACKUP REFRESH CYCLE
(A0-A10 = DON'T CARE)



HIDDEN REFRESH CYCLE [23]
($\overline{WE}$ = HIGH)



4 MEG POWER-UP AND REFRESH CONSTRAINTS

The EIA/JEDEC 4 Meg DRAM introduces two potential incompatibilities compared to the previous generation 1 Meg DRAM. The incompatibilities involve refresh and power-up. Understanding these incompatibilities and providing for them will offer the designer and system user greater compatibility between the 1 Meg and 4 Meg.

REFRESH

The most commonly used refresh mode of the 1 Meg is the CBR ($\overline{CAS}$-BEFORE-$\overline{RAS}$) REFRESH cycle. The CBR for the 1 Meg specifies the $\overline{WE}$ pin as a "don't care." The 4 Meg, on the other hand, specifies the CBR REFRESH mode with the $\overline{WE}$ pin held at a voltage HIGH level.

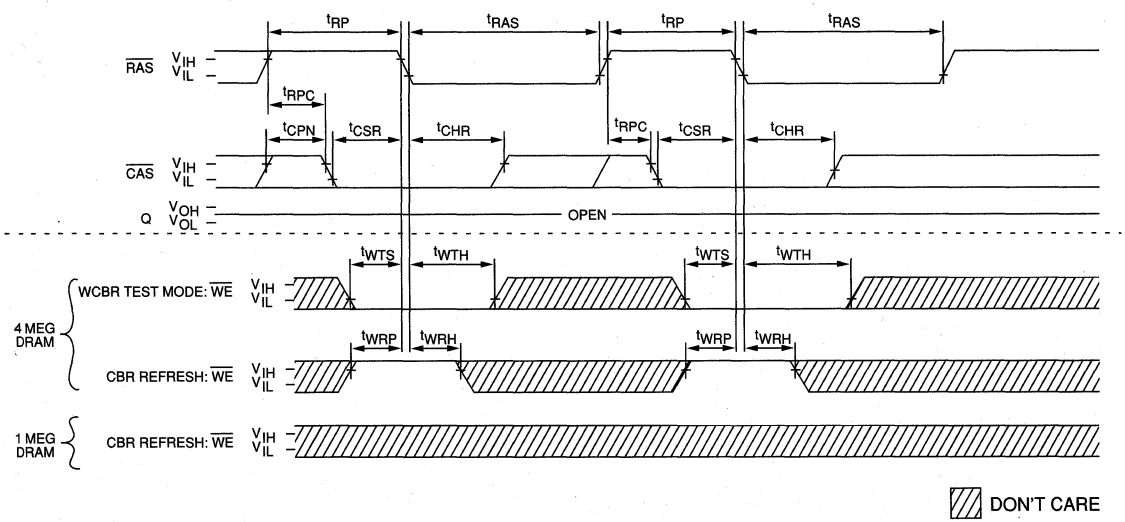
A CBR cycle with $\overline{WE}$ LOW will put the 4 Meg into the JEDEC specified test mode (WCBR).

POWER-UP

The 4 Meg JEDEC test mode constraint may introduce another problem. The 1 Meg POWER-UP cycle requires a 100µs delay followed by any eight $\overline{RAS}$ cycles. The 4 Meg POWER-UP is more restrictive in that eight $\overline{RAS}$-ONLY or CBR REFRESH ($\overline{WE}$ held HIGH) cycles must be used. The restriction is needed since the 4 Meg may power-up in the JEDEC specified test mode and must exit out of the test mode. The only way to exit the 4 Meg JEDEC test mode is with either a $\overline{RAS}$-ONLY or a CBR REFRESH cycle ($\overline{WE}$ held HIGH).

SUMMARY

1. The 1 Meg CBR REFRESH allows the $\overline{WE}$ pin to be "don't care" while the 4 Meg CBR requires $\overline{WE}$ to be HIGH.
2. The eight $\overline{RAS}$ wake-up cycles on the 1 Meg may be any valid $\overline{RAS}$ cycle while the 4 Meg may only use $\overline{RAS}$-ONLY or CBR REFRESH cycles ($\overline{WE}$ held HIGH).



COMPARISON OF 4 MEG TEST MODE AND WCBR TO 1 MEG CBR

DRAM

4 MEG x 1 DRAM

STATIC COLUMN

FEATURES

- Industry standard x1 pinout, timing, functions and packages
- High-performance, CMOS silicon-gate process
- Single +5V ±10% power supply
- Low power, 3mW standby; 225mW active, typical
- All inputs, outputs and clocks are fully TTL compatible
- 1,024-cycle refresh distributed across 16ms
- Refresh modes: RAS-ONLY, CAS-BEFORE-RAS (CBR) and HIDDEN
- STATIC COLUMN access cycle

OPTIONS MARKING

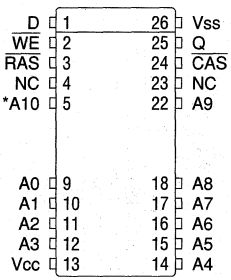
- Timing
  - 70ns access -7
  - 80ns access -8
- Packages
  - Plastic SOJ (300 mil) DJ
  - Plastic ZIP (350 mil) Z

NOTE: Available in die form (commercial or military) or military ceramic packages. Please consult factory for die data sheets or refer to Micron's *Military Data Book.*

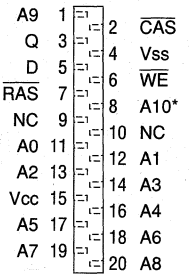
Part Number Example: MT4C1006JDJ-7

PIN ASSIGNMENT (Top View)

20-Pin SOJ (Q-1)



20-Pin ZIP (O-1)



*Address not used for RAS-ONLY REFRESH

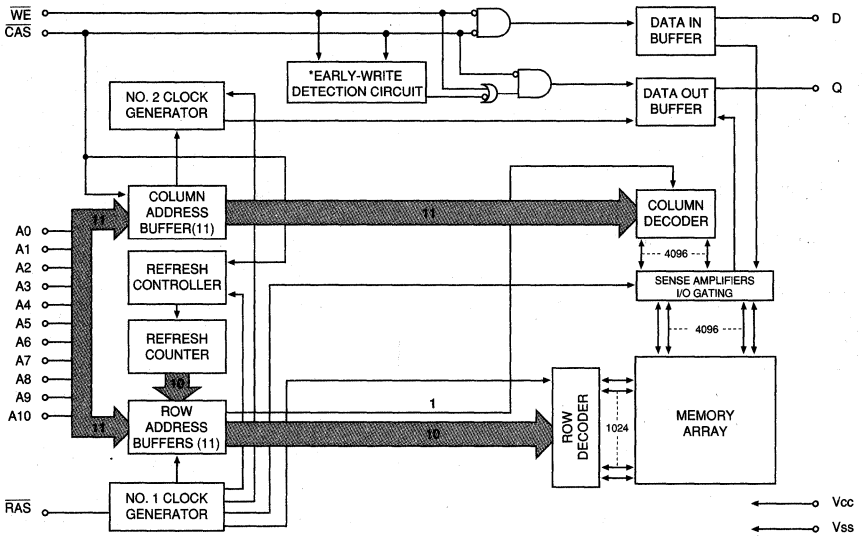
GENERAL DESCRIPTION

The MT4C1006J is a randomly accessed solid-state memory containing 4,194,304 bits organized in a x1 configuration. During READ or WRITE cycles, each bit is uniquely addressed through the 22 address bits, which are entered 11 bits (A0-A10) at a time. RAS is used to latch the first 11 bits and CAS the latter 11 bits. READ and WRITE cycles are selected with the WE input. A logic HIGH on WE dictates READ mode while a logic LOW on WE dictates WRITE mode. During a WRITE cycle, data in (D) is latched by the falling edge of WE or CAS, whichever occurs last. If WE goes LOW prior to CAS going LOW, the output pin remains open (High-Z) until the next CAS cycle. If WE goes LOW after data reaches the output pin, data out (Q) is activated and retains the selected cell data as long as CAS remains LOW (regardless of WE or RAS). This late WE pulse results in a READ-WRITE cycle.

STATIC COLUMN operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row address (A0-A10) defined page boundary. After the first read, any column address transition will result in new data out. Unlike the page-mode part, which requires CAS to be toggled for each successive page-mode access, the STATIC COLUMN part allows CAS to be left LOW for successive STATIC COLUMN accesses. Returning RAS HIGH terminates the STATIC COLUMN operation.

Returning RAS and CAS HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the RAS high time. Memory cell data is retained in its correct state by maintaining power and executing any RAS cycle (READ, WRITE, RAS ONLY, CAS-BEFORE-RAS (CBR), or HIDDEN refresh) so that all 1,024 combinations of RAS addresses (A0-A9) are executed at least every 16ms, regardless of sequence. The CBR cycle will invoke the internal refresh counter for automatic RAS addressing.

FUNCTIONAL BLOCK DIAGRAM
STATIC COLUMN



*NOTE: $\overline{WE}$ LOW prior to $\overline{CAS}$ LOW, EW detection circuit output is a HIGH (EARLY-WRITE)
$\overline{CAS}$ LOW prior to $\overline{WE}$ LOW, EW detection circuit output is a LOW (LATE-WRITE)

TRUTH TABLE

FUNCTION		$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	ADDRESSES ^tR	ADDRESSES ^tC	DATA D (Data In)	DATA Q (Data Out)
Standby		H	H→X	X	X	X	Don't Care	High-Z
READ		L	L	H	ROW	COL	Don't Care	Data Out
EARLY-WRITE		L	L	L	ROW	COL	Data In	High-Z
READ-WRITE		L	L	H→L	ROW	COL	Data In	Data Out
STATIC COLUMN	1st Cycle	L	L	H	ROW	COL	Don't Care	Data Out
READ	2nd Cycle	L	L	H	n/a	COL	Don't Care	Data Out
STATIC COLUMN	1st Cycle	L	L	L	ROW	COL	Data In	High-Z
EARLY-WRITE	2nd Cycle	L	L	H→L	n/a	COL	Data In	High-Z
STATIC COLUMN	1st Cycle	L	L	H→L	ROW	COL	Data In	Data Out
READ-WRITE	2nd Cycle	L	L	H→L	n/a	COL	Data In	Data Out
$\overline{RAS}$-ONLY REFRESH		L	H	X	ROW	n/a	Don't Care	High-Z
HIDDEN	READ	L→H→L	L	H	ROW	COL	Don't Care	Data Out
REFRESH	WRITE	L→H→L	L	L	ROW	COL	Data In	High-Z
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH		H→L	L	H	X	X	Don't Care	High-Z

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Vss ..... -1V to +7V
Operating Temperature, T_A (Ambient) ..... 0°C to +70°C
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 3, 4, 6, 7) (0°C ≤ T_A ≤ 70°C; Vcc = 5V ±10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	Vcc	4.5	5.5	V	1
Input High (Logic 1) Voltage, All Inputs	VIH	2.4	Vcc+1	V	1
Input Low (Logic 0) Voltage, All Inputs	VIL	-1.0	0.8	V	1
INPUT LEAKAGE CURRENT Any Input 0V ≤ VIN ≤ 6.5V (All other pins not under test = 0V)	II	-2	2	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled, 0V ≤ VOUT ≤ 5.5V)	IOZ	-10	10	µA	
OUTPUT LEVELS	VOH	2.4		V	
Output High Voltage (IOUT = -5mA) Output Low Voltage (IOUT = 4.2mA)	VOL		0.4	V	

		MAX			
PARAMETER/CONDITION	SYMBOL	-7	-8	UNITS	NOTES
STANDBY CURRENT: (TTL) ($\overline{RAS}$ = $\overline{CAS}$ = VIH)	ICC1	2	2	mA	
STANDBY CURRENT: (CMOS) ($\overline{RAS}$ = $\overline{CAS}$ = Vcc -0.2V)	ICC2	1	1	mA	
OPERATING CURRENT: Random READ/WRITE Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC (MIN))	ICC3	100	90	mA	3, 4
OPERATING CURRENT: STATIC COLUMN Average power supply current ($\overline{RAS}$ = VIL, $\overline{CAS}$, Address Cycling: ^tSC = ^tSC (MIN))	ICC4	70	60	mA	3, 4
REFRESH CURRENT: $\overline{RAS}$-ONLY Average power supply current ($\overline{RAS}$ Cycling, $\overline{CAS}$ = VIH: ^tRC = ^tRC (MIN))	ICC5	100	90	mA	3
REFRESH CURRENT: $\overline{CAS}$-BEFORE-$\overline{RAS}$ Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC (MIN))	ICC6	100	90	mA	3, 5

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A10, D	C_{I1}		5	pF	2
Input Capacitance: $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	C_{I2}		7	pF	2
Output Capacitance: Q	C_O		7	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (V_{CC} = 5V ±10%)

AC CHARACTERISTICS		-7		-8			
PARAMETER	SYM	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	^tRC	130		150		ns	
READ-WRITE cycle time	^tRWC	155		175		ns	
STATIC-COLUMN READ or WRITE cycle time	^tSC	40		45		ns	
STATIC-COLUMN READ-WRITE cycle time	^tSRWC	70		75		ns	
Access time from $\overline{RAS}$	^tRAC		70		80	ns	14
Access time from $\overline{CAS}$	^tCAC		20		20	ns	15
Access time from column address	^tAA		35		40	ns	
$\overline{RAS}$ pulse width	^tRAS	70	100,000	80	100,000	ns	
$\overline{RAS}$ pulse width (STATIC COLUMN)	^tRASC	70	100,000	80	100,000	ns	
$\overline{RAS}$ hold time	^tRSH	20		20		ns	
$\overline{RAS}$ precharge time	^tRP	50		60		ns	
$\overline{CAS}$ pulse width	^tCAS	20	100,000	20	100,000	ns	
$\overline{CAS}$ hold time	^tCSH	70		80		ns	
$\overline{CAS}$ precharge time	^tCPN	10		10		ns	16
$\overline{CAS}$ precharge time (STATIC COLUMN)	^tCP	10		10		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	^tRCD	20	50	20	60	ns	17
$\overline{CAS}$ to $\overline{RAS}$ precharge time	^tCRP	10		10		ns	
Row address setup time	^tASR	0		0		ns	
Row address hold time	^tRAH	10		10		ns	
$\overline{RAS}$ to column address delay time	^tRAD	15	35	15	40	ns	18
Column address setup time	^tASC	0		0		ns	
Column address hold time	^tCAH	15		15		ns	
Column address hold time (referenced to $\overline{RAS}$)	^tAR	80		90		ns	
Column address to $\overline{RAS}$ lead time	^tRAL	35		40		ns	
Read command setup time	^tRCS	0		0		ns	
Read command hold time (referenced to $\overline{CAS}$)	^tRCH	0		0		ns	19
Read command hold time (referenced to $\overline{RAS}$)	^tRRH	0		0		ns	19
$\overline{CAS}$ to output in Low-Z	^tCLZ	0		0		ns	
Output buffer turn-off delay	^tOFF	0	20	0	20	ns	20
Column address hold time (referenced to $\overline{RAS}$)	^tAWR	55		60		ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

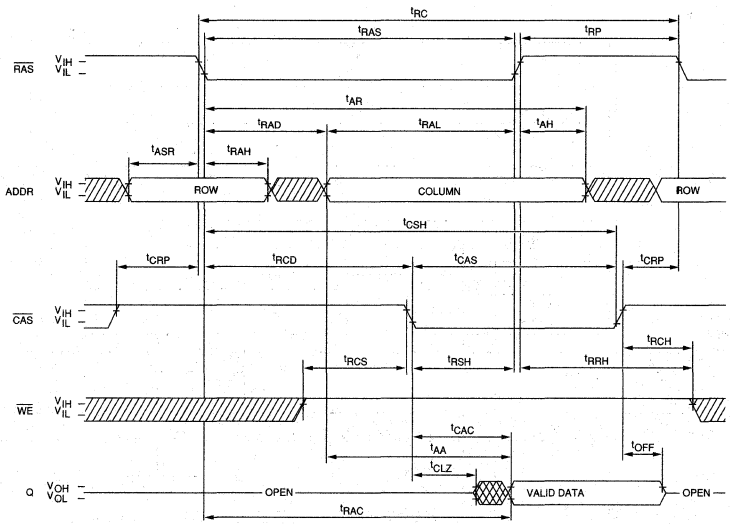
(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (Vcc = 5.0V ± 10%)

AC CHARACTERISTICS		-7		-8			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
$\overline{WE}$ command setup time	tWCS	0		0		ns	21
Write command hold time	tWCH	15		15		ns	
Write command hold time (referenced to $\overline{RAS}$)	tWCR	55		60		ns	
Write command pulse width	tWP	15		15		ns	
Write command to $\overline{RAS}$ lead time	tRWL	20		20		ns	
Write command to $\overline{CAS}$ lead time	tCWL	20		20		ns	
Data-in setup time	tDS	0		0		ns	22
Data-in hold time	tDH	15		15		ns	22
Data-in hold time (referenced to $\overline{RAS}$)	tDHR	55		60		ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	tRWD	70		80		ns	21
Column address to $\overline{WE}$ delay time	tAWD	35		40		ns	21
$\overline{CAS}$ to $\overline{WE}$ delay time	tCWD	20		20		ns	21
Transition time (rise or fall)	tT	3	50	3	50	ns	9, 10
Refresh period (1024 cycles)	tREF		16		16	ms	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	tRPC	0		0		ns	
$\overline{CAS}$ setup time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	tCSR	10		10		ns	5
$\overline{CAS}$ hold time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	tCHR	15		15		ns	5
$\overline{WE}$ hold time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	tWRH	10		10		ns	24
$\overline{WE}$ setup time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	tWRP	10		10		ns	24
$\overline{WE}$ hold time (WCBR test cycle)	tWTH	10		10		ns	24
$\overline{WE}$ setup time (WCBR test cycle)	tWTS	10		10		ns	24
Write inactive time	tWI	10		10		ns	
Previous WRITE to column address delay time	tLWAD	20	30	20	35	ns	
Previous WRITE to column address hold time	tAHLW	65		75		ns	
Output data hold time from column address	tAOH	5		5		ns	
Output data enable from WRITE	tOW	tAA + 5		tAA + 5		ns	
Access time from last WRITE	tALW	65		75		ns	
Column address hold time referenced to RAS HIGH	tAH	5		10		ns	
CAS pulse width in STATIC-COLUMN mode	tCSC	tCAS		tCAS		ns	
Output data hold from WRITE	tWOH	0		0		ns	

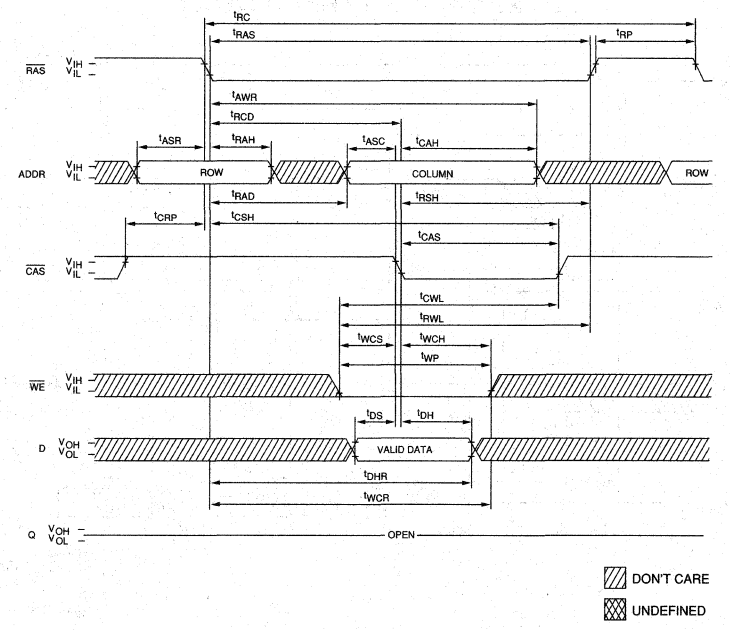
NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. V_{CC} = 5V ±10%, f = 1 MHz.
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \le T_A \le 70°C$) is assured.
7. An initial pause of 100µs is required after power-up followed by eight $\overline{RAS}$ refresh cycles ($\overline{RAS}$-ONLY or CBR with $\overline{WE}$ HIGH) before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-up should be repeated any time the ^tREF refresh requirement is exceeded.
8. AC characteristics assume ^tT = 5ns.
9. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS}$ = V_{IH}, data output is High-Z.
12. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to 2 TTL gates and 100pF.
14. Assumes that $^tRCD < {}^tRCD$ (MAX). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
15. Assumes that $^tRCD \ge {}^tRCD$ (MAX).
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer, $\overline{CAS}$ must be pulsed HIGH for ^tCPN.
17. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (MAX) limit, then access time is controlled exclusively by ^tCAC.
18. Operation within the ^tRAD (MAX) limit ensures that ^tRAC (MIN) and ^tCAC (MIN) can be met. ^tRAD (MAX) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (MAX) limit, then access time is controlled exclusively by ^tAA.
19. Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
20. ^tOFF (MAX) defines the time at which the output achieves the open circuit condition, and is not referenced to V_{OH} or V_{OL}.
21. ^tWCS, ^tRWD, ^tAWD and ^tCWD are restrictive operating parameters in late WRITE, READ-WRITE and READ-MODIFY-WRITE cycles only. If $^tWCS \ge {}^tWCS$ (MIN), the cycle is an EARLY-WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If $^tRWD \ge {}^tRWD$ (MIN), $^tAWD \ge {}^tAWD$ (MIN) and $^tCWD \ge {}^tCWD$ (MIN), the cycle is a READ-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the cycle is a LATE-WRITE and the state of data out is indeterminate (at access time and until $\overline{CAS}$ goes back to V_{IH}).
22. These parameters are referenced to $\overline{CAS}$ leading edge in early WRITE cycles and $\overline{WE}$ leading edge in late WRITE or READ-WRITE cycles.
23. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW.
24. ^tWTS and ^tWTH are set up and hold specifications for the $\overline{WE}$ pin being held LOW to enable the JEDEC test mode (with CBR timing constraints). These two parameters are the inverts of ^tWRP and ^tWRH in the CBR refresh cycle.

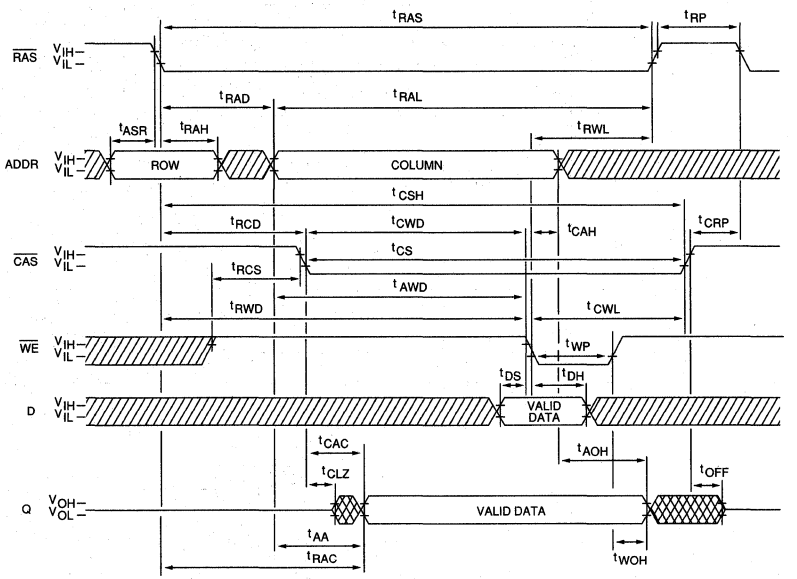
READ CYCLE



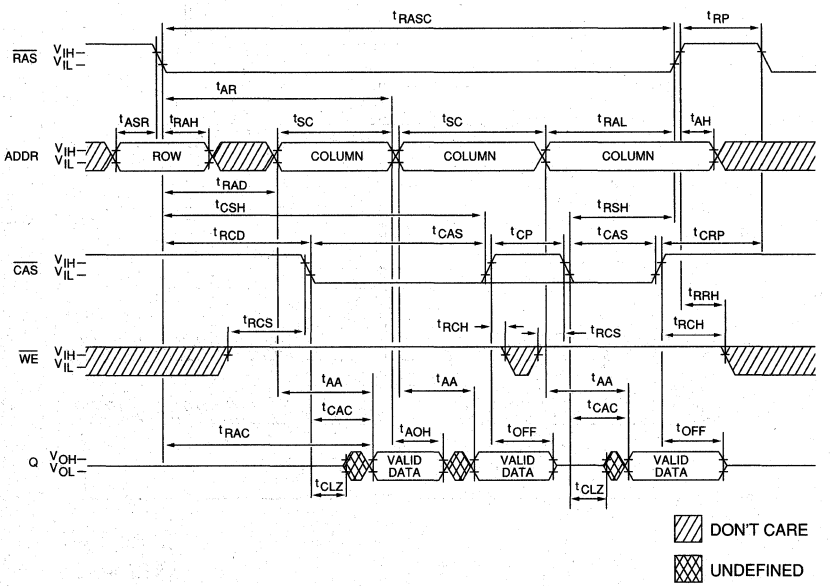
EARLY-WRITE CYCLE



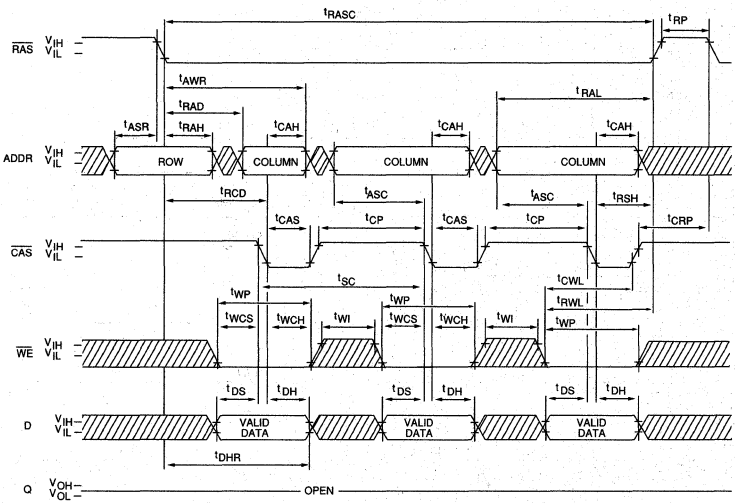
READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)



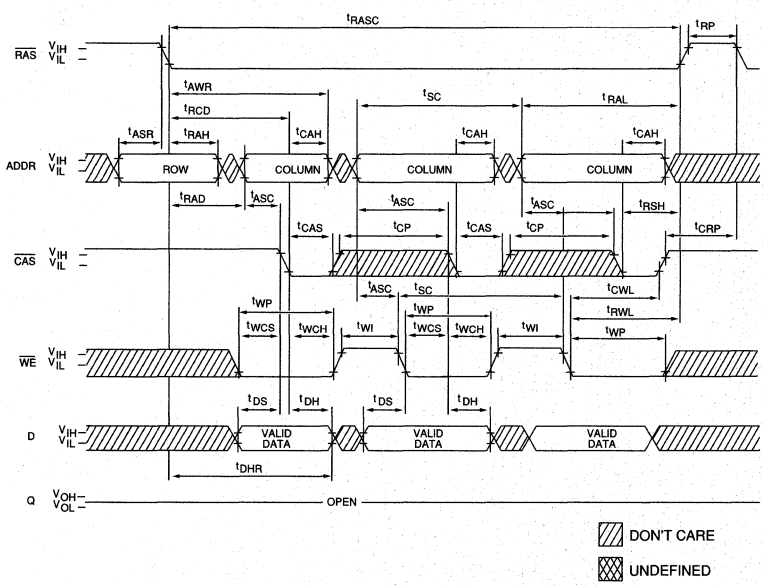
STATIC-COLUMN READ CYCLE



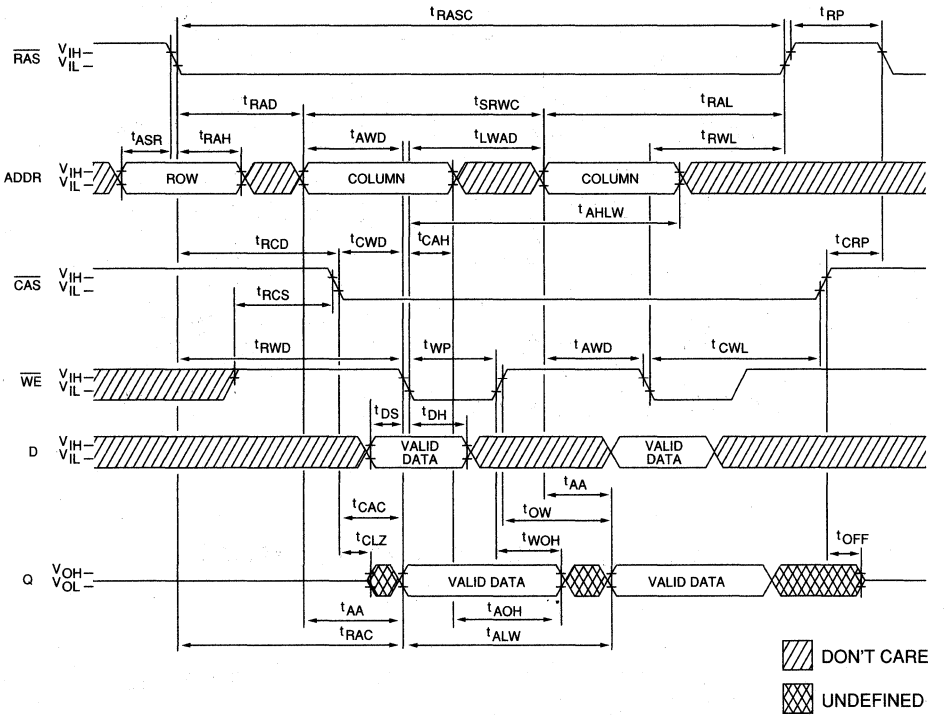
STATIC-COLUMN EARLY-WRITE CYCLE
($\overline{CAS}$ controlled)



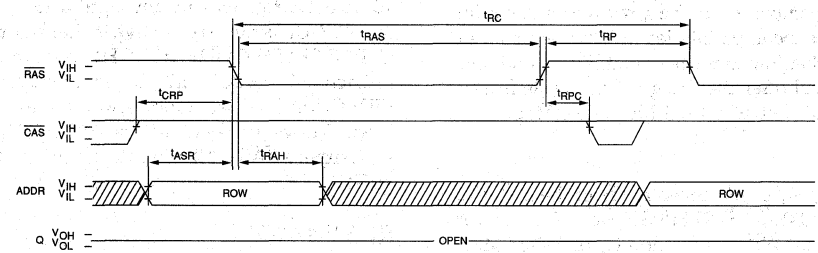
STATIC-COLUMN EARLY-WRITE CYCLE
($\overline{WE}$ controlled)



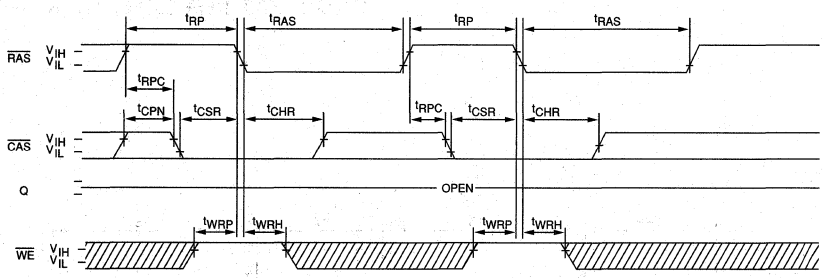
STATIC-COLUMN READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)



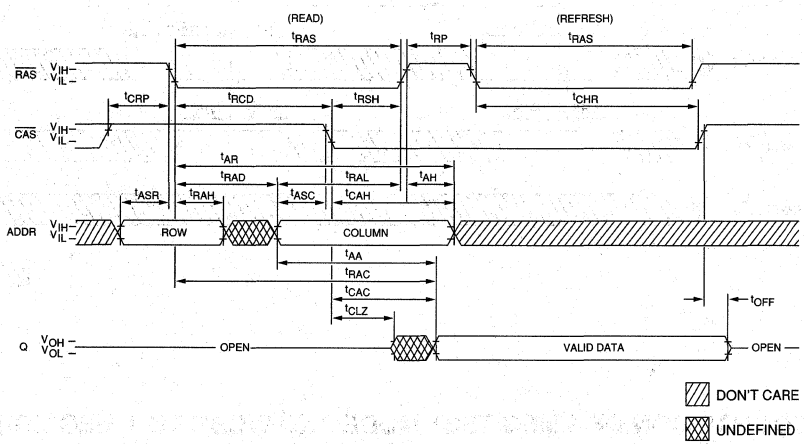
$\overline{RAS}$-ONLY REFRESH CYCLE
(ADDR = A0-A9; A10 and $\overline{WE}$ = DON'T CARE)



$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE
(A0-A10 = DON'T CARE)



HIDDEN REFRESH CYCLE [23]
($\overline{WE}$ = HIGH)



4 MEG POWER-UP AND REFRESH CONSTRAINTS

The EIA/JEDEC 4 Meg DRAM introduces two potential incompatibilities compared to the previous generation 1 Meg DRAM. The incompatibilities involve refresh and power-up. Understanding these incompatibilities and providing for them will offer the designer and system user greater compatibility between the 1 Meg and 4 Meg.

REFRESH

The most commonly used refresh mode of the 1 Meg is the CBR ($\overline{CAS}$-BEFORE-$\overline{RAS}$) REFRESH cycle. The CBR for the 1 Meg specifies the $\overline{WE}$ pin as a "don't care." The 4 Meg, on the other hand, specifies the CBR REFRESH mode with the $\overline{WE}$ pin held at a voltage HIGH level.

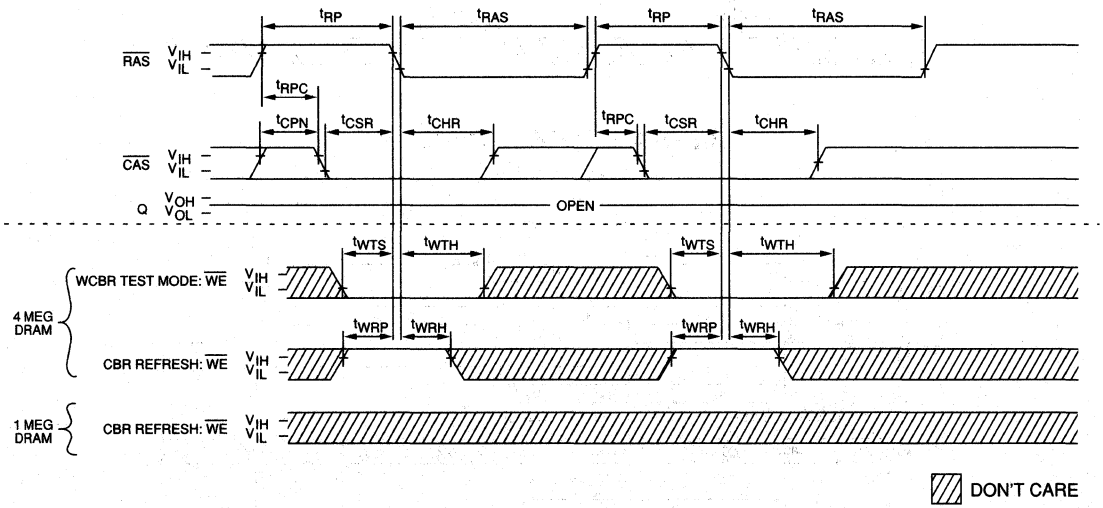
A CBR cycle with $\overline{WE}$ LOW will put the 4 Meg into the JEDEC specified test mode (WCBR).

POWER-UP

The 4 Meg JEDEC test mode constraint may introduce another problem. The 1 Meg POWER-UP cycle requires a 100µs delay followed by any eight $\overline{RAS}$ cycles. The 4 Meg POWER-UP is more restrictive in that eight $\overline{RAS}$-ONLY or CBR REFRESH ($\overline{WE}$ held HIGH) cycles must be used. The restriction is needed since the 4 Meg may power-up in the JEDEC specified test mode and must exit out of the test mode. The only way to exit the 4 Meg JEDEC test mode is with either a $\overline{RAS}$-ONLY or a CBR REFRESH cycle ($\overline{WE}$ held HIGH).

SUMMARY

1. The 1 Meg CBR REFRESH allows the $\overline{WE}$ pin to be "don't care" while the 4 Meg CBR requires $\overline{WE}$ to be HIGH.
2. The eight $\overline{RAS}$ wake-up cycles on the 1 Meg may be any valid $\overline{RAS}$ cycle while the 4 Meg may only use $\overline{RAS}$-ONLY or CBR REFRESH cycles ($\overline{WE}$ held HIGH).



COMPARISON OF 4 MEG TEST MODE AND WCBR TO 1 MEG CBR

DRAM

16 MEG x 1 DRAM

FAST PAGE MODE

FEATURES

- Industry standard x1 pinout, timing, functions and packages
- High-performance, CMOS silicon-gate process
- Single power supply: +5V ±10% only or +3.3V ±10% only
- Low power, 3mW standby; 325mW active, typical (5V)
- All inputs, outputs and clocks are fully TTL compatible
- Refresh modes: $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$ (CBR) and HIDDEN
- 4,096-cycle refresh distributed across 64ms

OPTIONS — MARKING

- Timing
  - 60ns access — -6
  - 70ns access — -7
  - 80ns access — -8
- Packages
  - Plastic SOJ (400 mil) — DJ
  - Plastic TSOP (400 mil) — TG

NOTE: Available in die form (commercial or military) or military ceramic packages. Please consult factory for die data sheets or refer to Micron's *Military Data Book*.

- Operating Temperature, T_A
  - Commercial (0°C to +70°C) — None
- Power Supply
  - +5V ±10% — MT4C16M1A1
  - +3.3V ±10% — MT4LC16M1A1

PIN ASSIGNMENT (Top View)

24-Pin SOJ (Q-3)

Vcc	1	28	Vss
D	2	27	Q
NC	3	26	NC
$\overline{WE}$	4	25	$\overline{CAS}$
$\overline{RAS}$	5	24	NC
A11	6	23	A9
A10	9	20	A8
A0	10	19	A7
A1	11	18	A6
A2	12	17	A5
A3	13	16	A4
Vcc	14	15	Vss

24-Pin TSOP (R-2)

Vcc	1	28	Vss
D	2	27	Q
NC	3	26	NC
$\overline{WE}$	4	25	$\overline{CAS}$
$\overline{RAS}$	5	24	NC
A11	6	23	A9
A10	9	20	A8
A0	10	19	A7
A1	11	18	A6
A2	12	17	A5
A3	13	16	A4
Vcc	14	15	Vss

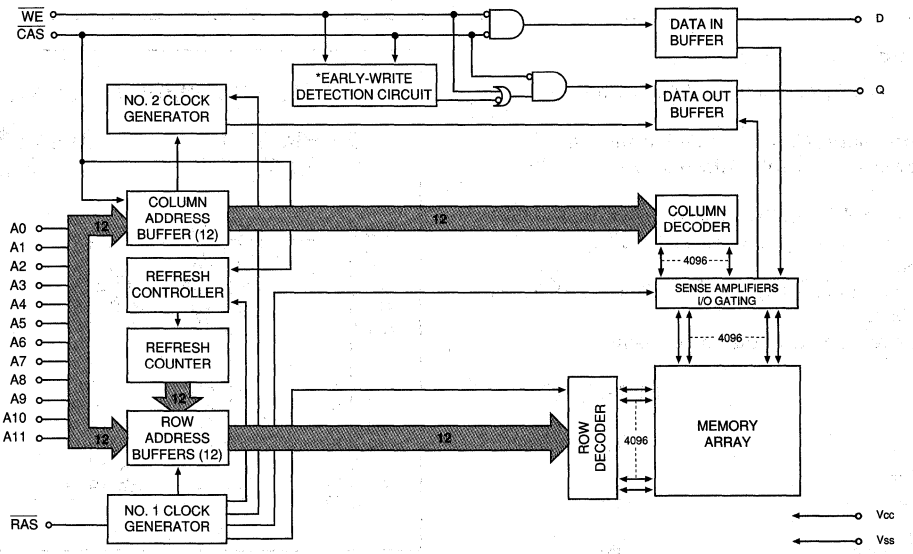
GENERAL DESCRIPTION

The MT4(L)C16M1A1 is a randomly accessed solid-state memory containing 16,777,216 bits organized in a x1 configuration. The MT4C16M1A1 and MT4LC16M1A1 are the same DRAM versions except that the MT4LC16M1A1 is a low voltage version of the MT4C16M1A1. The MT4LC16M1A1 is designed to operate in a 3.3+/-10% memory system. All further references made for the MT4C16M1A1 also apply to the MT4LC16M1A1 unless specifically stated otherwise. During READ and WRITE cycles, each bit is uniquely addressed through the 24 address bits, which are entered 12 bits (A0-A11) at a time. $\overline{RAS}$ is used to latch the first 12 bits and $\overline{CAS}$ the latter 12 bits. READ and WRITE cycles are selected with the $\overline{WE}$ input. A logic HIGH on $\overline{WE}$ dictates READ mode while a logic LOW on $\overline{WE}$ dictates WRITE mode. During a WRITE cycle, data in (D) is latched by the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. If $\overline{WE}$ goes LOW prior to $\overline{CAS}$ going LOW, the output pin remains open (High-Z) until the next $\overline{CAS}$ cycle. If $\overline{WE}$ goes LOW after data reaches the output pin, data out (Q) is activated and retains the selected cell data as long as $\overline{CAS}$ remains LOW (regardless of $\overline{WE}$ or $\overline{RAS}$). This late $\overline{WE}$ pulse results in a READ-WRITE cycle.

FAST PAGE MODE operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row address (A0-A11) defined page boundary. The FAST PAGE MODE cycle is always initiated with a row address strobed-in by $\overline{RAS}$ followed by a column address strobed-in by $\overline{CAS}$. $\overline{CAS}$ may be toggled-in by holding $\overline{RAS}$ LOW and strobing-in different column addresses, thus executing faster memory cycles. Returning $\overline{RAS}$ HIGH terminates the FAST PAGE MODE operation.

Returning $\overline{RAS}$ and $\overline{CAS}$ HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the $\overline{RAS}$ high time. Memory cell data is retained in its correct state by maintaining power and executing any $\overline{RAS}$ cycle (READ, WRITE, $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$ (CBR), or HIDDEN refresh) so that all 4,096 combinations of $\overline{RAS}$ addresses (A0-A11) are executed at least every 64ms, regardless of sequence. The CBR refresh cycle will invoke the internal refresh counter for automatic $\overline{RAS}$ addressing.

FUNCTIONAL BLOCK DIAGRAM
FAST PAGE MODE



*NOTE: $\overline{WE}$ LOW prior to $\overline{CAS}$ LOW, EW detection circuit output is a HIGH (EARLY-WRITE)
$\overline{CAS}$ LOW prior to $\overline{WE}$ LOW, EW detection circuit output is a LOW (LATE-WRITE)

TRUTH TABLE

FUNCTION		$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	ADDRESSES		DATA	
					^tR	^tC	D (Data In)	Q (Data Out)
Standby		H	H→X	X	X	X	Don't Care	High-Z
READ		L	L	H	ROW	COL	Don't Care	Data Out
EARLY-WRITE		L	L	L	ROW	COL	Data In	High-Z
READ-WRITE		L	L	H→L	ROW	COL	Data In	Data Out
FAST-PAGE-MODE	1st Cycle	L	H→L	H	ROW	COL	Don't Care	Data Out
READ	2nd Cycle	L	H→L	H	n/a	COL	Don't Care	Data Out
FAST-PAGE-MODE	1st Cycle	L	H→L	L	ROW	COL	Data In	High-Z
EARLY-WRITE	2nd Cycle	L	H→L	L	n/a	COL	Data In	High-Z
FAST-PAGE-MODE	1st Cycle	L	H→L	H→L	ROW	COL	Data In	Data Out
READ-WRITE	2nd Cycle	L	H→L	H→L	n/a	COL	Data In	Data Out
$\overline{RAS}$-ONLY REFRESH		L	H	X	ROW	n/a	Don't Care	High-Z
HIDDEN	READ	L→H→L	L	H	ROW	COL	Don't Care	Data Out
REFRESH	WRITE	L→H→L	L	L	ROW	COL	Data In	High-Z
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH		H→L	L	H	X	X	Don't Care	High-Z

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to V_{SS} (3.3V) ...-1V to +4.5V
Voltage on Any Pin Relative to V_{SS} (5V) .....-1V to +7V
Operating Temperature, T_A (Ambient) .....0°C to +70°C
Storage Temperature (Plastic) .....-55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 3, 4, 6, 7) (V_{CC} = 5V ±10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.5	V	1
Input High (Logic 1) Voltage, All Inputs	V_{IH}	2.4	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, All Inputs	V_{IL}	-1.0	0.8	V	1
INPUT LEAKAGE CURRENT Any Input 0V ≤ V_{IN} ≤ 6.5V (All other pins not under test = 0V)	I_I	-2	2	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled, 0V ≤ V_{OUT} ≤ 5.5V)	I_{OZ}	-10	10	µA	
OUTPUT LEVELS Output High Voltage (I_{OUT} = -5mA)	V_{OH}	2.4		V	
Output Low Voltage (I_{OUT} = 4.2mA)	V_{OL}		0.4	V	

(Notes: 1, 3, 4, 6, 7) (V_{CC} = 3.3V ±10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	3.0	3.6	V	1
Input High (Logic 1) Voltage, All Inputs	V_{IH}	2.0	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, All Inputs	V_{IL}	-1.0	0.8	V	1
INPUT LEAKAGE CURRENT Any input 0V ≤ V_{IN} ≤ 3.6V (All other pins not under test = 0V)	I_I	-2	2	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled, 0V ≤ V_{OUT} ≤ 3.6V)	I_{OZ}	-10	10	µA	
OUTPUT LEVELS Output High Voltage (I_{OUT} = -2mA)	V_{OH}	2.4		V	
Output Low Voltage (I_{OUT} = 2mA)	V_{OL}		0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 3, 4, 6, 7) (V_{CC} = 5V ±10%)

		MAX				
PARAMETER/CONDITION	**SYMBOL**	**-6**	**-7**	**-8**	**UNITS**	**NOTES**
STANDBY CURRENT: (TTL) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC1}	2	2	2	mA	
STANDBY CURRENT: (CMOS) ($\overline{RAS}$ = $\overline{CAS}$ = Other Inputs = V_{CC} -0.2V)	I_{CC2}	1	1	1	mA	
OPERATING CURRENT: Random READ/WRITE Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC (MIN))	I_{CC3}	90	80	70	mA	3, 4
OPERATING CURRENT: FAST PAGE MODE Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: ^tPC = ^tPC (MIN))	I_{CC4}	70	60	50	mA	3, 4
REFRESH CURRENT: $\overline{RAS}$-ONLY Average power supply current ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}: ^tRC = ^tRC (MIN))	I_{CC5}	90	80	70	mA	3
REFRESH CURRENT: $\overline{CAS}$-BEFORE-$\overline{RAS}$ Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC (MIN))	I_{CC6}	90	80	70	mA	3, 5

(Notes: 1, 3, 4, 6, 7) (V_{CC} = 3.3V ±10%)

		MAX				
PARAMETER/CONDITION	**SYMBOL**	**-6**	**-7**	**-8**	**UNITS**	**NOTES**
STANDBY CURRENT: (TTL) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC1}	2	2	2	mA	
STANDBY CURRENT: (CMOS) ($\overline{RAS}$ = $\overline{CAS}$ = Other Inputs = V_{CC} -0.2V)	I_{CC2}	400	400	400	µA	
OPERATING CURRENT: Random READ/WRITE Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC (MIN))	I_{CC3}	60	55	50	mA	3, 4
OPERATING CURRENT: FAST PAGE MODE Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: ^tPC = ^tPC (MIN))	I_{CC4}	40	35	30	mA	3, 4
REFRESH CURRENT: $\overline{RAS}$-ONLY Average power supply current ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}: ^tRC = ^tRC (MIN))	I_{CC5}	60	55	50	mA	3
REFRESH CURRENT: $\overline{CAS}$-BEFORE-$\overline{RAS}$ Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC (MIN))	I_{CC6}	60	55	50	mA	3, 5

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A11, D	C_{I1}		5	pF	2
Input Capacitance: $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	C_{I2}		7	pF	2
Output Capacitance: Q	C_O		7	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13)

AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	^tRC	110		130		150		ns	
READ-WRITE cycle time	^tRWC	130		155		175		ns	
FAST-PAGE-MODE READ or WRITE cycle time	^tPC	40		45		50		ns	
FAST-PAGE-MODE READ-WRITE cycle time	^tPRWC	60		70		75		ns	
Access time from $\overline{RAS}$	^tRAC		60		70		80	ns	14
Access time from $\overline{CAS}$	^tCAC		15		20		20	ns	15
Access time from column address	^tAA		30		35		40	ns	
Access time from $\overline{CAS}$ precharge	^tCPA		35		40		45	ns	
$\overline{RAS}$ pulse width	^tRAS	60	100,000	70	100,000	80	100,000	ns	
$\overline{RAS}$ pulse width (FAST PAGE MODE)	^tRASP	60	100,000	70	100,000	80	100,000	ns	
$\overline{RAS}$ hold time	^tRSH	15		20		20		ns	
$\overline{RAS}$ precharge time	^tRP	40		50		60		ns	
$\overline{CAS}$ pulse width	^tCAS	15	100,000	20	100,000	20	100,000	ns	
$\overline{CAS}$ hold time	^tCSH	60		70		80		ns	
$\overline{CAS}$ precharge time	^tCPN	10		10		10		ns	16
$\overline{CAS}$ precharge time (FAST PAGE MODE)	^tCP	10		10		10		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	^tRCD	20	45	20	50	20	60	ns	17
$\overline{CAS}$ to $\overline{RAS}$ precharge time	^tCRP	5		5		5		ns	
Row address setup time	^tASR	0		0		0		ns	
Row address hold time	^tRAH	10		10		10		ns	
$\overline{RAS}$ to column address delay time	^tRAD	15	30	15	35	15	40	ns	18
Column address setup time	^tASC	0		0		0		ns	
Column address hold time	^tCAH	10		15		15		ns	
Column address hold time (referenced to $\overline{RAS}$)	^tAR	50		55		60		ns	
Column address to $\overline{RAS}$ lead time	^tRAL	30		35		40		ns	
Read command setup time	^tRCS	0		0		0		ns	
Read command hold time (referenced to $\overline{CAS}$)	^tRCH	0		0		0		ns	19
Read command hold time (referenced to $\overline{RAS}$)	^tRRH	0		0		0		ns	19
$\overline{CAS}$ to output in Low-Z	^tCLZ	0		0		0		ns	
Output buffer turn-off delay	^tOFF	0	15	0	20	0	20	ns	20
$\overline{WE}$ command setup time	^tWCS	0		0		0		ns	21

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

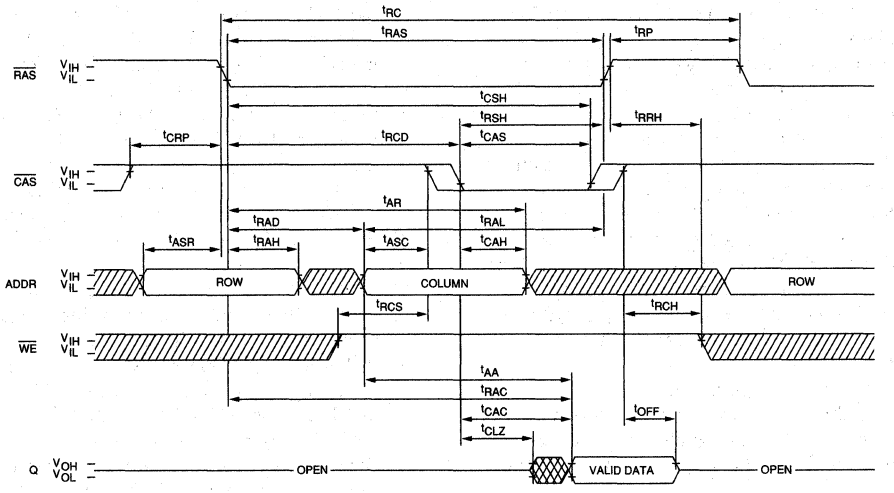
(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (V_{CC} = 5V ±10%)

AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Write command hold time	^tWCH	10		15		15		ns	
Write command hold time (referenced to $\overline{RAS}$)	^tWCR	45		55		60		ns	
Write command pulse width	^tWP	10		15		15		ns	
Write command to $\overline{RAS}$ lead time	^tRWL	15		20		20		ns	
Write command to $\overline{CAS}$ lead time	^tCWL	15		20		20		ns	
Data-in setup time	^tDS	0		0		0		ns	22
Data-in hold time	^tDH	10		15		15		ns	22
Data-in hold time (referenced to $\overline{RAS}$)	^tDHR	45		55		60		ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	^tRWD	60		70		80		ns	21
Column address to $\overline{WE}$ delay time	^tAWD	30		35		40		ns	21
$\overline{CAS}$ to $\overline{WE}$ delay time	^tCWD	15		20		20		ns	21
Transition time (rise or fall)	^tT	3	50	3	50	3	50	ns	9, 10
Refresh period (1,024 cycles)	^tREF		64		64		64	ms	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	^tRPC	0		0		0		ns	
$\overline{CAS}$ setup time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tCSR	5		5		5		ns	5
$\overline{CAS}$ hold time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tCHR	15		15		15		ns	5
$\overline{WE}$ hold time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tWRH	10		10		10		ns	24
$\overline{WE}$ setup time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tWRP	10		10		10		ns	24
$\overline{WE}$ hold time (WCBR test cycle)	^tWTH	10		10		10		ns	24
$\overline{WE}$ setup time (WCBR test cycle)	^tWTS	10		10		10		ns	24

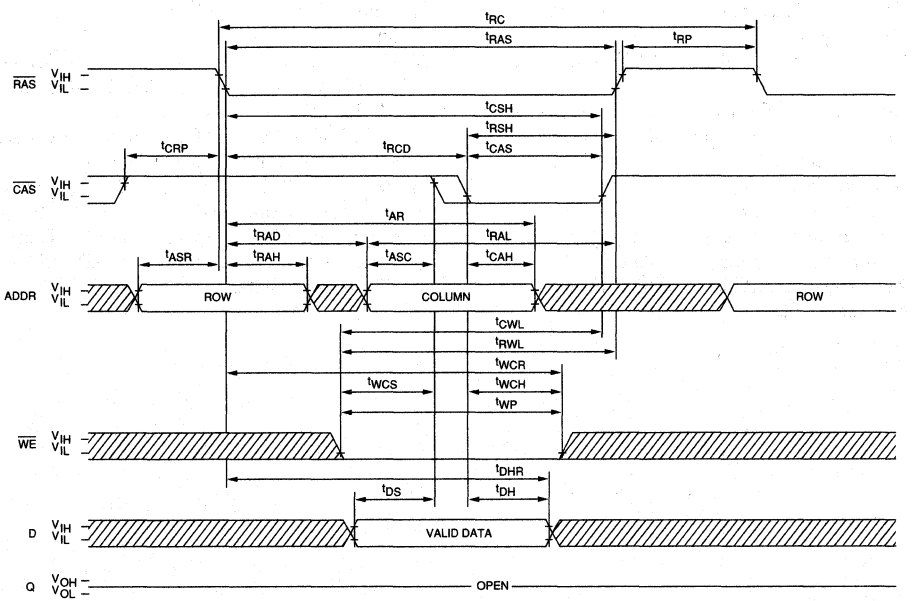
NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. V_{CC} = 5V ±10%, f = 1 MHz.
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is assured.
7. An initial pause of 100µs is required after power-up followed by eight $\overline{RAS}$ refresh cycles ($\overline{RAS}$-ONLY or CBR with $\overline{WE}$ HIGH) before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-up should be repeated any time the ^{t}REF refresh requirement is exceeded.
8. AC characteristics assume ^{t}T = 5ns.
9. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS}$ = V_{IH}, data output is High-Z.
12. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to 2 TTL gates and 100pF.
14. Assumes that $^{t}RCD < {}^{t}RCD$ (MAX). If ^{t}RCD is greater than the maximum recommended value shown in this table, ^{t}RAC will increase by the amount that ^{t}RCD exceeds the value shown.
15. Assumes that $^{t}RCD \geq {}^{t}RCD$ (MAX).
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer, $\overline{CAS}$ must be pulsed HIGH for ^{t}CPN.
17. Operation within the ^{t}RCD (MAX) limit ensures that ^{t}RAC (MAX) can be met. ^{t}RCD (MAX) is specified as a reference point only; if ^{t}RCD is greater than the specified ^{t}RCD (MAX) limit, then access time is controlled exclusively by ^{t}CAC.
18. Operation within the ^{t}RAD (MAX) limit ensures that ^{t}RAC (MIN) and ^{t}CAC (MIN) can be met. ^{t}RAD (MAX) is specified as a reference point only; if ^{t}RAD is greater than the specified ^{t}RAD (MAX) limit, then access time is controlled exclusively by ^{t}AA.
19. Either ^{t}RCH or ^{t}RRH must be satisfied for a READ cycle.
20. ^{t}OFF (MAX) defines the time at which the output achieves the open circuit condition, and is not referenced to V_{OH} or V_{OL}.
21. ^{t}WCS, ^{t}RWD, ^{t}AWD and ^{t}CWD are restrictive operating parameters in LATE-WRITE, READ-WRITE and READ-MODIFY-WRITE cycles only. If $^{t}WCS \geq {}^{t}WCS$ (MIN), the cycle is an EARLY-WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If $^{t}RWD \geq {}^{t}RWD$ (MIN), $^{t}AWD \geq {}^{t}AWD$ (MIN) and $^{t}CWD \geq {}^{t}CWD$ (MIN), the cycle is a READ-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the cycle is a LATE-WRITE and the state of data out is indeterminate (at access time and until $\overline{CAS}$ goes back to V_{IH}).
22. These parameters are referenced to $\overline{CAS}$ leading edge in early WRITE cycles and $\overline{WE}$ leading edge in late WRITE or READ-WRITE cycles.
23. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW.
24. ^{t}WTS and ^{t}WTH are set up and hold specifications for the $\overline{WE}$ pin being held LOW to enable the JEDEC test mode (with CBR timing constraints). These two parameters are the inverts of ^{t}WRP and ^{t}WRH in the CBR refresh cycle.

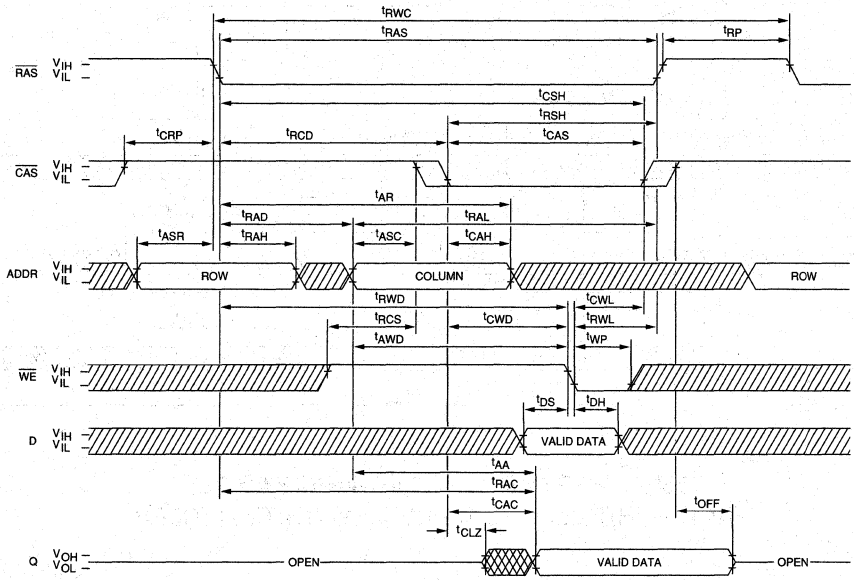
READ CYCLE



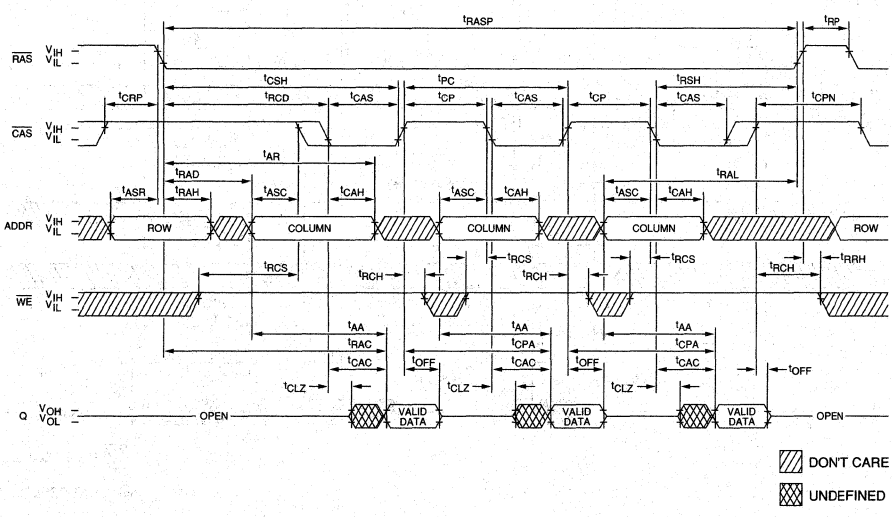
EARLY-WRITE CYCLE



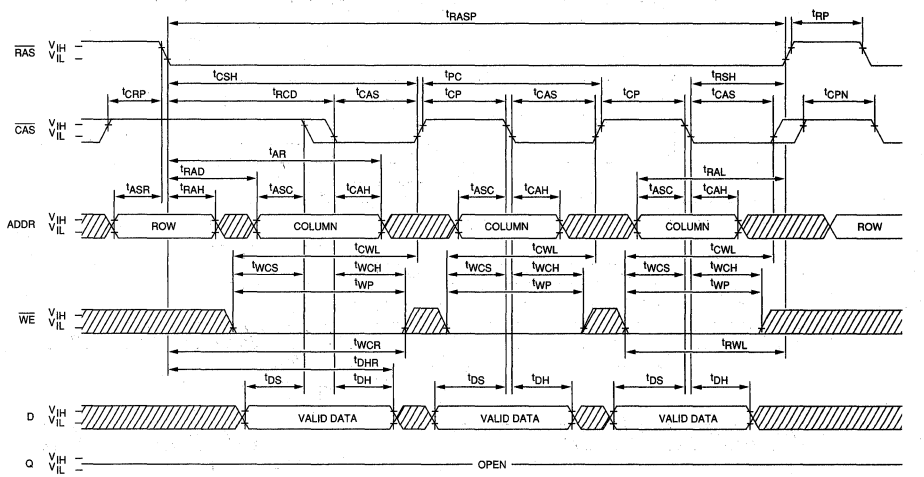
READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)



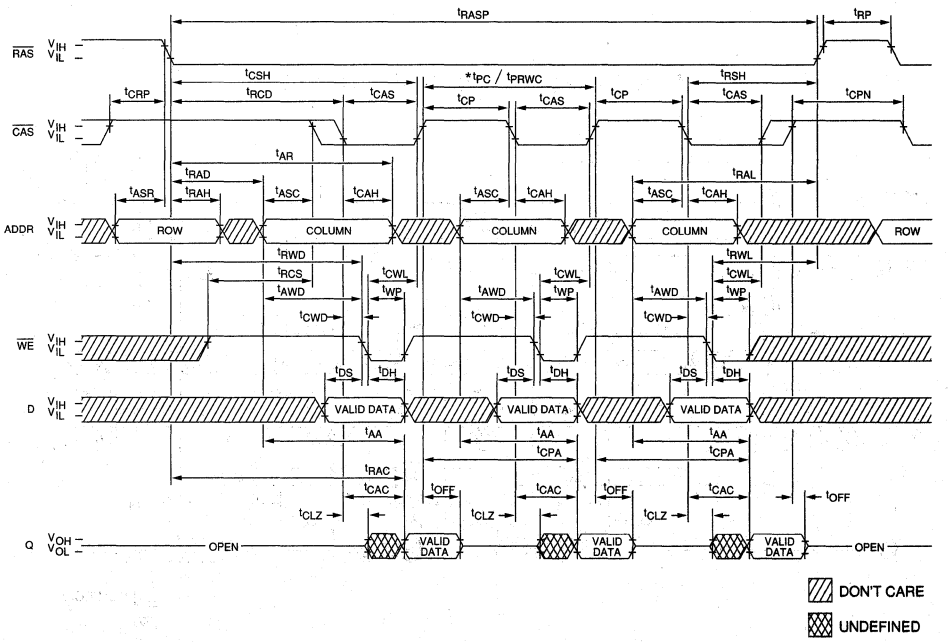
FAST-PAGE-MODE READ CYCLE



FAST-PAGE-MODE EARLY-WRITE CYCLE

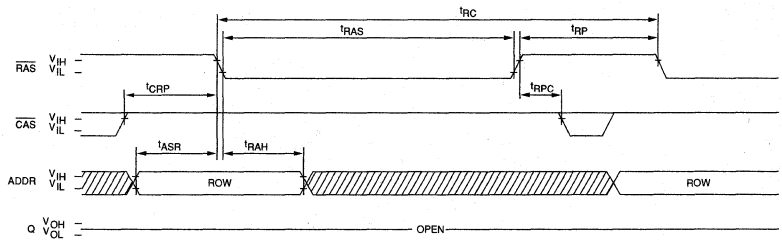


FAST-PAGE-MODE READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)



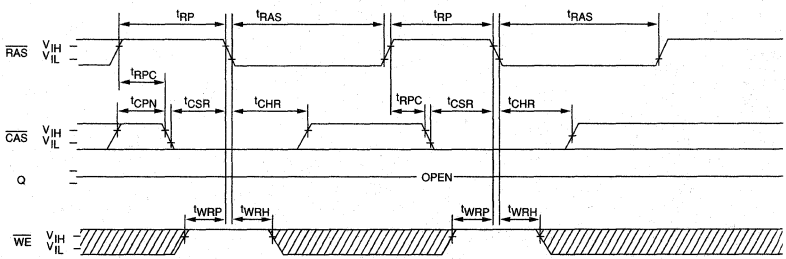
RAS-ONLY REFRESH CYCLE

(ADDR = A0-A10; A11 and WE = DON'T CARE)



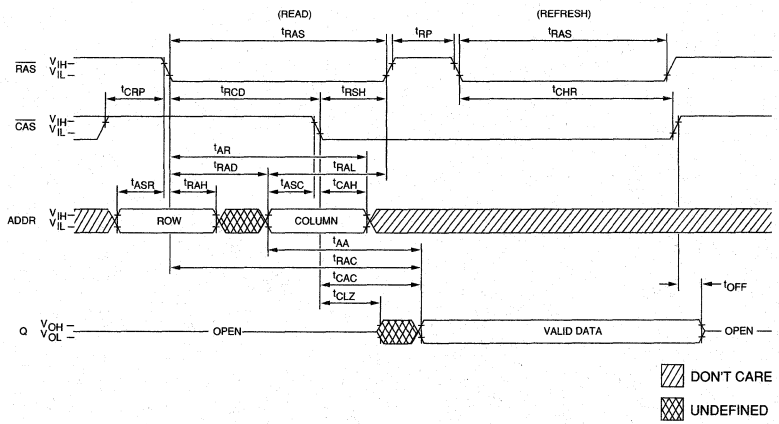
CAS-BEFORE-RAS REFRESH CYCLE

(A0-A11 = DON'T CARE)



HIDDEN REFRESH CYCLE [23]

(WE = HIGH)



DRAM

16 MEG x 1 DRAM

STATIC COLUMN

FEATURES

- Industry standard x1 pinout, timing, functions and packages
- High-performance, CMOS silicon-gate process
- Single power supply: +5V ±10%
- Low power, 3mW standby; 330mW active, typical
- All inputs, outputs and clocks are fully TTL compatible
- Refresh modes: $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$ (CBR) and HIDDEN
- 4,096-cycle refresh distributed across 64ms

OPTIONS — MARKING

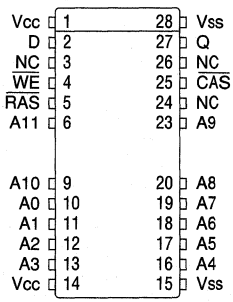
- Timing
  - 60ns access — -6
  - 70ns access — -7
  - 80ns access — -8
- Packages
  - Plastic SOJ (400 mil) — DJ

NOTE: Available in die form (commercial or military) or military ceramic packages. Please consult factory for die data sheets or refer to Micron's ***Military Data Book.***

- Operating Temperature, T_A
  - Commercial (0°C to +70°C) — None
- Part Number Example: MT4C16M1D1DJ-6

PIN ASSIGNMENT (Top View)

24-Pin SOJ
(Q-3)



GENERAL DESCRIPTION

The MT4C16M1D1 is a randomly accessed solid-state memory containing 16,777,216 bits organized in a x1 configuration. During READ or WRITE cycles, each bit is uniquely addressed through the 24 address bits, which are entered 12 bits (A0-A11) at a time. $\overline{RAS}$ is used to latch the first 12 bits and $\overline{CAS}$ the latter 12 bits. READ and WRITE cycles are selected with the $\overline{WE}$ input. A logic HIGH on $\overline{WE}$ dictates READ mode while a logic LOW on $\overline{WE}$ dictates WRITE mode. During a WRITE cycle, data in (D) is latched by the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. If $\overline{WE}$ goes LOW prior to $\overline{CAS}$ going LOW, the output pin remains open (High-Z) until the next $\overline{CAS}$ cycle. If $\overline{WE}$ goes LOW after data reaches the output pin, data out (Q) is activated and retains the selected cell data as long as $\overline{CAS}$ remains LOW (regardless of $\overline{WE}$ or $\overline{RAS}$). This late $\overline{WE}$ pulse results in a READ-WRITE cycle.

STATIC COLUMN operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row address (A0-A11) defined page boundary. After the first read, any column address transition will result in new data out. Unlike the PAGE-MODE part, which requires $\overline{CAS}$ to be toggled for each successive PAGE-MODE access, the STATIC COLUMN part allows $\overline{CAS}$ to be left LOW for successive STATIC COLUMN accesses. Returning $\overline{RAS}$ HIGH terminates the STATIC COLUMN operation.

Returning $\overline{RAS}$ and $\overline{CAS}$ HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the $\overline{RAS}$ high time. Memory cell data is retained in its correct state by maintaining power and executing any $\overline{RAS}$ cycle (READ, WRITE, $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$ or HIDDEN refresh) so that all 4,096 combinations of $\overline{RAS}$ addresses (A0-A11) are executed at least every 64ms, regardless of sequence. The CBR refresh cycle will invoke the internal refresh counter for automatic $\overline{RAS}$ addressing.

DRAM

256K x 4 DRAM

FAST PAGE MODE

FEATURES

- Industry standard x4 pinout, timing, functions and packages
- High-performance, CMOS silicon-gate process
- Single +5V ±10% power supply
- Low power, 3mW standby; 175mW active, typical
- All inputs, outputs and clocks are fully TTL compatible
- 512-cycle refresh in 8ms
- Refresh modes: $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$ (CBR) and HIDDEN
- Optional FAST PAGE MODE access cycle

OPTIONS — MARKING

- Timing

60ns access	- 6
70ns access	- 7
80ns access	- 8

- Packages

Plastic DIP (300 mil)	None
Plastic SOJ (300 mil)	DJ
Plastic TSOP (300 mil)*	TG
Plastic ZIP (350 mil)	Z

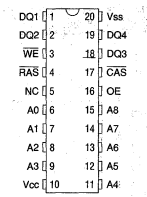
NOTE: Available in die form (commercial or military) or military ceramic packages. Please consult factory for die data sheets or refer to Micron's *Military Data Book*.

- Operating Temperature, T_A

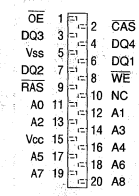
Commercial (0°C to +70°C)	None
Industrial (-40°C to +85°C)	IT

PIN ASSIGNMENT (Top View)

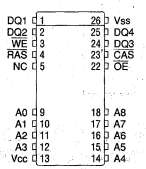
20-Pin DIP (N-2)



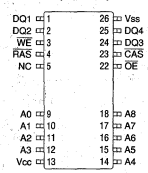
20-Pin ZIP (O-1)



20-Pin SOJ (Q-1)



20-Pin TSOP (R-1)



*Consult factory on availability of reverse pinout TSOP packages

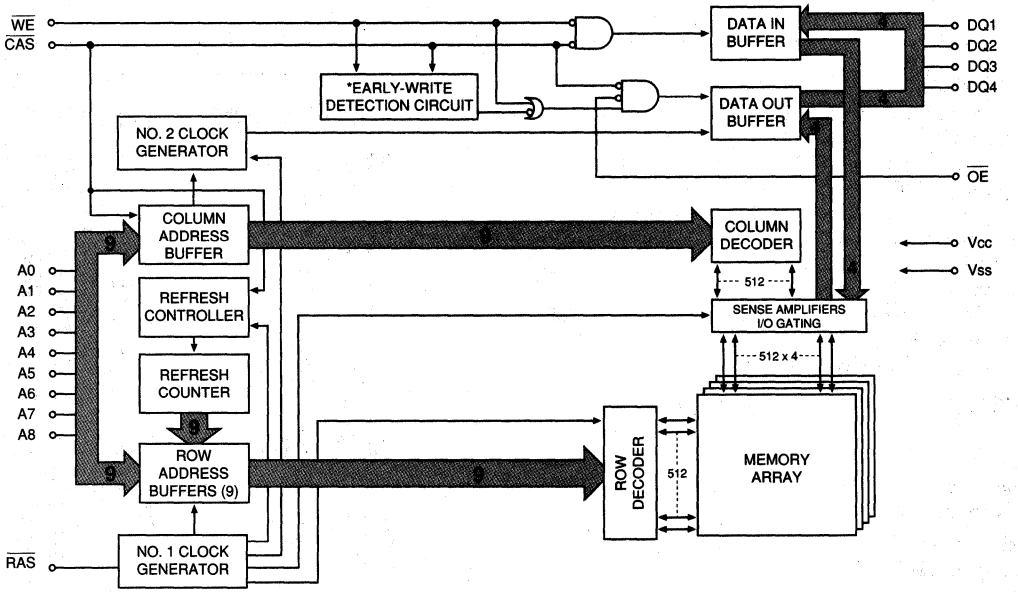
GENERAL DESCRIPTION

The MT4C4256 is a randomly accessed solid-state memory containing 1,048,576 bits organized in a x4 configuration. During READ or WRITE cycles each bit is uniquely addressed through the 18 address bits which are entered 9 bits (A0-A8) at a time. $\overline{RAS}$ is used to latch the first 9 bits and $\overline{CAS}$ the latter 9 bits. READ and WRITE cycles are selected with the $\overline{WE}$ input. A logic HIGH on $\overline{WE}$ dictates READ mode while a logic LOW on $\overline{WE}$ dictates WRITE mode. During a WRITE cycle, data in (D) is latched by the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. If $\overline{WE}$ goes LOW prior to $\overline{CAS}$ going LOW, the output pin(s) remain open (High-Z) until the next $\overline{CAS}$ cycle. If $\overline{WE}$ goes LOW after data reaches the output pin, data out (Q) is activated and retains the selected cell data as long as $\overline{CAS}$ remains LOW (regardless of $\overline{WE}$ or $\overline{RAS}$). This late $\overline{WE}$ pulse results in a READ-WRITE cycle. The four data inputs and four data outputs are routed through four pins using common I/O, and pin direction is controlled by $\overline{WE}$ and $\overline{OE}$.

FAST PAGE MODE operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row address (A0-A8) defined page boundary. The FAST PAGE MODE cycle is always initiated with a row address strobed-in by $\overline{RAS}$ followed by a column address strobed-in by $\overline{CAS}$. $\overline{CAS}$ may be toggled-in by holding $\overline{RAS}$ LOW and strobing-in different column addresses, thus executing faster memory cycles. Returning $\overline{RAS}$ HIGH terminates the FAST PAGE MODE cycle.

Returning $\overline{RAS}$ and $\overline{CAS}$ HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the $\overline{RAS}$ high time. Memory cell data is retained in its correct state by maintaining power and executing any $\overline{RAS}$ cycle (READ, WRITE, $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$ (CBR) or HIDDEN refresh) so that all 512 combinations of $\overline{RAS}$ addresses (A0-A8) are executed at least every 8ms, regardless of sequence. The CBR refresh cycle will invoke the internal refresh counter for automatic $\overline{RAS}$ addressing.

FUNCTIONAL BLOCK DIAGRAM
FAST PAGE MODE



*NOTE: $\overline{WE}$ LOW prior to $\overline{CAS}$ LOW, EW detection circuit output is a HIGH (EARLY-WRITE)
$\overline{CAS}$ LOW prior to $\overline{WE}$ LOW, EW detection circuit output is a LOW (LATE-WRITE)

TRUTH TABLE

FUNCTION		$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	$\overline{OE}$	ADDRESSES t_R	ADDRESSES t_C	DATA IN/OUT DQ1-DQ4
Standby		H	H→X	X	X	X	X	High-Z
READ		L	L	H	L	ROW	COL	Data Out
EARLY-WRITE		L	L	L	X	ROW	COL	Data In
READ-WRITE		L	L	H→L	L→H	ROW	COL	Data Out, Data In
FAST-PAGE-MODE	1st Cycle	L	H→L	H	L	ROW	COL	Data Out
READ	2nd Cycle	L	H→L	H	L	n/a	COL	Data Out
FAST-PAGE-MODE	1st Cycle	L	H→L	L	X	ROW	COL	Data In
EARLY-WRITE	2nd Cycle	L	H→L	L	X	n/a	COL	Data In
FAST-PAGE-MODE	1st Cycle	L	H→L	H→L	L→H	ROW	COL	Data Out, Data In
READ-WRITE	2nd Cycle	L	H→L	H→L	L→H	n/a	COL	Data Out, Data In
$\overline{RAS}$-ONLY REFRESH		L	H	X	X	ROW	n/a	High-Z
HIDDEN	READ	L→H→L	L	H	L	ROW	COL	Data Out
REFRESH	WRITE	L→H→L	L	L	X	ROW	COL	Data In
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH		H→L	L	X	X	X	X	High-Z

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Vss ..... -1V to +7V
Operating Temperature, T_A (Ambient) ..... 0°C to +70°C
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 3, 4, 6, 7) (V_{CC} = 5V ±10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.5	V	1
Input High (Logic 1) Voltage, All Inputs	V_{IH}	2.4	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, All Inputs	V_{IL}	-1.0	0.8	V	1
INPUT LEAKAGE CURRENT Any Input 0V ≤ V_{IN} ≤ 6.5V (All other pins not under test = 0V)	I_I	-2	2	µA	
OUTPUT LEAKAGE CURRENT: (Q is disabled; 0V ≤ V_{OUT} ≤ 5.5V)	I_{OZ}	-10	10	µA	
OUTPUT LEVELS Output High Voltage (I_{OUT} = -5mA)	V_{OH}	2.4		V	
Output Low Voltage (I_{OUT} = 4.2mA)	V_{OL}		0.4	V	

		MAX				
PARAMETER/CONDITION	SYMBOL	-6	-7	-8	UNITS	NOTES
STANDBY CURRENT: (TTL) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC1}	2	2	2	mA	
STANDBY CURRENT: (CMOS) ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} -0.2V)	I_{CC2}	1	1	1	mA	
OPERATING CURRENT: Random READ/WRITE Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC (MIN))	I_{CC3}	90	80	70	mA	3, 4
OPERATING CURRENT: FAST PAGE MODE Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: ^tPC = ^tPC (MIN))	I_{CC4}	70	60	50	mA	3, 4
REFRESH CURRENT: $\overline{RAS}$-ONLY Average power supply current ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}: ^tRC = ^tRC (MIN))	I_{CC5}	90	80	70	mA	3
REFRESH CURRENT: $\overline{CAS}$-BEFORE-$\overline{RAS}$ Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC (MIN))	I_{CC6}	90	80	70	mA	3, 5

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A8	C_{I1}		5	pF	2
Input Capacitance: $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$	C_{I2}		7	pF	2
Input/Output Capacitance: DQ	C_{IO}		7	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13, 23) (V_{CC} = 5V ±10%)

AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	^tRC	110		130		150		ns	
READ-WRITE cycle time	^tRWC	165		185		205		ns	
FAST-PAGE-MODE READ or WRITE cycle time	^tPC	40		40		45		ns	
FAST-PAGE-MODE READ-WRITE cycle time	^tPRWC	90		95		100		ns	
Access time from $\overline{RAS}$	^tRAC		60		70		80	ns	14
Access time from $\overline{CAS}$	^tCAC		20		20		20	ns	15
Output Enable	^tOE		20		20		20	ns	
Access time from column address	^tAA		30		35		40	ns	
Access time from $\overline{CAS}$ precharge	^tCPA		35		40		45	ns	
$\overline{RAS}$ pulse width	^tRAS	60	100,000	70	100,000	80	100,000	ns	
$\overline{RAS}$ pulse width (FAST PAGE MODE)	^tRASP	60	100,000	70	100,000	80	100,000	ns	
$\overline{RAS}$ hold time	^tRSH	20		20		20		ns	
$\overline{RAS}$ precharge time	^tRP	40		50		60		ns	
$\overline{CAS}$ pulse width	^tCAS	20	100,000	20	100,000	20	100,000	ns	
$\overline{CAS}$ hold time	^tCSH	60		70		80		ns	
$\overline{CAS}$ precharge time	^tCPN	10		10		10		ns	16
$\overline{CAS}$ precharge time (FAST PAGE MODE)	^tCP	10		10		10		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	^tRCD	20	40	20	50	20	60	ns	17
$\overline{CAS}$ to $\overline{RAS}$ precharge time	^tCRP	5		5		5		ns	
Row address setup time	^tASR	0		0		0		ns	
Row address hold time	^tRAH	10		10		10		ns	
$\overline{RAS}$ to column address delay time	^tRAD	15	30	15	35	15	40	ns	18
Column address setup time	^tASC	0		0		0		ns	
Column address hold time	^tCAH	15		15		15		ns	
Column address hold time (referenced to $\overline{RAS}$)	^tAR	45		55		60		ns	
Column address to $\overline{RAS}$ lead time	^tRAL	30		35		40		ns	
Read command setup time	^tRCS	0		0		0		ns	
Read command hold time (referenced to $\overline{CAS}$)	^tRCH	0		0		0		ns	19
Read command hold time (referenced to $\overline{RAS}$)	^tRRH	0		0		0		ns	19
$\overline{CAS}$ to output in Low-Z	^tCLZ	0		0		0		ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

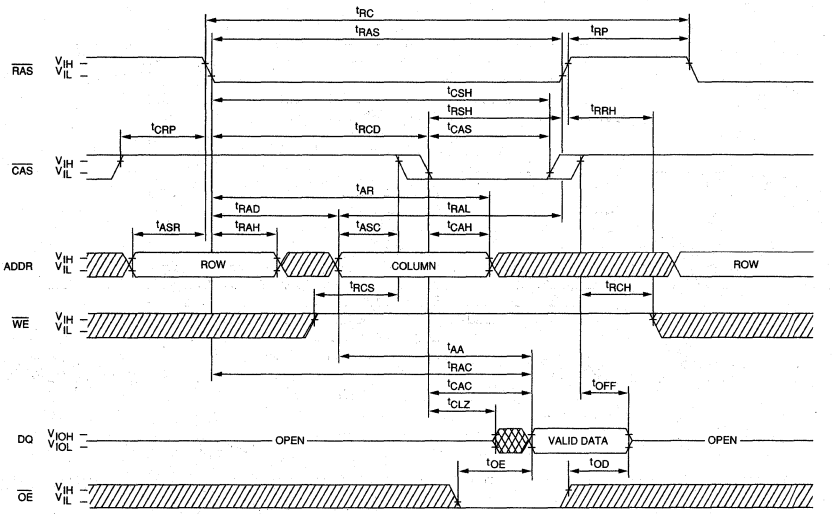
(Notes: 6, 7, 8, 9, 10, 11, 12, 13, 23) (Vcc = 5V ±10%)

AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Output buffer turn-off delay	^tOFF	0	20	0	20	0	20	ns	20, 26
Output disable	^tOD		15		20		20	ns	26
$\overline{WE}$ command setup time	^tWCS	0		0		0		ns	21
Write command hold time	^tWCH	10		15		15		ns	
Write command hold time (referenced to $\overline{RAS}$)	^tWCR	45		55		60		ns	
Write command pulse width	^tWP	10		15		15		ns	
Write command to $\overline{RAS}$ lead time	^tRWL	20		20		20		ns	
Write command to $\overline{CAS}$ lead time	^tCWL	20		20		20		ns	
Data-in setup time	^tDS	0		0		0		ns	22
Data-in hold time	^tDH	15		15		15		ns	22
Data-in hold time (referenced to $\overline{RAS}$)	^tDHR	45		55		60		ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	^tRWD	85		100		110		ns	21
Column address to $\overline{WE}$ delay time	^tAWD	60		65		70		ns	21
$\overline{CAS}$ to $\overline{WE}$ delay time	^tCWD	40		50		55		ns	21
Transition time (rise or fall)	^tT	3	50	3	50	3	50	ns	9, 10
Refresh period (512 cycles)	^tREF		8		8		8	ms	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	^tRPC	0		0		0		ns	
$\overline{CAS}$ setup time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tCSR	10		10		10		ns	5
$\overline{CAS}$ hold time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tCHR	10		15		15		ns	5
$\overline{OE}$ hold time from $\overline{WE}$ during READ-MODIFY-WRITE cycle	^tOEH	15		20		20		ns	25
$\overline{OE}$ setup prior to $\overline{RAS}$ during HIDDEN REFRESH cycle	^tORD	0		0		0		ns	24

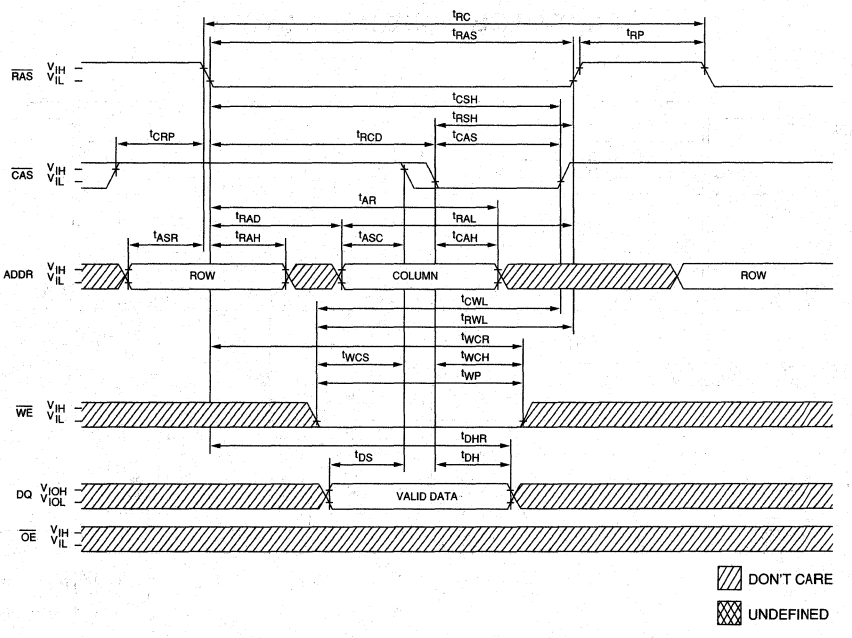
NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. V_{CC} = 5V ±10%, f = 1 MHz.
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is assured.
7. An initial pause of 100µs is required after power-up followed by any eight $\overline{RAS}$ cycles before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-up should be repeated any time the ^{t}REF refresh requirement is exceeded.
8. AC characteristics assume ^{t}T = 5ns.
9. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS}$ = V_{IH}, data output is High-Z.
12. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to 2 TTL gates and 100pF.
14. Assumes that $^{t}RCD < {}^{t}RCD$ (MAX). If ^{t}RCD is greater than the maximum recommended value shown in this table, ^{t}RAC will increase by the amount that ^{t}RCD exceeds the value shown.
15. Assumes that $^{t}RCD \geq {}^{t}RCD$ (MAX).
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer, $\overline{CAS}$ must be pulsed HIGH for ^{t}CPN.
17. Operation within the ^{t}RCD (MAX) limit ensures that ^{t}RAC (MAX) can be met. ^{t}RCD (MAX) is specified as a reference point only; if ^{t}RCD is greater than the specified ^{t}RCD (MAX) limit, then access time is controlled exclusively by ^{t}CAC.
18. Operation within the ^{t}RAD (MAX) limit ensures that ^{t}RAC (MIN) and ^{t}CAC (MIN) can be met. ^{t}RAD (MAX) is specified as a reference point only; if ^{t}RAD is greater than the specified ^{t}RAD (MAX) limit, then access time is controlled exclusively by ^{t}AA.
19. Either ^{t}RCH or ^{t}RRH must be satisfied for a READ cycle.
20. ^{t}OFF (MAX) defines the time at which the output achieves the open circuit condition, and is not referenced to V_{OH} or V_{OL}.
21. ^{t}WCS, ^{t}RWD, ^{t}AWD and ^{t}CWD are not restrictive operating parameters. ^{t}WCS applies to EARLY-WRITE cycles. ^{t}RWD, ^{t}AWD and ^{t}CWD apply to READ-MODIFY-WRITE cycles. If $^{t}WCS \geq {}^{t}WCS$ (MIN), the cycle is an EARLY-WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If $^{t}RWD \geq {}^{t}RWD$ (MIN), $^{t}AWD \geq {}^{t}AWD$ (MIN) and $^{t}CWD \geq {}^{t}CWD$ (MIN), the cycle is a READ-MODIFY-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of data out is indeterminate. $\overline{OE}$ held HIGH and $\overline{WE}$ taken LOW after $\overline{CAS}$ goes LOW results in a LATE-WRITE ($\overline{OE}$ controlled) cycle. ^{t}WCS, ^{t}RWD, ^{t}CWD and ^{t}AWD are not applicable in a LATE-WRITE cycle.
22. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY-WRITE cycles and $\overline{WE}$ leading edge in LATE-WRITE or READ-MODIFY-WRITE cycles.
23. If $\overline{OE}$ is tied permanently LOW, LATE-WRITE or READ-MODIFY-WRITE operations are not possible.
24. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW and $\overline{OE}$ = HIGH.
25. LATE-WRITE and READ-MODIFY-WRITE cycles must have both ^{t}OD and ^{t}OEH met ($\overline{OE}$ HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. The DQs will provide the previously read data if $\overline{CAS}$ remains LOW and $\overline{OE}$ is taken back LOW after ^{t}OEH is met. If $\overline{CAS}$ goes HIGH prior to $\overline{OE}$ going back LOW, the DQs will remain open.
26. The DQs open during READ cycles once ^{t}OD or ^{t}OFF occur. If $\overline{CAS}$ goes HIGH first, $\overline{OE}$ becomes a "don't care." If $\overline{OE}$ goes HIGH and $\overline{CAS}$ stays LOW, $\overline{OE}$ is not a "don't care;" and the DQs will provide the previously read data if $\overline{OE}$ is taken back LOW (while $\overline{CAS}$ remains LOW).

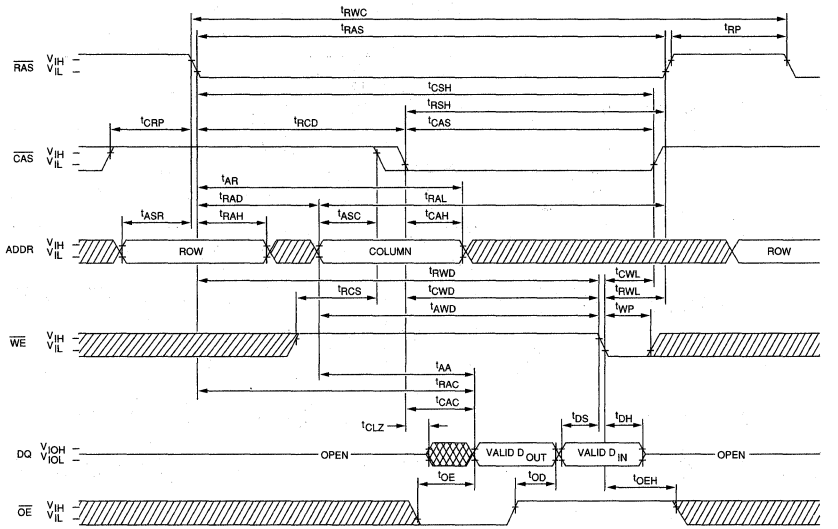
READ CYCLE



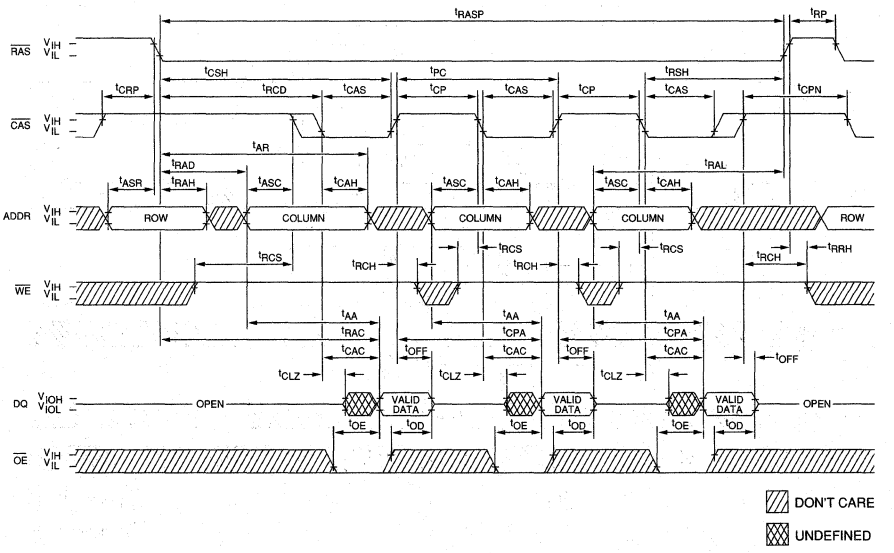
EARLY-WRITE CYCLE



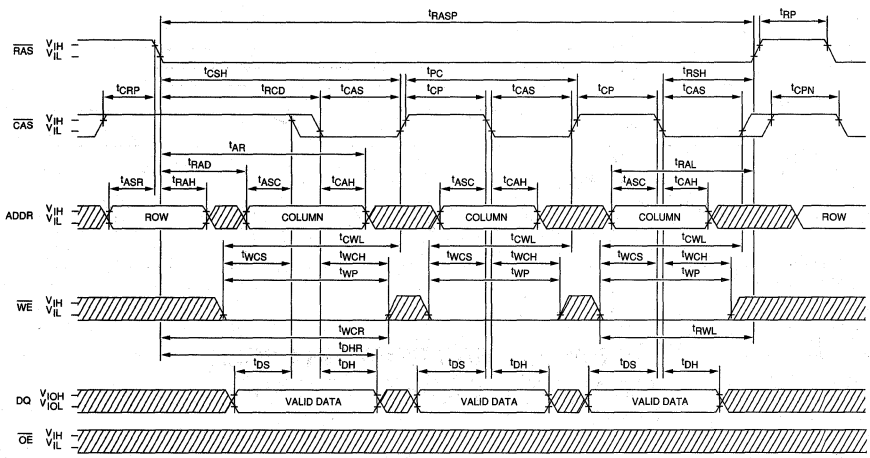
READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)



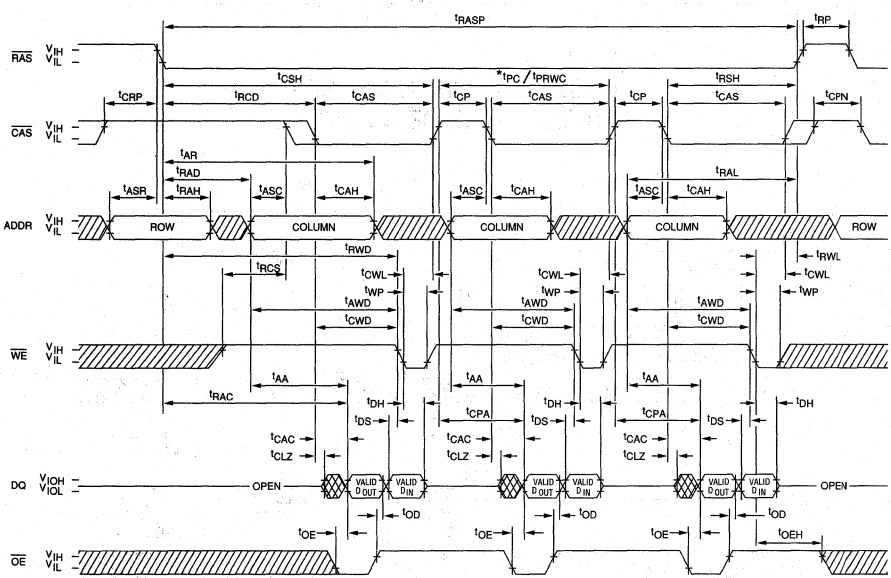
FAST-PAGE-MODE READ CYCLE



FAST-PAGE-MODE EARLY-WRITE CYCLE

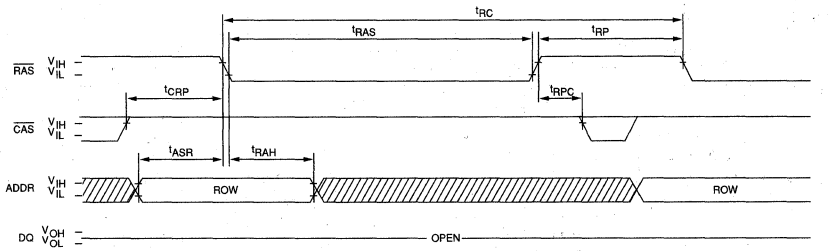


FAST-PAGE-MODE READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)

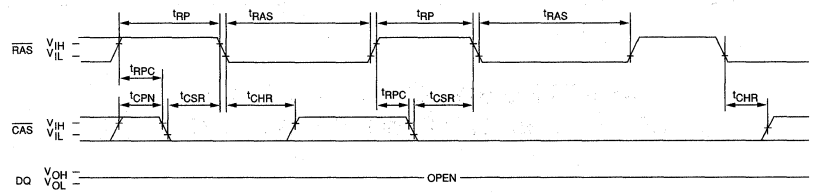


*tPC is for LATE-WRITE only.

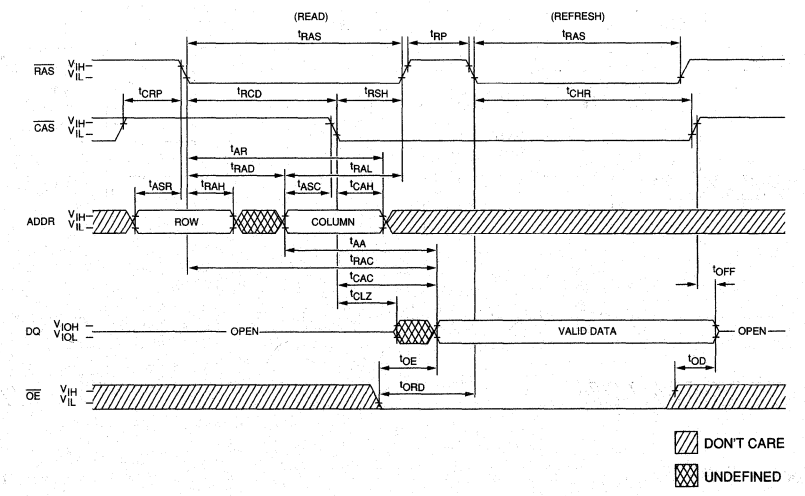
RAS-ONLY REFRESH CYCLE
(ADDR = A0-A8; WE = DON'T CARE)



CAS-BEFORE-RAS REFRESH CYCLE
(A0-A8, WE and OE = DON'T CARE)



HIDDEN REFRESH CYCLE [24]
(WE = HIGH; OE = LOW)



DRAM

256K x 4 DRAM

LOW POWER, EXTENDED REFRESH

FEATURES

- Industry standard x4 pinout, timing, functions and packages
- High-performance, CMOS silicon-gate process
- Single +5V ±10% power supply
- Low power, .3mW standby; 150mW active, typical
- All inputs, outputs and clocks are fully TTL compatible
- Optional FAST PAGE MODE access cycle
- Refresh modes: $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$ (CBR), HIDDEN and BATTERY BACKUP (BBU)
- 512-cycle extended refresh in 64ms
- Low CMOS STANDBY CURRENT, 200µA Maximum

OPTIONS — MARKING

- Timing

70ns access	- 7
80ns access	- 8
100ns access	-10

- Packages

Plastic DIP (300 mil)	None
Plastic SOJ (300 mil)	DJ
Plastic TSOP (300 mil)*	TG
Plastic ZIP (350 mil)	Z

NOTE: Available in die form (commercial or military) or military ceramic packages. Please consult factory for die data sheets or refer to Micron's ***Military Data Book.***

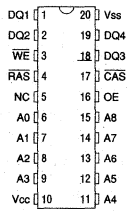
- Operating Temperature, T_A

Commercial (0°C to +70°C)	None
Industrial (-40°C to +85°C)	IT

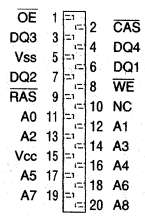
- Part Number Example: MT4C4256DJ-7 L

PIN ASSIGNMENT (Top View)

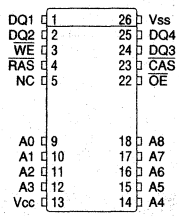
20-Pin DIP (N-2)



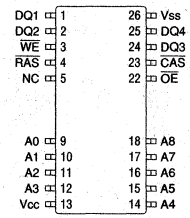
20-Pin ZIP (O-1)



20-Pin SOJ (Q-1)



20-Pin TSOP (R-1)



*Consult factory on availability of reverse pinout TSOP packages

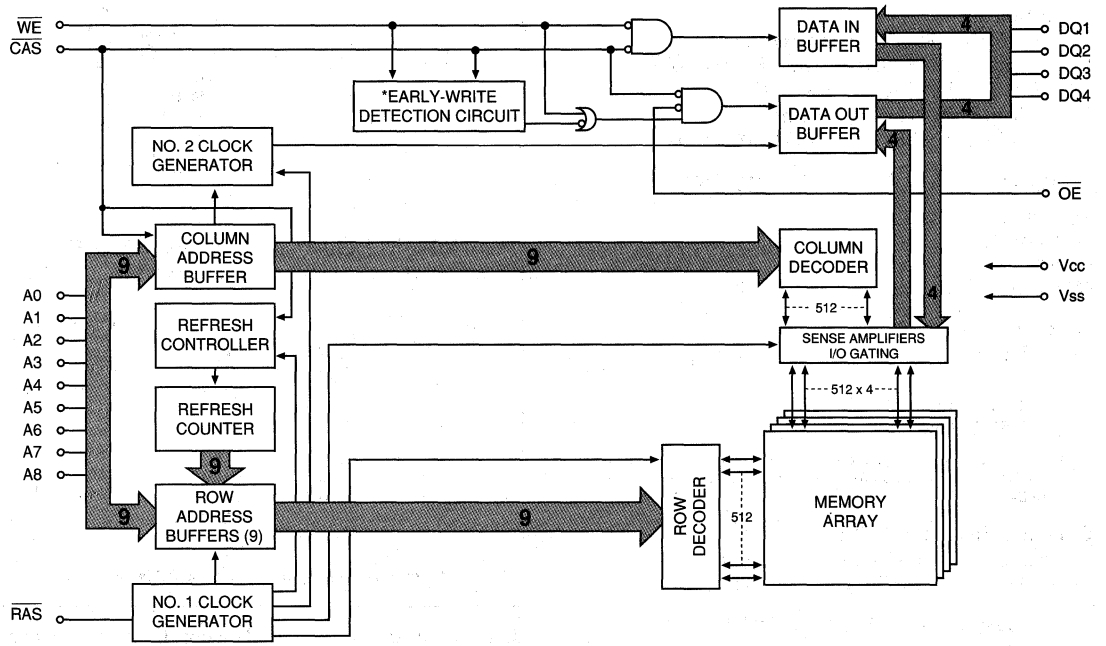
GENERAL DESCRIPTION

The MT4C4256 L is a randomly accessed solid-state memory containing 1,048,576 bits organized in a x4 configuration. During READ or WRITE cycles, each bit is uniquely addressed through the 18 address bits, which are entered 9 bits (A0-A8) at a time. $\overline{RAS}$ is used to latch the first 9 bits and $\overline{CAS}$ the latter 9 bits. READ and WRITE cycles are selected with the $\overline{WE}$ input. A logic HIGH on $\overline{WE}$ dictates READ mode while a logic LOW on $\overline{WE}$ dictates WRITE mode. During a WRITE cycle, data in (D) is latched by the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. If $\overline{WE}$ goes LOW prior to $\overline{CAS}$ going LOW, the output pin(s) remain open (High-Z) until the next $\overline{CAS}$ cycle. If $\overline{WE}$ goes LOW after data reaches the output pin, data out (Q) is activated and retains the selected cell data as long as $\overline{CAS}$ remains LOW (regardless of $\overline{WE}$ or $\overline{RAS}$). This late $\overline{WE}$ pulse results in a READ-WRITE cycle. The four data inputs and four data outputs are routed through four pins using common I/O, and pin direction is controlled by $\overline{WE}$ and $\overline{OE}$.

FAST PAGE MODE operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row address (A0-A8) defined page boundary. The FAST PAGE MODE cycle is always initiated with a row address strobed-in by $\overline{RAS}$ followed by a column address strobed-in by $\overline{CAS}$. $\overline{CAS}$ may be toggled-in by holding $\overline{RAS}$ LOW and strobing-in different column addresses, thus executing faster memory cycles. Returning $\overline{RAS}$ HIGH terminates the FAST PAGE MODE cycle.

Returning $\overline{RAS}$ and $\overline{CAS}$ HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the $\overline{RAS}$ high time. Memory cell data is retained in its correct state by maintaining power and executing any $\overline{RAS}$ cycle (READ, WRITE, $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$ (CBR), or HIDDEN refresh) so that all 512 combinations of $\overline{RAS}$ addresses (A0-A8) are executed at least every 64ms, regardless of sequence. The CBR refresh cycle will invoke the internal refresh counter for automatic $\overline{RAS}$ addressing.

FUNCTIONAL BLOCK DIAGRAM
FAST PAGE MODE



*NOTE: $\overline{WE}$ LOW prior to $\overline{CAS}$ LOW, EW detection circuit output is a HIGH (EARLY-WRITE)
$\overline{CAS}$ LOW prior to $\overline{WE}$ LOW, EW detection circuit output is a LOW (LATE-WRITE)

TRUTH TABLE

FUNCTION		RAS	CAS	WE	OE	ADDRESSES		DATA IN/OUT
						^tR	^tC	DQ1-DQ4
Standby		H	H→X	X	X	X	X	High-Z
READ		L	L	H	L	ROW	COL	Data Out
EARLY-WRITE		L	L	L	X	ROW	COL	Data In
READ-WRITE		L	L	H→L	L→H	ROW	COL	Data Out, Data In
FAST-PAGE-MODE	1st Cycle	L	H→L	H	L	ROW	COL	Data Out
READ	2nd Cycle	L	H→L	H	L	n/a	COL	Data Out
FAST-PAGE-MODE	1st Cycle	L	H→L	L	X	ROW	COL	Data In
EARLY-WRITE	2nd Cycle	L	H→L	L	X	n/a	COL	Data In
FAST-PAGE-MODE	1st Cycle	L	H→L	H→L	L→H	ROW	COL	Data Out, Data In
READ-WRITE	2nd Cycle	L	H→L	H→L	L→H	n/a	COL	Data Out, Data In
RAS-ONLY REFRESH		L	H	X	X	ROW	n/a	High-Z
HIDDEN	READ	L→H→L	L	H	L	ROW	COL	Data Out
REFRESH	WRITE	L→H→L	L	L	X	ROW	COL	Data In
CAS-BEFORE-RAS REFRESH		H→L	L	X	X	X	X	High-Z
BATTERY BACKUP REFRESH		H→L	L	X	X	X	X	High-Z

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to V_{SS} ..... -1V to +7V
Operating Temperature, T_A (Ambient) ..... 0°C to +70°C
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 3, 4, 6, 7) (V_{CC} = 5V ±10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.5	V	1
Input High (Logic 1) Voltage, All Inputs	V_{IH}	2.4	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, All Inputs	V_{IL}	-1.0	0.8	V	1
INPUT LEAKAGE CURRENT Any Input 0V ≤ V_{IN} ≤ 6.5V (All other pins not under test = 0V)	I_I	-2	2	µA	
OUTPUT LEAKAGE CURRENT: (Q is disabled; 0V ≤ V_{OUT} ≤ 5.5V)	I_{OZ}	-10	10	µA	
OUTPUT LEVELS Output High Voltage (I_{OUT} = -5mA)	V_{OH}	2.4		V	
Output Low Voltage (I_{OUT} = 4.2mA)	V_{OL}		0.4	V	

		MAX				
PARAMETER/CONDITION	SYMBOL	-7	-8	-10	UNITS	NOTES
STANDBY CURRENT: (TTL) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC1}	2	2	2	mA	
STANDBY CURRENT: (CMOS) ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} -0.2V)	I_{CC2}	200	200	200	µA	
OPERATING CURRENT: Random READ/WRITE Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Single Address Cycling: ^tRC = ^tRC (MIN))	I_{CC3}	75	65	55	mA	3, 4
OPERATING CURRENT: FAST PAGE MODE Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: ^tPC = ^tPC (MIN))	I_{CC4}	55	45	40	mA	3, 4
REFRESH CURRENT: $\overline{RAS}$-ONLY Average power supply current ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}: ^tRC = ^tRC (MIN))	I_{CC5}	75	65	55	mA	3
REFRESH CURRENT: $\overline{CAS}$-BEFORE-$\overline{RAS}$ (CBR) Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC (MIN))	I_{CC6}	75	65	60	mA	3, 5
REFRESH CURRENT: BATTERY BACKUP (BBU) Average power supply current during BATTERY BACKUP refresh: $\overline{CAS}$ = 0.2V or $\overline{CAS}$-BEFORE-$\overline{RAS}$ cycling; $\overline{RAS}$ = ^tRAS (MIN) to 1µs; $\overline{WE}$, A0-A9 and D_{IN} = Vcc -0.2V or 0.2V (D_{IN} may be left OPEN), ^tRC = 125µs (512 rows at 125µs = 64ms)	I_{CC7}	200	200	200	µA	3, 5, 7, 27

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A8	C_{I1}		5	pF	2
Input Capacitance: $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$	C_{I2}		7	pF	2
Input/Output Capacitance: DQ	C_{IO}		7	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13, 23) (V_{CC} = 5V ±10%)

AC CHARACTERISTICS		-7		-8		-10			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	t_{RC}	130		150		180		ns	
READ-WRITE cycle time	t_{RWC}	185		205		245		ns	
FAST-PAGE-MODE READ or WRITE cycle time	t_{PC}	40		45		55		ns	
FAST-PAGE-MODE READ-WRITE cycle time	t_{PRWC}	95		100		115		ns	
Access time from $\overline{RAS}$	t_{RAC}		70		80		100	ns	14
Access time from $\overline{CAS}$	t_{CAC}		20		20		25	ns	15
Output Enable	t_{OE}		20		20		25	ns	
Access time from column address	t_{AA}		35		40		50	ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		40		45		50	ns	
$\overline{RAS}$ pulse width	t_{RAS}	70	100,000	80	100,000	100	100,000	ns	
$\overline{RAS}$ pulse width (FAST PAGE MODE)	t_{RASP}	70	100,000	80	100,000	100	100,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	20		20		25		ns	
$\overline{RAS}$ precharge time	t_{RP}	50		60		70		ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	100,000	20	100,000	25	100,000	ns	
$\overline{CAS}$ hold time	t_{CSH}	70		80		100		ns	
$\overline{CAS}$ precharge time	t_{CPN}	10		10		15		ns	16
$\overline{CAS}$ precharge time (FAST PAGE MODE)	t_{CP}	10		10		10		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	50	20	60	25	75	ns	17
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		5		ns	
Row address setup time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	10		10		15		ns	
$\overline{RAS}$ to column address delay time	t_{RAD}	15	35	15	40	20	50	ns	18
Column address setup time	t_{ASC}	0		0		0		ns	
Column address hold time	t_{CAH}	15		15		20		ns	
Column address hold time (referenced to $\overline{RAS}$)	t_{AR}	55		60		70		ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	35		40		50		ns	
Read command setup time	t_{RCS}	0		0		0		ns	
Read command hold time (referenced to $\overline{CAS}$)	t_{RCH}	0		0		0		ns	19
Read command hold time (referenced to $\overline{RAS}$)	t_{RRH}	0		0		0		ns	19
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	0		0		0		ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

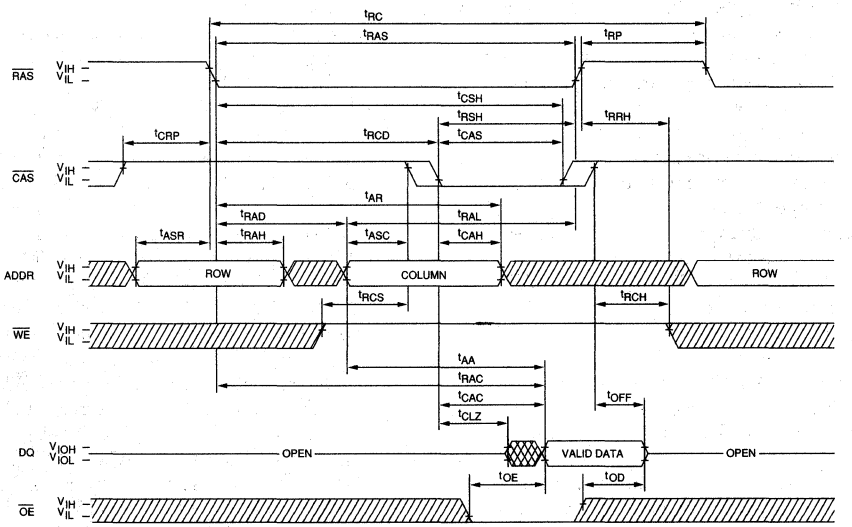
(Notes: 6, 7, 8, 9, 10, 11, 12, 13, 23) (V_{CC} = 5V ±10%)

AC CHARACTERISTICS		-7		-8		-10			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Output buffer turn-off delay	^tOFF	0	20	0	20	0	20	ns	20, 26
Output disable	^tOD		20		20		20	ns	26
$\overline{WE}$ command setup time	^tWCS	0		0		0		ns	21
Write command hold time	^tWCH	15		15		20		ns	
Write command hold time (referenced to $\overline{RAS}$)	^tWCR	55		60		75		ns	
Write command pulse width	^tWP	15		15		20		ns	
Write command to $\overline{RAS}$ lead time	^tRWL	20		20		25		ns	
Write command to $\overline{CAS}$ lead time	^tCWL	20		20		25		ns	
Data-in setup time	^tDS	0		0		0		ns	22
Data-in hold time	^tDH	15		15		20		ns	22
Data-in hold time (referenced to $\overline{RAS}$)	^tDHR	55		60		75		ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	^tRWD	100		110		130		ns	21
Column address to $\overline{WE}$ delay time	^tAWD	65		70		80		ns	21
$\overline{CAS}$ to $\overline{WE}$ delay time	^tCWD	50		55		60		ns	21
Transition time (rise or fall)	^tT	3	50	3	50	3	50	ns	9, 10
Refresh period (512 cycles)	^tREF		64		64		64	ms	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	^tRPC	0		0		0		ns	
$\overline{CAS}$ setup time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tCSR	10		10		10		ns	5
$\overline{CAS}$ hold time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tCHR	15		15		15		ns	5
$\overline{OE}$ hold time from $\overline{WE}$ during READ-MODIFY-WRITE cycle	^tOEH	20		20		20		ns	25
$\overline{OE}$ setup prior to $\overline{RAS}$ during HIDDEN REFRESH cycle	^tORD	0		0		0		ns	24

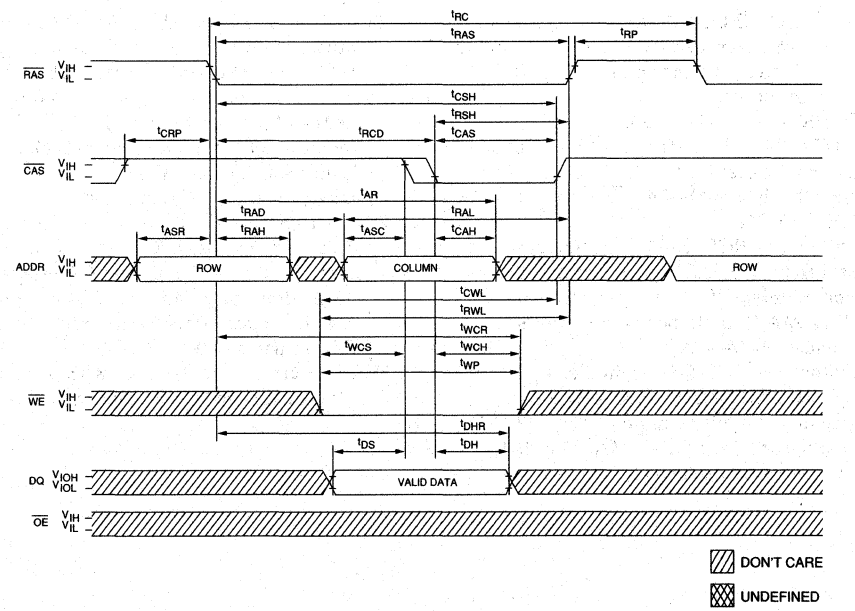
NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. V_{CC} = 5V ±10%, f = 1 MHz.
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is assured.
7. An initial pause of 100µs is required after power-up followed by any eight $\overline{RAS}$ cycles before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-up should be repeated any time the ^{t}REF refresh requirement is exceeded.
8. AC characteristics assume ^{t}T = 5ns.
9. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS}$ = V_{IH}, data output is High-Z.
12. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to 2 TTL gates and 100pF.
14. Assumes that $^{t}RCD < {}^{t}RCD$ (MAX). If ^{t}RCD is greater than the maximum recommended value shown in this table, ^{t}RAC will increase by the amount that ^{t}RCD exceeds the value shown.
15. Assumes that $^{t}RCD \geq {}^{t}RCD$ (MAX).
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer, $\overline{CAS}$ must be pulsed HIGH for ^{t}CPN.
17. Operation within the ^{t}RCD (MAX) limit ensures that ^{t}RAC (MAX) can be met. ^{t}RCD (MAX) is specified as a reference point only; if ^{t}RCD is greater than the specified ^{t}RCD (MAX) limit, then access time is controlled exclusively by ^{t}CAC.
18. Operation within the ^{t}RAD (MAX) limit ensures that ^{t}RAC (MIN) and ^{t}CAC (MIN) can be met. ^{t}RAD (MAX) is specified as a reference point only; if ^{t}RAD is greater than the specified ^{t}RAD (MAX) limit, then access time is controlled exclusively by ^{t}AA.
19. Either ^{t}RCH or ^{t}RRH must be satisfied for a READ cycle.
20. ^{t}OFF (MAX) defines the time at which the output achieves the open circuit condition, and is not referenced to V_{OH} or V_{OL}.
21. ^{t}WCS, ^{t}RWD, ^{t}AWD and ^{t}CWD are not restrictive operating parameters. ^{t}WCS applies to EARLY-WRITE cycles. ^{t}RWD, ^{t}AWD and ^{t}CWD apply to READ-MODIFY-WRITE cycles. If $^{t}WCS \geq {}^{t}WCS$ (MIN), the cycle is an EARLY-WRITE cycle, and the data output will remain an open circuit throughout the entire cycle. If $^{t}RWD \geq {}^{t}RWD$ (MIN), $^{t}AWD \geq {}^{t}AWD$ (MIN) and $^{t}CWD \geq {}^{t}CWD$ (MIN), the cycle is a READ-MODIFY-WRITE cycle, and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of data out is indeterminate. $\overline{OE}$ held HIGH and $\overline{WE}$ taken LOW after $\overline{CAS}$ goes LOW results in a LATE-WRITE ($\overline{OE}$ controlled) cycle. ^{t}WCS, ^{t}RWD, ^{t}CWD and ^{t}AWD are not applicable in a LATE-WRITE cycle.
22. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY-WRITE cycles and $\overline{WE}$ leading edge in LATE-WRITE or READ-MODIFY-WRITE cycles.
23. If $\overline{OE}$ is tied permanently LOW, LATE-WRITE or READ-MODIFY-WRITE operations are not possible.
24. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW and $\overline{OE}$ = HIGH.
25. LATE-WRITE and READ-MODIFY-WRITE cycles must have both ^{t}OD and ^{t}OEH met ($\overline{OE}$ HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. The DQs will provide the previously read data if $\overline{CAS}$ remains LOW and $\overline{OE}$ is taken back LOW after ^{t}OEH is met. If $\overline{CAS}$ goes HIGH prior to $\overline{OE}$ going back LOW, the DQs will remain open.
26. The DQs open during READ cycles once ^{t}OD or ^{t}OFF occur. If $\overline{CAS}$ goes HIGH first, $\overline{OE}$ becomes a "don't care." If $\overline{OE}$ goes HIGH and $\overline{CAS}$ stays LOW, $\overline{OE}$ is not a "don't care," and the DQs will provide the previously read data if $\overline{OE}$ is taken back LOW (while $\overline{CAS}$ remains LOW).
27. BBU current is reduced as ^{t}RAS is reduced from its maximum specification during the BBU cycle.

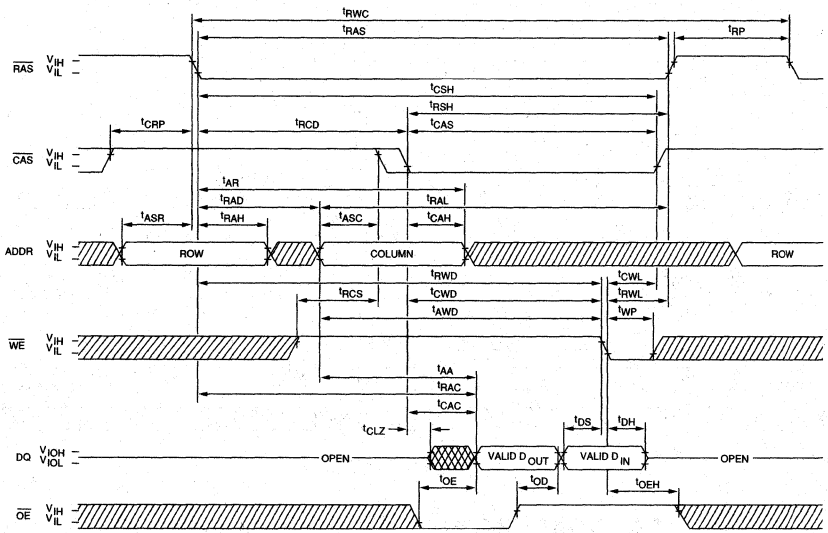
READ CYCLE



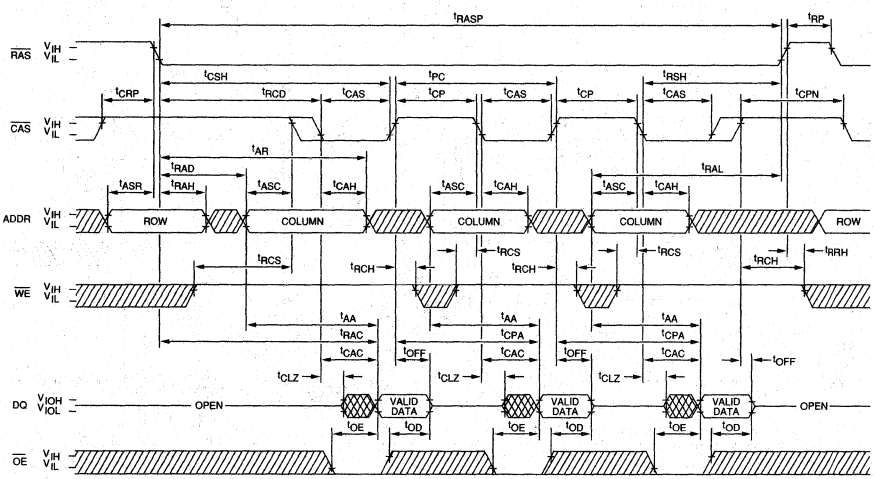
EARLY-WRITE CYCLE



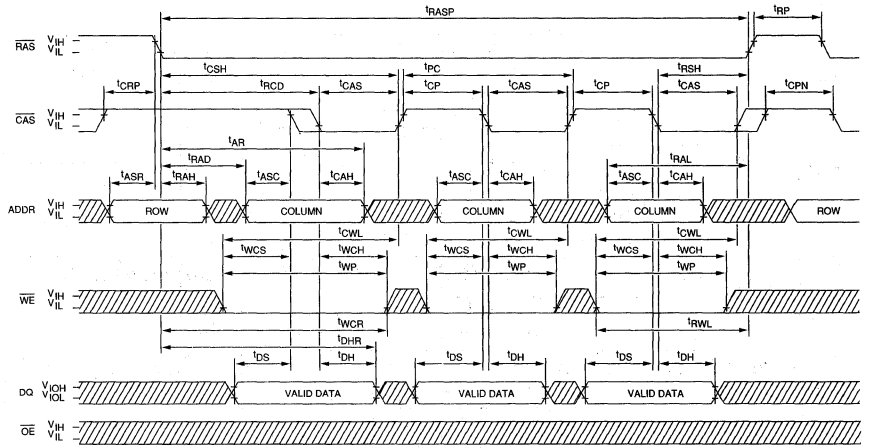
READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)



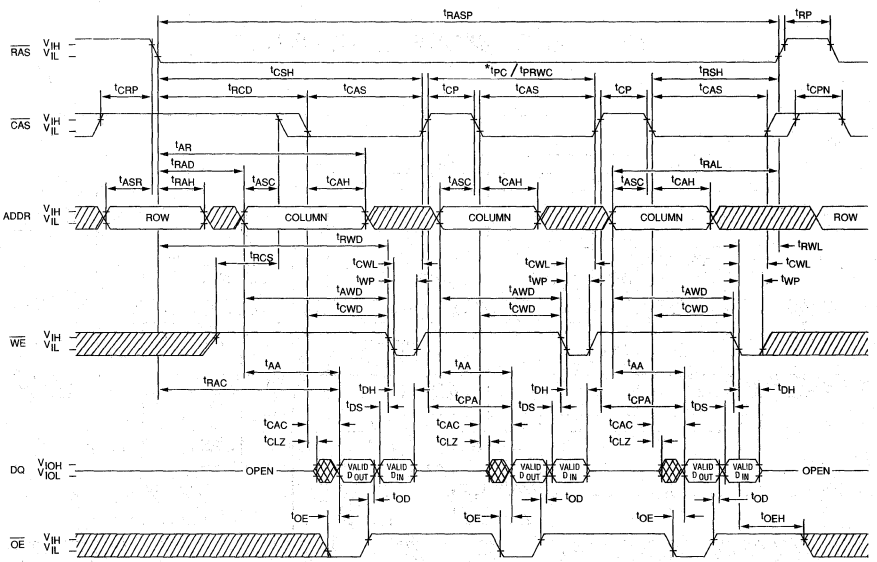
FAST-PAGE-MODE READ CYCLE



FAST-PAGE-MODE EARLY-WRITE CYCLE

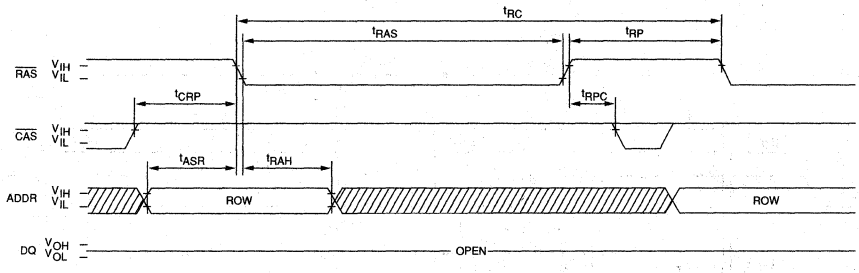


FAST-PAGE-MODE READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)

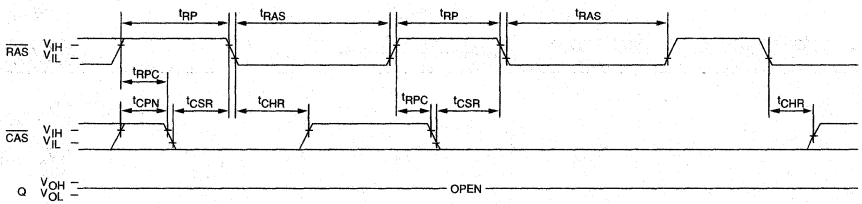


*tPC is for LATE-WRITE only.

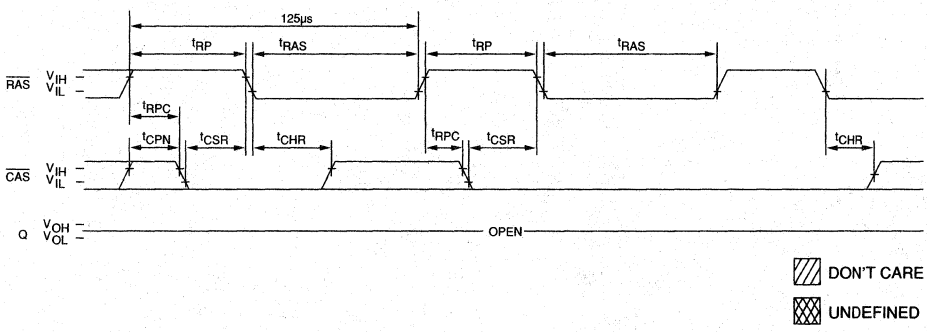
$\overline{\text{RAS}}$-ONLY REFRESH CYCLE
(ADDR = A0-A8; $\overline{\text{WE}}$ = DON'T CARE)



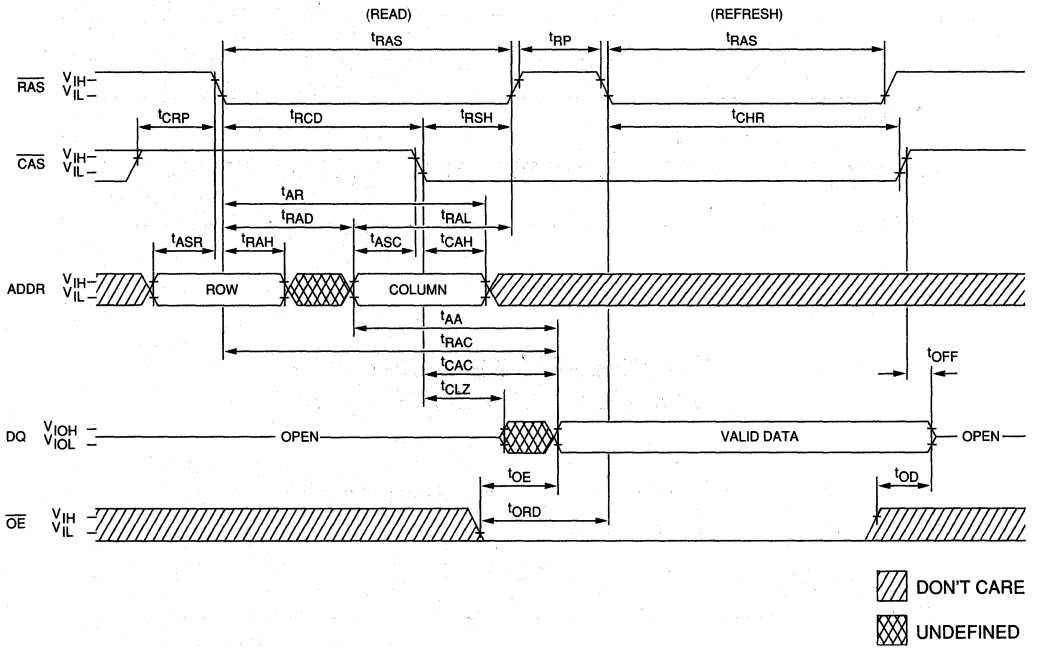
$\overline{\text{CAS}}$-BEFORE-$\overline{\text{RAS}}$ REFRESH CYCLE
(A0-A8, $\overline{\text{WE}}$ and $\overline{\text{OE}}$ = DON'T CARE)



BATTERY BACKUP REFRESH CYCLE
(A0-A8, $\overline{\text{WE}}$ and $\overline{\text{OE}}$ = DON'T CARE)



HIDDEN REFRESH CYCLE [24]
($\overline{WE}$ = HIGH; $\overline{OE}$ = LOW)



DRAM

256K x 4 DRAM

3.3V, EXTENDED REFRESH

FEATURES

- Best memory solution for 3.3V flat-panel controllers
- Single +3.3V ±5% power supply
- TSOP and SOJ compatible with 1 Meg x 4 TSOP
- Industry standard x4 pinout, timing, functions and packages
- High-performance, CMOS silicon-gate process
- All inputs and outputs are TTL compatible
- Optional FAST PAGE MODE access cycle
- Refresh modes: $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$ (CBR), HIDDEN and BATTERY BACKUP (BBU)
- Low power, 0.1mW standby; 100mW active, typical
- 512-cycle extended refresh distributed across 64ms
- Low BBU current, 60µA typical, 90µA (MAX)
- Low STANDBY CURRENT, 25µA typical, 60µA (MAX)

OPTIONS — MARKING

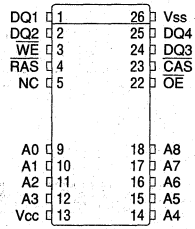
- Timing
  - 100ns access — -10
  - 120ns access — -12
- Packages
  - Plastic SOJ (300 mil) — DJ
  - Plastic TSOP (300 mil) — TG
  - Plastic ZIP (350 mil) — Z

NOTE: Available in die form (commercial or military) or military ceramic packages. Please consult factory for die data sheets or refer to Micron's ***Military Data Book.***

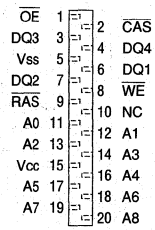
- Part Number Example: MT4C4256DJ-10 VL

PIN ASSIGNMENT (Top View)

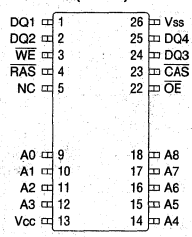
20-Pin SOJ (Q-1)



20-Pin ZIP (O-1)



20-Pin TSOP (R-1)



GENERAL DESCRIPTION

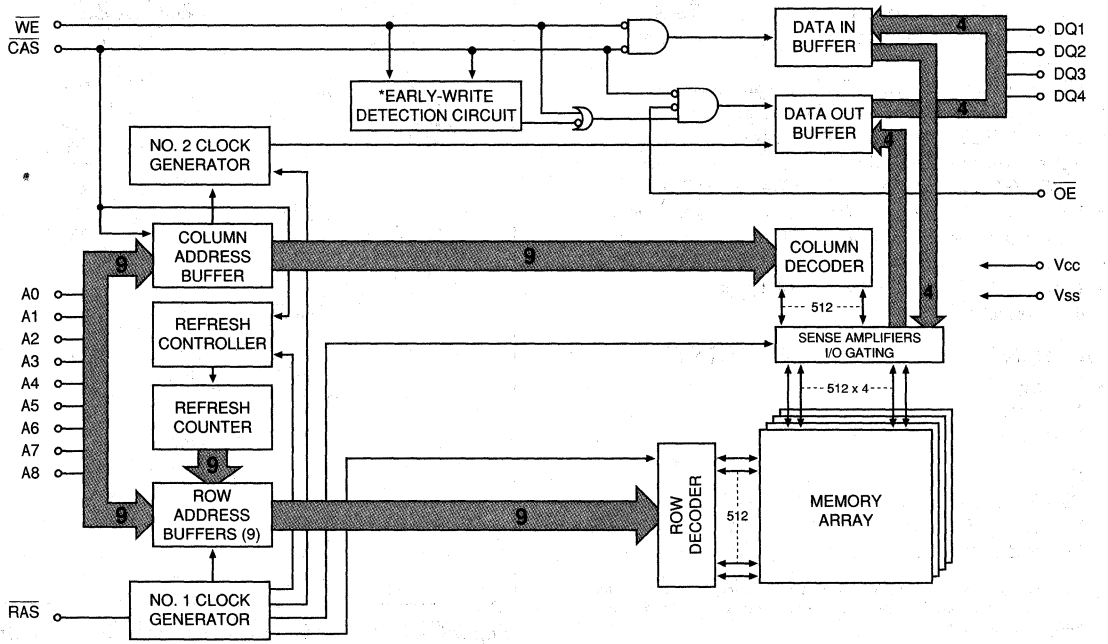
The MT4C4256 VL is specially processed to operate at 3.3 volts allowing for maximum power savings. It is a randomly accessed solid-state memory containing 1,048,576 bits organized in a x4 configuration. During READ or WRITE cycles, each bit is uniquely addressed through the 18 address bits, which are entered 9 bits (A0-A8) at a time. $\overline{RAS}$ is used to latch the first 9 bits and $\overline{CAS}$ the latter 9 bits. READ and WRITE cycles are selected with the $\overline{WE}$ input. A logic HIGH on $\overline{WE}$ dictates READ mode while a logic LOW on $\overline{WE}$ dictates WRITE mode. During a WRITE cycle, data in (D) is latched by the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. If $\overline{WE}$ goes LOW prior to $\overline{CAS}$ going LOW, the output pin(s) remain open (High-Z) until the next $\overline{CAS}$ cycle. If $\overline{WE}$ goes LOW after data reaches the output pin, data out (Q) is activated and retains the selected cell data as long as $\overline{CAS}$ remains LOW (regardless of $\overline{WE}$ or $\overline{RAS}$). This late $\overline{WE}$ pulse results in a READ-WRITE cycle. The four data inputs and four data outputs are routed through four pins using common I/O, and pin direction is controlled by $\overline{WE}$ and $\overline{OE}$.

FAST PAGE MODE operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row address (A0-A8) defined page boundary. The FAST PAGE MODE cycle is always initiated with a row address strobed-in by $\overline{RAS}$ followed by a column address strobed-in by $\overline{CAS}$. $\overline{CAS}$ may be toggled-in by holding $\overline{RAS}$ LOW and strobing-in different column addresses, thus executing faster memory cycles. Returning $\overline{RAS}$ HIGH terminates the FAST PAGE MODE cycle.

Returning $\overline{RAS}$ and $\overline{CAS}$ HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the $\overline{RAS}$ high time. Memory cell data is retained in its correct state by maintaining power and executing any $\overline{RAS}$ cycle

(READ, WRITE, $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$ (CBR) or HIDDEN refresh) so that all 512 combinations of $\overline{RAS}$ addresses (A0-A8) are executed at least every 64ms, regardless of sequence. The CBR and BATTERY BACKUP (BBU) refresh cycles will invoke the internal refresh counter for automatic $\overline{RAS}$ addressing.

FUNCTIONAL BLOCK DIAGRAM
FAST PAGE MODE



*NOTE: $\overline{WE}$ LOW prior to $\overline{CAS}$ LOW, EW detection circuit output is a HIGH (EARLY-WRITE)
$\overline{CAS}$ LOW prior to $\overline{WE}$ LOW, EW detection circuit output is a LOW (LATE-WRITE)

TRUTH TABLE

FUNCTION		RAS	CAS	WE	OE	ADDRESSES ^tR	ADDRESSES ^tC	DATA IN/OUT DQ1-DQ4
Standby		H	H→X	X	X	X	X	High-Z
READ		L	L	H	L	ROW	COL	Data Out
EARLY-WRITE		L	L	L	X	ROW	COL	Data In
READ-WRITE		L	L	H→L	L→H	ROW	COL	Data Out, Data In
FAST-PAGE-MODE	1st Cycle	L	H→L	H	L	ROW	COL	Data Out
READ	2nd Cycle	L	H→L	H	L	n/a	COL	Data Out
FAST-PAGE-MODE	1st Cycle	L	H→L	L	X	ROW	COL	Data In
EARLY-WRITE	2nd Cycle	L	H→L	L	X	n/a	COL	Data In
FAST-PAGE-MODE	1st Cycle	L	H→L	H→L	L→H	ROW	COL	Data Out, Data In
READ-WRITE	2nd Cycle	L	H→L	H→L	L→H	n/a	COL	Data Out, Data In
RAS-ONLY REFRESH		L	H	X	X	ROW	n/a	High-Z
HIDDEN	READ	L→H→L	L	H	L	ROW	COL	Data Out
REFRESH	WRITE	L→H→L	L	L	X	ROW	COL	Data In
CAS-BEFORE-RAS REFRESH		H→L	L	X	X	X	X	High-Z
BATTERY BACKUP REFRESH		H→L	L	X	X	X	X	High-Z

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} ..... -1V to +6V
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 3, 4, 6, 7) (V_{CC} = 3.3V ± 5%, T_A = 0°C to 70°C)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	3.15	3.45	V	1
Input High (Logic 1) Voltage, All Inputs	V_{IH}	2.4	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, All Inputs	V_{IL}	-1.0	0.8	V	1
INPUT LEAKAGE CURRENT Any Input 0V ≤ V_{IN} ≤ 4.6V (All other pins not under test = 0V)	I_I	-2	2	µA	
OUTPUT LEAKAGE CURRENT: (Q is disabled; 0V ≤ V_{OUT} ≤ V_{CC})	I_{OZ}	-10	10	µA	
OUTPUT LEVELS Output High Voltage (I_{OUT} = -1mA)	V_{OH}	2.0		V	
Output Low Voltage (I_{OUT} = 2.0mA)	V_{OL}		0.4	V	

		MAX			
PARAMETER/CONDITION	SYMBOL	-10	-12	UNITS	NOTES
STANDBY CURRENT: (TTL) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC1}	1	1	mA	
STANDBY CURRENT: (CMOS) ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} -0.2V)	I_{CC2}	60	60	µA	25
OPERATING CURRENT: Random READ/WRITE Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Single Address Cycling: ^tRC = ^tRC (MIN))	I_{CC3}	40	35	mA	3, 4
OPERATING CURRENT: FAST PAGE MODE Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: ^tPC = ^tPC (MIN))	I_{CC4}	30	25	mA	3, 4
REFRESH CURRENT: $\overline{RAS}$-ONLY Average power supply current ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}: ^tRC = ^tRC (MIN))	I_{CC5}	40	35	mA	3
REFRESH CURRENT: $\overline{CAS}$-BEFORE-$\overline{RAS}$ (CBR) Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC (MIN))	I_{CC6}	40	35	mA	3, 5
REFRESH CURRENT: BATTERY BACKUP (BBU) Average power supply current during battery backup refresh: $\overline{CAS}$ = 0.2V or $\overline{CAS}$-BEFORE-$\overline{RAS}$ cycling; $\overline{RAS}$ = ^tRAS (MIN) to 300ns; $\overline{WE}$, A0-A9 and DQ = V_{CC} -0.2V or 0.2V (DQ_{IN} may be left OPEN), ^tRC = 125µs (512 rows at 125µs = 64ms)	I_{CC7}	90	90	µA	3, 5, 7, 27

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A8	C_{I1}		5	pF	2
Input Capacitance: $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$	C_{I2}		7	pF	2
Input/Output Capacitance: DQ	C_{IO}		7	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13, 23) (V_{CC} = 3.3V ±5%, T_A= 0°C to 70°C)

AC CHARACTERISTICS		-10		-12			
PARAMETER	SYM	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	^tRC	180		210		ns	
READ-WRITE cycle time	^tRWC	245		255		ns	
FAST-PAGE-MODE READ or WRITE cycle time	^tPC	55		60		ns	
FAST-PAGE-MODE READ-WRITE cycle time	^tPRWC	115		140		ns	
Access time from $\overline{RAS}$	^tRAC		100		120	ns	14
Access time from $\overline{CAS}$	^tCAC		30		40	ns	15
Output Enable	^tOE		25		30	ns	
Access time from column address	^tAA		50		60	ns	
Access time from $\overline{CAS}$ precharge	^tCPA		50		60	ns	
$\overline{RAS}$ pulse width	^tRAS	100	100,000	120	100,000	ns	
$\overline{RAS}$ pulse width (FAST PAGE MODE)	^tRASP	100	100,000	120	100,000	ns	
$\overline{RAS}$ hold time	^tRSH	25		35		ns	
$\overline{RAS}$ precharge time	^tRP	70		80		ns	
$\overline{CAS}$ pulse width	^tCAS	25	100,000	35	100,000	ns	
$\overline{CAS}$ hold time	^tCSH	100		120		ns	
$\overline{CAS}$ precharge time	^tCPN	10		15		ns	16
$\overline{CAS}$ precharge time (FAST PAGE MODE)	^tCP	10		15		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	^tRCD	25	75	25	90	ns	17
$\overline{CAS}$ to $\overline{RAS}$ precharge time	^tCRP	5		10		ns	
Row address setup time	^tASR	0		0		ns	
Row address hold time	^tRAH	15		15		ns	
$\overline{RAS}$ to column address delay time	^tRAD	20	50	20	60	ns	18
Column address setup time	^tASC	0		0		ns	
Column address hold time	^tCAH	20		25		ns	
Column address hold time (referenced to $\overline{RAS}$)	^tAR	70		85		ns	
Column address to $\overline{RAS}$ lead time	^tRAL	50		60		ns	
Read command setup time	^tRCS	0		0		ns	
Read command hold time (referenced to $\overline{CAS}$)	^tRCH	0		0		ns	19
Read command hold time (referenced to $\overline{RAS}$)	^tRRH	0		0		ns	19
$\overline{CAS}$ to output in Low-Z	^tCLZ	0		0		ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

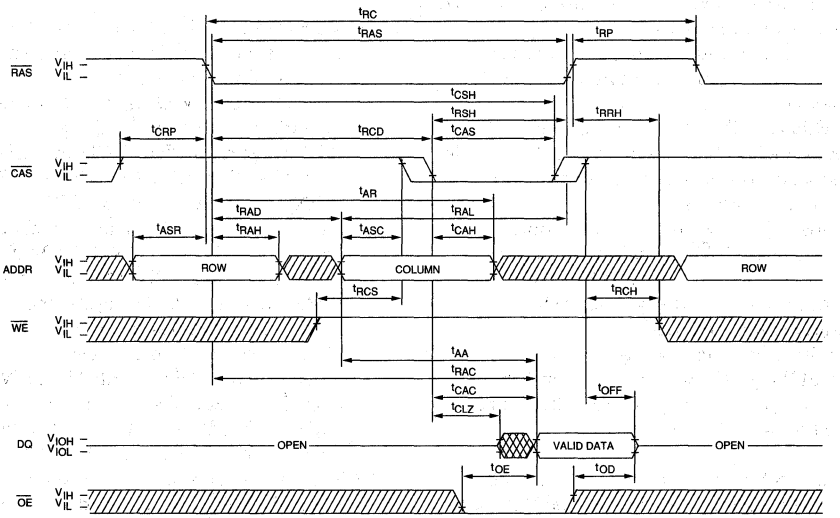
(Notes: 6, 7, 8, 9, 10, 11, 12, 13, 23) (V_{CC} = 3.3V ±5%, T_A= 0°C to 70°C)

AC CHARACTERISTICS		-10		-12			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Output buffer turn-off delay	^tOFF	0	25	0	35	ns	20, 26
Output disable	^tOD		25		35	ns	26
$\overline{WE}$ command setup time	^tWCS	0		0		ns	21
Write command hold time	^tWCH	20		25		ns	
Write command hold time (referenced to $\overline{RAS}$)	^tWCR	75		85		ns	
Write command pulse width	^tWP	20		25		ns	
Write command to $\overline{RAS}$ lead time	^tRWL	25		30		ns	
Write command to $\overline{CAS}$ lead time	^tCWL	25		30		ns	
Data-in setup time	^tDS	0		0		ns	22
Data-in hold time	^tDH	20		25		ns	22
Data-in hold time (referenced to $\overline{RAS}$)	^tDHR	75		90		ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	^tRWD	130		160		ns	21
Column address to $\overline{WE}$ delay time	^tAWD	80		100		ns	21
$\overline{CAS}$ to $\overline{WE}$ delay time	^tCWD	60		75		ns	21
Transition time (rise or fall)	^tT	3	50	3	50	ns	9, 10
Refresh period (512 cycles)	^tREF		64		64	ms	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	^tRPC	0		0		ns	
$\overline{CAS}$ setup time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tCSR	10		10		ns	5
$\overline{CAS}$ hold time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tCHR	20		20		ns	5
$\overline{OE}$ hold time from $\overline{WE}$ during READ-MODIFY-WRITE cycle	^tOEH	20		20		ns	25
$\overline{OE}$ setup prior to $\overline{RAS}$ during HIDDEN REFRESH cycle	^tORD	0		0		ns	24

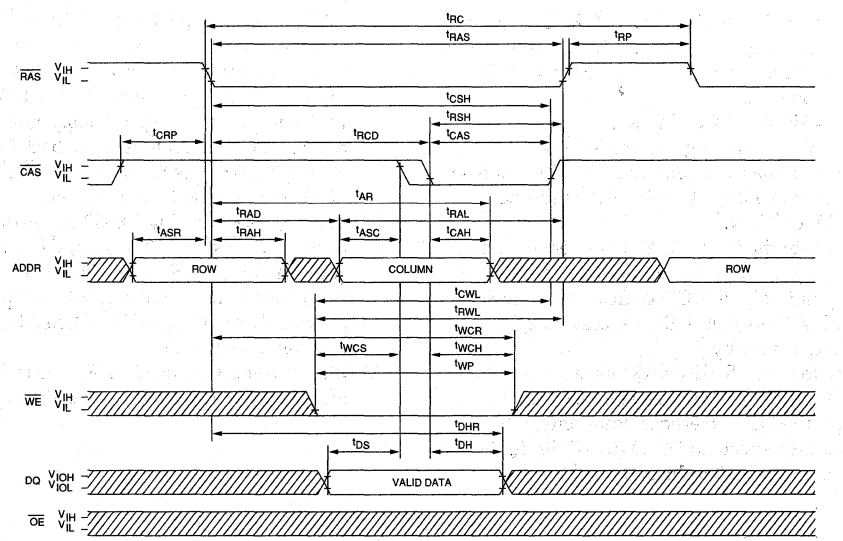
NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. V_{CC} = 5V ±10%, f = 1 MHz.
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is assured.
7. An initial pause of 100µs is required after power-up followed by any eight $\overline{RAS}$ cycles before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-up should be repeated any time the ^{t}REF refresh requirement is exceeded.
8. AC characteristics assume ^{t}T = 5ns.
9. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS}$ = V_{IH}, data output is High-Z.
12. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to 1 TTL gate and 50pF.
14. Assumes that $^{t}RCD < {}^{t}RCD$ (MAX). If ^{t}RCD is greater than the maximum recommended value shown in this table, ^{t}RAC will increase by the amount that ^{t}RCD exceeds the value shown.
15. Assumes that $^{t}RCD \geq {}^{t}RCD$ (MAX).
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer, $\overline{CAS}$ must be pulsed HIGH for ^{t}CPN.
17. Operation within the ^{t}RCD (MAX) limit ensures that ^{t}RAC (MAX) can be met. ^{t}RCD (MAX) is specified as a reference point only; if ^{t}RCD is greater than the specified ^{t}RCD (MAX) limit, then access time is controlled exclusively by ^{t}CAC.
18. Operation within the ^{t}RAD (MAX) limit ensures that ^{t}RAC (MIN) and ^{t}CAC (MIN) can be met. ^{t}RAD (MAX) is specified as a reference point only; if ^{t}RAD is greater than the specified ^{t}RAD (MAX) limit, then access time is controlled exclusively by ^{t}AA.
19. Either ^{t}RCH or ^{t}RRH must be satisfied for a READ cycle.
20. ^{t}OFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
21. ^{t}WCS, ^{t}RWD, ^{t}AWD and ^{t}CWD are not restrictive operating parameters. ^{t}WCS applies to EARLY-WRITE cycles. ^{t}RWD, ^{t}AWD and ^{t}CWD apply to READ-MODIFY-WRITE cycles. If $^{t}WCS \geq {}^{t}WCS$ (MIN), the cycle is an EARLY-WRITE cycle, and the data output will remain an open circuit throughout the entire cycle. If $^{t}RWD \geq {}^{t}RWD$ (MIN), $^{t}AWD \geq {}^{t}AWD$ (MIN) and $^{t}CWD \geq {}^{t}CWD$ (MIN), the cycle is a READ-MODIFY-WRITE cycle, and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of data out is indeterminate. $\overline{OE}$ held HIGH and $\overline{WE}$ taken LOW after $\overline{CAS}$ goes LOW results in a LATE-WRITE ($\overline{OE}$ controlled) cycle. ^{t}WCS, ^{t}RWD, ^{t}CWD and ^{t}AWD are not applicable in a LATE-WRITE cycle.
22. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY-WRITE cycles and $\overline{WE}$ leading edge in LATE-WRITE or READ-MODIFY-WRITE cycles.
23. If $\overline{OE}$ is tied permanently LOW, LATE-WRITE or READ-MODIFY-WRITE operations are not possible.
24. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW and $\overline{OE}$ = HIGH.
25. LATE-WRITE and READ-MODIFY-WRITE cycles must have both ^{t}OD and ^{t}OEH met ($\overline{OE}$ HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. The DQs will provide the previously read data if $\overline{CAS}$ remains LOW and $\overline{OE}$ is taken back LOW after ^{t}OEH is met. If $\overline{CAS}$ goes HIGH prior to $\overline{OE}$ going back LOW, the DQs will remain open.
26. The DQs open during READ cycles once ^{t}OD or ^{t}OFF occur. If $\overline{CAS}$ goes HIGH first, $\overline{OE}$ becomes a "don't care." If $\overline{OE}$ goes HIGH and $\overline{CAS}$ stays LOW, $\overline{OE}$ is not a "don't care," and the DQs will provide the previously read data if $\overline{OE}$ is taken back LOW (while $\overline{CAS}$ remains LOW).
27. BBU current is reduced as ^{t}RAS is reduced from its maximum specification during BBU cycle.

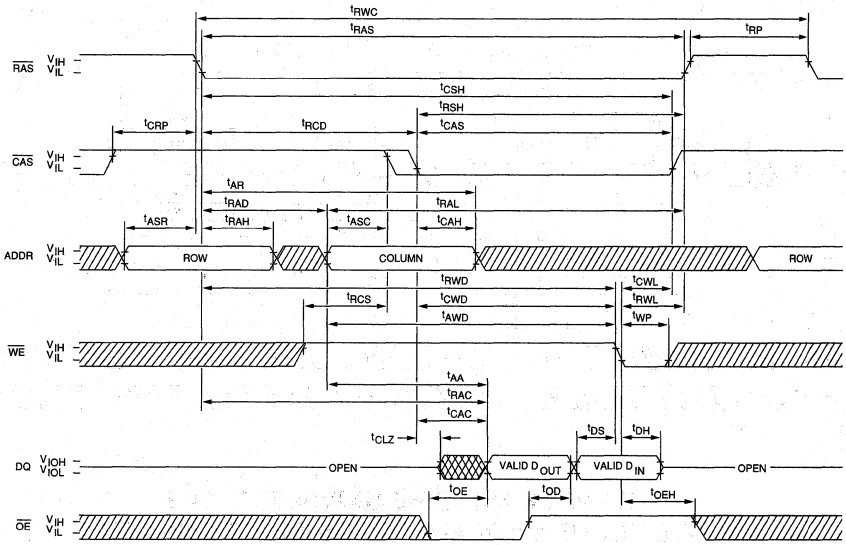
READ CYCLE



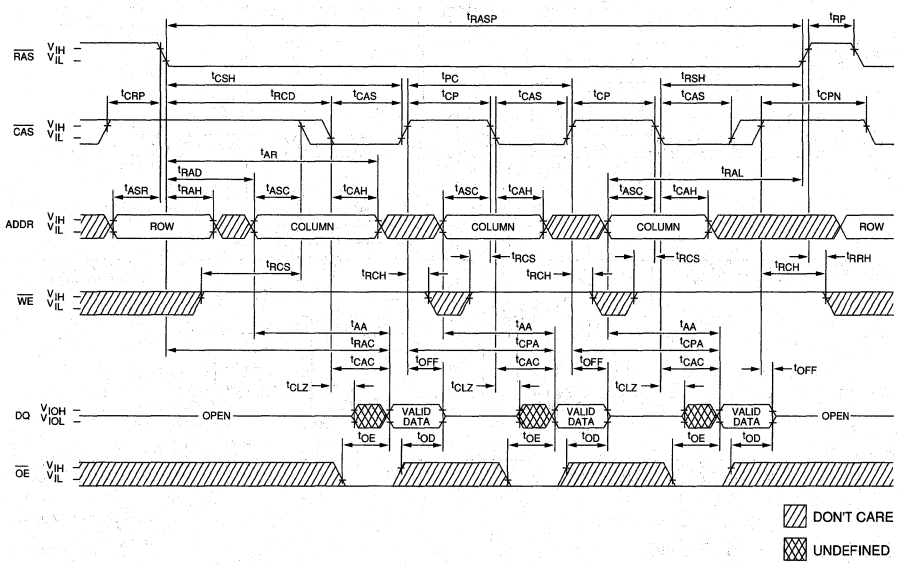
EARLY-WRITE CYCLE



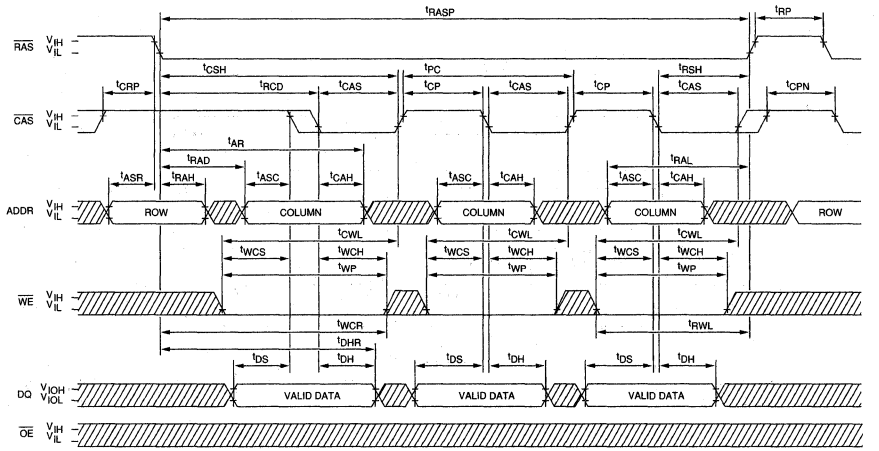
READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)



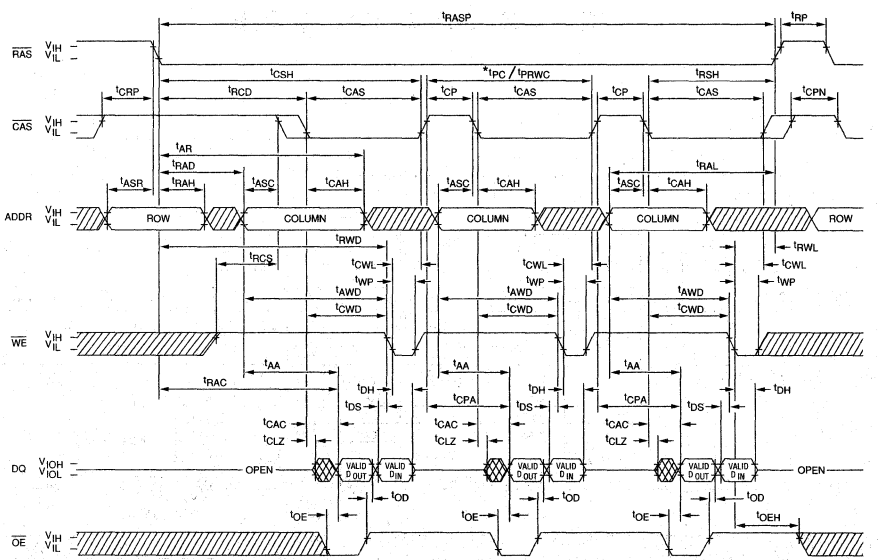
FAST-PAGE-MODE READ CYCLE



FAST-PAGE-MODE EARLY-WRITE CYCLE

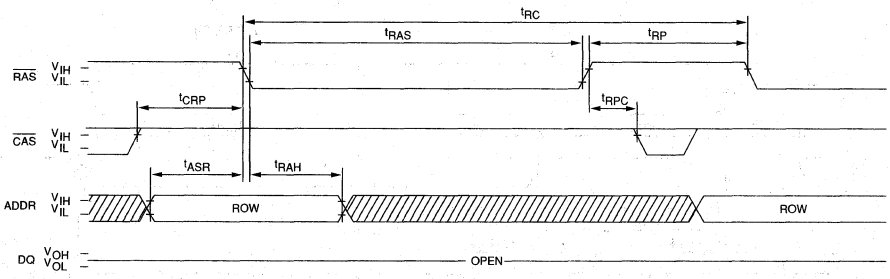


FAST-PAGE-MODE READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)

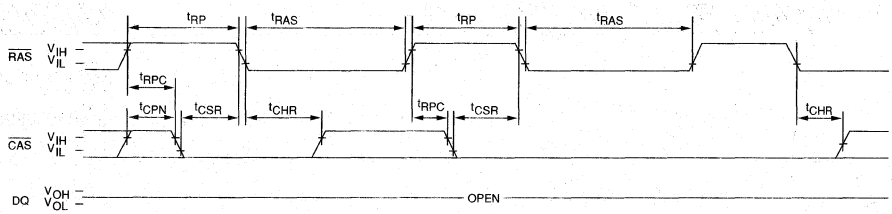


*tPC is for LATE-WRITE only.

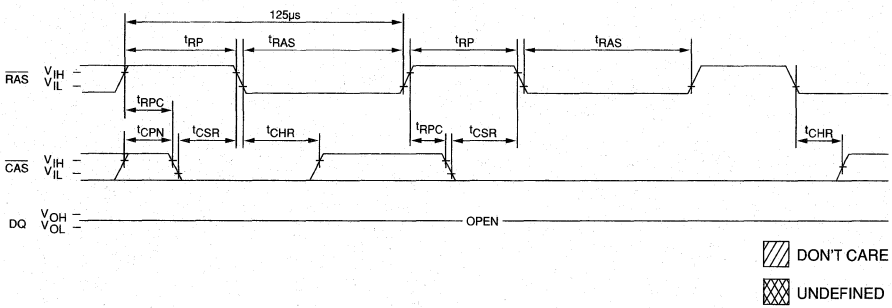
RAS-ONLY REFRESH CYCLE
(ADDR = A0-A8; WE = DON'T CARE)



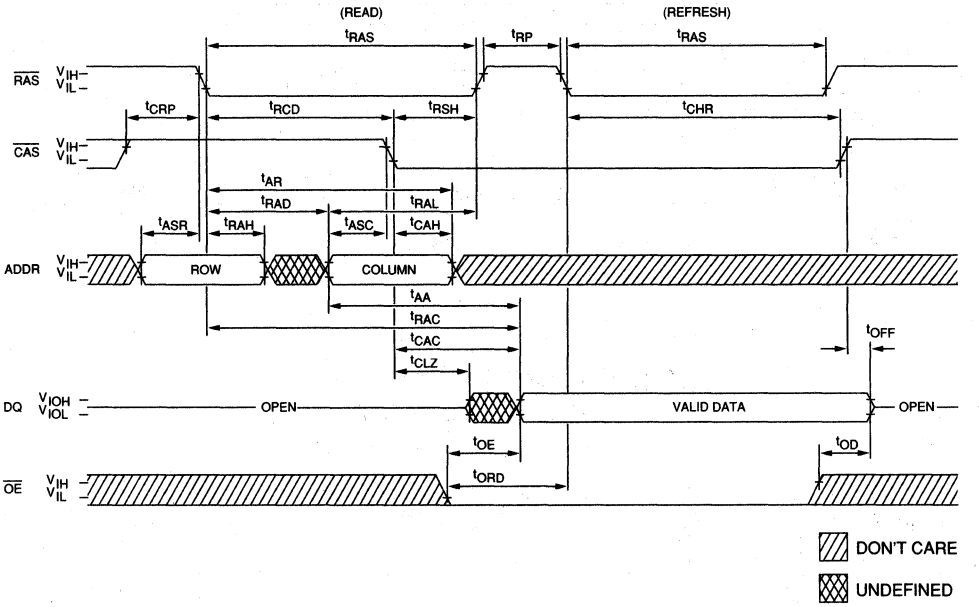
CAS-BEFORE-RAS REFRESH CYCLE
(A0-A8, WE and OE = DON'T CARE)



BATTERY BACKUP REFRESH CYCLE
(A0-A8, WE and OE = DON'T CARE)



HIDDEN REFRESH CYCLE [24]
($\overline{WE}$ = HIGH; $\overline{OE}$ = LOW)



DRAM

256K x 4 DRAM

STATIC COLUMN

FEATURES

- Industry standard x4 pinout, timing, functions and packages
- High-performance, CMOS silicon-gate process
- Single +5V ±10% power supply
- Low power, 3mW standby; 175mW active, typical
- All inputs, outputs and clocks are fully TTL compatible
- 512-cycle refresh in 8ms
- Refresh modes: RAS-ONLY, CAS-BEFORE-RAS (CBR) and HIDDEN
- Optional STATIC COLUMN access cycle

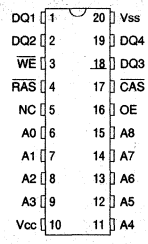
OPTIONS / MARKING

• Timing	
70ns access	- 7
80ns access	- 8
100ns access	-10
• Packages	
Plastic DIP (300 mil)	None
Plastic SOJ (300 mil)	DJ
Plastic ZIP (350 mil)	Z

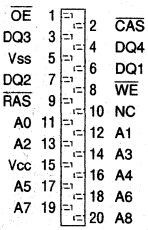
NOTE: Available in die form (commercial or military) or military ceramic packages. Please consult factory for die data sheets or refer to Micron's *Military Data Book*.

PIN ASSIGNMENT (Top View)

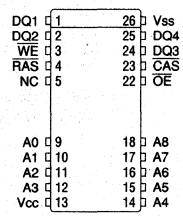
20-Pin DIP (N-2)



20-Pin ZIP (O-1)



20-Pin SOJ (Q-1)



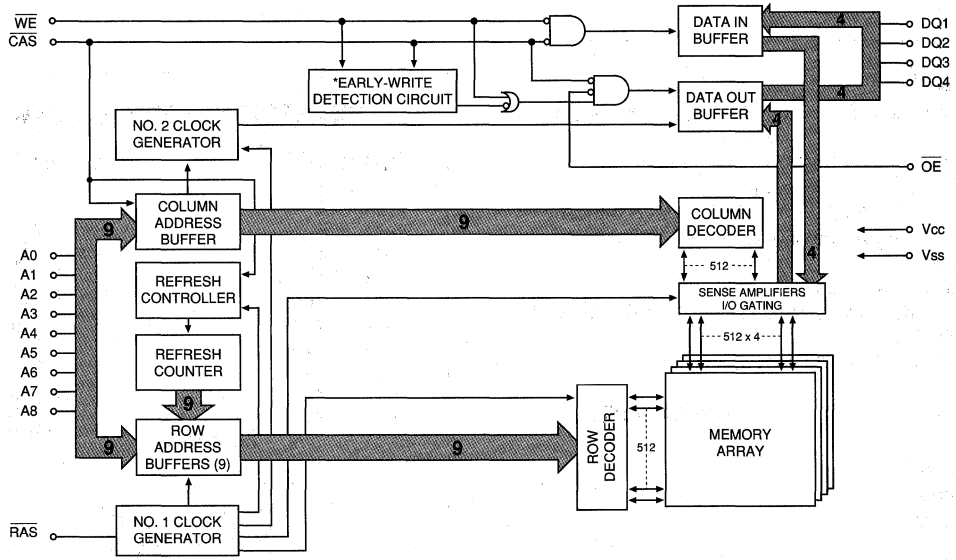
GENERAL DESCRIPTION

The MT4C4258 is a randomly accessed solid-state memory containing 1,048,576 bits organized in a x4 configuration. During READ or WRITE cycles, each bit is uniquely addressed through the 18 address bits, which are entered 9 bits (A0-A8) at a time. RAS is used to latch the first 9 bits and CAS the latter 9 bits. READ and WRITE cycles are selected with the WE input. A logic HIGH on WE dictates READ mode while a logic LOW on WE dictates WRITE mode. During a WRITE cycle, data in (D) is latched by the falling edge of WE or CAS, whichever occurs last. If WE goes LOW prior to CAS going LOW, the output pin(s) remain open (High-Z) until the next CAS cycle. If WE goes LOW after data reaches the output pin(s), data out (Q) is activated and retains the selected cell data as long as CAS remains LOW (regardless of WE or RAS). This late WE pulse results in a READ-WRITE cycle. The four data inputs and four data outputs are routed through four pins using common I/O and pin direction is controlled by WE and OE.

STATIC COLUMN operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row address (A0-A9) defined page boundary. After the first read, any column address transition will result in new data out. Unlike the page-mode part, which requires CAS to be toggled for each successive page-mode access, the STATIC COLUMN part allows CAS to be left LOW for successive STATIC COLUMN accesses. Returning RAS HIGH terminates the STATIC COLUMN operation.

Returning RAS and CAS HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the RAS high time. Memory cell data is retained in its correct state by maintaining power and executing any RAS cycle (READ, WRITE, RAS-ONLY, CAS-BEFORE-RAS (CBR) or HIDDEN refresh) so that all 512 combinations of RAS addresses (A0-A8) are executed at least every 8ms, regardless of sequence. The CBR refresh cycle will invoke the internal refresh counter for automatic RAS addressing.

FUNCTIONAL BLOCK DIAGRAM
STATIC COLUMN



*NOTE: $\overline{WE}$ LOW prior to $\overline{CAS}$ LOW, EW detection circuit output is a HIGH (EARLY-WRITE)
$\overline{CAS}$ LOW prior to $\overline{WE}$ LOW, EW detection circuit output is a LOW (LATE-WRITE)

TRUTH TABLE

FUNCTION		$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	$\overline{OE}$	ADDRESSES t_R	ADDRESSES t_C	DATA IN/OUT DQ1-DQ4
Standby		H	H→X	X	X	X	X	High-Z
READ		L	L	H	L	ROW	COL	Data Out
EARLY-WRITE		L	L	L	X	ROW	COL	Data In
READ-WRITE		L	L	H→L	L→H	ROW	COL	Data Out, Data In
STATIC COLUMN	1st Cycle	L	L	H	L	ROW	COL	Data Out
READ	2nd Cycle	L	L	H	L	n/a	COL	Data Out
STATIC COLUMN	1st Cycle	L	L	L	X	ROW	COL	Data In
EARLY-WRITE	2nd Cycle	L	L	H→L	X	n/a	COL	Data In
STATIC COLUMN	1st Cycle	L	L	H→L	L→H	ROW	COL	Data Out, Data In
READ-WRITE	2nd Cycle	L	L	H→L	L→H	n/a	COL	Data Out, Data In
$\overline{RAS}$-ONLY REFRESH		L	H	X	X	ROW	n/a	High-Z
HIDDEN	READ	L→H→L	L	H	L	ROW	COL	Data Out
REFRESH	WRITE	L→H→L	L	L	X	ROW	COL	Data In
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH		H→L	L	X	X	X	X	High-Z

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to V_{SS} ..... -1V to +7V
Operating Temperature, T_A (Ambient) ..... 0°C to +70°C
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 3, 4, 6, 7) (V_{CC} = 5V ±10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.5	V	1
Input High (Logic 1) Voltage, All Inputs	V_{IH}	2.4	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, All Inputs	V_{IL}	-1.0	0.8	V	1
INPUT LEAKAGE CURRENT Any Input 0V ≤ V_{IN} ≤ 6.5V (All other pins not under test = 0V)	I_I	-2	2	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled; 0V ≤ V_{OUT} ≤ 5.5V)	I_{OZ}	-10	10	µA	
OUTPUT LEVELS Output High Voltage (I_{OUT} = -5mA)	V_{OH}	2.4		V	
Output Low Voltage (I_{OUT} = 4.2mA)	V_{OL}		0.4	V	

		MAX				
PARAMETER/CONDITION	SYMBOL	-7	-8	-10	UNITS	NOTES
STANDBY CURRENT: (TTL) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC1}	2	2	2	mA	
STANDBY CURRENT: (CMOS) ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} -0.2V)	I_{CC2}	1	1	1	mA	
OPERATING CURRENT: Random READ/WRITE Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC (MIN))	I_{CC3}	80	70	60	mA	3, 4
OPERATING CURRENT: STATIC COLUMN Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: ^tSC = ^tSC (MIN))	I_{CC4}	60	50	40	mA	3, 4
REFRESH CURRENT: $\overline{RAS}$-ONLY Average power supply current ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}: ^tRC = ^tRC (MIN))	I_{CC5}	80	70	60	mA	3
REFRESH CURRENT: $\overline{CAS}$-BEFORE-$\overline{RAS}$ Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC (MIN))	I_{CC6}	80	70	60	mA	3, 5

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A8	C_{I1}		5	pF	2
Input Capacitance: $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$	C_{I2}		7	pF	2
Input/Output Capacitance: DQ	C_{IO}		7	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13, 23) (V_{CC} = 5V ±10%)

AC CHARACTERISTICS		-7		-8		-10			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	t_{RC}	130		150		180		ns	
READ-WRITE cycle time	t_{RWC}	185		205		245		ns	
STATIC-COLUMN READ or WRITE cycle time	t_{SC}	40		45		55		ns	
STATIC-COLUMN READ-WRITE cycle time	t_{SRWC}	100		110		135		ns	
Access time from $\overline{RAS}$	t_{RAC}		70		80		100	ns	14
Access time from $\overline{CAS}$	t_{CAC}		20		20		25	ns	15
Output Enable	t_{OE}		20		20		25	ns	
Access time from column address	t_{AA}		35		40		50	ns	
$\overline{RAS}$ pulse width	t_{RAS}	70	100,000	80	100,000	100	100,000	ns	
$\overline{RAS}$ pulse width (STATIC COLUMN)	t_{RASC}	70	100,000	80	100,000	100	100,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	20		20		25		ns	
$\overline{RAS}$ precharge time	t_{RP}	50		60		70		ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	100,000	20	100,000	25	100,000	ns	
$\overline{CAS}$ hold time	t_{CSH}	70		80		100		ns	
$\overline{CAS}$ precharge time	t_{CPN}	10		10		15		ns	16
$\overline{CAS}$ precharge time (STATIC COLUMN)	t_{CP}	10		10		10		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	50	20	60	25	75	ns	17
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		5		ns	
Row address setup time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	10		10		15		ns	
$\overline{RAS}$ to column address delay time	t_{RAD}	15	35	15	40	20	50	ns	18
Column address setup time	t_{ASC}	0		0		0		ns	
Column address hold time	t_{CAH}	15		15		20		ns	
Column address hold time (referenced to $\overline{RAS}$)	t_{AR}	80		90		100		ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	35		40		50		ns	
Read command setup time	t_{RCS}	0		0		0		ns	
Read command hold time (referenced to $\overline{CAS}$)	t_{RCH}	0		0		0		ns	19
Read command hold time (referenced to $\overline{RAS}$)	t_{RRH}	0		0		0		ns	19
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	0		0		0		ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

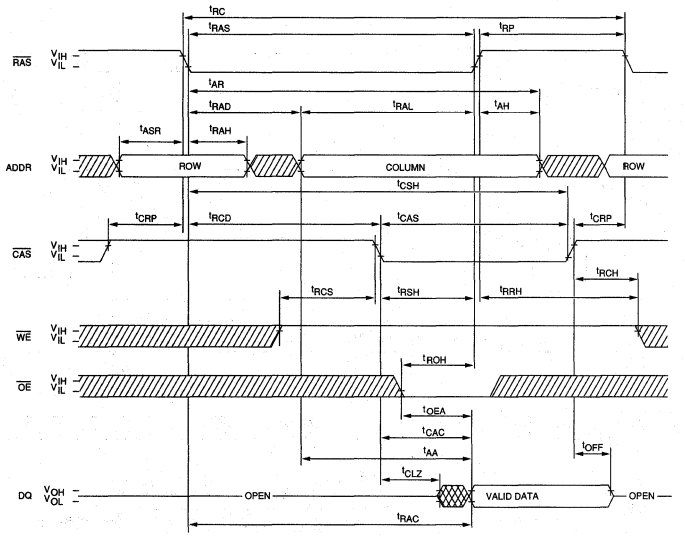
(Notes: 6, 7, 8, 9, 10, 11, 12, 13, 23) (V_{CC} = 5V ±10%)

AC CHARACTERISTICS		-7		-8		-10			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Output buffer turn-off delay	^tOFF	0	20	0	20	0	20	ns	20, 26
Output disable	^tOD		20		20		20	ns	26
Column address hold time EARLY-WRITE (referenced to $\overline{RAS}$)	^tAWR		55		60		70	ns	
$\overline{WE}$ command setup time	^tWCS	0		0		0		ns	21
Write command hold time	^tWCH	15		15		20		ns	
Write command hold time (referenced to $\overline{RAS}$)	^tWCR	55		60		75		ns	
Write command pulse width	^tWP	15		15		20		ns	
Write command to $\overline{RAS}$ lead time	^tRWL	20		20		25		ns	
Write command to $\overline{CAS}$ lead time	^tCWL	20		20		25		ns	
Data-in setup time	^tDS	0		0		0		ns	22
Data-in hold time	^tDH	15		15		20		ns	22
Data-in hold time (referenced to $\overline{RAS}$)	^tDHR	55		60		75		ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	^tRWD	100		110		130		ns	21
Column address to $\overline{WE}$ delay time	^tAWD	65		70		80		ns	21
$\overline{CAS}$ to $\overline{WE}$ delay time	^tCWD	50		55		60		ns	21
Transition time (rise or fall)	^tT	3	50	3	50	3	50	ns	9, 10
Refresh period (512 cycles)	^tREF		8		8		8	ms	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	^tRPC	0		0		0		ns	
$\overline{CAS}$ setup time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tCSR	10		10		10		ns	5
$\overline{CAS}$ hold time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tCHR	15		15		15		ns	5
$\overline{OE}$ hold time from $\overline{WE}$ during READ-MODIFY-WRITE cycle	^tOEH	20		20		20		ns	25
$\overline{OE}$ setup prior to $\overline{RAS}$ during HIDDEN REFRESH cycle	^tORD	0		0		0		ns	24
Write inactive time	^tWI	10		10		10		ns	
Previous WRITE to column address delay time	^tLWAD	20	30	20	35	25	45	ns	
Previous WRITE to column address hold time	^tAHLW	65		75		95		ns	
$\overline{RAS}$ hold time referenced to $\overline{OE}$	^tROH	10		10		10		ns	
Output data hold time from column address	^tAOH	5		5		5		ns	
Output data enable from WRITE	^tOW	^tAA + 5		^tAA + 5		^tAA + 5		ns	
Access time from last WRITE	^tALW	65		75		95		ns	
Column address hold time referenced to $\overline{RAS}$ HIGH	^tAH	5		5		10		ns	
CAS pulse width in STATIC-COLUMN mode	^tCSC	^tCAS		^tCAS		^tCAS		ns	

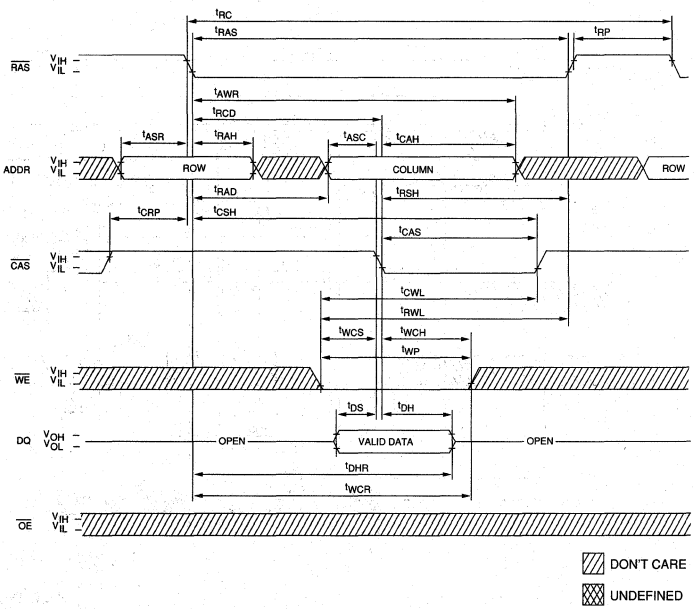
NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. V_{CC} = 5V ±10%, f = 1 MHz.
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is assured.
7. An initial pause of 100µs is required after power-up followed by any eight $\overline{RAS}$ cycles before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-up should be repeated any time the ^{t}REF refresh requirement is exceeded.
8. AC characteristics assume ^{t}T = 5ns.
9. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS}$ = V_{IH}, data output is High-Z.
12. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to 2 TTL gates and 100pF.
14. Assumes that $^{t}RCD < {}^{t}RCD$ (MAX). If ^{t}RCD is greater than the maximum recommended value shown in this table, ^{t}RAC will increase by the amount that ^{t}RCD exceeds the value shown.
15. Assumes that $^{t}RCD \geq {}^{t}RCD$ (MAX).
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer, $\overline{CAS}$ must be pulsed HIGH for ^{t}CPN.
17. Operation within the ^{t}RCD (MAX) limit ensures that ^{t}RAC (MAX) can be met. ^{t}RCD (max) is specified as a reference point only; if ^{t}RCD is greater than the specified ^{t}RCD (MAX) limit, then access time is controlled exclusively by ^{t}CAC.
18. Operation within the ^{t}RAD (MAX) limit ensures that ^{t}RAC (MIN) and ^{t}CAC (MIN) can be met. ^{t}RAD (MAX) is specified as a reference point only; if ^{t}RAD is greater than the specified ^{t}RAD (MAX) limit, then access time is controlled exclusively by ^{t}AA.
19. Either ^{t}RCH or ^{t}RRH must be satisfied for a READ cycle.
20. ^{t}OFF (MAX) defines the time at which the output achieves the open circuit condition, and is not referenced to V_{OH} or V_{OL}.
21. ^{t}WCS, ^{t}RWD, ^{t}AWD and ^{t}CWD are not restrictive operating parameters. ^{t}WCS applies to EARLY-WRITE cycles. ^{t}RWD, ^{t}AWD and ^{t}CWD apply to READ-MODIFY-WRITE cycles. If $^{t}WCS \geq {}^{t}WCS$ (MIN), the cycle is an EARLY-WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If $^{t}RWD \geq {}^{t}RWD$ (MIN), $^{t}AWD \geq {}^{t}AWD$ (MIN) and $^{t}CWD \geq {}^{t}CWD$ (MIN), the cycle is a READ-MODIFY-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of data out are indeterminate. $\overline{OE}$ held HIGH and $\overline{WE}$ taken LOW after $\overline{CAS}$ goes LOW results in a LATE-WRITE ($\overline{OE}$ controlled) cycle. ^{t}WCS, ^{t}RWD, ^{t}CWD and ^{t}AWD are not applicable in a LATE-WRITE cycle.
22. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY-WRITE cycles and $\overline{WE}$ leading edge in LATE-WRITE or READ-MODIFY-WRITE cycles.
23. If $\overline{OE}$ is tied permanently LOW, LATE-WRITE or READ-MODIFY-WRITE operations are not possible.
24. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW and $\overline{OE}$ = HIGH.
25. LATE-WRITE and READ-MODIFY-WRITE cycles must have both ^{t}OD and ^{t}OEH met ($\overline{OE}$ HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. The DQs will provide the previously read data if $\overline{CAS}$ remains LOW and $\overline{OE}$ is taken back LOW after ^{t}OEH is met. If $\overline{CAS}$ goes HIGH prior to $\overline{OE}$ going back LOW, the DQs will remain open.
26. The DQs open during READ cycles once ^{t}OD or ^{t}OFF occur. If $\overline{CAS}$ goes HIGH first, $\overline{OE}$ becomes a don't care. If $\overline{OE}$ goes HIGH and $\overline{CAS}$ stays LOW, $\overline{OE}$ is not a don't care; and the DQs will provide the previously read data if $\overline{OE}$ is taken back LOW (while $\overline{CAS}$ remains LOW).

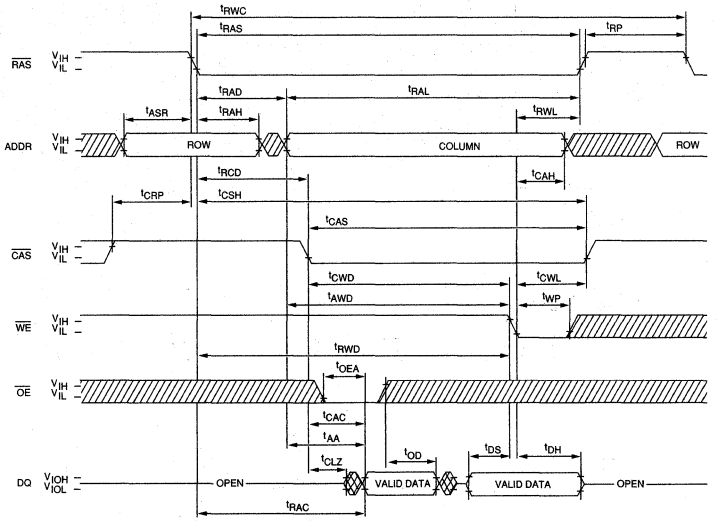
READ CYCLE



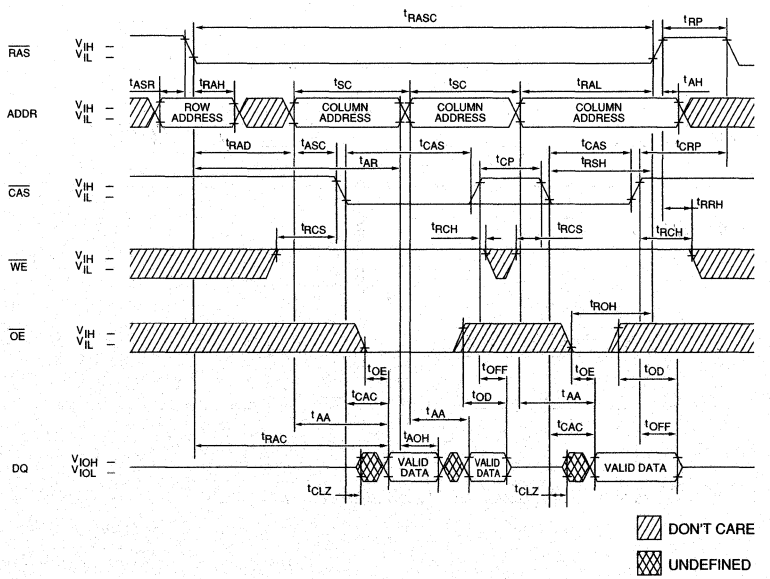
EARLY-WRITE CYCLE



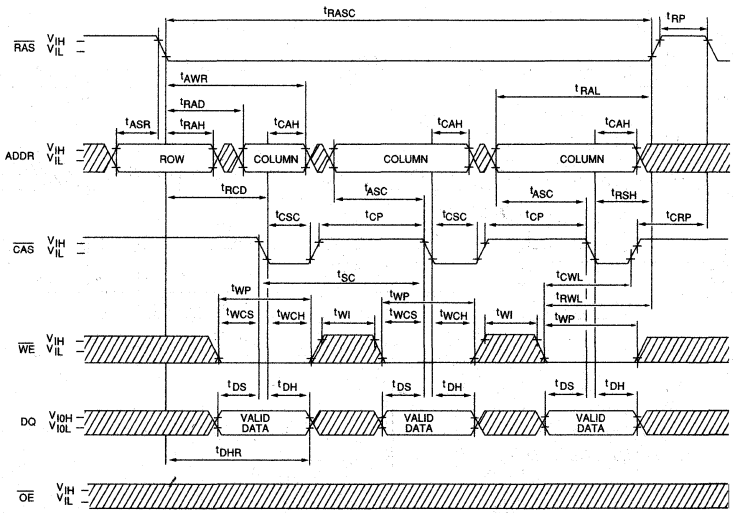
READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)



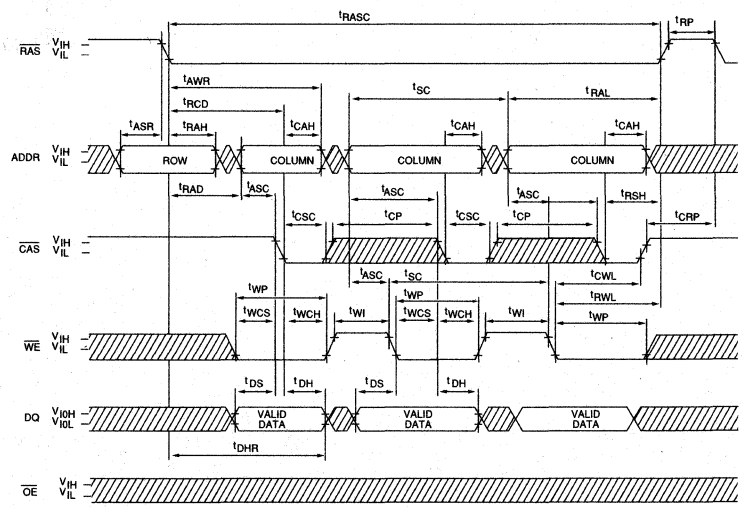
STATIC-COLUMN READ CYCLE



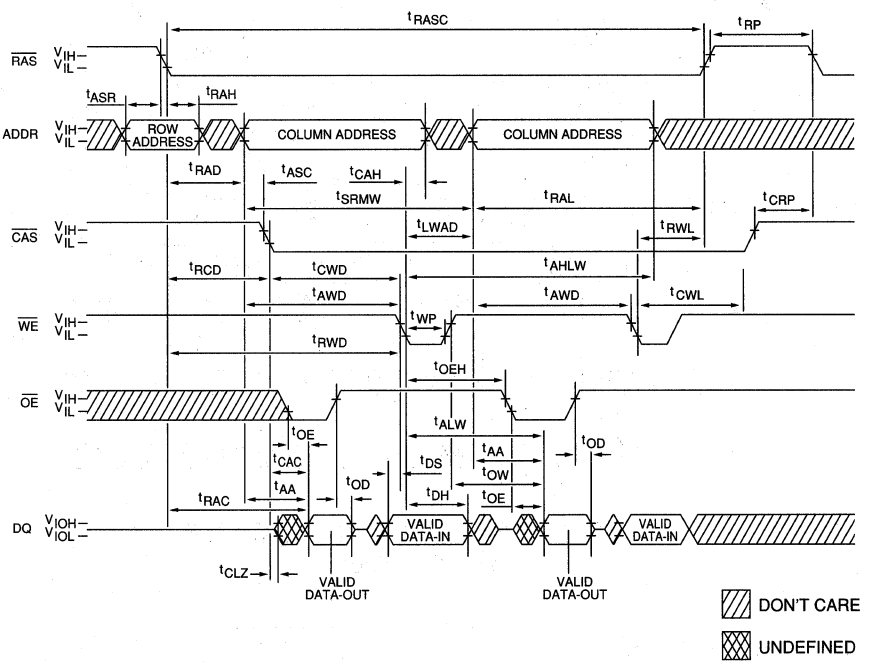
STATIC-COLUMN EARLY-WRITE CYCLE
(CAS controlled)



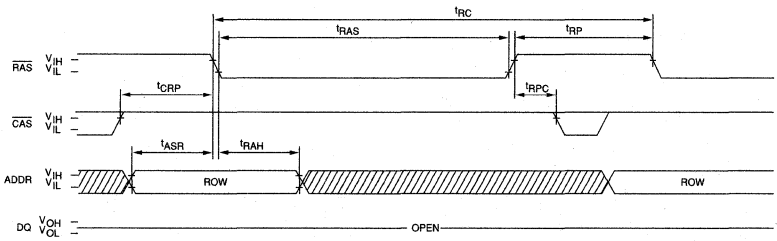
STATIC-COLUMN EARLY-WRITE CYCLE
(WE controlled)



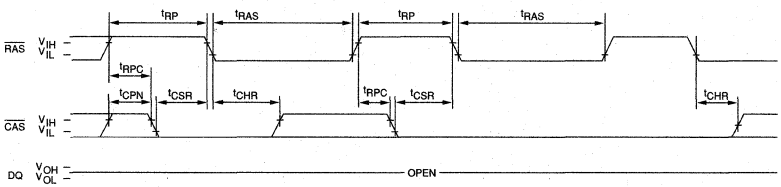
STATIC-COLUMN READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)



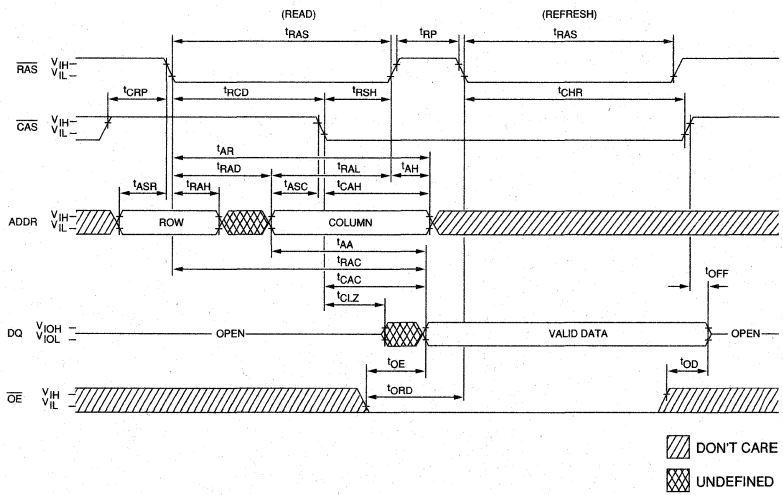
RAS-ONLY REFRESH CYCLE
(ADDR = A0-A8; WE = DON'T CARE)



CAS-BEFORE-RAS REFRESH CYCLE
(A0-A8, WE and OE = DON'T CARE)



HIDDEN REFRESH CYCLE[24]
(WE = HIGH; OE = LOW)



DRAM

1 MEG x 4 DRAM

FAST PAGE MODE

FEATURES

- Industry standard x4 pinout, timing, functions and packages
- High-performance, CMOS silicon-gate process
- Single +5V ±10% power supply
- Low power, 3mW standby; 225mW active, typical
- All inputs, outputs and clocks are fully TTL compatible
- 1,024-cycle refresh distributed across 16ms
- Refresh modes: $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$ (CBR) and HIDDEN
- FAST PAGE MODE access cycle

OPTIONS MARKING

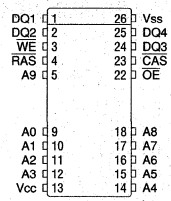
- Timing
  - 60ns access -6
  - 70ns access -7
  - 80ns access -8
- Packages
  - Plastic SOJ (300 mil) DJ
  - Plastic TSOP (300 mil)* TG
  - Plastic ZIP (350 mil) Z

NOTE: Available in die form (commercial or military) or military ceramic packages. Please consult factory for die data sheets or refer to Micron's ***Military Data Book.***

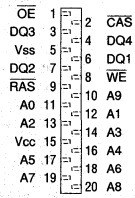
- Operating Temperature, T_A
  - Commercial (0°C to +70°C) None
  - Industrial (-40°C to +85°C) IT
- Part Number Example: MT4C4001JDJ-6

PIN ASSIGNMENT (Top View)

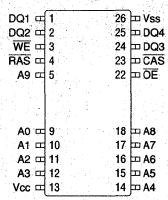
20-Pin SOJ (N-2)



20-Pin ZIP (O-1)



20-Pin TSOP (R-1)



*Consult factory on availability of reverse pinout TSOP packages

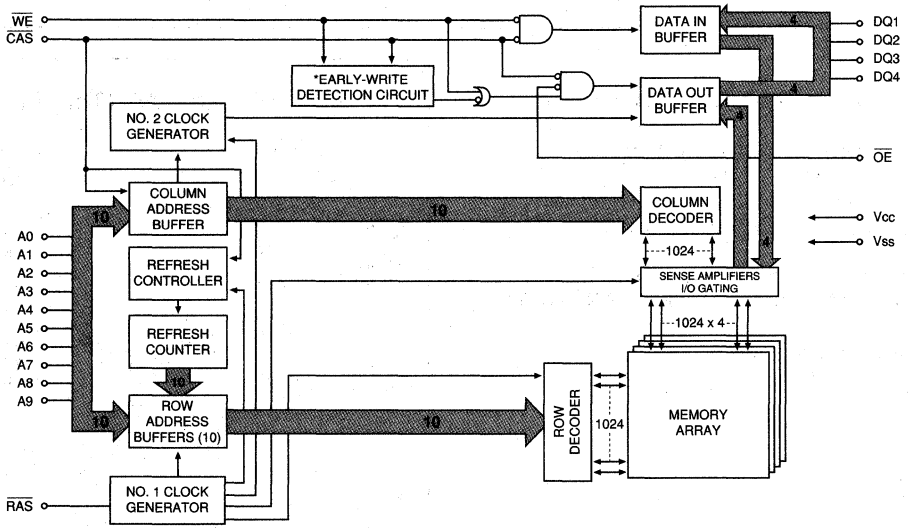
GENERAL DESCRIPTION

The MT4C4001J is a randomly accessed solid-state memory containing 4,194,304 bits organized in a x4 configuration. During READ or WRITE cycles, each bit is uniquely addressed through the 20 address bits, which are entered 10 bits (A0-A9) at a time. $\overline{RAS}$ is used to latch the first 10 bits and $\overline{CAS}$ the latter 10 bits. READ and WRITE cycles are selected with the $\overline{WE}$ input. A logic HIGH on $\overline{WE}$ dictates READ mode while a logic LOW on $\overline{WE}$ dictates WRITE mode. During a WRITE cycle, data in (D) is latched by the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. If $\overline{WE}$ goes LOW prior to $\overline{CAS}$ going LOW, the output pin(s) remain open (High-Z) until the next $\overline{CAS}$ cycle. If $\overline{WE}$ goes LOW after data reaches the output pin(s), The Qs are activated and retain the selected cell data as long as $\overline{CAS}$ remains low (regardless of $\overline{WE}$ or $\overline{RAS}$). This late $\overline{WE}$ pulse results in a READ-WRITE cycle. The four data inputs and four data outputs are routed through four pins using common I/O, and pin direction is controlled by $\overline{WE}$ and $\overline{OE}$.

FAST PAGE MODE operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row address (A0-A9) defined page boundary. The FAST PAGE MODE cycle is always initiated with a row address strobed-in by $\overline{RAS}$ followed by a column address strobed-in by $\overline{CAS}$. $\overline{CAS}$ may be toggled-in by holding $\overline{RAS}$ LOW and strobing-in different column addresses, thus executing faster memory cycles. Returning $\overline{RAS}$ HIGH terminates the FAST PAGE MODE operation.

Returning $\overline{RAS}$ and $\overline{CAS}$ HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the $\overline{RAS}$ high time. Memory cell data is retained in its correct state by maintaining power and executing any $\overline{RAS}$ cycle (READ, WRITE, $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$ (CBR) or HIDDEN refresh) so that all 1,024 combinations of $\overline{RAS}$ addresses (A0-A9) are executed at least every 16ms, regardless of sequence. The CBR refresh cycle will invoke the internal refresh counter for automatic $\overline{RAS}$ addressing.

FUNCTIONAL BLOCK DIAGRAM
FAST PAGE MODE



*NOTE: $\overline{WE}$ LOW prior to $\overline{CAS}$ LOW, EW detection circuit output is a HIGH (EARLY-WRITE)
$\overline{CAS}$ LOW prior to $\overline{WE}$ LOW, EW detection circuit output is a LOW (LATE-WRITE)

TRUTH TABLE

FUNCTION		$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	$\overline{OE}$	ADDRESSES t_R	ADDRESSES t_C	DATA IN/OUT DQ1-DQ4
Standby		H	H→X	X	X	X	X	High-Z
READ		L	L	H	L	ROW	COL	Data Out
EARLY-WRITE		L	L	L	X	ROW	COL	Data In
READ-WRITE		L	L	H→L	L→H	ROW	COL	Data Out, Data In
FAST-PAGE-MODE READ	1st Cycle	L	H→L	H	L	ROW	COL	Data Out
	2nd Cycle	L	H→L	H	L	n/a	COL	Data Out
FAST-PAGE-MODE EARLY-WRITE	1st Cycle	L	H→L	L	X	ROW	COL	Data In
	2nd Cycle	L	H→L	L	X	n/a	COL	Data In
FAST-PAGE-MODE READ-WRITE	1st Cycle	L	H→L	H→L	L→H	ROW	COL	Data Out, Data In
	2nd Cycle	L	H→L	H→L	L→H	n/a	COL	Data Out, Data In
$\overline{RAS}$-ONLY REFRESH		L	H	X	X	ROW	n/a	High-Z
HIDDEN REFRESH	READ	L→H→L	L	H	L	ROW	COL	Data Out
	WRITE	L→H→L	L	L	X	ROW	COL	Data In
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH		H→L	L	H	X	X	X	High-Z

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to V_{SS} ..... -1V to +7V
Operating Temperature, T_A (Ambient) ..... 0°C to +70°C
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 3, 4, 6, 7) (V_{CC} = 5V ±10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.5	V	1
Input High (Logic 1) Voltage, All Inputs	V_{IH}	2.4	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, All Inputs	V_{IL}	-1.0	0.8	V	1
INPUT LEAKAGE CURRENT Any Input 0V ≤ V_{IN} ≤ 6.5V (All other pins not under test = 0V)	I_I	-2	2	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled, 0V ≤ V_{OUT} ≤ 5.5V)	I_{OZ}	-10	10	µA	
OUTPUT LEVELS Output High Voltage (I_{OUT} = -5mA)	V_{OH}	2.4		V	
Output Low Voltage (I_{OUT} = 4.2mA)	V_{OL}		0.4	V	

		MAX				
PARAMETER/CONDITION	SYMBOL	-6	-7	-8	UNITS	NOTES
STANDBY CURRENT: (TTL) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC1}	2	2	2	mA	
STANDBY CURRENT: (CMOS) ($\overline{RAS}$ = $\overline{CAS}$ = Other Inputs = V_{CC} -0.2V)	I_{CC2}	1	1	1	mA	
OPERATING CURRENT: Random READ/WRITE Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC (MIN))	I_{CC3}	110	100	90	mA	3, 4
OPERATING CURRENT: FAST PAGE MODE Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: ^tPC = ^tPC (MIN))	I_{CC4}	80	70	60	mA	3, 4
REFRESH CURRENT: $\overline{RAS}$-ONLY Average power supply current ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}: ^tRC = ^tRC (MIN))	I_{CC5}	110	100	90	mA	3
REFRESH CURRENT: $\overline{CAS}$-BEFORE-$\overline{RAS}$ Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC (MIN))	I_{CC6}	110	100	90	mA	3, 5

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A9	C_{I1}		5	pF	2
Input Capacitance: $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$	C_{I2}		7	pF	2
Input/Output Capacitance: DQ	C_{IO}		7	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13, 23) (V_{CC} = 5V ±10%)

AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	t_{RC}	110		130		150		ns	
READ-WRITE cycle time	t_{RWC}	145		185		205		ns	
FAST-PAGE-MODE READ or WRITE cycle time	t_{PC}	40		40		45		ns	
FAST-PAGE-MODE READ-WRITE cycle time	t_{PRWC}	90		95		100		ns	
Access time from $\overline{RAS}$	t_{RAC}		60		70		80	ns	14
Access time from $\overline{CAS}$	t_{CAC}		15		20		20	ns	15
Output Enable	t_{OE}		15		20		20	ns	23
Access time from column address	t_{AA}		30		35		40	ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		35		40		45	ns	
$\overline{RAS}$ pulse width	t_{RAS}	60	100,000	70	100,000	80	100,000	ns	
$\overline{RAS}$ pulse width (FAST PAGE MODE)	t_{RASP}	60	100,000	70	100,000	80	100,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	15		20		20		ns	
$\overline{RAS}$ precharge time	t_{RP}	40		50		60		ns	
$\overline{CAS}$ pulse width	t_{CAS}	15	100,000	20	100,000	20	100,000	ns	
$\overline{CAS}$ hold time	t_{CSH}	60		70		80		ns	
$\overline{CAS}$ precharge time	t_{CPN}	10		10		10		ns	16
$\overline{CAS}$ precharge time (FAST PAGE MODE)	t_{CP}	10		10		10		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	45	20	50	20	60	ns	17
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		10		10		ns	
Row address setup time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	10		10		10		ns	
$\overline{RAS}$ to column address delay time	t_{RAD}	15	30	15	35	15	40	ns	18
Column address setup time	t_{ASC}	0		0		0		ns	
Column address hold time	t_{CAH}	10		15		15		ns	
Column address hold time (referenced to $\overline{RAS}$)	t_{AR}	50		55		60		ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	30		35		40		ns	
Read command setup time	t_{RCS}	0		0		0		ns	
Read command hold time (referenced to $\overline{CAS}$)	t_{RCH}	0		0		0		ns	19
Read command hold time (referenced to $\overline{RAS}$)	t_{RRH}	0		0		0		ns	19
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	0		0		0		ns	
Output buffer turn-off delay	t_{OFF}	0	15	0	20	0	20	ns	20

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

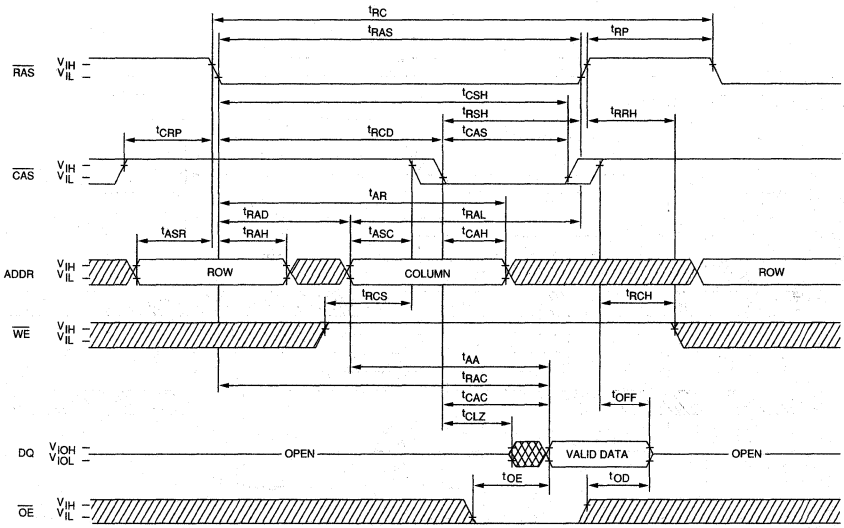
(Notes: 6, 7, 8, 9, 10, 11, 12, 13, 23) (V_{CC} = 5V ±10%)

AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
$\overline{WE}$ command setup time	^tWCS	0		0		0		ns	21, 27
Write command hold time	^tWCH	10		15		15		ns	
Write command hold time (referenced to $\overline{RAS}$)	^tWCR	45		55		60		ns	
Write command pulse width	^tWP	10		15		15		ns	
Write command to $\overline{RAS}$ lead time	^tRWL	15		20		20		ns	
Write command to $\overline{CAS}$ lead time	^tCWL	15		20		20		ns	
Data-in setup time	^tDS	0		0		0		ns	22
Data-in hold time	^tDH	10		15		15		ns	22
Data-in hold time (referenced to $\overline{RAS}$)	^tDHR	45		55		60		ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	^tRWD	85		100		110		ns	21
Column address to $\overline{WE}$ delay time	^tAWD	60		65		70		ns	21
$\overline{CAS}$ to $\overline{WE}$ delay time	^tCWD	45		50		50		ns	21
Transition time (rise or fall)	^tT	3	50	3	50	3	50	ns	9, 10
Refresh period (1,024 cycles)	^tREF		16		16		16	ms	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	^tRPC	0		0		0		ns	
$\overline{CAS}$ setup time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tCSR	10		10		10		ns	5
$\overline{CAS}$ hold time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tCHR	15		15		15		ns	5
$\overline{WE}$ hold time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tWRH	10		10		10		ns	25, 28
$\overline{WE}$ setup time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tWRP	10		10		10		ns	25, 28
$\overline{WE}$ hold time (WCBR test cycle)	^tWTH	10		10		10		ns	25, 28
$\overline{WE}$ setup time (WCBR test cycle)	^tWTS	10		10		10		ns	25, 28
$\overline{OE}$ setup prior to RAS during HIDDEN REFRESH cycle	^tORD	0		0		0		ns	
Output disable	^tOD		15		20		20	ns	27
$\overline{OE}$ hold time from $\overline{WE}$ during READ-MODIFY-WRITE cycle	^tOEH	15		20		20		ns	26

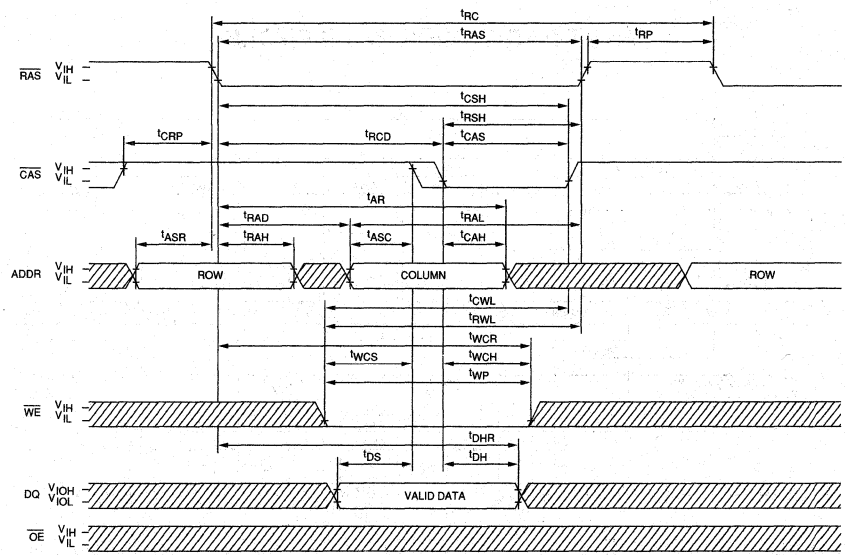
NOTES

1. All voltages referenced to Vss.
2. This parameter is sampled. Vcc = 5V ±10%, f = 1 MHz.
3. Icc is dependent on cycle rates.
4. Icc is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is assured.
7. An initial pause of 100µs is required after power-up followed by eight $\overline{RAS}$ refresh cycles ($\overline{RAS}$-ONLY or CBR with $\overline{WE}$ HIGH) before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-up should be repeated any time the ^{t}REF refresh requirement is exceeded.
8. AC characteristics assume ^{t}T = 5ns.
9. VIH (MIN) and VIL (MAX) are reference levels for measuring timing of input signals. Transition times are measured between VIH and VIL (or between VIL and VIH).
10. In addition to meeting the transition rate specification, all input signals must transit between VIH and VIL (or between VIL and VIH) in a monotonic manner.
11. If $\overline{CAS}$ = VIH, data output is High-Z.
12. If $\overline{CAS}$ = VIL, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to 2 TTL gates and 100pF.
14. Assumes that ^{t}RCD < ^{t}RCD (MAX). If ^{t}RCD is greater than the maximum recommended value shown in this table, ^{t}RAC will increase by the amount that ^{t}RCD exceeds the value shown.
15. Assumes that ^{t}RCD ≥ ^{t}RCD (MAX).
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer, $\overline{CAS}$ must be pulsed HIGH for ^{t}CPN.
17. Operation within the ^{t}RCD (MAX) limit ensures that ^{t}RAC (MAX) can be met. ^{t}RCD (MAX) is specified as a reference point only; if ^{t}RCD is greater than the specified ^{t}RCD (MAX) limit, then access time is controlled exclusively by ^{t}CAC.
18. Operation within the ^{t}RAD (MAX) limit ensures that ^{t}RAC (MIN) and ^{t}CAC (MIN) can be met. ^{t}RAD (MAX) is specified as a reference point only; if ^{t}RAD is greater than the specified ^{t}RAD (MAX) limit, then access time is controlled exclusively by ^{t}AA.
19. Either ^{t}RCH or ^{t}RRH must be satisfied for a READ cycle.
20. ^{t}OFF (MAX) defines the time at which the output achieves the open circuit condition, and is not referenced to VOH or VOL.
21. ^{t}WCS, ^{t}RWD, ^{t}AWD and ^{t}CWD are not restrictive operating parameters. ^{t}WCS applies to EARLY-WRITE cycles. ^{t}RWD, ^{t}AWD and ^{t}CWD apply to READ-MODIFY-WRITE cycles. If ^{t}WCS ≥ ^{t}WCS (MIN), the cycle is an EARLY-WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If ^{t}RWD ≥ ^{t}RWD (MIN), ^{t}AWD ≥ ^{t}AWD (MIN) and ^{t}CWD ≥ ^{t}CWD (MIN), the cycle is a READ-MODIFY-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of data out is indeterminate. $\overline{OE}$ held HIGH and $\overline{WE}$ taken LOW after $\overline{CAS}$ goes LOW results in a LATE-WRITE ($\overline{OE}$ controlled) cycle. ^{t}WCS, ^{t}RWD, ^{t}CWD and ^{t}AWD are not applicable in a LATE-WRITE cycle.
22. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY-WRITE cycles and $\overline{WE}$ leading edge in LATE-WRITE or READ-MODIFY-WRITE cycles.
23. If $\overline{OE}$ is tied permanently LOW, LATE-WRITE or READ-MODIFY-WRITE operations are not possible.
24. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW and $\overline{OE}$ = HIGH.
25. ^{t}WTS and ^{t}WTH are setup and hold specifications for the $\overline{WE}$ pin being held LOW to enable the JEDEC test mode (with CBR timing constraints). These two parameters are the inverts of ^{t}WRP and ^{t}WRH in the CBR refresh cycle.
26. LATE-WRITE and READ-MODIFY-WRITE cycles must have both ^{t}OD and ^{t}OEH met ($\overline{OE}$ HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. The DQs will provide the previously read data if $\overline{CAS}$ remains LOW and $\overline{OE}$ is taken back LOW after ^{t}OEH is met. If $\overline{CAS}$ goes HIGH prior to $\overline{OE}$ going back LOW, the DQs will remain open.
27. The DQs open during READ cycles once ^{t}OD or ^{t}OFF occur. If $\overline{CAS}$ goes HIGH first, $\overline{OE}$ becomes a "don't care." If $\overline{OE}$ goes HIGH and $\overline{CAS}$ stays LOW, $\overline{OE}$ is not a "don't care;" and the DQs will provide the previously read data if $\overline{OE}$ is taken back LOW (while $\overline{CAS}$ remains LOW).
28. JEDEC test version only.

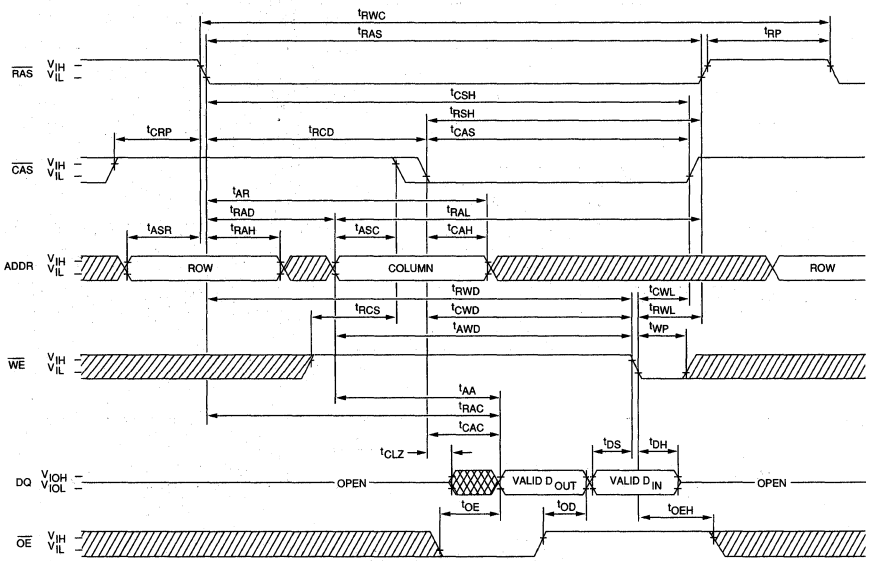
READ CYCLE



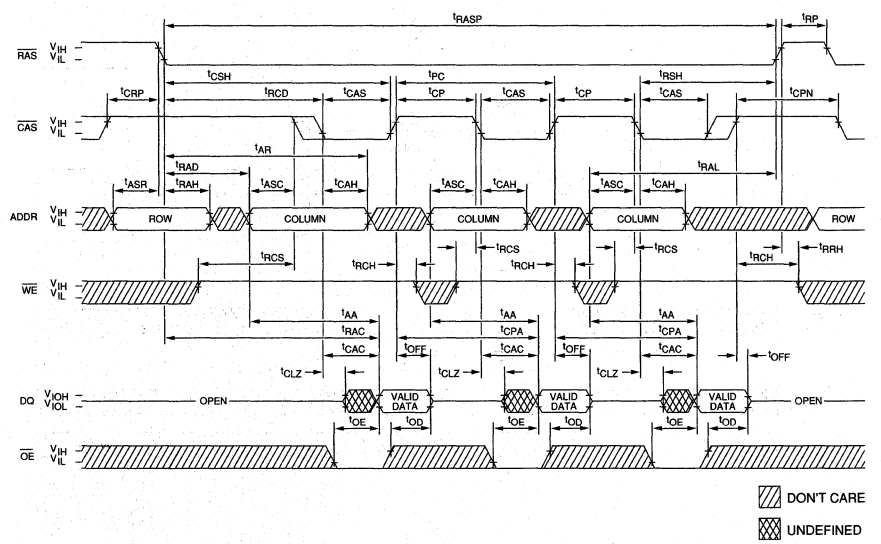
EARLY-WRITE CYCLE



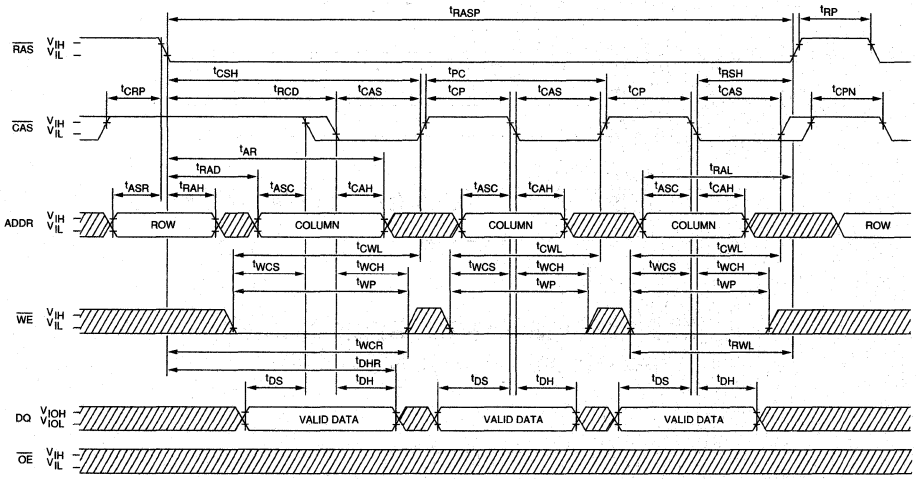
READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)



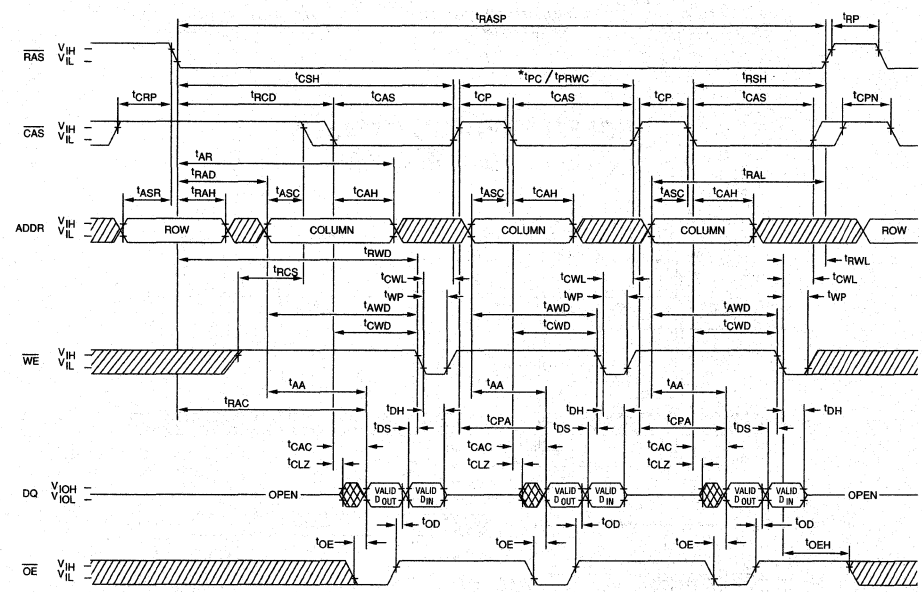
FAST-PAGE-MODE READ CYCLE



FAST-PAGE-MODE EARLY-WRITE CYCLE



FAST-PAGE-MODE READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)

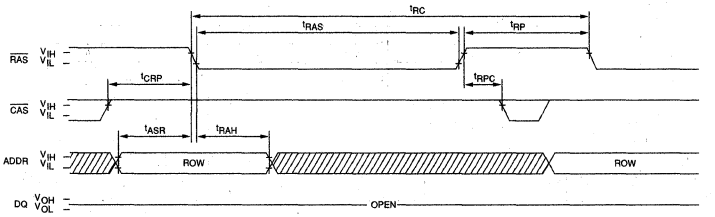


DON'T CARE

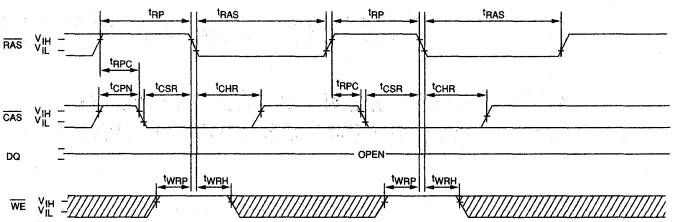
UNDEFINED

*tPC is for LATE-WRITE only.

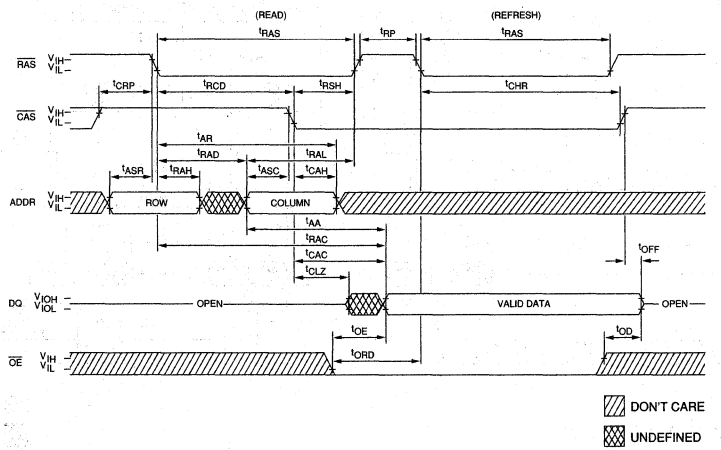
RAS-ONLY REFRESH CYCLE
(ADDR = A0-A9; WE = DON'T CARE)



CAS-BEFORE-RAS REFRESH CYCLE
(A0-A9, and OE = DON'T CARE)



HIDDEN REFRESH CYCLE [24]
(WE = HIGH; OE = LOW)



4 MEG POWER-UP AND REFRESH CONSTRAINTS

The EIA/JEDEC 4 Meg DRAM introduces two potential incompatibilities compared to the previous generation 1 Meg DRAM. The incompatibilities involve refresh and power-up. Understanding these incompatibilities and providing for them will offer the designer and system user greater compatibility between the 1 Meg and 4 Meg.

REFRESH

The most commonly used refresh mode of the 1 Meg is the CBR ($\overline{CAS}$-BEFORE-$\overline{RAS}$) REFRESH cycle. The CBR for the 1 Meg specifies the $\overline{WE}$ pin as a "don't care." The 4 Meg, on the other hand, specifies the CBR REFRESH mode with the $\overline{WE}$ pin held at a voltage HIGH level.

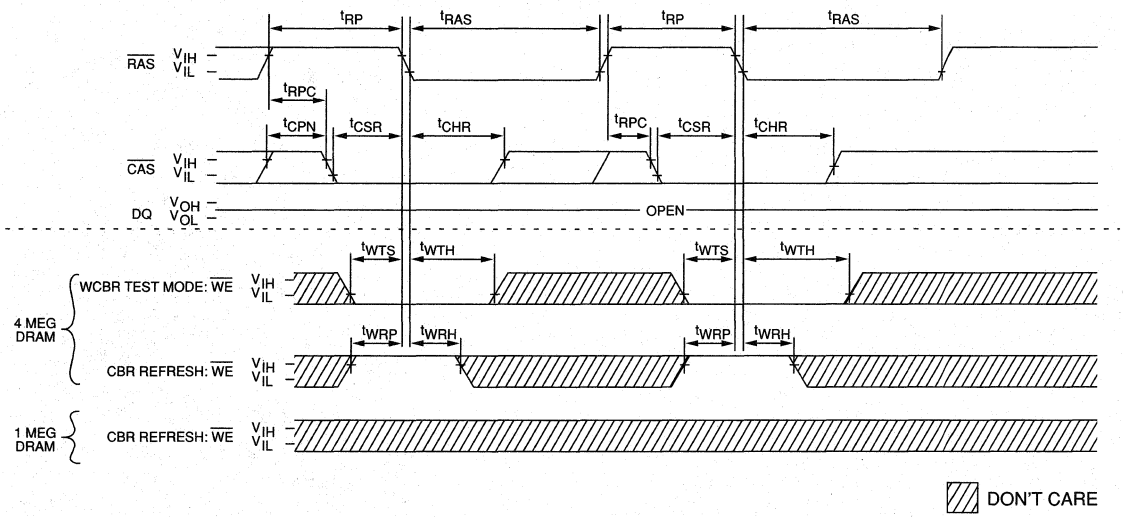
A CBR cycle with $\overline{WE}$ LOW will put the 4 Meg into the JEDEC specified test mode (WCBR).

POWER-UP

The 4 Meg JEDEC test mode constraint may introduce another problem. The 1 Meg POWER-UP cycle requires a 100µs delay followed by any eight $\overline{RAS}$ cycles. The 4 Meg POWER-UP is more restrictive in that eight $\overline{RAS}$-ONLY or CBR REFRESH ($\overline{WE}$ held HIGH) cycles must be used. The restriction is needed since the 4 Meg may power-up in the JEDEC specified test mode and must exit out of the test mode. The only way to exit the 4 Meg JEDEC test mode is with either a $\overline{RAS}$-ONLY or a CBR REFRESH cycle ($\overline{WE}$ held HIGH).

SUMMARY

1. The 1 Meg CBR REFRESH allows the $\overline{WE}$ pin to be "don't care" while the 4 Meg CBR requires $\overline{WE}$ to be HIGH.
2. The eight $\overline{RAS}$ wake-up cycles on the 1 Meg may be any valid $\overline{RAS}$ cycle while the 4 Meg may only use $\overline{RAS}$-ONLY or CBR REFRESH cycles ($\overline{WE}$ held HIGH).



COMPARISON OF 4 MEG TEST MODE AND WCBR TO 1 MEG CBR

NEW DRAM

DRAM

1 MEG x 4 DRAM

LOW POWER, EXTENDED REFRESH

FEATURES

- Industry standard x4 pinout, timing, functions and packages
- High-performance, CMOS silicon-gate process
- Single +5V ±10% power supply
- All inputs, outputs and clocks are fully TTL compatible
- Refresh modes: $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$ (CBR), HIDDEN and BATTERY BACKUP (BBU)
- FAST PAGE MODE access cycle
- 1,024-cycle extended refresh distributed across 128ms
- Low power, 1mW standby; 225mW active, typical

OPTIONS / MARKING

- Timing

60ns access	-6
70ns access	-7
80ns access	-8

- Packages

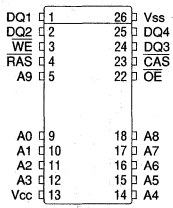
Plastic SOJ (300 mil)	DJ
Plastic TSOP (300 mil)*	TG
Plastic ZIP (350 mil)	Z

NOTE: Available in die form (commercial or military) or military ceramic packages. Please consult factory for die data sheets or refer to Micron's *Military Data Book.*

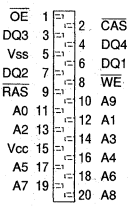
- Part Number Example: MT4C4001JDJ-6 L

PIN ASSIGNMENT (Top View)

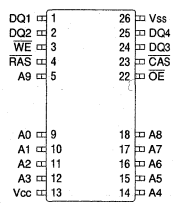
20-Pin SOJ (N-2)



20-Pin ZIP (O-1)



20-Pin TSOP (R-1)



*Consult factory on availability of reverse pinout TSOP packages

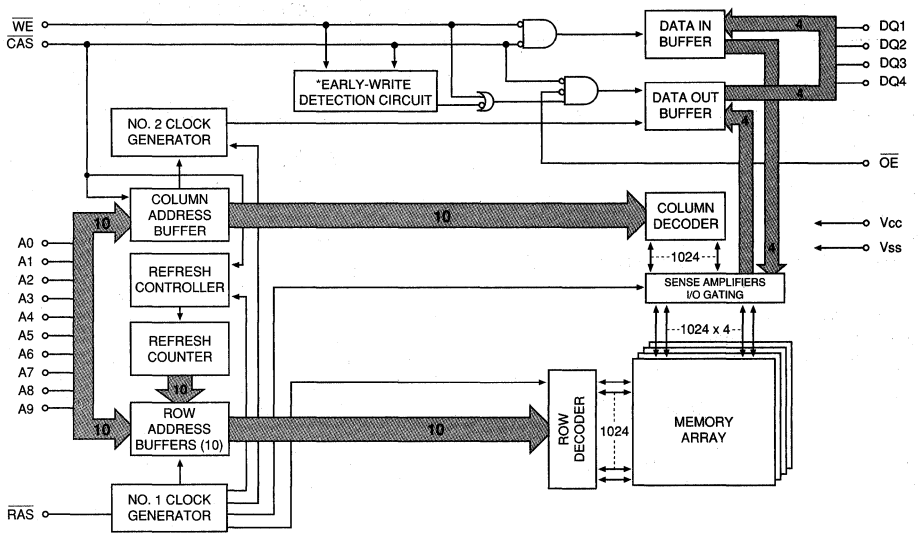
GENERAL DESCRIPTION

The MT4C4001J L is a randomly accessed solid-state memory containing 4,194,304 bits organized in a x4 configuration. During READ or WRITE cycles, each bit is uniquely addressed through the 20 address bits, which are entered 10 bits (A0-A9) at a time. $\overline{RAS}$ is used to latch the first 10 bits and $\overline{CAS}$ the latter 10 bits. READ and WRITE cycles are selected with the $\overline{WE}$ input. A logic HIGH on $\overline{WE}$ dictates READ mode while a logic LOW on $\overline{WE}$ dictates WRITE mode. During a WRITE cycle, data in (D) is latched by the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. If $\overline{WE}$ goes LOW prior to $\overline{CAS}$ going LOW, the output pin(s) remain open (High-Z) until the next $\overline{CAS}$ cycle. If $\overline{WE}$ goes LOW after data reaches the output pins, the outputs (Qs) are activated and retain the selected cell data as long as $\overline{CAS}$ remains LOW (regardless of $\overline{WE}$ or $\overline{RAS}$). This late $\overline{WE}$ pulse results in a READ-WRITE cycle. The four data inputs and four data outputs are routed through four pins using common I/O, and pin direction is controlled by $\overline{WE}$ and $\overline{OE}$.

FAST PAGE MODE operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row address (A0-A9) defined page boundary. The FAST PAGE MODE cycle is always initiated with a row address strobed-in by $\overline{RAS}$ followed by a column address strobed-in by $\overline{CAS}$. $\overline{CAS}$ may be toggled-in by holding $\overline{RAS}$ LOW and strobing-in different column addresses, thus executing faster memory cycles. Returning $\overline{RAS}$ HIGH terminates the FAST PAGE MODE operation.

Returning $\overline{RAS}$ and $\overline{CAS}$ HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the $\overline{RAS}$ high time. Memory cell data is retained in its correct state by maintaining power and executing any $\overline{RAS}$ cycle (READ, WRITE, $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$ (CBR), BATTERY BACKUP or HIDDEN refresh) so that all 1,024 combinations of $\overline{RAS}$ addresses (A0-A9) are executed at least every 128ms, regardless of sequence. The CBR refresh cycle will invoke the internal refresh counter for automatic $\overline{RAS}$ addressing.

FUNCTIONAL BLOCK DIAGRAM
FAST PAGE MODE



*NOTE: WE LOW prior to CAS LOW, EW detection circuit output is a HIGH (EARLY-WRITE)
CAS LOW prior to WE LOW, EW detection circuit output is a LOW (LATE-WRITE)

TRUTH TABLE

FUNCTION		RAS	CAS	WE	OE	ADDRESSES tR	ADDRESSES tC	DATA IN/OUT DQ1-DQ4
Standby		H	H→X	X	X	X	X	High-Z
READ		L	L	H	L	ROW	COL	Data Out
EARLY-WRITE		L	L	L	X	ROW	COL	Data In
READ-WRITE		L	L	H→L	L→H	ROW	COL	Data Out, Data In
FAST-PAGE-MODE	1st Cycle	L	H→L	H	L	ROW	COL	Data Out
READ	2nd Cycle	L	H→L	H	L	n/a	COL	Data Out
FAST-PAGE-MODE	1st Cycle	L	H→L	L	X	ROW	COL	Data In
EARLY-WRITE	2nd Cycle	L	H→L	L	X	n/a	COL	Data In
FAST-PAGE-MODE	1st Cycle	L	H→L	H→L	L→H	ROW	COL	Data Out, Data In
READ-WRITE	2nd Cycle	L	H→L	H→L	L→H	n/a	COL	Data Out, Data In
RAS-ONLY REFRESH		L	H	X	X	ROW	n/a	High-Z
HIDDEN	READ	L→H→L	L	H	L	ROW	COL	Data Out
REFRESH	WRITE	L→H→L	L	L	X	ROW	COL	Data In
CAS-BEFORE-RAS REFRESH		H→L	L	H	X	X	X	High-Z
BATTERY BACKUP REFRESH		H→L	L	H	X	X	X	High-Z

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Vss ..... -1V to +7V
Operating Temperature, T_A (Ambient) ..... 0°C to +70°C
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 3, 4, 6, 7) (V_{CC} = 5V ±10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.5	V	1
Input High (Logic 1) Voltage, All Inputs	V_{IH}	2.4	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, All Inputs	V_{IL}	-1.0	0.8	V	1
INPUT LEAKAGE CURRENT Any Input 0V ≤ V_{IN} ≤ 6.5V (All other pins not under test = 0V)	I_I	-2	2	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled, 0V ≤ V_{OUT} ≤ 5.5V)	I_{OZ}	-10	10	µA	
OUTPUT LEVELS Output High Voltage (I_{OUT} = -5mA)	V_{OH}	2.4		V	
Output Low Voltage (I_{OUT} = 4.2mA)	V_{OL}		0.4	V	

		MAX				
PARAMETER/CONDITION	SYMBOL	-6	-7	-8	UNITS	NOTES
STANDBY CURRENT: (TTL) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC1}	2	2	2	mA	
STANDBY CURRENT: (CMOS) ($\overline{RAS}$ = $\overline{CAS}$ = Other Inputs = V_{CC} -0.2V)	I_{CC2}	200	200	200	µA	
OPERATING CURRENT: Random READ/WRITE Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC (MIN))	I_{CC3}	110	100	90	mA	3, 4
OPERATING CURRENT: FAST PAGE MODE Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: ^tPC = ^tPC (MIN))	I_{CC4}	80	70	60	mA	3, 4
REFRESH CURRENT: $\overline{RAS}$-ONLY Average power supply current ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}: ^tRC = ^tRC (MIN))	I_{CC5}	110	100	90	mA	3
REFRESH CURRENT: $\overline{CAS}$-BEFORE-$\overline{RAS}$ (CBR) Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC (MIN))	I_{CC6}	110	100	90	mA	3, 5
REFRESH CURRENT: BATTERY BACKUP (BBU) Average power supply current during BATTERY BACKUP refresh: $\overline{CAS}$ = 0.2V or $\overline{CAS}$-BEFORE-$\overline{RAS}$ cycling; $\overline{RAS}$ = ^tRAS (MIN) to 300ns; $\overline{WE}$ = V_{CC} -0.2V; A0-A9 and D_{IN} = V_{CC} - 0.2V or 0.2V (D_{IN} may be left open), ^tRC = 125µs (1,024 rows at 125µs = 128ms)	I_{CC7}	300	300	300	µA	3, 5, 7, 28

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A9	C_{I1}		5	pF	2
Input Capacitance: $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$	C_{I2}		7	pF	2
Input/Output Capacitance: DQ	C_{IO}		7	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13, 23) (V_{CC} = 5V ±10%)

AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	t_{RC}	110		130		150		ns	
READ-WRITE cycle time	t_{RWC}	145		185		205		ns	
FAST-PAGE-MODE READ or WRITE cycle time	t_{PC}	40		40		45		ns	
FAST-PAGE-MODE READ-WRITE cycle time	t_{PRWC}	90		95		100		ns	
Access time from $\overline{RAS}$	t_{RAC}		60		70		80	ns	14
Access time from $\overline{CAS}$	t_{CAC}		15		20		20	ns	15
Output Enable	t_{OE}		15		20		20	ns	23
Access time from column address	t_{AA}		30		35		40	ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		35		40		45	ns	
$\overline{RAS}$ pulse width	t_{RAS}	60	100,000	70	100,000	80	100,000	ns	
$\overline{RAS}$ pulse width (FAST PAGE MODE)	t_{RASP}	60	100,000	70	100,000	80	100,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	15		20		20		ns	
$\overline{RAS}$ precharge time	t_{RP}	40		50		60		ns	
$\overline{CAS}$ pulse width	t_{CAS}	15	100,000	20	100,000	20	100,000	ns	
$\overline{CAS}$ hold time	t_{CSH}	60		70		80		ns	
$\overline{CAS}$ precharge time	t_{CPN}	10		10		10		ns	16
$\overline{CAS}$ precharge time (FAST PAGE MODE)	t_{CP}	10		10		10		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	45	20	50	20	60	ns	17
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		10		10		ns	
Row address setup time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	10		10		10		ns	
$\overline{RAS}$ to column address delay time	t_{RAD}	15	30	15	35	15	40	ns	18
Column address setup time	t_{ASC}	0		0		0		ns	
Column address hold time	t_{CAH}	10		15		15		ns	
Column address hold time (referenced to $\overline{RAS}$)	t_{AR}	50		55		60		ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	30		35		40		ns	
Read command setup time	t_{RCS}	0		0		0		ns	
Read command hold time (referenced to $\overline{CAS}$)	t_{RCH}	0		0		0		ns	19
Read command hold time (referenced to $\overline{RAS}$)	t_{RRH}	0		0		0		ns	19
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	0		0		0		ns	
Output buffer turn-off delay	t_{OFF}	0	15	0	20	0	20	ns	20

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

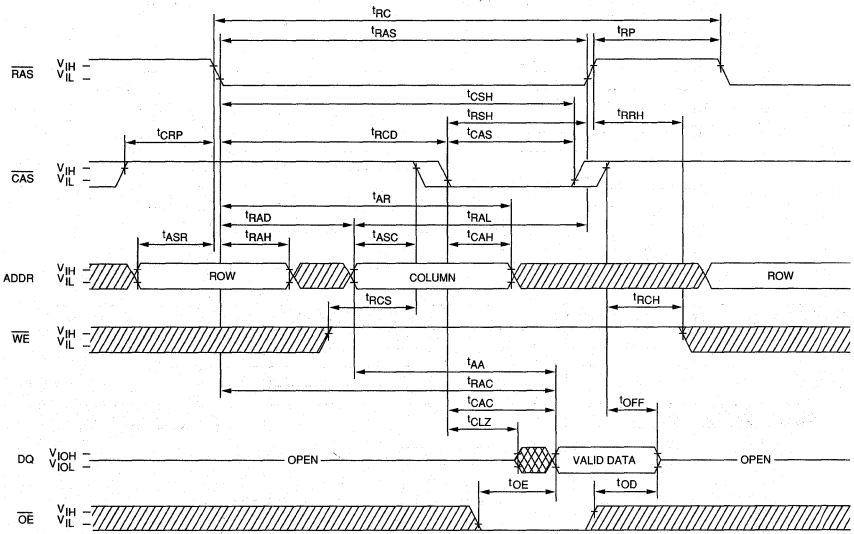
(Notes: 6, 7, 8, 9, 10, 11, 12, 13, 23) (V_{CC} = 5V ±10%)

AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
$\overline{WE}$ command setup time	^tWCS	0		0		0		ns	21, 27
Write command hold time	^tWCH	10		15		15		ns	
Write command hold time (referenced to $\overline{RAS}$)	^tWCR	45		55		60		ns	
Write command pulse width	^tWP	10		15		15		ns	
Write command to $\overline{RAS}$ lead time	^tRWL	15		20		20		ns	
Write command to $\overline{CAS}$ lead time	^tCWL	15		20		20		ns	
Data-in setup time	^tDS	0		0		0		ns	22
Data-in hold time	^tDH	10		15		15		ns	22
Data-in hold time (referenced to $\overline{RAS}$)	^tDHR	45		55		60		ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	^tRWD	90		100		110		ns	21
Column address to $\overline{WE}$ delay time	^tAWD	60		65		70		ns	21
$\overline{CAS}$ to $\overline{WE}$ delay time	^tCWD	45		50		50		ns	21
Transition time (rise or fall)	^tT	3	50	3	50	3	50	ns	9, 10
Refresh period (1024 cycles)	^tREF		128		128		128	ms	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	^tRPC	0		0		0		ns	
$\overline{CAS}$ setup time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tCSR	10		10		10		ns	5
$\overline{CAS}$ hold time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tCHR	15		15		15		ns	5
$\overline{WE}$ hold time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tWRH	10		10		10		ns	25
$\overline{WE}$ setup time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tWRP	10		10		10		ns	25
$\overline{WE}$ hold time (WCBR test cycle)	^tWTH	10		10		10		ns	25
$\overline{WE}$ setup time (WCBR test cycle)	^tWTS	10		10		10		ns	25
$\overline{OE}$ setup prior to RAS during HIDDEN REFRESH cycle	^tORD	0		0		0		ns	
Output disable	^tOD		15		20		20	ns	27
$\overline{OE}$ hold time from $\overline{WE}$ during READ-MODIFY-WRITE cycle	^tOEH	15		20		20		ns	26

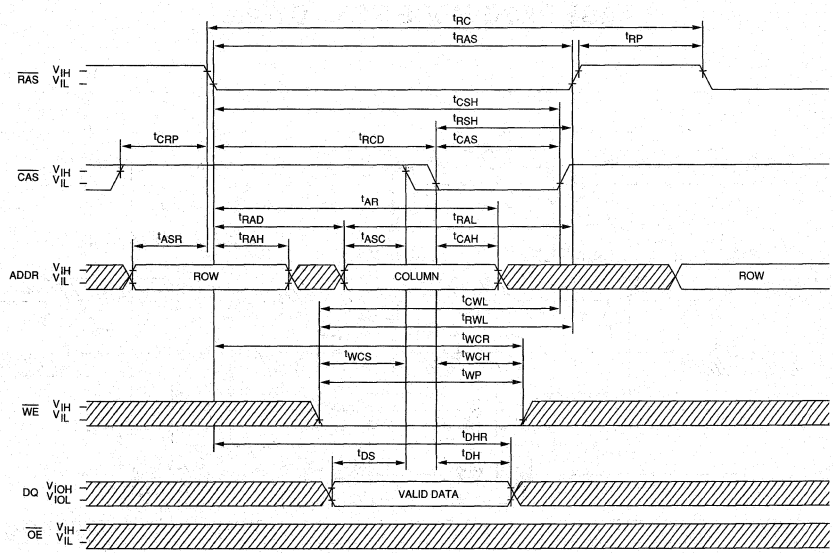
NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. V_{CC} = 5V ±10%, f = 1 MHz.
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is assured.
7. An initial pause of 100µs is required after power-up followed by eight $\overline{RAS}$ refresh cycles ($\overline{RAS}$-ONLY or CBR with $\overline{WE}$ HIGH) before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-up should be repeated any time the ^{t}REF refresh requirement is exceeded.
8. AC characteristics assume ^{t}T = 5ns.
9. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS}$ = V_{IH}, data output is High-Z.
12. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to 2 TTL gates and 100pF.
14. Assumes that $^{t}RCD < {}^{t}RCD$ (MAX). If ^{t}RCD is greater than the maximum recommended value shown in this table, ^{t}RAC will increase by the amount that ^{t}RCD exceeds the value shown.
15. Assumes that $^{t}RCD \geq {}^{t}RCD$ (MAX).
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer, $\overline{CAS}$ must be pulsed HIGH for ^{t}CPN.
17. Operation within the ^{t}RCD (MAX) limit ensures that ^{t}RAC (MAX) can be met. ^{t}RCD (MAX) is specified as a reference point only; if ^{t}RCD is greater than the specified ^{t}RCD (MAX) limit, then access time is controlled exclusively by ^{t}CAC.
18. Operation within the ^{t}RAD (MAX) limit ensures that ^{t}RAC (MIN) and ^{t}CAC (MIN) can be met. ^{t}RAD (MAX) is specified as a reference point only; if ^{t}RAD is greater than the specified ^{t}RAD (MAX) limit, then access time is controlled exclusively by ^{t}AA.
19. Either ^{t}RCH or ^{t}RRH must be satisfied for a READ cycle.
20. ^{t}OFF (MAX) defines the time at which the output achieves the open circuit condition, and is not referenced to V_{OH} or V_{OL}.
21. ^{t}WCS, ^{t}RWD, ^{t}AWD and ^{t}CWD are not restrictive operating parameters. ^{t}WCS applies to EARLY-WRITE cycles. ^{t}RWD, ^{t}AWD and ^{t}CWD apply to READ-MODIFY-WRITE cycles. If $^{t}WCS \geq {}^{t}WCS$ (MIN), the cycle is an EARLY-WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If $^{t}RWD \geq {}^{t}RWD$ (MIN), $^{t}AWD \geq {}^{t}AWD$ (MIN) and $^{t}CWD \geq {}^{t}CWD$ (MIN), the cycle is a READ-MODIFY-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of data out is indeterminate. $\overline{OE}$ held HIGH and $\overline{WE}$ taken LOW after $\overline{CAS}$ goes LOW results in a LATE-WRITE ($\overline{OE}$ controlled) cycle. ^{t}WCS, ^{t}RWD, ^{t}CWD and ^{t}AWD are not applicable in a LATE-WRITE cycle.
22. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY-WRITE cycles and $\overline{WE}$ leading edge in LATE-WRITE or READ-MODIFY-WRITE cycles.
23. If $\overline{OE}$ is tied permanently LOW, LATE-WRITE or READ-MODIFY-WRITE operations are not possible.
24. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW and $\overline{OE}$ = HIGH.
25. ^{t}WTS and ^{t}WTH are setup and hold specifications for the $\overline{WE}$ pin being held LOW to enable the JEDEC test mode (with CBR timing constraints). These two parameters are the inverts of ^{t}WRP and ^{t}WRH in the CBR refresh cycle.
26. LATE-WRITE and READ-MODIFY-WRITE cycles must have both ^{t}OD and ^{t}OEH met ($\overline{OE}$ HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. The DQs will provide the previously read data if $\overline{CAS}$ remains LOW and $\overline{OE}$ is taken back LOW after ^{t}OEH is met. If $\overline{CAS}$ goes HIGH prior to $\overline{OE}$ going back LOW, the DQs will remain open.
27. The DQs open during READ cycles once ^{t}OD or ^{t}OFF occur. If $\overline{CAS}$ goes HIGH first, $\overline{OE}$ becomes a "don't care." If $\overline{OE}$ goes HIGH and $\overline{CAS}$ stays LOW, $\overline{OE}$ is not a "don't care;" and the DQs will provide the previously read data if $\overline{OE}$ is taken back LOW (while $\overline{CAS}$ remains LOW).
28. BBU current is reduced as ^{t}RAS is reduced from its maximum specification during the BBU cycle.

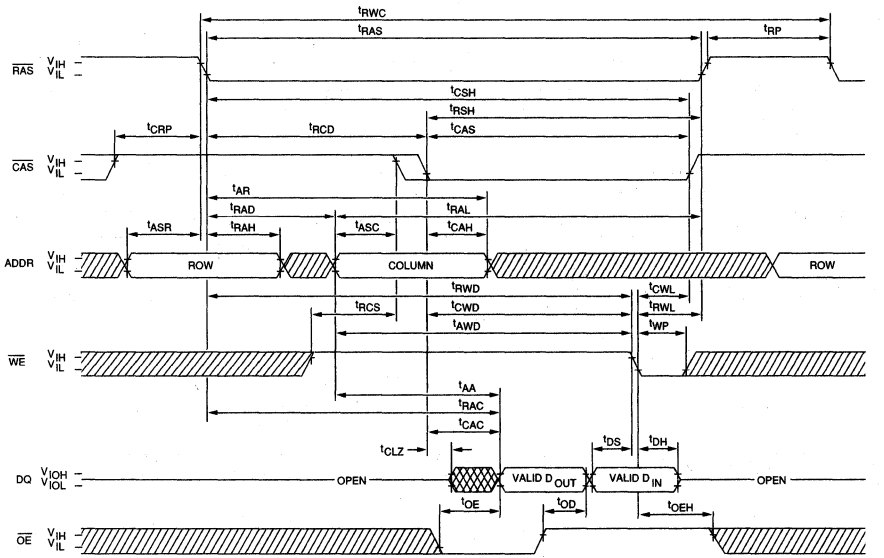
READ CYCLE



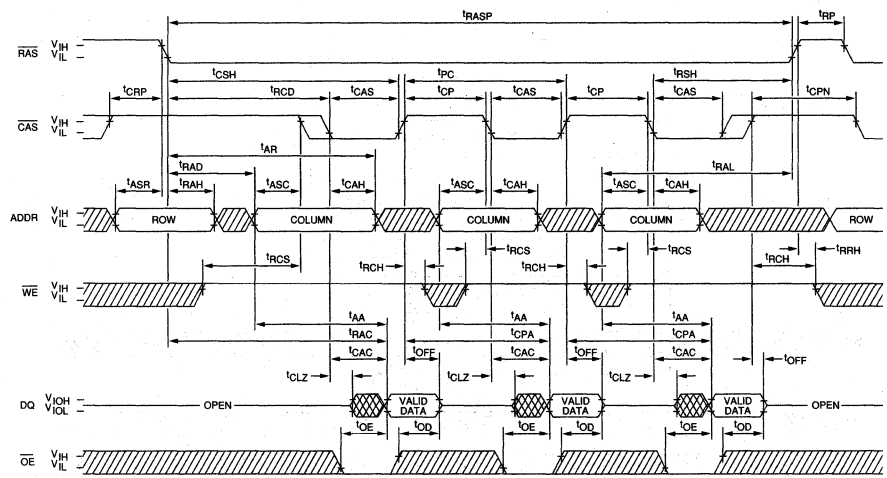
EARLY-WRITE CYCLE



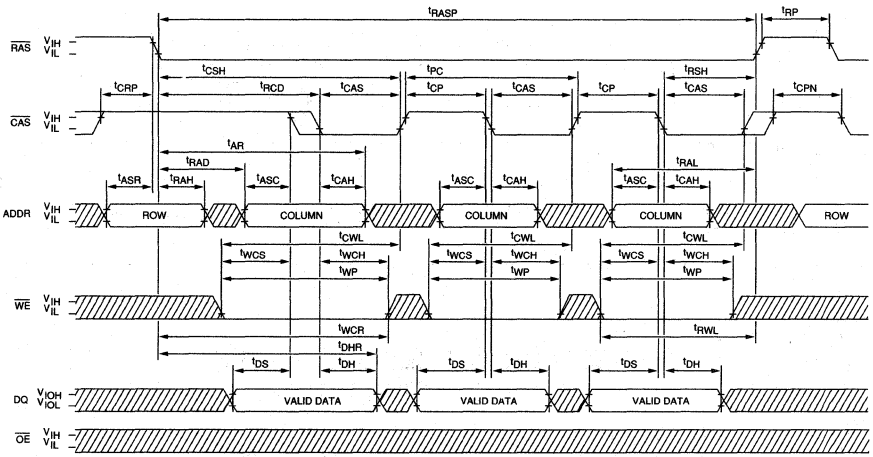
READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)



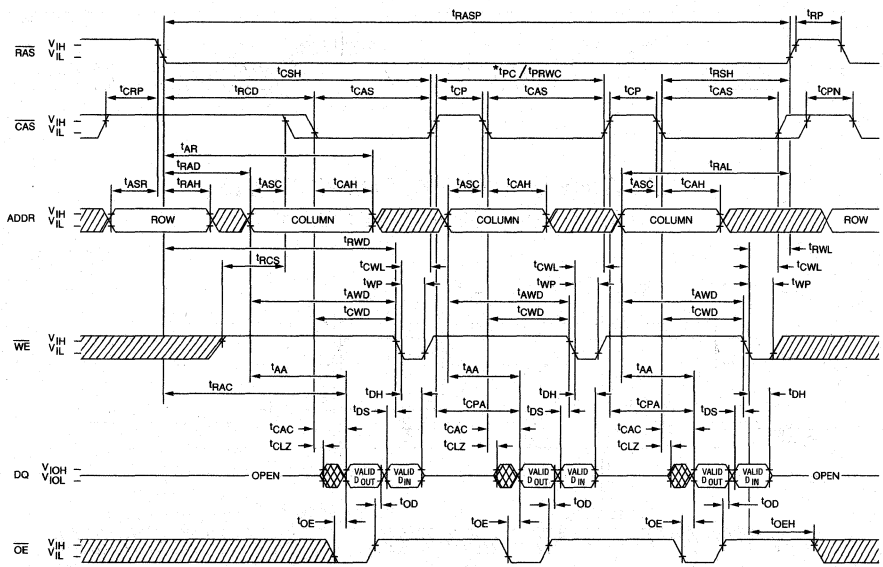
FAST-PAGE-MODE READ CYCLE



FAST-PAGE-MODE EARLY-WRITE CYCLE

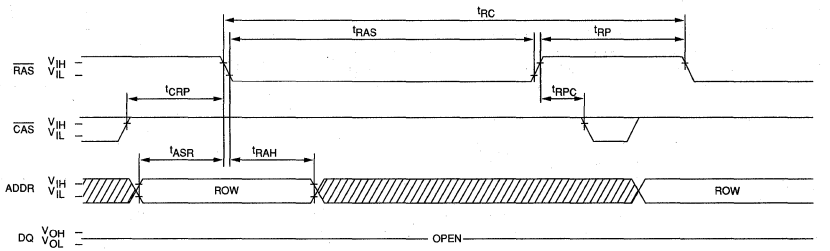


FAST-PAGE-MODE READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)

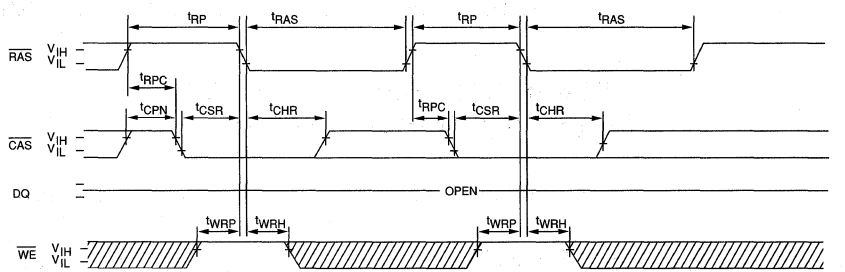


*tPC is for LATE-WRITE only.

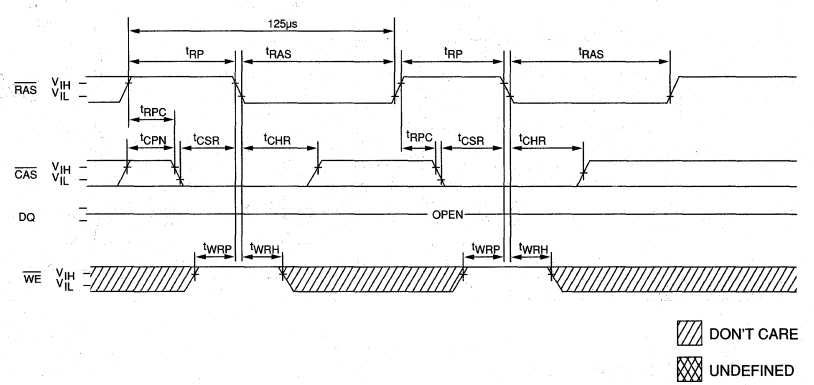
$\overline{\text{RAS}}$-ONLY REFRESH CYCLE
(ADDR = A0-A9; $\overline{\text{WE}}$ = DON'T CARE)



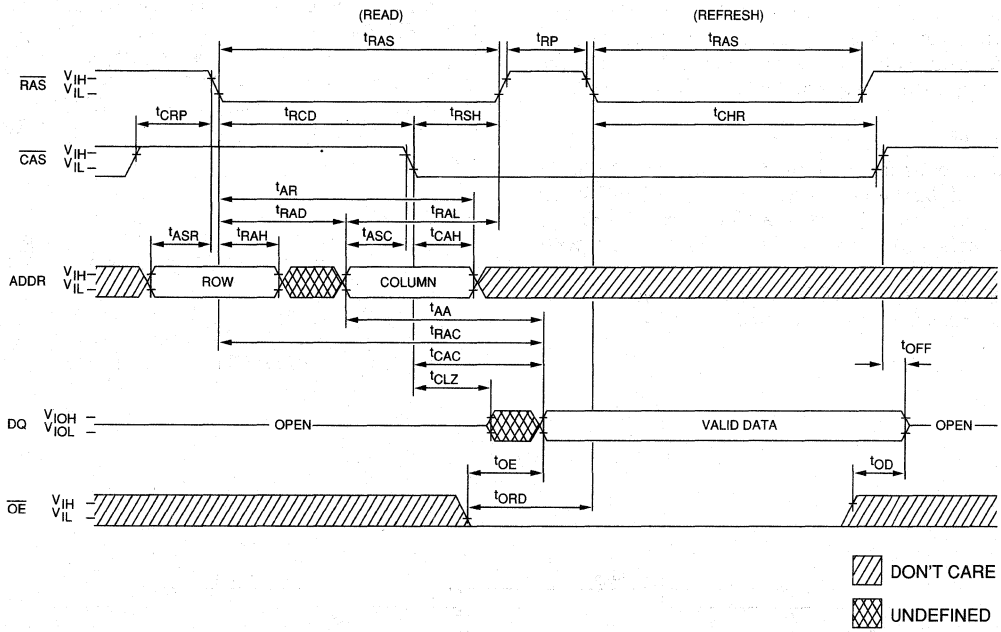
$\overline{\text{CAS}}$-BEFORE-$\overline{\text{RAS}}$ REFRESH CYCLE
(A0-A9, and $\overline{\text{OE}}$ = DON'T CARE)



BATTERY BACKUP REFRESH CYCLE
(A0-A9, and $\overline{\text{OE}}$ = DON'T CARE)



HIDDEN REFRESH CYCLE [24]
($\overline{WE}$ = HIGH; $\overline{OE}$ = LOW)



4 MEG POWER-UP AND REFRESH CONSTRAINTS

The EIA/JEDEC 4 Meg DRAM introduces two potential incompatibilities compared to the previous generation 1 Meg DRAM. The incompatibilities involve refresh and power-up. Understanding these incompatibilities and providing for them will offer the designer and system user greater compatibility between the 1 Meg and 4 Meg.

REFRESH

The most commonly used refresh mode of the 1 Meg is the CBR ($\overline{CAS}$-BEFORE-$\overline{RAS}$) REFRESH cycle. The CBR for the 1 Meg specifies the $\overline{WE}$ pin as a "don't care." The 4 Meg, on the other hand, specifies the CBR REFRESH mode with the $\overline{WE}$ pin held at a voltage HIGH level.

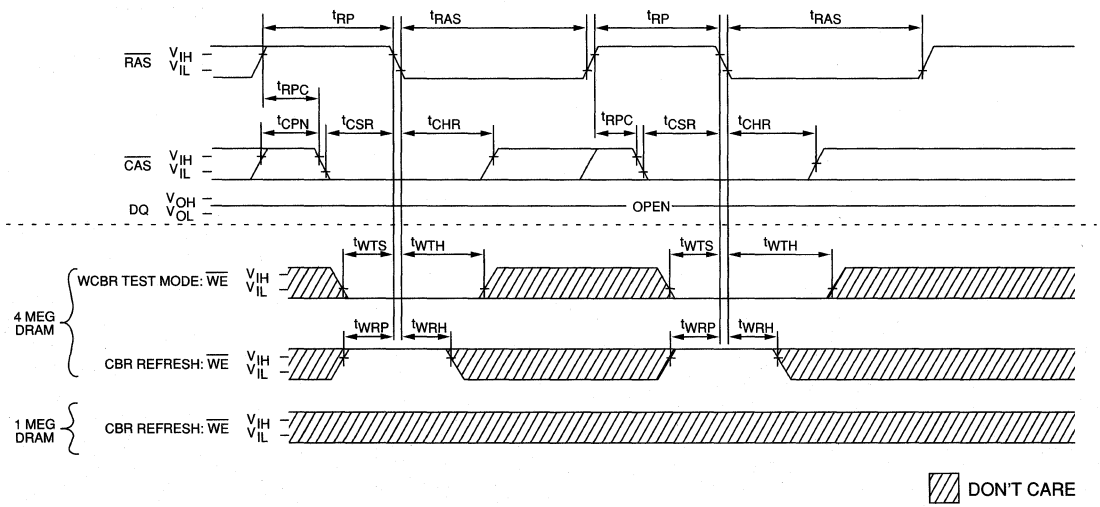
A CBR cycle with $\overline{WE}$ LOW will put the 4 Meg into the JEDEC specified test mode (WCBR).

POWER-UP

The 4 Meg JEDEC test mode constraint may introduce another problem. The 1 Meg POWER-UP cycle requires a 100µs delay followed by any eight $\overline{RAS}$ cycles. The 4 Meg POWER-UP is more restrictive in that eight $\overline{RAS}$-ONLY or CBR REFRESH ($\overline{WE}$ held HIGH) cycles must be used. The restriction is needed since the 4 Meg may power-up in the JEDEC specified test mode and must exit out of the test mode. The only way to exit the 4 Meg JEDEC test mode is with either a $\overline{RAS}$-ONLY or a CBR REFRESH cycle ($\overline{WE}$ held HIGH).

SUMMARY

1. The 1 Meg CBR REFRESH allows the $\overline{WE}$ pin to be "don't care" while the 4 Meg CBR requires $\overline{WE}$ to be HIGH.
2. The eight $\overline{RAS}$ wake-up cycles on the 1 Meg may be any valid $\overline{RAS}$ cycle while the 4 Meg may only use $\overline{RAS}$-ONLY or CBR REFRESH cycles ($\overline{WE}$ held HIGH).



COMPARISON OF 4 MEG TEST MODE AND WCBR TO 1 MEG CBR

DRAM

1 MEG x 4 DRAM

STATIC COLUMN

FEATURES

- Industry standard x4 pinout, timing, functions and packages
- High-performance, CMOS silicon-gate process
- Single +5V ±10% power supply
- Low power, 3mW standby; 225mW active, typical
- All inputs, outputs and clocks are fully TTL compatible
- 1,024-cycle refresh distributed across 16ms
- Refresh modes: $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$ (CBR), and HIDDEN
- STATIC COLUMN access cycle

OPTIONS MARKING

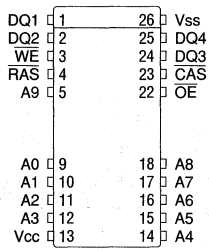
- Timing
  - 70ns access -7
  - 80ns access -8
- Packages
  - Plastic SOJ (300 mil) DJ
  - Plastic ZIP (350 mil) Z

NOTE: Available in die form (commercial or military) or military ceramic packages. Please consult factory for die data sheets or refer to Micron's ***Military Data Book.***

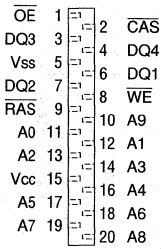
- Part Number Example: MT4C4003JDJ-7

PIN ASSIGNMENT (Top View)

20-Pin SOJ
(N-2)



20-Pin ZIP
(O-1)



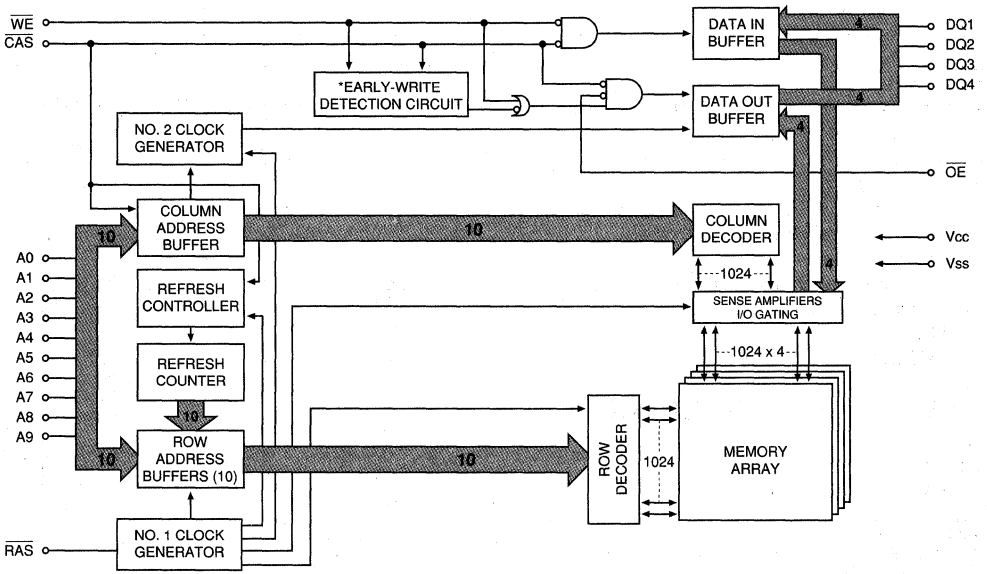
GENERAL DESCRIPTION

The MT4C4003J is a randomly accessed solid-state memory containing 4,194,304 bits organized in a x4 configuration. During READ or WRITE cycles, each bit is uniquely addressed through the 20 address bits, which are entered 10 bits (A0-A9) at a time. $\overline{RAS}$ is used to latch the first 10 bits and $\overline{CAS}$ the latter 10 bits. READ and WRITE cycles are selected with the $\overline{WE}$ input. A logic HIGH on $\overline{WE}$ dictates READ mode while a logic LOW on $\overline{WE}$ dictates WRITE mode. During a WRITE cycle, data in (D) is latched by the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. If $\overline{WE}$ goes LOW prior to $\overline{CAS}$ going LOW, the output pin(s) remain open (High-Z) until the next $\overline{CAS}$ cycle. If $\overline{WE}$ goes LOW after data reaches the output pin(s), data out (Q) is activated and retains the selected cell data as long as $\overline{CAS}$ remains LOW (regardless of $\overline{WE}$ or $\overline{RAS}$). This late $\overline{WE}$ pulse results in a READ-WRITE cycle. The four data inputs and four data outputs are routed through four pins using common I/O and pin direction is controlled by $\overline{WE}$ and $\overline{OE}$.

STATIC COLUMN operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row address (A0-A9) defined page boundary. After the first read, any column address transition will result in new data out. Unlike the page-mode part, which requires $\overline{CAS}$ to be toggled for each successive page-mode access, the STATIC COLUMN part allows $\overline{CAS}$ to be left low for successive STATIC COLUMN accesses. Returning $\overline{RAS}$ HIGH terminates the STATIC COLUMN operation.

Returning $\overline{RAS}$ and $\overline{CAS}$ HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the $\overline{RAS}$ high time. Memory cell data is retained in its correct state by maintaining power and executing any $\overline{RAS}$ cycle (READ, WRITE, $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$ (CBR) or HIDDEN refresh) so that all 1,024 combinations of $\overline{RAS}$ addresses (A0-A9) are executed at least every 16ms, regardless of sequence. The CBR refresh cycle will invoke the internal refresh counter for automatic $\overline{RAS}$ addressing.

FUNCTIONAL BLOCK DIAGRAM
STATIC COLUMN



*NOTE: $\overline{WE}$ LOW prior to $\overline{CAS}$ LOW, EW detection circuit output is a HIGH (EARLY-WRITE)
$\overline{CAS}$ LOW prior to $\overline{WE}$ LOW, EW detection circuit output is a LOW (LATE-WRITE)

TRUTH TABLE

FUNCTION		$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	$\overline{OE}$	ADDRESSES ^tR	ADDRESSES ^tC	DATA IN/OUT DQ1-DQ4
Standby		H	H→X	X	X	X	X	High-Z
READ		L	L	H	L	ROW	COL	Data Out
EARLY-WRITE		L	L	L	X	ROW	COL	Data In
READ-WRITE		L	L	H→L	L→H	ROW	COL	Data Out, Data In
FAST-PAGE-MODE	1st Cycle	L	L	H	L	ROW	COL	Data Out
READ	2nd Cycle	L	L	H	L	n/a	COL	Data Out
FAST-PAGE-MODE	1st Cycle	L	L	L	X	ROW	COL	Data In
EARLY-WRITE	2nd Cycle	L	L	L	X	n/a	COL	Data In
FAST-PAGE-MODE	1st Cycle	L	L	H→L	L→H	ROW	COL	Data Out, Data In
READ-WRITE	2nd Cycle	L	L	H→L	L→H	n/a	COL	Data Out, Data In
$\overline{RAS}$-ONLY REFRESH		L	H	X	X	ROW	n/a	High-Z
HIDDEN	READ	L→H→L	L	H	L	ROW	COL	Data Out
REFRESH	WRITE	L→H→L	L	L	X	ROW	COL	Data In
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH		H→L	L	H	X	X	X	High-Z

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to V_{SS} ..... -1V to +7V
Operating Temperature, T_A (Ambient) ..... 0°C to +70°C
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 3, 4, 6, 7) (V_{CC} = 5V ±10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.5	V	1
Input High (Logic 1) Voltage, All Inputs	V_{IH}	2.4	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, All Inputs	V_{IL}	-1.0	0.8	V	1
INPUT LEAKAGE CURRENT Any Input 0V ≤ V_{IN} ≤ 6.5V (All other pins not under test = 0V)	I_I	-2	2	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled, 0V ≤ V_{OUT} ≤ 5.5V)	I_{OZ}	-10	10	µA	
OUTPUT LEVELS Output High Voltage (I_{OUT} = -5mA)	V_{OH}	2.4		V	
Output Low Voltage (I_{OUT} = 4.2mA)	V_{OL}		0.4	V	

		MAX			
PARAMETER/CONDITION	SYMBOL	-7	-8	UNITS	NOTES
STANDBY CURRENT: (TTL) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC1}	2	2	mA	
STANDBY CURRENT: (CMOS) ($\overline{RAS}$ = $\overline{CAS}$ = Other Inputs = V_{CC} -0.2V)	I_{CC2}	1	1	mA	
OPERATING CURRENT: Random READ/WRITE Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC (MIN))	I_{CC3}	100	90	mA	3, 4
OPERATING CURRENT: STATIC COLUMN Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: ^tSC = ^tSC (MIN))	I_{CC4}	70	60	mA	3, 4
REFRESH CURRENT: $\overline{RAS}$-ONLY Average power supply current ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}: ^tRC = ^tRC (MIN))	I_{CC5}	100	90	mA	3
REFRESH CURRENT: $\overline{CAS}$-BEFORE-$\overline{RAS}$ Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC (MIN))	I_{CC6}	100	90	mA	3, 5

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A9	C_{I1}		5	pF	2
Input Capacitance: $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$	C_{I2}		7	pF	2
Input/Output Capacitance: DQ	C_{IO}		7	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13, 23) (V_{CC} = 5.V ±10%)

AC CHARACTERISTICS		-7		-8			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Random READ or WRITE cycle time	^tRC	130		150		ns	
READ-WRITE cycle time	^tRWC	185		205		ns	
STATIC-COLUMN READ or WRITE cycle time	^tSC	40		45		ns	
STATIC-COLUMN READ-WRITE cycle time	^tSRWC	100		110		ns	
Access time from $\overline{RAS}$	^tRAC		70		80	ns	14
Access time from $\overline{CAS}$	^tCAC		20		20	ns	15
Output Enable	^tOE		20		20	ns	23
Access time from column address	^tAA		35		40	ns	
$\overline{RAS}$ pulse width	^tRAS	70	100,000	80	100,000	ns	
$\overline{RAS}$ pulse width (STATIC COLUMN)	^tRASC	70	100,000	80	100,000	ns	
$\overline{RAS}$ hold time	^tRSH	20		20		ns	
$\overline{RAS}$ precharge time	^tRP	50		60		ns	
$\overline{CAS}$ pulse width	^tCAS	20	100,000	20	100,000	ns	
$\overline{CAS}$ hold time	^tCSH	70		80		ns	
$\overline{CAS}$ precharge time	^tCPN	10		10		ns	16
$\overline{CAS}$ precharge time (STATIC COLUMN)	^tCP	10		10		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	^tRCD	20	50	20	60	ns	17
$\overline{CAS}$ to $\overline{RAS}$ precharge time	^tCRP	10		10		ns	
Row address setup time	^tASR	0		0		ns	
Row address hold time	^tRAH	10		10		ns	
$\overline{RAS}$ to column address delay time	^tRAD	15	35	15	40	ns	18
Column address setup time	^tASC	0		0		ns	
Column address hold time	^tCAH	15		15		ns	
Column address hold time (referenced to $\overline{RAS}$)	^tAR	75		85		ns	
Column address to $\overline{RAS}$ lead time	^tRAL	35		40		ns	
Read command setup time	^tRCS	0		0		ns	
Read command hold time (referenced to $\overline{CAS}$)	^tRCH	0		0		ns	19
Read command hold time (referenced to $\overline{RAS}$)	^tRRH	0		0		ns	19
$\overline{CAS}$ to output in Low-Z	^tCLZ	0		0		ns	
Output buffer turn-off delay	^tOFF	0	20	0	20	ns	20
Column address hold time (referenced to $\overline{RAS}$)	^tAWR	55		60		ns	
$\overline{WE}$ command setup time	^tWCS	0		0		ns	21, 27
Write command hold time	^tWCH	15		15		ns	
Write command hold time (referenced to $\overline{RAS}$)	^tWCR	55		60		ns	
Write command pulse width	^tWP	15		15		ns	
Write command to $\overline{RAS}$ lead time	^tRWL	20		20		ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

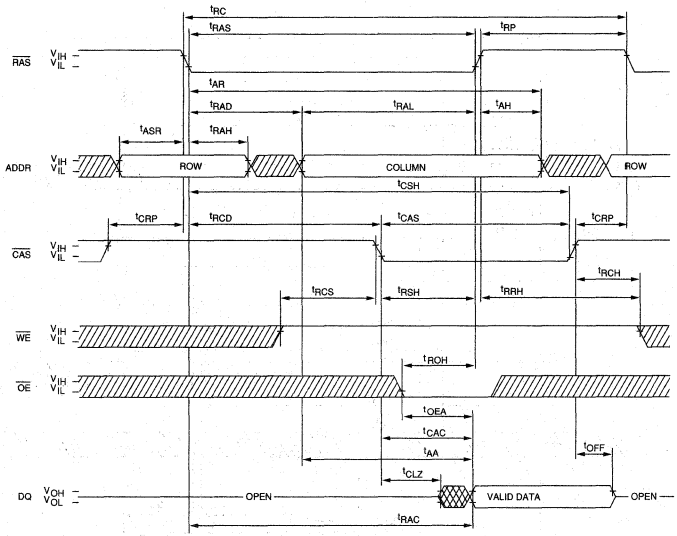
(Notes: 6, 7, 8, 9, 10, 11, 12, 13, 23) (V_{CC} = 5V ±10%)

AC CHARACTERISTICS		-7		-8			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Write command to $\overline{CAS}$ lead time	^tCWL	20		20		ns	
Data-in setup time	^tDS	0		0		ns	22
Data-in hold time	^tDH	15		15		ns	22
Data-in hold time (referenced to $\overline{RAS}$)	^tDHR	55		60		ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	^tRWD	100		110		ns	21
Column address to $\overline{WE}$ delay time	^tAWD	65		70		ns	21
$\overline{CAS}$ to $\overline{WE}$ delay time	^tCWD	50		50		ns	21
Transition time (rise or fall)	^tT	3	50	3	50	ns	9, 10
Refresh period (1,024 cycles)	^tREF		16		16	ms	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	^tRPC	0		0		ns	
$\overline{CAS}$ setup time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tCSR	10		10		ns	5
$\overline{CAS}$ hold time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tCHR	15		15		ns	5
$\overline{WE}$ hold time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tWRH	10		10		ns	25
$\overline{WE}$ setup time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tWRP	10		10		ns	25
$\overline{WE}$ hold time (WCBR test cycle)	^tWTH	10		10		ns	25
$\overline{WE}$ setup time (WCBR test cycle)	^tWTS	10		10		ns	25
$\overline{OE}$ setup prior to RAS during HIDDEN REFRESH cycle	^tORD	0		0		ns	
Output disable	^tOD		20		20	ns	27
$\overline{OE}$ hold time from $\overline{WE}$ during READ-MODIFY-WRITE cycle	^tOEH	20		20		ns	26
Write inactive time	^tWI	10		10		ns	
Previous WRITE to column address delay time	^tLWAD	20	30	20	35	ns	
Previous WRITE to column address hold time	^tAHLW	65		75		ns	
$\overline{RAS}$ hold time referenced to $\overline{OE}$	^tROH	10		10		ns	
Output data hold time from column address	^tAOH	5		5		ns	
Output data enable from WRITE	^tOW	^tAA + 5		^tAA + 5		ns	
Access time from last WRITE	^tALW	65		75		ns	
Column address hold time referenced to $\overline{RAS}$ HIGH	^tAH	5		10		ns	
$\overline{CAS}$ pulse width in STATIC-COLUMN mode	^tCSC	^tCAS		^tCAS		ns	

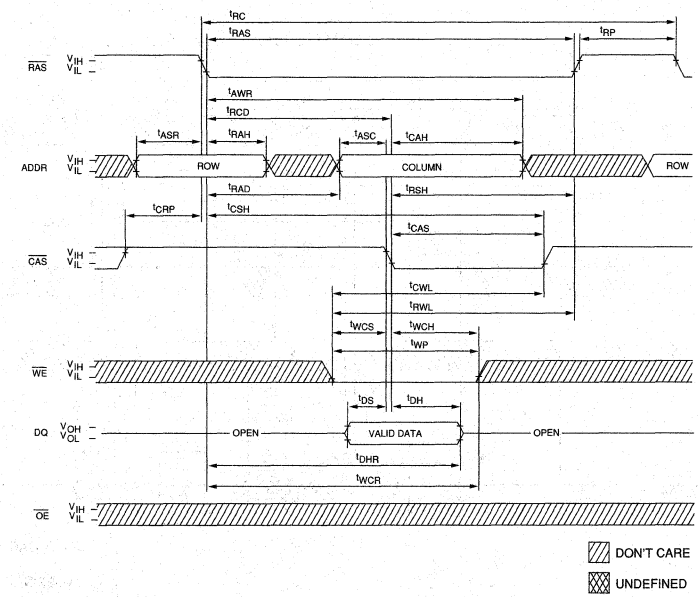
NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. V_{CC} = 5V ±10%, f = 1 MHz.
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is assured.
7. An initial pause of 100µs is required after power-up followed by eight $\overline{RAS}$ refresh cycles ($\overline{RAS}$-ONLY or CBR with $\overline{WE}$ HIGH) before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-up should be repeated any time the ^tREF refresh requirement is exceeded.
8. AC characteristics assume ^tT = 5ns.
9. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS}$ = V_{IH}, data output is High-Z.
12. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to 2 TTL gates and 100pF.
14. Assumes that $^tRCD < ^tRCD$ (MAX). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
15. Assumes that $^tRCD \geq ^tRCD$ (MAX).
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer, $\overline{CAS}$ must be pulsed HIGH for ^tCPN.
17. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (MAX) limit, then access time is controlled exclusively by ^tCAC.
18. Operation within the ^tRAD (MAX) limit ensures that ^tRAC (MIN) and ^tCAC (MIN) can be met. ^tRAD (MAX) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (MAX) limit, then access time is controlled exclusively by ^tAA.
19. Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
20. ^tOFF (MAX) defines the time at which the output achieves the open circuit condition, and is not referenced to V_{OH} or V_{OL}.
21. ^tWCS, ^tRWD, ^tAWD and ^tCWD are not restrictive operating parameters. ^tWCS applies to EARLY-WRITE cycles. ^tRWD, ^tAWD and ^tCWD apply to READ-MODIFY-WRITE cycles. If $^tWCS \geq ^tWCS$ (MIN), the cycle is an EARLY-WRITE cycle and the data output will remain an open circuit through out the entire cycle. If $^tRWD \geq ^tRWD$ (MIN), $^tAWD \geq ^tAWD$ (MIN) and $^tCWD \geq ^tCWD$ (MIN), the cycle is a READ-MODIFY-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of data out are indeterminate. $\overline{OE}$ held HIGH and $\overline{WE}$ taken LOW after $\overline{CAS}$ goes LOW results in a LATE-WRITE ($\overline{OE}$ controlled) cycle. ^tWCS, ^tRWD, ^tCWD and ^tAWD are not applicable in a LATE-WRITE cycle.
22. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY-WRITE cycles and $\overline{WE}$ leading edge in LATE-WRITE or READ-MODIFY-WRITE cycles.
23. If $\overline{OE}$ is tied permanently LOW, LATE-WRITE or READ-MODIFY-WRITE operations are not possible.
24. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW and $\overline{OE}$ = HIGH.
25. ^tWTS and ^tWTH are setup and hold specifications for the $\overline{WE}$ pin being held LOW to enable the JEDEC test mode (with CBR timing constraints). These two parameters are the inverts of ^tWRP and ^tWRH in the CBR refresh cycle.
26. LATE-WRITE and READ-MODIFY-WRITE cycles must have both ^tOD and ^tOEH met ($\overline{OE}$ HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. The DQs will provide the previously read data if $\overline{CAS}$ remains LOW and $\overline{OE}$ is taken back LOW after ^tOEH is met. If $\overline{CAS}$ goes HIGH prior to $\overline{OE}$ going back LOW, the DQs will remain open.
27. The DQs open during READ cycles once ^tOD or ^tOFF occur. If $\overline{CAS}$ goes HIGH first, $\overline{OE}$ becomes a "don't care." If $\overline{OE}$ goes HIGH and $\overline{CAS}$ stays LOW, $\overline{OE}$ is not a "don't care;" and the DQs will provide the previously read data if $\overline{OE}$ is taken back LOW (while $\overline{CAS}$ remains LOW).

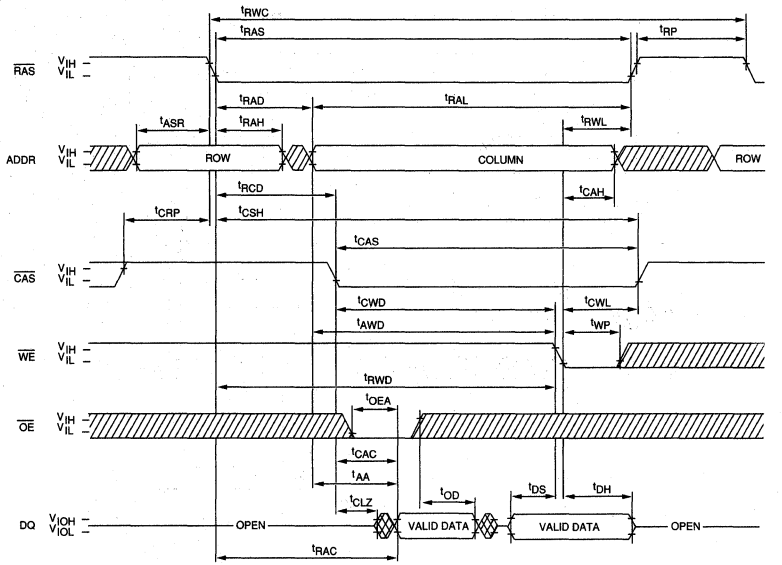
READ CYCLE



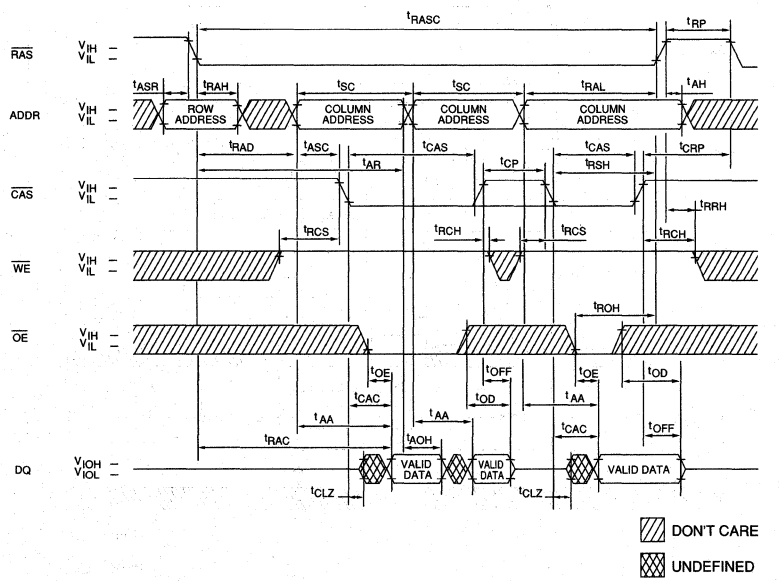
EARLY-WRITE CYCLE



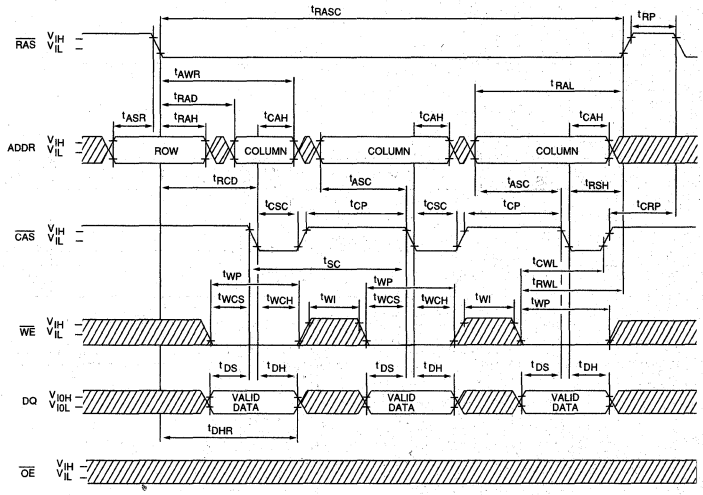
READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)



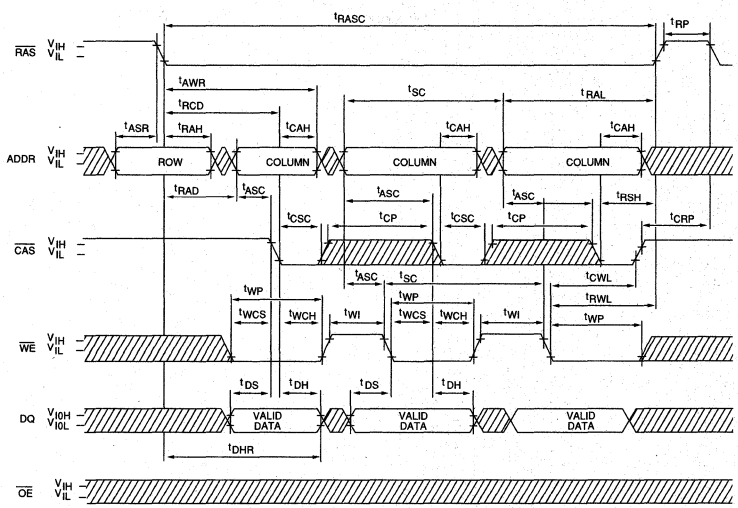
STATIC-COLUMN READ CYCLE



STATIC-COLUMN EARLY-WRITE CYCLE
(CAS Controlled)



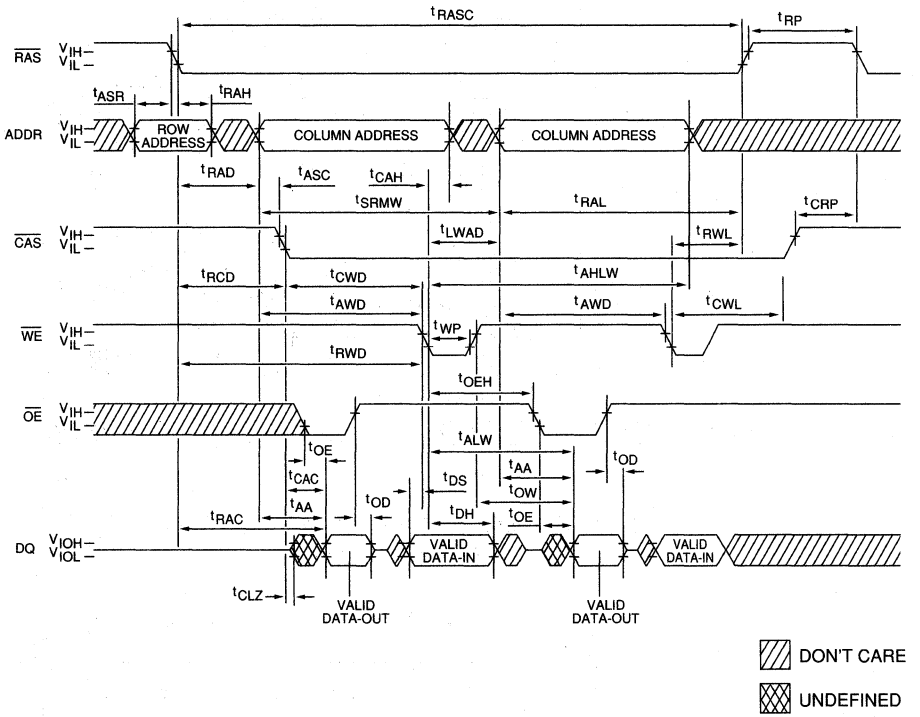
STATIC-COLUMN EARLY-WRITE CYCLE
(WE Controlled)



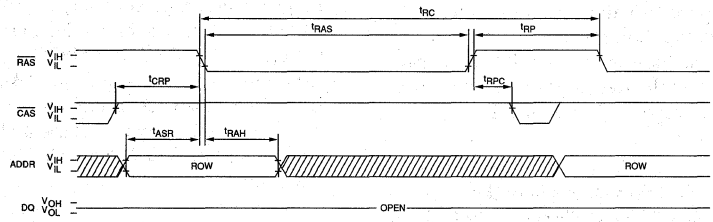
DON'T CARE

UNDEFINED

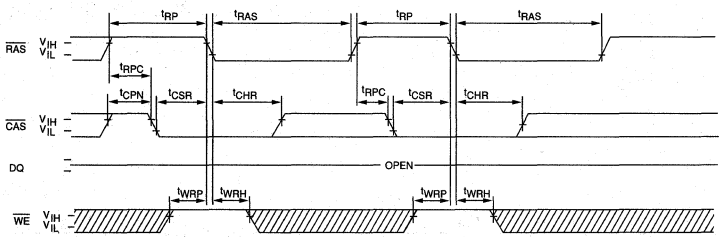
STATIC-COLUMN READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)



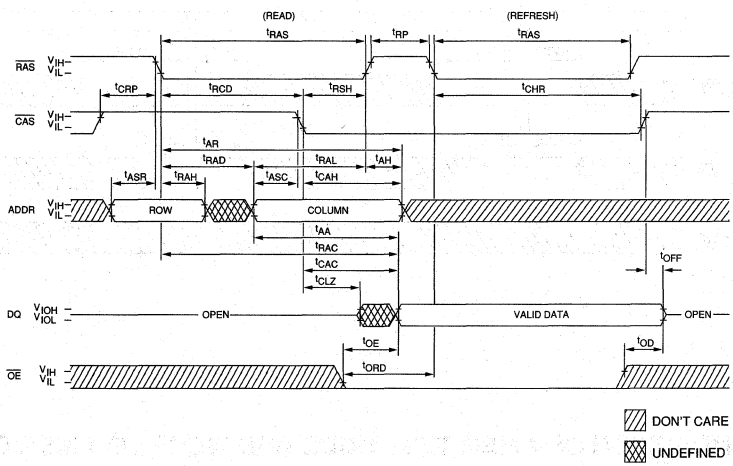
$\overline{\text{RAS}}$-ONLY REFRESH CYCLE
(ADDR = A0-A9; $\overline{\text{WE}}$ = DON'T CARE)



$\overline{\text{CAS}}$-BEFORE-$\overline{\text{RAS}}$ REFRESH CYCLE
(A0-A9, and $\overline{\text{OE}}$ = DON'T CARE)



HIDDEN REFRESH CYCLE [24]
($\overline{\text{WE}}$ = HIGH; $\overline{\text{OE}}$ = LOW)



4 MEG POWER-UP AND REFRESH CONSTRAINTS

The EIA/JEDEC 4 Meg DRAM introduces two potential incompatibilities compared to the previous generation 1 Meg DRAM. The incompatibilities involve refresh and power-up. Understanding these incompatibilities and providing for them will offer the designer and system user greater compatibility between the 1 Meg and 4 Meg.

REFRESH

The most commonly used refresh mode of the 1 Meg is the CBR ($\overline{CAS}$-BEFORE-$\overline{RAS}$) REFRESH cycle. The CBR for the 1 Meg specifies the $\overline{WE}$ pin as a "don't care." The 4 Meg, on the other hand, specifies the CBR REFRESH mode with the $\overline{WE}$ pin held at a voltage HIGH level.

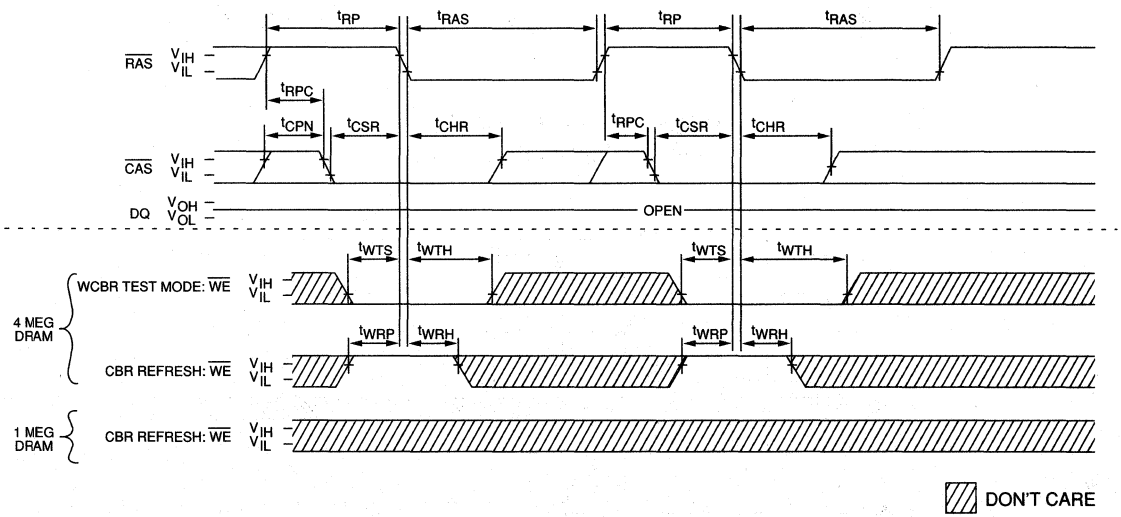
A CBR cycle with $\overline{WE}$ LOW will put the 4 Meg into the JEDEC specified test mode (WCBR).

POWER-UP

The 4 Meg JEDEC test mode constraint may introduce another problem. The 1 Meg POWER-UP cycle requires a 100µs delay followed by any eight $\overline{RAS}$ cycles. The 4 Meg POWER-UP is more restrictive in that eight $\overline{RAS}$-ONLY or CBR REFRESH ($\overline{WE}$ held HIGH) cycles must be used. The restriction is needed since the 4 Meg may power-up in the JEDEC specified test mode and must exit out of the test mode. The only way to exit the 4 Meg JEDEC test mode is with either a $\overline{RAS}$-ONLY or a CBR REFRESH cycle ($\overline{WE}$ held HIGH).

SUMMARY

1. The 1 Meg CBR REFRESH allows the $\overline{WE}$ pin to be "don't care" while the 4 Meg CBR requires $\overline{WE}$ to be HIGH.
2. The eight $\overline{RAS}$ wake-up cycles on the 1 Meg may be any valid $\overline{RAS}$ cycle while the 4 Meg may only use $\overline{RAS}$-ONLY or CBR REFRESH cycles ($\overline{WE}$ held HIGH).



COMPARISON OF 4 MEG TEST MODE AND WCBR TO 1 MEG CBR

DRAM

1 MEG x 4 DRAM

QUAD CAS PARITY, FAST PAGE MODE

FEATURES

- Four independent $\overline{CAS}$ controls, allowing individual manipulation to each of the four data Input/Output ports (DQ1 through DQ4).
- Offers a single chip solution to byte level parity for 36-bit words when using 1 Meg x 4 DRAMs for memory
- Emulates write-per-bit, at design-in level, with simplified timing constraints
- High-performance, CMOS silicon-gate process
- Single +5V ±10% power supply
- Low power, 3mW standby; 225mW active, typical
- All inputs, outputs and clocks are fully TTL compatible
- 1,024-cycle refresh in 16ms
- Refresh modes: $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$ (CBR) and HIDDEN

OPTIONS MARKING

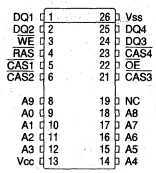
- Timing
  - 70ns access - 7
  - 80ns access - 8
  - 100ns access -10
- Packages
  - Plastic SOJ (300 mil) DJ

NOTE: Available in die form (commercial or military) or military ceramic packages. Please consult factory for die data sheets or refer to Micron's *Military Data Book*.

- Part Number Example: MT4C4004JDJ-7

PIN ASSIGNMENT (Top View)

24-Pin SOJ (Q-2)



GENERAL DESCRIPTION

The MT4C4004J is a randomly accessed solid-state memory containing 4,194,304 bits organized in a x4 configuration. This 1 Meg x 4 DRAM is unique in that each $\overline{CAS}$ ($\overline{CAS1}$ through $\overline{CAS4}$) controls its corresponding data I/O port in conjunction with $\overline{OE}$ (eg. $\overline{CAS1}$ controls DQ1 I/O port, $\overline{CAS2}$ controls DQ2, $\overline{CAS3}$ controls DQ3 and $\overline{CAS4}$ controls DQ4).

The best way to view the Quad $\overline{CAS}$ function is to imagine the $\overline{CAS}$ inputs going into an AND gate to obtain an internally generated $\overline{CAS}$ signal functioning in an identical manner to the single $\overline{CAS}$ input on a standard 1 Meg x 4 DRAM device. The key difference is each $\overline{CAS}$ controls its corresponding DQ tristate logic (in conjunction with $\overline{OE}$ and $\overline{WE}$) on the Quad CAS DRAM.

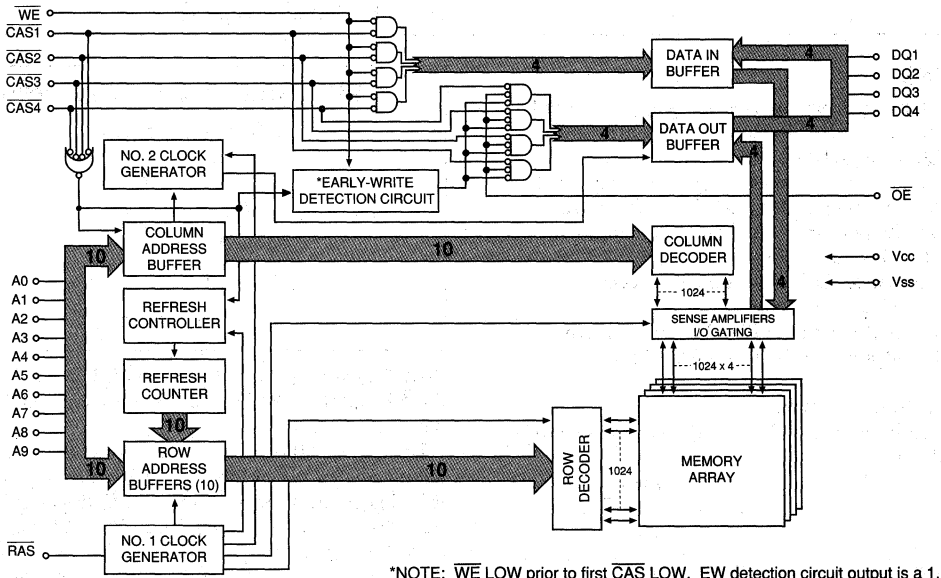
During READ or WRITE cycles, each bit is uniquely addressed through the 20 address bits, which are entered 10 bits (A0-A9) at a time. $\overline{RAS}$ is used to latch the first 10 bits, and the first $\overline{CAS}$ is used to latch the latter 10 bits. READ and WRITE cycles are selected with the $\overline{WE}$ input. A logic HIGH on $\overline{WE}$ dictates READ mode while a logic LOW on $\overline{WE}$ dictates WRITE mode.

During a WRITE cycle, data-in (Dx) is latched by the falling edge of $\overline{WE}$ or the first $\overline{CAS}$, whichever occurs last. If $\overline{WE}$ goes LOW prior to the first $\overline{CAS}$ going LOW, the output pin(s) remain open (High-Z) until the next $\overline{CAS}$ cycle. If $\overline{WE}$ goes LOW after data reaches the output buffer, data out (Q) is activated and retains the selected cell data until the trailing edge of its corresponding $\overline{CAS}$ occurs (regardless of $\overline{WE}$ or $\overline{RAS}$). This late $\overline{WE}$ pulse results in a READ-WRITE cycle ($\overline{OE}$ switching the device from a READ to a WRITE function). The four data inputs and four data outputs are routed through four pins using common I/O, with pin direction controlled by $\overline{WE}$ and $\overline{OE}$.

FAST PAGE MODE operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row address (A0-A9) defined page boundary. The FAST PAGE MODE cycle is always initiated with a row address strobed-in by $\overline{RAS}$ followed by a column address strobed-in by the first $\overline{CAS}$. $\overline{CAS}$ may be toggled-in by holding $\overline{RAS}$ LOW and strobing-in different column addresses, thus executing faster memory cycles. Returning $\overline{RAS}$ HIGH terminates the FAST PAGE MODE operation.

Returning $\overline{RAS}$ and all four $\overline{CAS}$ controls HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the $\overline{RAS}$ high time. Memory cell data is retained in its correct state by maintaining power and executing any $\overline{RAS}$ cycle (READ, WRITE, $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$ (CBR) or HIDDEN refresh) so that all 1,024 combinations of $\overline{RAS}$ addresses (A0-A9) are executed at least every 16ms, regardless of sequence. The CBR refresh cycle will invoke the internal refresh counter for automatic $\overline{RAS}$ addressing.

FUNCTIONAL BLOCK DIAGRAM
QUAD CAS



*NOTE: $\overline{WE}$ LOW prior to first $\overline{CAS}$ LOW, EW detection circuit output is a 1.
First $\overline{CAS}$ LOW while $\overline{WE}$ HIGH, EW detection circuit output is a 0,
($\overline{OE}$ will now determine I/O).

TRUTH TABLE

FUNCTION		$\overline{RAS}$	$\overline{CASx}$	$\overline{CASy}$	$\overline{WE}$	$\overline{OE}$	ADDRESSES ^tR	ADDRESSES ^tC	DQx (DQy always High-Z)
Standby		H	H→X	H→X	X	X	X	X	High-Z
READ		L	L	H	H	L	ROW	COL	Data Out
EARLY-WRITE		L	L	H	L	X	ROW	COL	Data In
READ-WRITE		L	L	H	H→L	L→H	ROW	COL	Data Out, Data In
FAST-PAGE-MODE	1st Cycle	L	H→L	H	H	L	ROW	COL	Data Out
READ	2nd Cycle	L	H→L	H	H	L	n/a	COL	Data Out
FAST-PAGE-MODE	1st Cycle	L	H→L	H	L	X	ROW	COL	Data In
EARLY-WRITE	2nd Cycle	L	H→L	H	L	X	n/a	COL	Data In
FAST-PAGE-MODE	1st Cycle	L	H→L	H	H→L	L→H	ROW	COL	Data Out, Data In
READ-WRITE	2nd Cycle	L	H→L	H	H→L	L→H	n/a	COL	Data Out, Data In
$\overline{RAS}$-ONLY REFRESH		L	H	H	X	X	ROW	n/a	High-Z
HIDDEN	READ	L→H→L	L	H	H	L	ROW	COL	Data Out
REFRESH	WRITE	L→H→L	L	H	L	X	ROW	COL	Data In
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH		H→L	L	H	X	X	X	X	High-Z

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to V_{SS} ..... -1V to +7V
Operating Temperature, T_A (Ambient) ..... 0°C to +70°C
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 3, 4, 6, 7) (V_{CC} = 5V ±10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.5	V	1
Input High (Logic 1) Voltage, All Inputs	V_{IH}	2.4	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, All Inputs	V_{IL}	-1.0	0.8	V	1
INPUT LEAKAGE CURRENT Any Input 0V ≤ V_{IN} ≤ 6.5V (All other pins not under test = 0V)	I_I	-2	2	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled, 0V ≤ V_{OUT} ≤ 5.5V)	I_{OZ}	-10	10	µA	
OUTPUT LEVELS Output High Voltage (I_{OUT} = -5mA)	V_{OH}	2.4		V	
Output Low Voltage (I_{OUT} = 4.2mA)	V_{OL}		0.4	V	

		MAX				
PARAMETER/CONDITION	SYMBOL	-7	-8	-10	UNITS	NOTES
STANDBY CURRENT: (TTL) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC1}	2.5	2.5	2.5	mA	
STANDBY CURRENT: (CMOS) ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} -0.2V)	I_{CC2}	1	1	1	mA	26
OPERATING CURRENT: Random READ/WRITE Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC= ^tRC (MIN))	I_{CC3}	100	90	80	mA	3, 4
OPERATING CURRENT: FAST PAGE MODE Average power supply current ($\overline{RAS}$ = V_{IL}; $\overline{CAS}$, Address Cycling: ^tPC= ^tPC (MIN))	I_{CC4}	70	60	50	mA	3, 4
REFRESH CURRENT: $\overline{RAS}$-ONLY Average power supply current ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}: ^tRC= ^tRC (MIN))	I_{CC5}	100	90	80	mA	3
REFRESH CURRENT: $\overline{CAS}$-BEFORE-$\overline{RAS}$ Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC= ^tRC (MIN))	I_{CC6}	100	90	80	mA	3, 5

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A9	C_{I1}		5	pF	2
Input Capacitance: $\overline{RAS}$, $\overline{CAS}$1-4, $\overline{WE}$, $\overline{OE}$	C_{I2}		7	pF	2
Input/Output Capacitance: DQ	C_{IO}		7	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (V_{CC} = 5V ±10%)

AC CHARACTERISTICS		-7		-8		-10			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	^tRC	130		150		180		ns	
READ-WRITE cycle time	^tRWC	185		205		220		ns	
FAST-PAGE-MODE READ or WRITE cycle time	^tPC	40		45		55		ns	31
FAST-PAGE-MODE READ-WRITE cycle time	^tPRWC	95		100		115		ns	31
Access time from $\overline{RAS}$	^tRAC		70		80		100	ns	14
Access time from $\overline{CAS}$	^tCAC		20		20		25	ns	15, 29
Output Enable	^tOE		20		20		25	ns	33
Access time from column address	^tAA		35		40		50	ns	
Access time from $\overline{CAS}$ precharge	^tCPA		40		45		50	ns	29
$\overline{RAS}$ pulse width	^tRAS	70	100,000	80	100,000	100	100,000	ns	
$\overline{RAS}$ pulse width (FAST PAGE MODE)	^tRASP	70	100,000	80	100,000	100	100,000	ns	
$\overline{RAS}$ hold time	^tRSH	20		20		25		ns	27
$\overline{RAS}$ precharge time	^tRP	50		60		70		ns	
$\overline{CAS}$ pulse width	^tCAS	20	100,000	20	100,000	25	100,000	ns	34
$\overline{CAS}$ hold time	^tCSH	70		80		100		ns	28
$\overline{CAS}$ precharge time	^tCPN	10		10		15		ns	16, 32
$\overline{CAS}$ precharge time (FAST PAGE MODE)	^tCP	10		10		10		ns	32
$\overline{RAS}$ to $\overline{CAS}$ delay time	^tRCD	20	50	20	60	25	75	ns	17, 27
$\overline{CAS}$ to $\overline{RAS}$ precharge time	^tCRP	5		5		5		ns	28
Row address setup time	^tASR	0		0		0		ns	
Row address hold time	^tRAH	10		10		15		ns	
$\overline{RAS}$ to column address delay time	^tRAD	15	35	15	40	20	50	ns	18
Column address setup time	^tASC	0		0		0		ns	27
Column address hold time	^tCAH	15		15		20		ns	27
Column address hold time (referenced to $\overline{RAS}$)	^tAR	55		60		70		ns	
Column address to $\overline{RAS}$ lead time	^tRAL	35		40		50		ns	
Read command setup time	^tRCS	0		0		0		ns	27
Read command hold time (referenced to $\overline{CAS}$)	^tRCH	0		0		0		ns	19, 28
Read command hold time (referenced to $\overline{RAS}$)	^tRRH	0		0		0		ns	19
$\overline{CAS}$ to output in Low-Z	^tCLZ	0		0		0		ns	29

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (V_{CC} = 5V ±10%)

AC CHARACTERISTICS		-7		-8		-10			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Output buffer turn-off delay	^tOFF	0	20	0	20	0	20	ns	20, 29, 38
Output disable	^tOD		20		20		20	ns	34, 38
$\overline{WE}$ command setup time	^tWCS	0		0		0		ns	21, 27
Write command hold time	^tWCH	15		15		20		ns	36
Write command hold time (referenced to $\overline{RAS}$)	^tWCR	55		60		75		ns	
Write command pulse width	^tWP	15		15		20		ns	
Write command to $\overline{RAS}$ lead time	^tRWL	20		20		25		ns	
Write command to $\overline{CAS}$ lead time	^tCWL	20		20		25		ns	28
Data-in setup time	^tDS	0		0		0		ns	22, 29
Data-in hold time	^tDH	15		15		20		ns	22, 29
Data-in hold time (referenced to $\overline{RAS}$)	^tDHR	55		60		75		ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	^tRWD	100		110		130		ns	21
Column address to $\overline{WE}$ delay time	^tAWD	65		70		80		ns	21
$\overline{CAS}$ to $\overline{WE}$ delay time	^tCWD	50		55		60		ns	21, 27
Transition time (rise or fall)	^tT	3	50	3	50	3	50	ns	9, 10
Refresh period (512 cycles)	^tREF		16		16		16	ms	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	^tRPC	0		0		0		ns	
$\overline{CAS}$ setup time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tCSR	10		10		10		ns	5, 27
$\overline{CAS}$ hold time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tCHR	15		15		15		ns	5, 28
Last $\overline{CAS}$ going LOW to first $\overline{CAS}$ to return HIGH	^tCLCH	10		10		10		ns	30
$\overline{OE}$ hold time from $\overline{WE}$ during READ-MODIFY-WRITE cycle	^tOEH	20		20		20		ns	37
$\overline{OE}$ setup prior to $\overline{RAS}$ during HIDDEN refresh cycle	^tORD	0		0		0		ns	

NOTES

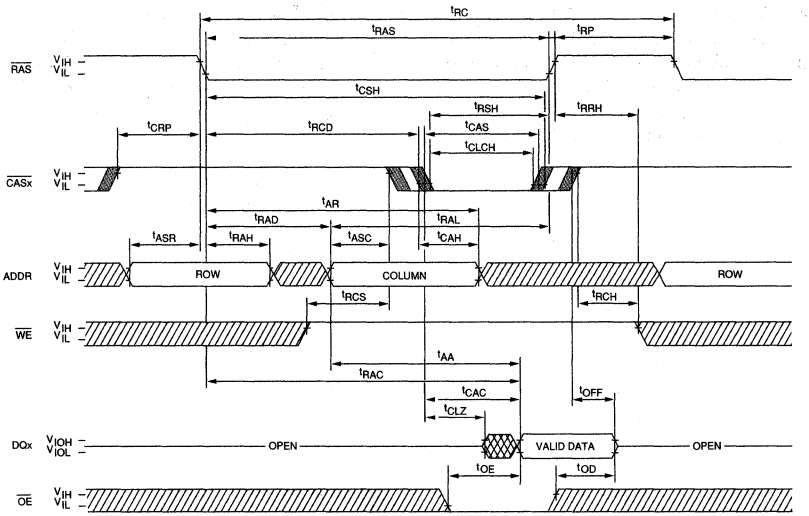
1. All voltages referenced to V_{SS}.
2. This parameter is sampled. V_{CC} = 5V ±10%, f = 1 MHz.
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is assured.
7. An initial 100µs pause is required after power-up followed by eight $\overline{RAS}$ refresh cycles ($\overline{RAS}$-ONLY or CBR) before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-up should be repeated any time the ^{t}REF refresh requirement is exceeded.
8. AC characteristics assume ^{t}T = 5ns.
9. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS}$x = V_{IH}, data output (Qx) is High-Z.
12. If $\overline{CAS}$x = V_{IL}, Qx may contain data from the last valid READ cycle.
13. Measured with a load equivalent to 2 TTL gates and 100pF.
14. Assumes that ^{t}RCD < ^{t}RCD (MAX). If ^{t}RCD is greater than the maximum recommended value shown in this table, ^{t}RAC will increase by the amount that ^{t}RCD exceeds the value shown.
15. Assumes that ^{t}RCD ≥ ^{t}RCD (MAX).
16. If at least one $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the Q buffer, all four $\overline{CAS}$ controls must be pulsed HIGH for ^{t}CPN.
17. Operation within the ^{t}RCD (MAX) limit ensures that ^{t}RAC (MAX) can be met. ^{t}RCD (MAX) is specified as a reference point only; if ^{t}RCD is greater than the specified ^{t}RCD (MAX) limit, then access time is controlled exclusively by ^{t}CAC.
18. Operation within the ^{t}RAD (MAX) limit ensures that ^{t}RAC (MIN) and ^{t}CAC (MIN) can be met. ^{t}RAD (MAX) is specified as a reference point only; if ^{t}RAD is greater than the specified ^{t}RAD (MAX) limit, then access time is controlled exclusively by ^{t}AA.
19. Either ^{t}RCH or ^{t}RRH must be satisfied for a READ cycle.
20. ^{t}OFF (MAX) defines the time at which the output achieves the open circuit condition, and is not referenced to V_{OH} or V_{OL}.
21. ^{t}WCS, ^{t}RWD, ^{t}AWD and ^{t}CWD are restrictive operating parameters in EARLY-WRITE and READ-WRITE cycles only. If ^{t}WCS ≥ ^{t}WCS (MIN), the cycle is an EARLY-WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If ^{t}RWD ≥ ^{t}RWD (MIN), ^{t}AWD ≥ ^{t}AWD (MIN) and ^{t}CWD ≥ ^{t}CWD (MIN), the cycle is a READ-WRITE cycle, and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of data out are indeterminate. $\overline{OE}$ held HIGH and $\overline{WE}$ taken LOW after $\overline{CAS}$ goes LOW results in a LATE-WRITE ($\overline{OE}$ controlled) cycle (at access time and until $\overline{CAS}$ or $\overline{OE}$ goes back to V_{IH}).
22. These parameters are referenced to $\overline{CAS}$x leading edge in EARLY-WRITE cycles and $\overline{WE}$ leading edge in LATE-WRITE or READ-WRITE cycles.
23. If $\overline{OE}$ is tied permanently LOW, READ-WRITE or READ-MODIFY-WRITE operations are not possible.
24. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW and $\overline{OE}$ = HIGH.
25. One to three $\overline{CAS}$ controls may be HIGH throughout any given $\overline{CAS}$ cycle, even though the timing waveforms show all $\overline{CAS}$ controls going LOW. If any one goes LOW, it must meet all the timing requirements listed, or the data for that I/O buffer may be invalid. At least one of the four $\overline{CAS}$ controls must be LOW for a valid $\overline{CAS}$ cycle to occur.
26. All other inputs at Vcc -0.2V.
27. The first $\overline{CAS}$x edge to transition LOW.
28. The last $\overline{CAS}$x edge to transition HIGH.
29. Output parameters (DQx) are referenced to corresponding $\overline{CAS}$x input; DQ1 by $\overline{CAS1}$, DQ2 by $\overline{CAS2}$, etc.
30. Last falling $\overline{CAS}$x edge to first rising $\overline{CAS}$x edge.
31. Last rising $\overline{CAS}$x edge to next cycle's last rising $\overline{CAS}$x edge.
32. Last rising $\overline{CAS}$x edge to first falling $\overline{CAS}$x edge.
33. First DQx controlled by the first $\overline{CAS}$x to go LOW.
34. Last DQx controlled by the last $\overline{CAS}$x to go HIGH.
35. Each $\overline{CAS}$x must meet minimum pulse width.
36. Last $\overline{CAS}$x to go LOW.

NOTES (continued)

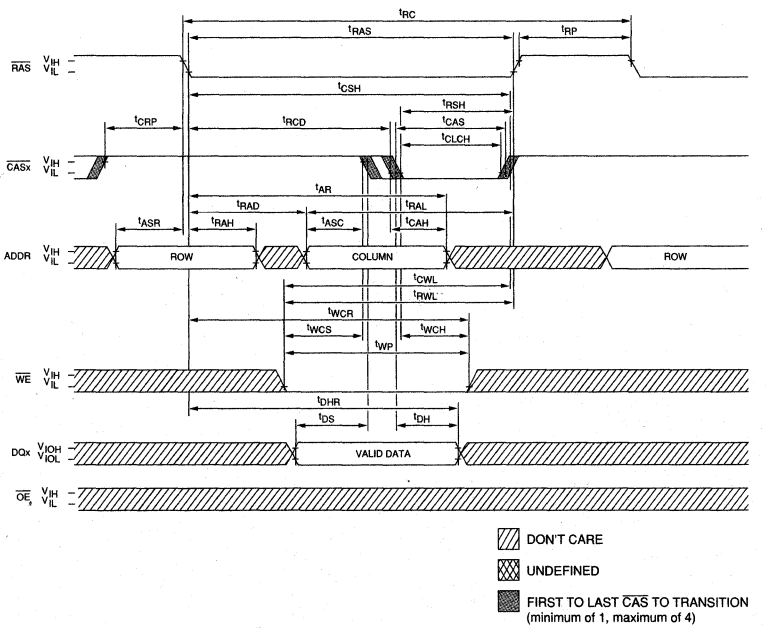
37. LATE-WRITE and READ-MODIFY-WRITE cycles must meet both ^{t}OD and ^{t}OEH ($\overline{OE}$ HIGH during WRITE cycle) to ensure that the output buffers will be open during the WRITE cycle. The DQs will provide the previously read data if $\overline{CAS}$ remains LOW and $\overline{OE}$ is taken back LOW after ^{t}OEH is met. If the last $\overline{CAS}$x goes HIGH prior to $\overline{OE}$ going back LOW, the DQs will remain open.

38. The DQs will open during READ cycles once ^{t}OD or ^{t}OFF occur. If the last $\overline{CAS}$x goes HIGH first, $\overline{OE}$ becomes a "don't care." If $\overline{OE}$ goes HIGH and $\overline{CAS}$x stays LOW, $\overline{OE}$ is not a "don't care;" and the DQs will provide the previously read data if $\overline{OE}$ is taken back LOW (while $\overline{CAS}$x remains LOW).

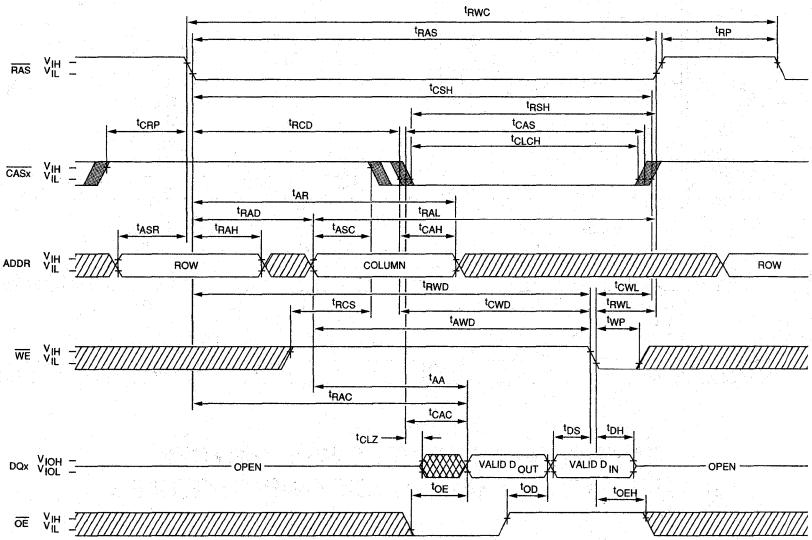
READ CYCLE



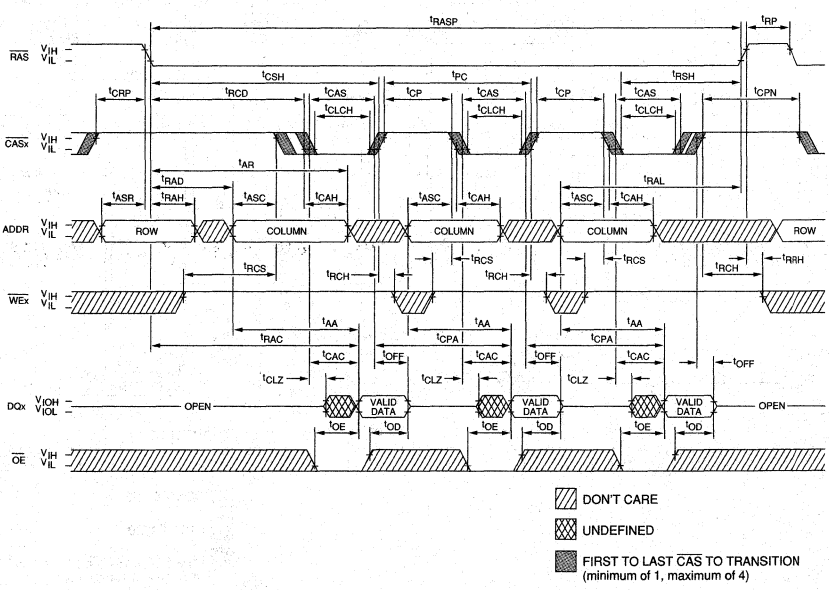
EARLY-WRITE CYCLE



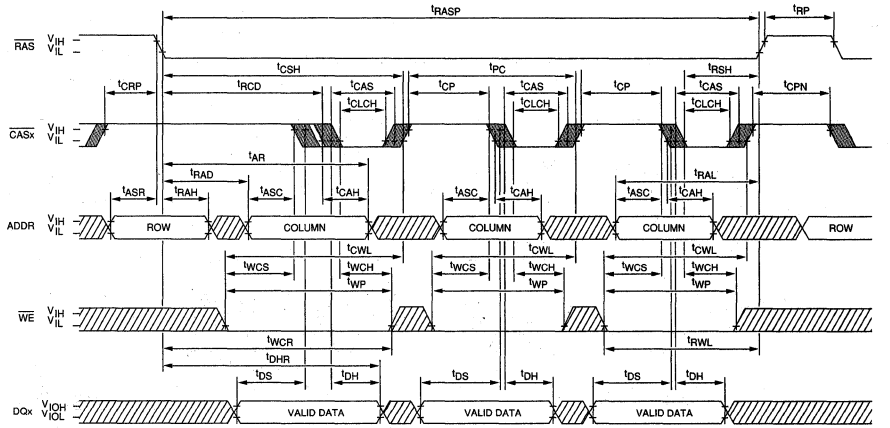
READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)



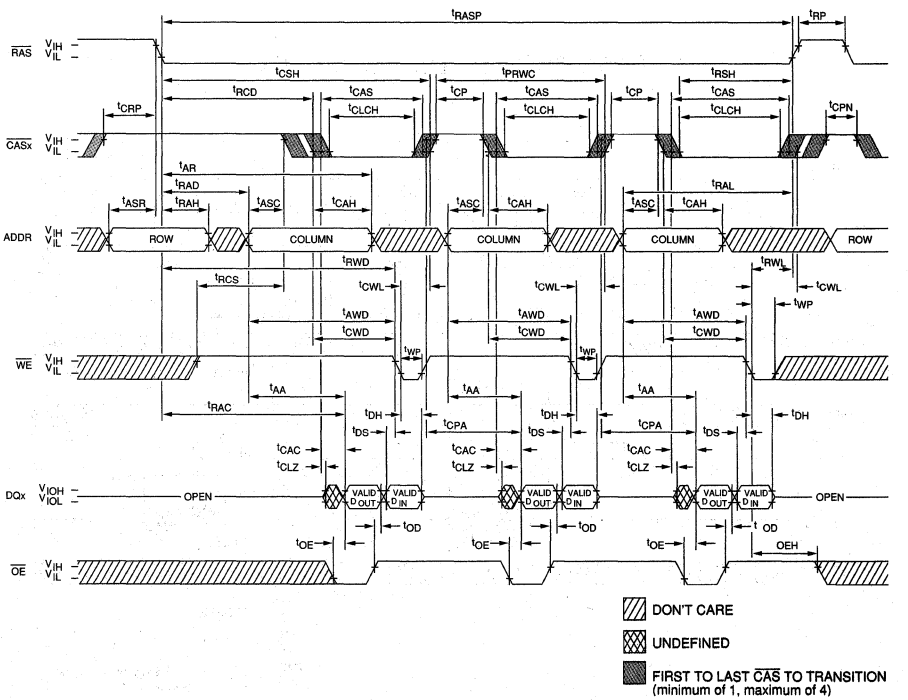
FAST-PAGE-MODE READ CYCLE



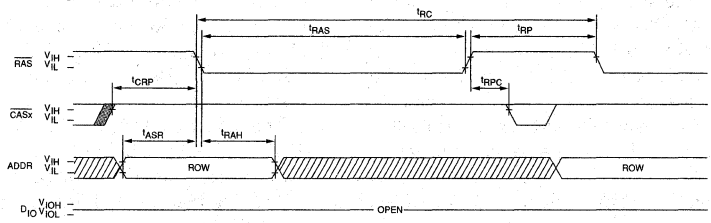
FAST-PAGE-MODE EARLY-WRITE CYCLE



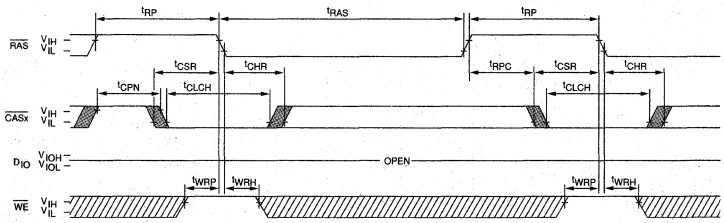
FAST-PAGE-MODE READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)



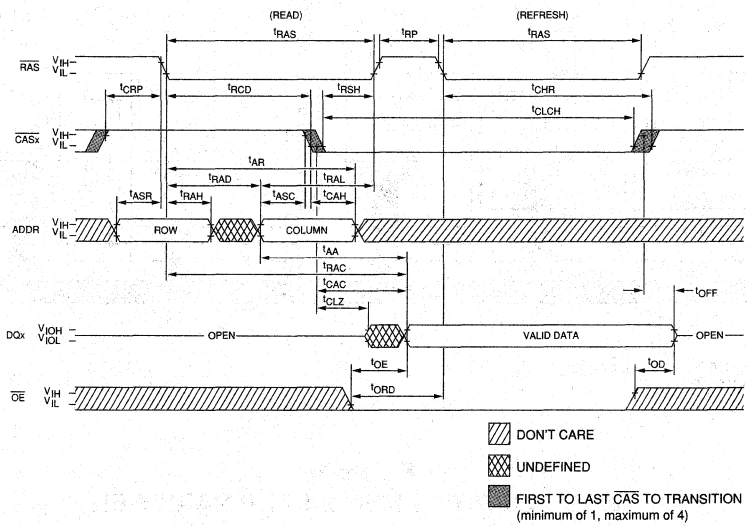
RAS-ONLY REFRESH CYCLE
(ADDR = A0-A9; WE and OE = DON'T CARE)



CAS-BEFORE-RAS REFRESH CYCLE
(A0-A9, OE = DON'T CARE)



HIDDEN REFRESH CYCLE [24]
(WE = HIGH, OE = LOW)

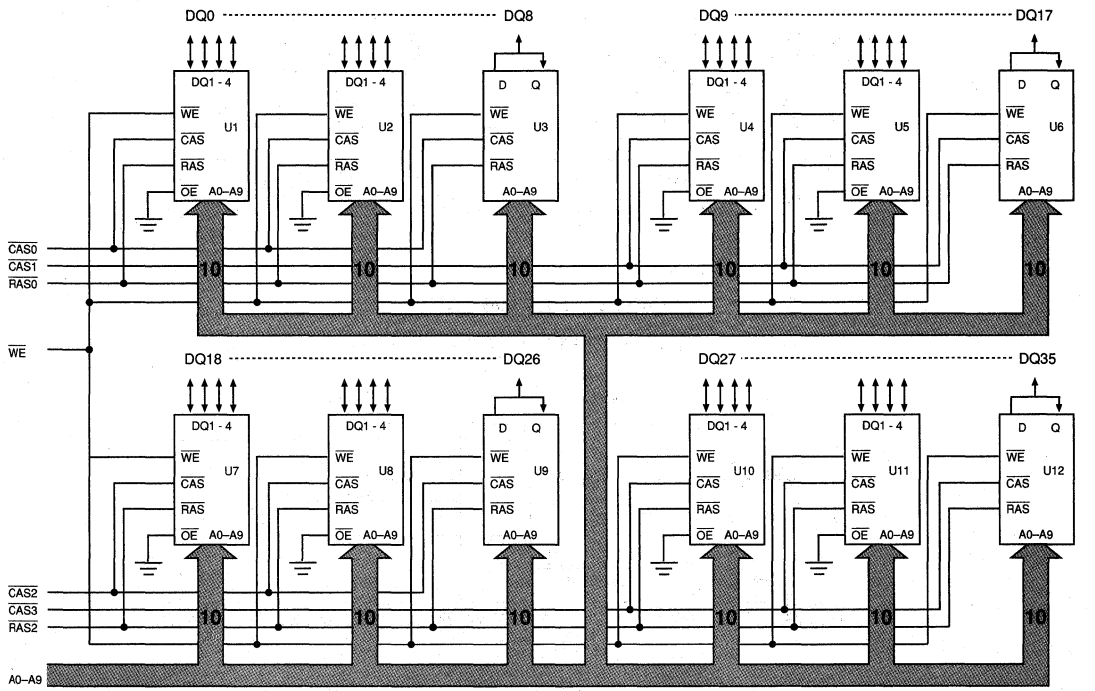


QUAD CAS MODULE UPGRADE

The MT4C4004J (Quad CAS DRAM) was developed to supersede the 1 Meg DRAMs used in the current 1 Meg and 2 Meg x 36 DRAM modules and to add leading-edge CMOS performance. The MT4C4004J is a 1 Meg x 4 CMOS FAST-PAGE-MODE DRAM with four $\overline{CAS}$ input controls. The four individual $\overline{CAS}$ inputs allow each I/O buffer (DQ) to be separately controlled, just as if there were four separate 1 Meg x 1 DRAMs. Most 1 Meg x 1 DRAMs use older CMOS technology and do not have the access speeds of the newer CMOS 4 Meg (1 Meg x 4).

The MT4C4004J reduces chip count on x36 modules; improving reliability, reducing power consumption and lowering cost. In the 1 Meg x 36, four 1 Meg x 1 DRAMs are replaced by either one or two Quad CAS DRAMs, depending on whether $\overline{RAS0}$ and $\overline{RAS1}$ must be separate or connected. In the 2 Meg x 36, eight 1 Meg x 1 DRAMs are replaced by either two or four Quad CAS DRAMs, depending on whether $\overline{RAS0}$, $\overline{RAS1}$, $\overline{RAS2}$, and $\overline{RAS3}$ must be split or connected.

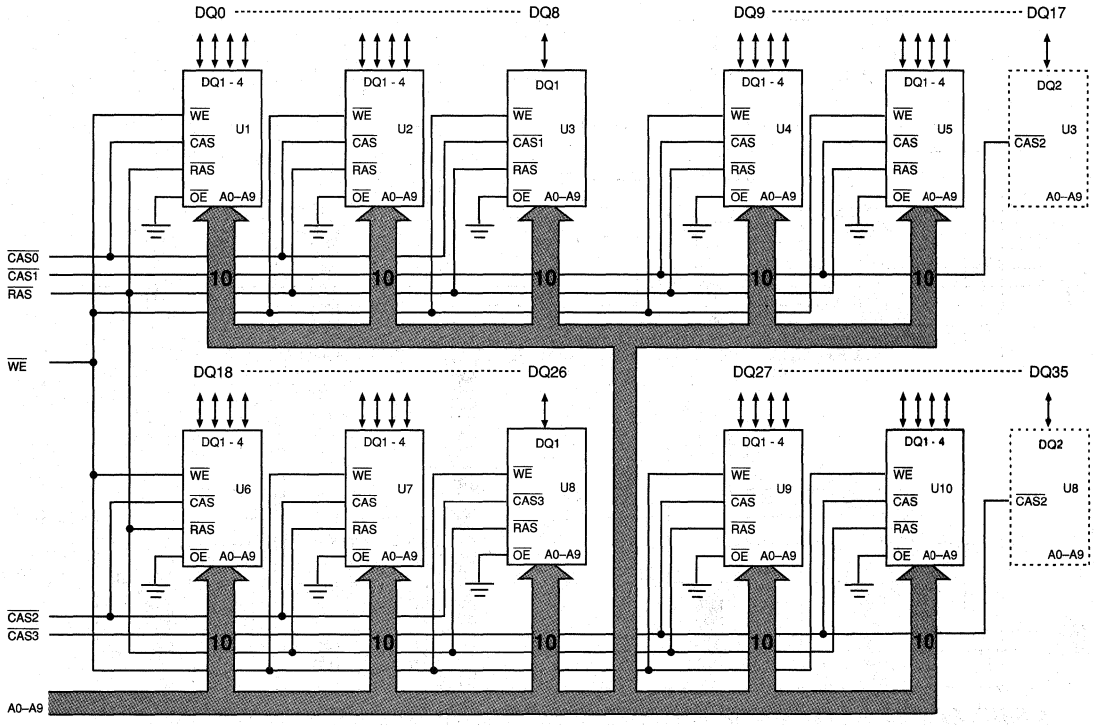
The current 1 Meg x 36 DRAM Module is shown with 256K x 1 DRAMs in Figure 1 below. Figures 2 and 3 show how the same module will be realized with the Quad CAS DRAM for both the split $\overline{RAS}$ (Figure 2) and the common $\overline{RAS}$ (Figure 3) modules.



U1, U2, U4, U5, U7, U8, U10, U11 = MT4C4001JDJ
U3, U6, U9, U12 = MT4C1024DJ

Figure 1
1 MEG x 36 WITH 1 MEG x 1 FOR PARITY BIT

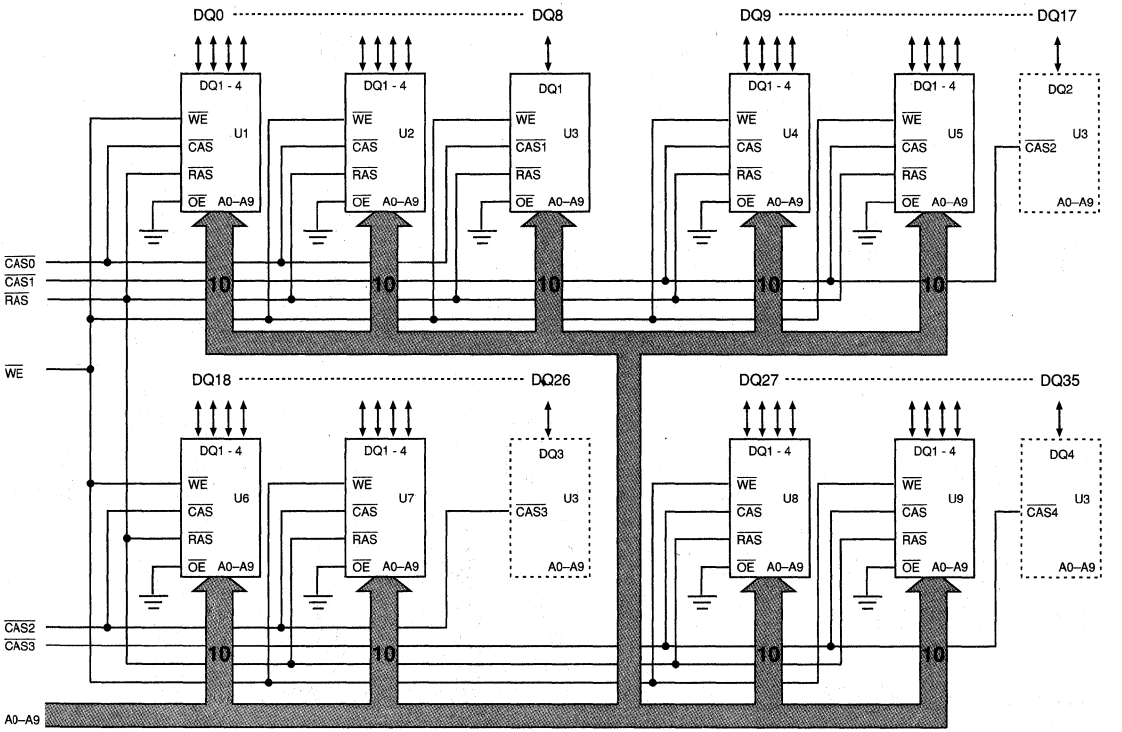
QUAD CAS ENHANCED x36 MODULES



U1, U2, U4, U5, U6, U7, U8, U9 = MT4C4001JDJ
U3 = MT4C4004JDJ

Figure 2
1 MEG x 36 WITH QUAD $\overline{CAS}$ FOR PARITY BIT AND SPLIT $\overline{RAS}$ CONTROL

QUAD CAS ENHANCED x36 MODULES



U1, U2, U4-U9 = MT4C4001JDJ
U3 = MT4C4004JDJ

Figure 3
1 MEG x 36 WITH QUAD $\overline{CAS}$ FOR PARITY BIT AND COMMON $\overline{RAS}$ CONTROL

DRAM

4 MEG x 4 DRAM

5.0V FAST PAGE MODE

FEATURES

- Industry standard x4 pinout, timing, functions and packages
- High-performance, CMOS silicon-gate process
- Single power supply : +5V ±10%
- Low power, 3mW standby; 325mW active, typical (A1)
- All inputs, outputs and clocks are fully TTL compatible
- Refresh modes: $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$ (CBR) and HIDDEN
- 2,048-cycle refresh distributed across 32ms or 4,096-cycle refresh distributed across 64ms

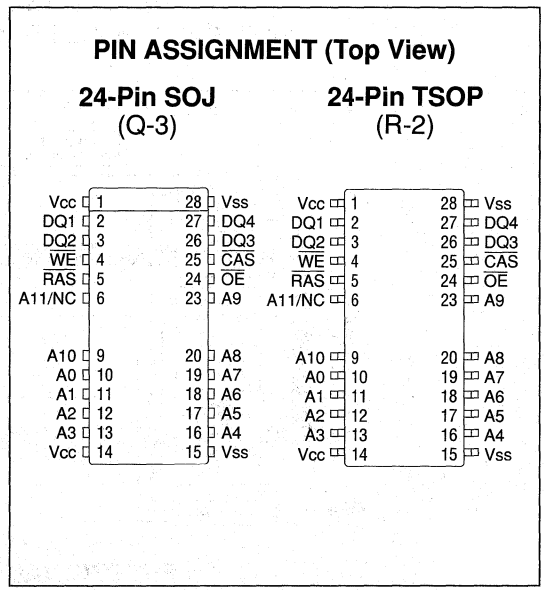
OPTIONS MARKING

- Timing
  - 60ns access - 6
  - 70ns access - 7
  - 80ns access - 8
- Packages
  - Plastic SOJ (400 mil) DJ
  - Plastic TSOP (400 mil) TG

NOTE: Available in die form (commercial or military) or military ceramic packages. Please consult factory for die data sheets or refer to Micron's *Military Data Book.*

- Refresh Period
  - 2,048 cycles @ 32ms, 11 Row Addresses MT4C4M4B1
  - 4,096 cycles @ 64ms, 12 Row Addresses MT4C4M4A1
- Operating Temperature, T_A
  - Commercial (0°C to +70°C) None

PIN ASSIGNMENT (Top View)



GENERAL DESCRIPTION

The MT4C4M4A1/B1 are randomly accessed solid-state memories containing 16,777,216 bits organized in a x4 configuration. The MT4C4M4A1 and MT4C4M4B1 are the same DRAM versions except that the MT4C4M4B1 has 2,048 cycle refresh instead of 4,096 cycle refresh. All further references made for the MT4C4M4A1 also apply to the MT4C4M4B1 unless specifically stated otherwise. For a device with 2,048 cycle refresh, $\overline{RAS}$ is used to latch the first 11 bits and $\overline{CAS}$ the latter 11 bits. For a device with 4,096 cycle refresh, $\overline{RAS}$ is used to latch the first 12 bits and $\overline{CAS}$ the latter 10 bits (A10 and A11 are "don't care" bits). READ and WRITE cycles are selected with the $\overline{WE}$ input. A logic HIGH on $\overline{WE}$ dictates READ mode while a logic LOW on $\overline{WE}$ dictates WRITE mode. During a WRITE cycle, data in (D) is latched by the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. If $\overline{WE}$ goes LOW prior to $\overline{CAS}$ going LOW, the output pins remain open (High- Z) until the next $\overline{CAS}$ cycle. If $\overline{WE}$ goes LOW after data reaches the output pins, data out (Q) is activated and retains the selected cell data as long as $\overline{CAS}$ remains LOW (regardless of $\overline{WE}$ or $\overline{RAS}$). This late $\overline{WE}$ pulse results in a READ-WRITE cycle. The four data inputs and the four data outputs are routed through four pins using common I/O, and pin direction is controlled by $\overline{WE}$ and $\overline{OE}$.

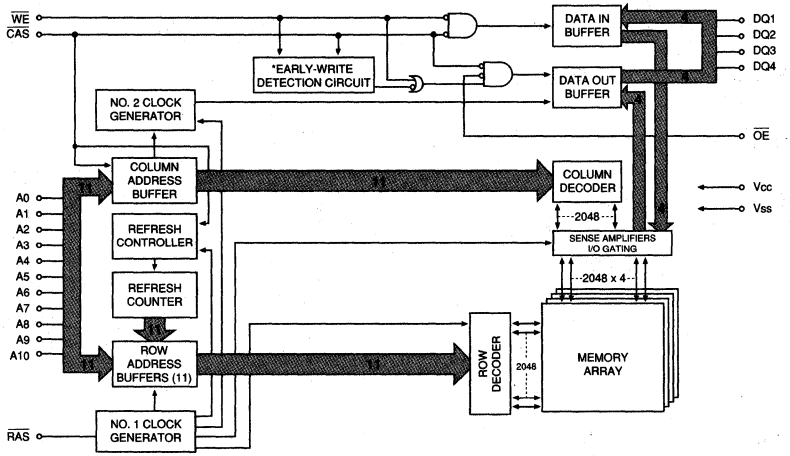
FAST PAGE MODE operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row address (A0 -A9/10) defined page boundary. The FAST PAGE MODE cycle is always initiated with a row address strobed-in by $\overline{RAS}$ followed by a column address strobed-in by $\overline{CAS}$. $\overline{CAS}$ may be toggled-in by holding $\overline{RAS}$ LOW and strobing-in different column addresses, thus executing faster memory cycles. Returning $\overline{RAS}$ HIGH terminates the FAST PAGE MODE operation.

Returning $\overline{RAS}$ and $\overline{CAS}$ HIGH terminates a memory cycle and decreases chip current to a reduced standby level.

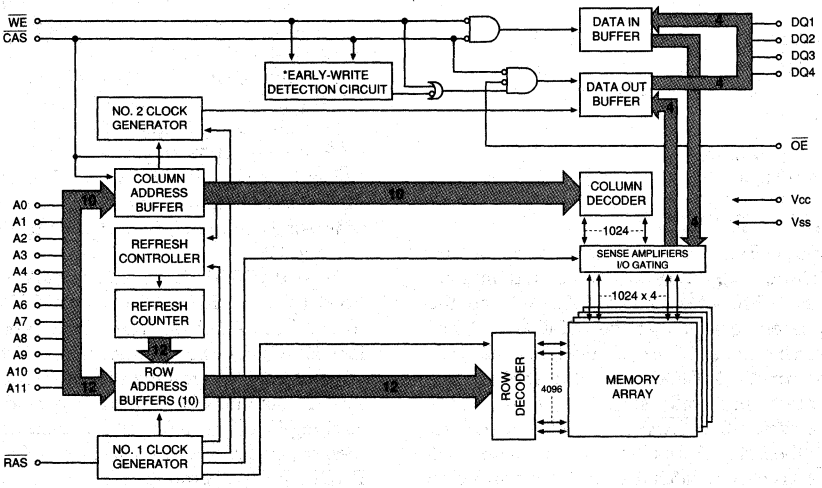
Also, the chip is preconditioned for the next cycle during the $\overline{RAS}$ high time. Memory cell data is retained in its correct state by maintaining power and executing any $\overline{RAS}$ cycle (READ, WRITE, $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$ (CBR) or HIDDEN refresh) so that all 2,048/4,096 combinations of $\overline{RAS}$ addresses (A0-A10/A11) are executed at least every 32ms/64ms, regardless of sequence. The CBR refresh cycle will invoke the refresh counter for automatic $\overline{RAS}$ addressing.

If CBR refresh is used, the number of cycles is a "don't care."

FUNCTIONAL BLOCK DIAGRAM
FAST PAGE MODE MT4C4M4B1 (11 Row Addresses)



FUNCTIONAL BLOCK DIAGRAM
FAST PAGE MODE MT4C4M4A1 (12 Row Addresses)



*NOTE: $\overline{WE}$ LOW prior to $\overline{CAS}$ LOW, EW detection circuit output is a HIGH (EARLY-WRITE)
$\overline{CAS}$ LOW prior to $\overline{WE}$ LOW, EW detection circuit output is a LOW (LATE-WRITE)

TRUTH TABLE

FUNCTION		RAS	CAS	WE	OE	ADDRESSES		DATA IN/OUT
						^tR	^tC	DQ1-DQ4
Standby		H	H→X	X	X	X	X	High-Z
READ		L	L	H	L	ROW	COL	Data Out
EARLY-WRITE		L	L	L	X	ROW	COL	Data In
READ-WRITE		L	L	H→L	L→H	ROW	COL	Data Out, Data In
FAST-PAGE-MODE	1st Cycle	L	H→L	H	L	ROW	COL	Data Out
READ	2nd Cycle	L	H→L	H	L	n/a	COL	Data Out
FAST-PAGE-MODE	1st Cycle	L	H→L	L	X	ROW	COL	Data In
EARLY-WRITE	2nd Cycle	L	H→L	L	X	n/a	COL	Data In
FAST-PAGE-MODE	1st Cycle	L	H→L	H→L	L→H	ROW	COL	Data Out, Data In
READ-WRITE	2nd Cycle	L	H→L	H→L	L→H	n/a	COL	Data Out, Data In
RAS-ONLY REFRESH		L	H	X	X	ROW	n/a	High-Z
HIDDEN	READ	L→H→L	L	H	L	ROW	COL	Data Out
REFRESH	WRITE	L→H→L	L	L	X	ROW	COL	Data In
CAS-BEFORE-RAS REFRESH		H→L	L	H	X	X	X	High-Z

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to V_{SS} (5.0V) ..-1.0V to +7.0V
Operating Temperature, T_A (Ambient) .....0°C to +70°C
Storage Temperature (Plastic) .....-55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 3, 4, 6, 7) (V_{CC} = 5V ±10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.5	V	1
Input High (Logic 1) Voltage, All Inputs	V_{IH}	2.4	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, All Inputs	V_{IL}	-1.0	0.8	V	1
INPUT LEAKAGE CURRENT Any Input 0V ≤ V_{IN} ≤ 6.5V (All other pins not under test = 0V)	I_I	-2	2	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled, 0V ≤ V_{OUT} ≤ 5.5V)	I_{OZ}	-10	10	µA	
OUTPUT LEVELS Output High Voltage (I_{OUT} = -5mA)	V_{OH}	2.4		V	
Output Low Voltage (I_{OUT} = 4.2mA)	V_{OL}		0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 3, 4, 6, 7) (V_{CC} = 5V ±10%), 4,096 cycle refresh

PARAMETER/CONDITION	SYMBOL	MAX -6	MAX -7	MAX -8	UNITS	NOTES
STANDBY CURRENT: (TTL) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC1}	2	2	2	mA	
STANDBY CURRENT: (CMOS) ($\overline{RAS}$ = $\overline{CAS}$ = Other Inputs = V_{CC} -0.2V)	I_{CC2}	1	1	1	mA	
OPERATING CURRENT: Random READ/WRITE Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC (MIN))	I_{CC3}	90	80	70	mA	3, 4, 28
OPERATING CURRENT: FAST PAGE MODE Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: ^tPC = ^tPC (MIN))	I_{CC4}	70	60	50	mA	3, 4, 28
REFRESH CURRENT: $\overline{RAS}$-ONLY Average power supply current ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}: ^tRC = ^tRC (MIN))	I_{CC5}	90	80	70	mA	3, 28
REFRESH CURRENT: $\overline{CAS}$-BEFORE-$\overline{RAS}$ Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC (MIN))	I_{CC6}	90	80	70	mA	3, 5, 28

(Notes: 1, 3, 4, 6, 7) (V_{CC} = 5V ±10%), 2,048 cycle refresh

PARAMETER/CONDITION	SYMBOL	MAX -6	MAX -7	MAX -8	UNITS	NOTES
STANDBY CURRENT: (TTL) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC1}	2	2	2	mA	
STANDBY CURRENT: (CMOS) ($\overline{RAS}$ = $\overline{CAS}$ = Other Inputs = V_{CC} -0.2V)	I_{CC2}	1	1	1	mA	
OPERATING CURRENT: Random READ/WRITE Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC (MIN))	I_{CC3}	120	110	100	mA	3, 4, 27
OPERATING CURRENT: FAST PAGE MODE Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: ^tPC = ^tPC (MIN))	I_{CC4}	90	80	70	mA	3, 4, 27
REFRESH CURRENT: $\overline{RAS}$-ONLY Average power supply current ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}: ^tRC = ^tRC (MIN))	I_{CC5}	120	110	100	mA	3, 27
REFRESH CURRENT: $\overline{CAS}$-BEFORE-$\overline{RAS}$ Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC (MIN))	I_{CC6}	120	110	100	mA	3, 5, 27

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A11	C_{I1}		5	pF	2
Input Capacitance: $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$	C_{I2}		7	pF	2
Input/Output Capacitance: DQ	C_{IO}		7	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13, 23)

AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	t_{RC}	110		130		150		ns	
READ-WRITE cycle time	t_{RWC}	150		180		200		ns	
FAST-PAGE-MODE READ or WRITE cycle time	t_{PC}	40		45		50		ns	
FAST-PAGE-MODE READ-WRITE cycle time	t_{PRWC}	85		95		100		ns	
Access time from $\overline{RAS}$	t_{RAC}		60		70		80	ns	14
Access time from $\overline{CAS}$	t_{CAC}		15		20		20	ns	15
Output Enable	t_{OE}		15		20		20	ns	23
Access time from column address	t_{AA}		30		35		40	ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		35		40		45	ns	
$\overline{RAS}$ pulse width	t_{RAS}	60	100,000	70	100,000	80	100,000	ns	
$\overline{RAS}$ pulse width (FAST PAGE MODE)	t_{RASP}	60	100,000	70	100,000	80	100,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	15		20		20		ns	
$\overline{RAS}$ precharge time	t_{RP}	40		50		60		ns	
$\overline{CAS}$ pulse width	t_{CAS}	15	100,000	20	100,000	20	100,000	ns	
$\overline{CAS}$ hold time	t_{CSH}	60		70		80		ns	
$\overline{CAS}$ precharge time	t_{CPN}	10		10		10		ns	16
$\overline{CAS}$ precharge time (FAST PAGE MODE)	t_{CP}	10		10		10		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	45	20	50	20	60	ns	17
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		5		ns	
Row address setup time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	10		10		10		ns	
$\overline{RAS}$ to column address delay time	t_{RAD}	15	30	15	35	15	40	ns	18
Column address setup time	t_{ASC}	0		0		0		ns	
Column address hold time	t_{CAH}	10		15		15		ns	
Column address hold time (referenced to $\overline{RAS}$)	t_{AR}	50		55		60		ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	30		35		40		ns	
Read command setup time	t_{RCS}	0		0		0		ns	
Read command hold time (referenced to $\overline{CAS}$)	t_{RCH}	0		0		0		ns	19
Read command hold time (referenced to $\overline{RAS}$)	t_{RRH}	0		0		0		ns	19
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	0		0		0		ns	
Output buffer turn-off delay	t_{OFF}	0	15	0	20	0	20	ns	20

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

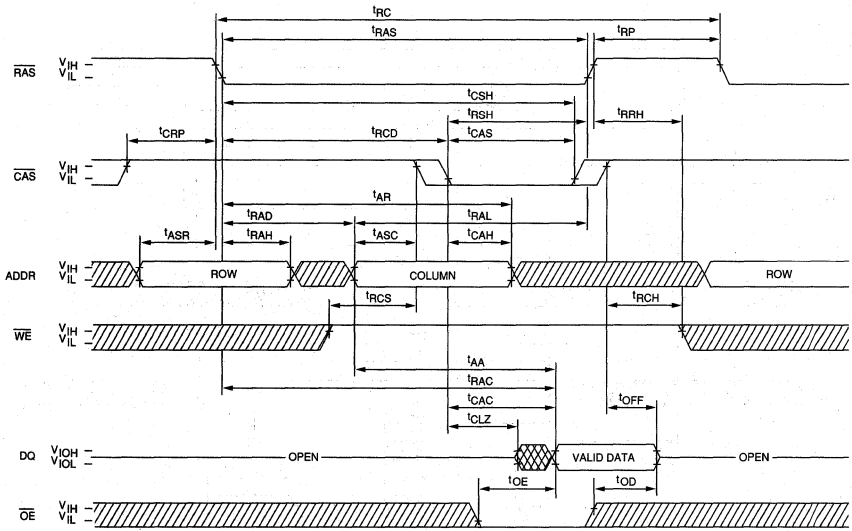
(Notes: 6, 7, 8, 9, 10, 11, 12, 13, 23)

AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
$\overline{WE}$ command setup time	^tWCS	0		0		0		ns	21, 27
Write command hold time	^tWCH	10		15		15		ns	
Write command hold time (referenced to $\overline{RAS}$)	^tWCR	45		55		60		ns	
Write command pulse width	^tWP	10		15		15		ns	
Write command to $\overline{RAS}$ lead time	^tRWL	15		20		20		ns	
Write command to $\overline{CAS}$ lead time	^tCWL	15		20		20		ns	
Data-in setup time	^tDS	0		0		0		ns	22
Data-in hold time	^tDH	10		15		15		ns	22
Data-in hold time (referenced to $\overline{RAS}$)	^tDHR	45		55		60		ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	^tRWD	85		95		105		ns	21
Column address to $\overline{WE}$ delay time	^tAWD	55		60		65		ns	21
$\overline{CAS}$ to $\overline{WE}$ delay time	^tCWD	40		45		45		ns	21
Transition time (rise or fall)	^tT	3	50	3	50	3	50	ns	9, 10
Refresh period (2,048/4,096 cycles)	^tREF		32/64		32/64		32/64	ms	26
$\overline{RAS}$ to $\overline{CAS}$ precharge time	^tRPC	0		0		0		ns	
$\overline{CAS}$ setup time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tCSR	5		5		5		ns	5
$\overline{CAS}$ hold time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tCHR	15		15		15		ns	5
$\overline{WE}$ hold time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tWRH	10		10		10		ns	25
$\overline{WE}$ setup time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tWRP	10		10		10		ns	25
$\overline{WE}$ hold time (WCBR test cycle)	^tWTH	10		10		10		ns	25
$\overline{WE}$ setup time (WCBR test cycle)	^tWTS	10		10		10		ns	25
$\overline{OE}$ setup prior to RAS during HIDDEN REFRESH cycle	^tORD	0		0		0		ns	
Output disable	^tOD		15		20		20	ns	
$\overline{OE}$ hold time from $\overline{WE}$ during READ-MODIFY-WRITE cycle	^tOEH	15		15		15		ns	

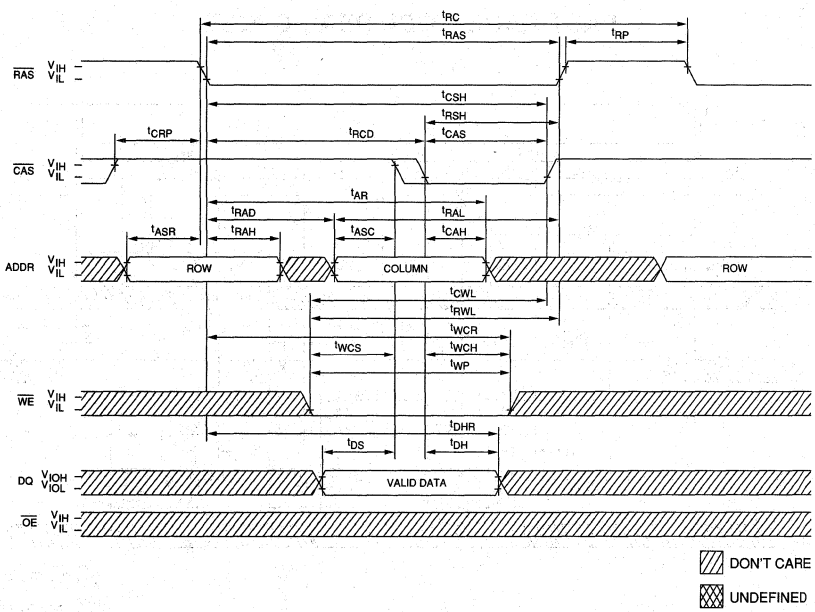
NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. V_{CC} = 5V ±10%, f = 1 MHz.
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is assured.
7. An initial pause of 100µs is required after power-up followed by eight $\overline{RAS}$ refresh cycles ($\overline{RAS}$-ONLY or CBR with $\overline{WE}$ HIGH) before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-up should be repeated any time the ^{t}REF refresh requirement is exceeded.
8. AC characteristics assume ^{t}T = 5ns.
9. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS}$ = V_{IH}, data output is High-Z.
12. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to 2 TTL gates and 100pF.
14. Assumes that $^{t}RCD < {}^{t}RCD$ (MAX). If ^{t}RCD is greater than the maximum recommended value shown in this table, ^{t}RAC will increase by the amount that ^{t}RCD exceeds the value shown.
15. Assumes that $^{t}RCD \geq {}^{t}RCD$ (MAX).
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer, $\overline{CAS}$ must be pulsed HIGH for ^{t}CPN.
17. Operation within the ^{t}RCD (MAX) limit ensures that ^{t}RAC (MAX) can be met. ^{t}RCD (MAX) is specified as a reference point only; if ^{t}RCD is greater than the specified ^{t}RCD (MAX) limit, then access time is controlled exclusively by ^{t}CAC.
18. Operation within the ^{t}RAD (MAX) limit ensures that ^{t}RAC (MIN) and ^{t}CAC (MIN) can be met. ^{t}RAD (MAX) is specified as a reference point only; if ^{t}RAD is greater than the specified ^{t}RAD (MAX) limit, then access time is controlled exclusively by ^{t}AA.
19. Either ^{t}RCH or ^{t}RRH must be satisfied for a READ cycle.
20. ^{t}OFF (MAX) defines the time at which the output achieves the open circuit condition, and is not referenced to V_{OH} or V_{OL}.
21. ^{t}WCS, ^{t}RWD, ^{t}AWD and ^{t}CWD are not restrictive operating parameters. ^{t}WCS applies to EARLY-WRITE cycles. ^{t}RWD, ^{t}AWD and ^{t}CWD apply to READ-MODIFY-WRITE cycles. If $^{t}WCS \geq {}^{t}WCS$ (MIN), the cycle is an EARLY-WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If $^{t}RWD \geq {}^{t}RWD$ (MIN), $^{t}AWD \geq {}^{t}AWD$ (MIN) and $^{t}CWD \geq {}^{t}CWD$ (MIN), the cycle is a READ-MODIFY-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of data out is indeterminate. $\overline{OE}$ held HIGH and $\overline{WE}$ taken LOW after $\overline{CAS}$ goes LOW results in a LATE-WRITE ($\overline{OE}$ controlled) cycle. ^{t}WCS, ^{t}RWD, ^{t}CWD and ^{t}AWD are not applicable in a LATE-WRITE cycle.
22. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY-WRITE cycles and $\overline{WE}$ leading edge in LATE-WRITE or READ-MODIFY-WRITE cycles.
23. If $\overline{OE}$ is tied permanently LOW, LATE-WRITE or READ-MODIFY-WRITE operations are not possible.
24. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW and $\overline{OE}$ = HIGH.
25. ^{t}WTS and ^{t}WTH are setup and hold specifications for the $\overline{WE}$ pin being held LOW to enable the JEDEC test mode (with CBR timing constraints). These two parameters are the inverts of ^{t}WRP and ^{t}WRH in the CBR refresh cycle.
26. 32ms is 2,048 refresh, 64ms is 4,096 refresh.
27. 2,048 row refresh.
28. 4,096 row refresh.

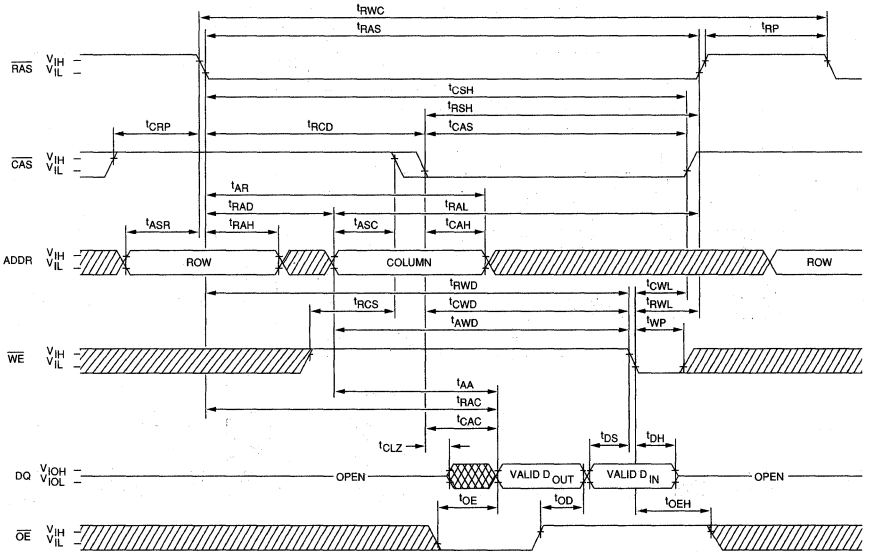
READ CYCLE



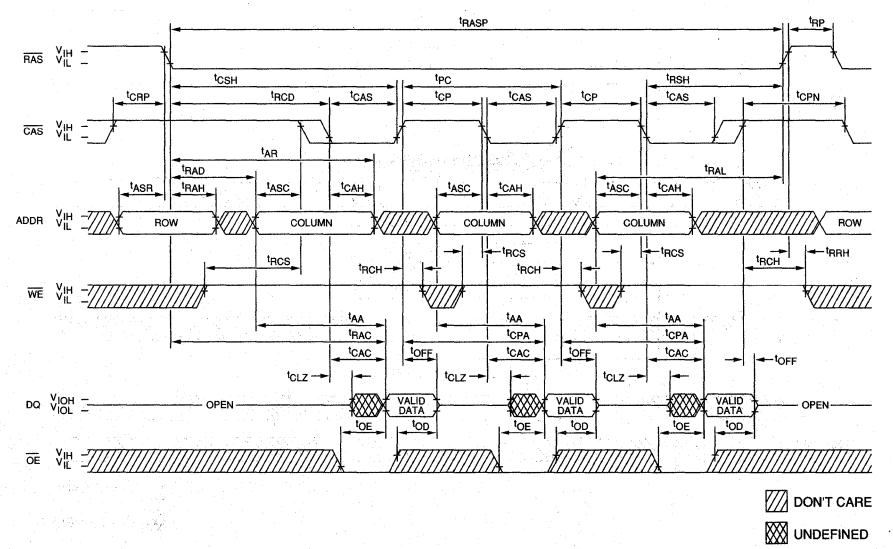
EARLY-WRITE CYCLE



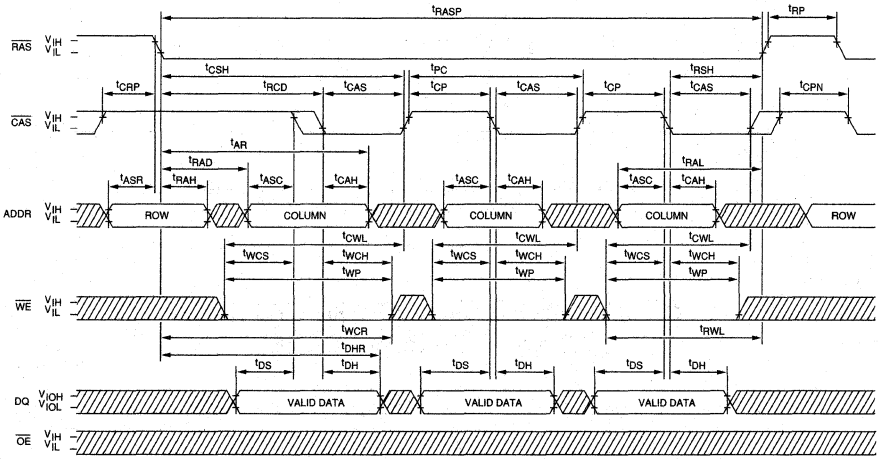
READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)



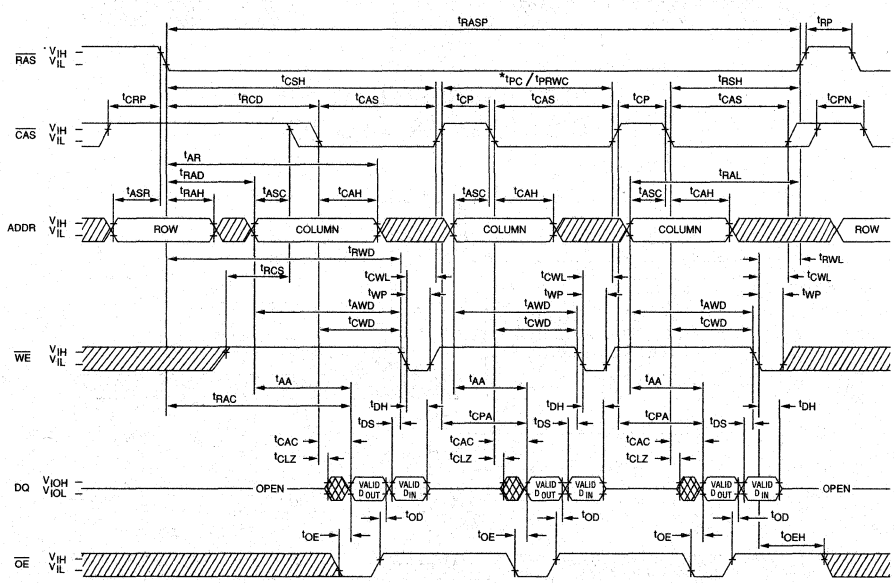
FAST-PAGE-MODE READ CYCLE



FAST-PAGE-MODE EARLY-WRITE CYCLE

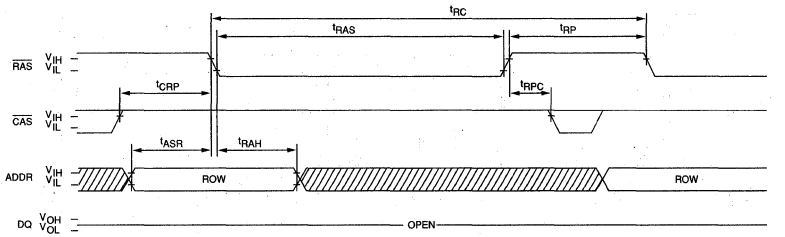


FAST-PAGE-MODE READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)

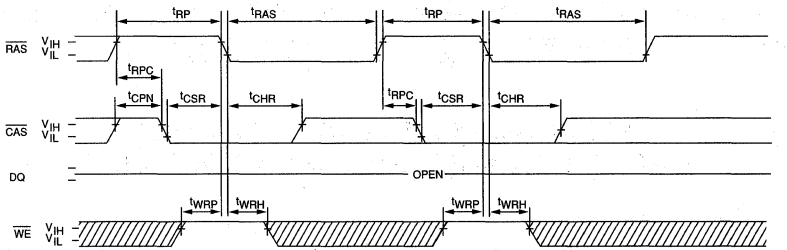


*tPC is for LATE-WRITE only.

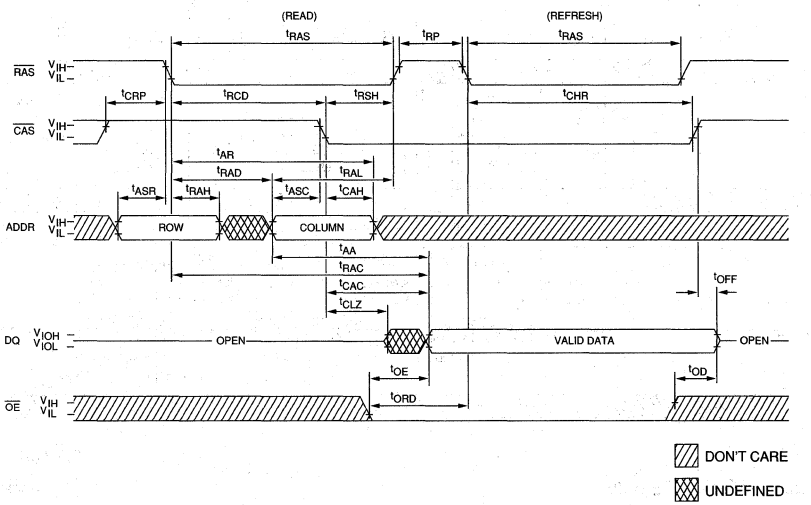
RAS-ONLY REFRESH CYCLE
(ADDR = A0-A9; WE = DON'T CARE)



CAS-BEFORE-RAS REFRESH CYCLE
(A0-A9, and OE = DON'T CARE)



HIDDEN REFRESH CYCLE [24]
(WE = HIGH; OE = LOW)



NEW DRAM

DRAM

4 MEG x 4 DRAM

3.3V FAST PAGE MODE

FEATURES

- Industry standard x4 pinout, timing, functions and packages
- High-performance, CMOS silicon-gate process
- Single power supply: +3.3V ±10%
- Low power, 1mW standby; 125mW active, typical (A1)
- All inputs, outputs and clocks are fully TTL compatible
- Refresh modes: $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$ (CBR) and HIDDEN
- 2,048-cycle refresh distributed across 32ms or 4,096-cycle refresh distributed across 64ms

OPTIONS MARKING

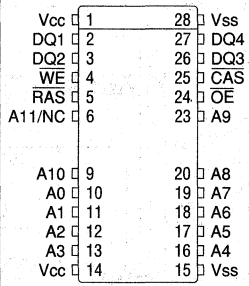
- Timing
  - 60ns access - 6
  - 70ns access - 7
  - 80ns access - 8
- Packages
  - Plastic SOJ (400 mil) DJ
  - Plastic TSOP (400 mil) TG

NOTE: Available in die form (commercial or military) or military ceramic packages. Please consult factory for die data sheets or refer to Micron's *Military Data Book*.

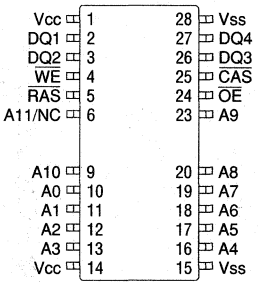
- Refresh Period
  - 2,048 cycles @ 32ms, 11 Row Addresses MT4LC4M4B1
  - 4,096 cycles @ 64ms, 12 Row Addresses MT4LC4M4A1
- Operating Temperature, T_A
  - Commercial (0°C to +70°C) None

PIN ASSIGNMENT (Top View)

24-Pin SOJ (Q-3)



24-Pin TSOP (R-2)



GENERAL DESCRIPTION

The MT4LC4M4A1/B1 are randomly accessed solid-state memories containing 16,777,216 bits organized in a x4 configuration. The MT4LC4M4A1 and MT4LC4M4B1 are the same DRAM versions except that the MT4LC4M4B1 has 2,048 cycle refresh instead of 4,096 cycle refresh. All further references made for the MT4LC4M4A1 also apply to the MT4LC4M4B1 unless specifically stated otherwise. For a device with 2,048 cycle refresh, $\overline{RAS}$ is used to latch the first 11 bits and $\overline{CAS}$ the latter 11 bits. For a device with 4,096 cycle refresh, $\overline{RAS}$ is used to latch the first 12 bits and $\overline{CAS}$ the latter 10 bits (A10 and A11 are "don't care" bits). READ and WRITE cycles are selected with the $\overline{WE}$ input. A logic HIGH on $\overline{WE}$ dictates READ mode while a logic LOW on $\overline{WE}$ dictates WRITE mode. During a WRITE cycle, data in (D) is latched by the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. If $\overline{WE}$ goes LOW prior to $\overline{CAS}$ going LOW, the output pins remain open (High-Z) until the next $\overline{CAS}$ cycle. If $\overline{WE}$ goes LOW after data reaches the output pins, data out (Q) is activated and retains the selected cell data as long as $\overline{CAS}$ remains LOW (regardless of $\overline{WE}$ or $\overline{RAS}$). This late $\overline{WE}$ pulse results in a READ-WRITE cycle. The four data inputs and the four data outputs are routed through four pins using common I/O, and pin direction is controlled by $\overline{WE}$ and $\overline{OE}$.

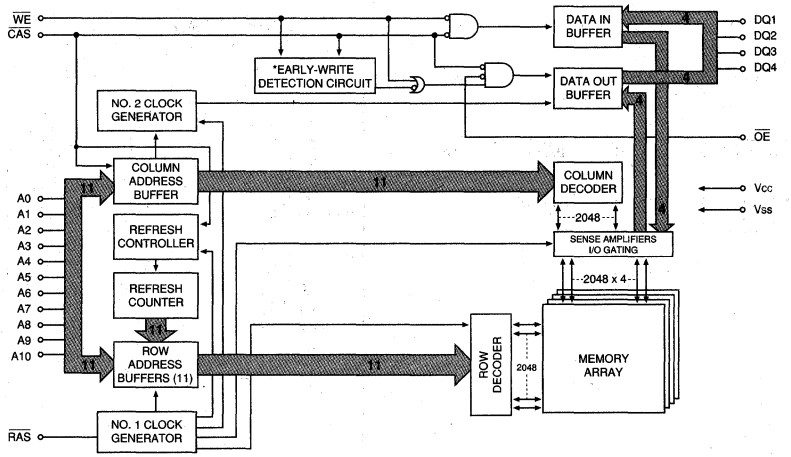
FAST PAGE MODE operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row address (A0-A9/10) defined page boundary. The FAST PAGE MODE cycle is always initiated with a row address strobed-in by $\overline{RAS}$ followed by a column address strobed-in by $\overline{CAS}$. $\overline{CAS}$ may be toggled-in by holding $\overline{RAS}$ LOW and strobing-in different column addresses, thus executing faster memory cycles. Returning $\overline{RAS}$ HIGH terminates the FAST PAGE MODE operation.

Returning $\overline{RAS}$ and $\overline{CAS}$ HIGH terminates a memory cycle and decreases chip current to a reduced standby level.

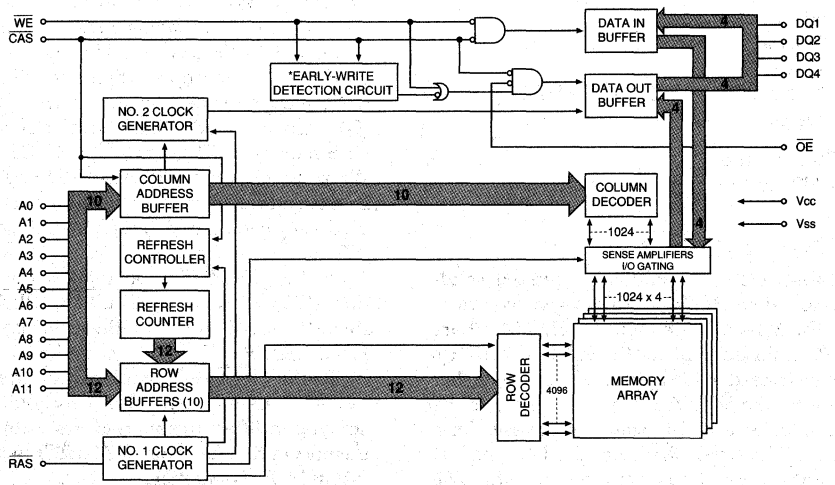
Also, the chip is preconditioned for the next cycle during the $\overline{RAS}$ high time. Memory cell data is retained in its correct state by maintaining power and executing any $\overline{RAS}$ cycle (READ, WRITE, $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$ (CBR) or HIDDEN refresh) so that all 2,048/4,096 combinations of $\overline{RAS}$ addresses (A0-A10/A11) are executed at least every 32ms/64ms, regardless of sequence. The CBR refresh cycle will invoke the refresh counter for automatic $\overline{RAS}$ addressing.

If CBR refresh is used, the number of cycles is a "don't care."

FUNCTIONAL BLOCK DIAGRAM
FAST PAGE MODE MT4LC4M4B1 (11 Row Addresses)



FUNCTIONAL BLOCK DIAGRAM
FAST PAGE MODE MT4LC4M4A1 (12 Row Addresses)



*NOTE: $\overline{WE}$ LOW prior to $\overline{CAS}$ LOW, EW detection circuit output is a HIGH (EARLY-WRITE)
$\overline{CAS}$ LOW prior to $\overline{WE}$ LOW, EW detection circuit output is a LOW (LATE-WRITE)

TRUTH TABLE

FUNCTION		RAS	CAS	WE	OE	ADDRESSES		DATA IN/OUT
						^tR	^tC	DQ1-DQ4
Standby		H	H→X	X	X	X	X	High-Z
READ		L	L	H	L	ROW	COL	Data Out
EARLY-WRITE		L	L	L	X	ROW	COL	Data In
READ-WRITE		L	L	H→L	L→H	ROW	COL	Data Out, Data In
FAST-PAGE-MODE	1st Cycle	L	H→L	H	L	ROW	COL	Data Out
READ	2nd Cycle	L	H→L	H	L	n/a	COL	Data Out
FAST-PAGE-MODE	1st Cycle	L	H→L	L	X	ROW	COL	Data In
EARLY-WRITE	2nd Cycle	L	H→L	L	X	n/a	COL	Data In
FAST-PAGE-MODE	1st Cycle	L	H→L	H→L	L→H	ROW	COL	Data Out, Data In
READ-WRITE	2nd Cycle	L	H→L	H→L	L→H	n/a	COL	Data Out, Data In
RAS-ONLY REFRESH		L	H	X	X	ROW	n/a	High-Z
HIDDEN	READ	L→H→L	L	H	L	ROW	COL	Data Out
REFRESH	WRITE	L→H→L	L	L	X	ROW	COL	Data In
CAS-BEFORE-RAS REFRESH		H→L	L	H	X	X	X	High-Z

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to V_{SS} (3.3V) ..-1.0V to +4.5V
Operating Temperature, T_A (Ambient) .....0°C to +70°C
Storage Temperature (Plastic) .....-55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 3, 4, 6, 7) (V_{CC} = 3.3V ±10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	3.0	3.6	V	1
Input High (Logic 1) Voltage, All Inputs	V_{IH}	2.0	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, All Inputs	V_{IL}	-1.0	0.8	V	1
INPUT LEAKAGE CURRENT Any Input 0V ≤ V_{IN} ≤ 3.6V (All other pins not under test = 0V)	I_I	-2	2	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled, 0V ≤ V_{OUT} ≤ 3.6V)	I_{OZ}	-10	10	µA	
OUTPUT LEVELS Output High Voltage (I_{OUT} = -2mA)	V_{OH}	2.4		V	
Output Low Voltage (I_{OUT} = 2mA)	V_{OL}		0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 3, 4, 6, 7) (V_{CC} = 3.3V ±10%), 4,096 cycle refresh

		MAX				
PARAMETER/CONDITION	**SYMBOL**	**-6**	**-7**	**-8**	**UNITS**	**NOTES**
STANDBY CURRENT: (TTL) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC1}	1	1	1	mA	
STANDBY CURRENT: (CMOS) ($\overline{RAS}$ = $\overline{CAS}$ = Other Inputs = V_{CC} -0.2V)	I_{CC2}	400	400	400	µA	
OPERATING CURRENT: Random READ/WRITE Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC (MIN))	I_{CC3}	60	55	50	mA	3, 4, 28
OPERATING CURRENT: FAST PAGE MODE Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: ^tPC = ^tPC (MIN))	I_{CC4}	40	35	30	mA	3, 4, 28
REFRESH CURRENT: $\overline{RAS}$-ONLY Average power supply current ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}: ^tRC = ^tRC (MIN))	I_{CC5}	60	55	50	mA	3, 28
REFRESH CURRENT: $\overline{CAS}$-BEFORE-$\overline{RAS}$ Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC (MIN))	I_{CC6}	60	55	50	mA	3, 5, 28

(Notes: 1, 3, 4, 6, 7) (V_{CC} = 3.3V ±10%), 2,048 cycle refresh

		MAX				
PARAMETER/CONDITION	**SYMBOL**	**-6**	**-7**	**-8**	**UNITS**	**NOTES**
STANDBY CURRENT: (TTL) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC1}	1	1	1	mA	
STANDBY CURRENT: (CMOS) ($\overline{RAS}$ = $\overline{CAS}$ = Other Inputs = V_{CC} -0.2V)	I_{CC2}	400	400	400	µA	
OPERATING CURRENT: Random READ/WRITE Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC (MIN))	I_{CC3}	80	70	60	mA	3, 4, 27
OPERATING CURRENT: FAST PAGE MODE Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: ^tPC = ^tPC (MIN))	I_{CC4}	60	50	40	mA	3, 4, 27
REFRESH CURRENT: $\overline{RAS}$-ONLY Average power supply current ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}: ^tRC = ^tRC (MIN))	I_{CC5}	80	70	60	mA	3, 27
REFRESH CURRENT: $\overline{CAS}$-BEFORE-$\overline{RAS}$ Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC (MIN))	I_{CC6}	80	70	60	mA	3, 5, 27

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A11	C_{I1}		5	pF	2
Input Capacitance: $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$	C_{I2}		7	pF	2
Input/Output Capacitance: DQ	C_{IO}		7	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13, 23)

AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	^tRC	110		130		150		ns	
READ-WRITE cycle time	^tRWC	150		180		200		ns	
FAST-PAGE-MODE READ or WRITE cycle time	^tPC	40		45		50		ns	
FAST-PAGE-MODE READ-WRITE cycle time	^tPRWC	85		95		100		ns	
Access time from $\overline{RAS}$	^tRAC		60		70		80	ns	14
Access time from $\overline{CAS}$	^tCAC		15		20		20	ns	15
Output Enable	^tOE		15		20		20	ns	23
Access time from column address	^tAA		30		35		40	ns	
Access time from $\overline{CAS}$ precharge	^tCPA		35		40		45	ns	
$\overline{RAS}$ pulse width	^tRAS	60	100,000	70	100,000	80	100,000	ns	
$\overline{RAS}$ pulse width (FAST PAGE MODE)	^tRASP	60	100,000	70	100,000	80	100,000	ns	
$\overline{RAS}$ hold time	^tRSH	15		20		20		ns	
$\overline{RAS}$ precharge time	^tRP	40		50		60		ns	
$\overline{CAS}$ pulse width	^tCAS	15	100,000	20	100,000	20	100,000	ns	
$\overline{CAS}$ hold time	^tCSH	60		70		80		ns	
$\overline{CAS}$ precharge time	^tCPN	10		10		10		ns	16
$\overline{CAS}$ precharge time (FAST PAGE MODE)	^tCP	10		10		10		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	^tRCD	20	45	20	50	20	60	ns	17
$\overline{CAS}$ to $\overline{RAS}$ precharge time	^tCRP	5		5		5		ns	
Row address setup time	^tASR	0		0		0		ns	
Row address hold time	^tRAH	10		10		10		ns	
$\overline{RAS}$ to column address delay time	^tRAD	15	30	15	35	15	40	ns	18
Column address setup time	^tASC	0		0		0		ns	
Column address hold time	^tCAH	10		15		15		ns	
Column address hold time (referenced to $\overline{RAS}$)	^tAR	50		55		60		ns	
Column address to $\overline{RAS}$ lead time	^tRAL	30		35		40		ns	
Read command setup time	^tRCS	0		0		0		ns	
Read command hold time (referenced to $\overline{CAS}$)	^tRCH	0		0		0		ns	19
Read command hold time (referenced to $\overline{RAS}$)	^tRRH	0		0		0		ns	19
$\overline{CAS}$ to output in Low-Z	^tCLZ	0		0		0		ns	
Output buffer turn-off delay	^tOFF	0	15	0	20	0	20	ns	20

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

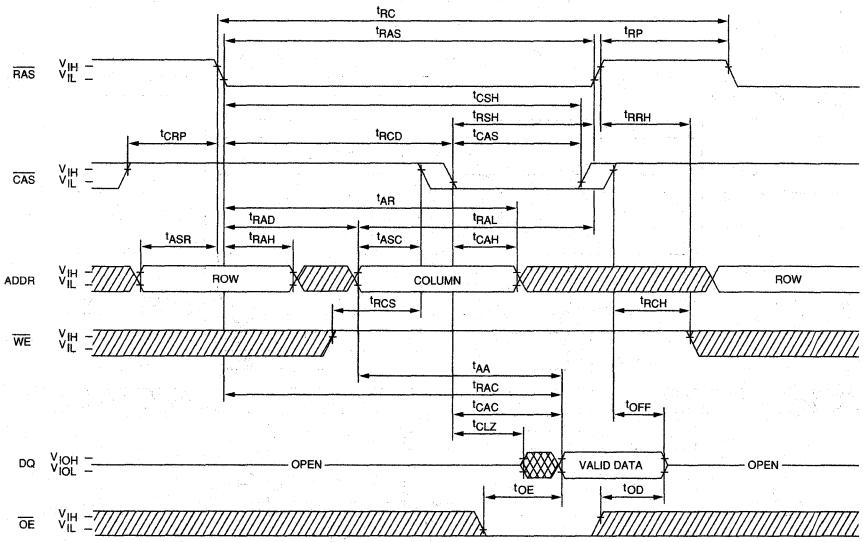
(Notes: 6, 7, 8, 9, 10, 11, 12, 13, 23)

AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
$\overline{WE}$ command setup time	^tWCS	0		0		0		ns	21, 27
Write command hold time	^tWCH	10		15		15		ns	
Write command hold time (referenced to $\overline{RAS}$)	^tWCR	45		55		60		ns	
Write command pulse width	^tWP	10		15		15		ns	
Write command to $\overline{RAS}$ lead time	^tRWL	15		20		20		ns	
Write command to $\overline{CAS}$ lead time	^tCWL	15		20		20		ns	
Data-in setup time	^tDS	0		0		0		ns	22
Data-in hold time	^tDH	10		15		15		ns	22
Data-in hold time (referenced to $\overline{RAS}$)	^tDHR	45		55		60		ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	^tRWD	85		95		105		ns	21
Column address to $\overline{WE}$ delay time	^tAWD	55		60		65		ns	21
$\overline{CAS}$ to $\overline{WE}$ delay time	^tCWD	40		45		45		ns	21
Transition time (rise or fall)	^tT	3	50	3	50	3	50	ns	9, 10
Refresh period (2,048/4,096 cycles)	^tREF		32/64		32/64		32/64	ms	26
$\overline{RAS}$ to $\overline{CAS}$ precharge time	^tRPC	0		0		0		ns	
$\overline{CAS}$ setup time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tCSR	5		5		5		ns	5
$\overline{CAS}$ hold time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tCHR	15		15		15		ns	5
$\overline{WE}$ hold time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tWRH	10		10		10		ns	25
$\overline{WE}$ setup time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tWRP	10		10		10		ns	25
$\overline{WE}$ hold time (WCBR test cycle)	^tWTH	10		10		10		ns	25
$\overline{WE}$ setup time (WCBR test cycle)	^tWTS	10		10		10		ns	25
$\overline{OE}$ setup prior to RAS during HIDDEN REFRESH cycle	^tORD	0		0		0		ns	
Output disable	^tOD		15		20		20	ns	
$\overline{OE}$ hold time from $\overline{WE}$ during READ-MODIFY-WRITE cycle	^tOEH	15		15		15		ns	

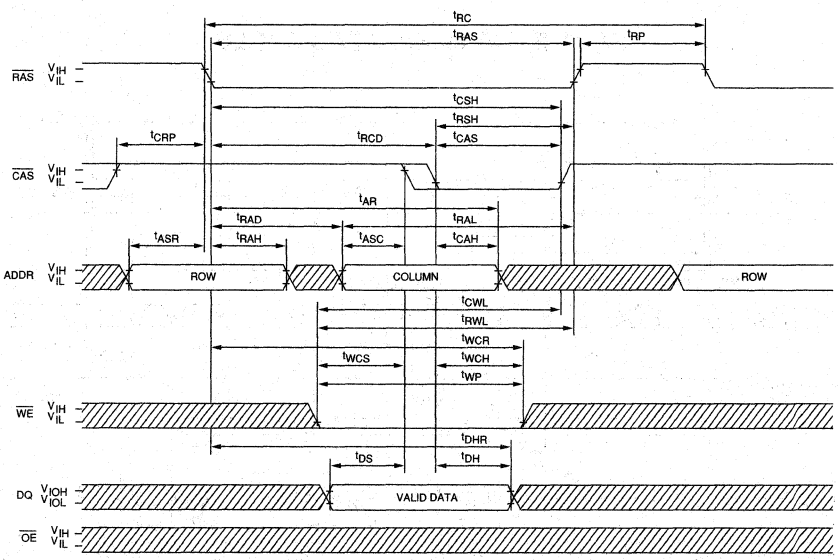
NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. V_{CC} = 5V ±10%, f = 1 MHz.
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is assured.
7. An initial pause of 100µs is required after power-up followed by eight $\overline{RAS}$ refresh cycles ($\overline{RAS}$-ONLY or CBR with $\overline{WE}$ HIGH) before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-up should be repeated any time the ^{t}REF refresh requirement is exceeded.
8. AC characteristics assume ^{t}T = 5ns.
9. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS}$ = V_{IH}, data output is High-Z.
12. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to 2 TTL gates and 100pF.
14. Assumes that $^{t}RCD < {}^{t}RCD$ (MAX). If ^{t}RCD is greater than the maximum recommended value shown in this table, ^{t}RAC will increase by the amount that ^{t}RCD exceeds the value shown.
15. Assumes that $^{t}RCD \geq {}^{t}RCD$ (MAX).
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer, $\overline{CAS}$ must be pulsed HIGH for ^{t}CPN.
17. Operation within the ^{t}RCD (MAX) limit ensures that ^{t}RAC (MAX) can be met. ^{t}RCD (MAX) is specified as a reference point only; if ^{t}RCD is greater than the specified ^{t}RCD (MAX) limit, then access time is controlled exclusively by ^{t}CAC.
18. Operation within the ^{t}RAD (MAX) limit ensures that ^{t}RAC (MIN) and ^{t}CAC (MIN) can be met. ^{t}RAD (MAX) is specified as a reference point only; if ^{t}RAD is greater than the specified ^{t}RAD (MAX) limit, then access time is controlled exclusively by ^{t}AA.
19. Either ^{t}RCH or ^{t}RRH must be satisfied for a READ cycle.
20. ^{t}OFF (MAX) defines the time at which the output achieves the open circuit condition, and is not referenced to V_{OH} or V_{OL}.
21. ^{t}WCS, ^{t}RWD, ^{t}AWD and ^{t}CWD are not restrictive operating parameters. ^{t}WCS applies to EARLY-WRITE cycles. ^{t}RWD, ^{t}AWD and ^{t}CWD apply to READ-MODIFY-WRITE cycles. If $^{t}WCS \geq {}^{t}WCS$ (MIN), the cycle is an EARLY-WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If $^{t}RWD \geq {}^{t}RWD$ (MIN), $^{t}AWD \geq {}^{t}AWD$ (MIN) and $^{t}CWD \geq {}^{t}CWD$ (MIN), the cycle is a READ-MODIFY-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of data out is indeterminate. $\overline{OE}$ held HIGH and $\overline{WE}$ taken LOW after $\overline{CAS}$ goes LOW results in a LATE-WRITE ($\overline{OE}$ controlled) cycle. ^{t}WCS, ^{t}RWD, ^{t}CWD and ^{t}AWD are not applicable in a LATE-WRITE cycle.
22. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY-WRITE cycles and $\overline{WE}$ leading edge in LATE-WRITE or READ-MODIFY-WRITE cycles.
23. If $\overline{OE}$ is tied permanently LOW, LATE-WRITE or READ-MODIFY-WRITE operations are not possible.
24. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW and $\overline{OE}$ = HIGH.
25. ^{t}WTS and ^{t}WTH are setup and hold specifications for the $\overline{WE}$ pin being held LOW to enable the JEDEC test mode (with CBR timing constraints). These two parameters are the inverts of ^{t}WRP and ^{t}WRH in the CBR refresh cycle.
26. 32ms is 2,048 refresh, 64ms is 4,096 refresh.
27. 2,048 row refresh.
28. 4,096 row refresh.

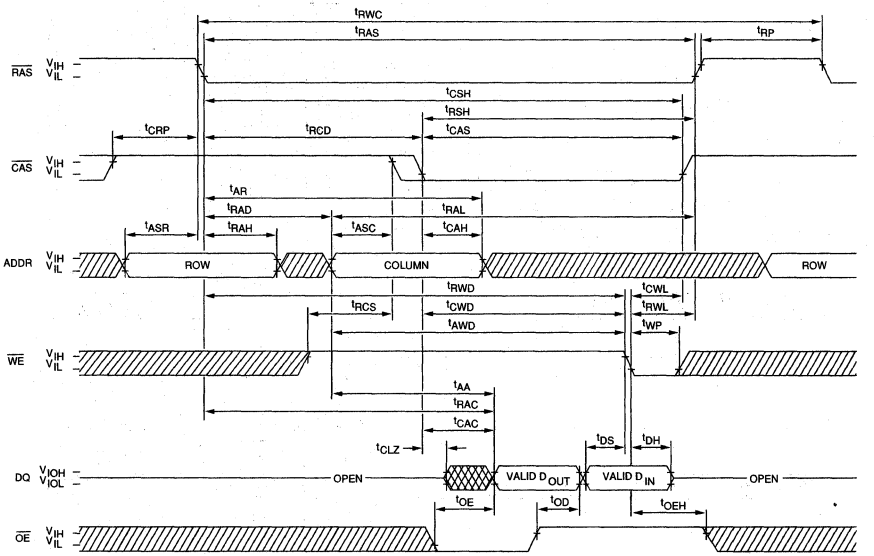
READ CYCLE



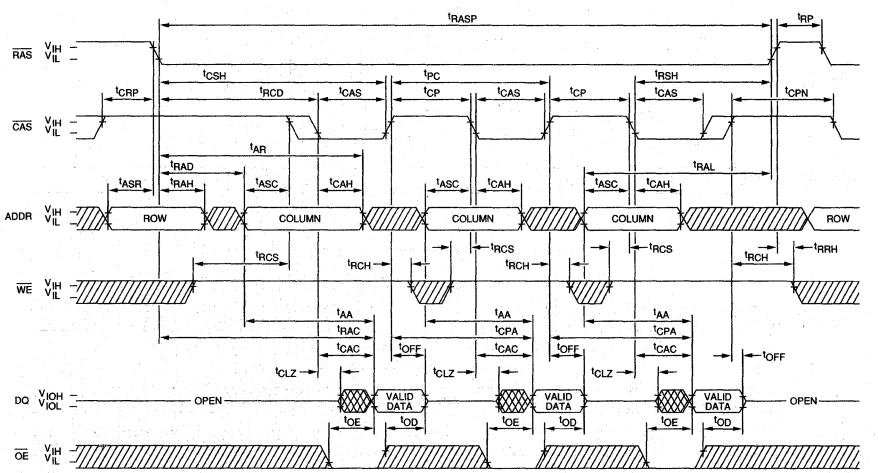
EARLY-WRITE CYCLE



READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)



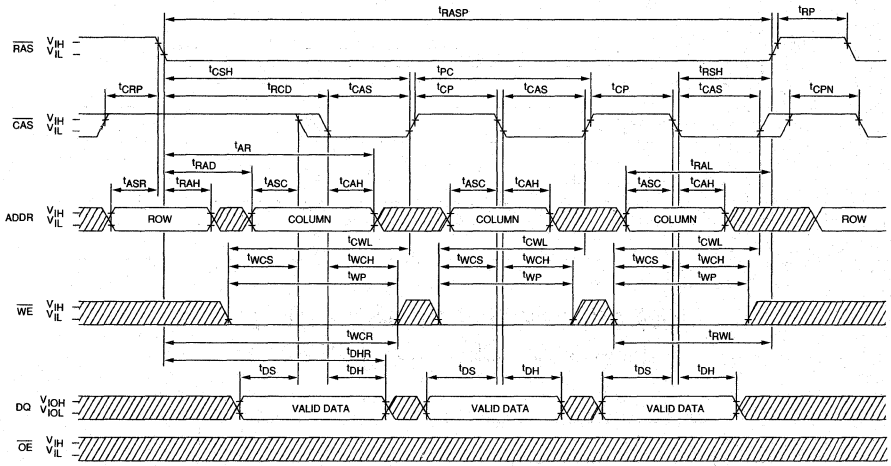
FAST-PAGE-MODE READ CYCLE



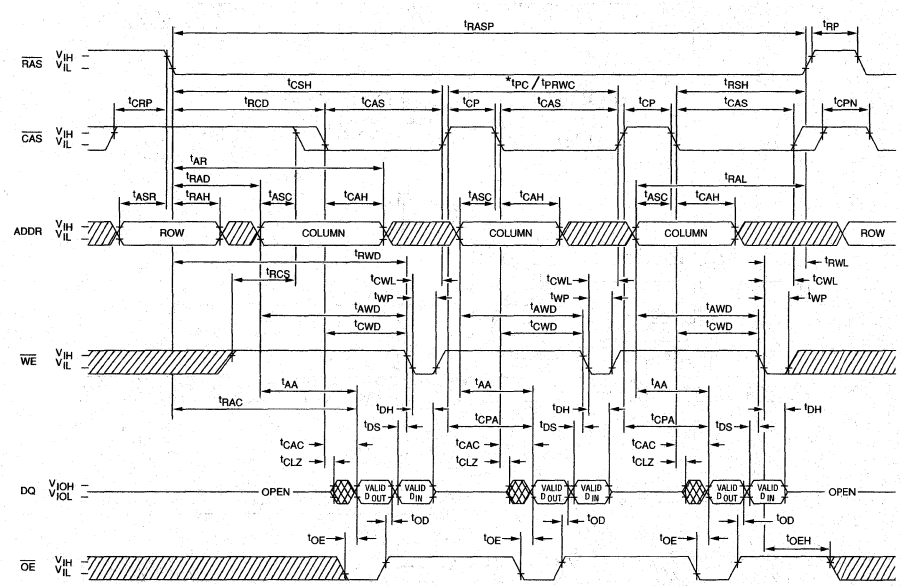
DON'T CARE

UNDEFINED

FAST-PAGE-MODE EARLY-WRITE CYCLE

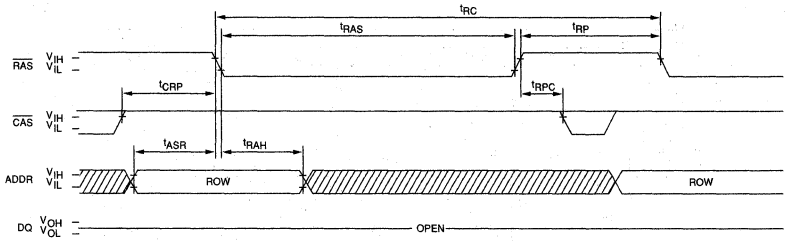


FAST-PAGE-MODE READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)

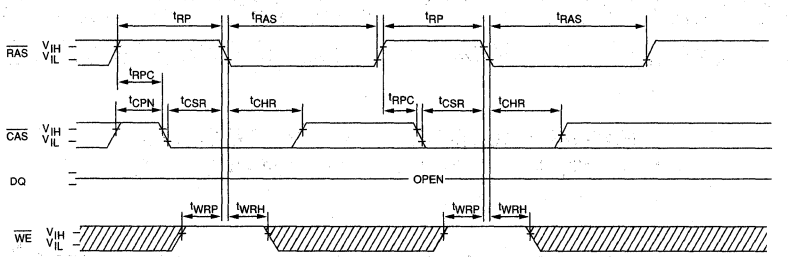


*tPC is for LATE-WRITE only.

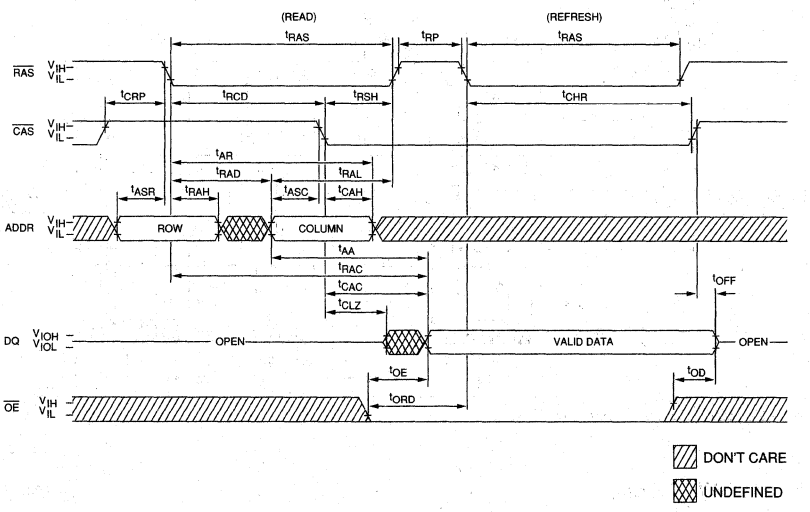
RAS-ONLY REFRESH CYCLE
(ADDR = A0-A9; WE = DON'T CARE)



CAS-BEFORE-RAS REFRESH CYCLE
(A0-A9, and OE = DON'T CARE)



HIDDEN REFRESH CYCLE [24]
(WE = HIGH; OE = LOW)



DRAM

4 MEG x 4 DRAM

STATIC COLUMN

FEATURES

- Industry standard x4 pinout, timing, functions and packages
- High-performance, CMOS silicon-gate process
- Single power supply: +5V ±10%
- Low power, 5mW standby; 275mW active, typical
- All inputs, outputs and clocks are fully TTL compatible
- Refresh modes: $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$ (CBR) and HIDDEN
- 4,096-cycle refresh distributed across 64ms

OPTIONS — MARKING

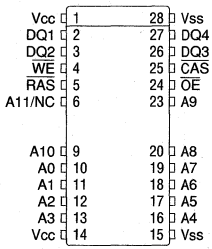
- Timing
  - 60ns access — -6
  - 70ns access — -7
  - 80ns access — -8
- Packages
  - Plastic SOJ (400 mil) — DJ

NOTE: Available in die form (commercial or military) or military ceramic packages. Please consult factory for die data sheets or refer to Micron's ***Military Data Book.***

- Refresh Period
  - 4,096 cycles @ 64ms, 12 Row Addresses — MT4C4M4D1
- Operating Temperature, T_A
  - Commercial (0°C to +70°C) — None

PIN ASSIGNMENT (Top View)

24-Pin SOJ
(Q-3)



GENERAL DESCRIPTION

The MT4C4M4D1 is a randomly accessed solid-state memory containing 16,777,216 bits organized in a x4 configuration. During READ or WRITE cycles, each bit is uniquely addressed through the 22 address bits, which are entered 10-12 bits (A0-A11) at a time. $\overline{RAS}$ is used to latch the first 12 bits and $\overline{CAS}$ the latter 10 (A10 and A11 are "don't care" bits). READ and WRITE cycles are selected with the $\overline{WE}$ input. A logic HIGH on $\overline{WE}$ dictates READ mode while a logic LOW on $\overline{WE}$ dictates WRITE mode. During a WRITE cycle, data in (D) is latched by the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. If $\overline{WE}$ goes LOW prior to $\overline{CAS}$ going LOW, the output pins remain open (High-Z) until the next $\overline{CAS}$ cycle. If $\overline{WE}$ goes LOW after data reaches the output pins, data out (Q) is activated and retains the selected cell data as long as $\overline{CAS}$ remains LOW (regardless of $\overline{WE}$ or $\overline{RAS}$). This late $\overline{WE}$ pulse results in a READ-WRITE cycle. The four data inputs and the four data outputs are routed through four pins using common I/O, and pin direction is controlled by $\overline{WE}$ and $\overline{OE}$.

STATIC COLUMN operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row address (A0-A9) defined page boundary. After the first READ, any column address transition will result in new data out. Unlike the PAGE-MODE part, which requires $\overline{CAS}$ to be toggled for each successive PAGE-MODE access, the STATIC COLUMN part allows $\overline{CAS}$ to be left LOW for successive STATIC COLUMN accesses. Returning $\overline{RAS}$ HIGH terminates the STATIC COLUMN operation.

Returning $\overline{RAS}$ and $\overline{CAS}$ HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the $\overline{RAS}$ high time. Memory cell data is retained in its correct state by maintaining power and executing any $\overline{RAS}$ cycle (READ, WRITE, $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$ (CBR), or HIDDEN refresh) so that all 4,096 combinations of $\overline{RAS}$ addresses (A0-A11) are executed at least every 64ms, regardless of sequence. The CBR refresh cycle will invoke the internal refresh counter for automatic $\overline{RAS}$ addressing.

MICRON TECHNOLOGY, INC.

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WIDE DRAM PRODUCT SELECTION GUIDE

Memory Configuration	Optional Access Cycle	Part Number*	Access Time (ns)	Typical Power Dissipation		Package/Number of Pins			Page
				Standby	Active	ZIP	SOJ	TSOP	
512K x 8	FP	MT4C8512	70, 80, 100	3mW	350mW	28	28	28	2-1
512K x 8	FP, WPB	MT4C8513	70, 80, 100	3mW	350mW	28	28	28	2-1
512K x 8	FP, LP	MT4C8512 L	70, 80, 100	1mW	350mW	28	28	28	2-15
512K x 8	FP, WPB, LP	MT4C8513 L	70, 80, 100	1mW	350mW	28	28	28	2-15
2 Meg x 8	FP, 4KR	MT4(L)C2M8A1	60, 70, 80	5mW	400mW	-	28, 32	28, 32	2-31
2 Meg x 8	FP, 4KR, WPB	MT4(L)C2M8A2	60, 70, 80	5mW	400mW	-	28, 32	28, 32	2-31
2 Meg x 8	FP, 2KR	MT4(L)C2M8B1	60, 70, 80	5mW	400mW	-	28, 32	28, 32	2-47
2 Meg x 8	FP, 2KR, WPB	MT4(L)C2M8B2	60, 70, 80	5mW	400mW	-	28, 32	28, 32	2-47
2 Meg x 8	FP, 4KR, S, LP	MT4(L)C2M8A1 S	60, 70, 80	2mW	400mW	-	28, 32	28, 32	2-63
2 Meg x 8	FP, 4KR, WPB, S, LP	MT4(L)C2M8A2 S	60, 70, 80	2mW	400mW	-	28, 32	28, 32	2-63
2 Meg x 8	FP, 2KR, S, LP	MT4(L)C2M8B1 S	60, 70, 80	2mW	400mW	-	28, 32	28, 32	2-81
2 Meg x 8	FP, 2KR, WPB, S, LP	MT4(L)C2M8B2 S	60, 70, 80	2mW	400mW	-	28, 32	28, 32	2-81
64K x 16	FP, DW	MT4C1664	70, 80, 100	3mW	225mW	40	40	40	2-99
64K x 16	FP, WPB	MT4C1665	70, 80, 100	3mW	225mW	40	40	40	2-99
64K x 16	FP, DW, LP	MT4C1664 L	70, 80, 100	1mW	225mW	40	40	40	2-115
64K x 16	FP, WPB, LP	MT4C1665 L	70, 80, 100	1mW	225mW	40	40	40	2-115
64K x 16	SC, DW	MT4C1670	70, 80, 100	3mW	225mW	40	40	40	2-133
64K x 16	SC, WPB	MT4C1671	70, 80, 100	3mW	225mW	40	40	40	2-133
64K x 16	SC, DW, LP	MT4C1670 L	70, 80, 100	1mW	225mW	40	40	40	2-151
64K x 16	SC, WPB, LP	MT4C1671 L	70, 80, 100	1mW	225mW	40	40	40	2-151
256K x 16	FP, DW	MT4C16256	70, 80, 100	3mW	500mW	40	40	40	2-169
256K x 16	FP, DC	MT4C16257	70, 80, 100	3mW	500mW	40	40	40	2-169
256K x 16	FP, DW, WPB	MT4C16258	70, 80, 100	3mW	500mW	40	40	40	2-169
256K x 16	FP, DC, WPB	MT4C16259	70, 80, 100	3mW	500mW	40	40	40	2-169
256K x 16	FP, DW, LP	MT4C16256 L	70, 80, 100	1mW	500mW	40	40	40	2-191
256K x 16	FP, DC, LP	MT4C16257 L	70, 80, 100	1mW	500mW	40	40	40	2-191
256K x 16	FP, DW, WPB, LP	MT4C16258 L	70, 80, 100	1mW	500mW	40	40	40	2-191
256K x 16	FP, DC, WPB, LP	MT4C16259 L	70, 80, 100	1mW	500mW	40	40	40	2-191
256K x 16	FP, ASY, DW	MT4C16260	70, 80, 100	1mW	500mW	40	40	40	2-213
256K x 16	FP, WPB, ASY	MT4C16261	70, 80, 100	1mW	500mW	40	40	40	2-213
1 Meg x 16	FP, DC	MT4(L)C1M16C3	60, 70, 80	5mW	500mW	-	42	44	2-229
1 Meg x 16	FP, DW	MT4(L)C1M16C5	60, 70, 80	5mW	500mW	-	42	44	2-229
1 Meg x 16	FP, DC, WPB	MT4(L)C1M16C6	60, 70, 80	5mW	500mW	-	42	44	2-229
1 Meg x 16	FP, DW, WPB	MT4(L)C1M16C7	60, 70, 80	5mW	500mW	-	42	44	2-229
1 Meg x 16	FP, DC, S, LP	MT4(L)C1M16C3 S	60, 70, 80	2mW	500mW	-	42	44	2-251
1 Meg x 16	FP, DW, S, LP	MT4(L)C1M16C5 S	60, 70, 80	2mW	500mW	-	42	44	2-251
1 Meg x 16	FP, DC, WPB, S, LP	MT4(L)C1M16C6 S	60, 70, 80	2mW	500mW	-	42	44	2-251
1 Meg x 16	FP, DW, WPB, S, LP	MT4(L)C1M16C7 S	60, 70, 80	2mW	500mW	-	42	44	2-251

FP = Fast Page Mode, SC = Static Column, LP = Low Power, Extended Refresh; WPB = Write Per Bit, DW = Dual WE, DC = Dual CAS, 2KR = 2,048 Refresh, 4KR = 4,096 Refresh, S = Self Refresh, ASY = Asymmetrical Addressing

*(L)C means device is available in both 5V Vcc (MT4CXXXXX) and 3/3.3V Vcc (MT4LCXXXXX) versions

DRAM

512K x 8 DRAM

FAST PAGE MODE

FEATURES

- Industry standard x8 pinouts, timing, functions and packages
- Address entry: 10 row addresses, nine column addresses
- High-performance, CMOS silicon-gate process
- Single +5V ±10% power supply
- Low power, 3mW standby; 350mW active, typical
- All device pins are fully TTL compatible
- 1,024-cycle refresh in 16ms
- Refresh modes: $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$ (CBR) and HIDDEN
- Optional FAST PAGE MODE access cycle
- NONPERSISTENT MASKED WRITE access cycle (MT4C8513 only)

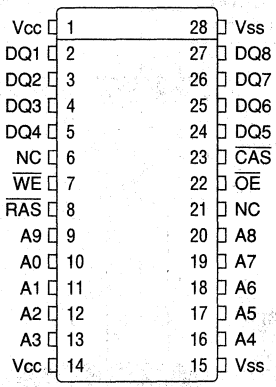
OPTIONS

	MARKING
• Timing	
70ns access	- 7
80ns access	- 8
100ns access	-10
• Masked Write	
Not available	MT4C8512
Available	MT4C8513
• Packages	
Plastic SOJ (400 mil)	DJ
Plastic TSOP (400 mil)	TG
Plastic ZIP (375 mil)	Z

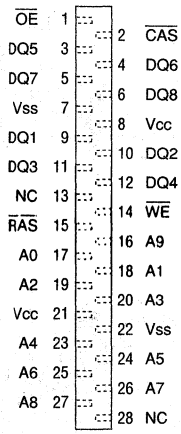
NOTE: Available in die form. Please consult factory for die data sheets.

PIN ASSIGNMENT (Top View)

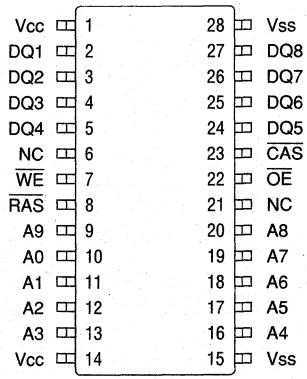
28-Pin SOJ (Q-4)



28-Pin ZIP (O-3)



28-Pin TSOP (R-3)



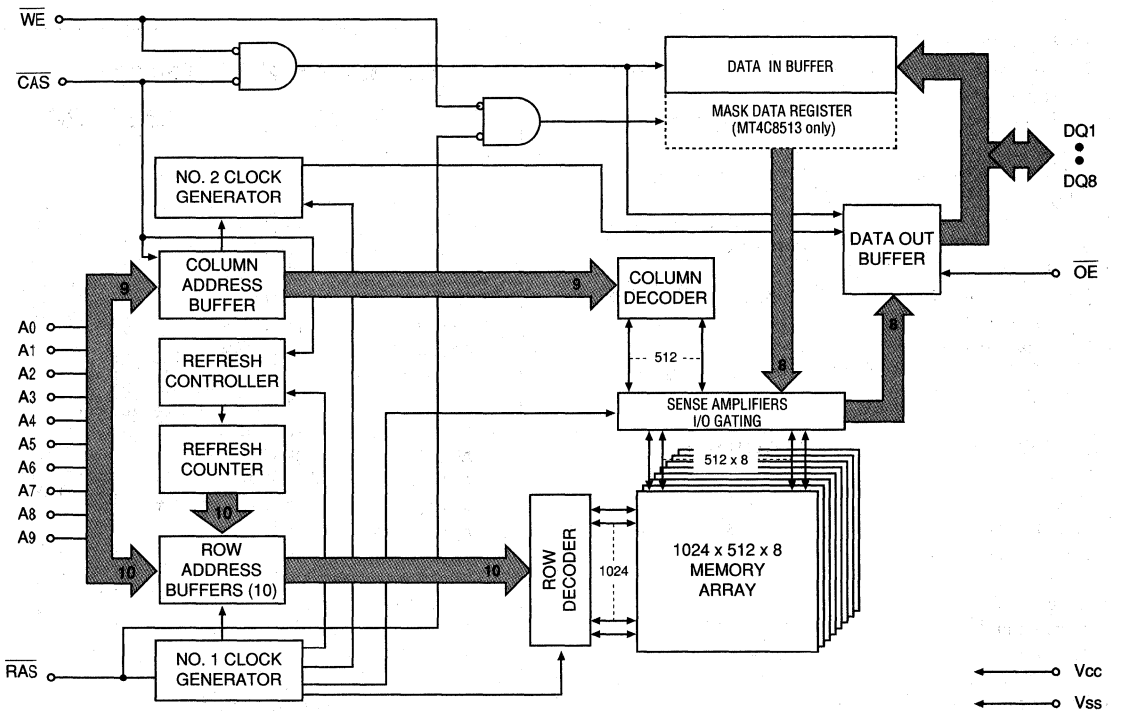
GENERAL DESCRIPTION

The MT4C8512/3 are randomly accessed solid-state memories containing 4,194,304 bits organized in a x8 configuration. Each byte is uniquely addressed through the 19 address bits during READ or WRITE cycles. The address is entered first by $\overline{RAS}$ latching 10 bits (A0-A9) and then $\overline{CAS}$ latching 9 bits (A0-A8).

The MT4C8513 has NONPERSISTENT MASKED WRITE allowing it to perform WRITE-PER-BIT accesses.

WIDE DRAM

FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTIONS

SOJ/TSOP PIN NUMBERS	ZIP PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
8	15	$\overline{RAS}$	Input	Row Address Strobe: $\overline{RAS}$ is used to clock-in the 10 row-address bits and strobe the $\overline{WE}$ and DQs in the MASKED WRITE mode (MT4C8513 only).
23	2	$\overline{CAS}$	Input	Column Address Strobe: $\overline{CAS}$ is used to clock-in the 9 column-address bits, enable the DRAM output buffers, and strobe the data inputs on WRITE cycles.
7	14	$\overline{WE}$	Input	Write Enable: $\overline{WE}$ is used to select a READ ($\overline{WE}$ = HIGH) or WRITE ($\overline{WE}$ = LOW) cycle. $\overline{WE}$ also serves as a Mask Enable ($\overline{WE}$ = LOW) at the falling edge of $\overline{RAS}$ in a MASKED-WRITE cycle (MT4C8513).
22	1	$\overline{OE}$	Input	Output Enable: $\overline{OE}$ enables the output buffers when taken LOW during a READ access cycle. $\overline{RAS}$ and $\overline{CAS}$ must be LOW and $\overline{WE}$ must be HIGH before $\overline{OE}$ will control the output buffers. Otherwise the output buffers are in a High-Z state.
10-13, 16-20, 9	17, 18, 19, 20, 23, 24, 25, 26, 27, 16	A0-A9	Input	Address Inputs: These inputs are multiplexed and clocked by $\overline{RAS}$ and $\overline{CAS}$ to select one byte out of the 512K available words.
2-5, 24-27	9, 10, 11, 12, 3, 4, 5, 6	DQ1-DQ8	Input	Data I/O: Includes inputs, outputs or High-Z and/or Output masked data input (for MASKED WRITE cycle only).
6, 21	13, 28	NC	-	No Connect: These pins should be either left unconnected or tied to ground.
1, 14	8, 21	V_{CC}	Supply	Power Supply: +5V ±10%
15, 28	7, 22	V_{SS}	Supply	Ground

FUNCTIONAL DESCRIPTION

Each bit is uniquely addressed through the 19 address bits during READ or WRITE cycles. First $\overline{RAS}$ is used to latch 10 bits (A0-A9) then $\overline{CAS}$ latches 9 bits (A0-A8).

The $\overline{CAS}$ control also determines whether the cycle will be a refresh cycle ($\overline{RAS}$-ONLY) or an active cycle (READ, WRITE or READ-WRITE) once $\overline{RAS}$ goes LOW.

READ or WRITE cycles are selected by $\overline{WE}$. A logic HIGH on $\overline{WE}$ dictates READ mode while a logic LOW on $\overline{WE}$ dictates WRITE mode. During a WRITE cycle, data in (D) is latched by the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. Taking $\overline{WE}$ LOW will initiate a WRITE cycle, selecting DQ1 through DQ8. If $\overline{WE}$ goes LOW prior to $\overline{CAS}$ going LOW, the output pin(s) remain open (High-Z) until the next $\overline{CAS}$ cycle. If $\overline{WE}$ goes LOW after $\overline{CAS}$ goes LOW and data reaches the output pins, data out (Q) is activated and retains the selected cell data as long as $\overline{CAS}$ and $\overline{OE}$ remain LOW (regardless of $\overline{WE}$ or $\overline{RAS}$). This late $\overline{WE}$ pulse results in a READ-WRITE cycle.

The eight data inputs and eight data outputs are routed through eight pins using common I/O, and pin direction is controlled by $\overline{OE}$ and $\overline{WE}$.

FAST PAGE MODE operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row address (A0-A9) defined page boundary. The FAST PAGE MODE cycle is always initiated with a row address strobed-in by $\overline{RAS}$ followed by a column address strobed-in by $\overline{CAS}$. $\overline{CAS}$ may be toggled-in by holding $\overline{RAS}$ LOW and strobing-in different column addresses, thus executing faster memory cycles. Returning $\overline{RAS}$ HIGH terminates the FAST PAGE MODE operation.

Returning $\overline{RAS}$ and $\overline{CAS}$ HIGH terminates a memory cycle and decreases chip current to a reduced standby level. The chip is also preconditioned for the next cycle during the $\overline{RAS}$ high time. Memory cell data is retained in its correct state by maintaining power and executing any $\overline{RAS}$ cycle (READ, WRITE, $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$, or HIDDEN REFRESH) so that all 1,024 combinations of $\overline{RAS}$ addresses (A0-A9) are executed at least every 16ms, regardless of sequence. The $\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh cycle will also invoke the refresh counter and controller for row address control.

MASKED WRITE ACCESS CYCLE (MT4C8513 ONLY)

Every WRITE access cycle can be a MASKED WRITE, depending on the state of $\overline{WE}$ at $\overline{RAS}$ time. A MASKED WRITE is selected when $\overline{WE}$ is LOW at $\overline{RAS}$ time and mask data is supplied on the DQ pins.

The mask data present on the DQ1-DQ8 inputs at $\overline{RAS}$ time will be written to an internal mask data register and will then act as an individual write enable for each of the corresponding DQ inputs. If a LOW (logic "0") is written to a mask data register bit, the input port for that bit is disabled during the subsequent WRITE operation and no new data will be written to that DRAM cell location. A HIGH (logic "1") on a mask data register bit enables the input port and allows normal WRITE operations to proceed. At $\overline{CAS}$ time, the bits present on the DQ1-DQ8 inputs will be either written to the DRAM (if the mask data bit was HIGH) or ignored (if the mask data bit was LOW).

In nonpersistent MASKED WRITEs, new mask data must be supplied each time a MASKED WRITE cycle is initiated.

Figure 1 illustrates the MT4C8513 MASKED WRITE operation (Note: $\overline{RAS}$ or $\overline{CAS}$ time refers to the time at which $\overline{RAS}$ or $\overline{CAS}$ transition from HIGH to LOW).

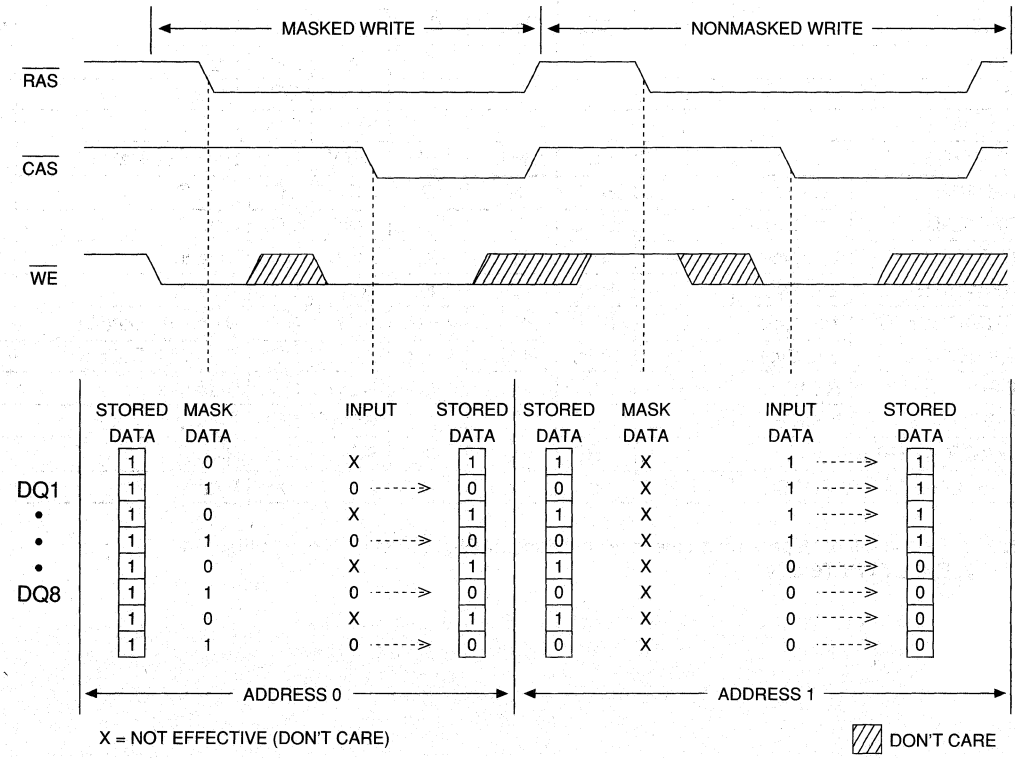


Figure 1
MT4C8513 MASKED WRITE EXAMPLE

TRUTH TABLE

FUNCTION		RAS	CAS	WE	OE	ADDRESSES tR	ADDRESSES tC	DQs	NOTES
Standby		H	H→X	X	X	X	X	High-Z	
READ		L	L	H	L	ROW	COL	Data Out	
EARLY-WRITE		L	L	L	X	ROW	COL	Data In	1
READ-WRITE		L	L	H→L	L→H	ROW	COL	Data Out, Data In	1
FAST-PAGE-	1st Cycle	L	H→L	H	L	ROW	COL	Data Out	
MODE READ	2nd Cycle	L	H→L	H	L	n/a	COL	Data Out	
FAST-PAGE-	1st Cycle	L	H→L	L	X	ROW	COL	Data In	1
MODE WRITE	2nd Cycle	L	H→L	L	X	n/a	COL	Data In	1
FAST-PAGE-MODE	1st Cycle	L	H→L	H→L	L→H	ROW	COL	Data Out, Data In	1
READ-WRITE	2nd Cycle	L	H→L	H→L	L→H	n/a	COL	Data Out, Data In	1
HIDDEN	READ	L→H→L	L	H	L	ROW	COL	Data Out	
REFRESH	WRITE	L→H→L	L	L	X	ROW	COL	Data In	1, 2
RAS-ONLY REFRESH		L	H	X	X	ROW	n/a	High-Z	
CAS-BEFORE-RAS REFRESH		H→L	L	H	X	X	X	High-Z	

NOTE: 1. Data in will be dependent on the mask provided (MT4C8513 only). Refer to Figure 1.
2. EARLY WRITE only.

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS} ..... -1V to +7V
Operating Temperature, T_A (Ambient) ..... 0°C to +70°C
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 3, 4, 6, 7) (0°C ≤ T_A ≤ 70°C; V_{CC} = 5V ±10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.5	V	1
Input High (Logic 1) Voltage, All Inputs	V_{IH}	2.4	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, All Inputs	V_{IL}	-1.0	0.8	V	1
INPUT LEAKAGE CURRENT Any Input 0V ≤ V_{IN} ≤ V_{CC} (All other pins not under test = 0V)	I_I	-2	2	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled, 0V ≤ V_{OUT} ≤ 5.5V)	I_{OZ}	-10	10	µA	
OUTPUT LEVELS Output High Voltage (I_{OUT} = -5mA)	V_{OH}	2.4		V	
Output Low Voltage (I_{OUT} = 4.2mA)	V_{OL}		0.4	V	

		MAX				
PARAMETER/CONDITION	SYMBOL	-7	-8	-10	UNITS	NOTES
STANDBY CURRENT: TTL ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC1}	2	2	2	mA	
STANDBY CURRENT: CMOS ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} -0.2V)	I_{CC2}	1	1	1	mA	25
OPERATING CURRENT: Random READ/WRITE Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC (MIN))	I_{CC3}	110	100	90	mA	3, 4, 30
OPERATING CURRENT: FAST PAGE MODE Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: ^tPC = ^tPC (MIN); ^tCP, ^tASC = 10ns)	I_{CC4}	90	80	70	mA	3, 4, 30
REFRESH CURRENT: $\overline{RAS}$-ONLY Average power supply current ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}: ^tRC = ^tRC (MIN))	I_{CC5}	110	100	90	mA	3, 30
REFRESH CURRENT: $\overline{CAS}$-BEFORE-$\overline{RAS}$ Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC (MIN))	I_{CC6}	110	100	90	mA	3

CAPACITANCE

PARAMETER	SYMBOL	MAX	UNITS	NOTES
Input Capacitance: A0-A9	C_{I1}	5	pF	2
Input Capacitance: $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$	C_{I2}	7	pF	2
Input/Output Capacitance: DQ	C_{IO}	7	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C ≤ T_A ≤ +70°C; V_{CC} = 5V ±10%)

AC CHARACTERISTICS		-7		-8		-10			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	t_{RC}	130		150		180		ns	
READ-WRITE cycle time	t_{RWC}	180		200		245		ns	
FAST-PAGE-MODE READ or WRITE cycle time	t_{PC}	45		50		55		ns	
FAST-PAGE-MODE READ-WRITE cycle time	t_{PRWC}	95		100		110		ns	
Access time from $\overline{RAS}$	t_{RAC}		70		80		100	ns	14
Access time from $\overline{CAS}$	t_{CAC}		20		20		25	ns	15
Output Enable time	t_{OE}		20		20		25	ns	
Access time from column address	t_{AA}		35		40		45	ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		40		45		55	ns	
$\overline{RAS}$ pulse width	t_{RAS}	70	100,000	80	100,000	100	100,000	ns	
$\overline{RAS}$ pulse width (FAST PAGE MODE)	t_{RASP}	70	100,000	80	100,000	100	100,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	20		20		25		ns	
$\overline{RAS}$ precharge time	t_{RP}	50		60		70		ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	100,000	20	100,000	25	100,000	ns	
$\overline{CAS}$ hold time	t_{CSH}	70		80		100		ns	
$\overline{CAS}$ precharge time	t_{CPN}	10		10		10		ns	16
$\overline{CAS}$ precharge time (FAST PAGE MODE)	t_{CP}	10		10		10		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	50	20	60	25	75	ns	17
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		10		10		ns	
Row address setup time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	10		10		15		ns	
$\overline{RAS}$ to column address delay time	t_{RAD}	15	35	15	40	20	55	ns	18
Column address setup time	t_{ASC}	0		0		0		ns	
Column address hold time	t_{CAH}	15		15		20		ns	
Column address hold time (referenced to $\overline{RAS}$)	t_{AR}	55		60		75		ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	35		40		55		ns	
Read command setup time	t_{RCS}	0		0		0		ns	26
Read command hold time (referenced to $\overline{CAS}$)	t_{RCH}	0		0		0		ns	19, 26
Read command hold time (referenced to $\overline{RAS}$)	t_{RRH}	0		0		0		ns	19
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	0		0		0		ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C ≤ T_A ≤ +70°C; Vcc = 5V ±10%)

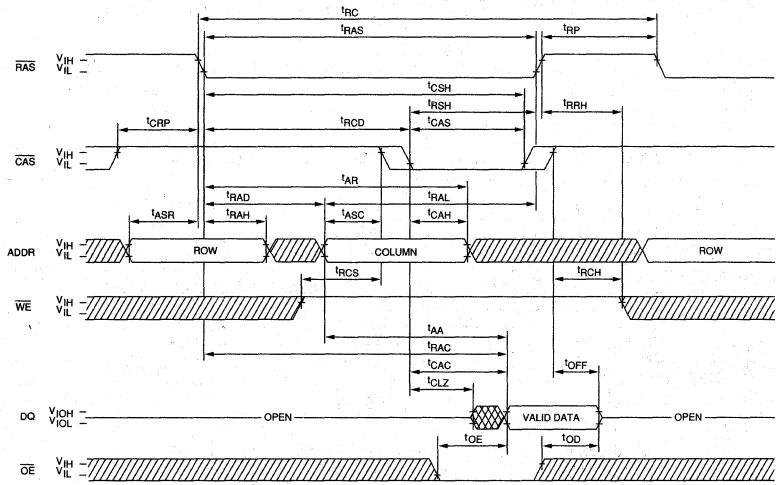
AC CHARACTERISTICS		-7		-8		-10			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Output buffer turn-off delay	tOFF	0	15	0	15	0	20	ns	20, 29
Output disable time	tOD		15		15		20	ns	29
Write command setup time	tWCS	0		0		0		ns	21, 26
Write command hold time	tWCH	15		15		20		ns	26
Write command hold time (referenced to $\overline{RAS}$)	tWCR	55		60		75		ns	26
Write command pulse width	tWP	10		10		20		ns	26
Write command to $\overline{RAS}$ lead time	tRWL	20		20		25		ns	26
Write command to $\overline{CAS}$ lead time	tCWL	20		20		25		ns	26
Data-in setup time	tDS	0		0		0		ns	22
Data-in hold time	tDH	15		15		20		ns	22
Data-in hold time (referenced to $\overline{RAS}$)	tDHR	55		60		75		ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	tRWD	95		105		135		ns	21
Column address to $\overline{WE}$ delay time	tAWD	60		65		80		ns	21
$\overline{CAS}$ to $\overline{WE}$ delay time	tCWD	45		45		60		ns	21
Transition time (rise or fall)	tT	3	50	3	50	3	50	ns	9, 10
Refresh period (1,024 cycles)	tREF		16		16		16	ms	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	tRPC	10		10		10		ns	
$\overline{CAS}$ setup time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	tCSR	10		10		10		ns	5
$\overline{CAS}$ hold time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	tCHR	10		10		10		ns	5
MASKED WRITE command to $\overline{RAS}$ setup time	tWRS	0		0		0		ns	26
$\overline{WE}$ setup time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	tWRP	10		10		10		ns	26
$\overline{WE}$ hold time to $\overline{RAS}$ (MASKED WRITE and $\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	tWRH	15		15		15		ns	26
Mask data to $\overline{RAS}$ setup time	tMS	0		0		0		ns	26, 27
Mask data to $\overline{RAS}$ hold time	tMH	15		15		15		ns	26, 27
$\overline{OE}$ hold time from $\overline{WE}$ during READ-MODIFY-WRITE cycle	tOEH	20		25		25		ns	28
$\overline{OE}$ setup prior to $\overline{RAS}$ during HIDDEN REFRESH cycle	tORD	0		0		0		ns	

WIDE DRAM

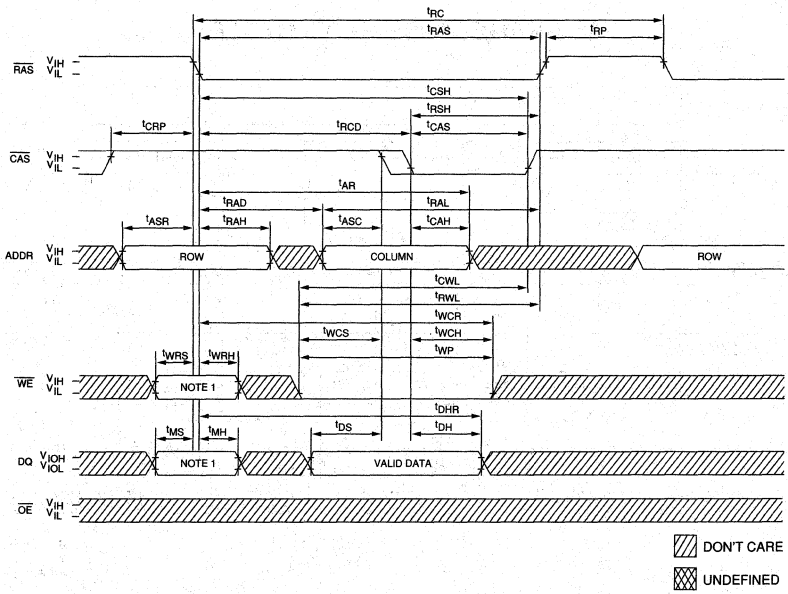
NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. V_{CC} = 5V ±10%, f = 1 MHz.
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \le T_A \le 70°C$) is assured.
7. An initial pause of 100µs is required after power-up followed by eight $\overline{RAS}$ refresh cycles ($\overline{RAS}$-ONLY or CBR) before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-up should be repeated any time the ^tREF refresh requirement is exceeded.
8. AC characteristics assume ^tT = 5ns.
9. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS}$ = V_{IH}, data output is high impedance.
12. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to 2 TTL gate and 100pF.
14. Assumes that $^tRCD < ^tRCD$ (MAX). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
15. Assumes that $^tRCD \ge ^tRCD$ (MAX).
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the Q buffer, $\overline{CAS}$ must be pulsed HIGH for ^tCPN.
17. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (MAX) limit, then access time is controlled exclusively by ^tCAC.
18. Operation within the ^tRAD limit ensures that ^tRCD (MAX) can be met. ^tRAD (MAX) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (MAX) limit, then access time is controlled exclusively by ^tAA.
19. Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
20. ^tOFF (MAX) defines the time at which the output achieves the open circuit condition, not a reference to V_{OH} or V_{OL}.
21. ^tWCS, ^tRWD, ^tAWD and ^tCWD are restrictive operating parameters in LATE-WRITE and READ-MODIFY-WRITE cycles only. If $^tWCS \ge ^tWCS$ (MIN), the cycle is an EARLY-WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If $^tRWD \ge ^tRWD$ (MIN), $^tAWD \ge ^tAWD$ (MIN) and $^tCWD \ge ^tCWD$ (MIN), the cycle is a READ-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of data out are indeterminate. $\overline{OE}$ held HIGH and $\overline{WE}$ taken LOW after $\overline{CAS}$ goes LOW results in a LATE-WRITE ($\overline{OE}$ controlled) cycle.
22. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY-WRITE cycles and $\overline{WE}$ leading edge in LATE-WRITE or READ-MODIFY-WRITE cycles.
23. During a READ cycle, if $\overline{OE}$ is LOW then taken HIGH before $\overline{CAS}$ goes HIGH, Q goes open. If $\overline{OE}$ is tied permanently LOW, LATE-WRITE or READ-MODIFY-WRITE operations are not possible.
24. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case $\overline{WE}$ = LOW and $\overline{OE}$ = HIGH.
25. All other inputs at Vcc -0.2V.
26. Write command is defined as $\overline{WE}$ going LOW.
27. MT4C8513 only.
28. LATE-WRITE and READ-MODIFY-WRITE cycles must have both ^tOD and ^tOEH met ($\overline{OE}$ HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. The DQs will provide the previously read data if $\overline{CAS}$ remains LOW and $\overline{OE}$ is taken back LOW after ^tOEH is met. If $\overline{CAS}$ goes HIGH prior to $\overline{OE}$ going back LOW, the DQs will remain open.
29. The DQs open during READ cycles once ^tOD or ^tOFF occur. If $\overline{CAS}$ goes HIGH first, $\overline{OE}$ becomes a "don't care." If $\overline{OE}$ goes HIGH and $\overline{CAS}$ stays LOW, $\overline{OE}$ is not a don't care; and the DQs will provide the previously read data if $\overline{OE}$ is taken back LOW (while $\overline{CAS}$ remains LOW).
30. Column address changed once while $\overline{RAS}$ = V_{IL} and $\overline{CAS}$ = V_{IH}.

READ CYCLE

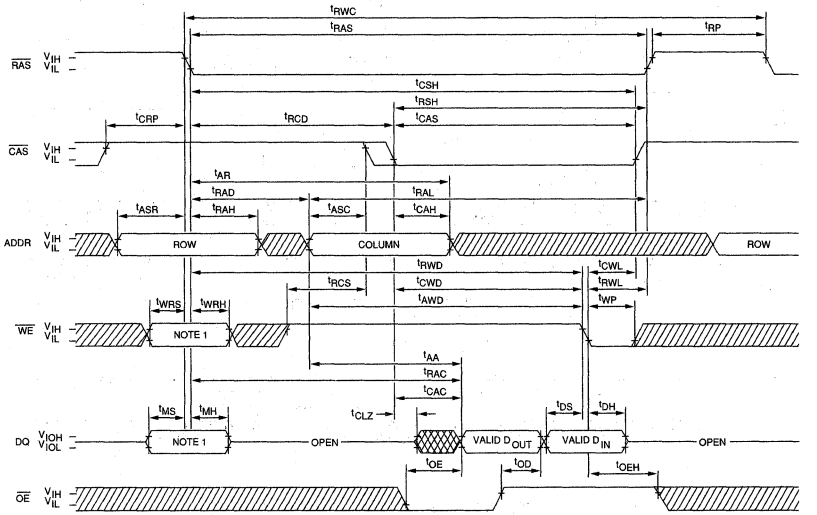


EARLY-WRITE CYCLE

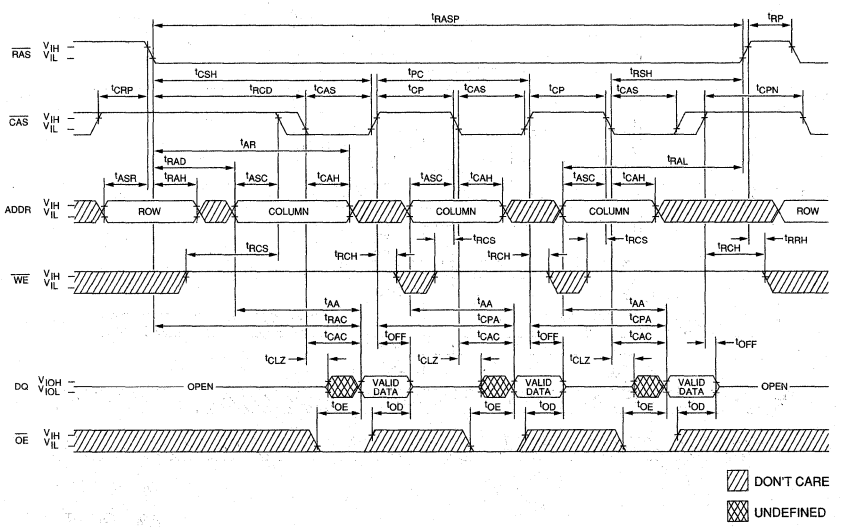


NOTE: 1. Applies to MT4C8513 only; $\overline{WE}$ and DQ inputs on MT4C8512 are "don't care" at $\overline{RAS}$ time. $\overline{WE}$ selects between normal WRITE and MASKED WRITE at $\overline{RAS}$ time. The DQ inputs are "don't care" for a normal WRITE ($\overline{WE}$ HIGH at $\overline{RAS}$ time). The DQ inputs provide the mask data at $\overline{RAS}$ time for a MASKED WRITE, $\overline{WE}$ LOW at $\overline{RAS}$ time.

READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)

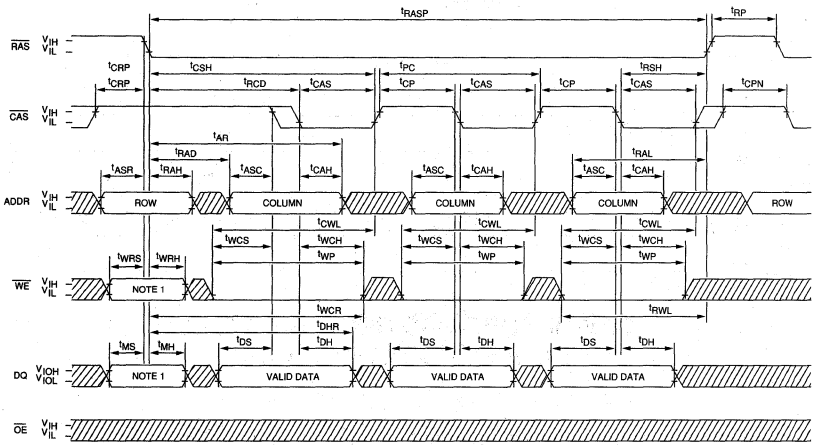


FAST-PAGE-MODE READ CYCLE

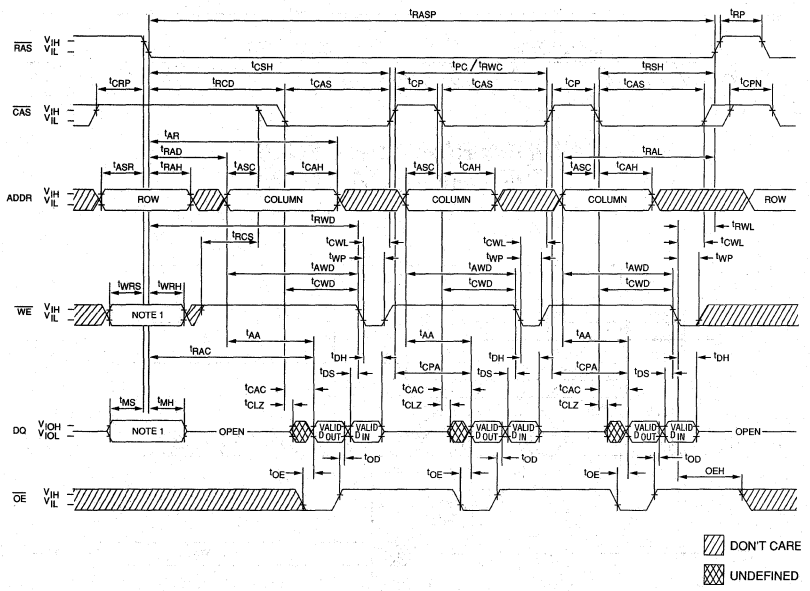


NOTE: 1. Applies to MT4C8513 only; $\overline{WE}$ and DQ inputs on MT4C8512 are "don't care" at $\overline{RAS}$ time. $\overline{WE}$ selects between normal WRITE and MASKED WRITE at $\overline{RAS}$ time. The DQ inputs are "don't care" for a normal WRITE ($\overline{WE}$ HIGH at $\overline{RAS}$ time). The DQ inputs provide the mask data at $\overline{RAS}$ time for a MASKED WRITE, $\overline{WE}$ LOW at $\overline{RAS}$ time.

FAST-PAGE-MODE EARLY-WRITE CYCLE



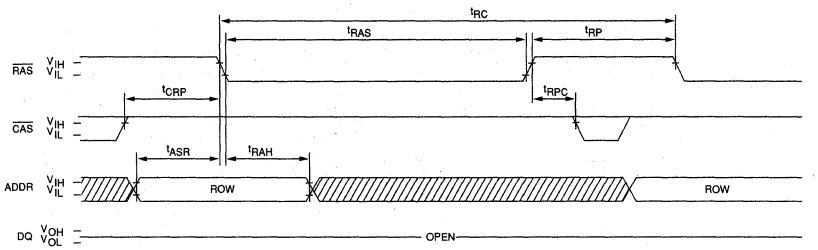
FAST-PAGE-MODE READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)



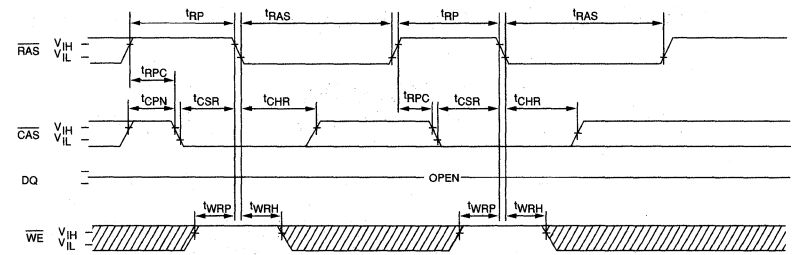
NOTE: 1. Applies to MT4C8513 only; $\overline{WE}$ and DQ inputs on MT4C8512 are "don't care" at $\overline{RAS}$ time. $\overline{WE}$ selects between normal WRITE and MASKED WRITE at $\overline{RAS}$ time. The DQ inputs are "don't care" for a normal WRITE ($\overline{WE}$ HIGH at $\overline{RAS}$ time). The DQ inputs provide the mask data at $\overline{RAS}$ time for a MASKED WRITE, $\overline{WE}$ LOW at $\overline{RAS}$ time.

WIDE DRAM

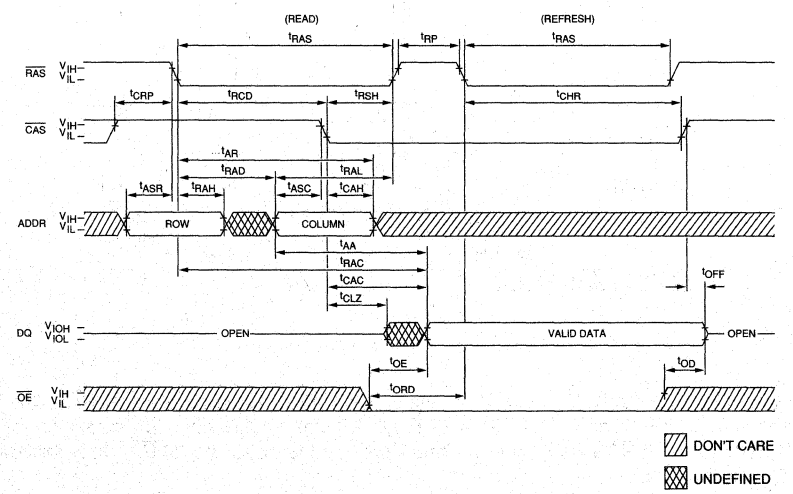
RAS-ONLY REFRESH CYCLE
(OE and WE = DON'T CARE)



CAS-BEFORE-RAS REFRESH CYCLE
(A0-A9; OE = DON'T CARE)



HIDDEN REFRESH CYCLE [24]
(WE = HIGH; OE = LOW)



NEW ■ WIDE DRAM

DRAM

512K x 8 DRAM

LOW POWER, EXTENDED REFRESH

FEATURES

- Industry standard x8 pinouts, timing, functions and packages
- Address entry: 10 row addresses, nine column addresses
- High-performance, CMOS silicon-gate process
- Single +5V ±10% power supply
- All device pins are fully TTL compatible
- Refresh modes: $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$ (CBR), HIDDEN and BATTERY BACKUP (BBU)
- Optional FAST PAGE MODE access cycle
- NONPERSISTENT MASKED WRITE access cycle (MT4C8513 only)
- 1,024-cycle refresh distributed accross 128ms
- Low-power, 1mW standby; 350mW active, typical

OPTIONS — MARKING

- Timing

70ns access	- 7
80ns access	- 8
100ns access	-10

- Masked Write

Not available	MT4C8512 L
Available	MT4C8513 L

- Packages

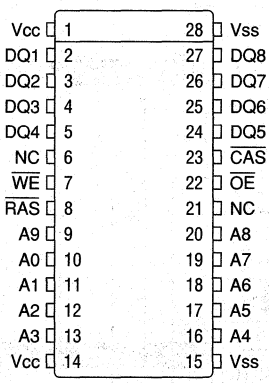
Plastic SOJ (400 mil)	DJ
Plastic TSOP (400 mil)	TG
Plastic ZIP (375 mil)	Z

NOTE: Available in die form. Please consult factory for die data sheets.

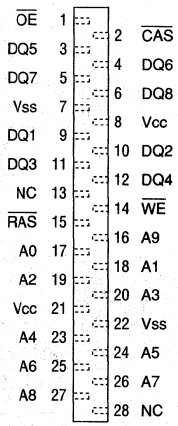
- Part number example: MT4C8512DJ-7 L

PIN ASSIGNMENT (Top View)

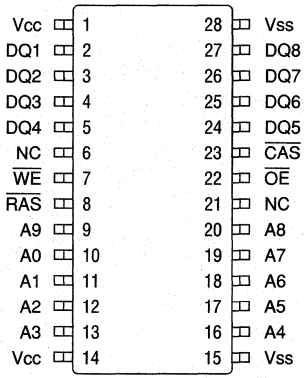
28-Pin SOJ
(Q-4)



28-Pin ZIP
(O-3)



28-Pin TSOP
(R-3)



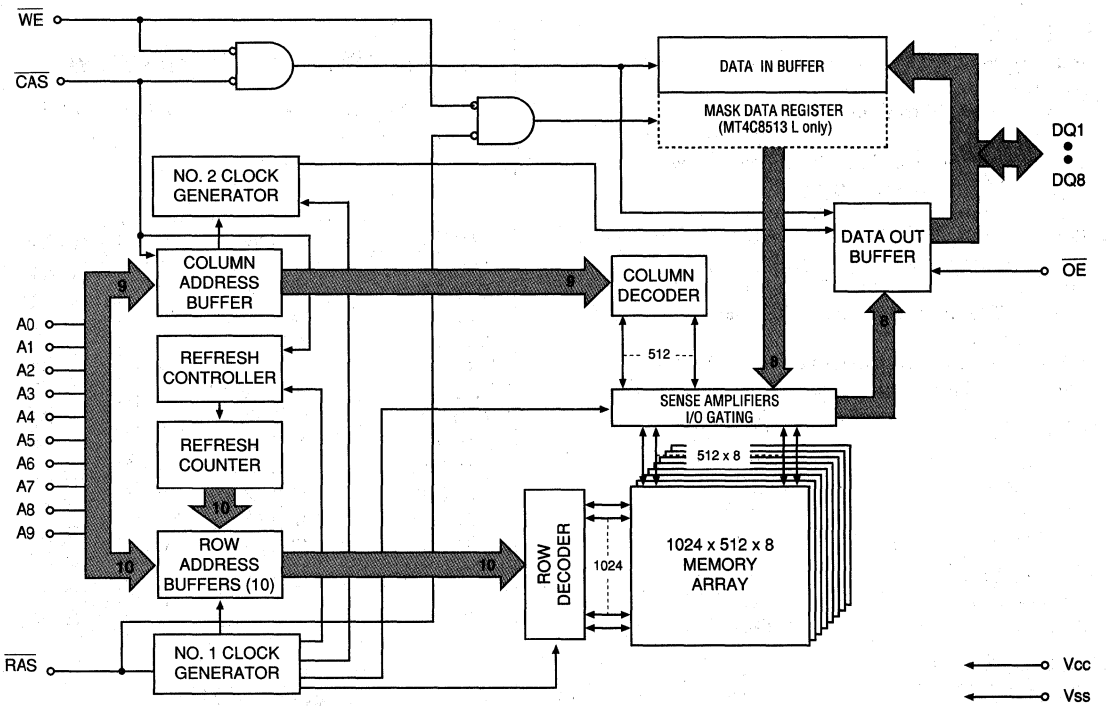
GENERAL DESCRIPTION

The MT4C8512/3 L are randomly accessed solid-state memories containing 4,194,304 bits organized in a x8 configuration. Each byte is uniquely addressed through the 19 address bits during $\overline{READ}$ or WRITE cycles. The address is entered first by $\overline{RAS}$ latching 10 bits (A0-A9) and then $\overline{CAS}$ latching 9 bits (A0-A8).

The MT4C8513 L has NONPERSISTENT MASKED WRITE allowing it to perform WRITE-PER-BIT accesses.

NEW ■ WIDE DRAM

FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTIONS

SOJ/TSOP PIN NUMBERS	ZIP PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
8	15	$\overline{RAS}$	Input	Row Address Strobe: $\overline{RAS}$ is used to clock-in the 10 row-address bits and strobe the $\overline{WE}$ and DQs in the MASKED WRITE mode (MT4C8513 L only).
23	2	$\overline{CAS}$	Input	Column Address Strobe: $\overline{CAS}$ is used to clock-in the 9 column-address bits, enable the DRAM output buffers, and strobe the data inputs on WRITE cycles.
7	14	$\overline{WE}$	Input	Write Enable: $\overline{WE}$ is used to select a READ ($\overline{WE}$ = HIGH) or WRITE ($\overline{WE}$ = LOW) cycle. $\overline{WE}$ also serves as a Mask Enable ($\overline{WE}$ = LOW) at the falling edge of $\overline{RAS}$ in a MASKED-WRITE cycle (MT4C8513 L).
22	1	$\overline{OE}$	Input	Output Enable: $\overline{OE}$ enables the output buffers when taken LOW during a READ access cycle. $\overline{RAS}$ and $\overline{CAS}$ must be LOW and $\overline{WE}$ must be HIGH before $\overline{OE}$ will control the output buffers. Otherwise the output buffers are in a High-Z state.
10-13, 16-20, 9	17, 18, 19, 20, 23, 24, 25, 26, 27, 16	A0-A9	Input	Address Inputs: These inputs are multiplexed and clocked by $\overline{RAS}$ and $\overline{CAS}$ to select one byte out of the 512K available words.
2-5, 24-27	9, 10, 11, 12, 3, 4, 5, 6	DQ1-DQ8	Input	Data I/O: Includes inputs, outputs or High-Z and/or Output masked data input (for MASKED WRITE cycle only).
6, 21	13, 28	NC	-	No Connect: These pins should be either left unconnected or tied to ground.
1, 14	8, 21	V_{CC}	Supply	Power Supply: +5V ±10%
15, 28	7, 22	V_{SS}	Supply	Ground

NEW ■ WIDE DRAM

FUNCTIONAL DESCRIPTION

Each bit is uniquely addressed through the 19 address bits during READ or WRITE cycles. First $\overline{RAS}$ is used to latch 10 bits (A0-A9) then $\overline{CAS}$ latches 9 bits (A0-A8).

The $\overline{CAS}$ control also determines whether the cycle will be a refresh cycle ($\overline{RAS}$-ONLY) or an active cycle (READ, WRITE or READ-WRITE) once $\overline{RAS}$ goes LOW.

READ or WRITE cycles are selected by $\overline{WE}$. A logic HIGH on $\overline{WE}$ dictates READ mode while a logic LOW on $\overline{WE}$ dictates WRITE mode. During a WRITE cycle, data in (D) is latched by the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. Taking $\overline{WE}$ LOW will initiate a WRITE cycle, selecting DQ1 through DQ8. If $\overline{WE}$ goes LOW prior to $\overline{CAS}$ going LOW, the output pin(s) remain open (High-Z) until the next $\overline{CAS}$ cycle. If $\overline{WE}$ goes LOW after $\overline{CAS}$ goes LOW and data reaches the output pins, data out (Q) is activated and retains the selected cell data as long as $\overline{CAS}$ and $\overline{OE}$ remain LOW (regardless of $\overline{WE}$ or $\overline{RAS}$). This late $\overline{WE}$ pulse results in a READ-WRITE cycle.

The eight data inputs and eight data outputs are routed through eight pins using common I/O, and pin direction is controlled by $\overline{OE}$ and $\overline{WE}$.

FAST PAGE MODE operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row address (A0-A9) defined page boundary. The FAST PAGE MODE cycle is always initiated with a row address strobed-in by $\overline{RAS}$ followed by a column address strobed-in by $\overline{CAS}$. $\overline{CAS}$ may be toggled-in by holding $\overline{RAS}$ LOW and strobing-in different column addresses, thus executing faster memory cycles. Returning $\overline{RAS}$ HIGH terminates the FAST PAGE MODE operation.

Returning $\overline{RAS}$ and $\overline{CAS}$ HIGH terminates a memory cycle and decreases chip current to a reduced standby level. The chip is also preconditioned for the next cycle during the $\overline{RAS}$ high time. Memory cell data is retained in its correct state by maintaining power and executing any $\overline{RAS}$ cycle (READ, WRITE, $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$, or HIDDEN REFRESH) so that all 1,024 combinations of $\overline{RAS}$ addresses (A0-A9) are executed at least every 16ms, regardless of sequence. The $\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh cycle will also invoke the refresh counter and controller for row address control.

BATTERY BACKUP MODE (BBU) is a CBR refresh performed at the extended refresh rate with CMOS input levels. This mode provides a very low current, data retention cycle. $\overline{RAS}$ or $\overline{CAS}$ time refers to the time at which $\overline{RAS}$ or $\overline{CAS}$ transition from HIGH to LOW).

MASKED WRITE ACCESS CYCLE (MT4C8513 L ONLY)

Every WRITE access cycle can be a MASKED WRITE, depending on the state of $\overline{WE}$ at $\overline{RAS}$ time. A MASKED WRITE is selected when $\overline{WE}$ is LOW at $\overline{RAS}$ time and mask data is supplied on the DQ pins.

The mask data present on the DQ1-DQ8 inputs at $\overline{RAS}$ time will be written to an internal mask data register and will then act as an individual write enable for each of the corresponding DQ inputs. If a LOW (logic "0") is written to a mask data register bit, the input port for that bit is disabled during the subsequent WRITE operation and no new data will be written to that DRAM cell location. A HIGH (logic "1") on a mask data register bit enables the input port and allows normal WRITE operations to proceed. At $\overline{CAS}$ time, the bits present on the DQ1-DQ8 inputs will be either written to the DRAM (if the mask data bit was HIGH) or ignored (if the mask data bit was LOW).

In nonpersistent MASKED WRITEs, new mask data must be supplied each time a MASKED WRITE cycle is initiated.

Figure 1 illustrates the MT4C8513 L MASKED WRITE operation (Note: $\overline{RAS}$ or $\overline{CAS}$ time refers to the time at which $\overline{RAS}$ or $\overline{CAS}$ transition from HIGH to LOW).

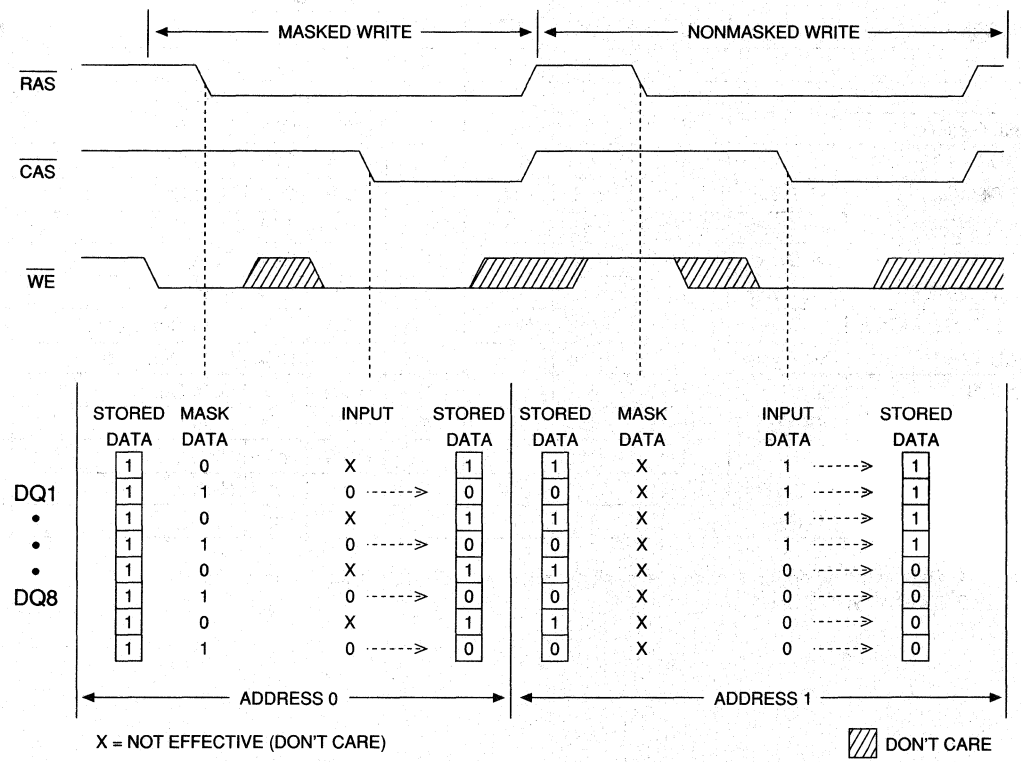


Figure 1
MT4C8513 L MASKED WRITE EXAMPLE

TRUTH TABLE

FUNCTION		RAS	CAS	WE	OE	ADDRESSES tR	ADDRESSES tC	DQs	NOTES
Standby		H	H→X	X	X	X	X	High-Z	
READ		L	L	H	L	ROW	COL	Data Out	
EARLY-WRITE		L	L	L	X	ROW	COL	Data In	1
READ-WRITE		L	L	H→L	L→H	ROW	COL	Data Out, Data In	1
FAST-PAGE-	1st Cycle	L	H→L	H	L	ROW	COL	Data Out	
MODE READ	2nd Cycle	L	H→L	H	L	n/a	COL	Data Out	
FAST-PAGE-	1st Cycle	L	H→L	L	X	ROW	COL	Data In	1
MODE WRITE	2nd Cycle	L	H→L	L	X	n/a	COL	Data In	1
FAST-PAGE-MODE	1st Cycle	L	H→L	H→L	L→H	ROW	COL	Data Out, Data In	1
READ-WRITE	2nd Cycle	L	H→L	H→L	L→H	n/a	COL	Data Out, Data In	1
HIDDEN	READ	L→H→L	L	H	L	ROW	COL	Data Out	
REFRESH	WRITE	L→H→L	L	L	X	ROW	COL	Data In	1, 2
RAS-ONLY REFRESH		L	H	X	X	ROW	n/a	High-Z	
CAS-BEFORE-RAS REFRESH		H→L	L	H	X	X	X	High-Z	
BATTERY BACKUP REFRESH		H→L	L	H	X	X	X	High-Z	

NOTE: 1. Data in will be dependent on the mask provided (MT4C8513 L only). Refer to Figure 1.
2. EARLY WRITE only.

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS} ..... -1V to +7V
Operating Temperature, T_A (Ambient) ..... 0°C to +70°C
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 3, 4, 6, 7) (0°C ≤ T_A ≤ 70°C; V_{CC} = 5V ±10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.5	V	1
Input High (Logic 1) Voltage, All Inputs	V_{IH}	2.4	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, All Inputs	V_{IL}	-1.0	0.8	V	1
INPUT LEAKAGE CURRENT Any Input 0V ≤ V_{IN} ≤ Vcc (All other pins not under test = 0V)	I_I	-2	2	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled, 0V ≤ V_{OUT} ≤ 5.5V)	I_{OZ}	-10	10	µA	
OUTPUT LEVELS Output High Voltage (I_{OUT} = -5mA)	V_{OH}	2.4		V	
Output Low Voltage (I_{OUT} = 4.2mA)	V_{OL}		0.4	V	

		MAX				
PARAMETER/CONDITION	SYMBOL	-7	-8	-10	UNITS	NOTES
STANDBY CURRENT: TTL ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC1}	2	2	2	mA	
STANDBY CURRENT: CMOS ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} -0.2V)	I_{CC2}	200	200	200	µA	25
OPERATING CURRENT: Random READ/WRITE Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC (MIN))	I_{CC3}	110	100	90	mA	3, 4, 31
OPERATING CURRENT: FAST PAGE MODE Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: ^tPC = ^tPC (MIN); ^tCP, ^tASC = 10ns)	I_{CC4}	90	80	70	mA	3, 4, 31
REFRESH CURRENT: $\overline{RAS}$-ONLY Average power supply current ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}: ^tRC = ^tRC (MIN))	I_{CC5}	110	100	90	mA	3, 31
REFRESH CURRENT: $\overline{CAS}$-BEFORE-$\overline{RAS}$ Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC (MIN))	I_{CC6}	110	100	90	mA	3
REFRESH CURRENT: BATTERY BACKUP (BBU) Average power supply current during BATTERY BACKUP refresh: $\overline{CAS}$ = 0.2V or $\overline{CAS}$-BEFORE-$\overline{RAS}$ cycling; $\overline{RAS}$ = ^tRAS (MIN) to 300ns; $\overline{WE}$, A0-A9 and D_{IN} = V_{CC} - 0.2V (D_{IN} may be left open), ^tRC = 125µs (1,024 rows at 125µs = 128ms)	I_{CC7}	300	300	300	µA	3, 5, 30

CAPACITANCE

PARAMETER	SYMBOL	MAX	UNITS	NOTES
Input Capacitance: A0-A9	C_{I1}	5	pF	2
Input Capacitance: $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$	C_{I2}	7	pF	2
Input/Output Capacitance: DQ	C_{IO}	7	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) ($0°C \le T_A \le +70°C$; V_{CC} = 5V ±10%)

AC CHARACTERISTICS		-7		-8		-10			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	t_{RC}	130		150		180		ns	
READ-WRITE cycle time	t_{RWC}	180		200		245		ns	
FAST-PAGE-MODE READ or WRITE cycle time	t_{PC}	45		50		55		ns	
FAST-PAGE-MODE READ-WRITE cycle time	t_{PRWC}	95		100		110		ns	
Access time from $\overline{RAS}$	t_{RAC}		70		80		100	ns	14
Access time from $\overline{CAS}$	t_{CAC}		20		20		25	ns	15
Output Enable time	t_{OE}		20		20		25	ns	
Access time from column address	t_{AA}		35		40		45	ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		40		45		55	ns	
$\overline{RAS}$ pulse width	t_{RAS}	70	100,000	80	100,000	100	100,000	ns	
$\overline{RAS}$ pulse width (FAST PAGE MODE)	t_{RASP}	70	100,000	80	100,000	100	100,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	20		20		25		ns	
$\overline{RAS}$ precharge time	t_{RP}	50		60		70		ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	100,000	20	100,000	25	100,000	ns	
$\overline{CAS}$ hold time	t_{CSH}	70		80		100		ns	
$\overline{CAS}$ precharge time	t_{CPN}	10		10		10		ns	16
$\overline{CAS}$ precharge time (FAST PAGE MODE)	t_{CP}	10		10		10		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	50	20	60	25	75	ns	17
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		10		10		ns	
Row address setup time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	10		10		15		ns	
$\overline{RAS}$ to column address delay time	t_{RAD}	15	35	15	40	20	55	ns	18
Column address setup time	t_{ASC}	0		0		0		ns	
Column address hold time	t_{CAH}	15		15		20		ns	
Column address hold time (referenced to $\overline{RAS}$)	t_{AR}	55		60		75		ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	35		40		55		ns	
Read command setup time	t_{RCS}	0		0		0		ns	26
Read command hold time (referenced to $\overline{CAS}$)	t_{RCH}	0		0		0		ns	19, 26
Read command hold time (referenced to $\overline{RAS}$)	t_{RRH}	0		0		0		ns	19
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	0		0		0		ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

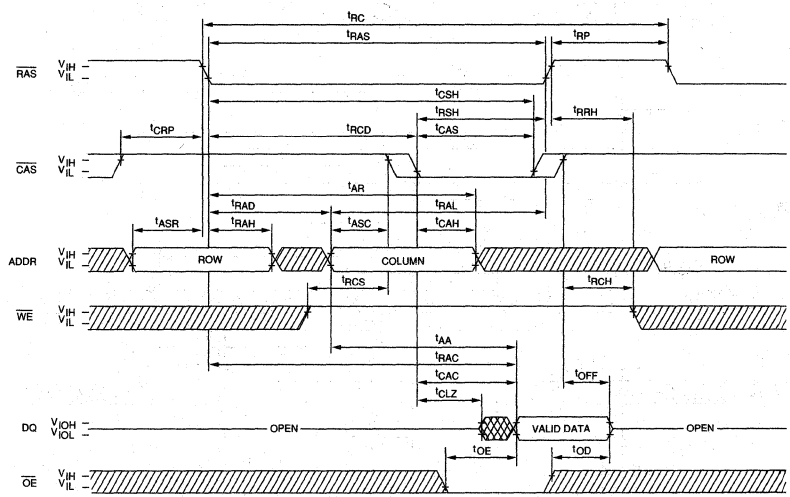
(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C ≤ T_A ≤ +70°C; Vcc = 5V ±10%)

AC CHARACTERISTICS		-7		-8		-10			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Output buffer turn-off delay	tOFF	0	15	0	15	0	20	ns	20, 29
Output disable time	tOD		15		15		20	ns	29
Write command setup time	tWCS	0		0		0		ns	21, 26
Write command hold time	tWCH	15		15		20		ns	26
Write command hold time (referenced to $\overline{RAS}$)	tWCR	55		60		75		ns	26
Write command pulse width	tWP	10		10		20		ns	26
Write command to $\overline{RAS}$ lead time	tRWL	20		20		25		ns	26
Write command to $\overline{CAS}$ lead time	tCWL	20		20		25		ns	26
Data-in setup time	tDS	0		0		0		ns	22
Data-in hold time	tDH	15		15		20		ns	22
Data-in hold time (referenced to $\overline{RAS}$)	tDHR	55		60		75		ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	tRWD	95		105		135		ns	21
Column address to $\overline{WE}$ delay time	tAWD	60		65		80		ns	21
$\overline{CAS}$ to $\overline{WE}$ delay time	tCWD	45		45		60		ns	21
Transition time (rise or fall)	tT	3	50	3	50	3	50	ns	9, 10
Refresh period (1,024 cycles)	tREF		128		128		128	ms	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	tRPC	10		10		10		ns	
$\overline{CAS}$ setup time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	tCSR	10		10		10		ns	5
$\overline{CAS}$ hold time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	tCHR	10		10		10		ns	5
MASKED WRITE command to $\overline{RAS}$ setup time	tWRS	0		0		0		ns	26
$\overline{WE}$ setup time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	tWRP	10		10		10		ns	26
$\overline{WE}$ hold time to $\overline{RAS}$ (MASKED WRITE and $\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	tWRH	15		15		15		ns	26
Mask data to $\overline{RAS}$ setup time	tMS	0		0		0		ns	26, 27
Mask data to $\overline{RAS}$ hold time	tMH	15		15		15		ns	26, 27
$\overline{OE}$ hold time from $\overline{WE}$ during READ-MODIFY-WRITE cycle	tOEH	20		25		25		ns	28
$\overline{OE}$ setup prior to $\overline{RAS}$ during HIDDEN REFRESH cycle	tORD	0		0		0		ns	

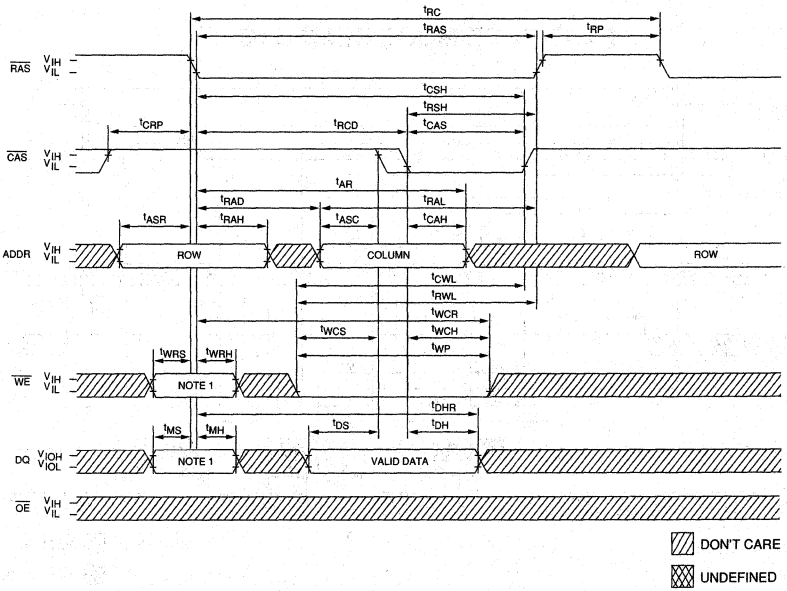
NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. V_{CC} = 5V ±10%, f = 1 MHz.
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \le T_A \le 70°C$) is assured.
7. An initial pause of 100µs is required after power-up followed by eight $\overline{RAS}$ refresh cycles ($\overline{RAS}$ -ONLY or CBR) before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-up should be repeated any time the ^tREF refresh requirement is exceeded.
8. AC characteristics assume ^tT = 5ns.
9. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS}$ = V_{IH}, data output is high impedance.
12. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to 2 TTL gate and 100pF.
14. Assumes that $^tRCD < {}^tRCD$ (MAX). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
15. Assumes that $^tRCD \ge {}^tRCD$ (MAX).
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the Q buffer, $\overline{CAS}$ must be pulsed HIGH for ^tCPN.
17. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (MAX) limit, then access time is controlled exclusively by ^tCAC.
18. Operation within the ^tRAD limit ensures that ^tRCD (MAX) can be met. ^tRAD (MAX) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (MAX) limit, then access time is controlled exclusively by ^tAA.
19. Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
20. ^tOFF (MAX) defines the time at which the output achieves the open circuit condition, not a reference to V_{OH} or V_{OL}.
21. ^tWCS, ^tRWD, ^tAWD and ^tCWD are restrictive operating parameters in LATE-WRITE and READ-MODIFY-WRITE cycles only. If $^tWCS \ge {}^tWCS$ (MIN), the cycle is an EARLY-WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If $^tRWD \ge {}^tRWD$ (MIN), $^tAWD \ge {}^tAWD$ (MIN) and $^tCWD \ge {}^tCWD$ (MIN), the cycle is a READ-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of data out are indeterminate. $\overline{OE}$ held HIGH and $\overline{WE}$ taken LOW after $\overline{CAS}$ goes LOW results in a LATE-WRITE ($\overline{OE}$ controlled) cycle.
22. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY-WRITE cycles and $\overline{WE}$ leading edge in LATE-WRITE or READ-MODIFY-WRITE cycles.
23. During a READ cycle, if $\overline{OE}$ is LOW then taken HIGH before $\overline{CAS}$ goes HIGH, Q goes open. If $\overline{OE}$ is tied permanently LOW, LATE-WRITE or READ-MODIFY-WRITE operations are not possible.
24. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case $\overline{WE}$ = LOW and $\overline{OE}$ = HIGH.
25. All other inputs at Vcc -0.2V.
26. Write command is defined as $\overline{WE}$ going LOW.
27. MT4C8513 L only.
28. LATE-WRITE and READ-MODIFY-WRITE cycles must have both ^tOD and ^tOEH met ($\overline{OE}$ HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. The DQs will provide the previously read data if $\overline{CAS}$ remains LOW and $\overline{OE}$ is taken back LOW after ^tOEH is met. If $\overline{CAS}$ goes HIGH prior to $\overline{OE}$ going back LOW, the DQs will remain open.
29. The DQs open during READ cycles once ^tOD or ^tOFF occur. If $\overline{CAS}$ goes HIGH first, $\overline{OE}$ becomes a "don't care." If $\overline{OE}$ goes HIGH and $\overline{CAS}$ stays LOW, $\overline{OE}$ is not a don't care; and the DQs will provide the previously read data if $\overline{OE}$ is taken back LOW (while $\overline{CAS}$ remains LOW).
30. BBU current is reduced as ^tRAS is reduced from its maximum specification during BBU cycle.
31. Column address changed once while $\overline{RAS}$ = V_{IL} and $\overline{CAS}$ = V_{IH}.

READ CYCLE

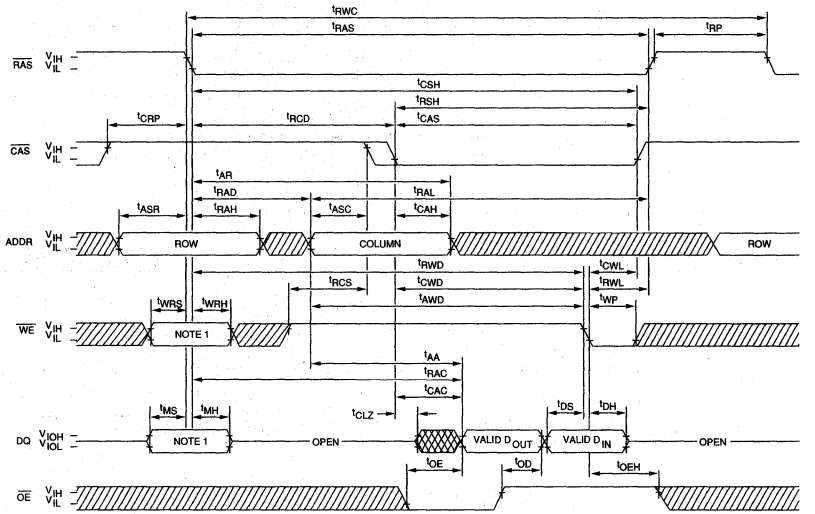


EARLY-WRITE CYCLE

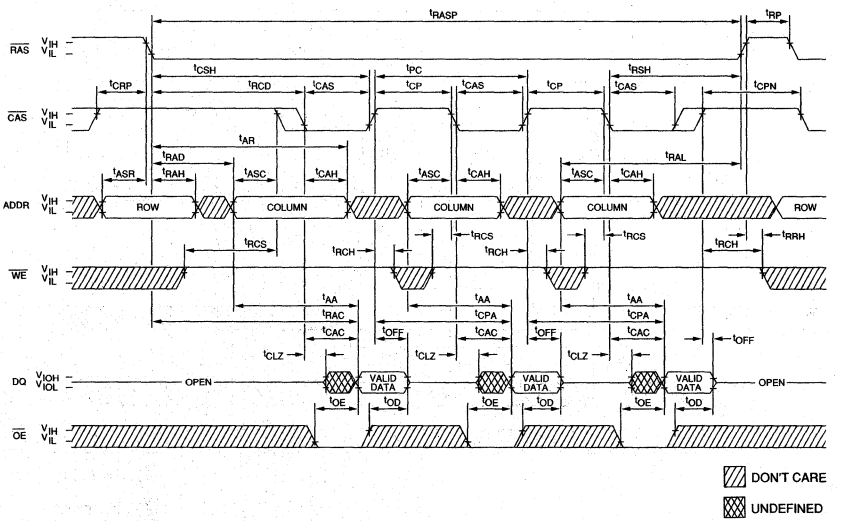


NOTE: 1. Applies to MT4C8513 L only; $\overline{WE}$ and DQ inputs on MT4C8512 L are "don't care" at $\overline{RAS}$ time. $\overline{WE}$ selects between normal WRITE and MASKED WRITE at $\overline{RAS}$ time. The DQ inputs are "don't care" for a normal WRITE ($\overline{WE}$ HIGH at $\overline{RAS}$ time). The DQ inputs provide the mask data at $\overline{RAS}$ time for a MASKED WRITE, $\overline{WE}$ LOW at $\overline{RAS}$ time.

READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)

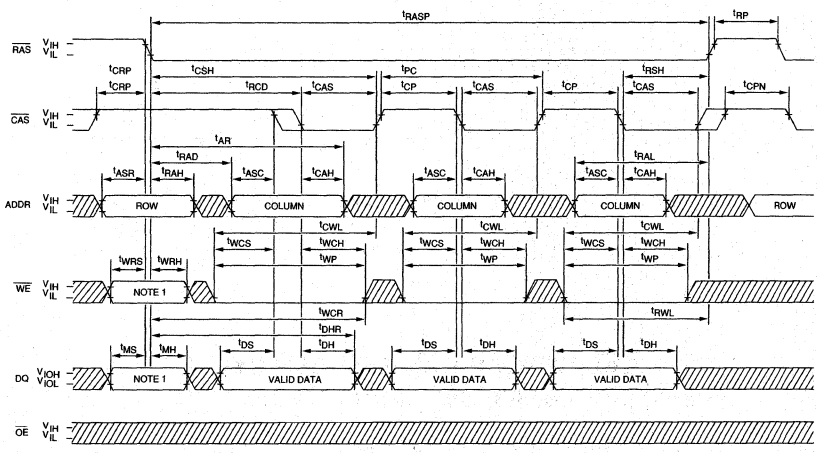


FAST-PAGE-MODE READ CYCLE

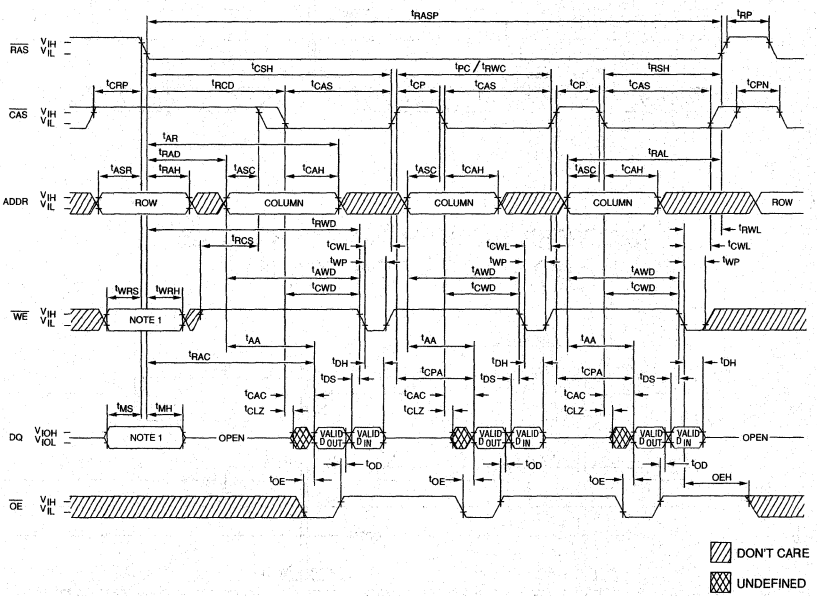


NOTE: 1. Applies to MT4C8513 L only; $\overline{WE}$ and DQ inputs on MT4C8512 L are "don't care" at $\overline{RAS}$ time. $\overline{WE}$ selects between normal WRITE and MASKED WRITE at $\overline{RAS}$ time. The DQ inputs are "don't care" for a normal WRITE ($\overline{WE}$ HIGH at $\overline{RAS}$ time). The DQ inputs provide the mask data at $\overline{RAS}$ time for a MASKED WRITE, $\overline{WE}$ LOW at $\overline{RAS}$ time.

FAST-PAGE-MODE EARLY-WRITE CYCLE

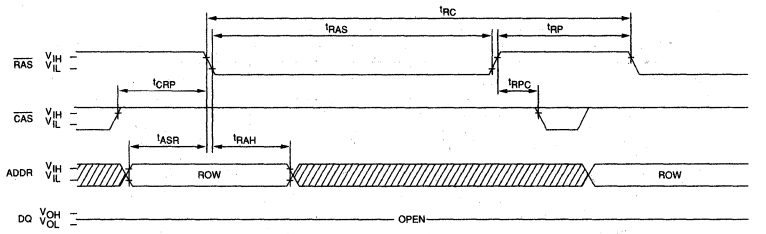


FAST-PAGE-MODE READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)

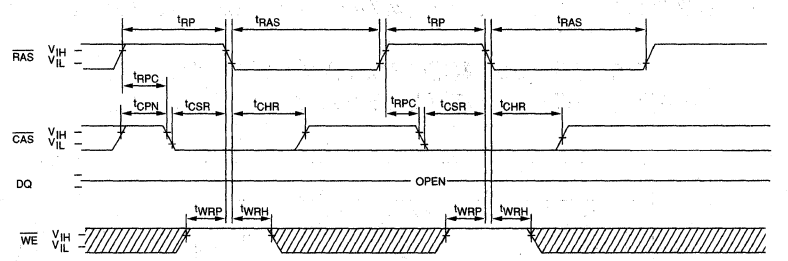


NOTE: 1. Applies to MT4C8513 L only; $\overline{WE}$ and DQ inputs on MT4C8512 L are "don't care" at $\overline{RAS}$ time. $\overline{WE}$ selects between normal WRITE and MASKED WRITE at $\overline{RAS}$ time. The DQ inputs are "don't care" for a normal WRITE ($\overline{WE}$ HIGH at $\overline{RAS}$ time). The DQ inputs provide the mask data at $\overline{RAS}$ time for a MASKED WRITE, $\overline{WE}$ LOW at $\overline{RAS}$ time.

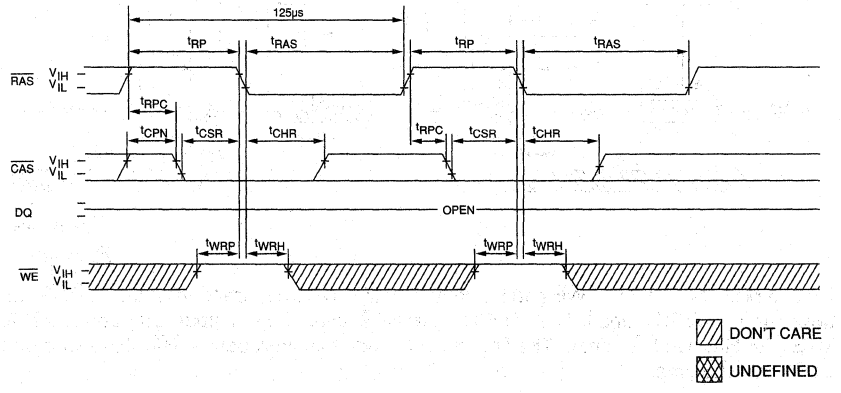
RAS-ONLY REFRESH CYCLE
(OE and WE = DON'T CARE)



CAS-BEFORE-RAS REFRESH CYCLE
(A0-A9; OE = DON'T CARE)

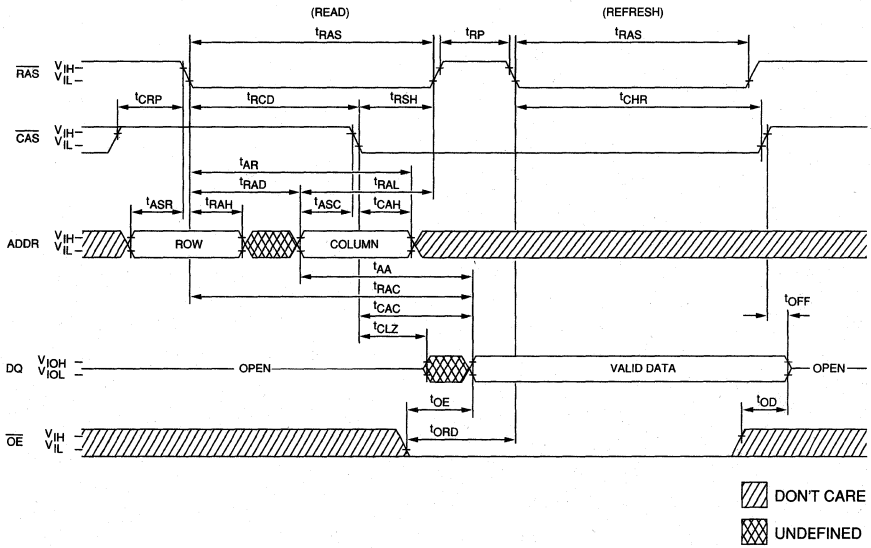


BATTERY BACKUP REFRESH CYCLE
(A0-A9; OE = DON'T CARE)



HIDDEN REFRESH CYCLE [24]

($\overline{WE}$ = HIGH; $\overline{OE}$ = LOW)



NEW ■ WIDE DRAM

DRAM

2 MEG x 8 DRAM

5.0V, FAST PAGE MODE (MT4C2M8A1/2)
3.0/3.3V, FAST PAGE MODE (MT4LC2M8A1/2)

FEATURES

- Industry standard x8 pinouts, timing, functions and packages
- Address entry: 12 row, nine column addresses (64ms)
- High-performance, CMOS silicon-gate process
- Single +5V only or 3.0/3.3V only ±10% power supply
- Low power, 5mW standby; 400mW active, typical (5V)
- All device pins are fully TTL compatible
- 4,096-cycle refresh (2,048-cycle refresh available as MT4(L)C2M8B1/2)
- Refresh modes: $\overline{\text{RAS}}$-ONLY, $\overline{\text{CAS}}$-BEFORE-$\overline{\text{RAS}}$ (CBR) and HIDDEN
- Optional FAST PAGE MODE access cycle
- NONPERSISTENT MASKED WRITE access cycle (MT4(L)C2M8A2 only)

OPTIONS MARKING

- Timing
  - 60ns access - 6
  - 70ns access - 7
  - 80ns access - 8
- Power Supply
  - 5V ±10% only 4C
  - 3.0/3.3V ±10% only 4LC
- Masked Write
  - Not available A1
  - Available A2
- Packages
  - Plastic 28-pin SOJ (400 mil) DJ
  - Plastic 28-pin TSOP (400 mil) TG
  - Plastic 32-pin SOJ (400 mil) DL
  - Plastic 32-pin TSOP (400 mil) TL

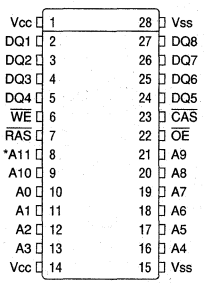
NOTE: Available in die form. Please consult factory for die data sheets.

PART DESCRIPTION

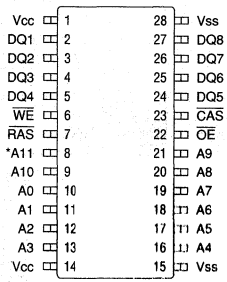
MT4C2M8A1	5V, non-masked write
MT4C2M8A2	5V, masked write
MT4LC2M8A1	3.0/3.3V, non-masked write
MT4LC2M8A2	3.0/3.3V, masked write

PIN ASSIGNMENT (Top View)

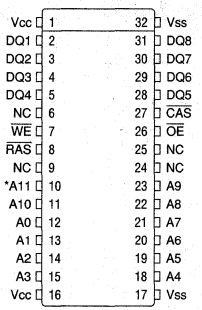
28-Pin SOJ (Q-4)



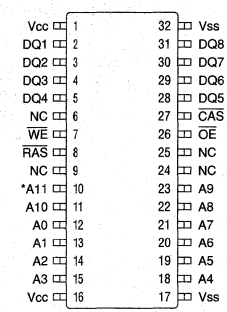
28-Pin TSOP (R-3)



32-Pin SOJ (Q-5)



32-Pin TSOP (R-4)



*NC on 11 row address version

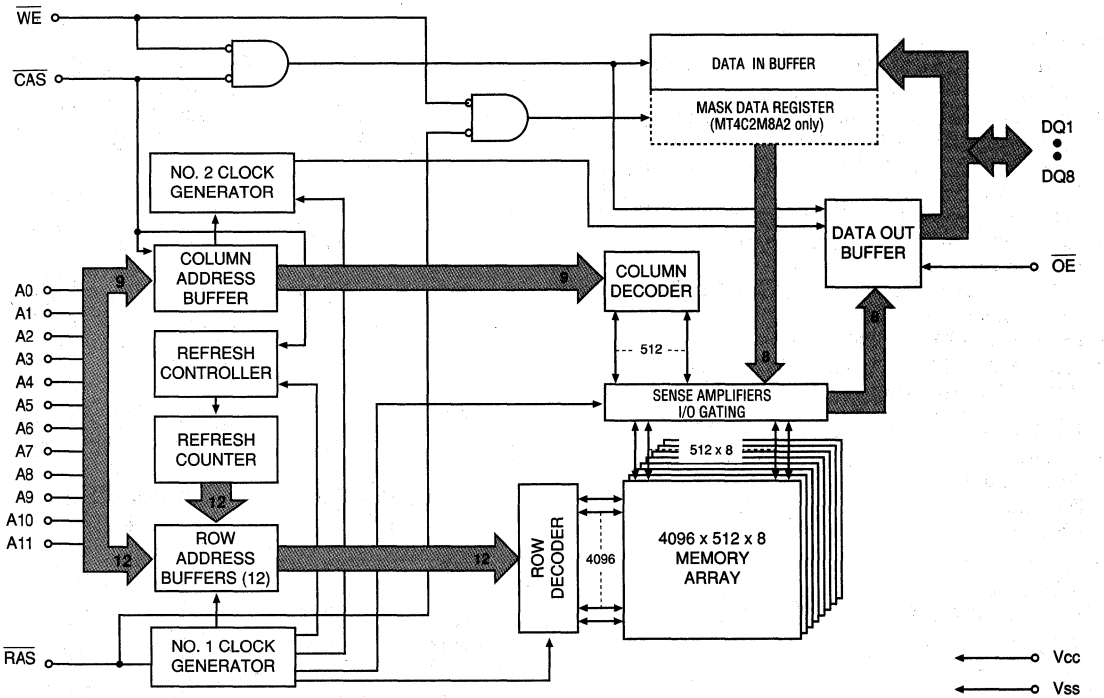
GENERAL DESCRIPTION

The MT4C2M8A1/2 and MT4LC2M8A1/2 are randomly accessed solid-state memories containing 16,777,216 bits organized in a x8 configuration. The MT4C2M8A1/2 and the MT4LC2M8A1/2 are the same DRAM versions except that the MT4LC2M8A1/2 are low voltage versions of the MT4C2M8A1/2. The MT4LC2M8A1/2 are designed to operate in either a 3.0V ±10% or a 3.3V ±10% memory system. All further references made for the MT4C2M8A1/2 also apply to the MT4LC2M8A1/2, unless specifically stated otherwise. Each byte is uniquely addressed through the 21 address bits during READ or WRITE cycles. The address is entered first by $\overline{\text{RAS}}$ latching 12 bits (A0-11) and then $\overline{\text{CAS}}$ latching 9 bits (A0-A9).

The MT4C2M8A2 has NONPERSISTENT MASKED WRITE, allowing it to perform WRITE-PER-BIT accesses.

NEW ■ WIDE DRAM

FUNCTIONAL BLOCK DIAGRAM
4,096 ROWS



PIN DESCRIPTIONS

28-PIN DEVICE PIN NUMBERS	32-PIN DEVICE PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
7	8	$\overline{RAS}$	Input	Row Address Strobe: $\overline{RAS}$ is used to clock-in the 12 row-address bits and strobe the $\overline{WE}$ and DQs in the MASKED WRITE mode (MT4C2M8A2 only).
23	27	$\overline{CAS}$	Input	Column Address Strobe: $\overline{CAS}$ is used to clock-in the 9 column-address bits, enable the DRAM output buffers, and strobe the data inputs on WRITE cycles.
6	7	$\overline{WE}$	Input	Write Enable: $\overline{WE}$ is used to select a READ ($\overline{WE}$ = HIGH) or WRITE ($\overline{WE}$ = LOW) cycle. $\overline{WE}$ also serves as a Mask Enable ($\overline{WE}$ = LOW) at the falling edge of $\overline{RAS}$ in a MASKED-WRITE cycle (MT4C2M8A2).
22	26	$\overline{OE}$	Input	Output Enable: $\overline{OE}$ enables the output buffers when taken LOW during a READ access cycle. $\overline{RAS}$ and $\overline{CAS}$ must be LOW and $\overline{WE}$ must be HIGH before $\overline{OE}$ will control the output buffers. Otherwise the output buffers are in a High-Z state.
10-13, 16-21, 9, 8	12-15, 18-23, 11, 10	A0-A11	Input	Address Inputs: These inputs are multiplexed and clocked by $\overline{RAS}$ and $\overline{CAS}$ to select one byte out of the 2 Meg available words.
2-5, 24-27	2-5, 28-31	DQ1-DQ8	Input	Data I/O: Includes inputs, outputs or High-Z and/or Output masked data input (for MASKED WRITE cycle only).
	6, 9, 24, 25	NC	-	No Connect: These pins should be either left unconnected or tied to ground.
1, 14	1, 16	V_{CC}	Supply	Power Supply: +5V ±10% (C), 3.0/3.3V ±10% (LC)
15, 28	17, 32	V_{SS}	Supply	Ground

NEW ■ WIDE DRAM

FUNCTIONAL DESCRIPTION

Each bit is uniquely addressed through the 21 address bits during READ or WRITE cycles. First $\overline{RAS}$ is used to latch 12 bits (A0-A11) then $\overline{CAS}$ latches 9 bits (A0-A8).

The $\overline{CAS}$ control also determines whether the cycle will be a refresh cycle ($\overline{RAS}$-ONLY) or an active cycle (READ, WRITE or READ-WRITE) once $\overline{RAS}$ goes LOW.

READ or WRITE cycles are selected by $\overline{WE}$. A logic HIGH on $\overline{WE}$ dictates READ mode while a logic LOW on $\overline{WE}$ dictates WRITE mode. During a WRITE cycle, data in (D) is latched by the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. Taking $\overline{WE}$ LOW will initiate a WRITE cycle, selecting DQ1 through DQ8. If $\overline{WE}$ goes LOW prior to $\overline{CAS}$ going LOW, the output pin(s) remain open (High-Z) until the next $\overline{CAS}$ cycle. If $\overline{WE}$ goes LOW after $\overline{CAS}$ goes LOW and data reaches the output pins, data out (Q) is activated and retains the selected cell data as long as $\overline{CAS}$ and $\overline{OE}$ remain LOW (regardless of $\overline{WE}$ or $\overline{RAS}$). This late $\overline{WE}$ pulse results in a READ-WRITE cycle.

The eight data inputs and eight data outputs are routed through eight pins using common I/O, and pin direction is controlled by $\overline{OE}$ and $\overline{WE}$.

FAST PAGE MODE operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row address (A0-12) defined page boundary. The FAST PAGE MODE cycle is always initiated with a row address strobed-in by $\overline{RAS}$ followed by a column address strobed-in by $\overline{CAS}$. $\overline{CAS}$ may be toggled-in by holding $\overline{RAS}$ LOW and strobing-in different column addresses, thus executing faster memory cycles. Returning $\overline{RAS}$ HIGH terminates the FAST PAGE MODE operation.

Returning $\overline{RAS}$ and $\overline{CAS}$ HIGH terminates a memory cycle and decreases chip current to a reduced standby level. The chip is also preconditioned for the next cycle during the $\overline{RAS}$ high time. Memory cell data is retained in its correct state by maintaining power and executing any $\overline{RAS}$ cycle (READ, WRITE, $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$, or HIDDEN REFRESH) so that all 4,096 combinations of $\overline{RAS}$ addresses (A0-11) are executed at least every 64ms, regardless of sequence. The $\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh cycle will also invoke the refresh counter and controller for row address control.

MASKED WRITE ACCESS CYCLE (MT4C2M8A2 ONLY)

Every WRITE access cycle can be a MASKED WRITE, depending on the state of $\overline{WE}$ at $\overline{RAS}$ time. A MASKED WRITE is selected when $\overline{WE}$ is LOW at $\overline{RAS}$ time and mask data is supplied on the DQ pins.

The mask data present on the DQ1-DQ8 inputs at $\overline{RAS}$ time will be written to an internal mask data register and will then act as an individual write enable for each of the corresponding DQ inputs. If a LOW (logic "0") is written to a mask data register bit, the input port for that bit is disabled during the subsequent WRITE operation and no new data will be written to that DRAM cell location. A HIGH (logic "1") on a mask data register bit enables the input port and allows normal WRITE operations to proceed. At $\overline{CAS}$ time, the bits present on the DQ1-DQ8 inputs will be written to the DRAM (if the mask data bit was HIGH) or ignored (if the mask data bit was LOW).

In nonpersistent MASKED WRITEs, new mask data must be supplied each time a MASKED WRITE cycle is initiated.

Figure 1 illustrates the MT4C2M8A2 MASKED WRITE operation (Note: $\overline{RAS}$ or $\overline{CAS}$ time refers to the time at which $\overline{RAS}$ or $\overline{CAS}$ transition from HIGH to LOW).

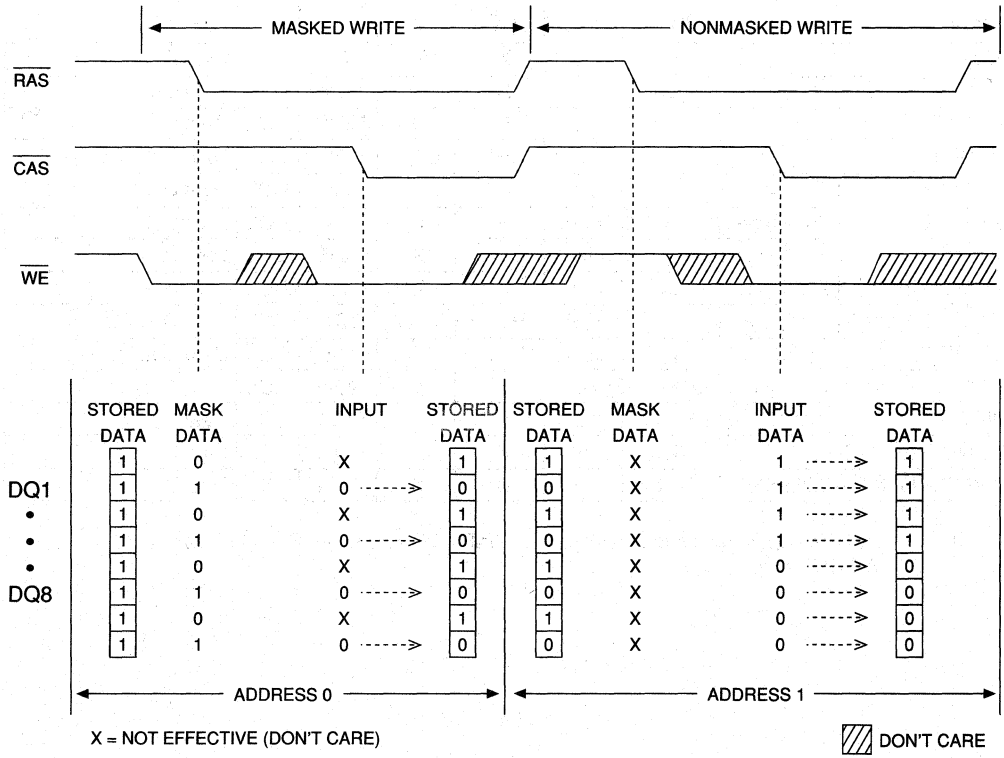


Figure 1
MT4C2M8A2 MASKED WRITE EXAMPLE

TRUTH TABLE

FUNCTION		RAS	CAS	WE	OE	ADDRESSES tR	ADDRESSES tC	DQs	NOTES
Standby		H	H→X	X	X	X	X	High-Z	
READ		L	L	H	L	ROW	COL	Data Out	
EARLY-WRITE		L	L	L	X	ROW	COL	Data In	1
READ-WRITE		L	L	H→L	L→H	ROW	COL	Data Out, Data In	1
FAST-PAGE-	1st Cycle	L	H→L	H	L	ROW	COL	Data Out	
MODE READ	2nd Cycle	L	H→L	H	L	n/a	COL	Data Out	
FAST-PAGE-	1st Cycle	L	H→L	L	X	ROW	COL	Data In	1
MODE WRITE	2nd Cycle	L	H→L	L	X	n/a	COL	Data In	1
FAST-PAGE-MODE	1st Cycle	L	H→L	H→L	L→H	ROW	COL	Data Out, Data In	1
READ-WRITE	2nd Cycle	L	H→L	H→L	L→H	n/a	COL	Data Out, Data In	1
HIDDEN	READ	L→H→L	L	H	L	ROW	COL	Data Out	
REFRESH	WRITE	L→H→L	L	L	X	ROW	COL	Data In	1, 2
RAS-ONLY REFRESH		L	H	X	X	ROW	n/a	High-Z	
CAS-BEFORE-RAS REFRESH		H→L	L	H	X	X	X	High-Z	

NOTE: 1. Data in will be dependent on the mask provided (MT4C2M8A2 only). Refer to Figure 1.
2. EARLY WRITE only.

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS} (5V) .....-1V to +7V
Voltage on V_{CC} supply relative to V_{SS} (3V) ....-1V to +4.6V
Operating Temperature, T_A (Ambient) .....0°C to +70°C
Storage Temperature (Plastic) .....-55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC OPERATING SPECIFICATIONS FOR 5V VERSION

(Notes: 1, 3, 4, 6, 7, 30) (0°C ≤ T_A ≤ 70°C; Vcc = 5V ±10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.5	V	1, 30
Input High (Logic 1) Voltage, All Inputs	V_{IH}	2.4	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, All Inputs	V_{IL}	-1.0	0.8	V	1
INPUT LEAKAGE CURRENT Any Input 0V ≤ V_{IN} ≤ Vcc (All other pins not under test = 0V)	I_I	-2	2	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled, 0V ≤ V_{OUT} ≤ 5.5V)	I_{OZ}	-10	10	µA	
OUTPUT LEVELS Output High Voltage (I_{OUT} = -2.5mA)	V_{OH}	2.4		V	
Output Low Voltage (I_{OUT} = 2.1mA)	V_{OL}		0.4	V	

DC OPERATING SPECIFICATIONS FOR 3.0/3.3V VERSION

(Notes: 1, 3, 4, 6, 7, 31) (0°C ≤ T_A ≤ 70°C; Vcc = 3.0/3.3V ±10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	2.7	3.6	V	1, 31
Input High (Logic 1) Voltage, All Inputs	V_{IH}	2.0	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, All Inputs	V_{IL}	-1.0	0.8	V	1
INPUT LEAKAGE CURRENT Any Input 0V ≤ V_{IN} ≤ Vcc (All other pins not under test = 0V)	I_I	-2	2	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled, 0V ≤ V_{OUT} ≤ 3.6V)	I_{OZ}	-10	10	µA	
OUTPUT LEVELS Output High Voltage (I_{OUT} = -2mA)	V_{OH}	2.4		V	
Output Low Voltage (I_{OUT} = 2mA)	V_{OL}		0.4	V	

DC OPERATING SPECIFICATIONS FOR 5V VERSION

(Notes: 1, 3, 4, 6, 7, 30) (0°C ≤ T_A ≤ 70°C; Vcc = 5V ±10%)

		MAX				
PARAMETER/CONDITION	**SYMBOL**	**-6**	**-7**	**-8**	**UNITS**	**NOTES**
STANDBY CURRENT: TTL ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC1}	2	2	2	mA	
STANDBY CURRENT: CMOS ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} -0.2V)	I_{CC2}	1	1	1	mA	25
OPERATING CURRENT: Random READ/WRITE Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC (MIN))	I_{CC3}	110	100	90	mA	3, 4, 32
OPERATING CURRENT: FAST PAGE MODE Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: ^tPC = ^tPC (MIN); ^tCP, ^tASC = 10ns)	I_{CC4}	80	70	60	mA	3, 4, 32
REFRESH CURRENT: $\overline{RAS}$-ONLY Average power supply current ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}: ^tRC = ^tRC (MIN))	I_{CC5}	110	100	90	mA	3, 32
REFRESH CURRENT: $\overline{CAS}$-BEFORE-$\overline{RAS}$ Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC (MIN))	I_{CC6}	110	100	90	mA	3

DC OPERATING SPECIFICATIONS FOR 3.0/3.3V VERSION

(Notes: 1, 3, 4, 6, 7, 31) (0°C ≤ T_A ≤ 70°C; Vcc = 3.0/3.3V ±10%)

		MAX				
PARAMETER/CONDITION	**SYMBOL**	**-6**	**-7**	**-8**	**UNITS**	**NOTES**
STANDBY CURRENT: TTL ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC1}	1	1	1	mA	
STANDBY CURRENT: CMOS ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} -0.2V)	I_{CC2}	400	400	400	µA	25
OPERATING CURRENT: Random READ/WRITE Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC (MIN))	I_{CC3}	80	70	60	mA	3, 4, 32
OPERATING CURRENT: FAST PAGE MODE Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: ^tPC = ^tPC (MIN); ^tCP, ^tASC = 10ns)	I_{CC4}	60	50	40	mA	3, 4, 32
REFRESH CURRENT: $\overline{RAS}$-ONLY Average power supply current ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}: ^tRC = ^tRC (MIN))	I_{CC5}	80	70	60	mA	3, 32
REFRESH CURRENT: $\overline{CAS}$-BEFORE-$\overline{RAS}$ Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC (MIN))	I_{CC6}	80	70	60	mA	3

CAPACITANCE

PARAMETER	SYMBOL	MAX	UNITS	NOTES
Input Capacitance: A0-A11	C_{I1}	5	pF	2
Input Capacitance: $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$	C_{I2}	7	pF	2
Input/Output Capacitance: DQ	C_{IO}	7	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C ≤ T_A ≤ +70°C)

AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	^tRC	110		130		150		ns	
READ-WRITE cycle time	^tRWC	155		180		200		ns	
FAST-PAGE-MODE READ or WRITE cycle time	^tPC	35		40		40		ns	
FAST-PAGE-MODE READ-WRITE cycle time	^tPRWC	85		95		100		ns	
Access time from $\overline{RAS}$	^tRAC		60		70		80	ns	14
Access time from $\overline{CAS}$	^tCAC		15		20		20	ns	15
Output Enable	^tOE		15		15		15	ns	
Access time from column address	^tAA		30		35		40	ns	
Access time from $\overline{CAS}$ precharge	^tCPA		35		40		45	ns	
$\overline{RAS}$ pulse width	^tRAS	60	100,000	70	100,000	80	100,000	ns	
$\overline{RAS}$ pulse width (FAST PAGE MODE)	^tRASP	60	100,000	70	100,000	80	100,000	ns	
$\overline{RAS}$ hold time	^tRSH	15		20		20		ns	
$\overline{RAS}$ precharge time	^tRP	40		50		60		ns	
$\overline{CAS}$ pulse width	^tCAS	15	100,000	20	100,000	20	100,000	ns	
$\overline{CAS}$ hold time	^tCSH	60		70		80		ns	
$\overline{CAS}$ precharge time	^tCPN	10		10		10		ns	16
$\overline{CAS}$ precharge time (FAST PAGE MODE)	^tCP	10		10		10		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	^tRCD	15	45	20	50	20	60	ns	17
$\overline{CAS}$ to $\overline{RAS}$ precharge time	^tCRP	5		5		5		ns	
Row address setup time	^tASR	0		0		0		ns	
Row address hold time	^tRAH	10		10		10		ns	
$\overline{RAS}$ to column address delay time	^tRAD	15	30	15	35	15	40	ns	18
Column address setup time	^tASC	0		0		0		ns	
Column address hold time	^tCAH	10		15		15		ns	
Column address hold time (referenced to $\overline{RAS}$)	^tAR	50		55		60		ns	
Column address to $\overline{RAS}$ lead time	^tRAL	30		35		40		ns	
Read command setup time	^tRCS	0		0		0		ns	26
Read command hold time (referenced to $\overline{CAS}$)	^tRCH	0		0		0		ns	19, 26
Read command hold time (referenced to $\overline{RAS}$)	^tRRH	0		0		0		ns	19
$\overline{CAS}$ to output in Low-Z	^tCLZ	0		0		0		ns	
Output buffer turn-off delay	^tOFF	0	15	0	20	0	20	ns	20, 29

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

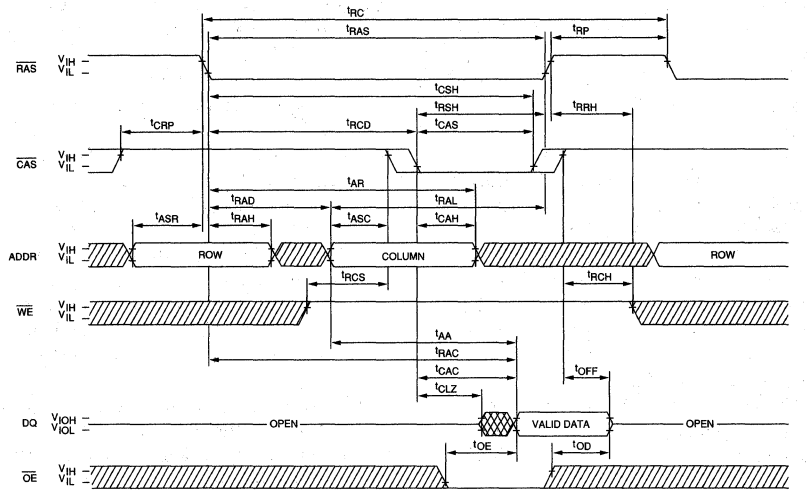
(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C ≤ T_A ≤ +70°C)

AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
$\overline{WE}$ command setup time	^tWCS	0		0		0		ns	21, 26
Write command hold time	^tWCH	10		15		15		ns	26
Write command hold time (referenced to $\overline{RAS}$)	^tWCR	45		55		60		ns	26
Write command pulse width	^tWP	10		15		15		ns	26
Write command to $\overline{RAS}$ lead time	^tRWL	15		20		20		ns	26
Write command to $\overline{CAS}$ lead time	^tCWL	15		20		20		ns	26
Data-in setup time	^tDS	0		0		0		ns	22
Data-in hold time	^tDH	10		15		15		ns	22
Data-in hold time (referenced to $\overline{RAS}$)	^tDHR	45		55		60		ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	^tRWD	85		95		105		ns	21
Column address to $\overline{WE}$ delay time	^tAWD	55		60		65		ns	21
$\overline{CAS}$ to $\overline{WE}$ delay time	^tCWD	40		45		45		ns	21
Transition time (rise or fall)	^tT	3	50	3	50	3	50	ns	9, 10
Refresh period (4,096 cycles)	^tREF		64		64		64	ms	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	^tRPC	0		0		0		ns	
$\overline{CAS}$ setup time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tCSR	5		5		5		ns	5
$\overline{CAS}$ hold time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tCHR	15		15		15		ns	5
$\overline{WE}$ hold time (MASKED WRITE and $\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tWRH	15		15		15		ns	26
$\overline{WE}$ setup time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tWRP	10		10		10		ns	26
$\overline{WE}$ setup time (MASKED WRITE)	^tWRS	10		10		10		ns	26
$\overline{OE}$ setup prior to RAS during HIDDEN REFRESH cycle	^tORD	0		0		0		ns	
Output disable	^tOD		15		15		15	ns	29
$\overline{OE}$ hold time from $\overline{WE}$ during READ-MODIFY-WRITE cycle	^tOEH	15		15		15		ns	28

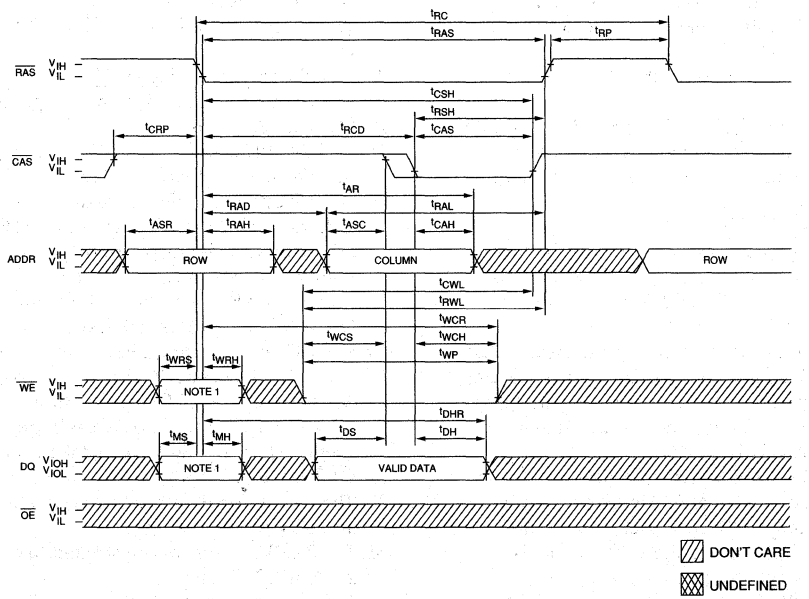
NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. V_{CC} = 5V ±10%, f = 1 MHz.
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is assured.
7. An initial pause of 100µs is required after power-up followed by eight $\overline{RAS}$ refresh cycles ($\overline{RAS}$-ONLY or CBR) before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-up should be repeated any time the ^tREF refresh requirement is exceeded.
8. AC characteristics assume ^tT = 5ns.
9. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS}$ = V_{IH}, data output is high impedance.
12. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to 1 TTL gate and 50pF.
14. Assumes that ^tRCD < ^tRCD (MAX). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
15. Assumes that ^tRCD ≥ ^tRCD (MAX).
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the Q buffer, $\overline{CAS}$ must be pulsed HIGH for ^tCPN.
17. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (MAX) limit, then access time is controlled exclusively by ^tCAC.
18. Operation within the ^tRAD limit ensures that ^tRCD (MAX) can be met. ^tRAD (MAX) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (MAX) limit, then access time is controlled exclusively by ^tAA.
19. Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
20. ^tOFF (MAX) defines the time at which the output achieves the open circuit condition, not a reference to V_{OH} or V_{OL}.
21. ^tWCS, ^tRWD, ^tAWD and ^tCWD are restrictive operating parameters in LATE-WRITE and READ-MODIFY-WRITE cycles only. If ^tWCS ≥ ^tWCS (MIN), the cycle is an EARLY-WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If ^tRWD ≥ ^tRWD (MIN), ^tAWD ≥ ^tAWD (MIN) and ^tCWD ≥ ^tCWD (MIN), the cycle is a READ-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of data out are indeterminate. $\overline{OE}$ held HIGH and $\overline{WE}$ taken LOW after $\overline{CAS}$ goes LOW results in a LATE-WRITE ($\overline{OE}$ controlled) cycle.
22. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY-WRITE cycles and $\overline{WE}$ leading edge in LATE-WRITE or READ-MODIFY-WRITE cycles.
23. During a READ cycle, if $\overline{OE}$ is LOW then taken HIGH before $\overline{CAS}$ goes HIGH, Q goes open. If $\overline{OE}$ is tied permanently LOW, LATE-WRITE or READ-MODIFY-WRITE operations are not possible.
24. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW and $\overline{OE}$ = HIGH.
25. All other inputs at Vcc -0.2V.
26. Write command is defined as $\overline{WE}$ going LOW.
27. MT4C2M8A2 only.
28. LATE-WRITE and READ-MODIFY-WRITE cycles must have both ^tOD and ^tOEH met ($\overline{OE}$ HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. The DQs will provide the previously read data if $\overline{CAS}$ remains LOW and $\overline{OE}$ is taken back LOW after ^tOEH is met. If $\overline{CAS}$ goes HIGH prior to $\overline{OE}$ going back LOW, the DQs will remain open.
29. The DQs open during READ cycles once ^tOD or ^tOFF occur. If $\overline{CAS}$ goes HIGH first, $\overline{OE}$ becomes a "don't care." If $\overline{OE}$ goes HIGH and $\overline{CAS}$ stays LOW, $\overline{OE}$ is not a don't care; and the DQs will provide the previously read data if $\overline{OE}$ is taken back LOW (while $\overline{CAS}$ remains LOW).
30. The 5V version is restricted to operate between 4.5 V and 5.5V only.
31. The 3.0/3.3V version is restricted to operate between 2.7 V and 3.6V only.
32. Column address changed once while $\overline{RAS}$ = V_{IL} and $\overline{CAS}$ = V_{IH}.

READ CYCLE

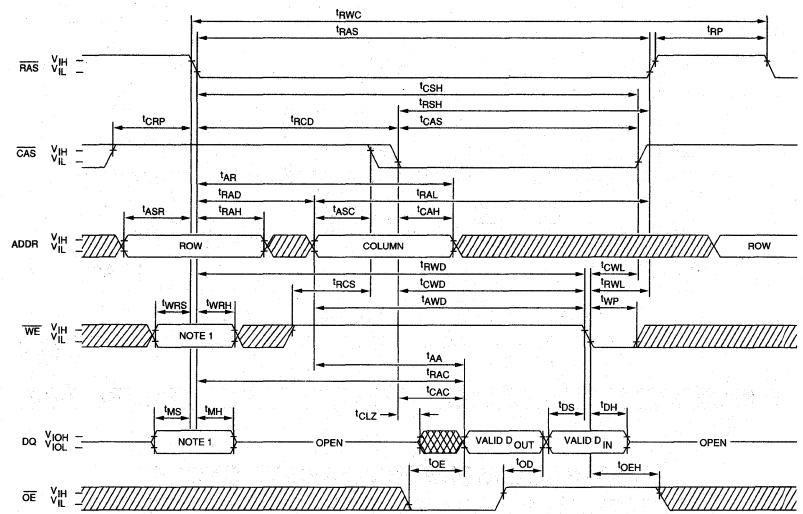


EARLY-WRITE CYCLE

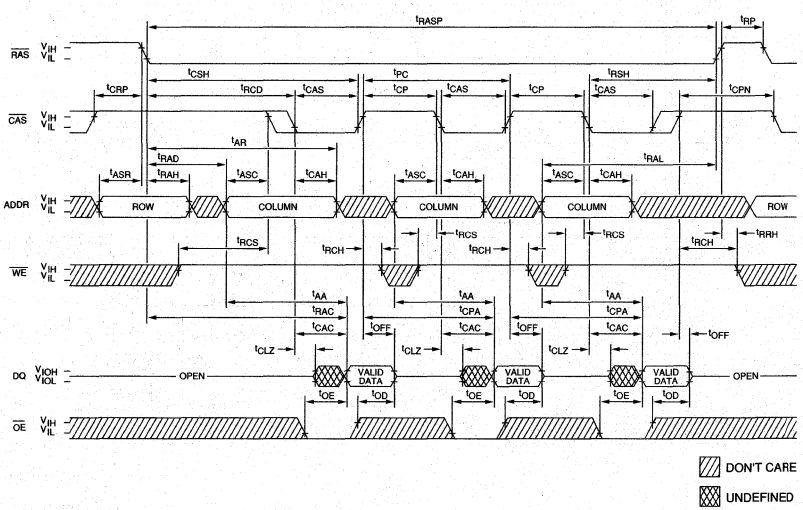


NOTE: 1. Applies to MT4C2M8A2 only; $\overline{WE}$ and DQ inputs on MT4C2M8A1 are "don't care" at $\overline{RAS}$ time. $\overline{WE}$ selects between normal WRITE and MASKED WRITE at $\overline{RAS}$ time. The DQ inputs are "don't care" for a normal WRITE ($\overline{WE}$ HIGH at $\overline{RAS}$ time). The DQ inputs provide the mask data at $\overline{RAS}$ time for a MASKED WRITE, $\overline{WE}$ LOW at $\overline{RAS}$ time.

READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)

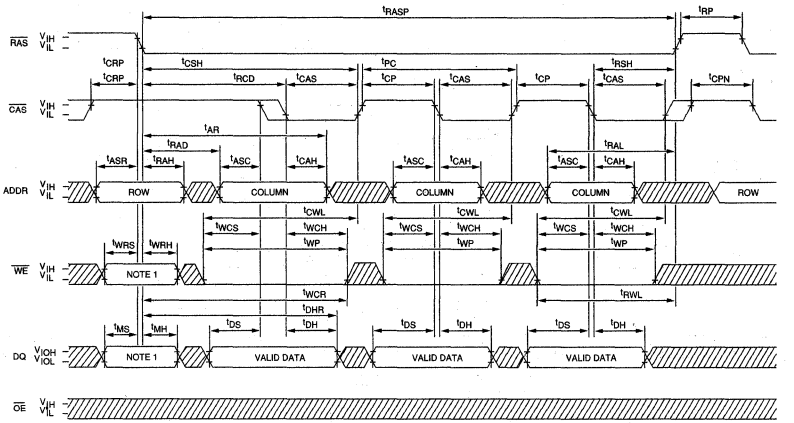


FAST-PAGE-MODE READ CYCLE

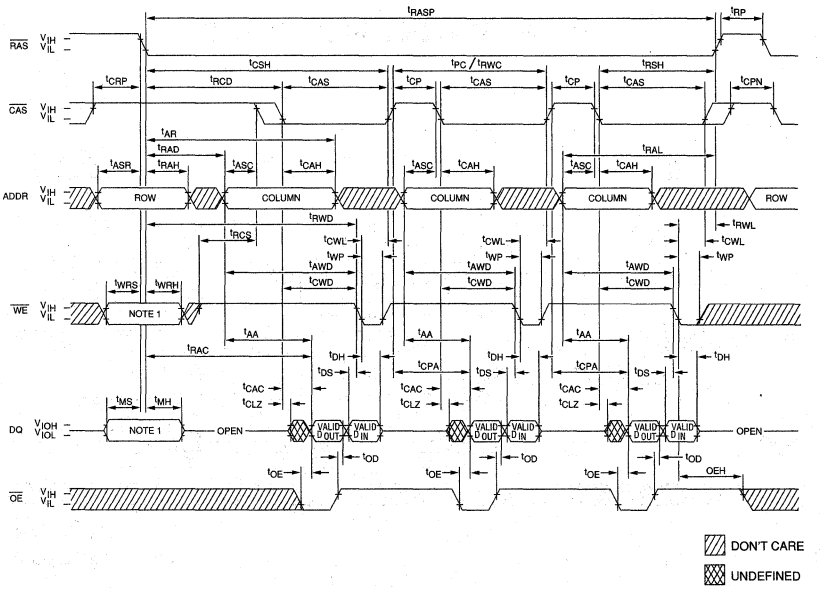


NOTE: 1. Applies to MT4C2M8A2 only; $\overline{WE}$ and DQ inputs on MT4C2M8A1 are "don't care" at $\overline{RAS}$ time. $\overline{WE}$ selects between normal WRITE and MASKED WRITE at $\overline{RAS}$ time. The DQ inputs are "don't care" for a normal WRITE ($\overline{WE}$ HIGH at $\overline{RAS}$ time). The DQ inputs provide the mask data at $\overline{RAS}$ time for a MASKED WRITE, $\overline{WE}$ LOW at $\overline{RAS}$ time.

FAST-PAGE-MODE EARLY-WRITE CYCLE

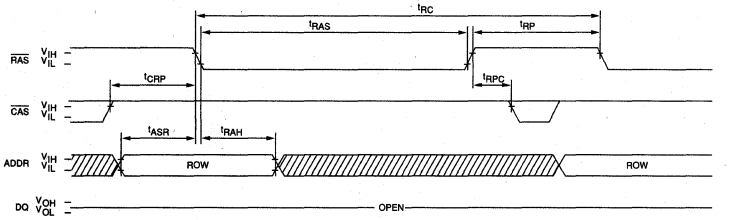


FAST-PAGE-MODE READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)

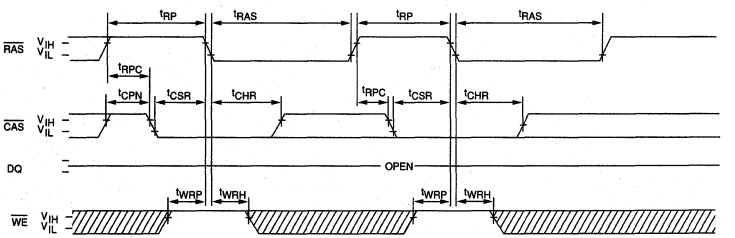


NOTE: 1. Applies to MT4C2M8A2 only; $\overline{WE}$ and DQ inputs on MT4C2M8A1 are "don't care" at $\overline{RAS}$ time. $\overline{WE}$ selects between normal WRITE and MASKED WRITE at $\overline{RAS}$ time. The DQ inputs are "don't care" for a normal WRITE ($\overline{WE}$ HIGH at $\overline{RAS}$ time). The DQ inputs provide the mask data at $\overline{RAS}$ time for a MASKED WRITE, $\overline{WE}$ LOW at $\overline{RAS}$ time.

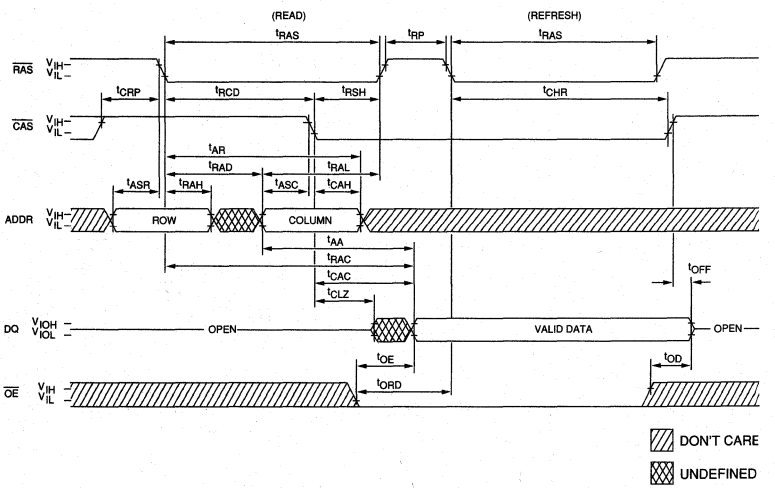
RAS-ONLY REFRESH CYCLE
(OE and WE = DON'T CARE)



CAS-BEFORE-RAS REFRESH CYCLE
(A0-A11; OE = DON'T CARE)



HIDDEN REFRESH CYCLE [24]
(WE = HIGH; OE = LOW)



NEW ■ WIDE DRAM

DRAM

2 MEG x 8 DRAM

5.0V FAST PAGE MODE (MT4C2M8B1/2)
3.0/3.3V, FAST PAGE MODE (MT4LC2M8B1/2)

FEATURES

- Industry standard x8 pinouts, timing, functions and packages
- Address entry: 11 row, 10 column addresses (32ms);
- 2,048-cycle refresh (4,096-cycle refresh available as MT4(L)C2M8B1/2)
- High-performance, CMOS silicon-gate process
- Single +5V only or 3.0/3.3V only ±10% power supply
- Low power, 5mW standby; 400mW active, typical (5V)
- All device pins are fully TTL compatible
- Refresh modes: $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$ (CBR) and HIDDEN
- Optional FAST PAGE MODE access cycle
- NONPERSISTENT MASKED WRITE access cycle (MT4C2M8B2 only)

OPTIONS — MARKING

- Timing
  - 60ns access — -6
  - 70ns access — -7
  - 80ns access — -8
- Power Supply
  - 5V ±10% only — 4C
  - 3.0/3.3V ±10% only — 4LC
- Masked Write
  - Not available — B1
  - Available — B2
- Packages
  - Plastic 28-pin SOJ (400 mil) — DJ
  - Plastic 28-pin TSOP (400 mil) — TG
  - Plastic 32-pin SOJ (400 mil) — DL
  - Plastic 32-pin TSOP (400 mil) — TL

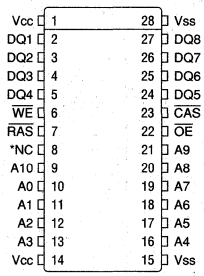
NOTE: Available in die form. Please consult factory for die data sheets.

PART DESCRIPTION

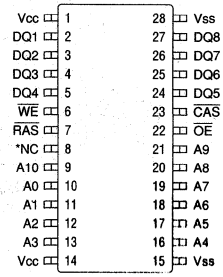
MT4C2M8B1	5.0V, non-masked write
MT4C2M8B2	5.0V, masked write
MT4LC2M8B1	3.0V/3.3V, non-masked write
MT4LC2M8B2	3.0V/3.3V, masked write

PIN ASSIGNMENT (Top View)

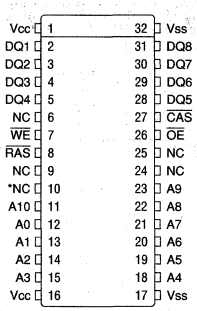
28-Pin SOJ (Q-4)



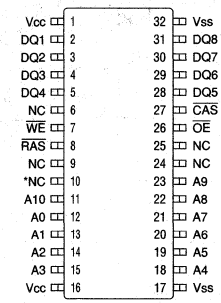
28-Pin TSOP (R-3)



32-Pin SOJ (Q-5)



32-Pin TSOP (R-4)



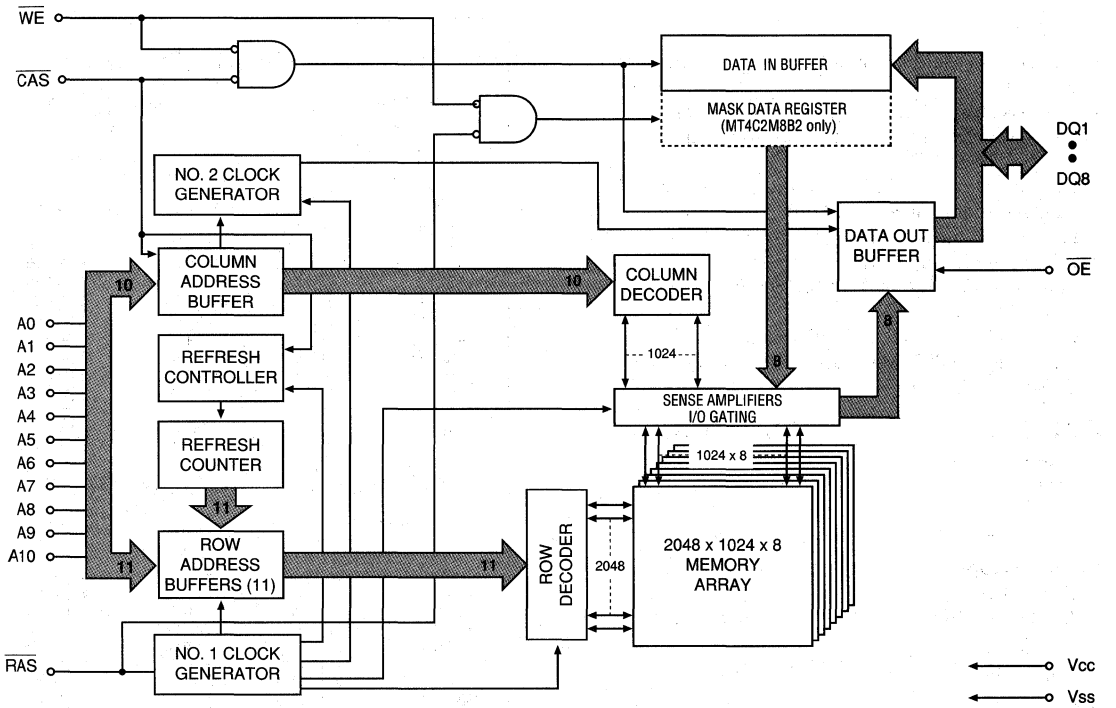
*A11 on 12 row address version

GENERAL DESCRIPTION

The MT4C2M8B1/2 and MT4LC2M8B1/2 are randomly accessed solid-state memories containing 16,777,216 bits organized in a x8 configuration. The MT4C2M8B1/2 and the MT4LC2M8B1/2 are the same DRAM versions except that the MT4LC2M8B1/2 are low voltage versions of the MT4C2M8B1/2. The MT4LC2M8B1/2 are designed to operate in either a 3.0V ±10% or a 3.3V ±10% memory system. All further references made for the MT4C2M8B1/2 also apply to the MT4LC2M8B1/2, unless specifically stated otherwise. Each byte is uniquely addressed through the 21 address bits during $\overline{READ}$ or WRITE cycles. The address is entered first by $\overline{RAS}$ latching 11 bits (A0-A10) and then $\overline{CAS}$ latching 10 bits (A0-A10).

The MT4C2M8B2 has NONPERSISTENT MASKED WRITE, allowing it to perform WRITE-PER-BIT accesses.

FUNCTIONAL BLOCK DIAGRAM
2,048 ROWS



PIN DESCRIPTIONS

28-PIN DEVICE PIN NUMBERS	32-PIN DEVICE PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
7	8	$\overline{RAS}$	Input	Row Address Strobe: $\overline{RAS}$ is used to clock-in the 11 row-address bits and strobe the $\overline{WE}$ and DQs in the MASKED WRITE mode (MT4C2M8B2 only).
23	27	$\overline{CAS}$	Input	Column Address Strobe: $\overline{CAS}$ is used to clock-in the 10 column-address bits, enable the DRAM output buffers, and strobe the data inputs on WRITE cycles.
6	7	$\overline{WE}$	Input	Write Enable: $\overline{WE}$ is used to select a READ ($\overline{WE}$ = HIGH) or WRITE ($\overline{WE}$ = LOW) cycle. $\overline{WE}$ also serves as a Mask Enable ($\overline{WE}$ = LOW) at the falling edge of $\overline{RAS}$ in a MASKED-WRITE cycle (MT4C2M8B2).
22	26	$\overline{OE}$	Input	Output Enable: $\overline{OE}$ enables the output buffers when taken LOW during a READ access cycle. $\overline{RAS}$ and $\overline{CAS}$ must be LOW and $\overline{WE}$ must be HIGH before $\overline{OE}$ will control the output buffers. Otherwise the output buffers are in a High-Z state.
10-13, 16-21, 9	12-15, 18-23, 11	A0-A10	Input	Address Inputs: These inputs are multiplexed and clocked by $\overline{RAS}$ and $\overline{CAS}$ to select one byte out of the 2 Meg available words.
2-5, 24-27	2-5, 28-31	DQ1-DQ8	Input	Data I/O: Includes inputs, outputs or High-Z and/or Output masked data input (for MASKED WRITE cycle only).
8	6, 9, 24, 25, 10	NC	-	No Connect: These pins should be either left unconnected or tied to ground.
1, 14	1, 16	V_{CC}	Supply	Power Supply: +5V ±10% (C), 3.0/3.3V ±10% (LC)
15, 28	17, 32	V_{SS}	Supply	Ground

NEW ■ WIDE DRAM

FUNCTIONAL DESCRIPTION

Each bit is uniquely addressed through the 21 address bits during READ or WRITE cycles. First $\overline{RAS}$ is used to latch 11 bits (A0-A10) then $\overline{CAS}$ latches 10 bits (A0-A9).

The $\overline{CAS}$ control also determines whether the cycle will be a refresh cycle ($\overline{RAS}$-ONLY) or an active cycle (READ, WRITE or READ-WRITE) once $\overline{RAS}$ goes LOW.

READ or WRITE cycles are selected by $\overline{WE}$. A logic HIGH on $\overline{WE}$ dictates READ mode while a logic LOW on $\overline{WE}$ dictates WRITE mode. During a WRITE cycle, data in (D) is latched by the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. Taking $\overline{WE}$ LOW will initiate a WRITE cycle, selecting DQ1 through DQ8. If $\overline{WE}$ goes LOW prior to $\overline{CAS}$ going LOW, the output pin(s) remain open (High-Z) until the next $\overline{CAS}$ cycle. If $\overline{WE}$ goes LOW after $\overline{CAS}$ goes LOW and data reaches the output pins, data out (Q) is activated and retains the selected cell data as long as $\overline{CAS}$ and $\overline{OE}$ remain LOW (regardless of $\overline{WE}$ or $\overline{RAS}$). This late $\overline{WE}$ pulse results in a READ-WRITE cycle.

The eight data inputs and eight data outputs are routed through eight pins using common I/O, and pin direction is controlled by $\overline{OE}$ and $\overline{WE}$.

FAST PAGE MODE operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row address (A0-A11) defined page boundary. The FAST PAGE MODE cycle is always initiated with a row address strobed-in by $\overline{RAS}$ followed by a column address strobed-in by $\overline{CAS}$. $\overline{CAS}$ may be toggled-in by holding $\overline{RAS}$ LOW and strobing-in different column addresses, thus executing faster memory cycles. Returning $\overline{RAS}$ HIGH terminates the FAST PAGE MODE operation.

Returning $\overline{RAS}$ and $\overline{CAS}$ HIGH terminates a memory cycle and decreases chip current to a reduced standby level. The chip is also preconditioned for the next cycle during the $\overline{RAS}$ high time. Memory cell data is retained in its correct state by maintaining power and executing any $\overline{RAS}$ cycle (READ, WRITE, $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$, or HIDDEN REFRESH) so that all 2,048 combinations of $\overline{RAS}$ addresses (A0-A10) are executed at least every 32ms, regardless of sequence. The $\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh cycle will also invoke the refresh counter and controller for row address control.

MASKED WRITE ACCESS CYCLE (MT4C2M8B2 ONLY)

Every WRITE access cycle can be a MASKED WRITE, depending on the state of $\overline{WE}$ at $\overline{RAS}$ time. A MASKED WRITE is selected when $\overline{WE}$ is LOW at $\overline{RAS}$ time and mask data is supplied on the DQ pins.

The mask data present on the DQ1-DQ8 inputs at $\overline{RAS}$ time will be written to an internal mask data register and will then act as an individual write enable for each of the corresponding DQ inputs. If a LOW (logic "0") is written to a mask data register bit, the input port for that bit is disabled during the subsequent WRITE operation and no new data will be written to that DRAM cell location. A HIGH (logic "1") on a mask data register bit enables the input port and allows normal WRITE operations to proceed. At $\overline{CAS}$ time, the bits present on the DQ1-DQ8 inputs will be written to the DRAM (if the mask data bit was HIGH) or ignored (if the mask data bit was LOW).

In nonpersistent MASKED WRITEs, new mask data must be supplied each time a MASKED WRITE cycle is initiated.

Figure 1 illustrates the MT4C2M8B2 MASKED WRITE operation (Note: $\overline{RAS}$ or $\overline{CAS}$ time refers to the time at which $\overline{RAS}$ or $\overline{CAS}$ transition from HIGH to LOW).

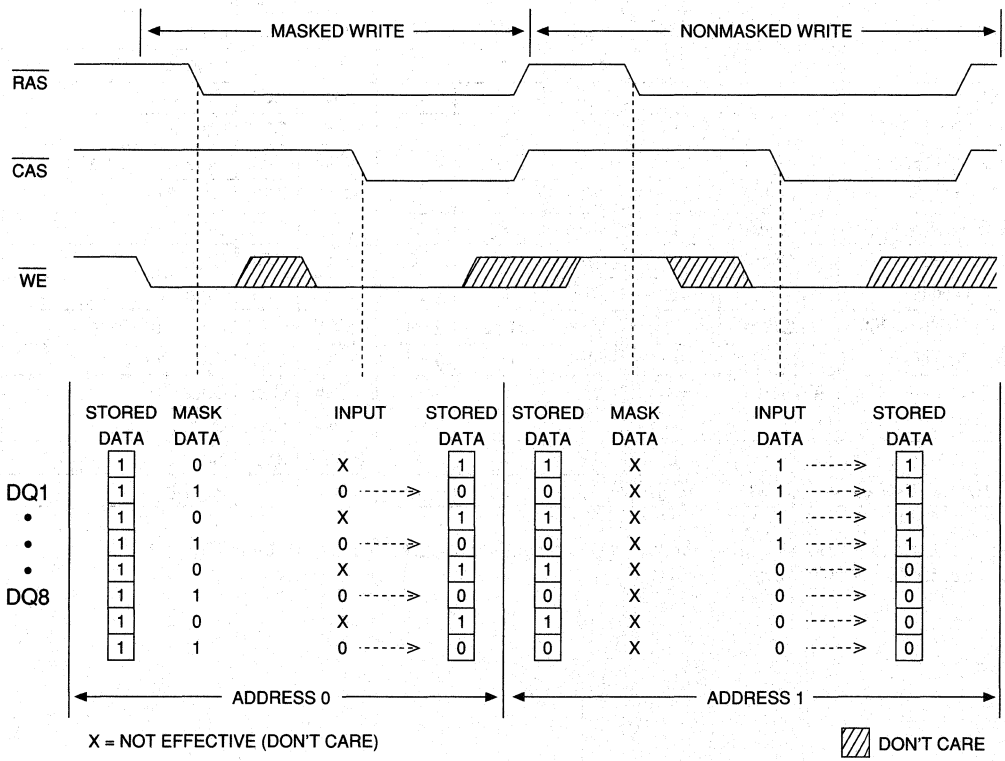


Figure 1
MT4C2M8B2 MASKED WRITE EXAMPLE

TRUTH TABLE

FUNCTION		RAS	CAS	WE	OE	ADDRESSES tR	ADDRESSES tC	DQs	NOTES
Standby		H	H→X	X	X	X	X	High-Z	
READ		L	L	H	L	ROW	COL	Data Out	
EARLY-WRITE		L	L	L	X	ROW	COL	Data In	1
READ-WRITE		L	L	H→L	L→H	ROW	COL	Data Out, Data In	1
FAST-PAGE-	1st Cycle	L	H→L	H	L	ROW	COL	Data Out	
MODE READ	2nd Cycle	L	H→L	H	L	n/a	COL	Data Out	
FAST-PAGE-	1st Cycle	L	H→L	L	X	ROW	COL	Data In	1
MODE WRITE	2nd Cycle	L	H→L	L	X	n/a	COL	Data In	1
FAST-PAGE-MODE	1st Cycle	L	H→L	H→L	L→H	ROW	COL	Data Out, Data In	1
READ-WRITE	2nd Cycle	L	H→L	H→L	L→H	n/a	COL	Data Out, Data In	1
HIDDEN	READ	L→H→L	L	H	L	ROW	COL	Data Out	
REFRESH	WRITE	L→H→L	L	L	X	ROW	COL	Data In	1, 2
RAS-ONLY REFRESH		L	H	X	X	ROW	n/a	High-Z	
CAS-BEFORE-RAS REFRESH		H→L	L	H	X	X	X	High-Z	

NOTE: 1. Data in will be dependent on the mask provided (MT4C2M8B2 only). Refer to Figure 1.
2. EARLY WRITE only.

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS} (5V) .....-1V to +7V
Voltage on V_{CC} supply relative to V_{SS} (3V) ...-1V to +4.6V
Operating Temperature, T_A (Ambient) .....0°C to +70°C
Storage Temperature (Plastic) .....-55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC OPERATING SPECIFICATIONS FOR 5V VERSION

(Notes: 1, 3, 4, 6, 7, 30) (0°C ≤ T_A ≤ 70°C; V_{CC} = 5V ±10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.5	V	1, 30
Input High (Logic 1) Voltage, All Inputs	V_{IH}	2.4	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, All Inputs	V_{IL}	-1.0	0.8	V	1
INPUT LEAKAGE CURRENT Any Input 0V ≤ V_{IN} ≤ Vcc (All other pins not under test = 0V)	I_I	-2	2	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled, 0V ≤ V_{OUT} ≤ 5.5V)	I_{OZ}	-10	10	µA	
OUTPUT LEVELS Output High Voltage (I_{OUT} = -2.5mA)	V_{OH}	2.4		V	
Output Low Voltage (I_{OUT} = 2.1mA)	V_{OL}		0.4	V	

DC OPERATING SPECIFICATIONS FOR 3.0/3.3V VERSION

(Notes: 1, 3, 4, 6, 7, 31) (0°C ≤ T_A ≤ 70°C; V_{CC} = 3.0/3.3V ±10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	2.7	3.6	V	1, 31
Input High (Logic 1) Voltage, All Inputs	V_{IH}	2.0	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, All Inputs	V_{IL}	-1.0	0.8	V	1
INPUT LEAKAGE CURRENT Any Input 0V ≤ V_{IN} ≤ Vcc (All other pins not under test = 0V)	I_I	-2	2	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled, 0V ≤ V_{OUT} ≤ 3.6V)	I_{OZ}	-10	10	µA	
OUTPUT LEVELS Output High Voltage (I_{OUT} = -2mA)	V_{OH}	2.4		V	
Output Low Voltage (I_{OUT} = 2mA)	V_{OL}		0.4	V	

DC OPERATING SPECIFICATIONS FOR 5V VERSION

(Notes: 1, 3, 4, 6, 7, 30) (0°C ≤ T_A ≤ 70°C; Vcc = 5V ±10%)

		MAX				
PARAMETER/CONDITION	**SYMBOL**	**-6**	**-7**	**-8**	**UNITS**	**NOTES**
STANDBY CURRENT: TTL ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC1}	2	2	2	mA	
STANDBY CURRENT: CMOS ($\overline{RAS}$ = $\overline{CAS}$ = Vcc -0.2V)	I_{CC2}	1	1	1	mA	25
OPERATING CURRENT: Random READ/WRITE Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC (MIN))	I_{CC3}	140	130	120	mA	3, 4, 32
OPERATING CURRENT: FAST PAGE MODE Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: ^tPC = ^tPC (MIN); ^tCP, ^tASC = 10ns)	I_{CC4}	100	90	80	mA	3, 4, 32
REFRESH CURRENT: $\overline{RAS}$-ONLY Average power supply current ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}: ^tRC = ^tRC (MIN))	I_{CC5}	140	130	120	mA	3, 32
REFRESH CURRENT: $\overline{CAS}$-BEFORE-$\overline{RAS}$ Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC (MIN))	I_{CC6}	140	130	120	mA	3

DC OPERATING SPECIFICATIONS FOR 3.0/3.3V VERSION

(Notes: 1, 3, 4, 6, 7, 31) (0°C ≤ T_A ≤ 70°C; Vcc = 3.0/3.3V ±10%)

		MAX				
PARAMETER/CONDITION	**SYMBOL**	**-6**	**-7**	**-8**	**UNITS**	**NOTES**
STANDBY CURRENT: TTL ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC1}	1	1	1	mA	
STANDBY CURRENT: CMOS ($\overline{RAS}$ = $\overline{CAS}$ = Vcc -0.2V)	I_{CC2}	400	400	400	µA	25
OPERATING CURRENT: Random READ/WRIT Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC (MIN))	I_{CC3}	100	90	80	mA	3, 4, 32
OPERATING CURRENT: FAST PAGE MODE Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: ^tPC = ^tPC (MIN); ^tCP, ^tASC = 10ns)	I_{CC4}	75	65	55	mA	3, 4, 32
REFRESH CURRENT: $\overline{RAS}$-ONLY Average power supply current ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}: ^tRC = ^tRC (MIN))	I_{CC5}	100	90	80	mA	3, 32
REFRESH CURRENT: $\overline{CAS}$-BEFORE-$\overline{RAS}$ Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC (MIN))	I_{CC6}	100	90	80	mA	3

CAPACITANCE

PARAMETER	SYMBOL	MAX	UNITS	NOTES
Input Capacitance: A0-A10	C_{I1}	5	pF	2
Input Capacitance: $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$	C_{I2}	7	pF	2
Input/Output Capacitance: DQ	C_{IO}	7	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C ≤ T_A ≤ +70°C)

AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	t_{RC}	110		130		150		ns	
READ-WRITE cycle time	t_{RWC}	155		180		200		ns	
FAST-PAGE-MODE READ or WRITE cycle time	t_{PC}	35		40		40		ns	
FAST-PAGE-MODE READ-WRITE cycle time	t_{PRWC}	85		95		100		ns	
Access time from $\overline{RAS}$	t_{RAC}		60		70		80	ns	14
Access time from $\overline{CAS}$	t_{CAC}		15		20		20	ns	15
Output Enable	t_{OE}		15		15		15	ns	
Access time from column address	t_{AA}		30		35		40	ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		35		40		45	ns	
$\overline{RAS}$ pulse width	t_{RAS}	60	100,000	70	100,000	80	100,000	ns	
$\overline{RAS}$ pulse width (FAST PAGE MODE)	t_{RASP}	60	100,000	70	100,000	80	100,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	15		20		20		ns	
$\overline{RAS}$ precharge time	t_{RP}	40		50		60		ns	
$\overline{CAS}$ pulse width	t_{CAS}	15	100,000	20	100,000	20	100,000	ns	
$\overline{CAS}$ hold time	t_{CSH}	60		70		80		ns	
$\overline{CAS}$ precharge time	t_{CPN}	10		10		10		ns	16
$\overline{CAS}$ precharge time (FAST PAGE MODE)	t_{CP}	10		10		10		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	15	45	20	50	20	60	ns	17
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		5		ns	
Row address setup time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	10		10		10		ns	
$\overline{RAS}$ to column address delay time	t_{RAD}	15	30	15	35	15	40	ns	18
Column address setup time	t_{ASC}	0		0		0		ns	
Column address hold time	t_{CAH}	10		15		15		ns	
Column address hold time (referenced to $\overline{RAS}$)	t_{AR}	50		55		60		ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	30		35		40		ns	
Read command setup time	t_{RCS}	0		0		0		ns	26
Read command hold time (referenced to $\overline{CAS}$)	t_{RCH}	0		0		0		ns	19, 26
Read command hold time (referenced to $\overline{RAS}$)	t_{RRH}	0		0		0		ns	19
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	0		0		0		ns	
Output buffer turn-off delay	t_{OFF}	0	15	0	20	0	20	ns	20, 29

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

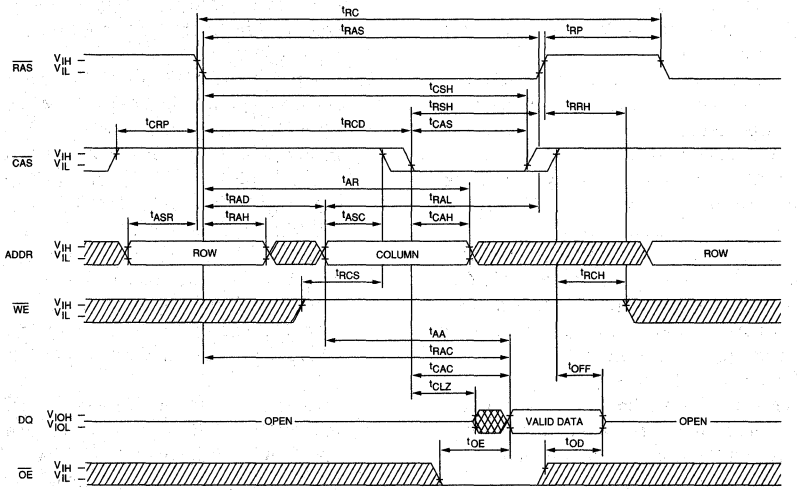
(Notes: 6, 7, 8, 9, 10, 11, 12, 13) ($0°C \le T_A \le +70°C$)

AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
$\overline{WE}$ command setup time	tWCS	0		0		0		ns	21, 29
Write command hold time	tWCH	10		15		15		ns	26
Write command hold time (referenced to $\overline{RAS}$)	tWCR	45		55		60		ns	26
Write command pulse width	tWP	10		15		15		ns	26
Write command to $\overline{RAS}$ lead time	tRWL	15		20		20		ns	26
Write command to $\overline{CAS}$ lead time	tCWL	15		20		20		ns	26
Data-in setup time	tDS	0		0		0		ns	22
Data-in hold time	tDH	10		15		15		ns	22
Data-in hold time (referenced to $\overline{RAS}$)	tDHR	45		55		60		ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	tRWD	85		95		105		ns	21
Column address to $\overline{WE}$ delay time	tAWD	55		60		65		ns	21
$\overline{CAS}$ to $\overline{WE}$ delay time	tCWD	40		45		45		ns	21
Transition time (rise or fall)	tT	3	50	3	50	3	50	ns	9, 10
Refresh period (2,048 cycles)	tREF		32		32		32	ms	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	tRPC	0		0		0		ns	
$\overline{CAS}$ setup time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	tCSR	5		5		5		ns	5
$\overline{CAS}$ hold time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	tCHR	15		15		15		ns	5
$\overline{WE}$ hold time (MASKED WRITE and $\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	tWRH	15		15		15		ns	26
$\overline{WE}$ setup time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	tWRP	10		10		10		ns	26
$\overline{WE}$ setup time (MASKED WRITE)	tWRS	10		10		10		ns	26
$\overline{OE}$ setup prior to RAS during HIDDEN REFRESH cycle	tORD	0		0		0		ns	
Output disable	tOD		15		15		15	ns	29
$\overline{OE}$ hold time from $\overline{WE}$ during READ-MODIFY-WRITE cycle	tOEH	15		15		15		ns	28

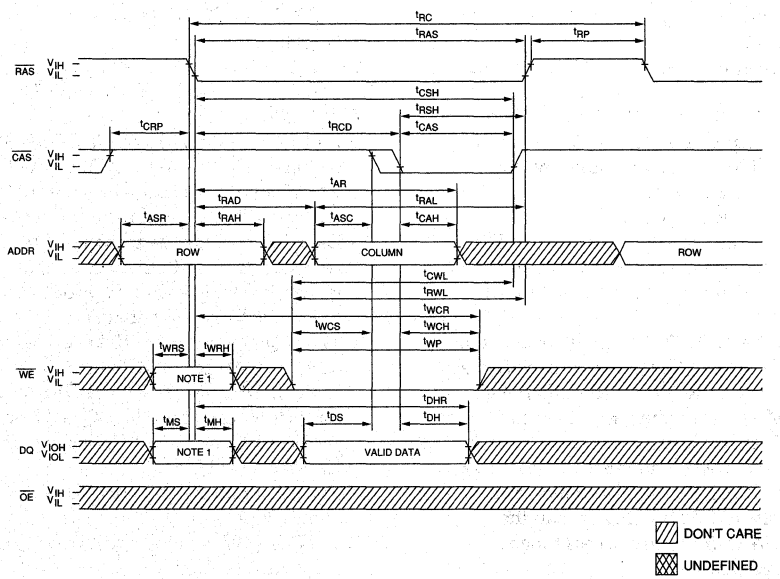
NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. V_{CC} = 5V ±10%, f = 1 MHz.
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \le T_A \le 70°C$) is assured.
7. An initial pause of 100µs is required after power-up followed by eight $\overline{RAS}$ refresh cycles ($\overline{RAS}$ -ONLY or CBR) before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-up should be repeated any time the ^tREF refresh requirement is exceeded.
8. AC characteristics assume ^tT = 5ns.
9. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS}$ = V_{IH}, data output is high impedance.
12. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to 1 TTL gate and 50pF.
14. Assumes that $^tRCD < ^tRCD$ (MAX). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
15. Assumes that $^tRCD \ge ^tRCD$ (MAX).
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the Q buffer, $\overline{CAS}$ must be pulsed HIGH for ^tCPN.
17. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (MAX) limit, then access time is controlled exclusively by ^tCAC.
18. Operation within the ^tRAD limit ensures that ^tRCD (MAX) can be met. ^tRAD (MAX) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (MAX) limit, then access time is controlled exclusively by ^tAA.
19. Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
20. ^tOFF (MAX) defines the time at which the output achieves the open circuit condition, not a reference to V_{OH} or V_{OL}.
21. ^tWCS, ^tRWD, ^tAWD and ^tCWD are restrictive operating parameters in LATE-WRITE and READ-MODIFY-WRITE cycles only. If $^tWCS \ge ^tWCS$ (MIN), the cycle is an EARLY-WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If $^tRWD \ge ^tRWD$ (MIN), $^tAWD \ge ^tAWD$ (MIN) and $^tCWD \ge ^tCWD$ (MIN), the cycle is a READ-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of data out are indeterminate. $\overline{OE}$ held HIGH and $\overline{WE}$ taken LOW after $\overline{CAS}$ goes LOW results in a LATE-WRITE ($\overline{OE}$ controlled) cycle.
22. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY-WRITE cycles and $\overline{WE}$ leading edge in LATE-WRITE or READ-MODIFY-WRITE cycles.
23. During a READ cycle, if $\overline{OE}$ is LOW then taken HIGH before $\overline{CAS}$ goes HIGH, Q goes open. If $\overline{OE}$ is tied permanently LOW, LATE-WRITE or READ-MODIFY-WRITE operations are not possible.
24. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW and $\overline{OE}$ = HIGH.
25. All other inputs at Vcc -0.2V.
26. Write command is defined as $\overline{WE}$ going LOW.
27. MT4C2M8B2 only.
28. LATE-WRITE and READ-MODIFY-WRITE cycles must have both ^tOD and ^tOEH met ($\overline{OE}$ HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. The DQs will provide the previously read data if $\overline{CAS}$ remains LOW and $\overline{OE}$ is taken back LOW after ^tOEH is met. If $\overline{CAS}$ goes HIGH prior to $\overline{OE}$ going back LOW, the DQs will remain open.
29. The DQs open during READ cycles once ^tOD or ^tOFF occur. If $\overline{CAS}$ goes HIGH first, $\overline{OE}$ becomes a "don't care." If $\overline{OE}$ goes HIGH and $\overline{CAS}$ stays LOW, $\overline{OE}$ is not a don't care; and the DQs will provide the previously read data if $\overline{OE}$ is taken back LOW (while $\overline{CAS}$ remains LOW).
30. The 5V version is restricted to operate between 4.5 V and 5.5V only.
31. The 3.0/3.3V version is restricted to operate between 2.7 V and 3.6V only.
32. Column address changed once while $\overline{RAS}$ = V_{IL} and $\overline{CAS}$ = V_{IH}.

READ CYCLE

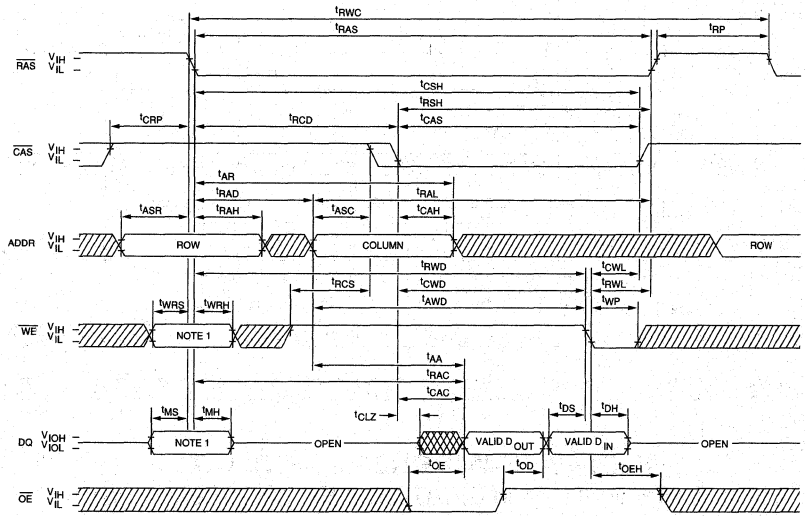


EARLY-WRITE CYCLE

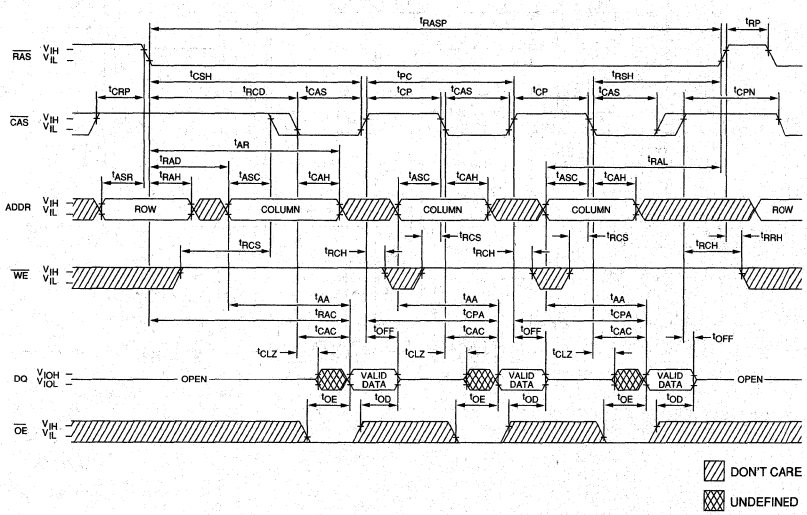


NOTE: 1. Applies to MT4C2M8B2 only; $\overline{WE}$ and DQ inputs on MT4C2M8B1 are "don't care" at $\overline{RAS}$ time. $\overline{WE}$ selects between normal WRITE and MASKED WRITE at $\overline{RAS}$ time. The DQ inputs are "don't care" for a normal WRITE ($\overline{WE}$ HIGH at $\overline{RAS}$ time). The DQ inputs provide the mask data at $\overline{RAS}$ time for a MASKED WRITE, $\overline{WE}$ LOW at $\overline{RAS}$ time.

READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)

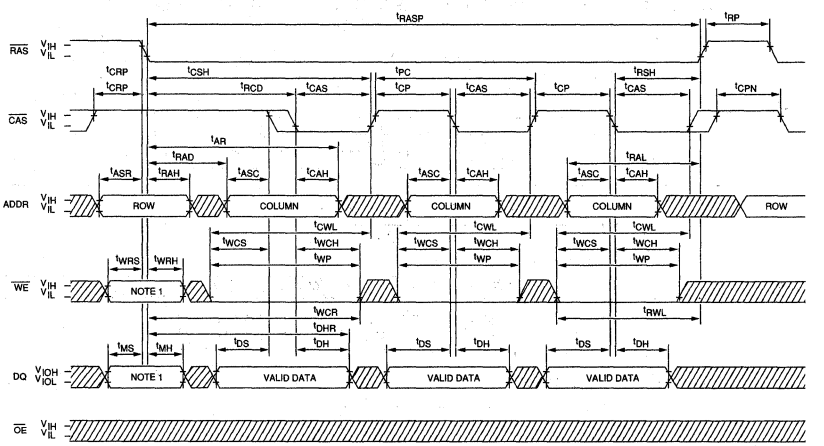


FAST-PAGE-MODE READ CYCLE

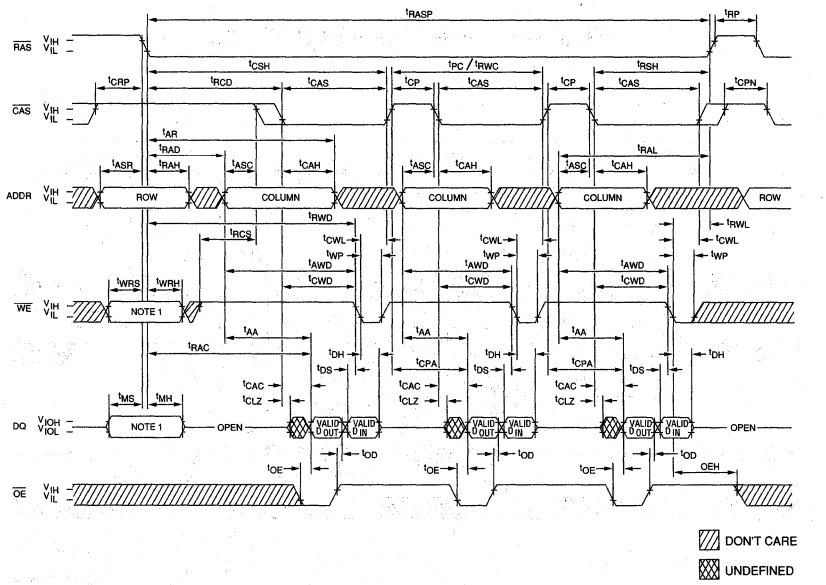


NOTE: 1. Applies to MT4C2M8B2 only; $\overline{WE}$ and DQ inputs on MT4C2M8B1 are "don't care" at $\overline{RAS}$ time. $\overline{WE}$ selects between normal WRITE and MASKED WRITE at $\overline{RAS}$ time. The DQ inputs are "don't care" for a normal WRITE ($\overline{WE}$ HIGH at $\overline{RAS}$ time). The DQ inputs provide the mask data at $\overline{RAS}$ time for a MASKED WRITE, $\overline{WE}$ LOW at $\overline{RAS}$ time.

FAST-PAGE-MODE EARLY-WRITE CYCLE

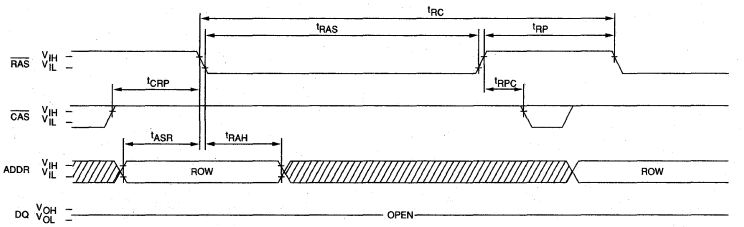


FAST-PAGE-MODE READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)

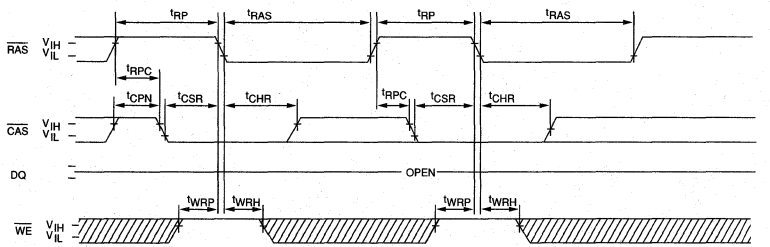


NOTE: 1. Applies to MT4C2M8B2 only; $\overline{WE}$ and DQ inputs on MT4C2M8B1 are "don't care" at $\overline{RAS}$ time. $\overline{WE}$ selects between normal WRITE and MASKED WRITE at $\overline{RAS}$ time. The DQ inputs are "don't care" for a normal WRITE ($\overline{WE}$ HIGH at $\overline{RAS}$ time). The DQ inputs provide the mask data at $\overline{RAS}$ time for a MASKED WRITE, $\overline{WE}$ LOW at $\overline{RAS}$ time.

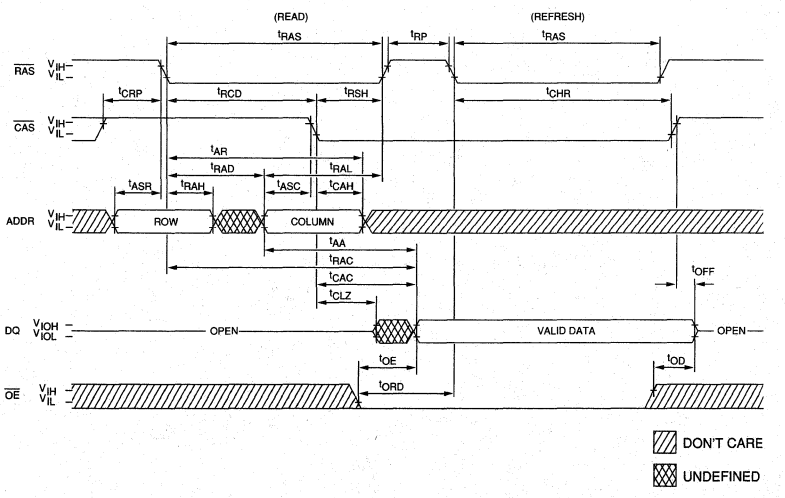
RAS-ONLY REFRESH CYCLE
($\overline{OE}$ and $\overline{WE}$ = DON'T CARE)



CAS-BEFORE-RAS REFRESH CYCLE
(A0-A10; $\overline{OE}$ = DON'T CARE)



HIDDEN REFRESH CYCLE [24]
($\overline{WE}$ = HIGH; $\overline{OE}$ = LOW)



NEW ■ WIDE DRAM

DRAM

2 MEG x 8 DRAM

5.0V, SELF REFRESH (MT4C2M8A1/2 S)
3.0/3.3V, SELF REFRESH (MT4LC2M8A1/2 S)

FEATURES

- SELF REFRESH, i.e. "Sleep Mode"
- Industry standard x8 pinouts, timing, functions and packages
- Address entry: 12 row, nine column addresses (512ms)
- High-performance, CMOS silicon-gate process
- Single +5V only or 3.0/3.3V only ±10% power supply
- All device pins are fully TTL compatible
- Refresh modes: RAS-ONLY, CAS-BEFORE-RAS (CBR), HIDDEN and BATTERY BACKUP (BBU)
- Optional FAST PAGE MODE access cycle
- NONPERSISTENT MASKED WRITE access cycle (MT4(L)C2M8A2 S only)
- 4,096-cycle refresh (2,048-cycle refresh available as MT4(L)C2M8B1/2 S)
- Low power, 2mW standby; 400mW active, typical (5V)

OPTIONS — MARKING

- Timing
  - 60ns access — -6
  - 70ns access — -7
  - 80ns access — -8
- Power Supply
  - 5V ±10% only — 4C
  - 3.0/3.3V ±10% only — 4LC
- Masked Write
  - Not available — A1 S
  - Available — A2 S
- Packages
  - Plastic 28-pin SOJ (400 mil) — DJ
  - Plastic 28-pin TSOP (400 mil) — TG
  - Plastic 32-pin SOJ (400 mil) — DL
  - Plastic 32-pin TSOP (400 mil) — TL

NOTE: Available in die form. Please consult factory for die data sheets.

- Part Number Example: MT4C2M8A1DJ-7 S

PART DESCRIPTION

MT4C2M8A1 S	5V, non-masked write
MT4C2M8A2 S	5V, masked write
MT4LC2M8A1 S	3.0/3.3V, non-masked write
MT4LC2M8A2 S	3.0/3.3V, masked write

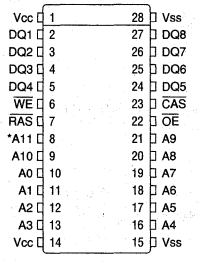
GENERAL DESCRIPTION

The MT4C2M8A1/2 S and MT4LC2M8A1/2 S are randomly accessed solid-state memories containing 16,777,216 bits organized in a x8 configuration. The MT4C2M8A1/2 S and the MT4LC2M8A1/2 S are the same DRAM versions except that the MT4LC2M8A1/2 S are low voltage versions of the MT4C2M8A1/2 S. The MT4LC2M8A1/2 S are designed to operate in either a 3.0V ±10% or a 3.3V ±10% memory system. All further references made for the MT4C2M8A1/2 S also apply to the MT4LC2M8A1/2 S, unless specifically stated otherwise. Each byte is uniquely addressed through the 21 address bits during READ or WRITE cycles. The address is entered first by RAS latching 12 bits (A0-11) and then CAS latching 9 bits (A0-A9).

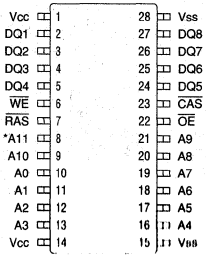
The MT4C2M8A2 S has NONPERSISTENT MASKED WRITE, allowing it to perform WRITE-PER-BIT accesses.

PIN ASSIGNMENT (Top View)

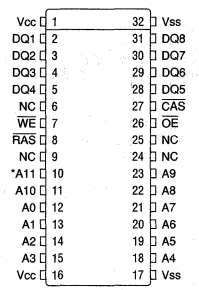
28-Pin SOJ (Q-4)



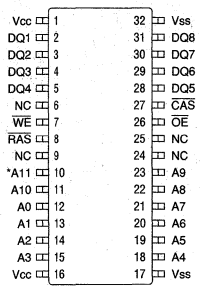
28-Pin TSOP (R-3)



32-Pin SOJ (Q-5)



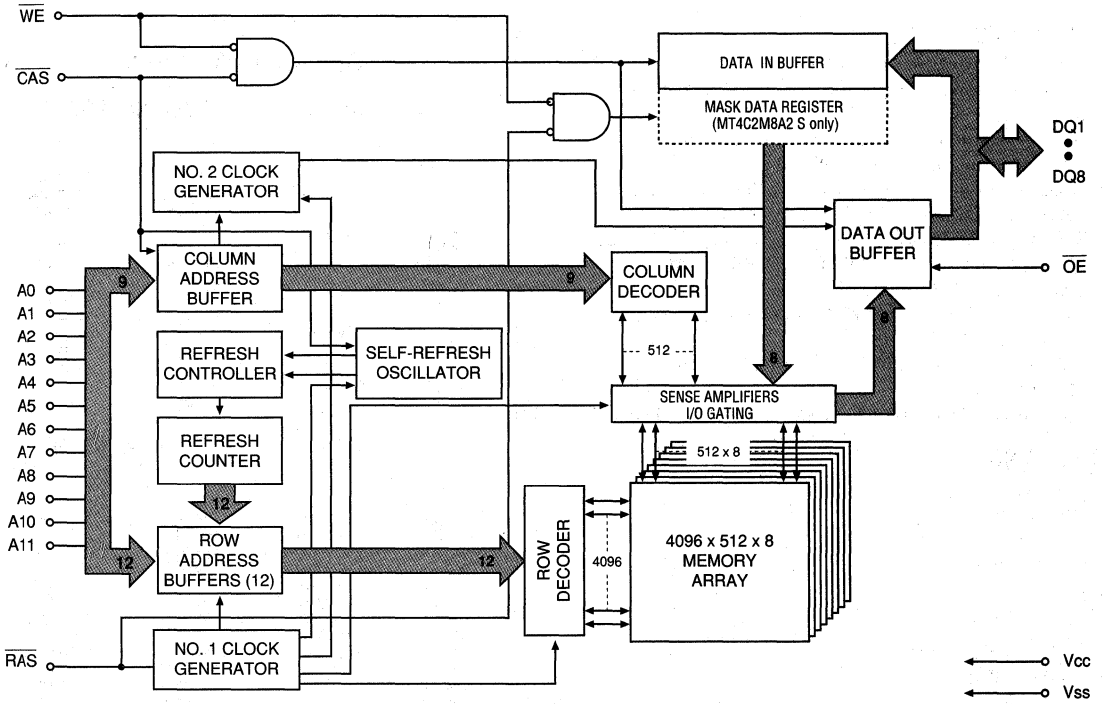
32-Pin TSOP (R-4)



*NC on 11 row address version

NEW ■ WIDE DRAM

FUNCTIONAL BLOCK DIAGRAM
4,096 ROWS



PIN DESCRIPTIONS

28-PIN DEVICE PIN NUMBERS	32-PIN DEVICE PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
7	8	$\overline{RAS}$	Input	Row Address Strobe: $\overline{RAS}$ is used to clock-in the 12 row-address bits and strobe the $\overline{WE}$ and DQs in the MASKED WRITE mode (MT4C2M8A2 S only).
23	27	$\overline{CAS}$	Input	Column Address Strobe: $\overline{CAS}$ is used to clock-in the 9 column-address bits, enable the DRAM output buffers, and strobe the data inputs on WRITE cycles.
6	7	$\overline{WE}$	Input	Write Enable: $\overline{WE}$ is used to select a READ ($\overline{WE}$ = HIGH) or WRITE ($\overline{WE}$ = LOW) cycle. $\overline{WE}$ also serves as a Mask Enable ($\overline{WE}$ = LOW) at the falling edge of $\overline{RAS}$ in a MASKED-WRITE cycle (MT4C2M8A2 S).
22	26	$\overline{OE}$	Input	Output Enable: $\overline{OE}$ enables the output buffers when taken LOW during a READ access cycle. $\overline{RAS}$ and $\overline{CAS}$ must be LOW and $\overline{WE}$ must be HIGH before $\overline{OE}$ will control the output buffers. Otherwise the output buffers are in a High-Z state.
10-13, 16-21, 9, 8	12-15, 18-23, 11, 10	A0-A11	Input	Address Inputs: These inputs are multiplexed and clocked by $\overline{RAS}$ and $\overline{CAS}$ to select one byte out of the 2 Meg available words.
2-5, 24-27	2-5, 28-31	DQ1-DQ8	Input	Data I/O: Includes inputs, outputs or High-Z and/or Output masked data input (for MASKED WRITE cycle only).
	6, 9, 24, 25	NC	-	No Connect: These pins should be either left unconnected or tied to ground.
1, 14	1, 16	V_{CC}	Supply	Power Supply: +5V ±10% (C), 3.0/3.3V ±10% (LC)
15, 28	17, 32	V_{SS}	Supply	Ground

NEW ■ WIDE DRAM

FUNCTIONAL DESCRIPTION

Each bit is uniquely addressed through the 21 address bits during READ or WRITE cycles. First $\overline{RAS}$ is used to latch 12 bits (A0-A11) then $\overline{CAS}$ latches 9 bits (A0-A8).

The $\overline{CAS}$ control also determines whether the cycle will be a refresh cycle ($\overline{RAS}$-ONLY) or an active cycle (READ, WRITE or READ-WRITE) once $\overline{RAS}$ goes LOW.

READ or WRITE cycles are selected by $\overline{WE}$. A logic HIGH on $\overline{WE}$ dictates READ mode while a logic LOW on $\overline{WE}$ dictates WRITE mode. During a WRITE cycle, data in (D) is latched by the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. Taking $\overline{WE}$ LOW will initiate a WRITE cycle, selecting DQ1 through DQ8. If $\overline{WE}$ goes LOW prior to $\overline{CAS}$ going LOW, the output pin(s) remain open (High-Z) until the next $\overline{CAS}$ cycle. If $\overline{WE}$ goes LOW after $\overline{CAS}$ goes LOW and data reaches the output pins, data out (Q) is activated and retains the selected cell data as long as $\overline{CAS}$ and $\overline{OE}$ remain LOW (regardless of $\overline{WE}$ or $\overline{RAS}$). This late $\overline{WE}$ pulse results in a READ-WRITE cycle.

The eight data inputs and eight data outputs are routed through eight pins using common I/O, and pin direction is controlled by $\overline{OE}$ and $\overline{WE}$.

FAST PAGE MODE operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row address (A0-12) defined page boundary. The FAST PAGE MODE cycle is always initiated with a row address strobed-in by $\overline{RAS}$ followed by a column address strobed-in by $\overline{CAS}$. $\overline{CAS}$ may be toggled-in by holding $\overline{RAS}$ LOW and strobing-in different column addresses, thus executing faster memory cycles. Returning $\overline{RAS}$ HIGH terminates the FAST PAGE MODE operation.

Returning $\overline{RAS}$ and $\overline{CAS}$ HIGH terminates a memory cycle and decreases chip current to a reduced standby level. The chip is also preconditioned for the next cycle during the $\overline{RAS}$ high time. Memory cell data is retained in its correct state by maintaining power and executing any $\overline{RAS}$ cycle (READ, WRITE, $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$, or HIDDEN REFRESH) so that all 4,096 combinations of $\overline{RAS}$ addresses (A0-11) are executed at least every 512ms, regardless of sequence. The $\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh cycle will also invoke the refresh counter and controller for row address control.

BATTERY BACKUP MODE (BBU) is a CBR refresh performed at the extended refresh rate with CMOS input levels. This mode provides a very low current, data retention cycle. $\overline{RAS}$ or $\overline{CAS}$ time refers to the time at which $\overline{RAS}$ or $\overline{CAS}$ transition from HIGH to LOW).

SELF REFRESH is similar to BBU except that the DRAM provides its own internal clocking during "SLEEP MODE". Thus, an external clock is not required for additional power savings and design ease. The SELF REFRESH version retains the extended refresh rate of 512ms.

MASKED WRITE ACCESS CYCLE (MT4C2M8A2 S ONLY)

Every WRITE access cycle can be a MASKED WRITE, depending on the state of $\overline{WE}$ at $\overline{RAS}$ time. A MASKED WRITE is selected when $\overline{WE}$ is LOW at $\overline{RAS}$ time and mask data is supplied on the DQ pins.

The mask data present on the DQ1-DQ8 inputs at $\overline{RAS}$ time will be written to an internal mask data register and will then act as an individual write enable for each of the corresponding DQ inputs. If a LOW (logic "0") is written to a mask data register bit, the input port for that bit is disabled during the subsequent WRITE operation and no new data will be written to that DRAM cell location. A HIGH (logic "1") on a mask data register bit enables the input port and allows normal WRITE operations to proceed. At $\overline{CAS}$ time, the bits present on the DQ1-DQ8 inputs will be written to the DRAM (if the mask data bit was HIGH) or ignored (if the mask data bit was LOW).

In nonpersistent MASKED WRITEs, new mask data must be supplied each time a MASKED WRITE cycle is initiated.

Figure 1 illustrates the MT4C2M8A2 S MASKED WRITE operation (Note: $\overline{RAS}$ or $\overline{CAS}$ time refers to the time at which $\overline{RAS}$ or $\overline{CAS}$ transition from HIGH to LOW).

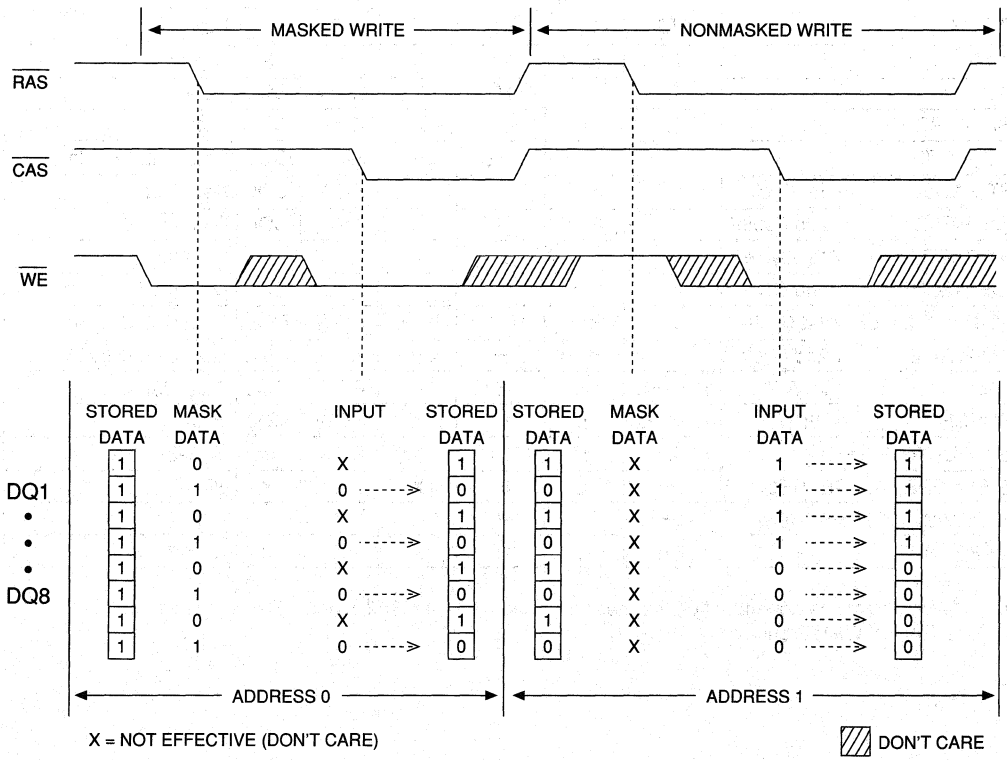


Figure 1
MT4C2M8A2 S MASKED WRITE EXAMPLE

TRUTH TABLE

FUNCTION		RAS	CAS	WE	OE	ADDRESSES tR	ADDRESSES tC	DQs	NOTES
Standby		H	H→X	X	X	X	X	High-Z	
READ		L	L	H	L	ROW	COL	Data Out	
EARLY-WRITE		L	L	L	X	ROW	COL	Data In	1
READ-WRITE		L	L	H→L	L→H	ROW	COL	Data Out, Data In	1
FAST-PAGE-	1st Cycle	L	H→L	H	L	ROW	COL	Data Out	
MODE READ	2nd Cycle	L	H→L	H	L	n/a	COL	Data Out	
FAST-PAGE-	1st Cycle	L	H→L	L	X	ROW	COL	Data In	1
MODE WRITE	2nd Cycle	L	H→L	L	X	n/a	COL	Data In	1
FAST-PAGE-MODE	1st Cycle	L	H→L	H→L	L→H	ROW	COL	Data Out, Data In	1
READ-WRITE	2nd Cycle	L	H→L	H→L	L→H	n/a	COL	Data Out, Data In	1
HIDDEN	READ	L→H→L	L	H	L	ROW	COL	Data Out	
REFRESH	WRITE	L→H→L	L	L	X	ROW	COL	Data In	1, 2
RAS-ONLY REFRESH		L	H	X	X	ROW	n/a	High-Z	
CAS-BEFORE-RAS REFRESH		H→L	L	H	X	X	X	High-Z	
BATTERY BACKUP REFRESH		H→L	L	H	X	X	X	High-Z	
SELF REFRESH		H→L	L	H	X	X	X	High-Z	

NOTE: 1. Data in will be dependent on the mask provided (MT4C2M8A2 S only). Refer to Figure 1.
2. EARLY WRITE only.

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS} (5V) .....-1V to +7V
Voltage on V_{CC} supply relative to V_{SS} (3V) ....-1V to +4.6V
Operating Temperature, T_A (Ambient) .....0°C to +70°C
Storage Temperature (Plastic) .....-55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC OPERATING SPECIFICATIONS FOR 5V VERSION

(Notes: 1, 3, 4, 6, 7, 30) (0°C ≤ T_A ≤ 70°C; V_{CC} = 5V ±10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.5	V	1, 30
Input High (Logic 1) Voltage, All Inputs	V_{IH}	2.4	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, All Inputs	V_{IL}	-1.0	0.8	V	1
INPUT LEAKAGE CURRENT Any Input 0V ≤ V_{IN} ≤ Vcc (All other pins not under test = 0V)	I_I	-2	2	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled, 0V ≤ V_{OUT} ≤ 5.5V)	I_{OZ}	-10	10	µA	
OUTPUT LEVELS Output High Voltage (I_{OUT} = -2.5mA)	V_{OH}	2.4		V	
Output Low Voltage (I_{OUT} = 2.1mA)	V_{OL}		0.4	V	

DC OPERATING SPECIFICATIONS FOR 3.0/3.3V VERSION

(Notes: 1, 3, 4, 6, 7, 31) (0°C ≤ T_A ≤ 70°C; V_{CC} = 3.0/3.3V ±10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	2.7	3.6	V	1, 31
Input High (Logic 1) Voltage, All Inputs	V_{IH}	2.0	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, All Inputs	V_{IL}	-1.0	0.8	V	1
INPUT LEAKAGE CURRENT Any Input 0V ≤ V_{IN} ≤ Vcc (All other pins not under test = 0V)	I_I	-2	2	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled, 0V ≤ V_{OUT} ≤ 3.6V)	I_{OZ}	-10	10	µA	
OUTPUT LEVELS Output High Voltage (I_{OUT} = -2mA)	V_{OH}	2.4		V	
Output Low Voltage (I_{OUT} = 2mA)	V_{OL}		0.4	V	

DC OPERATING SPECIFICATIONS FOR 5V VERSION

(Notes: 1, 3, 4, 6, 7, 30) (0°C ≤ T_A ≤ 70°C; Vcc = 5V ±10%)

		MAX				
PARAMETER/CONDITION	**SYMBOL**	**-6**	**-7**	**-8**	**UNITS**	**NOTES**
STANDBY CURRENT: TTL ($\overline{RAS}$ = $\overline{CAS}$ = VIH)	ICC1	2	2	2	mA	
STANDBY CURRENT: CMOS ($\overline{RAS}$ = $\overline{CAS}$ = Vcc -0.2V)	ICC2	200	200	200	µA	25
OPERATING CURRENT: Random READ/WRITE Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: tRC = tRC (MIN))	ICC3	110	100	90	mA	3, 4, 32
OPERATING CURRENT: FAST PAGE MODE Average power supply current ($\overline{RAS}$ = VIL, $\overline{CAS}$, Address Cycling: tPC = tPC (MIN); tCP, tASC = 10ns)	ICC4	80	70	60	mA	3, 4, 32
REFRESH CURRENT: $\overline{RAS}$-ONLY Average power supply current ($\overline{RAS}$ Cycling, $\overline{CAS}$ = VIH: tRC = tRC (MIN))	ICC5	110	100	90	mA	3, 32
REFRESH CURRENT: $\overline{CAS}$-BEFORE-$\overline{RAS}$ Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: tRC = tRC (MIN))	ICC6	110	100	90	mA	3, 5
REFRESH CURRENT: BATTERY BACKUP (BBU) Average power supply current during BATTERY BACKUP refresh: $\overline{CAS}$ = 0.2V or $\overline{CAS}$-BEFORE-$\overline{RAS}$ cycling; $\overline{RAS}$ = tRAS (MIN) to 300ns; $\overline{WE}$, A0-A11 and DIN = Vcc - 0.2V (DIN may be left open), tRC = 125µs (1,024 rows at 125µs = 128ms)	ICC7	300	300	300	µA	3, 30
REFRESH CURRENT: SELF Average power supply current during SELF refresh: CBR cycle with $\overline{RAS}$ ≥ tRASS (MIN) and $\overline{CAS}$ held LOW; $\overline{WE}$ = Vcc - 0.2V; A0-A9 and DIN = Vcc - 0.2V or 0.2V (DIN may be left open)	ICC8	300	300	300	µA	5

DC OPERATING SPECIFICATIONS FOR 3.0/3.3V VERSION

(Notes: 1, 3, 4, 6, 7, 31) ($0°C \le T_A \le 70°C$; V_{CC} = 3.0/3.3V ±10%)

		MAX				
PARAMETER/CONDITION	**SYMBOL**	**-6**	**-7**	**-8**	**UNITS**	**NOTES**
STANDBY CURRENT: TTL ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC1}	1	1	1	mA	
STANDBY CURRENT: CMOS ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} -0.2V)	I_{CC2}	80	80	80	µA	25
OPERATING CURRENT: Random READ/WRITE Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC (MIN))	I_{CC3}	80	70	60	mA	3, 4, 32
OPERATING CURRENT: FAST PAGE MODE Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: ^tPC = ^tPC (MIN); ^tCP, ^tASC = 10ns)	I_{CC4}	60	50	40	mA	3, 4, 32
REFRESH CURRENT: $\overline{RAS}$-ONLY Average power supply current ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}: ^tRC = ^tRC (MIN))	I_{CC5}	80	70	60	mA	3, 32
REFRESH CURRENT: $\overline{CAS}$-BEFORE-$\overline{RAS}$ Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC (MIN))	I_{CC6}	80	70	60	mA	3, 5
REFRESH CURRENT: BATTERY BACKUP (BBU) Average power supply current during BATTERY BACKUP refresh: $\overline{CAS}$ = 0.2V or $\overline{CAS}$-BEFORE-$\overline{RAS}$ cycling; $\overline{RAS}$ = ^tRAS (MIN) to 300ns; $\overline{WE}$, A0-A11 and D_{IN} = Vcc - 0.2V (D_{IN} may be left open), ^tRC = 125µs (1,024 rows at 125µs = 128ms)	I_{CC7}	100	100	100	µA	3, 30
REFRESH CURRENT: SELF Average power supply current during SELF refresh: CBR cycle with $\overline{RAS} \ge {}^tRASS$ (MIN) and $\overline{CAS}$ held LOW; $\overline{WE}$ = Vcc - 0.2V; A0-A9 and D_{IN} = Vcc - 0.2V or 0.2V (D_{IN} may be left open)	I_{CC8}	100	100	100	µA	5

NEW ■ WIDE DRAM

CAPACITANCE

PARAMETER	SYMBOL	MAX	UNITS	NOTES
Input Capacitance: A0-A11	C_{I1}	5	pF	2
Input Capacitance: $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$	C_{I2}	7	pF	2
Input/Output Capacitance: DQ	C_{IO}	7	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C ≤ T_A ≤ +70°C)

AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	^tRC	110		130		150		ns	
READ-WRITE cycle time	^tRWC	155		180		200		ns	
FAST-PAGE-MODE READ or WRITE cycle time	^tPC	35		40		40		ns	
FAST-PAGE-MODE READ-WRITE cycle time	^tPRWC	85		95		100		ns	
Access time from $\overline{RAS}$	^tRAC		60		70		80	ns	14
Access time from $\overline{CAS}$	^tCAC		15		20		20	ns	15
Output Enable	^tOE		15		15		15	ns	
Access time from column address	^tAA		30		35		40	ns	
Access time from $\overline{CAS}$ precharge	^tCPA		35		40		45	ns	
$\overline{RAS}$ pulse width	^tRAS	60	100,000	70	100,000	80	100,000	ns	
$\overline{RAS}$ pulse width (FAST PAGE MODE)	^tRASP	60	100,000	70	100,000	80	100,000	ns	
$\overline{RAS}$ hold time	^tRSH	15		20		20		ns	
$\overline{RAS}$ precharge time	^tRP	40		50		60		ns	
$\overline{CAS}$ pulse width	^tCAS	15	100,000	20	100,000	20	100,000	ns	
$\overline{CAS}$ hold time	^tCSH	60		70		80		ns	
$\overline{CAS}$ precharge time	^tCPN	10		10		10		ns	16
$\overline{CAS}$ precharge time (FAST PAGE MODE)	^tCP	10		10		10		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	^tRCD	15	45	20	50	20	60	ns	17
$\overline{CAS}$ to $\overline{RAS}$ precharge time	^tCRP	5		5		5		ns	
Row address setup time	^tASR	0		0		0		ns	
Row address hold time	^tRAH	10		10		10		ns	
$\overline{RAS}$ to column address delay time	^tRAD	15	30	15	35	15	40	ns	18
Column address setup time	^tASC	0		0		0		ns	
Column address hold time	^tCAH	10		15		15		ns	
Column address hold time (referenced to $\overline{RAS}$)	^tAR	50		55		60		ns	
Column address to $\overline{RAS}$ lead time	^tRAL	30		35		40		ns	
Read command setup time	^tRCS	0		0		0		ns	26
Read command hold time (referenced to $\overline{CAS}$)	^tRCH	0		0		0		ns	19, 26
Read command hold time (referenced to $\overline{RAS}$)	^tRRH	0		0		0		ns	19
$\overline{CAS}$ to output in Low-Z	^tCLZ	0		0		0		ns	
Output buffer turn-off delay	^tOFF	0	15	0	20	0	20	ns	20, 29

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

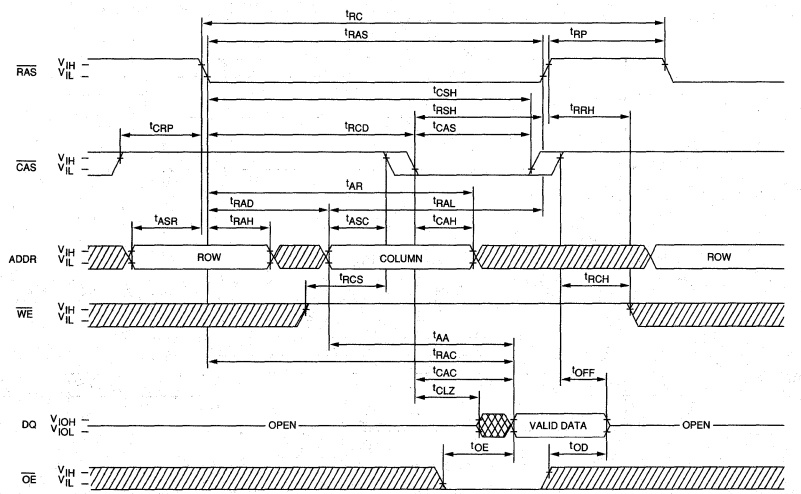
(Notes: 6, 7, 8, 9, 10, 11, 12, 13) ($0°C \le T_A \le +70°C$)

AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
$\overline{WE}$ command setup time	tWCS	0		0		0		ns	21, 26
Write command hold time	tWCH	10		15		15		ns	26
Write command hold time (referenced to $\overline{RAS}$)	tWCR	45		55		60		ns	26
Write command pulse width	tWP	10		15		15		ns	26
Write command to $\overline{RAS}$ lead time	tRWL	15		20		20		ns	26
Write command to $\overline{CAS}$ lead time	tCWL	15		20		20		ns	26
Data-in setup time	tDS	0		0		0		ns	22
Data-in hold time	tDH	10		15		15		ns	22
Data-in hold time (referenced to $\overline{RAS}$)	tDHR	45		55		60		ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	tRWD	85		95		105		ns	21
Column address to $\overline{WE}$ delay time	tAWD	55		60		65		ns	21
$\overline{CAS}$ to $\overline{WE}$ delay time	tCWD	40		45		45		ns	21
Transition time (rise or fall)	tT	3	50	3	50	3	50	ns	9, 10
Refresh period (4,096 cycles)	tREF		512		512		512	ms	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	tRPC	0		0		0		ns	
$\overline{CAS}$ setup time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	tCSR	5		5		5		ns	5
$\overline{CAS}$ hold time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	tCHR	15		15		15		ns	5
$\overline{WE}$ hold time (MASKED WRITE and $\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	tWRH	15		15		15		ns	26
$\overline{WE}$ setup time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	tWRP	10		10		10		ns	26
$\overline{WE}$ setup time (MASKED WRITE)	tWRS	10		10		10		ns	26
$\overline{OE}$ setup prior to RAS during HIDDEN REFRESH cycle	tORD	0		0		0		ns	
Output disable	tOD		15		15		15	ns	29
$\overline{OE}$ hold time from $\overline{WE}$ during READ-MODIFY-WRITE cycle	tOEH	15		15		15		ns	28
$\overline{RAS}$ pulse width during SELF REFRESH cycle	tRASS	100		100		100		µs	
$\overline{RAS}$ precharge time during SELF REFRESH cycle	tRPS	150		150		150		ns	
$\overline{CAS}$ hold time during SELF REFRESH cycle	tCHS	-70		-70		-70		ns	

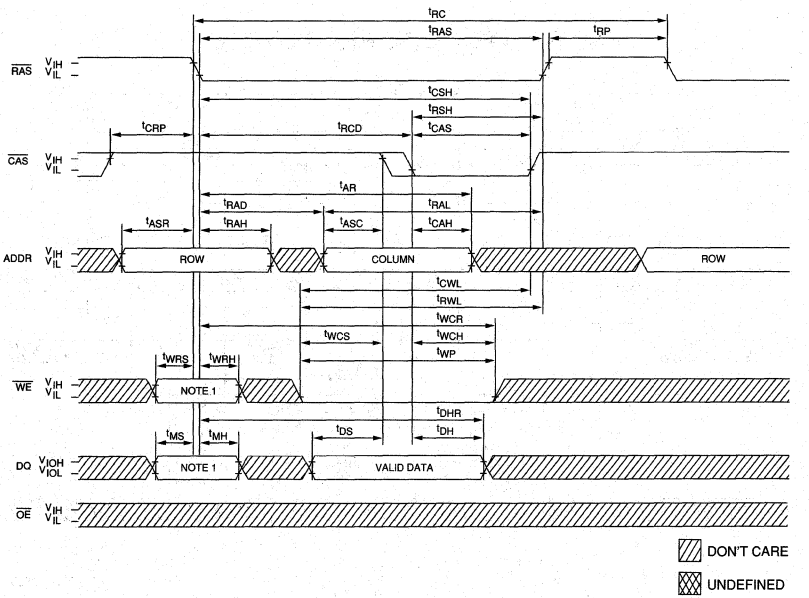
NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. V_{CC} = 5V ±10%, f = 1 MHz.
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \le T_A \le 70°C$) is assured.
7. An initial pause of 100µs is required after power-up followed by eight $\overline{RAS}$ refresh cycles ($\overline{RAS}$-ONLY or CBR) before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-up should be repeated any time the ^tREF refresh requirement is exceeded.
8. AC characteristics assume ^tT = 5ns.
9. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS}$ = V_{IH}, data output is high impedance.
12. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to 1 TTL gate and 50pF.
14. Assumes that $^tRCD < {}^tRCD$ (MAX). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
15. Assumes that $^tRCD \ge {}^tRCD$ (MAX).
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the Q buffer, $\overline{CAS}$ must be pulsed HIGH for ^tCPN.
17. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (MAX) limit, then access time is controlled exclusively by ^tCAC.
18. Operation within the ^tRAD limit ensures that ^tRCD (MAX) can be met. ^tRAD (MAX) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (MAX) limit, then access time is controlled exclusively by ^tAA.
19. Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
20. ^tOFF (MAX) defines the time at which the output achieves the open circuit condition, not a reference to V_{OH} or V_{OL}.
21. ^tWCS, ^tRWD, ^tAWD and ^tCWD are restrictive operating parameters in LATE-WRITE and READ-MODIFY-WRITE cycles only. If $^tWCS \ge {}^tWCS$ (MIN), the cycle is an EARLY-WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If $^tRWD \ge {}^tRWD$ (MIN), $^tAWD \ge {}^tAWD$ (MIN) and $^tCWD \ge {}^tCWD$ (MIN), the cycle is a READ-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of data out are indeterminate. $\overline{OE}$ held HIGH and $\overline{WE}$ taken LOW after $\overline{CAS}$ goes LOW results in a LATE-WRITE ($\overline{OE}$ controlled) cycle.
22. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY-WRITE cycles and $\overline{WE}$ leading edge in LATE-WRITE or READ-MODIFY-WRITE cycles.
23. During a READ cycle, if $\overline{OE}$ is LOW then taken HIGH before $\overline{CAS}$ goes HIGH, Q goes open. If $\overline{OE}$ is tied permanently LOW, LATE-WRITE or READ-MODIFY-WRITE operations are not possible.
24. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW and $\overline{OE}$ = HIGH.
25. All other inputs at Vcc -0.2V.
26. Write command is defined as $\overline{WE}$ going LOW.
27. MT4C2M8A2 S only.
28. LATE-WRITE and READ-MODIFY-WRITE cycles must have both ^tOD and ^tOEH met ($\overline{OE}$ HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. The DQs will provide the previously read data if $\overline{CAS}$ remains LOW and $\overline{OE}$ is taken back LOW after ^tOEH is met. If $\overline{CAS}$ goes HIGH prior to $\overline{OE}$ going back LOW, the DQs will remain open.
29. The DQs open during READ cycles once ^tOD or ^tOFF occur. If $\overline{CAS}$ goes HIGH first, $\overline{OE}$ becomes a "don't care." If $\overline{OE}$ goes HIGH and $\overline{CAS}$ stays LOW, $\overline{OE}$ is not a don't care; and the DQs will provide the previously read data if $\overline{OE}$ is taken back LOW (while $\overline{CAS}$ remains LOW).
30. BBU current is reduced as ^tRAS is reduced from its maximum specification during BBU cycle.
31. The 5V version is restricted to operate between 4.5 V and 5.5V only.
32. The 3.0/3.3V version is restricted to operate between 2.7 V and 3.6V only.
33. Column address changed once while $\overline{RAS}$ = V_{IL} and $\overline{CAS}$ = V_{IH}.

READ CYCLE



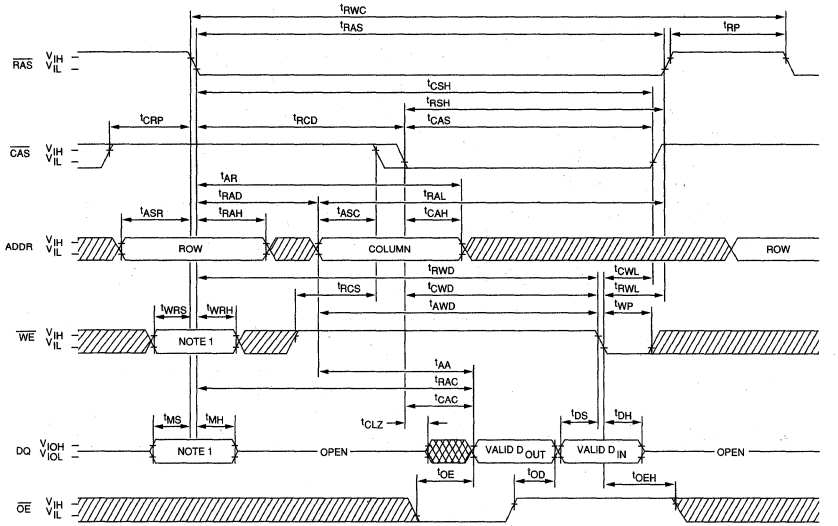
EARLY-WRITE CYCLE



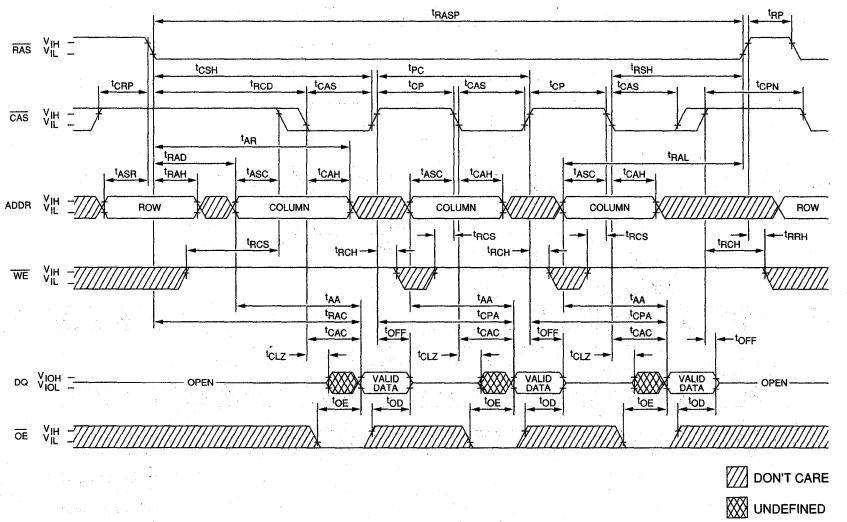
NOTE: 1. Applies to MT4C2M8A2 S only; $\overline{WE}$ and DQ inputs on MT4C2M8A1 S are "don't care" at $\overline{RAS}$ time. $\overline{WE}$ selects between normal WRITE and MASKED WRITE at $\overline{RAS}$ time. The DQ inputs are "don't care" for a normal WRITE ($\overline{WE}$ HIGH at $\overline{RAS}$ time). The DQ inputs provide the mask data at $\overline{RAS}$ time for a MASKED WRITE, $\overline{WE}$ LOW at $\overline{RAS}$ time.

NEW ■ WIDE DRAM

READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)

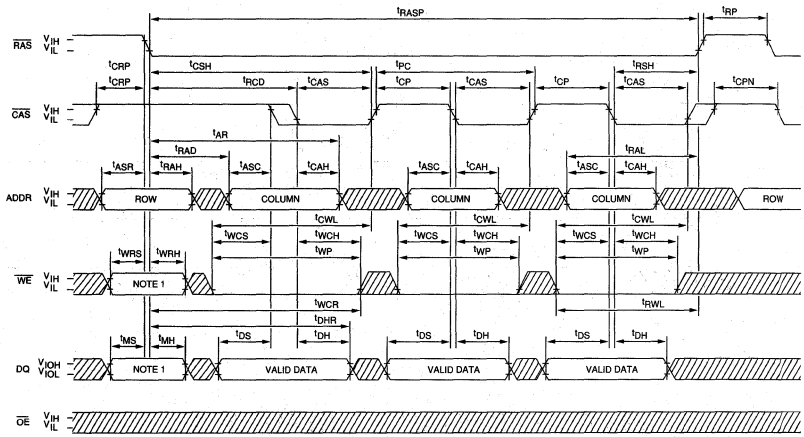


FAST-PAGE-MODE READ CYCLE

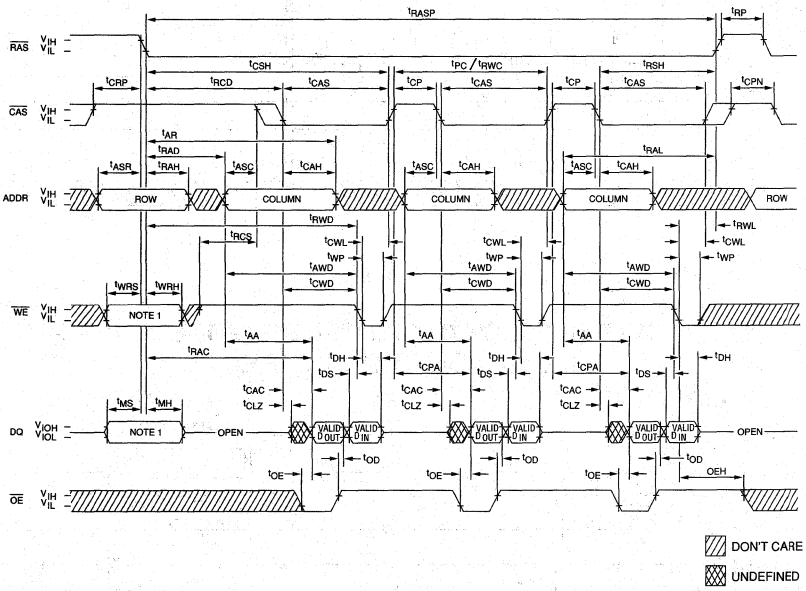


NOTE: 1. Applies to MT4C2M8A2 S only; $\overline{WE}$ and DQ inputs on MT4C2M8A1 S are "don't care" at $\overline{RAS}$ time. $\overline{WE}$ selects between normal WRITE and MASKED WRITE at $\overline{RAS}$ time. The DQ inputs are "don't care" for a normal WRITE ($\overline{WE}$ HIGH at $\overline{RAS}$ time). The DQ inputs provide the mask data at $\overline{RAS}$ time for a MASKED WRITE, $\overline{WE}$ LOW at $\overline{RAS}$ time.

FAST-PAGE-MODE EARLY-WRITE CYCLE



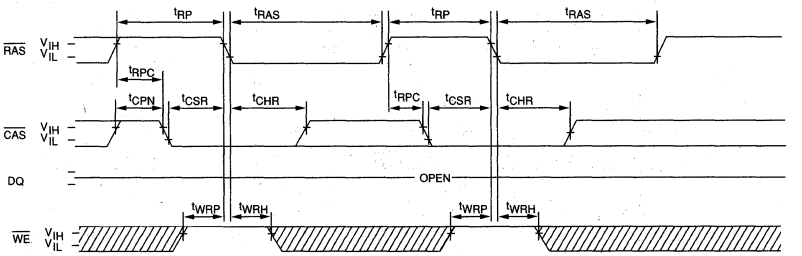
FAST-PAGE-MODE READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)



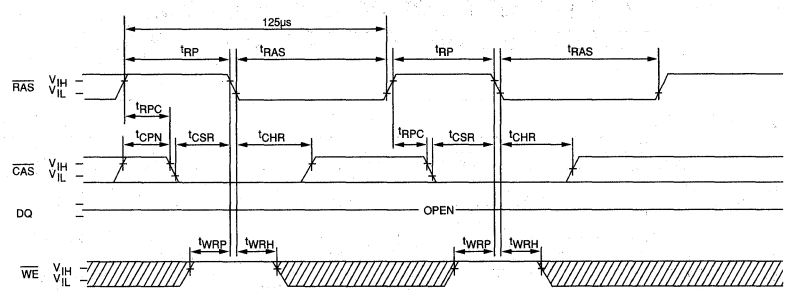
NOTE: 1. Applies to MT4C2M8A2 S only; $\overline{WE}$ and DQ inputs on MT4C2M8A1 S are "don't care" at $\overline{RAS}$ time. $\overline{WE}$ selects between normal WRITE and MASKED WRITE at $\overline{RAS}$ time. The DQ inputs are "don't care" for a normal WRITE ($\overline{WE}$ HIGH at $\overline{RAS}$ time). The DQ inputs provide the mask data at $\overline{RAS}$ time for a MASKED WRITE, $\overline{WE}$ LOW at $\overline{RAS}$ time.

NEW ■ WIDE DRAM

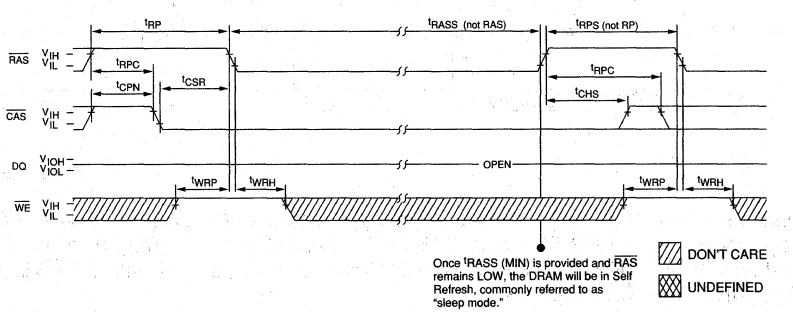
CAS-BEFORE-RAS REFRESH CYCLE
(A0-A11; OE = DON'T CARE)



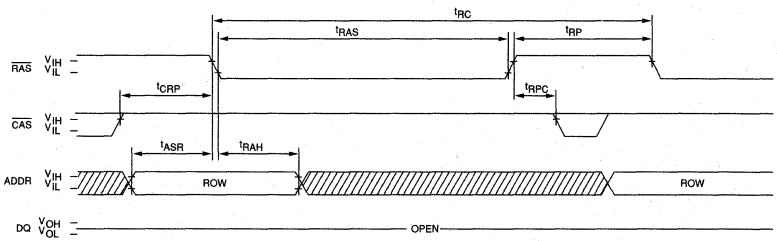
BATTERY BACKUP REFRESH CYCLE
(A0-A11; OE = DON'T CARE)



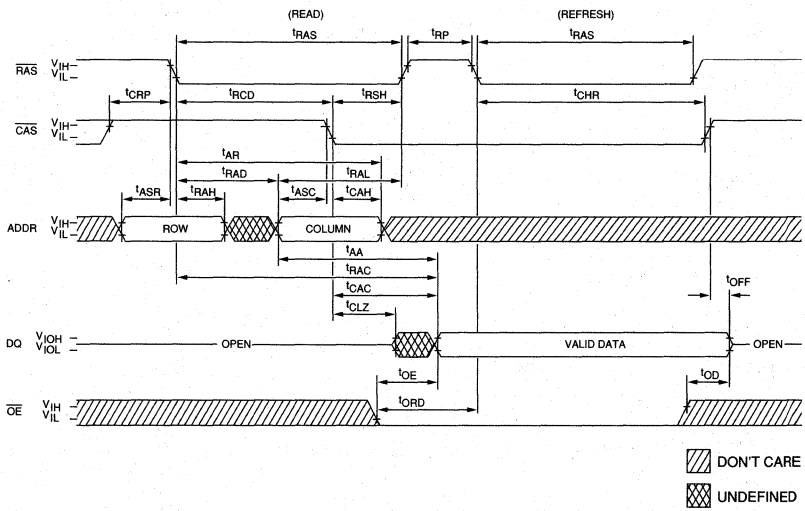
SELF REFRESH CYCLE ("SLEEP MODE")
(A0-A11; OE = DON'T CARE)



RAS-ONLY REFRESH CYCLE
($\overline{OE}$ and $\overline{WE}$ = DON'T CARE)



HIDDEN REFRESH CYCLE [24]
($\overline{WE}$ = HIGH; $\overline{OE}$ = LOW)



NEW WIDE DRAM

DRAM

2 MEG x 8 DRAM

5.0V SELF REFRESH (MT4C2M8B1/2 S)
3.0/3.3V, SELF REFRESH (MT4LC2M8B1/2 S)

FEATURES

- SELF REFRESH, i.e. "Sleep Mode"
- Industry standard x8 pinouts, timing, functions and packages
- Address entry: 11 row, 10 column addresses (256ms);
- High-performance, CMOS silicon-gate process
- Single +5V only or 3/3.3V only ±10% power supply
- All device pins are fully TTL compatible
- Refresh modes: RAS-ONLY, CAS-BEFORE-RAS (CBR), HIDDEN and BATTERY BACKUP (BBU)
- Optional FAST PAGE MODE access cycle
- NONPERSISTENT MASKED WRITE access cycle (MT4(L)C2M8B2 S only)
- 2,048-cycle refresh (4,096-cycle refresh available as MT4(L)C2M8A1/2 S)
- Low power, 2mW standby; 400mW active, typical (5V)

OPTIONS — MARKING

- Timing
  - 60ns access — -6
  - 70ns access — -7
  - 80ns access — -8
- Power Supply
  - 5V ±10% only — 4C
  - 3.0/3.3V ±10% only — 4LC
- Masked Write
  - Not available — B1 S
  - Available — B2 S
- Packages
  - Plastic 28-pin SOJ (400 mil) — DJ
  - Plastic 28-pin TSOP (400 mil) — TG
  - Plastic 32-pin SOJ (400 mil) — DL
  - Plastic 32-pin TSOP (400 mil) — TL

NOTE: Available in die form. Please consult factory for die data sheets.

- Part Number Example: MT4C2M8B1DJ-7 S

PART DESCRIPTION

MT4C2M8B1 S	5.0V, non-masked write
MT4C2M8B2 S	5.0V, masked write
MT4LC2M8B1 S	3.0V/3.3V, non-masked write
MT4LC2M8B2 S	3.0V/3.3V, masked write

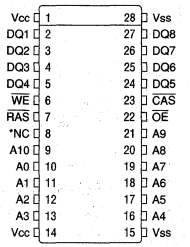
GENERAL DESCRIPTION

The MT4C2M8B1/2 S and MT4LC2M8B1/2 S are randomly accessed solid-state memories containing 16,777,216 bits organized in a x8 configuration. The MT4C2M8B1/2 S and the MT4LC2M8B1/2 S are the same DRAM versions except that the MT4LC2M8B1/2 S are low voltage versions of the MT4C2M8B1/2 S. The MT4LC2M8B1/2 S are designed to operate in either a 3.0V ±10% or a 3.3V ±10% memory system. All further references made for the MT4C2M8B1/2 S also apply to the MT4LC2M8B1/2 S, unless specifically stated otherwise. Each byte is uniquely addressed through the 21 address bits during READ or WRITE cycles. The address is entered first by RAS latching 11 bits (A0-A10) and then CAS latching 10 bits (A0-A10).

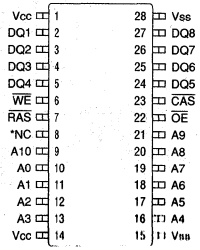
The MT4C2M8B2 S has NONPERSISTENT MASKED WRITE, allowing it to perform WRITE-PER-BIT accesses.

PIN ASSIGNMENT (Top View)

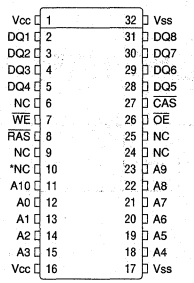
28-Pin SOJ (Q-4)



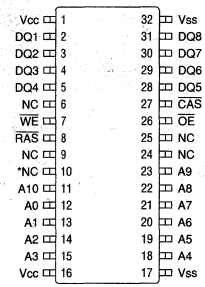
28-Pin TSOP (R-3)



32-Pin SOJ (Q-5)



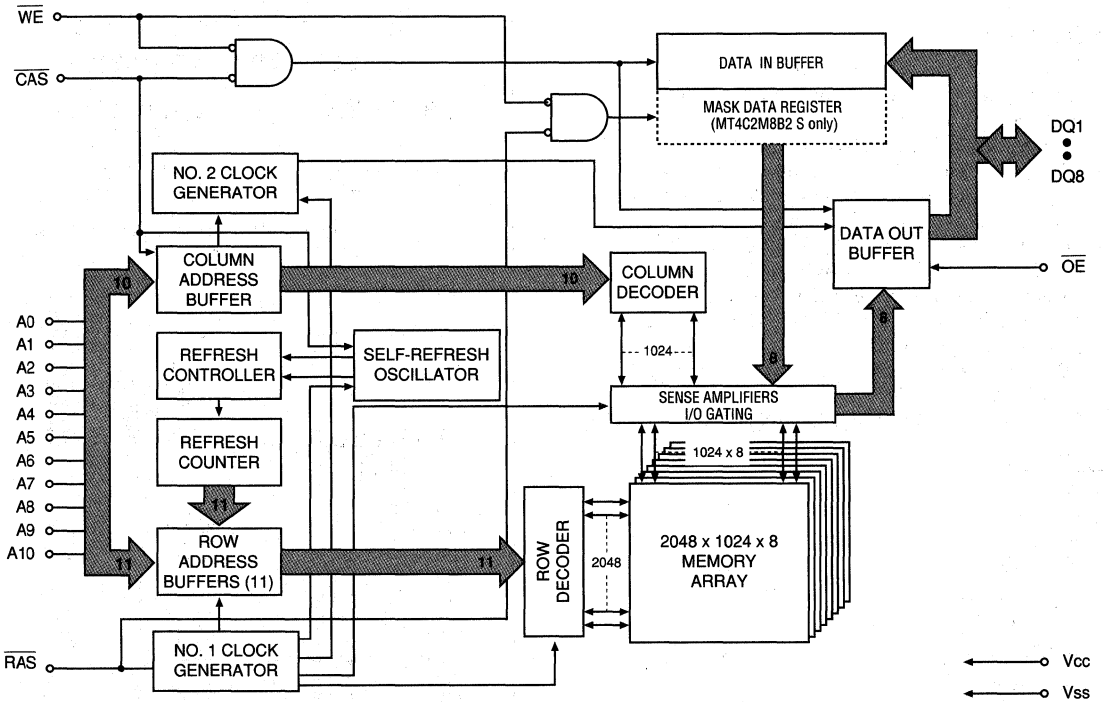
32-Pin TSOP (R-4)



*A11 on 12 row address version

NEW ■ WIDE DRAM

FUNCTIONAL BLOCK DIAGRAM
2,048 ROWS



PIN DESCRIPTIONS

28-PIN DEVICE PIN NUMBERS	32-PIN DEVICE PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
7	8	$\overline{RAS}$	Input	Row Address Strobe: $\overline{RAS}$ is used to clock-in the 11 row-address bits and strobe the $\overline{WE}$ and DQs in the MASKED WRITE mode (MT4C2M8B2 S only).
23	27	$\overline{CAS}$	Input	Column Address Strobe: $\overline{CAS}$ is used to clock-in the 10 column-address bits, enable the DRAM output buffers, and strobe the data inputs on WRITE cycles.
6	7	$\overline{WE}$	Input	Write Enable: $\overline{WE}$ is used to select a READ ($\overline{WE}$ = HIGH) or WRITE ($\overline{WE}$ = LOW) cycle. $\overline{WE}$ also serves as a Mask Enable ($\overline{WE}$ = LOW) at the falling edge of $\overline{RAS}$ in a MASKED-WRITE cycle (MT4C2M8B2 S).
22	26	$\overline{OE}$	Input	Output Enable: $\overline{OE}$ enables the output buffers when taken LOW during a READ access cycle. $\overline{RAS}$ and $\overline{CAS}$ must be LOW and $\overline{WE}$ must be HIGH before $\overline{OE}$ will control the output buffers. Otherwise the output buffers are in a High-Z state.
10-13, 16-21, 9	12-15, 18-23, 11	A0-A10	Input	Address Inputs: These inputs are multiplexed and clocked by $\overline{RAS}$ and $\overline{CAS}$ to select one byte out of the 2 Meg available words.
2-5, 24-27	2-5, 28-31	DQ1-DQ8	Input	Data I/O: Includes inputs, outputs or High-Z and/or Output masked data input (for MASKED WRITE cycle only).
8	6, 9, 24, 25, 10	NC	-	No Connect: These pins should be either left unconnected or tied to ground.
1, 14	1, 16	V_{CC}	Supply	Power Supply: +5V ±10% (C), 3.0/3.3V ±10% (LC)
15, 28	17, 32	V_{SS}	Supply	Ground

NEW ■ WIDE DRAM

FUNCTIONAL DESCRIPTION

Each bit is uniquely addressed through the 21 address bits during READ or WRITE cycles. First $\overline{RAS}$ is used to latch 11 bits (A0-A10) then $\overline{CAS}$ latches 10 bits (A0-A9).

The $\overline{CAS}$ control also determines whether the cycle will be a refresh cycle ($\overline{RAS}$-ONLY) or an active cycle (READ, WRITE or READ-WRITE) once $\overline{RAS}$ goes LOW.

READ or WRITE cycles are selected by $\overline{WE}$. A logic HIGH on $\overline{WE}$ dictates READ mode while a logic LOW on $\overline{WE}$ dictates WRITE mode. During a WRITE cycle, data in (D) is latched by the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. Taking $\overline{WE}$ LOW will initiate a WRITE cycle, selecting DQ1 through DQ8. If $\overline{WE}$ goes LOW prior to $\overline{CAS}$ going LOW, the output pin(s) remain open (High-Z) until the next $\overline{CAS}$ cycle. If $\overline{WE}$ goes LOW after $\overline{CAS}$ goes LOW and data reaches the output pins, data out (Q) is activated and retains the selected cell data as long as $\overline{CAS}$ and $\overline{OE}$ remain LOW (regardless of $\overline{WE}$ or $\overline{RAS}$). This late $\overline{WE}$ pulse results in a READ-WRITE cycle.

The eight data inputs and eight data outputs are routed through eight pins using common I/O, and pin direction is controlled by $\overline{OE}$ and $\overline{WE}$.

FAST PAGE MODE operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row address (A0-A11) defined page boundary. The FAST PAGE MODE cycle is always initiated with a row address strobed-in by $\overline{RAS}$ followed by a column address strobed-in by $\overline{CAS}$. $\overline{CAS}$ may be toggled-in by holding $\overline{RAS}$ LOW and strobing-in different column addresses, thus executing faster memory cycles. Returning $\overline{RAS}$ HIGH terminates the FAST PAGE MODE operation.

Returning $\overline{RAS}$ and $\overline{CAS}$ HIGH terminates a memory cycle and decreases chip current to a reduced standby level. The chip is also preconditioned for the next cycle during the $\overline{RAS}$ high time. Memory cell data is retained in its correct state by maintaining power and executing any $\overline{RAS}$ cycle (READ, WRITE, $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$, or HIDDEN REFRESH) so that all 2,048 combinations of $\overline{RAS}$ addresses (A0-A10) are executed at least every 256ms, regardless of sequence. The $\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh cycle will also invoke the refresh counter and controller for row address control.

BATTERY BACKUP MODE (BBU) is a CBR refresh performed at the extended refresh rate with CMOS input levels. This mode provides a very low current, data retention cycle. $\overline{RAS}$ or $\overline{CAS}$ time refers to the time at which $\overline{RAS}$ or $\overline{CAS}$ transition from HIGH to LOW).

SELF REFRESH is similar to BBU except that the DRAM provides its own internal clocking during "SLEEP MODE". Thus, an external clock is not required for additional power savings and design ease. The SELF REFRESH version retains the extended refresh rate of 512ms.

MASKED WRITE ACCESS CYCLE (MT4C2M8B2 S ONLY)

Every WRITE access cycle can be a MASKED WRITE, depending on the state of $\overline{WE}$ at $\overline{RAS}$ time. A MASKED WRITE is selected when $\overline{WE}$ is LOW at $\overline{RAS}$ time and mask data is supplied on the DQ pins.

The mask data present on the DQ1-DQ8 inputs at $\overline{RAS}$ time will be written to an internal mask data register and will then act as an individual write enable for each of the corresponding DQ inputs. If a LOW (logic "0") is written to a mask data register bit, the input port for that bit is disabled during the subsequent WRITE operation and no new data will be written to that DRAM cell location. A HIGH (logic "1") on a mask data register bit enables the input port and allows normal WRITE operations to proceed. At $\overline{CAS}$ time, the bits present on the DQ1-DQ8 inputs will be written to the DRAM (if the mask data bit was HIGH) or ignored (if the mask data bit was LOW).

In nonpersistent MASKED WRITEs, new mask data must be supplied each time a MASKED WRITE cycle is initiated.

Figure 1 illustrates the MT4C2M8B2 S MASKED WRITE operation (Note: $\overline{RAS}$ or $\overline{CAS}$ time refers to the time at which $\overline{RAS}$ or $\overline{CAS}$ transition from HIGH to LOW).

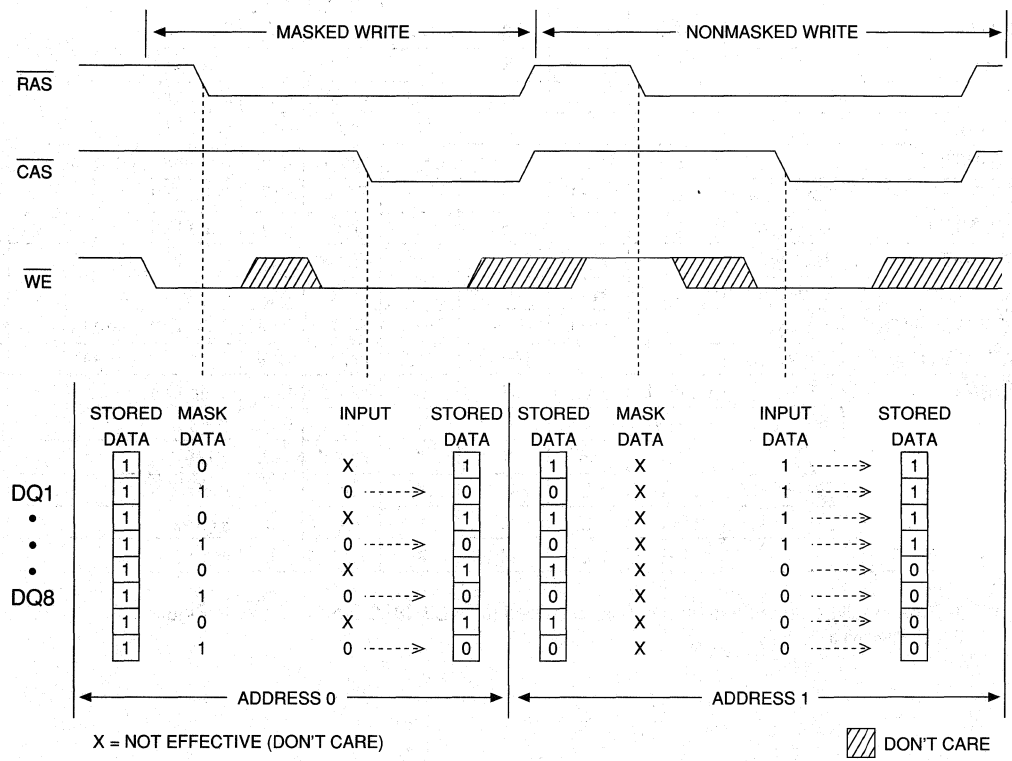


Figure 1
MT4C2M8B2 S MASKED WRITE EXAMPLE

TRUTH TABLE

FUNCTION		RAS	CAS	WE	OE	ADDRESSES tR	ADDRESSES tC	DQs	NOTES
Standby		H	H→X	X	X	X	X	High-Z	
READ		L	L	H	L	ROW	COL	Data Out	
EARLY-WRITE		L	L	L	X	ROW	COL	Data In	1
READ-WRITE		L	L	H→L	L→H	ROW	COL	Data Out, Data In	1
FAST-PAGE-	1st Cycle	L	H→L	H	L	ROW	COL	Data Out	
MODE READ	2nd Cycle	L	H→L	H	L	n/a	COL	Data Out	
FAST-PAGE-	1st Cycle	L	H→L	L	X	ROW	COL	Data In	1
MODE WRITE	2nd Cycle	L	H→L	L	X	n/a	COL	Data In	1
FAST-PAGE-MODE	1st Cycle	L	H→L	H→L	L→H	ROW	COL	Data Out, Data In	1
READ-WRITE	2nd Cycle	L	H→L	H→L	L→H	n/a	COL	Data Out, Data In	1
HIDDEN	READ	L→H→L	L	H	L	ROW	COL	Data Out	
REFRESH	WRITE	L→H→L	L	L	X	ROW	COL	Data In	1, 2
RAS-ONLY REFRESH		L	H	X	X	ROW	n/a	High-Z	
CAS-BEFORE-RAS REFRESH		H→L	L	H	X	X	X	High-Z	
BATTERY BACKUP REFRESH		H→L	L	H	X	X	X	High-Z	
SELF REFRESH		H→L	L	H	X	X	X	High-Z	

NOTE: 1. Data in will be dependent on the mask provided (MT4C2M8B2 S only). Refer to Figure 1.
2. EARLY WRITE only.

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS} (5V) .....-1V to +7V
Voltage on V_{CC} supply relative to V_{SS} (3V) ...-1V to +4.6V
Operating Temperature, T_A (Ambient) .....0°C to +70°C
Storage Temperature (Plastic) .....-55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC OPERATING SPECIFICATIONS FOR 5V VERSION

(Notes: 1, 3, 4, 6, 7, 30) ($0°C \le T_A \le 70°C$; V_{CC} = 5V ±10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.5	V	1, 30
Input High (Logic 1) Voltage, All Inputs	V_{IH}	2.4	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, All Inputs	V_{IL}	-1.0	0.8	V	1
INPUT LEAKAGE CURRENT Any Input 0V ≤ V_{IN} ≤ Vcc (All other pins not under test = 0V)	I_I	-2	2	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled, 0V ≤ V_{OUT} ≤ 5.5V)	I_{OZ}	-10	10	µA	
OUTPUT LEVELS Output High Voltage (I_{OUT} = -2.5mA)	V_{OH}	2.4		V	
Output Low Voltage (I_{OUT} = 2.1mA)	V_{OL}		0.4	V	

DC OPERATING SPECIFICATIONS FOR 3.0/3.3V VERSION

(Notes: 1, 3, 4, 6, 7, 31) ($0°C \le T_A \le 70°C$; V_{CC} = 3.0/3.3V ±10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	2.7	3.6	V	1, 31
Input High (Logic 1) Voltage, All Inputs	V_{IH}	2.0	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, All Inputs	V_{IL}	-1.0	0.8	V	1
INPUT LEAKAGE CURRENT Any Input 0V ≤ V_{IN} ≤ Vcc (All other pins not under test = 0V)	I_I	-2	2	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled, 0V ≤ V_{OUT} ≤ 3.6V)	I_{OZ}	-10	10	µA	
OUTPUT LEVELS Output High Voltage (I_{OUT} = -2mA)	V_{OH}	2.4		V	
Output Low Voltage (I_{OUT} = 2mA)	V_{OL}		0.4	V	

NEW ■ WIDE DRAM

DC OPERATING SPECIFICATIONS FOR 5V VERSION

(Notes: 1, 3, 4, 6, 7, 30) (0°C ≤ T_A ≤ 70°C; V_{CC} = 5V ±10%)

		MAX				
PARAMETER/CONDITION	**SYMBOL**	**-6**	**-7**	**-8**	**UNITS**	**NOTES**
STANDBY CURRENT: TTL ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC1}	2	2	2	mA	
STANDBY CURRENT: CMOS ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} -0.2V)	I_{CC2}	200	200	200	µA	25
OPERATING CURRENT: Random READ/WRITE Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC (MIN))	I_{CC3}	140	130	120	mA	3, 4, 32
OPERATING CURRENT: FAST PAGE MODE Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: ^tPC = ^tPC (MIN); ^tCP, ^tASC = 10ns)	I_{CC4}	100	90	80	mA	3, 4, 32
REFRESH CURRENT: $\overline{RAS}$-ONLY Average power supply current ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}: ^tRC = ^tRC (MIN))	I_{CC5}	140	130	120	mA	3, 32
REFRESH CURRENT: $\overline{CAS}$-BEFORE-$\overline{RAS}$ Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC (MIN))	I_{CC6}	140	130	120	mA	3, 5
REFRESH CURRENT: BATTERY BACKUP (BBU) Average power supply current during BATTERY BACKUP refresh: $\overline{CAS}$ = 0.2V or $\overline{CAS}$-BEFORE-$\overline{RAS}$ cycling; $\overline{RAS}$ = ^tRAS (MIN) to 300ns; $\overline{WE}$, A0-A11 and D_{IN} = Vcc - 0.2V (D_{IN} may be left open), ^tRC = 125µs (1,024 rows at 125µs = 128ms)	I_{CC7}	300	300	300	µA	3, 30
REFRESH CURRENT: SELF Average power supply current during SELF refresh: CBR cycle with $\overline{RAS}$ ≥ ^tRASS (MIN) and $\overline{CAS}$ held LOW; $\overline{WE}$ = V_{CC} - 0.2V; A0-A9 and D_{IN} = V_{CC} - 0.2V or 0.2V (D_{IN} may be left open)	I_{CC8}	300	300	300	µA	5

DC OPERATING SPECIFICATIONS FOR 3.0/3.3V VERSION

(Notes: 1, 3, 4, 6, 7, 31) ($0°C \le T_A \le 70°C$; V_{CC} = 3.0/3.3V ±10%)

		MAX				
PARAMETER/CONDITION	**SYMBOL**	**-6**	**-7**	**-8**	**UNITS**	**NOTES**
STANDBY CURRENT: TTL ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC1}	1	1	1	mA	
STANDBY CURRENT: CMOS ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} -0.2V)	I_{CC2}	80	80	80	µA	25
OPERATING CURRENT: Random READ/WRITE Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC (MIN))	I_{CC3}	90	90	80	mA	3, 4, 32
OPERATING CURRENT: FAST PAGE MODE Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: ^tPC = ^tPC (MIN); ^tCP, ^tASC = 10ns)	I_{CC4}	75	65	55	mA	3, 4, 32
REFRESH CURRENT: $\overline{RAS}$-ONLY Average power supply current ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}: ^tRC = ^tRC (MIN))	I_{CC5}	100	90	80	mA	3, 32
REFRESH CURRENT: $\overline{CAS}$-BEFORE-$\overline{RAS}$ Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC (MIN))	I_{CC6}	100	90	80	mA	3, 5
REFRESH CURRENT: BATTERY BACKUP (BBU) Average power supply current during BATTERY BACKUP refresh: $\overline{CAS}$ = 0.2V or $\overline{CAS}$-BEFORE-$\overline{RAS}$ cycling; $\overline{RAS}$ = ^tRAS (MIN) to 300ns; $\overline{WE}$, A0-A11 and D_{IN} = V_{CC} - 0.2V (D_{IN} may be left open), ^tRC = 125µs (1,024 rows at 125µs = 128ms)	I_{CC7}	100	100	100	µA	3, 30
REFRESH CURRENT: SELF Average power supply current during SELF refresh: CBR cycle with $\overline{RAS} \ge {}^tRASS$ (MIN) and $\overline{CAS}$ held LOW; $\overline{WE}$ = V_{CC} - 0.2V; A0-A9 and D_{IN} = V_{CC} - 0.2V or 0.2V (D_{IN} may be left open)	I_{CC8}	100	100	100	µA	5

NEW ■ WIDE DRAM

CAPACITANCE

PARAMETER	SYMBOL	MAX	UNITS	NOTES
Input Capacitance: A0-A10	C_{I1}	5	pF	2
Input Capacitance: $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$	C_{I2}	7	pF	2
Input/Output Capacitance: DQ	C_{IO}	7	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C ≤ T_A ≤ +70°C)

AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	^tRC	110		130		150		ns	
READ-WRITE cycle time	^tRWC	155		180		200		ns	
FAST-PAGE-MODE READ or WRITE cycle time	^tPC	35		40		40		ns	
FAST-PAGE-MODE READ-WRITE cycle time	^tPRWC	85		95		100		ns	
Access time from $\overline{RAS}$	^tRAC		60		70		80	ns	14
Access time from $\overline{CAS}$	^tCAC		15		20		20	ns	15
Output Enable	^tOE		15		15		15	ns	
Access time from column address	^tAA		30		35		40	ns	
Access time from $\overline{CAS}$ precharge	^tCPA		35		40		45	ns	
$\overline{RAS}$ pulse width	^tRAS	60	100,000	70	100,000	80	100,000	ns	
$\overline{RAS}$ pulse width (FAST PAGE MODE)	^tRASP	60	100,000	70	100,000	80	100,000	ns	
$\overline{RAS}$ hold time	^tRSH	15		20		20		ns	
$\overline{RAS}$ precharge time	^tRP	40		50		60		ns	
$\overline{CAS}$ pulse width	^tCAS	15	100,000	20	100,000	20	100,000	ns	
$\overline{CAS}$ hold time	^tCSH	60		70		80		ns	
$\overline{CAS}$ precharge time	^tCPN	10		10		10		ns	16
$\overline{CAS}$ precharge time (FAST PAGE MODE)	^tCP	10		10		10		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	^tRCD	15	45	20	50	20	60	ns	17
$\overline{CAS}$ to $\overline{RAS}$ precharge time	^tCRP	5		5		5		ns	
Row address setup time	^tASR	0		0		0		ns	
Row address hold time	^tRAH	10		10		10		ns	
$\overline{RAS}$ to column address delay time	^tRAD	15	30	15	35	15	40	ns	18
Column address setup time	^tASC	0		0		0		ns	
Column address hold time	^tCAH	10		15		15		ns	
Column address hold time (referenced to $\overline{RAS}$)	^tAR	50		55		60		ns	
Column address to $\overline{RAS}$ lead time	^tRAL	30		35		40		ns	
Read command setup time	^tRCS	0		0		0		ns	26
Read command hold time (referenced to $\overline{CAS}$)	^tRCH	0		0		0		ns	19, 26
Read command hold time (referenced to $\overline{RAS}$)	^tRRH	0		0		0		ns	19
$\overline{CAS}$ to output in Low-Z	^tCLZ	0		0		0		ns	
Output buffer turn-off delay	^tOFF	0	15	0	20	0	20	ns	20, 29

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

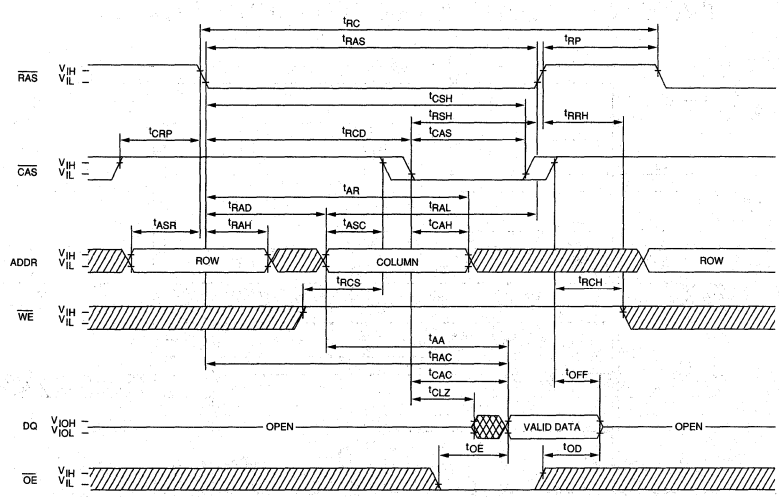
(Notes: 6, 7, 8, 9, 10, 11, 12, 13) ($0°C \le T_A \le +70°C$)

AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
$\overline{WE}$ command setup time	^tWCS	0		0		0		ns	21, 26
Write command hold time	^tWCH	10		15		15		ns	26
Write command hold time (referenced to $\overline{RAS}$)	^tWCR	45		55		60		ns	26
Write command pulse width	^tWP	10		15		15		ns	26
Write command to $\overline{RAS}$ lead time	^tRWL	15		20		20		ns	26
Write command to $\overline{CAS}$ lead time	^tCWL	15		20		20		ns	26
Data-in setup time	^tDS	0		0		0		ns	22
Data-in hold time	^tDH	10		15		15		ns	22
Data-in hold time (referenced to $\overline{RAS}$)	^tDHR	45		55		60		ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	^tRWD	85		95		105		ns	21
Column address to $\overline{WE}$ delay time	^tAWD	55		60		65		ns	21
$\overline{CAS}$ to $\overline{WE}$ delay time	^tCWD	40		45		45		ns	21
Transition time (rise or fall)	^tT	3	50	3	50	3	50	ns	9, 10
Refresh period (2,048 cycles)	^tREF		256		256		256	ms	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	^tRPC	0		0		0		ns	
$\overline{CAS}$ setup time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tCSR	5		5		5		ns	5
$\overline{CAS}$ hold time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tCHR	15		15		15		ns	5
$\overline{WE}$ hold time (MASKED WRITE and $\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tWRH	15		15		15		ns	26
$\overline{WE}$ setup time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tWRP	10		10		10		ns	26
$\overline{WE}$ setup time (MASKED WRITE)	^tWRS	10		10		10		ns	26
$\overline{OE}$ setup prior to RAS during HIDDEN REFRESH cycle	^tORD	0		0		0		ns	
Output disable	^tOD		15		15		15	ns	
$\overline{OE}$ hold time from $\overline{WE}$ during READ-MODIFY-WRITE cycle	^tOEH	15		15		15		ns	28
$\overline{RAS}$ pulse width during SELF REFRESH cycle	^tRASS	100		100		100		µs	34
$\overline{RAS}$ precharge time during SELF REFRESH cycle	^tRPS	150		150		150		ns	34
$\overline{CAS}$ hold time during SELF REFRESH cycle	^tCHS	-70		-70		-70		ns	34

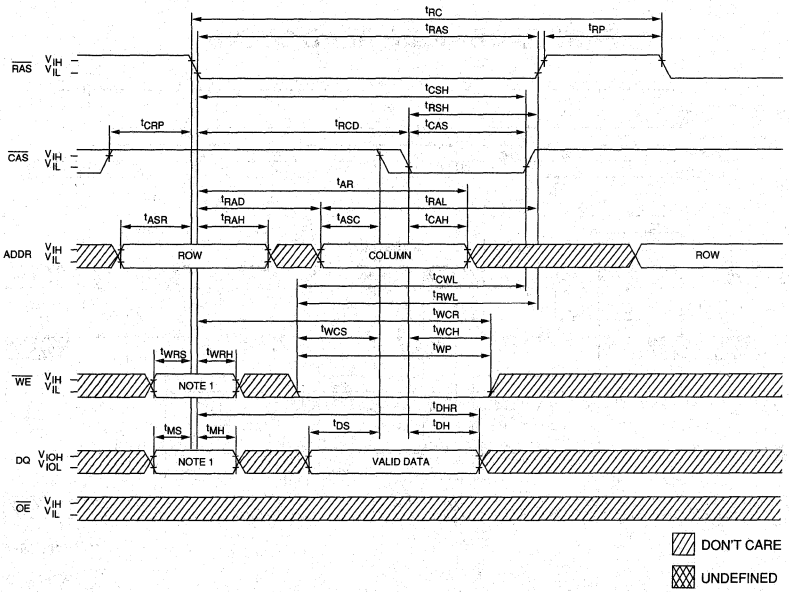
NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. V_{CC} = 5V ±10%, f = 1 MHz.
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is assured.
7. An initial pause of 100µs is required after power-up followed by eight $\overline{RAS}$ refresh cycles ($\overline{RAS}$-ONLY or CBR) before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-up should be repeated any time the ^tREF refresh requirement is exceeded.
8. AC characteristics assume ^tT = 5ns.
9. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS}$ = V_{IH}, data output is high impedance.
12. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to 1 TTL gate and 50pF.
14. Assumes that ^tRCD < ^tRCD (MAX). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
15. Assumes that ^tRCD ≥ ^tRCD (MAX).
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the Q buffer, $\overline{CAS}$ must be pulsed HIGH for ^tCPN.
17. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (MAX) limit, then access time is controlled exclusively by ^tCAC.
18. Operation within the ^tRAD limit ensures that ^tRCD (MAX) can be met. ^tRAD (MAX) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (MAX) limit, then access time is controlled exclusively by ^tAA.
19. Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
20. ^tOFF (MAX) defines the time at which the output achieves the open circuit condition, not a reference to V_{OH} or V_{OL}.
21. ^tWCS, ^tRWD, ^tAWD and ^tCWD are restrictive operating parameters in LATE-WRITE and READ-MODIFY-WRITE cycles only. If ^tWCS ≥ ^tWCS (MIN), the cycle is an EARLY-WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If ^tRWD ≥ ^tRWD (MIN), ^tAWD ≥ ^tAWD (MIN) and ^tCWD ≥ ^tCWD (MIN), the cycle is a READ-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of data out are indeterminate. $\overline{OE}$ held HIGH and $\overline{WE}$ taken LOW after $\overline{CAS}$ goes LOW results in a LATE-WRITE ($\overline{OE}$ controlled) cycle.
22. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY-WRITE cycles and $\overline{WE}$ leading edge in LATE-WRITE or READ-MODIFY-WRITE cycles.
23. During a READ cycle, if $\overline{OE}$ is LOW then taken HIGH before $\overline{CAS}$ goes HIGH, Q goes open. If $\overline{OE}$ is tied permanently LOW, LATE-WRITE or READ-MODIFY-WRITE operations are not possible.
24. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW and $\overline{OE}$ = HIGH.
25. All other inputs at Vcc -0.2V.
26. Write command is defined as $\overline{WE}$ going LOW.
27. MT4C2M8B2 S only.
28. LATE-WRITE and READ-MODIFY-WRITE cycles must have both ^tOD and ^tOEH met ($\overline{OE}$ HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. The DQs will provide the previously read data if $\overline{CAS}$ remains LOW and $\overline{OE}$ is taken back LOW after ^tOEH is met. If $\overline{CAS}$ goes HIGH prior to $\overline{OE}$ going back LOW, the DQs will remain open.
29. The DQs open during READ cycles once ^tOD or ^tOFF occur. If $\overline{CAS}$ goes HIGH first, $\overline{OE}$ becomes a "don't care." If $\overline{OE}$ goes HIGH and $\overline{CAS}$ stays LOW, $\overline{OE}$ is not a don't care; and the DQs will provide the previously read data if $\overline{OE}$ is taken back LOW (while $\overline{CAS}$ remains LOW).
30. BBU current is reduced as ^tRAS is reduced from its maximum specification during BBU cycle.
31. The 5V version is restricted to operate between 4.5 V and 5.5V only.
32. The 3.0/3.3V version is restricted to operate between 2.7 V and 3.6V only.
33. Column address changed once while $\overline{RAS}$ = V_{IL} and $\overline{CAS}$ = V_{IH}.
34. When exiting the SELF REFRESH mode, a complete set of row refreshes must be executed in order to ensure the DRAM will be fully refreshed.

READ CYCLE

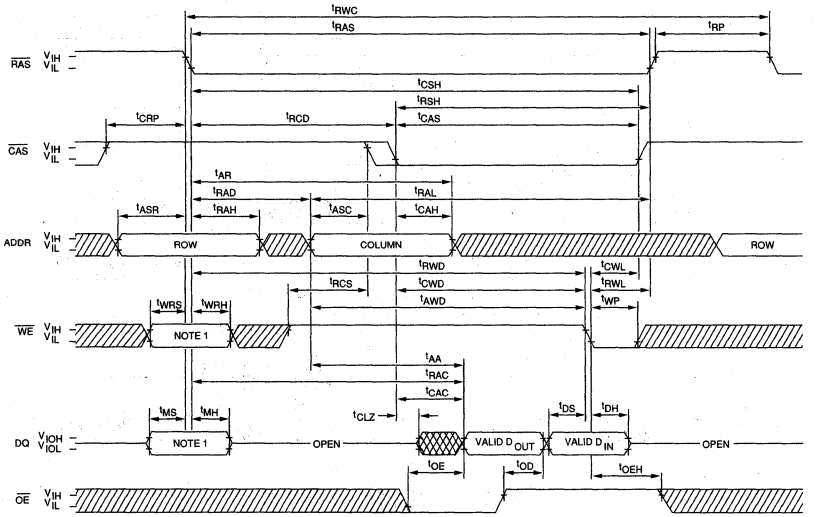


EARLY-WRITE CYCLE

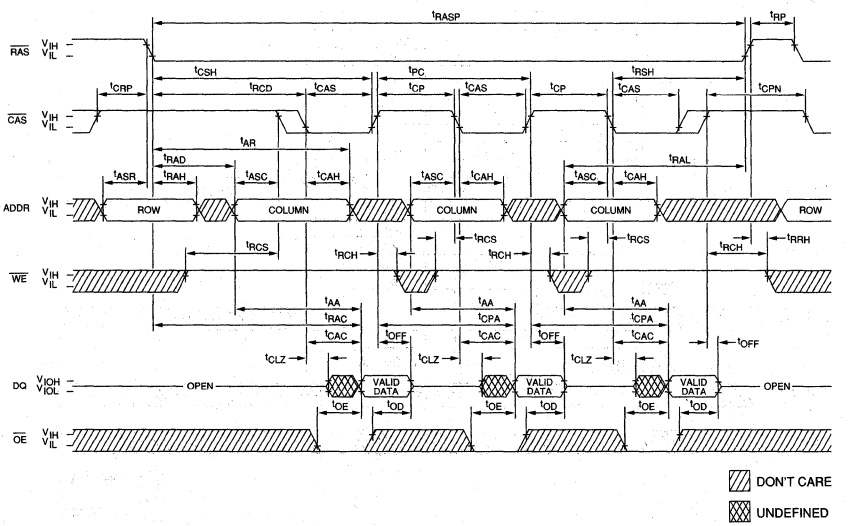


NOTE: 1. Applies to MT4C2M8B2 S only; $\overline{WE}$ and DQ inputs on MT4C2M8B1 S are "don't care" at $\overline{RAS}$ time. $\overline{WE}$ selects between normal WRITE and MASKED WRITE at $\overline{RAS}$ time. The DQ inputs are "don't care" for a normal WRITE ($\overline{WE}$ HIGH at $\overline{RAS}$ time). The DQ inputs provide the mask data at $\overline{RAS}$ time for a MASKED WRITE, $\overline{WE}$ LOW at $\overline{RAS}$ time.

READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)

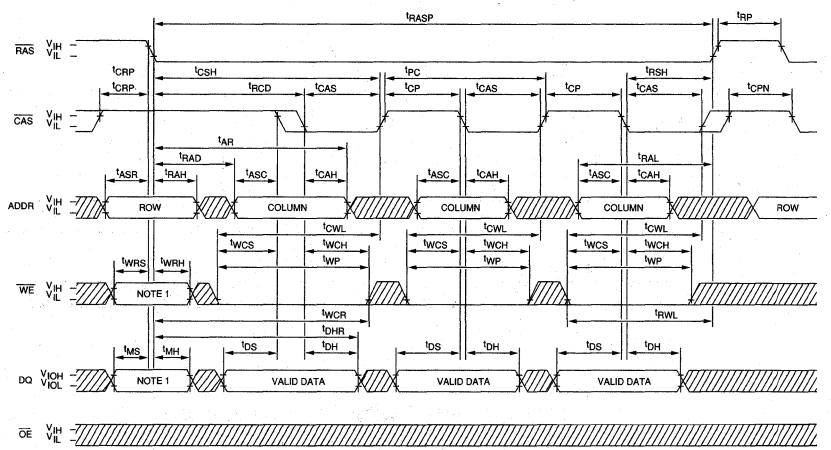


FAST-PAGE-MODE READ CYCLE

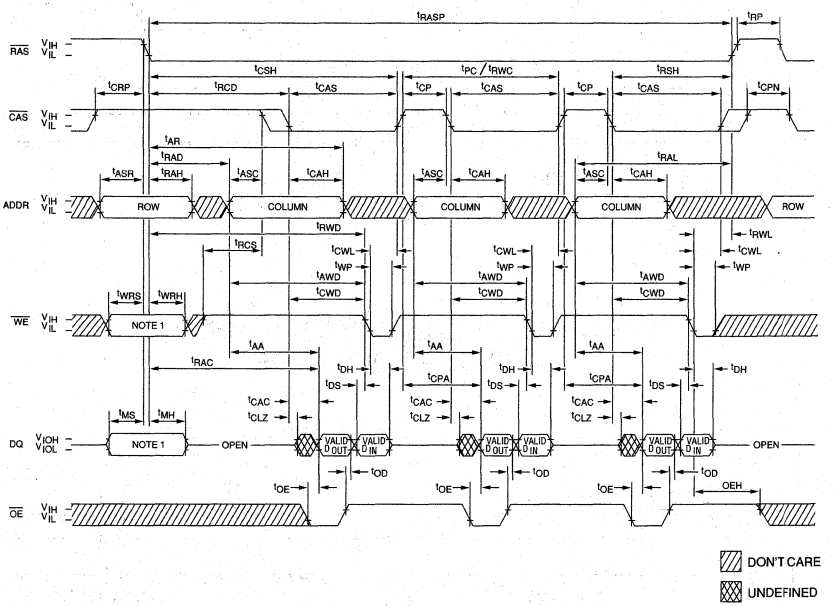


NOTE: 1. Applies to MT4C2M8B2 S only; $\overline{WE}$ and DQ inputs on MT4C2M8B1 S are "don't care" at $\overline{RAS}$ time. $\overline{WE}$ selects between normal WRITE and MASKED WRITE at $\overline{RAS}$ time. The DQ inputs are "don't care" for a normal WRITE ($\overline{WE}$ HIGH at $\overline{RAS}$ time). The DQ inputs provide the mask data at $\overline{RAS}$ time for a MASKED WRITE, $\overline{WE}$ LOW at $\overline{RAS}$ time.

FAST-PAGE-MODE EARLY-WRITE CYCLE

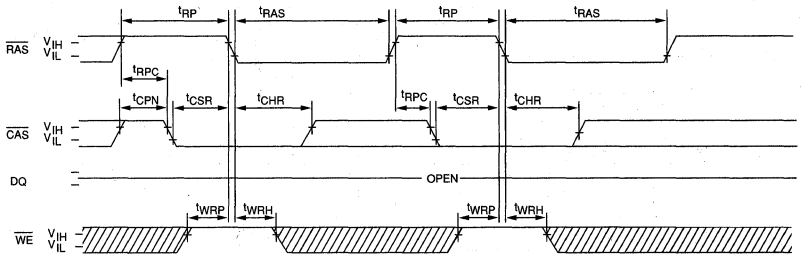


FAST-PAGE-MODE READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)

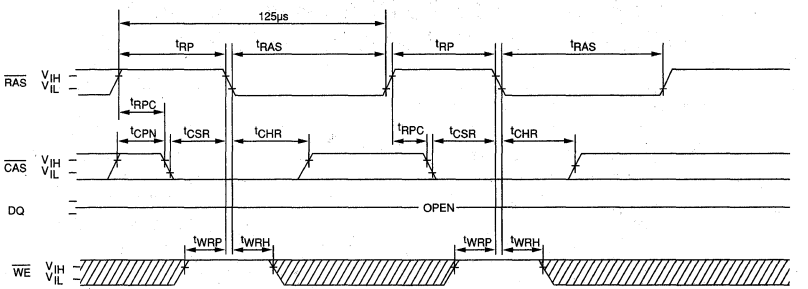


NOTE: 1. Applies to MT4C2M8B2 S only; $\overline{WE}$ and DQ inputs on MT4C2M8B1 S are "don't care" at $\overline{RAS}$ time. $\overline{WE}$ selects between normal WRITE and MASKED WRITE at $\overline{RAS}$ time. The DQ inputs are "don't care" for a normal WRITE ($\overline{WE}$ HIGH at $\overline{RAS}$ time). The DQ inputs provide the mask data at $\overline{RAS}$ time for a MASKED WRITE, $\overline{WE}$ LOW at $\overline{RAS}$ time.

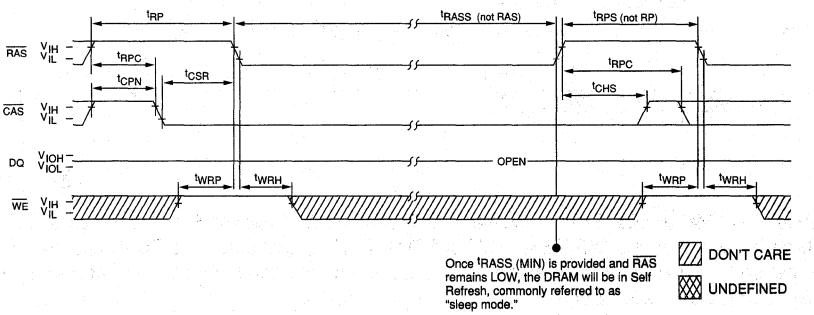
CAS-BEFORE-RAS REFRESH CYCLE
(A0-A10; OE = DON'T CARE)



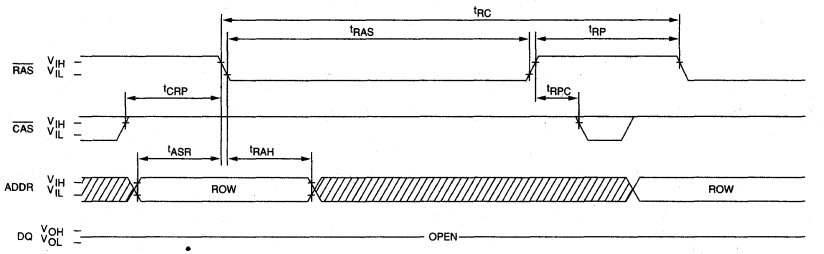
BATTERY BACKUP REFRESH CYCLE
(A0-A10; OE = DON'T CARE)



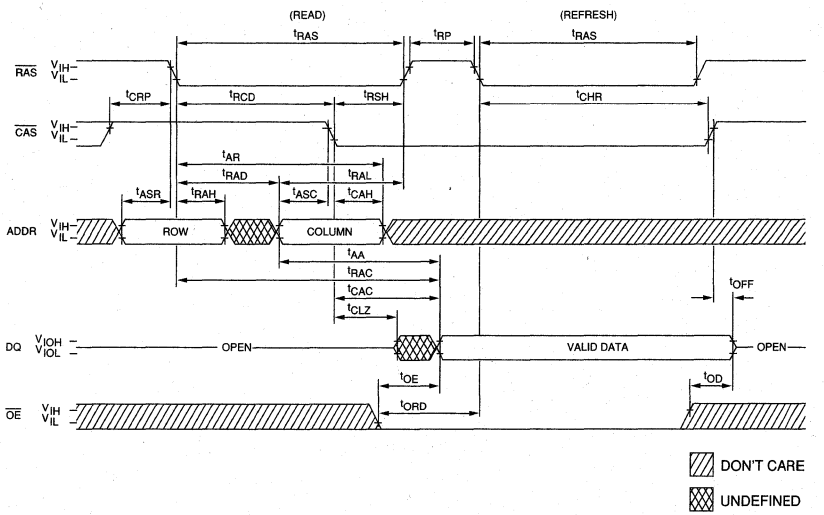
SELF REFRESH CYCLE ("SLEEP MODE")
(A0-A10; OE = DON'T CARE)



RAS-ONLY REFRESH CYCLE
(OE and WE = DON'T CARE)



HIDDEN REFRESH CYCLE [24]
(WE = HIGH; OE = LOW)



DRAM

64K x 16 DRAM

FAST PAGE MODE

FEATURES

- Industry standard x16 pinouts, timing, functions and packages
- High-performance, CMOS silicon-gate process
- Single +5V±10% power supply
- Low power, 3mW standby; 225mW active, typical
- All device pins are fully TTL compatible
- 256-cycle refresh in 4ms
- Refresh modes: $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$ and HIDDEN
- Optional FAST PAGE MODE access cycle
- BYTE WRITE access cycle (MT4C1664 only)
- NONPERSISTENT MASKED WRITE access cycle (MT4C1665 only)

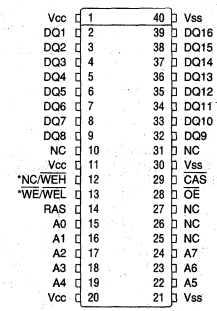
OPTIONS

	MARKING
• Timing	
70ns access	- 7
80ns access	- 8
100ns access	-10
• Write Enable	
Byte or Word	MT4C1664
Word only	MT4C1665
• Mask Enable	
Not Available	MT4C1664
Always Available	MT4C1665
• Packages	
Plastic SOJ (400mil)	DJ
Plastic TSOP (400mil)	TG
Plastic ZIP (475mil)	Z

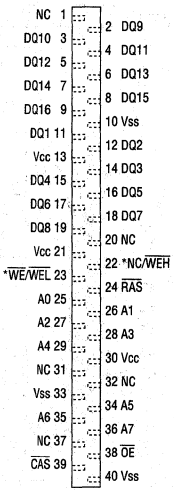
NOTE: Available in die form Please consult factory for die data sheets.

PIN ASSIGNMENT (Top View)

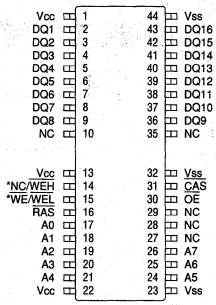
40-Pin SOJ (Q-6)



40-Pin Zip (O-4)



40-Pin TSOP (R-5)



*MT4C1665/MT4C1664

GENERAL DESCRIPTION

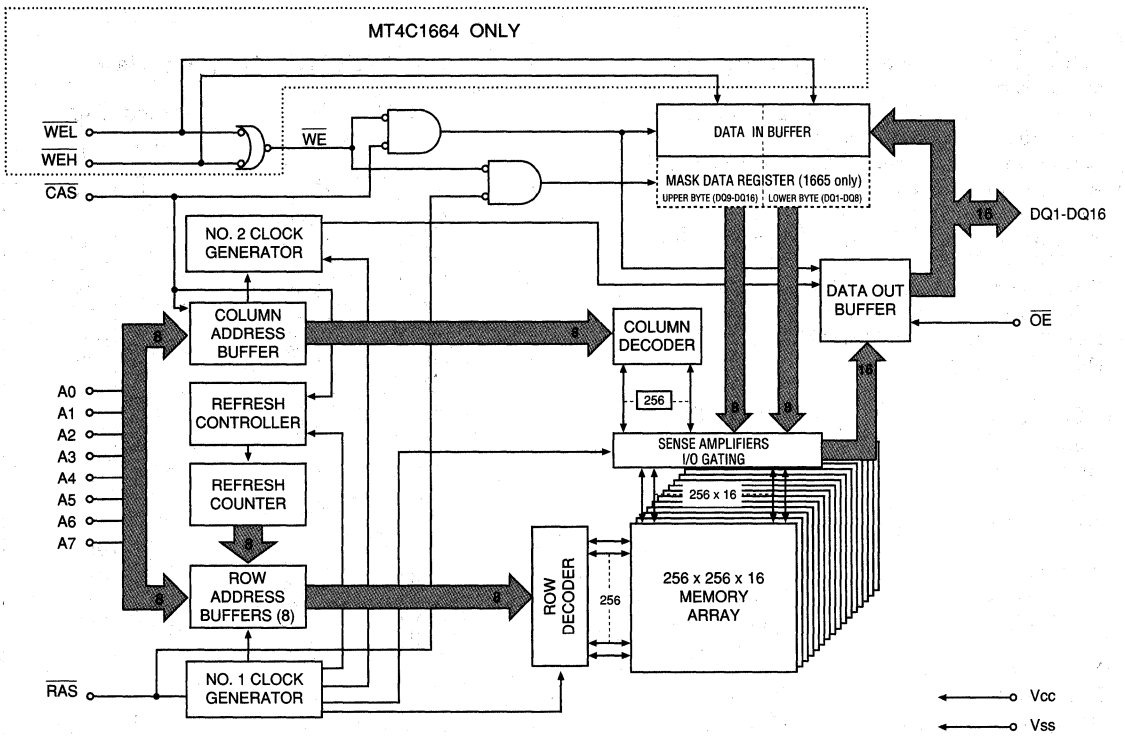
The MT4C1664/5 are randomly accessed solid-state memories containing 1,048,576 bits organized in a x16 configuration. The MT4C1664 has both BYTE and WORD WRITE access cycles while the MT4C1665 has only WORD WRITE access cycles.

The MT4C1664 functions in a similar manner to the MT4C1665 except that replacing $\overline{WE}$ with $\overline{WEL}$ and $\overline{WEH}$ allows for BYTE WRITE access cycles. $\overline{WEL}$ and $\overline{WEH}$ function in an identical manner to $\overline{WE}$: either $\overline{WEL}$ or $\overline{WEH}$ will generate an internal $\overline{WE}$ through an AND gate (Inverted NOR gate).

The MT4C1664 "$\overline{WE}$" function and timing are determined by the first BYTE WRITE ($\overline{WEL}$ or $\overline{WEH}$) to transition LOW and the last to transition back HIGH. Use of only one of the two results in a BYTE WRITE cycle: $\overline{WEL}$ transitioning LOW selects a WRITE cycle for the lower byte (DQ1-DQ8) or $\overline{WEH}$ transitioning LOW selects a WRITE cycle for the upper byte (DQ9-DQ16).

The MT4C1665 has NONPERSISTENT MASKED WRITE cycles.

FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTIONS

SOJ PIN NUMBERS	ZIP PIN NUMBERS	TSOP PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
14	24	16	$\overline{RAS}$	Input	ROW Address Strobe: $\overline{RAS}$ is used to clock-in the 8 row address bits and strobe the $\overline{WEL}$, $\overline{WEH}$ and DQ inputs for the MASKED WRITE function.
29	39	31	$\overline{CAS}$	Input	Column Address Strobe: $\overline{CAS}$ is used to clock-in the 8 column address bits, enable the DRAM output buffers, and strobe the data inputs on WRITE cycles.
28	38	30	$\overline{OE}$	Input	Output Enable: $\overline{OE}$ enables the output buffers when taken LOW during a READ access cycle. $\overline{RAS}$ and $\overline{CAS}$ must be LOW and $\overline{WEL}$ and $\overline{WEH}$ must be HIGH before $\overline{OE}$ will control the output buffers. Otherwise the output buffers are in a High-Z state.
13	23	15	$\overline{WE}$/$\overline{WEL}$*	Input	WRITE Enable Lower Byte: $\overline{WEL}$ on MT4C1664 is $\overline{WE}$ control for the DQ1 through DQ8 inputs. $\overline{WE}$ on MT4C1665 controls DQ1 through DQ16 inputs. If ($\overline{WEL}$ or $\overline{WEH}$)/$\overline{WE}$ is LOW, the access is a WRITE cycle. The DQ outputs for the byte not being written will remain in a High-Z state (byte WRITE cycle only).
12	22	14	NC/$\overline{WEH}$*	Input	Write Enable Upper Byte: $\overline{WEH}$ on MT4C1664 is $\overline{WE}$ control for the DQ9 through DQ16 inputs. If ($\overline{WEL}$ or $\overline{WEH}$)/$\overline{WE}$ is LOW, the access is a WRITE cycle. This pin is a no connect on the MT4C1665 as it has only WORD WRITE access cycles.
15-19, 22-24	25-29, 34-36	17-21, 24-26	A0-A7	Input	Address Inputs: These inputs are multiplexed and clocked by $\overline{RAS}$ and $\overline{CAS}$ to select one 16-bit word out of the 64K available words.
2-9, 32-39	11, 12, 14-17, 2, 18, 19, 3-9	2-9, 36-43	DQ1-DQ16	Input/ Output	Data I/O: For WRITE cycles, DQ1-DQ16 act as inputs to the addressed DRAM location. BYTE WRITEs can be performed by using $\overline{WEL}$ or $\overline{WEH}$ to select the byte to be written. For READ access cycles, DQ1-DQ16 act as outputs for the addressed DRAM ocation. All 16 I/Os are active for READ cycles (there is no BYTE READ cycle).
10, 25-27, 31	1, 20, 31, 32, 37	10, 27-29, 35	NC	-	No Connect: These pins should be either left unconnected or tied to ground.
1, 11, 20	13, 21, 30	1, 13, 22	Vcc	Supply	Power Supply: +5V ± 10%
21, 30, 40	10, 33, 40	23, 32, 44	Vss	Supply	Ground

NOTE: *MT4C1665/MT4C1664

FUNCTIONAL DESCRIPTION

Each bit is uniquely addressed through the 16 address bits during READ or WRITE cycles. These are entered 8 bits (A0-A7) at a time. $\overline{RAS}$ is used to latch the first 8 bits and $\overline{CAS}$ the latter 8 bits.

READ or WRITE cycles on the MT4C1665 are selected with the $\overline{WE}$ input while either $\overline{WEL}$ or $\overline{WEH}$ perform the "$\overline{WE}$" on the MT4C1664. The MT4C1664 "$\overline{WE}$" function is determined by the first BYTE WRITE ($\overline{WEL}$ or $\overline{WEH}$) to transition LOW and the last one to transition back HIGH.

A logic HIGH on $\overline{WE}$ dictates READ mode while a logic LOW on $\overline{WE}$ dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. Taking $\overline{WE}$ LOW will initiate a WRITE cycle, selecting DQ1 through DQ16. If $\overline{WE}$ goes LOW prior to $\overline{CAS}$ going LOW, the output pin(s) remain open (High-Z) until the next $\overline{CAS}$ cycle. If $\overline{WE}$ goes LOW after $\overline{CAS}$ goes LOW and data reaches the output pins, data out (Q) is activated and retains the selected cell data as long as $\overline{CAS}$ and $\overline{OE}$ remain LOW (regardless of $\overline{WE}$ or $\overline{RAS}$). This late $\overline{WE}$ pulse results in a READ-WRITE cycle.

The 16 data inputs and 16 data outputs are routed through 16 pins using common I/O, and pin direction is controlled by $\overline{OE}$, $\overline{WEL}$ and $\overline{WEH}$ (MT4C1664) or $\overline{WE}$ (MT4C1665).

FAST PAGE MODE operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row address (A0-A7) defined page boundary. The FAST PAGE MODE cycle is always initiated with a row address strobed-in by $\overline{RAS}$ followed by a column address strobed-in by $\overline{CAS}$. $\overline{CAS}$ may be toggled-in by holding $\overline{RAS}$ LOW and strobing-in different column addresses, thus executing faster memory cycles. Returning $\overline{RAS}$ HIGH terminates the FAST PAGE MODE operation.

Returning $\overline{RAS}$ and $\overline{CAS}$ HIGH terminates a memory cycle and decreases chip current to a reduced standby level. The chip is also preconditioned for the next cycle during the $\overline{RAS}$ high time. Memory cell data is retained in its correct state by maintaining power and executing any $\overline{RAS}$ cycle (READ, WRITE, $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$, or HIDDEN refresh) so that all 256 combinations of $\overline{RAS}$ addresses (A0-A7) are executed at least every 4ms, regardless of sequence. The $\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh cycle will also invoke the refresh counter and controller for row address control.

BYTE WRITE DESCRIPTION (MT4C1664 ONLY)

The BYTE WRITE mode is determined by the use of $\overline{WEL}$ and $\overline{WEH}$. Enabling $\overline{WEL}$ will select a lower BYTE WRITE cycle (DQ1-DQ8) while enabling $\overline{WEH}$ will select an upper BYTE WRITE (DQ9-DQ16). Enabling both $\overline{WEL}$ and $\overline{WEH}$ selects a WORD WRITE cycle.

The MT4C1664 can be viewed as two 64K x 8 DRAMs which have common input controls, with the exception of the WE input. Figure 1 illustrates the MT4C1664 BYTE and WORD WRITE cycles.

MASKED WRITE DESCRIPTION (MT4C1665 ONLY)

Every WRITE access cycle can be a MASKED WRITE, depending on the state of $\overline{WE}$ at $\overline{RAS}$ time. A MASKED WRITE is selected when mask data is supplied on the DQ pins and $\overline{WE}$ is LOW at $\overline{RAS}$ time. The MT4C1665 is only word selectable when $\overline{WE}$ is LOW at $\overline{RAS}$ time (the MT4C1664 does not have MASKED WRITE cycle function).

The data (mask data) present on the DQ1-DQ16 inputs at $\overline{RAS}$ time will be written to an internal bit mask data register and will then act as an individual write enable for each of the corresponding DQ inputs. If a LOW (logic "0") is written to a mask data register bit, the input port for that bit is disabled during the following WRITE operation and no new data will be written to that DRAM cell location. A HIGH (logic "1") on a mask data register bit enables the input port and allows normal WRITE operations to proceed. At $\overline{CAS}$ time, the bits present on the DQ1-DQ16 inputs will be either written to the DRAM (if the mask data bit was HIGH) or ignored (if the mask data bit was LOW).

New mask data must be supplied each time a MASKED WRITE cycle is initiated, even if the previous cycle's mask was the same mask.

Figure 2 illustrates the MT4C1665* MASKED WRITE operation (Note: $\overline{RAS}$ or $\overline{CAS}$ time refers to the time at which $\overline{RAS}$ or $\overline{CAS}$ transition from HIGH to LOW).

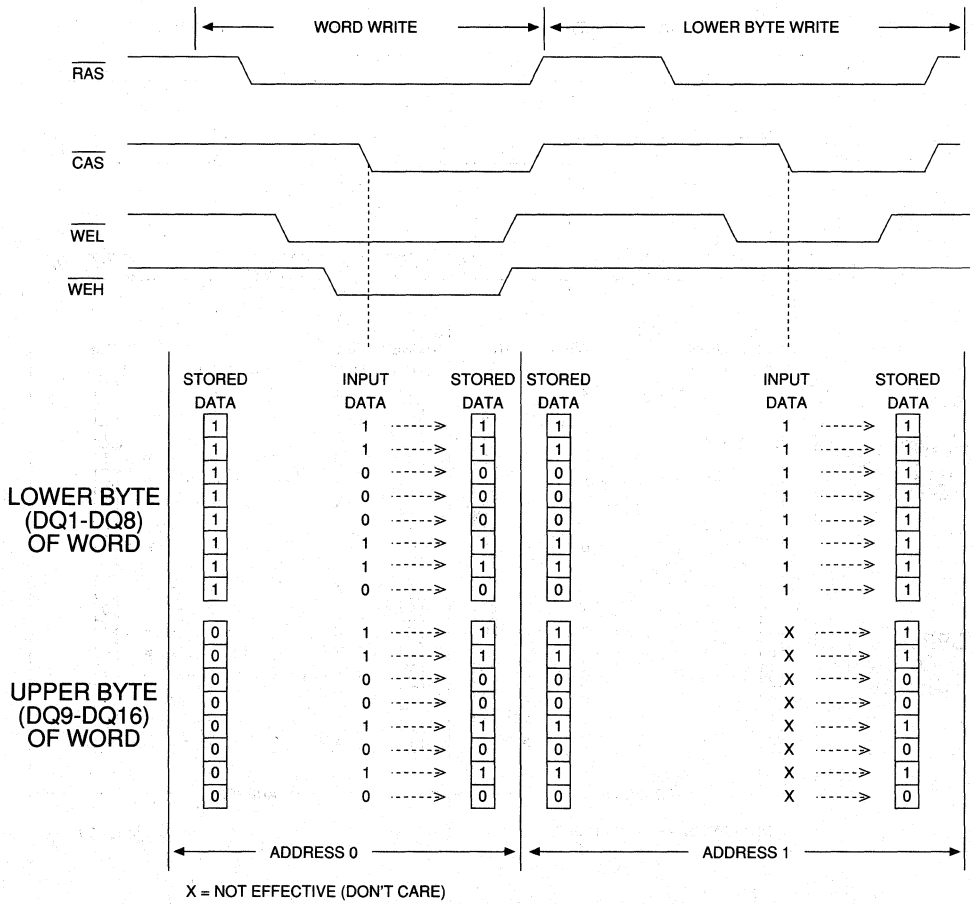


Figure 1
MT4C1664 WORD AND BYTE WRITE EXAMPLE

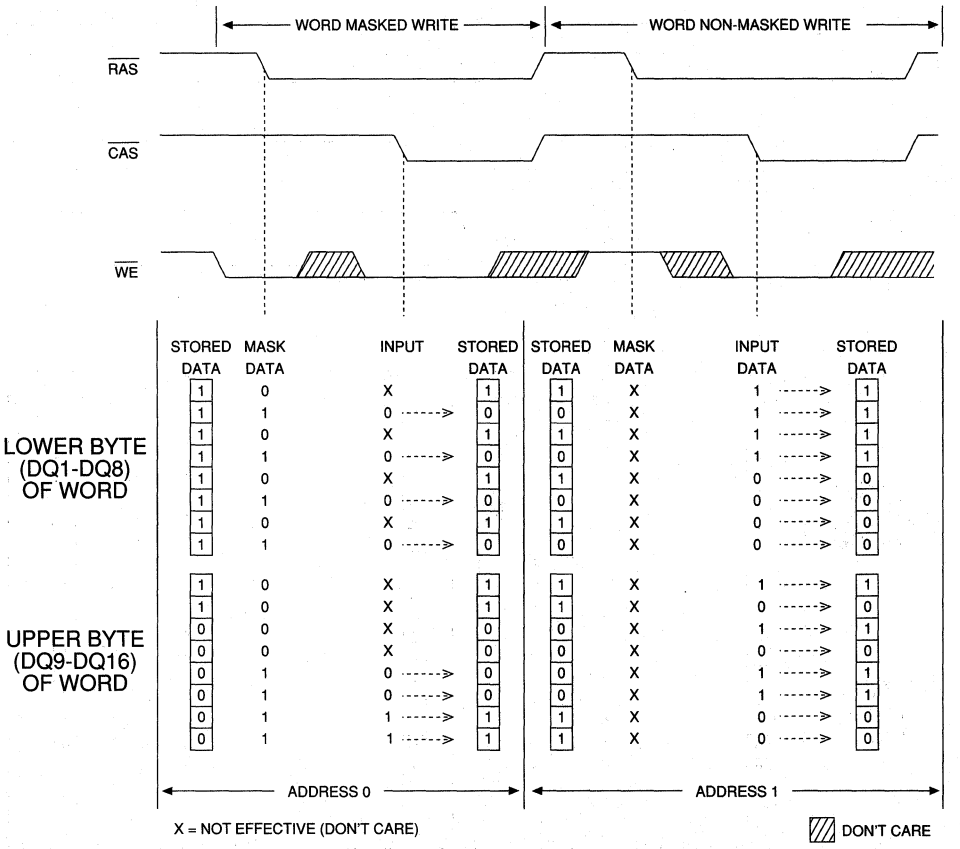


Figure 2
MT4C1665 MASKED WRITE EXAMPLE

TRUTH TABLE: MT4C1664

FUNCTION		RAS	CAS	WEL	WEH	OE	ADDRESSES tR	ADDRESSES tC	DQs	NOTES
Standby		H	H→X	X	X	X	X	X	High-Z	
READ		L	L	H	H	L	ROW	COL	Data Out	
WRITE: WORD (EARLY-WRITE)		L	L	L	L	X	ROW	COL	Data In	
WRITE: LOWER BYTE (EARLY)		L	L	L	H	X	ROW	COL	Lower Byte, Data In Upper Byte, High-Z	
WRITE: UPPER BYTE (EARLY)		L	L	H	L	X	ROW	COL	Lower Byte, High-Z Upper Byte, Data In	
READ-WRITE		L	L	H→L	H→L	L→H	ROW	COL	Data Out, Data In	1
FAST-PAGE-MODE	1st Cycle	L	H→L	H	H	L	ROW	COL	Data Out	
READ	2nd Cycle	L	H→L	H	H	L	n/a	COL	Data Out	
FAST-PAGE-MODE	1st Cycle	L	H→L	L	L	X	ROW	COL	Data In	1
EARLY-WRITE	2nd Cycle	L	H→L	L	L	X	n/a	COL	Data In	1
FAST-PAGE-MODE	1st Cycle	L	H→L	H→L	H→L	L→H	ROW	COL	Data Out, Data In	1
READ-WRITE	2nd Cycle	L	H→L	H→L	H→L	L→H	n/a	COL	Data Out, Data In	1
HIDDEN	READ	L→H→L	L	H	H	L	ROW	COL	Data Out	
REFRESH	WRITE	L→H→L	L	L	L	X	ROW	COL	Data In	1, 2
RAS-ONLY REFRESH		L	H	X	X	X	ROW	n/a	High-Z	
CAS-BEFORE-RAS REFRESH		H→L	L	X	X	X	X	X	High-Z	

NOTE: 1. These cycles may also be byte WRITE cycles (either WEL or WEH active).
2. EARLY-WRITE only.

TRUTH TABLE: MT4C1665

FUNCTION		RAS	CAS	WE	OE	ADDRESSES tR	ADDRESSES tC	DQs	NOTES
Standby		H	H→X	X	X	X	X	High-Z	
READ		L	L	H	L	ROW	COL	Data Out	
WRITE: WORD (EARLY-WRITE)		L	L	L	X	ROW	COL	Data In	1
READ-WRITE		L	L	H→L	L→H	ROW	COL	Data Out, Data In	1
FAST-PAGE-MODE	1st Cycle	L	H→L	H	L	ROW	COL	Data Out	
READ	2nd Cycle	L	H→L	H	L	n/a	COL	Data Out	
FAST-PAGE-MODE	1st Cycle	L	H→L	L	X	ROW	COL	Data In	1
EARLY-WRITE	2nd Cycle	L	H→L	L	X	n/a	COL	Data In	1
FAST-PAGE-MODE	1st Cycle	L	H→L	H→L	L→H	ROW	COL	Data Out, Data In	1
READ-WRITE	2nd Cycle	L	H→L	H→L	L→H	n/a	COL	Data Out, Data In	1
HIDDEN	READ	L→H→L	L	H	L	ROW	COL	Data Out	
REFRESH	WRITE	L→H→L	L	L	X	ROW	COL	Data In	1, 2
RAS-ONLY REFRESH		L	H	X	X	ROW	n/a	High-Z	
CAS-BEFORE-RAS REFRESH		H→L	L	X	X	X	X	High-Z	

NOTE: 1. Data In will be dependent on the mask provided. Refer to Figure 2.
2. EARLY-WRITE only.

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} ..... -1.0V to +7.0V
Operating Temperature, T_A (Ambient) ..... 0°C to +70°C
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 3, 4, 6, 7) (0°C ≤ T_A ≤ 70°C; V_{CC} = 5V ± 10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.5	V	1
Input High (Logic 1) Voltage, All Inputs	V_{IH}	2.4	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, All Inputs	V_{IL}	-1.0	0.8	V	1
INPUT LEAKAGE CURRENT Any Input 0V ≤ V_{IN} ≤ Vcc (All other pins not under test = 0V)	I_I	-2	2	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled, 0V ≤ V_{OUT} ≤ 5.5V)	I_{OZ}	-10	10	µA	
OUTPUT LEVELS Output High Voltage (I_{OUT} = -2.5mA)	V_{OH}	2.4		V	
Output Low Voltage (I_{OUT} = 2.1mA)	V_{OL}		0.4	V	

		MAX				
PARAMETER/CONDITION	SYMBOL	-7	-8	-10	UNITS	NOTES
STANDBY CURRENT: (TTL) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC1}	2	2	2	mA	
STANDBY CURRENT: (CMOS) ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} -0.2V)	I_{CC2}	1	1	1	mA	25
OPERATING CURRENT: Random READ/WRITE Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC (MIN))	I_{CC3}	120	110	100	mA	3, 4, 31
OPERATING CURRENT: FAST PAGE MODE Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: ^tPC = ^tPC (MIN); ^tCP, ^tASC = 10ns)	I_{CC4}	80	70	60	mA	3, 4, 31
REFRESH CURRENT: $\overline{RAS}$-ONLY Average power supply current ($\overline{RAS}$ Cycling, $\overline{CAS}$=V_{IH}: ^tRC = ^tRC (MIN))	I_{CC5}	120	110	100	mA	3, 31
REFRESH CURRENT: $\overline{CAS}$-BEFORE-$\overline{RAS}$ Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC (MIN))	I_{CC6}	120	110	100	mA	3, 5

CAPACITANCE

(Note: 2)

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A7	C_{I1}		5	pF	2
Input Capacitance: $\overline{RAS}$, $\overline{CAS}$,($\overline{WEL}$, $\overline{WEH}$)/ $\overline{WE}$, $\overline{OE}$	C_{I2}		7	pF	2
Input/Output Capacitance: DQ	C_{IO}		7	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13, 23) ($0°C \le T_A \le +70°C$; $V_{CC} = 5V \pm 10\%$)

AC CHARACTERISTICS		-7		-8		-10			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	^tRC	130		145		170		ns	
READ-WRITE cycle time	^tRWC	175		185		220		ns	
FAST-PAGE-MODE READ or WRITE cycle time	^tPC	45		50		60		ns	
FAST-PAGE-MODE READ-WRITE cycle time	^tPRWC	95		100		120		ns	
Access time from $\overline{RAS}$	^tRAC		70		80		100	ns	14
Access time from $\overline{CAS}$	^tCAC		25		25		30	ns	15
Output Enable time	^tOE		25		25		30	ns	
Access time from column address	^tAA		40		45		50	ns	
Access time from $\overline{CAS}$ precharge	^tCPA		45		50		55	ns	
$\overline{RAS}$ pulse width	^tRAS	70	100,000	80	100,000	100	100,000	ns	
$\overline{RAS}$ pulse width (FAST PAGE MODE)	^tRASP	70	100,000	80	100,000	100	100,000	ns	
$\overline{RAS}$ hold time	^tRSH	20		20		25		ns	
$\overline{RAS}$ precharge time	^tRP	45		45		60		ns	
$\overline{CAS}$ pulse width	^tCAS	25	100,000	25	100,000	30	100,000	ns	
$\overline{CAS}$ hold time	^tCSH	70		80		100		ns	
$\overline{CAS}$ precharge time	^tCPN	10		10		15		ns	16
$\overline{CAS}$ precharge time (FAST PAGE MODE)	^tCP	10		10		10		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	^tRCD	20	45	20	50	25	60	ns	17
$\overline{CAS}$ to $\overline{RAS}$ precharge time	^tCRP	5		5		5		ns	
Row address setup time	^tASR	0		0		0		ns	
Row address hold time	^tRAH	10		10		10		ns	
$\overline{RAS}$ to column address delay time	^tRAD	15	35	15	40	15	50	ns	18
Column address setup time	^tASC	0		0		0		ns	
Column address hold time	^tCAH	15		15		15		ns	
Column address hold time (referenced to $\overline{RAS}$)	^tAR	55		60		70		ns	
Column address to $\overline{RAS}$ lead time	^tRAL	35		40		50		ns	
Read command setup time	^tRCS	0		0		0		ns	26
Read command hold time (referenced to $\overline{CAS}$)	^tRCH	0		0		0		ns	19, 26
Read command hold time (referenced to $\overline{RAS}$)	^tRRH	0		0		0		ns	19
$\overline{CAS}$ to output in Low-Z	^tCLZ	0		0		0		ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

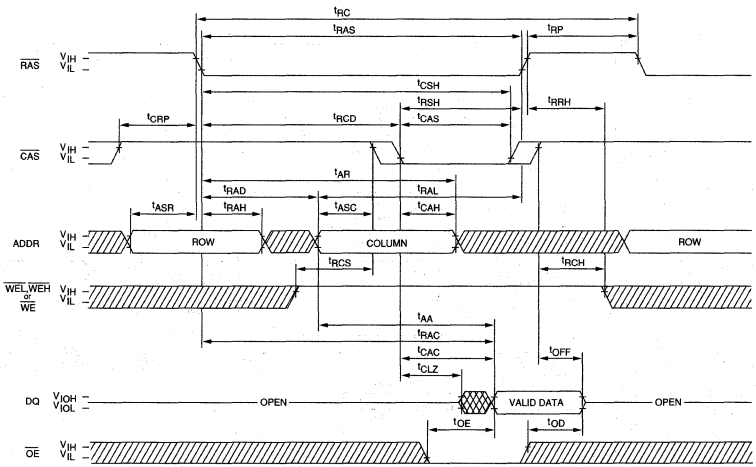
(Notes: 6, 7, 8, 9, 10, 11, 12, 13, 23) (0°C ≤ T_A ≤ +70°C; Vcc = 5V ± 10%)

AC CHARACTERISTICS		-7		-8		-10			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Output buffer turn-off delay	^tOFF	0	20	0	20	0	20	ns	20, 30
Output disable time	^tOD		15		15		20	ns	30
Write command setup time	^tWCS	0		0		0		ns	21, 26
Write command hold time	^tWCH	15		15		15		ns	26
Write command hold time (referenced to $\overline{RAS}$)	^tWCR	50		55		65		ns	26
Write command pulse width	^tWP	15		15		15		ns	26
Write command to $\overline{RAS}$ lead time	^tRWL	20		20		20		ns	26
Write command to $\overline{CAS}$ lead time	^tCWL	20		20		20		ns	26
Data-in setup time	^tDS	0		0		0		ns	22
Data-in hold time	^tDH	15		15		20		ns	22
Data-in hold time (referenced to $\overline{RAS}$)	^tDHR	50		55		65		ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	^tRWD	90		100		125		ns	21
Column address to $\overline{WE}$ delay time	^tAWD	65		70		80		ns	21
$\overline{CAS}$ to $\overline{WE}$ delay time	^tCWD	50		55		70		ns	21
Transition time (rise or fall)	^tT	3	50	3	50	3	50	ns	9, 10
Refresh period (256 cycles)	^tREF		4		4		4	ms	28
$\overline{RAS}$ to $\overline{CAS}$ precharge time	^tRPC	0		0		0		ns	
$\overline{CAS}$ setup time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tCSR	10		10		10		ns	5
$\overline{CAS}$ hold time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tCHR	15		15		15		ns	5
MASKED WRITE command to $\overline{RAS}$ setup time	^tWRS	0		0		0		ns	26, 27
MASKED WRITE command to $\overline{RAS}$ hold time	^tWRH	15		15		15		ns	26, 27
Mask data to $\overline{RAS}$ setup time	^tMS	0		0		0		ns	26
Mask data to $\overline{RAS}$ hold time	^tMH	15		15		15		ns	26
$\overline{OE}$ hold time from $\overline{WE}$ during READ-MODIFY-WRITE cycle	^tOEH	10		10		20		ns	29
$\overline{OE}$ setup prior to $\overline{RAS}$ during HIDDEN REFRESH cycle	^tORD	0		0		0		ns	

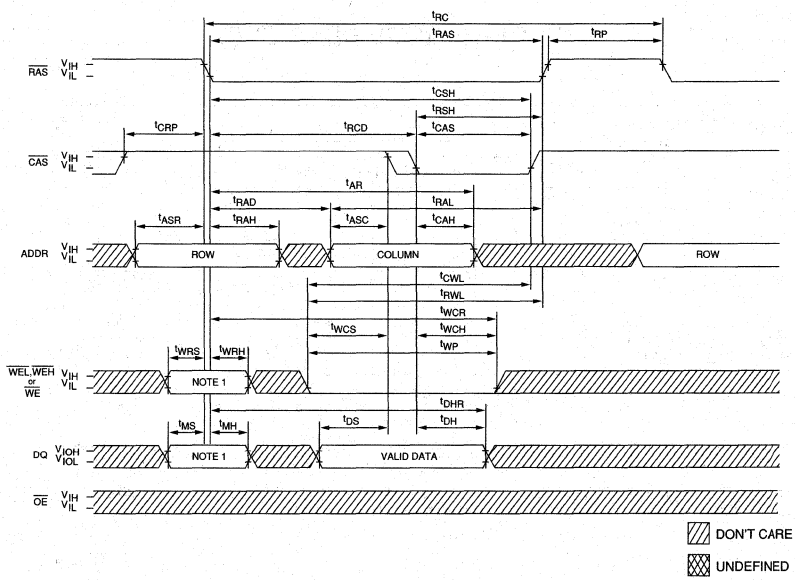
NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. Vcc = 5V ±10%, f = 1 MHz.
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \le T_A \le 70°C$) is assured.
7. An initial pause of 100µs is required after power-up followed by any eight $\overline{RAS}$ cycles before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-up should be repeated any time the ^tREF refresh requirement is exceeded.
8. AC characteristics assume ^tT = 5ns.
9. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS}$ = V_{IH}, data output is High-Z.
12. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to 1 TTL gates and 50pF.
14. Assumes that $^tRCD < ^tRCD$ (MAX). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
15. Assumes that $^tRCD \ge ^tRCD$ (MAX).
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the Q buffer, $\overline{CAS}$ must be pulsed HIGH for ^tCPN.
17. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (MAX) limit, then access time is controlled exclusively by ^tCAC.
18. Operation within the ^tRAD (MAX) limit ensures that ^tRCD (MAX) can be met. ^tRAD (MAX) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (MAX) limit, then access time is controlled exclusively by ^tAA.
19. Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
20. ^tOFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
21. ^tWCS, ^tRWD, ^tAWD and ^tCWD are restrictive operating parameters in LATE-WRITE and READ-MODIFY-WRITE cycles only. If $^tWCS \ge ^tWCS$ (MIN), the cycle is an EARLY-WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If $^tRWD \ge ^tRWD$ (MIN), $^tAWD \ge ^tAWD$ (MIN) and $^tCWD \ge ^tCWD$ (MIN), the cycle is a LATE-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions are met, the state of data out are indeterminate. $\overline{OE}$ held HIGH and $\overline{WE}$ taken LOW after $\overline{CAS}$ goes LOW results in a LATE-WRITE ($\overline{OE}$ controlled) cycle.
22. These parameters are referenced to $\overline{CAS}$ leading edge in early WRITE cycles and $\overline{WE}$ leading edge in LATE-WRITE or READ-MODIFY-WRITE cycles.
23. If $\overline{OE}$ is tied permanently LOW, LATE-WRITE or READ-MODIFY-WRITE operations are not possible.
24. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case $\overline{WE}$ = LOW and $\overline{OE}$=HIGH.
25. All other inputs at Vcc -0.2V.
26. Write command is defined as either $\overline{WEL}$ or $\overline{WEH}$ or both going LOW on the MT4C1664. Write command is defined as $\overline{WE}$ going LOW on the MT4C1665.
27. Must be held LOW to ensure MASKED WRITE is enabled and must be held HIGH to ensure MASKED WRITE is disabled.
28. The refresh period may be extended to 8ms without experiencing problems.
29. LATE-WRITE and READ-MODIFY-WRITE cycles must have both ^tOD and ^tOEH met ($\overline{OE}$ HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. The DQs will provide the previously read data if $\overline{CAS}$ remains LOW and $\overline{OE}$ is taken back LOW after ^tOEH is met. If $\overline{CAS}$ goes HIGH prior to $\overline{OE}$ going back LOW, the DQs will remain open.
30. The DQs open during READ cycles once ^tOD or ^tOFF occur. If $\overline{CAS}$ goes HIGH first, $\overline{OE}$ becomes a "don't care." If $\overline{OE}$ goes HIGH and $\overline{CAS}$ stays LOW, $\overline{OE}$ is not a "don't care;" and the DQs will provide the previously read data if $\overline{OE}$ is taken back LOW (while $\overline{CAS}$ remains LOW).
31. Column address changed once while $\overline{RAS}$ = V_{IL} and $\overline{CAS}$ = V_{IH}.

READ CYCLE

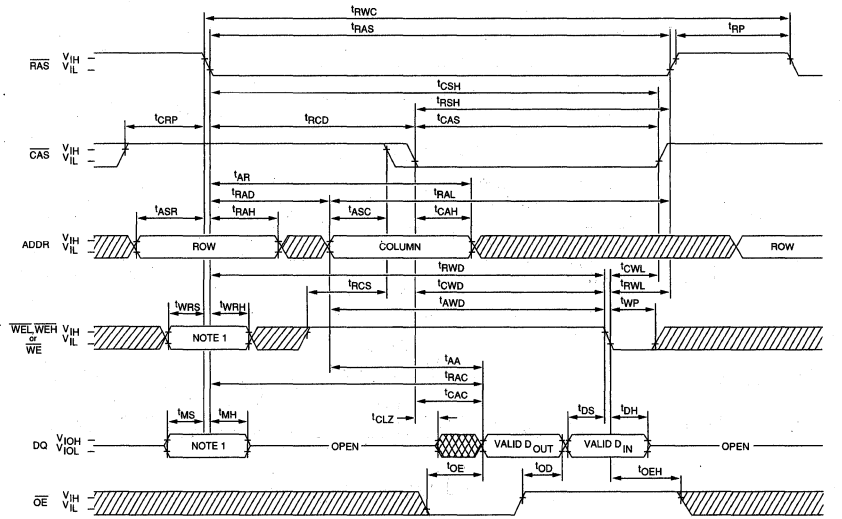


EARLY-WRITE CYCLE

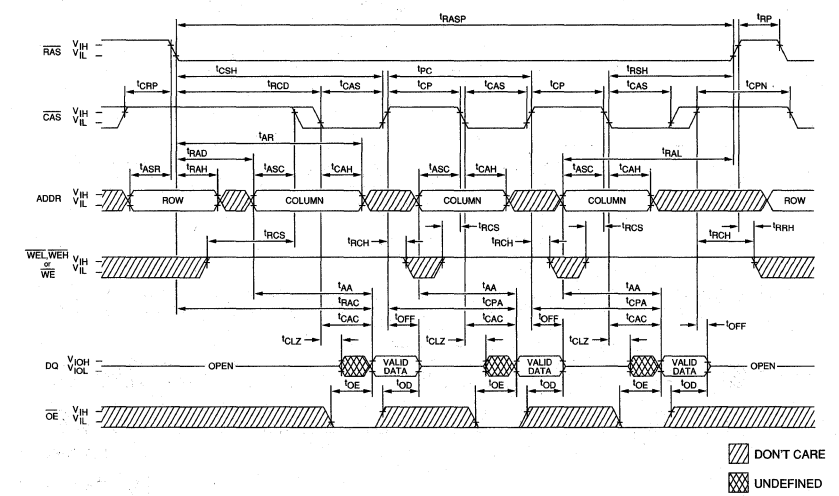


NOTE: 1. Applies to MT4C1665 only; $\overline{WEL}$, $\overline{WEH}$ and DQ inputs on MT4C1664 are "don't care" at $\overline{RAS}$ time. $\overline{WE}$ selects between normal WRITE and MASKED WRITE at $\overline{RAS}$ time. The DQ inputs are "don't care" for a normal WRITE, $\overline{WE}$ HIGH at $\overline{RAS}$ time. The DQ inputs provide the mask data at $\overline{RAS}$ time for a MASKED WRITE, $\overline{WE}$ LOW at $\overline{RAS}$ time.

READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)

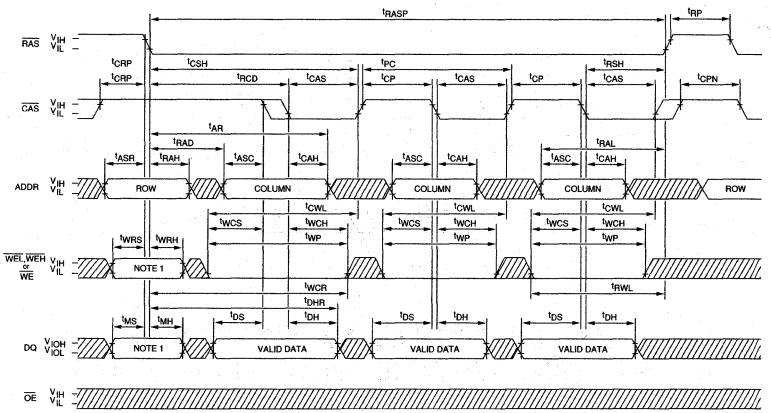


FAST-PAGE-MODE READ CYCLE

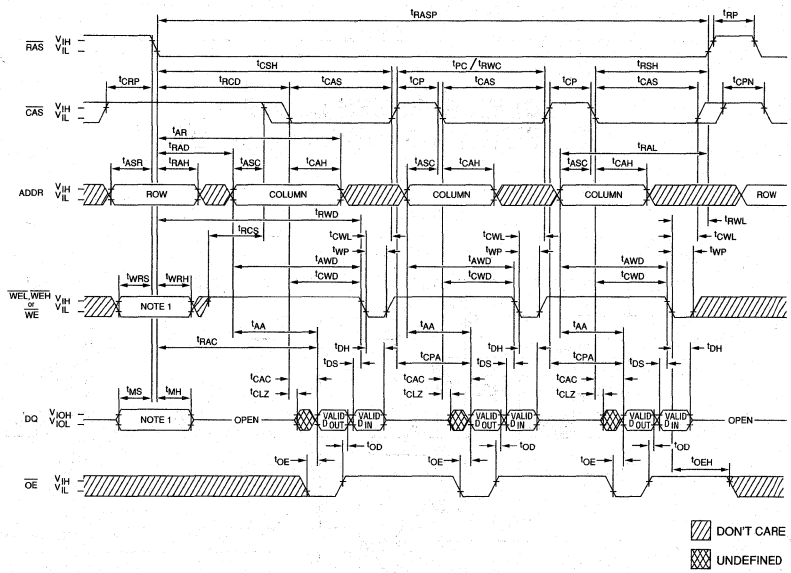


NOTE: 1. Applies to MT4C1665 only; $\overline{WEL}$, $\overline{WEH}$ and DQ inputs on MT4C1664 are "don't care" at $\overline{RAS}$ time. $\overline{WE}$ selects between normal WRITE and MASKED WRITE at $\overline{RAS}$ time. The DQ inputs are "don't care" for a normal WRITE, $\overline{WE}$ HIGH at $\overline{RAS}$ time. The DQ inputs provide the mask data at $\overline{RAS}$ time for a MASKED WRITE, $\overline{WE}$ LOW at $\overline{RAS}$ time.

FAST-PAGE-MODE EARLY-WRITE CYCLE

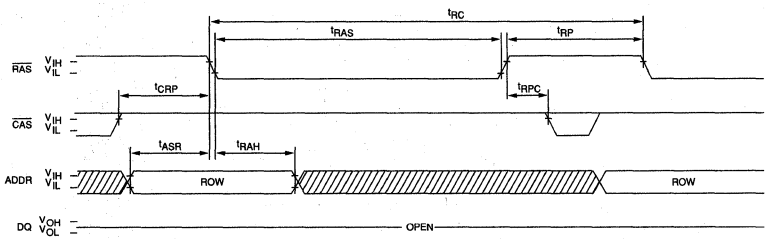


FAST-PAGE-MODE READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)

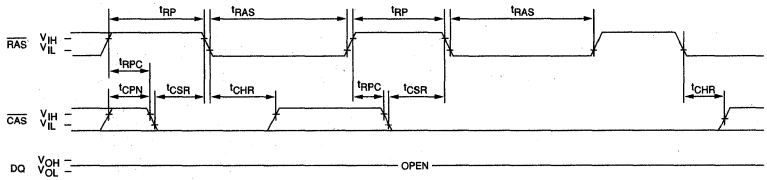


NOTE: 1. Applies to MT4C1665 only; $\overline{WEL}$, $\overline{WEH}$ and DQ inputs on MT4C1664 are "don't care" at $\overline{RAS}$ time. $\overline{WE}$ selects between normal WRITE and MASKED WRITE at $\overline{RAS}$ time. The DQ inputs are "don't care" for a normal WRITE, $\overline{WE}$ HIGH at $\overline{RAS}$ time. The DQ inputs provide the mask data at $\overline{RAS}$ time for a MASKED WRITE, $\overline{WE}$ LOW at $\overline{RAS}$ time.

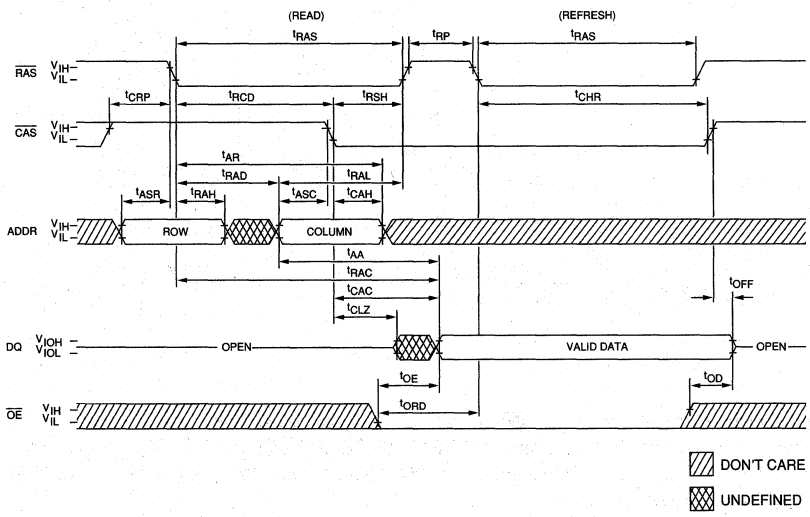
RAS-ONLY REFRESH CYCLE
(ADDR = A0-A7, OE; WEL, WEH or WE = DON'T CARE)



CAS-BEFORE-RAS REFRESH CYCLE
(A0-A7; WEL, WEH or WE, and OE = DON'T CARE)



HIDDEN REFRESH CYCLE [24]
(WEL, WEH or WE = HIGH; OE = LOW)



DRAM

64K x 16 DRAM

LOW POWER
EXTENDED REFRESH

FEATURES

- Industry standard x16 pinouts, timing, functions and packages
- High-performance, CMOS silicon-gate process
- Single +5V ±10% power supply
- All device pins are fully TTL compatible
- Refresh modes: RAS-ONLY, CAS-BEFORE-RAS (CBR), HIDDEN and BATTERY BACKUP (BBU)
- Optional FAST PAGE MODE access cycle
- BYTE WRITE access cycle (MT4C1664 L only)
- NONPERSISTENT MASKED WRITE access cycle (MT4C1665 L only)
- Reduced CMOS STANDBY CURRENT
- Low power, 1mW standby; 225mW active, typical
- Extended refresh: 256 cycles over 32ms (125µs cycles)

OPTIONS — MARKING

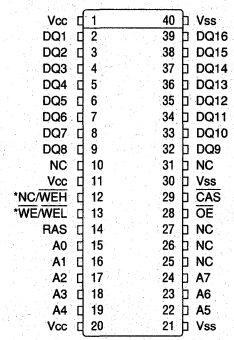
- Timing
  - 70ns access — -7
  - 80ns access — -8
  - 100ns access — -10
- Write Enable
  - Byte or Word — MT4C1664 L
  - Word only — MT4C1665 L
- Mask Enable
  - Not available — MT4C1664 L
  - Always available — MT4C1665 L
- Packages
  - Plastic SOJ (400mil) — DJ
  - Plastic TSOP (400mil) — TG
  - Plastic ZIP (475mil) — Z

NOTE: Available in die form Please consult factory for die data sheets.

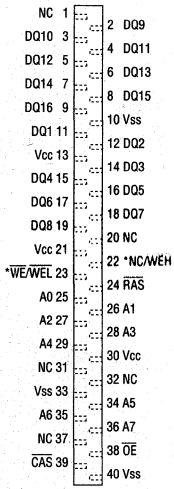
- Part Number Example: MT4C1664DJ-7 L

PIN ASSIGNMENT (Top View)

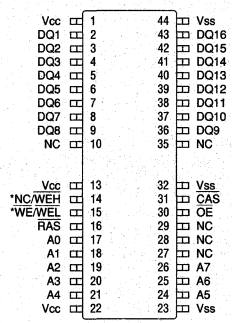
40-Pin SOJ (Q-6)



40-Pin Zip (O-4)



40-Pin TSOP (R-5)



*MT4C1665 L/MT4C1664 L

GENERAL DESCRIPTION

The MT4C1664/5 L are randomly accessed solid-state memories containing 1,048,576 bits organized in a x16 configuration. The MT4C1664 L has both BYTE and WORD WRITE access cycles while the MT4C1665 L has only WORD WRITE access cycles.

The MT4C1664 L functions in a similar manner to the MT4C1665 L except that replacing $\overline{WE}$ with $\overline{WEL}$ and $\overline{WEH}$ allows for BYTE WRITE access cycles. $\overline{WEL}$ and $\overline{WEH}$ function in an identical manner to $\overline{WE}$: either $\overline{WEL}$ or $\overline{WEH}$ will generate an internal $\overline{WE}$ through an AND gate (inverted NOR gate).

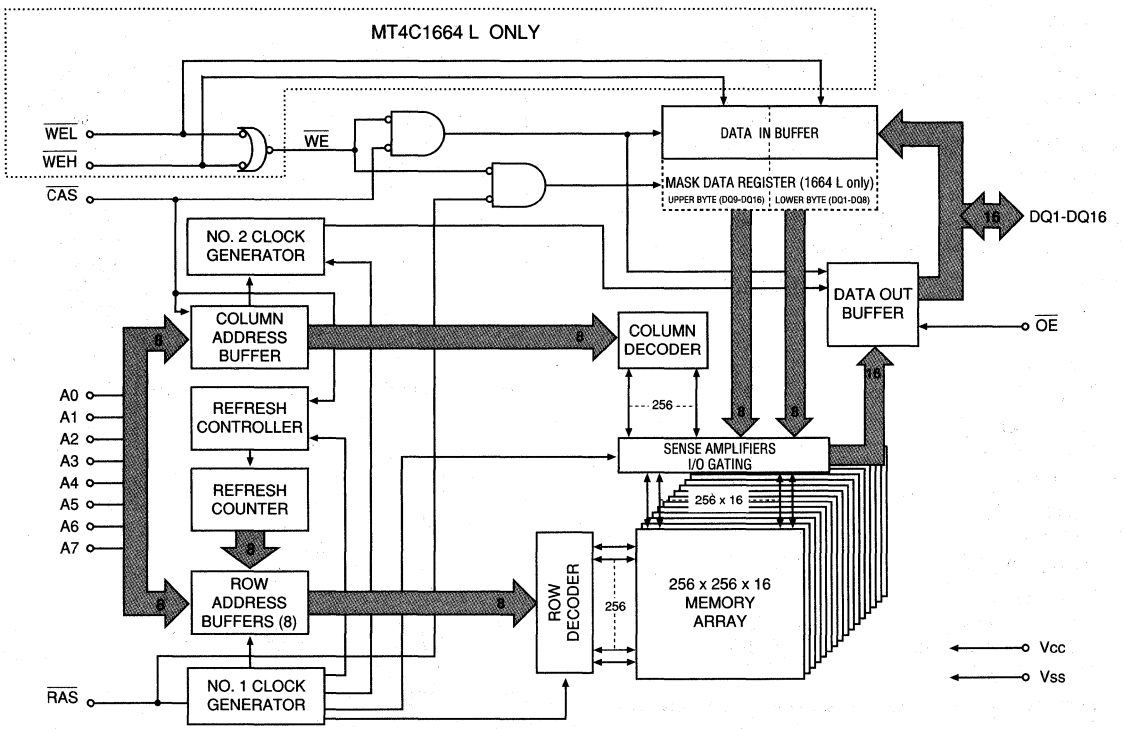
The MT4C1664 L "$\overline{WE}$" function and timing are determined by the first BYTE WRITE ($\overline{WEL}$ or $\overline{WEH}$) to transition LOW and the last to transition back HIGH. Use of only one of the two results in a BYTE WRITE cycle: $\overline{WEL}$ transitioning LOW selects a WRITE cycle for the lower byte (DQ1-DQ8) or $\overline{WEH}$ transitioning LOW selects a WRITE cycle for the upper byte (DQ9-DQ16).

The MT4C1665 L has NONPERSISTENT MASKED WRITE capability.

The extended refresh of the MT4C1664/5 L provides a factor-of-eight reduction of refresh intervals required, as compared to a standard 64K x 16 DRAM (MT4C1664/5).

The MT4C1664/5 L offers lower operating power as well as reduced refresh and standby currents. The MT4C1664/5 L are the same devices as the MT4C1664/5, but with low power capabilites.

FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTIONS

SOJ PIN NUMBERS	ZIP PIN NUMBERS	TSOP PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
14	24	16	$\overline{RAS}$	Input	ROW Address Strobe: $\overline{RAS}$ is used to clock-in the 8 row address bits and strobe the $\overline{WEL}$, $\overline{WEH}$ and DQ inputs for the MASKED WRITE function.
29	39	31	$\overline{CAS}$	Input	Column Address Strobe: $\overline{CAS}$ is used to clock-in the 8 column address bits, enable the DRAM output buffers, and strobe the data inputs on WRITE cycles.
28	38	30	$\overline{OE}$	Input	Output Enable: $\overline{OE}$ enables the output buffers when taken LOW during a READ access cycle. $\overline{RAS}$ and $\overline{CAS}$ must be LOW and $\overline{WEL}$ and $\overline{WEH}$ must be HIGH before $\overline{OE}$ will control the output buffers. Otherwise the output buffers are in a High-Z state.
13	23	15	$\overline{WE}$/$\overline{WEL}$*	Input	WRITE Enable Lower Byte: $\overline{WEL}$ on MT4C1664 L is $\overline{WE}$ control for the DQ1 through DQ8 inputs. $\overline{WE}$ on MT4C1665 L controls DQ1 through DQ16 inputs. If ($\overline{WEL}$ or $\overline{WEH}$)/$\overline{WE}$ is LOW, the access is a WRITE cycle. The DQ outputs for the byte not being written will remain in a High-Z state (byte WRITE cycle only).
12	22	14	NC/$\overline{WEH}$*	Input	Write Enable Upper Byte: $\overline{WEH}$ on MT4C1664 L is $\overline{WE}$ control for the DQ9 through DQ16 inputs. If ($\overline{WEL}$ or $\overline{WEH}$)/$\overline{WE}$ is LOW, the access is a WRITE cycle. This pin is a no connect on the MT4C1665 L as it has only WORD WRITE access cycles.
15-19, 22-24	25-29, 34-36	17-21, 24-26	A0-A7	Input	Address Inputs: These inputs are multiplexed and clocked by $\overline{RAS}$ and $\overline{CAS}$ to select one 16-bit word out of the 64K available words.
2-9, 32-39	11, 12, 14-17, 2, 18, 19, 3-9	2-9, 36-43	DQ1-DQ16	Input/ Output	Data I/O: For WRITE cycles, DQ1-DQ16 act as inputs to the addressed DRAM location. BYTE WRITEs can be performed by using $\overline{WEL}$ or $\overline{WEH}$ to select the byte to be written. For READ access cycles, DQ1-DQ16 act as outputs for the addressed DRAM ocation. All 16 I/Os are active for READ cycles (there is no BYTE READ cycle).
10, 25, 26, 27, 31	1, 20, 31, 32, 37	10, 27-29, 35	NC	-	No Connect: These pins should be either left unconnected or tied to ground.
1, 11, 20	13, 21, 30	1, 13, 22	V_{CC}	Supply	Power Supply: +5V ± 10%
21, 30, 40	10, 33, 40	23, 32, 44	V_{SS}	Supply	Ground

NOTE: *MT4C1665 L/MT4C1664 L

FUNCTIONAL DESCRIPTION

Each bit is uniquely addressed through the 16 address-bits during READ or WRITE cycles. These are entered 8 bits (A0-A7) at a time. $\overline{RAS}$ is used to latch the first 8 bits and $\overline{CAS}$ the latter 8 bits.

READ or WRITE cycles on the MT4C1665 L are selected with the $\overline{WE}$ input while either $\overline{WEL}$ or $\overline{WEH}$ perform the "$\overline{WE}$" on the MT4C1664 L. The MT4C1664 L "$\overline{WE}$" function is determined by the first BYTE WRITE ($\overline{WEL}$ or $\overline{WEH}$) to transition LOW and the last one to transition back HIGH.

A logic HIGH on $\overline{WE}$ dictates READ mode while a logic LOW on $\overline{WE}$ dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. Taking $\overline{WE}$ LOW will initiate a WRITE cycle, selecting DQ1 through DQ16. If $\overline{WE}$ goes LOW prior to $\overline{CAS}$ going LOW, the output pin(s) remain open (High-Z) until the next $\overline{CAS}$ cycle. If $\overline{WE}$ goes LOW after $\overline{CAS}$ goes LOW and data reaches the output pins, data out (Q) is activated and retains the selected cell data as long as $\overline{CAS}$ and $\overline{OE}$ remain LOW (regardless of $\overline{WE}$ or $\overline{RAS}$). This late $\overline{WE}$ pulse results in a READ-WRITE cycle.

The 16 data inputs and 16 data outputs are routed through 16 pins using common I/O, and pin direction is controlled by $\overline{OE}$, $\overline{WEL}$ and $\overline{WEH}$ (MT4C1664 L) or $\overline{WE}$ (MT4C1665 L).

FAST PAGE MODE operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row address (A0-A7) defined page boundary. The FAST PAGE MODE cycle is always initiated with a row address strobed-in by $\overline{RAS}$ followed by a column address strobed-in by $\overline{CAS}$. $\overline{CAS}$ may be toggled-in by holding $\overline{RAS}$ LOW and strobing-in different column addresses, thus executing faster memory cycles. Returning $\overline{RAS}$ HIGH terminates the FAST PAGE MODE operation.

Returning $\overline{RAS}$ and $\overline{CAS}$ HIGH terminates a memory cycle and decreases chip current to a reduced standby level. The chip is also preconditioned for the next cycle during the $\overline{RAS}$ high time. Memory cell data is retained in its correct state by maintaining power and executing any $\overline{RAS}$ cycle (READ, WRITE, $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$, or HIDDEN refresh) so that all 256 combinations of $\overline{RAS}$ addresses (A0-A7) are executed at least every 32ms, regardless of sequence. The $\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh cycle will also invoke the refresh counter and controller for row address control.

BATTERY BACKUP MODE (BBU) is a CBR refresh performed at the extended refresh rate with CMOS input levels. This mode provides a very low current, data retention cycle. $\overline{RAS}$ or $\overline{CAS}$ time refers to the time at which $\overline{RAS}$ or $\overline{CAS}$ transition from HIGH to LOW).

BYTE WRITE DESCRIPTION (MT4C1664 L ONLY)

The BYTE WRITE mode is determined by the use of $\overline{WEL}$ and $\overline{WEH}$. Enabling $\overline{WEL}$ will select a lower BYTE WRITE cycle (DQ1-DQ8) while enabling $\overline{WEH}$ will select an upper BYTE WRITE (DQ9-DQ16). Enabling both $\overline{WEL}$ and $\overline{WEH}$ selects a WORD WRITE cycle.

The MT4C1664 L may be viewed as two 64K x 8 DRAMs which have common input controls, with the exception of the WE input. Figure 1 illustrates the MT4C1664 L BYTE and WORD WRITE cycles.

MASKED WRITE DESCRIPTION (MT4C1665 L ONLY)

Every WRITE access cycle may be a MASKED WRITE, depending on the state of $\overline{WE}$ at $\overline{RAS}$ time. A MASKED WRITE is selected when mask data is supplied on the DQ pins and $\overline{WE}$ is LOW at $\overline{RAS}$ time. The MT4C1665 L is only word selectable when $\overline{WE}$ is LOW at $\overline{RAS}$ time (the MT4C1664 L does not have a MASKED WRITE cycle function).

The data (mask data) present on the DQ1-DQ16 inputs at $\overline{RAS}$ time will be written to an internal bit mask data register and will then act as an individual write enable for each of the corresponding DQ inputs. If a LOW (logic "0") is written to a mask data register bit, the input port for that bit is disabled during the subsequent WRITE operation and no new data will be written to that DRAM cell location. A HIGH (logic "1") on a mask data register bit enables the input port and allows normal WRITE operations to proceed. At $\overline{CAS}$ time, the bits present on the DQ1-DQ16 inputs will be written to the DRAM (if the mask data bit was HIGH) or ignored (if the mask data bit was LOW).

New mask data must be supplied each time a MASKED WRITE cycle is initiated, even if the previous cycle's mask was the same mask.

Figure 2 illustrates the MT4C1665 L MASKED WRITE operation (Note: $\overline{RAS}$ or $\overline{CAS}$ time refers to the time at which $\overline{RAS}$ or $\overline{CAS}$ transition from HIGH to LOW).

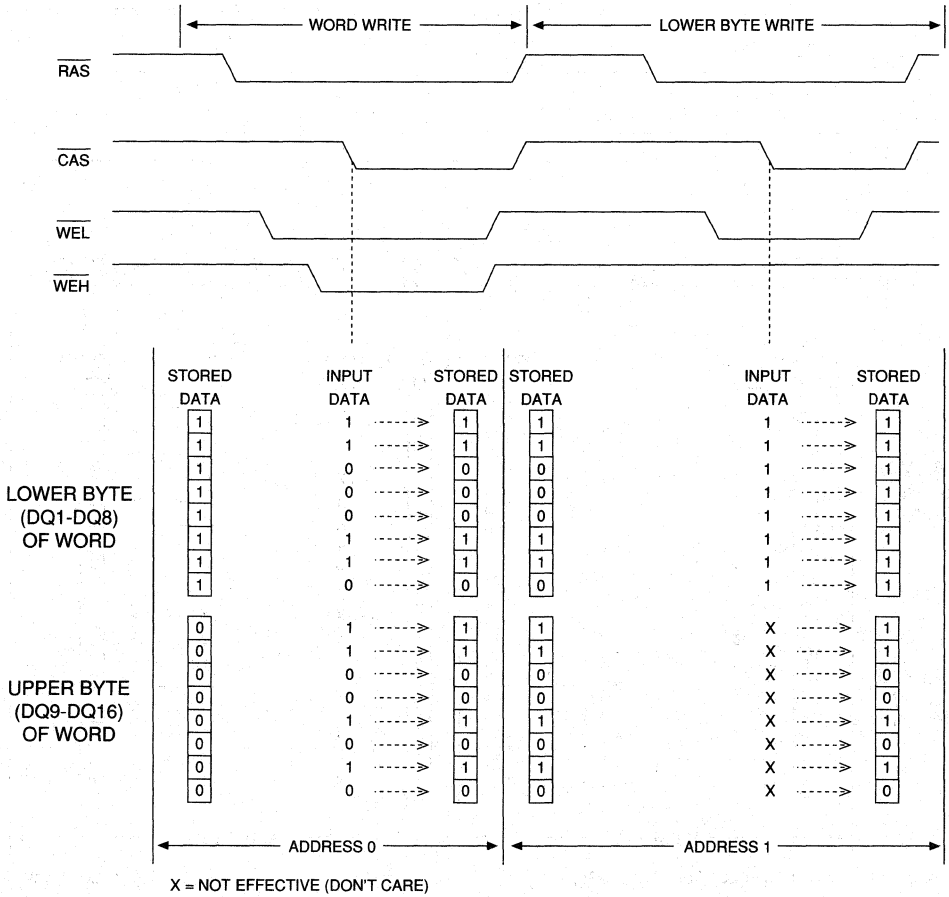


Figure 1
MT4C1664 L WORD AND BYTE WRITE EXAMPLE

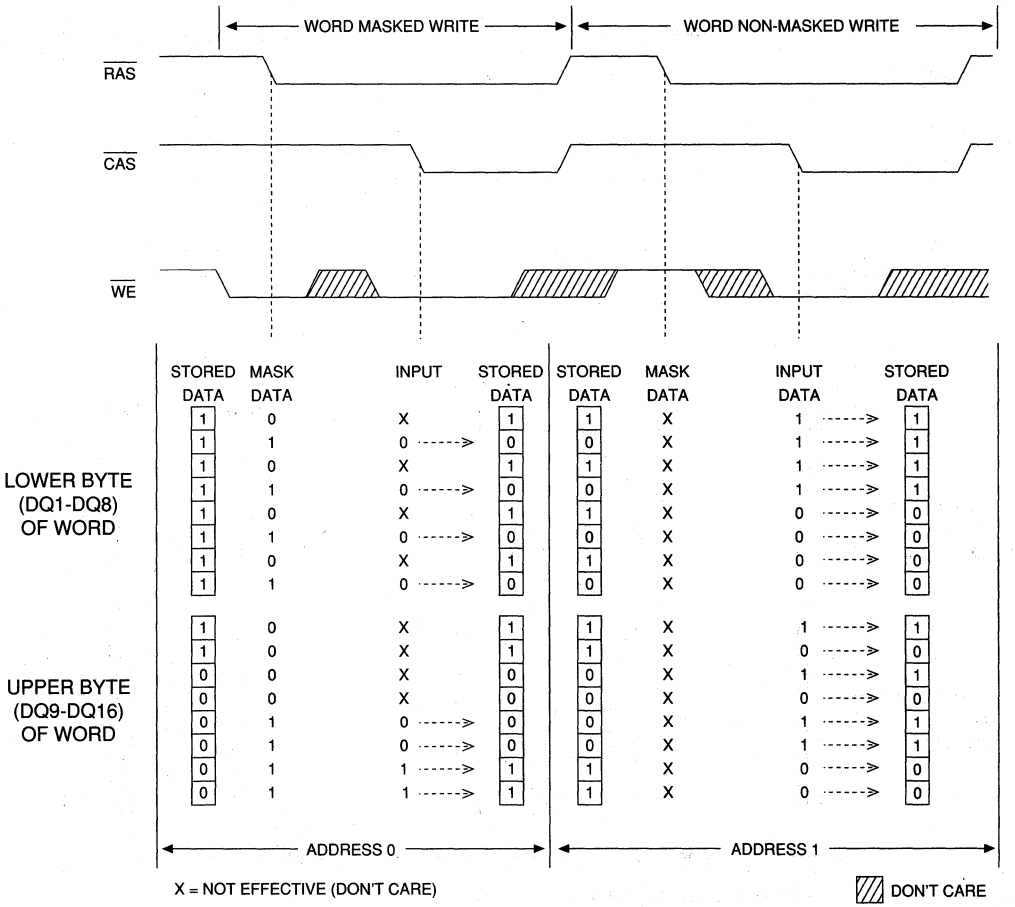


Figure 2
MT4C1665 L MASKED WRITE EXAMPLE

TRUTH TABLE: MT4C1664 L

FUNCTION		RAS	CAS	WEL	WEH	OE	ADDRESSES tR	ADDRESSES tC	DQs	NOTES
Standby		H	H→X	X	X	X	X	X	High-Z	
READ		L	L	H	H	L	ROW	COL	Data Out	
WRITE: WORD (EARLY-WRITE)		L	L	L	L	X	ROW	COL	Data In	
WRITE: LOWER BYTE (EARLY)		L	L	L	H	X	ROW	COL	Lower Byte, Data In Upper Byte, High-Z	
WRITE: UPPER BYTE (EARLY)		L	L	H	L	X	ROW	COL	Lower Byte, High-Z Upper Byte, Data In	
READ-WRITE		L	L	H→L	H→L	L→H	ROW	COL	Data Out, Data In	1
FAST-PAGE-MODE	1st Cycle	L	H→L	H	H	L	ROW	COL	Data Out	
READ	2nd Cycle	L	H→L	H	H	L	n/a	COL	Data Out	
FAST-PAGE-MODE	1st Cycle	L	H→L	L	L	X	ROW	COL	Data In	1
EARLY-WRITE	2nd Cycle	L	H→L	L	L	X	n/a	COL	Data In	1
FAST-PAGE-MODE	1st Cycle	L	H→L	H→L	H→L	L→H	ROW	COL	Data Out, Data In	1
READ-WRITE	2nd Cycle	L	H→L	H→L	H→L	L→H	n/a	COL	Data Out, Data In	1
HIDDEN	READ	L→H→L	L	H	H	L	ROW	COL	Data Out	
REFRESH	WRITE	L→H→L	L	L	L	X	ROW	COL	Data In	1, 2
RAS-ONLY REFRESH		L	H	X	X	X	ROW	n/a	High-Z	
CAS-BEFORE-RAS REFRESH		H→L	L	X	X	X	X	X	High-Z	
BATTERY BACKUP REFRESH		H→L	L	X	X	X	X	X	High-Z	

NOTE: 1. These cycles may also be BYTE WRITE cycles (either WEL or WEH active).
2. EARLY-WRITE only.

TRUTH TABLE: MT4C1665 L

FUNCTION		RAS	CAS	WE	OE	ADDRESSES tR	ADDRESSES tC	DQs	NOTES
Standby		H	H→X	X	X	X	X	High-Z	
READ		L	L	H	L	ROW	COL	Data Out	
WRITE: WORD (EARLY-WRITE)		L	L	L	X	ROW	COL	Data In	1
READ-WRITE		L	L	H→L	L→H	ROW	COL	Data Out, Data In	1
FAST-PAGE-MODE	1st Cycle	L	H→L	H	L	ROW	COL	Data Out	
READ	2nd Cycle	L	H→L	H	L	n/a	COL	Data Out	
FAST-PAGE-MODE	1st Cycle	L	H→L	L	X	ROW	COL	Data In	1
EARLY-WRITE	2nd Cycle	L	H→L	L	X	n/a	COL	Data In	1
FAST-PAGE-MODE	1st Cycle	L	H→L	H→L	L→H	ROW	COL	Data Out, Data In	1
READ-WRITE	2nd Cycle	L	H→L	H→L	L→H	n/a	COL	Data Out, Data In	1
HIDDEN	READ	L→H→L	L	H	L	ROW	COL	Data Out	
REFRESH	WRITE	L→H→L	L	L	X	ROW	COL	Data In	1, 2
RAS-ONLY REFRESH		L	H	X	X	ROW	n/a	High-Z	
CAS-BEFORE-RAS REFRESH		H→L	L	X	X	X	X	High-Z	
BATTERY BACKUP REFRESH		H→L	L	X	X	X	X	High-Z	

NOTE: 1. Data-in will be dependent on the mask provided. Refer to Figure 2.
2. EARLY-WRITE only.

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} ..... -1V to +7V
Operating Temperature, T_A (Ambient) ..... 0°C to +70°C
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 3, 4, 6, 7) (0°C ≤ T_A ≤ 70°C; V_{CC} = 5V ±10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.5	V	1
Input High (Logic 1) Voltage, All Inputs	V_{IH}	2.4	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, All Inputs	V_{IL}	-1.0	0.8	V	1
INPUT LEAKAGE CURRENT Any Input 0V ≤ V_{IN} ≤ V_{CC} (All other pins not under test = 0V)	I_I	-2	2	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled; 0V ≤ V_{OUT} ≤ 5.5V)	I_{OZ}	-10	10	µA	
OUTPUT LEVELS Output High Voltage (I_{OUT} = -2.5mA)	V_{OH}	2.4		V	
Output Low Voltage (I_{OUT} = 2.1mA)	V_{OL}		0.4	V	

		MAX				
PARAMETER/CONDITION	SYMBOL	-7	-8	-10	UNITS	NOTES
STANDBY CURRENT: (TTL) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC1}	2	2	2	mA	
STANDBY CURRENT: (CMOS) ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} -0.2V)	I_{CC2}	300	300	300	µA	25
OPERATING CURRENT: Random READ/WRITE Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC (MIN))	I_{CC3}	120	110	100	mA	3, 4, 32
OPERATING CURRENT: FAST PAGE MODE Average power supply current ($\overline{RAS}$ = V_{IL}; $\overline{CAS}$, Address Cycling: ^tPC = ^tPC (MIN); ^tCP, ^tASC = 10ns)	I_{CC4}	80	70	60	mA	3, 4, 32
REFRESH CURRENT: $\overline{RAS}$-ONLY Average power supply current ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}: ^tRC = ^tRC (MIN))	I_{CC5}	120	110	100	mA	3, 32
REFRESH CURRENT: $\overline{CAS}$-BEFORE-$\overline{RAS}$ Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC (MIN))	I_{CC6}	120	110	100	mA	3, 5
REFRESH CURRENT: BATTERY BACKUP (BBU) Average power supply current with $\overline{CAS}$ = 0.2V or CBR; $\overline{RAS}$ = minimum ^tRAS to 1µs; A0-A7, $\overline{WE}$, $\overline{OE}$ and DQs = V_{CC} -0.2V or 0.2V (DQs may float); ^tRC = 125µs	I_{CC7}	400	400	400	µA	3, 31

CAPACITANCE

(Note: 2)

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A7	C_{I1}		5	pF	2
Input Capacitance: $\overline{RAS}$, $\overline{CAS}$,($\overline{WEL}$, $\overline{WEH}$)/ $\overline{WE}$, $\overline{OE}$	C_{I2}		7	pF	2
Input/Output Capacitance: DQ	C_{IO}		7	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13, 23) (0°C ≤ T_A ≤ +70°C; V_{CC} = 5V ±10%)

AC CHARACTERISTICS		-7		-8		-10			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	^tRC	130		145		170		ns	
READ-WRITE cycle time	^tRWC	175		185		220		ns	
FAST-PAGE-MODE READ or WRITE cycle time	^tPC	45		50		60		ns	
FAST-PAGE-MODE READ-WRITE cycle time	^tPRWC	95		100		120		ns	
Access time from $\overline{RAS}$	^tRAC		70		80		100	ns	14
Access time from $\overline{CAS}$	^tCAC		25		25		30	ns	15
Output Enable time	^tOE		25		25		30	ns	
Access time from column address	^tAA		40		45		50	ns	
Access time from $\overline{CAS}$ precharge	^tCPA		45		50		55	ns	
$\overline{RAS}$ pulse width	^tRAS	70	100,000	80	100,000	100	100,000	ns	
$\overline{RAS}$ pulse width (FAST PAGE MODE)	^tRASP	70	100,000	80	100,000	100	100,000	ns	
$\overline{RAS}$ hold time	^tRSH	20		20		25		ns	
$\overline{RAS}$ precharge time	^tRP	45		45		60		ns	
$\overline{CAS}$ pulse width	^tCAS	25	100,000	25	100,000	30	100,000	ns	
$\overline{CAS}$ hold time	^tCSH	70		80		100		ns	
$\overline{CAS}$ precharge time	^tCPN	10		10		15		ns	16
$\overline{CAS}$ precharge time (FAST PAGE MODE)	^tCP	10		10		10		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	^tRCD	20	45	20	50	25	60	ns	17
$\overline{CAS}$ to $\overline{RAS}$ precharge time	^tCRP	5		5		5		ns	
Row address setup time	^tASR	0		0		0		ns	
Row address hold time	^tRAH	10		10		10		ns	
$\overline{RAS}$ to column address delay time	^tRAD	15	35	15	40	15	50	ns	18
Column address setup time	^tASC	0		0		0		ns	
Column address hold time	^tCAH	15		15		15		ns	
Column address hold time (referenced to $\overline{RAS}$)	^tAR	55		60		70		ns	
Column address to $\overline{RAS}$ lead time	^tRAL	35		40		50		ns	
Read command setup time	^tRCS	0		0		0		ns	26
Read command hold time (referenced to $\overline{CAS}$)	^tRCH	0		0		0		ns	19, 26
Read command hold time (referenced to $\overline{RAS}$)	^tRRH	0		0		0		ns	19
$\overline{CAS}$ to output in Low-Z	^tCLZ	0		0		0		ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

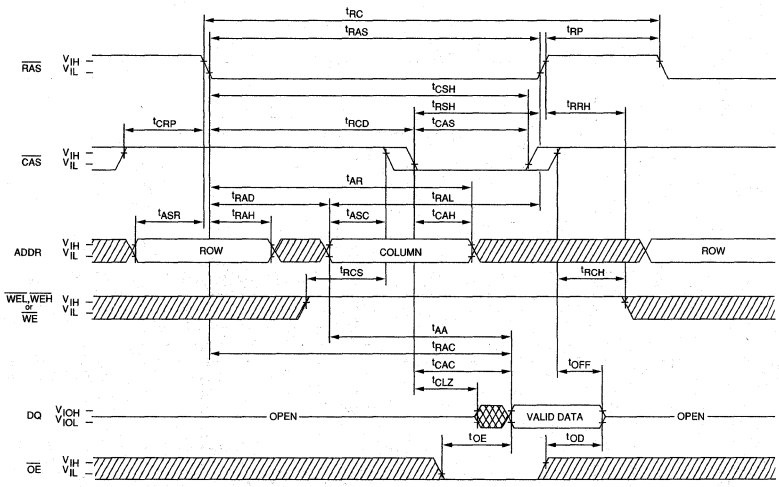
(Notes: 6, 7, 8, 9, 10, 11, 12, 13, 23) (0°C ≤ T_A ≤ +70°C; Vcc = 5V ±10%)

AC CHARACTERISTICS		-7		-8		-10			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Output buffer turn-off delay	^tOFF	0	20	0	20	0	20	ns	20, 30
Output disable time	^tOD		15		15		20	ns	30
Write command setup time	^tWCS	0		0		0		ns	21, 26
Write command hold time	^tWCH	15		15		15		ns	26
Write command hold time (referenced to $\overline{RAS}$)	^tWCR	50		55		65		ns	26
Write command pulse width	^tWP	15		15		15		ns	26
Write command to $\overline{RAS}$ lead time	^tRWL	20		20		20		ns	26
Write command to $\overline{CAS}$ lead time	^tCWL	20		20		20		ns	26
Data-in setup time	^tDS	0		0		0		ns	22
Data-in hold time	^tDH	15		15		20		ns	22
Data-in hold time (referenced to $\overline{RAS}$)	^tDHR	50		55		65		ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	^tRWD	90		100		125		ns	21
Column address to $\overline{WE}$ delay time	^tAWD	65		70		80		ns	21
$\overline{CAS}$ to $\overline{WE}$ delay time	^tCWD	50		55		70		ns	21
Transition time (rise or fall)	^tT	3	50	3	50	3	50	ns	9, 10
Refresh period (256 cycles)	^tREF		32		32		32	ms	28
$\overline{RAS}$ to $\overline{CAS}$ precharge time	^tRPC	0		0		0		ns	
$\overline{CAS}$ setup time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tCSR	10		10		10		ns	5
$\overline{CAS}$ hold time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tCHR	15		15		15		ns	5
MASKED WRITE command to $\overline{RAS}$ setup time	^tWRS	0		0		0		ns	26, 27
MASKED WRITE command to $\overline{RAS}$ hold time	^tWRH	15		15		15		ns	26, 27
Mask data to $\overline{RAS}$ setup time	^tMS	0		0		0		ns	26
Mask data to $\overline{RAS}$ hold time	^tMH	15		15		15		ns	26
$\overline{OE}$ hold time from $\overline{WE}$ during READ-MODIFY-WRITE cycle	^tOEH	10		10		20		ns	29
$\overline{OE}$ setup prior to $\overline{RAS}$ during HIDDEN REFRESH cycle	^tORD	0		0		0		ns	

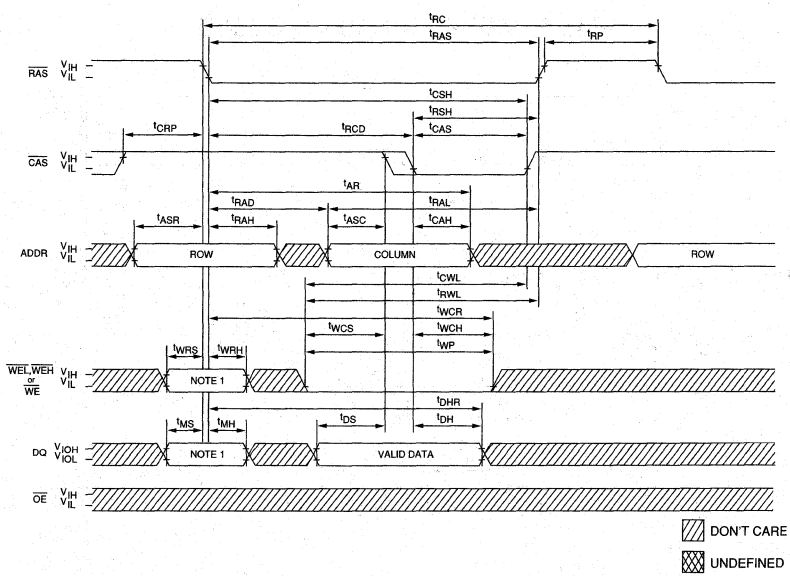
NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. V_{CC} = 5V ±10%, f = 1 MHz.
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is assured.
7. An initial pause of 100µs is required after power-up followed by any eight $\overline{RAS}$ cycles before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-up should be repeated any time the ^tREF refresh requirement is exceeded.
8. AC characteristics assume ^tT = 5ns.
9. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS}$ = V_{IH}, data output is high impedance.
12. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to 1 TTL gates and 50pF.
14. Assumes that $^tRCD < ^tRCD$ (MAX). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
15. Assumes that $^tRCD \geq ^tRCD$ (MAX).
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, data out (Q) will be maintained from the previous cycle. To initiate a new cycle and clear the Q buffer, $\overline{CAS}$ must be pulsed HIGH for ^tCPN.
17. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (MAX) limit, then access time is controlled exclusively by ^tCAC.
18. Operation within the ^tRAD (MAX) limit ensures that ^tRCD (MAX) can be met. ^tRAD (MAX) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (MAX) limit, then access time is controlled exclusively by ^tAA.
19. Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
20. ^tOFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
21. ^tWCS, ^tRWD, ^tAWD and ^tCWD are restrictive operating parameters in LATE-WRITE and READ-MODIFY-WRITE cycles only. If $^tWCS \geq ^tWCS$ (MIN), the cycle is an EARLY-WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If $^tRWD \geq ^tRWD$ (MIN), $^tAWD \geq ^tAWD$ (MIN) and $^tCWD \geq ^tCWD$ (MIN), the cycle is a LATE-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions are met, the state of data out is indeterminate. $\overline{OE}$ held HIGH and $\overline{WE}$ taken LOW after $\overline{CAS}$ goes LOW results in a LATE-WRITE ($\overline{OE}$ controlled) cycle.
22. These parameters are referenced to $\overline{CAS}$ leading edge in early WRITE cycles and $\overline{WE}$ leading edge in LATE-WRITE or READ-MODIFY-WRITE cycles.
23. If $\overline{OE}$ is tied permanently LOW, LATE-WRITE or READ-MODIFY-WRITE operations are not possible.
24. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW and $\overline{OE}$ = HIGH.
25. All other inputs at V_{CC} -0.2V.
26. WRITE command is defined as either $\overline{WEL}$ or $\overline{WEH}$ or both going LOW on the MT4C1664 L. WRITE command is defined as $\overline{WE}$ going LOW on the MT4C1665 L.
27. Must be held LOW to ensure MASKED WRITE is enabled and must be held HIGH to ensure MASKED WRITE is disabled.
28. The refresh period may be extended to 8ms without causing problems.
29. LATE-WRITE and READ-MODIFY-WRITE cycles must have both ^tOD and ^tOEH met ($\overline{OE}$ HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. The DQs will provide the previously read data if $\overline{CAS}$ remains LOW and $\overline{OE}$ is taken back LOW after ^tOEH is met. If $\overline{CAS}$ goes HIGH prior to $\overline{OE}$ going back LOW, the DQs will remain open.
30. The DQs open during READ cycles once ^tOD or ^tOFF occur. If $\overline{CAS}$ goes HIGH first, $\overline{OE}$ becomes a "don't care." If $\overline{OE}$ goes HIGH and $\overline{CAS}$ stays LOW, $\overline{OE}$ is not a "don't care;" and the DQs will provide the previously read data if $\overline{OE}$ is taken back LOW (while $\overline{CAS}$ remains LOW).
31. BBU current does not significantly change when ^tRAS is reduced from its maximum specification during BBU cycle.
32. Column address changed once while $\overline{RAS}$ = V_{IL} and $\overline{CAS}$ = V_{IH}

READ CYCLE

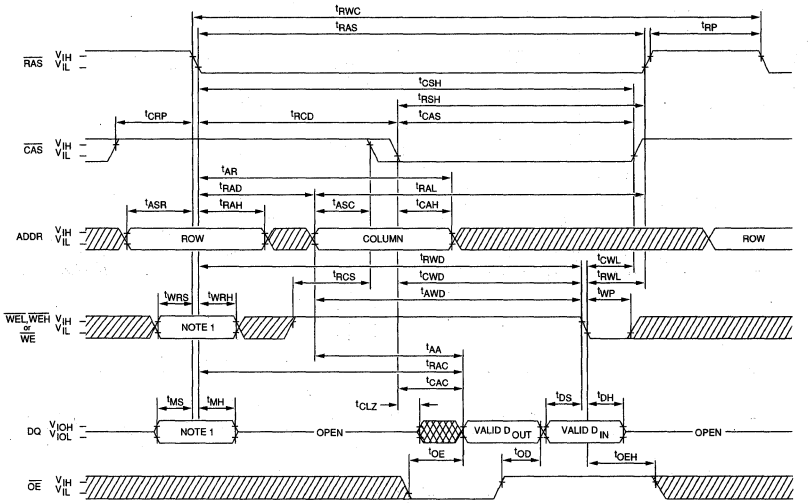


EARLY-WRITE CYCLE

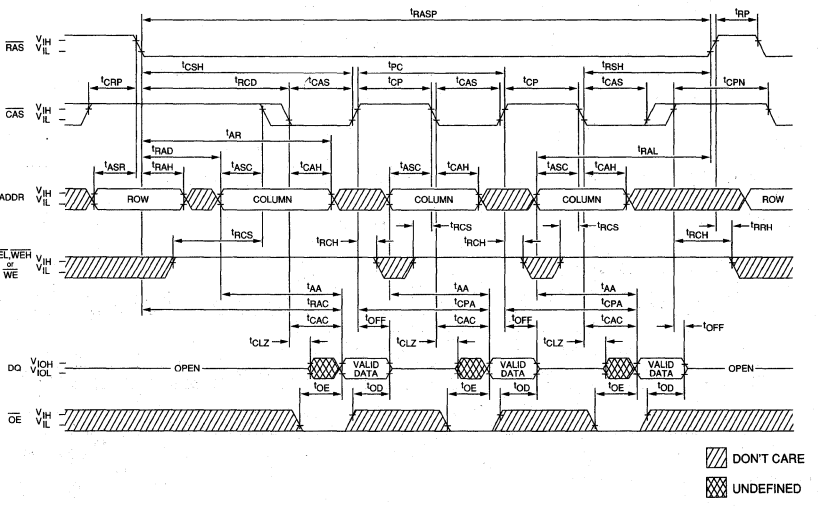


NOTE: 1. Applies to MT4C1665 L only; $\overline{WEL}$, $\overline{WEH}$ and DQ inputs on MT4C1664 L are "don't care" at $\overline{RAS}$ time. $\overline{WE}$ selects between normal WRITE and MASKED WRITE at $\overline{RAS}$ time. The DQ inputs are "don't care" for a normal WRITE, $\overline{WE}$ HIGH at $\overline{RAS}$ time. The DQ inputs provide the mask data at $\overline{RAS}$ time for a MASKED WRITE, $\overline{WE}$ LOW at $\overline{RAS}$ time.

READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)

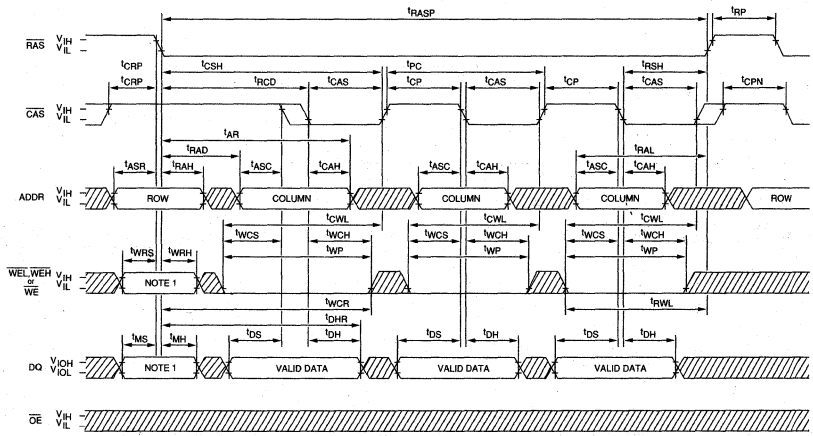


FAST-PAGE-MODE READ CYCLE

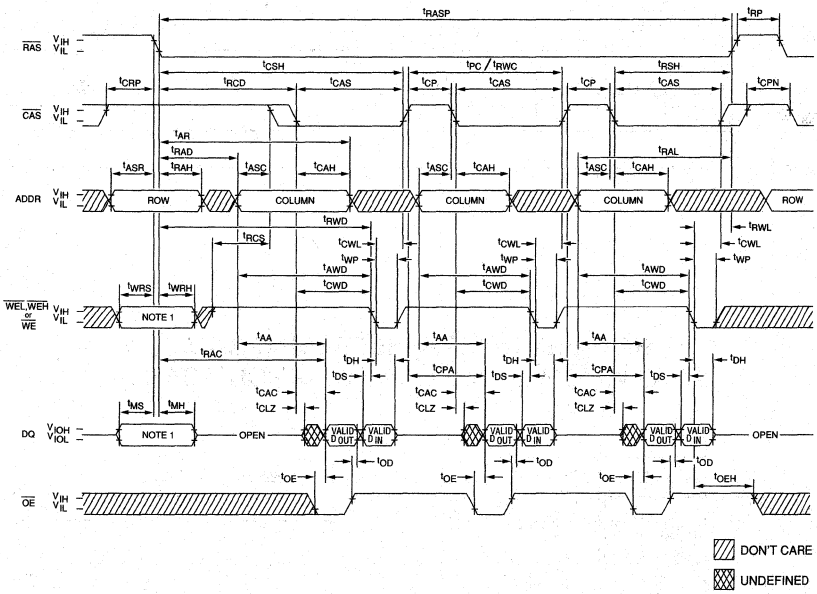


NOTE: 1. Applies to MT4C1665 L only; $\overline{WEL}$, $\overline{WEH}$ and DQ inputs on MT4C1664 L are "don't care" at $\overline{RAS}$ time. $\overline{WE}$ selects between normal WRITE and MASKED WRITE at $\overline{RAS}$ time. The DQ inputs are "don't care" for a normal WRITE, $\overline{WE}$ HIGH at $\overline{RAS}$ time. The DQ inputs provide the mask data at $\overline{RAS}$ time for a MASKED WRITE, $\overline{WE}$ LOW at $\overline{RAS}$ time.

FAST-PAGE-MODE EARLY-WRITE CYCLE



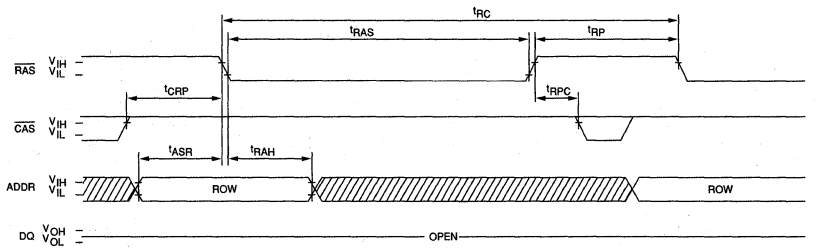
FAST-PAGE-MODE READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)



NOTE: 1. Applies to MT4C1665 L only; $\overline{WEL}$, $\overline{WEH}$ and DQ inputs on MT4C1664 L are "don't care" at $\overline{RAS}$ time. $\overline{WE}$ selects between normal WRITE and MASKED WRITE at $\overline{RAS}$ time. The DQ inputs are "don't care" for a normal WRITE, $\overline{WE}$ HIGH at $\overline{RAS}$ time. The DQ inputs provide the mask data at $\overline{RAS}$ time for a MASKED WRITE, $\overline{WE}$ LOW at $\overline{RAS}$ time.

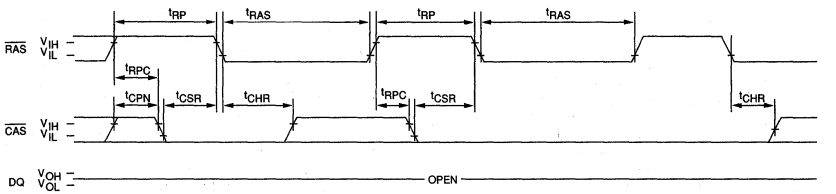
RAS-ONLY REFRESH CYCLE

(ADDR = A0-A7, OE; WEL, WEH or WE = DON'T CARE)



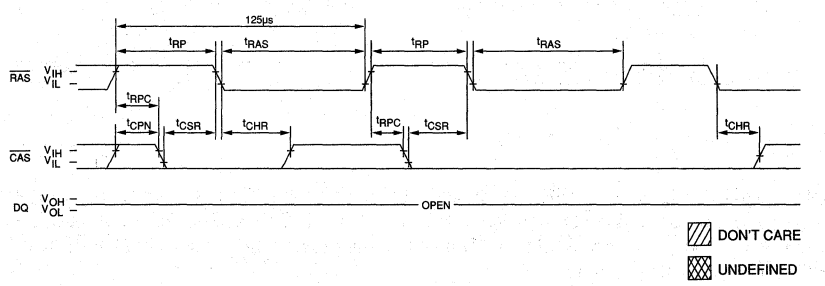
CAS-BEFORE-RAS REFRESH CYCLE

(A0-A7 WEL, WEH or WE, and OE = DON'T CARE)



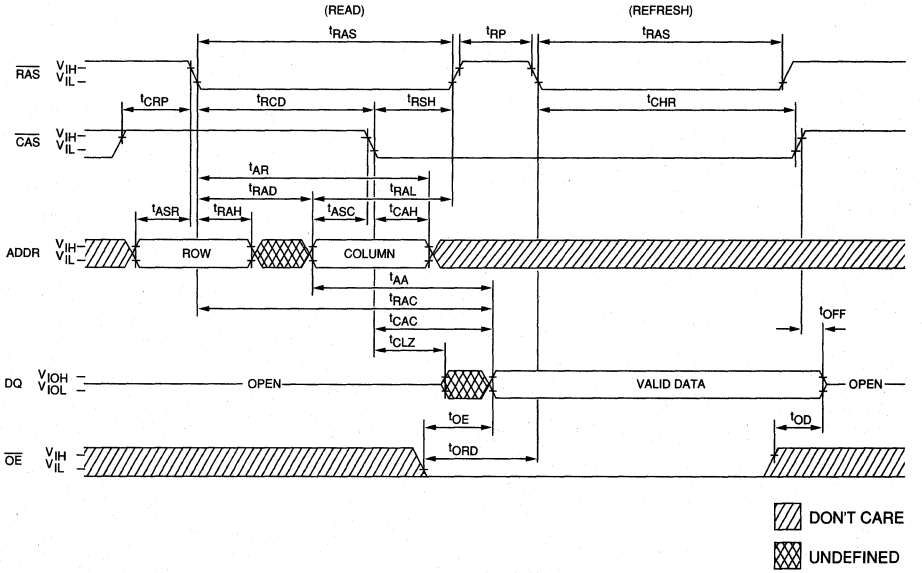
BATTERY BACKUP REFRESH CYCLE

(A0-A7 WEL, WEH or WE, and OE = DON'T CARE)



HIDDEN REFRESH CYCLE [24]

($\overline{WEL}$, $\overline{WEH}$ or $\overline{WE}$ = HIGH; $\overline{OE}$ = LOW)



DRAM

64K x 16 DRAM

STATIC COLUMN MODE

FEATURES

- Industry standard x16 pinouts, timing, functions and packages
- High-performance, CMOS silicon-gate process
- Single +5V±10% power supply
- Low power, 3mW standby; 225mW active, typical
- All device pins are fully TTL compatible
- 256 cycle refresh in 4ms
- Refresh modes: $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$ and HIDDEN
- Optional STATIC COLUMN MODE access cycle
- BYTE WRITE access cycle (MT4C1670 only)
- NONPERSISTENT MASKED WRITE access cycle (MT4C1671 only)

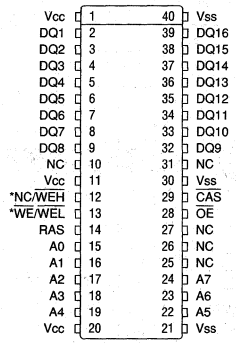
OPTIONS — MARKING

- Timing
  - 70ns access — -7
  - 80ns access — -8
  - 100ns access — -10
- Write Enable
  - Byte or Word — MT4C1670
  - Word only — MT4C1671
- Mask Enable
  - Not Available — MT4C1670
  - Always Available — MT4C1671
- Packages
  - Plastic SOJ (400mil) — DJ
  - Plastic TSOP (400mil) — TG
  - Plastic ZIP (475mil) — Z

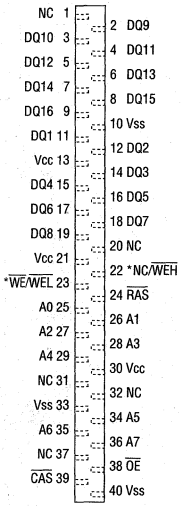
NOTE: Available in die form Please consult factory for die data sheets.

PIN ASSIGNMENT (Top View)

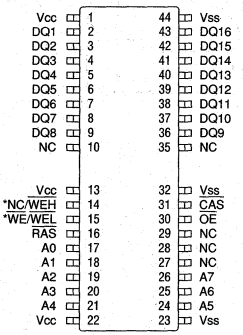
40-Pin SOJ (Q-6)



40-Pin Zip (O-4)



40-Pin TSOP (R-5)



*MT4C1671/MT4C1670

GENERAL DESCRIPTION

The MT4C1670/1 are randomly accessed solid-state memories containing 1,048,576 bits organized in a x16 configuration. The MT4C1670 has both BYTE and WORD WRITE access cycles while the MT4C1671 has only WORD WRITE access cycles.

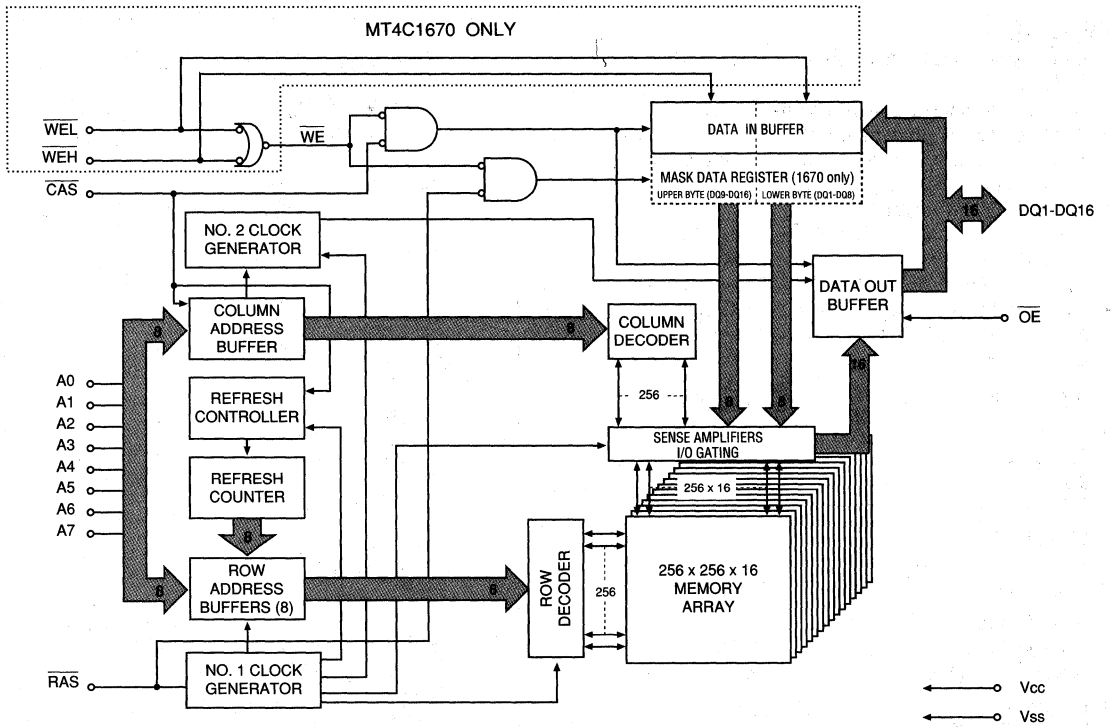
The MT4C1670 functions in a similar manner to the MT4C1671 except that replacing $\overline{WE}$ with $\overline{WEL}$ and $\overline{WEH}$ allows for BYTE WRITE access cycles. $\overline{WEL}$ and $\overline{WEH}$ function in an identical manner to $\overline{WE}$: either $\overline{WEL}$ or $\overline{WEH}$ will generate an internal $\overline{WE}$ through an AND gate (Inverted NOR gate).

The MT4C1670 "$\overline{WE}$" function and timing are determined by the first BYTE WRITE ($\overline{WEL}$ or $\overline{WEH}$) to transition LOW and the last to transition back HIGH. Use of only one of the two results in a BYTE WRITE cycle: $\overline{WEL}$ transitioning LOW selects a WRITE cycle for the lower byte (DQ1-DQ8) or $\overline{WEH}$ transitioning LOW selects a WRITE cycle for the upper byte (DQ9-DQ16).

The MT4C1671 has NONPERSISTENT MASKED WRITE capability.

WIDE DRAM

FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTIONS

SOJ PIN NUMBERS	ZIP PIN NUMBERS	TSOP PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
14	24	16	$\overline{RAS}$	Input	ROW Address Strobe: $\overline{RAS}$ is used to clock-in the 8 row address bits and strobe the $\overline{WEL}$, $\overline{WEH}$ and DQ inputs for the MASKED WRITE function.
29	39	31	$\overline{CAS}$	Input	Column Address Strobe: $\overline{CAS}$ is used to clock-in the 8 column address bits, enable the DRAM output buffers, and strobe the data inputs on WRITE cycles.
28	38	30	$\overline{OE}$	Input	Output Enable: $\overline{OE}$ enables the output buffers when taken LOW during a READ access cycle. $\overline{RAS}$ and $\overline{CAS}$ must be LOW and $\overline{WEL}$ and $\overline{WEH}$ must be HIGH before $\overline{OE}$ will control the output buffers. Otherwise the output buffers are in a High-Z state.
13	23	15	$\overline{WE}$/$\overline{WEL}$*	Input	Write Enable Lower Byte: $\overline{WEL}$ on MT4C1670 is $\overline{WE}$ control for the DQ1 through DQ8 inputs. $\overline{WE}$ on MT4C1671 controls DQ1 through DQ16 inputs. If ($\overline{WEL}$ or $\overline{WEH}$)/$\overline{WE}$ is LOW, the access is a WRITE cycle. The DQ outputs for the byte not being written will remain in a High-Z state (byte WRITE cycle only).
12	22	14	NC/$\overline{WEH}$*	Input	Write Enable Upper Byte: $\overline{WEH}$ on MT4C1670 is $\overline{WE}$ control for the DQ9 through DQ16 inputs. If ($\overline{WEL}$ or $\overline{WEH}$)/$\overline{WE}$ is LOW, the access is a WRITE cycle. This pin is a no connect on the MT4C1671 as it has only WORD WRITE access cycles.
15-19, 22-24	25-29, 34-36	17-21, 24-26	A0-A7	Input	Address Inputs: These inputs are multiplexed and clocked by $\overline{RAS}$ and $\overline{CAS}$ to select one 16-bit word out of the 64K available words.
2-9, 32-39	11, 12, 14-17, 2, 18, 19, 3-9	2-9, 36-43	DQ1-DQ16	Input/ Output	Data I/O: For WRITE cycles, DQ1-DQ16 act as inputs to the addressed DRAM location. BYTE WRITEs can be performed by using $\overline{WEL}$ or $\overline{WEH}$ to select the byte to be written. For READ access cycles, DQ1-DQ16 act as outputs for the addressed DRAM ocation. All 16 I/Os are active for READ cycles (there is no BYTE READ cycle).
10, 25, 26, 27, 31	1, 20, 31, 32, 37	10, 27-29, 35	NC	-	No Connect: These pins should be either left unconnected or tied to ground.
1, 11, 20	13, 21, 30	1, 13, 22	Vcc	Supply	Power Supply: +5V ± 10%
21, 30, 40	10, 33, 40	23, 32, 44	Vss	Supply	Ground

NOTE: *MT4C1671/MT4C1670

FUNCTIONAL DESCRIPTION

Each bit is uniquely addressed through the 16 address-bits during READ or WRITE cycles. These are entered 8 bits (A0-A7) at a time. $\overline{RAS}$ is used to latch the first 8 bits and $\overline{CAS}$ the latter 8 bits.

READ or WRITE cycles on the MT4C1671 are selected with the $\overline{WE}$ input while either $\overline{WEL}$ or $\overline{WEH}$ perform the "$\overline{WE}$" on the MT4C1670. The MT4C1670 "$\overline{WE}$" function is determined by the first BYTE WRITE ($\overline{WEL}$ or $\overline{WEH}$) to transition LOW and the last one to transition back HIGH.

A logic HIGH on $\overline{WE}$ dictates READ mode while a logic LOW on $\overline{WE}$ dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. Taking $\overline{WE}$ LOW will initiate a WRITE cycle, selecting DQ1 through DQ16. If $\overline{WE}$ goes LOW prior to $\overline{CAS}$ going LOW, the output pin(s) remain open (High-Z) until the next $\overline{CAS}$ cycle. If $\overline{WE}$ goes LOW after $\overline{CAS}$ goes LOW and data reaches the output pins, data out (Q) is activated and retains the selected cell data as long as $\overline{CAS}$ and $\overline{OE}$ remain LOW (regardless of $\overline{WE}$ or $\overline{RAS}$). This late $\overline{WE}$ pulse results in a READ-WRITE cycle.

The 16 data inputs and 16 data outputs are routed through 16 pins using common I/O, and pin direction is controlled by $\overline{OE}$, $\overline{WEL}$ and $\overline{WEH}$ (MT4C1670) or $\overline{WE}$ (MT4C1671).

STATIC COLUMN operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row address (A0-A7) defined page boundary. The STATIC COLUMN cycle is always initiated with a row address strobed-in by $\overline{RAS}$ followed by a column address strobed-in by $\overline{CAS}$. $\overline{CAS}$ may be toggled by holding $\overline{RAS}$ LOW and strobing-in different column addresses, thus executing faster memory cycles. Faster STATIC COLUMN WRITE cycles must have $\overline{CAS}$ or $\overline{WE}$ toggled strobing-in the different column addresses. Returning $\overline{RAS}$ HIGH terminates the STATIC COLUMN operation.

Returning $\overline{RAS}$ and $\overline{CAS}$ HIGH terminates a memory cycle and decreases chip current to a reduced standby level. The chip is also preconditioned for the next cycle during the $\overline{RAS}$ high time. Memory cell data is retained in its correct state by maintaining power and executing any $\overline{RAS}$ cycle (READ, WRITE, $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$, or HIDDEN refresh) so that all 256 combinations of $\overline{RAS}$ addresses (A0-A7) are executed at least every 4ms, regardless of sequence. The $\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh cycle will also invoke the refresh counter and controller for row address control.

BYTE WRITE ACCESS CYCLE (MT4C1670 ONLY)

The BYTE WRITE mode is determined by the use of $\overline{WEL}$ and $\overline{WEH}$. Enabling $\overline{WEL}$ will select a lower BYTE WRITE cycle (DQ1-DQ8) while Enabling $\overline{WEH}$ will select an upper BYTE WRITE (DQ9-DQ16). Enabling both $\overline{WEL}$ and $\overline{WEH}$ selects a WORD WRITE cycle.

The MT4C1670 may be viewed as two 64K x 8 DRAMS, which have common input controls, with the exception of the WE input. Figure 1 illustrates the MT4C1670 BYTE and WORD WRITE cycles.

MASKED WRITE DESCRIPTION (MT4C1671 ONLY)

Every WRITE access cycle may be a MASKED WRITE, depending on the state of $\overline{WE}$ at $\overline{RAS}$ time. A MASKED WRITE is selected when mask data is supplied on the DQ pins and $\overline{WE}$ is LOW at $\overline{RAS}$ time. The MT4C1671 is only word selectable when $\overline{WE}$ is LOW at $\overline{RAS}$ time (the MT4C1670 does not have a MASKED WRITE cycle function).

The data (mask data) present on the DQ1-DQ16 inputs at $\overline{RAS}$ time will be written to an internal bit mask data register and will then act as an individual write enable for each of the corresponding DQ inputs. If a LOW (logic "0") is written to a mask data register bit, the input port for that bit is disabled during the subsequent WRITE operation and no new data will be written to that DRAM cell location. A HIGH (logic "1") on a mask data register bit enables the input port and allows normal WRITE operations to proceed. At $\overline{CAS}$ time, the bits present on the DQ1-DQ16 inputs will be written to the DRAM (if the mask data bit was HIGH) or ignored (if the mask data bit was LOW).

New mask data must be supplied each time a MASKED WRITE cycle is initiated, even if the previous cycle's mask was the same mask.

Figure 2 illustrates the MT4C1671 MASKED WRITE operation (Note: $\overline{RAS}$ or $\overline{CAS}$ time refers to the time at which $\overline{RAS}$ or $\overline{CAS}$ transition from HIGH to LOW).

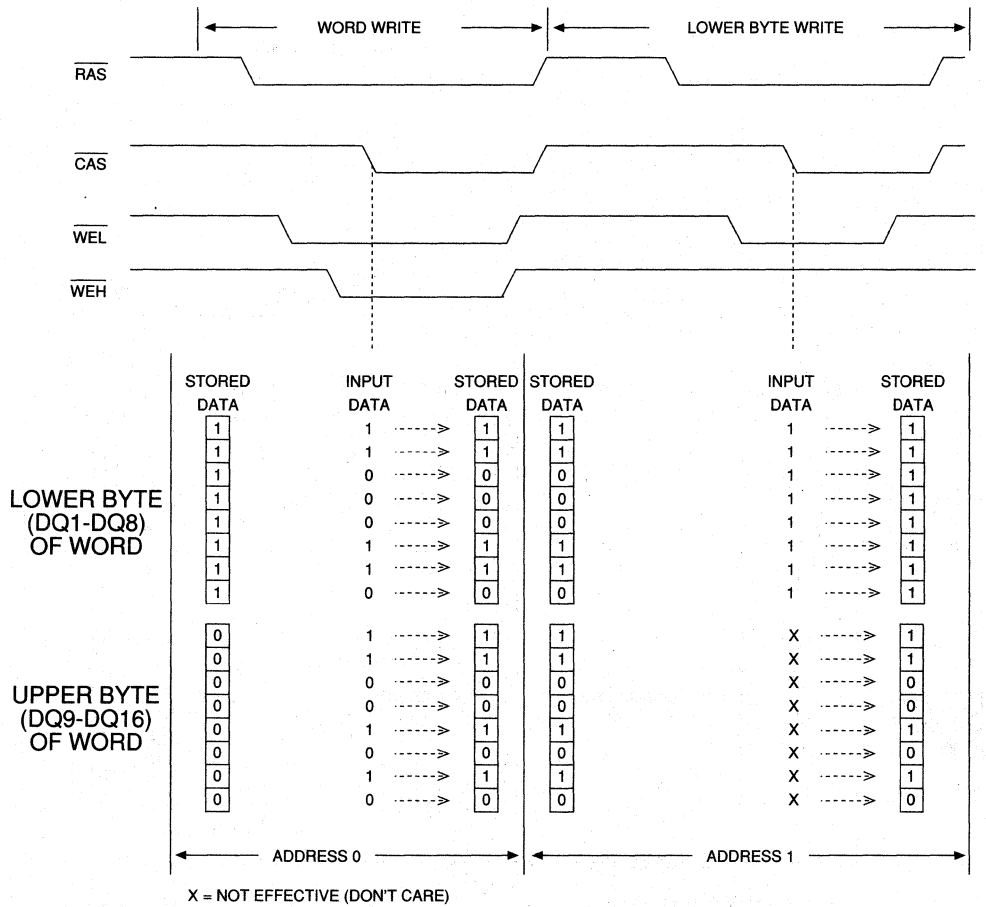


Figure 1
MT4C1670 WORD AND BYTE WRITE EXAMPLE

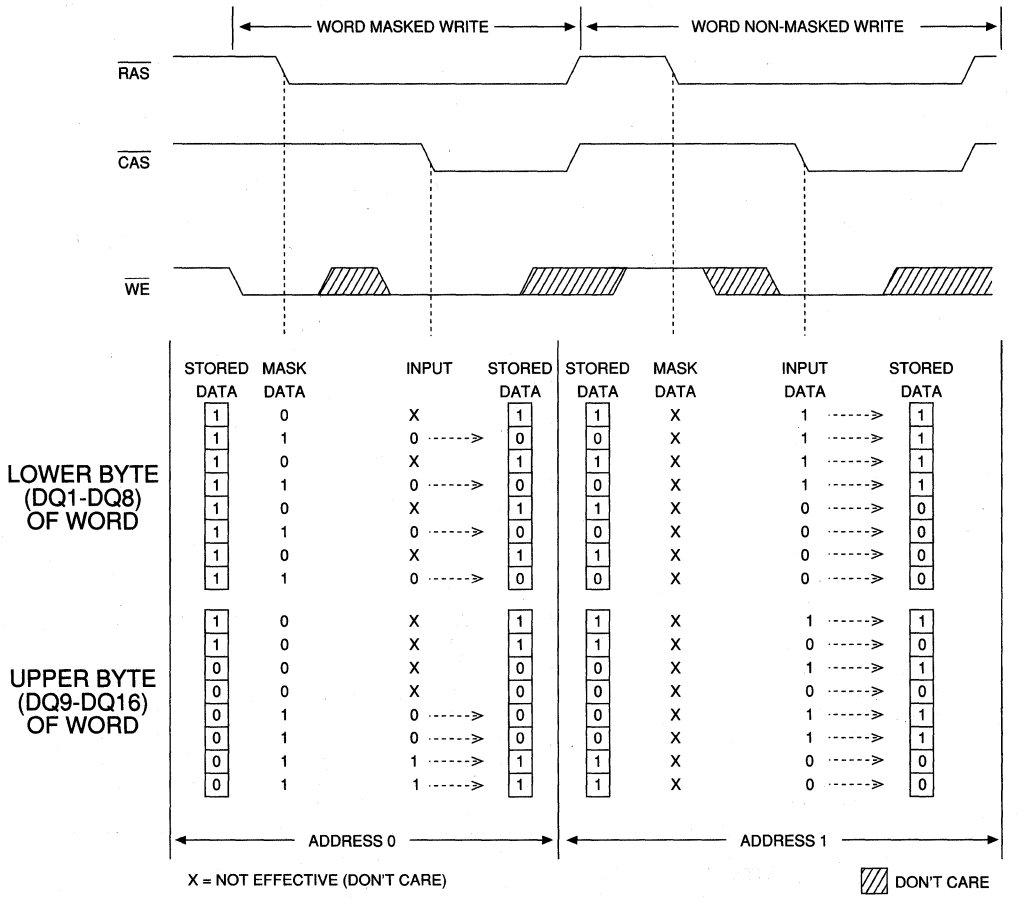


Figure 2
MT4C1671 MASKED WRITE EXAMPLE

TRUTH TABLE: MT4C1670

FUNCTION		RAS	CAS	WEL	WEH	OE	ADDRESSES tR	ADDRESSES tC	DQs	NOTES
Standby		H	H→X	X	X	X	X	X	High-Z	
READ		L	L	H	H	L	ROW	COL	Data Out	
WRITE: WORD (EARLY-WRITE)		L	L	L	L	X	ROW	COL	Data In	
WRITE: LOWER BYTE (EARLY)		L	L	L	H	X	ROW	COL	Lower Byte, Data In Upper Byte, High-Z	
WRITE: UPPER BYTE (EARLY)		L	L	H	L	X	ROW	COL	Lower Byte, High-Z Upper Byte, Data In	
READ-WRITE		L	L	H→L	H→L	L→H	ROW	COL	Data Out, Data In	1
STATIC COLUMN	1st Cycle	L	L	H	H	L	ROW	COL	Data Out	
READ	2nd Cycle	L	L	H	H	L	n/a	COL	Data Out	
STATIC COLUMN	1st Cycle	L	L	L	L	X	ROW	COL	Data In	1
EARLY-WRITE	2nd Cycle	L	L	L	L	X	n/a	COL	Data In	1, 3
STATIC COLUMN	1st Cycle	L	L	H→L	H→L	L→H	ROW	COL	Data Out, Data In	1
READ-WRITE	2nd Cycle	L	L	H→L	H→L	L→H	n/a	COL	Data Out, Data In	1
HIDDEN	READ	L→H→L	L	H	H	L	ROW	COL	Data Out	
REFRESH	WRITE	L→H→L	L	L	L	X	ROW	COL	Data In	1, 2
RAS-ONLY REFRESH		L	H	X	X	X	ROW	n/a	High-Z	
CAS-BEFORE-RAS REFRESH		H→L	L	X	X	X	X	X	High-Z	

NOTE: 1. These cycles may also be BYTE WRITE cycles (either WEL or WEH active).
2. EARLY-WRITE only.
3. Either CAS or WEL / WEH must latch in each additional column address and input data.

TRUTH TABLE: MT4C1671

FUNCTION		RAS	CAS	WE	OE	ADDRESSES t_R	ADDRESSES t_C	DQs	NOTES
Standby		H	H→X	X	X	X	X	High-Z	
READ		L	L	H	L	ROW	COL	Data Out	
WRITE: WORD (EARLY-WRITE)		L	L	L	X	ROW	COL	Data In	1
READ-WRITE		L	L	H→L	L→H	ROW	COL	Data Out, Data In	1
STATIC COLUMN	1st Cycle	L	L	H	L	ROW	COL	Data Out	
READ	2nd Cycle	L	L	H	L	n/a	COL	Data Out	
STATIC COLUMN	1st Cycle	L	L	L	X	ROW	COL	Data In	1
EARLY-WRITE	2nd Cycle	L	L	L	X	n/a	COL	Data In	1, 3
STATIC COLUMN	1st Cycle	L	L	H→L	L→H	ROW	COL	Data Out, Data In	1
READ-WRITE	2nd Cycle	L	L	H→L	L→H	n/a	COL	Data Out, Data In	1
HIDDEN	READ	L→H→L	L	H	L	ROW	COL	Data Out	
REFRESH	WRITE	L→H→L	L	L	X	ROW	COL	Data In	1, 2
RAS-ONLY REFRESH		L	H	X	X	ROW	n/a	High-Z	
CAS-BEFORE-RAS REFRESH		H→L	L	X	X	X	X	High-Z	

NOTE: 1. Data-in will be dependent on the mask provided. Refer to Figure 2.
2. EARLY-WRITE only.
3. Either CAS or WEL / WEH must latch in each additional column address and input data.

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} ..... -1.0V to +7.0V
Operating Temperature, T_A (Ambient) ..... 0°C to +70°C
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 3, 4, 6, 7) (0°C ≤ T_A ≤ 70°C; V_{CC} = 5V ± 10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.5	V	1
Input High (Logic 1) Voltage, All Inputs	V_{IH}	2.4	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, All Inputs	V_{IL}	-1.0	0.8	V	1
INPUT LEAKAGE CURRENT Any Input 0V ≤ V_{IN} ≤ Vcc (All other pins not under test = 0V)	I_I	-2	2	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled; 0V ≤ V_{OUT} ≤ 5.5V)	I_{OZ}	-10	10	µA	
OUTPUT LEVELS Output High Voltage (I_{OUT} = -2.5mA)	V_{OH}	2.4		V	
Output Low Voltage (I_{OUT} = 2.1mA)	V_{OL}		0.4	V	

		MAX				
PARAMETER/CONDITION	SYMBOL	-7	-8	-10	UNITS	NOTES
STANDBY CURRENT: (TTL) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC1}	2	2	2	mA	
STANDBY CURRENT: (CMOS) ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} -0.2V)	I_{CC2}	1	1	1	mA	25
OPERATING CURRENT: Random READ/WRITE Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC (MIN))	I_{CC3}	120	115	90	mA	3, 4, 31
OPERATING CURRENT: STATIC COLUMN Average power supply current ($\overline{RAS}$ = V_{IL}; $\overline{CAS}$, Address Cycling: ^tSC = ^tSC (MIN))	I_{CC4}	110	95	80	mA	3, 4, 31
REFRESH CURRENT: $\overline{RAS}$-ONLY Average power supply current ($\overline{RAS}$ Cycling, $\overline{CAS}$=V_{IH}: ^tRC = ^tRC (MIN))	I_{CC5}	120	115	90	mA	3, 31
REFRESH CURRENT: $\overline{CAS}$-BEFORE-$\overline{RAS}$ (CBR) Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC (MIN))	I_{CC6}	120	115	90	mA	3, 5

CAPACITANCE

(Note: 2)

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A7	C_{I1}		5	pF	2
Input Capacitance: $\overline{RAS}$, $\overline{CAS}$,($\overline{WEL}$, $\overline{WEH}$)/ $\overline{WE}$, $\overline{OE}$	C_{I2}		7	pF	2
Input/Output Capacitance: DQ	C_{IO}		7	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13, 23) (0°C ≤ T_A ≤ +70°C; Vcc = 5V ± 10%)

AC CHARACTERISTICS		-7		-8		-10			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	^tRC	130		150		180		ns	
READ-WRITE cycle time	^tRWC	175		185		220		ns	
STATIC-COLUMN READ or WRITE cycle time	^tSC	45		50		55		ns	
STATIC-COLUMN READ-WRITE cycle time	^tSRWC	95		100		120		ns	
Access time from $\overline{RAS}$	^tRAC		70		80		100	ns	14
Access time from $\overline{CAS}$	^tCAC		25		35		40	ns	15
Output Enable time	^tOE		25		35		40	ns	
Access time from column address	^tAA		40		45		55	ns	
Access time from $\overline{CAS}$ precharge	^tCPA		45		50		55	ns	
$\overline{RAS}$ pulse width	^tRAS	70	100,000	80	100,000	100	100,000	ns	
$\overline{RAS}$ pulse width (STATIC COLUMN)	^tRASC	70	100,000	80	100,000	100	100,000	ns	
$\overline{RAS}$ hold time	^tRSH	20		35		40		ns	
$\overline{RAS}$ precharge time	^tRP	50		60		70		ns	
$\overline{CAS}$ pulse width	^tCAS	25	100,000	35	100,000	40	100,000	ns	
$\overline{CAS}$ hold time	^tCSH	70		80		100		ns	
$\overline{CAS}$ precharge time	^tCPN	10		10		15		ns	16
$\overline{CAS}$ precharge time (STATIC COLUMN)	^tCP	10		10		10		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	^tRCD	20	45	20	45	25	60	ns	17
$\overline{CAS}$ to $\overline{RAS}$ precharge time	^tCRP	5		10		10		ns	
Row address setup time	^tASR	0		0		0		ns	
Row address hold time	^tRAH	10		12		15		ns	
$\overline{RAS}$ to column address delay time	^tRAD	15	35	17	40	20	55	ns	18
Column address setup time	^tASC	0		0		0		ns	
Column address hold time	^tCAH	15		15		20		ns	
Column address hold time (referenced to $\overline{RAS}$)	^tAR	55		60		70		ns	
Column address to $\overline{RAS}$ lead time	^tRAL	35		45		55		ns	
Read command setup time	^tRCS	0		0		0		ns	26
Read command hold time (referenced to $\overline{CAS}$)	^tRCH	0		0		0		ns	19, 26
Read command hold time (referenced to $\overline{RAS}$)	^tRRH	0		10		10		ns	19
$\overline{CAS}$ to output in Low-Z	^tCLZ	0		0		0		ns	
Output buffer turn-off delay	^tOFF	0	20	0	20	0	20	ns	20, 30

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

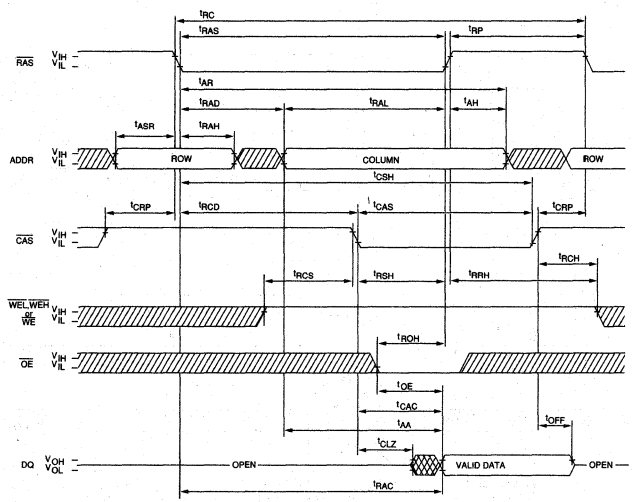
(Notes: 6, 7, 8, 9, 10, 11, 12, 13, 23) (0°C ≤ T_A ≤ +70°C; Vcc = 5V ± 10%)

AC CHARACTERISTICS		-7		-8		-10			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Output disable time	^tOD		15		20		20	ns	30
Write command setup time	^tWCS	0		0		0		ns	21, 26
Write command hold time	^tWCH	15		15		20		ns	26
Write command hold time (referenced to $\overline{RAS}$)	^tWCR	50		55		70		ns	26
Write command pulse width	^tWP	15		15		20		ns	26
Write command to $\overline{RAS}$ lead time	^tRWL	20		35		40		ns	26
Write command to $\overline{CAS}$ lead time	^tCWL	20		35		40		ns	26
Data-in setup time	^tDS	0		0		0		ns	22
Data-in hold time	^tDH	15		15		20		ns	22
Data-in hold time (referenced to $\overline{RAS}$)	^tDHR	50		60		70		ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	^tRWD	90		100		125		ns	21
Column address to $\overline{WE}$ delay time	^tAWD	65		70		80		ns	21
$\overline{CAS}$ to $\overline{WE}$ delay time	^tCWD	50		55		70		ns	21
Transition time (rise or fall)	^tT	3	50	3	50	3	50	ns	9, 10
Refresh period (256 cycles)	^tREF		4		4		4	ms	28
$\overline{RAS}$ to $\overline{CAS}$ precharge time	^tRPC	0		10		10		ns	
$\overline{CAS}$ setup time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tCSR	10		10		10		ns	5
$\overline{CAS}$ hold time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tCHR	15		25		30		ns	5
MASKED WRITE command to $\overline{RAS}$ setup time	^tWRS	0		0		0		ns	26, 27
MASKED WRITE command to $\overline{RAS}$ hold time	^tWRH	15		15		15		ns	26, 27
Mask data to $\overline{RAS}$ setup time	^tMS	0		0		0		ns	26
Mask data to $\overline{RAS}$ hold time	^tMH	15		15		15		ns	26
$\overline{OE}$ hold time from $\overline{WE}$ during READ-MODIFY-WRITE cycle	^tOEH	10		20		20		ns	29
$\overline{OE}$ setup prior to $\overline{RAS}$ during HIDDEN REFRESH cycle	^tORD	0		0		0		ns	
Last WRITE to column address delay	^tLWAD	20	30	20	35	25	45	ns	
Access time from last WRITE	^tALW	65		75		95		ns	
Output data enable from WRITE	^tOW	^tAA		^tAA		^tAA		ns	
Output data hold time from column address	^tAOH	5		5		5		ns	
$\overline{RAS}$ hold time referenced to $\overline{OE}$	^tROH	10		10		10		ns	
Column address hold time referenced to $\overline{RAS}$ HIGH	^tAH	5		5		10		ns	
$\overline{CAS}$ pulse width in STATIC-COLUMN mode	^tCSC	^tCAS		^tCAS		^tCAS		ns	
Write command inactive time	^tWI	10		10		10		ns	

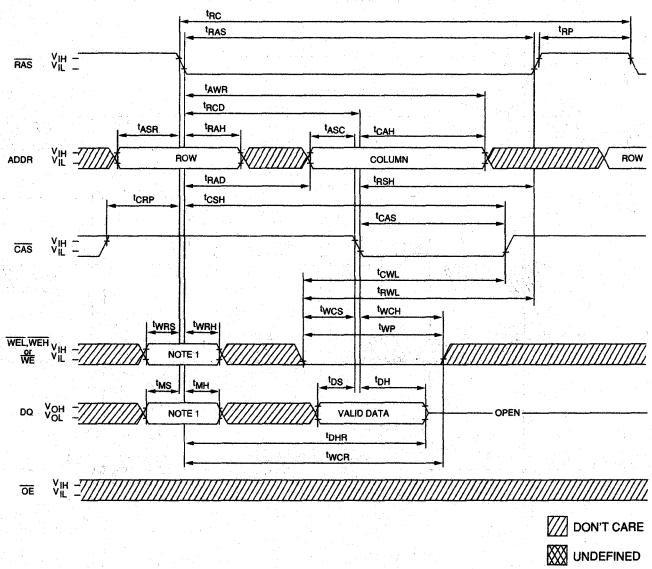
NOTES

1. All voltages referenced to Vss.
2. This parameter is sampled. Vcc = 5V ±10%, f = 1 MHz.
3. Icc is dependent on cycle rates.
4. Icc is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \le T_A \le 70°C$) is assured.
7. An initial pause of 100µs is required after power-up followed by any eight $\overline{RAS}$ cycles before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-up should be repeated any time the 4ms refresh requirement is exceeded.
8. AC characteristics assume ^tT = 5ns.
9. VIH (MIN) and VIL (MAX) are reference levels for measuring timing of input signals. Transition times are measured between VIH and VIL (or between VIL and VIH).
10. In addition to meeting the transition rate specification, all input signals must transit between VIH and VIL (or between VIL and VIH) in a monotonic manner.
11. If $\overline{CAS}$ = VIH, data output is High-Z.
12. If $\overline{CAS}$ = VIL, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to 1 TTL gates and 50pF.
14. Assumes that $^tRCD < ^tRCD$ (MAX). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
15. Assumes that $^tRCD \ge ^tRCD$ (MAX).
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, data out (Q) will be maintained from the previous cycle. To initiate a new cycle and clear the Q buffer, $\overline{CAS}$ must be pulsed HIGH for ^tCPN.
17. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (MAX) limit, then access time is controlled exclusively by ^tCAC.
18. Operation within the ^tRAD (MAX) limit ensures that ^tRCD (MAX) can be met. ^tRAD (MAX) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (MAX) limit, then access time is controlled exclusively by ^tAA.
19. Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
20. ^tOFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to VOH or VOL.
21. ^tWCS, ^tRWD, ^tAWD and ^tCWD are restrictive operating parameters in LATE-WRITE and READ-MODIFY-WRITE cycles only. If $^tWCS \ge ^tWCS$ (MIN), the cycle is an EARLY-WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If $^tRWD \ge ^tRWD$ (MIN), $^tAWD \ge ^tAWD$ (MIN) and $^tCWD \ge ^tCWD$ (MIN), the cycle is a LATE-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions are met, the state of data out are indeterminate. $\overline{OE}$ held HIGH and $\overline{WE}$ taken LOW after $\overline{CAS}$ goes LOW results in a LATE-WRITE ($\overline{OE}$ controlled) cycle.
22. These parameters are referenced to $\overline{CAS}$ leading edge in early WRITE cycles and $\overline{WE}$ leading edge in LATE-WRITE or READ-MODIFY-WRITE cycles.
23. If $\overline{OE}$ is tied permanently LOW, LATE-WRITE or READ-MODIFY-WRITE operations are not possible.
24. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case $\overline{WE}$ = LOW and $\overline{OE}$=HIGH.
25. All other inputs at Vcc -0.2V.
26. WRITE command is defined as either $\overline{WEL}$ or $\overline{WEH}$ or both going LOW on the MT4C1670. WRITE command is defined as $\overline{WE}$ going LOW on the MT4C1671.
27. Must be held LOW to ensure MASKED WRITE is enabled and must be held HIGH to ensure MASKED WRITE is disabled.
28. The refresh period may be extended to 8ms without experiencing problems.
29. LATE-WRITE and READ-MODIFY-WRITE cycles must have both ^tOD and ^tOEH met ($\overline{OE}$ HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. The DQs will provide the previously read data if $\overline{CAS}$ remains LOW and $\overline{OE}$ is taken back LOW after ^tOEH is met. If $\overline{CAS}$ goes HIGH prior to $\overline{OE}$ going back LOW, the DQs will remain open.
30. The DQs open during READ cycles once ^tOD or ^tOFF occur. If $\overline{CAS}$ goes HIGH first, $\overline{OE}$ becomes a "don't care." If $\overline{OE}$ goes HIGH and $\overline{CAS}$ stays LOW, $\overline{OE}$ is not a "don't care;" and the DQs will provide the previously read data if $\overline{OE}$ is taken back LOW (while $\overline{CAS}$ remains LOW).
31. Column address changed once while $\overline{RAS}$ = VIL and $\overline{CAS}$ = VIH.

READ CYCLE

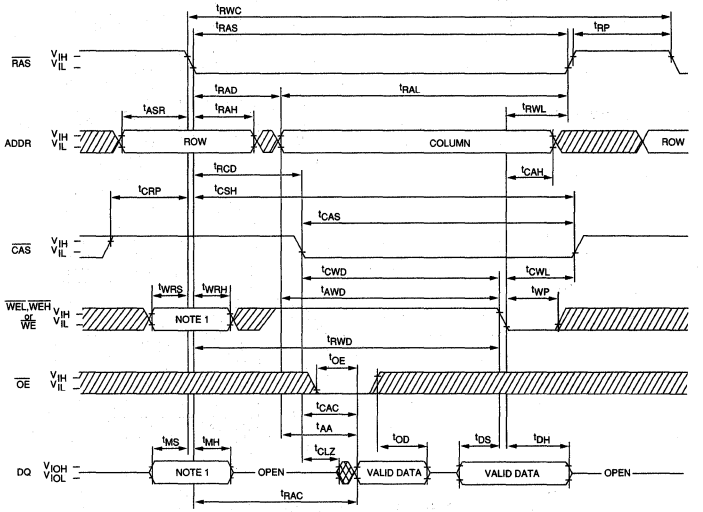


EARLY-WRITE CYCLE

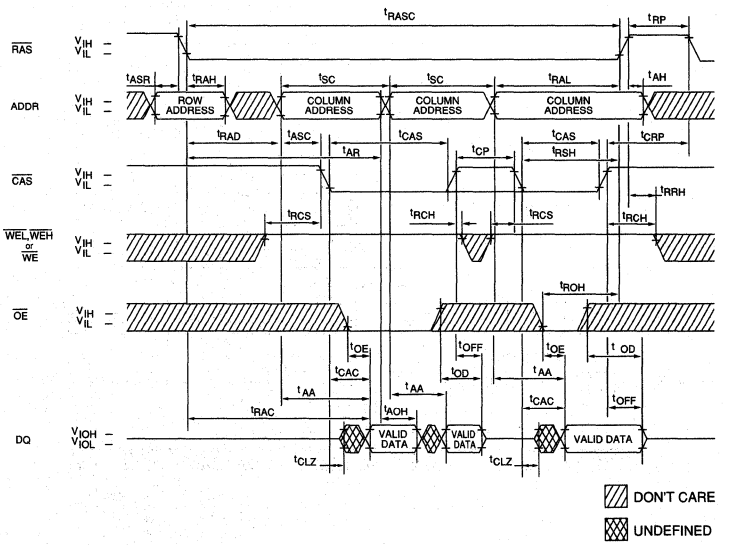


NOTE: 1. Applies to MT4C1671 only; $\overline{WEL}$, $\overline{WEH}$ and DQ inputs on MT4C1670 are "don't care" at $\overline{RAS}$ time. $\overline{WE}$ selects between normal WRITE and MASKED WRITE at $\overline{RAS}$ time. The DQ inputs are "don't care" for a normal WRITE, $\overline{WE}$ HIGH at $\overline{RAS}$ time. The DQ inputs provide the mask data at $\overline{RAS}$ time for a MASKED WRITE, $\overline{WE}$ LOW at $\overline{RAS}$ time.

READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)

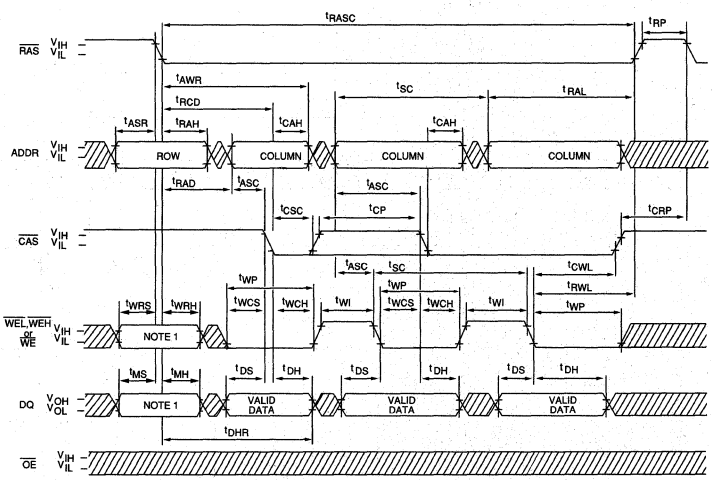


STATIC-COLUMN READ CYCLE

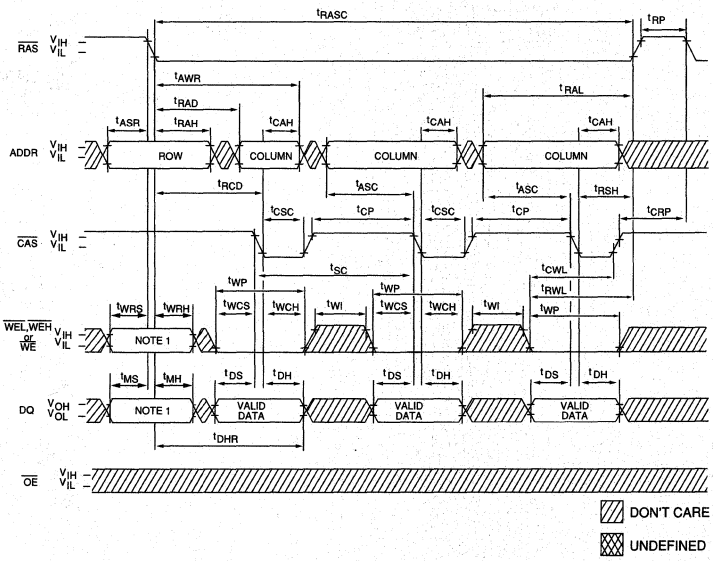


NOTE: 1. Applies to MT4C1671 only; $\overline{WEL}$, $\overline{WEH}$ and DQ inputs on MT4C1670 are "don't care" at $\overline{RAS}$ time. $\overline{WE}$ selects between normal WRITE and MASKED WRITE at $\overline{RAS}$ time. The DQ inputs are "don't care" for a normal WRITE, $\overline{WE}$ HIGH at $\overline{RAS}$ time. The DQ inputs provide the mask data at $\overline{RAS}$ time for a MASKED WRITE, $\overline{WE}$ LOW at $\overline{RAS}$ time.

STATIC-COLUMN EARLY-WRITE CYCLE
($\overline{WE}$ CONTROLLED)

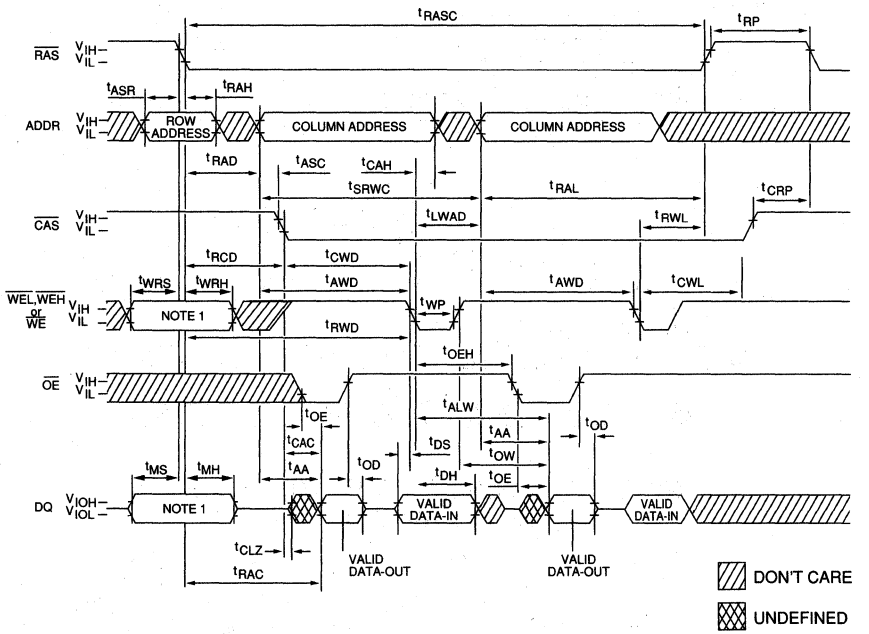


STATIC-COLUMN EARLY-WRITE CYCLE
($\overline{CAS}$ CONTROLLED)



NOTE: 1. Applies to MT4C1671 only; $\overline{WEL}$, $\overline{WEH}$ and DQ inputs on MT4C1670 are "don't care" at $\overline{RAS}$ time. $\overline{WE}$ selects between normal WRITE and MASKED WRITE at $\overline{RAS}$ time. The DQ inputs are "don't care" for a normal WRITE, $\overline{WE}$ HIGH at $\overline{RAS}$ time. The DQ inputs provide the mask data at $\overline{RAS}$ time for a MASKED WRITE, $\overline{WE}$ LOW at $\overline{RAS}$ time.

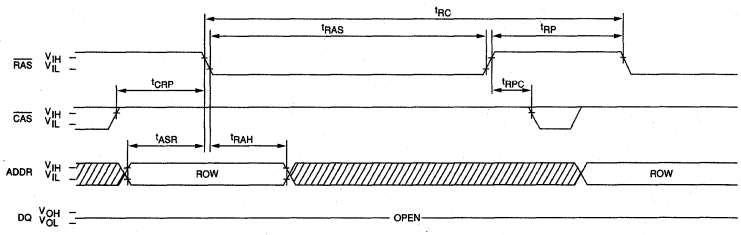
STATIC COLUMN READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)



NOTE: 1. Applies to MT4C1671 only; $\overline{WEL}$, $\overline{WEH}$ and DQ inputs on MT4C1670 are "don't care" at $\overline{RAS}$ time. $\overline{WE}$ selects between normal WRITE and MASKED WRITE at $\overline{RAS}$ time. The DQ inputs are "don't care" for a normal WRITE, $\overline{WE}$ HIGH at $\overline{RAS}$ time. The DQ inputs provide the mask data at $\overline{RAS}$ time for a MASKED WRITE, $\overline{WE}$ LOW at $\overline{RAS}$ time.

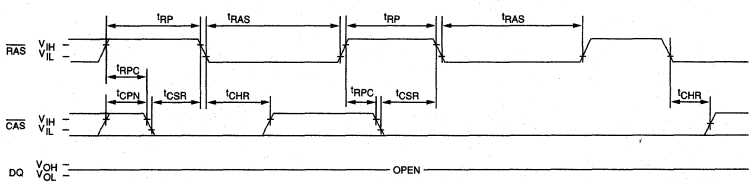
RAS-ONLY REFRESH CYCLE

(ADDR = A0-A7, OE; WEL, WEH or WE = DON'T CARE)



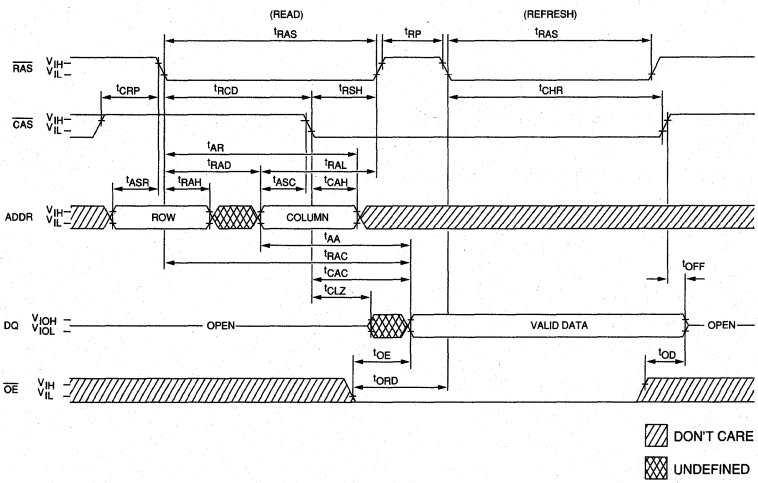
CAS-BEFORE-RAS REFRESH CYCLE

(A0-A7; WEL, WEH or WE,and OE = DON'T CARE)



HIDDEN REFRESH CYCLE [24]

(WEL, WEH or WE = HIGH; OE = LOW)



NEW ■ WIDE DRAM

DRAM

64K x 16 DRAM

STATIC COLUMN MODE, LOW POWER, EXTENDED REFRESH

FEATURES

- Industry standard x16 pinouts, timing, functions and packages
- High-performance, CMOS silicon-gate process
- Single +5V ±10% power supply
- All device pins are fully TTL compatible
- Refresh modes: $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$ ($\overline{CBR}$), HIDDEN and BATTERY BACKUP (BBU)
- Optional STATIC COLUMN MODE access cycle
- BYTE WRITE access cycle (MT4C1670 L only)
- NONPERSISTENT MASKED WRITE access cycle (MT4C1671 L only)
- 256 cycle extended refresh distributed across 32ms
- Low power, 1mW standby; 225mW active, typical

OPTIONS

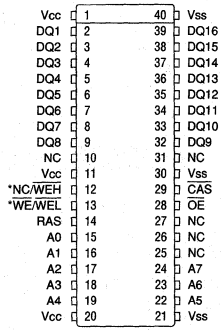
OPTIONS	MARKING
• Timing	
70ns access	- 7
80ns access	- 8
100ns access	-10
• Write Enable	
Byte or Word	MT4C1670 L
Word only	MT4C1671 L
• Mask Enable	
Not Available	MT4C1670 L
Always Available	MT4C1671 L
• Packages	
Plastic SOJ (400 mil)	DJ
Plastic TSOP (400 mil)	TG
Plastic ZIP (475 mil)	Z

NOTE: Available in die form Please consult factory for die data sheets.

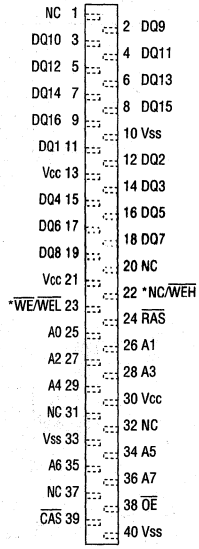
- Part Number Example: MT4C1670DJ-7 L

PIN ASSIGNMENT (Top View)

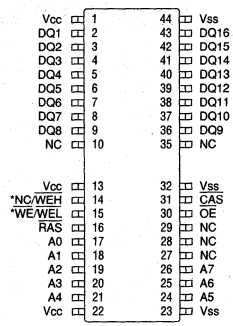
40-Pin SOJ (Q-6)



40-Pin Zip (O-4)



40-Pin TSOP (R-5)



*MT4C1671 L/MT4C1670 L

GENERAL DESCRIPTION

The MT4C1670/1 L are randomly accessed solid-state memories containing 1,048,576 bits organized in a x16 configuration. The MT4C1670 L has both BYTE and WORD WRITE access cycles while the MT4C1671 L has only WORD WRITE access cycles.

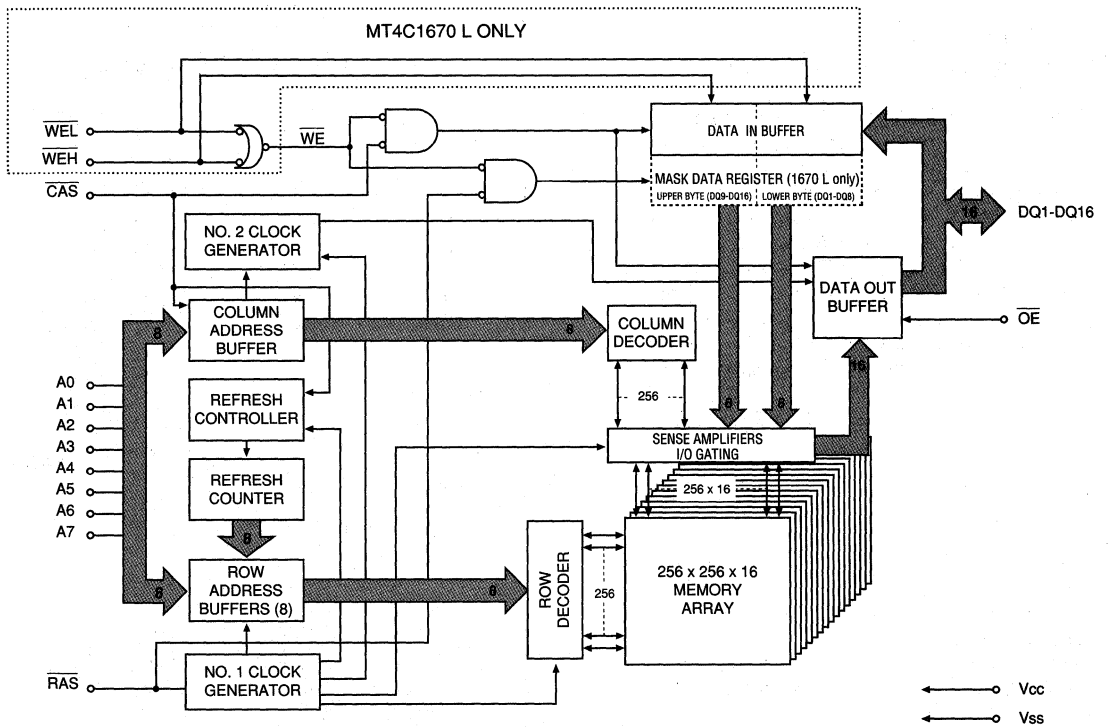
The MT4C1670 L functions in a similar manner to the MT4C1671 L except that replacing $\overline{WE}$ with $\overline{WEL}$ and $\overline{WEH}$ allows for BYTE WRITE access cycles. $\overline{WEL}$ and $\overline{WEH}$ function in an identical manner to $\overline{WE}$: either $\overline{WEL}$ or $\overline{WEH}$ will generate an internal $\overline{WE}$ through an AND gate (inverted NOR gate).

The MT4C1670 L "$\overline{WE}$" function and timing are determined by the first BYTE WRITE ($\overline{WEL}$ or $\overline{WEH}$) to transition LOW and the last to transition back HIGH. Use of only one of the two results in a BYTE WRITE cycle: $\overline{WEL}$ transitioning LOW selects a WRITE cycle for the lower byte (DQ1-DQ8) or $\overline{WEH}$ transitioning LOW selects a WRITE cycle for the upper byte (DQ9-DQ16).

The MT4C1671 L has NONPERSISTENT MASKED WRITE capability.

NEW ■ WIDE DRAM

FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTIONS

SOJ PIN NUMBERS	ZIP PIN NUMBERS	TSOP PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
14	24	16	$\overline{RAS}$	Input	ROW Address Strobe: $\overline{RAS}$ is used to clock-in the 8 row address bits and strobe the $\overline{WEL}$, $\overline{WEH}$ and DQ inputs for the MASKED WRITE function.
29	39	31	$\overline{CAS}$	Input	Column Address Strobe: $\overline{CAS}$ is used to clock-in the 8 column address bits, enable the DRAM output buffers, and strobe the data inputs on WRITE cycles.
28	38	30	$\overline{OE}$	Input	Output Enable: $\overline{OE}$ enables the output buffers when taken LOW during a READ access cycle. $\overline{RAS}$ and $\overline{CAS}$ must be LOW and $\overline{WEL}$ and $\overline{WEH}$ must be HIGH before $\overline{OE}$ will control the output buffers. Otherwise the output buffers are in a High-Z state.
13	23	15	$\overline{WE}$/$\overline{WEL}$*	Input	Write Enable Lower Byte: $\overline{WEL}$ on MT4C1670 L is $\overline{WE}$ control for the DQ1 through DQ8 inputs. $\overline{WE}$ on MT4C1671 L controls DQ1 through DQ16 inputs. If ($\overline{WEL}$ or $\overline{WEH}$)/$\overline{WE}$ is LOW, the access is a WRITE cycle. The DQ outputs for the byte not being written will remain in a High-Z state (byte WRITE cycle only).
12	22	14	NC/$\overline{WEH}$*	Input	Write Enable Upper Byte: $\overline{WEH}$ on MT4C1670 L is $\overline{WE}$ control for the DQ9 through DQ16 inputs. If ($\overline{WEL}$ or $\overline{WEH}$)/$\overline{WE}$ is LOW, the access is a WRITE cycle. This pin is a no connect on the MT4C1671 L as it has only WORD WRITE access cycles.
15-19, 22-24	25-29, 34-36	17-21, 24-26	A0-A7	Input	Address Inputs: These inputs are multiplexed and clocked by $\overline{RAS}$ and $\overline{CAS}$ to select one 16-bit word out of the 64K available words.
2-9, 32-39,	11, 12, 14-17, 2, 18, 19, 3-9	2-9, 36-43	DQ1-DQ16	Input/ Output	Data I/O: For WRITE cycles, DQ1-DQ16 act as inputs to the addressed DRAM location. BYTE WRITEs can be performed by using $\overline{WEL}$ or $\overline{WEH}$ to select the byte to be written. For READ access cycles, DQ1-DQ16 act as outputs for the addressed DRAM ocation. All 16 I/Os are active for READ cycles (there is no BYTE READ cycle).
10, 25, 26, 27, 31	1, 20, 31, 32, 37	13, 27-29, 35	NC	-	No Connect: These pins should be either left unconnected or tied to ground.
1, 11, 20	13, 21, 30	1, 13, 22	Vcc	Supply	Power Supply: +5V ± 10%
21, 30, 40	10, 33, 40	23, 32, 44	Vss	Supply	Ground

NOTE: *MT4C1671 L/MT4C1670 L

FUNCTIONAL DESCRIPTION

Each bit is uniquely addressed through the 16 address-bits during READ or WRITE cycles. These are entered 8 bits (A0-A7) at a time. $\overline{RAS}$ is used to latch the first 8 bits and $\overline{CAS}$ the latter 8 bits.

READ or WRITE cycles on the MT4C1671 L are selected with the $\overline{WE}$ input while either $\overline{WEL}$ or $\overline{WEH}$ perform the "$\overline{WE}$" on the MT4C1670 L. The MT4C1670 L "$\overline{WE}$" function is determined by the first BYTE WRITE ($\overline{WEL}$ or $\overline{WEH}$) to transition LOW and the last one to transition back HIGH.

A logic HIGH on $\overline{WE}$ dictates READ mode while a logic LOW on $\overline{WE}$ dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. Taking $\overline{WE}$ LOW will initiate a WRITE cycle, selecting DQ1 through DQ16. If $\overline{WE}$ goes LOW prior to $\overline{CAS}$ going LOW, the output pin(s) remain open (High-Z) until the next $\overline{CAS}$ cycle. If $\overline{WE}$ goes LOW after $\overline{CAS}$ goes LOW and data reaches the output pins, data out (Q) is activated and retains the selected cell data as long as $\overline{CAS}$ and $\overline{OE}$ remain LOW (regardless of $\overline{WE}$ or $\overline{RAS}$). This late $\overline{WE}$ pulse results in a READ-WRITE cycle.

The 16 data inputs and 16 data outputs are routed through 16 pins using common I/O, and pin direction is controlled by $\overline{OE}$, $\overline{WEL}$ and $\overline{WEH}$ (MT4C1670 L) or $\overline{WE}$ (MT4C1671 L).

STATIC COLUMN operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row address (A0-A7) defined page boundary. The STATIC COLUMN cycle is always initiated with a row address strobed-in by $\overline{RAS}$ followed by a column address strobed-in by $\overline{CAS}$. $\overline{CAS}$ may be toggled by holding $\overline{RAS}$ LOW and strobing-in different column addresses, thus executing faster memory cycles. Faster STATIC COLUMN WRITE cycles must have $\overline{CAS}$ or $\overline{WE}$ toggled strobing-in the different column addresses. Returning $\overline{RAS}$ HIGH terminates the STATIC COLUMN operation.

Returning $\overline{RAS}$ and $\overline{CAS}$ HIGH terminates a memory cycle and decreases chip current to a reduced standby level. The chip is also preconditioned for the next cycle during the $\overline{RAS}$ high time. Memory cell data is retained in its correct state by maintaining power and executing any $\overline{RAS}$ cycle (READ, WRITE, $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$, or HIDDEN refresh) so that all 256 combinations of $\overline{RAS}$ addresses (A0-A7) are executed at least every 32ms, regardless of sequence. The $\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh cycle will also invoke the refresh counter and controller for row address control.

BATTERY BACKUP MODE (BBU) is a CBR refresh performed at the extended refresh rate with CMOS input levels. This mode provides a very low current, data retention cycle. $\overline{RAS}$ must be clocked by an external source during the BBU MODE or "SLEEP MODE".

BYTE WRITE ACCESS CYCLE (MT4C1670 L ONLY)

The BYTE WRITE mode is determined by the use of $\overline{WEL}$ and $\overline{WEH}$. Enabling $\overline{WEL}$ will select a lower BYTE WRITE cycle (DQ1-DQ8) while Enabling $\overline{WEH}$ will select an upper BYTE WRITE (DQ9-DQ16). Enabling both $\overline{WEL}$ and $\overline{WEH}$ selects a WORD WRITE cycle.

The MT4C1670 L may be viewed as two 64K x 8 DRAMS, which have common input controls, with the exception of the WE input. Figure 1 illustrates the MT4C1670 L BYTE and WORD WRITE cycles.

MASKED WRITE DESCRIPTION (MT4C1671 L ONLY)

Every WRITE access cycle may be a MASKED WRITE, depending on the state of $\overline{WE}$ at $\overline{RAS}$ time. A MASKED WRITE is selected when mask data is supplied on the DQ pins and $\overline{WE}$ is LOW at $\overline{RAS}$ time. The MT4C1671 L is only word selectable when $\overline{WE}$ is LOW at $\overline{RAS}$ time (the MT4C1670 L does not have a MASKED WRITE cycle function).

The data (mask data) present on the DQ1-DQ16 inputs at $\overline{RAS}$ time will be written to an internal bit mask data register and will then act as an individual write enable for each of the corresponding DQ inputs. If a LOW (logic "0") is written to a mask data register bit, the input port for that bit is disabled during the subsequent WRITE operation and no new data will be written to that DRAM cell location. A HIGH (logic "1") on a mask data register bit enables the input port and allows normal WRITE operations to proceed. At $\overline{CAS}$ time, the bits present on the DQ1-DQ16 inputs will be written to the DRAM (if the mask data bit was HIGH) or ignored (if the mask data bit was LOW).

New mask data must be supplied each time a MASKED WRITE cycle is initiated, even if the previous cycle's mask was the same mask.

Figure 2 illustrates the MT4C1671 L MASKED WRITE operation (Note: $\overline{RAS}$ or $\overline{CAS}$ time refers to the time at which $\overline{RAS}$ or $\overline{CAS}$ transition from HIGH to LOW).

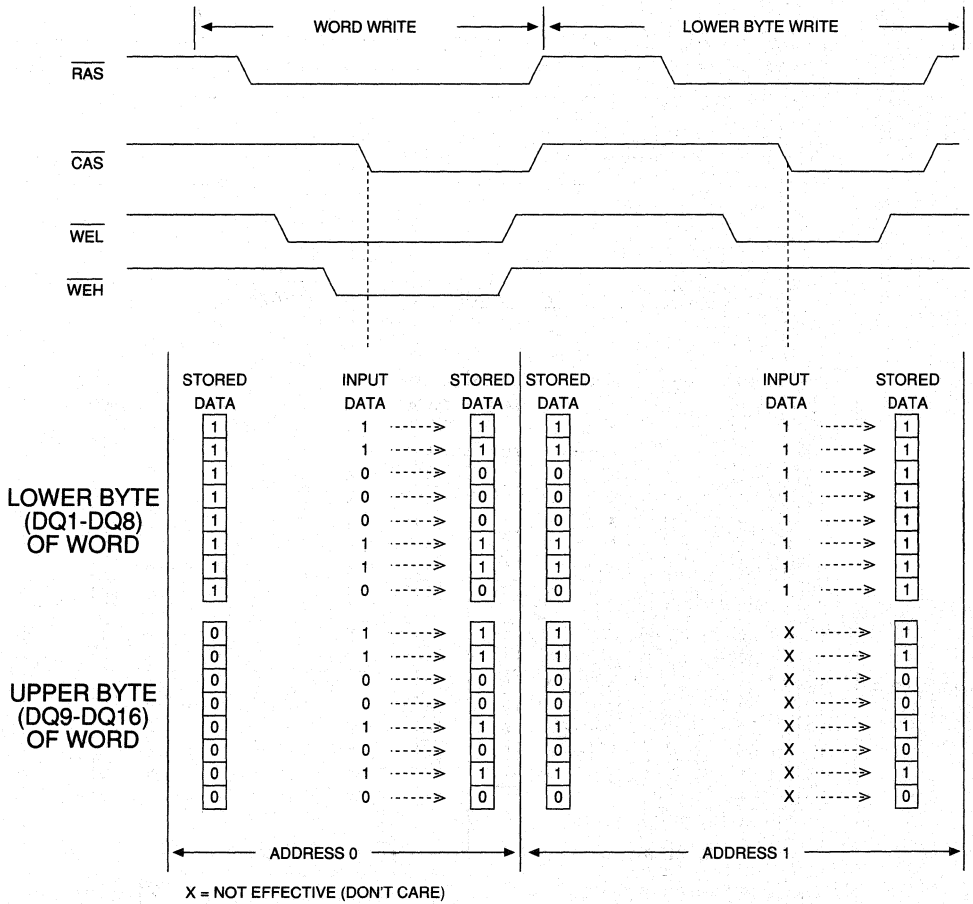


Figure 1
MT4C1670 L WORD AND BYTE WRITE EXAMPLE

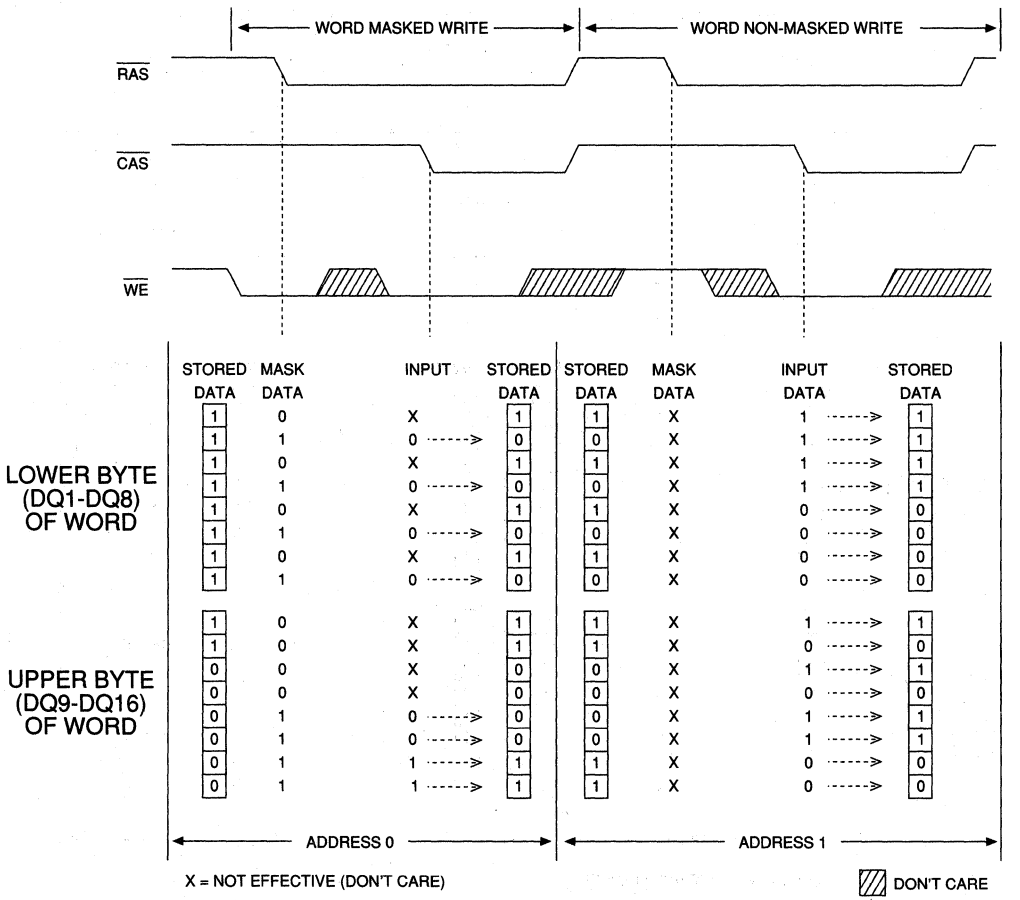


Figure 2
MT4C1671 L MASKED WRITE EXAMPLE

TRUTH TABLE: MT4C1670 L

FUNCTION		RAS	CAS	WEL	WEH	OE	ADDRESSES tR	ADDRESSES tC	DQs	NOTES
Standby		H	H→X	X	X	X	X	X	High-Z	
READ		L	L	H	H	L	ROW	COL	Data Out	
WRITE: WORD (EARLY-WRITE)		L	L	L	L	X	ROW	COL	Data In	
WRITE: LOWER BYTE (EARLY)		L	L	L	H	X	ROW	COL	Lower Byte, Data In Upper Byte, High-Z	
WRITE: UPPER BYTE (EARLY)		L	L	H	L	X	ROW	COL	Lower Byte, High-Z Upper Byte, Data In	
READ-WRITE		L	L	H→L	H→L	L→H	ROW	COL	Data Out, Data In	1
STATIC COLUMN	1st Cycle	L	L	H	H	L	ROW	COL	Data Out	
READ	2nd Cycle	L	L	H	H	L	n/a	COL	Data Out	
STATIC COLUMN	1st Cycle	L	L	L	L	X	ROW	COL	Data In	1
EARLY-WRITE	2nd Cycle	L	L	L	L	X	n/a	COL	Data In	1, 3
STATIC COLUMN	1st Cycle	L	L	H→L	H→L	L→H	ROW	COL	Data Out, Data In	1
READ-WRITE	2nd Cycle	L	L	H→L	H→L	L→H	n/a	COL	Data Out, Data In	1
HIDDEN	READ	L→H→L	L	H	H	L	ROW	COL	Data Out	
REFRESH	WRITE	L→H→L	L	L	L	X	ROW	COL	Data In	1, 2
RAS-ONLY REFRESH		L	H	X	X	X	ROW	n/a	High-Z	
CAS-BEFORE-RAS REFRESH		H→L	L	X	X	X	X	X	High-Z	
BATTERY BACKUP REFRESH		H→L	L	X	X	X	X	X	High-Z	

NOTE: 1. These cycles may also be BYTE WRITE cycles (either WEL or WEH active).
2. EARLY-WRITE only.
3. Either CAS or WEL / WEH must latch in each additional column address and input data.

NEW ■ WIDE DRAM

TRUTH TABLE: MT4C1671 L

FUNCTION		RAS	CAS	WE	OE	ADDRESSES tR	ADDRESSES tC	DQs	NOTES
Standby		H	H→X	X	X	X	X	High-Z	
READ		L	L	H	L	ROW	COL	Data Out	
WRITE: WORD (EARLY-WRITE)		L	L	L	X	ROW	COL	Data In	1
READ-WRITE		L	L	H→L	L→H	ROW	COL	Data Out, Data In	1
STATIC COLUMN	1st Cycle	L	L	H	L	ROW	COL	Data Out	
READ	2nd Cycle	L	L	H	L	n/a	COL	Data Out	
STATIC COLUMN	1st Cycle	L	L	L	X	ROW	COL	Data In	1
EARLY-WRITE	2nd Cycle	L	L	L	X	n/a	COL	Data In	1, 3
STATIC COLUMN	1st Cycle	L	L	H→L	L→H	ROW	COL	Data Out, Data In	1
READ-WRITE	2nd Cycle	L	L	H→L	L→H	n/a	COL	Data Out, Data In	1
HIDDEN	READ	L→H→L	L	H	L	ROW	COL	Data Out	
REFRESH	WRITE	L→H→L	L	L	X	ROW	COL	Data In	1, 2
RAS-ONLY REFRESH		L	H	X	X	ROW	n/a	High-Z	
CAS-BEFORE-RAS REFRESH		H→L	L	X	X	X	X	High-Z	
BATTERY BACKUP REFRESH		H→L	L	X	X	X	X	High-Z	

NOTE: 1. Data-in will be dependent on the mask provided. Refer to Figure 2.
2. EARLY-WRITE only.
3. Either CAS or WEL / WEH must latch in each additional column address and input data.

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} ..... -1.0V to +7.0V
Operating Temperature, T_A (Ambient) ..... 0°C to +70°C
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 3, 4, 6, 7) (0°C ≤ T_A ≤ 70°C; V_{CC} = 5V ± 10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.5	V	1
Input High (Logic 1) Voltage, All Inputs	V_{IH}	2.4	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, All Inputs	V_{IL}	-1.0	0.8	V	1
INPUT LEAKAGE CURRENT Any Input 0V ≤ V_{IN} ≤ V_{CC} (All other pins not under test = 0V)	I_I	-2	2	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled; 0V ≤ V_{OUT} ≤ 5.5V)	I_{OZ}	-10	10	µA	
OUTPUT LEVELS Output High Voltage (I_{OUT} = -2.5mA)	V_{OH}	2.4		V	
Output Low Voltage (I_{OUT} = 2.1mA)	V_{OL}		0.4	V	

PARAMETER/CONDITION	SYMBOL	MAX -7	MAX -8	MAX -10	UNITS	NOTES
STANDBY CURRENT: (TTL) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC1}	2	2	2	mA	
STANDBY CURRENT: (CMOS) ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} -0.2V)	I_{CC2}	300	300	300	µA	25
OPERATING CURRENT: Random READ/WRITE Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC (MIN))	I_{CC3}	120	115	90	mA	3, 4, 31
OPERATING CURRENT: STATIC COLUMN Average power supply current ($\overline{RAS}$ = V_{IL}; $\overline{CAS}$, Address Cycling: ^tSC = ^tSC (MIN))	I_{CC4}	110	95	80	mA	3, 4, 31
REFRESH CURRENT: $\overline{RAS}$-ONLY Average power supply current ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}: ^tRC = ^tRC (MIN))	I_{CC5}	120	115	90	mA	3, 31
REFRESH CURRENT: $\overline{CAS}$-BEFORE-$\overline{RAS}$ (CBR) Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC (MIN))	I_{CC6}	120	115	90	mA	3, 5
REFRESH CURRENT: BATTERY BACKUP (BBU) Average power supply current during BATTERY BACKUP refresh: $\overline{CAS}$ 0.2V or $\overline{CAS}$-BEFORE-$\overline{RAS}$ cycling; $\overline{RAS}$ = ^tRAS (MIN) to 1,000ns; $\overline{WE}$, A0-A9 and D_{IN} = V_{CC} - 0.2V or 0.2V (D_{IN} may be left open), ^tRC = 125µs (1,024 rows at 125µs = 128ms)	I_{CC7}	400	400	400	µA	3, 5, 28

CAPACITANCE

(Note: 2)

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A7	C_{I1}		5	pF	2
Input Capacitance: $\overline{RAS}$, $\overline{CAS}$,($\overline{WEL}$, $\overline{WEH}$)/ $\overline{WE}$, $\overline{OE}$	C_{I2}		7	pF	2
Input/Output Capacitance: DQ	C_{IO}		7	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13, 23) (0°C ≤ T_A ≤ +70°C; V_{CC} = 5V ± 10%)

AC CHARACTERISTICS		-7		-8		-10			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	t_{RC}	130		150		180		ns	
READ-WRITE cycle time	t_{RWC}	175		185		220		ns	
STATIC-COLUMN READ or WRITE cycle time	t_{SC}	45		50		55		ns	
STATIC-COLUMN READ-WRITE cycle time	t_{SRWC}	95		100		120		ns	
Access time from $\overline{RAS}$	t_{RAC}		70		80		100	ns	14
Access time from $\overline{CAS}$	t_{CAC}		25		35		40	ns	15
Output Enable time	t_{OE}		25		35		40	ns	
Access time from column address	t_{AA}		40		45		55	ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		45		50		55	ns	
$\overline{RAS}$ pulse width	t_{RAS}	70	100,000	80	100,000	100	100,000	ns	
$\overline{RAS}$ pulse width (STATIC COLUMN)	t_{RASC}	70	100,000	80	100,000	100	100,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	20		35		40		ns	
$\overline{RAS}$ precharge time	t_{RP}	50		60		70		ns	
$\overline{CAS}$ pulse width	t_{CAS}	25	100,000	35	100,000	40	100,000	ns	
$\overline{CAS}$ hold time	t_{CSH}	70		80		100		ns	
$\overline{CAS}$ precharge time	t_{CPN}	10		10		15		ns	16
$\overline{CAS}$ precharge time (STATIC COLUMN)	t_{CP}	10		10		10		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	45	20	45	25	60	ns	17
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		10		10		ns	
Row address setup time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	10		12		15		ns	
$\overline{RAS}$ to column address delay time	t_{RAD}	15	35	17	40	20	55	ns	18
Column address setup time	t_{ASC}	0		0		0		ns	
Column address hold time	t_{CAH}	15		15		20		ns	
Column address hold time (referenced to $\overline{RAS}$)	t_{AR}	55		60		70		ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	35		45		55		ns	
Read command setup time	t_{RCS}	0		0		0		ns	26
Read command hold time (referenced to $\overline{CAS}$)	t_{RCH}	0		0		0		ns	19, 26
Read command hold time (referenced to $\overline{RAS}$)	t_{RRH}	0		10		10		ns	19
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	0		0		0		ns	
Output buffer turn-off delay	t_{OFF}	0	20	0	20	0	20	ns	20, 30

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

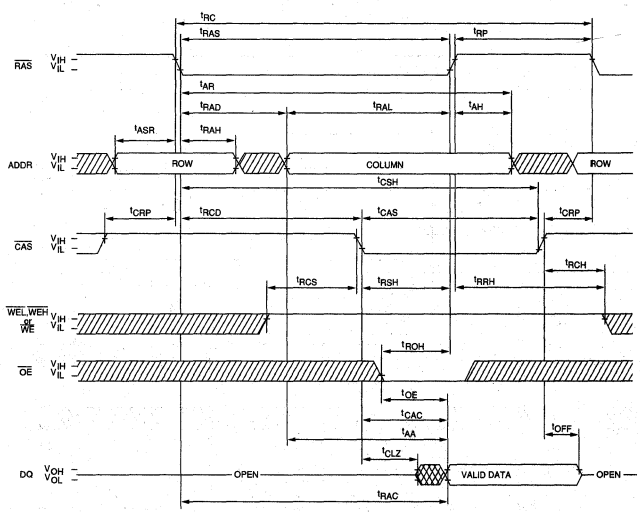
(Notes: 6, 7, 8, 9, 10, 11, 12, 13, 23) ($0°C \le T_A \le +70°C$; $V_{CC} = 5V \pm 10\%$)

AC CHARACTERISTICS		-7		-8		-10			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Output Disable time	^tOD		15		20		20	ns	30
Write command setup time	^tWCS	0		0		0		ns	21, 26
Write command hold time	^tWCH	15		15		20		ns	26
Write command hold time (referenced to $\overline{RAS}$)	^tWCR	50		60		70		ns	26
Write command pulse width	^tWP	15		15		20		ns	26
Write command to $\overline{RAS}$ lead time	^tRWL	20		35		40		ns	26
Write command to $\overline{CAS}$ lead time	^tCWL	20		35		40		ns	26
Data-in setup time	^tDS	0		0		0		ns	22
Data-in hold time	^tDH	15		15		20		ns	22
Data-in hold time (referenced to $\overline{RAS}$)	^tDHR	50		60		70		ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	^tRWD	90		100		125		ns	21
Column address to $\overline{WE}$ delay time	^tAWD	65		70		80		ns	21
$\overline{CAS}$ to $\overline{WE}$ delay time	^tCWD	50		55		70		ns	21
Transition time (rise or fall)	^tT	3	50	3	50	3	50	ns	9, 10
Refresh period (256 cycles)	^tREF		32		32		32	ms	28
$\overline{RAS}$ to $\overline{CAS}$ precharge time	^tRPC	0		10		10		ns	
$\overline{CAS}$ setup time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tCSR	10		10		10		ns	5
$\overline{CAS}$ hold time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tCHR	15		25		30		ns	5
MASKED WRITE command to $\overline{RAS}$ setup time	^tWRS	0		0		0		ns	26, 27
MASKED WRITE command to $\overline{RAS}$ hold time	^tWRH	15		15		15		ns	26, 27
Mask data to $\overline{RAS}$ setup time	^tMS	0		0		0		ns	26
Mask data to $\overline{RAS}$ hold time	^tMH	15		15		15		ns	26
$\overline{OE}$ hold time from $\overline{WE}$ during READ-MODIFY-WRITE cycle	^tOEH	10		20		20		ns	29
$\overline{OE}$ setup prior to $\overline{RAS}$ during HIDDEN REFRESH cycle	^tORD	0		0		0		ns	
Last WRITE to column address delay	^tLWAD	20	30	20	35	25	45	ns	
Access time from last WRITE	^tALW	65		75		95		ns	
Output data enable from WRITE	^tOW	^tAA		^tAA		^tAA		ns	
Output data hold time from column address	^tAOH	5		5		5		ns	
$\overline{RAS}$ hold time referenced to $\overline{OE}$	^tROH	10		10		10		ns	
Column address hold time referenced to $\overline{RAS}$ HIGH	^tAH	5		5		10		ns	
$\overline{CAS}$ pulse width in STATIC-COLUMN mode	^tCSC	^tCAS		^tCAS		^tCAS		ns	
Write command inactive time	^tWI	10		10		10		ns	

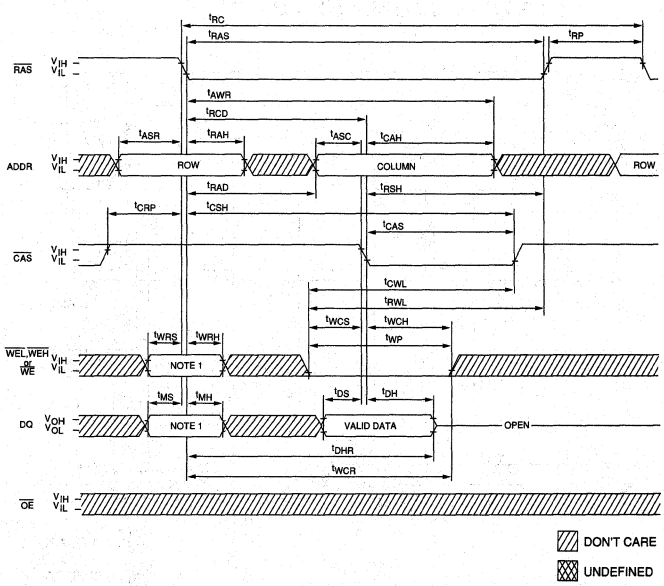
NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. Vcc = 5V ±10%, f = 1 MHz.
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \le T_A \le 70°C$) is assured.
7. An initial pause of 100µs is required after power-up followed by any eight $\overline{RAS}$ cycles before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-up should be repeated any time the 4ms refresh requirement is exceeded.
8. AC characteristics assume ^tT = 5ns.
9. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS}$ = V_{IH}, data output is High-Z.
12. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to 1 TTL gates and 50pF.
14. Assumes that $^tRCD < {}^tRCD$ (MAX). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
15. Assumes that $^tRCD \ge {}^tRCD$ (MAX).
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, data out (Q) will be maintained from the previous cycle. To initiate a new cycle and clear the Q buffer, $\overline{CAS}$ must be pulsed HIGH for ^tCPN.
17. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (MAX) limit, then access time is controlled exclusively by ^tCAC.
18. Operation within the ^tRAD (MAX) limit ensures that ^tRCD (MAX) can be met. ^tRAD (MAX) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (MAX) limit, then access time is controlled exclusively by ^tAA.
19. Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
20. ^tOFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
21. ^tWCS, ^tRWD, ^tAWD and ^tCWD are restrictive operating parameters in LATE-WRITE and READ-MODIFY-WRITE cycles only. If $^tWCS \ge {}^tWCS$ (MIN), the cycle is an EARLY-WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If $^tRWD \ge {}^tRWD$ (MIN), $^tAWD \ge {}^tAWD$ (MIN) and $^tCWD \ge {}^tCWD$ (MIN), the cycle is a LATE-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions are met, the state of data out are indeterminate. $\overline{OE}$ held HIGH and $\overline{WE}$ taken LOW after $\overline{CAS}$ goes LOW results in a LATE-WRITE ($\overline{OE}$ controlled) cycle.
22. These parameters are referenced to $\overline{CAS}$ leading edge in early WRITE cycles and $\overline{WE}$ leading edge in LATE-WRITE or READ-MODIFY-WRITE cycles.
23. If $\overline{OE}$ is tied permanently LOW, LATE-WRITE or READ-MODIFY-WRITE operations are not possible.
24. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case $\overline{WE}$ = LOW and $\overline{OE}$=HIGH.
25. All other inputs at Vcc -0.2V.
26. WRITE command is defined as either $\overline{WEL}$ or $\overline{WEH}$ or both going LOW on the MT4C1670 L. WRITE command is defined as $\overline{WE}$ going LOW on the MT4C1671 L.
27. Must be held LOW to ensure MASKED WRITE is enabled and must be held HIGH to ensure MASKED WRITE is disabled.
28. BBU current is reduced as ^tRAS is reduced from its maximum specification during the BBU cycle.
29. LATE-WRITE and READ-MODIFY-WRITE cycles must have both ^tOD and ^tOEH met ($\overline{OE}$ HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. The DQs will provide the previously read data if $\overline{CAS}$ remains LOW and $\overline{OE}$ is taken back LOW after ^tOEH is met. If $\overline{CAS}$ goes HIGH prior to $\overline{OE}$ going back LOW, the DQs will remain open.
30. The DQs open during READ cycles once ^tOD or ^tOFF occur. If $\overline{CAS}$ goes HIGH first, $\overline{OE}$ becomes a "don't care." If $\overline{OE}$ goes HIGH and $\overline{CAS}$ stays LOW, $\overline{OE}$ is not a "don't care;" and the DQs will provide the previously read data if $\overline{OE}$ is taken back LOW (while $\overline{CAS}$ remains LOW).
31. Column address changed once while $\overline{RAS}$ = V_{IL} and $\overline{CAS}$ = V_{IH}.

READ CYCLE



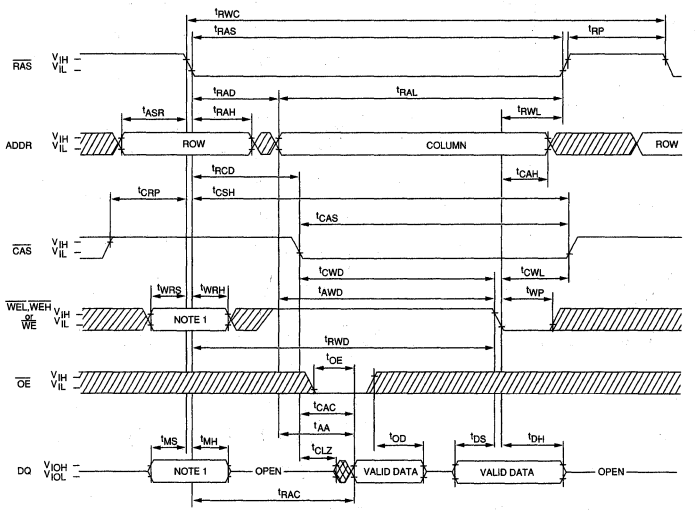
EARLY-WRITE CYCLE



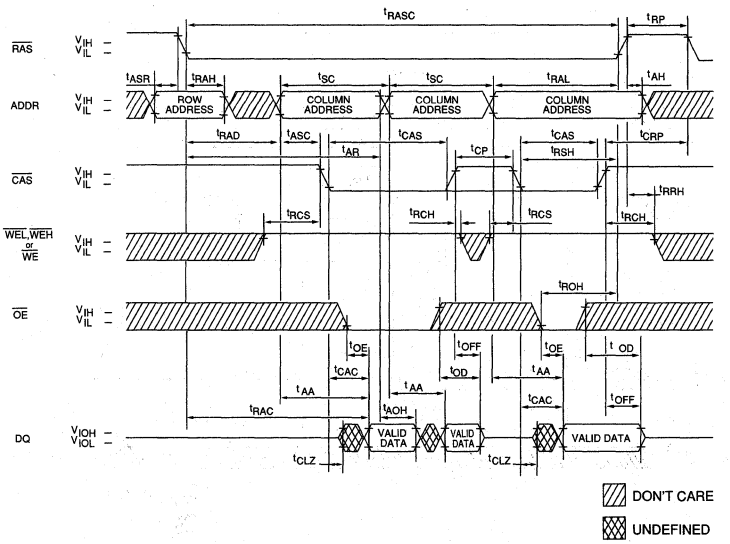
NOTE: 1. Applies to MT4C1671 L only; $\overline{WEL}$, $\overline{WEH}$ and DQ inputs on MT4C1670 L are "don't care" at $\overline{RAS}$ time. $\overline{WE}$ selects between normal WRITE and MASKED WRITE at $\overline{RAS}$ time. The DQ inputs are "don't care" for a normal WRITE, $\overline{WE}$ HIGH at $\overline{RAS}$ time. The DQ inputs provide the mask data at $\overline{RAS}$ time for a MASKED WRITE, $\overline{WE}$ LOW at $\overline{RAS}$ time.

NEW ■ WIDE DRAM

READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)



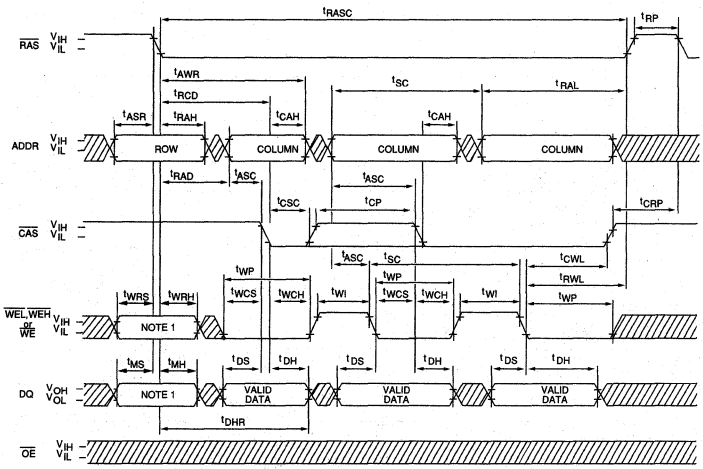
STATIC-COLUMN READ CYCLE



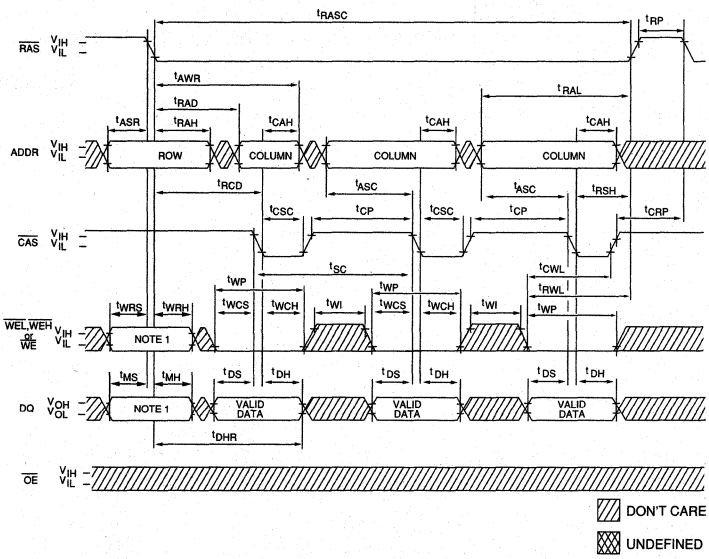
NOTE: 1. Applies to MT4C1671 L only; $\overline{WEL}$, $\overline{WEH}$ and DQ inputs on MT4C1670 L are "don't care" at $\overline{RAS}$ time. $\overline{WE}$ selects between normal WRITE and MASKED WRITE at $\overline{RAS}$ time. The DQ inputs are "don't care" for a normal WRITE, $\overline{WE}$ HIGH at $\overline{RAS}$ time. The DQ inputs provide the mask data at $\overline{RAS}$ time for a MASKED WRITE, $\overline{WE}$ LOW at $\overline{RAS}$ time.

NEW ■ WIDE DRAM

STATIC-COLUMN EARLY-WRITE CYCLE
($\overline{WE}$ CONTROLLED)



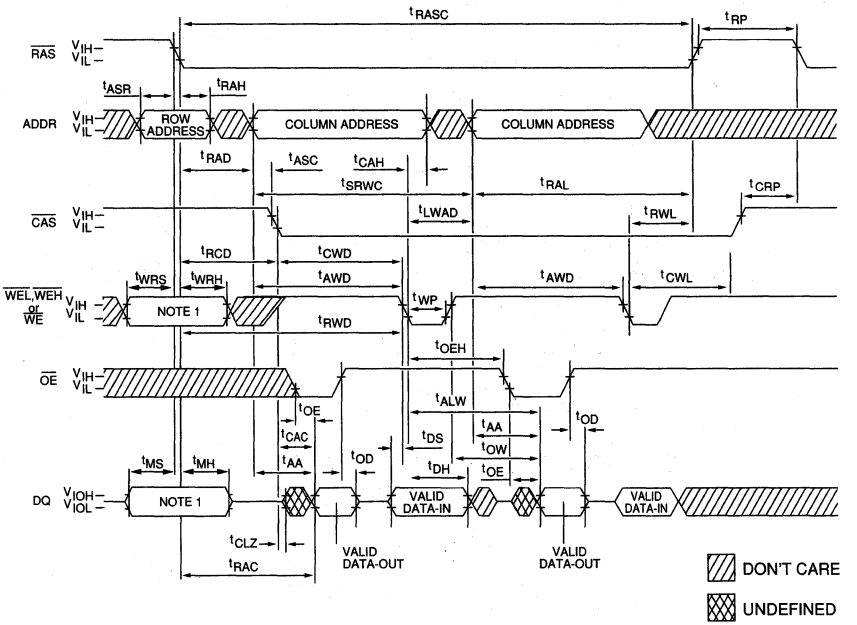
STATIC-COLUMN EARLY-WRITE CYCLE
($\overline{CAS}$ CONTROLLED)



NOTE: 1. Applies to MT4C1671 L only; $\overline{WEL}$, $\overline{WEH}$ and DQ inputs on MT4C1670 L are "don't care" at $\overline{RAS}$ time. $\overline{WE}$ selects between normal WRITE and MASKED WRITE at $\overline{RAS}$ time. The DQ inputs are "don't care" for a normal WRITE, $\overline{WE}$ HIGH at $\overline{RAS}$ time. The DQ inputs provide the mask data at $\overline{RAS}$ time for a MASKED WRITE, $\overline{WE}$ LOW at $\overline{RAS}$ time.

NEW ■ WIDE DRAM

STATIC-COLUMN READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)

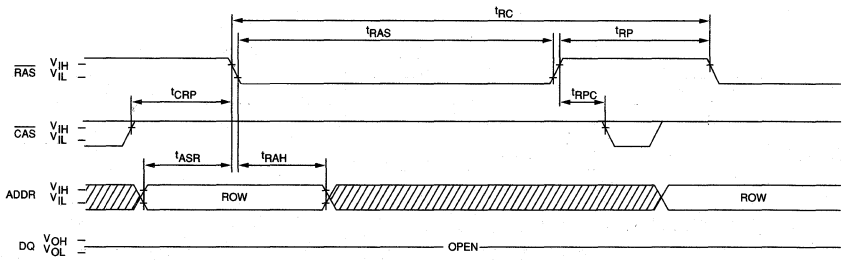


NOTE: 1. Applies to MT4C1671 L only; $\overline{WEL}$, $\overline{WEH}$ and DQ inputs on MT4C1670 L are "don't care" at $\overline{RAS}$ time. $\overline{WE}$ selects between normal WRITE and MASKED WRITE at $\overline{RAS}$ time. The DQ inputs are "don't care" for a normal WRITE, $\overline{WE}$ HIGH at $\overline{RAS}$ time. The DQ inputs provide the mask data at $\overline{RAS}$ time for a MASKED WRITE, $\overline{WE}$ LOW at $\overline{RAS}$ time.

NEW ■ WIDE DRAM

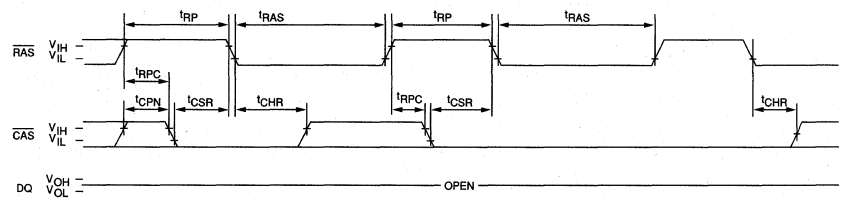
RAS-ONLY REFRESH CYCLE

(ADDR = A0-A7, OE; WEL, WEH or WE = DON'T CARE)



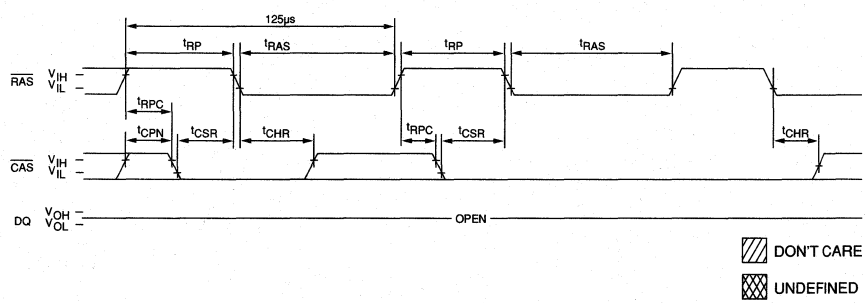
CAS-BEFORE-RAS REFRESH CYCLE

(A0-A7; WEL, WEH or WE, and OE = DON'T CARE)



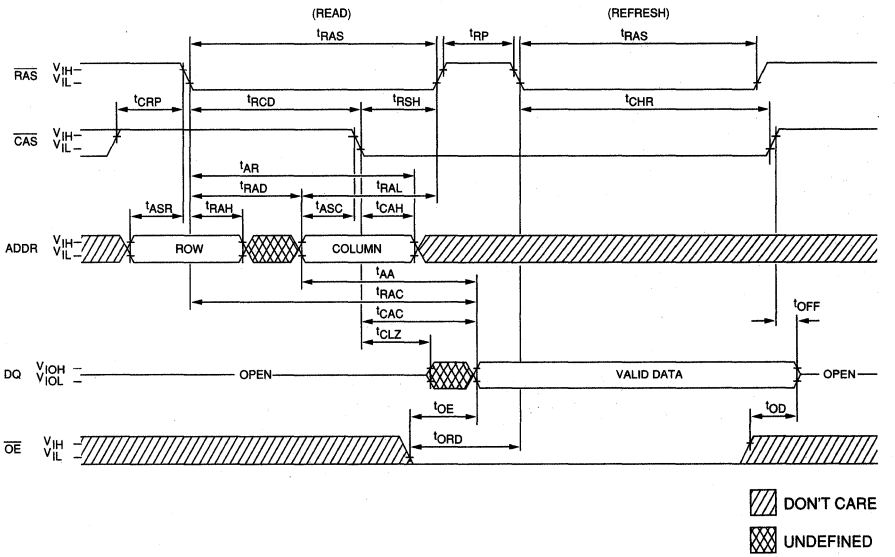
BATTERY BACKUP REFRESH CYCLE

(A0-A7; WEL, WEH or WE, and OE = DON'T CARE)



NEW ■ WIDE DRAM

HIDDEN REFRESH CYCLE [24]
($\overline{WEL}$, $\overline{WEH}$ or $\overline{WE}$ = HIGH; $\overline{OE}$ = LOW)



DRAM

256K x 16 DRAM

FAST PAGE MODE

FEATURES

- Industry standard x16 pinouts, timing, functions and packages
- High-performance, CMOS silicon-gate process
- Single +5V ±10% power supply
- Low power, 3mW standby; 500mW active, typical
- All device pins are fully TTL compatible
- 512 cycle refresh in 8ms (9 rows and 9 columns)
- Refresh modes: RAS-ONLY, CAS-BEFORE-RAS and HIDDEN
- Optional FAST PAGE MODE access cycle
- BYTE WRITE access cycle
- BYTE READ access cycle (MT4C16257/9 only)
- NONPERSISTENT MASKED WRITE access cycle (MT4C16258/9 only)

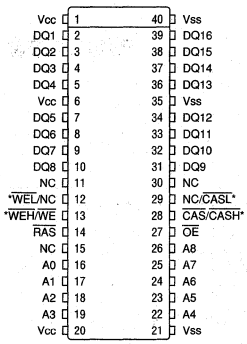
OPTIONS

	MARKING
• Timing	
70ns access	- 7
80ns access	- 8
100ns access	-10
• Write Cycle Access	
BYTE or WORD via WE (non-maskable)	MT4C16256
BYTE or WORD via CAS (non-maskable)	MT4C16257
BYTE or WORD via WE (maskable)	MT4C16258
BYTE or WORD via CAS (maskable)	MT4C16259
• Packages	
Plastic SOJ (400 mil)	DJ
Plastic TSOP (400 mil)	TG
Plastic ZIP (475 mil)	Z

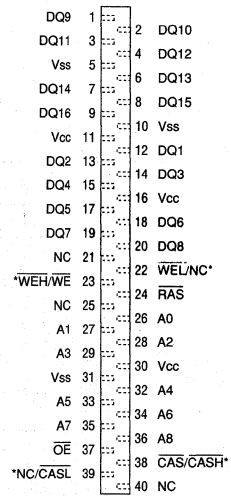
NOTE: Available in die form. Please consult factory for die data sheets.

PIN ASSIGNMENT (Top View)

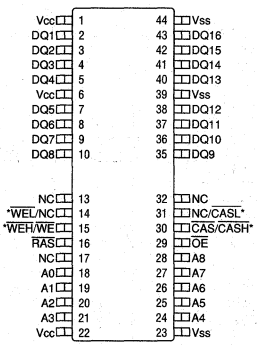
40-Pin SOJ (Q-6)



40-Pin ZIP (O-4)



40-Pin TSOP (R-5)



*MT4C16256/8 / MT4C16257/9

GENERAL DESCRIPTION

The MT4C16256/7/8/9 are randomly accessed solid-state memories containing 4,194,304 bits organized in a x16 configuration. The MT4C16256 and MT4C16258 have both BYTE WRITE and WORD WRITE access cycles via two write enable pins. The MT4C16257 and MT4C16259 have both BYTE WRITE and WORD WRITE access cycles via two CAS pins. The MT4C16258 and MT4C16259 are also able to perform WRITE-PER-BIT accesses.

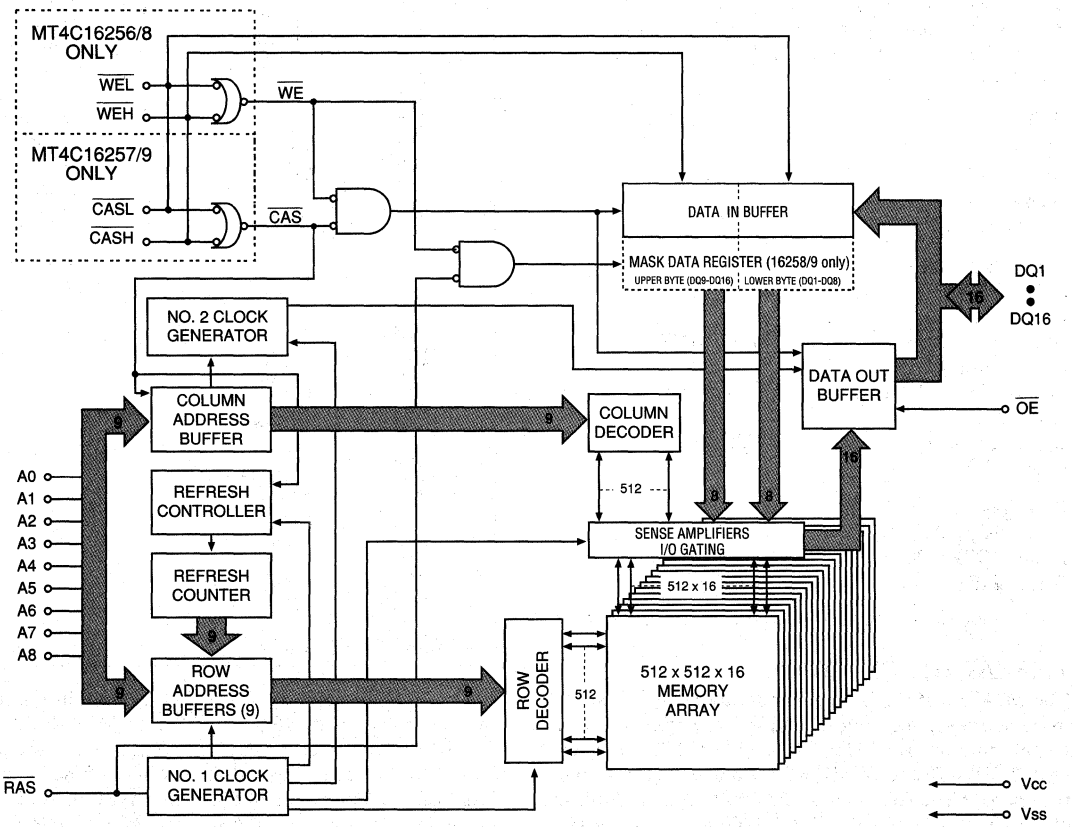
The MT4C16256 and MT4C16257 function in the same manner except that WEL and WEH on MT4C16256 and CASL and CASH on MT4C16257 control the selection of byte WRITE access cycles. WEL and WEH function in an identical manner to WE in that either WEL or WEH will generate an internal WE. CASL and CASH function in an identical manner to CAS in that either CASL or CASH will generate an internal CAS.

The MT4C16256 "$\overline{WE}$" function and timing are determined by the first $\overline{WE}$ ($\overline{WEL}$ or $\overline{WEH}$) to transition LOW and by the last to transition back HIGH. Use of only one of the two results in a BYTE WRITE cycle. $\overline{WEL}$ transitioning LOW selects a WRITE cycle for the lower byte (DQ1-DQ8) and $\overline{WEH}$ transitioning LOW selects a WRITE cycle for the upper byte (DQ9-DQ16).

The MT4C16257 "$\overline{CAS}$" function and timing are determined by the first $\overline{CAS}$ ($\overline{CASL}$ or $\overline{CASH}$)to transition LOW and by the last to transition back HIGH. Use of only one of the two results in a BYTE WRITE cycle. $\overline{CASL}$ transitioning LOW selects a WRITE cycle for the lower byte (DQ1-DQ8) and $\overline{CASH}$ transitioning LOW selects a WRITE cycle for the upper byte (DQ9-DQ16). BYTE READ cycles are achieved through $\overline{CASL}$ or $\overline{CASH}$ in the same manner during READ cycles for the MT4C16257.

The MT4C16258 and MT4C16259 function in the same manner as MT4C16256 and MT4C16257, respectively; and they have NONPERSISTENT MASKED WRITE cycles capabilities. This option allows the MT4C16258 and MT4C16259 to operate with either normal WRITE cycles or with NONPERSISTENT MASKED WRITE cycles.

FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTIONS

SOJ PINS	TSOP PINS	ZIP PINS	SYMBOL	TYPE	DESCRIPTION
14	16	24	$\overline{RAS}$	Input	ROW Address Strobe: $\overline{RAS}$ is used to latch in the 9 row-address bits and strobe the $\overline{WE}$ and DQs on the MASKED WRITE option (MT4C16258 and MT4C16259 only).
28	30	38	$\overline{CAS}$/ $\overline{CASH}$	Input	Column Address Strobe: $\overline{CAS}$ (MT4C16256/8) is used to latch-in the 9 column-address bits and enable the DRAM output buffers, and strobe the data inputs on WRITE cycles. $\overline{CAS}$ controls DQ1 through DQ16. Column Address Strobe Upper Byte: $\overline{CASH}$ (MT4C16257/9) is the $\overline{CAS}$ control for DQ9 through DQ16. The DQs for the byte not being accessed will remain in a High-Z (high impedance) state during either a READ or a WRITE access cycle.
27	29	37	$\overline{OE}$	Input	Output Enable: $\overline{OE}$ enables the output buffers when taken LOW during a READ access cycle. $\overline{RAS}$ and $\overline{CAS}$ (MT4C16256/8) or $\overline{CASL}$ / $\overline{CASH}$ (MT4C16257/9) must be LOW and $\overline{WEL}$ / $\overline{WEH}$ (MT4C16256/8) or $\overline{WE}$ (MT4C16257/9) must be HIGH before $\overline{OE}$ will control the output buffers. Otherwise, the output buffers are in a High-Z state.
13	15	23	$\overline{WEH}$/$\overline{WE}$	Input	Write Enable Upper Byte: $\overline{WEH}$ (MT4C16256/8) is $\overline{WE}$ control for the DQ9 through DQ16 inputs. If $\overline{WE}$ or $\overline{WEH}$ is LOW, the access is a WRITE cycle. If either $\overline{WE}$ or $\overline{WEH}$ is LOW at $\overline{RAS}$ time on MT4C16258, then it is also a MASKED WRITE cycle. The DQs for the byte not being written will remain in a High-Z state (BYTE WRITE cycle only). Write Enable: $\overline{WE}$ (MT4C16257/9) controls DQ1 through DQ16inputs. If $\overline{WE}$ is LOW, the access is a WRITE cycle. The MT4C16258/9 also use $\overline{WE}$ to enable the MASK register during $\overline{RAS}$ time.
12	14	22	$\overline{WEL}$/NC	Input	Write Enable Lower Byte: $\overline{WEL}$ (MT4C16256/8) is the $\overline{WE}$ control for DQ1 through DQ8 inputs. If $\overline{WEL}$ is LOW, the access is a WRITE cycle. If $\overline{WEL}$ is LOW at $\overline{RAS}$ time on MT4C16258, then it is also a MASKED WRITE cycle. The DQs for the byte not being written will remain in a High-Z state (BYTE WRITE cycle only).
29	31	39	NC/$\overline{CASL}$	Input	Column Address Strobe Low Byte: $\overline{CASL}$ (MT4C16257/9) is the $\overline{CAS}$ control for DQ1 through DQ8. The DQs for the byte not being accessed will remain in a High-Z state during either a READ or a WRITE access cycle.
16-19, 22-26	18-21, 24-28	26-29, 32-36	A0-A8	Input	Address Inputs: These inputs are multiplexed and clocked by $\overline{RAS}$ and $\overline{CAS}$ (or $\overline{CASL}$ / $\overline{CASH}$) to select one 16-bit word (or 8-bit byte) out of the 256K available words.

PIN DESCRIPTIONS (continued)

SOJ PINS	TSOP PINS	ZIP PINS	SYMBOL	TYPE	DESCRIPTION
2-5, 7-10, 31-34, 36-39	2-5, 7-10, 35-38, 40-43	12-15, 17-20, 1-4, 6-9	DQ1-DQ16	Input/ Output	Data I/O: For WRITE cycles, DQ1-DQ16 act as inputs to the addressed DRAM location. BYTE WRITEs can be performed by using $\overline{WEL}$ / $\overline{WEH}$ (MT4C16256/8) or $\overline{CASL}$ / $\overline{CASH}$ (MT4C16257/8) to select the byte to be written. For READ access cycles, DQ1-DQ16 act as outputs for the addressed DRAM Location. All sixteen I/Os are active for READ cycles (MT4C16256/8). The MT4C16257/9 allow for BYTE READ cycles.
11, 15, 30	13, 17	21, 25, 40	NC	-	No Connect: These pins should be either left unconnected or tied to ground.
1, 6, 20	1, 6, 22	11, 16, 30	Vcc	Supply	Power Supply: +5V ±10%
21, 35, 40	23, 39, 44	5, 10, 31	Vss	Supply	Ground

FUNCTIONAL DESCRIPTION

Each bit is uniquely addressed through the 18 address bits during READ or WRITE cycles. These are entered 9 bits (A0-A8) at a time. $\overline{RAS}$ is used to latch the first 9 bits and $\overline{CAS}$ the latter 9 bits.

The $\overline{CAS}$ control also determines whether the cycle will be a refresh cycle ($\overline{RAS}$-ONLY) or an active cycle (READ, WRITE or READ-WRITE) once $\overline{RAS}$ goes LOW. The MT4C16256 and MT4C16258 each have one $\overline{CAS}$ control while the MT4C16257 and MT4C16259 have two: $\overline{CASL}$ and $\overline{CASH}$.

The $\overline{CASL}$ and $\overline{CASH}$ inputs internally generate a $\overline{CAS}$ signal functioning in an identical manner to the single $\overline{CAS}$ input on the other 256K x 16 DRAMs. The key difference is each $\overline{CAS}$ controls its corresponding DQ tristate logic (in conjunction with $\overline{OE}$ and $\overline{WE}$). $\overline{CASL}$ controls DQ1 through DQ8, and $\overline{CASH}$ controls DQ9 through DQ16.

The MT4C16257 and MT4C16259 "$\overline{CAS}$" function is determined by the first $\overline{CAS}$ ($\overline{CASL}$ or $\overline{CASH}$) to transition LOW and the last one to transition back HIGH. The two $\overline{CAS}$ controls give the MT4C16257 and MT4C16259 both byte READ and byte WRITE cycle capabilities.

READ or WRITE cycles on the MT4C16257 or MT4C16259 are selected with the $\overline{WE}$ input while either $\overline{WEL}$ or $\overline{WEH}$ perform the "$\overline{WE}$" on the MT4C16256 or MT4C16258. The MT4C16256 and MT4C16258 "$\overline{WE}$" function is determined by the first BYTE WRITE ($\overline{WEL}$ or $\overline{WEH}$) to transition LOW and the last one to transition back HIGH.

A logic HIGH on $\overline{WE}$ dictates READ mode while a logic LOW on $\overline{WE}$ dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. Taking $\overline{WE}$ LOW will initiate a WRITE cycle, selecting DQ1 through DQ16. If $\overline{WE}$ goes LOW prior to $\overline{CAS}$ going LOW, the output pin(s) remain open (High- Z) until the next $\overline{CAS}$ cycle. If $\overline{WE}$ goes LOW after $\overline{CAS}$ goes LOW and data reaches the output pins, data out (Q) is activated and retains the selected cell data as long as $\overline{CAS}$ and $\overline{OE}$ remain LOW (regardless of $\overline{WE}$ or $\overline{RAS}$). This late $\overline{WE}$ pulse results in a READ-WRITE cycle.

The 16 data inputs and 16 data outputs are routed through 16 pins using common I/O, and pin direction is controlled by $\overline{OE}$, $\overline{WEL}$ and $\overline{WEH}$ (MT4C16256 and MT4C16258) or $\overline{WE}$ (MT4C16257 and MT4C16259).

FAST PAGE MODE operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row address (A0-A8) defined page boundary. The FAST PAGE MODE cycle is always initiated with a row address strobed-in by $\overline{RAS}$ followed by a column address strobed-in by $\overline{CAS}$. $\overline{CAS}$ may be toggled by holding $\overline{RAS}$ LOW and strobing-in different column addresses, thus executing faster memory cycles. Returning $\overline{RAS}$ HIGH terminates the FAST PAGE MODE operation.

Returning $\overline{RAS}$ and $\overline{CAS}$ HIGH terminates a memory cycle and decreases chip current to a reduced standby level. The chip is also preconditioned for the next cycle during the $\overline{RAS}$ high time. Memory cell data is retained in its correct state by maintaining power and executing any $\overline{RAS}$ cycle (READ, WRITE, $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$, or HIDDEN refresh) so that all 512 combinations of $\overline{RAS}$ addresses (A0-A8) are executed at least every 8ms, regardless of sequence. The $\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh cycle will also invoke the refresh counter and controller for ROW address control.

BYTE ACCESS CYCLE

The BYTE WRITE mode is determined by the use of $\overline{WEL}$ and $\overline{WEH}$ or $\overline{CASL}$ and $\overline{CASH}$. Enabling $\overline{WEL}$/$\overline{CASL}$ will select a lower BYTE WRITE cycle (DQ1-DQ8) while Enabling $\overline{WEH}$ or $\overline{CASH}$ will select an upper BYTE WRITE cycle (DQ9-DQ16). Enabling both $\overline{WEL}$ and $\overline{WEH}$ or $\overline{CASL}$ and $\overline{CASH}$ selects a WORD WRITE cycle.

The MT4C16256, MT4C16257, MT4C16258 and MT4C16259 can be viewed as two 256K x 8 DRAMS which have common input controls, with the exception of the $\overline{WE}$ or the $\overline{CAS}$ inputs. Figure 1 illustrates the MT4C16256 BYTE WRITE and WORD WRITE cycles and Figure 2 illustrates the MT4C16257 BYTE WRITE and WORD WRITE cycles.

The MT4C16257 also has BYTE READ and WORD READ cycles, since it uses two $\overline{CAS}$ inputs to control its byte accesses. Figure 3 illustrates the MT4C16257 BYTE READ and WORD READ cycles.

MASKED WRITE ACCESS CYCLE (MT4C16258/9 Only)

The MASKED WRITE mode control input selects normal WRITE access or MASKED WRITE access cycles. Every WRITE access cycle can be a MASKED WRITE, depending on the state of $\overline{WE}$ at $\overline{RAS}$ time. A MASKED WRITE is selected when mask data is supplied on the DQ pins and $\overline{WE}$ is LOW at $\overline{RAS}$ time. The MT4C16256 and MT4C16257 do not have the MASKED WRITE cycle function.

The data (mask data) present on the DQ1-DQ16 inputs at $\overline{RAS}$ time will be written to an internal bit mask data register and will then act as an individual write enable for each of the corresponding DQ inputs. If a LOW (logic "0") is written to a mask data register bit, the input port for that bit is disabled during the following WRITE operation and no new data will be written to that DRAM cell location. A HIGH (logic "1") on a mask data register bit enables the input port and allows normal WRITE operations to proceed. At $\overline{CAS}$ time, the bits present on the DQ1-DQ16 inputs will be either written to the DRAM (if the mask data bit was HIGH) or ignored (if the mask data bit was LOW).

New mask data must be supplied each time a MASKED WRITE cycle is initiated (non-persistent), even if the previous cycle's mask was the same mask.

Figure 4 illustrates the MT4C16258 MASKED WRITE operation and Figure 5 illustrates the MT4C16259 MASKED WRITE operation.

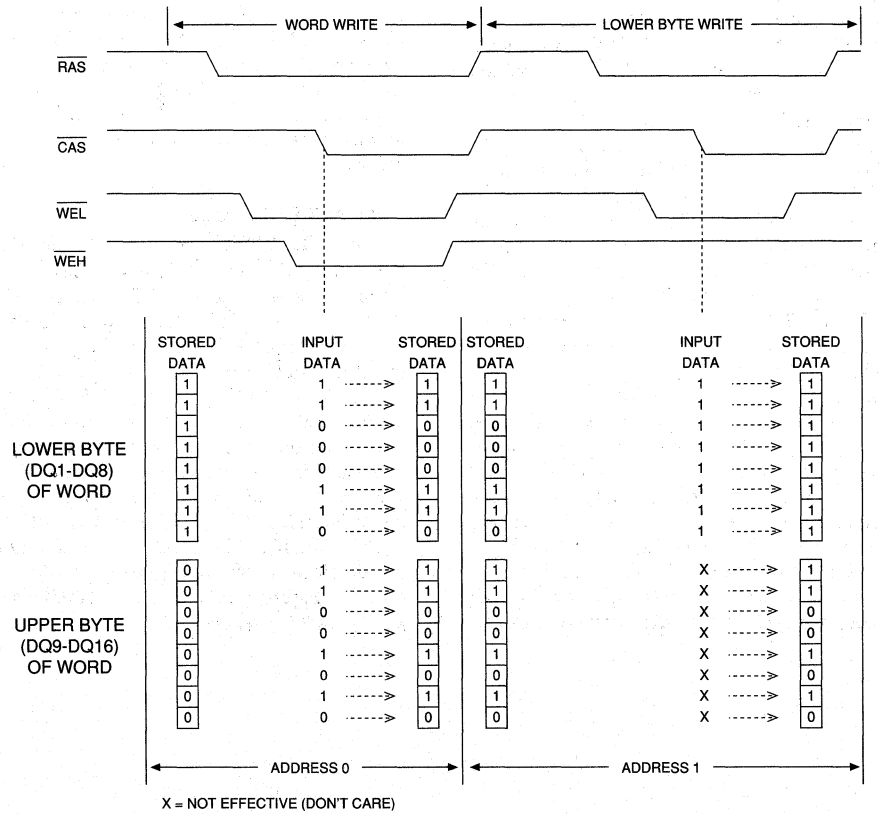


Figure 1
MT4C16256/8 WORD AND BYTE WRITE EXAMPLE

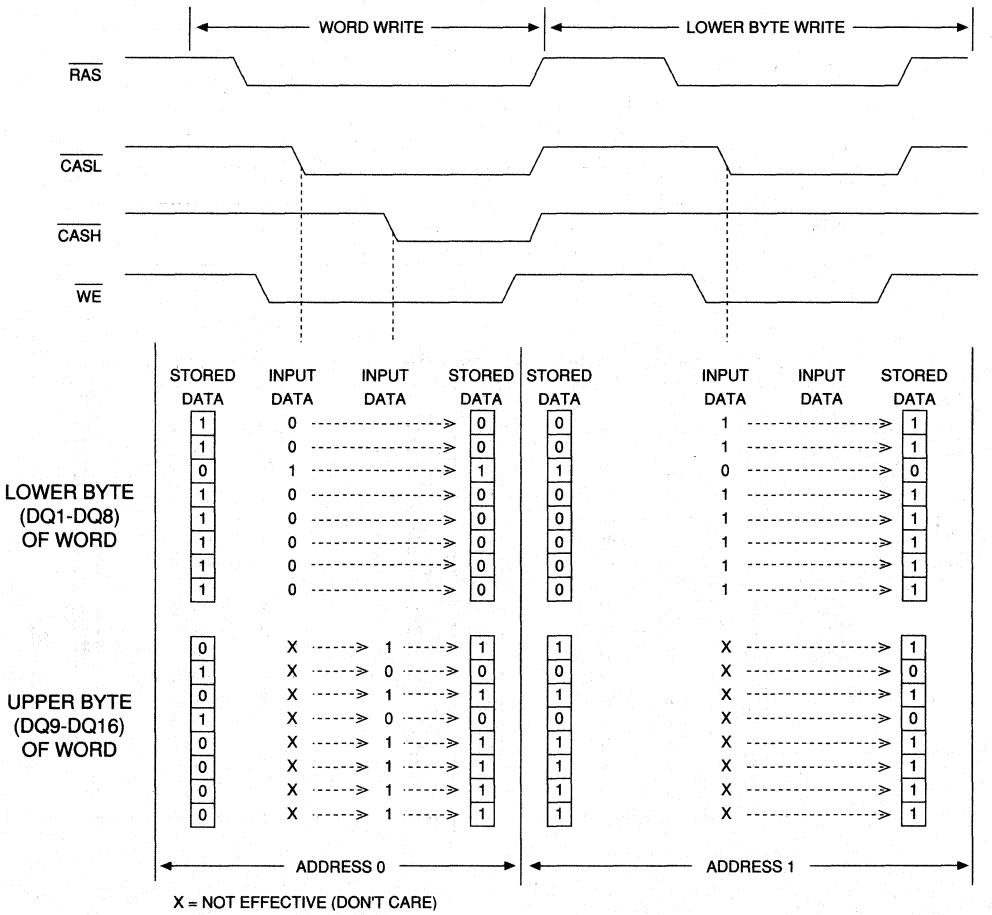


Figure 2
MT4C16257/9 WORD AND BYTE WRITE EXAMPLE

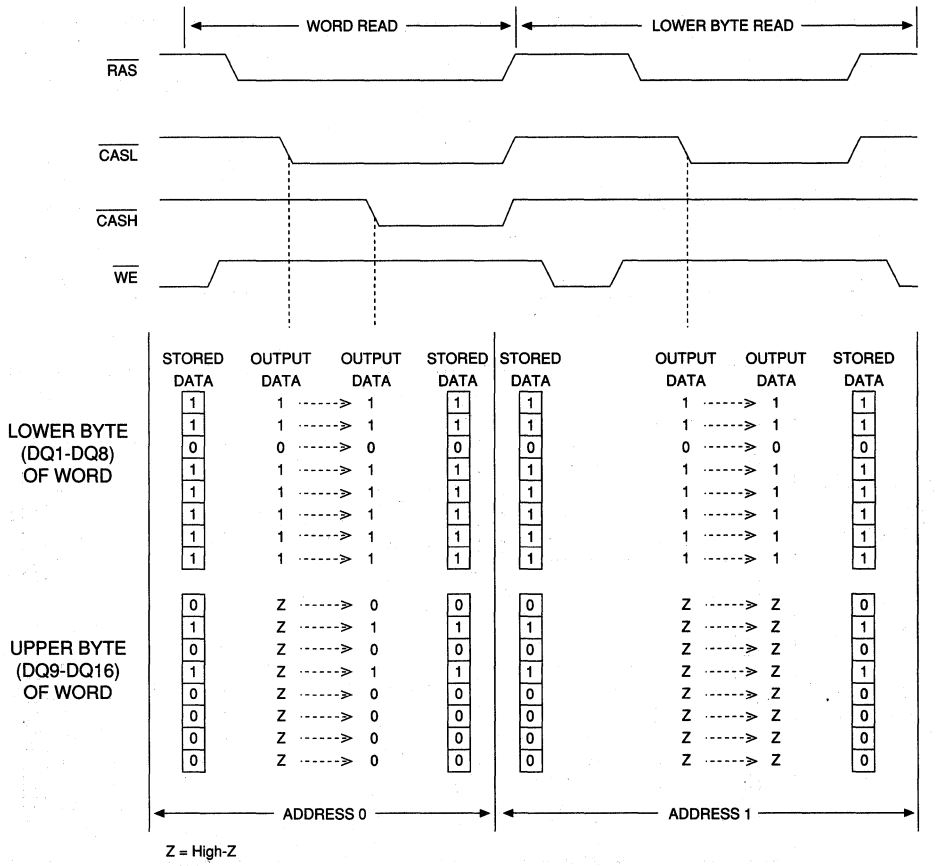


Figure 3
MT4C16257/9 WORD AND BYTE READ EXAMPLE

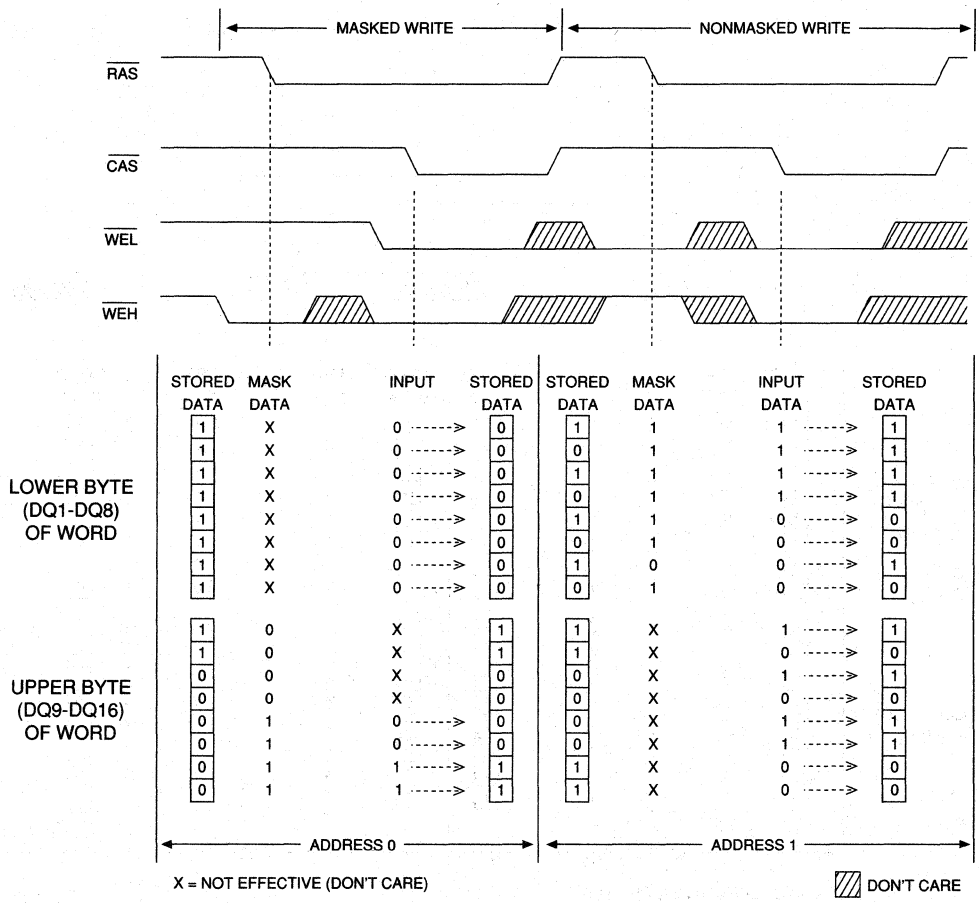


Figure 4
MT4C16258 MASKED WRITE EXAMPLE

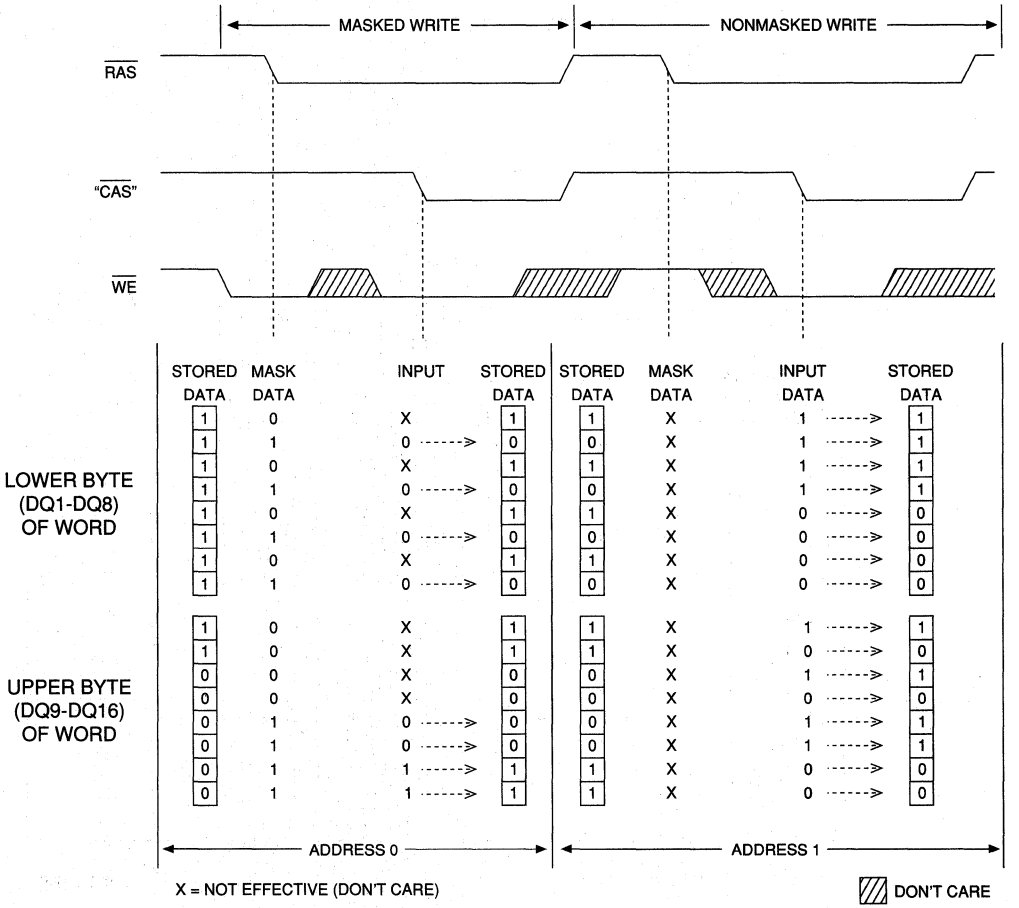


Figure 5
MT4C16259 MASKED WRITE EXAMPLE

TRUTH TABLE: MT4C16256/8

FUNCTION		RAS	CAS	WEL	WEH	OE	ADDRESSES tR	ADDRESSES tC	DQs	NOTES
Standby		H	H→X	X	X	X	X	X	High-Z	
READ		L	L	H	H	L	ROW	COL	Data Out	
WRITE: WORD (EARLY-WRITE)		L	L	L	L	X	ROW	COL	Data In	3
WRITE: LOWER BYTE (EARLY)		L	L	L	H	X	ROW	COL	Lower Byte, Data In Upper Byte, High-Z	3
WRITE: UPPER BYTE (EARLY)		L	L	H	L	X	ROW	COL	Lower Byte, High-Z Upper Byte, Data In	3
READ-WRITE		L	L	H→L	H→L	L→H	ROW	COL	Data Out, Data In	1, 3
PAGE-MODE	1st Cycle	L	H→L	H	H	L	ROW	COL	Data Out	
READ	2nd Cycle	L	H→L	H	H	L	n/a	COL	Data Out	
PAGE-MODE	1st Cycle	L	H→L	L	L	X	ROW	COL	Data In	1, 3
WRITE	2nd Cycle	L	H→L	L	L	X	n/a	COL	Data In	1, 3
PAGE-MODE	1st Cycle	L	H→L	H→L	H→L	L→H	ROW	COL	Data In	1, 3
READ-WRITE	2nd Cycle	L	H→L	H→L	H→L	L→H	n/a	COL	Data Out, Data In	1, 3
HIDDEN	READ	L→H→L	L	H	H	L	ROW	COL	Data Out	
REFRESH	WRITE	L→H→L	L	L	L	X	ROW	COL	Data In	1, 2, 3
RAS-ONLY REFRESH		L	H	H	H	X	ROW	n/a	High-Z	
CAS-BEFORE-RAS REFRESH		H→L	L	H	H	X	X	X	High-Z	

NOTE: 1. These cycles may also be BYTE WRITE cycles (either WEL or WEH active).
2. EARLY-WRITE only.
3. Data-in will be dependent on the mask provided (MT4C16258 only). Refer to Figure 4.

TRUTH TABLE: MT4C16257/9

FUNCTION		RAS	CASL	CASH	WE	OE	ADDRESSES tR	ADDRESSES tC	DQs	NOTES
Standby		H	H→X	H→X	X	X	X	X	High-Z	
READ: WORD		L	L	L	H	L	ROW	COL	Data Out	
READ: LOWER BYTE		L	L	H	H	L	ROW	COL	Lower Byte, Data Out Upper Byte, High-Z	
READ: UPPER BYTE		L	H	L	H	L	ROW	COL	Lower Byte, High-Z Upper Byte, Data Out	
WRITE: WORD (EARLY-WRITE)		L	L	L	L	X	ROW	COL	Data In	5
WRITE: LOWER BYTE (EARLY)		L	L	H	L	X	ROW	COL	Lower Byte, Data In Upper Byte, High-Z	5
WRITE: UPPER BYTE (EARLY)		L	H	L	L	X	ROW	COL	Lower Byte, High-Z Upper Byte, Data In	5
READ-WRITE		L	L	L	H→L	L→H	ROW	COL	Data Out, Data In	1, 2, 5
PAGE-MODE READ	1st Cycle	L	H→L	H→L	H	L	ROW	COL	Data Out	2
	2nd Cycle	L	H→L	H→L	H	L	n/a	COL	Data Out	2
PAGE-MODE WRITE	1st Cycle	L	H→L	H→L	L	X	ROW	COL	Data In	1, 5
	2nd Cycle	L	H→L	H→L	L	X	n/a	COL	Data In	1, 5
PAGE-MODE READ-WRITE	1st Cycle	L	H→L	H→L	H→L	L→H	ROW	COL	Data Out, Data In	1, 2, 5
	2nd Cycle	L	H→L	H→L	H→L	L→H	n/a	COL	Data Out, Data In	1, 2, 5
HIDDEN REFRESH	READ	L→H→L	L	L	H	L	ROW	COL	Data Out	2
	WRITE	L→H→L	L	L	L	X	ROW	COL	Data In	1, 3, 5
RAS-ONLY REFRESH		L	H	H	X	X	ROW	n/a	High-Z	
CAS-BEFORE-RAS REFRESH		H→L	L	L	H	X	X	X	High-Z	4

NOTE:
1. These WRITE cycles may also be BYTE WRITE cycles (either CASL or CASH active).
2. These READ cycles may also be BYTE READ cycles (either CASL or CASH active).
3. EARLY-WRITE only.
4. Only one of the two CAS must be active (CASL or CASH).
3. Data-in will be dependent on the mask provided (MT4C16259 only). Refer to Figure 5.

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS} ..... -1V to +7V
Operating Temperature, T_A (Ambient) ..... 0°C to +70°C
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 3, 4, 6, 7) (0°C ≤ T_A ≤ 70°C; V_{CC} = 5V ±10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.5	V	1
Input High (Logic 1) Voltage, All Inputs	V_{IH}	2.4	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, All Inputs	V_{IL}	-1.0	0.8	V	1
INPUT LEAKAGE CURRENT Any Input 0V ≤ V_{IN} ≤ Vcc (All other pins not under test = 0V)	I_I	-2	2	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled, 0V ≤ V_{OUT} ≤ 5.5V)	I_{OZ}	-10	10	µA	
OUTPUT LEVELS Output High Voltage (I_{OUT} = -5mA)	V_{OH}	2.4		V	
Output Low Voltage (I_{OUT} = 4.2mA)	V_{OL}		0.4	V	

		MAX				
PARAMETER/CONDITION	SYMBOL	-7	-8	-10	UNITS	NOTES
STANDBY CURRENT: (TTL) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC1}	2	2	2	mA	
STANDBY CURRENT: (CMOS) ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} -0.2V)	I_{CC2}	1	1	1	mA	25
OPERATING CURRENT: Random READ/WRITE Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC (MIN))	I_{CC3}	160	140	120	mA	3, 4, 42
OPERATING CURRENT: FAST PAGE MODE Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: ^tPC = ^tPC (MIN); ^tCP, ^tASC = 10ns)	I_{CC4}	120	110	100	mA	3, 4, 42
REFRESH CURRENT: $\overline{RAS}$-ONLY Average power supply current ($\overline{RAS}$ Cycling, $\overline{CAS}$=V_{IH}: ^tRC = ^tRC (MIN))	I_{CC5}	160	140	120	mA	3, 5, 42
REFRESH CURRENT: $\overline{CAS}$-BEFORE-$\overline{RAS}$ Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC (MIN))	I_{CC6}	160	140	120	mA	3, 5

CAPACITANCE

(Note: 2)

PARAMETER	SYMBOL	MAX	UNITS	NOTES
Input Capacitance: A0-A8	C_{I1}	5	pF	2
Input Capacitance: $\overline{RAS}$, $\overline{CAS}$/($\overline{CASL}$,$\overline{CASH}$), ($\overline{WEL}$, $\overline{WEH}$)/ $\overline{WE}$, $\overline{OE}$	C_{I2}	7	pF	2
Input/Output Capacitance: DQ	C_{IO}	7	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C ≤ T_A ≤ +70°C; V_{CC} = 5V ±10%)

AC CHARACTERISTICS		-7		-8		-10			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	^tRC	130		150		180		ns	
READ-WRITE cycle time	^tRWC	180		200		245		ns	
FAST-PAGE-MODE READ or WRITE cycle time	^tPC	45		50		55		ns	35
FAST-PAGE-MODE READ-WRITE cycle time	^tPRWC	95		100		110		ns	35
Access time from $\overline{RAS}$	^tRAC		70		80		100	ns	14
Access time from $\overline{CAS}$	^tCAC		20		20		25	ns	15, 33
Output Enable time	^tOE		20		20		25	ns	33
Access time from column address	^tAA		35		40		45	ns	
Access time from $\overline{CAS}$ precharge	^tCPA		40		45		55	ns	33
$\overline{RAS}$ pulse width	^tRAS	70	100,000	80	100,000	100	100,000	ns	
$\overline{RAS}$ pulse width (PAGE MODE)	^tRASP	70	100,000	80	100,000	100	100,000	ns	
$\overline{RAS}$ hold time	^tRSH	20		20		25		ns	40
$\overline{RAS}$ precharge time	^tRP	50		60		70		ns	
$\overline{CAS}$ pulse width	^tCAS	20	100,000	20	100,000	25	100,000	ns	39
$\overline{CAS}$ hold time	^tCSH	70		80		100		ns	32
$\overline{CAS}$ precharge time	^tCPN	10		10		10		ns	16, 36
$\overline{CAS}$ precharge time (PAGE MODE)	^tCP	10		10		10		ns	36
$\overline{RAS}$ to $\overline{CAS}$ delay time	^tRCD	20	50	20	60	25	75	ns	17, 31
$\overline{CAS}$ to $\overline{RAS}$ precharge time	^tCRP	10		10		10		ns	32
Row address setup time	^tASR	0		0		0		ns	
Row address hold time	^tRAH	10		10		15		ns	
$\overline{RAS}$ to column address delay time	^tRAD	15	35	15	40	20	55	ns	18
Column address setup time	^tASC	0		0		0		ns	31
Column address hold time	^tCAH	15		15		20		ns	31
Column address hold time (referenced to $\overline{RAS}$)	^tAR	55		60		75		ns	
Column address to $\overline{RAS}$ lead time	^tRAL	35		40		55		ns	
Read command setup time	^tRCS	0		0		0		ns	26, 31
Read command hold time (referenced to $\overline{CAS}$)	^tRCH	0		0		0		ns	19, 26 ,32
Read command hold time (referenced to $\overline{RAS}$)	^tRRH	0		0		0		ns	19
$\overline{CAS}$ to output in Low-Z	^tCLZ	0		0		0		ns	33

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C ≤ T_A ≤ +70°C; Vcc = 5V ±10%)

AC CHARACTERISTICS		-7		-8		-10			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Output buffer turn-off delay	^tOFF	0	15	0	15	0	20	ns	20, 29, 33
Output disable time	^tOD		15		15		20	ns	29, 41
Write command setup time	^tWCS	0		0		0		ns	21, 26, 31
Write command hold time	^tWCH	15		15		20		ns	26, 40
Write command hold time (referenced to $\overline{RAS}$)	^tWCR	55		60		75		ns	26
Write command pulse width	^tWP	10		10		20		ns	26
Write command to $\overline{RAS}$ lead time	^tRWL	20		20		25		ns	26
Write command to $\overline{CAS}$ lead time	^tCWL	20		20		25		ns	26, 32
Data-in setup time	^tDS	0		0		0		ns	22, 33
Data-in hold time	^tDH	15		15		20		ns	22, 33
Data-in hold time (referenced to $\overline{RAS}$)	^tDHR	55		60		75		ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	^tRWD	95		105		135		ns	21
Column address to $\overline{WE}$ delay time	^tAWD	60		65		80		ns	21
$\overline{CAS}$ to $\overline{WE}$ delay time	^tCWD	45		45		60		ns	21, 31
Transition time (rise or fall)	^tT	3	50	3	50	3	50	ns	9, 10
Refresh period (512 cycles)	^tREF		8		8		8	ms	28
$\overline{RAS}$ to $\overline{CAS}$ precharge time	^tRPC	10		10		10		ns	
$\overline{CAS}$ setup time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tCSR	10		10		10		ns	5, 31
$\overline{CAS}$ hold time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tCHR	10		10		10		ns	5, 32
MASKED WRITE command to $\overline{RAS}$ setup time	^tWRS	0		0		0		ns	26, 27
$\overline{WE}$ hold time (MASKED WRITE and $\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tWRH	15		15		15		ns	26
Mask data to $\overline{RAS}$ setup time	^tMS	0		0		0		ns	26, 27
Mask data to $\overline{RAS}$ hold time	^tMH	15		15		15		ns	26, 27
$\overline{OE}$ hold time from $\overline{WE}$ during READ-MODIFY-WRITE cycle	^tOEH	20		20		25		ns	28
$\overline{OE}$ setup prior to $\overline{RAS}$ during HIDDEN REFRESH cycle	^tORD	0		0		0		ns	
Last $\overline{CAS}$ going LOW to first $\overline{CAS}$ to return HIGH	^tCLCH	10		10		10		ns	34
$\overline{WE}$ setup time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tWRP	10		10		10		ns	

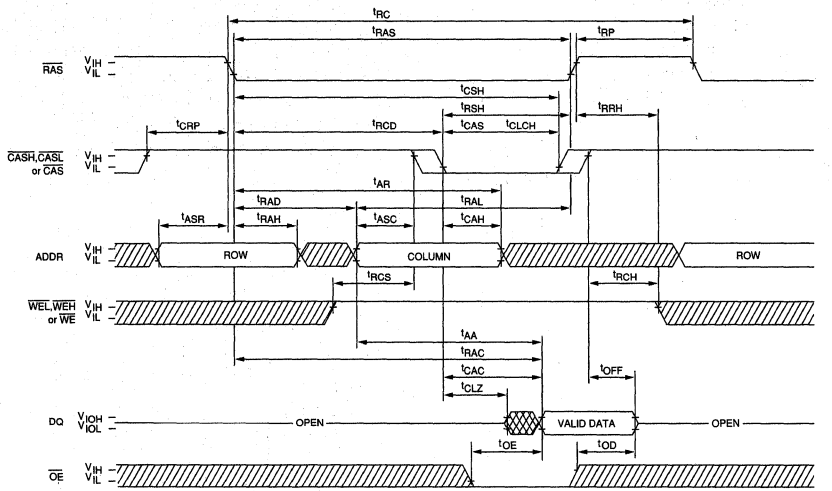
NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. V_{CC} = 5V ±10%, f = 1 MHz.
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \le T_A \le 70°C$) is assured.
7. An initial pause of 100µs is required after power-up followed by eight $\overline{RAS}$ refresh cycles ($\overline{RAS}$-ONLY or CBR) before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-up should be repeated any time the ^tREF refresh requirement is exceeded.
8. AC characteristics assume ^tT = 5ns.
9. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS}$ = V_{IH}, data output is High-Z.
12. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to 2 TTL gate and 100pF.
14. Assumes that $^tRCD < ^tRCD$ (MAX). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
15. Assumes that $^tRCD \ge ^tRCD$ (MAX).
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the Q buffer, $\overline{CAS}$ must be pulsed HIGH for ^tCPN.
17. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (MAX) limit, then access time is controlled exclusively by ^tCAC.
18. Operation within the ^tRAD limit ensures that ^tRCD (MAX) can be met. ^tRAD (MAX) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (MAX) limit, then access time is controlled exclusively by ^tAA.
19. Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
20. ^tOFF (MAX) defines the time at which the output achieves the open circuit condition, not a reference to V_{OH} or V_{OL}.
21. ^tWCS, ^tRWD, ^tAWD and ^tCWD are restrictive operating parameters in LATE-WRITE and READ-MODIFY-WRITE cycles only. If $^tWCS \ge ^tWCS$ (MIN), the cycle is an EARLY-WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If $^tRWD \ge ^tRWD$ (MIN), $^tAWD \ge ^tAWD$ (MIN) and $^tCWD \ge ^tCWD$ (MIN), the cycle is a READ-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of Q (at access time and until $\overline{CAS}$ or $\overline{OE}$ goes back to V_{IH}) is indeterminate. $\overline{OE}$ held HIGH and $\overline{WE}$ taken LOW after $\overline{CAS}$ goes LOW results in a LATE-WRITE ($\overline{OE}$ controlled) cycle.
22. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY-WRITE cycles and $\overline{WE}$ leading edge in LATE-WRITE or READ-MODIFY-WRITE cycles.
23. During a READ cycle, if $\overline{OE}$ is LOW then taken HIGH before $\overline{CAS}$ goes HIGH, Q goes open. If $\overline{OE}$ is tied permanently LOW, a LATE-WRITE or READ-MODIFY-WRITE operation is not possible.
24. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW and $\overline{OE}$ = HIGH.
25. All other inputs at Vcc -0.2V.
26. Write command is defined as either $\overline{WEL}$ or $\overline{WEH}$ or both going LOW on the MT4C16256/8. Write command is defined as $\overline{WE}$ going LOW on the MT4C16257/9.
27. MT4C16258/9 only.
28. LATE-WRITE and READ-MODIFY-WRITE cycles must have both ^tOD and ^tOEH met ($\overline{OE}$ HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. The DQs will provide the previously read data if $\overline{CAS}$ remains LOW and $\overline{OE}$ is taken back LOW after ^tOEH is met. If $\overline{CAS}$ goes HIGH prior to $\overline{OE}$ going back LOW, the DQs will remain open.
29. The DQs open during READ cycles once ^tOD or ^tOFF occur. If $\overline{CAS}$ goes HIGH first, $\overline{OE}$ becomes a "don't care." If $\overline{OE}$ goes HIGH and $\overline{CAS}$ stays LOW, $\overline{OE}$ is not a "don't care;" and the DQs will provide the previously read data if $\overline{OE}$ is taken back LOW (while $\overline{CAS}$ remains LOW).

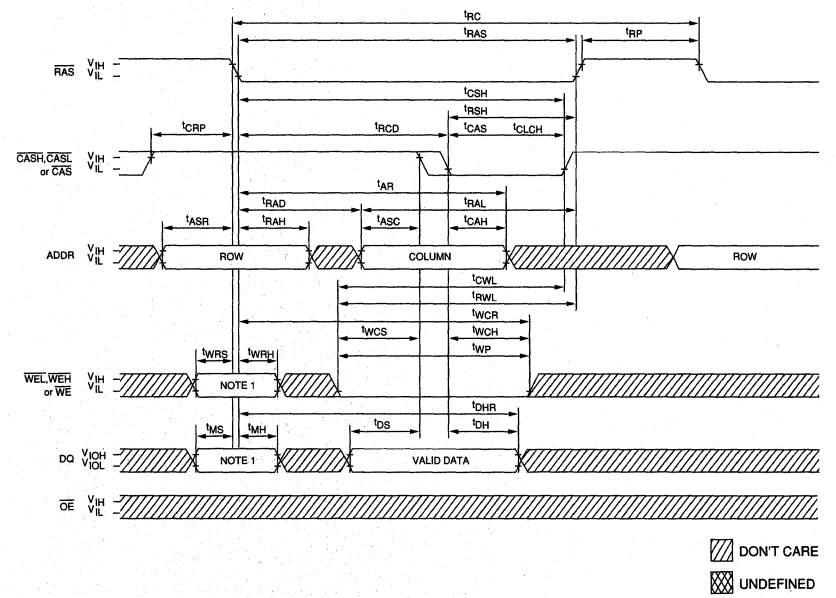
NOTES (continued)

30. Notes 31 through 41 apply to MT4C16257/9 only (*):
31. *The first $\overline{CAS}$x edge to transition LOW.
32. *The last $\overline{CAS}$x edge to transition HIGH.
33. *Output parameter (DQx) is referenced to corresponding $\overline{CAS}$ input; DQ1-DQ8 by $\overline{CASL}$ and DQ9-DQ16 by $\overline{CASH}$.
34. *Last falling $\overline{CAS}$x edge to first rising $\overline{CAS}$x edge.
35. *Last rising $\overline{CAS}$x edge to next cycle's last rising $\overline{CAS}$x edge.
36. *Last rising $\overline{CAS}$x edge to first falling $\overline{CAS}$x edge.
37. *First DQs controlled by the first $\overline{CAS}$x to go LOW.
38. *Last DQs controlled by the last $\overline{CAS}$x to go HIGH.
39. *Each $\overline{CAS}$x must meet minimum pulse width.
40. *Last $\overline{CAS}$x to go LOW.
41. *All DQs controlled, regardless $\overline{CASL}$ and $\overline{CASH}$.
42. Column address changed once while $\overline{RAS}$ = V_{IL} and $\overline{CAS}$ = V_{IH}.

READ CYCLE

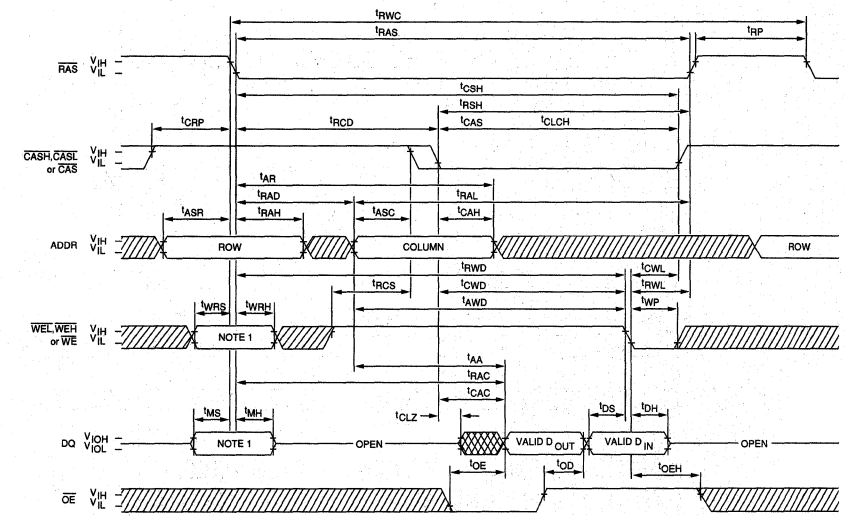


EARLY-WRITE CYCLE

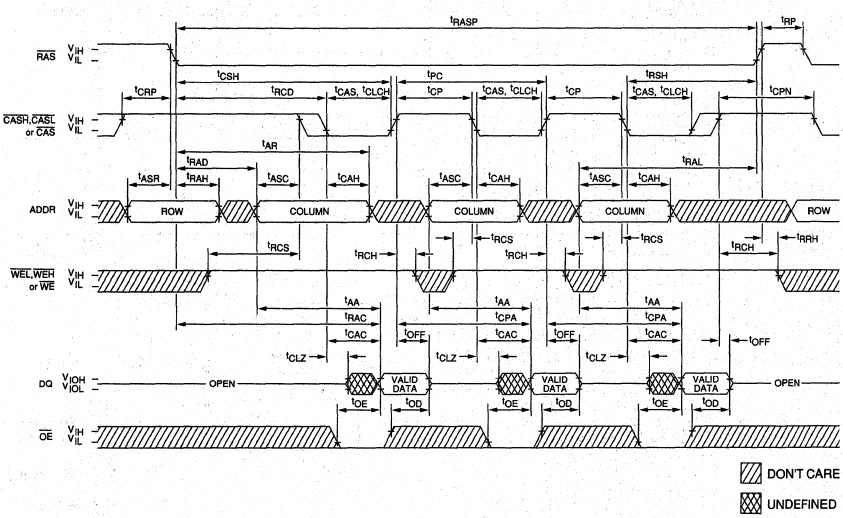


NOTE: 1. Applies to MT4C16258 and MT4C16259 only. $\overline{WE}$ selects between normal WRITE and MASKED WRITE at $\overline{RAS}$ time. The DQ inputs are "don't care" for a normal WRITE ($\overline{WE}$ HIGH at $\overline{RAS}$ time). The DQ inputs provide the mask data at $\overline{RAS}$ time for a MASKED WRITE ($\overline{WE}$ LOW at $\overline{RAS}$ time). $\overline{WEL}$, $\overline{WEH}$ and DQ inputs on MT4C16256 and MT4C16257 are "don't care" at $\overline{RAS}$ time.

READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)

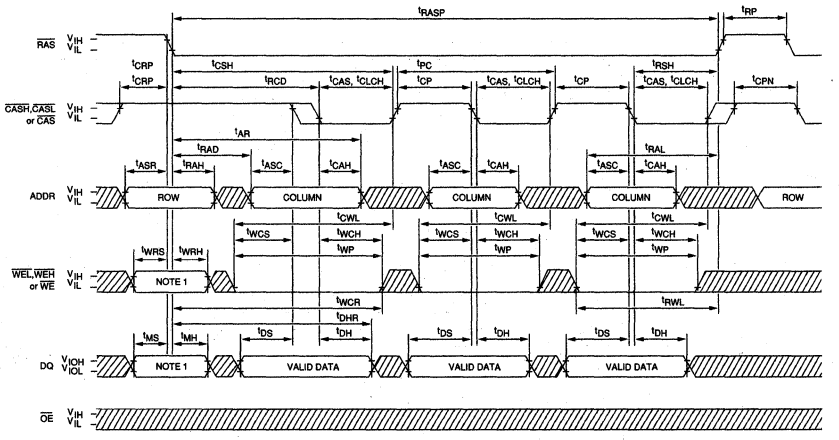


FAST-PAGE-MODE READ CYCLE

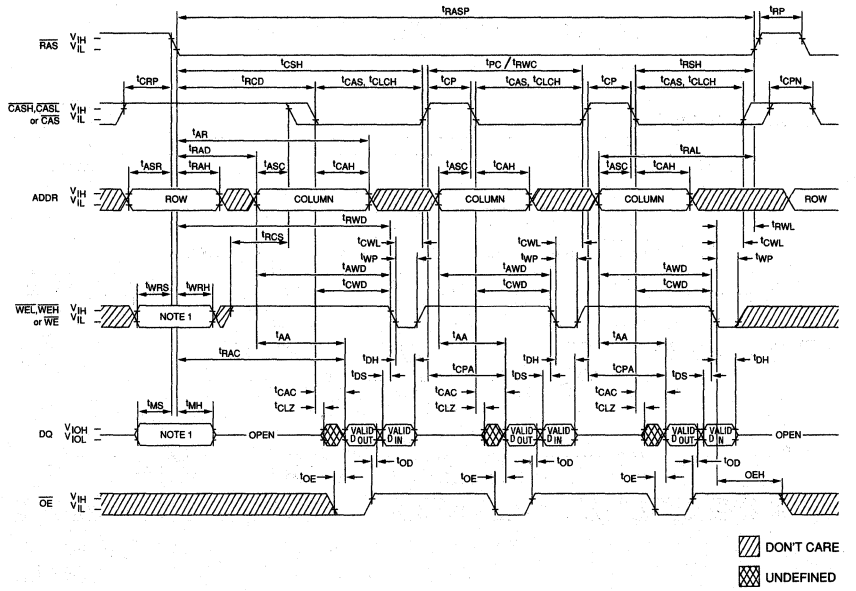


NOTE: 1. Applies to MT4C16258 and MT4C16259 only. $\overline{WE}$ selects between normal WRITE and MASKED WRITE at $\overline{RAS}$ time. The DQ inputs are "don't care" for a normal WRITE ($\overline{WE}$ HIGH at $\overline{RAS}$ time). The DQ inputs provide the mask data at $\overline{RAS}$ time for a MASKED WRITE ($\overline{WE}$ LOW at $\overline{RAS}$ time). $\overline{WEL}$, $\overline{WEH}$ and DQ inputs on MT4C16256 and MT4C16257 are "don't care" at $\overline{RAS}$ time.

FAST-PAGE-MODE EARLY-WRITE CYCLE

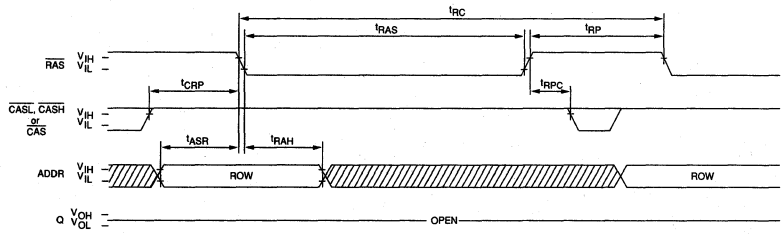


FAST-PAGE-MODE READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)

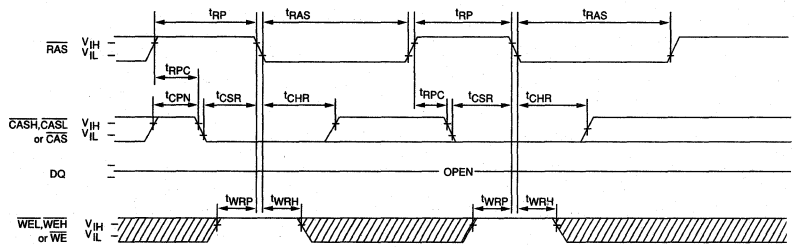


NOTE: 1. Applies to MT4C16258 and MT4C16259 only. $\overline{WE}$ selects between normal WRITE and MASKED WRITE at $\overline{RAS}$ time. The DQ inputs are "don't care" for a normal WRITE ($\overline{WE}$ HIGH at $\overline{RAS}$ time). The DQ inputs provide the mask data at $\overline{RAS}$ time for a MASKED WRITE ($\overline{WE}$ LOW at $\overline{RAS}$ time). $\overline{WEL}$, $\overline{WEH}$ and DQ inputs on MT4C16256 and MT4C16257 are "don't care" at $\overline{RAS}$ time.

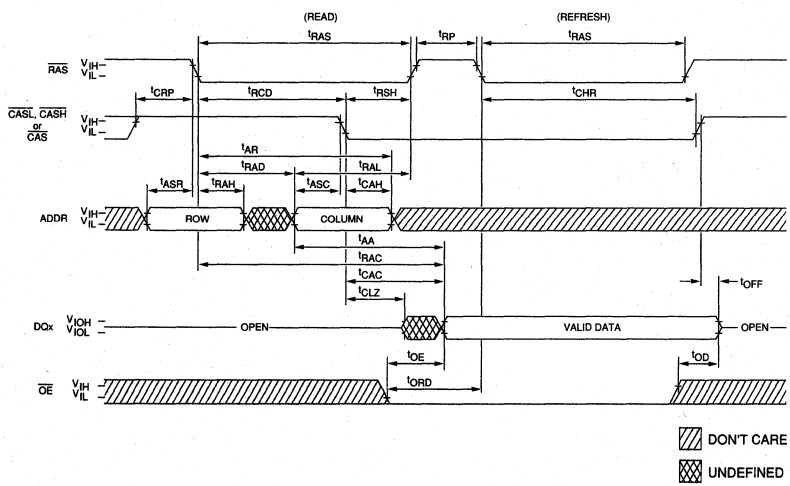
RAS ONLY REFRESH CYCLE
(ADDR = A0-A8, OE; WEL, WEH or WE = DON'T CARE)



CAS-BEFORE-RAS REFRESH CYCLE
(A0-A8; and OE = DON'T CARE)



HIDDEN REFRESH CYCLE [24]
(WEL, WEH or WE = HIGH; OE = LOW)



NEW ■ WIDE DRAM

DRAM

256K x 16 DRAM

LOW POWER, EXTENDED REFRESH

FEATURES

- Industry standard x16 pinouts, timing, functions and packages
- High-performance, CMOS silicon-gate process
- Single +5V ±10% power supply
- All device pins are fully TTL compatible
- Refresh modes: $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$ (CBR), HIDDEN and BATTERY BACKUP (BBU)
- FAST PAGE MODE access cycle
- BYTE WRITE access cycle
- BYTE READ access cycle (MT4C16257/9 L only)
- NONPERSISTENT MASKED WRITE access cycle (MT4C16258/9 L only)
- 512 cycle refresh distributed across 64ms
- Low power, 1mW standby; 500mW active, typical

OPTIONS — MARKING

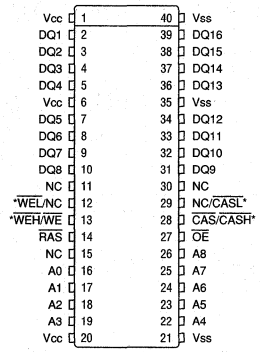
- Timing
  - 70ns access — -7
  - 80ns access — -8
  - 100ns access — -10
- Write Cycle Access
  - BYTE or WORD via $\overline{WE}$ (non-maskable) — MT4C16256 L
  - BYTE or WORD via $\overline{CAS}$ (non-maskable) — MT4C16257 L
  - BYTE or WORD via $\overline{WE}$ (maskable) — MT4C16258 L
  - BYTE or WORD via $\overline{CAS}$ (maskable) — MT4C16259 L
- Packages
  - Plastic SOJ (400 mil) — DJ
  - Plastic TSOP (400 mil) — TG
  - Plastic ZIP (475 mil) — Z

NOTE: Available in die form. Please consult factory for die data sheets.

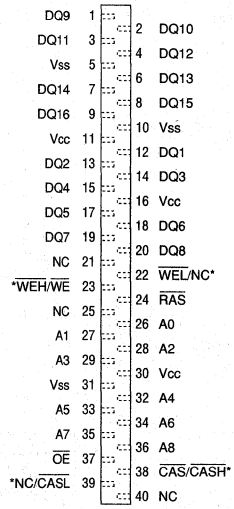
- Part Number Example: MT4C16256DJ-7 L

PIN ASSIGNMENT (Top View)

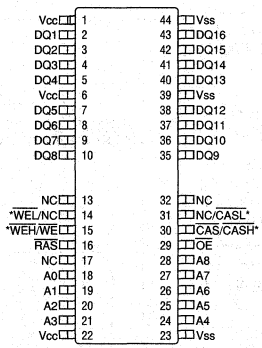
40-Pin SOJ (Q-6)



40-Pin ZIP (O-4)



40-Pin TSOP (R-5)



*MT4C16256/8 L / MT4C16257/9 L

GENERAL DESCRIPTION

The MT4C16256/7/8/9 L are randomly accessed solid-state memories containing 4,194,304 bits organized in a x16 configuration. The MT4C16256 L and MT4C16258 L have both BYTE WRITE and WORD WRITE access cycles via two write enable pins. The MT4C16257 L and MT4C16259 L have both BYTE WRITE and WORD WRITE access cycles via two $\overline{CAS}$ pins. The MT4C16258 L and MT4C16259 L are also able to perform WRITE-PER-BIT accesses.

The MT4C16256 L and MT4C16257 L function in the same manner except that $\overline{WEL}$ and $\overline{WEH}$ on MT4C16256 L and $\overline{CASL}$ and $\overline{CASH}$ on MT4C16257 L control the selection of byte WRITE access cycles. $\overline{WEL}$ and $\overline{WEH}$ function in an

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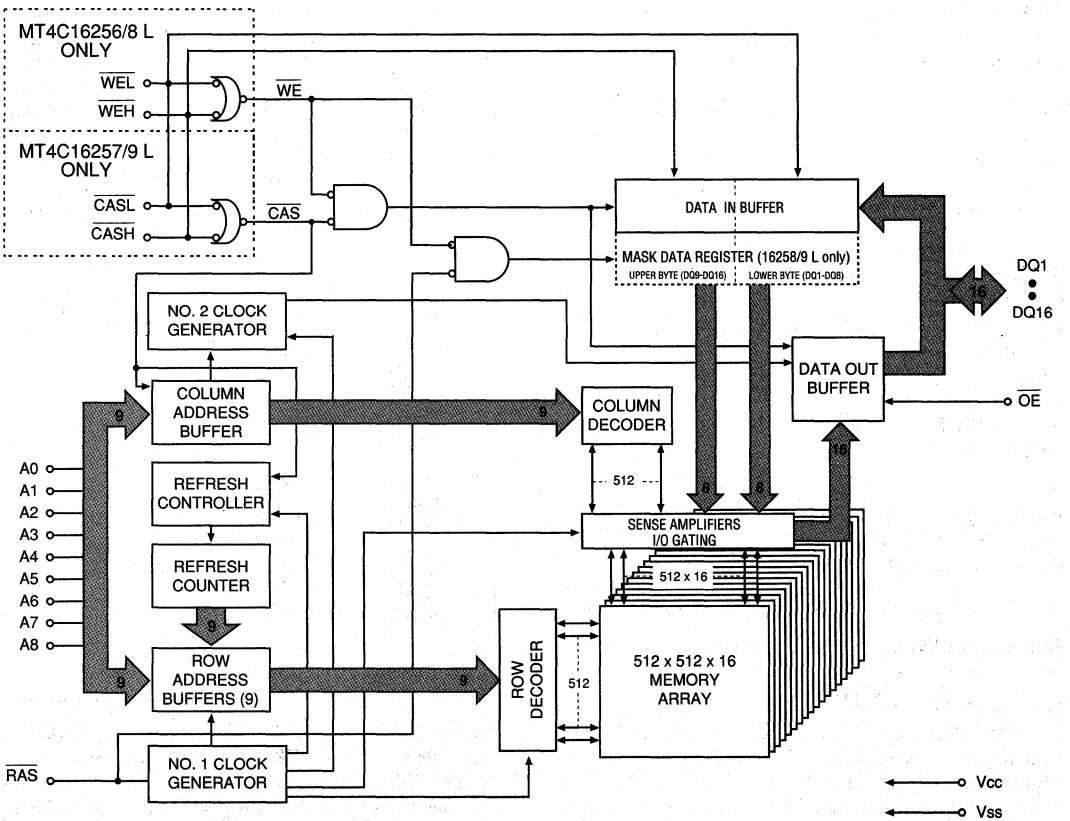
identical manner to $\overline{WE}$ in that either $\overline{WEL}$ or $\overline{WEH}$ will generate an internal $\overline{WE}$. $\overline{CASL}$ and $\overline{CASH}$ function in an identical manner to $\overline{CAS}$ in that either $\overline{CASL}$ or $\overline{CASH}$ will generate an internal $\overline{CAS}$.

The MT4C16256 L "$\overline{WE}$" function and timing are determined by the first $\overline{WE}$ ($\overline{WEL}$ or $\overline{WEH}$) to transition LOW and by the last to transition back HIGH. Use of only one of the two results in a BYTE WRITE cycle. $\overline{WEL}$ transitioning LOW selects a WRITE cycle for the lower byte (DQ1-DQ8) and $\overline{WEH}$ transitioning LOW selects a WRITE cycle for the upper byte (DQ9-DQ16).

The MT4C16257 L "$\overline{CAS}$" function and timing are determined by the first $\overline{CAS}$ ($\overline{CASL}$ or $\overline{CASH}$) to transition LOW and by the last to transition back HIGH. Use of only one of the two results in a BYTE WRITE cycle. $\overline{CASL}$ transitioning LOW selects a WRITE cycle for the lower byte (DQ1-DQ8) and $\overline{CASH}$ transitioning LOW selects a WRITE cycle for the upper byte (DQ9-DQ16). BYTE READ cycles are achieved through $\overline{CASL}$ or $\overline{CASH}$ in the same manner during READ cycles for the MT4C16257 L.

The MT4C16258 L and MT4C16259 L function in the same manner as MT4C16256 L and MT4C16257 L, respectively; and they have NONPERSISTENT MASKED WRITE cycle capabilities. This option allows the MT4C16258 L and MT4C16259 L to operate with either normal WRITE cycles or with NONPERSISTENT MASKED WRITE cycles.

FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTIONS

SOJ PINS	TSOP PINS	ZIP PINS	SYMBOL	TYPE	DESCRIPTION
14	16	24	$\overline{RAS}$	Input	ROW Address Strobe: $\overline{RAS}$ is used to latch in the 9 row-address bits and strobe the $\overline{WE}$ and DQs on the MASKED WRITE option (MT4C16258 L and MT4C16259 L only).
28	30	38	$\overline{CAS}$/ $\overline{CASH}$	Input	Column Address Strobe: $\overline{CAS}$ (MT4C16256/8 L) is used to latch-in the 9 column-address bits, enable the DRAM output buffers, and strobe the data inputs on WRITE cycles. $\overline{CAS}$ controls DQ1 through DQ16. Column Address Strobe Upper Byte: $\overline{CASH}$ (MT4C16257/9 L) is the $\overline{CAS}$ control for DQ9 through DQ16. The DQs for the byte not being accessed will remain in a High-Z (high impedance) state during either a READ or a WRITE access cycle.
27	29	37	$\overline{OE}$	Input	Output Enable: $\overline{OE}$ enables the output buffers when taken LOW during a READ access cycle. $\overline{RAS}$ and $\overline{CAS}$ (MT4C16256/8 L) or $\overline{CASL}$ / $\overline{CASH}$ (MT4C16257/9 L) must be LOW and $\overline{WEL}$ / $\overline{WEH}$ (MT4C16256/8 L) or $\overline{WE}$ (MT4C16257/9 L) must be HIGH before $\overline{OE}$ will control the output buffers. Otherwise, the output buffers are in a High-Z state.
13	15	23	$\overline{WEH}$/$\overline{WE}$	Input	Write Enable Upper Byte: $\overline{WEH}$ (MT4C1625L6/8 L) is $\overline{WE}$ control for the DQ9 through DQ16 inputs. If $\overline{WE}$ or $\overline{WEH}$ is LOW, the access is a WRITE cycle. If either $\overline{WE}$ or $\overline{WEH}$ is LOW at $\overline{RAS}$ time on MT4C16258 L, then it is also a MASKED WRITE cycle. The DQs for the byte not being written will remain in a High-Z state (BYTE WRITE cycle only). Write Enable: $\overline{WE}$ (MT4C16257/9 L) controls DQ1 through DQ16 inputs. If $\overline{WE}$ is LOW, the access is a WRITE cycle. The MT4C16258/9 L also use $\overline{WE}$ to enable the MASK register during $\overline{RAS}$ time.
12	14	22	$\overline{WEL}$/NC	Input	Write Enable Lower Byte: $\overline{WEL}$ (MT4C16256/8 L) is the $\overline{WE}$ control for DQ1 through DQ8 inputs. If $\overline{WEL}$ is LOW, the access is a WRITE cycle. If $\overline{WEL}$ is LOW at $\overline{RAS}$ time on MT4C16258 L, then it is also a MASKED WRITE cycle. The DQs for the byte not being written will remain in a High-Z state (BYTE WRITE cycle only).
29	31	39	NC/$\overline{CASL}$	Input	Column Address Strobe Low Byte: $\overline{CASL}$ (MT4C16257/9 L) is the $\overline{CAS}$ control for DQ1 through DQ8. The DQs for the byte not being accessed will remain in a High-Z state during either a READ or a WRITE access cycle.
16-19, 22-26	18-21, 24-28	26-29, 32-36	A0-A8	Input	Address Inputs: These inputs are multiplexed and clocked by $\overline{RAS}$ and $\overline{CAS}$ (or $\overline{CASL}$ / $\overline{CASH}$) to select one 16-bit word (or 8-bit byte) out of the 256K available words.

PIN DESCRIPTIONS (continued)

SOJ PINS	TSOP PINS	ZIP PINS	SYMBOL	TYPE	DESCRIPTION
2-5, 7-10, 31-34, 36-39	2-5, 7-10, 35-38, 40-43	12-15, 17-20, 1-4, 6-9	DQ1-DQ16	Input/ Output	Data I/O: For WRITE cycles, DQ1-DQ16 act as inputs to the addressed DRAM location. BYTE WRITEs can be performed by using $\overline{WEL}$ / $\overline{WEH}$ (MT4C16256/8L) or $\overline{CASL}$ / $\overline{CASH}$ (MT4C16257/8L) to select the byte to be written. For READ access cycles, DQ1-DQ16 act as outputs for the addressed DRAM Location. All sixteen I/Os are active for READ cycles (MT4C16256/8L). The MT4C16257/9L allow for BYTE READ cycles.
11, 15, 30	13, 17	21, 25, 40	NC	-	No Connect: These pins should be either left unconnected or tied to ground.
1, 6, 20	1, 6, 22	11, 16, 30	Vcc	Supply	Power Supply: +5V ±10%
21, 35, 40	23, 39, 44	5, 10, 31	Vss	Supply	Ground

FUNCTIONAL DESCRIPTION

Each bit is uniquely addressed through the 18 address bits during READ or WRITE cycles. These are entered 9 bits (A0-A8) at a time. $\overline{RAS}$ is used to latch the first 9 bits and $\overline{CAS}$ the latter 9 bits.

The $\overline{CAS}$ control also determines whether the cycle will be a refresh cycle ($\overline{RAS}$-ONLY) or an active cycle (READ, WRITE or READ-WRITE) once $\overline{RAS}$ goes LOW. The MT4C16256 L and MT4C16258 L each have one $\overline{CAS}$ control while the MT4C16257 L and MT4C16259 L have two:$\overline{CASL}$ and $\overline{CASH}$.

The $\overline{CASL}$ and $\overline{CASH}$ inputs internally generate a $\overline{CAS}$ signal functioning in an identical manner to the single $\overline{CAS}$ input on the other 256K x 16 DRAMs. The key difference is each $\overline{CAS}$ controls its corresponding DQ tristate logic (in conjunction with $\overline{OE}$ and $\overline{WE}$). $\overline{CASL}$ controls DQ1 through DQ8, and $\overline{CASH}$ controls DQ9 through DQ16.

The MT4C16257 L and MT4C16259 L "$\overline{CAS}$" function is determined by the first $\overline{CAS}$ ($\overline{CASL}$ or $\overline{CASH}$) to transition LOW and the last one to transition back HIGH. The two $\overline{CAS}$ controls give the MT4C16257 L and MT4C16259 L both BYTE READ and BYTE WRITE cycle capabilities.

READ or WRITE cycles on the MT4C16257 L or MT4C16259 L are selected with the $\overline{WE}$ input while either $\overline{WEL}$ or $\overline{WEH}$ perform the "$\overline{WE}$" on the MT4C16256L or MT4C16258 L. The MT4C16256 L and MT4C16258 L "$\overline{WE}$" function is determined by the first BYTE WRITE ($\overline{WEL}$ or $\overline{WEH}$) to transition LOW and the last one to transition back HIGH.

A logic HIGH on $\overline{WE}$ dictates READ mode while a logic LOW on $\overline{WE}$ dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. Taking $\overline{WE}$ LOW will initiate a WRITE cycle, selecting DQ1 through DQ16. If $\overline{WE}$ goes LOW prior to $\overline{CAS}$ going LOW, the output pin(s) remain open (High- Z) until the next $\overline{CAS}$ cycle. If $\overline{WE}$ goes LOW after $\overline{CAS}$ goes LOW and data reaches the output pins, data out (Q) is activated and retains the selected cell data as long as $\overline{CAS}$ and $\overline{OE}$ remain LOW (regardless of $\overline{WE}$ or $\overline{RAS}$). This late $\overline{WE}$ pulse results in a READ-WRITE cycle.

The 16 data inputs and 16 data outputs are routed through 16 pins using common I/O, and pin direction is controlled by $\overline{OE}$, $\overline{WEL}$ and $\overline{WEH}$ (MT4C16256 L and MT4C16258 L) or $\overline{WE}$ (MT4C16257 L and MT4C16259 L).

FAST PAGE MODE operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row address (A0-A8) defined page boundary. The FAST PAGE MODE cycle is always initiated with a row address strobed-in by $\overline{RAS}$ followed by a column address strobed-in by $\overline{CAS}$. $\overline{CAS}$ may be toggled by holding $\overline{RAS}$ LOW and strobing-in different column addresses, thus executing faster memory cycles. Returning $\overline{RAS}$ HIGH terminates the FAST PAGE MODE operation.

Returning $\overline{RAS}$ and $\overline{CAS}$ HIGH terminates a memory cycle and decreases chip current to a reduced standby level. The chip is also preconditioned for the next cycle during the $\overline{RAS}$ high time. Memory cell data is retained in its correct state by maintaining power and executing any $\overline{RAS}$ cycle (READ, WRITE, $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$, or HIDDEN refresh) so that all 512 combinations of $\overline{RAS}$ addresses (A0-A8) are executed at least every 64ms, regardless of sequence. The $\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh cycle will also invoke the refresh counter and controller for ROW address control.

BATTERY BACKUP MODE (BBU) is a CBR refresh performed at the extended refresh rate with CMOS input levels. This mode provides a very low current, data retention cycle. $\overline{RAS}$ or $\overline{CAS}$ time refers to the time at which $\overline{RAS}$ or $\overline{CAS}$ transition from HIGH to LOW).

BYTE ACCESS CYCLE

The BYTE WRITE mode is determined by the use of $\overline{WEL}$ and $\overline{WEH}$ or $\overline{CASL}$ and $\overline{CASH}$. Enabling $\overline{WEL}$/$\overline{CASL}$ will select a lower BYTE WRITE cycle (DQ1-DQ8) while enabling $\overline{WEH}$ or $\overline{CASH}$ will select an upper BYTE WRITE cycle (DQ9-DQ16). Enabling both $\overline{WEL}$ and $\overline{WEH}$ or $\overline{CASL}$ and $\overline{CASH}$ selects a WORD WRITE cycle.

The MT4C16256 L, MT4C16257 L, MT4C16258 L and MT4C16259 L can be viewed as two 256K x 8 DRAMS which have common input controls, with the exception of the $\overline{WE}$ or the $\overline{CAS}$ inputs. Figure 1 illustrates the MT4C16256 L BYTE WRITE and WORD WRITE cycles and Figure 2 illustrates the MT4C16257 L BYTE WRITE and WORD WRITE cycles.

The MT4C16257 L also has BYTE READ and WORD READ cycles, since it uses two $\overline{CAS}$ inputs to control its byte accesses. Figure 3 illustrates the MT4C16257 L BYTE READ and WORD READ cycles.

MASKED WRITE ACCESS CYCLE (MT4C16258/9 L Only)

The MASKED WRITE mode control input selects normal WRITE access or MASKED WRITE access cycles. Every WRITE access cycle can be a MASKED WRITE, depending on the state of $\overline{WE}$ at $\overline{RAS}$ time. A MASKED WRITE is selected when mask data is supplied on the DQ pins and $\overline{WE}$ is LOW at $\overline{RAS}$ time. The MT4C16256 L and MT4C16257 L do not have the MASKED WRITE cycle function.

The data (mask data) present on the DQ1-DQ16 inputs at $\overline{RAS}$ time will be written to an internal bit mask data register and will then act as an individual write enable for each of the corresponding DQ inputs. If a LOW (logic "0") is written to a mask data register bit, the input port for that bit is disabled during the subsequent WRITE operation and no new data will be written to that DRAM cell location. A HIGH (logic "1") on a mask data register bit enables the input port and allows normal WRITE operations to proceed. At $\overline{CAS}$ time, the bits present on the DQ1-DQ16 inputs will be either written to the DRAM (if the mask data bit was HIGH) or ignored (if the mask data bit was LOW).

New mask data must be supplied each time a MASKED WRITE cycle is initiated (non-persistent), even if the previous cycle's mask was the same mask.

Figure 4 illustrates the MT4C16258 L MASKED WRITE operation and Figure 5 illustrates the MT4C16259 L MASKED WRITE operation.

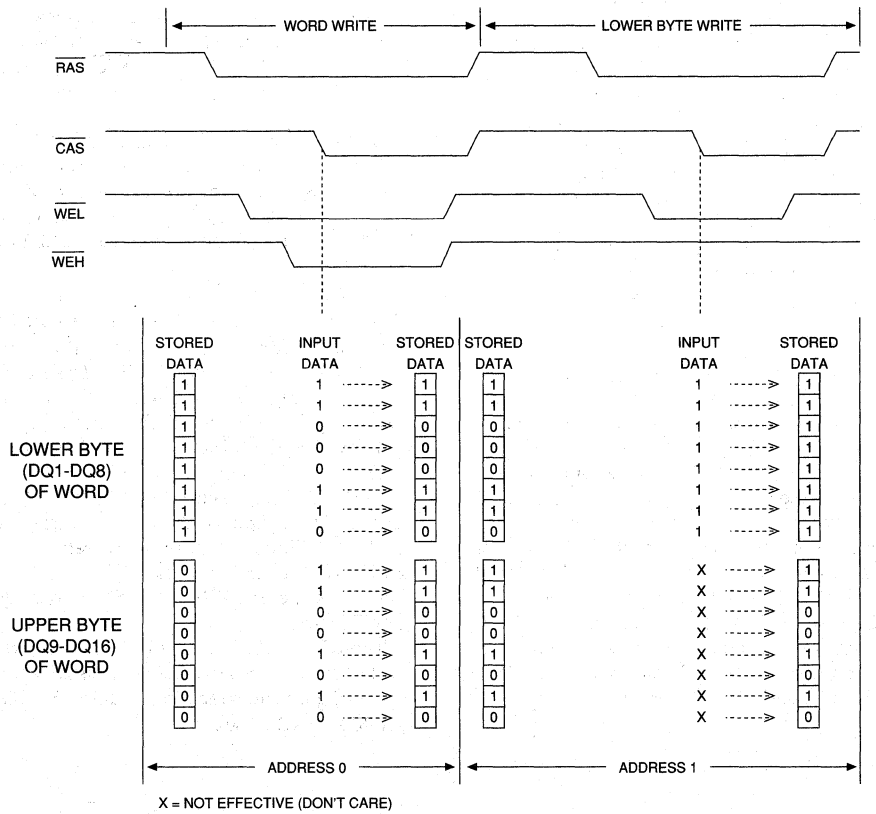


Figure 1
MT4C16256/8 L WORD AND BYTE WRITE EXAMPLE

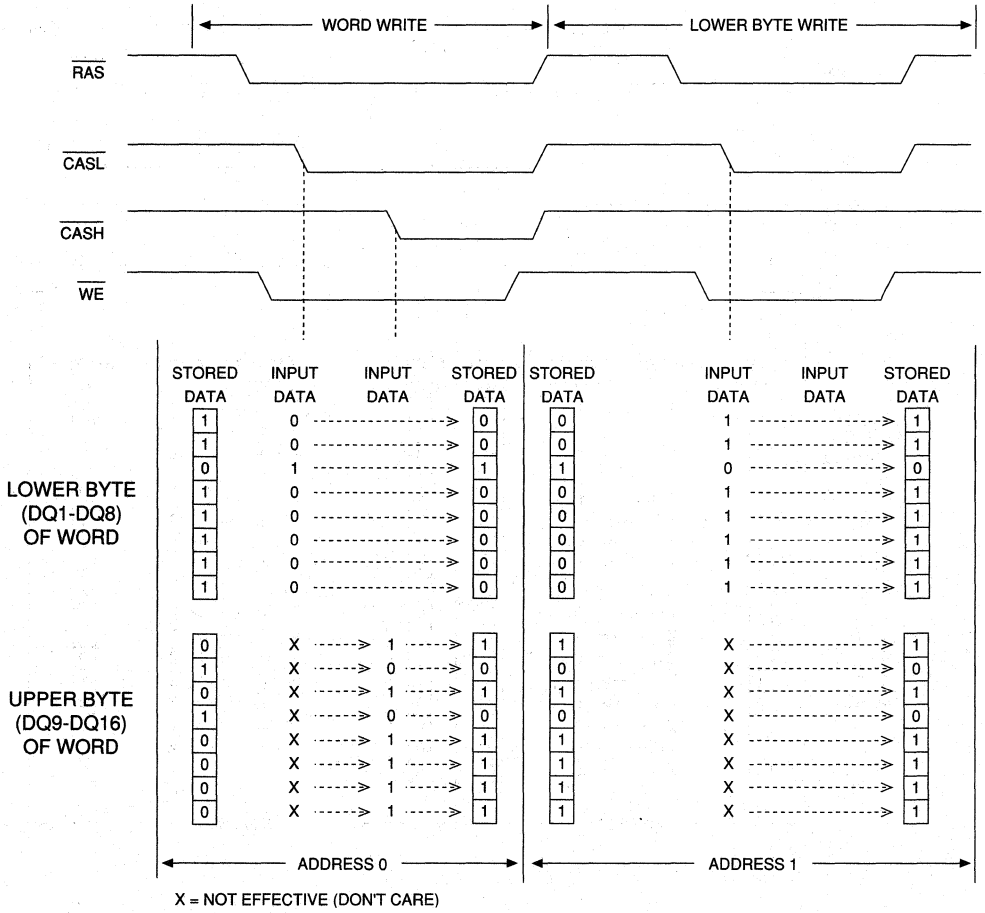


Figure 2
MT4C16257/9 L WORD AND BYTE WRITE EXAMPLE

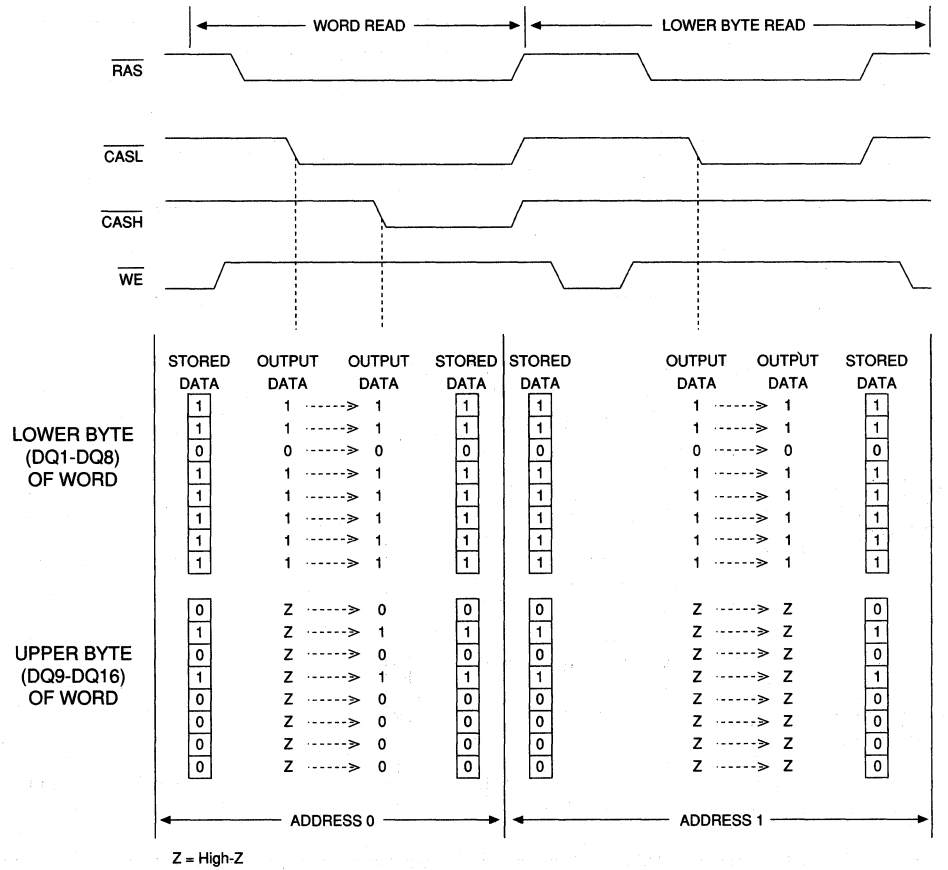


Figure 3
MT4C16257/9 L WORD AND BYTE READ EXAMPLE

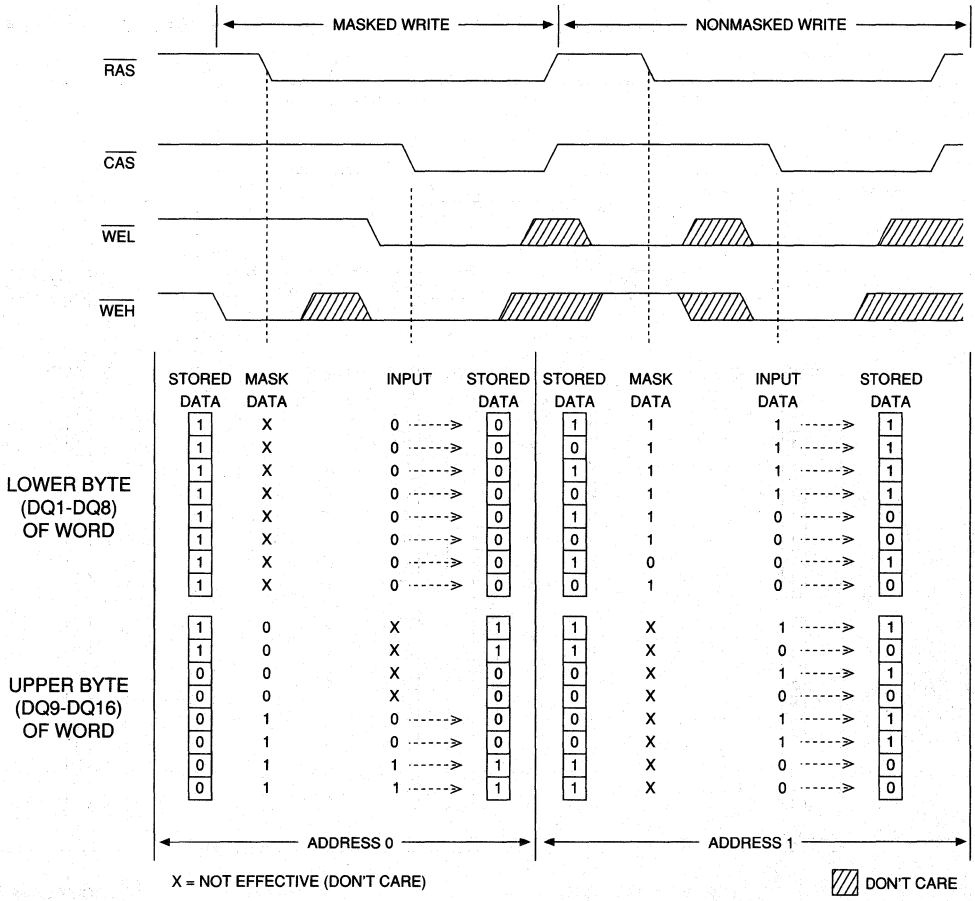


Figure 4
MT4C16258 L MASKED WRITE EXAMPLE

NEW ■ WIDE DRAM

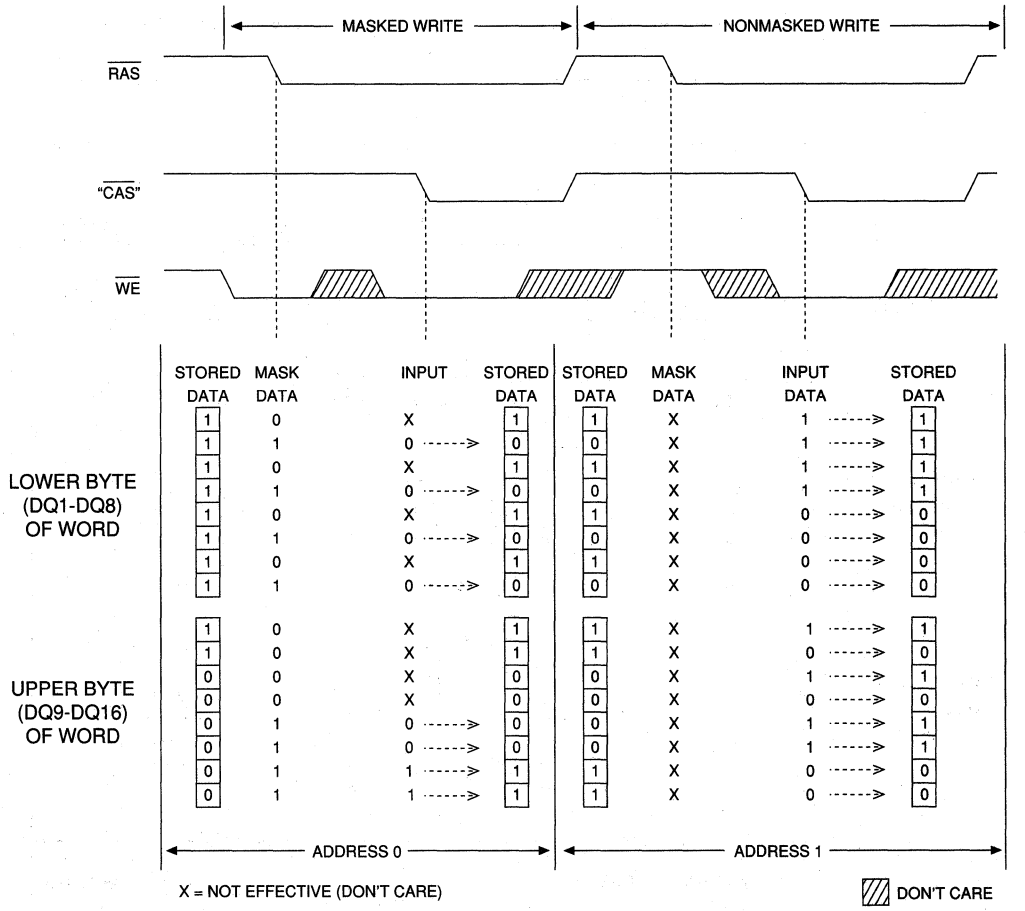


Figure 5
MT4C16259 L MASKED WRITE EXAMPLE

TRUTH TABLE: MT4C16256/8 L

FUNCTION		RAS	CAS	WEL	WEH	OE	ADDRESSES tR	ADDRESSES tC	DQs	NOTES
Standby		H	H→X	X	X	X	X	X	High-Z	
READ		L	L	H	H	L	ROW	COL	Data Out	
WRITE: WORD (EARLY-WRITE)		L	L	L	L	X	ROW	COL	Data In	3
WRITE: LOWER BYTE (EARLY)		L	L	L	H	X	ROW	COL	Lower Byte, Data In Upper Byte, High-Z	3
WRITE: UPPER BYTE (EARLY)		L	L	H	L	X	ROW	COL	Lower Byte, High-Z Upper Byte, Data In	3
READ-WRITE		L	L	H→L	H→L	L→H	ROW	COL	Data Out, Data In	1, 3
PAGE-MODE READ	1st Cycle	L	H→L	H	H	L	ROW	COL	Data Out	
	2nd Cycle	L	H→L	H	H	L	n/a	COL	Data Out	
PAGE-MODE WRITE	1st Cycle	L	H→L	L	L	X	ROW	COL	Data In	1, 3
	2nd Cycle	L	H→L	L	L	X	n/a	COL	Data In	1, 3
PAGE-MODE READ-WRITE	1st Cycle	L	H→L	H→L	H→L	L→H	ROW	COL	Data In	1, 3
	2nd Cycle	L	H→L	H→L	H→L	L→H	n/a	COL	Data Out, Data In	1, 3
HIDDEN REFRESH	READ	L→H→L	L	H	H	L	ROW	COL	Data Out	
	WRITE	L→H→L	L	L	L	X	ROW	COL	Data In	1, 2, 3
RAS-ONLY REFRESH		L	H	H	H	X	ROW	n/a	High-Z	
CAS-BEFORE-RAS REFRESH		H→L	L	H	H	X	X	X	High-Z	
BATTERY BACKUP REFRESH		H→L	L	H	H	X	X	X	High-Z	

NOTE: 1. These cycles may also be BYTE WRITE cycles (either WEL or WEH active).
2. EARLY-WRITE only.
3. Data-in will be dependent on the mask provided (MT4C16258 L only). Refer to Figure 4.

NEW ■ WIDE DRAM

TRUTH TABLE: MT4C16257/9 L

FUNCTION		RAS	CASL	CASH	WE	OE	ADDRESSES tR	ADDRESSES tC	DQs	NOTES
Standby		H	H→X	H→X	X	X	X	X	High-Z	
READ: WORD		L	L	L	H	L	ROW	COL	Data Out	
READ: LOWER BYTE		L	L	H	H	L	ROW	COL	Lower Byte, Data Out Upper Byte, High-Z	
READ: UPPER BYTE		L	H	L	H	L	ROW	COL	Lower Byte, High-Z Upper Byte, Data Out	
WRITE: WORD (EARLY-WRITE)		L	L	L	L	X	ROW	COL	Data In	5
WRITE: LOWER BYTE (EARLY)		L	L	H	L	X	ROW	COL	Lower Byte, Data In Upper Byte, High-Z	5
WRITE: UPPER BYTE (EARLY)		L	H	L	L	X	ROW	COL	Lower Byte, High-Z Upper Byte, Data In	5
READ-WRITE		L	L	L	H→L	L→H	ROW	COL	Data Out, Data In	1, 2, 5
PAGE-MODE READ	1st Cycle	L	H→L	H→L	H	L	ROW	COL	Data Out	2
	2nd Cycle	L	H→L	H→L	H	L	n/a	COL	Data Out	2
PAGE-MODE WRITE	1st Cycle	L	H→L	H→L	L	X	ROW	COL	Data In	1, 5
	2nd Cycle	L	H→L	H→L	L	X	n/a	COL	Data In	1, 5
PAGE-MODE READ-WRITE	1st Cycle	L	H→L	H→L	H→L	L→H	ROW	COL	Data Out, Data In	1, 2, 5
	2nd Cycle	L	H→L	H→L	H→L	L→H	n/a	COL	Data Out, Data In	1, 2, 5
HIDDEN REFRESH	READ	L→H→L	L	L	H	L	ROW	COL	Data Out	2
	WRITE	L→H→L	L	L	L	X	ROW	COL	Data In	1, 3, 5
RAS-ONLY REFRESH		L	H	H	X	X	ROW	n/a	High-Z	
CAS-BEFORE-RAS REFRESH		H→L	L	L	H	X	X	X	High-Z	4
BATTERY BACKUP REFRESH		H→L	L	L	H	X	X	X	High-Z	4

NOTE:
1. These WRITE cycles may also be BYTE WRITE cycles (either CASL or CASH active).
2. These READ cycles may also be BYTE READ cycles (either CASL or CASH active).
3. EARLY-WRITE only.
4. Only one of the two CAS must be active (CASL or CASH).
5. Data-in will be dependent on the mask provided (MT4C16259 L only). Refer to Figure 5.

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS} ..... -1V to +7V
Operating Temperature, T_A (Ambient) ..... 0°C to +70°C
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 3, 4, 6, 7) (0°C ≤ T_A ≤ 70°C; V_{CC} = 5V ±10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.5	V	1
Input High (Logic 1) Voltage, All Inputs	V_{IH}	2.4	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, All Inputs	V_{IL}	-1.0	0.8	V	1
INPUT LEAKAGE CURRENT Any Input 0V ≤ V_{IN} ≤ V_{CC} (All other pins not under test = 0V)	I_I	-2	2	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled, 0V ≤ V_{OUT} ≤ 5.5V)	I_{OZ}	-10	10	µA	
OUTPUT LEVELS Output High Voltage (I_{OUT} = -5mA)	V_{OH}	2.4		V	
Output Low Voltage (I_{OUT} = 4.2mA)	V_{OL}		0.4	V	

		MAX				
PARAMETER/CONDITION	SYMBOL	-7	-8	-10	UNITS	NOTES
STANDBY CURRENT: (TTL) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC1}	2	2	2	mA	
STANDBY CURRENT: (CMOS) ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} -0.2V)	I_{CC2}	200	200	200	µA	25
OPERATING CURRENT: Random READ/WRITE Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC (MIN))	I_{CC3}	160	140	120	mA	3, 4 43
OPERATING CURRENT: FAST PAGE MODE Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: ^tPC = ^tPC (MIN); ^tCP, ^tASC = 10ns)	I_{CC4}	120	110	100	mA	3, 4 43
REFRESH CURRENT: $\overline{RAS}$-ONLY Average power supply current ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}: ^tRC = ^tRC (MIN))	I_{CC5}	160	140	120	mA	3, 5 43
REFRESH CURRENT: $\overline{CAS}$-BEFORE-$\overline{RAS}$ Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC (MIN))	I_{CC6}	160	140	120	mA	3, 5
REFRESH CURRENT: BATTERY BACKUP (BBU) Average power supply current during BATTERY BACKUP refresh: $\overline{CAS}$ = 0.2V or $\overline{CAS}$-BEFORE-$\overline{RAS}$ cycling; $\overline{RAS}$ = ^tRAS (MIN) to 300ns; $\overline{WE}$, A0-A9 and D_{IN} = V_{CC} - 0.2V (D_{IN} may be left open), ^tRC = 125µs (512 rows at 125µs = 64ms)	I_{CC7}	300	300	300	µA	3, 5 42

CAPACITANCE

(Note: 2)

PARAMETER	SYMBOL	MAX	UNITS	NOTES
Input Capacitance: A0-A8	C_{I1}	5	pF	2
Input Capacitance: $\overline{RAS}$, $\overline{CAS}$/($\overline{CASL}$,$\overline{CASH}$), ($\overline{WEL}$, $\overline{WEH}$)/ $\overline{WE}$, $\overline{OE}$	C_{I2}	7	pF	2
Input/Output Capacitance: DQ	C_{IO}	7	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C ≤ T_A ≤ +70°C; Vcc = 5V ±10%)

AC CHARACTERISTICS		-7		-8		-10			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	^tRC	130		150		180		ns	
READ-WRITE cycle time	^tRWC	180		200		245		ns	
FAST-PAGE-MODE READ or WRITE cycle time	^tPC	45		50		55		ns	35
FAST-PAGE-MODE READ-WRITE cycle time	^tPRWC	95		100		110		ns	35
Access time from $\overline{RAS}$	^tRAC		70		80		100	ns	14
Access time from $\overline{CAS}$	^tCAC		20		20		25	ns	15, 33
Output Enable time	^tOE		20		20		25	ns	33
Access time from column address	^tAA		35		40		45	ns	
Access time from $\overline{CAS}$ precharge	^tCPA		40		45		55	ns	33
$\overline{RAS}$ pulse width	^tRAS	70	100,000	80	100,000	100	100,000	ns	
$\overline{RAS}$ pulse width (PAGE MODE)	^tRASP	70	100,000	80	100,000	100	100,000	ns	
$\overline{RAS}$ hold time	^tRSH	20		20		25		ns	40
$\overline{RAS}$ precharge time	^tRP	50		60		70		ns	
$\overline{CAS}$ pulse width	^tCAS	20	100,000	20	100,000	25	100,000	ns	39
$\overline{CAS}$ hold time	^tCSH	70		80		100		ns	32
$\overline{CAS}$ precharge time	^tCPN	10		10		10		ns	16, 36
$\overline{CAS}$ precharge time (PAGE MODE)	^tCP	10		10		10		ns	36
$\overline{RAS}$ to $\overline{CAS}$ delay time	^tRCD	20	50	20	60	25	75	ns	17, 31
$\overline{CAS}$ to $\overline{RAS}$ precharge time	^tCRP	10		10		10		ns	32
Row address setup time	^tASR	0		0		0		ns	
Row address hold time	^tRAH	10		10		15		ns	
$\overline{RAS}$ to column address delay time	^tRAD	15	35	15	40	20	55	ns	18
Column address setup time	^tASC	0		0		0		ns	31
Column address hold time	^tCAH	15		15		20		ns	31
Column address hold time (referenced to $\overline{RAS}$)	^tAR	55		60		75		ns	
Column address to $\overline{RAS}$ lead time	^tRAL	35		40		55		ns	
Read command setup time	^tRCS	0		0		0		ns	26, 31
Read command hold time (referenced to $\overline{CAS}$)	^tRCH	0		0		0		ns	19, 26 ,32
Read command hold time (referenced to $\overline{RAS}$)	^tRRH	0		0		0		ns	19
$\overline{CAS}$ to output in Low-Z	^tCLZ	0		0		0		ns	33

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) ($0°C \le T_A \le +70°C$; V_{CC} = 5V ±10%)

AC CHARACTERISTICS		-7		-8		-10			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Output buffer turn-off delay	^tOFF	0	15	0	15	0	20	ns	20, 29, 33
Output disable time	^tOD		15		15		20	ns	29, 41
Write command setup time	^tWCS	0		0		0		ns	21, 26, 31
Write command hold time	^tWCH	15		15		20		ns	26, 40
Write command hold time (referenced to $\overline{RAS}$)	^tWCR	55		60		75		ns	26
Write command pulse width	^tWP	10		10		20		ns	26
Write command to $\overline{RAS}$ lead time	^tRWL	20		20		25		ns	26
Write command to $\overline{CAS}$ lead time	^tCWL	20		20		25		ns	26, 32
Data-in setup time	^tDS	0		0		0		ns	22, 33
Data-in hold time	^tDH	15		15		20		ns	22, 33
Data-in hold time (referenced to $\overline{RAS}$)	^tDHR	55		60		75		ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	^tRWD	95		105		135		ns	21
Column address to $\overline{WE}$ delay time	^tAWD	60		65		80		ns	21
$\overline{CAS}$ to $\overline{WE}$ delay time	^tCWD	45		45		60		ns	21, 31
Transition time (rise or fall)	^tT	3	50	3	50	3	50	ns	9, 10
Refresh period (512 cycles)	^tREF		64		64		64	ms	28
$\overline{RAS}$ to $\overline{CAS}$ precharge time	^tRPC	10		10		10		ns	
$\overline{CAS}$ setup time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tCSR	10		10		10		ns	5, 31
$\overline{CAS}$ hold time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tCHR	10		10		10		ns	5, 32
MASKED WRITE command to $\overline{RAS}$ setup time	^tWRS	0		0		0		ns	26, 27
$\overline{WE}$ hold time (MASKED WRITE and $\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tWRH	15		15		15		ns	26
Mask data to $\overline{RAS}$ setup time	^tMS	0		0		0		ns	26, 27
Mask data to $\overline{RAS}$ hold time	^tMH	15		15		15		ns	26, 27
$\overline{OE}$ hold time from $\overline{WE}$ during READ-MODIFY-WRITE cycle	^tOEH	20		20		25		ns	28
$\overline{OE}$ setup prior to $\overline{RAS}$ during HIDDEN REFRESH cycle	^tORD	0		0		0		ns	
Last $\overline{CAS}$ going LOW to first $\overline{CAS}$ to return HIGH	^tCLCH	10		10		10		ns	34
$\overline{WE}$ setup time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tWRP	10		10		10		ns	

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NOTES

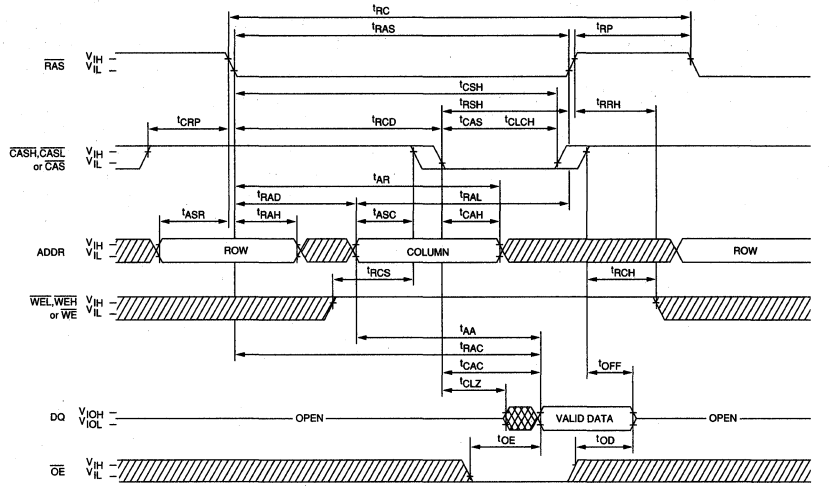
1. All voltages referenced to V_{SS}.
2. This parameter is sampled. V_{CC} = 5V ±10%, f = 1 MHz.
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \le T_A \le 70°C$) is assured.
7. An initial pause of 100µs is required after power-up followed by eight $\overline{RAS}$ refresh cycles ($\overline{RAS}$-ONLY or CBR) before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-up should be repeated any time the ^tREF refresh requirement is exceeded.
8. AC characteristics assume ^tT = 5ns.
9. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS}$ = V_{IH}, data output is High-Z.
12. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to 2 TTL gate and 100pF.
14. Assumes that $^tRCD < ^tRCD$ (MAX). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
15. Assumes that $^tRCD \ge ^tRCD$ (MAX).
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the Q buffer, $\overline{CAS}$ must be pulsed HIGH for ^tCPN.
17. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (MAX) limit, then access time is controlled exclusively by ^tCAC.
18. Operation within the ^tRAD limit ensures that ^tRCD (MAX) can be met. ^tRAD (MAX) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (MAX) limit, then access time is controlled exclusively by ^tAA.
19. Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
20. ^tOFF (MAX) defines the time at which the output achieves the open circuit condition, not a reference to V_{OH} or V_{OL}.
21. ^tWCS, ^tRWD, ^tAWD and ^tCWD are restrictive operating parameters in LATE-WRITE and READ-MODIFY-WRITE cycles only. If $^tWCS \ge ^tWCS$ (MIN), the cycle is an EARLY-WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If $^tRWD \ge ^tRWD$ (MIN), $^tAWD \ge ^tAWD$ (MIN) and $^tCWD \ge ^tCWD$ (MIN), the cycle is a READ-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of Q (at access time and until $\overline{CAS}$ or $\overline{OE}$ goes back to V_{IH}) is indeterminate. $\overline{OE}$ held HIGH and $\overline{WE}$ taken LOW after $\overline{CAS}$ goes LOW results in a LATE-WRITE ($\overline{OE}$ controlled) cycle.
22. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY-WRITE cycles and $\overline{WE}$ leading edge in LATE-WRITE or READ-MODIFY-WRITE cycles.
23. During a READ cycle, if $\overline{OE}$ is LOW then taken HIGH before $\overline{CAS}$ goes HIGH, Q goes open. If $\overline{OE}$ is tied permanently LOW, a LATE-WRITE or READ-MODIFY-WRITE operation is not possible.
24. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW and $\overline{OE}$ = HIGH.
25. All other inputs at Vcc -0.2V.
26. Write command is defined as either $\overline{WEL}$ or $\overline{WEH}$ or both going LOW on the MT4C16256/8 L. Write command is defined as $\overline{WE}$ going LOW on the MT4C16257/9 L.
27. MT4C16258/9 L only.
28. LATE-WRITE and READ-MODIFY-WRITE cycles must have both ^tOD and ^tOEH met ($\overline{OE}$ HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. The DQs will provide the previously read data if $\overline{CAS}$ remains LOW and $\overline{OE}$ is taken back LOW after ^tOEH is met. If $\overline{CAS}$ goes HIGH prior to $\overline{OE}$ going back LOW, the DQs will remain open.
29. The DQs open during READ cycles once ^tOD or ^tOFF occur. If $\overline{CAS}$ goes HIGH first, $\overline{OE}$ becomes a "don't care." If $\overline{OE}$ goes HIGH and $\overline{CAS}$ stays LOW, $\overline{OE}$ is not a "don't care;" and the DQs will provide the previously read data if $\overline{OE}$ is taken back LOW (while $\overline{CAS}$ remains LOW).

NOTES (continued)

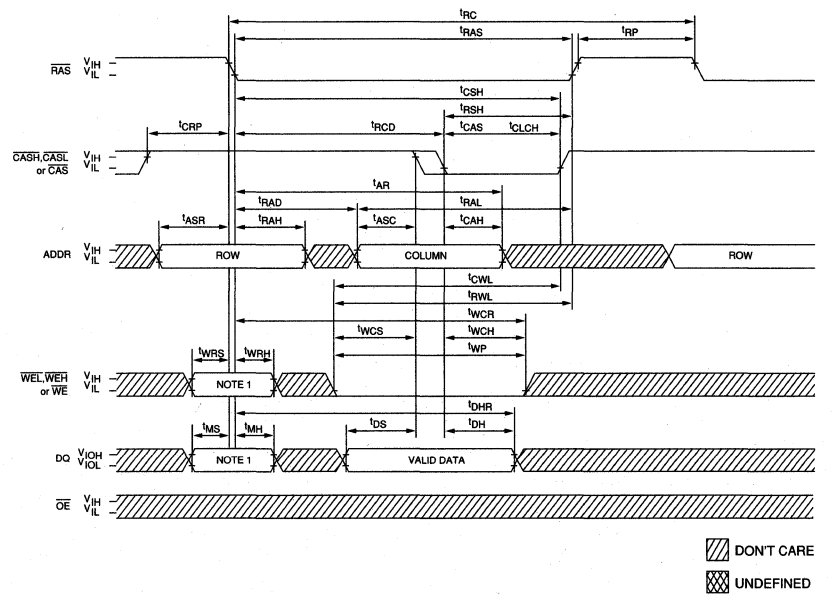
30. Notes 31 through 41 apply to MT4C16257/9 L only (*):
31. *The first $\overline{CAS}$x edge to transition LOW.
32. *The last $\overline{CAS}$x edge to transition HIGH.
33. *Output parameter (DQx) is referenced to corresponding $\overline{CAS}$ input; DQ1-DQ8 by $\overline{CASL}$ and DQ9-DQ16 by $\overline{CASH}$.
34. *Last falling $\overline{CAS}$x edge to first rising $\overline{CAS}$x edge.
35. *Last rising $\overline{CAS}$x edge to next cycle's last rising $\overline{CAS}$x edge.
36. *Last rising $\overline{CAS}$x edge to first falling $\overline{CAS}$x edge.
37. *First DQs controlled by the first $\overline{CAS}$x to go LOW.
38. *Last DQs controlled by the last $\overline{CAS}$x to go HIGH.
39. *Each $\overline{CAS}$x must meet minimum pulse width.
40. *Last $\overline{CAS}$x to go LOW.
41. *All DQs controlled, regardless $\overline{CASL}$ and $\overline{CASH}$.
42. BBU current is reduced as ^{t}RAS is reduced from its maximum specification during the BBU cycle.
43. Column address changed once while $\overline{RAS}$ = V_{IL} and $\overline{CAS}$ = V_{IH}.

NEW ■ WIDE DRAM

READ CYCLE

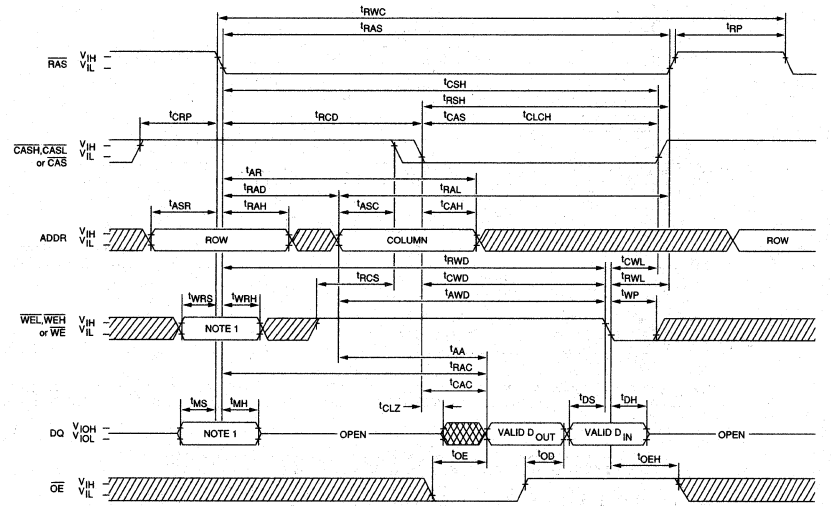


EARLY-WRITE CYCLE

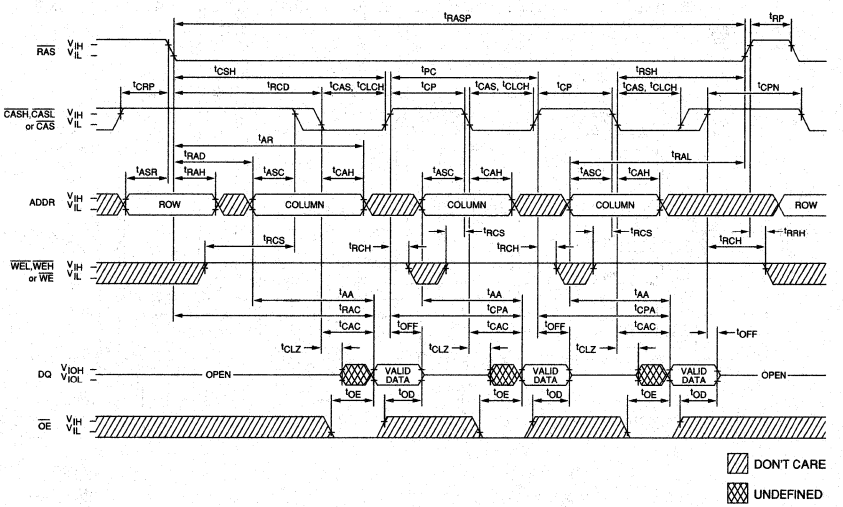


NOTE: 1. Applies to MT4C16258 L and MT4C16259 L only. $\overline{WE}$ selects between normal WRITE and MASKED WRITE at $\overline{RAS}$ time. The DQ inputs are "don't care" for a normal WRITE ($\overline{WE}$ HIGH at $\overline{RAS}$ time). The DQ inputs provide the mask data at $\overline{RAS}$ time for a MASKED WRITE ($\overline{WE}$ LOW at $\overline{RAS}$ time). $\overline{WEL}$, $\overline{WEH}$ and DQ inputs on MT4C16256L and MT4C16257 L are "don't care" at $\overline{RAS}$ time.

READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)

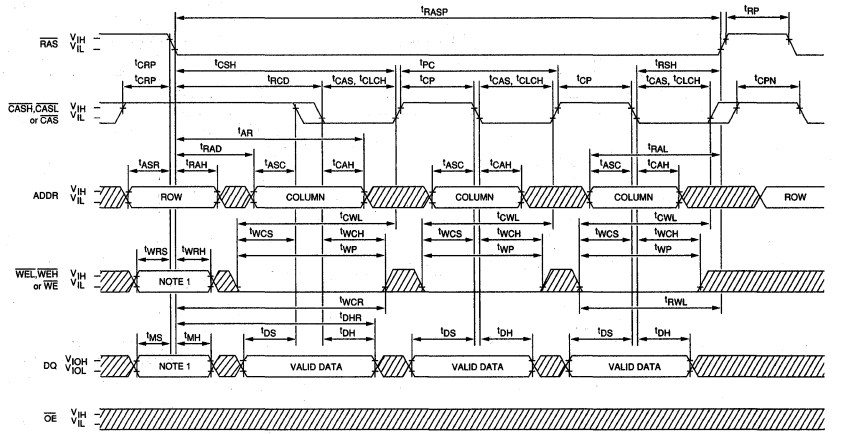


FAST-PAGE-MODE READ CYCLE

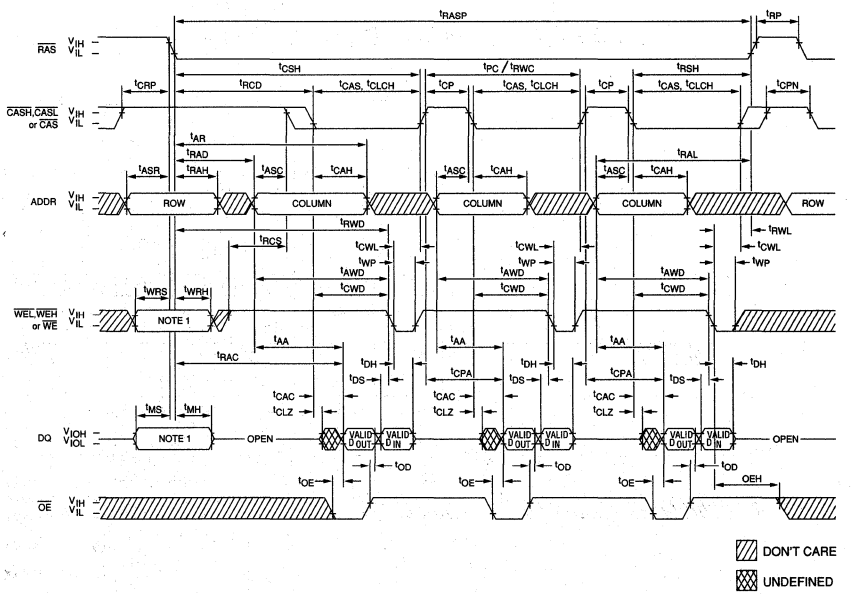


NOTE: 1. Applies to MT4C16258 L and MT4C16259 L only. $\overline{WE}$ selects between normal WRITE and MASKED WRITE at $\overline{RAS}$ time. The DQ inputs are "don't care" for a normal WRITE ($\overline{WE}$ HIGH at $\overline{RAS}$ time). The DQ inputs provide the mask data at $\overline{RAS}$ time for a MASKED WRITE ($\overline{WE}$ LOW at $\overline{RAS}$ time). $\overline{WEL}$, $\overline{WEH}$ and DQ inputs on MT4C16256 L and MT4C16257 L are "don't care" at $\overline{RAS}$ time.

FAST-PAGE-MODE EARLY-WRITE CYCLE



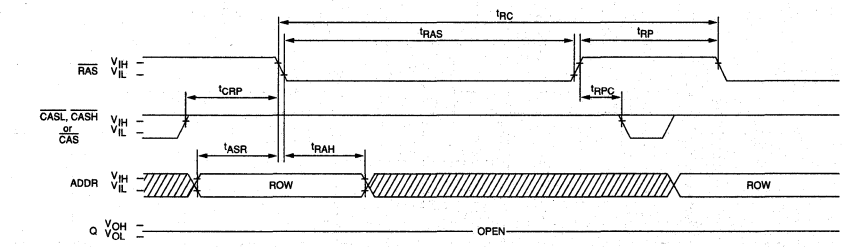
FAST-PAGE-MODE READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)



NOTE: 1. Applies to MT4C16258 L and MT4C16259 L only. $\overline{WE}$ selects between normal WRITE and MASKED WRITE at $\overline{RAS}$ time. The DQ inputs are "don't care" for a normal WRITE ($\overline{WE}$ HIGH at $\overline{RAS}$ time). The DQ inputs provide the mask data at $\overline{RAS}$ time for a MASKED WRITE ($\overline{WE}$ LOW at $\overline{RAS}$ time). $\overline{WEL}$, $\overline{WEH}$ and DQ inputs on MT4C16256 L and MT4C16257 L are "don't care" at $\overline{RAS}$ time.

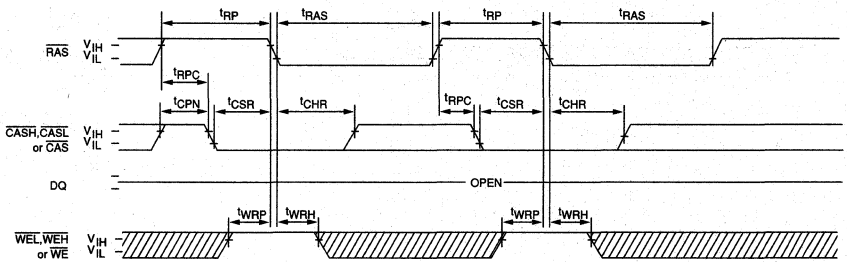
RAS-ONLY REFRESH CYCLE

(ADDR = A0-A8, OE; WEL, WEH or WE = DON'T CARE)



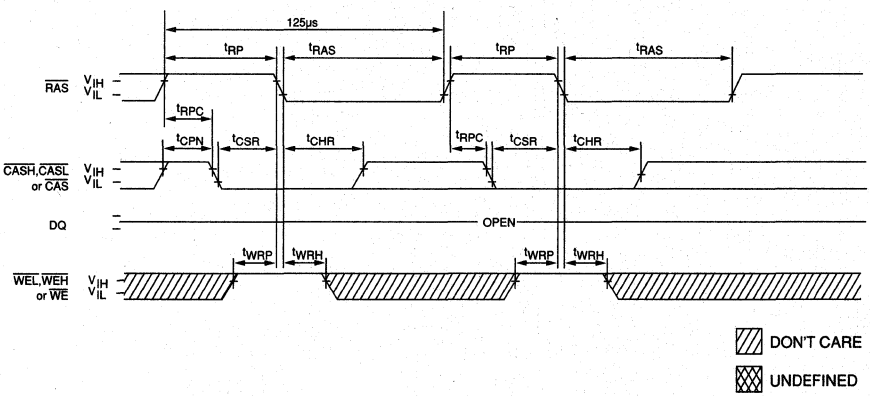
CAS-BEFORE-RAS REFRESH CYCLE

(A0-A8; and OE = DON'T CARE)

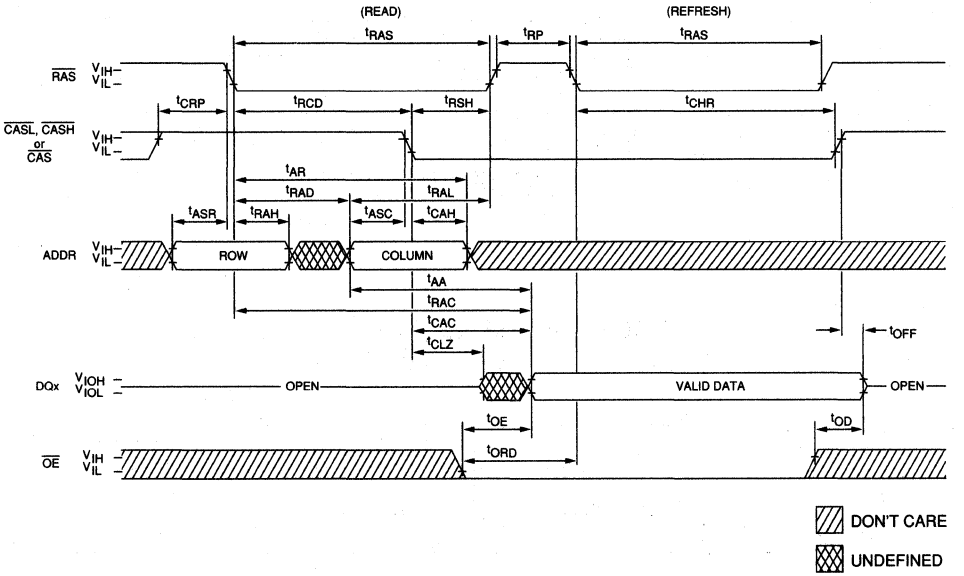


BATTERY BACKUP REFRESH CYCLE

(A0-A8; and OE = DON'T CARE)



HIDDEN REFRESH CYCLE[24]
(WEL, WEH or WE = HIGH; OE = LOW)



NEW ■ WIDE DRAM

DRAM

256K x 16 DRAM

ASYMMETRICAL, FAST PAGE MODE

FEATURES

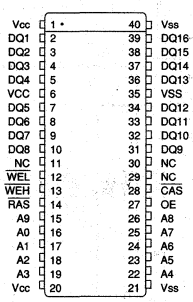
- Industry standard x16 pinouts, timing, functions and packages
- Address entry: 10 row addresses, eight column addresses
- High-performance, CMOS silicon-gate process
- Single +5V±10% power supply
- Low power, 3mW standby; 500mW active, typical
- All device pins are fully TTL compatible
- 1,024 cycle refresh in 16ms
- Refresh modes: $\overline{RAS}$ ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$ (CBR) and HIDDEN
- Optional FAST-PAGE-MODE access cycle, 256 locations wide
- BYTE WRITE access cycle
- NONPERSISTENT MASKED WRITE access cycle (MT4C16261 only)

OPTIONS

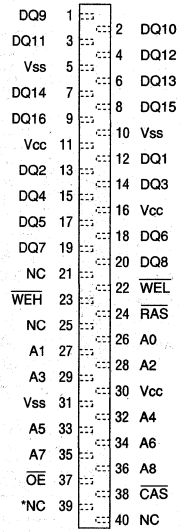
OPTIONS	MARKING
• Timing	
70ns access	- 7
80ns access	- 8
100ns access	-10
• Masked Write	
Not Available	MT4C16260
Available	MT4C16261
• Packages	
Plastic SOJ (400mil)	DJ
Plastic TSOP (400mil)	TG
Plastic ZIP (475mil)	Z

PIN ASSIGNMENT (Top View)

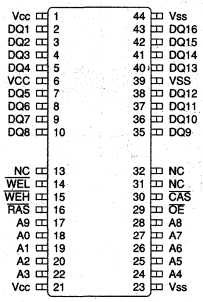
40-Pin SOJ (Q-6)



40-Pin ZIP (O-4)



40-Pin TSOP (R-5)



GENERAL DESCRIPTION

The MT4C16260 and MT4C16261 are randomly accessed solid-state memories containing 4,194,304 bits organized in a x16 configuration. Each word or byte is uniquely addressed through the 18 address bits during READ or WRITE cycles. These are entered 10 bits (A0-A9) first, then eight bits second (A0-A7). $\overline{RAS}$ is used to latch the first 10 bits and $\overline{CAS}$ the latter eight bits.

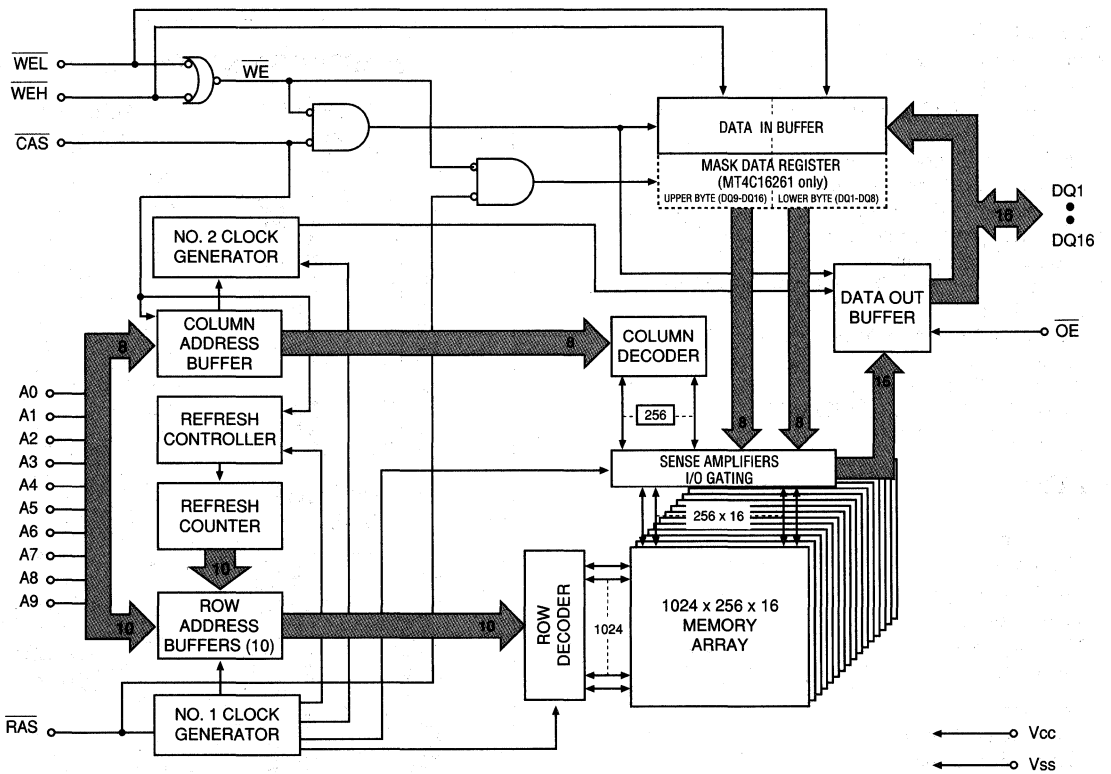
The MT4C16260 and MT4C16261 have both BYTE WRITE and WORD WRITE access cycles via two write enable pins. The MT4C16261 is able to perform WRITE-PER-BIT accesses.

The MT4C16260 and MT4C16261 function in the same manner in that $\overline{WEL}$ and $\overline{WEH}$ control the selection of BYTE WRITE access cycles. $\overline{WEL}$ and $\overline{WEH}$ function identically to $\overline{WE}$ in that either $\overline{WEL}$ or $\overline{WEH}$ will generate an internal $\overline{WE}$.

The $\overline{WE}$ function and timing are determined by the first $\overline{WE}$ ($\overline{WEL}$ or $\overline{WEH}$) to transition LOW and by the last to transition back HIGH. Use of only one of the two results in a BYTE WRITE cycle. $\overline{WEL}$ transitioning LOW selects a WRITE cycle for the lower byte (DQ1-DQ8) and $\overline{WEH}$ transitioning LOW selects a WRITE cycle for the upper byte (DQ9-DQ16).

The MT4C16261 has NONPERSISTENT, MASKED WRITE capability.

FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTIONS

SOJ PINS	TSOP PINS	ZIP PINS	SYMBOL	TYPE	DESCRIPTION
14	16	24	$\overline{RAS}$	Input	ROW Address Strobe: $\overline{RAS}$ is used to latch in the 9 row-address bits and strobe the $\overline{WE}$ and DQs on the MASKED WRITE option.
28	30	38	$\overline{CAS}$	Input	Column Address Strobe: $\overline{CAS}$ is used to latch-in the 9 column-address bits, enable the DRAM output buffers, and strobe the data inputs on WRITE cycles. $\overline{CAS}$ controls DQ1 through DQ16.
27	29	37	$\overline{OE}$	Input	Output Enable: $\overline{OE}$ enables the output buffers when taken LOW during a READ access cycle. $\overline{RAS}$ and $\overline{CAS}$ must be LOW and $\overline{WEL}$ / $\overline{WEH}$ HIGH before $\overline{OE}$ will control the output buffers. Otherwise, the output buffers are in a High-Z state.
13	15	23	$\overline{WEH}$	Input	Write Enable Upper Byte: $\overline{WEH}$ is $\overline{WE}$ control for the DQ9 through DQ16 inputs. If $\overline{WE}$ or $\overline{WEH}$ is LOW, the access is a WRITE cycle. If either $\overline{WE}$ or $\overline{WEH}$ is LOW at $\overline{RAS}$ time on MT4C16261, then it is also a MASKED WRITE cycle. The DQs for the byte not being written will remain in a High-Z state (BYTE WRITE cycle only).
12	14	22	$\overline{WEL}$	Input	Write Enable Lower Byte: $\overline{WEL}$ is the $\overline{WE}$ control for DQ1 through DQ8 inputs. If $\overline{WEL}$ is LOW, the access is a WRITE cycle. If $\overline{WEL}$ is LOW at $\overline{RAS}$ time on MT4C16261, then it is also a MASKED WRITE cycle. The DQs for the byte not being written will remain in a High-Z state (BYTE WRITE cycle only).
16-19, 22-26	18-21, 24-28	26-29, 32-36	A0-A8	Input	Address Inputs: These inputs are multiplexed and clocked by $\overline{RAS}$ and $\overline{CAS}$ to select one 16-bit word (or 8-bit byte) out of the 256K available words.
2-5, 7-10, 31-34, 36-39	2-5, 7-10, 35-38, 40-43	12-15, 17-20, 1-4, 6-9	DQ1-DQ16	Input/ Output	Data I/O: For WRITE cycles, DQ1-DQ16 act as inputs to the addressed DRAM location. BYTE WRITEs can be performed by using $\overline{WEL}$ / $\overline{WEH}$ to select the byte to be written. For READ access cycles, DQ1-DQ16 act as outputs for the addressed DRAM Location. All sixteen I/Os are active for READ cycles.
11, 15, 30, 29	13, 17, 31	21, 25, 40, 39	NC	-	No Connect: These pins should be either left unconnected or tied to ground.
1, 6, 20	1, 6, 22	11, 16, 30	Vcc	Supply	Power Supply: +5V ±10%
21, 35, 40	23, 39, 44	5, 10, 31	Vss	Supply	Ground

NEW ■ WIDE DRAM

FUNCTIONAL DESCRIPTION

Each bit is uniquely addressed through the 18 address bits during READ or WRITE cycles. $\overline{RAS}$ is used to latch the first 10 bits (A0-A9) and $\overline{CAS}$ the latter 8 bits (A0-A7).

The $\overline{CAS}$ control also determines whether the cycle will be a refresh cycle ($\overline{RAS}$-ONLY) or an active cycle (READ, WRITE or READ-WRITE) once $\overline{RAS}$ goes LOW.

A READ or WRITE cycle is selected with either $\overline{WEL}$ or $\overline{WEH}$ performing the "$\overline{WE}$" function. The "$\overline{WE}$" function is determined by the first BYTE WRITE ($\overline{WEL}$ or $\overline{WEH}$) to transition LOW and the last one to transition back HIGH.

A logic HIGH on $\overline{WE}$ dictates READ mode while a logic LOW on $\overline{WE}$ dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. Taking $\overline{WE}$ LOW will initiate a WRITE cycle, selecting DQ1 through DQ16. If $\overline{WE}$ goes LOW prior to $\overline{CAS}$ going LOW, the output pin(s) remain open (High-Z) until the next $\overline{CAS}$ cycle. If $\overline{WE}$ goes LOW after $\overline{CAS}$ goes LOW and data reaches the output pins, data out (Q) is activated and retains the selected cell data as long as $\overline{CAS}$ and $\overline{OE}$ remain LOW (regardless of $\overline{WE}$ or $\overline{RAS}$). This late $\overline{WE}$ pulse results in a READ-WRITE cycle.

The 16 data inputs and 16 data outputs are routed through 16 pins using common I/O, and pin direction is controlled by $\overline{OE}$, $\overline{WEL}$ and $\overline{WEH}$.

FAST PAGE MODE operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row address (A0-A9) defined page boundary. The FAST PAGE MODE cycle is always initiated with a row address strobed-in by $\overline{RAS}$ followed by a column address strobed-in by $\overline{CAS}$. $\overline{CAS}$ may be toggled-in by holding $\overline{RAS}$ LOW and strobing-in different column addresses, thus executing faster memory cycles. Returning $\overline{RAS}$ HIGH terminates the FAST PAGE MODE operation.

Returning $\overline{RAS}$ and $\overline{CAS}$ HIGH terminates a memory cycle and decreases chip current to a reduced standby level. The chip is also preconditioned for the next cycle during the $\overline{RAS}$ HIGH time. Memory cell data is retained in its correct state by maintaining power and executing any $\overline{RAS}$ cycle (READ, WRITE, $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$, or HIDDEN refresh) so that all 1,024 combinations of $\overline{RAS}$ addresses (A0-A9) are executed at least every 16ms, regardless of sequence. The $\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh cycle will also invoke the refresh counter and controller for ROW address control.

BYTE ACCESS CYCLE

The BYTE WRITE mode is determined by the use of $\overline{WEL}$ and $\overline{WEH}$. Enabling $\overline{WEL}$ will select a lower byte WRITE cycle (DQ1-DQ8) while Enabling $\overline{WEH}$ will select an upper byte WRITE cycle (DQ9-DQ16). Enabling both $\overline{WEL}$ and $\overline{WEH}$ selects a word WRITE cycle.

The MT4C16260/1 may be viewed as two 256K x 8 DRAMS that have common input controls, with the exception of the $\overline{WE}$ inputs. Figure 1 illustrates the MT4C16260/1 BYTE and WORD WRITE cycles.

MASKED WRITE ACCESS CYCLE (MT4C16261 ONLY)

Every WRITE access cycle can be a MASKED WRITE, depending on the state of $\overline{WE}$ at $\overline{RAS}$ time. A MASKED WRITE is selected when $\overline{WE}$ is LOW at $\overline{RAS}$ time and mask data is supplied on the DQ pins.

The mask data present on the DQ1-DQ16 inputs at $\overline{RAS}$ time will be written to an internal mask data register and will then act as an individual write enable for each of the corresponding DQ inputs. If a LOW (logic "0") is written to a mask data register bit, the input port for that bit is disabled during the following WRITE operation and no new data will be written to that DRAM cell location. A HIGH (logic "1") on a mask data register bit enables the input port and allows normal WRITE operations to proceed. At $\overline{CAS}$ time, the bits present on the DQ1-DQ16 inputs will be either written to the DRAM (if the mask data bit was HIGH) or ignored (if the mask data bit was LOW).

For NONPERSISTENT MASKED WRITEs, new mask data must be supplied each time a MASKED WRITE cycle is initiated.

Figure 2 illustrates the MT4C16261 MASKED WRITE operation (Note: $\overline{RAS}$ or $\overline{CAS}$ time refers to the time at which $\overline{RAS}$ or $\overline{CAS}$ transition from HIGH to LOW).

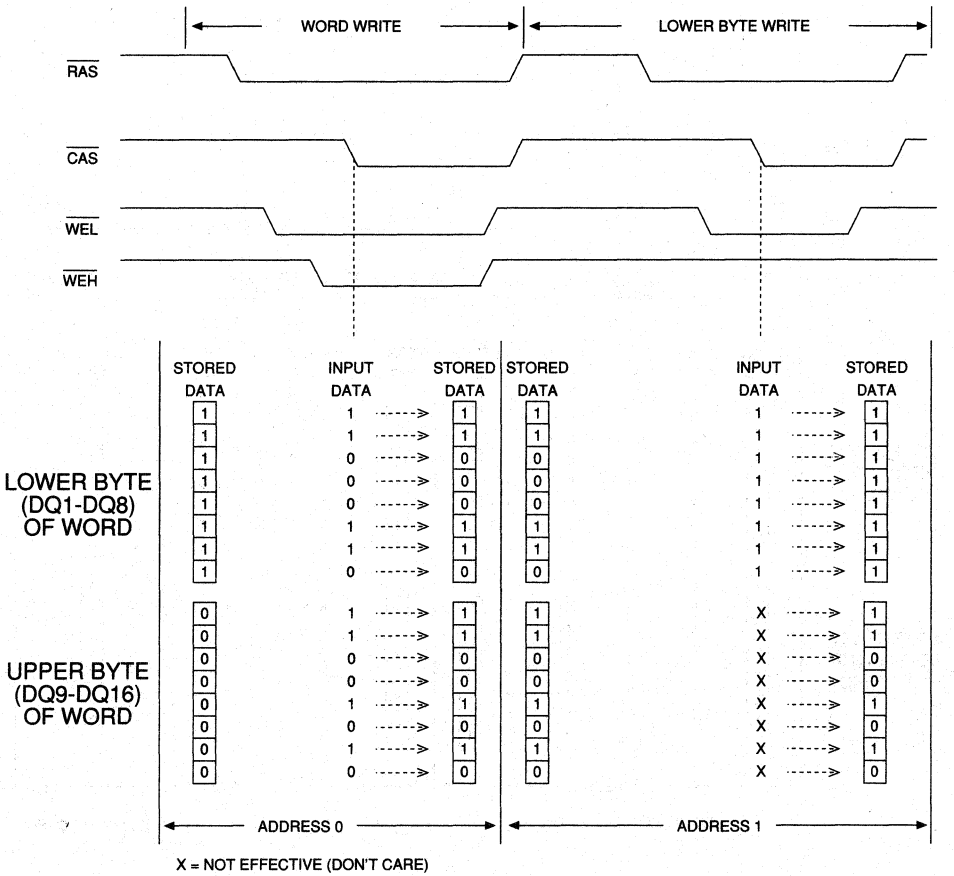


Figure 1
MT4C16260/1 WORD AND BYTE WRITE EXAMPLE

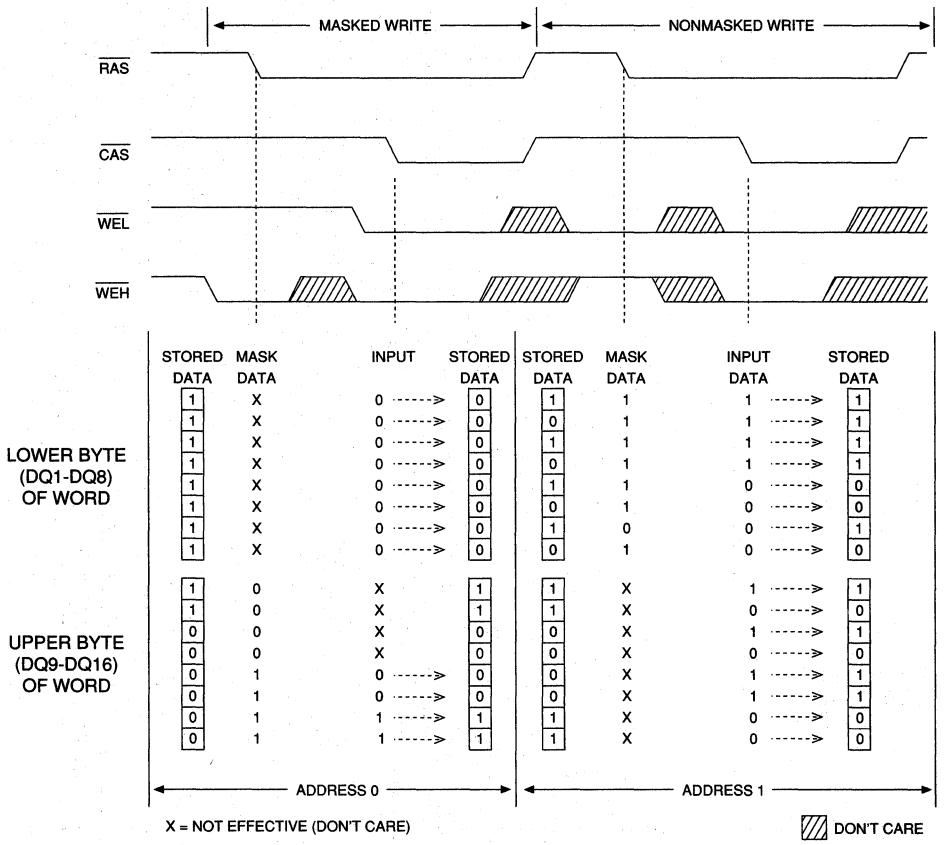


Figure 2
MT4C16261 MASKED WRITE EXAMPLE

TRUTH TABLE: MT4C16260/1

FUNCTION		RAS	CAS	WEL	WEH	OE	ADDRESSES tR	ADDRESSES tC	DQs	NOTES
Standby		H	H→X	X	X	X	X	X	High-Z	
READ		L	L	H	H	L	ROW	COL	Data Out	
WRITE: WORD (EARLY-WRITE)		L	L	L	L	X	ROW	COL	Data In	3
WRITE: LOWER BYTE (EARLY)		L	L	L	H	X	ROW	COL	Lower Byte, Data In Upper Byte, High-Z	3
WRITE: UPPER BYTE (EARLY)		L	L	H	L	X	ROW	COL	Lower Byte, High-Z Upper Byte, Data In	3
READ-WRITE		L	L	H→L	H→L	L→H	ROW	COL	Data Out, Data In	1, 3
FAST-PAGE-MODE READ	1st Cycle	L	H→L	H	H	L	ROW	COL	Data Out	
	2nd Cycle	L	H→L	H	H	L	n/a	COL	Data Out	
FAST-PAGE-MODE WRITE	1st Cycle	L	H→L	L	L	X	ROW	COL	Data In	1, 3
	2nd Cycle	L	H→L	L	L	X	n/a	COL	Data In	1, 3
FAST-PAGE-MODE READ-WRITE	1st Cycle	L	H→L	H→L	H→L	L→H	ROW	COL	Data Out, Data In	1, 3
	2nd Cycle	L	H→L	H→L	H→L	L→H	n/a	COL	Data Out, Data In	1, 3
HIDDEN REFRESH	READ	L→H→L	L	H	H	L	ROW	COL	Data Out	
	WRITE	L→H→L	L	L	L	X	ROW	COL	Data In	1, 2, 3
RAS-ONLY REFRESH		L	H	X	X	X	ROW	n/a	High-Z	
CAS-BEFORE-RAS REFRESH		H→L	L	H	H	X	X	X	High-Z	

NOTE: 1. These cycles may also be BYTE WRITE cycles (either WEL or WEH active).
2. EARLY-WRITE only.
3. Data In will be dependent on the mask provided (MT4C16261 only). Refer to figure 2.

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply Relative to V_{SS} ..... -1V to +7V
Operating Temperature, T_A (Ambient) ..... 0°C to +70°C
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$; V_{CC} = 5V ±10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.5	V	1
Input High (Logic 1) Voltage, All Inputs	V_{IH}	2.4	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, All Inputs	V_{IL}	-1.0	0.8	V	1
INPUT LEAKAGE CURRENT Any Input $0V \le V_{IN} \le V_{CC}$ (All other pins not under test = 0 V)	I_I	-2	2	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled; $0V \le V_{OUT} \le 5.5V$)	I_{OZ}	-10	10	µA	
OUTPUT LEVELS Output High Voltage (I_{OUT} = -5mA)	V_{OH}	2.4		V	
Output Low Voltage (I_{OUT} = 4.2mA)	V_{OL}		0.4	V	

(Notes: 1, 3, 4, 6, 7) ($0°C \le T_A \le 70°C$; V_{CC} = 5V ± 10%)

		MAX				
PARAMETER/CONDITION	SYMBOL	-7	-8	-10	UNITS	NOTES
STANDBY CURRENT: (TTL) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC1}	2	2	2	mA	
STANDBY CURRENT: (CMOS) ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} -0.2V)	I_{CC2}	1	1	1	mA	25
OPERATING CURRENT: Random READ/WRITE Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC (MIN))	I_{CC3}	140	130	120	mA	3, 4, 30
OPERATING CURRENT: FAST-PAGE-MODE Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: ^tPC = ^tPC (MIN); ^tCP, ^tASC = 10ns)	I_{CC4}	100	90	80	mA	3, 4, 30
REFRESH CURRENT: $\overline{RAS}$ ONLY Average power supply current ($\overline{RAS}$ Cycling, $\overline{CAS}$=V_{IH}: ^tRC = ^tRC (MIN))	I_{CC5}	140	130	120	mA	3, 30
REFRESH CURRENT: $\overline{CAS}$-BEFORE-$\overline{RAS}$ Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC (MIN))	I_{CC6}	140	130	120	mA	3

CAPACITANCE

(Note: 2)

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A9	C_{I1}		5	pF	2
Input Capacitance: $\overline{RAS}$, $\overline{CAS}$, $\overline{WEL}$, $\overline{WEH}$, $\overline{OE}$	C_{I2}		7	pF	2
Input/Output Capacitance: DQ	C_{IO}		7	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) ($0°C \le T_A \le +70°C$; $V_{CC} = 5V \pm 10\%$)

AC CHARACTERISTICS		-7		-8		-10			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	^tRC	130		150		180		ns	
READ-WRITE cycle time	^tRWC	180		200		245		ns	
FAST-PAGE-MODE READ or WRITE cycle time	^tPC	45		50		55		ns	
FAST-PAGE-MODE READ-WRITE cycle time	^tPRWC	95		100		110		ns	
Access time from $\overline{RAS}$	^tRAC		70		80		100	ns	14
Access time from $\overline{CAS}$	^tCAC		20		20		25	ns	15
Output Enable time	^tOE		20		20		25	ns	
Access time from column address	^tAA		35		40		45	ns	
Access time from $\overline{CAS}$ precharge	^tCPA		40		45		55	ns	
$\overline{RAS}$ pulse width	^tRAS	70	100,000	80	100,000	100	100,000	ns	
$\overline{RAS}$ pulse width (FAST PAGE MODE)	^tRASP	70	100,000	80	100,000	100	100,000	ns	
$\overline{RAS}$ hold time	^tRSH	20		20		25		ns	
$\overline{RAS}$ precharge time	^tRP	50		60		70		ns	
$\overline{CAS}$ pulse width	^tCAS	20	100,000	20	100,000	25	100,000	ns	
$\overline{CAS}$ hold time	^tCSH	70		80		100		ns	
$\overline{CAS}$ precharge time	^tCPN	10		10		10		ns	16
$\overline{CAS}$ precharge time (FAST PAGE MODE)	^tCP	10		10		10		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	^tRCD	20	50	20	60	25	75	ns	17
$\overline{CAS}$ to $\overline{RAS}$ precharge time	^tCRP	10		10		10		ns	
Row address setup time	^tASR	0		0		0		ns	
Row address hold time	^tRAH	10		10		15		ns	
$\overline{RAS}$ to column address delay time	^tRAD	15	35	15	40	20	55	ns	18
Column address setup time	^tASC	0		0		0		ns	
Column address hold time	^tCAH	15		15		20		ns	
Column address hold time (referenced to $\overline{RAS}$)	^tAR	55		60		75		ns	
Column address to $\overline{RAS}$ lead time	^tRAL	35		40		55		ns	
Read command setup time	^tRCS	0		0		0		ns	26
Read command hold time (referenced to $\overline{CAS}$)	^tRCH	0		0		0		ns	19, 26
Read command hold time (referenced to $\overline{RAS}$)	^tRRH	0		0		0		ns	19
$\overline{CAS}$ to output in Low-Z	^tCLZ	0		0		0		ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

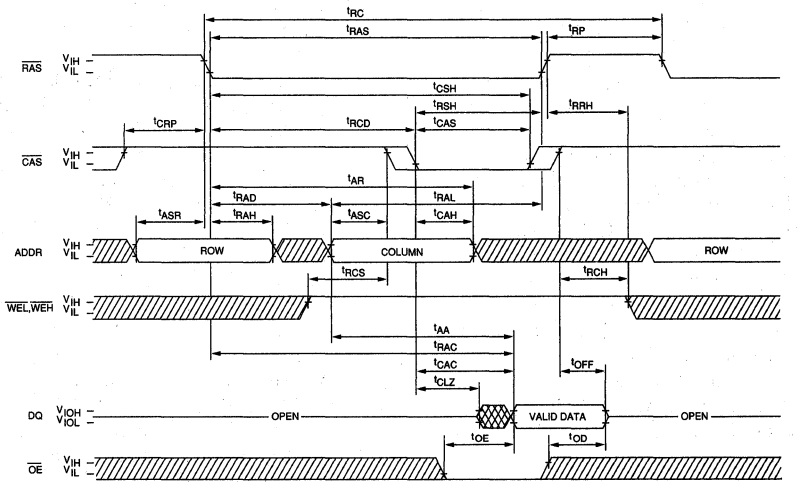
(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C ≤ T_A ≤ +70°C; Vcc = 5V ± 10%)

AC CHARACTERISTICS		-7		-8		-10			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Output buffer turn-off delay	tOFF	0	15	0	15	0	20	ns	20, 29
Output disable time	tOD		15		15		20	ns	29
Write command setup time	tWCS	0		0		0		ns	21, 26
Write command hold time	tWCH	15		15		20		ns	26
Write command hold time (referenced to $\overline{RAS}$)	tWCR	55		60		75		ns	26
Write command pulse width	tWP	10		10		20		ns	26
Write command to $\overline{RAS}$ lead time	tRWL	20		20		25		ns	26
Write command to $\overline{CAS}$ lead time	tCWL	20		20		25		ns	26
Data-in setup time	tDS	0		0		0		ns	22
Data-in hold time	tDH	15		15		20		ns	22
Data-in hold time (referenced to $\overline{RAS}$)	tDHR	55		60		75		ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	tRWD	95		105		135		ns	21
Column address to $\overline{WE}$ delay time	tAWD	60		65		80		ns	21
$\overline{CAS}$ to $\overline{WE}$ delay time	tCWD	45		45		60		ns	21
Transition time (rise or fall)	tT	3	50	3	50	3	50	ns	9, 10
Refresh period (1,024 cycles)	tREF		16		16		16	ms	28
$\overline{RAS}$ to $\overline{CAS}$ precharge time	tRPC	10		10		10		ns	
$\overline{CAS}$ setup time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	tCSR	10		10		10		ns	5
$\overline{CAS}$ hold time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	tCHR	10		10		10		ns	5
MASKED WRITE command to $\overline{RAS}$ setup time	tWRS	0		0		0		ns	26, 27
$\overline{WE}$ hold time (MASKED WRITE and $\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	tWRH	10		10		15		ns	26
Mask data to $\overline{RAS}$ setup time	tMS	0		0		0		ns	26, 27
Mask data to $\overline{RAS}$ hold time	tMH	10		10		10		ns	26, 27
$\overline{OE}$ hold time from $\overline{WE}$ during READ-MODIFY-WRITE cycle	tOEH	20		20		25		ns	28
$\overline{OE}$ setup prior to $\overline{RAS}$ during HIDDEN REFRESH cycle	tORD	0		0		0		ns	
Last $\overline{CAS}$ going low to first $\overline{CAS}$ to return high	tCLCH	10		10		10		ns	
$\overline{WE}$ setup time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	tWRP	10		10		10		ns	

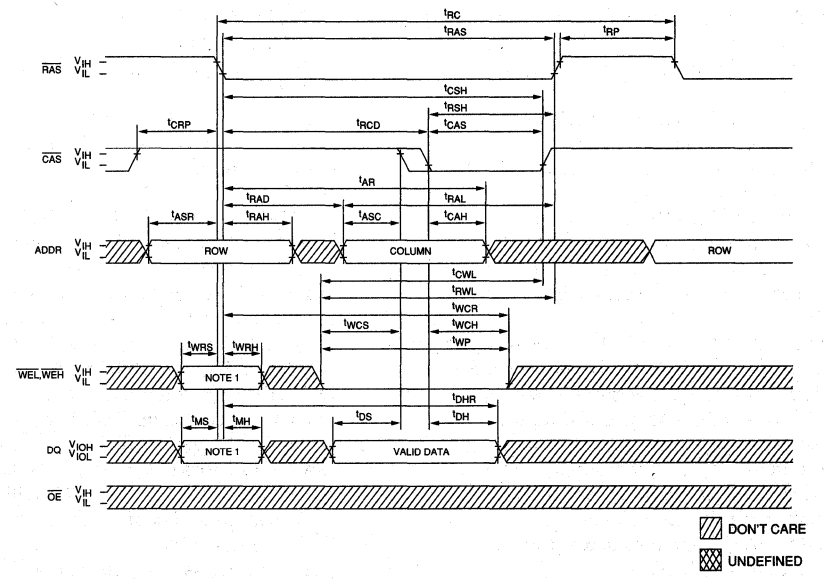
NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. V_{CC} = 5V ±10%, f = 1 MHz.
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \le T_A \le 70°C$) is assured.
7. An initial pause of 100µs is required after power-up followed by 8 $\overline{RAS}$ refresh cycles ($\overline{RAS}$-ONLY or $\overline{CBR}$) before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-up should be repeated any time the ^tRAF refresh requirement is exceeded.
8. AC characteristics assume ^tT = 5ns.
9. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS}$ = V_{IH}, data output is High-Z.
12. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to 2 TTL gate and 100pF.
14. Assumes that $^tRCD < {}^tRCD$ (max). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
15. Assumes that $^tRCD \ge {}^tRCD$ (MAX).
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the Q buffer, $\overline{CAS}$ must be pulsed HIGH for ^tCPN.
17. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (MAX) limit, then access time is controlled exclusively by ^tCAC.
18. Operation within the ^tRAD limit ensures that ^tRCD (MAX) can be met. ^tRAD (MAX) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (MAX) limit, then access time is controlled exclusively by ^tAA.
19. Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
20. ^tOFF (MAX) defines the time at which the output achieves the open circuit condition, not a reference to V_{OH} or V_{OL}.
21. ^tWCS, ^tRWD, ^tAWD and ^tCWD are restrictive operating parameters in LATE-WRITE and READ-MODIFY-WRITE cycles only. If $^tWCS \ge {}^tWCS$ (MIN), the cycle is an EARLY-WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If $^tRWD \ge {}^tRWD$ (MIN), $^tAWD \ge {}^tAWD$ (MIN) and $^tCWD \ge {}^tCWD$ (MIN), the cycle is a READ-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions are met, the state of Q (at access time and until $\overline{CAS}$ goes back to V_{IH}) is indeterminate. $\overline{WE}$ determines either EARLY-WRITE (WCS), LATE-WRITE (RWD, AWD and CWD) or an indeterminate (WCS or RWD, AWD and CWD not met) cycle when $\overline{WE}$ goes LOW in reference to $\overline{CAS}$ going LOW.
22. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY-WRITE cycles and $\overline{WE}$ leading edge in LATE-WRITE or READ-MODIFY-WRITE cycles.
23. During a READ cycle, if $\overline{OE}$ is LOW then taken HIGH before $\overline{CAS}$ goes HIGH, Q goes open. If $\overline{OE}$ is tied permanently LOW, LATE-WRITE or READ-MODIFY-WRITE operations are not possible.
24. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW and $\overline{OE}$ = HIGH.
25. All other inputs at Vcc -0.2V.
26. Write command is defined as either $\overline{WEL}$ or $\overline{WEH}$ or both going LOW.
27. MT4C16261 only.
28. LATE-WRITE and READ-MODIFY-WRITE cycles must have both ^tOD and ^tOEH met ($\overline{OE}$ HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. The DQs will provide the previously read data if $\overline{CAS}$ remains LOW and $\overline{OE}$ is taken back LOW after ^tOEH is met. If $\overline{CAS}$ goes HIGH prior to $\overline{OE}$ going back LOW, the DQs will remain open.
29. The DQs open during READ cycles once ^tOD or ^tOFF occur. If $\overline{CAS}$ goes HIGH first, $\overline{OE}$ becomes a "don't care." If $\overline{OE}$ goes HIGH and $\overline{CAS}$ stays LOW, $\overline{OE}$ is not a "don't care;" and the DQs will provide the previously read data if $\overline{OE}$ is taken back LOW (while $\overline{CAS}$ remains LOW).
30. Column address changed once while $\overline{RAS}$ = V_{IL} and $\overline{CAS}$ = V_{IH}.

READ CYCLE

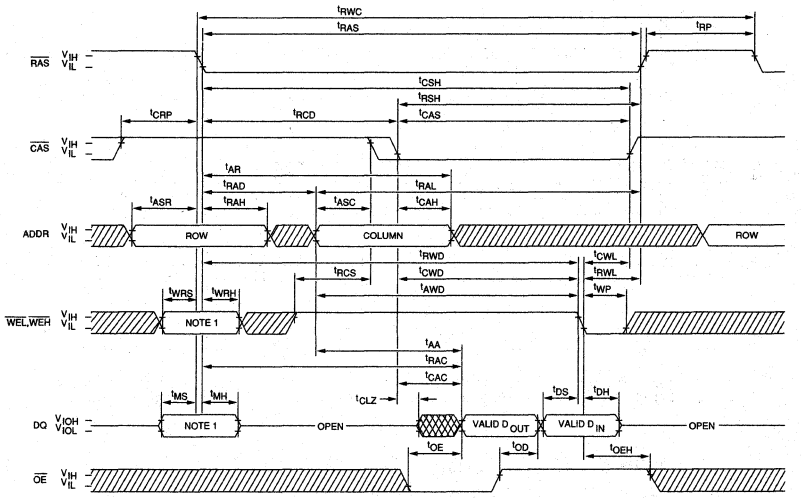


EARLY-WRITE CYCLE

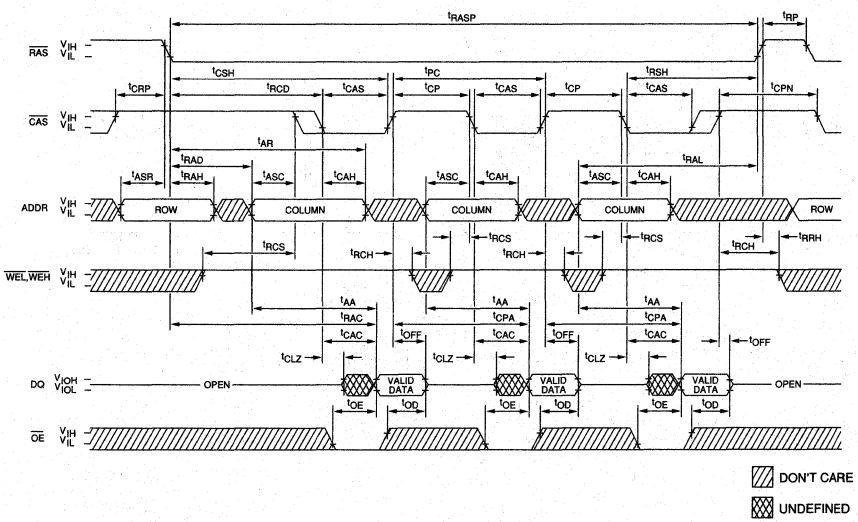


NOTE: 1. Applies to MT4C16261 only; $\overline{WEL}$, $\overline{WEH}$ and DQ inputs on MT4C16260 are "don't care" at $\overline{RAS}$ time. $\overline{WE}$ selects between normal WRITE and MASKED WRITE at $\overline{RAS}$ time. The DQ inputs are "don't care" for a normal WRITE, with $\overline{WE}$ HIGH at $\overline{RAS}$ time. The DQ inputs provide the mask data at $\overline{RAS}$ time for a MASKED WRITE, with $\overline{WE}$ LOW at $\overline{RAS}$ time.

READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)

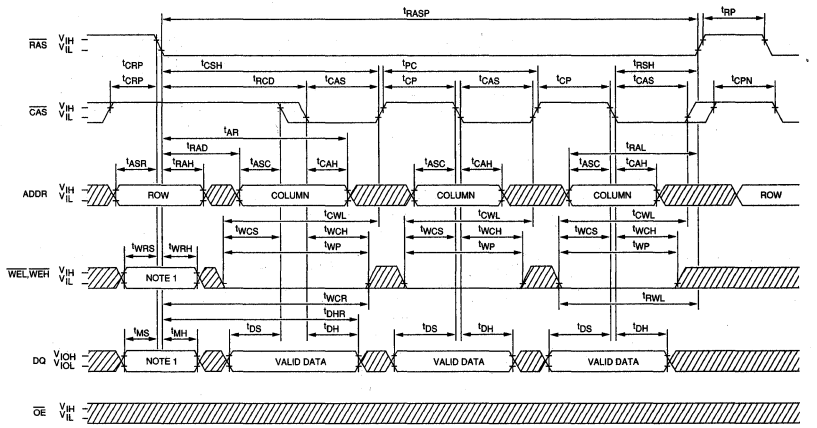


FAST-PAGE-MODE READ CYCLE

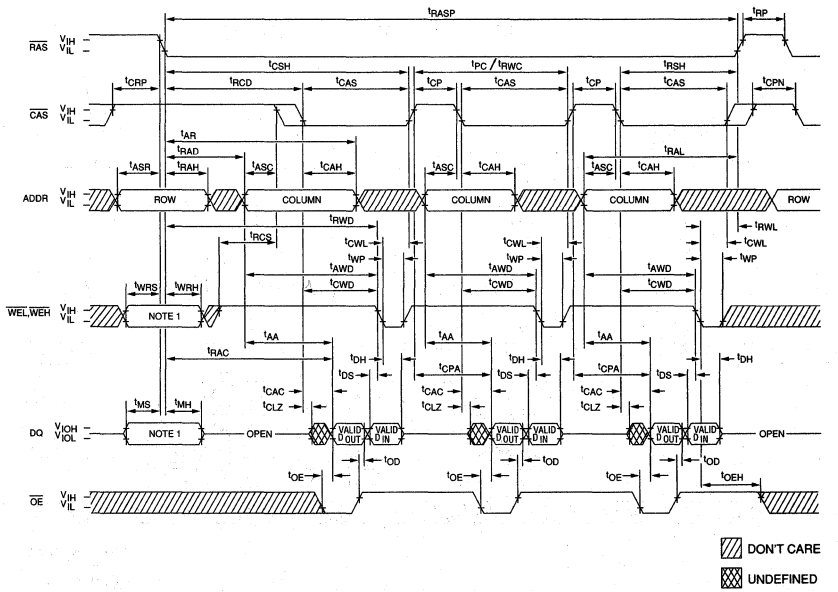


NOTE: 1. Applies to MT4C16261 only; $\overline{WEL}$, $\overline{WEH}$ and DQ inputs on MT4C16260 are "don't care" at $\overline{RAS}$ time. $\overline{WE}$ selects between normal WRITE and MASKED WRITE at $\overline{RAS}$ time. The DQ inputs are "don't care" for a normal WRITE, with $\overline{WE}$ HIGH at $\overline{RAS}$ time. The DQ inputs provide the mask data at $\overline{RAS}$ time for a MASKED WRITE, with $\overline{WE}$ LOW at $\overline{RAS}$ time.

FAST-PAGE-MODE EARLY-WRITE CYCLE

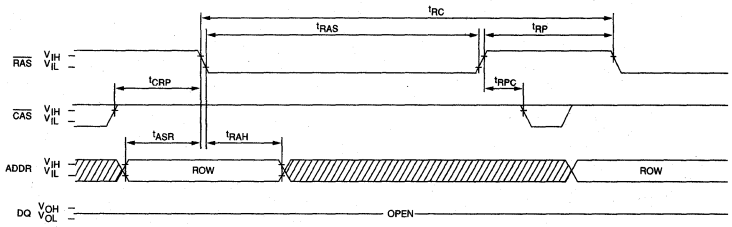


FAST-PAGE-MODE READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)

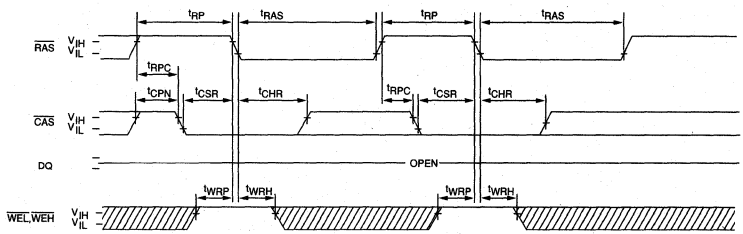


NOTE: 1. Applies to MT4C16261 only; $\overline{WEL}$, $\overline{WEH}$ and DQ inputs on MT4C16260 are "don't care" at $\overline{RAS}$ time. $\overline{WE}$ selects between normal WRITE and MASKED WRITE at $\overline{RAS}$ time. The DQ inputs are "don't care" for a normal WRITE, with $\overline{WE}$ HIGH at $\overline{RAS}$ time. The DQ inputs provide the mask data at $\overline{RAS}$ time for a MASKED WRITE, with $\overline{WE}$ LOW at $\overline{RAS}$ time.

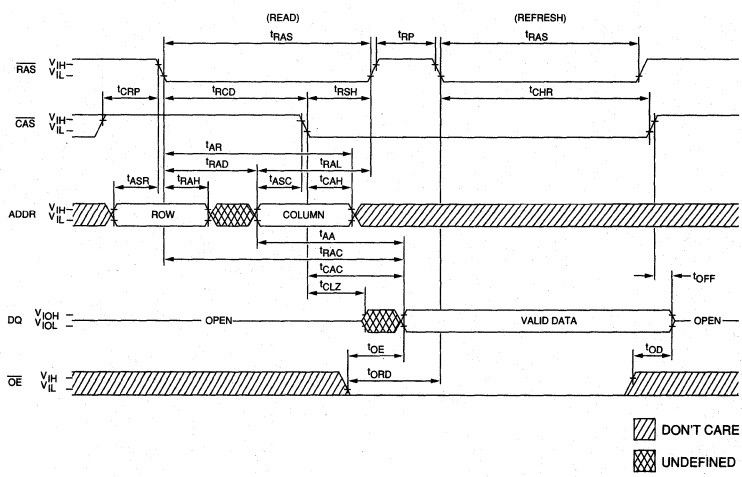
RAS-ONLY REFRESH CYCLE
(ADDR = A0-A9,,OE; WEL and WEH = DON'T CARE)



CAS-BEFORE-RAS REFRESH CYCLE
(A0-A9, and OE = DON'T CARE)



HIDDEN REFRESH CYCLE [24]
(WEL, WEH = HIGH; OE=LOW)



NEW ■ WIDE DRAM

NEW ■ WIDE DRAM

DRAM

1 MEG x 16 DRAM

5.0V FAST PAGE MODE (MT4C1M16CX)
3.0/3.3V, FAST PAGE MODE (MT4LC1M16CX)

FEATURES

- Industry standard x16 pinouts, timing, functions and packages
- High-performance, CMOS silicon-gate process
- Single +5V only or +3.0/+3.3V only ±10% power supply
- Low power, 5mW standby; 500mW active, typical (5V)
- All device pins are fully TTL compatible
- 1,024 cycle refresh in 16ms (10 rows and 10 columns)
- Refresh modes: $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$ (CBR) and HIDDEN
- Optional FAST PAGE MODE access cycle
- BYTE WRITE access cycle
- BYTE READ access cycle (MT4C1M16C3/5 only)
- NONPERSISTENT MASKED WRITE access cycle (MT4C1M16C5/7 only)

OPTIONS / MARKING

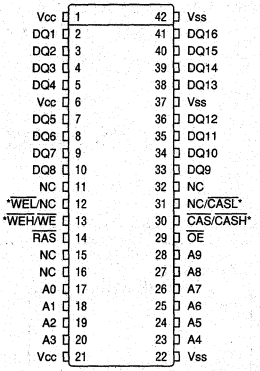
• Timing	
60ns access	- 6
70ns access	- 7
80ns access	- 8
• Power Supply	
+5V ±10% only	4C
+3.0/3.3V ±10% only	4LC
• Refresh Rate	
1,024 Rows	None
4,096 Rows	Contact Factory
• Write Cycle Access	
BYTE or WORD via $\overline{CAS}$ (non-maskable)	16C3
BYTE or WORD via $\overline{CAS}$ (maskable)	16C5
BYTE or WORD via $\overline{WE}$ (non-maskable)	16C6
BYTE or WORD via $\overline{WE}$ (maskable)	16C7
• Packages	
Plastic SOJ (400 mil)	DJ
Plastic TSOP (400 mil)	TG

• Part Number Example: MT4C1M16C3DJ-7

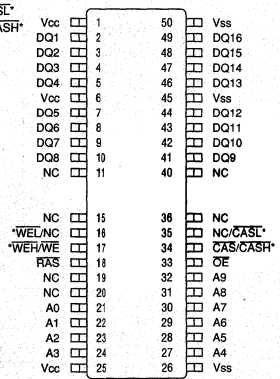
NOTE: Available in die form. Please consult factory for die data sheets.

PIN ASSIGNMENT (Top View)

42-Pin SOJ (Q-7)



44-Pin TSOP (R-6)



*MT4C1M16C6/7 / MT4C1M16C3/5

GENERAL DESCRIPTION

The MT4C1M16CX and MT4LC1M16CX are randomly accessed solid-state memories containing 16,777,216 bits organized in a x16 configuration. The MT4C1M16CX and the MT4LC1M16CX are the same DRAM versions except that the MT4LC1M16CX is the low voltage version of MT4C1M16CX. The MT4LC1M16CX is designed to operate in either a 3.0V ±10% or a 3.3V ±10% memory system. All further references made for the MT4C1M16CX also apply to the MT4LC1M16CX, unless specifically state otherwise. The MT4C1M16C6 and MT4C1M16C7 have both BYTE WRITE and WORD WRITE access cycles via two write enable pins. The MT4C1M16C3 and MT4C1M16C5 have both BYTE WRITE and WORD WRITE access cycles via two $\overline{CAS}$ pins. The MT4C1M16C5 and MT4C1M16C7 are also able to perform WRITE-PER-BIT accesses.

NEW ■ WIDE DRAM

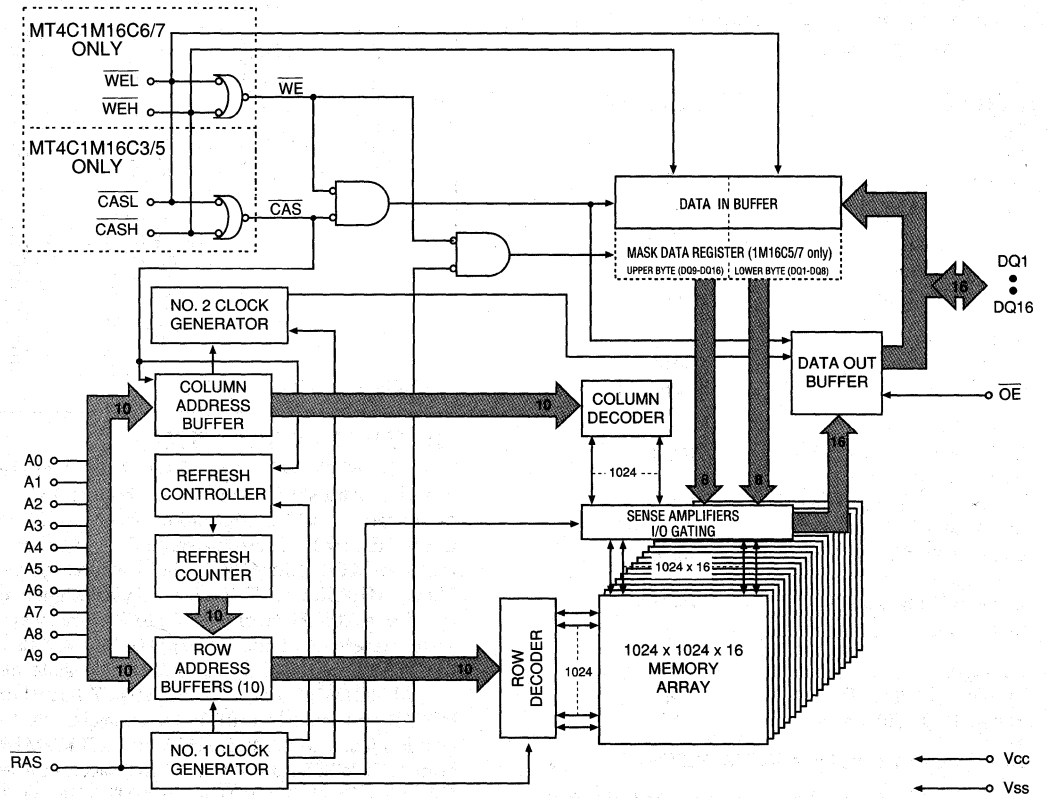
The MT4C1M16C3 and MT4C1M16C6 function in the same manner except that $\overline{WEL}$ and $\overline{WEH}$ on MT4C1M16C6 and $\overline{CASL}$ and $\overline{CASH}$ on MT4C1M16C3 control the selection of BYTE WRITE access cycles. $\overline{WEL}$ and $\overline{WEH}$ function in an identical manner to $\overline{WE}$ in that either $\overline{WEL}$ or $\overline{WEH}$ will generate an internal $\overline{WE}$. $\overline{CASL}$ and $\overline{CASH}$ function in an identical manner to $\overline{CAS}$ in that either $\overline{CASL}$ or $\overline{CASH}$ will generate an internal $\overline{CAS}$.

The MT4C1M16C6 "$\overline{WE}$" function and timing are determined by the first $\overline{WE}$ ($\overline{WEL}$ or $\overline{WEH}$) to transition LOW and by the last to transition back HIGH. Use of only one of the two results in a BYTE WRITE cycle. $\overline{WEL}$ transitioning LOW selects a WRITE cycle for the lower byte (DQ1-DQ8), and $\overline{WEH}$ transitioning LOW selects a WRITE cycle for the upper byte (DQ9-DQ16).

The MT4C1M16C3 "$\overline{CAS}$" function and timing are determined by the first $\overline{CAS}$ ($\overline{CASL}$ or $\overline{CASH}$) to transition LOW and the last to transition back HIGH. Use of only one of the two results in a BYTE WRITE cycle. $\overline{CASL}$ transitioning LOW selects a WRITE cycle for the lower byte (DQ1-DQ8) and $\overline{CASH}$ transitioning LOW selects a WRITE cycle for the upper byte (DQ9-DQ16). BYTE READ cycles are achieved through $\overline{CASL}$ or $\overline{CASH}$ in the same manner during READ cycles for the MT4C1M16C3.

The MT4C1M16C5 and MT4C1M16C7 function in the same manner as MT4C1M16C3 and MT4C1M16C6, respectively; and they have NONPERSISTENT MASKED WRITE cycle capabilities. This option allows the MT4C1M16C5 and MT4C1M16C7 to operate with either normal WRITE cycles or NONPERSISTENT MASKED WRITE cycles.

FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTIONS

SOJ PINS	TSOP PINS	SYMBOL	TYPE	DESCRIPTION
14	18	$\overline{RAS}$	Input	ROW Address Strobe: $\overline{RAS}$ is used to latch-in the 10 row-address bits and strobe the $\overline{WE}$ and DQs on the MASKED WRITE option (MT4C1M16C5 and MT4C1M16C7 only).
30	34	$\overline{CAS}$/ $\overline{CASH}$	Input	Column Address Strobe: $\overline{CAS}$ (MT4C1M16C6/7) is used to latch-in the 10 column-address bits, enable the DRAM output buffers, and strobe the data inputs on WRITE cycles $\overline{CAS}$ controls DQ1 through DQ16. Column Address Strobe Upper Byte: $\overline{CASH}$ (MT4C1M16C3/5) is the $\overline{CAS}$ control for DQ9 through DQ16. The DQs for the byte not being accessed will remain in a High-Z (high impedance) state during either a READ or a WRITE access cycle.
29	33	$\overline{OE}$	Input	Output Enable: $\overline{OE}$ enables the output buffers when taken LOW during a READ access cycle. $\overline{RAS}$ and $\overline{CAS}$ (MT4C1M16C6/7) or $\overline{CASL}$ / $\overline{CASH}$ (MT4C1M16C3/5) must be LOW and $\overline{WEL}$ / $\overline{WEH}$ (MT4C1M16C6/7) or $\overline{WE}$ (MT4C1M16C3/5) must be HIGH before $\overline{OE}$ will control the output buffers. Otherwise, the output buffers are in a High-Z state.
13	17	$\overline{WEH}$/$\overline{WE}$	Input	Write Enable Upper Byte: $\overline{WEH}$ (MT4C1M16C6/7) is $\overline{WE}$ control for the DQ9 through DQ16 inputs. If $\overline{WE}$ or $\overline{WEH}$ is LOW, the access is a WRITE cycle. If either $\overline{WE}$ or $\overline{WEH}$ is LOW at $\overline{RAS}$ time on MT4C1M16C7, then it is also a MASKED WRITE cycle. The DQs for the byte not being written will remain in a High-Z state (BYTE WRITE cycle only). Write Enable: $\overline{WE}$ (MT4C1M16C3/5) controls DQ1 through DQ16 inputs. If $\overline{WE}$ is LOW, the access is a WRITE cycle. The MT4C1M16C5/7 also use $\overline{WE}$ to enable the MASK register during $\overline{RAS}$ time.
12	16	$\overline{WEL}$/NC	Input	Write Enable Lower Byte: $\overline{WEL}$ (MT4C1M16C6/7) is the $\overline{WE}$ control for DQ1 through DQ8 inputs. If $\overline{WEL}$ is LOW, the access is a WRITE cycle. If $\overline{WEL}$ is LOW at $\overline{RAS}$ time on MT4C1M16C3, then it is also a MASKED WRITE cycle. The DQs for the byte not being written will remain in a High-Z state (BYTE WRITE cycle only).
31	35	NC/$\overline{CASL}$	Input	Column Address Strobe Lower Byte: $\overline{CASL}$ (MT4C1M16C3/5) is the $\overline{CAS}$ control for DQ1 through DQ8. The DQs for the byte not being accessed will remain in a High-Z state during either a READ or a WRITE access cycle.
17-20, 23-28	21-24, 27-32	A0-A9	Input	Address Inputs: These inputs are multiplexed and clocked by $\overline{RAS}$ and $\overline{CAS}$ (or $\overline{CASL}$ / $\overline{CASH}$) to select one 16-bit word (or 8-bit byte) out of the 1 Meg available words.

PIN DESCRIPTIONS (continued)

SOJ PINS	TSOP PINS	SYMBOL	TYPE	DESCRIPTION
2-5, 7-10, 33-36, 38-41	2-5, 7-10, 41-44, 46-49	DQ1-DQ16	Input/ Output	Data I/O: For WRITE cycles, DQ1-DQ16 act as inputs to the addressed DRAM location. BYTE WRITEs can be performed by using $\overline{WEL}$ / $\overline{WEH}$ (MT4C1M16C6/7) or $\overline{CASL}$ / $\overline{CASH}$ (MT4C1M16C3/7) to select the byte to be written. For READ access cycles, DQ1-DQ16 act as outputs for the addressed DRAM location. All sixteen I/Os are active for READ cycles (MT4C1M16C6/7). The MT4C1M16C3/5 allow for BYTE READ cycles.
11, 15, 16, 30-32	11, 15, 36, 40	NC	-	No Connect: These pins should be left either unconnected or tied to ground.
1, 6, 21	1, 6, 25	Vcc	Supply	Power Supply: +5V ±10% (C) or 3.0/3.3V ±10% (LC)
22, 37, 42	26, 45, 50	Vss	Supply	Ground

FUNCTIONAL DESCRIPTION

Each bit is uniquely addressed through the 20 address bits during READ or WRITE cycles. These are entered 10 bits (A0-A9) at a time. $\overline{RAS}$ is used to latch the first 10 bits and $\overline{CAS}$ the latter 10 bits.

The $\overline{CAS}$ control also determines whether the cycle will be a refresh cycle ($\overline{RAS}$-ONLY) or an active cycle (READ, WRITE or READ-WRITE) once $\overline{RAS}$ goes LOW. The MT4C1M16C6 and MT4C1M16C7 each have one $\overline{CAS}$ control while the MT4C1M16C3 and MT4C1M16C5 have two: $\overline{CASL}$ and $\overline{CASH}$.

The $\overline{CASL}$ and $\overline{CASH}$ inputs internally generate a $\overline{CAS}$ signal functioning in an identical manner to the single $\overline{CAS}$ input on the other 1 Meg x 16 DRAMs. The key difference is each $\overline{CAS}$ controls its corresponding DQ tri-state logic (in conjunction with $\overline{OE}$ and $\overline{WE}$). $\overline{CASL}$ controls DQ1 through DQ8, and $\overline{CASH}$ controls DQ9 through DQ16.

The MT4C1M16C3 and MT4C1M16C5 "$\overline{CAS}$" function is determined by the first $\overline{CAS}$ ($\overline{CASL}$ or $\overline{CASH}$) to transition LOW and the last one to transition back HIGH. The two $\overline{CAS}$ controls give the MT4C1M16C3 and MT4C1M16C5 both BYTE READ and BYTE WRITE cycle capabilities.

READ or WRITE cycles on the MT4C1M16C3 or MT4C1M16C5 are selected with the $\overline{WE}$ input while either $\overline{WEL}$ or $\overline{WEH}$ perform the "$\overline{WE}$" on the MT4C1M16C6 or MT4C1M16C7. The MT4C1M16C6 and MT4C1M16C7 "$\overline{WE}$" function is determined by the first BYTE WRITE ($\overline{WEL}$ or $\overline{WEH}$) to transition LOW and the last one to transition back HIGH.

A logic HIGH on $\overline{WE}$ dictates READ mode while a logic LOW on $\overline{WE}$ dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. Taking $\overline{WE}$ LOW will initiate a WRITE cycle, selecting DQ1 through DQ16. If $\overline{WE}$ goes LOW prior to $\overline{CAS}$ going LOW, the output pin(s) remain open (High- Z) until the next $\overline{CAS}$ cycle. If $\overline{WE}$ goes LOW after $\overline{CAS}$ goes LOW and data reaches the output pins, data out (Q) is activated and retains the selected cell data as long as $\overline{CAS}$ and $\overline{OE}$ remain LOW (regardless of $\overline{WE}$ or $\overline{RAS}$). This late $\overline{WE}$ pulse results in a READ-WRITE cycle.

The 16 data inputs and 16 data outputs are routed through 16 pins using common I/O. Pin direction is controlled by $\overline{OE}$, $\overline{WEL}$ and $\overline{WEH}$ (MT4C1M16C6 and MT4C1M16C7) or $\overline{WE}$ (MT4C1M16C3 and MT4C1M16C5).

FAST PAGE MODE operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row address (A0-A9) defined page boundary. The FAST PAGE MODE cycle is always initiated with a row address strobed-in by $\overline{RAS}$ followed by a column address strobed-in by $\overline{CAS}$. $\overline{CAS}$ may be toggled-in by holding $\overline{RAS}$ LOW and strobing-in different column addresses, thus executing faster memory cycles. Returning $\overline{RAS}$ HIGH terminates the FAST PAGE MODE operation.

Returning $\overline{RAS}$ and $\overline{CAS}$ HIGH terminates a memory cycle and decreases chip current to a reduced standby level. The chip is also preconditioned for the next cycle during the $\overline{RAS}$ high time. Memory cell data is retained in its correct state by maintaining power and executing any $\overline{RAS}$ cycle (READ, WRITE, $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$, or HIDDEN refresh) so that all 1024 combinations of $\overline{RAS}$ addresses (A0-A9) are executed at least every 16ms, regardless of sequence. The $\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh cycle will also invoke the refresh counter and controller for ROW address control.

BYTE ACCESS CYCLE

The BYTE WRITE mode is determined by the use of $\overline{WEL}$ and $\overline{WEH}$ or $\overline{CASL}$ and $\overline{CASH}$. Enabling $\overline{WEL}$/$\overline{CASL}$ will select a lower BYTE WRITE cycle (DQ1-DQ8). Enabling $\overline{WEH}$ or $\overline{CASH}$ will select an upper BYTE WRITE cycle (DQ9-DQ16). Enabling both $\overline{WEL}$ and $\overline{WEH}$ or $\overline{CASL}$ and $\overline{CASH}$ selects a WORD WRITE cycle.

The MT4C1M16C3, MT4C1M16C5, MT4C1M16C6 and MT4C1M16C7 may be viewed as two 1 Meg x 8 DRAMs that have common input controls, with the exception of the $\overline{WE}$ or the $\overline{CAS}$ inputs. Figure 1 illustrates the MT4C1M16C6 BYTE WRITE and WORD WRITE cycles and Figure 2 illustrates the MT4C1M16C3 BYTE WRITE and WORD WRITE cycles.

The MT4C1M16C3 also has BYTE READ and WORD READ cycles, since it uses two $\overline{CAS}$ inputs to control its byte accesses. Figure 3 illustrates the MT4C1M16C3 BYTE READ and WORD READ cycles.

MASKED WRITE ACCESS CYCLE (MT4C1M16C5/7 Only)

The MASKED WRITE mode control input selects normal WRITE access or MASKED WRITE access cycles. Every WRITE access cycle can be a MASKED WRITE, depending on the state of $\overline{WE}$ at $\overline{RAS}$ time. A MASKED WRITE is selected when mask data is supplied on the DQ pins and $\overline{WE}$ is LOW at $\overline{RAS}$ time. The MT4C1M16C3 and MT4C1M16C6 do not have the MASKED WRITE cycle function.

The data (mask data) present on the DQ1-DQ16 inputs at $\overline{RAS}$ time will be written to an internal bit mask data register and will then act as an individual write enable for each of the corresponding DQ inputs. If a LOW (logic "0") is written to a mask data register bit, the input port for that bit is disabled during the following WRITE operation and no new data will be written to that DRAM cell location. A HIGH (logic "1") on a mask data register bit enables the input port and allows normal WRITE operations to proceed. At $\overline{CAS}$ time, the bits present on the DQ1-DQ16 inputs will be written to the DRAM (if the mask data bit was HIGH) or ignored (if the mask data bit was LOW).

New mask data must be supplied each time a MASKED WRITE cycle is initiated (non-persistent), even if the previous cycle's mask was the same.

Figure 4 illustrates the MT4C1M16C7 MASKED WRITE operation and Figure 5 illustrates the MT4C1M16C5 MASKED WRITE operation.

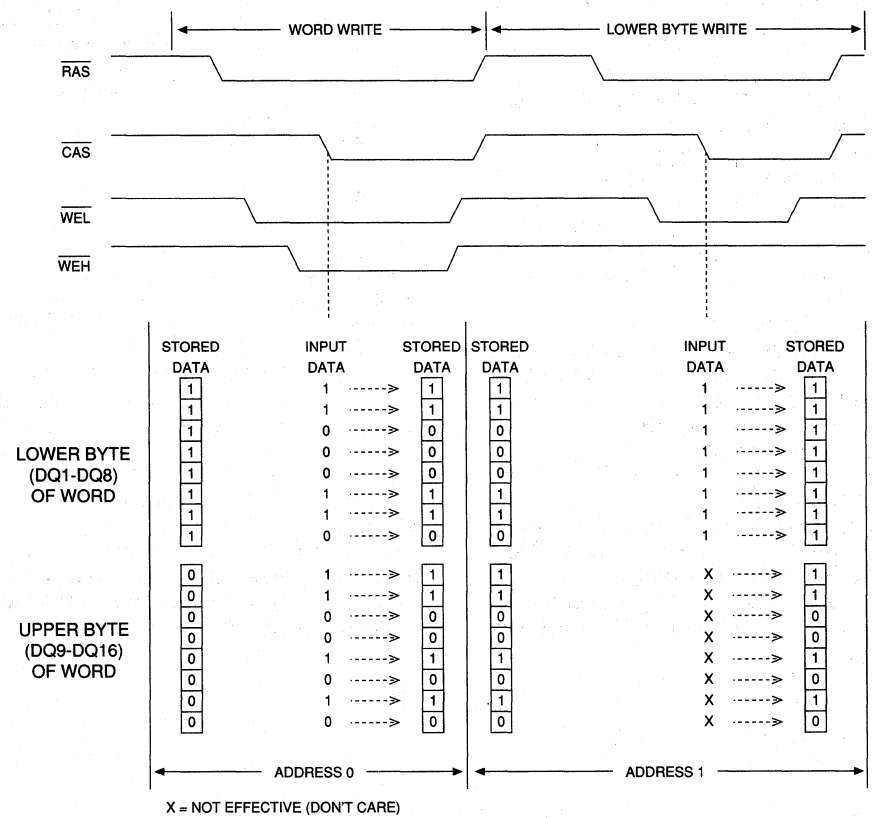


Figure 1
MT4C1M16C6/7 WORD AND BYTE WRITE EXAMPLE

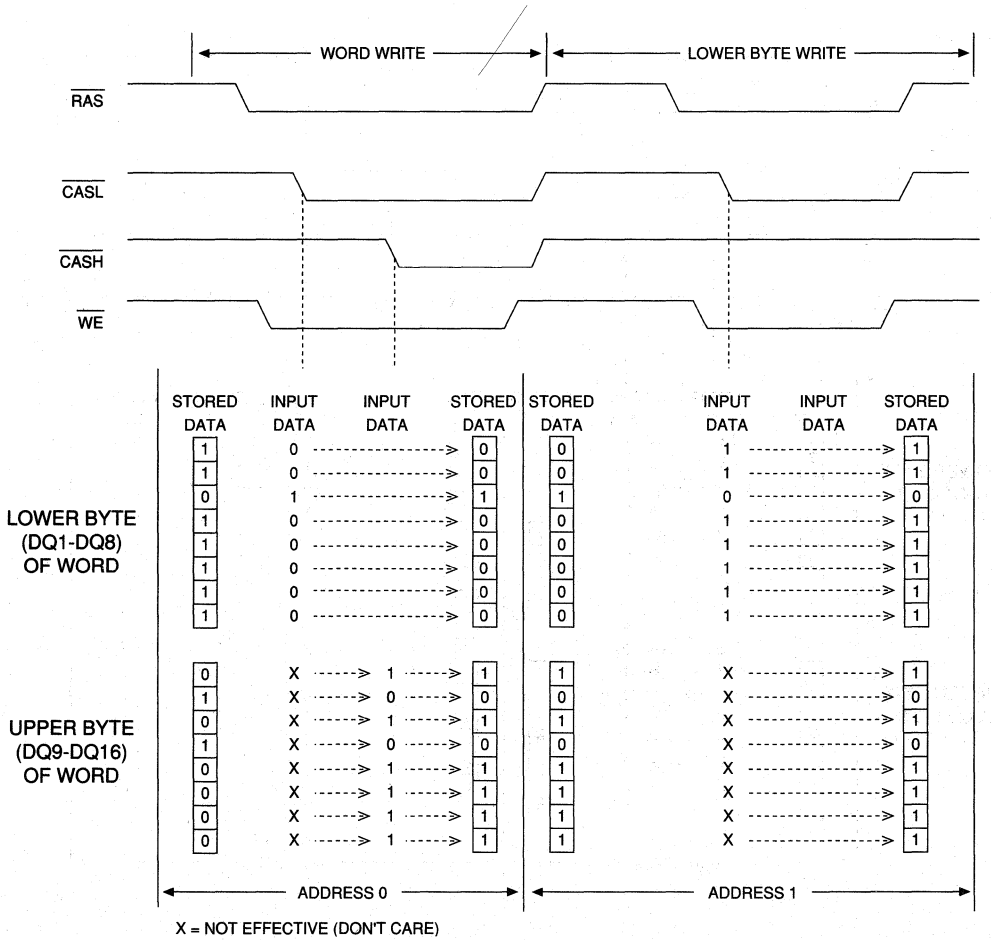


Figure 2
MT4C1M16C3/5 WORD AND BYTE WRITE EXAMPLE

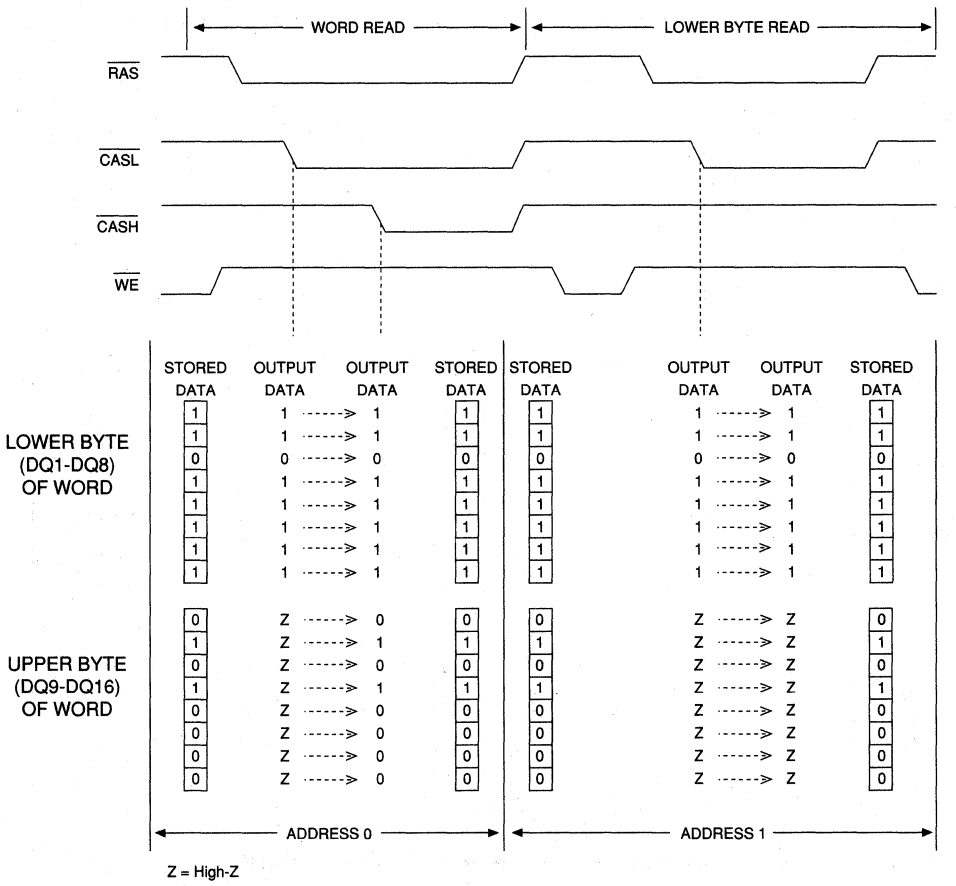


Figure 3
MT4C1M16C3/5 WORD AND BYTE READ EXAMPLE

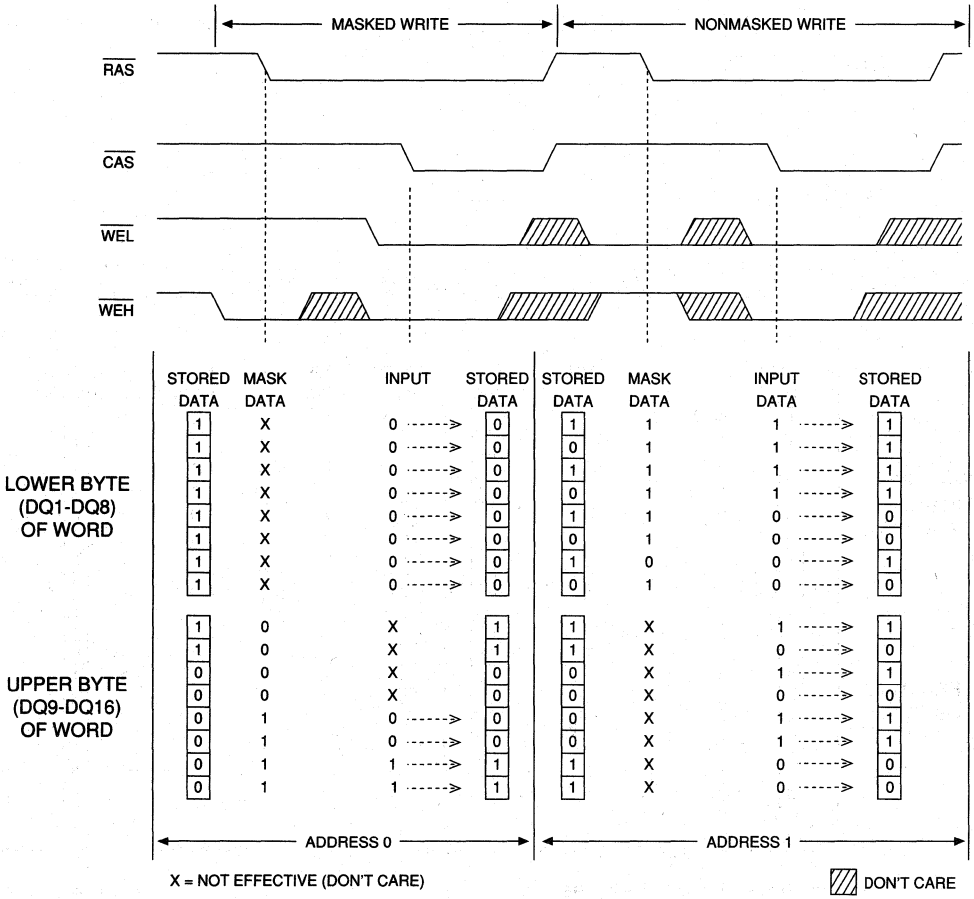


Figure 4
MT4C1M16C7 MASKED WRITE EXAMPLE

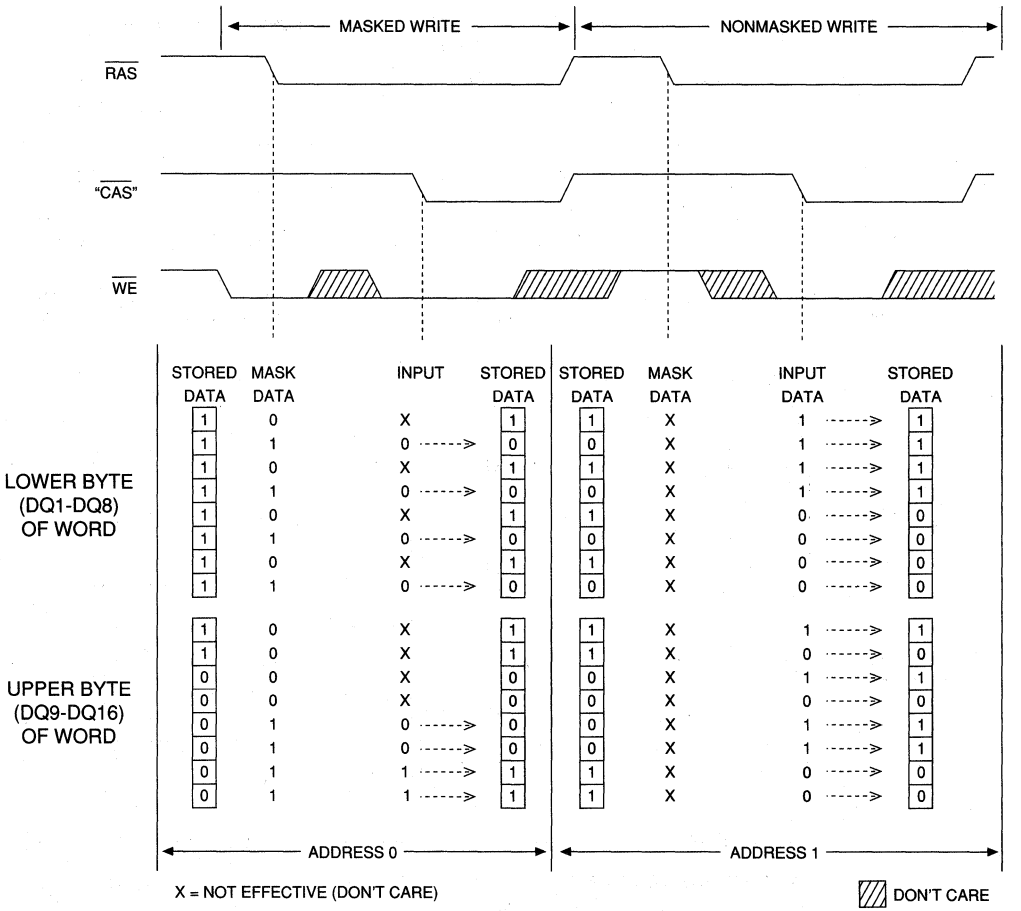


Figure 5
MT4C1M16C5 MASKED WRITE EXAMPLE

TRUTH TABLE: MT4C1M16C6/7

FUNCTION		RAS	CAS	WEL	WEH	OE	ADDRESSES tR	ADDRESSES tC	DQs	NOTES
Standby		H	H→X	X	X	X	X	X	High-Z	
READ		L	L	H	H	L	ROW	COL	Data Out	
WRITE: WORD (EARLY-WRITE)		L	L	L	L	X	ROW	COL	Data In	3
WRITE: LOWER BYTE (EARLY)		L	L	L	H	X	ROW	COL	Lower Byte, Data In Upper Byte, High-Z	3
WRITE: UPPER BYTE (EARLY)		L	L	H	L	X	ROW	COL	Lower Byte, High-Z Upper Byte, Data In	3
READ-WRITE		L	L	H→L	H→L	L→H	ROW	COL	Data Out, Data In	1, 3
PAGE-MODE	1st Cycle	L	H→L	H	H	L	ROW	COL	Data Out	
READ	2nd Cycle	L	H→L	H	H	L	n/a	COL	Data Out	
PAGE-MODE	1st Cycle	L	H→L	L	L	X	ROW	COL	Data In	1, 3
WRITE	2nd Cycle	L	H→L	L	L	X	n/a	COL	Data In	1, 3
PAGE-MODE	1st Cycle	L	H→L	H→L	H→L	L→H	ROW	COL	Data In	1, 3
READ-WRITE	2nd Cycle	L	H→L	H→L	H→L	L→H	n/a	COL	Data Out, Data In	1, 3
HIDDEN	READ	L→H→L	L	H	H	L	ROW	COL	Data Out	
REFRESH	WRITE	L→H→L	L	L	L	X	ROW	COL	Data In	1, 2, 3
RAS-ONLY REFRESH		L	H	H	H	X	ROW	n/a	High-Z	
CAS-BEFORE-RAS REFRESH		H→L	L	H	H	X	X	X	High-Z	

NOTE: 1. These cycles may also be BYTE WRITE cycles (either WEL or WEH active).
2. EARLY-WRITE only.
3. Data-in will be dependent on the mask provided (MT4C1M16C7 only). Refer to Figure 4.

TRUTH TABLE: MT4C1M16C3/5

FUNCTION		RAS	CASL	CASH	WE	OE	ADDRESSES tR	ADDRESSES tC	DQs	NOTES
Standby		H	H→X	H→X	X	X	X	X	High-Z	
READ: WORD		L	L	L	H	L	ROW	COL	Data Out	
READ: LOWER BYTE		L	L	H	H	L	ROW	COL	Lower Byte, Data Out Upper Byte, High-Z	
READ: UPPER BYTE		L	H	L	H	L	ROW	COL	Lower Byte, High-Z Upper Byte, Data Out	
WRITE: WORD (EARLY-WRITE)		L	L	L	L	X	ROW	COL	Data In	5
WRITE: LOWER BYTE (EARLY)		L	L	H	L	X	ROW	COL	Lower Byte, Data In Upper Byte, High-Z	5
WRITE: UPPER BYTE (EARLY)		L	H	L	L	X	ROW	COL	Lower Byte, High-Z Upper Byte, Data In	5
READ-WRITE		L	L	L	H→L	L→H	ROW	COL	Data Out, Data In	1, 2, 5
PAGE-MODE READ	1st Cycle	L	H→L	H→L	H	L	ROW	COL	Data Out	2
	2nd Cycle	L	H→L	H→L	H	L	n/a	COL	Data Out	2
PAGE-MODE WRITE	1st Cycle	L	H→L	H→L	L	X	ROW	COL	Data In	1, 5
	2nd Cycle	L	H→L	H→L	L	X	n/a	COL	Data In	1, 5
PAGE-MODE READ-WRITE	1st Cycle	L	H→L	H→L	H→L	L→H	ROW	COL	Data Out, Data In	1, 2, 5
	2nd Cycle	L	H→L	H→L	H→L	L→H	n/a	COL	Data Out, Data In	1, 2, 5
HIDDEN REFRESH	READ	L→H→L	L	L	H	L	ROW	COL	Data Out	2
	WRITE	L→H→L	L	L	L	X	ROW	COL	Data In	1, 3, 5
RAS-ONLY REFRESH		L	H	H	X	X	ROW	n/a	High-Z	
CAS-BEFORE-RAS REFRESH		H→L	L	L	H	X	X	X	High-Z	4

NOTE:
1. These WRITE cycles may also be BYTE WRITE cycles (either CASL or CASH active).
2. These READ cycles may also be BYTE READ cycles (either CASL or CASH active).
3. EARLY-WRITE only.
4. Only one CAS must be active (CASL or CASH).
3. Data-in will be dependent on the mask provided (MT4C1M16C5 only). Refer to Figure 5.

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS} (5V) .....-1V to +7V
Voltage on V_{CC} supply relative to V_{SS} (3V) ....-1V to +4.6V
Operating Temperature, T_A (Ambient) .....0°C to +70°C
Storage Temperature (Plastic) .....-55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC OPERATING SPECIFICATIONS FOR 5V VERSION

(Notes: 1, 3, 4, 6, 7, 42) (0°C ≤ T_A ≤ 70°C; V_{CC} = 5V ±10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.5	V	1, 44
Input High (Logic 1) Voltage, All Inputs	V_{IH}	2.4	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, All Inputs	V_{IL}	-1.0	0.8	V	1
INPUT LEAKAGE CURRENT Any Input 0V ≤ V_{IN} ≤ Vcc (All other pins not under test = 0V)	I_I	-2	2	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled, 0V ≤ V_{OUT} ≤ 5.5V)	I_{OZ}	-10	10	µA	
OUTPUT LEVELS Output High Voltage (I_{OUT} = -2.5mA)	V_{OH}	2.4		V	
Output Low Voltage (I_{OUT} = 2.1mA)	V_{OL}		0.4	V	

DC OPERATING SPECIFICATIONS FOR 3.0/3.3V VERSION

(Notes: 1, 3, 4, 6, 7, 43) (0°C ≤ T_A ≤ 70°C; V_{CC} = 3.0/3.3V ±10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	2.7	3.6	V	1, 44
Input High (Logic 1) Voltage, All Inputs	V_{IH}	2.0	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, All Inputs	V_{IL}	-1.0	0.8	V	1
INPUT LEAKAGE CURRENT Any Input 0V ≤ V_{IN} ≤ Vcc (All other pins not under test = 0V)	I_I	-2	2	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled, 0V ≤ V_{OUT} ≤ 3.6V)	I_{OZ}	-10	10	µA	
OUTPUT LEVELS Output High Voltage (I_{OUT} = -1.0mA)	V_{OH}	2.4		V	
Output Low Voltage (I_{OUT} = 1.0mA)	V_{OL}		0.4	V	

DC OPERATING SPECIFICATIONS FOR 5V VERSION

(Notes: 1, 3, 4, 6, 7, 42) ($0°C \le T_A \le 70°C$; V_{CC} = 5V ±10%)

		MAX				
PARAMETER/CONDITION	**SYMBOL**	**-6**	**-7**	**-8**	**UNITS**	**NOTES**
STANDBY CURRENT: (TTL) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC1}	2	2	2	mA	
STANDBY CURRENT: (CMOS) ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} -0.2V)	I_{CC2}	1	1	1	mA	25
OPERATING CURRENT: Random READ/WRITE Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC (MIN))	I_{CC3}	170	160	140	mA	3, 4, 44
OPERATING CURRENT: FAST PAGE MODE Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: ^tPC = ^tPC (MIN); ^tCP, ^tASC = 10ns)	I_{CC4}	130	120	110	mA	3, 4, 44
REFRESH CURRENT: $\overline{RAS}$-ONLY Average power supply current ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}: ^tRC = ^tRC (MIN))	I_{CC5}	170	160	140	mA	3, 5, 44
REFRESH CURRENT: $\overline{CAS}$-BEFORE-$\overline{RAS}$ Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC (MIN))	I_{CC6}	170	160	140	mA	3, 5

DC OPERATING SPECIFICATIONS FOR 3.0/3.3V VERSION

(Notes: 1, 3, 4, 6, 7, 43) ($0°C \le T_A \le 70°C$; V_{CC} = 3.0/3.3V ±10%)

		MAX				
PARAMETER/CONDITION	**SYMBOL**	**-6**	**-7**	**-8**	**UNITS**	**NOTES**
STANDBY CURRENT: (TTL) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC1}	1	1	1	mA	
STANDBY CURRENT: (CMOS) ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} -0.2V)	I_{CC2}	400	400	400	µA	25
OPERATING CURRENT: Random READ/WRITE Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC (MIN))	I_{CC3}	130	120	100	mA	3, 4, 44
OPERATING CURRENT: FAST PAGE MODE Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: ^tPC = ^tPC (MIN); ^tCP, ^tASC = 10ns)	I_{CC4}	90	80	70	mA	3, 4, 44
REFRESH CURRENT: $\overline{RAS}$-ONLY Average power supply current ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}: ^tRC = ^tRC (MIN))	I_{CC5}	130	120	100	mA	3, 4, 44
REFRESH CURRENT: $\overline{CAS}$-BEFORE-$\overline{RAS}$ Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC (MIN))	I_{CC6}	130	120	100	mA	3, 4

CAPACITANCE

(Note: 2)

PARAMETER	SYMBOL	MAX	UNITS	NOTES
Input Capacitance: A0-A9	C_{I1}	5	pF	2
Input Capacitance: $\overline{RAS}$, $\overline{CAS}$/($\overline{CASL}$,$\overline{CASH}$), ($\overline{WEL}$, $\overline{WEH}$)/ $\overline{WE}$, $\overline{OE}$	C_{I2}	7	pF	2
Input/Output Capacitance: DQ	C_{IO}	7	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C ≤ T_A ≤ +70°C; V_{CC} = 5V or 3.0/3.3V ±10%)

AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	^tRC	110		130		150		ns	
READ-WRITE cycle time	^tRWC	155		180		200		ns	
FAST-PAGE-MODE READ or WRITE cycle time	^tPC	35		40		40		ns	35
FAST-PAGE-MODE READ-WRITE cycle time	^tPRWC	85		95		100		ns	35
Access time from $\overline{RAS}$	^tRAC		60		70		80	ns	14
Access time from $\overline{CAS}$	^tCAC		15		20		20	ns	15, 33
Output Enable	^tOE		15		15		15	ns	23
Access time from column address	^tAA		30		35		40	ns	
Access time from $\overline{CAS}$ precharge	^tCPA		35		40		45	ns	33
$\overline{RAS}$ pulse width	^tRAS	60	100,000	70	100,000	80	100,000	ns	
$\overline{RAS}$ pulse width (FAST PAGE MODE)	^tRASP	60	100,000	70	100,000	80	100,000	ns	
$\overline{RAS}$ hold time	^tRSH	15		20		20		ns	40
$\overline{RAS}$ precharge time	^tRP	40		50		60		ns	
$\overline{CAS}$ pulse width	^tCAS	15	100,000	20	100,000	20	100,000	ns	39
$\overline{CAS}$ hold time	^tCSH	60		70		80		ns	32
$\overline{CAS}$ precharge time	^tCPN	10		10		10		ns	16, 36
$\overline{CAS}$ precharge time (FAST PAGE MODE)	^tCP	10		10		10		ns	36
$\overline{RAS}$ to $\overline{CAS}$ delay time	^tRCD	15	45	20	50	20	60	ns	17, 31
$\overline{CAS}$ to $\overline{RAS}$ precharge time	^tCRP	5		5		5		ns	32
Row address setup time	^tASR	0		0		0		ns	
Row address hold time	^tRAH	10		10		10		ns	
$\overline{RAS}$ to column address delay time	^tRAD	15	30	15	35	15	40	ns	18
Column address setup time	^tASC	0		0		0		ns	31
Column address hold time	^tCAH	10		15		15		ns	31
Column address hold time (referenced to $\overline{RAS}$)	^tAR	50		55		60		ns	
Column address to $\overline{RAS}$ lead time	^tRAL	30		35		40		ns	
Read command setup time	^tRCS	0		0		0		ns	26, 31
Read command hold time (referenced to $\overline{CAS}$)	^tRCH	0		0		0		ns	19, 26, 32
Read command hold time (referenced to $\overline{RAS}$)	^tRRH	0		0		0		ns	19
$\overline{CAS}$ to output in Low-Z	^tCLZ	0		0		0		ns	33

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C ≤ T_A ≤ +70°C; Vcc = 5V or 3.0/3.3V ±10%)

AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Output buffer turn-off delay	^tOFF	0	15	0	20	0	20	ns	20, 29, 33
$\overline{WE}$ command setup time	^tWCS	0		0		0		ns	21, 26, 31
Write command hold time	^tWCH	10		15		15		ns	26, 40
Write command hold time (referenced to $\overline{RAS}$)	^tWCR	45		55		60		ns	26
Write command pulse width	^tWP	10		15		15		ns	26
Write command to $\overline{RAS}$ lead time	^tRWL	15		20		20		ns	26
Write command to $\overline{CAS}$ lead time	^tCWL	15		20		20		ns	26, 32
Data-in setup time	^tDS	0		0		0		ns	22, 33
Data-in hold time	^tDH	10		15		15		ns	22, 33
Data-in hold time (referenced to $\overline{RAS}$)	^tDHR	45		55		60		ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	^tRWD	85		95		105		ns	21
Column address to $\overline{WE}$ delay time	^tAWD	55		60		65		ns	21
$\overline{CAS}$ to $\overline{WE}$ delay time	^tCWD	40		45		45		ns	21, 31
Transition time (rise or fall)	^tT	3	50	3	50	3	50	ns	9, 10
Refresh period (1,024 cycles)	^tREF		16		16		16	ms	28
$\overline{RAS}$ to $\overline{CAS}$ precharge time	^tRPC	0		0		0		ns	
$\overline{CAS}$ setup time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tCSR	5		5		5		ns	5, 31
$\overline{CAS}$ hold time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tCHR	15		15		15		ns	5, 32
$\overline{WE}$ hold time (MASKED WRITE and $\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tWRH	15		15		15		ns	26, 27
$\overline{WE}$ setup time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tWRP	10		10		10		ns	26
$\overline{WE}$ setup time (MASKED WRITE)	^tWRS	10		10		10		ns	26, 27
$\overline{OE}$ setup prior to RAS during HIDDEN REFRESH cycle	^tORD	0		0		0		ns	
Output disable	^tOD		15		15		15	ns	29, 41
$\overline{OE}$ hold time from $\overline{WE}$ during HIDDEN REFRESH cycle	^tOEH	15		15		15		ns	28
Last $\overline{CAS}$ going LOW to first $\overline{CAS}$ to return HIGH	^tCLCH	10		10		10		ns	34
Mask data to $\overline{RAS}$ setup time	^tMS	0		0		0		ns	26, 27
Mask data to $\overline{RAS}$ setup time	^tMH	15		15		15		ns	26, 27

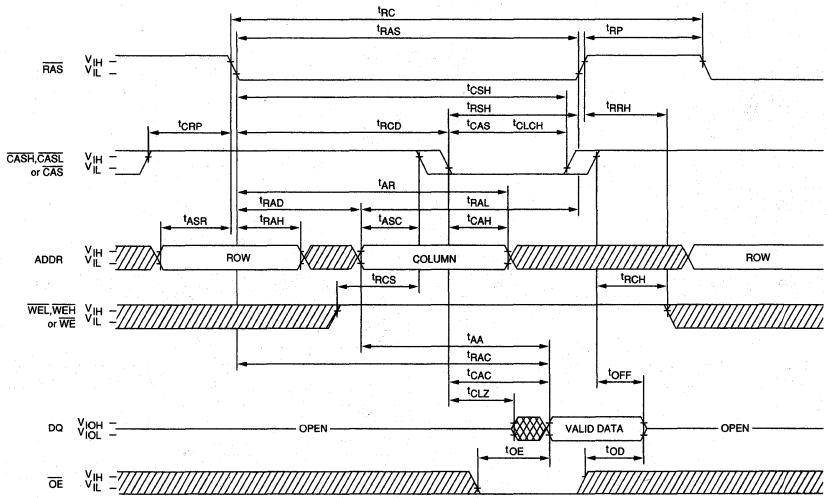
NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. V_{CC} = 5V or 3.0/3.3V ±10%; f = 1 MHz.
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \le T_A \le 70°C$) is assured.
7. An initial pause of 100µs is required after power-up followed by eight $\overline{RAS}$ refresh cycles ($\overline{RAS}$-ONLY or CBR) before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-up should be repeated any time the ^tREF refresh requirement is exceeded.
8. AC characteristics assume ^tT = 5ns.
9. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS}$ = V_{IH}, data output is High-Z.
12. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to 1 TTL gate and 50pF.
14. Assumes that $^tRCD < ^tRCD$ (MAX). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
15. Assumes that $^tRCD \ge ^tRCD$ (MAX).
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the Q buffer, $\overline{CAS}$ must be pulsed HIGH for ^tCPN.
17. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (MAX) limit, then access time is controlled exclusively by ^tCAC.
18. Operation within the ^tRAD limit ensures that ^tRCD (MAX) can be met. ^tRAD (MAX) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (MAX) limit, then access time is controlled exclusively by ^tAA.
19. Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
20. ^tOFF (MAX) defines the time at which the output achieves the open circuit condition (not a reference to V_{OH} or V_{OL}).
21. ^tWCS, ^tRWD, ^tAWD and ^tCWD are restrictive operating parameters in LATE-WRITE and READ-MODIFY-WRITE cycles only. If $^tWCS \ge ^tWCS$ (MIN), the cycle is an EARLY-WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If $^tRWD \ge ^tRWD$ (MIN), $^tAWD \ge ^tAWD$ (MIN) and $^tCWD \ge ^tCWD$ (MIN), the cycle is a READ-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of Q (at access time and until $\overline{CAS}$ or $\overline{OE}$ goes back to V_{IH}) is indeterminate. $\overline{OE}$ held HIGH and $\overline{WE}$ taken LOW after $\overline{CAS}$ goes LOW results in a LATE-WRITE ($\overline{OE}$ controlled) cycle.
22. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY-WRITE cycles and $\overline{WE}$ leading edge in LATE-WRITE or READ-MODIFY-WRITE cycles.
23. During a READ cycle, if $\overline{OE}$ is LOW then taken HIGH before $\overline{CAS}$ goes HIGH, Q goes open. If $\overline{OE}$ is tied permanently LOW, LATE-WRITE and READ-MODIFY-WRITE operations are not possible.
24. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW and $\overline{OE}$ = HIGH.
25. All other inputs at Vcc -0.2V.
26. Write command is defined as either $\overline{WEL}$ or $\overline{WEH}$ or both going LOW on the MT4C1M16C6/7. Write command is defined as $\overline{WE}$ going LOW on the MT4C1M16C3/5.
27. MT4C1M16C5/7 only.
28. LATE-WRITE and READ-MODIFY-WRITE cycles must have both ^tOD and ^tOEH met ($\overline{OE}$ HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. The DQs will provide the previously read data if $\overline{CAS}$ remains LOW and $\overline{OE}$ is taken back LOW after ^tOEH is met. If $\overline{CAS}$ goes HIGH prior to $\overline{OE}$ going back LOW, the DQs will remain open.
29. The DQs open during READ cycles once ^tOD or ^tOFF occur. If $\overline{CAS}$ goes HIGH first, $\overline{OE}$ becomes a "don't care." If $\overline{OE}$ goes HIGH and $\overline{CAS}$ stays LOW, $\overline{OE}$ is not a "don't care;" and the DQs will provide the previously read data if $\overline{OE}$ is taken back LOW (while $\overline{CAS}$ remains LOW).

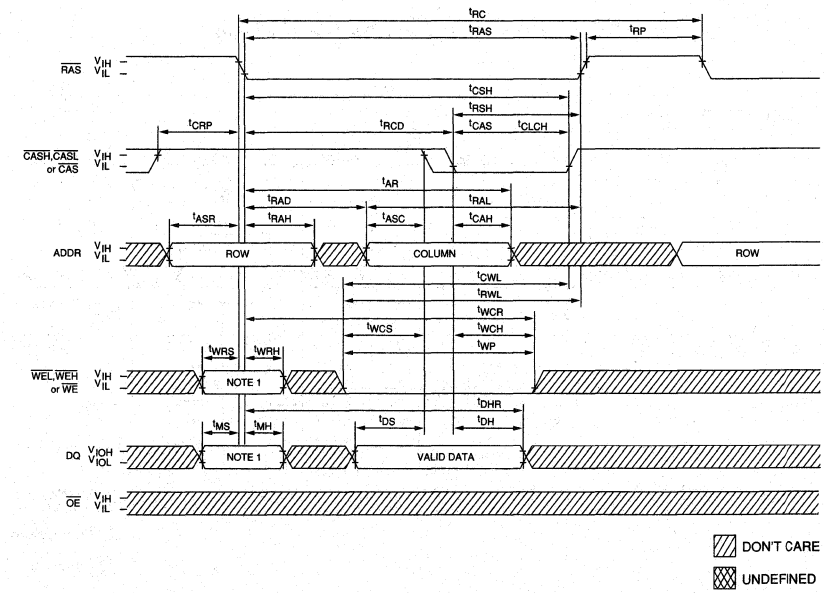
NOTES (continued)

30. Notes 31 through 41 apply to MT4C1M16C3/5 only (*).
31. *The first $\overline{CAS}$x edge to transition LOW.
32. *The last $\overline{CAS}$x edge to transition HIGH.
33. *Output parameter (DQx) is referenced to corresponding $\overline{CAS}$ input; DQ1-DQ8 by $\overline{CASL}$ and DQ9-DQ16 by $\overline{CASH}$.
34. *Last falling $\overline{CAS}$x edge to first rising $\overline{CAS}$x edge.
35. *Last rising $\overline{CAS}$x edge to next cycle's last rising $\overline{CAS}$x edge.
36. *Last rising $\overline{CAS}$x edge to first falling $\overline{CAS}$x edge.
37. *First DQs controlled by the first $\overline{CAS}$x to go LOW.
38. *Last DQs controlled by the last $\overline{CAS}$x to go HIGH.
39. *Each $\overline{CAS}$x must meet minimum pulse width.
40. *Last $\overline{CAS}$x to go LOW.
41. *All DQs controlled, regardless $\overline{CASL}$ and $\overline{CASH}$.
42. The 5V version is restricted to operate between 4.5 V and 5.5V only.
43. The 3.0/3.3V version is restricted to operate between 2.7 V and 3.6V only.
44. Column address changed once while $\overline{RAS}$ = V_{IL} and $\overline{CAS}$ = V_{IH}.

READ CYCLE

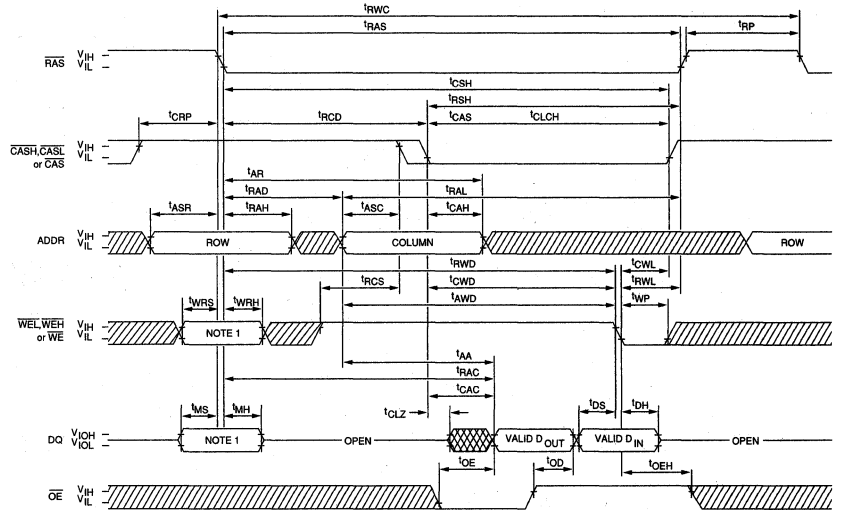


EARLY-WRITE CYCLE

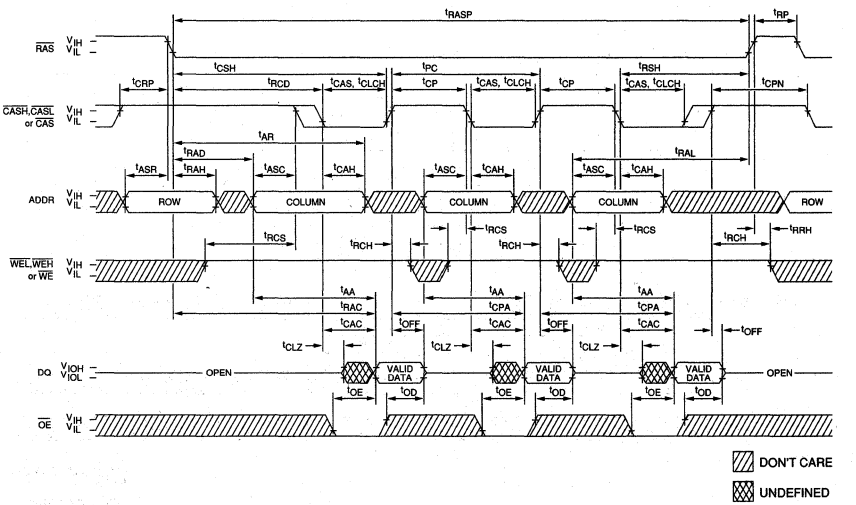


NOTE: 1. Applies to MT4C1M16C5 and MT4C1M16C7 only. $\overline{WE}$ selects between normal WRITE and MASKED WRITE at $\overline{RAS}$ time. The DQ inputs are "don't care" for a normal WRITE ($\overline{WE}$ HIGH at $\overline{RAS}$ time). The DQ inputs provide the mask data at $\overline{RAS}$ time for a MASKED WRITE ($\overline{WE}$ LOW at $\overline{RAS}$ time). $\overline{WEL}$, $\overline{WEH}$ and DQ inputs on MT4C1M16C3 and MT4C1M16C6 are "don't care" at $\overline{RAS}$ time.

READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)

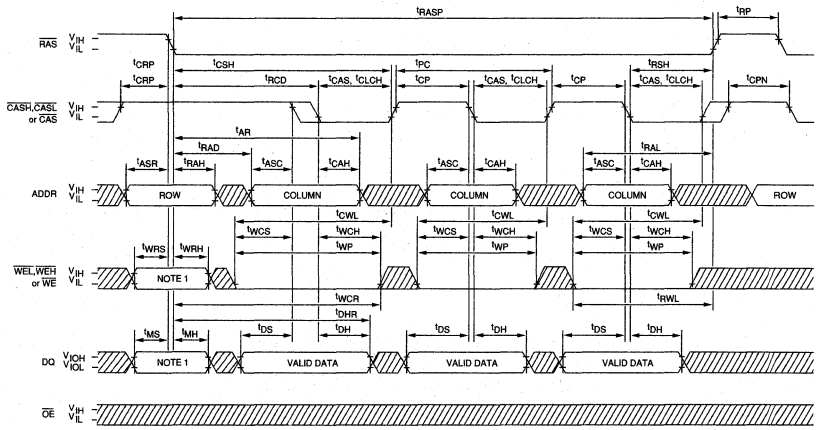


FAST-PAGE-MODE READ CYCLE

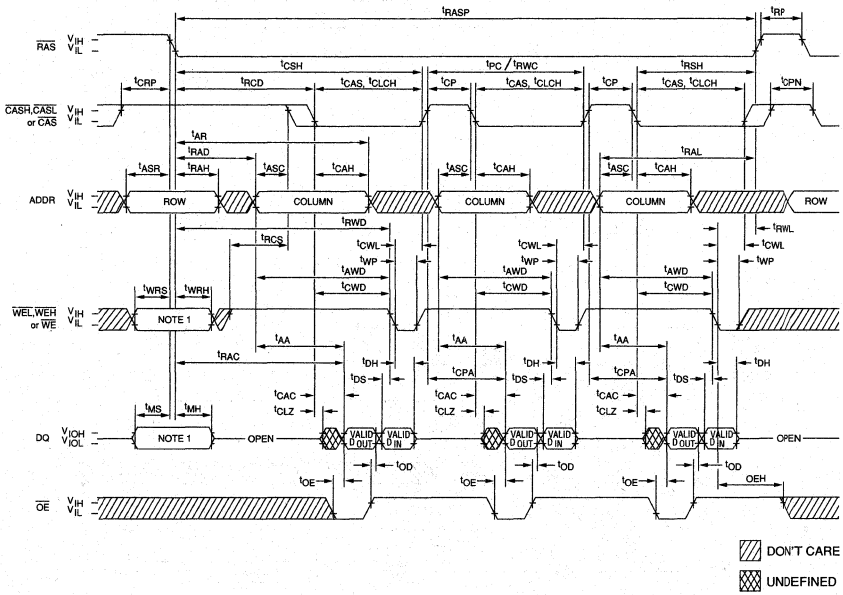


NOTE: 1. Applies to MT4C1M16C5 and MT4C1M16C7 only. $\overline{WE}$ selects between normal WRITE and MASKED WRITE at $\overline{RAS}$ time. The DQ inputs are "don't care" for a normal WRITE ($\overline{WE}$ HIGH at $\overline{RAS}$ time). The DQ inputs provide the mask data at $\overline{RAS}$ time for a MASKED WRITE ($\overline{WE}$ LOW at $\overline{RAS}$ time). $\overline{WEL}$, $\overline{WEH}$ and DQ inputs on MT4C1M16C3 and MT4C1M16C6 are "don't care" at $\overline{RAS}$ time.

FAST-PAGE-MODE EARLY-WRITE CYCLE



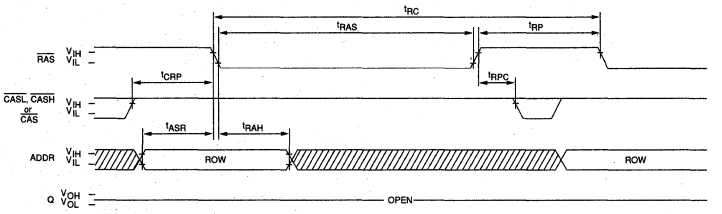
FAST-PAGE-MODE READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)



NOTE: 1. Applies to MT4C1M16C5 and MT4C1M16C7 only. $\overline{WE}$ selects between normal WRITE and MASKED WRITE at $\overline{RAS}$ time. The DQ inputs are "don't care" for a normal WRITE ($\overline{WE}$ HIGH at $\overline{RAS}$ time). The DQ inputs provide the mask data at $\overline{RAS}$ time for a MASKED WRITE ($\overline{WE}$ LOW at $\overline{RAS}$ time). $\overline{WEL}$, $\overline{WEH}$ and DQ inputs on MT4C1M16C3 and MT4C1M16C6 are "don't care" at $\overline{RAS}$ time.

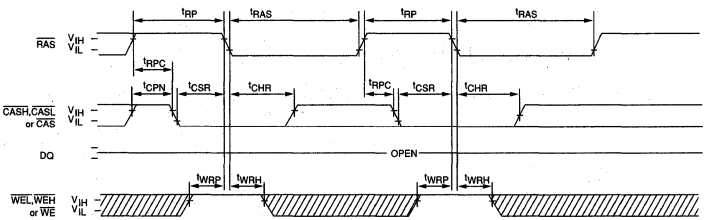
RAS-ONLY REFRESH CYCLE

(ADDR = A0-A9, OE; WEL, WEH or WE = DON'T CARE)



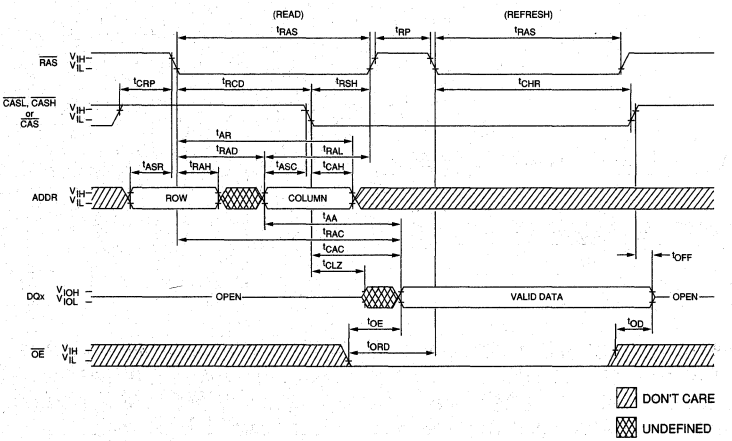
CAS-BEFORE-RAS REFRESH CYCLE

(A0-A9; and OE = DON'T CARE)



HIDDEN REFRESH CYCLE [24]

(WEL, WEH or WE = HIGH; OE = LOW)



NEW ■ WIDE DRAM

DRAM

1 MEG x 16 DRAM

5.0V SELF REFRESH (MT4C1M16CX S)
3.0/3.3V, SELF REFRESH (MT4LC1M16CX S)

FEATURES

- Self Refresh, ie "Sleep Mode"
- Industry standard x16 pinouts, timing, functions and packages
- High-performance, CMOS silicon-gate process
- Single +5V only or +3.0/+3.3V only ±10% power supply
- All device pins are fully TTL compatible
- Refresh modes: RAS-ONLY, CAS-BEFORE-RAS (CBR), HIDDEN and BATTERY BACKUP (BBU)
- Optional FAST PAGE MODE access cycle
- BYTE WRITE access cycle
- BYTE READ access cycle (MT4C1M16C3/5 S only)
- NONPERSISTENT MASKED WRITE access cycle (MT4C1M16C5/7 S only)
- 1,024 cycle refresh in 128ms (10 rows and 10 columns)
- Low power, 2mW standby; 500mW active, typical (5V)

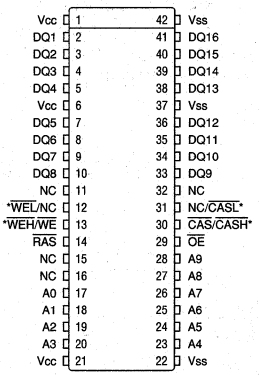
OPTIONS — MARKING

- Timing
  - 60ns access — -6
  - 70ns access — -7
  - 80ns access — -8
- Power Supply
  - +5V ±10% only — 4C
  - +3.0/3.3V ±10% only — 4LC
- Refresh Rate
  - 1,024 Rows — None
  - 4,096 Rows — Contact Factory
- Write Cycle Access
  - BYTE or WORD via CAS (non-maskable) — 16C3 S
  - BYTE or WORD via CAS (maskable) — 16C5 S
  - BYTE or WORD via WE (non-maskable) — 16C6 S
  - BYTE or WORD via WE (maskable) — 16C7 S
- Packages
  - Plastic SOJ (400 mil) — DJ
  - Plastic TSOP (400 mil) — TG
- Part Number Example: MT4C1M16C3DJ-7 S

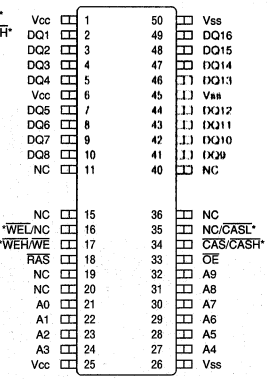
NOTE: Available in die form. Please consult factory for die data sheets.

PIN ASSIGNMENT (Top View)

42-Pin SOJ (Q-7)



44-Pin TSOP (R-6)



*MT4C1M16C6/7 S / MT4C1M16C3/5 S

GENERAL DESCRIPTION

The MT4C1M16CX S and MT4LC1M16CX S are randomly accessed solid-state memories containing 16,777,216 bits organized in a x16 configuration. The MT4C1M16CX S and the MT4LC1M16CX S are the same DRAM versions except that the MT4LC1M16CX S is the low voltage version of MT4C1M16CX S. The MT4LC1M16CX S is designed to operate in either a 3.0V ±10% or a 3.3V ±10% memory system. All further references made for the MT4C1M16CX S also apply to the MT4LC1M16CX S, unless specifically state otherwise. The MT4C1M16C6 S and MT4C1M16C7 S have both BYTE WRITE and WORD WRITE access cycles via two write enable pins. The MT4C1M16C3 S and MT4C1M16C5 S have both BYTE WRITE and WORD WRITE access cycles via two CAS pins.

NEW ■ WIDE DRAM

The MT4C1M16C5 S and MT4C1M16C7 S are also able to perform WRITE-PER-BIT accesses.

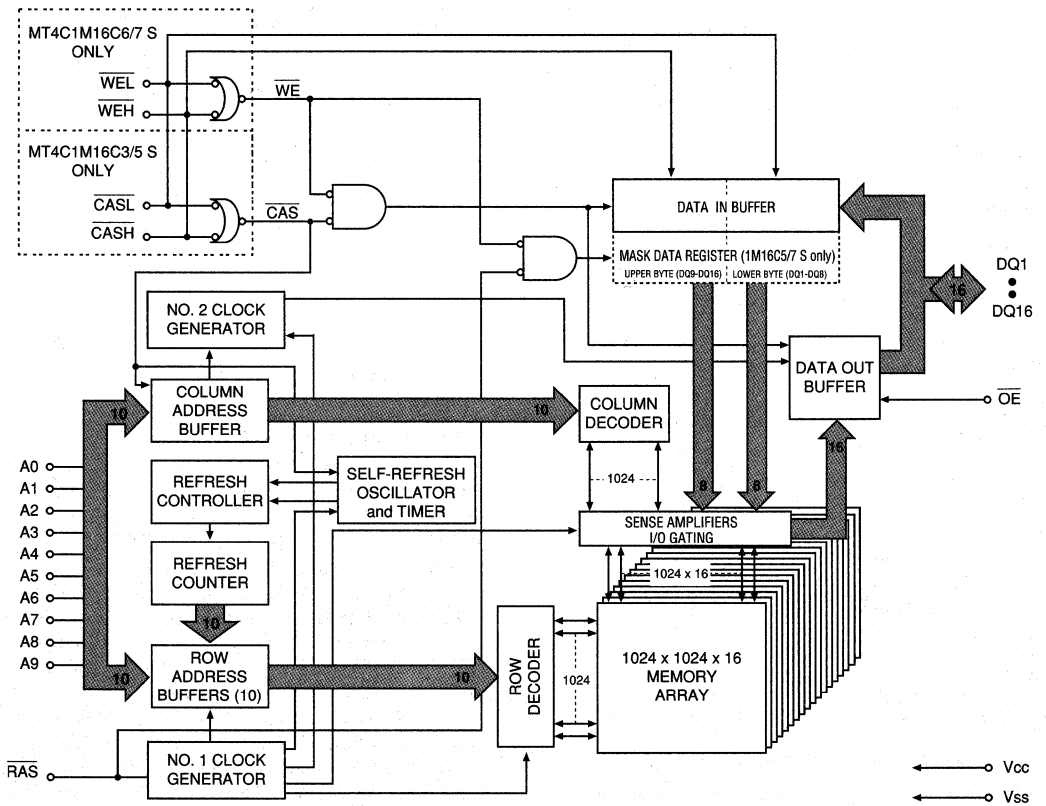
The MT4C1M16C3 S and MT4C1M16C6 S function in the same manner except that $\overline{WEL}$ and $\overline{WEH}$ on MT4C1M16C6 S and $\overline{CASL}$ and $\overline{CASH}$ on MT4C1M16C3 S control the selection of BYTE WRITE access cycles. $\overline{WEL}$ and $\overline{WEH}$ function in an identical manner to $\overline{WE}$ in that either $\overline{WEL}$ or $\overline{WEH}$ will generate an internal $\overline{WE}$. $\overline{CASL}$ and $\overline{CASH}$ function in an identical manner to $\overline{CAS}$ in that either $\overline{CASL}$ or $\overline{CASH}$ will generate an internal $\overline{CAS}$.

The MT4C1M16C6 S "$\overline{WE}$" function and timing are determined by the first $\overline{WE}$ ($\overline{WEL}$ or $\overline{WEH}$) to transition LOW and by the last to transition back HIGH. Use of only one of the two results in a BYTE WRITE cycle. $\overline{WEL}$ transitioning LOW selects a WRITE cycle for the lower byte (DQ1-DQ8), and $\overline{WEH}$ transitioning LOW selects a WRITE cycle for the upper byte (DQ9-DQ16).

The MT4C1M16C3 S "$\overline{CAS}$" function and timing are determined by the first $\overline{CAS}$ ($\overline{CASL}$ or $\overline{CASH}$) to transition LOW and the last to transition back HIGH. Use of only one of the two results in a BYTE WRITE cycle. $\overline{CASL}$ transitioning LOW selects a WRITE cycle for the lower byte (DQ1-DQ8) and $\overline{CASH}$ transitioning LOW selects a WRITE cycle for the upper byte (DQ9-DQ16). BYTE READ cycles are achieved through $\overline{CASL}$ or $\overline{CASH}$ in the same manner during READ cycles for the MT4C1M16C3 S.

The MT4C1M16C5 S and MT4C1M16C7 S function in the same manner as MT4C1M16C3 S and MT4C1M16C6 S, respectively; and they have NONPERSISTENT MASKED WRITE cycle capabilities. This option allows the MT4C1M16C5 S and MT4C1M16C7 S to operate with either normal WRITE cycles or NONPERSISTENT MASKED WRITE cycles.

FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTIONS

SOJ PINS	TSOP PINS	SYMBOL	TYPE	DESCRIPTION
14	18	$\overline{RAS}$	Input	ROW Address Strobe: $\overline{RAS}$ is used to latch-in the 10 row-address bits and strobe the $\overline{WE}$ and DQs on the MASKED WRITE option (MT4C1M16C5 S and MT4C1M16C7 S only).
30	34	$\overline{CAS}$/ $\overline{CASH}$	Input	Column Address Strobe: $\overline{CAS}$ (MT4C1M16C6/7 S) is used to latch-in the 10 column-address bits, enable the DRAM output buffers, and strobe the data inputs on WRITE cycles. $\overline{CAS}$ controls DQ1 through DQ16. Column Address Strobe Upper Byte: $\overline{CASH}$ (MT4C1M16C3/5 S) is the $\overline{CAS}$ control for DQ9 through DQ16. The DQs for the byte not being accessed will remain in a High-Z (high impedance) state during either a READ or a WRITE access cycle.
29	33	$\overline{OE}$	Input	Output Enable: $\overline{OE}$ enables the output buffers when taken LOW during a READ access cycle. $\overline{RAS}$ and $\overline{CAS}$ (MT4C1M16C6/7 S) or $\overline{CASL}$ / $\overline{CASH}$ (MT4C1M16C3/5 S) must be LOW and $\overline{WEL}$ / $\overline{WEH}$ (MT4C1M16C6/7 S) or $\overline{WE}$ (MT4C1M16C3/5 S) must be HIGH before $\overline{OE}$ will control the output buffers. Otherwise, the output buffers are in a High-Z state.
13	17	$\overline{WEH}$/$\overline{WE}$	Input	Write Enable Upper Byte: $\overline{WEH}$ (MT4C1M16C6/7 S) is $\overline{WE}$ control for the DQ9 through DQ16 inputs. If $\overline{WE}$ or $\overline{WEH}$ is LOW, the access is a WRITE cycle. If either $\overline{WE}$ or $\overline{WEH}$ is LOW at $\overline{RAS}$ time on MT4C1M16C7 S, then it is also a MASKED WRITE cycle. The DQs for the byte not being written will remain in a High-Z state (BYTE WRITE cycle only). Write Enable: $\overline{WE}$ (MT4C1M16C3/5 S) controls DQ1 through DQ16 inputs. If $\overline{WE}$ is LOW, the access is a WRITE cycle. The MT4C1M16C5/7 S also use $\overline{WE}$ to enable the MASK register during $\overline{RAS}$ time.
12	16	$\overline{WEL}$/NC	Input	Write Enable Lower Byte: $\overline{WEL}$ (MT4C1M16C6/7 S) is the $\overline{WE}$ control for DQ1 through DQ8 inputs. If $\overline{WEL}$ is LOW, the access is a WRITE cycle. If $\overline{WEL}$ is LOW at $\overline{RAS}$ time on MT4C1M16C3 S, then it is also a MASKED WRITE cycle. The DQs for the byte not being written will remain in a High-Z state (BYTE WRITE cycle only).
31	35	NC/$\overline{CASL}$	Input	Column Address Strobe Lower Byte: $\overline{CASL}$ (MT4C1M16C3/5 S) is the $\overline{CAS}$ control for DQ1 through DQ8. The DQs for the byte not being accessed will remain in a High-Z state during either a READ or a WRITE access cycle.
17-20, 23-28	21-24, 27-32	A0-A9	Input	Address Inputs: These inputs are multiplexed and clocked by $\overline{RAS}$ and $\overline{CAS}$ (or $\overline{CASL}$ / $\overline{CASH}$) to select one 16-bit word (or 8-bit byte) out of the 1 Meg available words.

PIN DESCRIPTIONS (continued)

SOJ PINS	TSOP PINS	SYMBOL	TYPE	DESCRIPTION
2-5, 7-10, 33-36, 38-41	2-5, 7-10, 41-44, 46-49	DQ1-DQ16	Input/ Output	Data I/O: For WRITE cycles, DQ1-DQ16 act as inputs to the addressed DRAM location. BYTE WRITEs can be performed by using $\overline{WEL}$ / $\overline{WEH}$ (MT4C1M16C6/7 S) or $\overline{CASL}$ / $\overline{CASH}$ (MT4C1M16C3/7 S) to select the byte to be written. For READ access cycles, DQ1-DQ16 act as outputs for the addressed DRAM location. All sixteen I/Os are active for READ cycles (MT4C1M16C6/7 S). The MT4C1M16C3/5 S allow for BYTE READ cycles.
11, 15, 16, 30-32	11, 15, 36, 40	NC	-	No Connect: These pins should be left either unconnected or tied to ground.
1, 6, 21	1, 6, 25	Vcc	Supply	Power Supply: +5V ±10% (C) or 3.0/3.3V ±10% (LC)
22, 37, 42	26, 45, 50	Vss	Supply	Ground

FUNCTIONAL DESCRIPTION

Each bit is uniquely addressed through the 20 address bits during READ or WRITE cycles. These are entered 10 bits (A0-A9) at a time. $\overline{RAS}$ is used to latch the first 10 bits and $\overline{CAS}$ the latter 10 bits.

The $\overline{CAS}$ control also determines whether the cycle will be a refresh cycle ($\overline{RAS}$-ONLY) or an active cycle (READ, WRITE or READ-WRITE) once $\overline{RAS}$ goes LOW. The MT4C1M16C6 S and MT4C1M16C7 S each have one $\overline{CAS}$ control while the MT4C1M16C3 S and MT4C1M16C5 S have two: $\overline{CASL}$ and $\overline{CASH}$.

The $\overline{CASL}$ and $\overline{CASH}$ inputs internally generate a $\overline{CAS}$ signal functioning in an identical manner to the single $\overline{CAS}$ input on the other 1 Meg x 16 DRAMs. The key difference is each $\overline{CAS}$ controls its corresponding DQ tristate logic (in conjunction with $\overline{OE}$ and $\overline{WE}$). $\overline{CASL}$ controls DQ1 through DQ8, and $\overline{CASH}$ controls DQ9 through DQ16.

The MT4C1M16C3 S and MT4C1M16C5 S "$\overline{CAS}$" function is determined by the first $\overline{CAS}$ ($\overline{CASL}$ or $\overline{CASH}$) to transition LOW and the last one to transition back HIGH. The two $\overline{CAS}$ controls give the MT4C1M16C3 S and MT4C1M16C5 S both BYTE READ and BYTE WRITE cycle capabilities.

READ or WRITE cycles on the MT4C1M16C3 S or MT4C1M16C5 S are selected with the $\overline{WE}$ input while either $\overline{WEL}$ or $\overline{WEH}$ perform the "$\overline{WE}$" on the MT4C1M16C6 S or MT4C1M16C7 S. The MT4C1M16C6 S and MT4C1M16C7 S "$\overline{WE}$" function is determined by the first BYTE WRITE ($\overline{WEL}$ or $\overline{WEH}$) to transition LOW and the last one to transition back HIGH.

A logic HIGH on $\overline{WE}$ dictates READ mode while a logic LOW on $\overline{WE}$ dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. Taking $\overline{WE}$ LOW will initiate a WRITE cycle, selecting DQ1 through DQ16. If $\overline{WE}$ goes LOW prior to $\overline{CAS}$ going LOW, the output pin(s) remain open (High- Z) until the next $\overline{CAS}$ cycle. If $\overline{WE}$ goes LOW after $\overline{CAS}$ goes LOW and data reaches the output pins, data out (Q) is activated and retains the selected cell data as long as $\overline{CAS}$ and $\overline{OE}$ remain LOW (regardless of $\overline{WE}$ or $\overline{RAS}$). This late $\overline{WE}$ pulse results in a READ-WRITE cycle.

The 16 data inputs and 16 data outputs are routed through 16 pins using common I/O. Pin direction is controlled by $\overline{OE}$, $\overline{WEL}$ and $\overline{WEH}$ (MT4C1M16C6 S and MT4C1M16C7 S) or $\overline{WE}$ (MT4C1M16C3 S and MT4C1M16C5 S).

FAST PAGE MODE operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row address (A0-A9) defined page boundary. The FAST PAGE MODE cycle is always initiated with a row address strobed-in by $\overline{RAS}$ followed by a column address strobed-in by $\overline{CAS}$. $\overline{CAS}$ may be toggled-in by holding $\overline{RAS}$ LOW and strobing-in different column addresses, thus executing faster memory cycles. Returning $\overline{RAS}$ HIGH terminates the FAST PAGE MODE operation.

Returning $\overline{RAS}$ and $\overline{CAS}$ HIGH terminates a memory cycle and decreases chip current to a reduced standby level. The chip is also preconditioned for the next cycle during the $\overline{RAS}$ high time. Memory cell data is retained in its correct state by maintaining power and executing any $\overline{RAS}$ cycle (READ, WRITE, $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$, or HIDDEN refresh) so that all 1,024 combinations of $\overline{RAS}$ addresses (A0-A9) are executed at least every 128ms, regardless of sequence. The $\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh cycle will also invoke the refresh counter and controller for ROW address control.

BATTERY BACKUP MODE (BBU) is a CBR refresh performed at the extended refresh rate with CMOS input levels. This mode provides a very low current, data retention cycle. $\overline{RAS}$ or $\overline{CAS}$ time refers to the time at which $\overline{RAS}$ or $\overline{CAS}$ transition from HIGH to LOW).

SELF REFRESH is similar to BBU except that the DRAM provides its own internal clocking during "SLEEP MODE". Thus, an external clock is not required for additional power savings and design ease. The SELF REFRESH version retains the extended refresh rate of 128ms.

BYTE ACCESS CYCLE

The BYTE WRITE mode is determined by the use of $\overline{WEL}$ and $\overline{WEH}$ or $\overline{CASL}$ and $\overline{CASH}$. Enabling $\overline{WEL}$/$\overline{CASL}$ will select a lower BYTE WRITE cycle (DQ1-DQ8). Enabling $\overline{WEH}$ or $\overline{CASH}$ will select an upper BYTE WRITE cycle (DQ9-DQ16). Enabling both $\overline{WEL}$ and $\overline{WEH}$ or $\overline{CASL}$ and $\overline{CASH}$ selects a WORD WRITE cycle.

The MT4C1M16C3 S, MT4C1M16C5 S, MT4C1M16C6 S and MT4C1M16C7 S may be viewed as two 1 Meg x 8 DRAMs that have common input controls, with the exception of the $\overline{WE}$ or the $\overline{CAS}$ inputs. Figure 1 illustrates the MT4C1M16C6 S BYTE WRITE and WORD WRITE cycles and Figure 2 illustrates the MT4C1M16C3 S BYTE WRITE and WORD WRITE cycles.

The MT4C1M16C3 S also has BYTE READ and WORD READ cycles, since it uses two $\overline{CAS}$ inputs to control its byte accesses. Figure 3 illustrates the MT4C1M16C3 S BYTE READ and WORD READ cycles.

MASKED WRITE ACCESS CYCLE (MT4C1M16C5/7 S Only)

The MASKED WRITE mode control input selects normal WRITE access or MASKED WRITE access cycles. Every WRITE access cycle can be a MASKED WRITE, depending on the state of $\overline{WE}$ at $\overline{RAS}$ time. A MASKED WRITE is selected when mask data is supplied on the DQ pins and $\overline{WE}$ is LOW at $\overline{RAS}$ time. The MT4C1M16C3 S and MT4C1M16C6 S do not have the MASKED WRITE cycle function.

The data (mask data) present on the DQ1-DQ16 inputs at $\overline{RAS}$ time will be written to an internal bit mask data register and will then act as an individual write enable for each of the corresponding DQ inputs. If a LOW (logic "0") is written to a mask data register bit, the input port for that bit is disabled during the following WRITE operation and no new data will be written to that DRAM cell location. A HIGH (logic "1") on a mask data register bit enables the input port and allows normal WRITE operations to proceed. At $\overline{CAS}$ time, the bits present on the DQ1-DQ16 inputs will be written to the DRAM (if the mask data bit was HIGH) or ignored (if the mask data bit was LOW).

New mask data must be supplied each time a MASKED WRITE cycle is initiated (non-persistent), even if the previous cycle's mask was the same.

Figure 4 illustrates the MT4C1M16C7 S MASKED WRITE operation and Figure 5 illustrates the MT4C1M16C5 S MASKED WRITE operation.

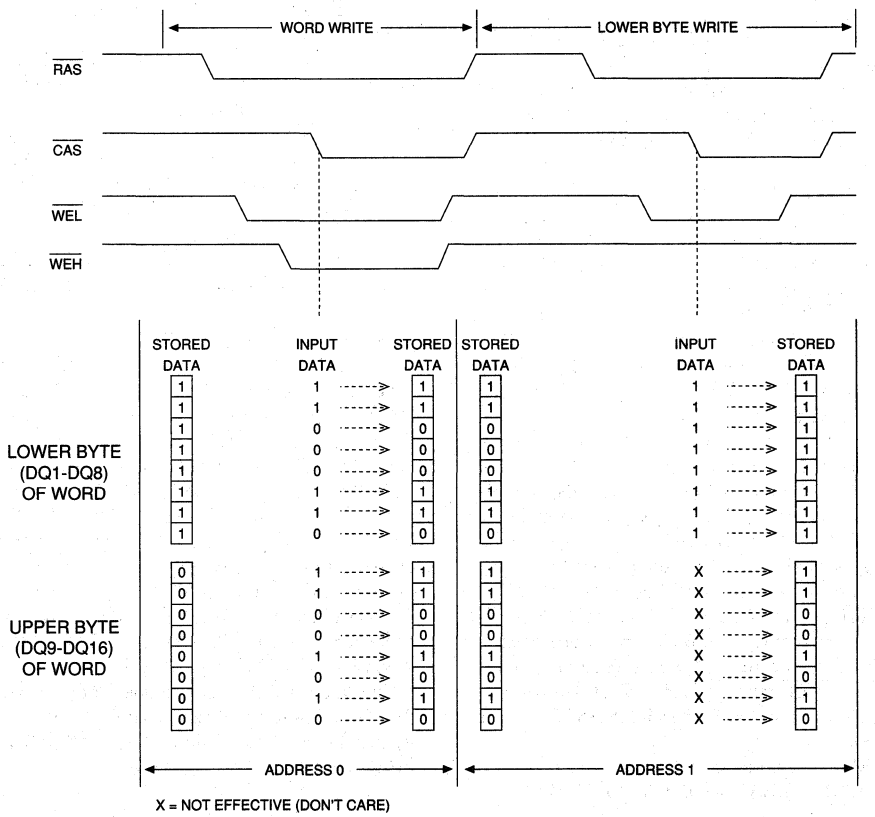


Figure 1
MT4C1M16C6/7 S WORD AND BYTE WRITE EXAMPLE

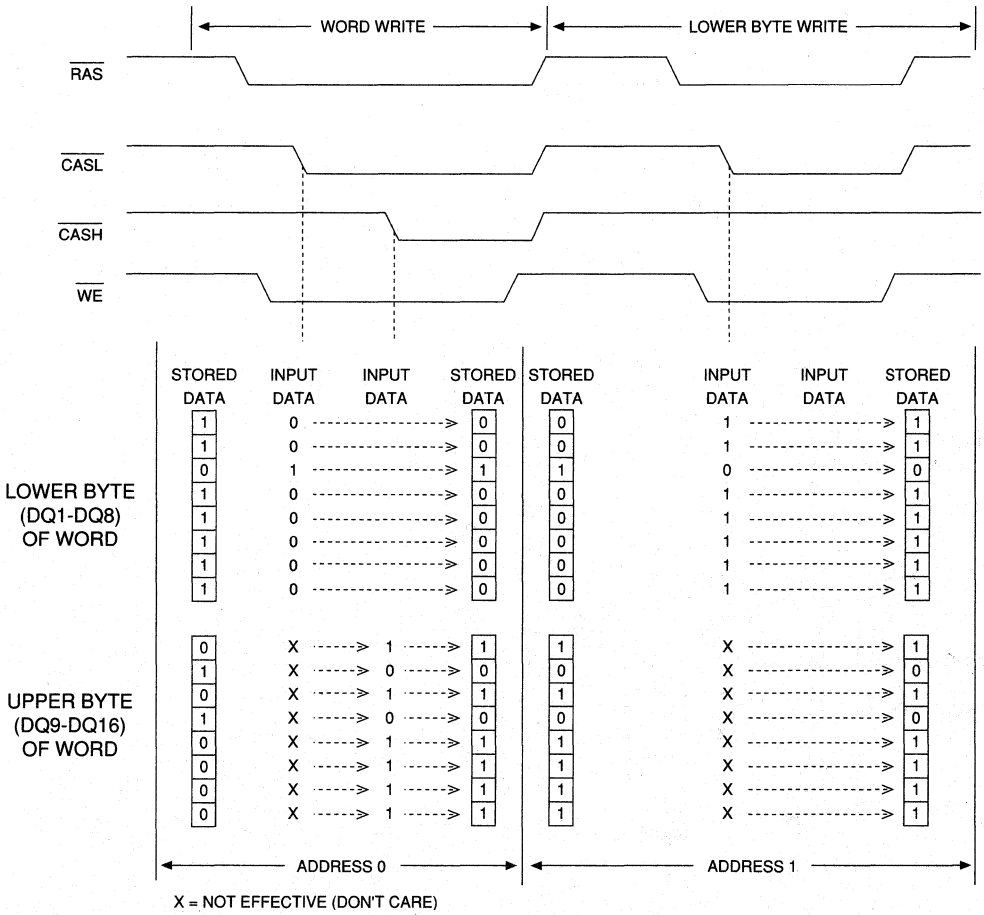


Figure 2
MT4C1M16C3/5 S WORD AND BYTE WRITE EXAMPLE

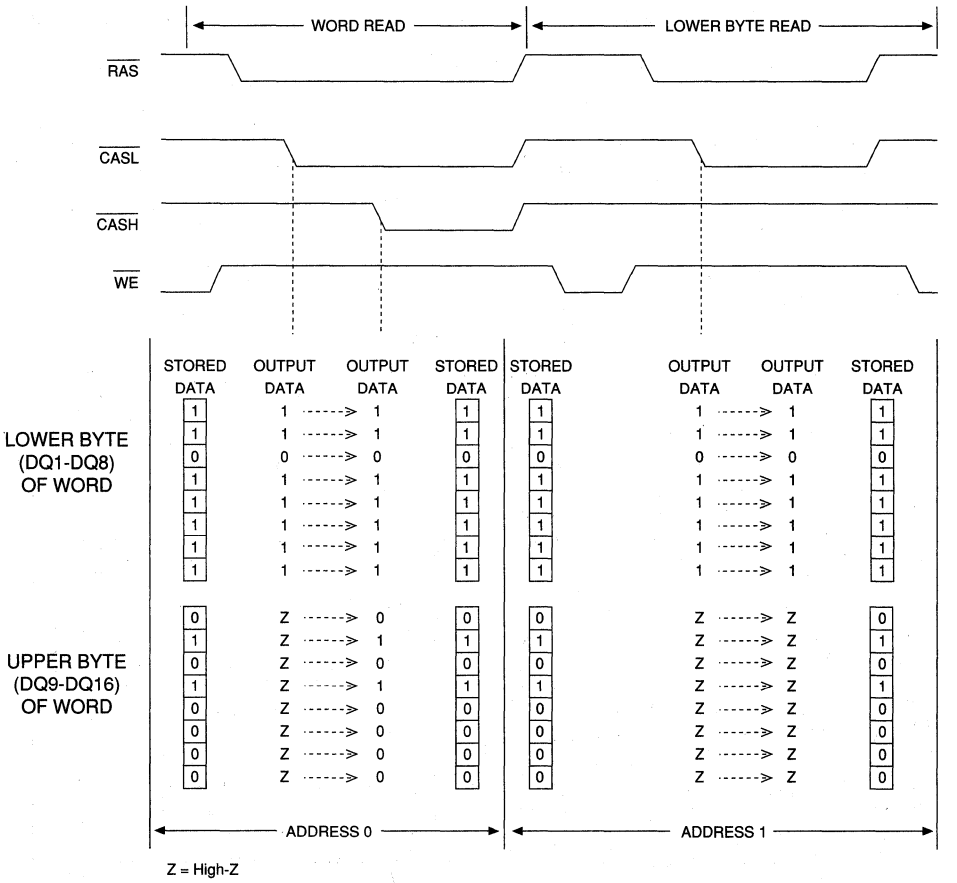


Figure 3
MT4C1M16C3/5 S WORD AND BYTE READ EXAMPLE

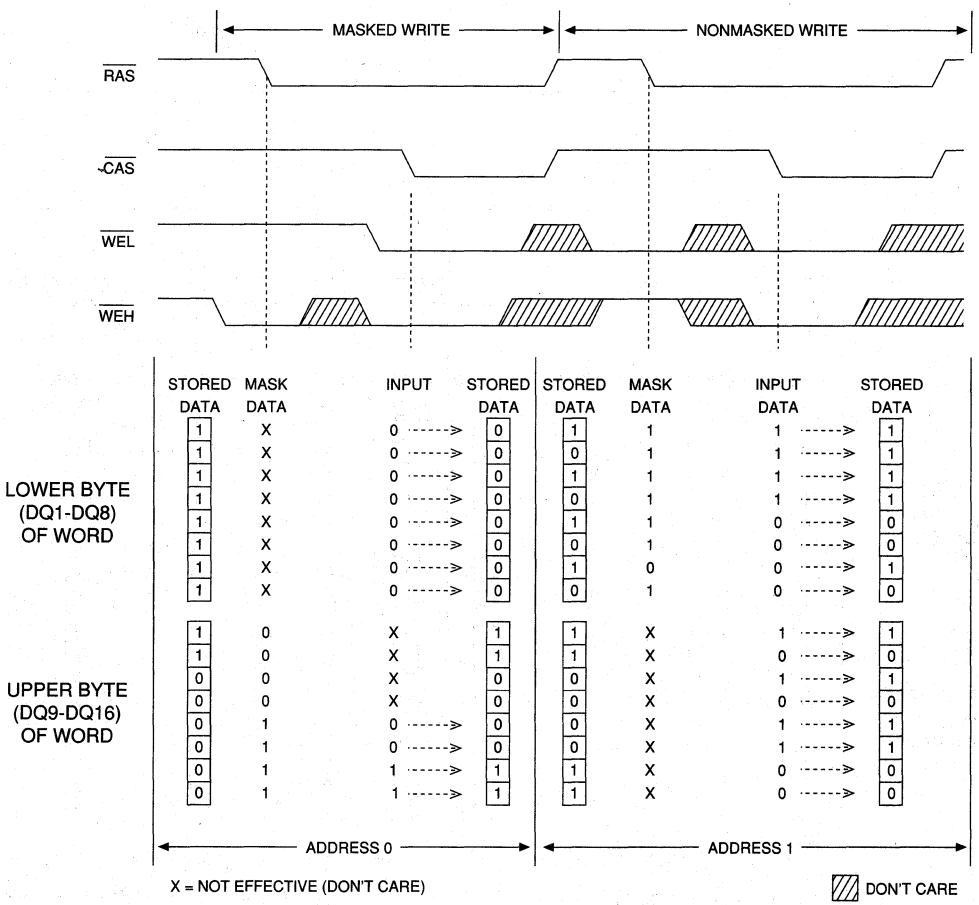


Figure 4
MT4C1M16C7 S MASKED WRITE EXAMPLE

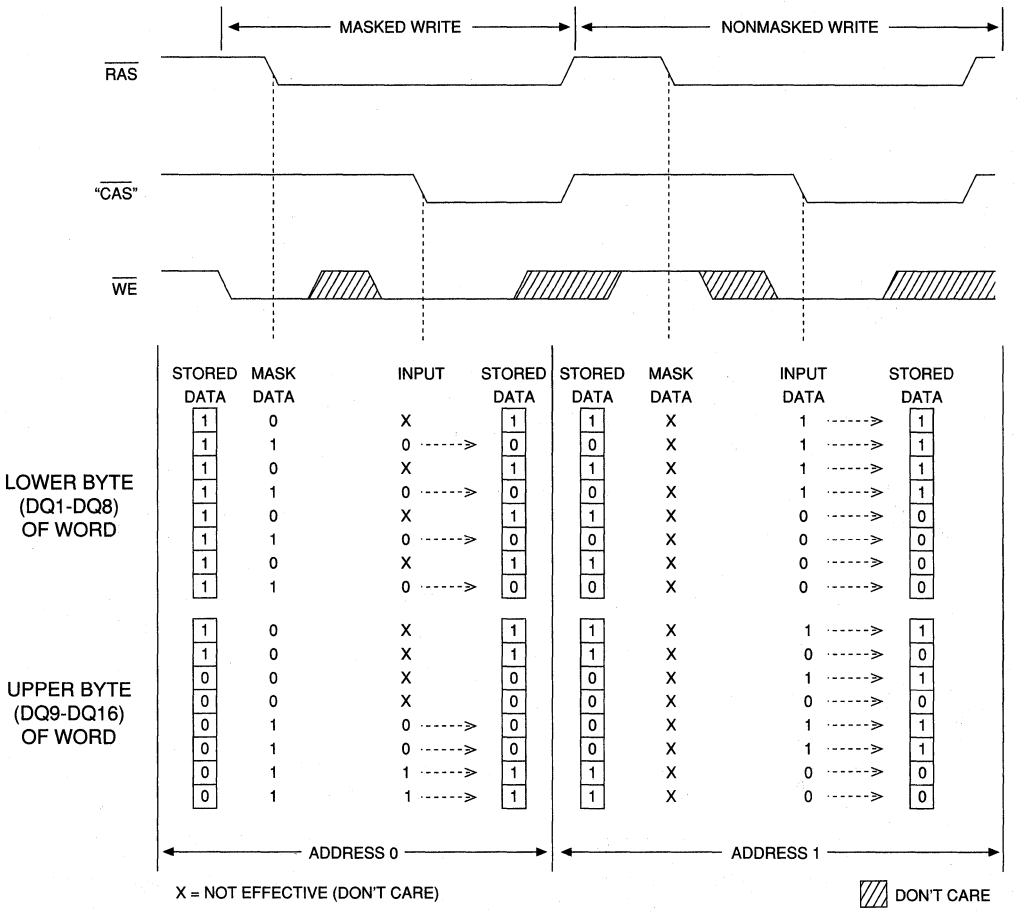


Figure 5
MT4C1M16C5 S MASKED WRITE EXAMPLE

TRUTH TABLE: MT4C1M16C6/7 S

FUNCTION		RAS	CAS	WEL	WEH	OE	ADDRESSES tR	ADDRESSES tC	DQs	NOTES
Standby		H	H→X	X	X	X	X	X	High-Z	
READ		L	L	H	H	L	ROW	COL	Data Out	
WRITE: WORD (EARLY-WRITE)		L	L	L	L	X	ROW	COL	Data In	3
WRITE: LOWER BYTE (EARLY)		L	L	L	H	X	ROW	COL	Lower Byte, Data In Upper Byte, High-Z	3
WRITE: UPPER BYTE (EARLY)		L	L	H	L	X	ROW	COL	Lower Byte, High-Z Upper Byte, Data In	3
READ-WRITE		L	L	H→L	H→L	L→H	ROW	COL	Data Out, Data In	1, 3
PAGE-MODE READ	1st Cycle	L	H→L	H	H	L	ROW	COL	Data Out	
	2nd Cycle	L	H→L	H	H	L	n/a	COL	Data Out	
PAGE-MODE WRITE	1st Cycle	L	H→L	L	L	X	ROW	COL	Data In	1, 3
	2nd Cycle	L	H→L	L	L	X	n/a	COL	Data In	1, 3
PAGE-MODE READ-WRITE	1st Cycle	L	H→L	H→L	H→L	L→H	ROW	COL	Data In	1, 3
	2nd Cycle	L	H→L	H→L	H→L	L→H	n/a	COL	Data Out, Data In	1, 3
HIDDEN REFRESH	READ	L→H→L	L	H	H	L	ROW	COL	Data Out	
	WRITE	L→H→L	L	L	L	X	ROW	COL	Data In	1, 2, 3
RAS-ONLY REFRESH		L	H	H	H	X	ROW	n/a	High-Z	
CAS-BEFORE-RAS REFRESH		H→L	L	H	H	X	X	X	High-Z	
BATTERY BACKUP REFRESH		H→L	L	H	H	X	X	X	High-Z	
SELF REFRESH		H→L	L	H	H	X	X	X	High-Z	

NOTE: 1. These cycles may also be BYTE WRITE cycles (either WEL or WEH active).
2. EARLY-WRITE only.
3. Data-in will be dependent on the mask provided (MT4C1M16C7 S only). Refer to Figure 4.

TRUTH TABLE: MT4C1M16C3/5 S

FUNCTION		RAS	CASL	CASH	WE	OE	ADDRESSES tR	ADDRESSES tC	DQs	NOTES
Standby		H	H→X	H→X	X	X	X	X	High-Z	
READ: WORD		L	L	L	H	L	ROW	COL	Data Out	
READ: LOWER BYTE		L	L	H	H	L	ROW	COL	Lower Byte, Data Out Upper Byte, High-Z	
READ: UPPER BYTE		L	H	L	H	L	ROW	COL	Lower Byte, High-Z Upper Byte, Data Out	
WRITE: WORD (EARLY-WRITE)		L	L	L	L	X	ROW	COL	Data In	5
WRITE: LOWER BYTE (EARLY)		L	L	H	L	X	ROW	COL	Lower Byte, Data In Upper Byte, High-Z	5
WRITE: UPPER BYTE (EARLY)		L	H	L	L	X	ROW	COL	Lower Byte, High-Z Upper Byte, Data In	5
READ-WRITE		L	L	L	H→L	L→H	ROW	COL	Data Out, Data In	1, 2, 5
PAGE-MODE READ	1st Cycle	L	H→L	H→L	H	L	ROW	COL	Data Out	2
	2nd Cycle	L	H→L	H→L	H	L	n/a	COL	Data Out	2
PAGE-MODE WRITE	1st Cycle	L	H→L	H→L	L	X	ROW	COL	Data In	1, 5
	2nd Cycle	L	H→L	H→L	L	X	n/a	COL	Data In	1, 5
PAGE-MODE READ-WRITE	1st Cycle	L	H→L	H→L	H→L	L→H	ROW	COL	Data Out, Data In	1, 2, 5
	2nd Cycle	L	H→L	H→L	H→L	L→H	n/a	COL	Data Out, Data In	1, 2, 5
HIDDEN REFRESH	READ	L→H→L	L	L	H	L	ROW	COL	Data Out	2
	WRITE	L→H→L	L	L	L	X	ROW	COL	Data In	1, 3, 5
RAS-ONLY REFRESH		L	H	H	X	X	ROW	n/a	High-Z	
CAS-BEFORE-RAS REFRESH		H→L	L	L	H	X	X	X	High-Z	4
BATTERY BACKUP REFRESH		H→L	L	L	H	X	X	X	High-Z	
SELF REFRESH		H→L	L	L	H	X	X	X	High-Z	

NOTE:
1. These WRITE cycles may also be BYTE WRITE cycles (either CASL or CASH active).
2. These READ cycles may also be BYTE READ cycles (either CASL or CASH active).
3. EARLY-WRITE only.
4. Only one CAS must be active (CASL or CASH).
3. Data-in will be dependent on the mask provided (MT4C1M16C5 S only). Refer to Figure 5.

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS} (5V) .....-1V to +7V
Voltage on V_{CC} supply relative to V_{SS} (3V) ....-1V to +4.6V
Operating Temperature, T_A (Ambient) .....0°C to +70°C
Storage Temperature (Plastic) .....-55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC OPERATING SPECIFICATIONS FOR 5V VERSION

(Notes: 1, 3, 4, 6, 7, 42) (0°C ≤ T_A ≤ 70°C; V_{CC} = 5V ±10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.5	V	1, 44
Input High (Logic 1) Voltage, All Inputs	V_{IH}	2.4	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, All Inputs	V_{IL}	-1.0	0.8	V	1
INPUT LEAKAGE CURRENT Any Input 0V ≤ V_{IN} ≤ V_{CC} (All other pins not under test = 0V)	I_I	-2	2	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled, 0V ≤ V_{OUT} ≤ 5.5V)	I_{OZ}	-10	10	µA	
OUTPUT LEVELS Output High Voltage (I_{OUT} = -2.5mA)	V_{OH}	2.4		V	
Output Low Voltage (I_{OUT} = 2.1mA)	V_{OL}		0.4	V	

DC OPERATING SPECIFICATIONS FOR 3.0/3.3V VERSION

(Notes: 1, 3, 4, 6, 7, 43) (0°C ≤ T_A ≤ 70°C; V_{CC} = 3.0/3.3V ±10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	2.7	3.6	V	1, 44
Input High (Logic 1) Voltage, All Inputs	V_{IH}	2.0	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, All Inputs	V_{IL}	-1.0	0.8	V	1
INPUT LEAKAGE CURRENT Any Input 0V ≤ V_{IN} ≤ Vcc (All other pins not under test = 0V)	I_I	-2	2	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled, 0V ≤ V_{OUT} ≤ 3.6V)	I_{OZ}	-10	10	µA	
OUTPUT LEVELS Output High Voltage (I_{OUT} = -1.0mA)	V_{OH}	2.4		V	
Output Low Voltage (I_{OUT} = 1.0mA)	V_{OL}		0.4	V	

DC OPERATING SPECIFICATIONS FOR 5V VERSION

(Notes: 1, 3, 4, 6, 7, 42) (0°C ≤ T_A ≤ 70°C; Vcc = 5V ±10%)

		MAX				
PARAMETER/CONDITION	**SYMBOL**	**-6**	**-7**	**-8**	**UNITS**	**NOTES**
STANDBY CURRENT: (TTL) ($\overline{RAS}$ = $\overline{CAS}$ = VIH)	ICC1	2	2	2	mA	
STANDBY CURRENT: (CMOS) ($\overline{RAS}$ = $\overline{CAS}$ = Vcc -0.2V)	ICC2	300	300	300	µA	25
OPERATING CURRENT: Random READ/WRITE Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: tRC = tRC (MIN))	ICC3	170	160	140	mA	3, 4, 44
OPERATING CURRENT: FAST PAGE MODE Average power supply current ($\overline{RAS}$ = VIL, $\overline{CAS}$, Address Cycling: tPC = tPC (MIN); tCP, tASC = 10ns)	ICC4	130	120	110	mA	3, 4, 44
REFRESH CURRENT: $\overline{RAS}$-ONLY Average power supply current ($\overline{RAS}$ Cycling, $\overline{CAS}$=VIH: tRC = tRC (MIN))	ICC5	170	160	140	mA	3, 5, 44
REFRESH CURRENT: $\overline{CAS}$-BEFORE-$\overline{RAS}$ Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: tRC = tRC (MIN))	ICC6	170	160	140	mA	3, 5
REFRESH CURRENT: BATTERY BACKUP (BBU) Average power supply current during BATTERY BACKUP refresh: $\overline{CAS}$ = 0.2V or $\overline{CAS}$-BEFORE-$\overline{RAS}$ cycling; $\overline{RAS}$ = tRAS (MIN) to 300ns; $\overline{WE}$, A0-A11 and DIN = Vcc - 0.2V (DIN may be left open), tRC = 125µs (1,024 rows at 125µs = 128ms)	ICC7	400	400	400	µA	3, 42
REFRESH CURRENT: SELF Average power supply current during SELF refresh: CBR cycle with $\overline{RAS}$ ≥ tRASS (MIN) and $\overline{CAS}$ held LOW; $\overline{WE}$ = Vcc - 0.2V; A0-A9 and DIN = Vcc - 0.2V or 0.2V (DIN may be left open)	ICC8	400	400	400	µA	5

DC OPERATING SPECIFICATIONS FOR 3.0/3.3V VERSION

(Notes: 1, 3, 4, 6, 7, 43) (0°C ≤ T_A ≤ 70°C; V_{CC} = 3.0/3.3V ±10%)

		MAX				
PARAMETER/CONDITION	**SYMBOL**	**-6**	**-7**	**-8**	**UNITS**	**NOTES**
STANDBY CURRENT: (TTL) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC1}	1	1	1	mA	
STANDBY CURRENT: (CMOS) ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} -0.2V)	I_{CC2}	80	80	80	µA	25
OPERATING CURRENT: Random READ/WRITE Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC (MIN))	I_{CC3}	130	120	100	mA	3, 4, 44
OPERATING CURRENT: FAST PAGE MODE Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: ^tPC = ^tPC (MIN); ^tCP, ^tASC = 10ns)	I_{CC4}	90	80	70	mA	3, 4, 44
REFRESH CURRENT: $\overline{RAS}$-ONLY Average power supply current ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}: ^tRC = ^tRC (MIN))	I_{CC5}	130	120	100	mA	3, 4, 44
REFRESH CURRENT: $\overline{CAS}$-BEFORE-$\overline{RAS}$ Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC (MIN))	I_{CC6}	130	120	100	mA	3, 4
REFRESH CURRENT: BATTERY BACKUP (BBU) Average power supply current during BATTERY BACKUP refresh: $\overline{CAS}$ = 0.2V or $\overline{CAS}$-BEFORE-$\overline{RAS}$ cycling; $\overline{RAS}$ = ^tRAS (MIN) to 300ns; $\overline{WE}$, A0-A11 and D_{IN} = V_{CC} - 0.2V (D_{IN} may be left open), ^tRC = 125µs (1,024 rows at 125µs = 128ms)	I_{CC7}	100	100	100	µA	3, 42
REFRESH CURRENT: SELF Average power supply current during SELF refresh: CBR cycle with $\overline{RAS}$ ≥ ^tRASS (MIN) and $\overline{CAS}$ held LOW; $\overline{WE}$ = V_{CC} - 0.2V; A0-A9 and D_{IN} = V_{CC} - 0.2V or 0.2V (D_{IN} may be left open)	I_{CC8}	100	100	100	µA	5

CAPACITANCE

(Note: 2)

PARAMETER	SYMBOL	MAX	UNITS	NOTES
Input Capacitance: A0-A9	C_{I1}	5	pF	2
Input Capacitance: $\overline{RAS}$, $\overline{CAS}$/($\overline{CASL}$,$\overline{CASH}$), ($\overline{WEL}$, $\overline{WEH}$)/ $\overline{WE}$, $\overline{OE}$	C_{I2}	7	pF	2
Input/Output Capacitance: DQ	C_{IO}	7	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C ≤ T_A ≤ +70°C; Vcc = 5V or 3.0/3.3V ±10%)

AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	^tRC	110		130		150		ns	
READ-WRITE cycle time	^tRWC	155		180		200		ns	
FAST-PAGE-MODE READ or WRITE cycle time	^tPC	35		40		40		ns	35
FAST-PAGE-MODE READ-WRITE cycle time	^tPRWC	85		95		100		ns	35
Access time from $\overline{RAS}$	^tRAC		60		70		80	ns	14
Access time from $\overline{CAS}$	^tCAC		15		20		20	ns	15, 33
Output Enable	^tOE		15		15		15	ns	33
Access time from column address	^tAA		30		35		40	ns	
Access time from $\overline{CAS}$ precharge	^tCPA		35		40		45	ns	33
$\overline{RAS}$ pulse width	^tRAS	60	100,000	70	100,000	80	100,000	ns	
$\overline{RAS}$ pulse width (FAST PAGE MODE)	^tRASP	60	100,000	70	100,000	80	100,000	ns	
$\overline{RAS}$ hold time	^tRSH	15		20		20		ns	40
$\overline{RAS}$ precharge time	^tRP	40		50		60		ns	
$\overline{CAS}$ pulse width	^tCAS	15	100,000	20	100,000	20	100,000	ns	39
$\overline{CAS}$ hold time	^tCSH	60		70		80		ns	32
$\overline{CAS}$ precharge time	^tCPN	10		10		10		ns	16, 36
$\overline{CAS}$ precharge time (FAST PAGE MODE)	^tCP	10		10		10		ns	36
$\overline{RAS}$ to $\overline{CAS}$ delay time	^tRCD	15	45	20	50	20	60	ns	17, 31
$\overline{CAS}$ to $\overline{RAS}$ precharge time	^tCRP	5		5		5		ns	32
Row address setup time	^tASR	0		0		0		ns	
Row address hold time	^tRAH	10		10		10		ns	
$\overline{RAS}$ to column address delay time	^tRAD	15	30	15	35	15	40	ns	18
Column address setup time	^tASC	0		0		0		ns	31
Column address hold time	^tCAH	10		15		15		ns	31
Column address hold time (referenced to $\overline{RAS}$)	^tAR	50		55		60		ns	
Column address to $\overline{RAS}$ lead time	^tRAL	30		35		40		ns	
Read command setup time	^tRCS	0		0		0		ns	26, 31
Read command hold time (referenced to $\overline{CAS}$)	^tRCH	0		0		0		ns	19, 26, 32
Read command hold time (referenced to $\overline{RAS}$)	^tRRH	0		0		0		ns	19
$\overline{CAS}$ to output in Low-Z	^tCLZ	0		0		0		ns	33

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C ≤ T_A ≤ +70°C; Vcc = 5V or 3.0/3.3V ±10%)

AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Output buffer turn-off delay	^tOFF	0	15	0	20	0	20	ns	20, 29, 33
$\overline{WE}$ command setup time	^tWCS	0		0		0		ns	21, 26, 31
Write command hold time	^tWCH	10		15		15		ns	26, 40
Write command hold time (referenced to $\overline{RAS}$)	^tWCR	45		55		60		ns	26
Write command pulse width	^tWP	10		15		15		ns	26
Write command to $\overline{RAS}$ lead time	^tRWL	15		20		20		ns	26
Write command to $\overline{CAS}$ lead time	^tCWL	15		20		20		ns	26, 32
Data-in setup time	^tDS	0		0		0		ns	22, 33
Data-in hold time	^tDH	10		15		15		ns	22, 33
Data-in hold time (referenced to $\overline{RAS}$)	^tDHR	45		55		60		ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	^tRWD	85		95		105		ns	21
Column address to $\overline{WE}$ delay time	^tAWD	55		60		65		ns	21
$\overline{CAS}$ to $\overline{WE}$ delay time	^tCWD	40		45		45		ns	21, 31
Transition time (rise or fall)	^tT	3	50	3	50	3	50	ns	9, 10
Refresh period (1,024 cycles)	^tREF		128		128		128	ms	28
$\overline{RAS}$ to $\overline{CAS}$ precharge time	^tRPC	0		0		0		ns	
$\overline{CAS}$ setup time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tCSR	5		5		5		ns	5, 31
$\overline{CAS}$ hold time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tCHR	15		15		15		ns	5, 32
$\overline{WE}$ hold time (MASKED WRITE and $\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tWRH	15		15		15		ns	26, 27
$\overline{WE}$ setup time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tWRP	10		10		10		ns	26
$\overline{WE}$ setup time (MASKED WRITE)	^tWRS	10		10		10		ns	26, 27
$\overline{OE}$ setup prior to RAS during HIDDEN REFRESH cycle	^tORD	0		0		0		ns	
Output disable	^tOD		15		15		15	ns	29, 41
$\overline{OE}$ hold time from $\overline{WE}$ during READ-MODIFY-WRITE cycle	^tOEH	15		15		15		ns	28
Last $\overline{CAS}$ going LOW to first $\overline{CAS}$ to return HIGH	^tCLCH	10		10		10		ns	34
Mask data to $\overline{RAS}$ setup time	^tMS	0		0		0		ns	26, 27
Mask data to $\overline{RAS}$ setup time	^tMH	15		15		15		ns	26, 27
$\overline{RAS}$ pulse width during SELF REFRESH cycle	^tRASS	100		100		100		µs	46
$\overline{RAS}$ precharge time during SELF REFRESH cycle	^tRPS	150		150		150		ns	46
$\overline{CAS}$ hold time during SELF REFRESH cycle	^tCHS	-70		-70		-70		ns	46

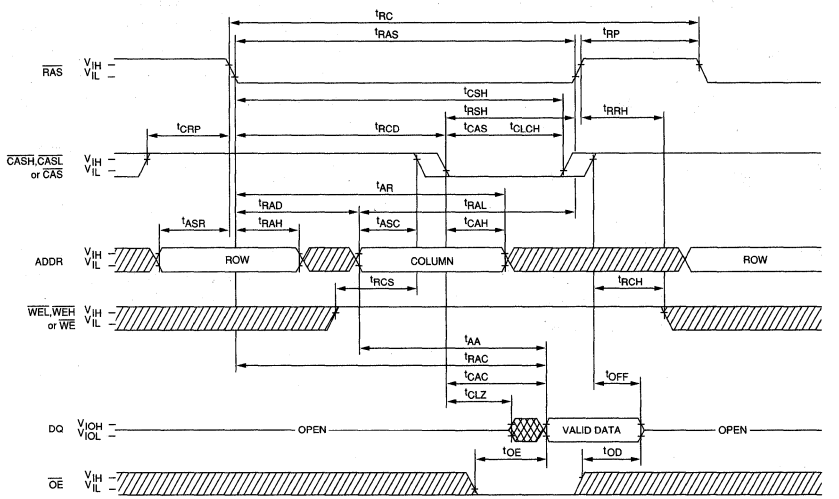
NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. V_{CC} = 5V or 3.0/3.3V ±10%; f = 1 MHz.
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \le T_A \le 70°C$) is assured.
7. An initial pause of 100µs is required after power-up followed by eight $\overline{RAS}$ refresh cycles ($\overline{RAS}$-ONLY or CBR) before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-up should be repeated any time the ^tREF refresh requirement is exceeded.
8. AC characteristics assume ^tT = 5ns.
9. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS}$ = V_{IH}, data output is High-Z.
12. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to 1 TTL gate and 50pF.
14. Assumes that $^tRCD < ^tRCD$ (MAX). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
15. Assumes that $^tRCD \ge ^tRCD$ (MAX).
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the Q buffer, $\overline{CAS}$ must be pulsed HIGH for ^tCPN.
17. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (MAX) limit, then access time is controlled exclusively by ^tCAC.
18. Operation within the ^tRAD limit ensures that ^tRCD (MAX) can be met. ^tRAD (MAX) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (MAX) limit, then access time is controlled exclusively by ^tAA.
19. Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
20. ^tOFF (MAX) defines the time at which the output achieves the open circuit condition (not a reference to V_{OH} or V_{OL}).
21. ^tWCS, ^tRWD, ^tAWD and ^tCWD are restrictive operating parameters in LATE-WRITE and READ-MODIFY-WRITE cycles only. If $^tWCS \ge ^tWCS$ (MIN), the cycle is an EARLY-WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If $^tRWD \ge ^tRWD$ (MIN), $^tAWD \ge ^tAWD$ (MIN) and $^tCWD \ge ^tCWD$ (MIN), the cycle is a READ-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of Q (at access time and until $\overline{CAS}$ or $\overline{OE}$ goes back to V_{IH}) is indeterminate. $\overline{OE}$ held HIGH and $\overline{WE}$ taken LOW after $\overline{CAS}$ goes LOW results in a LATE-WRITE ($\overline{OE}$ controlled) cycle.
22. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY-WRITE cycles and $\overline{WE}$ leading edge in LATE-WRITE or READ-MODIFY-WRITE cycles.
23. During a READ cycle, if $\overline{OE}$ is LOW then taken HIGH before $\overline{CAS}$ goes HIGH, Q goes open. If $\overline{OE}$ is tied permanently LOW, LATE-WRITE and READ-MODIFY-WRITE operations are not possible.
24. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW and $\overline{OE}$ = HIGH.
25. All other inputs at Vcc -0.2V.
26. Write command is defined as either $\overline{WEL}$ or $\overline{WEH}$ or both going LOW on the MT4C1M16C6/7 S. Write command is defined as $\overline{WE}$ going LOW on the MT4C1M16C3/5 S.
27. MT4C1M16C5/7 S only.
28. LATE-WRITE and READ-MODIFY-WRITE cycles must have both ^tOD and ^tOEH met ($\overline{OE}$ HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. The DQs will provide the previously read data if $\overline{CAS}$ remains LOW and $\overline{OE}$ is taken back LOW after ^tOEH is met. If $\overline{CAS}$ goes HIGH prior to $\overline{OE}$ going back LOW, the DQs will remain open.
29. The DQs open during READ cycles once ^tOD or ^tOFF occur. If $\overline{CAS}$ goes HIGH first, $\overline{OE}$ becomes a "don't care." If $\overline{OE}$ goes HIGH and $\overline{CAS}$ stays LOW, $\overline{OE}$ is not a "don't care;" and the DQs will provide the previously read data if $\overline{OE}$ is taken back LOW (while $\overline{CAS}$ remains LOW).

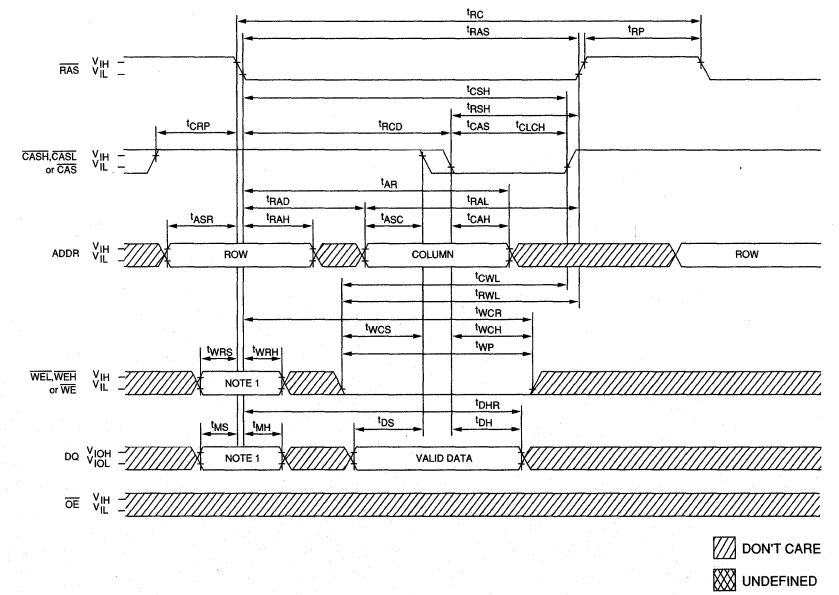
NOTES (continued)

30. Notes 31 through 41 apply to MT4C1M16C3/5 S only (*).
31. *The first $\overline{CAS}$x edge to transition LOW.
32. *The last $\overline{CAS}$x edge to transition HIGH.
33. *Output parameter (DQx) is referenced to corresponding $\overline{CAS}$ input; DQ1-DQ8 by $\overline{CASL}$ and DQ9-DQ16 by $\overline{CASH}$.
34. *Last falling $\overline{CAS}$x edge to first rising $\overline{CAS}$x edge.
35. *Last rising $\overline{CAS}$x edge to next cycle's last rising $\overline{CAS}$x edge.
36. *Last rising $\overline{CAS}$x edge to first falling $\overline{CAS}$x edge.
37. *First DQs controlled by the first $\overline{CAS}$x to go LOW.
38. *Last DQs controlled by the last $\overline{CAS}$x to go HIGH.
39. *Each $\overline{CAS}$x must meet minimum pulse width.
40. *Last $\overline{CAS}$x to go LOW.
41. *All DQs controlled, regardless $\overline{CASL}$ and $\overline{CASH}$.
42. BBU current is reduced as ^{t}RAS is reduced from its maximum specification during BBU cycle.
43. The 5V version is restricted to operate between 4.5 V and 5.5V only.
44. The 3.0/3.3V version is restricted to operate between 2.7 V and 3.6V only.
45. Column address changed once while $\overline{RAS}$ = V_{IL} and $\overline{CAS}$ = V_{IH}.
46. When exiting the SELF REFRESH mode, a complete set of row refreshes must be executed in order to ensure the DRAM will be fully refreshed.

READ CYCLE

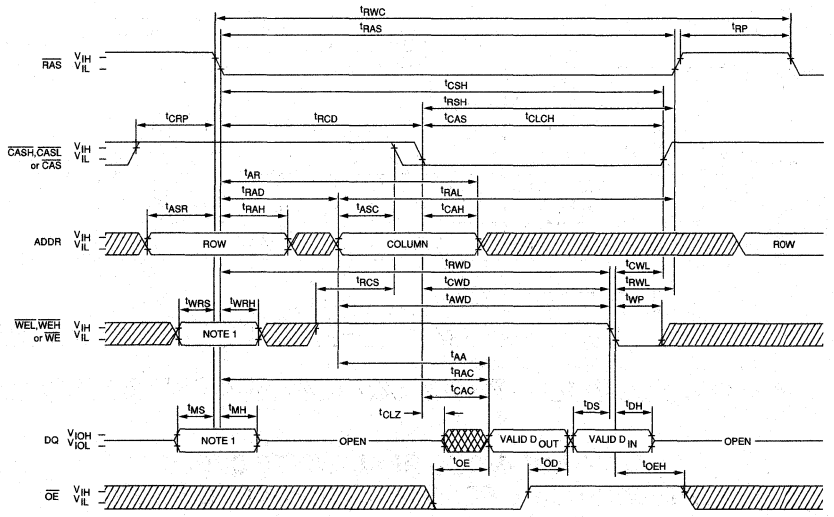


EARLY-WRITE CYCLE

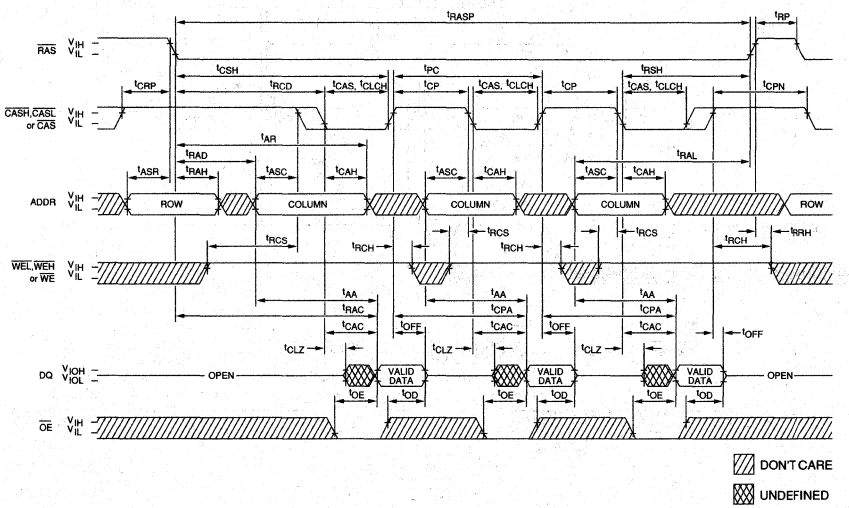


NOTE: 1. Applies to MT4C1M16C5 S and MT4C1M16C7 S only. $\overline{WE}$ selects between normal WRITE and MASKED WRITE at $\overline{RAS}$ time. The DQ inputs are "don't care" for a normal WRITE ($\overline{WE}$ HIGH at $\overline{RAS}$ time). The DQ inputs provide the mask data at $\overline{RAS}$ time for a MASKED WRITE ($\overline{WE}$ LOW at $\overline{RAS}$ time). $\overline{WEL}$, $\overline{WEH}$ and DQ inputs on MT4C1M16C3 S and MT4C1M16C6 S are "don't care" at $\overline{RAS}$ time.

READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)



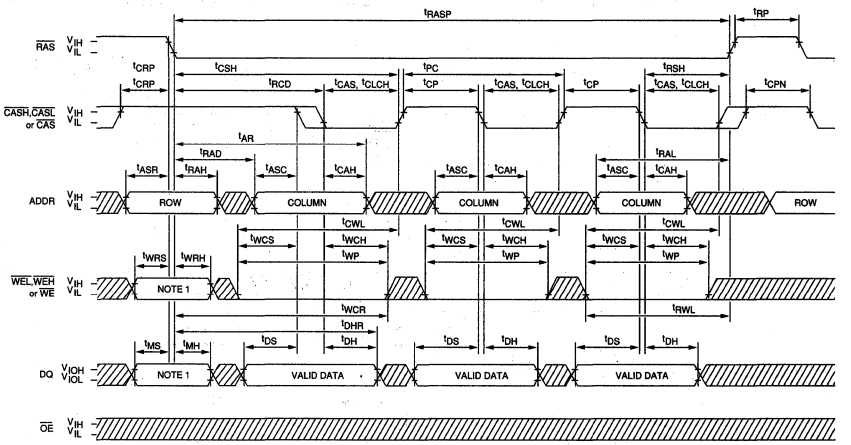
FAST-PAGE-MODE READ CYCLE



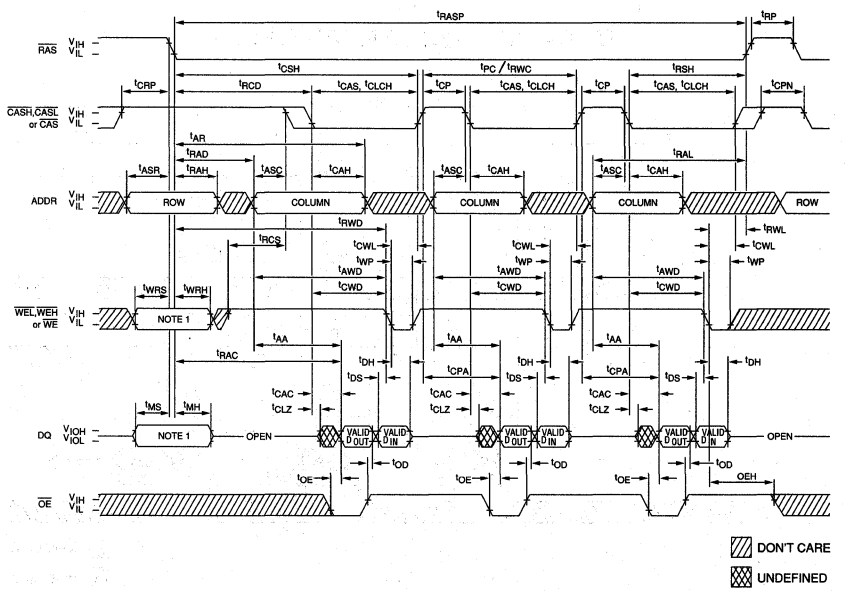
NOTE: 1. Applies to MT4C1M16C5 S and MT4C1M16C7 S only. $\overline{WE}$ selects between normal WRITE and MASKED WRITE at $\overline{RAS}$ time. The DQ inputs are "don't care" for a normal WRITE ($\overline{WE}$ HIGH at $\overline{RAS}$ time). The DQ inputs provide the mask data at $\overline{RAS}$ time for a MASKED WRITE ($\overline{WE}$ LOW at $\overline{RAS}$ time). $\overline{WEL}$, $\overline{WEH}$ and DQ inputs on MT4C1M16C3 S and MT4C1M16C6 S are "don't care" at $\overline{RAS}$ time.

NEW ■ WIDE DRAM

FAST-PAGE-MODE EARLY-WRITE CYCLE

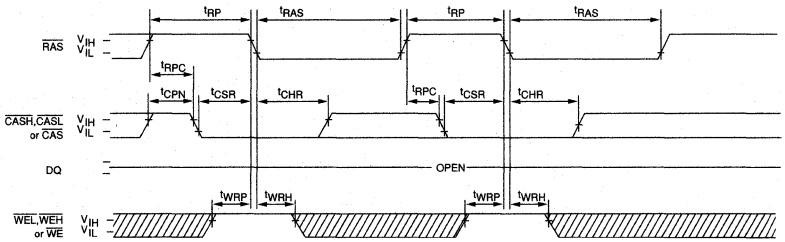


FAST-PAGE-MODE READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)

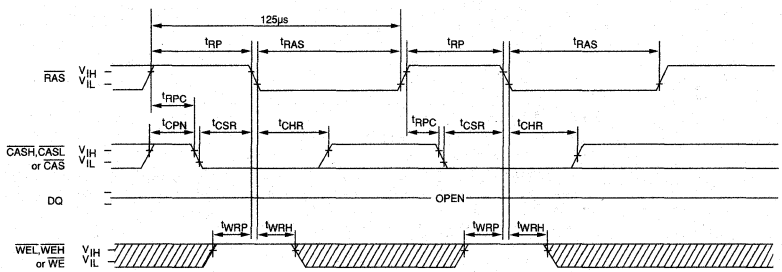


NOTE: 1. Applies to MT4C1M16C5 S and MT4C1M16C7 S only. $\overline{WE}$ selects between normal WRITE and MASKED WRITE at $\overline{RAS}$ time. The DQ inputs are "don't care" for a normal WRITE ($\overline{WE}$ HIGH at $\overline{RAS}$ time). The DQ inputs provide the mask data at $\overline{RAS}$ time for a MASKED WRITE ($\overline{WE}$ LOW at $\overline{RAS}$ time). $\overline{WEL}$, $\overline{WEH}$ and DQ inputs on MT4C1M16C3 S and MT4C1M16C6 S are "don't care" at $\overline{RAS}$ time.

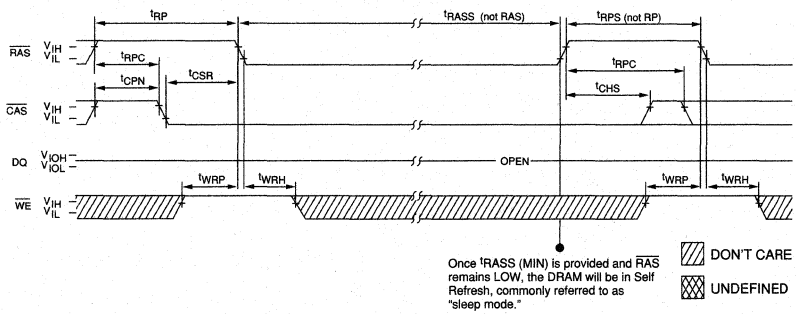
$\overline{\text{CAS}}$-BEFORE-$\overline{\text{RAS}}$ REFRESH CYCLE
(A0-A9; and $\overline{\text{OE}}$ = DON'T CARE)



BATTERY BACKUP REFRESH CYCLE
(A0-A9; and $\overline{\text{OE}}$ = DON'T CARE)

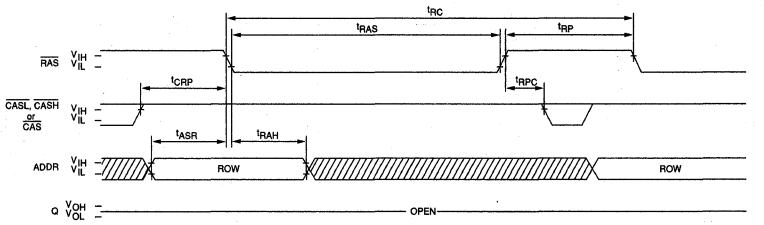


SELF REFRESH CYCLE ("SLEEP MODE")
(A0-A9; and $\overline{\text{OE}}$ = DON'T CARE)



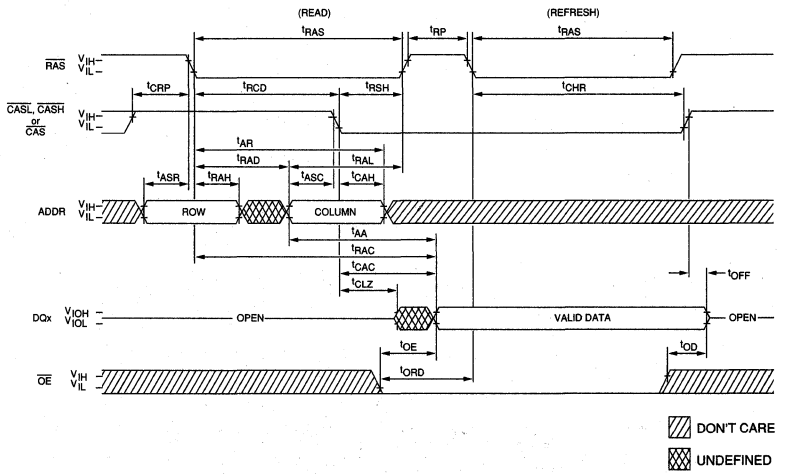
$\overline{\text{RAS}}$-ONLY REFRESH CYCLE

(ADDR = A0-A9, $\overline{\text{OE}}$; $\overline{\text{WEL}}$, $\overline{\text{WEH}}$ or $\overline{\text{WE}}$ = DON'T CARE)



HIDDEN REFRESH CYCLE [24]

($\overline{\text{WEL}}$, $\overline{\text{WEH}}$ or $\overline{\text{WE}}$ = HIGH; $\overline{\text{OE}}$ = LOW)



MICRON TECHNOLOGY, INC.

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DRAM MODULE PRODUCT SELECTION GUIDE

Memory Configuration	Part Number	Optional Access Cycle	Access Time (ns)	Power Dissipation		Package		Page
				Standby	Active	SIMM	SIP	
256K x 8	MT2D2568	LP, LV*	60, 70, 80	6mW	350mW	30	30	3-1
1 Meg x 8	MT2D18	LP, LV*	60, 70, 80	6mW	450mW	30	30	3-11
1 Meg x 8	MT8D18	LP	60, 70, 80	24mW	1,400mW	30	30	3-21
4 Meg x 8	MT2D48		60, 70, 80	10mW	550mW	30	30	3-31
4 Meg x 8	MT8D48	LP	60, 70, 80	24mW	1,800mW	30	30	3-41
16 Meg x 8	MT8D168		60, 70, 80	24mW	2,200mW	30	30	3-51
256K x 9	MT3D2569	LP	60, 70, 80	9mW	625mW	30	30	3-61
1 Meg x 9	MT3D19	LP	60, 70, 80	9mW	625mW	30	30	3-71
1 Meg x 9	MT9D19	LP	60, 70, 80	27mW	1,575mW	30	30	3-81
4 Meg x 9	MT3D49		60, 70, 80	12mW	775mW	30	30	3-91
4 Meg x 9	MT9D49	LP	60, 70, 80	27mW	2,025mW	30	30	3-101
16 Meg x 9	MT9D169		60, 70, 80	27mW	2,475mW	30	30	3-111
512K x 16	MT8D25632	LP, LV*	60, 70, 80	24mW	1,400mW	72	-	3-121
1 Meg x 16	MT16D51232	LP, LV*	60, 70, 80	48mW	2,800mW	72	-	3-133
2 Meg x 16	MT8D132	LP, LV*	60, 70, 80	24mW	1,800mW	72	-	3-145
4 Meg x 16	MT16D232	LP, LV*	60, 70, 80	48mW	1,824mW	72	-	3-157
8 Meg x 16	MT8D432		60, 70, 80	40mW	2,200mW	72	-	3-169
16 Meg x 16	MT16D832		60, 70, 80	80mW	2,240mW	72	-	3-179
512K x 18	MT10D25636		60, 70, 80	30mW	1,750mW	72	-	3-199
1 Meg x 18	MT6D118		60, 70, 80	18mW	1,250mW	72	-	3-209
1 Meg x 18	MT20D51236		60, 70, 80	60mW	1,780mW	72	-	3-229
2 Meg x 18	MT12D136	LP	60, 70, 80	36mW	2,500mW	72	-	3-249
4 Meg x 18	MT24D236	LP	60, 70, 80	72mW	2,536mW	72	-	3-271
8 Meg x 18	MT12D436		60, 70, 80	52mW	3,100mW	72	-	3-283
16 Meg x 18	MT24D836		60, 70, 80	104mW	3,152mW	72	-	3-293
256K x 32	MT8D25632	LP, LV*	60, 70, 80	24mW	1,400mW	72	-	3-121
512K x 32	MT16D51232	LP, LV*	60, 70, 80	48mW	1,424mW	72	-	3-133
1 Meg x 32	MT8D132	LP, LV*	60, 70, 80	24mW	1,800mW	72	-	3-145
2 Meg x 32	MT16D232	LP, LV*	60, 70, 80	48mW	1,824mW	72	-	3-157
4 Meg x 32	MT8D432		60, 70, 80	40mW	2,200mW	72	-	3-169
8 Meg x 32	MT16D832		60, 70, 80	80mW	2,240mW	72	-	3-179
256K x 36	MT9D25636		60, 70, 80	27mW	1,575mW	72	-	3-189
256K x 36	MT10D25636		60, 70, 80	30mW	1,750mW	72	-	3-199
512K x 36	MT18D51236		60, 70, 80	54mW	1,600mW	72	-	3-219
512K x 36	MT20D51236		60, 70, 80	60mW	1,780mW	72	-	3-229
1 Meg x 36	MT9D136		60, 70, 80	27mW	2,175mW	72	-	3-239
1 Meg x 36	MT12D136	LP	60, 70, 80	36mW	2,500mW	72	-	3-249
2 Meg x 36	MT18D236		60, 70, 80	54mW	2,052mW	72	-	3-261
2 Meg x 36	MT24D236	LP	60, 70, 80	72mW	2,536mW	72	-	3-271
4 Meg x 36	MT12D436		60, 70, 80	52mW	3,100mW	72	-	3-283
8 Meg x 36	MT24D836		60, 70, 80	104mW	3,152mW	72	-	3-293
256K x 40	MT10D25640	LP, LV*	60, 70, 80	30mW	1,750mW	72	-	3-303
512K x 40	MT20D51240	LP, LV*	60, 70, 80	60mW	1,780mW	72	-	3-315
1 Meg x 40	MT10D140	LP, LV*	60, 70, 80	30mW	2,250mW	72	-	3-327
2 Meg x 40	MT20D240	LP, LV*	60, 70, 80	60mW	2,280mW	72	-	3-339

LP = Low Power, Extended Refresh; LV = Low Voltage

NOTE: All modules include FAST PAGE MODE cycle.

*Contact factory regarding availability of low voltage versions.

DRAM MODULE

256K x 8 DRAM

FAST PAGE MODE (MT2D2568)
LOW POWER,
EXTENDED REFRESH (MT2D2568 L)

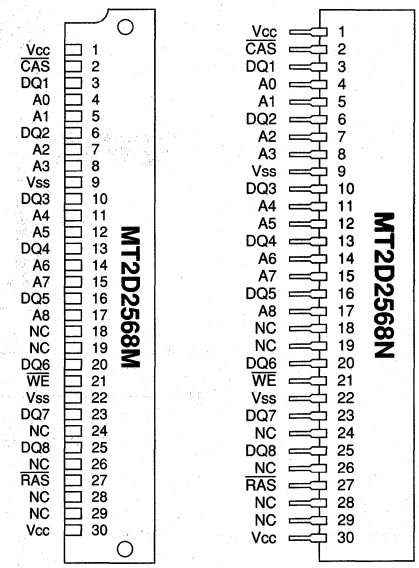
FEATURES

- Industry standard pinout in a 30-pin single-in-line memory module
- High-performance, CMOS silicon-gate process
- Single 5V ±10% power supply
- Low power, 6mW (.6mW L-version) standby; 350mW active, typical
- All device pins are fully TTL compatible
- FAST PAGE MODE access cycle
- Refresh modes: RAS-ONLY, CAS-BEFORE-RAS (CBR) and HIDDEN
- Low profile
- 512-cycle refresh distributed across 8ms or 512-cycle extended refresh distributed across 64ms
- Low CMOS standby current, 400µA maximum (L-version)

OPTIONS MARKING

- Timing
  - 60ns access - 6
  - 70ns access - 7
  - 80ns access - 8
- Packages
  - Leadless 30-pin SIMM M
  - Leaded 30-pin SIP N
- Power/Refresh
  - Normal Power/8ms Blank
  - Low Power/64ms L
- Part Number Example: MT2D2568ML-6

PIN ASSIGNMENT (Top View)



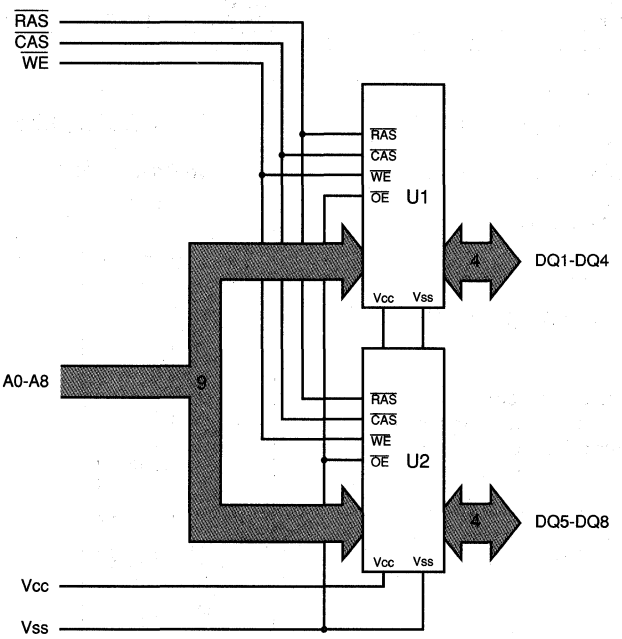
GENERAL DESCRIPTION

The MT2D2568 is a randomly accessed solid-state memory containing 262,144 words organized in a x8 configuration. During READ or WRITE cycles, each word is uniquely addressed through the 18 address bits, which are entered 9 bits (A0-A8) at a time. RAS is used to latch the first 9 bits and CAS the latter 9 bits. READ or WRITE cycles are selected with the WE input. A logic HIGH on WE dictates READ mode while a logic LOW on WE dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of WE or CAS, whichever occurs last. EARLY-WRITE occurs when WE goes LOW prior to CAS going LOW, and the output pins remain open (High-Z) until the next CAS cycle.

FAST PAGE MODE operations allow faster data operations (READ or WRITE) within a row address (A0-A8) defined page boundary. The FAST PAGE MODE cycle is always initiated with a row address strobed-in by RAS followed by a column address strobed-in by CAS. CAS may be toggled-in by holding RAS LOW and strobing-in different column addresses, thus executing faster memory cycles.

Returning RAS and CAS HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the RAS high time. Memory cell data is retained in its correct state by maintaining power and executing any RAS cycle (READ, WRITE, RAS-ONLY, CAS-BEFORE-RAS or HIDDEN REFRESH) so that all 512 combinations of RAS addresses (A0-A8) are executed at least every 8ms, (64ms on L-version) regardless of sequence.

FUNCTIONAL BLOCK DIAGRAM



U1, U2 = MT4C4256DJ
U1, U2 = MT4C4256DJ L (L-version)

TRUTH TABLE

FUNCTION		RAS	CAS	WE	ADDRESSES		DATA IN/OUT
					^tR	^tC	DQ1-DQ8
Standby		H	H→X	X	X	X	High-Z
READ		L	L	H	ROW	COL	Data Out
EARLY-WRITE		L	L	L	ROW	COL	Data In
FAST-PAGE-MODE	1st Cycle	L	H→L	H	ROW	COL	Data Out
READ	2nd Cycle	L	H→L	H	n/a	COL	Data Out
FAST-PAGE-MODE	1st Cycle	L	H→L	L	ROW	COL	Data In
WRITE	2nd Cycle	L	H→L	L	n/a	COL	Data In
RAS-ONLY REFRESH		L	H	X	ROW	n/a	High-Z
HIDDEN	READ	L→H→L	L	H	ROW	COL	Data Out
REFRESH	WRITE	L→H→L	L	L	ROW	COL	Data In
CAS-BEFORE-RAS REFRESH		H→L	L	X	X	X	High-Z
BATTERY BACKUP REFRESH (L-version)		H→L	L	X	X	X	High-Z

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} ..... -1V to +7V
Operating Temperature, T_A (Ambient) ..... 0°C to +70°C
Storage Temperature ..... -55°C to +125°C
Power Dissipation 2W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 2, 3, 6, 22) (0°C ≤ T_A ≤ 70°C; V_{CC} = 5V ±10%)

PARAMETER/CONDITION		SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage		V_{CC}	4.5	5.5	V	1
Input High (Logic 1) Voltage, All Inputs		V_{IH}	2.4	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, All Inputs		V_{IL}	-1	0.8	V	1
INPUT LEAKAGE Any Input 0V ≤ V_{IN} ≤ V_{CC} (All other pins not under test = 0V)	A0-A8, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	I_I	-4	4	µA	
OUTPUT LEAKAGE (Q is disabled, 0V ≤ V_{OUT} ≤ V_{CC})	DQ1-DQ8	I_{OZ}	-10	10	µA	
OUTPUT LEVELS Output High (Logic 1) Voltage (I_{OUT} = -5mA)		V_{OH}	2.4		V	
Output Low (Logic 0) Voltage (I_{OUT} = 5mA)		V_{OL}		0.4	V	

PARAMETER/CONDITION	SYMBOL	MAX -6	MAX -7	MAX -8	UNITS	NOTES
STANDBY CURRENT: (TTL) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC1}	4	4	4	mA	
STANDBY CURRENT: (CMOS)	I_{CC2}	2	2	2	mA	23
($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} -0.2V)		.4	.4	.4	mA	23, 25
OPERATING CURRENT: Random READ/WRITE Average power supply current	I_{CC3}	180	160	140	mA	2, 22
($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC (MIN))		170	150	130	mA	2,22,25
OPERATING CURRENT: FAST PAGE MODE Average power supply current	I_{CC4}	140	120	100	mA	2, 22
($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: ^tPC = ^tPC (MIN))		130	110	90	mA	2,22,25
REFRESH CURRENT: $\overline{RAS}$-ONLY Average power supply current	I_{CC5}	180	160	140	mA	2
($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}: ^tRC = ^tRC (MIN))		170	150	130	mA	2, 25
REFRESH CURRENT: $\overline{CAS}$-BEFORE-$\overline{RAS}$ Average power supply current	I_{CC6}	180	160	140	mA	2, 19
($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC (MIN))		170	150	130	mA	2,19,25
REFRESH CURRENT: BATTERY BACKUP (BBU) Average power supply current during BATTERY BACKUP refresh: $\overline{CAS}$ = 0.2V or $\overline{CAS}$-BEFORE-$\overline{RAS}$ cycling; $\overline{RAS}$ = ^tRAS (MIN) to 1µs; $\overline{WE}$, A0-A9 and D_{IN} = Vcc -0.2V or 0.2V (D_{IN} may be left OPEN), ^tRC = 125µs (512 rows at 125µs = 64ms)	I_{CC7}	.4	.4	.4	mA	25

DRAM MODULE

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A8	C_{I1}		13	pF	17
Input Capacitance: $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	C_{I2}		17	pF	17
Input/Output Capacitance: DQ1-DQ8	C_{IO}		10	pF	17

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 3, 4, 5, 6, 7, 10, 11, 16, 21) (0°C ≤ T_A ≤ +70°C; Vcc = 5V ±10%)

AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	^tRC	110		130		150		ns	
READ-WRITE cycle time	^tRWC	n/a		n/a		n/a		n/a	21
FAST-PAGE-MODE READ or WRITE cycle time	^tPC	40		40		40		ns	
FAST-PAGE-MODE READ-WRITE cycle time	^tPRWC	n/a		n/a		n/a		n/a	21
Access time from $\overline{RAS}$	^tRAC		60		70		80	ns	8
Access time from $\overline{CAS}$	^tCAC		20		20		20	ns	9
Output Enable	^tOE		20		20		20	ns	
Access time from column address	^tAA		30		35		40	ns	
Access time from $\overline{CAS}$ precharge	^tCPA		35		40		45	ns	
$\overline{RAS}$ pulse width	^tRAS	60	100,000	70	100,000	80	100,000	ns	
$\overline{RAS}$ pulse width (FAST PAGE MODE)	^tRASP	60	100,000	70	100,000	80	100,000	ns	
$\overline{RAS}$ hold time	^tRSH	20		20		20		ns	
$\overline{RAS}$ precharge time	^tRP	40		50		60		ns	
$\overline{CAS}$ pulse width	^tCAS	20	100,000	20	100,000	20	100,000	ns	
$\overline{CAS}$ hold time	^tCSH	60		70		80		ns	
$\overline{CAS}$ precharge time	^tCPN	10		10		10		ns	18
$\overline{CAS}$ precharge time (FAST PAGE MODE)	^tCP	10		10		10		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	^tRCD	20	40	20	50	20	60	ns	13
$\overline{CAS}$ to $\overline{RAS}$ precharge time	^tCRP	5		5		5		ns	
Row address setup time	^tASR	0		0		0		ns	
Row address hold time	^tRAH	10		10		10		ns	
$\overline{RAS}$ to column address delay time	^tRAD	15	30	15	35	15	40	ns	24
Column address setup time	^tASC	0		0		0		ns	
Column address hold time	^tCAH	15		15		15		ns	
Column address hold time (referenced to $\overline{RAS}$)	^tAR	45		55		60		ns	
Column address to $\overline{RAS}$ lead time	^tRAL	30		35		40		ns	
Read command setup time	^tRCS	0		0		0		ns	
Read command hold time (referenced to $\overline{CAS}$)	^tRCH	0		0		0		ns	14
Read command hold time (referenced to $\overline{RAS}$)	^tRRH	0		0		0		ns	14
$\overline{CAS}$ to output in Low-Z	^tCLZ	0		0		0		ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

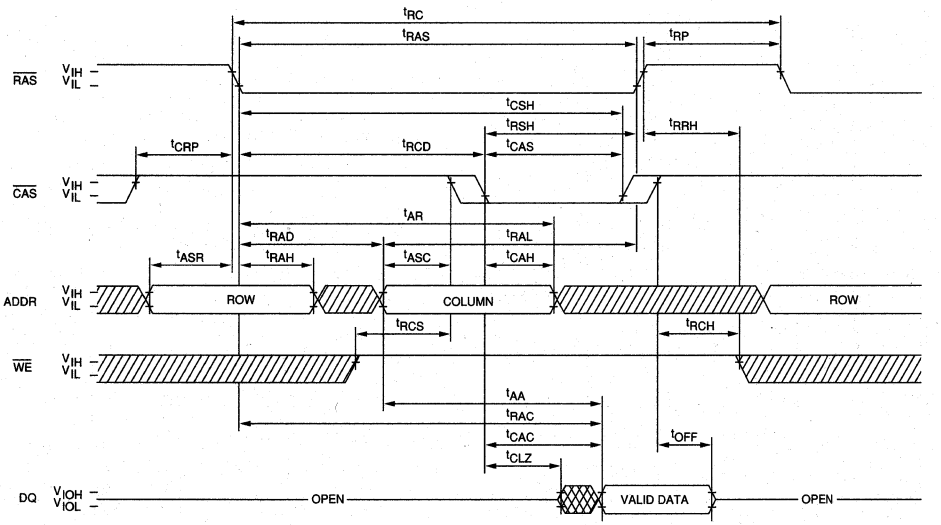
(Notes: 3, 4, 5, 6, 7, 10, 11, 16, 21) (0°C ≤ T_A ≤ +70°C; Vcc = 5V ±10%)

AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Output buffer turn-off delay	tOFF	0	20	0	20	0	20	ns	12
$\overline{WE}$ command setup time	tWCS	0		0		0		ns	
Write command hold time	tWCH	10		15		15		ns	
Write command hold time (referenced to $\overline{RAS}$)	tWCR	45		55		60		ns	
Write command pulse width	tWP	10		15		15		ns	
Write command to $\overline{RAS}$ lead time	tRWL	20		20		20		ns	
Write command to $\overline{CAS}$ lead time	tCWL	20		20		20		ns	
Data-in setup time	tDS	0		0		0		ns	15
Data-in hold time	tDH	15		15		15		ns	15
Data-in hold time (referenced to $\overline{RAS}$)	tDHR	45		55		60		ns	
Transition time (rise or fall)	tT	3	50	3	50	3	50	ns	5, 16
Refresh period (512 cycles)	tREF		8/64		8/64		8/64	ms	3/25
$\overline{RAS}$ to $\overline{CAS}$ precharge time	tRPC	0		0		0		ns	
$\overline{CAS}$ setup time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH)	tCSR	10		10		10		ns	19
$\overline{CAS}$ hold time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH)	tCHR	10		15		15		ns	19

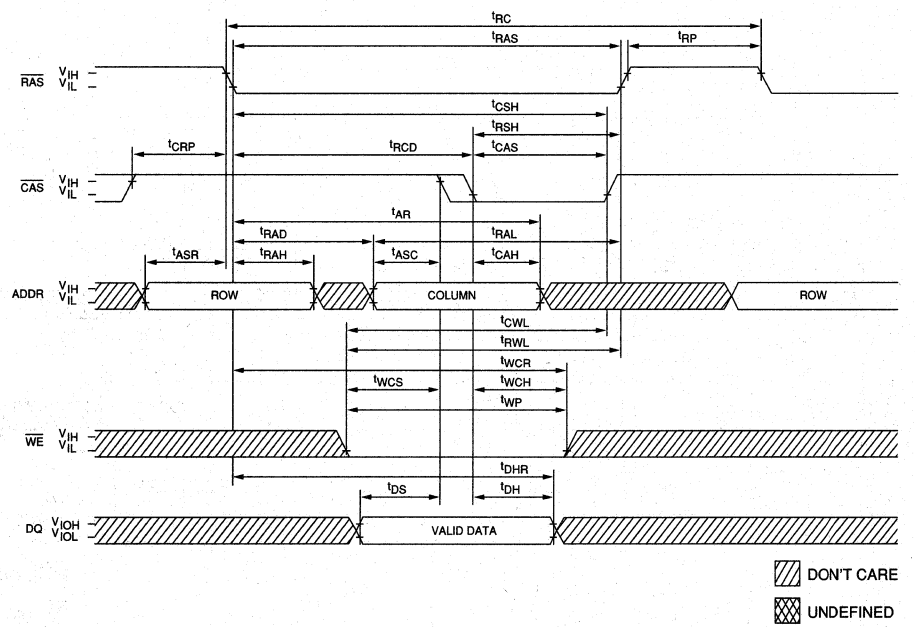
NOTES

1. All voltages referenced to V_{SS}.
2. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
3. An initial pause of 100µs is required after power-up followed by any eight $\overline{RAS}$ cycles before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-up should be repeated any time the ^{t}REF refresh requirement is exceeded.
4. AC characteristics assume ^{t}T = 5ns.
5. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \le T_A \le 70°C$) is assured.
7. Measured with a load equivalent to two TTL gates and 100pF.
8. Assumes that $^{t}RCD < ^{t}RCD$ (MAX). If ^{t}RCD is greater than the maximum recommended value shown in this table, ^{t}RAC will increase by the amount that ^{t}RCD exceeds the value shown.
9. Assumes that $^{t}RCD \ge ^{t}RCD$ (MAX).
10. If $\overline{CAS}$ = V_{IH}, data output is High-Z.
11. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
12. ^{t}OFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
13. Operation within the ^{t}RCD (MAX) limit ensures that ^{t}RAC (MAX) can be met. ^{t}RCD (MAX) is specified as a reference point only; if ^{t}RCD is greater than the specified ^{t}RCD (MAX) limit, then access time is controlled exclusively by ^{t}CAC.
14. Either ^{t}RCH or ^{t}RRH must be satisfied for a READ cycle.
15. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY-WRITE cycles.
16. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
17. This parameter is sampled. Capacitance is measured using MIL-STD-883C, Method 3012.1 (1 MHz AC, Vcc = 5V, DC bias = 2.4V @ 15mV RMS).
18. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, data-out (Q) will be maintained from the previous cycle. To initiate a new cycle and clear the Q buffer, $\overline{CAS}$ must be pulsed HIGH for ^{t}CP.
19. On-chip refresh and address counters are enabled.
20. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW.
21. LATE-WRITE, READ-WRITE or READ-MODIFY-WRITE cycles are not available due to $\overline{OE}$ being grounded on U1 and U2.
22. I_{CC} is dependent on cycle rates.
23. All other inputs at Vcc -0.2V.
24. Operation within the ^{t}RAD (MAX) limit ensures that ^{t}RCD (MAX) can be met. ^{t}RAD (MAX) is specified as a reference point only; if ^{t}RAD is greater than the specified ^{t}RAD (MAX) limit, then access time is controlled exclusively by ^{t}AA.
25. Applies to L-version only.

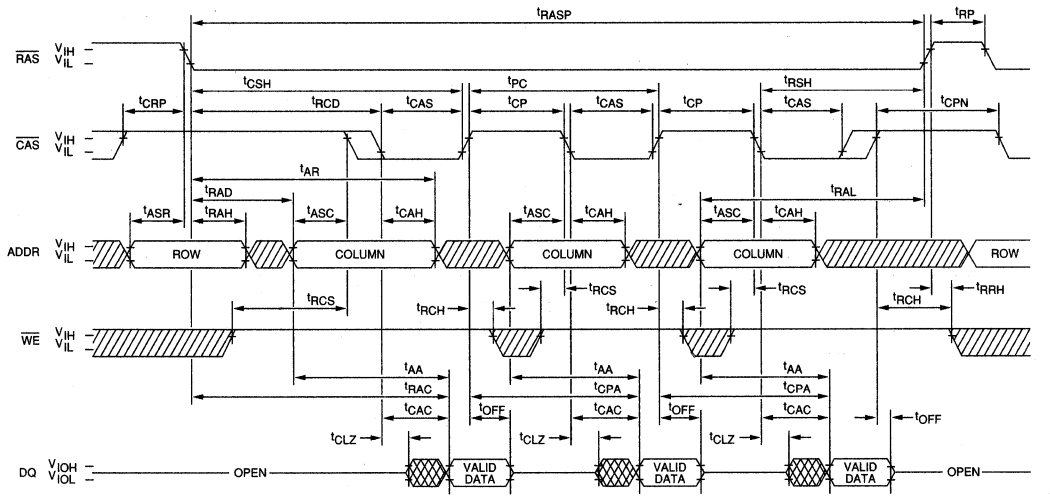
READ CYCLE



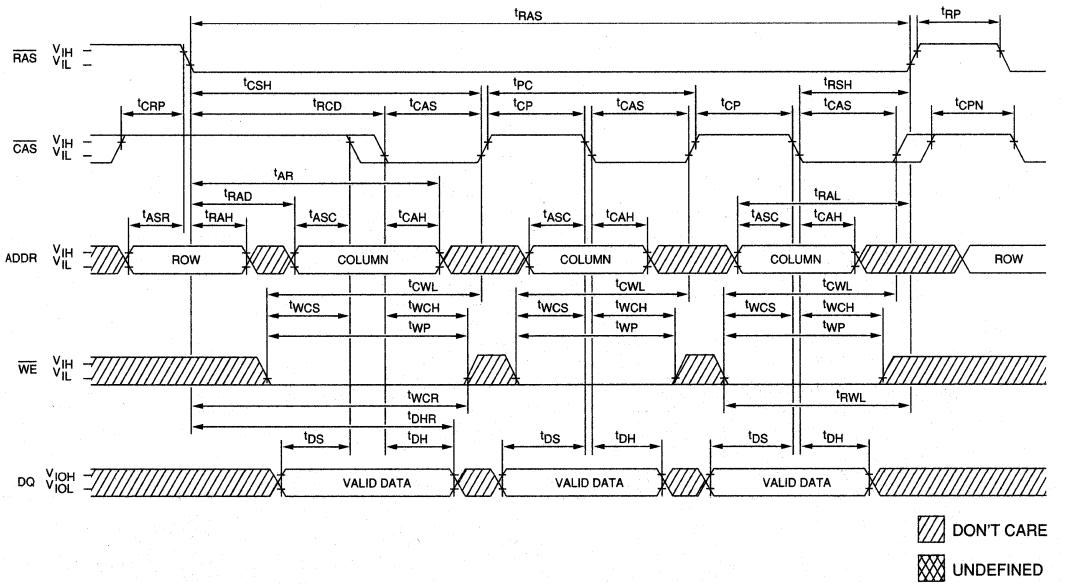
EARLY-WRITE CYCLE



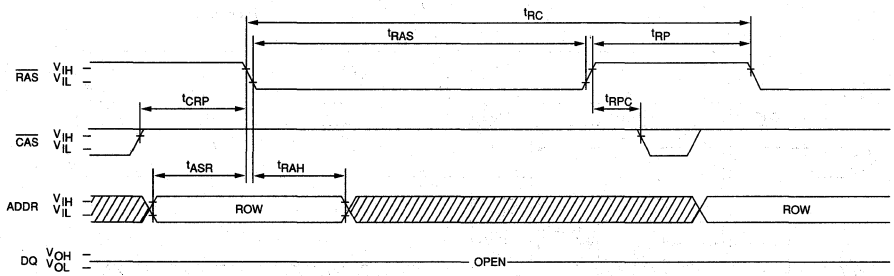
FAST-PAGE-MODE READ CYCLE



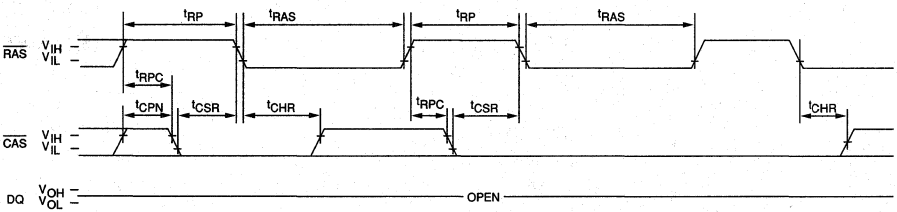
FAST-PAGE-MODE EARLY-WRITE CYCLE



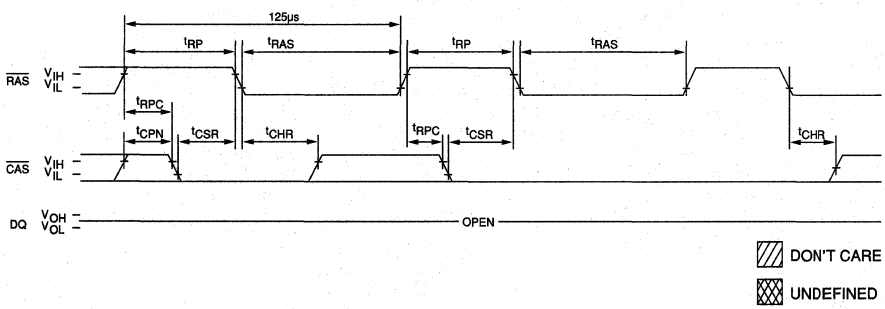
$\overline{RAS}$-ONLY REFRESH CYCLE
(ADDR = A0-A8; $\overline{WE}$ = DON'T CARE)



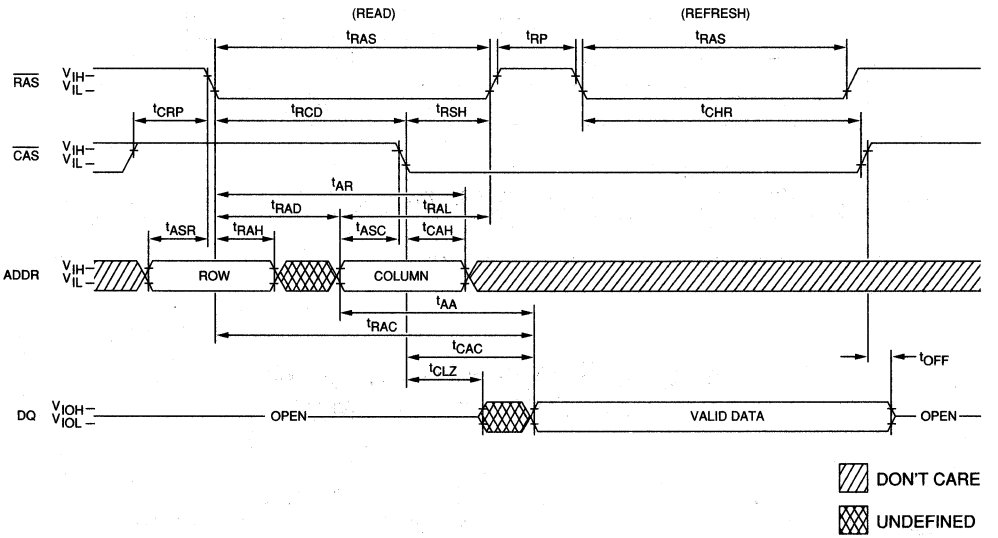
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE
(A0-A8 and $\overline{WE}$ = DON'T CARE)



BATTERY BACKUP REFRESH CYCLE [25]
(A0-A8 and $\overline{WE}$ = DON'T CARE)



HIDDEN REFRESH CYCLE [20]
($\overline{WE}$ = HIGH)



DRAM MODULE

1 MEG x 8 DRAM

FAST PAGE MODE (MT2D18)
LOW POWER,
EXTENDED REFRESH (MT2D18 L)

FEATURES

- Industry standard pinout in a 30-pin, single-in-line memory module
- High-performance, CMOS silicon-gate process
- Single 5V ±10% power supply
- Low power, 6mW (2mW L-version) standby; 450mW active, typical
- All device pins are fully TTL compatible
- FAST PAGE MODE access cycle
- Refresh modes: RAS-ONLY, CAS-BEFORE-RAS (CBR) and HIDDEN
- Low profile
- 1,024-cycle refresh distributed across 16ms or 1,024-cycle extended refresh distributed across 128ms
- Low CMOS standby current, 400µA maximum (L-version)

OPTIONS — MARKING

- Timing
  - 60ns access — -6
  - 70ns access — -7
  - 80ns access — -8
- Packages
  - Leadless 30-pin SIMM — M
  - Leaded 30-pin SIP — N
- Power/Refresh
  - Normal power/16ms — Blank
  - Low power/128ms — L
- Part Number Example: MT2D18ML-6

PIN ASSIGNMENT (Top View)

30-Pin SIMM (T-1) — MT2D18M

Vcc	1	16	DQ5
CAS	2	17	A8
DQ1	3	18	A9
A0	4	19	NC
A1	5	20	DQ6
DQ2	6	21	WE
A2	7	22	Vss
A3	8	23	DQ7
Vss	9	24	NC
DQ3	10	25	DQ8
A4	11	26	NC
A5	12	27	RAS
DQ4	13	28	NC
A6	14	29	NC
A7	15	30	Vcc

30-Pin SIP (S-1) — MT2D18N

Vcc	1	16	DQ5
CAS	2	17	A8
DQ1	3	18	A9
A0	4	19	NC
A1	5	20	DQ6
DQ2	6	21	WE
A2	7	22	Vss
A3	8	23	DQ7
Vss	9	24	NC
DQ3	10	25	DQ8
A4	11	26	NC
A5	12	27	RAS
DQ4	13	28	NC
A6	14	29	NC
A7	15	30	Vcc

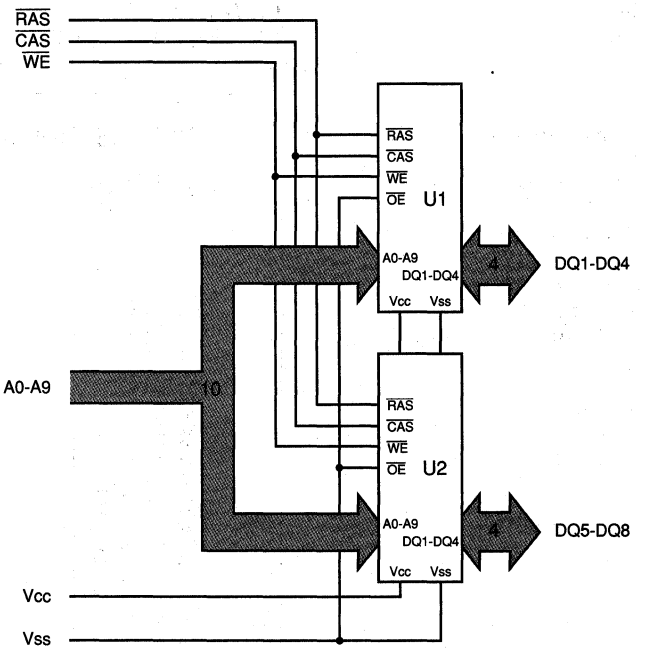
GENERAL DESCRIPTION

The MT2D18 is a randomly accessed solid-state memory containing 1,048,576 words organized in a x8 configuration. During READ or WRITE cycles, each word is uniquely addressed through 20 address bits, which are entered 10 bits (A0-A9) at a time. RAS is used to latch the first 10 bits and CAS the latter 10 bits. READ or WRITE cycles are selected with the WE input. A logic HIGH on WE dictates READ mode while a logic LOW on WE dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of WE or CAS, whichever occurs last. Early WRITE occurs when WE goes LOW prior to CAS going LOW, and the output pins remain open (High-Z) until the next CAS cycle.

FAST PAGE MODE operations allow faster data operations (READ or WRITE) within a row address (A0-A9) defined page boundary. The FAST PAGE MODE cycle is always initiated with a row address strobed-in by RAS followed by a column address strobed-in by CAS. CAS may be toggled-in by holding RAS LOW and strobing-in different column addresses, thus executing faster memory cycles.

Returning RAS and CAS HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the RAS high time. Memory cell data is retained in its correct state by maintaining power and executing any RAS cycle (READ, WRITE, RAS-ONLY, CAS-BEFORE-RAS or HIDDEN REFRESH) so that all 1,024 combinations of RAS addresses (A0-A9) are executed at least every 16ms (128ms on L-version), regardless of sequence.

FUNCTIONAL BLOCK DIAGRAM



U1, U2 = MT4C4001JDJ
U1, U2 = MT4C4001JDJ L (L-version)

TRUTH TABLE

FUNCTION		RAS	CAS	WE	ADDRESSES		DATA IN/OUT
					^tR	^tC	DQ1-DQ8
Standby		H	H→X	X	X	X	High-Z
READ		L	L	H	ROW	COL	Data Out
EARLY-WRITE		L	L	L	ROW	COL	Data In
FAST-PAGE-MODE	1st Cycle	L	H→L	H	ROW	COL	Data Out
READ	2nd Cycle	L	H→L	H	n/a	COL	Data Out
FAST-PAGE-MODE	1st Cycle	L	H→L	L	ROW	COL	Data In
WRITE	2nd Cycle	L	H→L	L	n/a	COL	Data In
RAS-ONLY REFRESH		L	H	X	ROW	n/a	High-Z
HIDDEN	READ	L→H→L	L	H	ROW	COL	Data Out
REFRESH	WRITE	L→H→L	L	L	ROW	COL	Data In
CAS-BEFORE-RAS REFRESH		H→L	L	H	X	X	High-Z
BATTERY BACKUP REFRESH (L-version)		H→L	L	X	X	X	High-Z

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} ..... -1V to +7V
Operating Temperature, T_A (Ambient) ..... 0°C to +70°C
Storage Temperature ..... -55°C to +125°C
Power Dissipation 2W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 2, 3, 6, 26) (0°C ≤ T_A ≤ 70°C; V_{CC} = 5V ±10%)

PARAMETER/CONDITION		SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage		V_{CC}	4.5	5.5	V	1
Input High (Logic 1) Voltage, All Inputs		V_{IH}	2.4	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, All Inputs		V_{IL}	-1.0	0.8	V	1
INPUT LEAKAGE Any Input 0V ≤ V_{IN} ≤ V_{CC} (All other pins not under test = 0V)	A0-A9, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	I_I	-4	4	µA	
OUTPUT LEAKAGE (Q is disabled, 0V ≤ V_{OUT} ≤ V_{CC})	DQ1-DQ8	I_{OZ}	-10	10	µA	
OUTPUT LEVELS Output High (Logic 1) Voltage (I_{OUT} = -5mA)		V_{OH}	2.4		V	
Output Low (Logic 0) Voltage (I_{OUT} = 5mA)		V_{OL}		0.4	V	

		MAX				
PARAMETER/CONDITION	SYMBOL	-6	-7	-8	UNITS	NOTES
STANDBY CURRENT: (TTL) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC1}	4	4	4	mA	
STANDBY CURRENT: (CMOS)	I_{CC2}	2	2	2	mA	25
($\overline{RAS}$ = $\overline{CAS}$ = Other Inputs = V_{CC} -0.2V)		.4	.4	.4	mA	25
OPERATING CURRENT: Random READ/WRITE Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC (MIN))	I_{CC3}	220	200	180	mA	2, 26
OPERATING CURRENT: FAST PAGE MODE Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: ^tPC = ^tPC (MIN))	I_{CC4}	160	140	120	mA	2, 26
REFRESH CURRENT: $\overline{RAS}$-ONLY Average power supply current ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}: ^tRC = ^tRC (MIN))	I_{CC5}	220	200	180	mA	2
REFRESH CURRENT: $\overline{CAS}$-BEFORE-$\overline{RAS}$ Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC (MIN))	I_{CC6}	220	200	180	mA	2, 19
REFRESH CURRENT: BATTERY BACKUP (BBU) Average power supply current during BATTERY BACKUP refresh: $\overline{CAS}$ = 0.2V or $\overline{CAS}$-BEFORE-$\overline{RAS}$ cycling; $\overline{RAS}$ = ^tRAS (MIN) to 300ns; $\overline{WE}$ = Vcc -0.2V; A0-A9 and D_{IN} = V_{CC} - 0.2V or 0.2V (D_{IN} may be left open), ^tRC = 125µs (1,024 rows at 125µs = 128ms)	I_{CC7}	.6	.6	.6	µA	27, 28

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A9	C_{I1}		13	pF	17
Input Capacitance: $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	C_{I2}		17	pF	17
Input/Output Capacitance: DQ1-DQ8	C_{IO}		10	pF	17

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 3, 4, 5, 6, 7, 10, 11, 16, 21) (0°C ≤ T_A ≤ +70°C; Vcc = 5V ±10%)

AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	^tRC	110		130		150		ns	
READ-WRITE cycle time	^tRWC	n/a		n/a		n/a		n/a	21
FAST-PAGE-MODE READ or WRITE cycle time	^tPC	40		40		45		ns	
FAST-PAGE-MODE READ-WRITE cycle time	^tPRWC	n/a		n/a		n/a		n/a	21
Access time from $\overline{RAS}$	^tRAC		60		70		80	ns	8
Access time from $\overline{CAS}$	^tCAC		15		20		20	ns	9
Access time from column address	^tAA		30		35		40	ns	
Access time from $\overline{CAS}$ precharge	^tCPA		35		40		45	ns	
$\overline{RAS}$ pulse width	^tRAS	60	100,000	70	100,000	80	100,000	ns	
$\overline{RAS}$ pulse width (FAST PAGE MODE)	^tRASP	60	100,000	70	100,000	80	100,000	ns	
$\overline{RAS}$ hold time	^tRSH	15		20		20		ns	
$\overline{RAS}$ precharge time	^tRP	40		50		60		ns	
$\overline{CAS}$ pulse width	^tCAS	15	100,000	20	100,000	20	100,000	ns	
$\overline{CAS}$ hold time	^tCSH	60		70		80		ns	
$\overline{CAS}$ precharge time	^tCPN	10		10		10		ns	18
$\overline{CAS}$ precharge time (FAST PAGE MODE)	^tCP	10		10		10		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	^tRCD	20	45	20	50	20	60	ns	13
$\overline{CAS}$ to $\overline{RAS}$ precharge time	^tCRP	10		10		10		ns	
Row address setup time	^tASR	0		0		0		ns	
Row address hold time	^tRAH	10		10		10		ns	
$\overline{RAS}$ to column address delay time	^tRAD	15	30	15	35	15	40	ns	22
Column address setup time	^tASC	0		0		0		ns	
Column address hold time	^tCAH	10		15		15		ns	
Column address hold time (referenced to $\overline{RAS}$)	^tAR	50		55		60		ns	
Column address to $\overline{RAS}$ lead time	^tRAL	30		35		40		ns	
Read command setup time	^tRCS	0		0		0		ns	
Read command hold time (referenced to $\overline{CAS}$)	^tRCH	0		0		0		ns	24
Read command hold time (referenced to $\overline{RAS}$)	^tRRH	0		0		0		ns	24
$\overline{CAS}$ to output in Low-Z	^tCLZ	0		0		0		ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

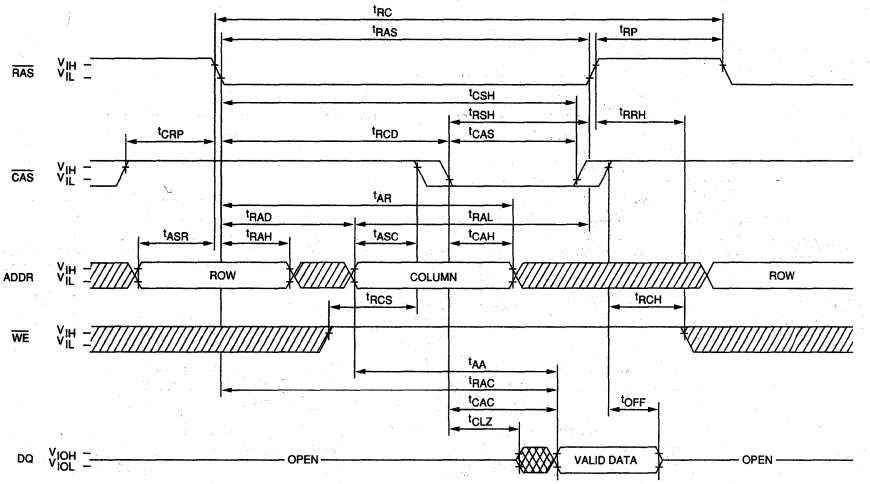
(Notes: 3, 4, 5, 6, 7, 10, 11, 16, 21) ($0°C \le T_A \le +70°C$; $V_{CC} = 5V \pm 10\%$)

AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Output buffer turn-off delay	tOFF	0	15	0	20	0	20	ns	12
$\overline{WE}$ command setup time	tWCS	0		0		0		ns	
Write command hold time	tWCH	10		15		15		ns	
Write command hold time (referenced to $\overline{RAS}$)	tWCR	45		55		60		ns	
Write command pulse width	tWP	10		15		15		ns	
Write command to $\overline{RAS}$ lead time	tRWL	15		20		20		ns	
Write command to $\overline{CAS}$ lead time	tCWL	15		20		20		ns	
Data-in setup time	tDS	0		0		0		ns	15
Data-in hold time	tDH	10		15		15		ns	15
Data-in hold time (referenced to $\overline{RAS}$)	tDHR	45		55		60		ns	
Transition time (rise or fall)	tT	3	50	3	50	3	50	ns	5, 16
Refresh period (1,024 cycles)	tREF		16/128		16/128		16/128	ms	3/28
$\overline{RAS}$ to $\overline{CAS}$ precharge time	tRPC	0		0		0		ns	
$\overline{CAS}$ setup time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH)	tCSR	10		10		10		ns	19
$\overline{CAS}$ hold time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH)	tCHR	15		15		15		ns	19
$\overline{WE}$ hold time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	tWRH	10		10		10		ns	23
$\overline{WE}$ setup time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	tWRP	10		10		10		ns	23
$\overline{WE}$ hold time (WCBR test cycle)	tWTH	10		10		10		ns	23
$\overline{WE}$ setup time (WCBR test cycle)	tWTS	10		10		10		ns	23

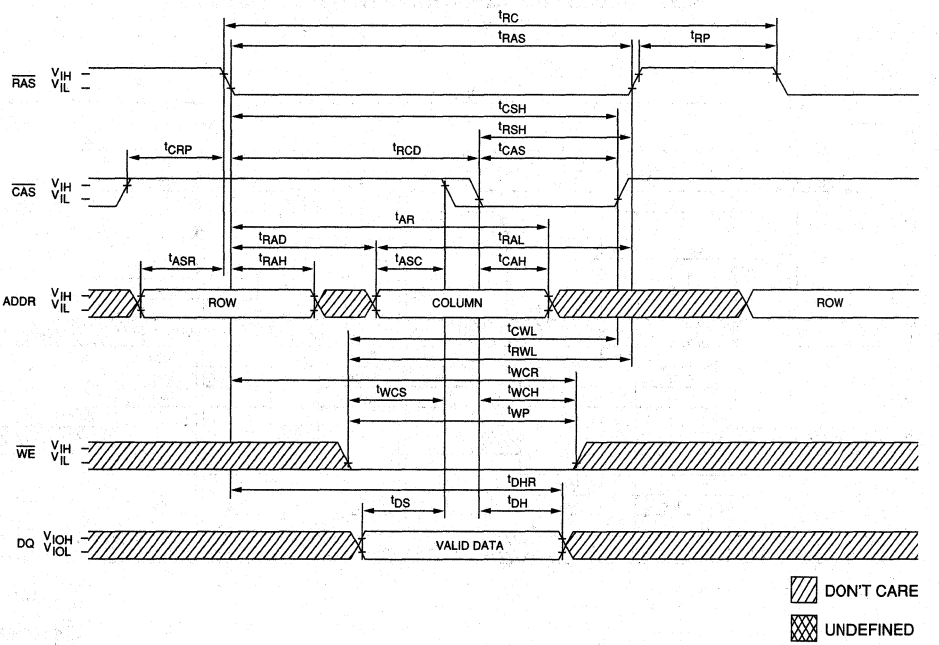
NOTES

1. All voltages referenced to V_{SS}.
2. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
3. An initial pause of 100µs is required after power-up followed by any eight $\overline{RAS}$ REFRESH cycles ($\overline{RAS}$-ONLY or CBR with $\overline{WE}$ HIGH) before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-up should be repeated any time the ^{t}REF refresh requirement is exceeded.
4. AC characteristics assume ^{t}T = 5ns.
5. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \leq T_A \leq 70°C$) is assured.
7. Measured with a load equivalent to 2 TTL gates and 100pF.
8. Assumes that $^{t}RCD < {}^{t}RCD$ (MAX). If ^{t}RCD is greater than the maximum recommended value shown in this table, ^{t}RAC will increase by the amount that ^{t}RCD exceeds the value shown.
9. Assumes that $^{t}RCD \geq {}^{t}RCD$ (MAX).
10. If $\overline{CAS}$ = V_{IH}, data output is High-Z.
11. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
12. ^{t}OFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
13. Operation within the ^{t}RCD (MAX) limit ensures that ^{t}RAC (MAX) can be met. ^{t}RCD (MAX) is specified as a reference point only; if ^{t}RCD is greater than the specified ^{t}RCD (MAX) limit, then access time is controlled exclusively by ^{t}CAC.
14. ^{t}RCH is referenced to the first rising edge of $\overline{RAS}$ or $\overline{CAS}$.
15. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY-WRITE cycles.
16. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
17. This parameter is sampled. Capacitance is measured using MIL-STD-883C, Method 3012.1 (1 MHz AC, Vcc = 5V, DC bias = 2.4V @ 15mV RMS).
18. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, data-out (Q) will be maintained from the previous cycle. To initiate a new cycle and clear the Q buffer, $\overline{CAS}$ must be pulsed HIGH for ^{t}CP.
19. On-chip refresh and address counters are enabled.
20. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW.
21. LATE-WRITE, READ-WRITE or READ-MODIFY-WRITE cycles are not available due to $\overline{OE}$ being grounded on U1 and U2.
22. Operation within the ^{t}RAD (MAX) limit ensures that ^{t}RCD (MAX) can be met. ^{t}RAD (MAX) is specified as a reference point only; if ^{t}RAD is greater than the specified ^{t}RAD (MAX) limit, then access time is controlled exclusively by ^{t}AA.
23. ^{t}WTS and ^{t}WTH are setup and hold specifications for the $\overline{WE}$ pin being held LOW to enable the JEDEC test mode (with CBR timing constraints). These two parameters are the inverts of ^{t}WRP and ^{t}WRH in the CBR refresh cycle.
24. Either ^{t}RCH or ^{t}RRH must be satisfied for a READ cycle.
25. All other inputs at V_{CC} -0.2V.
26. I_{CC} is dependent on cycle rates.
27. BBU current is reduced as ^{t}RAS is reduced from its maximum specification during the BBU cycle.
28. Applies to L-version only.

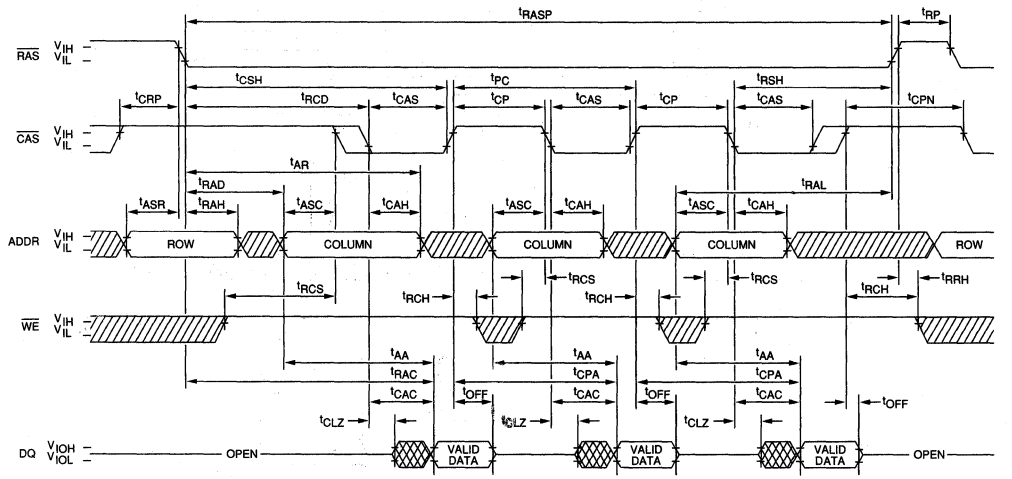
READ CYCLE



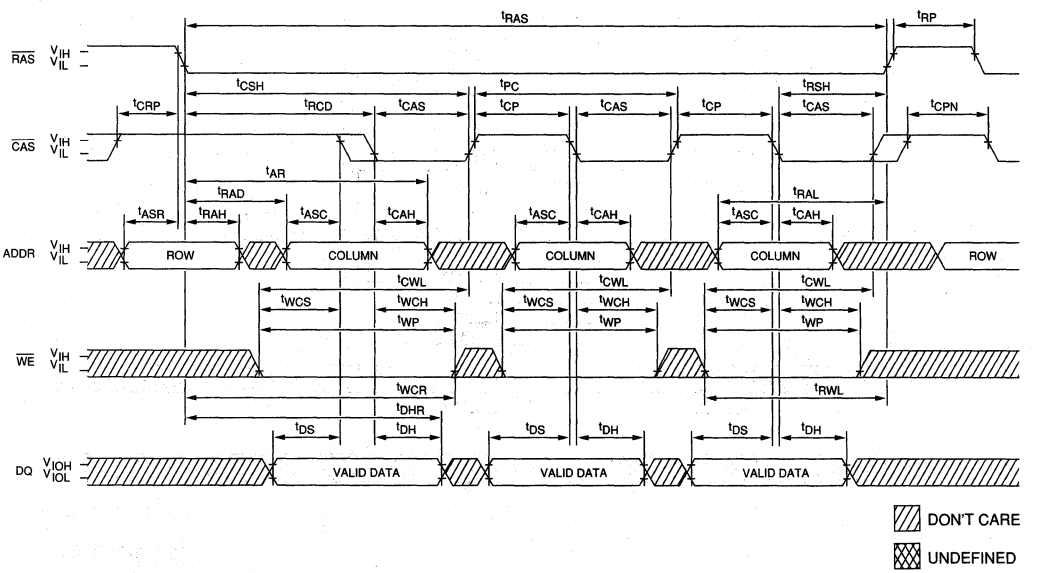
EARLY-WRITE CYCLE



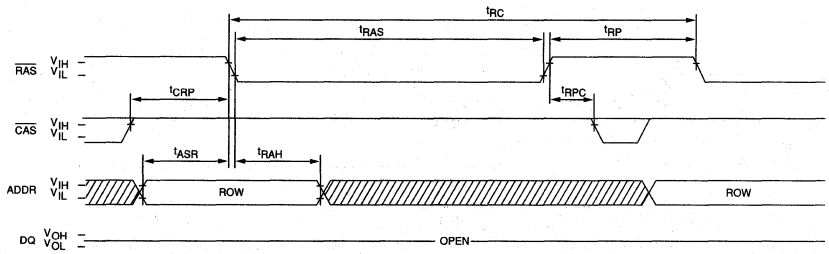
FAST-PAGE-MODE READ CYCLE



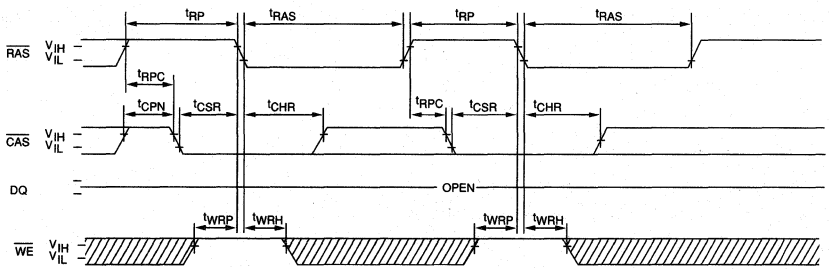
FAST-PAGE-MODE EARLY-WRITE CYCLE



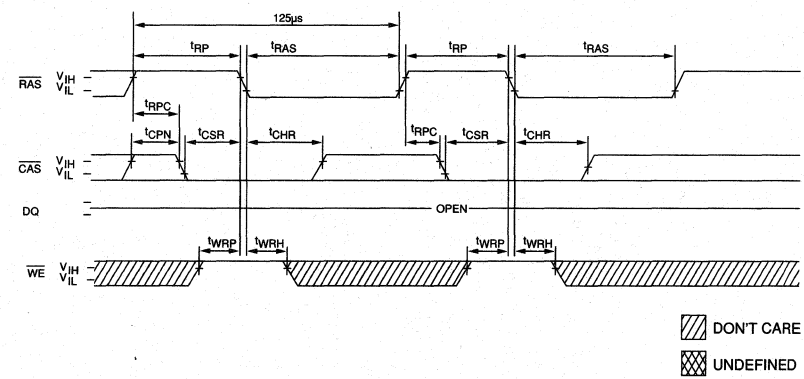
$\overline{\text{RAS}}$-ONLY REFRESH CYCLE
(ADDR = A0-A9; $\overline{\text{WE}}$ = DON'T CARE)



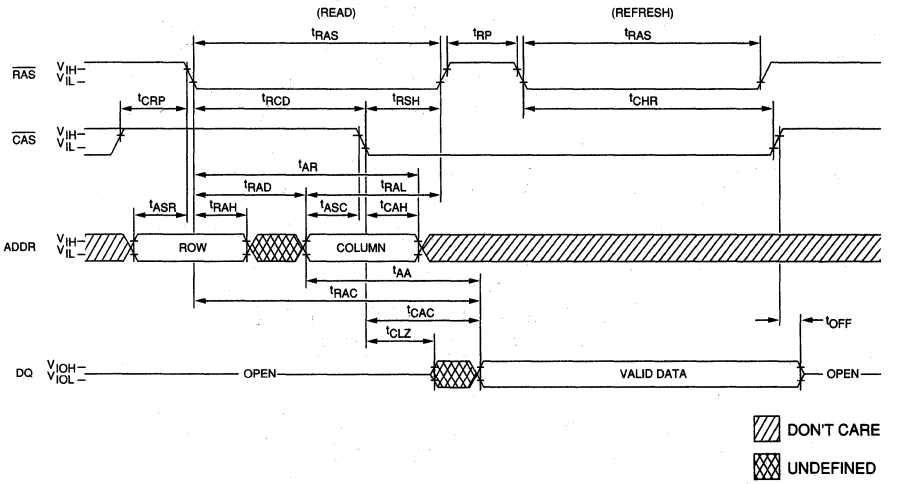
$\overline{\text{CAS}}$-BEFORE-$\overline{\text{RAS}}$ REFRESH CYCLE
(A0-A9 = DON'T CARE)



BATTERY BACKUP REFRESH CYCLE [28]
(A0-A9 = DON'T CARE)



HIDDEN REFRESH CYCLE [20]
($\overline{WE}$ = HIGH)



DRAM MODULE

1 MEG x 8 DRAM

FAST PAGE MODE (MT8D18)
LOW POWER,
EXTENDED REFRESH (MT8D18 L)

FEATURES

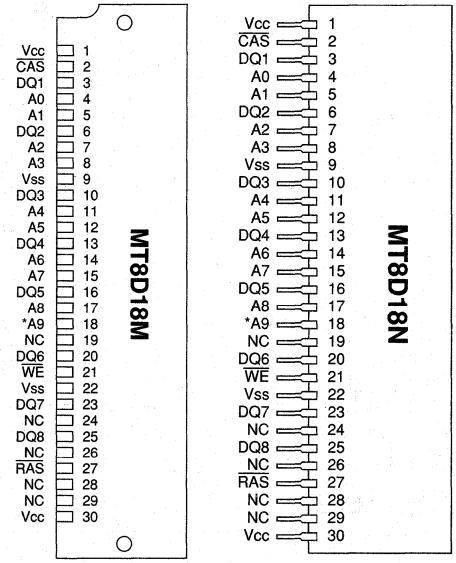
- Industry standard pinout in a 30-pin single-in-line package
- High-performance, CMOS silicon-gate process
- Single 5V ±10% power supply
- Low power, 24mW (2.4mW L-version) standby; 1,400mW active, typical
- All device pins are fully TTL compatible
- Refresh modes: RAS-ONLY, CAS-BEFORE-RAS (CBR) and HIDDEN
- 512-cycle refresh distributed across 8ms or 512-cycle extended refresh distributed across 64ms
- FAST PAGE MODE access cycle
- Low CMOS standby current, 1.6mA maximum (L-version)

OPTIONS

	MARKING
Timing	
60ns access	- 6
70ns access	- 7
80ns access	- 8
Packages	
Leadless 30-pin SIMM	M
Leaded 30-pin SIP	N
Power/Refresh	
Normal Power/8ms	Blank
Low Power/64ms	L

Part Number Example: MT8D18ML-6

PIN ASSIGNMENT (Top View)



*Address not used for RAS-ONLY REFRESH

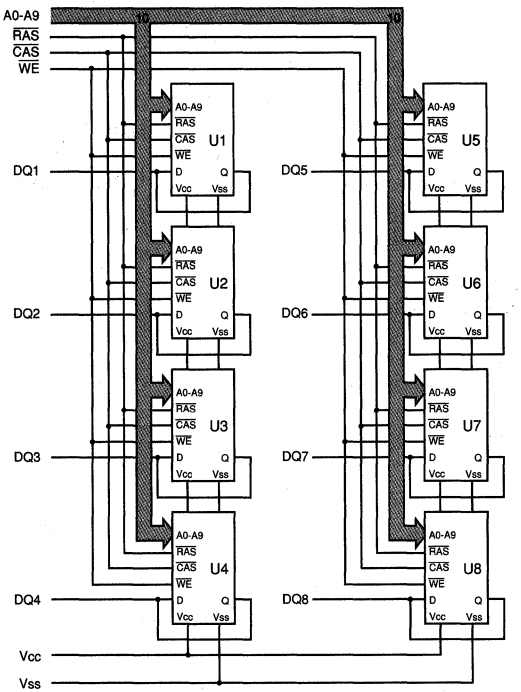
GENERAL DESCRIPTION

The MT8D18 is a randomly accessed solid-state memory containing 1,048,576 words organized in a x8 configuration. During READ or WRITE cycles, each word is uniquely addressed through the 20 address bits, which are entered 10 bits (A0-A9) at a time. RAS is used to latch the first 10 bits and CAS the latter 10 bits. READ or WRITE cycles are selected with the WE input. A logic HIGH on WE dictates READ mode while a logic LOW on WE dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of WE or CAS, whichever occurs last. Early WRITE occurs when WE goes LOW prior to CAS going LOW, and the output pins remain open (High-Z) until the next CAS cycle.

FAST PAGE MODE operations allow faster data operations (READ or WRITE) within a row-address (A0-A9) defined page boundary. The FAST PAGE MODE cycle is always initiated with a row address strobed-in by RAS followed by a column address strobed-in by CAS. CAS may be toggled-in by holding RAS LOW and strobing-in different column addresses, thus executing faster memory cycles.

Returning RAS and CAS HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the RAS high time. Memory cell data is retained in its correct state by maintaining power and executing any RAS cycles (READ, WRITE, RAS-ONLY, CAS-BEFORE-RAS or HIDDEN REFRESH) so that all 512 combinations of RAS addresses (A0-A8) are executed at least every 8ms (64ms on L-version only), regardless of sequence.

FUNCTIONAL BLOCK DIAGRAM



U1 - U8 = MT4C1024DJ
U1 - U8 = MT4C1024DJ L (L-version)

TRUTH TABLE

FUNCTION		RAS	CAS	WE	ADDRESSES tR	ADDRESSES tC	DATA IN/OUT DQ1-DQ8
Standby		H	H→X	X	X	X	High-Z
READ		L	L	H	ROW	COL	Data Out
EARLY-WRITE		L	L	L	ROW	COL	Data In
FAST-PAGE-MODE	1st Cycle	L	H→L	H	ROW	COL	Data Out
READ	2nd Cycle	L	H→L	H	n/a	COL	Data Out
FAST-PAGE-MODE	1st Cycle	L	H→L	L	ROW	COL	Data In
WRITE	2nd Cycle	L	H→L	L	n/a	COL	Data In
RAS-ONLY REFRESH		L	H	X	ROW	n/a	High-Z
HIDDEN	READ	L→H→L	L	H	ROW	COL	Data Out
REFRESH	WRITE	L→H→L	L	L	ROW	COL	Data In
CAS-BEFORE-RAS REFRESH		H→L	L	X	X	X	High-Z
BATTERY BACKUP REFRESH (L-version)		H→L	L	X	X	X	High-Z

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} ..... -1V to +7V
Operating Temperature, T_A (Ambient) ..... 0°C to +70°C
Storage Temperature (Plastic) ..... -55°C to +125°C
Power Dissipation 8W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 3, 4, 6, 7) (0°C ≤ T_A ≤ 70°C; V_{CC} = 5V ±10%)

PARAMETER/CONDITION		SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage		V_{CC}	4.5	5.5	V	1
Input High (Logic 1) Voltage, All Inputs		V_{IH}	2.4	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, All Inputs		V_{IL}	-1.0	0.8	V	1
INPUT LEAKAGE: Any Input 0V ≤ V_{IN} ≤ V_{CC}, (All other pins not under test = 0V)	D9, $\overline{CAS9}$	I_I	-2	2	µA	
	A0-A9, $\overline{RAS}$, $\overline{WE}$	I_I	-16	16	µA	
OUTPUT LEAKAGE: (Q is disabled, 0V ≤ V_{OUT} ≤ V_{CC})	DQ1-8, Q9	I_{OZ}	-10	10	µA	
OUTPUT LEVELS Output HighVoltage (I_{OUT} = -5mA)		V_{OH}	2.4		V	
Output Low Voltage (I_{OUT} = 5mA)		V_{OL}		0.4	V	

		MAX				
PARAMETER/CONDITION	SYMBOL	-6	-7	-8	UNITS	NOTES
STANDBY CURRENT: (TTL) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC1}	16	16	16	mA	
STANDBY CURRENT: (CMOS)	I_{CC2}	8	8	8	mA	23
($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} -0.2V)		1.6	1.6	1.6	mA	23, 25
OPERATING CURRENT: Random READ/WRITE Average power supply current	I_{CC3}	720	640	560	mA	3, 4
($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC (MIN))		680	600	520	mA	3, 4, 25
OPERATING CURRENT: FAST PAGE MODE Average power supply current	I_{CC4}	560	480	400	mA	3, 4
($\overline{RAS}$ = V_{IL}; $\overline{CAS}$, Address Cycling: ^tPC = ^tPC (MIN))		520	440	360	mA	3, 4, 25
REFRESH CURRENT: $\overline{RAS}$-ONLY Average power supply current	I_{CC5}	720	640	560	mA	3
($\overline{RAS}$ Cycling; $\overline{CAS}$ = V_{IH}: ^tRC = ^tRC (MIN))		680	600	520	mA	3, 25
REFRESH CURRENT: $\overline{CAS}$-BEFORE-$\overline{RAS}$ Average power supply current	I_{CC6}	720	640	560	mA	3, 5
($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC (MIN))		680	600	520	mA	3, 5, 25
REFRESH CURRENT: BATTERY BACKUP (BBU) Average power supply current during BATTERY BACKUP refresh: $\overline{CAS}$ = 0.2V or $\overline{CAS}$-BEFORE-$\overline{RAS}$ cycling; $\overline{RAS}$ = ^tRAS (MIN) to 1µs; $\overline{WE}$, A0-A9 and D_{IN} = V_{CC} -0.2V or 0.2V (D_{IN} may be left OPEN), ^tRC = 125µs (512 rows at 125µs = 64ms)	I_{CC7}	1.6	1.6	1.6	mA	25

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A9	C_{I1}		51	pF	2
Input Capacitance: $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	C_{I2}		67	pF	2
Input/Output Capacitance: DQ1-DQ8	C_{IO}		16	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C ≤ T_A ≤ 70°C; Vcc = 5V ±10%)

AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	^tRC	110		130		150		ns	
READ-WRITE cycle time	^tRWC	n/a		n/a		n/a		n/a	24
FAST-PAGE-MODE READ or WRITE cycle time	^tPC	40		40		ns			
FAST-PAGE-MODE READ-WRITE cycle time	^tPRWC	n/a		n/a		n/a		n/a	24
Access time from $\overline{RAS}$	^tRAC		60		70		80	ns	14
Access time from $\overline{CAS}$	^tCAC		20		20		20	ns	15
Access time from column address	^tAA		30		35		40	ns	
Access time from $\overline{CAS}$ precharge	^tCPA		35		40		45	ns	
$\overline{RAS}$ pulse width	^tRAS	60	100,000	70	100,000	80	100,000	ns	
$\overline{RAS}$ pulse width (FAST PAGE MODE)	^tRASP	60	100,000	70	100,000	80	100,000	ns	
$\overline{RAS}$ hold time	^tRSH	20		20		20		ns	
$\overline{RAS}$ precharge time	^tRP	40		50		60		ns	
$\overline{CAS}$ pulse width	^tCAS	20	100,000	20	100,000	20	100,000	ns	
$\overline{CAS}$ hold time	^tCSH	60		70		80		ns	
$\overline{CAS}$ precharge time	^tCPN	10		10		10		ns	16
$\overline{CAS}$ precharge time (FAST PAGE MODE)	^tCP	10		10		10		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	^tRCD	20	40	20	60	20	60	ns	17
$\overline{CAS}$ to $\overline{RAS}$ precharge time	^tCRP	5		5		5		ns	
Row address setup time	^tASR	0		0		0		ns	
Row address hold time	^tRAH	10		10		10		ns	
$\overline{RAS}$ to column address delay time	^tRAD	15	30	15	35	15	40	ns	18
Column address setup time	^tASC	0		0		0		ns	
Column address hold time	^tCAH	15		15		15		ns	
Column address hold time (referenced to $\overline{RAS}$)	^tAR	45		55		60		ns	
Column address to $\overline{RAS}$ lead time	^tRAL	30		35		40		ns	
Read command setup time	^tRCS	0		0		0		ns	
Read command hold time (referenced to $\overline{CAS}$)	^tRCH	0		0		0		ns	19
Read command hold time (referenced to $\overline{RAS}$)	^tRRH	0		0		0		ns	19

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

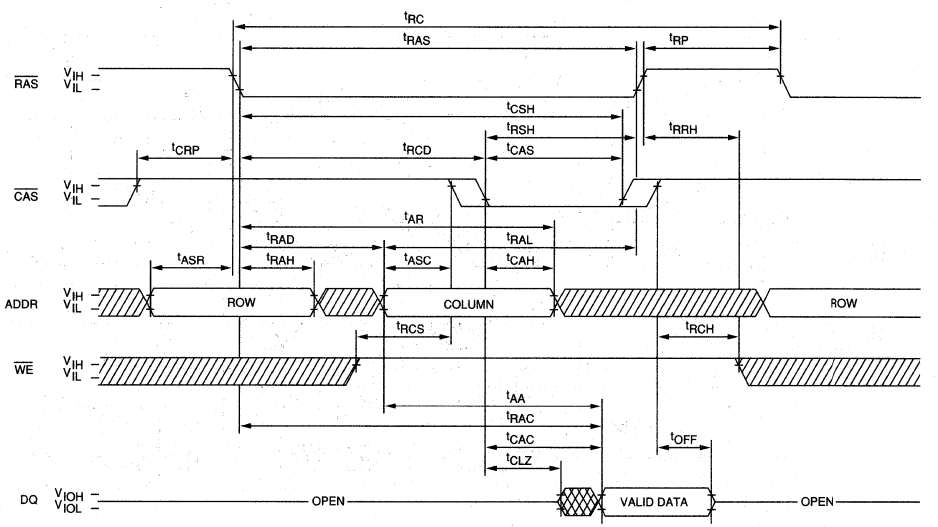
(Notes: 6, 7, 8, 9, 10, 11, 12, 13) ($0°C \le T_A \le 75°C$; $V_{CC} = 5V \pm 10\%$)

AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
$\overline{CAS}$ to output in Low-Z	^tCLZ	0		0		0		ns	
Output buffer turn-off delay	^tOFF	0	20	0	20	0	20	ns	20
$\overline{WE}$ command setup time	^tWCS	0		0		0		ns	
Write command hold time	^tWCH	10		15		15		ns	
Write command hold time (referenced to $\overline{RAS}$)	^tWCR	45		55		60		ns	
Write command pulse width	^tWP	10		15		15		ns	
Write command to $\overline{RAS}$ lead time	^tRWL	20		20		20		ns	
Write command to $\overline{CAS}$ lead time	^tCWL	20		20		20		ns	
Data-in setup time	^tDS	0		0		0		ns	21
Data-in hold time	^tDH	15		15		15		ns	21
Data-in hold time (referenced to $\overline{RAS}$)	^tDHR	45		55		60		ns	
Transition time (rise or fall)	^tT	3	50	3	50	3	50	ns	9, 10
Refresh period (512 cycles)	^tREF		8/64		8/64		8/64	ms	7/25
$\overline{RAS}$ to $\overline{CAS}$ precharge time	^tRPC	0		0		0		ns	
$\overline{CAS}$ setup time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH)	^tCSR	10		10		10		ns	5
$\overline{CAS}$ hold time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH)	^tCHR	10		15		15		ns	5

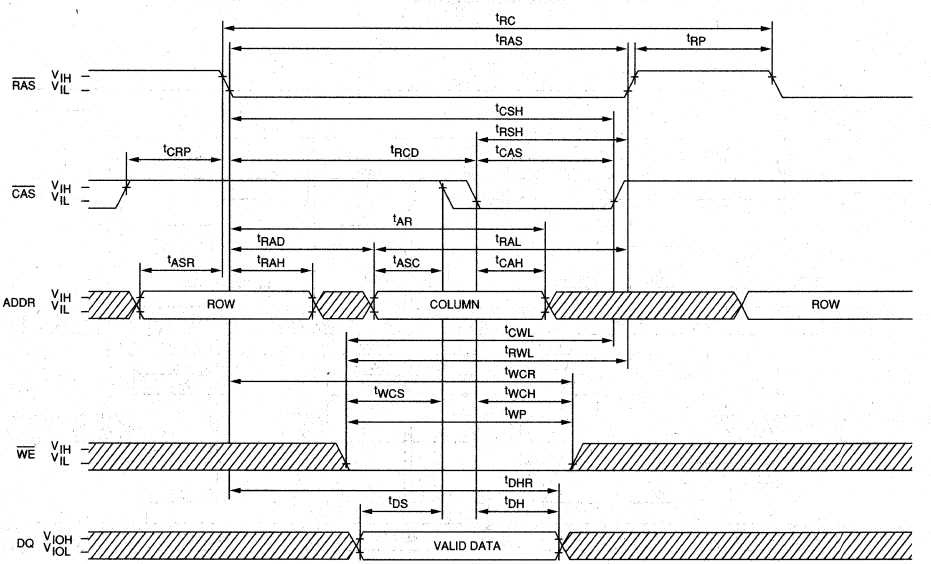
NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. Capacitance is measured using MIL-STD-883C, Method 3012.1 (1 MHz AC, Vcc = 5V, DC bias = 2.4V @ 15mV RMS).
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \le T_A \le 70°C$) is assured.
7. An initial pause of 100µs is required after power-up followed by any eight $\overline{RAS}$ cycles before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-up should be repeated any time the ^tREF refresh requirement is exceeded.
8. AC characteristics assume ^tT = 5ns.
9. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS}$ = V_{IH}, data output is High-Z.
12. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to 2 TTL gates and 100pF.
14. Assumes that $^tRCD < ^tRCD$ (MAX). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
15. Assumes that $^tRCD \ge ^tRCD$ (MAX).
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer, $\overline{CAS}$ must be pulsed HIGH for ^tCPN.
17. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (MAX) limit, then access time is controlled exclusively by ^tCAC.
18. Operation within the ^tRAD (MAX) limit ensures that ^tRCD (MAX) can be met. ^tRAD (MAX) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (MAX) limit, then access time is controlled exclusively by ^tAA.
19. Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
20. ^tOFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
21. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY-WRITE cycles.
22. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW.
23. All other inputs equal Vcc -0.2V.
24. LATE-WRITE, READ-WRITE or READ-MODIFY-WRITE cycles are not available due to the common DQ configuration of U1-U8.
25. Applies to the L-version only.

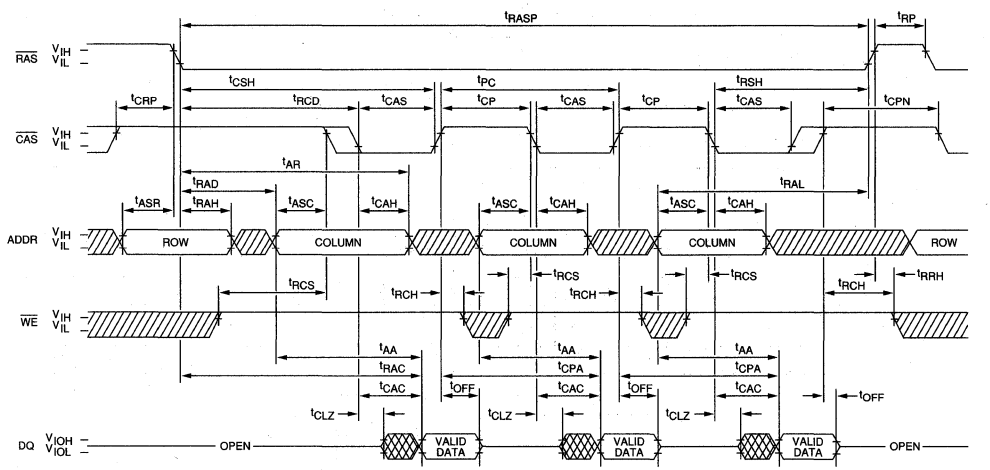
READ CYCLE



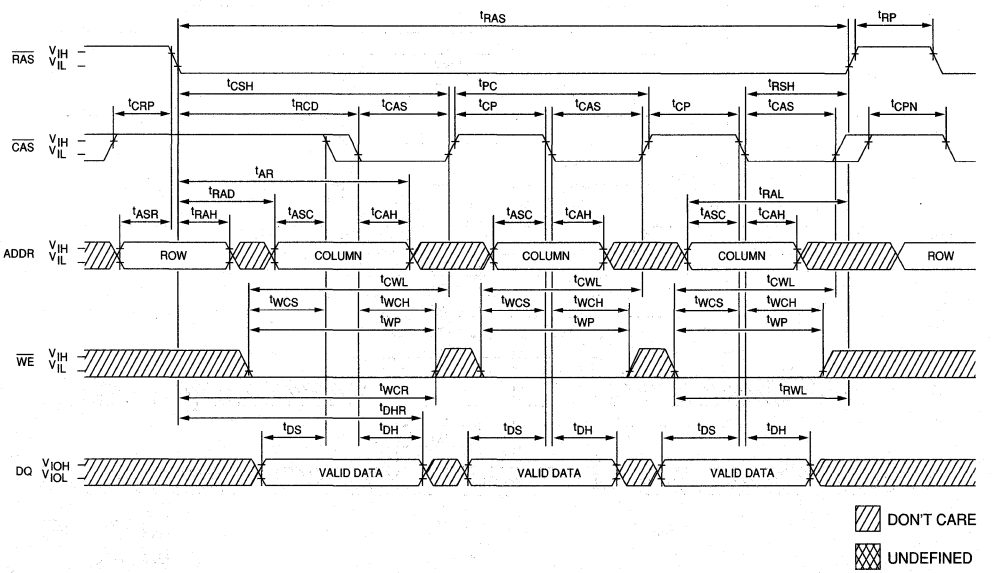
EARLY-WRITE CYCLE



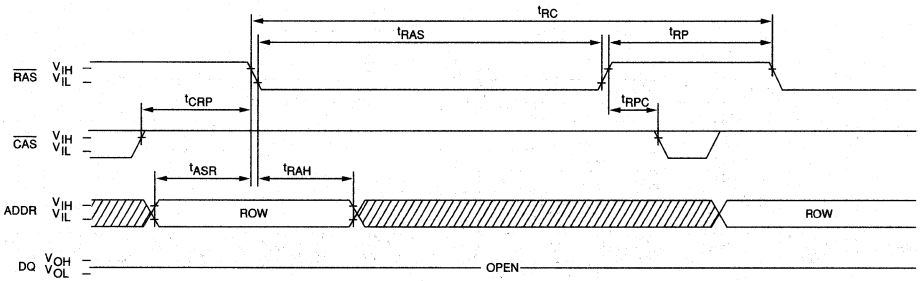
FAST-PAGE-MODE READ CYCLE



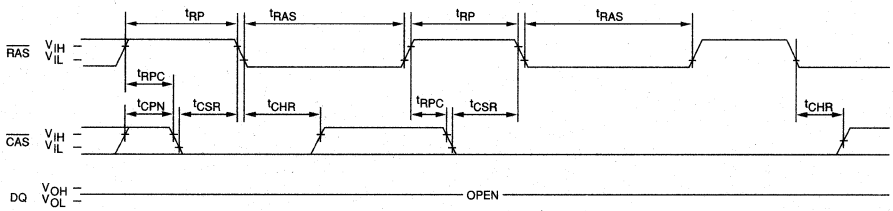
FAST-PAGE-MODE EARLY-WRITE CYCLE



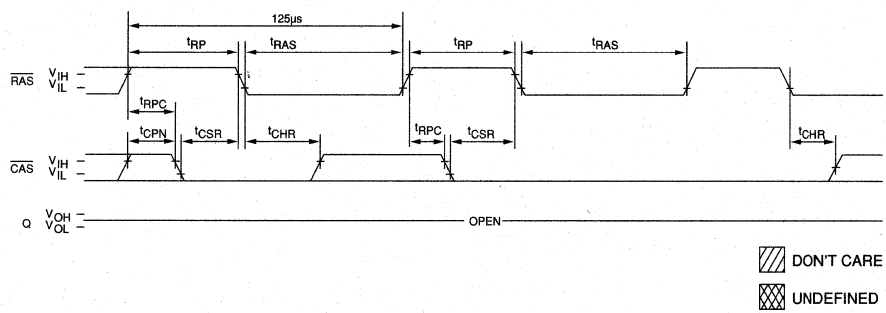
$\overline{\text{RAS}}$-ONLY REFRESH CYCLE
(ADDR = A0-A8; A9 and $\overline{\text{WE}}$ = DON'T CARE)



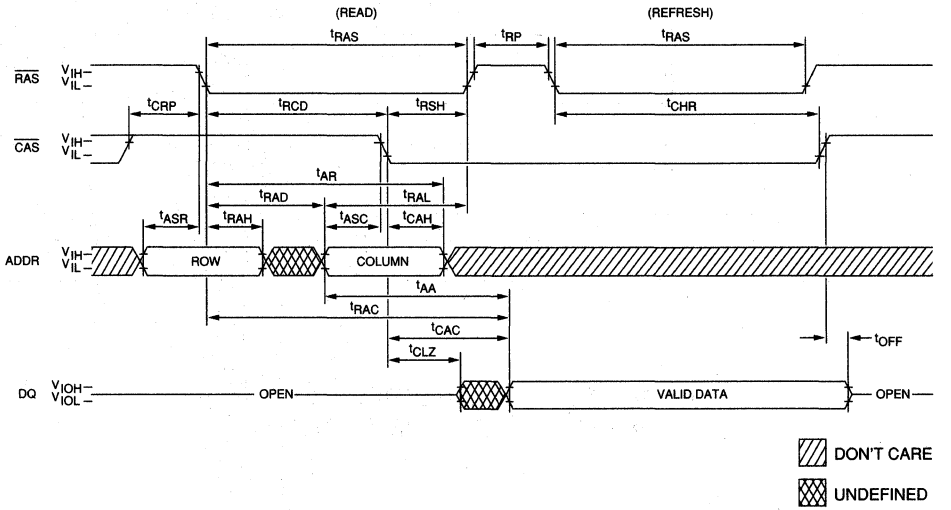
$\overline{\text{CAS}}$-BEFORE-$\overline{\text{RAS}}$ REFRESH CYCLE
(A0-A9 and $\overline{\text{WE}}$ = DON'T CARE)



BATTERY BACKUP REFRESH CYCLE [25]
(A0-A9 and $\overline{\text{WE}}$ = DON'T CARE)



HIDDEN REFRESH CYCLE [22]
($\overline{WE}$ = HIGH)



DRAM MODULE

4 MEG x 8 DRAM

FAST PAGE MODE

NEW DRAM MODULE

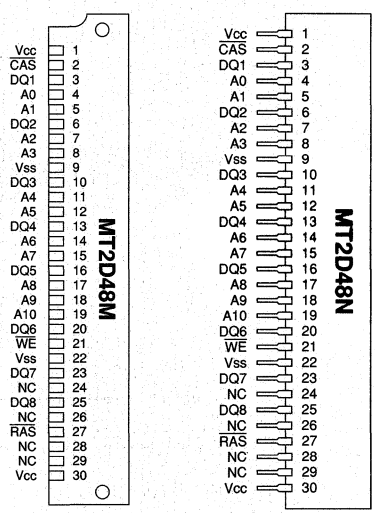
FEATURES

- Industry standard pinout in a 30-pin, single-in-line memory module
- High-performance, CMOS silicon-gate process
- Single 5V ±10% power supply
- Low power, 6mW standby; 550mW active, typical
- All device pins are fully TTL compatible
- FAST PAGE MODE access cycle
- Refresh modes: $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$ (CBR) and HIDDEN
- 2,048-cycle refresh distributed across 32ms
- Low profile

OPTIONS MARKING

- Timing
  - 60ns access - 6
  - 70ns access - 7
  - 80ns access - 8
- Packages
  - Leadless 30-pin SIMM M
  - Leaded 30-pin SIP N
- Part Number Example: MT2D48M-6

PIN ASSIGNMENT (Top View)



GENERAL DESCRIPTION

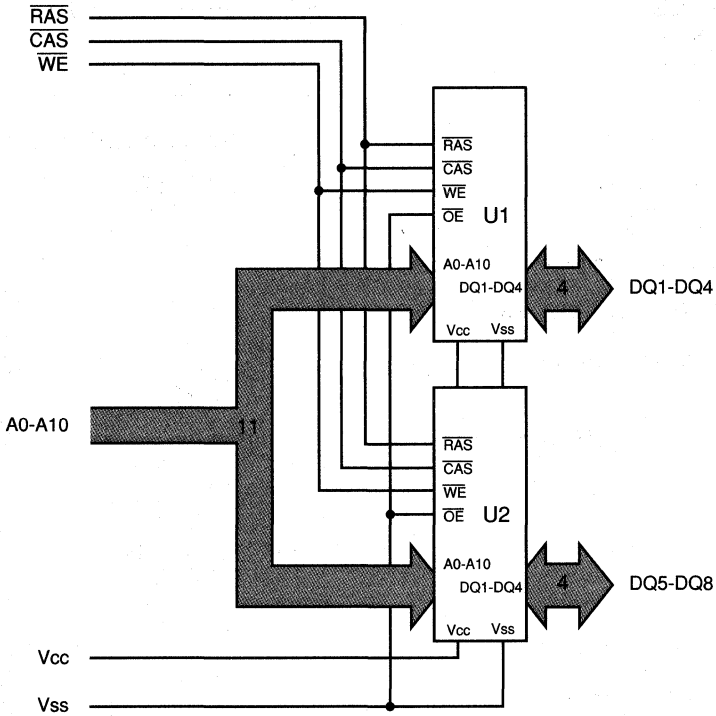
The MT2D48 is a randomly accessed solid-state memory containing 4,194,304 words organized in a x8 configuration. During READ or WRITE cycles, each word is uniquely addressed through 22 address bits, which are entered 11 bits (A0-A10) at a time. $\overline{RAS}$ is used to latch the first 11 bits and $\overline{CAS}$ the latter 11 bits. READ or WRITE cycles are selected with the $\overline{WE}$ input. A logic HIGH on $\overline{WE}$ dictates READ mode while a logic LOW on $\overline{WE}$ dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of $\overline{CAS}$. Since $\overline{WE}$ goes LOW prior to $\overline{CAS}$ going LOW, the output pins remain open (High-Z) until the next $\overline{CAS}$ cycle.

FAST PAGE MODE operations allow faster data operations (READ or WRITE) within a row address (A0-A10) defined page boundary. The FAST PAGE MODE cycle is always initiated with a row address strobed-in by $\overline{RAS}$ followed by a column address strobed-in by $\overline{CAS}$. $\overline{CAS}$ may be toggled-in by holding $\overline{RAS}$ LOW and strobing-in different column addresses, thus executing faster memory cycles. Returning $\overline{RAS}$ HIGH terminates the FAST-PAGE-MODE operations.

Returning $\overline{RAS}$ and $\overline{CAS}$ HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the $\overline{RAS}$ high time. Memory cell data is retained in its correct state by maintaining power and executing any $\overline{RAS}$ cycle (READ, WRITE, $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$ or HIDDEN REFRESH) so that all 2,048 combinations of $\overline{RAS}$ addresses (A0-A10) are executed at least every 32ms, regardless of sequence. The CBR REFRESH cycle will invoke the refresh counter for automatic $\overline{RAS}$ addressing.

NEW ■ DRAM MODULE

FUNCTIONAL BLOCK DIAGRAM



U1, U2 = MT4C4M4B1DJ

TRUTH TABLE

FUNCTION		RAS	CAS	WE	ADDRESSES		DATA IN/OUT
					^tR	^tC	DQ1-DQ8
Standby		H	H→X	X	X	X	High-Z
READ		L	L	H	ROW	COL	Data Out
EARLY-WRITE		L	L	L	ROW	COL	Data In
FAST-PAGE-MODE	1st Cycle	L	H→L	H	ROW	COL	Data Out
READ	2nd Cycle	L	H→L	H	n/a	COL	Data Out
FAST-PAGE-MODE	1st Cycle	L	H→L	L	ROW	COL	Data In
WRITE	2nd Cycle	L	H→L	L	n/a	COL	Data In
RAS-ONLY REFRESH		L	H	X	ROW	n/a	High-Z
HIDDEN	READ	L→H→L	L	H	ROW	COL	Data Out
REFRESH	WRITE	L→H→L	L	L	ROW	COL	Data In
CAS-BEFORE-RAS REFRESH		H→L	L	H	X	X	High-Z

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} ..... -1V to +7V
Operating Temperature, T_A (Ambient) ..... 0°C to +70°C
Storage Temperature ..... -55°C to +125°C
Power Dissipation 2W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 3, 4, 6, 7) (0°C ≤ T_A ≤ 70°C; V_{CC} = 5V ±10%)

PARAMETER/CONDITION		SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage		V_{CC}	4.5	5.5	V	1
Input High (Logic 1) Voltage, All Inputs		V_{IH}	2.4	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, All Inputs		V_{IL}	-1.0	0.8	V	1
INPUT LEAKAGE Any Input 0V ≤ V_{IN} ≤ V_{CC} (All other pins not under test = 0V)	A0-A10, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	I_I	-4	4	µA	
OUTPUT LEAKAGE (Q is disabled, 0V ≤ V_{OUT} ≤ V_{CC})	DQ1-DQ8	I_{OZ}	-10	10	µA	
OUTPUT LEVELS Output High (Logic 1) Voltage (I_{OUT} = -5mA)		V_{OH}	2.4		V	
Output Low (Logic 0) Voltage (I_{OUT} = 5mA)		V_{OL}		0.4	V	

		MAX				
PARAMETER/CONDITION	SYMBOL	-6	-7	-8	UNITS	NOTES
STANDBY CURRENT: (TTL) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC1}	4	4	4	mA	
STANDBY CURRENT: (CMOS) ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} -0.2V)	I_{CC2}	2	2	2	mA	
OPERATING CURRENT: Random READ/WRITE Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC (MIN))	I_{CC3}	240	200	180	mA	3, 4
OPERATING CURRENT: FAST PAGE MODE Average power supply current ($\overline{RAS}$ = V_{IL}; $\overline{CAS}$, Address Cycling: ^tPC = ^tPC (MIN))	I_{CC4}	160	140	120	mA	3, 4
REFRESH CURRENT: $\overline{RAS}$-ONLY Average power supply current ($\overline{RAS}$ Cycling; $\overline{CAS}$ = V_{IH}: ^tRC = ^tRC (MIN))	I_{CC5}	240	200	180	mA	3
REFRESH CURRENT: $\overline{CAS}$-BEFORE-$\overline{RAS}$ Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC (MIN))	I_{CC6}	240	200	180	mA	3, 5

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A10	C_{I1}		13	pF	2
Input Capacitance: $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	C_{I2}		17	pF	2
Input/Output Capacitance: DQ1-DQ8	C_{IO}		10	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13, 22) (V_{CC} = 5V ±10%)

AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	t_{RC}	110		130		150		ns	
READ-WRITE cycle time	t_{RWC}	n/a		n/a		n/a		ns	22
FAST-PAGE-MODE READ or WRITE cycle time	t_{PC}	40		40		45		ns	
FAST-PAGE-MODE READ-WRITE cycle time	t_{PRWC}	n/a		n/a		n/a		ns	22
Access time from $\overline{RAS}$	t_{RAC}		60		70		80	ns	14
Access time from $\overline{CAS}$	t_{CAC}		15		20		20	ns	15
Access time from column address	t_{AA}		30		35		40	ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		35		40		45	ns	
$\overline{RAS}$ pulse width	t_{RAS}	60	100,000	70	100,000	80	100,000	ns	
$\overline{RAS}$ pulse width (FAST PAGE MODE)	t_{RASP}	60	100,000	70	100,000	80	100,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	15		20		20		ns	
$\overline{RAS}$ precharge time	t_{RP}	40		50		60		ns	
$\overline{CAS}$ pulse width	t_{CAS}	15	100,000	20	100,000	20	100,000	ns	
$\overline{CAS}$ hold time	t_{CSH}	60		70		80		ns	
$\overline{CAS}$ precharge time	t_{CPN}	10		10		10		ns	16
$\overline{CAS}$ precharge time (FAST PAGE MODE)	t_{CP}	10		10		10		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	45	20	50	20	60	ns	17
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		5		ns	
Row address setup time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	10		10		10		ns	
$\overline{RAS}$ to column address delay time	t_{RAD}	15	30	15	35	15	40	ns	18
Column address setup time	t_{ASC}	0		0		0		ns	
Column address hold time	t_{CAH}	10		15		15		ns	
Column address hold time (referenced to $\overline{RAS}$)	t_{AR}	50		55		60		ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	30		35		40		ns	
Read command setup time	t_{RCS}	0		0		0		ns	
Read command hold time (referenced to $\overline{CAS}$)	t_{RCH}	0		0		0		ns	19
Read command hold time (referenced to $\overline{RAS}$)	t_{RRH}	0		0		0		ns	19
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	0		0		0		ns	
Output buffer turn-off delay	t_{OFF}	0	15	0	20	0	20	ns	20
$\overline{WE}$ command setup time	t_{WCS}	0		0		0		ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13, 23) (V_{CC} = 5V ±10%)

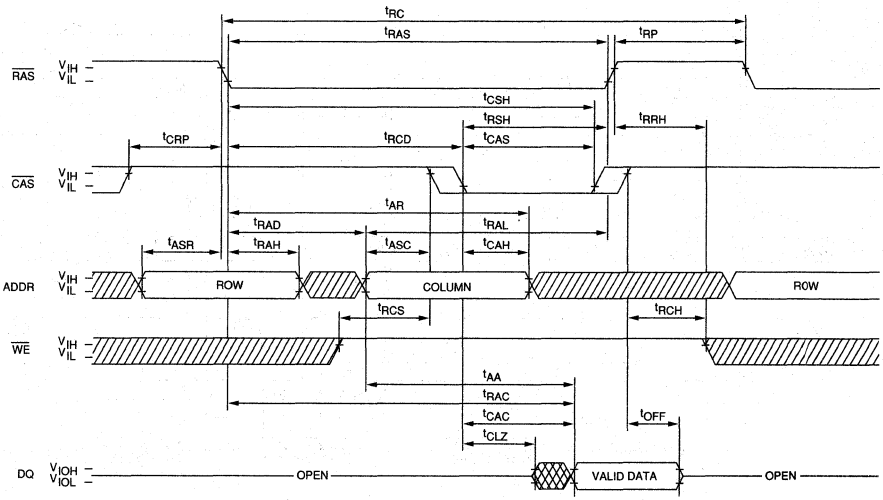
AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Write command hold time	^tWCH	10		15		15		ns	
Write command hold time (referenced to $\overline{RAS}$)	^tWCR	45		55		60		ns	
Write command pulse width	^tWP	10		15		15		ns	
Write command to $\overline{RAS}$ lead time	^tRWL	15		20		20		ns	
Write command to $\overline{CAS}$ lead time	^tCWL	15		20		20		ns	
Data-in setup time	^tDS	0		0		0		ns	21
Data-in hold time	^tDH	10		15		15		ns	21
Data-in hold time (referenced to $\overline{RAS}$)	^tDHR	45		55		60		ns	
Transition time (rise or fall)	^tT	3	50	3	50	3	50	ns	9, 10
Refresh period (2,048 cycles)	^tREF		32		32		32	ms	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	^tRPC	0		0		0		ns	
$\overline{CAS}$ setup time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tCSR	5		5		5		ns	5
$\overline{CAS}$ hold time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tCHR	15		15		15		ns	5
$\overline{WE}$ hold time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tWRH	10		10		10		ns	24
$\overline{WE}$ setup time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tWRP	10		10		10		ns	24
$\overline{WE}$ hold time (WCBR test cycle)	^tWTH	10		10		10		ns	24
$\overline{WE}$ setup time (WCBR test cycle)	^tWTS	10		10		10		ns	24

NEW ■ DRAM MODULE

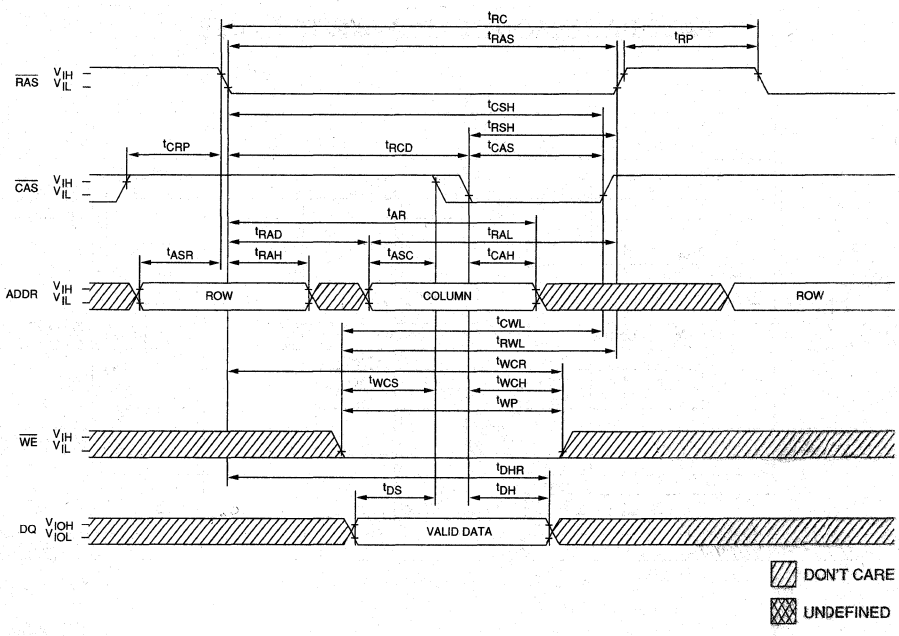
NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. Capacitance is measured using MIL-STD-883C, Method 3012.1 (1 MHz AC, Vcc = 5V, DC bias = 2.4V @ 15mV RMS).
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is assured.
7. An initial pause of 100µs is required after power-up followed by eight $\overline{RAS}$ refresh cycles ($\overline{RAS}$-ONLY or CBR with $\overline{WE}$ HIGH) before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-up should be repeated any time the ^tREF refresh requirement is exceeded.
8. AC characteristics assume ^tT = 5ns.
9. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS}$ = V_{IH}, data output is High-Z.
12. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to 2 TTL gates and 100pF.
14. Assumes that $^tRCD < ^tRCD$ (MAX). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
15. Assumes that $^tRCD \geq ^tRCD$ (MAX).
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer, $\overline{CAS}$ must be pulsed HIGH for ^tCPN.
17. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (MAX) limit, then access time is controlled exclusively by ^tCAC.
18. Operation within the ^tRAD (MAX) limit ensures that ^tRCD (MAX) can be met. ^tRAD (MAX) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (MAX) limit, then access time is controlled exclusively by ^tAA.
19. Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
20. ^tOFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
21. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY-WRITE cycles.
22. $\overline{OE}$ is tied permanently LOW; LATE-WRITE or READ-MODIFY-WRITE operations are not possible.
23. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW and $\overline{OE}$=HIGH.
24. ^tWTS and ^tWTH are setup and hold specifications for the $\overline{WE}$ pin being held LOW to enable the JEDEC test mode (with CBR timing constraints). These two parameters are the inverts of ^tWRP and ^tWRH in the CBR refresh cycle.

READ CYCLE

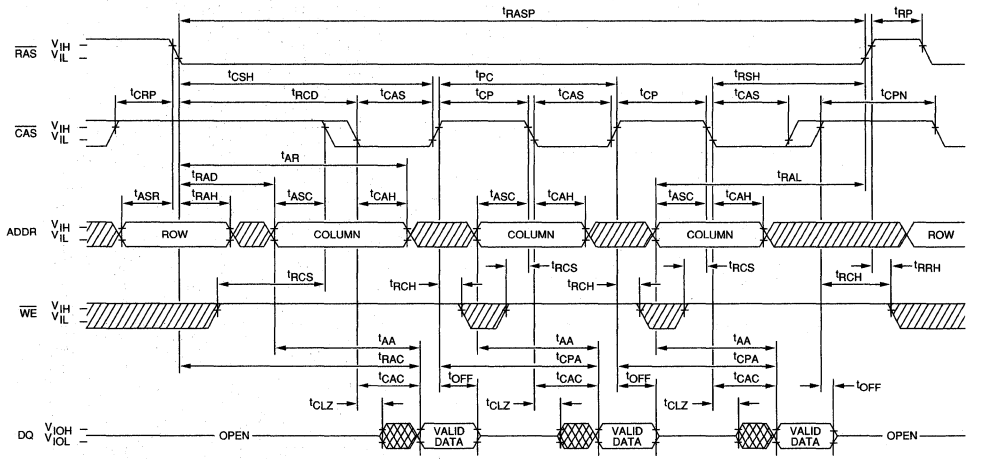


EARLY-WRITE CYCLE

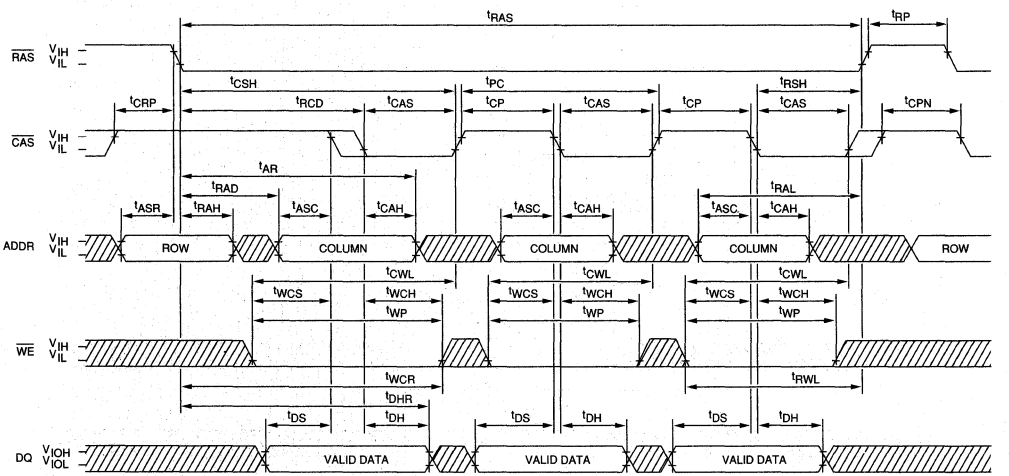


NEW ■ DRAM MODULE

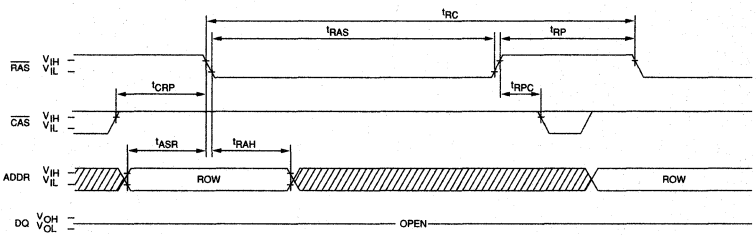
FAST-PAGE-MODE READ CYCLE



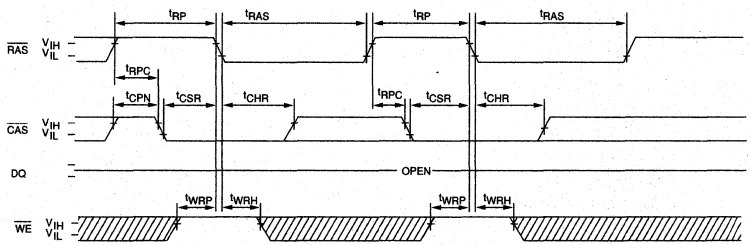
FAST-PAGE-MODE EARLY-WRITE CYCLE



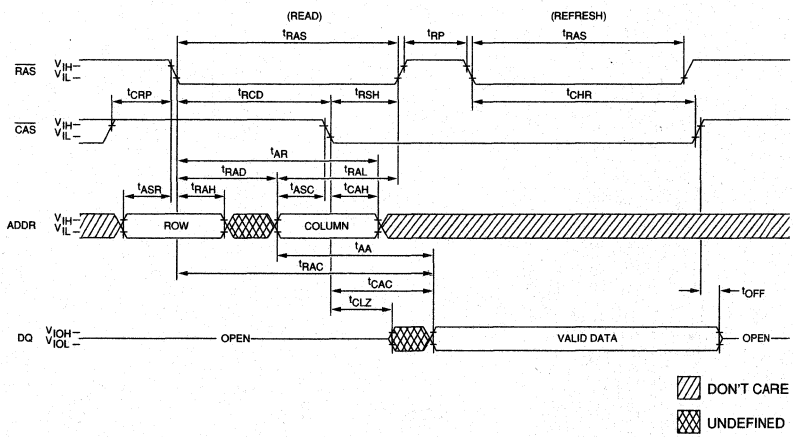
RAS-ONLY REFRESH CYCLE
(ADDR = A0-A10; WE = DON'T CARE)



CAS-BEFORE-RAS REFRESH CYCLE
(A0-A10 = DON'T CARE)



HIDDEN REFRESH CYCLE [23]
(WE = HIGH)



DRAM MODULE

4 MEG x 8 DRAM

FAST PAGE MODE (MT8D48)
LOW POWER,
EXTENDED REFRESH (MT8D48 L)

FEATURES

- Industry standard pinout in a 30-pin single-in-line package
- High-performance, CMOS silicon-gate process
- Single 5V ±10% power supply
- All device pins are fully TTL compatible
- Low power, 24mW (8mW L-version) standby; 1,800mW active, typical
- Refresh modes: RAS-ONLY, CAS-BEFORE-RAS (CBR) and HIDDEN
- 1,024-cycle refresh distributed across 16ms or 1,024-cycle extended refresh distributed across 128ms
- FAST PAGE MODE access cycle
- Low CMOS standby current, 1.6mA maximum (L-version)

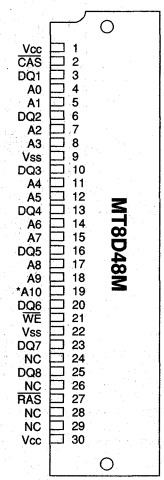
OPTIONS

	MARKING
Timing	
60ns access	-6
70ns access	-7
80ns access	-8
Packages	
Leadless 30-pin SIMM	M
Leaded 30-pin SIP	N
Power/Refresh	
Normal Power/16ms	Blank
Low Power/128ms	L

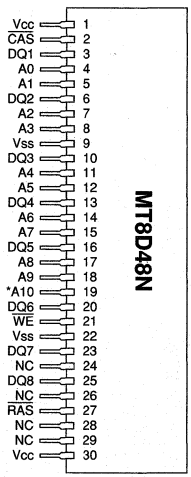
Part Number Example: MT8D48ML-6

PIN ASSIGNMENT (Top View)

30-Pin SIMM (T-3)



30-Pin SIP (S-3)



*Address not used for RAS-ONLY REFRESH

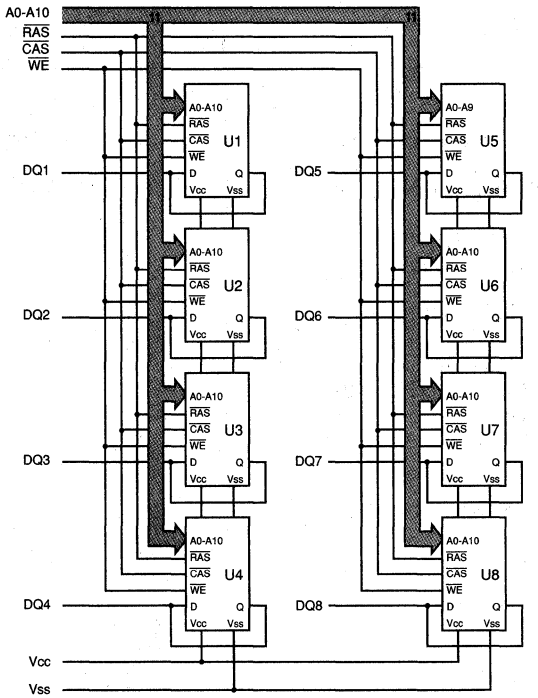
GENERAL DESCRIPTION

The MT8D48 is a randomly accessed solid-state memory containing 4,194,304 words organized in a x8 configuration. During READ or WRITE cycles, each bit is uniquely addressed through the 22 address bits which are entered 11 bits (A0-A10) at a time. RAS is used to latch the first 11 bits and CAS the latter 11 bits. A READ or WRITE cycle is selected with the WE input. A logic HIGH on WE dictates READ mode, while a logic LOW on WE dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of WE or CAS, whichever occurs last. If WE goes LOW prior to CAS going LOW, the output pin(s) remain open (High-Z) until the next CAS cycle. EARLY-WRITE occurs when WE goes LOW prior to CAS going LOW, and the ouput remains open (High-Z) until the next CAS cycle.

FAST PAGE MODE operations allow faster data operations (READ or WRITE) within a row-address (A0-A10) defined page boundary. The FAST PAGE MODE cycle is always initiated with a row address strobed-in by RAS followed by a column address strobed-in by CAS. CAS may be toggled-in by holding RAS LOW and strobing-in different column addresses, thus executing faster memory cycles. Returning RAS HIGH terminates the FAST PAGE MODE operation.

Returning RAS and CAS HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the RAS high time. Memory cell data is retained in its correct state by maintaining power and executing any RAS cycle (READ, WRITE, RAS-ONLY, CAS-BEFORE-RAS or HIDDEN REFRESH) so that all 1,024 combinations of RAS addresses (A0-A9) are executed at least every16ms (128ms on L-version), regardless of sequence.

FUNCTIONAL BLOCK DIAGRAM



U1-U8 = MT4C1004JDJ
U1-U8 = MT4C1004JDJ L (L-version)

TRUTH TABLE

FUNCTION		RAS	CAS	WE	ADDRESSES tR	ADDRESSES tC	DATA IN/OUT DQ1-DQ8
Standby		H	H→X	X	X	X	High-Z
READ		L	L	H	ROW	COL	Data Out
EARLY-WRITE		L	L	L	ROW	COL	Data In
FAST-PAGE-MODE	1st Cycle	L	H→L	H	ROW	COL	Data Out
READ	2nd Cycle	L	H→L	H	n/a	COL	Data Out
FAST-PAGE-MODE	1st Cycle	L	H→L	L	ROW	COL	Data In
WRITE	2nd Cycle	L	H→L	L	n/a	COL	Data In
RAS-ONLY REFRESH		L	H	X	ROW	n/a	High-Z
HIDDEN	READ	L→H→L	L	H	ROW	COL	Data Out
REFRESH	WRITE	L→H→L	L	L	ROW	COL	Data In
CAS-BEFORE-RAS REFRESH		H→L	L	H	X	X	High-Z
BATTERY BACKUP REFRESH (L-version)		H→L	L	X	X	X	High-Z

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} ..... -1V to +7V
Operating Temperature, T_A (Ambient) ..... 0°C to +70°C
Storage Temperature (Plastic) ..... -55°C to +125°C
Power Dissipation 8W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 3, 4, 6, 7) (0°C ≤ T_A ≤ 70°C; V_{CC} = 5V ±10%)

PARAMETER/CONDITION		SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage		V_{CC}	4.5	5.5	V	1
Input High (Logic 1) Voltage, All Inputs		V_{IH}	2.4	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, All Inputs		V_{IL}	-1.0	0.8	V	1
INPUT LEAKAGE CURRENT Any Input: 0V ≤ V_{IN} ≤ 6.5V (All other pins not under test = 0V)	A0-A10, $\overline{WE}$, $\overline{CAS}$, $\overline{RAS}$	I_I	-16	16	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled, 0V ≤ V_{OUT} ≤ 5.5V)	DQ1-DQ8	I_{OZ}	-10	10	µA	
OUTPUT LEVELS Output High Voltage (I_{OUT} = -5mA)		V_{OH}	2.4		V	
Output Low Voltage (I_{OUT} = 4.2mA)		V_{OL}		0.4	V	

		MAX				
PARAMETER/CONDITION	SYMBOL	-6	-7	-8	UNITS	NOTES
STANDBY CURRENT: (TTL) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC1}	16	16	16	mA	
STANDBY CURRENT: (CMOS)	I_{CC2}	8	8	8	mA	23
($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} -0.2V)		1.6	1.6	1.6	mA	23, 26
OPERATING CURRENT: Random READ/WRITE Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC (MIN))	I_{CC3}	880	800	720	mA	3, 4
OPERATING CURRENT: FAST PAGE MODE Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: ^tPC = ^tPC (MIN))	I_{CC4}	640	560	480	mA	3, 4
REFRESH CURRENT: $\overline{RAS}$-ONLY Average power supply current ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}: ^tRC = ^tRC (MIN))	I_{CC5}	880	800	720	mA	3
REFRESH CURRENT: $\overline{CAS}$-BEFORE-$\overline{RAS}$ Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC (MIN))	I_{CC6}	880	800	720	mA	3, 5
REFRESH CURRENT: BATTERY BACKUP (BBU) Average power supply current during BATTERY BACKUP refresh: $\overline{CAS}$ = 0.2V or $\overline{CAS}$-BEFORE-$\overline{RAS}$ cycling; $\overline{RAS}$ = ^tRAS (MIN) to 300ns; $\overline{WE}$ = V_{CC} -0.2V, A0-A9 and D_{IN} = V_{CC} - 0.2V or 0.2V (D_{IN} may be left open), ^tRC = 125µs (1,024 rows at 125µs = 128ms)	I_{CC7}	2.4	2.4	2.4	mA	26

CAPACITANCE

DESCRIPTION	SYMBOL	MAX	UNITS	NOTES
Input Capacitance: A0-A10	C_{I1}	51	pF	2
Input Capacitance: $\overline{RAS}$, $\overline{WE}$	C_{I2}	67	pF	2
Input/Output Capacitance: DQ1-DQ8	C_{IO}	15	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (V_{CC} = 5V ±10%)

AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	t_{RC}	110		130		150		ns	
READ-WRITE cycle time	t_{RWC}	n/a		n/a		n/a		n/a	24
FAST-PAGE-MODE READ or WRITE cycle time	t_{PC}	40		40		45		ns	
FAST-PAGE-MODE READ-WRITE cycle time	t_{PRWC}	n/a		n/a		n/a		n/a	24
Access time from $\overline{RAS}$	t_{RAC}		60		70		80	ns	14
Access time from $\overline{CAS}$	t_{CAC}		15		20		20	ns	15
Access time from column address	t_{AA}		30		35		40	ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		35		40		45	ns	
$\overline{RAS}$ pulse width	t_{RAS}	60	100,000	70	100,000	80	100,000	ns	
$\overline{RAS}$ pulse width (FAST PAGE MODE)	t_{RASP}	60	100,000	70	100,000	80	100,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	15		20		20		ns	
$\overline{RAS}$ precharge time	t_{RP}	40		50		60		ns	
$\overline{CAS}$ pulse width	t_{CAS}	15	100,000	20	100,000	20	100,000	ns	
$\overline{CAS}$ hold time	t_{CSH}	60		70		80		ns	
$\overline{CAS}$ precharge time	t_{CPN}	10		10		10		ns	16
$\overline{CAS}$ precharge time (FAST PAGE MODE)	t_{CP}	10		10		10		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	45	20	50	20	60	ns	17
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		10		10		ns	
Row address setup time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	10		10		10		ns	
$\overline{RAS}$ to column address delay time	t_{RAD}	15	30	15	35	15	40	ns	18
Column address setup time	t_{ASC}	0		0		0		ns	
Column address hold time	t_{CAH}	10		15		15		ns	
Column address hold time (referenced to $\overline{RAS}$)	t_{AR}	50		55		60		ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	30		35		40		ns	
Read command setup time	t_{RCS}	0		0		0		ns	
Read command hold time (referenced to $\overline{CAS}$)	t_{RCH}	0		0		0		ns	19
Read command hold time (referenced to $\overline{RAS}$)	t_{RRH}	0		0		0		ns	19
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	0		0		0		ns	
Output buffer turn-off delay	t_{OFF}	0	15	0	20	0	20	ns	20
$\overline{WE}$ command setup time	t_{WCS}	0		0		0		ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

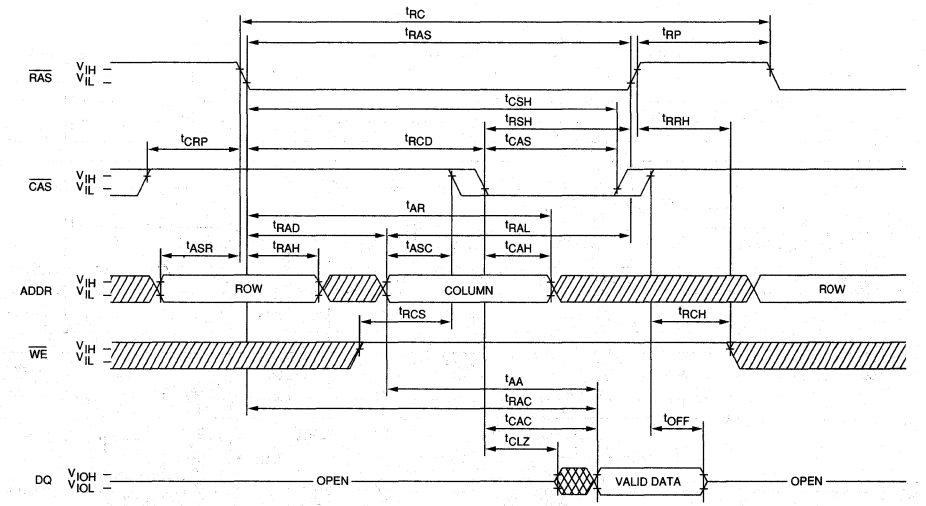
(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (V_{CC} = 5V ±10%)

AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Write command hold time	^tWCH	10		15		15		ns	
Write command hold time (referenced to $\overline{RAS}$)	^tWCR	45		55		60		ns	
Write command pulse width	^tWP	10		15		15		ns	
Write command to $\overline{RAS}$ lead time	^tRWL	15		20		20		ns	
Write command to $\overline{CAS}$ lead time	^tCWL	20		20		20		ns	
Data-in setup time	^tDS	0		0		0		ns	21
Data-in hold time	^tDH	10		15		15		ns	21
Data-in hold time (referenced to $\overline{RAS}$)	^tDHR	45		55		60		ns	
Transition time (rise or fall)	^tT	3	50	3	50	3	50	ns	9, 10
Refresh period (1,024 cycles)	^tREF		16/128		16/128		16/128	ms	7/26
$\overline{RAS}$ to $\overline{CAS}$ precharge time	^tRPC	0		0		0		ns	
$\overline{CAS}$ setup time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH)	^tCSR	10		10		10		ns	5
$\overline{CAS}$ hold time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH)	^tCHR	15		15		15		ns	5
$\overline{WE}$ setup time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH)	^tWRP	10		10		10		ns	25
$\overline{WE}$ hold time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH)	^tWRH	10		10		10		ns	25
$\overline{WE}$ setup time (WCBR test cycle)	^tWTS	10		10		10		ns	25
$\overline{WE}$ hold time (WCBR test cycle)	^tWTH	10		10		10		ns	25

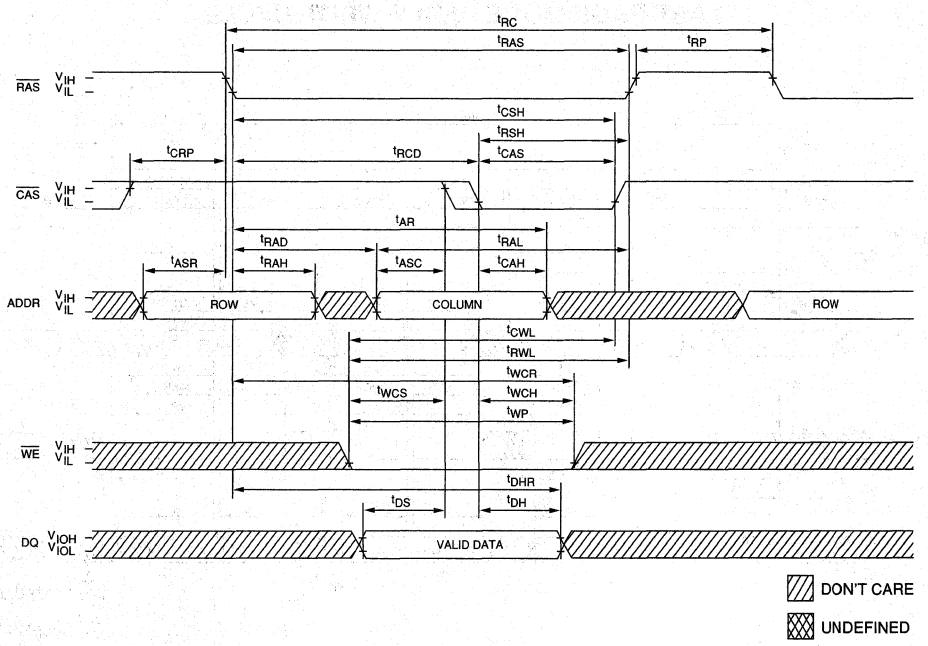
NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. Capacitance is measured using MIL-STD-883C, Method 3012.1 (1 MHz AC, Vcc = 5V, DC bias = 2.4V @ 15mV RMS).
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \leq T_A \leq 70°C$) is assured.
7. An initial pause of 100µs is required after power-up followed by any eight $\overline{RAS}$ refresh cycles ($\overline{RAS}$-ONLY or CBR with $\overline{WE}$ HIGH) before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-up should be repeated any time the ^tREF refresh requirement is exceeded.
8. AC characteristics assume ^tT = 5ns.
9. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS}$ = V_{IH}, data output is High-Z.
12. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to 2 TTL gates and 100pF.
14. Assumes that $^tRCD < {}^tRCD$ (MAX). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
15. Assumes that $^tRCD \geq {}^tRCD$ (MAX).
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer, $\overline{CAS}$ must be pulsed HIGH for ^tCPN.
17. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (MAX) limit, then access time is controlled exclusively by ^tCAC.
18. Operation within the ^tRAD (MAX) limit ensures that ^tRCD (MAX) can be met. ^tRAD (MAX) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (MAX) limit, then access time is controlled exclusively by ^tAA.
19. Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
20. ^tOFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
21. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY-WRITE cycles.
22. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW.
23. All other inputs equal Vcc -0.2V.
24. LATE-WRITE, READ-WRITE or READ-MODIFY-WRITE cycles are not available due to the common DQ configuration of U1-U8.
25. ^tWTS and ^tWTH are set up and hold specifications for the $\overline{WE}$ pin being held LOW to enable the JEDEC test mode (with CBR timing constraints). These two parameters are the inverts of ^tWRP and ^tWRH in the CBR refresh cycle.
26. Applies to L-version only.

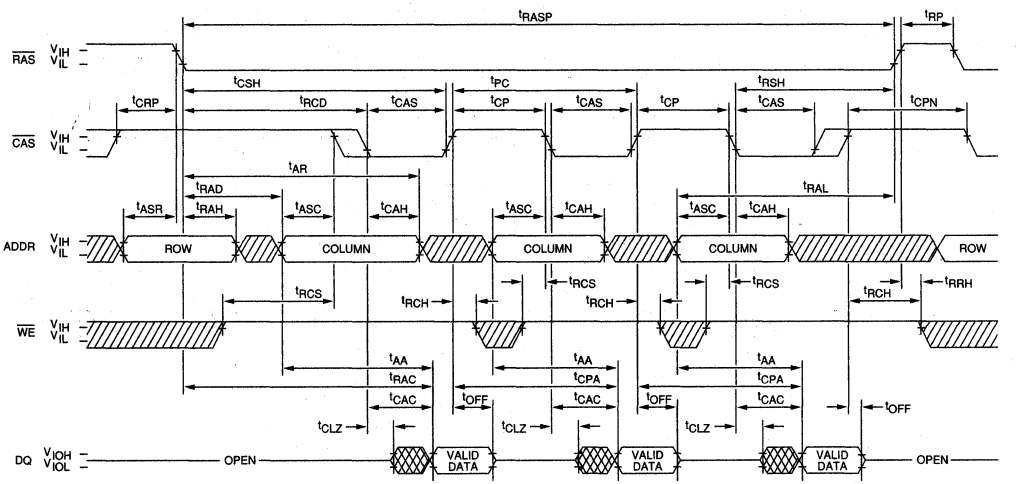
READ CYCLE



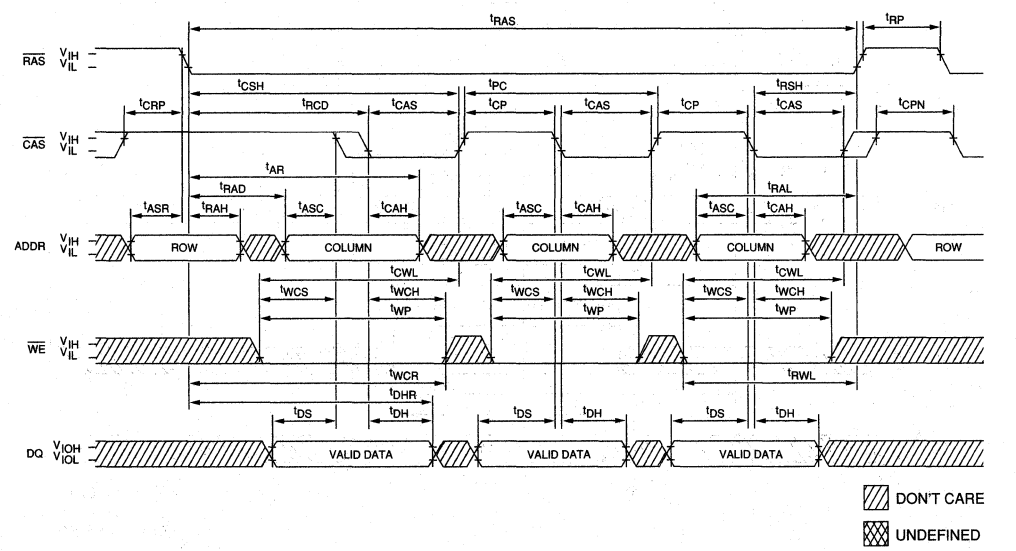
EARLY-WRITE CYCLE



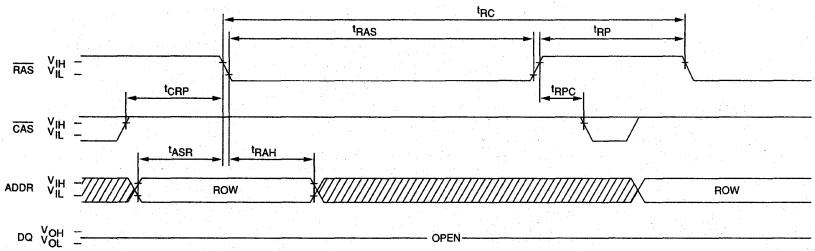
FAST-PAGE-MODE READ CYCLE



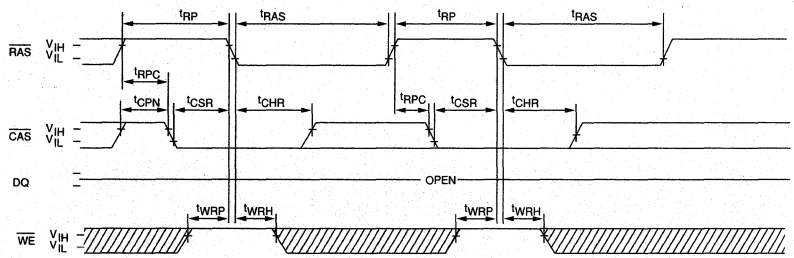
FAST-PAGE-MODE EARLY-WRITE CYCLE



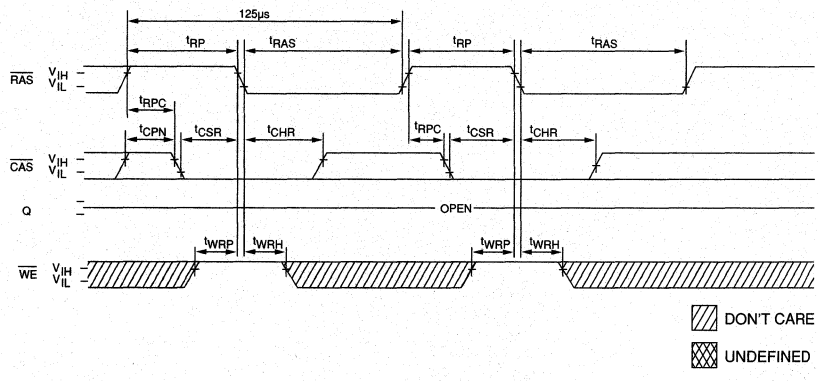
$\overline{\text{RAS}}$-ONLY REFRESH CYCLE
(ADDR = A0-A9; A10 and $\overline{\text{WE}}$ = DON'T CARE)



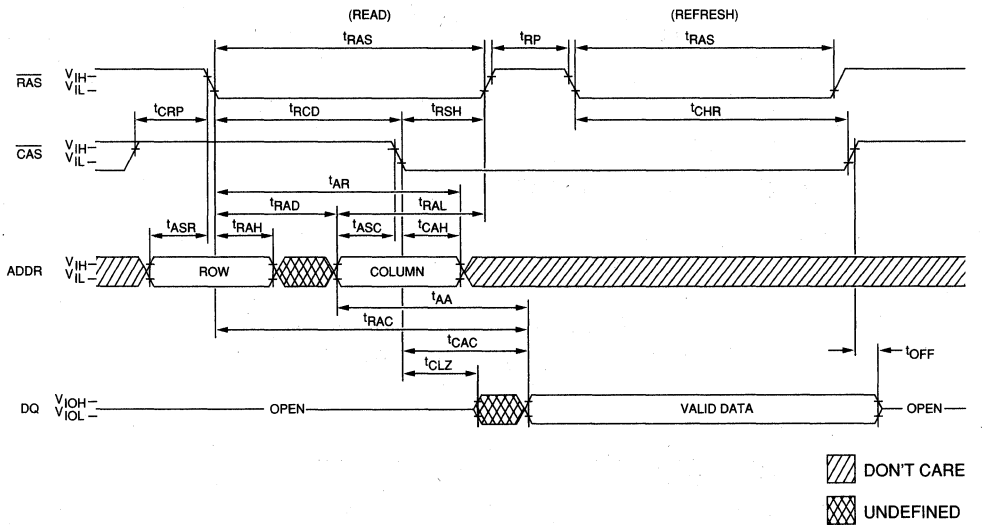
$\overline{\text{CAS}}$-BEFORE-$\overline{\text{RAS}}$ REFRESH CYCLE
(A0-A10 = DON'T CARE)



BATTERY BACKUP REFRESH CYCLE [26]
(A0-A10 = DON'T CARE)



HIDDEN REFRESH CYCLE [22]
($\overline{WE}$ = HIGH)



DRAM MODULE

16 MEG x 8 DRAM

FAST PAGE MODE

NEW DRAM MODULE

FEATURES

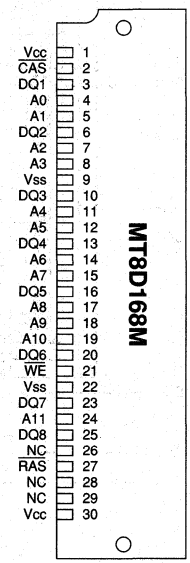
- Industry standard pinout in a 30-pin single-in-line package
- High-performance, CMOS silicon-gate process
- Single 5V ±10% power supply
- All device pins are fully TTL compatible
- Low power, 24mW standby; 2,200mW active, typical
- Refresh modes: RAS-ONLY, CAS-BEFORE-RAS (CBR) and HIDDEN
- 4,096-cycle refresh distributed across 64ms
- FAST PAGE MODE access cycle

OPTIONS	MARKING
Timing	
60ns access	-6
70ns access	-7
80ns access	-8
Packages	
Leadless 30-pin SIMM	M
Leaded 30-pin SIP	N

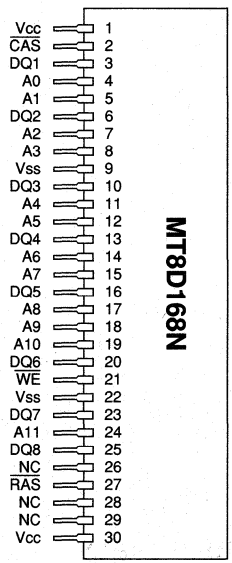
- Part Number Example: MT8D168M-6

PIN ASSIGNMENT (Top View)

30-Pin SIMM (T-6)



30-Pin SIP (S-6)



GENERAL DESCRIPTION

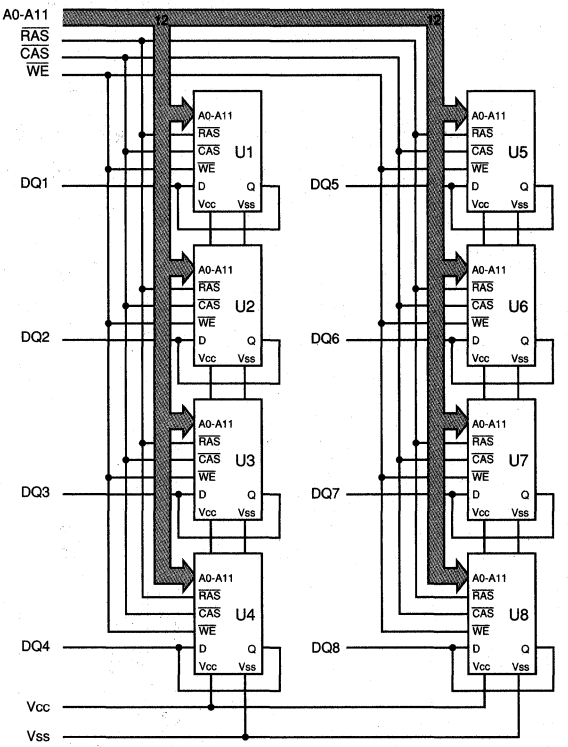
The MT8D168 is a randomly accessed solid-state memory containing 16,777,216 words organized in a x8 configuration. During READ or WRITE cycles, each bit is uniquely addressed through the 24 address bits which are entered 12 bits (A0-A11) at a time. RAS is used to latch the first 12 bits and CAS the latter 12 bits. READ or WRITE cycles are selected with the WE input. A logic HIGH on WE dictates READ mode, while a logic LOW on WE dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of CAS. Since WE goes LOW prior to CAS going LOW, the output pin(s) remain open (High-Z) until the next CAS cycle.

FAST PAGE MODE allows faster data operations (READ or WRITE) within a row-address (A0-A11) defined page boundary. The FAST PAGE MODE cycle is always initiated with a row address strobed-in by RAS followed by a column address strobed-in by CAS. CAS may be toggled-in by holding RAS LOW and strobing-in different column addresses, thus executing faster memory cycles. Returning RAS HIGH terminates the FAST PAGE MODE operation.

Returning RAS and CAS HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the RAS high time. Memory cell data is retained in its correct state by maintaining power and executing any RAS cycle (READ, WRITE, RAS-ONLY, CAS-BEFORE-RAS, or HIDDEN REFRESH) so that all 4,096 combinations of RAS addresses (A0-A11) are executed at least every 64ms, regardless of sequence. The CBR refresh cycle will invoke the refresh counter for automatic RAS addressing.

NEW DRAM MODULE

FUNCTIONAL BLOCK DIAGRAM



U1-U8 = MT4C16M1A1DJ

TRUTH TABLE

FUNCTION		RAS	CAS	WE	ADDRESSES tR	ADDRESSES tC	DATA IN/OUT DQ1-DQ8
Standby		H	H→X	X	X	X	High-Z
READ		L	L	H	ROW	COL	Data Out
EARLY-WRITE		L	L	L	ROW	COL	Data In
FAST-PAGE-MODE	1st Cycle	L	H→L	H	ROW	COL	Data Out
READ	2nd Cycle	L	H→L	H	n/a	COL	Data Out
FAST-PAGE-MODE	1st Cycle	L	H→L	L	ROW	COL	Data In
WRITE	2nd Cycle	L	H→L	L	n/a	COL	Data In
RAS-ONLY REFRESH		L	H	X	ROW	n/a	High-Z
HIDDEN	READ	L→H→L	L	H	ROW	COL	Data Out
REFRESH	WRITE	L→H→L	L	L	ROW	COL	Data In
CAS-BEFORE-RAS REFRESH		H→L	L	H	X	X	High-Z

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} ..... -1V to +7V
Operating Temperature, T_A (Ambient) ..... 0°C to +70°C
Storage Temperature (Plastic) ..... -55°C to +125°C
Power Dissipation 8W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 3, 4, 6, 7) (0°C ≤ T_A ≤ 70°C; V_{CC} = 5V ±10%)

PARAMETER/CONDITION		SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage		V_{CC}	4.5	5.5	V	1
Input High (Logic 1) Voltage, All Inputs		V_{IH}	2.4	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, All Inputs		V_{IL}	-1.0	0.8	V	1
INPUT LEAKAGE CURRENT Any Input: 0V ≤ V_{IN} ≤ 6.5V (All other pins not under test = 0V)	A0-A11, $\overline{WE}$, $\overline{CAS}$, $\overline{RAS}$	I_I	-16	16	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled, 0V ≤ V_{OUT} ≤ 5.5V)	DQ1-DQ8	I_{OZ}	-10	10	µA	
OUTPUT LEVELS Output High Voltage (I_{OUT} = -5mA)		V_{OH}	2.4		V	
Output Low Voltage (I_{OUT} = 4.2mA)		V_{OL}		0.4	V	

		MAX				
PARAMETER/CONDITION	SYMBOL	-6	-7	-8	UNITS	NOTES
STANDBY CURRENT (TTL) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC1}	16	16	16	mA	
STANDBY CURRENT (CMOS) ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} -0.2V)	I_{CC2}	8	8	8	mA	
OPERATING CURRENT: Random READ/WRITE Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC (MIN))	I_{CC3}	720	640	560	mA	3, 4
OPERATING CURRENT: FAST PAGE MODE Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: ^tPC = ^tPC (MIN))	I_{CC4}	560	480	400	mA	3, 4
REFRESH CURRENT: $\overline{RAS}$-ONLY Average power supply current ($\overline{RAS}$ Cycling, $\overline{CAS}$=V_{IH}: ^tRC = ^tRC (MIN))	I_{CC5}	720	640	560	mA	3
REFRESH CURRENT: $\overline{CAS}$-BEFORE-$\overline{RAS}$ Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC (MIN))	I_{CC6}	720	640	560	mA	3

NEW DRAM MODULE

CAPACITANCE

DESCRIPTION	SYMBOL	MAX	UNITS	NOTES
Input Capacitance: A0-A11	C_{I1}	51	pF	2
Input Capacitance: $\overline{RAS}$, $\overline{WE}$, $\overline{CAS}$	C_{I2}	67	pF	2
Input/Output Capacitance: DQ1-DQ8	C_{IO}	15	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (V_{CC} = 5V ±10%)

AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	tRC	110		130		150		ns	
READ-WRITE cycle time	tRWC	n/a		n/a		n/a		ns	22
FAST-PAGE-MODE READ or WRITE cycle time	tPC	40		45		50		ns	
FAST-PAGE-MODE READ-WRITE cycle time	tPRWC	n/a		n/a		n/a		ns	22
Access time from $\overline{RAS}$	tRAC		60		70		80	ns	14
Access time from $\overline{CAS}$	tCAC		15		20		20	ns	15
Access time from column address	tAA		30		35		40	ns	
Access time from $\overline{CAS}$ precharge	tCPA		35		40		45	ns	
$\overline{RAS}$ pulse width	tRAS	60	100,000	70	100,000	80	100,000	ns	
$\overline{RAS}$ pulse width (FAST PAGE MODE)	tRASP	60	100,000	70	100,000	80	100,000	ns	
$\overline{RAS}$ hold time	tRSH	15		20		20		ns	
$\overline{RAS}$ precharge time	tRP	40		50		60		ns	
$\overline{CAS}$ pulse width	tCAS	15	100,000	20	100,000	20	100,000	ns	
$\overline{CAS}$ hold time	tCSH	60		70		80		ns	
$\overline{CAS}$ precharge time	tCPN	10		10		10		ns	16
$\overline{CAS}$ precharge time (FAST PAGE MODE)	tCP	10		10		10		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	tRCD	20	45	20	50	20	60	ns	17
$\overline{CAS}$ to $\overline{RAS}$ precharge time	tCRP	5		5		5		ns	
Row address setup time	tASR	0		0		0		ns	
Row address hold time	tRAH	10		10		10		ns	
$\overline{RAS}$ to column address delay time	tRAD	15	30	15	35	15	40	ns	18
Column address setup time	tASC	0		0		0		ns	
Column address hold time	tCAH	10		15		15		ns	
Column address hold time (referenced to $\overline{RAS}$)	tAR	50		55		60		ns	
Column address to $\overline{RAS}$ lead time	tRAL	30		35		40		ns	
Read command setup time	tRCS	0		0		0		ns	
Read command hold time (referenced to $\overline{CAS}$)	tRCH	0		0		0		ns	19
Read command hold time (referenced to $\overline{RAS}$)	tRRH	0		0		0		ns	19
$\overline{CAS}$ to output in Low-Z	tCLZ	0		0		0		ns	
Output buffer turn-off delay	tOFF	0	15	0	15	0	15	ns	20
$\overline{WE}$ command setup time	tWCS	0		0		0		ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

Notes: 6, 7, 8, 9, 10, 11, 12, 13) (V_{CC} = 5V ±10%)

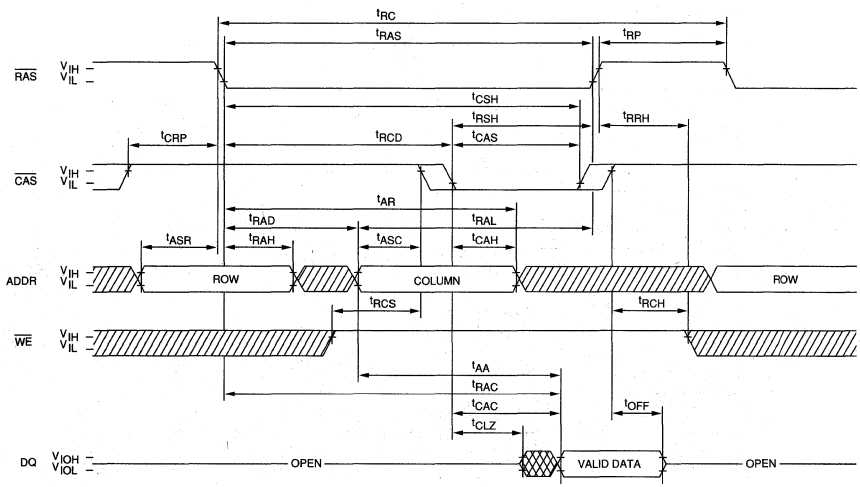
AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Write command hold time	^tWCH	10		15		15		ns	
Write command hold time (referenced to $\overline{RAS}$)	^tWCR	45		55		60		ns	
Write command pulse width	^tWP	10		15		15		ns	
Write command to $\overline{RAS}$ lead time	^tRWL	15		20		20		ns	
Write command to $\overline{CAS}$ lead time	^tCWL	15		20		20		ns	
Data-in setup time	^tDS	0		0		0		ns	21
Data-in hold time	^tDH	10		15		15		ns	21
Data-in hold time (referenced to $\overline{RAS}$)	^tDHR	45		55		60		ns	
Transition time (rise or fall)	^tT	3	50	3	50	3	50	ns	9, 10
Refresh period (4,096 cycles)	^tREF		64		64		64	ms	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	^tRPC	0		0		0		ns	
$\overline{CAS}$ setup time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tCSR	5		5		5		ns	5
$\overline{CAS}$ hold time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tCHR	15		15		15		ns	5
$\overline{WE}$ hold time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tWRH	10		10		10		ns	24
$\overline{WE}$ setup time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tWRP	10		10		10		ns	24
$\overline{WE}$ hold time (WCBR test cycle)	^tWTH	10		10		10		ns	24
$\overline{WE}$ setup time (WCBR test cycle)	^tWTS	10		10		10		ns	24

NEW DRAM MODULE

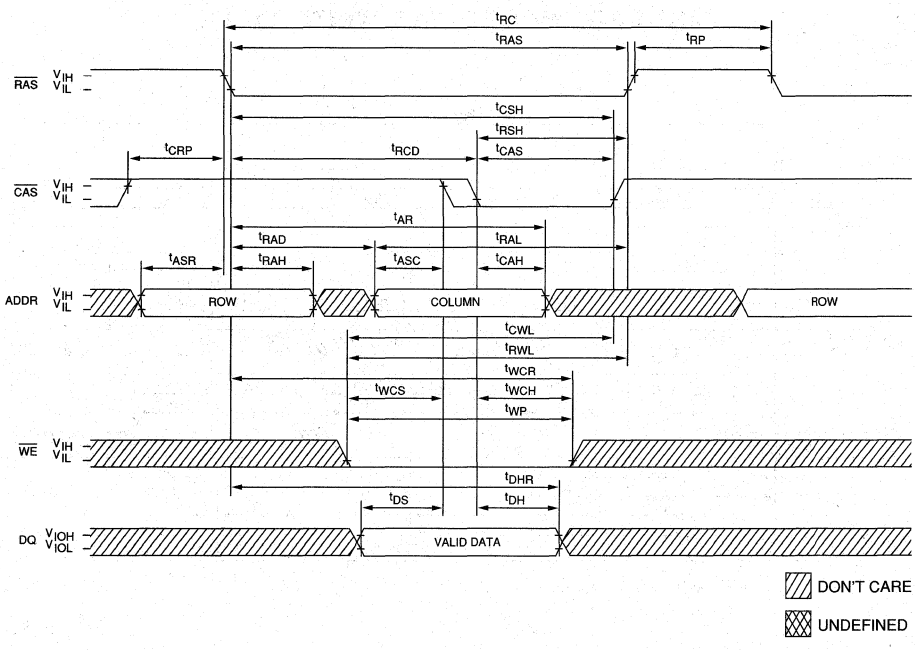
NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. Capacitance is measured using MIL-STD-883C, Method 3012.1 (1 MHz AC, Vcc = 5V, DC bias = 2.4V @ 15mV RMS).
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is assured.
7. An initial pause of 100µs is required after power-up followed by eight $\overline{RAS}$ refresh cycles ($\overline{RAS}$-ONLY or CBR with $\overline{WE}$ HIGH) before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-up should be repeated any time the ^{t}REF refresh requirement is exceeded.
8. AC characteristics assume ^{t}T = 5ns.
9. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS}$ = V_{IH}, data output is High-Z.
12. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to 2 TTL gates and 100pF.
14. Assumes that $^{t}RCD < {}^{t}RCD$ (MAX). If ^{t}RCD is greater than the maximum recommended value shown in this table, ^{t}RAC will increase by the amount that ^{t}RCD exceeds the value shown.
15. Assumes that $^{t}RCD \geq {}^{t}RCD$ (MAX).
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer, $\overline{CAS}$ must be pulsed HIGH for ^{t}CPN.
17. Operation within the ^{t}RCD (MAX) limit ensures that ^{t}RAC (MAX) can be met. ^{t}RCD (MAX) is specified as a reference point only; if ^{t}RCD is greater than the specified ^{t}RCD (MAX) limit, then access time is controlled exclusively by ^{t}CAC.
18. Operation within the ^{t}RAD (MAX) limit ensures that ^{t}RCD (MAX) can be met. ^{t}RAD (MAX) is specified as a reference point only; if ^{t}RAD is greater than the specified ^{t}RAD (MAX) limit, then access time is controlled exclusively by ^{t}AA.
19. Either ^{t}RCH or ^{t}RRH must be satisfied for a READ cycle.
20. ^{t}OFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
21. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY-WRITE cycles.
22. LATE-WRITE, READ-WRITE or READ-MODIFY-WRITE cycles are not available due to the common DQ configuration of U1-U8.
23. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW and $\overline{OE}$ = HIGH.
24. ^{t}WTS and ^{t}WTH are setup and hold specifications for the $\overline{WE}$ pin being held LOW to enable the JEDEC test mode (with CBR timing constraints). ^{t}WRP and ^{t}WRH are setup and hold specifications for the $\overline{WE}$ pin being held HIGH to enable the CBR refresh cycle.

READ CYCLE

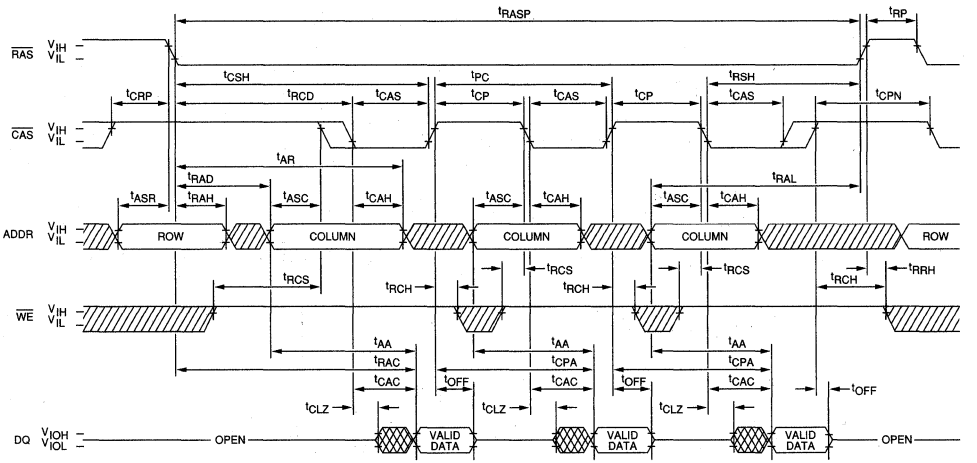


EARLY-WRITE CYCLE

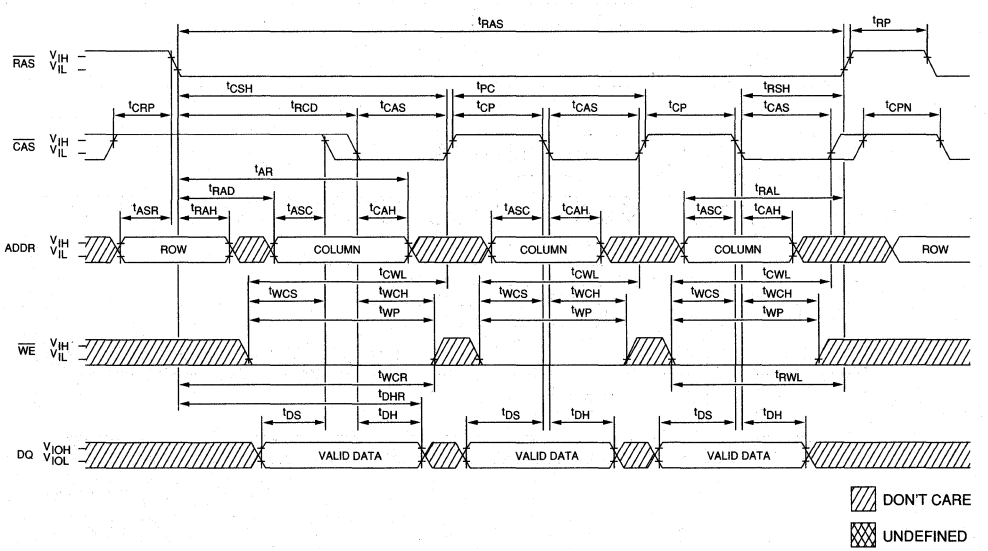


NEW ■ DRAM MODULE

FAST-PAGE-MODE READ CYCLE

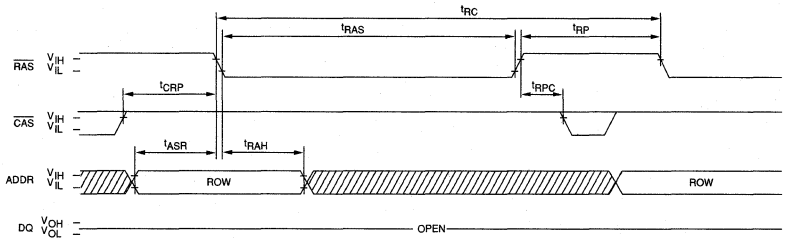


FAST-PAGE-MODE EARLY-WRITE CYCLE



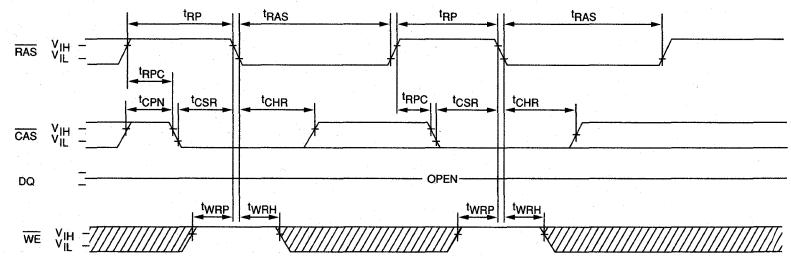
$\overline{RAS}$-ONLY REFRESH CYCLE

(ADDR = A0-A10; A11 and $\overline{WE}$ = DON'T CARE)



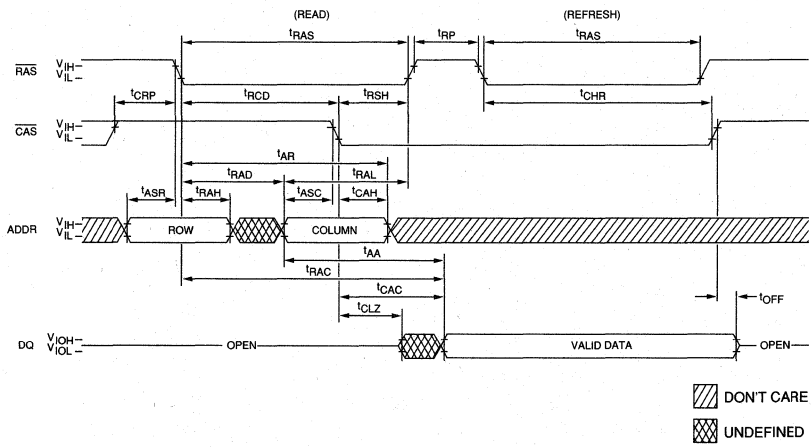
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

(A0-A11 = DON'T CARE)



HIDDEN REFRESH CYCLE [23]

($\overline{WE}$ = HIGH)



MICRON TECHNOLOGY, INC.

MT8D168
16 MEG x 8 DRAM MODULE

DRAM MODULE

256K x 9 DRAM

FAST PAGE MODE (MT3D2569)
LOW POWER,
EXTENDED REFRESH (MT3D2569 L)

FEATURES

- Industry standard pinout in a 30-pin single-in-line memory module
- High-performance, CMOS silicon-gate process
- Single 5V ±10% power supply
- Low power, 9mW (.9mW L-version) standby; 625mW active, typical
- All device pins are fully TTL compatible
- FAST PAGE MODE access cycle
- Refresh modes: $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$ (CBR) and HIDDEN
- 512-cycle refresh distributed across 8ms or 512-cycle extended refresh distributed across 64ms
- Low CMOS standby current, 60µA maximum (L-version)

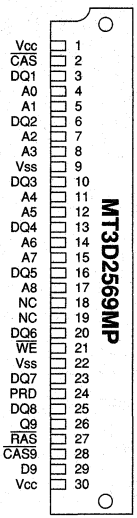
OPTIONS / MARKING

• Timing	
60ns access	-6
70ns access	-7
80ns access	-8
• Packages	
Leadless 30-pin SIMM	M
Leaded 30-pin SIP	N
• Access Mode	
FAST PAGE MODE	P
• Power/Refresh	
Normal Power/8ms	Blank
Low Power/64ms	L

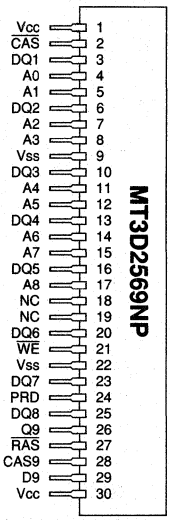
- Part Number Example: MT3D2569MPL-6

PIN ASSIGNMENT (Top View)

30-Pin SIMM (T-2)



30-Pin SIP (S-2)



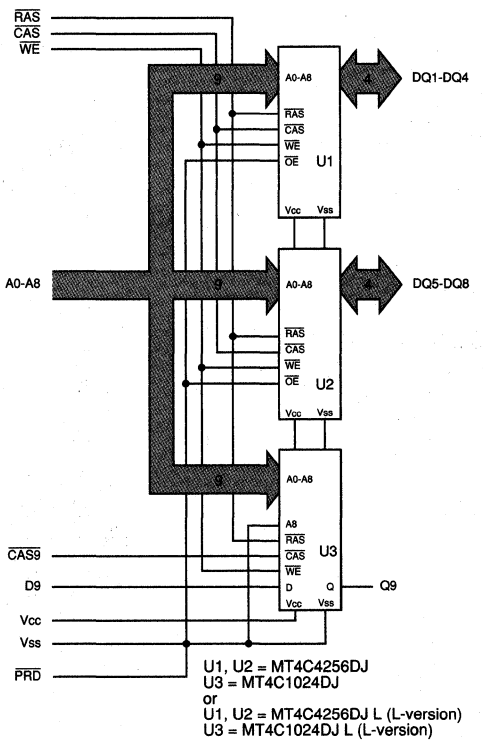
GENERAL DESCRIPTION

The MT3D2569 is a randomly accessed solid-state memory containing 262,144 words organized in a x9 configuration. During READ or WRITE cycles, each word is uniquely addressed through the 18 address bits, which are entered nine bits (A0-A8) at a time. $\overline{RAS}$ is used to latch the first nine bits and $\overline{CAS}$ the latter nine bits. READ or WRITE cycles are selected with the $\overline{WE}$ input. A logic HIGH on $\overline{WE}$ dictates READ mode while a logic LOW on $\overline{WE}$ dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. EARLY-WRITE occurs when $\overline{WE}$ goes LOW prior to $\overline{CAS}$ going LOW, and the output pins remain open (High-Z) until the next $\overline{CAS}$ cycle.

FAST PAGE MODE operations allow faster data operations (READ or WRITE) within a row address (A0-A8) defined page boundary. The FAST PAGE MODE cycle is always initiated with a row address strobed-in by $\overline{RAS}$ followed by a column address strobed-in by $\overline{CAS}$. $\overline{CAS}$ may be toggled-in by holding $\overline{RAS}$ LOW and strobing-in different column addresses, thus executing faster memory cycles.

Returning $\overline{RAS}$ and $\overline{CAS}$ HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the $\overline{RAS}$ high time. Memory cell data is retained in its correct state by maintaining power and executing any $\overline{RAS}$ cycle (READ, WRITE, $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$ or HIDDEN REFRESH) so that all 512 combinations of $\overline{RAS}$ addresses (A0-A8) are executed at least every 8ms (64ms on L-version), regardless of sequence.

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

FUNCTION		RAS	CAS	CAS9	WE	ADDRESSES		DATA IN/OUT
						^tR	^tC	DQ1-DQ8, D9, Q9
Standby		H	H→X	H→X	X	X	X	High-Z
READ		L	L	L	H	ROW	COL	Data Out
EARLY-WRITE		L	L	L	L	ROW	COL	Data In
FAST-PAGE-MODE	1st Cycle	L	H→L	H→L	H	ROW	COL	Data Out
READ	2nd Cycle	L	H→L	H→L	H	n/a	COL	Data Out
FAST-PAGE-MODE	1st Cycle	L	H→L	H→L	L	ROW	COL	Data In
WRITE	2nd Cycle	L	H→L	H→L	L	n/a	COL	Data In
RAS-ONLY REFRESH		L	H	H	X	ROW	n/a	High-Z
HIDDEN	READ	L→H→L	L	L	H	ROW	COL	Data Out
REFRESH	WRITE	L→H→L	L	L	L	ROW	COL	Data In
CAS-BEFORE-RAS REFRESH		H→L	L	L	X	X	X	High-Z
BATTERY BACKUP REFRESH (L-version)		H→L	L	L	X	X	X	High-Z

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} ..... -1V to +7V
Operating Temperature, T_A (Ambient) ..... 0°C to +70°C
Storage Temperature ..... -55°C to +125°C
Power Dissipation 3W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 2, 3, 6, 22) (0°C ≤ T_A ≤ 70°C; V_{CC} = 5V ±10%)

PARAMETER/CONDITION		SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage		V_{CC}	4.5	5.5	V	1
Input High (Logic 1) Voltage, All Inputs		V_{IH}	2.4	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, All Inputs		V_{IL}	-1.0	0.8	V	1
INPUT LEAKAGE Any Input 0V ≤ V_{IN} ≤ V_{CC}, (All other pins not under test = 0V)	D9, $\overline{CAS9}$	I_I	-2	2	µA	
	A0-A8, $\overline{RAS}$, $\overline{WE}$	I_I	-6	6	µA	
OUTPUT LEAKAGE (Q is disabled, 0V ≤ V_{OUT} ≤ V_{CC})	DQ1-DQ8, Q9	I_{OZ}	-10	10	µA	
OUTPUT LEVELS Output High (Logic 1) Voltage (I_{OUT} = -5mA)		V_{OH}	2.4		V	
Output Low (Logic 0) Voltage (I_{OUT} = 5mA)		V_{OL}		0.4	V	

PARAMETER/CONDITION	SYMBOL	MAX -6	MAX -7	MAX -8	UNITS	NOTES
STANDBY CURRENT: (TTL) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC1}	6	6	6	mA	
STANDBY CURRENT: (CMOS)	I_{CC2}	3	3	3	mA	24
($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} -0.2V)		.6	.6	.6	mA	24, 26
OPERATING CURRENT: Random READ/WRITE Average power supply current	I_{CC3}	270	240	210	mA	2, 22
($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC (MIN))		255	225	195	mA	2,22,26
OPERATING CURRENT: FAST PAGE MODE Average power supply current	I_{CC4}	210	180	150	mA	2, 22
($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: ^tPC = ^tPC (MIN))		195	165	135	mA	2,22,26
REFRESH CURRENT: $\overline{RAS}$-ONLY Average power supply current	I_{CC5}	270	240	210	mA	2
($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}: ^tRC = ^tRC (MIN))		255	225	195	mA	2, 26
REFRESH CURRENT: $\overline{CAS}$-BEFORE-$\overline{RAS}$ Average power supply current	I_{CC6}	270	240	210	mA	2, 19
($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC (MIN))		255	225	195	mA	2,19,26
REFRESH CURRENT: BATTERY BACKUP (BBU) Average power supply current during BATTERY BACKUP refresh: $\overline{CAS}$ = 0.2V or $\overline{CAS}$-BEFORE-$\overline{RAS}$ cycling; $\overline{RAS}$ = ^tRAS (MIN) to 1µs; $\overline{WE}$, A0-A9 and D_{IN} = Vcc -0.2V or 0.2V (D_{IN} may be left OPEN), ^tRC = 125µs (512 rows at 125µs = 64ms)	I_{CC7}	.6	.6	.6	mA	26

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A8	C_{I1}		19	pF	17
Input Capacitance: $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	C_{I2}		25	pF	17
Input Capacitance: D9	C_{I3}		10	pF	17
Input/Output Capacitance: DQ1-DQ8	C_{IO}		15	pF	17
Output Capacitance: Q9	C_O		10	pF	17

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 3, 4, 5, 6, 7, 10, 11, 16, 21) ($0°C \le T_A \le +70°C$; V_{CC} = 5V ±10%)

AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	^tRC	110		130		150		ns	
READ-WRITE cycle time	^tRWC	n/a		n/a		n/a		n/a	21
FAST-PAGE-MODE READ or WRITE cycle time	^tPC	40		40		45		ns	
PAGE-MODE READ or WRITE cycle time	^tPC	n/a		n/a		n/a		ns	
Access time from $\overline{RAS}$	^tRAC		60		70		80	ns	8
Access time from $\overline{CAS}$ (FAST PAGE MODE)	^tCAC		20		20		20	ns	9
Output Enable	^tOE		20		20		20	ns	
Access time from column address	^tAA		30		35		40	ns	
Access time from $\overline{CAS}$ precharge	^tCPA		35		40		45	ns	
$\overline{RAS}$ pulse width	^tRAS	60	100,000	70	100,000	80	100,000	ns	
$\overline{RAS}$ pulse width (FAST PAGE MODE)	^tRASP	60	100,000	70	100,000	80	100,000	ns	
$\overline{RAS}$ hold time	^tRSH	20		20		20		ns	
$\overline{RAS}$ precharge time	^tRP	40		50		60		ns	
$\overline{CAS}$ pulse width	^tCAS	20	100,000	20	100,000	20	100,000	ns	
$\overline{CAS}$ hold time	^tCSH	60		70		80		ns	
$\overline{CAS}$ precharge time	^tCPN	10		10		10		ns	18
$\overline{CAS}$ precharge time (FAST PAGE MODE)	^tCP	10		10		10		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	^tRCD	20	40	20	50	20	60	ns	13
$\overline{CAS}$ to $\overline{RAS}$ precharge time	^tCRP	5		5		5		ns	
Row address setup time	^tASR	0		0		0		ns	
Row address hold time	^tRAH	10		10		10		ns	
$\overline{RAS}$ to column address delay time	^tRAD	15	30	15	35	15	40	ns	24
Column address setup time	^tASC	0		0		0		ns	
Column address hold time	^tCAH	15		15		15		ns	
Column address hold time (referenced to $\overline{RAS}$)	^tAR	45		55		60		ns	
Column address to $\overline{RAS}$ lead time	^tRAL	30		35		40		ns	
Read command setup time	^tRCS	0		0		0		ns	
Read command hold time (referenced to $\overline{CAS}$)	^tRCH	0		0		0		ns	25
Read command hold time (referenced to $\overline{RAS}$)	^tRRH	0		0		0		ns	25

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

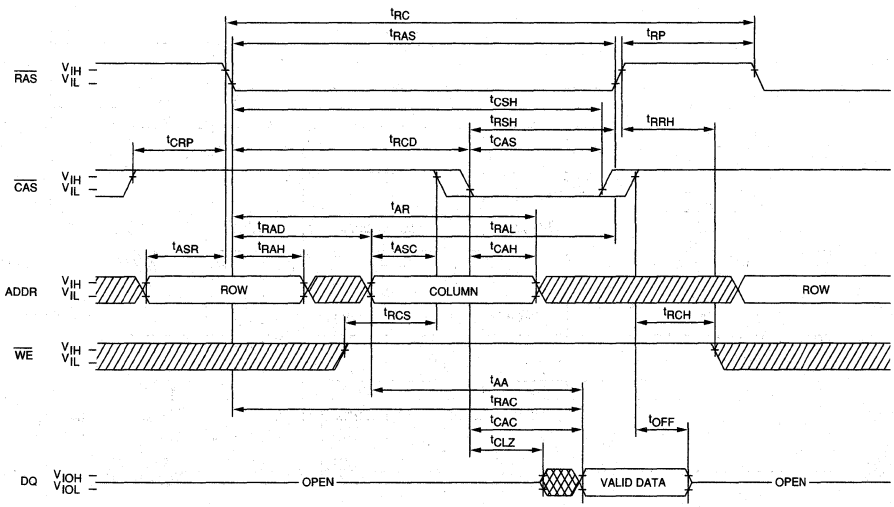
(Notes: 3, 4, 5, 6, 7, 10, 11, 16, 21) (0°C ≤ T_A ≤ +70°C; Vcc = 5V ±10%)

AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
$\overline{CAS}$ to output in Low-Z	^tCLZ	0		0		0		ns	
Output buffer turn-off delay	^tOFF	0	20	0	20	0	20	ns	12
$\overline{WE}$ command setup time	^tWCS	0		0		0		ns	
Write command hold time	^tWCH	10		15		15		ns	
Write command hold time (referenced to $\overline{RAS}$)	^tWCR	45		55		60		ns	
Write command pulse width	^tWP	10		15		15		ns	
Write command to $\overline{RAS}$ lead time	^tRWL	20		20		20		ns	
Write command to $\overline{CAS}$ lead time	^tCWL	20		20		20		ns	
Data-in setup time	^tDS	0		0		0		ns	15
Data-in hold time	^tDH	15		15		15		ns	15
Data-in hold time (referenced to $\overline{RAS}$)	^tDHR	45		55		60		ns	
Transition time (rise or fall)	^tT	3	50	3	50	3	50	ns	5, 16
Refresh period (512 cycles)	^tREF		8/64		8/64		8/64	ms	3/26
$\overline{RAS}$ to $\overline{CAS}$ precharge time	^tRPC	0		0		0		ns	
$\overline{CAS}$ setup time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH)	^tCSR	10		10		10		ns	19
$\overline{CAS}$ hold time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH)	^tCHR	10		15		15		ns	19

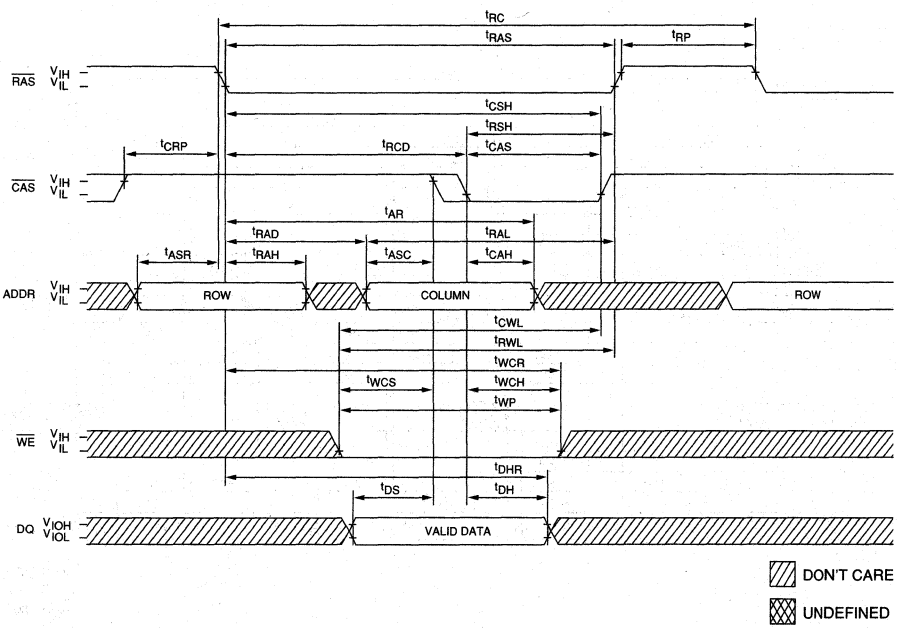
NOTES

1. All voltages referenced to V_{SS}.
2. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
3. An initial pause of 100µs is required after power-up followed by any eight $\overline{RAS}$ cycles before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-up should be repeated any time the ^{t}REF refresh requirement is exceeded.
4. AC characteristics assume ^{t}T = 5ns.
5. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \le T_A \le 70°C$) is assured.
7. Measured with a load equivalent to two TTL gates and 100pF.
8. Assumes that $^{t}RCD < ^{t}RCD$ (MAX). If ^{t}RCD is greater than the maximum recommended value shown in this table, ^{t}RAC will increase by the amount that ^{t}RCD exceeds the value shown.
9. Assumes that $^{t}RCD \ge ^{t}RCD$ (MAX).
10. If $\overline{CAS}$ = V_{IH}, data output is High-Z.
11. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
12. ^{t}OFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
13. Operation within the ^{t}RCD (MAX) limit ensures that ^{t}RAC (MAX) can be met. ^{t}RCD (MAX) is specified as a reference point only; if ^{t}RCD is greater than the specified ^{t}RCD (MAX) limit, then access time is controlled exclusively by ^{t}CAC.
14. ^{t}RCH is referenced to the first rising edge of $\overline{RAS}$ or $\overline{CAS}$.
15. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY-WRITE cycles.
16. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
17. This parameter is sampled. Capacitance is measured using MIL-STD-883C, Method 3012.1 (1 MHz AC, Vcc = 5V, DC bias = 2.4V @ 15mV RMS).
18. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, data-out (Q) will be maintained from the previous cycle. To initiate a new cycle and clear the Q buffer, $\overline{CAS}$ must be pulsed HIGH for ^{t}CP.
19. On-chip refresh and address counters are enabled.
20. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW.
21. LATE-WRITE, READ-WRITE or READ-MODIFY-WRITE cycles are not available due to $\overline{OE}$ being grounded on U1 andU2.
22. I_{CC} is dependent on cycle rates.
23. All other inputs at V_{CC} -0.2V.
24. Operation within the ^{t}RAD (MAX) limit ensures that ^{t}RCD (MAX) can be met. ^{t}RAD (MAX) is specified as a reference point only; if ^{t}RAD is greater than the specified ^{t}RAD (MAX) limit, then access time is controlled exclusively by ^{t}AA.
25. Either ^{t}RCH or ^{t}RRH must be satisfied for a READ cycle.
26. Applies to L-version only.

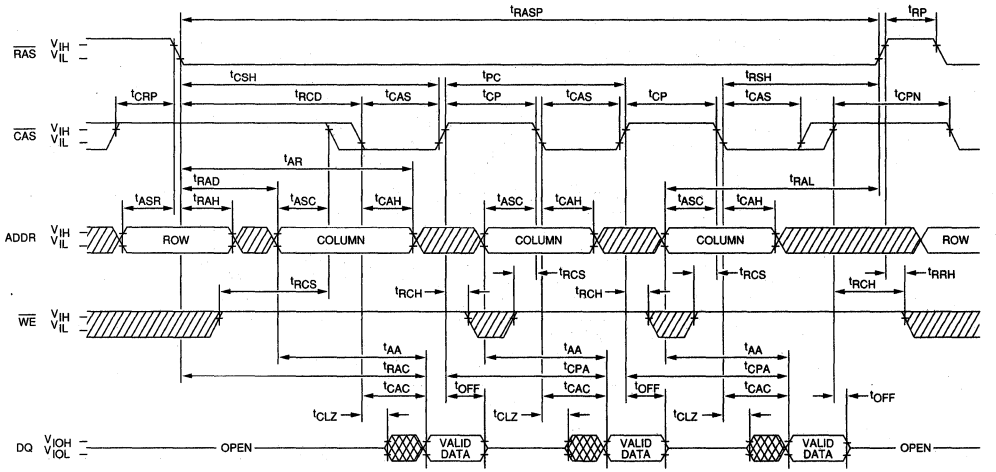
READ CYCLE



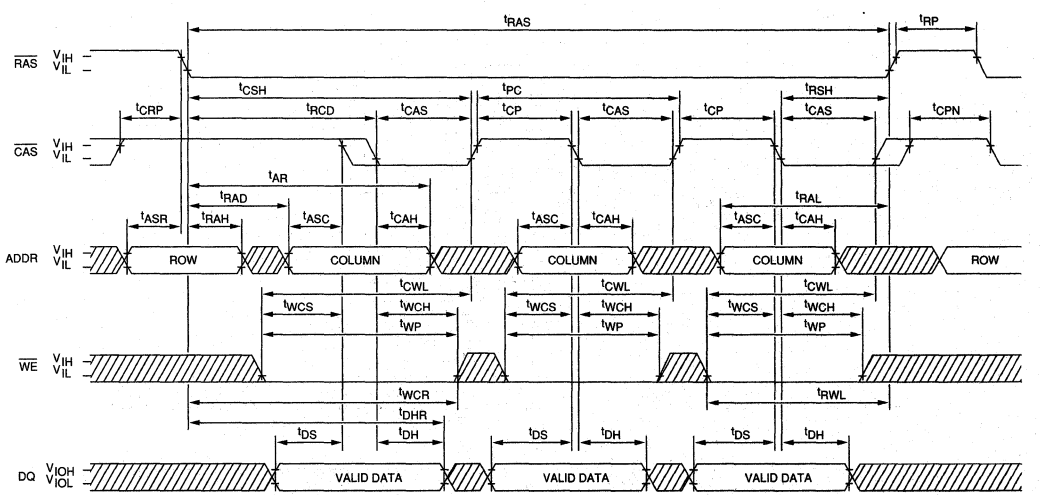
EARLY-WRITE CYCLE



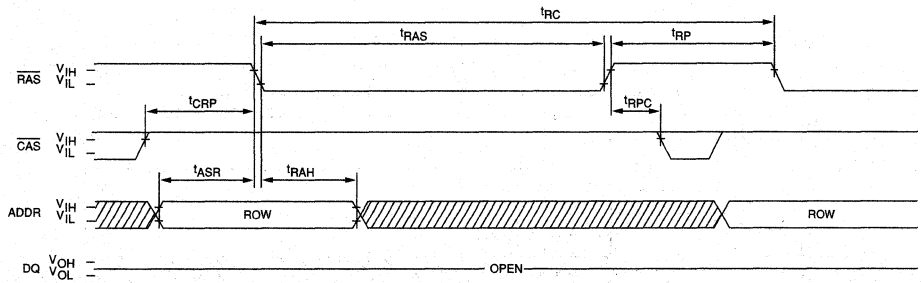
FAST-PAGE-MODE READ CYCLE



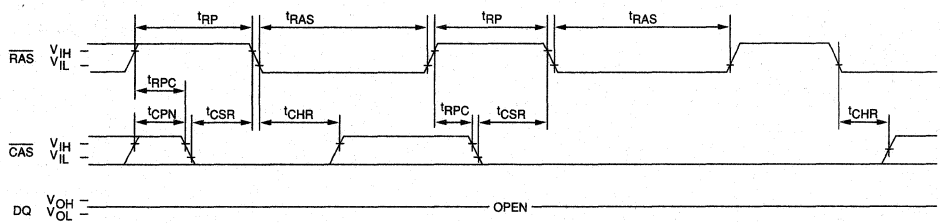
FAST-PAGE-MODE EARLY-WRITE CYCLE



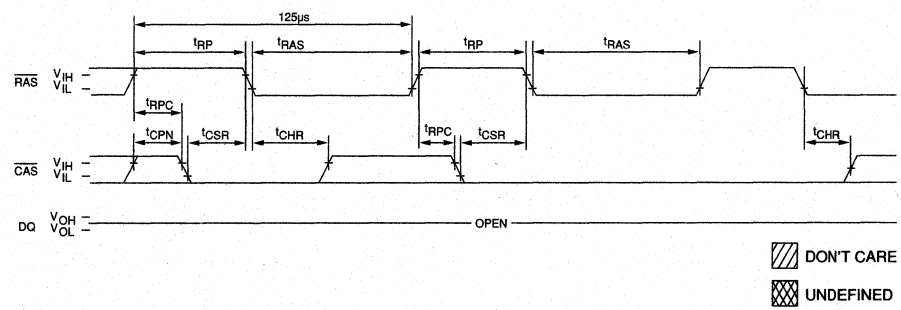
RAS-ONLY REFRESH CYCLE
(ADDR = A0-A8; WE = DON'T CARE)



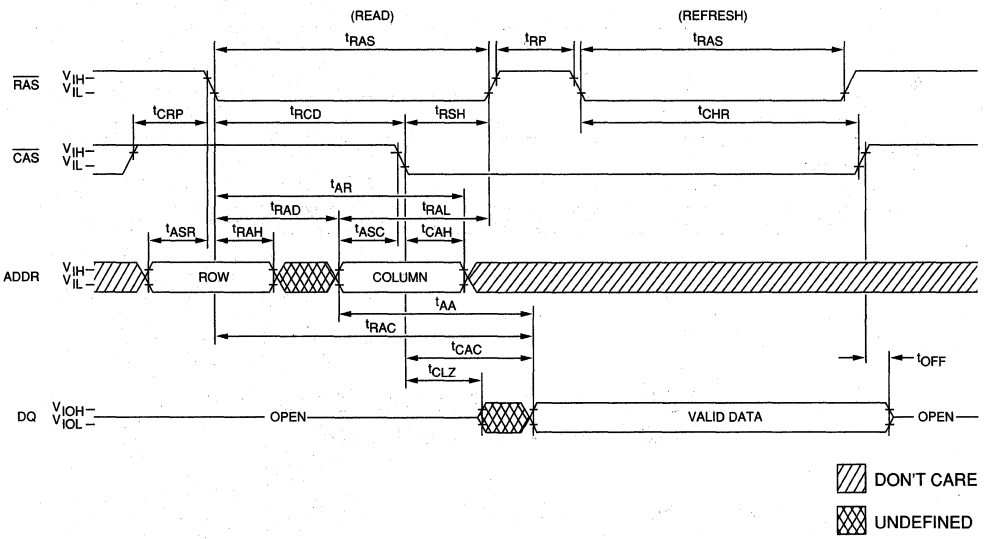
CAS-BEFORE-RAS REFRESH CYCLE
(A0-A8 and WE = DON'T CARE)



BATTERY BACKUP REFRESH CYCLE [26]
(A0-A8 and WE = DON'T CARE)



HIDDEN REFRESH CYCLE [20]
($\overline{WE}$ = HIGH)



DRAM MODULE

1 MEG x 9 DRAM

FAST PAGE MODE (MT3D19)
LOW POWER,
EXTENDED REFRESH (MT3D19 L)

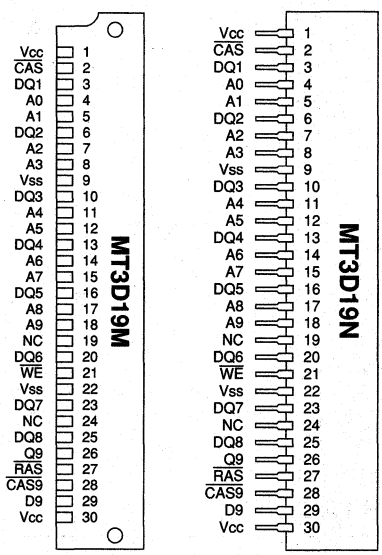
FEATURES

- Industry standard pinout in a 30-pin single-in-line memory module
- High-performance, CMOS silicon-gate process
- Single 5V ±10% power supply
- Low power, 9mW (3mW L-version) standby; 625mW active, typical
- All device pins are fully TTL compatible
- FAST PAGE MODE access cycle
- Refresh modes: $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$ (CBR) and HIDDEN
- Low profile
- 1,024-cycle refresh distributed across 16ms or 1,024-cycle extended refresh distributed across 128ms
- Low CMOS standby current, 600µA maximum (L-version)

OPTIONS MARKING

- Timing
  - 60ns access - 6
  - 70ns access - 7
  - 80ns access - 8
- Packages
  - Leadless 30-pin SIMM M
  - Leaded 30-pin SIP N
- Power/Refresh
  - Normal Power/16ms Blank
  - Low Power/128ms L
- Part Number Example: MT3D19ML-6

PIN ASSIGNMENT (Top View)



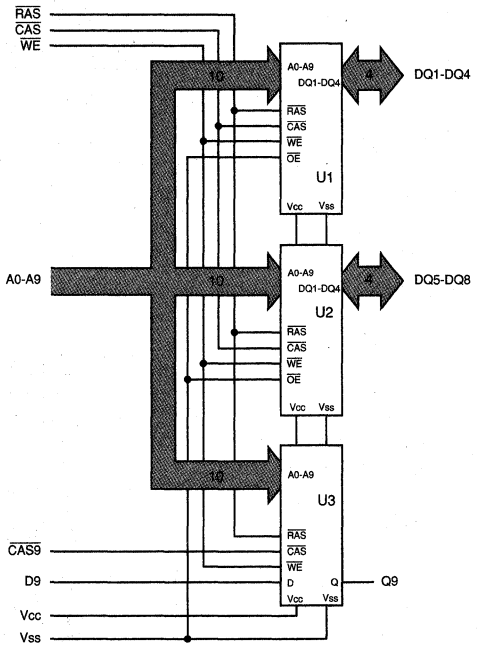
GENERAL DESCRIPTION

The MT3D19 is a randomly accessed solid-state memory containing 1,048,576 words organized in a x9 configuration. During READ or WRITE cycles, each word is uniquely addressed through 20 address bits, which are entered 10 bits (A0-A9) at a time. $\overline{RAS}$ is used to latch the first 10 bits and $\overline{CAS}$ the latter 10 bits. READ or WRITE cycles are selected with the $\overline{WE}$ input. A logic HIGH on $\overline{WE}$ dictates READ mode while a logic LOW on $\overline{WE}$ dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. EARLY WRITE occurs when $\overline{WE}$ goes LOW prior to $\overline{CAS}$ going LOW, and the output pins remain open (High-Z) until the next $\overline{CAS}$ cycle.

FAST PAGE MODE operations allow faster data operations (READ or WRITE) within a row-address (A0-A9) defined page boundary. The FAST PAGE MODE cycle is always initiated with a row address strobed-in by $\overline{RAS}$ followed by a column address strobed-in by $\overline{CAS}$. $\overline{CAS}$ may be toggled-in by holding $\overline{RAS}$ LOW and strobing-in different column addresses, thus executing faster memory cycles.

Returning $\overline{RAS}$ and $\overline{CAS}$ HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the $\overline{RAS}$ high time. Memory cell data is retained in its correct state by maintaining power and executing any $\overline{RAS}$ cycle (READ, WRITE, $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$ or HIDDEN REFRESH) so that all 1,024 combinations of $\overline{RAS}$ addresses (A0-A9) are executed at least every 16ms (128ms on L-version), regardless of sequence.

FUNCTIONAL BLOCK DIAGRAM



U1, U2 = MT4C4001JDJ
U3 = MT4C1024DJ
or
U1, U2 = MT4C4001JDJ L (L-version)
U3 = MT4C1024DJ L (L-version)

TRUTH TABLE

FUNCTION		RAS	CAS	CAS9	WE	ADDRESSES tR	ADDRESSES tC	DATA IN/OUT DQ1-DQ8, D9, Q9
Standby		H	H→X	H→X	X	X	X	High-Z
READ		L	L	L	H	ROW	COL	Data Out
EARLY-WRITE		L	L	L	L	ROW	COL	Data In
FAST-PAGE-MODE	1st Cycle	L	H→L	H→L	H	ROW	COL	Data Out
READ	2nd Cycle	L	H→L	H→L	H	n/a	COL	Data Out
FAST-PAGE-MODE	1st Cycle	L	H→L	H→L	L	ROW	COL	Data In
WRITE	2nd Cycle	L	H→L	H→L	L	n/a	COL	Data In
RAS-ONLY REFRESH		L	H	H	X	ROW	n/a	High-Z
HIDDEN	READ	L→H→L	L	L	H	ROW	COL	Data Out
REFRESH	WRITE	L→H→L	L	L	L	ROW	COL	Data In
CAS-BEFORE-RAS REFRESH		H→L	L	L	H	X	X	High-Z
BATTERY BACKUP REFRESH (L-version)		H→L	L	L	X	X	X	High-Z

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} ..... -1V to +7V
Operating Temperature, T_A (Ambient) ..... 0°C to +70°C
Storage Temperature ..... -55°C to +125°C
Power Dissipation 3W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 2, 3, 6, 7, 25) (0°C ≤ T_A ≤ 70°C; V_{CC} = 5V ±10%)

PARAMETER/CONDITION		SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage		V_{CC}	4.5	5.5	V	1
Input High (Logic 1) Voltage, All Inputs		V_{IH}	2.4	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, All Inputs		V_{IL}	-1.0	0.8	V	1
INPUT LEAKAGE Any Input 0V ≤ V_{IN} ≤ V_{CC}	D9, $\overline{CAS9}$	I_I	-2	2	µA	
(All other pins not under test = 0V)	A0-A9, $\overline{RAS}$, $\overline{WE}$	I_I	-6	6	µA	
OUTPUT LEAKAGE (Q is disabled, 0V ≤ V_{OUT} ≤ V_{CC})	DQ1-DQ8, Q9	I_{OZ}	-10	10	µA	
OUTPUT LEVELS Output High (Logic 1) Voltage (I_{OUT} = -5mA)		V_{OH}	2.4		V	
Output Low (Logic 0) Voltage (I_{OUT} = 5mA)		V_{OL}		0.4	V	

		MAX				
PARAMETER/CONDITION	SYMBOL	-6	-7	-8	UNITS	NOTES
STANDBY CURRENT: (TTL) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC1}	6	6	6	mA	
STANDBY CURRENT: (CMOS)	I_{CC2}	3	3	3	mA	26
($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} -0.2V)		.6	.6	.6	mA	26, 27
OPERATING CURRENT: Random READ/WRITE Average power supply current	I_{CC3}	310	280	250	mA	2, 25
($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC (MIN))		305	275	245	mA	2,25,27
OPERATING CURRENT: FAST PAGE MODE Average power supply current	I_{CC4}	230	200	170	mA	2, 25
($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: ^tPC = ^tPC (MIN))		225	195	165	mA	2,25,27
REFRESH CURRENT: $\overline{RAS}$-ONLY Average power supply current	I_{CC5}	310	280	250	mA	2
($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}: ^tRC = ^tRC (MIN))		305	275	245	mA	2, 27
REFRESH CURRENT: $\overline{CAS}$-BEFORE-$\overline{RAS}$ Average power supply current	I_{CC6}	310	280	250	mA	2, 19
($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC (MIN))		305	275	245	mA	2,19,27
REFRESH CURRENT: BATTERY BACKUP (BBU) Average power supply current during BATTERY BACKUP refresh: $\overline{CAS}$ = 0.2V or $\overline{CAS}$-BEFORE-$\overline{RAS}$ cycling; $\overline{RAS}$ = ^tRAS (MIN) to 300ns; $\overline{WE}$ = V_{CC} -0.2V; A0-A9 and D_{IN} = V_{CC} - 0.2V or 0.2V (D_{IN} may be left open), ^tRC = 125µs (1,024 rows at 125µs = 128ms)	I_{CC7}	.8	.8	.8	mA	27

DRAM MODULE

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A9	C_{I1}		19	pF	17
Input Capacitance: $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	C_{I2}		25	pF	17
Input Capacitance: D9	C_{I3}		10	pF	17
Input/Output Capacitance: DQ1-DQ8	$C_{I/O}$		10	pF	17
Output Capacitance: Q9	C_O		10	pF	17

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 3, 4, 5, 6, 7, 10, 11, 16, 21) ($0°C \le T_A \le +70°C$; V_{CC} = 5V ±10%)

AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	^tRC	110		130		150		ns	
READ-WRITE cycle time	^tRWC	n/a		n/a		n/a		n/a	21
FAST-PAGE-MODE READ or WRITE cycle time	^tPC	40		40		45		ns	
FAST-PAGE-MODE READ-WRITE cycle time	^tPRWC	n/a		n/a		n/a		n/a	21
Access time from $\overline{RAS}$	^tRAC	60			70		80	ns	8
Access time from $\overline{CAS}$	^tCAC		15		20		20	ns	9
Access time from column address	^tAA		30		35		40	ns	
Access time from $\overline{CAS}$ precharge	^tCPA		35		40		45	ns	
$\overline{RAS}$ pulse width	^tRAS	60	100,000	70	100,000	80	100,000	ns	
$\overline{RAS}$ pulse width (FAST PAGE MODE)	^tRASP	60	100,000	70	100,000	80	100,000	ns	
$\overline{RAS}$ hold time	^tRSH	15		20		20		ns	
$\overline{RAS}$ precharge time	^tRP	40		50		60		ns	
$\overline{CAS}$ pulse width	^tCAS	15	100,000	20	100,000	20	100,000	ns	
$\overline{CAS}$ hold time	^tCSH	60		70		80		ns	
$\overline{CAS}$ precharge time	^tCPN	10		10		10		ns	18
$\overline{CAS}$ precharge time (FAST PAGE MODE)	^tCP	10		10		10		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	^tRCD	20	40	20	50	20	60	ns	13
$\overline{CAS}$ to $\overline{RAS}$ precharge time	^tCRP	10		10		10		ns	
Row address setup time	^tASR	0		0		0		ns	
Row address hold time	^tRAH	10		10		10		ns	
$\overline{RAS}$ to column address delay time	^tRAD	15	30	15	35	15	40	ns	22
Column address setup time	^tASC	0		0		0		ns	
Column address hold time	^tCAH	10		15		15		ns	
Column address hold time (referenced to $\overline{RAS}$)	^tAR	50		55		60		ns	
Column address to $\overline{RAS}$ lead time	^tRAL	30		35		40		ns	
Read command setup time	^tRCS	0		0		0		ns	
Read command hold time (referenced to $\overline{CAS}$)	^tRCH	0		0		0		ns	24
Read command hold time (referenced to $\overline{RAS}$)	^tRRH	0		0		0		ns	24
$\overline{CAS}$ to output in Low-Z	^tCLZ	0		0		0		ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

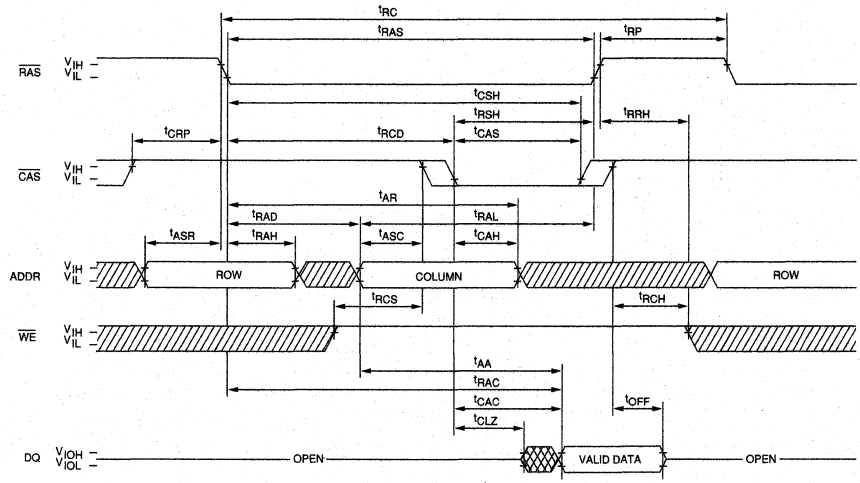
(Notes: 3, 4, 5, 6, 7, 10, 11, 16, 21) (0°C ≤ T_A ≤ +70°C; Vcc = 5V ±10%)

AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Output buffer turn-off delay	tOFF	0	20	0	20	0	20	ns	12
$\overline{WE}$ command setup time	tWCS	0		0		0		ns	
Write command hold time	tWCH	10		15		15		ns	
Write command hold time (referenced to $\overline{RAS}$)	tWCR	45		55		60		ns	
Write command pulse width	tWP	10		15		15		ns	
Write command to $\overline{RAS}$ lead time	tRWL	15		20		20		ns	
Write command to $\overline{CAS}$ lead time	tCWL	15		20		20		ns	
Data-in setup time	tDS	0		0		0		ns	15
Data-in hold time	tDH	10		15		15		ns	15
Data-in hold time (referenced to $\overline{RAS}$)	tDHR	45		55		60		ns	
Transition time (rise or fall)	tT	3	50	3	50	3	50	ns	5, 16
Refresh period (1,024 cycles)	tREF		16/128		16/128		16/128	ms	3/27
$\overline{RAS}$ to $\overline{CAS}$ precharge time	tRPC	0		0		0		ns	
$\overline{CAS}$ setup time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	tCSR	10		10		10		ns	19
$\overline{CAS}$ hold time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	tCHR	15		15		15		ns	19
$\overline{WE}$ hold time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	tWRH	10		10		10		ns	23
$\overline{WE}$ setup time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	tWRP	10		10		10		ns	23
$\overline{WE}$ hold time (WCBR test cycle)	tWTH	10		10		10		ns	23
$\overline{WE}$ setup time (WCBR test cycle)	tWTS	10		10		10		ns	23

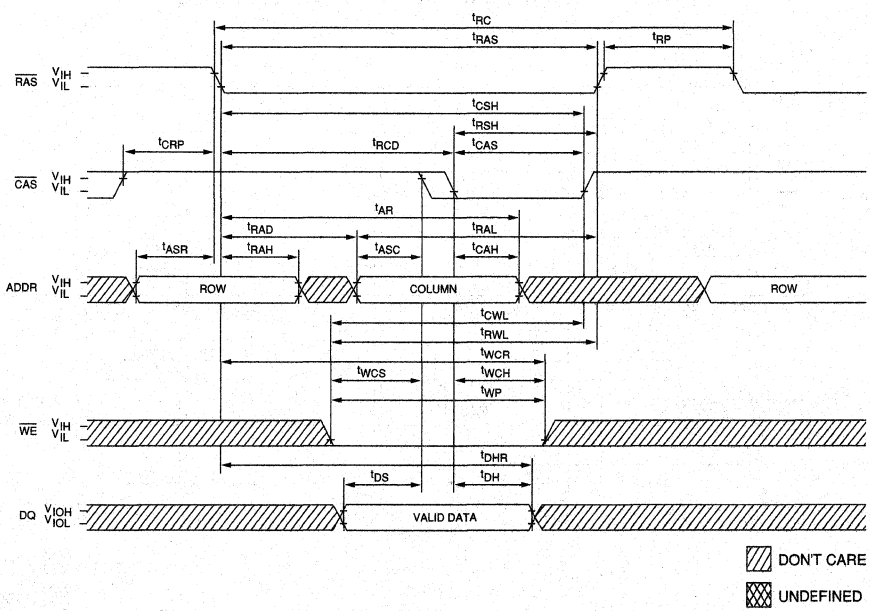
NOTES

1. All voltages referenced to V_{SS}.
2. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
3. An initial pause of 100µs is required after power-up followed by any eight $\overline{RAS}$ REFRESH cycles ($\overline{RAS}$-ONLY or CBR with $\overline{WE}$ HIGH) before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-up should be repeated any time the ^{t}REF refresh requirement is exceeded.
4. AC characteristics assume ^{t}T = 5ns.
5. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is assured.
7. Measured with a load equivalent to two TTL gates and 100pF.
8. Assumes that $^{t}RCD < ^{t}RCD$ (MAX). If ^{t}RCD is greater than the maximum recommended value shown in this table, ^{t}RAC will increase by the amount that ^{t}RCD exceeds the value shown.
9. Assumes that $^{t}RCD \geq ^{t}RCD$ (MAX).
10. If $\overline{CAS}$ = V_{IH}, data output is High-Z.
11. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
12. ^{t}OFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
13. Operation within the ^{t}RCD (MAX) limit ensures that ^{t}RAC (MAX) can be met. ^{t}RCD (MAX) is specified as a reference point only; if ^{t}RCD is greater than the specified ^{t}RCD (MAX) limit, then access time is controlled exclusively by ^{t}CAC.
14. Either ^{t}RCH or ^{t}RRH must be satisfied for a READ cycle.
15. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY-WRITE cycles.
16. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
17. This parameter is sampled. Capacitance is measured using MIL-STD-883C, Method 3012.1 (1 MHz AC, Vcc = 5V, DC bias = 2.4V @ 15mV RMS).
18. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, data-out (Q) will be maintained from the previous cycle. To initiate a new cycle and clear the Q buffer, $\overline{CAS}$ must be pulsed HIGH for ^{t}CP.
19. On-chip refresh and address counters are enabled.
20. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW.
21. LATE-WRITE, READ-WRITE or READ-MODIFY-WRITE cycles are not available due to $\overline{OE}$ being grounded on U1 and U2.
22. Operation within the ^{t}RAD (MAX) limit ensures that ^{t}RCD (MAX) can be met. ^{t}RAD (MAX) is specified as a reference point only; if ^{t}RAD is greater than the specified ^{t}RAD (MAX) limit, then access time is controlled exclusively by ^{t}AA.
23. ^{t}WTS and ^{t}WTH are setup and hold specifications for the $\overline{WE}$ pin being held LOW to enable the JEDEC test mode (with CBR timing constraints). These two parameters are the inverts of ^{t}WRP and ^{t}WRH in the CBR refresh cycle.
24. Either ^{t}RCH or ^{t}RRH must be satisfied for a READ cycle.
25. I_{CC} is dependent on cycle rates.
26. All other inputs at Vcc - 0.2V.
27. Applies to L-version only.

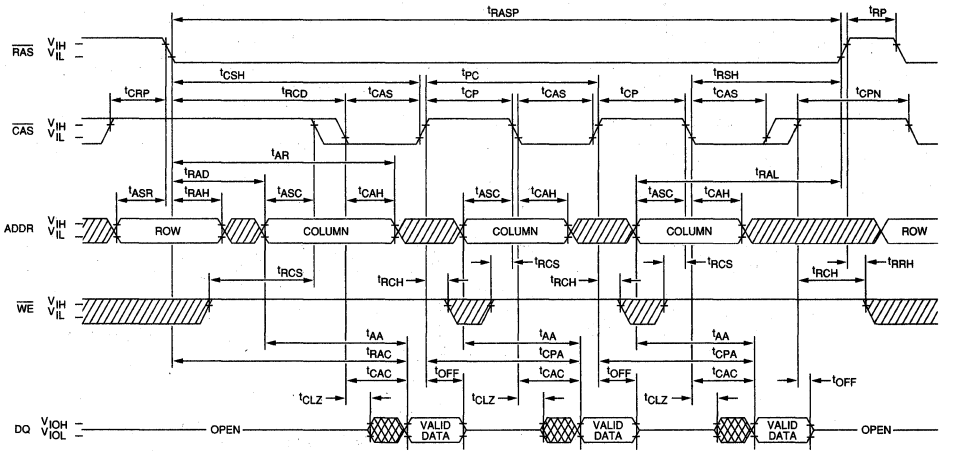
READ CYCLE



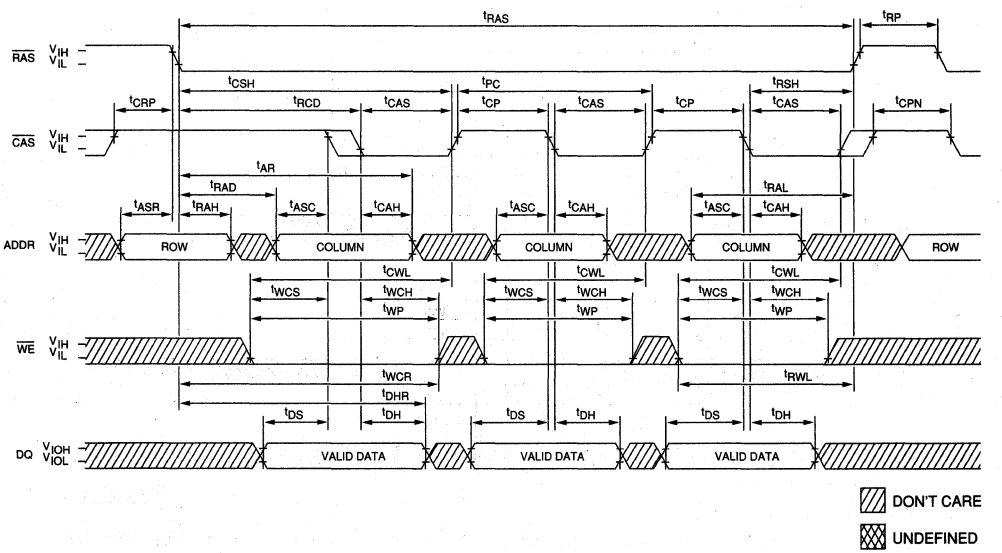
EARLY-WRITE CYCLE



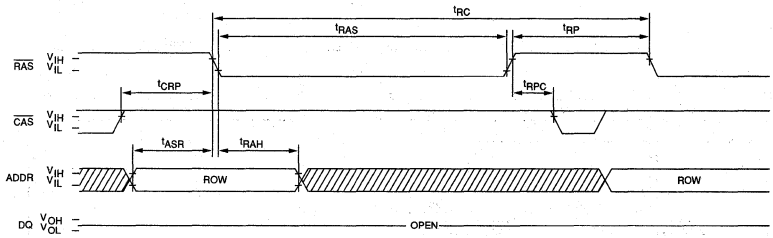
FAST-PAGE-MODE READ CYCLE



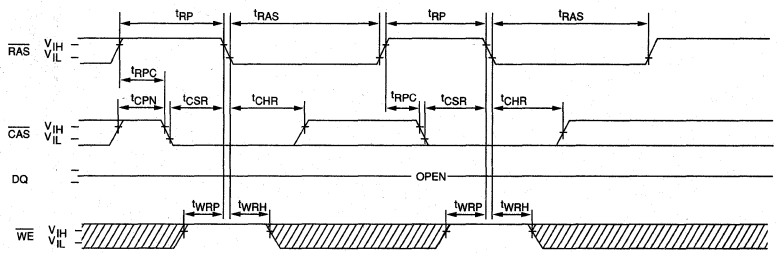
FAST-PAGE-MODE EARLY-WRITE CYCLE



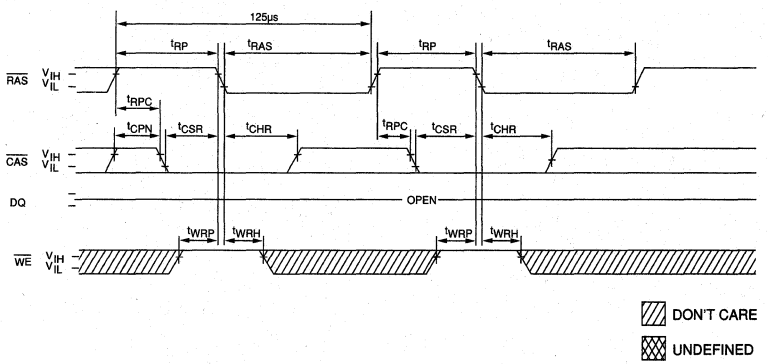
$\overline{\text{RAS}}$-ONLY REFRESH CYCLE
(ADDR = A0-A9; $\overline{\text{WE}}$ = DON'T CARE)



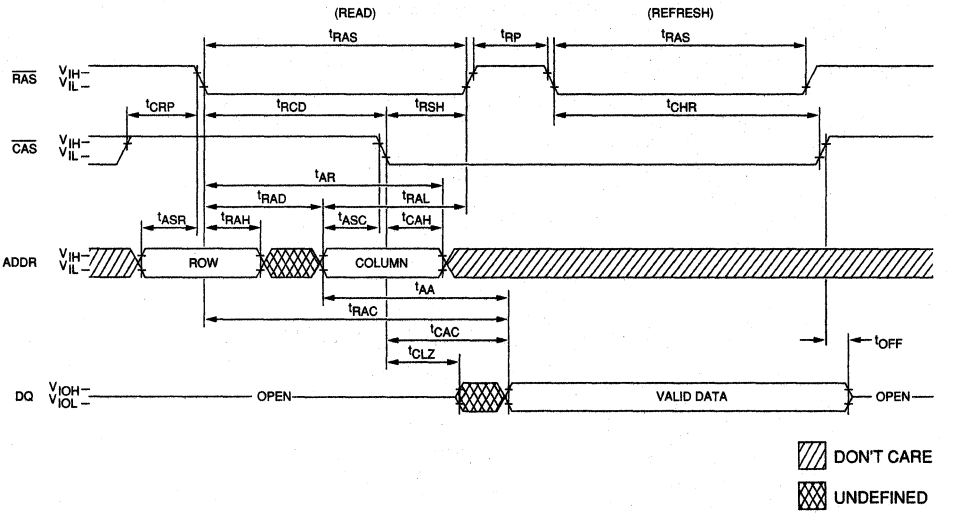
$\overline{\text{CAS}}$-BEFORE-$\overline{\text{RAS}}$ REFRESH CYCLE
(A0-A9 = DON'T CARE)



BATTERY BACKUP REFRESH CYCLE [27]
(A0-A9 = DON'T CARE)



HIDDEN REFRESH CYCLE [20]
($\overline{WE}$ = HIGH)



DRAM MODULE

1 MEG x 9 DRAM

FAST PAGE MODE (MT9D19)
LOW POWER,
EXTENDED REFRESH (MT9D19 L)

FEATURES

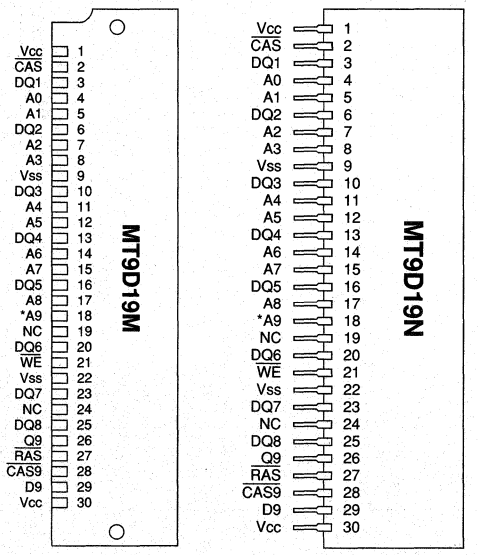
- Industry standard pinout in a 30-pin single-in-line package
- High-performance, CMOS silicon-gate process
- Single 5V ±10% power supply
- All device pins are fully TTL compatible
- Low power, 27mW (2.7mW L-version) standby; 1,575mW active, typical
- Refresh modes: RAS-ONLY, CAS-BEFORE-RAS (CBR) and HIDDEN
- 512-cycle refresh distributed across 8ms or 512-cycle extended refresh distributed across 64ms
- FAST PAGE MODE access cycle
- Low CMOS standby current, 1.6mA maximum (L-version)

OPTIONS

	MARKING
Timing	
60ns access	- 6
70ns access	- 7
80ns access	- 8
Packages	
Leadless 30-pin SIMM	M
Leaded 30-pin SIP	N
Power/Refresh	
Normal Power/8ms	Blank
Low Power/64ms	L

Part Number Example: MT9D19ML-6

PIN ASSIGNMENT (Top View)



*Address not used for RAS-ONLY REFRESH

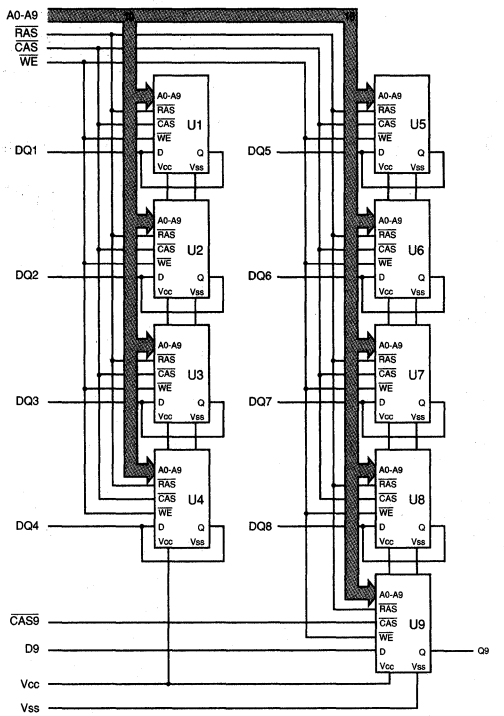
GENERAL DESCRIPTION

The MT9D19 is a randomly accessed solid-state memory containing 1,048,576 words organized in a x9 configuration. During READ or WRITE cycles, each word is uniquely addressed through the 20 address bits, which are entered 10 bits (A0-A9) at a time. RAS is used to latch the first 10 bits and CAS the latter 10 bits. A READ or WRITE cycle is selected with the WE input. A logic HIGH on WE dictates READ mode while a logic LOW on WE dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of WE or CAS, whichever occurs last. EARLY-WRITE occurs when WE goes LOW prior to CAS going LOW, and the output pins remain open (High-Z) until the next CAS cycle.

FAST PAGE MODE operations allow faster data operations (READ or WRITE) within a row-address (A0-A9) defined page boundary. The FAST PAGE MODE cycle is always initiated with a row address strobed-in by RAS followed by a column address strobed-in by CAS. CAS may be toggled-in by holding RAS LOW and strobing-in different column addresses, thus executing faster memory cycles.

Returning RAS and CAS HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the RAS high time. Memory cell data is retained in its correct state by maintaining power and executing any RAS cycle (READ, WRITE, RAS-ONLY, CAS-BEFORE-RAS or HIDDEN REFRESH) so that all 512 combinations of RAS addresses (A0-A8) are executed at least every 8ms (64ms on L-version), regardless of sequence.

FUNCTIONAL BLOCK DIAGRAM



U1-U9 = MT4C1024DJ
U1-U9 = MT4C1024DJ L (L-version)

TRUTH TABLE

FUNCTION		RAS	CAS	CAS9	WE	ADDRESSES tR	ADDRESSES tC	DATA IN/OUT DQ1-DQ8, D9, Q9
Standby		H	H→X	H→X	X	X	X	High-Z
READ		L	L	L	H	ROW	COL	Data Out
EARLY-WRITE		L	L	L	L	ROW	COL	Data In
FAST-PAGE-MODE	1st Cycle	L	H→L	H→L	H	ROW	COL	Data Out
READ	2nd Cycle	L	H→L	H→L	H	n/a	COL	Data Out
FAST-PAGE-MODE	1st Cycle	L	H→L	H→L	L	ROW	COL	Data In
WRITE	2nd Cycle	L	H→L	H→L	L	n/a	COL	Data In
RAS-ONLY REFRESH		L	H	H	X	ROW	n/a	High-Z
HIDDEN	READ	L→H→L	L	L	H	ROW	COL	Data Out
REFRESH	WRITE	L→H→L	L	L	L	ROW	COL	Data In
CAS-BEFORE-RAS REFRESH		H→L	L	L	X	X	X	High-Z
BATTERY BACKUP REFRESH (L-version)		H→L	L	L	X	X	X	High-Z

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} ..... -1V to +7V
Operating Temperature, T_A (Ambient) ..... 0°C to +70°C
Storage Temperature (Plastic) ..... -55°C to +125°C
Power Dissipation 9W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 3, 4, 6, 7) (0°C ≤ T_A ≤ 70°C; V_{CC} = 5V ±10%)

PARAMETER/CONDITION		SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage		V_{CC}	4.5	5.5	V	1
Input High (Logic 1) Voltage, All Inputs		V_{IH}	2.4	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, All Inputs		V_{IL}	-1.0	0.8	V	1
INPUT LEAKAGE: Any Input 0V ≤ V_{IN} ≤ V_{CC} (All other pins not under test = 0V)	D9, $\overline{CAS9}$	I_I	-2	2	µA	
	A0-A9, $\overline{RAS}$, $\overline{WE}$	I_I	-18	18	µA	
OUTPUT LEAKAGE: (Q is disabled, 0V ≤ V_{OUT} ≤ V_{CC})	DQ1-DQ8, Q9	I_{OZ}	-10	10	µA	
OUTPUT LEVELS Output High Voltage (I_{OUT} = -5mA)		V_{OH}	2.4		V	
Output Low Voltage (I_{OUT} = 5mA)		V_{OL}		0.4	V	

		MAX				
PARAMETER/CONDITION	SYMBOL	-6	-7	-8	UNITS	NOTES
STANDBY CURRENT: (TTL) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC1}	18	18	18	mA	
STANDBY CURRENT: (CMOS)	I_{CC2}	9	9	9	mA	23
($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} -0.2V)		1.8	1.8	1.8	mA	23, 25
OPERATING CURRENT: Random READ/WRITE Average power supply current	I_{CC3}	810	720	630	mA	3, 4
($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC (MIN))		765	675	585	mA	3,4,25
OPERATING CURRENT: FAST PAGE MODE Average power supply current	I_{CC4}	630	540	450	mA	3, 4
($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: ^tPC = ^tPC (MIN))		585	495	405	mA	3,4,25
REFRESH CURRENT: $\overline{RAS}$-ONLY Average power supply current	I_{CC5}	810	720	630	mA	3
($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}: ^tRC = ^tRC (MIN))		765	675	585	mA	3, 25
REFRESH CURRENT: $\overline{CAS}$-BEFORE-$\overline{RAS}$ Average power supply current	I_{CC6}	810	720	630	mA	3, 5
($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC (MIN))		765	675	585	mA	3,5,25
REFRESH CURRENT: BATTERY BACKUP (BBU) Average power supply current during BATTERY BACKUP refresh: $\overline{CAS}$ = 0.2V or $\overline{CAS}$-BEFORE-$\overline{RAS}$ cycling; $\overline{RAS}$ = ^tRAS (MIN) to 1µs; $\overline{WE}$, A0-A9 and D_{IN} = V_{CC} -0.2V or 0.2V (D_{IN} may be left OPEN), ^tRC = 125µs (512 rows at 125µs = 64ms)	I_{CC7}	1.8	1.8	1.8	mA	25

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A9	C_{I1}		58	pF	2
Input Capacitance: $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	C_{I2}		76	pF	2
Input Capacitance: D9	C_{I3}		10	pF	2
Input/Output Capacitance: DQ1-DQ8	C_{IO}		15	pF	2
Output Capacitance: Q9	C_O		10	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C ≤ T_A ≤ 70°C; Vcc = 5V ±10%)

AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	^tRC	110		130		150		ns	
READ-WRITE cycle time	^tRWC	n/a		n/a		n/a		n/a	24
FAST-PAGE-MODE READ or WRITE cycle time	^tPC	40		40		40		ns	
FAST-PAGE-MODE READ-WRITE cycle time	^tPRWC	n/a		n/a		n/a		n/a	24
Access time from $\overline{RAS}$	^tRAC		60		70		80	ns	14
Access time from $\overline{CAS}$	^tCAC		20		20		20	ns	15
Access time from column address	^tAA		30		35		40	ns	
Access time from $\overline{CAS}$ precharge	^tCPA		35		40		45	ns	
$\overline{RAS}$ pulse width	^tRAS	60	100,000	70	100,000	80	100,000	ns	
$\overline{RAS}$ pulse width (FAST PAGE MODE)	^tRASP	60	100,000	70	100,000	80	100,000	ns	
$\overline{RAS}$ hold time	^tRSH	20		20		20		ns	
$\overline{RAS}$ precharge time	^tRP	40		50		60		ns	
$\overline{CAS}$ pulse width	^tCAS	20	100,000	20	100,000	20	100,000	ns	
$\overline{CAS}$ hold time	^tCSH	60		70		80		ns	
$\overline{CAS}$ precharge time	^tCPN	10		10		10		ns	16
$\overline{CAS}$ precharge time (FAST PAGE MODE)	^tCP	10		10		10		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	^tRCD	20	40	20	60	20	60	ns	17
$\overline{CAS}$ to $\overline{RAS}$ precharge time	^tCRP	5		5		5		ns	
Row address setup time	^tASR	0		0		0		ns	
Row address hold time	^tRAH	10		10		10		ns	
$\overline{RAS}$ to column address delay time	^tRAD	15	30	15	35	15	40	ns	18
Column address setup time	^tASC	0		0		0		ns	
Column address hold time	^tCAH	15		15		15		ns	
Column address hold time (referenced to $\overline{RAS}$)	^tAR	45		55		60		ns	
Column address to $\overline{RAS}$ lead time	^tRAL	30		35		40		ns	
Read command setup time	^tRCS	0		0		0		ns	
Read command hold time (referenced to $\overline{CAS}$)	^tRCH	0		0		0		ns	19
Read command hold time (referenced to $\overline{RAS}$)	^tRRH	0		0		0		ns	19

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

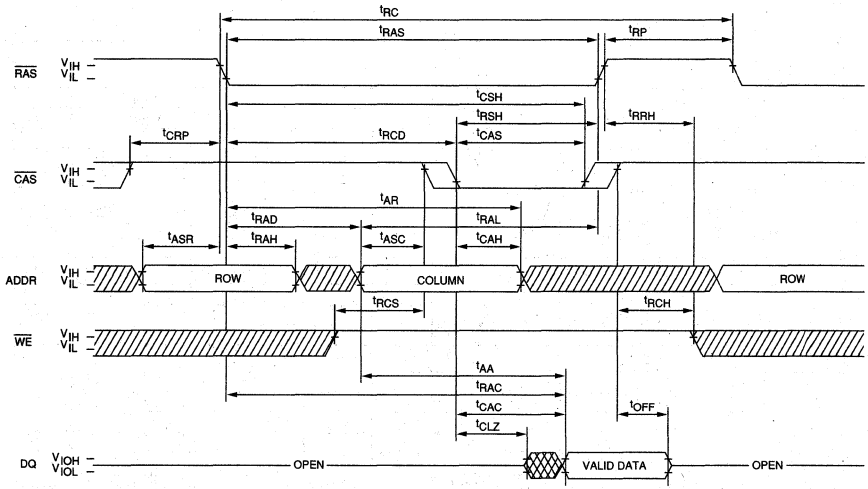
(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C ≤ T_A ≤ 75°C; Vcc = 5V ±10%)

AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
$\overline{CAS}$ to output in Low-Z	^tCLZ	0		0		0		ns	
Output buffer turn-off delay	^tOFF	0	20	0	20	0	20	ns	20
$\overline{WE}$ command setup time	^tWCS	0		0		0		ns	
Write command hold time	^tWCH	10		15		15		ns	
Write command hold time (referenced to $\overline{RAS}$)	^tWCR	45		55		60		ns	
Write command pulse width	^tWP	10		15		15		ns	
Write command to $\overline{RAS}$ lead time	^tRWL	20		20		20		ns	
Write command to $\overline{CAS}$ lead time	^tCWL	20		20		20		ns	
Data-in setup time	^tDS	0		0		0		ns	21
Data-in hold time	^tDH	15		15		15		ns	21
Data-in hold time (referenced to $\overline{RAS}$)	^tDHR	45		55		60		ns	
Transition time (rise or fall)	^tT	3	50	3	50	3	50	ns	9, 10
Refresh period (512 cycles)	^tREF		8/64		8/64		8/64	ms	7/25
$\overline{RAS}$ to $\overline{CAS}$ precharge time	^tRPC	0		0		0		ns	
$\overline{CAS}$ setup time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH)	^tCSR	10		10		10		ns	5
$\overline{CAS}$ hold time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH)	^tCHR	10		15		15		ns	5

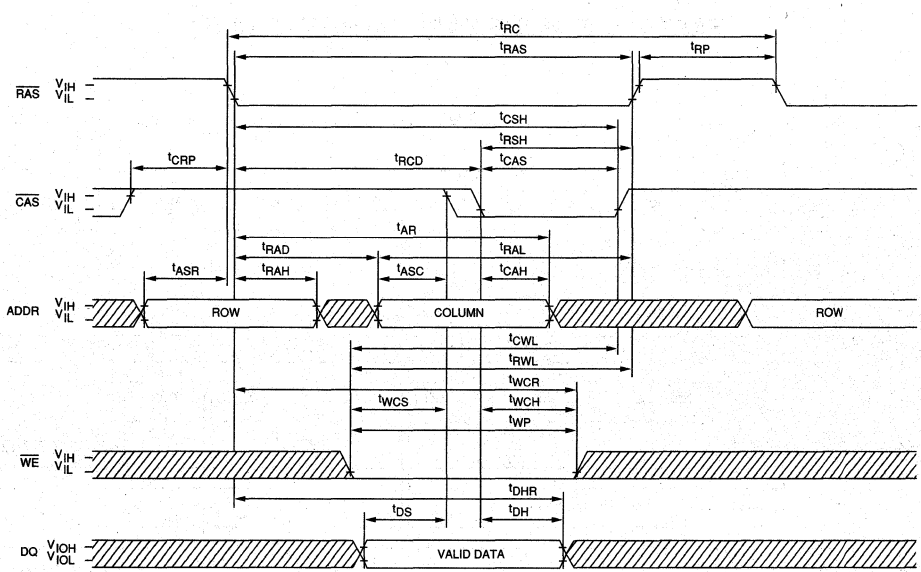
NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. Capacitance is measured using MIL-STD-883C, Method 3012.1 (1 MHz AC, Vcc = 5V, DC bias = 2.4V @ 15mV RMS).
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \le T_A \le 70°C$) is assured.
7. An initial pause of 100µs is required after power-up followed by any eight $\overline{RAS}$ cycles before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-up should be repeated any time the ^tREF refresh requirement is exceeded.
8. AC characteristics assume ^tT = 5ns.
9. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS}$ = V_{IH}, data output is High-Z.
12. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to two TTL gates and 100pF.
14. Assumes that $^tRCD < {}^tRCD$ (MAX). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
15. Assumes that $^tRCD \ge {}^tRCD$ (MAX).
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer, $\overline{CAS}$ must be pulsed HIGH for ^tCPN.
17. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (MAX) limit, then access time is controlled exclusively by ^tCAC.
18. Operation within the ^tRAD (MAX) limit ensures that ^tRCD (MAX) can be met. ^tRAD (MAX) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (MAX) limit, then access time is controlled exclusively by ^tAA.
19. Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
20. ^tOFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
21. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY-WRITE cycles.
22. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW.
23. All other inputs equal Vcc -0.2V.
24. LATE-WRITE, READ-WRITE or READ-MODIFY-WRITE cycles are not available due to the common DQ configuration of U1-U8.
25. Applies to L-version only.

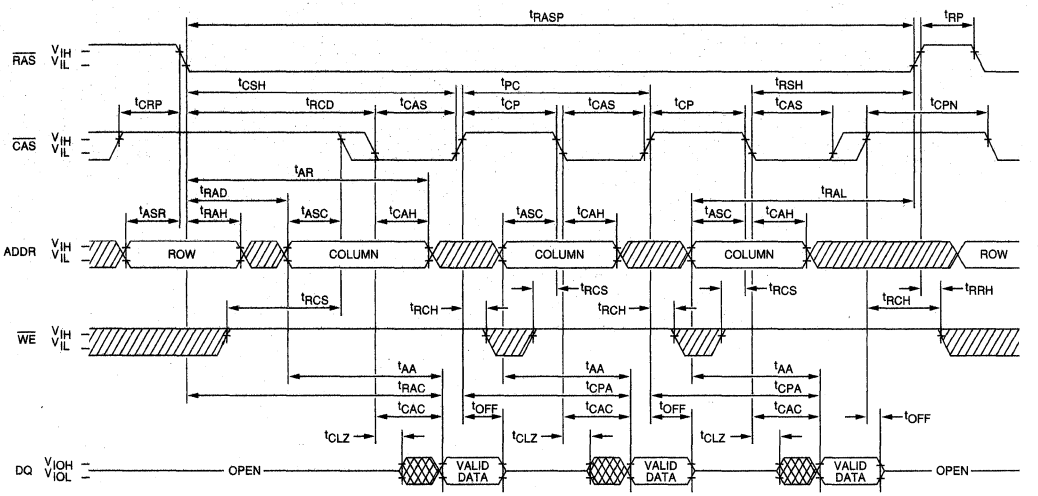
READ CYCLE



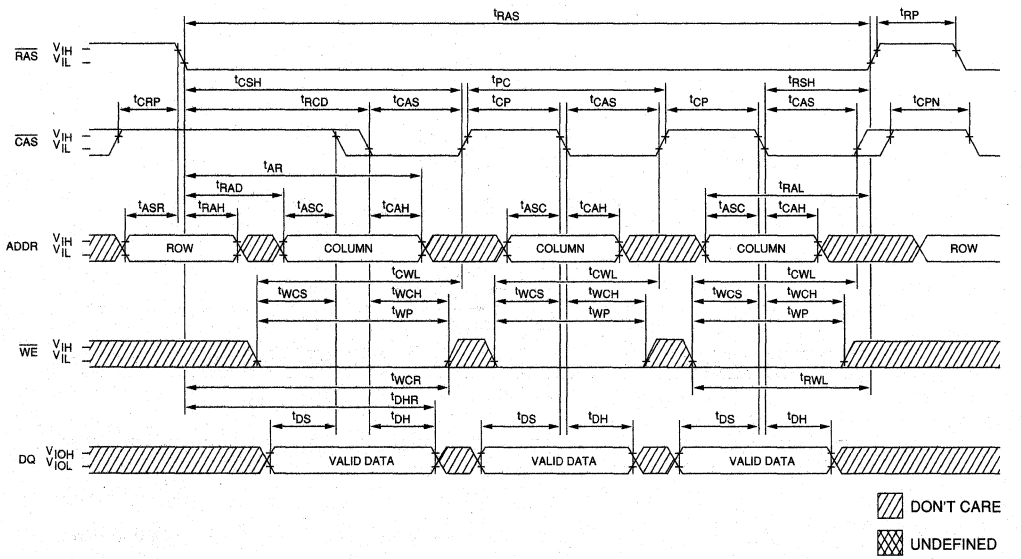
EARLY-WRITE CYCLE



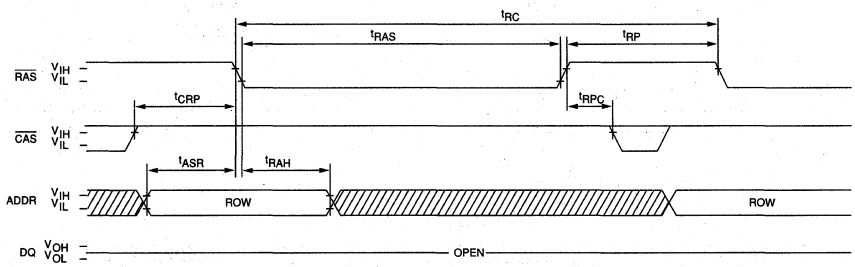
FAST-PAGE-MODE READ CYCLE



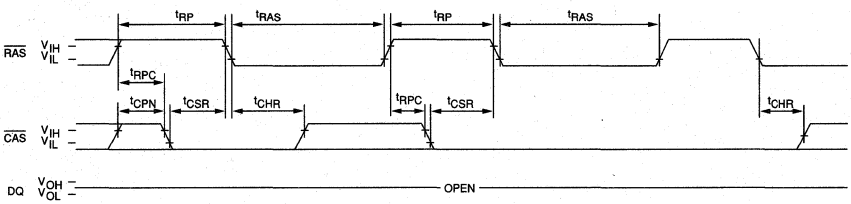
FAST-PAGE-MODE EARLY-WRITE CYCLE



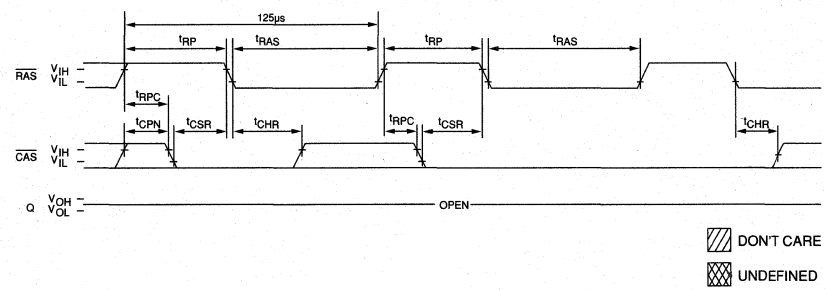
$\overline{\text{RAS}}$-ONLY REFRESH CYCLE
(ADDR = A0-A8; A9 and $\overline{\text{WE}}$ = DON'T CARE)



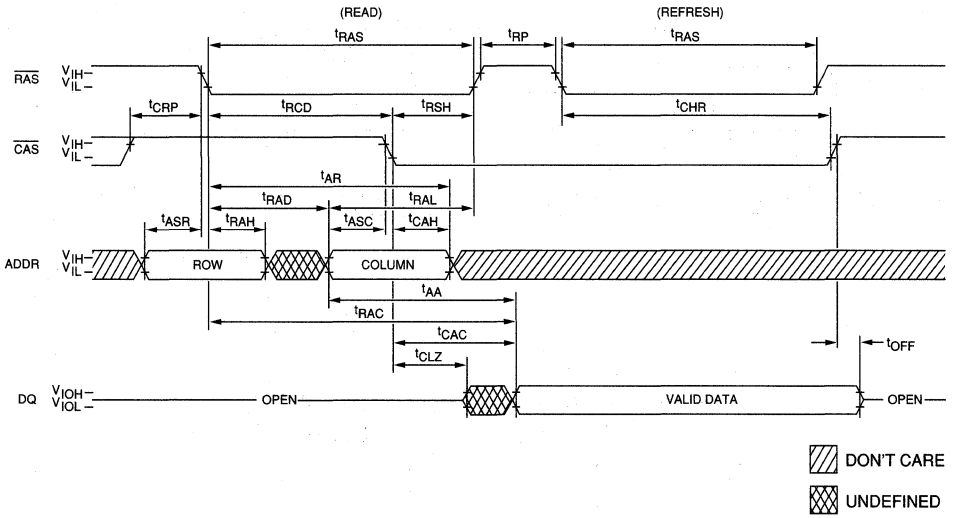
$\overline{\text{CAS}}$-BEFORE-$\overline{\text{RAS}}$ REFRESH CYCLE
(A0-A9 and $\overline{\text{WE}}$ = DON'T CARE)



BATTERY BACKUP REFRESH CYCLE [25]
(A0-A9 and $\overline{\text{WE}}$ = DON'T CARE)



HIDDEN REFRESH CYCLE [22]
($\overline{WE}$ = HIGH)



DRAM MODULE

4 MEG x 9 DRAM

FAST PAGE MODE

NEW DRAM MODULE

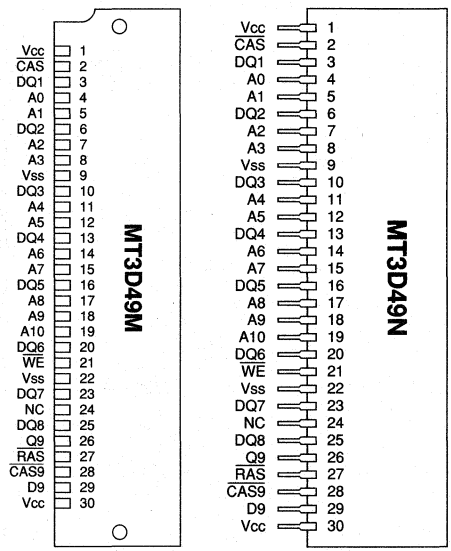
FEATURES

- Industry standard pinout in a 30-pin, single-in-line memory module
- High-performance, CMOS silicon-gate process
- Single 5V ±10% power supply
- Low power, 12mW standby; 775mW active, typical
- All device pins are fully TTL compatible
- FAST PAGE MODE access cycle
- Refresh modes: $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$ (CBR) and HIDDEN
- 2,048-cycle refresh distributed across 32ms
- Low profile

OPTIONS MARKING

- Timing
  - 60ns access - 6
  - 70ns access - 7
  - 80ns access - 8
- Packages
  - Leadless 30-pin SIMM M
  - Leaded 30-pin SIP N
- Part Number Example: MT3D49M-6

PIN ASSIGNMENT (Top View)



GENERAL DESCRIPTION

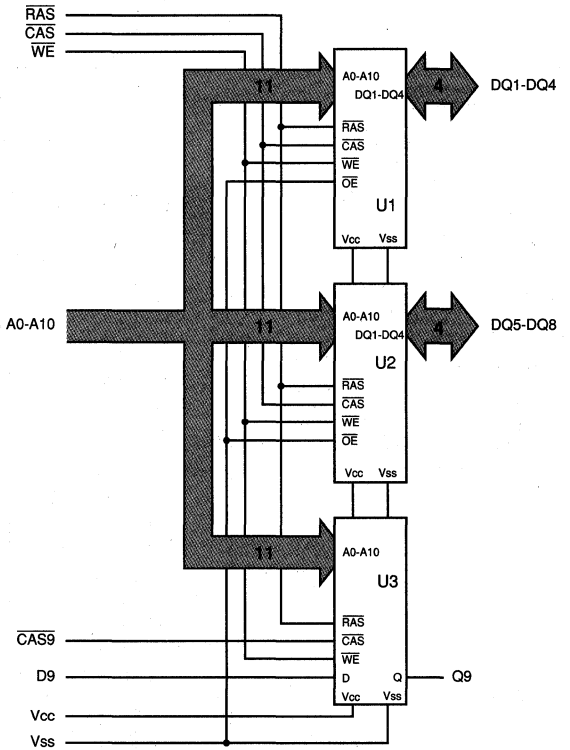
The MT3D49 is a randomly accessed solid-state memory containing 4,194,304 words organized in a x9 configuration. During READ or WRITE cycles, each word is uniquely addressed through 22 address bits, which are entered 11 bits (A0-A10) at a time. $\overline{RAS}$ is used to latch the first 11 bits and $\overline{CAS}$ the latter 11 bits. READ or WRITE cycles are selected with the $\overline{WE}$ input. A logic HIGH on $\overline{WE}$ dictates READ mode while a logic LOW on $\overline{WE}$ dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of $\overline{CAS}$. Since $\overline{WE}$ goes LOW prior to $\overline{CAS}$ going LOW, the output pins remain open (High-Z) until the next $\overline{CAS}$ cycle.

FAST PAGE MODE operations allow faster data operations (READ or WRITE) within a row address (A0-A10) defined page boundary. The FAST PAGE MODE cycle is always initiated with a row address strobed-in by $\overline{RAS}$ followed by a column address strobed-in by $\overline{CAS}$. $\overline{CAS}$ may be toggled-in by holding $\overline{RAS}$ LOW and strobing-in different column addresses, thus executing faster memory cycles. Returning $\overline{RAS}$ HIGH terminates the FAST-PAGE-MODE operations.

Returning $\overline{RAS}$ and $\overline{CAS}$ HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the $\overline{RAS}$ high time. Memory cell data is retained in its correct state by maintaining power and executing any $\overline{RAS}$ cycle (READ, WRITE, $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$ or HIDDEN REFRESH) so that all 2,048 combinations of $\overline{RAS}$ addresses (A0-A10) are executed at least every 32ms, regardless of sequence. The CBR REFRESH cycle will invoke the refresh counter for automatic $\overline{RAS}$ addressing.

NEW DRAM MODULE

FUNCTIONAL BLOCK DIAGRAM



U1-U2 = MT4C4M4B1DJ
U3 = MT4C1004JDJ

TRUTH TABLE

FUNCTION		RAS	CAS	CAS9	WE	ADDRESSES		DATA IN/OUT
						^tR	^tC	DQ1-DQ8, D9, Q9
Standby		H	H→X	H→X	X	X	X	High-Z
READ		L	L	L	H	ROW	COL	Data Out
EARLY-WRITE		L	L	L	L	ROW	COL	Data In
FAST-PAGE-MODE	1st Cycle	L	H→L	H→L	H	ROW	COL	Data Out
READ	2nd Cycle	L	H→L	H→L	H	n/a	COL	Data Out
FAST-PAGE-MODE	1st Cycle	L	H→L	H→L	L	ROW	COL	Data In
WRITE	2nd Cycle	L	H→L	H→L	L	n/a	COL	Data In
RAS-ONLY REFRESH		L	H	H	X	ROW	n/a	High-Z
HIDDEN	READ	L→H→L	L	L	H	ROW	COL	Data Out
REFRESH	WRITE	L→H→L	L	L	L	ROW	COL	Data In
CAS-BEFORE-RAS REFRESH		H→L	L	L	H	X	X	High-Z

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} ..... -1V to +7V
Operating Temperature, T_A (Ambient) ..... 0°C to +70°C
Storage Temperature ..... -55°C to +125°C
Power Dissipation 3W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 3, 4, 6, 7) (0°C ≤ T_A ≤ 70°C; V_{CC} = 5V ±10%)

PARAMETER/CONDITION		SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage		V_{CC}	4.5	5.5	V	1
Input High (Logic 1) Voltage, All Inputs		V_{IH}	2.4	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, All Inputs		V_{IL}	-1.0	0.8	V	1
INPUT LEAKAGE Any Input 0V ≤ V_{IN} ≤ V_{CC} (All other pins not under test = 0V)	D9, $\overline{CAS9}$	I_I	-2	2	µA	
	A0-A10, $\overline{RAS}$, $\overline{WE}$	I_I	-6	6	µA	
OUTPUT LEAKAGE (Q is disabled, 0V ≤ V_{OUT} ≤ V_{CC})	DQ1-DQ8, Q9	I_{OZ}	-10	10	µA	
OUTPUT LEVELS Output High (Logic 1) Voltage (I_{OUT} = -5mA)		V_{OH}	2.4		V	
Output Low (Logic 0) Voltage (I_{OUT} = 5mA)		V_{OL}		0.4	V	

		MAX				
PARAMETER/CONDITION	SYMBOL	-6	-7	-8	UNITS	NOTES
STANDBY CURRENT: TTL Input Levels ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC1}	6	6	6	mA	
STANDBY CURRENT: CMOS Input Levels ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} -0.2V)	I_{CC2}	3	3	3	mA	
OPERATING CURRENT ($\overline{RAS}$ and $\overline{CAS}$ = Cycling; ^tRC = ^tRC (MIN))	I_{CC3}	350	300	270	mA	3, 4
OPERATING CURRENT: FAST PAGE MODE ($\overline{RAS}$ = V_{IL}; $\overline{CAS}$ = Cycling; ^tPC = ^tPC (MIN))	I_{CC4}	240	210	180	mA	3, 4
REFRESH CURRENT: $\overline{RAS}$-ONLY ($\overline{RAS}$ = Cycling; $\overline{CAS}$ = V_{IH}; ^tRC = ^tRC (MIN))	I_{CC5}	350	300	270	mA	3
REFRESH CURRENT: $\overline{CAS}$-BEFORE-$\overline{RAS}$	I_{CC6}	350	300	270	mA	3, 5

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A10	C_{I1}		19	pF	2
Input Capacitance: $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	C_{I2}		25	pF	2
Input/Output Capacitance: DQ1-DQ8	C_{IO}		10	pF	2
Input Capacitance: DQ9	C_{I3}		10	pF	2
Output Capacitance: Q9	C_O		10	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13, 22) (V_{CC} = 5V ±10%)

AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Random READ or WRITE cycle time	^tRC	110		130		150		ns	
READ-WRITE cycle time	^tRWC	n/a		n/a		n/a		ns	22
FAST-PAGE-MODE READ or WRITE cycle time	^tPC	40		40		45		ns	
FAST-PAGE-MODE READ-WRITE cycle time	^tPRWC	n/a		n/a		n/a		ns	22
Access time from $\overline{RAS}$	^tRAC		60		70		80	ns	14
Access time from $\overline{CAS}$	^tCAC		15		20		20	ns	15
Access time from column address	^tAA		30		35		40	ns	
Access time from $\overline{CAS}$ precharge	^tCPA		35		40		45	ns	
$\overline{RAS}$ pulse width	^tRAS	60	100,000	70	100,000	80	100,000	ns	
$\overline{RAS}$ pulse width (FAST PAGE MODE)	^tRASP	60	100,000	70	100,000	80	100,000	ns	
$\overline{RAS}$ hold time	^tRSH	15		20		20		ns	
$\overline{RAS}$ precharge time	^tRP	40		50		60		ns	
$\overline{CAS}$ pulse width	^tCAS	15	100,000	20	100,000	20	100,000	ns	
$\overline{CAS}$ hold time	^tCSH	60		70		80		ns	
$\overline{CAS}$ precharge time	^tCPN	10		10		10		ns	16
$\overline{CAS}$ precharge time (FAST PAGE MODE)	^tCP	10		10		10		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	^tRCD	20	40	20	50	20	60	ns	17
$\overline{CAS}$ to $\overline{RAS}$ precharge time	^tCRP	5		5		5		ns	
Row address setup time	^tASR	0		0		0		ns	
Row address hold time	^tRAH	10		10		10		ns	
$\overline{RAS}$ to column address delay time	^tRAD	15	30	15	35	15	40	ns	18
Column address setup time	^tASC	0		0		0		ns	
Column address hold time	^tCAH	10		15		15		ns	
Column address hold time (referenced to $\overline{RAS}$)	^tAR	50		55		60		ns	
Column address to $\overline{RAS}$ lead time	^tRAL	30		35		40		ns	
Read command setup time	^tRCS	0		0		0		ns	
Read command hold time (referenced to $\overline{CAS}$)	^tRCH	0		0		0		ns	19
Read command hold time (referenced to $\overline{RAS}$)	^tRRH	0		0		0		ns	19
$\overline{CAS}$ to output in Low-Z	^tCLZ	0		0		0		ns	
Output buffer turn-off delay	^tOFF	0	15	0	20	0	20	ns	20
$\overline{WE}$ command setup time	^tWCS	0		0		0		ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13, 23) (V_{CC} = 5V ±10%)

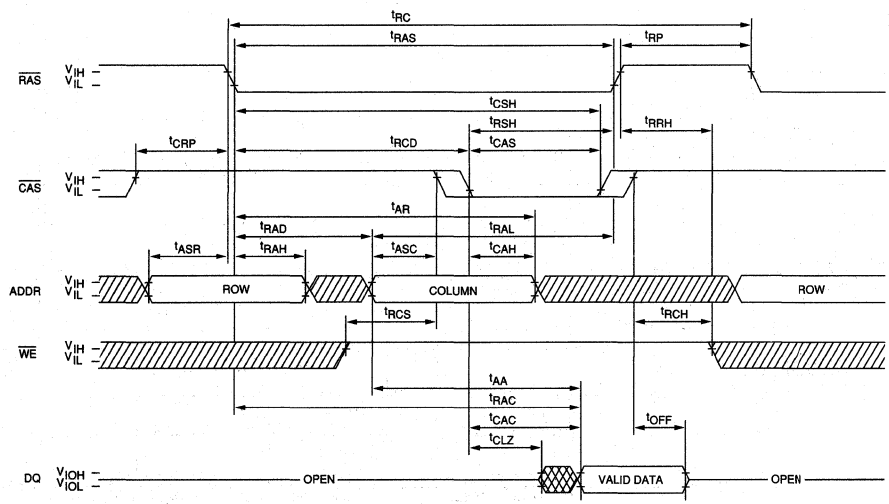
AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Write command hold time	^tWCH	10		15		15		ns	
Write command hold time (referenced to $\overline{RAS}$)	^tWCR	45		55		60		ns	
Write command pulse width	^tWP	10		15		15		ns	
Write command to $\overline{RAS}$ lead time	^tRWL	15		20		20		ns	
Write command to $\overline{CAS}$ lead time	^tCWL	15		20		20		ns	
Data-in setup time	^tDS	0		0		0		ns	21
Data-in hold time	^tDH	10		15		15		ns	21
Data-in hold time (referenced to $\overline{RAS}$)	^tDHR	45		55		60		ns	
Transition time (rise or fall)	^tT	3	50	3	50	3	50	ns	9, 10
Refresh period (2,048 cycles)	^tREF		32		32		32	ms	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	^tRPC	0		0		0		ns	
$\overline{CAS}$ setup time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tCSR	10		10		10		ns	5
$\overline{CAS}$ hold time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tCHR	15		15		15		ns	5
$\overline{WE}$ hold time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tWRH	10		10		10		ns	24
$\overline{WE}$ setup time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tWRP	10		10		10		ns	24
$\overline{WE}$ hold time (WCBR test cycle)	^tWTH	10		10		10		ns	24
$\overline{WE}$ setup time (WCBR test cycle)	^tWTS	10		10		10		ns	24

NEW ■ DRAM MODULE

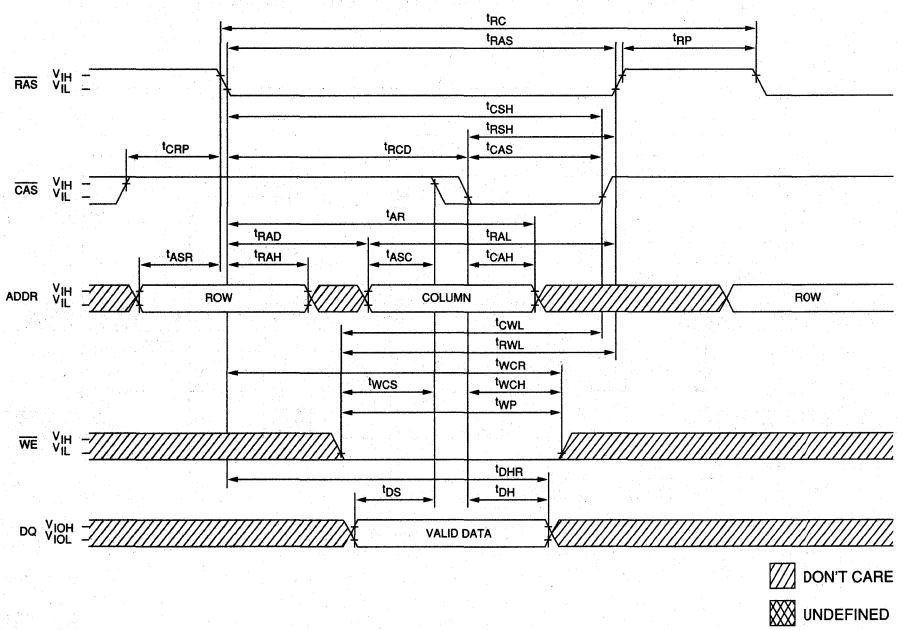
NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. Capacitance is measured using MIL-STD-883C, Method 3012.1 (1 MHz AC, Vcc = 5V, DC bias = 2.4V @ 15mV RMS).
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is assured.
7. An initial pause of 100µs is required after power-up followed by eight $\overline{RAS}$ refresh cycles ($\overline{RAS}$-ONLY or CBR with $\overline{WE}$ HIGH) before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-up should be repeated any time the ^{t}REF refresh requirement is exceeded.
8. AC characteristics assume ^{t}T = 5ns.
9. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS}$ = V_{IH}, data output is High-Z.
12. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to 2 TTL gates and 100pF.
14. Assumes that $^{t}RCD < {}^{t}RCD$ (MAX). If ^{t}RCD is greater than the maximum recommended value shown in this table, ^{t}RAC will increase by the amount that ^{t}RCD exceeds the value shown.
15. Assumes that $^{t}RCD \geq {}^{t}RCD$ (MAX).
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer, $\overline{CAS}$ must be pulsed HIGH for ^{t}CPN.
17. Operation within the ^{t}RCD (MAX) limit ensures that ^{t}RAC (MAX) can be met. ^{t}RCD (MAX) is specified as a reference point only; if ^{t}RCD is greater than the specified ^{t}RCD (MAX) limit, then access time is controlled exclusively by ^{t}CAC.
18. Operation within the ^{t}RAD (MAX) limit ensures that ^{t}RCD (MAX) can be met. ^{t}RAD (MAX) is specified as a reference point only; if ^{t}RAD is greater than the specified ^{t}RAD (MAX) limit, then access time is controlled exclusively by ^{t}AA.
19. Either ^{t}RCH or ^{t}RRH must be satisfied for a READ cycle.
20. ^{t}OFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
21. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY-WRITE cycles.
22. $\overline{OE}$ is tied permanently LOW; LATE-WRITE or READ-MODIFY-WRITE operations are not possible.
23. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW and $\overline{OE}$ = HIGH.
24. ^{t}WTS and ^{t}WTH are setup and hold specifications for the $\overline{WE}$ pin being held LOW to enable the JEDEC test mode (with CBR timing constraints). These two parameters are the inverts of ^{t}WRP and ^{t}WRH in the CBR refresh cycle.

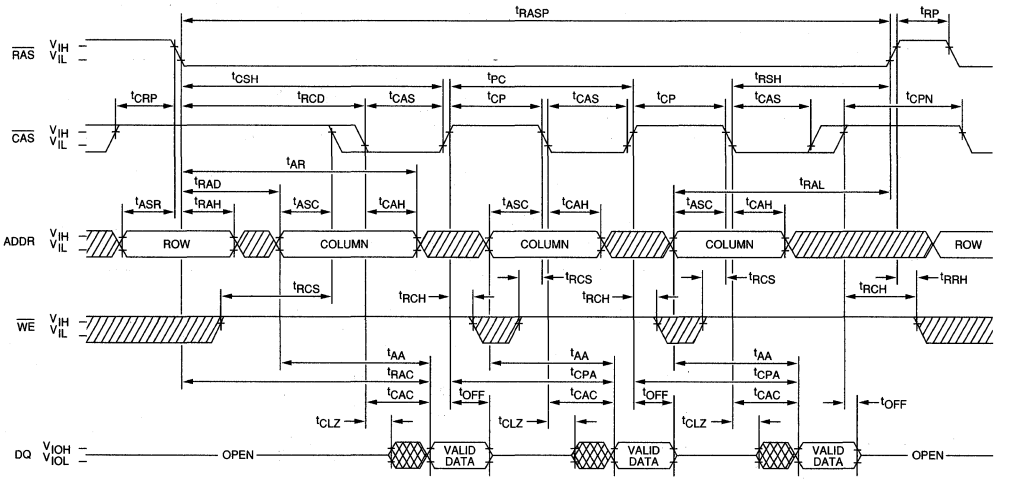
READ CYCLE



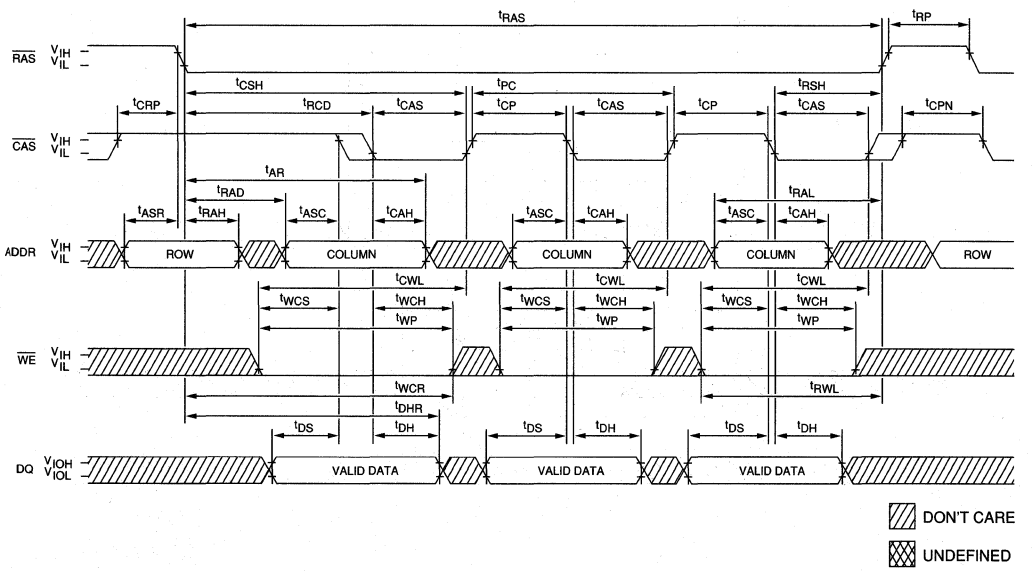
EARLY-WRITE CYCLE



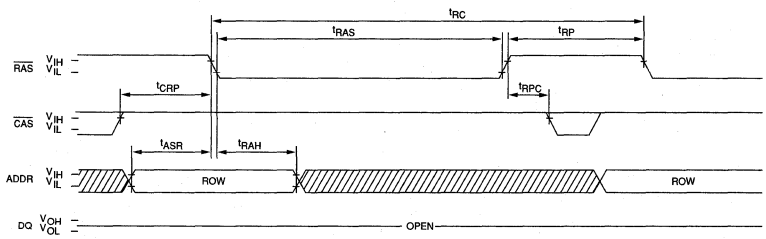
FAST-PAGE-MODE READ CYCLE



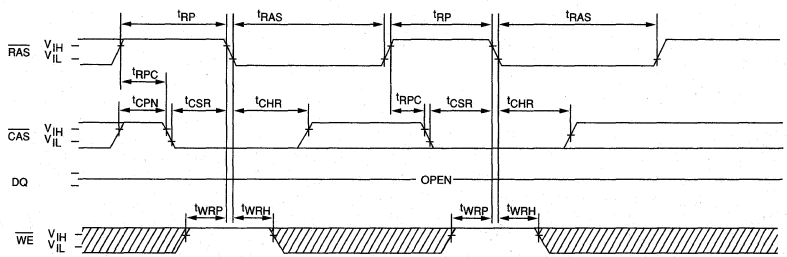
FAST-PAGE-MODE EARLY-WRITE CYCLE



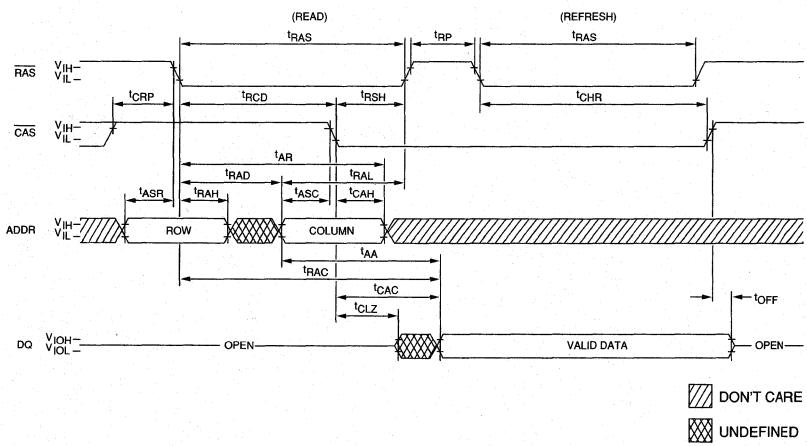
$\overline{RAS}$-ONLY REFRESH CYCLE
(ADDR = A0-A10; $\overline{WE}$ = DON'T CARE)



$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE
(A0-A10 = DON'T CARE)



HIDDEN REFRESH CYCLE [23]
($\overline{WE}$ = HIGH)



MICRON TECHNOLOGY, INC.

MT3D49
4 MEG x 9 DRAM MODULE

DRAM MODULE

4 MEG x 9 DRAM

FAST PAGE MODE (MT9D49)
LOW POWER,
EXTEDEND REFRESH (MT9D49 L)

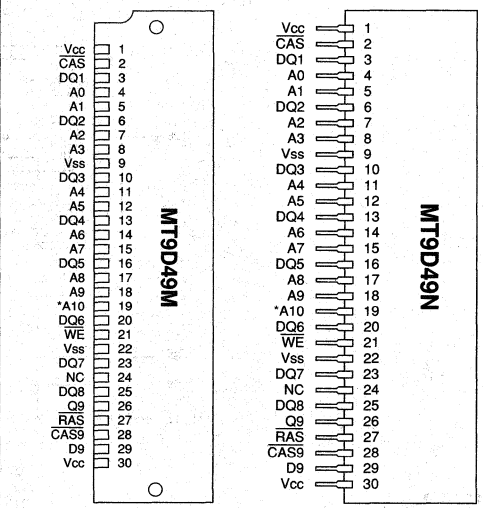
FEATURES

- Industry standard pinout in a 30-pin single-in-line package
- High-performance, CMOS silicon-gate process
- Single 5V ±10% power supply
- All device pins are fully TTL compatible
- Low power, 27mW (9mW L-version) standby; 2,025mW active, typical
- Refresh modes: RAS-ONLY, CAS-BEFORE-RAS (CBR) and HIDDEN
- 1,024-cycle refresh distributed across 16ms or 1,024-cycle extended refresh distributed across 128ms
- FAST PAGE MODE access cycle
- Low CMOS standby current, 1.8mA maximum (L-version)

OPTIONS MARKING

- Timing
  - 60ns access - 6
  - 70ns access - 7
  - 80ns access - 8
- Packages
  - Leadless 30-pin SIMM M
  - Leaded 30-pin SIP N
- Power/Refresh
  - Normal Power/16ms Blank
  - Low Power/128ms L
- Part Number Example: MT9D49ML-6

PIN ASSIGNMENT (Top View)



*Address not used for RAS-ONLY REFRESH

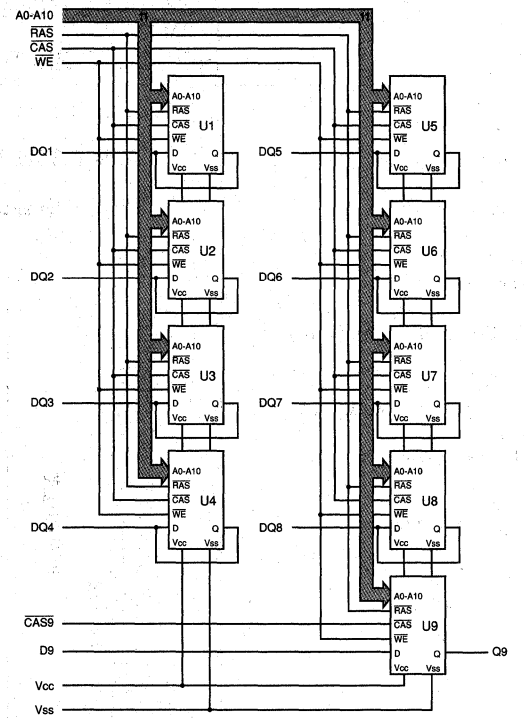
GENERAL DESCRIPTION

The MT9D49 is a randomly accessed solid-state memory containing 4,194,304 words organized in a x9 configuration. During READ or WRITE cycles, each bit is uniquely addressed through the 22 address bits which are entered 11 bits (A0-A10) at a time. RAS is used to latch the first 11 bits and CAS the latter 11 bits. A READ or WRITE cycle is selected with the WE input. A logic HIGH on WE dictates READ mode while a logic LOW on WE dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of WE or CAS, whichever occurs last. If WE goes LOW prior to CAS going LOW, the output pin(s) remain open (High-Z) until the next CAS cycle. EARLY WRITE occurs when WE goes LOW prior to CAS going LOW, and the ouput remains open (High-Z) until the next CAS cycle.

FAST PAGE MODE operations allow faster data operations (READ or WRITE) within a row-address (A0-A10) defined page boundary. The FAST PAGE MODE cycle is always initiated with a row address strobed-in by RAS followed by a column address strobed-in by CAS. CAS may be toggled-in by holding RAS LOW and strobing-in different column addresses, thus executing faster memory cycles. Returning RAS HIGH terminates the FAST PAGE MODE operation.

Returning RAS and CAS HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the RAS high time. Memory cell data is retained in its correct state by maintaining power and executing any RAS cycle (READ, WRITE, RAS-ONLY, CAS-BEFORE-RAS or HIDDEN REFRESH) so that all 1,024 combinations of RAS addresses (A0-A9) are executed at least every 16ms (128ms on L-version), regardless of sequence.

FUNCTIONAL BLOCK DIAGRAM



U1-U9 = MT4C1004JDJ
or
U1-U9 = MT4C1004JDJ L (L-version)

TRUTH TABLE

FUNCTION		RAS	CAS	CAS9	WE	ADDRESSES tR	ADDRESSES tC	DATA IN/OUT DQ1-DQ8, D9, Q9
Standby		H	H→X	H→X	X	X	X	High-Z
READ		L	L	L	H	ROW	COL	Data Out
EARLY-WRITE		L	L	L	L	ROW	COL	Data In
FAST-PAGE-MODE	1st Cycle	L	H→L	H→L	H	ROW	COL	Data Out
READ	2nd Cycle	L	H→L	H→L	H	n/a	COL	Data Out
FAST-PAGE-MODE	1st Cycle	L	H→L	H→L	L	ROW	COL	Data In
WRITE	2nd Cycle	L	H→L	H→L	L	n/a	COL	Data In
RAS-ONLY REFRESH		L	H	H	X	ROW	n/a	High-Z
HIDDEN	READ	L→H→L	L	L	H	ROW	COL	Data Out
REFRESH	WRITE	L→H→L	L	L	L	ROW	COL	Data In
CAS-BEFORE-RAS REFRESH		H→L	L	L	H	X	X	High-Z
BATTERY BACKUP REFRESH (L-version)		H→L	L	L	X	X	X	High-Z

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} ..... -1V to +7V
Operating Temperature, T_A (Ambient) ..... 0°C to +70°C
Storage Temperature (Plastic) ..... -55°C to +125°C
Power Dissipation 9W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 3, 4, 6, 7) (0°C ≤ T_A ≤ 70°C; V_{CC} = 5V ±10%)

PARAMETER/CONDITION		SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage		V_{CC}	4.5	5.5	V	1
Input High (Logic 1) Voltage, All Inputs		V_{IH}	2.4	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, All Inputs		V_{IL}	-1.0	0.8	V	1
INPUT LEAKAGE CURRENT Any Input: 0V ≤ V_{IN} ≤ 6.5V (All other pins not under test = 0V)	D9, $\overline{CAS9}$	I_I	-2	2	µA	
	A0-A10, $\overline{WE}$, $\overline{CAS}$, $\overline{RAS}$	I_I	-18	18	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled, 0V ≤ V_{OUT} ≤ 5.5V)	Q9	I_{OZ}	-10	10	µA	
	DQ1-DQ8	I_{OZ}	-12	12	µA	
OUTPUT LEVELS Output High Voltage (I_{OUT} = -5mA)		V_{OH}	2.4		V	
Output Low Voltage (I_{OUT} = 4.2mA)		V_{OL}		0.4	V	

		MAX				
PARAMETER/CONDITION	SYMBOL	-6	-7	-8	UNITS	NOTES
STANDBY CURRENT: (TTL) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC1}	18	18	18	mA	
STANDBY CURRENT: (CMOS)	I_{CC2}	9	9	9	mA	23
($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} -0.2V)		1.8	1.8	1.8	mA	23, 26
OPERATING CURRENT: Random READ/WRITE Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC (MIN))	I_{CC3}	990	900	810	mA	3, 4
OPERATING CURRENT: FAST PAGE MODE Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: ^tPC = ^tPC (MIN))	I_{CC4}	720	630	540	mA	3, 4
REFRESH CURRENT: $\overline{RAS}$-ONLY Average power supply current ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}: ^tRC = ^tRC (MIN))	I_{CC5}	990	900	810	mA	3
REFRESH CURRENT: $\overline{CAS}$-BEFORE-$\overline{RAS}$ Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC (MIN))	I_{CC6}	990	900	810	mA	3, 5
REFRESH CURRENT: BATTERY BACKUP (BBU) Average power supply current during BATTERY BACKUP refresh: $\overline{CAS}$ = 0.2V or $\overline{CAS}$-BEFORE-$\overline{RAS}$ cycling; $\overline{RAS}$ = ^tRAS (MIN) to 300ns; $\overline{WE}$ = V_{CC} -0.2V, A0-A9 and D_{IN} = Vcc - 0.2V or 0.2V (D_{IN} may be left open), ^tRC = 125µs (1,024 rows at 125µs = 128ms)	I_{CC7}	2.7	2.7	2.7	mA	26

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A10	C_{I1}		58	pF	2
Input Capacitance: $\overline{RAS}$, $\overline{WE}$	C_{I2}		76	pF	2
Input Capacitance: D9	C_{I3}		10	pF	2
Input/Output Capacitance: DQ1-DQ8	C_{IO}		15	pF	2
Output Capacitance: Q9	C_O		10	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (V_{CC} = 5V ±10%)

AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	^tRC	110		130		150		ns	
READ-WRITE cycle time	^tRWC	n/a		n/a		n/a		n/a	24
FAST-PAGE-MODE READ or WRITE cycle time	^tPC	40		40		45		ns	
FAST-PAGE-MODE READ-WRITE cycle time	^tPRWC	n/a		n/a		n/a		n/a	24
Access time from $\overline{RAS}$	^tRAC		60		70		80	ns	14
Access time from $\overline{CAS}$	^tCAC		15		20		20	ns	15
Access time from column address	^tAA		30		35		40	ns	
Access time from $\overline{CAS}$ precharge	^tCPA		35		40		45	ns	
$\overline{RAS}$ pulse width	^tRAS	60	100,000	70	100,000	80	100,000	ns	
$\overline{RAS}$ pulse width (FAST PAGE MODE)	^tRASP	60	100,000	70	100,000	80	100,000	ns	
$\overline{RAS}$ hold time	^tRSH	15		20		20		ns	
$\overline{RAS}$ precharge time	^tRP	40		50		60		ns	
$\overline{CAS}$ pulse width	^tCAS	15	100,000	20	100,000	20	100,000	ns	
$\overline{CAS}$ hold time	^tCSH	60		70		80		ns	
$\overline{CAS}$ precharge time	^tCPN	10		10		10		ns	16
$\overline{CAS}$ precharge time (FAST PAGE MODE)	^tCP	10		10		10		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	^tRCD	20	45	20	50	20	60	ns	17
$\overline{CAS}$ to $\overline{RAS}$ precharge time	^tCRP	10		10		10		ns	
Row address setup time	^tASR	0		0		0		ns	
Row address hold time	^tRAH	10		10		10		ns	
$\overline{RAS}$ to column address delay time	^tRAD	15	30	15	35	15	40	ns	18
Column address setup time	^tASC	0		0		0		ns	
Column address hold time	^tCAH	10		15		15		ns	
Column address hold time (referenced to $\overline{RAS}$)	^tAR	50		55		60		ns	
Column address to $\overline{RAS}$ lead time	^tRAL	30		35		40		ns	
Read command setup time	^tRCS	0		0		0		ns	
Read command hold time (referenced to $\overline{CAS}$)	^tRCH	0		0		0		ns	19
Read command hold time (referenced to $\overline{RAS}$)	^tRRH	0		0		0		ns	19
$\overline{CAS}$ to output in Low-Z	^tCLZ	0		0		0		ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

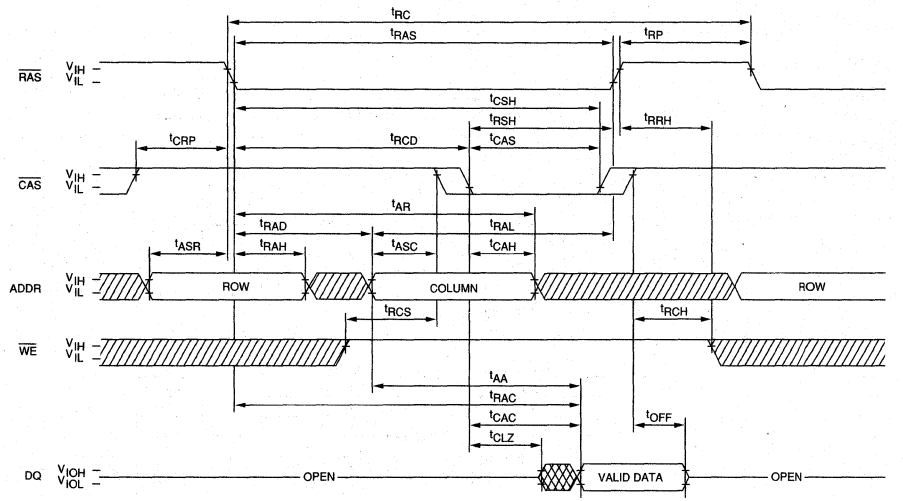
(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (V_{CC} = 5V ±10%)

AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Output buffer turn-off delay	^tOFF	0	15	0	20	0	20	ns	20
$\overline{WE}$ command setup time	^tWCS	0		0		0		ns	
Write command hold time	^tWCH	10		15		15		ns	
Write command hold time (referenced to $\overline{RAS}$)	^tWCR	45		55		60		ns	
Write command pulse width	^tWP	10		15		15		ns	
Write command to $\overline{RAS}$ lead time	^tRWL	15		20		20		ns	
Write command to $\overline{CAS}$ lead time	^tCWL	15		20		20		ns	
Data-in setup time	^tDS	0		0		0		ns	21
Data-in hold time	^tDH	10		15		15		ns	21
Data-in hold time (referenced to $\overline{RAS}$)	^tDHR	45		55		60		ns	
Transition time (rise or fall)	^tT	3	50	3	50	3	50	ns	9, 10
Refresh period (1,024 cycles)	^tREF		16/128		16/128		16/128	ms	7/26
$\overline{RAS}$ to $\overline{CAS}$ precharge time	^tRPC	0		0		0		ns	
$\overline{CAS}$ setup time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH)	^tCSR	10		10		10		ns	5
$\overline{CAS}$ hold time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH)	^tCHR	15		15		15		ns	5
$\overline{WE}$ hold time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tWRH	10		10		10		ns	25
$\overline{WE}$ setup time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tWRP	10		10		10		ns	25
$\overline{WE}$ hold time (WCBR test cycle)	^tWTH	10		10		10		ns	25
$\overline{WE}$ setup time (WCBR test cycle)	^tWTS	10		10		10		ns	25

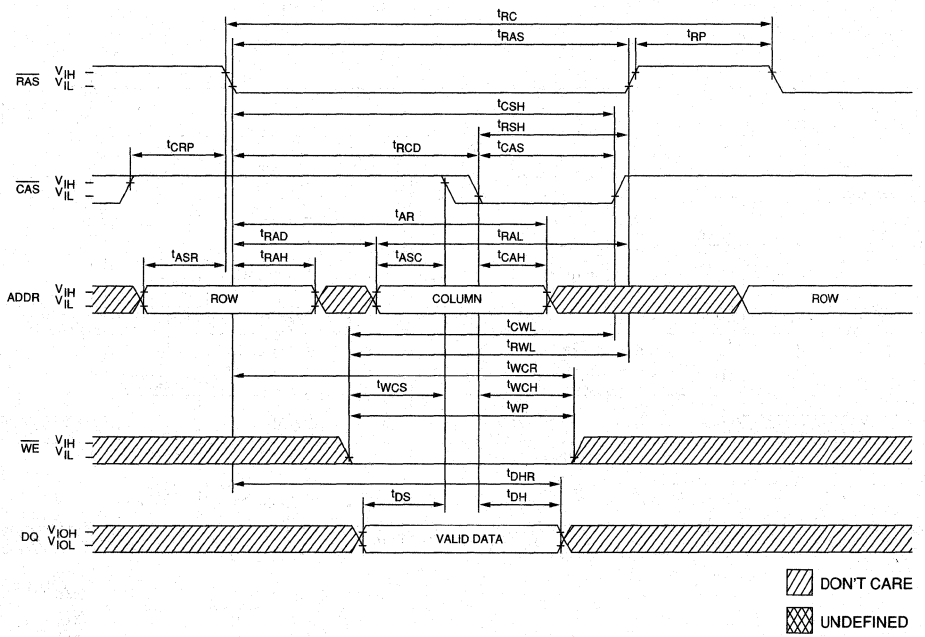
NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. Capacitance is measured using MIL-STD-883C, Method 3012.1 (1 MHz AC, Vcc = 5V, DC bias = 2.4V @ 15mV RMS).
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \leq T_A \leq 70°C$) is assured.
7. An initial pause of 100µs is required after power-up followed by any eight $\overline{RAS}$ refresh cycles ($\overline{RAS}$-ONLY or CBR with $\overline{WE}$ HIGH) before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-up should be repeated any time the ^{t}REF refresh requirement is exceeded.
8. AC characteristics assume ^{t}T = 5ns.
9. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS}$ = V_{IH}, data output is High-Z.
12. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to two TTL gates and 100pF.
14. Assumes that $^{t}RCD < {}^{t}RCD$ (MAX). If ^{t}RCD is greater than the maximum recommended value shown in this table, ^{t}RAC will increase by the amount that ^{t}RCD exceeds the value shown.
15. Assumes that $^{t}RCD \geq {}^{t}RCD$ (MAX).
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer, $\overline{CAS}$ must be pulsed HIGH for ^{t}CPN.
17. Operation within the ^{t}RCD (MAX) limit ensures that ^{t}RAC (MAX) can be met. ^{t}RCD (MAX) is specified as a reference point only; if ^{t}RCD is greater than the specified ^{t}RCD (MAX) limit, then access time is controlled exclusively by ^{t}CAC.
18. Operation within the ^{t}RAD (MAX) limit ensures that ^{t}RCD (MAX) can be met. ^{t}RAD (MAX) is specified as a reference point only; if ^{t}RAD is greater than the specified ^{t}RAD (MAX) limit, then access time is controlled exclusively by ^{t}AA.
19. Either ^{t}RCH or ^{t}RRH must be satisfied for a READ cycle.
20. ^{t}OFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
21. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY-WRITE cycles.
22. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW.
23. All other inputs equal Vcc -0.2V.
24. LATE-WRITE, READ-WRITE or READ-MODIFY-WRITE cycles are not available due to the common DQ configuration of U1-U8.
25. ^{t}WTS and ^{t}WTH are set up and hold specifications for the $\overline{WE}$ pin being held LOW to enable the JEDEC test mode (with CBR timing constraints). These two parameters are the inverts of ^{t}WRP and ^{t}WRH in the CBR refresh cycle.
26. Applies to L-version only.

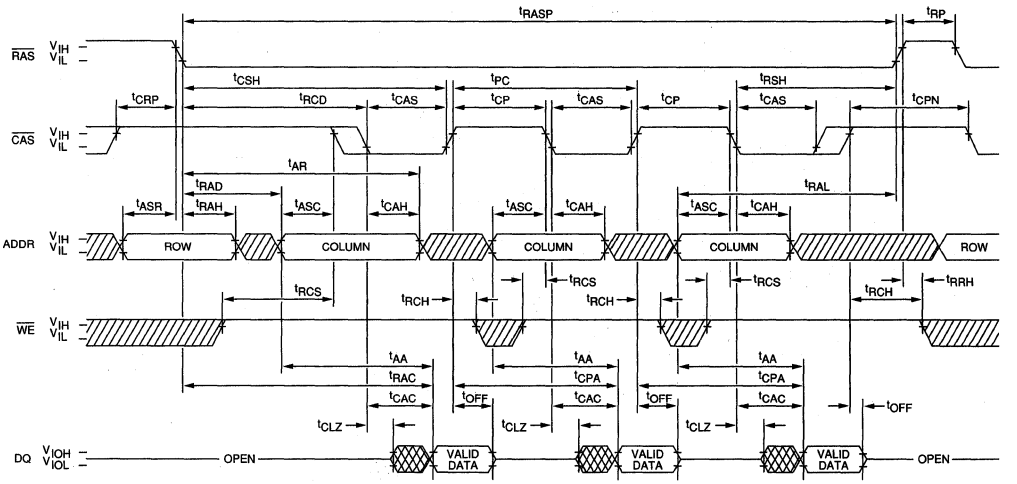
READ CYCLE



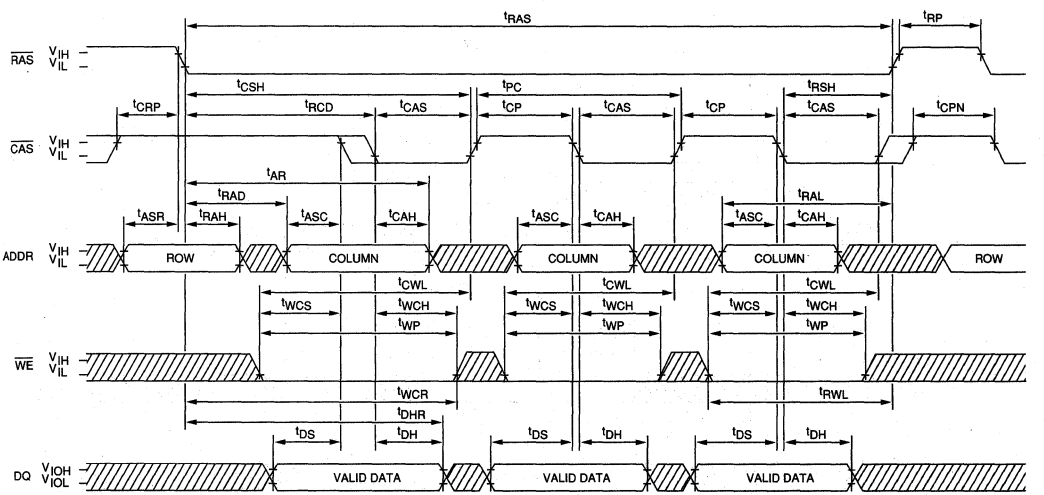
EARLY-WRITE CYCLE



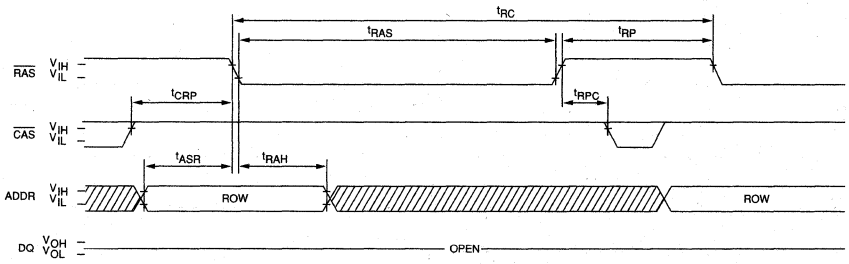
FAST-PAGE-MODE READ CYCLE



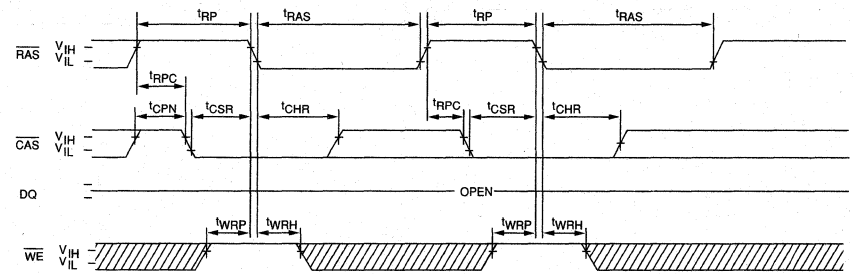
FAST-PAGE-MODE EARLY-WRITE CYCLE



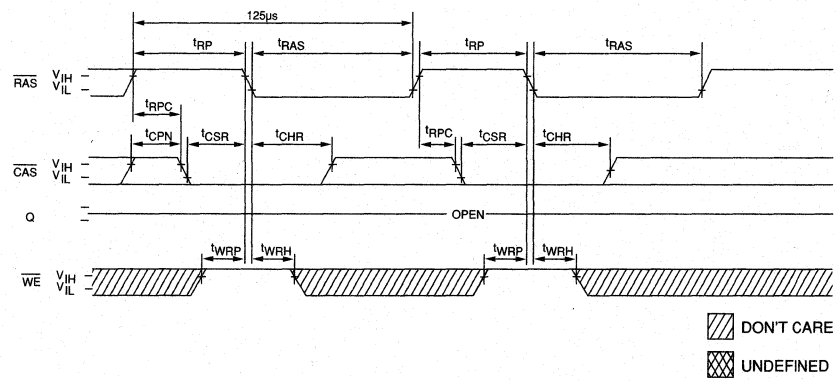
$\overline{\text{RAS}}$-ONLY REFRESH CYCLE
(ADDR = A0-A9; A10 and $\overline{\text{WE}}$ = DON'T CARE)



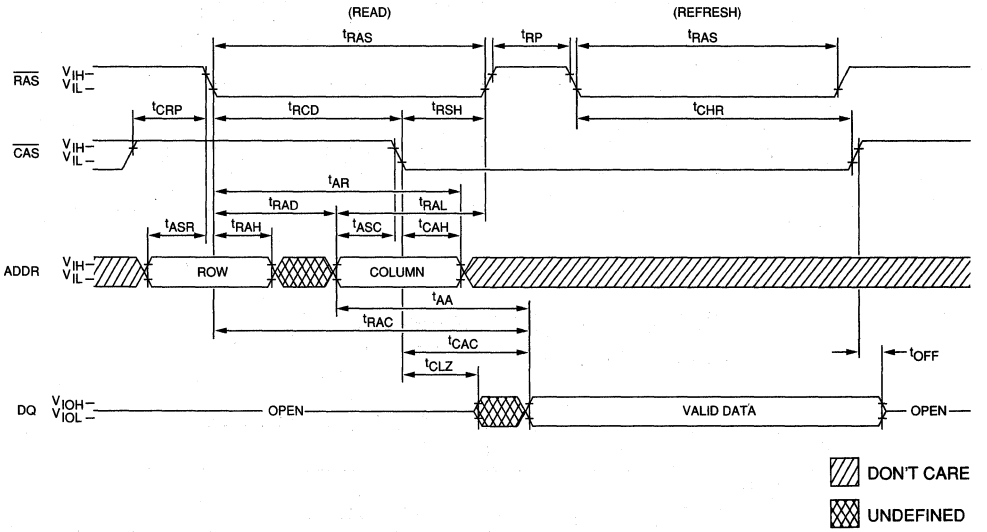
$\overline{\text{CAS}}$-BEFORE-$\overline{\text{RAS}}$ REFRESH CYCLE
(A0-A10 = DON'T CARE)



BATTERY BACKUP REFRESH CYCLE [26]
(A0-A10 = DON'T CARE)



HIDDEN REFRESH CYCLE [22]
($\overline{WE}$ = HIGH)



DRAM MODULE

16 MEG x 9 DRAM

FAST PAGE MODE

NEW DRAM MODULE

FEATURES

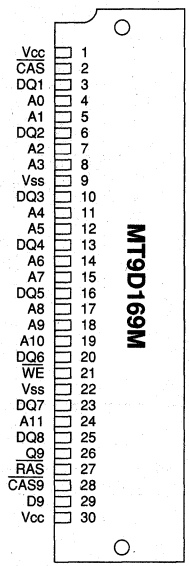
- Industry standard pinout in a 30-pin single-in-line package
- High-performance, CMOS silicon-gate process
- Single 5V ±10% power supply
- All device pins are fully TTL compatible
- Low power, 27mW standby; 2,475mW active, typical
- Refresh modes: RAS-ONLY, CAS-BEFORE-RAS (CBR) and HIDDEN
- 4,096-cycle refresh distributed across 64ms
- FAST PAGE MODE access cycle

OPTIONS MARKING

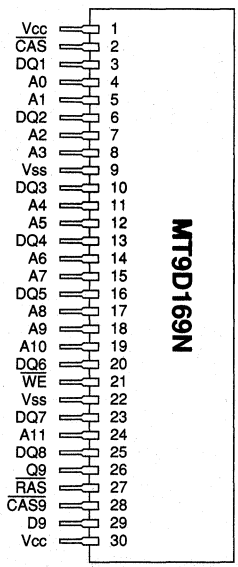
- Timing
  - 60ns access -6
  - 70ns access -7
  - 80ns access -8
- Packages
  - Leadless 30-pin SIMM M
  - Leaded 30-pin SIP N
- Part Number Example: MT9D169M-6

PIN ASSIGNMENT (Top View)

30-Pin SIMM (T-8)



30-Pin SIP (S-8)



GENERAL DESCRIPTION

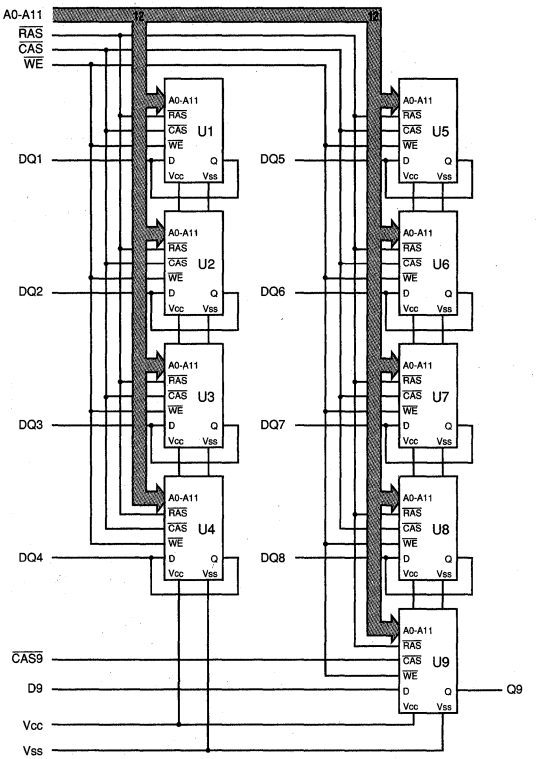
The MT9D169 is a randomly accessed solid-state memory containing 16,777,216 words organized in a x9 configuration. During READ or WRITE cycles, each bit is uniquely addressed through the 24 address bits which are entered 12 bits (A0-A11) at a time. RAS is used to latch the first 12 bits and CAS the latter 12 bits. A READ or WRITE cycle is selected with the WE input. A logic HIGH on WE dictates READ mode, while a logic LOW on WE dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of CAS. Since WE goes LOW prior to CAS going LOW, the output pin(s) remain open (High-Z) until the next CAS cycle.

FAST PAGE MODE operations allow faster data operations (READ or WRITE) within a row-address (A0-A11) defined page boundary. The FAST PAGE MODE cycle is always initiated with a row address strobed-in by RAS followed by a column address strobed-in by CAS. CAS may be toggled-in by holding RAS LOW and strobing-in different column addresses, thus executing faster memory cycles. Returning RAS HIGH terminates the FAST PAGE MODE operation.

Returning RAS and CAS HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the RAS high time. Memory cell data is retained in its correct state by maintaining power and executing any RAS cycle (READ, WRITE, RAS-ONLY, CAS-BEFORE-RAS or HIDDEN REFRESH) so that all 4,096 combinations of RAS addresses (A0-A11) are executed at least every 64ms, regardless of sequence. The CBR refresh cycle will invoke the refresh counter for automatic RAS addressing.

NEW ■ DRAM MODULE

FUNCTIONAL BLOCK DIAGRAM



U1-U9 = MT4C16M1A1DJ

TRUTH TABLE

FUNCTION		RAS	CAS	CAS9	WE	ADDRESSES		DATA IN/OUT
						^tR	^tC	DQ1-DQ8, D9, Q9
Standby		H	H→X	H→X	X	X	X	High-Z
READ		L	L	L	H	ROW	COL	Data Out
EARLY-WRITE		L	L	L	L	ROW	COL	Data In
FAST-PAGE-MODE	1st Cycle	L	H→L	H→L	H	ROW	COL	Data Out
READ	2nd Cycle	L	H→L	H→L	H	n/a	COL	Data Out
FAST-PAGE-MODE	1st Cycle	L	H→L	H→L	L	ROW	COL	Data In
WRITE	2nd Cycle	L	H→L	H→L	L	n/a	COL	Data In
RAS-ONLY REFRESH		L	H	H	X	ROW	n/a	High-Z
HIDDEN	READ	L→H→L	L	L	H	ROW	COL	Data Out
REFRESH	WRITE	L→H→L	L	L	L	ROW	COL	Data In
CAS-BEFORE-RAS REFRESH		H→L	L	L	H	X	X	High-Z

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} ..... -1V to +7V
Operating Temperature, T_A (Ambient) ..... 0°C to +70°C
Storage Temperature (Plastic) ..... -55°C to +125°C
Power Dissipation 9W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

NEW DRAM MODULE

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 3, 4, 6, 7) (0°C ≤ T_A ≤ 70°C; V_{CC} = 5V ±10%)

PARAMETER/CONDITION		SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage		V_{CC}	4.5	5.5	V	1
Input High (Logic 1) Voltage, All Inputs		V_{IH}	2.4	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, All Inputs		V_{IL}	-1.0	0.8	V	1
INPUT LEAKAGE CURRENT Any Input: 0V ≤ V_{IN} ≤ 6.5V (All other pins not under test = 0V)	A0-A11, $\overline{WE}$, $\overline{RAS}$	I_I	-18	18	µA	
	D9, $\overline{CAS9}$	I_I	-2	2	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled, 0V ≤ V_{OUT} ≤ 5.5V)	DQ1-DQ8, Q9	I_{OZ}	-10	10	µA	
OUTPUT LEVELS Output High Voltage (I_{OUT} = -5mA)		V_{OH}	2.4		V	
Output Low Voltage (I_{OUT} = 4.2mA)		V_{OL}		0.4	V	

		MAX				
PARAMETER/CONDITION	SYMBOL	-6	-7	-8	UNITS	NOTES
STANDBY CURRENT (TTL) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC1}	18	18	18	mA	
STANDBY CURRENT (CMOS) ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} -0.2V)	I_{CC2}	9	9	9	mA	
OPERATING CURRENT: Random READ/WRITE Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC (MIN))	I_{CC3}	810	720	630	mA	3, 4
OPERATING CURRENT: FAST PAGE MODE Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: ^tPC = ^tPC (MIN))	I_{CC4}	630	540	450	mA	3, 4
REFRESH CURRENT: $\overline{RAS}$-ONLY Average power supply current ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}: ^tRC = ^tRC (MIN))	I_{CC5}	810	720	630	mA	3
REFRESH CURRENT: $\overline{CAS}$-BEFORE-$\overline{RAS}$ Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC (MIN))	I_{CC6}	810	720	630	mA	3

NEW ■ DRAM MODULE

CAPACITANCE

DESCRIPTION	SYMBOL	MAX	UNITS	NOTES
Input Capacitance: A0-A11	C_{I1}	58	pF	2
Input Capacitance: $\overline{RAS}$, $\overline{WE}$, $\overline{CAS}$	C_{I2}	76	pF	2
Input/Output Capacitance: DQ1-DQ8	C_{IO}	15	pF	2
Input Capacitance: D9, $\overline{CAS9}$	C_{I3}	10	pF	2
Output Capacitance: Q9	C_O	10	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (V_{CC} = 5V ±10%)

AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	^tRC	110		130		150		ns	
READ-WRITE cycle time	^tRWC	n/a		n/a		n/a		ns	22
FAST-PAGE-MODE READ or WRITE cycle time	^tPC	35		40		40		ns	
FAST-PAGE-MODE READ-WRITE cycle time	^tPRWC	n/a		n/a		n/a		ns	22
Access time from $\overline{RAS}$	^tRAC		60		70		80	ns	14
Access time from $\overline{CAS}$	^tCAC		15		20		20	ns	15
Access time from column address	^tAA		30		35		40	ns	
Access time from $\overline{CAS}$ precharge	^tCPA		35		40		45	ns	
$\overline{RAS}$ pulse width	^tRAS	60	100,000	70	100,000	80	100,000	ns	
$\overline{RAS}$ pulse width (FAST PAGE MODE)	^tRASP	60	100,000	70	100,000	80	100,000	ns	
$\overline{RAS}$ hold time	^tRSH	15		20		20		ns	
$\overline{RAS}$ precharge time	^tRP	40		50		60		ns	
$\overline{CAS}$ pulse width	^tCAS	15	100,000	20	100,000	20	100,000	ns	
$\overline{CAS}$ hold time	^tCSH	60		70		80		ns	
$\overline{CAS}$ precharge time	^tCPN	10		10		10		ns	16
$\overline{CAS}$ precharge time (FAST PAGE MODE)	^tCP	10		10		10		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	^tRCD	15	45	20	50	20	60	ns	17
$\overline{CAS}$ to $\overline{RAS}$ precharge time	^tCRP	5		5		5		ns	
Row address setup time	^tASR	0		0		0		ns	
Row address hold time	^tRAH	10		10		10		ns	
$\overline{RAS}$ to column address delay time	^tRAD	15	30	15	35	15	40	ns	18
Column address setup time	^tASC	0		0		0		ns	
Column address hold time	^tCAH	10		15		15		ns	
Column address hold time (referenced to $\overline{RAS}$)	^tAR	50		55		60		ns	
Column address to $\overline{RAS}$ lead time	^tRAL	30		35		40		ns	
Read command setup time	^tRCS	0		0		0		ns	
Read command hold time (referenced to $\overline{CAS}$)	^tRCH	0		0		0		ns	19
Read command hold time (referenced to $\overline{RAS}$)	^tRRH	0		0		0		ns	19

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (V_{CC} = 5V ±10%)

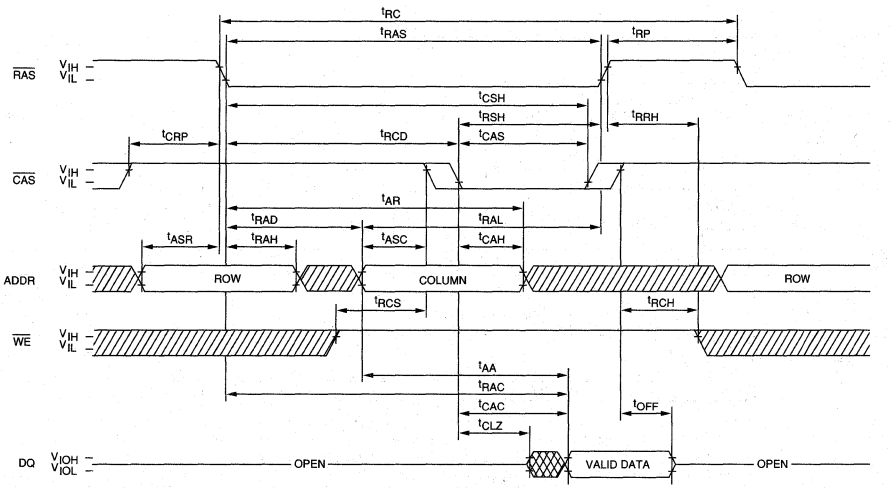
AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
$\overline{CAS}$ to output in Low-Z	^tCLZ	0		0		0		ns	
Output buffer turn-off delay	^tOFF	5	15	5	15	5	15	ns	20
$\overline{WE}$ command setup time	^tWCS	0		0		0		ns	
Write command hold time	^tWCH	10		15		15		ns	
Write command hold time (referenced to $\overline{RAS}$)	^tWCR	45		55		60		ns	
Write command pulse width	^tWP	10		15		15		ns	
Write command to $\overline{RAS}$ lead time	^tRWL	15		20		20		ns	
Write command to $\overline{CAS}$ lead time	^tCWL	15		20		20		ns	
Data-in setup time	^tDS	0		0		0		ns	21
Data-in hold time	^tDH	10		15		15		ns	21
Data-in hold time (referenced to $\overline{RAS}$)	^tDHR	45		55		60		ns	
Transition time (rise or fall)	^tT	3	50	3	50	3	50	ns	9, 10
Refresh period (4,096 cycles)	^tREF		64		64		64	ms	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	^tRPC	0		0		0		ns	
$\overline{CAS}$ setup time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tCSR	5		5		5		ns	5
$\overline{CAS}$ hold time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tCHR	15		15		15		ns	5
$\overline{WE}$ hold time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tWRH	10		10		10		ns	24
$\overline{WE}$ setup time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tWRP	10		10		10		ns	24
$\overline{WE}$ hold time (WCBR test cycle)	^tWTH	10		10		10		ns	24
$\overline{WE}$ setup time (WCBR test cycle)	^tWTS	10		10		10		ns	24

NEW DRAM MODULE

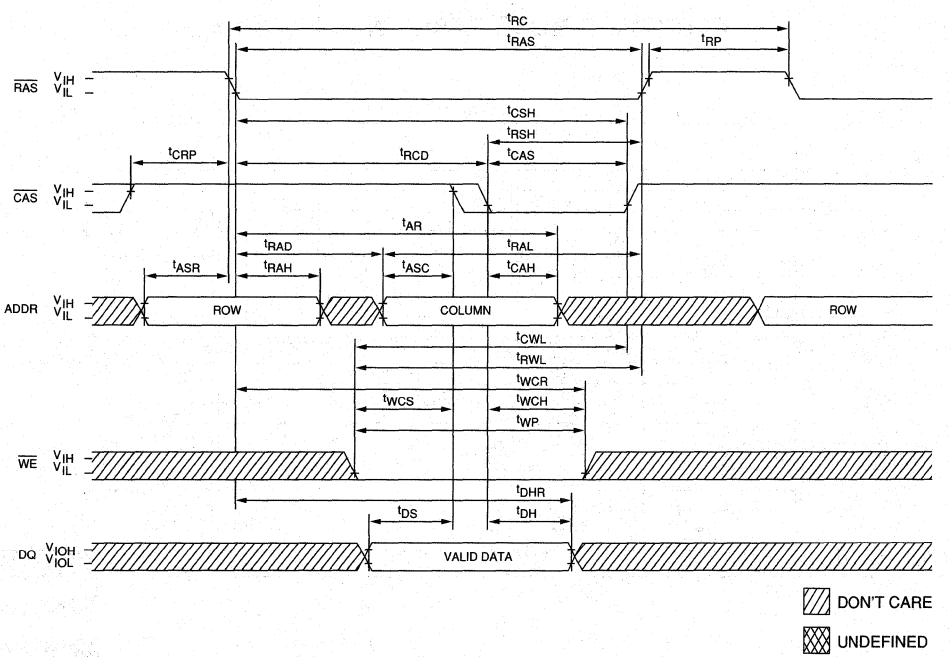
NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. Capacitance is measured using MIL-STD-883C, Method 3012.1 (1 MHz AC, Vcc = 5V, DC bias = 2.4V @ 15mV RMS)
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is assured.
7. An initial pause of 100µs is required after power-up followed by eight $\overline{RAS}$ refresh cycles ($\overline{RAS}$-ONLY or CBR with $\overline{WE}$ HIGH) before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-up should be repeated any time the ^{t}REF refresh requirement is exceeded.
8. AC characteristics assume ^{t}T = 5ns.
9. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS}$ = V_{IH}, data output is High-Z.
12. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to 2 TTL gates and 100pF.
14. Assumes that $^{t}RCD < {}^{t}RCD$ (MAX). If ^{t}RCD is greater than the maximum recommended value shown in this table, ^{t}RAC will increase by the amount that ^{t}RCD exceeds the value shown.
15. Assumes that $^{t}RCD \geq {}^{t}RCD$ (MAX).
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer, $\overline{CAS}$ must be pulsed HIGH for ^{t}CPN.
17. Operation within the ^{t}RCD (MAX) limit ensures that ^{t}RAC (MAX) can be met. ^{t}RCD (MAX) is specified as a reference point only; if ^{t}RCD is greater than the specified ^{t}RCD (MAX) limit, then access time is controlled exclusively by ^{t}CAC.
18. Operation within the ^{t}RAD (MAX) limit ensures that ^{t}RCD (MAX) can be met. ^{t}RAD (MAX) is specified as a reference point only; if ^{t}RAD is greater than the specified ^{t}RAD (MAX) limit, then access time is controlled exclusively by ^{t}AA.
19. Either ^{t}RCH or ^{t}RRH must be satisfied for a READ cycle.
20. ^{t}OFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
21. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY-WRITE cycles.
22. LATE-WRITE, READ-WRITE or READ-MODIFY-WRITE cycles are not available due to the common DQ configuration of U1-U8.
23. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW and $\overline{OE}$ = HIGH.
24. ^{t}WTS and ^{t}WTH are setup and hold specifications for the $\overline{WE}$ pin being held LOW to enable the JEDEC test mode (with CBR timing constraints). These two parameters are the inverts of ^{t}WRP and ^{t}WRH in the CBR refresh cycle.

READ CYCLE

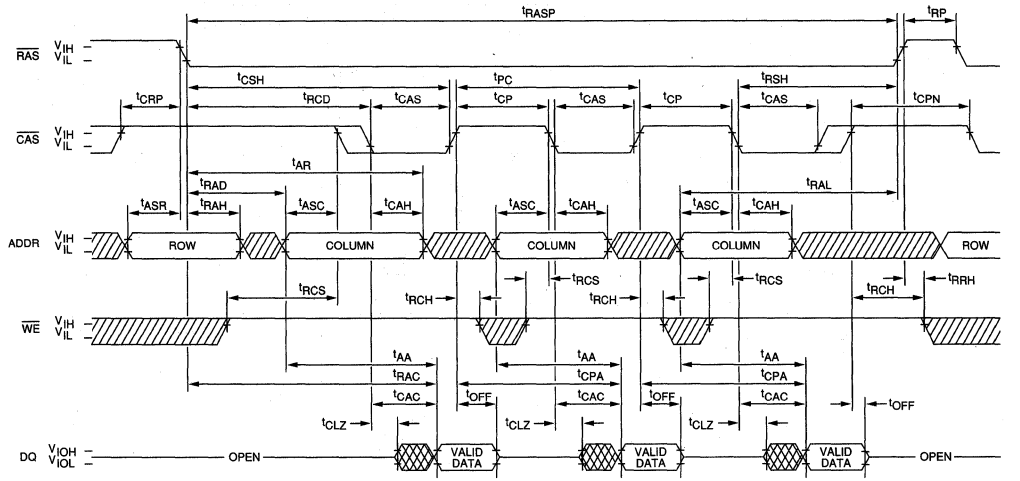


EARLY-WRITE CYCLE

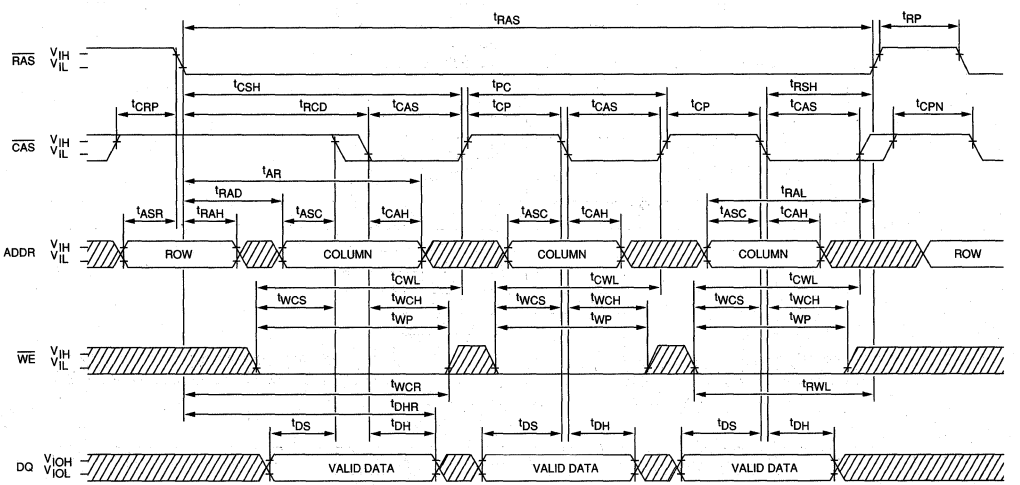


NEW DRAM MODULE

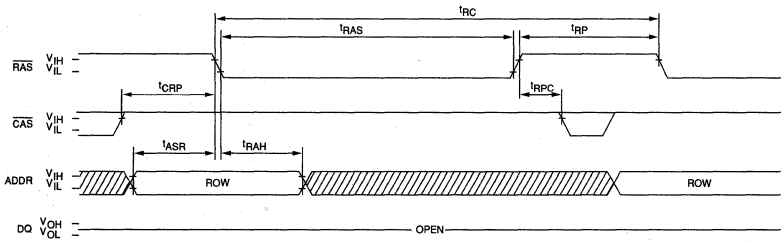
FAST-PAGE-MODE READ CYCLE



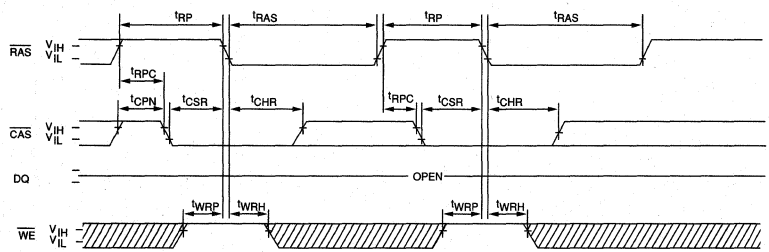
FAST-PAGE-MODE EARLY-WRITE CYCLE



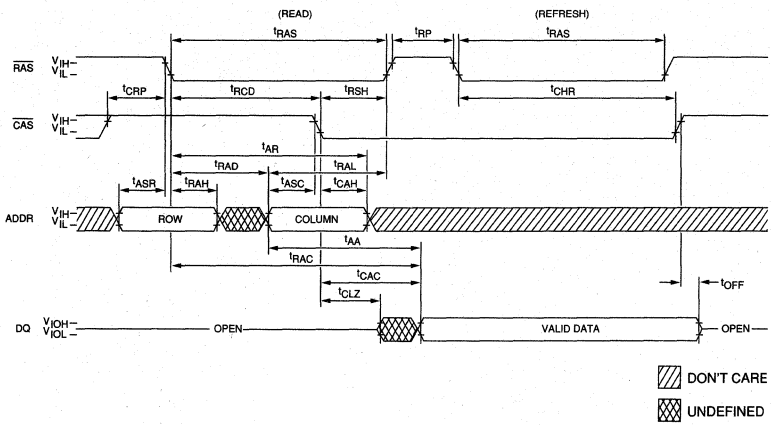
$\overline{RAS}$-ONLY REFRESH CYCLE
(ADDR = A0-A11; $\overline{WE}$ = DON'T CARE)



$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE
(A0-A11 = DON'T CARE)



HIDDEN REFRESH CYCLE [23]
($\overline{WE}$ = HIGH)



MICRON TECHNOLOGY, INC.

MT9D169
16 MEG x 9 DRAM MODULE

DRAM MODULE

256K x 32, 512K x 16

FAST PAGE MODE (MT8D25632)
LOW POWER,
EXTENDED REFRESH (MT8D25632 L)

FEATURES

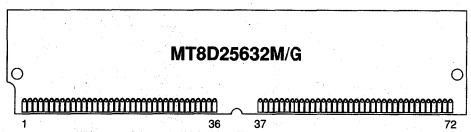
- Industry standard pinout in a 72-pin single-in-line package
- High-performance, CMOS silicon-gate process.
- Single 5V ±10% power supply
- All device pins are fully TTL compatible
- Low power, 24mW (2.4mW L-version) standby; 1,400mW active, typical
- Multiple $\overline{RAS}$ lines offer x16 or x32 widths
- Refresh modes: $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$ (CBR) and HIDDEN
- 512-cycle refresh distributed across 8ms or 512-cycle extended refresh distributed across 64ms
- FAST PAGE MODE access cycle
- Low CMOS standby current, 1.6mA maximum (L-version)

OPTIONS MARKING

- Timing
  - 60ns access - 6
  - 70ns access - 7
  - 80ns access - 8
- Packages
  - Leadless 72-pin SIMM M
  - Leadless 72-pin SIMM (Gold) G
- Power/Refresh
  - Normal Power/8ms Blank
  - Low Power/64ms L
- Part Number Example: MT8D25632ML-6

PIN ASSIGNMENT (Top View)

72-Pin SIMM
(T-9)



PIN #	SYMBOL	PIN #	SYMBOL	PIN #	SYMBOL	PIN #	SYMBOL
1	Vss	19	NC	37	NC	55	DQ12
2	DQ1	20	DQ5	38	NC	56	DQ28
3	DQ17	21	DQ21	39	Vss	57	DQ13
4	DQ2	22	DQ6	40	$\overline{CAS0}$	58	DQ29
5	DQ18	23	DQ22	41	$\overline{CAS2}$	59	Vcc
6	DQ3	24	DQ7	42	$\overline{CAS3}$	60	DQ30
7	DQ19	25	DQ23	43	$\overline{CAS1}$	61	DQ14
8	DQ4	26	DQ8	44	$\overline{RAS0}$	62	DQ31
9	DQ20	27	DQ24	45	NC	63	DQ15
10	Vcc	28	A7	46	NC	64	DQ32
11	NC	29	NC	47	$\overline{WE}$	65	DQ16
12	A0	30	Vcc	48	NC	66	NC
13	A1	31	A8	49	DQ9	67	PRD1
14	A2	32	NC	50	DQ25	68	PRD2
15	A3	33	NC	51	DQ10	69	PRD3
16	A4	34	$\overline{RAS2}$	52	DQ26	70	PRD4
17	A5	35	NC	53	DQ11	71	NC
18	A6	36	NC	54	DQ27	72	Vss

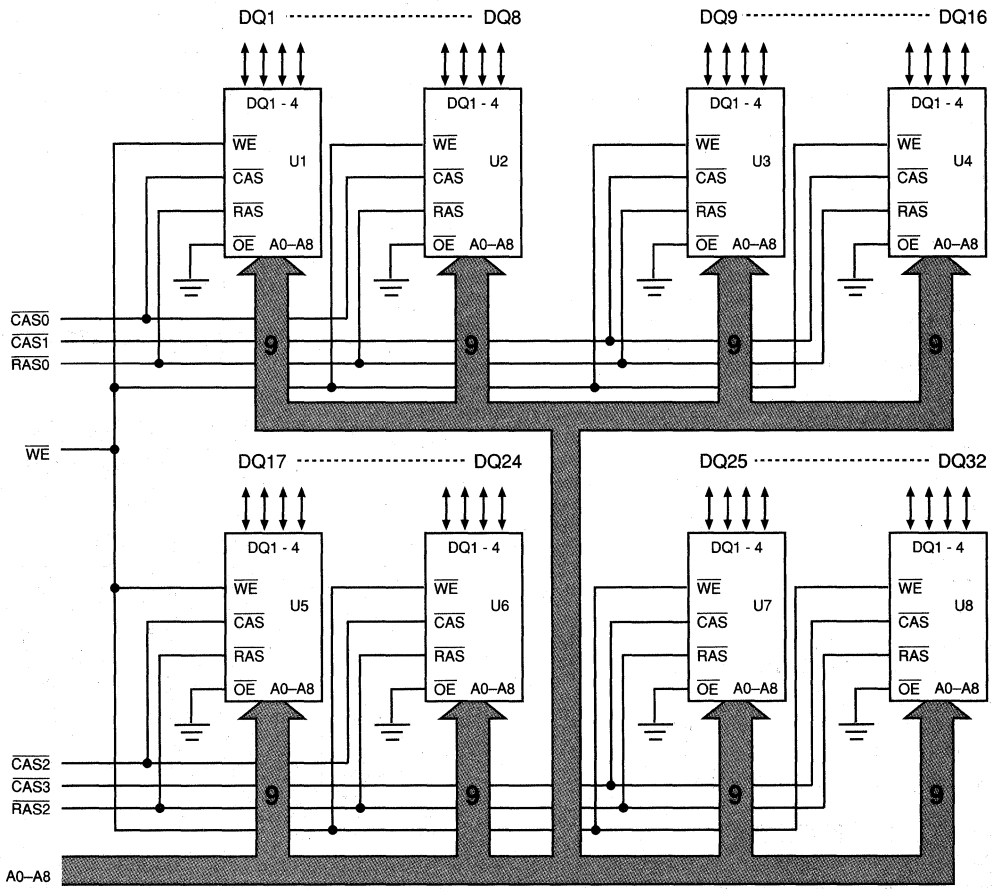
GENERAL DESCRIPTION

The MT8D25632 is a randomly accessed solid-state memory containing 262,144 words organized in a x32 configuration. During READ or WRITE cycles, each bit is uniquely addressed through the 18 address bits which are entered 9 bits (A0-A8) at a time. $\overline{RAS}$ is used to latch the first 9 bits and $\overline{CAS}$ the latter 9 bits. A READ or WRITE cycle is selected with the $\overline{WE}$ input. A logic HIGH on $\overline{WE}$ dictates READ mode while a logic LOW on $\overline{WE}$ dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. If $\overline{WE}$ goes LOW prior to $\overline{CAS}$ going LOW, the output pin(s) remain open (High-Z) until the next $\overline{CAS}$ cycle.

FAST PAGE MODE operations allow faster data operations (READ or WRITE) within a row-address (A0-A8) defined page boundary. The FAST PAGE MODE cycle is always initiated with a row address strobed-in by $\overline{RAS}$ followed by a column address strobed-in by $\overline{CAS}$. $\overline{CAS}$ may be toggled-in by holding $\overline{RAS}$ LOW and strobing-in different column addresses, thus executing faster memory cycles. Returning $\overline{RAS}$ HIGH terminates the FAST PAGE MODE operation.

Returning $\overline{RAS}$ and $\overline{CAS}$ HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the $\overline{RAS}$ HIGH time. Memory cell data is retained in its correct state by maintaining power and executing any $\overline{RAS}$ cycle (READ, WRITE, $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$ or HIDDEN REFRESH) so that all 512 combinations of $\overline{RAS}$ addresses (A0-A8) are executed at least every 8ms (64ms on L-version), regardless of sequence.

FUNCTIONAL BLOCK DIAGRAM



U1-U8 = MT4C4256DJ
U1-U8 = MT4C4256DJ L (L-version)

TRUTH TABLE

FUNCTION		RAS	CAS	WE	ADDRESSES		DATA IN/OUT
					^tR	^tC	DQ1-DQ32
Standby		H	H→X	X	X	X	High-Z
READ		L	L	H	ROW	COL	Data Out
EARLY-WRITE		L	L	L	ROW	COL	Data In
FAST-PAGE-MODE	1st Cycle	L	H→L→H	H	ROW	COL	Data Out
READ	2nd Cycle	L	H→L→H	H	n/a	COL	Data Out
FAST-PAGE-MODE	1st Cycle	L	H→L→H	L	ROW	COL	Data In
WRITE	2nd Cycle	L	H→L→H	L	n/a	COL	Data In
RAS-ONLY REFRESH		L	H	X	ROW	n/a	High-Z
HIDDEN	READ	L→H→L	L	H	ROW	COL	Data Out
REFRESH	WRITE	L→H→L	L	L	ROW	COL	Data In
CAS-BEFORE-RAS REFRESH		H→L	L	X	X	X	High-Z
BATTERY BACKUP REFRESH (L-version)		H→L	L	X	X	X	High-Z

PRESENCE DETECT

SYMBOL	-6	-7	-8
PRD1	Vss	Vss	Vss
PRD2	NC	NC	NC
PRD3	NC	Vss	NC
PRD4	NC	NC	Vss

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} ..... -1V to +7V
Operating Temperature, T_A (Ambient) ..... 0°C to +70°C
Storage Temperature (Plastic) ..... -55°C to +125°C
Power Dissipation 8W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 2, 3, 6, 22) (0°C ≤ T_A ≤ 70°C; V_{CC} = 5V ±10%)

PARAMETER/CONDITION		SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage		V_{CC}	4.5	5.5	V	1
Input High (Logic 1) Voltage, All Inputs		V_{IH}	2.4	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, All Inputs		V_{IL}	-1.0	0.8	V	1
INPUT LEAKAGE CURRENT	$\overline{RAS0}$, $\overline{RAS2}$	I_{I1}	-8	8	µA	
Any input: 0V ≤ V_{IN} ≤ V_{CC}	A0-A8, $\overline{WE}$	I_{I2}	-16	16	µA	
(All other pins not under test = 0V) For each package input	$\overline{CAS0}$-$\overline{CAS3}$	I_{I3}	-4	4	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled, 0V ≤ V_{OUT} ≤ V_{CC}) For each package input	DQ1-DQ32	I_{OZ}	-10	10	µA	
OUTPUT LEVELS		V_{OH}	2.4		V	
Output High Voltage (I_{OUT} = -5mA)						
Output Low Voltage (I_{OUT} = 5mA)		V_{OL}		0.4	V	

PARAMETER/CONDITION	SYMBOL	MAX -6	MAX -7	MAX -8	UNITS	NOTES
STANDBY CURRENT: (TTL) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC1}	16	16	16	mA	
STANDBY CURRENT: (CMOS)	I_{CC2}	8	8	8	mA	
($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} -0.2V)		1.6	1.6	1.6	mA	24
OPERATING CURRENT: Random READ/WRITE Average power supply current	I_{CC3}	720	640	560	mA	2, 22
($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC (MIN))		680	600	520	mA	2,22,24
OPERATING CURRENT: FAST PAGE MODE Average power supply current	I_{CC4}	560	480	400	mA	2, 22
($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: ^tPC = ^tPC (MIN))		520	440	360	mA	2,22,24
REFRESH CURRENT: $\overline{RAS}$-ONLY Average power supply current	I_{CC5}	720	640	560	mA	2
($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}: ^tRC = ^tRC (MIN))		680	600	520	mA	2, 24
REFRESH CURRENT: $\overline{CAS}$-BEFORE-$\overline{RAS}$ Average power supply current	I_{CC6}	720	640	560	mA	2, 19
($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC (MIN))		680	600	520	mA	2,19,24
REFRESH CURRENT: BATTERY BACKUP (BBU) Average power supply current during BATTERY BACKUP refresh: $\overline{CAS}$ = 0.2V or $\overline{CAS}$-BEFORE-$\overline{RAS}$ cycling; $\overline{RAS}$ = ^tRAS (MIN) to 1µs; $\overline{WE}$, A0-A9 and D_{IN} = V_{CC} -0.2V or 0.2V (D_{IN} may be left OPEN), ^tRC = 125µs (512 rows at 125µs = 64ms)	I_{CC7}	1.6	1.6	1.6	mA	24

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A8	C_{I1}		51	pF	17
Input Capacitance: $\overline{WE}$	C_{I2}		67	pF	17
Input Capacitance: $\overline{RAS0}$	C_{I3}		34	pF	17
Input Capacitance: $\overline{CAS0}$-$\overline{CAS3}$	C_{I4}		17	pF	17
Input/Output Capacitance: DQ1-DQ32	C_{IO}		10	pF	17

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 3, 4, 5, 6, 7, 10, 11, 16, 21) ($0°C \le T_A \le 70°C$; V_{CC} = 5V ±10%)

AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	^tRC	110		130		150		ns	
READ-WRITE cycle time	^tRWC	n/a		n/a		n/a		ns	21
FAST-PAGE-MODE READ or WRITE cycle time	^tPC	40		40		45		ns	
FAST-PAGE-MODE READ-WRITE cycle time	^tPRWC	n/a		n/a		n/a		ns	21
Access time from $\overline{RAS}$	^tRAC		60		70		80	ns	8
Access time from $\overline{CAS}$	^tCAC		20		20		20	ns	9
Output Enable	^tOE		20		20		20	ns	
Access time from column address	^tAA		30		35		40	ns	
Access time from $\overline{CAS}$ precharge	^tCPA		35		40		45	ns	
$\overline{RAS}$ pulse width	^tRAS	60	100,000	70	100,000	80	100,000	ns	
$\overline{RAS}$ pulse width (FAST PAGE MODE)	^tRASP	60	100,000	70	100,000	80	100,000	ns	
$\overline{RAS}$ hold time	^tRSH	20		20		20		ns	
$\overline{RAS}$ precharge time	^tRP	40		50		60		ns	
$\overline{CAS}$ pulse width	^tCAS	20	100,000	20	100,000	20	100,000	ns	
$\overline{CAS}$ hold time	^tCSH	60		70		80		ns	
$\overline{CAS}$ precharge time	^tCPN	10		10		10		ns	18
$\overline{CAS}$ precharge time (FAST PAGE MODE)	^tCP	10		10		10		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	^tRCD	20	40	20	50	20	60	ns	13
$\overline{CAS}$ to $\overline{RAS}$ precharge time	^tCRP	5		5		5		ns	
Row address setup time	^tASR	0		0		0		ns	
Row address hold time	^tRAH	10		10		10		ns	
$\overline{RAS}$ to column address delay time	^tRAD	15	30	15	35	15	40	ns	23
Column address setup time	^tASC	0		0		0		ns	
Column address hold time	^tCAH	15		15		15		ns	
Column address hold time (referenced to $\overline{RAS}$)	^tAR	45		55		60		ns	
Column address to $\overline{RAS}$ lead time	^tRAL	30		35		40		ns	
Read command setup time	^tRCS	0		0		0		ns	
Read command hold time (referenced to $\overline{CAS}$)	^tRCH	0		0		0		ns	14
Read command hold time (referenced to $\overline{RAS}$)	^tRRH	0		0		0		ns	14

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

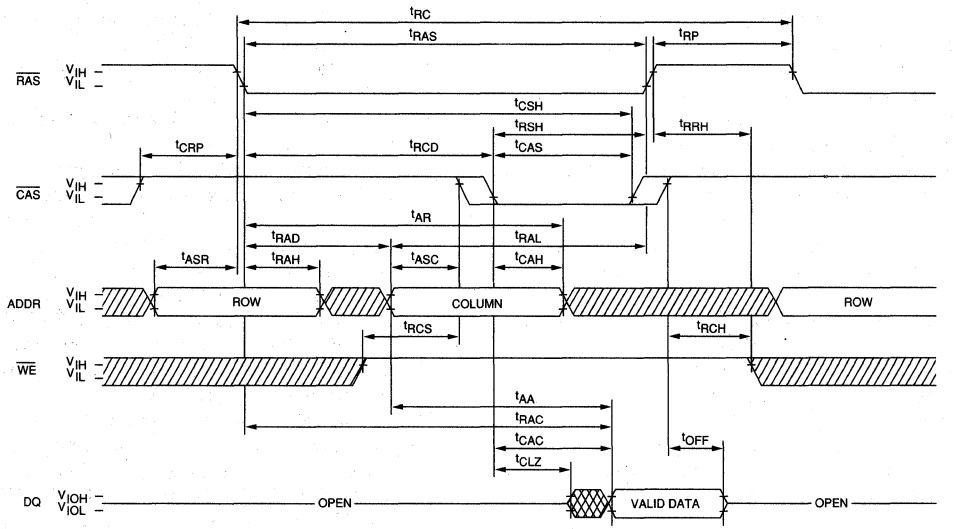
(Notes: 3, 4, 5, 6, 7, 10, 11, 16, 21) (0°C ≤ T_A ≤ 70°C; Vcc = 5V ±10%)

AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
$\overline{CAS}$ to output in Low-Z	^tCLZ	0		0		0		ns	
Output buffer turn-off delay	^tOFF	0	20	0	20	0	20	ns	12
$\overline{WE}$ command setup time	^tWCS	0		0		0		ns	
Write command hold time	^tWCH	10		15		15		ns	
Write command hold time (referenced to $\overline{RAS}$)	^tWCR	45		55		60		ns	
Write command pulse width	^tWP	10		15		15		ns	
Write command to $\overline{RAS}$ lead time	^tRWL	20		20		20		ns	
Write command to $\overline{CAS}$ lead time	^tCWL	20		20		20		ns	
Data-in setup time	^tDS	0		0		0		ns	15
Data-in hold time	^tDH	15		15		15		ns	15
Data-in hold time (referenced to $\overline{RAS}$)	^tDHR	45		55		60		ns	
Transition time (rise or fall)	^tT	3	50	3	50	3	50	ns	5, 16
Refresh period (512 cycles)	^tREF		8/64		8/64		8/64	ms	3/24
$\overline{RAS}$ to $\overline{CAS}$ precharge time	^tRPC	0		0		0		ns	
$\overline{CAS}$ setup time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tCSR	10		10		10		ns	19
$\overline{CAS}$ hold time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tCHR	15		15		15		ns	19

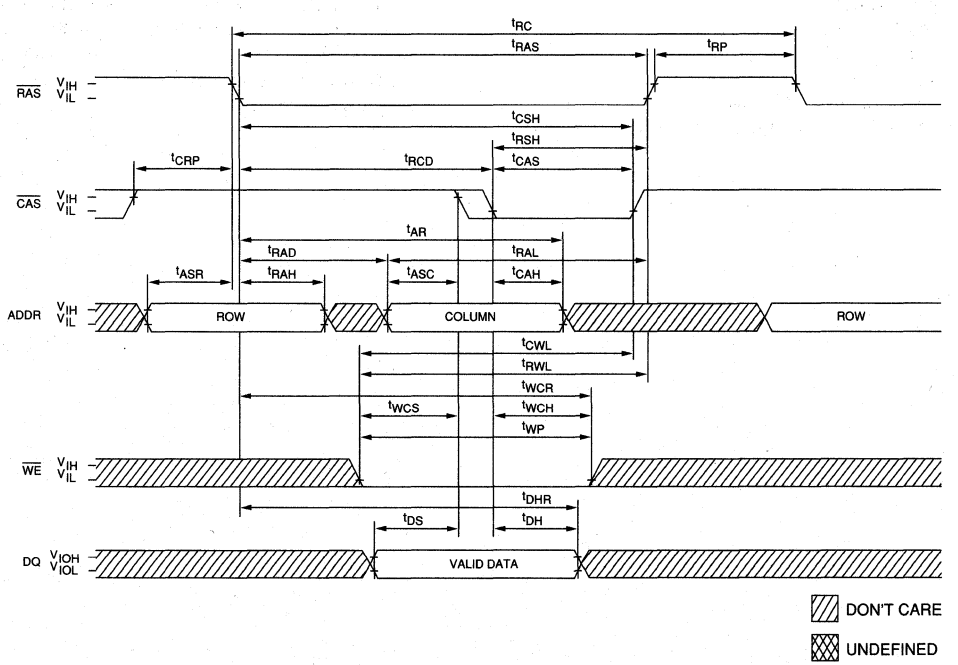
NOTES

1. All voltages referenced to V_{SS}.
2. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
3. An initial pause of 100µs is required after power-up followed by any eight $\overline{RAS}$ cycles before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-up should be repeated any time the ^{t}REF refresh requirement is exceeded.
4. AC characteristics assume ^{t}T = 5ns.
5. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \le T_A \le 70°C$) is assured.
7. Measured with a load equivalent to two TTL gates and 100pF.
8. Assumes that $^{t}RCD < {}^{t}RCD$ (MAX). If ^{t}RCD is greater than the maximum recommended value shown in this table, ^{t}RAC will increase by the amount that ^{t}RCD exceeds the value shown.
9. Assumes that $^{t}RCD \ge {}^{t}RCD$ (MAX).
10. If $\overline{CAS}$ = V_{IH}, data output is High-Z.
11. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
12. ^{t}OFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
13. Operation within the ^{t}RCD (MAX) limit ensures that ^{t}RAC (MAX) can be met. ^{t}RCD (MAX) is specified as a reference point only; if ^{t}RCD is greater than the specified ^{t}RCD (MAX) limit, then access time is controlled exclusively by ^{t}CAC.
14. Either ^{t}RCH or ^{t}RRH must be satisfied for a READ cycle.
15. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY-WRITE cycles.
16. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
17. This parameter is sampled. Capacitance is measured using MIL-STD-883C, Method 3012.1 (1 MHz AC, Vcc = 5V, DC bias = 2.4V @ 15mV RMS).
18. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, data-out (Q) will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer, $\overline{CAS}$ must be pulsed HIGH for ^{t}CP.
19. On-chip refresh and address counters are enabled.
20. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW.
21. LATE-WRITE, READ-WRITE or READ-MODIFY-WRITE cycles are not available due to $\overline{OE}$ being grounded on U1-U8.
22. I_{CC} is dependent on cycle rates.
23. Operation within the ^{t}RAD (MAX) limit ensures that ^{t}RCD (MAX) can be met. ^{t}RAD (MAX) is specified as a reference point only; if ^{t}RAD is greater than the specified ^{t}RAD (MAX) limit, then access time is controlled exclusively by ^{t}AA.
24. Applies to L-version only.

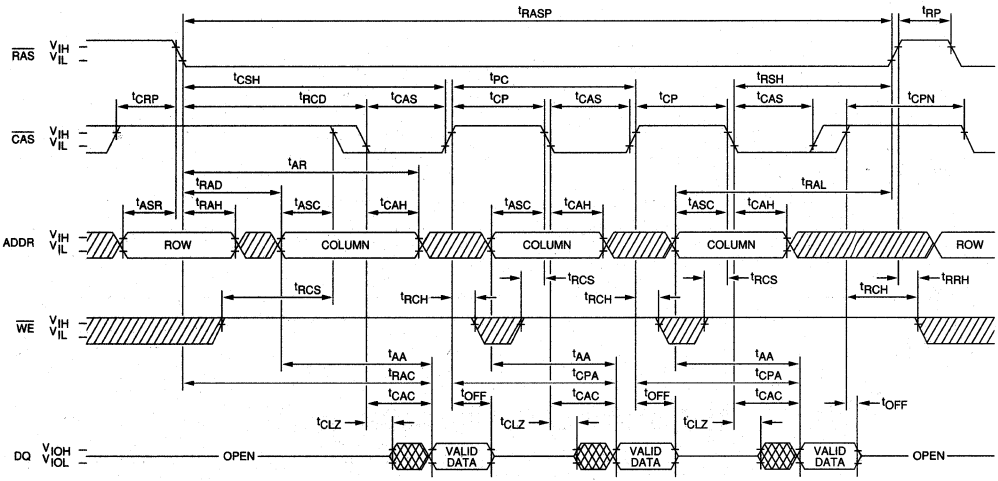
READ CYCLE



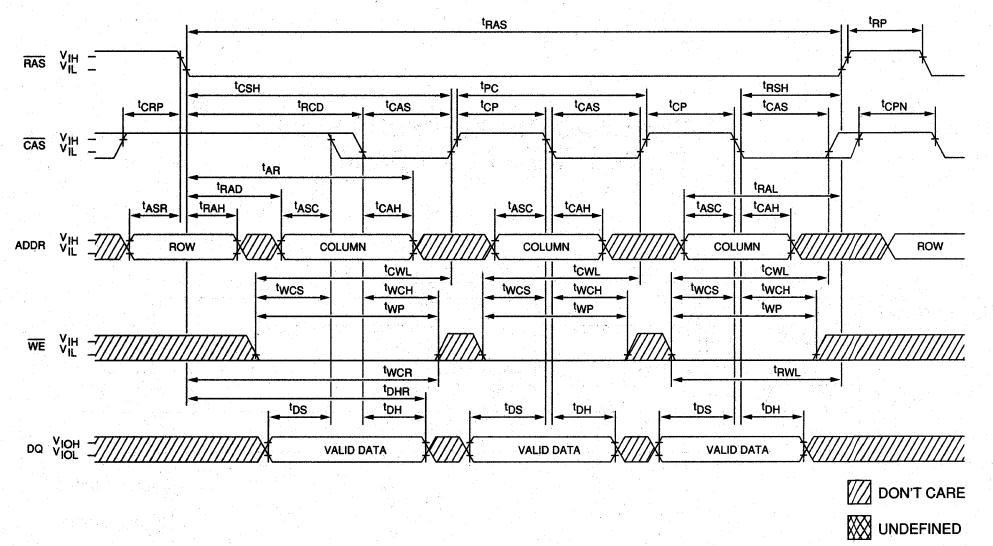
EARLY-WRITE CYCLE



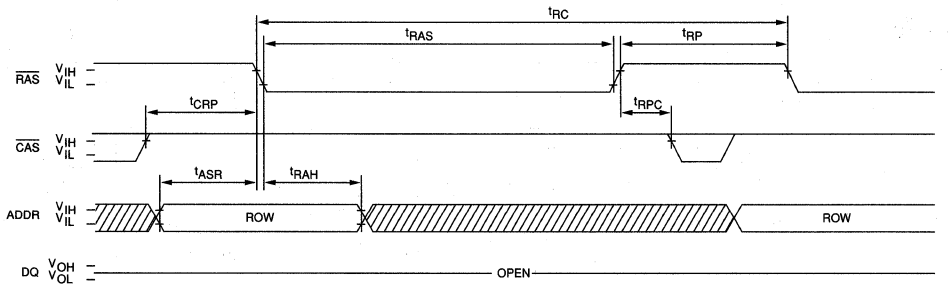
FAST-PAGE-MODE READ CYCLE



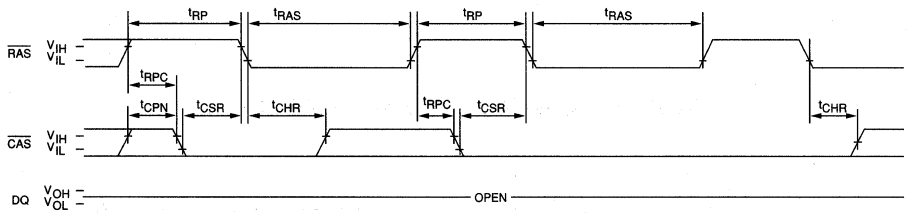
FAST-PAGE-MODE EARLY-WRITE CYCLE



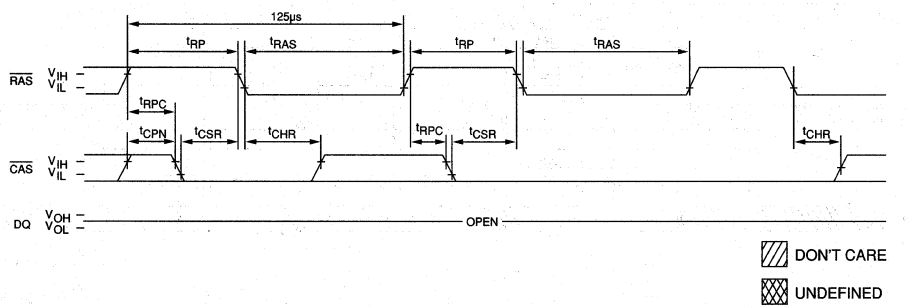
$\overline{\text{RAS}}$-ONLY REFRESH CYCLE
(ADDR = A0-A8; $\overline{\text{WE}}$ = DON'T CARE)



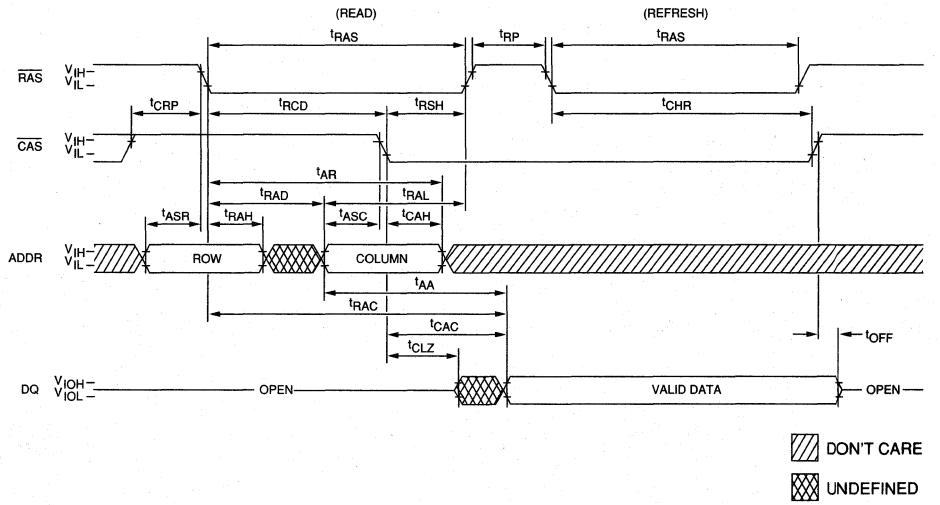
$\overline{\text{CAS}}$-BEFORE-$\overline{\text{RAS}}$ REFRESH CYCLE
(A0-A8, $\overline{\text{WE}}$ = DON'T CARE)



BATTERY BACKUP REFRESH CYCLE [24]
(A0-A8, $\overline{\text{WE}}$ = DON'T CARE)



HIDDEN REFRESH CYCLE [20]
($\overline{WE}$ = HIGH)



DRAM MODULE

512K x 32, 1 MEG x 16

FAST PAGE MODE (MT16D51232)
LOW POWER,
EXTENDED REFRESH (MT16D51232 L)

FEATURES

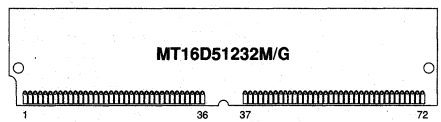
- Industry standard pinout in a 72-pin single-in-line package
- High-performance, CMOS silicon-gate process.
- Single 5V ±10% power supply
- All device pins are fully TTL compatible
- Low power, 48mW (4.8mW L-version) standby; 1,424mW active, typical
- Refresh modes: $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$ (CBR) and HIDDEN
- Multiple $\overline{RAS}$ lines offer x16 or x32 widths
- 512-cycle refresh distributed across 8ms or 512-cycle extended refresh distributed across 64ms
- FAST PAGE MODE access cycle
- Low CMOS standby current, 3.2µA maximum (L-version)

OPTIONS MARKING

- Timing
  - 60ns access - 6
  - 70ns access - 7
  - 80ns access - 8
- Packages
  - Leadless 72-pin SIMM M
  - Leadless 72-pin SIMM (Gold) G
- Power/Refresh
  - Normal Power/8ms Blank
  - Low Power/64ms L
- Part Number Example: MT16D51232G-6

PIN ASSIGNMENT (Top View)

72-Pin SIMM
(T-10)



PIN #	SYMBOL	PIN #	SYMBOL	PIN #	SYMBOL	PIN #	SYMBOL
1	Vss	19	NC	37	NC	55	DQ12
2	DQ1	20	DQ5	38	NC	56	DQ28
3	DQ17	21	DQ21	39	Vss	57	DQ13
4	DQ2	22	DQ6	40	$\overline{CAS0}$	58	DQ29
5	DQ18	23	DQ22	41	$\overline{CAS2}$	59	Vcc
6	DQ3	24	DQ7	42	$\overline{CAS3}$	60	DQ30
7	DQ19	25	DQ23	43	$\overline{CAS1}$	61	DQ14
8	DQ4	26	DQ8	44	$\overline{RAS0}$	62	DQ31
9	DQ20	27	DQ24	45	$\overline{RAS1}$	63	DQ15
10	Vcc	28	A7	46	NC	64	DQ32
11	NC	29	NC	47	$\overline{WE}$	65	DQ16
12	A0	30	Vcc	48	NC	66	NC
13	A1	31	A8	49	DQ9	67	PRD1
14	A2	32	NC	50	DQ25	68	PRD2
15	A3	33	$\overline{RAS3}$	51	DQ10	69	PRD3
16	A4	34	$\overline{RAS2}$	52	DQ26	70	PRD4
17	A5	35	NC	53	DQ11	71	NC
18	A6	36	NC	54	DQ27	72	Vss

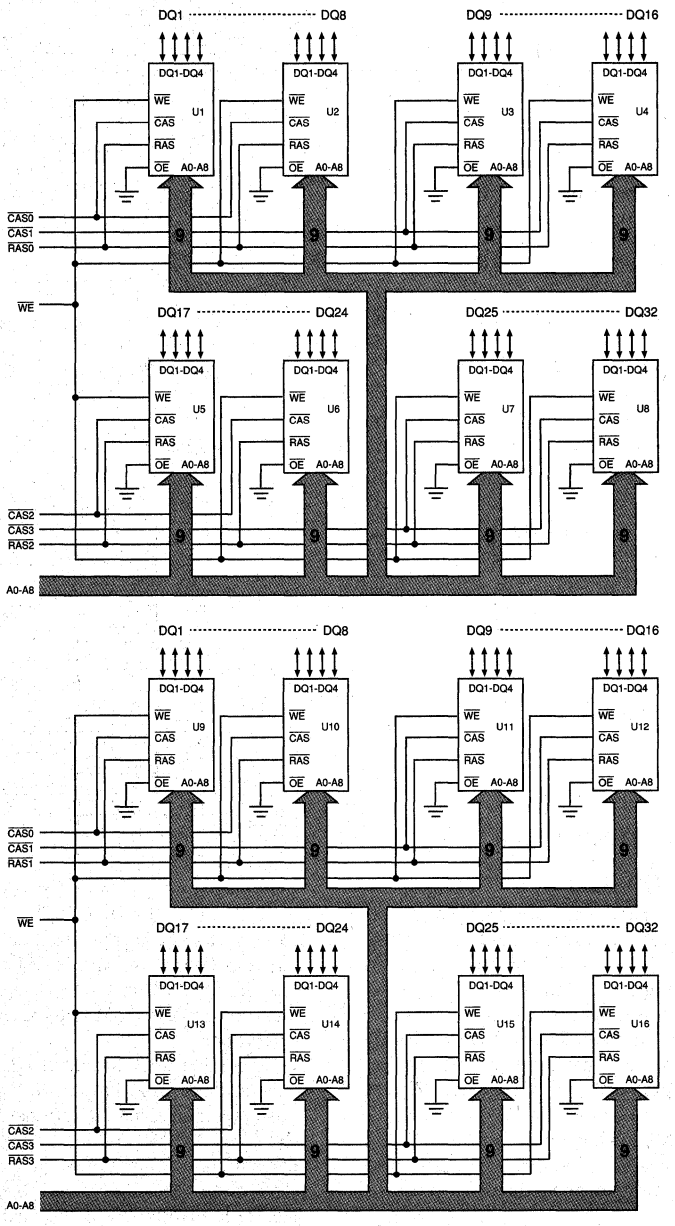
GENERAL DESCRIPTION

The MT16D51232 is a randomly accessed solid-state memory containing 524,288 words organized in a x32 configuration. During READ or WRITE cycles, each bit is uniquely addressed through the 18 address bits which are entered 9 bits (A0-A8) at a time. $\overline{RAS}$ is used to latch the first 9 bits and $\overline{CAS}$ the latter 9 bits. READ or WRITE cycles are selected with the $\overline{WE}$ input. A logic HIGH on $\overline{WE}$ dictates READ mode while a logic LOW on $\overline{WE}$ dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. EARLY WRITE occurs when $\overline{WE}$ goes LOW prior to $\overline{CAS}$ going LOW, the output pin(s) remain open (High-Z) until the next $\overline{CAS}$ cycle.

FAST PAGE MODE operations allow faster data operations (READ or WRITE) within a row-address (A0-A8) defined page boundary. The FAST PAGE MODE cycle is always initiated with a row address strobed-in by $\overline{RAS}$ followed by a column address strobed-in by $\overline{CAS}$. $\overline{CAS}$ may be toggled-in by holding $\overline{RAS}$ LOW and strobing-in different column addresses, thus executing faster memory cycles. Returning $\overline{RAS}$ HIGH terminates the FAST-PAGE-MODE operation.

Returning $\overline{RAS}$ and $\overline{CAS}$ HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the $\overline{RAS}$ high time. Memory cell data is retained in its correct state by maintaining power and executing any $\overline{RAS}$ cycle (READ, WRITE, $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$ or HIDDEN REFRESH) so that all 512 combinations of $\overline{RAS}$ addresses (A0-A8) are executed at least every 8ms (64ms on L-version), regardless of sequence.

FUNCTIONAL BLOCK DIAGRAM



U1-U16 = MT4C4256DJ
U1-U16 = MT4C4256DJ L (L-version)

TRUTH TABLE

FUNCTION		RAS	CAS	WE	ADDRESSES		DATA IN/OUT
					^tR	^tC	DQ1-DQ32
Standby		H	H→X	X	X	X	High-Z
READ		L	L	H	ROW	COL	Data Out
EARLY-WRITE		L	L	L	ROW	COL	Data In
FAST-PAGE-MODE	1st Cycle	L	H→L	H	ROW	COL	Data Out
READ	2nd Cycle	L	H→L	H	n/a	COL	Data Out
FAST-PAGE-MODE	1st Cycle	L	H→L	L	ROW	COL	Data In
WRITE	2nd Cycle	L	H→L	L	n/a	COL	Data In
RAS-ONLY REFRESH		L	H	X	ROW	n/a	High-Z
HIDDEN	READ	L→H→L	L	H	ROW	COL	Data Out
REFRESH	WRITE	L→H→L	L	L	ROW	COL	Data In
CAS-BEFORE-RAS REFRESH		H→L	L	X	X	X	High-Z
BATTERY BACKUP REFRESH (L-version)		H→L	L	X	X	X	High-Z

PRESENCE DETECT

SYMBOL	-6	-7	-8
PRD1	NC	NC	NC
PRD2	Vss	Vss	Vss
PRD3	NC	Vss	NC
PRD4	NC	NC	Vss

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} ..... -1V to +7V
Operating Temperature, T_A (Ambient) ..... 0°C to +70°C
Storage Temperature (Plastic) ..... -55°C to +125°C
Power Dissipation 16W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 2, 3, 6, 22) (0°C ≤ T_A ≤ 70°C; V_{CC} = 5V ±10%)

PARAMETER/CONDITION		SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage		V_{CC}	4.5	5.5	V	1
Input High (Logic 1) Voltage, All Inputs		V_{IH}	2.4	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, All Inputs		V_{IL}	-1.0	0.8	V	1
INPUT LEAKAGE CURRENT	$\overline{CAS0}$-$\overline{CAS3}$	I_{I1}	-8	8	µA	
Any Input: 0V ≤ V_{IN} ≤ V_{CC}	A0-A8, $\overline{WE}$	I_{I2}	-32	32	µA	
(All other pins not under test = 0V) For each package input	$\overline{RAS0}$-$\overline{RAS3}$	I_{I3}	-8	8	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled, 0V ≤ V_{OUT} ≤ V_{CC}) For each package input	DQ1-DQ32	I_{OZ}	-20	20	µA	
OUTPUT LEVELS Output High Voltage (I_{OUT} = -5mA)		V_{OH}	2.4		V	
Output Low Voltage (I_{OUT} = 5mA)		V_{OL}		0.4	V	

		MAX				
PARAMETER/CONDITION	SYMBOL	-6	-7	-8	UNITS	NOTES
STANDBY CURRENT: (TTL) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC1}	32	32	32	mA	
STANDBY CURRENT: (CMOS)	I_{CC2}	16	16	16	mA	
($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} -0.2V)		3.2	3.2	3.2	mA	24
OPERATING CURRENT: Random READ/WRITE Average power supply current	I_{CC3}	736	656	576	mA	2, 22
($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC (MIN))		684	604	524	mA	2,22,24
OPERATING CURRENT: FAST PAGE MODE Average power supply current	I_{CC4}	576	496	416	mA	2, 22
($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: ^tPC = ^tPC (MIN))		524	444	364	mA	2,22,24
REFRESH CURRENT: $\overline{RAS}$-ONLY Average power supply current	I_{CC5}	736	656	576	mA	2
($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}: ^tRC = ^tRC (MIN))		684	604	524	mA	2, 24
REFRESH CURRENT: $\overline{CAS}$-BEFORE-$\overline{RAS}$ Average power supply current	I_{CC6}	736	656	576	mA	2, 19
($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC (MIN))		684	604	524	mA	2,19,24
REFRESH CURRENT: BATTERY BACKUP (BBU) Average power supply current during BATTERY BACKUP refresh: $\overline{CAS}$ = 0.2V or $\overline{CAS}$-BEFORE-$\overline{RAS}$ cycling; $\overline{RAS}$ = ^tRAS (MIN) to 1µs; $\overline{WE}$, A0-A9 and D_{IN} = Vcc -0.2V or 0.2V (D_{IN} may be left OPEN), ^tRC = 125µs (512 rows at 125µs = 64ms)	I_{CC7}	3.2	3.2	3.2	mA	24

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A8	C_{I1}		102	pF	17
Input Capacitance: $\overline{WE}$	C_{I2}		134	pF	17
Input Capacitance: $\overline{CAS0}$-$\overline{CAS3}$, $\overline{RAS0}$-$\overline{RAS3}$	C_{I4}		34	pF	17
Input/Output Capacitance: DQ1-DQ32	C_{IO}		20	pF	17

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 3, 4, 5, 6, 7, 10, 11, 16, 21) ($0°C \le T_A \le 70°C$; V_{CC} = 5V ±10%)

AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	^tRC	110		130		150		ns	
READ-WRITE cycle time	^tRWC	n/a		n/a		n/a		ns	21
FAST-PAGE-MODE READ or WRITE cycle time	^tPC	40		40		45		ns	
FAST-PAGE-MODE READ-WRITE cycle time	^tPRWC	n/a		n/a		n/a		ns	21
Access time from $\overline{RAS}$	^tRAC		60		70		80	ns	8
Access time from $\overline{CAS}$	^tCAC		20		20		20	ns	9
Output Enable	^tOE		20		20		20	ns	
Access time from column address	^tAA		30		35		40	ns	
Access time from $\overline{CAS}$ precharge	^tCPA		35		40		45	ns	
$\overline{RAS}$ pulse width	^tRAS	60	100,000	70	100,000	80	100,000	ns	
$\overline{RAS}$ pulse width (FAST PAGE MODE)	^tRASP	60	100,000	70	100,000	80	100,000	ns	
$\overline{RAS}$ hold time	^tRSH	20		20		20		ns	
$\overline{RAS}$ precharge time	^tRP	40		50		60		ns	
$\overline{CAS}$ pulse width	^tCAS	20	100,000	20	100,000	20	100,000	ns	
$\overline{CAS}$ hold time	^tCSH	60		70		80		ns	
$\overline{CAS}$ precharge time	^tCPN	10		10		10		ns	18
$\overline{CAS}$ precharge time (FAST PAGE MODE)	^tCP	10		10		10		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	^tRCD	20	40	20	50	20	60	ns	13
$\overline{CAS}$ to $\overline{RAS}$ precharge time	^tCRP	5		5		5		ns	
Row address setup time	^tASR	0		0		0		ns	
Row address hold time	^tRAH	10		10		10		ns	
$\overline{RAS}$ to column address delay time	^tRAD	15	30	15	35	15	40	ns	23
Column address setup time	^tASC	0		0		0		ns	
Column address hold time	^tCAH	15		15		15		ns	
Column address hold time (referenced to $\overline{RAS}$)	^tAR	45		55		60		ns	
Column address to $\overline{RAS}$ lead time	^tRAL	30		35		40		ns	
Read command setup time	^tRCS	0		0		0		ns	
Read command hold time (referenced to $\overline{CAS}$)	^tRCH	0		0		0		ns	14
Read command hold time (referenced to $\overline{RAS}$)	^tRRH	0		0		0		ns	14

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

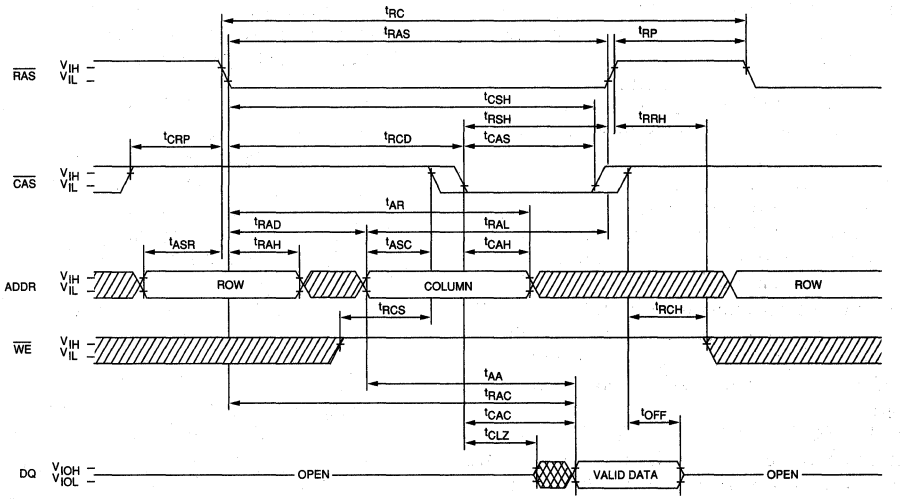
(Notes: 3, 4, 5, 6, 7, 10, 11, 16, 21) ($0°C \le T_A \le 70°C$; Vcc = 5V ±10%)

AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
$\overline{CAS}$ to output in Low-Z	^tCLZ	0		0		0		ns	
Output buffer turn-off delay	^tOFF	0	20	0	20	0	20	ns	12
$\overline{WE}$ command setup time	^tWCS	0		0		0		ns	
Write command hold time	^tWCH	10		15		15		ns	
Write command hold time (referenced to $\overline{RAS}$)	^tWCR	45		55		60		ns	
Write command pulse width	^tWP	10		15		15		ns	
Write command to $\overline{RAS}$ lead time	^tRWL	20		20		20		ns	
Write command to $\overline{CAS}$ lead time	^tCWL	20		20		20		ns	
Data-in setup time	^tDS	0		0		0		ns	15
Data-in hold time	^tDH	15		15		15		ns	15
Data-in hold time (referenced to $\overline{RAS}$)	^tDHR	45		55		60		ns	
Transition time (rise or fall)	^tT	3	50	3	50	3	50	ns	5, 16
Refresh period (512 cycles)	^tREF		8/64		8/64		8/64	ms	3/24
$\overline{RAS}$ to $\overline{CAS}$ precharge time	^tRPC	0		0		0		ns	
$\overline{CAS}$ setup time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tCSR	10		10		10		ns	19
$\overline{CAS}$ hold time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tCHR	10		15		15		ns	19

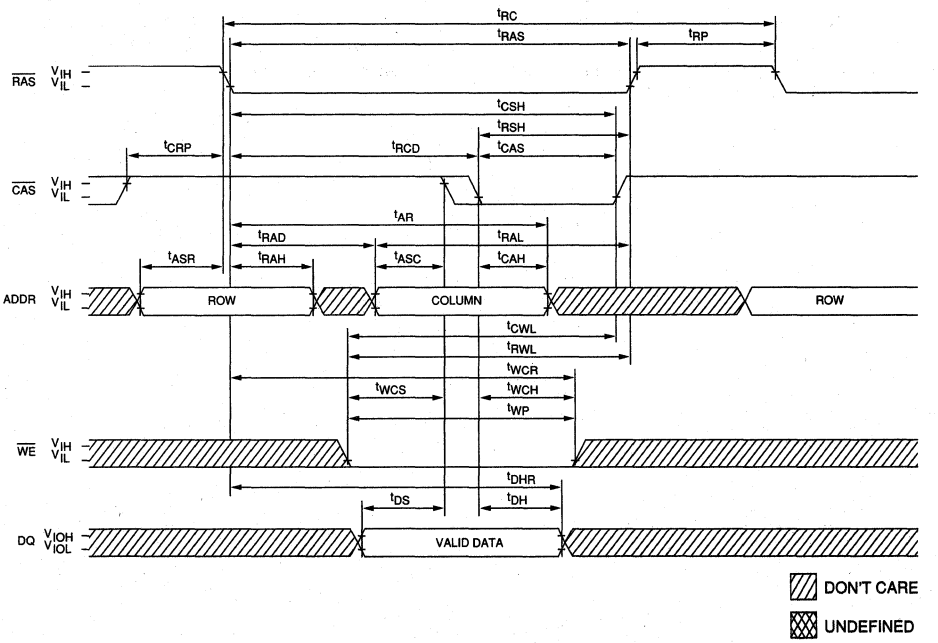
NOTES

1. All voltages referenced to V_{SS}.
2. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
3. An initial pause of 100µs is required after power-up followed by any eight $\overline{RAS}$ cycles before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-up should be repeated any time the ^{t}REF refresh requirement is exceeded.
4. AC characteristics assume ^{t}T = 5ns.
5. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \le T_A \le 70°C$) is assured.
7. Measured with a load equivalent to two TTL gates and 100pF.
8. Assumes that $^{t}RCD < ^{t}RCD$ (MAX). If ^{t}RCD is greater than the maximum recommended value shown in this table, ^{t}RAC will increase by the amount that ^{t}RCD exceeds the value shown.
9. Assumes that $^{t}RCD \ge ^{t}RCD$ (MAX).
10. If $\overline{CAS}$ = V_{IH}, data output is High-Z.
11. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
12. ^{t}OFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
13. Operation within the ^{t}RCD (MAX) limit ensures that ^{t}RAC (MAX) can be met. ^{t}RCD (MAX) is specified as a reference point only; if ^{t}RCD is greater than the specified ^{t}RCD (MAX) limit, then access time is controlled exclusively by ^{t}CAC.
14. Either ^{t}RCH or ^{t}RRH must be satisfied for a READ cycle.
15. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY-WRITE cycles.
16. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
17. This parameter is sampled. Capacitance is measured using MIL-STD-883C, Method 3012.1 (1 MHz AC, Vcc = 5V, DC bias = 2.4V @ 15mV RMS).
18. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, data-out (Q) will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer, $\overline{CAS}$ must be pulsed HIGH for ^{t}CP.
19. On-chip refresh and address counters are enabled.
20. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW.
21. LATE-WRITE, READ-WRITE or READ-MODIFY-WRITE cycles are not available due to $\overline{OE}$ being grounded on U1-U16.
22. Icc is dependent on cycle rates.
23. Operation within the ^{t}RAD (MAX) limit ensures that ^{t}RCD (MAX) can be met. ^{t}RAD (MAX) is specified as a reference point only; if ^{t}RAD is greater than the specified ^{t}RAD (MAX) limit, then access time is controlled exclusively by ^{t}AA.
24. Applies to L-version only.

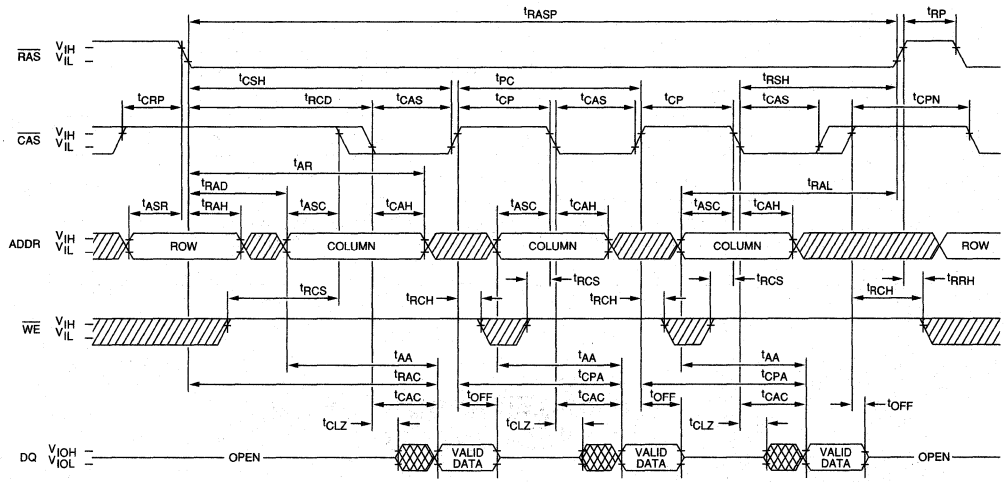
READ CYCLE



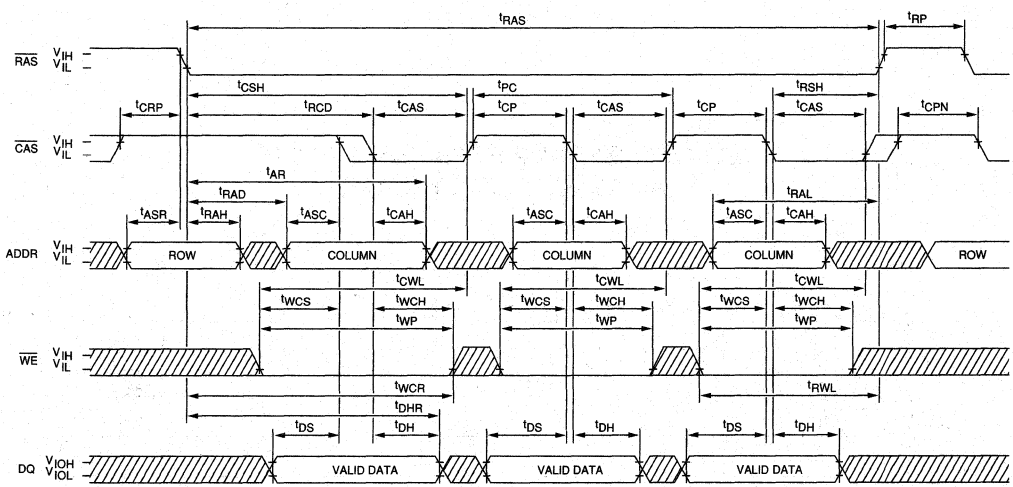
EARLY-WRITE CYCLE



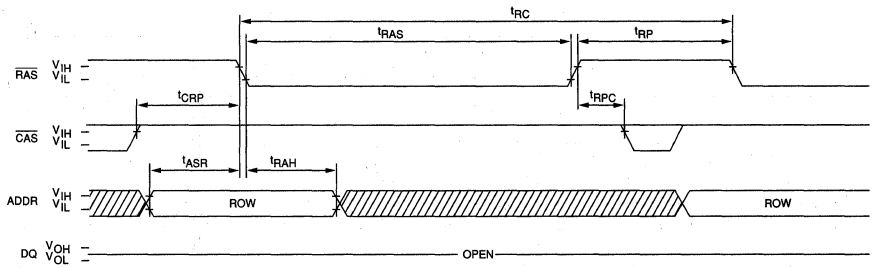
FAST-PAGE-MODE READ CYCLE



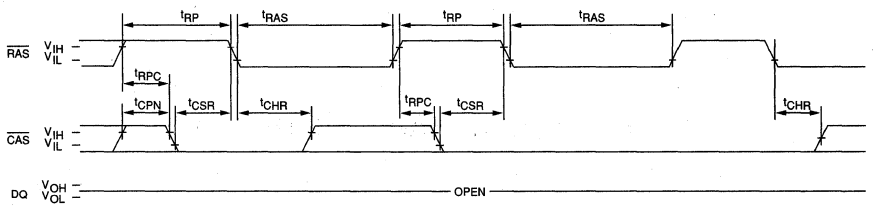
FAST-PAGE-MODE EARLY-WRITE CYCLE



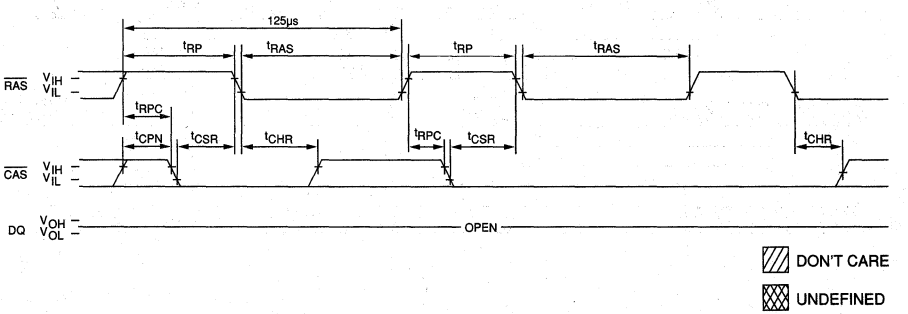
$\overline{\text{RAS}}$-ONLY REFRESH CYCLE
(ADDR = A0-A7; A8 and $\overline{\text{WE}}$ = DON'T CARE)



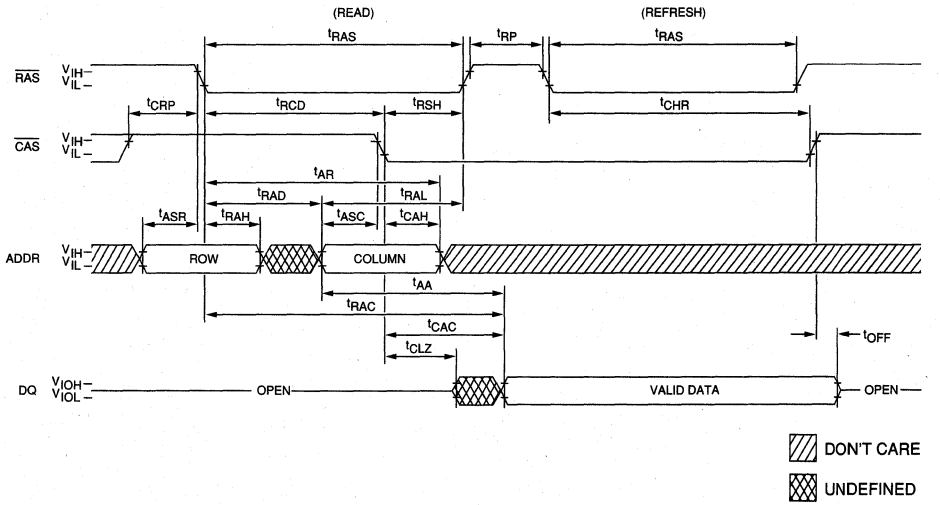
$\overline{\text{CAS}}$-BEFORE-$\overline{\text{RAS}}$ REFRESH CYCLE
(A0-A8, $\overline{\text{WE}}$ = DON'T CARE)



BATTERY BACKUP REFRESH CYCLE [24]
(A0-A8, $\overline{\text{WE}}$ = DON'T CARE)



HIDDEN REFRESH CYCLE[20]
($\overline{WE}$ = HIGH)



DRAM MODULE

1 MEG x 32, 2 MEG x 16

FAST PAGE MODE (MT8D132)
LOW POWER,
EXTENDED REFRESH (MT8D132 L)

FEATURES

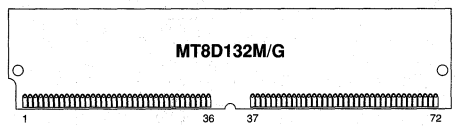
- Industry standard pinout in a 72-pin single-in-line package
- High-performance, CMOS silicon-gate process.
- Single 5V ±10% power supply
- All device pins are fully TTL compatible
- Low power, 24mW (8mW L-version) standby; 1,800mW active, typical
- Refresh modes: RAS-ONLY, CAS-BEFORE-RAS (CBR) and HIDDEN
- 1,024-cycle refresh distributed across 16ms or 1,024-cycle extended refresh distributed across 128ms
- FAST PAGE MODE access cycle
- Low CMOS standby current 1.6mA maximum (L-version)

OPTIONS — MARKING

- Timing
  - 60ns access - 6
  - 70ns access - 7
  - 80ns access - 8
- Packages
  - Leadless 72-pin SIMM M
  - Leadless 72-pin SIMM (Gold) G
- Power/Refresh
  - Normal Power/16ms Blank
  - Low Power/128ms L
- Part Number Example: MT8D132GL-6

PIN ASSIGNMENT (Top View)

72-Pin SIMM
(T-9)



PIN #	SYMBOL	PIN #	SYMBOL	PIN #	SYMBOL	PIN #	SYMBOL
1	Vss	19	NC	37	NC	55	DQ12
2	DQ1	20	DQ5	38	NC	56	DQ28
3	DQ17	21	DQ21	39	Vss	57	DQ13
4	DQ2	22	DQ6	40	CAS0	58	DQ29
5	DQ18	23	DQ22	41	CAS2	59	Vcc
6	DQ3	24	DQ7	42	CAS3	60	DQ30
7	DQ19	25	DQ23	43	CAS1	61	DQ14
8	DQ4	26	DQ8	44	RAS0	62	DQ31
9	DQ20	27	DQ24	45	NC	63	DQ15
10	Vcc	28	A7	46	NC	64	DQ32
11	NC	29	NC	47	WE	65	DQ16
12	A0	30	Vcc	48	NC	66	NC
13	A1	31	A8	49	DQ9	67	PRD1
14	A2	32	A9	50	DQ25	68	PRD2
15	A3	33	NC	51	DQ10	69	PRD3
16	A4	34	RAS2	52	DQ26	70	PRD4
17	A5	35	NC	53	DQ11	71	NC
18	A6	36	NC	54	DQ27	72	Vss

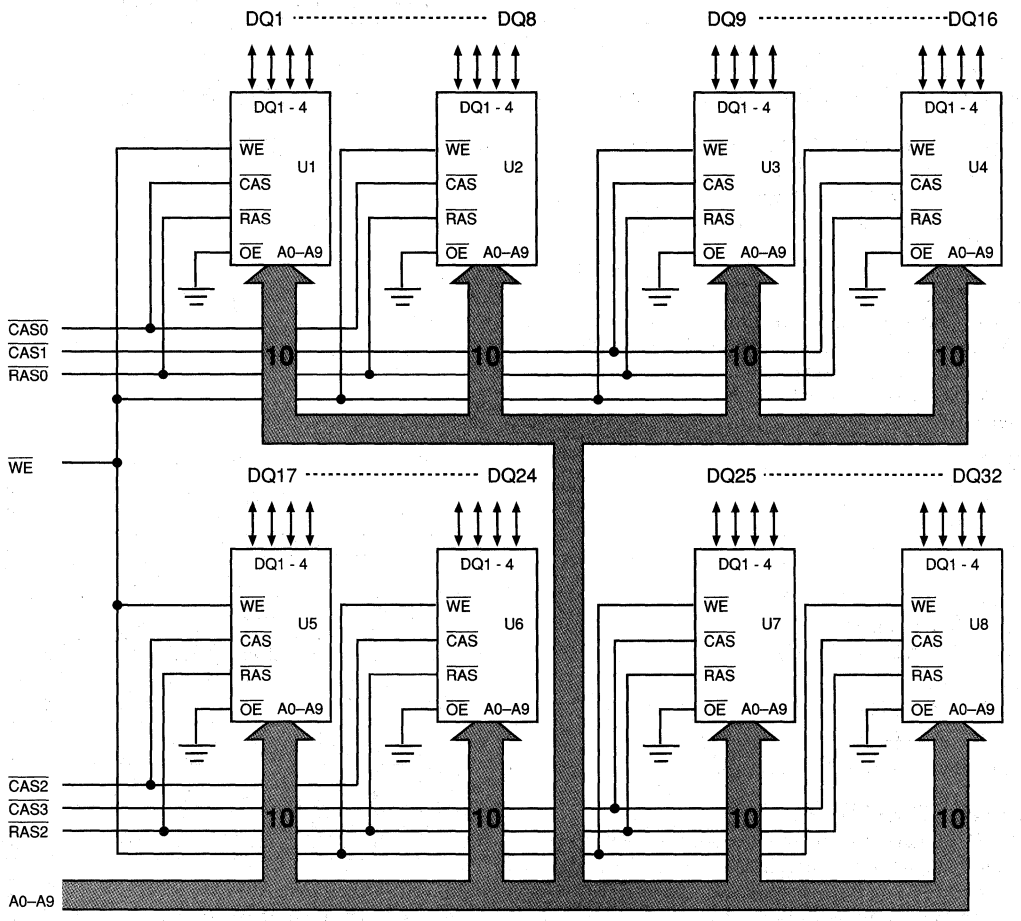
GENERAL DESCRIPTION

The MT8D132 is a randomly accessed solid-state memory containing 1,048,576 words organized in a x32 configuration. During READ or WRITE cycles, each bit is uniquely addressed through the 20 address bits which are entered 10 bits (A0-A9) at a time. RAS is used to latch the first 10 bits and CAS the latter 10 bits. A READ or WRITE cycle is selected with the WE input. A logic HIGH on WE dictates READ mode while a logic LOW on WE dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of WE or CAS, whichever occurs last. If WE goes LOW prior to CAS going LOW, the output pin(s) remain open (High-Z) until the next CAS cycle.

FAST PAGE MODE operations allow faster data operations (READ or WRITE) within a row-address (A0-A9) defined page boundary. The FAST PAGE MODE cycle is always initiated with a row address strobed-in by RAS followed by a column address strobed-in by CAS. CAS may be toggled-in by holding RAS LOW and strobing-in different column addresses, thus executing faster memory cycles. Returning RAS HIGH terminates the FAST PAGE MODE operation.

Returning RAS and CAS HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the RAS HIGH time. Memory cell data is retained in its correct state by maintaining power and executing any RAS cycle (READ, WRITE, RAS-ONLY, CAS-BEFORE-RAS or HIDDEN REFRESH) so that all 1,024 combinations of RAS addresses (A0-A9) are executed at least every 16ms (128ms on L-version), regardless of sequence.

FUNCTIONAL BLOCK DIAGRAM



U1-U8 = MT4C4001JDJ
U1-U8 = MT4C4001JDJ L (L-version)

TRUTH TABLE

FUNCTION		RAS	CAS	WE	ADDRESSES		DATA IN/OUT
					^tR	^tC	DQ1-DQ32
Standby		H	H→X	X	X	X	High-Z
READ		L	L	H	ROW	COL	Data Out
EARLY-WRITE		L	L	L	ROW	COL	Data In
FAST-PAGE-MODE	1st Cycle	L	H→L	H	ROW	COL	Data Out
READ	2nd Cycle	L	H→L	H	n/a	COL	Data Out
FAST-PAGE-MODE	1st Cycle	L	H→L	L	ROW	COL	Data In
WRITE	2nd Cycle	L	H→L	L	n/a	COL	Data In
RAS-ONLY REFRESH		L	H	X	ROW	n/a	High-Z
HIDDEN	READ	L→H→L	L	H	ROW	COL	Data Out
REFRESH	WRITE	L→H→L	L	L	ROW	COL	Data In
CAS-BEFORE-RAS REFRESH		H→L	L	H	X	X	High-Z
BATTERY BACKUP REFRESH (L-version)		H→L	L	X	X	X	High-Z

PRESENCE DETECT

SYMBOL	-6	-7	-8
PRD1	Vss	Vss	Vss
PRD2	Vss	Vss	Vss
PRD3	NC	Vss	NC
PRD4	NC	NC	Vss

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS} ..... -1V to +7V
Operating Temperature, T_A (Ambient) ..... 0°C to +70°C
Storage Temperature (Plastic) ..... -55°C to +125°C
Power Dissipation 8W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 2, 3, 6, 22) (0°C ≤ T_A ≤ 70°C; V_{CC} = 5V ± 10%)

PARAMETER/CONDITION		SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage		V_{CC}	4.5	5.5	V	1
Input High (Logic 1) Voltage, All Inputs		V_{IH}	2.4	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, All Inputs		V_{IL}	-1.0	0.8	V	1
INPUT LEAKAGE CURRENT	$\overline{RAS0}$, $\overline{RAS2}$	I_{I1}	-8	8	µA	
Any Input: 0V ≤ V_{IN} ≤ V_{CC}	A0-A9, $\overline{WE}$	I_{I2}	-16	16	µA	
(All other pins not under test = 0V) For each package input	$\overline{CAS0}$-$\overline{CAS3}$	I_{I3}	-4	4	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled, 0V ≤ V_{OUT} ≤ V_{CC}) For each package input	DQ1-DQ32	I_{OZ}	-10	10	µA	
OUTPUT LEVELS Output High Voltage (I_{OUT} = -5mA)		V_{OH}	2.4		V	
Output Low Voltage (I_{OUT} = 5mA)		V_{OL}		0.4	V	

		MAX				
PARAMETER/CONDITION	SYMBOL	-6	-7	-8	UNITS	NOTES
STANDBY CURRENT: (TTL) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC1}	16	16	16	mA	
STANDBY CURRENT: (CMOS)	I_{CC2}	8	8	8	mA	
($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} -0.2V)		1.6	1.6	1.6	mA	24
OPERATING CURRENT: Random READ/WRITE Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC (MIN))	I_{CC3}	880	800	720	mA	2, 22
OPERATING CURRENT: FAST PAGE MODE Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: ^tPC = ^tPC (MIN))	I_{CC4}	640	560	480	mA	2, 22
REFRESH CURRENT: $\overline{RAS}$-ONLY Average power supply current ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}: ^tRC = ^tRC (MIN))	I_{CC5}	880	800	720	mA	2
REFRESH CURRENT: $\overline{CAS}$-BEFORE-$\overline{RAS}$ Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC (MIN))	I_{CC6}	880	800	720	mA	2, 19
REFRESH CURRENT: BATTERY BACKUP (BBU) Average power supply current during BATTERY BACKUP refresh: $\overline{CAS}$ = 0.2V or $\overline{CAS}$-BEFORE-$\overline{RAS}$ cycling; $\overline{RAS}$ = ^tRAS (MIN) to 300µs; $\overline{WE}$ = Vcc -0.2V; A0-A9 and D_{IN} = Vcc -0.2V or 0.2V (D_{IN} may be left open), ^tRC = 125µs (1,024 rows at 125µs = 128ms)	I_{CC7}	2.4	2.4	2.4	mA	24

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A9	C_{I1}		51	pF	17
Input Capacitance: $\overline{WE}$	C_{I2}		67	pF	17
Input Capacitance: $\overline{RAS0}$, $\overline{RAS2}$	C_{I3}		34	pF	17
Input Capacitance: $\overline{CAS0}$, $\overline{CAS0}$, $\overline{CAS2}$, $\overline{CAS3}$	C_{I4}		17	pF	17
Input/Output Capacitance: DQ1-DQ32	C_{IO}		10	pF	17

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 3, 4, 5, 6, 7, 10, 11, 16, 21) (0°C ≤ T_A ≤ 70°C; Vcc = 5V ±10%)

AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	^tRC	110		130		150		ns	
READ-WRITE cycle time	^tRWC	n/a		n/a		n/a		ns	21
FAST-PAGE-MODE READ or WRITE cycle time	^tPC	40		40		45		ns	
FAST-PAGE-MODE READ-WRITE cycle time	^tPRWC	n/a		n/a		n/a		ns	21
Access time from $\overline{RAS}$	^tRAC		60		70		80	ns	8
Access time from $\overline{CAS}$	^tCAC		15		20		20	ns	9
Output Enable	^tOE		15		20		20	ns	
Access time from column address	^tAA		30		35		40	ns	
Access time from $\overline{CAS}$ precharge	^tCPA		35		40		45	ns	
$\overline{RAS}$ pulse width	^tRAS	60	100,000	70	100,000	80	100,000	ns	
$\overline{RAS}$ pulse width (FAST PAGE MODE)	^tRASP	60	200,000	70	200,000	80	200,000	ns	
$\overline{RAS}$ hold time	^tRSH	15		20		20		ns	
$\overline{RAS}$ precharge time	^tRP	40		50		60		ns	
$\overline{CAS}$ pulse width	^tCAS	15	100,000	20	100,000	20	100,000	ns	
$\overline{CAS}$ hold time	^tCSH	60		70		80		ns	
$\overline{CAS}$ precharge time	^tCPN	10		10		10		ns	18
$\overline{CAS}$ precharge time (FAST PAGE MODE)	^tCP	10		10		10		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	^tRCD	20	45	20	50	20	60	ns	13
$\overline{CAS}$ to $\overline{RAS}$ precharge time	^tCRP	10		10		10		ns	
Row address setup time	^tASR	0		0		0		ns	
Row address hold time	^tRAH	10		10		10		ns	
$\overline{RAS}$ to column address delay time	^tRAD	15	30	15	35	15	40	ns	23
Column address setup time	^tASC	0		0		0		ns	
Column address hold time	^tCAH	10		15		15		ns	
Column address hold time (referenced to $\overline{RAS}$)	^tAR	50		55		60		ns	
Column address to $\overline{RAS}$ lead time	^tRAL	30		35		40		ns	
Read command setup time	^tRCS	0		0		0		ns	
Read command hold time (referenced to $\overline{CAS}$)	^tRCH	0		0		0		ns	14
Read command hold time (referenced to $\overline{RAS}$)	^tRRH	0		0		0		ns	14

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

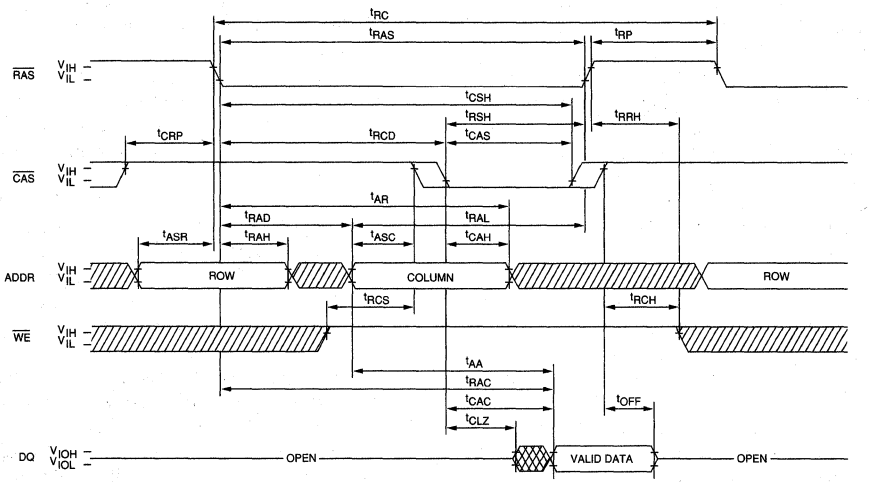
(Notes: 3, 4, 5, 6, 7, 10, 11, 16, 21) (0°C ≤ T_A ≤ 70°C; Vcc = 5V ±10%)

AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
$\overline{CAS}$ to output in Low-Z	^tCLZ	0		0		0		ns	
Output buffer turn-off delay	^tOFF	0	15	0	20	0	20	ns	12
$\overline{WE}$ command setup time	^tWCS	0		0		0		ns	
Write command hold time	^tWCH	10		15		15		ns	
Write command hold time (referenced to $\overline{RAS}$)	^tWCR	45		55		60		ns	
Write command pulse width	^tWP	10		15		15		ns	
Write command to $\overline{RAS}$ lead time	^tRWL	15		20		20		ns	
Write command to $\overline{CAS}$ lead time	^tCWL	15		20		20		ns	
Data-in setup time	^tDS	0		0		0		ns	15
Data-in hold time	^tDH	10		15		15		ns	15
Data-in hold time (referenced to $\overline{RAS}$)	^tDHR	45		55		60		ns	
Transition time (rise or fall)	^tT	3	50	3	50	3	50	ns	5, 16
Refresh period (1,024 cycles)	^tREF		16/128		16/128		16/128	ms	3/24
$\overline{RAS}$ to $\overline{CAS}$ precharge time	^tRPC	0		0		0		ns	
$\overline{CAS}$ setup time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tCSR	10		10		10		ns	19
$\overline{CAS}$ hold time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tCHR	15		15		15		ns	19
$\overline{WE}$ hold time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tWRH	10		10		10		ns	
$\overline{WE}$ setup time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tWRP	10		10		10		ns	
$\overline{WE}$ hold time (WCBR test cycle)	^tWTH	10		10		10		ns	
$\overline{WE}$ setup time (WCBR test cycle)	^tWTS	10		10		10		ns	

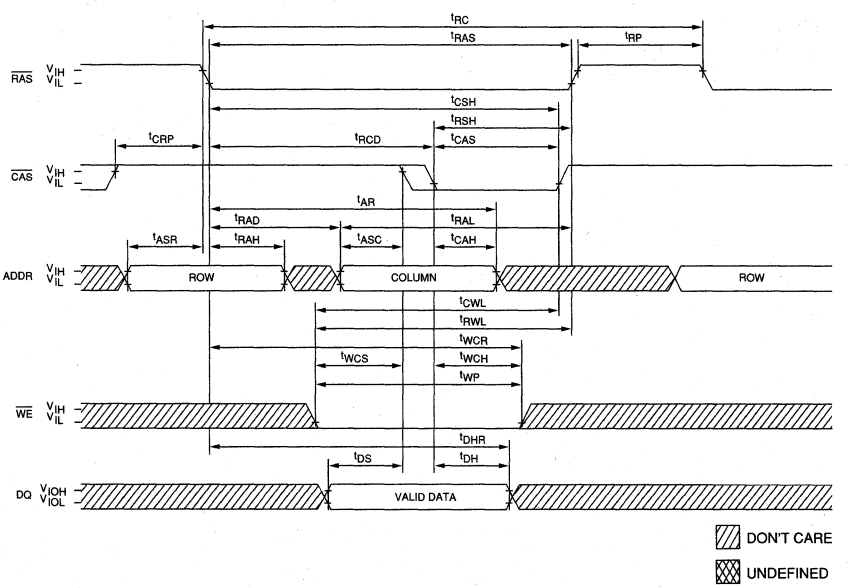
NOTES

1. All voltages referenced to V_{SS}.
2. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
3. An initial pause of 100µs is required after power-up followed by any eight $\overline{RAS}$ REFRESH cycles ($\overline{RAS}$-ONLY or CBR with $\overline{WE}$ HIGH) before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-up should be repeated any time the ^tREF refresh requirement is exceeded.
4. AC characteristics assume ^tT = 5ns.
5. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is assured.
7. Measured with a load equivalent to two TTL gates and 100pF.
8. Assumes that $^tRCD < ^tRCD$ (MAX). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
9. Assumes that $^tRCD \geq ^tRCD$ (MAX).
10. If $\overline{CAS}$ = V_{IH}, data output is High-Z.
11. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
12. ^tOFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
13. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (MAX) limit, then access time is controlled exclusively by ^tCAC.
14. Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
15. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY-WRITE cycles.
16. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
17. This parameter is sampled. Capacitance is measured using MIL-STD-883C, Method 3012.1 (1 MHz AC, Vcc = 5V, DC bias = 2.4V @ 15mV RMS).
18. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, data-out (Q) will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer, $\overline{CAS}$ must be pulsed HIGH for ^tCP.
19. On-chip refresh and address counters are enabled.
20. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW.
21. LATE-WRITE, READ-WRITE or READ-MODIFY-WRITE cycles are not available due to $\overline{OE}$ being grounded on U1-U8.
22. I_{CC} is dependent on cycle rates.
23. Operation within the ^tRAD (MAX) limit ensures that ^tRCD (MAX) can be met. ^tRAD (MAX) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (MAX) limit, then access time is controlled exclusively by ^tAA.
24. Applies to L-version only.

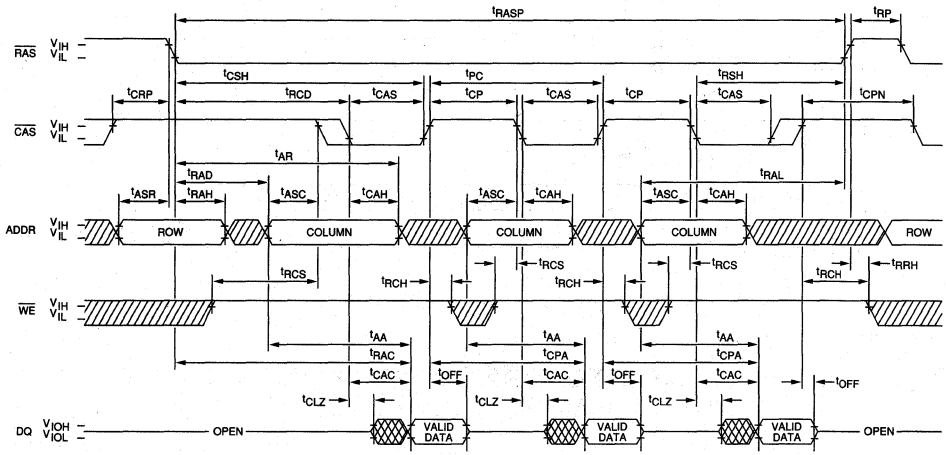
READ CYCLE



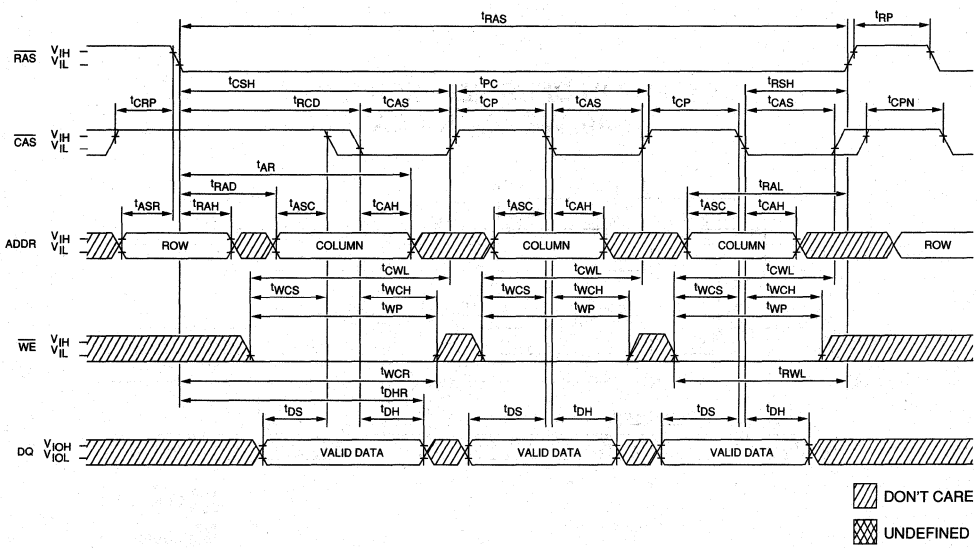
EARLY-WRITE CYCLE



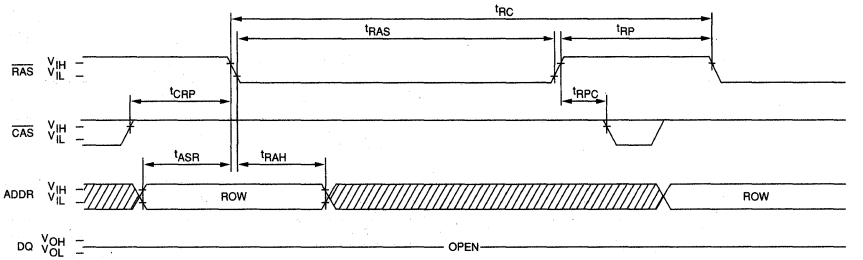
FAST-PAGE-MODE READ CYCLE



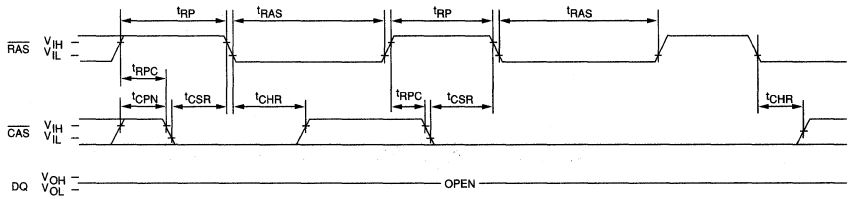
FAST-PAGE-MODE EARLY-WRITE CYCLE



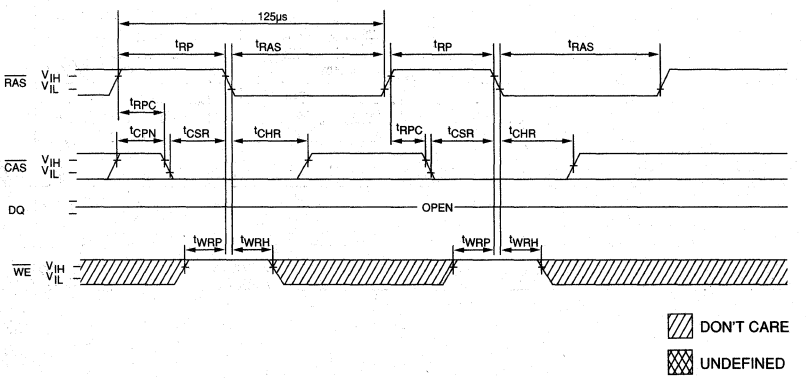
$\overline{RAS}$-ONLY REFRESH CYCLE
(ADDR = A0-A9; $\overline{WE}$ = DON'T CARE)



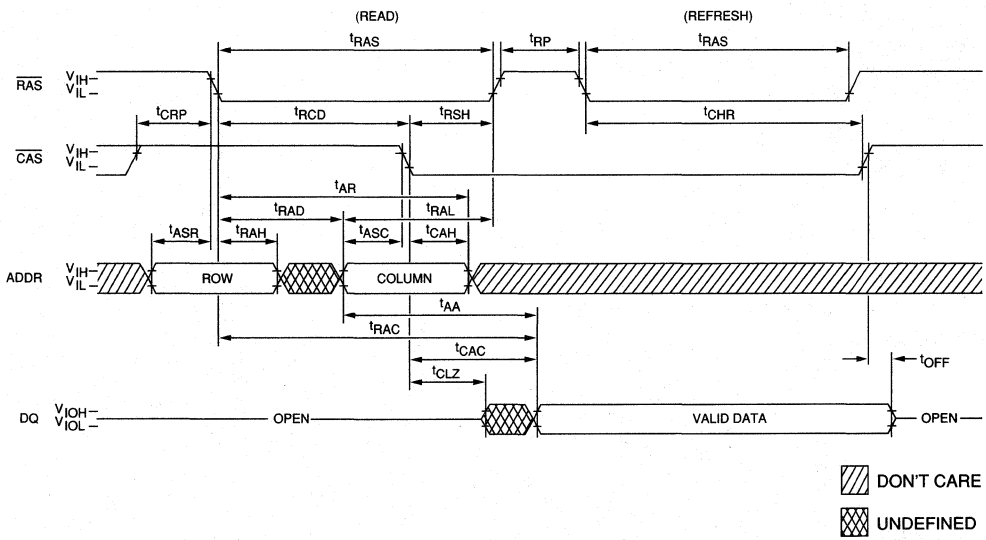
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE
(A0-A9, $\overline{WE}$ = DON'T CARE)



BATTERY BACKUP REFRESH CYCLE [24]
(A0-A9, $\overline{WE}$ = DON'T CARE)



HIDDEN REFRESH CYCLE [20]
($\overline{WE}$ = HIGH)



DRAM MODULE

2 MEG x 32, 4 MEG x 16

FAST PAGE MODE (MT16D232)
LOW POWER,
EXTENDED REFRESH (MT16D232 L)

FEATURES

- Industry standard pinout in a 72-pin single-in-line package
- High-performance, CMOS silicon-gate process.
- Single 5V ±10% power supply
- All device pins are fully TTL compatible
- Low power, 48mW (16mW L-version) standby; 1,824mW active, typical
- Refresh modes: $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$ (CBR) and HIDDEN
- Multiple $\overline{RAS}$ lines allow x16 or x32 width
- 1,024-cycle refresh distributed across 16ms or 1,024-cycle extended refresh distributed across 128ms
- FAST PAGE MODE access cycle
- Low CMOS standby current, 3.2mA maximum (L-version)

OPTIONS MARKING

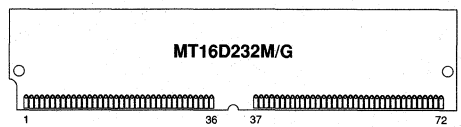
- Timing
  - 60ns access - 6
  - 70ns access - 7
  - 80ns access - 8
- Packages
  - Leadless 72-pin SIMM M
  - Leadless 72-pin SIMM (Gold) G
- Power/Refresh
  - Normal Power/16ms Blank
  - Low Power/128ms L
- Part Number Example: MT16D232GL-6

GENERAL DESCRIPTION

The MT16D232 is a randomly accessed solid-state memory containing 2,097,152 words organized in a x32 configuration. During READ or WRITE cycles each bit is uniquely addressed through the 20 address bits, which are entered 10 bits (A0-A9) at a time. $\overline{RAS}$ is used to latch the first 10 bits and $\overline{CAS}$ the latter 10 bits. A READ or WRITE cycle is selected with the $\overline{WE}$ input. A logic HIGH on $\overline{WE}$ dictates READ mode while a logic LOW on $\overline{WE}$ dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. EARLY-WRITE occurs when $\overline{WE}$ goes LOW prior to $\overline{CAS}$ going LOW, the output pin(s) remain open (High-Z) until the next $\overline{CAS}$ cycle.

PIN ASSIGNMENT (Top View)

72-Pin SIMM
(T-10)

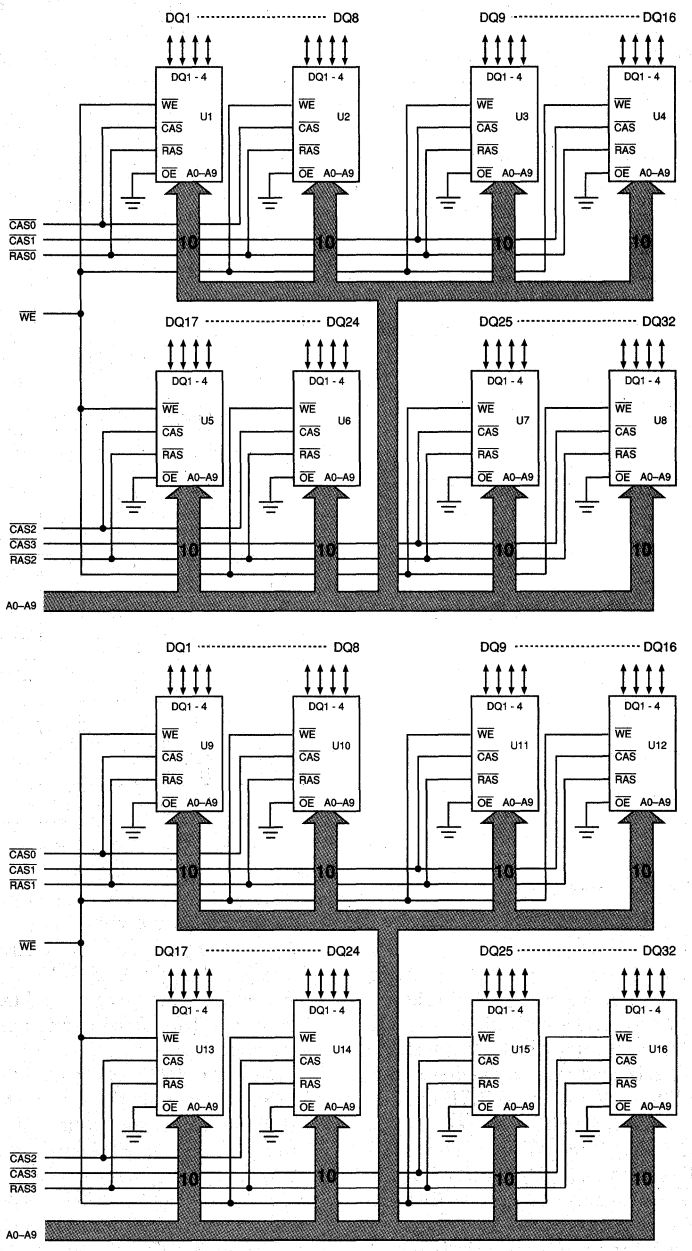


PIN #	SYMBOL	PIN #	SYMBOL	PIN #	SYMBOL	PIN #	SYMBOL
1	Vss	19	NC	37	NC	55	DQ12
2	DQ1	20	DQ5	38	NC	56	DQ28
3	DQ17	21	DQ21	39	Vss	57	DQ13
4	DQ2	22	DQ6	40	$\overline{CAS0}$	58	DQ29
5	DQ18	23	DQ22	41	$\overline{CAS2}$	59	Vcc
6	DQ3	24	DQ7	42	$\overline{CAS3}$	60	DQ30
7	DQ19	25	DQ23	43	$\overline{CAS1}$	61	DQ14
8	DQ4	26	DQ8	44	$\overline{RAS0}$	62	DQ31
9	DQ20	27	DQ24	45	$\overline{RAS1}$	63	DQ15
10	Vcc	28	A7	46	NC	64	DQ32
11	NC	29	NC	47	$\overline{WE}$	65	DQ16
12	A0	30	Vcc	48	NC	66	NC
13	A1	31	A8	49	DQ9	67	PRD1
14	A2	32	A9	50	DQ25	68	PRD2
15	A3	33	$\overline{RAS3}$	51	DQ10	69	PRD3
16	A4	34	$\overline{RAS2}$	52	DQ26	70	PRD4
17	A5	35	NC	53	DQ11	71	NC
18	A6	36	NC	54	DQ27	72	Vss

FAST PAGE MODE operations allow faster data operations (READ or WRITE) within a row-address (A0-A9) defined page boundary. The FAST PAGE MODE cycle is always initiated with a row address strobed-in by $\overline{RAS}$ followed by a column address strobed-in by $\overline{CAS}$. $\overline{CAS}$ may be toggled-in by holding $\overline{RAS}$ LOW and strobing-in different column addresses, thus executing faster memory cycles. Returning $\overline{RAS}$ HIGH terminates the FAST PAGE MODE operation.

Returning $\overline{RAS}$ and $\overline{CAS}$ HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the $\overline{RAS}$ high time. Memory cell data is retained in its correct state by maintaining power and executing any $\overline{RAS}$ cycle (READ, WRITE, $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$ or HIDDEN REFRESH) so that all 1,024 combination of $\overline{RAS}$ addresses (A0-A9) are executed at least every 16ms (128ms on L-version), regardless of sequence.

FUNCTIONAL BLOCK DIAGRAM



U1-U16 = MT4C4001JDJ
U1-U16 = MT4C4001JDJ L (L-version)

TRUTH TABLE

FUNCTION		RAS	CAS	WE	ADDRESSES		DATA IN/OUT
					^tR	^tC	DQ1-DQ32
Standby		H	H→X	X	X	X	High-Z
READ		L	L	H	ROW	COL	Data Out
EARLY-WRITE		L	L	L	ROW	COL	Data In
FAST-PAGE-MODE	1st Cycle	L	H→L	H	ROW	COL	Data Out
READ	2nd Cycle	L	H→L	H	n/a	COL	Data Out
FAST-PAGE-MODE	1st Cycle	L	H→L	L	ROW	COL	Data In
WRITE	2nd Cycle	L	H→L	L	n/a	COL	Data In
RAS-ONLY REFRESH		L	H	X	ROW	n/a	High-Z
HIDDEN	READ	L→H→L	L	H	ROW	COL	Data Out
REFRESH	WRITE	L→H→L	L	L	ROW	COL	Data In
CAS-BEFORE-RAS REFRESH		H→L	L	H	X	X	High-Z
BATTERY BACKUP REFRESH (L-version)		H→L	L	X	X	X	High-Z

PRESENCE DETECT

SYMBOL	-6	-7	-8
PRD1	NC	NC	NC
PRD2	NC	NC	NC
PRD3	NC	Vss	NC
PRD4	NC	NC	Vss

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} ..... -1V to +7V
Operating Temperature, T_A (Ambient) ..... 0°C to +70°C
Storage Temperature (Plastic) ..... -55°C to +125°C
Power Dissipation 16W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 2, 3, 6, 22) (0°C ≤ T_A ≤ 70°C; V_{CC} = 5V ±10%)

PARAMETER/CONDITION		SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage		V_{CC}	4.5	5.5	V	1
Input High (Logic 1) Voltage, All Inputs		V_{IH}	2.4	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, All Inputs		V_{IL}	-1.0	0.8	V	1
INPUT LEAKAGE CURRENT	$\overline{CAS0}$-$\overline{CAS3}$	I_{I1}	-8	8	µA	
Any Input 0V ≤ V_{IN} ≤ V_{CC}	A0-A9, $\overline{WE}$	I_{I2}	-32	32	µA	
(All other pins not under test = 0V) For each package input	$\overline{RAS0}$-$\overline{RAS3}$	I_{I3}	-8	8	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled, 0V ≤ V_{OUT} ≤ V_{CC}) For each package input	DQ1-DQ32	I_{OZ}	-20	20	µA	
OUTPUT LEVELS		V_{OH}	2.4		V	
Output High Voltage (I_{OUT} = -5mA)						
Output Low Voltage (I_{OUT} = 5mA)		V_{OL}		0.4	V	

PARAMETER/CONDITION	SYMBOL	MAX -6	MAX -7	MAX -8	UNITS	NOTES
STANDBY CURRENT: (TTL) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC1}	32	32	32	mA	
STANDBY CURRENT: (CMOS)	I_{CC2}	16	16	16	mA	
($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} -0.2V)		3.2	3.2	3.2	mA	24
OPERATING CURRENT: Random READ/WRITE Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC (MIN))	I_{CC3}	896	816	736	mA	2, 22
OPERATING CURRENT: FAST PAGE MODE Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: ^tPC = ^tPC (MIN))	I_{CC4}	656	576	496	mA	2, 22
REFRESH CURRENT: $\overline{RAS}$-ONLY Average power supply current ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}: ^tRC = ^tRC (MIN))	I_{CC5}	896	816	736	mA	2
REFRESH CURRENT: $\overline{CAS}$-BEFORE-$\overline{RAS}$ Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC (MIN))	I_{CC6}	896	816	736	mA	2, 19
REFRESH CURRENT: BATTERY BACKUP (BBU) Average power supply current during BATTERY BACKUP refresh: $\overline{CAS}$ = 0.2V or $\overline{CAS}$-BEFORE-$\overline{RAS}$ cycling; $\overline{RAS}$ = ^tRAS (MIN) to 300ns; $\overline{WE}$ = Vcc -0.2V; A0-A9 and D_{IN} = Vcc -0.2V or 0.2V (D_{IN} may be left OPEN), ^tRC = 125µs (1,024 rows at 125µs = 128ms)	I_{CC7}	4.8	4.8	4.8	mA	24

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A9	C_{I1}		102	pF	17
Input Capacitance: $\overline{WE}$	C_{I2}		134	pF	17
Input Capacitance: $\overline{CAS0}$-$\overline{CAS3}$, $\overline{RAS0}$-$\overline{RAS3}$	C_{I4}		34	pF	17
Input/Output Capacitance: DQ1-DQ32	C_{IO}		10	pF	17

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 3, 4, 5, 6, 7, 10, 11, 16, 21) (0°C ≤ T_A ≤ 70°C; V_{CC} = 5V ±10%)

AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	^tRC	110		130		150		ns	
READ-WRITE cycle time	^tRWC	n/a		n/a		n/a		ns	21
FAST-PAGE-MODE READ or WRITE cycle time	^tPC	40		40		45		ns	
FAST-PAGE-MODE READ-WRITE cycle time	^tPRWC	n/a		n/a		n/a		ns	21
Access time from $\overline{RAS}$	^tRAC		60		70		80	ns	8
Access time from $\overline{CAS}$	^tCAC		15		20		20	ns	9
Output Enable	^tOE		15		20		20	ns	
Access time from column address	^tAA		30		35		40	ns	
Access time from $\overline{CAS}$ precharge	^tCPA		35		40		45	ns	
$\overline{RAS}$ pulse width	^tRAS	60	100,000	70	100,000	80	100,000	ns	
$\overline{RAS}$ pulse width (FAST PAGE MODE)	^tRASP	60	200,000	70	200,000	80	200,000	ns	
$\overline{RAS}$ hold time	^tRSH	15		20		20		ns	
$\overline{RAS}$ precharge time	^tRP	40		50		60		ns	
$\overline{CAS}$ pulse width	^tCAS	15	100,000	20	100,000	20	100,000	ns	
$\overline{CAS}$ hold time	^tCSH	60		70		80		ns	
$\overline{CAS}$ precharge time	^tCPN	10		10		10		ns	18
$\overline{CAS}$ precharge time (FAST PAGE MODE)	^tCP	10		10		10		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	^tRCD	20	45	20	50	20	60	ns	13
$\overline{CAS}$ to $\overline{RAS}$ precharge time	^tCRP	10		10		10		ns	
Row address setup time	^tASR	0		0		0		ns	
Row address hold time	^tRAH	10		10		10		ns	
$\overline{RAS}$ to column address delay time	^tRAD	15	30	15	35	15	40	ns	23
Column address setup time	^tASC	0		0		0		ns	
Column address hold time	^tCAH	10		15		15		ns	
Column address hold time (referenced to $\overline{RAS}$)	^tAR	50		55		60		ns	
Column address to $\overline{RAS}$ lead time	^tRAL	30		35		40		ns	
Read command setup time	^tRCS	0		0		0		ns	
Read command hold time (referenced to $\overline{CAS}$)	^tRCH	0		0		0		ns	14
Read command hold time (referenced to $\overline{RAS}$)	^tRRH	0		0		0		ns	14
$\overline{CAS}$ to output in Low-Z	^tCLZ	0		0		0		ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

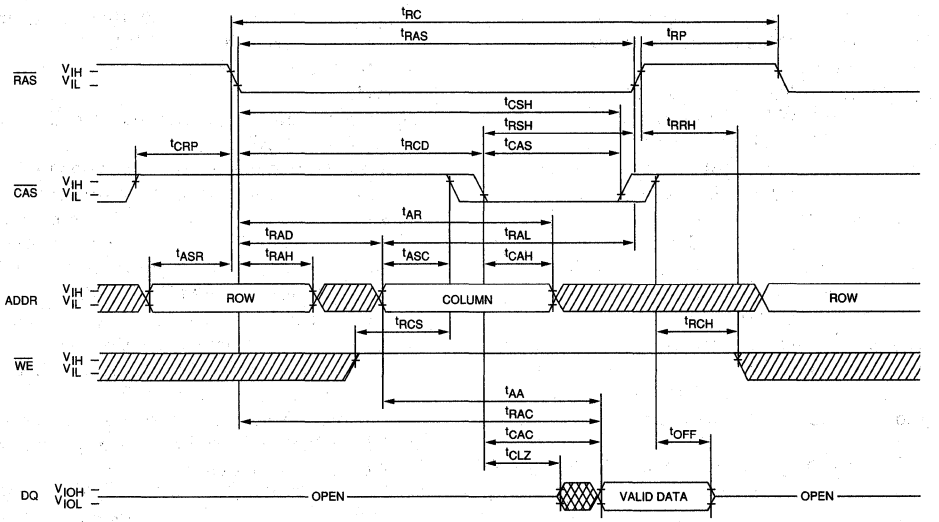
(Notes: 3, 4, 5, 6, 7, 10, 11, 16, 21) (0°C ≤ T_A ≤ 70°C; Vcc = 5V ±10%)

AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Output buffer turn-off delay	^tOFF	0	15	0	20	0	20	ns	12
$\overline{WE}$ command setup time	^tWCS	0		0		0		ns	
Write command hold time	^tWCH	10		15		15		ns	
Write command hold time (referenced to $\overline{RAS}$)	^tWCR	45		55		60		ns	
Write command pulse width	^tWP	10		15		15		ns	
Write command to $\overline{RAS}$ lead time	^tRWL	15		20		20		ns	
Write command to $\overline{CAS}$ lead time	^tCWL	15		20		20		ns	
Data-in setup time	^tDS	0		0		0		ns	15
Data-in hold time	^tDH	10		15		15		ns	15
Data-in hold time (referenced to $\overline{RAS}$)	^tDHR	45		55		60		ns	
Transition time (rise or fall)	^tT	3	50	3	50	3	50	ns	5, 16
Refresh period (1,024 cycles)	^tREF		16/128		16/128		16/128	ms	3/24
$\overline{RAS}$ to $\overline{CAS}$ precharge time	^tRPC	0		0		0		ns	
$\overline{CAS}$ setup time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tCSR	10		10		10		ns	19
$\overline{CAS}$ hold time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tCHR	15		15		15		ns	19
$\overline{WE}$ hold time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tWRH	10		10		10		ns	
$\overline{WE}$ setup time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tWRP	10		10		10		ns	
$\overline{WE}$ hold time (WCBR test cycle)	^tWTH	10		10		10		ns	
$\overline{WE}$ setup time (WCBR test cycle)	^tWTS	10		10		10		ns	

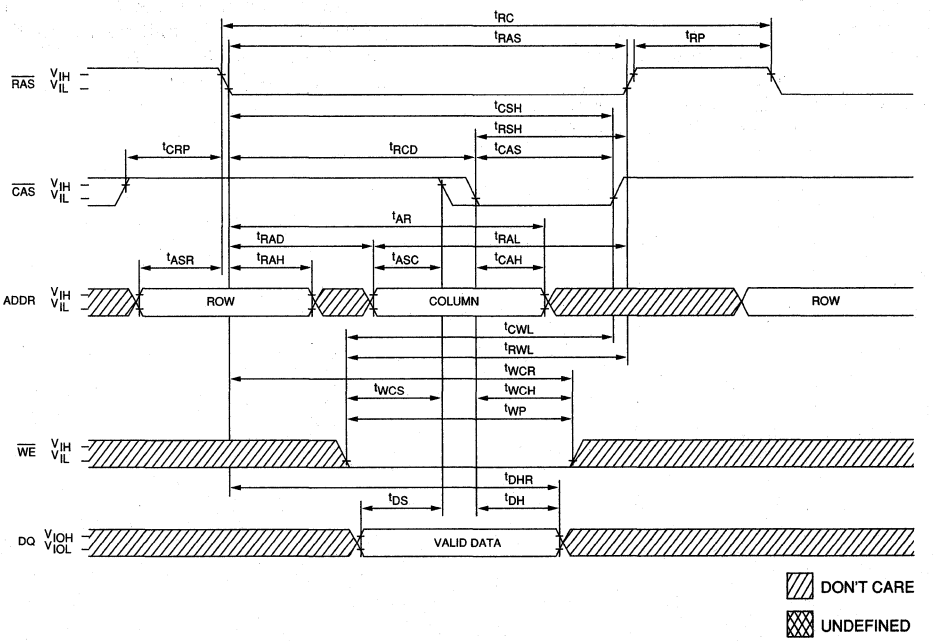
NOTES

1. All voltages referenced to V_{SS}.
2. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
3. An initial pause of 100µs is required after power-up followed by eight $\overline{RAS}$ REFRESH cycles ($\overline{RAS}$-ONLY or CBR with $\overline{WE}$ HIGH) before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-up should be repeated any time the ^tREF refresh requirement is exceeded.
4. AC characteristics assume ^tT = 5ns.
5. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \le T_A \le 70°C$) is assured.
7. Measured with a load equivalent to two TTL gates and 100pF.
8. Assumes that $^tRCD < ^tRCD$ (MAX). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
9. Assumes that $^tRCD \ge ^tRCD$ (MAX).
10. If $\overline{CAS}$ = V_{IH}, data output is High-Z.
11. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
12. ^tOFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
13. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (MAX) limit, then access time is controlled exclusively by ^tCAC.
14. Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
15. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY-WRITE cycles.
16. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
17. This parameter is sampled. Capacitance is measured using MIL-STD-883C, Method 3012.1 (1 MHz AC, Vcc = 5V, DC bias = 2.4V @ 15mV RMS).
18. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, data-out (Q) will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer, $\overline{CAS}$ must be pulsed HIGH for ^tCP.
19. On-chip refresh and address counters are enabled.
20. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW.
21. LATE-WRITE, READ-WRITE or READ-MODIFY-WRITE cycles are not available due to $\overline{OE}$ being grounded on U1-U16.
22. I_{CC} is dependent on cycle rates.
23. Operation within the ^tRAD (MAX) limit ensures that ^tRCD (MAX) can be met. ^tRAD (MAX) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (MAX) limit, then access time is controlled exclusively by ^tAA.
24. Applies to L-version only.

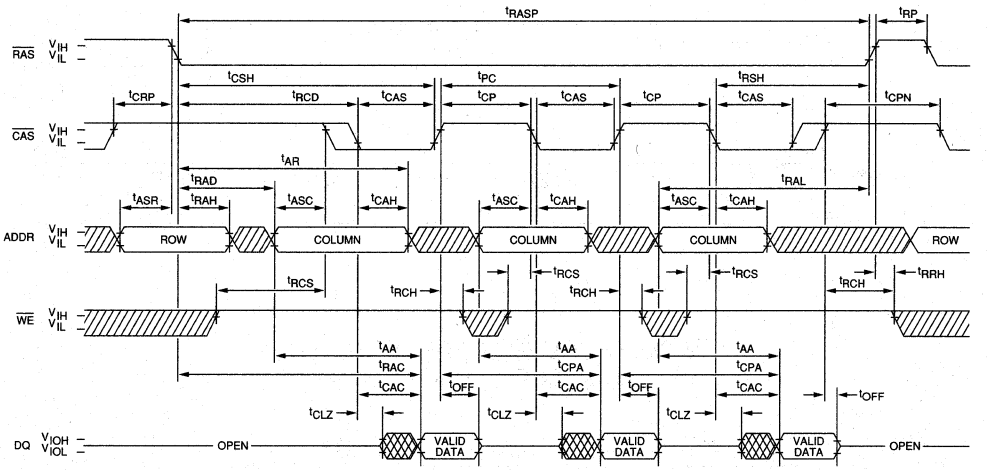
READ CYCLE



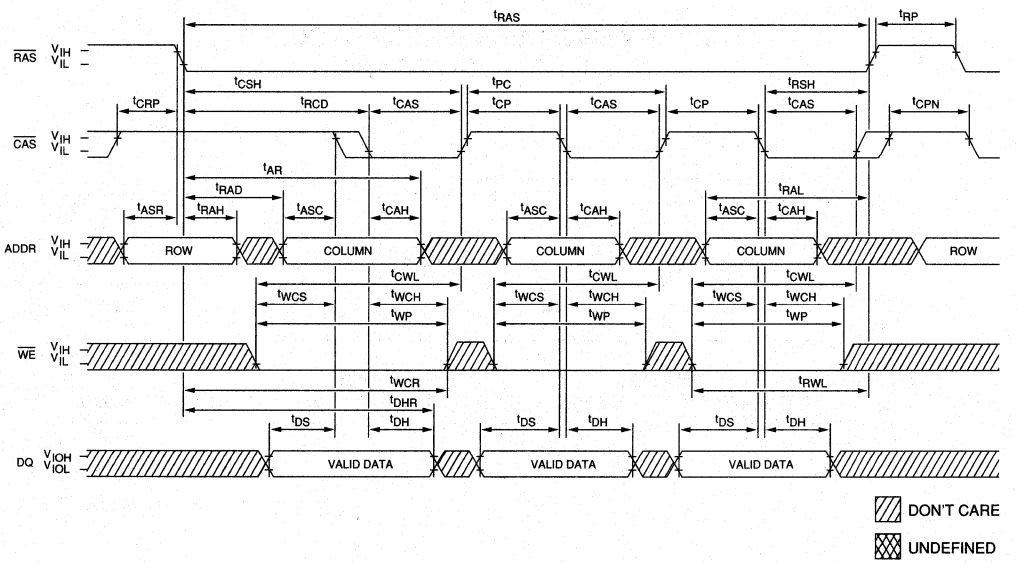
EARLY-WRITE CYCLE



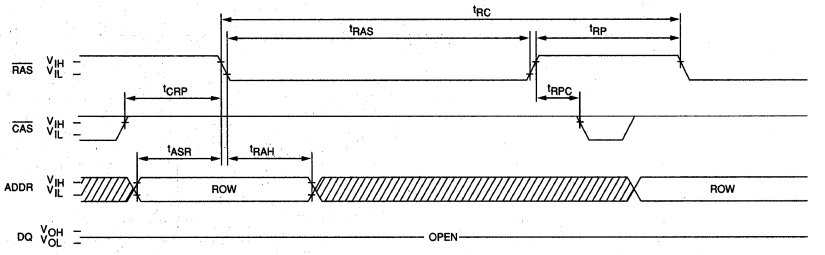
FAST-PAGE-MODE READ CYCLE



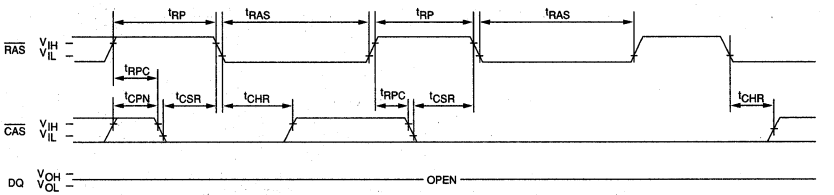
FAST-PAGE-MODE EARLY-WRITE CYCLE



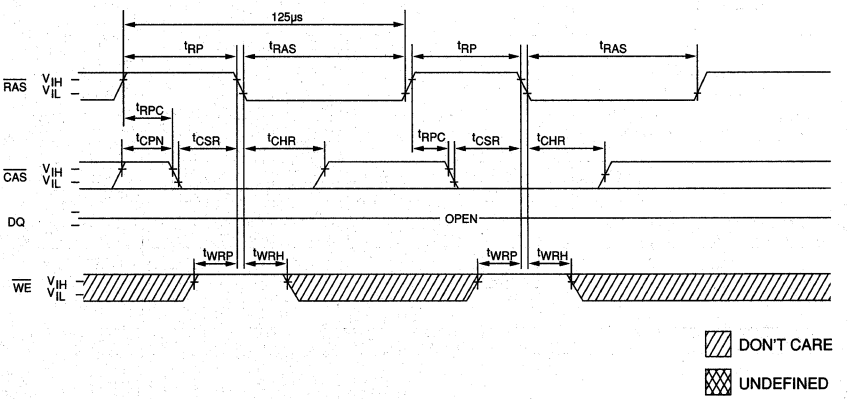
$\overline{RAS}$-ONLY REFRESH CYCLE
(ADDR = A0-A9; $\overline{WE}$ = DON'T CARE)



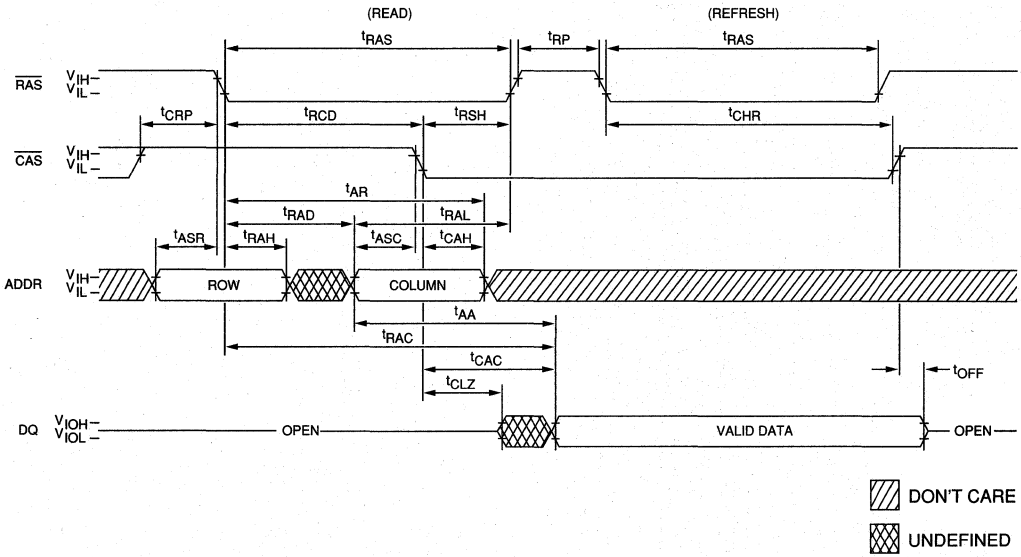
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE
(A0-A9, $\overline{WE}$ = DON'T CARE)



BATTERY BACKUP REFRESH CYCLE [24]
(A0-A9, $\overline{WE}$ = DON'T CARE)



HIDDEN REFRESH CYCLE [20]
($\overline{WE}$ = HIGH)



DRAM MODULE

4 MEG x 32, 8 MEG x 16

FAST PAGE MODE

NEW DRAM MODULE

FEATURES

- Industry standard pinout in a 72-pin single-in-line package
- High-performance, CMOS silicon-gate process
- Single 5V ±10% power supply
- All device pins are fully TTL compatible
- Low power, 40mW standby; 2,200mW active, typical
- Refresh modes: RAS-ONLY, CAS-BEFORE-RAS (CBR) and HIDDEN
- Multiple RAS lines allow x16 or x32 width
- 2,048-cycle refresh distributed across 32ms
- FAST PAGE MODE access cycle

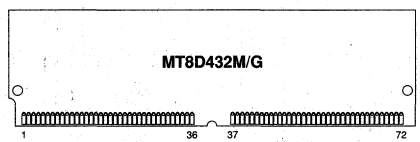
OPTIONS MARKING

- Timing
  - 60ns access - 6
  - 70ns access - 7
  - 80ns access - 8
- Packages
  - Leadless 72-pin SIMM M
  - Leadless 72-pin SIMM (Gold) G
- Part Number Example: MT8D432G-6

PIN ASSIGNMENT (Top View)

72-Pin SIMM

(T-17)



PIN #	SYMBOL	PIN #	SYMBOL	PIN #	SYMBOL	PIN #	SYMBOL
1	Vss	19	A10	37	NC	55	DQ12
2	DQ1	20	DQ5	38	NC	56	DQ28
3	DQ17	21	DQ21	39	Vss	57	DQ13
4	DQ2	22	DQ6	40	CAS0	58	DQ29
5	DQ18	23	DQ22	41	CAS2	59	Vcc
6	DQ3	24	DQ7	42	CAS3	60	DQ30
7	DQ19	25	DQ23	43	CAS1	61	DQ14
8	DQ4	26	DQ8	44	RAS0	62	DQ31
9	DQ20	27	DQ24	45	NC	63	DQ15
10	Vcc	28	A7	46	NC	64	DQ32
11	NC	29	NC	47	WE	65	DQ16
12	A0	30	Vcc	48	NC	66	NC
13	A1	31	A8	49	DQ9	67	PRD1
14	A2	32	A9	50	DQ25	68	PRD2
15	A3	33	NC	51	DQ10	69	PRD3
16	A4	34	RAS2	52	DQ26	70	PRD4
17	A5	35	NC	53	DQ11	71	NC
18	A6	36	NC	54	DQ27	72	Vss

GENERAL DESCRIPTION

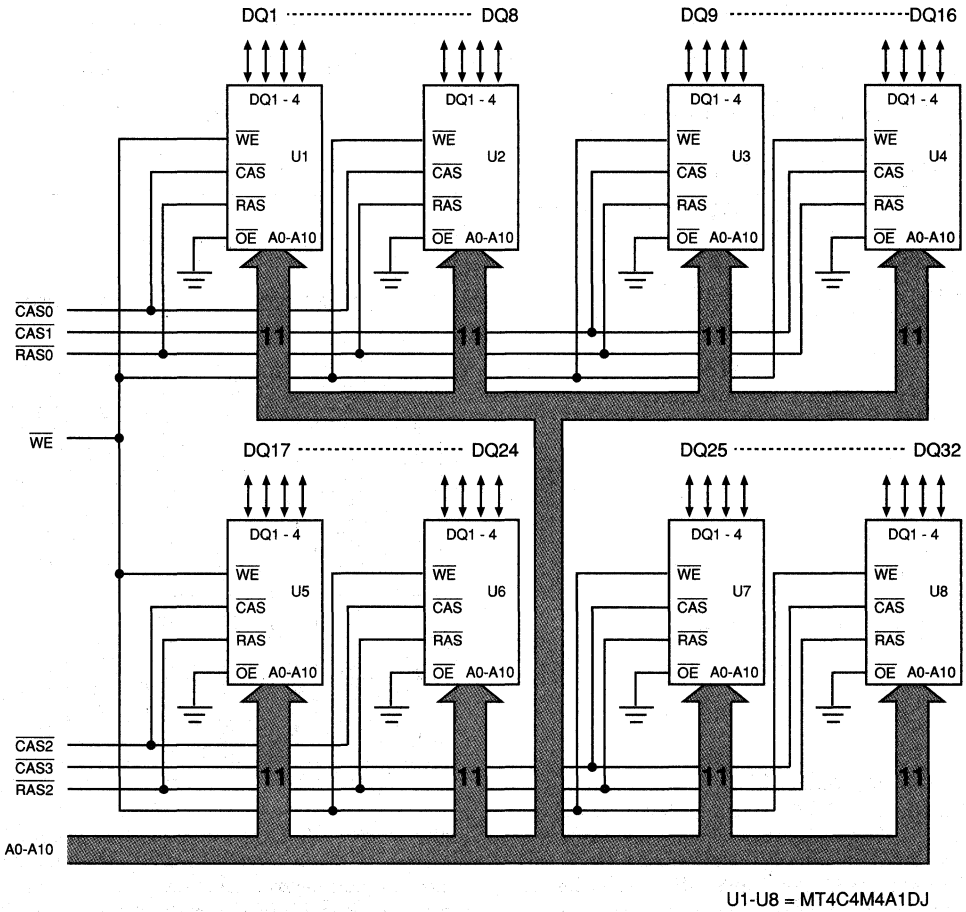
The MT8D432 is a randomly accessed solid-state memory containing 4,194,304 words organized in a x32 configuration. During READ or WRITE cycles, each bit is uniquely addressed through the 22 address bits, which are entered 11 bits (A0-A10) at a time. RAS is used to latch the first 11 bits and CAS the latter 11 bits. A READ or WRITE cycle is selected with the WE input. A logic HIGH on WE dictates READ mode while a logic LOW on WE dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of CAS. Since WE goes LOW prior to CAS going LOW, the output pin(s) remain open (High-Z) until the next CAS cycle.

FAST PAGE MODE operations allow faster data operations (READ or WRITE) within a row-address (A0-A10) defined page boundary. The FAST PAGE MODE cycle is always initiated with a row address strobed-in by RAS followed by a column address strobed-in by CAS. CAS may be toggled-in by holding RAS LOW and strobing-in different column addresses, thus executing faster memory cycles. Returning RAS HIGH terminates the FAST PAGE MODE operation.

Returning RAS and CAS HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the RAS HIGH time. Memory cell data is retained in its correct state by maintaining power and executing any RAS cycle (READ, WRITE, RAS-ONLY, CAS-BEFORE-RAS or HIDDEN REFRESH) so that all 2,048 combinations of RAS addresses (A0-A10) are executed at least every 32ms, regardless of sequence. The CBR REFRESH cycle will invoke the refresh counter for automatic RAS addressing.

NEW ■ DRAM MODULE

FUNCTIONAL BLOCK DIAGRAM



U1-U8 = MT4C4M4A1DJ

TRUTH TABLE

FUNCTION		RAS	CAS	WE	ADDRESSES		DATA IN/OUT
					^tR	^tC	DQ1-DQ8
Standby		H	H→X	X	X	X	High-Z
READ		L	L	H	ROW	COL	Data Out
EARLY-WRITE		L	L	L	ROW	COL	Data In
FAST-PAGE-MODE	1st Cycle	L	H→L	H	ROW	COL	Data Out
READ	2nd Cycle	L	H→L	H	n/a	COL	Data Out
FAST-PAGE-MODE	1st Cycle	L	H→L	L	ROW	COL	Data In
WRITE	2nd Cycle	L	H→L	L	n/a	COL	Data In
RAS-ONLY REFRESH		L	H	X	ROW	n/a	High-Z
HIDDEN	READ	L→H→L	L	H	ROW	COL	Data Out
REFRESH	WRITE	L→H→L	L	L	ROW	COL	Data In
CAS-BEFORE-RAS REFRESH		H→L	L	H	X	X	High-Z

PRESENCE DETECT

SYMBOL	-6	-7	-8
PRD1	Vss	Vss	Vss
PRD2	NC	NC	NC
PRD3	NC	Vss	NC
PRD4	NC	NC	Vss

NEW DRAM MODULE

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} ..... -1V to +7V
Operating Temperature, T_A (Ambient) ..... 0°C to +70°C
Storage Temperature (Plastic) ..... -55°C to +125°C
Power Dissipation 8W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 3, 4, 6, 7) (0°C ≤ T_A ≤ 70°C; V_{CC} = 5V ±10%)

PARAMETER/CONDITION		SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage		V_{CC}	4.5	5.5	V	1
Input High (Logic 1) Voltage, All Inputs		V_{IH}	2.4	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, All Inputs		V_{IL}	-1.0	0.8	V	1
INPUT LEAKAGE CURRENT	$\overline{RAS0}$, $\overline{RAS2}$	I_{I1}	-8	8	µA	
Any Input 0V ≤ V_{IN} ≤ V_{CC}	A0-A10, $\overline{WE}$	I_{I2}	-16	16	µA	
(All other pins not under test = 0V) for each package input	$\overline{CAS0}$-$\overline{CAS3}$	I_{I3}	-4	4	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled, 0V ≤ V_{OUT} ≤ V_{CC}) for each package input	DQ1-DQ32	I_{OZ}	-10	10	µA	
OUTPUT LEVELS		V_{OH}	2.4		V	
Output High Voltage (I_{OUT} = -5mA)						
Output Low Voltage (I_{OUT} = 5mA)		V_{OL}		0.4	V	

		MAX				
PARAMETER/CONDITION	SYMBOL	-6	-7	-8	UNITS	NOTES
STANDBY CURRENT: (TTL) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC1}	16	16	16	mA	
STANDBY CURRENT: (CMOS) ($\overline{RAS}$ = $\overline{CAS}$ = Other Inputs = V_{CC} -0.2V)	I_{CC2}	8	8	8	mA	
OPERATING CURRENT: Random READ/WRITE Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC (MIN))	I_{CC3}	960	800	680	mA	3, 4
OPERATING CURRENT: FAST PAGE MODE Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: ^tPC = ^tPC (MIN))	I_{CC4}	640	560	480	mA	3, 4
REFRESH CURRENT: $\overline{RAS}$-ONLY Average power supply current ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}: ^tRC = ^tRC (MIN))	I_{CC5}	960	800	680	mA	3
REFRESH CURRENT: $\overline{CAS}$-BEFORE-$\overline{RAS}$ Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC (MIN))	I_{CC6}	960	800	680	mA	3, 5

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A10	C_{I1}		51	pF	2
Input Capacitance: $\overline{WE}$	C_{I2}		67	pF	2
Input Capacitance: $\overline{RAS0}$, $\overline{RAS2}$	C_{I3}		34	pF	2
Input Capacitance: $\overline{CAS0}$, $\overline{CAS1}$, $\overline{CAS2}$, $\overline{CAS3}$	C_{I4}		17	pF	2
Input/Output Capacitance: DQ1-DQ32	C_{IO}		10	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13, 22) (V_{CC} = 5V ±10%)

AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	^tRC	110		130		150		ns	
READ-WRITE cycle time	^tRWC	n/a		n/a		n/a		ns	22
FAST-PAGE-MODE READ or WRITE cycle time	^tPC	40		40		45		ns	
FAST-PAGE-MODE READ-WRITE cycle time	^tPRWC	n/a		n/a		n/a		ns	22
Access time from $\overline{RAS}$	^tRAC		60		70		80	ns	14
Access time from $\overline{CAS}$	^tCAC		15		20		20	ns	15
Access time from column address	^tAA		30		35		40	ns	
Access time from $\overline{CAS}$ precharge	^tCPA		40		40		45	ns	
$\overline{RAS}$ pulse width	^tRAS	60	100,000	70	100,000	80	100,000	ns	
$\overline{RAS}$ pulse width (FAST PAGE MODE)	^tRASP	60	100,000	70	100,000	80	100,000	ns	
$\overline{RAS}$ hold time	^tRSH	15		20		20		ns	
$\overline{RAS}$ precharge time	^tRP	40		50		60		ns	
$\overline{CAS}$ pulse width	^tCAS	15	100,000	20	100,000	20	100,000	ns	
$\overline{CAS}$ hold time	^tCSH	60		70		80		ns	
$\overline{CAS}$ precharge time	^tCPN	10		10		10		ns	16
$\overline{CAS}$ precharge time (FAST PAGE MODE)	^tCP	10		10		10		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	^tRCD	20	45	20	50	20	60	ns	17
$\overline{CAS}$ to $\overline{RAS}$ precharge time	^tCRP	5		5		5		ns	
Row address setup time	^tASR	0		0		0		ns	
Row address hold time	^tRAH	10		10		10		ns	
$\overline{RAS}$ to column address delay time	^tRAD	15	30	15	35	15	40	ns	18
Column address setup time	^tASC	0		0		0		ns	
Column address hold time	^tCAH	10		15		15		ns	
Column address hold time (referenced to $\overline{RAS}$)	^tAR	50		55		60		ns	
Column address to $\overline{RAS}$ lead time	^tRAL	30		35		40		ns	
Read command setup time	^tRCS	0		0		0		ns	
Read command hold time (referenced to $\overline{CAS}$)	^tRCH	0		0		0		ns	19
Read command hold time (referenced to $\overline{RAS}$)	^tRRH	0		0		0		ns	19
$\overline{CAS}$ to output in Low-Z	^tCLZ	0		0		0		ns	

NEW DRAM MODULE

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13, 22) (V_{CC} = 5V ±10%)

AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Output buffer turn-off delay	^tOFF	0	15	0	20	0	20	ns	20
$\overline{WE}$ command setup time	^tWCS	0		0		0		ns	
Write command hold time	^tWCH	10		15		15		ns	
Write command hold time (referenced to $\overline{RAS}$)	^tWCR	45		55		60		ns	
Write command pulse width	^tWP	10		15		15		ns	
Write command to $\overline{RAS}$ lead time	^tRWL	15		20		20		ns	
Write command to $\overline{CAS}$ lead time	^tCWL	15		20		20		ns	
Data-in setup time	^tDS	0		0		0		ns	21
Data-in hold time	^tDH	10		15		15		ns	21
Data-in hold time (referenced to $\overline{RAS}$)	^tDHR	45		55		60		ns	
Transition time (rise or fall)	^tT	3	50	3	50	3	50	ns	9, 10
Refresh period (2,048 cycles)	^tREF		32		32		32	ms	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	^tRPC	0		0		0		ns	
$\overline{CAS}$ setup time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tCSR	5		5		5		ns	5
$\overline{CAS}$ hold time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tCHR	15		15		15		ns	5
$\overline{WE}$ hold time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tWRH	10		10		10		ns	24
$\overline{WE}$ setup time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tWRP	10		10		10		ns	24
$\overline{WE}$ hold time (WCBR test cycle)	^tWTH	10		10		10		ns	24
$\overline{WE}$ setup time (WCBR test cycle)	^tWTS	10		10		10		ns	24

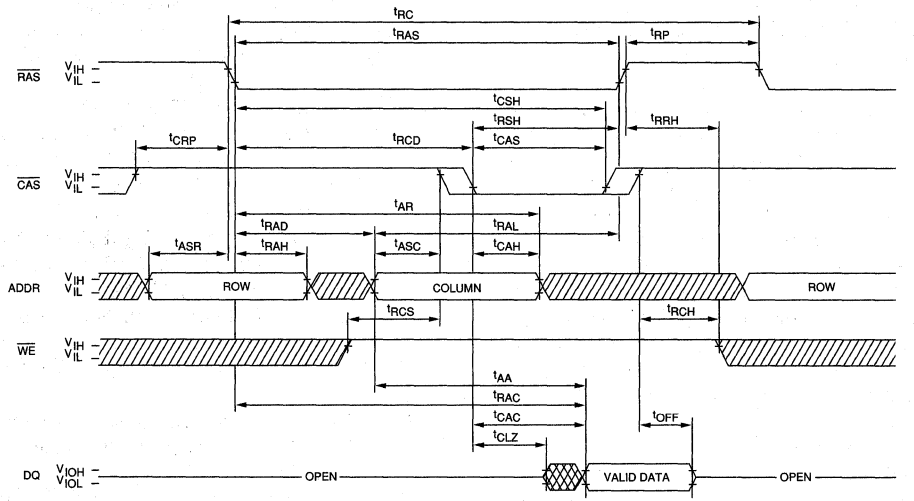
NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. Capacitance is measured using MIL-STD-883C, Method 3012.1 (1 MHz AC, Vcc = 5V, DC bias = 2.4V @ 15mV RMS)
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is assured.
7. An initial pause of 100µs is required after power-up followed by eight $\overline{RAS}$ refresh cycles ($\overline{RAS}$-ONLY or CBR with $\overline{WE}$ HIGH) before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-up should be repeated any time the ^{t}REF refresh requirement is exceeded.
8. AC characteristics assume ^{t}T = 5ns.
9. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS}$ = V_{IH}, data output is High-Z.
12. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to 2 TTL gates and 100pF.
14. Assumes that $^{t}RCD < {}^{t}RCD$ (MAX). If ^{t}RCD is greater than the maximum recommended value shown in this table, ^{t}RAC will increase by the amount that ^{t}RCD exceeds the value shown.
15. Assumes that $^{t}RCD \geq {}^{t}RCD$ (MAX).
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer, $\overline{CAS}$ must be pulsed HIGH for ^{t}CPN.
17. Operation within the ^{t}RCD (MAX) limit ensures that ^{t}RAC (MAX) can be met. ^{t}RCD (MAX) is specified as a reference point only; if ^{t}RCD is greater than the specified ^{t}RCD (MAX) limit, then access time is controlled exclusively by ^{t}CAC.
18. Operation within the ^{t}RAD (MAX) limit ensures that ^{t}RCD (MAX) can be met. ^{t}RAD (MAX) is specified as a reference point only; if ^{t}RAD is greater than the specified ^{t}RAD (MAX) limit, then access time is controlled exclusively by ^{t}AA.
19. Either ^{t}RCH or ^{t}RRH must be satisfied for a READ cycle.
20. ^{t}OFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
21. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY-WRITE cycles.
22. $\overline{OE}$ is tied permanently LOW, LATE-WRITE or READ-MODIFY-WRITE operations are not possible.
23. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW and $\overline{OE}$ = HIGH.
24. ^{t}WTS and ^{t}WTH are setup and hold specifications for the $\overline{WE}$ pin being held LOW to enable the JEDEC test mode (with CBR timing constraints). These two parameters are the inverts of ^{t}WRP and ^{t}WRH in the CBR refresh cycle.

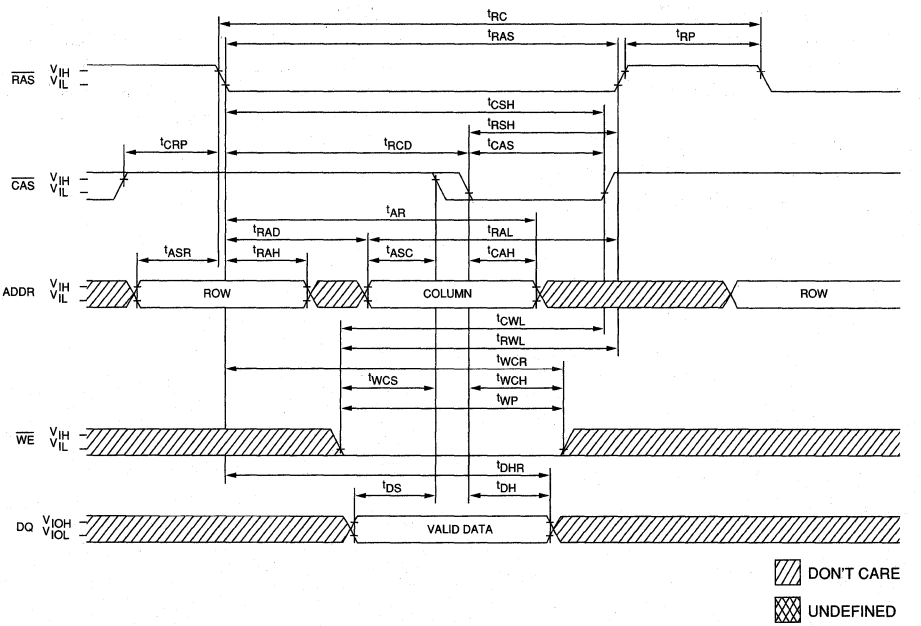
NEW DRAM MODULE

NEW DRAM MODULE

READ CYCLE

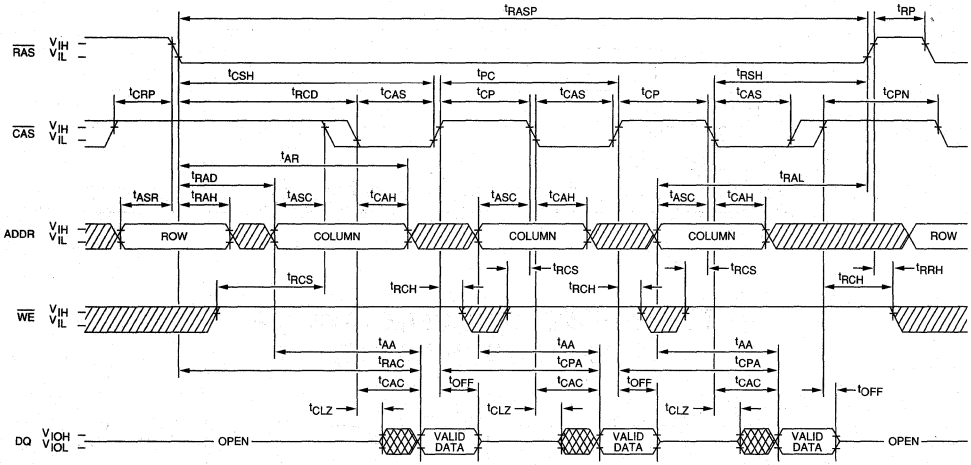


EARLY-WRITE CYCLE

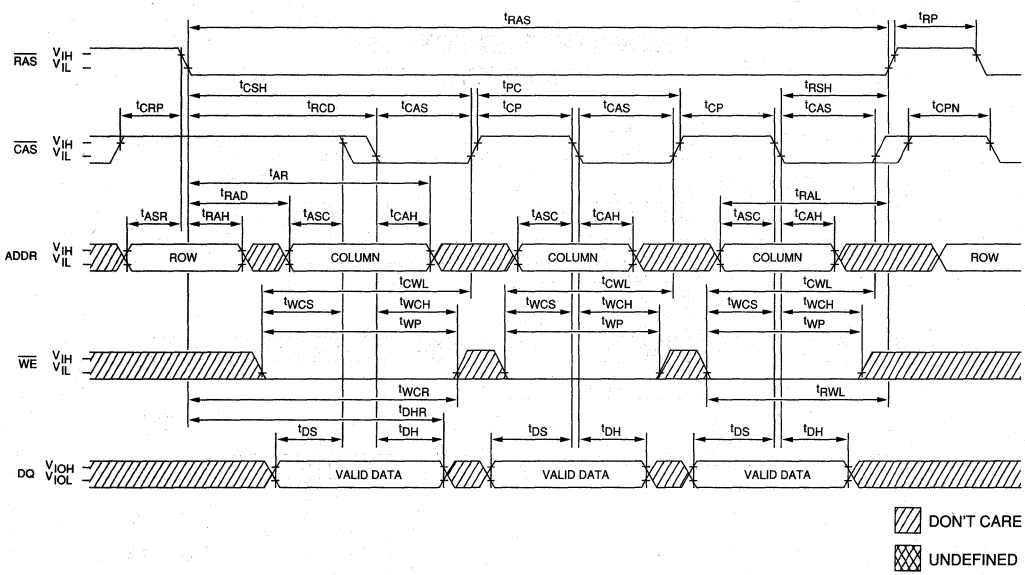


NEW DRAM MODULE

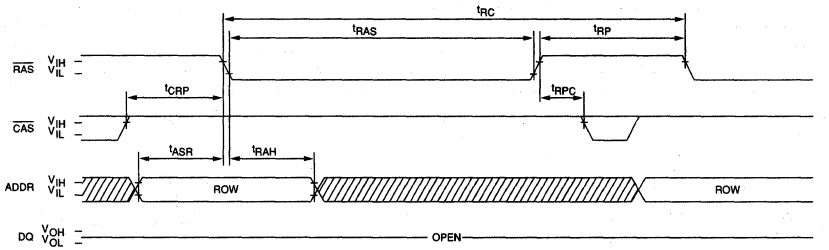
FAST-PAGE-MODE READ CYCLE



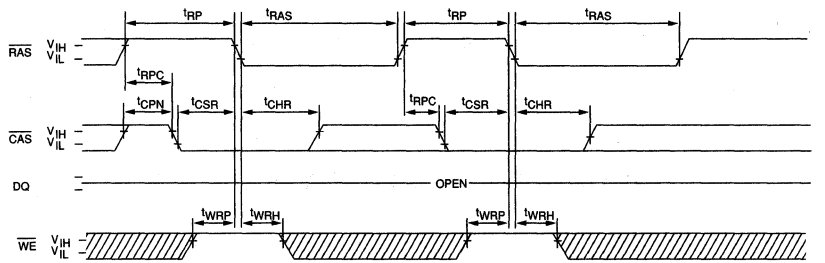
FAST-PAGE-MODE EARLY-WRITE CYCLE



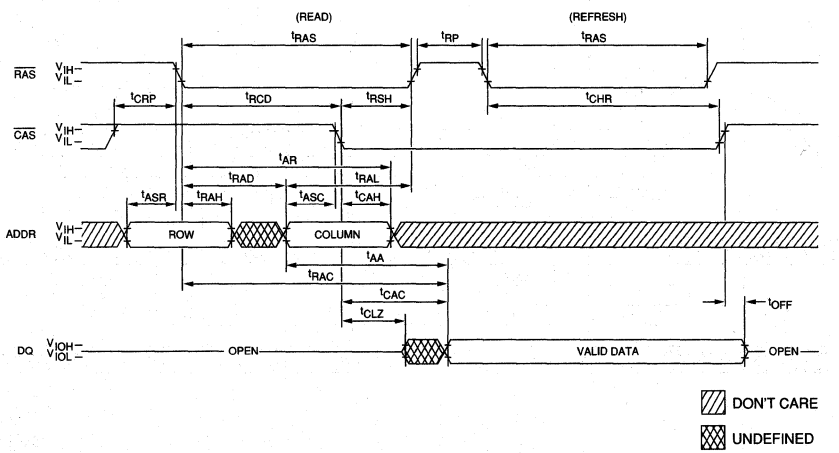
$\overline{RAS}$-ONLY REFRESH CYCLE
(ADDR = A0-A10; $\overline{WE}$ = DON'T CARE)



$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE
(A0-A10 = DON'T CARE)



HIDDEN REFRESH CYCLE [23]
($\overline{WE}$ = HIGH)



DRAM MODULE

8 MEG x 32,16 MEG x16
FAST PAGE MODE

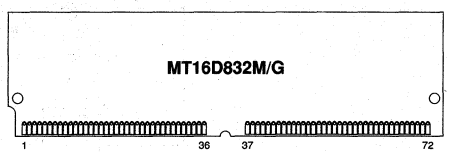
NEW DRAM MODULE

FEATURES
- Industry standard pinout in a 72-pin single-in-line package
- High-performance, CMOS silicon-gate process
- Single 5V ±10% power supply
- All device pins are fully TTL compatible
- Low power, 80mW standby; 2,240mW active, typical
- Refresh modes: RAS-ONLY, CAS-BEFORE-RAS (CBR) and HIDDEN
- 2,048-cycle refresh distributed across 32ms
- FAST PAGE MODE access cycle
- Multiple RAS lines allow x16 or x32 width

OPTIONS MARKING
- Timing
  - 60ns access - 6
  - 70ns access - 7
  - 80ns access - 8
- Packages
  - Leadless 72-pin SIMM M
  - Leadless 72-pin SIMM (Gold) G
- Part Number Example: MT16D832G-6

PIN ASSIGNMENT (Top View)

72-Pin SIMM
(T-18)



PIN #	SYMBOL	PIN #	SYMBOL	PIN #	SYMBOL	PIN #	SYMBOL
1	Vss	19	A10	37	NC	55	DQ12
2	DQ1	20	DQ5	38	NC	56	DQ28
3	DQ17	21	DQ21	39	Vss	57	DQ13
4	DQ2	22	DQ6	40	CAS0	58	DQ29
5	DQ18	23	DQ22	41	CAS2	59	Vcc
6	DQ3	24	DQ7	42	CAS3	60	DQ30
7	DQ19	25	DQ23	43	CAS1	61	DQ14
8	DQ4	26	DQ8	44	RAS0	62	DQ31
9	DQ20	27	DQ24	45	RAS1	63	DQ15
10	Vcc	28	A7	46	NC	64	DQ32
11	NC	29	NC	47	WE	65	DQ16
12	A0	30	Vcc	48	NC	66	NC
13	A1	31	A8	49	DQ9	67	PRD1
14	A2	32	A9	50	DQ25	68	PRD2
15	A3	33	RAS3	51	DQ10	69	PRD3
16	A4	34	RAS2	52	DQ26	70	PRD4
17	A5	35	NC	53	DQ11	71	NC
18	A6	36	NC	54	DQ27	72	Vss

GENERAL DESCRIPTION

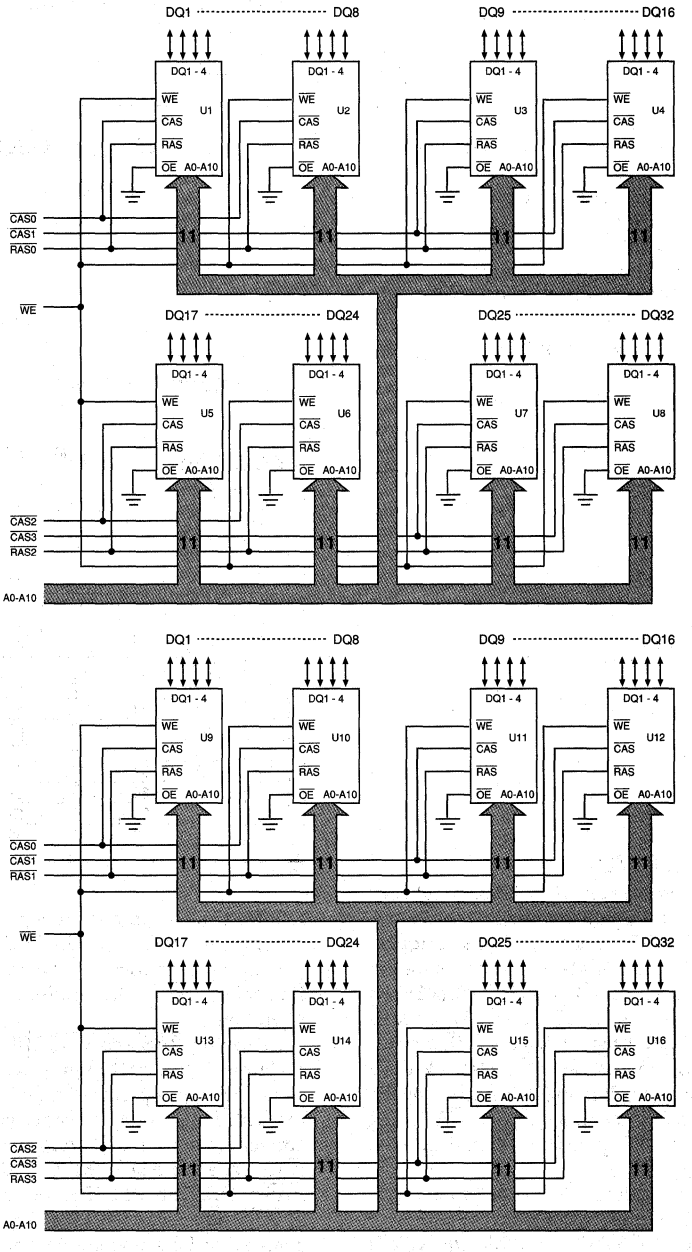
The MT16D832 is a randomly accessed solid-state memory containing 8,388,608 words organized in a x32 configuration. During READ or WRITE cycles, each bit is uniquely addressed through the 22 address bits, which are entered 11 bits (A0-A10) at a time. RAS is used to latch the first 11 bits and CAS the latter 11 bits. A READ or WRITE cycle is selected with the WE input. A logic HIGH on WE dictates READ mode while a logic LOW on WE dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of CAS. Since WE goes LOW prior to CAS going LOW, the output pin(s) remain open (High-Z) until the next CAS cycle.

FAST PAGE MODE operations allow faster data operations (READ or WRITE) within a row-address (A0-A10) defined page boundary. The FAST PAGE MODE cycle is always initiated with a row address strobed-in by RAS followed by a column address strobed-in by CAS. CAS may be toggled-in by holding RAS LOW and strobing-in different column addresses, thus executing faster memory cycles. Returning RAS HIGH terminates the FAST PAGE MODE operation.

Returning RAS and CAS HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the RAS HIGH time. Memory cell data is retained in its correct state by maintaining power and executing any RAS cycle (READ, WRITE, RAS-ONLY, CAS-BEFORE-RAS or HIDDEN REFRESH) so that all 2,048 combinations of RAS addresses (A0-A10) are executed at least every 32ms, regardless of sequence. The CBR REFRESH cycle will invoke the refresh counter for automatic RAS addressing.

NEW ■ DRAM MODULE

FUNCTIONAL BLOCK DIAGRAM



U1-U16 = MT4C4MA1DJ

TRUTH TABLE

FUNCTION		RAS	CAS	WE	ADDRESSES		DATA IN/OUT
					^tR	^tC	DQ1-DQ32
Standby		H	H→X	X	X	X	High-Z
READ		L	L	H	ROW	COL	Data Out
EARLY-WRITE		L	L	L	ROW	COL	Data In
FAST-PAGE-MODE	1st Cycle	L	H→L	H	ROW	COL	Data Out
READ	2nd Cycle	L	H→L	H	n/a	COL	Data Out
FAST-PAGE-MODE	1st Cycle	L	H→L	L	ROW	COL	Data In
WRITE	2nd Cycle	L	H→L	L	n/a	COL	Data In
RAS-ONLY REFRESH		L	H	X	ROW	n/a	High-Z
HIDDEN	READ	L→H→L	L	H	ROW	COL	Data Out
REFRESH	WRITE	L→H→L	L	L	ROW	COL	Data In
CAS-BEFORE-RAS REFRESH		H→L	L	H	X	X	High-Z

PRESENCE DETECT

SYMBOL	-6	-7	-8
PRD1	NC	NC	NC
PRD2	Vss	Vss	Vss
PRD3	NC	Vss	NC
PRD4	NC	NC	Vss

NEW DRAM MODULE

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} ..... -1V to +7V
Operating Temperature, T_A (Ambient) ..... 0°C to +70°C
Storage Temperature (Plastic) ..... -55°C to +125°C
Power Dissipation 16W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 3, 4, 6, 7) (0°C ≤ T_A ≤ 70°C; V_{CC} = 5V ±10%)

PARAMETER/CONDITION		SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage		V_{CC}	4.5	5.5	V	1
Input High (Logic 1) Voltage, All Inputs		V_{IH}	2.4	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, All Inputs		V_{IL}	-1.0	0.8	V	1
INPUT LEAKAGE CURRENT	$\overline{RAS0}$-$\overline{RAS3}$	I_{I1}	-8	8	µA	
Any Input 0V ≤ V_{IN} ≤ V_{CC}	A0-A10, $\overline{WE}$	I_{I2}	-32	32	µA	
(All other pins not under test = 0V) for each package input	$\overline{CAS0}$-$\overline{CAS3}$	I_{I3}	-8	8	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled, 0V ≤ V_{OUT} ≤ V_{CC}) for each package input	DQ1-DQ32	I_{OZ}	-20	20	µA	
OUTPUT LEVELS		V_{OH}	2.4		V	
Output High Voltage (I_{OUT} = -5mA)						
Output Low Voltage (I_{OUT} = 5mA)		V_{OL}		0.4	V	

		MAX				
PARAMETER/CONDITION	SYMBOL	-6	-7	-8	UNITS	NOTES
STANDBY CURRENT: (TTL) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC1}	32	32	32	mA	
STANDBY CURRENT: (CMOS) ($\overline{RAS}$ = $\overline{CAS}$ = Other Inputs = V_{CC} -0.2V)	I_{CC2}	16	16	16	mA	
OPERATING CURRENT: Random READ/WRITE Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC (MIN))	I_{CC3}	976	816	696	mA	3, 4
OPERATING CURRENT: FAST PAGE MODE Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: ^tPC = ^tPC (MIN))	I_{CC4}	656	576	496	mA	3, 4
REFRESH CURRENT: $\overline{RAS}$-ONLY Average power supply current ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}: ^tRC = ^tRC (MIN))	I_{CC5}	976	816	696	mA	3
REFRESH CURRENT: $\overline{CAS}$-BEFORE-$\overline{RAS}$ Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC (MIN))	I_{CC6}	976	816	696	mA	3, 5

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A10	C_{I1}		102	pF	2
Input Capacitance: $\overline{WE}$	C_{I2}		134	pF	2
Input Capacitance: $\overline{RAS0}$, $\overline{RAS1}$, $\overline{RAS2}$, $\overline{RAS3}$	C_{I3}		34	pF	2
Input Capacitance: $\overline{CAS0}$, $\overline{CAS1}$, $\overline{CAS2}$, $\overline{CAS3}$	C_{I4}		34	pF	2
Input/Output Capacitance: DQ1-DQ32	C_{IO}		20	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13, 22) (V_{CC} = 5V ±10%)

AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	t_{RC}	110		130		150		ns	
READ-WRITE cycle time	t_{RWC}	n/a		n/a		n/a		ns	22
FAST-PAGE-MODE READ or WRITE cycle time	t_{PC}	40		40		45		ns	
FAST-PAGE-MODE READ-WRITE cycle time	t_{PRWC}	n/a		n/a		n/a		ns	22
Access time from $\overline{RAS}$	t_{RAC}		60		70		80	ns	14
Access time from $\overline{CAS}$	t_{CAC}		15		20		20	ns	15
Access time from column address	t_{AA}		30		35		40	ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		40		40		45	ns	
$\overline{RAS}$ pulse width	t_{RAS}	60	100,000	70	100,000	80	100,000	ns	
$\overline{RAS}$ pulse width (FAST PAGE MODE)	t_{RASP}	60	100,000	70	100,000	80	100,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	15		20		20		ns	
$\overline{RAS}$ precharge time	t_{RP}	40		50		60		ns	
$\overline{CAS}$ pulse width	t_{CAS}	15	100,000	20	100,000	20	100,000	ns	
$\overline{CAS}$ hold time	t_{CSH}	60		70		80		ns	
$\overline{CAS}$ precharge time	t_{CPN}	10		10		10		ns	16
$\overline{CAS}$ precharge time (FAST PAGE MODE)	t_{CP}	10		10		10		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	45	20	50	20	60	ns	17
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		5		ns	
Row address setup time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	10		10		10		ns	
$\overline{RAS}$ to column address delay time	t_{RAD}	15	30	15	35	15	40	ns	18
Column address setup time	t_{ASC}	0		0		0		ns	
Column address hold time	t_{CAH}	10		15		15		ns	
Column address hold time (referenced to $\overline{RAS}$)	t_{AR}	50		55		60		ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	30		35		40		ns	
Read command setup time	t_{RCS}	0		0		0		ns	
Read command hold time (referenced to $\overline{CAS}$)	t_{RCH}	0		0		0		ns	19
Read command hold time (referenced to $\overline{RAS}$)	t_{RRH}	0		0		0		ns	19
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	0		0		0		ns	

NEW DRAM MODULE

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13, 22) (V_{CC} = 5V ±10%)

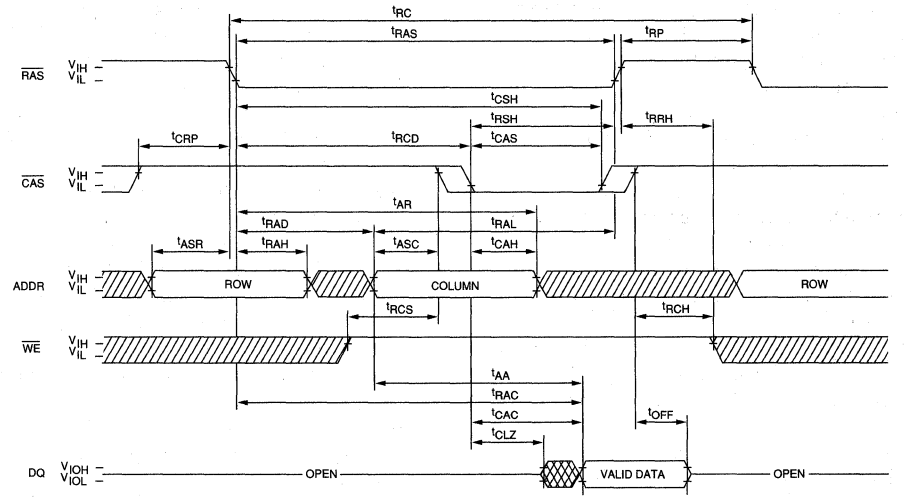
AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Output buffer turn-off delay	^tOFF	0	15	0	20	0	20	ns	20
$\overline{WE}$ command setup time	^tWCS	0		0		0		ns	
Write command hold time	^tWCH	10		15		15		ns	
Write command hold time (referenced to $\overline{RAS}$)	^tWCR	45		55		60		ns	
Write command pulse width	^tWP	10		15		15		ns	
Write command to $\overline{RAS}$ lead time	^tRWL	15		20		20		ns	
Write command to $\overline{CAS}$ lead time	^tCWL	15		20		20		ns	
Data-in setup time	^tDS	0		0		0		ns	21
Data-in hold time	^tDH	10		15		15		ns	21
Data-in hold time (referenced to $\overline{RAS}$)	^tDHR	45		55		60		ns	
Transition time (rise or fall)	^tT	3	50	3	50	3	50	ns	9, 10
Refresh period (2,048 cycles)	^tREF		32		32		32	ms	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	^tRPC	0		0		0		ns	
$\overline{CAS}$ setup time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tCSR	5		5		5		ns	5
$\overline{CAS}$ hold time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tCHR	15		15		15		ns	5
$\overline{WE}$ hold time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tWRH	10		10		10		ns	24
$\overline{WE}$ setup time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tWRP	10		10		10		ns	24
$\overline{WE}$ hold time (WCBR test cycle)	^tWTH	10		10		10		ns	24
$\overline{WE}$ setup time (WCBR test cycle)	^tWTS	10		10		10		ns	24

NOTES

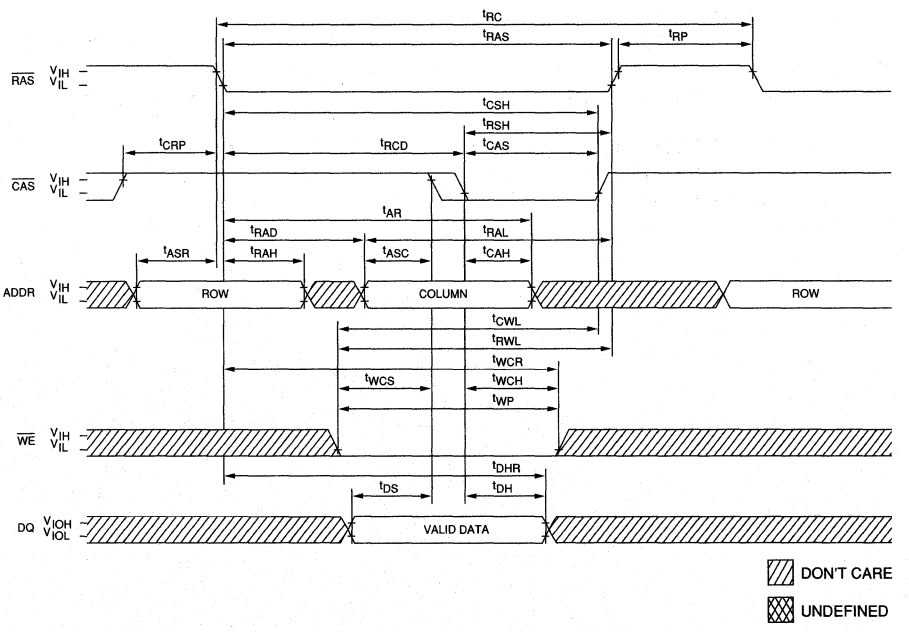
1. All voltages referenced to V_{SS}.
2. This parameter is sampled. Capacitance is measured using MIL-STD-883C, Method 3012.1 (1 MHz AC, Vcc = 5V, DC bias = 2.4V @ 15mV RMS)
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is assured.
7. An initial pause of 100µs is required after power-up followed by eight $\overline{RAS}$ refresh cycles ($\overline{RAS}$-ONLY or CBR with $\overline{WE}$ HIGH) before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-up should be repeated any time the ^{t}REF refresh requirement is exceeded.
8. AC characteristics assume ^{t}T = 5ns.
9. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS}$ = V_{IH}, data output is High-Z.
12. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to 2 TTL gates and 100pF.
14. Assumes that $^{t}RCD < {}^{t}RCD$ (MAX). If ^{t}RCD is greater than the maximum recommended value shown in this table, ^{t}RAC will increase by the amount that ^{t}RCD exceeds the value shown.
15. Assumes that $^{t}RCD \geq {}^{t}RCD$ (MAX).
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer, $\overline{CAS}$ must be pulsed HIGH for ^{t}CPN.
17. Operation within the ^{t}RCD (MAX) limit ensures that ^{t}RAC (MAX) can be met. ^{t}RCD (MAX) is specified as a reference point only; if ^{t}RCD is greater than the specified ^{t}RCD (MAX) limit, then access time is controlled exclusively by ^{t}CAC.
18. Operation within the ^{t}RAD (MAX) limit ensures that ^{t}RCD (MAX) can be met. ^{t}RAD (MAX) is specified as a reference point only; if ^{t}RAD is greater than the specified ^{t}RAD (MAX) limit, then access time is controlled exclusively by ^{t}AA.
19. Either ^{t}RCH or ^{t}RRH must be satisfied for a READ cycle.
20. ^{t}OFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
21. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY-WRITE cycles.
22. $\overline{OE}$ is tied permanently LOW, LATE-WRITE or READ-MODIFY-WRITE operations are not possible.
23. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW and $\overline{OE}$ = HIGH.
24. ^{t}WTS and ^{t}WTH are setup and hold specifications for the $\overline{WE}$ pin being held LOW to enable the JEDEC test mode (with CBR timing constraints). These two parameters are the inverts of ^{t}WRP and ^{t}WRH in the CBR refresh cycle.

NEW DRAM MODULE

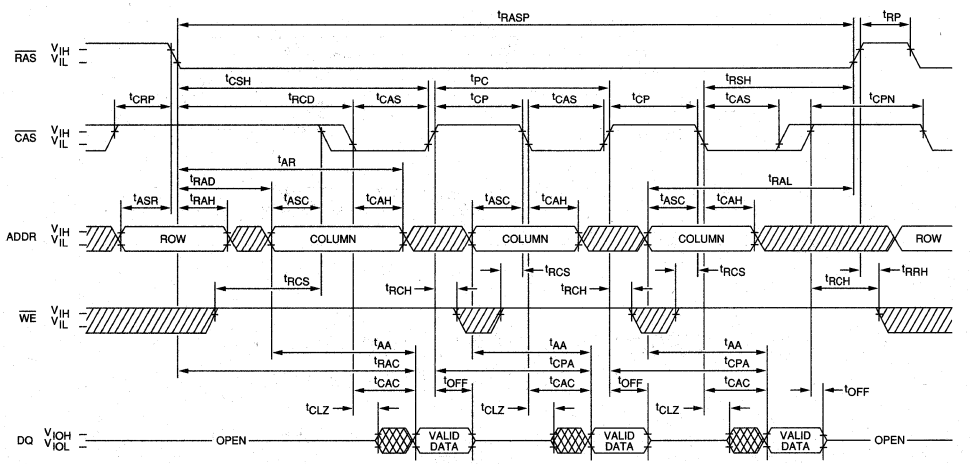
READ CYCLE



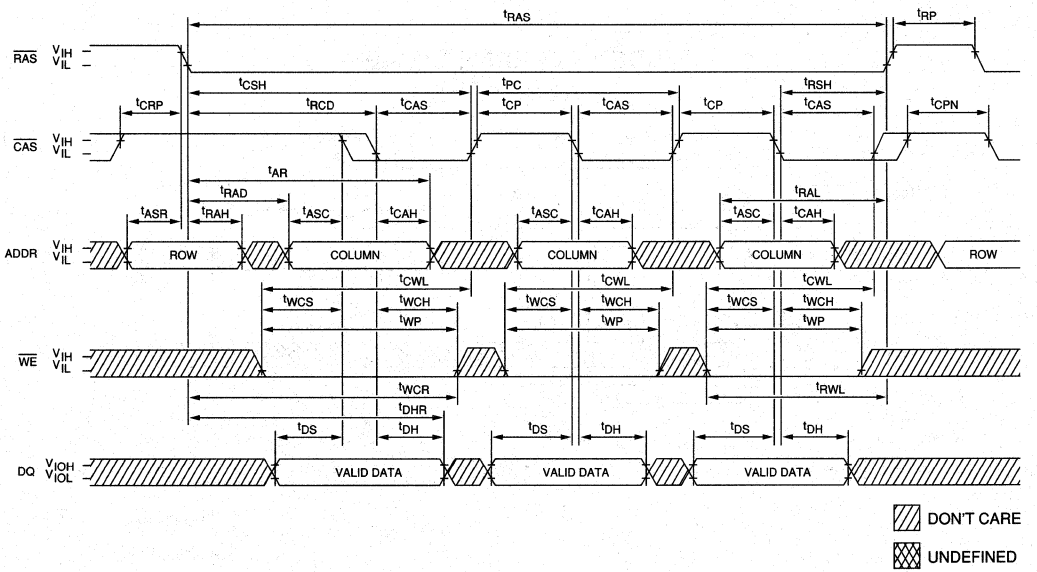
EARLY-WRITE CYCLE



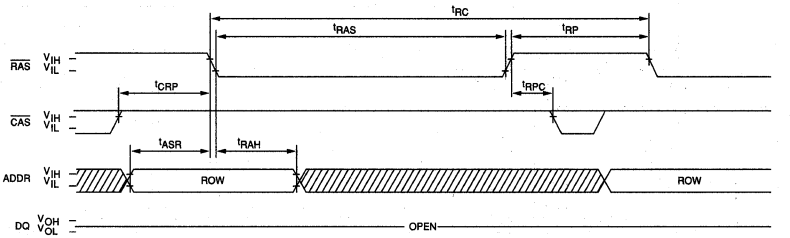
FAST-PAGE-MODE READ CYCLE



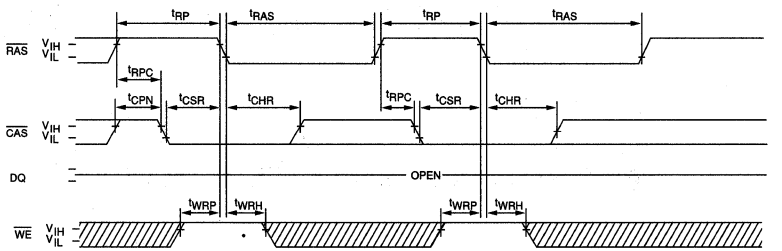
FAST-PAGE-MODE EARLY-WRITE CYCLE



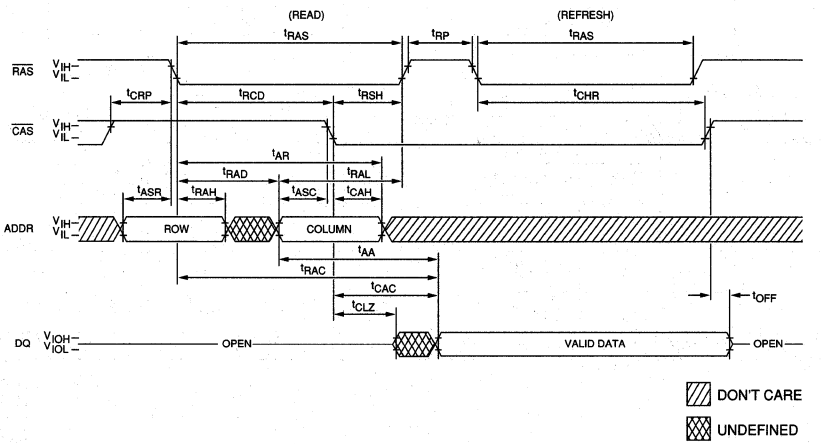
RAS-ONLY REFRESH CYCLE
(ADDR = A0-A10; WE = DON'T CARE)



CAS-BEFORE-RAS REFRESH CYCLE
(A0-A10 = DON'T CARE)



HIDDEN REFRESH CYCLE [23]
(WE = HIGH)



DRAM MODULE

256K x 36 DRAM

FAST PAGE MODE

FEATURES

- Common $\overline{RAS}$ control pinout in a 72-pin single-in-line package
- High-performance, CMOS silicon-gate process
- Single 5V ±10% power supply
- All device pins are fully TTL compatible
- Low power, 27mW standby; 1,575mW active, typical
- Refresh modes: $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$ (CBR) and HIDDEN
- 512-cycle refresh distributed across 8ms
- FAST PAGE MODE access cycle

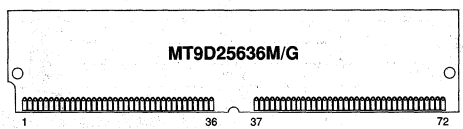
OPTIONS MARKING

- Timing
  - 60ns access - 6
  - 70ns access - 7
  - 80ns access - 8
- Packages
  - Leadless 72-pin SIMM M
  - Leadless 72-pin SIMM (Gold) G
- Part Number Example: MT9D25636G-6

PIN ASSIGNMENT (Top View)

72-Pin SIMM

(T-11)



PIN #	SYMBOL	PIN #	SYMBOL	PIN #	SYMBOL	PIN #	SYMBOL
1	Vss	19	NC	37	DQ18	55	DQ13
2	DQ1	20	DQ5	38	DQ36	56	DQ31
3	DQ19	21	DQ23	39	Vss	57	DQ14
4	DQ2	22	DQ6	40	$\overline{CAS0}$	58	DQ32
5	DQ20	23	DQ24	41	$\overline{CAS2}$	59	Vcc
6	DQ3	24	DQ7	42	$\overline{CAS3}$	60	DQ33
7	DQ21	25	DQ25	43	$\overline{CAS1}$	61	DQ15
8	DQ4	26	DQ8	44	$\overline{RAS0}$	62	DQ34
9	DQ22	27	DQ26	45	NC	63	DQ16
10	Vcc	28	A7	46	NC	64	DQ35
11	NC	29	NC	47	$\overline{WE}$	65	DQ17
12	A0	30	Vcc	48	NC	66	NC
13	A1	31	A8	49	DQ10	67	PRD1
14	A2	32	NC	50	DQ28	68	PRD2
15	A3	33	NC	51	DQ11	69	PRD3
16	A4	34	$\overline{RAS0}$	52	DQ29	70	PRD4
17	A5	35	DQ27	53	DQ12	71	NC
18	A6	36	DQ9	54	DQ30	72	Vss

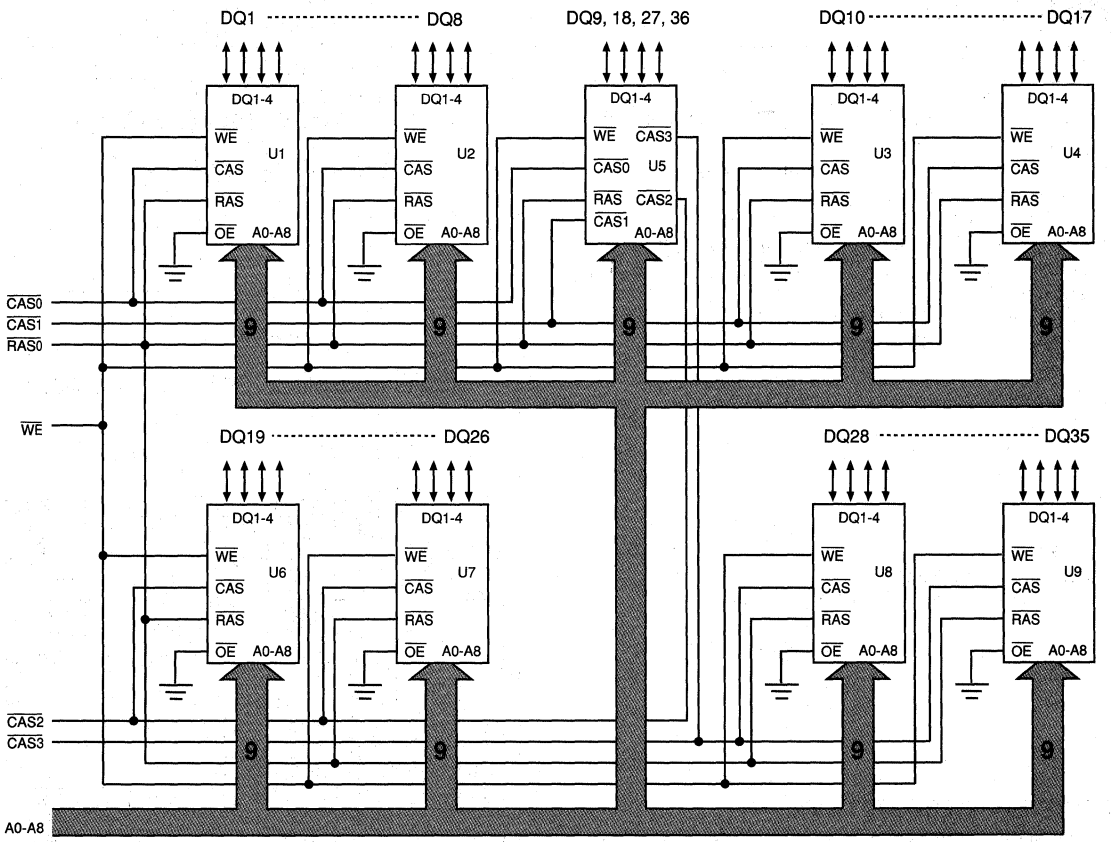
GENERAL DESCRIPTION

The MT9D25636 is a randomly accessed solid-state memory containing 262,144 words organized in a x36 configuration. During READ or WRITE cycles, each bit is uniquely addressed through the 18 address bits which are entered 9 bits (A0-A8) at a time. $\overline{RAS}$ is used to latch the first 9 bits and $\overline{CAS}$ the latter 9 bits. READ or WRITE cycles are selected with the $\overline{WE}$ input. A logic HIGH on $\overline{WE}$ dictates READ mode while a logic LOW on $\overline{WE}$ dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. If $\overline{WE}$ goes LOW prior to $\overline{CAS}$ going LOW, the output pin(s) remain open (High-Z) until the next $\overline{CAS}$ cycle.

FAST PAGE MODE operations allow faster data operations (READ or WRITE) within a row-address (A0-A8) defined page boundary. The FAST PAGE MODE cycle is always initiated with a row address strobed-in by $\overline{RAS}$ followed by a column address strobed-in by $\overline{CAS}$. $\overline{CAS}$ may be toggled-in by holding $\overline{RAS}$ LOW and strobing-in different column addresses, thus executing faster memory cycles. Returning $\overline{RAS}$ HIGH terminates the FAST PAGE MODE operation.

Returning $\overline{RAS}$ and $\overline{CAS}$ HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the $\overline{RAS}$ HIGH time. Memory cell data is retained in its correct state by maintaining power and executing any $\overline{RAS}$ cycle (READ, WRITE, $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$ or HIDDEN REFRESH) so that all 512 combinations of $\overline{RAS}$ addresses (A0-A8) are executed at least every 8ms, regardless of sequence.

FUNCTIONAL BLOCK DIAGRAM



U1-U4, U6-U9 = MT4C4256DJ
U5 = MT4C4259DJ

NOTE: Due to the use of a Quad $\overline{CAS}$ parity DRAM, $\overline{RAS0}$ is common to all devices.

TRUTH TABLE

FUNCTION		RAS	CAS	WE	ADDRESSES		DATA IN/OUT
					^tR	^tC	DQ1-DQ36
Standby		H	H→X	X	X	X	High-Z
READ		L	L	H	ROW	COL	Data Out
EARLY-WRITE		L	L	L	ROW	COL	Data In
FAST-PAGE-MODE READ	1st Cycle	L	H→L→H	H	ROW	COL	Data Out
	2nd Cycle	L	H→L→H	H	n/a	COL	Data Out
FAST-PAGE-MODE WRITE	1st Cycle	L	H→L→H	L	ROW	COL	Data In
	2nd Cycle	L	H→L→H	L	n/a	COL	Data In
RAS-ONLY REFRESH		L	H	X	ROW	n/a	High-Z
HIDDEN REFRESH	READ	L→H→L	L	H	ROW	COL	Data Out
	WRITE	L→H→L	L	L	ROW	COL	Data In
CAS-BEFORE-RAS REFRESH		H→L	L	X	X	X	High-Z

PRESENCE DETECT

SYMBOL	-6	-7	-8
PRD1	Vss	Vss	Vss
PRD2	NC	NC	NC
PRD3	NC	Vss	NC
PRD4	NC	NC	Vss

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} ..... -1V to +7V
Operating Temperature, T_A (Ambient) ..... 0°C to +70°C
Storage Temperature (Plastic) ..... -55°C to +125°C
Power Dissipation 9W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 2, 3, 4, 6, 23) (0°C ≤ T_A ≤ 70°C; V_{CC} = 5V ±10%)

PARAMETER/CONDITION		SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage		V_{CC}	4.5	5.5	V	1
Input High (Logic 1) Voltage, All Inputs		V_{IH}	2.4	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, All Inputs		V_{IL}	-1.0	0.8	V	1
INPUT LEAKAGE CURRENT	$\overline{CAS0}$-$\overline{CAS3}$	I_{I1}	-6	6	µA	
Any Input 0V ≤ V_{IN} ≤ V_{CC}	A0-A8, $\overline{WE}$	I_{I2}	-18	18	µA	
(All other pins not under test = 0V) For each package input	$\overline{RAS0}$	I_{I3}	-18	18	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled, 0V ≤ V_{OUT} ≤ V_{CC}) For each package input	DQ1-DQ36	I_{OZ}	-10	10	µA	
OUTPUT LEVELS		V_{OH}	2.4		V	
Output High Voltage (I_{OUT} = -5mA)						
Output Low Voltage (I_{OUT} = 5mA)		V_{OL}		0.4	V	

		MAX				
PARAMETER/CONDITION	SYMBOL	-6	-7	-8	UNITS	NOTES
STANDBY CURRENT: (TTL) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC1}	18	18	18	mA	
STANDBY CURRENT: (CMOS) ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} -0.2V)	I_{CC2}	9	9	9	mA	
OPERATING CURRENT: Random READ/WRITE Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC (MIN))	I_{CC3}	810	720	630	mA	2, 23
OPERATING CURRENT: FAST PAGE MODE Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: ^tPC = ^tPC (MIN))	I_{CC4}	630	540	450	mA	2, 23
REFRESH CURRENT: $\overline{RAS}$-ONLY Average power supply current ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}: ^tRC = ^tRC (MIN))	I_{CC5}	810	720	630	mA	2
REFRESH CURRENT: $\overline{CAS}$-BEFORE-$\overline{RAS}$ Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC (MIN))	I_{CC6}	810	720	630	mA	2, 19

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A8	C_{I1}		58	pF	17
Input Capacitance: $\overline{WE}$	C_{I2}		76	pF	17
Input Capacitance: $\overline{RAS0}$	C_{I3}		76	pF	17
Input Capacitance: $\overline{CAS0}$, $\overline{CAS1}$, $\overline{CAS2}$, $\overline{CAS3}$	C_{I4}		25	pF	17
Input/Output Capacitance: DQ1-DQ36	C_{IO}		10	pF	17

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 3, 4, 5, 6, 7, 10, 11, 16, 21) (0°C ≤ T_A ≤ 70°C; Vcc = 5V ±10%)

AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	^tRC	110		130		150		ns	
READ-WRITE cycle time	^tRWC	n/a		n/a		n/a		ns	21
FAST-PAGE-MODE READ or WRITE cycle time	^tPC	40		40		45		ns	
FAST-PAGE-MODE READ-WRITE cycle time	^tPRWC	n/a		n/a		n/a		ns	21
Access time from $\overline{RAS}$	^tRAC		60		70		80	ns	8
Access time from $\overline{CAS}$	^tCAC		20		20		20	ns	9
Output Enable	^tOE		20		20		20	ns	
Access time from column address	^tAA		30		35		40	ns	
Access time from $\overline{CAS}$ precharge	^tCPA		35		40		45	ns	
$\overline{RAS}$ pulse width	^tRAS	60	100,000	70	100,000	80	100,000	ns	
$\overline{RAS}$ pulse width (FAST PAGE MODE)	^tRASP	60	100,000	70	100,000	80	100,000	ns	
$\overline{RAS}$ hold time	^tRSH	20		20		20		ns	
$\overline{RAS}$ precharge time	^tRP	40		50		60		ns	
$\overline{CAS}$ pulse width	^tCAS	20	100,000	20	100,000	20	100,000	ns	
$\overline{CAS}$ hold time	^tCSH	60		70		80		ns	
$\overline{CAS}$ precharge time	^tCPN	10		10		10		ns	18,22
$\overline{CAS}$ precharge time (FAST PAGE MODE)	^tCP	10		10		10		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	^tRCD	20	40	20	50	20	60	ns	13
$\overline{CAS}$ to $\overline{RAS}$ precharge time	^tCRP	5		5		5		ns	
Row address setup time	^tASR	0		0		0		ns	
Row address hold time	^tRAH	10		10		10		ns	
$\overline{RAS}$ to column address delay time	^tRAD	15	30	15	35	15	40	ns	24
Column address setup time	^tASC	0		0		0		ns	
Column address hold time	^tCAH	15		15		15		ns	
Column address hold time (referenced to $\overline{RAS}$)	^tAR	45		55		60		ns	
Column address to $\overline{RAS}$ lead time	^tRAL	30		35		40		ns	
Read command setup time	^tRCS	0		0		0		ns	
Read command hold time (referenced to $\overline{CAS}$)	^tRCH	0		0		0		ns	14
Read command hold time (referenced to $\overline{RAS}$)	^tRRH	0		0		0		ns	14

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

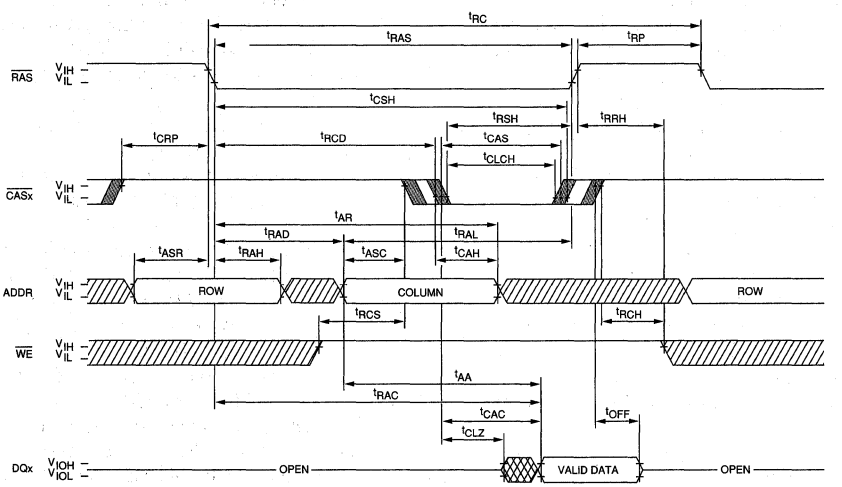
(Notes: 3, 4, 5, 6, 7, 10, 11, 16, 21) ($0°C \le T_A \le 70°C$; V_{CC} = 5V ±10%)

AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
$\overline{CAS}$ to output in Low-Z	^tCLZ	0		0		0		ns	
Output buffer turn-off delay	^tOFF	0	20	0	20	0	20	ns	12
$\overline{WE}$ command setup time	^tWCS	0		0		0		ns	
Write command hold time	^tWCH	10		15		15		ns	
Write command hold time (referenced to $\overline{RAS}$)	^tWCR	45		55		60		ns	
Write command pulse width	^tWP	10		15		15		ns	
Write command to $\overline{RAS}$ lead time	^tRWL	20		20		20		ns	
Write command to $\overline{CAS}$ lead time	^tCWL	20		20		20		ns	
Data-in setup time	^tDS	0		0		0		ns	15
Data-in hold time	^tDH	15		15		15		ns	15
Data-in hold time (referenced to $\overline{RAS}$)	^tDHR	45		55		60		ns	
Transition time (rise or fall)	^tT	3	50	3	50	3	50	ns	5, 16
Refresh period (512 cycles)	^tREF		8		8		8	ms	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	^tRPC	0		0		0		ns	
$\overline{CAS}$ setup time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tCSR	10		10		10		ns	19
$\overline{CAS}$ hold time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tCHR	10		15		15		ns	19
Last $\overline{CAS}$ going LOW to first $\overline{CAS}$ to return HIGH	^tCLCH	10		10		10		ns	22

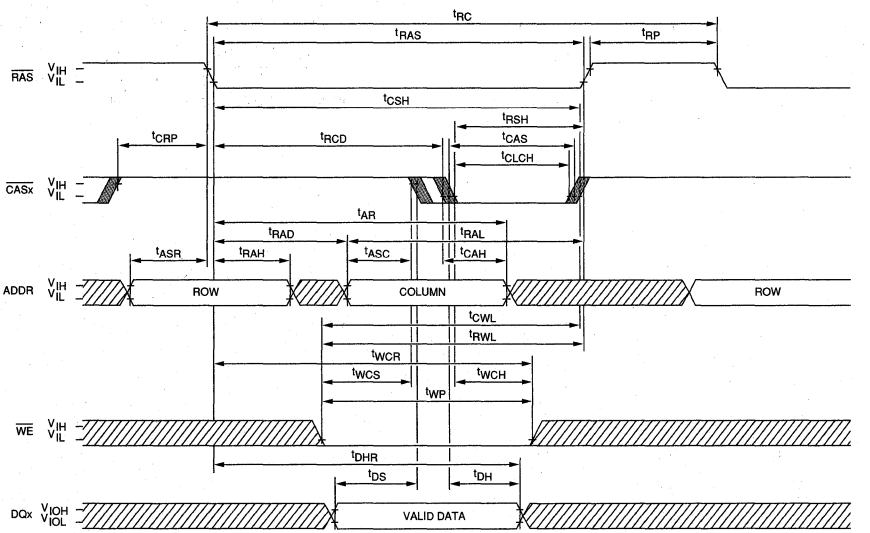
NOTES

1. All voltages referenced to V_{SS}.
2. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
3. An initial pause of 100µs is required after power-up followed by any eight $\overline{RAS}$ cycles before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-up should be repeated any time the ^{t}REF refresh requirement is exceeded.
4. AC characteristics assume ^{t}T = 5ns.
5. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \le T_A \le 70°C$) is assured.
7. Measured with a load equivalent to two TTL gates and 100pF.
8. Assumes that $^{t}RCD < {}^{t}RCD$ (MAX). If ^{t}RCD is greater than the maximum recommended value shown in this table, ^{t}RAC will increase by the amount that ^{t}RCD exceeds the value shown.
9. Assumes that $^{t}RCD \ge {}^{t}RCD$ (MAX).
10. If $\overline{CAS}$ = V_{IH}, data output is High-Z.
11. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
12. ^{t}OFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
13. Operation within the ^{t}RCD (MAX) limit ensures that ^{t}RAC (MAX) can be met. ^{t}RCD (MAX) is specified as a reference point only; if ^{t}RCD is greater than the specified ^{t}RCD (MAX) limit, then access time is controlled exclusively by ^{t}CAC.
14. Either ^{t}RCH or ^{t}RRH must be satisfied for a READ cycle.
15. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY-WRITE cycles.
16. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
17. This parameter is sampled. Capacitance is measured using MIL-STD-883C, Method 3012.1 (1 MHz AC, Vcc = 5V, DC bias = 2.4V @ 15mV RMS).
18. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, data out (Q) will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer, $\overline{CAS}$ must be pulsed HIGH for ^{t}CP.
19. On-chip refresh and address counters are enabled.
20. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW.
21. LATE-WRITE, READ-WRITE or READ-MODIFY-WRITE cycles are not available due to $\overline{OE}$ being grounded on U1-U9.
22. Last falling $\overline{CAS}$x edge to first rising $\overline{CAS}$x edge.
23. I_{CC} is dependent on cycle rates.
24. Operation within the ^{t}RAD (MAX) limit ensures that ^{t}RCD (MAX) can be met. ^{t}RAD (MAX) is specified as a reference point only; if ^{t}RAD is greater than the specified ^{t}RAD (MAX) limit, then access time is controlled exclusively by ^{t}AA.

READ CYCLE



EARLY-WRITE CYCLE

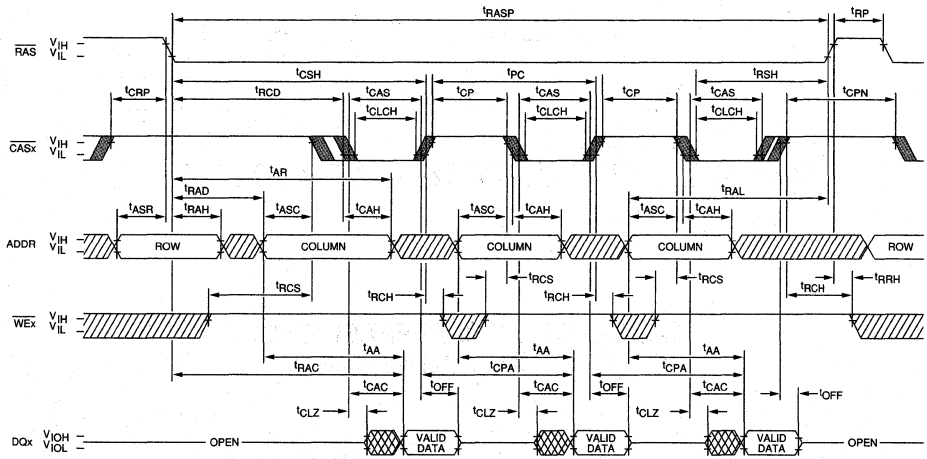


DON'T CARE

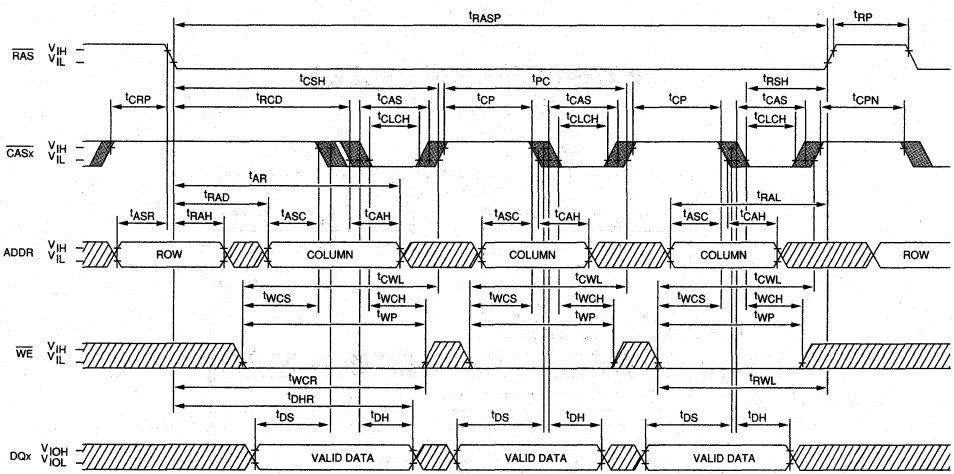
UNDEFINED

FIRST TO LAST $\overline{CAS}$ TO TRANSITION
(minimum of 1, maximum of 4)

FAST-PAGE-MODE READ CYCLE



FAST-PAGE-MODE EARLY-WRITE CYCLE

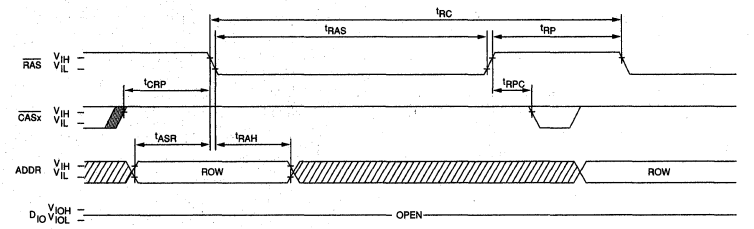


DON'T CARE

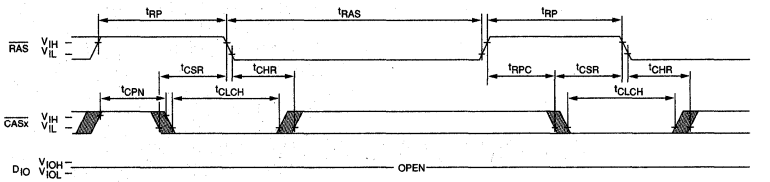
UNDEFINED

FIRST TO LAST $\overline{CAS}$ TO TRANSITION
(minimum of 1, maximum of 4)

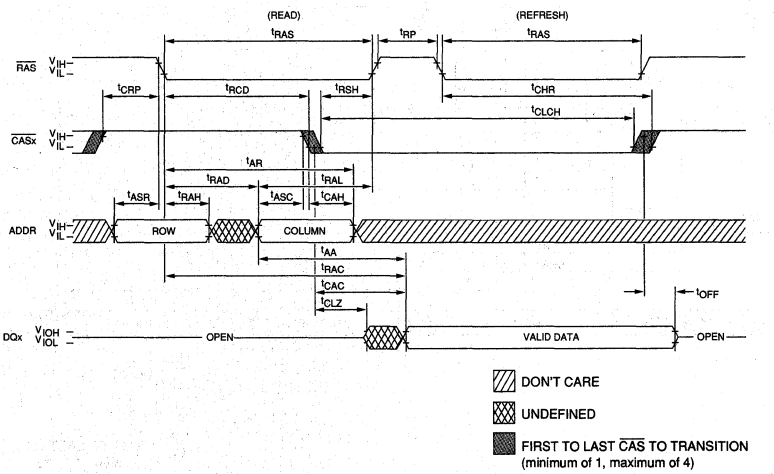
RAS-ONLY REFRESH CYCLE
(ADDR = A0-A8; WE = DON'T CARE)



CAS-BEFORE-RAS REFRESH CYCLE
(A0-A8, WE = DON'T CARE)



HIDDEN REFRESH CYCLE [20]
(WE = HIGH)



DRAM MODULE

256K x 36, 512K x 18

FAST PAGE MODE

FEATURES

- Industry standard pinout in a 72-pin single-in-line package
- High-performance, CMOS silicon-gate process.
- Single 5V ±10% power supply
- All device pins are fully TTL compatible
- Low power, 30mW standby; 1,750mW active, typical
- Refresh modes: $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$ (CBR) and HIDDEN
- 512-cycle refresh distributed across 8ms
- FAST PAGE MODE access cycle
- Multiple $\overline{RAS}$ lines allow x18 or x36 width

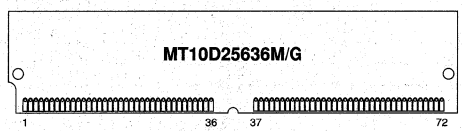
OPTIONS MARKING

- Timing
  - 60ns access - 6
  - 70ns access - 7
  - 80ns access - 8
- Packages
  - Leadless 72-pin SIMM M
  - Leadless 72-pin SIMM (Gold) G
- Part Number Example: MT10D25636G-6

PIN ASSIGNMENT (Top View)

72-Pin SIMM

(T-13)



PIN #	SYMBOL	PIN #	SYMBOL	PIN #	SYMBOL	PIN #	SYMBOL
1	Vss	19	NC	37	DQ18	55	DQ13
2	DQ1	20	DQ5	38	DQ36	56	DQ31
3	DQ19	21	DQ23	39	Vss	57	DQ14
4	DQ2	22	DQ6	40	$\overline{CAS0}$	58	DQ32
5	DQ20	23	DQ24	41	$\overline{CAS2}$	59	Vcc
6	DQ3	24	DQ7	42	$\overline{CAS3}$	60	DQ33
7	DQ21	25	DQ25	43	$\overline{CAS1}$	61	DQ15
8	DQ4	26	DQ8	44	$\overline{RAS0}$	62	DQ34
9	DQ22	27	DQ26	45	NC	63	DQ16
10	Vcc	28	A7	46	NC	64	DQ35
11	NC	29	NC	47	$\overline{WE}$	65	DQ17
12	A0	30	Vcc	48	NC	66	NC
13	A1	31	A8	49	DQ10	67	PRD1
14	A2	32	NC	50	DQ28	68	PRD2
15	A3	33	NC	51	DQ11	69	PRD3
16	A4	34	$\overline{RAS2}$	52	DQ29	70	PRD4
17	A5	35	DQ27	53	DQ12	71	NC
18	A6	36	DQ9	54	DQ30	72	Vss

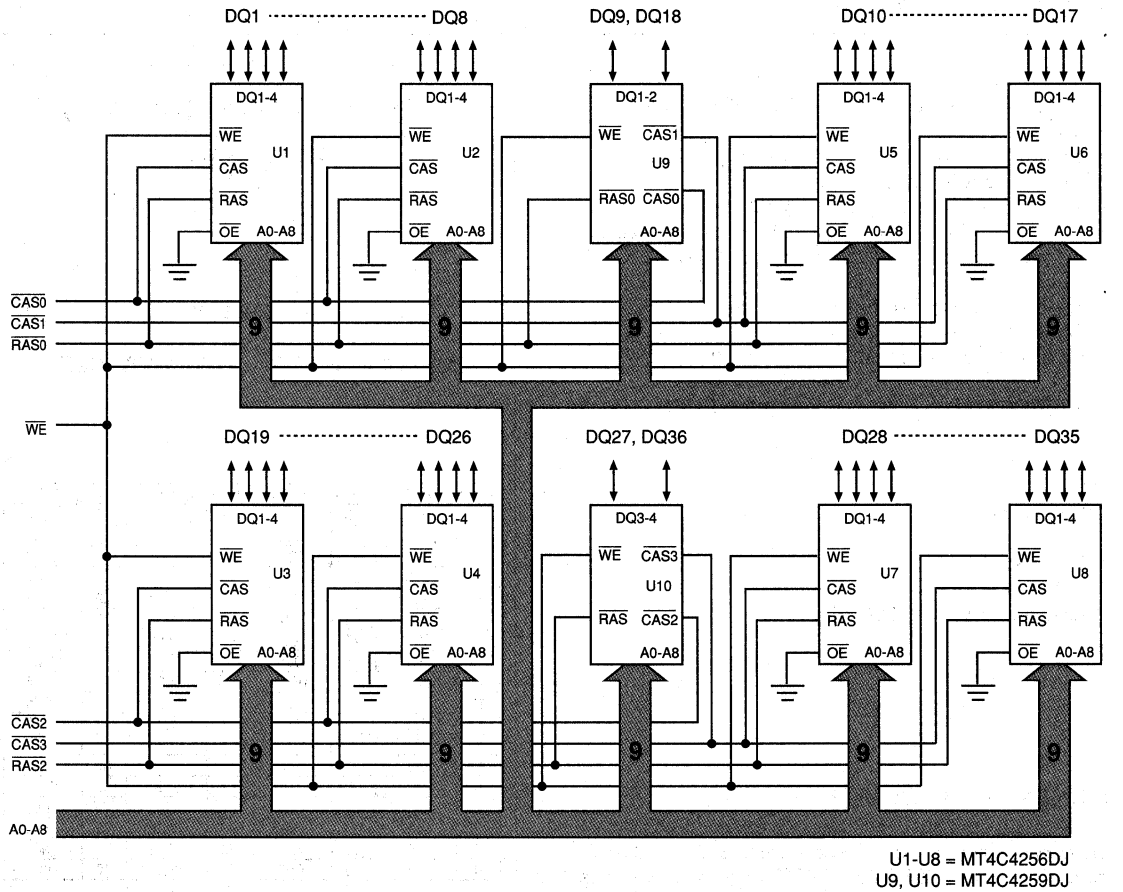
GENERAL DESCRIPTION

The MT10D25636 is a randomly accessed solid-state memory containing 262,144 words organized in a x36 configuration. During READ or WRITE cycles, each bit is uniquely addressed through the 18 address bits, which are entered 9 bits (A0-A8) at a time. $\overline{RAS}$ is used to latch the first 9 bits and $\overline{CAS}$ the latter 9 bits. READ or WRITE cycles are selected with the $\overline{WE}$ input. A logic HIGH on $\overline{WE}$ dictates READ mode while a logic LOW on $\overline{WE}$ dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. If $\overline{WE}$ goes LOW prior to $\overline{CAS}$ going LOW, the output pin(s) remain open (High-Z) until the next $\overline{CAS}$ cycle.

FAST PAGE MODE operations allow faster data operations (READ or WRITE) within a row-address (A0-A8) defined page boundary. The FAST PAGE MODE cycle is always initiated with a row address strobed-in by $\overline{RAS}$ followed by a column address strobed-in by $\overline{CAS}$. $\overline{CAS}$ may be toggled-in by holding $\overline{RAS}$ LOW and strobing-in different column addresses, thus executing faster memory cycles. Returning $\overline{RAS}$ HIGH terminates the FAST PAGE MODE operation.

Returning $\overline{RAS}$ and $\overline{CAS}$ HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the $\overline{RAS}$ HIGH time. Memory cell data is retained in its correct state by maintaining power and executing any $\overline{RAS}$ cycle (READ, WRITE, $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$ or HIDDEN REFRESH) so that all 512 combinations of $\overline{RAS}$ addresses (A0-A8) are executed at least every 8ms, regardless of sequence.

FUNCTIONAL BLOCK DIAGRAM



U1-U8 = MT4C4256DJ
U9, U10 = MT4C4259DJ

TRUTH TABLE

FUNCTION		RAS	CAS	WE	ADDRESSES		DATA IN/OUT
					^tR	^tC	DQ1-DQ36
Standby		H	H→X	X	X	X	High-Z
READ		L	L	H	ROW	COL	Data Out
EARLY-WRITE		L	L	L	ROW	COL	Data In
FAST-PAGE-MODE	1st Cycle	L	H→L→H	H	ROW	COL	Data Out
READ	2nd Cycle	L	H→L→H	H	n/a	COL	Data Out
FAST-PAGE-MODE	1st Cycle	L	H→L→H	L	ROW	COL	Data In
WRITE	2nd Cycle	L	H→L→H	L	n/a	COL	Data In
RAS-ONLY REFRESH		L	H	X	ROW	n/a	High-Z
HIDDEN	READ	L→H→L	L	H	ROW	COL	Data Out
REFRESH	WRITE	L→H→L	L	L	ROW	COL	Data In
CAS-BEFORE-RAS REFRESH		H→L	L	X	X	X	High-Z

PRESENCE DETECT

SYMBOL	-6	-7	-8
PRD1	Vss	Vss	Vss
PRD2	NC	NC	NC
PRD3	NC	Vss	NC
PRD4	NC	NC	Vss

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} ..... -1V to +7V
Operating Temperature, T_A (Ambient) ..... 0°C to +70°C
Storage Temperature (Plastic) ..... -55°C to +125°C
Power Dissipation 10W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 2, 3, 6, 23) (0°C ≤ T_A ≤ 70°C; V_{CC} = 5V ±10%)

PARAMETER/CONDITION		SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage		V_{CC}	4.5	5.5	V	1
Input High (Logic 1) Voltage, All Inputs		V_{IH}	2.4	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, All Inputs		V_{IL}	-1.0	0.8	V	1
INPUT LEAKAGE CURRENT	$\overline{CAS0}$-$\overline{CAS3}$	I_{I1}	-6	6	µA	
Any Input 0V ≤ V_{IN} ≤ V_{CC}	A0-A8, $\overline{WE}$	I_{I2}	-20	20	µA	
(All other pins not under test = 0V) for each package input	$\overline{RAS0}$, $\overline{RAS2}$	I_{I3}	-10	10	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled, 0V ≤ V_{OUT} ≤ V_{CC}) for each package input	DQ1-DQ36	I_{OZ}	-10	10	µA	
OUTPUT LEVELS		V_{OH}	2.4		V	
Output High Voltage (I_{OUT} = -5mA)						
Output Low Voltage (I_{OUT} = 5mA)		V_{OL}		0.4	V	

		MAX				
PARAMETER/CONDITION	SYMBOL	-6	-7	-8	UNITS	NOTES
STANDBY CURRENT: (TTL) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC1}	20	20	20	mA	
STANDBY CURRENT: (CMOS) ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} -0.2V)	I_{CC2}	10	10	10	mA	
OPERATING CURRENT: Random READ/WRITE Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC (MIN))	I_{CC3}	900	800	700	mA	2, 23
OPERATING CURRENT: FAST PAGE MODE Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: ^tPC = ^tPC (MIN))	I_{CC4}	700	600	500	mA	2, 23
REFRESH CURRENT: $\overline{RAS}$-ONLY Average power supply current ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}: ^tRC = ^tRC (MIN))	I_{CC5}	900	800	700	mA	2
REFRESH CURRENT: $\overline{CAS}$-BEFORE-$\overline{RAS}$ Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC (MIN))	I_{CC6}	900	800	700	mA	2, 19

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A8	C_{I1}		64	pF	17
Input Capacitance: $\overline{WE}$	C_{I2}		84	pF	17
Input Capacitance: $\overline{RAS0}$, $\overline{RAS2}$	C_{I3}		42	pF	17
Input Capacitance: $\overline{CAS0}$, $\overline{CAS1}$, $\overline{CAS2}$, $\overline{CAS3}$	C_{I4}		25	pF	17
Input/Output Capacitance: DQ1-DQ36	C_{IO}		10	pF	17

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 3, 4, 5, 6, 7, 10, 11, 16, 21) ($0°C \le T_A \le 70°C$; V_{CC} = 5V ±10%)

AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	^tRC	110		130		150		ns	
READ-WRITE cycle time	^tRWC	n/a		n/a		n/a		ns	21
FAST-PAGE-MODE READ or WRITE cycle time	^tPC	40		40		45		ns	
FAST-PAGE-MODE READ-WRITE cycle time	^tPRWC	n/a		n/a		n/a		ns	21
Access time from $\overline{RAS}$	^tRAC		60		70		80	ns	8
Access time from $\overline{CAS}$	^tCAC		20		20		20	ns	9
Output Enable	^tOE		20		20		20	ns	
Access time from column address	^tAA		30		35		40	ns	
Access time from $\overline{CAS}$ precharge	^tCPA		35		40		45	ns	
$\overline{RAS}$ pulse width	^tRAS	60	100,000	70	100,000	80	100,000	ns	
$\overline{RAS}$ pulse width (FAST PAGE MODE)	^tRASP	60	100,000	70	100,000	80	100,000	ns	
$\overline{RAS}$ hold time	^tRSH	20		20		20		ns	
$\overline{RAS}$ precharge time	^tRP	40		50		60		ns	
$\overline{CAS}$ pulse width	^tCAS	20	100,000	20	100,000	20	100,000	ns	
$\overline{CAS}$ hold time	^tCSH	60		70		80		ns	
$\overline{CAS}$ precharge time	^tCPN	10		10		10		ns	18, 23
$\overline{CAS}$ precharge time (FAST PAGE MODE)	^tCP	10		10		10		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	^tRCD	20	40	20	50	20	60	ns	13
$\overline{CAS}$ to $\overline{RAS}$ precharge time	^tCRP	5		5		5		ns	
Row address setup time	^tASR	0		0		0		ns	
Row address hold time	^tRAH	10		10		10		ns	
$\overline{RAS}$ to column address delay time	^tRAD	15	30	15	35	15	40	ns	25
Column address setup time	^tASC	0		0		0		ns	
Column address hold time	^tCAH	15		15		15		ns	
Column address hold time (referenced to $\overline{RAS}$)	^tAR	45		55		60		ns	
Column address to $\overline{RAS}$ lead time	^tRAL	30		35		40		ns	
Read command setup time	^tRCS	0		0		0		ns	
Read command hold time (referenced to $\overline{CAS}$)	^tRCH	0		0		0		ns	14
Read command hold time (referenced to $\overline{RAS}$)	^tRRH	0		0		0		ns	14

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

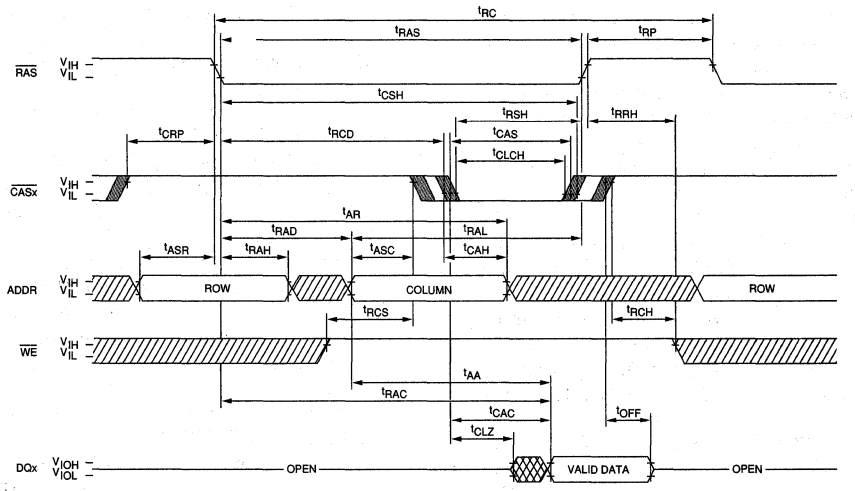
(Notes: 3, 4, 5, 6, 7, 10, 11, 16, 21) ($0°C \le T_A \le 70°C$; Vcc = 5V ±10%)

AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
$\overline{CAS}$ to output in Low-Z	tCLZ	0		0		0		ns	
Output buffer turn-off delay	tOFF	0	20	0	20	0	20	ns	12
$\overline{WE}$ command setup time	tWCS	0		0		0		ns	
Write command hold time	tWCH	10		15		15		ns	
Write command hold time (referenced to $\overline{RAS}$)	tWCR	45		55		60		ns	
Write command pulse width	tWP	10		15		15		ns	
Write command to $\overline{RAS}$ lead time	tRWL	20		20		20		ns	
Write command to $\overline{CAS}$ lead time	tCWL	20		20		20		ns	
Data-in setup time	tDS	0		0		0		ns	15
Data-in hold time	tDH	15		15		15		ns	15
Data-in hold time (referenced to $\overline{RAS}$)	tDHR	45		55		60		ns	
Transition time (rise or fall)	tT	3	50	3	50	3	50	ns	5, 16
Refresh period (512 cycles)	tREF		8		8		8	ms	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	tRPC	0		0		0		ns	
$\overline{CAS}$ setup time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	tCSR	10		10		10		ns	19
$\overline{CAS}$ hold time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	tCHR	10		15		15		ns	19
Last $\overline{CAS}$ going LOW to First $\overline{CAS}$ to return HIGH	tCLCH	10		10		10		ns	

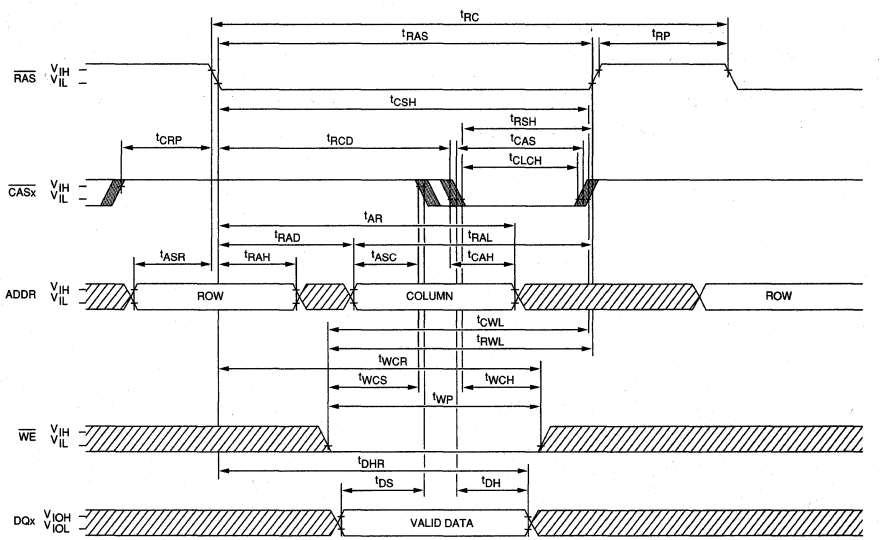
NOTES

1. All voltages referenced to V_{SS}.
2. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
3. An initial pause of 100µs is required after power-up followed by any eight $\overline{RAS}$ cycles before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-up should be repeated any time the ^{t}REF refresh requirement is exceeded.
4. AC characteristics assume ^{t}T = 5ns.
5. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \le T_A \le 70°C$) is assured.
7. Measured with a load equivalent to two TTL gates and 100pF.
8. Assumes that $^{t}RCD < ^{t}RCD$ (MAX). If ^{t}RCD is greater than the maximum recommended value shown in this table, ^{t}RAC will increase by the amount that ^{t}RCD exceeds the value shown.
9. Assumes that $^{t}RCD \ge ^{t}RCD$ (MAX).
10. If $\overline{CAS}$ = V_{IH}, data output is High-Z.
11. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
12. ^{t}OFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
13. Operation within the ^{t}RCD (MAX) limit ensures that ^{t}RAC (MAX) can be met. ^{t}RCD (MAX) is specified as a reference point only; if ^{t}RCD is greater than the specified ^{t}RCD (MAX) limit, then access time is controlled exclusively by ^{t}CAC.
14. Either ^{t}RCH or ^{t}RRH must be satisfied for a READ cycle.
15. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY-WRITE cycles.
16. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
17. This parameter is sampled. Capacitance is measured using MIL-STD-883C, Method 3012.1 (1 MHz AC, Vcc = 5V, DC bias = 2.4V @ 15mV RMS).
18. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, data-out (Q) will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer, $\overline{CAS}$ must be pulsed HIGH for ^{t}CP.
19. On-chip refresh and address counters are enabled.
20. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW.
21. LATE-WRITE, READ-WRITE or READ-MODIFY-WRITE cycles are not available due to $\overline{OE}$ being grounded on U1-U9.
22. Last falling $\overline{CASx}$ edge to first rising $\overline{CASx}$ edge.
23. I_{CC} is dependent on cycle rates.
24. Operation within the ^{t}RAD (MAX) limit ensures that ^{t}RCD (MAX) can be met. ^{t}RAD (MAX) is specified as a reference point only; if ^{t}RAD is greater than the specified ^{t}RAD (MAX) limit, then access time is controlled exclusively by ^{t}AA.

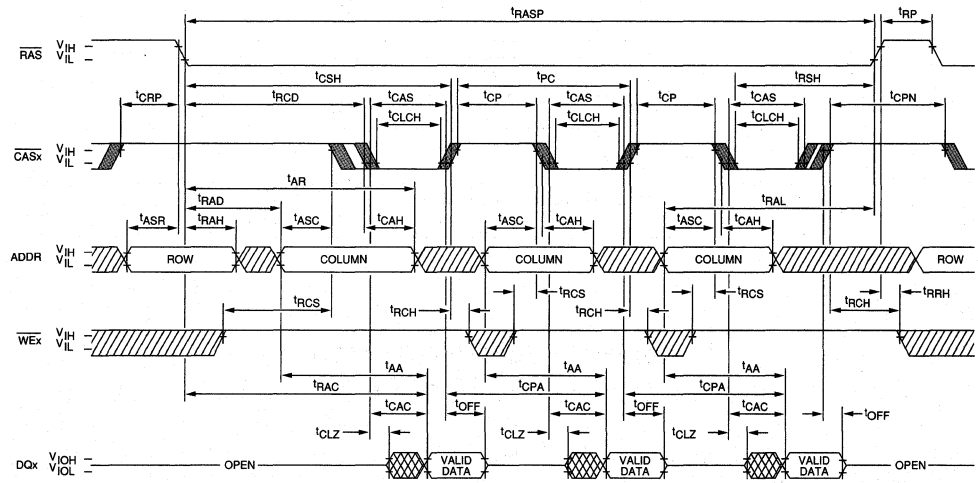
READ CYCLE



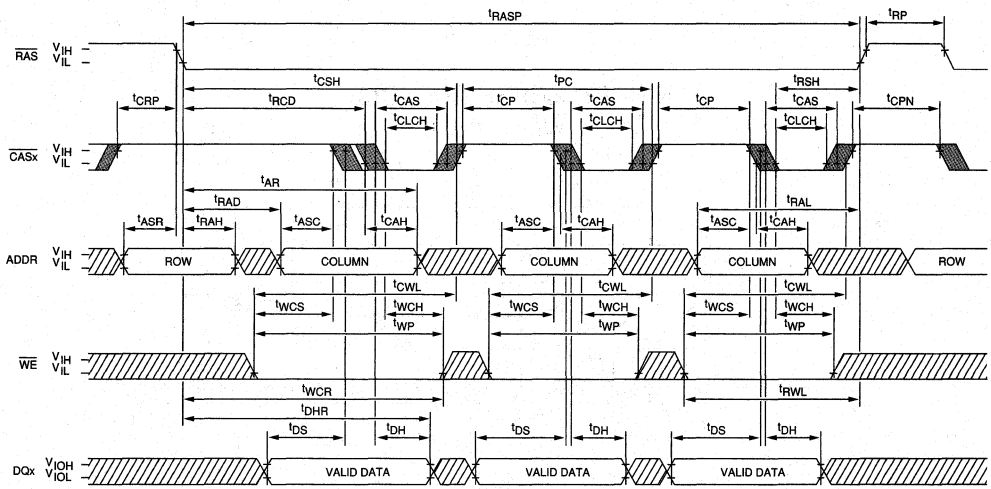
EARLY-WRITE CYCLE



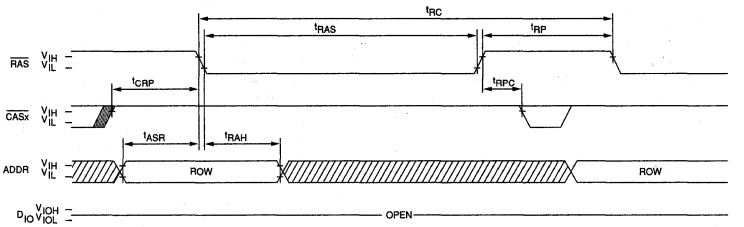
FAST-PAGE-MODE READ CYCLE



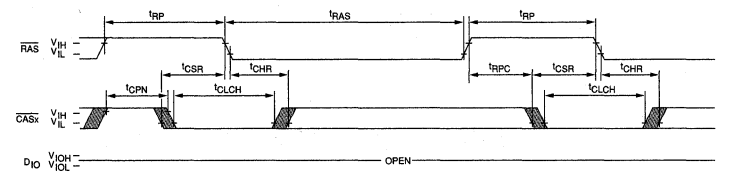
FAST-PAGE-MODE EARLY-WRITE CYCLE



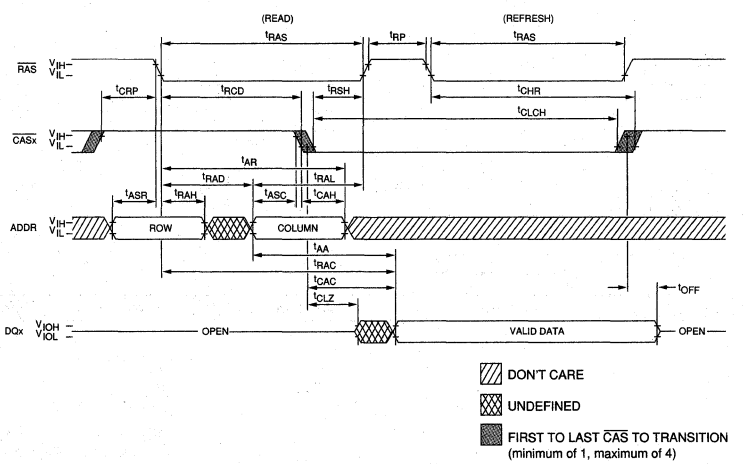
$\overline{RAS}$-ONLY REFRESH CYCLE
(ADDR = A0-A8; $\overline{WE}$ = DON'T CARE)



$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE
(A0-A8, $\overline{WE}$ = DON'T CARE)



HIDDEN REFRESH CYCLE [20]
($\overline{WE}$ = HIGH)



DRAM MODULE

1 MEG x 18 DRAM

FAST PAGE MODE

NEW DRAM MODULE

FEATURES

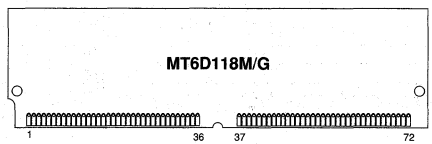
- Industry standard pinout in a 72-pin single-in-line package
- High-performance, CMOS silicon-gate process
- Single 5V ±10% power supply
- All device pins are fully TTL compatible
- Low power, 18mW standby; 1,250mW active, typical
- Refresh modes: $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$ (CBR) and HIDDEN
- 1,024-cycle refresh distributed across 16ms
- FAST PAGE MODE access cycle

OPTIONS MARKING

- Timing
  - 60ns access - 6
  - 70ns access - 7
  - 80ns access - 8
- Packages
  - Leadless 72-pin SIMM M
  - Leadless 72-pin SIMM (Gold) G
- Part Number Example: MT6D118G-6

PIN ASSIGNMENT (Top View)

72-Pin SIMM
(T-16)



PIN #	SYMBOL	PIN #	SYMBOL	PIN #	SYMBOL	PIN #	SYMBOL
1	Vss	19	NC	37	DQ18	55	DQ13
2	DQ1	20	DQ5	38	NC	56	NC
3	NC	21	NC	39	Vss	57	DQ14
4	DQ2	22	DQ6	40	$\overline{CAS0}$	58	NC
5	NC	23	NC	41	NC	59	Vcc
6	DQ3	24	DQ7	42	NC	60	NC
7	NC	25	NC	43	$\overline{CAS1}$	61	DQ15
8	DQ4	26	DQ8	44	$\overline{RAS0}$	62	NC
9	NC	27	NC	45	NC	63	DQ16
10	Vcc	28	A7	46	NC	64	NC
11	NC	29	NC	47	$\overline{WE}$	65	DQ17
12	A0	30	Vcc	48	NC	66	NC
13	A1	31	A8	49	DQ10	67	PRD1
14	A2	32	A9	50	NC	68	PRD2
15	A3	33	NC	51	DQ11	69	PRD3
16	A4	34	NC	52	NC	70	PRD4
17	A5	35	NC	53	DQ12	71	NC
18	A6	36	DQ9	54	NC	72	Vss

GENERAL DESCRIPTION

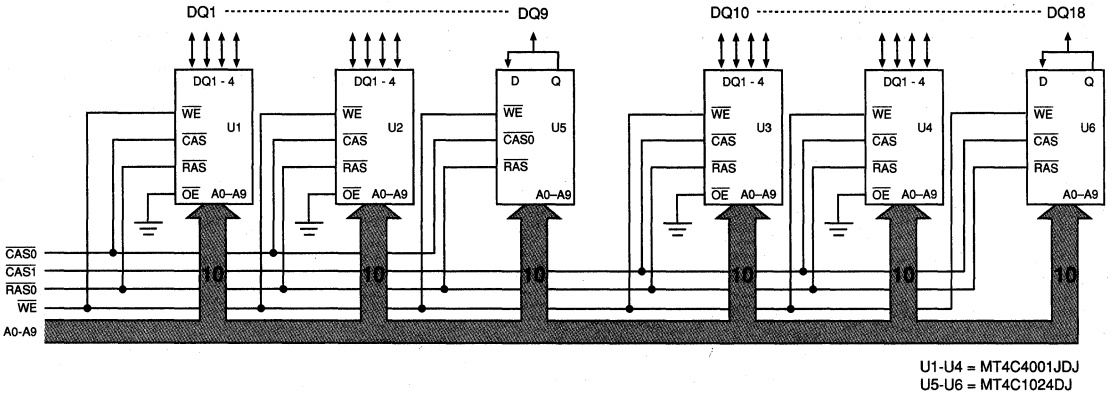
The MT6D118 is a randomly accessed solid-state memory containing 1,048,576 words organized in a x18 configuration. During READ or WRITE cycles, each bit is uniquely addressed through the 20 address bits, which are entered 10 bits (A0-A9) at a time. $\overline{RAS}$ is used to latch the first 10 bits and $\overline{CAS}$ the latter 10 bits. A READ or WRITE cycle is selected with the $\overline{WE}$ input. A logic HIGH on $\overline{WE}$ dictates READ mode while a logic LOW on $\overline{WE}$ dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. If $\overline{WE}$ goes LOW prior to $\overline{CAS}$ going LOW, the output pin(s) remain open (High-Z) until the next $\overline{CAS}$ cycle.

FAST PAGE MODE operations allow faster data operations (READ or WRITE) within a row-address (A0-A9) defined page boundary. The FAST PAGE MODE cycle is always initiated with a row address strobed-in by $\overline{RAS}$ followed by a column address strobed-in by $\overline{CAS}$. $\overline{CAS}$ may be toggled-in by holding $\overline{RAS}$ LOW and strobing-in different column addresses, thus executing faster memory cycles. Returning $\overline{RAS}$ HIGH terminates the FAST PAGE MODE operation.

Returning $\overline{RAS}$ and $\overline{CAS}$ HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the $\overline{RAS}$ HIGH time. Memory cell data is retained in its correct state by maintaining power and executing any $\overline{RAS}$ cycle (READ, WRITE, $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$ or HIDDEN REFRESH) so that all 1,024 combinations of $\overline{RAS}$ addresses (A0-A9) are executed at least every 16ms, regardless of sequence. The CBR refresh cycle will invoke the internal refresh counter for automatic $\overline{RAS}$ addressing.

NEW ■ DRAM MODULE

FUNCTIONAL BLOCK DIAGRAM



U1-U4 = MT4C4001JDJ
U5-U6 = MT4C1024DJ

TRUTH TABLE

FUNCTION		RAS	CAS	WE	ADDRESSES		DATA IN/OUT
					^tR	^tC	DQ1-DQ18
Standby		H	H→X	X	X	X	High-Z
READ		L	L	H	ROW	COL	Data Out
EARLY-WRITE		L	L	L	ROW	COL	Data In
FAST-PAGE-MODE	1st Cycle	L	H→L	H	ROW	COL	Data Out
READ	2nd Cycle	L	H→L	H	n/a	COL	Data Out
FAST-PAGE-MODE	1st Cycle	L	H→L	L	ROW	COL	Data In
WRITE	2nd Cycle	L	H→L	L	n/a	COL	Data In
RAS-ONLY REFRESH		L	H	X	ROW	n/a	High-Z
HIDDEN	READ	L→H→L	L	H	ROW	COL	Data Out
REFRESH	WRITE	L→H→L	L	L	ROW	COL	Data In
CAS-BEFORE-RAS REFRESH		H→L	L	H	X	X	High-Z

PRESENCE DETECT

SYMBOL	-7	-8	-10
PRD1	X	X	X
PRD2	X	X	X
PRD3	X	X	X
PRD4	X	X	X

X = "don't care"

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} ..... -1V to +7V
Operating Temperature, T_A (Ambient) ..... 0°C to +70°C
Storage Temperature (Plastic) ..... -55°C to +125°C
Power Dissipation 6W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

NEW DRAM MODULE

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 2, 3, 6, 25) (0°C ≤ T_A ≤ 70°C; V_{CC} = 5V ±10%)

PARAMETER/CONDITION		SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage		V_{CC}	4.5	5.5	V	1
Input High (Logic 1) Voltage, All Inputs		V_{IH}	2.4	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, All Inputs		V_{IL}	-1.0	0.8	V	1
INPUT LEAKAGE CURRENT Any Input 0V ≤ V_{IN} ≤ V_{CC}	A0-A9, $\overline{WE}$, $\overline{RAS0}$,	I_{I1}	-12	12	µA	
(All other pins not under test = 0V) for each package input	$\overline{CAS0}$, $\overline{CAS1}$	I_{I2}	-6	6	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled, 0V ≤ V_{OUT} ≤ V_{CC}) for each package input	DQ1-DQ18	I_{OZ}	-10	10	µA	
OUTPUT LEVELS Output High Voltage (I_{OUT} = -5mA)		V_{OH}	2.4		V	
Output Low Voltage (I_{OUT} = 5mA)		V_{OL}		0.4	V	

		MAX				
PARAMETER/CONDITION	SYMBOL	-6	-7	-8	UNITS	NOTES
STANDBY CURRENT: (TTL) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC1}	12	12	12	mA	
STANDBY CURRENT: (CMOS) ($\overline{RAS}$ = $\overline{CAS}$ = Other Inputs = V_{CC} -0.2V)	I_{CC2}	6	6	6	mA	
OPERATING CURRENT: Random READ/WRITE Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC (MIN))	I_{CC3}	620	560	500	mA	2, 25
OPERATING CURRENT: FAST PAGE MODE Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: ^tPC = ^tPC (MIN))	I_{CC4}	450	390	330	mA	2, 25
REFRESH CURRENT: $\overline{RAS}$-ONLY Average power supply current ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}: ^tRC = ^tRC (MIN))	I_{CC5}	620	560	500	mA	2
REFRESH CURRENT: $\overline{CAS}$-BEFORE-$\overline{RAS}$ Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC (MIN))	I_{CC6}	620	560	500	mA	2, 19

NEW ■ DRAM MODULE

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A9	C_{I1}		38	pF	17
Input Capacitance: $\overline{WE}$	C_{I2}		50	pF	17
Input Capacitance: $\overline{RAS0}$	C_{I3}		50	pF	17
Input Capacitance: $\overline{CAS0}$, $\overline{CAS1}$	C_{I4}		25	pF	17
Input/Output Capacitance: DQ1-DQ18	C_{IO}		15	pF	17

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 3, 4, 5, 6, 7, 9, 10, 11, 16, 21) ($0°C \le T_A \le 70°C$; V_{CC} = 5V ±10%)

AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	tRC	110		130		150		ns	
FAST PAGE MODE cycle time	tPC	40		40		45		ns	
Access time from $\overline{RAS}$	tRAC	60			70		80	ns	
Access time from $\overline{CAS}$	tCAC	15			20		20	ns	
Access time from column address	tAA	30			30		35	ns	
Access time from $\overline{CAS}$ precharge	tCPA	35			35		40	ns	
$\overline{RAS}$ pulse width	tRAS	60	100,000	70	100,000	80	100,000	ns	
$\overline{RAS}$ hold time	tRSH	15		20		20		ns	
$\overline{RAS}$ precharge time	tRP	40		50		60		ns	
$\overline{CAS}$ pulse width	tCAS	15	100,000	20	100,000	20	100,000	ns	
$\overline{CAS}$ hold time	tCSH	60		70		80		ns	
$\overline{CAS}$ precharge time	tCPN	10		10		10		ns	18
$\overline{CAS}$ precharge time (FAST PAGE MODE)	tCP	10		10		10		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	tRCD	20	40	20	50	20	60	ns	13
$\overline{CAS}$ to $\overline{RAS}$ setup time	tCRP	10		10		10		ns	
Row address setup time	tASR	0		0		0		ns	
$\overline{RAS}$ to column address delay time	tRAD	15	30	15	30	15	35	ns	23
Row address hold time	tRAH	10		10		10		ns	
Column address setup time	tASC	0		0		0		ns	
Column address hold time	tCAH	10		15		15		ns	
Column address to $\overline{RAS}$ lead time	tRAL	30		30		35		ns	
Column address hold time referenced to $\overline{RAS}$	tAR	50		55		60		ns	
Read command setup time	tRCS	0		0		0		ns	
Read command hold time referenced to $\overline{CAS}$	tRCH	0		0		0		ns	14
$\overline{CAS}$ to output in Low-Z	tCLZ	0		0		0		ns	
Read command hold time referenced to $\overline{RAS}$	tRRH	0		0		0		ns	14
Output buffer turn-off delay	tOFF	0	15	0	20	0	20	ns	12
$\overline{WE}$ command setup time	tWCS	0		0		0		ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 3, 4, 5, 6, 7, 9, 10, 11, 16, 21) (0°C ≤ T_A ≤ 70°C; Vcc = 5V ±10%)

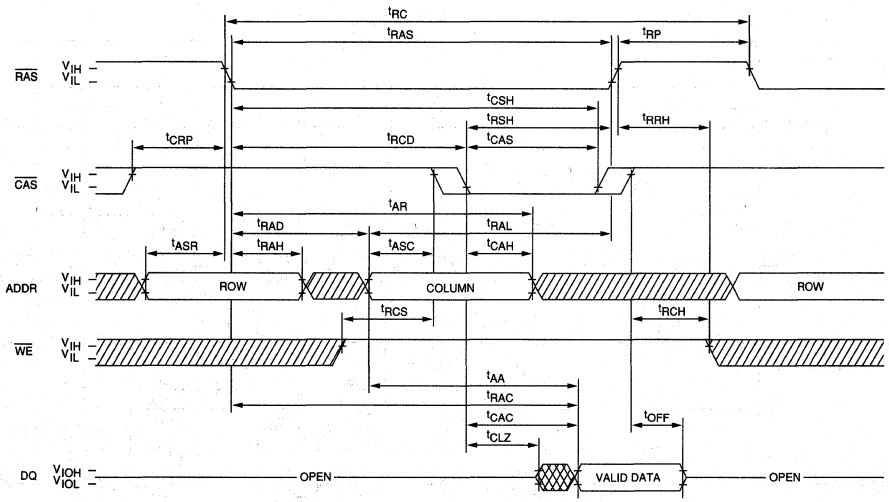
A.C. CHARACTERISTICS		-6		-7		-8			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Write command hold time	tWCH	10		15		15		ns	
Write command hold time referenced to $\overline{RAS}$	tWCR	45		55		60		ns	
Write command pulse width	tWP	10		15		15		ns	
Write command to $\overline{RAS}$ lead time	tRWL	15		20		20		ns	
Write command to $\overline{CAS}$ lead time	tCWL	15		20		20		ns	
Data-in setup time	tDS	0		0		0		ns	15
Data-in hold time	tDH	10		15		15		ns	15
Data-in hold time referenced to $\overline{RAS}$	tDHR	45		55		60		ns	
Transition time (rise or fall)	tT	3	50	3	50	3	50	ns	5, 16
Refresh period (1024 cycles)	tREF		16		16		16	ms	
$\overline{CAS}$ hold time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH)	tCHR	15		15		15		ns	19
$\overline{CAS}$ setup time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH)	tCSR	10		10		10		ns	19
$\overline{RAS}$ to $\overline{CAS}$ precharge time	tRPC	0		0		0		ns	
$\overline{WE}$ hold time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	tWRH	10		10		10		ns	22
$\overline{WE}$ setup time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	tWRP	10		10		10		ns	22
$\overline{WE}$ hold time (WCBR test cycle)	tWTH	10		10		10		ns	22
$\overline{WE}$ setup time (WCBR test cycle)	tWTS	10		10		10		ns	22

NEW DRAM MODULE

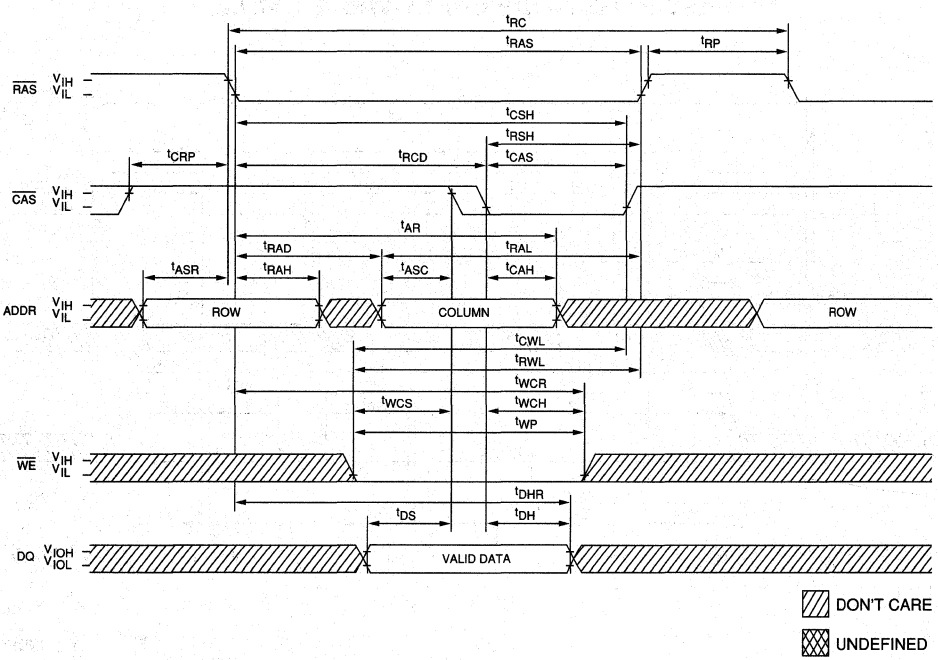
NOTES

1. All voltages referenced to V_{SS}.
2. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
3. An initial pause of 100µs is required after power-up followed by any eight $\overline{RAS}$ REFRESH cycles ($\overline{RAS}$-ONLY or CBR with $\overline{WE}$ HIGH) before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-up should be repeated any time the ^{t}REF refresh requirement is exceeded.
4. AC characteristics assume ^{t}T = 5ns.
5. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \le T_A \le 70°C$) is assured.
7. Measured with a load equivalent to two TTL gates and 100pF.
8. Assumes that $^{t}RCD < ^{t}RCD$ (MAX). If ^{t}RCD is greater than the maximum recommended value shown in this table, ^{t}RAC will increase by the amount that ^{t}RCD exceeds the value shown.
9. Assumes that $^{t}RCD \ge ^{t}RCD$ (MAX).
10. If $\overline{CAS}$ = V_{IH}, data output is High-Z.
11. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
12. ^{t}OFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
13. Operation within the ^{t}RCD (MAX) limit ensures that ^{t}RAC (MAX) can be met. ^{t}RCD (MAX) is specified as a reference point only; if ^{t}RCD is greater than the specified ^{t}RCD (MAX) limit, then access time is controlled exclusively by ^{t}CAC.
14. Either ^{t}RCH or ^{t}RRH must be satisfied for a READ cycle.
15. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY-WRITE cycles.
16. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
17. This parameter is sampled. Capacitance is measured using MIL-STD-883C, Method 3012.1 (1 MHz AC, Vcc = 5V, DC bias = 2.4V @ 15mV RMS).
18. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, data-out (Q) will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer, $\overline{CAS}$ must be pulsed HIGH for ^{t}CP.
19. On-chip refresh and address counters are enabled.
20. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW.
21. LATE-WRITE, READ-WRITE or READ-MODIFY-WRITE cycles are not available due to $\overline{OE}$ being grounded on all 4 Meg DRAMs.
22. ^{t}WTS and ^{t}WTH are setup and hold specifications for the $\overline{WE}$ pin being held LOW to enable the JEDEC test mode (with CBR timing constraints). These two parameters are the inverts of ^{t}WRP and ^{t}WRH in the CBR refresh cycle.
23. Operation within the ^{t}RAD (MAX) limit ensures that ^{t}RCD (MAX) can be met. ^{t}RAD (MAX) is specified as a reference point only; if ^{t}RAD is greater than the specified ^{t}RAD (MAX) limit, then access time is controlled exclusively by ^{t}AA.
24. All other inputs at Vcc -0.2V.
25. I_{CC} is dependent on cycle rates.

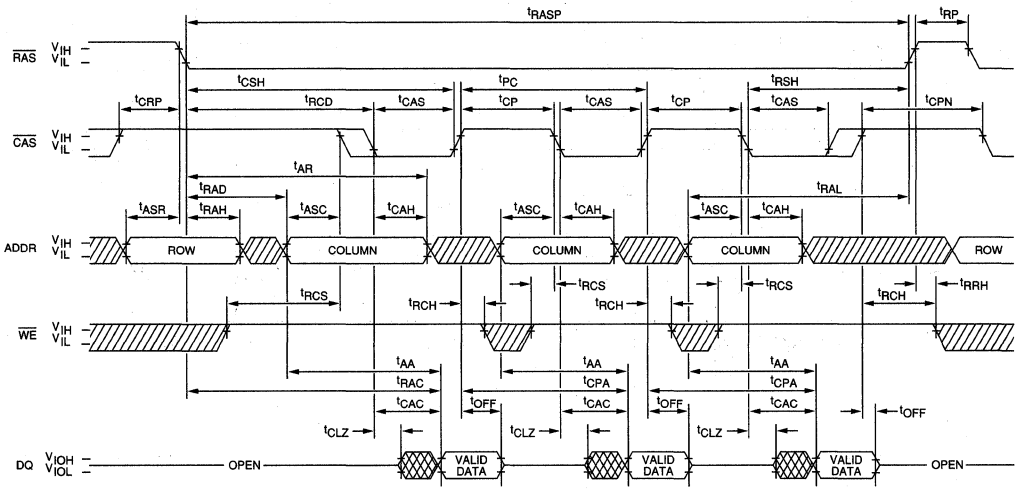
READ CYCLE



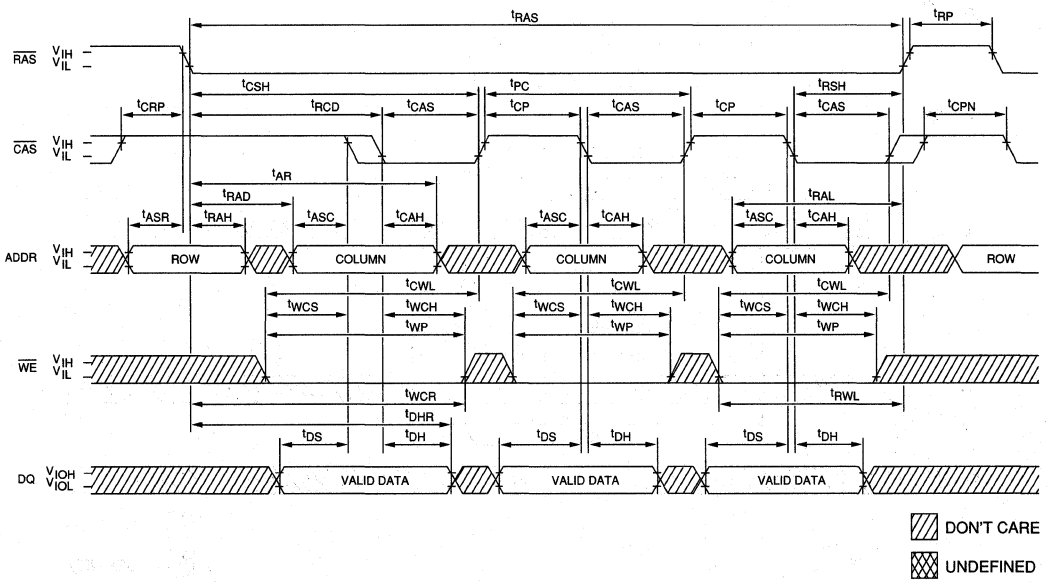
EARLY-WRITE CYCLE



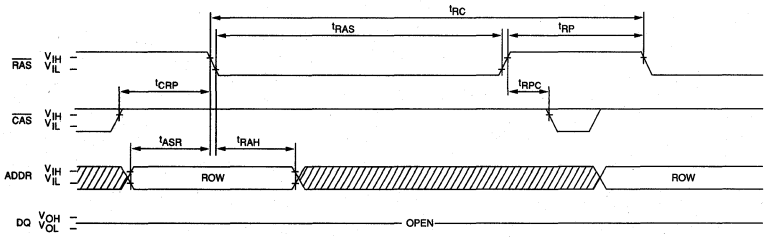
FAST-PAGE-MODE READ CYCLE



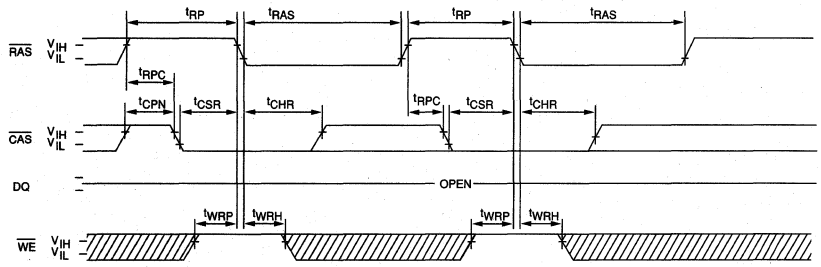
FAST-PAGE-MODE EARLY-WRITE CYCLE



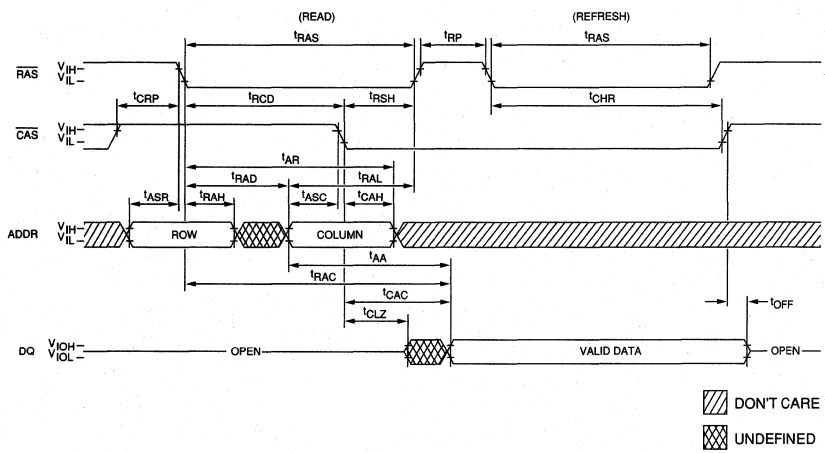
RAS-ONLY REFRESH CYCLE
(ADDR = A0-A9; WE = DON'T CARE)



CAS-BEFORE-RAS REFRESH CYCLE
(A0-A9 = DON'T CARE)



HIDDEN REFRESH CYCLE [20]
(WE = HIGH)



DRAM MODULE

512K x 36 DRAM

FAST PAGE MODE

FEATURES

- Common $\overline{RAS}$ control per side pinout in a 72-pin single-in-line package
- High-performance, CMOS silicon-gate process.
- Single 5V ±10% power supply
- All device pins are fully TTL compatible
- Low power, 54mW standby; 1,602mW active, typical
- Refresh modes: $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$ (CBR) and HIDDEN
- 512-cycle refresh distributed across 8ms
- FAST PAGE MODE access cycle

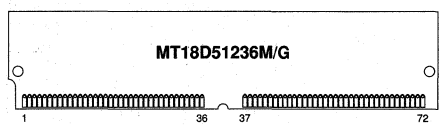
OPTIONS MARKING

- Timing
  - 60ns access - 6
  - 70ns access - 7
  - 80ns access - 8
- Packages
  - Leadless 72-pin SIMM M
  - Leadless 72-pin SIMM (Gold) G
- Part Number Example: MT18D51236G-6

PIN ASSIGNMENT (Top View)

72-Pin SIMM

(T-12)



PIN #	SYMBOL	PIN #	SYMBOL	PIN #	SYMBOL	PIN #	SYMBOL
1	Vss	19	NC	37	DQ18	55	DQ13
2	DQ1	20	DQ5	38	DQ36	56	DQ31
3	DQ19	21	DQ23	39	Vss	57	DQ14
4	DQ2	22	DQ6	40	$\overline{CAS0}$	58	DQ32
5	DQ20	23	DQ24	41	$\overline{CAS2}$	59	Vcc
6	DQ3	24	DQ7	42	$\overline{CAS3}$	60	DQ33
7	DQ21	25	DQ25	43	$\overline{CAS1}$	61	DQ15
8	DQ4	26	DQ8	44	$\overline{RAS0}$	62	DQ34
9	DQ22	27	DQ26	45	$\overline{RAS1}$	63	DQ16
10	Vcc	28	A7	46	NC	64	DQ35
11	NC	29	NC	47	$\overline{WE}$	65	DQ17
12	A0	30	Vcc	48	NC	66	NC
13	A1	31	A8	49	DQ10	67	PRD1
14	A2	32	NC	50	DQ28	68	PRD2
15	A3	33	$\overline{RAS1}$	51	DQ11	69	PRD3
16	A4	34	$\overline{RAS0}$	52	DQ29	70	PRD4
17	A5	35	DQ27	53	DQ12	71	NC
18	A6	36	DQ9	54	DQ30	72	Vss

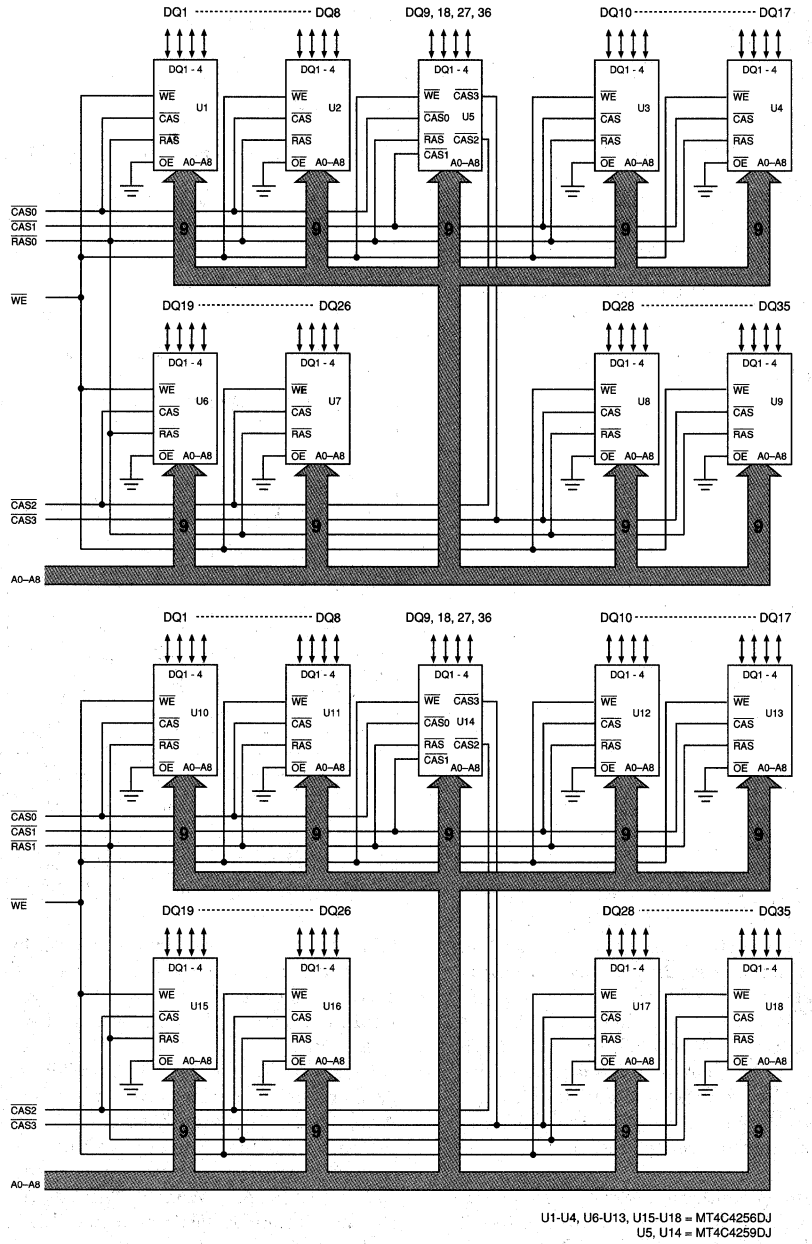
GENERAL DESCRIPTION

The MT18D51236 is a randomly accessed solid-state memory containing 524,288 words organized in a x36 configuration. During READ or WRITE cycles, each bit is uniquely addressed through the 18 address bits, which are entered 9 bits (A0-A8) at a time. $\overline{RAS}$ is used to latch the first 9 bits and $\overline{CAS}$ the latter 9 bits. READ or WRITE cycles are selected with the $\overline{WE}$ input. A logic HIGH on $\overline{WE}$ dictates READ mode while a logic LOW on $\overline{WE}$ dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. EARLY WRITE occurs when $\overline{WE}$ goes LOW prior to $\overline{CAS}$ going LOW, the output pin(s) remain open (High-Z) until the next $\overline{CAS}$ cycle.

FAST PAGE MODE operations allow faster data operations (READ or WRITE) within a row-address (A0-A8) defined page boundary. The FAST PAGE MODE cycle is always initiated with a row address strobed-in by $\overline{RAS}$ followed by a column address strobed-in by $\overline{CAS}$. $\overline{CAS}$ may be toggled-in by holding $\overline{RAS}$ LOW and strobing-in different column addresses, thus executing faster memory cycles. Returning $\overline{RAS}$ HIGH terminates the FAST PAGE MODE operation.

Returning $\overline{RAS}$ and $\overline{CAS}$ HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the $\overline{RAS}$ high time. Memory cell data is retained in its correct state by maintaining power and executing any $\overline{RAS}$ cycle (READ, WRITE, $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$ or HIDDEN REFRESH) so that all 512 combinations of $\overline{RAS}$ addresses (A0-A8) are executed at least every 8ms, regardless of sequence.

FUNCTIONAL BLOCK DIAGRAM



U1-U4, U6-U13, U15-U18 = MT4C4256DJ
U5, U14 = MT4C4259DJ

NOTE: Due to the use of a Quad $\overline{CAS}$ parity DRAM, $\overline{RAS0}$ is common to side 1 and $\overline{RAS1}$ is common to side 2.

TRUTH TABLE

FUNCTION		$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	ADDRESSES		DATA IN/OUT
					^tR	^tC	DQ1-DQ36
Standby		H	H→X	X	X	X	High-Z
READ		L	L	H	ROW	COL	Data Out
EARLY-WRITE		L	L	L	ROW	COL	Data In
FAST-PAGE-MODE	1st Cycle	L	H→L→H	H	ROW	COL	Data Out
READ	2nd Cycle	L	H→L→H	H	n/a	COL	Data Out
FAST-PAGE-MODE	1st Cycle	L	H→L→H	L	ROW	COL	Data In
WRITE	2nd Cycle	L	H→L→H	L	n/a	COL	Data In
$\overline{RAS}$-ONLY REFRESH		L	H	X	ROW	n/a	High-Z
HIDDEN	READ	L→H→L	L	H	ROW	COL	Data Out
REFRESH	WRITE	L→H→L	L	L	ROW	COL	Data In
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH		H→L	L	X	X	X	High-Z

PRESENCE DETECT

SYMBOL	-6	-7	-8
PRD1	NC	NC	NC
PRD2	Vss	Vss	Vss
PRD3	NC	Vss	NC
PRD4	NC	NC	Vss

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} ..... -1V to +7V
Operating Temperature, T_A (Ambient) ..... 0°C to +70°C
Storage Temperature (Plastic) ..... -55°C to +125°C
Power Dissipation 18W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 2, 3, 6, 23) (0°C ≤ T_A ≤ 70°C; V_{CC} = 5V ±10%)

PARAMETER/CONDITION		SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage		V_{CC}	4.5	5.5	V	1
Input High (Logic 1) Voltage, All Inputs		V_{IH}	2.4	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, All Inputs		V_{IL}	-1.0	0.8	V	1
INPUT LEAKAGE CURRENT	$\overline{CAS0}$-$\overline{CAS3}$	I_{I1}	-12	12	µA	
Any Input 0V ≤ V_{IN} ≤ V_{CC}	A0-A8, $\overline{WE}$	I_{I2}	-36	36	µA	
(All other pins not under test = 0V) For each package input	$\overline{RAS0}$, $\overline{RAS1}$	I_{I3}	-18	18	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled, 0V ≤ V_{OUT} ≤ V_{CC}) For each package input	DQ1-DQ36	I_{OZ}	-20	20	µA	
OUTPUT LEVELS		V_{OH}	2.4		V	
Output High Voltage (I_{OUT} = -5mA)						
Output Low Voltage (I_{OUT} = 5mA)		V_{OL}		0.4	V	

		MAX				
PARAMETER/CONDITION	SYMBOL	-6	-7	-8	UNITS	NOTES
STANDBY CURRENT: (TTL) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC1}	36	36	36	mA	
STANDBY CURRENT: (CMOS) ($\overline{RAS}$ = $\overline{CAS}$ = Other Inputs = V_{CC} -0.2V)	I_{CC2}	18	18	18	mA	
OPERATING CURRENT: Random READ/WRITE Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC (MIN))	I_{CC3}	828	738	648	mA	2, 23
OPERATING CURRENT: FAST PAGE MODE Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: ^tPC = ^tPC (MIN))	I_{CC4}	648	558	468	mA	2, 23
REFRESH CURRENT: $\overline{RAS}$-ONLY Average power supply current ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}: ^tRC = ^tRC (MIN))	I_{CC5}	828	738	648	mA	2
REFRESH CURRENT: $\overline{CAS}$-BEFORE-$\overline{RAS}$ Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC (MIN))	I_{CC6}	828	738	648	mA	2, 19

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A8	C_{I1}		115	pF	17
Input Capacitance: $\overline{WE}$	C_{I2}		151	pF	17
Input Capacitance: $\overline{RAS0}$, $\overline{RAS1}$	C_{I3}		76	pF	17
Input Capacitance: $\overline{CAS0}$, $\overline{CAS1}$, $\overline{CAS2}$, $\overline{CAS3}$	C_{I4}		50	pF	17
Input/Output Capacitance: DQ1-DQ36	C_{IO}		20	pF	17

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 3, 4, 5, 6, 7, 10, 11, 16, 21) (0°C ≤ T_A ≤ 70°C; Vcc = 5V ±10%)

AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	^tRC	110		130		150		ns	
READ-WRITE cycle time	^tRWC	n/a		n/a		n/a		ns	21
FAST-PAGE-MODE READ or WRITE cycle time	^tPC	40		40		45		ns	
FAST-PAGE-MODE READ-WRITE cycle time	^tPRWC	n/a		n/a		n/a		ns	21
Access time from $\overline{RAS}$	^tRAC		60		70		80	ns	8
Access time from $\overline{CAS}$	^tCAC		20		20		20	ns	9
Output Enable	^tOE		20		20		20	ns	
Access time from column address	^tAA		30		35		40	ns	
Access time from $\overline{CAS}$ precharge	^tCPA		35		40		45	ns	
$\overline{RAS}$ pulse width	^tRAS	60	100,000	70	100,000	80	100,000	ns	
$\overline{RAS}$ pulse width (FAST PAGE MODE)	^tRASP	60	100,000	70	100,000	80	100,000	ns	
$\overline{RAS}$ hold time	^tRSH	20		20		20		ns	
$\overline{RAS}$ precharge time	^tRP	40		50		60		ns	
$\overline{CAS}$ pulse width	^tCAS	20	100,000	20	100,000	20	100,000	ns	
$\overline{CAS}$ hold time	^tCSH	60		70		80		ns	
$\overline{CAS}$ precharge time	^tCPN	10		10		10		ns	18, 22
$\overline{CAS}$ precharge time (FAST PAGE MODE)	^tCP	10		10		10		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	^tRCD	20	40	20	50	20	60	ns	13
$\overline{CAS}$ to $\overline{RAS}$ precharge time	^tCRP	5		5		5		ns	
Row address setup time	^tASR	0		0		0		ns	
Row address hold time	^tRAH	10		10		10		ns	
$\overline{RAS}$ to column address delay time	^tRAD	15	30	15	35	15	40	ns	24
Column address setup time	^tASC	0		0		0		ns	
Column address hold time	^tCAH	15		15		15		ns	
Column address hold time (referenced to $\overline{RAS}$)	^tAR	45		55		60		ns	
Column address to $\overline{RAS}$ lead time	^tRAL	30		35		40		ns	
Read command setup time	^tRCS	0		0		0		ns	
Read command hold time (referenced to $\overline{CAS}$)	^tRCH	0		0		0		ns	14
Read command hold time (referenced to $\overline{RAS}$)	^tRRH	0		0		0		ns	14

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

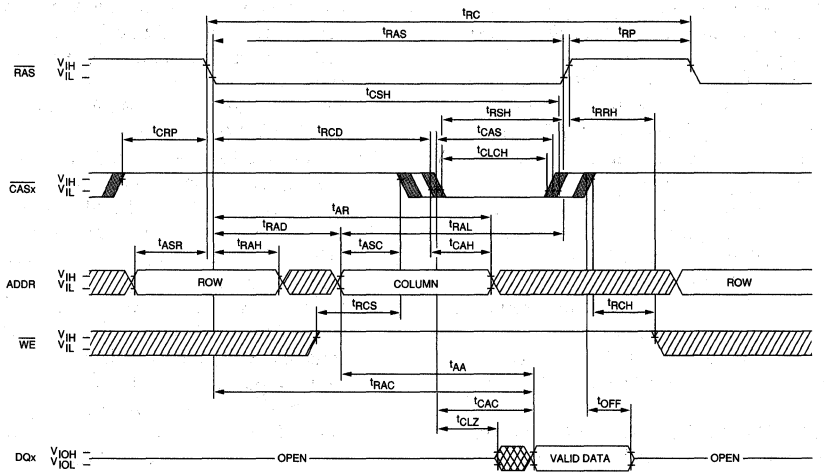
(Notes: 3, 4, 5, 6, 7, 10, 11, 16, 21) (0°C ≤ T_A ≤ 70°C; Vcc = 5V ±10%)

AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
$\overline{CAS}$ to output in Low-Z	^tCLZ	0		0		0		ns	
Output buffer turn-off delay	^tOFF	0	20	0	20	0	20	ns	12
$\overline{WE}$ command setup time	^tWCS	0		0		0		ns	
Write command hold time	^tWCH	10		15		15		ns	
Write command hold time (referenced to $\overline{RAS}$)	^tWCR	45		55		60		ns	
Write command pulse width	^tWP	10		15		15		ns	
Write command to $\overline{RAS}$ lead time	^tRWL	20		20		20		ns	
Write command to $\overline{CAS}$ lead time	^tCWL	20		20		20		ns	
Data-in setup time	^tDS	0		0		0		ns	15
Data-in hold time	^tDH	15		15		15		ns	15
Data-in hold time (referenced to $\overline{RAS}$)	^tDHR	45		55		60		ns	
Transition time (rise or fall)	^tT	3	50	3	50	3	50	ns	5, 16
Refresh period (512 cycles)	^tREF		8		8		8	ms	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	^tRPC	0		0		0		ns	
$\overline{CAS}$ setup time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tCSR	10		10		10		ns	19
$\overline{CAS}$ hold time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tCHR	10		15		15		ns	19
Last $\overline{CAS}$ going LOW to First $\overline{CAS}$ to return HIGH	^tCLCH	10		10		10		ns	

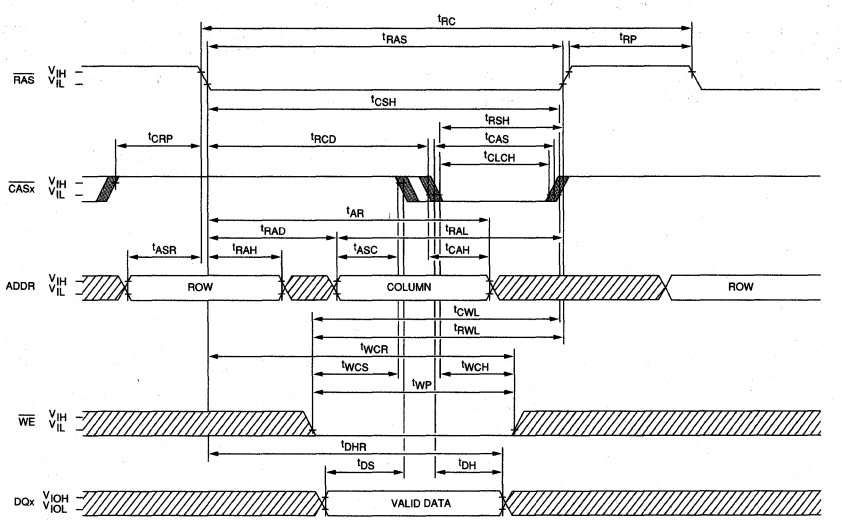
NOTES

1. All voltages referenced to V_{SS}.
2. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
3. An initial pause of 100µs is required after power-up followed by any eight $\overline{RAS}$ cycles before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-up should be repeated any time the ^tREF refresh requirement is exceeded.
4. AC characteristics assume ^tT = 5ns.
5. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \le T_A \le 70°C$) is assured.
7. Measured with a load equivalent to two TTL gates and 100pF.
8. Assumes that $^tRCD < ^tRCD$ (MAX). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
9. Assumes that $^tRCD \ge ^tRCD$ (MAX).
10. If $\overline{CAS}$ = V_{IH}, data output is High-Z.
11. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
12. ^tOFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
13. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (MAX) limit, then access time is controlled exclusively by ^tCAC.
14. Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
15. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY-WRITE cycles.
16. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
17. This parameter is sampled. Capacitance is measured using MIL-STD-883C, Method 3012.1 (1 MHz AC, Vcc = 5V, DC bias = 2.4V @ 15mV RMS).
18. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, data-out (Q) will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer, $\overline{CAS}$ must be pulsed HIGH for ^tCP.
19. On-chip refresh and address counters are enabled.
20. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW.
21. LATE-WRITE, READ-WRITE or READ-MODIFY-WRITE cycles are not available due to $\overline{OE}$ being grounded on U1-U18.
22. Last falling $\overline{CASx}$ edge to first rising $\overline{CASx}$ edge.
23. I_{CC} is dependent on cycle rates.
24. Operation within the ^tRAD (MAX) limit ensures that ^tRCD (MAX) can be met. ^tRAD (MAX) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (MAX) limit, then access time is controlled exclusively by ^tAA.

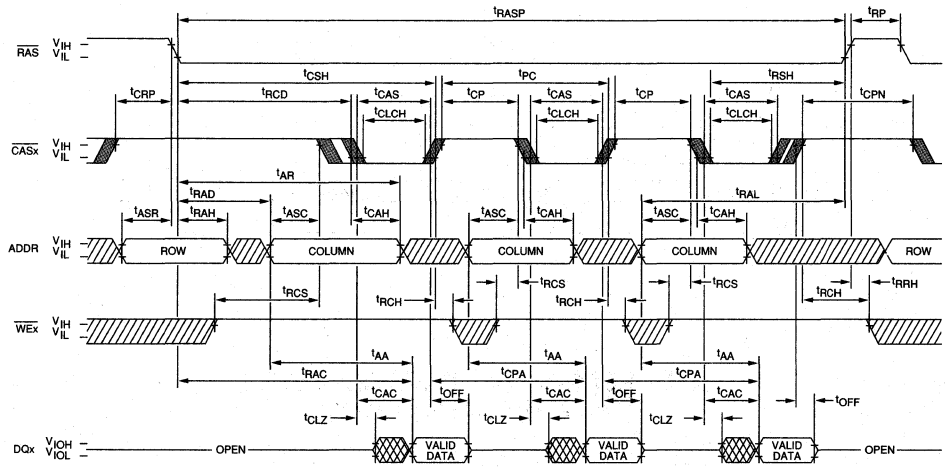
READ CYCLE



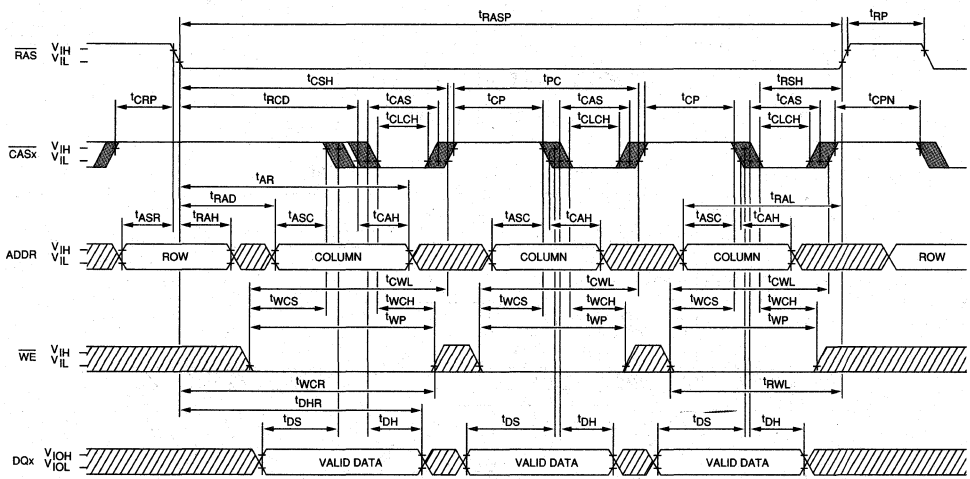
EARLY-WRITE CYCLE



FAST-PAGE-MODE READ CYCLE



FAST-PAGE-MODE EARLY-WRITE CYCLE

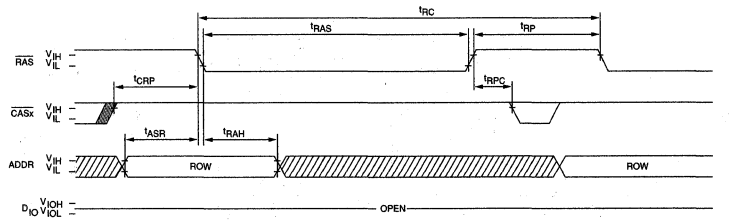


DON'T CARE

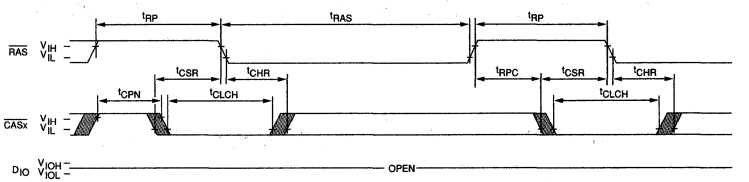
UNDEFINED

FIRST TO LAST $\overline{CAS}$ TO TRANSITION
(minimum of 1, maximum of 4)

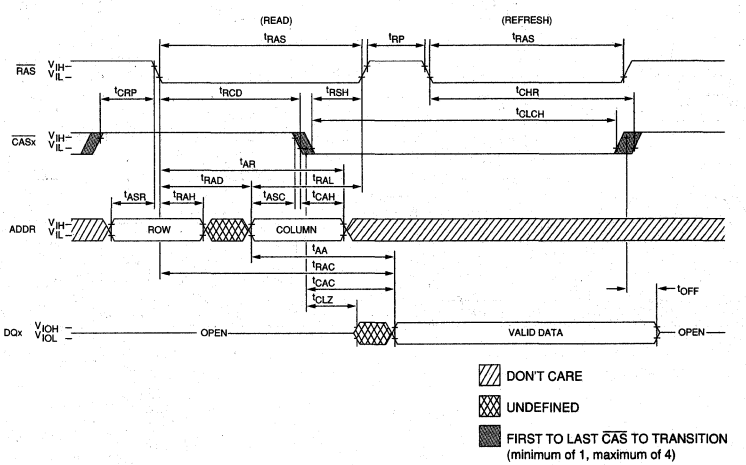
RAS-ONLY REFRESH CYCLE
(ADDR = A0-A8; WE = DON'T CARE)



CAS-BEFORE-RAS REFRESH CYCLE
(A0-A8, WE = DON'T CARE)



HIDDEN REFRESH CYCLE [20]
(WE = HIGH)



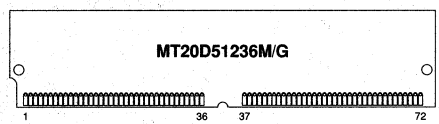
DRAM MODULE

512K x 36, 1 MEG x 18
FAST PAGE MODE

FEATURES
- Industry standard pinout in a 72-pin single-in-line package
- High-performance, CMOS silicon-gate process.
- Single 5V ±10% power supply
- All device pins are fully TTL compatible
- Low power, 60mW standby; 1,780mW active, typical
- Refresh modes: $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$ (CBR) and HIDDEN
- 512-cycle refresh distributed across 8ms
- FAST PAGE MODE access cycle
- Multiple $\overline{RAS}$ lines allow x16 or x32 width

OPTIONS — MARKING
- Timing
  - 60ns access - 6
  - 70ns access - 7
  - 80ns access - 8
- Packages
  - Leadless 72-pin SIMM M
  - Leadless 72-pin SIMM (Gold) G
- Part Number Example: MT20D51236G-6

PIN ASSIGNMENT (Top View)
72-Pin SIMM
(T-14)



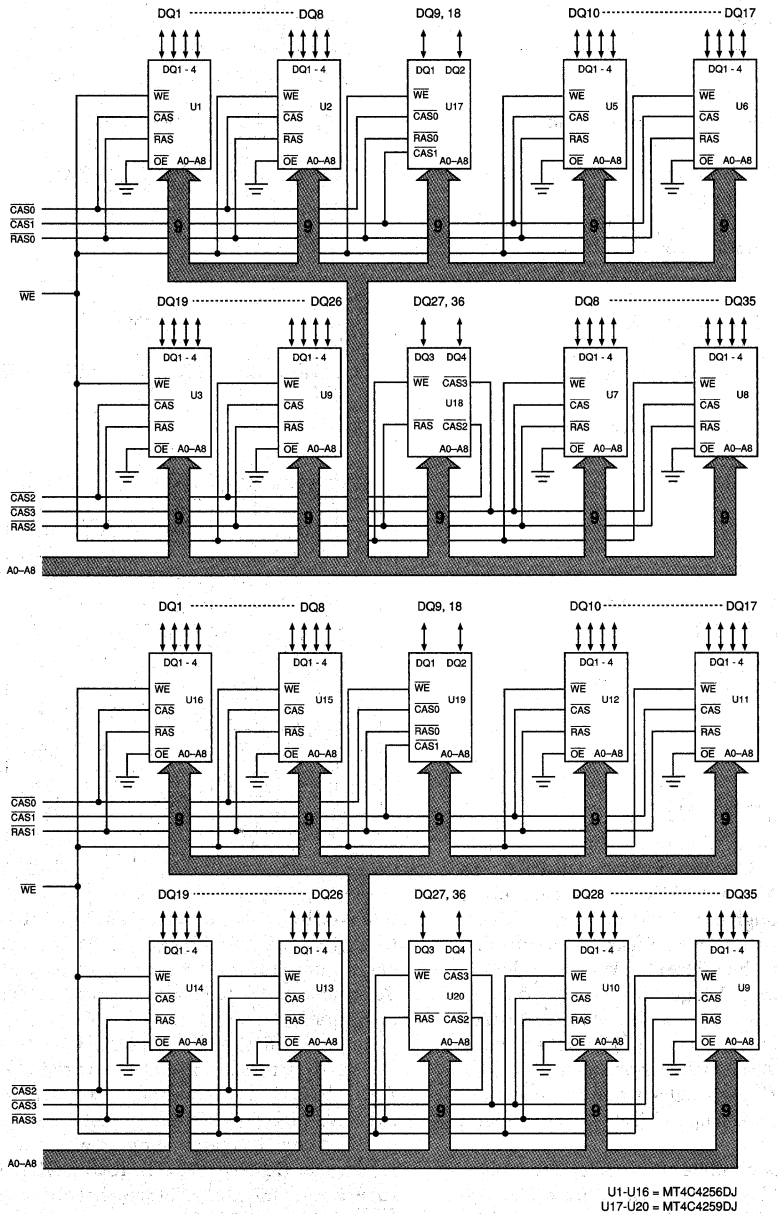
PIN #	SYMBOL	PIN #	SYMBOL	PIN #	SYMBOL	PIN #	SYMBOL
1	Vss	19	NC	37	DQ18	55	DQ13
2	DQ1	20	DQ5	38	DQ36	56	DQ31
3	DQ19	21	DQ23	39	Vss	57	DQ14
4	DQ2	22	DQ6	40	$\overline{CAS0}$	58	DQ32
5	DQ20	23	DQ24	41	$\overline{CAS2}$	59	Vcc
6	DQ3	24	DQ7	42	$\overline{CAS3}$	60	DQ33
7	DQ21	25	DQ25	43	$\overline{CAS1}$	61	DQ15
8	DQ4	26	DQ8	44	$\overline{RAS0}$	62	DQ34
9	DQ22	27	DQ26	45	$\overline{RAS1}$	63	DQ16
10	Vcc	28	A7	46	NC	64	DQ35
11	NC	29	NC	47	$\overline{WE}$	65	DQ17
12	A0	30	Vcc	48	NC	66	NC
13	A1	31	A8	49	DQ10	67	PRD1
14	A2	32	NC	50	DQ28	68	PRD2
15	A3	33	$\overline{RAS3}$	51	DQ11	69	PRD3
16	A4	34	$\overline{RAS2}$	52	DQ29	70	PRD4
17	A5	35	DQ27	53	DQ12	71	NC
18	A6	36	DQ9	54	DQ30	72	Vss

GENERAL DESCRIPTION
The MT20D51236 is a randomly accessed solid-state memory containing 524,288 words organized in a x36 configuration. During READ or WRITE cycles, each bit is uniquely addressed through the 18 address bits, which are entered 9 bits (A0-A8) at a time. $\overline{RAS}$ is used to latch the first 9 bits and $\overline{CAS}$ the latter 9 bits. READ or WRITE cycles are selected with the $\overline{WE}$ input. A logic HIGH on $\overline{WE}$ dictates READ mode while a logic LOW on $\overline{WE}$ dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. EARLY WRITE occurs when $\overline{WE}$ goes LOW prior to $\overline{CAS}$ going LOW, the output pin(s) remain open (High-Z) until the next $\overline{CAS}$ cycle.

FAST PAGE MODE operations allow faster data operations (READ or WRITE) within a row-address (A0-A8) defined page boundary. The FAST PAGE MODE cycle is always initiated with a row address strobed-in by $\overline{RAS}$ followed by a column address strobed-in by $\overline{CAS}$. $\overline{CAS}$ may be toggled-in by holding $\overline{RAS}$ LOW and strobing-in different column addresses, thus executing faster memory cycles. Returning $\overline{RAS}$ HIGH terminates the FAST PAGE MODE operation.

Returning $\overline{RAS}$ and $\overline{CAS}$ HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the $\overline{RAS}$ high time. Memory cell data is retained in its correct state by maintaining power and executing any $\overline{RAS}$ cycle (READ, WRITE, $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$ or HIDDEN REFRESH) so that all 512 combinations of $\overline{RAS}$ addresses (A0-A8) are executed at least every 8ms, regardless of sequence.

FUNCTIONAL BLOCK DIAGRAM



U1-U16 = MT4C4256DJ
U17-U20 = MT4C4259DJ

TRUTH TABLE

FUNCTION		RAS	CAS	WE	ADDRESSES		DATA IN/OUT
					^tR	^tC	DQ1-DQ36
Standby		H	H→X	X	X	X	High-Z
READ		L	L	H	ROW	COL	Data Out
EARLY-WRITE		L	L	L	ROW	COL	Data In
FAST-PAGE-MODE	1st Cycle	L	H→L→H	H	ROW	COL	Data Out
READ	2nd Cycle	L	H→L→H	H	n/a	COL	Data Out
FAST-PAGE-MODE	1st Cycle	L	H→L→H	L	ROW	COL	Data In
WRITE	2nd Cycle	L	H→L→H	L	n/a	COL	Data In
RAS-ONLY REFRESH		L	H	X	ROW	n/a	High-Z
HIDDEN	READ	L→H→L	L	H	ROW	COL	Data Out
REFRESH	WRITE	L→H→L	L	L	ROW	COL	Data In
CAS-BEFORE-RAS REFRESH		H→L	L	X	X	X	High-Z

PRESENCE DETECT

SYMBOL	-6	-7	-8
PRD1	NC	NC	NC
PRD2	Vss	Vss	Vss
PRD3	NC	Vss	NC
PRD4	NC	NC	Vss

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} ..... -1V to +7V
Operating Temperature, T_A (Ambient) ..... 0°C to +70°C
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation 20W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 2, 3, 6, 23) (0°C ≤ T_A ≤ 70°C; V_{CC} = 5V ±10%)

PARAMETER/CONDITION		SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage		V_{CC}	4.5	5.5	V	1
Input High (Logic 1) Voltage, All Inputs		V_{IH}	2.4	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, All Inputs		V_{IL}	-1.0	0.8	V	1
INPUT LEAKAGE CURRENT	$\overline{RAS0}$-$\overline{RAS3}$	I_{I1}	-10	10	µA	
Any Input 0V ≤ V_{IN} ≤ V_{CC}	A0-A8, $\overline{WE}$	I_{I2}	-40	40	µA	
(All other pins not under test = 0V) for each package input	$\overline{CAS0}$-$\overline{CAS3}$	I_{I3}	-12	12	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled, 0V ≤ V_{OUT} ≤ V_{CC}) for each package input	DQ1-DQ36	I_{OZ}	-20	20	µA	
OUTPUT LEVELS		V_{OH}	2.4		V	
Output High Voltage (I_{OUT} = -5mA)						
Output Low Voltage (I_{OUT} = 5mA)		V_{OL}		0.4	V	

		MAX				
PARAMETER/CONDITION	SYMBOL	-6	-7	-8	UNITS	NOTES
STANDBY CURRENT: (TTL) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC1}	40	40	40	mA	
STANDBY CURRENT: (CMOS) ($\overline{RAS}$ = $\overline{CAS}$ = Other Inputs = V_{CC} -0.2V)	I_{CC2}	20	20	20	mA	
OPERATING CURRENT: Random READ/WRITE Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC (MIN))	I_{CC3}	920	820	720	mA	2, 23
OPERATING CURRENT: FAST PAGE MODE ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: ^tPC = ^tPC (MIN)) Average power supply current	I_{CC4}	720	620	520	mA	2, 23
REFRESH CURRENT: $\overline{RAS}$-ONLY Average power supply current ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}: ^tRC = ^tRC (MIN))	I_{CC5}	920	820	720	mA	2
REFRESH CURRENT: $\overline{CAS}$-BEFORE-$\overline{RAS}$ Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC (MIN))	I_{CC6}	920	820	720	mA	2, 19

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A8	C_{I1}		128	pF	17
Input Capacitance: $\overline{WE}$	C_{I2}		168	pF	17
Input Capacitance: $\overline{RAS0}$, $\overline{RAS1}$, $\overline{RAS2}$, $\overline{RAS3}$	C_{I3}		42	pF	17
Input Capacitance: $\overline{CAS0}$, $\overline{CAS1}$, $\overline{CAS2}$, $\overline{CAS3}$	C_{I4}		50	pF	17
Input/Output Capacitance: DQ1-DQ36	C_{IO}		20	pF	17

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 3, 4, 5, 6, 7, 10, 11, 16, 21) (0°C ≤ T_A ≤ 70°C; V_{CC} = 5V ±10%)

AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	^tRC	110		130		150		ns	
READ-WRITE cycle time	^tRWC	n/a		n/a		n/a		ns	21
FAST-PAGE-MODE READ or WRITE cycle time	^tPC	40		40		45		ns	
FAST-PAGE-MODE READ-WRITE cycle time	^tPRWC	n/a		n/a		n/a		ns	21
Access time from $\overline{RAS}$	^tRAC		60		70		80	ns	8
Access time from $\overline{CAS}$	^tCAC		20		20		20	ns	9
Output Enable	^tOE		20		20		20	ns	
Access time from column address	^tAA		30		35		40	ns	
Access time from $\overline{CAS}$ precharge	^tCPA		35		40		45	ns	
$\overline{RAS}$ pulse width	^tRAS	60	100,000	70	100,000	80	100,000	ns	
$\overline{RAS}$ pulse width (FAST PAGE MODE)	^tRASP	60	100,000	70	100,000	80	100,000	ns	
$\overline{RAS}$ hold time	^tRSH	20		20		20		ns	
$\overline{RAS}$ precharge time	^tRP	40		50		60		ns	
$\overline{CAS}$ pulse width	^tCAS	20	100,000	20	100,000	20	100,000	ns	
$\overline{CAS}$ hold time	^tCSH	60		70		80		ns	
$\overline{CAS}$ precharge time	^tCPN	10		10		10		ns	18, 22
$\overline{CAS}$ precharge time (FAST PAGE MODE)	^tCP	10		10		10		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	^tRCD	20	40	20	50	20	60	ns	13
$\overline{CAS}$ to $\overline{RAS}$ precharge time	^tCRP	5		5		5		ns	
Row address setup time	^tASR	0		0		0		ns	
Row address hold time	^tRAH	10		10		10		ns	
$\overline{RAS}$ to column address delay time	^tRAD	15	30	15	35	15	40	ns	24
Column address setup time	^tASC	0		0		0		ns	
Column address hold time	^tCAH	15		15		15		ns	
Column address hold time (referenced to $\overline{RAS}$)	^tAR	45		55		60		ns	
Column address to $\overline{RAS}$ lead time	^tRAL	30		35		40		ns	
Read command setup time	^tRCS	0		0		0		ns	
Read command hold time (referenced to $\overline{CAS}$)	^tRCH	0		0		0		ns	14
Read command hold time (referenced to $\overline{RAS}$)	^tRRH	0		0		0		ns	14

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

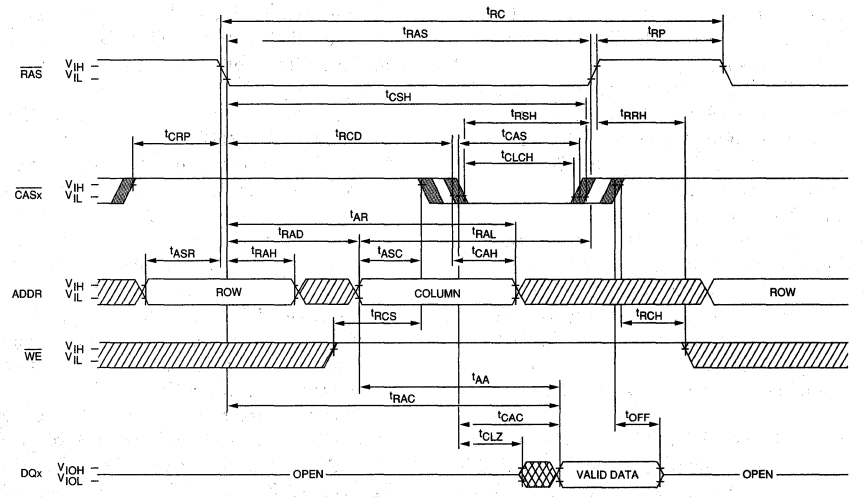
(Notes: 3, 4, 5, 6, 7, 10, 11, 16, 21) (0°C ≤ T_A ≤ 70°C; Vcc = 5V ±10%)

AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
$\overline{CAS}$ to output in Low-Z	^tCLZ	0		0		0		ns	
Output buffer turn-off delay	^tOFF	0	20	0	20	0	20	ns	12
$\overline{WE}$ command setup time	^tWCS	0		0		0		ns	
Write command hold time	^tWCH	10		15		15		ns	
Write command hold time (referenced to $\overline{RAS}$)	^tWCR	45		55		60		ns	
Write command pulse width	^tWP	10		15		15		ns	
Write command to $\overline{RAS}$ lead time	^tRWL	20		20		20		ns	
Write command to $\overline{CAS}$ lead time	^tCWL	20		20		20		ns	
Data-in setup time	^tDS	0		0		0		ns	15
Data-in hold time	^tDH	15		15		15		ns	15
Data-in hold time (referenced to $\overline{RAS}$)	^tDHR	45		55		60		ns	
Transition time (rise or fall)	^tT	3	50	3	50	3	50	ns	5, 16
Refresh period (512 cycles)	^tREF		8		8		8	ms	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	^tRPC	0		0		0		ns	
$\overline{CAS}$ setup time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tCSR	10		10		10		ns	19
$\overline{CAS}$ hold time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tCHR	10		15		15		ns	19
Last $\overline{CAS}$ going LOW to First $\overline{CAS}$ to return HIGH	^tCLCH	10		10		10		ns	22

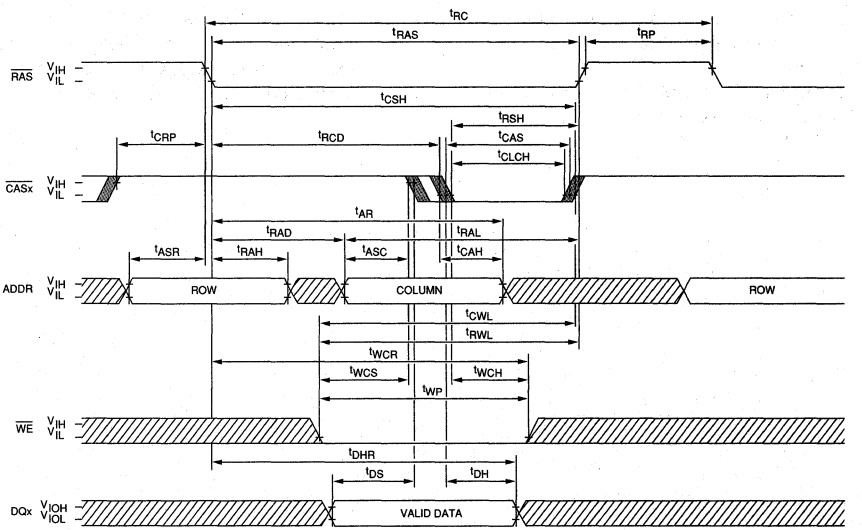
NOTES

1. All voltages referenced to V_{SS}.
2. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
3. An initial pause of 100µs is required after power-up followed by any eight $\overline{RAS}$ cycles before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-up should be repeated any time the ^{t}REF refresh requirement is exceeded.
4. AC characteristics assume ^{t}T = 5ns.
5. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \le T_A \le 70°C$) is assured.
7. Measured with a load equivalent to two TTL gates and 100pF.
8. Assumes that $^{t}RCD < ^{t}RCD$ (MAX). If ^{t}RCD is greater than the maximum recommended value shown in this table, ^{t}RAC will increase by the amount that ^{t}RCD exceeds the value shown.
9. Assumes that $^{t}RCD \ge ^{t}RCD$ (MAX).
10. If $\overline{CAS}$ = V_{IH}, data output is High-Z.
11. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
12. ^{t}OFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
13. Operation within the ^{t}RCD (MAX) limit ensures that ^{t}RAC (MAX) can be met. ^{t}RCD (MAX) is specified as a reference point only; if ^{t}RCD is greater than the specified ^{t}RCD (MAX) limit, then access time is controlled exclusively by ^{t}CAC.
14. Either ^{t}RCH or ^{t}RRH must be satisfied for a READ cycle.
15. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY-WRITE cycles.
16. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
17. This parameter is sampled. Capacitance is measured using MIL-STD-883C, Method 3012.1 (1 MHz AC, Vcc = 5V, DC bias = 2.4V @ 15mV RMS).
18. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, data-out (Q) will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer, $\overline{CAS}$ must be pulsed HIGH for ^{t}CP.
19. On-chip refresh and address counters are enabled.
20. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW.
21. LATE-WRITE, READ-WRITE or READ-MODIFY-WRITE cycles are not available due to $\overline{OE}$ being grounded on U1-U18.
22. Last falling $\overline{CASx}$ edge to first rising $\overline{CASx}$ edge.
23. I_{CC} is dependent on cycle rates.
24. Operation within the ^{t}RAD (MAX) limit ensures that ^{t}RCD (MAX) can be met. ^{t}RAD (MAX) is specified as a reference point only; if ^{t}RAD is greater than the specified ^{t}RAD (MAX) limit, then access time is controlled exclusively by ^{t}AA.

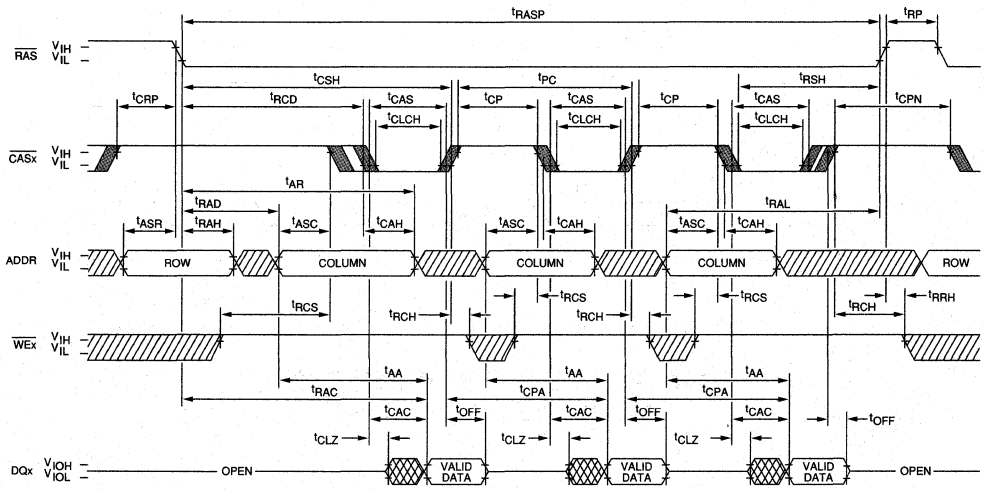
READ CYCLE



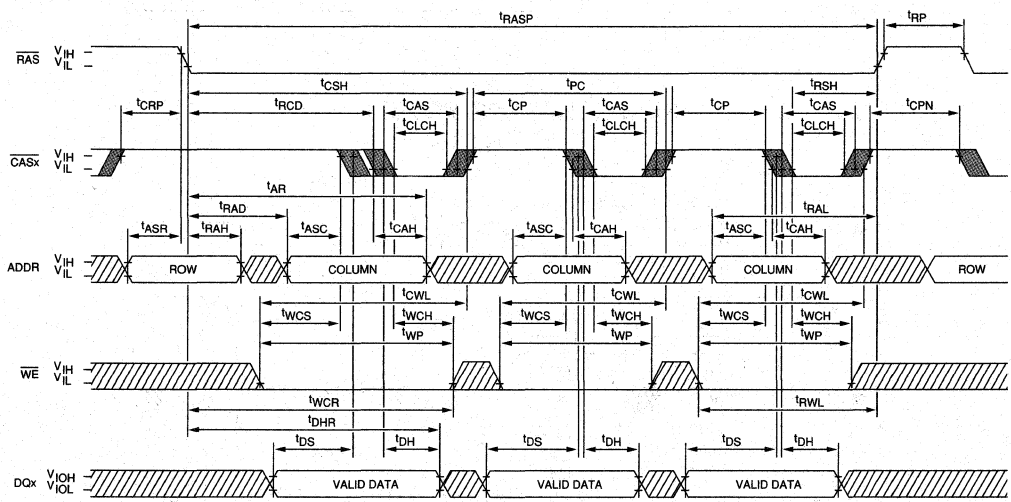
EARLY-WRITE CYCLE



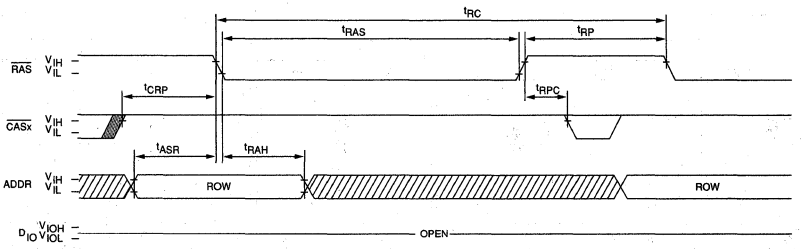
FAST-PAGE-MODE READ CYCLE



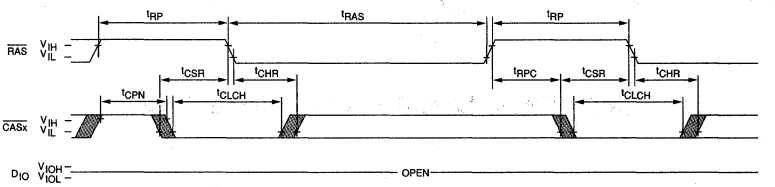
FAST-PAGE-MODE EARLY-WRITE CYCLE



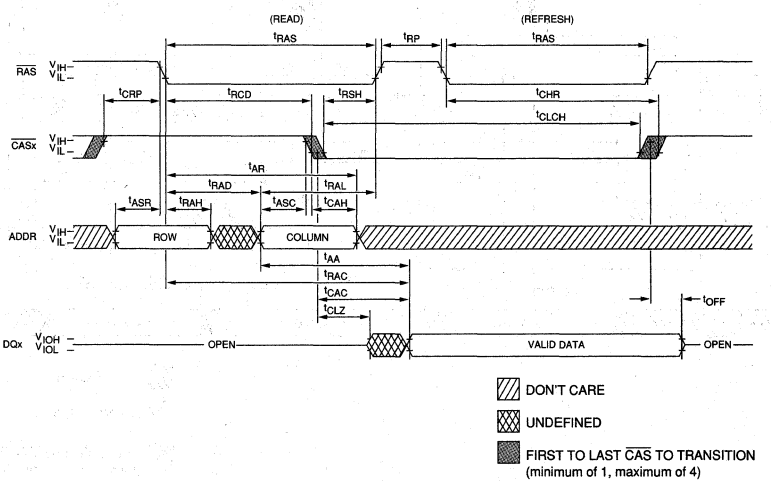
$\overline{\text{RAS}}$-ONLY REFRESH CYCLE
(ADDR = A0-A8; $\overline{\text{WE}}$ = DON'T CARE)



$\overline{\text{CAS}}$-BEFORE-$\overline{\text{RAS}}$ REFRESH CYCLE
(A0-A8, $\overline{\text{WE}}$ = DON'T CARE)



HIDDEN REFRESH CYCLE [20]
($\overline{\text{WE}}$ = HIGH)



DRAM MODULE

1 MEG x 36 DRAM

FAST PAGE MODE

FEATURES

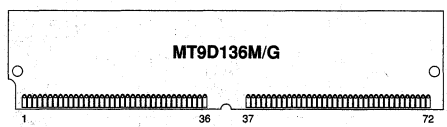
- Common $\overline{RAS}$ control pinout in a 72-pin single-in-line package
- High-performance, CMOS silicon-gate process.
- Single 5V ±10% power supply
- All device pins are fully TTL compatible
- Low power, 27mW standby; 2,175mW active, typical
- Refresh modes: $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$ (CBR) and HIDDEN
- 1,024-cycle refresh distributed across 16ms
- FAST PAGE MODE access cycle

OPTIONS — MARKING

- Timing
  - 60ns access — -6
  - 70ns access — -7
  - 80ns access — -8
- Packages
  - Leadless 72-pin SIMM — M
  - Leadless 72-pin SIMM (Gold) — G
- Part Number Example: MT9D136G-6

PIN ASSIGNMENT (Top View)

72-Pin SIMM
(T-11)



PIN #	SYMBOL	PIN #	SYMBOL	PIN #	SYMBOL	PIN #	SYMBOL
1	Vss	19	NC	37	DQ18	55	DQ13
2	DQ1	20	DQ5	38	DQ36	56	DQ31
3	DQ19	21	DQ23	39	Vss	57	DQ14
4	DQ2	22	DQ6	40	$\overline{CAS0}$	58	DQ32
5	DQ20	23	DQ24	41	$\overline{CAS2}$	59	Vcc
6	DQ3	24	DQ7	42	$\overline{CAS3}$	60	DQ33
7	DQ21	25	DQ25	43	$\overline{CAS1}$	61	DQ15
8	DQ4	26	DQ8	44	$\overline{RAS0}$	62	DQ34
9	DQ22	27	DQ26	45	NC	63	DQ16
10	Vcc	28	A7	46	NC	64	DQ35
11	NC	29	NC	47	$\overline{WE}$	65	DQ17
12	A0	30	Vcc	48	NC	66	NC
13	A1	31	A8	49	DQ10	67	PRD1
14	A2	32	A9	50	DQ28	68	PRD2
15	A3	33	NC	51	DQ11	69	PRD3
16	A4	34	$\overline{RAS0}$	52	DQ29	70	PRD4
17	A5	35	DQ27	53	DQ12	71	NC
18	A6	36	DQ9	54	DQ30	72	Vss

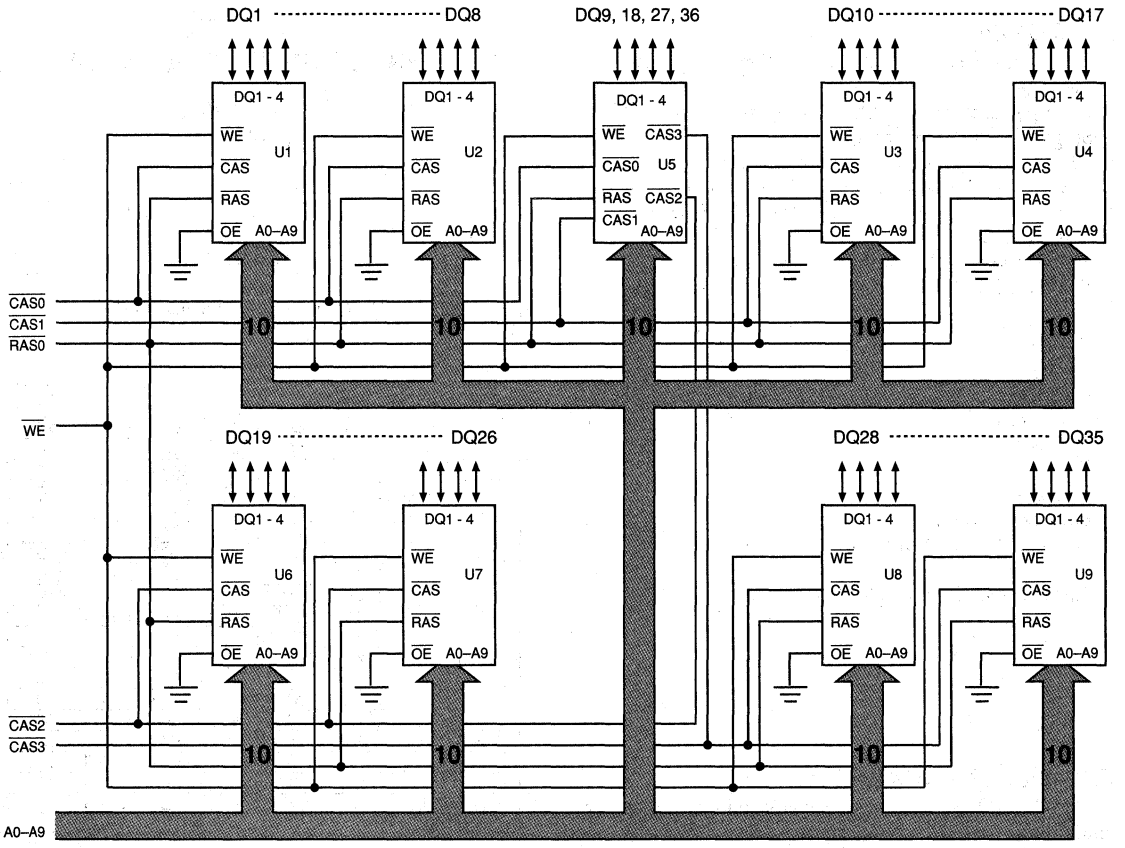
GENERAL DESCRIPTION

The MT9D136 is a randomly accessed solid-state memory containing 1,048,576 words organized in a x36 configuration. During READ or WRITE cycles, each bit is uniquely addressed through the 20 address bits which are entered 10 bits (A0-A9) at a time. $\overline{RAS}$ is used to latch the first 10 bits and $\overline{CAS}$ the latter 10 bits. READ or WRITE cycles are selected with the $\overline{WE}$ input. A logic HIGH on $\overline{WE}$ dictates READ mode while a logic LOW on $\overline{WE}$ dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. If $\overline{WE}$ goes LOW prior to $\overline{CAS}$ going LOW, the output pin(s) remain open (High-Z) until the next $\overline{CAS}$ cycle.

FAST PAGE MODE operations allow faster data operations (READ or WRITE) within a row-address (A0-A9) defined page boundary. The FAST PAGE MODE cycle is always initiated with a row address strobed-in by $\overline{RAS}$ followed by a column address strobed-in by $\overline{CAS}$. $\overline{CAS}$ may be toggled-in by holding $\overline{RAS}$ LOW and strobing-in different column addresses, thus executing faster memory cycles. Returning $\overline{RAS}$ HIGH terminates the FAST PAGE MODE operation.

Returning $\overline{RAS}$ and $\overline{CAS}$ HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the $\overline{RAS}$ high time. Memory cell data is retained in its correct state by maintaining power and executing any $\overline{RAS}$ cycle (READ, WRITE, $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$ or HIDDEN REFRESH) so that all 1,024 combinations of $\overline{RAS}$ addresses (A0-A9) are executed at least every 16ms, regardless of sequence.

FUNCTIONAL BLOCK DIAGRAM



U1-U4, U6-U9 = MT4C4001JDJ
U5 = MT4C4004JDJ

NOTE: Due to the use of a Quad $\overline{CAS}$ DRAM, $\overline{RAS0}$ is common to all devices.

TRUTH TABLE

FUNCTION		RAS	CAS	WE	ADDRESSES		DATA IN/OUT
					^tR	^tC	DQ1-DQ36
Standby		H	H→X	X	X	X	High-Z
READ		L	L	H	ROW	COL	Data Out
EARLY-WRITE		L	L	L	ROW	COL	Data In
FAST-PAGE-MODE	1st Cycle	L	H→L	H	ROW	COL	Data Out
READ	2nd Cycle	L	H→L	H	n/a	COL	Data Out
FAST-PAGE-MODE	1st Cycle	L	H→L	L	ROW	COL	Data In
WRITE	2nd Cycle	L	H→L	L	n/a	COL	Data In
RAS-ONLY REFRESH		L	H	X	ROW	n/a	High-Z
HIDDEN	READ	L→H→L	L	H	ROW	COL	Data Out
REFRESH	WRITE	L→H→L	L	L	ROW	COL	Data In
CAS-BEFORE-RAS REFRESH		H→L	L	H	X	X	High-Z

PRESENCE DETECT

SYMBOL	-6	-7	-8
PRD1	Vss	Vss	Vss
PRD2	Vss	Vss	Vss
PRD3	NC	Vss	NC
PRD4	NC	NC	Vss

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} ..... -1V to +7V
Operating Temperature, T_A (Ambient) ..... 0°C to +70°C
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation 9W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 2, 3, 6, 23) (0°C ≤ T_A ≤ 70°C; Vcc = 5V ±10%)

PARAMETER/CONDITION		SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage		V_{CC}	4.5	5.5	V	1
Input High (Logic 1) Voltage, All Inputs		V_{IH}	2.4	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, All Inputs		V_{IL}	-1.0	0.8	V	1
INPUT LEAKAGE CURRENT	$\overline{CAS0}$-$\overline{CAS3}$	I_{I1}	-6	6	µA	
Any Input 0V ≤ V_{IN} ≤ V_{CC}	A0-A8, $\overline{WE}$,	I_{I2}	-18	18	µA	
(All other pins not under test = 0V) For each package input	$\overline{RAS0}$					
OUTPUT LEAKAGE CURRENT	DQ1-DQ36	I_{OZ}	-10	10	µA	
(Q is disabled, 0V ≤ V_{OUT} ≤ V_{CC}) For each package input						
OUTPUT LEVELS		V_{OH}	2.4		V	
Output High Voltage (I_{OUT} = -5mA)						
Output Low Voltage (I_{OUT} = 5mA)		V_{OL}		0.4	V	

		MAX				
PARAMETER/CONDITION	SYMBOL	-6	-7	-8	UNITS	NOTES
STANDBY CURRENT: (TTL) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC1}	18	18	18	mA	
STANDBY CURRENT: (CMOS) ($\overline{RAS}$ = $\overline{CAS}$ = Other Inputs = V_{CC} -0.2V)	I_{CC2}	9	9	9	mA	
OPERATING CURRENT: Random READ/WRITE Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC (MIN))	I_{CC3}	990	900	810	mA	2, 23
OPERATING CURRENT: FAST PAGE MODE Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: ^tPC = ^tPC (MIN))	I_{CC4}	720	630	540	mA	2, 23
REFRESH CURRENT: $\overline{RAS}$-ONLY Average power supply current ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}: ^tRC = ^tRC (MIN))	I_{CC5}	990	900	810	mA	2
REFRESH CURRENT: $\overline{CAS}$-BEFORE-$\overline{RAS}$ Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC (MIN))	I_{CC6}	990	900	810	mA	2, 19

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A9	C_{I1}		58	pF	17
Input Capacitance: $\overline{WE}$	C_{I2}		76	pF	17
Input Capacitance: $\overline{RAS0}$	C_{I3}		76	pF	17
Input Capacitance: $\overline{CAS0}$, $\overline{CAS1}$, $\overline{CAS2}$, $\overline{CAS3}$	C_{I4}		25	pF	17
Input/Output Capacitance: DQ1-DQ36	C_{IO}		10	pF	17

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 3, 4, 5, 6, 7, 10, 11, 16, 21) ($0°C \le T_A \le 70°C$; V_{CC} = 5V ±10%)

AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	^tRC	110		130		150		ns	
READ-WRITE cycle time	^tRWC	n/a		n/a		n/a		ns	21
FAST-PAGE-MODE READ or WRITE cycle time	^tPC	40		40		45		ns	
FAST-PAGE-MODE READ-WRITE cycle time	^tPRWC	n/a		n/a		n/a		ns	21
Access time from $\overline{RAS}$	^tRAC		60		70		80	ns	8
Access time from $\overline{CAS}$	^tCAC		15		20		20	ns	9
Output Enable	^tOE		15		20		20	ns	
Access time from column address	^tAA		30		35		40	ns	
Access time from $\overline{CAS}$ precharge	^tCPA		35		40		45	ns	
$\overline{RAS}$ pulse width	^tRAS	60	100,000	70	100,000	80	100,000	ns	
$\overline{RAS}$ pulse width (FAST PAGE MODE)	^tRASP	60	100,000	70	100,000	80	100,000	ns	
$\overline{RAS}$ hold time	^tRSH	15		20		20		ns	
$\overline{RAS}$ precharge time	^tRP	40		50		60		ns	
$\overline{CAS}$ pulse width	^tCAS	15	100,000	20	100,000	20	100,000	ns	
$\overline{CAS}$ hold time	^tCSH	60		70		80		ns	
$\overline{CAS}$ precharge time	^tCPN	10		10		10		ns	18, 22
$\overline{CAS}$ precharge time (FAST PAGE MODE)	^tCP	10		10		10		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	^tRCD	20	45	20	50	20	60	ns	13
$\overline{CAS}$ to $\overline{RAS}$ precharge time	^tCRP	10		10		10		ns	
Row address setup time	^tASR	0		0		0		ns	
Row address hold time	^tRAH	10		10		10		ns	
$\overline{RAS}$ to column address delay time	^tRAD	15	30	15	35	15	40	ns	24
Column address setup time	^tASC	0		0		0		ns	
Column address hold time	^tCAH	10		15		15		ns	
Column address hold time (referenced to $\overline{RAS}$)	^tAR	50		55		60		ns	
Column address to $\overline{RAS}$ lead time	^tRAL	30		35		40		ns	
Read command setup time	^tRCS	0		0		0		ns	
Read command hold time (referenced to $\overline{CAS}$)	^tRCH	0		0		0		ns	14
Read command hold time (referenced to $\overline{RAS}$)	^tRRH	0		0		0		ns	14

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

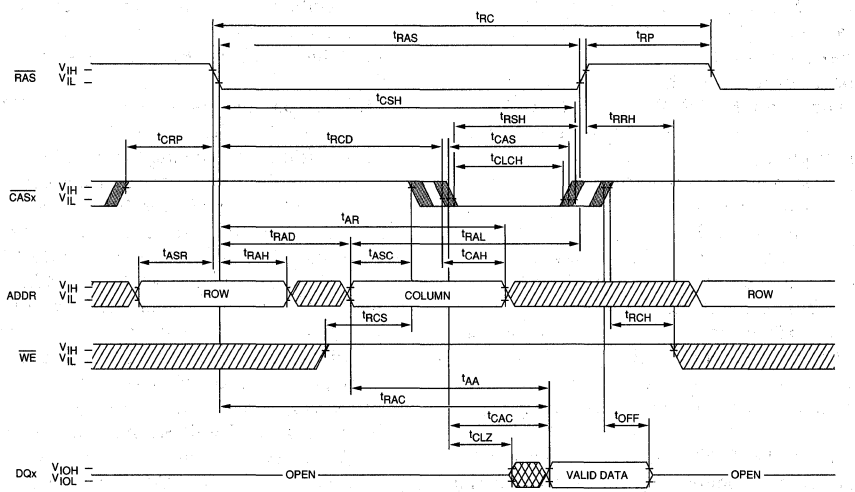
(Notes: 3, 4, 5, 6, 7, 10, 11, 16, 21) ($0°C \le T_A \le 70°C$; V_{CC} = 5V ±10%)

AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
$\overline{CAS}$ to output in Low-Z	^tCLZ	0		0		0		ns	
Output buffer turn-off delay	^tOFF	0	15	0	20	0	20	ns	12
$\overline{WE}$ command setup time	^tWCS	0		0		0		ns	
Write command hold time	^tWCH	10		15		15		ns	
Write command hold time (referenced to $\overline{RAS}$)	^tWCR	45		55		60		ns	
Write command pulse width	^tWP	10		15		15		ns	
Write command to $\overline{RAS}$ lead time	^tRWL	15		20		20		ns	
Write command to $\overline{CAS}$ lead time	^tCWL	15		20		20		ns	
Data-in setup time	^tDS	0		0		0		ns	15
Data-in hold time	^tDH	10		15		15		ns	15
Data-in hold time (referenced to $\overline{RAS}$)	^tDHR	45		55		60		ns	
Transition time (rise or fall)	^tT	3	50	3	50	3	50	ns	5, 16
Refresh period (1,024 cycles)	^tREF		16		16		16	ms	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	^tRPC	0		0		0		ns	
$\overline{CAS}$ setup time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tCSR	10		10		10		ns	19
$\overline{CAS}$ hold time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tCHR	15		15		15		ns	19
$\overline{WE}$ hold time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tWRH	10		10		10		ns	
$\overline{WE}$ setup time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tWRP	10		10		10		ns	
$\overline{WE}$ hold time (WCBR test cycle)	^tWTH	10		10		10		ns	
$\overline{WE}$ setup time (WCBR test cycle)	^tWTS	10		10		10		ns	
Last $\overline{CAS}$ going LOW to First $\overline{CAS}$ to return HIGH	^tCLCH	10		10		10		ns	22

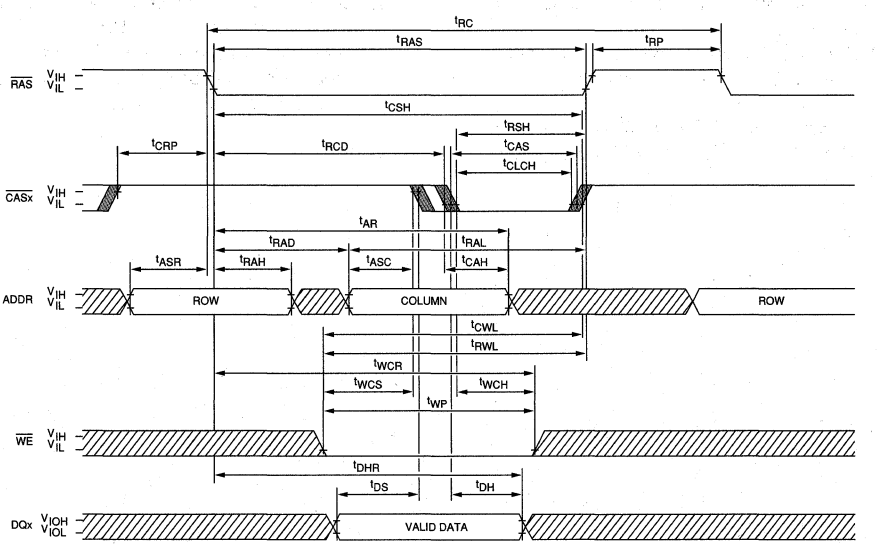
NOTES

1. All voltages referenced to V_{SS}.
2. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
3. An initial pause of 100µs is required after power-up followed by any eight $\overline{RAS}$ REFRESH cycles ($\overline{RAS}$-ONLY or CBR with $\overline{WE}$ HIGH) before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-up should be repeated any time the ^tREF refresh requirement is exceeded.
4. AC characteristics assume ^tT = 5ns.
5. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \le T_A \le 70°C$) is assured.
7. Measured with a load equivalent to two TTL gates and 100pF.
8. Assumes that $^tRCD < ^tRCD$ (MAX). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
9. Assumes that $^tRCD \ge ^tRCD$ (MAX).
10. If $\overline{CAS}$ = V_{IH}, data output is High-Z.
11. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
12. ^tOFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
13. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (MAX) limit, then access time is controlled exclusively by ^tCAC.
14. Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
15. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY-WRITE cycles.
16. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
17. This parameter is sampled. Capacitance is measured using MIL-STD-883C, Method 3012.1 (1 MHz AC, Vcc = 5V, DC bias = 2.4V @ 15mV RMS).
18. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, data-out (Q) will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer, $\overline{CAS}$ must be pulsed HIGH for ^tCP.
19. On-chip refresh and address counters are enabled.
20. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW.
21. LATE-WRITE, READ-WRITE or READ-MODIFY-WRITE cycles are not available due to $\overline{OE}$ being grounded on U1-U9.
22. Last falling $\overline{CASx}$ edge to first rising $\overline{CASx}$ edge.
23. I_{CC} is dependent on cycle rates.
24. Operation within the ^tRAD (MAX) limit ensures that ^tRCD (MAX) can be met. ^tRAD (MAX) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (MAX) limit, then access time is controlled exclusively by ^tAA.

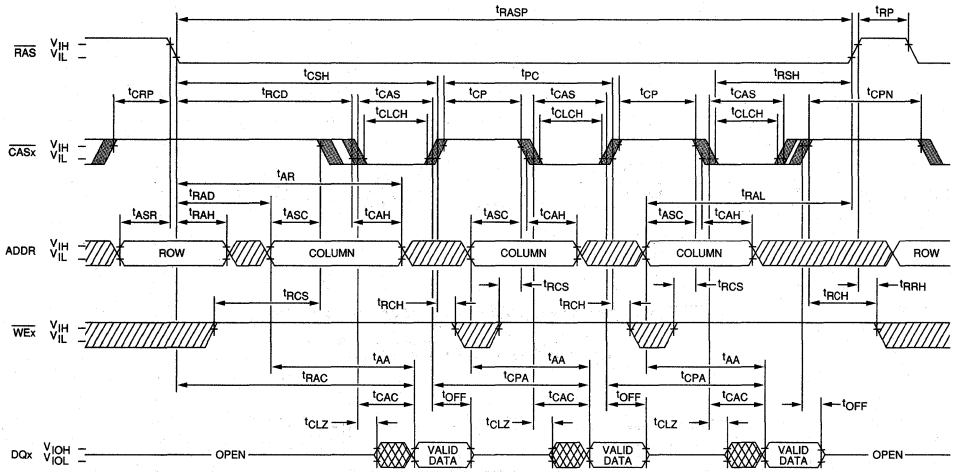
READ CYCLE



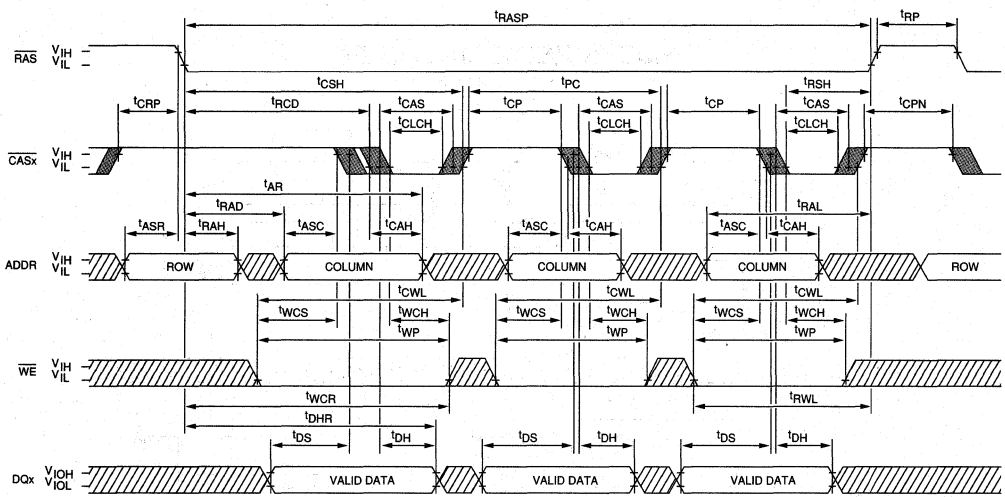
EARLY-WRITE CYCLE



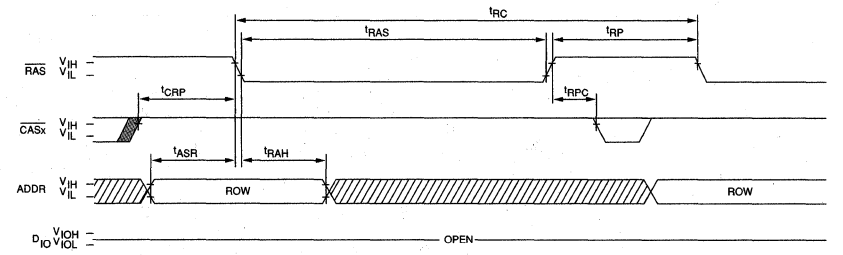
FAST-PAGE-MODE READ CYCLE



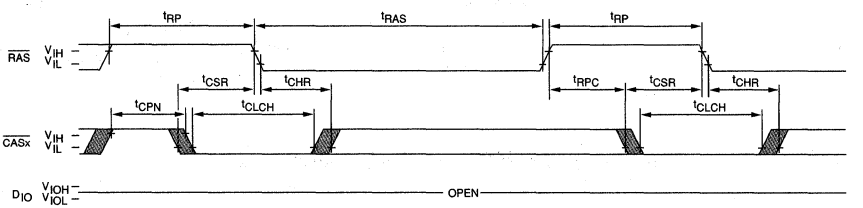
FAST-PAGE-MODE EARLY-WRITE CYCLE



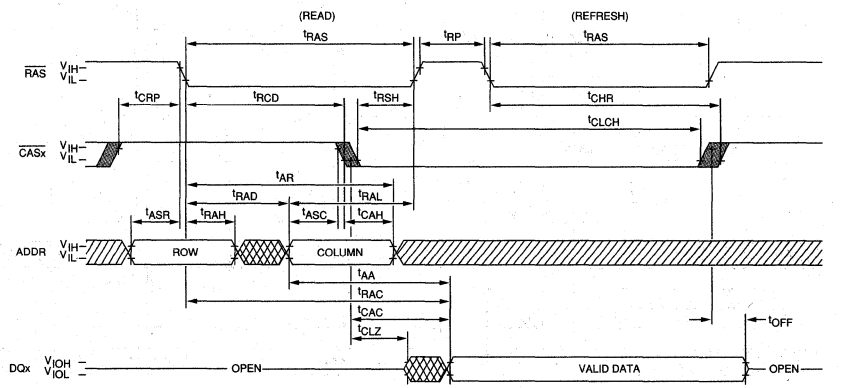
$\overline{\text{RAS}}$-ONLY REFRESH CYCLE
(ADDR = A0-A9; $\overline{\text{WE}}$ = DON'T CARE)



$\overline{\text{CAS}}$-BEFORE-$\overline{\text{RAS}}$ REFRESH CYCLE
(A0-A9 = DON'T CARE)



HIDDEN REFRESH CYCLE [20]
($\overline{\text{WE}}$ = HIGH)



DRAM MODULE

1 MEG x 36, 2 MEG x 18

FAST PAGE MODE (MT12D136)
LOW POWER,
EXTENDED REFRESH (MT12D136 L)

NEW DRAM MODULE

FEATURES

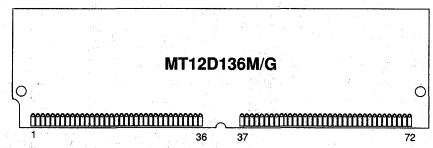
- Industry standard pinout in a 72-pin single-in-line package
- High-performance, CMOS silicon-gate process
- Single 5V ±10% power supply
- All device pins are fully TTL compatible
- Low power, 36mW (9.2mW L-version) standby; 2,500mW active, typical
- Refresh modes: $\overline{\text{RAS}}$-ONLY, $\overline{\text{CAS}}$-BEFORE-$\overline{\text{RAS}}$ (CBR) and HIDDEN
- 1,024-cycle refresh distributed across 16ms or 1,024-cycle extended refresh distributed across 128ms
- FAST PAGE MODE access cycle
- Low CMOS standby current, 2.4mA maximum (L-version)
- Multiple $\overline{\text{RAS}}$ lines allow x18 or x36 width

OPTIONS — MARKING

- Timing
  - 60ns access — -6
  - 70ns access — -7
  - 80ns access — -8
- Packages
  - Leadless 72-pin SIMM — M
  - Leadless 72-pin SIMM (Gold) — G
- Power/Refresh
  - Normal Power/16ms — Blank
  - Low Power/128ms — L
- Part Number Example: MT12D136GL-6

PIN ASSIGNMENT (Top View)

72-Pin SIMM
(T-19)



PIN #	SYMBOL	PIN #	SYMBOL	PIN #	SYMBOL	PIN #	SYMBOL
1	Vss	19	NC	37	DQ18	55	DQ13
2	DQ1	20	DQ5	38	DQ36	56	DQ31
3	DQ19	21	DQ23	39	Vss	57	DQ14
4	DQ2	22	DQ6	40	$\overline{\text{CAS0}}$	58	DQ32
5	DQ20	23	DQ24	41	$\overline{\text{CAS2}}$	59	Vcc
6	DQ3	24	DQ7	42	$\overline{\text{CAS3}}$	60	DQ33
7	DQ21	25	DQ25	43	$\overline{\text{CAS1}}$	61	DQ15
8	DQ4	26	DQ8	44	$\overline{\text{RAS0}}$	62	DQ34
9	DQ22	27	DQ26	45	NC	63	DQ16
10	Vcc	28	A7	46	NC	64	DQ35
11	NC	29	NC	47	$\overline{\text{WE}}$	65	DQ17
12	A0	30	Vcc	48	NC	66	NC
13	A1	31	A8	49	DQ10	67	PRD1
14	A2	32	A9	50	DQ28	68	PRD2
15	A3	33	NC	51	DQ11	69	PRD3
16	A4	34	$\overline{\text{RAS2}}$	52	DQ29	70	PRD4
17	A5	35	DQ27	53	DQ12	71	NC
18	A6	36	DQ9	54	DQ30	72	Vss

GENERAL DESCRIPTION

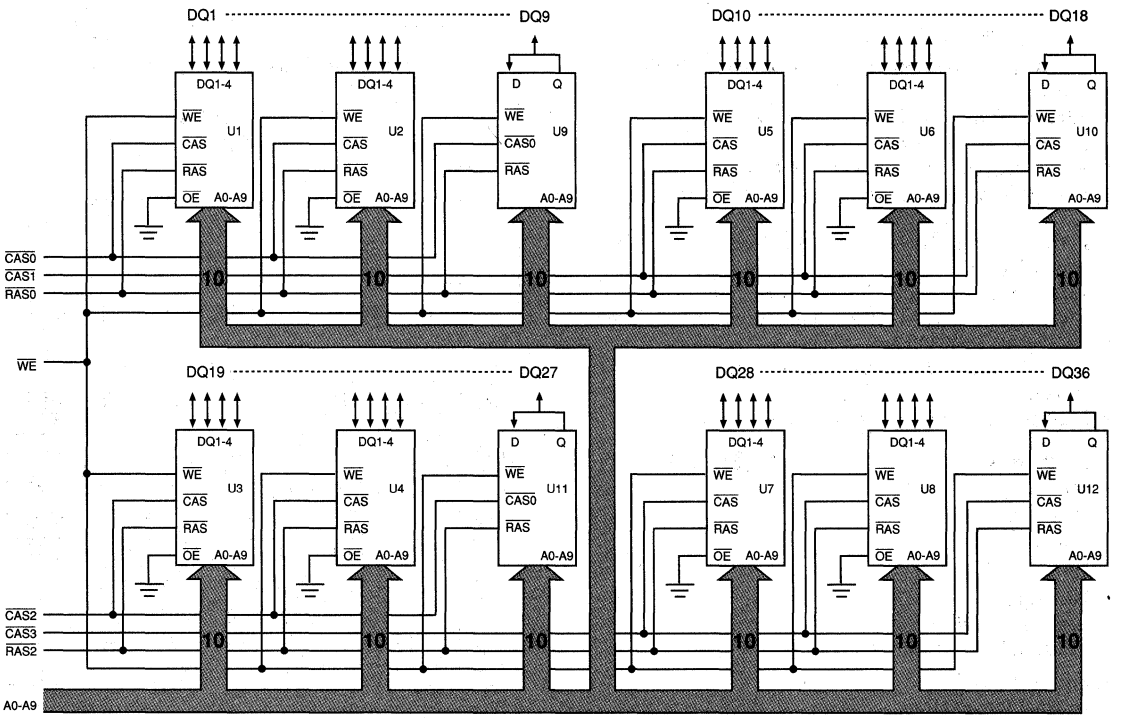
The MT12D136 is a randomly accessed solid-state memory containing 1,048,576 words organized in a x36 configuration. During READ or WRITE cycles, each bit is uniquely addressed through the 20 address bits, which are entered 10 bits (A0-A9) at a time. $\overline{\text{RAS}}$ is used to latch the first 10 bits and $\overline{\text{CAS}}$ the latter 10 bits. A READ or WRITE cycle is selected with the $\overline{\text{WE}}$ input. A logic HIGH on $\overline{\text{WE}}$ dictates READ mode while a logic LOW on $\overline{\text{WE}}$ dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of $\overline{\text{WE}}$ or $\overline{\text{CAS}}$, whichever occurs last. If $\overline{\text{WE}}$ goes LOW prior to $\overline{\text{CAS}}$ going LOW, the output pin(s) remain open (High-Z) until the next $\overline{\text{CAS}}$ cycle.

FAST PAGE MODE operations allow faster data operations (READ or WRITE) within a row-address (A0-A9) defined page boundary. The FAST PAGE MODE cycle is always initiated with a row address strobed-in by $\overline{\text{RAS}}$ followed by a column address strobed-in by $\overline{\text{CAS}}$. $\overline{\text{CAS}}$ may be toggled-in by holding $\overline{\text{RAS}}$ LOW and strobing-in different column addresses, thus executing faster memory cycles. Returning $\overline{\text{RAS}}$ HIGH terminates the FAST PAGE MODE operation.

Returning $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the $\overline{\text{RAS}}$ HIGH time. Memory cell data is retained in its correct state by maintaining power and executing any $\overline{\text{RAS}}$ cycle (READ, WRITE, $\overline{\text{RAS}}$-ONLY, $\overline{\text{CAS}}$-BEFORE-$\overline{\text{RAS}}$ or HIDDEN REFRESH) so that all 1,024 combinations of $\overline{\text{RAS}}$ addresses (A0-A9) are executed at least every 16ms (128ms on L-version), regardless of sequence.

NEW ■ DRAM MODULE

FUNCTIONAL BLOCK DIAGRAM



U1-U8 = MT4C4001JDJ
U9-U12 = MT4C1024DJ
or
U1-U8 = MT4C4001JDJ L (L-version)
U9-U12 = MT4C1024DJ L (L-version)

TRUTH TABLE

FUNCTION		RAS	CAS	WE	ADDRESSES		DATA IN/OUT
					^tR	^tC	DQ1-DQ36
Standby		H	H→X	X	X	X	High-Z
READ		L	L	H	ROW	COL	Data Out
EARLY-WRITE		L	L	L	ROW	COL	Data In
FAST-PAGE-MODE	1st Cycle	L	H→L	H	ROW	COL	Data Out
READ	2nd Cycle	L	H→L	H	n/a	COL	Data Out
FAST-PAGE-MODE	1st Cycle	L	H→L	L	ROW	COL	Data In
WRITE	2nd Cycle	L	H→L	L	n/a	COL	Data In
RAS-ONLY REFRESH		L	H	X	ROW	n/a	High-Z
HIDDEN	READ	L→H→L	L	H	ROW	COL	Data Out
REFRESH	WRITE	L→H→L	L	L	ROW	COL	Data In
CAS-BEFORE-RAS REFRESH		H→L	L	H	X	X	High-Z
BATTERY BACKUP REFRESH (L-version)		H→L	L	X	X	X	High-Z

PRESENCE DETECT

SYMBOL	-6	-7	-8
PRD1	Vss	Vss	Vss
PRD2	Vss	Vss	Vss
PRD3	NC	Vss	NC
PRD4	NC	NC	Vss

NEW ■ DRAM MODULE

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} ..... -1V to +7V
Operating Temperature, T_A (Ambient) ..... 0°C to +70°C
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation 12W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 2, 3, 6, 22) (0°C ≤ T_A ≤ 70°C; V_{CC} = 5V ±10%)

PARAMETER/CONDITION		SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage		V_{CC}	4.5	5.5	V	1
Input High (Logic 1) Voltage, All Inputs		V_{IH}	2.4	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, All Inputs		V_{IL}	-1.0	0.8	V	1
INPUT LEAKAGE CURRENT	$\overline{CAS0}$-$\overline{CAS3}$	I_{I1}	-6	6	µA	
Any Input 0V ≤ V_{IN} ≤ V_{CC}	A0-A9, $\overline{WE}$	I_{I2}	-24	24	µA	
(All other pins not under test = 0V) for each package input	$\overline{RAS0}$, $\overline{RAS2}$	I_{I3}	-12	12	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled, 0V ≤ V_{OUT} ≤ V_{CC}) for each package input	DQ1-DQ36	I_{OZ}	-10	10	µA	
OUTPUT LEVELS		V_{OH}	2.4		V	
Output High Voltage (I_{OUT} = -5mA)						
Output Low Voltage (I_{OUT} = 5mA)		V_{OL}		0.4	V	

PARAMETER/CONDITION	SYMBOL	MAX -6	MAX -7	MAX -8	UNITS	NOTES
STANDBY CURRENT: (TTL) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC1}	24	24	24	mA	
STANDBY CURRENT: (CMOS)	I_{CC2}	12	12	12	mA	
($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} -0.2V)		2.4	2.4	2.4	mA	24
OPERATING CURRENT: Random READ/WRITE Average power supply current	I_{CC3}	1240	1120	1000	mA	2, 22
($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC (MIN))		1220	1100	980	mA	2,22,24
OPERATING CURRENT: FAST PAGE MODE Average power supply current	I_{CC4}	920	800	680	mA	2, 22
($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: ^tPC = ^tPC (MIN))		900	780	660	mA	2,22,24
REFRESH CURRENT: $\overline{RAS}$-ONLY Average power supply current	I_{CC5}	1240	1120	1000	mA	2
($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}: ^tRC = ^tRC (MIN))		1220	1100	980	mA	2, 24
REFRESH CURRENT: $\overline{CAS}$-BEFORE-$\overline{RAS}$ Average power supply current	I_{CC6}	1240	1120	1000	mA	2, 19
($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC (MIN))		1220	1100	980	mA	2,19,24
REFRESH CURRENT: BATTERY BACKUP (BBU) Average power supply current during BATTERY BACKUP refresh: $\overline{CAS}$ = 0.2V or $\overline{CAS}$-BEFORE-$\overline{RAS}$ cycling; $\overline{RAS}$ = ^tRAS (MIN) to 300ns; $\overline{WE}$ = V_{CC} -0.2; A0-A9 and D_{IN} = V_{CC} -0.2V or 0.2V (D_{IN} may be left open), ^tRC = 125µs (1,024 rows at 125µs = 128ms)	I_{CC7}	3.2	3.2	3.2	mA	24

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A9	C_{I1}		77	pF	17
Input Capacitance: $\overline{WE}$	C_{I2}		101	pF	17
Input Capacitance: $\overline{RAS0}$, $\overline{RAS2}$	C_{I3}		50	pF	17
Input Capacitance: $\overline{CAS0}$, $\overline{CAS1}$, $\overline{CAS2}$, $\overline{CAS3}$	C_{I4}		25	pF	17
Input/Output Capacitance: DQ1-DQ36	C_{IO}		10	pF	17

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 3, 4, 5, 6, 7, 10, 11, 16, 21) ($0°C \le T_A \le 70°C$; V_{CC} = 5V ±10%)

AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	^tRC	110		130		150		ns	
READ-WRITE cycle time	^tRWC	n/a		n/a		n/a		ns	21
FAST-PAGE-MODE READ or WRITE cycle time	^tPC	40		40		45		ns	
FAST-PAGE-MODE READ-WRITE cycle time	^tPRWC	n/a		n/a		n/a		ns	21
Access time from $\overline{RAS}$	^tRAC		60		70		80	ns	8
Access time from $\overline{CAS}$	^tCAC		15		20		20	ns	9
Output Enable	^tOE		15		20		20	ns	
Access time from column address	^tAA		30		35		40	ns	
Access time from $\overline{CAS}$ precharge	^tCPA		35		40		45	ns	
$\overline{RAS}$ pulse width	^tRAS	60	100,000	70	100,000	80	100,000	ns	
$\overline{RAS}$ pulse width (FAST PAGE MODE)	^tRASP	60	100,000	70	100,000	80	100,000	ns	
$\overline{RAS}$ hold time	^tRSH	15		20		20		ns	
$\overline{RAS}$ precharge time	^tRP	40		50		60		ns	
$\overline{CAS}$ pulse width	^tCAS	15	100,000	20	100,000	20	100,000	ns	
$\overline{CAS}$ hold time	^tCSH	60		70		80		ns	
$\overline{CAS}$ precharge time	^tCPN	10		10		10		ns	18
$\overline{CAS}$ precharge time (FAST PAGE MODE)	^tCP	10		10		10		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	^tRCD	20	40	20	50	20	60	ns	13
$\overline{CAS}$ to $\overline{RAS}$ precharge time	^tCRP	10		10		10		ns	
Row address setup time	^tASR	0		0		0		ns	
Row address hold time	^tRAH	10		10		10		ns	
$\overline{RAS}$ to column address delay time	^tRAD	15	30	15	35	15	40	ns	23
Column address setup time	^tASC	0		0		0		ns	
Column address hold time	^tCAH	10		15		15		ns	
Column address hold time (referenced to $\overline{RAS}$)	^tAR	50		55		60		ns	
Column address to $\overline{RAS}$ lead time	^tRAL	30		35		40		ns	
Read command setup time	^tRCS	0		0		0		ns	
Read command hold time (referenced to $\overline{CAS}$)	^tRCH	0		0		0		ns	14
Read command hold time (referenced to $\overline{RAS}$)	^tRRH	0		0		0		ns	14

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

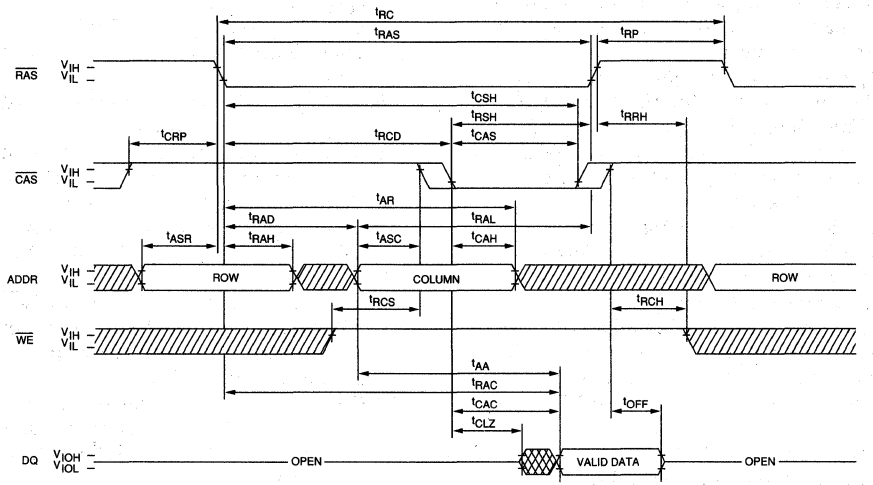
(Notes: 3, 4, 5, 6, 7, 10, 11, 16, 21) ($0°C \le T_A \le 70°C$; Vcc = 5V ±10%)

AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
$\overline{CAS}$ to output in Low-Z	tCLZ	0		0		0		ns	
Output buffer turn-off delay	tOFF	0	20	0	20	0	20	ns	12
$\overline{WE}$ command setup time	tWCS	0		0		0		ns	
Write command hold time	tWCH	10		15		15		ns	
Write command hold time (referenced to $\overline{RAS}$)	tWCR	45		55		60		ns	
Write command pulse width	tWP	10		15		15		ns	
Write command to $\overline{RAS}$ lead time	tRWL	15		20		20		ns	
Write command to $\overline{CAS}$ lead time	tCWL	15		20		20		ns	
Data-in setup time	tDS	0		0		0		ns	15
Data-in hold time	tDH	10		15		15		ns	15
Data-in hold time (referenced to $\overline{RAS}$)	tDHR	45		55		60		ns	
Transition time (rise or fall)	tT	3	50	3	50	3	50	ns	5, 16
Refresh period (1,024 cycles)	tREF		16/128		16/128		16/128	ms	3/24
$\overline{RAS}$ to $\overline{CAS}$ precharge time	tRPC	0		0		0		ns	
$\overline{CAS}$ setup time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	tCSR	10		10		10		ns	19
$\overline{CAS}$ hold time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	tCHR	15		15		15		ns	19
$\overline{WE}$ hold time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	tWRH	10		10		10		ns	
$\overline{WE}$ setup time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	tWRP	10		10		10		ns	
$\overline{WE}$ hold time (WCBR test cycle)	tWTH	10		10		10		ns	
$\overline{WE}$ setup time (WCBR test cycle)	tWTS	10		10		10		ns	

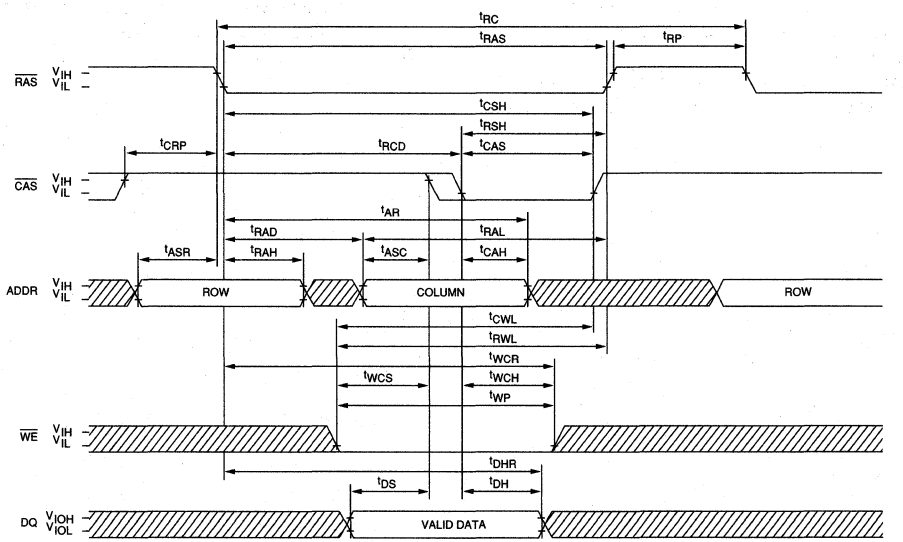
NOTES

1. All voltages referenced to V_{SS}.
2. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
3. An initial pause of 100µs is required after power-up followed by any eight $\overline{RAS}$ REFRESH cycles ($\overline{RAS}$-ONLY or CBR with $\overline{WE}$ HIGH) before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-up should be repeated any time the ^tREF refresh requirement is exceeded.
4. AC characteristics assume ^tT = 5ns.
5. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \le T_A \le 70°C$) is assured.
7. Measured with a load equivalent to two TTL gates and 100pF.
8. Assumes that $^tRCD < ^tRCD$ (MAX). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
9. Assumes that $^tRCD \ge ^tRCD$ (MAX).
10. If $\overline{CAS}$ = V_{IH}, data output is High-Z.
11. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
12. ^tOFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
13. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (MAX) limit, then access time is controlled exclusively by ^tCAC.
14. Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
15. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY-WRITE cycles.
16. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
17. This parameter is sampled. Capacitance is measured using MIL-STD-883C, Method 3012.1 (1 MHz AC, Vcc = 5V, DC bias = 2.4V @ 15mV RMS).
18. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, data-out (Q) will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer, $\overline{CAS}$ must be pulsed HIGH for ^tCP.
19. On-chip refresh and address counters are enabled.
20. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW.
21. LATE-WRITE, READ-WRITE or READ-MODIFY-WRITE cycles are not available due to $\overline{OE}$ being grounded on all 4 Meg DRAMs.
22. I_{CC} is dependent on cycle rates.
23. Operation within the ^tRAD (MAX) limit ensures that ^tRCD (MAX) can be met. ^tRAD (MAX) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (MAX) limit, then access time is controlled exclusively by ^tAA.
24. Applies to L-version only.

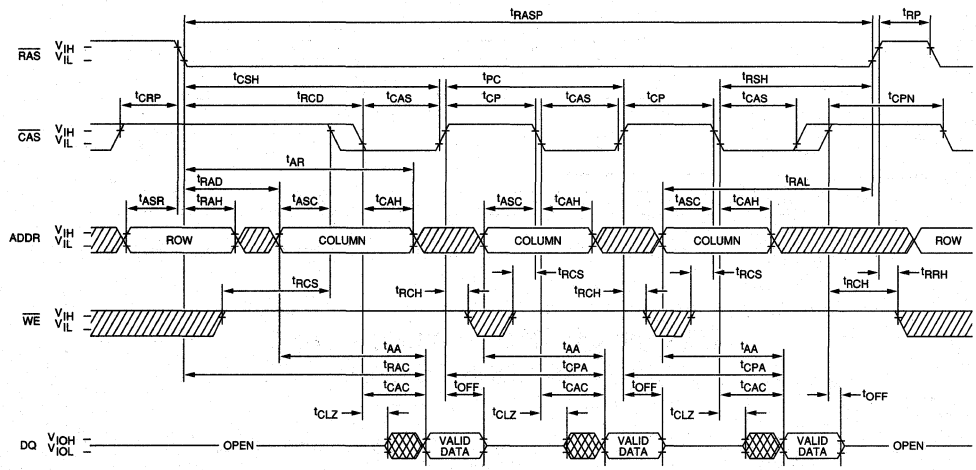
READ CYCLE



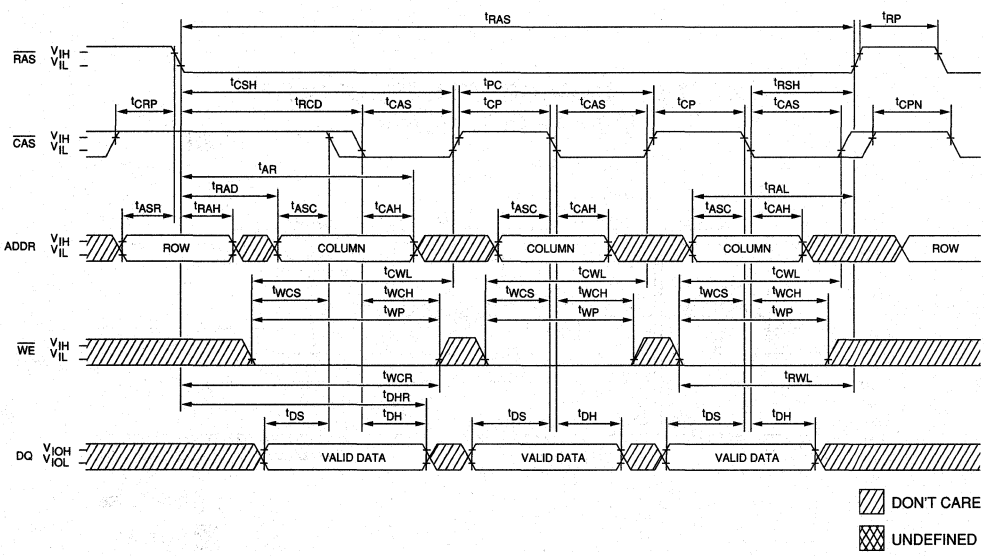
EARLY-WRITE CYCLE



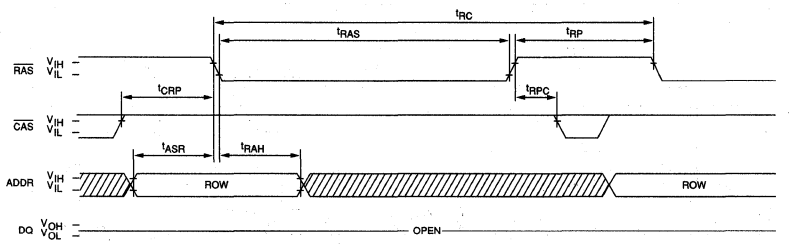
FAST-PAGE-MODE READ CYCLE



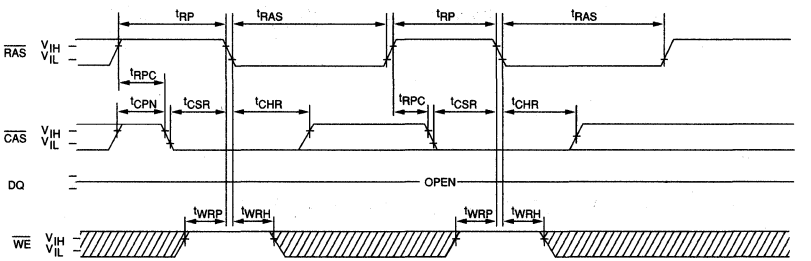
FAST-PAGE-MODE EARLY-WRITE CYCLE



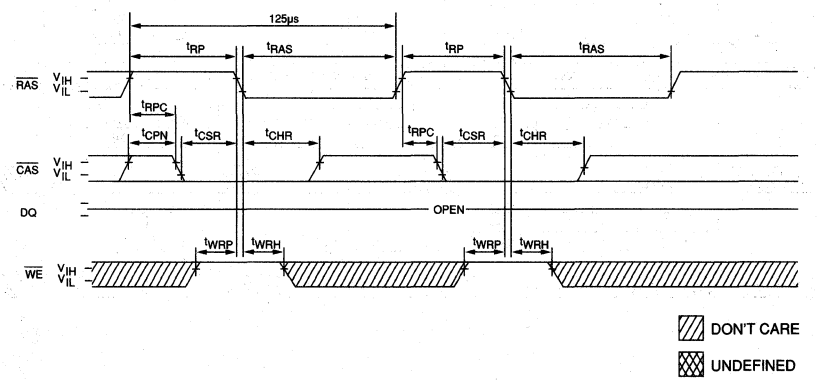
RAS-ONLY REFRESH CYCLE
(ADDR = A0-A9; WE = DON'T CARE)



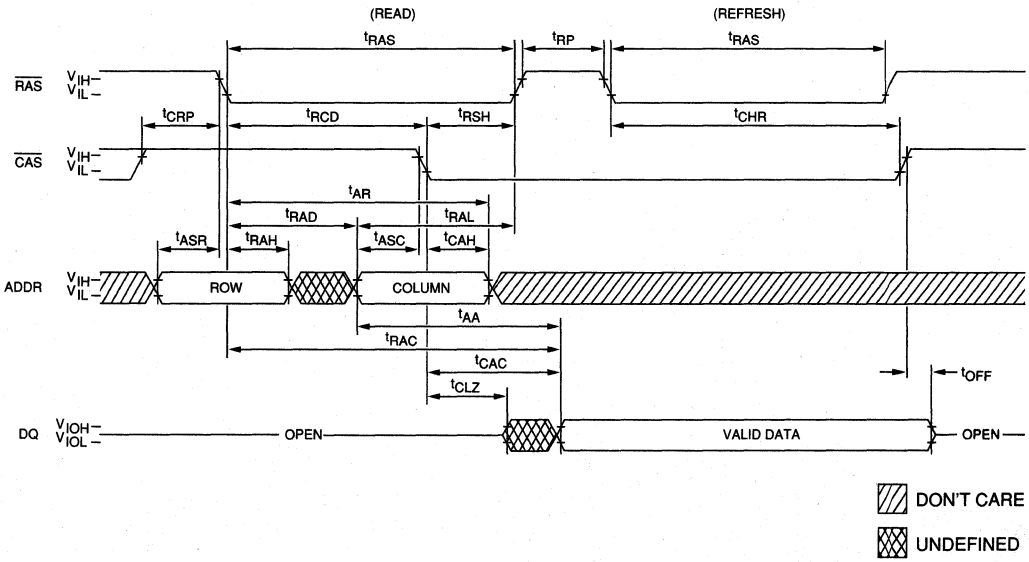
CAS-BEFORE-RAS REFRESH CYCLE
(A0-A9 = DON'T CARE)



BATTERY BACKUP REFRESH CYCLE [24]
(A0-A9 = DON'T CARE)



HIDDEN REFRESH CYCLE [20]
($\overline{WE}$ = HIGH)



DRAM MODULE

2 MEG x 36 DRAM

FAST PAGE MODE

FEATURES

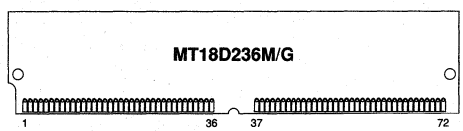
- Common $\overline{RAS}$ control per side pinout in a 72-pin single-in-line package
- High-performance, CMOS silicon-gate process.
- Single 5V ±10% power supply
- All device pins are fully TTL compatible
- Low power, 54mW standby; 2,052mW active, typical
- Refresh modes: $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$ (CBR) and HIDDEN
- 1,024-cycle refresh distributed across 16ms
- FAST PAGE MODE access cycle

OPTIONS MARKING

- Timing
  - 60ns access - 6
  - 70ns access - 7
  - 80ns access - 8
- Packages
  - Leadless 72-pin SIMM M
  - Leadless 72-pin SIMM (Gold) G
- Part Number Example: MT18D236G-6

PIN ASSIGNMENT (Top View)

72-Pin SIMM
(T-12)



PIN #	SYMBOL	PIN #	SYMBOL	PIN #	SYMBOL	PIN #	SYMBOL
1	Vss	19	NC	37	DQ18	55	DQ13
2	DQ1	20	DQ5	38	DQ36	56	DQ31
3	DQ19	21	DQ23	39	Vss	57	DQ14
4	DQ2	22	DQ6	40	$\overline{CAS0}$	58	DQ32
5	DQ20	23	DQ24	41	$\overline{CAS2}$	59	Vcc
6	DQ3	24	DQ7	42	$\overline{CAS3}$	60	DQ33
7	DQ21	25	DQ25	43	$\overline{CAS1}$	61	DQ15
8	DQ4	26	DQ8	44	$\overline{RAS0}$	62	DQ34
9	DQ22	27	DQ26	45	$\overline{RAS1}$	63	DQ16
10	Vcc	28	A7	46	NC	64	DQ35
11	NC	29	NC	47	$\overline{WE}$	65	DQ17
12	A0	30	Vcc	48	NC	66	NC
13	A1	31	A8	49	DQ10	67	PRD1
14	A2	32	A9	50	DQ28	68	PRD2
15	A3	33	$\overline{RAS1}$	51	DQ11	69	PRD3
16	A4	34	$\overline{RAS0}$	52	DQ29	70	PRD4
17	A5	35	DQ27	53	DQ12	71	NC
18	A6	36	DQ9	54	DQ30	72	Vss

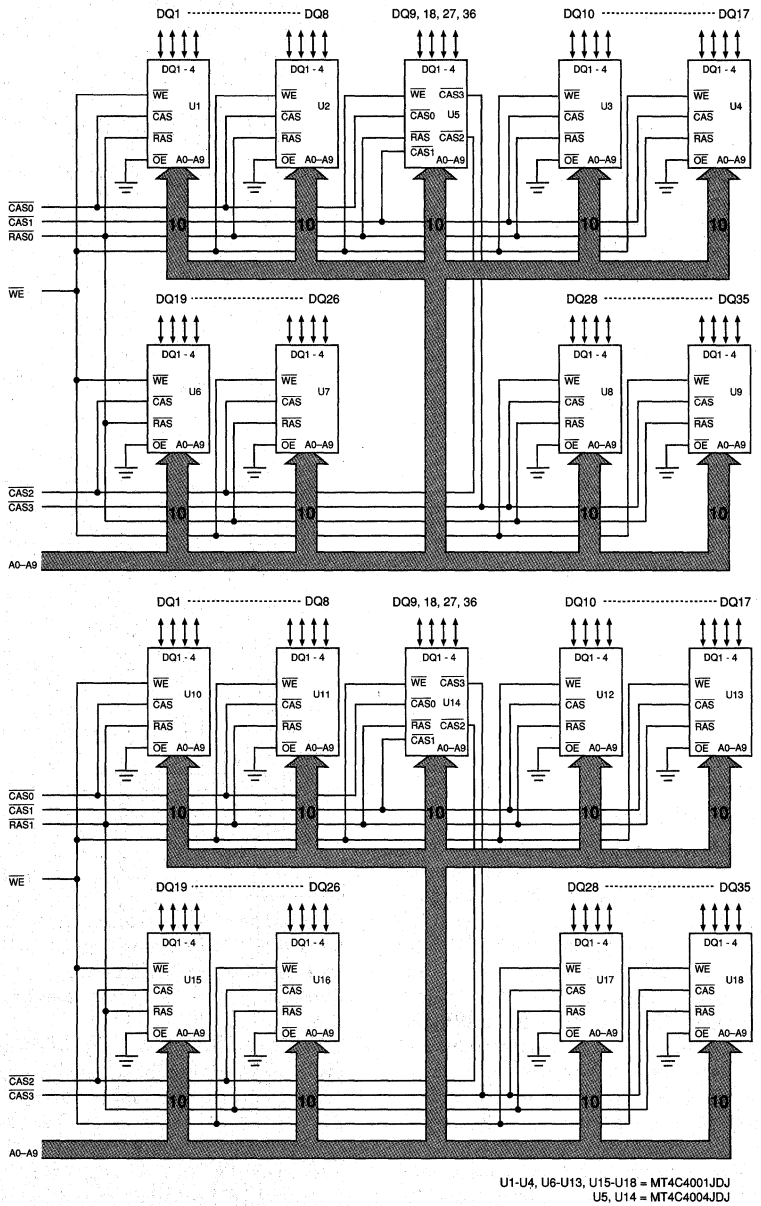
GENERAL DESCRIPTION

The MT18D236 is a randomly accessed solid-state memory containing 2,097,152 words organized in a x36 configuration. During READ or WRITE cycles, each bit is uniquely addressed through the 20 address bits which are entered 10 bits (A0-A9) at a time. $\overline{RAS}$ is used to latch the first 10 bits and $\overline{CAS}$ the latter 10 bits. READ or WRITE cycles are selected with the $\overline{WE}$ input. A logic HIGH on $\overline{WE}$ dictates READ mode while a logic LOW on $\overline{WE}$ dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. EARLY WRITE occurs when $\overline{WE}$ goes LOW prior to $\overline{CAS}$ going LOW, the output pin(s) remain open (High-Z) until the next $\overline{CAS}$ cycle.

FAST PAGE MODE operations allow faster data operations (READ or WRITE) within a row-address (A0-A9) defined page boundary. The FAST PAGE MODE cycle is always initiated with a row address strobed-in by $\overline{RAS}$ followed by a column address strobed-in by $\overline{CAS}$. $\overline{CAS}$ may be toggled-in by holding $\overline{RAS}$ LOW and strobing-in different column addresses, thus executing faster memory cycles. Returning $\overline{RAS}$ HIGH terminates the FAST PAGE MODE operation.

Returning $\overline{RAS}$ and $\overline{CAS}$ HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the $\overline{RAS}$ high time. Memory cell data is retained in its correct state by maintaining power and executing any $\overline{RAS}$ cycle (READ, WRITE, $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$ or HIDDEN REFRESH) so that all 1,024 combinations of $\overline{RAS}$ addresses (A0-A9) are executed at least every 16ms, regardless of sequence.

FUNCTIONAL BLOCK DIAGRAM



NOTE: Due to the use of a Quad $\overline{CAS}$ parity DRAM, $\overline{RAS0}$ is common to side 1 and $\overline{RAS1}$ is common to side 2.

TRUTH TABLE

FUNCTION		RAS	CAS	WE	ADDRESSES		DATA IN/OUT
					^tR	^tC	DQ1-DQ36
Standby		H	H→X	X	X	X	High-Z
READ		L	L	H	ROW	COL	Data Out
EARLY-WRITE		L	L	L	ROW	COL	Data In
FAST-PAGE-MODE	1st Cycle	L	H→L	H	ROW	COL	Data Out
READ	2nd Cycle	L	H→L	H	n/a	COL	Data Out
FAST-PAGE-MODE	1st Cycle	L	H→L	L	ROW	COL	Data In
WRITE	2nd Cycle	L	H→L	L	n/a	COL	Data In
RAS-ONLY REFRESH		L	H	X	ROW	n/a	High-Z
HIDDEN	READ	L→H→L	L	H	ROW	COL	Data Out
REFRESH	WRITE	L→H→L	L	L	ROW	COL	Data In
CAS-BEFORE-RAS REFRESH		H→L	L	H	X	X	High-Z

PRESENCE DETECT

SYMBOL	-6	-7	-8
PRD1	NC	NC	NC
PRD2	NC	NC	NC
PRD3	NC	Vss	NC
PRD4	NC	NC	Vss

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} ..... -1V to +7V
Operating Temperature, T_A (Ambient) ..... 0°C to +70°C
Storage Temperature (Plastic) ..... -55°C to +125°C
Power Dissipation 18W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 2, 3, 6, 23) (0°C ≤ T_A ≤ 70°C; V_{CC} = 5V ±10%)

PARAMETER/CONDITION		SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage		V_{CC}	4.5	5.5	V	1
Input High (Logic 1) Voltage, All Inputs		V_{IH}	2.4	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, All Inputs		V_{IL}	-1.0	0.8	V	1
INPUT LEAKAGE CURRENT	$\overline{CAS0}$-$\overline{CAS3}$	I_{I1}	-12	12	µA	
Any Input: 0V ≤ V_{IN} ≤ V_{CC}	A0-A9, $\overline{WE}$	I_{I2}	-36	36	µA	
(All other pins not under test = 0V) For each package input	$\overline{RAS0}$, $\overline{RAS1}$	I_{I3}	-18	18	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled, 0V ≤ V_{OUT} ≤ V_{CC}) For each package input	DQ1-DQ36	I_{OZ}	-20	20	µA	
OUTPUT LEVELS		V_{OH}	2.4		V	
Output High Voltage (I_{OUT} = -5mA)						
Output Low Voltage (I_{OUT} = 5mA)		V_{OL}		0.4	V	

		MAX				
PARAMETER/CONDITION	SYMBOL	-6	-7	-8	UNITS	NOTES
STANDBY CURRENT: (TTL) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC1}	36	36	36	mA	
STANDBY CURRENT: (CMOS) ($\overline{RAS}$ = $\overline{CAS}$ = Other Inputs = V_{CC} -0.2V)	I_{CC2}	18	18	18	mA	
OPERATING CURRENT: Random READ/WRITE Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC (MIN))	I_{CC3}	1008	918	828	mA	2, 23
OPERATING CURRENT: FAST PAGE MODE Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: ^tPC = ^tPC (MIN))	I_{CC4}	738	648	558	mA	2, 23
REFRESH CURRENT: $\overline{RAS}$-ONLY Average power supply current ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}: ^tRC = ^tRC (MIN))	I_{CC5}	1008	918	828	mA	2
REFRESH CURRENT: $\overline{CAS}$-BEFORE-$\overline{RAS}$ Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC (MIN))	I_{CC6}	1008	918	828	mA	2, 19

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A9	C_{I1}		115	pF	17
Input Capacitance: $\overline{WE}$	C_{I2}		151	pF	17
Input Capacitance: $\overline{RAS0}$, $\overline{RAS1}$	C_{I3}		76	pF	17
Input Capacitance: $\overline{CAS0}$, $\overline{CAS1}$, $\overline{CAS2}$, $\overline{CAS3}$	C_{I4}		50	pF	17
Input/Output Capacitance: DQ1-DQ36	C_{IO}		20	pF	17

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 3, 4, 5, 6, 7, 10, 11, 16, 21) ($0°C \le T_A \le 70°C$; V_{CC} = 5V ±10%)

AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	^tRC	110		130		150		ns	
READ-WRITE cycle time	^tRWC	n/a		n/a		n/a		ns	21
FAST-PAGE-MODE READ or WRITE cycle time	^tPC	40		40		45		ns	
FAST-PAGE-MODE READ-WRITE cycle time	^tPRWC	n/a		n/a		n/a		ns	21
Access time from $\overline{RAS}$	^tRAC		60		70		80	ns	8
Access time from $\overline{CAS}$	^tCAC		15		20		20	ns	9
Output Enable	^tOE		15		20		20	ns	
Access time from column address	^tAA		30		35		40	ns	
Access time from $\overline{CAS}$ precharge	^tCPA		35		40		45	ns	
$\overline{RAS}$ pulse width	^tRAS	60	100,000	70	100,000	80	100,000	ns	
$\overline{RAS}$ pulse width (FAST PAGE MODE)	^tRASP	60	100,000	70	100,000	80	100,000	ns	
$\overline{RAS}$ hold time	^tRSH	15		20		20		ns	
$\overline{RAS}$ precharge time	^tRP	40		50		60		ns	
$\overline{CAS}$ pulse width	^tCAS	15	100,000	20	100,000	20	100,000	ns	
$\overline{CAS}$ hold time	^tCSH	60		70		80		ns	
$\overline{CAS}$ precharge time	^tCPN	10		10		10		ns	18, 22
$\overline{CAS}$ precharge time (FAST PAGE MODE)	^tCP	10		10		10		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	^tRCD	20	45	20	50	20	60	ns	13
$\overline{CAS}$ to $\overline{RAS}$ precharge time	^tCRP	10		10		10		ns	
Row address setup time	^tASR	0		0		0		ns	
Row address hold time	^tRAH	10		10		10		ns	
$\overline{RAS}$ to column address delay time	^tRAD	15	30	15	35	15	40	ns	24
Column address setup time	^tASC	0		0		0		ns	
Column address hold time	^tCAH	10		15		15		ns	
Column address hold time (referenced to $\overline{RAS}$)	^tAR	50		55		60		ns	
Column address to $\overline{RAS}$ lead time	^tRAL	30		35		40		ns	
Read command setup time	^tRCS	0		0		0		ns	
Read command hold time (referenced to $\overline{CAS}$)	^tRCH	0		0		0		ns	14
Read command hold time (referenced to $\overline{RAS}$)	^tRRH	0		0		0		ns	14

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

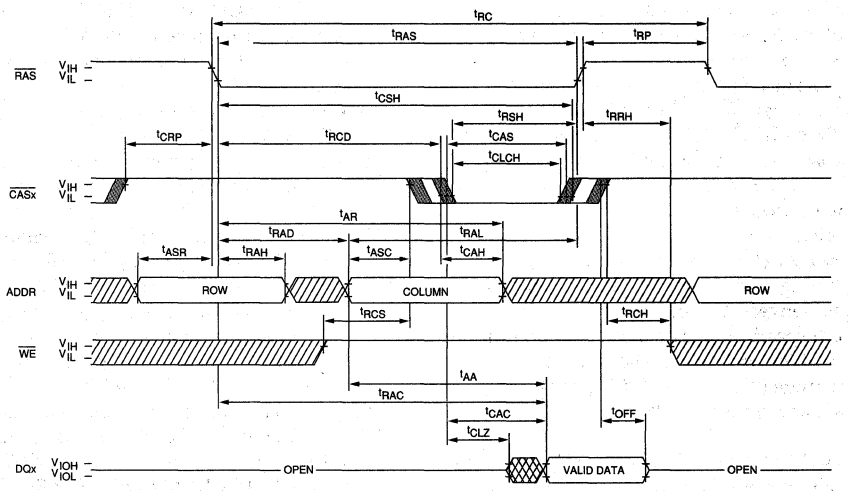
(Notes: 3, 4, 5, 6, 7, 10, 11, 16, 21) ($0°C \le T_A \le 70°C$; Vcc = 5V ±10%)

AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
$\overline{CAS}$ to output in Low-Z	tCLZ	0		0		0		ns	
Output buffer turn-off delay	tOFF	0	15	0	20	0	20	ns	12
$\overline{WE}$ command setup time	tWCS	0		0		0		ns	
Write command hold time	tWCH	10		15		15		ns	
Write command hold time (referenced to $\overline{RAS}$)	tWCR	45		55		60		ns	
Write command pulse width	tWP	10		15		15		ns	
Write command to $\overline{RAS}$ lead time	tRWL	15		20		20		ns	
Write command to $\overline{CAS}$ lead time	tCWL	15		20		20		ns	
Data-in setup time	tDS	0		0		0		ns	15
Data-in hold time	tDH	10		15		15		ns	15
Data-in hold time (referenced to $\overline{RAS}$)	tDHR	45		55		60		ns	
Transition time (rise or fall)	tT	3	50	3	50	3	50	ns	5, 16
Refresh period (1,024 cycles)	tREF		16		16		16	ms	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	tRPC	0		0		0		ns	
$\overline{CAS}$ setup time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	tCSR	10		10		10		ns	19
$\overline{CAS}$ hold time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	tCHR	15		15		15		ns	19
$\overline{WE}$ hold time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	tWRH	10		10		10		ns	
$\overline{WE}$ setup time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	tWRP	10		10		10		ns	
$\overline{WE}$ hold time (WCBR test cycle)	tWTH	10		10		10		ns	
$\overline{WE}$ setup time (WCBR test cycle)	tWTS	10		10		10		ns	
Last $\overline{CAS}$ going LOW to first $\overline{CAS}$ to return HIGH	tCLCH	10		10		10		ns	

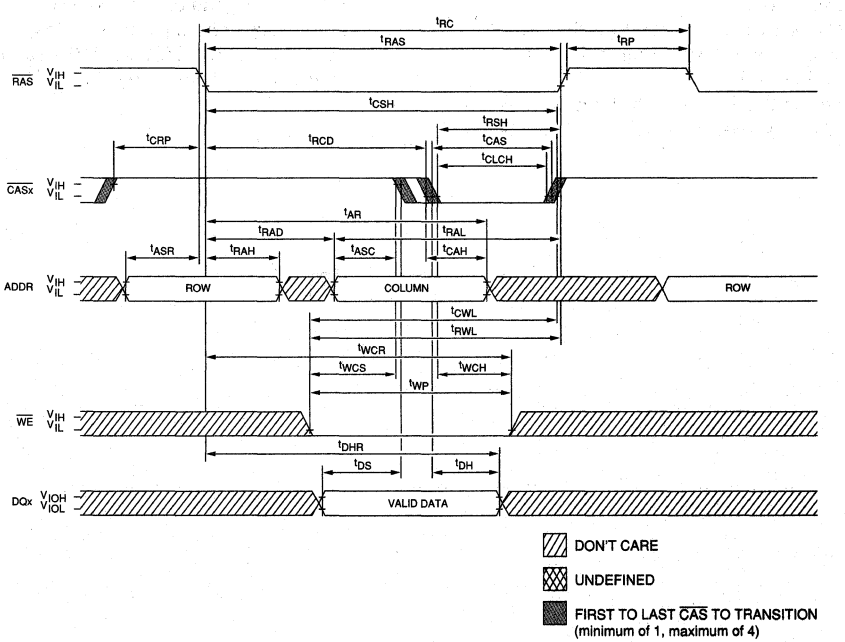
NOTES

1. All voltages referenced to V_{SS}.
2. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
3. An initial pause of 100µs is required after power-up followed by any eight $\overline{RAS}$ REFRESH cycles ($\overline{RAS}$-ONLY or CBR with $\overline{WE}$ HIGH) before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-up should be repeated any time the ^tREF refresh requirement is exceeded.
4. AC characteristics assume ^tT = 5ns.
5. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \le T_A \le 70°C$) is assured.
7. Measured with a load equivalent to two TTL gates and 100pF.
8. Assumes that $^tRCD < ^tRCD$ (MAX). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
9. Assumes that $^tRCD \ge ^tRCD$ (MAX).
10. If $\overline{CAS}$ = V_{IH}, data output is High-Z.
11. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
12. ^tOFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
13. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (MAX) limit, then access time is controlled exclusively by ^tCAC.
14. Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
15. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY-WRITE cycles.
16. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
17. This parameter is sampled. Capacitance is measured using MIL-STD-883C, Method 3012.1 (1 MHz AC, Vcc = 5V, DC bias = 2.4V @ 15mV RMS).
18. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, data-out (Q) will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer, $\overline{CAS}$ must be pulsed HIGH for ^tCP.
19. On-chip refresh and address counters are enabled.
20. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW.
21. LATE-WRITE, READ-WRITE or READ-MODIFY-WRITE cycles are not available due to $\overline{OE}$ being grounded on U1-U18.
22. Last falling $\overline{CAS}$x edge to first rising $\overline{CAS}$x edge.
23. I_{CC} is dependent on cycle rates.
24. Operation within the ^tRAD (MAX) limit ensures that ^tRCD (MAX) can be met. ^tRAD (MAX) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (MAX) limit, then access time is controlled exclusively by ^tAA.

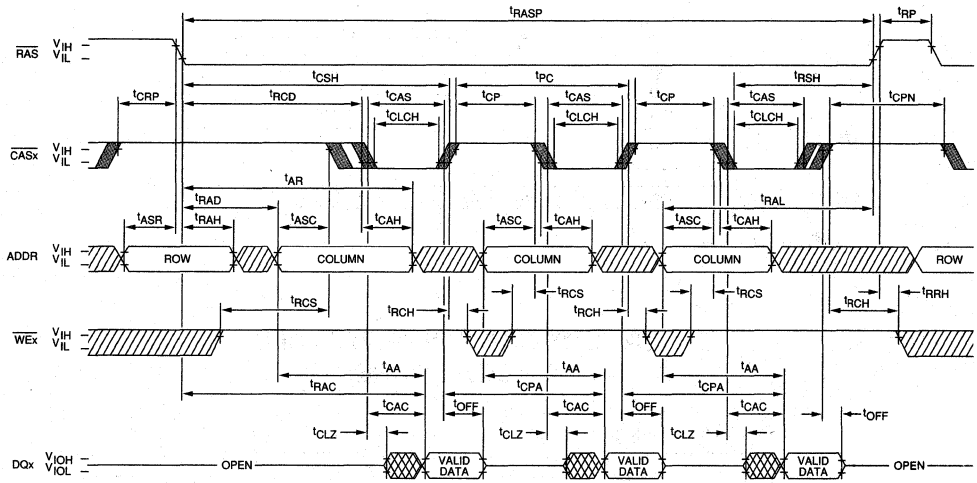
READ CYCLE



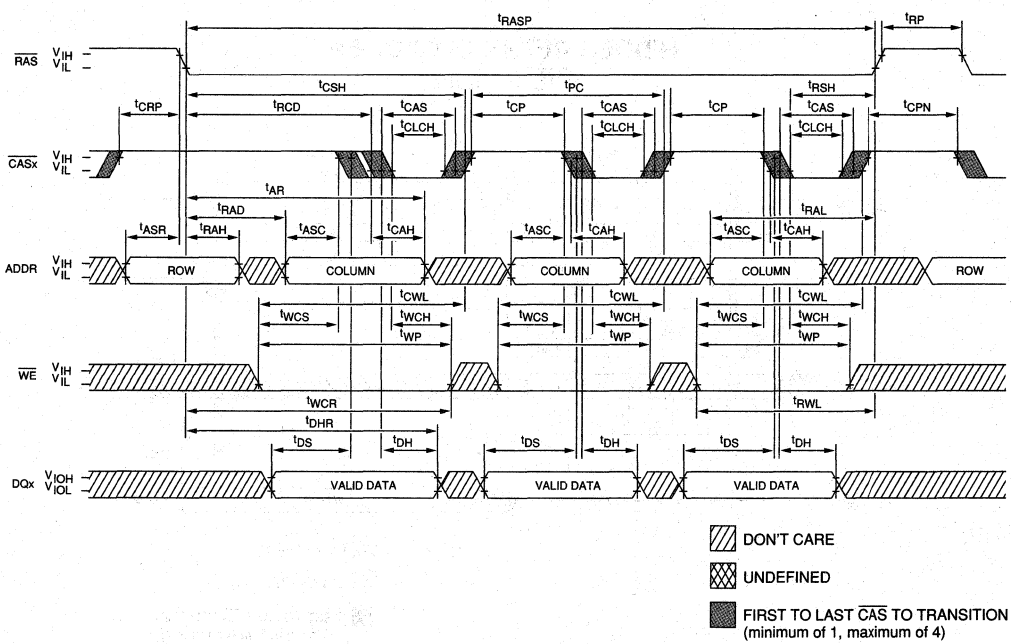
EARLY-WRITE CYCLE



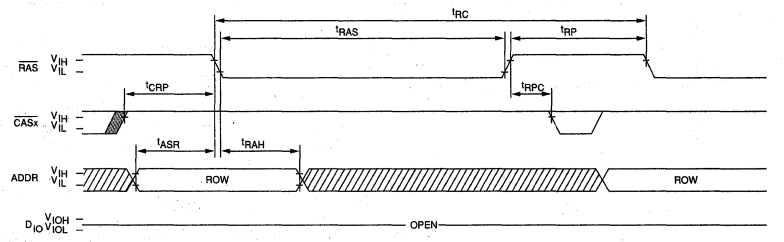
FAST-PAGE-MODE READ CYCLE



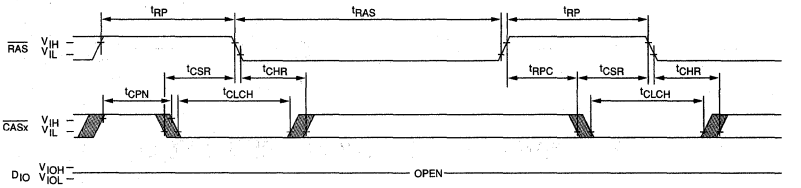
FAST-PAGE-MODE EARLY-WRITE CYCLE



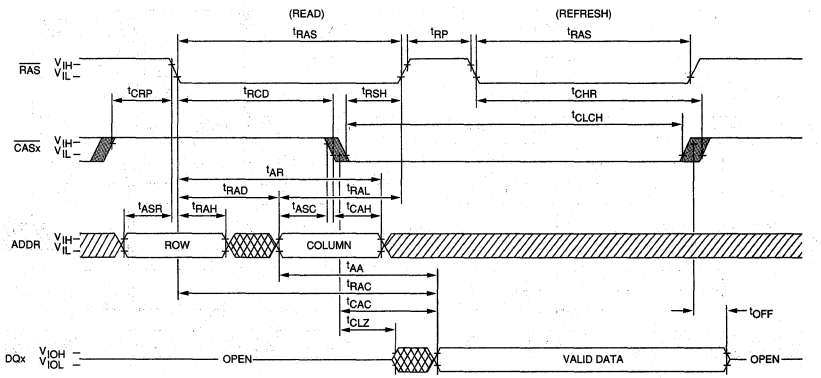
RAS-ONLY REFRESH CYCLE
(ADDR = A0-A9; WE = DON'T CARE)



CAS-BEFORE-RAS REFRESH CYCLE
(A0-A9 = DON'T CARE)



HIDDEN REFRESH CYCLE [20]
(WE = HIGH)



DON'T CARE

UNDEFINED

FIRST TO LAST CAS TO TRANSITION
(minimum of 1, maximum of 4)

)RAM MODULE

2 MEG x 36, 4 MEG x 18

FAST PAGE MODE (MT24D236)
LOW POWER,
EXTENDED REFRESH (MT24D236 L)

NEW DRAM MODULE

EATURES

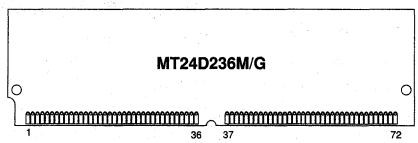
- Industry standard pinout in a 72-pin single-in-line package
- High-performance, CMOS silicon-gate process
- Single 5V ±10% power supply
- All device pins are fully TTL compatible
- Low power, 72mW (18.4mW L-version) standby; 2,536mW active, typical
- Refresh modes: $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$ (CBR) and HIDDEN
- 1,024-cycle refresh distributed across 16ms or 1,024-cycle extended refresh distributed across 128ms
- FAST PAGE MODE access cycle
- Low CMOS standby current, 4.8mA maximum (L-version)
- Multiple $\overline{RAS}$ lines allow x18 or x36 width

)PTIONS	MARKING
Timing	
60ns access	- 6
70ns access	- 7
80ns access	- 8
Packages	
Leadless 72-pin SIMM	M
Leadless 72-pin SIMM (Gold)	G
Power/Refresh	
Normal Power/16ms	Blank
Low Power/128ms	L

Part Number Example: MT24D236GL-6

PIN ASSIGNMENT (Top View)

72-Pin SIMM
(T-20)



PIN #	SYMBOL	PIN #	SYMBOL	PIN #	SYMBOL	PIN #	SYMBOL
1	Vss	19	NC	37	DQ18	55	DQ13
2	DQ1	20	DQ5	38	DQ36	56	DQ31
3	DQ19	21	DQ23	39	Vss	57	DQ14
4	DQ2	22	DQ6	40	$\overline{CAS0}$	58	DQ32
5	DQ20	23	DQ24	41	$\overline{CAS2}$	59	Vcc
6	DQ3	24	DQ7	42	$\overline{CAS3}$	60	DQ33
7	DQ21	25	DQ25	43	$\overline{CAS1}$	61	DQ15
8	DQ4	26	DQ8	44	$\overline{RAS0}$	62	DQ34
9	DQ22	27	DQ26	45	$\overline{RAS1}$	63	DQ16
10	Vcc	28	A7	46	NC	64	DQ35
11	NC	29	NC	47	$\overline{WE}$	65	DQ17
12	A0	30	Vcc	48	NC	66	NC
13	A1	31	A8	49	DQ10	67	PRD1
14	A2	32	A9	50	DQ28	68	PRD2
15	A3	33	$\overline{RAS3}$	51	DQ11	69	PRD3
16	A4	34	$\overline{RAS2}$	52	DQ29	70	PRD4
17	A5	35	DQ27	53	DQ12	71	NC
18	A6	36	DQ9	54	DQ30	72	Vss

ENERAL DESCRIPTION

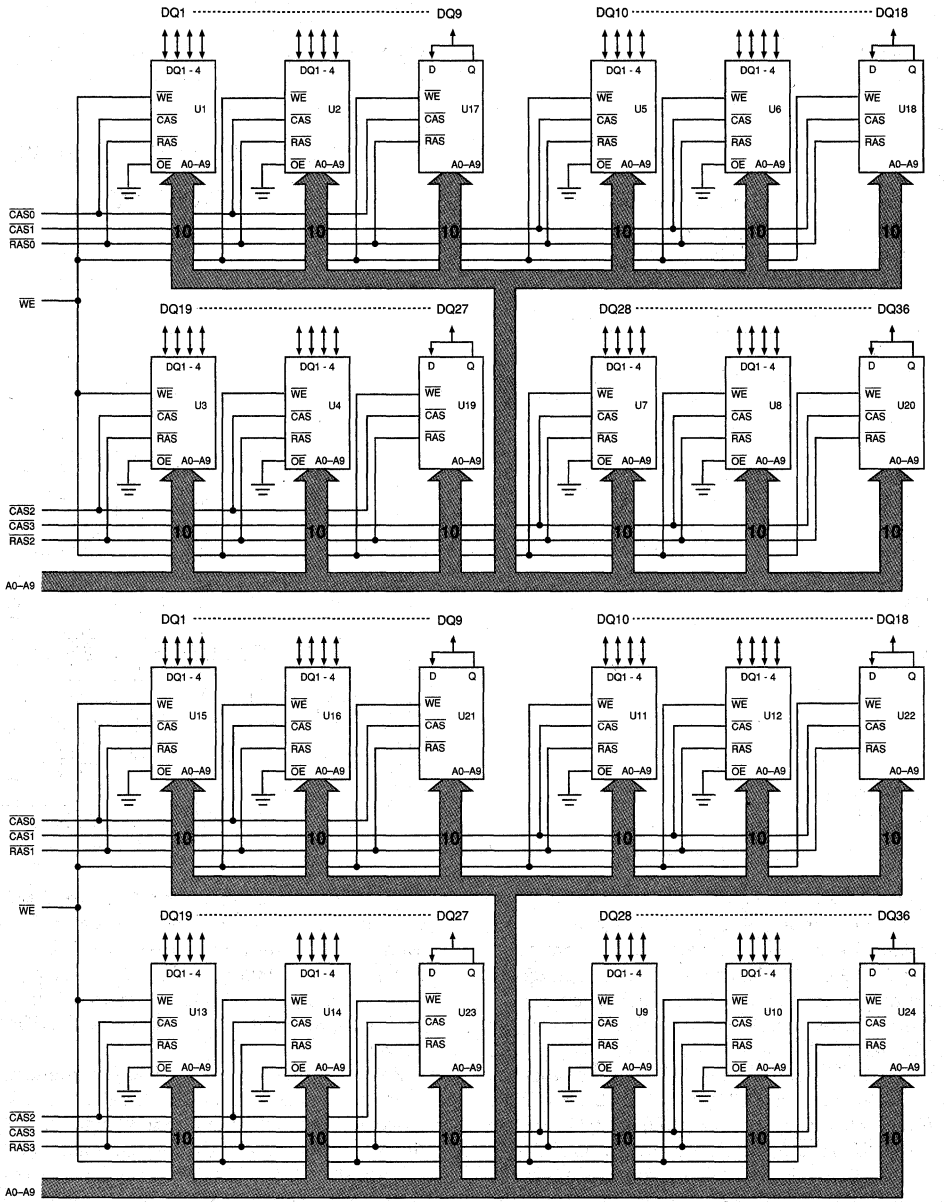
The MT24D236 is a randomly accessed solid-state memory ntaining 2,097,152 words organized in a x36 configura-)n. During READ or WRITE cycles, each bit is uniquely .dressed through the 20 address bits, which are entered 10 :s (A0-A9) at a time. $\overline{RAS}$ is used to latch the first 10 bits d $\overline{CAS}$ the latter 10 bits. A READ or WRITE cycle is lected with the $\overline{WE}$ input. A logic HIGH on $\overline{WE}$ dictates :AD mode while a logic LOW on $\overline{WE}$ dictates WRITE)de. During a WRITE cycle, data-in (D) is latched by the ling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. EARLY RITE occurs when $\overline{WE}$ goes LOW prior to $\overline{CAS}$ going)W, and the output pin(s) remain open (High-Z) until the xt $\overline{CAS}$ cycle.

FAST PAGE MODE operations allow faster data opera-)ns (READ or WRITE) within a row-address (A0-A9) defined page boundary. The FAST PAGE MODE cycle is always initiated with a row address strobed-in by $\overline{RAS}$ followed by a column address strobed-in by $\overline{CAS}$. $\overline{CAS}$ may be toggled-in by holding $\overline{RAS}$ LOW and strobing-in different column addresses, thus executing faster memory cycles. Returning $\overline{RAS}$ HIGH terminates the FAST PAGE MODE operation.

Returning $\overline{RAS}$ and $\overline{CAS}$ HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the $\overline{RAS}$ HIGH time. Memory cell data is retained in its correct state by maintaining power and executing any $\overline{RAS}$ cycle (READ, WRITE, $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$ or HIDDEN REFRESH) so that all 1,024 combinations of $\overline{RAS}$ addresses (A0-A9) are executed at least every 16ms (128ms on L-version), regardless of sequence.

NEW DRAM MODULE

FUNCTIONAL BLOCK DIAGRAM



U1-U16 = MT4C4001JDJ
U17-U24 = MT4C1024DJ
or
U1-U16 = MT4C4001JDJ L (L-version)
U17-U24 = MT4C1024DJ L (L-version)

TRUTH TABLE

FUNCTION		RAS	CAS	WE	ADDRESSES		DATA IN/OUT
					^tR	^tC	DQ1-DQ36
Standby		H	H→X	X	X	X	High-Z
READ		L	L	H	ROW	COL	Data Out
EARLY-WRITE		L	L	L	ROW	COL	Data In
FAST-PAGE-MODE	1st Cycle	L	H→L	H	ROW	COL	Data Out
READ	2nd Cycle	L	H→L	H	n/a	COL	Data Out
FAST-PAGE-MODE	1st Cycle	L	H→L	L	ROW	COL	Data In
WRITE	2nd Cycle	L	H→L	L	n/a	COL	Data In
RAS-ONLY REFRESH		L	H	X	ROW	n/a	High-Z
HIDDEN	READ	L→H→L	L	H	ROW	COL	Data Out
REFRESH	WRITE	L→H→L	L	L	ROW	COL	Data In
CAS-BEFORE-RAS REFRESH		H→L	L	H	X	X	High-Z
BATTERY BACKUP REFRESH (L-version)		H→L	L	X	X	X	High-Z

PRESENCE DETECT

SYMBOL	-6	-7	-8
PRD1	NC	NC	NC
PRD2	NC	NC	NC
PRD3	NC	Vss	NC
PRD4	NC	NC	Vss

NEW ■ DRAM MODULE

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} ..... -1V to +7V
Operating Temperature, T_A (Ambient) ..... 0°C to +70°C
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation 24W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 2, 3, 6, 22) (0°C ≤ T_A ≤ 70°C; V_{CC} = 5V ±10%)

PARAMETER/CONDITION		SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage		V_{CC}	4.5	5.5	V	1
Input High (Logic 1) Voltage, All Inputs		V_{IH}	2.4	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, All Inputs		V_{IL}	-1.0	0.8	V	1
INPUT LEAKAGE CURRENT	$\overline{CAS0}$-$\overline{CAS3}$	I_{I1}	-12	12	µA	
Any Input: 0V ≤ V_{IN} ≤ V_{CC}	A0-A9, $\overline{WE}$	I_{I2}	-48	48	µA	
(All other pins not under test = 0V) for each package input	$\overline{RAS0}$-$\overline{RAS3}$	I_{I3}	-12	12	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled, 0V ≤ V_{OUT} ≤ V_{CC}) for each package input	DQ1-DQ36	I_{OZ}	-10	10	µA	
OUTPUT LEVELS		V_{OH}	2.4		V	
Output High Voltage (I_{OUT} = -5mA)						
Output Low Voltage (I_{OUT} = 5mA)		V_{OL}		0.4	V	

PARAMETER/CONDITION	SYMBOL	MAX -6	MAX -7	MAX -8	UNITS	NOTES
STANDBY CURRENT: (TTL) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC1}	48	48	48	mA	
STANDBY CURRENT: (CMOS)	I_{CC2}	24	24	24	mA	
($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} -0.2V)		4.8	4.8	4.8	mA	24
OPERATING CURRENT: Random READ/WRITE Average power supply current	I_{CC3}	1264	1144	1024	mA	2, 22
($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC (MIN))		1225	1105	985	mA	2,22,24
OPERATING CURRENT: FAST PAGE MODE Average power supply current	I_{CC4}	944	824	704	mA	2, 22
($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: ^tPC = ^tPC (MIN))		905	785	665	mA	2,22,24
REFRESH CURRENT: $\overline{RAS}$-ONLY Average power supply current	I_{CC5}	1264	1144	1024	mA	2
($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}: ^tRC = ^tRC (MIN))		1225	1105	985	mA	2, 24
REFRESH CURRENT: $\overline{CAS}$-BEFORE-$\overline{RAS}$ Average power supply current	I_{CC6}	1264	1144	1024	mA	2, 19
($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC (MIN))		1225	1105	985	mA	2,19,24
REFRESH CURRENT: BATTERY BACKUP (BBU) Average power supply current during BATTERY BACKUP refresh: $\overline{CAS}$ = 0.2V or $\overline{CAS}$-BEFORE-$\overline{RAS}$ cycling; $\overline{RAS}$ = ^tRAS (MIN) to 300ns; $\overline{WE}$ = V_{CC} -0.2V; A0-A9 and D_{IN} = V_{CC} -0.2V or 0.2V (D_{IN} may be left open), ^tRC = 125µs (1,024 rows at 125µs = 128ms)	I_{CC7}	6.4	6.4	6.4	mA	24

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A9	C_{I1}		154	pF	17
Input Capacitance: $\overline{WE}$	C_{I2}		202	pF	17
Input Capacitance: $\overline{RAS0}$, $\overline{RAS1}$, $\overline{RAS2}$, $\overline{RAS3}$	C_{I3}		50	pF	17
Input Capacitance: $\overline{CAS0}$, $\overline{CAS1}$, $\overline{CAS2}$, $\overline{CAS3}$	C_{I4}		50	pF	17
Input/Output Capacitance: DQ1-DQ36	C_{IO}		20	pF	17

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 3, 4, 5, 6, 7, 10, 11, 16, 21) ($0°C \le T_A \le 70°C$; $V_{CC} = 5V \pm 10\%$)

AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	^tRC	110		130		150		ns	
READ-WRITE cycle time	^tRWC	n/a		n/a		n/a		ns	21
FAST-PAGE-MODE READ or WRITE cycle time	^tPC	40		40		45		ns	
FAST-PAGE-MODE READ-WRITE cycle time	^tPRWC	n/a		n/a		n/a		ns	21
Access time from $\overline{RAS}$	^tRAC		60		70		80	ns	8
Access time from $\overline{CAS}$	^tCAC		15		20		20	ns	9
Output Enable	^tOE		15		20		20	ns	
Access time from column address	^tAA		30		35		40	ns	
Access time from $\overline{CAS}$ precharge	^tCPA		35		40		45	ns	
$\overline{RAS}$ pulse width	^tRAS	60	100,000	70	100,000	80	100,000	ns	
$\overline{RAS}$ pulse width (FAST PAGE MODE)	^tRASP	60	100,000	70	100,000	80	100,000	ns	
$\overline{RAS}$ hold time	^tRSH	15		20		20		ns	
$\overline{RAS}$ precharge time	^tRP	40		50		60		ns	
$\overline{CAS}$ pulse width	^tCAS	15	100,000	20	100,000	20	100,000	ns	
$\overline{CAS}$ hold time	^tCSH	60		70		80		ns	
$\overline{CAS}$ precharge time	^tCPN	10		10		10		ns	18
$\overline{CAS}$ precharge time (FAST PAGE MODE)	^tCP	10		10		10		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	^tRCD	20	40	20	50	20	60	ns	13
$\overline{CAS}$ to $\overline{RAS}$ precharge time	^tCRP	10		10		10		ns	
Row address setup time	^tASR	0		0		0		ns	
Row address hold time	^tRAH	10		10		10		ns	
$\overline{RAS}$ to column address delay time	^tRAD	15	30	15	35	15	40	ns	23
Column address setup time	^tASC	0		0		0		ns	
Column address hold time	^tCAH	10		15		15		ns	
Column address hold time (referenced to $\overline{RAS}$)	^tAR	50		55		60		ns	
Column address to $\overline{RAS}$ lead time	^tRAL	30		35		40		ns	
Read command setup time	^tRCS	0		0		0		ns	
Read command hold time (referenced to $\overline{CAS}$)	^tRCH	0		0		0		ns	14
Read command hold time (referenced to $\overline{RAS}$)	^tRRH	0		0		0		ns	14

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

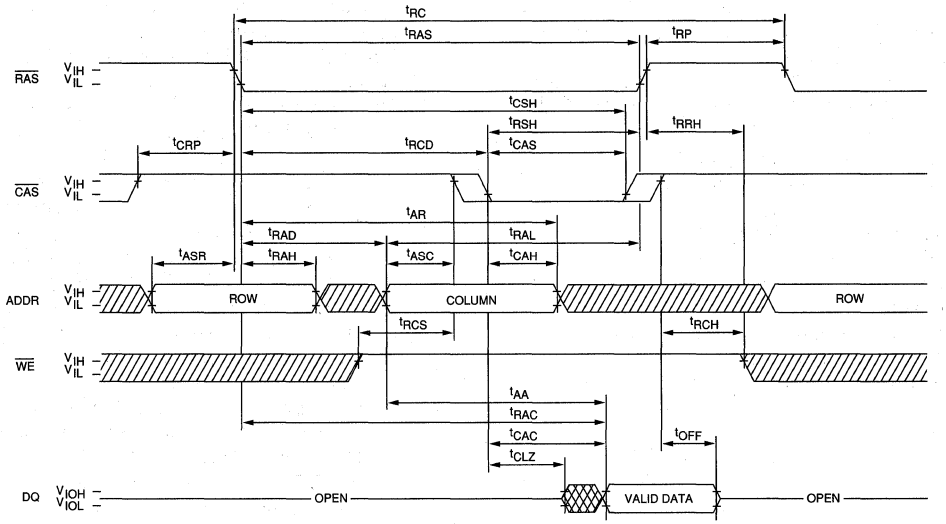
(Notes: 3, 4, 5, 6, 7, 10, 11, 16, 21) ($0°C \le T_A \le 70°C$; $V_{CC} = 5V \pm 10\%$)

AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
$\overline{CAS}$ to output in Low-Z	^tCLZ	0		0		0		ns	
Output buffer turn-off delay	^tOFF	0	20	0	20	0	20	ns	12
$\overline{WE}$ command setup time	^tWCS	0		0		0		ns	
Write command hold time	^tWCH	10		15		15		ns	
Write command hold time (referenced to $\overline{RAS}$)	^tWCR	45		55		60		ns	
Write command pulse width	^tWP	10		15		15		ns	
Write command to $\overline{RAS}$ lead time	^tRWL	15		20		20		ns	
Write command to $\overline{CAS}$ lead time	^tCWL	15		20		20		ns	
Data-in setup time	^tDS	0		0		0		ns	15
Data-in hold time	^tDH	10		15		15		ns	15
Data-in hold time (referenced to $\overline{RAS}$)	^tDHR	45		55		60		ns	
Transition time (rise or fall)	^tT	3	50	3	50	3	50	ns	5, 16
Refresh period (1,024 cycles)	^tREF		16/128		16/128		16/128	ms	3/24
$\overline{RAS}$ to $\overline{CAS}$ precharge time	^tRPC	0		0		0		ns	
$\overline{CAS}$ setup time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tCSR	10		10		10		ns	19
$\overline{CAS}$ hold time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tCHR	15		15		15		ns	19
$\overline{WE}$ hold time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tWRH	10		10		10		ns	
$\overline{WE}$ setup time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tWRP	10		10		10		ns	
$\overline{WE}$ hold time (WCBR test cycle)	^tWTH	10		10		10		ns	
$\overline{WE}$ setup time (WCBR test cycle)	^tWTS	10		10		10		ns	

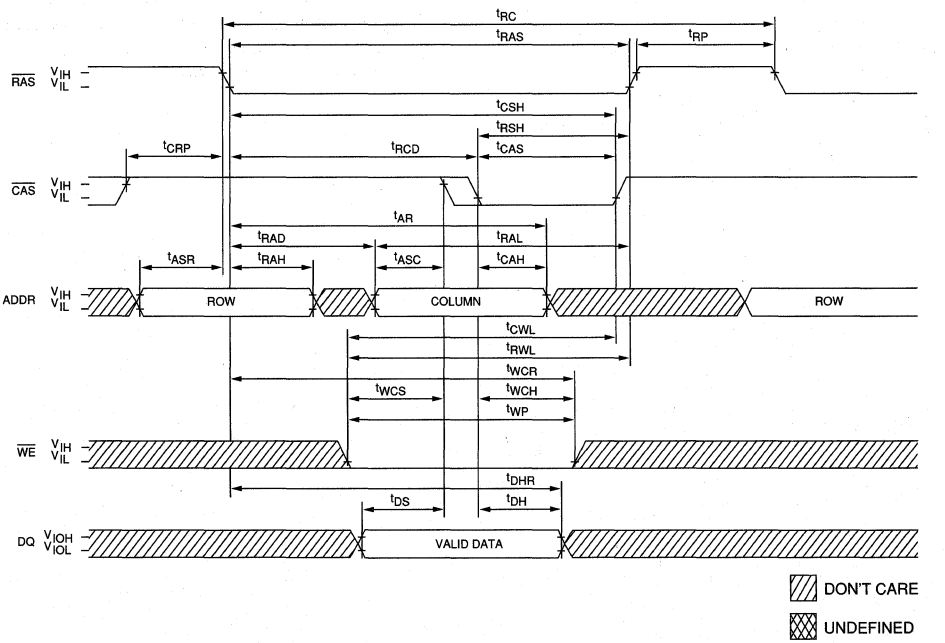
NOTES

. All voltages referenced to V_{SS}.
. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
. An initial pause of 100µs is required after power-up followed by any eight $\overline{RAS}$ REFRESH cycles ($\overline{RAS}$-ONLY or CBR with $\overline{WE}$ HIGH) before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-up should be repeated any time the ^{t}REF refresh requirement is exceeded.
. AC characteristics assume ^{t}T = 5ns.
. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \le T_A \le 70°C$) is assured.
. Measured with a load equivalent to two TTL gates and 100pF.
. Assumes that $^{t}RCD < {}^{t}RCD$ (MAX). If ^{t}RCD is greater than the maximum recommended value shown in this table, ^{t}RAC will increase by the amount that ^{t}RCD exceeds the value shown.
. Assumes that $^{t}RCD \ge {}^{t}RCD$ (MAX).
). If $\overline{CAS}$ = V_{IH}, data output is High-Z.
1. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
2. ^{t}OFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
3. Operation within the ^{t}RCD (MAX) limit ensures that ^{t}RAC (MAX) can be met. ^{t}RCD (MAX) is specified as a reference point only; if ^{t}RCD is greater than the specified ^{t}RCD (MAX) limit, then access time is controlled exclusively by ^{t}CAC.
14. Either ^{t}RCH or ^{t}RRH must be satisfied for a READ cycle.
15. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY-WRITE cycles.
16. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
17. This parameter is sampled. Capacitance is measured using MIL-STD-883C, Method 3012.1 (1 MHz AC, Vcc = 5V, DC bias = 2.4V @ 15mV RMS).
18. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, data-out (Q) will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer, $\overline{CAS}$ must be pulsed HIGH for ^{t}CP.
19. On-chip refresh and address counters are enabled.
20. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW.
21. LATE-WRITE, READ-WRITE or READ-MODIFY-WRITE cycles are not available due to $\overline{OE}$ being grounded on all 4 Meg DRAMs.
22. I_{CC} is dependent on cycle rates.
23. Operation within the ^{t}RAD (MAX) limit ensures that ^{t}RCD (MAX) can be met. ^{t}RAD (MAX) is specified as a reference point only; if ^{t}RAD is greater than the specified ^{t}RAD (MAX) limit, then access time is controlled exclusively by ^{t}AA.
24. Applies to L-version only.

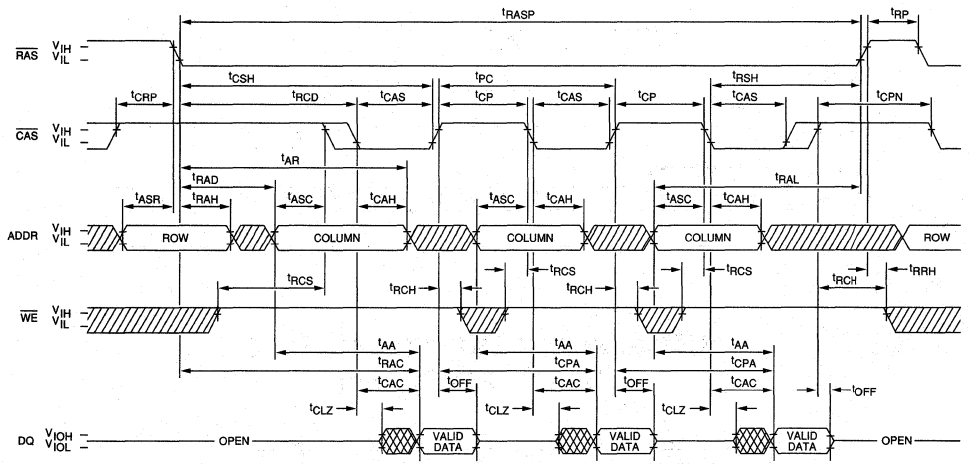
READ CYCLE



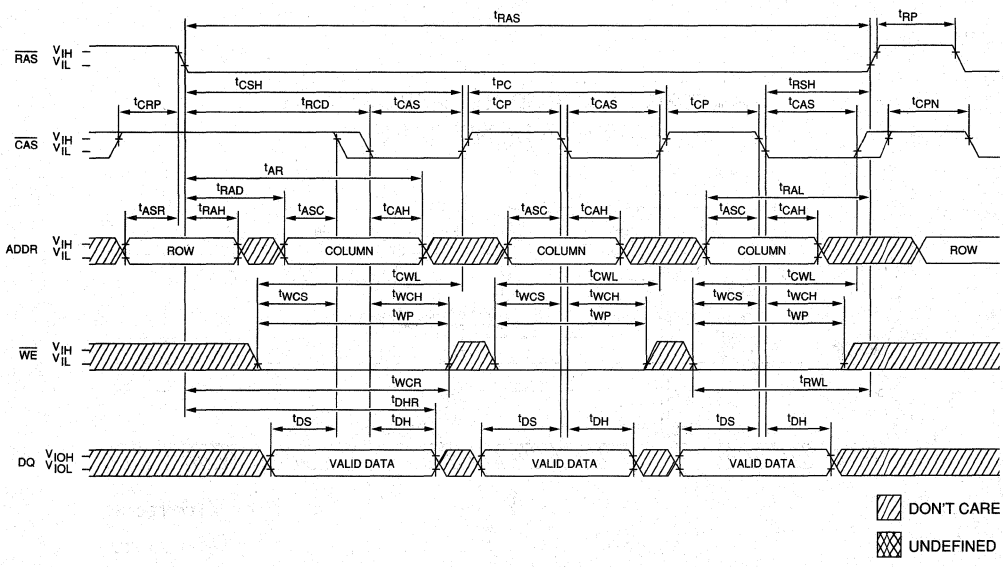
EARLY-WRITE CYCLE



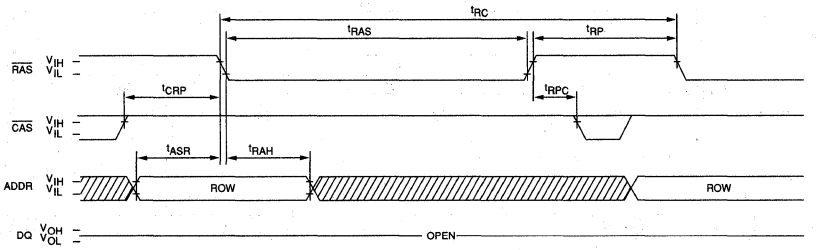
FAST-PAGE-MODE READ CYCLE



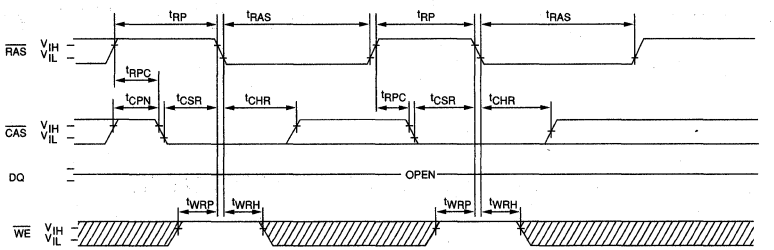
FAST-PAGE-MODE EARLY-WRITE CYCLE



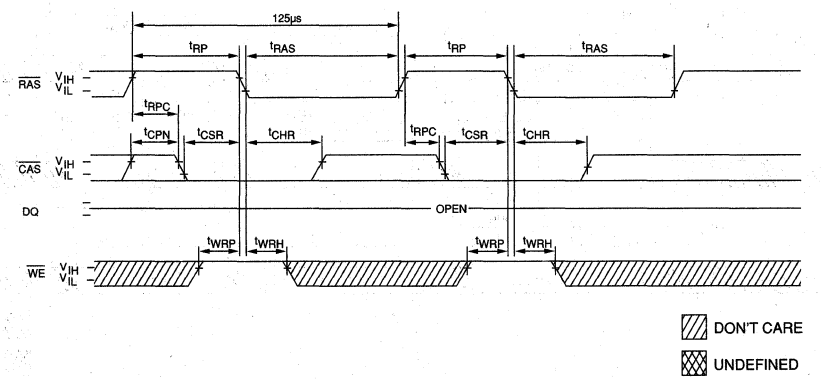
$\overline{RAS}$-ONLY REFRESH CYCLE
(ADDR = A0-A9; $\overline{WE}$ = DON'T CARE)



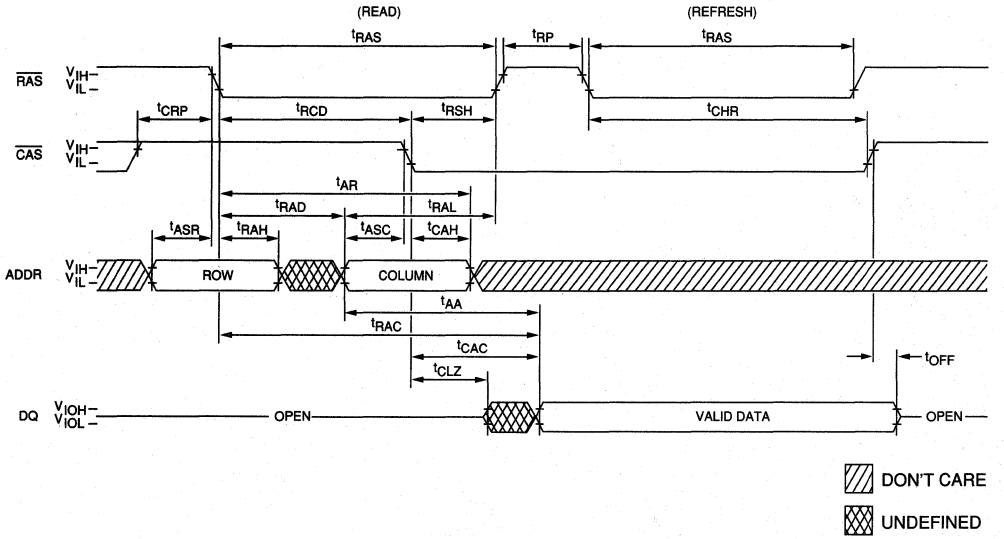
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE
(A0-A9 = DON'T CARE)



BATTERY BACKUP REFRESH CYCLE [24]
(A0-A9 = DON'T CARE)



HIDDEN REFRESH CYCLE [20]
($\overline{WE}$ = HIGH)



DRAM MODULE

4 MEG x 36, 8 MEG x 18
FAST PAGE MODE

NEW DRAM MODULE

FEATURES

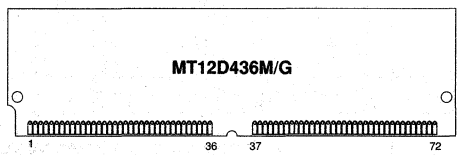
- Industry standard pinout in a 72-pin single-in-line package
- High-performance, CMOS silicon-gate process
- Single 5V ±10% power supply
- All device pins are fully TTL compatible
- Low power, 52mW standby; 3,100mW active, typical
- Refresh modes: RAS-ONLY, CAS-BEFORE-RAS (CBR) and HIDDEN
- 2,048-cycle refresh distributed across 32ms
- FAST PAGE MODE access cycle
- Multiple RAS lines allow x18 or x36 width

OPTIONS MARKING

- Timing
  - 60ns access - 6
  - 70ns access - 7
  - 80ns access - 8
- Packages
  - Leadless 72-pin SIMM M
  - Leadless 72-pin SIMM (Gold) G
- Part Number Example: MT12D436G-6

PIN ASSIGNMENT (Top View)

72-Pin SIMM
(T-21)



PIN #	SYMBOL	PIN #	SYMBOL	PIN #	SYMBOL	PIN #	SYMBOL
1	Vss	19	A10	37	DQ18	55	DQ13
2	DQ1	20	DQ5	38	DQ36	56	DQ31
3	DQ19	21	DQ23	39	Vss	57	DQ14
4	DQ2	22	DQ6	40	CAS0	58	DQ32
5	DQ20	23	DQ24	41	CAS2	59	Vcc
6	DQ3	24	DQ7	42	CAS3	60	DQ33
7	DQ21	25	DQ25	43	CAS1	61	DQ15
8	DQ4	26	DQ8	44	RAS0	62	DQ34
9	DQ22	27	DQ26	45	NC	63	DQ16
10	Vcc	28	A7	46	NC	64	DQ35
11	NC	29	NC	47	WE	65	DQ17
12	A0	30	Vcc	48	NC	66	NC
13	A1	31	A8	49	DQ10	67	PRD1
14	A2	32	A9	50	DQ28	68	PRD2
15	A3	33	NC	51	DQ11	69	PRD3
16	A4	34	RAS2	52	DQ29	70	PRD4
17	A5	35	DQ27	53	DQ12	71	NC
18	A6	36	DQ9	54	DQ30	72	Vss

GENERAL DESCRIPTION

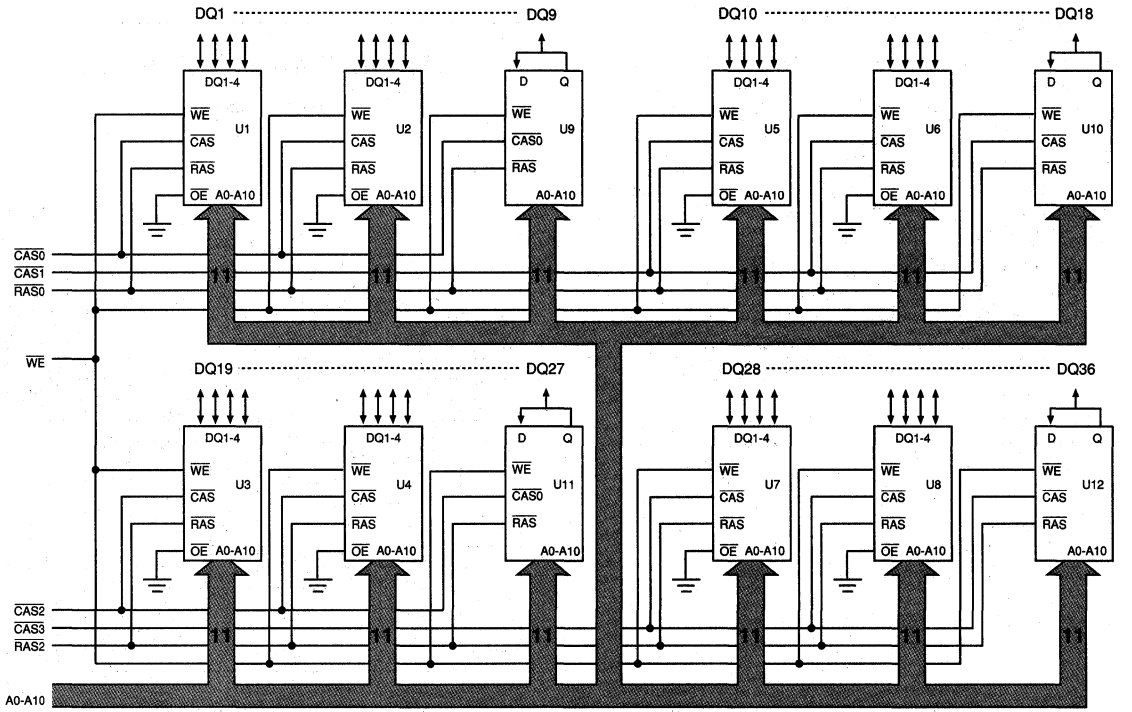
The MT12D436 is a randomly accessed solid-state memory containing 4,194,304 words organized in a x36 configuration. During READ or WRITE cycles, each bit is uniquely addressed through the 22 address bits, which are entered 11 bits (A0-A10) at a time. RAS is used to latch the first 11 bits and CAS the latter 11 bits. A READ or WRITE cycle is selected with the WE input. A logic HIGH on WE dictates READ mode while a logic LOW on WE dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of CAS. Since WE goes LOW prior to CAS going LOW, the output pin(s) remain open (High-Z) until the next CAS cycle.

FAST PAGE MODE operations allow faster data operations (READ or WRITE) within a row-address (A0-A10) defined page boundary. The FAST PAGE MODE cycle is always initiated with a row address strobed-in by RAS followed by a column address strobed-in by CAS. CAS may be toggled-in by holding RAS LOW and strobing-in different column addresses, thus executing faster memory cycles. Returning RAS HIGH terminates the FAST PAGE MODE operation.

Returning RAS and CAS HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the RAS HIGH time. Memory cell data is retained in its correct state by maintaining power and executing any RAS cycle (READ, WRITE, RAS-ONLY, CAS-BEFORE-RAS or HIDDEN REFRESH) so that all 2,048 combinations of RAS addresses (A0-A10) are executed at least every 32ms, regardless of sequence. The CBR REFRESH cycle will invoke the refresh counter for automatic RAS addressing.

NEW ■ DRAM MODULE

FUNCTIONAL BLOCK DIAGRAM



U1-U8 = MT4C4M4A1DJ
U9-U12 = MT4C1004JDJ

TRUTH TABLE

FUNCTION		RAS	CAS	WE	ADDRESSES		DATA IN/OUT
					^tR	^tC	DQ1-DQ36
Standby		H	H→X	X	X	X	High-Z
READ		L	L	H	ROW	COL	Data Out
EARLY-WRITE		L	L	L	ROW	COL	Data In
FAST-PAGE-MODE	1st Cycle	L	H→L	H	ROW	COL	Data Out
READ	2nd Cycle	L	H→L	H	n/a	COL	Data Out
FAST-PAGE-MODE	1st Cycle	L	H→L	L	ROW	COL	Data In
WRITE	2nd Cycle	L	H→L	L	n/a	COL	Data In
RAS-ONLY REFRESH		L	H	X	ROW	n/a	High-Z
HIDDEN	READ	L→H→L	L	H	ROW	COL	Data Out
REFRESH	WRITE	L→H→L	L	L	ROW	COL	Data In
CAS-BEFORE-RAS REFRESH		H→L	L	H	X	X	High-Z

PRESENCE DETECT

SYMBOL	-6	-7	-8
PRD1	Vss	Vss	Vss
PRD2	NC	NC	NC
PRD3	NC	Vss	NC
PRD4	NC	NC	Vss

NEW DRAM MODULE

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} ..... -1V to +7V
Operating Temperature, T_A (Ambient) ..... 0°C to +70°C
Storage Temperature (Plastic) ..... -55°C to +125°C
Power Dissipation 12W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 3, 4, 6, 7) (0°C ≤ T_A ≤ 70°C; V_{CC} = 5V ±10%)

PARAMETER/CONDITION		SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage		V_{CC}	4.5	5.5	V	1
Input High (Logic 1) Voltage, All Inputs		V_{IH}	2.4	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, All Inputs		V_{IL}	-1.0	0.8	V	1
INPUT LEAKAGE CURRENT	$\overline{RAS0}$, $\overline{RAS2}$	I_{I1}	-12	12	µA	
Any Input 0V ≤ V_{IN} ≤ V_{CC}	A0-A10, $\overline{WE}$	I_{I2}	-24	24	µA	
(All other pins not under test = 0V) for each package input	$\overline{CAS0}$-$\overline{CAS3}$	I_{I3}	-6	6	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled, 0V ≤ V_{OUT} ≤ V_{CC}) for each package input	DQ1-DQ36	I_{OZ}	-10	10	µA	
OUTPUT LEVELS Output High Voltage (I_{OUT} = -5mA)		V_{OH}	2.4		V	
Output Low Voltage (I_{OUT} = 5mA)		V_{OL}		0.4	V	

PARAMETER/CONDITION	SYMBOL	MAX -6	MAX -7	MAX -8	UNITS	NOTES
STANDBY CURRENT: (TTL) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC1}	24	24	24	mA	
STANDBY CURRENT: (CMOS) ($\overline{RAS}$ = $\overline{CAS}$ = Other Inputs = V_{CC} -0.2V)	I_{CC2}	12	12	12	mA	
OPERATING CURRENT: Random READ/WRITE Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC (MIN))	I_{CC3}	1400	1200	1040	mA	3, 4
OPERATING CURRENT: FAST PAGE MODE Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: ^tPC = ^tPC (MIN))	I_{CC4}	960	840	720	mA	3, 4
REFRESH CURRENT: $\overline{RAS}$-ONLY Average power supply current ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}: ^tRC = ^tRC (MIN))	I_{CC5}	1400	1200	1040	mA	3
REFRESH CURRENT: $\overline{CAS}$-BEFORE-$\overline{RAS}$ Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC (MIN))	I_{CC6}	1400	1200	1040	mA	3, 5

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A10	C_{I1}		77	pF	2
Input Capacitance: $\overline{WE}$	C_{I2}		100	pF	2
Input Capacitance: $\overline{RAS0}$, $\overline{RAS2}$	C_{I3}		51	pF	2
Input Capacitance: $\overline{CAS0}$, $\overline{CAS1}$, $\overline{CAS2}$, $\overline{CAS3}$	C_{I4}		25	pF	2
Input/Output Capacitance: DQ1-DQ36	C_{IO}		10	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13, 22) (V_{CC} = 5V ±10%)

AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	^tRC	110		130		150		ns	
READ-WRITE cycle time	^tRWC	n/a		n/a		n/a		ns	22
FAST-PAGE-MODE READ or WRITE cycle time	^tPC	40		40		45		ns	
FAST-PAGE-MODE READ-WRITE cycle time	^tPRWC	n/a		n/a		n/a		ns	22
Access time from $\overline{RAS}$	^tRAC		60		70		80	ns	14
Access time from $\overline{CAS}$	^tCAC		15		20		20	ns	15
Access time from column address	^tAA		30		35		40	ns	
Access time from $\overline{CAS}$ precharge	^tCPA		40		40		45	ns	
$\overline{RAS}$ pulse width	^tRAS	60	100,000	70	100,000	80	100,000	ns	
$\overline{RAS}$ pulse width (FAST PAGE MODE)	^tRASP	60	100,000	70	100,000	80	100,000	ns	
$\overline{RAS}$ hold time	^tRSH	15		20		20		ns	
$\overline{RAS}$ precharge time	^tRP	40		50		60		ns	
$\overline{CAS}$ pulse width	^tCAS	15	100,000	20	100,000	20	100,000	ns	
$\overline{CAS}$ hold time	^tCSH	60		70		80		ns	
$\overline{CAS}$ precharge time	^tCPN	10		10		10		ns	16
$\overline{CAS}$ precharge time (FAST PAGE MODE)	^tCP	10		10		10		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	^tRCD	20	40	20	50	20	60	ns	17
$\overline{CAS}$ to $\overline{RAS}$ precharge time	^tCRP	5		5		5		ns	
Row address setup time	^tASR	0		0		0		ns	
Row address hold time	^tRAH	10		10		10		ns	
$\overline{RAS}$ to column address delay time	^tRAD	15	30	15	35	15	40	ns	18
Column address setup time	^tASC	0		0		0		ns	
Column address hold time	^tCAH	10		15		15		ns	
Column address hold time (referenced to $\overline{RAS}$)	^tAR	50		55		60		ns	
Column address to $\overline{RAS}$ lead time	^tRAL	30		35		40		ns	
Read command setup time	^tRCS	0		0		0		ns	
Read command hold time (referenced to $\overline{CAS}$)	^tRCH	0		0		0		ns	19
Read command hold time (referenced to $\overline{RAS}$)	^tRRH	0		0		0		ns	19

NEW ■ DRAM MODULE

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13, 23) (V_{CC} = 5V ±10%)

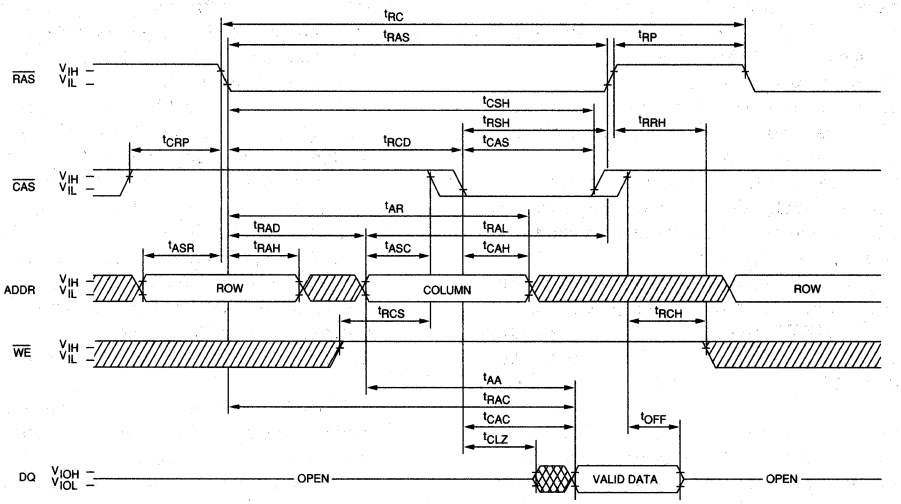
AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
$\overline{CAS}$ to output in Low-Z	^tCLZ	0		0		0		ns	
Output buffer turn-off delay	^tOFF	0	20	0	20	0	20	ns	20
$\overline{WE}$ command setup time	^tWCS	0		0		0		ns	
Write command hold time	^tWCH	10		15		15		ns	
Write command hold time (referenced to $\overline{RAS}$)	^tWCR	45		55		60		ns	
Write command pulse width	^tWP	10		15		15		ns	
Write command to $\overline{RAS}$ lead time	^tRWL	15		20		20		ns	
Write command to $\overline{CAS}$ lead time	^tCWL	15		20		20		ns	
Data-in setup time	^tDS	0		0		0		ns	21
Data-in hold time	^tDH	10		15		15		ns	21
Data-in hold time (referenced to $\overline{RAS}$)	^tDHR	45		55		60		ns	
Transition time (rise or fall)	^tT	3	50	3	50	3	50	ns	9, 10
Refresh period (2,048 cycles)	^tREF		32		32		32	ms	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	^tRPC	0		0		0		ns	
$\overline{CAS}$ setup time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tCSR	10		10		10		ns	5
$\overline{CAS}$ hold time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tCHR	15		15		15		ns	5
$\overline{WE}$ hold time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tWRH	10		10		10		ns	24
$\overline{WE}$ setup time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tWRP	10		10		10		ns	24
$\overline{WE}$ hold time (WCBR test cycle)	^tWTH	10		10		10		ns	24
$\overline{WE}$ setup time (WCBR test cycle)	^tWTS	10		10		10		ns	24

NOTES

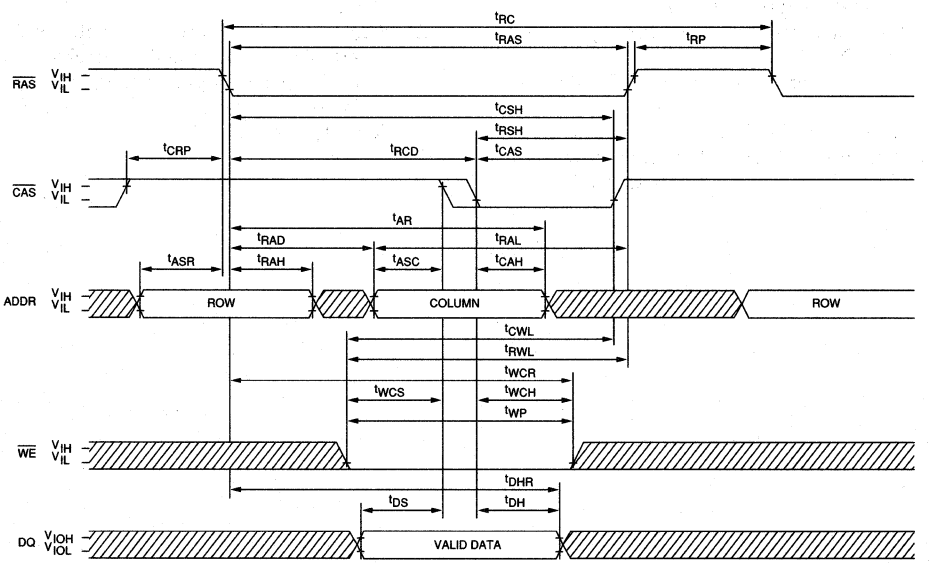
1. All voltages referenced to V_{SS}.
2. This parameter is sampled. Capacitance is measured using MIL-STD-883C, Method 3012.1 (1 MHz AC, Vcc = 5V, DC bias = 2.4V @ 15mV RMS).
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is assured.
7. An initial pause of 100µs is required after power-up followed by eight $\overline{RAS}$ refresh cycles ($\overline{RAS}$-ONLY or CBR with $\overline{WE}$ HIGH) before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-up should be repeated any time the ^{t}REF refresh requirement is exceeded.
8. AC characteristics assume ^{t}T = 5ns.
9. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS}$ = V_{IH}, data output is High-Z.
12. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to 2 TTL gates and 100pF.
14. Assumes that $^{t}RCD < {}^{t}RCD$ (MAX). If ^{t}RCD is greater than the maximum recommended value shown in this table, ^{t}RAC will increase by the amount that ^{t}RCD exceeds the value shown.
15. Assumes that $^{t}RCD \geq {}^{t}RCD$ (MAX).
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer, $\overline{CAS}$ must be pulsed HIGH for ^{t}CPN.
17. Operation within the ^{t}RCD (MAX) limit ensures that ^{t}RAC (MAX) can be met. ^{t}RCD (MAX) is specified as a reference point only; if ^{t}RCD is greater than the specified ^{t}RCD (MAX) limit, then access time is controlled exclusively by ^{t}CAC.
18. Operation within the ^{t}RAD (MAX) limit ensures that ^{t}RCD (MAX) can be met. ^{t}RAD (MAX) is specified as a reference point only; if ^{t}RAD is greater than the specified ^{t}RAD (MAX) limit, then access time is controlled exclusively by ^{t}AA.
19. Either ^{t}RCH or ^{t}RRH must be satisfied for a READ cycle.
20. ^{t}OFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
21. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY-WRITE cycles.
22. $\overline{OE}$ is tied permanently LOW; LATE-WRITE or READ-MODIFY-WRITE operations are not possible.
23. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW and $\overline{OE}$ = HIGH.
24. ^{t}WTS and ^{t}WTH are setup and hold specifications for the $\overline{WE}$ pin being held LOW to enable the JEDEC test mode (with CBR timing constraints). These two parameters are the inverts of ^{t}WRP and ^{t}WRH in the CBR refresh cycle.

NEW DRAM MODULE

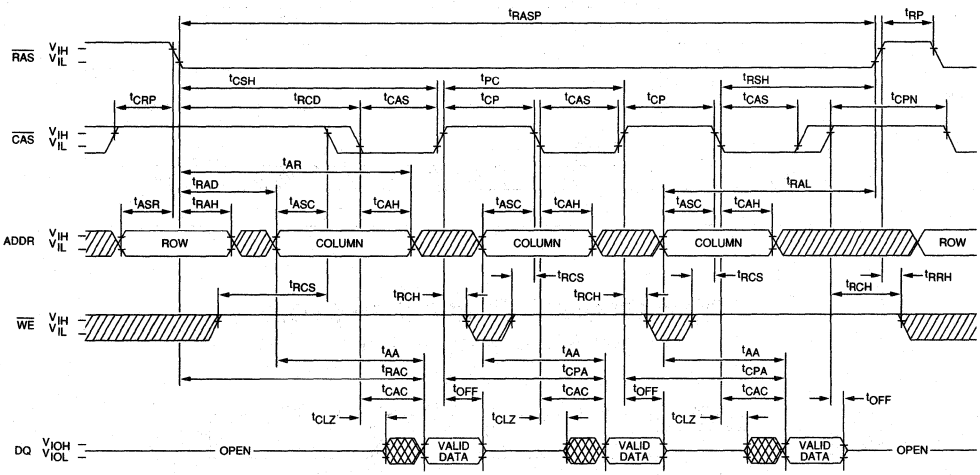
READ CYCLE



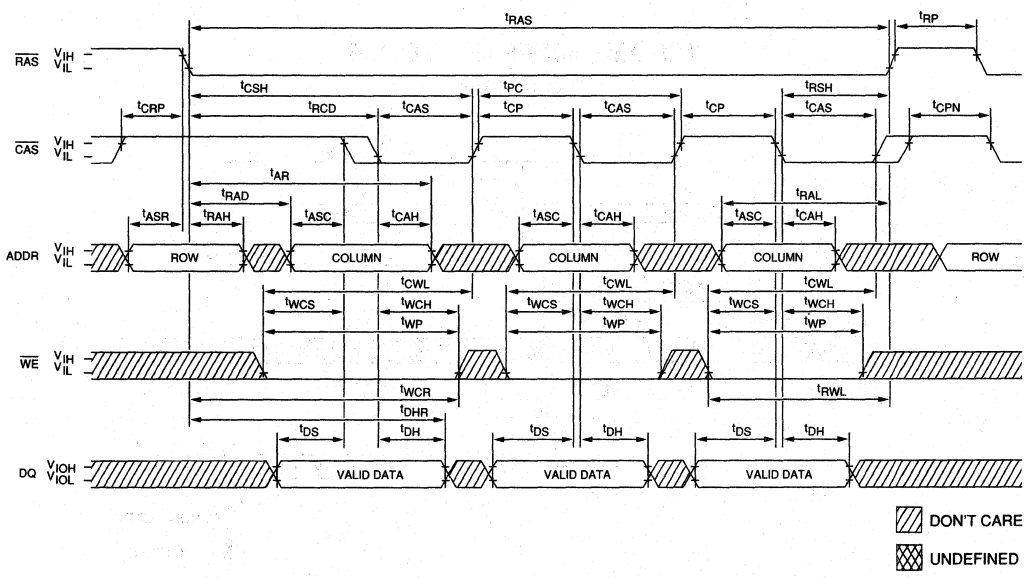
EARLY-WRITE CYCLE



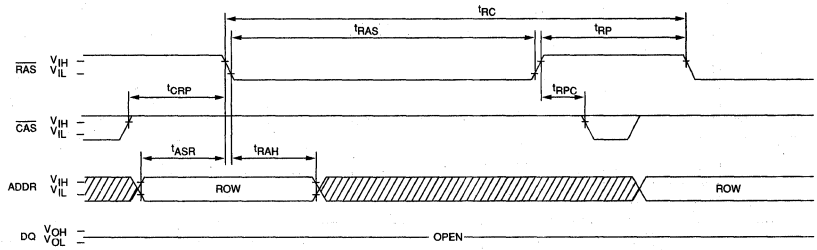
FAST-PAGE-MODE READ CYCLE



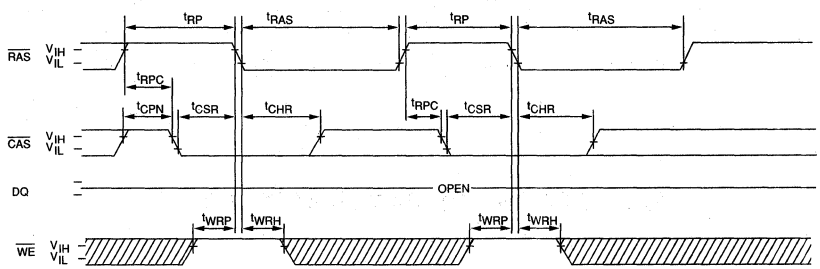
FAST-PAGE-MODE EARLY-WRITE CYCLE



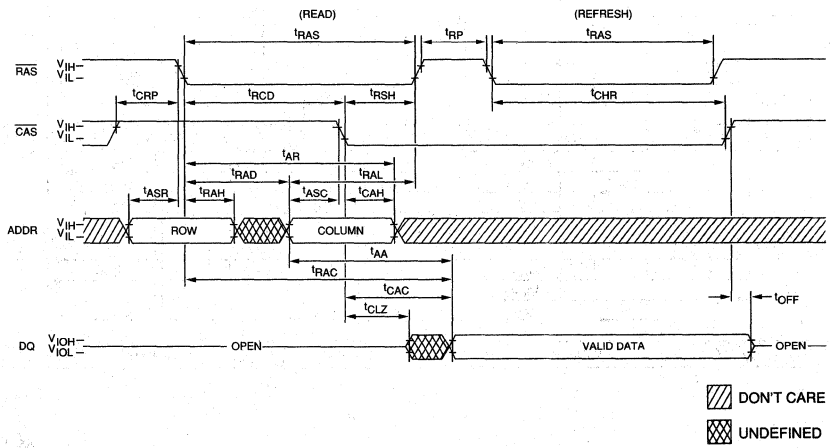
$\overline{\text{RAS}}$-ONLY REFRESH CYCLE
(ADDR = A0-A10; $\overline{\text{WE}}$ = DON'T CARE)



$\overline{\text{CAS}}$-BEFORE-$\overline{\text{RAS}}$ REFRESH CYCLE
(A0-A10 = DON'T CARE)



HIDDEN REFRESH CYCLE [23]
($\overline{\text{WE}}$ = HIGH)



DRAM MODULE

8 MEG x 36,16 MEG x18
FAST PAGE MODE

NEW DRAM MODULE

FEATURES

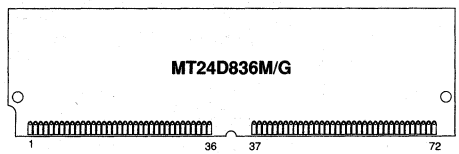
- Industry standard pinout in a 72-pin single-in-line package
- High-performance, CMOS silicon-gate process
- Single 5V ±10% power supply
- All device pins are fully TTL compatible
- Low power, 104mW standby; 3,152mW active, typical
- Refresh modes: $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$ (CBR) and HIDDEN
- 2,048-cycle refresh distributed across 32ms
- FAST PAGE MODE access cycle
- Multiple $\overline{RAS}$ lines allow x18 or x36 widths

OPTIONS MARKING

- Timing
  - 60ns access - 6
  - 70ns access - 7
  - 80ns access - 8
- Packages
  - Leadless 72-pin SIMM M
  - Leadless 72-pin SIMM (Gold) G
- Part Number Example: MT24D836G-6

PIN ASSIGNMENT (Top View)

72-Pin SIMM
(T-22)



PIN #	SYMBOL	PIN #	SYMBOL	PIN #	SYMBOL	PIN #	SYMBOL
1	Vss	19	A10	37	DQ18	55	DQ13
2	DQ1	20	DQ5	38	DQ36	56	DQ31
3	DQ19	21	DQ23	39	Vss	57	DQ14
4	DQ2	22	DQ6	40	$\overline{CAS0}$	58	DQ32
5	DQ20	23	DQ24	41	$\overline{CAS2}$	59	Vcc
6	DQ3	24	DQ7	42	$\overline{CAS3}$	60	DQ33
7	DQ21	25	DQ25	43	$\overline{CAS1}$	61	DQ15
8	DQ4	26	DQ8	44	$\overline{RAS0}$	62	DQ34
9	DQ22	27	DQ26	45	$\overline{RAS1}$	63	DQ16
10	Vcc	28	A7	46	NC	64	DQ35
11	NC	29	NC	47	$\overline{WE}$	65	DQ17
12	A0	30	Vcc	48	NC	66	NC
13	A1	31	A8	49	DQ10	67	PRD1
14	A2	32	A9	50	DQ28	68	PRD2
15	A3	33	$\overline{RAS3}$	51	DQ11	69	PRD3
16	A4	34	$\overline{RAS2}$	52	DQ29	70	PRD4
17	A5	35	DQ27	53	DQ12	71	NC
18	A6	36	DQ9	54	DQ30	72	Vss

GENERAL DESCRIPTION

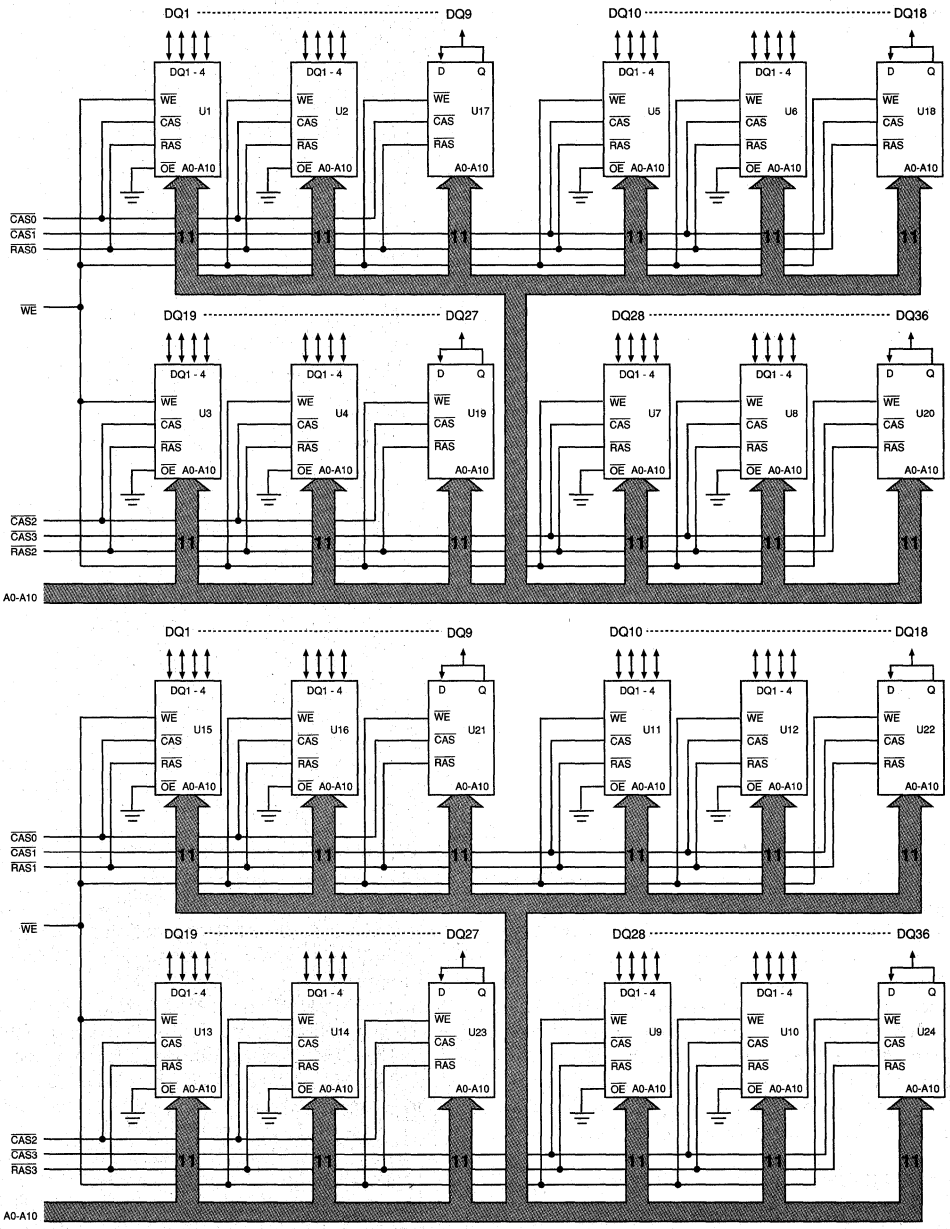
The MT24D836 is a randomly accessed solid-state memory containing 8,388,608 words organized in a x36 configuration. During READ or WRITE cycles, each bit is uniquely addressed through the 22 address bits, which are entered 11 bits (A0-A10) at a time. $\overline{RAS}$ is used to latch the first 11 bits and $\overline{CAS}$ the latter 11 bits. A READ or WRITE cycle is selected with the $\overline{WE}$ input. A logic HIGH on $\overline{WE}$ dictates READ mode while a logic LOW on $\overline{WE}$ dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of $\overline{CAS}$. Since $\overline{WE}$ goes LOW prior to $\overline{CAS}$ going LOW, the output pin(s) remain open (High-Z) until the next $\overline{CAS}$ cycle.

FAST PAGE MODE operations allow faster data operations (READ or WRITE) within a row-address (A0-A10) defined page boundary. The FAST PAGE MODE cycle is always initiated with a row address strobed-in by $\overline{RAS}$ followed by a column address strobed-in by $\overline{CAS}$. $\overline{CAS}$ may be toggled-in by holding $\overline{RAS}$ LOW and strobing-in different column addresses, thus executing faster memory cycles. Returning $\overline{RAS}$ HIGH terminates the FAST PAGE MODE operation.

Returning $\overline{RAS}$ and $\overline{CAS}$ HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the $\overline{RAS}$ HIGH time. Memory cell data is retained in its correct state by maintaining power and executing any $\overline{RAS}$ cycle (READ, WRITE, $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$ or HIDDEN REFRESH) so that all 2,048 combinations of $\overline{RAS}$ addresses (A0-A10) are executed at least every 32ms, regardless of sequence. The CBR REFRESH cycle will invoke the refresh counter for automatic $\overline{RAS}$ addressing.

NEW ■ DRAM MODULE

FUNCTIONAL BLOCK DIAGRAM



U1-U16 = MT4C4M4A1DJ
U17-U24 = MT4C1004JDJ

TRUTH TABLE

FUNCTION		RAS	CAS	WE	ADDRESSES		DATA IN/OUT
					^tR	^tC	DQ1-DQ36
Standby		H	H→X	X	X	X	High-Z
READ		L	L	H	ROW	COL	Data Out
EARLY-WRITE		L	L	L	ROW	COL	Data In
FAST-PAGE-MODE	1st Cycle	L	H→L	H	ROW	COL	Data Out
READ	2nd Cycle	L	H→L	H	n/a	COL	Data Out
FAST-PAGE-MODE	1st Cycle	L	H→L	L	ROW	COL	Data In
WRITE	2nd Cycle	L	H→L	L	n/a	COL	Data In
RAS-ONLY REFRESH		L	H	X	ROW	n/a	High-Z
HIDDEN	READ	L→H→L	L	H	ROW	COL	Data Out
REFRESH	WRITE	L→H→L	L	L	ROW	COL	Data In
CAS-BEFORE-RAS REFRESH		H→L	L	H	X	X	High-Z

PRESENCE DETECT

SYMBOL	-6	-7	-8
PRD1	NC	NC	NC
PRD2	Vss	Vss	Vss
PRD3	NC	Vss	NC
PRD4	NC	NC	Vss

NEW ■ DRAM MODULE

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} ..... -1V to +7V
Operating Temperature, T_A (Ambient) ..... 0°C to +70°C
Storage Temperature (Plastic) ..... -55°C to +125°C
Power Dissipation 24W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 3, 4, 6, 7) (0°C ≤ T_A ≤ 70°C; V_{CC} = 5V ±10%)

PARAMETER/CONDITION		SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage		V_{CC}	4.5	5.5	V	1
Input High (Logic 1) Voltage, All Inputs		V_{IH}	2.4	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, All Inputs		V_{IL}	-1.0	0.8	V	1
INPUT LEAKAGE CURRENT	$\overline{RAS0}$-$\overline{RAS3}$	I_{I1}	-12	12	µA	
Any Input 0V ≤ V_{IN} ≤ V_{CC}	A0-A10, $\overline{WE}$	I_{I2}	-48	48	µA	
(All other pins not under test = 0V) for each package input	$\overline{CAS0}$-$\overline{CAS3}$	I_{I3}	-12	12	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled, 0V ≤ V_{OUT} ≤ V_{CC}) for each package input	DQ1-DQ36	I_{OZ}	-20	20	µA	
OUTPUT LEVELS Output High Voltage (I_{OUT} = -5mA)		V_{OH}	2.4		V	
Output Low Voltage (I_{OUT} = 5mA)		V_{OL}		0.4	V	

		MAX				
PARAMETER/CONDITION	SYMBOL	-6	-7	-8	UNITS	NOTES
STANDBY CURRENT: (TTL) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC1}	48	48	48	mA	
STANDBY CURRENT: (CMOS) ($\overline{RAS}$ = $\overline{CAS}$ = Other Inputs = V_{CC} -0.2V)	I_{CC2}	24	24	24	mA	
OPERATING CURRENT: Random READ/WRITE Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC (MIN))	I_{CC3}	1424	1224	1064	mA	3, 4
OPERATING CURRENT: FAST PAGE MODE Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: ^tPC = ^tPC (MIN))	I_{CC4}	984	864	744	mA	3, 4
REFRESH CURRENT: $\overline{RAS}$-ONLY Average power supply current ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}: ^tRC = ^tRC (MIN))	I_{CC5}	1424	1224	1064	mA	3
REFRESH CURRENT: $\overline{CAS}$-BEFORE-$\overline{RAS}$ Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC (MIN))	I_{CC6}	1424	1224	1064	mA	3, 5

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A10	C_{I1}		154	pF	2
Input Capacitance: $\overline{WE}$	C_{I2}		200	pF	2
Input Capacitance: $\overline{RAS0}$, $\overline{RAS1}$, $\overline{RAS2}$, $\overline{RAS3}$	C_{I3}		51	pF	2
Input Capacitance: $\overline{CAS0}$, $\overline{CAS1}$, $\overline{CAS2}$, $\overline{CAS3}$	C_{I4}		50	pF	2
Input/Output Capacitance: DQ1-DQ36	C_{IO}		20	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13, 22) (V_{CC} = 5V ±10%)

AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	^tRC	110		130		150		ns	
READ-WRITE cycle time	^tRWC	n/a		n/a		n/a		ns	22
FAST-PAGE-MODE READ or WRITE cycle time	^tPC	40		40		45		ns	
FAST-PAGE-MODE READ-WRITE cycle time	^tPRWC	n/a		n/a		n/a		ns	22
Access time from $\overline{RAS}$	^tRAC		60		70		80	ns	14
Access time from $\overline{CAS}$	^tCAC		15		20		20	ns	15
Access time from column address	^tAA		30		35		40	ns	
Access time from $\overline{CAS}$ precharge	^tCPA		40		40		45	ns	
$\overline{RAS}$ pulse width	^tRAS	60	100,000	70	100,000	80	100,000	ns	
$\overline{RAS}$ pulse width (FAST PAGE MODE)	^tRASP	60	100,000	70	100,000	80	100,000	ns	
$\overline{RAS}$ hold time	^tRSH	15		20		20		ns	
$\overline{RAS}$ precharge time	^tRP	40		50		60		ns	
$\overline{CAS}$ pulse width	^tCAS	15	100,000	20	100,000	20	100,000	ns	
$\overline{CAS}$ hold time	^tCSH	60		70		80		ns	
$\overline{CAS}$ precharge time	^tCPN	10		10		10		ns	16
$\overline{CAS}$ precharge time (FAST PAGE MODE)	^tCP	10		10		10		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	^tRCD	20	40	20	50	20	60	ns	17
$\overline{CAS}$ to $\overline{RAS}$ precharge time	^tCRP	5		5		5		ns	
Row address setup time	^tASR	0		0		0		ns	
Row address hold time	^tRAH	10		10		10		ns	
$\overline{RAS}$ to column address delay time	^tRAD	15	30	15	35	15	40	ns	18
Column address setup time	^tASC	0		0		0		ns	
Column address hold time	^tCAH	10		15		15		ns	
Column address hold time (referenced to $\overline{RAS}$)	^tAR	50		55		60		ns	
Column address to $\overline{RAS}$ lead time	^tRAL	30		35		40		ns	
Read command setup time	^tRCS	0		0		0		ns	
Read command hold time (referenced to $\overline{CAS}$)	^tRCH	0		0		0		ns	19
Read command hold time (referenced to $\overline{RAS}$)	^tRRH	0		0		0		ns	19
$\overline{CAS}$ to output in Low-Z	^tCLZ	0		0		0		ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13, 23) (V_{CC} = 5V ±10%)

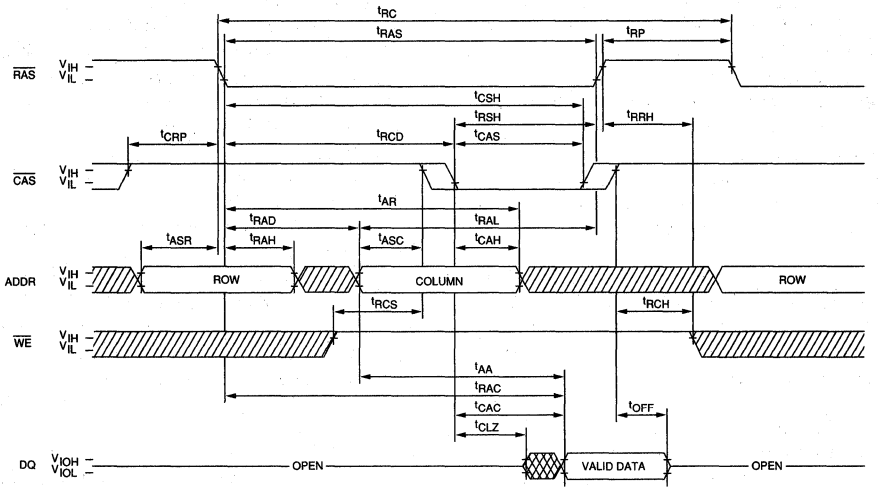
AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Output buffer turn-off delay	^tOFF	0	20	0	20	0	20	ns	20
$\overline{WE}$ command setup time	^tWCS	0		0		0		ns	
Write command hold time	^tWCH	10		15		15		ns	
Write command hold time (referenced to $\overline{RAS}$)	^tWCR	45		55		60		ns	
Write command pulse width	^tWP	10		15		15		ns	
Write command to $\overline{RAS}$ lead time	^tRWL	15		20		20		ns	
Write command to $\overline{CAS}$ lead time	^tCWL	15		20		20		ns	
Data-in setup time	^tDS	0		0		0		ns	21
Data-in hold time	^tDH	10		15		15		ns	21
Data-in hold time (referenced to $\overline{RAS}$)	^tDHR	45		55		60		ns	
Transition time (rise or fall)	^tT	3	50	3	50	3	50	ns	9, 10
Refresh period (2,048 cycles)	^tREF		32		32		32	ms	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	^tRPC	0		0		0		ns	
$\overline{CAS}$ setup time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tCSR	10		10		10		ns	5
$\overline{CAS}$ hold time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tCHR	15		15		15		ns	5
$\overline{WE}$ hold time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tWRH	10		10		10		ns	24
$\overline{WE}$ setup time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tWRP	10		10		10		ns	24
$\overline{WE}$ hold time (WCBR test cycle)	^tWTH	10		10		10		ns	24
$\overline{WE}$ setup time (WCBR test cycle)	^tWTS	10		10		10		ns	24

NOTES

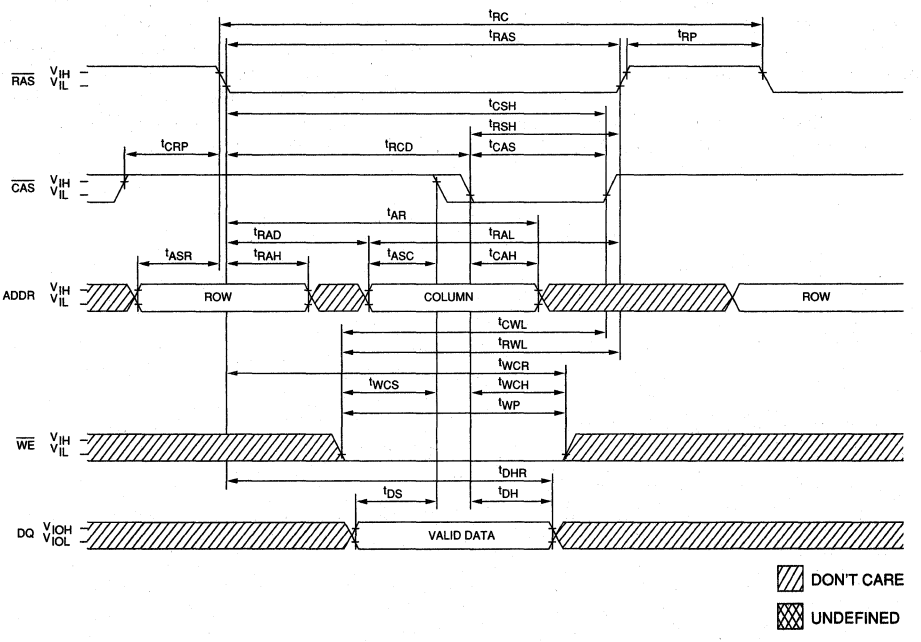
1. All voltages referenced to V_{SS}.
2. This parameter is sampled. Capacitance is measured using MIL-STD-883C, Method 3012.1 (1 MHz AC, Vcc = 5V, DC bias = 2.4V @ 15mV RMS)
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is assured.
7. An initial pause of 100µs is required after power-up followed by eight $\overline{RAS}$ refresh cycles ($\overline{RAS}$-ONLY or CBR with $\overline{WE}$ HIGH) before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-up should be repeated any time the ^{t}REF refresh requirement is exceeded.
8. AC characteristics assume ^{t}T = 5ns.
9. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS}$ = V_{IH}, data output is High-Z.
12. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to 2 TTL gates and 100pF.
14. Assumes that $^{t}RCD < {}^{t}RCD$ (MAX). If ^{t}RCD is greater than the maximum recommended value shown in this table, ^{t}RAC will increase by the amount that ^{t}RCD exceeds the value shown.
15. Assumes that $^{t}RCD \geq {}^{t}RCD$ (MAX).
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer, $\overline{CAS}$ must be pulsed HIGH for ^{t}CPN.
17. Operation within the ^{t}RCD (MAX) limit ensures that ^{t}RAC (MAX) can be met. ^{t}RCD (MAX) is specified as a reference point only; if ^{t}RCD is greater than the specified ^{t}RCD (MAX) limit, then access time is controlled exclusively by ^{t}CAC.
18. Operation within the ^{t}RAD (MAX) limit ensures that ^{t}RCD (MAX) can be met. ^{t}RAD (MAX) is specified as a reference point only; if ^{t}RAD is greater than the specified ^{t}RAD (MAX) limit, then access time is controlled exclusively by ^{t}AA.
19. Either ^{t}RCH or ^{t}RRH must be satisfied for a READ cycle.
20. ^{t}OFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
21. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY-WRITE cycles.
22. $\overline{OE}$ is tied permanently LOW, LATE-WRITE or READ-MODIFY-WRITE operations are not possible.
23. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW and $\overline{OE}$=HIGH.
24. ^{t}WTS and ^{t}WTH are setup and hold specifications for the $\overline{WE}$ pin being held LOW to enable the JEDEC test mode (with CBR timing constraints). These two parameters are the inverts of ^{t}WRP and ^{t}WRH in the CBR refresh cycle.

NEW ■ DRAM MODULE

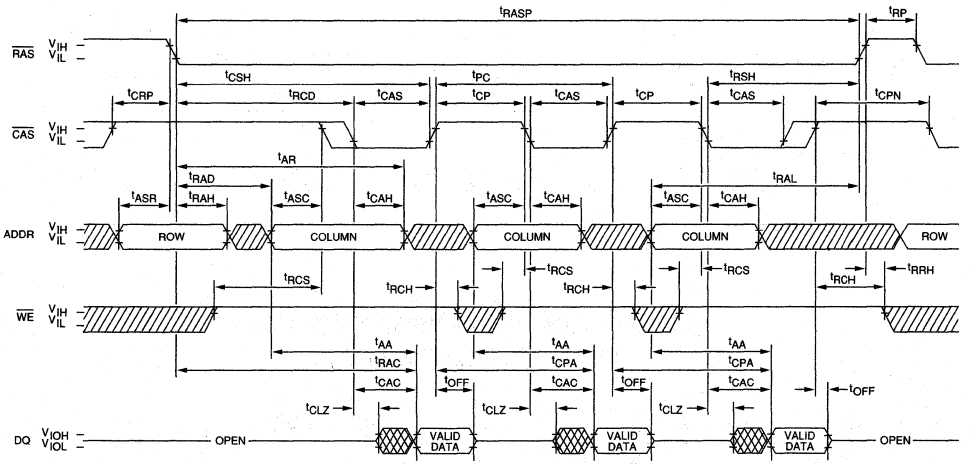
READ CYCLE



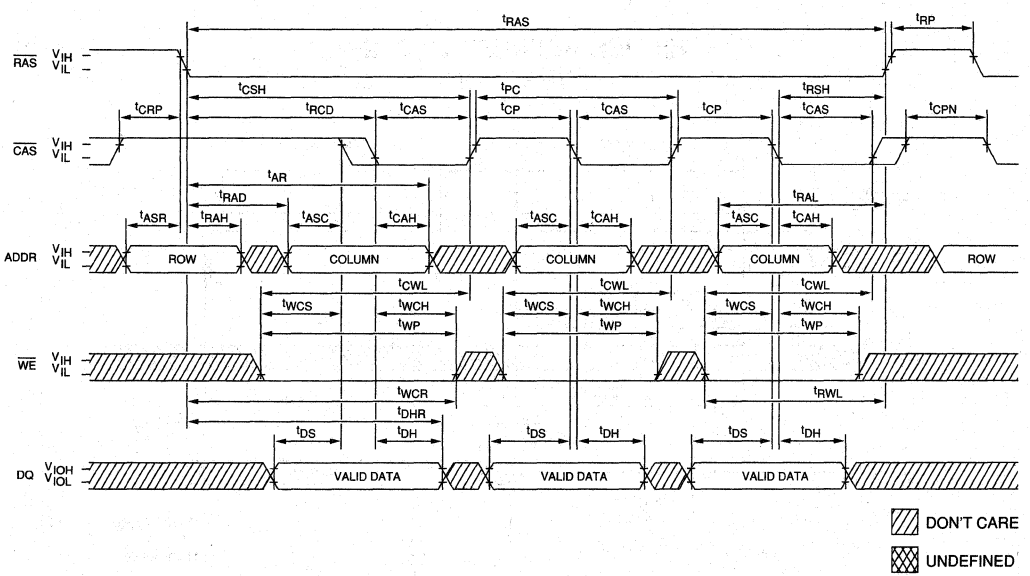
EARLY-WRITE CYCLE



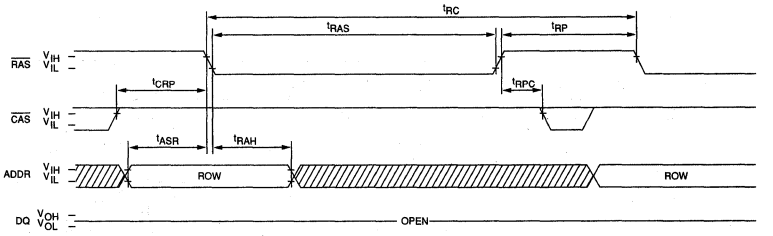
FAST-PAGE-MODE READ CYCLE



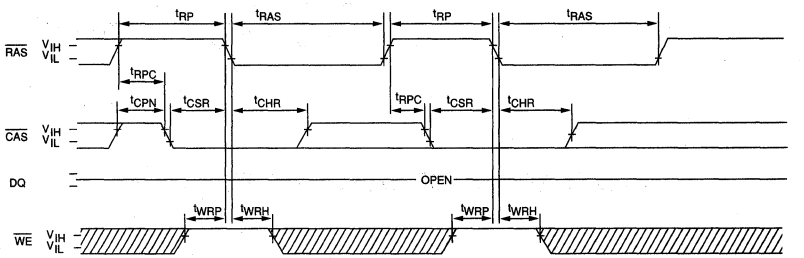
FAST-PAGE-MODE EARLY-WRITE CYCLE



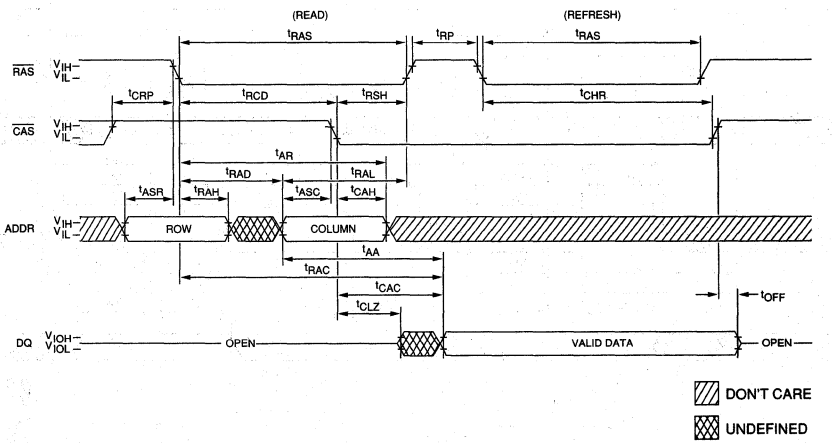
RAS-ONLY REFRESH CYCLE
(ADDR = A0-A10; WE = DON'T CARE)



CAS-BEFORE-RAS REFRESH CYCLE
(A0-A10 = DON'T CARE)



HIDDEN REFRESH CYCLE [23]
(WE = HIGH)



DRAM MODULE

256K x 40 DRAM

FAST PAGE MODE (MT10D25640)
LOW POWER,
EXTENDED REFRESH (MT10D25640 L)

NEW DRAM MODULE

FEATURES

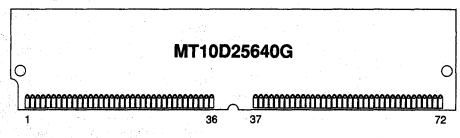
- 72-pin single-in-line package
- High-performance, CMOS silicon-gate process.
- Single 5V ±10% power supply
- All device pins are fully TTL compatible
- Low power, 30mW (3mW L-version) standby; 1,750mW active, typical
- FAST PAGE MODE access cycle
- Refresh modes: $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$ (CBR) and HIDDEN
- 512-cycle refresh distributed across 8ms or 512-cycle extended refresh distributed across 64ms
- Low CMOS standby current, 2mA maximum (L-version)

OPTIONS MARKING

- Timing
  - 60ns access - 6
  - 70ns access - 7
  - 80ns access - 8
- Packages
  - Leadless 72-pin SIMM (Gold) G
- Presence Detect
  - Industry standard Blank
  - Application specific IB
- Power/Refresh
  - Normal power/8ms Blank
  - Low power/64ms L
- Part Number Example: MT10D25640GL-6 IB

PIN ASSIGNMENT (Top View)

72-Pin SIMM
(T-13)



PIN #	SYMBOL	PIN #	SYMBOL	PIN #	SYMBOL	PIN #	SYMBOL
1	Vss	19	$\overline{OE}$	37	DQ34	55	DQ12
2	DQ1	20	DQ5	38	DQ36	56	DQ28
3	DQ17	21	DQ21	39	Vss	57	DQ13
4	DQ2	22	DQ6	40	$\overline{CAS0}$	58	DQ29
5	DQ18	23	DQ22	41	NC	59	Vcc
6	DQ3	24	DQ7	42	NC	60	DQ30
7	DQ19	25	DQ23	43	$\overline{CAS1}$	61	DQ14
8	DQ4	26	DQ8	44	$\overline{RAS0}$	62	DQ31
9	DQ20	27	DQ24	45	NC	63	DQ15
10	Vcc	28	A7	46	DQ38	64	DQ32
11	NC	29	DQ37	47	$\overline{WE}$	65	DQ16
12	A0	30	Vcc	48	Vss	66	DQ39
13	A1	31	A8	49	DQ9	67	PRD1
14	A2	32	NC	50	DQ25	68	PRD2
15	A3	33	NC	51	DQ10	69	PRD3
16	A4	34	NC	52	DQ26	70	PRD4
17	A5	35	DQ35	53	DQ11	71	DQ40
18	A6	36	DQ33	54	DQ27	72	Vss

GENERAL DESCRIPTION

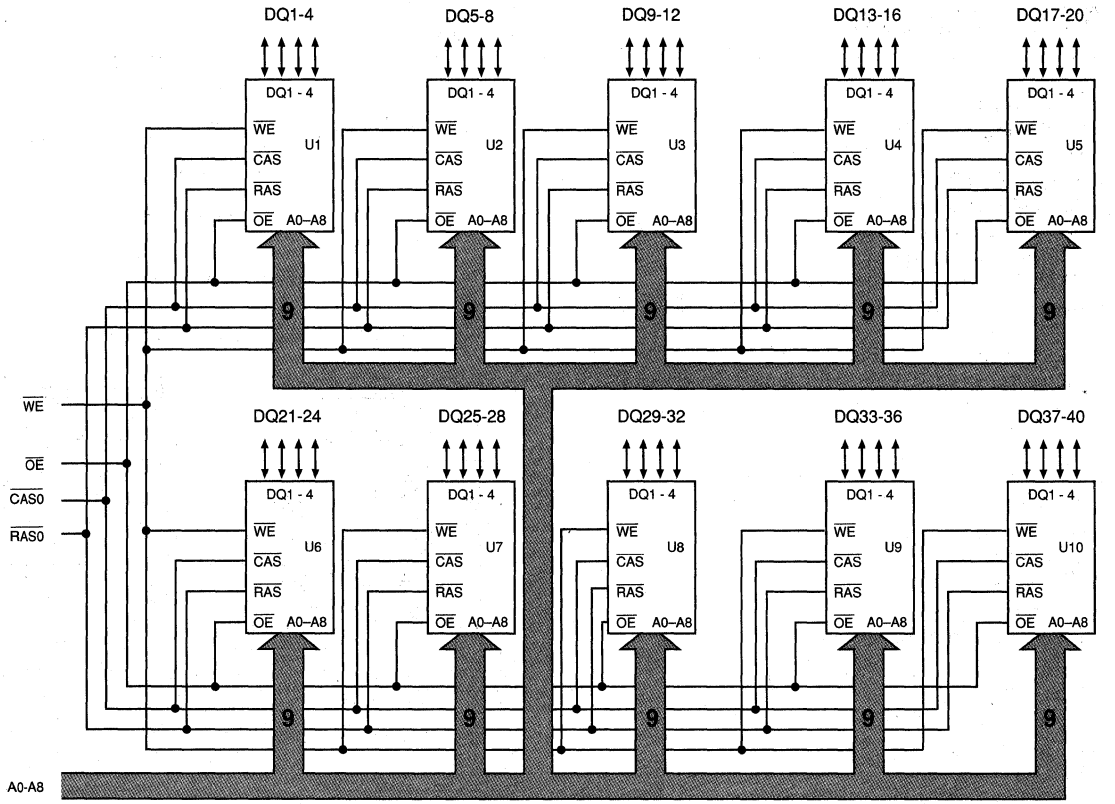
The MT10D25640 is a randomly accessed solid-state memory containing 262,144 words organized in a x40 configuration. During READ or WRITE cycles, each bit is uniquely addressed through the 18 address bits, which are entered 9 bits (A0-A8) at a time. $\overline{RAS}$ is used to latch the first 9 bits and $\overline{CAS}$ the latter 9 bits. READ or WRITE cycles are selected with the $\overline{WE}$ input. A logic HIGH on $\overline{WE}$ dictates READ mode while a logic LOW on $\overline{WE}$ dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. EARLY WRITE occurs when $\overline{WE}$ goes LOW prior to $\overline{CAS}$ going LOW; the output pin(s) remain open (High-Z) until the next $\overline{CAS}$ cycle.

FAST PAGE MODE operations allow faster data operations (READ or WRITE) within a row-address (A0-A8) defined page boundary. The FAST PAGE MODE cycle is always initiated with a row address strobed-in by $\overline{RAS}$ followed by a column address strobed-in by $\overline{CAS}$. $\overline{CAS}$ may be toggled-in by holding $\overline{RAS}$ LOW and strobing-in different column addresses, thus executing faster memory cycles. Returning $\overline{RAS}$ HIGH terminates the FAST PAGE MODE operation.

Returning $\overline{RAS}$ and $\overline{CAS}$ HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the $\overline{RAS}$ high time. Memory cell data is retained in its correct state by maintaining power and executing any $\overline{RAS}$ cycle (READ, WRITE, $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$ or HIDDEN REFRESH) so that all 512 combinations of $\overline{RAS}$ addresses (A0-A8) are executed at least every 8ms (64ms on L-version), regardless of sequence.

NEW ■ DRAM MODULE

FUNCTIONAL BLOCK DIAGRAM



U1-U10 = MT4C4256DJ
U1-U10 = MT4C4256DJ L (L-version)

TRUTH TABLE

FUNCTION		RAS	CAS	WE	OE	ADDRESSES tR	ADDRESSES tC	DATA IN/OUT DQ1-DQ40	NOTES
Standby		H	H→X	X	X	X	X	High-Z	
READ		L	L	H	L	ROW	COL	Data Out	
EARLY-WRITE		L	L	L	X	ROW	COL	Data In	
READ-WRITE		L	L	H→L	L→H	ROW	COL	Data Out, Data In	
FAST-PAGE-MODE	1st Cycle	L	H→L	H	L	ROW	COL	Data Out	
READ	2nd Cycle	L	H→L	H	L	n/a	COL	Data Out	
FAST-PAGE-MODE	1st Cycle	L	H→L	L	X	ROW	COL	Data In	
EARLY-WRITE	2nd Cycle	L	H→L	L	X	n/a	COL	Data In	
FAST-PAGE-MODE	1st Cycle	L	H→L	H→L	L→H	ROW	COL	Data Out, Data In	
READ-WRITE	2nd Cycle	L	H→L	H→L	L→H	n/a	COL	Data Out, Data In	
RAS-ONLY REFRESH		L	H	X	X	ROW	n/a	High-Z	
HIDDEN	READ	L→H→L	L	H	L	ROW	COL	Data Out	
REFRESH	WRITE	L→H→L	L	L	X	ROW	COL	Data In	
CAS-BEFORE-RAS REFRESH		H→L	L	X	X	X	X	High-Z	
BATTERY BACKUP REFRESH		H→L	L	X	X	X	X	High-Z	22

PRESENCE DETECT–INDUSTRY STANDARD

SYMBOL	-6	-7	-8
PRD1	Vss	Vss	Vss
PRD2	NC	NC	NC
PRD3	NC	Vss	NC
PRD4	NC	NC	Vss

PRESENCE DETECT–APPLICATION SPECIFIC

SYMBOL	-6	-7	-8
PRD1	Vss	NC	Vss
PRD2	NC	NC	NC
PRD3	Vss	Vss	NC
PRD4	NC	Vss	Vss

NEW DRAM MODULE

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} ..... -1V to +7V
Operating Temperature, T_A (Ambient) ..... 0°C to +70°C
Storage Temperature (Plastic) ..... -55°C to +125°C
Power Dissipation 10W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 2, 3, 6, 26) (0°C ≤ T_A ≤ 70°C; V_{CC} = 5V ±10%)

PARAMETER/CONDITION		SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage		V_{CC}	4.5	5.5	V	1
Input High (Logic 1) Voltage, All Inputs		V_{IH}	2.4	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, All Inputs		V_{IL}	-1.0	0.8	V	1
INPUT LEAKAGE CURRENT Any Input 0V ≤ V_{IN} ≤ V_{CC} (All other pins not under test = 0V) for each package input	A0-A8, $\overline{WE}$	I_I	-20	20	µA	
	$\overline{RAS}$, $\overline{CAS}$	I_{I2}	-10	10	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled, 0V ≤ V_{OUT} ≤ V_{CC}) for each package input	DQ1-DQ40	I_{OZ}	-10	10	µA	
OUTPUT LEVELS Output High Voltage (I_{OUT} = -5mA)		V_{OH}	2.4		V	
Output Low Voltage (I_{OUT} = 4.2mA)		V_{OL}		0.4	V	

PARAMETER/CONDITION	SYMBOL	MAX -6	MAX -7	MAX -8	UNITS	NOTES
STANDBY CURRENT: (TTL) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC3}	20	20	20	mA	
STANDBY CURRENT: (CMOS) ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} -0.2V)	I_{CC4}	10	10	10	mA	27
		2	2	2	mA	22
OPERATING CURRENT: Random READ/WRITE Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Single Address Cycling: ^tRC = ^tRC (MIN))	I_{CC1}	900	800	700	mA	2, 26
		850	750	650	mA	22
OPERATING CURRENT: FAST PAGE MODE Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: ^tPC = ^tPC (MIN))	I_{CC2}	700	600	500	mA	2, 26
		650	550	450	mA	22
REFRESH CURRENT: $\overline{RAS}$-ONLY Average power supply current ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}: ^tRC = ^tRC (MIN))	I_{CC5}	900	800	700	mA	2
		850	750	650	mA	22
REFRESH CURRENT: $\overline{CAS}$-BEFORE-$\overline{RAS}$ (CBR) Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC (MIN))	I_{CC6}	900	800	700	mA	2, 19
		850	750	650	mA	22
REFRESH CURRENT: BATTERY BACKUP (BBU) Average power supply current during battery backup refresh: $\overline{CAS}$ = 0.2V or $\overline{CAS}$-BEFORE-$\overline{RAS}$ cycling; $\overline{RAS}$ = ^tRAS (MIN) to 1µs; $\overline{WE}$, A0-A8 and D_{IN} = Vcc -0.2V or 0.2V (D_{IN} may be left OPEN), ^tRC = 125µs (512 rows at 125µs = 64ms)	I_{CC7}	2	2	2	mA	22

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A8	C_{I1}		64	pF	17
Input Capacitance: $\overline{WE}$, $\overline{OE}$, $\overline{RAS0}$, $\overline{CAS0}$	C_{I2}		84	pF	17
Input/Output Capacitance: DQ1-DQ40	C_{IO}		10	pF	17

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 3, 4, 5, 6, 7, 10, 11, 16) (V_{CC} = 5V ±10%)

AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	^tRC	110		130		150		ns	
READ-WRITE cycle time	^tRWC	165		185		205		ns	
FAST-PAGE-MODE READ or WRITE cycle time	^tPC	40		40		45		ns	
FAST-PAGE-MODE READ-WRITE cycle time	^tPRWC	90		95		100		ns	
Access time from $\overline{RAS}$	^tRAC		60		70		80	ns	8
Access time from $\overline{CAS}$	^tCAC		20		20		20	ns	9
Output Enable	^tOE		20		20		20	ns	
Access time from column address	^tAA		30		35		40	ns	
Access time from $\overline{CAS}$ precharge	^tCPA		35		40		45	ns	
$\overline{RAS}$ pulse width	^tRAS	60	100,000	70	100,000	80	100,000	ns	
$\overline{RAS}$ pulse width (FAST PAGE MODE)	^tRASP	60	100,000	70	100,000	80	100,000	ns	
$\overline{RAS}$ hold time	^tRSH	20		20		20		ns	
$\overline{RAS}$ precharge time	^tRP	40		50		60		ns	
$\overline{CAS}$ pulse width	^tCAS	20	100,000	20	100,000	20	100,000	ns	
$\overline{CAS}$ hold time	^tCSH	60		70		80		ns	
$\overline{CAS}$ precharge time	^tCPN	10		10		10		ns	18
$\overline{CAS}$ precharge time (FAST PAGE MODE)	^tCP	10		10		10		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	^tRCD	20	40	20	50	20	60	ns	13
$\overline{CAS}$ to $\overline{RAS}$ precharge time	^tCRP	5		5		5		ns	
Row address setup time	^tASR	0		0		0		ns	
Row address hold time	^tRAH	10		10		10		ns	
$\overline{RAS}$ to column address delay time	^tRAD	15	30	15	35	15	40	ns	21
Column address setup time	^tASC	0		0		0		ns	
Column address hold time	^tCAH	15		15		15		ns	
Column address hold time (referenced to $\overline{RAS}$)	^tAR	45		55		60		ns	
Column address to $\overline{RAS}$ lead time	^tRAL	30		35		40		ns	
Read command setup time	^tRCS	0		0		0		ns	
Read command hold time (referenced to $\overline{CAS}$)	^tRCH	0		0		0		ns	14
Read command hold time (referenced to $\overline{RAS}$)	^tRRH	0		0		0		ns	14
$\overline{CAS}$ to output in Low-Z	^tCLZ	0		0		0		ns	

NEW DRAM MODULE

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 3, 4, 5, 6, 7, 10, 11, 16) (Vcc = 5V ±10%)

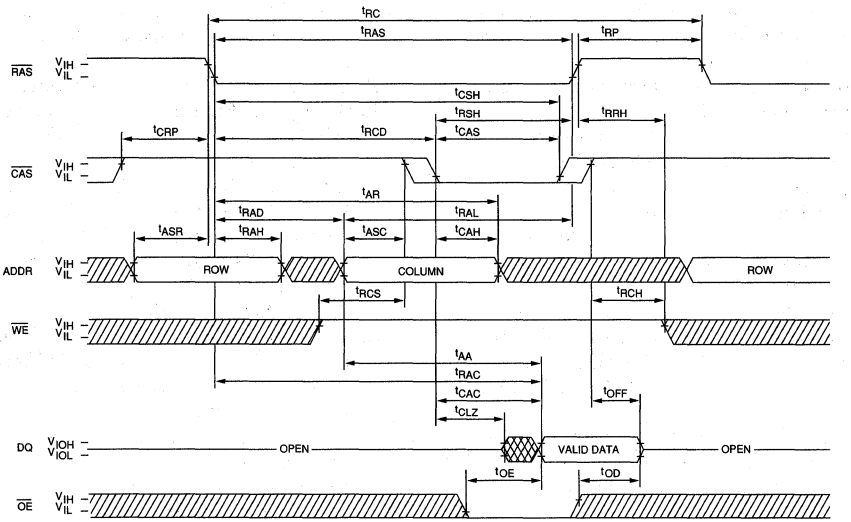
AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Output buffer turn-off delay	^tOFF	0	20	0	20	0	20	ns	12, 23
Output disable	^tOD		15		20		20	ns	23
$\overline{WE}$ command setup time	^tWCS	0		0		0		ns	24
Write command hold time	^tWCH	10		15		15		ns	
Write command hold time (referenced to $\overline{RAS}$)	^tWCR	45		55		60		ns	
Write command pulse width	^tWP	10		15		15		ns	
Write command to $\overline{RAS}$ lead time	^tRWL	20		20		20		ns	
Write command to $\overline{CAS}$ lead time	^tCWL	20		20		20		ns	
Data-in setup time	^tDS	0		0		0		ns	15
Data-in hold time	^tDH	15		15		15		ns	15
Data-in hold time (referenced to $\overline{RAS}$)	^tDHR	45		55		60		ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	^tRWD	85		100		110		ns	24
Column address to $\overline{WE}$ delay time	^tAWD	60		65		70		ns	24
$\overline{CAS}$ to $\overline{WE}$ delay time	^tCWD	40		50		55		ns	24
Transition time (rise or fall)	^tT	3	50	3	50	3	50	ns	5, 16
Refresh period (512 cycles)	^tREF		8/64		8/64		8/64	ms	3/22
$\overline{RAS}$ to $\overline{CAS}$ precharge time	^tRPC	0		0		0		ns	
$\overline{CAS}$ setup time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tCSR	10		10		10		ns	19
$\overline{CAS}$ hold time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tCHR	10		15		15		ns	19
$\overline{OE}$ hold time from $\overline{WE}$ during READ-MODIFY-WRITE cycle	^tOEH	15		20		20		ns	25
$\overline{OE}$ setup prior to $\overline{RAS}$ during HIDDEN REFRESH cycle	^tORD	0		0		0		ns	20

NOTES

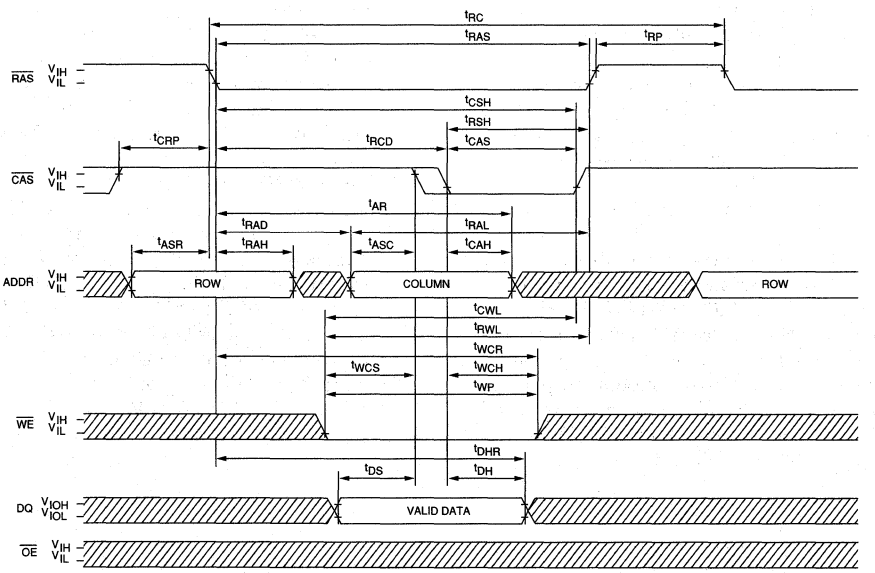
1. All voltages referenced to V_{SS}.
2. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
3. An initial pause of 100µs is required after power-up followed by any eight $\overline{RAS}$ cycles before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-up should be repeated any time the 8ms (64ms L version) refresh requirement is exceeded.
4. AC characteristics assume ^tT = 5ns.
5. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \le T_A \le 70°C$) is assured.
7. Measured with a load equivalent to two TTL gates and 100pF.
8. Assumes that $^tRCD < {}^tRCD$ (MAX). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
9. Assumes that $^tRCD \ge {}^tRCD$ (MAX).
10. If $\overline{CAS}$ = V_{IH}, data output is High-Z.
11. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
12. ^tOFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
13. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (MAX) limit, then access time is controlled exclusively by ^tCAC.
14. Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
15. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY-WRITE cycles and $\overline{WE}$ leading edge in LATE-WRITE or READ-MODIFY-WRITE cycles.
16. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
17. This parameter is sampled. Capacitance is measured using MIL-STD-883C, Method 3012.1 (1 MHz AC, Vcc = 5V, DC bias = 2.4V @ 15mV RMS).
18. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, data-out (Q) will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer, $\overline{CAS}$ must be pulsed HIGH for ^tCP.
19. On-chip refresh and address counters are enabled.
20. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW and $\overline{OE}$ = HIGH.
21. Operation within the ^tRAD (MAX) limit ensures that ^tRCD (MAX) can be met. ^tRAD (MAX) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (MAX) limit, then access time is controlled exclusively by ^tAA.
22. Applies to L-version only.
23. The DQs open during READ cycles once ^tOD or ^tOFF occur. If $\overline{CAS}$ goes HIGH first, $\overline{OE}$ becomes a "don't care." If $\overline{OE}$ goes HIGH and $\overline{CAS}$ stays LOW, $\overline{OE}$ is not a "don't care;" the DQs will provide the previously read data if $\overline{OE}$ is taken back LOW (while $\overline{CAS}$ remains LOW).
24. ^tWCS, ^tRWD, ^tAWD and ^tCWD are restrictive operating parameters in LATE-WRITE, and READ-MODIFY-WRITE cycles only. If $^tWCS \ge {}^tWCS$ (MIN), the cycle is an EARLY-WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If $^tRWD \ge {}^tRWD$ (MIN), $^tAWD \ge {}^tAWD$ (MIN) and $^tCWD \ge {}^tCWD$ (MIN), the cycle is a READ-MODIFY-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions are met, the state of data out is indeterminate. $\overline{OE}$ held HIGH and $\overline{WE}$ taken LOW after $\overline{CAS}$ goes LOW results in a LATE-WRITE ($\overline{OE}$ controlled) cycle.
25. LATE-WRITE and READ-MODIFY-WRITE cycles must have both ^tOD and ^tOEH met ($\overline{OE}$ HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. The DQs will provide the previously read data if $\overline{CAS}$ remains LOW and $\overline{OE}$ is taken back LOW after ^tOEH is met. If $\overline{CAS}$ goes HIGH prior to $\overline{OE}$ going back LOW, the DQs will remain open.
26. I_{CC} is dependent on cycle rates.
27. All other inputs at Vcc -0.2V.

NEW DRAM MODULE

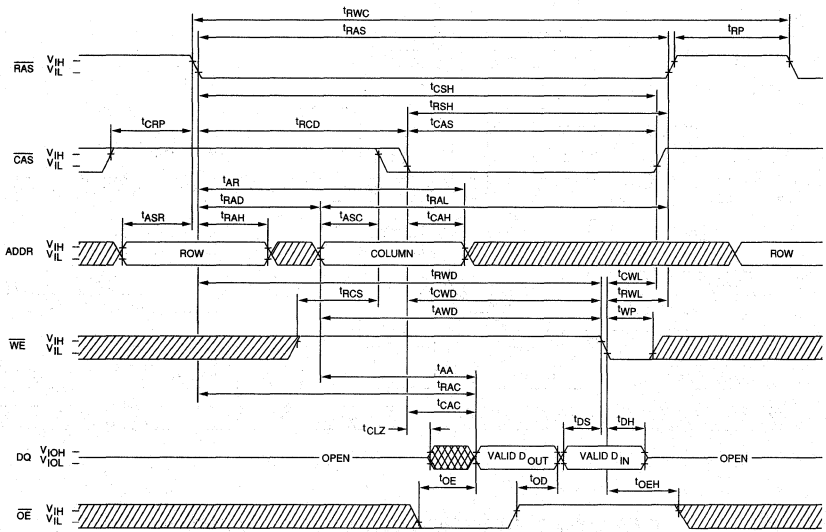
READ CYCLE



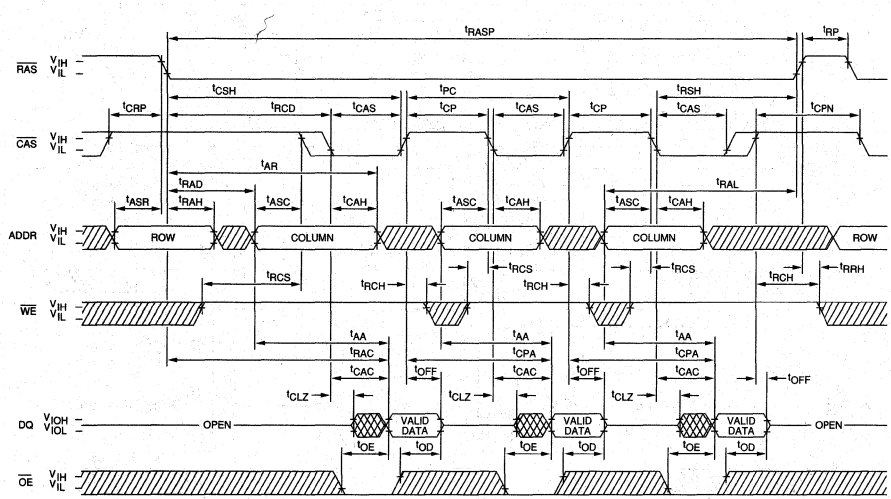
EARLY-WRITE CYCLE



READ-WRITE CYCLE
(LATE WRITE and READ-MODIFY-WRITE CYCLES)

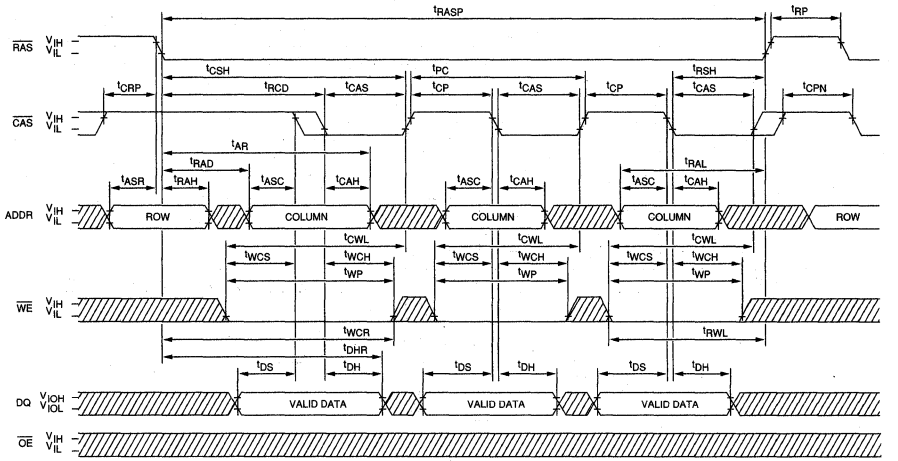


FAST-PAGE-MODE READ CYCLE

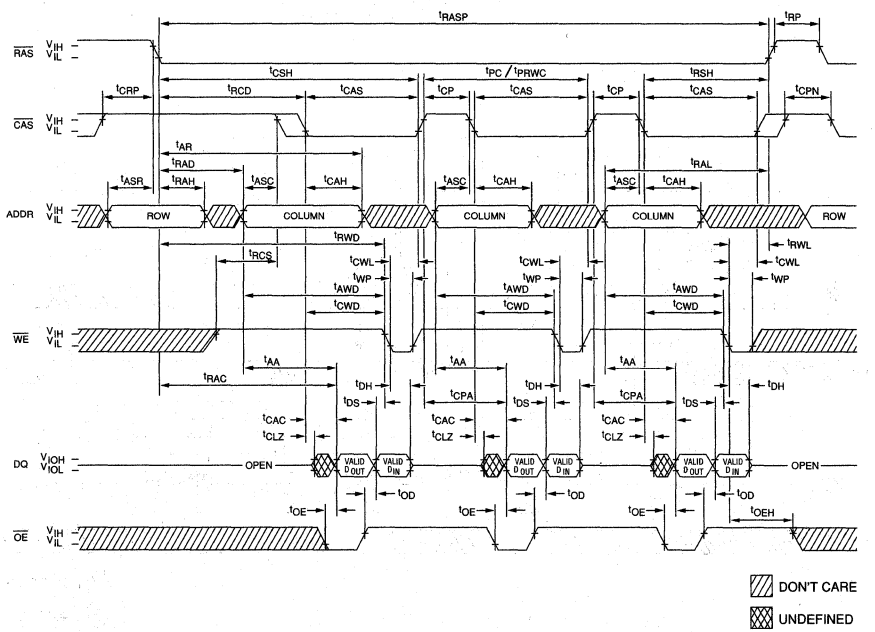


NEW ■ DRAM MODULE

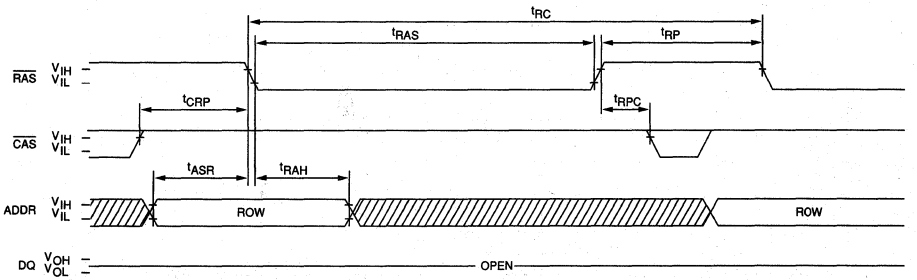
FAST-PAGE-MODE EARLY-WRITE CYCLE



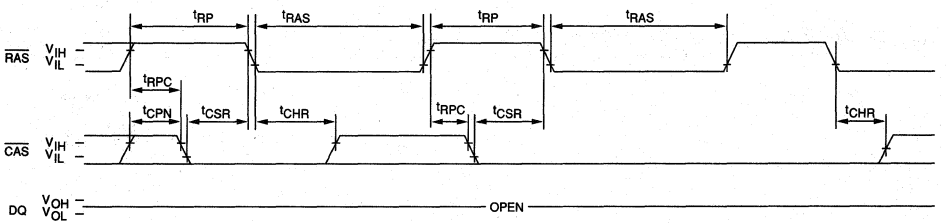
FAST-PAGE-MODE READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)



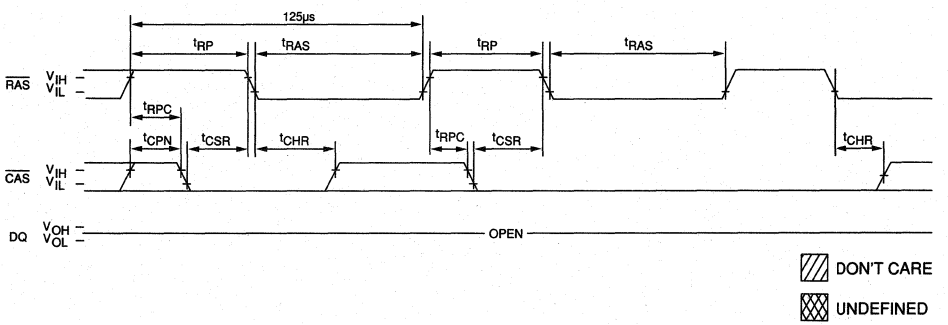
$\overline{RAS}$-ONLY REFRESH CYCLE
(ADDR = A0-A8; $\overline{WE}$ = DON'T CARE)



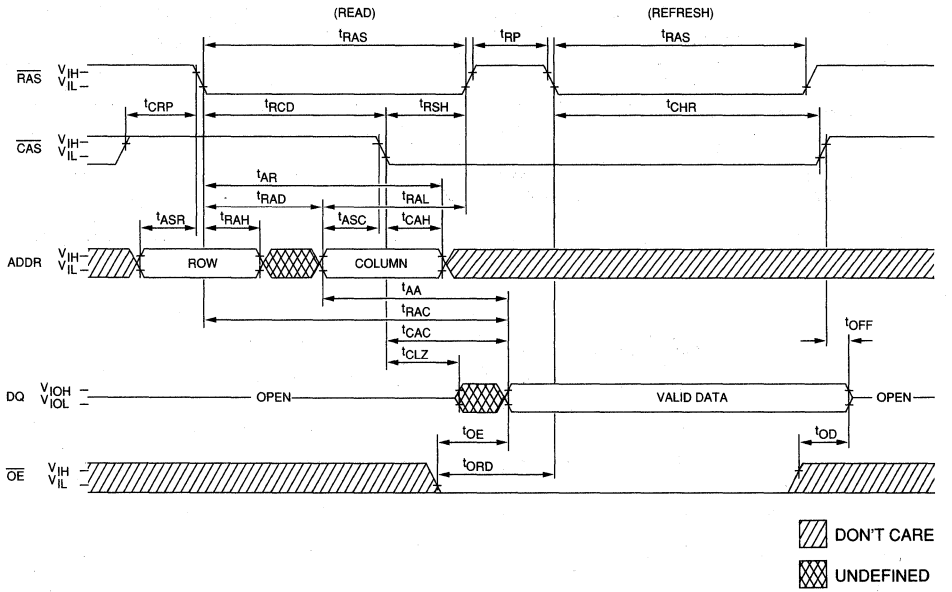
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE
(A0-A8, $\overline{WE}$ and $\overline{OE}$ = DON'T CARE)



BATTERY BACKUP REFRESH CYCLE [22]
($\overline{WE}$ = DON'T CARE)



HIDDEN REFRESH CYCLE [20]
($\overline{WE}$ = HIGH; $\overline{OE}$ = LOW)



DRAM MODULE

512K x 40 DRAM

FAST PAGE MODE (MT20D51240)
LOW POWER,
EXTENDED REFRESH (MT20D51240 L)

NEW ■ DRAM MODULE

FEATURES

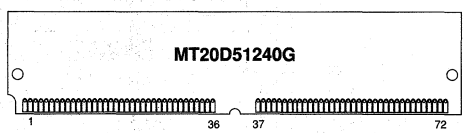
- 72-pin single-in-line package
- High-performance, CMOS silicon-gate process.
- Single 5V ±10% power supply
- All device pins are fully TTL compatible
- Low power, 60mW (6mW L-version) standby; 1,780mW active, typical
- FAST PAGE MODE access cycle
- Refresh modes: $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$ (CBR) and HIDDEN
- 512-cycle refresh distributed across 8ms or 512-cycle extended refresh distributed across 64ms
- Low CMOS standby current, 4mA maximum (L-version)

OPTIONS MARKING

- Timing
  - 60ns access - 6
  - 70ns access - 7
  - 80ns access - 8
- Packages
  - Leadless 72-pin SIMM (Gold) G
- Presence Detect
  - Industry standard Blank
  - Application specific IB
- Power/Refresh
  - Normal power/8ms Blank
  - Low power/64ms L
- Part Number Example: MT20D51240GL-6 IB

PIN ASSIGNMENT (Top View)

72-Pin SIMM
(T-15)



PIN #	SYMBOL	PIN #	SYMBOL	PIN #	SYMBOL	PIN #	SYMBOL
1	Vss	19	$\overline{OE}$	37	DQ34	55	DQ12
2	DQ1	20	DQ5	38	DQ36	56	DQ28
3	DQ17	21	DQ21	39	Vss	57	DQ13
4	DQ2	22	DQ6	40	$\overline{CAS0}$	58	DQ29
5	DQ18	23	DQ22	41	NC	59	Vcc
6	DQ3	24	DQ7	42	NC	60	DQ30
7	DQ19	25	DQ23	43	$\overline{CAS1}$	61	DQ14
8	DQ4	26	DQ8	44	$\overline{RAS0}$	62	DQ31
9	DQ20	27	DQ24	45	$\overline{RAS1}$	63	DQ15
10	Vcc	28	A7	46	DQ38	64	DQ32
11	NC	29	DQ37	47	$\overline{WE}$	65	DQ16
12	A0	30	Vcc	48	Vss	66	DQ39
13	A1	31	A8	49	DQ9	67	PRD1
14	A2	32	NC	50	DQ25	68	PRD2
15	A3	33	NC	51	DQ10	69	PRD3
16	A4	34	NC	52	DQ26	70	PRD4
17	A5	35	DQ35	53	DQ11	71	DQ40
18	A6	36	DQ33	54	DQ27	72	Vss

GENERAL DESCRIPTION

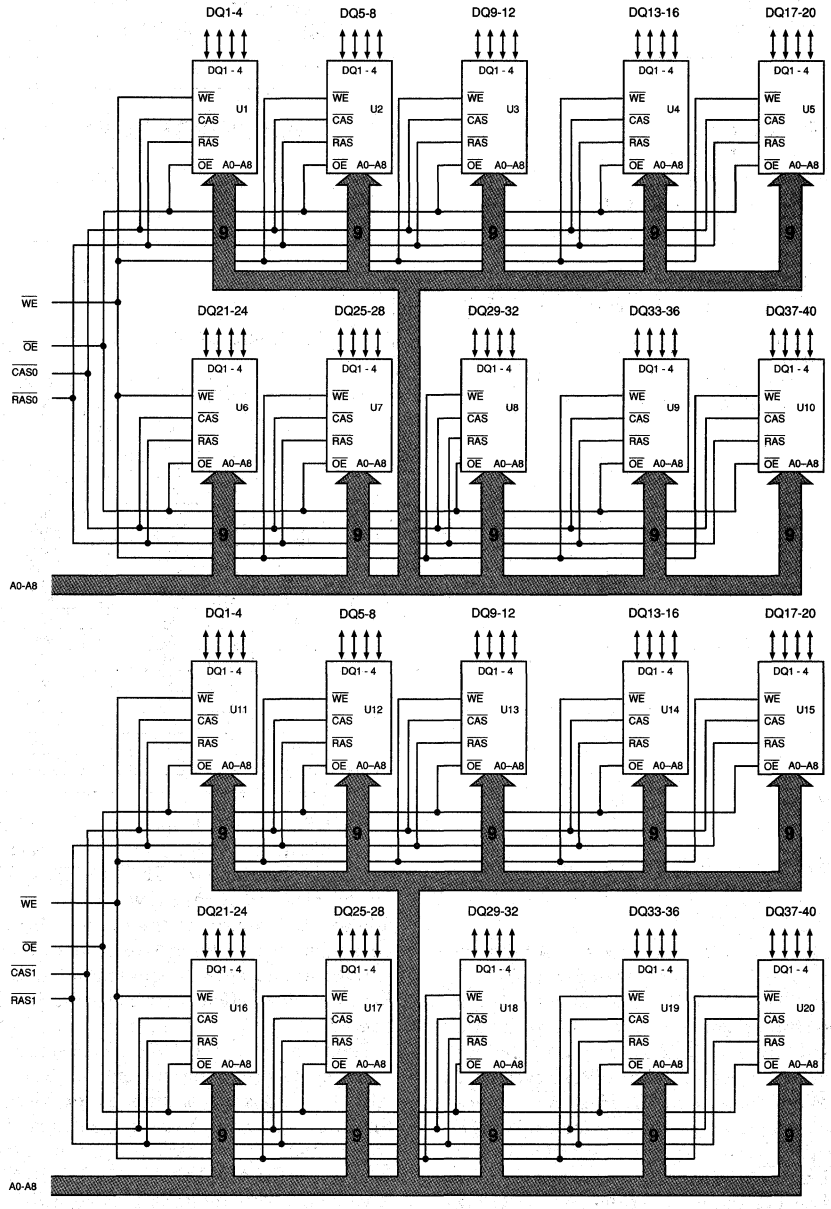
The MT20D51240 is a randomly accessed solid-state memory containing 524,288 words organized in a x40 configuration. During READ or WRITE cycles, each bit is uniquely addressed through the 18 address bits, which are entered 9 bits (A0-A8) at a time. $\overline{RAS}$ is used to latch the first 9 bits and $\overline{CAS}$ the latter 9 bits. READ or WRITE cycles are selected with the $\overline{WE}$ input. A logic HIGH on $\overline{WE}$ dictates READ mode while a logic LOW on $\overline{WE}$ dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. EARLY WRITE occurs when $\overline{WE}$ goes LOW prior to $\overline{CAS}$ going LOW; the output pin(s) remain open (High-Z) until the next $\overline{CAS}$ cycle.

FAST PAGE MODE operations allow faster data operations (READ or WRITE) within a row-address (A0-A8) defined page boundary. The FAST PAGE MODE cycle is always initiated with a row address strobed-in by $\overline{RAS}$ followed by a column address strobed-in by $\overline{CAS}$. $\overline{CAS}$ may be toggled-in by holding $\overline{RAS}$ LOW and strobing-in different column addresses, thus executing faster memory cycles. Returning $\overline{RAS}$ HIGH terminates the FAST PAGE MODE operation.

Returning $\overline{RAS}$ and $\overline{CAS}$ HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the $\overline{RAS}$ high time. Memory cell data is retained in its correct state by maintaining power and executing any $\overline{RAS}$ cycle (READ, WRITE, $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$ or HIDDEN REFRESH) so that all 512 combinations of $\overline{RAS}$ addresses (A0-A8) are executed at least every 8ms (64ms on L version), regardless of sequence.

NEW ■ DRAM MODULE

FUNCTIONAL BLOCK DIAGRAM



U1-U20 = MT4C4256DJ
U1-U20 = MT4C4256DJ L (L-version)

TRUTH TABLE

FUNCTION		RAS	CAS	WE	OE	ADDRESSES tR	ADDRESSES tC	DATA IN/OUT DQ1-DQ40	NOTES
Standby		H	H→X	X	X	X	X	High-Z	
READ		L	L	H	L	ROW	COL	Data Out	
EARLY-WRITE		L	L	L	X	ROW	COL	Data In	
READ-WRITE		L	L	H→L	L→H	ROW	COL	Data Out, Data In	
FAST-PAGE-MODE	1st Cycle	L	H→L	H	L	ROW	COL	Data Out	
READ	2nd Cycle	L	H→L	H	L	n/a	COL	Data Out	
FAST-PAGE-MODE	1st Cycle	L	H→L	L	X	ROW	COL	Data In	
EARLY-WRITE	2nd Cycle	L	H→L	L	X	n/a	COL	Data In	
FAST-PAGE-MODE	1st Cycle	L	H→L	H→L	L→H	ROW	COL	Data Out, Data In	
READ-WRITE	2nd Cycle	L	H→L	H→L	L→H	n/a	COL	Data Out, Data In	
RAS-ONLY REFRESH		L	H	X	X	ROW	n/a	High-Z	
HIDDEN	READ	L→H→L	L	H	L	ROW	COL	Data Out	
REFRESH	WRITE	L→H→L	L	L	X	ROW	COL	Data In	
CAS-BEFORE-RAS REFRESH		H→L	L	H	X	X	X	High-Z	
BATTERY BACKUP REFRESH		H→L	L	X	X	X	X	High-Z	22

PRESENCE DETECT–INDUSTRY STANDARD

SYMBOL	-6	-7	-8
PRD1	NC	NC	NC
PRD2	Vss	Vss	Vss
PRD3	NC	Vss	NC
PRD4	NC	NC	Vss

PRESENCE DETECT–APPLICATION SPECIFIC

SYMBOL	-6	-7	-8
PRD1	NC	Vss	NC
PRD2	NC	Vss	Vss
PRD3	NC	NC	Vss
PRD4	Vss	NC	NC

NEW DRAM MODULE

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} ..... -1V to +7V
Operating Temperature, T_A (Ambient) ..... 0°C to +70°C
Storage Temperature (Plastic) ..... -55°C to +125°C
Power Dissipation 20W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 2, 3, 6, 26) (0°C ≤ T_A ≤ 70°C; V_{CC} = 5V ±10%)

PARAMETER/CONDITION		SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage		V_{CC}	4.5	5.5	V	1
Input High (Logic 1) Voltage, All Inputs		V_{IH}	2.4	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, All Inputs		V_{IL}	-1.0	0.8	V	1
INPUT LEAKAGE CURRENT Any Input 0V ≤ V_{IN} ≤ V_{CC}	A0-A8, $\overline{WE}$	I_I	-40	40	µA	
(All other pins not under test = 0V) for each package input	$\overline{RAS}$, $\overline{CAS}$	I_{I2}	-20	20	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled, 0V ≤ V_{OUT} ≤ V_{CC}) for each package input	DQ1-DQ40	I_{OZ}	-20	20	µA	
OUTPUT LEVELS Output High Voltage (I_{OUT} = -5mA)		V_{OH}	2.4		V	
Output Low Voltage (I_{OUT} = 4.2mA)		V_{OL}		0.4	V	

PARAMETER/CONDITION	SYMBOL	MAX -6	MAX -7	MAX -8	UNITS	NOTES
STANDBY CURRENT: (TTL) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC3}	40	40	40	mA	
STANDBY CURRENT: (CMOS) ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} -0.2V)	I_{CC4}	20	20	20	mA	27
		4	4	4	mA	22
OPERATING CURRENT: Random READ/WRITE ($\overline{RAS}$, $\overline{CAS}$, Single Address Cycling: ^tRC = ^tRC (MIN)) Average power supply current	I_{CC1}	920	820	720	mA	2, 26
		854	754	654	mA	22
OPERATING CURRENT: FAST PAGE MODE Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: ^tPC = ^tPC (MIN))	I_{CC2}	720	620	520	mA	2, 26
		654	554	454	mA	22
REFRESH CURRENT: $\overline{RAS}$-ONLY Average power supply current ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}: ^tRC = ^tRC (MIN))	I_{CC5}	920	820	720	mA	2
		854	754	654	mA	22
REFRESH CURRENT: $\overline{CAS}$-BEFORE-$\overline{RAS}$ (CBR) Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC (MIN))	I_{CC6}	920	820	720	mA	2, 19
		854	754	654	mA	22
REFRESH CURRENT: BATTERY BACKUP (BBU) Average power supply current during battery backup refresh: $\overline{CAS}$ = 0.2V or $\overline{CAS}$-BEFORE-$\overline{RAS}$ cycling; $\overline{RAS}$ = ^tRAS (MIN) to 1µs; $\overline{WE}$, A0-A8 and D_{IN} = Vcc -0.2V or 0.2V (D_{IN} may be left OPEN), ^tRC = 125µs (512 rows at 125µs = 64ms)	I_{CC7}	4	4	4	mA	22

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A8	C_{I1}		128	pF	17
Input Capacitance: $\overline{WE}$, $\overline{OE}$	C_{I2}		168	pF	17
Input Capacitance: $\overline{RAS0}$, $\overline{RAS1}$, $\overline{CAS0}$, $\overline{CAS1}$	C_{I3}		84	pF	17
Input/Output Capacitance: DQ1-DQ40	C_{IO}		20	pF	17

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 3, 4, 5, 6, 7, 10, 11, 16) (V_{CC} = 5V ±10%)

AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	^tRC	110		130		150		ns	
READ-WRITE cycle time	^tRWC	165		185		205		ns	
FAST-PAGE-MODE READ or WRITE cycle time	^tPC	40		40		45		ns	
FAST-PAGE-MODE READ-WRITE cycle time	^tPRWC	90		95		100		ns	
Access time from $\overline{RAS}$	^tRAC		60		70		80	ns	8
Access time from $\overline{CAS}$	^tCAC		20		20		20	ns	9
Output Enable	^tOE		20		20		20	ns	
Access time from column address	^tAA		30		35		40	ns	
Access time from $\overline{CAS}$ precharge	^tCPA		35		40		45	ns	
$\overline{RAS}$ pulse width	^tRAS	60	100,000	70	100,000	80	100,000	ns	
$\overline{RAS}$ pulse width (FAST PAGE MODE)	^tRASP	60	100,000	70	100,000	80	100,000	ns	
$\overline{RAS}$ hold time	^tRSH	20		20		20		ns	
$\overline{RAS}$ precharge time	^tRP	40		50		60		ns	
$\overline{CAS}$ pulse width	^tCAS	20	100,000	20	100,000	20	100,000	ns	
$\overline{CAS}$ hold time	^tCSH	60		70		80		ns	
$\overline{CAS}$ precharge time	^tCPN	10		10		10		ns	18
$\overline{CAS}$ precharge time (FAST PAGE MODE)	^tCP	10		10		10		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	^tRCD	20	40	20	50	20	60	ns	13
$\overline{CAS}$ to $\overline{RAS}$ precharge time	^tCRP	5		5		5		ns	
Row address setup time	^tASR	0		0		0		ns	
Row address hold time	^tRAH	10		10		10		ns	
$\overline{RAS}$ to column address delay time	^tRAD	15	30	15	35	15	40	ns	21
Column address setup time	^tASC	0		0		0		ns	
Column address hold time	^tCAH	15		15		15		ns	
Column address hold time (referenced to $\overline{RAS}$)	^tAR	45		55		60		ns	
Column address to $\overline{RAS}$ lead time	^tRAL	30		35		40		ns	
Read command setup time	^tRCS	0		0		0		ns	
Read command hold time (referenced to $\overline{CAS}$)	^tRCH	0		0		0		ns	14
Read command hold time (referenced to $\overline{RAS}$)	^tRRH	0		0		0		ns	14
$\overline{CAS}$ to output in Low-Z	^tCLZ	0		0		0		ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

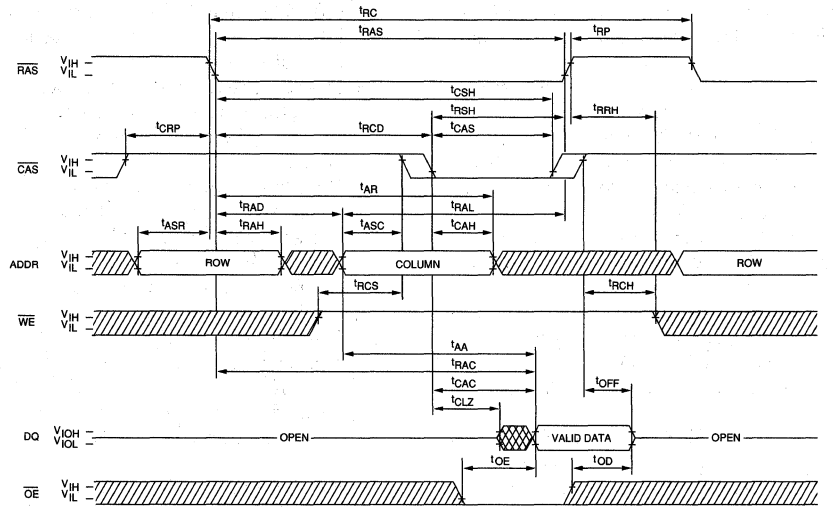
(Notes: 3, 4, 5, 6, 7, 10, 11, 16) (V_{CC} = 5V ±10%)

AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Output buffer turn-off delay	^tOFF	0	20	0	20	0	20	ns	12, 23
Output disable	^tOD		15		20		20	ns	23
$\overline{WE}$ command setup time	^tWCS	0		0		0		ns	24
Write command hold time	^tWCH	10		15		15		ns	
Write command hold time (referenced to $\overline{RAS}$)	^tWCR	45		55		60		ns	
Write command pulse width	^tWP	10		15		15		ns	
Write command to $\overline{RAS}$ lead time	^tRWL	20		20		20		ns	
Write command to $\overline{CAS}$ lead time	^tCWL	20		20		20		ns	
Data-in setup time	^tDS	0		0		0		ns	15
Data-in hold time	^tDH	15		15		15		ns	15
Data-in hold time (referenced to $\overline{RAS}$)	^tDHR	45		55		60		ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	^tRWD	85		100		110		ns	24
Column address to $\overline{WE}$ delay time	^tAWD	60		65		70		ns	24
$\overline{CAS}$ to $\overline{WE}$ delay time	^tCWD	40		50		55		ns	24
Transition time (rise or fall)	^tT	3	50	3	50	3	50	ns	5, 16
Refresh period (512 cycles)	^tREF		8/64		8/64		8/64	ms	3/22
$\overline{RAS}$ to $\overline{CAS}$ precharge time	^tRPC	0		0		0		ns	
$\overline{CAS}$ setup time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tCSR	10		10		10		ns	19
$\overline{CAS}$ hold time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tCHR	10		15		15		ns	19
$\overline{OE}$ hold time from $\overline{WE}$ during READ-MODIFY-WRITE cycle	^tOEH	15		20		20		ns	25
$\overline{OE}$ setup prior to $\overline{RAS}$ during HIDDEN REFRESH cycle	^tORD	0		0		0		ns	20

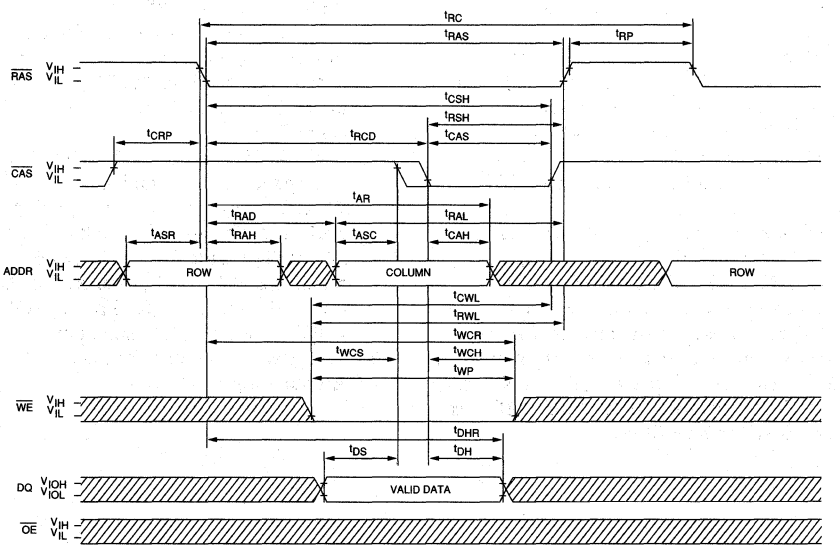
NOTES

1. All voltages referenced to V_{SS}.
2. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
3. An initial pause of 100µs is required after power-up followed by any eight $\overline{RAS}$ cycles before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-up should be repeated any time the 8ms (64ms L version) refresh requirement is exceeded.
4. AC characteristics assume ^tT = 5ns.
5. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is assured.
7. Measured with a load equivalent to two TTL gates and 100pF.
8. Assumes that $^tRCD < ^tRCD$ (MAX). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
9. Assumes that $^tRCD \geq ^tRCD$ (MAX).
10. If $\overline{CAS}$ = V_{IH}, data output is High-Z.
11. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
12. ^tOFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
13. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (MAX) limit, then access time is controlled exclusively by ^tCAC.
14. Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
15. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY-WRITE cycles and $\overline{WE}$ leading edge in LATE-WRITE or READ-MODIFY-WRITE cycles.
16. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
17. This parameter is sampled. Capacitance is measured using MIL-STD-883C, Method 3012.1 (1 MHz AC, Vcc = 5V, DC bias = 2.4V @ 15mV RMS).
18. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, data-out (Q) will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer, $\overline{CAS}$ must be pulsed HIGH for ^tCP.
19. On-chip refresh and address counters are enabled.
20. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW and $\overline{OE}$ = HIGH.
21. Operation within the ^tRAD (MAX) limit ensures that ^tRCD (MAX) can be met. ^tRAD (MAX) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (MAX) limit, then access time is controlled exclusively by ^tAA.
22. Applies to L-version only.
23. The DQs open during READ cycles once ^tOD or ^tOFF occur. If $\overline{CAS}$ goes HIGH first, $\overline{OE}$ becomes a "don't care." If $\overline{OE}$ goes HIGH and $\overline{CAS}$ stays LOW, $\overline{OE}$ is not a "don't care;" the DQs will provide the previously read data if $\overline{OE}$ is taken back LOW (while $\overline{CAS}$ remains LOW).
24. ^tWCS, ^tRWD, ^tAWD and ^tCWD are restrictive operating parameters in LATE-WRITE, and READ-MODIFY-WRITE cycles only. If $^tWCS \geq ^tWCS$ (MIN), the cycle is an EARLY-WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If $^tRWD \geq ^tRWD$ (MIN), $^tAWD \geq ^tAWD$ (MIN) and $^tCWD \geq ^tCWD$ (MIN), the cycle is a READ-MODIFY-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of data out is indeterminate. $\overline{OE}$ held HIGH and $\overline{WE}$ taken LOW after $\overline{CAS}$ goes LOW results in a LATE-WRITE ($\overline{OE}$ controlled) cycle.
25. LATE-WRITE and READ-MODIFY-WRITE cycles must have both ^tOD and ^tOEH met ($\overline{OE}$ HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. The DQs will provide the previously read data if $\overline{CAS}$ remains LOW and $\overline{OE}$ is taken back LOW after ^tOEH is met. If $\overline{CAS}$ goes HIGH prior to $\overline{OE}$ going back LOW, the DQs will remain open.
26. I_{CC} is dependent on cycle rates.
27. All other inputs at Vcc -0.2V.

READ CYCLE

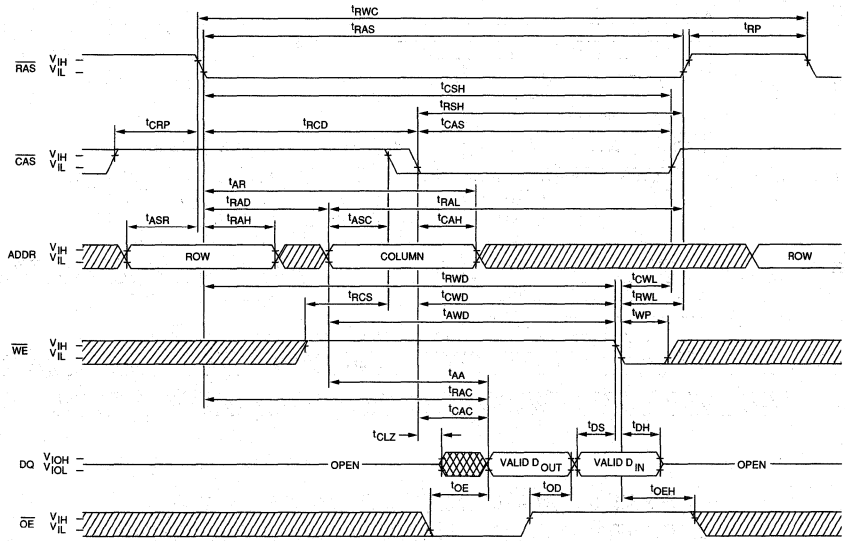


EARLY-WRITE CYCLE

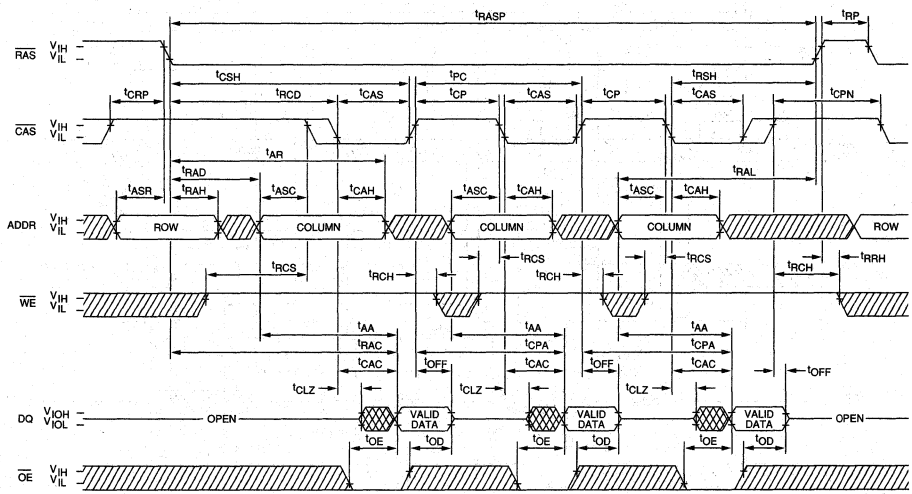


NEW DRAM MODULE

READ-WRITE CYCLE
(LATE WRITE and READ-MODIFY-WRITE CYCLES)

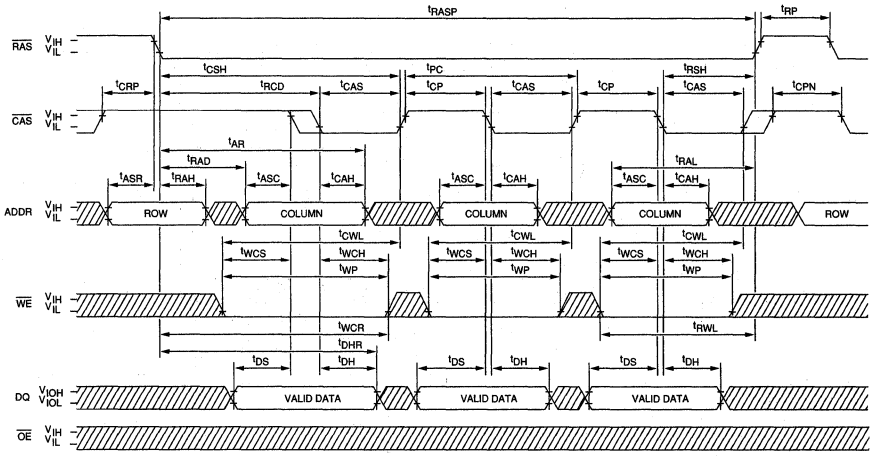


FAST-PAGE-MODE READ CYCLE

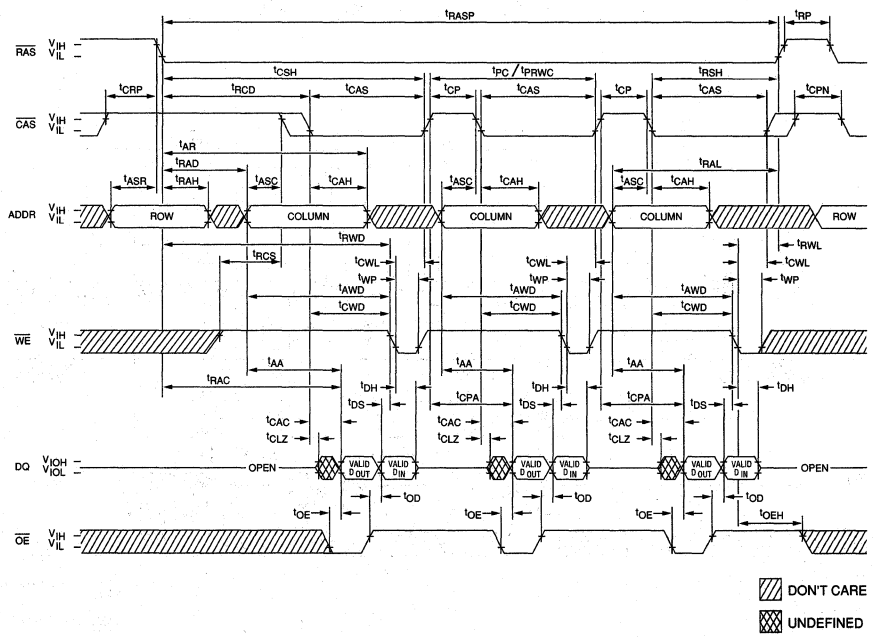


NEW ■ DRAM MODULE

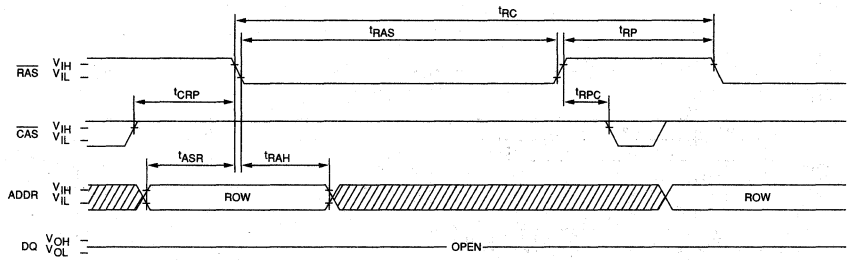
FAST-PAGE-MODE EARLY-WRITE CYCLE



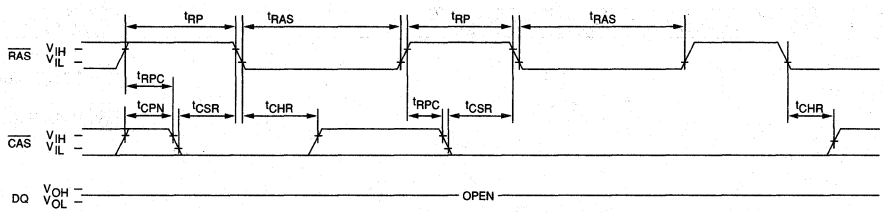
FAST-PAGE-MODE READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)



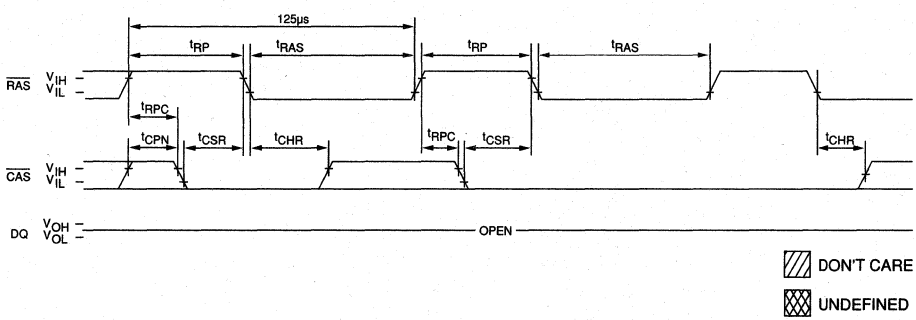
$\overline{\text{RAS}}$-ONLY REFRESH CYCLE
(ADDR = A0-A8; $\overline{\text{WE}}$ = DON'T CARE)



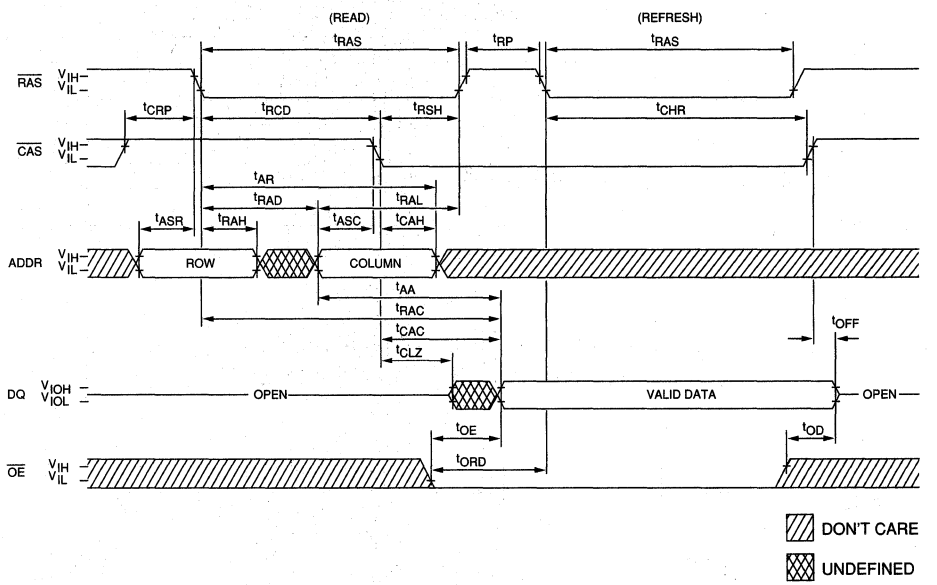
$\overline{\text{CAS}}$-BEFORE-$\overline{\text{RAS}}$ REFRESH CYCLE
(A0-A8, $\overline{\text{WE}}$ and $\overline{\text{OE}}$ = DON'T CARE)



BATTERY BACKUP REFRESH CYCLE [22]
($\overline{\text{WE}}$ = DON'T CARE)



HIDDEN REFRESH CYCLE [20]
($\overline{WE}$ = HIGH; $\overline{OE}$ = LOW)



DRAM MODULE

1 MEG x 40 DRAM

FAST PAGE MODE (MT10D140)
LOW POWER,
EXTENDED REFRESH (MT10D140 L)

NEW DRAM MODULE

FEATURES

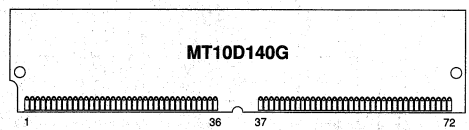
- 72-pin single-in-line package
- High-performance, CMOS silicon-gate process.
- Single 5V ±10% power supply
- All device pins are fully TTL compatible
- Low power, 30mW (10mW L-version) standby; 2,250mW active, typical
- FAST PAGE MODE access cycle
- Refresh modes: $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$ (CBR) and HIDDEN
- 1,024-cycle refresh distributed across 16ms or 1,024-cycle extended refresh distributed across 128ms
- Low CMOS standby current, 2mA maximum (L-version)

OPTIONS / MARKING

- Timing
  - 60ns access - 6
  - 70ns access - 7
  - 80ns access - 8
- Packages
  - Leadless 72-pin SIMM (Gold) G
- Presence Detect
  - Industry standard Blank
  - Application specific IB
- Power/Refresh
  - Normal power/16ms Blank
  - Low power/128ms L
- Part Number Example: MT10D140GL-6 IB

PIN ASSIGNMENT (Top View)

72-Pin SIMM
(T-13)



PIN #	SYMBOL	PIN #	SYMBOL	PIN #	SYMBOL	PIN #	SYMBOL
1	Vss	19	$\overline{OE}$	37	DQ34	55	DQ12
2	DQ1	20	DQ5	38	DQ36	56	DQ28
3	DQ17	21	DQ21	39	Vss	57	DQ13
4	DQ2	22	DQ6	40	$\overline{CAS0}$	58	DQ29
5	DQ18	23	DQ22	41	NC	59	Vcc
6	DQ3	24	DQ7	42	NC	60	DQ30
7	DQ19	25	DQ23	43	$\overline{CAS1}$	61	DQ14
8	DQ4	26	DQ8	44	$\overline{RAS0}$	62	DQ31
9	DQ20	27	DQ24	45	NC	63	DQ15
10	Vcc	28	A7	46	DQ38	64	DQ32
11	NC	29	DQ37	47	$\overline{WE}$	65	DQ16
12	A0	30	Vcc	48	Vss	66	DQ39
13	A1	31	A8	49	DQ9	67	PRD1
14	A2	32	A9	50	DQ25	68	PRD2
15	A3	33	NC	51	DQ10	69	PRD3
16	A4	34	NC	52	DQ26	70	PRD4
17	A5	35	DQ35	53	DQ11	71	DQ40
18	A6	36	DQ33	54	DQ27	72	Vss

GENERAL DESCRIPTION

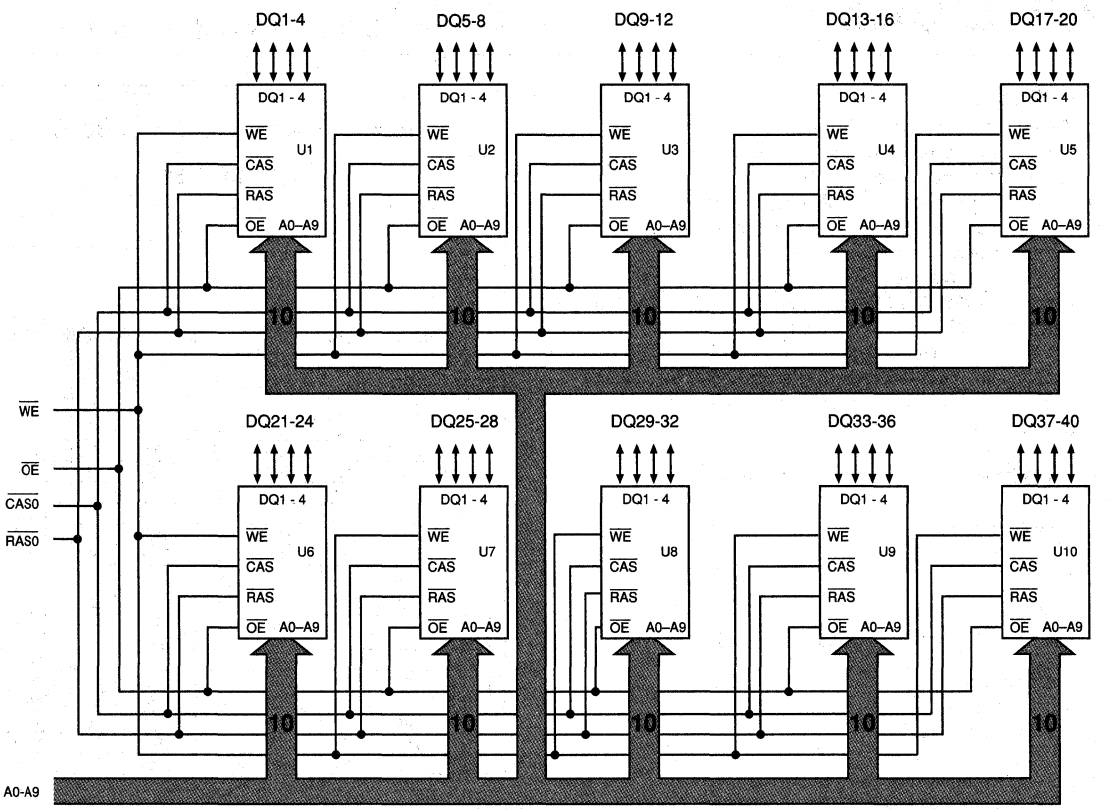
The MT10D140 is a randomly accessed solid-state memory containing 1,048,576 words organized in a x40 configuration. During READ or WRITE cycles, each bit is uniquely addressed through the 20 address bits, which are entered 10 bits (A0-A9) at a time. $\overline{RAS}$ is used to latch the first 10 bits and $\overline{CAS}$ the latter 10 bits. READ or WRITE cycles are selected with the $\overline{WE}$ input. A logic HIGH on $\overline{WE}$ dictates READ mode while a logic LOW on $\overline{WE}$ dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. EARLY WRITE occurs when $\overline{WE}$ goes LOW prior to $\overline{CAS}$ going LOW; the output pin(s) remain open (High-Z) until the next $\overline{CAS}$ cycle.

FAST PAGE MODE operations allow faster data operations (READ or WRITE) within a row-address (A0-A9) defined page boundary. The FAST PAGE MODE cycle is always initiated with a row address strobed-in by $\overline{RAS}$ followed by a column address strobed-in by $\overline{CAS}$. $\overline{CAS}$ may be toggled-in by holding $\overline{RAS}$ LOW and strobing-in different column addresses, thus executing faster memory cycles. Returning $\overline{RAS}$ HIGH terminates the FAST PAGE MODE operation.

Returning $\overline{RAS}$ and $\overline{CAS}$ HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the $\overline{RAS}$ high time. Memory cell data is retained in its correct state by maintaining power and executing any $\overline{RAS}$ cycle (READ, WRITE, $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$ or HIDDEN REFRESH) so that all 1,024 combinations of $\overline{RAS}$ addresses (A0-A9) are executed at least every 16ms (128ms on L-version), regardless of sequence.

NEW ■ DRAM MODULE

FUNCTIONAL BLOCK DIAGRAM



U1-U10 = MT4C4001JDJ
U1-U10 = MT4C4001JDJ L (L-version)

TRUTH TABLE

FUNCTION		RAS	CAS	WE	OE	ADDRESSES		DATA IN/OUT	NOTES
						^tR	^tC	DQ1-DQ40	
Standby		H	H→X	X	X	X	X	High-Z	
READ		L	L	H	L	ROW	COL	Data Out	
EARLY-WRITE		L	L	L	X	ROW	COL	Data In	
READ-WRITE		L	L	H→L	L→H	ROW	COL	Data Out, Data In	
FAST-PAGE-MODE	1st Cycle	L	H→L	H	L	ROW	COL	Data Out	
READ	2nd Cycle	L	H→L	H	L	n/a	COL	Data Out	
FAST-PAGE-MODE	1st Cycle	L	H→L	L	X	ROW	COL	Data In	
EARLY-WRITE	2nd Cycle	L	H→L	L	X	n/a	COL	Data In	
FAST-PAGE-MODE	1st Cycle	L	H→L	H→L	L→H	ROW	COL	Data Out, Data In	
READ-WRITE	2nd Cycle	L	H→L	H→L	L→H	n/a	COL	Data Out, Data In	
RAS-ONLY REFRESH		H	X	X	X	ROW	n/a	High-Z	
HIDDEN	READ	L→H→L	L	H	L	ROW	COL	Data Out	
REFRESH	WRITE	L→H→L	L	L	X	ROW	COL	Data In	
CAS-BEFORE-RAS REFRESH		H→L	L	H	X	X	X	High-Z	
BATTERY BACKUP REFRESH		H→L	L	X	X	X	X	High-Z	22

PRESENCE DETECT–INDUSTRY STANDARD

SYMBOL	-6	-7	-8
PRD1	Vss	Vss	Vss
PRD2	Vss	Vss	Vss
PRD3	NC	Vss	NC
PRD4	NC	NC	Vss

PRESENCE DETECT–APPLICATION SPECIFIC

SYMBOL	-6	-7	-8
PRD1	Vss	Vss	Vss
PRD2	NC	Vss	Vss
PRD3	NC	NC	Vss
PRD4	NC	Vss	Vss

NEW ■ DRAM MODULE

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} ..... -1V to +7V
Operating Temperature, T_A (Ambient) ..... 0°C to +70°C
Storage Temperature (Plastic) ..... -55°C to +125°C
Power Dissipation 10W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 2, 3, 6, 26) (0°C ≤ T_A ≤ 70°C; V_{CC} = 5V ±10%)

PARAMETER/CONDITION		SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage		V_{CC}	4.5	5.5	V	1
Input High (Logic 1) Voltage, All Inputs		V_{IH}	2.4	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, All Inputs		V_{IL}	-1.0	0.8	V	1
INPUT LEAKAGE CURRENT Any Input 0V ≤ V_{IN} ≤ V_{CC}	A0-A9, $\overline{WE}$	I_I	-20	20	µA	
(All other pins not under test = 0V) for each package input	$\overline{RAS}$, $\overline{CAS}$	I_{I2}	-10	10	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled, 0V ≤ V_{OUT} ≤ V_{CC}) for each package input	DQ1-DQ40	I_{OZ}	-10	10	µA	
OUTPUT LEVELS Output High Voltage (I_{OUT} = -5mA)		V_{OH}	2.4		V	
Output Low Voltage (I_{OUT} = 5mA)		V_{OL}		0.4	V	

PARAMETER/CONDITION	SYMBOL	MAX -6	MAX -7	MAX -8	UNITS	NOTES
STANDBY CURRENT: TTL INPUT LEVELS Power supply standby current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH} after 8 $\overline{RAS}$ cycles (MIN))	I_{CC3}	20	20	20	mA	
STANDBY CURRENT: CMOS INPUT LEVELS Power supply standby current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} -0.2V	I_{CC4}	10	10	10	mA	
after 8 $\overline{RAS}$ cycles (MIN)). (All other inputs at V_{CC} -0.2V or V_{SS} +0.2V)		2	2	2	mA	22
OPERATING CURRENT ($\overline{RAS}$ and $\overline{CAS}$ = Cycling: ^tRC = ^tRC (MIN))	I_{CC1}	1100	1000	900	mA	2, 26
OPERATING CURRENT: FAST PAGE MODE ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ = Cycling: ^tPC = ^tPC (MIN))	I_{CC2}	800	700	600	mA	2, 26
REFRESH CURRENT: $\overline{RAS}$-ONLY ($\overline{RAS}$ = Cycling: $\overline{CAS}$ = V_{IH})	I_{CC5}	1100	1000	900	mA	2
REFRESH CURRENT: $\overline{CAS}$-BEFORE-$\overline{RAS}$ ($\overline{RAS}$ and $\overline{CAS}$ = Cycling)	I_{CC6}	1100	1000	900	mA	2, 19
REFRESH CURRENT: BATTERY BACKUP (BBU) Average power supply current during BATTERY BACKUP refresh: $\overline{CAS}$ = 0.2V or $\overline{CAS}$-BEFORE-$\overline{RAS}$ cycling; $\overline{RAS}$ = ^tRAS (MIN) to 300ns; $\overline{WE}$, A0-A9 and D_{IN} = Vcc - 0.2V or 0.2V (D_{IN} may be left open), ^tRC = 125µs (1024 rows at 125µs = 128ms)	I_{CC7}	3	3	3	mA	22

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A9	C_{I1}		64	pF	17
Input Capacitance: $\overline{WE}$, $\overline{OE}$, $\overline{RAS0}$, $\overline{CAS0}$	C_{I2}		84	pF	17
Input/Output Capacitance: DQ1-DQ40	C_{IO}		10	pF	17

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 3, 4, 5, 6, 7, 10, 11, 16) (V_{CC} = 5V ±10%)

AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	t_{RC}	110		130		150		ns	
READ-WRITE cycle time	t_{RWC}	165		185		205		ns	
FAST-PAGE-MODE READ or WRITE cycle time	t_{PC}	40		40		45		ns	
FAST-PAGE-MODE READ-WRITE cycle time	t_{PRWC}	90		95		100		ns	
Access time from $\overline{RAS}$	t_{RAC}		60		70		80	ns	8
Access time from $\overline{CAS}$	t_{CAC}		15		20		20	ns	9
Access time from column address	t_{AA}		30		35		40	ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		35		40		45	ns	
$\overline{RAS}$ pulse width	t_{RAS}	60	100,000	70	100,000	80	100,000	ns	
$\overline{RAS}$ pulse width (FAST PAGE MODE)	t_{RASP}	60	100,000	70	100,000	80	100,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	15		20		20		ns	
$\overline{RAS}$ precharge time	t_{RP}	45		50		60		ns	
$\overline{CAS}$ pulse width	t_{CAS}	15	100,000	20	100,000	20	100,000	ns	
$\overline{CAS}$ hold time	t_{CSH}	60		70		80		ns	
$\overline{CAS}$ precharge time	t_{CPN}	10		10		10		ns	18
$\overline{CAS}$ precharge time (FAST PAGE MODE)	t_{CP}	10		10		10		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	40	20	50	20	60	ns	13
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		10		10		ns	
Row address setup time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	10		10		10		ns	
$\overline{RAS}$ to column address delay time	t_{RAD}	15	30	15	35	15	40	ns	21
Column address setup time	t_{ASC}	0		0		0		ns	
Column address hold time	t_{CAH}	10		15		15		ns	
Column address hold time (referenced to $\overline{RAS}$)	t_{AR}	50		55		60		ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	30		35		40		ns	
Read command setup time	t_{RCS}	0		0		0		ns	
Read command hold time (referenced to $\overline{CAS}$)	t_{RCH}	0		0		0		ns	14
Read command hold time (referenced to $\overline{RAS}$)	t_{RRH}	0		0		0		ns	14
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	0		0		0		ns	
Output buffer turn-off delay	t_{OFF}	0	20	0	20	0	20	ns	12, 23
$\overline{WE}$ command setup time	t_{WCS}	0		0		0		ns	24

NEW DRAM MODULE

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 3, 4, 5, 6, 7, 10, 11, 16) (V_{CC} = 5V ±10%)

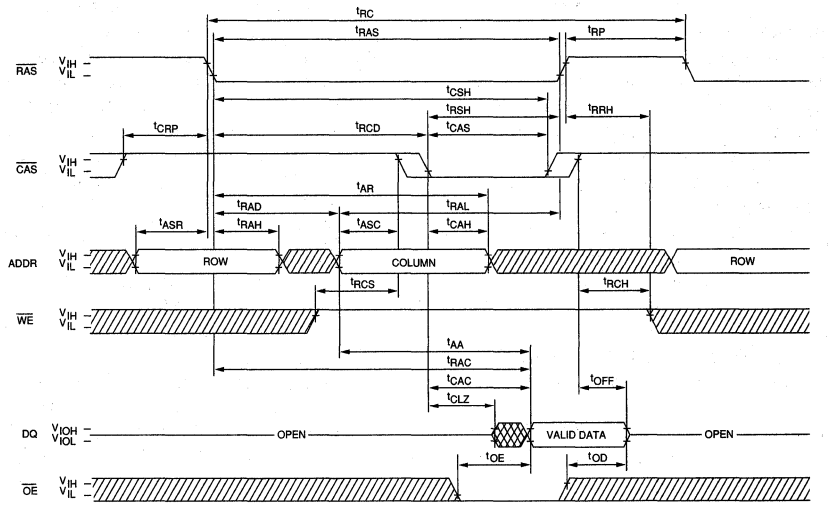
AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Write command hold time	^tWCH	10		15		15		ns	
Write command hold time (referenced to $\overline{RAS}$)	^tWCR	45		55		60		ns	
Write command pulse width	^tWP	10		15		15		ns	
Write command to $\overline{RAS}$ lead time	^tRWL	15		20		20		ns	
Write command to $\overline{CAS}$ lead time	^tCWL	15		20		20		ns	
Data-in setup time	^tDS	0		0		0		ns	15
Data-in hold time	^tDH	10		15		15		ns	15
Data-in hold time (referenced to $\overline{RAS}$)	^tDHR	45		55		60		ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	^tRWD	90		100		110		ns	24
Column address to $\overline{WE}$ delay time	^tAWD	60		65		70		ns	24
$\overline{CAS}$ to $\overline{WE}$ delay time	^tCWD	45		50		50		ns	24
Transition time (rise or fall)	^tT	3	50	3	50	3	50	ns	5, 16
Refresh period (1024 cycles)	^tREF		16/128		16/128		16/128	ms	3/22
$\overline{RAS}$ to $\overline{CAS}$ precharge time	^tRPC	0		0		0		ns	19
$\overline{CAS}$ setup time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tCSR	10		10		10		ns	19
$\overline{CAS}$ hold time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tCHR	15		15		15		ns	19
$\overline{OE}$ setup prior to RAS during HIDDEN REFRESH cycle	^tORD	0		0		0		ns	20
Output disable	^tOD	15		20		20		ns	23
Output enable	^tOE	15		20		20		ns	
$\overline{OE}$ hold time from $\overline{WE}$ during READ-MODIFY-WRITE cycle	^tOEH	15		20		20		ns	25

NOTES

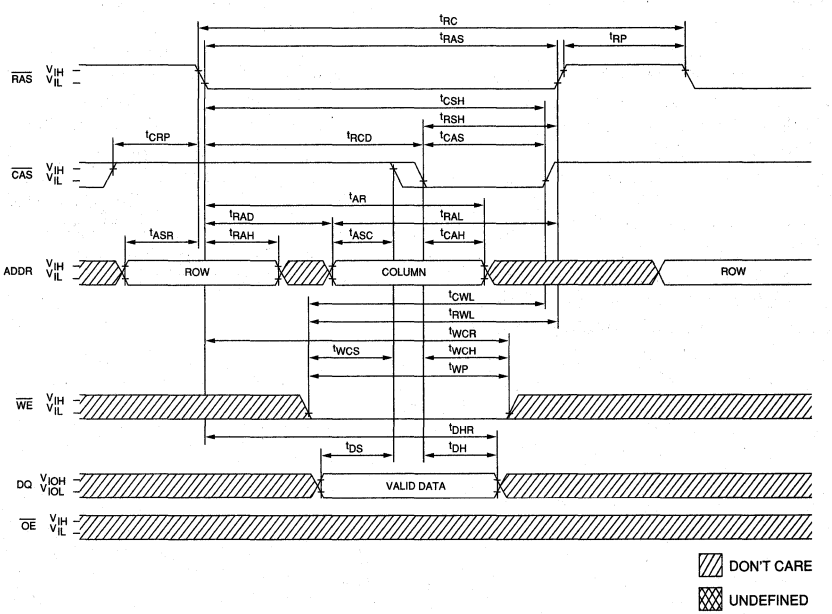
1. All voltages referenced to V_{SS}.
2. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
3. An initial pause of 100µs is required after power-up followed by any eight $\overline{RAS}$ cycles before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-up should be repeated any time the 16ms (128ms L version) refresh requirement is exceeded.
4. AC characteristics assume ^tT = 5ns.
5. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \le T_A \le 70°C$) is assured.
7. Measured with a load equivalent to two TTL gates and 100pF.
8. Assumes that $^tRCD < {}^tRCD$ (MAX). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
9. Assumes that $^tRCD \ge {}^tRCD$ (MAX).
10. If $\overline{CAS}$ = V_{IH}, data output is High-Z.
11. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
12. ^tOFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
13. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (MAX) limit, then access time is controlled exclusively by ^tCAC.
14. Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
15. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY-WRITE cycles.
16. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
17. This parameter is sampled. Capacitance is measured using MIL-STD-883C, Method 3012.1 (1 MHz AC, Vcc = 5V, DC bias = 2.4V @ 15mV RMS).
18. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, data-out (Q) will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer, $\overline{CAS}$ must be pulsed HIGH for ^tCP.
19. On-chip refresh and address counters are enabled.
20. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW.
21. Operation within the ^tRAD (MAX) limit ensures that ^tRCD (MAX) can be met. ^tRAD (MAX) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (MAX) limit, then access time is controlled exclusively by ^tAA.
22. L-version only.
23. ^tWCS, ^tRWD, ^tAWD and ^tCWD are restrictive operating parameters in LATE-WRITE, and READ-MODIFY-WRITE cycles only. If $^tWCS \ge {}^tWCS$ (MIN), the cycle is an EARLY-WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If $^tRWD \ge {}^tRWD$ (MIN), $^tAWD \ge {}^tAWD$ (MIN) and $^tCWD \ge {}^tCWD$ (MIN), the cycle is a READ-MODIFY-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions are met, the state of data out is indeterminate. $\overline{OE}$ held HIGH and $\overline{WE}$ taken LOW after $\overline{CAS}$ goes LOW results in a LATE-WRITE ($\overline{OE}$ controlled) cycle.
24. LATE-WRITE and READ-MODIFY-WRITE cycles must have both ^tOD and ^tOEH met ($\overline{OE}$ HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. The DQs will provide the previously read data if $\overline{CAS}$ remains LOW and $\overline{OE}$ is taken back LOW after ^tOEH is met. If $\overline{CAS}$ goes HIGH prior to $\overline{OE}$ going back LOW, the DQs will remain open.
25. I_{CC} is dependent on cycle rates.
26. All other inputs at Vcc -0.2V.

NEW DRAM MODULE

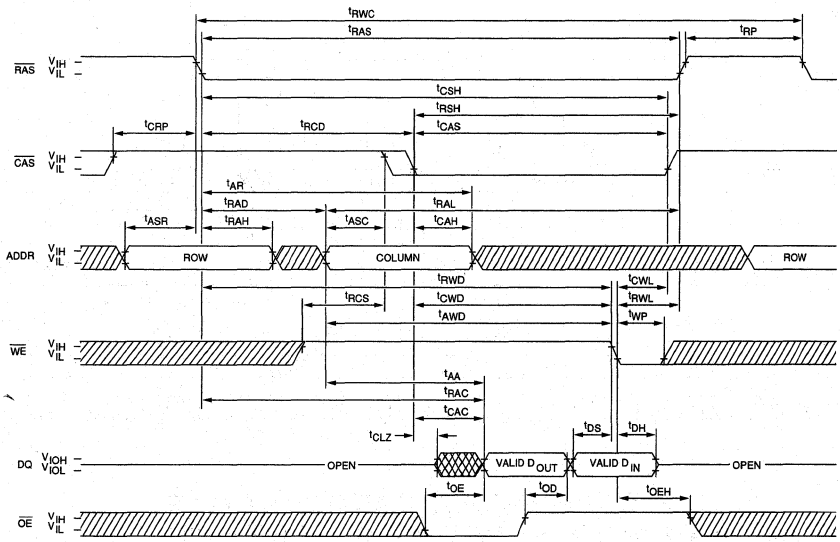
READ CYCLE



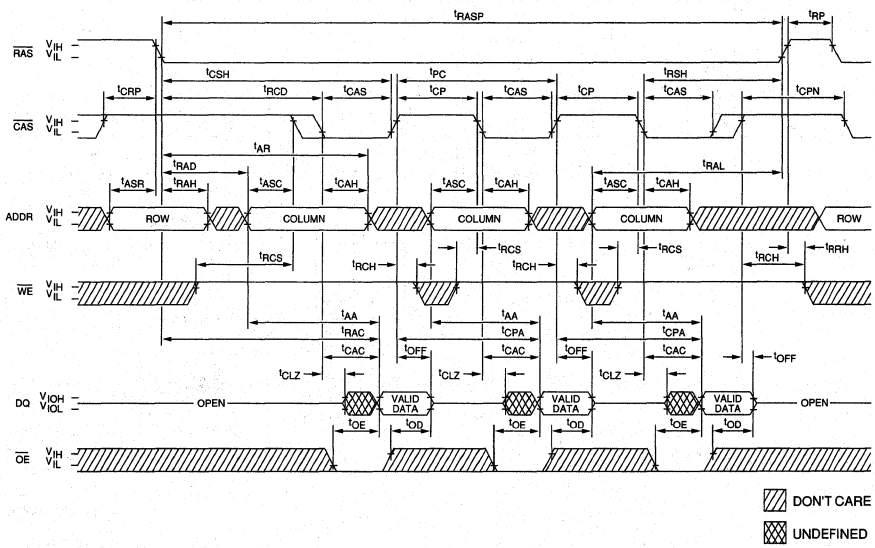
EARLY-WRITE CYCLE



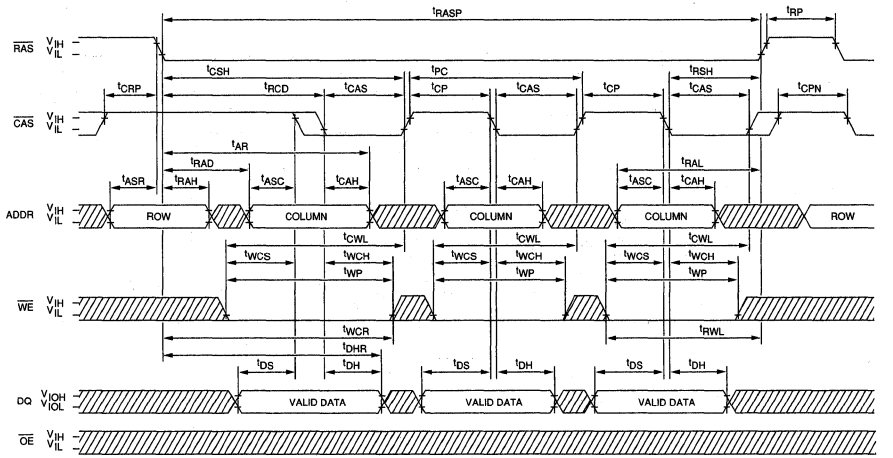
READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)



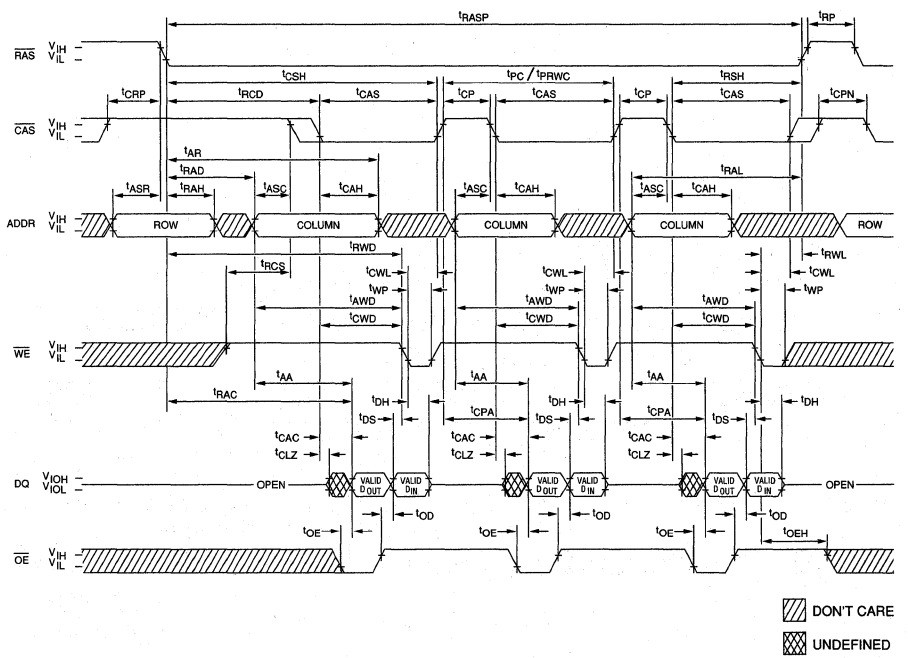
FAST-PAGE-MODE READ CYCLE



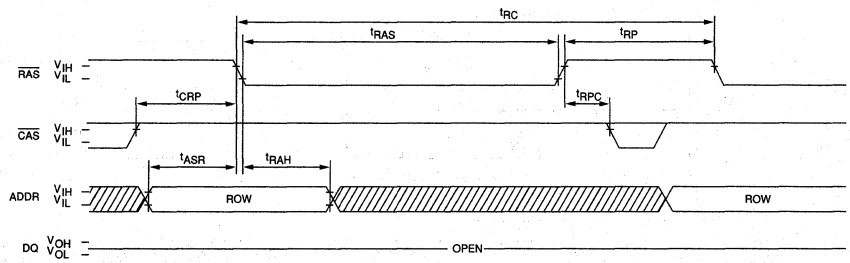
FAST-PAGE-MODE EARLY-WRITE CYCLE



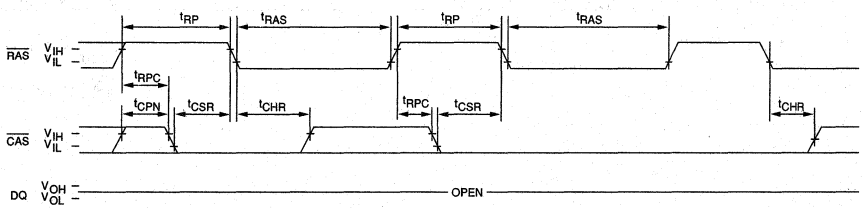
FAST-PAGE-MODE READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)



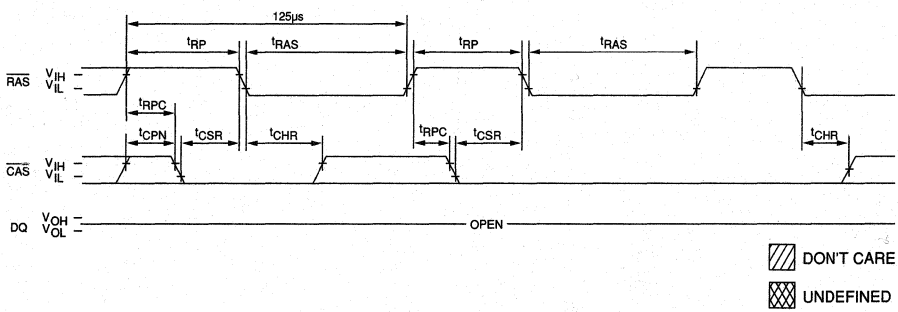
$\overline{\text{RAS}}$-ONLY REFRESH CYCLE
(ADDR = A0-A9; and $\overline{\text{WE}}$ = DON'T CARE)



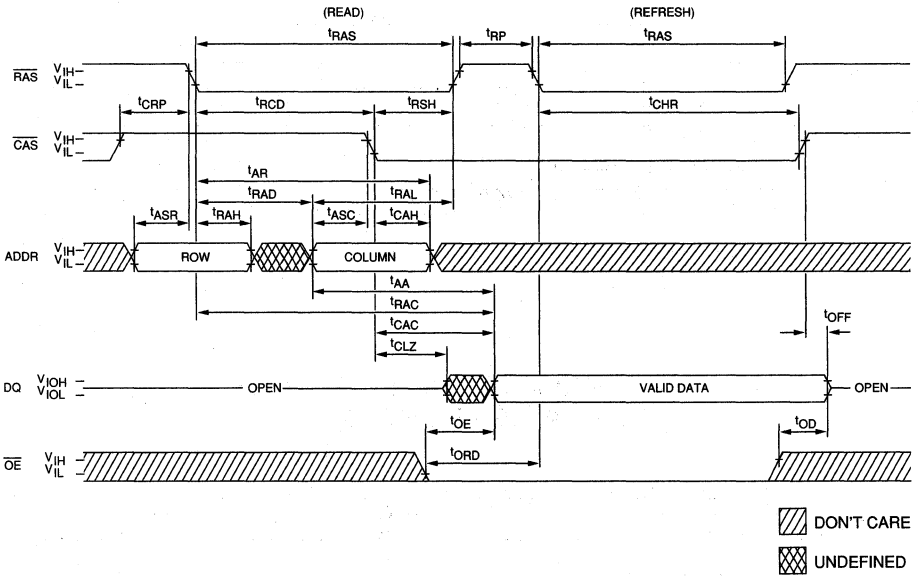
$\overline{\text{CAS}}$-BEFORE-$\overline{\text{RAS}}$ REFRESH CYCLE
(A0-A9, $\overline{\text{OE}}$ = DON'T CARE)



BATTERY BACKUP REFRESH CYCLE [22]
($\overline{\text{WE}}$ = DON'T CARE)



HIDDEN REFRESH CYCLE [20]
($\overline{WE}$ = HIGH; $\overline{OE}$ = LOW)



DRAM MODULE

2 MEG x 40 DRAM

FAST PAGE MODE (MT20D240)
LOW POWER,
EXTENDED REFRESH (MT20D240 L)

NEW DRAM MODULE

FEATURES

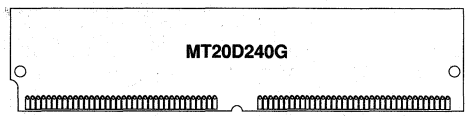
- 72-pin single-in-line package
- High-performance CMOS silicon-gate process.
- Single 5V ±10% power supply
- All device pins are fully TTL compatible
- Low power, 60mW (20mW L-version) standby; 2,280mW active, typical
- FAST PAGE MODE access cycle
- Refresh modes: $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$ (CBR) and HIDDEN
- 1,024-cycle refresh distributed across 16ms or 1,024-cycle extended refresh distributed across 128ms (L-version)
- Low CMOS standby current, 4mA maximum (L-version)

OPTIONS — MARKING

- Timing
  - 60ns access — -6
  - 70ns access — -7
  - 80ns access — -8
- Packages
  - Leadless 72-pin SIMM (Gold) — G
- Presence Detect
  - Industry standard — Blank
  - Application specific — IB
- Power/Refresh
  - Normal power/16ms — Blank
  - Low power/128ms — L
- Part Number Example: MT20D240GL-6 IB

PIN ASSIGNMENT (Top View)

72-Pin SIMM
(T-15)



PIN #	SYMBOL	PIN #	SYMBOL	PIN #	SYMBOL	PIN #	SYMBOL
1	Vss	19	$\overline{OE}$	37	DQ34	55	DQ12
2	DQ1	20	DQ5	38	DQ36	56	DQ28
3	DQ17	21	DQ21	39	Vss	57	DQ13
4	DQ2	22	DQ6	40	$\overline{CAS0}$	58	DQ29
5	DQ18	23	DQ22	41	NC	59	Vcc
6	DQ3	24	DQ7	42	NC	60	DQ30
7	DQ19	25	DQ23	43	$\overline{CAS1}$	61	DQ14
8	DQ4	26	DQ8	44	$\overline{RAS0}$	62	DQ31
9	DQ20	27	DQ24	45	$\overline{RAS1}$	63	DQ15
10	Vcc	28	A7	46	DQ38	64	DQ32
11	NC	29	DQ37	47	$\overline{WE}$	65	DQ16
12	A0	30	Vcc	48	Vss	66	DQ39
13	A1	31	A8	49	DQ9	67	PRD1
14	A2	32	A9	50	DQ25	68	PRD2
15	A3	33	NC	51	DQ10	69	PRD3
16	A4	34	NC	52	DQ26	70	PRD4
17	A5	35	DQ35	53	DQ11	71	DQ40
18	A6	36	DQ33	54	DQ27	72	Vss

GENERAL DESCRIPTION

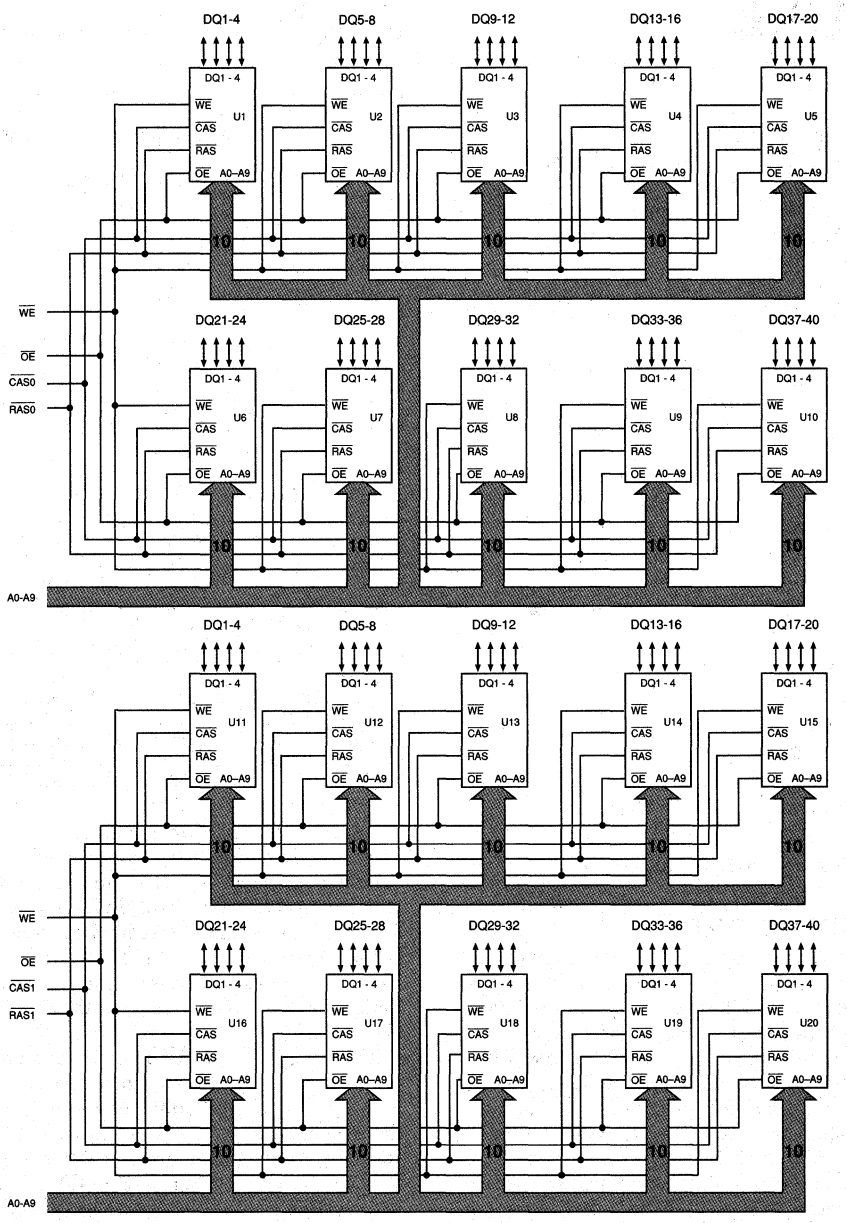
The MT20D240 is a randomly accessed solid-state memory containing 2,097,152 words organized in a x40 configuration. During READ or WRITE cycles, each bit is uniquely addressed through the 20 address bits, which are entered 10 bits (A0-A9) at a time. $\overline{RAS}$ is used to latch the first 10 bits and $\overline{CAS}$ the latter 10 bits. READ or WRITE cycles are selected with the $\overline{WE}$ input. A logic HIGH on $\overline{WE}$ dictates READ mode while a logic LOW on $\overline{WE}$ dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. EARLY WRITE occurs when $\overline{WE}$ goes LOW prior to $\overline{CAS}$ going LOW; the output pin(s) remain open (High-Z) until the next $\overline{CAS}$ cycle.

FAST PAGE MODE operations allow faster data operations (READ or WRITE) within a row-address (A0-A9) defined page boundary. The FAST PAGE MODE cycle is always initiated with a row address strobed-in by $\overline{RAS}$ followed by a column address strobed-in by $\overline{CAS}$. $\overline{CAS}$ may be toggled-in by holding $\overline{RAS}$ LOW and strobing-in different column addresses, thus executing faster memory cycles. Returning $\overline{RAS}$ HIGH terminates the FAST PAGE MODE operation.

Returning $\overline{RAS}$ and $\overline{CAS}$ HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the $\overline{RAS}$ high time. Memory cell data is retained in its correct state by maintaining power and executing any $\overline{RAS}$ cycle (READ, WRITE, $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$ or HIDDEN REFRESH) so that all 1,024 combinations of $\overline{RAS}$ addresses (A0-A9) are executed at least every 16ms (128ms on L-version), regardless of sequence.

NEW DRAM MODULE

FUNCTIONAL BLOCK DIAGRAM



U1-U20 = MT4C4001JDJ
U1-U20 = MT4C4001JDJ L (L-version)

TRUTH TABLE

FUNCTION		RAS	CAS	WE	OE	ADDRESSES tR	ADDRESSES tC	DATA IN/OUT DQ1-DQ40	NOTES
Standby		H	H→X	X	X	X	X	High-Z	
READ		L	L	H	L	ROW	COL	Data Out	
EARLY-WRITE		L	L	L	X	ROW	COL	Data In	
READ-WRITE		L	L	H→L	L→H	ROW	COL	Data Out, Data In	
FAST-PAGE-MODE	1st Cycle	L	H→L	H	L	ROW	COL	Data Out	
READ	2nd Cycle	L	H→L	H	L	n/a	COL	Data Out	
FAST-PAGE-MODE	1st Cycle	L	H→L	L	X	ROW	COL	Data In	
EARLY-WRITE	2nd Cycle	L	H→L	L	X	n/a	COL	Data In	
FAST-PAGE-MODE	1st Cycle	L	H→L	H→L	L→H	ROW	COL	Data Out, Data In	
READ-WRITE	2nd Cycle	L	H→L	H→L	L→H	n/a	COL	Data Out, Data In	
RAS-ONLY REFRESH		H	X	X	X	ROW	n/a	High-Z	
HIDDEN	READ	L→H→L	L	H	L	ROW	COL	Data Out	
REFRESH	WRITE	L→H→L	L	L	X	ROW	COL	Data In	
CAS-BEFORE-RAS REFRESH		H→L	L	H	X	X	X	High-Z	
BATTERY BACKUP REFRESH		H→L	L	X	X	X	X	High-Z	22

PRESENCE DETECT–INDUSTRY STANDARD

SYMBOL	-6	-7	-8
PRD1	NC	NC	NC
PRD2	NC	NC	NC
PRD3	NC	Vss	NC
PRD4	NC	NC	Vss

PRESENCE DETECT–APPLICATION SPECIFIC

SYMBOL	-6	-7	-8
PRD1	NC	NC	Vss
PRD2	Vss	NC	Vss
PRD3	NC	Vss	Vss
PRD4	NC	NC	NC

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} ..... -1V to +7V
Operating Temperature, T_A (Ambient) ..... 0°C to +70°C
Storage Temperature (Plastic) ..... -55°C to +125°C
Power Dissipation 20W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 2, 3, 6, 26) (0°C ≤ T_A ≤ 70°C; V_{CC} = 5V ±10%)

PARAMETER/CONDITION		SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage		V_{CC}	4.5	5.5	V	1
Input High (Logic 1) Voltage, All Inputs		V_{IH}	2.4	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, All Inputs		V_{IL}	-1.0	0.8	V	1
INPUT LEAKAGE CURRENT Any Input 0V ≤ V_{IN} ≤ V_{CC}	A0-A9, $\overline{WE}$	I_I	-40	40	µA	
(All other pins not under test = 0V) for each package input	$\overline{RAS}$, $\overline{CAS}$	I_{I2}	-20	20	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled, 0V ≤ V_{OUT} ≤ V_{CC}) for each package input	DQ1-DQ40	I_{OZ}	-20	20	µA	
OUTPUT LEVELS Output High Voltage (I_{OUT} = -5mA)		V_{OH}	2.4		V	
Output Low Voltage (I_{OUT} = 4.2mA)		V_{OL}		0.4	V	

		MAX				
PARAMETER/CONDITION	SYMBOL	-6	-7	-8	UNITS	NOTES
STANDBY CURRENT: TTL INPUT LEVELS Power supply standby current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH} after 8 $\overline{RAS}$ cycles (MIN))	I_{CC3}	40	40	40	mA	
STANDBY CURRENT: CMOS INPUT LEVELS Power supply standby current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} -0.2V	I_{CC4}	20	20	20	mA	
after 8 $\overline{RAS}$ cycles (MIN)). (All other inputs at V_{CC} -0.2V or V_{SS} +0.2V)		4	4	4	mA	22
OPERATING CURRENT ($\overline{RAS}$ and $\overline{CAS}$ = Cycling: ^tRC = ^tRC (MIN))	I_{CC1}	1120	1020	920	mA	2, 26
		1104	1004	904	mA	2,22,26
OPERATING CURRENT: FAST PAGE MODE ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ = Cycling: ^tPC = ^tPC (MIN))	I_{CC2}	820	720	620	mA	2, 26
		804	704	604	mA	2,22,26
REFRESH CURRENT: $\overline{RAS}$-ONLY ($\overline{RAS}$ = Cycling: $\overline{CAS}$ = V_{IH})	I_{CC5}	1120	1020	920	mA	2
		1104	1004	904	mA	2, 22
REFRESH CURRENT: $\overline{CAS}$-BEFORE-$\overline{RAS}$ ($\overline{RAS}$ and $\overline{CAS}$ = Cycling)	I_{CC6}	1120	1020	920	mA	2, 19
		1104	1004	904	mA	2,19,22
REFRESH CURRENT: BATTERY BACKUP (BBU) Average power supply current during BATTERY BACKUP refresh: $\overline{CAS}$ = 0.2V or $\overline{CAS}$-BEFORE-$\overline{RAS}$ cycling; $\overline{RAS}$ = ^tRAS (MIN) to 300ns; $\overline{WE}$, A0-A9 and D_{IN} = Vcc - 0.2V or 0.2V (D_{IN} may be left open), ^tRC = 125µs (1,024 rows at 125µs = 128ms)	I_{CC7}	6	6	6	mA	22

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A9	C_{I1}		128	pF	17
Input Capacitance: $\overline{WE}$, $\overline{OE}$	C_{I2}		168	pF	17
Input Capacitance: $\overline{RAS0}$, $\overline{RAS1}$, $\overline{CAS0}$, $\overline{CAS1}$	C_{I3}		84	pF	17
Input/Output Capacitance: DQ1-DQ40	C_{IO}		20	pF	17

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 3, 4, 5, 6, 7, 10, 11, 16) (V_{CC} = 5V ±10%)

AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	^tRC	110		130		150		ns	
READ-WRITE cycle time	^tRWC	165		185		205		ns	
FAST-PAGE-MODE READ or WRITE cycle time	^tPC	40		40		45		ns	
FAST-PAGE-MODE READ-WRITE cycle time	^tPRWC	90		95		100		ns	
Access time from $\overline{RAS}$	^tRAC		60		70		80	ns	8
Access time from $\overline{CAS}$	^tCAC		15		20		20	ns	9
Access time from column address	^tAA		30		35		40	ns	
Access time from $\overline{CAS}$ precharge	^tCPA		35		40		45	ns	
$\overline{RAS}$ pulse width	^tRAS	60	100,000	70	100,000	80	100,000	ns	
$\overline{RAS}$ pulse width (FAST PAGE MODE)	^tRASP	60	100,000	70	100,000	80	100,000	ns	
$\overline{RAS}$ hold time	^tRSH	15		20		20		ns	
$\overline{RAS}$ precharge time	^tRP	45		50		60		ns	
$\overline{CAS}$ pulse width	^tCAS	15	100,000	20	100,000	20	100,000	ns	
$\overline{CAS}$ hold time	^tCSH	60		70		80		ns	
$\overline{CAS}$ precharge time	^tCPN	10		10		10		ns	18
$\overline{CAS}$ precharge time (FAST PAGE MODE)	^tCP	10		10		10		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	^tRCD	20	40	20	50	20	60	ns	13
$\overline{CAS}$ to $\overline{RAS}$ precharge time	^tCRP	10		10		10		ns	
Row address setup time	^tASR	0		0		0		ns	
Row address hold time	^tRAH	10		10		10		ns	
$\overline{RAS}$ to column address delay time	^tRAD	15	30	15	35	15	40	ns	21
Column address setup time	^tASC	0		0		0		ns	
Column address hold time	^tCAH	10		15		15		ns	
Column address hold time (referenced to $\overline{RAS}$)	^tAR	50		55		60		ns	
Column address to $\overline{RAS}$ lead time	^tRAL	30		35		40		ns	
Read command setup time	^tRCS	0		0		0		ns	
Read command hold time (referenced to $\overline{CAS}$)	^tRCH	0		0		0		ns	14
Read command hold time (referenced to $\overline{RAS}$)	^tRRH	0		0		0		ns	14
$\overline{CAS}$ to output in Low-Z	^tCLZ	0		0		0		ns	
Output buffer turn-off delay	^tOFF	0	20	0	20	0	20	ns	12, 23
$\overline{WE}$ command setup time	^tWCS	0		0		0		ns	24

NEW DRAM MODULE

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 3, 4, 5, 6, 7, 10, 11, 16) (V_{CC} = 5V ±10%)

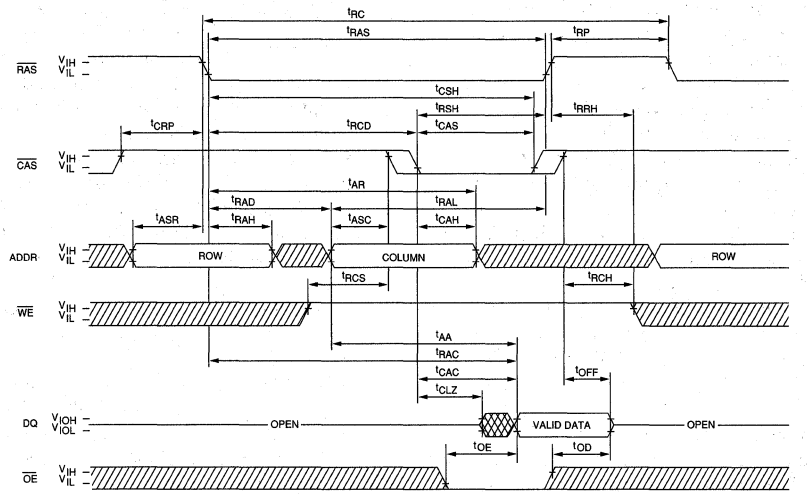
AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Write command hold time	^tWCH	10		15		15		ns	
Write command hold time (referenced to $\overline{RAS}$)	^tWCR	45		55		60		ns	
Write command pulse width	^tWP	10		15		15		ns	
Write command to $\overline{RAS}$ lead time	^tRWL	15		20		20		ns	
Write command to $\overline{CAS}$ lead time	^tCWL	15		20		20		ns	
Data-in setup time	^tDS	0		0		0		ns	15
Data-in hold time	^tDH	10		15		15		ns	15
Data-in hold time (referenced to $\overline{RAS}$)	^tDHR	45		55		60		ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	^tRWD	90		100		110		ns	24
Column address to $\overline{WE}$ delay time	^tAWD	60		65		70		ns	24
$\overline{CAS}$ to $\overline{WE}$ delay time	^tCWD	45		50		50		ns	24
Transition time (rise or fall)	^tT	3	50	3	50	3	50	ns	5, 16
Refresh period (1,024 cycles)	^tREF		16/128		16/128		16/128	ms	3/22
$\overline{RAS}$ to $\overline{CAS}$ precharge time	^tRPC	0		0		0		ns	19
$\overline{CAS}$ setup time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tCSR	10		10		10		ns	19
$\overline{CAS}$ hold time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tCHR	15		15		15		ns	19
$\overline{OE}$ setup prior to RAS during HIDDEN REFRESH cycle	^tORD	0		0		0		ns	20
Output disable	^tOD	15		20		20		ns	23
Output enable	^tOE	15		20		20		ns	
$\overline{OE}$ hold time from $\overline{WE}$ during READ-MODIFY-WRITE cycle	^tOEH	15		20		20		ns	25

NOTES

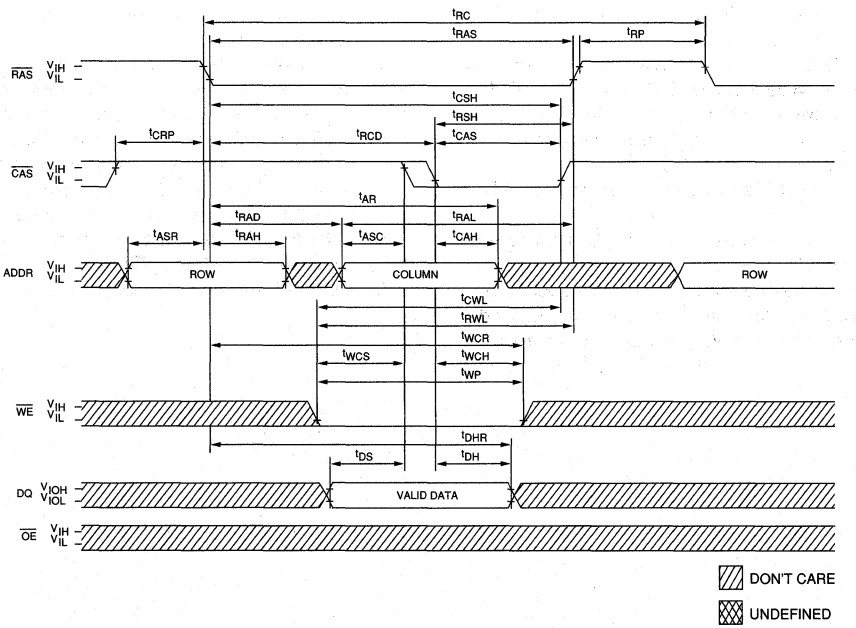
1. All voltages referenced to V_{SS}.
2. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
3. An initial pause of 100µs is required after power-up followed by any eight $\overline{RAS}$ cycles before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-up should be repeated any time the 16ms (128ms L version) refresh requirement is exceeded.
4. AC characteristics assume ^tT = 5ns.
5. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \le T_A \le 70°C$) is assured.
7. Measured with a load equivalent to two TTL gates and 100pF.
8. Assumes that $^tRCD < ^tRCD$ (MAX). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
9. Assumes that $^tRCD \ge ^tRCD$ (MAX).
10. If $\overline{CAS}$ = V_{IH}, data output is High-Z.
11. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
12. ^tOFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
13. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (MAX) limit, then access time is controlled exclusively by ^tCAC.
14. Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
15. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY-WRITE cycles.
16. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
17. This parameter is sampled. Capacitance is measured using MIL-STD-883C, Method 3012.1 (1 MHz AC, Vcc = 5V, DC bias = 2.4V @ 15mV RMS).
18. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, data-out (Q) will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer, $\overline{CAS}$ must be pulsed HIGH for ^tCP.
19. On-chip refresh and address counters are enabled.
20. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW.
21. Operation within the ^tRAD (MAX) limit ensures that ^tRCD (MAX) can be met. ^tRAD (MAX) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (MAX) limit, then access time is controlled exclusively by ^tAA.
22. L version only.
23. ^tWCS, ^tRWD, ^tAWD and ^tCWD are restrictive operating parameters in LATE-WRITE, and READ-MODIFY-WRITE cycles only. If $^tWCS \ge ^tWCS$ (MIN), the cycle is an EARLY-WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If $^tRWD \ge ^tRWD$ (MIN), $^tAWD \ge ^tAWD$ (MIN) and $^tCWD \ge ^tCWD$ (MIN), the cycle is a READ-MODIFY-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions are met, the state of data out is indeterminate. $\overline{OE}$ held HIGH and $\overline{WE}$ taken LOW after $\overline{CAS}$ goes LOW results in a LATE-WRITE ($\overline{OE}$ controlled) cycle.
24. LATE-WRITE and READ-MODIFY-WRITE cycles must have both ^tOD and ^tOEH met ($\overline{OE}$ HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. The DQs will provide the previously read data if $\overline{CAS}$ remains LOW and $\overline{OE}$ is taken back LOW after ^tOEH is met. If $\overline{CAS}$ goes HIGH prior to $\overline{OE}$ going back LOW, the DQs will remain open.
25. I_{CC} is dependent on cycle rates.
26. All other inputs at Vcc -0.2V.

NEW DRAM MODULE

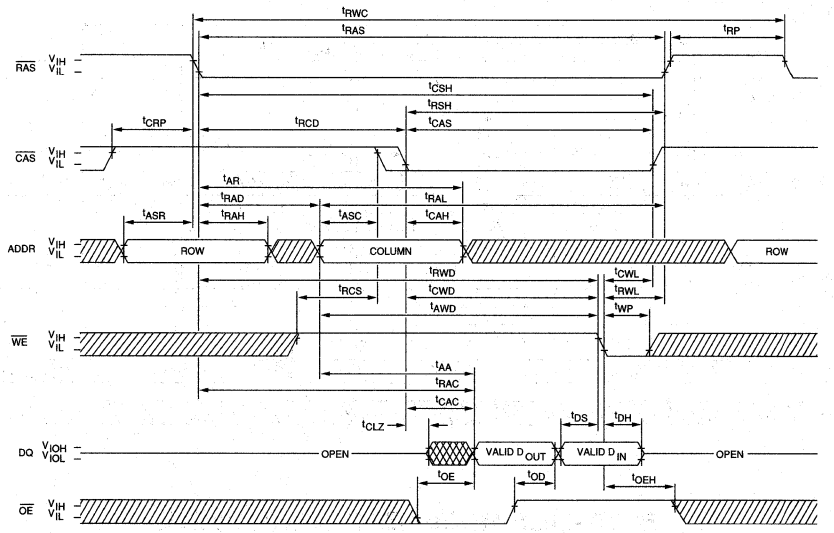
READ CYCLE



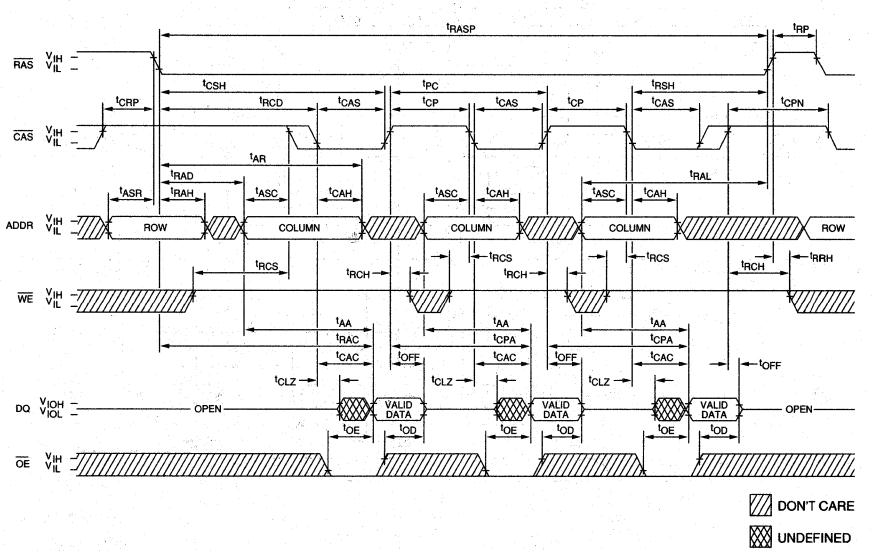
EARLY-WRITE CYCLE



READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)

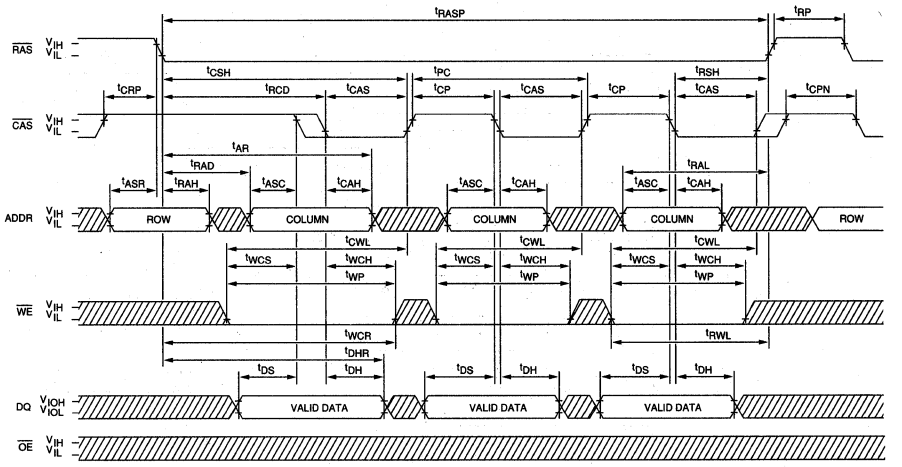


FAST-PAGE-MODE READ CYCLE

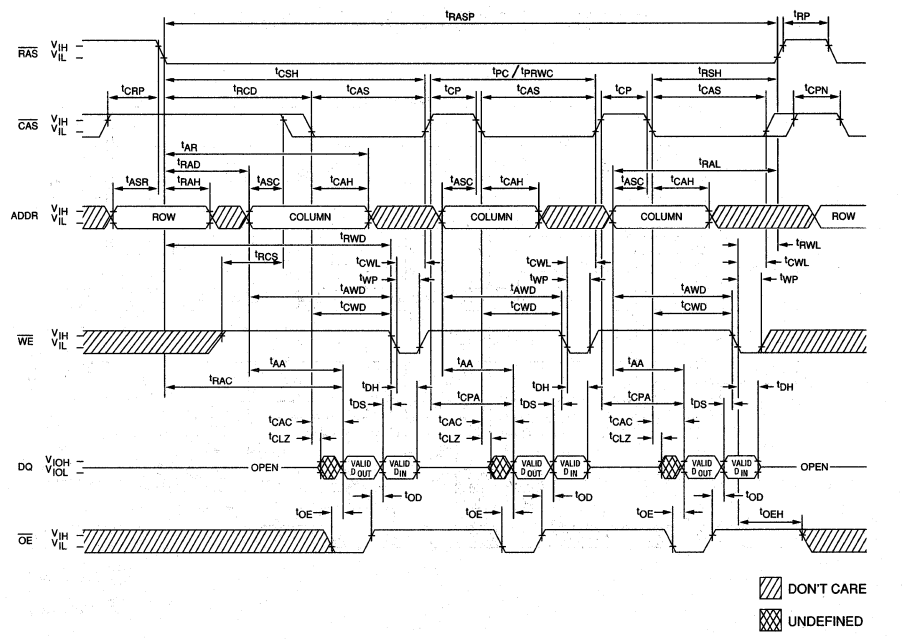


NEW ■ DRAM MODULE

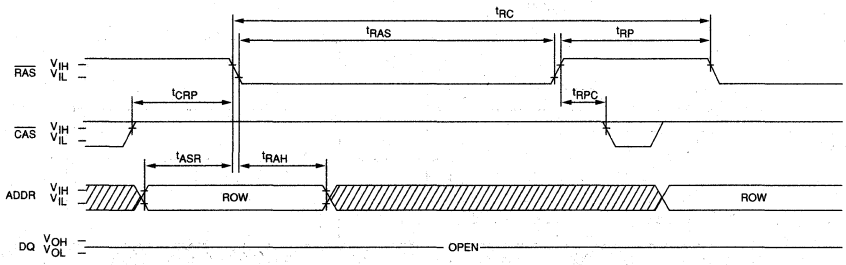
FAST-PAGE-MODE EARLY-WRITE CYCLE



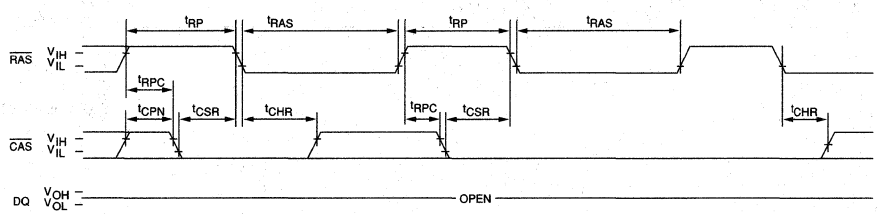
FAST-PAGE-MODE READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)



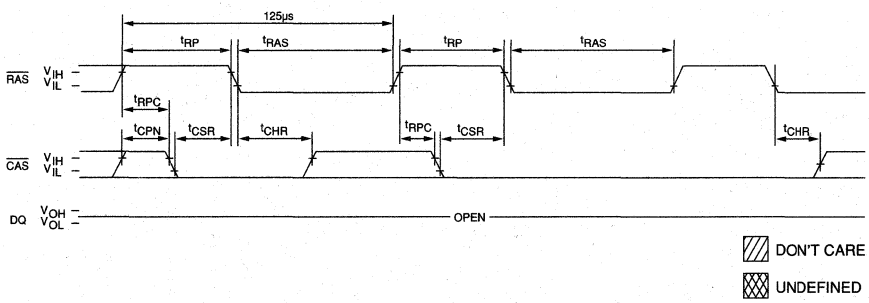
RAS-ONLY REFRESH CYCLE
(ADDR = A0-A9; and WE = DON'T CARE)



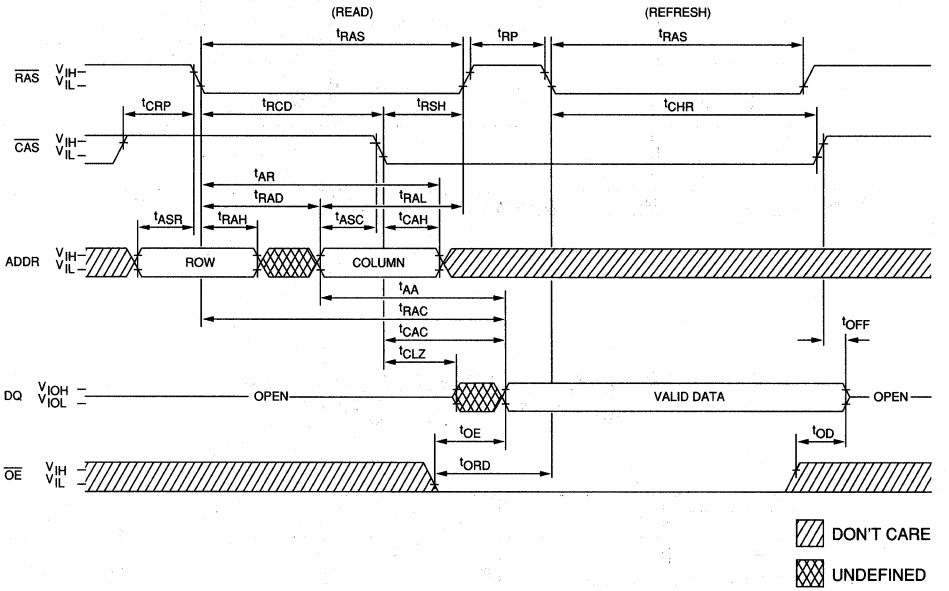
CAS-BEFORE-RAS REFRESH CYCLE
(A0-A9, OE = DON'T CARE)



BATTERY BACKUP REFRESH CYCLE [22]
(WE = DON'T CARE)



HIDDEN REFRESH CYCLE[20]
($\overline{WE}$ = HIGH; $\overline{OE}$ = LOW)



MICRON TECHNOLOGY, INC.

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IC DRAM CARD SELECTION GUIDE

Memory Configuration		Part Number	Access Time (ns)	Number of Pins Card	Page
512K x 16	1 Megabyte	MT8D88C25632	60, 70, 80	88	4-1
1 Meg x 16	2 Megabytes	MT16D88C51232	60, 70, 80	88	4-17
2 Meg x 16	4 Megabytes	MT8D88C132	60, 70, 80	88	4-33
4 Meg x 16	8 Megabytes	MT16D88C232	60, 70, 80	88	4-49
512K x 18	1 Megabyte	MT12D88C25636	60, 70, 80	88	4-65
1 Meg x 18	2 Megabytes	MT24D88C51236	60, 70, 80	88	4-79
2 Meg x 18	4 Megabytes	MT12D88C136	60, 70, 80	88	4-93
4 Meg x 18	8 Megabytes	MT24D88C236	60, 70, 80	88	4-107
512K x 20	1 Megabyte	MT12D88C25640	60, 70, 80	88	4-121
1 Meg x 20	2 Megabytes	MT24D88C51240	60, 70, 80	88	4-137
2 Meg x 20	4 Megabytes	MT12D88C140	60, 70, 80	88	4-153
4 Meg x 20	8 Megabytes	MT24D88C240	60, 70, 80	88	4-169
256K x 32	1 Megabyte	MT8D88C25632	60, 70, 80	88	4-1
512K x 32	2 Megabytes	MT16D88C51232	60, 70, 80	88	4-17
1 Meg x 32	4 Megabytes	MT8D88C132	60, 70, 80	88	4-33
2 Meg x 32	8 Megabytes	MT16D88C232	60, 70, 80	88	4-49
256K x 36	1 Megabyte	MT12D88C25636	60, 70, 80	88	4-65
512K x 36	2 Megabytes	MT24D88C51236	60, 70, 80	88	4-79
1 Meg x 36	4 Megabytes	MT12D88C136	60, 70, 80	88	4-93
2 Meg x 36	8 Megabytes	MT24D88C236	60, 70, 80	88	4-107
256K x 40	1 Megabyte	MT12D88C25640	60, 70, 80	88	4-121
512K x 40	2 Megabytes	MT24D88C51240	60, 70, 80	88	4-137
1 Meg x 40	4 Megabytes	MT12D88C140	60, 70, 80	88	4-153
2 Meg x 40	8 Megabytes	MT24D88C240	60, 70, 80	88	4-169

IC DRAM CARD 1 MEGABYTE

256K x 32, 512K x 16

NEW ■ IC DRAM CARD

FEATURES

- JEIDA, JEDEC and PCMCIA standard 88-pin IC DRAM card
- Polarized receptacle connector
- Industry standard DRAM functions and timing
- High-performance, CMOS silicon-gate process
- All outputs are fully TTL compatible
- All inputs buffered except $\overline{RAS}$ inputs
- Multiple $\overline{RAS}$ inputs for x16 or x32 selectability
- Refresh modes: $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$ (CBR), HIDDEN and BATTERY BACKUP (BBU)
- FAST PAGE MODE access cycle
- Single +5V ±5% power supply
- Low power; 8mW standby, 1.8W active (typical)
- Extended refresh standard: 512 cycles every 64ms

OPTIONS MARKING

- Timing

60ns access	-6
70ns access	-7
80ns access	-8

GENERAL DESCRIPTION

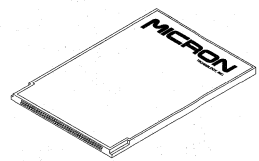
The MT8D88C25632 is a 1 megabyte, IC DRAM card organized as a 256K x 32 bit memory array. It may also be configured as a 512K x 16 bit memory array, provided the corresponding DQs on the host system are made common and memory bank control procedures are implemented. Separate $\overline{CAS}$ inputs allow byte accesses.

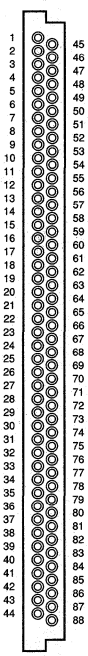
All inputs to the DRAMs are buffered, with the exception of $\overline{RAS}$. The line drivers used for buffers reduce reflections on the card and ensure compatibility in a wide range of systems. At the same time, the line drivers add delays to the buffered input timings when compared to standard DRAMs.

The MT8D88C25632 is designed for low power operation using 256K x 4 low power, extended refresh DRAMs. These devices support BATTERY BACKUP (BBU) cycle refresh; a very low current, data retention mode. Standard component DRAM refresh modes are supported as well.

Multiple $\overline{RAS}$ inputs conserve power by allowing individual bank selection. In the x32 organization, the memory is a single array that may be divided into four separate bytes. In the x16 organization, up to two banks, each with two separate bytes, may be independently selected. One bank is activated by each $\overline{RAS}$ selection; the others not selected remain in standby mode, drawing minimum power.

PIN ASSIGNMENT (End View)
88-Pin Card (U-1)





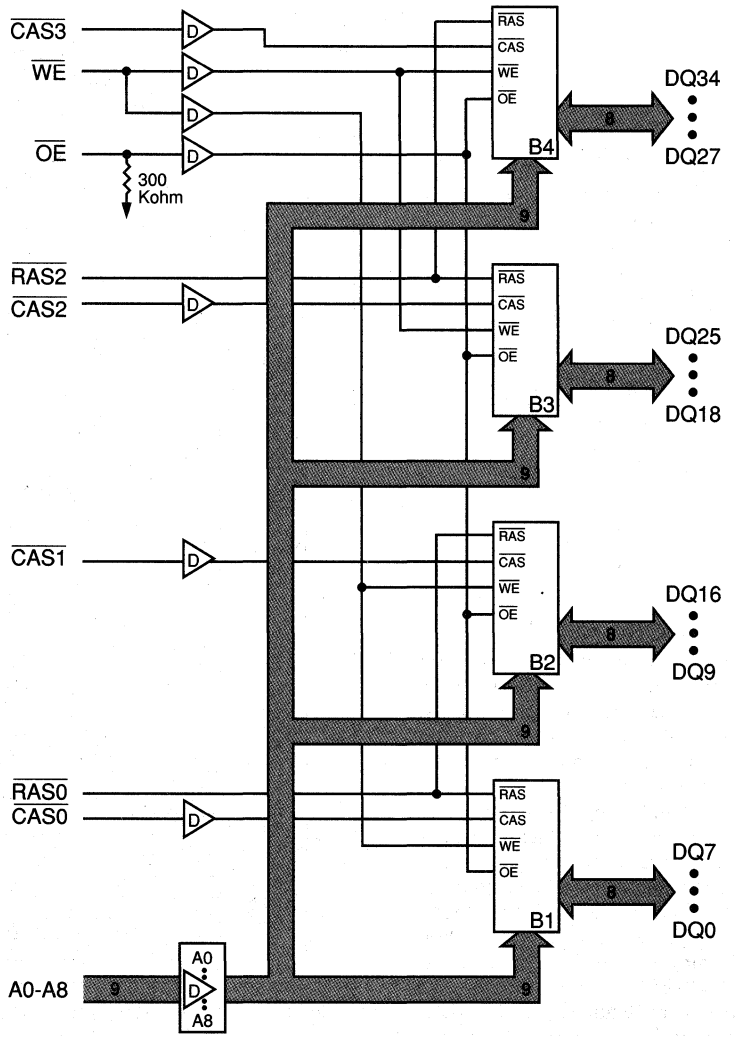
PIN #	SYMBOL	PIN #	SYMBOL	PIN #	SYMBOL
1	Vss	31	NC	61	NC
2	DQ0	32	NC	62	NC
3	DQ1	33	NC	63	Vss
4	DQ2	34	DQ9	64	NC
5	DQ3	35	NC	65	NC
6	DQ4	36	DQ10	66	$\overline{CAS2}$
7	DQ5	37	Vcc	67	Vss
8	DQ6	38	DQ11	68	$\overline{CAS3}$
9	Vcc	39	DQ12	69	NC
10	DQ7	40	DQ13	70	$\overline{WE}$
11	NC	41	DQ14	71	PD1 (Vss)
12	NC	42	DQ15	72	PD3 (Vss)
13	A0	43	DQ16	73	Vss
14	A2	44	Vss	74	PD5 (NC)
15	Vcc	45	Vss	75	PD7 (TBD)
16	A4	46	DQ18	76	PD8 (NC)
17	NC	47	DQ19	77	NC
18	A6	48	DQ20	78	NC
19	A8	49	DQ21	79	NC
20	NC	50	DQ22	80	DQ27
21	NC	51	DQ23	81	DQ28
22	$\overline{RAS0}$	52	DQ24	82	DQ29
23	$\overline{CAS0}$	53	DQ25	83	DQ30
24	$\overline{CAS1}$	54	NC	84	DQ31
25	NC	55	$\overline{OE}$ (Vss)	85	DQ32
26	$\overline{RAS2}$	56	Vss	86	DQ33
27	Vcc	57	A1	87	DQ34
28	PD2 (Vss)	58	A3	88	Vss
29	PD4 (Vss)	59	A5		
30	PD6 (TBD)	60	A7		

Eight presence detect pins may be read by the host to identify the MT8D88C25632 organization, number of banks, access time and refresh mode. These extensive presence detect functions allow systems to utilize the advanced power-saving features.

The MT8D88C25632 is built with a plastic frame covered by stainless steel panels. This package, containing an 88-pin receptacle connector, is keyed to prevent improper installation or insertion into other types of IC card sockets.

NEW ■ IC DRAM CARD

FUNCTIONAL BLOCK DIAGRAM



NOTE: 1. D = 74AC11244 line drivers.
2. B1 through B4 = 256K x 8 memory blocks.
3. $\overline{OE}$ is internally connected to ground via a 300 Kohm resistor and is also buffered to DRAM.

PIN DESCRIPTIONS

PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
22, 26	$\overline{RAS0}$, $\overline{RAS2}$	Input	Row Address Strobe: $\overline{RAS}$ is used to clock-in the 9 row-address bits. Two $\overline{RAS}$ inputs allow for a single x32 bank or two x16 banks.
23, 24, 66, 68	$\overline{CAS}$0-3	Input	Column Address Strobe: $\overline{CAS}$ is used to clock-in the 9 column-address bits, enable the DRAM output buffers, and strobe the data inputs on WRITE cycles. Four $\overline{CAS}$ inputs allow byte access control for any memory bank configuration.
70	$\overline{WE}$	Input	Write Enable: $\overline{WE}$ is the READ/WRITE control for the DQ pins. If $\overline{WE}$ is LOW prior to $\overline{CAS}$ going LOW, the access is an EARLY-WRITE cycle. If $\overline{WE}$ is HIGH while $\overline{CAS}$ is LOW, the access is a READ cycle, provided $\overline{OE}$ is also LOW. If WE goes LOW after $\overline{CAS}$ goes LOW, then the cycle is a LATE-WRITE cycle. A LATE-WRITE cycle is generally used in conjuction with a READ cycle to form a READ-MODIFY-WRITE cycle.
55	$\overline{OE}$	Input	Output Enable: $\overline{OE}$ is the input/output control for the DQ pins. $\overline{OE}$ is connected to ground through a 300 Kohm resistor and is intended to be LOW allowing for EARLY-WRITE cycles only. This signal may be driven, allowing for LATE-WRITE cycles.
13, 57, 14, 58, 16, 59, 18, 60, 19	A0-A8	Input	Address Inputs: These inputs are multiplexed and clocked by $\overline{RAS}$ and $\overline{CAS}$.
2-8, 10, 34, 36, 38-43, 46-53, 80-87	DQ0-DQ34	Input/ Output	Data I/O: For WRITE cycles, DQ0-DQ34 act as inputs to the addressed DRAM location. BYTE WRITEs may be performed by using the corresponding $\overline{CAS}$ select. For READ access cycles, DQ0-DQ34 act as outputs for the addressed DRAM location.
71, 28, 72, 29, 74, 30, 75, 76	PD1-PD8	-	Presence Detect: These pins are read by the host system and tell the system the card's personality. They will be either left floating (NC) or they will be grounded (Vss).
11, 12, 17, 20, 21, 25, 31, 32, 33, 35, 54, 61, 62, 64, 65, 69, 77, 78, 79	NC	-	No Connect: These pins should be left unconnected (reserved for future use).
9, 15, 27, 37	Vcc	Supply	Power Supply: +5V ±5%
1, 44, 45, 56, 63, 67, 73, 88	Vss	Supply	Ground

FUNCTIONAL DESCRIPTION

The MT8D88C25632 is a 1 megabyte memory card structured as a 256K x 32 bit memory array ($\overline{RAS0}$ = $\overline{RAS2}$). It also may be configured as a 512K x 16 bit memory array, provided the corresponding DQs on the host are connected and memory bank control procedures are implemented by interleaving both $\overline{RAS}$ lines.

Most x32 bit applications use the same signal to control the $\overline{CAS}$ inputs. $\overline{RAS0}$ controls the lower 16 bits, and $\overline{RAS2}$ controls the upper 16 bits to obtain a x32 memory array. For x16 applications, the corresponding DQs and the corresponding $\overline{CAS}$ pins must be connected together (DQ0 to DQ18, DQ1 to DQ19 and so forth, and $\overline{CAS0}$ to $\overline{CAS2}$ and $\overline{CAS1}$ to $\overline{CAS3}$). Each $\overline{RAS}$ is then a bank select for the 512K x 16 memory organization.

DRAM OPERATION

DRAM REFRESH

Memory cell data is retained in its correct state by maintaining power and executing any $\overline{RAS}$ cycle [READ, WRITE, $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$ (CBR), HIDDEN or BATTERY BACKUP (BBU) REFRESH] so that all 512 combinations of $\overline{RAS}$ addresses (A0-A8) are executed at least every 64ms, regardless of sequence.

The implied method of choice for refreshing the memory card is the BBU cycle. This is a very low current, data retention mode made possible by using the CBR REFRESH cycle over the extended refresh range (I_{CC7}).

The memory card may be used with the other refresh modes common in standard DRAMs. This allows the memory card to be used on existing systems that do not utilize the BBU REFRESH cycle. However, the memory card will draw more current in the STANDBY mode. The CBR REFRESH mode is recommended when not using the BBU mode.

DRAM READ AND WRITE CYCLES

During READ or WRITE cycles, each bit is uniquely addressed through the 18 address bits, which are entered 9 bits (A0-A8) at a time. $\overline{RAS}$ is used to latch the first 9 bits and $\overline{CAS}$ the latter 9 bits. READ or WRITE cycles are selected with the $\overline{WE}$ input. A logic HIGH on $\overline{WE}$ dictates READ mode while a logic LOW on $\overline{WE}$ dictates WRITE mode. During a WRITE cycle, data in (D) is latched by the falling edge of $\overline{CAS}$. $\overline{WE}$ must fall prior to $\overline{CAS}$ (EARLY WRITE); if $\overline{WE}$ goes LOW after $\overline{CAS}$, the outputs (Q) will be activated and will drive invalid data to the inputs, unless LATE-WRITE cycle timing specifications are met. The data inputs and data outputs are routed through pins using common I/O, and pin direction is controlled by $\overline{WE}$.

FAST PAGE MODE operation allows faster data operations (READ or WRITE) within a row address (A0-A8) defined page boundary. The FAST PAGE MODE cycle is always initiated with a row address strobed-in by $\overline{RAS}$ followed by a column address strobed-in by $\overline{CAS}$. $\overline{CAS}$ may be toggled-in by holding $\overline{RAS}$ LOW and strobing-in different column addresses, thus executing faster memory cycles. Returning $\overline{RAS}$ HIGH terminates the FAST PAGE MODE operation. Returning $\overline{RAS}$ and $\overline{CAS}$ HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the $\overline{RAS}$ high time.

DRAM TIMING

In accordance with JEDEC standard specifications, all inputs to the IC DRAM card are buffered, with the exception of $\overline{RAS}$ inputs. The line drivers used for buffers reduce reflections on the card and ensure compatibility in a wide range of systems. The implementation of buffers on the card may relieve the need for additional host system line drivers. Notes 23 though 29 indicate which parameters on the IC DRAM card are affected by the line drivers, and to what magnitude they are affected. The component DRAM timing specifications, rather than those of the IC DRAM card (in systems that use both), may cause timing incompatibilities.

All traces on the IC DRAM card (buffered and non-buffered) are approximately 50 ohms characteristic impedance. Matching impedance on the system board to 50 ohms characteristic impedance on traces to the IC DRAM card will decrease signal noise to the IC DRAM card, enhancing overall system reliability.

PHYSICAL DESIGN

The MT8D88C25632 is constructed with a molded plastic frame and covered with stainless steel panels. Inside, eight thin small-outline package (TSOP) DRAMs are mounted on an ultrathin printed circuit board. The board is attached to a high insertion, 88-pin receptacle connector. The package has a polarized key to prevent improper installation, including insertion into other types of IC card sockets. The MT8D88C25632 operates reliably up to 55°C.

MEMORY TRUTH TABLE

FUNCTION		RAS	CAS	WE	OE	ADDRESSES tR	ADDRESSES tC	DATA IN/OUT DQ0-DQ34
Standby		H	H→X	X	X	X	X	High-Z
READ		L	L	H	L (NC)	ROW	COL	Data Out
EARLY-WRITE		L	L	L	X	ROW	COL	Data In
READ-WRITE		L	L	H→L	L→H	ROW	COL	Data Out
FAST-PAGE-MODE	1st Cycle	L	H→L	H	L (NC)	ROW	COL	Data Out
READ	2nd Cycle	L	H→L	H	L (NC)	n/a	COL	Data Out
FAST-PAGE-MODE	1st Cycle	L	H→L	L	X	ROW	COL	Data In
EARLY-WRITE	2nd Cycle	L	H→L	L	X	n/a	COL	Data In
FAST-PAGE-MODE	1st Cycle	L	H→L	H→L	L→H	ROW	COL	Data In
READ-WRITE	2nd Cycle	L	H→L	H→L	L→H	n/a	COL	Data In
RAS-ONLY REFRESH		L	X	X	X	ROW	n/a	High-Z
HIDDEN	READ	L→H→L	L	H	L (NC)	ROW	COL	Data Out
REFRESH	WRITE	L→H→L	L	L	X	ROW	COL	Data In
CAS-BEFORE-RAS REFRESH		H→L	L	H	X	X	X	High-Z
BATTERY BACKUP REFRESH		H→L	L	H	X	X	X	High-Z

PRESENCE DETECT TRUTH TABLE

CHARACTERISTICS						PRESENT DETECT PIN (PDx)							
Card Density	DRAM Organizations	Card Address	RAS Address	CAS Address	Page Depth	1	2	3	4	5	6	7	8
0MB	No card installed	X	X	X	X	NC	NC	NC	NC	NC	X	X	X
• 1MB	256K x 1, 4, 16, 18	18	9	9	512	Vss	Vss	Vss	Vss	NC	X	X	X
2MB	256K x 1, 4, 16, 18	18	9	9	512	Vss	Vss	Vss	Vss	Vss	X	X	X
2MB	512K x 8, 9	19	10	9	512	NC	Vss	Vss	Vss	NC	X	X	X
4MB	512K x 8, 9	19	10	9	512	NC	Vss	Vss	Vss	Vss	X	X	X
4MB	1 Meg x 1, 4, 16, 18	20	10	10	1,024	Vss	NC	Vss	Vss	NC	X	X	X
8MB	1 Meg x 1, 4, 16, 18	20	10	10	1,024	Vss	NC	Vss	Vss	Vss	X	X	X
8MB	2 Meg x 8, 9	21	11	10	1,024	NC	NC	Vss	Vss	NC	X	X	X
16MB	2 Meg x 8, 9	21	11	10	1,024	NC	NC	Vss	Vss	Vss	X	X	X
16MB	4 Meg x 1, 4, 16, 18	22	12	11	1,024	Vss	Vss	NC	Vss	NC	X	X	X
32MB	4 Meg x 1, 4, 16, 18	22	12	11	1,024	Vss	Vss	NC	Vss	Vss	X	X	X
Access Timing		100ns				X	X	X	X	X	Vss	Vss	X
		80ns				X	X	X	X	X	NC	Vss	X
		70ns				X	X	X	X	X	Vss	NC	X
		60ns				X	X	X	X	X	NC	NC	X
		50ns				X	X	X	X	X	Vss	Vss	X
Refresh Control		Standard				X	X	X	X	X	X	X	NC
		Auto				X	X	X	X	X	X	X	Vss

NOTE: Vss = Ground.

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} ..... -0.5V to +5.25V
Operating Temperature, T_A (Ambient) ..... 0°C to +55°C
Storage Temperature ..... -20°C to +80°C
Power Dissipation 15W
Short Circuit Output Current 50mA
Card Insertions (Connector's Life Cycle) 10,000

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 3, 4, 6, 7) (0°C ≤ T_A ≤ 55°C; V_{CC} = 5V ±5%)

PARAMETER/CONDITION		SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage		V_{CC}	4.75	5.25	V	1
Input High (Logic 1) Voltage, All Inputs		V_{IH}	3.5	V_{CC}+0.5	V	1
Input Low (Logic 0) Voltage, All Inputs		V_{IL}	-0.5	0.8	V	1
INPUT LEAKAGE CURRENT, Any input	Non-buffered	I_{IN}	-12	12	µA	
(0V ≤ V_{IN} ≤ 5.25V; all other pins not under test = 0V)	Buffered	I_{IB}	-2	2	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled; 0V ≤ V_{OUT} ≤ 5.25V)		I_{OZ}	-10	10	µA	
OUTPUT LEVELS Output High Voltage (I_{OUT} = -5mA)		V_{OH}	2.4		V	
Output Low Voltage (I_{OUT} = 4.2mA)		V_{OL}		0.4	V	

		MAX				
PARAMETER/CONDITION	SYMBOL	-6	-7	-8	UNITS	NOTES
STANDBY CURRENT: (TTL) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC1}	16	16	16	mA	
STANDBY CURRENT: (CMOS) ($\overline{RAS}$ = $\overline{CAS}$ = Other Inputs = V_{CC} -0.2V)	I_{CC2}	1.6	1.6	1.6	mA	
OPERATING CURRENT: Random READ/WRITE Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC (MIN))	I_{CC3}	680	600	520	mA	3, 4, 30
OPERATING CURRENT: FAST PAGE MODE Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: ^tPC = ^tPC (MIN))	I_{CC4}	520	440	360	mA	3, 4, 30
REFRESH CURRENT: $\overline{RAS}$-ONLY Average power supply current ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}: ^tRC = ^tRC (MIN))	I_{CC5}	680	600	520	mA	3, 30
REFRESH CURRENT: $\overline{CAS}$-BEFORE-$\overline{RAS}$ (CBR) Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC (MIN))	I_{CC6}	680	600	520	mA	3, 5, 30
REFRESH CURRENT: BATTERY BACKUP (BBU) Average power supply current during BBU: $\overline{CAS}$ = 0.2V or CBR cycling; $\overline{RAS}$ = ^tRAS (MIN) up to 300ns; ^tRC = 125µs; $\overline{WE}$, A0-A8 and DQ = V_{CC} -0.2V or 0.2V (DQ may be left open)	I_{CC7}	1.6	1.6	1.6	mA	3 , 5

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: $\overline{CAS0}$, $\overline{CAS1}$, $\overline{CAS2}$, $\overline{CAS3}$, A0-A8, $\overline{OE}$	C_{I1}		9	pF	2
Input Capacitance: $\overline{WE}$	C_{I2}		13	pF	2
Input Capacitance: $\overline{RAS0}$, $\overline{RAS2}$	C_{I3}		50	pF	2
Input/Output Capacitance: DQ	C_{IO}		12	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C ≤ T_A ≤ 55°C; V_{CC} = 5V ±5%)

AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	^tRC	110		130		150		ns	23
FAST-PAGE-MODE READ or WRITE cycle time	^tPC	40		40		45		ns	23
Access time from $\overline{RAS}$	^tRAC		60		70		80	ns	14, 23
Access time from $\overline{CAS}$	^tCAC		25		30		30	ns	15, 26
Access time from column address	^tAA		40		45		50	ns	26
Access time from $\overline{CAS}$ precharge	^tCPA		50		50		55	ns	26
$\overline{RAS}$ pulse width	^tRAS	60	100,000	70	100,000	80	100,000	ns	23
$\overline{RAS}$ pulse width (FAST PAGE MODE)	^tRASP	60	100,000	70	100,000	80	100,000	ns	23
$\overline{RAS}$ hold time	^tRSH	25		30		30		ns	26
$\overline{RAS}$ precharge time	^tRP	40		50		60		ns	23
$\overline{CAS}$ pulse width	^tCAS	15	100,000	20	100,000	20	100,000	ns	23
$\overline{CAS}$ hold time	^tCSH	55		65		75		ns	25
$\overline{CAS}$ precharge time	^tCPN	10		10		10		ns	16, 23
$\overline{CAS}$ precharge time (FAST PAGE MODE)	^tCP	10		10		10		ns	23
$\overline{RAS}$ to $\overline{CAS}$ delay time	^tRCD	10	35	15	40	15	50	ns	17, 28
$\overline{CAS}$ to $\overline{RAS}$ precharge time	^tCRP	15		15		15		ns	26
Row address setup time	^tASR	10		10		10		ns	26
Row address hold time	^tRAH	5		5		5		ns	25
$\overline{RAS}$ to column address delay time	^tRAD	10	20	10	25	10	30	ns	18, 28
Column address setup time	^tASC	5		5		5		ns	24
Column address hold time	^tCAH	15		20		20		ns	24
Column address hold time (referenced to $\overline{RAS}$)	^tAR	45		50		55		ns	25
Column address to $\overline{RAS}$ lead time	^tRAL	40		45		50		ns	26
Read command setup time	^tRCS	5		5		5		ns	25
Read command hold time (referenced to $\overline{CAS}$)	^tRCH	5		5		5		ns	19, 24
Read command hold time (referenced to $\overline{RAS}$)	^tRRH	-5		-5		-5		ns	19, 25
$\overline{CAS}$ to output in Low-Z	^tCLZ	5		5		5		ns	24
Output buffer turn-off delay	^tOFF	5	30	5	30	5	30	ns	20, 29, 35
$\overline{WE}$ command setup time	^tWCS	5		5		5		ns	24

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C ≤ T_A ≤ 55°C; Vcc = 5V ±5%)

AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Write command hold time	^tWCH	15		20		20		ns	24
Write command hold time (referenced to $\overline{RAS}$)	^tWCR	40		50		55		ns	25
Write command pulse width	^tWP	10		15		15		ns	23
Write command to $\overline{RAS}$ lead time	^tRWL	25		30		30		ns	26
Write command to $\overline{CAS}$ lead time	^tCWL	20		25		25		ns	24
Data-in setup time	^tDS	5		5		5		ns	24, 32
Data-in hold time	^tDH	5		10		10		ns	25, 32
Data-in hold time (referenced to $\overline{RAS}$)	^tDHR	45		55		60		ns	23
Transition time (rise or fall)	^tT	2	15	2	15	2	15	ns	9, 10, 23
Refresh period (1,024 cycles)	^tREF		128		128		128	ms	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	^tRPC	10		10		10		ns	26
$\overline{CAS}$ setup time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tCSR	20		20		20		ns	5, 26
$\overline{CAS}$ hold time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tCHR	10		10		10		ns	5, 25
$\overline{WE}$ hold time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tWRH	5		5		5		ns	22, 25
$\overline{WE}$ setup time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tWRP	20		20		20		ns	22, 26
$\overline{WE}$ hold time (WCBR test cycle)	^tWTH	5		5		5		ns	22, 25
$\overline{WE}$ setup time	^tWTS	20		20		20		ns	22, 26
READ-WRITE cycle time	^tRWC	165		185		205		ns	
FAST-PAGE-MODE READ-WRITE cycle time	^tPRWC	90		95		100		ns	23
$\overline{RAS}$ to $\overline{WE}$ delay time	^tRWD	80		90		100		ns	31, 27
Column Address to $\overline{WE}$ delay time	^tAWD	65		70		75		ns	31, 24
$\overline{CAS}$ to $\overline{WE}$ delay time	^tCWD	50		65		55		ns	31, 24
Output buffer turn-off delay	^tOE		25		30		30	ns	20, 33, 26
Output disable	^tOD		25		30		30	ns	35, 26
$\overline{OE}$ hold time from $\overline{WE}$ during READ-MODIFY-WRITE cycle	^tOEH	5		10		10		ns	34, 27
$\overline{OE}$ hold time from $\overline{RAS}$ during HIDDEN REFRESH cycle	^tORD	10		10		10		ns	21, 26

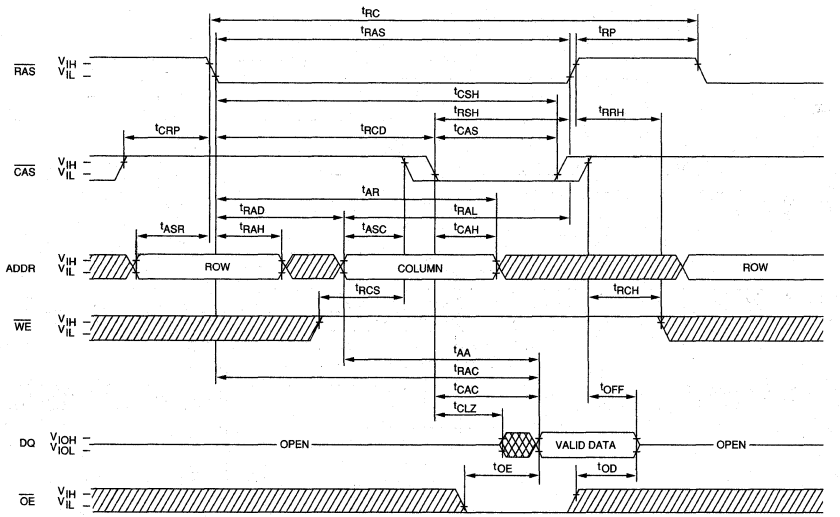
NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. V_{CC} = 5V ±10%, f = 1 MHz.
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is assured.
7. An initial pause of 100µs is required after power-up followed by eight $\overline{RAS}$ refresh cycles ($\overline{RAS}$-ONLY or CBR with $\overline{WE}$ HIGH) before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-up should be repeated any time the ^{t}REF refresh requirement is exceeded.
8. AC characteristics assume ^{t}T = 5ns.
9. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS}$ = V_{IH}, data output is High-Z.
12. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to 2 TTL gates and 100pF.
14. Assumes that $^{t}RCD < {}^{t}RCD$ (MAX). If ^{t}RCD is greater than the maximum recommended value shown in this table, ^{t}RAC will increase by the amount that ^{t}RCD exceeds the value shown.
15. Assumes that $^{t}RCD \geq {}^{t}RCD$ (MAX).
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer, $\overline{CAS}$ must be pulsed HIGH for ^{t}CPN.
17. Operation within the ^{t}RCD (MAX) limit ensures that ^{t}RAC (MAX) can be met. ^{t}RCD (MAX) is specified as a reference point only; if ^{t}RCD is greater than the specified ^{t}RCD (MAX) limit, then access time is controlled exclusively by ^{t}CAC.
18. Operation within the ^{t}RAD (MAX) limit ensures that ^{t}RCD (MAX) can be met. ^{t}RAD (MAX) is specified as a reference point only; if ^{t}RAD is greater than the specified ^{t}RAD (MAX) limit, then access time is controlled exclusively by ^{t}AA.
19. Either ^{t}RCH or ^{t}RRH must be satisfied for a READ cycle.
20. ^{t}OFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
21. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW.
22. ^{t}WTS and ^{t}WTH are setup and hold specifications for the $\overline{WE}$ pin being held LOW to enable the JEDEC test mode (with CBR timing constraints). These two parameters are the inverse of ^{t}WRP and ^{t}WRH in the CBR refresh cycle.
23. Timing between the DRAMs and the DRAM card did not change with the addition of the line drivers.
24. A +5ns timing skew from the DRAM to the DRAM card resulted from the addition of line drivers.
25. A -5ns timing skew from the DRAM to the DRAM card resulted from the addition of line drivers.
26. A +10ns timing skew from the DRAM to the DRAM card resulted from the addition of line drivers.
27. A -10ns timing skew from the DRAM to the DRAM card resulted from the addition of line drivers.
28. A -5ns (MIN) and a -10ns (MAX) timing skew from the DRAM to the DRAM card resulted from the addition of line drivers.
29. A +5ns (MIN) and a +10ns (MAX) timing skew from the DRAM to the DRAM card resulted from the addition of line drivers.
30. The maximum current ratings are based with the memory operating or being refreshed in the x32 mode. The stated maximums may be reduced by one half when used in the x16 mode.
31. ^{t}WCS, ^{t}RWD, ^{t}AWD and ^{t}CWD are restrictive operating parameters in late WRITE, and READ-MODIFY-WRITE cycles only. If $^{t}WCS \geq {}^{t}WCS$ (MIN), the cycle is an EARLY-WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If $^{t}RWD \geq {}^{t}RWD$ (MIN), $^{t}AWD \geq {}^{t}AWD$ (MIN) and $^{t}CWD \geq {}^{t}CWD$ (MIN), the cycle is a READ-MODIFY-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of data out is indeterminate. $\overline{OE}$ held HIGH and $\overline{WE}$ taken LOW after $\overline{CAS}$ goes LOW results in a LATE-WRITE ($\overline{OE}$ controlled) cycle.

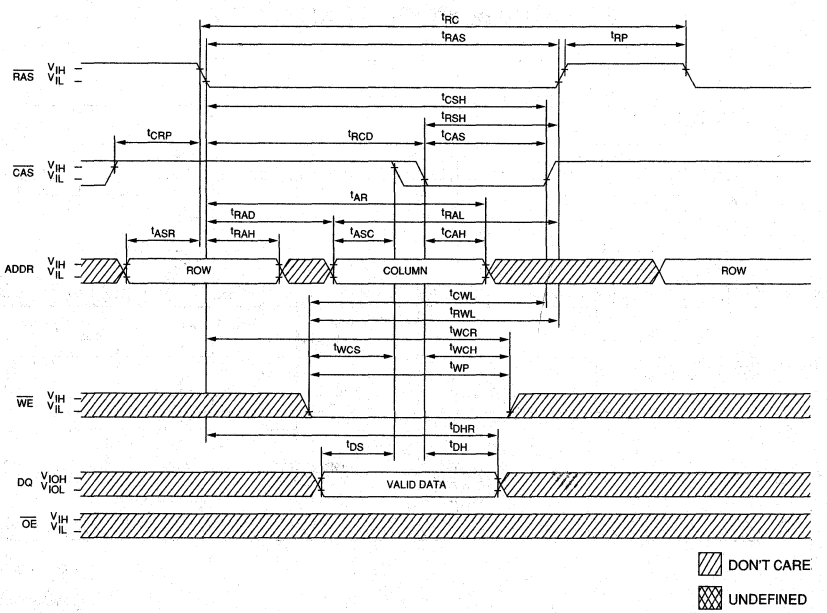
NOTES (continued)

32. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY-WRITE cycles and $\overline{WE}$ leading edge in LATE-WRITE or READ-MODIFY-WRITE cycles.
33. If $\overline{OE}$ is tied permanently LOW, LATE-WRITE or READ-MODIFY-WRITE operations are not possible.
34. LATE-WRITE and READ-MODIFY-WRITE cycles must have both ^{t}OD and ^{t}OEH met ($\overline{OE}$ HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. The DQs will provide the previously read data if $\overline{CAS}$ remains LOW and $\overline{OE}$ is taken back LOW after ^{t}OEH is met. If $\overline{CAS}$ goes HIGH prior to $\overline{OE}$ going back LOW, the DQs will remain open.
35. The DQs open during READ cycles once ^{t}OD or ^{t}OFF occur. If $\overline{CAS}$ goes HIGH first, $\overline{OE}$ becomes a "don't care." If $\overline{OE}$ goes HIGH and $\overline{CAS}$ stays LOW, $\overline{OE}$ is not a "don't care;" and the DQs will provide the previously read data if $\overline{OE}$ is taken back LOW (while $\overline{CAS}$ remains LOW).

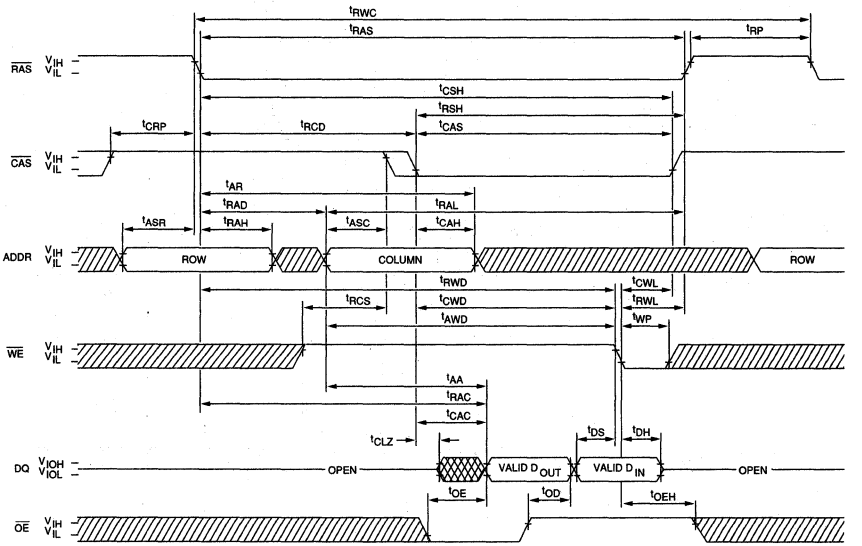
READ CYCLE



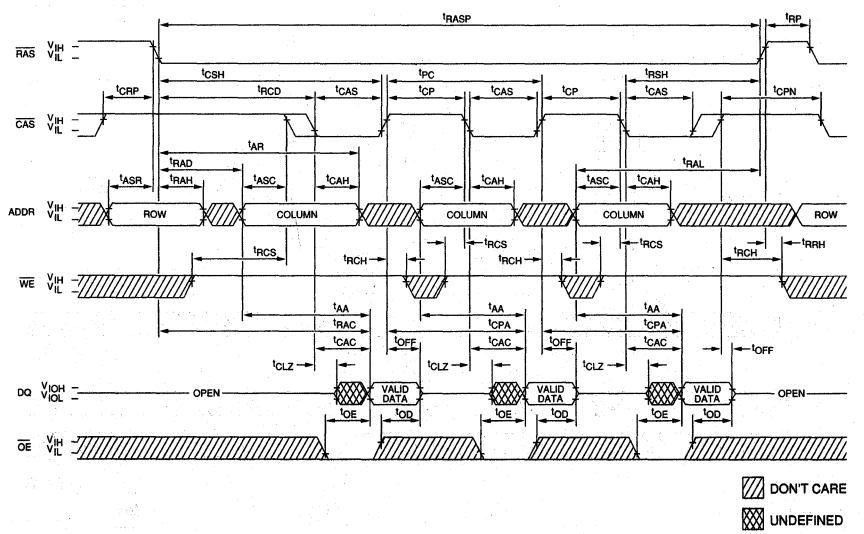
EARLY-WRITE CYCLE



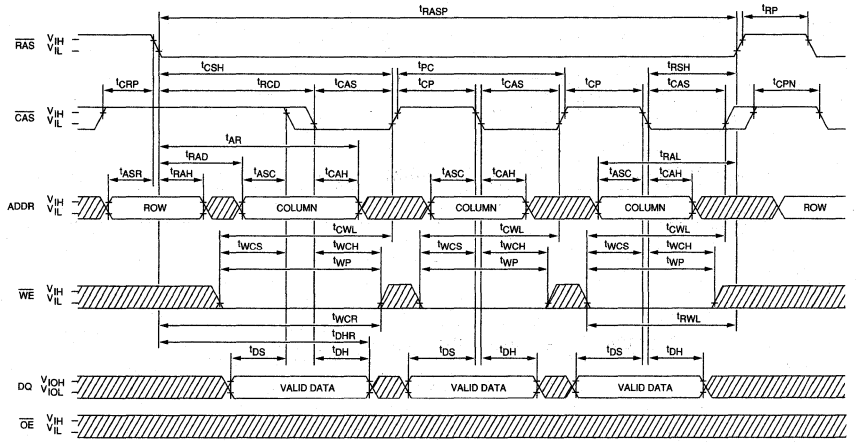
READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)



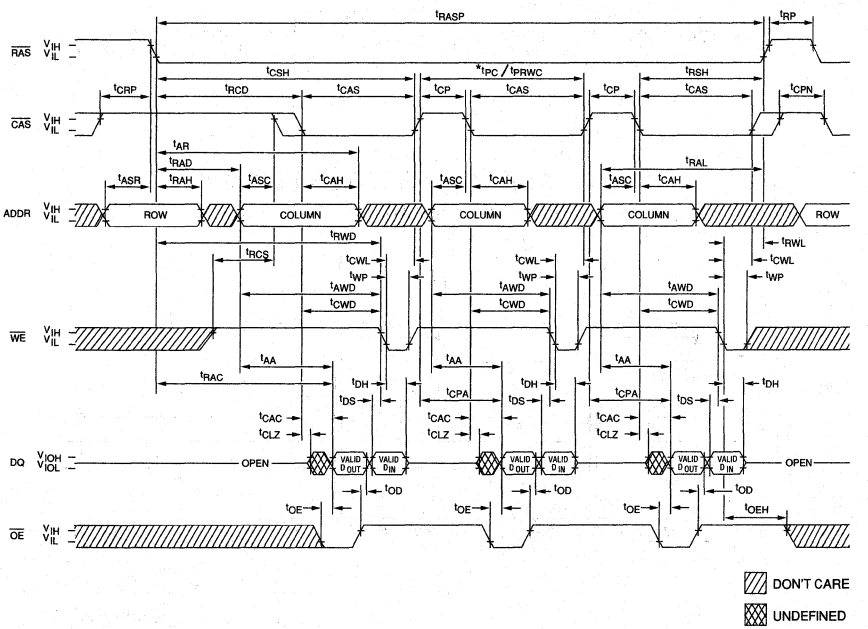
FAST-PAGE-MODE READ CYCLE



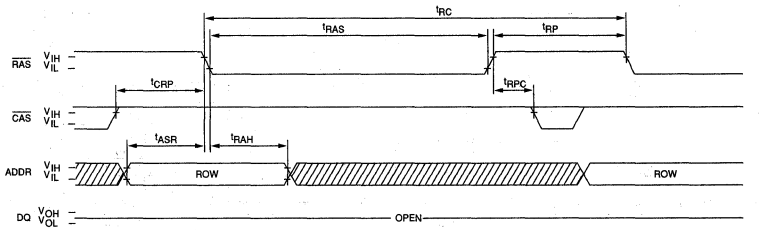
FAST-PAGE-MODE EARLY-WRITE CYCLE



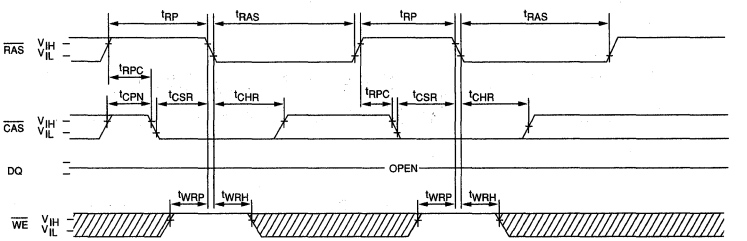
FAST-PAGE-MODE READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)



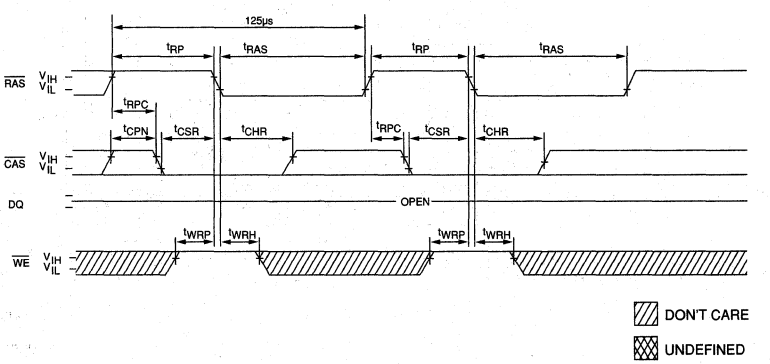
$\overline{RAS}$-ONLY REFRESH CYCLE
(ADDR = A0-A8; $\overline{WE}$ = DON'T CARE)



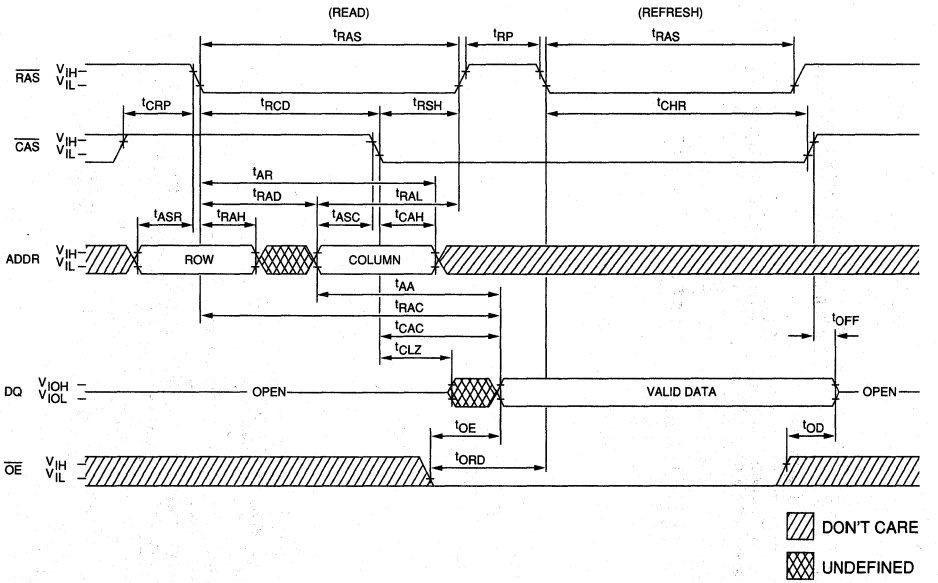
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE
(A0-A8 = DON'T CARE)



BATTERY BACKUP REFRESH CYCLE
(A0-A8 = DON'T CARE)

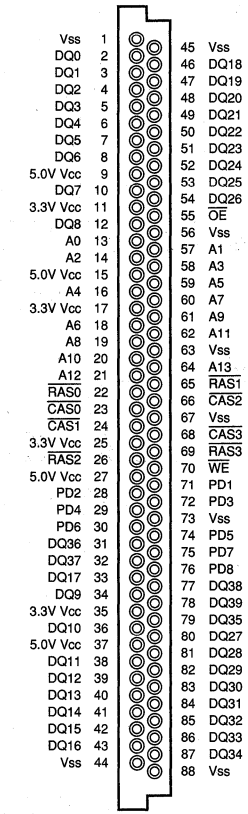


HIDDEN REFRESH CYCLE [21]
($\overline{WE}$ = HIGH)

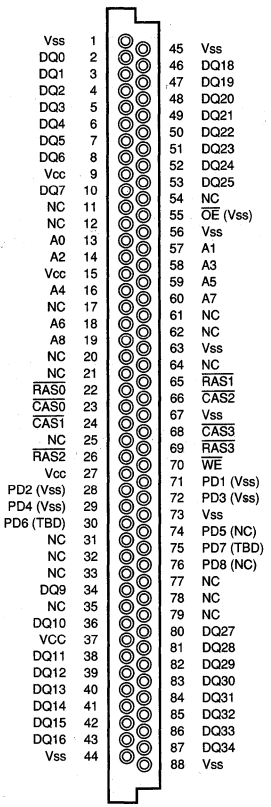


NEW ■ IC DRAM CARD

RESERVED JEDEC, JEIDA and PCMCIA 88-PIN ASSIGNMENT
(All Possible Combinations)



MT8D88C25632 PIN ASSIGNMENT
(JEDEC Standard)



IC DRAM CARD 2 MEGABYTES

512K x 32, 1 MEG x 16

NEW IC DRAM CARD

FEATURES

- JEIDA, JEDEC and PCMCIA standard 88-pin IC DRAM card
- Polarized receptacle connector
- Industry standard DRAM functions and timing
- High-performance, CMOS silicon-gate process
- All outputs are fully TTL compatible
- All inputs buffered except $\overline{RAS}$ inputs
- Multiple $\overline{RAS}$ inputs for x16 or x32 selectability
- Refresh modes: $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$ (CBR), BATTERY BACKUP (BBU) and HIDDEN
- FAST PAGE MODE access cycle
- Single +5V ±5% power supply
- Low power; 16mW standby, 1.8W active (typical)
- Extended refresh standard: 512 cycles every 64ms

OPTIONS MARKING

- Timing

60ns access	-6
70ns access	-7
80ns access	-8

GENERAL DESCRIPTION

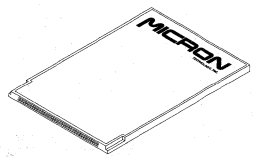
The MT16D88C51232 is a 2 megabyte, IC DRAM card organized as a 512K x 32 bit memory array. It may also be configured as a 1 Meg x 16 bit memory array, provided the corresponding DQs on the host system are made common and memory bank control procedures are implemented. Separate $\overline{CAS}$ inputs allow byte accesses.

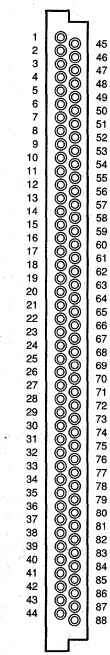
All inputs to the DRAMs are buffered, with the exception of $\overline{RAS}$. The line drivers used for buffers reduce reflections on the card and ensure compatibility in a wide range of systems. At the same time, the line drivers add delays to the buffered input timings when compared to standard DRAMs.

The MT16D88C51232 is designed for low power operation using 256K x 4 low power, extended refresh DRAMs. These devices support BATTERY BACKUP (BBU) cycle refresh; a very low current, data retention mode. Standard component DRAM refresh modes are supported as well.

Multiple $\overline{RAS}$ inputs conserve power by allowing individual bank selection. In the x32 organization, the memory array may be divided into two banks, each with four separate bytes. In the x16 organization, up to four banks, each with two separate bytes, may be independently selected. One bank is activated by each $\overline{RAS}$ selection; the others not selected remain in standby mode, drawing minimum power.

PIN ASSIGNMENT (End View)
88-Pin Card (U-1)





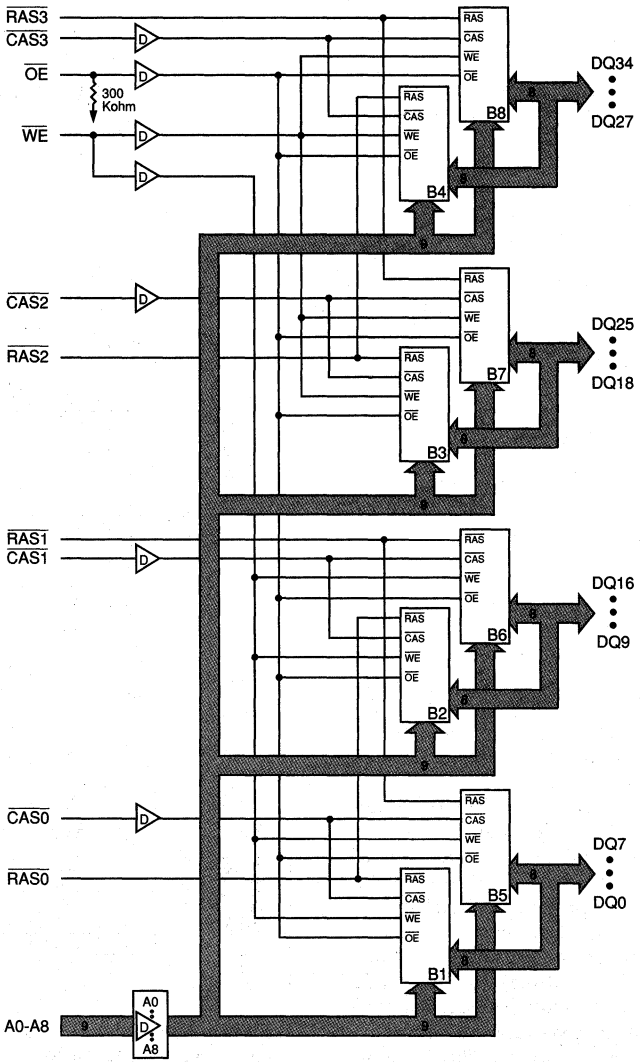
PIN #	SYMBOL	PIN #	SYMBOL	PIN #	SYMBOL
1	Vss	31	NC	61	NC
2	DQ0	32	NC	62	NC
3	DQ1	33	NC	63	Vss
4	DQ2	34	DQ9	64	NC
5	DQ3	35	NC	65	$\overline{RAS1}$
6	DQ4	36	DQ10	66	$\overline{CAS2}$
7	DQ5	37	Vcc	67	Vss
8	DQ6	38	DQ11	68	$\overline{CAS3}$
9	Vcc	39	DQ12	69	$\overline{RAS3}$
10	DQ7	40	DQ13	70	$\overline{WE}$
11	NC	41	DQ14	71	PD1 (Vss)
12	NC	42	DQ15	72	PD3 (Vss)
13	A0	43	DQ16	73	Vss
14	A2	44	Vss	74	PD5 (Vss)
15	Vcc	45	Vss	75	PD7 (TBD)
16	A4	46	DQ18	76	PD8 (NC)
17	NC	47	DQ19	77	NC
18	A6	48	DQ20	78	NC
19	A8	49	DQ21	79	NC
20	NC	50	DQ22	80	DQ27
21	NC	51	DQ23	81	DQ28
22	$\overline{RAS0}$	52	DQ24	82	DQ29
23	$\overline{CAS0}$	53	DQ25	83	DQ30
24	$\overline{CAS1}$	54	NC	84	DQ31
25	NC	55	$\overline{OE}$ (Vss)	85	DQ32
26	$\overline{RAS2}$	56	Vss	86	DQ33
27	Vcc	57	A1	87	DQ34
28	PD2 (Vss)	58	A3	88	Vss
29	PD4 (Vss)	59	A5		
30	PD6 (TBD)	60	A7		

Eight presence detect pins may be read by the host to identify the MT16D88C51232 organization, number of banks, access time and refresh mode. These extensive presence detect functions allow systems to utilize the advanced power-saving features.

The MT16D88C51232 is built with a plastic frame covered by stainless steel panels. This package, containing an 88-pin receptacle connector, is keyed to prevent improper installation or insertion into other types of IC card sockets.

NEW ■ IC DRAM CARD

FUNCTIONAL BLOCK DIAGRAM



NOTE: 1. D = 74AC11244 line drivers.
2. B1 through B8 = 256K x 8 memory blocks.
3. $\overline{OE}$ is internally connected to ground via a 300 Kohm resistor and is also buffered to DRAM.

PIN DESCRIPTIONS

PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
22, 26, 65, 69	$\overline{RAS}$0-3	Input	Row Address Strobe: $\overline{RAS}$ is used to clock-in the 9 row-address bits. Four $\overline{RAS}$ inputs allow for two x32 banks or four x16 banks.
23, 24, 66, 68	$\overline{CAS}$0-3	Input	Column Address Strobe: $\overline{CAS}$ is used to clock-in the 9 column-address bits, enable the DRAM output buffers, and strobe the data inputs on WRITE cycles. Four $\overline{CAS}$ inputs allow byte access control for any memory bank configuration.
70	$\overline{WE}$	Input	Write Enable: $\overline{WE}$ is the READ/WRITE control for the DQ pins. If $\overline{WE}$ is LOW prior to $\overline{CAS}$ going LOW, the access is an EARLY-WRITE cycle. If $\overline{WE}$ is HIGH while $\overline{CAS}$ is LOW, the access is a READ cycle, provided $\overline{OE}$ is also LOW. If WE goes LOW after $\overline{CAS}$ goes LOW, then the cycle is a LATE-WRITE cycle. A LATE-WRITE cycle is generally used in conjuction with a READ cycle to form a READ-MODIFY-WRITE cycle.
55	$\overline{OE}$	Input	Output Enable: $\overline{OE}$ is the input/output control for the DQ pins. $\overline{OE}$ is connected to ground through a 300 Kohm resistor and is intended to be LOW allowing for EARLY-WRITE cycles only. This signal may be driven, allowing for LATE-WRITE cycles.
13, 57, 14, 58, 16, 59, 18, 60, 19	A0-A8	Input	Address Inputs: These inputs are multiplexed and clocked by $\overline{RAS}$ and $\overline{CAS}$.
2-8, 10, 34, 36, 38-43, 46-53, 80-87	DQ0-DQ34	Input/ Output	Data I/O: For WRITE cycles, DQ0-DQ34 act as inputs to the addressed DRAM location. BYTE WRITEs may be performed by using the corresponding $\overline{CAS}$ select. For READ access cycles, DQ0-DQ34 act as outputs for the addressed DRAM location.
71, 28, 72, 29, 74, 30, 75, 76	PD1-PD8	-	Presence Detect: These pins are read by the host system and tell the system the card's personality. They will be either left floating (NC) or they will be grounded (Vss).
11, 12, 17, 20, 21, 25, 31, 32, 33, 35, 54, 61, 62, 64, 77, 78, 79	NC	-	No Connect: These pins should be left unconnected (reserved for future use).
9, 15, 27, 37	Vcc	Supply	Power Supply: +5V ±5%
1, 44, 45, 56, 63, 67, 73, 88	Vss	Supply	Ground

FUNCTIONAL DESCRIPTION

The MT16D88C51232 is a 2 megabyte memory card structured as a 512K x 32 bit memory array ($\overline{RAS0}$ = $\overline{RAS2}$ $\overline{RAS1}$ = $\overline{RAS3}$). It also may be configured as a 1 Meg x 16 bit memory array provided the corresponding DQs on the host are connected and memory bank control procedures are implemented by interleaving all four $\overline{RAS}$ lines.

Most x32 bit applications use the same signal to control the $\overline{CAS}$ inputs. $\overline{RAS0}$ and $\overline{RAS1}$ control the lower 16 bits, and $\overline{RAS2}$ and $\overline{RAS3}$ control the upper 16 bits to obtain a x32 memory array. For x16 applications, the corresponding DQs and the corresponding $\overline{CAS}$ pins must be connected together (DQ0 to DQ18, DQ1 to DQ19 and so forth, and $\overline{CAS0}$ to $\overline{CAS2}$ and $\overline{CAS1}$ to $\overline{CAS3}$). Each $\overline{RAS}$ is then a bank select for the 1 Meg x 16 memory organization.

DRAM OPERATION

DRAM REFRESH

Memory cell data is retained in its correct state by maintaining power and executing any $\overline{RAS}$ cycle [READ, WRITE, $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$ (CBR), HIDDEN or BATTERY BACKUP (BBU) REFRESH] so that all 512 combinations of $\overline{RAS}$ addresses (A0-A8) are executed at least every 64ms, regardless of sequence.

The implied method of choice for refreshing the memory card is the BBU cycle. This is a very low current, data retention mode made possible by using the CBR REFRESH cycle over the extended refresh range (I_{CC7}).

The memory card may be used with the other refresh modes common in standard DRAMs. This allows the memory card to be used on existing systems that do not utilize the BBU REFRESH cycle. However, the memory card will draw more current in the STANDBY mode. The CBR REFRESH mode is recommended when not using the BBU mode.

DRAM READ AND WRITE CYCLES

During READ or WRITE cycles, each bit is uniquely addressed through the 18 address bits, which are entered 9 bits (A0-A8) at a time. $\overline{RAS}$ is used to latch the first 9 bits and $\overline{CAS}$ the latter 9 bits. READ or WRITE cycles are selected with the $\overline{WE}$ input. A logic HIGH on $\overline{WE}$ dictates READ mode while a logic LOW on $\overline{WE}$ dictates WRITE mode. During a WRITE cycle, data in (D) is latched by the falling edge of $\overline{CAS}$. $\overline{WE}$ must fall prior to $\overline{CAS}$ (EARLY WRITE); if $\overline{WE}$ goes LOW after $\overline{CAS}$, the outputs (Q) will be activated and will drive invalid data to the inputs, unless LATE-WRITE cycle timing specifications are met. The data inputs and data outputs are routed through pins using common I/O, and pin direction is controlled by $\overline{WE}$.

FAST PAGE MODE operation allows faster data operations (READ or WRITE) within a row address (A0-A8) defined page boundary. The FAST PAGE MODE cycle is always initiated with a row address strobed-in by $\overline{RAS}$ followed by a column address strobed-in by $\overline{CAS}$. $\overline{CAS}$ may be toggled-in by holding $\overline{RAS}$ LOW and strobing-in different column addresses, thus executing faster memory cycles. Returning $\overline{RAS}$ HIGH terminates the FAST PAGE MODE operation. Returning $\overline{RAS}$ and $\overline{CAS}$ HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the $\overline{RAS}$ high time.

DRAM TIMING

In accordance with JEDEC standard specifications, all inputs to the IC DRAM card are buffered, with the exception of $\overline{RAS}$ inputs. The line drivers used for buffers reduce reflections on the card and ensure compatibility in a wide range of systems. The implementation of buffers on the card may relieve the need for additional host system line drivers. Notes 23 though 29 indicate which parameters on the IC DRAM card are affected by the line drivers, and to what magnitude they are affected. The component DRAM timing specifications, rather than those of the IC DRAM card (in systems which use both), may cause timing incompatibilities.

All traces on the IC DRAM card (buffered and non-buffered) are approximately 50 ohms characteristic impedance. Matching impedance on the system board to 50 ohms characteristic impedance on traces to the IC DRAM card will decrease signal noise to the IC DRAM card, enhancing overall system reliability.

PHYSICAL DESIGN

The MT16D88C51232 is constructed with a molded plastic frame and covered with stainless steel panels. Inside, 16 thin small-outline package (TSOP) DRAMs are mounted on both sides of an ultrathin printed circuit board. The board is attached to a high insertion, 88-pin receptacle connector. The package has a polarized key to prevent improper installation, including insertion into other types of IC card sockets. The MT16D88C51232 operates reliably up to 55°C.

MEMORY TRUTH TABLE

FUNCTION		RAS	CAS	WE	OE	ADDRESSES tR	ADDRESSES tC	DATA IN/OUT DQ0-DQ34
Standby		H	H→X	X	X	X	X	High-Z
READ		L	L	H	L (NC)	ROW	COL	Data Out
EARLY-WRITE		L	L	L	X	ROW	COL	Data In
READ-WRITE		L	L	H→L	L→H	ROW	COL	Data Out
FAST-PAGE-MODE	1st Cycle	L	H→L	H	L (NC)	ROW	COL	Data Out
READ	2nd Cycle	L	H→L	H	L (NC)	n/a	COL	Data Out
FAST-PAGE-MODE	1st Cycle	L	H→L	L	X	ROW	COL	Data In
EARLY-WRITE	2nd Cycle	L	H→L	L	X	n/a	COL	Data In
FAST-PAGE-MODE	1st Cycle	L	H→L	H→L	L→H	ROW	COL	Data In
READ-WRITE	2nd Cycle	L	H→L	H→L	L→H	n/a	COL	Data In
RAS-ONLY REFRESH		L	X	X	X	ROW	n/a	High-Z
HIDDEN	READ	L→H→L	L	H	L (NC)	ROW	COL	Data Out
REFRESH	WRITE	L→H→L	L	L	X	ROW	COL	Data In
CAS-BEFORE-RAS REFRESH		H→L	L	H	X	X	X	High-Z
BATTERY BACKUP REFRESH		H→L	L	H	X	X	X	High-Z

PRESENCE DETECT TRUTH TABLE

CHARACTERISTICS						PRESENT DETECT PIN (PDx)							
Card Density	DRAM Organizations	Card Address	RAS Address	CAS Address	Page Depth	1	2	3	4	5	6	7	8
0MB	No card installed	X	X	X	X	NC	NC	NC	NC	NC	X	X	X
1MB	256K x 1, 4, 16, 18	18	9	9	512	Vss	Vss	Vss	Vss	NC	X	X	X
• 2MB	256K x 1, 4, 16, 18	18	9	9	512	Vss	Vss	Vss	Vss	Vss	X	X	X
2MB	512K x 8, 9	19	10	9	512	NC	Vss	Vss	Vss	NC	X	X	X
4MB	512K x 8, 9	19	10	9	512	NC	Vss	Vss	Vss	Vss	X	X	X
4MB	1 Meg x 1, 4, 16, 18	20	10	10	1,024	Vss	NC	Vss	Vss	NC	X	X	X
8MB	1 Meg x 1, 4, 16, 18	20	10	10	1,024	Vss	NC	Vss	Vss	Vss	X	X	X
8MB	2 Meg x 8, 9	21	11	10	1,024	NC	NC	Vss	Vss	NC	X	X	X
16MB	2 Meg x 8, 9	21	11	10	1,024	NC	NC	Vss	Vss	Vss	X	X	X
16MB	4 Meg x 1, 4, 16, 18	22	12	11	1,024	Vss	Vss	NC	Vss	NC	X	X	X
32MB	4 Meg x 1, 4, 16, 18	22	12	11	1,024	Vss	Vss	NC	Vss	Vss	X	X	X
Access Timing		100ns				X	X	X	X	X	Vss	Vss	X
		80ns				X	X	X	X	X	NC	Vss	X
		70ns				X	X	X	X	X	Vss	NC	X
		60ns				X	X	X	X	X	NC	NC	X
		50ns				X	X	X	X	X	Vss	Vss	X
Refresh Control		Standard				X	X	X	X	X	X	X	NC
		Auto				X	X	X	X	X	X	X	Vss

NOTE: Vss = Ground.

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} ..... -0.5V to +5.25V
Operating Temperature, T_A (Ambient) ..... 0°C to +55°C
Storage Temperature ..... -20°C to +80°C
Power Dissipation 15W
Short Circuit Output Current 50mA
Card Insertions (Connector's Life Cycle) 10,000

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 3, 4, 6, 7) (0°C ≤ T_A ≤ 55°C; V_{CC} = 5V ±5%)

PARAMETER/CONDITION		SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage		V_{CC}	4.75	5.25	V	1
Input High (Logic 1) Voltage, All Inputs		V_{IH}	3.5	V_{CC}+0.5	V	1
Input Low (Logic 0) Voltage, All Inputs		V_{IL}	-0.5	0.8	V	1
INPUT LEAKAGE CURRENT, Any input	Non-buffered	I_{IN}	-12	12	µA	
(0V ≤ V_{IN} ≤ 5.25V; all other pins not under test = 0V)	Buffered	I_{IB}	-2	2	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled; 0V ≤ V_{OUT} ≤ 5.25V)		I_{OZ}	-10	10	µA	
OUTPUT LEVELS Output High Voltage (I_{OUT} = -5mA)		V_{OH}	2.4		V	
Output Low Voltage (I_{OUT} = 4.2mA)		V_{OL}		0.4	V	

PARAMETER/CONDITION	SYMBOL	MAX -6	MAX -7	MAX -8	UNITS	NOTES
STANDBY CURRENT: (TTL) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC1}	32	32	32	mA	
STANDBY CURRENT: (CMOS) ($\overline{RAS}$ = $\overline{CAS}$ = Other Inputs = V_{CC} -0.2V)	I_{CC2}	3.2	3.2	3.2	mA	
OPERATING CURRENT: Random READ/WRITE Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC (MIN))	I_{CC3}	680	600	520	mA	3, 4, 30
OPERATING CURRENT: FAST PAGE MODE Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: ^tPC = ^tPC (MIN))	I_{CC4}	520	440	360	mA	3, 4, 30
REFRESH CURRENT: $\overline{RAS}$-ONLY Average power supply current ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}: ^tRC = ^tRC (MIN))	I_{CC5}	680	600	520	mA	3, 30
REFRESH CURRENT: $\overline{CAS}$-BEFORE-$\overline{RAS}$ (CBR) Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC (MIN))	I_{CC6}	680	600	520	mA	3, 5, 30
REFRESH CURRENT: BATTERY BACKUP (BBU) Average power supply current during BBU: $\overline{CAS}$ = 0.2V or CBR cycling; $\overline{RAS}$ = ^tRAS (MIN) up to 300ns; ^tRC = 125µs; $\overline{WE}$, A0-A8 and DQ = V_{CC} -0.2V or 0.2V (DQ may be left open)	I_{CC7}	3.2	3.2	3.2	mA	3, 5

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: $\overline{CAS0}$, $\overline{CAS1}$, $\overline{CAS2}$, $\overline{CAS3}$, A0-A8, $\overline{OE}$	C_{I1}		9	pF	2
Input Capacitance: $\overline{WE}$	C_{I2}		13	pF	2
Input Capacitance: $\overline{RAS0}$, $\overline{RAS1}$, $\overline{RAS2}$, $\overline{RAS3}$	C_{I3}		50	pF	2
Input/Output Capacitance: DQ	C_{IO}		20	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) ($0°C \le T_A \le 55°C$; V_{CC} = 5V ±5%)

AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	t_{RC}	110		130		150		ns	23
FAST-PAGE-MODE READ or WRITE cycle time	t_{PC}	40		40		45		ns	23
Access time from $\overline{RAS}$	t_{RAC}		60		70		80	ns	14, 23
Access time from $\overline{CAS}$	t_{CAC}		25		30		30	ns	15, 26
Access time from column address	t_{AA}		40		45		50	ns	26
Access time from $\overline{CAS}$ precharge	t_{CPA}		50		50		55	ns	26
$\overline{RAS}$ pulse width	t_{RAS}	60	100,000	70	100,000	80	100,000	ns	23
$\overline{RAS}$ pulse width (FAST PAGE MODE)	t_{RASP}	60	100,000	70	100,000	80	100,000	ns	23
$\overline{RAS}$ hold time	t_{RSH}	25		30		30		ns	26
$\overline{RAS}$ precharge time	t_{RP}	40		50		60		ns	23
$\overline{CAS}$ pulse width	t_{CAS}	15	100,000	20	100,000	20	100,000	ns	23
$\overline{CAS}$ hold time	t_{CSH}	55		65		75		ns	25
$\overline{CAS}$ precharge time	t_{CPN}	10		10		10		ns	16, 23
$\overline{CAS}$ precharge time (FAST PAGE MODE)	t_{CP}	10		10		10		ns	23
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	10	35	15	40	15	50	ns	17, 28
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	15		15		15		ns	26
Row address setup time	t_{ASR}	10		10		10		ns	26
Row address hold time	t_{RAH}	5		5		5		ns	25
$\overline{RAS}$ to column address delay time	t_{RAD}	10	20	10	25	10	30	ns	18, 28
Column address setup time	t_{ASC}	5		5		5		ns	24
Column address hold time	t_{CAH}	15		20		20		ns	24
Column address hold time (referenced to $\overline{RAS}$)	t_{AR}	45		50		55		ns	25
Column address to $\overline{RAS}$ lead time	t_{RAL}	40		45		50		ns	26
Read command setup time	t_{RCS}	5		5		5		ns	25
Read command hold time (referenced to $\overline{CAS}$)	t_{RCH}	5		5		5		ns	19, 24
Read command hold time (referenced to $\overline{RAS}$)	t_{RRH}	-5		-5		-5		ns	19, 25
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	5		5		5		ns	24
Output buffer turn-off delay	t_{OFF}	5	30	5	30	5	30	ns	20, 29, 35
$\overline{WE}$ command setup time	t_{WCS}	5		5		5		ns	24

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C ≤ T_A ≤ 55°C; Vcc = 5V ±5%)

AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Write command hold time	^tWCH	15		20		20		ns	24
Write command hold time (referenced to $\overline{RAS}$)	^tWCR	40		50		55		ns	25
Write command pulse width	^tWP	10		15		15		ns	23
Write command to $\overline{RAS}$ lead time	^tRWL	25		30		30		ns	26
Write command to $\overline{CAS}$ lead time	^tCWL	20		25		25		ns	24
Data-in setup time	^tDS	5		5		5		ns	24, 32
Data-in hold time	^tDH	5		10		10		ns	25, 32
Data-in hold time (referenced to $\overline{RAS}$)	^tDHR	45		55		60		ns	23
Transition time (rise or fall)	^tT	2	15	2	15	2	15	ns	9, 10, 23
Refresh period (1,024 cycles)	^tREF		128		128		128	ms	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	^tRPC	10		10		10		ns	26
$\overline{CAS}$ setup time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tCSR	20		20		20		ns	5, 26
$\overline{CAS}$ hold time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tCHR	10		10		10		ns	5, 25
$\overline{WE}$ hold time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tWRH	5		5		5		ns	22, 25
$\overline{WE}$ setup time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tWRP	20		20		20		ns	22, 26
$\overline{WE}$ hold time (WCBR test cycle)	^tWTH	5		5		5		ns	22, 25
$\overline{WE}$ setup time	^tWTS	20		20		20		ns	22, 26
READ-WRITE cycle time	^tRWC	165		185		205		ns	
FAST-PAGE-MODE READ-WRITE cycle time	^tPRWC	90		95		100		ns	23
$\overline{RAS}$ to $\overline{WE}$ delay time	^tRWD	80		90		100		ns	31, 27
Column Address to $\overline{WE}$ delay time	^tAWD	65		70		75		ns	31, 24
$\overline{CAS}$ to $\overline{WE}$ delay time	^tCWD	50		65		55		ns	31, 24
Output buffer turn-off delay	^tOE		25		30		30	ns	20, 33, 26
Output disable	^tOD		25		30		30	ns	35, 26
$\overline{OE}$ hold time from $\overline{WE}$ during READ-MODIFY-WRITE cycle	^tOEH	5		10		10		ns	34, 27
$\overline{OE}$ hold time from $\overline{RAS}$ during HIDDEN REFRESH cycle	^tORD	10		10		10		ns	21, 26

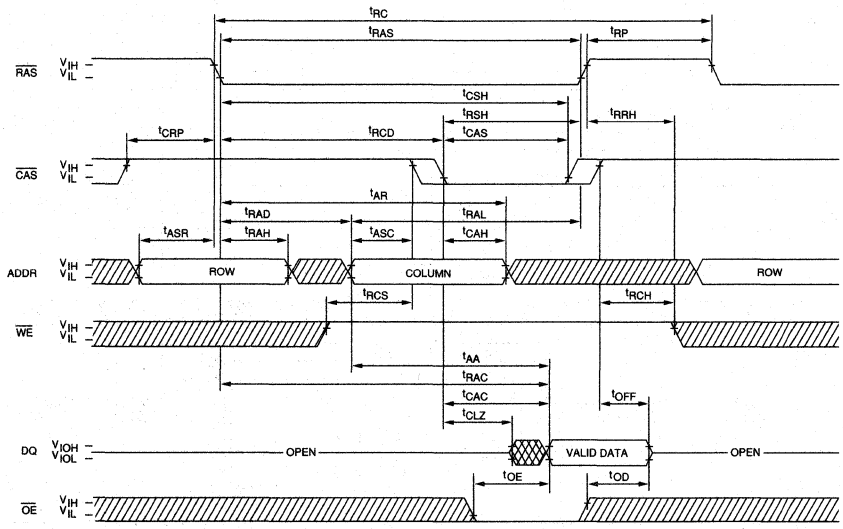
NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. V_{CC} = 5V ±10%, f = 1 MHz.
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is assured.
7. An initial pause of 100µs is required after power-up followed by eight $\overline{RAS}$ refresh cycles ($\overline{RAS}$-ONLY or CBR with $\overline{WE}$ HIGH) before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-up should be repeated any time the ^{t}REF refresh requirement is exceeded.
8. AC characteristics assume ^{t}T = 5ns.
9. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS}$ = V_{IH}, data output is High-Z.
12. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to 2 TTL gates and 100pF.
14. Assumes that $^{t}RCD < {}^{t}RCD$ (MAX). If ^{t}RCD is greater than the maximum recommended value shown in this table, ^{t}RAC will increase by the amount that ^{t}RCD exceeds the value shown.
15. Assumes that $^{t}RCD \geq {}^{t}RCD$ (MAX).
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer, $\overline{CAS}$ must be pulsed HIGH for ^{t}CPN.
17. Operation within the ^{t}RCD (MAX) limit ensures that ^{t}RAC (MAX) can be met. ^{t}RCD (MAX) is specified as a reference point only; if ^{t}RCD is greater than the specified ^{t}RCD (MAX) limit, then access time is controlled exclusively by ^{t}CAC.
18. Operation within the ^{t}RAD (MAX) limit ensures that ^{t}RCD (MAX) can be met. ^{t}RAD (MAX) is specified as a reference point only; if ^{t}RAD is greater than the specified ^{t}RAD (MAX) limit, then access time is controlled exclusively by ^{t}AA.
19. Either ^{t}RCH or ^{t}RRH must be satisfied for a READ cycle.
20. ^{t}OFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
21. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW.
22. ^{t}WTS and ^{t}WTH are setup and hold specifications for the $\overline{WE}$ pin being held LOW to enable the JEDEC test mode (with CBR timing constraints). These two parameters are the inverse of ^{t}WRP and ^{t}WRH in the CBR refresh cycle.
23. Timing between the DRAMs and the DRAM card did not change with addition of the line drivers.
24. A +5ns timing skew from the DRAM to the DRAM Card resulted from the addition of line drivers.
25. A -5ns timing skew from the DRAM to the DRAM Card resulted from the addition of line drivers.
26. A +10ns timing skew from the DRAM to the DRAM Card resulted from the addition of line drivers.
27. A -10ns timing skew from the DRAM to the DRAM Card resulted from the addition of line drivers.
28. A -5ns (MIN) and a -10ns (MAX) timing skew from the DRAM to the DRAM Card resulted from the addition of line drivers.
29. A +5ns (MIN) and a +10ns (MAX) timing skew from the DRAM to the DRAM Card resulted from the addition of line drivers.
30. The maximum current ratings are based on one of the two banks operating or being refreshed (x32 mode). The stated maximums may be reduced by one half when used in the x16 mode. Standby currents of non-active bank is not included.
31. ^{t}WCS, ^{t}RWD, ^{t}AWD and ^{t}CWD are restrictive operating parameters in late WRITE, and READ-MODIFY-WRITE cycles only. If $^{t}WCS \geq {}^{t}WCS$ (MIN), the cycle is an EARLY-WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If $^{t}RWD \geq {}^{t}RWD$ (MIN), $^{t}AWD \geq {}^{t}AWD$ (MIN) and $^{t}CWD \geq {}^{t}CWD$ (MIN), the cycle is a READ-MODIFY-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of data out is indeterminate. $\overline{OE}$ held HIGH and $\overline{WE}$ taken LOW after $\overline{CAS}$ goes LOW results in a LATE-WRITE ($\overline{OE}$ controlled) cycle.

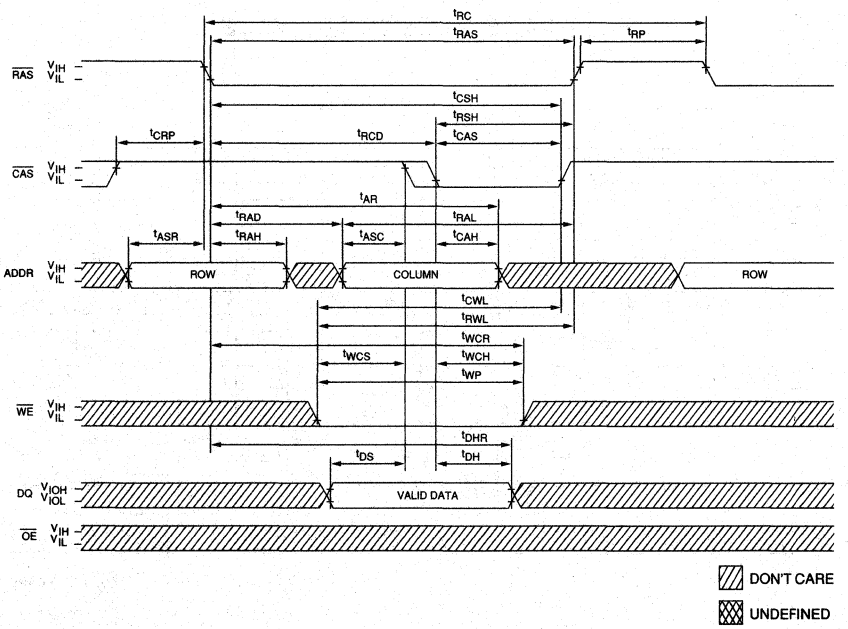
NOTES (continued)

32. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY-WRITE cycles and $\overline{WE}$ leading edge in LATE-WRITE or READ-MODIFY-WRITE cycles.
33. If $\overline{OE}$ is tied permanently LOW, LATE-WRITE or READ-MODIFY-WRITE operations are not possible.
34. LATE-WRITE and READ-MODIFY-WRITE cycles must have both ^{t}OD and ^{t}OEH met ($\overline{OE}$ HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. The DQs will provide the previously read data if $\overline{CAS}$ remains LOW and $\overline{OE}$ is taken back LOW after ^{t}OEH is met. If $\overline{CAS}$ goes HIGH prior to $\overline{OE}$ going back LOW, the DQs will remain open.
35. The DQs open during READ cycles once ^{t}OD or ^{t}OFF occur. If $\overline{CAS}$ goes HIGH first, $\overline{OE}$ becomes a "don't care." If $\overline{OE}$ goes HIGH and $\overline{CAS}$ stays LOW, $\overline{OE}$ is not a "don't care;" and the DQs will provide the previously read data if $\overline{OE}$ is taken back LOW (while $\overline{CAS}$ remains LOW).

READ CYCLE

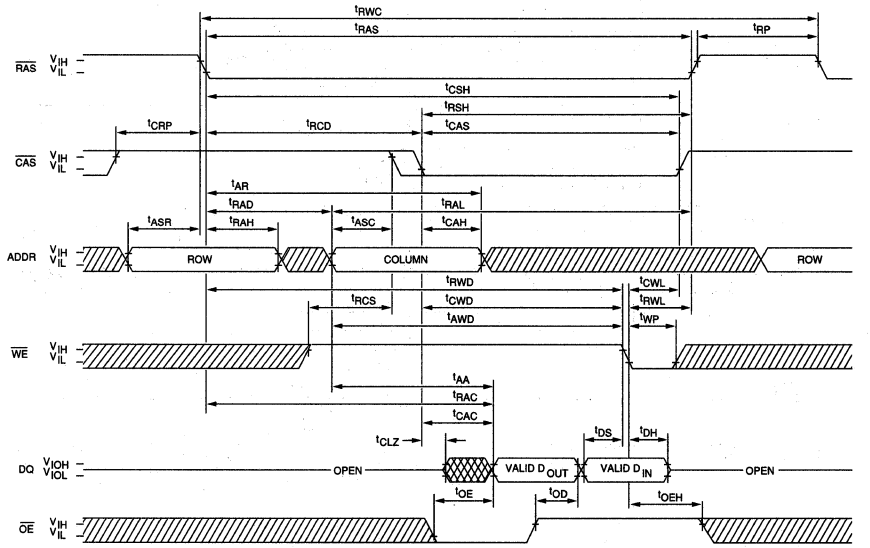


EARLY-WRITE CYCLE

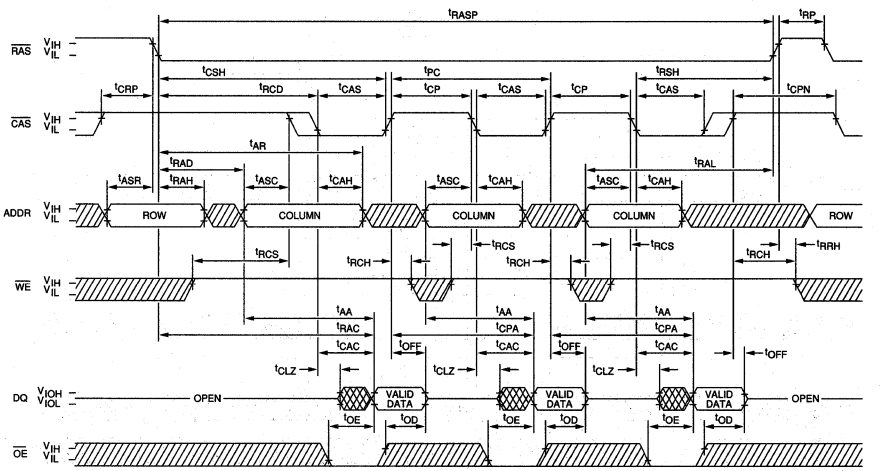


NEW ■ IC DRAM CARD

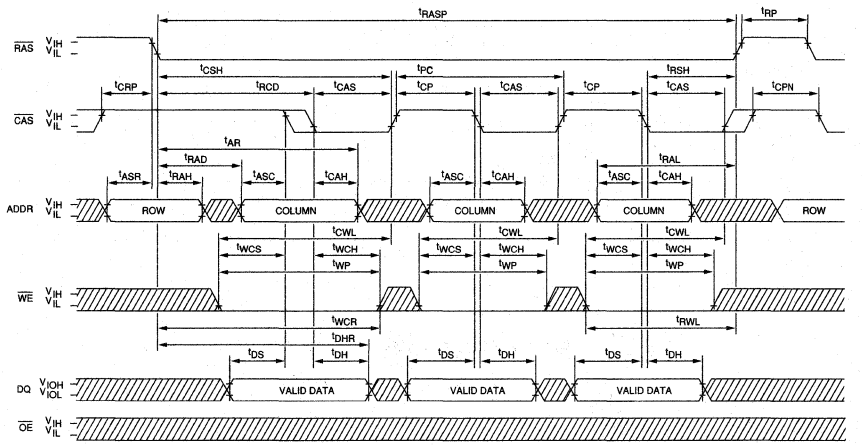
READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)



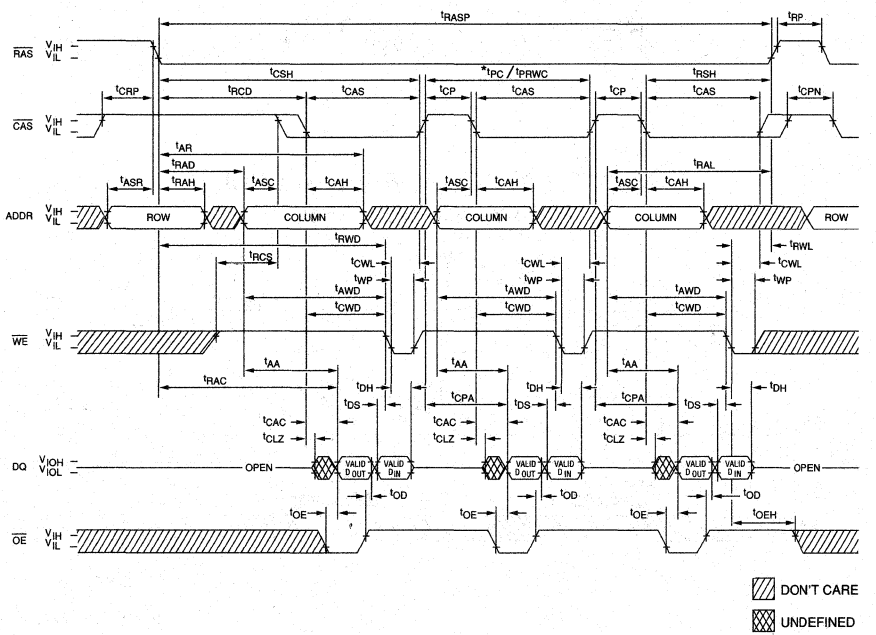
FAST-PAGE-MODE READ CYCLE



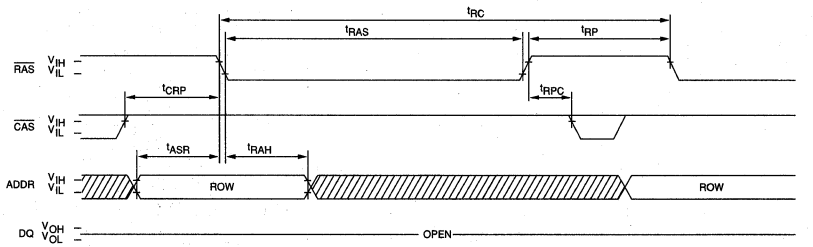
FAST-PAGE-MODE EARLY-WRITE CYCLE



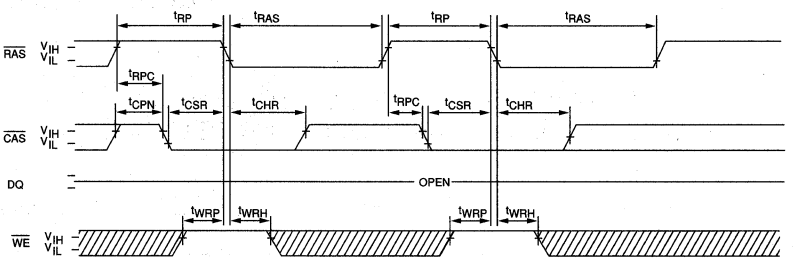
FAST-PAGE-MODE READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)



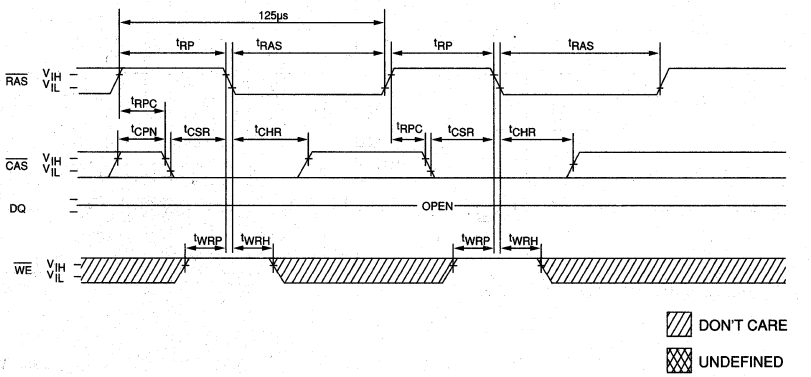
$\overline{RAS}$-ONLY REFRESH CYCLE
(ADDR = A0-A8; $\overline{WE}$ = DON'T CARE)



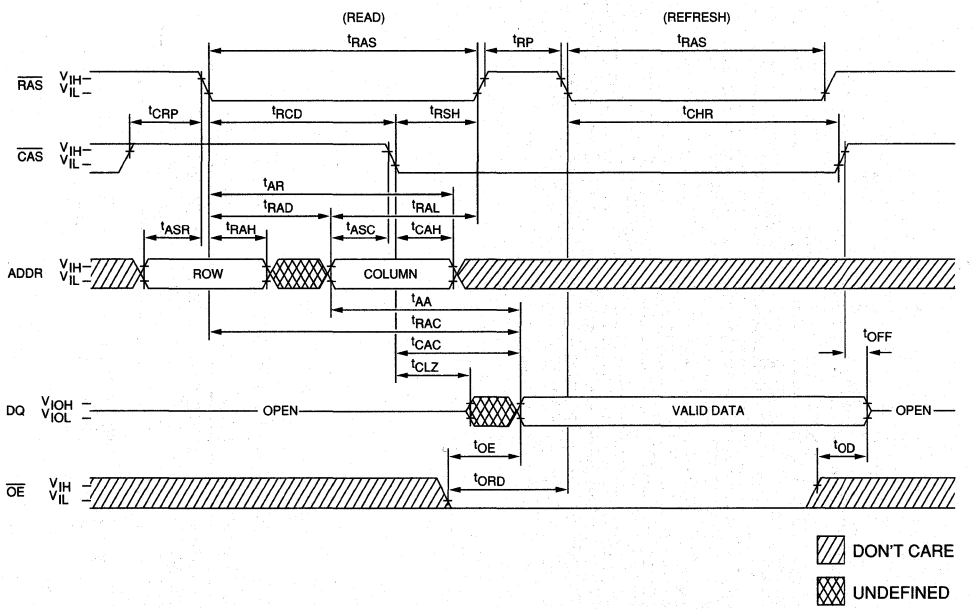
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE
(A0-A8 = DON'T CARE)



BATTERY BACKUP REFRESH CYCLE
(A0-A8 = DON'T CARE)

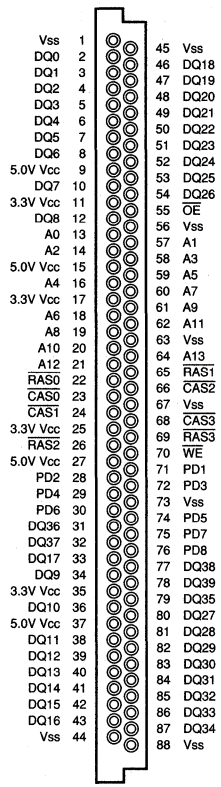


HIDDEN REFRESH CYCLE [21]
($\overline{WE}$ = HIGH)



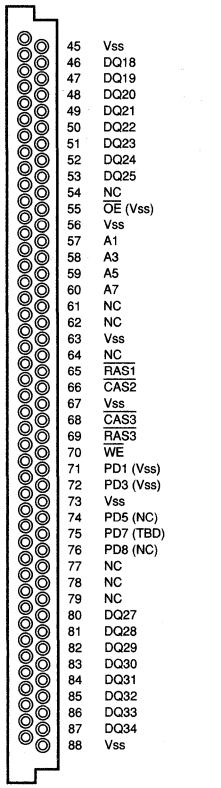
NEW ■ IC DRAM CARD

RESERVED JEDEC, JEIDA and PCMCIA 88-PIN ASSIGNMENT
(All Possible Combinations)



Vss	1	45	Vss
DQ0	2	46	DQ18
DQ1	3	47	DQ19
DQ2	4	48	DQ20
DQ3	5	49	DQ21
DQ4	6	50	DQ22
DQ5	7	51	DQ23
DQ6	8	52	DQ24
5.0V Vcc	9	53	DQ25
DQ7	10	54	DQ26
3.3V Vcc	11	55	$\overline{OE}$
DQ8	12	56	Vss
A0	13	57	A1
A2	14	58	A3
5.0V Vcc	15	59	A5
A4	16	60	A7
3.3V Vcc	17	61	A9
A6	18	62	A11
A8	19	63	Vss
A10	20	64	A13
A12	21	65	$\overline{RAS1}$
$\overline{RAS0}$	22	66	$\overline{CAS2}$
$\overline{CAS0}$	23	67	Vss
$\overline{CAS1}$	24	68	$\overline{CAS3}$
3.3V Vcc	25	69	$\overline{RAS3}$
$\overline{RAS2}$	26	70	$\overline{WE}$
5.0V Vcc	27	71	PD1
PD2	28	72	PD3
PD4	29	73	Vss
PD6	30	74	PD5
DQ36	31	75	PD7
DQ37	32	76	PD8
DQ17	33	77	DQ38
DQ9	34	78	DQ39
3.3V Vcc	35	79	DQ35
DQ10	36	80	DQ27
5.0V Vcc	37	81	DQ28
DQ11	38	82	DQ29
DQ12	39	83	DQ30
DQ13	40	84	DQ31
DQ14	41	85	DQ32
DQ15	42	86	DQ33
DQ16	43	87	DQ34
Vss	44	88	Vss

MT16D88C51232 PIN ASSIGNMENT
(JEDEC Standard)



Vss	1	45	Vss
DQ0	2	46	DQ18
DQ1	3	47	DQ19
DQ2	4	48	DQ20
DQ3	5	49	DQ21
DQ4	6	50	DQ22
DQ5	7	51	DQ23
DQ6	8	52	DQ24
Vcc	9	53	DQ25
DQ7	10	54	NC
NC	11	55	$\overline{OE}$ (Vss)
NC	12	56	Vss
A0	13	57	A1
A2	14	58	A3
Vcc	15	59	A5
A4	16	60	A7
NC	17	61	NC
A6	18	62	NC
A8	19	63	Vss
NC	20	64	NC
NC	21	65	$\overline{RAS1}$
$\overline{RAS0}$	22	66	$\overline{CAS2}$
$\overline{CAS0}$	23	67	Vss
$\overline{CAS1}$	24	68	$\overline{CAS3}$
NC	25	69	$\overline{RAS3}$
$\overline{RAS2}$	26	70	$\overline{WE}$
Vcc	27	71	PD1 (Vss)
PD2 (Vss)	28	72	PD3 (Vss)
PD4 (Vss)	29	73	Vss
PD6 (TBD)	30	74	PD5 (NC)
NC	31	75	PD7 (TBD)
NC	32	76	PD8 (NC)
NC	33	77	NC
DQ9	34	78	NC
NC	35	79	NC
DQ10	36	80	DQ27
Vcc	37	81	DQ28
DQ11	38	82	DQ29
DQ12	39	83	DQ30
DQ13	40	84	DQ31
DQ14	41	85	DQ32
DQ15	42	86	DQ33
DQ16	43	87	DQ34
Vss	44	88	Vss

IC DRAM CARD

4 MEGABYTES

1 MEG x 32, 2 MEG x 16

FEATURES

- JEIDA, JEDEC and PCMCIA standard 88-pin IC DRAM card
- Polarized receptacle connector
- Industry standard DRAM functions and timing
- High-performance, CMOS silicon-gate process
- All outputs are fully TTL compatible
- All inputs buffered except $\overline{RAS}$ inputs
- Multiple $\overline{RAS}$ inputs for x16 or x32 selectability
- Refresh modes: $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$ (CBR), HIDDEN and BATTERY BACKUP (BBU)
- FAST PAGE MODE access cycle
- Single +5V ±5% power supply
- Low power; 8mW standby, 2.2W active (typical)
- Extended refresh standard: 1,024 cycles every 128ms

OPTIONS — MARKING

- Timing

60ns access	-6
70ns access	-7
80ns access	-8

GENERAL DESCRIPTION

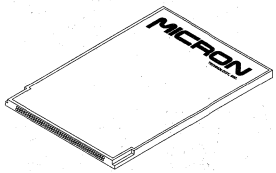
The MT8D88C132 is a 4 megabyte, IC DRAM card organized as a 1 Meg x 32 bit memory array. It may also be configured as a 2 Meg x 16 bit memory array, provided the corresponding DQs on the host system are made common, and memory bank control procedures are implemented. Separate $\overline{CAS}$ inputs allow byte accesses.

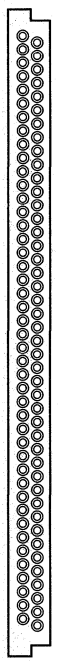
All inputs to the DRAMs are buffered, with the exception of $\overline{RAS}$. The line drivers used for buffers reduce reflections on the card and ensure compatibility in a wide range of systems. At the same time, the line drivers add delays to the buffered input timings when as compared to standard DRAMs.

The MT8D88C132 is designed for low power operation using 1 Meg x 4 low power, extended refresh DRAMs. These devices support BATTERY BACKUP (BBU) cycle refresh; a very low current, data retention mode. Standard component DRAM refresh modes are supported as well.

Multiple $\overline{RAS}$ inputs conserve power by allowing individual bank selection. In the x32 organization, the memory is a single array that may be divided into four separate bytes. In the x16 organization, up to two banks, each with two separate bytes, may be independently selected. One bank is activated by each $\overline{RAS}$ selection; the others not selected remain in standby mode, drawing minimum power.

PIN ASSIGNMENT (End View)
88-Pin Card (U-1)





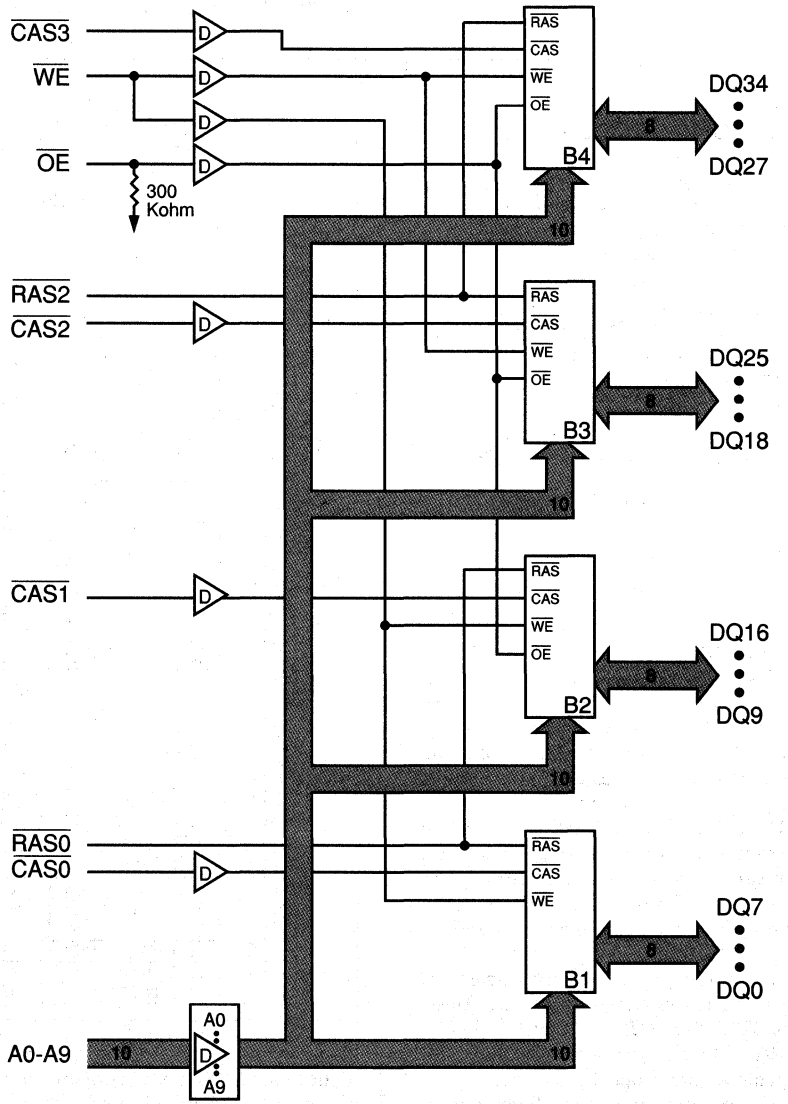
PIN #	SYMBOL	PIN #	SYMBOL	PIN #	SYMBOL
1	Vss	31	NC	61	A9
2	DQ0	32	NC	62	NC
3	DQ1	33	NC	63	Vss
4	DQ2	34	DQ9	64	NC
5	DQ3	35	NC	65	NC
6	DQ4	36	DQ10	66	$\overline{CAS2}$
7	DQ5	37	Vcc	67	Vss
8	DQ6	38	DQ11	68	$\overline{CAS3}$
9	Vcc	39	DQ12	69	NC
10	DQ7	40	DQ13	70	$\overline{WE}$
11	NC	41	DQ14	71	PD1 (Vss)
12	NC	42	DQ15	72	PD3 (Vss)
13	A0	43	DQ16	73	Vss
14	A2	44	Vss	74	PD5 (NC)
15	Vcc	45	Vss	75	PD7 (TBD)
16	A4	46	DQ18	76	PD8 (NC)
17	NC	47	DQ19	77	NC
18	A6	48	DQ20	78	NC
19	A8	49	DQ21	79	NC
20	NC	50	DQ22	80	DQ27
21	NC	51	DQ23	81	DQ28
22	$\overline{RAS0}$	52	DQ24	82	DQ29
23	$\overline{CAS0}$	53	DQ25	83	DQ30
24	$\overline{CAS1}$	54	NC	84	DQ31
25	NC	55	$\overline{OE}$ (Vss)	85	DQ32
26	$\overline{RAS2}$	56	Vss	86	DQ33
27	Vcc	57	A1	87	DQ34
28	PD2 (NC)	58	A3	88	Vss
29	PD4 (Vss)	59	A5		
30	PD6 (TBD)	60	A7		

Eight presence detect pins may be read by the host to identify the MT8D88C132 organization, number of banks, access time and refresh mode. These extensive presence detect functions allow systems to utilize the advanced power-saving features.

The MT8D88C132 is built with a plastic frame covered by stainless steel panels. This package, containing an 88-pin receptacle connector, is keyed to prevent improper installation or insertion into other types of IC card sockets.

NEW ■ IC DRAM CARD

FUNCTIONAL BLOCK DIAGRAM



NOTE: 1. D = 74AC11244 line drivers.
2. B1 through B4 = 1 Meg x 8 memory blocks.
3. $\overline{OE}$ is internally connected to ground via a 300 Kohm resistor and is also buffered to DRAM.

PIN DESCRIPTIONS

PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
22, 26	$\overline{RAS0}$, $\overline{RAS2}$	Input	Row Address Strobe: $\overline{RAS}$ is used to clock-in the 10 row-address bits. Two$\overline{RAS}$ inputs allow for a single x32 bank or two x16 banks.
23, 24, 66, 68	$\overline{CAS}$0-3	Input	Column Address Strobe: $\overline{CAS}$ is used to clock-in the 10 column-address bits, enable the DRAM output buffers, and strobe the data inputs on WRITE cycles. Four $\overline{CAS}$ inputs allow byte access control for any memory bank configuration.
70	$\overline{WE}$	Input	Write Enable: $\overline{WE}$ is the READ/WRITE control for the DQ pins. If $\overline{WE}$ is LOW prior to $\overline{CAS}$ going LOW, the access is an EARLY-WRITE cycle. If $\overline{WE}$ is HIGH while $\overline{CAS}$ is LOW, the access is a READ cycle, provided $\overline{OE}$ is also LOW. If WE goes LOW after $\overline{CAS}$ goes LOW, then the cycle is a LATE-WRITE cycle. A LATE-WRITE cycle is generally used in conjuction with a READ cycle to form a READ-MODIFY-WRITE cycle.
55	$\overline{OE}$	Input	Output Enable: $\overline{OE}$ is the input/output control for the DQ pins. $\overline{OE}$ is connected to ground through a 300 Kohm resistor and is intended to be LOW allowing for EARLY-WRITE cycles only. This signal may be driven, allowing for LATE-WRITE cycles.
13, 57, 14, 58, 16, 59, 18, 60, 19, 61	A0-A9	Input	Address Inputs: These inputs are multiplexed and clocked by $\overline{RAS}$ and $\overline{CAS}$.
2-8, 10, 34, 36, 38-43, 46-53, 80-87	DQ0-DQ34	Input/ Output	Data I/O: For WRITE cycles, DQ0-DQ34 act as inputs to the addressed DRAM location. BYTE WRITEs may be performed by using the corresponding $\overline{CAS}$ select. For READ access cycles, DQ0-DQ34 act as outputs for the addressed DRAM location.
71, 28, 72, 29, 74, 30, 75, 76	PD1-PD8	-	Presence Detect: These pins are read by the host system and tell the system the card's personality. They will be either left floating (NC) or they will be grounded (Vss).
11, 12, 17, 20, 21, 25, 31, 32, 33, 35, 54, 62, 64, 65, 69, 77, 78, 79	NC	-	No Connect: These pins should be left unconnected (reserved for future use).
9, 15, 27, 37	Vcc	Supply	Power Supply: +5V ±5%
1, 44, 45, 56, 63, 67, 73, 88	Vss	Supply	Ground

FUNCTIONAL DESCRIPTION

The MT8D88C132 is a 4 megabyte memory card as a 1 Meg x 32 bit memory array ($\overline{RAS0}$ = $\overline{RAS2}$). It also may be configured as a 2 Meg x 16 bit memory array provided the corresponding DQs on the host are connected and memory bank control procedures are implemented by interleaving both $\overline{RAS}$ lines.

Most x32 bit applications use the same signal to control the $\overline{CAS}$ inputs. $\overline{RAS0}$ controls the lower 16 bits and $\overline{RAS2}$ controls the upper 16 bits to obtain a x32 memory array. For x16 applications, the corresponding DQs and the corresponding $\overline{CAS}$ pins must be connected together (DQ0 to DQ18, DQ1 to DQ19 and so forth, and $\overline{CAS0}$ to $\overline{CAS2}$ and $\overline{CAS1}$ to $\overline{CAS3}$). Each $\overline{RAS}$ is then a bank select for the 2 Meg x 16 memory organization.

DRAM OPERATION

DRAM REFRESH

Memory cell data is retained in its correct state by maintaining power and executing any $\overline{RAS}$ cycle [READ, WRITE, $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$ (CBR), HIDDEN or BATTERY BACKUP (BBU) REFRESH] so that all 1,024 combinations of $\overline{RAS}$ addresses (A0-A9) are executed at least every 128ms, regardless of sequence.

The implied method of choice for refreshing the memory card is the BBU cycle. This is a very low current, data retention mode made possible by using the CBR REFRESH cycle over the extended refresh range (I_{CC7}).

The memory card may be used with the other refresh modes common in standard DRAMs. This allows the memory card to be used on existing systems that do not utilize the BBU REFRESH cycle. However, the penalty is the memory card will draw more current in the STANDBY mode. The CBR REFRESH mode is recommended when not using the BBU mode.

DRAM READ AND WRITE CYCLES

During READ or WRITE cycles, each bit is uniquely addressed through the 20 address bits, which are entered 10 bits (A0-A9) at a time. $\overline{RAS}$ is used to latch the first 10 bits and $\overline{CAS}$ the latter 10 bits. READ or WRITE cycles are selected with the $\overline{WE}$ input. A logic HIGH on $\overline{WE}$ dictates READ mode while a logic LOW on $\overline{WE}$ dictates WRITE mode. During a WRITE cycle, data in (D) is latched by the falling edge of $\overline{CAS}$. $\overline{WE}$ must fall prior to $\overline{CAS}$ (EARLY WRITE); if $\overline{WE}$ goes LOW after $\overline{CAS}$, the outputs (Q) will be activated and will drive invalid data to the inputs, unless LATE-WRITE cycle timing specifications are met. The data inputs and data outputs are routed through pins using common I/O, and pin direction is controlled by $\overline{WE}$.

FAST PAGE MODE operation allows faster data operations (READ or WRITE) within a row address (A0-A9) defined page boundary. The FAST PAGE MODE cycle is always initiated with a row address strobed-in by $\overline{RAS}$ followed by a column address strobed-in by $\overline{CAS}$. $\overline{CAS}$ may be toggled-in by holding $\overline{RAS}$ LOW and strobing-in different column addresses, thus executing faster memory cycles. Returning $\overline{RAS}$ HIGH terminates the FAST PAGE MODE operation. Returning $\overline{RAS}$ and $\overline{CAS}$ HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the $\overline{RAS}$ high time.

DRAM TIMING

In accordance with JEDEC standard specifications, all inputs to the IC DRAM card are buffered, with the exception of $\overline{RAS}$ inputs. The line drivers used for buffers reduce reflections on the card and ensure compatibility in a wide range of systems. The implementation of buffers on the card may relieve the need for additional host system line drivers. Notes 23 though 29 indicate which parameters on the IC DRAM card are affected by the line drivers, and to what magnitude they are affected. The component DRAM timing specifications, rather than those of the IC DRAM card (in systems which use both), may cause timing incompatibilities.

All traces on the IC DRAM card (buffered and non-buffered) are approximately 50 ohms characteristic impedance. Matching impedance on the system board to 50 ohms characteristic impedance on traces to the IC DRAM card will decrease signal noise to the IC DRAM card, enhancing overall system reliability.

PHYSICAL DESIGN

The MT8D88C132 is constructed with a molded plastic frame and covered with stainless steel panels. Inside, eight thin small-outline package (TSOP) DRAMs are mounted on an ultrathin printed circuit board. The board is attached to a high insertion, 88-pin receptacle connector. The package has a polarized key to prevent improper installation, including insertion into other types of IC card sockets. The MT8D88C132 operates reliably up to 55°C.

MEMORY TRUTH TABLE

FUNCTION		RAS	CAS	WE	OE	ADDRESSES tR	ADDRESSES tC	DATA IN/OUT DQ0-DQ34
Standby		H	H→X	X	X	X	X	High-Z
READ		L	L	H	L (NC)	ROW	COL	Data Out
EARLY-WRITE		L	L	L	X	ROW	COL	Data In
READ-WRITE		L	L	H→L	L→H	ROW	COL	Data Out
FAST-PAGE-MODE	1st Cycle	L	H→L	H	L (NC)	ROW	COL	Data Out
READ	2nd Cycle	L	H→L	H	L (NC)	n/a	COL	Data Out
FAST-PAGE-MODE	1st Cycle	L	H→L	L	X	ROW	COL	Data In
EARLY-WRITE	2nd Cycle	L	H→L	L	X	n/a	COL	Data In
FAST-PAGE-MODE	1st Cycle	L	H→L	H→L	L→H	ROW	COL	Data In
READ-WRITE	2nd Cycle	L	H→L	H→L	L→H	n/a	COL	Data In
RAS-ONLY REFRESH		L	X	X	X	ROW	n/a	High-Z
HIDDEN	READ	L→H→L	L	H	L (NC)	ROW	COL	Data Out
REFRESH	WRITE	L→H→L	L	L	X	ROW	COL	Data In
CAS-BEFORE-RAS REFRESH		H→L	L	H	X	X	X	High-Z
BATTERY BACKUP REFRESH		H→L	L	H	X	X	X	High-Z

PRESENCE DETECT TRUTH TABLE

CHARACTERISTICS						PRESENT DETECT PIN (PDx)							
Card Density	DRAM Organizations	Card Address	RAS Address	CAS Address	Page Depth	1	2	3	4	5	6	7	8
0MB	No card installed	X	X	X	X	NC	NC	NC	NC	NC	X	X	X
1MB	256K x 1, 4, 16, 18	18	9	9	512	Vss	Vss	Vss	Vss	NC	X	X	X
2MB	256K x 1, 4, 16, 18	18	9	9	512	Vss	Vss	Vss	Vss	Vss	X	X	X
2MB	512K x 8, 9	19	10	9	512	NC	Vss	Vss	Vss	NC	X	X	X
4MB	512K x 8, 9	19	10	9	512	NC	Vss	Vss	Vss	Vss	X	X	X
• 4MB	1 Meg x 1, 4, 16, 18	20	10	10	1,024	Vss	NC	Vss	Vss	NC	X	X	X
8MB	1 Meg x 1, 4, 16, 18	20	10	10	1,024	Vss	NC	Vss	Vss	Vss	X	X	X
8MB	2 Meg x 8, 9	21	11	10	1,024	NC	NC	Vss	Vss	NC	X	X	X
16MB	2 Meg x 8, 9	21	11	10	1,024	NC	NC	Vss	Vss	Vss	X	X	X
16MB	4 Meg x 1, 4, 16, 18	22	12	11	1,024	Vss	Vss	NC	Vss	NC	X	X	X
32MB	4 Meg x 1, 4, 16, 18	22	12	11	1,024	Vss	Vss	NC	Vss	Vss	X	X	X
Access Timing		100ns				X	X	X	X	X	Vss	Vss	X
		80ns				X	X	X	X	X	NC	Vss	X
		70ns				X	X	X	X	X	Vss	NC	X
		60ns				X	X	X	X	X	NC	NC	X
		50ns				X	X	X	X	X	Vss	Vss	X
Refresh Control		Standard				X	X	X	X	X	X	X	NC
		Auto				X	X	X	X	X	X	X	Vss

NOTE: Vss = Ground.

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} ..... -0.5V to +5.25V
Operating Temperature, T_A (Ambient) ..... 0°C to +55°C
Storage Temperature ..... -20°C to +80°C
Power Dissipation 15W
Short Circuit Output Current 50mA
Card Insertions (Connector's Life Cycle) 10,000

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 3, 4, 6, 7) (0°C ≤ T_A ≤ 55°C; V_{CC} = 5V ±5%)

PARAMETER/CONDITION		SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage		V_{CC}	4.75	5.25	V	1
Input High (Logic 1) Voltage, All Inputs		V_{IH}	3.5	V_{CC}+0.5	V	1
Input Low (Logic 0) Voltage, All Inputs		V_{IL}	-0.5	0.8	V	1
INPUT LEAKAGE CURRENT, Any input	Non-buffered	I_{IN}	-12	12	µA	
(0V ≤ V_{IN} ≤ 5.25V; all other pins not under test = 0V)	Buffered	I_{IB}	-2	2	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled; 0V ≤ V_{OUT} ≤ 5.25V)		I_{OZ}	-10	10	µA	
OUTPUT LEVELS Output High Voltage (I_{OUT} = -5mA)		V_{OH}	2.4		V	
Output Low Voltage (I_{OUT} = 4.2mA)		V_{OL}		0.4	V	

PARAMETER/CONDITION	SYMBOL	MAX -6	MAX -7	MAX -8	UNITS	NOTES
STANDBY CURRENT: (TTL) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC1}	16	16	16	mA	
STANDBY CURRENT: (CMOS) ($\overline{RAS}$ = $\overline{CAS}$ = Other Inputs = V_{CC} -0.2V)	I_{CC2}	1.6	1.6	1.6	mA	
OPERATING CURRENT: Random READ/WRITE Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC (MIN))	I_{CC3}	840	760	680	mA	3, 4, 30
OPERATING CURRENT: FAST PAGE MODE Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: ^tPC = ^tPC (MIN))	I_{CC4}	600	520	440	mA	3, 4, 30
REFRESH CURRENT: $\overline{RAS}$-ONLY Average power supply current ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}: ^tRC = ^tRC (MIN))	I_{CC5}	840	760	680	mA	3, 30
REFRESH CURRENT: $\overline{CAS}$-BEFORE-$\overline{RAS}$ (CBR) Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC (MIN))	I_{CC6}	840	760	680	mA	3, 5, 30
REFRESH CURRENT: BATTERY BACKUP (BBU) Average power supply current during BBU: $\overline{CAS}$ = 0.2V or CBR cycling; $\overline{RAS}$ = ^tRAS (MIN) up to 300ns; ^tRC = 125µs; $\overline{WE}$, A0-A9 and DQ = Vcc -0.2V or 0.2V (DQ may be left open)	I_{CC7}	2.4	2.4	2.4	mA	3, 5

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: $\overline{CAS0}$, $\overline{CAS1}$, $\overline{CAS2}$, $\overline{CAS3}$, A0-A9, $\overline{OE}$	C_{I1}		9	pF	2
Input Capacitance: $\overline{WE}$	C_{I2}		13	pF	2
Input Capacitance: $\overline{RAS0}$, $\overline{RAS2}$	C_{I3}		50	pF	2
Input/Output Capacitance: DQ	C_{IO}		12	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C ≤ T_A ≤ 55°C; Vcc = 5V ±5%)

AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	^tRC	110		130		150		ns	23
FAST-PAGE-MODE READ or WRITE cycle time	^tPC	40		40		45		ns	23
Access time from $\overline{RAS}$	^tRAC		60		70		80	ns	14, 23
Access time from $\overline{CAS}$	^tCAC		25		30		30	ns	15, 26
Access time from column address	^tAA		40		45		50	ns	26
Access time from $\overline{CAS}$ precharge	^tCPA		50		50		55	ns	26
$\overline{RAS}$ pulse width	^tRAS	60	100,000	70	100,000	80	100,000	ns	23
$\overline{RAS}$ pulse width (FAST PAGE MODE)	^tRASP	60	100,000	70	100,000	80	100,000	ns	23
$\overline{RAS}$ hold time	^tRSH	25		30		30		ns	26
$\overline{RAS}$ precharge time	^tRP	45		50		60		ns	23
$\overline{CAS}$ pulse width	^tCAS	15	100,000	20	100,000	20	100,000	ns	23
$\overline{CAS}$ hold time	^tCSH	55		65		75		ns	25
$\overline{CAS}$ precharge time	^tCPN	10		10		10		ns	16, 23
$\overline{CAS}$ precharge time (FAST PAGE MODE)	^tCP	10		10		10		ns	23
$\overline{RAS}$ to $\overline{CAS}$ delay time	^tRCD	10	35	15	40	15	50	ns	17, 28
$\overline{CAS}$ to $\overline{RAS}$ precharge time	^tCRP	15		15		15		ns	26
Row address setup time	^tASR	10		10		10		ns	26
Row address hold time	^tRAH	5		5		5		ns	25
$\overline{RAS}$ to column address delay time	^tRAD	10	20	10	25	10	30	ns	18, 28
Column address setup time	^tASC	5		5		5		ns	24
Column address hold time	^tCAH	15		20		20		ns	24
Column address hold time (referenced to $\overline{RAS}$)	^tAR	45		50		55		ns	25
Column address to $\overline{RAS}$ lead time	^tRAL	40		45		50		ns	26
Read command setup time	^tRCS	5		5		5		ns	25
Read command hold time (referenced to $\overline{CAS}$)	^tRCH	5		5		5		ns	19, 24
Read command hold time (referenced to $\overline{RAS}$)	^tRRH	-5		-5		-5		ns	19, 25
$\overline{CAS}$ to output in Low-Z	^tCLZ	5		5		5		ns	24
Output buffer turn-off delay	^tOFF	5	30	5	30	5	30	ns	20, 29, 35
$\overline{WE}$ command setup time	^tWCS	5		5		5		ns	24

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C ≤ T_A ≤ 55°C; Vcc = 5V ±5%)

AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Write command hold time	tWCH	15		20		20		ns	24
Write command hold time (referenced to $\overline{RAS}$)	tWCR	40		50		55		ns	25
Write command pulse width	tWP	10		15		15		ns	23
Write command to $\overline{RAS}$ lead time	tRWL	25		30		30		ns	26
Write command to $\overline{CAS}$ lead time	tCWL	20		25		25		ns	24
Data-in setup time	tDS	5		5		5		ns	24, 32
Data-in hold time	tDH	5		10		10		ns	25, 32
Data-in hold time (referenced to $\overline{RAS}$)	tDHR	45		55		60		ns	23
Transition time (rise or fall)	tT	2	15	2	15	2	15	ns	9, 10, 23
Refresh period (1,024 cycles)	tREF		128		128		128	ms	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	tRPC	10		10		10		ns	26
$\overline{CAS}$ setup time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	tCSR	20		20		20		ns	5, 26
$\overline{CAS}$ hold time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	tCHR	10		10		10		ns	5, 25
$\overline{WE}$ hold time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	tWRH	5		5		5		ns	22, 25
$\overline{WE}$ setup time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	tWRP	20		20		20		ns	22, 26
$\overline{WE}$ hold time (WCBR test cycle)	tWTH	5		5		5		ns	22, 25
$\overline{WE}$ setup time	tWTS	20		20		20		ns	22, 26
READ-WRITE cycle time	tRWC	165		185		205		ns	
FAST-PAGE-MODE READ-WRITE cycle time	tPRWC	90		95		100		ns	23
$\overline{RAS}$ to $\overline{WE}$ delay time	tRWD	80		90		100		ns	31, 27
Column Address to $\overline{WE}$ delay time	tAWD	65		70		75		ns	31, 24
$\overline{CAS}$ to $\overline{WE}$ delay time	tCWD	50		65		55		ns	31, 24
Output buffer turn-off delay	tOE		25		30		30	ns	20, 33, 26
Output disable	tOD		25		30		30	ns	35, 26
$\overline{OE}$ hold time from $\overline{WE}$ during READ-MODIFY-WRITE cycle	tOEH	5		10		10		ns	34, 27
$\overline{OE}$ hold time from $\overline{RAS}$ during HIDDEN REFRESH cycle	tORD	10		10		10		ns	21, 26

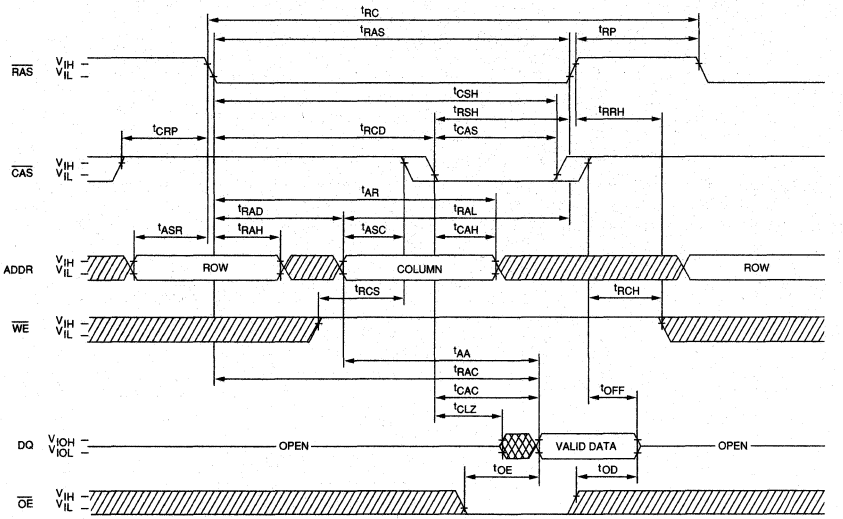
NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. V_{CC} = 5V ±10%, f = 1 MHz.
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is assured.
7. An initial pause of 100µs is required after power-up followed by eight $\overline{RAS}$ refresh cycles ($\overline{RAS}$-ONLY or CBR with $\overline{WE}$ HIGH) before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-up should be repeated any time the ^{t}REF refresh requirement is exceeded.
8. AC characteristics assume ^{t}T = 5ns.
9. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS}$ = V_{IH}, data output is High-Z.
12. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to 2 TTL gates and 100pF.
14. Assumes that $^{t}RCD < {}^{t}RCD$ (MAX). If ^{t}RCD is greater than the maximum recommended value shown in this table, ^{t}RAC will increase by the amount that ^{t}RCD exceeds the value shown.
15. Assumes that $^{t}RCD \geq {}^{t}RCD$ (MAX).
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer, $\overline{CAS}$ must be pulsed HIGH for ^{t}CPN.
17. Operation within the ^{t}RCD (MAX) limit ensures that ^{t}RAC (MAX) can be met. ^{t}RCD (MAX) is specified as a reference point only; if ^{t}RCD is greater than the specified ^{t}RCD (MAX) limit, then access time is controlled exclusively by ^{t}CAC.
18. Operation within the ^{t}RAD (MAX) limit ensures that ^{t}RCD (MAX) can be met. ^{t}RAD (MAX) is specified as a reference point only; if ^{t}RAD is greater than the specified ^{t}RAD (MAX) limit, then access time is controlled exclusively by ^{t}AA.
19. Either ^{t}RCH or ^{t}RRH must be satisfied for a READ cycle.
20. ^{t}OFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
21. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW.
22. ^{t}WTS and ^{t}WTH are setup and hold specifications for the $\overline{WE}$ pin being held LOW to enable the JEDEC test mode (with CBR timing constraints). These two parameters are the inverse of ^{t}WRP and ^{t}WRH in the CBR refresh cycle.
23. Timing between the DRAMs and the DRAM card did not change with the addition of the line drivers.
24. A +5ns timing skew from the DRAM to the DRAM card resulted from the addition of line drivers.
25. A -5ns timing skew from the DRAM to the DRAM card resulted from the addition of line drivers.
26. A +10ns timing skew from the DRAM to the DRAM card resulted from the addition of line drivers.
27. A -10ns timing skew from the DRAM to the DRAM card resulted from the addition of line drivers.
28. A -5ns (MIN) and a -10ns (MAX) timing skew from the DRAM to the DRAM card resulted from the addition of line drivers.
29. A +5ns (MIN) and a +10ns (MAX) timing skew from the DRAM to the DRAM card resulted from the addition of line drivers.
30. The maximum current ratings are based with the memory operating or being refreshed in the x32 mode. The stated maximums may be reduced by one half when used in the x16 mode.
31. ^{t}WCS, ^{t}RWD, ^{t}AWD and ^{t}CWD are restrictive operating parameters in late WRITE, and READ-MODIFY-WRITE cycles only. If $^{t}WCS \geq {}^{t}WCS$ (MIN), the cycle is an EARLY-WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If $^{t}RWD \geq {}^{t}RWD$ (MIN), $^{t}AWD \geq {}^{t}AWD$ (MIN) and $^{t}CWD \geq {}^{t}CWD$ (MIN), the cycle is a READ-MODIFY-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of data out is indeterminate. $\overline{OE}$ held HIGH and $\overline{WE}$ taken LOW after $\overline{CAS}$ goes LOW results in a LATE-WRITE ($\overline{OE}$ controlled) cycle.

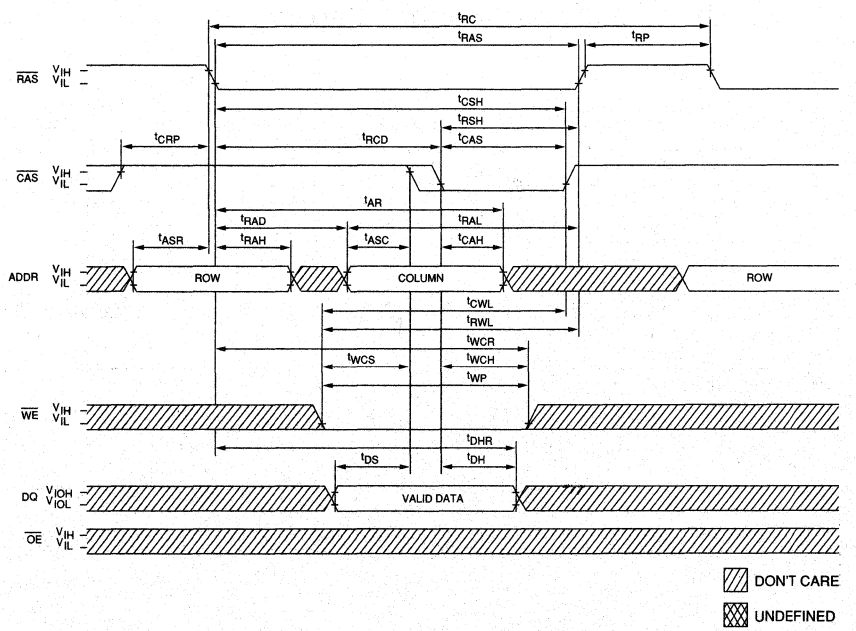
NOTES (continued)

32. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY-WRITE cycles and $\overline{WE}$ leading edge in LATE-WRITE or READ-MODIFY-WRITE cycles.
33. If $\overline{OE}$ is tied permanently LOW, LATE-WRITE or READ-MODIFY-WRITE operations are not possible.
34. LATE-WRITE and READ-MODIFY-WRITE cycles must have both ^{t}OD and ^{t}OEH met ($\overline{OE}$ HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. The DQs will provide the previously read data if $\overline{CAS}$ remains LOW and $\overline{OE}$ is taken back LOW after ^{t}OEH is met. If $\overline{CAS}$ goes HIGH prior to $\overline{OE}$ going back LOW, the DQs will remain open.
35. The DQs open during READ cycles once ^{t}OD or ^{t}OFF occur. If $\overline{CAS}$ goes HIGH first, $\overline{OE}$ becomes a "don't care." If $\overline{OE}$ goes HIGH and $\overline{CAS}$ stays LOW, $\overline{OE}$ is not a "don't care;" and the DQs will provide the previously read data if $\overline{OE}$ is taken back LOW (while $\overline{CAS}$ remains LOW).

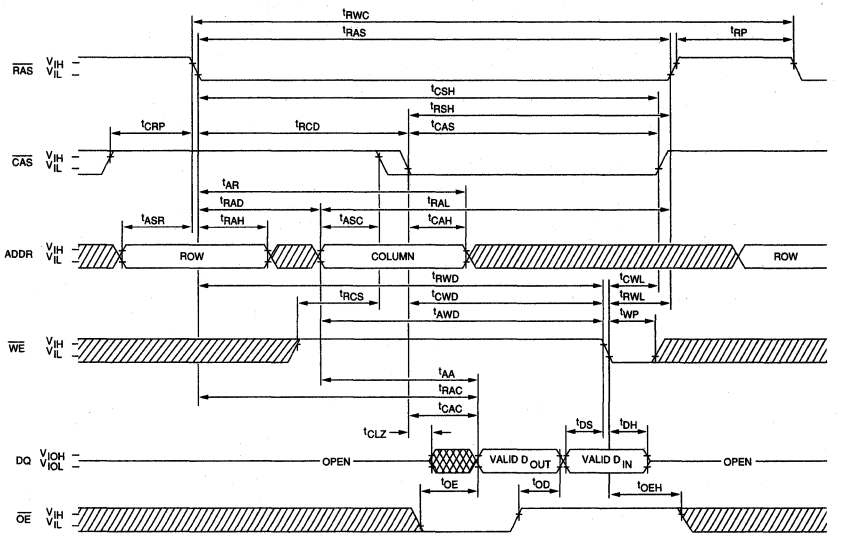
READ CYCLE



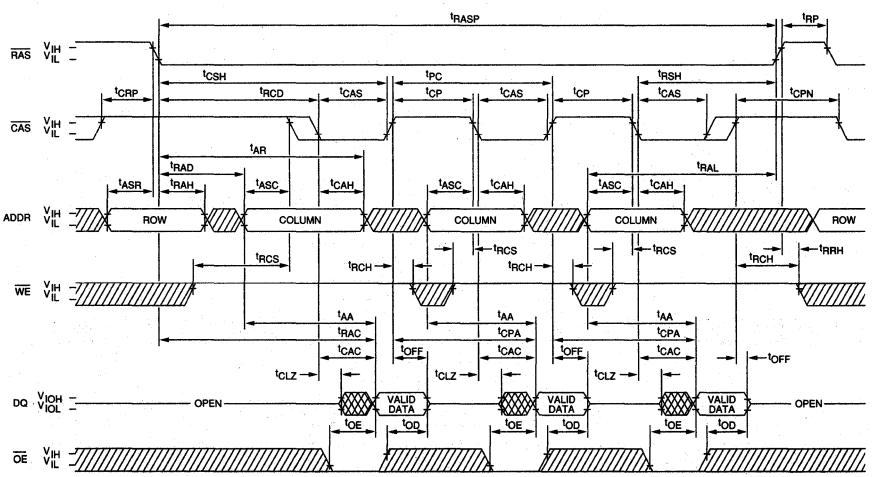
EARLY-WRITE CYCLE



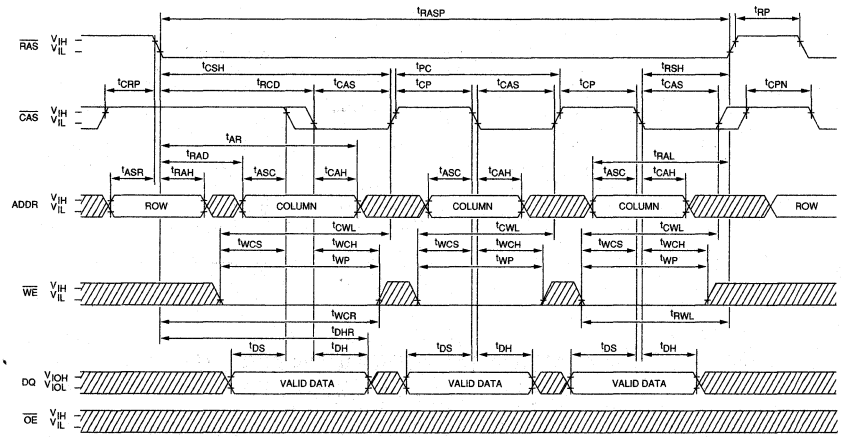
READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)



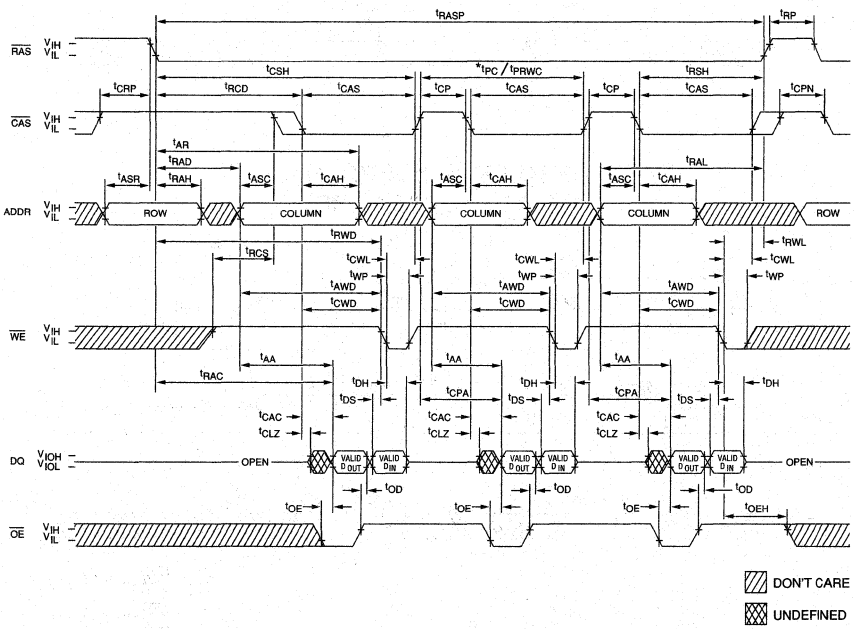
FAST-PAGE-MODE READ CYCLE



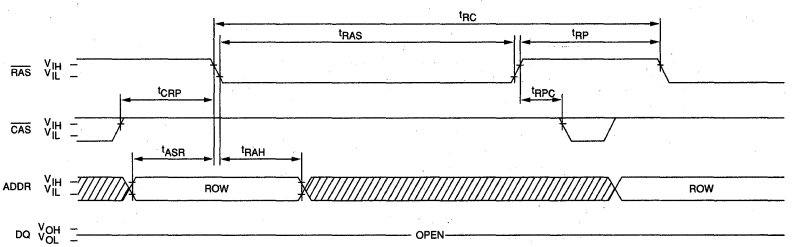
FAST-PAGE-MODE EARLY-WRITE CYCLE



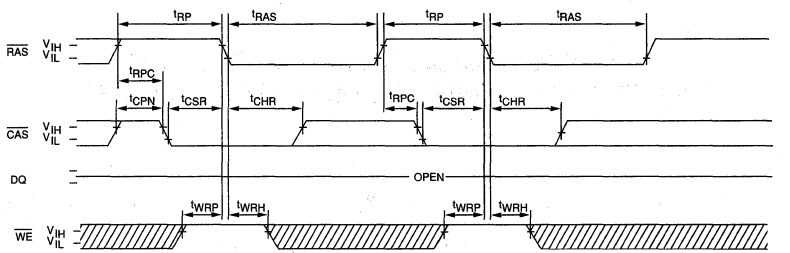
FAST-PAGE-MODE READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)



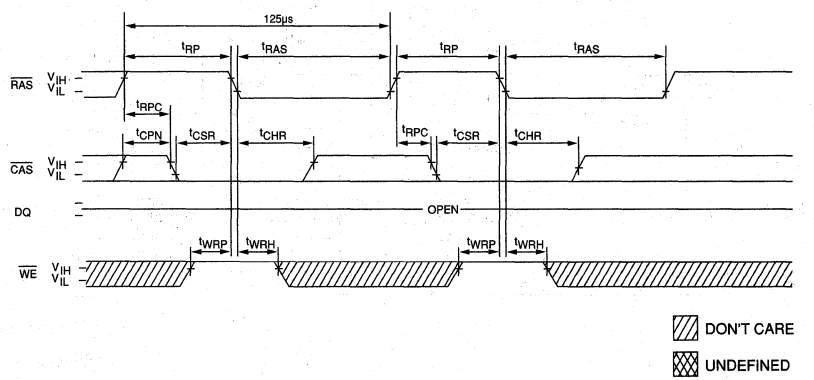
$\overline{\text{RAS}}$-ONLY REFRESH CYCLE
(ADDR = A0-A9; $\overline{\text{WE}}$ = DON'T CARE)



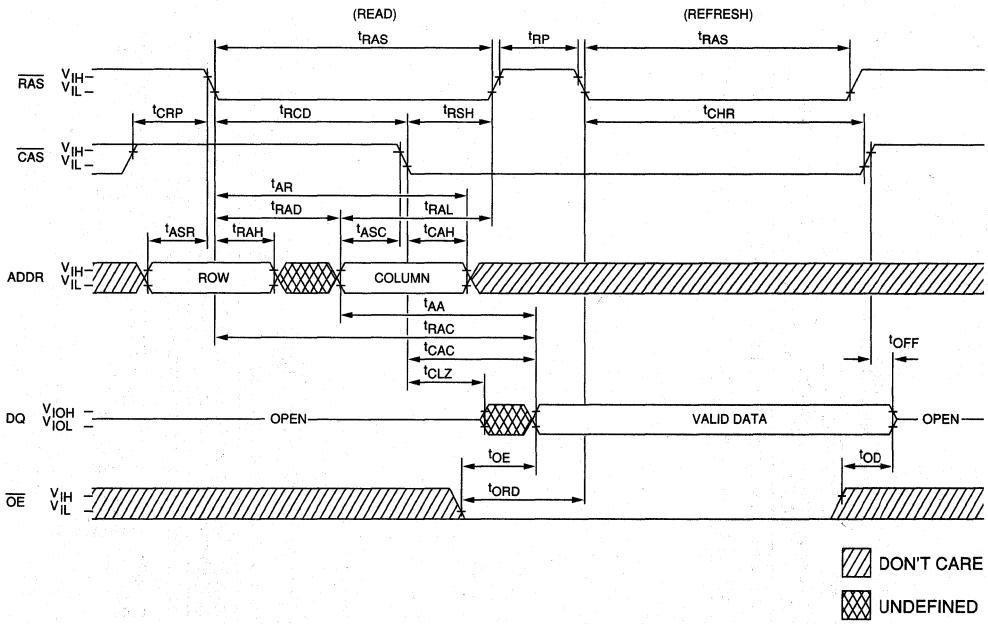
$\overline{\text{CAS}}$-BEFORE-$\overline{\text{RAS}}$ REFRESH CYCLE
(A0-A9 = DON'T CARE)



BATTERY BACKUP REFRESH CYCLE
(A0-A9 = DON'T CARE)

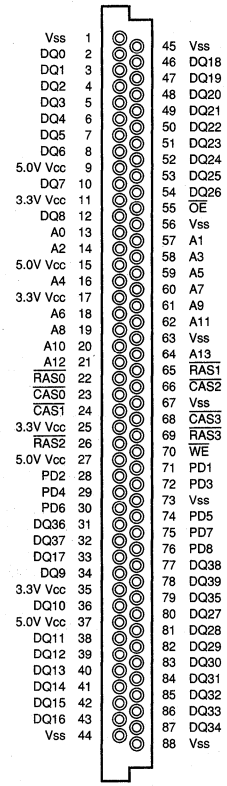


HIDDEN REFRESH CYCLE [21]
($\overline{WE}$ = HIGH)

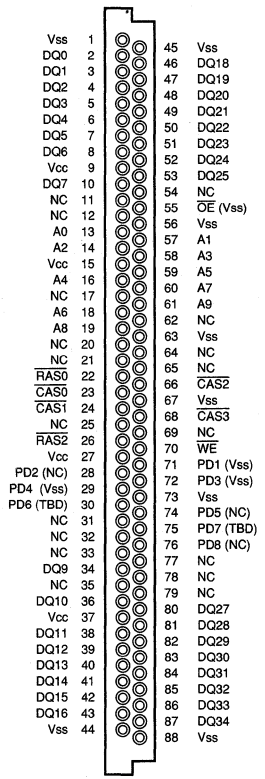


NEW ■ IC DRAM CARD

RESERVED JEDEC, JEIDA and PCMCIA 88-PIN ASSIGNMENT
(All Possible Combinations)



MT8D88C132 PIN ASSIGNMENT
(JEDEC Standard)



IC DRAM CARD 8 MEGABYTES

2 MEG x 32, 4 MEG x 16

NEW ■ IC DRAM CARD

FEATURES

- JEIDA, JEDEC and PCMCIA standard 88-pin IC DRAM card
- Polarized receptacle connector
- Industry standard DRAM functions and timing
- High-performance, CMOS silicon-gate process
- All outputs are fully TTL compatible
- All inputs buffered except $\overline{RAS}$ inputs
- Multiple $\overline{RAS}$ inputs for x16 or x32 selectability
- Refresh modes: $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$ (CBR), HIDDEN and BATTERY BACKUP (BBU)
- FAST PAGE MODE access cycle
- Single +5V ±5% power supply
- Low power; 16mW standby, 2.2W active (typical)
- Extended refresh standard: 1,024 cycles every 128ms

OPTIONS MARKING

- Timing

60ns access	-6
70ns access	-7
80ns access	-8

GENERAL DESCRIPTION

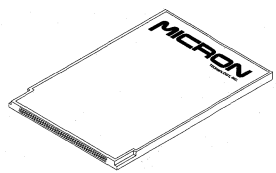
The MT16D88C232 is an 8 megabyte, IC DRAM card organized as a 2 Meg x 32 bit memory array. It may also be configured as a 4 Meg x 16 bit memory array, provided the corresponding DQs on the host system are made common and memory bank control procedures are implemented. Separate $\overline{CAS}$ inputs allow byte accesses.

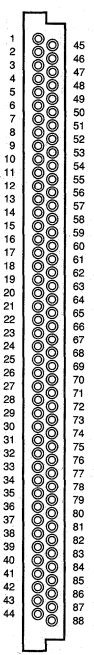
All inputs to the DRAMs are buffered, with the exception of $\overline{RAS}$. The line drivers used for buffers reduce reflections on the card and ensure compatibility in a wide range of systems. At the same time, the line drivers add delays to the buffered input timings when compared to standard DRAMs.

The MT16D88C232 is designed for low power operation using 1 Meg x 4 low power, extended refresh DRAMs. These devices support BATTERY BACKUP (BBU) cycle refresh; a very low current, data retention mode. Standard component DRAM refresh modes are supported as well.

Multiple $\overline{RAS}$ inputs conserve power by allowing individual bank selection. In the x32 organization, the memory array may be divided into two banks, each with four separate bytes. In the x16 organization, up to four banks, each with two separate bytes, may be independently selected. One bank is activated by each $\overline{RAS}$ selection; the others not selected remain in standby mode, drawing minimum power.

PIN ASSIGNMENT (End View)
88-Pin Card (U-1)





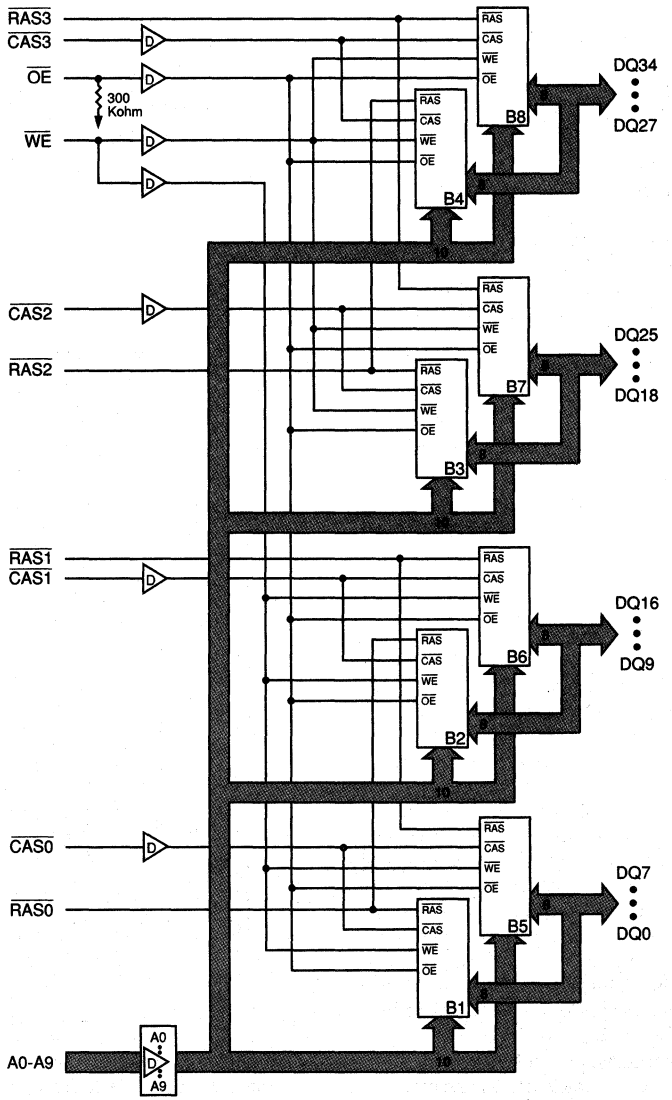
PIN #	SYMBOL	PIN #	SYMBOL	PIN #	SYMBOL
1	Vss	31	NC	61	A9
2	DQ0	32	NC	62	NC
3	DQ1	33	NC	63	Vss
4	DQ2	34	DQ9	64	NC
5	DQ3	35	NC	65	$\overline{RAS1}$
6	DQ4	36	DQ10	66	$\overline{CAS2}$
7	DQ5	37	Vcc	67	Vss
8	DQ6	38	DQ11	68	$\overline{CAS3}$
9	Vcc	39	DQ12	69	$\overline{RAS3}$
10	DQ7	40	DQ13	70	$\overline{WE}$
11	NC	41	DQ14	71	PD1 (Vss)
12	NC	42	DQ15	72	PD3 (Vss)
13	A0	43	DQ16	73	Vss
14	A2	44	Vss	74	PD5 (Vss)
15	Vcc	45	Vss	75	PD7 (TBD)
16	A4	46	DQ18	76	PD8 (NC)
17	NC	47	DQ19	77	NC
18	A6	48	DQ20	78	NC
19	A8	49	DQ21	79	NC
20	NC	50	DQ22	80	DQ27
21	NC	51	DQ23	81	DQ28
22	$\overline{RAS0}$	52	DQ24	82	DQ29
23	$\overline{CAS0}$	53	DQ25	83	DQ30
24	$\overline{CAS1}$	54	NC	84	DQ31
25	NC	55	$\overline{OE}$ (Vss)	85	DQ32
26	$\overline{RAS2}$	56	Vss	86	DQ33
27	Vcc	57	A1	87	DQ34
28	PD2 (NC)	58	A3	88	Vss
29	PD4 (Vss)	59	A5		
30	PD6 (TBD)	60	A7		

Eight presence detect pins may be read by the host to identify the MT16D88C232 organization, number of banks, access time and refresh mode. These extensive presence detect functions allow systems to utilize the advanced power-saving features.

The MT16D88C232 is built with a plastic frame covered by stainless steel panels. This package, containing an 88-pin receptacle connector, is keyed to prevent improper installa-

NEW ■ IC DRAM CARD

FUNCTIONAL BLOCK DIAGRAM



NOTE: 1. D = 74AC11244 line drivers.
2. B1 through B8 = 1 Meg x 8 memory blocks.
3. $\overline{OE}$ is internally connected to ground via a 300 Kohm resistor and is also buffered to DRAM.

PIN DESCRIPTIONS

PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
22, 26, 65, 69	$\overline{RAS}$0-3	Input	Row Address Strobe: $\overline{RAS}$ is used to clock-in the 10 row-address bits. Four $\overline{RAS}$ inputs allow for two x32 banks or four x16 banks.
23, 24, 66, 68	$\overline{CAS}$0-3	Input	Column Address Strobe: $\overline{CAS}$ is used to clock-in the 10 column-address bits, enable the DRAM output buffers, and strobe the data inputs on WRITE cycles. Four $\overline{CAS}$ inputs allow byte access control for any memory bank configuration.
70	$\overline{WE}$	Input	Write Enable: $\overline{WE}$ is the READ/WRITE control for the DQ pins. If $\overline{WE}$ is LOW prior to $\overline{CAS}$ going LOW, the access is an EARLY-WRITE cycle. If $\overline{WE}$ is HIGH while $\overline{CAS}$ is LOW, the access is a READ cycle, provided $\overline{OE}$ is also LOW. If WE goes LOW after $\overline{CAS}$ goes LOW, then the cycle is a LATE-WRITE cycle. A LATE-WRITE cycle is generally used in conjuction with a READ cycle to form a READ-MODIFY-WRITE cycle.
55	$\overline{OE}$	Input	Output Enable: $\overline{OE}$ is the input/output control for the DQ pins. $\overline{OE}$ is connected to ground through a 300 Kohm resistor and is intended to be LOW allowing for EARLY-WRITE cycles only. This signal may be driven, allowing for LATE-WRITE cycles.
13, 57, 14, 58, 16, 59, 18, 60, 19, 61	A0-A9	Input	Address Inputs: These inputs are multiplexed and clocked by $\overline{RAS}$ and $\overline{CAS}$.
2-8, 10, 34, 36, 38-43, 46-53, 80-87	DQ0-DQ34	Input/ Output	Data I/O: For WRITE cycles, DQ0-DQ34 act as inputs to the addressed DRAM location. BYTE WRITEs may be performed by using the corresponding $\overline{CAS}$ select. For READ access cycles, DQ0-DQ34 act as outputs for the addressed DRAM location.
71, 28, 72, 29, 74, 30, 75, 76	PD1-PD8	-	Presence Detect: These pins are read by the host system and tell the system the card's personality. They will be either left floating (NC) or they will be grounded (Vss).
11, 12, 17, 20, 21, 25, 31, 32, 33, 35, 54, 62, 64, 77, 78, 79	NC	-	No Connect: These pins should be left unconnected (reserved for future use).
9, 15, 27, 37	Vcc	Supply	Power Supply: +5V ±5%
1, 44, 45, 56, 63, 67, 73, 88	Vss	Supply	Ground

FUNCTIONAL DESCRIPTION

The MT16D88C232 is an 8 megabyte memory card structured as a 2 Meg x 32 bit memory array ($\overline{RAS0}$ = $\overline{RAS2}$, $\overline{RAS1}$ = $\overline{RAS3}$). It also may be configured as a 4 Meg x 16 bit memory array provided the corresponding DQs on the host are connected and memory bank control procedures are implemented by interleaving all four $\overline{RAS}$ lines.

Most x32 bit applications use the same signal to control the $\overline{CAS}$ inputs. $\overline{RAS0}$ and $\overline{RAS1}$ control the lower 16 bits, and $\overline{RAS2}$ and $\overline{RAS3}$ control the upper 16 bits to obtain a x32 memory array. For x16 applications, the corresponding DQs and the corresponding $\overline{CAS}$ pins must be connected together (DQ0 to DQ18, DQ1 to DQ19 and so forth, and $\overline{CAS0}$ to $\overline{CAS2}$ and $\overline{CAS1}$ to $\overline{CAS3}$). Each $\overline{RAS}$ is then a bank select for the 4 Meg x 16 memory organization.

DRAM OPERATION

DRAM REFRESH

Memory cell data is retained in its correct state by maintaining power and executing any $\overline{RAS}$ cycle [READ, WRITE, $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$ (CBR), HIDDEN or BATTERY BACKUP (BBU) REFRESH] so that all 1,024 combinations of $\overline{RAS}$ addresses (A0-A9) are executed at least every 128ms, regardless of sequence.

The implied method of choice for refreshing the memory card is the BBU cycle. This is a very low current, data retention mode made possible by using the CBR REFRESH cycle over the extended refresh range (I_{CC7}).

The memory card may be used with the other refresh modes common in standard DRAMs. This allows the memory card to be used on existing systems that do not utilize the BBU REFRESH cycle. However, the memory card will draw more current in the STANDBY mode. The CBR REFRESH mode is recommended when not using the BBU mode.

DRAM READ AND WRITE CYCLES

During READ or WRITE cycles, each bit is uniquely addressed through the 20 address bits, which are entered 10 bits (A0-A9) at a time. $\overline{RAS}$ is used to latch the first 10 bits and $\overline{CAS}$ the latter 10 bits. READ or WRITE cycles are selected with the $\overline{WE}$ input. A logic HIGH on $\overline{WE}$ dictates READ mode while a logic LOW on $\overline{WE}$ dictates WRITE mode. During a WRITE cycle, data in (D) is latched by the falling edge of $\overline{CAS}$. $\overline{WE}$ must fall prior to $\overline{CAS}$ (EARLY WRITE); if $\overline{WE}$ goes LOW after $\overline{CAS}$, the outputs (Q) will be activated and will drive invalid data to the inputs, unless LATE-WRITE cycle timing specifications are met. The data inputs and data outputs are routed through pins using common I/O, and pin direction is controlled by $\overline{WE}$.

FAST PAGE MODE operation allows faster data operations (READ or WRITE) within a row address (A0-A9) defined page boundary. The FAST PAGE MODE cycle is always initiated with a row address strobed-in by $\overline{RAS}$ followed by a column address strobed-in by $\overline{CAS}$. $\overline{CAS}$ may be toggled-in by holding $\overline{RAS}$ LOW and strobing-in different column addresses, thus executing faster memory cycles. Returning $\overline{RAS}$ HIGH terminates the FAST PAGE MODE operation. Returning $\overline{RAS}$ and $\overline{CAS}$ HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the $\overline{RAS}$ high time.

DRAM TIMING

In accordance with JEDEC standard specifications, all inputs to the IC DRAM card are buffered, with the exception of $\overline{RAS}$ inputs. The line drivers used for buffers reduce reflections on the card and ensure compatibility in a wide range of systems. The implementation of buffers on the card may relieve the need for additional host system line drivers. Notes 23 though 29 indicate which parameters on the IC DRAM card are affected by the line drivers, and to what magnitude they are affected. The component DRAM timing specifications, rather than those of the IC DRAM card (in systems that use both), may cause timing incompatibilities.

All traces on the IC DRAM card (buffered and non-buffered) are approximately 50 ohms characteristic impedance. Matching impedance on the system board to 50 ohms characteristic impedance on traces to the IC DRAM card will decrease signal noise to the IC DRAM card, enhancing overall system reliability.

PHYSICAL DESIGN

The MT16D88C232 is constructed with a molded plastic frame and covered with stainless steel panels. Inside, 16 thin small-outline package (TSOP) DRAMs are mounted on both sides of an ultrathin printed circuit board. The board is attached to a high insertion, 88-pin receptacle connector. The package has a polarized key to prevent improper installation, including insertion into other types of IC card sockets. The MT16D88C232 operates reliably up to 55°C.

MEMORY TRUTH TABLE

FUNCTION		RAS	CAS	WE	OE	ADDRESSES tR	ADDRESSES tC	DATA IN/OUT DQ0-DQ34
Standby		H	H→X	X	X	X	X	High-Z
READ		L	L	H	L (NC)	ROW	COL	Data Out
EARLY-WRITE		L	L	L	X	ROW	COL	Data In
READ-WRITE		L	L	H→L	L→H	ROW	COL	Data Out
FAST-PAGE-MODE	1st Cycle	L	H→L	H	L (NC)	ROW	COL	Data Out
READ	2nd Cycle	L	H→L	H	L (NC)	n/a	COL	Data Out
FAST-PAGE-MODE	1st Cycle	L	H→L	L	X	ROW	COL	Data In
EARLY-WRITE	2nd Cycle	L	H→L	L	X	n/a	COL	Data In
FAST-PAGE-MODE	1st Cycle	L	H→L	H→L	L→H	ROW	COL	Data In
READ-WRITE	2nd Cycle	L	H→L	H→L	L→H	n/a	COL	Data In
RAS-ONLY REFRESH		L	X	X	X	ROW	n/a	High-Z
HIDDEN	READ	L→H→L	L	H	L (NC)	ROW	COL	Data Out
REFRESH	WRITE	L→H→L	L	L	X	ROW	COL	Data In
CAS-BEFORE-RAS REFRESH		H→L	L	H	X	X	X	High-Z
BATTERY BACKUP REFRESH		H→L	L	H	X	X	X	High-Z

PRESENCE DETECT TRUTH TABLE

CHARACTERISTICS						PRESENT DETECT PIN (PDx)							
Card Density	DRAM Organizations	Card Address	RAS Address	CAS Address	Page Depth	1	2	3	4	5	6	7	8
0MB	No card installed	X	X	X	X	NC	NC	NC	NC	NC	X	X	X
1MB	256K x 1, 4, 16, 18	18	9	9	512	Vss	Vss	Vss	Vss	NC	X	X	X
2MB	256K x 1, 4, 16, 18	18	9	9	512	Vss	Vss	Vss	Vss	Vss	X	X	X
2MB	512K x 8, 9	19	10	9	512	NC	Vss	Vss	Vss	NC	X	X	X
4MB	512K x 8, 9	19	10	9	512	NC	Vss	Vss	Vss	Vss	X	X	X
4MB	1 Meg x 1, 4, 16, 18	20	10	10	1,024	Vss	NC	Vss	Vss	NC	X	X	X
• 8MB	1 Meg x 1, 4, 16, 18	20	10	10	1,024	Vss	NC	Vss	Vss	Vss	X	X	X
8MB	2 Meg x 8, 9	21	11	10	1,024	NC	NC	Vss	Vss	NC	X	X	X
16MB	2 Meg x 8, 9	21	11	10	1,024	NC	NC	Vss	Vss	Vss	X	X	X
16MB	4 Meg x 1, 4, 16, 18	22	12	11	1,024	Vss	Vss	NC	Vss	NC	X	X	X
32MB	4 Meg x 1, 4, 16, 18	22	12	11	1,024	Vss	Vss	NC	Vss	Vss	X	X	X
Access Timing		100ns				X	X	X	X	X	Vss	Vss	X
		80ns				X	X	X	X	X	NC	Vss	X
		70ns				X	X	X	X	X	Vss	NC	X
		60ns				X	X	X	X	X	NC	NC	X
		50ns				X	X	X	X	X	Vss	Vss	X
Refresh Control		Standard				X	X	X	X	X	X	X	NC
		Auto				X	X	X	X	X	X	X	Vss

NOTE: Vss = Ground.

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} ..... -0.5V to +5.25V
Operating Temperature T_A (Ambient) ..... 0°C to 55°C
Storage Temperature ..... -20°C to +80°C
Power Dissipation 15W
Short Circuit Output Current 50mA
Card Insertions (Connector's Life Cycle) 10,000

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 3, 4, 6, 7) (0°C ≤ T_A ≤ 55°C; V_{CC} = 5V ±5%)

PARAMETER/CONDITION		SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage		V_{CC}	4.75	5.25	V	1
Input High (Logic 1) Voltage, All Inputs		V_{IH}	3.5	V_{CC}+0.5	V	1
Input Low (Logic 0) Voltage, All Inputs		V_{IL}	-0.5	0.8	V	1
INPUT LEAKAGE CURRENT, Any input	Non-buffered	I_{IN}	-12	12	µA	
(0V ≤ V_{IN} ≤ 5.25V; all other pins not under test = 0V)	Buffered	I_{IB}	-2	2	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled; 0V ≤ V_{OUT} ≤ 5.25V)		I_{OZ}	-10	10	µA	
OUTPUT LEVELS		V_{OH}	2.4		V	
Output High Voltage (I_{OUT} = -5mA) Output Low Voltage (I_{OUT} = 4.2mA)		V_{OL}		0.4	V	

		MAX				
PARAMETER/CONDITION	SYMBOL	-6	-7	-8	UNITS	NOTES
STANDBY CURRENT: (TTL) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC1}	32	32	32	mA	
STANDBY CURRENT: (CMOS) ($\overline{RAS}$ = $\overline{CAS}$ = Other Inputs = V_{CC} -0.2V)	I_{CC2}	3.2	3.2	3.2	mA	
OPERATING CURRENT: Random READ/WRITE Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC (MIN))	I_{CC3}	840	760	680	mA	3, 4, 30
OPERATING CURRENT: FAST PAGE MODE Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: ^tPC = ^tPC (MIN))	I_{CC4}	600	520	440	mA	3, 4, 30
REFRESH CURRENT: $\overline{RAS}$-ONLY Average power supply current ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}: ^tRC = ^tRC (MIN))	I_{CC5}	840	760	680	mA	3, 30
REFRESH CURRENT: $\overline{CAS}$-BEFORE-$\overline{RAS}$ (CBR) Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC (MIN))	I_{CC6}	840	760	680	mA	3, 5, 30
REFRESH CURRENT: BATTERY BACKUP (BBU) Average power supply current during BBU: $\overline{CAS}$ = 0.2V or CBR cycling; $\overline{RAS}$ = ^tRAS (MIN) up to 300ns; ^tRC = 125µs; $\overline{WE}$, A0-A9 and DQ = V_{CC} -0.2V or 0.2V (DQ may be left open)	I_{CC7}	4.8	4.8	4.8	mA	3, 5

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: $\overline{CAS0}$, $\overline{CAS1}$, $\overline{CAS2}$, $\overline{CAS3}$, A0-A9, $\overline{OE}$	C_{I1}		9	pF	2
Input Capacitance: $\overline{WE}$	C_{I2}		13	pF	2
Input Capacitance: $\overline{RAS0}$, $\overline{RAS1}$, $\overline{RAS2}$, $\overline{RAS3}$	C_{I3}		50	pF	2
Input/Output Capacitance: DQ	C_{IO}		20	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C ≤ T_A ≤ 55°C; V_{CC} = 5V ±5%)

AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	^tRC	110		130		150		ns	23
FAST-PAGE-MODE READ or WRITE cycle time	^tPC	40		40		45		ns	23
Access time from $\overline{RAS}$	^tRAC		60		70		80	ns	14, 23
Access time from $\overline{CAS}$	^tCAC		25		30		30	ns	15, 26
Access time from column address	^tAA		40		45		50	ns	26
Access time from $\overline{CAS}$ precharge	^tCPA		50		50		55	ns	26
$\overline{RAS}$ pulse width	^tRAS	60	100,000	70	100,000	80	100,000	ns	23
$\overline{RAS}$ pulse width (FAST PAGE MODE)	^tRASP	60	100,000	70	100,000	80	100,000	ns	23
$\overline{RAS}$ hold time	^tRSH	25		30		30		ns	26
$\overline{RAS}$ precharge time	^tRP	45		50		60		ns	23
$\overline{CAS}$ pulse width	^tCAS	15	100,000	20	100,000	20	100,000	ns	23
$\overline{CAS}$ hold time	^tCSH	55		65		75		ns	25
$\overline{CAS}$ precharge time	^tCPN	10		10		10		ns	16, 23
$\overline{CAS}$ precharge time (FAST PAGE MODE)	^tCP	10		10		10		ns	23
$\overline{RAS}$ to $\overline{CAS}$ delay time	^tRCD	10	35	15	40	15	50	ns	17, 28
$\overline{CAS}$ to $\overline{RAS}$ precharge time	^tCRP	15		15		15		ns	26
Row address setup time	^tASR	10		10		10		ns	26
Row address hold time	^tRAH	5		5		5		ns	25
$\overline{RAS}$ to column address delay time	^tRAD	10	20	10	25	10	30	ns	18, 28
Column address setup time	^tASC	5		5		5		ns	24
Column address hold time	^tCAH	15		20		20		ns	24
Column address hold time (referenced to $\overline{RAS}$)	^tAR	45		50		55		ns	25
Column address to $\overline{RAS}$ lead time	^tRAL	40		45		50		ns	26
Read command setup time	^tRCS	5		5		5		ns	25
Read command hold time (referenced to $\overline{CAS}$)	^tRCH	5		5		5		ns	19, 24
Read command hold time (referenced to $\overline{RAS}$)	^tRRH	-5		-5		-5		ns	19, 25
$\overline{CAS}$ to output in Low-Z	^tCLZ	5		5		5		ns	24
Output buffer turn-off delay	^tOFF	5	30	5	30	5	30	ns	20, 29, 35
$\overline{WE}$ command setup time	^tWCS	5		5		5		ns	24

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C ≤ T_A ≤ 55°C; Vcc = 5V ±5%)

AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Write command hold time	tWCH	15		20		20		ns	24
Write command hold time (referenced to $\overline{RAS}$)	tWCR	40		50		55		ns	25
Write command pulse width	tWP	10		15		15		ns	23
Write command to $\overline{RAS}$ lead time	tRWL	25		30		30		ns	26
Write command to $\overline{CAS}$ lead time	tCWL	20		25		25		ns	24
Data-in setup time	tDS	5		5		5		ns	24, 32
Data-in hold time	tDH	5		10		10		ns	25, 32
Data-in hold time (referenced to $\overline{RAS}$)	tDHR	45		55		60		ns	23
Transition time (rise or fall)	tT	2	15	2	15	2	15	ns	9, 10, 23
Refresh period (1,024 cycles)	tREF		128		128		128	ms	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	tRPC	10		10		10		ns	26
$\overline{CAS}$ setup time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	tCSR	20		20		20		ns	5, 26
$\overline{CAS}$ hold time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	tCHR	10		10		10		ns	5, 25
$\overline{WE}$ hold time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	tWRH	5		5		5		ns	22, 25
$\overline{WE}$ setup time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	tWRP	20		20		20		ns	22, 26
$\overline{WE}$ hold time (WCBR test cycle)	tWTH	5		5		5		ns	22, 25
$\overline{WE}$ setup time	tWTS	20		20		20		ns	22, 26
READ-WRITE cycle time	tRWC	165		185		205		ns	
FAST-PAGE-MODE READ-WRITE cycle time	tPRWC	90		95		100		ns	23
$\overline{RAS}$ to $\overline{WE}$ delay time	tRWD	80		90		100		ns	31, 27
Column Address to $\overline{WE}$ delay time	tAWD	65		70		75		ns	31, 24
$\overline{CAS}$ to $\overline{WE}$ delay time	tCWD	50		65		55		ns	31, 24
Output buffer turn-off delay	tOE		25		30		30	ns	20, 33, 26
Output disable	tOD		25		30		30	ns	35, 26
$\overline{OE}$ hold time from $\overline{WE}$ during READ-MODIFY-WRITE cycle	tOEH	5		10		10		ns	34, 27
$\overline{OE}$ hold time from $\overline{RAS}$ during HIDDEN REFRESH cycle	tORD	10		10		10		ns	21, 26

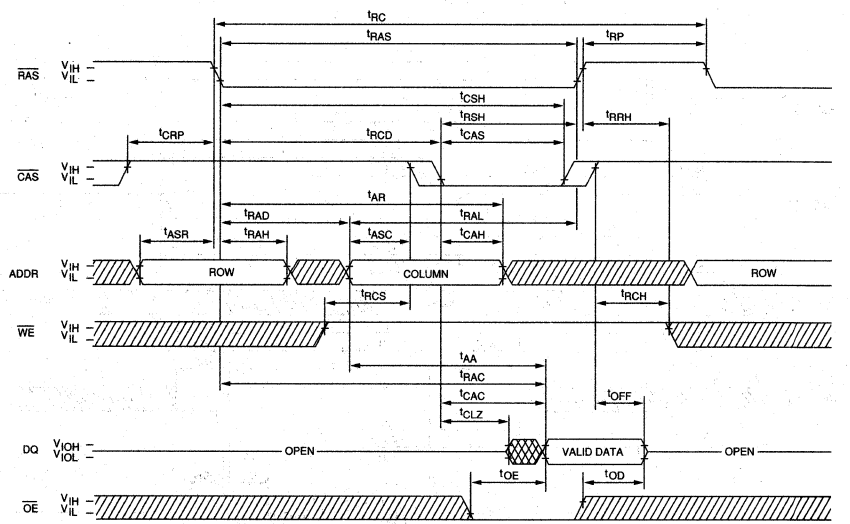
NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. V_{CC} = 5V ±10%, f = 1 MHz.
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is assured.
7. An initial pause of 100µs is required after power-up followed by eight $\overline{RAS}$ refresh cycles ($\overline{RAS}$-ONLY or CBR with $\overline{WE}$ HIGH) before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-up should be repeated any time the ^tREF refresh requirement is exceeded.
8. AC characteristics assume ^tT = 5ns.
9. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS}$ = V_{IH}, data output is High-Z.
12. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to 2 TTL gates and 100pF.
14. Assumes that $^tRCD < ^tRCD$ (MAX). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
15. Assumes that $^tRCD \geq ^tRCD$ (MAX).
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer, $\overline{CAS}$ must be pulsed HIGH for ^tCPN.
17. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (MAX) limit, then access time is controlled exclusively by ^tCAC.
18. Operation within the ^tRAD (MAX) limit ensures that ^tRCD (MAX) can be met. ^tRAD (MAX) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (MAX) limit, then access time is controlled exclusively by ^tAA.
19. Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
20. ^tOFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
21. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW.
22. ^tWTS and ^tWTH are setup and hold specifications for the $\overline{WE}$ pin being held LOW to enable the JEDEC test mode (with CBR timing constraints). These two parameters are the inverse of ^tWRP and ^tWRH in the CBR refresh cycle.
23. Timing between the DRAMs and the DRAM card did not change with the addition of the line drivers.
24. A +5ns timing skew from the DRAM to the DRAM card resulted from the addition of line drivers.
25. A -5ns timing skew from the DRAM to the DRAM card resulted from the addition of line drivers.
26. A +10ns timing skew from the DRAM to the DRAM card resulted from the addition of line drivers.
27. A -10ns timing skew from the DRAM to the DRAM card resulted from the addition of line drivers.
28. A -5ns (MIN) and a -10ns (MAX) timing skew from the DRAM to the DRAM card resulted from the addition of line drivers.
29. A +5ns (MIN) and a +10ns (MAX) timing skew from the DRAM to the DRAM card resulted from the addition of line drivers.
30. The maximum current ratings are based on one of the two banks operating or being refreshed (x32 mode). The stated maximums may be reduced by one half when used in the x16 mode. Standby currents of the non-active bank are not included.
31. ^tWCS, ^tRWD, ^tAWD and ^tCWD are restrictive operating parameters in late WRITE, and READ-MODIFY-WRITE cycles only. If $^tWCS \geq ^tWCS$ (MIN), the cycle is an EARLY-WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If $^tRWD \geq ^tRWD$ (MIN), $^tAWD \geq ^tAWD$ (MIN) and $^tCWD \geq ^tCWD$ (MIN), the cycle is a READ-MODIFY-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of data out is indeterminate. $\overline{OE}$ held HIGH and $\overline{WE}$ taken LOW after $\overline{CAS}$ goes LOW results in a LATE-WRITE ($\overline{OE}$ controlled) cycle.

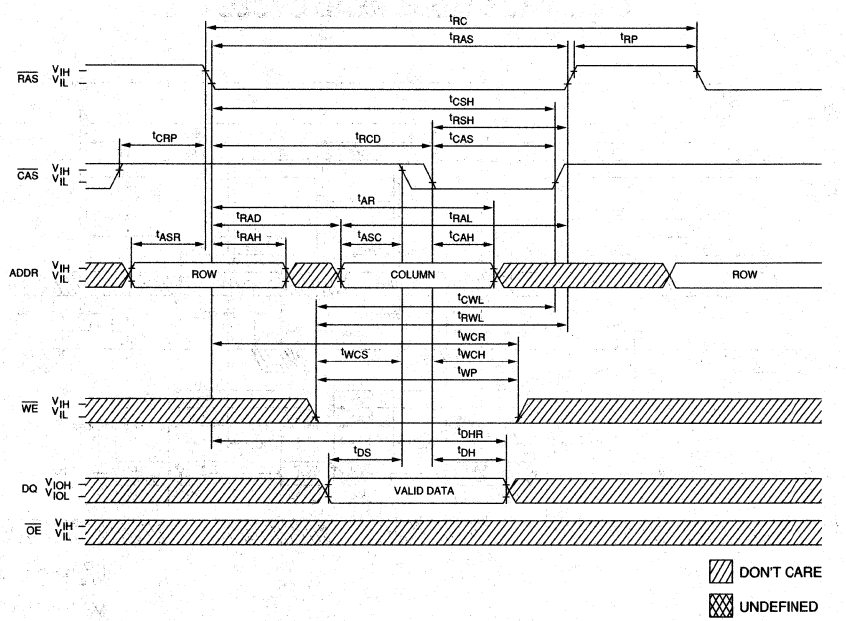
NOTES (continued)

32. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY-WRITE cycles and $\overline{WE}$ leading edge in LATE-WRITE or READ-MODIFY-WRITE cycles.
33. If $\overline{OE}$ is tied permanently LOW, LATE-WRITE or READ-MODIFY-WRITE operations are not possible.
34. LATE-WRITE and READ-MODIFY-WRITE cycles must have both ^{t}OD and ^{t}OEH met ($\overline{OE}$ HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. The DQs will provide the previously read data if $\overline{CAS}$ remains LOW and $\overline{OE}$ is taken back LOW after ^{t}OEH is met. If $\overline{CAS}$ goes HIGH prior to $\overline{OE}$ going back LOW, the DQs will remain open.
35. The DQs open during READ cycles once ^{t}OD or ^{t}OFF occur. If $\overline{CAS}$ goes HIGH first, $\overline{OE}$ becomes a "don't care." If $\overline{OE}$ goes HIGH and $\overline{CAS}$ stays LOW, $\overline{OE}$ is not a "don't care;" and the DQs will provide the previously read data if $\overline{OE}$ is taken back LOW (while $\overline{CAS}$ remains LOW).

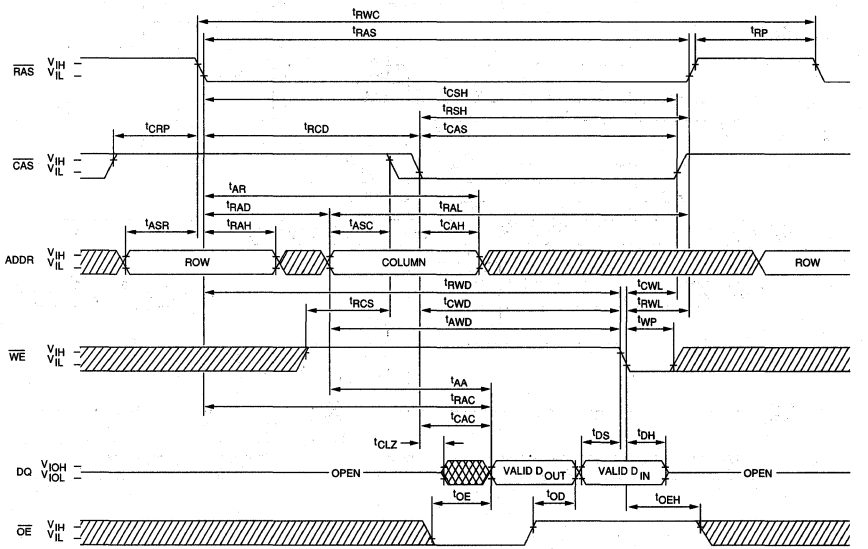
READ CYCLE



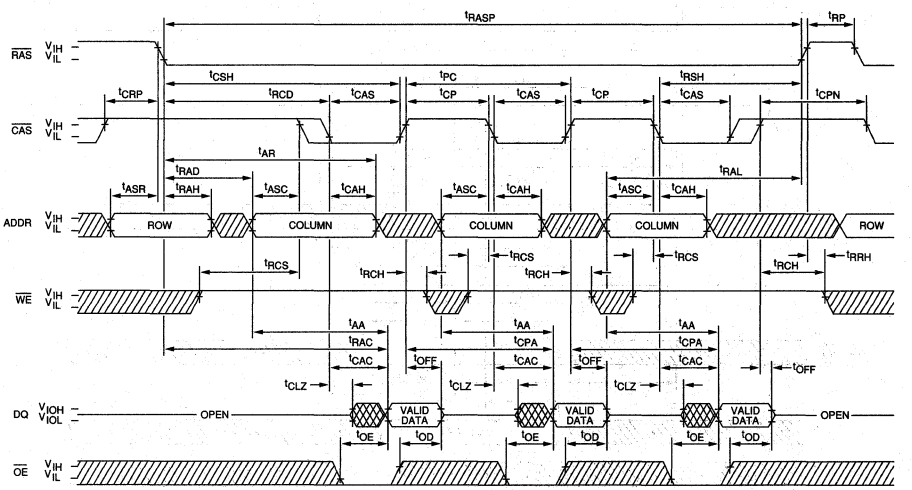
EARLY-WRITE CYCLE



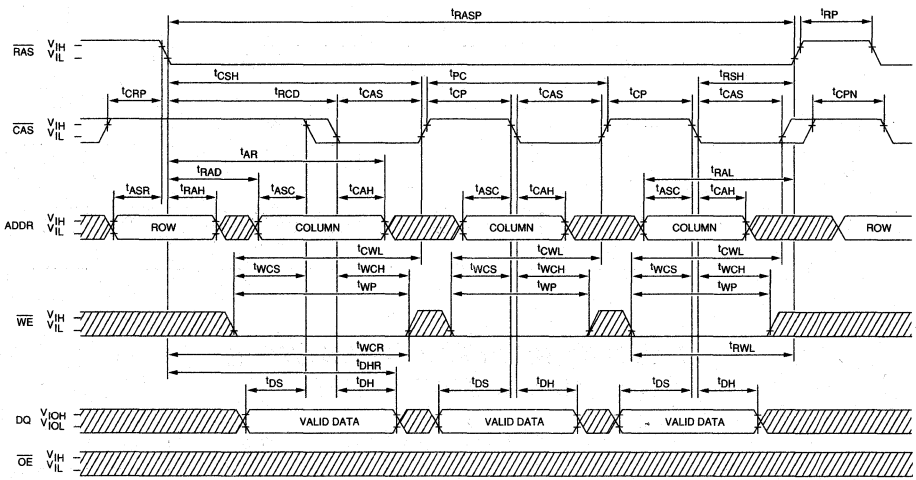
READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)



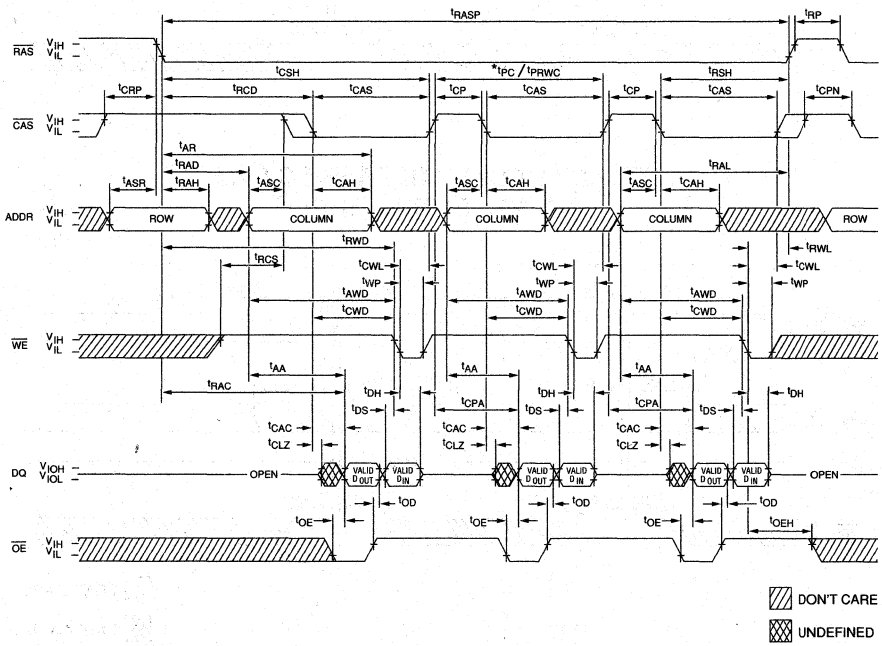
FAST-PAGE-MODE READ CYCLE



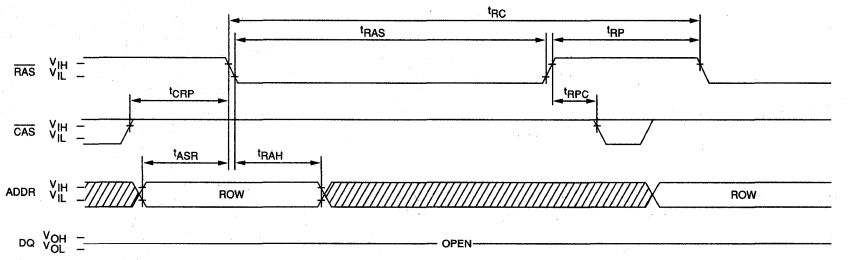
FAST-PAGE-MODE EARLY-WRITE CYCLE



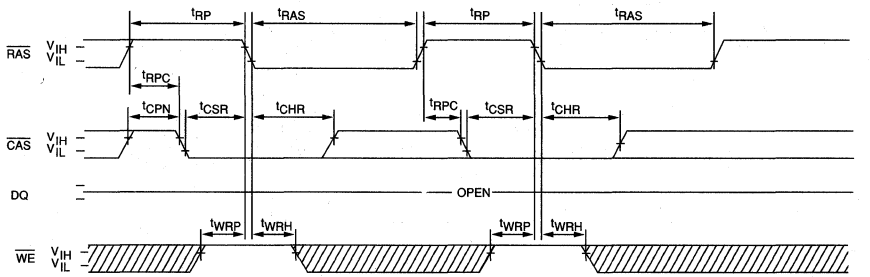
FAST-PAGE-MODE READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)



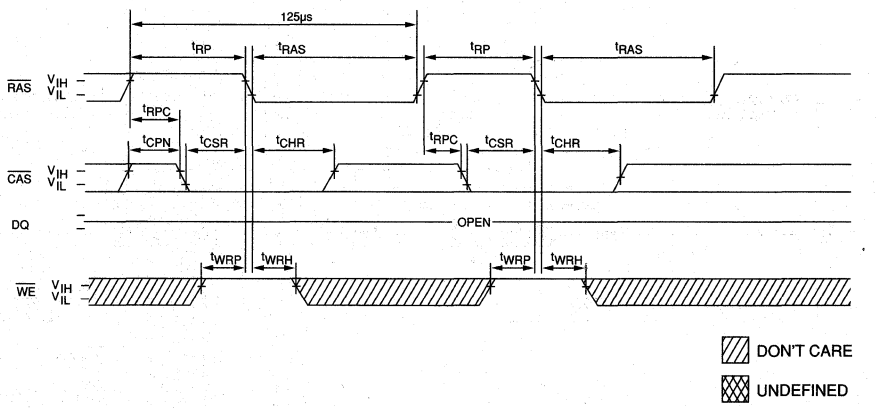
$\overline{\text{RAS}}$-ONLY REFRESH CYCLE
(ADDR = A0-A9; $\overline{\text{WE}}$ = DON'T CARE)



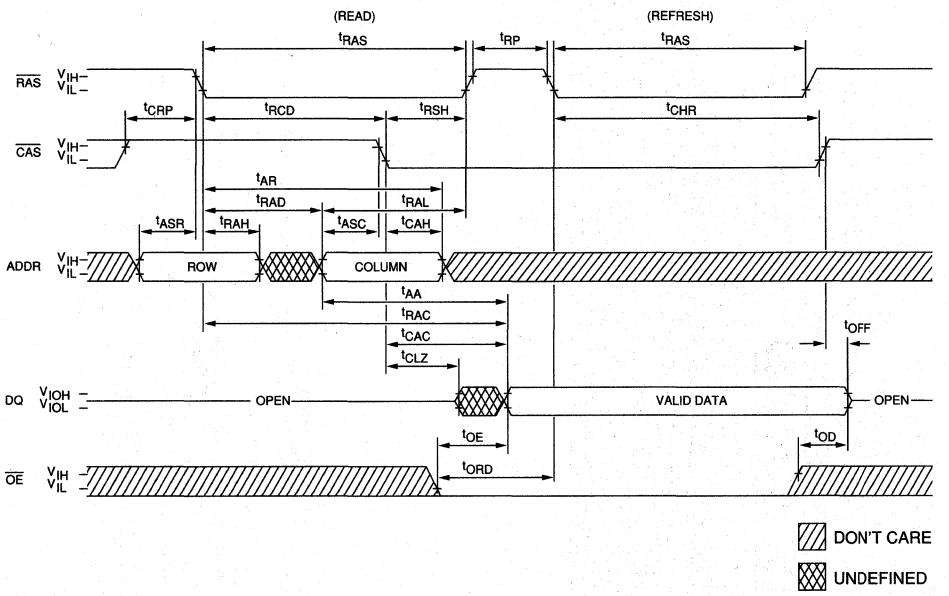
$\overline{\text{CAS}}$-BEFORE-$\overline{\text{RAS}}$ REFRESH CYCLE
(A0-A9 = DON'T CARE)



BATTERY BACKUP REFRESH CYCLE
(A0-A9 = DON'T CARE)



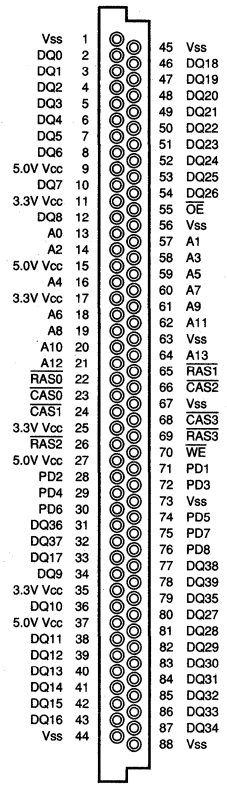
HIDDEN REFRESH CYCLE [21]
($\overline{WE}$ = HIGH)



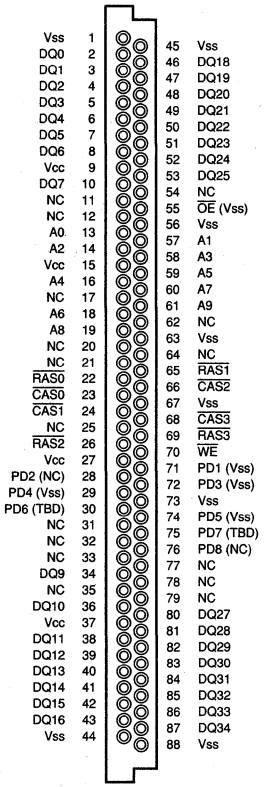
NEW IC DRAM CARD

NEW ■ IC DRAM CARD

RESERVED JEDEC, JEIDA and PCMCIA 88-PIN ASSIGNMENT
(All Possible Combinations)



MT16D88C232 PIN ASSIGNMENT
(JEDEC Standard)



IC DRAM CARD 1 MEGABYTE

256K x 36, 512K x 18

FEATURES

- JEIDA, JEDEC and PCMCIA standard 88-pin IC DRAM card
- Polarized receptacle connector
- Industry standard DRAM functions and timing
- High-performance, CMOS silicon-gate process
- All outputs are fully TTL compatible
- All inputs buffered except $\overline{RAS}$ inputs
- Multiple $\overline{RAS}$ inputs for x18 or x36 selectability
- Refresh modes: $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$ (CBR), HIDDEN and BATTERY BACKUP (BBU)
- FAST PAGE MODE access cycle
- Single +5V ±5% power supply
- Low power; 12mW standby, 2.7W active (typical)
- Extended refresh standard: 512 cycles every 64ms

OPTIONS MARKING

- Timing

60ns access	-6
70ns access	-7
80ns access	-8

GENERAL DESCRIPTION

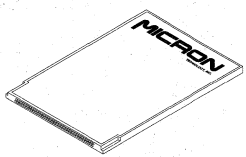
The MT12D88C25636 is a 1 megabyte, IC DRAM card organized as a 256K x 36 bit memory array. It may also be configured as a 512K x 18 bit memory array, provided the corresponding DQs on the host system are made common and memory bank control procedures are implemented. Separate $\overline{CAS}$ inputs allow byte accesses.

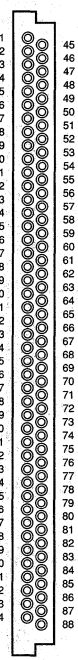
All inputs to the DRAMs are buffered, with the exception of $\overline{RAS}$. The line drivers used for buffers reduce reflections on the card and ensure compatibility in a wide range of systems. At the same time, the line drivers add delays to the buffered input timings when compared to standard DRAMs.

The MT12D88C25636 is designed for low power operation using 256K x 4 low power, extended refresh DRAMs. These devices support BATTERY BACKUP (BBU) cycle refresh; a very low current, data retention mode. Standard component DRAM refresh modes are supported as well.

Multiple $\overline{RAS}$ inputs conserve power by allowing individual bank selection. In the x36 organization, the memory is a single array that may be divided into four separate bytes. In the x18 organization, up to two banks, each with two separate bytes, may be independently selected. One bank is activated by each $\overline{RAS}$ selection; the others not selected remain in standby mode, drawing minimum power.

PIN ASSIGNMENT (End View)
88-Pin Card (U-1)





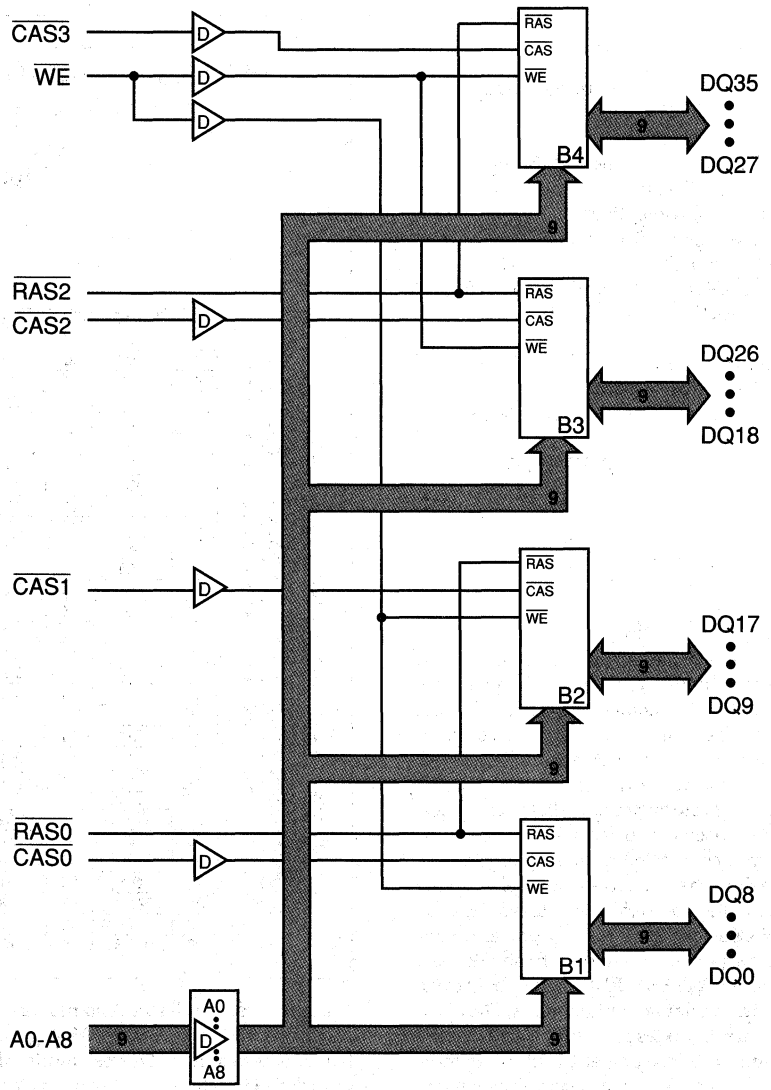
PIN #	SYMBOL	PIN #	SYMBOL	PIN #	SYMBOL
1	Vss	31	NC	61	NC
2	DQ0	32	NC	62	NC
3	DQ1	33	DQ17	63	Vss
4	DQ2	34	DQ9	64	NC
5	DQ3	35	NC	65	NC
6	DQ4	36	DQ10	66	$\overline{CAS2}$
7	DQ5	37	Vcc	67	Vss
8	DQ6	38	DQ11	68	$\overline{CAS3}$
9	Vcc	39	DQ12	69	NC
10	DQ7	40	DQ13	70	$\overline{WE}$
11	NC	41	DQ14	71	PD1 (Vss)
12	DQ8	42	DQ15	72	PD3 (Vss)
13	A0	43	DQ16	73	Vss
14	A2	44	Vss	74	PD5 (NC)
15	Vcc	45	Vss	75	PD7 (TBD)
16	A4	46	DQ18	76	PD8 (NC)
17	NC	47	DQ19	77	NC
18	A6	48	DQ20	78	NC
19	A8	49	DQ21	79	DQ35
20	NC	50	DQ22	80	DQ27
21	NC	51	DQ23	81	DQ28
22	$\overline{RAS0}$	52	DQ24	82	DQ29
23	$\overline{CAS0}$	53	DQ25	83	DQ30
24	$\overline{CAS1}$	54	DQ26	84	DQ31
25	NC	55	NC	85	DQ32
26	$\overline{RAS2}$	56	Vss	86	DQ33
27	Vcc	57	A1	87	DQ34
28	PD2 (Vss)	58	A3	88	Vss
29	PD4 (Vss)	59	A5		
30	PD6 (TBD)	60	A7		

Eight presence detect pins may be read by the host to identify the MT12D88C25636 organization, number of banks, access time and refresh mode. These extensive presence detect functions allow systems to utilize the advanced power-saving features.

The MT12D88C25636 is built with a plastic frame covered by stainless steel panels. This package, containing an 88-pin receptacle connector, is keyed to prevent improper installation or insertion into other types of IC card sockets.

NEW ■ IC DRAM CARD

FUNCTIONAL BLOCK DIAGRAM



NOTE: 1. D = 74AC11244 line drivers.
2. B1 through B4 = 256K x 9 memory blocks.

PIN DESCRIPTIONS

PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
22, 26	$\overline{RAS0}$, $\overline{RAS2}$	Input	Row Address Strobe: $\overline{RAS}$ is used to clock-in the 9 row-address bits. Two $\overline{RAS}$ inputs allow for a single x36 bank or two x18 banks.
23, 24, 66, 68	$\overline{CAS}$0-3	Input	Column Address Strobe: $\overline{CAS}$ is used to clock-in the 9 column-address bits, enable the DRAM output buffers, and strobe the data inputs on WRITE cycles. Four $\overline{CAS}$ inputs allow byte access control for any memory bank configuration.
70	$\overline{WE}$	Input	Write Enable: $\overline{WE}$ is the READ/WRITE control for the DQ pins. If $\overline{WE}$ is LOW prior to $\overline{CAS}$ going LOW, the access is a WRITE cycle. If $\overline{WE}$ is HIGH while $\overline{CAS}$ is LOW, the access is a READ cycle.
13, 57, 14, 58, 16, 59, 18, 60, 19	A0-A8	Input	Address Inputs: These inputs are multiplexed and clocked by $\overline{RAS}$ and $\overline{CAS}$.
2-8, 10, 12, 34, 36, 38-43, 33, 46-54, 80-87, 79	DQ0-DQ35	Input/ Output	Data I/O: For WRITE cycles, DQ0-DQ35 act as inputs to the addressed DRAM location. BYTE WRITEs may be performed by using the corresponding $\overline{CAS}$ select. For READ access cycles, DQ0-DQ35 act as outputs for the addressed DRAM location.
71, 28, 72, 29, 74, 30, 75, 76	PD1-PD8	-	Presence Detect: These pins are read by the host system and tell the system the card's personality. They will be either left floating (NC) or they will be grounded (Vss).
11, 17, 20, 21, 25, 31, 32, 35, 61, 62, 55, 64, 65, 69, 77, 78	NC	-	No Connect: These pins should be left unconnected (reserved for future use).
9, 15, 27, 37	Vcc	Supply	Power Supply: +5V ±5%
1, 44, 45, 56, 63, 67, 73, 88	Vss	Supply	Ground

FUNCTIONAL DESCRIPTION

The MT12D88C25636 is a 1 megabyte memory card structured as a 256K x 36 bit memory array ($\overline{RAS0}$ = $\overline{RAS2}$). It also may be configured as a 512K x 18 bit memory array provided the corresponding DQs on the host are connected and memory bank control procedures are implemented by interleaving both $\overline{RAS}$ lines.

Most x36 bit applications use the same signal to control the $\overline{CAS}$ inputs. $\overline{RAS0}$ controls the lower 18 bits, and $\overline{RAS2}$ controls the upper 18 bits to obtain a x36 memory array. For x18 applications, the corresponding DQs and the corresponding $\overline{CAS}$ pins must be connected together (DQ0 to DQ18, DQ1 to DQ19 and so forth, and $\overline{CAS0}$ to $\overline{CAS2}$ and $\overline{CAS1}$ to $\overline{CAS3}$). Each $\overline{RAS}$ is then a bank select for the 512K x 18 memory organization.

DRAM OPERATION

DRAM REFRESH

Memory cell data is retained in its correct state by maintaining power and executing any $\overline{RAS}$ cycle [READ, WRITE, $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$ (CBR), HIDDEN or BATTERY BACKUP (BBU) REFRESH] so that all 512 combinations of $\overline{RAS}$ addresses (A0-A8) are executed at least every 64ms, regardless of sequence.

The implied method of choice for refreshing the memory card is the BBU cycle. This is a very low current, data retention mode made possible by using the CBR REFRESH cycle over the extended refresh range (I_{CC7}).

The memory card may be used with the other refresh modes common in standard DRAMs. This allows the memory card to be used on existing systems that do not utilize the BBU REFRESH cycle. However, the memory card will draw more current in the STANDBY mode. The CBR REFRESH mode is recommended when not using the BBU mode.

DRAM READ AND WRITE CYCLES

During READ or WRITE cycles, each bit is uniquely addressed through the 18 address bits, which are entered 9 bits (A0-A8) at a time. $\overline{RAS}$ is used to latch the first 9 bits and $\overline{CAS}$ the latter 9 bits. READ or WRITE cycles are selected with the $\overline{WE}$ input. A logic HIGH on $\overline{WE}$ dictates READ mode while a logic LOW on $\overline{WE}$ dictates WRITE mode. During a WRITE cycle, data in (D) is latched by the falling edge of $\overline{CAS}$. $\overline{WE}$ must fall prior to $\overline{CAS}$ (EARLY WRITE); if $\overline{WE}$ goes LOW after $\overline{CAS}$, the outputs (Q) will be activated and will drive invalid data to the inputs. The data inputs and data outputs are routed through pins using common I/O, and pin direction is controlled by $\overline{WE}$.

FAST PAGE MODE operation allows faster data operations (READ or WRITE) within a row address (A0-A8) defined page boundary. The FAST PAGE MODE cycle is always initiated with a row address strobed-in by $\overline{RAS}$ followed by a column address strobed-in by $\overline{CAS}$. $\overline{CAS}$ may be toggled-in by holding $\overline{RAS}$ LOW and strobing-in different column addresses, thus executing faster memory cycles. Returning $\overline{RAS}$ HIGH terminates the FAST PAGE MODE operation. Returning $\overline{RAS}$ and $\overline{CAS}$ HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the $\overline{RAS}$ high time.

DRAM TIMING

In accordance with JEDEC standard specifications, all inputs to the IC DRAM card are buffered, with the exception of $\overline{RAS}$ inputs. The line drivers used for buffers reduce reflections on the card and ensure compatibility in a wide range of systems. The implementation of buffers on the card may relieve the need for additional host system line drivers. Notes 23 though 29 indicate which parameters on the IC DRAM card are affected by the line drivers, and to what magnitude they are affected. The component DRAM timing specifications, rather than those of the IC DRAM card (in systems that use both), may cause timing incompatibilities.

All traces on the IC DRAM card (buffered and non-buffered) are approximately 50 ohms characteristic impedance. Matching impedance on the system board to 50 ohms characteristic impedance on traces to the IC DRAM card will decrease signal noise to the IC DRAM card, enhancing overall system reliability.

PHYSICAL DESIGN

The MT12D88C25636 is constructed with a molded plastic frame and covered with stainless steel panels. Inside, 12 thin small-outline package (TSOP) DRAMs are mounted an ultrathin printed circuit board. The board is attached to a high insertion, 88-pin receptacle connector. The package has a polarized key to prevent improper installation, including insertion into other types of IC card sockets. The MT12D88C25636 operates reliably up to 55°C.

MEMORY TRUTH TABLE

FUNCTION		RAS	CAS	WE	ADDRESSES		DATA IN/OUT
					^tR	^tC	DQ0-DQ35
Standby		H	H→X	X	X	X	High-Z
READ		L	L	H	ROW	COL	Data Out
EARLY-WRITE		L	L	L	ROW	COL	Data In
READ-WRITE		L	L	H→L	ROW	COL	Data In
FAST-PAGE-MODE	1st Cycle	L	H→L	H	ROW	COL	Data Out
READ	2nd Cycle	L	H→L	H	n/a	COL	Data Out
FAST-PAGE-MODE	1st Cycle	L	H→L	L	ROW	COL	High-Z
EARLY-WRITE	2nd Cycle	L	H→L	L	n/a	COL	High-Z
FAST-PAGE-MODE	1st Cycle	L	H→L	H→L	ROW	COL	Data Out
READ-WRITE	2nd Cycle	L	H→L	H→L	n/a	COL	Data Out
RAS-ONLY REFRESH		H	X	X	ROW	n/a	High-Z
HIDDEN	READ	L→H→L	L	H	ROW	COL	Data Out
REFRESH	WRITE	L→H→L	L	L	ROW	COL	Data In
CAS-BEFORE-RAS REFRESH		H→L	L	H	X	X	High-Z
BATTERY BACKUP REFRESH		H→L	L	H	X	X	High-Z

PRESENCE DETECT TRUTH TABLE

CHARACTERISTICS						PRESENT DETECT PIN (PDx)							
Card Density	DRAM Organizations	Card Address	RAS Address	CAS Address	Page Depth	1	2	3	4	5	6	7	8
0MB	No card installed	X	X	X	X	NC	NC	NC	NC	NC	X	X	X
• 1MB	256K x 1, 4, 16, 18	18	9	9	512	Vss	Vss	Vss	Vss	NC	X	X	X
2MB	256K x 1, 4, 16, 18	18	9	9	512	Vss	Vss	Vss	Vss	Vss	X	X	X
2MB	512K x 8, 9	19	10	9	512	NC	Vss	Vss	Vss	NC	X	X	X
4MB	512K x 8, 9	19	10	9	512	NC	Vss	Vss	Vss	Vss	X	X	X
4MB	1 Meg x 1, 4, 16, 18	20	10	10	1,024	Vss	NC	Vss	Vss	NC	X	X	X
8MB	1 Meg x 1, 4, 16, 18	20	10	10	1,024	Vss	NC	Vss	Vss	Vss	X	X	X
8MB	2 Meg x 8, 9	21	11	10	1,024	NC	NC	Vss	Vss	NC	X	X	X
16MB	2 Meg x 8, 9	21	11	10	1,024	NC	NC	Vss	Vss	Vss	X	X	X
16MB	4 Meg x 1, 4, 16, 18	22	12	11	1,024	Vss	Vss	NC	Vss	NC	X	X	X
32MB	4 Meg x 1, 4, 16, 18	22	12	11	1,024	Vss	Vss	NC	Vss	Vss	X	X	X
Access Timing		100ns				X	X	X	X	X	Vss	Vss	X
		80ns				X	X	X	X	X	NC	Vss	X
		70ns				X	X	X	X	X	Vss	NC	X
		60ns				X	X	X	X	X	NC	NC	X
		50ns				X	X	X	X	X	Vss	Vss	X
Refresh Control		Standard				X	X	X	X	X	X	X	NC
		Auto				X	X	X	X	X	X	X	Vss

NOTE: Vss = Ground.

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} ..... -0.5V to +5.25V
Operating Temperature T_A (Ambient) ..... 0°C to 55°C
Storage Temperature ..... -20°C to +80°C
Power Dissipation 15W
Short Circuit Output Current 50mA
Card Insertions (Connector's Life Cycle) 10,000

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 3, 4, 6, 7) (0°C ≤ T_A ≤ 55°C; V_{CC} = 5V ±5%)

PARAMETER/CONDITION		SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage		V_{CC}	4.75	5.25	V	1
Input High (Logic 1) Voltage, All Inputs		V_{IH}	3.5	V_{CC}+0.5	V	1
Input Low (Logic 0) Voltage, All Inputs		V_{IL}	-0.5	0.8	V	1
INPUT LEAKAGE CURRENT, Any input	Non-buffered	I_{IN}	-12	12	µA	
(0V ≤ V_{IN} ≤ 5.25V; all other pins not under test = 0V)	Buffered	I_{IB}	-2	2	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled; 0V ≤ V_{OUT} ≤ 5.25V)		I_{OZ}	-10	10	µA	
OUTPUT LEVELS		V_{OH}	2.4		V	
Output High Voltage (I_{OUT} = -5mA)						
Output Low Voltage (I_{OUT} = 4.2mA)		V_{OL}		0.4	V	

		MAX				
PARAMETER/CONDITION	SYMBOL	-6	-7	-8	UNITS	NOTES
STANDBY CURRENT: (TTL) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC1}	24	24	24	mA	
STANDBY CURRENT: (CMOS) ($\overline{RAS}$ = $\overline{CAS}$ = Other Inputs = V_{CC} -0.2V)	I_{CC2}	2.4	2.4	2.4	mA	
OPERATING CURRENT: Random READ/WRITE Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC (MIN))	I_{CC3}	1.0	0.9	0.8	A	3, 4, 30
OPERATING CURRENT: FAST PAGE MODE Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: ^tPC = ^tPC (MIN))	I_{CC4}	780	660	540	mA	3, 4, 30
REFRESH CURRENT: $\overline{RAS}$-ONLY Average power supply current ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}: ^tRC = ^tRC (MIN))	I_{CC5}	1.0	0.9	0.8	A	3, 30
REFRESH CURRENT: $\overline{CAS}$-BEFORE-$\overline{RAS}$ (CBR) Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC (MIN))	I_{CC6}	1.0	0.9	0.8	A	3, 5, 30
REFRESH CURRENT: BATTERY BACKUP (BBU) Average power supply current during BBU: $\overline{CAS}$ = 0.2V or CBR cycling; $\overline{RAS}$ = ^tRAS (MIN) up to 300ns; ^tRC = 125µs; $\overline{WE}$, A0-A8 and DQ = V_{CC} -0.2V or 0.2V (DQ may be left open)	I_{CC7}	2.4	2.4	2.4	mA	3, 5

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: $\overline{CAS0}$, $\overline{CAS1}$, $\overline{CAS2}$, $\overline{CAS3}$, A0-A8	C_{I1}		9	pF	2
Input Capacitance: $\overline{WE}$	C_{I2}		13	pF	2
Input Capacitance: $\overline{RAS0}$, $\overline{RAS2}$	C_{I3}		50	pF	2
Input/Output Capacitance: DQ	C_{IO}		12	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C ≤ T_A ≤ 55°C; Vcc = 5V ±5%)

AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	^tRC	110		130		150		ns	23
FAST-PAGE-MODE READ or WRITE cycle time	^tPC	40		40		45		ns	23
Access time from $\overline{RAS}$	^tRAC		60		70		80	ns	14, 23
Access time from $\overline{CAS}$	^tCAC		25		30		30	ns	15, 26
Access time from column address	^tAA		40		45		50	ns	26
Access time from $\overline{CAS}$ precharge	^tCPA		50		50		55	ns	26
$\overline{RAS}$ pulse width	^tRAS	60	100,000	70	100,000	80	100,000	ns	23
$\overline{RAS}$ pulse width (FAST PAGE MODE)	^tRASP	60	100,000	70	100,000	80	100,000	ns	23
$\overline{RAS}$ hold time	^tRSH	25		30		30		ns	26
$\overline{RAS}$ precharge time	^tRP	40		50		60		ns	23
$\overline{CAS}$ pulse width	^tCAS	15	100,000	20	100,000	20	100,000	ns	23
$\overline{CAS}$ hold time	^tCSH	55		65		75		ns	25
$\overline{CAS}$ precharge time	^tCPN	10		10		10		ns	16, 23
$\overline{CAS}$ precharge time (FAST PAGE MODE)	^tCP	10		10		10		ns	23
$\overline{RAS}$ to $\overline{CAS}$ delay time	^tRCD	10	35	15	40	15	50	ns	17, 28
$\overline{CAS}$ to $\overline{RAS}$ precharge time	^tCRP	15		15		15		ns	26
Row address setup time	^tASR	10		10		10		ns	26
Row address hold time	^tRAH	5		5		5		ns	25
$\overline{RAS}$ to column address delay time	^tRAD	10	20	10	25	10	30	ns	18, 28
Column address setup time	^tASC	5		5		5		ns	24
Column address hold time	^tCAH	15		20		20		ns	24
Column address hold time (referenced to $\overline{RAS}$)	^tAR	45		50		55		ns	25
Column address to $\overline{RAS}$ lead time	^tRAL	40		45		50		ns	26
Read command setup time	^tRCS	5		5		5		ns	25
Read command hold time (referenced to $\overline{CAS}$)	^tRCH	5		5		5		ns	19, 24
Read command hold time (referenced to $\overline{RAS}$)	^tRRH	-5		-5		-5		ns	19, 25
$\overline{CAS}$ to output in Low-Z	^tCLZ	5		5		5		ns	24
Output buffer turn-off delay	^tOFF	5	30	5	30	5	30	ns	20, 29
$\overline{WE}$ command setup time	^tWCS	5		5		5		ns	24

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

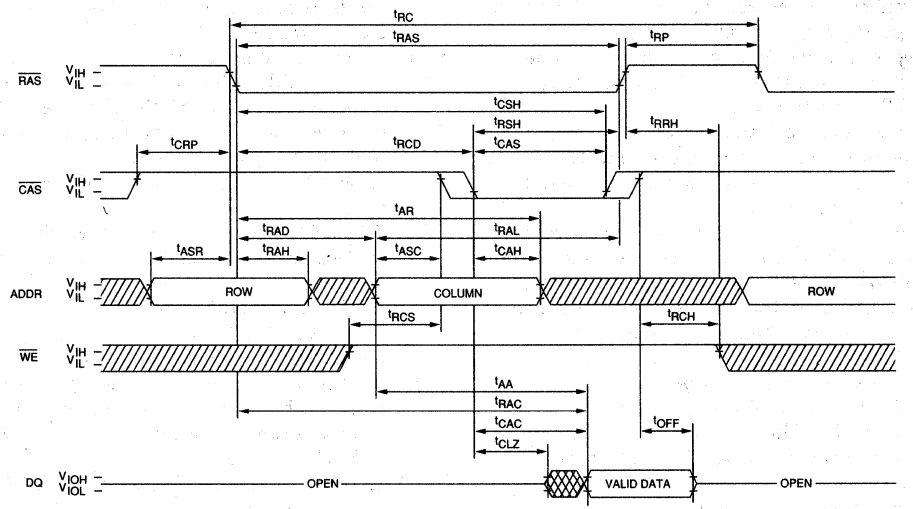
(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C ≤ T_A ≤ 55°C; Vcc = 5V ±5%)

AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Write command hold time	^tWCH	15		20		20		ns	24
Write command hold time (referenced to $\overline{RAS}$)	^tWCR	40		50		55		ns	25
Write command pulse width	^tWP	10		15		15		ns	23
Write command to $\overline{RAS}$ lead time	^tRWL	25		30		30		ns	26
Write command to $\overline{CAS}$ lead time	^tCWL	20		25		25		ns	24
Data-in setup time	^tDS	5		5		5		ns	24
Data-in hold time	^tDH	5		10		10		ns	25
Data-in hold time (referenced to $\overline{RAS}$)	^tDHR	45		55		60		ns	23
Transition time (rise or fall)	^tT	2	15	2	15	2	15	ns	9, 10, 23
Refresh period (1,024 cycles)	^tREF		64		64		64	ms	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	^tRPC	10		10		10		ns	26
$\overline{CAS}$ setup time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tCSR	20		20		20		ns	5, 26
$\overline{CAS}$ hold time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tCHR	10		10		10		ns	5, 25
$\overline{WE}$ hold time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tWRH	5		5		5		ns	22, 25
$\overline{WE}$ setup time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tWRP	20		20		20		ns	22, 26
$\overline{WE}$ hold time (WCBR test cycle)	^tWTH	5		5		5		ns	22, 25
$\overline{WE}$ setup time	^tWTS	20		20		20		ns	22, 26

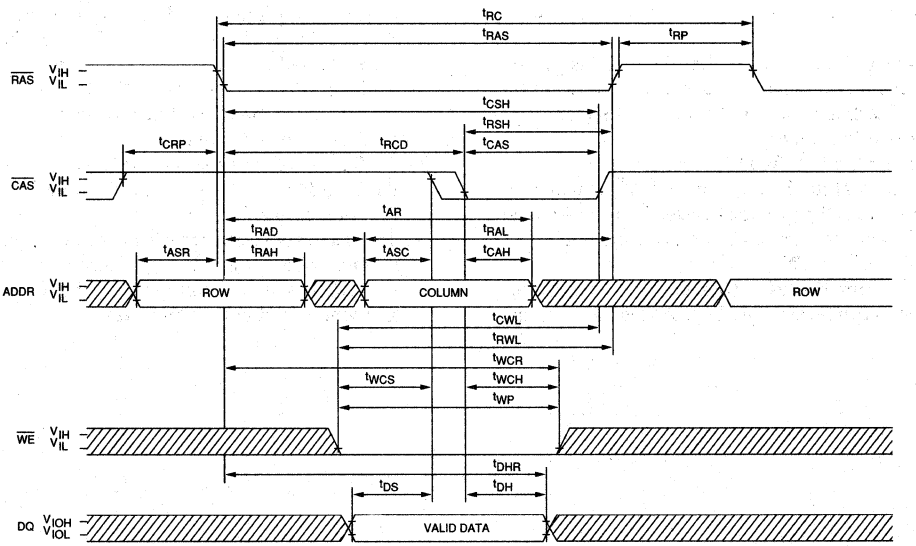
NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. V_{CC} = 5V ±10%, f = 1 MHz.
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is assured.
7. An initial pause of 100µs is required after power-up followed by eight $\overline{RAS}$ refresh cycles ($\overline{RAS}$-ONLY or CBR with $\overline{WE}$ HIGH) before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-up should be repeated any time the ^{t}REF refresh requirement is exceeded.
8. AC characteristics assume ^{t}T = 5ns.
9. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS}$ = V_{IH}, data output is High-Z.
12. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to 2 TTL gates and 100pF.
14. Assumes that ^{t}RCD < ^{t}RCD (MAX). If ^{t}RCD is greater than the maximum recommended value shown in this table, ^{t}RAC will increase by the amount that ^{t}RCD exceeds the value shown.
15. Assumes that ^{t}RCD ≥ ^{t}RCD (MAX).
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer, $\overline{CAS}$ must be pulsed HIGH for ^{t}CPN.
17. Operation within the ^{t}RCD (MAX) limit ensures that ^{t}RAC (MAX) can be met. ^{t}RCD (MAX) is specified as a reference point only; if ^{t}RCD is greater than the specified ^{t}RCD (MAX) limit, then access time is controlled exclusively by ^{t}CAC.
18. Operation within the ^{t}RAD (MAX) limit ensures that ^{t}RCD (MAX) can be met. ^{t}RAD (MAX) is specified as a reference point only; if ^{t}RAD is greater than the specified ^{t}RAD (MAX) limit, then access time is controlled exclusively by ^{t}AA.
19. Either ^{t}RCH or ^{t}RRH must be satisfied for a READ cycle.
20. ^{t}OFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
21. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW.
22. ^{t}WTS and ^{t}WTH are setup and hold specifications for the $\overline{WE}$ pin being held LOW to enable the JEDEC test mode (with CBR timing constraints). These two parameters are the inverse of ^{t}WRP and ^{t}WRH in the CBR refresh cycle.
23. Timing between the DRAMs and the DRAM card did not change with the addition of the line drivers.
24. A +5ns timing skew from the DRAM to the DRAM card resulted from the addition of line drivers.
25. A -5ns timing skew from the DRAM to the DRAM card resulted from the addition of line drivers.
26. A +10ns timing skew from the DRAM to the DRAM card resulted from the addition of line drivers.
27. A -10ns timing skew from the DRAM to the DRAM card resulted from the addition of line drivers.
28. A -5ns (MIN) and a -10ns (MAX) timing skew from the DRAM to the DRAM card resulted from the addition of line drivers.
29. A +5ns (MIN) and a +10ns (MAX) timing skew from the DRAM to the DRAM card resulted from the addition of line drivers.
30. The maximum current ratings are based with the memory operating or being refreshed in the x36 mode. The stated maximums may be reduced by one half when used in the x18 mode.

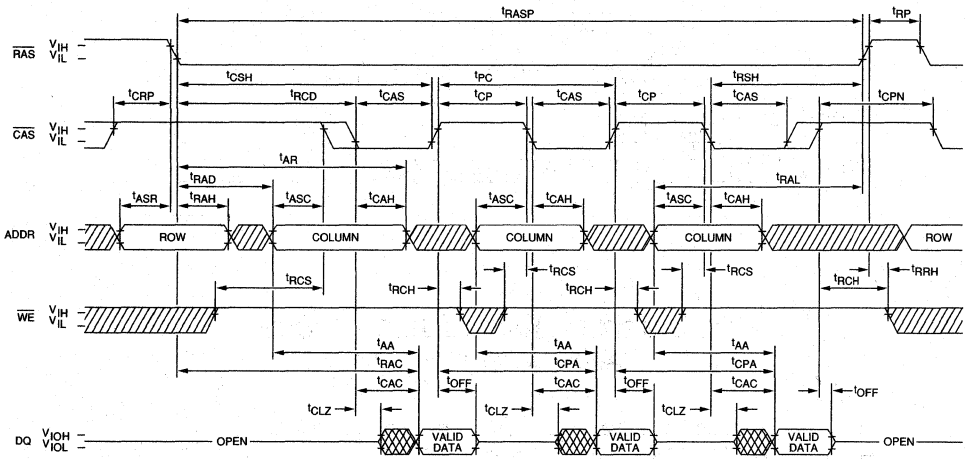
READ CYCLE



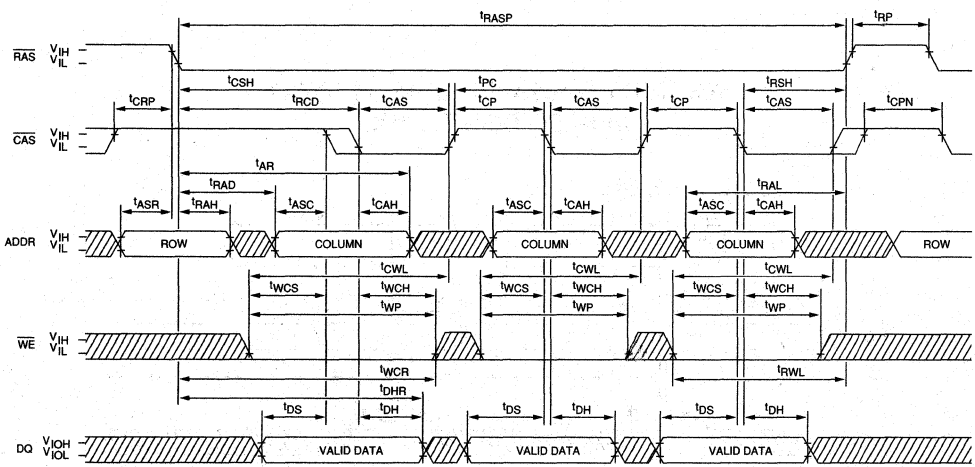
EARLY-WRITE CYCLE



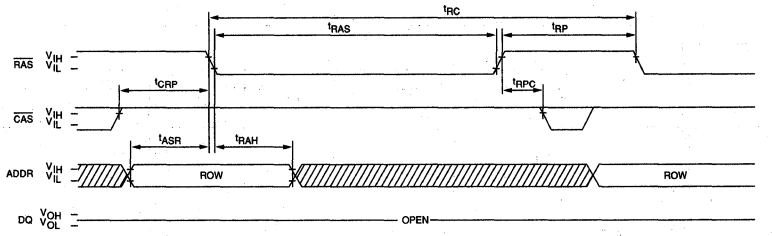
FAST-PAGE-MODE READ CYCLE



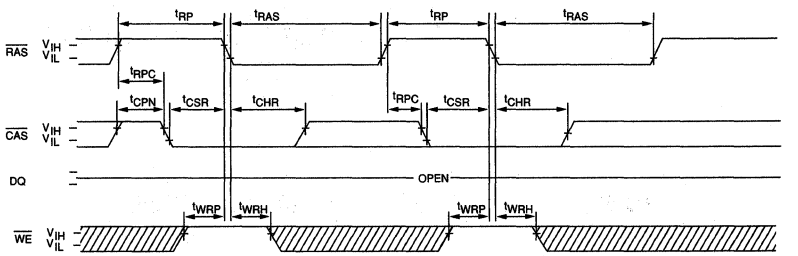
FAST-PAGE-MODE EARLY-WRITE CYCLE



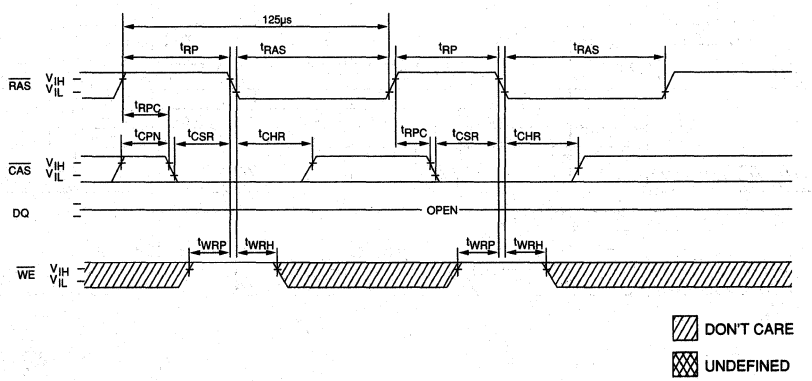
$\overline{RAS}$-ONLY REFRESH CYCLE
(ADDR = A0-A8; $\overline{WE}$ = DON'T CARE)



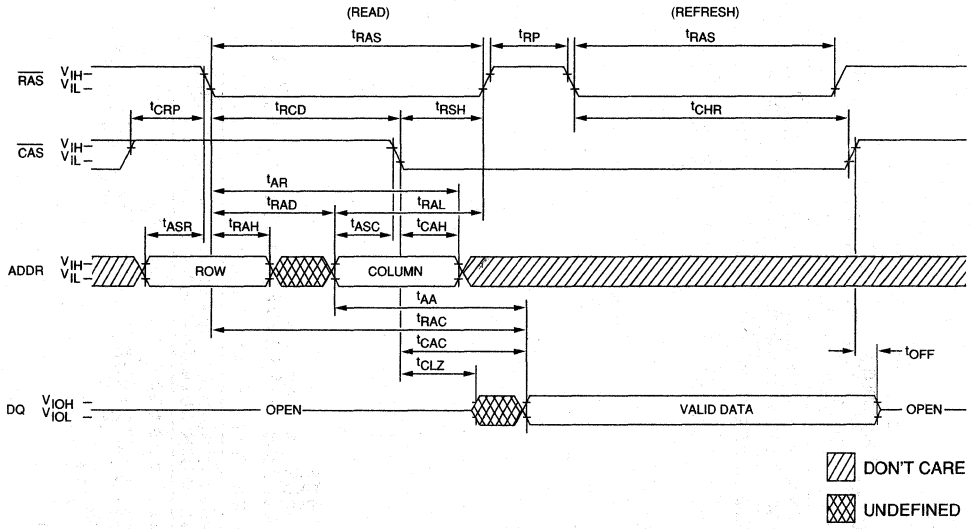
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE
(A0-A8 = DON'T CARE)



BATTERY BACKUP REFRESH CYCLE
(A0-A8 = DON'T CARE)



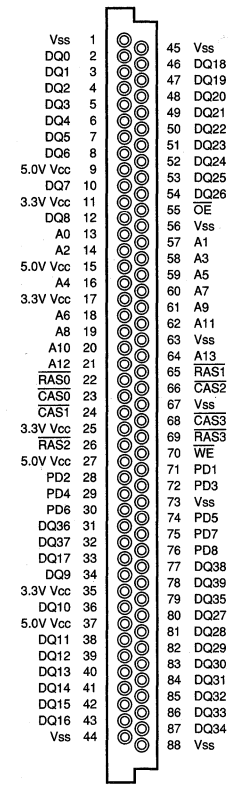
HIDDEN REFRESH CYCLE [21]
($\overline{WE}$ = HIGH)



NEW IC DRAM CARD

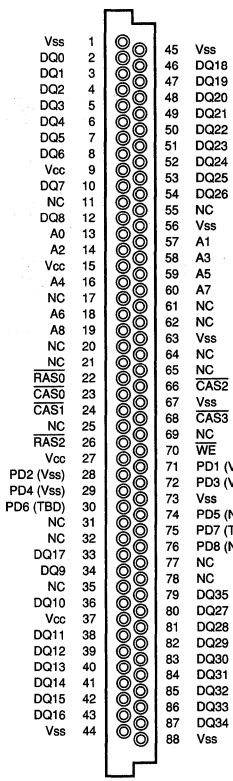
NEW ■ IC DRAM CARD

RESERVED JEDEC, JEIDA and PCMCIA 88-PIN ASSIGNMENT
(All Possible Combinations)



Vss	1	45	Vss
DQ0	2	46	DQ18
DQ1	3	47	DQ19
DQ2	4	48	DQ20
DQ3	5	49	DQ21
DQ4	6	50	DQ22
DQ5	7	51	DQ23
DQ6	8	52	DQ24
5.0V Vcc	9	53	DQ25
DQ7	10	54	DQ26
3.3V Vcc	11	55	$\overline{OE}$
DQ8	12	56	Vss
A0	13	57	A1
A2	14	58	A3
5.0V Vcc	15	59	A5
A4	16	60	A7
3.3V Vcc	17	61	A9
A6	18	62	A11
A8	19	63	Vss
A10	20	64	A13
A12	21	65	$\overline{RAS1}$
$\overline{RAS0}$	22	66	$\overline{CAS2}$
$\overline{CAS0}$	23	67	Vss
$\overline{CAS1}$	24	68	$\overline{CAS3}$
3.3V Vcc	25	69	$\overline{RAS3}$
$\overline{RAS2}$	26	70	$\overline{WE}$
5.0V Vcc	27	71	PD1
PD2	28	72	PD3
PD4	29	73	Vss
PD6	30	74	PD5
DQ36	31	75	PD7
DQ37	32	76	PD8
DQ17	33	77	DQ38
DQ9	34	78	DQ39
3.3V Vcc	35	79	DQ35
DQ10	36	80	DQ27
5.0V Vcc	37	81	DQ28
DQ11	38	82	DQ29
DQ12	39	83	DQ30
DQ13	40	84	DQ31
DQ14	41	85	DQ32
DQ15	42	86	DQ33
DQ16	43	87	DQ34
Vss	44	88	Vss

MT12D88C25636 PIN ASSIGNMENT
(JEDEC Standard)



Vss	1	45	Vss
DQ0	2	46	DQ18
DQ1	3	47	DQ19
DQ2	4	48	DQ20
DQ3	5	49	DQ21
DQ4	6	50	DQ22
DQ5	7	51	DQ23
DQ6	8	52	DQ24
Vcc	9	53	DQ25
DQ7	10	54	DQ26
NC	11	55	NC
DQ8	12	56	Vss
A0	13	57	A1
A2	14	58	A3
Vcc	15	59	A5
A4	16	60	A7
NC	17	61	NC
A6	18	62	NC
A8	19	63	Vss
NC	20	64	NC
NC	21	65	NC
$\overline{RAS0}$	22	66	$\overline{CAS2}$
$\overline{CAS0}$	23	67	Vss
$\overline{CAS1}$	24	68	$\overline{CAS3}$
NC	25	69	NC
$\overline{RAS2}$	26	70	$\overline{WE}$
Vcc	27	71	PD1 (Vss)
PD2 (Vss)	28	72	PD3 (Vss)
PD4 (Vss)	29	73	Vss
PD6 (TBD)	30	74	PD5 (NC)
NC	31	75	PD7 (TBD)
NC	32	76	PD8 (NC)
DQ17	33	77	NC
DQ9	34	78	NC
NC	35	79	DQ35
DQ10	36	80	DQ27
Vcc	37	81	DQ28
DQ11	38	82	DQ29
DQ12	39	83	DQ30
DQ13	40	84	DQ31
DQ14	41	85	DQ32
DQ15	42	86	DQ33
DQ16	43	87	DQ34
Vss	44	88	Vss

IC DRAM CARD 2 MEGABYTES

512K x 36, 1 MEG x 18

NEW ■ IC DRAM CARD

FEATURES

- JEIDA, JEDEC and PCMCIA standard 88-pin IC DRAM card
- Polarized receptacle connector
- Industry standard DRAM functions and timing
- High-performance, CMOS silicon-gate process
- All outputs are fully TTL compatible
- All inputs buffered except $\overline{RAS}$ inputs
- Multiple $\overline{RAS}$ inputs for x18 or x36 selectability
- Refresh modes: $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$ (CBR), HIDDEN and BATTERY BACKUP (BBU)
- FAST PAGE MODE access cycle
- Single +5V ±5% power supply
- Low power; 24mW standby, 2.7W active (typical)
- Extended refresh standard: 512 cycles every 64ms

OPTIONS MARKING

- Timing

60ns access	-6
70ns access	-7
80ns access	-8

GENERAL DESCRIPTION

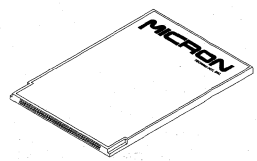
The MT24D88C51236 is a 2 megabyte, IC DRAM card organized as a 512K x 36 bit memory array. It may also be configured as a 1 Meg x 18 bit memory array, provided the corresponding DQs on the host system are made common and memory bank control procedures are implemented. Separate $\overline{CAS}$ inputs allow byte accesses.

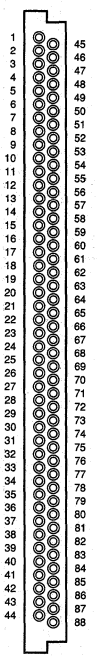
All inputs to the DRAMs are buffered, with the exception of $\overline{RAS}$. The line drivers used for buffers reduce reflections on the card and ensure compatibility in a wide range of systems. At the same time, the line drivers add delays to the buffered input timings when compared to standard DRAMs.

The MT24D88C51236 is designed for low power operation using 256K x 4 low power, extended refresh DRAMs. These devices support BATTERY BACKUP (BBU) cycle refresh; a very low current, data retention mode. Standard component DRAM refresh modes are supported as well.

Multiple $\overline{RAS}$ inputs conserve power by allowing individual bank selection. In the x36 organization, the memory array may be divided into two banks, each with four separate bytes. In the x18 organization, up to four banks, each with two separate bytes, may be independently selected. One bank is activated by each $\overline{RAS}$ selection; the others not selected remain in standby mode, drawing minimum power.

PIN ASSIGNMENT (End View)
88-Pin Card (U-1)





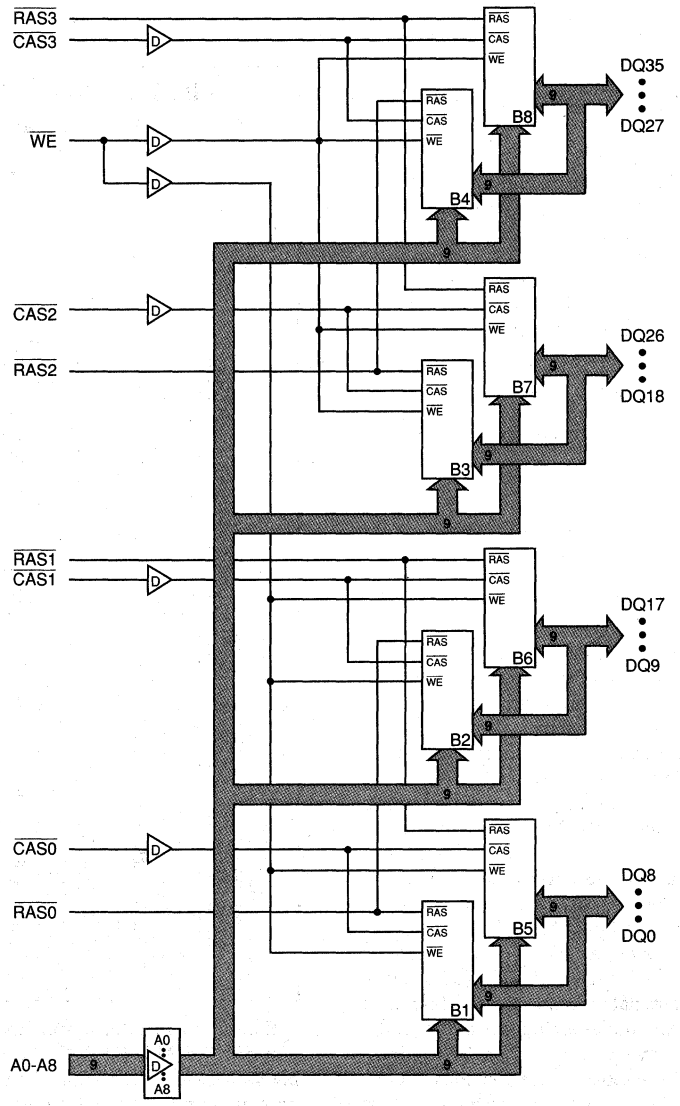
PIN #	SYMBOL	PIN #	SYMBOL	PIN #	SYMBOL
1	Vss	31	NC	61	NC
2	DQ0	32	NC	62	NC
3	DQ1	33	DQ17	63	Vss
4	DQ2	34	DQ9	64	NC
5	DQ3	35	NC	65	$\overline{RAS1}$
6	DQ4	36	DQ10	66	$\overline{CAS2}$
7	DQ5	37	Vcc	67	Vss
8	DQ6	38	DQ11	68	$\overline{CAS3}$
9	Vcc	39	DQ12	69	$\overline{RAS3}$
10	DQ7	40	DQ13	70	$\overline{WE}$
11	NC	41	DQ14	71	PD1 (Vss)
12	DQ8	42	DQ15	72	PD3 (Vss)
13	A0	43	DQ16	73	Vss
14	A2	44	Vss	74	PD5 (Vss)
15	Vcc	45	Vss	75	PD7 (TBD)
16	A4	46	DQ18	76	PD8 (NC)
17	NC	47	DQ19	77	NC
18	A6	48	DQ20	78	NC
19	A8	49	DQ21	79	DQ35
20	NC	50	DQ22	80	DQ27
21	NC	51	DQ23	81	DQ28
22	$\overline{RAS0}$	52	DQ24	82	DQ29
23	$\overline{CAS0}$	53	DQ25	83	DQ30
24	$\overline{CAS1}$	54	DQ26	84	DQ31
25	NC	55	NC	85	DQ32
26	$\overline{RAS2}$	56	Vss	86	DQ33
27	Vcc	57	A1	87	DQ34
28	PD2 (Vss)	58	A3	88	Vss
29	PD4 (Vss)	59	A5		
30	PD6 (TBD)	60	A7		

Eight presence detect pins may be read by the host to identify the MT24D88C51236 organization, number of banks, access time and refresh mode. These extensive presence detect functions allow systems to utilize the advanced power-saving features.

The MT24D88C51236 is built with a plastic frame covered by stainless steel panels. This package, containing an 88-pin receptacle connector, is keyed to prevent improper installation or insertion into other types of IC card sockets.

NEW ■ IC DRAM CARD

FUNCTIONAL BLOCK DIAGRAM



NOTE: 1. D = 74AC11244 line drivers.
2. B1 through B8 = 256K x 8 memory blocks.

PIN DESCRIPTIONS

PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
22, 26, 65, 69	$\overline{RAS}$0-3	Input	Row Address Strobe: $\overline{RAS}$ is used to clock-in the 9 row-address bits. Four $\overline{RAS}$ inputs allow for two x36 banks or four x18 banks.
23, 24, 66, 68	$\overline{CAS}$0-3	Input	Column Address Strobe: $\overline{CAS}$ is used to clock-in the 9 column-address bits, enable the DRAM output buffers, and strobe the data inputs on WRITE cycles. Four $\overline{CAS}$ inputs allow byte access control for any memory bank configuration.
70	$\overline{WE}$	Input	Write Enable: $\overline{WE}$ is the READ/WRITE control for the DQ pins. If $\overline{WE}$ is LOW prior to $\overline{CAS}$ going LOW, the access is a WRITE cycle. If $\overline{WE}$ is HIGH while $\overline{CAS}$ is LOW, the access is a READ cycle.
13, 57, 14, 58, 16, 59, 18, 60, 19	A0-A8	Input	Address Inputs: These inputs are multiplexed and clocked by $\overline{RAS}$ and $\overline{CAS}$.
2-8, 10, 12, 34, 36, 38-43, 33, 46-54, 80-87, 79	DQ0-DQ35	Input/ Output	Data I/O: For WRITE cycles, DQ0-DQ35 act as inputs to the addressed DRAM location. BYTE WRITEs may be performed by using the corresponding $\overline{CAS}$ select. For READ access cycles, DQ0-DQ35 act as outputs for the addressed DRAM location.
71, 28, 72, 29, 74, 30, 75, 76	PD1-PD8	-	Presence Detect: These pins are read by the host system and tell the system the card's personality. They will be either left floating (NC) or they will be grounded (Vss).
11, 17, 20, 21, 25, 31, 32, 35, 61, 62, 55, 64, 77, 78	NC	-	No Connect: These pins should be left unconnected (reserved for future use).
9, 15, 27, 37	Vcc	Supply	Power Supply: +5V ±5%
1, 44, 45, 56, 63, 67, 73, 88	Vss	Supply	Ground

FUNCTIONAL DESCRIPTION

The MT24D88C51236 is a 2 megabyte memory card structured as a 512K x 36 bit memory array ($\overline{RAS0}$ = $\overline{RAS2}$ $\overline{RAS1}$ = $\overline{RAS3}$). It also may be configured as a 1 Meg x 18 bit memory array provided the corresponding DQs on the host are connected and memory bank control procedures are implemented by interleaving all four $\overline{RAS}$ lines.

Most x36 bit applications use the same signal to control the $\overline{CAS}$ inputs. $\overline{RAS0}$ and $\overline{RAS1}$ control the lower 18 bits, and $\overline{RAS2}$ and $\overline{RAS3}$ control the upper 18 bits to obtain a x36 memory array. For x18 applications, the corresponding DQs and the corresponding $\overline{CAS}$ pins must be connected together (DQ0 to DQ18, DQ1 to DQ19 and so forth, and $\overline{CAS0}$ to $\overline{CAS2}$ and $\overline{CAS1}$ to $\overline{CAS3}$). Each $\overline{RAS}$ is then a bank select for the 1 Meg x 18 memory organization.

DRAM OPERATION

DRAM REFRESH

Memory cell data is retained in its correct state by maintaining power and executing any $\overline{RAS}$ cycle [READ, WRITE, $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$ (CBR), HIDDEN or BATTERY BACKUP (BBU) REFRESH] so that all 512 combinations of $\overline{RAS}$ addresses (A0-A8) are executed at least every 64ms, regardless of sequence.

The implied method of choice for refreshing the memory card is the BBU cycle. This is a very low current, data retention mode made possible by using the CBR REFRESH cycle over the extended refresh range (I_{CC7}).

The memory card may be used with the other refresh modes common in standard DRAMs. This allows the memory card to be used on existing systems that do not utilize the BBU REFRESH cycle. However, the memory card will draw more current in the STANDBY mode. The CBR REFRESH mode is recommended when not using the BBU mode.

DRAM READ AND WRITE CYCLES

During READ or WRITE cycles, each bit is uniquely addressed through the 18 address bits, which are entered 9 bits (A0-A8) at a time. $\overline{RAS}$ is used to latch the first 9 bits and $\overline{CAS}$ the latter 9 bits. READ or WRITE cycles are selected with the $\overline{WE}$ input. A logic HIGH on $\overline{WE}$ dictates READ mode while a logic LOW on $\overline{WE}$ dictates WRITE mode. During a WRITE cycle, data in (D) is latched by the falling edge of $\overline{CAS}$. $\overline{WE}$ must fall prior to $\overline{CAS}$ (EARLY WRITE); if $\overline{WE}$ goes LOW after $\overline{CAS}$, the outputs (Q) will be activated and will drive invalid data to the inputs. The data inputs and data outputs are routed through pins using common I/O, and pin direction is controlled by $\overline{WE}$.

FAST PAGE MODE operation allows faster data operations (READ or WRITE) within a row address (A0-A8) defined page boundary. The FAST PAGE MODE cycle is always initiated with a row address strobed-in by $\overline{RAS}$ followed by a column address strobed-in by $\overline{CAS}$. $\overline{CAS}$ may be toggled-in by holding $\overline{RAS}$ LOW and strobing-in different column addresses, thus executing faster memory cycles. Returning $\overline{RAS}$ HIGH terminates the FAST PAGE MODE operation. Returning $\overline{RAS}$ and $\overline{CAS}$ HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the $\overline{RAS}$ high time.

DRAM TIMING

In accordance with JEDEC standard specifications, all inputs to the IC DRAM card are buffered, with the exception of the $\overline{RAS}$ inputs. The line drivers used for buffers reduce reflections on the card and ensure compatibility in a wide range of systems. The implementation of buffers on the card may relieve the need for additional host system line drivers. Notes 23 though 29 indicate which parameters on the IC DRAM card are affected by the line drivers, and to what magnitude they are affected. The component DRAM timing specifications, rather than those of the IC DRAM card (in systems that use both), may cause timing incompatibilities.

All traces on the IC DRAM card (buffered and non-buffered) are approximately 50 ohms characteristic impedance. Matching impedance on the system board to 50 ohms characteristic impedance on traces to the IC DRAM card will decrease signal noise to the IC DRAM card, enhancing overall system reliability.

PHYSICAL DESIGN

The MT24D88C51236 is constructed with a molded plastic frame and covered with stainless steel panels. Inside, 24 thin small-outline package (TSOP) DRAMs are mounted on both sides of an ultrathin printed circuit board. The board is attached to a high insertion, 88-pin receptacle connector. The package has a polarized key to prevent improper installation, including insertion into other types of IC card sockets. The MT24D88C51236 operates reliably up to 55°C.

MEMORY TRUTH TABLE

FUNCTION		RAS	CAS	WE	ADDRESSES tR	ADDRESSES tC	DATA IN/OUT DQ0-DQ35
Standby		H	H→X	X	X	X	High-Z
READ		L	L	H	ROW	COL	Data Out
EARLY-WRITE		L	L	L	ROW	COL	Data In
READ-WRITE		L	L	H→L	ROW	COL	Data In
FAST-PAGE-MODE	1st Cycle	L	H→L	H	ROW	COL	Data Out
READ	2nd Cycle	L	H→L	H	n/a	COL	Data Out
FAST-PAGE-MODE	1st Cycle	L	H→L	L	ROW	COL	High-Z
EARLY-WRITE	2nd Cycle	L	H→L	L	n/a	COL	High-Z
FAST-PAGE-MODE	1st Cycle	L	H→L	H→L	ROW	COL	Data Out
READ-WRITE	2nd Cycle	L	H→L	H→L	n/a	COL	Data Out
RAS-ONLY REFRESH		H	X	X	ROW	n/a	High-Z
HIDDEN	READ	L→H→L	L	H	ROW	COL	Data Out
REFRESH	WRITE	L→H→L	L	L	ROW	COL	Data In
CAS-BEFORE-RAS REFRESH		H→L	L	H	X	X	High-Z
BATTERY BACKUP REFRESH		H→L	L	H	X	X	High-Z

PRESENCE DETECT TRUTH TABLE

CHARACTERISTICS						PRESENT DETECT PIN (PDx)							
Card Density	DRAM Organizations	Card Address	RAS Address	CAS Address	Page Depth	1	2	3	4	5	6	7	8
0MB	No card installed	X	X	X	X	NC	NC	NC	NC	NC	X	X	X
1MB	256K x 1, 4, 16, 18	18	9	9	512	Vss	Vss	Vss	Vss	NC	X	X	X
• 2MB	256K x 1, 4, 16, 18	18	9	9	512	Vss	Vss	Vss	Vss	Vss	X	X	X
2MB	512K x 8, 9	19	10	9	512	NC	Vss	Vss	Vss	NC	X	X	X
4MB	512K x 8, 9	19	10	9	512	NC	Vss	Vss	Vss	Vss	X	X	X
4MB	1 Meg x 1, 4, 16, 18	20	10	10	1,024	Vss	NC	Vss	Vss	NC	X	X	X
8MB	1 Meg x 1, 4, 16, 18	20	10	10	1,024	Vss	NC	Vss	Vss	Vss	X	X	X
8MB	2 Meg x 8, 9	21	11	10	1,024	NC	NC	Vss	Vss	NC	X	X	X
16MB	2 Meg x 8, 9	21	11	10	1,024	NC	NC	Vss	Vss	Vss	X	X	X
16MB	4 Meg x 1, 4, 16, 18	22	12	11	1,024	Vss	Vss	NC	Vss	NC	X	X	X
32MB	4 Meg x 1, 4, 16, 18	22	12	11	1,024	Vss	Vss	NC	Vss	Vss	X	X	X
Access Timing		100ns				X	X	X	X	X	Vss	Vss	X
		80ns				X	X	X	X	X	NC	Vss	X
		70ns				X	X	X	X	X	Vss	NC	X
		60ns				X	X	X	X	X	NC	NC	X
		50ns				X	X	X	X	X	Vss	Vss	X
Refresh Control		Standard				X	X	X	X	X	X	X	NC
		Auto				X	X	X	X	X	X	X	Vss

NOTE: Vss = Ground.

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} ..... -0.5V to +5.25V
Operating Temperature T_A (Ambient) ..... 0°C to 55°C
Storage Temperature ..... -20°C to +80°C
Power Dissipation 15W
Short Circuit Output Current 50mA
Card Insertions (Connector's Life Cycle) 10,000

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 3, 4, 6, 7) (0°C ≤ T_A ≤ 55°C; V_{CC} = 5V ±5%)

PARAMETER/CONDITION		SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage		V_{CC}	4.75	5.25	V	1
Input High (Logic 1) Voltage, All Inputs		V_{IH}	3.5	V_{CC}+0.5	V	1
Input Low (Logic 0) Voltage, All Inputs		V_{IL}	-0.5	0.8	V	1
INPUT LEAKAGE CURRENT, Any input	Non-buffered	I_{IN}	-12	12	µA	
(0V ≤ V_{IN} ≤ 5.25V; all other pins not under test = 0V)	Buffered	I_{IB}	-2	2	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled; 0V ≤ V_{OUT} ≤ 5.25V)		I_{OZ}	-10	10	µA	
OUTPUT LEVELS Output High Voltage (I_{OUT} = -5mA)		V_{OH}	2.4		V	
Output Low Voltage (I_{OUT} = 4.2mA)		V_{OL}		0.4	V	

		MAX				
PARAMETER/CONDITION	SYMBOL	-6	-7	-8	UNITS	NOTES
STANDBY CURRENT: (TTL) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC1}	48	48	48	mA	
STANDBY CURRENT: (CMOS) ($\overline{RAS}$ = $\overline{CAS}$ = Other Inputs = V_{CC} -0.2V)	I_{CC2}	4.8	4.8	4.8	mA	
OPERATING CURRENT: Random READ/WRITE Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC (MIN))	I_{CC3}	1.0	0.9	0.8	A	3, 4, 30
OPERATING CURRENT: FAST PAGE MODE Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: ^tPC = ^tPC (MIN))	I_{CC4}	780	660	540	mA	3, 4, 30
REFRESH CURRENT: $\overline{RAS}$-ONLY Average power supply current ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}: ^tRC = ^tRC (MIN))	I_{CC5}	1.0	0.9	0.8	A	3, 30
REFRESH CURRENT: $\overline{CAS}$-BEFORE-$\overline{RAS}$ (CBR) Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC (MIN))	I_{CC6}	1.0	0.9	0.8	A	3, 5, 30
REFRESH CURRENT: BATTERY BACKUP (BBU) Average power supply current during BBU: $\overline{CAS}$ = 0.2V or CBR cycling; $\overline{RAS}$ = ^tRAS (MIN) up to 300ns; ^tRC = 125µs; $\overline{WE}$, A0-A8 and DQ = V_{CC} -0.2V or 0.2V (DQ may be left open)	I_{CC7}	4.8	4.8	4.8	mA	3, 5

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: $\overline{CAS0}$, $\overline{CAS1}$, $\overline{CAS2}$, $\overline{CAS3}$, A0-A8	C_{I1}		9	pF	2
Input Capacitance: $\overline{WE}$	C_{I2}		13	pF	2
Input Capacitance: $\overline{RAS0}$, $\overline{RAS1}$, $\overline{RAS2}$, $\overline{RAS3}$	C_{I3}		50	pF	2
Input/Output Capacitance: DQ	C_{IO}		20	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) ($0°C \le T_A \le 55°C$; V_{CC} = 5V ±5%)

AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	^tRC	110		130		150		ns	23
FAST-PAGE-MODE READ or WRITE cycle time	^tPC	40		40		45		ns	23
Access time from $\overline{RAS}$	^tRAC		60		70		80	ns	14, 23
Access time from $\overline{CAS}$	^tCAC		25		30		30	ns	15, 26
Access time from column address	^tAA		40		45		50	ns	26
Access time from $\overline{CAS}$ precharge	^tCPA		50		50		55	ns	26
$\overline{RAS}$ pulse width	^tRAS	60	100,000	70	100,000	80	100,000	ns	23
$\overline{RAS}$ pulse width (FAST PAGE MODE)	^tRASP	60	100,000	70	100,000	80	100,000	ns	23
$\overline{RAS}$ hold time	^tRSH	25		30		30		ns	26
$\overline{RAS}$ precharge time	^tRP	40		50		60		ns	23
$\overline{CAS}$ pulse width	^tCAS	15	100,000	20	100,000	20	100,000	ns	23
$\overline{CAS}$ hold time	^tCSH	55		65		75		ns	25
$\overline{CAS}$ precharge time	^tCPN	10		10		10		ns	16, 23
$\overline{CAS}$ precharge time (FAST PAGE MODE)	^tCP	10		10		10		ns	23
$\overline{RAS}$ to $\overline{CAS}$ delay time	^tRCD	10	35	15	40	15	50	ns	17, 28
$\overline{CAS}$ to $\overline{RAS}$ precharge time	^tCRP	15		15		15		ns	26
Row address setup time	^tASR	10		10		10		ns	26
Row address hold time	^tRAH	5		5		5		ns	25
$\overline{RAS}$ to column address delay time	^tRAD	10	20	10	25	10	30	ns	18, 28
Column address setup time	^tASC	5		5		5		ns	24
Column address hold time	^tCAH	15		20		20		ns	24
Column address hold time (referenced to $\overline{RAS}$)	^tAR	45		50		55		ns	25
Column address to $\overline{RAS}$ lead time	^tRAL	40		45		50		ns	26
Read command setup time	^tRCS	5		5		5		ns	25
Read command hold time (referenced to $\overline{CAS}$)	^tRCH	5		5		5		ns	19, 24
Read command hold time (referenced to $\overline{RAS}$)	^tRRH	-5		-5		-5		ns	19, 25
$\overline{CAS}$ to output in Low-Z	^tCLZ	5		5		5		ns	24
Output buffer turn-off delay	^tOFF	5	30	5	30	5	30	ns	20, 29
$\overline{WE}$ command setup time	^tWCS	5		5		5		ns	24

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

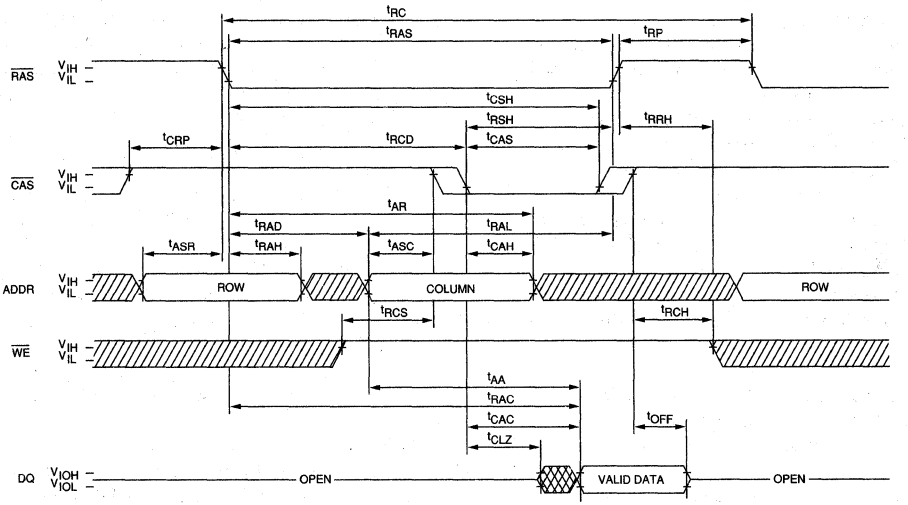
(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C ≤ T_A ≤ 55°C; Vcc = 5V ±5%)

AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Write command hold time	^tWCH	15		20		20		ns	24
Write command hold time (referenced to $\overline{RAS}$)	^tWCR	40		50		55		ns	25
Write command pulse width	^tWP	10		15		15		ns	23
Write command to $\overline{RAS}$ lead time	^tRWL	25		30		30		ns	26
Write command to $\overline{CAS}$ lead time	^tCWL	20		25		25		ns	24
Data-in setup time	^tDS	5		5		5		ns	24
Data-in hold time	^tDH	5		10		10		ns	25
Data-in hold time (referenced to $\overline{RAS}$)	^tDHR	45		55		60		ns	23
Transition time (rise or fall)	^tT	2	15	2	15	2	15	ns	9, 10, 23
Refresh period (1,024 cycles)	^tREF		64		64		64	ms	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	^tRPC	10		10		10		ns	26
$\overline{CAS}$ setup time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tCSR	20		20		20		ns	5, 26
$\overline{CAS}$ hold time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tCHR	10		10		10		ns	5, 25
$\overline{WE}$ hold time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tWRH	5		5		5		ns	22, 25
$\overline{WE}$ setup time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tWRP	20		20		20		ns	22, 26
$\overline{WE}$ hold time (WCBR test cycle)	^tWTH	5		5		5		ns	22, 25
$\overline{WE}$ setup time	^tWTS	20		20		20		ns	22, 26

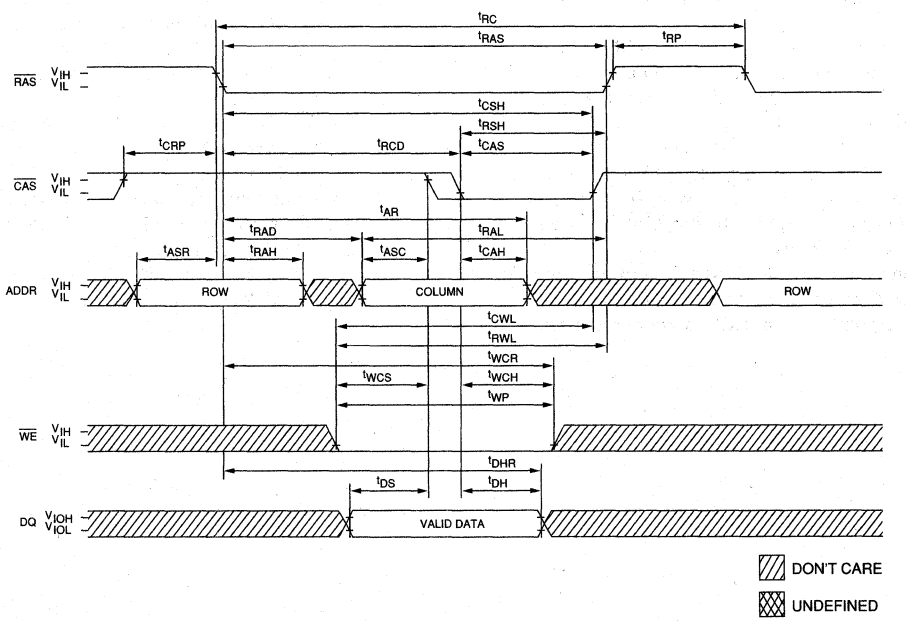
NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. V_{CC} = 5V ±10%, f = 1 MHz.
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is assured.
7. An initial pause of 100µs is required after power-up followed by eight $\overline{RAS}$ refresh cycles ($\overline{RAS}$-ONLY or CBR with $\overline{WE}$ HIGH) before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-up should be repeated any time the ^{t}REF refresh requirement is exceeded.
8. AC characteristics assume ^{t}T = 5ns.
9. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS}$ = V_{IH}, data output is High-Z.
12. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to 2 TTL gates and 100pF.
14. Assumes that ^{t}RCD < ^{t}RCD (MAX). If ^{t}RCD is greater than the maximum recommended value shown in this table, ^{t}RAC will increase by the amount that ^{t}RCD exceeds the value shown.
15. Assumes that ^{t}RCD ≥ ^{t}RCD (MAX).
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer, $\overline{CAS}$ must be pulsed HIGH for ^{t}CPN.
17. Operation within the ^{t}RCD (MAX) limit ensures that ^{t}RAC (MAX) can be met. ^{t}RCD (MAX) is specified as a reference point only; if ^{t}RCD is greater than the specified ^{t}RCD (MAX) limit, then access time is controlled exclusively by ^{t}CAC.
18. Operation within the ^{t}RAD (MAX) limit ensures that ^{t}RCD (MAX) can be met. ^{t}RAD (MAX) is specified as a reference point only; if ^{t}RAD is greater than the specified ^{t}RAD (MAX) limit, then access time is controlled exclusively by ^{t}AA.
19. Either ^{t}RCH or ^{t}RRH must be satisfied for a READ cycle.
20. ^{t}OFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
21. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW.
22. ^{t}WTS and ^{t}WTH are setup and hold specifications for the $\overline{WE}$ pin being held LOW to enable the JEDEC test mode (with CBR timing constraints). These two parameters are the inverse of ^{t}WRP and ^{t}WRH in the CBR refresh cycle.
23. Timing between the DRAMs and the DRAM card did not change with the addition of the line drivers.
24. A +5ns timing skew from the DRAM to the DRAM card resulted from the addition of line drivers.
25. A -5ns timing skew from the DRAM to the DRAM card resulted from the addition of line drivers.
26. A +10ns timing skew from the DRAM to the DRAM card resulted from the addition of line drivers.
27. A -10ns timing skew from the DRAM to the DRAM card resulted from the addition of line drivers.
28. A -5ns (MIN) and a -10ns (MAX) timing skew from the DRAM to the DRAM card resulted from the addition of line drivers.
29. A +5ns (MIN) and a +10ns (MAX) timing skew from the DRAM to the DRAM card resulted from the addition of line drivers.
30. The maximum current ratings are based on one of the two banks operating or being refreshed (x36 mode). The stated maximums may be reduced by one half when used in the x18 mode. Standby currents of the non-active bank are not included.

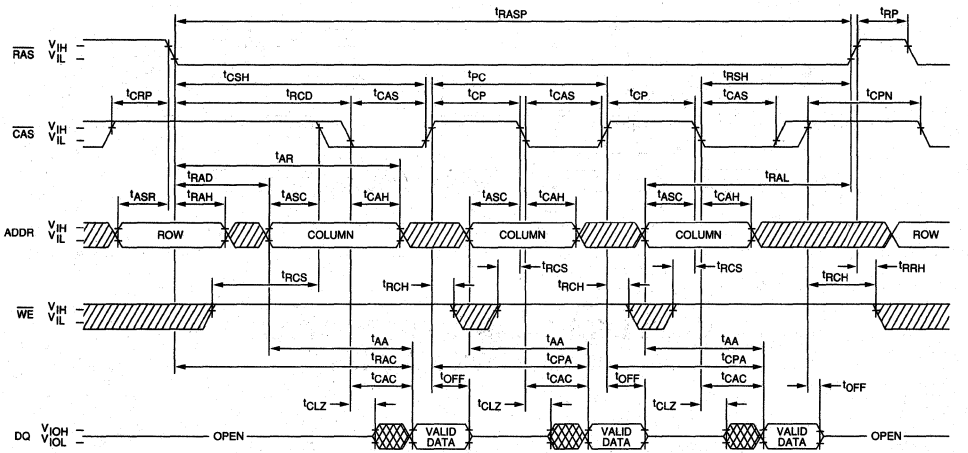
READ CYCLE



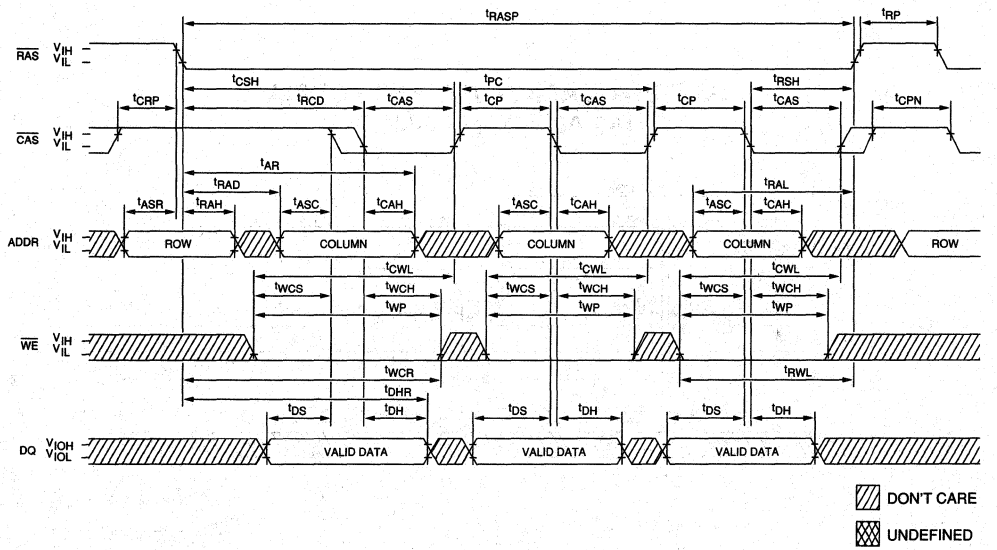
EARLY-WRITE CYCLE



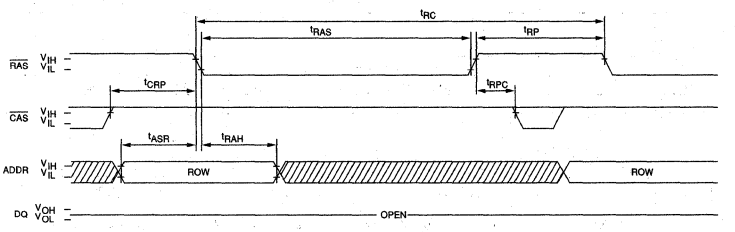
FAST-PAGE-MODE READ CYCLE



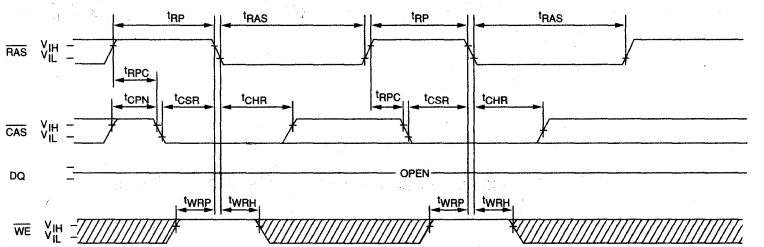
FAST-PAGE-MODE EARLY-WRITE CYCLE



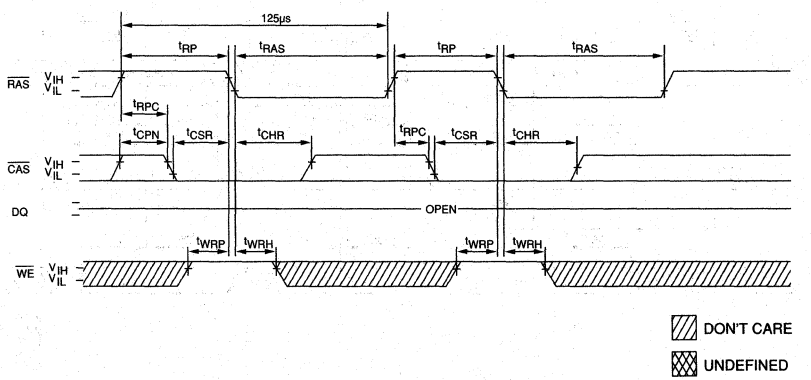
$\overline{\text{RAS}}$-ONLY REFRESH CYCLE
(ADDR = A0-A8; $\overline{\text{WE}}$ = DON'T CARE)



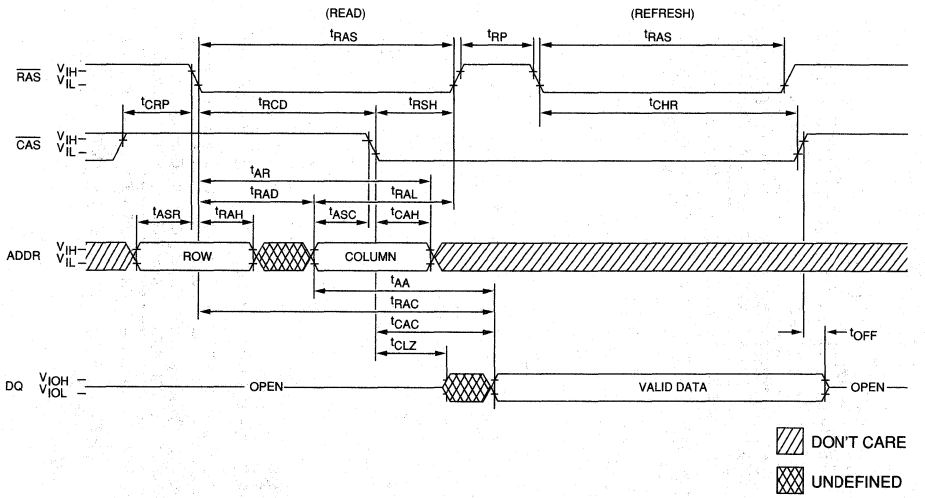
$\overline{\text{CAS}}$-BEFORE-$\overline{\text{RAS}}$ REFRESH CYCLE
(A0-A8 = DON'T CARE)



BATTERY BACKUP REFRESH CYCLE
(A0-A8 = DON'T CARE)

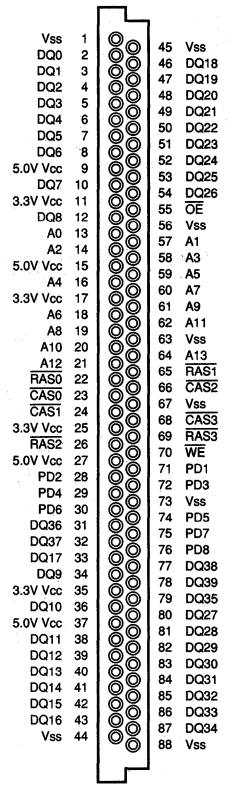


HIDDEN REFRESH CYCLE [21]
($\overline{WE}$ = HIGH)



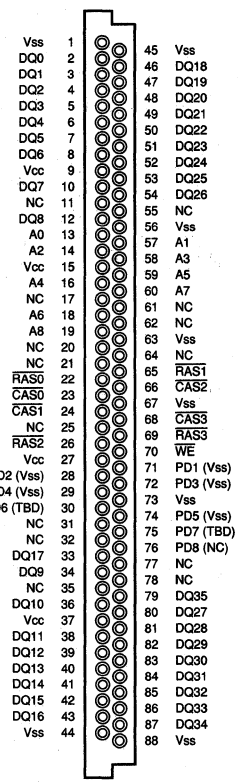
NEW ■ IC DRAM CARD

RESERVED JEDEC, JEIDA and PCMCIA 88-PIN ASSIGNMENT
(All Possible Combinations)



Vss	1	45	Vss
DQ0	2	46	DQ18
DQ1	3	47	DQ19
DQ2	4	48	DQ20
DQ3	5	49	DQ21
DQ4	6	50	DQ22
DQ5	7	51	DQ23
DQ6	8	52	DQ24
5.0V Vcc	9	53	DQ25
DQ7	10	54	DQ26
3.3V Vcc	11	55	$\overline{OE}$
DQ8	12	56	Vss
A0	13	57	A1
A2	14	58	A3
5.0V Vcc	15	59	A5
A4	16	60	A7
3.3V Vcc	17	61	A9
A6	18	62	A11
A8	19	63	Vss
A10	20	64	A13
A12	21	65	$\overline{RAS1}$
$\overline{RAS0}$	22	66	$\overline{CAS2}$
$\overline{CAS0}$	23	67	Vss
$\overline{CAS1}$	24	68	$\overline{CAS3}$
3.3V Vcc	25	69	$\overline{RAS3}$
$\overline{RAS2}$	26	70	$\overline{WE}$
5.0V Vcc	27	71	PD1
PD2	28	72	PD3
PD4	29	73	Vss
PD6	30	74	PD5
DQ36	31	75	PD7
DQ37	32	76	PD8
DQ17	33	77	DQ38
DQ9	34	78	DQ39
3.3V Vcc	35	79	DQ35
DQ10	36	80	DQ27
5.0V Vcc	37	81	DQ28
DQ11	38	82	DQ29
DQ12	39	83	DQ30
DQ13	40	84	DQ31
DQ14	41	85	DQ32
DQ15	42	86	DQ33
DQ16	43	87	DQ34
Vss	44	88	Vss

MT24D88C51236 PIN ASSIGNMENT
(JEDEC Standard)



Vss	1	45	Vss
DQ0	2	46	DQ18
DQ1	3	47	DQ19
DQ2	4	48	DQ20
DQ3	5	49	DQ21
DQ4	6	50	DQ22
DQ5	7	51	DQ23
DQ6	8	52	DQ24
Vcc	9	53	DQ25
DQ7	10	54	DQ26
NC	11	55	NC
DQ8	12	56	Vss
A0	13	57	A1
A2	14	58	A3
Vcc	15	59	A5
A4	16	60	A7
NC	17	61	NC
A6	18	62	NC
A8	19	63	Vss
NC	20	64	NC
NC	21	65	$\overline{RAS1}$
$\overline{RAS0}$	22	66	$\overline{CAS2}$
$\overline{CAS0}$	23	67	Vss
$\overline{CAS1}$	24	68	$\overline{CAS3}$
NC	25	69	$\overline{RAS3}$
$\overline{RAS2}$	26	70	$\overline{WE}$
Vcc	27	71	PD1 (Vss)
PD2 (Vss)	28	72	PD3 (Vss)
PD4 (Vss)	29	73	Vss
PD6 (TBD)	30	74	PD5 (Vss)
NC	31	75	PD7 (TBD)
NC	32	76	PD8 (NC)
DQ17	33	77	NC
DQ9	34	78	NC
NC	35	79	DQ35
DQ10	36	80	DQ27
Vcc	37	81	DQ28
DQ11	38	82	DQ29
DQ12	39	83	DQ30
DQ13	40	84	DQ31
DQ14	41	85	DQ32
DQ15	42	86	DQ33
DQ16	43	87	DQ34
Vss	44	88	Vss

IC DRAM CARD 4 MEGABYTES

1 MEG x 36, 2 MEG x 18

NEW IC DRAM CARD

FEATURES

- JEIDA, JEDEC and PCMCIA standard 88-pin IC DRAM card
- Polarized receptacle connector
- Industry standard DRAM functions and timing
- High-performance, CMOS silicon-gate process
- All outputs are fully TTL compatible
- All inputs buffered except $\overline{RAS}$ inputs
- Multiple $\overline{RAS}$ inputs for x18 or x36 selectability
- Refresh modes: $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$ (CBR), HIDDEN and BATTERY BACKUP (BBU)
- FAST PAGE MODE access cycle
- Single +5V ±5% power supply
- Low power; 12mW standby, 3.1W active (typical)
- Extended refresh standard: 1,024 cycles every 128ms

OPTIONS MARKING

- Timing

60ns access	-6
70ns access	-7
80ns access	-8

GENERAL DESCRIPTION

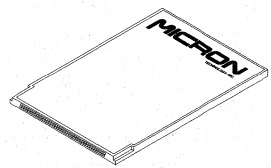
The MT12D88C136 is a 4 megabyte, IC DRAM card organized as a 1 Meg x 36 bit memory array. It may also be configured as a 2 Meg x 18 bit memory array, provided the corresponding DQs on the host system are made common, and memory bank control procedures are implemented. Separate $\overline{CAS}$ inputs allow byte accesses.

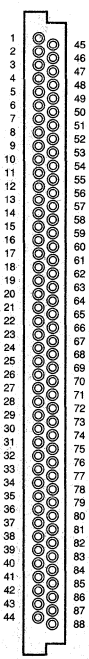
All inputs to the DRAMs are buffered, with the exception of $\overline{RAS}$. The line drivers used for buffers reduce reflections on the card and ensure compatibility in a wide range of systems. At the same time, the line drivers add delays to the buffered input timings when as compared to standard DRAMs.

The MT12D88C136 is designed for low power operation using 1 Meg x 4 low power, extended refresh DRAMs. These devices support BATTERY BACKUP (BBU) cycle refresh; a very low current, data retention mode. Standard component DRAM refresh modes are supported as well.

Multiple $\overline{RAS}$ inputs conserve power by allowing individual bank selection. In the x36 organization, the memory is a single array that may be divided into four separate bytes. In the x18 organization, up to two banks, each with two separate bytes, may be independently selected. One bank is activated by each $\overline{RAS}$ selection; the others not selected remain in standby mode, drawing minimum power.

PIN ASSIGNMENT (End View)
88-Pin Card (U-1)





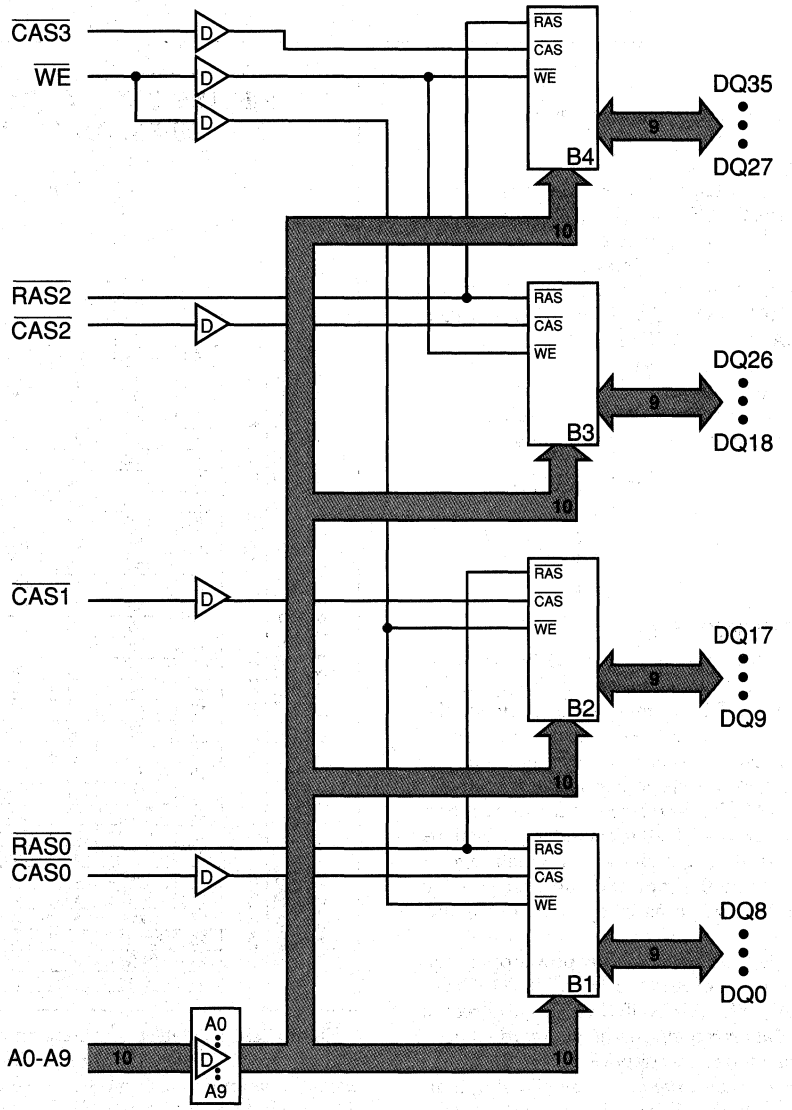
PIN #	SYMBOL	PIN #	SYMBOL	PIN #	SYMBOL
1	Vss	31	NC	61	A9
2	DQ0	32	NC	62	NC
3	DQ1	33	DQ17	63	Vss
4	DQ2	34	DQ9	64	NC
5	DQ3	35	NC	65	NC
6	DQ4	36	DQ10	66	$\overline{CAS2}$
7	DQ5	37	Vcc	67	Vss
8	DQ6	38	DQ11	68	$\overline{CAS3}$
9	Vcc	39	DQ12	69	NC
10	DQ7	40	DQ13	70	$\overline{WE}$
11	NC	41	DQ14	71	PD1 (Vss)
12	DQ8	42	DQ15	72	PD3 (Vss)
13	A0	43	DQ16	73	Vss
14	A2	44	Vss	74	PD5 (NC)
15	Vcc	45	Vss	75	PD7 (TBD)
16	A4	46	DQ18	76	PD8 (NC)
17	NC	47	DQ19	77	NC
18	A6	48	DQ20	78	NC
19	A8	49	DQ21	79	DQ35
20	NC	50	DQ22	80	DQ27
21	NC	51	DQ23	81	DQ28
22	$\overline{RAS0}$	52	DQ24	82	DQ29
23	$\overline{CAS0}$	53	DQ25	83	DQ30
24	$\overline{CAS1}$	54	DQ26	84	DQ31
25	NC	55	NC	85	DQ32
26	$\overline{RAS2}$	56	Vss	86	DQ33
27	Vcc	57	A1	87	DQ34
28	PD2 (NC)	58	A3	88	Vss
29	PD4 (Vss)	59	A5		
30	PD6 (TBD)	60	A7		

Eight presence detect pins may be read by the host to identify the MT12D88C136 organization, number of banks, access time and refresh mode. These extensive presence detect functions allow systems to utilize the advanced power-saving features.

The MT12D88C136 is built with a plastic frame covered by stainless steel panels. This package, containing an 88-pin receptacle connector, is keyed to prevent improper installation or insertion into other types of IC card sockets.

NEW ■ IC DRAM CARD

FUNCTIONAL BLOCK DIAGRAM



NOTE: 1. D = 74AC11244 line drivers.
2. B1 through B4 = 1 Meg x 9 memory blocks.

PIN DESCRIPTIONS

PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
22, 26	$\overline{RAS0}$, $\overline{RAS2}$	Input	Row Address Strobe: $\overline{RAS}$ is used to clock-in the 10 row-address bits. Two $\overline{RAS}$ inputs allow for a single x36 bank or two x18 banks.
23, 24, 66, 68	$\overline{CAS}$0-3	Input	Column Address Strobe: $\overline{CAS}$ is used to clock-in the 10 column-address bits, enable the DRAM output buffers, and strobe the data inputs on WRITE cycles. Four $\overline{CAS}$ inputs allow byte access control for any memory bank configuration.
70	$\overline{WE}$	Input	Write Enable: $\overline{WE}$ is the READ/WRITE control for the DQ pins. If $\overline{WE}$ is LOW prior to $\overline{CAS}$ going LOW, the access is a WRITE cycle. If $\overline{WE}$ is HIGH while $\overline{CAS}$ is LOW, the access is a READ cycle.
13, 57, 14, 58, 16, 59, 18, 60, 19, 61	A0-A9	Input	Address Inputs: These inputs are multiplexed and clocked by $\overline{RAS}$ and $\overline{CAS}$.
2-8, 10, 12, 34, 36, 38-43, 33, 46-54, 80-87, 79	DQ0-DQ35	Input/ Output	Data I/O: For WRITE cycles, DQ0-DQ35 act as inputs to the addressed DRAM location. BYTE WRITEs may be performed by using the corresponding $\overline{CAS}$ select. For READ access cycles, DQ0-DQ35 act as outputs for the addressed DRAM location.
71, 28, 72, 29, 74, 30, 75, 76	PD1-PD8	-	Presence Detect: These pins are read by the host system and tell the system the card's personality. They will be either left floating (NC) or they will be grounded (Vss).
11, 17, 20, 21, 25, 31, 32, 35, 62, 55, 64, 77, 78, 65, 69	NC	-	No Connect: These pins should be left unconnected (reserved for future use).
9, 15, 27, 37	Vcc	Supply	Power Supply: +5V ±5%
1, 44, 45, 56, 63, 67, 73, 88	Vss	Supply	Ground

FUNCTIONAL DESCRIPTION

The MT12D88C136 is a 4 megabyte memory card as a 1 Meg x 36 bit memory array ($\overline{RAS0}$ = $\overline{RAS2}$). It also may be configured as a 2 Meg x 18 bit memory array provided the corresponding DQs on the host are connected and memory bank control procedures are implemented by interleaving both $\overline{RAS}$ lines.

Most x36 bit applications use the same signal to control the $\overline{CAS}$ inputs. $\overline{RAS0}$ controls the lower 18 bits and $\overline{RAS2}$ controls the upper 18 bits to obtain a x36 memory array. For x18 applications, the corresponding DQs and the corresponding $\overline{CAS}$ pins must be connected together (DQ0 to DQ18, DQ1 to DQ19 and so forth, and $\overline{CAS0}$ to $\overline{CAS2}$ and $\overline{CAS1}$ to $\overline{CAS3}$). Each $\overline{RAS}$ is then a bank select for the 2 Meg x 18 memory organization.

DRAM OPERATION

DRAM REFRESH

Memory cell data is retained in its correct state by maintaining power and executing any $\overline{RAS}$ cycle [READ, WRITE, $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$ (CBR), HIDDEN or BATTERY BACKUP (BBU) REFRESH] so that all 1,024 combinations of $\overline{RAS}$ addresses (A0-A9) are executed at least every 128ms, regardless of sequence.

The implied method of choice for refreshing the memory card is the BBU cycle. This is a very low current, data retention mode made possible by using the CBR REFRESH cycle over the extended refresh range (I_{CC7}).

The memory card may be used with the other refresh modes common in standard DRAMs. This allows the memory card to be used on existing systems that do not utilize the BBU REFRESH cycle. However, the penalty is the memory card will draw more current in the STANDBY mode. The CBR REFRESH mode is recommended when not using the BBU mode.

DRAM READ AND WRITE CYCLES

During READ or WRITE cycles, each bit is uniquely addressed through the 20 address bits, which are entered 10 bits (A0-A9) at a time. $\overline{RAS}$ is used to latch the first 10 bits and $\overline{CAS}$ the latter 10 bits. READ or WRITE cycles are selected with the $\overline{WE}$ input. A logic HIGH on $\overline{WE}$ dictates READ mode while a logic LOW on $\overline{WE}$ dictates WRITE mode. During a WRITE cycle, data in (D) is latched by the falling edge of $\overline{CAS}$. $\overline{WE}$ must fall prior to $\overline{CAS}$ (EARLY WRITE); if $\overline{WE}$ goes LOW after $\overline{CAS}$, the outputs (Q) will be activated and will drive invalid data to the inputs. The data inputs and data outputs are routed through pins using common I/O, and pin direction is controlled by $\overline{WE}$.

FAST PAGE MODE operation allows faster data operations (READ or WRITE) within a row address (A0-A9) defined page boundary. The FAST PAGE MODE cycle is always initiated with a row address strobed-in by $\overline{RAS}$ followed by a column address strobed-in by $\overline{CAS}$. $\overline{CAS}$ may be toggled-in by holding $\overline{RAS}$ LOW and strobing-in different column addresses, thus executing faster memory cycles. Returning $\overline{RAS}$ HIGH terminates the FAST PAGE MODE operation. Returning $\overline{RAS}$ and $\overline{CAS}$ HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the $\overline{RAS}$ high time.

DRAM TIMING

In accordance with JEDEC standard specifications, all inputs to the IC DRAM card are buffered, with the exception of $\overline{RAS}$ inputs. The line drivers used for buffers reduce reflections on the card and ensure compatibility in a wide range of systems. The implementation of buffers on the card may relieve the need for additional host system line drivers. Notes 23 though 29 indicate which parameters on the IC DRAM card are affected by the line drivers, and to what magnitude they are affected. The component DRAM timing specifications, rather than those of the IC DRAM card (in systems that use both), may cause timing incompatibilities.

All traces on the IC DRAM card (buffered and non-buffered) are approximately 50 ohms characteristic impedance. Matching impedance on the system board to 50 ohms characteristic impedance on traces to the IC DRAM card will decrease signal noise to the IC DRAM card, enhancing overall system reliability.

PHYSICAL DESIGN

The MT12D88C136 is constructed with a molded plastic frame and covered with stainless steel panels. Inside, 12 thin small-outline package (TSOP) DRAMs are mounted on an ultrathin printed circuit board. The board is attached to a high insertion, 88-pin receptacle connector. The package has a polarized key to prevent improper installation, including insertion into other types of IC card sockets. The MT12D88C136 operates reliably up to 55°C.

MEMORY TRUTH TABLE

FUNCTION		RAS	CAS	WE	ADDRESSES tR	ADDRESSES tC	DATA IN/OUT DQ0-DQ35
Standby		H	H→X	X	X	X	High-Z
READ		L	L	H	ROW	COL	Data Out
EARLY-WRITE		L	L	L	ROW	COL	Data In
READ-WRITE		L	L	H→L	ROW	COL	Data In
FAST-PAGE-MODE	1st Cycle	L	H→L	H	ROW	COL	Data Out
READ	2nd Cycle	L	H→L	H	n/a	COL	Data Out
FAST-PAGE-MODE	1st Cycle	L	H→L	L	ROW	COL	Data In
EARLY-WRITE	2nd Cycle	L	H→L	L	n/a	COL	Data In
FAST-PAGE-MODE	1st Cycle	L	H→L	H→L	ROW	COL	Data Out
READ-WRITE	2nd Cycle	L	H→L	H→L	n/a	COL	Data Out
RAS-ONLY REFRESH		H	X	X	ROW	n/a	High-Z
HIDDEN	READ	L→H→L	L	H	ROW	COL	Data Out
REFRESH	WRITE	L→H→L	L	L	ROW	COL	Data In
CAS-BEFORE-RAS REFRESH		H→L	L	H	X	X	High-Z
BATTERY BACKUP REFRESH		H→L	L	H	X	X	High-Z

PRESENCE DETECT TRUTH TABLE

CHARACTERISTICS						PRESENT DETECT PIN (PDx)							
Card Density	DRAM Organizations	Card Address	RAS Address	CAS Address	Page Depth	1	2	3	4	5	6	7	8
0MB	No card installed	X	X	X	X	NC	NC	NC	NC	NC	X	X	X
1MB	256K x 1, 4, 16, 18	18	9	9	512	Vss	Vss	Vss	Vss	NC	X	X	X
2MB	256K x 1, 4, 16, 18	18	9	9	512	Vss	Vss	Vss	Vss	Vss	X	X	X
2MB	512K x 8, 9	19	10	9	512	NC	Vss	Vss	Vss	NC	X	X	X
4MB	512K x 8, 9	19	10	9	512	NC	Vss	Vss	Vss	Vss	X	X	X
• 4MB	1 Meg x 1, 4, 16, 18	20	10	10	1,024	Vss	NC	Vss	Vss	NC	X	X	X
8MB	1 Meg x 1, 4, 16, 18	20	10	10	1,024	Vss	NC	Vss	Vss	Vss	X	X	X
8MB	2 Meg x 8, 9	21	11	10	1,024	NC	NC	Vss	Vss	NC	X	X	X
16MB	2 Meg x 8, 9	21	11	10	1,024	NC	NC	Vss	Vss	Vss	X	X	X
16MB	4 Meg x 1, 4, 16, 18	22	12	11	1,024	Vss	Vss	NC	Vss	NC	X	X	X
32MB	4 Meg x 1, 4, 16, 18	22	12	11	1,024	Vss	Vss	NC	Vss	Vss	X	X	X
Access Timing		100ns				X	X	X	X	X	Vss	Vss	X
		80ns				X	X	X	X	X	NC	Vss	X
		70ns				X	X	X	X	X	Vss	NC	X
		60ns				X	X	X	X	X	NC	NC	X
		50ns				X	X	X	X	X	Vss	Vss	X
Refresh Control		Standard				X	X	X	X	X	X	X	NC
		Auto				X	X	X	X	X	X	X	Vss

NOTE: Vss = Ground.

NEW ■ IC DRAM CARD

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} ..... -0.5V to +5.25V
Operating Temperature T_A (Ambient) ..... 0°C to 55°C
Storage Temperature ..... -20°C to +80°C
Power Dissipation 15W
Short Circuit Output Current 50mA
Card Insertions (Connector's Life Cycle) 10,000

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 3, 4, 6, 7) (0°C ≤ T_A ≤ 55°C; V_{CC} = 5V ±5%)

PARAMETER/CONDITION		SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage		V_{CC}	4.75	5.25	V	1
Input High (Logic 1) Voltage, All Inputs		V_{IH}	3.5	V_{CC}+0.5	V	1
Input Low (Logic 0) Voltage, All Inputs		V_{IL}	-0.5	0.8	V	1
INPUT LEAKAGE CURRENT, Any input	Non-buffered	I_{IN}	-12	12	µA	
(0V ≤ V_{IN} ≤ 5.25V; all other pins not under test = 0V)	Buffered	I_{IB}	-2	2	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled; 0V ≤ V_{OUT} ≤ 5.25V)		I_{OZ}	-10	10	µA	
OUTPUT LEVELS Output High Voltage (I_{OUT} = -5mA)		V_{OH}	2.4		V	
Output Low Voltage (I_{OUT} = 4.2mA)		V_{OL}		0.4	V	

		MAX				
PARAMETER/CONDITION	SYMBOL	-6	-7	-8	UNITS	NOTES
STANDBY CURRENT: (TTL) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC1}	24	24	24	mA	
STANDBY CURRENT: (CMOS) ($\overline{RAS}$ = $\overline{CAS}$ = Other Inputs = V_{CC} -0.2V)	I_{CC2}	2.4	2.4	2.4	mA	
OPERATING CURRENT: Random READ/WRITE Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC (MIN))	I_{CC3}	1.2	1.1	1.0	A	3, 4, 30
OPERATING CURRENT: FAST PAGE MODE Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: ^tPC = ^tPC (MIN))	I_{CC4}	900	750	625	mA	3, 4, 30
REFRESH CURRENT: $\overline{RAS}$-ONLY Average power supply current ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}: ^tRC = ^tRC (MIN))	I_{CC5}	1.2	1.1	1.0	A	3, 30
REFRESH CURRENT: $\overline{CAS}$-BEFORE-$\overline{RAS}$ (CBR) Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC (MIN))	I_{CC6}	1.2	1.1	1.0	A	3, 5, 30
REFRESH CURRENT: BATTERY BACKUP (BBU) Average power supply current during BBU: $\overline{CAS}$ = 0.2V or CBR cycling; $\overline{RAS}$ = ^tRAS (MIN) up to 300ns; ^tRC = 125µs; $\overline{WE}$, A0-A9 and DQ = V_{CC} -0.2V or 0.2V (DQ may be left open)	I_{CC7}	3.2	3.2	3.2	mA	3, 5

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: $\overline{CAS0}$, $\overline{CAS1}$, $\overline{CAS2}$, $\overline{CAS3}$, A0-A9	C_{I1}		9	pF	2
Input Capacitance: $\overline{WE}$	C_{I2}		13	pF	2
Input Capacitance: $\overline{RAS0}$, $\overline{RAS2}$	C_{I3}		50	pF	2
Input/Output Capacitance: DQ	C_{IO}		12	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13,) (0°C ≤ T_A ≤ 55°C; Vcc = 5V ±5%)

AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	^tRC	110		130		150		ns	23
FAST-PAGE-MODE READ or WRITE cycle time	^tPC	40		40		45		ns	23
Access time from $\overline{RAS}$	^tRAC		60		70		80	ns	14, 23
Access time from $\overline{CAS}$	^tCAC		25		30		30	ns	15, 26
Access time from column address	^tAA		40		45		50	ns	26
Access time from $\overline{CAS}$ precharge	^tCPA		50		50		55	ns	26
$\overline{RAS}$ pulse width	^tRAS	60	100,000	70	100,000	80	100,000	ns	23
$\overline{RAS}$ pulse width (FAST PAGE MODE)	^tRASP	60	100,000	70	100,000	80	100,000	ns	23
$\overline{RAS}$ hold time	^tRSH	25		30		30		ns	26
$\overline{RAS}$ precharge time	^tRP	45		50		60		ns	23
$\overline{CAS}$ pulse width	^tCAS	15	100,000	20	100,000	20	100,000	ns	23
$\overline{CAS}$ hold time	^tCSH	55		65		75		ns	25
$\overline{CAS}$ precharge time	^tCPN	10		10		10		ns	16, 23
$\overline{CAS}$ precharge time (FAST PAGE MODE)	^tCP	10		10		10		ns	23
$\overline{RAS}$ to $\overline{CAS}$ delay time	^tRCD	10	35	15	40	15	50	ns	17, 28
$\overline{CAS}$ to $\overline{RAS}$ precharge time	^tCRP	15		15		15		ns	26
Row address setup time	^tASR	10		10		10		ns	26
Row address hold time	^tRAH	5		5		5		ns	25
$\overline{RAS}$ to column address delay time	^tRAD	10	20	10	25	10	30	ns	18, 28
Column address setup time	^tASC	5		5		5		ns	24
Column address hold time	^tCAH	15		20		20		ns	24
Column address hold time (referenced to $\overline{RAS}$)	^tAR	45		50		55		ns	25
Column address to $\overline{RAS}$ lead time	^tRAL	40		45		50		ns	26
Read command setup time	^tRCS	5		5		5		ns	25
Read command hold time (referenced to $\overline{CAS}$)	^tRCH	5		5		5		ns	19, 24
Read command hold time (referenced to $\overline{RAS}$)	^tRRH	-5		-5		-5		ns	19, 25
$\overline{CAS}$ to output in Low-Z	^tCLZ	5		5		5		ns	24
Output buffer turn-off delay	^tOFF	5	30	5	30	5	30	ns	20, 29
$\overline{WE}$ command setup time	^tWCS	5		5		5		ns	24

NEW ■ IC DRAM CARD

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

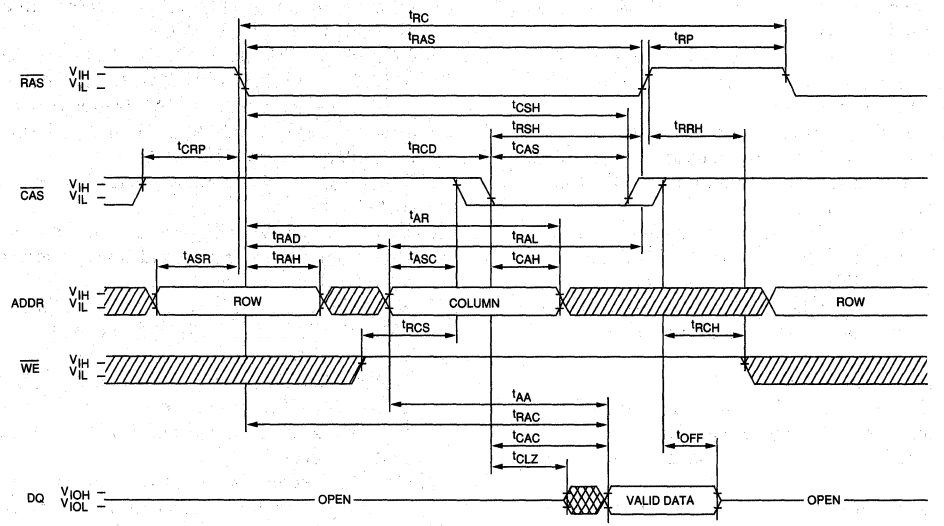
(Notes: 6, 7, 8, 9, 10, 11, 12, 13) ($0°C \le T_A \le 55°C$; V_{CC} = 5V ±5%)

AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Write command hold time	tWCH	15		20		20		ns	24
Write command hold time (referenced to $\overline{RAS}$)	tWCR	40		50		55		ns	25
Write command pulse width	tWP	10		15		15		ns	23
Write command to $\overline{RAS}$ lead time	tRWL	25		30		30		ns	26
Write command to $\overline{CAS}$ lead time	tCWL	20		25		25		ns	24
Data-in setup time	tDS	5		5		5		ns	24
Data-in hold time	tDH	5		10		10		ns	25
Data-in hold time (referenced to $\overline{RAS}$)	tDHR	45		55		60		ns	23
Transition time (rise or fall)	tT	2	15	2	15	2	15	ns	9, 10, 23
Refresh period (1,024 cycles)	tREF		128		128		128	ms	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	tRPC	10		10		10		ns	26
$\overline{CAS}$ setup time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	tCSR	20		20		20		ns	5, 26
$\overline{CAS}$ hold time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	tCHR	10		10		10		ns	5, 25
$\overline{WE}$ hold time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	tWRH	5		5		5		ns	22, 25
$\overline{WE}$ setup time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	tWRP	20		20		20		ns	22, 26
$\overline{WE}$ hold time (WCBR test cycle)	tWTH	5		5		5		ns	22, 25
$\overline{WE}$ setup time	tWTS	20		20		20		ns	22, 26

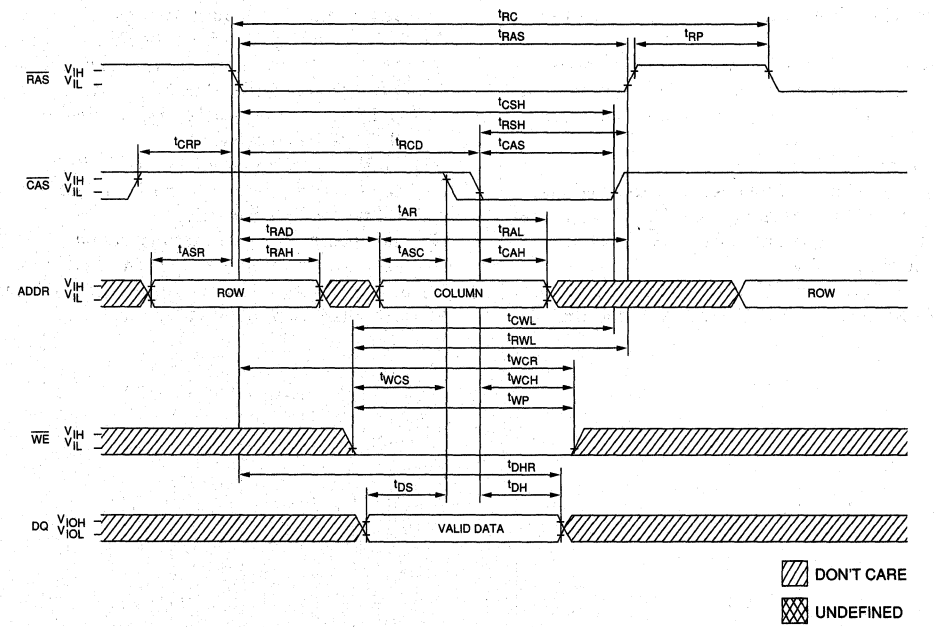
NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. V_{CC} = 5V ±10%, f = 1 MHz.
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is assured.
7. An initial pause of 100µs is required after power-up followed by eight $\overline{RAS}$ refresh cycles ($\overline{RAS}$-ONLY or CBR with $\overline{WE}$ HIGH) before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-up should be repeated any time the ^{t}REF refresh requirement is exceeded.
8. AC characteristics assume ^{t}T = 5ns.
9. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS}$ = V_{IH}, data output is high impedance.
12. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to 2 TTL gates and 100pF.
14. Assumes that $^{t}RCD < {}^{t}RCD$ (MAX). If ^{t}RCD is greater than the maximum recommended value shown in this table, ^{t}RAC will increase by the amount that ^{t}RCD exceeds the value shown.
15. Assumes that $^{t}RCD \geq {}^{t}RCD$ (MAX).
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer, $\overline{CAS}$ must be pulsed HIGH for ^{t}CPN.
17. Operation within the ^{t}RCD (MAX) limit ensures that ^{t}RAC (MAX) can be met. ^{t}RCD (MAX) is specified as a reference point only; if ^{t}RCD is greater than the specified ^{t}RCD (MAX) limit, then access time is controlled exclusively by ^{t}CAC.
18. Operation within the ^{t}RAD (MAX) limit ensures that ^{t}RCD (MAX) can be met. ^{t}RAD (MAX) is specified as a reference point only; if ^{t}RAD is greater than the specified ^{t}RAD (MAX) limit, then access time is controlled exclusively by ^{t}AA.
19. Either ^{t}RCH or ^{t}RRH must be satisfied for a READ cycle.
20. ^{t}OFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
21. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW.
22. ^{t}WTS and ^{t}WTH are setup and hold specifications for the $\overline{WE}$ pin being held LOW to enable the JEDEC test mode (with CBR timing constraints). These two parameters are the inverse of ^{t}WRP and ^{t}WRH in the CBR refresh cycle.
23. Timing between the DRAMs and the DRAM card did not change with the addition of the line drivers.
24. A +5ns timing skew from the DRAM to the DRAM card resulted from the addition of line drivers.
25. A -5ns timing skew from the DRAM to the DRAM card resulted from the addition of line drivers.
26. A +10ns timing skew from the DRAM to the DRAM card resulted from the addition of line drivers.
27. A -10ns timing skew from the DRAM to the DRAM card resulted from the addition of line drivers.
28. A -5ns (MIN) and a -10ns (MAX) timing skew from the DRAM to the DRAM card resulted from the addition of line drivers.
29. A +5ns (MIN) and a +10ns (MAX) timing skew from the DRAM to the DRAM card resulted from the addition of line drivers.
30. The maximum current ratings are based with the memory operating or being refreshed in the x36 mode. The stated maximums may be reduced by one half when used in the x18 mode.

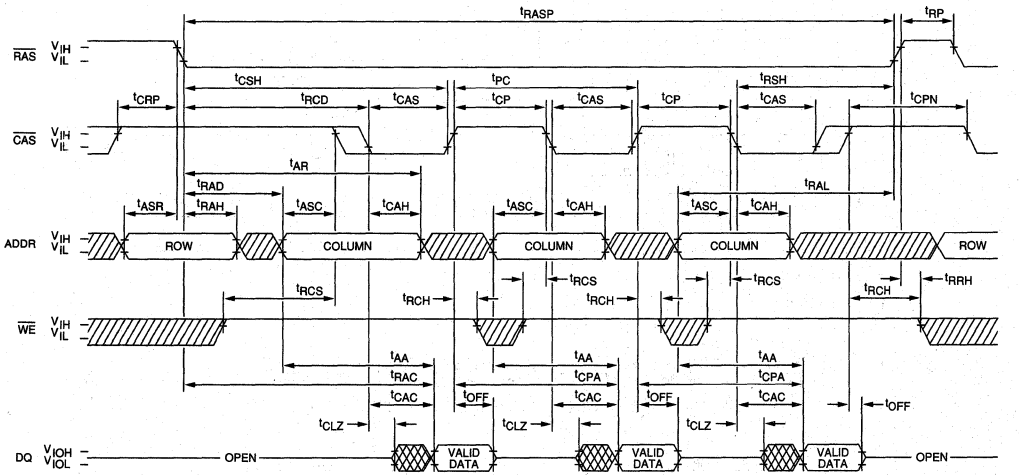
READ CYCLE



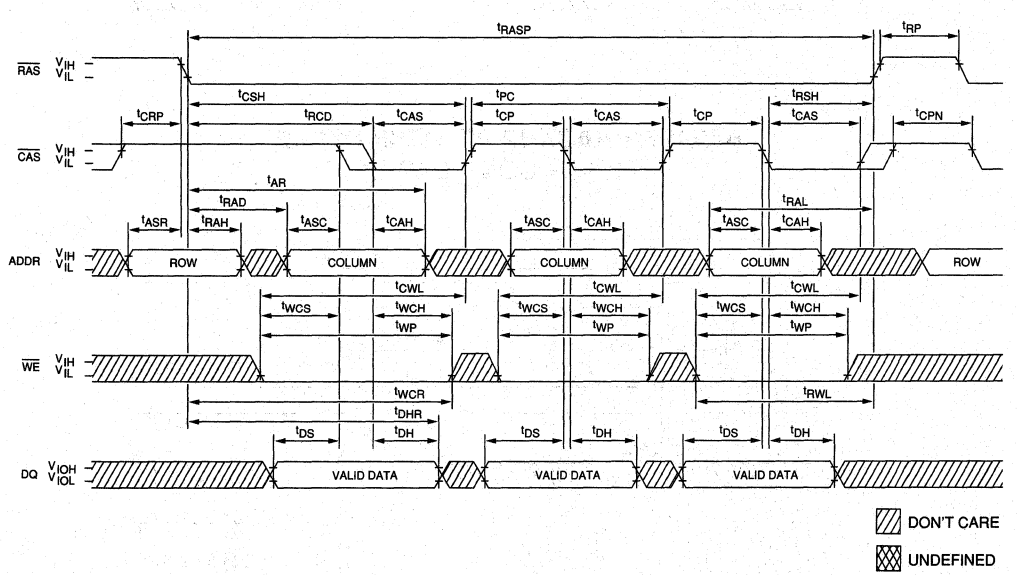
EARLY-WRITE CYCLE



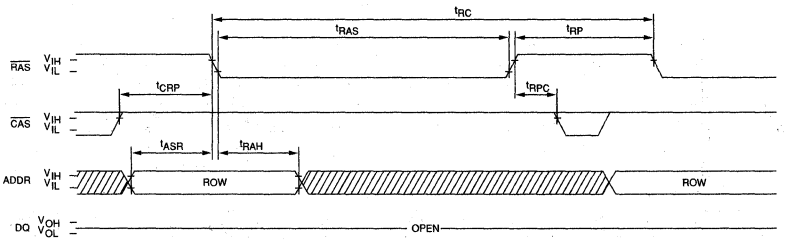
FAST-PAGE-MODE READ CYCLE



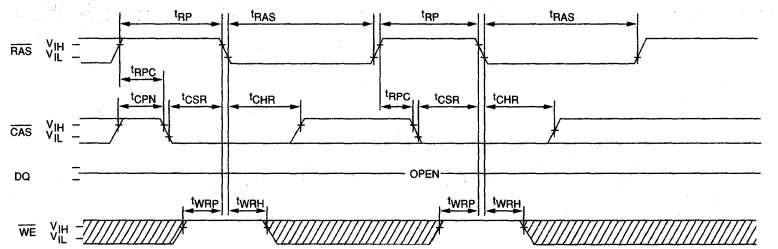
FAST-PAGE-MODE EARLY-WRITE CYCLE



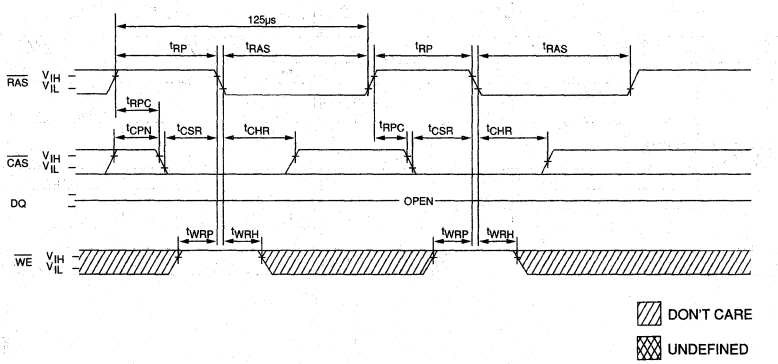
RAS-ONLY REFRESH CYCLE
(ADDR = A0-A9; WE = DON'T CARE)



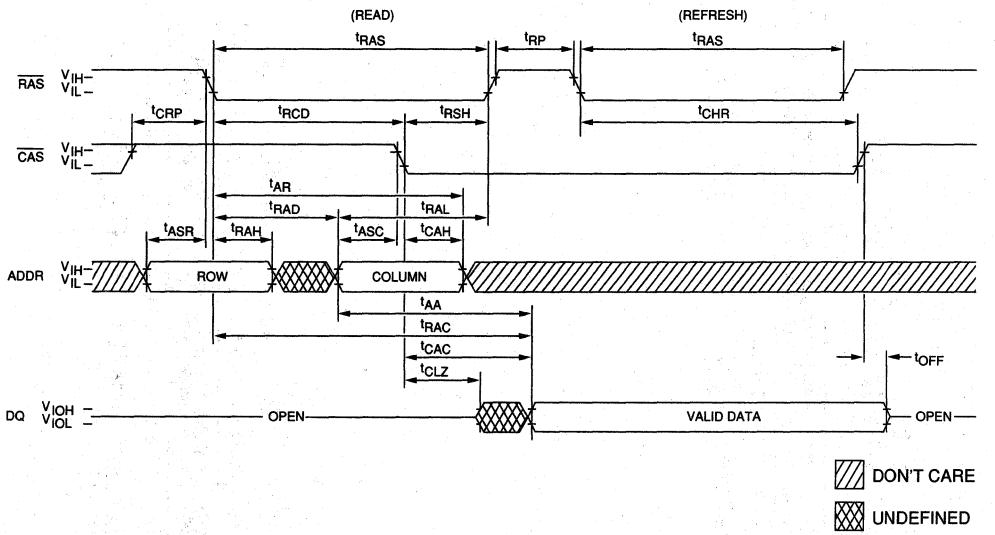
CAS-BEFORE-RAS REFRESH CYCLE
(A0-A9 = DON'T CARE)



BATTERY BACKUP REFRESH CYCLE
(A0-A9 = DON'T CARE)



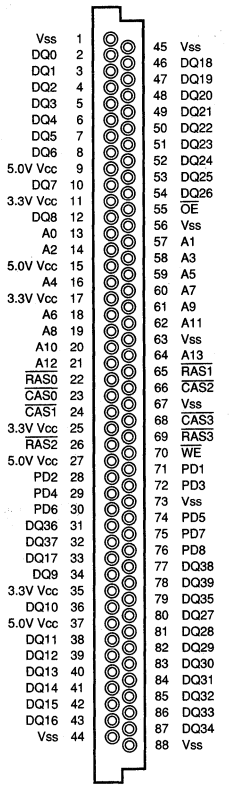
HIDDEN REFRESH CYCLE [21]
($\overline{WE}$ = HIGH)



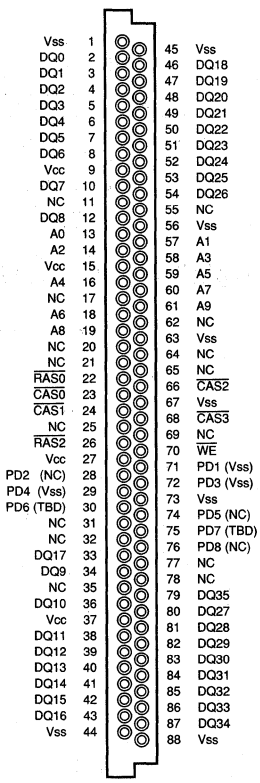
NEW IC DRAM CARD

NEW ■ IC DRAM CARD

RESERVED JEDEC, JEIDA and PCMCIA 88-PIN ASSIGNMENT
(All Possible Combinations)



MT12D88C136 PIN ASSIGNMENT
(JEDEC Standard)



IC DRAM CARD

8 MEGABYTES

2 MEG x 36, 4 MEG x 18

NEW ■ IC DRAM CARD

FEATURES

- JEIDA, JEDEC and PCMCIA standard 88-pin IC DRAM card
- Polarized receptacle connector
- Industry standard DRAM functions and timing
- High-performance, CMOS silicon-gate process
- All outputs are fully TTL compatible
- All inputs buffered except $\overline{RAS}$ inputs
- Multiple $\overline{RAS}$ inputs for x18 or x36 selectability
- Refresh modes: $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$ (CBR), HIDDEN and BATTERY BACKUP (BBU)
- FAST PAGE MODE access cycle
- Single +5V ±5% power supply
- Low power; 24mW standby, 3.1W active (typical)
- Extended refresh standard: 1,024 cycles every 128ms

OPTIONS — MARKING

- Timing

60ns access	-6
70ns access	-7
80ns access	-8

GENERAL DESCRIPTION

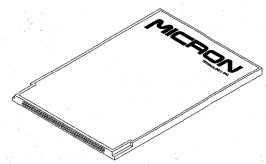
The MT24D88C236 is an 8 megabyte, IC DRAM card organized as a 2 Meg x 36 bit memory array. It may also be configured as a 4 Meg x 18 bit memory array, provided the corresponding DQs on the host system are made common and memory bank control procedures are implemented. Separate $\overline{CAS}$ inputs allow byte accesses.

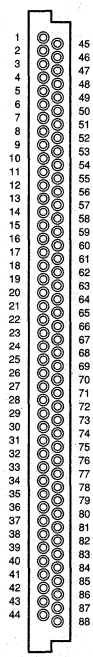
All inputs to the DRAMs are buffered, with the exception of $\overline{RAS}$. The line drivers used for buffers reduce reflections on the card and ensure compatibility in a wide range of systems. At the same time, the line drivers add delays to the buffered input timings when compared to standard DRAMs.

The MT24D88C236 is designed for low power operation using 1 Meg x 4 low power, extended refresh DRAMs. These devices support BATTERY BACKUP (BBU) cycle refresh; a very low current, data retention mode. Standard component DRAM refresh modes are supported as well.

Multiple $\overline{RAS}$ inputs conserve power by allowing individual bank selection. In the x36 organization, the memory array may be divided into two banks, each with four separate bytes. In the x18 organization, up to four banks, each with two separate bytes, may be independently selected. One bank is activated by each $\overline{RAS}$ selection; the others not selected remain in standby mode, drawing minimum power.

PIN ASSIGNMENT (End View)
88-Pin Card (U-1)



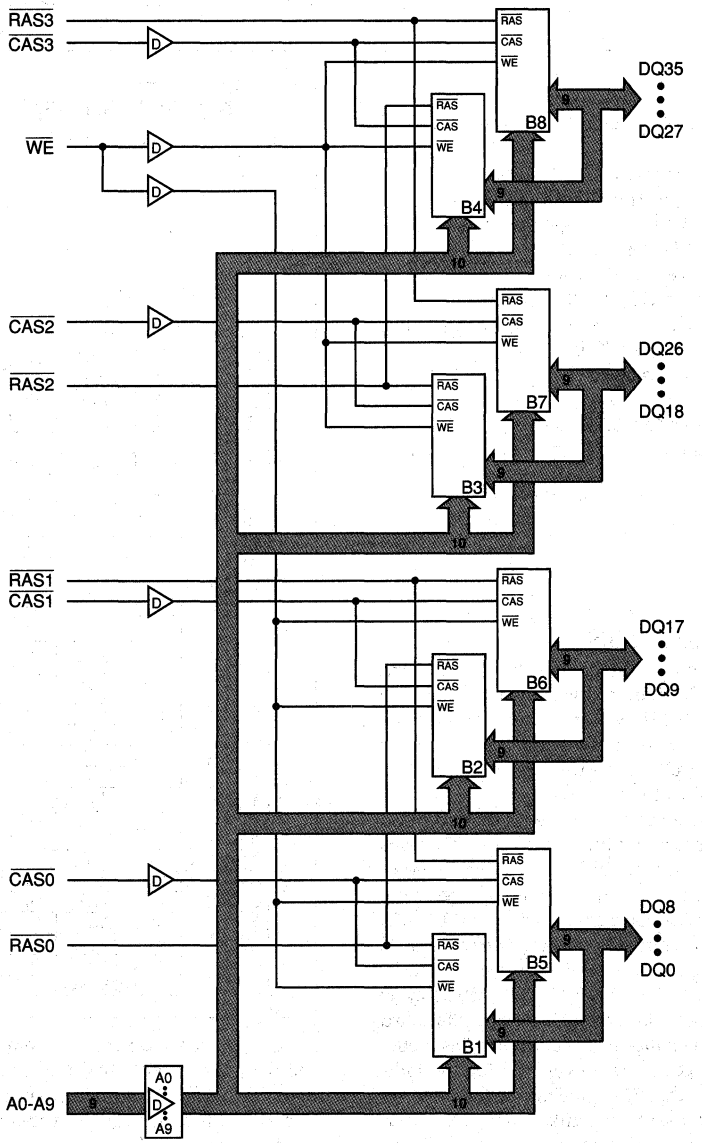


PIN #	SYMBOL	PIN #	SYMBOL	PIN #	SYMBOL
1	Vss	31	NC	61	A9
2	DQ0	32	NC	62	NC
3	DQ1	33	DQ17	63	Vss
4	DQ2	34	DQ9	64	NC
5	DQ3	35	NC	65	$\overline{RAS1}$
6	DQ4	36	DQ10	66	$\overline{CAS2}$
7	DQ5	37	Vcc	67	Vss
8	DQ6	38	DQ11	68	$\overline{CAS3}$
9	Vcc	39	DQ12	69	$\overline{RAS3}$
10	DQ7	40	DQ13	70	$\overline{WE}$
11	NC	41	DQ14	71	PD1 (Vss)
12	DQ8	42	DQ15	72	PD3 (Vss)
13	A0	43	DQ16	73	Vss
14	A2	44	Vss	74	PD5 (Vss)
15	Vcc	45	Vss	75	PD7 (TBD)
16	A4	46	DQ18	76	PD8 (NC)
17	NC	47	DQ19	77	NC
18	A6	48	DQ20	78	NC
19	A8	49	DQ21	79	DQ35
20	NC	50	DQ22	80	DQ27
21	NC	51	DQ23	81	DQ28
22	$\overline{RAS0}$	52	DQ24	82	DQ29
23	$\overline{CAS0}$	53	DQ25	83	DQ30
24	$\overline{CAS1}$	54	DQ26	84	DQ31
25	NC	55	NC	85	DQ32
26	$\overline{RAS2}$	56	Vss	86	DQ33
27	Vcc	57	A1	87	DQ34
28	PD2 (NC)	58	A3	88	Vss
29	PD4 (Vss)	59	A5		
30	PD6 (TBD)	60	A7		

Eight presence detect pins may be read by the host to identify the MT24D88C236 organization, number of banks, access time and refresh mode. These extensive presence detect functions allow systems to utilize the advanced power-saving features.

The MT24D88C236 is built with a plastic frame covered by stainless steel panels. This package, containing an 88-pin receptacle connector, is keyed to prevent improper installation or insertion into other types of IC card sockets.

FUNCTIONAL BLOCK DIAGRAM



NOTE: 1. D = 74AC11244 line drivers.
2. B1 through B8 = 1 Meg x 9 memory blocks.

PIN DESCRIPTIONS

PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
22, 26, 65, 69	$\overline{RAS}$0-3	Input	Row Address Strobe: $\overline{RAS}$ is used to clock-in the 10 row-address bits. Four $\overline{RAS}$ inputs allow for two x36 banks or four x18 banks.
23, 24, 66, 68	$\overline{CAS}$0-3	Input	Column Address Strobe: $\overline{CAS}$ is used to clock-in the 10 column-address bits, enable the DRAM output buffers, and strobe the data inputs on WRITE cycles. Four $\overline{CAS}$ inputs allow byte access control for any memory bank configuration.
70	$\overline{WE}$	Input	Write Enable: $\overline{WE}$ is the READ/WRITE control for the DQ pins. If $\overline{WE}$ is LOW prior to $\overline{CAS}$ going LOW, the access is a WRITE cycle. If $\overline{WE}$ is HIGH while $\overline{CAS}$ is LOW, the access is a READ cycle.
13, 57, 14, 58, 16, 59, 18, 60, 19, 61	A0-A9	Input	Address Inputs: These inputs are multiplexed and clocked by $\overline{RAS}$ and $\overline{CAS}$.
2-8, 10, 12, 34, 36, 38-43, 33, 46-54, 80-87, 79	DQ0-DQ35	Input/ Output	Data I/O: For WRITE cycles, DQ0-DQ35 act as inputs to the addressed DRAM location. BYTE WRITEs may be performed by using the corresponding $\overline{CAS}$ select. For READ access cycles, DQ0-DQ35 act as outputs for the addressed DRAM location.
71, 28, 72, 29, 74, 30, 75, 76	PD1-PD8	-	Presence Detect: These pins are read by the host system and tell the system the card's personality. They will be either left floating (NC) or they will be grounded (Vss).
11, 17, 20, 21, 25, 31, 32, 35, 62, 55, 64, 77, 78	NC	-	No Connect: These pins should be left unconnected (reserved for future use).
9, 15, 27, 37	Vcc	Supply	Power Supply: +5V ±5%
1, 44, 45, 56, 63, 67, 73, 88	Vss	Supply	Ground

FUNCTIONAL DESCRIPTION

The MT24D88C236 is an 8 megabyte memory card structured as a 2 Meg x 36 bit memory array ($\overline{RAS0}$ = $\overline{RAS2}$, $\overline{RAS1}$ = $\overline{RAS3}$). It also may be configured as a 4 Meg x 18 bit memory array provided the corresponding DQs on the host are connected and memory bank control procedures are implemented by interleaving all four $\overline{RAS}$ lines.

Most x36 bit applications use the same signal to control the $\overline{CAS}$ inputs. $\overline{RAS0}$ and $\overline{RAS1}$ control the lower 18 bits, and $\overline{RAS2}$ and $\overline{RAS3}$ control the upper 18 bits to obtain a x36 memory array. For x18 applications, the corresponding DQs and the corresponding $\overline{CAS}$ pins must be connected together (DQ0 to DQ18, DQ1 to DQ19 and so forth, and $\overline{CAS0}$ to $\overline{CAS2}$ and $\overline{CAS1}$ to $\overline{CAS3}$). Each $\overline{RAS}$ is then a bank select for the 4 Meg x 18 memory organization.

DRAM OPERATION

DRAM REFRESH

Memory cell data is retained in its correct state by maintaining power and executing any $\overline{RAS}$ cycle [READ, WRITE, $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$ (CBR), HIDDEN or BATTERY BACKUP (BBU) REFRESH] so that all 1,024 combinations of $\overline{RAS}$ addresses (A0-A9) are executed at least every 128ms, regardless of sequence.

The implied method of choice for refreshing the memory card is the BBU cycle. This is a very low current, data retention mode made possible by using the CBR REFRESH cycle over the extended refresh range (Icc7).

The memory card may be used with the other refresh modes common in standard DRAMs. This allows the memory card to be used on existing systems that do not utilize the BBU REFRESH cycle. However, the memory card will draw more current in the STANDBY mode. The CBR REFRESH mode is recommended when not using the BBU mode.

DRAM READ AND WRITE CYCLES

During READ or WRITE cycles, each bit is uniquely addressed through the 20 address bits, which are entered 10 bits (A0-A9) at a time. $\overline{RAS}$ is used to latch the first 10 bits and $\overline{CAS}$ the latter 10 bits. READ or WRITE cycles are selected with the $\overline{WE}$ input. A logic HIGH on $\overline{WE}$ dictates READ mode while a logic LOW on $\overline{WE}$ dictates WRITE mode. During a WRITE cycle, data in (D) is latched by the falling edge of $\overline{CAS}$. $\overline{WE}$ must fall prior to $\overline{CAS}$ (EARLY WRITE); if $\overline{WE}$ goes LOW after $\overline{CAS}$, the outputs (Q) will be activated and will drive invalid data to the inputs. The data inputs and data outputs are routed through pins using common I/O, and pin direction is controlled by $\overline{WE}$.

FAST PAGE MODE operation allows faster data operations (READ or WRITE) within a row address (A0-A9) defined page boundary. The FAST PAGE MODE cycle is always initiated with a row address strobed-in by $\overline{RAS}$ followed by a column address strobed-in by $\overline{CAS}$. $\overline{CAS}$ may be toggled-in by holding $\overline{RAS}$ LOW and strobing-in different column addresses, thus executing faster memory cycles. Returning $\overline{RAS}$ HIGH terminates the FAST PAGE MODE operation. Returning $\overline{RAS}$ and $\overline{CAS}$ HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the $\overline{RAS}$ high time.

DRAM TIMING

In accordance with JEDEC standard specifications, all inputs to the IC DRAM card are buffered, with the exception of $\overline{RAS}$ inputs. The line drivers used for buffers reduce reflections on the card and ensure compatibility in a wide range of systems. The implementation of buffers on the card may relieve the need for additional host system line drivers. Notes 23 though 29 indicate which parameters on the IC DRAM card are affected by the line drivers, and to what magnitude they are affected. The component DRAM timing specifications, rather than those of the IC DRAM card (in systems that use both), may cause timing incompatibilities.

All traces on the IC DRAM card (buffered and non-buffered) are approximately 50 ohms characteristic impedance. Matching impedance on the system board to 50 ohms characteristic impedance on traces to the IC DRAM card will decrease signal noise to the IC DRAM card, enhancing overall system reliability.

PHYSICAL DESIGN

The MT24D88C236 is constructed with a molded plastic frame and covered with stainless steel panels. Inside, 24 thin small-outline package (TSOP) DRAMs are mounted on both sides of an ultrathin printed circuit board. The board is attached to a high insertion, 88-pin receptacle connector. The package has a polarized key to prevent improper installation, including insertion into other types of IC card sockets. The MT24D88C236 operates reliably up to 55°C.

MEMORY TRUTH TABLE

FUNCTION		RAS	CAS	WE	ADDRESSES tR	ADDRESSES tC	DATA IN/OUT DQ0-DQ35
Standby		H	H→X	X	X	X	High-Z
READ		L	L	H	ROW	COL	Data Out
EARLY-WRITE		L	L	L	ROW	COL	Data In
READ-WRITE		L	L	H→L	ROW	COL	Data In
FAST-PAGE-MODE	1st Cycle	L	H→L	H	ROW	COL	Data Out
READ	2nd Cycle	L	H→L	H	n/a	COL	Data Out
FAST-PAGE-MODE	1st Cycle	L	H→L	L	ROW	COL	Data In
EARLY-WRITE	2nd Cycle	L	H→L	L	n/a	COL	Data In
FAST-PAGE-MODE	1st Cycle	L	H→L	H→L	ROW	COL	Data Out
READ-WRITE	2nd Cycle	L	H→L	H→L	n/a	COL	Data Out
RAS-ONLY REFRESH		H	X	X	ROW	n/a	High-Z
HIDDEN	READ	L→H→L	L	H	ROW	COL	Data Out
REFRESH	WRITE	L→H→L	L	L	ROW	COL	Data In
CAS-BEFORE-RAS REFRESH		H→L	L	H	X	X	High-Z
BATTERY BACKUP REFRESH		H→L	L	H	X	X	High-Z

PRESENCE DETECT TRUTH TABLE

CHARACTERISTICS						PRESENT DETECT PIN (PDx)							
Card Density	DRAM Organizations	Card Address	RAS Address	CAS Address	Page Depth	1	2	3	4	5	6	7	8
0MB	No card installed	X	X	X	X	NC	NC	NC	NC	NC	X	X	X
1MB	256K x 1, 4, 16, 18	18	9	9	512	Vss	Vss	Vss	Vss	NC	X	X	X
2MB	256K x 1, 4, 16, 18	18	9	9	512	Vss	Vss	Vss	Vss	Vss	X	X	X
2MB	512K x 8, 9	19	10	9	512	NC	Vss	Vss	Vss	NC	X	X	X
4MB	512K x 8, 9	19	10	9	512	NC	Vss	Vss	Vss	Vss	X	X	X
4MB	1 Meg x 1, 4, 16, 18	20	10	10	1,024	Vss	NC	Vss	Vss	NC	X	X	X
• 8MB	1 Meg x 1, 4, 16, 18	20	10	10	1,024	Vss	NC	Vss	Vss	Vss	X	X	X
8MB	2 Meg x 8, 9	21	11	10	1,024	NC	NC	Vss	Vss	NC	X	X	X
16MB	2 Meg x 8, 9	21	11	10	1,024	NC	NC	Vss	Vss	Vss	X	X	X
16MB	4 Meg x 1, 4, 16, 18	22	12	11	1,024	Vss	Vss	NC	Vss	NC	X	X	X
32MB	4 Meg x 1, 4, 16, 18	22	12	11	1,024	Vss	Vss	NC	Vss	Vss	X	X	X
Access Timing		100ns				X	X	X	X	X	Vss	Vss	X
		80ns				X	X	X	X	X	NC	Vss	X
		70ns				X	X	X	X	X	Vss	NC	X
		60ns				X	X	X	X	X	NC	NC	X
		50ns				X	X	X	X	X	Vss	Vss	X
Refresh Control		Standard				X	X	X	X	X	X	X	NC
		Auto				X	X	X	X	X	X	X	Vss

NOTE: Vss = Ground.

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} ..... -0.5V to +5.25V
Operating Temperature T_A (Ambient) ..... 0°C to 55°C
Storage Temperature ..... -20°C to +80°C
Power Dissipation 15W
Short Circuit Output Current 50mA
Card Insertions (Connector's Life Cycle) 10,000

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 3, 4, 6, 7) (0°C ≤ T_A ≤ 55°C; V_{CC} = 5V ±5%)

PARAMETER/CONDITION		SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage		V_{CC}	4.75	5.25	V	1
Input High (Logic 1) Voltage, All Inputs		V_{IH}	3.5	V_{CC}+0.5	V	1
Input Low (Logic 0) Voltage, All Inputs		V_{IL}	-0.5	0.8	V	1
INPUT LEAKAGE CURRENT, Any input	Non-buffered	I_{IN}	-12	12	µA	
(0V ≤ V_{IN} ≤ 5.25V; all other pins not under test = 0V)	Buffered	I_{IB}	-2	2	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled; 0V ≤ V_{OUT} ≤ 5.25V)		I_{OZ}	-10	10	µA	
OUTPUT LEVELS Output High Voltage (I_{OUT} = -5mA)		V_{OH}	2.4		V	
Output Low Voltage (I_{OUT} = 4.2mA)		V_{OL}		0.4	V	

		MAX				
PARAMETER/CONDITION	SYMBOL	-6	-7	-8	UNITS	NOTES
STANDBY CURRENT: (TTL) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC1}	48	48	48	mA	
STANDBY CURRENT: (CMOS) ($\overline{RAS}$ = $\overline{CAS}$ = Other Inputs = V_{CC} -0.2V)	I_{CC2}	4.8	4.8	4.8	mA	
OPERATING CURRENT: Random READ/WRITE Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC (MIN))	I_{CC3}	1.2	1.1	1.0	A	3, 4, 30
OPERATING CURRENT: FAST PAGE MODE Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: ^tPC = ^tPC (MIN))	I_{CC4}	860	740	620	mA	3, 4, 30
REFRESH CURRENT: $\overline{RAS}$-ONLY Average power supply current ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}: ^tRC = ^tRC (MIN))	I_{CC5}	1.2	1.1	1.0	A	3, 30
REFRESH CURRENT: $\overline{CAS}$-BEFORE-$\overline{RAS}$ (CBR) Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC (MIN))	I_{CC6}	1.2	1.1	1.0	A	3, 5, 30
REFRESH CURRENT: BATTERY BACKUP (BBU) Average power supply current during BBU: $\overline{CAS}$ = 0.2V or CBR cycling; $\overline{RAS}$ = ^tRAS (MIN) up to 300ns; ^tRC = 125µs; $\overline{WE}$, A0-A9 and DQ = V_{CC} -0.2V or 0.2V (DQ may be left open)	I_{CC7}	6.4	6.4	6.4	mA	3, 5

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: $\overline{CAS0}$, $\overline{CAS1}$, $\overline{CAS2}$, $\overline{CAS3}$, A0-A9	C_{I1}		9	pF	2
Input Capacitance: $\overline{WE}$	C_{I2}		13	pF	2
Input Capacitance: $\overline{RAS0}$, $\overline{RAS1}$, $\overline{RAS2}$, $\overline{RAS3}$	C_{I3}		50	pF	2
Input/Output Capacitance: DQ	C_{IO}		24	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C ≤ T_A ≤ 55°C; Vcc = 5V ±5%)

AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	^tRC	110		130		150		ns	23
FAST-PAGE-MODE READ or WRITE cycle time	^tPC	40		40		45		ns	23
Access time from $\overline{RAS}$	^tRAC		60		70		80	ns	14, 23
Access time from $\overline{CAS}$	^tCAC		25		30		30	ns	15, 26
Access time from column address	^tAA		40		45		50	ns	26
Access time from $\overline{CAS}$ precharge	^tCPA		50		50		55	ns	26
$\overline{RAS}$ pulse width	^tRAS	60	100,000	70	100,000	80	100,000	ns	23
$\overline{RAS}$ pulse width (FAST PAGE MODE)	^tRASP	60	100,000	70	100,000	80	100,000	ns	23
$\overline{RAS}$ hold time	^tRSH	25		30		30		ns	26
$\overline{RAS}$ precharge time	^tRP	45		50		60		ns	23
$\overline{CAS}$ pulse width	^tCAS	15	100,000	20	100,000	20	100,000	ns	23
$\overline{CAS}$ hold time	^tCSH	55		65		75		ns	25
$\overline{CAS}$ precharge time	^tCPN	10		10		10		ns	16, 23
$\overline{CAS}$ precharge time (FAST PAGE MODE)	^tCP	10		10		10		ns	23
$\overline{RAS}$ to $\overline{CAS}$ delay time	^tRCD	10	35	15	40	15	50	ns	17, 28
$\overline{CAS}$ to $\overline{RAS}$ precharge time	^tCRP	15		15		15		ns	26
Row address setup time	^tASR	10		10		10		ns	26
Row address hold time	^tRAH	5		5		5		ns	25
$\overline{RAS}$ to column address delay time	^tRAD	10	20	10	25	10	30	ns	18, 28
Column address setup time	^tASC	5		5		5		ns	24
Column address hold time	^tCAH	15		20		20		ns	24
Column address hold time (referenced to $\overline{RAS}$)	^tAR	45		50		55		ns	25
Column address to $\overline{RAS}$ lead time	^tRAL	40		45		50		ns	26
Read command setup time	^tRCS	5		5		5		ns	25
Read command hold time (referenced to $\overline{CAS}$)	^tRCH	5		5		5		ns	19, 24
Read command hold time (referenced to $\overline{RAS}$)	^tRRH	-5		-5		-5		ns	19, 25
$\overline{CAS}$ to output in Low-Z	^tCLZ	5		5		5		ns	24
Output buffer turn-off delay	^tOFF	5	30	5	30	5	30	ns	20, 29
$\overline{WE}$ command setup time	^tWCS	5		5		5		ns	24

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

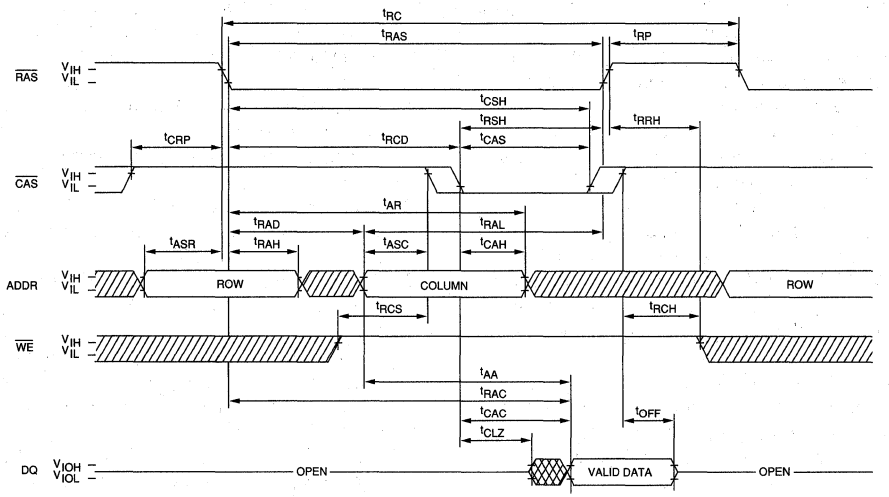
(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C ≤ T_A ≤ 55°C; Vcc = 5V ±5%)

AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Write command hold time	tWCH	15		20		20		ns	24
Write command hold time (referenced to $\overline{RAS}$)	tWCR	40		50		55		ns	25
Write command pulse width	tWP	10		15		15		ns	23
Write command to $\overline{RAS}$ lead time	tRWL	25		30		30		ns	26
Write command to $\overline{CAS}$ lead time	tCWL	20		25		25		ns	24
Data-in setup time	tDS	5		5		5		ns	24
Data-in hold time	tDH	5		10		10		ns	25
Data-in hold time (referenced to $\overline{RAS}$)	tDHR	45		55		60		ns	23
Transition time (rise or fall)	tT	2	15	2	15	2	15	ns	9, 10, 23
Refresh period (1,024 cycles)	tREF		128		128		128	ms	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	tRPC	10		10		10		ns	26
$\overline{CAS}$ setup time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	tCSR	20		20		20		ns	5, 26
$\overline{CAS}$ hold time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	tCHR	10		10		10		ns	5, 25
$\overline{WE}$ hold time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	tWRH	5		5		5		ns	22, 25
$\overline{WE}$ setup time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	tWRP	20		20		20		ns	22, 26
$\overline{WE}$ hold time (WCBR test cycle)	tWTH	5		5		5		ns	22, 25
$\overline{WE}$ setup time	tWTS	20		20		20		ns	22, 26

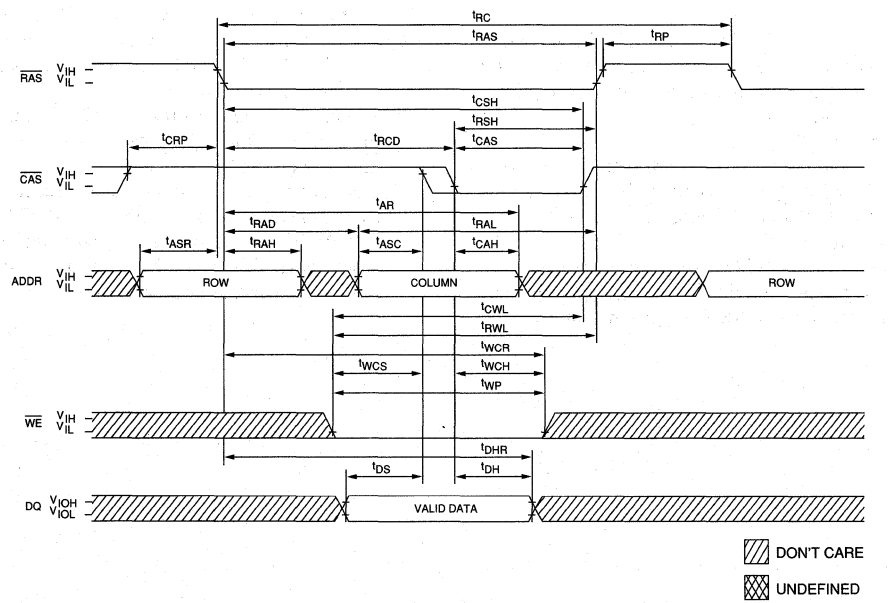
NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. V_{CC} = 5V ±10%, f = 1 MHz.
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is assured.
7. An initial pause of 100µs is required after power-up followed by eight $\overline{RAS}$ refresh cycles ($\overline{RAS}$-ONLY or CBR with $\overline{WE}$ HIGH) before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-up should be repeated any time the ^tREF refresh requirement is exceeded.
8. AC characteristics assume ^tT = 5ns.
9. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS}$ = V_{IH}, data output is High-Z.
12. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to 2 TTL gates and 100pF.
14. Assumes that $^tRCD < {}^tRCD$ (MAX). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
15. Assumes that $^tRCD \geq {}^tRCD$ (MAX).
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer, $\overline{CAS}$ must be pulsed HIGH for ^tCPN.
17. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (MAX) limit, then access time is controlled exclusively by ^tCAC.
18. Operation within the ^tRAD (MAX) limit ensures that ^tRCD (MAX) can be met. ^tRAD (MAX) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (MAX) limit, then access time is controlled exclusively by ^tAA.
19. Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
20. ^tOFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
21. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW.
22. ^tWTS and ^tWTH are setup and hold specifications for the $\overline{WE}$ pin being held LOW to enable the JEDEC test mode (with CBR timing constraints). These two parameters are the inverse of ^tWRP and ^tWRH in the CBR refresh cycle.
23. Timing between the DRAMs and the DRAM card did not change with the addition of the line drivers.
24. A +5ns timing skew from the DRAM to the DRAM card resulted from the addition of line drivers.
25. A -5ns timing skew from the DRAM to the DRAM card resulted from the addition of line drivers.
26. A +10ns timing skew from the DRAM to the DRAM card resulted from the addition of line drivers.
27. A -10ns timing skew from the DRAM to the DRAM card resulted from the addition of line drivers.
28. A -5ns (MIN) and a -10ns (MAX) timing skew from the DRAM to the DRAM card resulted from the addition of line drivers.
29. A +5ns (MIN) and a +10ns (MAX) timing skew from the DRAM to the DRAM card resulted from the addition of line drivers.
30. The maximum current ratings are based on one of the two banks operating or being refreshed (x36 mode). The stated maximums may be reduced by one half when used in the x18 mode. Standby currents of the non-active bank are not included.

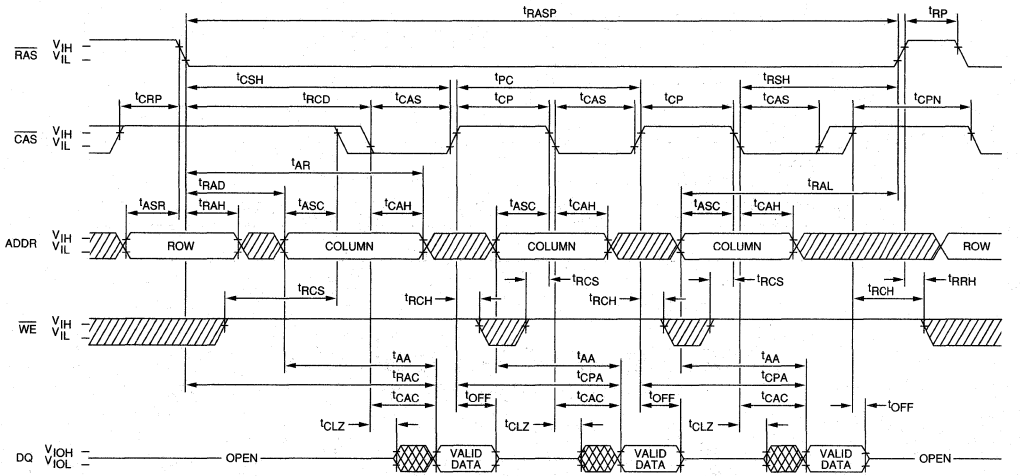
READ CYCLE



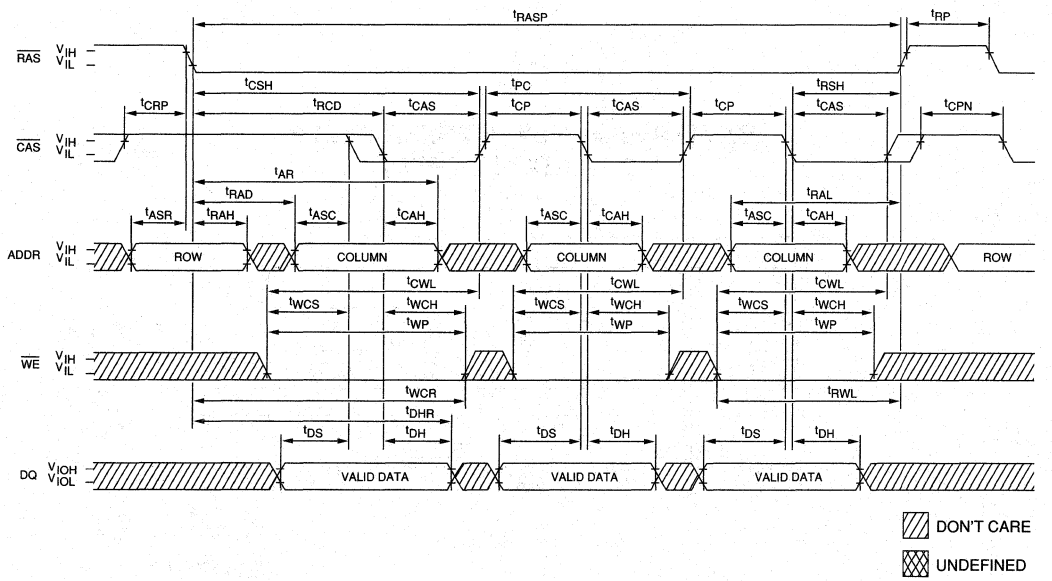
EARLY-WRITE CYCLE



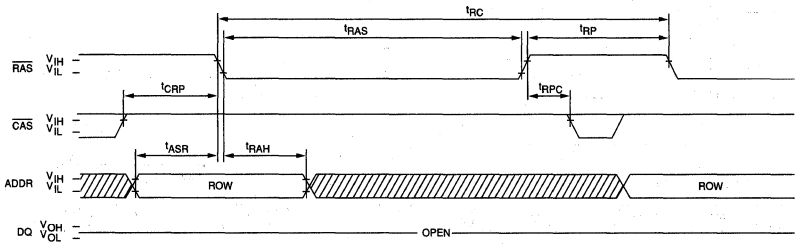
FAST-PAGE-MODE READ CYCLE



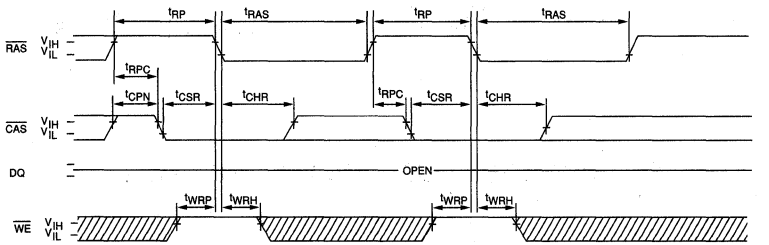
FAST-PAGE-MODE EARLY-WRITE CYCLE



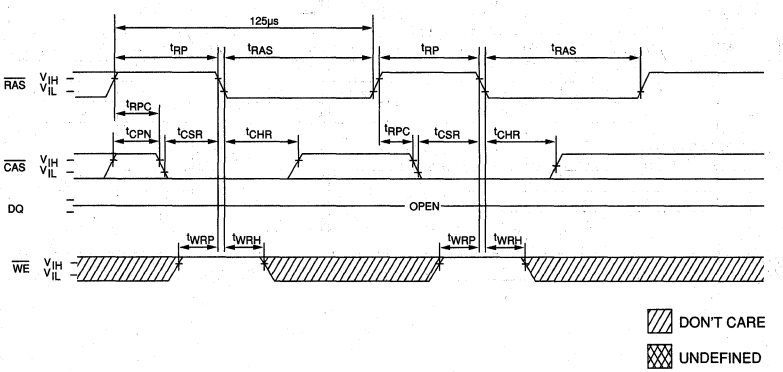
$\overline{RAS}$-ONLY REFRESH CYCLE
(ADDR = A0-A9; $\overline{WE}$ = DON'T CARE)



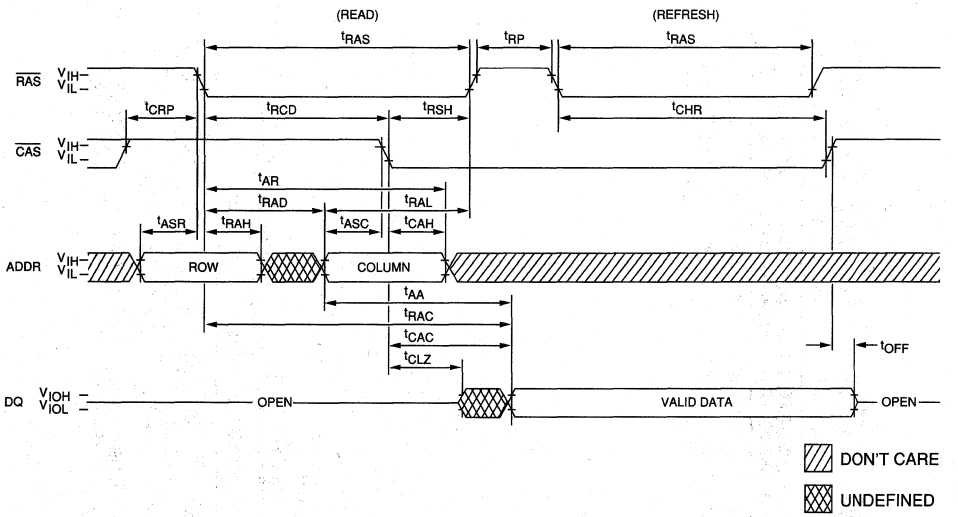
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE
(A0-A9 = DON'T CARE)



BATTERY BACKUP REFRESH CYCLE
(A0-A9 = DON'T CARE)



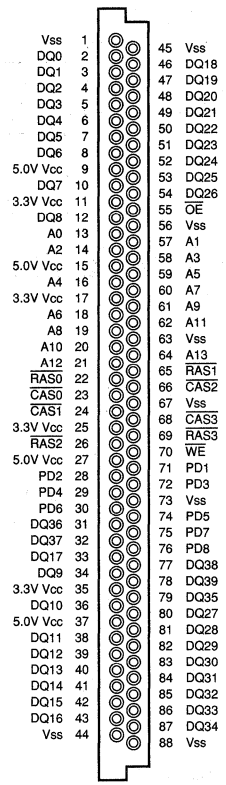
HIDDEN REFRESH CYCLE [21]
($\overline{WE}$ = HIGH)



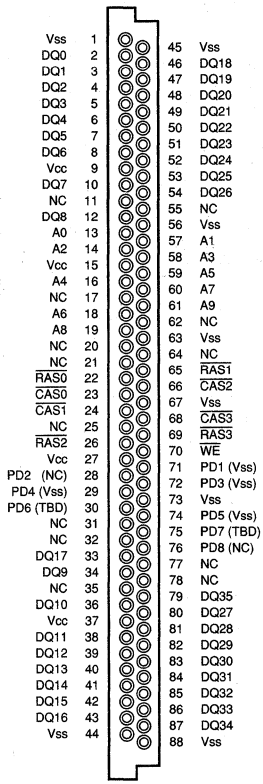
NEW ■ IC DRAM CARD

NEW ■ IC DRAM CARD

RESERVED JEDEC 88-PIN ASSIGNMENT
(All Possible Combinations)



MT24D88C236 PIN ASSIGNMENT
(JEDEC Standard)



IC DRAM CARD 1 MEGABYTE

256K x 40, 512K x 20

NEW ■ IC DRAM CARD

FEATURES

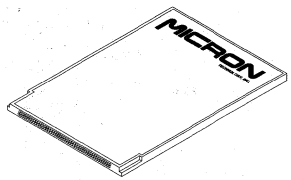
- JEIDA, JEDEC and PCMCIA standard 88-pin IC DRAM card
- Polarized receptacle connector
- Industry standard DRAM functions and timing
- High-performance, CMOS silicon-gate process
- All outputs are fully TTL compatible
- All inputs buffered except $\overline{RAS}$ inputs
- Multiple $\overline{RAS}$ inputs for x16/18/20 or x32/36/40 selectability
- Refresh modes: $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$ (CBR), HIDDEN and BATTERY BACKUP (BBU)
- FAST PAGE MODE access cycle
- Single +5V ±5% power supply
- Low power; 12mW standby, 2.7W active (typical)
- Extended refresh standard: 512 cycles every 64ms

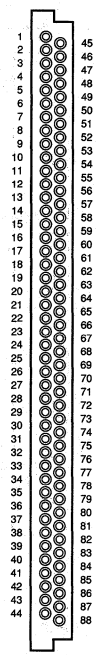
OPTIONS MARKING

- Timing

60ns access	-6
70ns access	-7
80ns access	-8

PIN ASSIGNMENT (End View)
88-Pin Card (U-1)





PIN #	SYMBOL	PIN #	SYMBOL	PIN #	SYMBOL
1	Vss	31	DQ36	61	NC
2	DQ0	32	DQ37	62	NC
3	DQ1	33	DQ17	63	Vss
4	DQ2	34	DQ9	64	NC
5	DQ3	35	NC	65	NC
6	DQ4	36	DQ10	66	$\overline{CAS2}$
7	DQ5	37	Vcc	67	Vss
8	DQ6	38	DQ11	68	$\overline{CAS3}$
9	Vcc	39	DQ12	69	NC
10	DQ7	40	DQ13	70	$\overline{WE}$
11	NC	41	DQ14	71	PD1 (Vss)
12	DQ8	42	DQ15	72	PD3 (Vss)
13	A0	43	DQ16	73	Vss
14	A2	44	Vss	74	PD5 (NC)
15	Vcc	45	Vss	75	PD7 (TBD)
16	A4	46	DQ18	76	PD8 (NC)
17	NC	47	DQ19	77	DQ38
18	A6	48	DQ20	78	DQ39
19	A8	49	DQ21	79	DQ35
20	NC	50	DQ22	80	DQ27
21	NC	51	DQ23	81	DQ28
22	$\overline{RAS0}$	52	DQ24	82	DQ29
23	$\overline{CAS0}$	53	DQ25	83	DQ30
24	$\overline{CAS1}$	54	DQ26	84	DQ31
25	NC	55	$\overline{OE}$ (Vss)	85	DQ32
26	$\overline{RAS2}$	56	Vss	86	DQ33
27	Vcc	57	A1	87	DQ34
28	PD2 (Vss)	58	A3	88	Vss
29	PD4 (Vss)	59	A5		
30	PD6 (TBD)	60	A7		

GENERAL DESCRIPTION

The MT12D88C25640 is a 1 megabyte, IC DRAM card organized primarily as a 256K x 40 bit memory array for EDC applications. It may be used as a x32 or x36 bit memory array (the unused DQs should be tied to Vss or Vcc through current limiting resistors). It may also be configured as a 512K x 20 bit memory array, provided the corresponding DQs on the host system are made common and memory bank control procedures are implemented. Separate $\overline{CAS}$ inputs allow byte accesses.

All inputs to the DRAMs are buffered, with the exception of $\overline{RAS}$. The line drivers used for buffers reduce reflections on the card and ensure compatibility in a wide range of systems. At the same time, the line drivers add delays to the buffered input timings when compared to standard DRAMs.

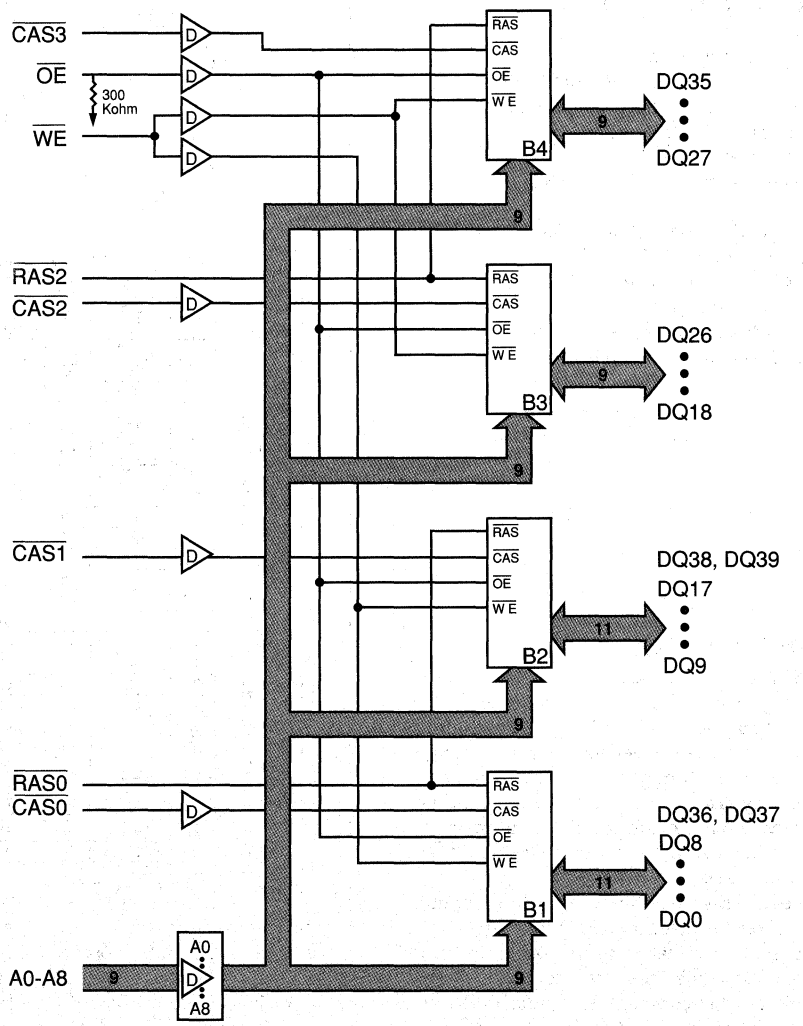
The MT12D88C25640 is designed for low power operation using 256K x 4 low power, extended refresh DRAMs. These devices support BATTERY BACKUP (BBU) cycle refresh; a very low current, data retention mode. Standard component DRAM refresh modes are supported as well.

Multiple $\overline{RAS}$ inputs conserve power by allowing individual bank selection. In the x32/36/40 organization, the memory is a single array that may be divided into four separate bytes (x32/x36 only). In the x16/18/20 organization, up to two banks, each with two separate bytes, may be independently selected. One bank is activated by each $\overline{RAS}$ selection; the others not selected remain in standby mode, drawing minimum power.

Eight presence detect pins may be read by the host to identify the MT12D88C25640 organization, number of banks, access time and refresh mode. These extensive presence detect functions allow systems to utilize the advanced power saving features.

The MT12D88C25640 is built with a plastic frame covered by stainless steel panels. This package, containing an 88-pin receptacle connector, is keyed to prevent improper installation or insertion into other types of IC card sockets.

FUNCTIONAL BLOCK DIAGRAM



NOTE:
1. D = 74AC11244 line drivers.
2. B1 and B2 = 256K x 11 memory blocks; B3 and B4 = 256K x 9 memory blocks.
3. $\overline{OE}$ is internally connected to ground via a 300 Kohm resistor and is also buffered to DRAM.

PIN DESCRIPTIONS

PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
22, 26	$\overline{RAS0}$, $\overline{RAS2}$	Input	Row Address Strobe: $\overline{RAS}$ is used to clock-in the 9 row-address bits. Two $\overline{RAS}$ inputs allow for a single x32/36/40 bank or two x16/18/20 banks.
23, 24, 66, 68	$\overline{CAS}$0-3	Input	Column Address Strobe: $\overline{CAS}$ is used to clock-in the 9 column-address bits, enable the DRAM output buffers, and strobe the data inputs on WRITE cycles. Four $\overline{CAS}$ inputs allow byte access control for any memory bank configuration (not in x40 mode).
70	$\overline{WE}$	Input	Write Enable: $\overline{WE}$ is the READ/WRITE control for the DQ pins. If $\overline{WE}$ is LOW prior to $\overline{CAS}$ going LOW, the access is an EARLY-WRITE cycle. If $\overline{WE}$ is HIGH while $\overline{CAS}$ is LOW, the access is a READ cycle, provided $\overline{OE}$ is also LOW. If WE goes LOW after $\overline{CAS}$ goes LOW, then the cycle is a LATE-WRITE cycle. A LATE-WRITE cycle is generally used in conjuction with a READ cycle to form a READ-MODIFY-WRITE cycle.
55	$\overline{OE}$	Input	Output Enable: $\overline{OE}$ is the input/output control for the DQ pins. $\overline{OE}$ is connected to ground through a 300 Kohm resistor and is intended to be LOW allowing for EARLY-WRITE cycles only. This signal may be driven, allowing for LATE-WRITE cycles.
13, 57, 14, 58, 16, 59, 18, 60, 19	A0-A8	Input	Address Inputs: These inputs are multiplexed and clocked by $\overline{RAS}$ and $\overline{CAS}$.
2-8, 10, 12, 34, 36, 38-43, 33, 46-54, 80-87, 79, 31, 32, 77, 78	DQ0-DQ39	Input/ Output	Data I/O: For WRITE cycles, DQ0-DQ39 act as inputs to the addressed DRAM location. BYTE WRITEs may be performed by using the corresponding $\overline{CAS}$ select (x32/36 mode only). For READ access cycles, DQ0-DQ39 act as outputs for the addressed DRAM location.
71, 28, 72, 29, 74, 30, 75, 76	PD1-PD8	-	Presence Detect: These pins are read by the host system and tell the system the card's personality. They will be either left floating (NC) or they will be grounded (Vss).
11, 17, 20, 21, 25, 35, 61, 62, 64, 65, 69	NC	-	No Connect: These pins should be left unconnected (reserved for future use).
9, 15, 27, 37	Vcc	Supply	Power Supply: +5V ±5%
1, 44, 45, 56, 63, 67, 73, 88	Vss	Supply	Ground

FUNCTIONAL DESCRIPTION

The MT12D88C25640 is a 1 megabyte memory card structured as a 256K x 32/36/40 bit memory array ($\overline{RAS0}$ = $\overline{RAS2}$). It also may be configured as a 512K x 16/18/20 bit memory array, provided the corresponding DQs on the host are connected and memory bank control procedures are implemented by interleaving both $\overline{RAS}$ lines.

Most x32/36/40 bit applications use the same signal to control the $\overline{CAS}$ inputs. $\overline{RAS0}$ controls the lower 16/18 bits, and $\overline{RAS2}$ controls the upper 16/18 bits to obtain a x32/36 memory array. For x16/18 applications, the corresponding DQs and the corresponding $\overline{CAS}$ pins must be connected together (DQ0 to DQ18, DQ1 to DQ19 and so forth, and $\overline{CAS0}$ to $\overline{CAS2}$ and $\overline{CAS1}$ to $\overline{CAS3}$). Each $\overline{RAS}$ is then a bank select for the 512K x 16/18 memory organization.

DRAM OPERATION

DRAM REFRESH

Memory cell data is retained in its correct state by maintaining power and executing any $\overline{RAS}$ cycle [READ, WRITE, $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$ (CBR), HIDDEN or BATTERY BACKUP (BBU) REFRESH] so that all 512 combinations of $\overline{RAS}$ addresses (A0-A8) are executed at least every 64ms, regardless of sequence.

The implied method of choice for refreshing the memory card is the BBU cycle. This is a very low current, data retention mode made possible by using the CBR REFRESH cycle over the extended refresh range (I_{CC7}).

The memory card may be used with the other refresh modes common in standard DRAMs. This allows the memory card to be used on existing systems that do not utilize the BBU REFRESH cycle. However, the memory card will draw more current in the STANDBY mode. The CBR REFRESH mode is recommended when not using the BBU mode.

DRAM READ AND WRITE CYCLES

During READ or WRITE cycles, each bit is uniquely addressed through the 18 address bits, which are entered 9 bits (A0-A8) at a time. $\overline{RAS}$ is used to latch the first 9 bits and $\overline{CAS}$ the latter 9 bits. READ or WRITE cycles are selected with the $\overline{WE}$ input. A logic HIGH on $\overline{WE}$ dictates READ mode while a logic LOW on $\overline{WE}$ dictates WRITE mode. During a WRITE cycle, data in (D) is latched by the falling edge of $\overline{CAS}$. $\overline{WE}$ must fall prior to $\overline{CAS}$ (EARLY WRITE); if $\overline{WE}$ goes LOW after $\overline{CAS}$, the outputs (Q) will be activated and will drive invalid data to the inputs, unless LATE-WRITE cycle timing specifications are met. The data inputs and data outputs are routed through pins using common I/O, and pin direction is controlled by $\overline{WE}$.

FAST PAGE MODE operation allows faster data operations (READ or WRITE) within a row address (A0-A8) defined page boundary. The FAST PAGE MODE cycle is always initiated with a row address strobed-in by $\overline{RAS}$ followed by a column address strobed-in by $\overline{CAS}$. $\overline{CAS}$ may be toggled-in by holding $\overline{RAS}$ LOW and strobing-in different column addresses, thus executing faster memory cycles. Returning $\overline{RAS}$ HIGH terminates the FAST PAGE MODE operation. Returning $\overline{RAS}$ and $\overline{CAS}$ HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the $\overline{RAS}$ high time.

DRAM TIMING

In accordance with JEDEC standard specifications, all inputs to the IC DRAM card are buffered, with the exception of $\overline{RAS}$ inputs. The line drivers used for buffers reduce reflections on the card and ensure compatibility in a wide range of systems. The implementation of buffers on the card may relieve the need for additional host system line drivers. Notes 23 though 29 indicate which parameters on the IC DRAM card are affected by the line drivers, and to what magnitude they are affected. The component DRAM timing specifications, rather than those of the IC DRAM card (in systems that use both), may cause timing incompatibilities.

All traces on the IC DRAM card (buffered and non-buffered) are approximately 50 ohms characteristic impedance. Matching impedance on the system board to 50 ohms characteristic impedance on traces to the IC DRAM card will decrease signal noise to the IC DRAM card, enhancing overall system reliability.

PHYSICAL DESIGN

The MT12D88C25640 is constructed with a molded plastic frame and covered with stainless steel panels. Inside, 8 thin small-outline package (TSOP) DRAMs are mounted on an ultrathin printed circuit board. The board is attached to a high insertion, 88-pin receptacle connector. The package has a polarized key to prevent improper installation, including insertion into other types of IC card sockets. The MT12D88C25640 operates reliably up to 55°C.

MEMORY TRUTH TABLE

FUNCTION		RAS	CAS	WE	OE	ADDRESSES tR	ADDRESSES tC	DATA IN/OUT DQ0-DQ39
Standby		H	H→X	X	X	X	X	High-Z
READ		L	L	H	L (NC)	ROW	COL	Data Out
EARLY-WRITE		L	L	L	X	ROW	COL	Data In
READ-WRITE		L	L	H→L	L→H	ROW	COL	Data Out
FAST-PAGE-MODE	1st Cycle	L	H→L	H	L (NC)	ROW	COL	Data Out
READ	2nd Cycle	L	H→L	H	L (NC)	n/a	COL	Data Out
FAST-PAGE-MODE	1st Cycle	L	H→L	L	X	ROW	COL	Data In
EARLY-WRITE	2nd Cycle	L	H→L	L	X	n/a	COL	Data In
FAST-PAGE-MODE	1st Cycle	L	H→L	H→L	L→H	ROW	COL	Data In
READ-WRITE	2nd Cycle	L	H→L	H→L	L→H	n/a	COL	Data In
RAS-ONLY REFRESH		L	X	X	X	ROW	n/a	High-Z
HIDDEN	READ	L→H→L	L	H	L (NC)	ROW	COL	Data Out
REFRESH	WRITE	L→H→L	L	L	X	ROW	COL	Data In
CAS-BEFORE-RAS REFRESH		H→L	L	H	X	X	X	High-Z
BATTERY BACKUP REFRESH		H→L	L	H	X	X	X	High-Z

PRESENCE DETECT TRUTH TABLE

CHARACTERISTICS						PRESENT DETECT PIN (PDx)							
Card Density	DRAM Organizations	Card Address	RAS Address	CAS Address	Page Depth	1	2	3	4	5	6	7	8
0MB	No card installed	X	X	X	X	NC	NC	NC	NC	NC	X	X	X
• 1MB	256K x 1, 4, 16, 18	18	9	9	512	Vss	Vss	Vss	Vss	NC	X	X	X
2MB	256K x 1, 4, 16, 18	18	9	9	512	Vss	Vss	Vss	Vss	Vss	X	X	X
2MB	512K x 8, 9	19	10	9	512	NC	Vss	Vss	Vss	NC	X	X	X
4MB	512K x 8, 9	19	10	9	512	NC	Vss	Vss	Vss	Vss	X	X	X
4MB	1 Meg x 1, 4, 16, 18	20	10	10	1,024	Vss	NC	Vss	Vss	NC	X	X	X
8MB	1 Meg x 1, 4, 16, 18	20	10	10	1,024	Vss	NC	Vss	Vss	Vss	X	X	X
8MB	2 Meg x 8, 9	21	11	10	1,024	NC	NC	Vss	Vss	NC	X	X	X
16MB	2 Meg x 8, 9	21	11	10	1,024	NC	NC	Vss	Vss	Vss	X	X	X
16MB	4 Meg x 1, 4, 16, 18	22	12	11	1,024	Vss	Vss	NC	Vss	NC	X	X	X
32MB	4 Meg x 1, 4, 16, 18	22	12	11	1,024	Vss	Vss	NC	Vss	Vss	X	X	X
Access Timing		100ns				X	X	X	X	X	Vss	Vss	X
		80ns				X	X	X	X	X	NC	Vss	X
		70ns				X	X	X	X	X	Vss	NC	X
		60ns				X	X	X	X	X	NC	NC	X
		50ns				X	X	X	X	X	Vss	Vss	X
Refresh Control		Standard				X	X	X	X	X	X	X	NC
		Auto				X	X	X	X	X	X	X	Vss

NOTE: Vss = Ground.

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} ..... -0.5V to +5.25V
Operating Temperature, T_A (Ambient) ..... 0°C to +55°C
Storage Temperature ..... -20°C to +80°C
Power Dissipation 15W
Short Circuit Output Current 50mA
Card Insertions (Connector's Life Cycle) 10,000

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 3, 4, 6, 7) (0°C ≤ T_A ≤ 55°C; V_{CC} = 5V ±5%)

PARAMETER/CONDITION		SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage		V_{CC}	4.75	5.25	V	1
Input High (Logic 1) Voltage, All Inputs		V_{IH}	3.5	V_{CC}+0.5	V	1
Input Low (Logic 0) Voltage, All Inputs		V_{IL}	-0.5	0.8	V	1
INPUT LEAKAGE CURRENT, Any input	Non-buffered	I_{IN}	-12	12	µA	
(0V ≤ V_{IN} ≤ 5.25V; all other pins not under test = 0V)	Buffered	I_{IB}	-2	2	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled; 0V ≤ V_{OUT} ≤ 5.25V)		I_{OZ}	-10	10	µA	
OUTPUT LEVELS Output High Voltage (I_{OUT} = -5mA)		V_{OH}	2.4		V	
Output Low Voltage (I_{OUT} = 4.2mA)		V_{OL}		0.4	V	

		MAX				
PARAMETER/CONDITION	SYMBOL	-6	-7	-8	UNITS	NOTES
STANDBY CURRENT: (TTL) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC1}	24	24	24	mA	
STANDBY CURRENT: (CMOS) ($\overline{RAS}$ = $\overline{CAS}$ = Other Inputs = V_{CC} -0.2V)	I_{CC2}	2.4	2.4	2.4	mA	
OPERATING CURRENT: Random READ/WRITE Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC (MIN))	I_{CC3}	1.0	0.9	0.8	A	3, 4, 30
OPERATING CURRENT: FAST PAGE MODE Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: ^tPC = ^tPC (MIN))	I_{CC4}	780	660	540	mA	3, 4, 30
REFRESH CURRENT: $\overline{RAS}$-ONLY Average power supply current ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}: ^tRC = ^tRC (MIN))	I_{CC5}	1.0	0.9	0.8	A	3, 30
REFRESH CURRENT: $\overline{CAS}$-BEFORE-$\overline{RAS}$ (CBR) Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC (MIN))	I_{CC6}	1.0	0.9	0.8	A	3, 5, 30
REFRESH CURRENT: BATTERY BACKUP (BBU) Average power supply current during BBU: $\overline{CAS}$ = 0.2V or CBR cycling; $\overline{RAS}$ = ^tRAS (MIN) up to 300ns; ^tRC = 125µs; $\overline{WE}$, A0-A8 and DQ = V_{CC} -0.2V or 0.2V (DQ may be left open)	I_{CC7}	2.4	2.4	2.4	mA	3 , 5

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: $\overline{CAS0}$, $\overline{CAS1}$, $\overline{CAS2}$, $\overline{CAS3}$, A0-A8, $\overline{OE}$	C_{I1}		9	pF	2
Input Capacitance: $\overline{WE}$	C_{I2}		13	pF	2
Input Capacitance: $\overline{RAS0}$, $\overline{RAS2}$	C_{I3}		50	pF	2
Input/Output Capacitance: DQ	C_{IO}		12	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C ≤ T_A ≤ 55°C; V_{CC} = 5V ±5%)

AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	^tRC	110		130		150		ns	23
FAST-PAGE-MODE READ or WRITE cycle time	^tPC	40		40		45		ns	23
Access time from $\overline{RAS}$	^tRAC		60		70		80	ns	14, 23
Access time from $\overline{CAS}$	^tCAC		25		30		30	ns	15, 26
Access time from column address	^tAA		40		45		50	ns	26
Access time from $\overline{CAS}$ precharge	^tCPA		50		50		55	ns	26
$\overline{RAS}$ pulse width	^tRAS	60	100,000	70	100,000	80	100,000	ns	23
$\overline{RAS}$ pulse width (FAST PAGE MODE)	^tRASP	60	100,000	70	100,000	80	100,000	ns	23
$\overline{RAS}$ hold time	^tRSH	25		30		30		ns	26
$\overline{RAS}$ precharge time	^tRP	40		50		60		ns	23
$\overline{CAS}$ pulse width	^tCAS	15	100,000	20	100,000	20	100,000	ns	23
$\overline{CAS}$ hold time	^tCSH	55		65		75		ns	25
$\overline{CAS}$ precharge time	^tCPN	10		10		10		ns	16, 23
$\overline{CAS}$ precharge time (FAST PAGE MODE)	^tCP	10		10		10		ns	23
$\overline{RAS}$ to $\overline{CAS}$ delay time	^tRCD	10	35	15	40	15	50	ns	17, 28
$\overline{CAS}$ to $\overline{RAS}$ precharge time	^tCRP	15		15		15		ns	26
Row address setup time	^tASR	10		10		10		ns	26
Row address hold time	^tRAH	5		5		5		ns	25
$\overline{RAS}$ to column address delay time	^tRAD	10	20	10	25	10	30	ns	18, 28
Column address setup time	^tASC	5		5		5		ns	24
Column address hold time	^tCAH	15		20		20		ns	24
Column address hold time (referenced to $\overline{RAS}$)	^tAR	45		50		55		ns	25
Column address to $\overline{RAS}$ lead time	^tRAL	40		45		50		ns	26
Read command setup time	^tRCS	5		5		5		ns	25
Read command hold time (referenced to $\overline{CAS}$)	^tRCH	5		5		5		ns	19, 24
Read command hold time (referenced to $\overline{RAS}$)	^tRRH	-5		-5		-5		ns	19, 25
$\overline{CAS}$ to output in Low-Z	^tCLZ	5		5		5		ns	24
Output buffer turn-off delay	^tOFF	5	30	5	30	5	30	ns	20, 29, 35
$\overline{WE}$ command setup time	^tWCS	5		5		5		ns	24

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C ≤ T_A ≤ 55°C; Vcc = 5V ±5%)

AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Write command hold time	^tWCH	15		20		20		ns	24
Write command hold time (referenced to $\overline{RAS}$)	^tWCR	40		50		55		ns	25
Write command pulse width	^tWP	10		15		15		ns	23
Write command to $\overline{RAS}$ lead time	^tRWL	25		30		30		ns	26
Write command to $\overline{CAS}$ lead time	^tCWL	20		25		25		ns	24
Data-in setup time	^tDS	5		5		5		ns	24, 32
Data-in hold time	^tDH	5		10		10		ns	25, 32
Data-in hold time (referenced to $\overline{RAS}$)	^tDHR	45		55		60		ns	23
Transition time (rise or fall)	^tT	2	15	2	15	2	15	ns	9, 10, 23
Refresh period (1,024 cycles)	^tREF		128		128		128	ms	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	^tRPC	10		10		10		ns	26
$\overline{CAS}$ setup time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tCSR	20		20		20		ns	5, 26
$\overline{CAS}$ hold time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tCHR	10		10		10		ns	5, 25
$\overline{WE}$ hold time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tWRH	5		5		5		ns	22, 25
$\overline{WE}$ setup time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tWRP	20		20		20		ns	22, 26
$\overline{WE}$ hold time (WCBR test cycle)	^tWTH	5		5		5		ns	22, 25
$\overline{WE}$ setup time	^tWTS	20		20		20		ns	22, 26
READ-WRITE cycle time	^tRWC	165		185		205		ns	
FAST-PAGE-MODE READ-WRITE cycle time	^tPRWC	90		95		100		ns	23
$\overline{RAS}$ to $\overline{WE}$ delay time	^tRWD	80		90		100		ns	31, 27
Column Address to $\overline{WE}$ delay time	^tAWD	65		70		75		ns	31, 24
$\overline{CAS}$ to $\overline{WE}$ delay time	^tCWD	50		65		55		ns	31, 24
Output buffer turn-off delay	^tOE		25		30		30	ns	20, 33, 26
Output disable	^tOD		25		30		30	ns	35, 26
$\overline{OE}$ hold time from $\overline{WE}$ during READ-MODIFY-WRITE cycle	^tOEH	5		10		10		ns	34, 27
$\overline{OE}$ hold time from $\overline{RAS}$ during HIDDEN REFRESH cycle	^tORD	10		10		10		ns	21, 26

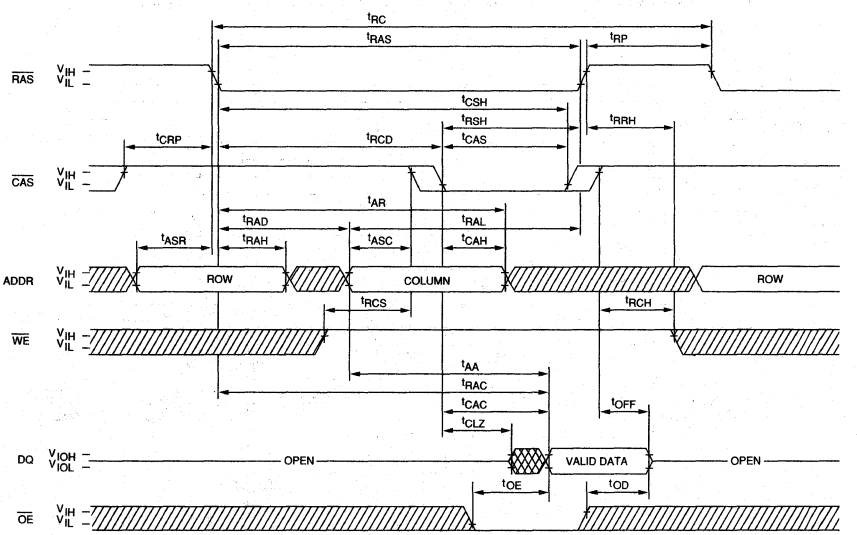
NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. V_{CC} = 5V ±10%, f = 1 MHz.
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is assured.
7. An initial pause of 100µs is required after power-up followed by eight $\overline{RAS}$ refresh cycles ($\overline{RAS}$-ONLY or CBR with $\overline{WE}$ HIGH) before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-up should be repeated any time the ^{t}REF refresh requirement is exceeded.
8. AC characteristics assume ^{t}T = 5ns.
9. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS}$ = V_{IH}, data output is High-Z.
12. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to 2 TTL gates and 100pF.
14. Assumes that $^{t}RCD < {}^{t}RCD$ (MAX). If ^{t}RCD is greater than the maximum recommended value shown in this table, ^{t}RAC will increase by the amount that ^{t}RCD exceeds the value shown.
15. Assumes that $^{t}RCD \geq {}^{t}RCD$ (MAX).
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer, $\overline{CAS}$ must be pulsed HIGH for ^{t}CPN.
17. Operation within the ^{t}RCD (MAX) limit ensures that ^{t}RAC (MAX) can be met. ^{t}RCD (MAX) is specified as a reference point only; if ^{t}RCD is greater than the specified ^{t}RCD (MAX) limit, then access time is controlled exclusively by ^{t}CAC.
18. Operation within the ^{t}RAD (MAX) limit ensures that ^{t}RCD (MAX) can be met. ^{t}RAD (MAX) is specified as a reference point only; if ^{t}RAD is greater than the specified ^{t}RAD (MAX) limit, then access time is controlled exclusively by ^{t}AA.
19. Either ^{t}RCH or ^{t}RRH must be satisfied for a READ cycle.
20. ^{t}OFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
21. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW.
22. ^{t}WTS and ^{t}WTH are setup and hold specifications for the $\overline{WE}$ pin being held LOW to enable the JEDEC test mode (with CBR timing constraints). These two parameters are the inverse of ^{t}WRP and ^{t}WRH in the CBR refresh cycle.
23. Timing between the DRAMs and the DRAM card did not change with the addition of the line drivers.
24. A +5ns timing skew from the DRAM to the DRAM card resulted from the addition of line drivers.
25. A -5ns timing skew from the DRAM to the DRAM card resulted from the addition of line drivers.
26. A +10ns timing skew from the DRAM to the DRAM card resulted from the addition of line drivers.
27. A -10ns timing skew from the DRAM to the DRAM card resulted from the addition of line drivers.
28. A -5ns (MIN) and a -10ns (MAX) timing skew from the DRAM to the DRAM card resulted from the addition of line drivers.
29. A +5ns (MIN) and a +10ns (MAX) timing skew from the DRAM to the DRAM card resulted from the addition of line drivers.
30. The maximum current ratings are based with the memory operating or being refreshed in the x32/36/40 mode. The stated maximums may be reduced by one half when used in the x16/18/20 mode.
31. ^{t}WCS, ^{t}RWD, ^{t}AWD and ^{t}CWD are restrictive operating parameters in late WRITE, and READ-MODIFY-WRITE cycles only. If $^{t}WCS \geq {}^{t}WCS$ (MIN), the cycle is an EARLY-WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If $^{t}RWD \geq {}^{t}RWD$ (MIN), $^{t}AWD \geq {}^{t}AWD$ (MIN) and $^{t}CWD \geq {}^{t}CWD$ (MIN), the cycle is a READ-MODIFY-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of data out is indeterminate. $\overline{OE}$ held HIGH and $\overline{WE}$ taken LOW after $\overline{CAS}$ goes LOW results in a LATE-WRITE ($\overline{OE}$ controlled) cycle.

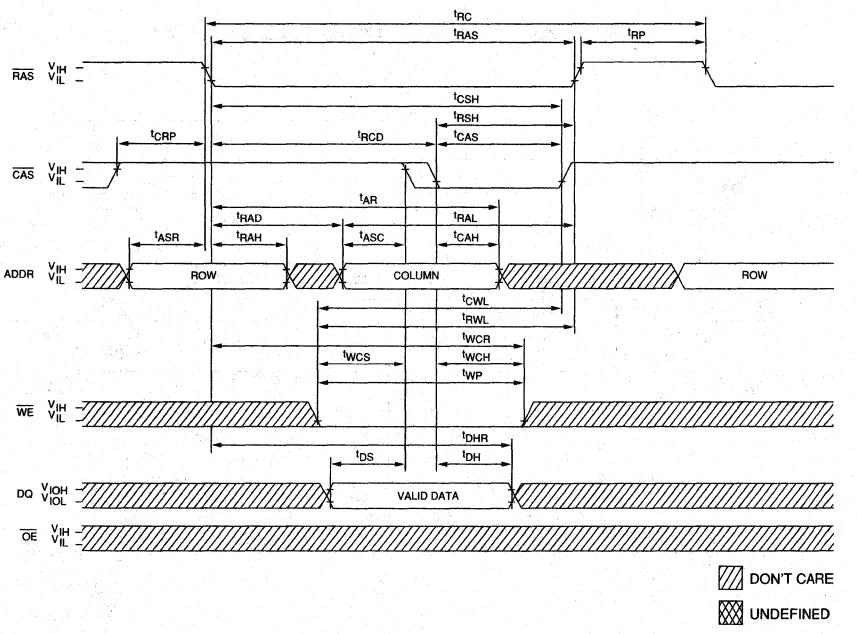
NOTES (continued)

32. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY-WRITE cycles and $\overline{WE}$ leading edge in LATE-WRITE or READ-MODIFY-WRITE cycles.
33. If $\overline{OE}$ is tied permanently LOW, LATE-WRITE or READ-MODIFY-WRITE operations are not possible.
34. LATE-WRITE and READ-MODIFY-WRITE cycles must have both ^{t}OD and ^{t}OEH met ($\overline{OE}$ HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. The DQs will provide the previously read data if $\overline{CAS}$ remains LOW and $\overline{OE}$ is taken back LOW after ^{t}OEH is met. If $\overline{CAS}$ goes HIGH prior to $\overline{OE}$ going back LOW, the DQs will remain open.
35. The DQs open during READ cycles once ^{t}OD or ^{t}OFF occur. If $\overline{CAS}$ goes HIGH first, $\overline{OE}$ becomes a "don't care." If $\overline{OE}$ goes HIGH and $\overline{CAS}$ stays LOW, $\overline{OE}$ is not a "don't care;" and the DQs will provide the previously read data if $\overline{OE}$ is taken back LOW (while $\overline{CAS}$ remains LOW).

READ CYCLE

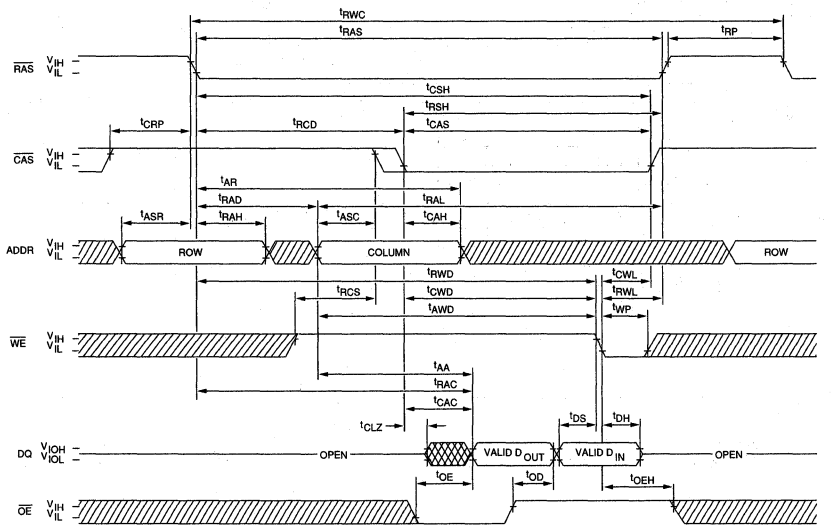


EARLY-WRITE CYCLE

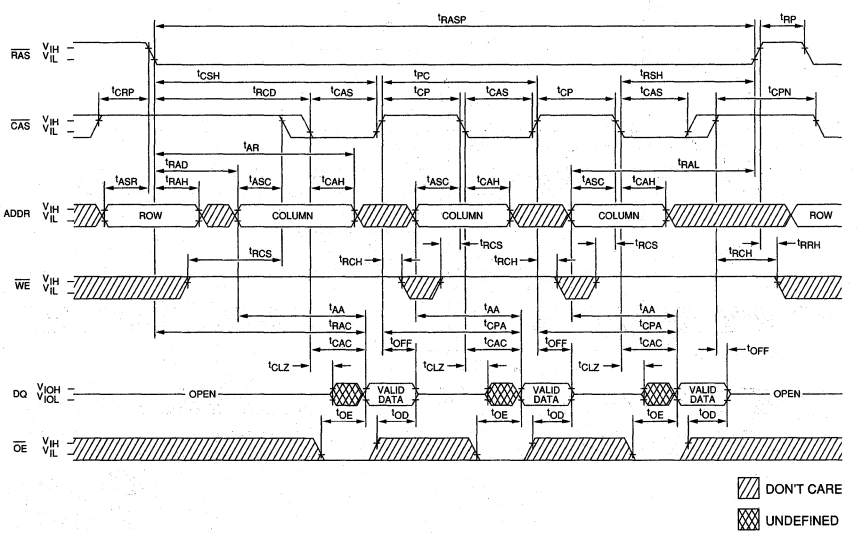


NEW ■ IC DRAM CARD

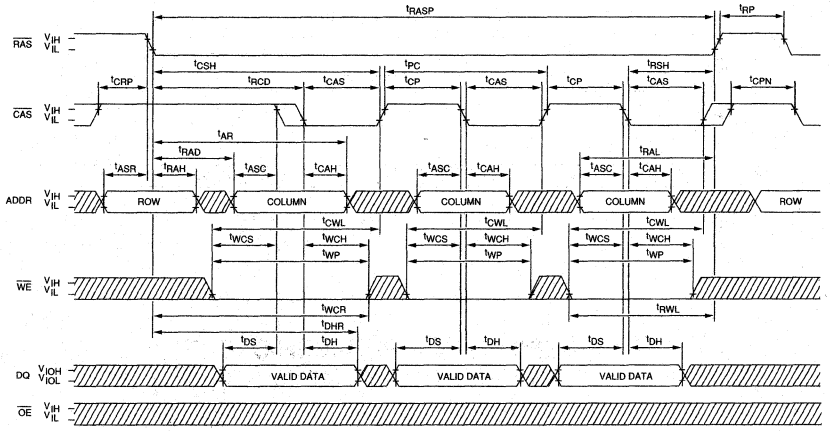
READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)



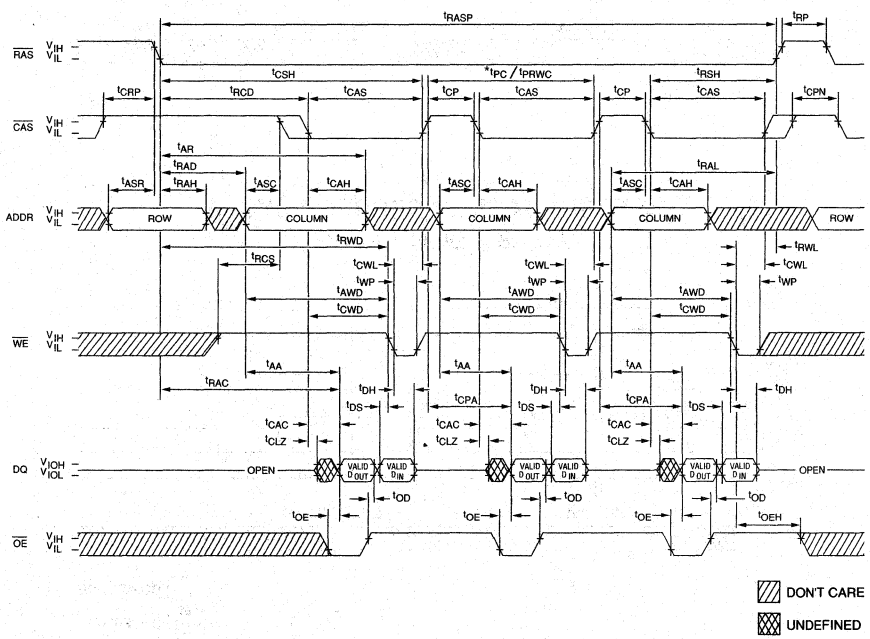
FAST-PAGE-MODE READ CYCLE



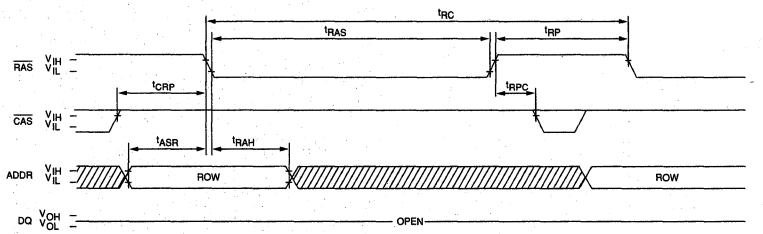
FAST-PAGE-MODE EARLY-WRITE CYCLE



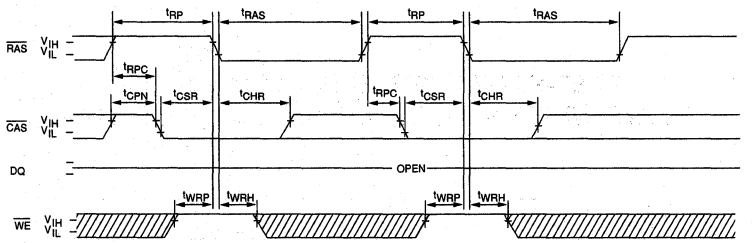
FAST-PAGE-MODE READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)



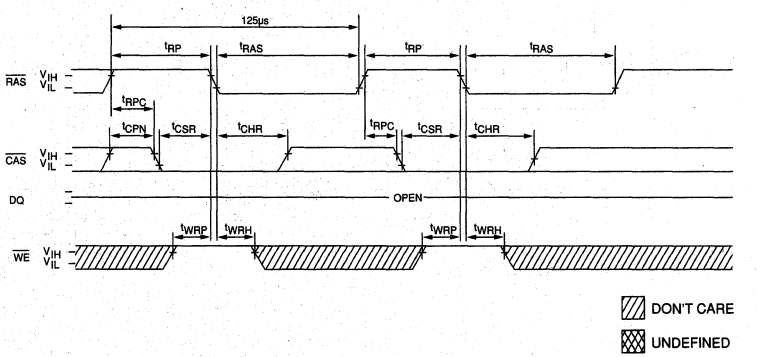
$\overline{\text{RAS}}$-ONLY REFRESH CYCLE
(ADDR = A0-A8; $\overline{\text{WE}}$ = DON'T CARE)



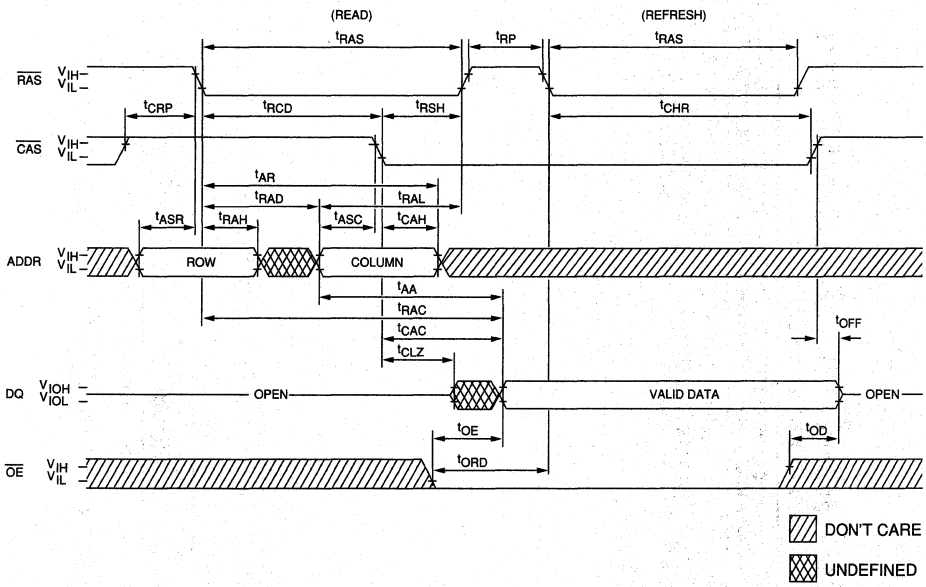
$\overline{\text{CAS}}$-BEFORE-$\overline{\text{RAS}}$ REFRESH CYCLE
(A0-A8 = DON'T CARE)



BATTERY BACKUP REFRESH CYCLE
(A0-A8 = DON'T CARE)

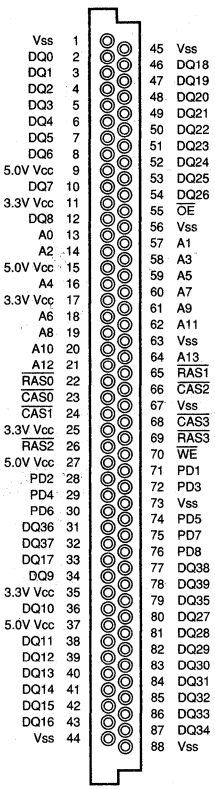


HIDDEN REFRESH CYCLE [21]
($\overline{WE}$ = HIGH)



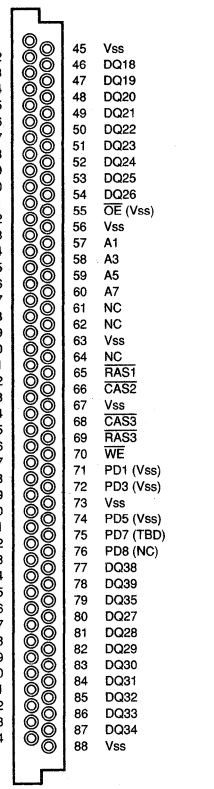
NEW ■ IC DRAM CARD

RESERVED JEDEC, JEIDA and PCMCIA 88-PIN ASSIGNMENT
(All Possible Combinations)



Vss	1	45	Vss
DQ0	2	46	DQ18
DQ1	3	47	DQ19
DQ2	4	48	DQ20
DQ3	5	49	DQ21
DQ4	6	50	DQ22
DQ5	7	51	DQ23
DQ6	8	52	DQ24
5.0V Vcc	9	53	DQ25
DQ7	10	54	DQ26
3.3V Vcc	11	55	$\overline{OE}$
DQ8	12	56	Vss
A0	13	57	A1
A2	14	58	A3
5.0V Vcc	15	59	A5
A4	16	60	A7
3.3V Vcc	17	61	A9
A6	18	62	A11
A8	19	63	Vss
A10	20	64	A13
A12	21	65	$\overline{RAS1}$
$\overline{RAS0}$	22	66	$\overline{CAS2}$
$\overline{CAS0}$	23	67	Vss
$\overline{CAS1}$	24	68	$\overline{CAS3}$
3.3V Vcc	25	69	$\overline{RAS3}$
$\overline{RAS2}$	26	70	$\overline{WE}$
5.0V Vcc	27	71	PD1
PD2	28	72	PD3
PD4	29	73	Vss
PD6	30	74	PD5
DQ36	31	75	PD7
DQ37	32	76	PD8
DQ17	33	77	DQ38
DQ9	34	78	DQ39
3.3V Vcc	35	79	DQ35
DQ10	36	80	DQ27
5.0V Vcc	37	81	DQ28
DQ11	38	82	DQ29
DQ12	39	83	DQ30
DQ13	40	84	DQ31
DQ14	41	85	DQ32
DQ15	42	86	DQ33
DQ16	43	87	DQ34
Vss	44	88	Vss

MT12D88C25640 PIN ASSIGNMENT
(JEDEC Standard)



Vss	1	45	Vss
DQ0	2	46	DQ18
DQ1	3	47	DQ19
DQ2	4	48	DQ20
DQ3	5	49	DQ21
DQ4	6	50	DQ22
DQ5	7	51	DQ23
DQ6	8	52	DQ24
Vcc	9	53	DQ25
DQ7	10	54	DQ26
NC	11	55	$\overline{OE}$ (Vss)
DQ8	12	56	Vss
A0	13	57	A1
A2	14	58	A3
Vcc	15	59	A5
A4	16	60	A7
NC	17	61	NC
A6	18	62	NC
A8	19	63	Vss
NC	20	64	NC
NC	21	65	$\overline{RAS1}$
$\overline{RAS0}$	22	66	$\overline{CAS2}$
$\overline{CAS0}$	23	67	Vss
$\overline{CAS1}$	24	68	$\overline{CAS3}$
NC	25	69	$\overline{RAS3}$
$\overline{RAS2}$	26	70	$\overline{WE}$
Vcc	27	71	PD1 (Vss)
PD2 (Vss)	28	72	PD3 (Vss)
PD4 (Vss)	29	73	Vss
PD6 (TBD)	30	74	PD5 (Vss)
DQ36	31	75	PD7 (TBD)
DQ37	32	76	PD8 (NC)
DQ17	33	77	DQ38
DQ9	34	78	DQ39
NC	35	79	DQ35
DQ10	36	80	DQ27
VCC	37	81	DQ28
DQ11	38	82	DQ29
DQ12	39	83	DQ30
DQ13	40	84	DQ31
DQ14	41	85	DQ32
DQ15	42	86	DQ33
DQ16	43	87	DQ34
Vss	44	88	Vss

IC DRAM CARD 2 MEGABYTES

512K x 40, 1 MEG x 20

NEW IC DRAM CARD

FEATURES

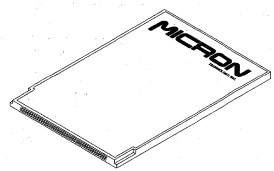
- JEIDA, JEDEC and PCMCIA standard 88-pin IC DRAM card
- Polarized receptacle connector
- Industry standard DRAM functions and timing
- High-performance, CMOS silicon-gate process
- All outputs are fully TTL compatible
- All inputs buffered except $\overline{RAS}$ inputs
- Multiple $\overline{RAS}$ inputs for x16/18/20 or x32/36/40 selectability
- Refresh modes: $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$ (CBR), BATTERY BACKUP (BBU) and HIDDEN
- FAST PAGE MODE access cycle
- Single +5V ±5% power supply
- Low power; 24mW standby, 2.7W active (typical)
- Extended refresh standard: 512 cycles every 64ms

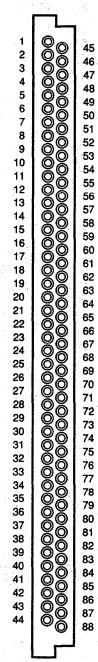
OPTIONS MARKING

- Timing

60ns access	-6
70ns access	-7
80ns access	-8

PIN ASSIGNMENT (End View)
88-Pin Card (U-1)





PIN #	SYMBOL	PIN #	SYMBOL	PIN #	SYMBOL
1	Vss	31	DQ36	61	NC
2	DQ0	32	DQ37	62	NC
3	DQ1	33	DQ17	63	Vss
4	DQ2	34	DQ9	64	NC
5	DQ3	35	NC	65	$\overline{RAS1}$
6	DQ4	36	DQ10	66	$\overline{CAS2}$
7	DQ5	37	Vcc	67	Vss
8	DQ6	38	DQ11	68	$\overline{CAS3}$
9	Vcc	39	DQ12	69	$\overline{RAS3}$
10	DQ7	40	DQ13	70	$\overline{WE}$
11	NC	41	DQ14	71	PD1 (Vss)
12	DQ8	42	DQ15	72	PD3 (Vss)
13	A0	43	DQ16	73	Vss
14	A2	44	Vss	74	PD5 (Vss)
15	Vcc	45	Vss	75	PD7 (TBD)
16	A4	46	DQ18	76	PD8 (NC)
17	NC	47	DQ19	77	DQ38
18	A6	48	DQ20	78	DQ39
19	A8	49	DQ21	79	DQ35
20	NC	50	DQ22	80	DQ27
21	NC	51	DQ23	81	DQ28
22	$\overline{RAS0}$	52	DQ24	82	DQ29
23	$\overline{CAS0}$	53	DQ25	83	DQ30
24	$\overline{CAS1}$	54	DQ26	84	DQ31
25	NC	55	$\overline{OE}$ (Vss)	85	DQ32
26	$\overline{RAS2}$	56	Vss	86	DQ33
27	Vcc	57	A1	87	DQ34
28	PD2 (Vss)	58	A3	88	Vss
29	PD4 (Vss)	59	A5		
30	PD6 (TBD)	60	A7		

GENERAL DESCRIPTION

The MT24D88C51240 is a 2 megabyte, IC DRAM card organized primarily as a 512K x 40 bit memory array for EDC applications. It may be used as a x32 or x36 bit memory array (the unused DQs should be tied to Vss or Vcc through current limiting resistors). It may also be configured as a 1 Meg x 20 bit memory array, provided the corresponding DQs on the host system are made common and memory bank control procedures are implemented. Separate $\overline{CAS}$ inputs allow byte accesses.

All inputs to the DRAMs are buffered, with the exception of $\overline{RAS}$. The line drivers used for buffers reduce reflections on the card and ensure compatibility in a wide range of systems. At the same time, the line drivers add delays to the buffered input timings when compared to standard DRAMs.

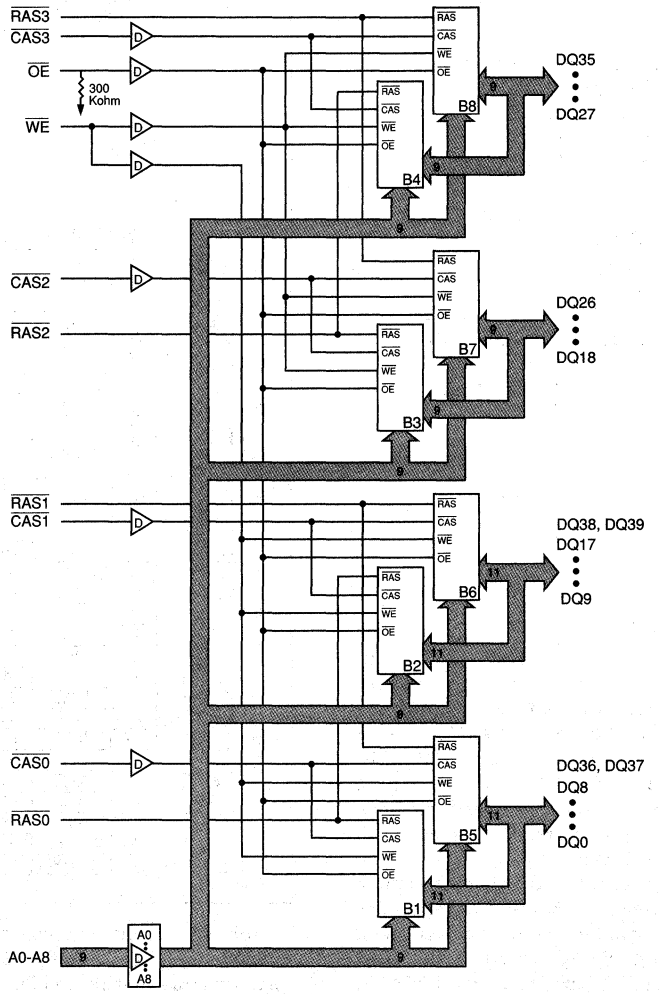
The MT24D88C51240 is designed for low power operation using 256K x 4 low power, extended refresh DRAMs. These devices support BATTERY BACKUP (BBU) cycle refresh; a very low current, data retention mode. Standard component DRAM refresh modes are supported as well.

Multiple $\overline{RAS}$ inputs conserve power by allowing individual bank selection. In the x32/36/40 organization, the memory array may be divided into two banks, each with four separate bytes (x32/36 only). In the x16/18/20 organization, up to four banks, each with two separate bytes, may be independently selected. One bank is activated by each $\overline{RAS}$ selection; the others not selected remain in standby mode, drawing minimum power.

Eight presence detect pins may be read by the host to identify the MT24D88C51240 organization, number of banks, access time and refresh mode. These extensive presence detect functions allow systems to utilize the advanced power saving features.

The MT24D88C51240 is built with a plastic frame covered by stainless steel panels. This package, containing an 88-pin receptacle connector, is keyed to prevent improper installation or insertion into other types of IC card sockets.

FUNCTIONAL BLOCK DIAGRAM



NOTE: 1. D = 74AC11244 line drivers.
2. B1, B2, B5 and B6 = 256K x 11 memory blocks; B3, B4, B7 and B8 = 256K x 9 memory blocks.
3. $\overline{OE}$ is internally connected to ground via a 300 Kohm resistor and is also buffered to DRAM.

PIN DESCRIPTIONS

PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
22, 26, 65, 69	$\overline{RAS}$0-3	Input	Row Address Strobe: $\overline{RAS}$ is used to clock-in the 9 row-address bits. Four $\overline{RAS}$ inputs allow for two x32/36/40 banks or four x16/18/20 banks.
23, 24, 66, 68	$\overline{CAS}$0-3	Input	Column Address Strobe: $\overline{CAS}$ is used to clock-in the 9 column-address bits, enable the DRAM output buffers, and strobe the data inputs on WRITE cycles. Four $\overline{CAS}$ inputs allow byte access control for any memory bank configuration (not in x40 mode).
70	$\overline{WE}$	Input	Write Enable: $\overline{WE}$ is the READ/WRITE control for the DQ pins. If $\overline{WE}$ is LOW prior to $\overline{CAS}$ going LOW, the access is an EARLY-WRITE cycle. If $\overline{WE}$ is HIGH while $\overline{CAS}$ is LOW, the access is a READ cycle, provided $\overline{OE}$ is also LOW. If WE goes LOW after $\overline{CAS}$ goes LOW, then the cycle is a LATE-WRITE cycle. A LATE-WRITE cycle is generally used in conjuction with a READ cycle to form a READ-MODIFY-WRITE cycle.
55	$\overline{OE}$	Input	Output Enable: $\overline{OE}$ is the input/output control for the DQ pins. $\overline{OE}$ is connected to ground through a 300 Kohm resistor and is intended to be LOW allowing for EARLY-WRITE cycles only. This signal may be driven, allowing for LATE-WRITE cycles.
13, 57, 14, 58, 16, 59, 18, 60, 19	A0-A8	Input	Address Inputs: These inputs are multiplexed and clocked by $\overline{RAS}$ and $\overline{CAS}$.
2-8, 10, 12, 34, 36, 38-43, 33, 46-54, 80-87, 79, 31, 32, 77, 78	DQ0-DQ39	Input/ Output	Data I/O: For WRITE cycles, DQ0-DQ39 act as inputs to the addressed DRAM location. BYTE WRITEs may be performed by using the corresponding $\overline{CAS}$ select (x32/36 mode only). For READ access cycles, DQ0-DQ39 act as outputs for the addressed DRAM location.
71, 28, 72, 29, 74, 30, 75, 76	PD1-PD8	-	Presence Detect: These pins are read by the host system and tell the system the card's personality. They will be either left floating (NC) or they will be grounded (Vss).
11, 17, 20, 21, 25, 35, 61, 62, 64	NC	-	No Connect: These pins should be left unconnected (reserved for future use).
9, 15, 27, 37	Vcc	Supply	Power Supply: +5V ±5%
1, 44, 45, 56, 63, 67, 73, 88	Vss	Supply	Ground

FUNCTIONAL DESCRIPTION

The MT24D88C51240 is a 2 megabyte memory card structured as a 512K x 32/36/40 bit memory array ($\overline{RAS0}$ = $\overline{RAS2}$, $\overline{RAS1}$ = $\overline{RAS3}$). It also may be configured as a 1 Meg x 16/18/20 bit memory array provided the corresponding DQs on the host are connected and memory bank control procedures are implemented by interleaving all four $\overline{RAS}$ lines.

Most x32/36/40 bit applications use the same signal to control the $\overline{CAS}$ inputs. $\overline{RAS0}$ and $\overline{RAS1}$ control the lower 16/18 bits, and $\overline{RAS2}$ and $\overline{RAS3}$ control the upper 16/18 bits to obtain a x32/36 memory array. For x16/18 applications, the corresponding DQs and the corresponding $\overline{CAS}$ pins must be connected together (DQ0 to DQ18, DQ1 to DQ19 and so forth, and $\overline{CAS0}$ to $\overline{CAS2}$ and $\overline{CAS1}$ to $\overline{CAS3}$). Each $\overline{RAS}$ is then a bank select for the 1 Meg x 16/18 memory organization.

DRAM OPERATION

DRAM REFRESH

Memory cell data is retained in its correct state by maintaining power and executing any $\overline{RAS}$ cycle [READ, WRITE, $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$ (CBR), HIDDEN or BATTERY BACKUP (BBU) REFRESH] so that all 512 combinations of $\overline{RAS}$ addresses (A0-A8) are executed at least every 64ms, regardless of sequence.

The implied method of choice for refreshing the memory card is the BBU cycle. This is a very low current, data retention mode made possible by using the CBR REFRESH cycle over the extended refresh range (I_{CC7}).

The memory card may be used with the other refresh modes common in standard DRAMs. This allows the memory card to be used on existing systems that do not utilize the BBU REFRESH cycle. However, the memory card will draw more current in the STANDBY mode. The CBR REFRESH mode is recommended when not using the BBU mode.

DRAM READ AND WRITE CYCLES

During READ or WRITE cycles, each bit is uniquely addressed through the 18 address bits, which are entered 9 bits (A0-A8) at a time. $\overline{RAS}$ is used to latch the first 9 bits and $\overline{CAS}$ the latter 9 bits. READ or WRITE cycles are selected with the $\overline{WE}$ input. A logic HIGH on $\overline{WE}$ dictates READ mode while a logic LOW on $\overline{WE}$ dictates WRITE mode. During a WRITE cycle, data in (D) is latched by the falling edge of $\overline{CAS}$. $\overline{WE}$ must fall prior to $\overline{CAS}$ (EARLY WRITE); if $\overline{WE}$ goes LOW after $\overline{CAS}$, the outputs (Q) will be activated and will drive invalid data to the inputs. The data inputs and data outputs are routed through pins using common I/O, and pin direction is controlled by $\overline{WE}$.

FAST PAGE MODE operation allows faster data operations (READ or WRITE) within a row address (A0-A8) defined page boundary. The FAST PAGE MODE cycle is always initiated with a row address strobed-in by $\overline{RAS}$ followed by a column address strobed-in by $\overline{CAS}$. $\overline{CAS}$ may be toggled-in by holding $\overline{RAS}$ LOW and strobing-in different column addresses, thus executing faster memory cycles. Returning $\overline{RAS}$ HIGH terminates the FAST PAGE MODE operation. Returning $\overline{RAS}$ and $\overline{CAS}$ HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the $\overline{RAS}$ high time.

DRAM TIMING

In accordance with JEDEC standard specifications, all inputs to the IC DRAM card are buffered, with the exception of $\overline{RAS}$ inputs. The line drivers used for buffers reduce reflections on the card and ensure compatibility in a wide range of systems. The implementation of buffers on the card may relieve the need for additional host system line drivers. Notes 23 though 29 indicate which parameters on the IC DRAM card are affected by the line drivers, and to what magnitude they are affected. The component DRAM timing specifications, rather than those of the IC DRAM card (in systems that use both), may cause timing incompatibilities.

All traces on the IC DRAM card (buffered and non-buffered) are approximately 50 ohms characteristic impedance. Matching impedance on the system board to 50 ohms characteristic impedance on traces to the IC DRAM card will decrease signal noise to the IC DRAM card, enhancing overall system reliability.

PHYSICAL DESIGN

The MT24D88C51240 is constructed with a molded plastic frame and covered with stainless steel panels. Inside, four thin small-outline package (TSOP) DRAMs are mounted on both sides of an ultrathin printed circuit board. The board is attached to a high insertion, 88-pin receptacle connector. The package has a polarized key to prevent improper installation, including insertion into other types of IC card sockets. The MT24D88C51240 operates reliably up to 55°C.

MEMORY TRUTH TABLE

FUNCTION		RAS	CAS	WE	OE	ADDRESSES tR	ADDRESSES tC	DATA IN/OUT DQ0-DQ39
Standby		H	H→X	X	X	X	X	High-Z
READ		L	L	H	L (NC)	ROW	COL	Data Out
EARLY-WRITE		L	L	L	X	ROW	COL	Data In
READ-WRITE		L	L	H→L	L→H	ROW	COL	Data Out
FAST-PAGE-MODE	1st Cycle	L	H→L	H	L (NC)	ROW	COL	Data Out
READ	2nd Cycle	L	H→L	H	L (NC)	n/a	COL	Data Out
FAST-PAGE-MODE	1st Cycle	L	H→L	L	X	ROW	COL	Data In
EARLY-WRITE	2nd Cycle	L	H→L	L	X	n/a	COL	Data In
FAST-PAGE-MODE	1st Cycle	L	H→L	H→L	L→H	ROW	COL	Data In
READ-WRITE	2nd Cycle	L	H→L	H→L	L→H	n/a	COL	Data In
RAS-ONLY REFRESH		L	X	X	X	ROW	n/a	High-Z
HIDDEN	READ	L→H→L	L	H	L (NC)	ROW	COL	Data Out
REFRESH	WRITE	L→H→L	L	L	X	ROW	COL	Data In
CAS-BEFORE-RAS REFRESH		H→L	L	H	X	X	X	High-Z
BATTERY BACKUP REFRESH		H→L	L	H	X	X	X	High-Z

PRESENCE DETECT TRUTH TABLE

CHARACTERISTICS						PRESENT DETECT PIN (PDx)							
Card Density	DRAM Organizations	Card Address	RAS Address	CAS Address	Page Depth	1	2	3	4	5	6	7	8
0MB	No card installed	X	X	X	X	NC	NC	NC	NC	NC	X	X	X
1MB	256K x 1, 4, 16, 18	18	9	9	512	Vss	Vss	Vss	Vss	NC	X	X	X
• 2MB	256K x 1, 4, 16, 18	18	9	9	512	Vss	Vss	Vss	Vss	Vss	X	X	X
2MB	512K x 8, 9	19	10	9	512	NC	Vss	Vss	Vss	NC	X	X	X
4MB	512K x 8, 9	19	10	9	512	NC	Vss	Vss	Vss	Vss	X	X	X
4MB	1 Meg x 1, 4, 16, 18	20	10	10	1,024	Vss	NC	Vss	Vss	NC	X	X	X
8MB	1 Meg x 1, 4, 16, 18	20	10	10	1,024	Vss	NC	Vss	Vss	Vss	X	X	X
8MB	2 Meg x 8, 9	21	11	10	1,024	NC	NC	Vss	Vss	NC	X	X	X
16MB	2 Meg x 8, 9	21	11	10	1,024	NC	NC	Vss	Vss	Vss	X	X	X
16MB	4 Meg x 1, 4, 16, 18	22	12	11	1,024	Vss	Vss	NC	Vss	NC	X	X	X
32MB	4 Meg x 1, 4, 16, 18	22	12	11	1,024	Vss	Vss	NC	Vss	Vss	X	X	X
Access Timing		100ns				X	X	X	X	X	Vss	Vss	X
		80ns				X	X	X	X	X	NC	Vss	X
		70ns				X	X	X	X	X	Vss	NC	X
		60ns				X	X	X	X	X	NC	NC	X
		50ns				X	X	X	X	X	Vss	Vss	X
Refresh Control		Standard				X	X	X	X	X	X	X	NC
		Auto				X	X	X	X	X	X	X	Vss

NOTE: Vss = Ground.

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} .....-0.5V to +5.25V
Operating Temperature, T_A (Ambient) .....0°C to +55°C
Storage Temperature .....-20°C to +80°C
Power Dissipation 15W
Short Circuit Output Current 50mA
Card Insertions (Connector's Life Cycle) 10,000

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 3, 4, 6, 7) (0°C ≤ T_A ≤ 55°C; V_{CC} = 5V ±5%)

PARAMETER/CONDITION		SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage		V_{CC}	4.75	5.25	V	1
Input High (Logic 1) Voltage, All Inputs		V_{IH}	3.5	V_{CC}+0.5	V	1
Input Low (Logic 0) Voltage, All Inputs		V_{IL}	-0.5	0.8	V	1
INPUT LEAKAGE CURRENT, Any input	Non-buffered	I_{IN}	-12	12	µA	
(0V ≤ V_{IN} ≤ 5.25V; all other pins not under test = 0V)	Buffered	I_{IB}	-2	2	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled; 0V ≤ V_{OUT} ≤ 5.25V)		I_{OZ}	-10	10	µA	
OUTPUT LEVELS Output High Voltage (I_{OUT} = -5mA)		V_{OH}	2.4		V	
Output Low Voltage (I_{OUT} = 4.2mA)		V_{OL}		0.4	V	

		MAX				
PARAMETER/CONDITION	SYMBOL	-6	-7	-8	UNITS	NOTES
STANDBY CURRENT: (TTL) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC1}	48	48	48	mA	
STANDBY CURRENT: (CMOS) ($\overline{RAS}$ = $\overline{CAS}$ = Other Inputs = V_{CC} -0.2V)	I_{CC2}	4.8	4.8	4.8	mA	
OPERATING CURRENT: Random READ/WRITE Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC (MIN))	I_{CC3}	1.0	0.9	0.8	A	3, 4, 30
OPERATING CURRENT: FAST PAGE MODE Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: ^tPC = ^tPC (MIN))	I_{CC4}	780	660	540	mA	3, 4, 30
REFRESH CURRENT: $\overline{RAS}$-ONLY Average power supply current ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}: ^tRC = ^tRC (MIN))	I_{CC5}	1.0	0.9	0.8	A	3, 30
REFRESH CURRENT: $\overline{CAS}$-BEFORE-$\overline{RAS}$ (CBR) Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC (MIN))	I_{CC6}	1.0	0.9	0.8	A	3, 5, 30
REFRESH CURRENT: BATTERY BACKUP (BBU) Average power supply current during BBU: $\overline{CAS}$ = 0.2V or CBR cycling; $\overline{RAS}$ = ^tRAS (MIN) up to 300ns; ^tRC = 125µs; $\overline{WE}$, A0-A8 and DQ = Vcc -0.2V or 0.2V (DQ may be left open)	I_{CC7}	4.8	4.8	4.8	mA	3, 5

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: $\overline{CAS0}$, $\overline{CAS1}$, $\overline{CAS2}$, $\overline{CAS3}$, A0-A8, $\overline{OE}$	C_{I1}		9	pF	2
Input Capacitance: $\overline{WE}$	C_{I2}		13	pF	2
Input Capacitance: $\overline{RAS0}$, $\overline{RAS1}$, $\overline{RAS2}$, $\overline{RAS3}$	C_{I3}		50	pF	2
Input/Output Capacitance: DQ	C_{IO}		20	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C ≤ T_A ≤ 55°C; Vcc = 5V ±5%)

AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	^tRC	110		130		150		ns	23
FAST-PAGE-MODE READ or WRITE cycle time	^tPC	40		40		45		ns	23
Access time from $\overline{RAS}$	^tRAC		60		70		80	ns	14, 23
Access time from $\overline{CAS}$	^tCAC		25		30		30	ns	15, 26
Access time from column address	^tAA		40		45		50	ns	26
Access time from $\overline{CAS}$ precharge	^tCPA		50		50		55	ns	26
$\overline{RAS}$ pulse width	^tRAS	60	100,000	70	100,000	80	100,000	ns	23
$\overline{RAS}$ pulse width (FAST PAGE MODE)	^tRASP	60	100,000	70	100,000	80	100,000	ns	23
$\overline{RAS}$ hold time	^tRSH	25		30		30		ns	26
$\overline{RAS}$ precharge time	^tRP	40		50		60		ns	23
$\overline{CAS}$ pulse width	^tCAS	15	100,000	20	100,000	20	100,000	ns	23
$\overline{CAS}$ hold time	^tCSH	55		65		75		ns	25
$\overline{CAS}$ precharge time	^tCPN	10		10		10		ns	16, 23
$\overline{CAS}$ precharge time (FAST PAGE MODE)	^tCP	10		10		10		ns	23
$\overline{RAS}$ to $\overline{CAS}$ delay time	^tRCD	10	35	15	40	15	50	ns	17, 28
$\overline{CAS}$ to $\overline{RAS}$ precharge time	^tCRP	15		15		15		ns	26
Row address setup time	^tASR	10		10		10		ns	26
Row address hold time	^tRAH	5		5		5		ns	25
$\overline{RAS}$ to column address delay time	^tRAD	10	20	10	25	10	30	ns	18, 28
Column address setup time	^tASC	5		5		5		ns	24
Column address hold time	^tCAH	15		20		20		ns	24
Column address hold time (referenced to $\overline{RAS}$)	^tAR	45		50		55		ns	25
Column address to $\overline{RAS}$ lead time	^tRAL	40		45		50		ns	26
Read command setup time	^tRCS	5		5		5		ns	25
Read command hold time (referenced to $\overline{CAS}$)	^tRCH	5		5		5		ns	19, 24
Read command hold time (referenced to $\overline{RAS}$)	^tRRH	-5		-5		-5		ns	19, 25
$\overline{CAS}$ to output in Low-Z	^tCLZ	5		5		5		ns	24
Output buffer turn-off delay	^tOFF	5	30	5	30	5	30	ns	20, 29, 35
$\overline{WE}$ command setup time	^tWCS	5		5		5		ns	24

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C ≤ T_A ≤ 55°C; Vcc = 5V ±5%)

AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Write command hold time	tWCH	15		20		20		ns	24
Write command hold time (referenced to $\overline{RAS}$)	tWCR	40		50		55		ns	25
Write command pulse width	tWP	10		15		15		ns	23
Write command to $\overline{RAS}$ lead time	tRWL	25		30		30		ns	26
Write command to $\overline{CAS}$ lead time	tCWL	20		25		25		ns	24
Data-in setup time	tDS	5		5		5		ns	24, 32
Data-in hold time	tDH	5		10		10		ns	25, 32
Data-in hold time (referenced to $\overline{RAS}$)	tDHR	45		55		60		ns	23
Transition time (rise or fall)	tT	2	15	2	15	2	15	ns	9, 10, 23
Refresh period (1,024 cycles)	tREF		128		128		128	ms	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	tRPC	10		10		10		ns	26
$\overline{CAS}$ setup time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	tCSR	20		20		20		ns	5, 26
$\overline{CAS}$ hold time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	tCHR	10		10		10		ns	5, 25
$\overline{WE}$ hold time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	tWRH	5		5		5		ns	22, 25
$\overline{WE}$ setup time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	tWRP	20		20		20		ns	22, 26
$\overline{WE}$ hold time (WCBR test cycle)	tWTH	5		5		5		ns	22, 25
$\overline{WE}$ setup time	tWTS	20		20		20		ns	22, 26
READ-WRITE cycle time	tRWC	165		185		205		ns	
FAST-PAGE-MODE READ-WRITE cycle time	tPRWC	90		95		100		ns	23
$\overline{RAS}$ to $\overline{WE}$ delay time	tRWD	80		90		100		ns	31, 27
Column Address to $\overline{WE}$ delay time	tAWD	65		70		75		ns	31, 24
$\overline{CAS}$ to $\overline{WE}$ delay time	tCWD	50		65		55		ns	31, 24
Output buffer turn-off delay	tOE		25		30		30	ns	20, 33, 26
Output disable	tOD		25		30		30	ns	35, 26
$\overline{OE}$ hold time from $\overline{WE}$ during READ-MODIFY-WRITE cycle	tOEH	5		10		10		ns	34, 27
$\overline{OE}$ hold time from $\overline{RAS}$ during HIDDEN REFRESH cycle	tORD	10		10		10		ns	21, 26

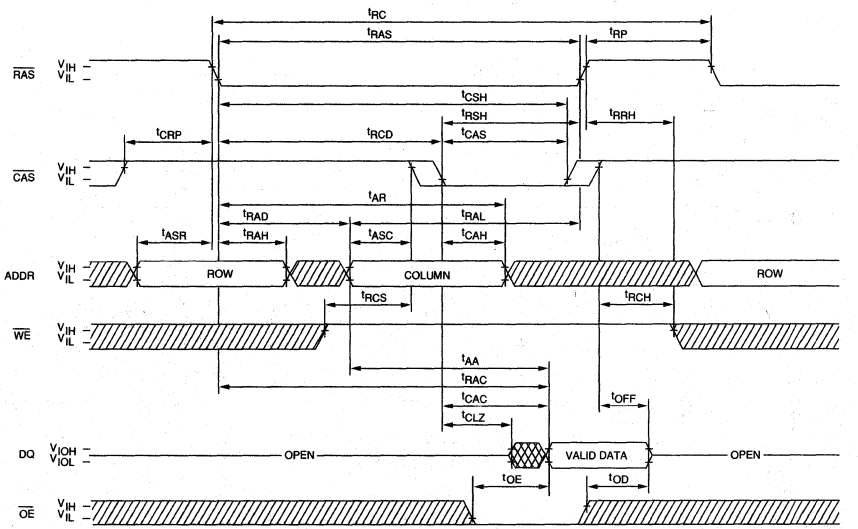
NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. V_{CC} = 5V ±10%, f = 1 MHz.
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is assured.
7. An initial pause of 100µs is required after power-up followed by eight $\overline{RAS}$ refresh cycles ($\overline{RAS}$-ONLY or CBR with $\overline{WE}$ HIGH) before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-up should be repeated any time the ^{t}REF refresh requirement is exceeded.
8. AC characteristics assume ^{t}T = 5ns.
9. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS}$ = V_{IH}, data output is High-Z.
12. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to 2 TTL gates and 100pF.
14. Assumes that $^{t}RCD < {}^{t}RCD$ (MAX). If ^{t}RCD is greater than the maximum recommended value shown in this table, ^{t}RAC will increase by the amount that ^{t}RCD exceeds the value shown.
15. Assumes that $^{t}RCD \geq {}^{t}RCD$ (MAX).
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer, $\overline{CAS}$ must be pulsed HIGH for ^{t}CPN.
17. Operation within the ^{t}RCD (MAX) limit ensures that ^{t}RAC (MAX) can be met. ^{t}RCD (MAX) is specified as a reference point only; if ^{t}RCD is greater than the specified ^{t}RCD (MAX) limit, then access time is controlled exclusively by ^{t}CAC.
18. Operation within the ^{t}RAD (MAX) limit ensures that ^{t}RCD (MAX) can be met. ^{t}RAD (MAX) is specified as a reference point only; if ^{t}RAD is greater than the specified ^{t}RAD (MAX) limit, then access time is controlled exclusively by ^{t}AA.
19. Either ^{t}RCH or ^{t}RRH must be satisfied for a READ cycle.
20. ^{t}OFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
21. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW.
22. ^{t}WTS and ^{t}WTH are setup and hold specifications for the $\overline{WE}$ pin being held LOW to enable the JEDEC test mode (with CBR timing constraints). These two parameters are the inverse of ^{t}WRP and ^{t}WRH in the CBR refresh cycle.
23. Timing between the DRAMs and the DRAM card did not change with the addition of the line drivers.
24. A +5ns timing skew from the DRAM to the DRAM card resulted from the addition of line drivers.
25. A -5ns timing skew from the DRAM to the DRAM card resulted from the addition of line drivers.
26. A +10ns timing skew from the DRAM to the DRAM card resulted from the addition of line drivers.
27. A -10ns timing skew from the DRAM to the DRAM card resulted from the addition of line drivers.
28. A -5ns (MIN) and a -10ns (MAX) timing skew from the DRAM to the DRAM card resulted from the addition of line drivers.
29. A +5ns (MIN) and a +10ns (MAX) timing skew from the DRAM to the DRAM card resulted from the addition of line drivers.
30. The maximum current ratings are based with the memory operating or being refreshed in the x32/36/40 mode. The stated maximums may be reduced by one half when used in the x16/18/20 mode.
31. ^{t}WCS, ^{t}RWD, ^{t}AWD and ^{t}CWD are restrictive operating parameters in late WRITE, and READ-MODIFY-WRITE cycles only. If $^{t}WCS \geq {}^{t}WCS$ (MIN), the cycle is an EARLY-WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If $^{t}RWD \geq {}^{t}RWD$ (MIN), $^{t}AWD \geq {}^{t}AWD$ (MIN) and $^{t}CWD \geq {}^{t}CWD$ (MIN), the cycle is a READ-MODIFY-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of data out is indeterminate. $\overline{OE}$ held HIGH and $\overline{WE}$ taken LOW after $\overline{CAS}$ goes LOW results in a LATE-WRITE ($\overline{OE}$ controlled) cycle.

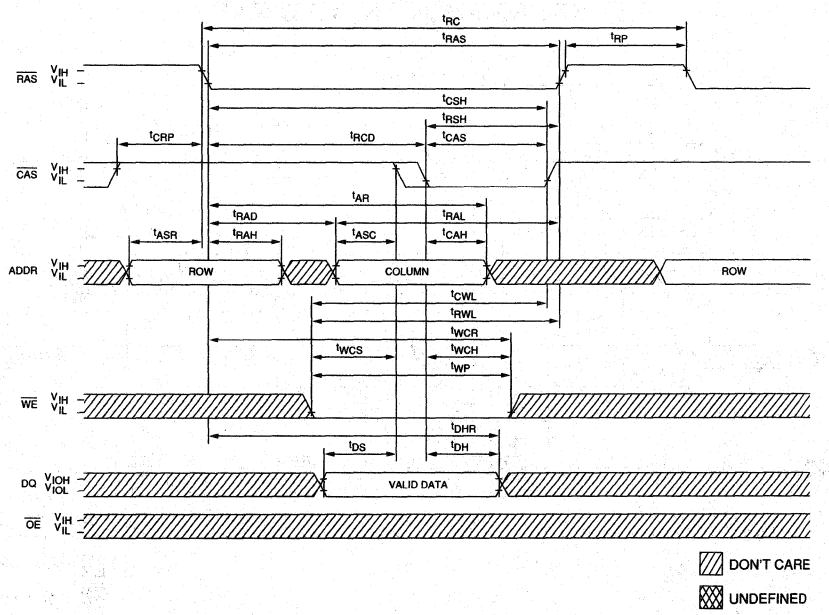
NOTES (continued)

32. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY-WRITE cycles and $\overline{WE}$ leading edge in LATE-WRITE or READ-MODIFY-WRITE cycles.
33. If $\overline{OE}$ is tied permanently LOW, LATE-WRITE or READ-MODIFY-WRITE operations are not possible.
34. LATE-WRITE and READ-MODIFY-WRITE cycles must have both ^{t}OD and ^{t}OEH met ($\overline{OE}$ HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. The DQs will provide the previously read data if $\overline{CAS}$ remains LOW and $\overline{OE}$ is taken back LOW after ^{t}OEH is met. If $\overline{CAS}$ goes HIGH prior to $\overline{OE}$ going back LOW, the DQs will remain open.
35. The DQs open during READ cycles once ^{t}OD or ^{t}OFF occur. If $\overline{CAS}$ goes HIGH first, $\overline{OE}$ becomes a "don't care." If $\overline{OE}$ goes HIGH and $\overline{CAS}$ stays LOW, $\overline{OE}$ is not a "don't care;" and the DQs will provide the previously read data if $\overline{OE}$ is taken back LOW (while $\overline{CAS}$ remains LOW).

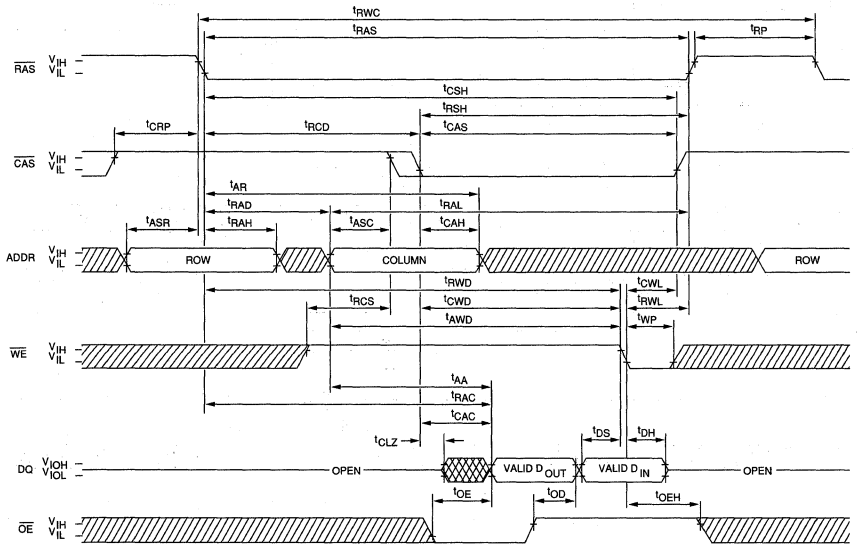
READ CYCLE



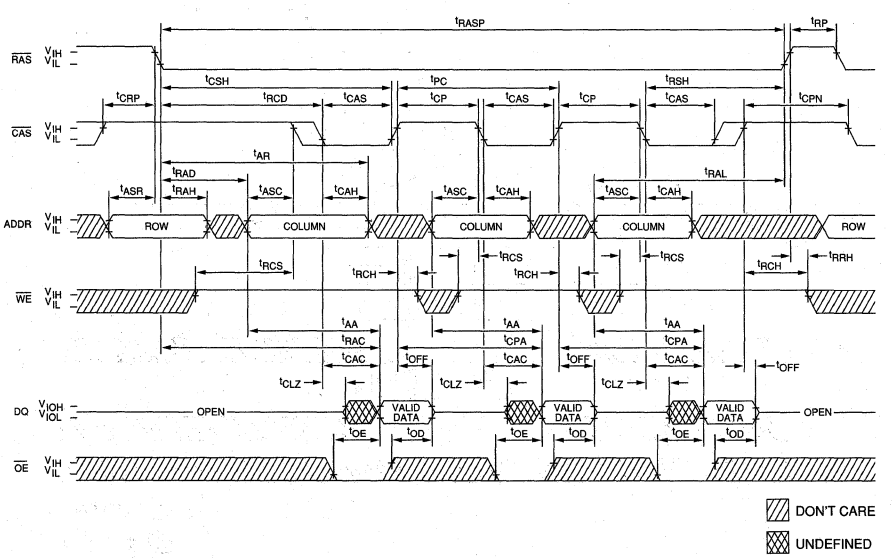
EARLY-WRITE CYCLE



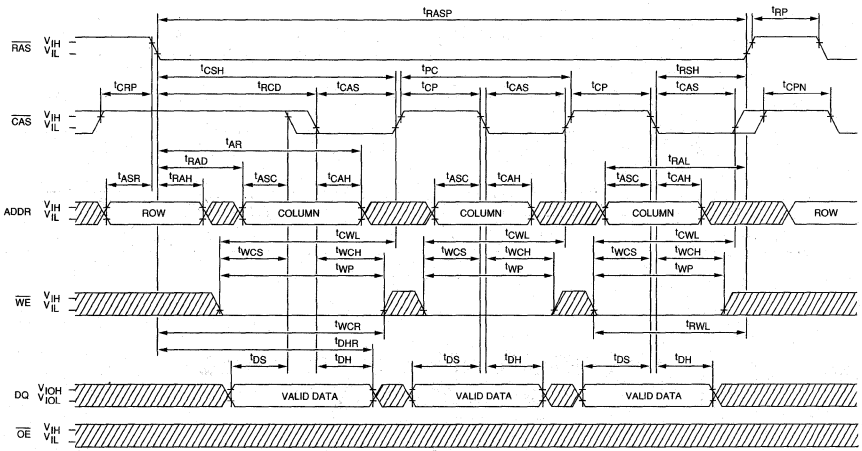
READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)



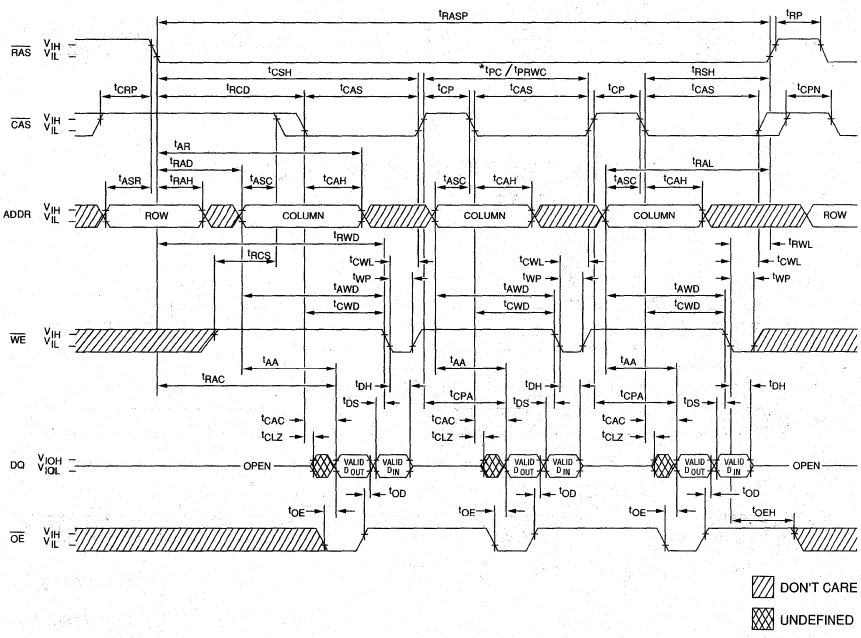
FAST-PAGE-MODE READ CYCLE



FAST-PAGE-MODE EARLY-WRITE CYCLE

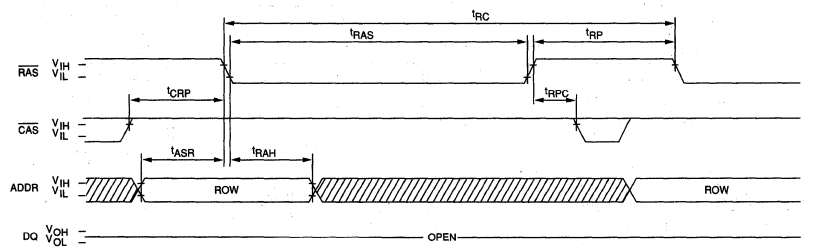


FAST-PAGE-MODE READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)

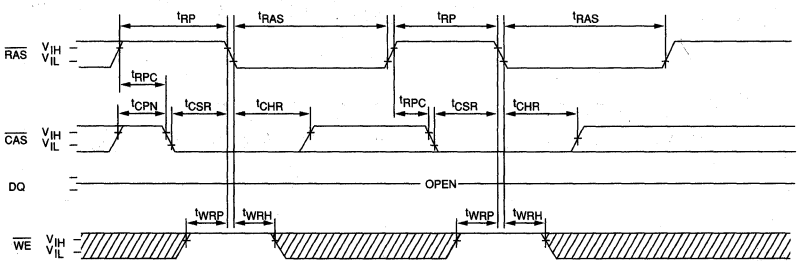


NEW ■ IC DRAM CARD

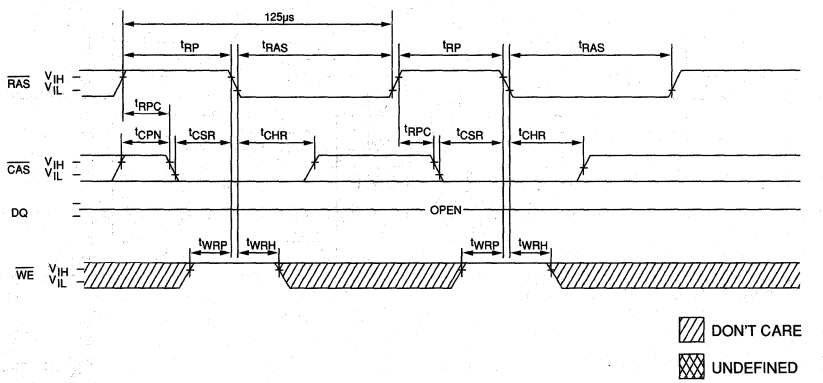
$\overline{RAS}$-ONLY REFRESH CYCLE
(ADDR = A0-A8; $\overline{WE}$ = DON'T CARE)



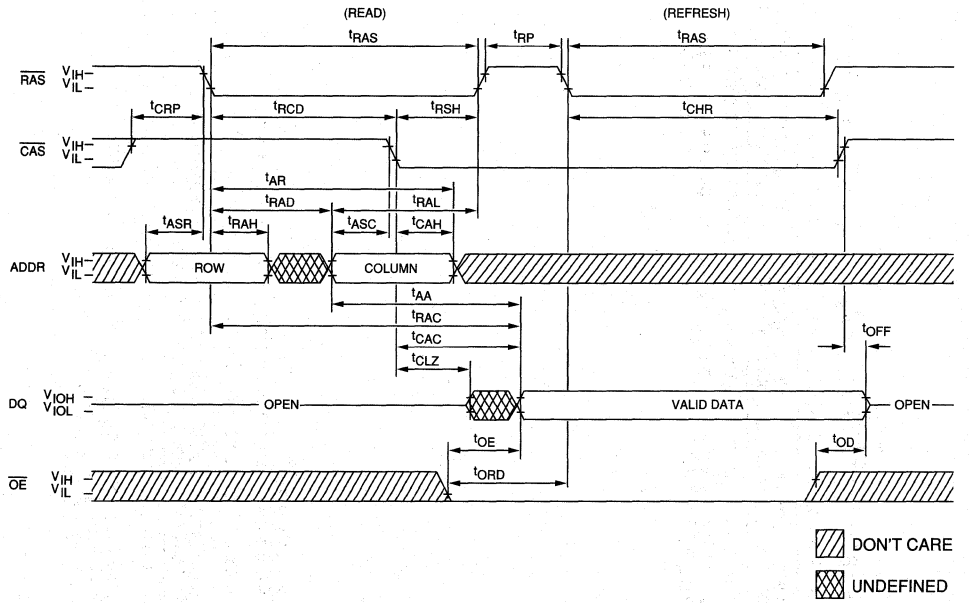
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE
(A0-A8 = DON'T CARE)



BATTERY BACKUP REFRESH CYCLE
(A0-A8 = DON'T CARE)

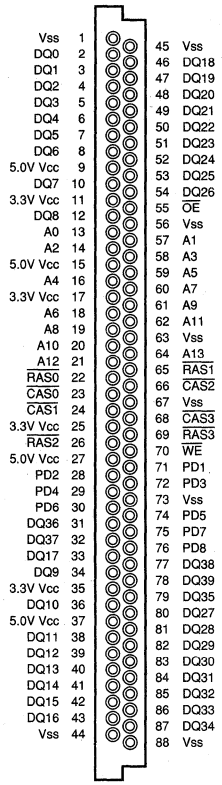


HIDDEN REFRESH CYCLE [21]
($\overline{WE}$ = HIGH)

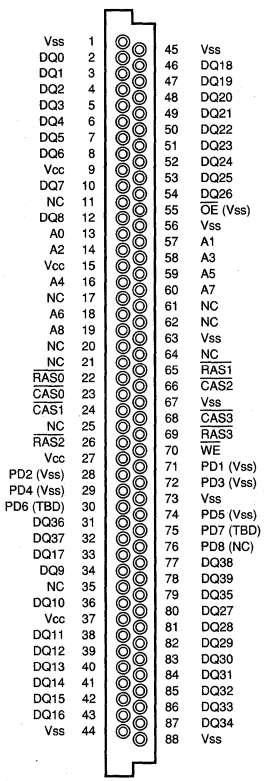


NEW ■ IC DRAM CARD

RESERVED JEDEC, JEIDA and PCMCIA 88-PIN ASSIGNMENT
(All Possible Combinations)



MT24D88C51240 PIN ASSIGNMENT
(JEDEC Standard)



IC DRAM CARD

4 MEGABYTES

1 MEG x 40, 2 MEG x 20

NEW ■ IC DRAM CARD

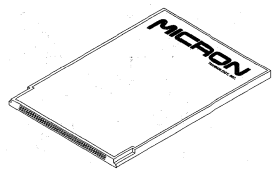
FEATURES

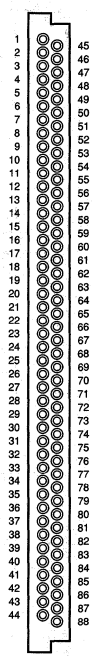
- JEIDA, JEDEC and PCMCIA standard 88-pin IC DRAM card
- Polarized receptacle connector
- Industry standard DRAM functions and timing
- High-performance, CMOS silicon-gate process
- All outputs are fully TTL compatible
- All inputs buffered except $\overline{RAS}$ inputs
- Multiple $\overline{RAS}$ inputs for x16/18/20 or x32/36/40 selectability
- Refresh modes: $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$ (CBR), HIDDEN and BATTERY BACKUP (BBU)
- FAST PAGE MODE access cycle
- Single +5V ±5% power supply
- Low power; 12mW standby, 3.3W active (typical)
- Extended refresh standard: 1,024 cycles every 128ms

OPTIONS / MARKING

• Timing	
60ns access	-6
70ns access	-7
80ns access	-8

PIN ASSIGNMENT (End View)
88-Pin Card (U-1)





PIN #	SYMBOL	PIN #	SYMBOL	PIN #	SYMBOL
1	Vss	31	DQ36	61	A9
2	DQ0	32	DQ37	62	NC
3	DQ1	33	DQ17	63	Vss
4	DQ2	34	DQ9	64	NC
5	DQ3	35	NC	65	NC
6	DQ4	36	DQ10	66	$\overline{CAS2}$
7	DQ5	37	Vcc	67	Vss
8	DQ6	38	DQ11	68	$\overline{CAS3}$
9	Vcc	39	DQ12	69	NC
10	DQ7	40	DQ13	70	$\overline{WE}$
11	NC	41	DQ14	71	PD1 (Vss)
12	DQ8	42	DQ15	72	PD3 (Vss)
13	A0	43	DQ16	73	Vss
14	A2	44	Vss	74	PD5 (NC)
15	Vcc	45	Vss	75	PD7 (TBD)
16	A4	46	DQ18	76	PD8 (NC)
17	NC	47	DQ19	77	DQ38
18	A6	48	DQ20	78	DQ39
19	A8	49	DQ21	79	DQ35
20	NC	50	DQ22	80	DQ27
21	NC	51	DQ23	81	DQ28
22	$\overline{RAS0}$	52	DQ24	82	DQ29
23	$\overline{CAS0}$	53	DQ25	83	DQ30
24	$\overline{CAS1}$	54	DQ26	84	DQ31
25	NC	55	$\overline{OE}$ (Vss)	85	DQ32
26	$\overline{RAS2}$	56	Vss	86	DQ33
27	Vcc	57	A1	87	DQ34
28	PD2 (NC)	58	A3	88	Vss
29	PD4 (Vss)	59	A5		
30	PD6 (TBD)	60	A7		

GENERAL DESCRIPTION

The MT12D88C140 is a 4 megabyte, IC DRAM card organized primarily as a 1 Meg x 40 bit memory array for EDC applications. It may be used as a x32 or x36 bit memory array (the unused DQs should be tied to Vss or Vcc through current limiting resistors). It may also be configured as a 2 Meg x 20 bit memory array, provided the corresponding DQs on the host system are made common, and memory bank control procedures are implemented. Separate $\overline{CAS}$ inputs allow byte accesses.

All inputs to the DRAMs are buffered, with the exception of $\overline{RAS}$. The line drivers used for buffers reduce reflections on the card and ensure compatibility in a wide range of systems. At the same time, the line drivers add delays to the buffered input timings when compared to standard DRAMs.

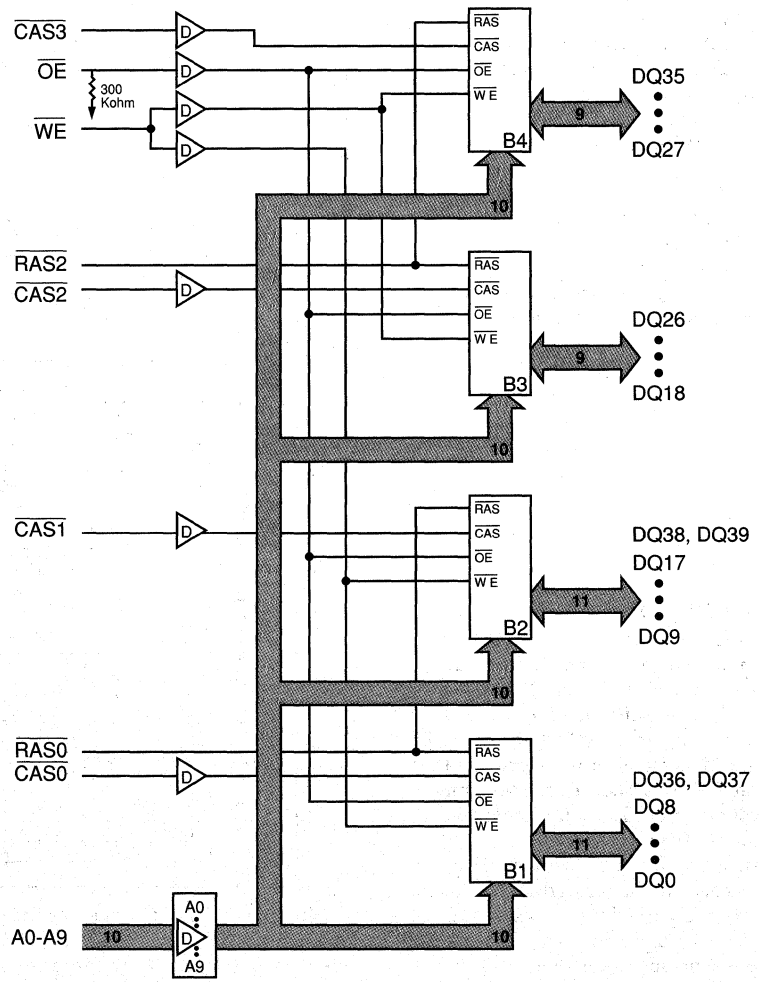
The MT12D88C140 is designed for low power operation using 1 Meg x 4 low power, extended refresh DRAMs. These devices support BATTERY BACKUP (BBU) cycle refresh; a very low current, data retention mode. Standard component DRAM refresh modes are supported as well.

Multiple $\overline{RAS}$ inputs conserve power by allowing individual bank selection. In the x32/36/40 organization, the memory is a single array that may be divided into four separate bytes (x32/36 only). In the x16/18/20 organization, up to two banks, each with two separate bytes, may be independently selected. One bank is activated by each $\overline{RAS}$ selection; the others not selected remain in standby mode, drawing minimum power.

Eight presence detect pins may be read by the host to identify the MT12D88C140 organization, number of banks, access time and refresh mode. These extensive presence detect functions allow systems to utilize the advanced power saving features.

The MT12D88C140 is built with a plastic frame covered by stainless steel panels. This package, containing an 88-pin receptacle connector, is keyed to prevent improper installation or insertion into other types of IC card sockets.

FUNCTIONAL BLOCK DIAGRAM



NOTE:
1. D = 74AC11244 line drivers.
2. B1 and B2 = 1 Meg x 11 memory blocks; B3 and B4 = 1 Meg x 9 memory blocks.
3. $\overline{OE}$ is internally connected to ground via a 300 Kohm resistor and is also buffered to DRAM.

PIN DESCRIPTIONS

PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
22, 26	$\overline{RAS0}$, $\overline{RAS2}$	Input	Row Address Strobe: $\overline{RAS}$ is used to clock-in the 10 row-address bits. Two $\overline{RAS}$ inputs allow for a single x32/36/40 bank or two x16/18/20 banks.
23, 24, 66, 68	$\overline{CAS}$0-3	Input	Column Address Strobe: $\overline{CAS}$ is used to clock-in the 10 column-address bits, enable the DRAM output buffers, and strobe the data inputs on WRITE cycles. Four $\overline{CAS}$ inputs allow byte access control for any memory bank configuration (not in x40 mode).
70	$\overline{WE}$	Input	Write Enable: $\overline{WE}$ is the READ/WRITE control for the DQ pins. If $\overline{WE}$ is LOW prior to $\overline{CAS}$ going LOW, the access is an EARLY-WRITE cycle. If $\overline{WE}$ is HIGH while $\overline{CAS}$ is LOW, the access is a READ cycle, provided $\overline{OE}$ is also LOW. If WE goes LOW after $\overline{CAS}$ goes LOW, then the cycle is a LATE-WRITE cycle. A LATE-WRITE cycle is generally used in conjuction with a READ cycle to form a READ-MODIFY-WRITE cycle.
55	$\overline{OE}$	Input	Output Enable: $\overline{OE}$ is the input/output control for the DQ pins. $\overline{OE}$ is connected to ground through a 300 Kohm resistor and is intended to be LOW allowing for EARLY-WRITE cycles only. This signal may be driven, allowing for LATE-WRITE cycles.
13, 57, 14, 58, 16, 59, 18, 60, 19, 61	A0-A9	Input	Address Inputs: These inputs are multiplexed and clocked by $\overline{RAS}$ and $\overline{CAS}$.
2-8, 10, 12, 34, 36, 38-43, 33, 46-54, 80-87, 79, 31, 32, 77, 78	DQ0-DQ39	Input/ Output	Data I/O: For WRITE cycles, DQ0-DQ39 act as inputs to the addressed DRAM location. BYTE WRITEs may be performed by using the corresponding $\overline{CAS}$ select (x32/36 mode only). For READ access cycles, DQ0-DQ39 act as outputs for the addressed DRAM location.
71, 28, 72, 29, 74, 30, 75, 76	PD1-PD8	-	Presence Detect: These pins are read by the host system and tell the system the card's personality. They will be either left floating (NC) or they will be grounded (Vss).
11, 17, 20, 21, 25, 35, 62, 64, 65, 69	NC	-	No Connect: These pins should be left unconnected (reserved for future use).
9, 15, 27, 37	Vcc	Supply	Power Supply: +5V ±5%
1, 44, 45, 56, 63, 67, 73, 88	Vss	Supply	Ground

FUNCTIONAL DESCRIPTION

The MT12D88C140 is a 4 megabyte memory card as a 1 Meg x 32/36/40 bit memory array ($\overline{RAS0}$ = $\overline{RAS2}$). It also may be configured as a 2 Meg x 16/18/20 bit memory array provided the corresponding DQs on the host are connected and memory bank control procedures are implemented by interleaving both $\overline{RAS}$ lines.

Most x32/36/40 bit applications use the same signal to control the $\overline{CAS}$ inputs. $\overline{RAS0}$ controls the lower 16/18 bits and $\overline{RAS2}$ controls the upper 16 bits to obtain a x32/36 memory array. For x16/18 applications, the corresponding DQs and the corresponding $\overline{CAS}$ pins must be connected together (DQ0 to DQ18, DQ1 to DQ19 and so forth, and $\overline{CAS0}$ to $\overline{CAS2}$ and $\overline{CAS1}$ to $\overline{CAS3}$). Each $\overline{RAS}$ is then a bank select for the 2 Meg x 16/18 memory organization.

DRAM OPERATION

DRAM REFRESH

Memory cell data is retained in its correct state by maintaining power and executing any $\overline{RAS}$ cycle [READ, WRITE, $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$ (CBR), HIDDEN or BATTERY BACKUP (BBU) REFRESH] so that all 1,024 combinations of $\overline{RAS}$ addresses (A0-A9) are executed at least every 128ms, regardless of sequence.

The implied method of choice for refreshing the memory card is the BBU cycle. This is a very low current, data retention mode made possible by using the CBR REFRESH cycle over the extended refresh range (I_{CC7}).

The memory card may be used with the other refresh modes common in standard DRAMs. This allows the memory card to be used on existing systems that do not utilize the BBU REFRESH cycle. However, the penalty is the memory card will draw more current in the STANDBY mode. The CBR REFRESH mode is recommended when not using the BBU mode.

DRAM READ AND WRITE CYCLES

During READ or WRITE cycles, each bit is uniquely addressed through the 20 address bits, which are entered 10 bits (A0-A9) at a time. $\overline{RAS}$ is used to latch the first 10 bits and $\overline{CAS}$ the latter 10 bits. READ or WRITE cycles are selected with the $\overline{WE}$ input. A logic HIGH on $\overline{WE}$ dictates READ mode while a logic LOW on $\overline{WE}$ dictates WRITE mode. During a WRITE cycle, data in (D) is latched by the falling edge of $\overline{CAS}$. $\overline{WE}$ must fall prior to $\overline{CAS}$ (EARLY WRITE); if $\overline{WE}$ goes LOW after $\overline{CAS}$, the outputs (Q) will be activated and will drive invalid data to the inputs, unless LATE-WRITE CYCLE timing specifications are met. The data inputs and data outputs are routed through pins using common I/O, and pin direction is controlled by $\overline{WE}$.

FAST PAGE MODE operation allows faster data operations (READ or WRITE) within a row address (A0-A9) defined page boundary. The FAST PAGE MODE cycle is always initiated with a row address strobed-in by $\overline{RAS}$ followed by a column address strobed-in by $\overline{CAS}$. $\overline{CAS}$ may be toggled-in by holding $\overline{RAS}$ LOW and strobing-in different column addresses, thus executing faster memory cycles. Returning $\overline{RAS}$ HIGH terminates the FAST PAGE MODE operation. Returning $\overline{RAS}$ and $\overline{CAS}$ HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the $\overline{RAS}$ high time.

DRAM TIMING

In accordance with JEDEC standard specifications, all inputs to the IC DRAM card are buffered, with the exception of $\overline{RAS}$ inputs. The line drivers used for buffers reduce reflections on the card and ensure compatibility in a wide range of systems. The implementation of buffers on the card may relieve the need for additional host system line drivers. Notes 23 though 29 indicate which parameters on the IC DRAM card are affected by the line drivers, and to what magnitude they are affected. The component DRAM timing specifications, rather than those of the IC DRAM card (in systems that use both), may cause timing incompatibilities.

All traces on the IC DRAM card (buffered and non-buffered) are approximately 50 ohms characteristic impedance. Matching impedance on the system board to 50 ohms characteristic impedance on traces to the IC DRAM card will decrease signal noise to the IC DRAM card, enhancing overall system reliability.

PHYSICAL DESIGN

The MT12D88C140 is constructed with a molded plastic frame and covered with stainless steel panels. Inside, 12 thin small-outline package (TSOP) DRAMs are mounted on an ultrathin printed circuit board. The board is attached to a high insertion, 88-pin receptacle connector. The package has a polarized key to prevent improper installation, including insertion into other types of IC card sockets. The MT12D88C140 operates reliably up to 55°C.

MEMORY TRUTH TABLE

FUNCTION		RAS	CAS	WE	OE	ADDRESSES tR	ADDRESSES tC	DATA IN/OUT DQ0-DQ39
Standby		H	H→X	X	X	X	X	High-Z
READ		L	L	H	L (NC)	ROW	COL	Data Out
EARLY-WRITE		L	L	L	X	ROW	COL	Data In
READ-WRITE		L	L	H→L	L→H	ROW	COL	Data Out
FAST-PAGE-MODE	1st Cycle	L	H→L	H	L (NC)	ROW	COL	Data Out
READ	2nd Cycle	L	H→L	H	L (NC)	n/a	COL	Data Out
FAST-PAGE-MODE	1st Cycle	L	H→L	L	X	ROW	COL	Data In
EARLY-WRITE	2nd Cycle	L	H→L	L	X	n/a	COL	Data In
FAST-PAGE-MODE	1st Cycle	L	H→L	H→L	L→H	ROW	COL	Data In
READ-WRITE	2nd Cycle	L	H→L	H→L	L→H	n/a	COL	Data In
RAS-ONLY REFRESH		L	X	X	X	ROW	n/a	High-Z
HIDDEN	READ	L→H→L	L	H	L (NC)	ROW	COL	Data Out
REFRESH	WRITE	L→H→L	L	L	X	ROW	COL	Data In
CAS-BEFORE-RAS REFRESH		H→L	L	H	X	X	X	High-Z
BATTERY BACKUP REFRESH		H→L	L	H	X	X	X	High-Z

PRESENCE DETECT TRUTH TABLE

CHARACTERISTICS						PRESENT DETECT PIN (PDx)							
Card Density	DRAM Organizations	Card Address	RAS Address	CAS Address	Page Depth	1	2	3	4	5	6	7	8
0MB	No card installed	X	X	X	X	NC	NC	NC	NC	NC	X	X	X
1MB	256K x 1, 4, 16, 18	18	9	9	512	Vss	Vss	Vss	Vss	NC	X	X	X
2MB	256K x 1, 4, 16, 18	18	9	9	512	Vss	Vss	Vss	Vss	Vss	X	X	X
2MB	512K x 8, 9	19	10	9	512	NC	Vss	Vss	Vss	NC	X	X	X
4MB	512K x 8, 9	19	10	9	512	NC	Vss	Vss	Vss	Vss	X	X	X
• 4MB	1 Meg x 1, 4, 16, 18	20	10	10	1,024	Vss	NC	Vss	Vss	NC	X	X	X
8MB	1 Meg x 1, 4, 16, 18	20	10	10	1,024	Vss	NC	Vss	Vss	Vss	X	X	X
8MB	2 Meg x 8, 9	21	11	10	1,024	NC	NC	Vss	Vss	NC	X	X	X
16MB	2 Meg x 8, 9	21	11	10	1,024	NC	NC	Vss	Vss	Vss	X	X	X
16MB	4 Meg x 1, 4, 16, 18	22	12	11	1,024	Vss	Vss	NC	Vss	NC	X	X	X
32MB	4 Meg x 1, 4, 16, 18	22	12	11	1,024	Vss	Vss	NC	Vss	Vss	X	X	X
Access Timing		100ns				X	X	X	X	X	Vss	Vss	X
		80ns				X	X	X	X	X	NC	Vss	X
		70ns				X	X	X	X	X	Vss	NC	X
		60ns				X	X	X	X	X	NC	NC	X
		50ns				X	X	X	X	X	Vss	Vss	X
Refresh Control		Standard				X	X	X	X	X	X	X	NC
		Auto				X	X	X	X	X	X	X	Vss

NOTE: Vss = Ground.

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} ..... -0.5V to +5.25V
Operating Temperature, T_A (Ambient) ..... 0°C to +55°C
Storage Temperature ..... -20°C to +80°C
Power Dissipation 15W
Short Circuit Output Current 50mA
Card Insertions (Connector's Life Cycle) 10,000

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 3, 4, 6, 7) (0°C ≤ T_A ≤ 55°C; V_{CC} = 5V ±5%)

PARAMETER/CONDITION		SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage		V_{CC}	4.75	5.25	V	1
Input High (Logic 1) Voltage, All Inputs		V_{IH}	3.5	V_{CC}+0.5	V	1
Input Low (Logic 0) Voltage, All Inputs		V_{IL}	-0.5	0.8	V	1
INPUT LEAKAGE CURRENT, Any input	Non-buffered	I_{IN}	-12	12	µA	
(0V ≤ V_{IN} ≤ 5.25V; all other pins not under test = 0V)	Buffered	I_{IB}	-2	2	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled; 0V ≤ V_{OUT} ≤ 5.25V)		I_{OZ}	-10	10	µA	
OUTPUT LEVELS Output High Voltage (I_{OUT} = -5mA)		V_{OH}	2.4		V	
Output Low Voltage (I_{OUT} = 4.2mA)		V_{OL}		0.4	V	

		MAX				
PARAMETER/CONDITION	SYMBOL	-6	-7	-8	UNITS	NOTES
STANDBY CURRENT: (TTL) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC1}	24	24	24	mA	
STANDBY CURRENT: (CMOS) ($\overline{RAS}$ = $\overline{CAS}$ = Other Inputs = V_{CC} -0.2V)	I_{CC2}	2.4	2.4	2.4	mA	
OPERATING CURRENT: Random READ/WRITE Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC (MIN))	I_{CC3}	1.26	1.14	1.02	A	3, 4, 30
OPERATING CURRENT: FAST PAGE MODE Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: ^tPC = ^tPC (MIN))	I_{CC4}	900	780	660	mA	3, 4, 30
REFRESH CURRENT: $\overline{RAS}$-ONLY Average power supply current ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}: ^tRC = ^tRC (MIN))	I_{CC5}	1.26	1.14	1.02	A	3, 30
REFRESH CURRENT: $\overline{CAS}$-BEFORE-$\overline{RAS}$ (CBR) Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC (MIN))	I_{CC6}	1.26	1.14	1.02	A	3, 5, 30
REFRESH CURRENT: BATTERY BACKUP (BBU) Average power supply current during BBU: $\overline{CAS}$ = 0.2V or CBR cycling; $\overline{RAS}$ = ^tRAS (MIN) up to 300ns; ^tRC = 125µs; $\overline{WE}$, A0-A9 and DQ = Vcc -0.2V or 0.2V (DQ may be left open)	I_{CC7}	3.6	3.6	3.6	mA	3, 5

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: $\overline{CAS0}$, $\overline{CAS1}$, $\overline{CAS2}$, $\overline{CAS3}$, A0-A9, $\overline{OE}$	C_{I1}		9	pF	2
Input Capacitance: $\overline{WE}$	C_{I2}		13	pF	2
Input Capacitance: $\overline{RAS0}$, $\overline{RAS2}$	C_{I3}		50	pF	2
Input/Output Capacitance: DQ	C_{IO}		12	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C ≤ T_A ≤ 55°C; V_{CC} = 5V ±5%)

AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	^tRC	110		130		150		ns	23
FAST-PAGE-MODE READ or WRITE cycle time	^tPC	40		40		45		ns	23
Access time from $\overline{RAS}$	^tRAC		60		70		80	ns	14, 23
Access time from $\overline{CAS}$	^tCAC		25		30		30	ns	15, 26
Access time from column address	^tAA		40		45		50	ns	26
Access time from $\overline{CAS}$ precharge	^tCPA		50		50		55	ns	26
$\overline{RAS}$ pulse width	^tRAS	60	100,000	70	100,000	80	100,000	ns	23
$\overline{RAS}$ pulse width (FAST PAGE MODE)	^tRASP	60	100,000	70	100,000	80	100,000	ns	23
$\overline{RAS}$ hold time	^tRSH	25		30		30		ns	26
$\overline{RAS}$ precharge time	^tRP	45		50		60		ns	23
$\overline{CAS}$ pulse width	^tCAS	15	100,000	20	100,000	20	100,000	ns	23
$\overline{CAS}$ hold time	^tCSH	55		65		75		ns	25
$\overline{CAS}$ precharge time	^tCPN	10		10		10		ns	16, 23
$\overline{CAS}$ precharge time (FAST PAGE MODE)	^tCP	10		10		10		ns	23
$\overline{RAS}$ to $\overline{CAS}$ delay time	^tRCD	10	35	15	40	15	50	ns	17, 28
$\overline{CAS}$ to $\overline{RAS}$ precharge time	^tCRP	15		15		15		ns	26
Row address setup time	^tASR	10		10		10		ns	26
Row address hold time	^tRAH	5		5		5		ns	25
$\overline{RAS}$ to column address delay time	^tRAD	10	20	10	25	10	30	ns	18, 28
Column address setup time	^tASC	5		5		5		ns	24
Column address hold time	^tCAH	15		20		20		ns	24
Column address hold time (referenced to $\overline{RAS}$)	^tAR	45		50		55		ns	25
Column address to $\overline{RAS}$ lead time	^tRAL	40		45		50		ns	26
Read command setup time	^tRCS	5		5		5		ns	25
Read command hold time (referenced to $\overline{CAS}$)	^tRCH	5		5		5		ns	19, 24
Read command hold time (referenced to $\overline{RAS}$)	^tRRH	-5		-5		-5		ns	19, 25
$\overline{CAS}$ to output in Low-Z	^tCLZ	5		5		5		ns	24
Output buffer turn-off delay	^tOFF	5	30	5	30	5	30	ns	20, 29, 35
$\overline{WE}$ command setup time	^tWCS	5		5		5		ns	24

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C ≤ T_A ≤ 55°C; Vcc = 5V ±5%)

AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Write command hold time	^tWCH	15		20		20		ns	24
Write command hold time (referenced to $\overline{RAS}$)	^tWCR	40		50		55		ns	25
Write command pulse width	^tWP	10		15		15		ns	23
Write command to $\overline{RAS}$ lead time	^tRWL	25		30		30		ns	26
Write command to $\overline{CAS}$ lead time	^tCWL	20		25		25		ns	24
Data-in setup time	^tDS	5		5		5		ns	24, 32
Data-in hold time	^tDH	5		10		10		ns	25, 32
Data-in hold time (referenced to $\overline{RAS}$)	^tDHR	45		55		60		ns	23
Transition time (rise or fall)	^tT	2	15	2	15	2	15	ns	9, 10, 23
Refresh period (1,024 cycles)	^tREF		128		128		128	ms	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	^tRPC	10		10		10		ns	26
$\overline{CAS}$ setup time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tCSR	20		20		20		ns	5, 26
$\overline{CAS}$ hold time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tCHR	10		10		10		ns	5, 25
$\overline{WE}$ hold time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tWRH	5		5		5		ns	22, 25
$\overline{WE}$ setup time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tWRP	20		20		20		ns	22, 26
$\overline{WE}$ hold time (WCBR test cycle)	^tWTH	5		5		5		ns	22, 25
$\overline{WE}$ setup time	^tWTS	20		20		20		ns	22, 26
READ-WRITE cycle time	^tRWC	165		185		205		ns	
FAST-PAGE-MODE READ-WRITE cycle time	^tPRWC	90		95		100		ns	23
$\overline{RAS}$ to $\overline{WE}$ delay time	^tRWD	80		90		100		ns	31, 27
Column Address to $\overline{WE}$ delay time	^tAWD	65		70		75		ns	31, 24
$\overline{CAS}$ to $\overline{WE}$ delay time	^tCWD	50		65		55		ns	31, 24
Output buffer turn-off delay	^tOE		25		30		30	ns	20, 33, 26
Output disable	^tOD		25		30		30	ns	35, 26
$\overline{OE}$ hold time from $\overline{WE}$ during READ-MODIFY-WRITE cycle	^tOEH	5		10		10		ns	34, 27
$\overline{OE}$ hold time from $\overline{RAS}$ during HIDDEN REFRESH cycle	^tORD	10		10		10		ns	21, 26

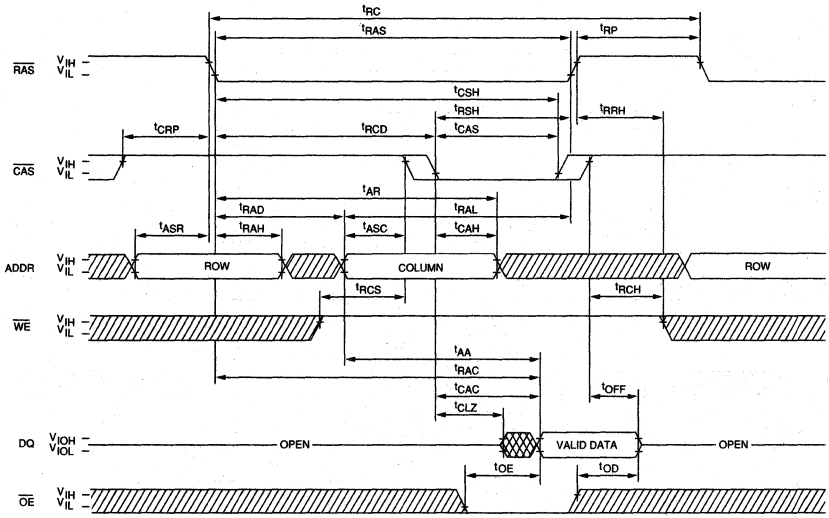
NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. V_{CC} = 5V ±10%, f = 1 MHz.
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is assured.
7. An initial pause of 100µs is required after power-up followed by eight $\overline{RAS}$ refresh cycles ($\overline{RAS}$-ONLY or CBR with $\overline{WE}$ HIGH) before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-up should be repeated any time the ^{t}REF refresh requirement is exceeded.
8. AC characteristics assume ^{t}T = 5ns.
9. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS}$ = V_{IH}, data output is High-Z.
12. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to 2 TTL gates and 100pF.
14. Assumes that $^{t}RCD < {}^{t}RCD$ (MAX). If ^{t}RCD is greater than the maximum recommended value shown in this table, ^{t}RAC will increase by the amount that ^{t}RCD exceeds the value shown.
15. Assumes that $^{t}RCD \geq {}^{t}RCD$ (MAX).
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer, $\overline{CAS}$ must be pulsed HIGH for ^{t}CPN.
17. Operation within the ^{t}RCD (MAX) limit ensures that ^{t}RAC (MAX) can be met. ^{t}RCD (MAX) is specified as a reference point only; if ^{t}RCD is greater than the specified ^{t}RCD (MAX) limit, then access time is controlled exclusively by ^{t}CAC.
18. Operation within the ^{t}RAD (MAX) limit ensures that ^{t}RCD (MAX) can be met. ^{t}RAD (MAX) is specified as a reference point only; if ^{t}RAD is greater than the specified ^{t}RAD (MAX) limit, then access time is controlled exclusively by ^{t}AA.
19. Either ^{t}RCH or ^{t}RRH must be satisfied for a READ cycle.
20. ^{t}OFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
21. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW.
22. ^{t}WTS and ^{t}WTH are setup and hold specifications for the $\overline{WE}$ pin being held LOW to enable the JEDEC test mode (with CBR timing constraints). These two parameters are the inverse of ^{t}WRP and ^{t}WRH in the CBR refresh cycle.
23. Timing between the DRAMs and the DRAM card did not change with the addition of the line drivers.
24. A +5ns timing skew from the DRAM to the DRAM card resulted from the addition of line drivers.
25. A -5ns timing skew from the DRAM to the DRAM card resulted from the addition of line drivers.
26. A +10ns timing skew from the DRAM to the DRAM card resulted from the addition of line drivers.
27. A -10ns timing skew from the DRAM to the DRAM card resulted from the addition of line drivers.
28. A -5ns (MIN) and a -10ns (MAX) timing skew from the DRAM to the DRAM card resulted from the addition of line drivers.
29. A +5ns (MIN) and a +10ns (MAX) timing skew from the DRAM to the DRAM card resulted from the addition of line drivers.
30. The maximum current ratings are based with the memory operating or being refreshed in the x32/36/40 mode. The stated maximums may be reduced by one half when used in the x16/18/20 mode.
31. ^{t}WCS, ^{t}RWD, ^{t}AWD and ^{t}CWD are restrictive operating parameters in late WRITE, and READ-MODIFY-WRITE cycles only. If $^{t}WCS \geq {}^{t}WCS$ (MIN), the cycle is an EARLY-WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If $^{t}RWD \geq {}^{t}RWD$ (MIN), $^{t}AWD \geq {}^{t}AWD$ (MIN) and $^{t}CWD \geq {}^{t}CWD$ (MIN), the cycle is a READ-MODIFY-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of data out is indeterminate. $\overline{OE}$ held HIGH and $\overline{WE}$ taken LOW after $\overline{CAS}$ goes LOW results in a LATE-WRITE ($\overline{OE}$ controlled) cycle.

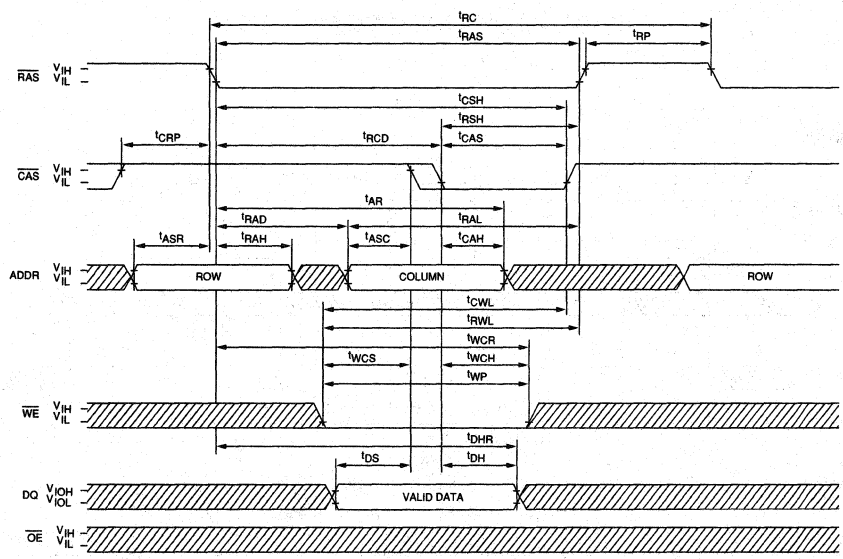
NOTES (continued)

32. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY-WRITE cycles and $\overline{WE}$ leading edge in LATE-WRITE or READ-MODIFY-WRITE cycles.
33. If $\overline{OE}$ is tied permanently LOW, LATE-WRITE or READ-MODIFY-WRITE operations are not possible.
34. LATE-WRITE and READ-MODIFY-WRITE cycles must have both ^{t}OD and ^{t}OEH met ($\overline{OE}$ HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. The DQs will provide the previously read data if $\overline{CAS}$ remains LOW and $\overline{OE}$ is taken back LOW after ^{t}OEH is met. If $\overline{CAS}$ goes HIGH prior to $\overline{OE}$ going back LOW, the DQs will remain open.
35. The DQs open during READ cycles once ^{t}OD or ^{t}OFF occur. If $\overline{CAS}$ goes HIGH first, $\overline{OE}$ becomes a "don't care." If $\overline{OE}$ goes HIGH and $\overline{CAS}$ stays LOW, $\overline{OE}$ is not a "don't care;" and the DQs will provide the previously read data if $\overline{OE}$ is taken back LOW (while $\overline{CAS}$ remains LOW).

READ CYCLE

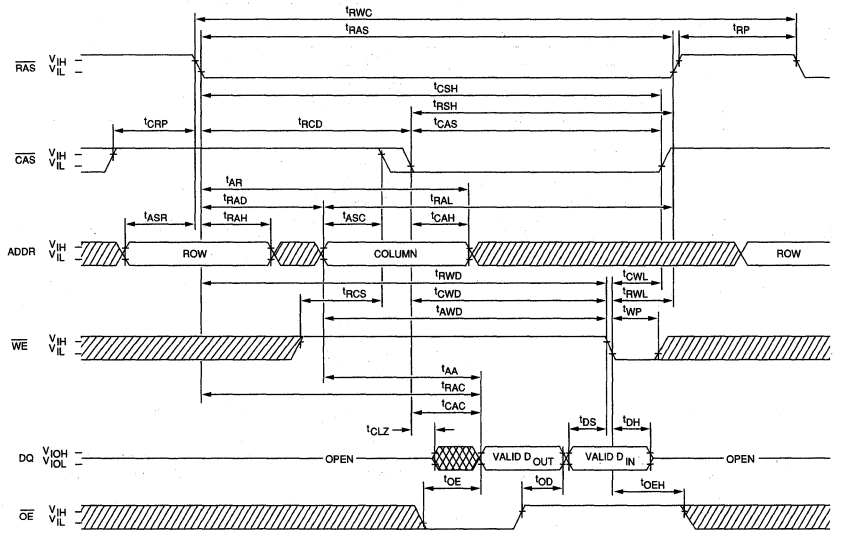


EARLY-WRITE CYCLE

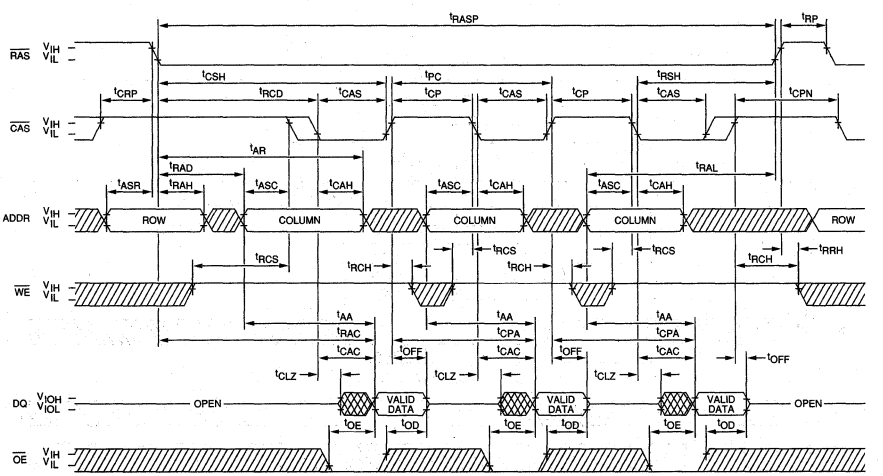


NEW ■ IC DRAM CARD

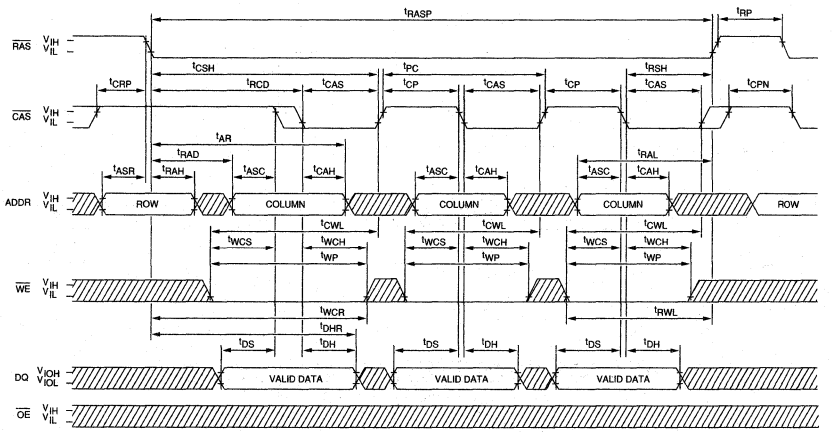
READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)



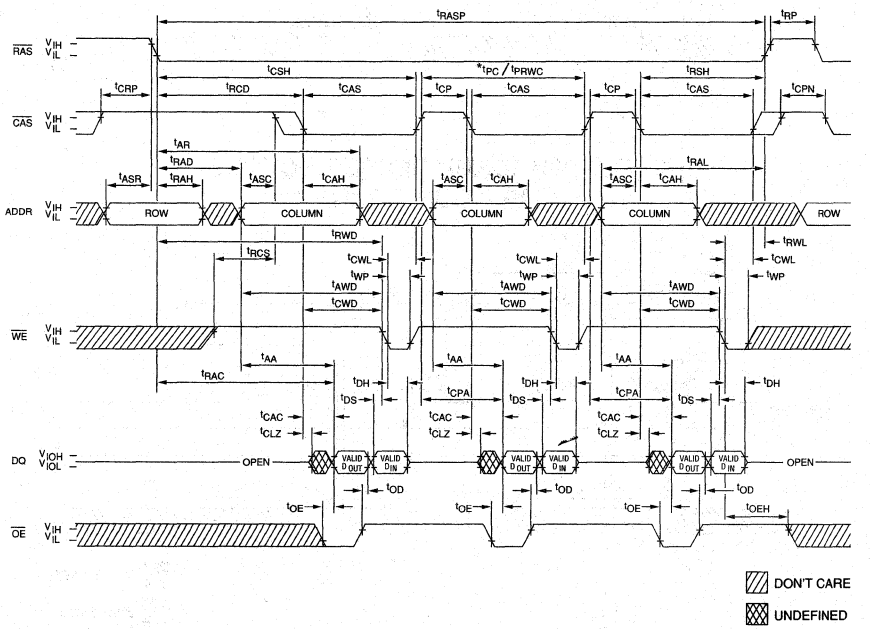
FAST-PAGE-MODE READ CYCLE



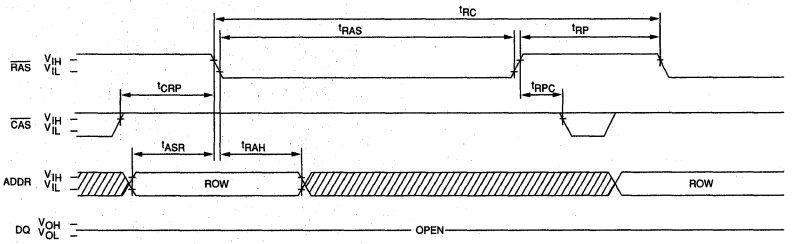
FAST-PAGE-MODE EARLY-WRITE CYCLE



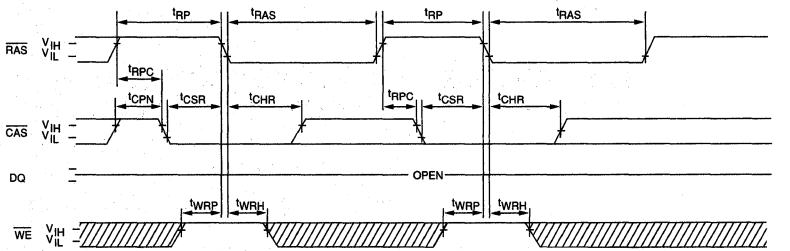
FAST-PAGE-MODE READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)



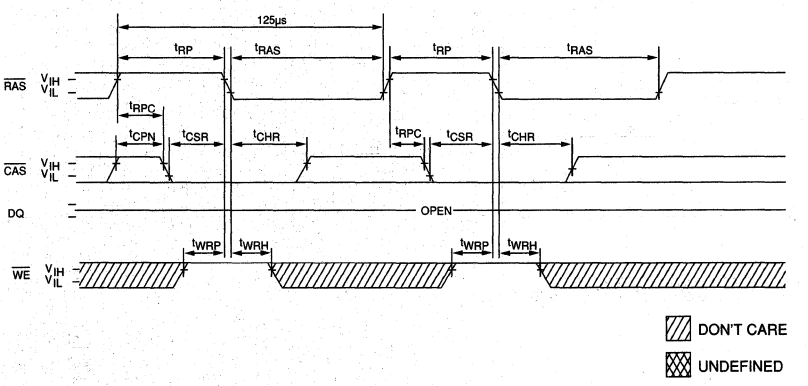
RAS-ONLY REFRESH CYCLE
(ADDR = A0-A9; WE = DON'T CARE)



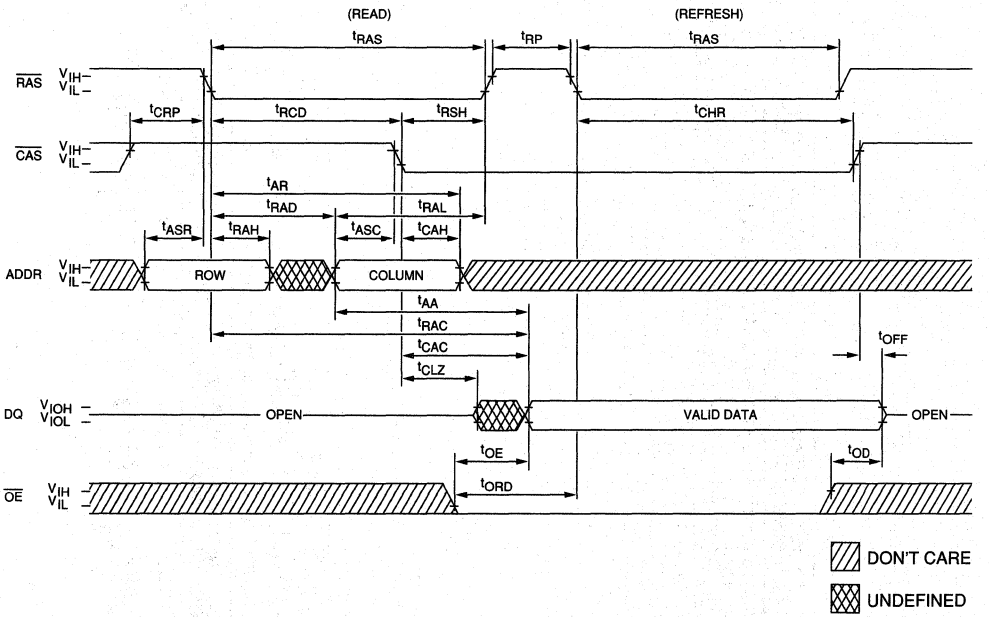
CAS-BEFORE-RAS REFRESH CYCLE
(A0-A9 = DON'T CARE)



BATTERY BACKUP REFRESH CYCLE
(A0-A9 = DON'T CARE)

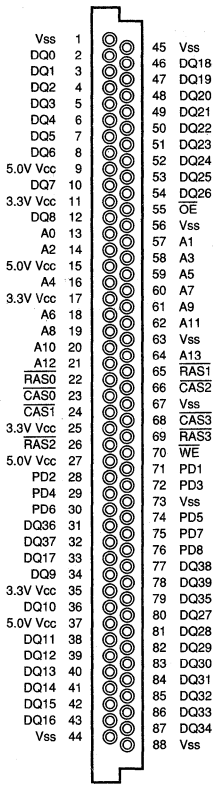


HIDDEN REFRESH CYCLE [21]
($\overline{WE}$ = HIGH)



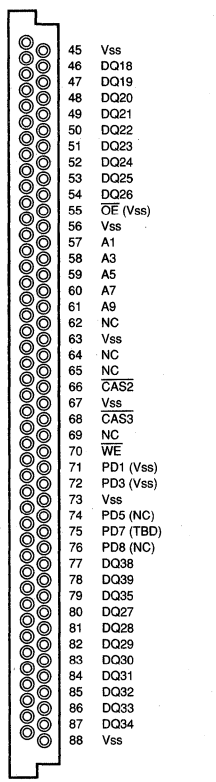
NEW ■ IC DRAM CARD

RESERVED JEDEC, JEIDA and PCMCIA 88-PIN ASSIGNMENT
(All Possible Combinations)



Vss	1	45	Vss
DQ0	2	46	DQ18
DQ1	3	47	DQ19
DQ2	4	48	DQ20
DQ3	5	49	DQ21
DQ4	6	50	DQ22
DQ5	7	51	DQ23
DQ6	8	52	DQ24
5.0V Vcc	9	53	DQ25
DQ7	10	54	DQ26
3.3V Vcc	11	55	$\overline{OE}$
DQ8	12	56	Vss
A0	13	57	A1
A2	14	58	A3
5.0V Vcc	15	59	A5
A4	16	60	A7
3.3V Vcc	17	61	A9
A6	18	62	A11
A8	19	63	Vss
A10	20	64	A13
A12	21	65	$\overline{RAS1}$
$\overline{RAS0}$	22	66	$\overline{CAS2}$
$\overline{CAS0}$	23	67	Vss
$\overline{CAS1}$	24	68	$\overline{CAS3}$
3.3V Vcc	25	69	$\overline{RAS3}$
$\overline{RAS2}$	26	70	$\overline{WE}$
5.0V Vcc	27	71	PD1
PD2	28	72	PD3
PD4	29	73	Vss
PD6	30	74	PD5
DQ36	31	75	PD7
DQ37	32	76	PD8
DQ17	33	77	DQ38
DQ9	34	78	DQ39
3.3V Vcc	35	79	DQ35
DQ10	36	80	DQ27
5.0V Vcc	37	81	DQ28
DQ11	38	82	DQ29
DQ12	39	83	DQ30
DQ13	40	84	DQ31
DQ14	41	85	DQ32
DQ15	42	86	DQ33
DQ16	43	87	DQ34
Vss	44	88	Vss

MT12D88C140 PIN ASSIGNMENT
(JEDEC Standard)



Vss	1	45	Vss
DQ0	2	46	DQ18
DQ1	3	47	DQ19
DQ2	4	48	DQ20
DQ3	5	49	DQ21
DQ4	6	50	DQ22
DQ5	7	51	DQ23
DQ6	8	52	DQ24
Vcc	9	53	DQ25
DQ7	10	54	DQ26
NC	11	55	$\overline{OE}$ (Vss)
DQ8	12	56	Vss
A0	13	57	A1
A2	14	58	A3
Vcc	15	59	A5
A4	16	60	A7
NC	17	61	A9
A6	18	62	NC
A8	19	63	Vss
NC	20	64	NC
NC	21	65	NC
$\overline{RAS0}$	22	66	$\overline{CAS2}$
$\overline{CAS0}$	23	67	Vss
$\overline{CAS1}$	24	68	$\overline{CAS3}$
NC	25	69	NC
$\overline{RAS2}$	26	70	$\overline{WE}$
Vcc	27	71	PD1 (Vss)
PD2 (NC)	28	72	PD3 (Vss)
PD4 (Vss)	29	73	Vss
PD6 (TBD)	30	74	PD5 (NC)
DQ36	31	75	PD7 (TBD)
DQ37	32	76	PD8 (NC)
DQ17	33	77	DQ38
DQ9	34	78	DQ39
NC	35	79	DQ35
DQ10	36	80	DQ27
Vcc	37	81	DQ28
DQ11	38	82	DQ29
DQ12	39	83	DQ30
DQ13	40	84	DQ31
DQ14	41	85	DQ32
DQ15	42	86	DQ33
DQ16	43	87	DQ34
Vss	44	88	Vss

IC DRAM CARD

8 MEGABYTES

2 MEG x 40, 4 MEG x 20

NEW IC DRAM CARD

FEATURES

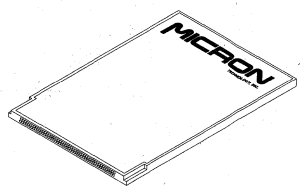
- JEIDA, JEDEC and PCMCIA standard 88-pin IC DRAM card
- Polarized receptacle connector
- Industry standard DRAM functions and timing
- High-performance, CMOS silicon-gate process
- All outputs are fully TTL compatible
- All inputs buffered except $\overline{RAS}$ inputs
- Multiple $\overline{RAS}$ inputs for x16/18/20 or x32/36/40 selectability
- Refresh modes: $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$ (CBR), HIDDEN and BATTERY BACKUP (BBU)
- FAST PAGE MODE access cycle
- Single +5V ±5% power supply
- Low power; 24mW standby, 3.3W active (typical)
- Extended refresh standard: 1,024 cycles every 128ms

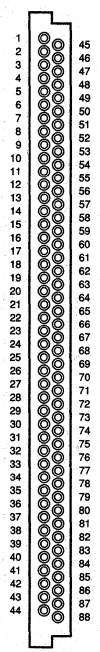
OPTIONS / MARKING

- Timing

60ns access	-6
70ns access	-7
80ns access	-8

PIN ASSIGNMENT (End View)
88-Pin Card (U-1)





PIN #	SYMBOL	PIN #	SYMBOL	PIN #	SYMBOL
1	Vss	31	DQ36	61	A9
2	DQ0	32	DQ37	62	NC
3	DQ1	33	DQ17	63	Vss
4	DQ2	34	DQ9	64	NC
5	DQ3	35	NC	65	$\overline{RAS1}$
6	DQ4	36	DQ10	66	$\overline{CAS2}$
7	DQ5	37	Vcc	67	Vss
8	DQ6	38	DQ11	68	$\overline{CAS3}$
9	Vcc	39	DQ12	69	$\overline{RAS3}$
10	DQ7	40	DQ13	70	$\overline{WE}$
11	NC	41	DQ14	71	PD1 (Vss)
12	DQ8	42	DQ15	72	PD3 (Vss)
13	A0	43	DQ16	73	Vss
14	A2	44	Vss	74	PD5 (Vss)
15	Vcc	45	Vss	75	PD7 (TBD)
16	A4	46	DQ18	76	PD8 (NC)
17	NC	47	DQ19	77	DQ38
18	A6	48	DQ20	78	DQ39
19	A8	49	DQ21	79	DQ35
20	NC	50	DQ22	80	DQ27
21	NC	51	DQ23	81	DQ28
22	$\overline{RAS0}$	52	DQ24	82	DQ29
23	$\overline{CAS0}$	53	DQ25	83	DQ30
24	$\overline{CAS1}$	54	DQ26	84	DQ31
25	NC	55	$\overline{OE}$ (Vss)	85	DQ32
26	$\overline{RAS2}$	56	Vss	86	DQ33
27	Vcc	57	A1	87	DQ34
28	PD2 (NC)	58	A3	88	Vss
29	PD4 (Vss)	59	A5		
30	PD6 (TBD)	60	A7		

GENERAL DESCRIPTION

The MT24D88C240 is an 8 megabyte, IC DRAM card organized primarily as a 2 Meg x 40 bit memory array for EDC applications. It may be used as a x32 or x36 bit memory array (the unused DQs should be tied to Vss or Vcc through current limiting resistors). It may also be configured as a 4 Meg x 20 bit memory array, provided the corresponding DQs on the host system are made common and memory bank control procedures are implemented. Separate $\overline{CAS}$ inputs allow byte accesses.

All inputs to the DRAMs are buffered, with the exception of $\overline{RAS}$. The line drivers used for buffers reduce reflections on the card and ensure compatibility in a wide range of systems. At the same time, the line drivers add delays to the buffered input timings when compared to standard DRAMs.

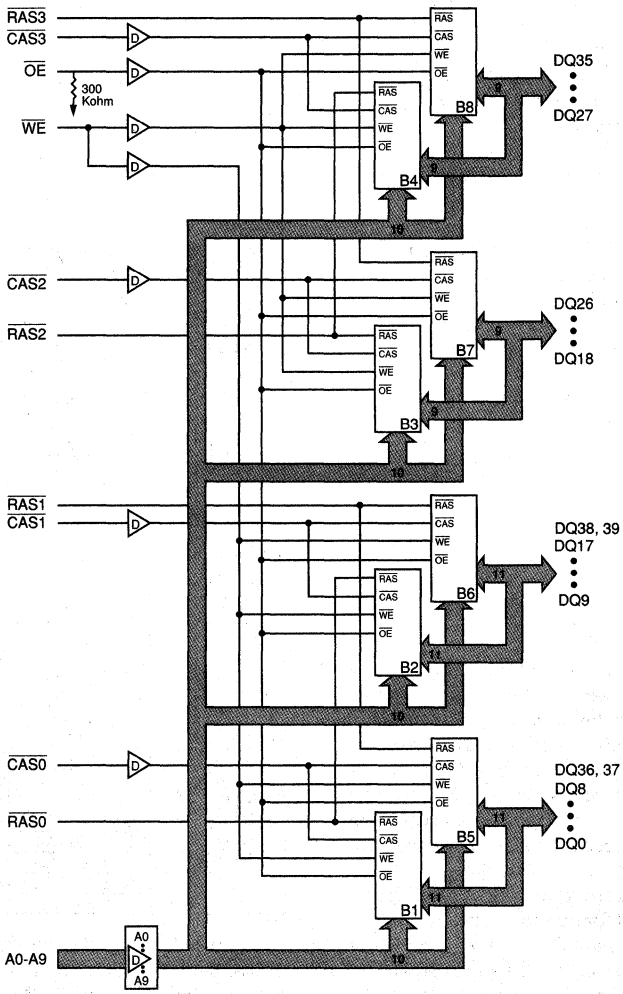
The MT24D88C240 is designed for low power operation using 1 Meg x 4 low power, extended refresh DRAMs. These devices support BATTERY BACKUP (BBU) cycle refresh; a very low current, data retention mode. Standard component DRAM refresh modes are supported as well.

Multiple $\overline{RAS}$ inputs conserve power by allowing individual bank selection. In the x32/36/40 organization, the memory array may be divided into two banks, each with four separate bytes (x32/36 only). In the x16/18/20 organization, up to four banks, each with two separate bytes, may be independently selected. One bank is activated by each $\overline{RAS}$ selection; the others not selected remain in standby mode, drawing minimum power.

Eight presence detect pins may be read by the host to identify the MT24D88C240 organization, number of banks, access time and refresh mode. These extensive presence detect functions allow systems to utilize the advanced power saving features.

The MT24D88C240 is built with a plastic frame covered by stainless steel panels. This package, containing an 88-pin receptacle connector, is keyed to prevent improper installation or insertion into other types of IC card sockets.

FUNCTIONAL BLOCK DIAGRAM



NOTE: 1. D = 74AC11244 line drivers.
2. B1, B2, B5 and B6 = 1 Meg x 8 memory blocks; B3, B4, B7 and B8 = 1 Meg x 9 memory blocks.
3. $\overline{OE}$ is internally connected to ground via a 300 Kohm resistor and is also buffered to the DRAMs.

PIN DESCRIPTIONS

PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
22, 26, 65, 69	$\overline{RAS}$0-3	Input	Row Address Strobe: $\overline{RAS}$ is used to clock-in the 10 row-address bits. Four $\overline{RAS}$ inputs allow for two x32/36/40 banks or four x16/18/20 banks.
23, 24, 66, 68	$\overline{CAS}$0-3	Input	Column Address Strobe: $\overline{CAS}$ is used to clock-in the 10 column-address bits, enable the DRAM output buffers, and strobe the data inputs on WRITE cycles. Four $\overline{CAS}$ inputs allow byte access control for any memory bank configuration (not in x40 mode).
70	$\overline{WE}$	Input	Write Enable: $\overline{WE}$ is the READ/WRITE control for the DQ pins. If $\overline{WE}$ is LOW prior to $\overline{CAS}$ going LOW, the access is an EARLY-WRITE cycle. If $\overline{WE}$ is HIGH while $\overline{CAS}$ is LOW, the access is a READ cycle, provided $\overline{OE}$ is also LOW. If WE goes LOW after $\overline{CAS}$ goes LOW, then the cycle is a LATE-WRITE cycle. A LATE-WRITE cycle is generally used in conjunction with a READ cycle to form a READ-MODIFY-WRITE cycle.
55	$\overline{OE}$	Input	Output Enable: $\overline{OE}$ is the input/output control for the DQ pins. $\overline{OE}$ is connected to ground through a 300 Kohm resistor and is intended to be LOW, allowing for EARLY-WRITE cycles only. This signal may be driven, allowing for LATE-WRITE cycles.
13, 57, 14, 58, 16, 59 18, 60, 19, 61	A0-A9	Input	Address Inputs: These inputs are multiplexed and clocked by $\overline{RAS}$ and $\overline{CAS}$.
2-8, 10, 12, 34, 36 38-43, 33, 46-54, 80-87 79, 31, 32, 77, 78	DQ0-DQ39	Input/ Output	Data I/O: For WRITE cycles, DQ0-DQ39 act as inputs to the addressed DRAM location. BYTE WRITEs may be performed by using the corresponding $\overline{CAS}$ select (x32/36 mode only). For READ access cycles, DQ0-DQ39 act as outputs for the addressed DRAM location.
71, 28, 72, 29 74, 30, 75, 76	PD1-PD8	-	Presence Detect: These pins are read by the host system and tell the system the card's personality. They will be either left floating (NC) or they will be grounded (Vss).
11, 17, 20, 21, 25 35, 62, 64	NC	-	No Connect: These pins should be left unconnected (reserved for future use).
9, 15, 27, 37	Vcc	Supply	Power Supply: +5V ± 5%
1, 44, 45, 56 63, 67, 73, 88	Vss	Supply	Ground

FUNCTIONAL DESCRIPTION

The MT24D88C240 is an 8 megabyte memory card structured as a 2 Meg x 32/36/40 bit memory array ($\overline{RAS0}$ = $\overline{RAS2}$, $\overline{RAS1}$ = $\overline{RAS3}$). It also may be configured as a 4 Meg x 16/18/20 bit memory array, provided the corresponding DQs on the host are connected and memory bank control procedures are implemented by interleaving all four $\overline{RAS}$ lines.

Most x32/36/40 bit applications use the same signal to control the $\overline{CAS}$ inputs. $\overline{RAS0}$ and $\overline{RAS1}$ control the lower 16/18 bits, and $\overline{RAS2}$ and $\overline{RAS3}$ control the upper 16/18 bits, to obtain a x32/36/40 memory array. For x16/18 applications, the corresponding DQs and the corresponding $\overline{CAS}$ pins must be connected together (DQ0 to DQ18, DQ1 to DQ19 and so forth, and $\overline{CAS0}$ to $\overline{CAS2}$ and $\overline{CAS1}$ to $\overline{CAS3}$). Each $\overline{RAS}$ is then a bank select for the 4 Meg x 16/18 memory organization.

DRAM OPERATION

DRAM REFRESH

Memory cell data is retained in its correct state by maintaining power and executing any $\overline{RAS}$ cycle [READ, WRITE, $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$ (CBR), HIDDEN or BATTERY BACKUP (BBU) REFRESH] so that all 1,024 combinations of $\overline{RAS}$ addresses (A0-A9) are executed at least every 128ms, regardless of sequence.

The implied method of choice for refreshing the memory card is the BBU cycle. This is a very low current, data retention mode made possible by using the CBR REFRESH cycle over the extended refresh range (I_{CC7}).

The memory card may be used with the other refresh modes common in standard DRAMs. This allows the memory card to be used on existing systems that do not utilize the BBU REFRESH cycle. However, the memory card will draw more current in the STANDBY mode. The CBR REFRESH mode is recommended when not using the BBU mode.

DRAM READ AND WRITE CYCLES

During READ or WRITE cycles, each bit is uniquely addressed through the 20 address bits, which are entered 10 bits (A0-A9) at a time. $\overline{RAS}$ is used to latch the first 10 bits and $\overline{CAS}$ the latter 10 bits. READ or WRITE cycles are selected with the $\overline{WE}$ input. A logic HIGH on $\overline{WE}$ dictates READ mode while a logic LOW on $\overline{WE}$ dictates WRITE mode. During a WRITE cycle, data in (D) is latched by the falling edge of $\overline{CAS}$. $\overline{WE}$ must fall prior to $\overline{CAS}$ (EARLY WRITE); if $\overline{WE}$ goes LOW after $\overline{CAS}$, the outputs (Q) will be activated and will drive invalid data to the inputs, unless LATE-WRITE cycle timing specifications are met. The data inputs and data outputs are routed through pins using common I/O, and pin direction is controlled by $\overline{WE}$.

FAST PAGE MODE operation allows faster data operations (READ or WRITE) within a row address (A0-A9) defined page boundary. The FAST PAGE MODE cycle is always initiated with a row address strobed-in by $\overline{RAS}$ followed by a column address strobed-in by $\overline{CAS}$. $\overline{CAS}$ may be toggled-in by holding $\overline{RAS}$ LOW and strobing-in different column addresses, thus executing faster memory cycles. Returning $\overline{RAS}$ HIGH terminates the FAST PAGE MODE operation. Returning $\overline{RAS}$ and $\overline{CAS}$ HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the $\overline{RAS}$ high time.

DRAM TIMING

In accordance with JEDEC standard specifications, all inputs to the IC DRAM card are buffered, with the exception of $\overline{RAS}$ inputs. The line drivers used for buffers reduce reflections on the card and ensure compatibility in a wide range of systems. The implementation of buffers on the card may relieve the need for additional host system lin drivers. Notes 23 though 29 indicate which parameters on the IC DRAM card are affected by the line drivers, and to what magnitude they are affected. The component DRAM timing specifications, rather than those of the IC DRAM card (in systems that use both), may cause timing incompatibilities.

All traces on the IC DRAM card (buffered and non-buffered) are approximately 50 ohms characteristic impedance. Matching impedance on the system board to 50 ohms characteristic impedance on traces to the IC DRAM card will decrease signal noise to the IC DRAM card, enhancing overall system reliability.

PHYSICAL DESIGN

The MT24D88C240 is constructed with a molded plastic frame and covered with stainless steel panels. Inside, 24 thin small-outline package (TSOP) DRAMs are mounted on both sides of an ultrathin printed circuit board. The board is attached to a high insertion, 88-pin receptacle connector. The package has a polarized key to prevent improper installation, including insertion into other types of IC card sockets. The MT24D88C240 operates reliably up to 55°C.

MEMORY TRUTH TABLE

FUNCTION		RAS	CAS	WE	OE	ADDRESSES tR	ADDRESSES tC	DATA IN/OUT DQ0-DQ39
Standby		H	H→X	X	X	X	X	High-Z
READ		L	L	H	L (NC)	ROW	COL	Data Out
EARLY-WRITE		L	L	L	X	ROW	COL	Data In
READ-WRITE		L	L	H→L	L→H	ROW	COL	Data Out
FAST-PAGE-MODE	1st Cycle	L	H→L	H	L (NC)	ROW	COL	Data Out
READ	2nd Cycle	L	H→L	H	L (NC)	n/a	COL	Data Out
FAST-PAGE-MODE	1st Cycle	L	H→L	L	X	ROW	COL	Data In
EARLY-WRITE	2nd Cycle	L	H→L	L	X	n/a	COL	Data In
FAST-PAGE-MODE	1st Cycle	L	H→L	H→L	L→H	ROW	COL	Data In
READ-WRITE	2nd Cycle	L	H→L	H→L	L→H	n/a	COL	Data In
RAS-ONLY REFRESH		H	X	X	X	ROW	n/a	High-Z
HIDDEN	READ	L→H→L	L	H	L (NC)	ROW	COL	Data Out
REFRESH	WRITE	L→H→L	L	L	X	ROW	COL	Data In
CAS-BEFORE-RAS REFRESH		H→L	L	H	H	X	X	High-Z
BATTERY BACKUP REFRESH		H→L	L	H	H	X	X	High-Z

PRESENCE DETECT TRUTH TABLE

CHARACTERISTICS						PRESENT DETECT PIN (PDx)							
Card Density	DRAM Organizations	Card Address	RAS Address	CAS Address	Page Depth	1	2	3	4	5	6	7	8
0MB	No card installed	X	X	X	X	NC	NC	NC	NC	NC	X	X	X
1MB	256K x 1, 4, 16, 18	18	9	9	512	Vss	Vss	Vss	Vss	NC	X	X	X
2MB	256K x 1, 4, 16, 18	18	9	9	512	Vss	Vss	Vss	Vss	Vss	X	X	X
2MB	512K x 8, 9	19	10	9	512	NC	Vss	Vss	Vss	NC	X	X	X
4MB	512K x 8, 9	19	10	9	512	NC	Vss	Vss	Vss	Vss	X	X	X
4MB	1 Meg x 1, 4, 16, 18	20	10	10	1,024	Vss	NC	Vss	Vss	NC	X	X	X
• 8MB	1 Meg x 1, 4, 16, 18	20	10	10	1,024	Vss	NC	Vss	Vss	Vss	X	X	X
8MB	2 Meg x 8, 9	21	11	10	1,024	NC	NC	Vss	Vss	NC	X	X	X
16MB	2 Meg x 8, 9	21	11	10	1,024	NC	NC	Vss	Vss	Vss	X	X	X
16MB	4 Meg x 1, 4, 16, 18	22	12	11	1,024	Vss	Vss	NC	Vss	NC	X	X	X
32MB	4 Meg x 1, 4, 16, 18	22	12	11	1,024	Vss	Vss	NC	Vss	Vss	X	X	X
Access Timing		100ns				X	X	X	X	X	Vss	Vss	X
		80ns				X	X	X	X	X	NC	Vss	X
		70ns				X	X	X	X	X	Vss	NC	X
		60ns				X	X	X	X	X	NC	NC	X
		50ns				X	X	X	X	X	Vss	Vss	X
Refresh Control		Standard				X	X	X	X	X	X	X	NC
		Auto				X	X	X	X	X	X	X	Vss

NOTE: Vss = Ground.

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} ..... -0.5V to +5.25V
Operating Temperature T_A (Ambient) ..... 0°C to 55°C
Storage Temperature ..... -20°C to +80°C
Power Dissipation 15W
Short Circuit Output Current 50mA
Card Insertions (Connector's Life Cycle) 10,000

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 3, 4, 6, 7) (0°C ≤ T_A ≤ 55°C; V_{CC} = 5V ±5%)

PARAMETER/CONDITION		SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage		V_{CC}	4.75	5.25	V	1
Input High (Logic 1) Voltage, All Inputs		V_{IH}	3.5	V_{CC}+0.5	V	1
Input Low (Logic 0) Voltage, All Inputs		V_{IL}	-0.5	0.8	V	1
INPUT LEAKAGE CURRENT, Any input	Non-buffered	I_{IN}	-12	12	µA	
(0V ≤ V_{IN} ≤ 5.25V; all other pins not under test = 0V)	Buffered	I_{IB}	-2	2	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled; 0V ≤ V_{OUT} ≤ 5.25V)		I_{OZ}	-10	10	µA	
OUTPUT LEVELS		V_{OH}	2.4		V	
Output High Voltage (I_{OUT} = -5mA)						
Output Low Voltage (I_{OUT} = 4.2mA)		V_{OL}		0.4	V	

		MAX				
PARAMETER/CONDITION	SYMBOL	-6	-7	-8	UNITS	NOTES
STANDBY CURRENT: (TTL) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC1}	48	48	48	mA	
STANDBY CURRENT: (CMOS) ($\overline{RAS}$ = $\overline{CAS}$ = Other Inputs = V_{CC} -0.2V)	I_{CC2}	4.8	4.8	4.8	mA	
OPERATING CURRENT: Random READ/WRITE Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC (MIN))	I_{CC3}	1.26	1.14	1.02	A	3, 4, 30
OPERATING CURRENT: FAST PAGE MODE Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: ^tPC = ^tPC (MIN))	I_{CC4}	900	780	660	mA	3, 4, 30
REFRESH CURRENT: $\overline{RAS}$-ONLY Average power supply current ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}: ^tRC = ^tRC (MIN))	I_{CC5}	1.26	1.14	1.02	A	3, 30
REFRESH CURRENT: $\overline{CAS}$-BEFORE-$\overline{RAS}$ (CBR) Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC (MIN))	I_{CC6}	1.26	1.14	1.02	A	3, 5, 30
REFRESH CURRENT: BATTERY BACKUP (BBU) Average power supply current during BBU: $\overline{CAS}$ = 0.2V or CBR cycling; $\overline{RAS}$ = ^tRAS (MIN) up to 300ns; ^tRC = 125µs; $\overline{WE}$, A0-A9 and DQ = Vcc -0.2V or 0.2V (DQ may be left open)	I_{CC7}	7.2	7.2	7.2	mA	3, 5

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: $\overline{CAS0}$, $\overline{CAS1}$, $\overline{CAS2}$, $\overline{CAS3}$, A0-A9, $\overline{OE}$	C_{I1}		9	pF	2
Input Capacitance: $\overline{WE}$	C_{I2}		13	pF	2
Input Capacitance: $\overline{RAS0}$, $\overline{RAS1}$, $\overline{RAS2}$, $\overline{RAS3}$	C_{I3}		50	pF	2
Input/Output Capacitance: DQ	C_{IO}		20	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) ($0°C \le T_A \le 55°C$; $V_{CC} = 5V \pm 5\%$)

AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	^tRC	110		130		150		ns	23
FAST-PAGE-MODE READ or WRITE cycle time	^tPC	40		40		45		ns	23
Access time from $\overline{RAS}$	^tRAC		60		70		80	ns	14, 23
Access time from $\overline{CAS}$	^tCAC		25		30		30	ns	15, 26
Access time from column address	^tAA		40		45		50	ns	26
Access time from $\overline{CAS}$ precharge	^tCPA		50		50		55	ns	26
$\overline{RAS}$ pulse width	^tRAS	60	100,000	70	100,000	80	100,000	ns	23
$\overline{RAS}$ pulse width (FAST PAGE MODE)	^tRASP	60	100,000	70	100,000	80	100,000	ns	23
$\overline{RAS}$ hold time	^tRSH	25		30		30		ns	26
$\overline{RAS}$ precharge time	^tRP	45		50		60		ns	23
$\overline{CAS}$ pulse width	^tCAS	15	100,000	20	100,000	20	100,000	ns	23
$\overline{CAS}$ hold time	^tCSH	55		65		75		ns	25
$\overline{CAS}$ precharge time	^tCPN	10		10		10		ns	16, 23
$\overline{CAS}$ precharge time (FAST PAGE MODE)	^tCP	10		10		10		ns	23
$\overline{RAS}$ to $\overline{CAS}$ delay time	^tRCD	10	35	15	40	15	50	ns	17, 28
$\overline{CAS}$ to $\overline{RAS}$ precharge time	^tCRP	15		15		15		ns	26
Row address setup time	^tASR	10		10		10		ns	26
Row address hold time	^tRAH	5		5		5		ns	25
$\overline{RAS}$ to column address delay time	^tRAD	10	20	10	25	10	30	ns	18, 28
Column address setup time	^tASC	5		5		5		ns	24
Column address hold time	^tCAH	15		20		20		ns	24
Column address hold time (referenced to $\overline{RAS}$)	^tAR	45		50		55		ns	25
Column address to $\overline{RAS}$ lead time	^tRAL	40		45		50		ns	26
Read command setup time	^tRCS	5		5		5		ns	25
Read command hold time (referenced to $\overline{CAS}$)	^tRCH	5		5		5		ns	19, 24
Read command hold time (referenced to $\overline{RAS}$)	^tRRH	-5		-5		-5		ns	19, 25
$\overline{CAS}$ to output in Low-Z	^tCLZ	5		5		5		ns	24
Output buffer turn-off delay	^tOFF	5	30	5	30	5	30	ns	20, 29, 35
$\overline{WE}$ command setup time	^tWCS	5		5		5		ns	24

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C ≤ T_A ≤ 55°C; Vcc = 5V ±5%)

AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Write command hold time	^tWCH	15		20		20		ns	24
Write command hold time (referenced to $\overline{RAS}$)	^tWCR	40		50		55		ns	25
Write command pulse width	^tWP	10		15		15		ns	23
Write command to $\overline{RAS}$ lead time	^tRWL	25		30		30		ns	26
Write command to $\overline{CAS}$ lead time	^tCWL	20		25		25		ns	24
Data-in setup time	^tDS	5		5		5		ns	24, 32
Data-in hold time	^tDH	5		10		10		ns	25, 32
Data-in hold time (referenced to $\overline{RAS}$)	^tDHR	45		55		60		ns	23
Transition time (rise or fall)	^tT	2	15	2	15	2	15	ns	9, 10, 23
Refresh period (1,024 cycles)	^tREF		128		128		128	ms	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	^tRPC	10		10		10		ns	26
$\overline{CAS}$ setup time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tCSR	20		20		20		ns	5, 26
$\overline{CAS}$ hold time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tCHR	10		10		10		ns	5, 25
$\overline{WE}$ hold time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tWRH	5		5		5		ns	22, 25
$\overline{WE}$ setup time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tWRP	20		20		20		ns	22, 26
$\overline{WE}$ hold time (WCBR test cycle)	^tWTH	5		5		5		ns	22, 25
$\overline{WE}$ setup time	^tWTS	20		20		20		ns	22, 26
READ-WRITE cycle time	^tRWC	165		185		205		ns	
FAST-PAGE-MODE READ-WRITE cycle time	^tPRWC	90		95		100		ns	23
$\overline{RAS}$ to $\overline{WE}$ delay time	^tRWD	80		90		100		ns	31, 27
Column Address to $\overline{WE}$ delay time	^tAWD	65		70		75		ns	31, 24
$\overline{CAS}$ to $\overline{WE}$ delay time	^tCWD	50		65		55		ns	31, 24
Output buffer turn-off delay	^tOE		25		30		30	ns	20, 33, 26
Output disable	^tOD		25		30		30	ns	35, 26
$\overline{OE}$ hold time from $\overline{WE}$ during READ-MODIFY-WRITE cycle	^tOEH	5		10		10		ns	34, 27
$\overline{OE}$ hold time from $\overline{RAS}$ during HIDDEN REFRESH cycle	^tORD	10		10		10		ns	21, 26

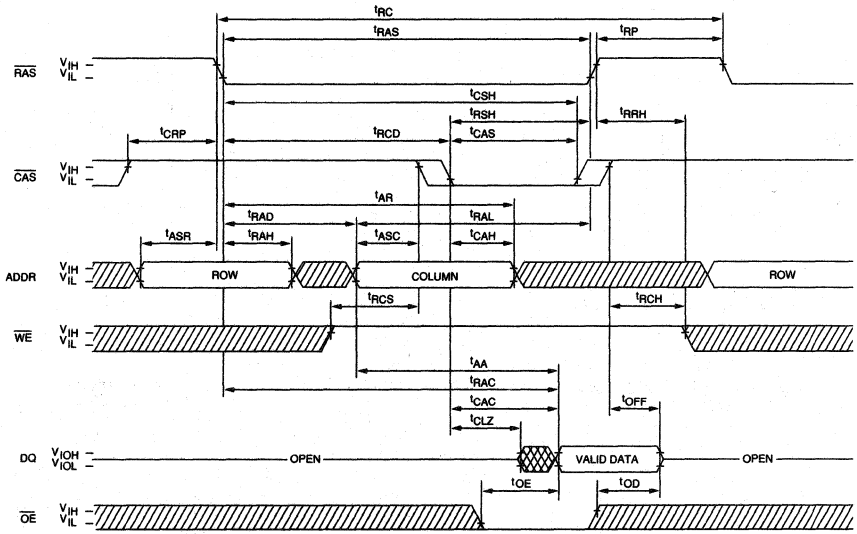
NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. V_{CC} = 5V ±10%, f = 1 MHz.
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is assured.
7. An initial pause of 100µs is required after power-up followed by eight $\overline{RAS}$ refresh cycles ($\overline{RAS}$-ONLY or CBR with $\overline{WE}$ HIGH) before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-up should be repeated any time the ^{t}REF refresh requirement is exceeded.
8. AC characteristics assume ^{t}T = 5ns.
9. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS}$ = V_{IH}, data output is High-Z.
12. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to 2 TTL gates and 100pF.
14. Assumes that $^{t}RCD < {}^{t}RCD$ (MAX). If ^{t}RCD is greater than the maximum recommended value shown in this table, ^{t}RAC will increase by the amount that ^{t}RCD exceeds the value shown.
15. Assumes that $^{t}RCD \geq {}^{t}RCD$ (MAX).
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer, $\overline{CAS}$ must be pulsed HIGH for ^{t}CPN.
17. Operation within the ^{t}RCD (MAX) limit ensures that ^{t}RAC (MAX) can be met. ^{t}RCD (MAX) is specified as a reference point only; if ^{t}RCD is greater than the specified ^{t}RCD (MAX) limit, then access time is controlled exclusively by ^{t}CAC.
18. Operation within the ^{t}RAD (MAX) limit ensures that ^{t}RCD (MAX) can be met. ^{t}RAD (MAX) is specified as a reference point only; if ^{t}RAD is greater than the specified ^{t}RAD (MAX) limit, then access time is controlled exclusively by ^{t}AA.
19. Either ^{t}RCH or ^{t}RRH must be satisfied for a READ cycle.
20. ^{t}OFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
21. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW.
22. ^{t}WTS and ^{t}WTH are setup and hold specifications for the $\overline{WE}$ pin being held LOW to enable the JEDEC test mode (with CBR timing constraints). These two parameters are the inverse of ^{t}WRP and ^{t}WRH in the CBR refresh cycle.
23. Timing between the DRAMs and the DRAM card did not change with the addition of the line drivers.
24. A +5ns timing skew from the DRAM to the DRAM card resulted from the addition of line drivers.
25. A -5ns timing skew from the DRAM to the DRAM card resulted from the addition of line drivers.
26. A +10ns timing skew from the DRAM to the DRAM card resulted from the addition of line drivers.
27. A -10ns timing skew from the DRAM to the DRAM card resulted from the addition of line drivers.
28. A -5ns (MIN) and a -10ns (MAX) timing skew from the DRAM to the DRAM card resulted from the addition of line drivers.
29. A +5ns (MIN) and a +10ns (MAX) timing skew from the DRAM to the DRAM card resulted from the addition of line drivers.
30. The maximum current ratings are based with the memory operating or being refreshed in the x32/36/40 mode. The stated maximums may be reduced by one half when used in the x16/18/20 mode.
31. ^{t}WCS, ^{t}RWD, ^{t}AWD and ^{t}CWD are restrictive operating parameters in late WRITE, and READ-MODIFY-WRITE cycles only. If $^{t}WCS \geq {}^{t}WCS$ (MIN), the cycle is an EARLY-WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If $^{t}RWD \geq {}^{t}RWD$ (MIN), $^{t}AWD \geq {}^{t}AWD$ (MIN) and $^{t}CWD \geq {}^{t}CWD$ (MIN), the cycle is a READ-MODIFY-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of data out is indeterminate. $\overline{OE}$ held HIGH and $\overline{WE}$ taken LOW after $\overline{CAS}$ goes LOW results in a LATE-WRITE ($\overline{OE}$ controlled) cycle.

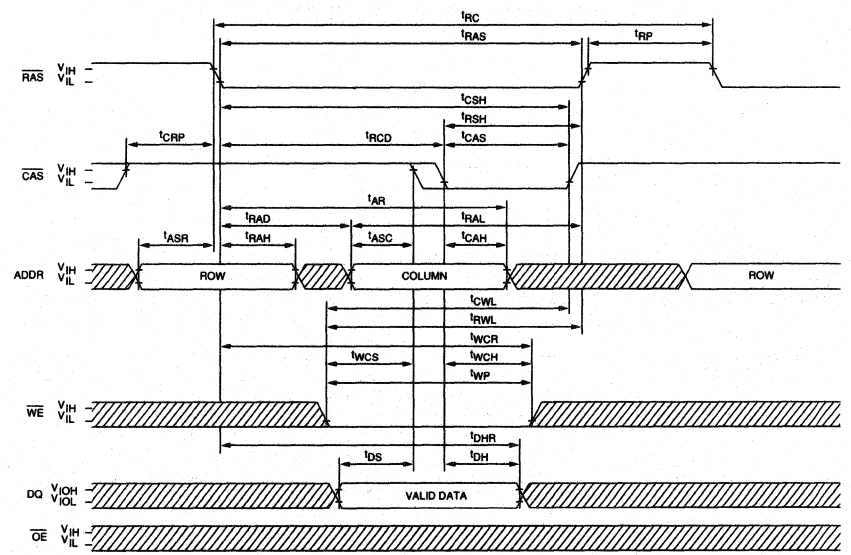
NOTES (continued)

32. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY-WRITE cycles and $\overline{WE}$ leading edge in LATE-WRITE or READ-MODIFY-WRITE cycles.
33. If $\overline{OE}$ is tied permanently LOW, LATE-WRITE or READ-MODIFY-WRITE operations are not possible.
34. LATE-WRITE and READ-MODIFY-WRITE cycles must have both ^{t}OD and ^{t}OEH met ($\overline{OE}$ HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. The DQs will provide the previously read data if $\overline{CAS}$ remains LOW and $\overline{OE}$ is taken back LOW after ^{t}OEH is met. If $\overline{CAS}$ goes HIGH prior to $\overline{OE}$ going back LOW, the DQs will remain open.
35. The DQs open during READ cycles once ^{t}OD or ^{t}OFF occur. If $\overline{CAS}$ goes HIGH first, $\overline{OE}$ becomes a "don't care." If $\overline{OE}$ goes HIGH and $\overline{CAS}$ stays LOW, $\overline{OE}$ is not a "don't care;" and the DQs will provide the previously read data if $\overline{OE}$ is taken back LOW (while $\overline{CAS}$ remains LOW).

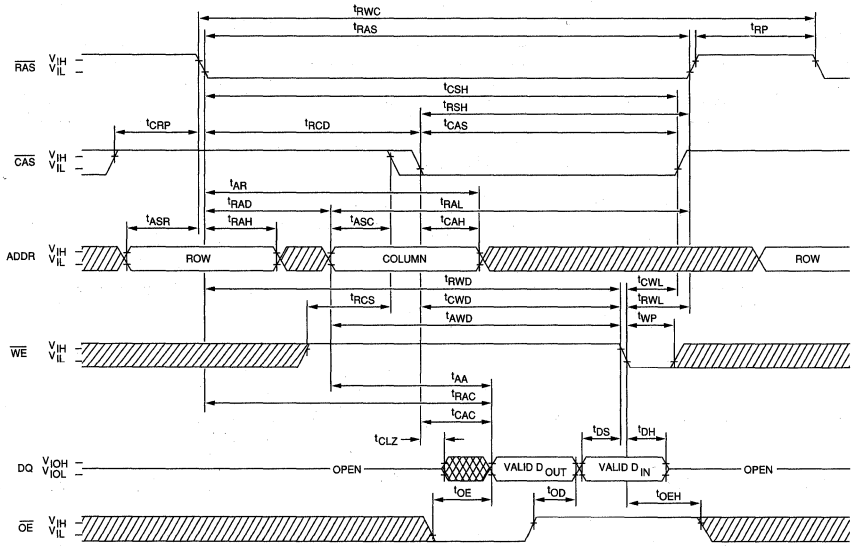
READ CYCLE



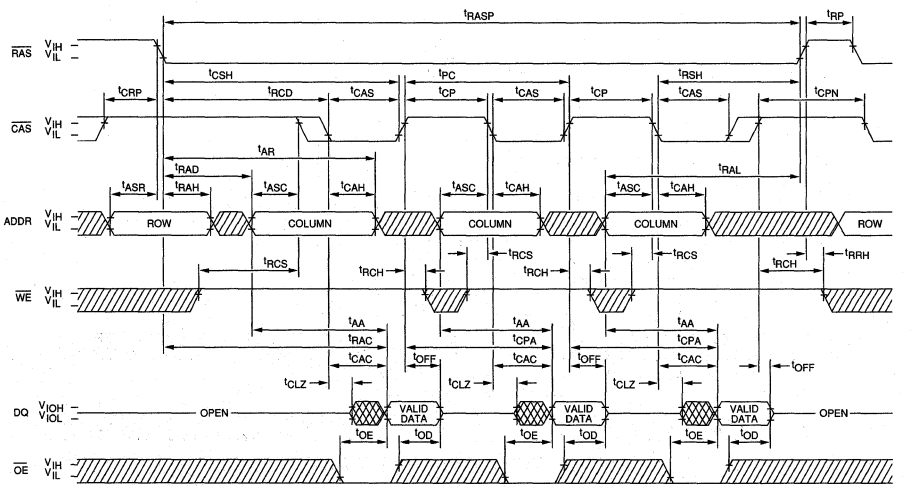
EARLY-WRITE CYCLE



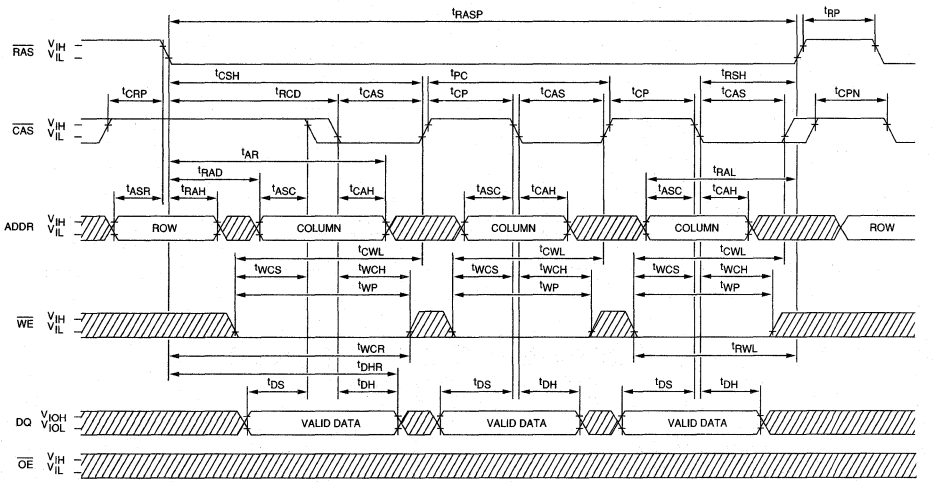
READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)



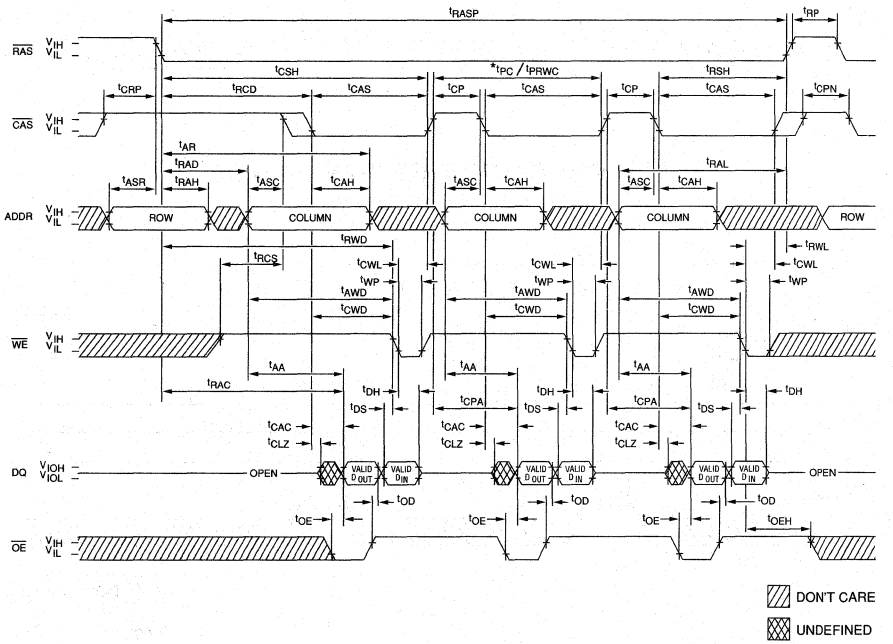
FAST-PAGE-MODE READ CYCLE



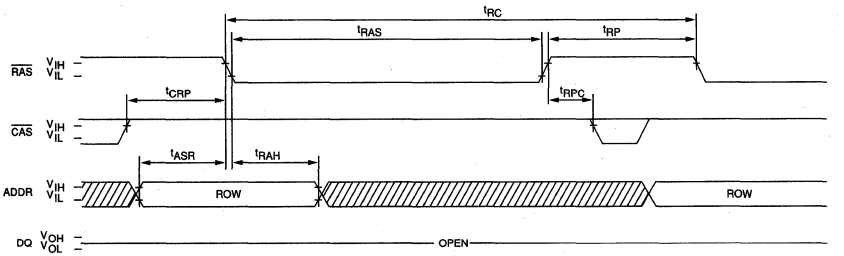
FAST-PAGE-MODE EARLY-WRITE CYCLE



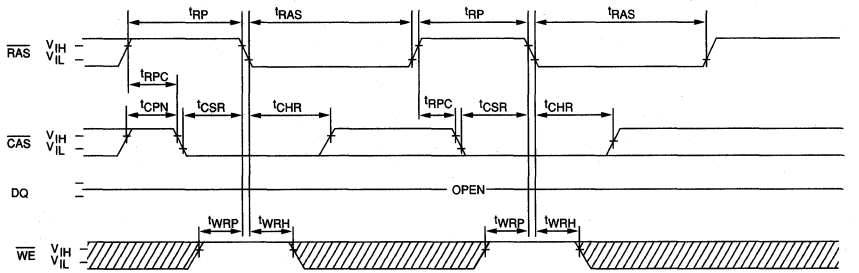
FAST-PAGE-MODE READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)



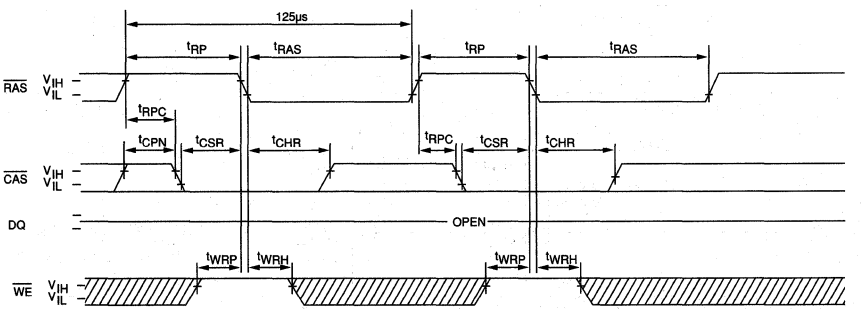
$\overline{RAS}$-ONLY REFRESH CYCLE
(ADDR = A0-A9; $\overline{WE}$ = DON'T CARE)



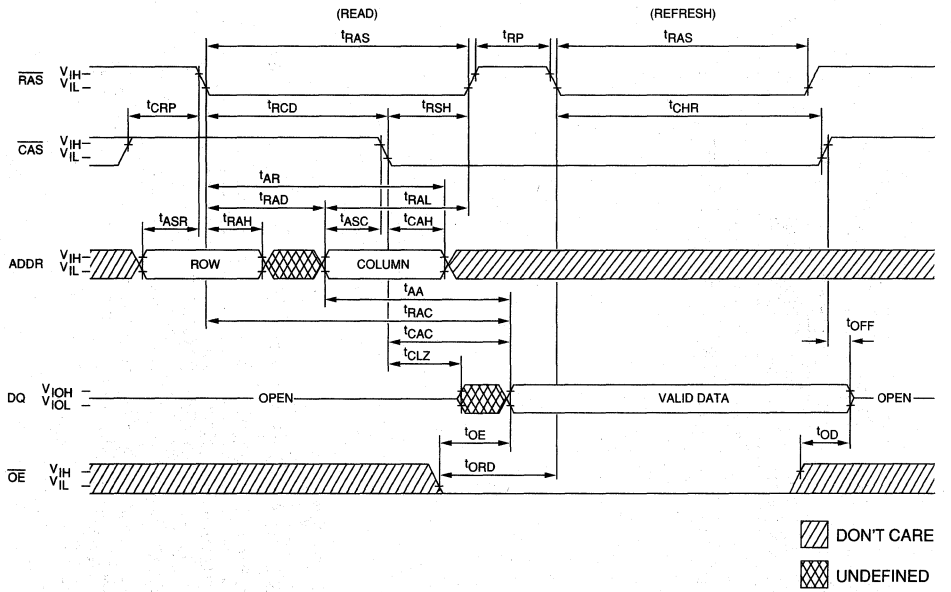
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE
(A0-A9 = DON'T CARE)



BATTERY BACKUP REFRESH CYCLE
(A0-A9 = DON'T CARE)



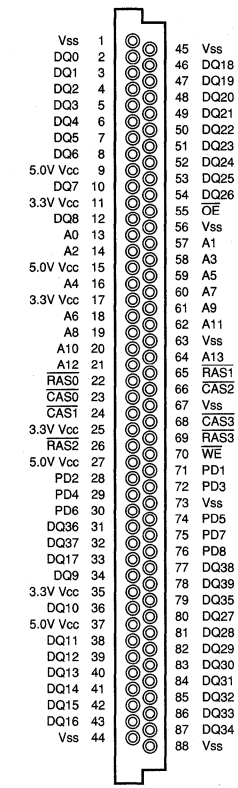
HIDDEN REFRESH CYCLE [21]
($\overline{WE}$ = HIGH)



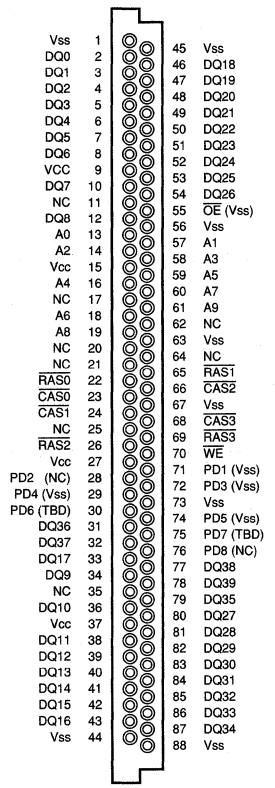
NEW IC DRAM CARD

NEW ■ IC DRAM CARD

RESERVED JEDEC, JEIDA and PCMCIA 88-PIN ASSIGNMENT
(All Possible Combinations)



MT24D88C240 PIN ASSIGNMENT
(JEDEC Standard)



MICRON TECHNOLOGY, INC.

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DUAL PORT DRAM (VRAM) PRODUCT SELECTION GUIDE

Memory Configuration	Access Cycle	Part Number	Access Time (ns)	Power Dissipation		Package and Number of Pins				
				Standby	Active	SOJ	SOG	TSOP	ZIP	Page
256K x 4	FP	MT42C4255	80, 100	15mW	275mW	28	-	-	28	5-1
256K x 4	FP, BW, LP	MT42C4256	70, 80, 100	15mW	275mW	28	-	-	28	5-3
128K x 8	FP	MT42C8127	80, 100	15mW	275mW	40	-	-	-	5-39
128K x 8	FP, BW, LP	MT42C8128	70, 80, 100	15mW	275mW	40	-	40/44	-	5-41
256K x 8	FP, BW	MT42C8255	70, 80	10mW	300mW	40	-	40/44	-	5-79
256K x 8	FP, BW	MT42C8256	70, 80	10mW	300mW	40	-	40/44	-	5-111
256K x 16	FP, BW	MT42C256K16A1	60, 70, 80	10mW	350mW	-	64	-	-	5-153

FP = Fast Page Mode, BW = Block Write, LP = Low Power, Extended Refresh

TRIPLE PORT DRAM PRODUCT SELECTION GUIDE

Memory Configuration	Access Cycle	Part Number	Access Time (ns)	Power Dissipation		Package/Number of Pins				
				Standby	Active	SOJ	SOG	TSOP	PLCC	Page
256K x 4	FP, BW, QSF pin	MT43C4257	80, 100	15mW	500mW	40	-	40/44	-	5-155
256K x 4	FP, BW, SSF pin	MT43C4258	80, 100	15mW	500mW	40	-	40/44	-	5-155
128K x 8	FP, BW, QSF pin	MT43C8128	80, 100	15mW	550mW	-	-	-	52	5-201
128K x 8	FP, BW, SSF pin	MT43C8129	80, 100	15mW	550mW	-	-	-	52	5-201
256K x 8	FP, BW	MT43C256K8A1	60, 70, 80	15mW	400mW	-	64	-	-	5-247

FP = Fast Page Mode, BW = Block Write

VRAM

256K x 4 DRAM WITH 512 x 4 SAM

FEATURES

- Industry standard pinout, timing and functions
- High-performance, CMOS silicon-gate process
- Single +5V ±10% (-10), +5V ±5% (-8S) power supply
- Inputs and outputs are fully TTL compatible
- Refresh modes: $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$ (CBR) and HIDDEN
- 512-cycle refresh within 8ms
- Optional FAST PAGE MODE access cycles
- Dual port organization: 256K x 4 DRAM port
  512 x 4 SAM port
- No refresh required for serial access memory
- Low power: 15mW standby; 275mW active, typical
- Fast access times – 80ns random, 25ns serial

SPECIAL FUNCTIONS

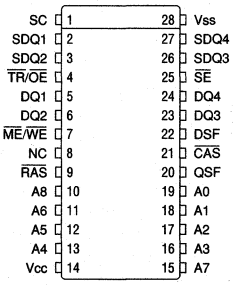
- JEDEC Standard Function set
- PERSISTENT MASKED WRITE
- SPLIT READ TRANSFER
- WRITE TRANSFER/SERIAL INPUT
- ALTERNATE WRITE TRANSFER

OPTIONS MARKING

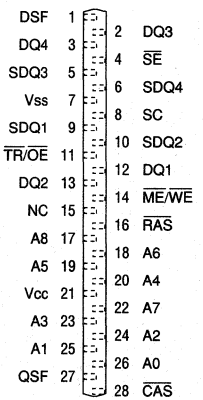
- Timing [DRAM, SAM (cycle/access)]
  80ns, 25ns/25ns -8S
  100ns, 30ns/30ns -10
- Packages
  Plastic SOJ (400 mil) DJ
  Plastic ZIP (375 mil) Z

PIN ASSIGNMENT (Top View)

28-Pin SOJ (Q-4)



28-Pin ZIP (O-3)



GENERAL DESCRIPTION

The MT42C4255 is a high speed, dual port CMOS dynamic random access memory or video RAM (VRAM) containing 1,048,576 bits. These bits may be accessed either by a 4-bit wide DRAM port or by a 512 x 4-bit serial access memory (SAM) port. Data may be transferred bidirectionally between the DRAM and the SAM.

The DRAM portion of the VRAM is functionally identical to the MT4C4256 (256K x 4-bit DRAM). Four 512-bit data registers make up the serial access memory portion of the VRAM. Data I/O and internal data transfer are accomplished using three separate bidirectional data paths: the 4-bit random access I/O port, the four internal 512 bit wide paths between the DRAM and the SAM, and the 4-bit serial I/O port for the SAM. The rest of the circuitry consists of the control, timing, and address decoding logic.

Each port may be operated asynchronously and independently of the other except when data is being transferred internally. As with all DRAMs, the VRAM must be refreshed to maintain data. The refresh cycles must be timed so that all 512 combinations of $\overline{RAS}$ addresses are executed at least every 8ms (regardless of sequence). Micron recommends evenly spaced refresh cycles for maximum data integrity. An internal transfer between the DRAM and the SAM counts as a refresh cycle. The SAM portion of the VRAM is fully static and does not require any refresh.

The operation and control of the MT42C4255 are optimized for high performance graphics and communication designs. The dual port architecture is well suited to buffering the sequential data used in raster graphics display, serial/parallel networking and data communications. Special features such as SPLIT READ TRANSFER, allow further enhancements to system performance.

VRAM

256K x 4 DRAM WITH 512 x 4 SAM

FEATURES

- Industry standard pinout, timing and functions
- High-performance, CMOS silicon-gate process
- Single +5V ±10% power supply
- Inputs and outputs are fully TTL compatible
- Refresh modes: RAS-ONLY, CAS-BEFORE-RAS (CBR) and HIDDEN
- 512-cycle refresh within 8ms, with 32ms option
- Optional FAST PAGE MODE access cycles
- Dual port organization: 256K x 4 DRAM port
  512 x 4 SAM port
- No refresh required for serial access memory
- Low power: 15mW standby; 275mW active, typical
- Fast access times – 70ns random, 22ns serial

SPECIAL FUNCTIONS

- JEDEC Standard Function set
- PERSISTENT MASKED WRITE
- SPLIT READ TRANSFER
- WRITE TRANSFER/SERIAL INPUT
- ALTERNATE WRITE TRANSFER
- BLOCK WRITE

OPTIONS MARKING

- Timing [DRAM, SAM (cycle/access)]
  70ns, 25ns/22ns - 7
  80ns, 30ns/25ns - 8
  100ns, 30ns/27ns -10
- Packages
  Plastic SOJ (400 mil) DJ
  Plastic ZIP (375 mil) Z
- Low power/extended refresh (32ms) L

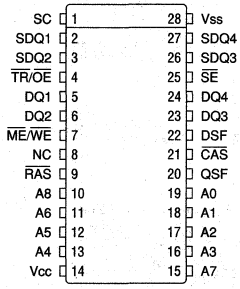
GENERAL DESCRIPTION

The MT42C4256 is a high-speed, dual port CMOS dynamic random access memory or video RAM (VRAM) containing 1,048,576 bits. These bits may be accessed by a 4-bit wide DRAM port or by a 512 x 4-bit serial access memory (SAM) port. Data may be transferred bidirectionally between the DRAM and the SAM. An extended refresh (32ms), low power standby option is available as the MT42C4256 L.

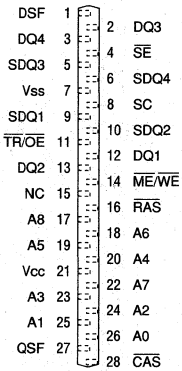
The DRAM portion of the VRAM is functionally identical to the MT4C4256 (256K x 4 DRAM). Four 512-bit data registers make up the SAM portion of the VRAM. Data I/O and internal data transfer are accomplished using three separate bidirectional data paths; the 4-bit random access

PIN ASSIGNMENT (Top View)

28-Pin SOJ (Q-4)



28-Pin ZIP (O-3)

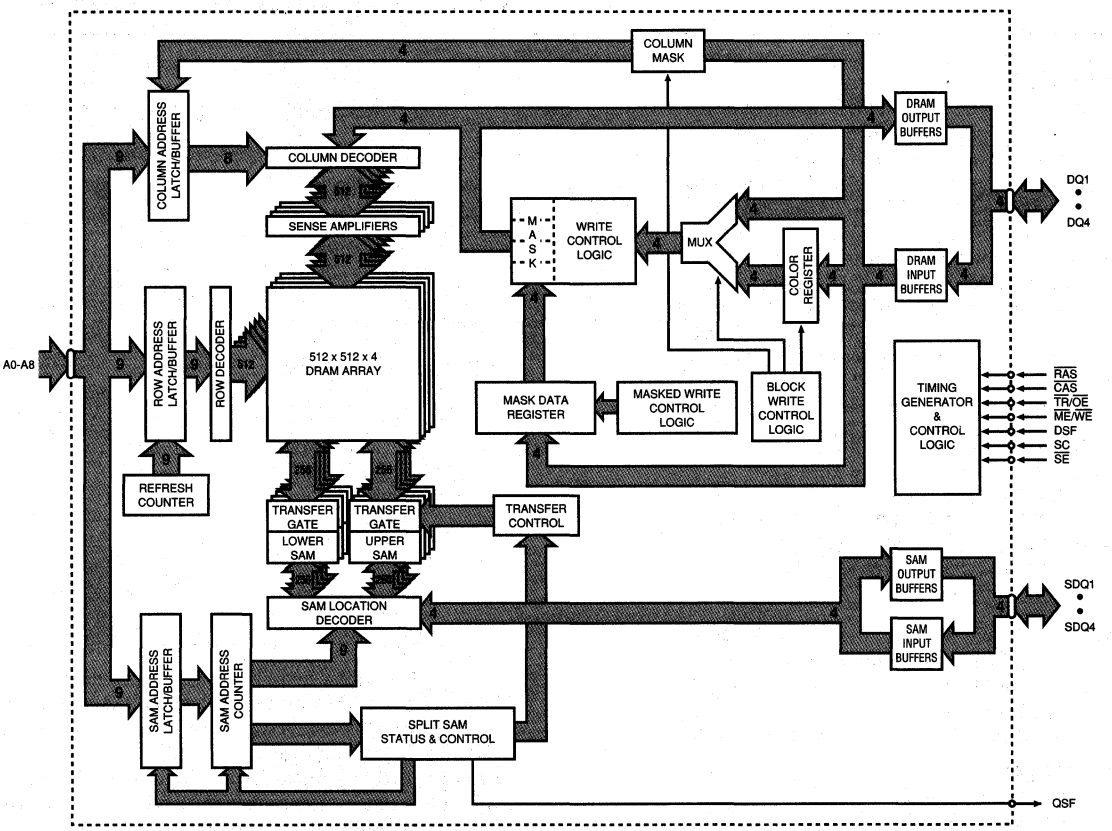


I/O port, the four internal 512 bit wide paths between the DRAM and the SAM, and the 4-bit serial I/O port for the SAM. The rest of the circuitry consists of the control, timing and address decoding logic.

Each port may be operated asynchronously and independently of the other except when data is being transferred internally. As with all DRAMs, the VRAM must be refreshed to maintain data. Refresh cycles must be timed so that all 512 combinations of RAS addresses are executed at least every 8ms, or 32ms for the MT42C4256 L, (regardless of sequence). Micron recommends evenly spaced refresh cycles for maximum data integrity. An internal transfer between the DRAM and the SAM counts as a refresh cycle. The SAM portion of the VRAM is fully static and does not require any refresh.

The operation and control of the MT42C4256 are optimized for high performance graphics and communication designs. The dual port architecture is well suited to buffering the sequential data used in raster graphics display, serial and parallel networking and data communications. Special features, such as SPLIT READ TRANSFER and BLOCK WRITE allow further enhancements to system performance.

FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTIONS

SOJ PIN NUMBERS	ZIP PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
1	8	SC	Input	Serial Clock: Clock input to the serial address counter for the SAM registers.
4	11	$\overline{TR/OE}$	Input	Transfer Enable: Enables an internal TRANSFER operation at $\overline{RAS}$ (H → L), or Output Enable: Enables the DRAM output buffers when taken LOW after $\overline{RAS}$ goes LOW ($\overline{CAS}$ must also be LOW), otherwise the output buffers are in a High-Z state.
7	14	$\overline{ME/WE}$	Input	Mask Enable: If $\overline{ME/WE}$ is LOW at the falling edge of $\overline{RAS}$ a MASKED WRITE cycle is performed, or Write Enable: $\overline{ME/WE}$ is also used to select a READ ($\overline{ME/WE}$ = H) or WRITE ($\overline{ME/WE}$ = L) cycle when accessing the DRAM. This includes a READ TRANSFER ($\overline{ME/WE}$ = H) or WRITE TRANSFER ($\overline{ME/WE}$ = L).
25	4	$\overline{SE}$	Input	Serial Port Enable: $\overline{SE}$ enables the serial I/O buffers and allows a serial READ or WRITE operation to occur, otherwise the output buffers are in a High-Z state. $\overline{SE}$ is also used during a WRITE TRANSFER operation to indicate whether a WRITE TRANSFER or a SERIAL INPUT MODE ENABLE cycle is performed.
22	1	DSF	Input	Special Function Select: DSF is used to indicate which special functions (BLOCK WRITE, MASKED WRITE vs. PERSISTENT MASKED WRITE, etc.) are used on a particular access cycle.
9	16	$\overline{RAS}$	Input	Row Address Strobe: $\overline{RAS}$ is used to clock-in the 9 row-address bits and strobe the $\overline{ME/WE}$, $\overline{TR/OE}$, DSF, $\overline{SE}$, $\overline{CAS}$ and DQ inputs. It also acts as the master chip enable and must fall for initiation of any DRAM or TRANSFER cycle.
21	28	$\overline{CAS}$	Input	Column Address Strobe: $\overline{CAS}$ is used to clock-in the 9 column-address bits, enable the DRAM output buffers (along with $\overline{TR/OE}$), and strobe the DSF input.
19, 18, 17, 16, 13, 12, 11, 15, 10	26, 25, 24, 23, 20, 19, 18, 22, 17	A0-A8	Input	Address Inputs: For the DRAM operation, these inputs are multiplexed and clocked by $\overline{RAS}$ and $\overline{CAS}$ to select one 4-bit word out of the 256K available. During TRANSFER operations, A0 to A8 indicate the DRAM row being accessed (when $\overline{RAS}$ goes LOW) and the SAM start address (when $\overline{CAS}$ goes LOW).
5, 6, 23, 24	12, 13, 2, 3	DQ1-DQ4	Input/ Output	DRAM Data I/O: Data input/output for DRAM cycles; inputs for Mask Data Register and Color Register load cycles, and DQ and Column Mask inputs for BLOCK WRITE.
2, 3, 26, 27	9, 10, 5, 6	SDQ1-SDQ4	Input/ Output	Serial Data I/O: Input, output, or High-Z.
20	27	QSF	Output	Split SAM Status: QSF indicates which half of the SAM is being accessed. LOW if address is 0-255, HIGH if address is 256-511.
8	15	NC	–	No Connect: This pin should be left either unconnected or tied to ground.
14	21	Vcc	Supply	Power Supply: +5V ±10%
28	7	Vss	Supply	Ground

FUNCTIONAL DESCRIPTION

The MT42C4256 may be divided into three functional blocks (see Figure 1): the DRAM, the transfer circuitry, and the SAM. All of the operations described below are shown in the AC Timing Diagrams section of this data sheet and summarized in the Truth Table.

Note: *For dual-function pins, the function not being discussed will be surrounded by parentheses. For example, the TR/OE pin will be shown as TR/(OE) in references to transfer operations.*

DRAM OPERATION

DRAM REFRESH

Like any DRAM based memory, the MT42C4256 VRAM must be refreshed to retain data. All 512 row address combinations must be accessed within 8ms. The MT42C4256 supports CAS-BEFORE-RAS, RAS-ONLY and HIDDEN types of refresh cycles.

For the CAS-BEFORE-RAS REFRESH cycle, the row addresses are generated and stored in an internal address counter. The user need not supply any address data, and simply must perform 512 CAS-BEFORE-RAS cycles within the 8ms time period.

The refresh address must be generated externally and applied to A0-A8 inputs for RAS-ONLY refresh cycles. The DQ pins remain in a High-Z state for both the RAS-ONLY and CAS-BEFORE-RAS refresh cycles.

HIDDEN REFRESH cycles are performed by toggling RAS (and keeping CAS LOW) after a READ or WRITE cycle. This performs CAS-BEFORE-RAS cycles but does not disturb the DQ lines.

Any DRAM READ, WRITE, or TRANSFER cycle also refreshes the DRAM row being accessed. The SAM portion of the MT42C4256 is fully static and does not require any refreshing.

DRAM READ AND WRITE CYCLES

The DRAM portion of the VRAM is nearly identical to standard 256K x 4 DRAMs. However, because several of the DRAM control pins are used for additional functions on this part, several conditions that were undefined or in "don't care" states for the DRAM are specified for the VRAM. These conditions are highlighted in the following discussion. In addition, the VRAM has several special functions that can be used when writing to the DRAM.

The 18 address bits that are used to select a 4-bit word from the 262,144 available are latched into the chip using the A0-A8, RAS and CAS inputs. First, the 9 row-address bits are set up on the address inputs and clocked into the part when RAS transitions from HIGH-to-LOW. Next, the 9 column address bits are set up on the address inputs and clocked-in when CAS goes from HIGH-to-LOW.

Note: *RAS also acts as a "master" chip enable for the VRAM. If RAS is inactive, HIGH, all other DRAM control pins (CAS, TR/OE, ME/WE, etc.) are "don't care" and may change state without effect. No DRAM or TRANSFER cycles will be initiated without RAS falling.*

For single port DRAMs, the OE pin is a "don't care" when RAS goes LOW. However, for the VRAM, when RAS goes LOW, TR/(OE) selects between DRAM access or TRANSFER cycles. TR/(OE) must be HIGH at the RAS HIGH-to-LOW transition for all DRAM operations (except CAS-BEFORE-RAS).

If (ME)/WE is HIGH when CAS goes LOW, a DRAM READ operation is performed and the data from the memory cells selected will appear at the DQ1-DQ4 port. The (TR)/OE input must transition from HIGH-to-LOW some time after RAS falls to enable the DRAM output port.

For single port normal DRAMs, WE is a "don't care" when RAS goes LOW. For the VRAM, ME/(WE) is used, when RAS goes LOW, to select between a MASKED WRITE cycle and a normal WRITE cycle. If ME/(WE) is LOW at the RAS HIGH-to-LOW transition, a MASKED WRITE operation is selected. For any DRAM access cycle (READ or WRITE), ME/(WE) must be HIGH at the RAS HIGH-to-LOW transition. If (ME)/WE is LOW before CAS goes LOW, a DRAM EARLY-WRITE operation is performed and the data present on the DQ1-DQ4 data port will be written into the selected memory cells. If (ME)/WE goes LOW after CAS goes LOW, a DRAM LATE-WRITE operation is performed. Refer to the AC timing diagrams.

The VRAM can perform all the normal DRAM cycles including READ, EARLY-WRITE, LATE-WRITE, READ-MODIFY-WRITE, FAST-PAGE-MODE READ, FAST-PAGE-MODE WRITE (Late or Early), and FAST-PAGE-MODE READ-MODIFY-WRITE. Refer to the AC timing parameters and diagrams in the data sheet for more details on these operations.

NONPERSISTENT MASKED WRITE

The MASKED WRITE feature eliminates the need for a READ-MODIFY-WRITE cycle when changing only specific bits within a 4-bit word. The MT42C4256 supports two types of MASKED WRITE cycles, NONPERSISTENT MASKED WRITE and PERSISTENT MASKED WRITE.

If $\overline{ME}$/($\overline{WE}$) and DSF are LOW at the $\overline{RAS}$ HIGH-to-LOW transition, a NONPERSISTENT MASKED WRITE is performed and the data (mask data) present on the DQ1-DQ4 inputs will be written into the mask data register. The mask data acts as an individual write enable for each of the four DQ1-DQ4 pins. If a LOW (logic "0") is written to a mask data register bit, the input port for that bit is disabled during the subsequent WRITE operation and no new data will be written to that DRAM cell location. A HIGH (logic "1") on a mask data register bit enables the input port and allows normal WRITE operation to proceed. Note that $\overline{CAS}$ is still HIGH. When $\overline{CAS}$ goes LOW, the bits present on the DQ1-DQ4 inputs will be either written to the DRAM (if the mask data bit is HIGH) or ignored (if the mask data bit is LOW). The DRAM contents that correspond to masked input bits will not be changed during the WRITE cycle. The MASKED WRITE is nonpersistent (must be re-entered at every $\overline{RAS}$ cycle) if DSF is LOW when $\overline{RAS}$ goes LOW. The mask data register is cleared at the end of every NONPERSISTENT MASKED WRITE. FAST PAGE MODE can be used with NONPERSISTENT MASKED WRITE to write several column locations in an addressed row. The same mask is used during the entire FAST-PAGE-MODE $\overline{RAS}$ cycle. An example NONPERSISTENT MASKED WRITE cycle is shown in Figure 1.

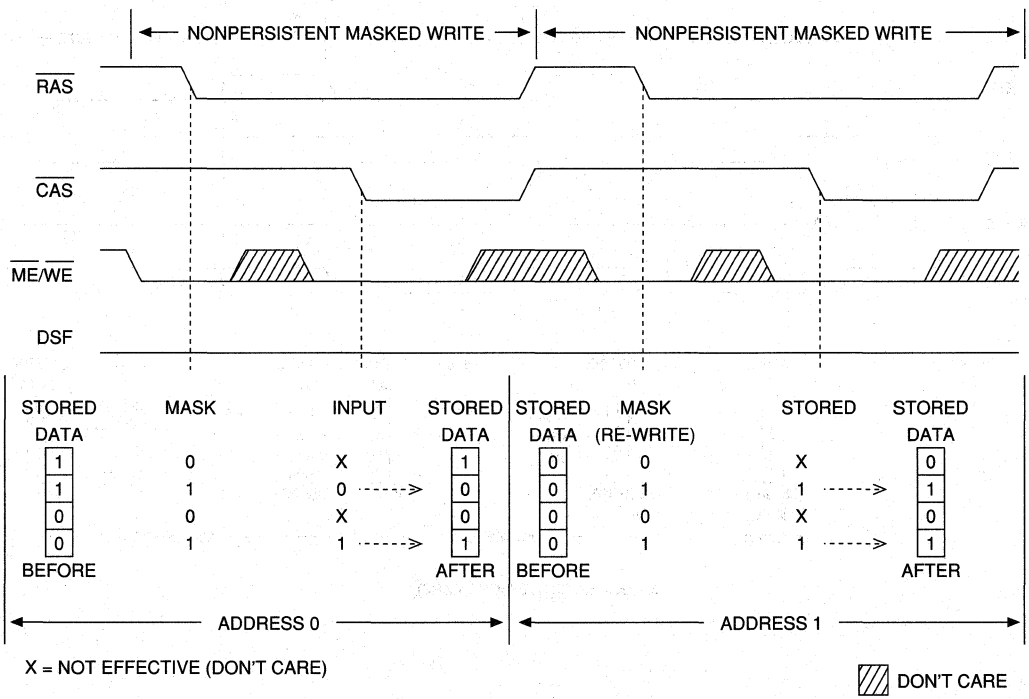


Figure 1
NONPERSISTENT MASKED WRITE EXAMPLE

PERSISTENT MASKED WRITE

The PERSISTENT MASKED WRITE feature eliminates the need to rewrite the mask data before each MASKED WRITE cycle if the same mask data is being used repeatedly. To initiate a PERSISTENT MASKED WRITE, a LOAD MASK REGISTER cycle is performed by taking $\overline{ME}/(\overline{WE})$ and DSF HIGH when $\overline{RAS}$ goes LOW. The mask data is loaded into the internal register when $\overline{CAS}$ goes LOW.

PERSISTENT MASKED WRITE cycles may then be performed by taking $\overline{ME}/(\overline{WE})$ LOW and DSF HIGH when $\overline{RAS}$ goes LOW. The contents of the mask data register will then be used as the mask data for the DRAM inputs. Unlike the NONPERSISTENT MASKED WRITE cycle, the data present on the DQ inputs is not loaded into the mask register when $\overline{RAS}$ falls, and the mask data register will not be cleared at the end of the cycle. Any number of PERSISTENT MASKED WRITE cycles, to any address, may be performed without having to reload the mask data register. Figure 2 shows the LOAD MASK REGISTER and two PERSISTENT MASKED WRITE cycles in operation. The LOAD MASK REGISTER and PERSISTENT MASKED WRITE cycles allow controllers that cannot provide mask data to the DQ pins at $\overline{RAS}$ time to perform MASKED WRITE operations. PERSISTENT MASKED WRITE operations may be performed during FAST PAGE MODE cycles and the same mask will apply to all addressed columns in the addressed row.

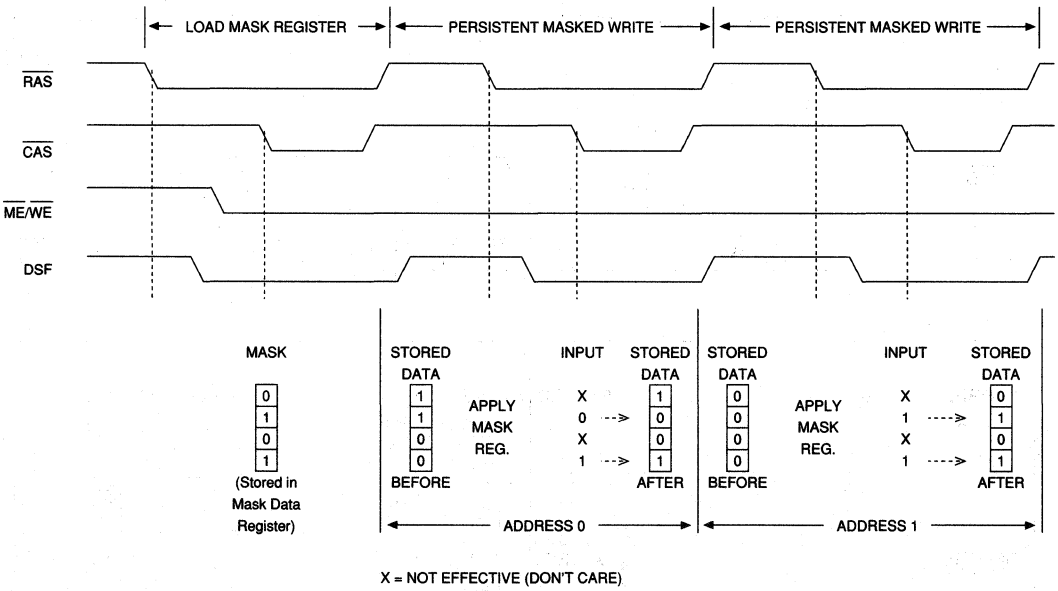


Figure 2
PERSISTENT MASKED WRITE EXAMPLE

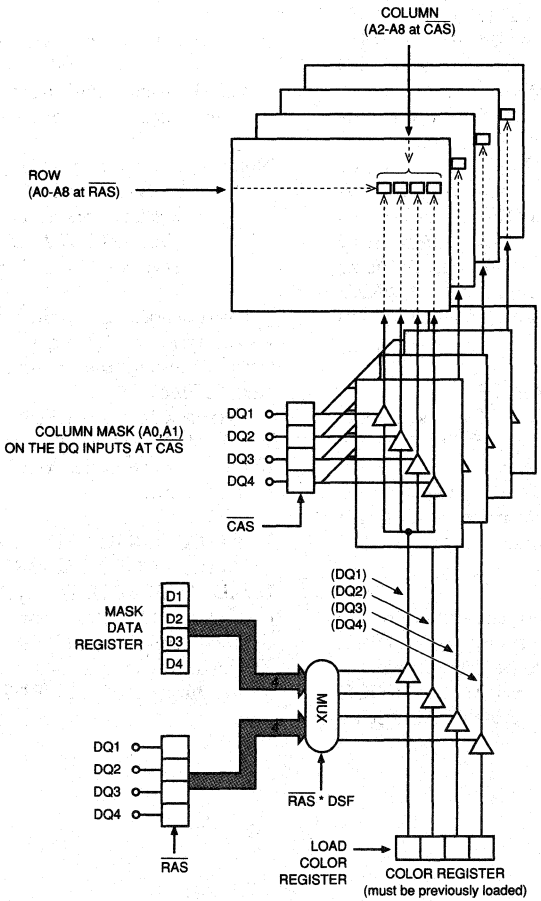


Figure 3
BLOCK WRITE EXAMPLE

BLOCK WRITE

If DSF is HIGH when $\overline{CAS}$ goes LOW, the MT42C4256 will perform a BLOCK WRITE cycle instead of a normal WRITE cycle. In BLOCK WRITE cycles, the contents of the color register are directly written to four adjacent column locations (see Figure 3). The color register must be loaded prior to beginning BLOCK WRITE cycles (see LOAD COLOR REGISTER). Each DQ location of the color register is written to the four column locations (or any of the four that are enabled) in the corresponding DQ bit plane.

The row is addressed as in a normal DRAM WRITE cycle. However, when $\overline{CAS}$ goes LOW only the A2-A8 inputs are used. A2-A8 specify the "block" of four adjacent column locations that will be accessed. The DQ inputs are then used to determine what combination of the four column locations will be changed. DQ1 acts as a write enable for column location A0 = 0, A1 = 0; DQ2 controls column location A0 = 1, A1 = 0; DQ3 controls A0 = 0, A1 = 1; and DQ4 controls A0 = 1, A1 = 1. The write enable controls are active HIGH; the WRITE function is enabled by a logic 1 and disabled by a logic 0.

NONPERSISTENT MASKED BLOCK WRITE

The MASKED WRITE functions can also be used during BLOCK WRITE cycles. NONPERSISTENT MASKED BLOCK WRITE operates exactly like the normal NONPERSISTENT MASKED WRITE, except that the mask is now applied to four column locations instead of just one.

Like NONPERSISTENT MASKED WRITE, the combination of $\overline{ME}$/($\overline{WE}$) LOW and DSF LOW when $\overline{RAS}$ goes LOW initiates a NONPERSISTENT MASKED cycle. The DSF pin must be driven HIGH when $\overline{CAS}$ goes LOW, to perform the NONPERSISTENT MASKED BLOCK WRITE. By using both the column mask input and the MASKED WRITE function, any combination of the four bit planes or column locations may be masked.

PERSISTENT MASKED BLOCK WRITE

This cycle is also performed exactly like the normal PERSISTENT MASKED WRITE except that DSF is HIGH when $\overline{CAS}$ goes LOW to indicate the BLOCK WRITE function. Both the mask data register and the color register must be loaded with the appropriate data prior to starting a PERSISTENT MASKED BLOCK WRITE.

LOAD MASK DATA REGISTER

The LOAD MASK REGISTER operation and timing are identical to a normal WRITE cycle except that DSF is HIGH when $\overline{RAS}$ goes LOW. As shown in the Truth Table, the combination of $\overline{TR}$/($\overline{OE}$), $\overline{ME}$/($\overline{WE}$), and DSF being HIGH when $\overline{RAS}$ goes LOW indicates the cycle is a LOAD REGISTER cycle. DSF is used when $\overline{CAS}$ goes LOW to select the register to be loaded and must be LOW for a LOAD MASK REGISTER cycle. The data present on the DQ lines will then be written to the mask data register.

Note: *For a normal DRAM WRITE cycle, the mask data register is disabled but not modified. The contents of mask data register will not be changed unless a NONPERSISTENT MASKED WRITE cycle or a LOAD MASK REGISTER cycle is performed.*

The row address supplied will be refreshed, but it is not necessary to provide any particular row address. The column address inputs are ignored during a LOAD MASK REGISTER cycle.

The mask data register contents are used during PERSISTENT MASKED WRITE and PERSISTENT MASKED BLOCK WRITE cycles to selectively enable writes to the four DQ planes.

LOAD COLOR REGISTER

A LOAD COLOR REGISTER cycle is identical to the LOAD MASK REGISTER cycle except DSF is HIGH when $\overline{CAS}$ goes LOW. The contents of the color register are retained until changed by another LOAD COLOR REGISTER cycle (or the part loses power) and are used as data inputs during BLOCK WRITE cycles.

TRANSFER OPERATIONS

TRANSFER operations are initiated when $\overline{TR}/(\overline{OE})$ is LOW then $\overline{RAS}$ goes LOW. The state of $(\overline{ME})/\overline{WE}$ when $\overline{RAS}$ goes LOW indicates the direction of the TRANSFER (to or from the DRAM), and DSF is used to select between NORMAL TRANSFER, SPLIT READ TRANSFER, and ALTERNATE WRITE TRANSFER cycles. Each of the TRANSFER cycles available is described below.

READ TRANSFER (DRAM-TO-SAM TRANSFER)

If $(\overline{ME})/\overline{WE}$ is HIGH and DSF is LOW when $\overline{RAS}$ goes LOW, a READ TRANSFER cycle is selected. The row address bits indicate the four 512-bit DRAM row planes that are to be transferred to the four SAM data register planes. The column address bits indicate the start address (or Tap address) of the serial output cycle from the SAM data registers. $\overline{CAS}$ must fall for every TRANSFER in order to load a valid Tap address. A read transfer may be accomplished in two ways. If the transfer is to be synchronized with SC (REAL-TIME READ TRANSFER), $\overline{TR}/(\overline{OE})$ is taken HIGH after $\overline{CAS}$ goes LOW. If the transfer does not have to be synchronized with SC (READ TRANSFER), $\overline{TR}/(\overline{OE})$ may go HIGH before $\overline{CAS}$ goes LOW (refer to the AC Timing Diagrams). The 2,048 bits of DRAM data are written into the SAM data registers and the serial shift start address is stored in an internal 9-bit register. QSF will be LOW if access is from the lower half (addresses 0 through 255), and HIGH if access is from the upper half (256 through 511). If $\overline{SE}$ is LOW, the first bits of the new row data will appear at the serial outputs with the first SC clock pulse. $\overline{SE}$ enables the serial outputs and may be either HIGH or LOW during this operation. The SAM address pointer will increment with the SC LOW-to-HIGH transition, regardless of the state of $\overline{SE}$. Performing a READ TRANSFER cycle sets the direction of the SAM I/O buffers to the output mode.

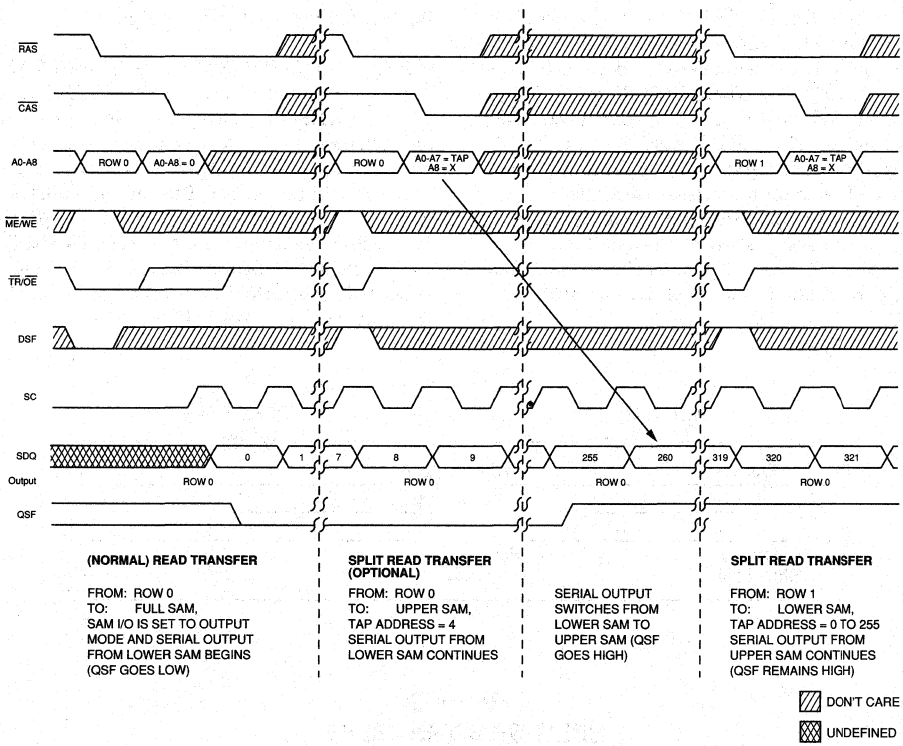


Figure 4
TYPICAL SPLIT-READ-TRANSFER INITIATION SEQUENCE

SPLIT READ TRANSFER (SPLIT DRAM-TO-SAM TRANSFER)

The SPLIT READ TRANSFER (SRT) cycle eliminates the critical transfer timing required to maintain a continuous serial output data stream. When using normal TRANSFER cycles, the REAL-TIME READ TRANSFER cycle has to occur immediately after the last bit of "old data" was clocked out of the SAM port.

When using the SPLIT TRANSFER mode, the SAM is divided into an upper half and a lower half. While data is being serially read from one half of the SAM, new DRAM data may be transferred to the other half. The transfer may occur at any time while the other half is sending data and need not be synchronized with the SC clock.

The $\overline{TR}/(\overline{OE})$ timing is also relaxed for SPLIT TRANSFER cycles. The rising edge of $\overline{TR}/(\overline{OE})$ is not used to complete the TRANSFER cycle and therefore is independent of the rising edges of $\overline{RAS}$ or $\overline{CAS}$. The transfer timing is generated internally for SPLIT TRANSFER cycles. A SPLIT READ TRANSFER does not change the direction of the SAM port.

A normal, non-split READ TRANSFER cycle must precede any sequence of SPLIT READ TRANSFER cycles to set SAM I/O direction and provide a reference to which half of the SAM the access will begin. Then SPLIT READ TRANSFERS may be initiated by taking DSF HIGH when $\overline{RAS}$ goes LOW during the TRANSFER cycle. As in nonsplit transfers, the row address is used to specify the DRAM row to be transferred. The column address, A0-A7, is used to input the SAM Tap address. Address pin A8 is a "don't care" when the Tap address is loaded at the HIGH-to-LOW transition of $\overline{CAS}$. It is internally generated so that the SPLIT TRANSFER will be to the SAM half not currently being accessed.

Figure 4 shows a typical SPLIT READ TRANSFER initiation sequence. The normal READ TRANSFER is first performed, followed by a SPLIT READ TRANSFER of the same row to the upper half of the SAM. The SRT to the upper half is optional and need only be done if the Tap for the upper half is ≠ 0. Serial access continues, and when the SAM address counter reaches 255 ("A8" = 0, A0-A7 = 1), the new Tap address is loaded for the next half ("A8" = 1, A0-A7 = Tap) and the QSF output goes HIGH. Once the serial access has switched to the upper SAM, new data may be transferred to the lower SAM. The controller must wait for the state of QSF to change and then the new data may be transferred to the SAM half not being accessed. For example, the next step in Figure 4 would be to wait until QSF went LOW (indicating that row-1 data is shifting out of the lower SAM) and then transfer the upper half of row 1 to the upper SAM. If the half boundary is reached before an SRT is done for the next half a Tap address of "0" will be used. Access will start at 0 if going to the lower half, or 256 if going to the upper half. See Figure 5.

WRITE TRANSFER (SAM-TO-DRAM TRANSFER)

The operation of the WRITE TRANSFER is identical to the READ TRANSFER described previously except $(\overline{ME})/\overline{WE}$ and $\overline{SE}$ must be LOW when $\overline{RAS}$ goes LOW. The row address indicates the DRAM row to which the SAM data registers will be written. The column address (Tap) indicates the starting address of the next SERIAL INPUT cycle for the SAM data registers. A WRITE TRANSFER changes the direction of the SAM I/O buffers to the input mode. QFS is LOW if access is to the lower half of the SAM, and HIGH if access is to the upper half.

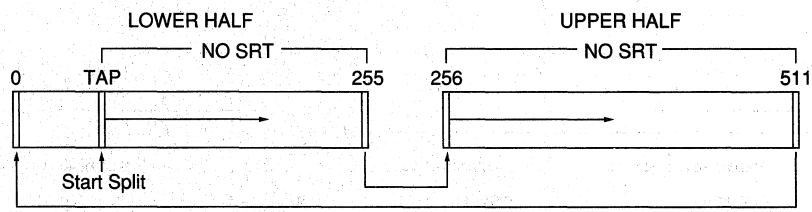


Figure 5
SPLIT SAM TRANSFER

PSEUDO WRITE TRANSFER (SERIAL-INPUT-MODE ENABLE)

The PSEUDO WRITE TRANSFER cycle is used to change the direction of SAM port from output to input without performing a WRITE TRANSFER cycle. A PSEUDO WRITE TRANSFER cycle is a WRITE TRANSFER cycle with $\overline{SE}$ held HIGH instead of LOW. The DRAM data will not be disturbed and the SAM will be ready to accept input data.

ALTERNATE WRITE TRANSFER (SAM-TO-DRAM TRANSFER)

The operation of the ALTERNATE WRITE TRANSFER is identical to the WRITE TRANSFER except that the DSF pin is HIGH and $(\overline{ME})/\overline{WE}$ is LOW when $\overline{RAS}$ goes LOW, allowing $\overline{SE}$ to be a "don't care." This allows the outputs to be disabled using $\overline{SE}$ during a WRITE TRANSFER cycle. ALTERNATE WRITE TRANSFER will change the SAM I/O direction to an input condition.

SERIAL INPUT AND SERIAL OUTPUT

The control inputs for SERIAL INPUT and SERIAL OUTPUT are SC and $\overline{SE}$. The rising edge of SC increments the serial address counter and provides access to the next SAM location. $\overline{SE}$ enables or disables the serial input/output buffers.

Serial output of the SAM contents will start at the serial start address that was loaded in the SAM address counter during a READ or SPLIT READ TRANSFER cycle. The SC input increments the address counter and presents the contents of the next SAM location to the 4-bit port. $\overline{SE}$ is used as an output enable during the SAM output operation. The serial address is automatically incremented with every SC LOW-to-HIGH transition, regardless of whether $\overline{SE}$ is HIGH or LOW. The address progresses through the SAM and will wrap around (after count 255 or 511) to the Tap address of the next half for split modes. If an SRT was not performed before the half boundary is reached the count will progress as illustrated in Figure 5. Address count will wrap around (after count 511) to Tap address 0 if in the "full" SAM modes.

SC is also used to clock-in data when the device is in the serial input mode. As in the serial output operation, the contents of the SAM address counter (loaded when the serial input mode was enabled) will determine the serial address of the first 4-bit word written. $\overline{SE}$ acts as a write enable for serial input data and must be LOW for valid serial input. If $\overline{SE}$ = HIGH, the data inputs are disabled and the SAM contents will not be modified. The serial address counter is incremented with every LOW-to-HIGH transition of SC, regardless of the logic level on the $\overline{SE}$ input.

POWER-UP AND INITIALIZATION

After Vcc is at specified operating conditions, for 100µs minimum, eight $\overline{RAS}$ cycles must be executed to initialize the dynamic memory array. Micron recommends that $\overline{RAS} = (\overline{TR})/\overline{OE} \geq V_{IH}$ during power up to ensure that the DRAM I/O pins (DQs) are in a High-Z state. The DRAM array will contain random data.

The SAM portion of the MT42C4256 is completely static in operation and does not require refresh or initialization. The SAM port will power-up in the serial input mode (WRITE TRANSFER) and the I/O pins (SDQs) will be High-Z, regardless of the state of $\overline{SE}$. The mask and color register will contain random data after power-up. QSF initializes in the LOW state.

TRUTH TABLE

CODE	FUNCTION	RAS FALLING EDGE					CAS FALL	A0-A8[1]		DQ1-DQ4[2]		REGISTERS	
		CAS	TR/OE	ME/WE	DSF	SE	DSF	RAS	CAS	RAS	CAS,WE[3]	MASK	COLOR
	DRAM OPERATIONS												
CBR	CAS-BEFORE-RAS REFRESH	0	X	X	X	X	X	—	X	—	X	X	X
ROR	RAS-ONLY REFRESH	1	1	X	X	X	—	ROW	—	X	—	X	X
RW	NORMAL DRAM READ OR WRITE	1	1	1	0	X	0	ROW	COLUMN	X	VALID	X	X
RWNM	NONPERSISTENT (LOAD AND USE) MASKED WRITE TO DRAM	1	1	0	0	X	0	ROW	COLUMN	WRITE MASK	VALID DATA	LOAD & USE	X
RWOM	PERSISTENT (USE REGISTER) MASKED WRITE TO DRAM	1	1	0	1	X	0	ROW	COLUMN	X	VALID DATA	USE	X
BW	BLOCK WRITE TO DRAM (NO DATA MASK)	1	1	1	0	X	1	ROW	COLUMN (A2-A8)	X	COLUMN MASK	X	USE
BWNM	NONPERSISTENT (LOAD & USE) MASKED BLOCK WRITE TO DRAM	1	1	0	0	X	1	ROW	COLUMN	WRITE MASK	COLUMN MASK	LOAD & USE	USE
BWOM	PERSISTENT (USE MASK REGISTER) MASKED BLOCK WRITE TO DRAM	1	1	0	1	X	1	ROW	COLUMN (A2-A8)	X	COLUMN MASK	USE	USE
	REGISTER OPERATIONS												
LMR	LOAD MASK REGISTER	1	1	1	1	X	0	ROW[4]	X	X	WRITE MASK	LOAD	X
LCR	LOAD COLOR REGISTER	1	1	1	1	X	1	ROW[4]	X	X	COLOR DATA	X	LOAD
	TRANSFER OPERATIONS												
RT	READ TRANSFER (DRAM-TO-SAM TRANSFER)	1	0	1	0	X	X	ROW	TAP[5]	X	X	X	X
SRT	SPLIT READ TRANSFER (SPLIT DRAM-TO-SAM TRANSFER)	1	0	1	1	X	X	ROW	TAP[5]	X	X	X	X
WT	WRITE TRANSFER (SAM-TO-DRAM TRANSFER)	1	0	0	0	0	X	ROW	TAP[5]	X	X	X	X
PWT	PSEUDO WRITE TRANSFER (SERIAL-INPUT-MODE ENABLE)	1	0	0	0	1	X	ROW[4]	TAP[5]	X	X	X	X
AWT	ALTERNATE WRITE TRANSFER (SAM-TO-DRAM TRANSFER)	1	0	0	1	X	X	ROW	TAP[5]	X	X	X	X

NOTE:
1. These columns show what must be present on the A0-A8 inputs when RAS falls and when CAS falls.
2. These columns show what must be present on the DQ1-DQ4 inputs when RAS falls and when CAS falls.
3. On WRITE cycles (except BLOCK WRITE), the input data is latched at the falling edge of CAS or ME/WE, whichever is later. Similarly, on READ cycles, the output data is activated at the falling edge of CAS or TR/OE, whichever is later.
4. The ROW that is addressed will be refreshed, but no particular ROW address is required.
5. This is the SAM location that the first SC cycle will access. For split SAM transfers, the Tap will be the first address location accessed of the "new" SAM half after the boundary of the current half is reached (255 for lower half, 511 for upper half).

ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc Supply Relative to Vss ..... -1V to +7V
Operating Temperature, T_A (Ambient) ..... 0°C to +70°C
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	Vcc	4.5	5.5	V	1
Input High (Logic 1) Voltage, All Inputs	VIH	2.4	Vcc+1	V	1
Input Low (Logic 0) Voltage, All Inputs	VIL	-1.0	0.8	V	1

DC ELECTRICAL CHARACTERISTICS

(0°C ≤ T_A ≤ 70°C; Vcc = 5V ±10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
INPUT LEAKAGE CURRENT Any input (0V ≤ VIN ≤ Vcc); all other pins not under test = 0V	IL	-10	10	µA	
OUTPUT LEAKAGE CURRENT (DQ, SDQ disabled, 0V ≤ VOUT ≤ Vcc)	IOZ	-10	10	µA	
OUTPUT LEVELS Output High Voltage (IOUT = -2.5mA)	VOH	2.4		V	1
Output Low Voltage (IOUT = 2.5mA)	VOL		0.4	V	

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A8	CI1		5	pF	2
Input Capacitance: $\overline{RAS}$, $\overline{CAS}$, $\overline{ME}$/$\overline{WE}$, $\overline{TR}$/$\overline{OE}$, SC, $\overline{SE}$, DSF	CI2		7	pF	2
Input/Output Capacitance: DQ, SDQ	CI/O		9	pF	2
Output Capacitance: QSF	CO		9	pF	2

CURRENT DRAIN, SAM IN STANDBY

(0°C ≤ T_A ≤ 70°C; Vcc = 5V ±10%)

		MAX				
PARAMETER/CONDITION	**SYMBOL**	**-7**	**-8**	**-10**	**UNITS**	**NOTES**
OPERATING CURRENT ($\overline{RAS}$ and $\overline{CAS}$ = Cycling: ^tRC = ^tRC (MIN))	I_{CC1}	95	85	75	mA	3, 4 26
OPERATING CURRENT: FAST PAGE MODE ($\overline{RAS}$ = V_{IL}; $\overline{CAS}$ = Cycling: ^tPC = ^tPC (MIN))	I_{CC2}	85	75	65	mA	3, 4 27
STANDBY CURRENT: TTL INPUT LEVELS Power supply standby current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH} after 8 $\overline{RAS}$ cycles (MIN), other inputs ≥ V_{IH} or ≤ V_{IL})	I_{CC3}	8	8	8	mA	4
STANDBY CURRENT: CMOS INPUT LEVELS (MT42C4256 L only) ($\overline{RAS}$ = $\overline{CAS}$ ≥ Vcc -0.2V, other inputs ≥ Vcc -0.2V or ≤ -0.2V)	I_{CC4}	500	500	500	µA	4
REFRESH CURRENT: $\overline{RAS}$-ONLY ($\overline{RAS}$ = Cycling; $\overline{CAS}$ = V_{IH})	I_{CC5}	95	85	75	mA	3, 26
REFRESH CURRENT: $\overline{CAS}$-BEFORE-$\overline{RAS}$ ($\overline{RAS}$ and $\overline{CAS}$ = Cycling)	I_{CC6}	95	85	75	mA	3, 5
REFRESH CURRENT: BATTERY BACKUP (BBU) MT42C4256 L only Average power supply current during BATTERY BACKUP refresh: $\overline{CAS}$ ≤ 0.2V or $\overline{CAS}$-BEFORE-$\overline{RAS}$ cycling; $\overline{RAS}$ = ^tRAS (MIN) to 300ns; $\overline{ME}$/$\overline{WE}$, A0-A8 and DQs ≥ Vcc - 0.2V or ≤ 0.2V (DQs may be left open), ^tRC = 62.5µs (512 rows at 62.5µs = 32ms)	I_{CC7}	600	600	600	µA	3, 5
SAM/DRAM DATA TRANSFER	I_{CC8}	105	95	95	mA	3

CURRENT DRAIN, SAM ACTIVE (^tSC = MIN)

(0°C ≤ T_A ≤ 70°C; Vcc = 5V ±10%)

		MAX				
PARAMETER/CONDITION	**SYMBOL**	**-7**	**-8**	**-10**	**UNITS**	**NOTES**
OPERATING CURRENT ($\overline{RAS}$ and $\overline{CAS}$ = Cycling: ^tRC = ^tRC (MIN))	I_{CC9}	150	130	120	mA	3, 4, 26
OPERATING CURRENT: FAST PAGE MODE ($\overline{RAS}$ = V_{IL}; $\overline{CAS}$ = Cycling: ^tPC = ^tPC (MIN))	I_{CC10}	140	120	110	mA	3, 4, 27
STANDBY CURRENT: TTL INPUT LEVELS Power supply standby current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH} after 8 $\overline{RAS}$ cycles (MIN), other inputs ≥ V_{IH} or ≤ V_{IL})	I_{CC11}	55	45	45	mA	3, 4
REFRESH CURRENT: $\overline{RAS}$-ONLY ($\overline{RAS}$ = Cycling; $\overline{CAS}$ = V_{IH})	I_{CC12}	150	130	120	mA	3, 4, 26
REFRESH CURRENT: $\overline{CAS}$-BEFORE-$\overline{RAS}$ ($\overline{RAS}$ and $\overline{CAS}$ = Cycling)	I_{CC13}	150	130	120	mA	3, 4, 5
SAM/DRAM DATA TRANSFER	I_{CC14}	160	130	125	mA	3, 4

DRAM TIMING PARAMETERS

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C ≤ T_A ≤ +70°C; Vcc = 5V ±10%)

AC CHARACTERISTICS		-7		-8		-10			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Random READ or WRITE cycle time	^tRC	130		150		180		ns	
READ-MODIFY-WRITE cycle time	^tRWC	175		190		230		ns	
FAST-PAGE-MODE READ or WRITE cycle time	^tPC	45		50		55		ns	
FAST-PAGE-MODE READ-MODIFY-WRITE cycle time	^tPRWC	90		95		110		ns	
Access time from $\overline{RAS}$	^tRAC		70		80		100	ns	14
Access time from $\overline{CAS}$	^tCAC		20		25		25	ns	15
Access time from ($\overline{TR}$)/$\overline{OE}$	^tOE		20		20		25	ns	
Access time from column address	^tAA		35		40		45	ns	
Access time from $\overline{CAS}$ precharge	^tCPA		40		45		50	ns	
$\overline{RAS}$ pulse width	^tRAS	70	20,000	80	20,000	100	20,000	ns	
$\overline{RAS}$ pulse width (FAST PAGE MODE)	^tRASP	70	100,000	80	100,000	100	100,000	ns	
$\overline{RAS}$ hold time	^tRSH	20		25		25		ns	
$\overline{RAS}$ precharge time	^tRP	50		60		70		ns	
$\overline{CAS}$ pulse width	^tCAS	20	10,000	25	10,000	25	10,000	ns	
$\overline{CAS}$ hold time	^tCSH	70		80		100		ns	
$\overline{CAS}$ precharge time	^tCP	10		10		10		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	^tRCD	20	50	20	55	25	75	ns	17
$\overline{CAS}$ to $\overline{RAS}$ precharge time	^tCRP	10		10		10		ns	
Row address setup time	^tASR	0		0		0		ns	
Row address hold time	^tRAH	10		10		15		ns	
$\overline{RAS}$ to column address delay time	^tRAD	15	35	15	40	20	50	ns	18
Column address setup time	^tASC	0		0		0		ns	
Column address hold time	^tCAH	15		15		15		ns	
Column address hold time (referenced to $\overline{RAS}$)	^tAR	45		55		70		ns	
Column address to $\overline{RAS}$ lead time	^tRAL	35		40		50		ns	
Read command setup time	^tRCS	0		0		0		ns	
Read command hold time (referenced to $\overline{CAS}$)	^tRCH	0		0		0		ns	19
Read command hold time (referenced to $\overline{RAS}$)	^tRRH	0		0		0		ns	19
$\overline{CAS}$ to output in Low-Z	^tCLZ	3		3		3		ns	
Output buffer turn-off delay	^tOFF	3	20	3	20	3	20	ns	20, 23
Output disable	^tOD	3	10	3	10	3	20	ns	20, 23
Output disable hold time from start of WRITE	^tOEH	10		10		20		ns	25
$\overline{OE}$ LOW to $\overline{RAS}$ HIGH delay time	^tROH	0		0		0		ns	

DRAM TIMING PARAMETERS (continued)

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C ≤ T_A ≤ +70°C; Vcc = 5V ±10%)

AC CHARACTERISTICS		-7		-8		-10			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Write command setup time	tWCS	0		0		0		ns	21
Write command hold time	tWCH	15		15		15		ns	
Write command hold time (referenced to $\overline{RAS}$)	tWCR	45		55		70		ns	
Write command pulse width	tWP	15		15		15		ns	
Write command to $\overline{RAS}$ lead time	tRWL	20		20		20		ns	
Write command to $\overline{CAS}$ lead time	tCWL	20		20		20		ns	
Data-in setup time	tDS	0		0		0		ns	22
Data-in hold time	tDH	15		15		15		ns	22
Data-in hold time (referenced to $\overline{RAS}$)	tDHR	45		55		65		ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	tRWD	90		100		130		ns	21
Column address to $\overline{WE}$ delay time	tAWD	55		65		75		ns	21
$\overline{CAS}$ to $\overline{WE}$ delay time	tCWD	40		45		55		ns	21
Transition time (rise or fall)	tT	3	35	3	35	3	35	ns	9, 10
Refresh period (512 cycles)	tREF		8 (32)		8 (32)		8 (32)	ms	29
$\overline{RAS}$ to $\overline{CAS}$ precharge time	tRPC	0		0		0		ns	
$\overline{CAS}$ setup time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH)	tCSR	10		10		10		ns	5
$\overline{CAS}$ hold time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH)	tCHR	10		10		10		ns	5
$\overline{ME}$/$\overline{WE}$ to $\overline{RAS}$ setup time	tWSR	0		0		0		ns	
$\overline{ME}$/$\overline{WE}$ to $\overline{RAS}$ hold time	tRWH	15		15		15		ns	
Mask Data to $\overline{RAS}$ setup time	tMS	0		0		0		ns	
Mask Data to $\overline{RAS}$ hold time	tMH	15		15		15		ns	

TRANSFER AND MODE CONTROL TIMING PARAMETERS

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes 6, 7, 8, 9, 10) (0° C ≤ T_A ≤ + 70°C; Vcc = 5V ±10%)

AC CHARACTERISTICS		-7		-8		-10			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
$\overline{TR}$/($\overline{OE}$) LOW to $\overline{RAS}$ setup time	^tTLS	0		0		0		ns	
$\overline{TR}$/($\overline{OE}$) LOW to $\overline{RAS}$ hold time	^tTLH	15	10,000	15	10,000	15	10,000	ns	
$\overline{TR}$/($\overline{OE}$) LOW to $\overline{RAS}$ hold time (REAL-TIME READ TRANSFER only)	^tRTH	65	10,000	70	10,000	80	10,000	ns	
$\overline{TR}$/($\overline{OE}$) LOW to $\overline{CAS}$ hold time (REAL-TIME READ TRANSFER only)	^tCTH	25		25		25		ns	
$\overline{TR}$/($\overline{OE}$) HIGH to SC lead time	^tTSL	5		5		5		ns	
$\overline{TR}$/($\overline{OE}$) HIGH to $\overline{RAS}$ precharge time	^tTRP	50		60		70		ns	
$\overline{TR}$/($\overline{OE}$) precharge time	^tTRW	20		20		30		ns	
First SC edge to $\overline{TR}$/($\overline{OE}$) HIGH delay time	^tTSD	15		15		15		ns	
Serial output buffer turn-off delay from $\overline{RAS}$	^tSDZ	7	40	7	40	7	40	ns	
SC to $\overline{RAS}$ setup time	^tSRS	25		30		30		ns	
Serial data input to $\overline{SE}$ delay time	^tSZE	0		0		0		ns	
Serial data input delay from $\overline{RAS}$	^tSDD	50		50		50		ns	
Serial data input to $\overline{RAS}$ delay time	^tSZS	0		0		0		ns	
Serial-input-mode enable ($\overline{SE}$) to $\overline{RAS}$ setup time	^tESR	0		0		0		ns	
Serial-input-mode enable ($\overline{SE}$) to $\overline{RAS}$ hold time	^tREH	15		15		15		ns	
$\overline{TR}$/($\overline{OE}$) HIGH to $\overline{RAS}$ setup time	^tYS	0		0		0		ns	
$\overline{TR}$/($\overline{OE}$) HIGH to $\overline{RAS}$ hold time	^tYH	15		15		15		ns	
DSF to $\overline{RAS}$ setup time	^tFSR	0		0		0		ns	
DSF to $\overline{RAS}$ hold time	^tRFH	15		15		15		ns	
SC to QSF delay time	^tSQD		30		30		30	ns	
SPLIT TRANSFER setup time	^tSTS	25		30		30		ns	
SPLIT TRANSFER hold time	^tSTH	0		0		0		ns	
$\overline{RAS}$ to QSF delay time	^tRQD		75		75		75	ns	
DSF to $\overline{RAS}$ hold time	^tFHR	45		55		70		ns	
DSF to $\overline{CAS}$ setup time	^tFSC	0		0		0		ns	
DSF to $\overline{CAS}$ hold time	^tCFH	15		15		20		ns	
$\overline{TR}$/$\overline{OE}$ to QSF delay time	^tTQD		25		25		25	ns	
$\overline{CAS}$ to QSF delay time	^tCQD		35		35		35	ns	
$\overline{RAS}$ to first SC delay	^tRSD	80		80		80		ns	
$\overline{CAS}$ to first SC delay	^tCSD	30		30		30		ns	

SAM TIMING PARAMETERS

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

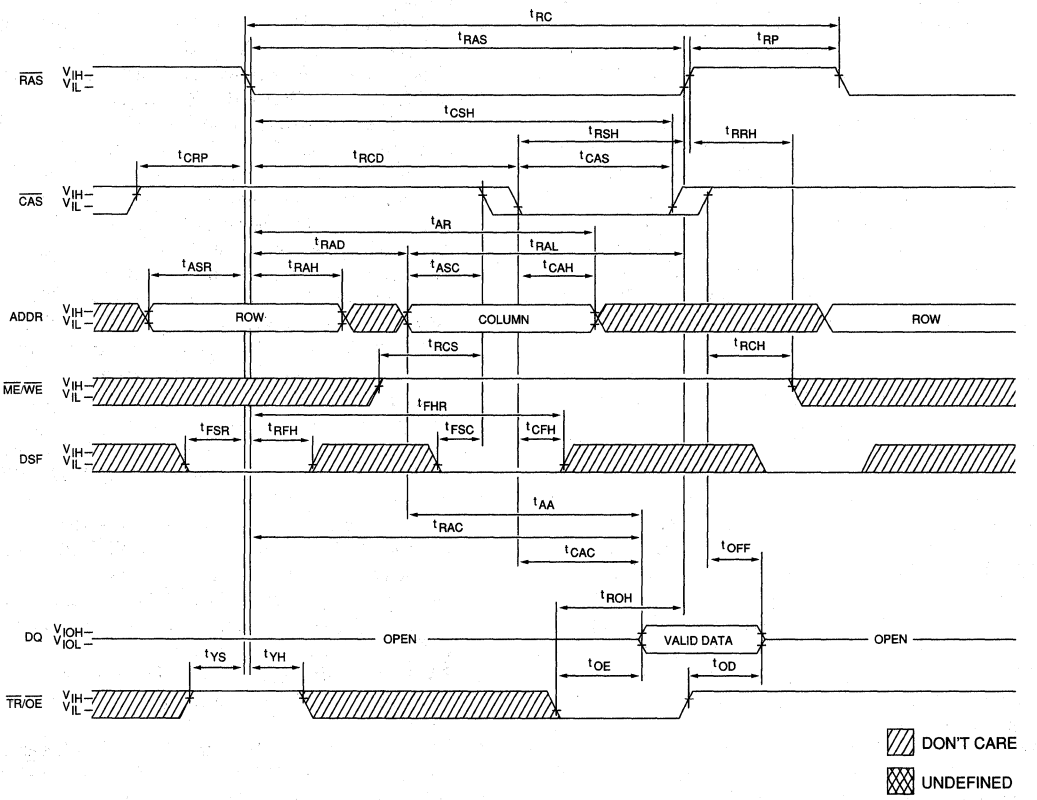
(Notes 6, 7, 8, 9, 10) (0° C ≤ T_A ≤ + 70°C; Vcc = 5V ±10%)

AC CHARACTERISTICS		-7		-8		-10			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Serial clock-cycle time	^tSC	25		30		30		ns	
Access time from SC	^tSAC		22		25		27	ns	24, 28
SC precharge time (SC LOW time)	^tSP	8		10		10		ns	
SC pulse width (SC HIGH time)	^tSAS	8		10		10		ns	
Access time from $\overline{SE}$	^tSEA		15		15		15	ns	24
$\overline{SE}$ precharge time	^tSEP	20		20		20		ns	
$\overline{SE}$ pulse width	^tSE	20		20		20		ns	
Serial data-out hold time after SC high	^tSOH	5		5		5		ns	24, 28
Serial output buffer turn-off delay from $\overline{SE}$	^tSEZ	3	12	3	12	3	12	ns	20, 24
Serial data-in setup time	^tSDS	0		0		0		ns	
Serial data-in hold time	^tSDH	10		10		10		ns	
Serial input (Write) Enable setup time	^tSWS	0		0		0		ns	
Serial input (Write) Enable hold time	^tSWH	15		15		15		ns	
Serial input (Write) disable setup time	^tSWIS	0		0		0		ns	
Serial input (Write) disable hold time	^tSWIH	15		15		15		ns	

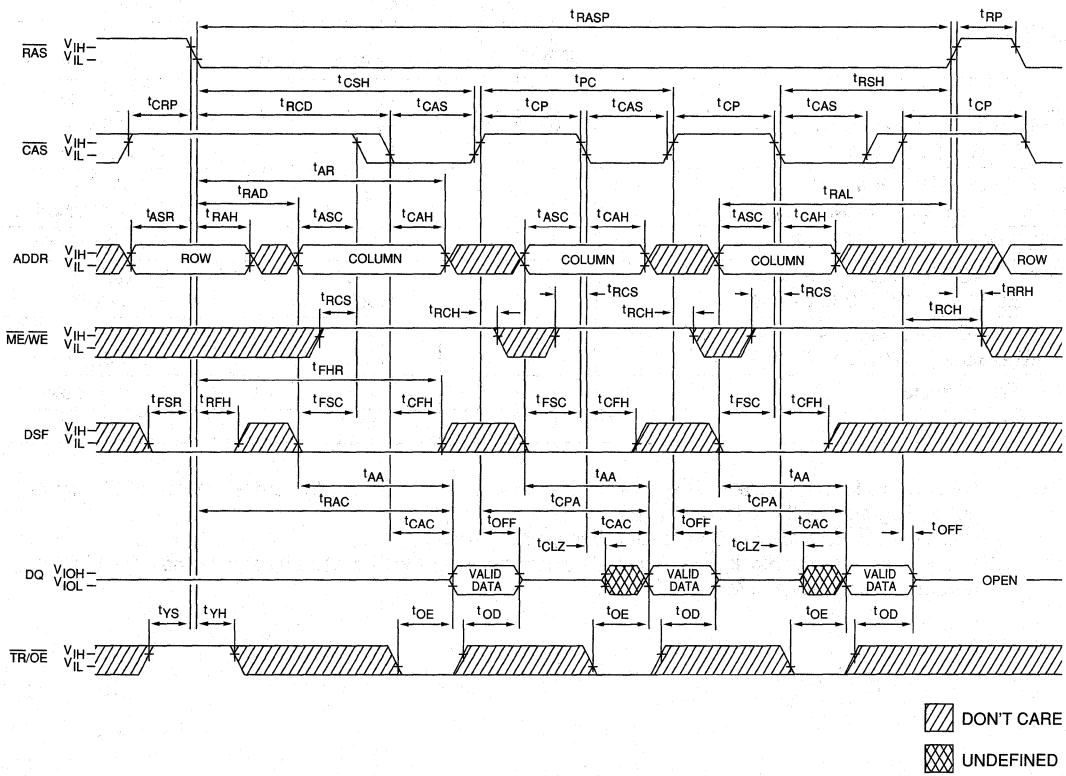
NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. V_{CC} = 5V ±10%, f = 1 MHz.
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on I/O loading. Specified values are obtained with minimum cycle time and the I/Os open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \le T_A \le 70°C$) is assured.
7. An initial pause of 100µs is required after power-up followed by any eight $\overline{RAS}$ cycles before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-up should be repeated any time the ^tREF refresh requirement is exceeded.
8. AC characteristics assume ^tT = 5ns.
9. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}). Input signals transition between 0V and 3V for AC testing.
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS}$ = V_{IH}, DRAM data output (DQ1-DQ4) is High-Z.
12. If $\overline{CAS}$ = V_{IL}, DRAM data output (DQ1-DQ4) may contain data from the last valid READ cycle.
13. DRAM output timing measured with a load equivalent to 2 TTL gates and 100pF. Output reference levels: V_{OH} = 2.0V; V_{OL} = 0.8V.
14. Assumes that $^tRCD < ^tRCD$ (MAX). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
15. Assumes that $^tRCD \ge ^tRCD$ (MIN).
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, DQ will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer, $\overline{CAS}$ must be pulsed HIGH for ^tCPN.
17. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (MAX) limit, then access time is controlled exclusively by ^tCAC.
18. Operation within the ^tRAD (MAX) limit ensures that ^tRCD (MAX) can be met. ^tRAD (MAX) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (MAX) limit, then access time is controlled exclusively by ^tAA.
19. Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
20. ^tOD, ^tOFF and ^tSEZ define the time when the output achieves open circuit (V_{OH} -200mV, V_{OL} +200mV). This parameter is sampled and not 100 percent tested.
21. ^tWCS, ^tRWD, ^tAWD and ^tCWD are restrictive operating parameters in LATE-WRITE, READ-WRITE and READ-MODIFY-WRITE cycles only. If $^tWCS \ge ^tWCS$ (MIN), the cycle is an EARLY-WRITE cycle and the data output will remain an open circuit throughout the entire cycle, regardless of $\overline{TR}/\overline{OE}$. If $^tWCS \le ^tWCS$ (MIN), the cycle is a LATE-WRITE and $\overline{TR}/\overline{OE}$ must control the output buffers during the WRITE to avoid data contention. If $^tRWD \ge ^tRWD$ (MIN), $^tAWD \ge ^tAWD$ (MIN) and $^tCWD \ge ^tCWD$ (MIN), the cycle is a READ-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of the output buffers (at access time and until $\overline{CAS}$ goes back to V_{IH}) is indeterminate but the WRITE will be valid, if ^tOD and ^tOEH are met. See the LATE-WRITE AC Timing diagram.
22. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY-WRITE cycles and $\overline{ME}/\overline{WE}$ leading edge in LATE-WRITE or READ-WRITE cycles.
23. During a READ cycle, if $\overline{TR}/\overline{OE}$ is LOW then taken HIGH, DQ goes open. The DQs will go open with $\overline{OE}$ or $\overline{CAS}$, whichever goes HIGH first.
24. SAM output timing is measured with a load equivalent to 1 TTL gate and 30pF. Output reference levels: V_{OH} = 2.0V; V_{OL} = 0.8V.
25. ^tOD and ^tOEH must be met in LATE-WRITE and READ-MODIFY-WRITE cycles ($\overline{OE}$ HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. The DQs will provide previously read data if $\overline{CAS}$ remains LOW and $\overline{OE}$ is taken LOW after ^tOEH is met. If $\overline{CAS}$ goes HIGH prior to $\overline{OE}$ going back LOW, the DQs will remain open.
26. Address (A0-A8) may be changed two times or less while $\overline{RAS}$ = V_{IL}.
27. Address (A0-A8) may be changed once or less while $\overline{CAS}$ = V_{IH} and $\overline{RAS}$ = V_{IL}.
28. ^tSAC is MAX at 70° C and 4.5V Vcc; ^tSOH is MIN at 0°C and 5.5V Vcc. These limits will not occur simultaneously at any given voltage or temperature. ^tSOH = ^tSAC - output transition time; this is guaranteed by design.
29. Values in parenthesis apply to the "L" version.

DRAM READ CYCLE



DRAM FAST-PAGE-MODE READ CYCLE



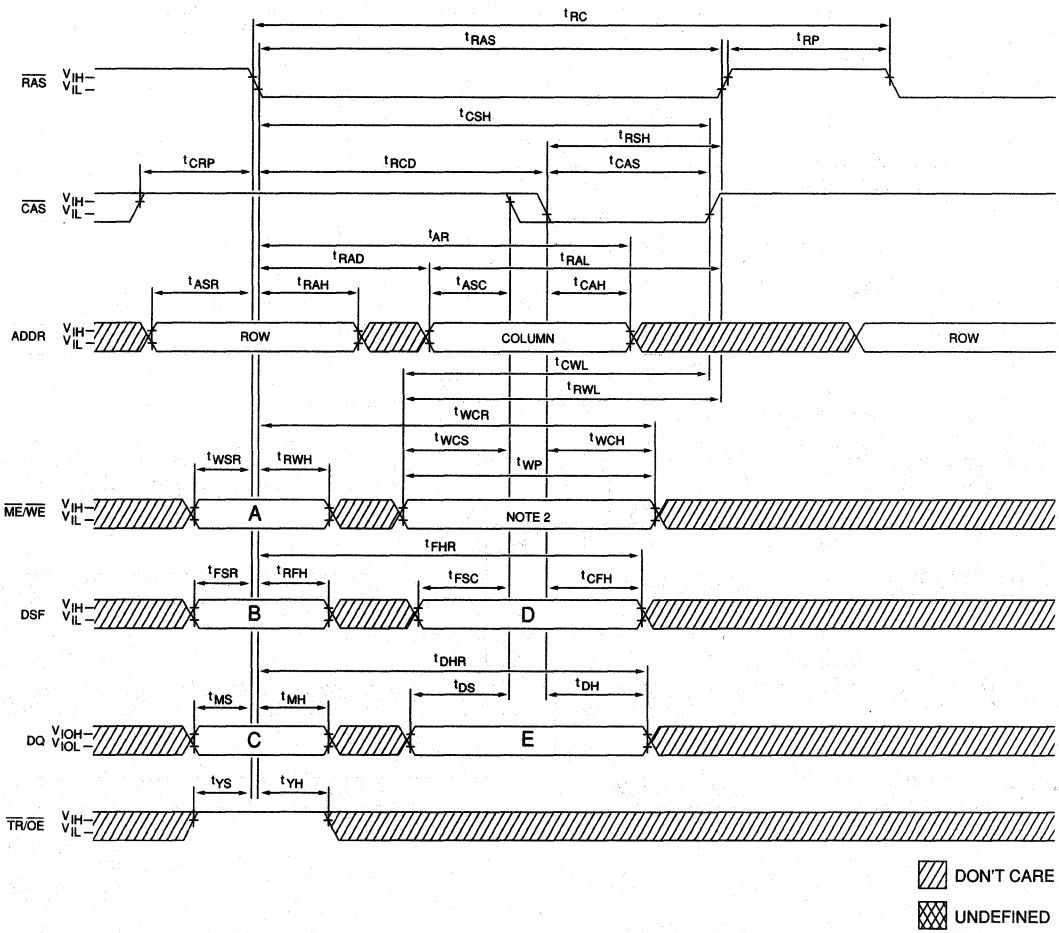
NOTE: WRITE cycles or READ-MODIFY-WRITE cycles may be mixed with READ cycles while in FAST PAGE MODE.

WRITE CYCLE FUNCTION TABLE [1]

FUNCTION	LOGIC STATES				
	$\overline{RAS}$ Falling Edge			$\overline{CAS}$ Falling Edge	
	A $\overline{ME}/\overline{WE}$	B DSF	C DQ (Input)	D DSF	E[2] DQ (Input)
Normal DRAM WRITE	1	0	X	0	DRAM Data
NONPERSISTENT (Load and Use) MASKED WRITE to DRAM	0	0	Write Mask	0	DRAM Data (Masked)
PERSISTENT (Use Register) MASKED WRITE to DRAM	0	1	X	0	DRAM Data (Masked)
BLOCK WRITE to DRAM (No Data Mask)	1	0	X	1	Column Mask[3]
NONPERSISTENT (Load and Use) MASKED BLOCK WRITE to DRAM	0	0	Write Mask	1	Column Mask[3]
PERSISTENT (Use Register) MASKED BLOCK WRITE to DRAM	0	1	X	1	Column Mask[3]
Load Mask Register	1	1	X	0	Write Mask
Load Color Register	1	1	X	1	Color Data

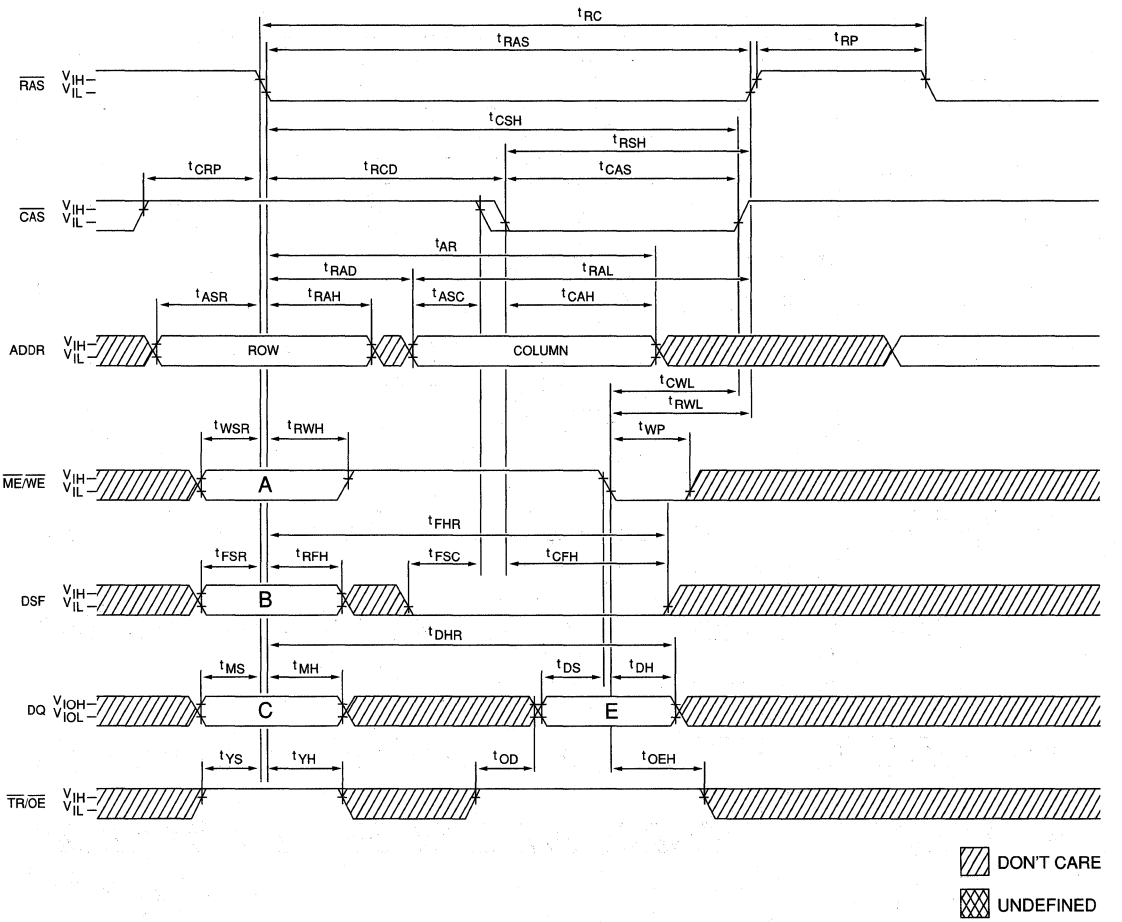
NOTE:
1. Refer to this function table to determine the logic states of "A", "B", "C", "D" and "E" for the WRITE cycle timing diagrams on the following pages.
2. $\overline{CAS}$ or $\overline{ME}/\overline{WE}$, whichever occurs later (Except Block Write).
3. $\overline{WE}$ = "don't care" for Block Write. The DQ column-mask data will be latched at the falling edge of $\overline{CAS}$, regardless of the state of $\overline{ME}/\overline{WE}$.

DRAM EARLY-WRITE CYCLE [1]



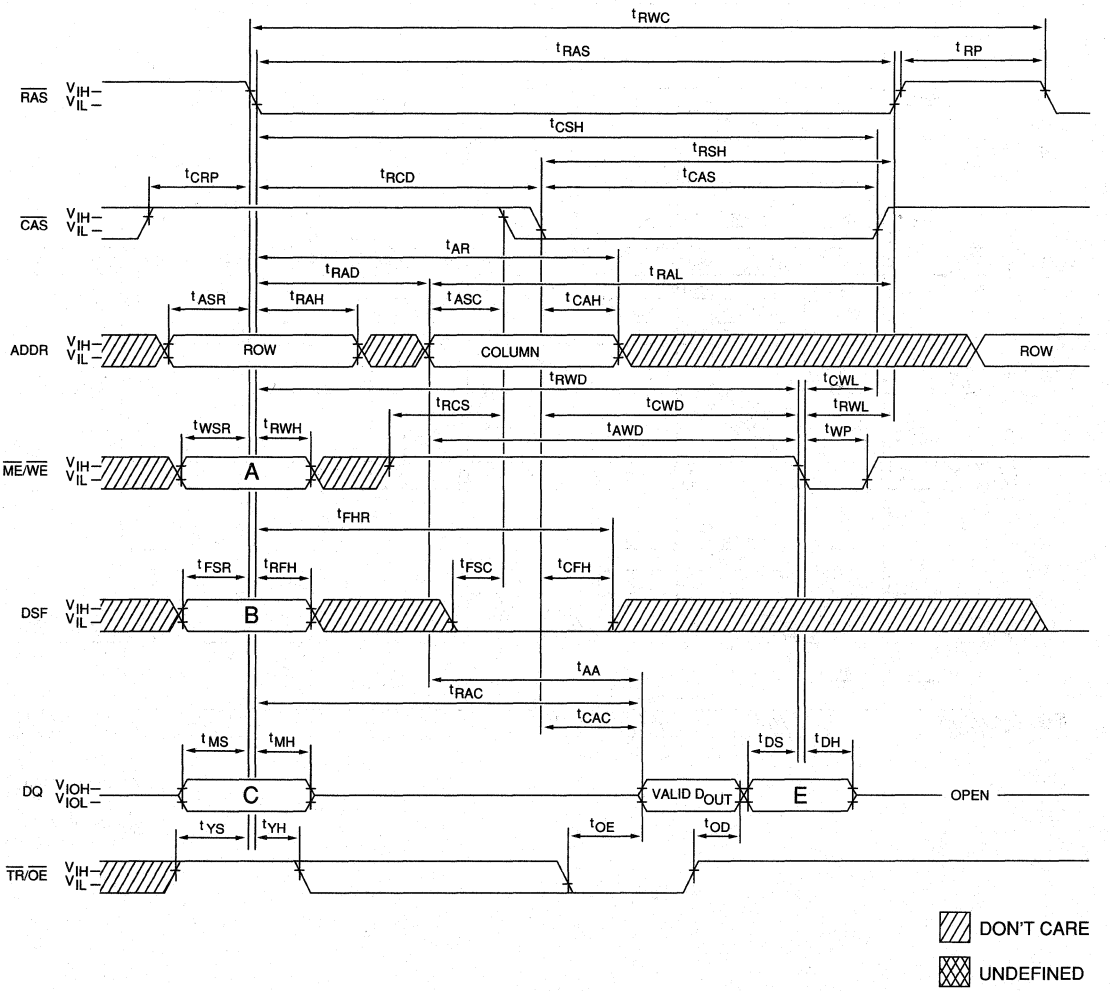
NOTE: 1. The logic states of "A", "B", "C", "D" and "E" determine the type of WRITE operation performed. See the Write Cycle Function Table for a detailed description.
2. For Block Write, $\overline{ME}/\overline{WE}$ = "don't care." For all other EARLY-WRITE cycles, $\overline{ME}/\overline{WE}$ = LOW.

DRAM LATE-WRITE CYCLE [1]



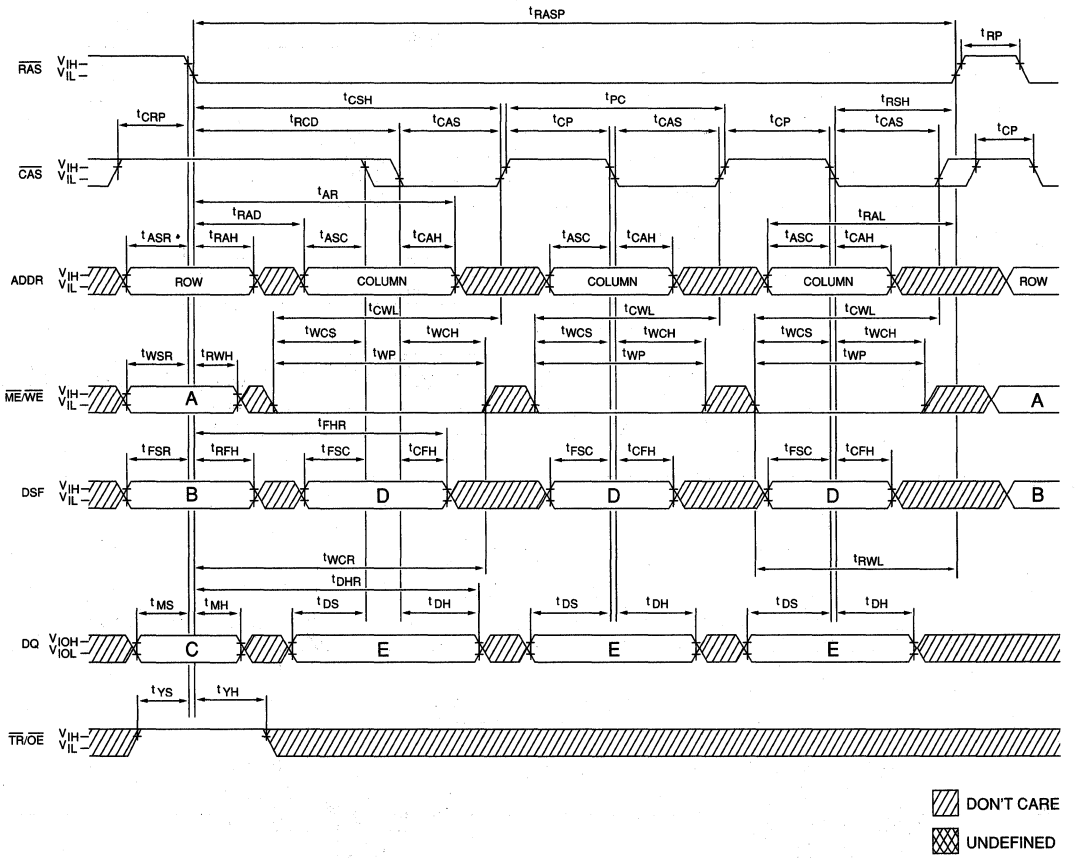
NOTE: 1. The logic states of "A", "B", "C" and "E" determine the type of WRITE operation performed. See the Write Cycle Function Table for a detailed description.

DRAM READ-WRITE CYCLE
(READ-MODIFY-WRITE CYCLE)



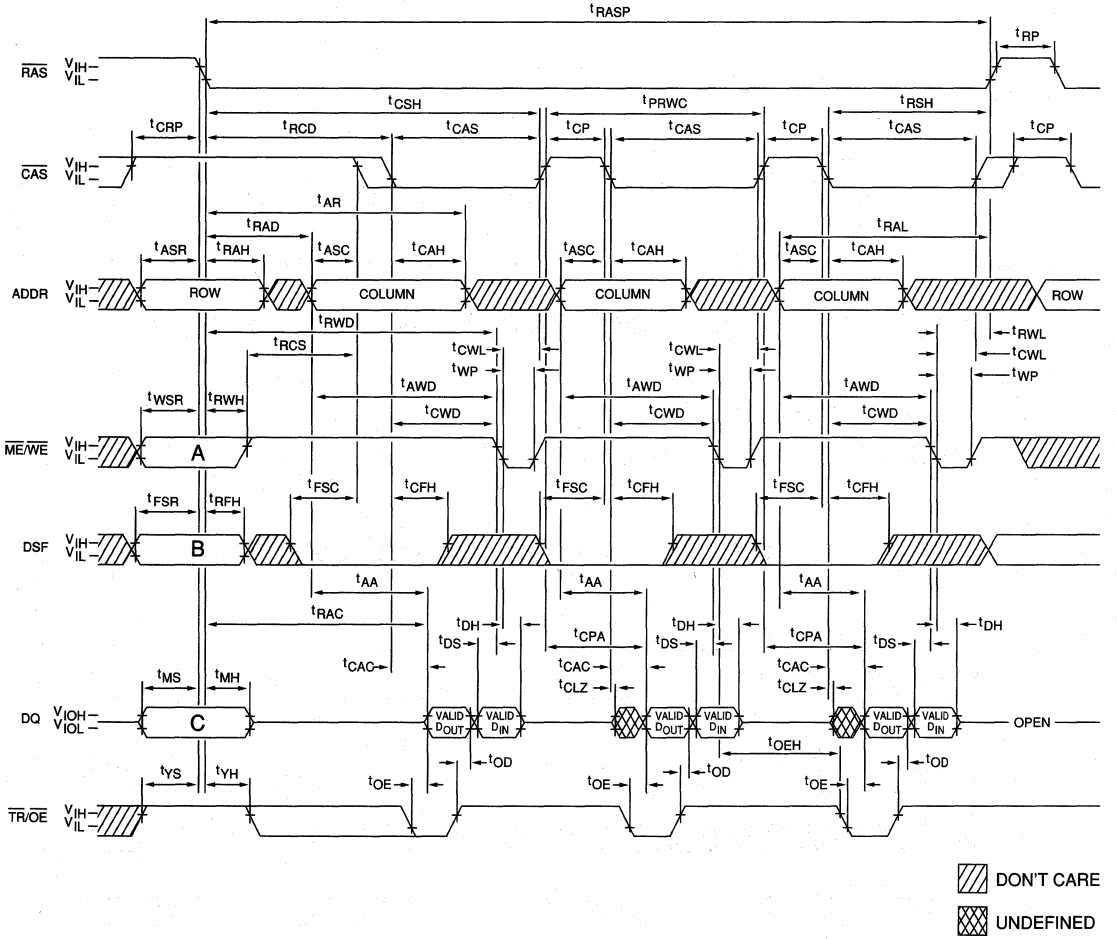
NOTE: The logic states of "A", "B", "C" and "E" determine the type of WRITE operation performed. See the Write Cycle Function Table for a detailed description.

DRAM FAST-PAGE-MODE EARLY-WRITE CYCLE



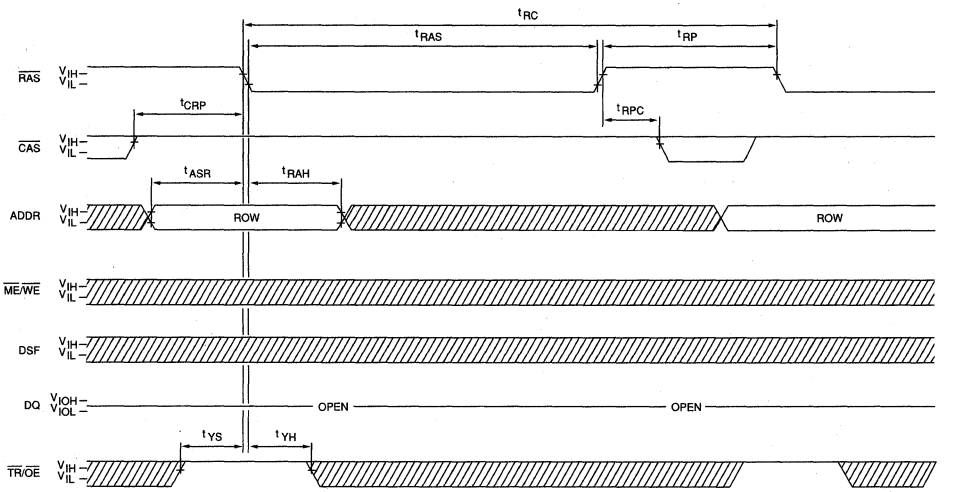
NOTE:
1. READ cycles or READ-MODIFY-WRITE cycles can be mixed with WRITE cycles while in FAST PAGE MODE.
2. The logic states of "A", "B", "C", "D" and "E" determine the type of WRITE operation performed. See the Write Cycle Function Table for a detailed description.

DRAM FAST-PAGE-MODE READ-WRITE CYCLE
(READ-MODIFY-WRITE OR LATE-WRITE CYCLES)

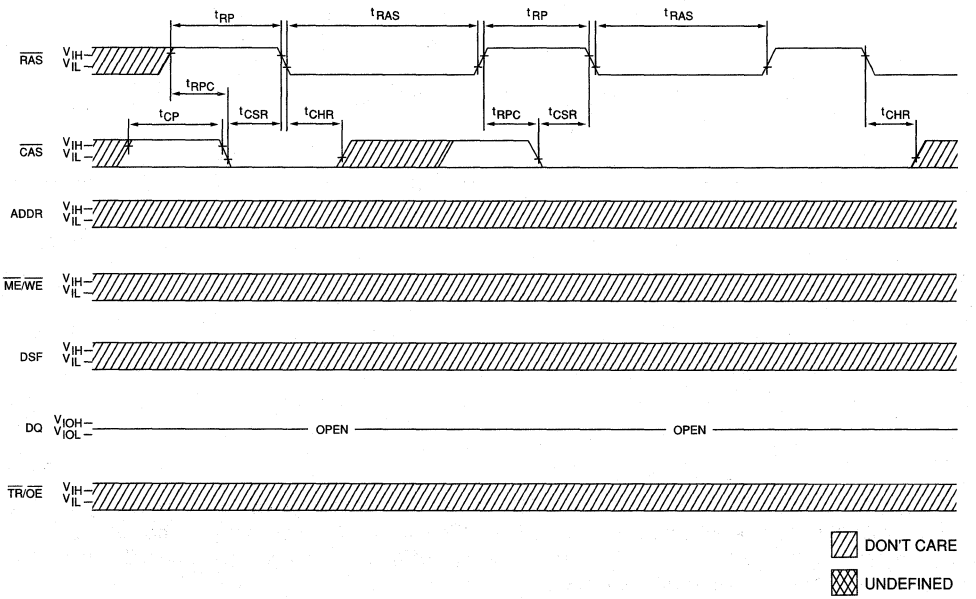


NOTE:
1. READ or WRITE cycles can be mixed with READ-MODIFY-WRITE cycles while in FAST PAGE MODE. Use the Write Function Table to determine the proper DSF state for the desired WRITE operation.
2. The logic states of "A", "B" and "C" determine the type of WRITE operation performed. See the Write Cycle Function Table for a detailed description.

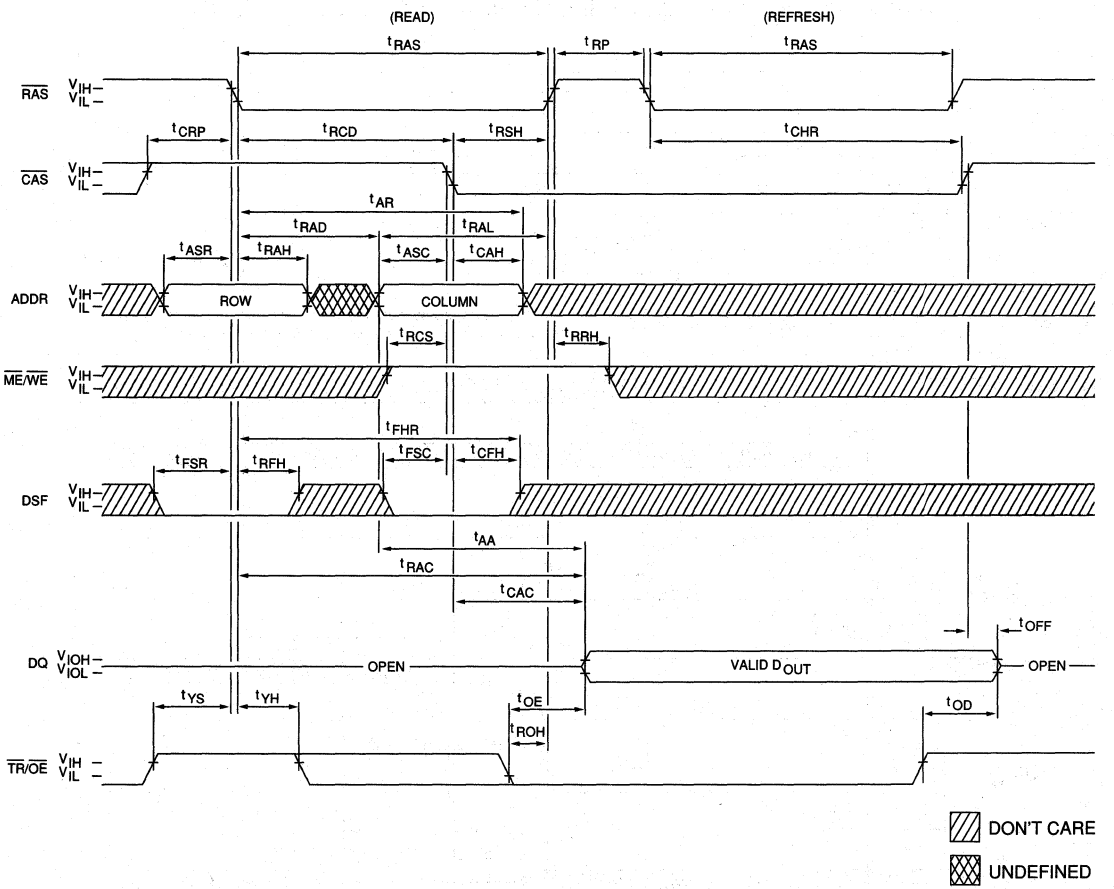
DRAM $\overline{RAS}$-ONLY REFRESH CYCLE
(ADDR = A0-A8)



DRAM $\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

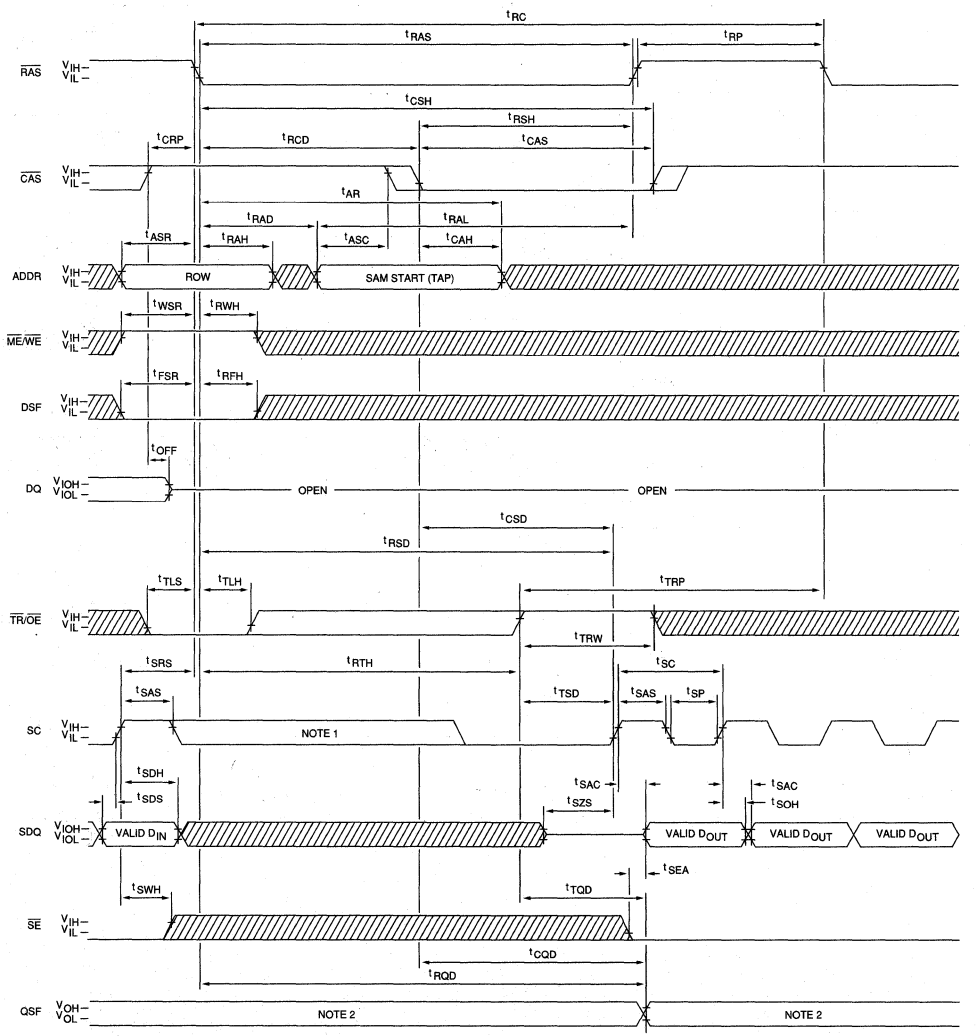


DRAM HIDDEN-REFRESH CYCLE



NOTE: A HIDDEN REFRESH may also be performed after a WRITE or TRANSFER cycle. In the WRITE case, $\overline{ME}/\overline{WE}$ = LOW (when $\overline{CAS}$ goes LOW) and $\overline{TR}/\overline{OE}$ = HIGH and the DQ pins stay High-Z. In the TRANSFER case, $\overline{TR}/\overline{OE}$ = LOW (when $\overline{RAS}$ goes LOW) and the DQ pins stay High-Z during the refresh period, regardless of $\overline{TR}/\overline{OE}$.

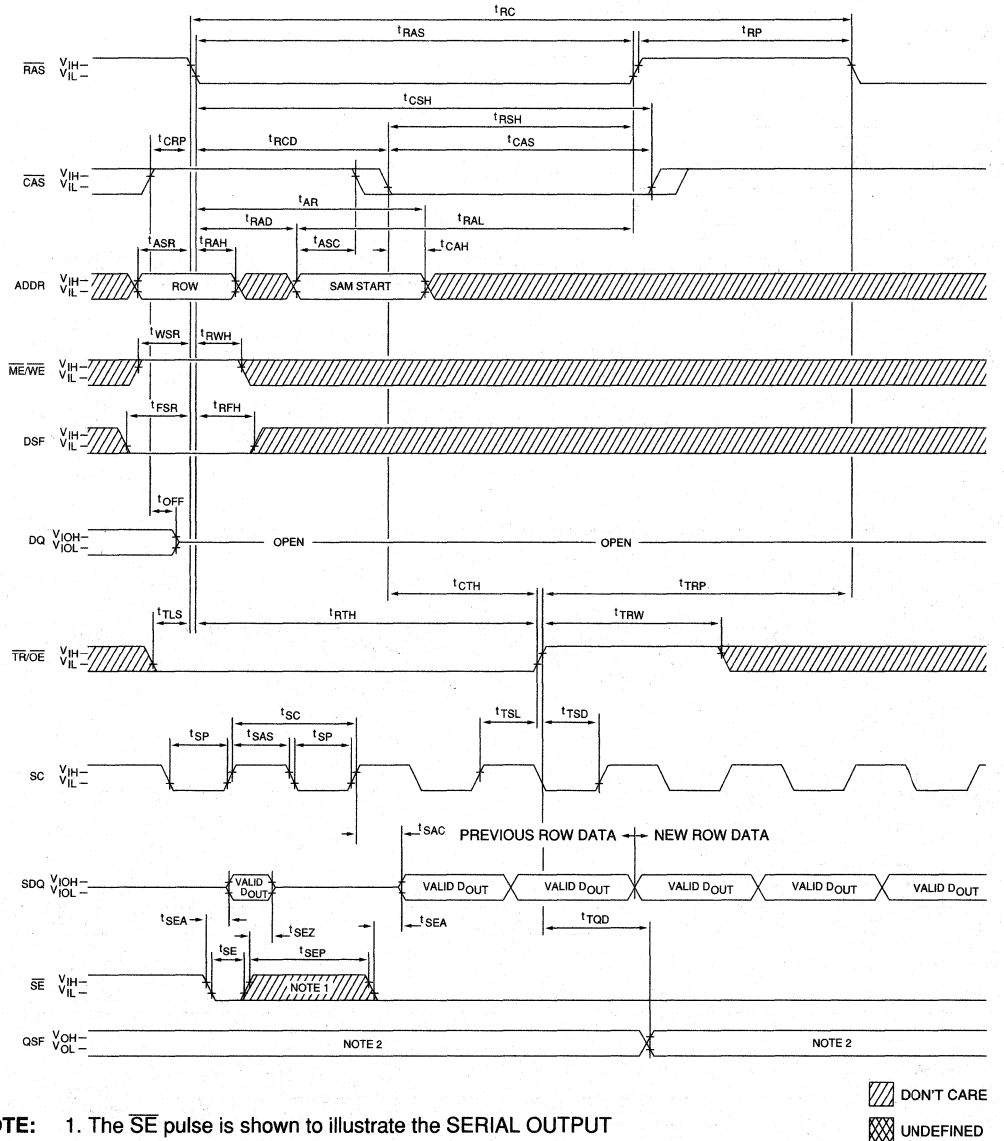
READ TRANSFER [3]
(DRAM-TO-SAM TRANSFER)
(When part was previously in the SERIAL INPUT mode or SC idle)



NOTE:
1. There must be no rising edges on the SC input during this time period.
2. QSF = 0 when the Lower SAM (bits 0–255) is being accessed.
   QSF = 1 when the Upper SAM (bits 256–511) is being accessed.
3. If ^{t}TLH is timing for the $\overline{TR}/(\overline{OE})$ rising edge, the transfer is self-timed and the ^{t}CSD and ^{t}RSD times must be met. If ^{t}RTH is timing for the $\overline{TR}/(\overline{OE})$ rising edge, the transfer is done off of the $\overline{TR}/(\overline{OE})$ rising edge and ^{t}TSD must be met.

REAL-TIME READ-TRANSFER (DRAM-TO-SAM TRANSFER)

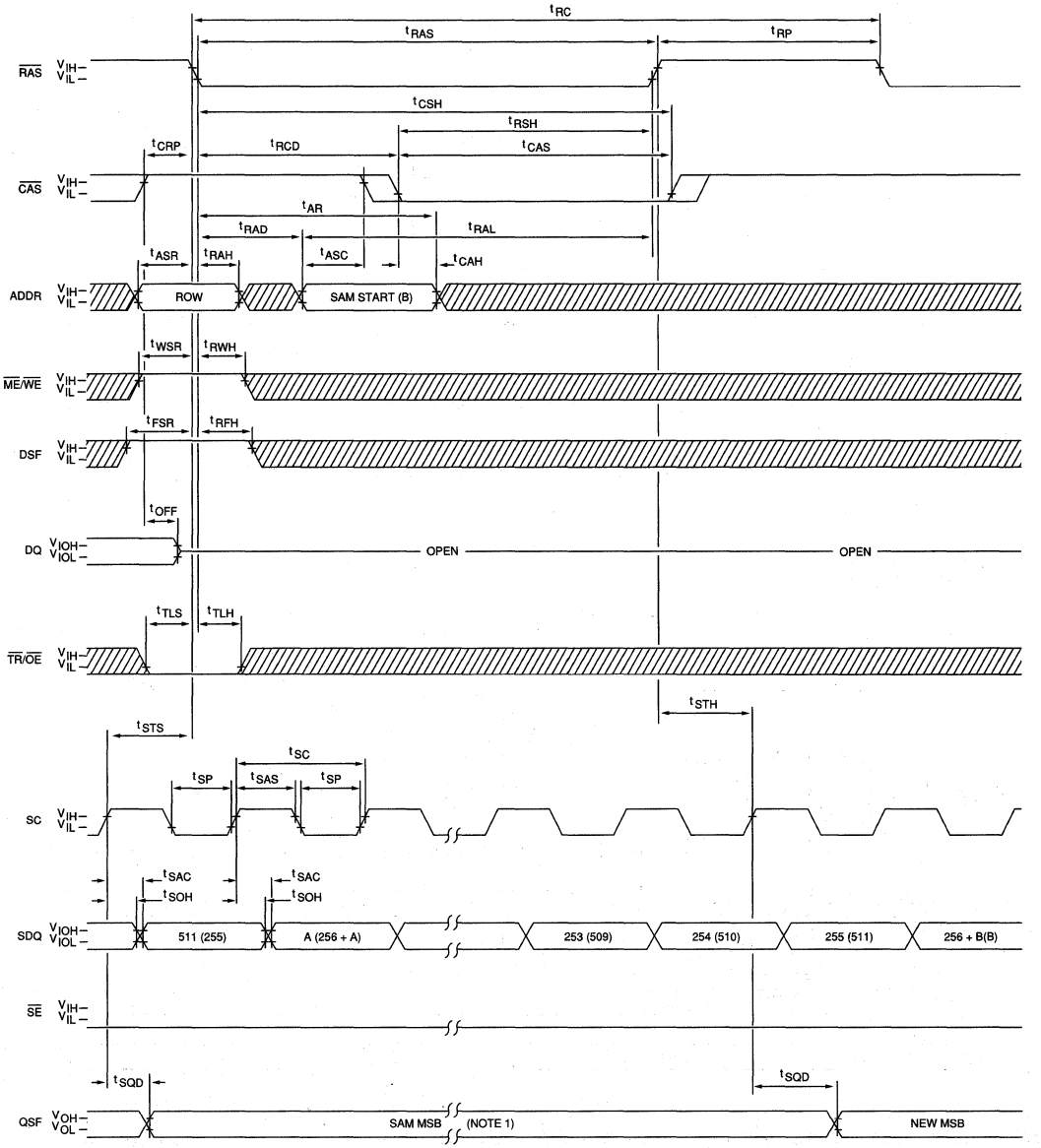
(When part was previously in the SERIAL OUTPUT mode)



NOTE: 1. The $\overline{SE}$ pulse is shown to illustrate the SERIAL OUTPUT ENABLE and DISABLE timing. It is not required.
2. QSF = 0 when the Lower SAM (bits 0–255) is being accessed.
QSF = 1 when the Upper SAM (bits 256–511) is being accessed.

MULTIPORT DRAM

SPLIT READ TRANSFER
(SPLIT DRAM-TO-SAM TRANSFER)

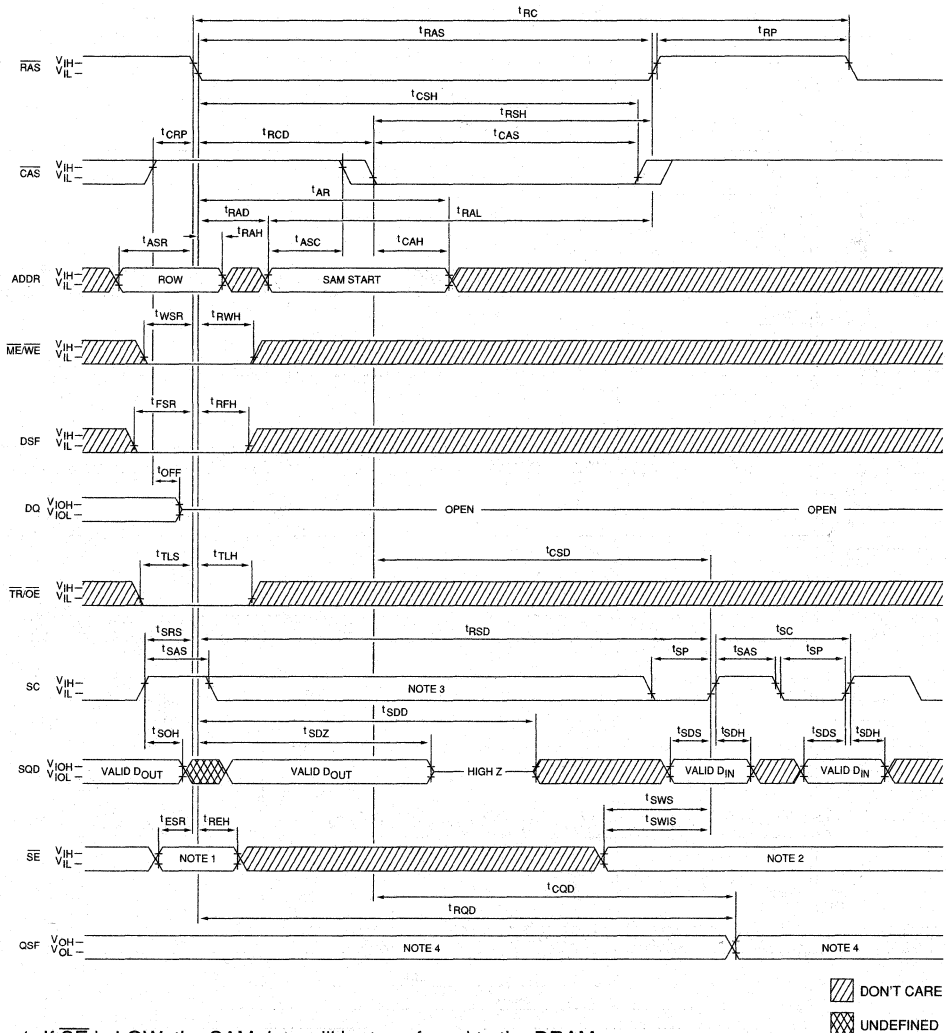


NOTE: 1. QSF = 0 when the Lower SAM (bits 0–255) is being accessed.
QSF = 1 when the Upper SAM (bits 256–511) is being accessed.

DON'T CARE
UNDEFINED

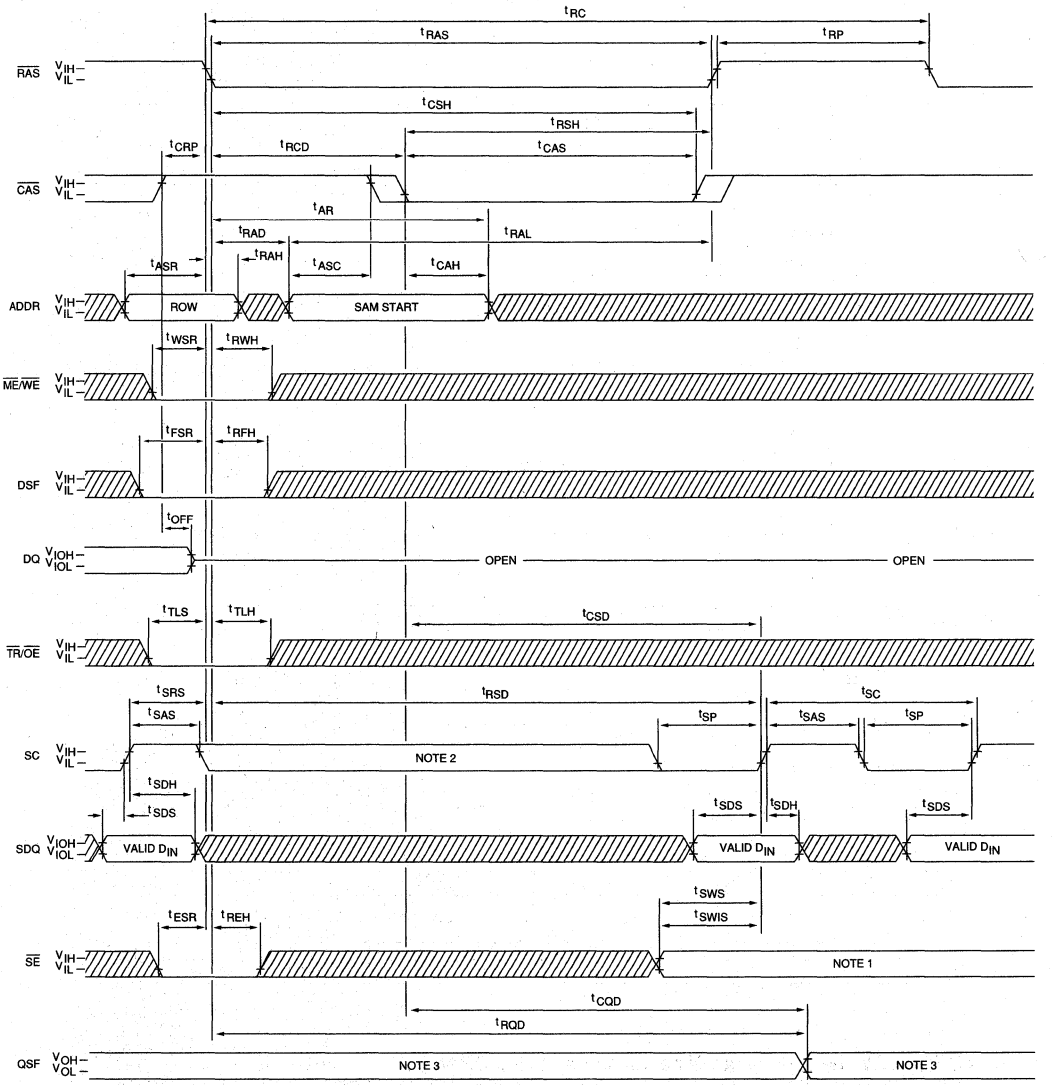
WRITE TRANSFER and PSEUDO WRITE TRANSFER (SAM-TO-DRAM TRANSFER)

(When part was previously in the SERIAL OUTPUT mode)



NOTE:
1. If $\overline{SE}$ is LOW, the SAM data will be transferred to the DRAM.
   If $\overline{SE}$ is HIGH, the SAM data will not be transferred to the DRAM (SERIAL-INPUT-MODE ENABLE cycle).
2. $\overline{SE}$ must be LOW to input new serial data, but the serial address register is incremented by SC regardless of $\overline{SE}$.
3. There must be no rising edges on the SC input during this time period.
4. QSF = 0 when the Lower SAM (bits 0–255) is being accessed.
   QSF = 1 when the Upper SAM (bits 256–511) is being accessed.

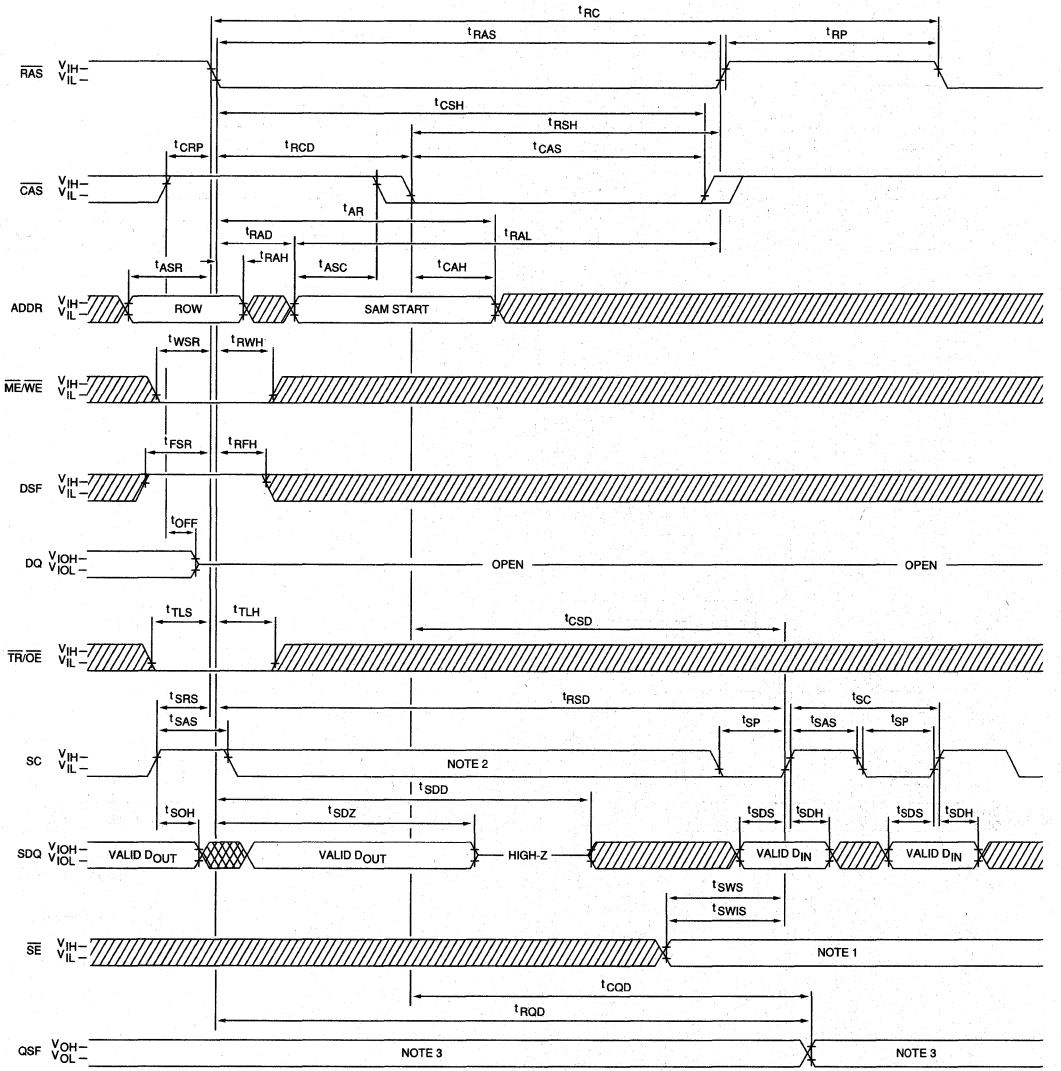
WRITE TRANSFER
(SAM-TO-DRAM TRANSFER)
(When part was previously in the SERIAL INPUT mode)



NOTE:
1. $\overline{SE}$ must be LOW to input new serial data, but the serial address register is incremented by SC regardless of $\overline{SE}$.
2. There must be no rising edges on the SC input during this time period.
3. QSF = 0 when the Lower SAM (bits 0–255) is being accessed.
   QSF = 1 when the Upper SAM (bits 256–511) is being accessed.

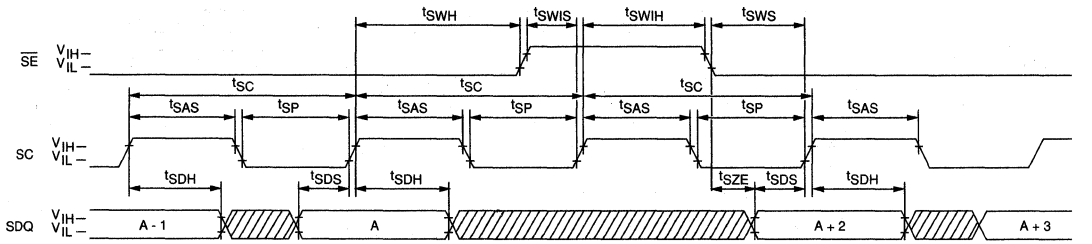
DON'T CARE
UNDEFINED

ALTERNATE WRITE TRANSFER (SAM-TO-DRAM TRANSFER)

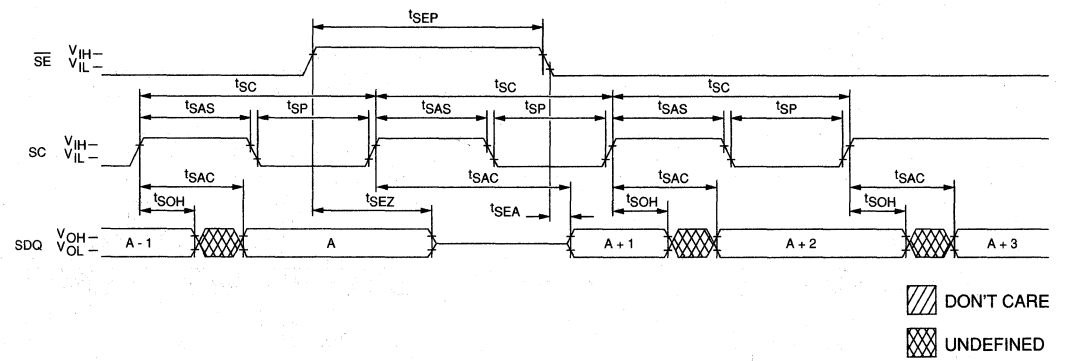


NOTE:
1. $\overline{SE}$ must be LOW to input new serial data, but the serial address register is incremented by SC regardless of $\overline{SE}$.
2. There must be no rising edges on the SC input during this time period.
3. QSF = 0 when the Lower SAM (bits 0–255) is being accessed.
   QSF = 1 when the Upper SAM (bits 256–511) is being accessed.

SAM SERIAL INPUT



SAM SERIAL OUTPUT



VRAM

128K x 8 DRAM WITH 256 x 8 SAM

FEATURES

- Industry standard pinout, timing and functions
- High-performance, CMOS silicon-gate process
- Single +5V ±10% (-10), +5V ±5% (-8S) power supply
- Inputs and outputs are fully TTL compatible
- Refresh modes: $\overline{\text{RAS}}$-ONLY, $\overline{\text{CAS}}$-BEFORE-$\overline{\text{RAS}}$ (CBR) and HIDDEN
- 512-cycle refresh within 8ms
- Optional FAST PAGE MODE access cycles
- Dual port organization: 128K x 8 DRAM port
  256 x 8 SAM port
- No refresh required for serial access memory
- Low power: 15mW standby; 275mW active, typical
- Fast access times – 80ns random, 25ns serial

SPECIAL FUNCTIONS

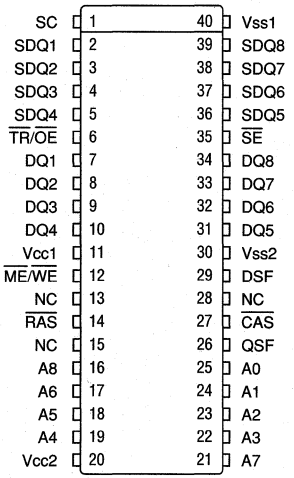
- JEDEC Standard Function set
- PERSISTENT MASKED WRITE
- SPLIT READ TRANSFER
- WRITE TRANSFER/SERIAL INPUT
- ALTERNATE WRITE TRANSFER

OPTIONS MARKING

- Timing [DRAM, SAM (cycle/access)]
  80ns, 25ns/25ns -8S
  100ns, 30ns/30ns -10
- Packages
  Plastic SOJ (400 mil) DJ

PIN ASSIGNMENT (Top View)

40-Pin SOJ
(Q-6)



GENERAL DESCRIPTION

The MT42C8127 is a high speed, dual port CMOS dynamic random access memory, or video RAM (VRAM) containing 1,048,576 bits. These bits may be accessed either by an 8-bit wide DRAM port or by a 256 x 8-bit serial access memory (SAM) port. Data may be transferred bidirectionally between the DRAM and the SAM.

The DRAM portion of the VRAM is functionally identical to the MT4C4256 (256K x 4-bit DRAM). Eight 256-bit data registers make up the serial access memory portion of the VRAM. Data I/O and internal data transfer are accomplished using three separate bidirectional data paths: the 8-bit random access I/O port, the eight internal 256 bit wide paths between the DRAM and the SAM, and the 8-bit serial I/O port for the SAM. The rest of the circuitry consists of the control, timing, and address decoding logic.

Each port may be operated asynchronously and independently of the other except when data is being transferred internally between them. As with all DRAMs, the VRAM must be refreshed to maintain data. The refresh cycles must be timed so that all 512 combinations of $\overline{\text{RAS}}$ addresses are executed at least every 8ms (regardless of sequence). Micron recommends evenly spaced refresh cycles for maximum data integrity. An internal transfer between the DRAM and the SAM counts as a refresh cycle. The SAM portion of the VRAM is fully static and does not require any refresh.

The operation and control of the MT42C8127 are optimized for high performance graphics and communication designs. The dual port architecture is well suited to buffering the sequential data types used in rastor graphics display, serial and parallel networking and data communications. Special features, such as SPLIT READ TRANSFER, allow further enhancements to system performance.

VRAM

128K x 8 DRAM WITH 256 x 8 SAM

FEATURES

- Industry standard pinout, timing and functions
- High-performance, CMOS silicon-gate process
- Single +5V ±10% power supply
- Low power: 15mW standby; 275mW active, typical
- Inputs and outputs are fully TTL compatible
- Refresh modes: RAS-ONLY, CAS-BEFORE-RAS (CBR) and HIDDEN
- 512-cycle refresh within 8ms
- No refresh required for serial access memory
- Optional FAST PAGE MODE access cycles
- Dual port organization: 128K x 8 DRAM port
  256 x 8 SAM port
- Fast access times – 70ns random, 22ns serial

SPECIAL FUNCTIONS

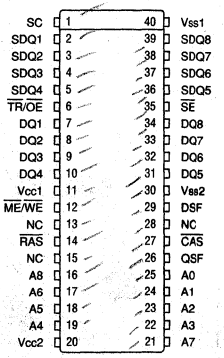
- JEDEC Standard Function set
- PERSISTENT MASKED WRITE
- SPLIT READ TRANSFER
- WRITE TRANSFER/SERIAL INPUT
- ALTERNATE WRITE TRANSFER
- BLOCK WRITE

OPTIONS MARKING

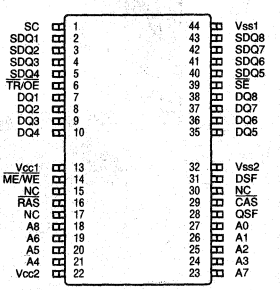
- Timing [DRAM, SAM (cycle/access)]
  - 70ns, 25ns/22ns - 7
  - 80ns, 30ns/25ns - 8
  - 100ns, 30ns/27ns -10
- Packages
  - Plastic SOJ (400 mil) DJ
  - Plastic TSOP (400 mil) TG
- 32ms low power/extended refresh L

PIN ASSIGNMENT (Top View)

40-Pin SOJ
(Q-6)



40/44-Pin TSOP*
(R-5)



*Consult factory on TSOP availability.

GENERAL DESCRIPTION

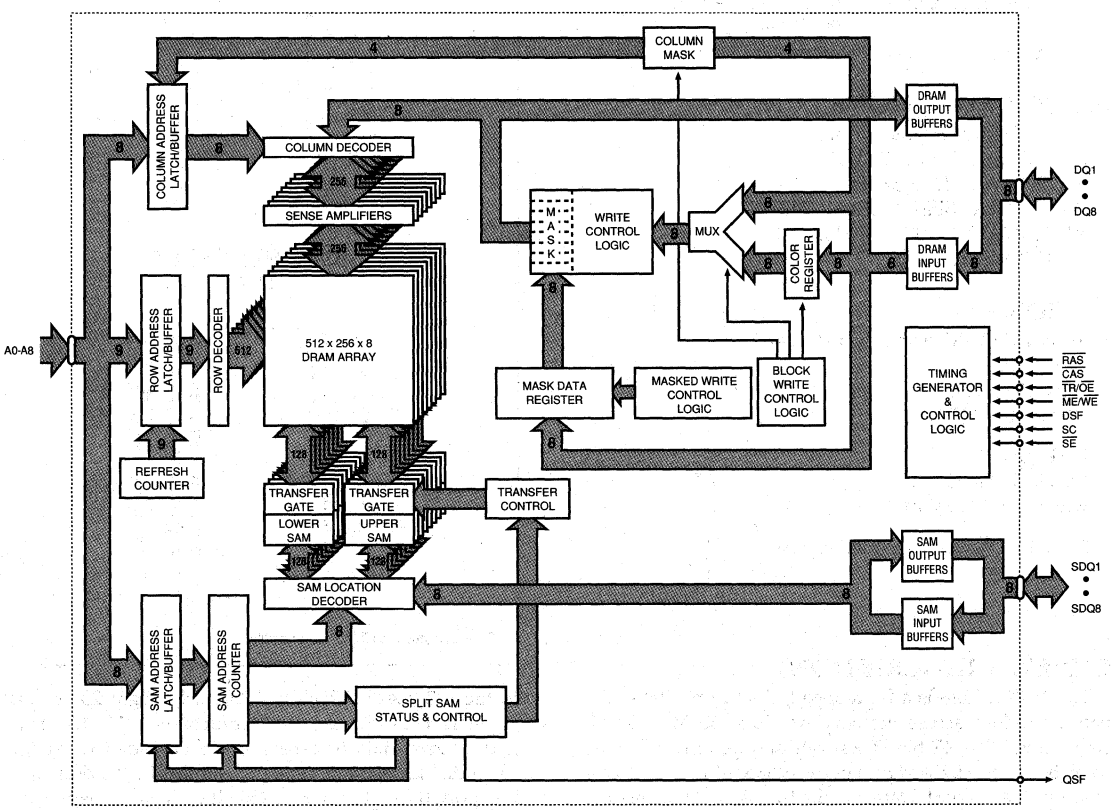
The MT42C8128 is a high-speed, dual port CMOS dynamic random access memory or video RAM (VRAM) containing 1,048,576 bits. These bits may be accessed either by an 8-bit wide DRAM port or by a 256 x 8-bit serial access memory (SAM) port. Data may be transferred bidirectionally between the DRAM and the SAM. An extended refresh (32ms), low power option is available as the MT42C8128 L.

The DRAM portion of the VRAM is functionally identical to the MT4C4256 (256K x 4 DRAM). Eight 256-bit data registers make up the SAM portion of the VRAM. Data I/O and internal data transfer are accomplished using three separate bidirectional data paths: the 8-bit random access I/O port, the eight internal 256 bit wide paths between the DRAM and the SAM, and the 8-bit serial I/O port for the SAM. The rest of the circuitry consists of the control, timing and address decoding logic.

Each port may be operated asynchronously and independently of the other except when data is being transferred internally between them. As with all DRAMs, the VRAM must be refreshed to maintain data. The refresh cycles must be timed so that all 512 combinations of $\overline{RAS}$ addresses are executed at least every 8ms, or 32ms for the MT42C8128 L, (regardless of sequence). Micron recommends evenly spaced refresh cycles for maximum data integrity. An internal transfer between the DRAM and SAM counts as a refresh cycle. The SAM portion of the VRAM is fully static and requires no refresh.

The operation and control of the MT42C8128 is optimized for high performance graphics and communication designs. The dual port architecture is well suited to buffering the sequential data used in raster graphics display, serial/parallel networking and data communications. Special features such as SPLIT READ TRANSFER and BLOCK WRITE, allow further enhancements to system performance.

FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTIONS

SOJ PIN NUMBERS	TSOP PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
1	1	SC	Input	Serial Clock: Clock input to the serial address counter for the SAM registers.
6	6	$\overline{TR/OE}$	Input	Transfer Enable: Enables an internal TRANSFER operation at $\overline{RAS}$ (H → L), or Output Enable: Enables the DRAM output buffers when taken LOW after $\overline{RAS}$ goes LOW ($\overline{CAS}$ must also be LOW), otherwise the output buffers are in a High-Z state.
12	14	$\overline{ME/WE}$	Input	Mask Enable: If $\overline{ME/WE}$ is LOW at the falling edge of $\overline{RAS}$, a MASKED WRITE cycle is performed, or Write Enable: $\overline{ME/WE}$ is also used to select a READ ($\overline{ME/WE}$ = H) or WRITE ($\overline{ME/WE}$ = L) cycle when accessing the DRAM. This includes a READ TRANSFER ($\overline{ME/WE}$ = H) or WRITE TRANSFER ($\overline{ME/WE}$ = L).
35	39	$\overline{SE}$	Input	Serial Port Enable: $\overline{SE}$ enables the serial I/O buffers and allows a serial READ or WRITE operation to occur, otherwise the output buffers are in a High-Z state. $\overline{SE}$ is also used during a WRITE TRANSFER operation to indicate whether a WRITE TRANSFER or a SERIAL INPUT MODE ENABLE cycle is performed.
29	31	DSF	Input	Special Function Select: DSF is used to indicate which special functions (BLOCK WRITE, MASKED WRITE vs. PERSISTENT MASKED WRITE, etc.) are used for a particular access cycle.
14	16	$\overline{RAS}$	Input	Row Address Strobe: $\overline{RAS}$ is used to clock in the 9 row-address bits and strobe the $\overline{ME/WE}$, $\overline{TR/OE}$, DSF, $\overline{SE}$, $\overline{CAS}$ and DQ inputs. It acts as master chip enable, and must fall to initiate any DRAM or TRANSFER cycle
27	29	$\overline{CAS}$	Input	Column Address Strobe: $\overline{CAS}$ is used to clock-in the 8 column-address bits, enable the DRAM output buffers (along with $\overline{TR/OE}$), and strobe the DSF input.
25, 24, 23, 22, 19, 18, 17, 21, 16	27, 26, 25, 24, 21, 20, 19, 23, 18	A0-A8	Input	Address Inputs: For the DRAM operation, these inputs are multiplexed and clocked by $\overline{RAS}$ and $\overline{CAS}$ to select one 8-bit word out of the 128K available. During TRANSFER operations, A0 to A8 indicate the DRAM row being accessed (when $\overline{RAS}$ goes LOW) and A0-A7 indicate the SAM start address (when $\overline{CAS}$ goes LOW). A7, A8 = "don't care" for the start address when during SPLIT TRANSFER.

PIN DESCRIPTIONS (continued)

SOJ PIN NUMBERS	TSOP PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
7, 8, 9, 10, 31, 32, 33, 34	7, 8, 9, 10, 35, 36, 37, 38	DQ1-DQ8	Input/ Output	DRAM Data I/O: Data input/output for DRAM cycles; inputs for Mask Data Register and Color Register load cycles, and DQ and Column Mask inputs for BLOCK WRITE.
2, 3, 4, 5, 36, 37, 38, 39	2, 3, 4, 5, 40, 41, 42, 43	SDQ1-SDQ8	Input/ Output	Serial Data I/O: Input, output, or High-Z.
26	28	QSF	Output	Split SAM Status: QSF indicates which half of the SAM is being accessed. LOW if address is 0-127, HIGH if address is 128-255.
15, 28	17, 30	NC	–	No Connect: This pin should be either left unconnected or tied to ground.
11, 20	13, 22	Vcc	Supply	Power Supply: +5V ±10%
30, 40	32, 44	Vss	Supply	Ground

FUNCTIONAL DESCRIPTION

The MT42C8128 may be divided into three functional blocks: the DRAM, the transfer circuitry, and the SAM. All of the operations described below are shown in the AC Timing Diagrams section of this data sheet and summarized in the Truth Table.

Note: *For dual-function pins, the function that is not being discussed will be surrounded by parentheses. For example, the TR/OE pin will be shown as TR/(OE) in references to transfer operations.*

DRAM OPERATION

DRAM REFRESH

Like any DRAM-based memory, the MT42C8128 VRAM must be refreshed to retain data. All 512 row address combinations must be accessed within 8ms. The MT42C8128 supports CAS-BEFORE-RAS, RAS-ONLY and HIDDEN types of refresh cycles.

For the CAS-BEFORE-RAS REFRESH cycle, the row addresses are generated and stored in an internal address counter. The user need not supply any address data, and simply must perform 512 CAS-BEFORE-RAS cycles within the 8ms time period.

The refresh address must be generated externally and applied to A0-A8 inputs for RAS-ONLY REFRESH cycles. The DQ pins remain in a High-Z state for both the RAS-ONLY and CAS-BEFORE-RAS cycles.

HIDDEN REFRESH cycles are performed by toggling RAS (and keeping CAS LOW) after a READ or WRITE cycle. This performs CAS-BEFORE-RAS cycles but does not disturb the DQ lines.

Any DRAM READ, WRITE, or TRANSFER cycle also refreshes the DRAM row that is being accessed. The SAM portion of the MT42C8128 is fully static and does not require any refreshing.

DRAM READ AND WRITE CYCLES

The DRAM portion of the VRAM is nearly identical to standard 256K x 4 DRAMs. However, because several of the DRAM control pins are used for additional functions on this part, several conditions that were undefined or in "don't care" states for the DRAM are specified for the VRAM. These conditions are highlighted in the following discussion. In addition, the VRAM has several special functions that can be used when writing to the DRAM.

The 17 address bits used to select an 8-bit word from the 131,072 available are latched into the chip using the A0-A8, RAS and CAS inputs. First, the 9 row-address bits are set up on the address inputs and clocked into the part when RAS transitions from HIGH-to-LOW. Next, the 8 column address bits are set up on the address inputs and clocked-in when CAS goes from HIGH-to-LOW.

Note: *RAS also acts as a "master" chip enable for the VRAM. If RAS is inactive, HIGH; all other DRAM control pins (CAS, TR/OE, ME/WE, etc.) are a "don't care" and may change state without effect. No DRAM or TRANSFER cycles will be initiated without RAS falling.*

For single port DRAMs, the OE pin is a "don't care" when RAS goes LOW. For the VRAM, when RAS goes LOW, TR/(OE) selects between DRAM access or TRANSFER cycles. TR/(OE) must be HIGH at the RAS HIGH-to-LOW transition for all DRAM operations (except CAS-BEFORE-RAS).

If (ME)/WE is HIGH when CAS goes LOW, a DRAM READ operation is performed and the data from the memory cells selected will appear at the DQ1-DQ8 port. To enable the DRAM output port, the (TR)/OE input must transition from HIGH-to-LOW some time after RAS falls.

For single port normal DRAMs, WE is a "don't care" when RAS goes LOW. For the VRAM, ME/(WE) is used, when RAS goes LOW, to select between a MASKED WRITE cycle and a normal WRITE cycle. If ME/(WE) is LOW at the RAS HIGH-to-LOW transition, a MASKED WRITE operation is selected. For any DRAM access cycle (READ or WRITE), ME/(WE) must be HIGH at the RAS HIGH-to-LOW transition. If (ME)/WE is LOW before CAS goes LOW, a DRAM EARLY-WRITE operation is performed and the data present on the DQ1-DQ8 data port will be written into the selected memory cells. If (ME)/WE goes LOW after CAS goes LOW, a DRAM LATE-WRITE operation is performed. Refer to the AC timing diagrams.

The VRAM can perform all the normal DRAM cycles including READ, EARLY-WRITE, LATE-WRITE, READ-MODIFY-WRITE, FAST-PAGE-MODE READ, FAST-PAGE-MODE WRITE (Late or Early), and FAST-PAGE-MODE READ-MODIFY-WRITE. Refer to the AC timing parameters and diagrams in the data sheet for more details on these operations.

NONPERSISTENT MASKED WRITE

The MASKED WRITE feature eliminates the need for a READ-MODIFY-WRITE cycle when changing only specific bits within an 8-bit word. The MT42C8128 supports two types of MASKED WRITE cycles, NONPERSISTENT MASKED WRITE and PERSISTENT MASKED WRITE.

If $\overline{ME}$/($\overline{WE}$) and DSF are LOW at the $\overline{RAS}$ HIGH-to-LOW transition, a NONPERSISTENT MASKED WRITE is performed and the data (mask data) present on the DQ1-DQ8 inputs will be written into the mask data register. The mask data acts as an individual write enable for each of the eight DQ1-DQ8 pins. If a LOW (logic "0") is written to a mask data register bit, the input port for that bit is disabled during the subsequent WRITE operation and no new data will be written to that DRAM cell location. A HIGH (logic "1") on a mask data register bit enables the input port and allows normal WRITE operation to proceed. Note that $\overline{CAS}$ is still HIGH. When $\overline{CAS}$ goes LOW, the bits present on the DQ1-DQ8 inputs will be either written to the DRAM (if the mask data bit is HIGH) or ignored (if the mask data bit is LOW). The DRAM contents that correspond to masked input bits will not be changed during the WRITE cycle. The MASKED WRITE is nonpersistent (must be re-entered at every $\overline{RAS}$ cycle) if DSF is LOW when $\overline{RAS}$ goes LOW. The mask data register is cleared at the end of every NONPERSISTENT MASKED WRITE. FAST PAGE MODE can be used with NONPERSISTENT MASKED WRITE to write several column locations in an addressed row. The same mask is used during the entire FAST-PAGE-MODE $\overline{RAS}$ cycle. An example NONPERSISTENT MASKED WRITE cycle is shown in Figure 1.

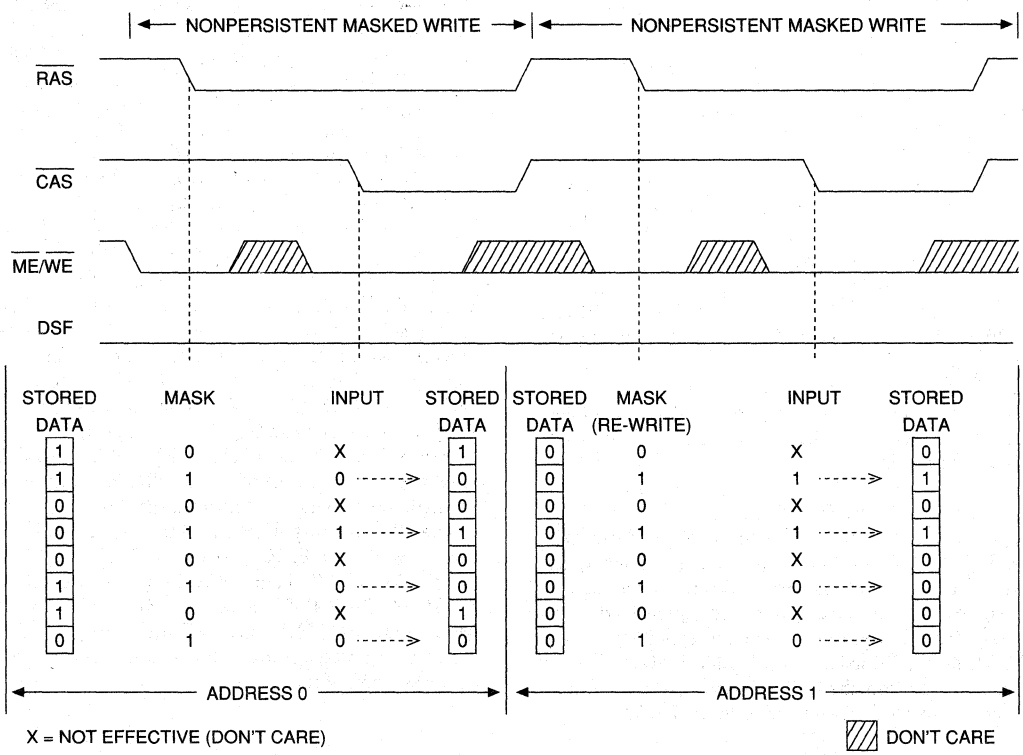


Figure 1
NONPERSISTENT MASKED WRITE EXAMPLE

PERSISTENT MASKED WRITE

The PERSISTENT MASKED WRITE feature eliminates the need to rewrite the mask data before each MASKED WRITE cycle if the same mask data is being used repeatedly. To initiate a PERSISTENT MASKED WRITE, a LOAD MASK REGISTER cycle is performed by taking $\overline{ME}/(\overline{WE})$ and DSF HIGH when $\overline{RAS}$ goes LOW. The mask data is loaded into the internal register when $\overline{CAS}$ goes LOW.

PERSISTENT MASKED WRITE cycles may then be performed by taking $\overline{ME}/(\overline{WE})$ LOW and DSF HIGH when $\overline{RAS}$ goes LOW. The contents of the mask data register will then be used as the mask data for the DRAM inputs. Unlike the NONPERSISTENT MASKED WRITE cycle, the data present on the DQ inputs is not loaded into the mask register when $\overline{RAS}$ falls, and the mask data register will not be cleared at the end of the cycle. Any number of PERSISTENT MASKED WRITE cycles, to any address, may be performed without having to reload the mask data register. Figure 2 shows the LOAD MASK REGISTER and two PERSISTENT MASKED WRITE cycles in operation. The LOAD MASK REGISTER and PERSISTENT MASKED WRITE cycles allow controllers that cannot provide mask data to the DQ pins at $\overline{RAS}$ time to perform MASKED WRITE operations. PERSISTENT MASKED WRITE operations can be performed during FAST PAGE MODE cycles and the same mask will apply to all addressed columns in the addressed row.

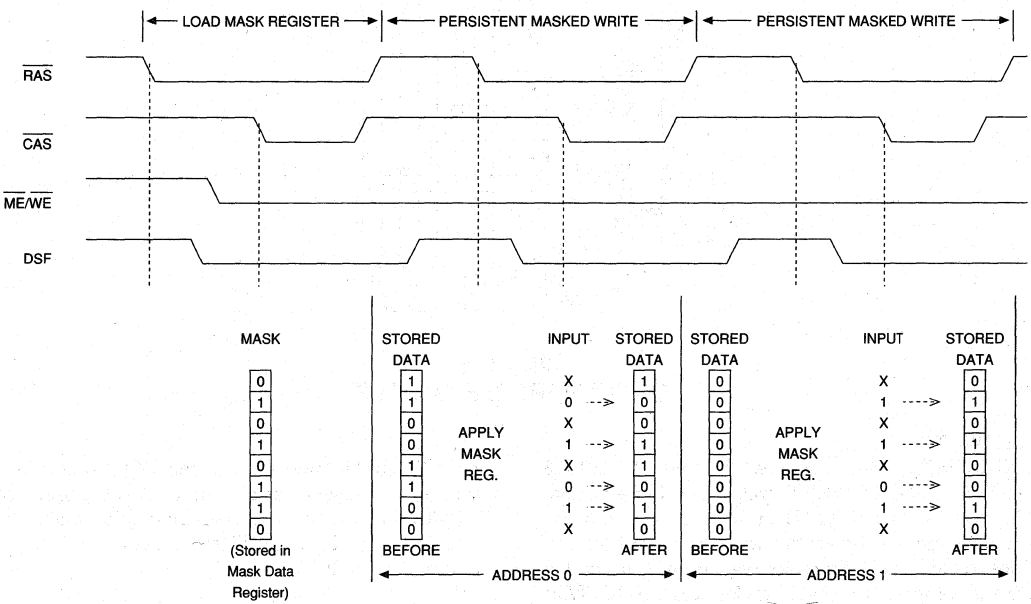


Figure 2
PERSISTENT MASKED WRITE EXAMPLE

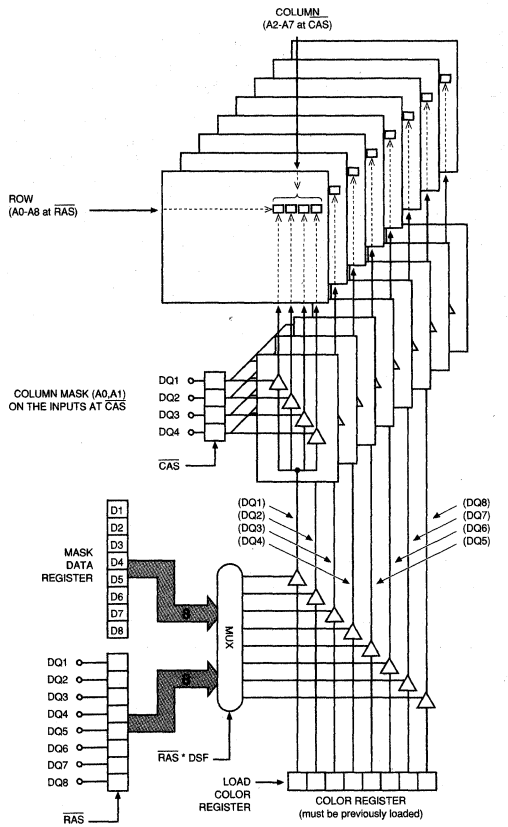


Figure 3
BLOCK WRITE EXAMPLE

BLOCK WRITE

If DSF is HIGH when $\overline{CAS}$ goes LOW, the MT42C8128 will perform a BLOCK WRITE cycle instead of a normal WRITE cycle. In BLOCK WRITE cycles, the contents of the color register are directly written to four adjacent column locations (see Figure 3). The color register must be loaded prior to beginning BLOCK WRITE cycles (see LOAD COLOR REGISTER). Each DQ location of the color register is written to the four column locations (or any of the four that are enabled) in the corresponding DQ bit plane.

The row is addressed as in a normal DRAM WRITE cycle. However when $\overline{CAS}$ goes LOW, only the A2-A7 inputs are used. A2-A7 specify the "block" of four adjacent column locations that will be accessed. The DQ inputs (DQ1, 2, 3, and 4) are then used to determine what combination of the four column locations will be changed. The table on this page illustrates how each of the DQ inputs is used to selectively enable or disable individual column locations within the block. The write enable controls are active HIGH; a logic "1" enables the WRITE function and a logic "0" disables the WRITE function.

	COLUMN ADDRESS CONTROLLED	
INPUTS	A0	A1
DQ1	0	0
DQ2	1	0
DQ3	0	1
DQ4	1	1

NONPERSISTENT MASKED BLOCK WRITE

The MASKED WRITE functions can also be used during BLOCK WRITE cycles. NONPERSISTENT MASKED BLOCK WRITE operates exactly like the normal NONPERSISTENT MASKED WRITE except the mask is now applied to four column locations instead of just one.

Like NONPERSISTENT MASKED WRITE, the combination of $\overline{ME}/(\overline{WE})$ LOW and DSF LOW when $\overline{RAS}$ goes LOW initiates a NONPERSISTENT MASK cycle. The DSF pin must be driven HIGH when $\overline{CAS}$ goes LOW, to perform a NONPERSISTENT MASKED BLOCK WRITE. Using the column mask input and MASKED WRITE function allows any combination of the eight bit planes or four column locations to be masked.

PERSISTENT MASKED BLOCK WRITE

This cycle is also performed exactly like the normal PERSISTENT MASKED WRITE except that DSF is HIGH when $\overline{CAS}$ goes LOW to indicate the BLOCK WRITE function. Both the mask data register and the color register must be loaded with the appropriate data prior to starting a PERSISTENT MASKED BLOCK WRITE.

LOAD MASK DATA REGISTER

The LOAD MASK REGISTER operation and timing are identical to a normal WRITE cycle except that DSF is HIGH when $\overline{RAS}$ goes LOW. As shown in the Truth Table, the combination of $\overline{TR}/(\overline{OE})$, $\overline{ME}/(\overline{WE})$, and DSF being HIGH when $\overline{RAS}$ goes LOW indicates the cycle is a LOAD REGISTER cycle. DSF is used when $\overline{CAS}$ goes LOW to select the register to be loaded, and must be LOW for a LOAD MASK REGISTER cycle. The data present on the DQ lines will then be written to the mask data register.

Note: *For a normal DRAM WRITE cycle, the mask data register is disabled but not modified. The mask data register contents will not be changed unless a NONPERSISTENT MASKED WRITE cycle or a LOAD MASK REGISTER cycle is performed.*

The row address supplied will be refreshed, but it is not necessary to provide any particular row address. The column address inputs are ignored during a LOAD MASK REGISTER cycle.

The mask data register contents are used during PERSISTENT MASKED WRITE and PERSISTENT MASKED BLOCK WRITE cycles to selectively enable writes to the eight DQ planes.

LOAD COLOR REGISTER

The LOAD COLOR REGISTER cycle is identical to the LOAD MASK REGISTER cycle except DSF is HIGH when $\overline{CAS}$ goes LOW. The contents of the color register are retained until changed by another LOAD COLOR REGISTER cycle (or the part loses power) and are used as data inputs during BLOCK WRITE cycles.

TRANSFER OPERATIONS

TRANSFER operations are initiated when $\overline{TR}/(\overline{OE})$ is LOW then $\overline{RAS}$ goes LOW. The state of $(\overline{ME})/\overline{WE}$ when $\overline{RAS}$ goes LOW indicates the direction of the TRANSFER (to or from the DRAM), and DSF is used to select between NORMAL TRANSFER, SPLIT READ TRANSFER, and ALTERNATE WRITE TRANSFER cycles. Each of the TRANSFER cycles available is described below.

READ TRANSFER (DRAM-TO-SAM TRANSFER)

If $(\overline{ME})/\overline{WE}$ is HIGH and DSF is LOW when $\overline{RAS}$ goes LOW, a READ TRANSFER cycle is selected. The row address bits indicate the eight 256-bit DRAM row planes that are to be transferred to the eight SAM data register planes. The column address bits indicate the start address (or Tap address) of the serial output cycle from the SAM data registers. $\overline{CAS}$ must fall for every TRANSFER in order to load a valid Tap address. A read transfer may be accomplished two ways. If the transfer is to be synchronized with SC (REAL-TIME READ TRANSFER), $\overline{TR}/(\overline{OE})$ is taken HIGH after $\overline{CAS}$ goes LOW. If the transfer does not have to be synchronized with SC (READ TRANSFER), $\overline{TR}/(\overline{OE})$ may go HIGH before $\overline{CAS}$ goes LOW (refer to the AC Timing Diagrams). The 2,048 bits of DRAM data are written into the SAM data registers and the serial shift start address is stored in an internal 8-bit register. QSF will be LOW if access is from the lower half (addresses 0 through 127), and HIGH if access is from the upper half (128 through 255). If $\overline{SE}$ is LOW, the first bits of the new row data will appear at the serial outputs with the first SC clock pulse. $\overline{SE}$ enables the serial outputs and may be either HIGH or LOW during this operation. The SAM address pointer will increment with the SC LOW-to-HIGH transition, regardless of the state of $\overline{SE}$. Performing a READ TRANSFER cycle sets the direction of the SAM I/O buffers to the output mode.

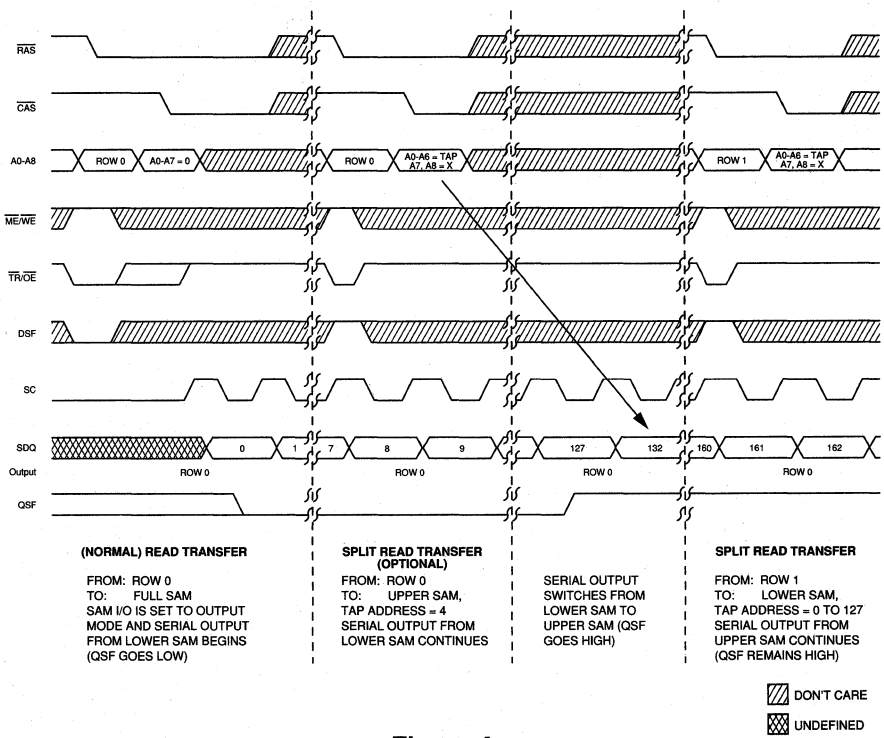


Figure 4
TYPICAL SPLIT-READ-TRANSFER INITIATION SEQUENCE

SPLIT READ TRANSFER (SPLIT DRAM-TO-SAM TRANSFER)

The SPLIT READ TRANSFER (SRT) cycle eliminates the critical transfer timing required to maintain a continuous serial output data stream. When using normal TRANSFER cycles, the REAL-TIME READ TRANSFER cycle has to occur immediately after the last bit of "old data" was clocked out of the SAM port.

When using the SPLIT TRANSFER mode, the SAM is divided into an upper half and a lower half. While data is being serially read from one half of the SAM, new DRAM data may be transferred to the other half. The transfer may occur at any time while the other half is sending data, and need not be synchronized with the SC clock.

The $\overline{TR}/(\overline{OE})$ timing is also relaxed for SPLIT TRANSFER cycles. The rising edge of $\overline{TR}/(\overline{OE})$ is not used to complete the TRANSFER cycle and therefore is independent of the rising edges of $\overline{RAS}$ or $\overline{CAS}$. The transfer timing is generated internally for SPLIT TRANSFER cycles. A SPLIT READ TRANSFER does not change the direction of the SAM port.

A normal, non-split READ TRANSFER cycle must precede any sequence of SPLIT READ TRANSFER cycles to provide a reference to which half of the SAM the access will begin, and to set SAM I/O direction. Then SPLIT READ TRANSFERS may be initiated by taking DSF HIGH when $\overline{RAS}$ goes LOW during the TRANSFER cycle. As in nonsplit transfers, the row address is used to specify the DRAM row to be transferred. The column address, A0-A6, is used to input the SAM Tap address. Address pin A7 is a "don't care" when the Tap address is loaded at the HIGH-to-LOW transition of $\overline{CAS}$. It is internally generated so that the SPLIT TRANSFER will be to the SAM half not currently being accessed.

Figure 4 shows a typical SPLIT READ TRANSFER initiation sequence. The normal READ TRANSFER is first performed, followed by a SPLIT READ TRANSFER of the same row to the upper half of the SAM. The SRT to the upper half is optional, it is only needed if the Tap for the upper half is ≠ 0. Serial access continues, and when the SAM address counter reaches 127 ("A7" = 0, A0-A6 = 1) the new Tap address is loaded for the next half ("A7" = 1, A0-A6 = Tap) and the QSF output goes HIGH. Once the serial access has switched to the upper SAM, new data may be transferred to the lower SAM. The controller must wait for the state of QSF to change and then the new data may be transferred to the SAM half not being accessed. For example, the next step in Figure 4 would be to wait until QSF went LOW (indicating that row-1 data is shifting out of the lower SAM) and then transfer the upper half of row 1 to the upper SAM. If the half boundary is reached, before an SRT is done for the half, a Tap address of "0" will be used. Access will start at 0 if going to the lower half, and 128 if going to the upper half. See Figure 5.

WRITE TRANSFER (SAM-TO-DRAM TRANSFER)

The operation of the WRITE TRANSFER is identical to that of the READ TRANSFER described previously except $(\overline{ME})/\overline{WE}$ and $\overline{SE}$ must be LOW when $\overline{RAS}$ goes LOW. The row address indicates the DRAM row to which the SAM data registers will be written. The column address (Tap) indicates the starting address of the next SERIAL INPUT cycle for the SAM data registers. A WRITE TRANSFER changes the direction of the SAM I/O buffers to the input mode. QSF is LOW if access is to the lower half of the SAM, and HIGH if to access the upper half.

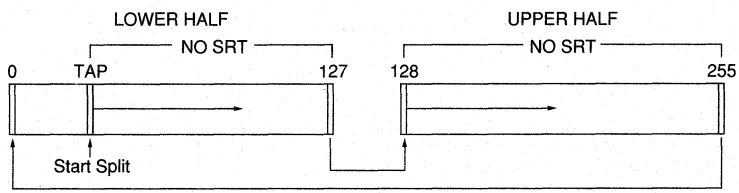


Figure 5
SPLIT SAM TRANSFER

PSEUDO WRITE TRANSFER (SERIAL-INPUT-MODE ENABLE)

The PSEUDO WRITE TRANSFER cycle is used to change the direction of the SAM port from output to input without performing a WRITE TRANSFER cycle. A PSEUDO WRITE TRANSFER cycle is a WRITE TRANSFER cycle with $\overline{SE}$ held HIGH instead of LOW. The DRAM data will not be disturbed and the SAM will be ready to accept input data.

ALTERNATE WRITE TRANSFER (SAM-TO-DRAM TRANSFER)

The operation of the ALTERNATE WRITE TRANSFER is identical to the WRITE TRANSFER except that the DSF pin is HIGH and $(\overline{ME})/\overline{WE}$ is LOW when $\overline{RAS}$ goes LOW, allowing $\overline{SE}$ to be a "don't care." This allows the outputs to be disabled using $\overline{SE}$ during a WRITE TRANSFER cycle. ALTERNATE WRITE TRANSFER will change the SAM I/O direction to an input condition.

SERIAL INPUT AND SERIAL OUTPUT

The control inputs for SERIAL INPUT and SERIAL OUTPUT are SC and $\overline{SE}$. The rising edge of SC increments the serial address counter and provides access to the next SAM location. $\overline{SE}$ enables or disables the serial input/output buffers.

Serial output of the SAM contents will start at the serial start address that was loaded in the SAM address counter during a READ or SPLIT READ TRANSFER cycle. The SC input increments the address counter and presents the contents of the next SAM location to the 8-bit port. $\overline{SE}$ is used as an output enable during the SAM output operation. The serial address is automatically incremented with every SC LOW-to-HIGH transition, regardless of whether $\overline{SE}$ is HIGH or LOW. The address progresses through the SAM and will wrap around (after count 127 or 255) to the Tap address of the next half, for split modes. If an SRT was not performed before the half boundary is reached, the count will progress as illustrated in Figure 5. Address count will wrap around (after count 255) to Tap address 0 if in the "full" SAM modes.

SC is also used to clock-in data when the device is in the serial input mode. As in the serial output operation, the contents of the SAM address counter (loaded when the serial input mode was enabled) will determine the serial address of the first 8-bit word written. $\overline{SE}$ acts as a write enable for serial input data and must be LOW for valid serial input. If $\overline{SE}$ = HIGH, the data inputs are disabled and the SAM contents will not be modified. The serial address counter is incremented with every LOW-to-HIGH transition of SC, regardless of the logic level on the $\overline{SE}$ input.

POWER-UP AND INITIALIZATION

After Vcc is at specified operating conditions, for 100µs minimum, eight $\overline{RAS}$ cycles must be executed to initialize the dynamic memory array. Micron recommends that $\overline{RAS}$ = $(\overline{TR})/\overline{OE} \geq V_{IH}$ during power up to ensure that the DRAM I/O pins (DQs) are in a High-Z state. The DRAM array will contain random data.

The SAM portion of the MT42C8128 is completely static in operation and does not require refresh or initialization. The SAM port will power-up in the serial input mode (WRITE TRANSFER) and the I/O pins (SDQs) will be High- Z, regardless of the state of $\overline{SE}$. The mask and color register will contain random data after power-up. QSF initializes in the LOW state.

TRUTH TABLE

CODE	FUNCTION	RAS FALLING EDGE					CAS FALL	A0-A8[1]		DQ1-DQ8[2]		REGISTERS	
		CAS	TR/OE	ME/WE	DSF	SE	DSF	RAS	CAS, A8=X	RAS	CAS, WE[3]	MASK	COLOR
	DRAM OPERATIONS												
CBR	CAS-BEFORE-RAS REFRESH	0	X	X	X	X	X	—	X	—	X	X	X
ROR	RAS-ONLY REFRESH	1	1	X	X	X	—	ROW	—	X	—	X	X
RW	NORMAL DRAM READ OR WRITE	1	1	1	0	X	0	ROW	COLUMN	X	VALID	X	X
RWNM	NONPERSISTENT (LOAD AND USE) MASKED WRITE TO DRAM	1	1	0	0	X	0	ROW	COLUMN	WRITE MASK	VALID DATA	LOAD & USE	X
RWOM	PERSISTENT (USE REGISTER) MASKED WRITE TO DRAM	1	1	0	1	X	0	ROW	COLUMN	X	VALID DATA	USE	X
BW	BLOCK WRITE TO DRAM (NO DATA MASK)	1	1	1	0	X	1	ROW	COLUMN (A2-A7)	X	COLUMN MASK	X	USE
BWNM	NONPERSISTENT (LOAD & USE) MASKED BLOCK WRITE TO DRAM	1	1	0	0	X	1	ROW	COLUMN	WRITE MASK	COLUMN MASK	LOAD & USE	USE
BWOM	PERSISTENT (USE MASK REGISTER) MASKED BLOCK WRITE TO DRAM	1	1	0	1	X	1	ROW	COLUMN (A2-A7)	X	COLUMN MASK	USE	USE
	REGISTER OPERATIONS												
LMR	LOAD MASK REGISTER	1	1	1	1	X	0	ROW[4]	X	X	WRITE MASK	LOAD	X
LCR	LOAD COLOR REGISTER	1	1	1	1	X	1	ROW[4]	X	X	COLOR DATA	X	LOAD
	TRANSFER OPERATIONS												
RT	READ TRANSFER (DRAM-TO-SAM TRANSFER)	1	0	1	0	X	X	ROW	TAP[5]	X	X	X	X
SRT	SPLIT READ TRANSFER (SPLIT DRAM-TO-SAM TRANSFER)	1	0	1	1	X	X	ROW	TAP[5]	X	X	X	X
WT	WRITE TRANSFER (SAM-TO-DRAM TRANSFER)	1	0	0	0	0	X	ROW	TAP[5]	X	X	X	X
PWT	PSEUDO WRITE TRANSFER (SERIAL-INPUT- MODE ENABLE)	1	0	0	0	1	X	ROW[4]	TAP[5]	X	X	X	X
AWT	ALTERNATE WRITE TRANSFER (SAM-TO-DRAM TRANSFER)	1	0	0	1	X	X	ROW	TAP[5]	X	X	X	X

NOTE:
1. These columns show what must be present on the A0-A8 inputs when RAS falls and A0-A7 when CAS falls.
2. These columns show what must be present on the DQ1-DQ8 inputs when RAS falls and when CAS falls.
3. On WRITE cycles (except BLOCK WRITE), the input data is latched at the falling edge of CAS or ME/WE, whichever is later. Similarly, on READ cycles, the output data is activated at the falling edge of CAS or TR/OE, whichever is later.
4. The ROW that is addressed will be refreshed, but no particular ROW address is required.
5. This is the SAM location that the first SC cycle will access. For split SAM transfers, the Tap will be the first address location accessed of the "new" SAM half after the boundary of the current half is reached (127 for lower half, 255 for upper half).

ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc Supply Relative to Vss ..... -1V to +7V
Operating Temperature, T_A (Ambient) ..... 0°C to +70°C
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.5	V	1
Input High (Logic 1) Voltage, All Inputs	V_{IH}	2.4	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, All Inputs	V_{IL}	-1.0	0.8	V	1

DC ELECTRICAL CHARACTERISTICS

(0°C ≤ T_A ≤ 70°C; V_{CC} = 5V ±10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
INPUT LEAKAGE CURRENT Any input (0V ≤ V_{IN} ≤ V_{CC}); all other pins not under test = 0V	I_L	-10	10	µA	
OUTPUT LEAKAGE CURRENT (DQ, SDQ disabled, 0V ≤ V_{OUT} ≤ V_{CC})	I_{OZ}	-10	10	µA	
OUTPUT LEVELS Output High Voltage (I_{OUT} = -2.5mA)	V_{OH}	2.4		V	1
Output Low Voltage (I_{OUT} = 2.5mA)	V_{OL}		0.4	V	

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A8	C_{I1}		5	pF	2
Input Capacitance: $\overline{RAS}$, $\overline{CAS}$, $\overline{ME}$/$\overline{WE}$, $\overline{TR}$/$\overline{OE}$, SC, $\overline{SE}$, DSF	C_{I2}		7	pF	2
Input/Output Capacitance: DQ, SDQ	$C_{I/O}$		9	pF	2
Output Capacitance: QSF	C_O		9	pF	2

CURRENT DRAIN, SAM IN STANDBY

(0°C ≤ T_A ≤ 70°C; Vcc = 5V ±10%)

PARAMETER/CONDITION	SYMBOL	MAX -7	MAX -8	MAX -10	UNITS	NOTES
OPERATING CURRENT ($\overline{RAS}$ and $\overline{CAS}$ = Cycling: ^tRC = ^tRC (MIN))	I_{CC1}	95	85	75	mA	3, 4 26
OPERATING CURRENT: FAST PAGE MODE ($\overline{RAS}$ = V_{IL}; $\overline{CAS}$ = Cycling: ^tPC = ^tPC (MIN))	I_{CC2}	85	75	65	mA	3, 4 27
STANDBY CURRENT: TTL INPUT LEVELS Power supply standby current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH} after 8 $\overline{RAS}$ cycles (MIN); other inputs ≥ V_{IH} or ≤ V_{IL})	I_{CC3}	8	8	8	mA	4
STANDBY CURRENT: CMOS INPUT LEVELS (MT42C8128 L only) ($\overline{RAS}$ = $\overline{CAS}$ ≥ Vcc -0.2V, other inputs ≥ Vcc -0.2V or ≤ 0.2V)	I_{CC4}	500	500	500	µA	4
REFRESH CURRENT: $\overline{RAS}$-ONLY ($\overline{RAS}$ = Cycling; $\overline{CAS}$ = V_{IH})	I_{CC5}	95	85	75	mA	3, 26
REFRESH CURRENT: $\overline{CAS}$-BEFORE-$\overline{RAS}$ ($\overline{RAS}$ and $\overline{CAS}$ = Cycling)	I_{CC6}	95	85	75	mA	3, 5
REFRESH CURRENT: BATTERY BACKUP (BBU) MT42C8128 L only Average power supply current during BATTERY BACKUP refresh: $\overline{CAS}$ ≤ 0.2V or $\overline{CAS}$-BEFORE-$\overline{RAS}$ cycling; $\overline{RAS}$ = ^tRAS (MIN) to 300ns; $\overline{ME}$/$\overline{WE}$, A0-A8 and DQs ≥ Vcc - 0.2V or ≤ 0.2V (DQs may be left open), ^tRC = 62.5µs (512 rows at 62.5µs = 32ms)	I_{CC7}	600	600	600	µA	3, 5
SAM/DRAM DATA TRANSFER	I_{CC8}	105	95	90	mA	3

CURRENT DRAIN, SAM ACTIVE (^tSC = MIN)

(0°C ≤ T_A ≤ 70°C; Vcc = 5V ±10%)

PARAMETER/CONDITION	SYMBOL	MAX -7	MAX -8	MAX -10	UNITS	NOTES
OPERATING CURRENT ($\overline{RAS}$ and $\overline{CAS}$ = Cycling: ^tRC = ^tRC (MIN))	I_{CC9}	150	130	120	mA	3, 4, 26
OPERATING CURRENT: FAST PAGE MODE ($\overline{RAS}$ = V_{IL}; $\overline{CAS}$ = Cycling: ^tPC = ^tPC (MIN))	I_{CC10}	140	120	110	mA	3, 4, 27
STANDBY CURRENT: TTL INPUT LEVELS Power supply standby current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH} after 8 $\overline{RAS}$ cycles (MIN); other inputs ≥ V_{IH} or ≤ V_{IL})	I_{CC11}	55	45	45	mA	3, 4
REFRESH CURRENT: $\overline{RAS}$-ONLY ($\overline{RAS}$ = Cycling; $\overline{CAS}$ = V_{IH})	I_{CC12}	150	130	120	mA	3, 4, 26
REFRESH CURRENT: $\overline{CAS}$-BEFORE-$\overline{RAS}$ ($\overline{RAS}$ and $\overline{CAS}$ = Cycling)	I_{CC13}	150	130	120	mA	3, 4, 5
SAM/DRAM DATA TRANSFER	I_{CC14}	160	130	125	mA	3, 4

DRAM TIMING PARAMETERS

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C ≤ T_A ≤ +70°C; Vcc = 5V ±10%)

AC CHARACTERISTICS		-7		-8		-10			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Random READ or WRITE cycle time	tRC	130		150		180		ns	
READ-MODIFY-WRITE cycle time	tRWC	175		190		230		ns	
FAST-PAGE-MODE READ or WRITE cycle time	tPC	45		50		55		ns	
FAST-PAGE-MODE READ-MODIFY-WRITE cycle time	tPRWC	90		95		110		ns	
Access time from $\overline{RAS}$	tRAC		70		80		100	ns	14
Access time from $\overline{CAS}$	tCAC		20		25		25	ns	15
Access time from ($\overline{TR}$)/$\overline{OE}$	tOE		20		20		25	ns	
Access time from column address	tAA		35		40		45	ns	
Access time from $\overline{CAS}$ precharge	tCPA		40		45		50	ns	
$\overline{RAS}$ pulse width	tRAS	70	20,000	80	20,000	100	20,000	ns	
$\overline{RAS}$ pulse width (FAST PAGE MODE)	tRASP	70	100,000	80	100,000	100	100,000	ns	
$\overline{RAS}$ hold time	tRSH	20		20		25		ns	
$\overline{RAS}$ precharge time	tRP	50		60		70		ns	
$\overline{CAS}$ pulse width	tCAS	20	10,000	20	10,000	25	10,000	ns	
$\overline{CAS}$ hold time	tCSH	70		80		100		ns	
$\overline{CAS}$ precharge time	tCP	10		10		10		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	tRCD	20	50	20	55	20	75	ns	17
$\overline{CAS}$ to $\overline{RAS}$ precharge time	tCRP	10		10		10		ns	
Row address setup time	tASR	0		0		0		ns	
Row address hold time	tRAH	10		10		15		ns	
$\overline{RAS}$ to column address delay time	tRAD	20	45	15	40	20	50	ns	18
Column address setup time	tASC	0		0		0		ns	
Column address hold time	tCAH	15		15		15		ns	
Column address hold time (referenced to $\overline{RAS}$)	tAR	45		55		70		ns	
Column address to $\overline{RAS}$ lead time	tRAL	35		40		50		ns	
Read command setup time	tRCS	0		0		0		ns	
Read command hold time (referenced to $\overline{CAS}$)	tRCH	0		0		0		ns	19
Read command hold time (referenced to $\overline{RAS}$)	tRRH	0		0		0		ns	19
$\overline{CAS}$ to output in Low-Z	tCLZ	3		3		3		ns	
Output buffer turn-off delay	tOFF	3	20	3	20	3	20	ns	20, 23
Output disable	tOD	3	10	3	10	3	20	ns	20, 23
Output disable hold time from start of WRITE	tOEH	10		10		20		ns	27
$\overline{OE}$ LOW to $\overline{RAS}$ HIGH delay time	tROH	0		0		0		ns	

DRAM TIMING PARAMETERS (continued)

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C ≤ T_A ≤ +70°C; Vcc = 5V ±10%)

AC CHARACTERISTICS		-7		-8		-10			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Write command setup time	^tWCS	0		0		0		ns	21
Write command hold time	^tWCH	15		15		15		ns	
Write command hold time (referenced to $\overline{RAS}$)	^tWCR	45		55		70		ns	
Write command pulse width	^tWP	15		15		15		ns	
Write command to $\overline{RAS}$ lead time	^tRWL	20		20		20		ns	
Write command to $\overline{CAS}$ lead time	^tCWL	20		20		20		ns	
Data-in setup time	^tDS	0		0		0		ns	22
Data-in hold time	^tDH	15		15		15		ns	22
Data-in hold time (referenced to $\overline{RAS}$)	^tDHR	45		55		65		ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	^tRWD	90		100		130		ns	21
Column address to $\overline{WE}$ delay time	^tAWD	55		65		75		ns	21
$\overline{CAS}$ to $\overline{WE}$ delay time	^tCWD	40		45		55		ns	21
Transition time (rise or fall)	^tT	3	35	3	35	3	35	ns	9, 10
Refresh period (512 cycles)	^tREF		8(32)		8(32)		8(32)	ms	29
$\overline{RAS}$ to $\overline{CAS}$ precharge time	^tRPC	0		0		0		ns	
$\overline{CAS}$ setup time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH)	^tCSR	10		10		10		ns	5
$\overline{CAS}$ hold time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH)	^tCHR	10		10		10		ns	5
$\overline{ME}$/$\overline{WE}$ to $\overline{RAS}$ setup time	^tWSR	0		0		0		ns	
$\overline{ME}$/$\overline{WE}$ to $\overline{RAS}$ hold time	^tRWH	15		15		15		ns	
Mask Data to $\overline{RAS}$ setup time	^tMS	0		0		0		ns	
Mask Data to $\overline{RAS}$ hold time	^tMH	15		15		15		ns	

TRANSFER AND MODE CONTROL TIMING PARAMETERS

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes 6, 7, 8, 9, 10) (0° C ≤ T_A ≤ + 70°C; Vcc = 5V ±10%)

AC CHARACTERISTICS		-7		-8		-10			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
$\overline{TR}/(\overline{OE})$ LOW to $\overline{RAS}$ setup time	tTLS	0		0		0		ns	
$\overline{TR}/(\overline{OE})$ LOW to $\overline{RAS}$ hold time	tTLH	15	10,000	15	10,000	15	10,000	ns	
$\overline{TR}/(\overline{OE})$ LOW to $\overline{RAS}$ hold time (REAL-TIME READ-TRANSFER only)	tRTH	65	10,000	70	10,000	80	10,000	ns	
$\overline{TR}/(\overline{OE})$ LOW to $\overline{CAS}$ hold time (REAL-TIME READ-TRANSFER only)	tCTH	25		25		25		ns	
$\overline{TR}/(\overline{OE})$ HIGH to SC lead time	tTSL	5		5		5		ns	
$\overline{TR}/(\overline{OE})$ HIGH to $\overline{RAS}$ precharge time	tTRP	50		60		70		ns	
$\overline{TR}/(\overline{OE})$ to precharge time	tTRW	20		20		30		ns	
First SC edge to $\overline{TR}/(\overline{OE})$ HIGH delay time	tTSD	15		15		15		ns	
Serial output buffer turn-off delay from $\overline{RAS}$	tSDZ	7	40	7	40	7	40	ns	
SC to $\overline{RAS}$ setup time	tSRS	25		30		30		ns	
Serial data input to $\overline{SE}$ delay time	tSZE	0		0		0		ns	
Serial data input delay from $\overline{RAS}$	tSDD	50		50		50		ns	
Serial data input to $\overline{RAS}$ delay time	tSZS	0		0		0		ns	
Serial-input-mode enable ($\overline{SE}$) to $\overline{RAS}$ setup time	tESR	0		0		0		ns	
Serial-input-mode enable ($\overline{SE}$) to $\overline{RAS}$ hold time	tREH	15		15		15		ns	
$\overline{TR}/(\overline{OE})$ HIGH to $\overline{RAS}$ setup time	tYS	0		0		0		ns	
$\overline{TR}/(\overline{OE})$ HIGH to $\overline{RAS}$ hold time	tYH	15		15		15		ns	
DSF to $\overline{RAS}$ setup time	tFSR	0		0		0		ns	
DSF to $\overline{RAS}$ hold time	tRFH	15		15		15		ns	
SC to QSF delay time	tSQD		30		30		30	ns	
SPLIT TRANSFER setup time	tSTS	25		30		30		ns	
SPLIT TRANSFER hold time	tSTH	0		0		0		ns	
$\overline{RAS}$ to QSF delay time	tRQD		75		75		75	ns	
DSF to $\overline{RAS}$ hold time	tFHR	45		60		65		ns	
DSF to $\overline{CAS}$ setup time	tFSC	0		0		0		ns	
DSF to $\overline{CAS}$ hold time	tCFH	15		15		20		ns	
$\overline{TR}/\overline{OE}$ to QSF delay time	tTQD		25		25		25	ns	
$\overline{CAS}$ to QSF delay time	tCQD		35		35		35	ns	
$\overline{RAS}$ to first SC delay	tRSD	80		80		80		ns	
$\overline{CAS}$ to first SC delay	tCSD	30		30		30		ns	

SAM TIMING PARAMETERS

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

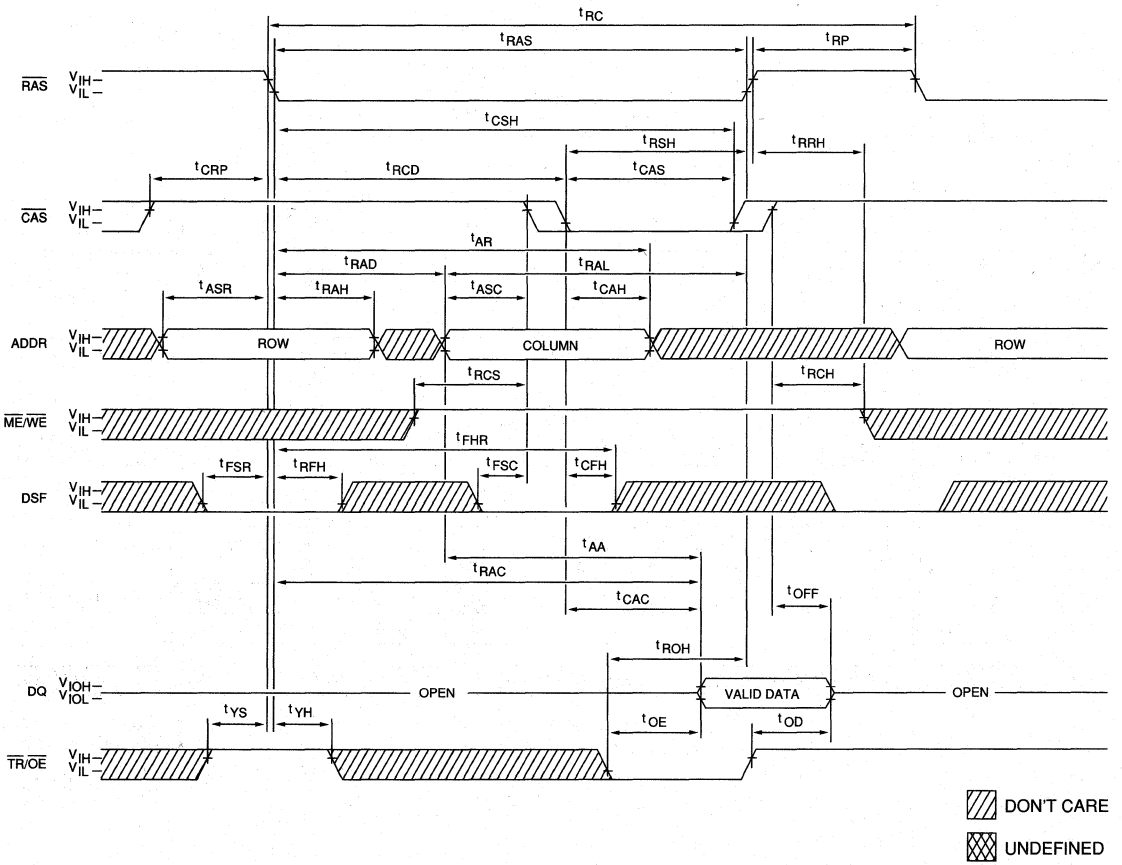
(Notes 6, 7, 8, 9, 10) (0° C ≤ T_A ≤ + 70°C; Vcc = 5V ±10%)

AC CHARACTERISTICS		-7		-8		-10			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Serial clock cycle time	^tSC	25		30		30		ns	
Access time from SC	^tSAC		22		25		27	ns	24
SC precharge time (SC LOW time)	^tSP	8		10		10		ns	
SC pulse width (SC HIGH time)	^tSAS	8		10		10		ns	
Access time from $\overline{SE}$	^tSEA		15		15		15	ns	24
$\overline{SE}$ precharge time	^tSEP	20		20		20		ns	
$\overline{SE}$ pulse width	^tSE	20		20		20		ns	
Serial data-out hold time after SC high	^tSOH	5		5		5		ns	24
Serial output buffer turn-off delay from $\overline{SE}$	^tSEZ	3	12	3	12	3	12	ns	20, 24
Serial data-in setup time	^tSDS	0		0		0		ns	
Serial data-in hold time	^tSDH	10		10		10		ns	
Serial input (Write) Enable setup time	^tSWS	0		0		0		ns	
Serial input (Write) Enable hold time	^tSWH	15		15		15		ns	
Serial input (Write) disable setup time	^tSWIS	0		0		0		ns	
Serial input (Write) disable hold time	^tSWIH	15		15		15		ns	

NOTES

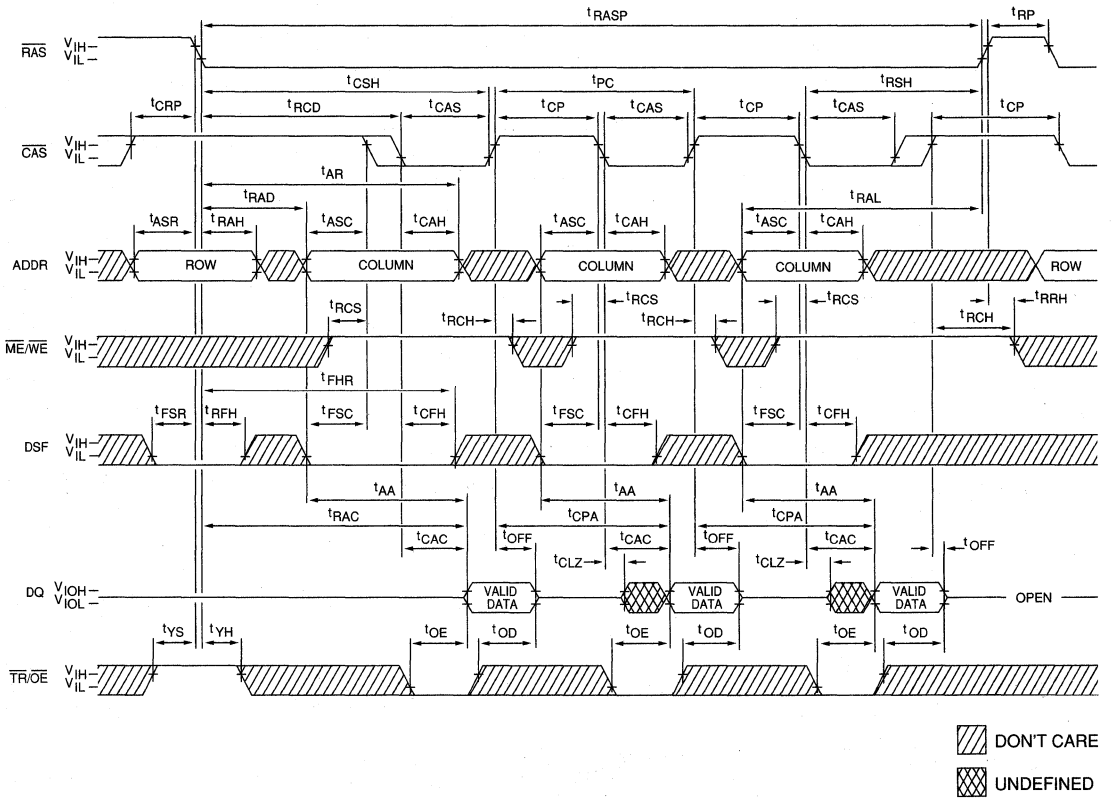
1. All voltages referenced to V_{SS}.
2. This parameter is sampled. V_{CC} = 5V ±10%, f = 1 MHz.
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on I/O loading. Specified values are obtained with minimum cycle time and the I/Os open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \le T_A \le 70°C$) is assured.
7. An initial pause of 100µs is required after power-up followed by any eight $\overline{RAS}$ cycles before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-up should be repeated any time the 8ms refresh requirement is exceeded.
8. AC characteristics assume ^tT = 5ns.
9. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}). Input signals transition between 0V and 3V for AC testing.
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS}$ = V_{IH}, DRAM data output (DQ1-DQ8) is High-Z.
12. If $\overline{CAS}$ = V_{IL}, DRAM data output (DQ1-DQ8) may contain data from the last valid READ cycle.
13. DRAM output timing measured with a load equivalent to 1 TTL gate and 50pF. Output reference levels: V_{OH} = 2.0V; V_{OL} = 0.8V.
14. Assumes that $^tRCD < {}^tRCD$ (MAX). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
15. Assumes that $^tRCD \ge {}^tRCD$ (MAX).
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, DQ will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer, $\overline{CAS}$ must be pulsed HIGH for ^tCPN.
17. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (MAX) limit, then access time is controlled exclusively by ^tCAC.
18. Operation within the ^tRAD (MAX) limit ensures that ^tRCD (MAX) can be met. ^tRAD (MAX) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (MAX) limit, then access time is controlled exclusively by ^tAA.
19. Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
20. ^tOD, ^tOFF and ^tSEZ define the time when the output achieves open circuit (V_{OH} -200mV, V_{OL} +200mV). This parameter is sampled and not 100% tested.
21. ^tWCS, ^tRWD, ^tAWD and ^tCWD are restrictive operating parameters in LATE-WRITE, READ-WRITE and READ-MODIFY-WRITE cycles only. If $^tWCS \ge {}^tWCS$ (MIN), the cycle is an EARLY-WRITE cycle and the data output will remain an open circuit throughout the entire cycle, regardless of $\overline{TR}/\overline{OE}$. If $^tWCS \le {}^tWCS$ (MIN), the cycle is a LATE-WRITE and $\overline{TR}/\overline{OE}$ must control the output buffers during the write to avoid data contention. If $^tRWD \ge {}^tRWD$ (MIN), $^tAWD \ge {}^tAWD$ (MIN) and $^tCWD \ge {}^tCWD$ (MIN), the cycle is a READ-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of the output buffers (at access time and until $\overline{CAS}$ goes back to V_{IH}) is indeterminate but the WRITE will be valid, if ^tOD and ^tOEH are met. See the LATE-WRITE AC Timing diagram.
22. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY-WRITE cycles and $\overline{ME}/\overline{WE}$ leading edge in LATE-WRITE or READ-WRITE cycles.
23. During a READ cycle, if $\overline{TR}/\overline{OE}$ is LOW then taken HIGH, DQ goes open. The DQs will go open with $\overline{OE}$ or $\overline{CAS}$, whichever goes HIGH first.
24. SAM output timing is measured with a load equivalent to 1 TTL gate and 30pF. Output reference levels: V_{OH} = 2.0V; V_{OL} = 0.8V.
25. LATE-WRITE and READ-MODIFY-WRITE cycles must have ^tOD and ^tOEH met ($\overline{OE}$ HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. The DQs will provide previously read data if $\overline{CAS}$ remains LOW and $\overline{OE}$ is taken LOW after ^tOEH is met. If $\overline{CAS}$ goes HIGH prior to $\overline{OE}$ going back LOW, the DQs will remain open.
26. Address (A0-A8) may be changed two times or less while $\overline{RAS}$ = V_{IL}.
27. Address (A0-A8) may be changed once or less while $\overline{CAS}$ = V_{IH} and $\overline{RAS}$ = V_{IL}.
28. ^tSAC is MAX at 70° C and 4.5V Vcc; ^tSOH is MIN at 0°C and 5.5V Vcc. These limits will not occur simultaneously at any given voltage or temperature $^tSOH = {}^tSAC$ - output transition time, this is guaranteed by design.
29. Values in parenthesis apply to the "L" version.

DRAM READ CYCLE



MULTIPORT DRAM

DRAM FAST-PAGE-MODE READ CYCLE



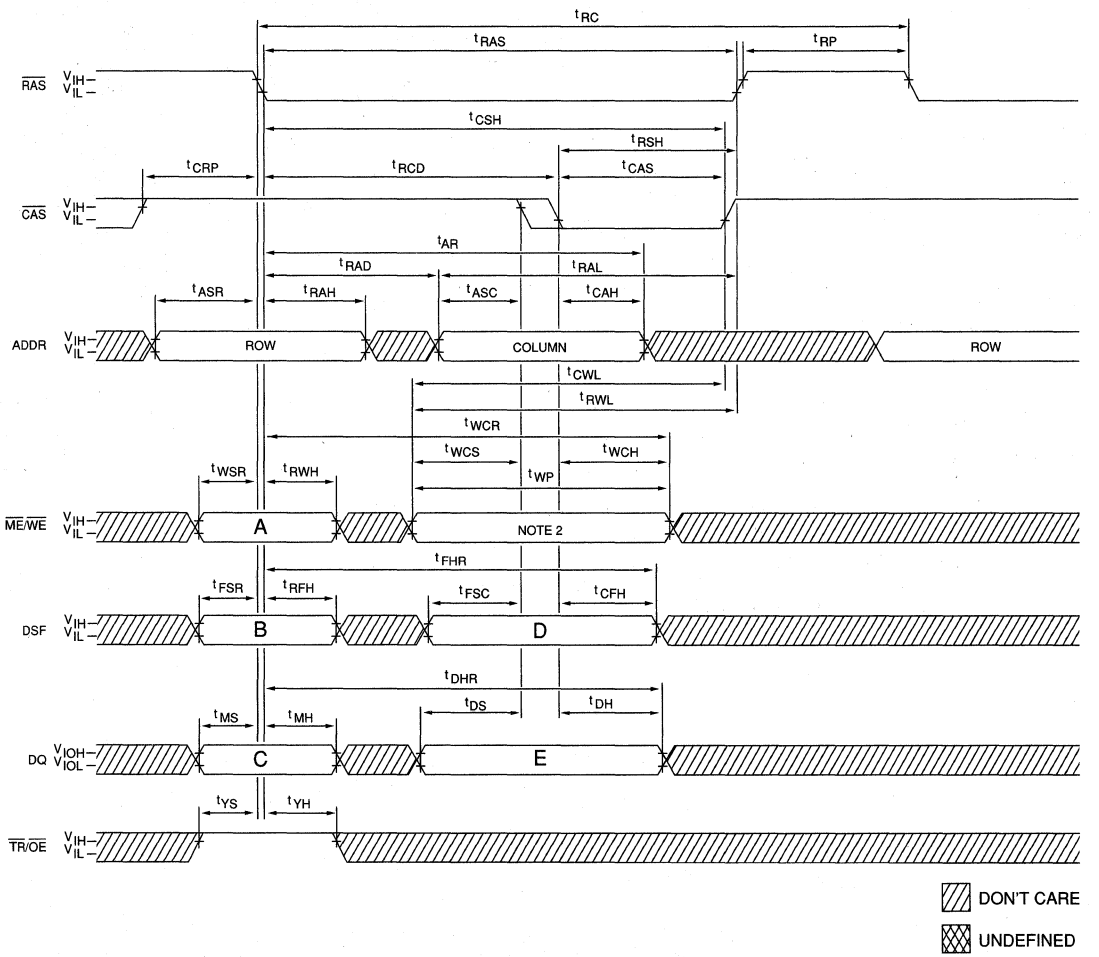
NOTE: WRITE cycles or READ-MODIFY-WRITE cycles may be mixed with READ cycles while in FAST PAGE MODE.

WRITE CYCLE FUNCTION TABLE [1]

FUNCTION	LOGIC STATES				
	RAS Falling Edge			CAS Falling Edge	
	A ME/WE	B DSF	C DQ (Input)	D DSF	E[2] DQ (Input)
Normal DRAM WRITE (or READ)	1	0	X	0	DRAM Data
NONPERSISTENT (Load and Use) MASKED WRITE to DRAM	0	0	Write Mask	0	DRAM Data (Masked)
PERSISTENT (Use Register) MASKED WRITE to DRAM	0	1	X	0	DRAM Data (Masked)
BLOCK WRITE to DRAM (No Data Mask)	1	0	X	1	Column Mask[3]
NONPERSISTENT (Load and Use) MASKED BLOCK WRITE to DRAM	0	0	Write Mask	1	Column Mask[3]
PERSISTENT (Use Register) MASKED BLOCK WRITE to DRAM	0	1	X	1	Column Mask[3]
Load Mask Register	1	1	X	0	Write Mask
Load Color Register	1	1	X	1	Color Data

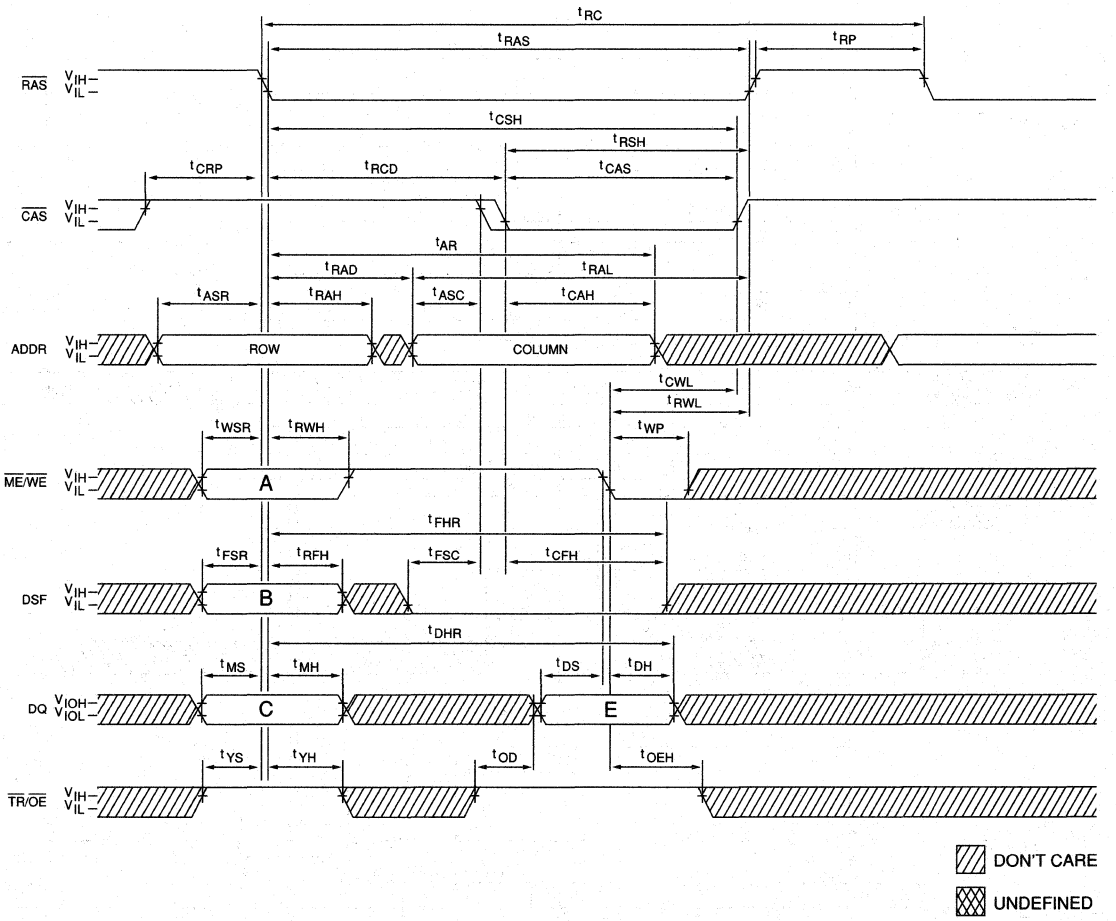
NOTE: 1. Refer to this function table to determine the logic states of "A", "B", "C", "D" and "E" for the WRITE cycle timing diagrams on the following pages.
2. $\overline{CAS}$ or $\overline{ME}/\overline{WE}$, whichever occurs later (except for BLOCK WRITE).
3. $\overline{WE}$ = "don't care" for BLOCK WRITE. The DQ column-mask data will be latched at the falling edge of $\overline{CAS}$, regardless of the state of $\overline{ME}/\overline{WE}$.

DRAM EARLY-WRITE CYCLE [1]



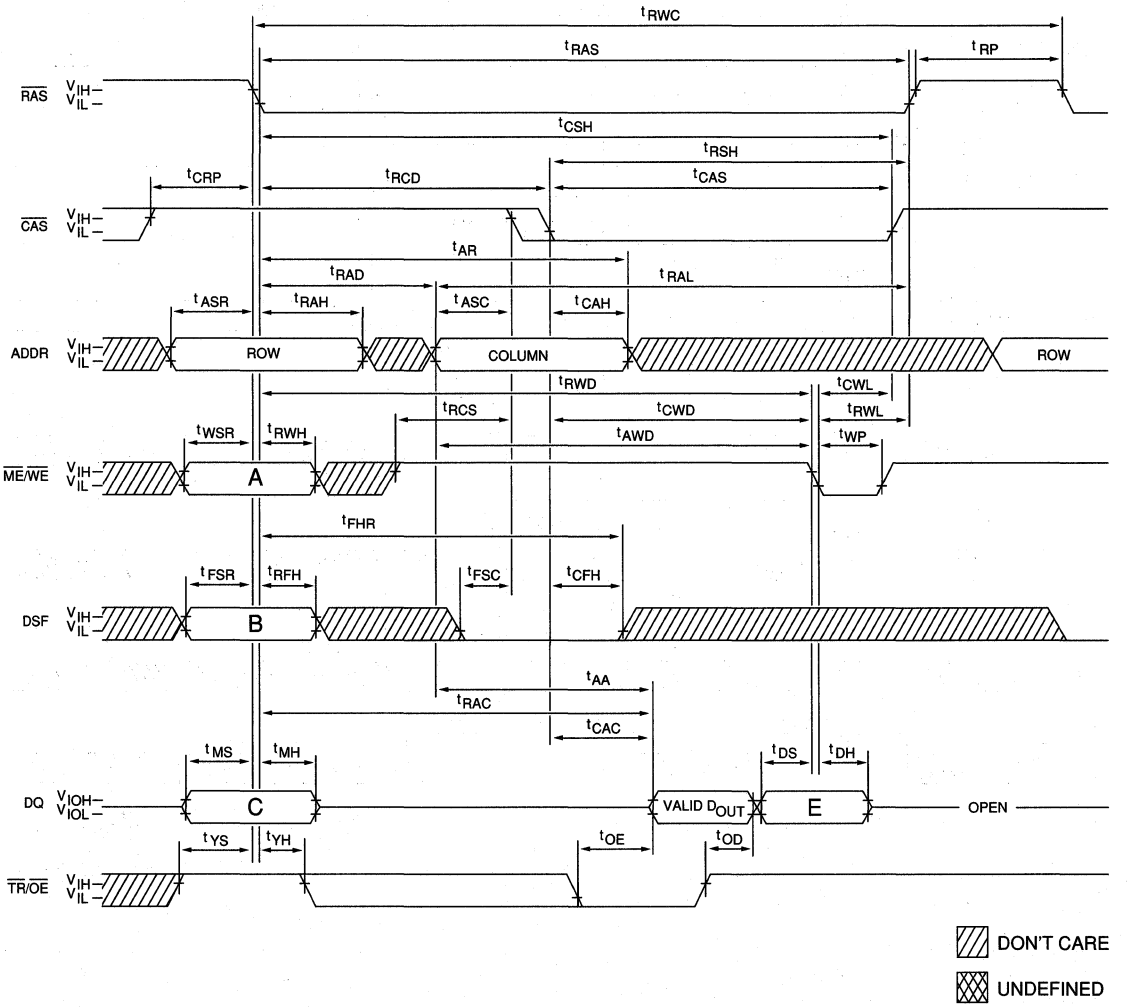
NOTE: 1. The logic states of "A", "B", "C", "D" and "E" determine the type of WRITE operation performed. See the Write Cycle Function Table for a detailed description.
2. For BLOCK WRITE, $\overline{ME}/\overline{WE}$ = "don't care." For all other EARLY-WRITE cycles, $\overline{ME}/\overline{WE}$ = LOW.

DRAM LATE-WRITE CYCLE



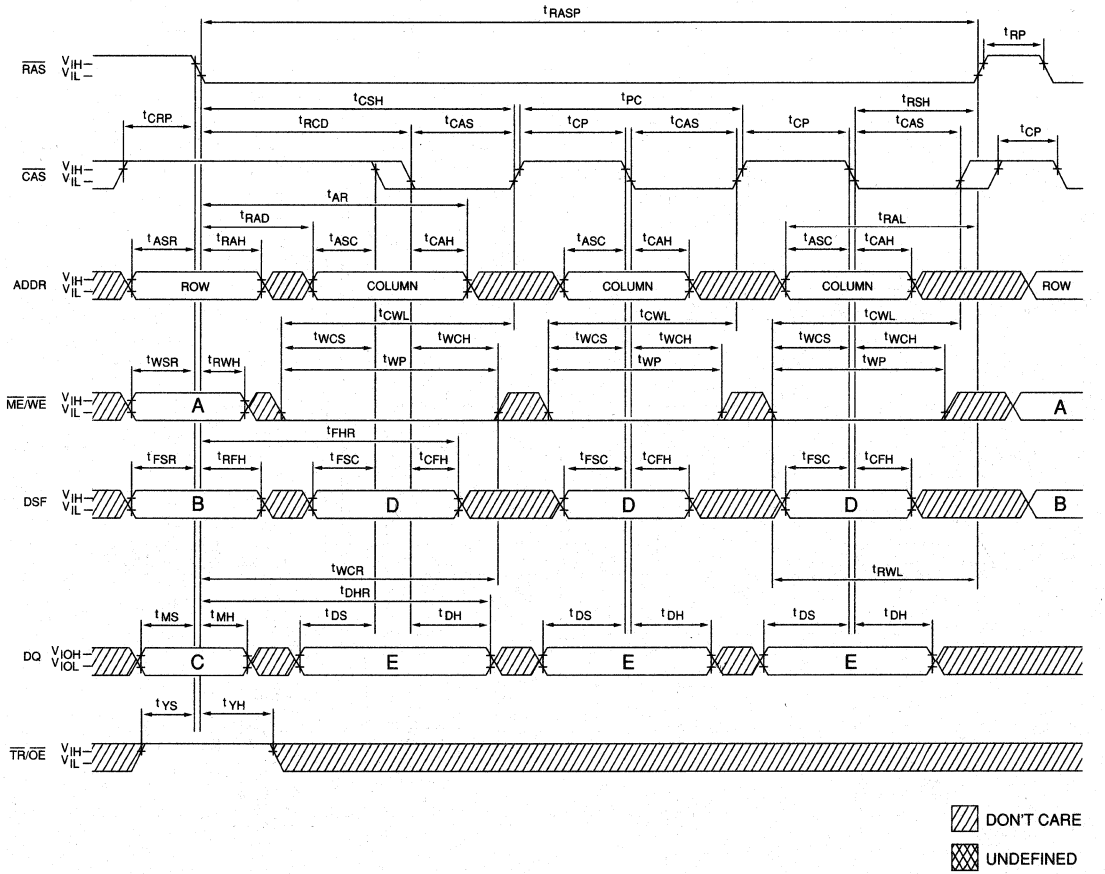
NOTE: The logic states of "A", "B", "C" and "E" determine the type of WRITE operation performed. See the Write Cycle Function Table for a detailed description.

DRAM READ-WRITE CYCLE
(READ-MODIFY-WRITE CYCLE)



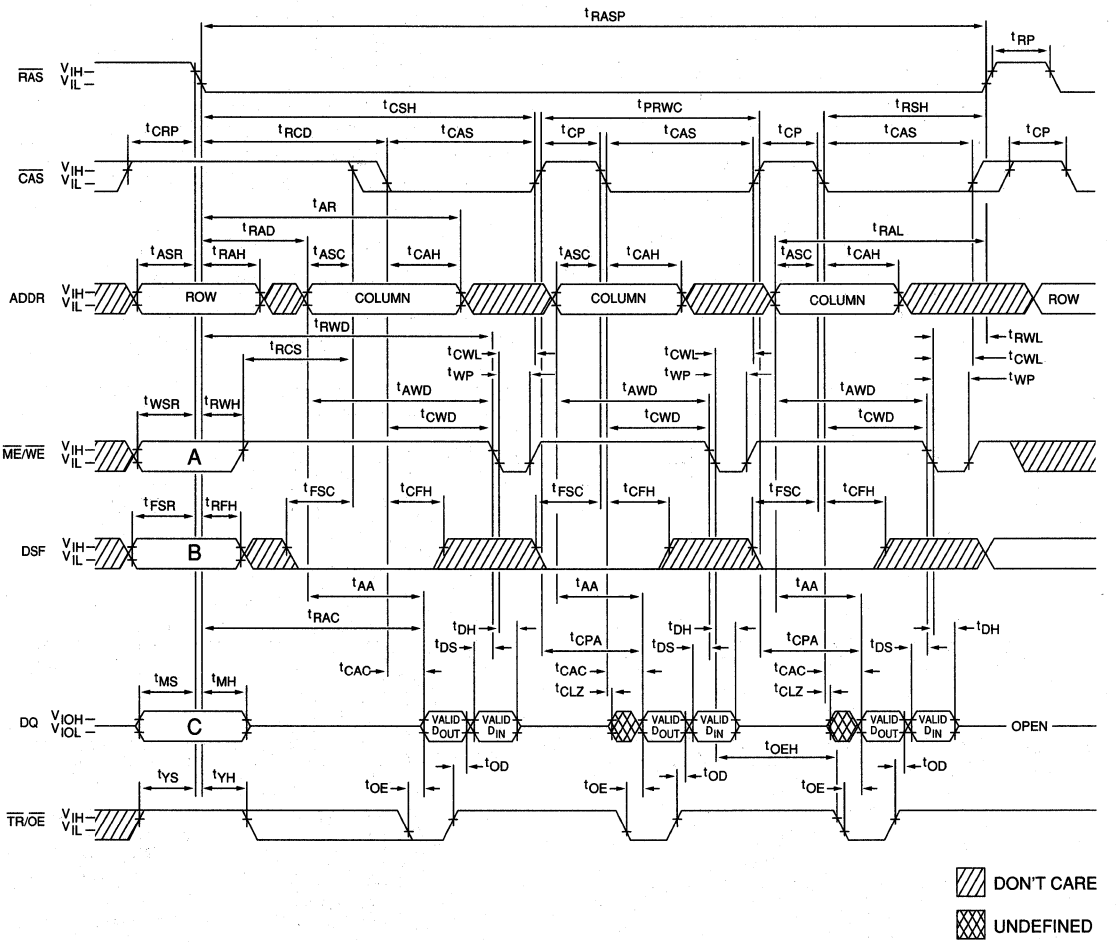
NOTE: The logic states of "A", "B", "C", "D" and "E" determine the type of WRITE operation performed. See the Write Cycle Function Table for a detailed description.

DRAM FAST-PAGE-MODE EARLY-WRITE CYCLE



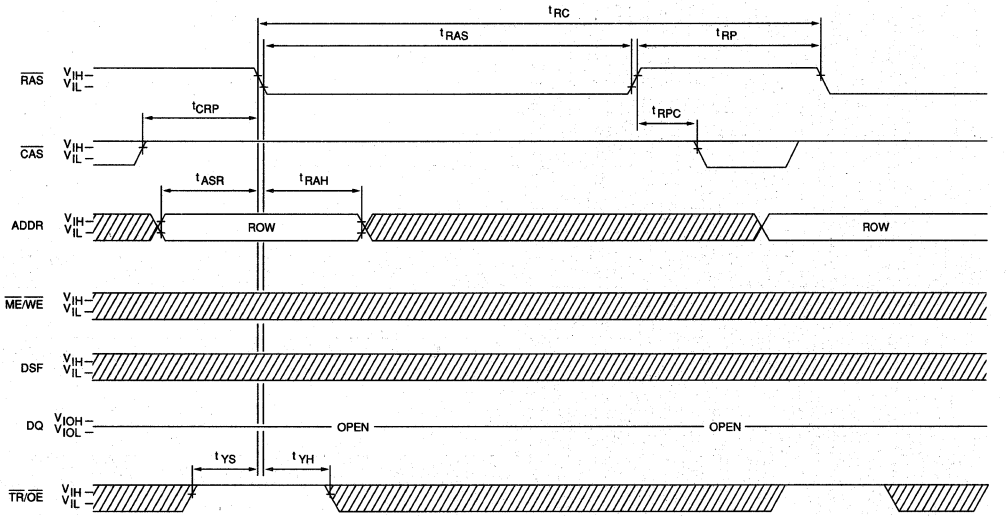
NOTE: 1. READ cycles or READ-MODIFY-WRITE cycles can be mixed with WRITE cycles while in FAST PAGE MODE.
2. The logic states of "A", "B", "C", "D" and "E" determine the type of WRITE operation performed. See the Write Cycle Function Table for a detailed description.

DRAM FAST-PAGE-MODE READ-WRITE CYCLE
(READ-MODIFY-WRITE OR LATE-WRITE CYCLES)

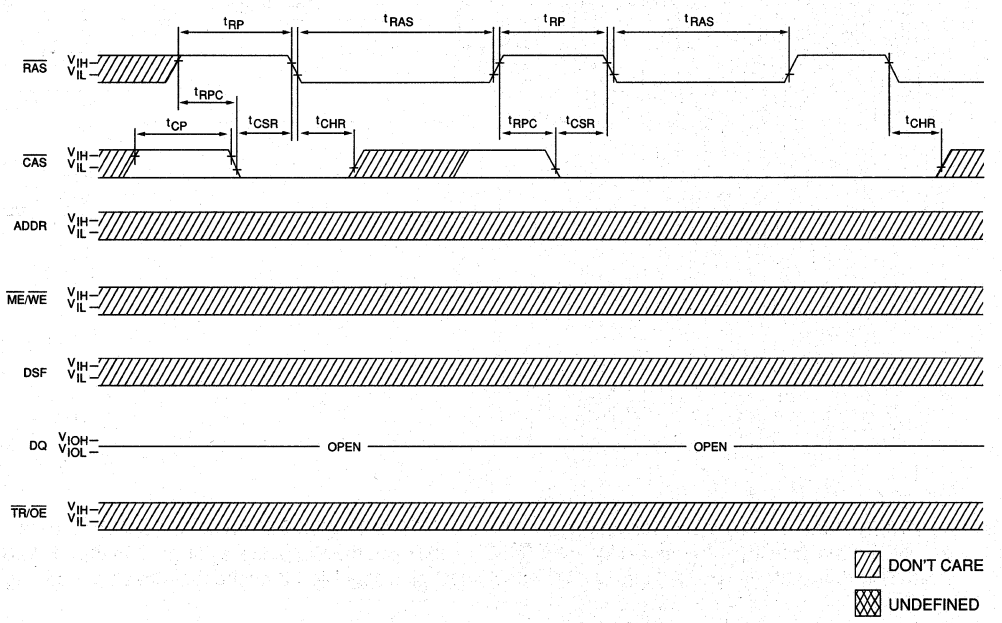


NOTE: 1. READ or WRITE cycles can be mixed with READ-MODIFY-WRITE cycles while in FAST PAGE MODE. Use the Write Function Table to determine the proper DSF state for the desired WRITE operation.
2. The logic states of "A", "B" and "C" determine the type of WRITE operation performed. See the Write Cycle Function Table for a detailed description.

DRAM $\overline{RAS}$-ONLY REFRESH CYCLE
(ADDR = A0-A8)

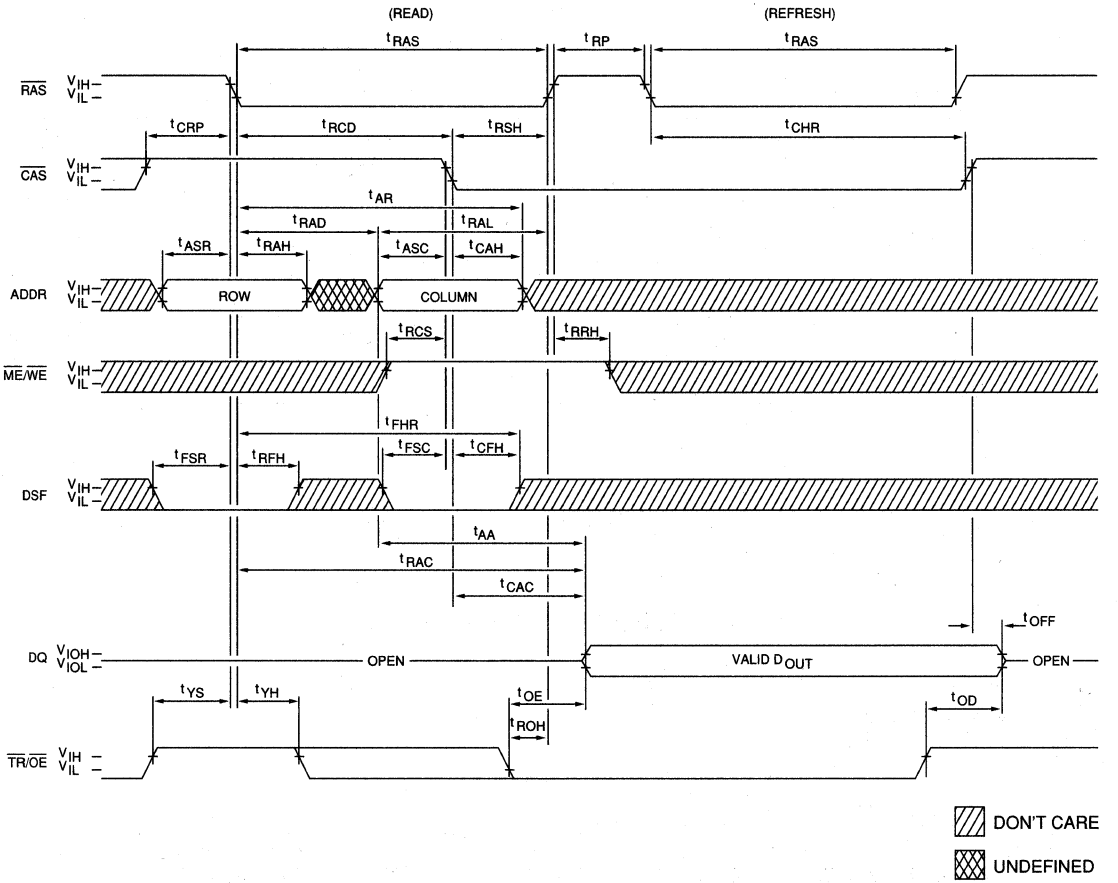


$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE



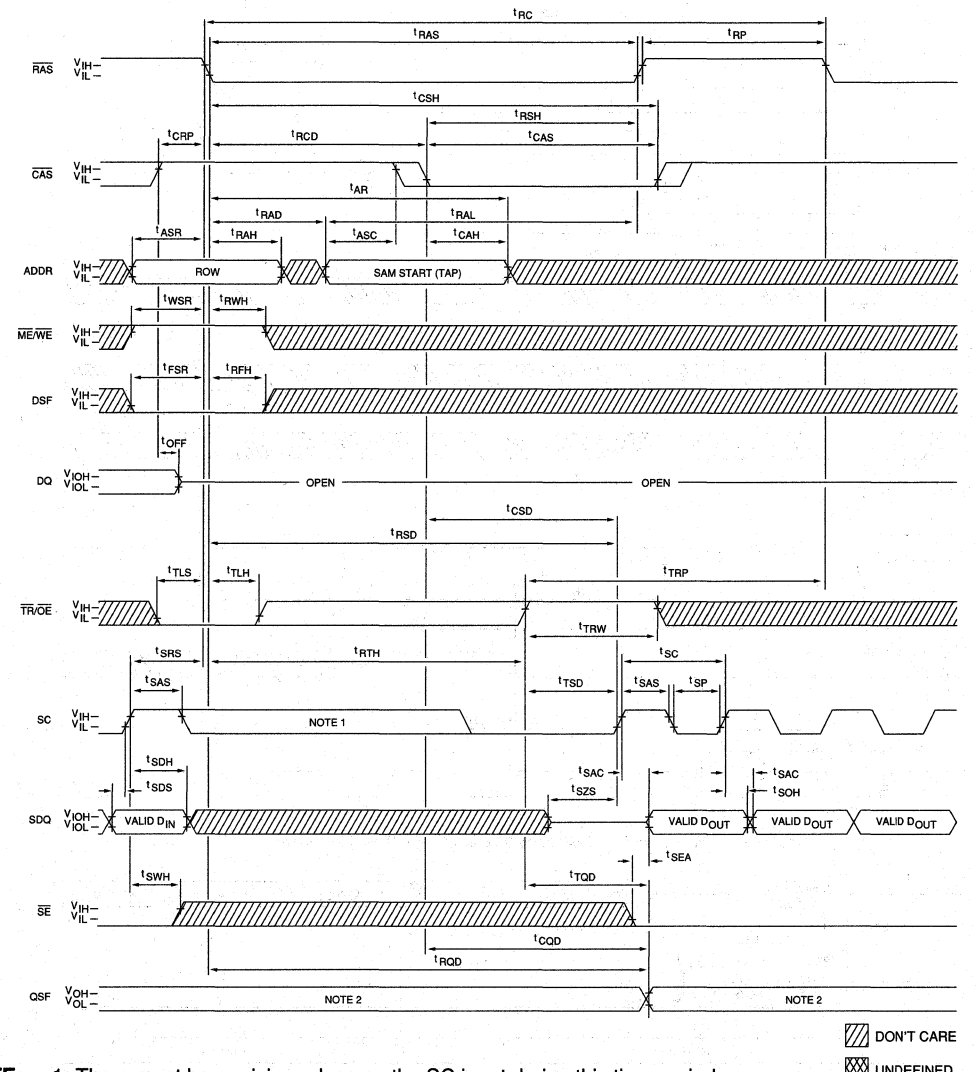
MULTIPORT DRAM

DRAM HIDDEN-REFRESH CYCLE



NOTE: A HIDDEN REFRESH may also be performed after a WRITE or TRANSFER cycle. In the WRITE case, $\overline{ME}/\overline{WE}$ = LOW (when $\overline{CAS}$ goes LOW) and $\overline{TR}/\overline{OE}$ = HIGH and the DQ pins stay High-Z. In the TRANSFER case, $\overline{TR}/\overline{OE}$ = LOW (when $\overline{RAS}$ goes LOW) and the DQ pins stay High-Z during the refresh period, regardless of $\overline{TR}/\overline{OE}$.

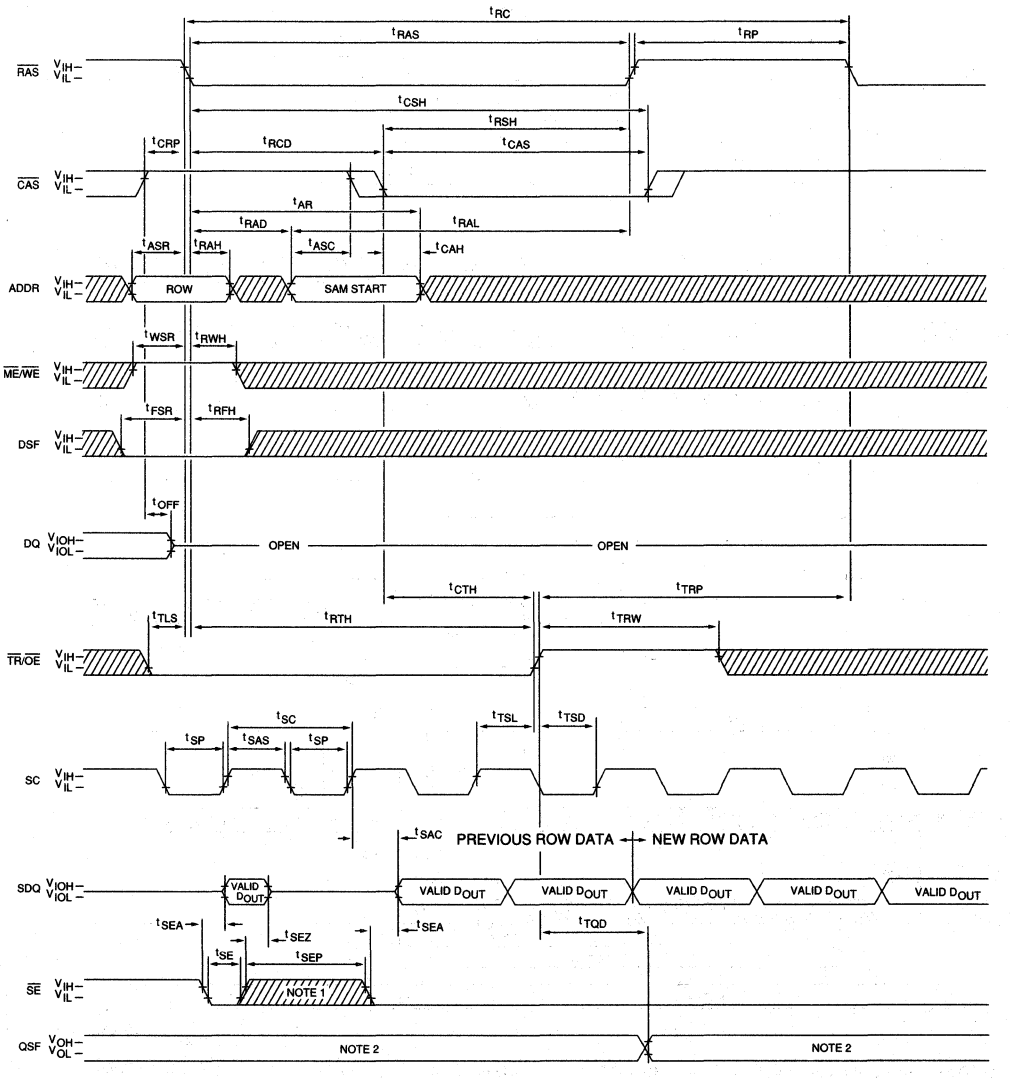
READ TRANSFER [3]
(DRAM-TO-SAM TRANSFER)
(When part was previously in the SERIAL INPUT mode or SC idle)



NOTE:
1. There must be no rising edges on the SC input during this time period.
2. QSF = 0 when the Lower SAM (bits 0–127) is being accessed.
   QSF = 1 when the Upper SAM (bits 128–255) is being accessed.
3. If tTLH is timing for the $\overline{TR}/(\overline{OE})$ rising edge, the transfer is self-timed and the tCSD and tRSD times must be met. If tRTH is timing for the $\overline{TR}/(\overline{OE})$ rising edge, the transfer is done off of the $\overline{TR}/(\overline{OE})$ rising edge and tTSD must be met.

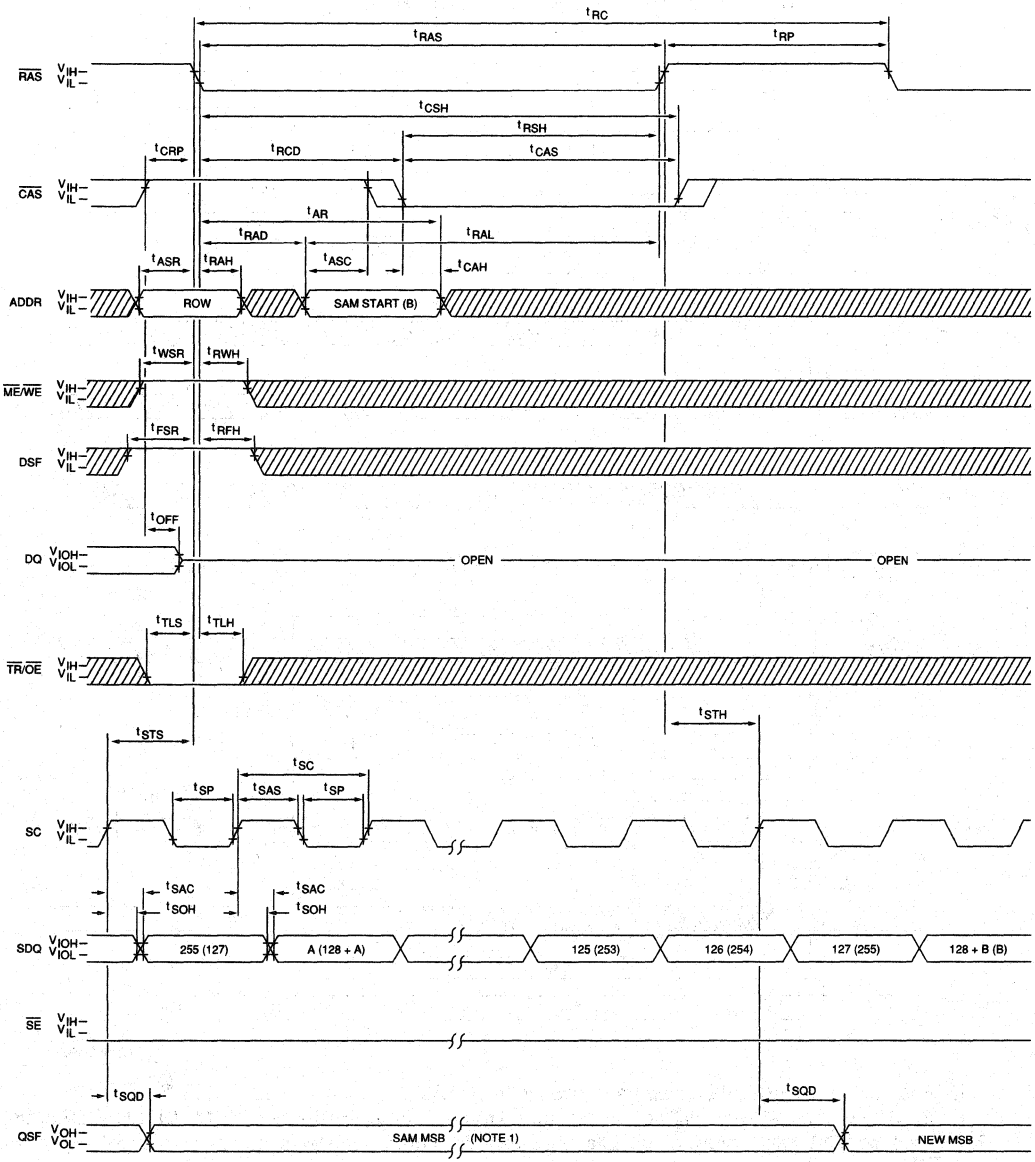
REAL-TIME READ TRANSFER (DRAM-TO-SAM TRANSFER)

(When part was previously in the SERIAL OUTPUT mode)



NOTE: 1. The $\overline{SE}$ pulse is shown to illustrate the SERIAL OUTPUT ENABLE and DISABLE timing. It is not required.
2. QSF = 0 when the Lower SAM (bits 0–127) is being accessed.
QSF = 1 when the Upper SAM (bits 128–255) is being accessed.

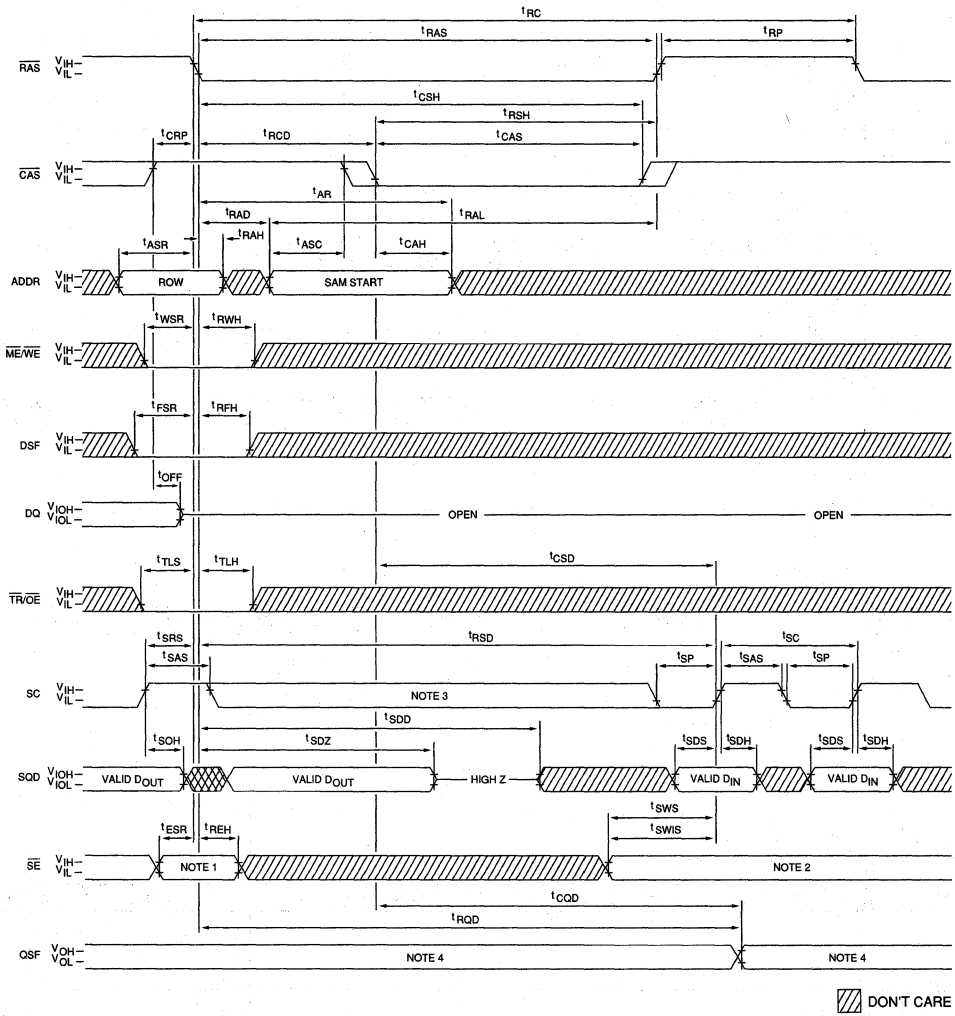
SPLIT READ TRANSFER
(SPLIT DRAM-TO-SAM TRANSFER)



NOTE: 1. QSF = 0 when the Lower SAM (bits 0–127) is being accessed.
QSF = 1 when the Upper SAM (bits 128–255) is being accessed.

WRITE TRANSFER and PSEUDO WRITE TRANSFER (SAM-TO-DRAM TRANSFER)

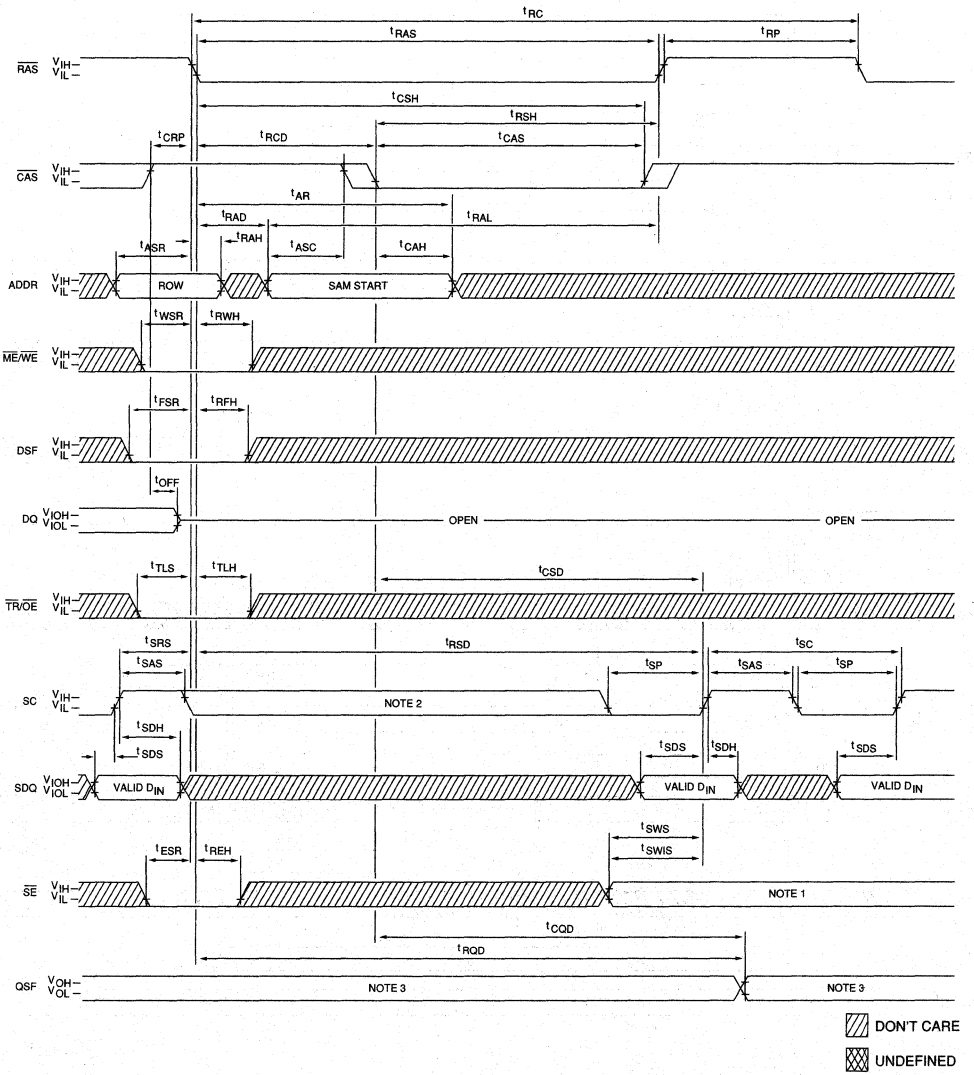
(When part was previously in the SERIAL OUTPUT mode)



NOTE:

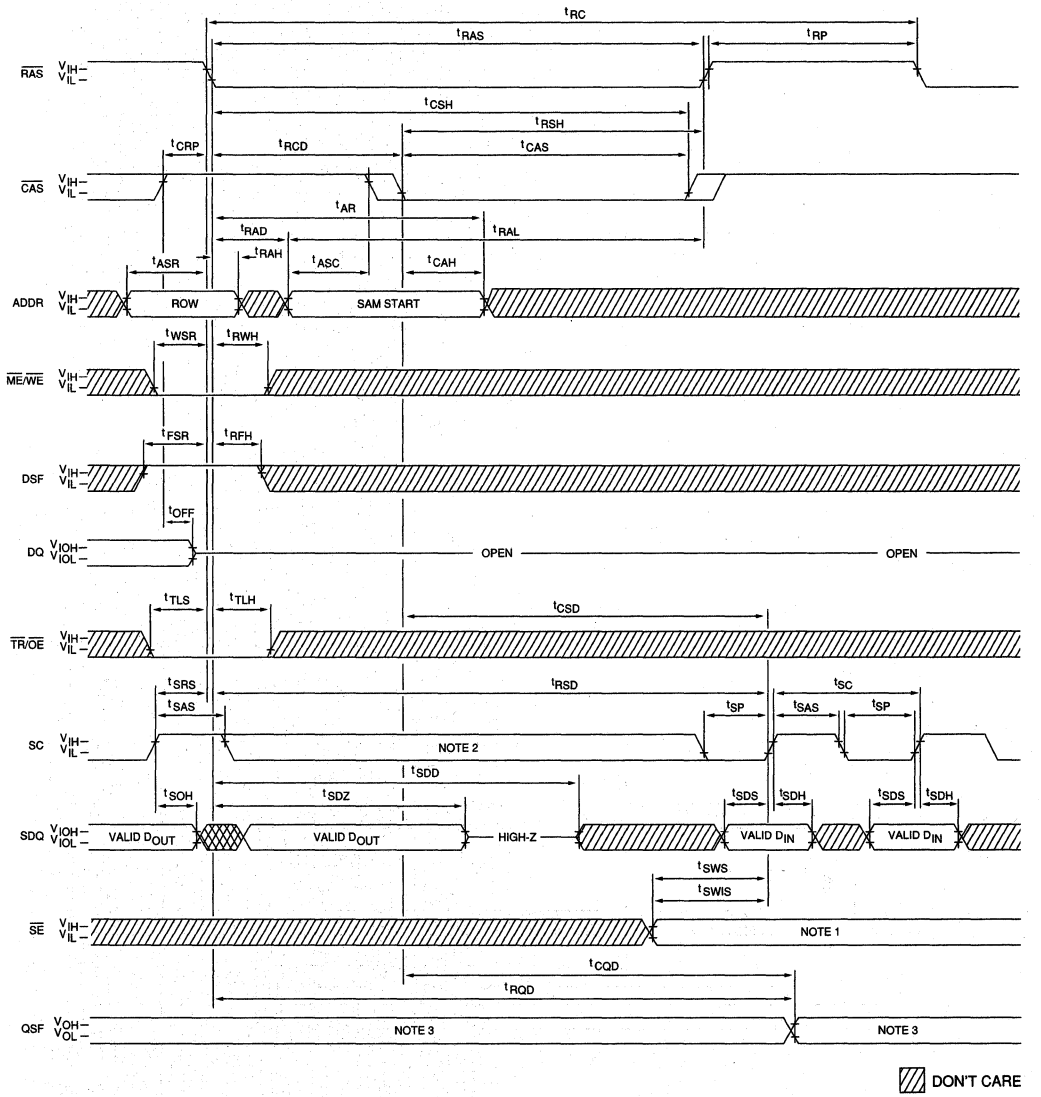
1. If $\overline{SE}$ is LOW, the SAM data will be transferred to the DRAM.
   If $\overline{SE}$ is HIGH, the SAM data will not be transferred to the DRAM (SERIAL-INPUT-MODE ENABLE cycle).
2. $\overline{SE}$ must be LOW to input new serial data, but the serial address register is incremented by SC regardless of $\overline{SE}$.
3. There must be no rising edges on the SC input during this time period.
4. QSF = 0 when the Lower SAM (bits 0–127) is being accessed.
   QSF = 1 when the Upper SAM (bits 128–255) is being accessed.

WRITE TRANSFER
(SAM-TO-DRAM TRANSFER)
(When part was previously in the SERIAL INPUT mode)



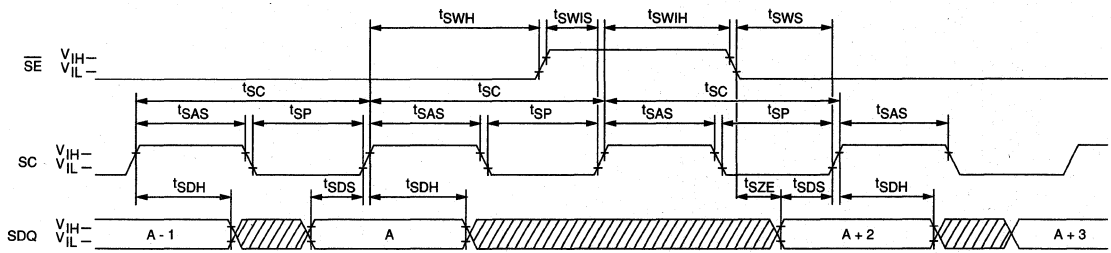
NOTE:
1. $\overline{SE}$ must be LOW to input new serial data, but the serial address register is incremented by SC regardless of $\overline{SE}$.
2. There must be no rising edges on the SC input during this time period.
3. QSF = 0 when the Lower SAM (bits 0–127) is being accessed.
   QSF = 1 when the Upper SAM (bits 128–255) is being accessed.

ALTERNATE WRITE TRANSFER (SAM-TO-DRAM TRANSFER)

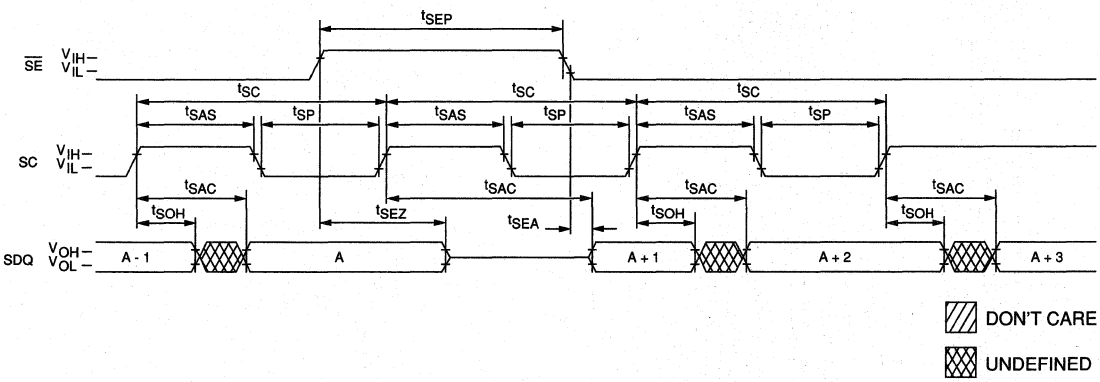


NOTE:
1. $\overline{SE}$ must be LOW to input new serial data, but the serial address register is incremented by SC regardless of $\overline{SE}$.
2. There must be no rising edges on the SC input during this time period.
3. QSF = 0 when the Lower SAM (bits 0–127) is being accessed.
   QSF = 1 when the Upper SAM (bits 128–255) is being accessed.

SAM SERIAL INPUT



SAM SERIAL OUTPUT



MULTIPORT DRAM

VRAM

256K x 8 DRAM WITH 512 x 8 SAM

NEW ■ MULTIPORT DRAM

FEATURES

- Industry standard pinout, timing, and functions
- High-performance, CMOS silicon-gate process
- Single +5V ±10% power supply
- Inputs and outputs are fully TTL compatible
- Refresh modes: RAS ONLY, CAS-BEFORE-RAS (CBR) and HIDDEN
- 512-cycle refresh within 8ms
- FAST PAGE MODE
- Dual port organization: 256K x 8 DRAM port
  512 x 8 SAM port
- No refresh required for serial access memory
- Low power: 10mW standby; 300mW active, typical
- Fast access times – 70ns random, 22ns serial

SPECIAL FUNCTIONS

- NONPERSISTENT MASKED WRITE
- BLOCK WRITE
- SPLIT READ TRANSFER

OPTIONS

	MARKING
• Timing [DRAM, SAM (cycle/access)]	
70ns, 25/22ns	- 7
80ns, 30/25ns	- 8
• Packages	
Plastic SOJ (400 mil)	DJ
Plastic TSOP (400 mil)	TG
Plastic TSOP (400 mil) reverse pinout	RG

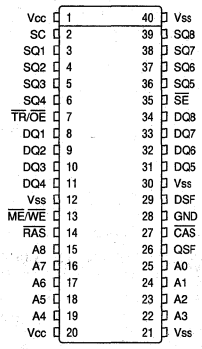
GENERAL DESCRIPTION

The MT42C8255 is a high speed, dual port CMOS dynamic random access memory or video RAM (VRAM) containing 2,097,152 bits. These bits may be accessed by an 8-bit wide DRAM port or by a 512 x 8 bit serial access memory (SAM) port. Data may be transferred from the DRAM to the SAM.

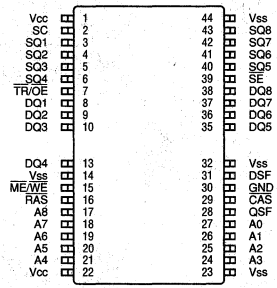
The DRAM portion of the VRAM is functionally identical to the MT4C4256 (256K x 4-bit DRAM), with the addition of MASKED WRITE and BLOCK WRITE. Eight 512-bit data registers make up the serial access memory portion of the VRAM. Data I/O and internal data transfer

PIN ASSIGNMENT (Top View)

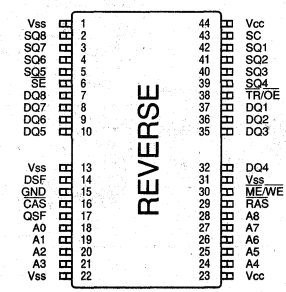
40-Pin SOJ (Q-6)



40/44-Pin TSOP (R-5)



40/44-Pin TSOP* (R-5)



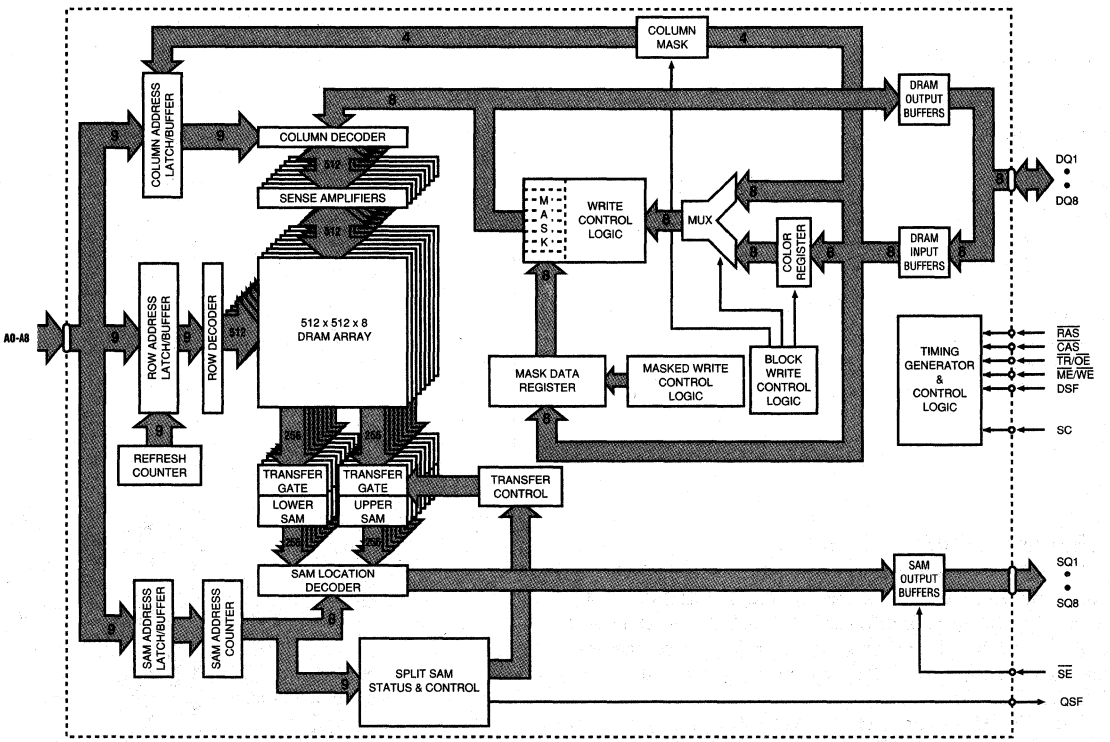
*Consult factory for availability.

are accomplished using three separate data paths: the 8-bit random access I/O port, the eight internal 512-bit wide paths between the DRAM and the SAM, and the 8-bit serial output port for the SAM. The rest of the circuitry consists of the control, timing, and address decoding logic.

Each port may be operated asynchronously and independently of the other except when data is being transferred internally. As with all DRAMs, the VRAM must be refreshed to maintain data. The refresh cycles must be timed so that all 512 combinations of $\overline{RAS}$ addresses are executed at least every 8ms (regardless of sequence). Micron recommends evenly spaced refresh cycles for maximum data integrity. An internal transfer between the DRAM and the SAM counts as a refresh cycle. The SAM portion of the VRAM is fully static and does not require any refresh.

The operation and control of the MT42C8255 are optimized for high performance graphics and communication designs. The dual port architecture is well suited to buffering the sequential data used in raster graphics display, serial/parallel networking and data communications. Special features such as SPLIT READ TRANSFER and BLOCK WRITE allow further enhancements to system performance.

FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTIONS

SOJ PIN NUMBERS	TSOP(TG) PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
2	2	SC	Input	Serial Clock: Clock input to the serial address counter for the SAM registers.
7	7	$\overline{TR/OE}$	Input	Transfer Enable: Enables an internal TRANSFER operation at $\overline{RAS}$ (H → L), or Output Enable: Enables the DRAM output buffers when taken LOW after $\overline{RAS}$ goes LOW ($\overline{CAS}$ must also be LOW), otherwise the output buffers are in a High-Z state.
13	15	$\overline{ME/WE}$	Input	Mask Enable: If $\overline{ME/WE}$ is LOW at the falling edge of $\overline{RAS}$, a MASKED WRITE cycle is performed, or Write Enable: $\overline{ME/WE}$ is also used to select a READ ($\overline{ME/WE}$ = H) or WRITE ($\overline{ME/WE}$ = L) cycle when accessing the DRAM and READ TRANSFER ($\overline{ME/WE}$ = H) to the SAM.
35	39	$\overline{SE}$	Input	Serial Port Enable: $\overline{SE}$ enables the serial output buffers and allows a serial READ operation to occur, otherwise the output buffers are in a High-Z state. The SAM address count will be incremented by the rising edge of SC when $\overline{SE}$ is inactive (HIGH).
29	31	DSF	Input	Special Function Select: DSF is used to indicate which special functions (BLOCK WRITE, MASKED WRITE, SPLIT TRANSFER, etc.) are used for a particular access cycle (see Truth Table).
14	16	$\overline{RAS}$	Input	Row Address Strobe: $\overline{RAS}$ is used to clock-in the 9 row-address bits and strobe the $\overline{ME/WE}$, $\overline{TR/OE}$, DSF, $\overline{SE}$, $\overline{CAS}$ and DQ inputs. It also acts as the master chip enable, and must fall for initiation of any DRAM or TRANSFER cycle.
27	29	$\overline{CAS}$	Input	Column Address Strobe: $\overline{CAS}$ is used to clock-in the 9 column-address bits and strobe the DSF input (BLOCK WRITE only).
25, 24, 23, 22, 19, 18, 17, 16, 15	27, 26, 25, 24, 21, 20, 19, 18, 17	A0-A8	Input	Address Inputs: For the DRAM operation, these inputs are multiplexed and clocked by $\overline{RAS}$ and $\overline{CAS}$ to select one 8-bit word out of the 262,144 available. During TRANSFER operations, A0 to A8 indicate the DRAM row being accessed (when $\overline{RAS}$ goes LOW) and A0-A8 indicate the SAM start address (when $\overline{CAS}$ goes LOW). A8 = "don't care" for the start address during SPLIT READ TRANSFER.
8, 9, 10, 11, 31, 32, 33, 34	8, 9, 10, 13, 35, 36, 37, 38	DQ1-DQ8	Input/ Output	DRAM Data I/O: Data input/output for DRAM access cycles: These pins also act as inputs for Color Register load cycles, DQ Mask and Column Mask for BLOCK WRITE.
3, 4, 5, 6, 36, 37, 38, 39	3, 4, 5, 6, 40, 41, 42, 43	SQ1-SQ8	Output	Serial Data Out: Output or High-Z.
26	28	QSF	Output	Split SAM Status: QSF indicates which half of the SAM is being accessed. LOW if address is 0-255, HIGH if address is 256-511.
28	30	GND	–	No Connect/GND: This pin must be tied to ground to allow for upward functional compatibility with future VRAM feature sets.
1, 20	1, 22	V_{CC}	Supply	Power Supply: +5V ±10%
12, 21, 30, 40	14, 23, 32, 44	V_{SS}	Supply	Ground

FUNCTIONAL DESCRIPTION

The MT42C8255 can be divided into three functional blocks (see Figure 1): the DRAM, the transfer circuitry, and the SAM. All of the operations described below are shown in the AC Timing Diagrams section of this data sheet and summarized in the Truth Table.

Note: *For dual-function pins, the function not being discussed will be surrounded by parentheses. For example, the TR/(OE) pin will be shown as TR/(OE) in references to transfer operations.*

DRAM OPERATION

DRAM REFRESH

Like any DRAM-based memory, the MT42C8255 VRAM must be refreshed to retain data. All 512 row address combinations must be accessed within 8ms. The MT42C8255 supports CAS-BEFORE-RAS, RAS-ONLY and HIDDEN types of refresh cycles.

For the CAS-BEFORE-RAS REFRESH (CBR) cycle, the row addresses are generated and stored in an internal address counter. The user need not supply any address data, and simply must perform 512 CAS-BEFORE-RAS cycles within the 8ms time period.

The refresh address must be generated externally and applied to A0-A8 inputs for RAS-ONLY REFRESH cycles. The DQ pins remain in a High-Z state for both the RAS-ONLY and CAS-BEFORE-RAS cycles.

HIDDEN REFRESH cycles are performed by toggling RAS (and keeping CAS LOW) after a READ or WRITE cycle. This performs CAS-BEFORE-RAS cycles but does not disturb the DQ lines.

Any DRAM READ, WRITE, or TRANSFER cycle also refreshes the DRAM row being accessed. The SAM portion of the MT42C8255 is fully static and does not require any refreshing.

DRAM ACCESS CYCLES (RW)

The DRAM portion of the VRAM is nearly identical to standard 256K x 4 DRAMs. However, because several of the DRAM control pins are used for additional functions on this part, several conditions that were undefined or in "don't care" states for the DRAM are specified for the VRAM. These conditions are highlighted in the following discussion. In addition, the VRAM has special functions that can be used when writing to the DRAM.

The 18 address bits that are used to select an 8-bit word from the 262,144 available are latched into the chip using the A0-A8, RAS and CAS inputs. First, the nine row-address bits are set up on the address inputs and clocked into the part when RAS transitions from HIGH-to-LOW. Next, the 9 column address bits are set up on the address inputs and clocked-in when CAS goes from HIGH-to-LOW.

Note: *RAS also acts as a "master" chip enable for the VRAM. If RAS is inactive, HIGH, all other DRAM control pins (CAS, TR/OE, ME/WE, etc.) are "don't care" and may change state without effect. No DRAM or TRANSFER cycles will be initiated without RAS falling.*

For single port DRAMs, the OE pin is a "don't care" when RAS goes LOW. However, for the VRAM, when RAS goes LOW, TR/(OE) selects between DRAM access or TRANSFER cycles. TR/(OE) must be HIGH at the RAS HIGH-to-LOW transition for all DRAM operations (except CAS-BEFORE-RAS).

A DRAM READ operation is performed if (ME)/WE is HIGH when CAS goes LOW and remains HIGH until CAS goes HIGH. The data from the memory cells selected will appear at the DQ1-DQ8 port. The (TR)/OE input must transition from HIGH-to-LOW some time after RAS falls to enable the DRAM output port.

For single port DRAMs, WE is a "don't care" when RAS goes LOW. For the VRAM, ME/WE performs two functions; write mask enable and data write enable. ME/(WE) is used, when RAS goes LOW, to select between a MASKED WRITE cycle and a normal WRITE cycle. If ME/(WE) is LOW at the RAS HIGH-to-LOW transition, a MASKED WRITE operation is selected. For any non-masked DRAM access cycle (READ or WRITE), ME/(WE) must be HIGH at the RAS HIGH-to-LOW transition. If (ME)/WE is LOW before CAS goes LOW, a DRAM EARLY-WRITE operation is performed and the data present on the DQ1-DQ8 data port will be written into the selected memory cells. If (ME)/WE goes LOW after CAS goes LOW, a DRAM LATE-WRITE operation is performed (refer to the AC timing diagrams).

The VRAM can perform all the normal DRAM cycles including READ, EARLY-WRITE, LATE-WRITE, READ-MODIFY-WRITE, FAST-PAGE-MODE READ, FAST-PAGE-MODE WRITE (Late or Early), and FAST-PAGE-MODE READ-MODIFY-WRITE. Refer to the AC timing parameters and diagrams in the data sheet for more details on these operations.

MASKED WRITE (RWM)

The MASKED WRITE feature eliminates the need for a READ-MODIFY-WRITE cycle when changing individual bits within the 8-bit word. When $\overline{ME}$/($\overline{WE}$) and DSF are LOW at the $\overline{RAS}$ HIGH-to-LOW transition, a MASKED WRITE is performed.

The MT42C8255 supports the nonpersistent mode of MASKED WRITE. In this mode, mask data must be entered with every $\overline{RAS}$ falling edge. The data (mask data) present on the DQ1-DQ8 inputs will be written into the mask data register (see Figure 1). The mask data acts as an individual write enable for each of the eight DQ1-DQ8 pins. If a LOW (logic "0") is written to a mask data register bit, the input port for that bit is disabled during the subsequent WRITE operation and no new data will be written to that DRAM cell location. A HIGH (logic "1") on a mask data register bit enables the input port and allows normal WRITE operation to proceed. Note that $\overline{CAS}$ is still HIGH. When $\overline{CAS}$ goes LOW, the bits present on the DQ1-DQ8 inputs will be either written to the DRAM (if the mask data bit is HIGH) or ignored (if the mask data bit is LOW). The DRAM contents that correspond to masked input bits will not be changed during the WRITE cycle. The mask data register is cleared at the end of every NONPERSISTENT MASKED WRITE.

FAST PAGE MODE can be used with MASKED WRITE to write several column locations in an addressed row. The same mask is used during the entire FAST-PAGE-MODE $\overline{RAS}$ cycle.

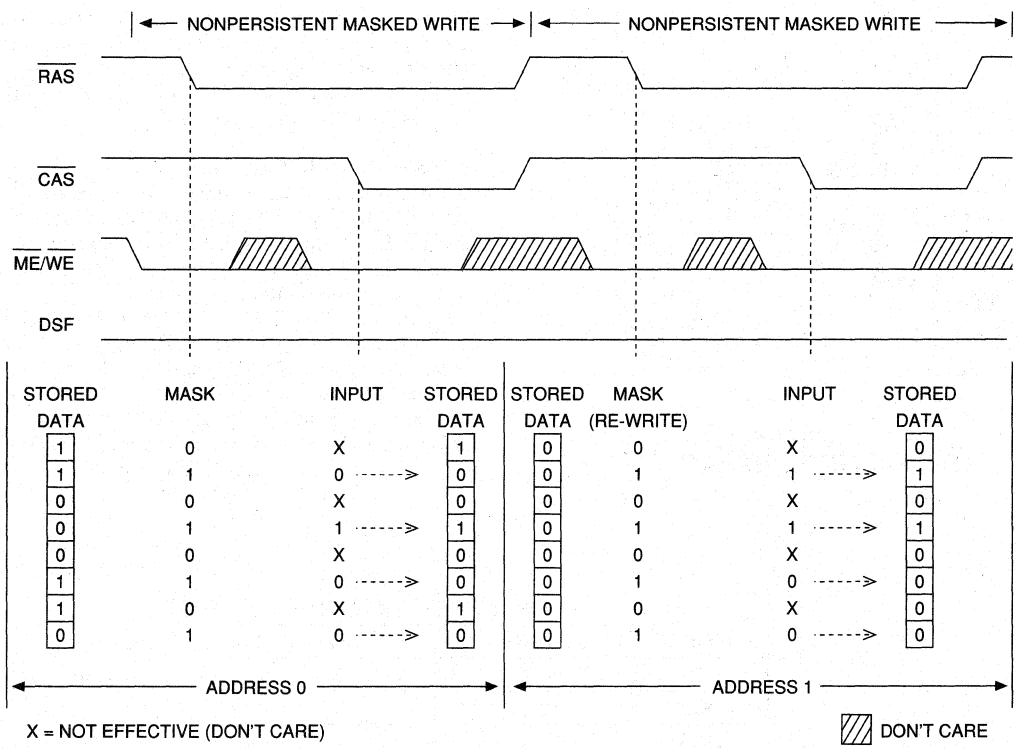


Figure 1
NONPERSISTENT MASKED WRITE EXAMPLE

NEW ■ MULTIPORT DRAM

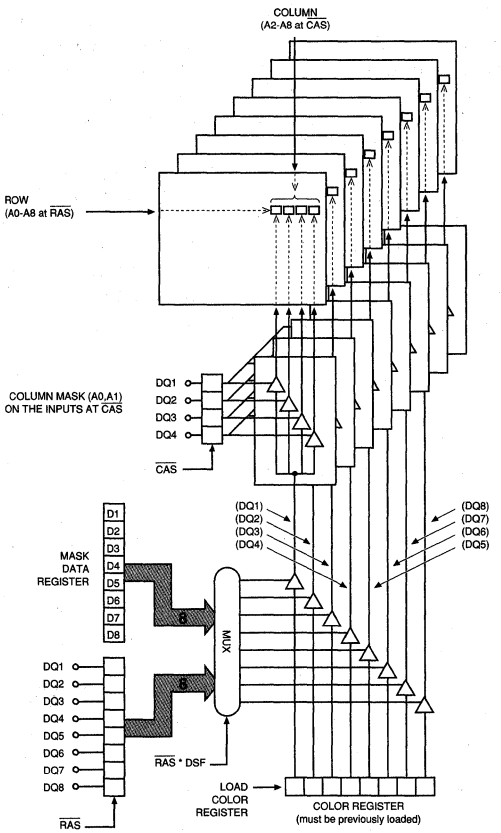


Figure 2
BLOCK WRITE EXAMPLE

BLOCK WRITE (BW)

If DSF is HIGH when $\overline{CAS}$ goes LOW, the MT42C8255 will perform a BLOCK WRITE cycle instead of a normal WRITE cycle. In BLOCK WRITE cycles, the contents of the color register are directly written to four adjacent column locations (see Figure 2). The color register must be loaded prior to beginning BLOCK WRITE cycles (see LOAD COLOR REGISTER). Each DQ location of the color register is written to the four column locations (or any of the four that are enabled) in the corresponding DQ bit plane.

The row is addressed as in a normal DRAM WRITE cycle. However when $\overline{CAS}$ goes LOW, only the A2-A8 inputs are used. A2-A8 specify the "block" of four adjacent column locations that will be accessed. The DQ inputs (DQ1, 2, 3, and 4) are then used to determine what combination of the four column locations will be changed. The DQ inputs are "written" at the falling edge of $\overline{CAS}$ or $\overline{WE}$, whichever occurs later (see the WRITE cycle waveforms). The table on this page illustrates how each of the DQ inputs is used to selectively enable or disable individual column locations within the block. The write enable controls are active HIGH; a logic "1" enables the WRITE function and a logic "0" disables the WRITE function.

MASKED BLOCK WRITE (BWM)

The MASKED WRITE functions may be used during BLOCK WRITE cycles. MASKED BLOCK WRITE operates exactly like the normal MASKED WRITE except the mask is now applied to the 8 bit-planes of 4 column locations instead of just one column location.

The combination of $\overline{ME}$/($\overline{WE}$) LOW and DSF LOW when $\overline{RAS}$ goes LOW initiates a nonpersistent MASKED WRITE cycle. To perform a MASKED BLOCK WRITE, the DSF pin must be HIGH when $\overline{CAS}$ goes LOW. By using both the column mask input and the MASKED WRITE function of BW, any combination of the eight bit planes may be masked, along with any combination of the four column locations.

	COLUMN ADDRESS CONTROLLED	
INPUTS	A0	A1
DQ1	0	0
DQ2	1	0
DQ3	0	1
DQ4	1	1

LOAD COLOR REGISTER (LCR)

A LOAD COLOR REGISTER cycle is identical to the LOAD MASK REGISTER cycle except DSF is HIGH when $\overline{CAS}$ goes LOW. The contents of the 8-bit color register are retained until changed by another LOAD COLOR REGISTER cycle (or the part loses power) and are used as data inputs during BLOCK WRITE cycles.

TRANSFER OPERATIONS

TRANSFER operations are initiated when $\overline{TR}/(\overline{OE})$ is LOW at the falling edge of $\overline{RAS}$. The state of $(\overline{ME})/\overline{WE}$ when $\overline{RAS}$ goes LOW indicates the direction of the TRANSFER (to or from the DRAM), and DSF is used to select between NORMAL TRANSFER and SPLIT TRANSFER cycles. Each of the TRANSFER cycles is described in this section.

READ TRANSFER (RT)

If $(\overline{ME})/\overline{WE}$ is HIGH and DSF is LOW when $\overline{RAS}$ goes LOW, a READ TRANSFER cycle is selected. The row address bits indicate which eight 512-bit DRAM row planes are transferred to the eight SAM data register planes. The column address bits indicate the start address (or Tap address) of the serial output cycle from the SAM data registers. $\overline{CAS}$ must fall for every RT in order to load a valid Tap address. An RT may be accomplished in two ways. If the transfer is to be synchronized with the serial clock, SC, (REAL-TIME READ TRANSFER), $\overline{TR}/(\overline{OE})$ is taken HIGH after $\overline{CAS}$ goes LOW. The TRANSFER will be made when $\overline{TR}/(\overline{OE})$ goes HIGH. If the transfer does not have to be synchronized with SC (READ TRANSFER), $\overline{TR}/(\overline{OE})$ may go HIGH before $\overline{CAS}$ goes LOW and the actual data TRANS-

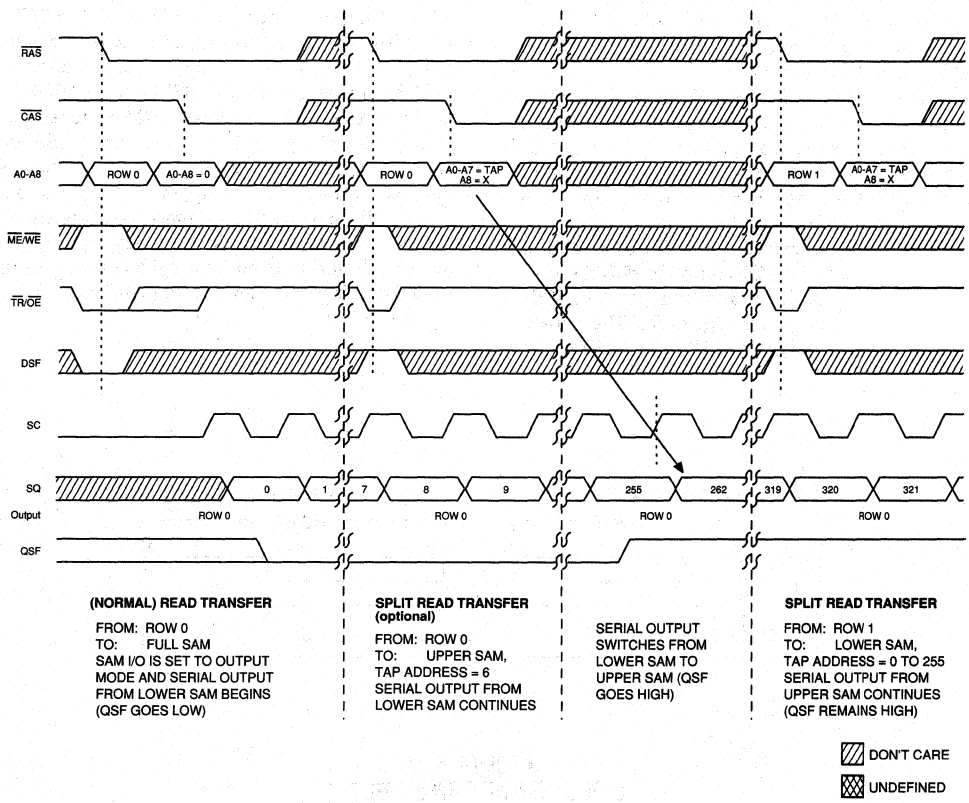


Figure 3
TYPICAL SPLIT-READ-TRANSFER INITIATION SEQUENCE

FER will be timed internally (refer to the AC Timing Diagrams). During the TRANSFER, 4,096 bits of DRAM data are written into the SAM data registers and the Tap address is stored in an internal 9-bit register. The split SAM status pin (QSF) will be LOW if the Tap is in the lower half (addresses 0 through 255), and HIGH if it is in the upper half (256 through 511). If $\overline{SE}$ is LOW, the first bits of the new row data will appear at the serial outputs with the first SC clock pulse. $\overline{SE}$ enables the serial outputs and may be either HIGH or LOW during this operation. The SAM address pointer will increment with the SC LOW-to-HIGH transition, regardless of the state of $\overline{SE}$.

SPLIT READ TRANSFER (SRT)

The SPLIT READ TRANSFER (SRT) cycle eliminates the critical transfer timing required to maintain a continuous serial output data stream. When using normal TRANSFER cycles to do midline reloads, a REAL-TIME READ TRANSFER must be done. The REAL-TIME READ TRANSFER has to occur between the last clock of "old" data and first clock of the "new" data of the SAM port.

When using the SPLIT TRANSFER mode, the SAM is divided into an upper half and a lower half. While data is being serially read from one half of the SAM, new DRAM data may be transferred to the other half. The transfer is not synchronized with the serial clock and may occur at any time while the other half is outputing data.

The $\overline{TR}/(\overline{OE})$ timing is also relaxed for SPLIT TRANSFER cycles. The rising edge of $\overline{TR}/(\overline{OE})$ is not used to complete the TRANSFER cycle and therefore is independent of the falling edge of $\overline{CAS}$ or the rising edge of SC. The transfer timing is generated internally for SPLIT TRANSFER cycles.

A "full" READ TRANSFER cycle must precede any sequence of SRT cycles to provide a reference to which half of the SAM the access will begin (the state of QSF). Then an SRT may be initiated by taking DSF HIGH when $\overline{RAS}$ goes LOW during the TRANSFER cycle. As in nonsplit transfers, the row address is used to specify the DRAM row to be transferred. The column address, A0-A7, is used to input the SAM Tap address. Address pin A8 is a "don't care" when the Tap address is loaded at the HIGH-to-LOW transition of $\overline{CAS}$. It is internally generated in such a manner that the SPLIT TRANSFER will automatically be to the SAM half not being accessed.

Figure 3 shows a typical SRT initiation sequence. The normal READ TRANSFER is performed first, followed by an SRT of the same row to the upper half of the SAM. The SRT to the upper half is optional, and need only be done if the Tap for the upper half is ≠ 0. Serial access continues, and when the SAM address counter reaches 255 ("A8" = 0, A0-A7 = 1) the QSF output goes HIGH, and if an SRT was done for the upper half, the new Tap address is loaded for the next half ("A8" = 1, A0-A7 = Tap). Once the serial access has switched to the upper SAM (QSF has gone HIGH), new data may be transferred to the lower SAM. For example, the next step in Figure 3 would be to wait until QSF went LOW (indicating that row-1 data is shifting out of the lower SAM) and execute an SRT of the upper half of row 1 to the upper SAM. If the half boundary is reached before an SRT is done for the next half, the device will leave split mode and the access will start from address 256 if going to the upper half or at 0 if going to the lower half (see Figure 4).

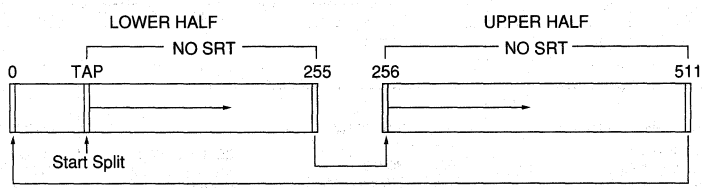


Figure 4
SPLIT SAM TRANSFER

SERIAL OUTPUT

The control inputs for serial output are SC and $\overline{SE}$. The rising edge of SC increments the serial address counter and provides access to the next SAM location. $\overline{SE}$ enables or disables the serial output buffers.

Serial output of the SAM contents will start at the serial start address that was loaded in the SAM address counter during a READ or SPLIT READ TRANSFER cycle. The SC input increments the address counter and presents the contents of the next SAM location to the 8-bit port. $\overline{SE}$ is used as an output enable during the SAM output operation. The serial address is automatically incremented with every SC LOW-to-HIGH transition, regardless of whether $\overline{SE}$ is HIGH or LOW. The address progresses through the SAM and will wrap around (after count 255 or 511) to the Tap address of the next half for split modes. If an SRT was not performed before the half boundary is reached, the count will progress as illustrated in Figure 4. Address count will wrap around (after count 511) to Tap address 0 if in the "full" SAM modes.

POWER-UP AND INITIALIZATION

After V_{CC} is at specified operating conditions, for 100µs minimum, eight $\overline{RAS}$ cycles must be executed to initialize the dynamic memory array. Micron recommends that $\overline{RAS}$ = $\overline{TR}$/ $\overline{OE}$ ≥ V_{IH} during power up to ensure that the DRAM I/O pins (DQs) are in a High-Z state. The DRAM array will contain random data.

The SAM portion of the MT42C8255 is completely static in operation and does not require refresh or initialization. The SAM port will power-up with the Output pins (SQs) in High- Z, regardless of the state of $\overline{SE}$. QSF initializes in the LOW state. The color register will contain random data after power-up.

NEW ■ MULTIPORT DRAM

TRUTH TABLE

CODE	FUNCTION	RAS FALLING EDGE				CAS FALL	A0-A8[1]		DQ1-DQ8[2]		REGISTER
		CAS	TR/OE	ME/WE	DSF	DSF	RAS	CAS	RAS	CAS,WE[3]	COLOR
	DRAM OPERATIONS										
CBR	CAS-BEFORE-RAS REFRESH	0	X	1[6]	1[6]	—	X	X	—	X	X
ROR	RAS ONLY REFRESH	1	1	X	X	—	ROW	—	X	—	X
RW	NORMAL DRAM READ OR WRITE	1	1	1	0	0	ROW	COLUMN	X	VALID DATA	X
RWM	MASKED WRITE TO DRAM (NEW MASK)	1	1	0	0	0	ROW	COLUMN	WRITE MASK	VALID DATA	X
BW	BLOCK WRITE TO DRAM	1	1	1	0	1	ROW	COLUMN (A2-A8)	X	COLUMN MASK	USE
BWM	MASKED BLOCK WRITE TO DRAM (NEW MASK)	1	1	0	0	1	ROW	COLUMN (A2-A8)	WRITE MASK	COLUMN MASK	USE
	REGISTER OPERATIONS										
LCR	LOAD COLOR REGISTER	1	1	1	1	1	ROW[4]	X	X	REG DATA	LOAD
	TRANSFER OPERATIONS										
RT	READ TRANSFER (DRAM-TO-SAM TRANSFER)	1	0	1	0	X	ROW	TAP[5]	X	X	X
SRT	SPLIT READ TRANSFER (SPLIT DRAM-TO-SAM TRANSFER)	1	0	1	1	X	ROW	TAP[5]	X	X	X

NOTE:

1. These columns show what must be present on the A0-A8 inputs when RAS falls and when CAS falls.
2. These columns show what must be present on the DQ1-DQ8 inputs when RAS falls and when CAS falls.
3. During WRITE (including BLOCK WRITE) cycles, the input data is latched at the falling edge of CAS or ME/WE, whichever is later. Similarly, on READ cycles, the output data is valid after the falling edge of CAS or TR/OE, whichever is later.
4. The ROW that is addressed will be refreshed, but a ROW address is not required.
5. This is the first SAM address location that the first SC cycle will access. For split SAM transfers, the Tap will be the first address location accessed of the "new" SAM half after the boundary of the current half is reached (255 for lower half, 511 for upper half).
6. The MT42C8255 does not require a "1" on these pins, but to ensure compatibility with other 2 Meg VRAM function sets, it is recommended.

ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc Supply Relative to Vss ..... -1V to +7V
Operating Temperature, T_A (Ambient) ..... 0°C to +70°C
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.5	V	1
Input High (Logic 1) Voltage, All Inputs	V_{IH}	2.4	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, All Inputs	V_{IL}	-1.0	0.8	V	1

DC ELECTRICAL CHARACTERISTICS

(0°C ≤ T_A ≤ 70°C; V_{CC} = 5V ±10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
INPUT LEAKAGE CURRENT Any input (0V ≤ V_{IN} ≤ V_{CC}); all other pins not under test = 0V	I_L	-10	10	µA	
OUTPUT LEAKAGE CURRENT (DQ, SQ disabled, 0V ≤ V_{OUT} ≤ V_{CC})	I_{OZ}	-10	10	µA	
OUTPUT LEVELS Output High Voltage (I_{OUT} = -2.5mA)	V_{OH}	2.4		V	1
Output Low Voltage (I_{OUT} = 2.5mA)	V_{OL}		0.4	V	

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A8	C_{I1}		5	pF	2
Input Capacitance: $\overline{RAS}$, $\overline{CAS}$, $\overline{ME/WE}$, $\overline{TR/OE}$, SC, $\overline{SE}$, DSF	C_{I2}		7	pF	2
Input/Output Capacitance: DQ, SQ	$C_{I/O}$		9	pF	2
Output Capacitance: QSF	C_O		9	pF	2

CURRENT DRAIN, SAM IN STANDBY

($0°C \le T_A \le 70°C$; V_{CC} = 5V ±10%)

PARAMETER/CONDITION	SYMBOL	MAX -7	MAX -8	UNITS	NOTES
OPERATING CURRENT ($\overline{RAS}$ and $\overline{CAS}$ = Cycling: ^tRC = ^tRC (MIN))	I_{CC1}	120	110	mA	3, 4 25
OPERATING CURRENT: FAST PAGE MODE ($\overline{RAS}$ = V_{IL}; $\overline{CAS}$ = Cycling: ^tPC = ^tPC (MIN), other inputs ≥ V_{IH} or ≤ V_{IL})	I_{CC2}	110	100	mA	3, 4 26
STANDBY CURRENT: TTL INPUT LEVELS Power supply standby current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH} after 8 $\overline{RAS}$ cycles (MIN); other inputs ≥ V_{IH} or ≤ V_{IL})	I_{CC3}	10	10	mA	4
REFRESH CURRENT: $\overline{RAS}$-ONLY ($\overline{RAS}$ = Cycling; $\overline{CAS}$ = V_{IH})	I_{CC4}	120	110	mA	3, 25
REFRESH CURRENT: $\overline{CAS}$-BEFORE-$\overline{RAS}$ ($\overline{RAS}$ and $\overline{CAS}$ = Cycling)	I_{CC5}	120	110	mA	3, 5
SAM/DRAM DATA TRANSFER	I_{CC6}	130	120	mA	3

CURRENT DRAIN, SAM ACTIVE (^tSC = MIN)

($0°C \le T_A \le 70°C$; V_{CC} = 5V ±10%)

PARAMETER/CONDITION	SYMBOL	MAX -7	MAX -8	UNITS	NOTES
OPERATING CURRENT ($\overline{RAS}$ and $\overline{CAS}$ = Cycling: ^tRC = ^tRC (MIN))	I_{CC7}	170	160	mA	3, 4 25
OPERATING CURRENT: FAST PAGE MODE ($\overline{RAS}$ = V_{IL}; $\overline{CAS}$ = Cycling: ^tPC = ^tPC (MIN))	I_{CC8}	160	150	mA	3, 4 26
STANDBY CURRENT: TTL INPUT LEVELS Power supply standby current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH} after 8 $\overline{RAS}$ cycles (MIN); other inputs ≥ V_{IH} or ≤V_{IL})	I_{CC9}	60	60	mA	3, 4
REFRESH CURRENT: $\overline{RAS}$-ONLY ($\overline{RAS}$ = Cycling; $\overline{CAS}$ = V_{IH})	I_{CC10}	170	160	mA	3, 4 25
REFRESH CURRENT: $\overline{CAS}$-BEFORE-$\overline{RAS}$ ($\overline{RAS}$ and $\overline{CAS}$ = Cycling)	I_{CC11}	170	160	mA	3, 4, 5
SAM/DRAM DATA TRANSFER	I_{CC12}	180	170	mA	3, 4

DRAM TIMING PARAMETERS

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C ≤ T_A ≤ +70°C; Vcc = 5V ±10%)

AC CHARACTERISTICS		-7		-8			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Random READ or WRITE cycle time	^tRC	130		150		ns	
READ-MODIFY-WRITE cycle time	^tRWC	175		190		ns	
FAST-PAGE-MODE READ or WRITE cycle time	^tPC	45		50		ns	
FAST-PAGE-MODE READ-MODIFY-WRITE cycle time	^tPRWC	90		95		ns	
Access time from $\overline{RAS}$	^tRAC		70		80	ns	14
Access time from $\overline{CAS}$	^tCAC		20		25	ns	15
Access time from ($\overline{TR}$)/$\overline{OE}$	^tOE		20		20	ns	
Access time from column address	^tAA		35		40	ns	
Access time from $\overline{CAS}$ precharge	^tCPA		40		45	ns	
$\overline{RAS}$ pulse width	^tRAS	70	20,000	80	20,000	ns	
$\overline{RAS}$ pulse width (FAST PAGE MODE)	^tRASP	70	100,000	80	100,000	ns	
$\overline{RAS}$ hold time	^tRSH	20		25		ns	
$\overline{RAS}$ precharge time	^tRP	50		60		ns	
$\overline{CAS}$ pulse width	^tCAS	20	10,000	25	10,000	ns	
$\overline{CAS}$ hold time	^tCSH	70		80		ns	
$\overline{CAS}$ precharge time	^tCP	10		10		ns	16
$\overline{RAS}$ to $\overline{CAS}$ delay time	^tRCD	20	45	20	55	ns	17
$\overline{CAS}$ to $\overline{RAS}$ precharge time	^tCRP	10		10		ns	
Row address setup time	^tASR	0		0		ns	
Row address hold time	^tRAH	10		10		ns	
$\overline{RAS}$ to column address delay time	^tRAD	15	35	15	45	ns	18
Column address setup time	^tASC	0		0		ns	
Column address hold time	^tCAH	15		15		ns	
Column address hold time (referenced to $\overline{RAS}$)	^tAR	45		55		ns	
Column address to $\overline{RAS}$ lead time	^tRAL	35		40		ns	
Read command setup time	^tRCS	0		0		ns	
Read command hold time (referenced to $\overline{CAS}$)	^tRCH	0		0		ns	19
Read command hold time (referenced to $\overline{RAS}$)	^tRRH	0		0		ns	19
$\overline{CAS}$ to output in Low-Z	^tCLZ	3		3		ns	
Output buffer turn-off delay from $\overline{CAS}$	^tOFF	3	20	3	20	ns	20,23
Output disable delay from ($\overline{TR}$)/$\overline{OE}$	^tOD	3	10	3	10	ns	20,23
Output disable hold time from start of WRITE	^tOEH	10		10		ns	27
Output Enable to $\overline{RAS}$ delay	^tROH	0		0		ns	

NEW MULTIPORT DRAM

NEW ■ MULTIPORT DRAM

DRAM TIMING PARAMETERS (continued)

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C ≤ T_A ≤ +70°C; Vcc = 5V ±10%)

AC CHARACTERISTICS		-7		-8			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Write command setup time	^tWCS	0		0		ns	21
Write command hold time	^tWCH	15		15		ns	
Write command hold time (referenced to $\overline{RAS}$)	^tWCR	45		55		ns	
Write command pulse width	^tWP	15		15		ns	
Write command to $\overline{RAS}$ lead time	^tRWL	20		20		ns	
Write command to $\overline{CAS}$ lead time	^tCWL	15		20		ns	
Data-in setup time	^tDS	0		0		ns	22
Data-in hold time	^tDH	15		15		ns	22
Data-in hold time (referenced to $\overline{RAS}$)	^tDHR	45		55		ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	^tRWD	90		100		ns	21
Column address to $\overline{WE}$ delay time	^tAWD	55		65		ns	21
$\overline{CAS}$ to $\overline{WE}$ delay time	^tCWD	40		45		ns	21
Transition time (rise or fall)	^tT	3	35	3	35	ns	9, 10
Refresh period (512 cycles)	^tREF		8		8	ms	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	^tRPC	0		0		ns	
$\overline{CAS}$ setup time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH)	^tCSR	10		10		ns	5
$\overline{CAS}$ hold time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH)	^tCHR	10		10		ns	5
$\overline{ME}$/$\overline{WE}$ to $\overline{RAS}$ setup time	^tWSR	0		0		ns	
$\overline{ME}$/$\overline{WE}$ to $\overline{RAS}$ hold time	^tRWH	15		15		ns	
Mask data to $\overline{RAS}$ setup time	^tMS	0		0		ns	
Mask data to $\overline{RAS}$ hold time	^tMH	15		15		ns	

TRANSFER AND MODE CONTROL TIMING PARAMETERS

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes 6, 7, 8, 9, 10) (0° C ≤ T_A ≤ + 70°C; Vcc = 5V ±10%)

AC CHARACTERISTICS		-7		-8			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
$\overline{TR}/(\overline{OE})$ LOW to $\overline{RAS}$ setup time	^tTLS	0		0		ns	
$\overline{TR}/(\overline{OE})$ LOW to $\overline{RAS}$ hold time	^tTLH	15	10,000	15	10,000	ns	
$\overline{TR}/(\overline{OE})$ LOW to $\overline{RAS}$ hold time (REAL-TIME READ-TRANSFER only)	^tRTH	65	10,000	70	10,000	ns	
$\overline{TR}/(\overline{OE})$ LOW to $\overline{CAS}$ hold time (REAL-TIME READ-TRANSFER only)	^tCTH	25		25		ns	
$\overline{TR}/(\overline{OE})$ HIGH to $\overline{RAS}$ precharge time	^tTRP	50		60		ns	
$\overline{TR}/(\overline{OE})$ precharge time	^tTRW	20		25		ns	
$\overline{TR}/(\overline{OE})$ HIGH to SC lead time	^tTSL	5		5		ns	
First SC edge to $\overline{TR}/(\overline{OE})$ HIGH delay time	^tTSD	15		15		ns	
SC to $\overline{RAS}$ setup time	^tSRS	25		30		ns	
$\overline{TR}/(\overline{OE})$ HIGH to $\overline{RAS}$ setup time	^tYS	0		0		ns	
$\overline{TR}/(\overline{OE})$ HIGH to $\overline{RAS}$ hold time	^tYH	15		15		ns	
DSF to $\overline{RAS}$ setup time	^tFSR	0		0		ns	
DSF to $\overline{RAS}$ hold time	^tRFH	15		15		ns	
SC to QSF delay time	^tSQD		25		30	ns	
SPLIT TRANSFER setup time	^tSTS	25		30		ns	
SPLIT TRANSFER hold time	^tSTH	0		0		ns	
DSF (at $\overline{CAS}$ LOW) to $\overline{RAS}$ hold time	^tFHR	50		55		ns	
DSF to $\overline{CAS}$ setup time	^tFSC	0		0		ns	
DSF to $\overline{CAS}$ hold time	^tCFH	15		15		ns	
$\overline{TR}/\overline{OE}$ to QSF delay time	^tTQD		25		25	ns	
$\overline{RAS}$ to QSF delay time	^tRQD		75		75	ns	
$\overline{CAS}$ to QSF delay time	^tCQD		35		35	ns	
$\overline{RAS}$ to first SC delay	^tRSD	80		80		ns	
$\overline{CAS}$ to first SC delay	^tCSD	30		30		ns	

NEW ■ MULTIPORT DRAM

SAM TIMING PARAMETERS

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes 6, 7, 8, 9, 10) (0° C ≤ T_A ≤ + 70°C; Vcc = 5V ±10%)

AC CHARACTERISTICS		-7		-8			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Serial clock cycle time	^tSC	25		30		ns	
Access time from SC	^tSAC		22		25	ns	24, 28
SC precharge time (SC LOW time)	^tSP	8		10		ns	
SC pulse width (SC HIGH time)	^tSAS	8		10		ns	
Access time from $\overline{SE}$	^tSEA		15		15	ns	24
$\overline{SE}$ precharge time	^tSEP	10		10		ns	
$\overline{SE}$ pulse width	^tSE	10		10		ns	
Serial data-out hold time after SC high	^tSOH	5		5		ns	24, 28
Serial output buffer turn-off delay from $\overline{SE}$	^tSEZ	3	12	3	12	ns	20, 24

NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. V_{CC} = 5V ±10%, f = 1 MHz.
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading. Specified values are obtained with minimum cycle time and the output open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is assured.
7. An initial pause of 100µs is required after power-up followed by any eight $\overline{RAS}$ cycles before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-up should be repeated any time the 8ms refresh requirement is exceeded.
8. AC characteristics assume ^tT = 5ns.
9. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}). Input signals transition from 0 to 3V for AC testing.
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS}$ = V_{IH}, DRAM data output (DQ1-DQ8) is High-Z.
12. If $\overline{CAS}$ = V_{IL}, DRAM data output (DQ1-DQ8) may contain data from the last valid READ cycle.
13. DRAM output timing measured with a load equivalent to 1 TTL gate and 50pF. Output reference levels: V_{OH} = 2.0V; V_{OL} = 0.8V.
14. Assumes that ^tRCD < ^tRCD (MAX). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
15. Assumes that ^tRCD ≥ ^tRCD (MAX).
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, DQ will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer, $\overline{CAS}$ must be pulsed HIGH for ^tCP.
17. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (MAX) limit, then access time is controlled exclusively by ^tCAC.
18. Operation within the ^tRAD (MAX) limit ensures that ^tRCD (MAX) can be met. ^tRAD (MAX) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (MAX) limit, then access time is controlled exclusively by ^tAA.
19. Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
20. ^tOD, ^tOFF and ^tSEZ define the time when the output achieves open circuit (V_{OH} -200mV, V_{OL} +200mV). This parameter is sampled and not 100% tested.
21. ^tWCS, ^tRWD, ^tAWD and ^tCWD are restrictive operating parameters in LATE-WRITE, READ-WRITE and READ-MODIFY-WRITE cycles only. If ^tWCS ≥ ^tWCS (MIN), the cycle is an EARLY-WRITE cycle and the data output will remain an open circuit throughout the entire cycle, regardless of $\overline{TR}/\overline{OE}$. If ^tWCS ≤ ^tWCS (MIN), the cycle is a LATE-WRITE and $\overline{TR}/\overline{OE}$ must control the output buffers during the write to avoid data contention. If ^tRWD ≥ ^tRWD (MIN), ^tAWD ≥ ^tAWD (MIN) and ^tCWD ≥ ^tCWD (MIN), the cycle is a READ-WRITE, and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of the output buffers (at access time and until $\overline{CAS}$ goes back to V_{IH}) is indeterminate but the WRITE will be valid, if ^tOD and ^tOEH are met. See the LATE-WRITE AC Timing diagram.
22. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY-WRITE cycles and $\overline{ME}/\overline{WE}$ leading edge in LATE-WRITE or READ-WRITE cycles.
23. During a READ cycle, if $\overline{TR}/\overline{OE}$ is LOW then taken HIGH, DQ goes open. The DQs will go open with $\overline{OE}$ or $\overline{CAS}$, whichever goes HIGH first.
24. SAM output timing is measured with a load equivalent to 1 TTL gate and 30pF. Output reference levels: V_{OH} = 2.0V; V_{OL} = 0.8V.
25. Address (A0-A8) may be changed two times or less while $\overline{RAS}$ = V_{IL}.
26. Address (A0-A8) may be changed once or less while $\overline{CAS}$ = V_{IH} and $\overline{RAS}$ = V_{IL}.
27. LATE-WRITE and READ-MODIFY-WRITE cycles must have ^tOD and ^tOEH met ($\overline{OE}$ HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. The DQs will provide previously read data if $\overline{CAS}$ remains LOW and $\overline{OE}$ is taken LOW after ^tOEH is met. If $\overline{CAS}$ goes HIGH prior to $\overline{OE}$ going back LOW, the DQs will remain open.
28. ^tSAC is MAX at 70° C and 4.5V Vcc; ^tSOH is MIN at 0°C and 5.5V Vcc. These limits will not occur simultaneously at any given voltage or temperature. (^tSOH = ^tSAC - output transition time); this is guaranteed by design.

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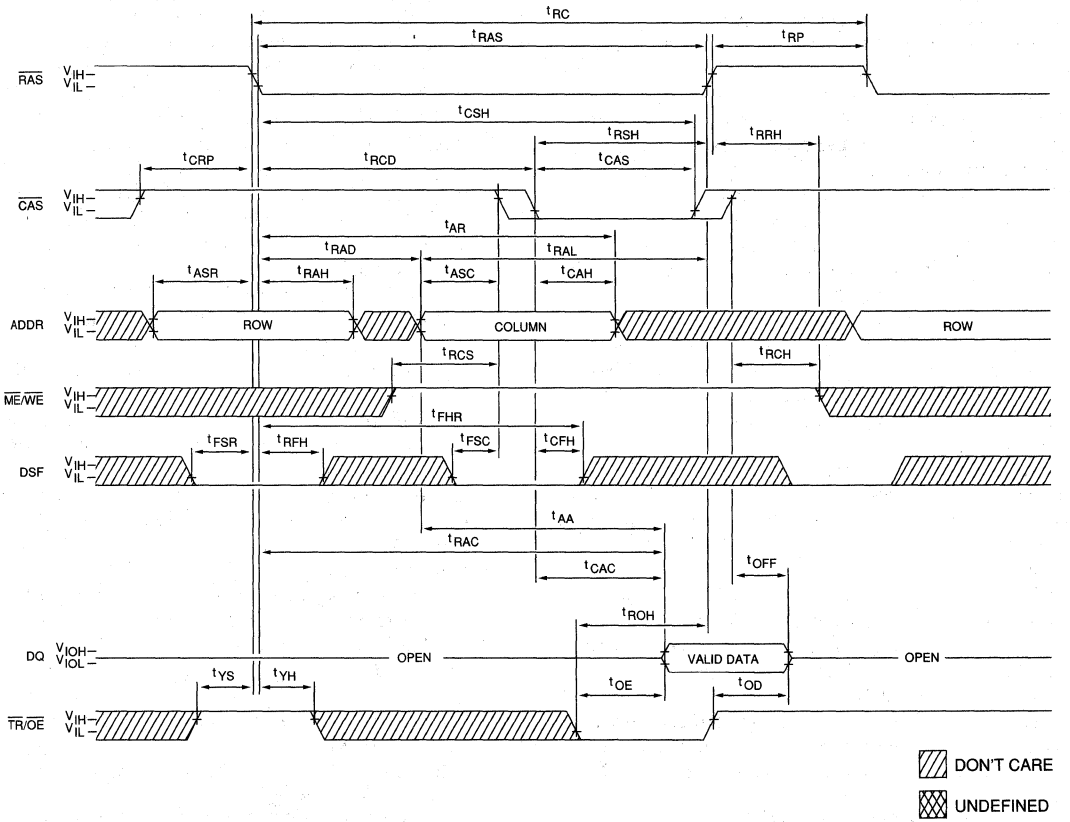
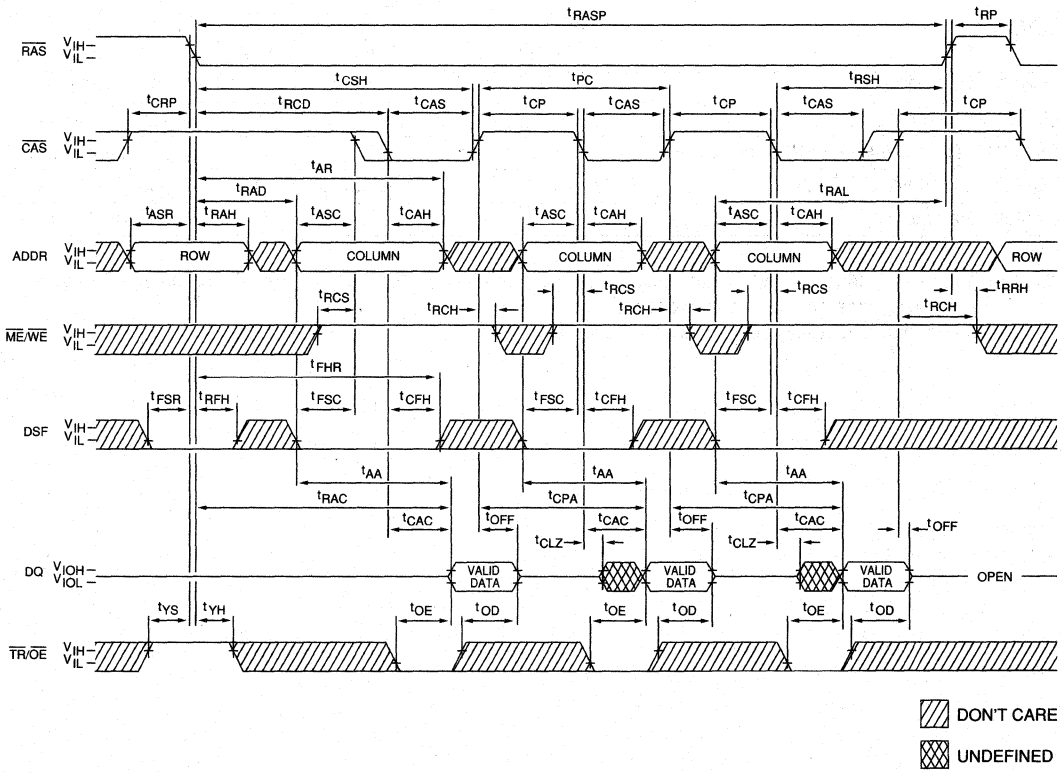
DRAM READ CYCLE



DRAM FAST-PAGE-MODE READ CYCLE



NOTE: WRITE cycles or READ-MODIFY-WRITE cycles may be mixed with READ cycles while in FAST PAGE MODE.

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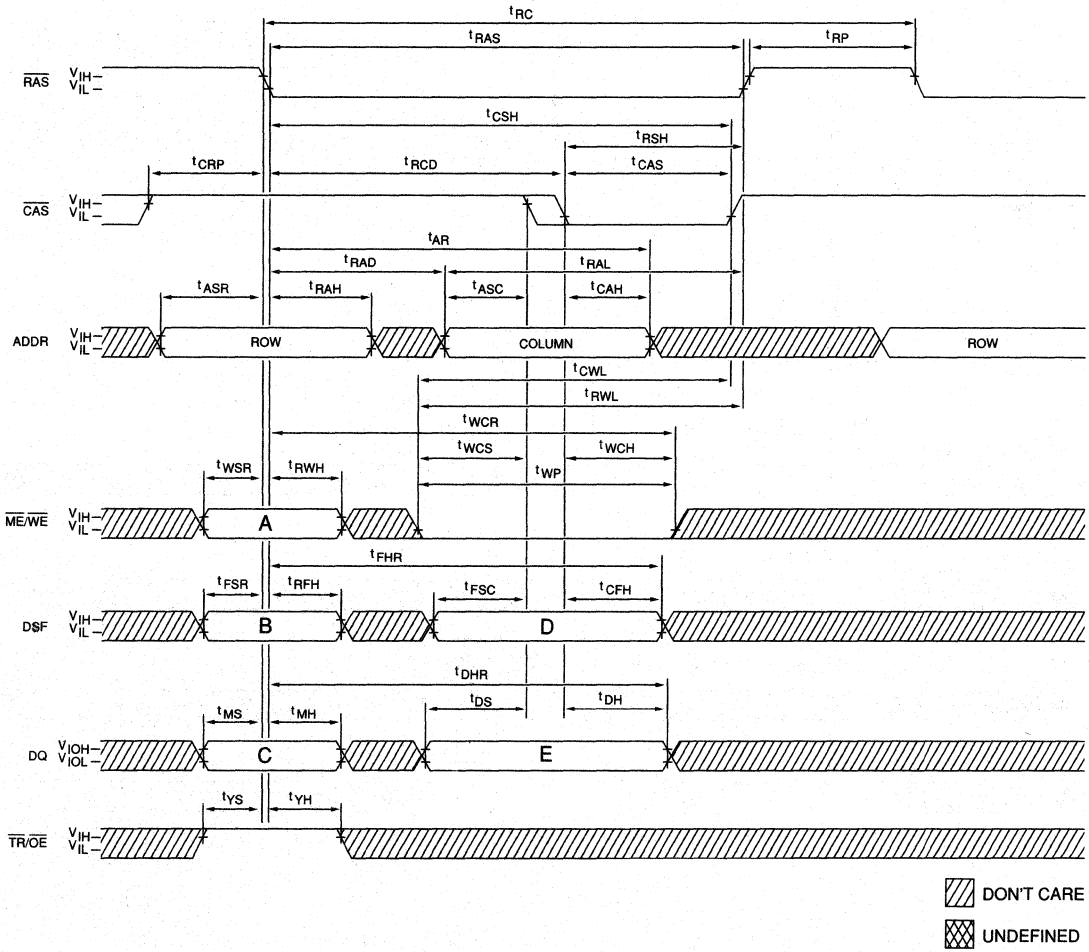
WRITE CYCLE FUNCTION TABLE [1]

FUNCTION	LOGIC STATES				
	$\overline{RAS}$ Falling Edge			$\overline{CAS}$ Falling Edge	
	A $\overline{ME}/\overline{WE}$	B DSF	C DQ (Input)	D DSF	E[2] DQ (Input)
Normal DRAM WRITE	1	0	X	0	DRAM Data
MASKED WRITE to DRAM	0	0	Write Mask	0	DRAM Data (Masked)
BLOCK WRITE to DRAM (No Bit-Plane Mask)	1	0	X	1	Column Mask
MASKED BLOCK WRITE to DRAM	0	0	Write Mask	1	Column Mask
Load Color Register	1	1	X	1	Color Data

NOTE: 1. Refer to this function table to determine the logic states of "A", "B", "C", "D" and "E" for the WRITE cycle timing diagrams on the following pages.
2. $\overline{CAS}$ or $\overline{ME}/\overline{WE}$ falling edge, whichever occurs later.

DRAM EARLY-WRITE CYCLE [1]



NOTE: 1. The logic states of "A", "B", "C", "D" and "E" determine the type of WRITE operation performed. See the Write Cycle Function Table for a detailed description.

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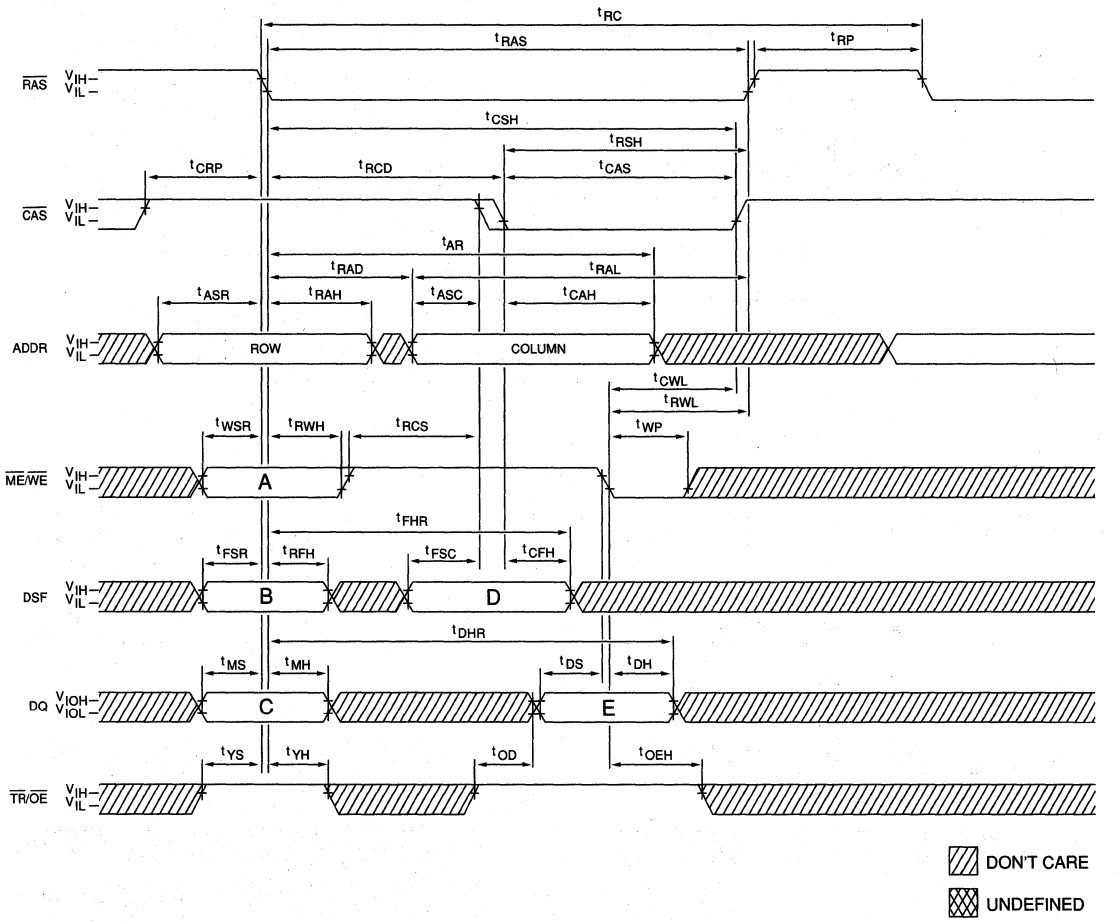
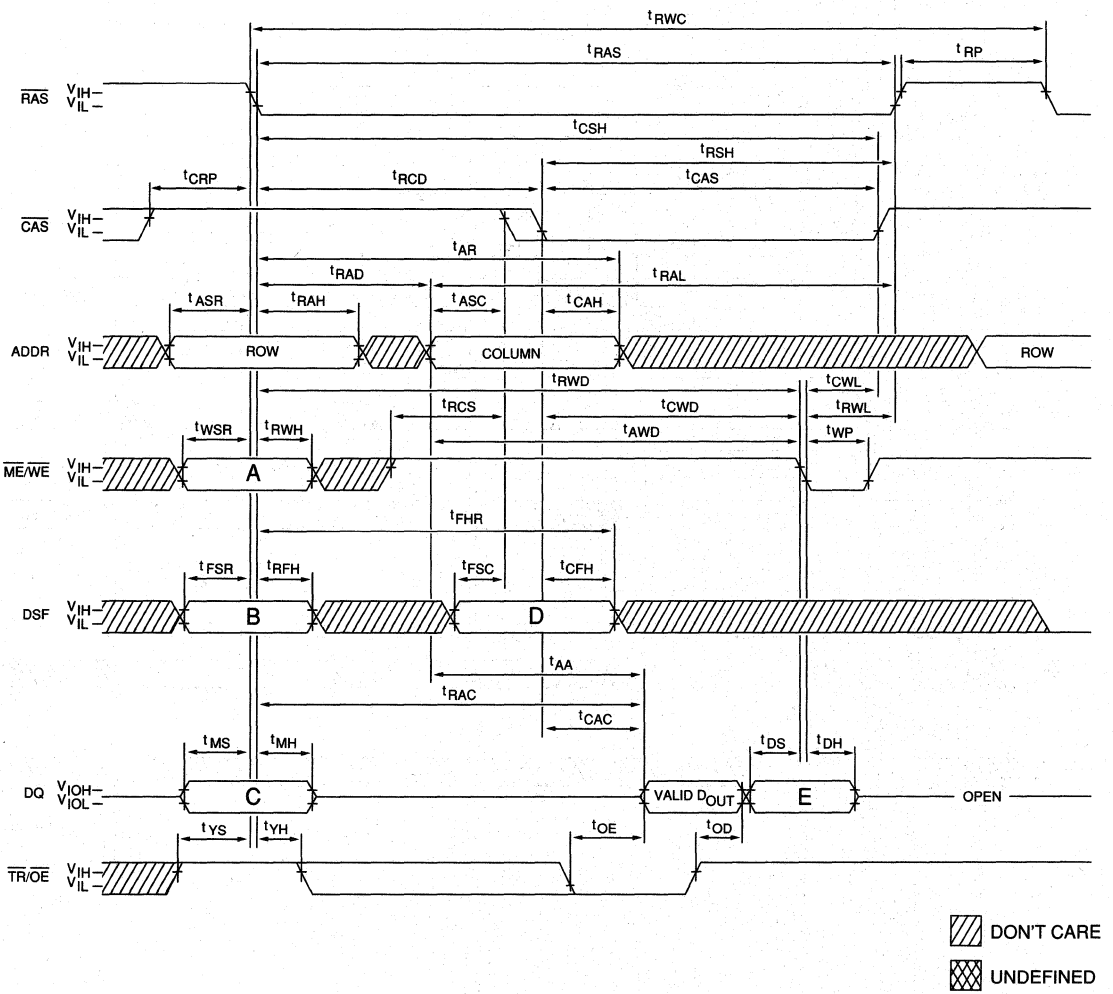
DRAM LATE-WRITE CYCLE



NOTE: The logic states of "A", "B", "C", "D" and "E" determine the type of WRITE operation performed. See the Write Cycle Function Table for a detailed description.

DRAM READ-WRITE CYCLE
(READ-MODIFY-WRITE CYCLE)



NOTE: The logic states of "A", "B", "C", "D" and "E" determine the type of WRITE operation performed. See the Write Cycle Function Table for a detailed description.

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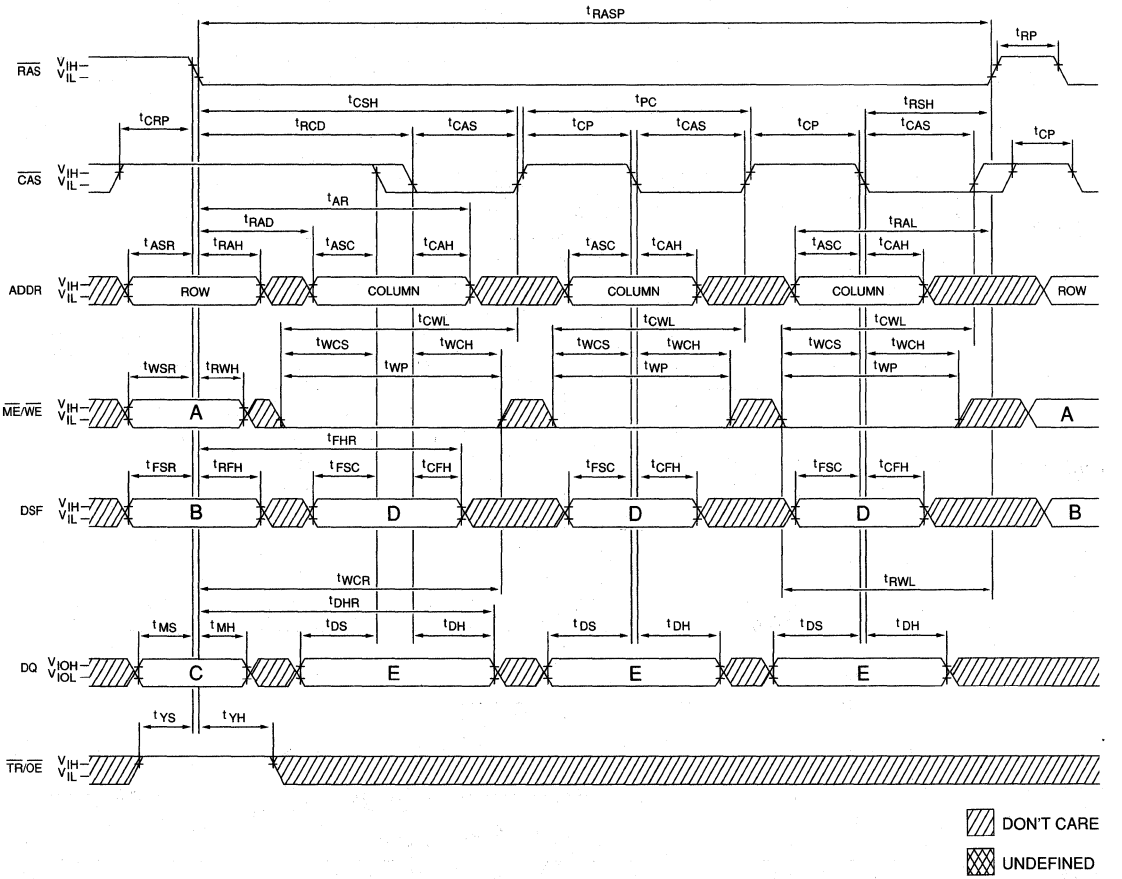
DRAM FAST-PAGE-MODE EARLY-WRITE CYCLE



NOTE: 1. READ cycles or READ-MODIFY-WRITE cycles can be mixed with WRITE cycles while in FAST PAGE MODE.

2. The logic states of "A", "B", "C", "D" and "E" determine the type of WRITE operation performed. See the Write Cycle Function Table for a detailed description.

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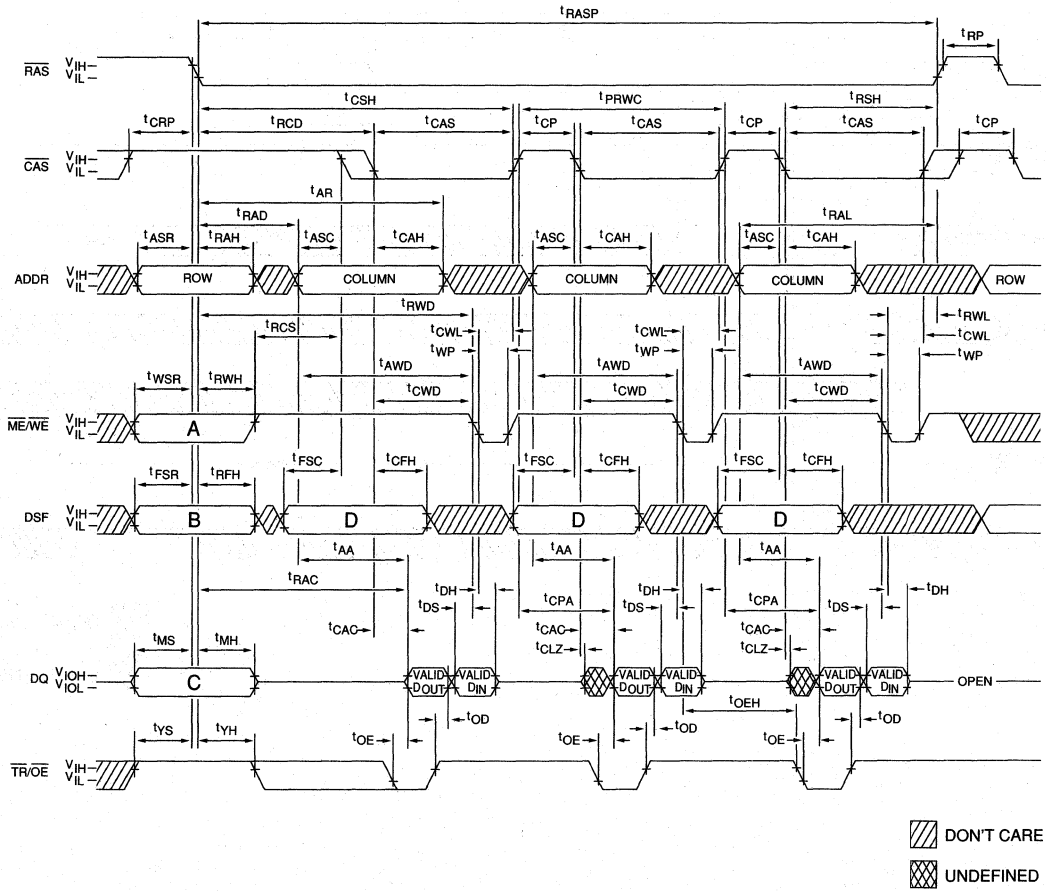
DRAM FAST-PAGE-MODE READ-WRITE CYCLE
(READ-MODIFY-WRITE OR LATE-WRITE CYCLES)



NOTE:
1. READ or WRITE cycles can be mixed with READ-MODIFY-WRITE cycles while in FAST PAGE MODE. Use the Write Function Table to determine the proper DSF state for the desired WRITE operation.
2. The logic states of "A", "B" , "C" and "D" determine the type of WRITE operation performed. See the Write Cycle Function Table for a detailed description.

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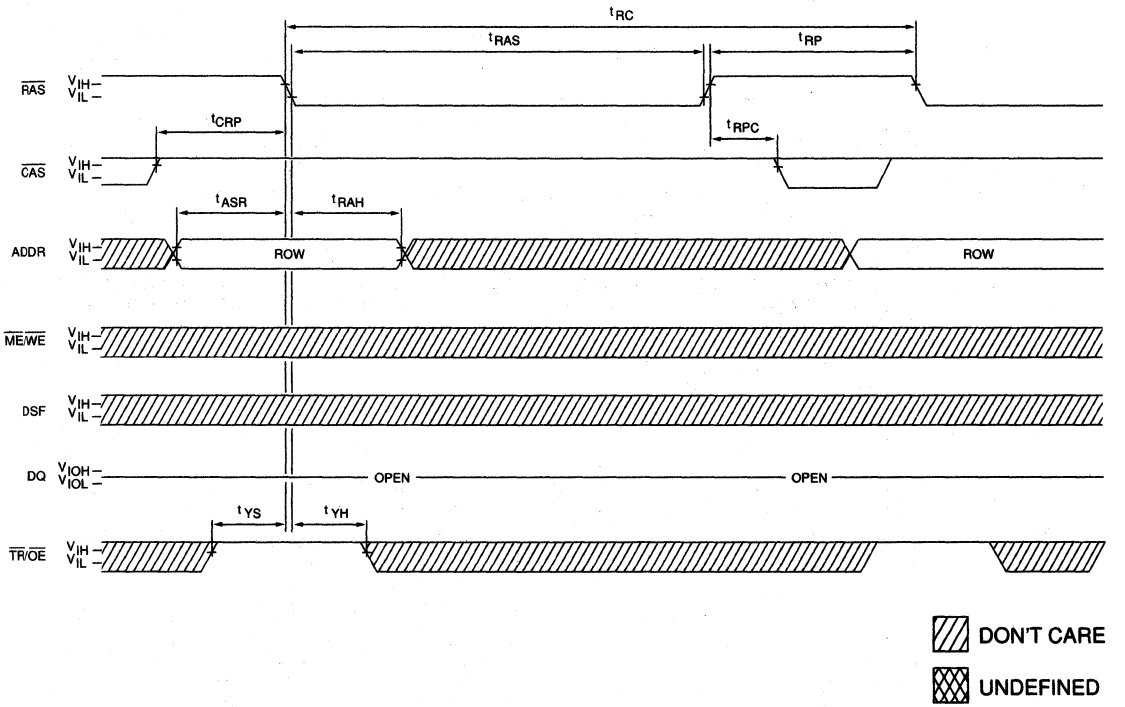
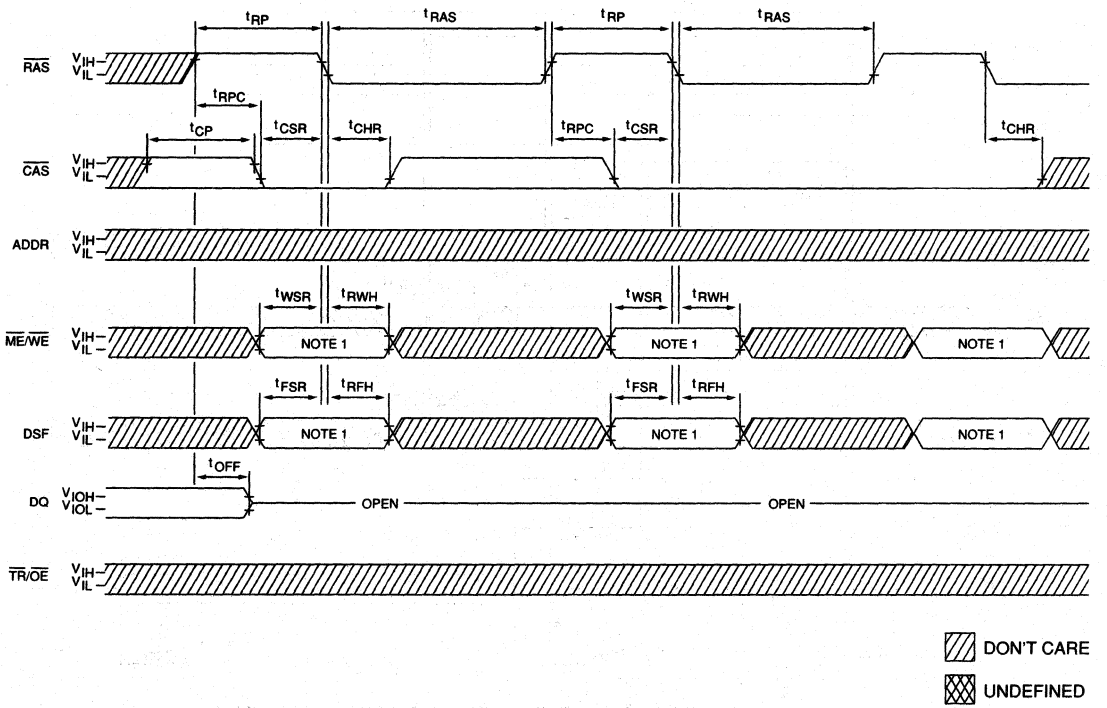
DRAM $\overline{RAS}$-ONLY REFRESH CYCLE
(ADDR = A0-A8)



CAS-BEFORE-RAS REFRESH CYCLE



OTE: 1. The MT42C8255 operates with ME/WE and DSF = "don't care," but to ensure compatibility with all 2 Meg VRAM feature sets, it is recommended that they be HIGH ("1").

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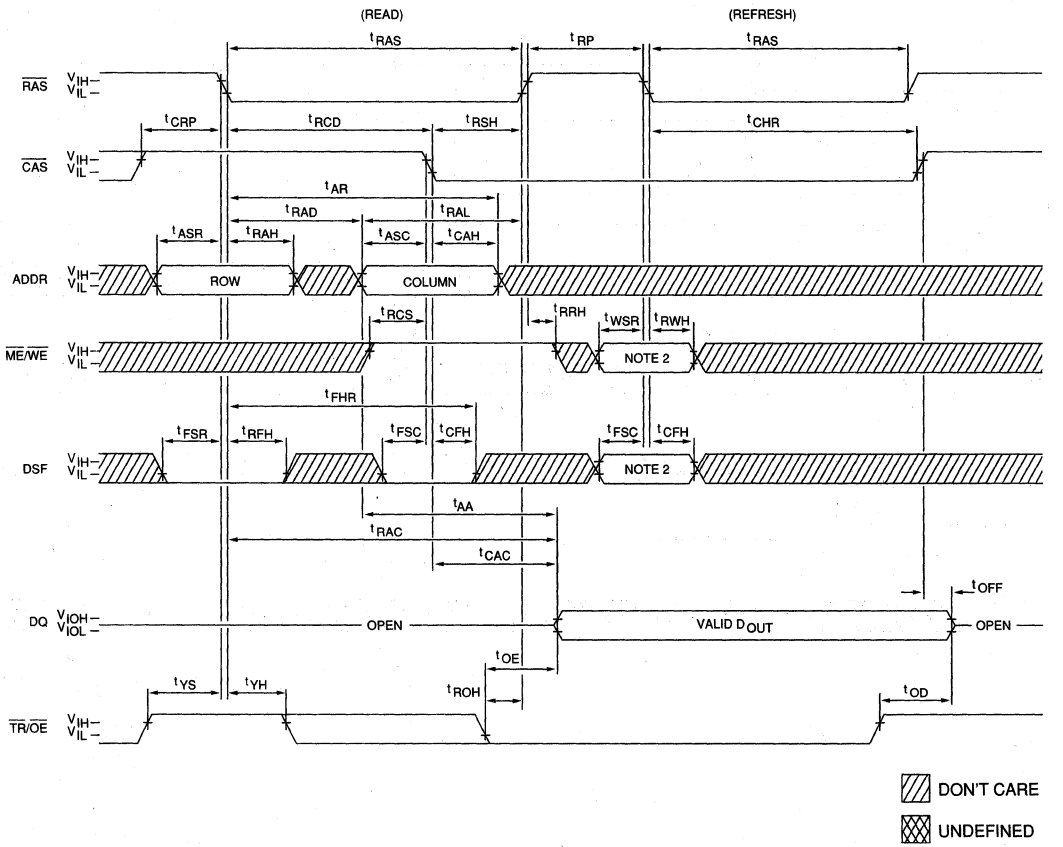
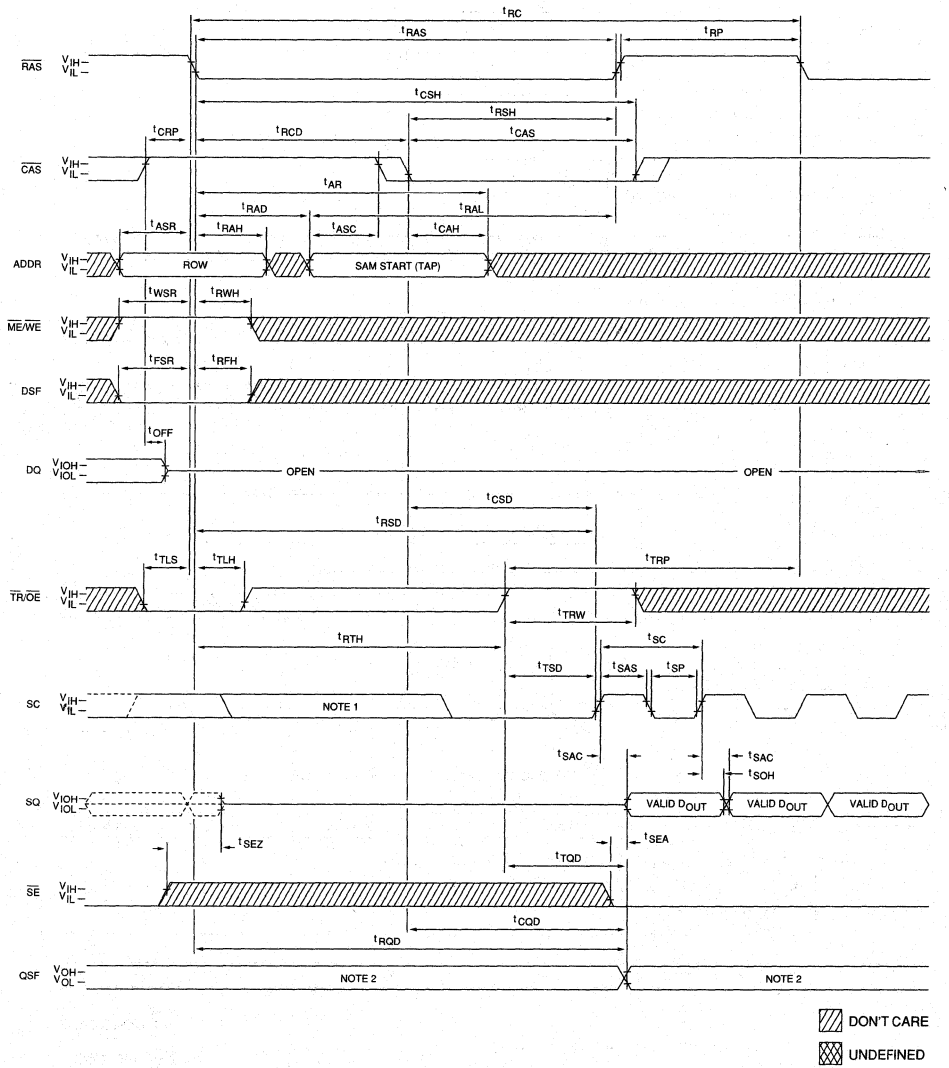
DRAM HIDDEN-REFRESH CYCLE



NOTE: 1. A HIDDEN REFRESH may also be performed after a WRITE or TRANSFER cycle. In this case, $\overline{ME}/\overline{WE}$ = LOW (when $\overline{CAS}$ goes LOW) and $\overline{TR}/\overline{OE}$ = HIGH. In the TRANSFER case, $\overline{TR}/\overline{OE}$ = LOW (when $\overline{RAS}$ goes LOW) and the DQ pins stay High-Z during the refresh period, regardless of $\overline{TR}/\overline{OE}$.

2. The MT42C8255 operates with $\overline{ME}/\overline{WE}$ and DSF = "don't care", but to ensure compatibility with all 2 Meg VRAM feature sets, it is recommended that they be HIGH ("1").

READ TRANSFER [3]
(DRAM-TO-SAM TRANSFER)
(When serial part was previously High-Z or SC idle)



IOTE:
1. There must be no rising edges on the SC input during this time period.
2. QSF = 0 when the Lower SAM (bits 0–255) is being accessed.
   QSF = 1 when the Upper SAM (bits 256–511) is being accessed.
3. If tTLH is timing for the $\overline{TR}/(\overline{OE})$ rising edge, the transfer is self-timed and the tCSD and tRSD times must be met. If tRTH is timing for the $\overline{TR}/(\overline{OE})$ rising edge, the transfer is done off of the $\overline{TR}/(\overline{OE})$ rising edge and tTSD must be met.

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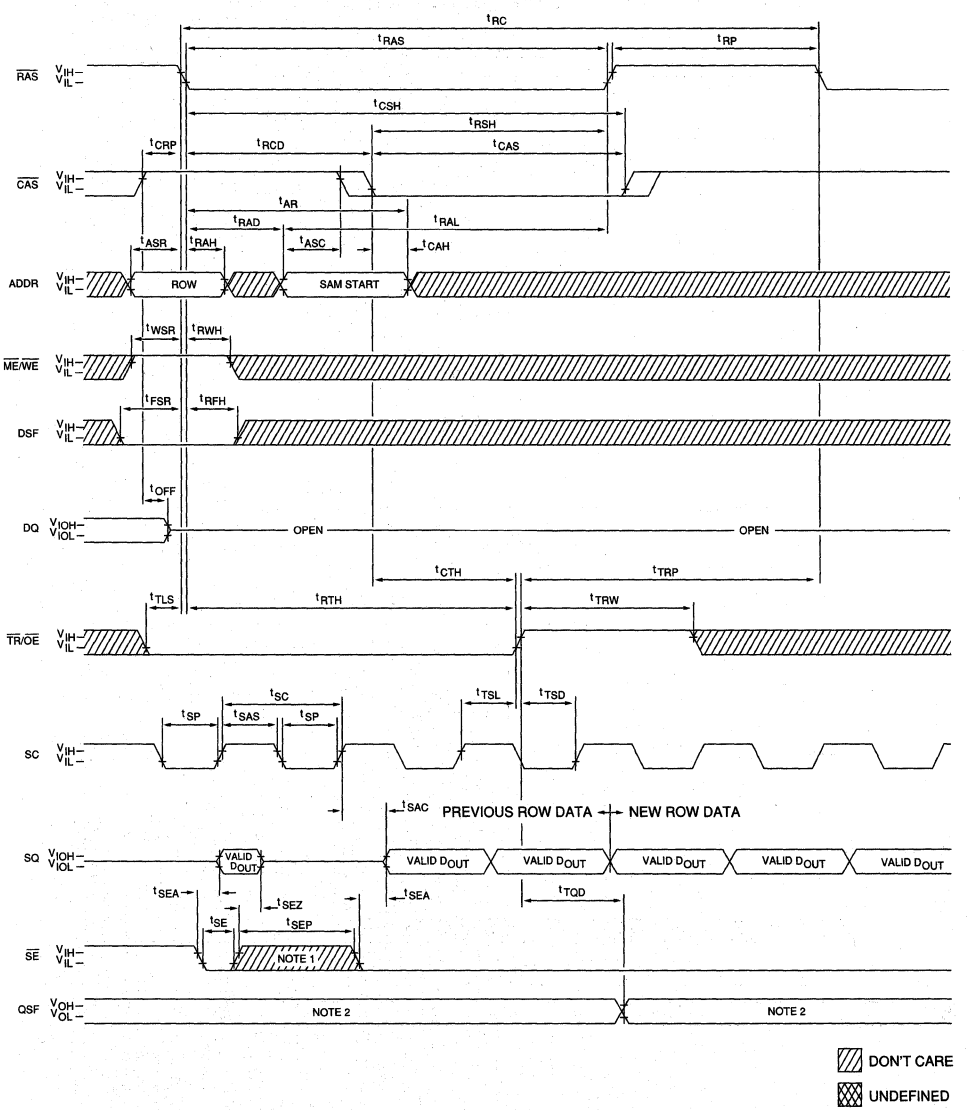
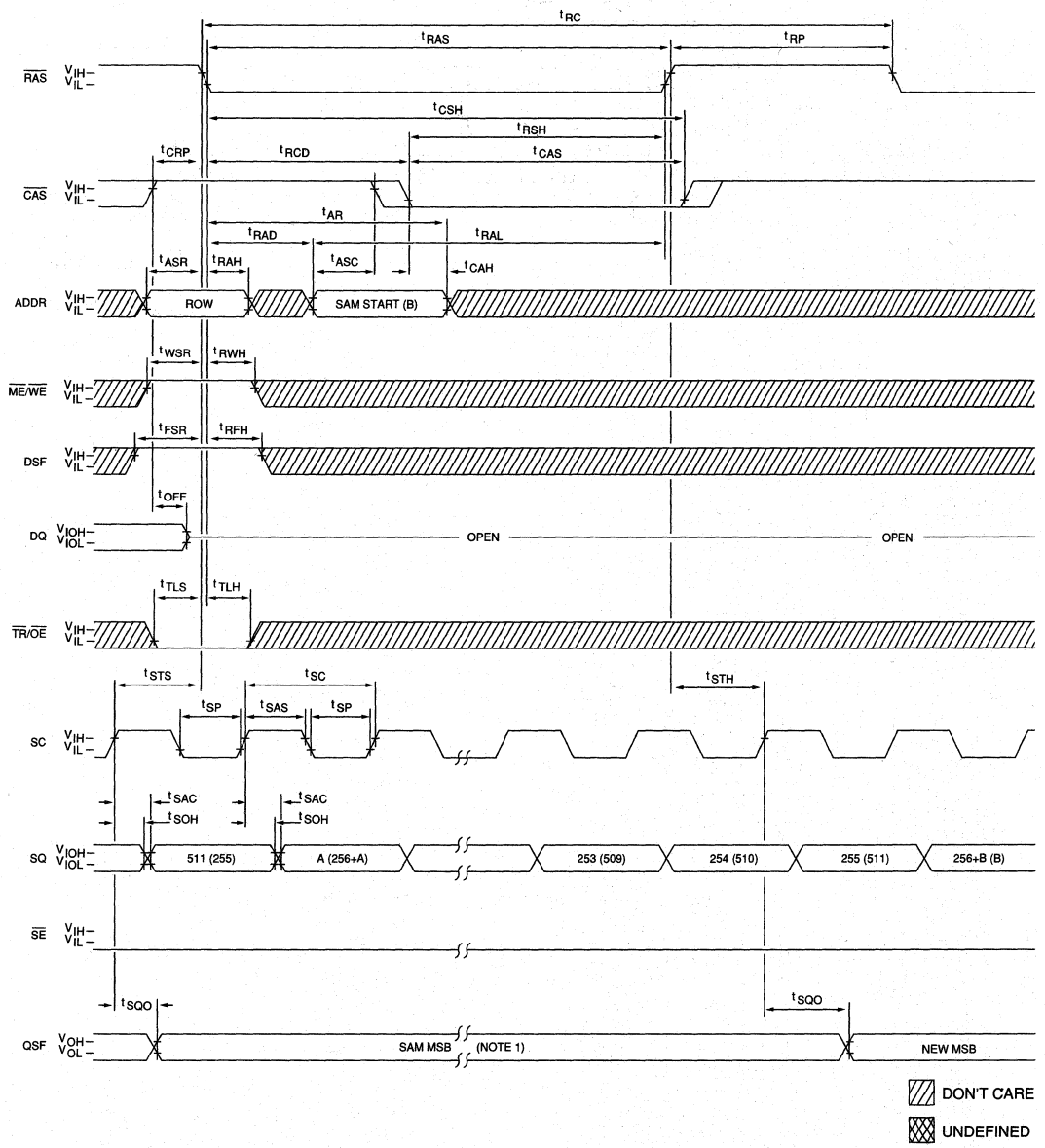
REAL-TIME READ TRANSFER (DRAM-TO-SAM TRANSFER)



NOTE: 1. The $\overline{SE}$ pulse is shown to illustrate the SERIAL OUTPUT ENABLE and DISABLE timing. It is not required.
2. QSF = 0 when the Lower SAM (bits 0–255) is being accessed.
QSF = 1 when the Upper SAM (bits 256–511) is being accessed.

SPLIT READ TRANSFER
(SPLIT DRAM-TO-SAM TRANSFER)



NOTE: 1. QSF = 0 when the Lower SAM (bits 0–255) is being accessed.
QSF = 1 when the Upper SAM (bits 256–511) is being accessed.

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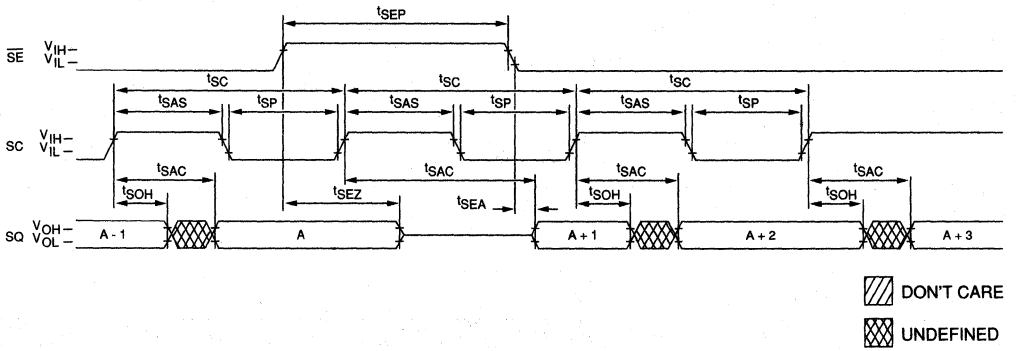
SAM SERIAL OUTPUT



VRAM

256K x 8 DRAM WITH 512 x 8 SAM

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FEATURES

- Industry standard pinout, timing, and functions
- High-performance, CMOS silicon-gate process
- Single +5V ±10% power supply
- Inputs and outputs are fully TTL and CMOS compatible
- Refresh modes: $\overline{\text{RAS}}$ ONLY, $\overline{\text{CAS}}$-BEFORE-$\overline{\text{RAS}}$ (CBR) and HIDDEN
- 512-cycle refresh within 8ms
- FAST PAGE MODE access with Extended Data Out
- Dual port organization: 256K x 8 DRAM port
  512 x 8 SAM port
- No refresh required for serial access memory
- Low power: 10mW standby; 300mW active, typical
- Fast access times – 70ns random, 15ns serial

SPECIAL FUNCTIONS

- JEDEC Standard Mandatory Function set
- PERSISTENT MASKED WRITE
- MASKED WRITE TRANSFER/SERIAL INPUT
- MASKED SPLIT WRITE TRANSFER
- BLOCK WRITE (MASK)
- MASKED FLASH WRITE
- PROGRAMMABLE SPLIT SAM

OPTIONS — MARKING

- Timing [DRAM, SAM (cycle/access)]
  70ns, 18/15ns — -7
  80ns, 25/20ns — -8
- Packages
  Plastic SOJ (400 mil) — DJ
  Plastic TSOP (400 mil) — TG
  Plastic TSOP (400 mil) reverse pinout — RG

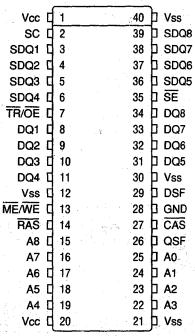
GENERAL DESCRIPTION

The MT42C8256 is a high speed, dual port CMOS dynamic random access memory, or video RAM (VRAM) containing 2,097,152 bits. These bits may be accessed by an 8-bit wide DRAM port or by a 512 x 8 bit serial access memory (SAM) port. Data may be transferred bidirectionally between the DRAM and the SAM.

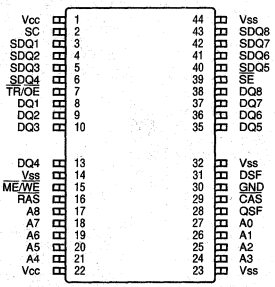
The DRAM portion of the VRAM is functionally identical to the MT4C4256 (256K x 4-bit DRAM), with the addition of MASKED WRITE, BLOCK WRITE and FLASH WRITE. Eight 512-bit data registers make up the serial access memory portion of the VRAM. Data I/O and internal data

PIN ASSIGNMENT (Top View)

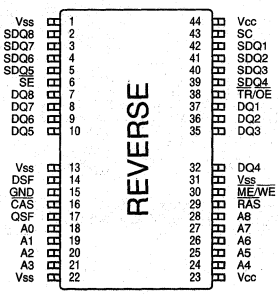
40-Pin SOJ (Q-6)



40/44-Pin TSOP (R-5)



40/44-Pin TSOP* (R-5)



*Consult factory for availability.

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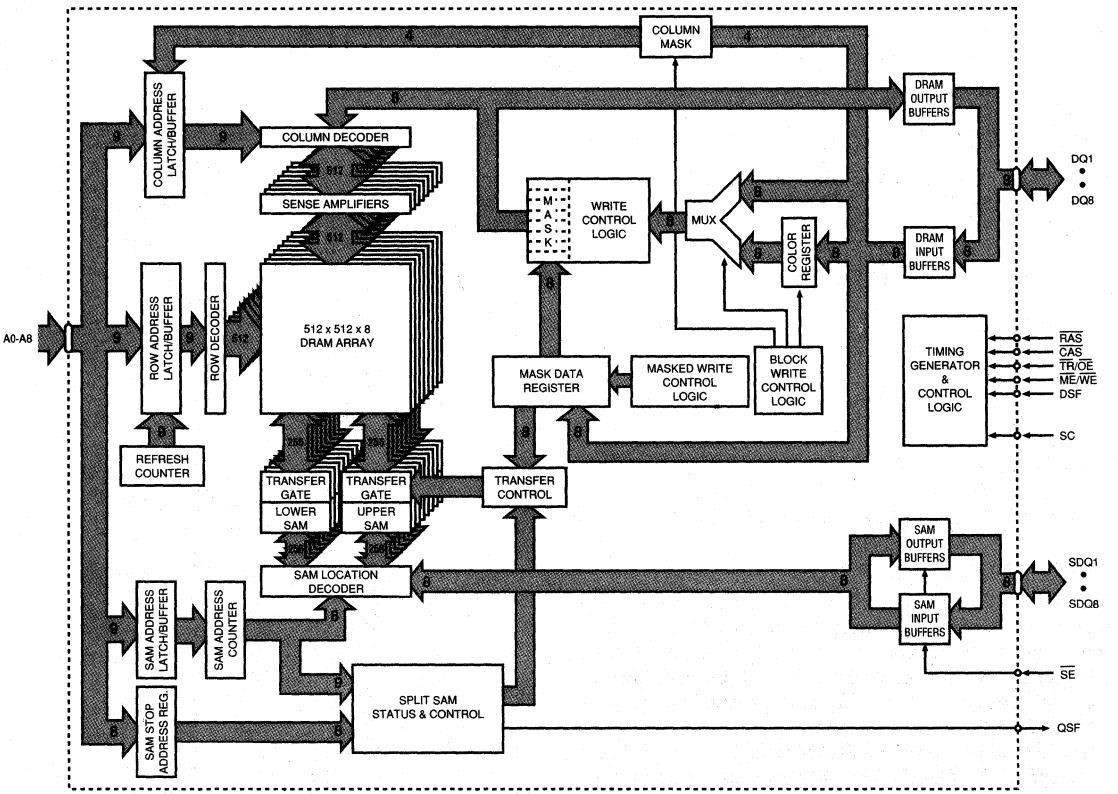
transfer are accomplished using three separate bidirectional data paths: the 8-bit random access I/O port, the eight internal 512 bit wide paths between the DRAM and the SAM, and the 8-bit serial I/O port for the SAM. The rest of the circuitry consists of the control, timing, and address decoding logic.

Each port may be operated asynchronously and independently of the other except when data is being transferred internally. As with all DRAMs, the VRAM must be refreshed to maintain data. The refresh cycles must be timed so that all 512 combinations of $\overline{RAS}$ addresses are executed at least every 8ms (regardless of sequence). Micron recommends evenly spaced refresh cycles for maximum data integrity. An internal transfer between the DRAM and the SAM counts as a refresh cycle. The SAM portion of the VRAM is fully static and does not require any refresh.

The operation and control of the MT42C8256 are optimized for high performance graphics and communication designs. The dual port architecture is well suited to buffering the sequential data types used in raster graphics display, serial, parallel networking and data communications. Special features such as SPLIT TRANSFERs, Extended Data Out and BLOCK WRITE allow further enhancements to system performance.

FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTIONS

SOJ PIN NUMBERS	TSOP(TG) PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
2	2	SC	Input	Serial Clock: Clock input to the serial address counter and data latch for the SAM registers.
7	7	$\overline{TR}/\overline{OE}$	Input	Transfer Enable: Enables an internal TRANSFER operation at $\overline{RAS}$ (H → L), or Output Enable: Enables the DRAM output buffers when taken LOW after $\overline{RAS}$ goes LOW ($\overline{CAS}$ must also be LOW), otherwise the output buffers are in a High-Z state.
13	15	$\overline{ME}/\overline{WE}$	Input	Mask Enable: If $\overline{ME}/\overline{WE}$ is LOW at the falling edge of $\overline{RAS}$, a MASKED WRITE cycle is performed, or Write Enable: $\overline{ME}/\overline{WE}$ is also used to select a READ ($\overline{ME}/\overline{WE}$ = H) or WRITE ($\overline{ME}/\overline{WE}$ = L) cycle when accessing the DRAM. This includes a READ TRANSFER ($\overline{ME}/\overline{WE}$ = H) or WRITE TRANSFER ($\overline{ME}/\overline{WE}$ = L).
35	39	$\overline{SE}$	Input	Serial Port Enable: $\overline{SE}$ enables the serial I/O buffers and allows a serial READ or WRITE operation to occur, otherwise the output buffers are in a High-Z state. The SAM address count will be incremented by the rising edge of SC when $\overline{SE}$ is inactive (HIGH).
29	31	DSF	Input	Special Function Select: DSF is used to indicate which special functions (BLOCK WRITE, FLASH WRITE, SPLIT TRANSFER, etc.) are used for a particular access cycle (see Truth Table).
14	16	$\overline{RAS}$	Input	Row Address Strobe: $\overline{RAS}$ is used to clock in the 9 row-address bits and strobe for $\overline{ME}/\overline{WE}$, $\overline{TR}/\overline{OE}$, DSF, $\overline{SE}$, $\overline{CAS}$ and DQ inputs. It also acts as the master chip enable, and must fall for initiation of any DRAM or TRANSFER cycles.
27	29	$\overline{CAS}$	Input	Column Address Strobe: $\overline{CAS}$ is used to clock in the 9 column-address bits and as a strobe for the DSF input (BLOCK WRITE only).
25, 24, 23, 22, 19, 18, 17, 16, 15	27, 26, 25, 24, 21, 20, 19, 18, 17	A0-A8	Input	Address Inputs: For the DRAM operation, these inputs are multiplexed and clocked by $\overline{RAS}$ and $\overline{CAS}$ to select one 8-bit word out of the 262,144 available. During TRANSFER operations, A0 to A8 indicate the DRAM row being accessed (when $\overline{RAS}$ goes LOW) and A0-A8 indicate the SAM start address (when $\overline{CAS}$ goes LOW). A8 = "don't care" for the start address during SPLIT TRANSFERs.
8, 9, 10, 11, 31, 32, 33, 34	8, 9, 10, 13, 35, 36, 37, 38	DQ1-DQ8	Input/ Output	DRAM Data I/O: Data input/output for DRAM access cycles: These pins also act as inputs for Mask and Color Register load cycles, DQ Mask and Column Mask for BLOCK WRITE.
3, 4, 5, 6, 36, 37, 38, 39	3, 4, 5, 6, 40, 41, 42, 43	SDQ1-SDQ8	Input/ Output	Serial Data I/O: Input, output, or High-Z.
26	28	QSF	Output	Split SAM Status: QSF indicates which half of the SAM is being accessed. LOW if address is 0-255, HIGH if address is 256-511.
28	30	GND	–	No Connect/GND: This pin must be tied to ground to allow for upward functional compatibility with future VRAM feature sets.
1, 20	1, 22	Vcc	Supply	Power Supply: +5V ±10%
12, 21, 30, 40	14, 23, 32, 44	Vss	Supply	Ground

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FUNCTIONAL DESCRIPTION

The MT42C8256 can be divided into three functional blocks (see Figure 1): the DRAM, the transfer circuitry, and the SAM. All of the operations described below are shown in the AC Timing Diagrams section of this data sheet and summarized in the Truth Table.

Note: *For dual-function pins, the function not being discussed will be surrounded by parentheses. For example, the TR/OE pin will be shown as TR/(OE) in references to transfer operations,*

DRAM OPERATION

DRAM REFRESH

Like any DRAM based memory, the MT42C8256 VRAM must be refreshed to retain data. All 512 row address combinations must be accessed within 8ms. The MT42C8256 supports CAS-BEFORE-RAS, RAS ONLY and HIDDEN types of refresh cycles.

For the CAS-BEFORE-RAS REFRESH (CBR) cycle, the row addresses are generated and stored in an internal address counter. The user need not supply any address data, and simply must perform 512 CAS-BEFORE-RAS cycles within the 8ms time period. CBR cycles are also used to reset MASKED WRITE and PROGRAMMABLE SPLIT SAM operating modes. There are three CBR cycles defined for the MT42C8256; CBR No Reset (CBRN), CBR Reset Stop Address (CBRS), and CBR Reset All Options (CBRR). To perform these functions, two additional pins are defined for CBR cycles, ME/WE and DSF1. These operations are described in detail in the MASKED WRITE and SPLIT READ/WRITE TRANSFER sections of the functional description.

The refresh address must be generated externally and applied to A0-A8 inputs for RAS-ONLY REFRESH cycles. The DQ pins remain in a High-Z state for both the RAS-ONLY and CAS-BEFORE-RAS cycles.

HIDDEN REFRESH cycles are performed by toggling RAS (and keeping CAS LOW) after a READ or WRITE cycle. This performs CAS-BEFORE-RAS cycles but does not disturb the DQ lines.

Any DRAM READ, WRITE, or TRANSFER cycle also refreshes the DRAM row being accessed. The SAM portion of the MT42C8256 is fully static and does not require any refreshing.

DRAM ACCESS CYCLES (RW)

The DRAM portion of the VRAM is nearly identical to standard 256K x 4 DRAMs. However, because several of the DRAM control pins are used for additional functions on this part, several conditions that were undefined or in "don't care" states for the DRAM are specified for the VRAM. These conditions are highlighted in the following discussion. In addition, the VRAM has special functions that can be used when writing to the DRAM.

The 18 address bits that are used to select an 8-bit word from the 262,144 available are latched into the chip using the A0-A8, RAS and CAS inputs. First, the nine row-address bits are set up on the address inputs and clocked into the part when RAS transitions from HIGH-to-LOW. Next, the 9 column address bits are set up on the address inputs and clocked-in when CAS goes from HIGH-to-LOW.

Note: *RAS also acts as a "master" chip enable for the VRAM. If RAS is inactive, HIGH, all other DRAM control pins (CAS, TR/OE, ME/WE, etc.) are a "don't care" and may change state without effect. No DRAM or TRANSFER cycles will be initiated without RAS falling.*

For single port DRAMS, the OE pin is a "don't care" when RAS goes LOW. However, for the VRAM, when RAS goes LOW, TR/(OE) selects between DRAM access or TRANSFER cycles. TR/(OE) must be HIGH at the RAS HIGH-to-LOW transition for all DRAM operations (except CAS-BEFORE-RAS).

A DRAM READ operation is performed if (ME)/WE is HIGH when CAS goes LOW and remains HIGH until CAS goes HIGH. The data from the memory cells selected will appear at the DQ1-DQ8 port. The (TR)/OE input must transition from HIGH-to-LOW some time after RAS falls to enable the DRAM output port.

For single port DRAMs, WE is a "don't care" when RAS goes LOW. For the VRAM, ME/WE performs two functions; write mask enable and data write enable. ME/(WE) is used, when RAS goes LOW, to select between a MASKED WRITE cycle and a normal WRITE cycle. If ME/(WE) is LOW at the RAS HIGH-to-LOW transition, a MASKED WRITE operation is selected. For any non-masked DRAM access cycle (READ or WRITE), ME/(WE) must be HIGH at the RAS HIGH-to-LOW transition. If (ME)/WE is LOW before CAS goes LOW, a DRAM EARLY-WRITE operation is performed and the data present on the DQ1-DQ8 data port will be written into the selected memory cells. If (ME)/WE goes LOW after CAS goes LOW, a DRAM LATE-WRITE operation is performed (refer to the AC timing diagrams).

The VRAM can perform all the normal DRAM cycles including READ, EARLY-WRITE, LATE-WRITE, READ-MODIFY-WRITE, FAST-PAGE-MODE READ (with Extended Data Out), FAST-PAGE-MODE WRITE (Late or Early), and FAST-PAGE- MODE READ-MODIFY-WRITE. Refer to the AC timing parameters and diagrams in the data sheet for more details on these operations.

EXTENDED DATA OUTPUT

DRAM READ cycles have traditionally turned the output buffers off (High-Z) with the rising edge of $\overline{CAS}$. If $\overline{CAS}$ goes HIGH, and $\overline{OE}$ is LOW (active), the output buffers will be disabled. The MT42C8256 offers an accelerated FAST PAGE MODE (FPM) cycle by eliminating output disable from $\overline{CAS}$ HIGH. This option is called Extended Data Out, and it allows $\overline{CAS}$ precharge time (^tCP) to occur without the output data going invalid (see DRAM READ and DRAM FAST-PAGE-MODE READ waveforms).

Extended Data Out operates as any DRAM READ or FPM READ, except data will be held valid after $\overline{CAS}$ goes HIGH, as long as $\overline{RAS}$ is LOW. If the DQ outputs are wire OR'd, $\overline{TR}/\overline{OE}$ must be used to disable idle banks of VRAMs. During non-PAGE-MODE READ cycles, the outputs are disabled at ^tOFF time after $\overline{RAS}$ and $\overline{CAS}$ are HIGH. The ^tOFF time is referenced from the rising edge of $\overline{RAS}$ or $\overline{CAS}$, whichever occurs later.

MASKED WRITE (RWM)

The MASKED WRITE feature eliminates the need to do a READ-MODIFY-WRITE cycle when changing individual bits within the 8-bit word. The MT42C8256 supports two types of MASKED WRITE cycles, nonpersistent MASKED WRITE and persistent MASKED WRITE. When $\overline{ME}/(\overline{WE})$ and DSF are LOW at the $\overline{RAS}$ HIGH-to-LOW transition, a MASKED WRITE is performed.

The MT42C8256 initializes in the nonpersistent mode. In this mode, mask data must be entered with every $\overline{RAS}$ falling edge. The data (mask data) present on the DQ1-DQ8 inputs will be written into the mask data register (see Figure 1). The mask data acts as an individual write enable for each of the eight DQ1-DQ8 pins. If a LOW (logic "0") is written to a mask data register bit, the input port for that bit is disabled during the subsequent WRITE operation and no new data will be written to that DRAM cell location. A HIGH (logic "1") on a mask data register bit enables the input port and allows normal WRITE operation to proceed. Note that $\overline{CAS}$ is still HIGH. When $\overline{CAS}$ goes LOW, the bits present on the DQ1-DQ8 inputs will be either written to the DRAM (if the mask data bit is HIGH) or ignored (if the mask data bit is LOW). The DRAM contents that correspond to masked input bits will not be changed during the WRITE cycle. The mask data register is cleared at the end of every nonpersistent MASKED WRITE.

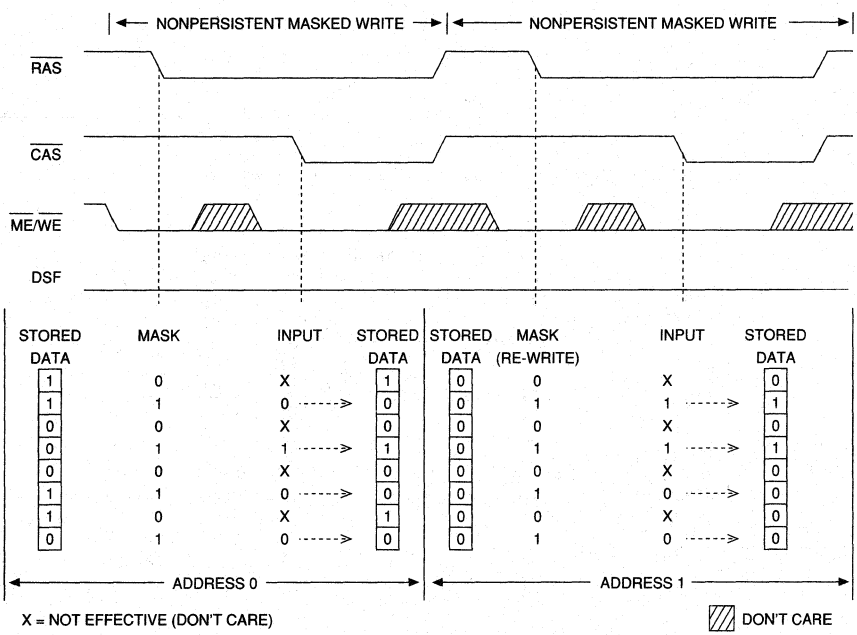


Figure 1
NONPERSISTENT MASKED WRITE EXAMPLE

The selection of persistent or nonpersistent MASKED WRITE is done by performing a LOAD MASK REGISTER (LMR) cycle (see LMR description). If an LMR is done, all ensuing MASKED WRITEs are persistent and the mask data will be provided by the Mask Data Register (see Figure 2). The mask data is applied in the same manner as in nonpersistent mode.

To reset the device back to the nonpersistent mode, a $\overline{CAS}$-BEFORE-$\overline{RAS}$, Reset All Options (CBRR) cycle must be performed. This cycle is defined as a CBR with DSF LOW when $\overline{RAS}$ falls, WE is "don't care." To preserve the persistent mode of MASKED WRITE, while using $\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH, a CBRN cycle is used. This cycle will perform a refresh of the internally addressed row of DRAM but will not reset the MASKED WRITE mode.

FAST PAGE MODE can be used with MASKED WRITE to write several column locations in an addressed row. The same mask is used during the entire FAST-PAGE-MODE $\overline{RAS}$ cycle.

BLOCK WRITE (BW)

If DSF is HIGH when $\overline{CAS}$ goes LOW, the MT42C8256 will perform a BLOCK WRITE cycle instead of a normal WRITE cycle. In BLOCK WRITE cycles, the contents of the color register are directly written to four adjacent column locations (see Figure 3). The color register must be loaded prior to beginning BLOCK WRITE cycles (see LOAD COLOR REGISTER).

The row is addressed as in a normal DRAM WRITE cycle. However when $\overline{CAS}$ goes LOW, only the A2-A8 inputs are used. A2-A8 specify the "block" of four adjacent column locations that will be accessed. The DQ inputs (DQ1, 2, 3, and 4) are then used to determine what combination of the four column locations will be changed. The DQ inputs are

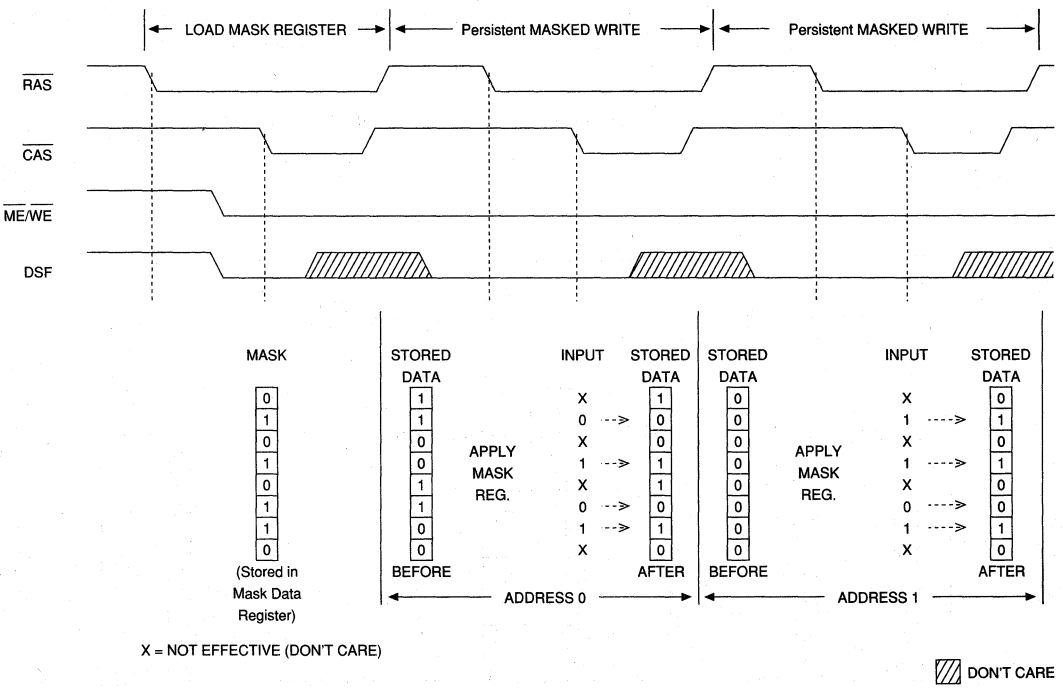


Figure 2
PERSISTENT MASKED WRITE EXAMPLE

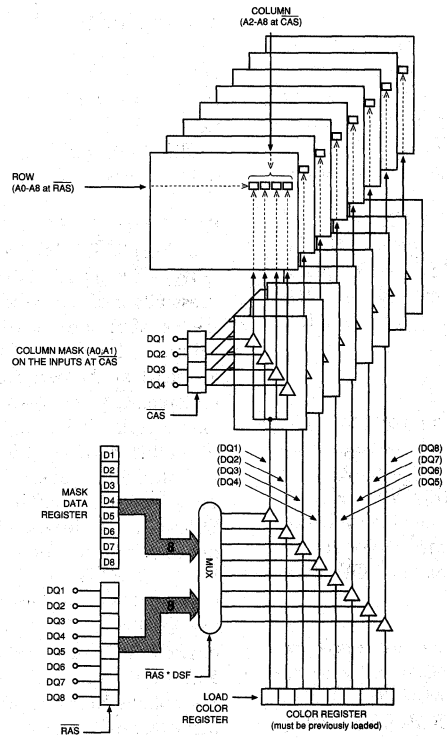


Figure 3
BLOCK WRITE EXAMPLE

"written" at the falling edge of $\overline{CAS}$ or $\overline{WE}$, whichever occurs later (see the WRITE cycle waveforms). The table on this page illustrates how each of the DQ inputs is used to selectively enable or disable individual column locations within the block. The write enable controls are active HIGH; a logic "1" enables the WRITE function and a logic "0" disables the WRITE function.

The contents of the color register will then be written to the column locations enabled. Each DQ location of the color register is written to the four column locations (or any of the four that are enabled) in the corresponding DQ bit plane.

MASKED BLOCK WRITE (BWM)

The MASKED WRITE functions may also be used during BLOCK WRITE cycles. MASKED BLOCK WRITE operates exactly like the normal MASKED WRITE except the mask is now applied to the 8 bit-planes of four column locations instead of just one column location.

The combination of $\overline{ME}$/($\overline{WE}$) LOW and DSF LOW when $\overline{RAS}$ goes LOW initiates a MASKED WRITE cycle. To perform a MASKED BLOCK WRITE, the DSF pin must be HIGH when $\overline{CAS}$ goes LOW. By using both the column mask input and the MASKED WRITE function of BW, any combination of the eight bit planes may be masked, along with any combination of the four column locations.

The MASKED BLOCK WRITE will be nonpersistent (new mask) at device power-up. To enter persistent mode (old mask) a LOAD MASK REGISTER cycle is performed. All MASKED BLOCK WRITEs will be persistent after the LMR. To reset to nonpersistent mode, a CBRR (reset all) cycle must be performed.

INPUTS	COLUMN ADDRESS CONTROLLED	
	A0	A1
DQ1	0	0
DQ2	1	0
DQ3	0	1
DQ4	1	1

NEW ■ MULTIPORT DRAM

MASKED FLASH WRITE (FWM)

The MASKED FLASH WRITE cycle is similar to the MASKED BLOCK WRITE cycle in that it uses the color register to accelerate the writing of a select color to the DRAM memory array. Instead of writing to four adjacent column locations in one DRAM cycle (BLOCK WRITE), FWM writes the contents of the color register to all column locations on an addressed row in one cycle.

The FWM cycle is selected by taking $\overline{TR}/(\overline{OE})$ and DSF HIGH and $\overline{ME}/(\overline{WE})$ LOW at the falling edge of $\overline{RAS}$. DSF is "don't care" at the falling edge of $\overline{CAS}$. The DQ plane mask applies as it does for all masked write cycles; if the mask register has been loaded, the mask is persistent; if it has not, the mask is nonpersistent.

LOAD MASK REGISTER (LMR)

The LOAD MASK REGISTER operation loads the data present on the DQ pins into the 8-bit Mask Data Register at the falling edge of $\overline{CAS}$ or $(\overline{ME})/\overline{WE}$. As shown in the Truth Table, the combination of $\overline{TR}/(\overline{OE})$, $(\overline{ME})/\overline{WE}$, and DSF being HIGH when $\overline{RAS}$ goes LOW indicates the cycle is a LOAD REGISTER cycle. DSF is used when $\overline{CAS}$ goes LOW to select the register to be loaded and must be LOW for a LOAD MASK REGISTER cycle.

Note: *LOAD MASK REGISTER cycles also enable the persistent MASKED WRITE mode. All ensuing MASKED WRITEs (including MASKED WRITE and MASKED SPLIT WRITE TRANSFER) will be masked with data from the mask register. A CBRR has to be done to reset back to nonpersistent mode.*

The row address supplied will be refreshed, but it is not necessary to provide any particular row address. The column address inputs are ignored during a LOAD MASK REGISTER cycle.

During persistent operation, the mask data register contents are used for MASKED WRITE, MASKED BLOCK WRITE, MASKED FLASH WRITE, and MASKED WRITE and SPLIT WRITE TRANSFER cycles to selectively enable writes to the eight DQ planes.

LOAD COLOR REGISTER (LCR)

A LOAD COLOR REGISTER cycle is identical to the LOAD MASK REGISTER cycle except DSF is HIGH when $\overline{CAS}$ goes LOW. The contents of the 8-bit color register are retained until changed by another LOAD COLOR REGISTER cycle (or the part loses power) and are used as data inputs during BLOCK WRITE and FLASH WRITE cycles.

TRANSFER OPERATIONS

TRANSFER operations are initiated when $\overline{TR}/(\overline{OE})$ is LOW at the falling edge of $\overline{RAS}$. The state of $(\overline{ME})/\overline{WE}$ when $\overline{RAS}$ goes LOW indicates the direction of the TRANSFER (to or from the DRAM), and DSF is used to select between NORMAL TRANSFER and SPLIT TRANSFER cycles. Each of the TRANSFER cycles is described in this section.

READ TRANSFER (RT)

If $(\overline{ME})/\overline{WE}$ is HIGH and DSF is LOW when $\overline{RAS}$ goes LOW, a READ TRANSFER cycle is selected. The row address bits indicate which eight 512-bit DRAM row planes are transferred to the eight SAM data register planes. The column address bits indicate the start address (or Tap address) of the serial output cycle from the SAM data registers. $\overline{CAS}$ must fall for every TRANSFER in order to load a valid Tap address. A read transfer may be accomplished in two ways. If the transfer is to be synchronized with the serial clock, SC (REAL-TIME READ TRANSFER), $\overline{TR}/(\overline{OE})$ is taken HIGH after $\overline{CAS}$ goes LOW. The TRANSFER will be made when $\overline{TR}/(\overline{OE})$ goes HIGH. If the transfer does not have to be synchronized with SC (READ TRANSFER), $\overline{TR}/(\overline{OE})$ may go HIGH before $\overline{CAS}$ goes LOW and the actual data TRANSFER will be timed internally (refer to the AC Timing Diagrams). During the TRANSFER, 4,096 bits of DRAM data are written into the SAM data registers and the Tap address is stored in an internal 9-bit register. The split SAM status pin (QSF) will be LOW if the Tap is in the lower half (addresses 0 through 255), and HIGH if it is in the upper half (256 through 511). If $\overline{SE}$ is LOW, the first bits of the new row data will appear at the serial outputs with the first SC clock pulse. $\overline{SE}$ enables the serial outputs and may be either HIGH or LOW during this operation. The SAM address pointer will increment with the SC LOW-to-HIGH transition, regardless of the state of $\overline{SE}$. Performing a READ TRANSFER cycle sets the direction of the SAM I/O buffers to the output mode.

SPLIT READ TRANSFER (SRT)

The SPLIT READ TRANSFER (SRT) cycle eliminates the critical transfer timing required to maintain a continuous serial output data stream. When using normal TRANSFER cycles to do midline reloads, a REAL-TIME READ TRANSFER must be done. The REAL-TIME READ TRANSFER has to occur between the last clock of "old" data and first clock of the "new" data of the SAM port.

When using the SPLIT TRANSFER mode, the SAM is divided into an upper half and a lower half. While data is being serially read from one half of the SAM, new DRAM data may be transferred to the other half. The transfer may occur at any time while the other half is sending data, and is not synchronized with the serial clock.

The $\overline{TR}/(\overline{OE})$ timing is also relaxed for SPLIT TRANSFER cycles. The rising edge of $\overline{TR}/(\overline{OE})$ is not used to complete the TRANSFER cycle and therefore is independent of the falling edge of $\overline{CAS}$ or the rising edge of SC. The transfer timing is generated internally for SPLIT TRANSFER cycles. A SPLIT READ TRANSFER does not change the direction of the SAM I/O port.

A "full" READ TRANSFER cycle must precede any sequence of SRT cycles to provide a reference to which half of the SAM the access will begin (the state of QSF), and to set SAM I/O direction. Then an SRT may be initiated by taking DSF HIGH when $\overline{RAS}$ goes LOW during the TRANSFER cycle. As in nonsplit transfers, the row address is used to specify the DRAM row to be transferred. The column address, A0-A7, is used to input the SAM Tap address. Address pin A8 is a "don't care" when the Tap address is loaded at the HIGH-to-LOW transition of $\overline{CAS}$. It is internally generated in such a manner that the SPLIT TRANSFER will automatically be to the SAM half not being accessed.

Figure 4 shows a typical SRT initiation sequence. The normal READ TRANSFER is performed first, followed by an SRT of the same row to the upper half of the SAM. The SRT to the upper half is optional, and need only be done if the Tap for the upper half is ≠ 0. Serial access continues, and when the SAM address counter reaches 255 ("A8"= 0, A0-A7=1) the QSF output goes HIGH and, if an SRT was done for the upper half, the new Tap address is loaded for the next half ("A8" = 1, A0-A7 = Tap). Once the serial access has switched to the upper SAM (QSF has gone HIGH), new data may be transferred to the lower SAM. For example, the next step in Figure 4 would be to wait until QSF went LOW (indicating that row-1 data is shifting out of the lower SAM) and execute an SRT of the upper half of row 1 to the upper SAM. If the half boundary is reached before an SRT is done for the next half, the device will leave split mode and the access will start from address 256 if going to the upper half or at 0 if going to the lower half (see Figure 5).

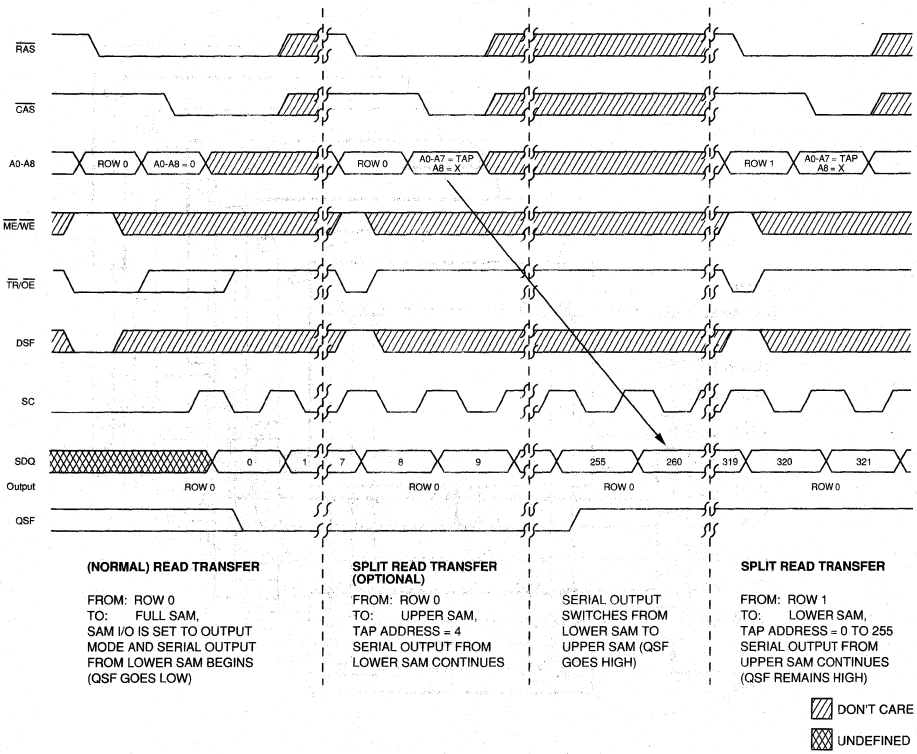


Figure 4
TYPICAL SPLIT-READ-TRANSFER INITIATION SEQUENCE

The stop address of the SAM half (the point at which access will change to the next half) is programmable on the MT42C8256. This function is described in the PROGRAMMABLE SPLIT SAM section of the Functional Description.

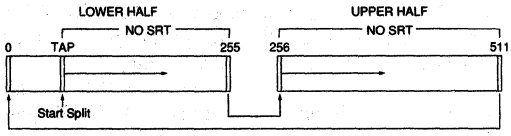


Figure 5
SPLIT SAM TRANSFER

MASKED WRITE TRANSFER (MWT)

The operation of the MASKED WRITE TRANSFER (MWT) is identical to that of the READ TRANSFER described previously except ($\overline{ME}$)/$\overline{WE}$ is LOW and a DQ plane mask is applied when $\overline{RAS}$ goes LOW. The row address indicates the DRAM row to which the SAM data registers will be written. The column address (Tap) indicates the starting address of the next SERIAL INPUT cycle for the SAM data registers. A DQ mask must be applied to all MWTs as shown in Figure 6. This may be done using persistent or nonpersistent modes. When using persistent mode, the mask will be supplied by the mask register. When in nonpersistent mode, the DQ pins are used to input a bit plane mask at the falling edge of $\overline{RAS}$. An MWT changes the direction of the SAM I/O buffers to the input mode. To change the SAM I/O buffers to input mode without SAM data being transferred to the DRAM, a mask of all 0's must be presented on the DQ pins when $\overline{RAS}$ falls. QSF is LOW if serial input is to the lower half of the SAM, and HIGH if it is to the upper.

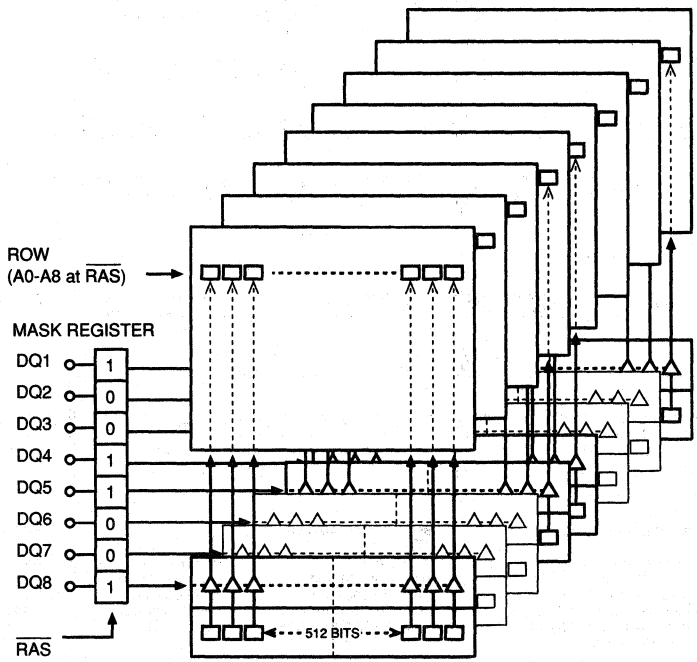


Figure 6
DQ MASKED WRITE TRANSFER

MASKED SPLIT WRITE TRANSFER (MSWT)

The MASKED SPLIT WRITE TRANSFER (MSWT) cycle allows serial input data to be transferred to the DRAM without interrupting the serial clock. Operation of the SWT cycle is very similar to the SPLIT READ TRANSFER cycle. It will transfer the idle half of the SAM to the DRAM and set the Tap address to where the new serial data will be loaded in that half. Selection of the MSWT cycle is the same as that of the MASKED WRITE TRANSFER with the exception of the state of DSF. When DSF is HIGH at the falling edge of $\overline{RAS}$, an MSWT will occur. The initiation sequence for MSWT is shown in Figure 7. An MSWT will not change the direction of the SAM I/O buffers.

PROGRAMMABLE SPLIT SAM

Programmable Split SAM operation is an extension of the Split SAM mode. This mode optimizes SAM performance by allowing user-programmable stop points to be defined in the split SAM. The stop points define a SAM location at which the access will change from one half of the SAM to the other half (at the loaded Tap address). The locations of the stop points are programmable in power-of-two increments. The stop points and size of the resulting partitions are shown in Figure 8, along with an example.

The stop points are set by performing a $\overline{CAS}$-BEFORE-$\overline{RAS}$ (Reset Stop Addrs) cycle (CBRS). A CBRS cycle is a $\overline{CAS}$-BEFORE-$\overline{RAS}$ with $\overline{ME}$/$\overline{WE}$ LOW and DSF HIGH at

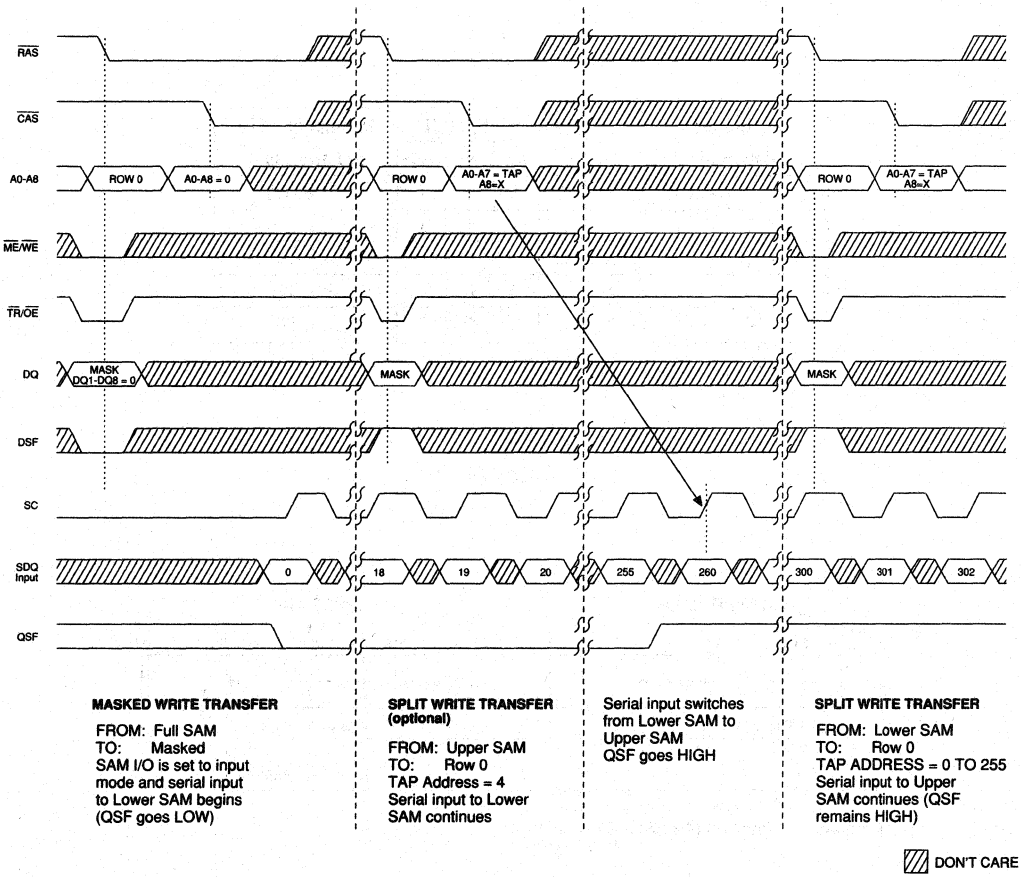


Figure 7
TYPICAL SPLIT-WRITE-TRANSFER INITIATION SEQUENCE

the $\overline{RAS}$ HIGH-to-LOW transition. This is a special $\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh cycle that, in addition to refreshing the DRAM, will sample the address pins (A4-A8) and set the stop point partition to the addressed value (See Figure 8). The programmable stop points will not become valid until a Split Transfer (READ or WRITE) is done, following the CBRS. Both halves of the SAM will be programmed simultaneously to the same partition lengths and stop points.

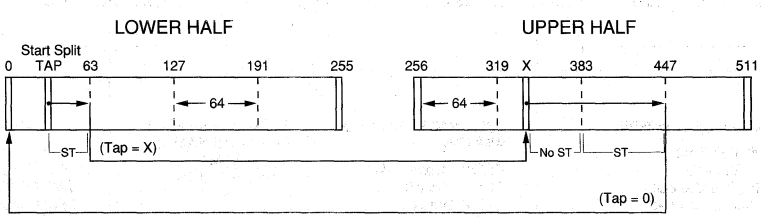
Access will progress from the Tap address to the end of the programmable partition into which the Tap fell. When the end of the "addressed" partition is reached, the access will jump to the tap address of the next half, provided that a SPLIT TRANSFER (READ or WRITE) was done before the partition boundary was reached. If a SPLIT TRANSFER (ST) is not done prior to the terminal count of the partition, the partition is not recognized and the address count will continue in the same half (this is shown Figure 8 at stop address 383). The count will continue in the same half until a SPLIT TRANSFER (READ or WRITE) occurs or the SAM half boundary is reached. In Figure 8, an ST occurs some time between addresses 383 and 447 and the boundary is recognized at 447. The programmable stop points may be reprogrammed at any time by performing another CBRS cycle, the new stop points will not be valid until an ST is performed.

Disabling the Programmable Split SAM requires a CBRR (Reset All Options). This is a $\overline{CAS}$-BEFORE-$\overline{RAS}$ cycle with DSF LOW at the $\overline{RAS}$ HIGH-to-LOW transition. The CBRR (Reset) will take effect immediately; it does not require an ST to become active valid.

Number Stop Points/Half	Address @ $\overline{RAS}$ LOW					Number and Size of Partition(s)
	A8	A7	A6	A5	A4	
1 (Default)	X	1	1	1	1	1 x 256
2	X	0	1	1	1	2 x 128
4	X	0	0	1	1	4 x 64
8	X	0	0	0	1	8 x 32
16	X	0	0	0	0	16 x 16

A0-A3 = "don't care"

EXAMPLE
(4 stop points)



Programmed Partition (A4-A8) = 000111111
MSB....LSB

Figure 8
PROGRAMMABLE SPLIT SAM OPERATION

NEW ■ MULTIPORT DRAM

SERIAL INPUT AND SERIAL OUTPUT

The control inputs for SERIAL INPUT and SERIAL OUTPUT are SC and $\overline{SE}$. The rising edge of SC increments the serial address counter and provides access to the next SAM location. $\overline{SE}$ enables or disables the serial input/output buffers.

Serial output of the SAM contents will start at the serial start address that was loaded in the SAM address counter during a READ or SPLIT READ TRANSFER cycle. The SC input increments the address counter and presents the contents of the next SAM location to the 8-bit port. $\overline{SE}$ is used as an output enable during the SAM output operation. The serial address is automatically incremented with every SC LOW-to-HIGH transition, regardless of whether $\overline{SE}$ is HIGH or LOW. The address progresses through the SAM and will wrap around (after count 255 or 511) to the Tap address of the next half, for split modes. If an SRT was not performed before the half boundary is reached, the count will progress as illustrated in Figure 5. Address count will wrap around (after count 511) to Tap address 0 if in the "full" SAM modes.

SC is also used to clock-in data when the device is in the serial input mode. As in the serial output operation, the contents of the SAM address counter (loaded when the serial input mode was enabled) will determine the serial address of the first 8-bit word written. $\overline{SE}$ acts as a write enable for serial input data and must be LOW for valid serial input. If $\overline{SE}$ = HIGH, the data inputs are disabled and the SAM contents will not be modified. The serial address counter is incremented with every LOW-to-HIGH transition of SC, regardless of the logic level on the $\overline{SE}$ input.

POWER-UP AND INITIALIZATION

After Vcc is at specified operating conditions, for 100µs minimum, eight $\overline{RAS}$ cycles must be executed to initialize the dynamic memory array. Micron recommends that $\overline{RAS} = (\overline{TR})/\overline{OE} \geq V_{IH}$ during power-up to ensure that the DRAM I/O pins (DQs) are in a High-Z state. The DRAM array will contain random data, and the nonpersistent MASKED WRITE mode is enabled.

The SAM portion of the MT42C8256 is completely static in operation and does not require refresh or initialization. The SAM port will power-up in the serial input mode (MASKED WRITE TRANSFER) and the I/O pins (SDQs) will be High- Z, regardless of the state of $\overline{SE}$. QSF initializes in the LOW state. The mask and color register will contain random data after power-up.

TRUTH TABLE

CODE	FUNCTION	RAS FALLING EDGE				CAS FALL	A0-A8[1]		DQ1-DQ8[2]		REGISTERS	
		CAS	TR/OE	ME/WE	DSF	DSF	RAS	CAS	RAS	CAS[3]	MASK	COLOR
	DRAM OPERATIONS											
CBRR	CAS-BEFORE-RAS REFRESH (RESET ALL OPTIONS)	0	X	X	0	—	X	X	—	X	X	X
CBRS	CAS-BEFORE-RAS REFRESH (RESET STOP ADDRESS)	0	X	0	1	—	STOP[7]	X	—	X	X	X
CBRN	CAS-BEFORE-RAS REFRESH (NO RESET)	0	X	1	1	—	X	X	—	X	X	X
ROR	RAS ONLY REFRESH	1	1	X	X	—	ROW	—	X	—	X	X
RW	NORMAL DRAM READ OR WRITE	1	1	1	0	0	ROW	COLUMN	X	VALID DATA	X	X
RWM	MASKED WRITE TO DRAM (OLD OR NEW MASK)	1	1	0	0	0	ROW	COLUMN	WRITE MASK[4]	VALID DATA	USE[4]	X
BW	BLOCK WRITE TO DRAM	1	1	1	0	1	ROW	COLUMN (A2-A8)	X	COLUMN MASK	X	USE
BWM	MASKED BLOCK WRITE TO DRAM (OLD OR NEW MASK)	1	1	0	0	1	ROW	COLUMN (A2-A8)	WRITE MASK[4]	COLUMN MASK	USE[4]	USE
FWM	MASKED FLASH WRITE TO DRAM (OLD OR NEW MASK)	1	1	0	1	X	ROW	X	WRITE MASK[4]	X	USE[4]	USE
	REGISTER OPERATIONS											
LMR	LOAD MASK REGISTER	1	1	1	1	0	ROW[5]	X	X	REG DATA	LOAD	X
LCR	LOAD COLOR REGISTER	1	1	1	1	1	ROW[5]	X	X	REG DATA	X	LOAD
	TRANSFER OPERATIONS											
RT	READ TRANSFER (DRAM-TO-SAM TRANSFER)	1	0	1	0	X	ROW	TAP[6]	X	X	X	X
SRT	SPLIT READ TRANSFER (SPLIT DRAM-TO-SAM TRANSFER)	1	0	1	1	X	ROW	TAP[6]	X	X	X	X
MWT	MASKED WRITE TRANSFER (SAM-TO-DRAM TRANSFER) (NEW OR OLD MASK)	1	0	0	0	X	ROW	TAP[6]	WRITE MASK[4]	X	USE[4]	X
MSWT	MASKED SPLIT WRITE TRANSFER (SAM-TO-DRAM TRANSFER) (NEW OR OLD MASK)	1	0	0	1	X	ROW	TAP[6]	WRITE MASK[4]	X	USE[4]	X

NOTE:

1. These columns show what must be present on the A0-A8 inputs when RAS falls and when CAS falls.
2. These columns show what must be present on the DQ1-DQ8 inputs when RAS falls and when CAS falls.
3. During WRITE (including BLOCK WRITE) cycles, the input data is latched at the falling edge of CAS or ME/WE, whichever is later. Similarly, on READ cycles, the output data is valid after the falling edge of CAS or TR/OE, whichever is later.
4. After an LMR cycle, all masked WRITEs use the mask register (old mask). Data on the DQs at RAS falling edge will be ignored. A CBRR will reset to new mask state and mask data must be presented on the DQs at every RAS falling edge.
5. The ROW that is addressed will be refreshed, but a ROW address is not required.
6. This is the first SAM address location that the first SC cycle will access. For split SAM transfers, the Tap will be the first address location accessed of the "new" SAM half after the boundary of the current half is reached (255 for lower half, 511 for upper half or Programmable Stop Address boundary).
7. Defines the column addresses where access moves to the next half, see Programmable Split SAM functional description.

ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc Supply Relative to Vss ..... -1V to +7V
Operating Temperature, T_A (Ambient) ..... 0°C to +70°C
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.5	V	1
Input High (Logic 1) Voltage, All Inputs	V_{IH}	2.4	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, All Inputs	V_{IL}	-1.0	0.8	V	1

DC ELECTRICAL CHARACTERISTICS

(0°C ≤ T_A ≤ 70°C; V_{CC} = 5V ±10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
INPUT LEAKAGE CURRENT Any input (0V ≤ V_{IN} ≤ V_{CC}); all other pins not under test = 0V	I_L	-10	10	µA	
OUTPUT LEAKAGE CURRENT (DQ, SDQ disabled, 0V ≤ V_{OUT} ≤ V_{CC})	I_{OZ}	-10	10	µA	
OUTPUT LEVELS Output High Voltage (I_{OUT} = -2.5mA)	V_{OH}	2.4		V	1
Output Low Voltage (I_{OUT} = 2.5mA)	V_{OL}		0.4	V	

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A8	C_{I1}		5	pF	2
Input Capacitance: $\overline{RAS}$, $\overline{CAS}$, $\overline{ME}/\overline{WE}$, $\overline{TR}/\overline{OE}$, SC, $\overline{SE}$, DSF	C_{I2}		8	pF	2
Input/Output Capacitance: DQ, SDQ	$C_{I/O}$		9	pF	2
Output Capacitance: QSF	C_O		9	pF	2

CURRENT DRAIN, SAM IN STANDBY

($0°C \le T_A \le 70°C$; V_{CC} = 5V ±10%)

PARAMETER/CONDITION	SYMBOL	MAX -7	MAX -8	UNITS	NOTES
OPERATING CURRENT ($\overline{RAS}$ and $\overline{CAS}$ = Cycling: $^tRC = ^tRC$ (MIN))	I_{CC1}	110	100	mA	3, 4 25
OPERATING CURRENT: FAST PAGE MODE ($\overline{RAS} = V_{IL}$; $\overline{CAS}$ = Cycling: $^tPC = ^tPC$ (MIN))	I_{CC2}	85	75	mA	3, 4 26
STANDBY CURRENT: TTL INPUT LEVELS Power supply standby current ($\overline{RAS} = \overline{CAS} = V_{IH}$ after 8 $\overline{RAS}$ cycles (MIN))	I_{CC3}	10	10	mA	
REFRESH CURRENT: $\overline{RAS}$-ONLY ($\overline{RAS}$ = Cycling; $\overline{CAS} = V_{IH}$)	I_{CC4}	110	100	mA	3, 25
REFRESH CURRENT: $\overline{CAS}$-BEFORE-$\overline{RAS}$ ($\overline{RAS}$ and $\overline{CAS}$ = Cycling)	I_{CC5}	110	100	mA	3, 5
SAM/DRAM DATA TRANSFER	I_{CC6}	115	105	mA	3

CURRENT DRAIN, SAM ACTIVE (^tSC = MIN)

($0°C \le T_A \le 70°C$; V_{CC} = 5V ±10%)

PARAMETER/CONDITION	SYMBOL	MAX -7	MAX -8	UNITS	NOTES
OPERATING CURRENT ($\overline{RAS}$ and $\overline{CAS}$ = Cycling: $^tRC = ^tRC$ (MIN))	I_{CC7}	160	145	mA	3, 4 25
OPERATING CURRENT: FAST PAGE MODE ($\overline{RAS} = V_{IL}$; $\overline{CAS}$ = Cycling: $^tPC = ^tPC$ (MIN))	I_{CC8}	135	120	mA	3, 4 26
STANDBY CURRENT: TTL INPUT LEVELS Power supply standby current ($\overline{RAS} = \overline{CAS} = V_{IH}$ after 8 $\overline{RAS}$ cycles (MIN))	I_{CC9}	50	45	mA	3, 4
REFRESH CURRENT: $\overline{RAS}$-ONLY ($\overline{RAS}$ = Cycling; $\overline{CAS} = V_{IH}$)	I_{CC10}	160	145	mA	3, 4 25
REFRESH CURRENT: $\overline{CAS}$-BEFORE-$\overline{RAS}$ ($\overline{RAS}$ and $\overline{CAS}$ = Cycling)	I_{CC11}	160	145	mA	3, 4, 5
SAM/DRAM DATA TRANSFER	I_{CC12}	165	150	mA	3, 4

DRAM TIMING PARAMETERS

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C ≤ T_A ≤ +70°C; Vcc = 5V ±10%)

AC CHARACTERISTICS		-7		-8			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Random READ or WRITE cycle time	tRC	130		150		ns	
READ-MODIFY-WRITE cycle time	tRWC	175		195		ns	
FAST-PAGE-MODE READ or WRITE cycle time [Extended Data Out (READ)]	tPC	30		40		ns	
FAST-PAGE-MODE READ-MODIFY-WRITE cycle time	tPRWC	75		85		ns	
Access time from $\overline{RAS}$	tRAC		70		80	ns	14
Access time from $\overline{CAS}$	tCAC		15		20	ns	15, 28
Access time from ($\overline{TR}$)/$\overline{OE}$	tOE		15		15	ns	
Access time from column address	tAA		25		35	ns	
Access time from $\overline{CAS}$ precharge	tCPA		30		40	ns	
$\overline{RAS}$ pulse width	tRAS	70	20,000	80	20,000	ns	
$\overline{RAS}$ pulse width (FAST PAGE MODE)	tRASP	70	100,000	80	100,000	ns	
$\overline{RAS}$ hold time	tRSH	15		20		ns	
$\overline{RAS}$ precharge time	tRP	50		60		ns	
$\overline{CAS}$ pulse width	tCAS	15	10,000	20	10,000	ns	
$\overline{CAS}$ hold time	tCSH	65		75		ns	
$\overline{CAS}$ precharge time	tCP	10		10		ns	16
$\overline{RAS}$ to $\overline{CAS}$ delay time	tRCD	20	50	20	55	ns	17
$\overline{CAS}$ to $\overline{RAS}$ precharge time	tCRP	5		5		ns	
Row address setup time	tASR	0		0		ns	
Row address hold time	tRAH	10		10		ns	
$\overline{RAS}$ to column address delay time	tRAD	15	45	15	45	ns	18
Column address setup time	tASC	0		0		ns	
Column address hold time	tCAH	10		10		ns	
Column address hold time (referenced to $\overline{RAS}$)	tAR	35		40		ns	
Column address to $\overline{RAS}$ lead time	tRAL	35		40		ns	
Read command setup time	tRCS	0		0		ns	
Read command hold time (referenced to $\overline{CAS}$)	tRCH	0		0		ns	19
Read command hold time (referenced to $\overline{RAS}$)	tRRH	0		0		ns	19
$\overline{CAS}$ to output in Low-Z	tCLZ	3		3		ns	
$\overline{CAS}$ HIGH to $\overline{RAS}$ HIGH lead time	tCRL	0		0		ns	
$\overline{RAS}$ HIGH to $\overline{CAS}$ HIGH lead time	tRCL	0		0		ns	
Output buffer turn-off delay from $\overline{CAS}$ or $\overline{RAS}$	tOFF	3	20	3	20	ns	20, 23
Output disable delay from ($\overline{TR}$)/$\overline{OE}$	tOD	3	10	3	10	ns	20, 23
Output disable delay from ($\overline{ME}$)/$\overline{WE}$	tWHZ	3	10	3	10	ns	
Output disable hold time from start of WRITE	tOEH	10		10		ns	27
Output Enable to $\overline{RAS}$ delay	tORD	0		0		ns	
Data output hold after $\overline{CAS}$ LOW	tCOH	5		5		ns	28

NEW ■ MULTIPORT DRAM

DRAM TIMING PARAMETERS (continued)

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C ≤ T_A ≤ +70°C; Vcc = 5V ±10%)

AC CHARACTERISTICS		-7		-8			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Write command setup time	^tWCS	0		0		ns	21
Write command hold time	^tWCH	15		15		ns	
Write command hold time (referenced to $\overline{RAS}$)	^tWCR	50		55		ns	
Write command pulse width	^tWP	15		15		ns	
Write command to $\overline{RAS}$ lead time	^tRWL	20		20		ns	
Write command to $\overline{CAS}$ lead time	^tCWL	15		20		ns	
Data-in setup time	^tDS	0		0		ns	22
Data-in hold time	^tDH	10		15		ns	22
Data-in hold time (referenced to $\overline{RAS}$)	^tDHR	50		55		ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	^tRWD	90		100		ns	21
Column address to $\overline{WE}$ delay time	^tAWD	45		55		ns	21
$\overline{CAS}$ to $\overline{WE}$ delay time	^tCWD	35		40		ns	21
Transition time (rise or fall)	^tT	3	35	3	35	ns	9, 10
Refresh period (512 cycles)	^tREF		8		8	ms	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	^tRPC	0		0		ns	
$\overline{CAS}$ setup time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH)	^tCSR	10		10		ns	5
$\overline{CAS}$ hold time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH)	^tCHR	15		15		ns	5
$\overline{ME}$/$\overline{WE}$ to $\overline{RAS}$ setup time	^tWSR	0		0		ns	
$\overline{ME}$/$\overline{WE}$ to $\overline{RAS}$ hold time	^tRWH	10		15		ns	
Mask data to $\overline{RAS}$ setup time	^tMS	0		0		ns	
Mask data to $\overline{RAS}$ hold time	^tMH	10		15		ns	

NEW ■ MULTIPORT DRAM

TRANSFER AND MODE CONTROL TIMING PARAMETERS

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes 6, 7, 8, 9, 10) (0° C ≤ T_A ≤ + 70°C; Vcc = 5V ±10%)

AC CHARACTERISTICS		-7		-8			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
$\overline{TR}/(\overline{OE})$ LOW to $\overline{RAS}$ setup time	^tTLS	0		0		ns	
$\overline{TR}/(\overline{OE})$ LOW to $\overline{RAS}$ hold time	^tTLH	10	10,000	15	10,000	ns	
$\overline{TR}/(\overline{OE})$ LOW to $\overline{RAS}$ hold time (REAL-TIME READ-TRANSFER only)	^tRTH	55	10,000	65	10,000	ns	
$\overline{TR}/(\overline{OE})$ LOW to $\overline{CAS}$ hold time (REAL-TIME READ-TRANSFER only)	^tCTH	20		20		ns	
$\overline{TR}/(\overline{OE})$ HIGH to $\overline{RAS}$ precharge time	^tTRP	50		60		ns	
$\overline{TR}/(\overline{OE})$ precharge time	^tTRW	25		25		ns	
$\overline{TR}/(\overline{OE})$ HIGH to SC lead time	^tTSL	5		5		ns	
First SC edge to $\overline{TR}/(\overline{OE})$ HIGH delay time	^tTSD	15		15		ns	
Serial output buffer turn-off delay from $\overline{RAS}$	^tSDZ	10	30	10	35	ns	
SC to $\overline{RAS}$ setup time	^tSRS	20		25		ns	
Serial data input to $\overline{SE}$ delay time	^tSZE	0		0		ns	
Serial data input delay from $\overline{RAS}$	^tSDD	40		45		ns	
Serial data input to $\overline{RAS}$ delay time	^tSZS	0		0		ns	
Serial-input-mode enable ($\overline{SE}$) to $\overline{RAS}$ setup time	^tESR	0		0		ns	
Serial-input-mode enable ($\overline{SE}$) to $\overline{RAS}$ hold time	^tREH	10		15		ns	
$\overline{TR}/(\overline{OE})$ HIGH to $\overline{RAS}$ setup time	^tYS	0		0		ns	
$\overline{TR}/(\overline{OE})$ HIGH to $\overline{RAS}$ hold time	^tYH	10		15		ns	
DSF to $\overline{RAS}$ setup time	^tFSR	0		0		ns	
DSF to $\overline{RAS}$ hold time	^tRFH	10		15		ns	
SC to QSF delay time	^tSQD		18		25	ns	
SPLIT TRANSFER setup time	^tSTS	25		30		ns	
SPLIT TRANSFER hold time	^tSTH	0		0		ns	
DSF (at $\overline{CAS}$ LOW) to $\overline{RAS}$ hold time	^tFHR	50		55		ns	
DSF to $\overline{CAS}$ setup time	^tFSC	0		0		ns	
DSF to $\overline{CAS}$ hold time	^tCFH	15		15		ns	
$\overline{TR}/\overline{OE}$ to QSF delay time	^tTQD		20		25	ns	
$\overline{RAS}$ to QSF delay time	^tRQD		55		65	ns	
$\overline{CAS}$ to QSF delay time	^tCQD		25		35	ns	
$\overline{RAS}$ to first SC delay	^tRSD	70		80		ns	
$\overline{CAS}$ to first SC delay	^tCSD	25		30		ns	

SAM TIMING PARAMETERS

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes 6, 7, 8, 9, 10) (0° C ≤ T_A ≤ + 70°C; Vcc = 5V ±10%)

AC CHARACTERISTICS		-7		-8			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Serial clock cycle time	^tSC	18		25		ns	
Access time from SC	^tSAC		15		20	ns	24, 28
SC precharge time (SC LOW time)	^tSP	5		10		ns	
SC pulse width (SC HIGH time)	^tSAS	5		10		ns	
Access time from $\overline{SE}$	^tSEA		12		15	ns	24
$\overline{SE}$ precharge time	^tSEP	10		10		ns	
$\overline{SE}$ pulse width	^tSE	10		10		ns	
Serial data-out hold time after SC high	^tSOH	5		5		ns	24, 28
Serial output buffer turn-off delay from $\overline{SE}$	^tSEZ	3	10	3	12	ns	20, 24
Serial data-in setup time	^tSDS	3		3		ns	
Serial data-in hold time	^tSDH	5		5		ns	
Serial input (Write) Enable setup time	^tSWS	0		0		ns	
Serial input (Write) Enable hold time	^tSWH	10		10		ns	
Serial input (Write) disable setup time	^tSWIS	0		0		ns	
Serial input (Write) disable hold time	^tSWIH	10		10		ns	

NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. V_{CC} = 5V ±10%, f = 1 MHz.
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading. Specified values are obtained with minimum cycle time and the output open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is assured.
7. An initial pause of 100µs is required after power-up followed by any eight $\overline{RAS}$ cycles before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-up should be repeated any time the ^{t}REF refresh requirement is exceeded.
8. AC characteristics assume ^{t}T = 5ns.
9. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}). Input signals transition from 0 to 3V for AC testing.
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS}$ = V_{IH}, DRAM data output (DQ1-DQ8) is High-Z.
12. If $\overline{CAS}$ = V_{IL}, DRAM data output (DQ1-DQ8) may contain data from the last valid READ cycle.
13. DRAM output timing measured with a load equivalent to 1 TTL gates and 50pF. Output reference levels: V_{OH} = 2.0V; V_{OL} = 0.8V.
14. Assumes that ^{t}RCD < ^{t}RCD (MAX). If ^{t}RCD is greater than the maximum recommended value shown in this table, ^{t}RAC will increase by the amount that ^{t}RCD exceeds the value shown.
15. Assumes that ^{t}RCD ≥ ^{t}RCD (MAX).
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, DQ will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer, $\overline{CAS}$ must be pulsed HIGH for ^{t}CP.
17. Operation within the ^{t}RCD (MAX) limit ensures that ^{t}RAC (MAX) can be met. ^{t}RCD (MAX) is specified as a reference point only; if ^{t}RCD is greater than the specified ^{t}RCD (MAX) limit, then access time is controlled exclusively by ^{t}CAC.
18. Operation within the ^{t}RAD (MAX) limit ensures that ^{t}RCD (MAX) can be met. ^{t}RAD (MAX) is specified as a reference point only; if ^{t}RAD is greater than the specified ^{t}RAD (MAX) limit, then access time is controlled exclusively by ^{t}AA.
19. Either ^{t}RCH or ^{t}RRH must be satisfied for a READ cycle.
20. ^{t}OD, ^{t}OFF and ^{t}SEZ define the time when the output achieves open circuit (V_{OH} -200mV, V_{OL} +200mV). This parameter is sampled and not 100% tested.
21. ^{t}WCS, ^{t}RWD, ^{t}AWD and ^{t}CWD are restrictive operating parameters in LATE-WRITE, READ-WRITE and READ-MODIFY-WRITE cycles only. If ^{t}WCS ≥ ^{t}WCS (MIN), the cycle is an EARLY-WRITE cycle and the data output will remain an open circuit throughout the entire cycle, regardless of $\overline{TR}/\overline{OE}$. If ^{t}WCS ≤ ^{t}WCS (MIN), the cycle is a LATE-WRITE and $\overline{TR}/\overline{OE}$ must control the output buffers during the WRITE to avoid data contention. If ^{t}RWD ≥ ^{t}RWD (MIN), ^{t}AWD ≥ ^{t}AWD (MIN) and ^{t}CWD ≥ ^{t}CWD (MIN), the cycle is a READ-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of the output buffers (at access time and until $\overline{CAS}$ goes back to V_{IH}) is indeterminate, but the WRITE will be valid if ^{t}OD and ^{t}OEH are met. See the LATE-WRITE AC Timing diagram.
22. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY-WRITE cycles and $\overline{ME}/\overline{WE}$ leading edge in LATE-WRITE or READ-WRITE cycles.
23. During a READ cycle, if $\overline{TR}/\overline{OE}$ is LOW then taken HIGH, DQ goes open. The DQs will go open with $\overline{OE}$ HIGH or when $\overline{RAS}$ and $\overline{CAS}$ go HIGH, whichever occurs first.
24. SAM output timing is measured with a load equivalent to 1 TTL gate and 30pF. Output reference levels: V_{OH} = 2.0V; V_{OL} = 0.8V.
25. Address (A0-A8) may be changed two times or less while $\overline{RAS}$ = V_{IL}.
26. Address (A0-A8) may be changed once or less while $\overline{CAS}$ = V_{IH} and $\overline{RAS}$ = V_{IL}.
27. LATE-WRITE and READ-MODIFY-WRITE cycles must have ^{t}OD and ^{t}OEH met ($\overline{OE}$ HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. The DQs will provide previously read data if $\overline{CAS}$ remains LOW and $\overline{OE}$ is taken LOW after ^{t}OEH is met. If $\overline{CAS}$ and $\overline{RAS}$ go HIGH prior to $\overline{OE}$ going back LOW, the DQs will remain open.
28. $^{t}SAC/^{t}CAC$ are MAX at 70° C and 4.5V Vcc; $^{t}SOH/^{t}COH$ are MIN at 0° C and 5.5V Vcc. These limits will not occur simultaneously at any given voltage or temperature. This is guaranteed by design ($^{t}SOH/^{t}COH$ = $^{t}SAC/^{t}CAC$ - output transition time).

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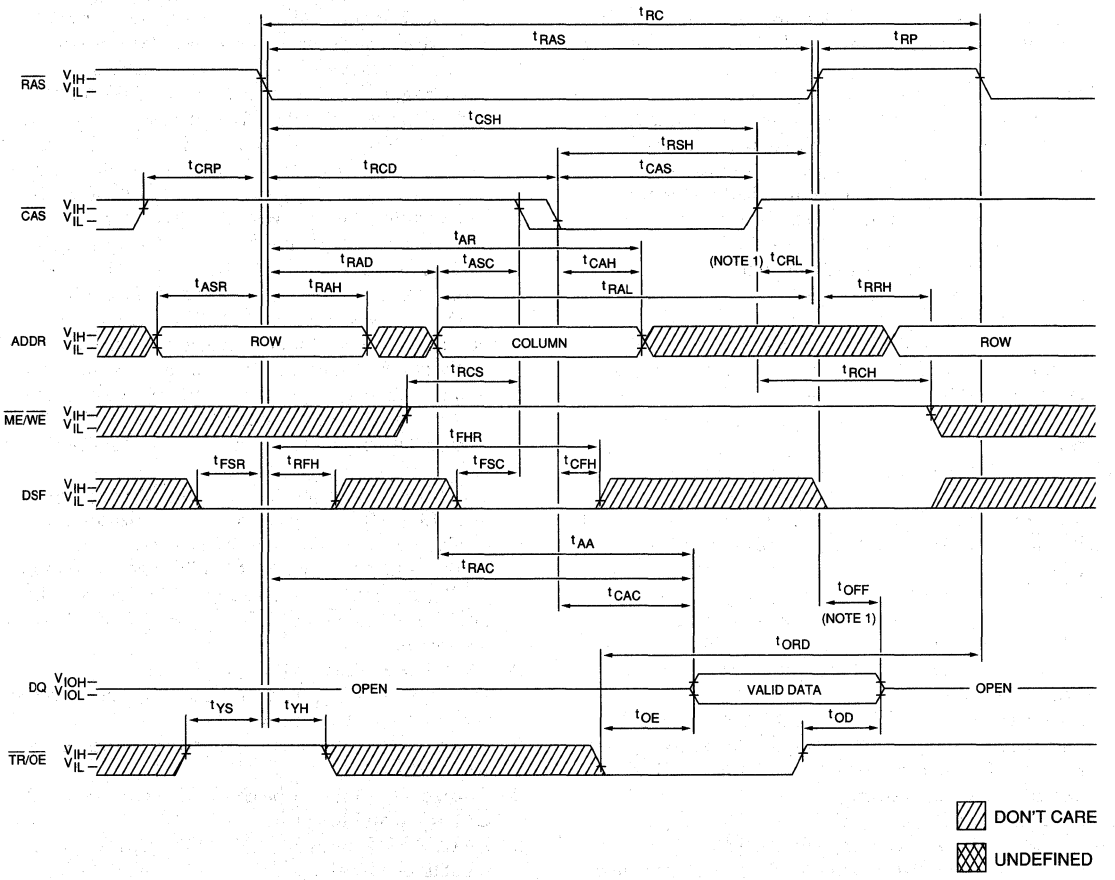
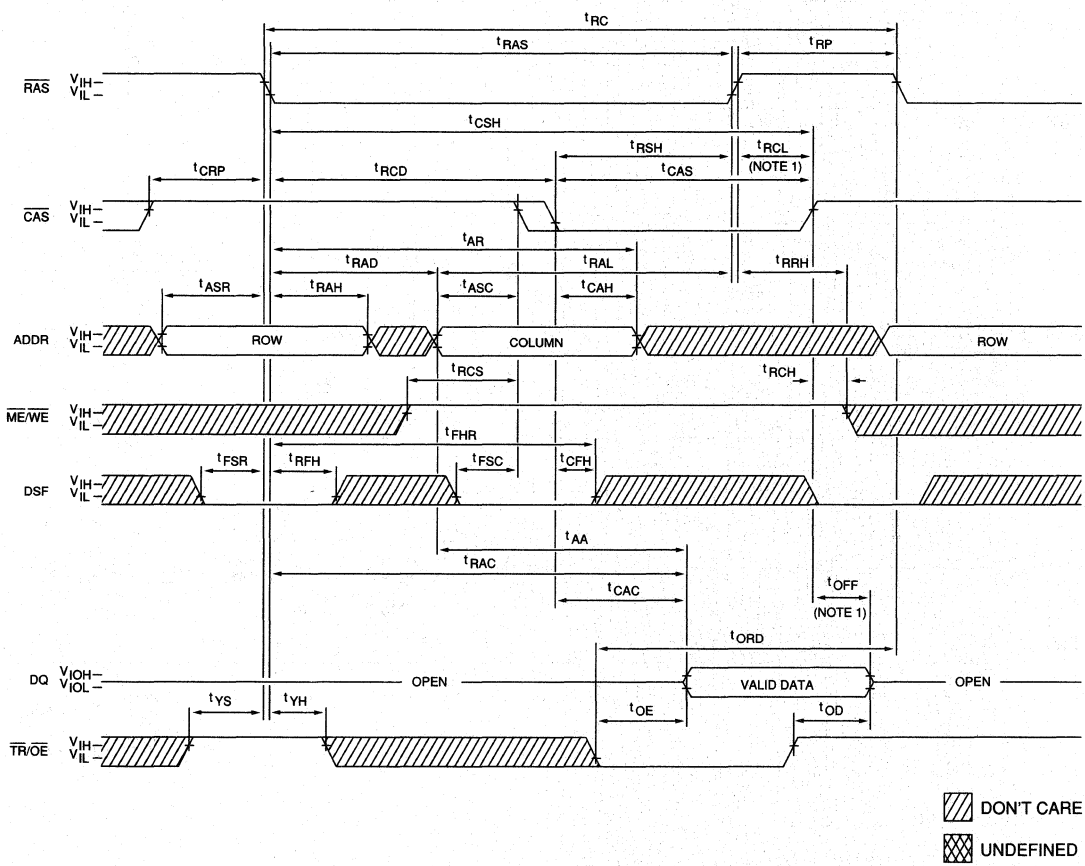
DRAM READ CYCLE [1]
(Outputs controlled by $\overline{RAS}$)



NOTE: 1. ^{t}CRL is a reference parameter. If $\overline{CAS}$ = HIGH ^{t}CRL before $\overline{RAS}$, ^{t}OFF is referenced from the rising edge of $\overline{RAS}$.

DRAM READ CYCLE [1]
(Outputs controlled by $\overline{CAS}$)



NOTE: 1. ^{t}RCL is a reference parameter. If $\overline{RAS}$ = HIGH ^{t}RCL before $\overline{CAS}$, ^{t}OFF is referenced from the rising edge of $\overline{CAS}$.

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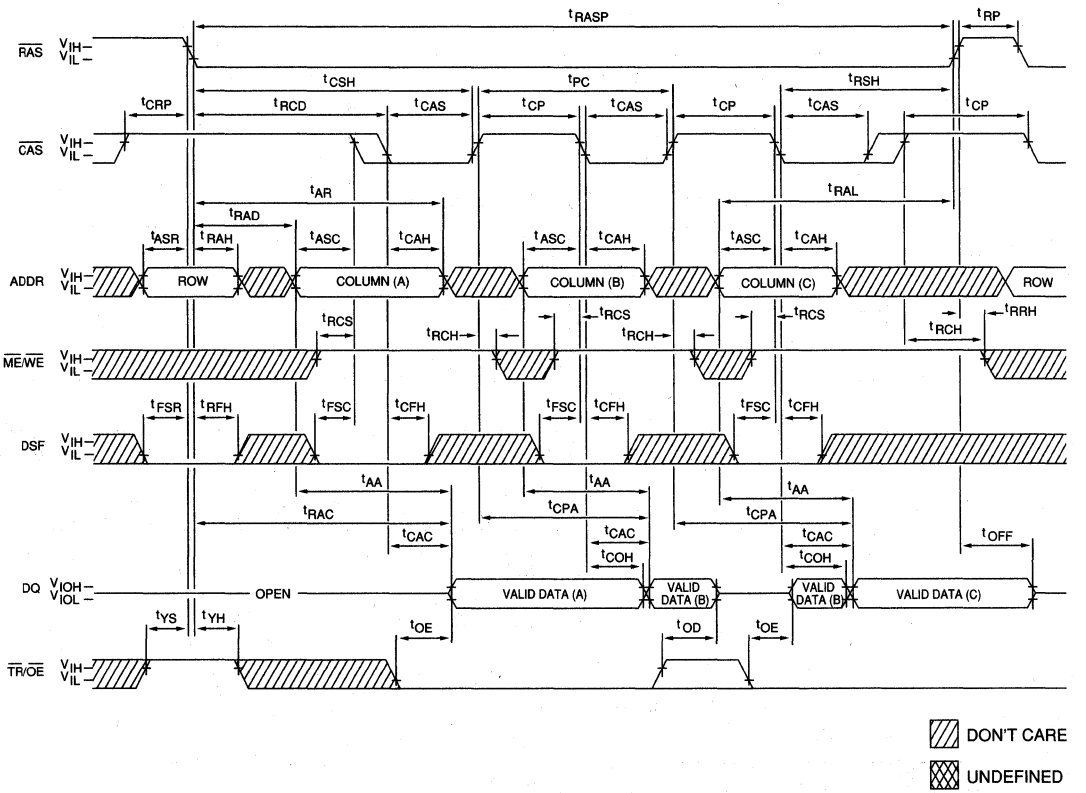
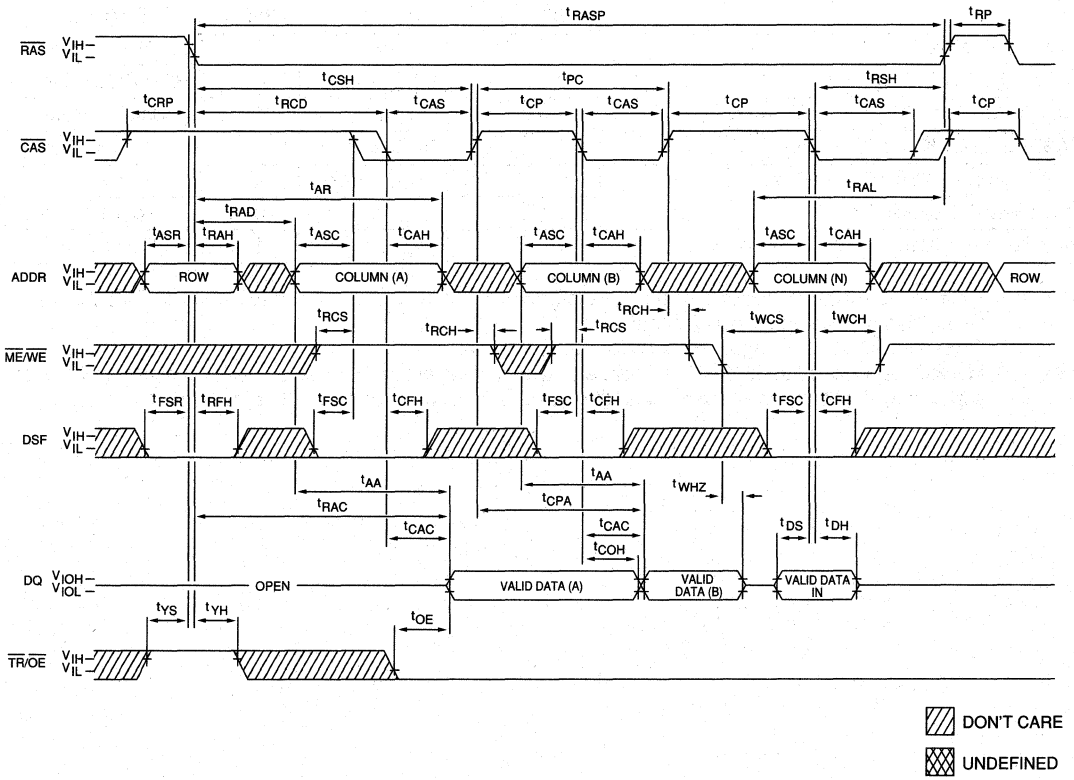
DRAM FAST-PAGE-MODE READ CYCLE
(Extended Data Out)



NOTE: WRITE cycles or READ-MODIFY-WRITE cycles may be mixed with READ cycles while in FAST PAGE MODE.

DRAM FAST-PAGE-MODE READ/WRITE CYCLE
(Extended Data Out)

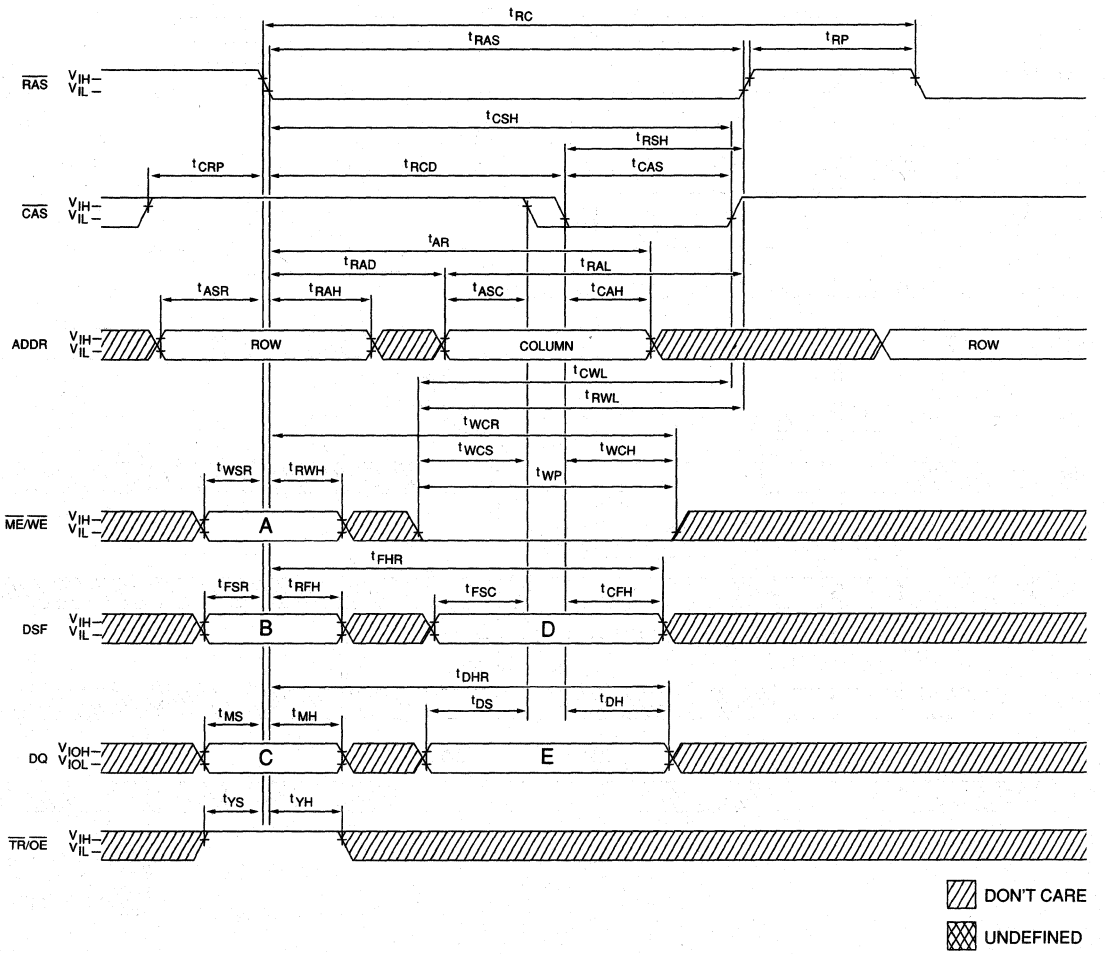


WRITE CYCLE FUNCTION TABLE [1]

FUNCTION	LOGIC STATES				
	RAS Falling Edge			CAS Falling Edge	
	A ME/WE	B DSF	C DQ (Input)	D DSF	E[2] DQ (Input)
Normal DRAM WRITE	1	0	X	0	DRAM Data
MASKED WRITE to DRAM	0	0	Write Mask[3]	0	DRAM Data (Masked)
BLOCK WRITE to DRAM (No Bit-Plane Mask)	1	0	X	1	Column Mask
MASKED BLOCK WRITE to DRAM	0	0	Write Mask[3]	1	Column Mask
MASKED FLASH WRITE to DRAM	0	1	Write Mask[3]	X	X
Load Mask Data Register	1	1	X	0	Write Mask Data
Load Color Register	1	1	X	1	Color Data

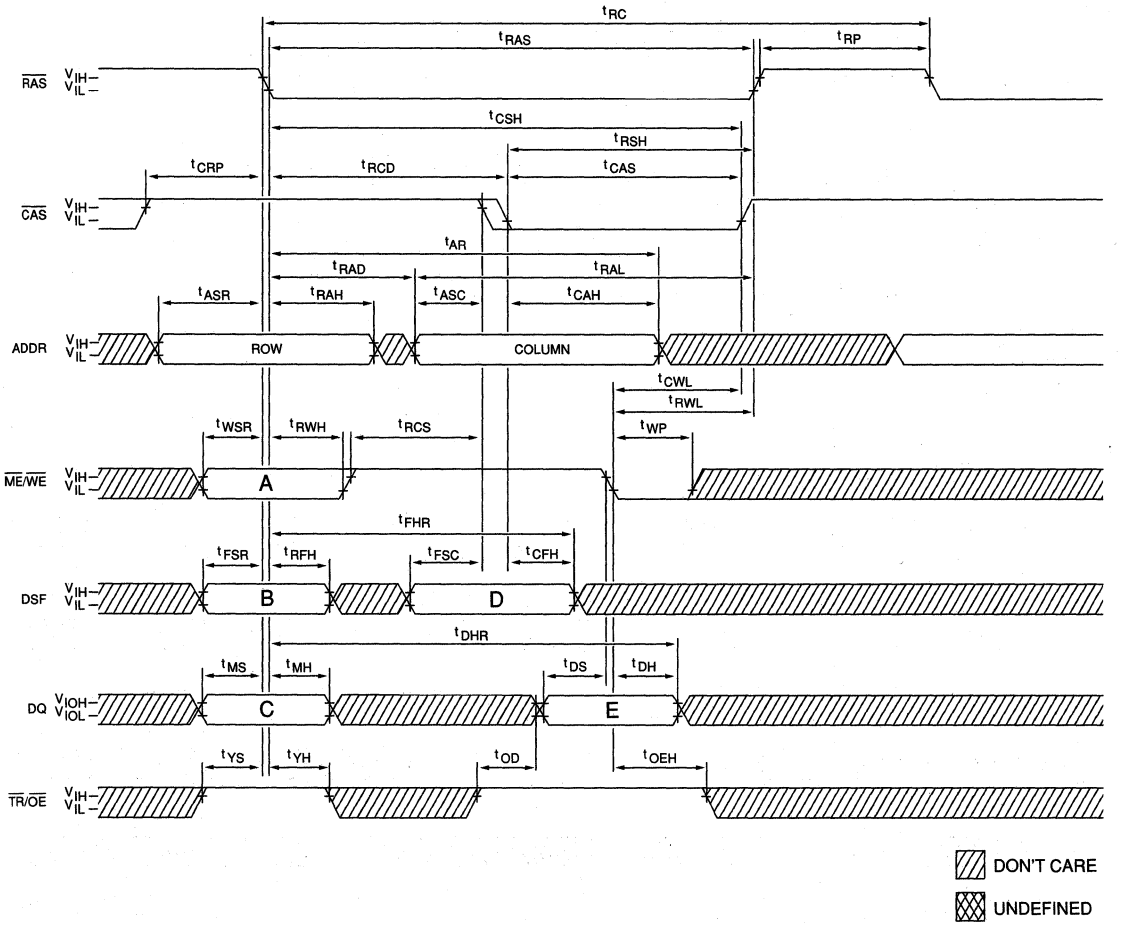
NOTE: 1. Refer to this function table to determine the logic states of "A", "B", "C", "D" and "E" for the WRITE cycle timing diagrams on the following pages.
2. $\overline{CAS}$ or $\overline{ME}/\overline{WE}$ falling edge, whichever occurs later.
3. Mask Data is loaded at $\overline{RAS}$ falling if nonpersistent mode is active. If persistent mode is active, mask data is supplied by the Mask Data Register and the DQs are "don't care" at the $\overline{RAS}$ falling edge.

DRAM EARLY-WRITE CYCLE [1]



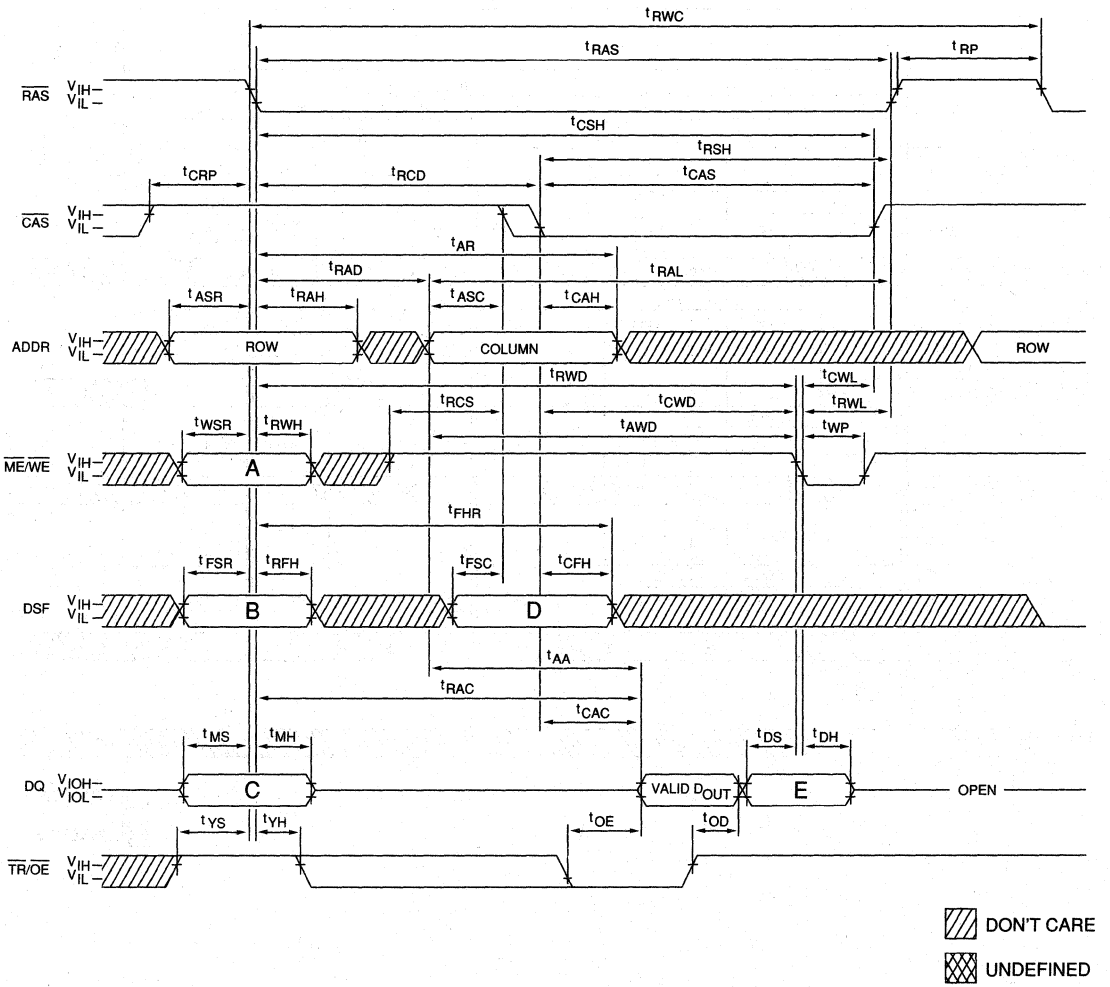
OTE: 1. The logic states of "A", "B", "C", "D" and "E" determine the type of WRITE operation performed. See the Write Cycle Function Table for a detailed description.

DRAM LATE-WRITE CYCLE



NOTE: The logic states of "A", "B", "C", "D" and "E" determine the type of WRITE operation performed. See the Write Cycle Function Table for a detailed description.

DRAM READ-WRITE CYCLE
(READ-MODIFY-WRITE CYCLE)

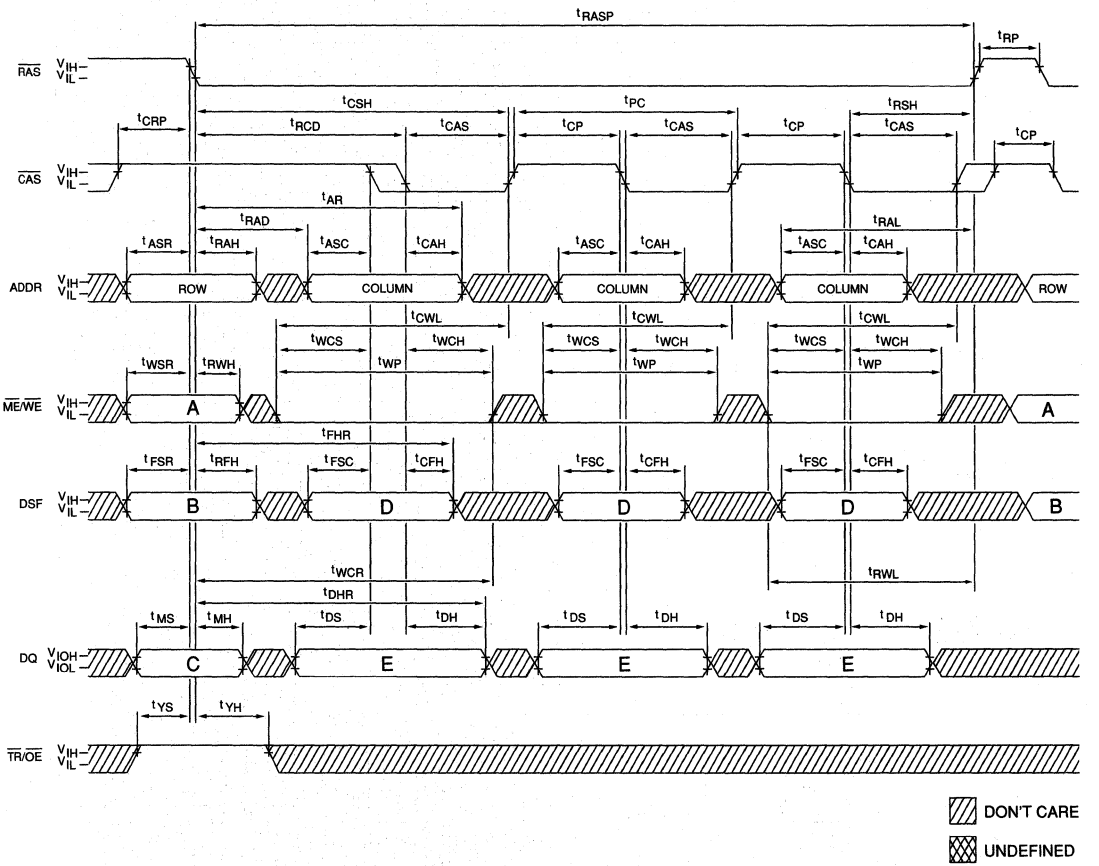


NOTE: The logic states of "A", "B", "C", "D" and "E" determine the type of WRITE operation performed. See the Write Cycle Function Table for a detailed description.

NEW ■ MULTIPORT DRAM

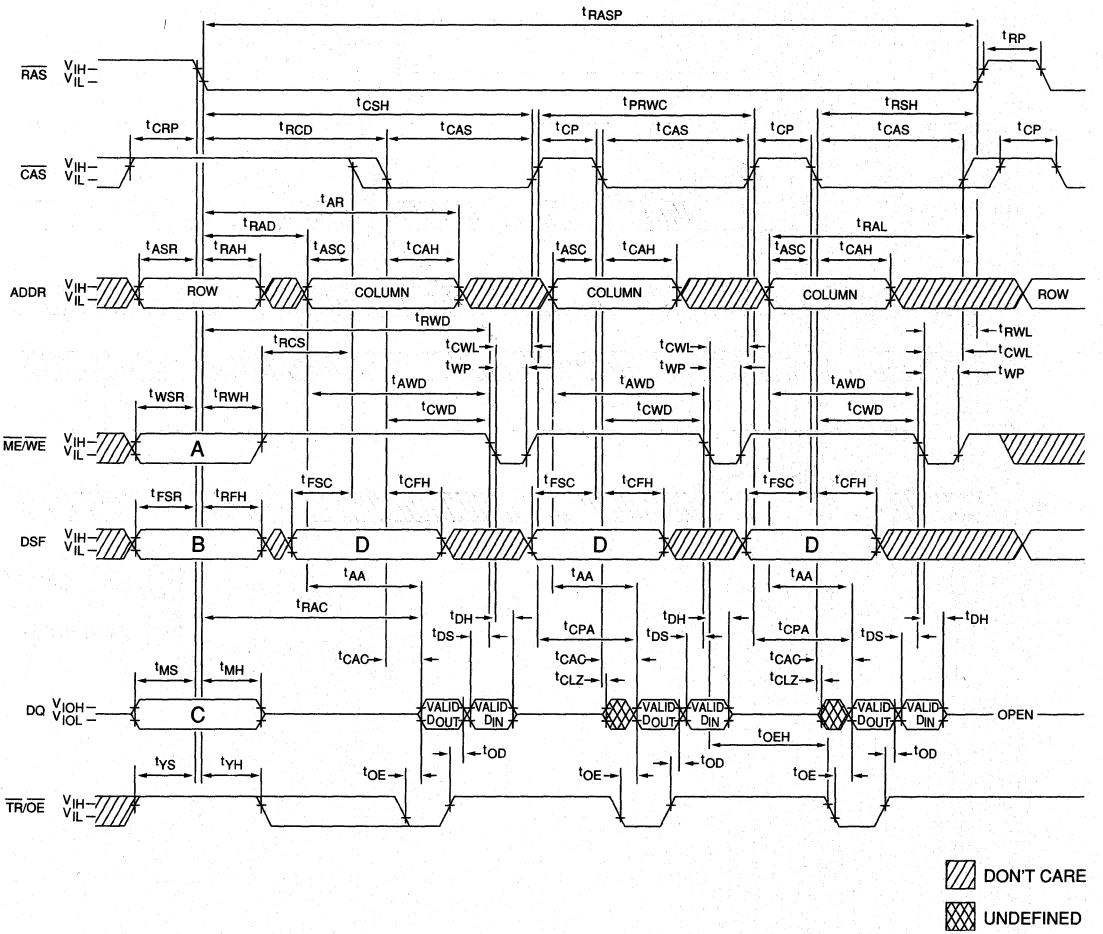
NEW ■ MULTIPORT DRAM

DRAM FAST-PAGE-MODE EARLY-WRITE CYCLE [1, 2]



NOTE: 1. READ cycles or READ-MODIFY-WRITE cycles can be mixed with WRITE cycles while in FAST PAGE MODE.
2. The logic states of "A", "B", "C", "D" and "E" determine the type of WRITE operation performed. See the Write Cycle Function Table for a detailed description.

DRAM FAST-PAGE-MODE READ-WRITE CYCLE [1, 2]
(READ-MODIFY-WRITE OR LATE-WRITE CYCLES)



NOTE:
1. READ or WRITE cycles can be mixed with READ-MODIFY-WRITE cycles while in FAST PAGE MODE. Use the Write Function Table to determine the proper DSF state for the desired WRITE operation.
2. The logic states of "A", "B" , "C" and "D" determine the type of WRITE operation performed. See the Write Cycle Function Table for a detailed description.

NEW ■ MULTIPORT DRAM

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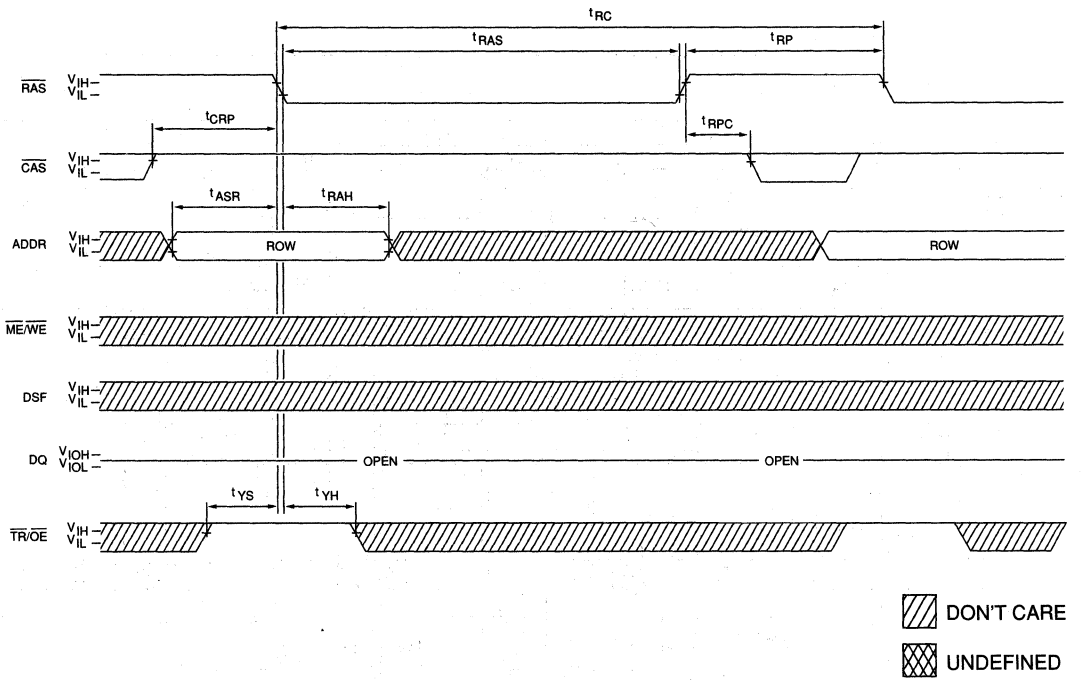
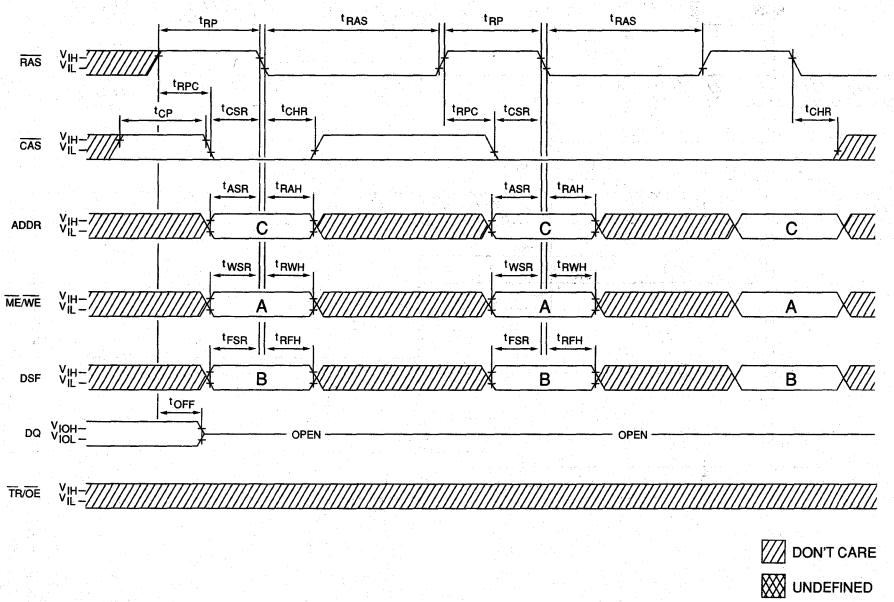
DRAM $\overline{\text{RAS}}$-ONLY REFRESH CYCLE
(ADDR = A0-A8)



CAS-BEFORE-RAS CYCLE FUNCTION TABLE

FUNCTION	CODE	LOGIC STATES		
		RAS Falling Edge (CAS = LOW)		
		A ME/WE	B DSF	C A0-A8
CAS-BEFORE-RAS REFRESH (Reset All Options)	CBRR	X	0	X
CAS-BEFORE-RAS REFRESH (Set/Reset Stop Address)	CBRS	0	1	STOP ADDRESS[1]
CAS-BEFORE-RAS REFRESH (No Reset)	CBRN	1	1	X

CAS-BEFORE-RAS REFRESH CYCLE [2]



NOTE: 1. Programmable Stop Point column addresses:

Number Stop Points/Half	Address @ RAS LOW					Number and Size of Partition(s)
	A8	A7	A6	A5	A4	
1 (Default)	X	1	1	1	1	1 x 256
2	X	0	1	1	1	2 x 128
4	X	0	0	1	1	4 x 64
8	X	0	0	0	1	8 x 32
16	X	0	0	0	0	16 x 16

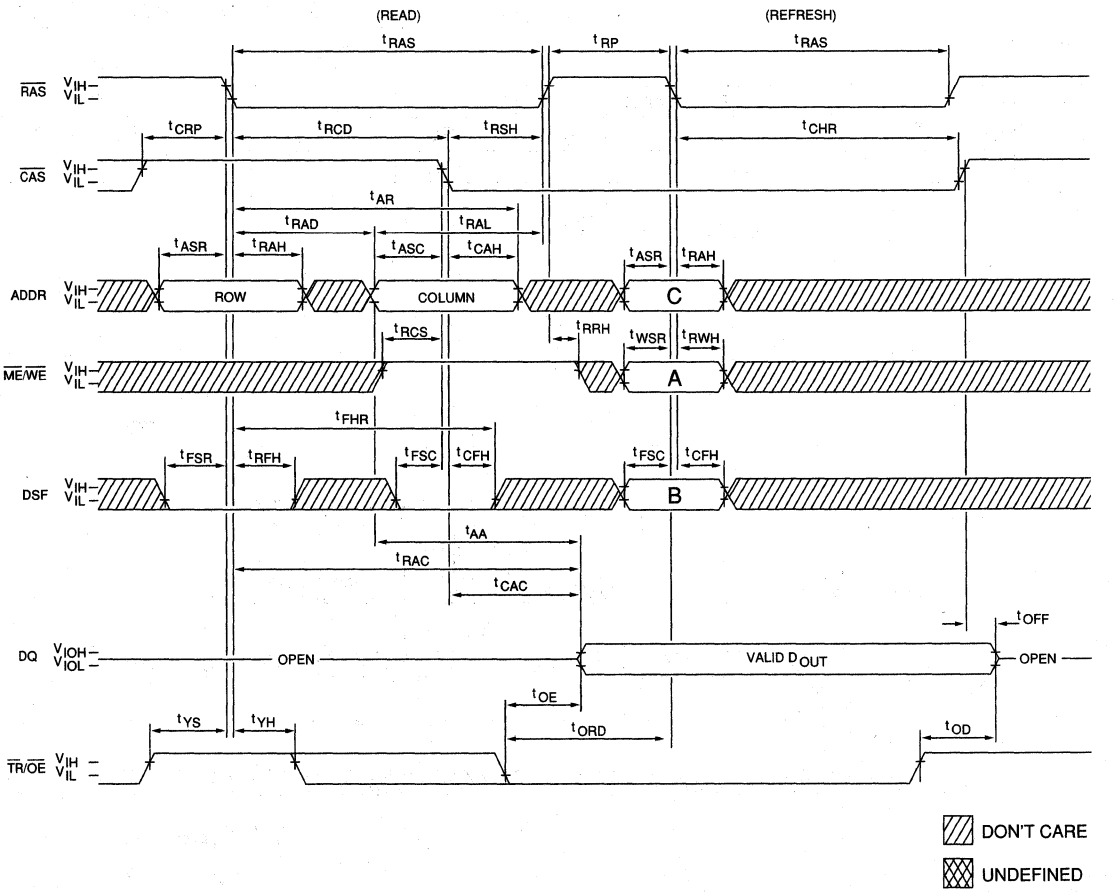
A0-A3 = "don't care"

2. The logic states of "A", "B" and "C" determine the type of CBR operation performed. See the CBR Cycle Function Table for a detailed description.

NEW MULTIPORT DRAM

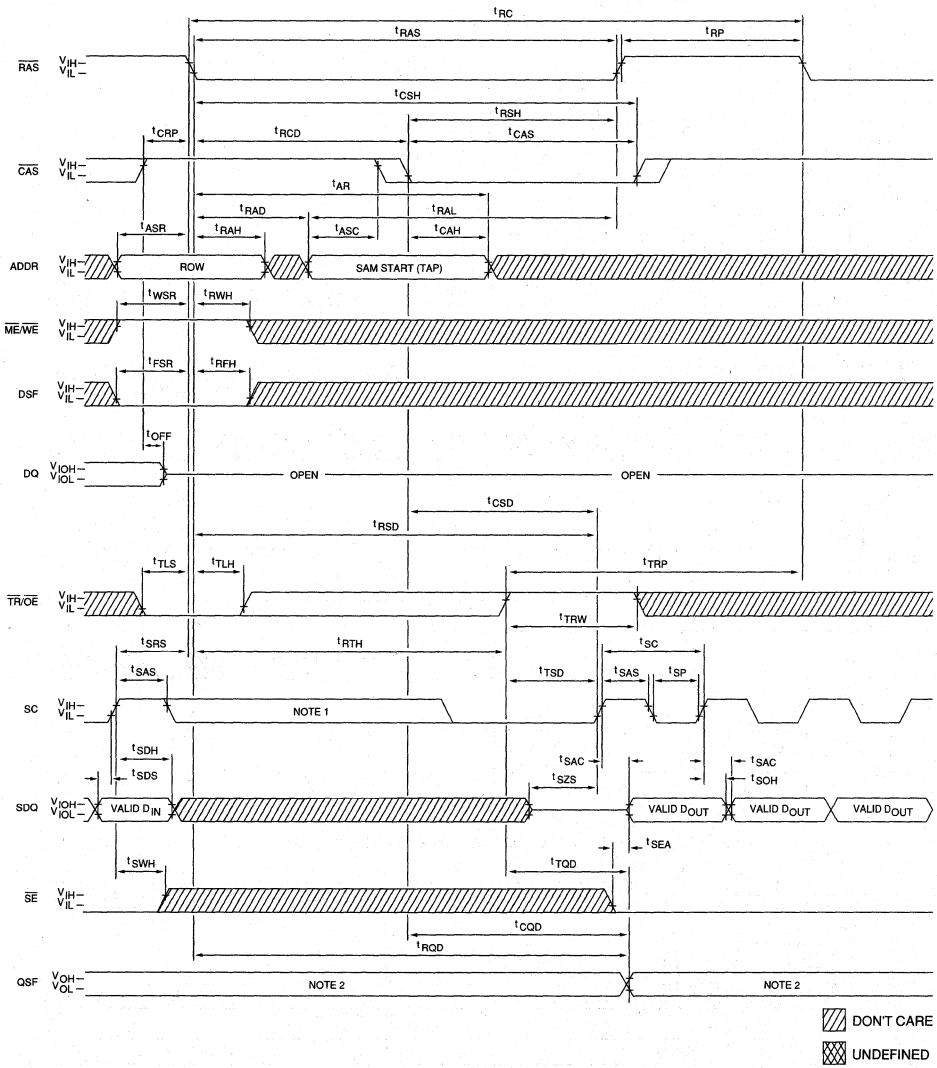
NEW ■ MULTIPORT DRAM

DRAM HIDDEN-REFRESH CYCLE [1, 2]



NOTE:
1. A HIDDEN REFRESH may also be performed after a WRITE or TRANSFER cycle. In this case $\overline{ME}/\overline{WE}$ = LOW (when $\overline{CAS}$ goes LOW) and $\overline{TR}/\overline{OE}$ = HIGH. In the TRANSFER case, $\overline{TR}/\overline{OE}$ = LOW (when $\overline{RAS}$ goes LOW) and the DQ pins stay High-Z during the refresh period, regardless of $\overline{TR}/\overline{OE}$.
2. The logic states of "A", "B" and "C" determine the type of CBR operation performed. See the CBR Cycle Function Table for a detailed description.

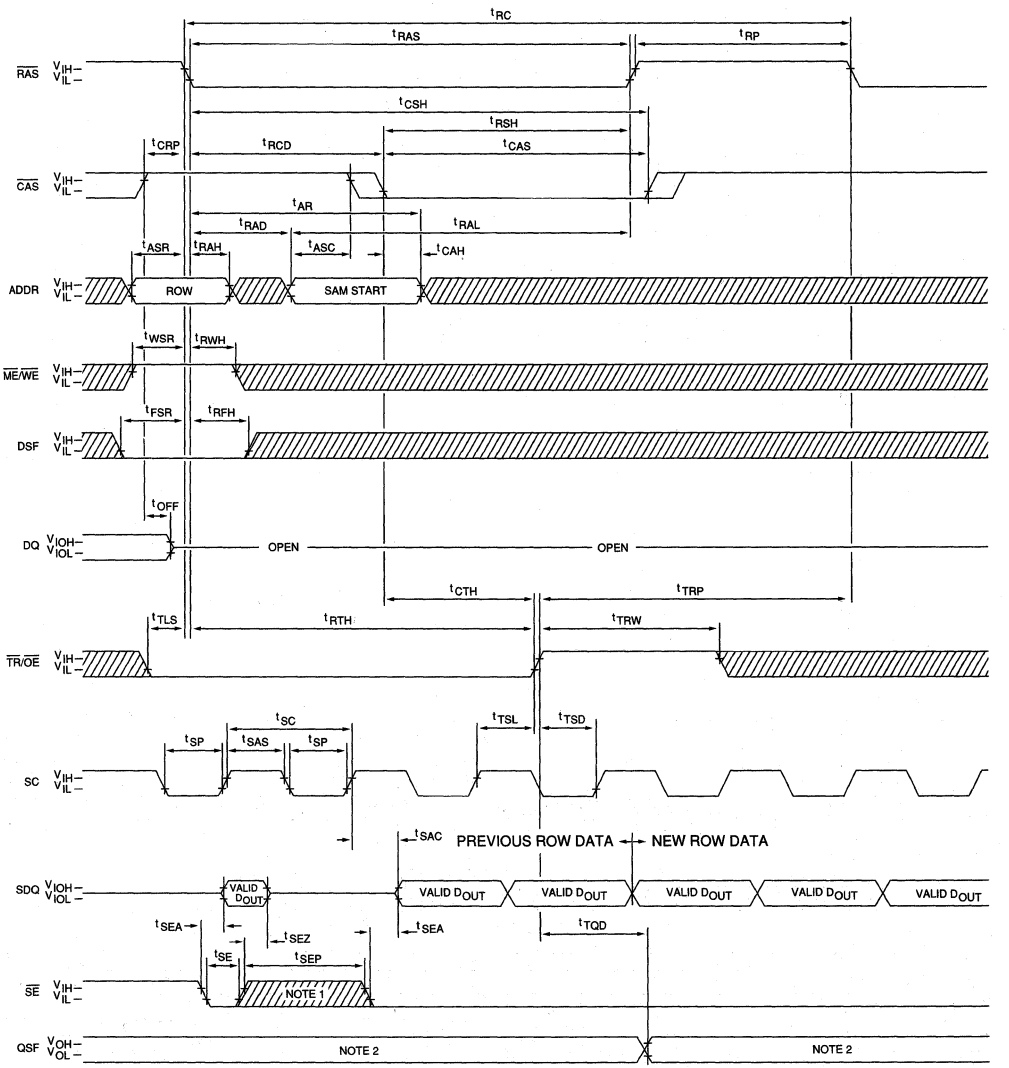
READ TRANSFER
(DRAM-TO-SAM TRANSFER)
(When part was previously in the SERIAL INPUT mode, or SC idle)



NOTE:
1. There must be no rising edges on the SC input during this time period.
2. QSF = 0 when the Lower SAM (bits 0–255) is being accessed.
   QSF = 1 when the Upper SAM (bits 256–511) is being accessed.
3. If tTLH is timing for the $\overline{TR}/(\overline{OE})$ rising edge, the transfer is self-timed and the tCSD and tRSD times must be met. If tRTH is timing for the $\overline{TR}/(\overline{OE})$ rising edge, the transfer is done off of the $\overline{TR}/(\overline{OE})$ rising edge and tTSD must be met.

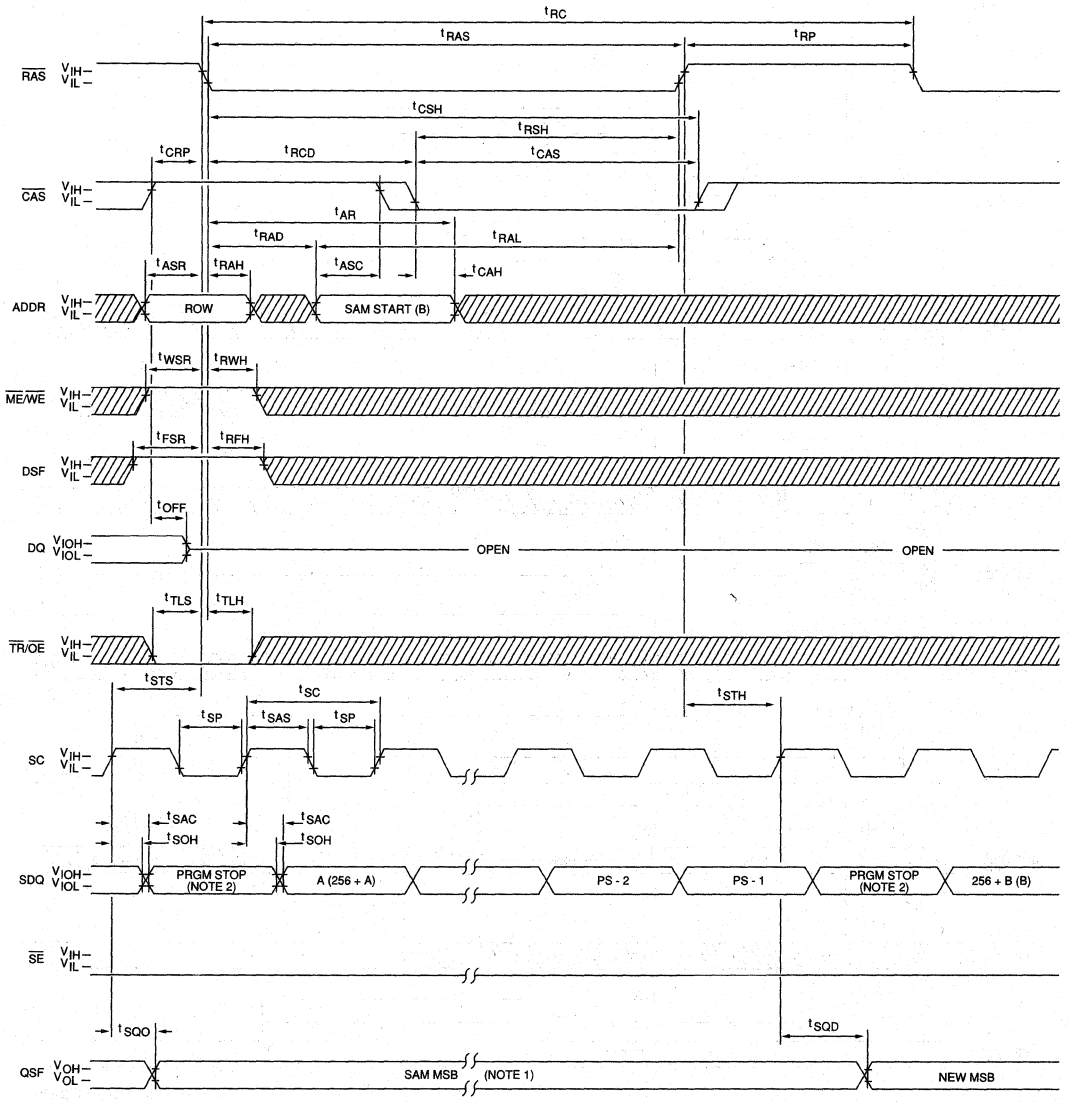
NEW ■ MULTIPORT DRAM

REAL-TIME READ TRANSFER
(DRAM-TO-SAM TRANSFER)
(When part was previously in the SERIAL OUTPUT mode)



NOTE: 1. The $\overline{SE}$ pulse is shown to illustrate the SERIAL OUTPUT ENABLE and DISABLE timing. It is not required.
2. QSF = 0 when the Lower SAM (bits 0–255) is being accessed.
QSF = 1 when the Upper SAM (bits 256–511) is being accessed.

SPLIT READ TRANSFER
(SPLIT DRAM-TO-SAM TRANSFER)

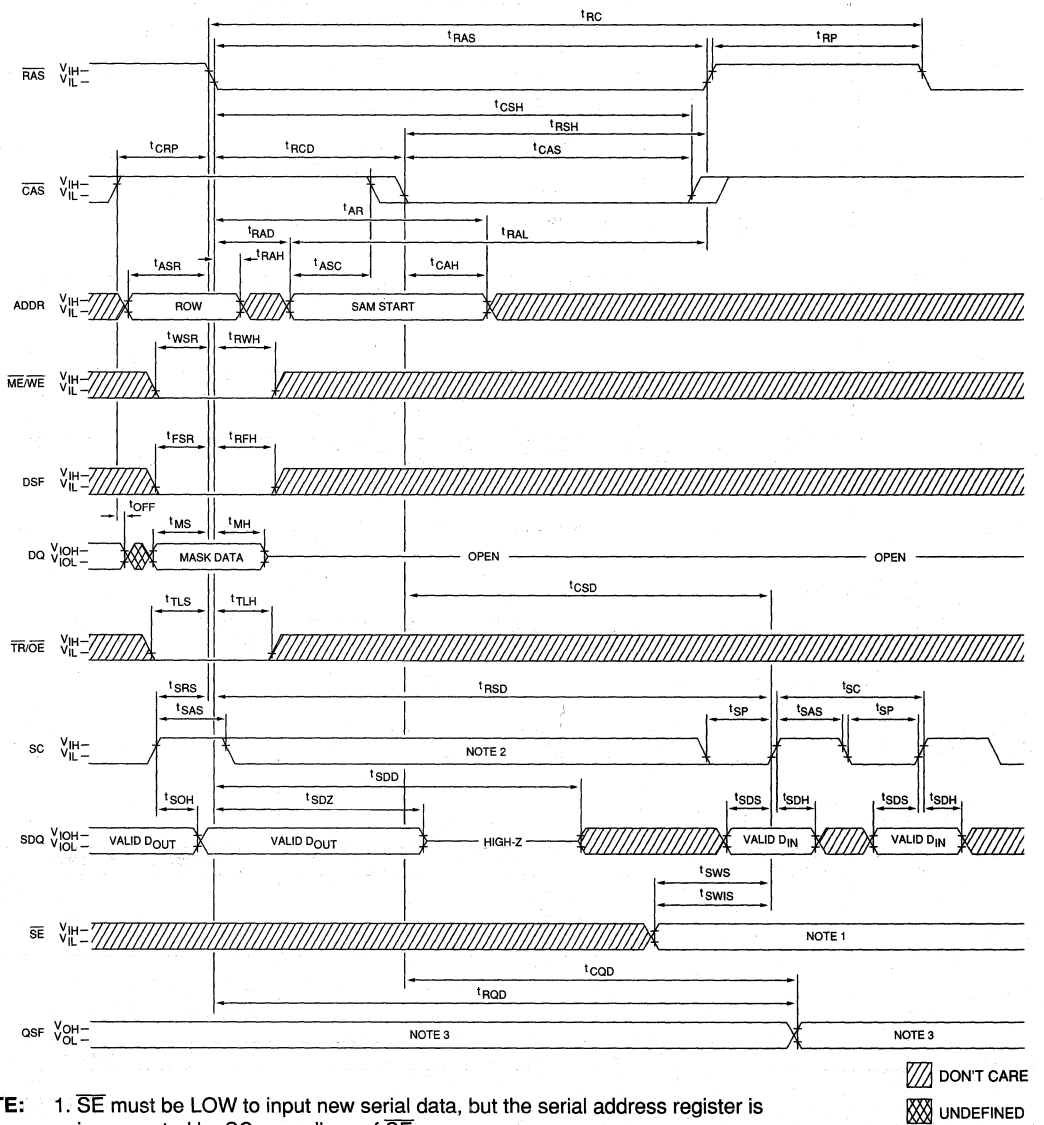


NOTE: 1. QSF = 0 when the Lower SAM (bits 0–255) is being accessed.
QSF = 1 when the Upper SAM (bits 256–511) is being accessed.
2. Programmable stop address or SAM half boundary (255 or 511). See the Programmable Split SAM functional description for detail.

NEW ■ MULTIPORT DRAM

MASKED WRITE TRANSFER
(SAM-TO-DRAM TRANSFER)

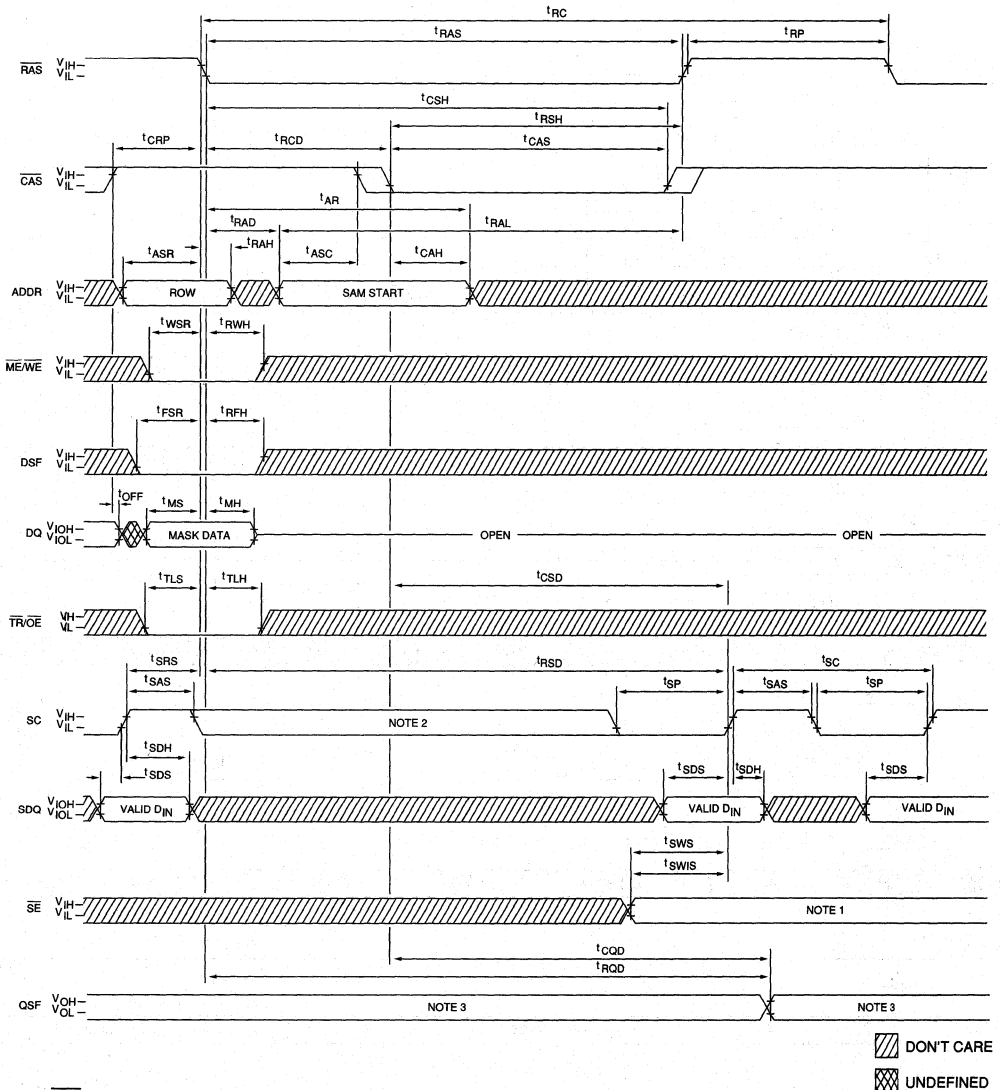
(When part was previously in the SERIAL OUTPUT mode)



NOTE:
1. $\overline{SE}$ must be LOW to input new serial data, but the serial address register is incremented by SC regardless of $\overline{SE}$.
2. There must be no rising edges on the SC input during this time period.
3. QSF = 0 when the Lower SAM (bits 0–255) is being accessed.
   QSF = 1 when the Upper SAM (bits 256–511) is being accessed.

MASKED WRITE TRANSFER (SAM-TO-DRAM TRANSFER)

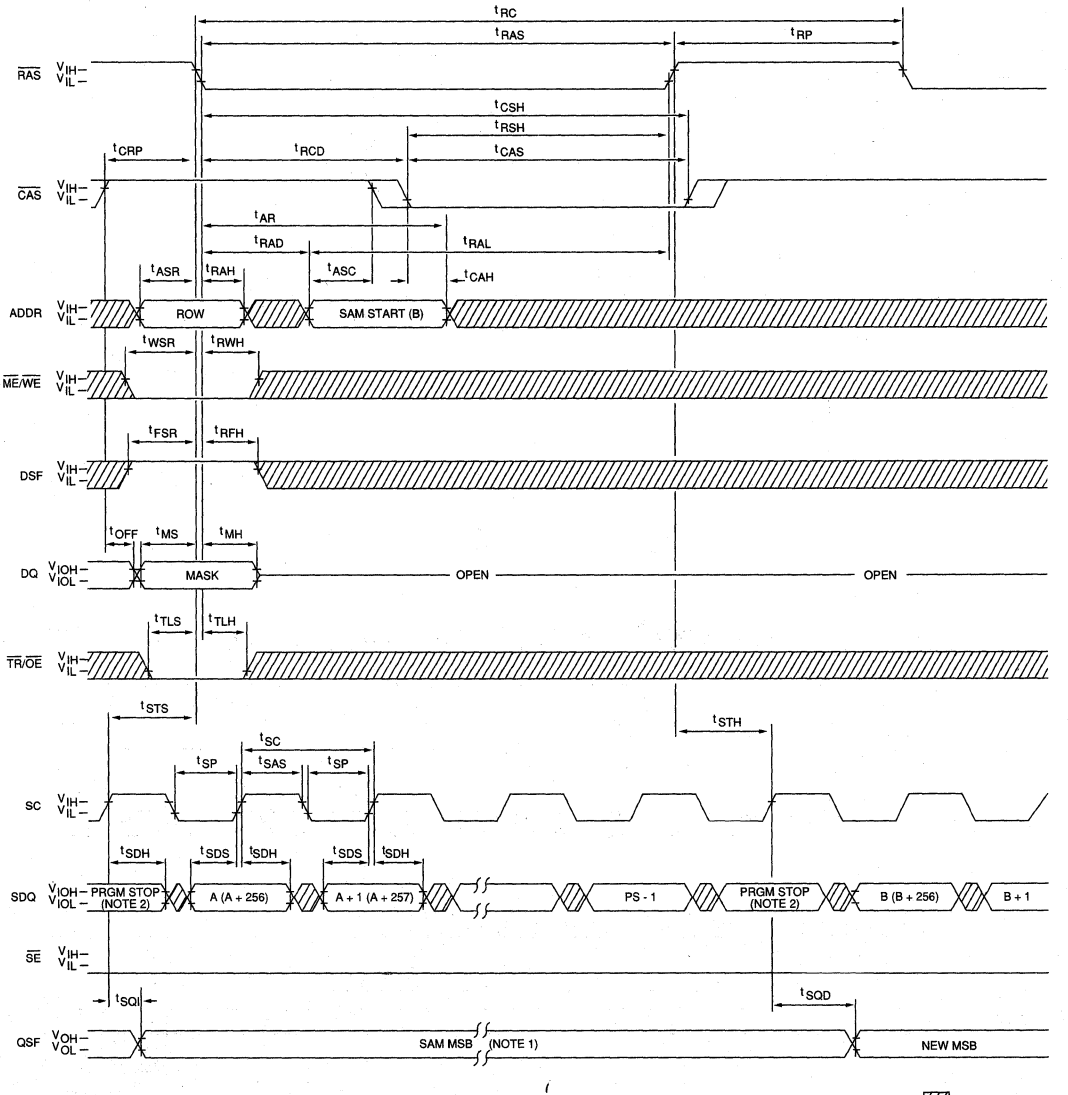
(When part was previously in the SERIAL INPUT mode)



NOTE:
1. $\overline{SE}$ must be LOW to input new serial data, but the serial address register is incremented by SC regardless of $\overline{SE}$.
2. There must be no rising edges on the SC input during this time period.
3. QSF = 0 when the Lower SAM (bits 0–255) is being accessed.
   QSF = 1 when the Upper SAM (bits 255–511) is being accessed.

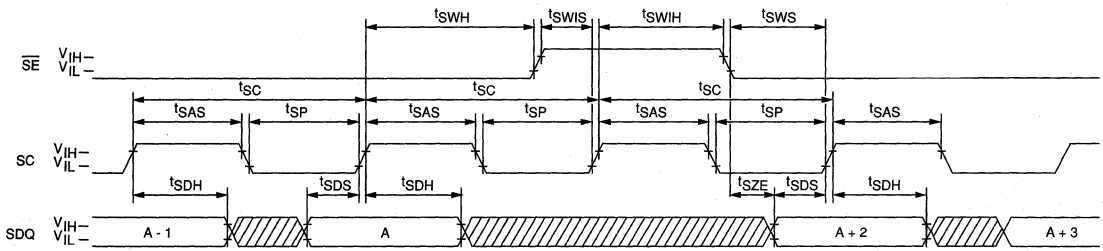
NEW ■ MULTIPORT DRAM

MASKED SPLIT WRITE TRANSFER (SAM-TO-DRAM TRANSFER)

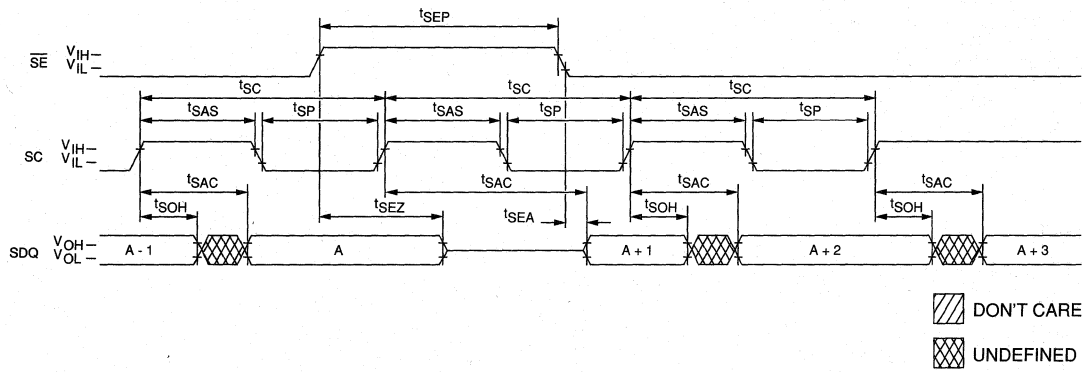


NOTE: 1. QSF = 0 when the Lower SAM (bits 0–255) is being accessed.
QSF = 1 when the Upper SAM (bits 256–511) is being accessed.
2. Programmable stop address or SAM half boundary (255 or 511). See the Programmable Split SAM functiona description for detail.

SAM SERIAL INPUT



SAM SERIAL OUTPUT



NEW ■ MULTIPORT DRAM

VRAM

256K x 16 DRAM WITH 512 x16 SAM

NEW ■ MULTIPORT DRAM

FEATURES

- Industry standard pinout, timing, and functions
- High-performance, CMOS silicon-gate process
- Single +5V ±10% power supply
- Inputs and outputs are fully TTL compatible
- Refresh modes: $\overline{RAS}$ ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$ (CBR) and HIDDEN
- 512-cycle refresh within 32ms
- FAST PAGE MODE access with Extended Data Out
- Upper and lower byte $\overline{WE}$ control
- Dual port organization: 256K x 16 DRAM port
  512 x 16 SAM port
- No refresh required for serial access memory
- Low power: 10mW standby; 350mW active, typical
- Fast access times – 60ns random, 15ns serial

SPECIAL FUNCTIONS

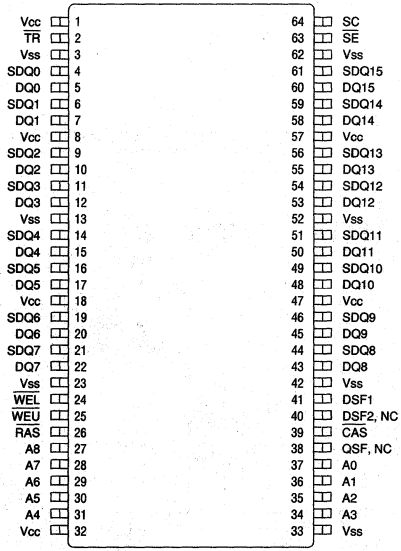
- JEDEC Standard Mandatory Function set plus
- PERSISTENT MASKED WRITE
- 4 or 8 COLUMN BLOCK WRITE (MASK)
- MASKED FLASH WRITE
- MASKED WRITE TRANSFER/SERIAL INPUT
- MASKED SPLIT WRITE TRANSFER
- PROGRAMMABLE SPLIT SAM

OPTIONS MARKING

- Timing [DRAM, SAM (cycle/access)]
  60ns, 18/15ns -6
  70ns, 25/20ns -7
  80ns, 30/25ns -8
- Packages
  Plastic SOP (550 mil) SG

PIN ASSIGNMENT (Top View)

64-Pin SOP



GENERAL DESCRIPTION

The MT42C256K16A1 is a high speed, dual port CMOS dynamic random access memory, or video RAM (VRAM) containing 4,194,304 bits. These bits may be accessed by an 16-bit wide DRAM port or by a 512 x 16 bit serial access memory (SAM) port. Data may be transferred bidirectionally between the DRAM and the SAM.

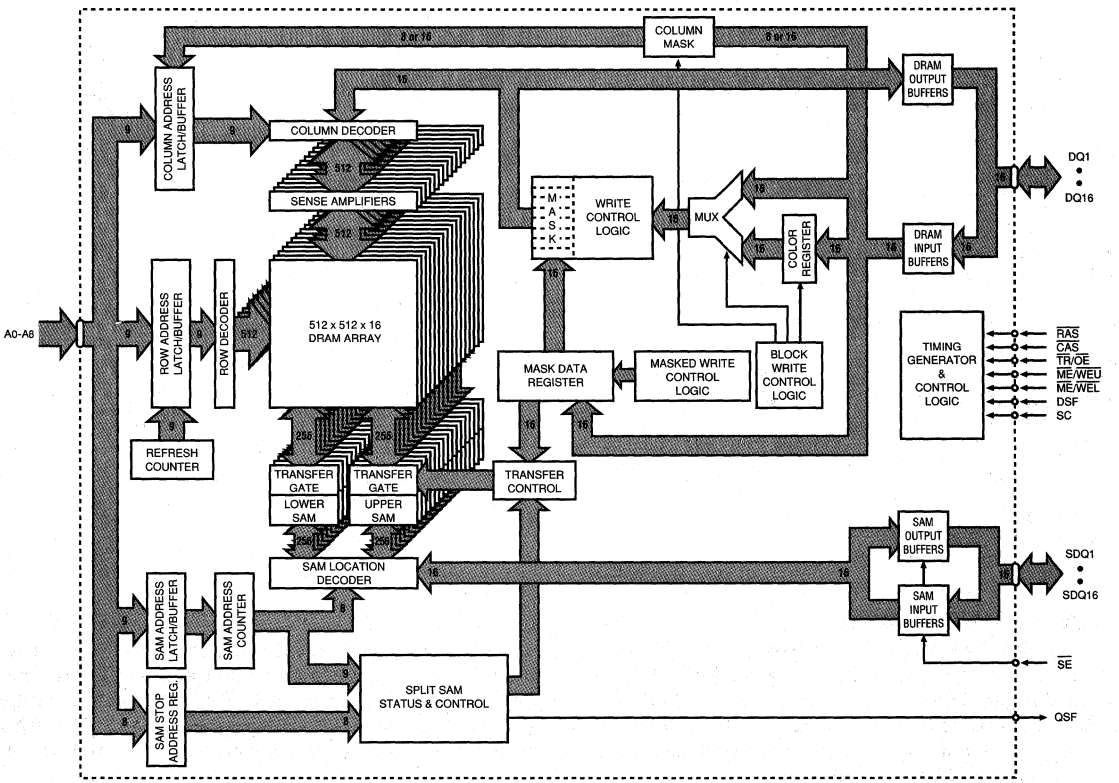
The DRAM portion of the VRAM is functionally identical to the MT4C4256 (256K x 4-bit DRAM), with the addition of MASKED WRITE, BLOCK WRITE and FLASH WRITE. Sixteen 512-bit data registers make up the serial access memory portion of the VRAM. Data I/O and internal data transfer are accomplished using three separate bidirectional data paths: the 16-bit random access I/O port, the 16 internal 512 bit wide paths between the DRAM and the SAM, and the 16-bit serial I/O port for the SAM. The rest of the circuitry consists of the control, timing, and address decoding logic.

Each of the ports may be operated asynchronously and independently of the other except when data is being transferred internally between them. As with all DRAMs, the VRAM must be refreshed to maintain data. The refresh cycles must be timed so that all 512 combinations of $\overline{RAS}$

addresses are executed at least every 32ms (regardless of sequence). Micron recommends evenly spaced refresh cycles for maximum data integrity. An internal transfer between the DRAM and the SAM counts as a refresh cycle. The SAM portion of the VRAM is fully static and does not require any refresh.

The operation and control of the MT42C256K16A1 are optimized for high performance graphics and communication designs. The dual port architecture is well suited to buffering the sequential data types used in raster graphics display, serial, parallel networking and data communications. Special features such as SPLIT READ TRANSFER, Extended Data Out and BLOCK WRITE allow further enhancements to system performance.

FUNCTIONAL BLOCK DIAGRAM



TRIPLE PORT DRAM

256K x 4 DRAM WITH DUAL 512 x 4 SAMS

FEATURES

- Three asynchronous, independent, data access ports
- Fast access times – 80ns random, 25ns serial
- Operation and control compatible with 1 Meg VRAM
- High-performance, CMOS silicon-gate process
- Inputs and outputs are fully TTL compatible
- Low power: 15mW standby; 500mW active, typical
- 512-cycle refresh within 8ms
- Refresh modes: RAS-ONLY, CAS-BEFORE-RAS (CBR) and HIDDEN
- FAST PAGE MODE access cycles
- Two bidirectional serial access memories (SAMs)
- Fully static SAM and Mask Register, no refresh required
- 2,048-bit Bit Mask Register
- SERIAL MASK DATA INPUT mode

SPECIAL FUNCTIONS

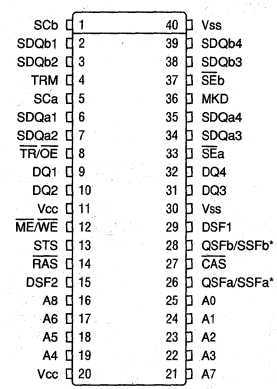
- MASKED WRITE (Write-Per-Bit)
- PERSISTENT MASKED WRITE
- SPLIT READ and WRITE TRANSFERs
- BLOCK WRITE
- BIT MASKED TRANSFERs

OPTIONS MARKING

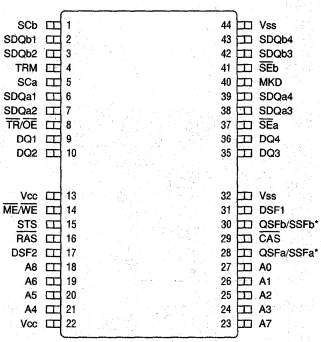
- Timing [DRAM, SAMs (cycle/access)]
  - 80ns, 28ns/25ns - 8
  - 100ns, 30ns/27ns -10
- Packages
  - Plastic SOJ (400 mil) DJ
  - Plastic TSOP (400 mil) TG
- Functionality
  - QSF output MT43C4257
    (indicates SAM-half accessed)
  - SSF input MT43C4258
    (Split SAM special function, stop count)

PIN ASSIGNMENT (Top View)

40-Pin SOJ
(Q-6)



40/44-Pin TSOP**
(R-5)



*MT43C4257/MT43C4258
**Consult factory for TSOP availability.

GENERAL DESCRIPTION

The MT43C4257/8 are high speed, triple port CMOS lynamic random access memories (TPDRAMs) containing ,048,576 bits. Data may be accessed by a 4 bit wide DRAM ›ort or by either of two independently-clocked 512 x 4-bit erial access memory (SAM) ports. Data may be transferred idirectionally between the DRAM and either SAM.

The DRAM portion of the TPDRAM is functionally identical to the MT4C4256 (256K x 4 DRAM). Eight 512-bit data registers make up the serial access memory portions of the TPDRAM. Data I/O and internal data transfer are accomplished using five separate bidirectional data paths; the 4-bit random access I/O port, the pair of internal 2,048 bit

wide paths between the DRAM and the SAMs, and the pair of 4-bit serial I/O ports for the SAMs. The rest of the circuitry consists of the control, timing and address decoding logic.

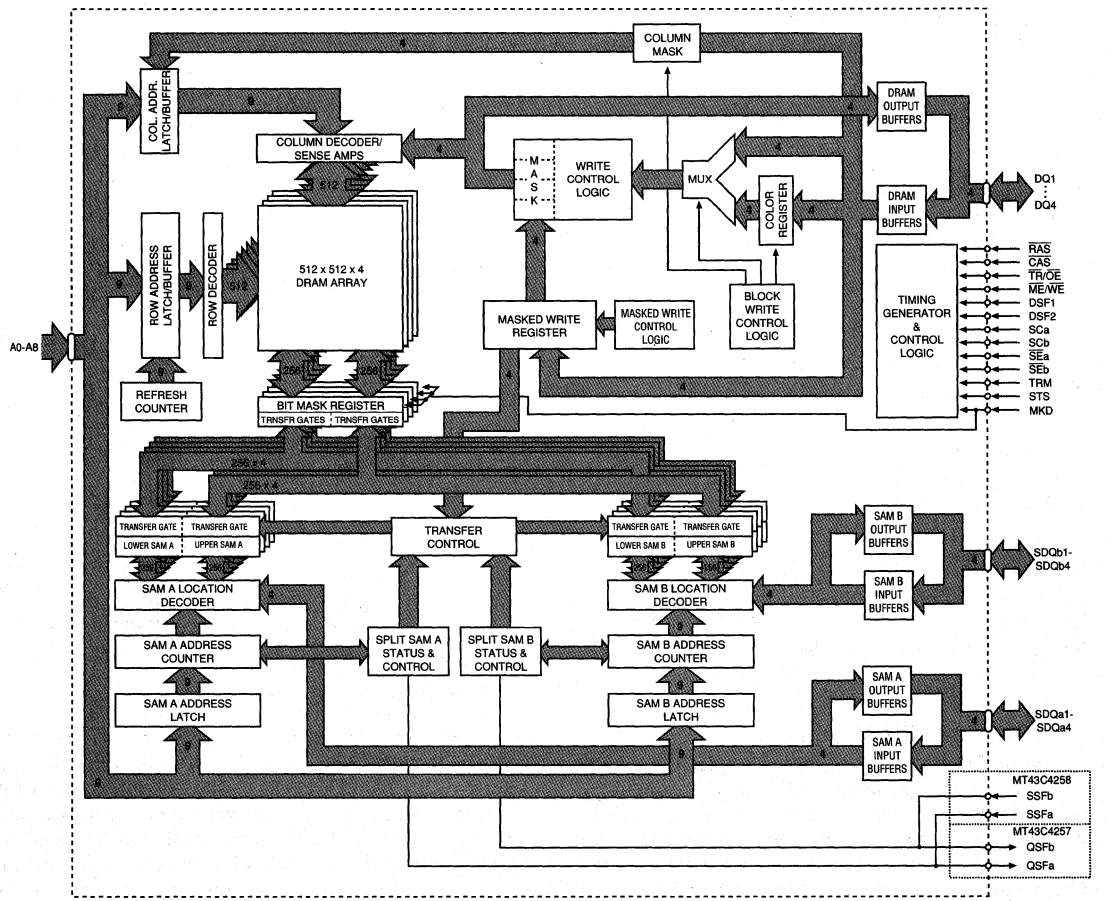
All three ports may be operated asynchronously and independently of the others except when data is being internally transferred between the DRAM and either SAM.

Each of the 2,048 bits involved in an internal transfer may be individually masked by performing a BIT MASKED TRANSFER operation. The 512 x 4-bit Bit Mask Data register can be parallel loaded from the DRAM or either SAM, or serial loaded through the MKD serial input.

As with all DRAMs, the TPDRAM must be refreshed to maintain data. The refresh cycles must be timed so that all 512 combinations of $\overline{RAS}$ addresses are executed at least every 8ms (regardless of sequence). Micron recommends evenly spaced refresh cycles for maximum data integrity. An internal transfer between the DRAM and either SAM counts as a refresh cycle. The SAM portions of the TPDRAM are fully static and do not require refresh.

The operation and control of the MT43C4257/8 are optimized for high performance graphics and communication designs. The triple port architecture is well suited to buffering the sequential data types used in raster graphics display, serial/parallel networking and data communications. Special features such as SPLIT READ TRANSFER, BIT MASKED TRANSFERs and BLOCK WRITE allow further enhancements to system performance.

FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTIONS

SOJ PIN NUMBERS	TSOP PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
5	5	SCa	Input	Serial Clock, SAMa: Clock input to the serial address counter for the SAMa registers and strobe for SAMa control and data inputs.
1	1	SCb	Input	Serial Clock, SAMb: Clock input to the serial address counter for the SAMb registers and strobe for SAMb control and data inputs.
8	8	$\overline{TR/OE}$	Input	Transfer Enable: Enables an internal TRANSFER operation at the falling edge of $\overline{RAS}$, or Output Enable: Enables the DRAM output buffers when taken LOW after $\overline{RAS}$ goes LOW ($\overline{CAS}$ must also be LOW), otherwise the output buffers are in a high impedance state.
12	14	$\overline{ME/WE}$	Input	Mask Enable: If $\overline{ME/WE}$ is LOW at the falling edge of $\overline{RAS}$, a MASKED WRITE cycle is performed, or Write Enable: $\overline{ME/WE}$ is also used to select a READ ($\overline{ME/WE}$ = H) or WRITE ($\overline{ME/WE}$ = L) cycle when accessing the DRAM. This includes a READ TRANSFER ($\overline{ME/WE}$ = H) or WRITE TRANSFER ($\overline{ME/WE}$ = L).
33	37	$\overline{SE}$a	Input	Serial Port Enable SAMa: $\overline{SE}$a enables Port A serial I/O buffers and allows a serial READ or WRITE operation to occur; otherwise, the output buffers are in a High-Z state. $\overline{SE}$a is also used during a TRANSFER operation to indicate whether a WRITE TRANSFER or a SERIAL-INPUT-MODE ENABLE (PSEUDO WRITE TRANSFER) cycle is performed.
37	41	$\overline{SE}$b	Input	Serial Port Enable, SAMb: $\overline{SE}$b enables Port B serial I/O buffers and allows a serial READ or WRITE operation to occur; otherwise, the output buffers are in a High-Z state. $\overline{SE}$b is also used during a TRANSFER operation to indicate whether a WRITE TRANSFER or a SERIAL-INPUT-MODE ENABLE (PSEUDO WRITE TRANSFER) cycle is performed.
29	31	DSF1	Input	Special Function (Control) 1: DSF1 is used to indicate which special functions are used on a particular access or transfer cycle. See the Functional Truth Table for a detailed description.
15	17	DSF2	Input	Special Function (Control) 2: DSF2 is used to indicate which special functions are used on a particular access or transfer cycle. See the Functional Truth Table for a detailed description.
14	16	$\overline{RAS}$	Input	Row Address Strobe: $\overline{RAS}$ is used to clock-in the 9 row-address bits and as a strobe for control and data inputs.
27	29	$\overline{CAS}$	Input	Column Address Strobe: $\overline{CAS}$ is used to clock-in the 9 column-address bits, enable the DRAM output buffers (along with $\overline{TR/OE}$), and strobe control and data inputs.

PIN DESCRIPTIONS (continued)

SOJ PIN NUMBERS	TSOP PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
25, 24, 23, 22, 19, 18, 17, 21, 16	27, 26, 25, 24, 21, 20, 19, 23, 18	A0-A8	Input	Address Inputs: For DRAM operation, these inputs are multiplexed and clocked by $\overline{RAS}$ and $\overline{CAS}$ to select one 4-bit word out of the 256K available. During TRANSFER operations, A0 to A8 indicate the DRAM row being accessed (when $\overline{RAS}$ goes LOW) and the SAM start address (when $\overline{CAS}$ goes LOW).
13	15	STS	Input	SAM Transfer Select: The state of STS at $\overline{RAS}$ time determines which SAM is involved in a transfer (SAMa = LOW, SAMb = HIGH).
36	40	MKD	Input	Mask Data Input: MKD is used during BIT MASK REGISTER LOAD cycles to enable or disable the serial mask input mode (SMI). If SMI is enabled (MKD = HIGH at $\overline{RAS}$), then MKD is used as mask data input and is clocked by SCb into the mask data register.
4	4	TRM	Input	Transfer Mask Select: TRM is used to select between NORMAL TRANSFER cycles and BIT MASKED TRANSFER or BIT MASK REGISTER LOAD cycles.
9, 10, 31, 32	9, 10, 35, 36	DQ1-DQ4	Input/ Output	DRAM Data I/O: Data inputs and outputs for the DRAM memory array; inputs for the MASK and COLOR REGISTER load cycles; address mask inputs for BLOCK WRITE cycles.
6, 7, 34, 35	6, 7, 38, 39	SDQa1-SDQa4	Input/ Output	Serial Data I/O, SAMa: Input, Output, or High-Z.
2, 3, 38, 39	2, 3, 42, 43	SDQb1-SDQb4	Input/ Output	Serial Data I/O, SAMb: Input, Output, or High-Z.
26	28	QSFa/SSFa	Output Input	Split SAM Status, SAMa (MT43C4257): QSFa indicates which half of SAMa is being accessed (Lower = LOW, Upper = HIGH). Split SAM Special Function, SAMa (MT43C4258): SSFa = HIGH stops access to current half of SAM and will load the Tap address of the next half into the address pointer. SSFa is synchronized with SCa.
28	30	QSFb/SSFb	Output Input	Split SAM Status, SAMb (MT43C4257): QSFb indicates which half of SAMb is being accessed (Lower = LOW, Upper = HIGH). Split SAM Special Function, SAMb (MT43C4258): SSFb = HIGH stops access to current half of SAM and will load the Tap address of the next half into the address pointer. SSFb is synchronized with SCb.
11, 20	13, 22	Vcc	Supply	Power Supply: +5V ±5%
30, 40	32, 44	Vss	Supply	Ground

FUNCTIONAL DESCRIPTION

The MT43C4257/8 may be divided into four functional blocks: the DRAM and its special functions, the bit mask register (BMR), the two serial access memories (SAMs), and the DRAM/SAM/BMR transfer circuitry. All the operations described below are also shown in the AC Timing Diagrams section of this data sheet and are summarized in the Functional Truth Table.

Note: *For dual function pins, the function that is not being discussed will be surrounded by parentheses. For example, the $\overline{TR}/(\overline{OE})$ pin will be shown as $\overline{TR}/(\overline{OE})$ in references to transfer operations.*

DRAM OPERATION

This section describes the operation of the random access port and the special functions associated with the DRAM.

DRAM REFRESH (ROR, CBR, and HR)

Like any DRAM-based memory, the MT43C4257/8 TPDRAM must be refreshed to retain data. All 512 row address combinations must be accessed within 8ms. The MT43C4257/8 support $\overline{CAS}$-BEFORE-$\overline{RAS}$, $\overline{RAS}$ ONLY and HIDDEN types of refresh cycles.

For the $\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH cycle, the row-addresses are generated and stored in an internal address counter. The user need not supply any address data and simply must perform 512 $\overline{CAS}$-BEFORE-$\overline{RAS}$ cycles within the 8ms time period.

For $\overline{RAS}$-ONLY REFRESH cycles, the refresh address must be generated externally and applied to the A0-A8 inputs. The DQ pins remain in a High-Z state for both the $\overline{RAS}$-ONLY and $\overline{CAS}$-BEFORE-$\overline{RAS}$ cycles.

HIDDEN REFRESH (HR) cycles are performed by toggling $\overline{RAS}$ (while keeping $\overline{CAS}$ LOW) after a READ or WRITE cycle. This performs $\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH cycles but does not disturb the DQ lines.

Any DRAM READ, WRITE, or TRANSFER cycle also refreshes the DRAM row that is being accessed. The SAM and BMR portions of the MT43C4257/8 are fully static and do not require any refreshing.

DRAM READ AND WRITE CYCLES (RW)

The DRAM portion of the TPDRAM is nearly identical to standard 256K x 4 DRAMs. However, because several of the DRAM control pins are used for additional functions on this device, several conditions that were undefined or "don't care" states for the DRAM are specified for the TPDRAM. These conditions are highlighted in the following discussion. In addition, the TPDRAM has several special functions that may be used when writing to the DRAM.

The 18 address bits used to select a 4-bit word from the 262,144 available are latched into the chip using the A0-A8, $\overline{RAS}$, and $\overline{CAS}$ inputs. First, the 9 row-address bits are set up on the address inputs and clocked into the part when $\overline{RAS}$ transitions from HIGH-to-LOW. Next, the 9 column-address bits are set up on the address inputs and clocked-in when $\overline{CAS}$ goes from HIGH-to-LOW.

Note: *$\overline{RAS}$ also acts as a "master" chip enable for the TPDRAM. If $\overline{RAS}$ is inactive, HIGH, all other DRAM control pins ($\overline{CAS}$, $\overline{TR}/\overline{OE}$, $\overline{ME}/\overline{WE}$, etc.) are a "don't care" and may change state without effect. No DRAM or TRANSFER cycles will be initiated without $\overline{RAS}$ falling.*

For single port DRAMS, the $\overline{OE}$ pin is a "don't care" when $\overline{RAS}$ goes LOW. For the TPDRAM, $\overline{TR}/(\overline{OE})$ is used when $\overline{RAS}$ goes LOW to select between DRAM and TRANSFER cycles. $\overline{TR}/(\overline{OE})$ must be HIGH at the $\overline{RAS}$ HIGH-to-LOW transition for all DRAM operations.

If $(\overline{ME})/\overline{WE}$ is HIGH when $\overline{CAS}$ goes LOW, a DRAM READ operation is performed and the data from the memory cells selected will appear at the DQ1-DQ4 port. The $(\overline{TR})/\overline{OE}$ input must transition from HIGH-to-LOW some time after $\overline{RAS}$ falls to enable the DRAM output port.

For single port DRAMs, $\overline{WE}$ is a "don't care" when $\overline{RAS}$ goes LOW. For the TPDRAM, $\overline{ME}/(\overline{WE})$ is used, when $\overline{RAS}$ goes LOW, to select between a MASKED WRITE cycle or a normal WRITE cycle. If $\overline{ME}/(\overline{WE})$ is LOW at the $\overline{RAS}$ HIGH-to-LOW transition, a MASKED WRITE operation is selected. For any TPDRAM non-masked access cycle (READ or WRITE), $\overline{ME}/(\overline{WE})$ must be HIGH at the $\overline{RAS}$ HIGH-to-LOW transition. If $(\overline{ME})/\overline{WE}$ is LOW when $\overline{CAS}$ goes LOW, a DRAM WRITE operation is performed and the data present on the DQ1-DQ4 data port will be written into the selected memory cells.

The TPDRAM can perform all the normal DRAM cycles: READ, EARLY-WRITE, LATE-WRITE, READ-MODIFY-WRITE, FAST-PAGE-MODE READ, FAST-PAGE-MODE WRITE, and FAST-PAGE-MODE READ-MODIFY-WRITE. Refer to the AC timing parameters and diagrams in the data sheet for more details on these operations.

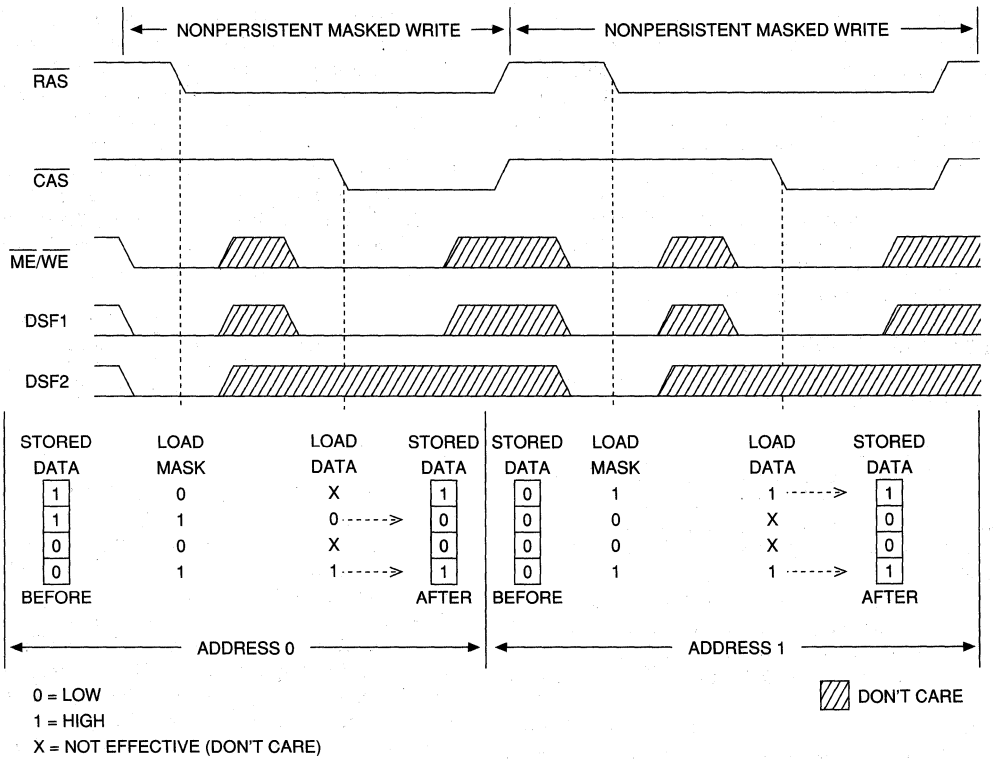


Figure 1
NONPERSISTENT MASKED WRITE EXAMPLE

NONPERSISTENT MASKED WRITE (RWNM)

The MASKED WRITE feature eliminates the need to do a READ-MODIFY-WRITE cycle when changing only certain bits within a 4-bit word. The MT43C4257/8 supports two types of MASKED WRITE cycles, NONPERSISTENT MASKED WRITE and PERSISTENT MASKED WRITE.

If $\overline{ME}/(\overline{WE})$, DSF1 and DSF2 are LOW at the $\overline{RAS}$ HIGH- to-LOW transition, the data (mask data) present on the DQ1-DQ4 inputs will be written into the mask data register. The mask data acts as an individual write enable for each of the four DQ1-DQ4 pins. If a LOW (logic 0) is written to a mask data register bit, the input port for that bit is disabled during the subsequent WRITE operation and no new data will be written to that DRAM cell location. A HIGH (logic 1) on a mask data register bit enables the input port and allows normal WRITE operations to proceed. This convention is used for all masks on the MT43C4257/8. Note that $\overline{CAS}$ is still HIGH. When $\overline{CAS}$ or $(\overline{ME})/\overline{WE}$ go LOW, the bits present on the DQ1-DQ4 inputs will be either written to the DRAM (if the mask data bit was HIGH) or ignored (if the mask data bit was LOW). The DRAM contents that correspond to the masked bits will not be changed during the WRITE cycle. When using NONPERSISTENT MASKED WRITE, the data present on the DQ inputs is loaded into the mask data register at every falling edge of $\overline{RAS}$. FAST PAGE MODE can be used in tandem with NONPERSISTENT MASKED WRITE to write several column locations using the same mask during one $\overline{RAS}$ cycle. An example of NONPERSISTENT MASKED WRITE cycle is shown in Figure 1.

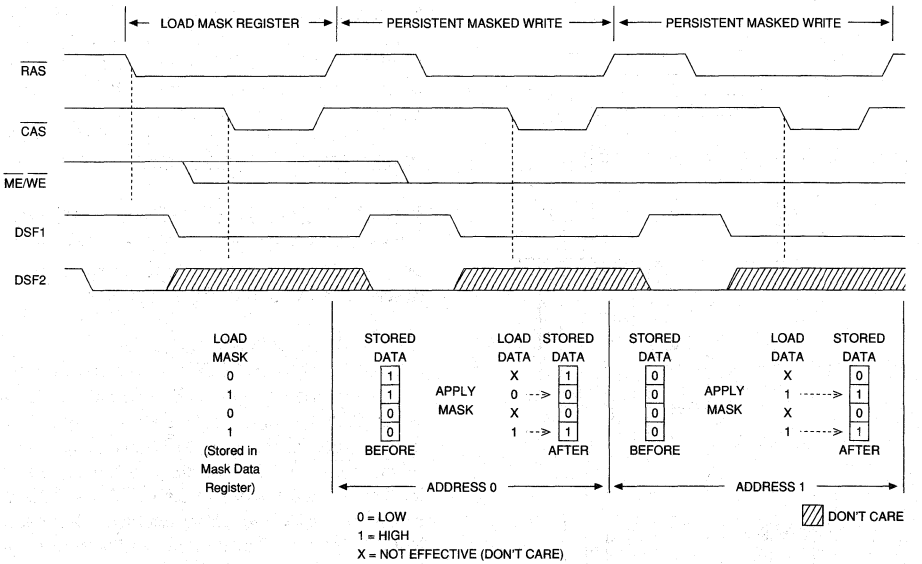


Figure 2
PERSISTENT MASKED WRITE EXAMPLE

PERSISTENT MASKED WRITE (RWOM)

The PERSISTENT MASKED WRITE feature eliminates the need to rewrite the mask data before each MASKED WRITE cycle if the same mask data is being used repeatedly. To initiate a PERSISTENT MASKED WRITE, a LOAD MASK REGISTER cycle is performed by taking $\overline{ME}/(\overline{WE})$ and DSF1 HIGH, and DSF2 LOW, when $\overline{RAS}$ goes LOW. The mask data is loaded into the internal register when $\overline{CAS}$ goes LOW, provided DSF1 is LOW (see the LOAD MASK REGISTER description).

PERSISTENT MASKED WRITE cycles may then be performed by taking $\overline{ME}/(\overline{WE})$ and DSF2 LOW and DSF1 HIGH when $\overline{RAS}$ goes LOW. The contents of the mask data register will then be used as the mask data for the DRAM inputs. Unlike the NONPERSISTENT MASKED WRITE cycle, the data present at the DQ inputs is not loaded into the mask register when $\overline{RAS}$ falls. Another PERSISTENT MASKED WRITE cycle may be performed without reloading the register. Figure 2 shows the LOAD MASK REGISTER and PERSISTENT MASKED WRITE cycle operations. The LOAD MASK REGISTER and PERSISTENT MASKED WRITE cycles allow systems that cannot output data at $\overline{RAS}$ time to perform MASKED WRITE cycles. PERSISTENT MASKED WRITE can also operate in FAST PAGE MODE.

BLOCK WRITE (BW)

The MT43C4257/8 will perform a BLOCK WRITE cycle if DSF1 is HIGH when $\overline{CAS}$ goes LOW. In BLOCK WRITE cycles, the contents of the color register (instead of the DQ inputs) are directly written to four adjacent column locations (see Figure 3). A total of 16 bits will be written simultaneously, improving the normal DRAM fill rate by four times. The color register must be loaded prior to beginning BLOCK WRITE cycles (see LOAD COLOR REGISTER).

The row is addressed as in a normal DRAM WRITE cycle. However, when $\overline{CAS}$ goes LOW, only the A2-A8 inputs are used. A2-A8 specify the "block" (out of the 128 possible) of four adjacent column locations that will be accessed. When the later of $\overline{ME}/\overline{WE}$ and $\overline{CAS}$ go LOW, the DQ inputs are latched and used to determine which of the four column locations will be written. DQ1 acts as a write enable for column location A0 = 0, A1 = 0; DQ2 controls column location A0 = 1, A1 = 0; DQ3 controls A0 = 0, A1 = 1; and DQ4 controls A0 = 1, A1 = 1. The write enable controls are active HIGH; a logic 1 enables and a logic 0 disables the WRITE function.

The contents of the color register will then be written to the column locations enabled. Each DQ location of the color register is written to the four column locations (or any of the four that are enabled) in the corresponding DQ bit plane. The DQ mask is not used in this mode.

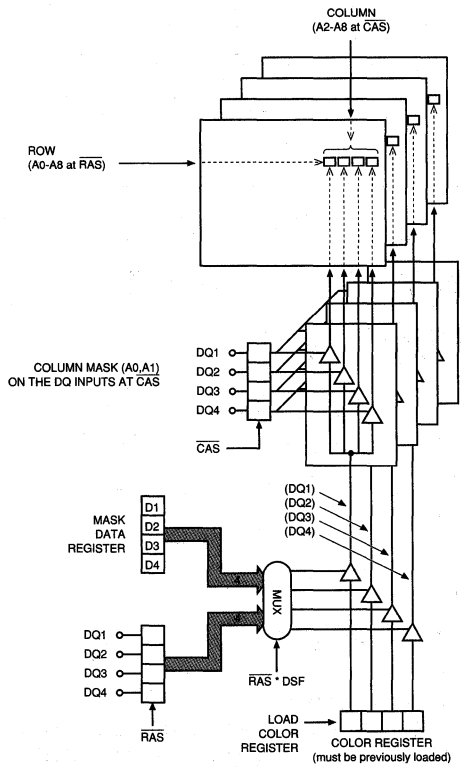


Figure 3
BLOCK WRITE EXAMPLE

NONPERSISTENT MASKED BLOCK WRITE (BWNM)

The MASKED WRITE functions can also be used during BLOCK WRITE cycles. NONPERSISTENT MASKED BLOCK WRITE operates exactly like the normal NONPERSISTENT MASKED WRITE except the mask is now applied to four column locations instead of just one column location.

Like NONPERSISTENT MASKED WRITE, the combination of $\overline{ME}/(\overline{WE})$ LOW and DSF1 LOW when $\overline{RAS}$ goes LOW, initiates a NONPERSISTENT MASK cycle. The DSF pin must be driven HIGH when $\overline{CAS}$ goes LOW to perform a NONPERSISTENT MASKED BLOCK WRITE. By using both the column mask input and the MASKED WRITE function, any combination of the four bit planes may be masked and any combination of the four column locations may be masked.

PERSISTENT MASKED BLOCK WRITE (BWOM)

This cycle is also performed exactly like the normal PERSISTENT MASKED WRITE except that DSF1 is HIGH when $\overline{CAS}$ goes LOW to indicate the BLOCK WRITE function. Both the mask data register and the color register must be loaded with the appropriate data prior to starting a PERSISTENT MASKED BLOCK WRITE.

DRAM REGISTER OPERATIONS

The MT43C4257/8 contains two 4-bit registers that are used as data registers for special functions. This section describes how to load these registers.

LOAD MASK REGISTER (LMR)

The LOAD MASK REGISTER operation and timing are identical to a normal WRITE cycle except that DSF1 is HIGH when $\overline{RAS}$ goes LOW. As shown in the Truth Table, the combination of $\overline{TR}/(\overline{OE})$, $\overline{ME}/(\overline{WE})$, and DSF1 being HIGH when $\overline{RAS}$ goes LOW indicates the cycle is a REGISTER load cycle. DSF1 is used when $\overline{CAS}$ goes LOW to select the register to be loaded, and must be LOW for a LOAD MASK REGISTER cycle. The data present on the DQ lines will then be written to the mask data register.

Note: *For a normal DRAM WRITE cycle, the mask data register is disabled but not modified. The contents of mask data register will not be changed unless a NONPERSISTENT MASKED WRITE cycle or a LOAD MASK REGISTER cycle is performed*

The row address supplied will be refreshed, but it is not necessary to provide any particular row address. The column address inputs are ignored during a LOAD MASK REGISTER cycle.

The mask data register contents are used during PERSISTENT MASKED WRITE and PERSISTENT MASKED BLOCK WRITE cycles to selectively enable writes to the four DQ planes.

LOAD COLOR REGISTER (LCR)

A LOAD COLOR REGISTER cycle is identical to the LOAD MASK REGISTER cycle except DSF1 is HIGH when $\overline{CAS}$ goes LOW. The contents of the color register are retained until changed by another LOAD COLOR REGISTER cycle (or the part loses power) and are used as data inputs during BLOCK WRITE cycles.

TRANSFER OPERATIONS

This section describes transfer operations between the DRAM and either SAM. The direction of the transfer is specified with respect to the DRAM portion of the device. A write is referenced to the DRAM array and a read is referenced from the array.

Note: *The three ports of the TPDRAM are independent and asynchronous to one another. Any or all of the ports may be accessed simultaneously at the maximum allowable frequencies. The only time the ports are synchronized is during transfers to or from the DRAM and SAM portions of the device. A transfer involving a SAM does not affect access from the other SAM port. Both SAMs may be accessed during a DRAM/BMR transfer operation or any other DRAM access cycle other than a SAM transfer.*

TRANSFER operations are initiated when $\overline{TR}/(\overline{OE})$ is LOW at the falling edge of $\overline{RAS}$. The state of STS when $\overline{RAS}$ goes LOW indicates which SAM the TRANSFER will address. The state of $(\overline{ME})/\overline{WE}$ when $\overline{RAS}$ goes LOW indicates the direction of the TRANSFER. At the same time, DSF1 is used to select between normal TRANSFER cycles and SPLIT TRANSFER cycles and DSF2 is used to select between normal TRANSFER cycles and MASKED TRANSFER cycles. A TRANSFER cycle can be performed without dropping $\overline{CAS}$. In this case, the previously loaded Tap address will be used.

The MT43C4257/8 include a feature called BIT MASKED TRANSFER, which uses a third 2,048-bit data register to individually mask every bit involved in a transfer operation. The BIT MASKED TRANSFER may be applied to either READ or WRITE TRANSFERs. The TRM pin is used to select between NORMAL and BIT MASKED TRANSFER (or BIT MASK REGISTER LOAD) cycles. The type of transfer operation is always selected on the falling edge of $\overline{RAS}$.

NORMAL TRANSFERS

The MT43C4257/8 support all of the popular transfer cycles available on the 1 Meg Video RAMs. Each of these is described in the following section.

READ TRANSFER (RT)

A READ TRANSFER cycle is selected if $(\overline{ME})/\overline{WE}$ is HIGH, and DSF1 and $\overline{TR}/(\overline{OE})$ are LOW when $\overline{RAS}$ goes LOW. When $\overline{RAS}$ goes LOW, the READ TRANSFER is to SAMa if STS = LOW, or to SAMb if STS = HIGH. The row address bits indicate the four 512-bit DRAM rows that are to be transferred to the four SAM data registers. The column address bits indicate the start address (or Tap point) of the next serial output cycle from the designated SAM data registers. QSF indicates the SAM half being accessed; LOW if the lower half, HIGH if the upper half. Performing a READ TRANSFER cycle sets the direction of the selected SAM's I/O buffers to the output mode.

To complete a REAL-TIME READ-TRANSFER, $\overline{TR}/(\overline{OE})$ is taken HIGH while $\overline{RAS}$ and $\overline{CAS}$ are LOW. In order to synchronize the REAL-TIME READ TRANSFER to the serial clock, the rising edge of $\overline{TR}/(\overline{OE})$ must occur between the rising edges of successive clocks on the SC input (refer to the AC timing diagrams). A "regular" READ TRANSFER is not sychronized with the SC pin of the addressed SAM. This type of RT is performed when $\overline{TR}/(\overline{OE})$ is taken HIGH "early," without regard to the falling edge of $\overline{CAS}$. The transfer will be completed internally by the device. The first serial clock must meet the ^tRSD and ^tCSD delays (see READ TRANSFER AC timing diagram). The 2,048 bits of DRAM data are then written into the SAM data registers, and the selected SAM's Tap address that was stored in the internal, 9-bit Tap address register is loaded into the address counter. If $\overline{SE}$ for the SAM selected ($\overline{SE}$a for SAMa) is LOW, the first bits of the new row data will appear at the serial outputs with the next SC clock pulse. $\overline{SE}$ enables the serial outputs, and may be either HIGH or LOW during this operation.

SPLIT READ TRANSFER (SRT)

The SPLIT READ TRANSFER cycle eliminates the critical transfer timing required to maintain a continuous serial output data stream (the "full" READ TRANSFER cycle has to occur immediately after the final bit of "old data," and before the first bit of "new data" is clocked out of the SAM port).

When using the SPLIT TRANSFER mode, the SAM is divided into an upper half and a lower half. While data is being serially read from one half of the SAM, new DRAM data may be transferred to the other half. The transfer can occur at any time while the other half is sending data, and need not be synchronized with the SC clock.

The $\overline{TR}/(\overline{OE})$ timing is relaxed for SRT cycles. The rising edge of $\overline{TR}/(\overline{OE})$ is not used to complete the TRANSFER cycle, and therefore is independent of the rising edges of $\overline{RAS}$ and $\overline{CAS}$. The transfer timing is generated internally for SPLIT TRANSFER cycles.

SPLIT TRANSFERs do not change the SAM I/O direction. A normal (non-split) READ TRANSFER cycle must precede any sequence of SRT cycles to put the SAM I/O in the output mode and provide the initial SAM Tap address (which half). Then an SRT can be initiated by taking DSF1 HIGH and selecting the desired SAM (using STS) when $\overline{RAS}$ goes LOW during the TRANSFER cycle. As in non-split transfers, the row address is used to specify the DRAM row to be transferred. When an SRT cycle is initiated, the half of the SAM not actively being accessed will be the half that receives the transfer. When $\overline{CAS}$ falls, address pins A0-

A7 determine the Tap address for the SAM-half selected; A8 = "don't care." If $\overline{CAS}$ does not fall, the previously loaded Tap address will be reused and the TRANSFER will be to the idle half.

Figure 4 shows a typical SRT initiation sequence. The normal READ TRANSFER is first performed, followed by an SRT of the same row to the upper half of the SAM. The SRT to the upper half is optional and need only be done if the Tap for the upper half ≠ 0. For the MT43C4257, serial access continues and when the SAM address counter reaches 255 ("A8" = 1, A0-A7 = 0), the QSF output for that SAM goes HIGH and the Tap address for the upper half is automatically loaded. Since the serial access has now switched to the upper half of the SAM, new data may be transferred to the lower half. This sequence of waiting for the state of QSF to change and then transferring new data to the SAM half that is not being accessed may now be repeated. For example, the next step in Figure 4 would be to wait until QSF went LOW (indicating that row-1 data is shifting out the lower SAM) and then transferring the upper half of row 1 to the upper SAM. $\overline{CAS}$ is used to load the Tap address. If $\overline{CAS}$ does not fall, the last Tap address load for the addressed SAM will be reused.

The split SAM operation is slightly different for the MT43C4258. Instead of having a QSF, this device has a Split SAM Special Function (SSF) input. With this input the serial access may be switched at will from one half of the SAM to the other. In other words, the address count may be stopped on the current half and the Tap address of the next half may be loaded, without waiting for the maximum address count of the current half (255; lower, 511; upper). If no SSF pulse is applied, the Tap address of the next half will be automatically loaded when the maximum count of the current SAM-half is reached. QSF = 0 when the Lower SAM (bits 0–255) is being accessed. QSF = 1 when the Upper SAM (bits 256–511) is being accessed.

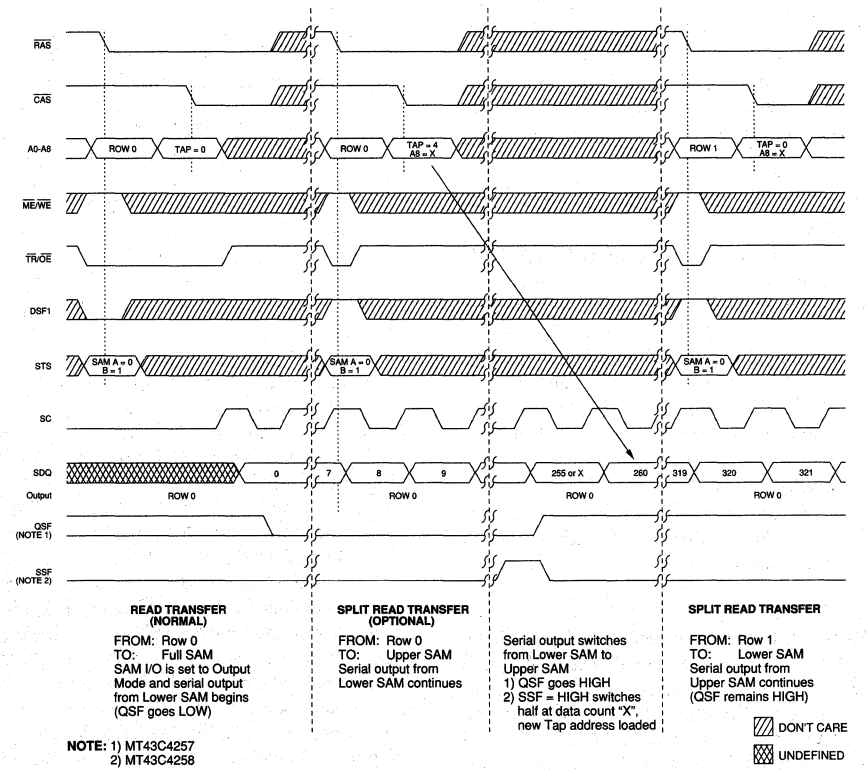


Figure 4
TYPICAL SPLIT-READ-TRANSFER INITIATION SEQUENCE

WRITE TRANSFER (WT)

The operation of the WRITE TRANSFER is identical to the READ TRANSFER described previously, except ($\overline{ME}$)/$\overline{WE}$ and $\overline{SE}$ must be LOW when $\overline{RAS}$ goes LOW. The DSF2 input is used to select between the WT and DQ MASKED WRITE TRANSFER cycles, and must be LOW for the WT cycle. The STS pin is also taken LOW or HIGH to select SAMa or SAMb, respectively, when $\overline{RAS}$ goes LOW. The row address indicates the DRAM row to which the SAM data register will be written, and the Tap address indicates the starting address of the next SERIAL INPUT cycle for the SAM data registers. QSF indicates the SAM half being accessed; LOW if the lower half, HIGH if the upper half. Performing a WT sets the direction of the SAM I/O buffers to the input mode.

PSEUDO WRITE TRANSFER (PWT)

The PSEUDO WRITE TRANSFER cycle may be used to change the direction of a SAM port from output to input without disturbing the DRAM data in the selected row. A PSEUDO WRITE TRANSFER cycle is a WRITE TRANSFER cycle with the $\overline{SE}$ of the appropriate SAM held HIGH instead of LOW. The addressed row will be refreshed. A DQ MASKED WRITE TRANSFER (with all bits masked) is an alternate method for changing the direction of the SAM port without disturbing the addressed row data.

DQ MASKED WRITE TRANSFER (MWT)

The data being transferred from either SAM to the DRAM may be masked by performing a DQ MASKED WRITE TRANSFER cycle. The transfer of data may be selectively enabled for each of the four DQ planes (see Figure 5). The MWT cycle is identical to the WRITE TRANSFER cycle except DSF2 is HIGH and mask data must be on the DQ inputs at the falling edge of $\overline{RAS}$.

The complete SAM register will be transferred to the selected row in each DQ plane if the mask data input is HIGH, and the SAM register will not be transferred if the mask data input for that DQ plane is LOW. DRAM data is not disturbed in masked DQ planes.

DQ MASKED SPLIT WRITE TRANSFER (MSWT)

The DQ MASKED SPLIT WRITE TRANSFER feature makes it possible to input and transfer uninterrupted bit streams. Figure 6 shows a typical initiation sequence for SWT cycles.

Like the SRT, the DQ MASKED SPLIT WRITE TRANSFER cycle does not change the state of the SAM I/O buffers. A normal, DQ MASKED or PSEUDO WRITE TRANSFER cycle is required to set the Tap address and set the SAM I/O direction to input mode.

After the WT, a MSWT is performed to enter the split SAM operating mode. This sets the Tap for the next half of the SAM. The addressed half of the SAM is immediately

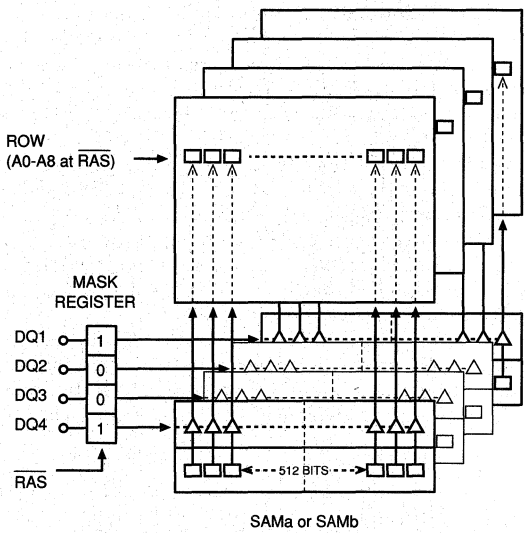


Figure 5
DQ MASKED WRITE TRANSFER

transferred to the first destination row. This half of the SAM may not yet contain valid data. However, another MSWT to the same row will normally occur after this is loaded, so the initial invalid data will be overwritten. Another approach would be to initiate an MSWT addressed to any DRAM row, but mask (disable) all four of the DQ planes. This method can be used to initiate the MSWT sequence without disturbing any DRAM data. The MSWT to the upper half is optional, it is only needed if the Tap for the upper half is $\neq 0$.

Write mask data must be supplied to the DQ inputs during every MSWT cycle at $\overline{RAS}$ time. The mask data acts as an individual write enable for each of the four DRAM DQ planes. For example, DQ1, at $\overline{RAS}$ time, during a MASKED WRITE enables or disables the transfer of the SAM SDQ1 register to the DQ1 plane of the DRAM row selected (see the DQ MASKED WRITE TRANSFER description). As in all other MASKED WRITE operations, a HIGH enables the WRITE TRANSFER and a LOW disables the WRITE TRANSFER. As with SPLIT READ TRANSFER, the half of the SAM not receiving data will be the half transferred and the Tap address (A0-A7) for the other half is loaded when $\overline{CAS}$ falls (A8 is a "don't care"). If $\overline{CAS}$ does not fall, the previously loaded Tap address, A0-A7, will be reused. The TRANSFER will be to the idle half. When the serial clock crosses the half-SAM boundary, the new Tap address for that half is automatically loaded.

The QSFa and QSFb outputs (MT43C4257) indicate which half of SAMa or SAMb, respectively, is currently accepting data. After QSF goes HIGH, indicating that serial input has now switched to the upper SAM, the contents of the lower half of the SAM may be transferred to any DRAM row. The cycle of checking for a change in QSF and then transferring the half of the SAM just filled may now be repeated. The next step on Figure 6 is to wait for QSF to go LOW and then SWT the contents of the upper half of the SAM to row 0. If the terminal count of the SAM half is reached before an SWT is performed for the next half, the access will be repeated from the same half and previously loaded Tap address (access will not move to the next half).

When operating the MT43C4258 in the MSWT mode, the address pointer may be changed to the new Tap address of the next half when the final desired input data is clocked in. When the final data is input, the SSF input is taken HIGH at the corresponding rising edge of SC. The next SC rising edge will input data into the Tap location of the next half of the SAM. If SSF is not applied, the Tap address will be automatically loaded when the maximum Tap address count is reached for the current half (255 or 511). If SSF is HIGH at SC before an MSWT is performed for the next half the access will jump to the old Tap address of the same half. Access will not proceed to the next half. If terminal count is reached before an MSWT, the access will proceed as it does for the MT43C4257.

SERIAL INPUT and SERIAL OUTPUT

The control inputs for SERIAL INPUT and SERIAL OUTPUT are SCa,b, $\overline{SE}$a,b and SSFa,b (MT43C4258). The rising edge of SC increments the serial address counter and provides access to the next SAM location. $\overline{SE}$ enables or disables the serial input/output buffers.

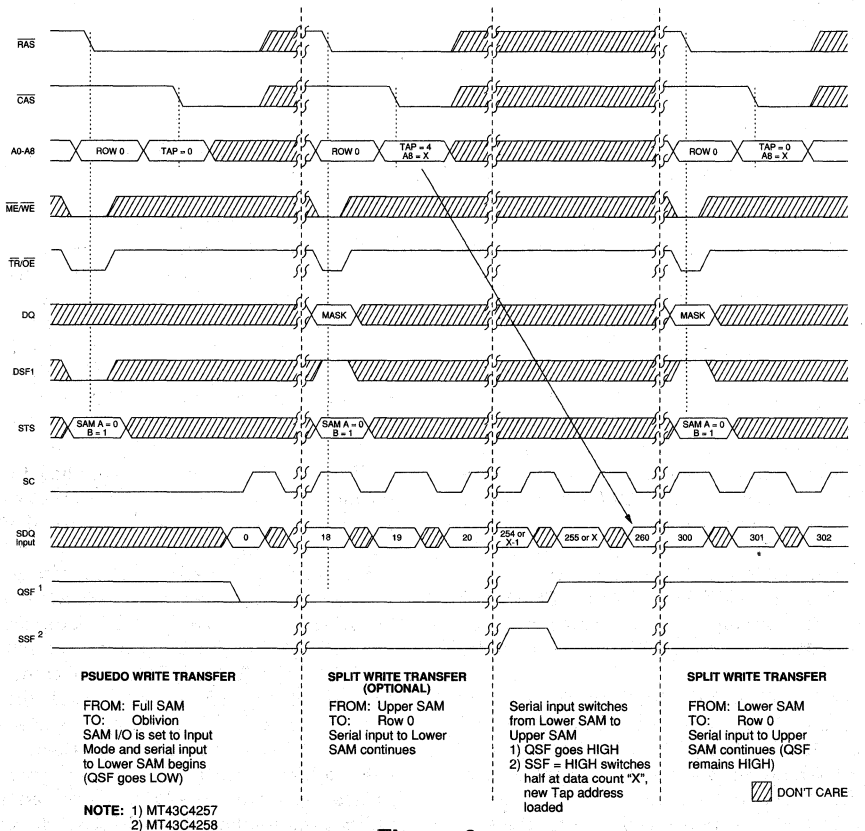


Figure 6
TYPICAL SPLIT-WRITE-TRANSFER INITIATION SEQUENCE

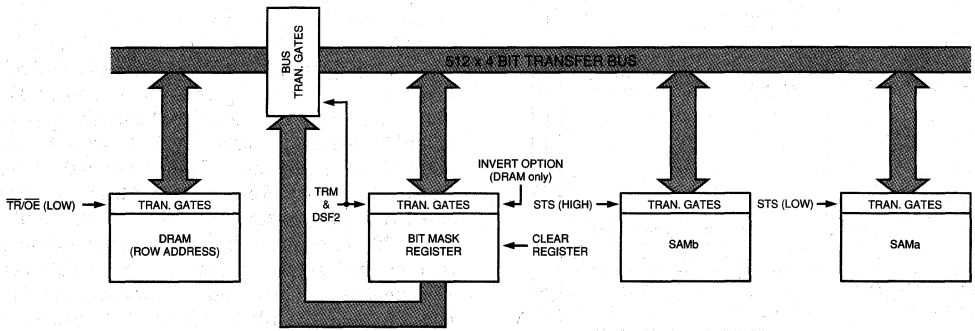


Figure 7
BIT MASKED TRANSFER BLOCK DIAGRAM

Serial output of the SAM contents will start at the serial tap address that was loaded in the SAMa,b address counter during the DRAM-TO-SAM TRANSFER cycle. The SC input increments the address counter and presents the contents of the next SAM location to the 4-bit port. $\overline{SE}$ is used as an output enable during the SAM output operation. The serial address is automatically incremented with every SC LOW-to-HIGH transition, regardless of whether $\overline{SE}$ is HIGH or LOW. For the MT43C4257, the address progresses through the SAM and will wrap around (after count 255 or 511) to the Tap address of the next half, for split modes. Address count will wrap around (after count 511) to Tap address 0 if in the "full" SAM modes.

For the 43C4258, the address count will wrap as it does for the MT43C4257 or it may be triggered, at will, to the next half by the SSF input (split SAM modes). If SSF is HIGH at a LOW-to-HIGH transition of SC, the Tap address of the next half will be loaded into the address pointer. The subsequent LOW-to-HIGH transition of SC will clock data from the Tap address of the new half.

SC is also used to clock-in data when the device is in the serial input mode. As in the serial output operation, the contents of the serial address counter (loaded when the serial input mode was enabled) will determine the serial address of the first 4-bit word written. $\overline{SE}$ acts as a write enable for serial input data and must be LOW for valid serial input. If $\overline{SE}$ = HIGH, the data inputs are disabled and the SAM contents will not be modified. The serial address counter is incremented with every LOW-to-HIGH transition of SC, regardless of the logic level on the $\overline{SE}$ input. The operation of SSF (MT43C4258) is the same as described for serial output.

BIT MASKED TRANSFERS

This section describes transfers between the DRAM and either of the two SAMs using the BIT MASKED TRANSFER capability. Before performing these BIT MASKED TRANSFERs, the bit mask register must first be loaded with the mask data. See the next section, BIT MASK REGISTER OPERATIONs, for instructions on how to load the bit mask register (BMR).

The BMR is a 2,048-bit register that individually controls each of the 2,048 transfer gates on the internal 512 x 4 transfer bus (see Figure 7). These bus transfer gates reside between the DRAM array and the three data registers and are set to the "pass-thru" mode for nonmasked transfers. For BIT MASKED TRANSFERs, the data in the BMR is coupled to the control inputs of the bus transfer gates. A logic "1" in the BMR will select the pass-thru (unmasked) mode for the corresponding SAM data bit, while a logic "0" will select the masked mode for that bit.

BIT MASKED TRANSFERs may be incorporated when doing READ, WRITE, SPLIT READ and SPLIT WRITE TRANSFERs. The timing and control required for any particular BIT MASKED TRANSFER cycle is identical to the corresponding normal TRANSFER cycle, except that TRM and DSF2 are HIGH instead of LOW. BIT MASKED TRANSFERs between the DRAM and either of the two SAM registers are possible. Figure 8 illustrates the BIT MASKED TRANSFER functions.

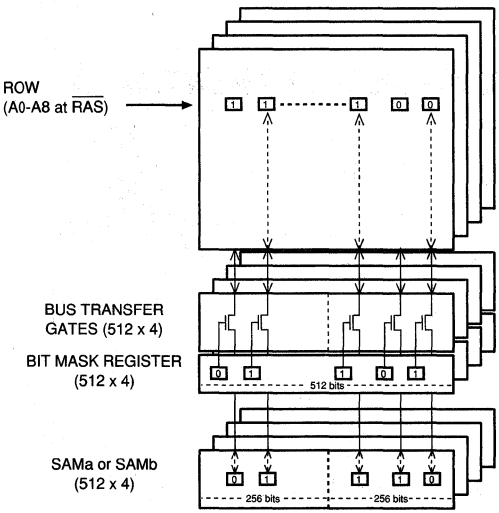


Figure 8
BIT MASK TRANSFER BLOCK DIAGRAM

BIT MASKED READ TRANSFER (BMRT)

BIT MASKED READ TRANSFER may be used to transfer any combination of the 2,048 bits contained in any DRAM row address to either of the two SAMs. The logic conditions and timing for the BMRT function are identical to the normal READ TRANSFER function except that TRM and DSF2 are HIGH to select the BIT MASKED feature. If a bit in the BMR is a logic "1", the bus connection between the corresponding DRAM bit and the selected SAM bit is enabled and the data at the destination (one of the SAMs for BMRT) will be changed to the source data (the DRAM row for BMRT).

BIT MASKED SPLIT READ TRANSFER (BMSRT)

The BIT MASKED SPLIT READ TRANSFER operation is identical to the normal SPLIT READ TRANSFER except that the bit mask (stored in the bit mask register) is applied to the transfer data by taking TRM and DSF2 HIGH when $\overline{RAS}$ falls. The remaining control timing is identical to the requirements for a normal SPLIT READ TRANSFER.

BIT MASKED WRITE TRANSFER (BMWT)

Like WRITE TRANSFER, the BIT MASKED WRITE TRANSFER function may be used to transfer data to any DRAM row address from either of the two SAM registers. In this case, the SAM data will be masked by the contents of the bit mask register before the data is written to the DRAM.

BIT MASKED SPLIT WRITE TRANSFER (BMSWT)

Like the other BIT MASKED TRANSFER cycles, the BMSWT is nearly identical to the SPLIT WRITE TRANSFER, except TRM and DSF2 are HIGH when $\overline{RAS}$ falls. Two masks are applied during a BMSWT operation. Each of the individual bits are masked by the bit mask register and each of the DQ planes are masked by the DQ inputs at $\overline{RAS}$ time. If a DQ input is LOW at $\overline{RAS}$ time, none of the 256 SAM bits for that DQ plane will be transferred to the DRAM row-half selected. If a DQ input is HIGH, the 256 SAM bits for that row half will be masked by the corresponding 256 mask register bits when written to the selected DRAM row-half. The remaining control timing is identical to the requirements for a normal SPLIT WRITE TRANSFER.

BIT MASK REGISTER OPERATIONS

This section describes how to transfer data to or from the Bit Mask Register (BMR) and how to clear the BMR contents. Data may also be inverted when being transferred between the BMR and DRAM.

BMR READ TRANSFER (BMR-RT)

Any DRAM row may be transferred to the BMR by using the BMR READ TRANSFER function. When $\overline{RAS}$ falls, $\overline{TR}$/$\overline{OE}$ is LOW to select a transfer cycle. TRM is HIGH to indicate that the BMR is involved in the TRANSFER cycle, and DSF2 is LOW to indicate that the data is to be transferred to the BMR (as opposed to using the contents of the BMR as bit mask data). The remainder of the timing and control required is identical to a normal READ TRANSFER cycle. No Tap address is loaded in this TRANSFER.

Note that the SAM transfer select (STS) pin is used to select whether non-inverted (STS = LOW) or inverted (STS = HIGH) data is transferred to the bit mask register. For all transfers to or from the bit mask register, the state of the MKD pin when $\overline{RAS}$ falls selects whether the serial mask input (SMI) feature is enabled (see the Functional Truth Table). SMI is a special serial input mode that allows mask information to be clocked into the BMR at the same address location as the data clocked into SAMb (see the SMI mode description). MKD is LOW when $\overline{RAS}$ falls to disable SMI or HIGH to enable SMI. After the transfer is completed, the MKD pin then acts either as a mask data input to the BMR (SMI enabled) or is "don't care" (SMI disabled). The MKD input is tied to the 4 bit-planes, the data on the MKD pin is written to each bit plane simultaneously.

BMR INVERTED READ TRANSFER (BMR-IRT)

If the STS pin is HIGH at $\overline{RAS}$ time the DRAM data will be inverted before being written to the BMR. All 2,048 bits involved in the transfer will be complemented. The functionality and logic levels for the other control inputs are identical to the BMR READ TRANSFER cycle. Note that

MKD is still used to enable or disable the SMI mode. There is no added cycle time delay for either the BMR INVERTED READ or BMR INVERTED WRITE TRANSFER cycles.

BMR WRITE TRANSFER (BMR-WT)

The contents of the BMR may also be transferred to any DRAM row by using the BMR WRITE TRANSFER cycle. $\overline{(ME)}/\overline{WE}$ and DSF2 are LOW and TRM is HIGH when $\overline{RAS}$ falls, to select a write transfer from the BMR. The DQ inputs are used to input a DQ bit-plane mask when $\overline{RAS}$ falls. This allows each of the four DQ planes to be write enabled or disabled during the BMR-WT. The MKD input is used to enable or disable the SMI mode. STS must be LOW at $\overline{RAS}$ time to transfer non-inverted BMR data to the DRAM row selected.

BMR INVERTED WRITE TRANSFER (BMR-IWT)

As with the BMR INVERTED READ TRANSFER, the 2,048 bits involved in the transfer may be inverted while being transferred. Taking STS HIGH at $\overline{RAS}$ time will cause the BMR data to be inverted before it is stored in the selected DRAM row. The other control and DQ (mask) inputs are the same as the BMR-WT.

SAM-TO-BMR TRANSFER (SAM-BMR)

The contents of either SAM may be transferred to the BMR in the same manner that a DRAM row is transferred. In this case, DSF1 is HIGH to indicate that the SAM is the source of the data instead of the DRAM. $\overline{(ME)}/\overline{WE}$ is used to indicate the direction of the transfer and must be LOW, when $\overline{RAS}$ falls, for a SAM-TO-BMR TRANSFER. STS is no longer used to select between normal and inverted data, it now indicates which SAM is involved in the transfer. Since a SAM-TO-BMR TRANSFER "reads" data from the SAM, the SAM will be placed into input mode by this transfer cycle. The MKD input is still used to determine if the SMI mode will be enabled after the transfer is completed. Since no DRAM access is involved, it is not necessary to provide any particular ROW address at $\overline{RAS}$ time. However, whichever ROW address is present at $\overline{RAS}$ time will be used as the address for a $\overline{RAS}$-ONLY REFRESH. Since a SAM is involved in the transfer, a new SAM starting address (or Tap) will be loaded at $\overline{CAS}$ time. This address will be loaded into the serial address counter of the SAM selected by STS at $\overline{RAS}$ time.

Note: *Any SAM/BMR TRANSFER will take the SAM involved in the transfer out of the split SAM mode, if it was in that mode before the transfer.*

BMR-TO-SAM TRANSFER (BMR-SAM)

The contents of the BMR may also be transferred to one of the SAM registers. The $\overline{(ME)}/\overline{WE}$ input is used to indicate the direction of the transfer and must be HIGH for a BMR-TO-SAM TRANSFER. STS is LOW to select SAMa or HIGH to select SAMb as the destination for the BMR data. The remaining inputs and functionality are identical to the SAM-TO-BMR TRANSFER. Since a BMR-TO-SAM TRANSFER writes new data to the selected SAM register, the I/O for the SAM involved will be placed in the output mode and a new Tap address will be loaded when $\overline{CAS}$ falls.

CLEAR BIT MASK REGISTER (CLR-BMR)

The entire contents of the BMR can be cleared (set all bit LOW) within a single transfer cycle by performing a CLEAR BMR cycle. Unlike the other cycles that access the BMR, TRM is LOW at $\overline{RAS}$ time for the CLEAR BIT MASK REGISTER function. $\overline{TR}/\overline{(OE)}$ is LOW to indicate that the cycle is a transfer cycle (although there is really no data transfer involved). The CLR-BMR function is selected when $\overline{ME}/\overline{(WE)}$, DSF1 and DSF2 are HIGH when $\overline{RAS}$ falls.

When the BMR is cleared, all data will be masked when a BIT MASKED TRANSFER cycle is performed.

The BMR INVERTED WRITE and BMR WRITE TRANSFERS may be used with the CLR-BMR function to set or clear, respectively, any DRAM row. The CLR-BMR function is used to clear the BMR then the BMR TRANSFERS are performed to the addressed DRAM row.

The CLEAR BIT MASK REGISTER function is useful when using the SERIAL MASK INPUT mode. It is automatically performed (when in the SMI mode) when data is transferred from SAMb to the DRAM (see SERIAL MASK INPUT section).

SERIAL MASK INPUT (SMI)

Whenever the BMR is accessed, the MKD input is sensed and latched into the BMR control logic. If the MKD pin is LOW at $\overline{RAS}$ time the serial mask input (SMI) mode is disabled and the BMR may only be loaded via internal transfer cycles. If MKD is HIGH when $\overline{RAS}$ falls, during a BMR access, then the BMR control logic enables the SMI mode and the BMR may be serially loaded via the MKD input.

When SMI is enabled, the MKD input is coupled to all four of the bit mask register's DQ planes (see Figure 9). The SCb clock input and SAMb's address counter are used to input data to SAMb and the BMR. SEb will enable (LOW) or disable (HIGH) input data to SAMb and the BMR, the address count will increment regardless of the state of SEb.

The most common application of the SMI mode is to automatically load a transfer mask with the new data written to SAMb. To initialize the sequence, the BMR is cleared (CLR-BMR) with MKD = HIGH at $\overline{RAS}$ time to enable the SMI mode. Then SAMb is prepared to accept input data by performing PSEUDO WRITE TRANSFER. The SAM starting address loaded will also apply to the

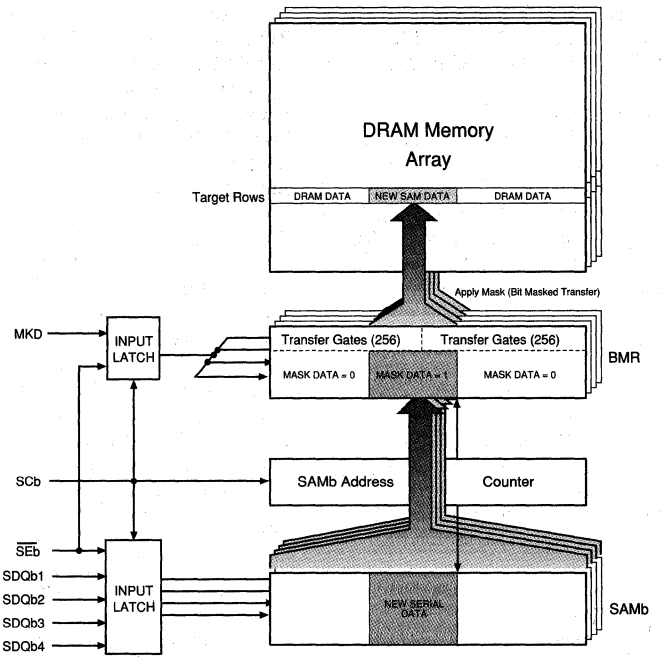


Figure 9
SERIAL-MASK-INPUT MODE BLOCK DIAGRAM

BMR. For every address location to which data is written in SAMb, the corresponding address location in the BMR will be written to the value present on MKD (all four planes of the BMR will be written). After the input of data to SAMb is complete, a BIT MASKED WRITE TRANSFER may be performed and only the unmasked data from SAMb will be transferred to the DRAM. The BMR will be cleared automatically after a BIT MASKED WRITE TRANSFER from SAMb, if the device is in the SMI mode. A BMSWT from SAMb will clear only half of the BMR. This allows a new mask to be loaded during the next fill of SAMb, without performing a CLR-BMR cycle. If data is to be masked during the BMWT, then MKD is held LOW when the corresponding SAMb data is written. If the data is to be written (unmasked) to the DRAM during the BMWT, then MKD is held HIGH when the corresponding SAMb location is written. The function of the MKD pin is dependent on the I/O direction of SAMb. MKD is an input only, if SMI is enabled and SAMb is in input mode. If SMI is enabled and SAMb is in output mode, the MKD input is a "don't care," and no new data may be written to the BMR via MKD. MKD is also "don't care" if the SMI mode is disabled. Note that the mask data loaded via SAMb may also be applied to a SAMa TRANSFER cycle, if the mask has not been cleared by a SAMb TRANSFER or a CLR-BMR cycle. The BMR will not be cleared after a TRANSFER involving SAMa.

POWER UP INITIALIZATION

When Vcc is initially supplied or when refresh is interrupted for more than 8ms, the device must be initialized.

After Vcc is at specified operating conditions, for 100µs (minimum), eight $\overline{RAS}$ cycles must be executed to initialize the dynamic memory array. When the device is initialized the DRAM I/O pins (DQs) are in a High-Z state, regardless of the state of $(\overline{TR})/\overline{OE}$. The DRAM array will contain random data.

The SAM portion of the device is completely static and does not require an initialization cycle. Both SAM ports will power-up in the serial input mode (WRITE TRANSFERs) and the SAM I/O pins (SDQs) are in a High-Z state, regardless of the state of $\overline{SE}$ ab. Also, SPLIT TRANSFER and SMI modes are disabled. Both QSF (MT43C4257) outputs may be in the HIGH or LOW state. The SAMs, as well as the bit mask, color, and DRAM mask registers all contain random data after power-up.

TRUTH TABLE [1]

CODE	FUNCTION	RAS FALLING EDGE									CAS FALL	A0-A8[2]		DQ1-DQ4[3]		REGISTERS	
		CAS	TR/OE	ME/WE[10]	DSF1	DSF2	SEa, SEb	TRM	MKD	STS	DSF1	RAS	CAS	RAS	CAS,WE[4]	MASK	COLOR
	DRAM OPERATIONS																
CBR	CAS-BEFORE-RAS REFRESH	0	X	1[11]	X	X	X	X	X	X	X	X	X	X	X	—	—
ROR	RAS-ONLY REFRESH	1	1	X	X	X	X	X	X	X	—	ROW	—	X	—	—	—
RW	NORMAL DRAM READ OR WRITE	1	1	1	0	0[11]	X	X	X	X	0	ROW	COLUMN	X	VALID DATA	—	—
RWNM	NONPERSISTENT (LOAD AND USE) MASKED WRITE TO DRAM	1	1	0	0	0[11]	X	X	X	X	0	ROW	COLUMN	WRITE MASK	VALID DATA	LOAD & USE	—
RWOM	PERSISTENT (USE REGISTER) MASKED WRITE TO DRAM	1	1	0	1	0[11]	X	X	X	X	0	ROW	COLUMN	X	VALID DATA	USE	—
BW	BLOCK WRITE TO DRAM (NO DATA MASK)	1	1	1	0	0[11]	X	X	X	X	1	ROW	COLUMN (A2-A8)	X	COLUMN MASK	—	USE
BWNM	NONPERSISTENT (LOAD & USE) MASKED BLOCK WRITE TO DRAM	1	1	0	0	0[11]	X	X	X	X	1	ROW	COLUMN (A2-A8)	WRITE MASK	COLUMN MASK	LOAD & USE	USE
BWOM	PERSISTENT (USE MASK REGISTER) MASKED BLOCK WRITE TO DRAM	1	1	0	1	0[11]	X	X	X	X	1	ROW	COLUMN (A2-A8)	X	COLUMN MASK	USE	USE
	REGISTER OPERATIONS																
LMR	LOAD MASK REGISTER	1	1	1	1	0[11]	X	X	X	X	0	X[5]	X	X	WRITE MASK	LOAD	—
LCR	LOAD COLOR REGISTER	1	1	1	1	0[11]	X	X	X	X	1	X[5]	X	X	COLOR DATA	—	LOAD
	TRANSFER OPERATIONS																
RT	READ TRANSFER (DRAM-TO-SAM TRANSFER)	1	0	1	0	0	X	0	X	0=SAMa 1=SAMb	X	ROW	TAP[6]	X	X	—	—
SRT[9]	SPLIT READ TRANSFER (SPLIT DRAM-TO-SAM TRANSFER)	1	0	1	1	0	X	0	X	0=SAMa 1=SAMb	X	ROW	TAP[6]	X	X	—	—
WT	WRITE TRANSFER (SAM-TO-DRAM TRANSFER)	1	0	0	0	0	0	0	X	0=SAMa 1=SAMb	X	ROW	TAP[6]	X	X	—	—
PWT	PSEUDO WRITE TRANSFER (SERIAL INPUT MODE ENABLE)	1	0	0	0	0	1	0	X	0=SAMa 1=SAMb	X	X[5]	TAP[6]	X	X	—	—
MSWT[9]	SPLIT WRITE TRANSFER (SPLIT SAM-TO-DRAM TRANSFER WITH DQ MASK)	1	0	0	1	0	X	0	X	0=SAMa 1=SAMb	X	ROW	TAP[6]	DQ MASK	X	—	—
MWT	DQ MASKED WRITE TRANSFER	1	0	0	0	1	X	0	X	0=SAMa 1=SAMb	X	ROW	TAP[6]	DQ MASK	X	—	—

TRUTH TABLE[1]

CODE	FUNCTION	RAS FALLING EDGE									CAS FALL	A0-A8[2]		DQ1-DQ4[3]		REGISTERS	
		CAS	TR/OE	ME/WE[10]	DSF1	DSF2	SEa, SEb	TRM	MKD	STS	DSF1	RAS	CAS	RAS	CAS,WE[4]	MASK	COLOR
	BIT MASK REGISTER OPERATIONS																
BMR-RT	BMR READ TRANSFER (DRAM→BMR TRANSFER)	1	0	1	0	0	X	1	0/1[7]	0	X	ROW	X	X	X	—	—
BMR-IRT	BMR READ TRANSFER (DRAM→INVERT→BMR TRANSFER)	1	0	1	0	0	X	1	0/1[7]	1	X	ROW	X	X	X	—	—
BMR-WT	BMR WRITE TRANSFER (BMR→DRAM TRANSFER)	1	0	0	0	0	X	1	0/1[7]	0	X	ROW	X	DQ MASK	X	—	—
BMR-IWT	BMR WRITE TRANSFER (BMR→INVERT→DRAM TRANSFER)	1	0	0	0	0	X	1	0/1[7]	1	X	ROW	X	DQ MASK	X	—	—
SAM-BMR	SAM→BMR TRANSFER	1	0	0	1	0	X	1	0/1[7]	0=SAMa 1=SAMb	X	X[5]	TAP[6]	X	X	—	—
BMR-SAM	BMR→SAM TRANSFER	1	0	1	1	0	X	1	0/1[7]	0=SAMa 1=SAMb	X	X[5]	TAP[6]	X	X	—	—
CLR-BMR	CLEAR BIT MASK REGISTER (SETS BMR TO ALL "0's")	1	0	1	1	1	X	0	0/1[7]	X	X	X[5]	X	X	X	—	—
	BIT MASKED TRANSFER OPERATIONS																
BMRT	BIT MASKED READ TRANSFER (BM DRAM→SAM TRANSFER)	1	0	1	0	1	X	1	X	0=SAMa 1=SAMb	X	ROW	TAP[6]	X	X	—	—
BMSRT[9]	BIT MASKED SPLIT READ TRANSFER (BM SPLIT DRAM→SAM TRANSFER)	1	0	1	1	1	X	1	X	0=SAMa 1=SAMb	X	ROW	TAP[6]	X	X	—	—
BMWT	BIT MASKED WRITE TRANSFER (BM SAM→DRAM TRANSFER)	1	0	0	0	1	X	1	X[8]	0=SAMa 1=SAMb	X	ROW	TAP[6]	X	X	—	—
BMSWT[9]	BIT MASKED SPLIT WRITE TRANSFER (BM SPLIT SAM→DRAM TRANSFER)	1	0	0	1	1	X	1	X[8]	0=SAMa 1=SAMb	X	ROW	TAP[6]	DQ MASK	X	—	—

NOTE:
1. 0 = LOW (V_{IL}), 1 = HIGH (V_{IH}), X = "don't care," — = "not applicable."
2. These columns show what must be present on the A0-A8 inputs when $\overline{RAS}$ falls and when $\overline{CAS}$ falls.
3. These columns show what must be present on the DQ1-DQ4 inputs when $\overline{RAS}$ falls and when $\overline{CAS}$ falls.
4. With WRITE cycles, the input data is latched at the falling edge of $\overline{CAS}$ or $\overline{ME}/\overline{WE}$, whichever is later. Similarly, with READ cycles, the output data is enabled on the falling edge of $\overline{CAS}$ or $\overline{TR}/\overline{OE}$, whichever is later.
5. The ROW that is addressed will be refreshed, but no particular ROW address is required.
6. Tap Address; this is the SAM location that the first SC cycle will access. For SPLIT TRANSFERs, the half receiving the transfer is determined by the MSB of the internal address counter. The SAM half not currently being accessed will be the half receiving the transfer.
   Column address A8 is a "don't care" for SPLIT TRANSFERs.
7. The Serial Mask Input mode (SMI) is enabled ("1") or disabled ("0") when the BMR is accessed (see BMR OPERATIONS). If SMI is enabled (MKD = "1"), mask data is serially clocked into the BMR with SCb and the BMR is automatically cleared after a BIT MASKED WRITE or BIT MASKED SPLIT WRITE TRANSFER cycle from SAMb. For BIT MASKED READ TRANSFERs to any SAM and BIT MASKED WRITE TRANSFERs from SAMa, the BMR is not cleared automatically.
8. If the SMI mode is enabled, mask data is clocked into the BMR with SCb.
9. SPLIT TRANSFERs 9.do not change SAM I/O direction.
10. SAM I/O direction is a function of the state of $\overline{ME}/\overline{WE}$ at $\overline{RAS}$ time. If $\overline{ME}/\overline{WE}$ is LOW, then the selected SAM is an input; if $\overline{ME}/\overline{WE}$ is HIGH, then the SAM is an output (except for SPLIT TRANSFERs).
11. The MT43C4257/8 operates properly if this state is "X", but to allow for future functional enhancements it is recommended that they are driven as shown in the Truth Table.

ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc Supply Relative to Vss ..... -1V to +7V
Operating Temperature, T_A (Ambient) ..... 0°C to +70°C
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation 1.5W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.75	5.25	V	1
Input High (Logic 1) Voltage, All Inputs	V_{IH}	2.4	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, All Inputs	V_{IL}	-1.0	0.8	V	1

DC ELECTRICAL CHARACTERISTICS

($0°C \le T_A \le 70°C$; V_{CC} = 5V ±5%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
INPUT LEAKAGE CURRENT Any input ($0V \le V_{IN} \le V_{CC}$); all other pins not under test = 0V	I_L	-10	10	µA	
OUTPUT LEAKAGE CURRENT (Dout is disabled, $0V \le V_{OUT} \le V_{CC}$).	I_{OZ}	-10	10	µA	
OUTPUT LEVELS Output High Voltage (I_{OUT} = -2.5mA, SDQs; -5mA all other outputs)	V_{OH}	2.4		V	1
Output Low Voltage (I_{OUT} = 2.5mA, SDQs; 5mA all other outputs)	V_{OL}		0.4	V	

CAPACITANCE

(T_A = 25°C)

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A8, TRM, MKD	C_{I1}		5	pF	2
Input Capacitance: $\overline{RAS}$, $\overline{CAS}$, $\overline{ME}/\overline{WE}$, $\overline{TR}/\overline{OE}$, SCa,b, $\overline{SE}$a,b, DSF1,2, STS SSFa,b	C_{I2}		7	pF	2
Input/Output Capacitance: DQ, SDQa,b	$C_{I/O}$		9	pF	2
Output Capacitance: QSFa,b	C_O		9	pF	2

TSOP THERMAL CONSIDERATIONS (preliminary)

DESCRIPTION	SYMBOL	MAX	UNITS	NOTES
Thermal resistance - Junction to Ambient	øJA	85	°C/W	
Thermal resistance - Junction to Case	øJC	15	°C/W	
Maximum Case Temperature	TC	110	°C	

DRAM CURRENT DRAIN; SAMa, SAMb and SERIAL MASK INPUT (SMI) INACTIVE

($0°C \le T_A \le 70°C$; V_{CC} = 5V ±5%)

PARAMETER/CONDITION	SYMBOL	MAX -8	MAX -10	UNITS	NOTES
OPERATING CURRENT ($\overline{RAS}$ and $\overline{CAS}$ = Cycling; ^tRC = ^tRC (MIN))	I_{CC1}	100	90	mA	3, 4 25
OPERATING CURRENT: PAGE MODE ($\overline{RAS}$ = V_{IL} $\overline{CAS}$ = Cycling; ^tPC = ^tPC (MIN))	I_{CC2}	95	85	mA	3, 4 27
STANDBY CURRENT: TTL INPUT LEVELS Power supply standby current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH}, after 8 $\overline{RAS}$ cycles (MIN))	I_{CC3}	10	10	mA	
STANDBY CURRENT: CMOS INPUT LEVELS Power supply standby current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC}-0.2V, after 8 $\overline{RAS}$ cycles min). All other inputs ≥ V_{CC} -0.2V or ≤ V_{SS} +0.2V	I_{CC4}	2	2	mA	
REFRESH CURRENT: $\overline{RAS}$-ONLY ($\overline{RAS}$ = Cycling; $\overline{CAS}$ = V_{IH})	I_{CC5}	105	95	mA	3, 26
REFRESH CURRENT: $\overline{CAS}$-BEFORE-$\overline{RAS}$ ($\overline{RAS}$ and $\overline{CAS}$ = Cycling)	I_{CC6}	105	95	mA	3, 5 26
TRANSFER CURRENT: SAM/DRAM DATA TRANSFER	I_{CC7}	100	90	mA	3

SERIAL PORT CURRENT DRAIN; SAMa, SAMb and/or SMI MODE

(Notes 3, 4) ($0°C \le T_A \le 70°C$; V_{CC} = 5V ±5%)

PARAMETER/CONDITION	SYMBOL	MAX -8	MAX -10	UNITS	NOTES
OPERATING CURRENT: SERIAL PORT (SAMa/SAMb) (SCa/SCb = Cycling; ^tSC = ^tSC (MIN); $\overline{SEa}$/$\overline{SEb}$ = V_{IL})	I_{CC8}	40	35	mA	
OPERATING CURRENT: SMI MODE (SAMb) (SCb = Cycling; ^tSC = ^tSC (MIN); $\overline{SEb}$ = V_{IL})	I_{CC9}	20	20	mA	
STANDBY CURRENT: SERIAL PORT (SAMa/SAMb) Power supply standby current (SCa/SCb = V_{IH} or V_{IL}; $\overline{SEa}$/$\overline{SEb}$ = V_{IH})	I_{CC10}	0	0	mA	
STANDBY CURRENT: SMI MODE (SAMb) Power supply standby current (SCb = V_{IH} or V_{IL}; $\overline{SEb}$ = V_{IH})	I_{CC11}	0	0	mA	

TOTAL CURRENT DRAIN

(Notes 3, 4) ($0°C \le T_A \le 70°C$; V_{CC} = 5V ±5%)

$I_{CC(TOTAL)}$	= DRAM CURRENT (I_{CC1-7}) + SAMa CURRENT (I_{CC8} or I_{CC10}) + SAMb CURRENT (I_{CC8} or I_{CC10}) + SMI CURRENT (I_{CC9} or I_{CC11}) [+ 10mA (If DRAM CURRENT = I_{CC3} or I_{CC4})]

Example 1:
Operating current (-8) with DRAM operating in Fast Page Mode, SAMa active, SAMb and SMI inactive:

$I_{CC(TOTAL)}$	= DRAM CURRENT (I_{CC2}) + SAMa CURRENT (I_{CC8}) + SAMb CURRENT (I_{CC10}) + SMI CURRENT (I_{CC11}) [+ 0] = 95 + 40 + 0 + 0 = 135mA (MAX)

Example 2:
Operating current (-10) with DRAM operating in CMOS Standby, SAMa and SAMb active, SMI active:

$I_{CC(TOTAL)}$	= DRAM CURRENT (I_{CC4}) + SAMa CURRENT (I_{CC8}) + SAMb CURRENT (I_{CC8}) + SMI CURRENT (I_{CC9}) [+ 10] = 2 + 35 + 35 + 20 + 10 = 102mA (MAX)

DRAM TIMING PARAMETERS

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C ≤ T_A ≤ +70°C; Vcc = 5V ±5%)

AC CHARACTERISTICS		-8		-10			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Random READ or WRITE cycle time	^tRC	150		180		ns	
READ-MODIFY-WRITE cycle time	^tRWC	205		235		ns	
FAST-PAGE-MODE READ or WRITE cycle time	^tPC	50		60		ns	
FAST-PAGE-MODE READ-MODIFY-WRITE cycle time	^tPRWC	95		120		ns	
Access time from $\overline{RAS}$	^tRAC		80		100	ns	14, 17
Access time from $\overline{CAS}$	^tCAC		20		25	ns	15
Access time from ($\overline{TR}$)/$\overline{OE}$	^tOE		20		25	ns	
Access time from column address	^tAA		40		50	ns	
Access time from $\overline{CAS}$ precharge	^tCPA		45		55	ns	
$\overline{RAS}$ pulse width	^tRAS	80	20,000	100	20,000	ns	
$\overline{RAS}$ pulse width (FAST PAGE MODE)	^tRASP	80	100,000	100	100,000	ns	
$\overline{RAS}$ hold time	^tRSH	20		25		ns	
$\overline{RAS}$ precharge time	^tRP	60		70		ns	
$\overline{CAS}$ pulse width	^tCAS	20	10,000	25	10,000	ns	
$\overline{CAS}$ hold time	^tCSH	80		100		ns	
$\overline{CAS}$ precharge time	^tCP	10		10		ns	16
$\overline{RAS}$ to $\overline{CAS}$ delay time	^tRCD	20	60	25	75	ns	17
$\overline{CAS}$ to $\overline{RAS}$ precharge time	^tCRP	5		5		ns	
Row address setup time	^tASR	0		0		ns	
Row address hold time	^tRAH	12		15		ns	
$\overline{RAS}$ to column address delay time	^tRAD	17	40	20	50	ns	18
Column address setup time	^tASC	0		0		ns	
Column address hold time	^tCAH	15		20		ns	
Column address hold time (referenced to $\overline{RAS}$)	^tAR	60		70		ns	
Column address to $\overline{RAS}$ lead time	^tRAL	40		50		ns	
Read command setup time	^tRCS	0		0		ns	
Read command hold time (referenced to $\overline{CAS}$)	^tRCH	0		0		ns	19
Read command hold time (referenced to $\overline{RAS}$)	^tRRH	0		0		ns	19
$\overline{CAS}$ to output in Low-Z	^tCLZ	3		3		ns	
Output buffer turn-off delay	^tOFF	3	20	3	20	ns	20, 23
Output disable	^tOD	3	10	3	20	ns	20, 23
Output disable hold time from start of WRITE	^tOEH	15		15		ns	28
Output Enable to $\overline{RAS}$ delay	^tORD	0		0		ns	

DRAM TIMING PARAMETERS (continued)

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C ≤ T_A ≤ +70°C; Vcc = 5V ±5%)

AC CHARACTERISTICS		-8		-10			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Write command setup time	^tWCS	0		0		ns	21
Write command hold time	^tWCH	15		20		ns	
Write command hold time (referenced to $\overline{RAS}$)	^tWCR	60		75		ns	
Write command pulse width	^tWP	15		15		ns	
Write command to $\overline{RAS}$ lead time	^tRWL	20		25		ns	
Write command to $\overline{CAS}$ lead time	^tCWL	20		25		ns	
Data-in setup time	^tDS	0		0		ns	22
Data-in hold time	^tDH	15		20		ns	22
Data-in hold time (referenced to $\overline{RAS}$)	^tDHR	55		70		ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	^tRWD	100		130		ns	21
Column address to $\overline{WE}$ delay time	^tAWD	60		80		ns	21
$\overline{CAS}$ to $\overline{WE}$ delay time	^tCWD	40		55		ns	21
Transition time (rise or fall)	^tT	3	35	3	35	ns	9, 10
Refresh period (512 cycles)	^tREF		8		8	ms	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	^tRPC	0		0		ns	
$\overline{CAS}$ setup time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tCSR	10		10		ns	5
$\overline{CAS}$ hold time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tCHR	30		30		ns	5
$\overline{ME}$/$\overline{WE}$ to $\overline{RAS}$ setup time	^tWSR	0		0		ns	
$\overline{ME}$/$\overline{WE}$ to $\overline{RAS}$ hold time	^tRWH	15		15		ns	
Mask data to $\overline{RAS}$ setup time	^tMS	0		0		ns	
Mask data to $\overline{RAS}$ hold time	^tMH	15		15		ns	

TRANSFER AND MODE CONTROL TIMING PARAMETERS

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes 6, 7, 8, 9, 10) (0° C ≤ T_A ≤ + 70°C; Vcc = 5V ±5%)

AC CHARACTERISTICS		-8		-10			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
$\overline{TR}/(\overline{OE})$ LOW to $\overline{RAS}$ setup time	^tTLS	0		0		ns	
$\overline{TR}/(\overline{OE})$ LOW to $\overline{RAS}$ hold time	^tTLH	15	10,000	15	10,000	ns	
$\overline{TR}/(\overline{OE})$ LOW to $\overline{RAS}$ hold time (REAL-TIME READ TRANSFER only)	^tRTH	70	10,000	80	10,000	ns	
$\overline{TR}/(\overline{OE})$ LOW to $\overline{CAS}$ hold time (REAL-TIME READ TRANSFER only)	^tCTH	20		25		ns	
$\overline{TR}/(\overline{OE})$ HIGH to SC lead time	^tTSL	5		5		ns	
$\overline{TR}/(\overline{OE})$ HIGH to $\overline{RAS}$ precharge time	^tTRP	60		70		ns	
$\overline{TR}/(\overline{OE})$ precharge time	^tTRW	25		30		ns	
First SC edge to $\overline{TR}/(\overline{OE})$ HIGH delay time	^tTSD	15		15		ns	
$\overline{RAS}$ to first SC edge delay time	^tRSD	80		95		ns	
$\overline{CAS}$ to first SC edge delay time	^tCSD	25		30		ns	
Serial output buffer turn-off delay from $\overline{RAS}$	^tSDZ	10	50	10	50	ns	
SC to $\overline{RAS}$ setup time	^tSRS	30		30		ns	
Serial data input to $\overline{SE}$ delay time	^tSZE	0		0		ns	
$\overline{RAS}$ to SD buffer turn on time	^tSRO	10		15		ns	
Serial data input delay from $\overline{RAS}$	^tSDD	60		60		ns	
Serial data input to $\overline{RAS}$ delay time	^tSZS	0		0		ns	
Serial-Input-Mode enable ($\overline{SE}$) to $\overline{RAS}$ setup time	^tESR	0		0		ns	
Serial-Input-Mode enable ($\overline{SE}$) to $\overline{RAS}$ hold time	^tREH	15		15		ns	
$\overline{TR}/(\overline{OE})$ HIGH to $\overline{RAS}$ setup time	^tYS	0		0		ns	
$\overline{TR}/(\overline{OE})$ HIGH to $\overline{RAS}$ hold time	^tYH	15		15		ns	
DSF, TRM, STS, MKD to $\overline{RAS}$ setup time	^tFSR	0		0		ns	
DSF, TRM, STS, MKD to $\overline{RAS}$ hold time	^tRFH	15		15		ns	
DSF to $\overline{RAS}$ hold time	^tFHR	60		65		ns	
DSF to $\overline{CAS}$ setup time	^tFSC	0		0		ns	
DSF to $\overline{CAS}$ hold time	^tCFH	15		20		ns	
SC to QSF delay time	^tSQD		35		40	ns	29
$\overline{RAS}$ to QSF delay time	^tRQD		65		85	ns	29
$\overline{CAS}$ to QSF delay time	^tCQD		35		40	ns	29
$\overline{TR}/\overline{OE}$ to QSF delay time	^tTQD		25		30	ns	29
SPLIT TRANSFER setup time	^tSTS	30		35		ns	29
SPLIT TRANSFER hold time	^tSTH	0		0		ns	29

SAM TIMING PARAMETERS

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

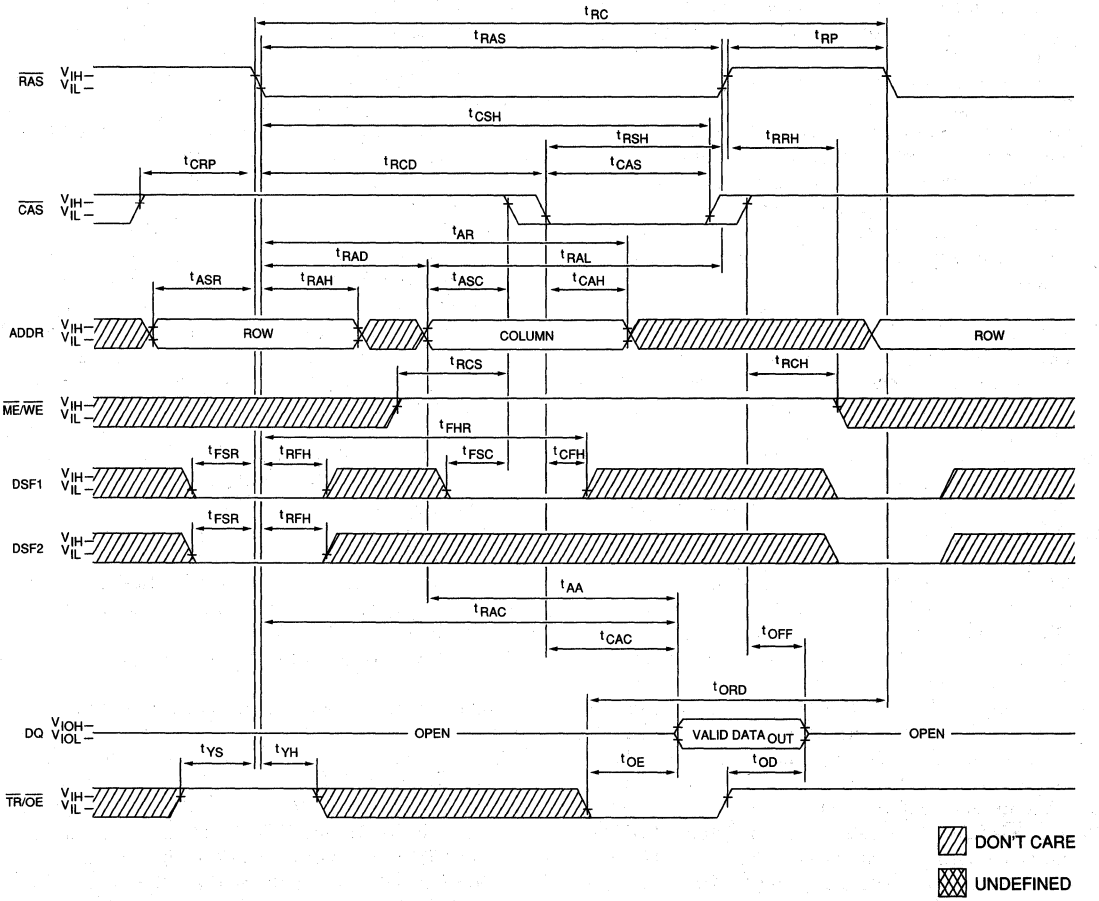
(Notes 6, 7, 8, 9, 10) (0° C ≤ T_A ≤ + 70°C; Vcc = 5V ±5%)

AC CHARACTERISTICS		-8		-10			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Serial clock cycle time	^tSC	28		30		ns	
Access time from SC	^tSAC		25		27	ns	24, 31
SC precharge time (SC LOW time)	^tSP	10		10		ns	
SC pulse width (SC HIGH time)	^tSAS	10		10		ns	
Access time from $\overline{SE}$	^tSEA		15		20	ns	24
$\overline{SE}$ precharge time	^tSEP	10		15		ns	
$\overline{SE}$ pulse width	^tSE	10		15		ns	
Serial data out hold time after SC HIGH	^tSOH	5		5		ns	24, 31
Serial output buffer turn off delay from $\overline{SE}$	^tSEZ	3	12	3	15	ns	20, 24
Serial data in setup time	^tSDS	0		0		ns	24
Serial data in hold time	^tSDH	10		10		ns	24
Serial mask data in setup time	^tMDS	0		0		ns	
Serial mask data in hold time	^tMDH	10		10		ns	
SERIAL INPUT (Write) Enable setup time	^tSWS	0		0		ns	
SERIAL INPUT (Write) Enable hold time	^tSWH	15		15		ns	
SERIAL INPUT (Write) disable setup time	^tSWIS	0		0		ns	
SERIAL INPUT (Write) disable hold time	^tSWIH	15		15		ns	
SSF to SC setup time	^tSFS	0		0		ns	30
SSF to SC hold time	^tSFH	15		20		ns	30
SSF LOW to SC HIGH delay	^tSFD	5		5		ns	30

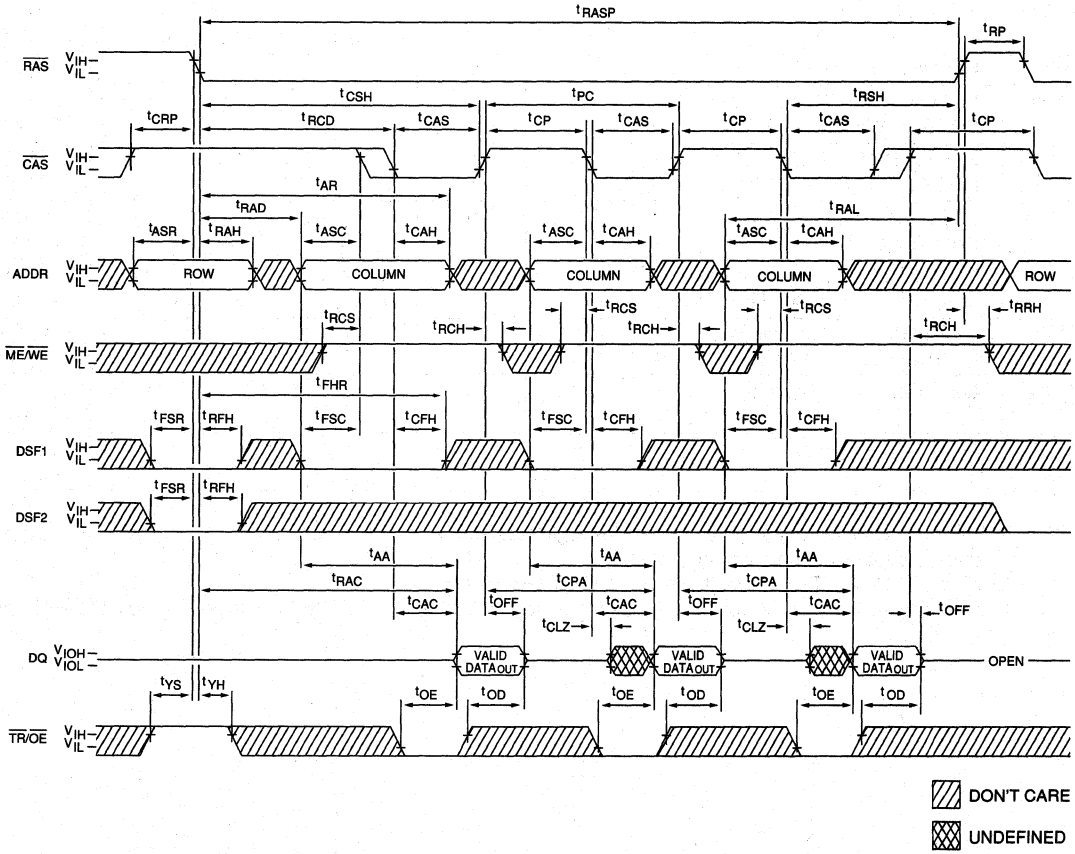
NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. V_{CC} = 5V ±5%, f = 1 MHz.
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading. Specified values are obtained with minimum cycle time and the outputs open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is assured.
7. An initial pause of 100µs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is assured. The 8 $\overline{RAS}$ cycle wake-up should be repeated any time the ^tREF refresh requirement is exceeded.
8. AC characteristics assume ^tT = 5ns.
9. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}). Input signals transition between 0V and 3V for AC testing.
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS}$ = V_{IH}, DRAM data outputs (DQ1-DQ4) is High-Z.
12. If $\overline{CAS}$ = V_{IL}, DRAM data outputs (DQ1-DQ4) may contain data from the last valid READ cycle.
13. DRAM output timing measured with a load equivalent to 2 TTL gates and 100pF. Output reference levels: V_{OH} = 2.0V; V_{OL} = 0.8V.
14. Assumes that ^tRCD < ^tRCD (MAX). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
15. Assumes that ^tRCD ≥ ^tRCD (MAX).
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, DQ will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer, $\overline{CAS}$ must be pulsed HIGH for ^tCP.
17. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (MAX) limit, then access time is controlled exclusively by ^tCAC.
18. Operation within the ^tRAD (MAX) limit ensures that ^tRCD (MAX) can be met. ^tRAD (MAX) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (MAX) limit, then access time is controlled exclusively by ^tAA.
19. Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
20. ^tOD, ^tOFF and ^tSEZ define the time when the output achieves open circuit (V_{OH} -200mV, V_{OL} +200mV). This parameter is sampled and not 100% tested.
21. ^tWCS, ^tRWD, ^tAWD and ^tCWD are restrictive operating parameters in LATE-WRITE, READ-WRITE and READ-MODIFY-WRITE cycles only. If ^tWCS ≥ ^tWCS (MIN), the cycle is an EARLY-WRITE cycle and the data output will remain an open circuit throughout the entire cycle, regardless of $\overline{TR}/\overline{OE}$. If ^tWCS ≤ ^tWCS (MIN), the cycle is a LATE-WRITE and $\overline{TR}/\overline{OE}$ must control the output buffers during the WRITE to avoid data contention. If ^tRWD ≥ ^tRWD (MIN), ^tAWD ≥ ^tAWD (MIN) and ^tCWD ≥ ^tCWD (MIN), the cycle is a READ-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of the output buffers (at access time and until $\overline{CAS}$ goes back to V_{IH}) is indeterminate but the WRITE will be valid, if ^tOD and ^tOEH are met. See the LATE-WRITE AC Timing diagram.
22. These parameters are referenced to $\overline{CAS}$ leading edge in early WRITE cycles and $\overline{ME}/\overline{WE}$ leading edge in late WRITE or READ-WRITE cycles.
23. During a READ cycle, if $\overline{TR}/\overline{OE}$ is LOW then taken HIGH, DQ goes open. The DQs will go open with $\overline{OE}$ or $\overline{CAS}$, whichever goes HIGH first.
24. SAM output timing is measured with a load equivalent to 1 TTL gate and 50pF. Output reference levels: V_{OH} = 2.0V; V_{OL} = 0.8V.
25. Addresses (A0-A8) change two times or less while $\overline{RAS}$ = V_{IL}.
26. Addresses (A0-A8) change once or less while $\overline{RAS}$ = V_{IL}.
27. Addresses (A0-A8) change once or less while $\overline{CAS}$ = V_{IH} and $\overline{RAS}$ = V_{IL}.
28. LATE-WRITE and READ-MODIFY-WRITE cycles must have ^tOD and ^tOEH met ($\overline{OE}$ HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. The DQs will provide previously read data if $\overline{CAS}$ remains LOW and $\overline{OE}$ is taken LOW after ^tOEH is met. If $\overline{CAS}$ goes HIGH prior to $\overline{OE}$ going back LOW, the DQs will remain open.
29. Applies to the MT43C4257 only.
30. Applies to the MT43C4258 only.
31. ^tSAC is MAX at 70° C and 4.75V Vcc; ^tSOH is MIN at 0°C and 5.25V Vcc. These limits will not occur simultaneously at any given voltage or temperature. ^tSOH = ^tSAC - output transition time, this is guaranteed by design.

DRAM READ CYCLE



DRAM FAST-PAGE-MODE READ CYCLE

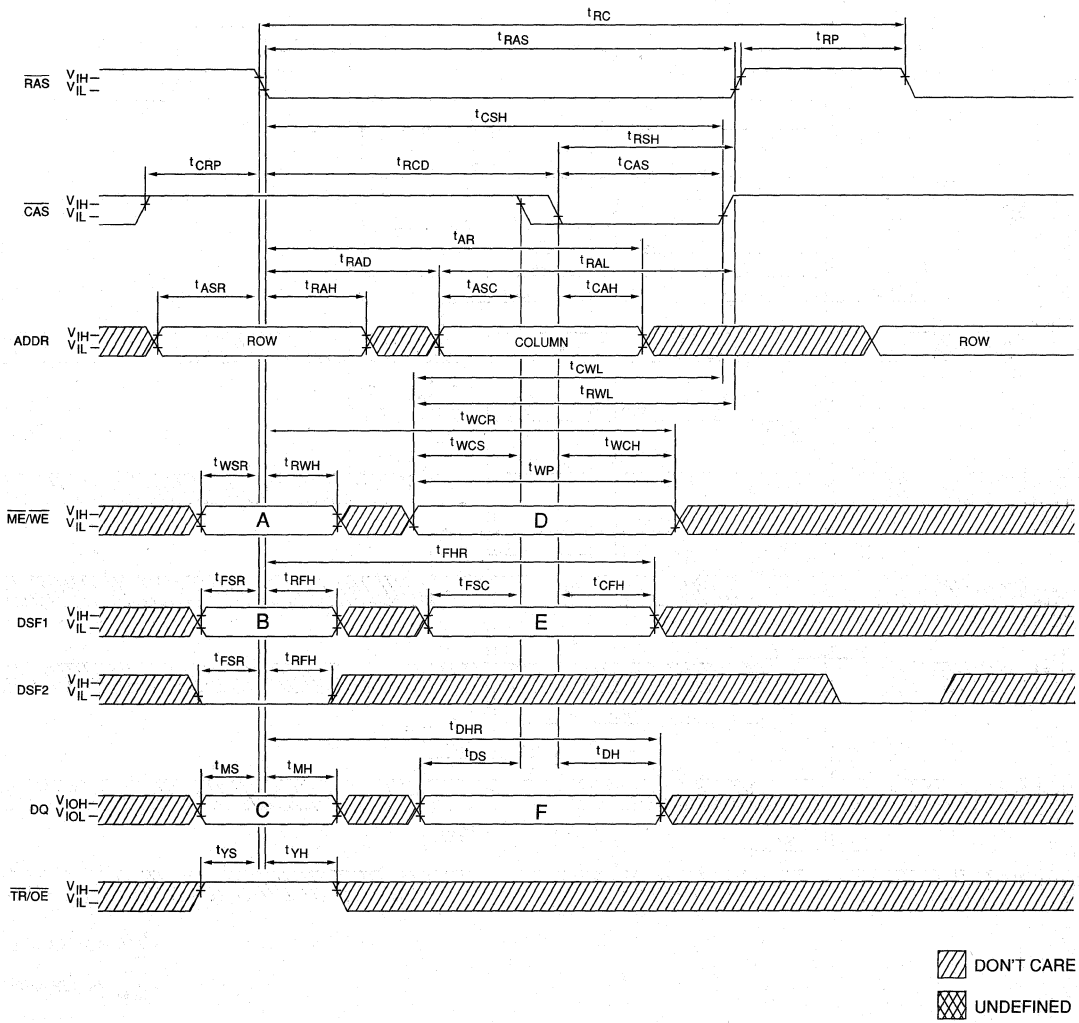


WRITE CYCLE FUNCTION TABLE [1]

CODE	FUNCTION	LOGIC STATES[2]					
		RAS Falling Edge			CAS Falling Edge		
		A ME/WE	B DSF1	C DQ (Input)	D ME/WE	E DSF1	F DQ (Input)
RW	Normal DRAM WRITE	1	0	X	0	0	DRAM
RWNM	NONPERSISTENT (Load and Use) MASKED WRITE to DRAM	0	0	Write Mask	0/1[3]	0	DRAM (Masked)
RWOM	PERSISTENT (Use Register) MASKED WRITE to DRAM	0	1	X	0/1[3]	0	DRAM (Masked)
BW	BLOCK WRITE to DRAM (No DQ Mask)	1	0	X	0/1[3]	1	Column Mask
BWNM	NONPERSISTENT (Load and Use) MASKED BLOCK WRITE to DRAM	0	0	Write Mask	0/1[3]	1	Column Mask
BWOM	PERSISTENT (Use Register) MASKED BLOCK WRITE to DRAM	0	1	X	0/1[3]	1	Column Mask
LMR	Load Mask Data Register	1	1	X	0/1[3]	0	Write Mask
LCR	Load Color Register	1	1	X	0/1[3]	1	Color Mask

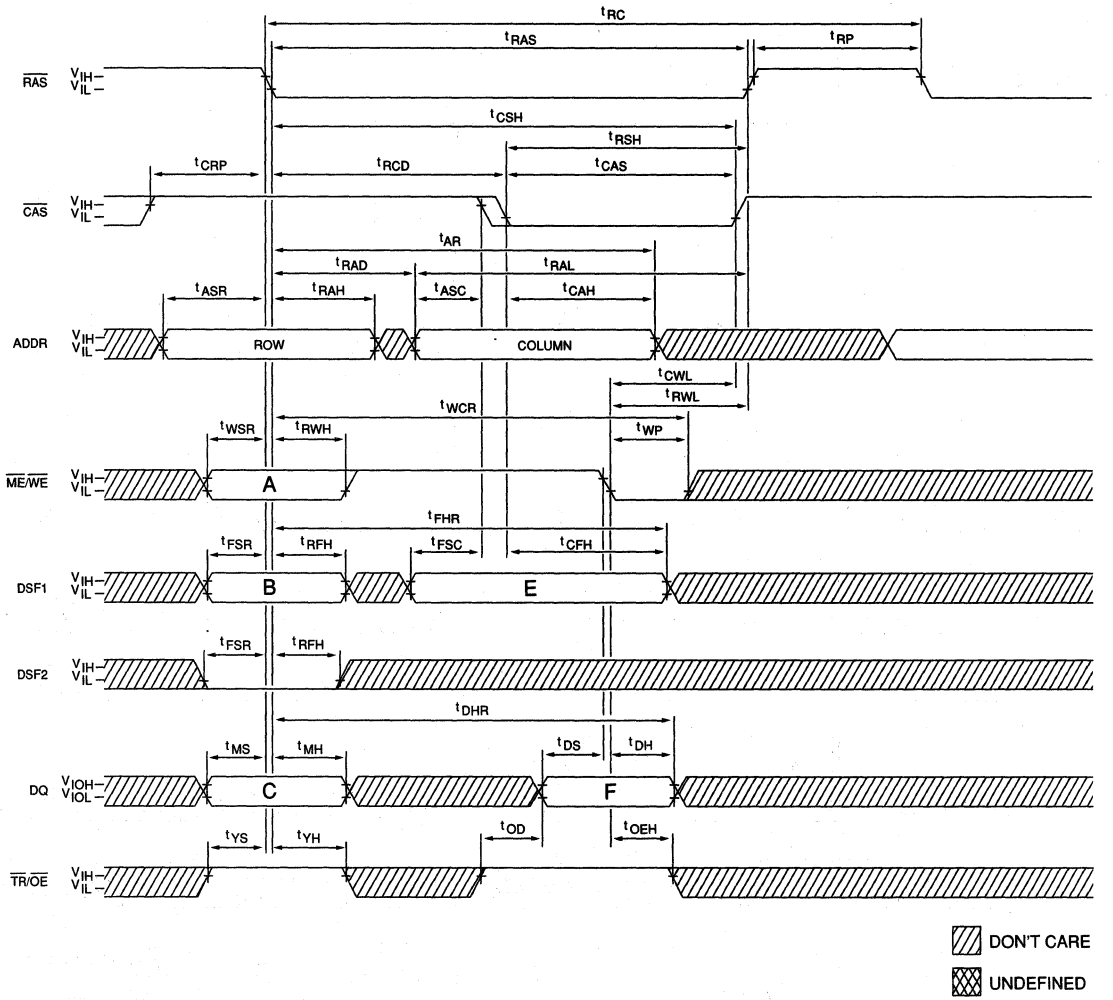
NOTE:
1. Refer to this function table to determine the logic states of "A", "B", "C", "D", "E" and "F" for the WRITE cycle timing diagrams on the following pages.
2. TRM, MKD and STS are "don't care" for all WRITE cycles.
3. If $\overline{ME}/\overline{WE}$ is LOW, an EARLY-WRITE is performed; if it is HIGH, a LATE-WRITE is performed if $\overline{ME}/\overline{WE}$ falls after $\overline{CAS}$.

DRAM EARLY-WRITE CYCLE



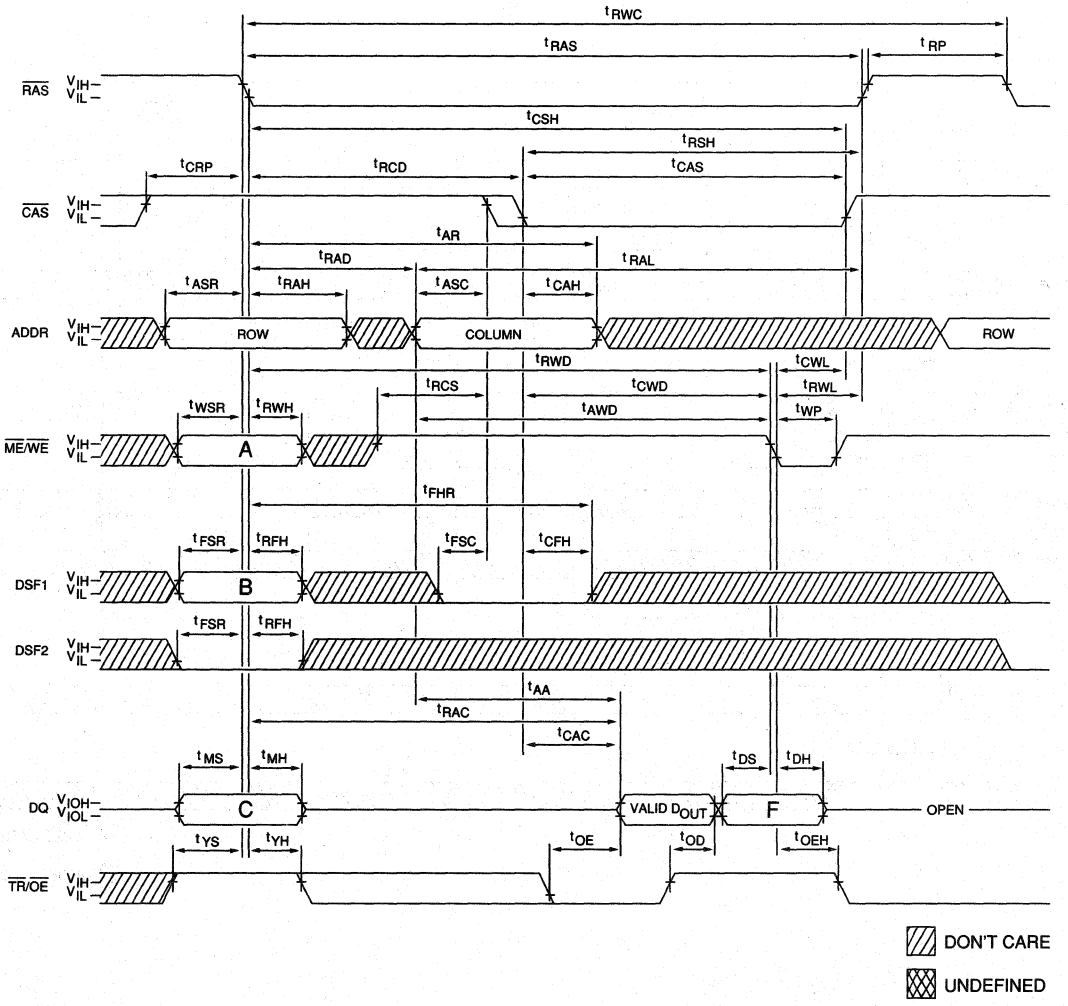
NOTE: The logic states of "A", "B", "C", "E" and "F" determine the type of WRITE operation performed. See the Write Cycle Function Table for a detailed description.

DRAM LATE-WRITE CYCLE [1]



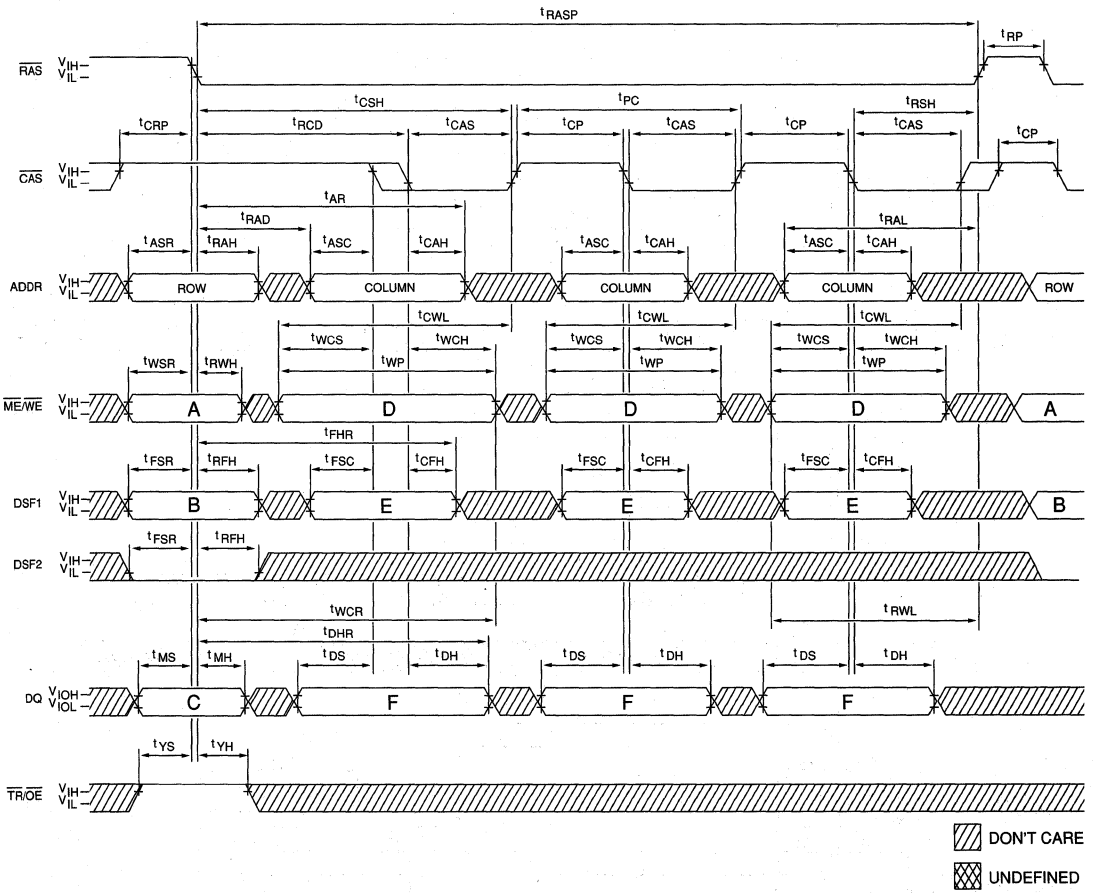
NOTE: 1. The logic states of "A", "B", "C", "E", and "F" determine the type of WRITE operation performed. See the Write Cycle Function Table for a detailed description.

DRAM READ-WRITE CYCLE
(READ-MODIFY-WRITE CYCLE)



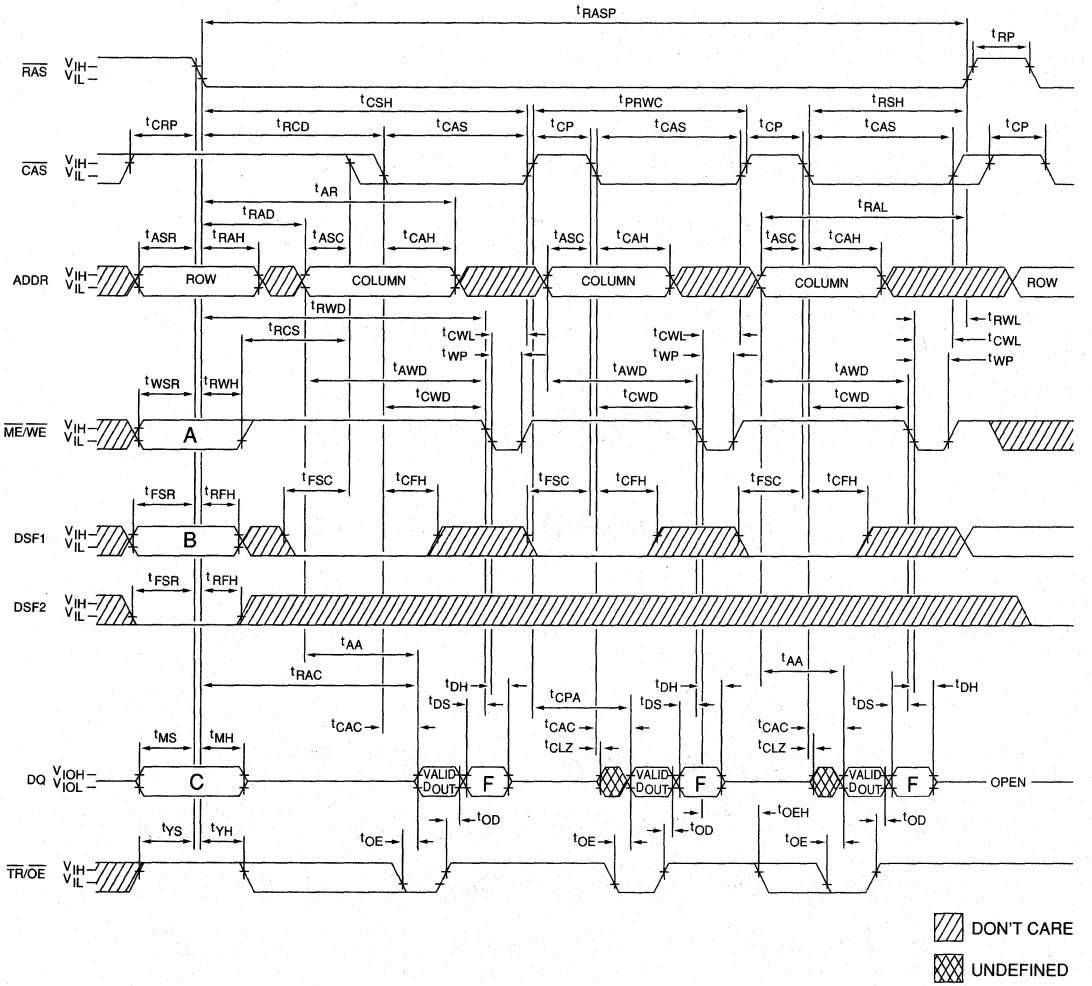
NOTE: The logic states of "A", "B", "C" and "F" determine the type of WRITE operation performed. See the Write Cycle Function Table for a detailed description.

DRAM FAST-PAGE-MODE EARLY-WRITE CYCLE [1, 2]



NOTE:
1. READ cycles or READ-MODIFY-WRITE cycles may be mixed with WRITE cycles while in FAST PAGE MODE.
2. The logic states of "A", "B", "C", "D", "E" and "F" determine the type of WRITE operation performed. See the Write Cycle Function Table for a detailed description.

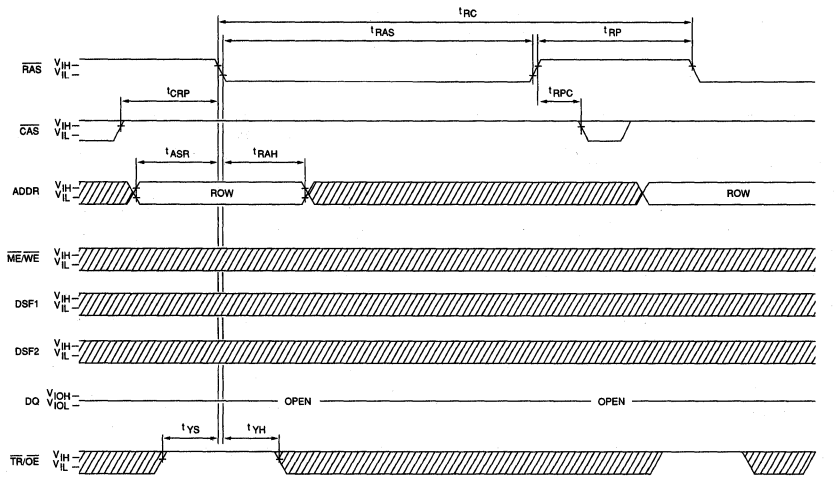
DRAM FAST-PAGE-MODE READ-WRITE CYCLE
(READ-MODIFY-WRITE or LATE-WRITE CYCLES)



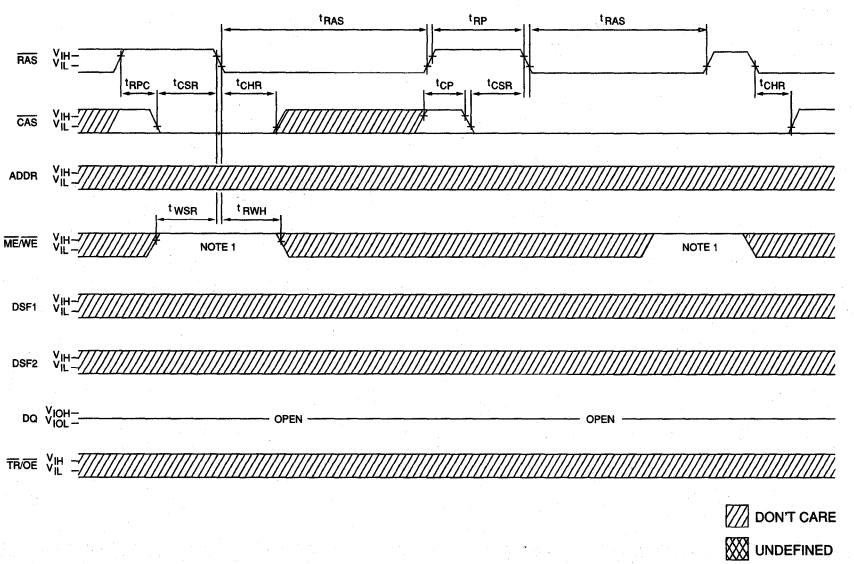
NOTE:
1. READ or WRITE cycles may be mixed with READ-MODIFY-WRITE cycles while in FAST PAGE MODE. Use the Write Function Table to determine the proper DSF1 state for the desired WRITE operation.
2. The logic states of "A", "B", "C" and "F" determine the type of WRITE operation performed. See the Write Cycle Function Table for a detailed description.

MULTIPORT DRAM

DRAM $\overline{RAS}$-ONLY REFRESH CYCLE
(ADDR = A0-A8)

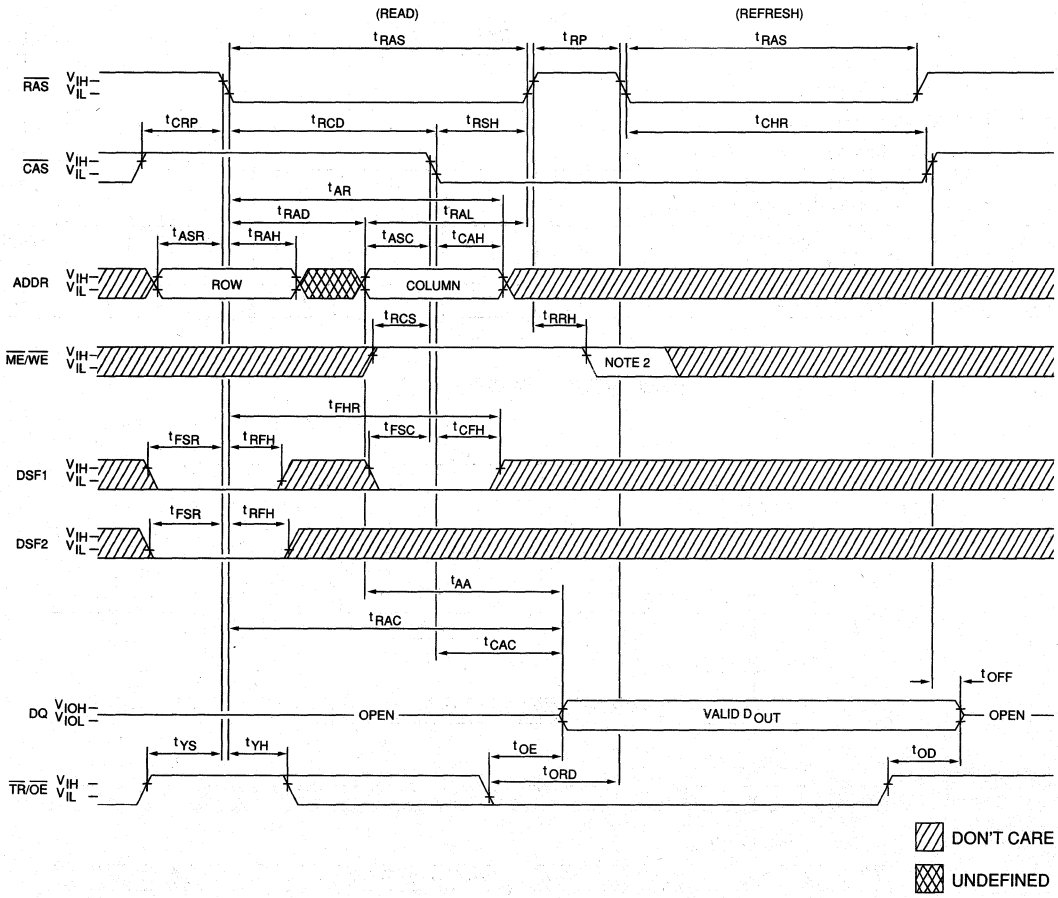


$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE



NOTE: 1. The MT43C4257/8 operates with this state as "don't care," but to allow for future functional enhancements, it is recommended that they be driven as illustrated for system upgradability.

DRAM HIDDEN-REFRESH CYCLE

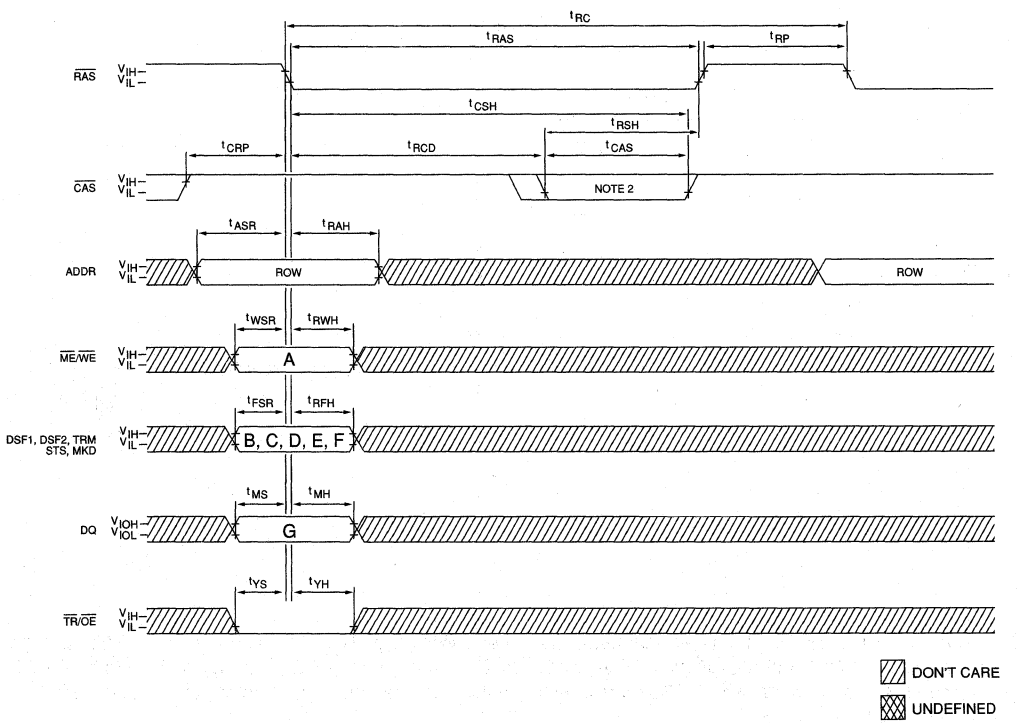


NOTE:
1. A HIDDEN REFRESH may also be performed after a WRITE or TRANSFER cycle. In the WRITE case, $\overline{ME}/\overline{WE}$ = LOW (when $\overline{CAS}$ goes LOW) and $\overline{TR}/\overline{OE}$ = HIGH and the DQ pins stay High-Z. In the TRANSFER case, $\overline{TR}/\overline{OE}$ = LOW (when $\overline{RAS}$ goes LOW) and the DQ pins stay High-Z during the refresh period, regardless of $\overline{TR}/\overline{OE}$.
2. The MT43C4257/8 operates with this state as "don't care," but to allow for future functional enhancements, it is recommended that they be driven as illustrated for system upgradability.

DRAM/BMR TRANSFER CYCLE FUNCTION TABLE [1]

CODE	FUNCTION	LOGIC STATES						
		$\overline{RAS}$ Falling Edge						
		A $\overline{ME/WE}$	B DSF1	C DSF2	D TRM	E STS	F MKD	G DQ(Input)
BMR-RT	BMR READ TRANSFER (DRAM→BMR TRANSFER)	1	0	0	1	0	0/1[1]	X
BMR-IRT	BMR $\overline{READ}$ TRANSFER (DRAM→invert→BMR TRANSFER)	1	0	0	1	1	0/1[1]	X
BMR-WT	BMR WRITE TRANSFER (BMR→DRAM TRANSFER)	0	0	0	1	0	0/1[1]	Mask
BMR-IWT	BMR $\overline{WRITE}$ TRANSFER (BMR→invert→DRAM TRANSFER)	0	0	0	1	1	0/1[1]	Mask
CLR-BMR	CLEAR BMR (CLR-BMR)	1	1	1	0	X	0/1[1]	X

DRAM/BMR TRANSFERS



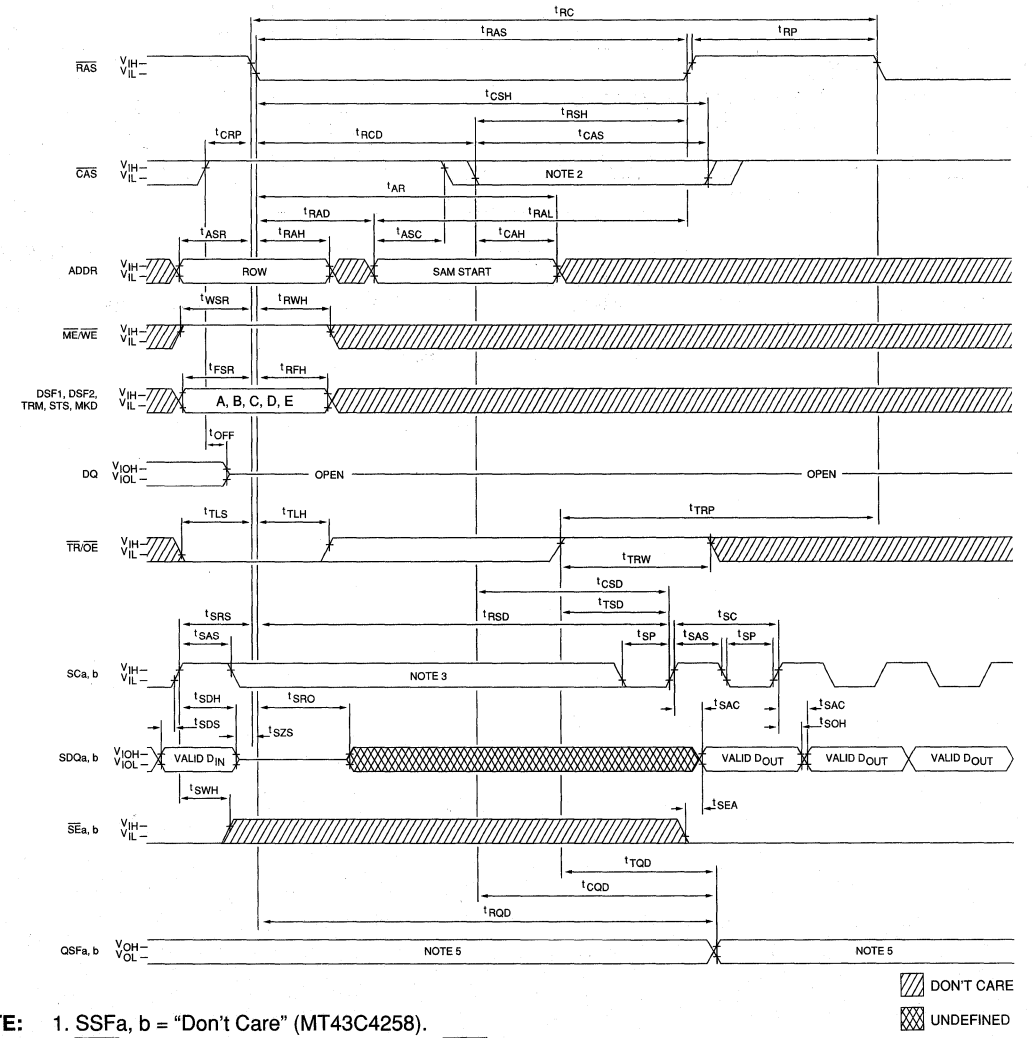
NOTE: 1. Serial Mask Input mode is enabled if MKD = HIGH; disabled if MKD = LOW.
2. It is not necessary to drop $\overline{CAS}$ during a DRAM/BMR TRANSFER.

READ TRANSFER CYCLE FUNCTION TABLE [1]

CODE	FUNCTION	LOGIC STATES				
		$\overline{RAS}$ Falling Edge				
		A DSF1	B DSF2	C TRM	D STS	E MKD
RW	READ TRANSFER	0	0	0	0/1[2]	X
SRT	SPLIT READ TRANSFER (DRAM→SAM)	1	0	0	0/1[2]	X
BMRT	BIT MASKED READ TRANSFER	0	1	1	0/1[2]	X
BMSRT	BIT MASKED SPLIT READ TRANSFER	1	1	1	0/1[2]	X
BMR-SAM	BMR→SAM TRANSFER	1	0	1	0/1[2]	0/1[3]

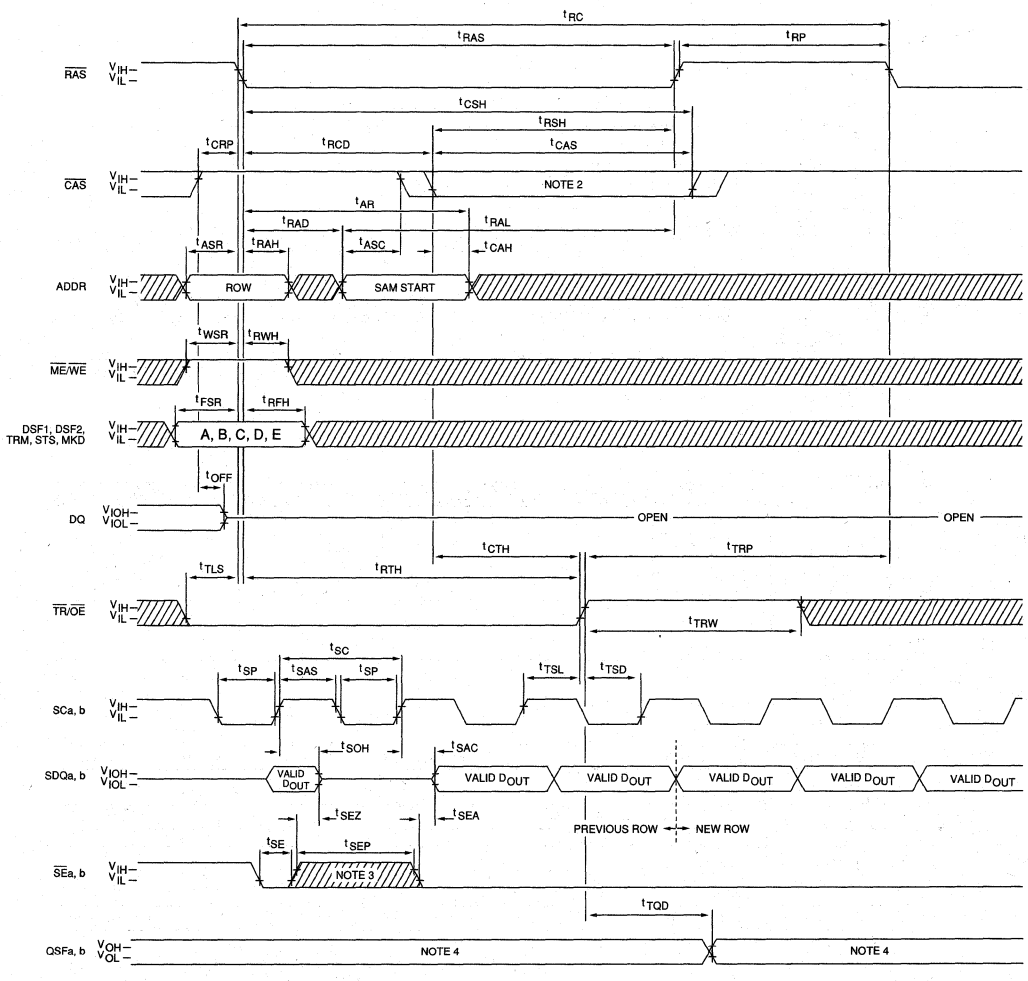
NOTE:
1. Refer to this function table to determine the logic states of "A", "B", "C", "D" and "E" for READ TRANSFER cycle timing diagrams on the following pages.
2. The state of STS at the falling edge of $\overline{RAS}$ determines the SAM involved in the transfer. When STS = LOW, the transfer is to SAMa; when STS = HIGH, the transfer is to SAMb.
3. Serial Mask Input mode is enabled if MKD = HIGH; disabled if MKD = LOW.

READ TRANSFER [1, 4]
(DRAM-TO-SAM TRANSFER)
(When part was previously in the SERIAL INPUT mode)



NOTE:
1. SSFa, b = "Don't Care" (MT43C4258).
2. $\overline{CAS}$ is used to load the Tap address. If $\overline{CAS}$ does not fall, the last Tap address loaded for the addressed SAM will be reused.
3. There must be no rising edges on the SC input during this time period.
4. The logic states of "A", "B", "C", "D" and "E" determine the type of TRANSFER operation performed. See the Read Transfer Cycle Function Table.
5. QSF = 0 when the Lower SAM (bits 0–255) is being accessed.
   QSF = 1 when the Upper SAM (bits 256–511) is being accessed.

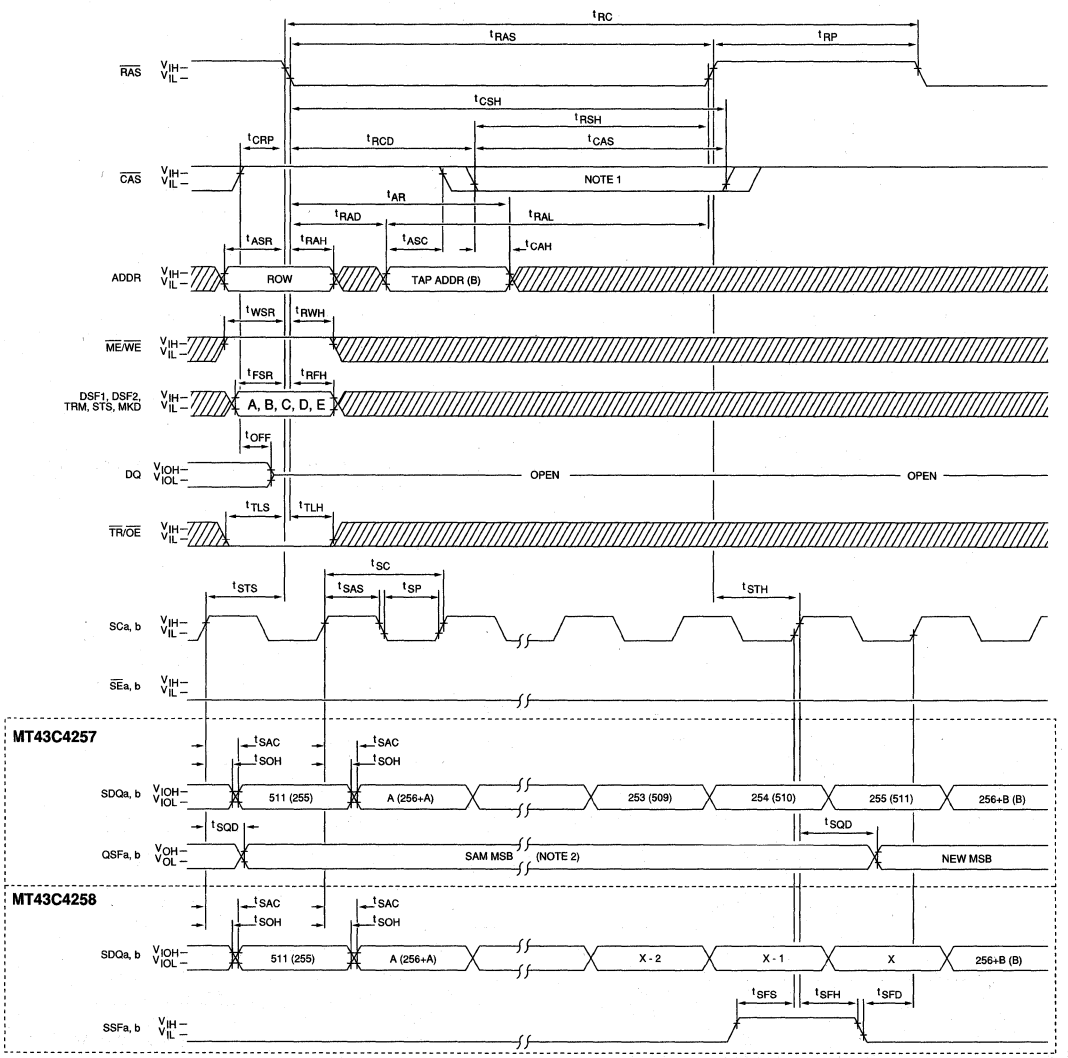
REAL-TIME READ TRANSFER [1, 5]
(DRAM-TO-SAM TRANSFER)
(When part was previously in the SERIAL OUTPUT mode)



DON'T CARE
UNDEFINED

NOTE:
1. SSFa, b = "Don't Care" (MT43C4258).
2. $\overline{CAS}$ is used to load the Tap address. If $\overline{CAS}$ does not fall, the last Tap address loaded for the addressed.
3. The $\overline{SE}$ pulse is shown to illustrate the serial output enable and disable timing. It is not required.
4. QSF = 0 when the Lower SAM (bits 0–255) is being accessed.
   QSF = 1 when the Upper SAM (bits 256–511) is being accessed.
5. The logic states of "A", "B", "C", "D" and "E" determine the type of TRANSFER operation performed. See the Read Transfer Cycle Function Table.

SPLIT READ TRANSFER [3]
(SPLIT DRAM-TO-SAM TRANSFER)



DON'T CARE
UNDEFINED

NOTE:
1. $\overline{CAS}$ is used to load the Tap address. If $\overline{CAS}$ does not fall, the last Tap address loaded for the addressed SAM will be reused for the idle half.
2. QSF = 0 when the Lower SAM (bits 0–255) is being accessed.
   QSF = 1 when the Upper SAM (bits 256–511) is being accessed.
3. The logic states of "A", "B", "C", "D" and "E" determine the type of TRANSFER operation performed. See the Read Transfer Cycle Function Table.

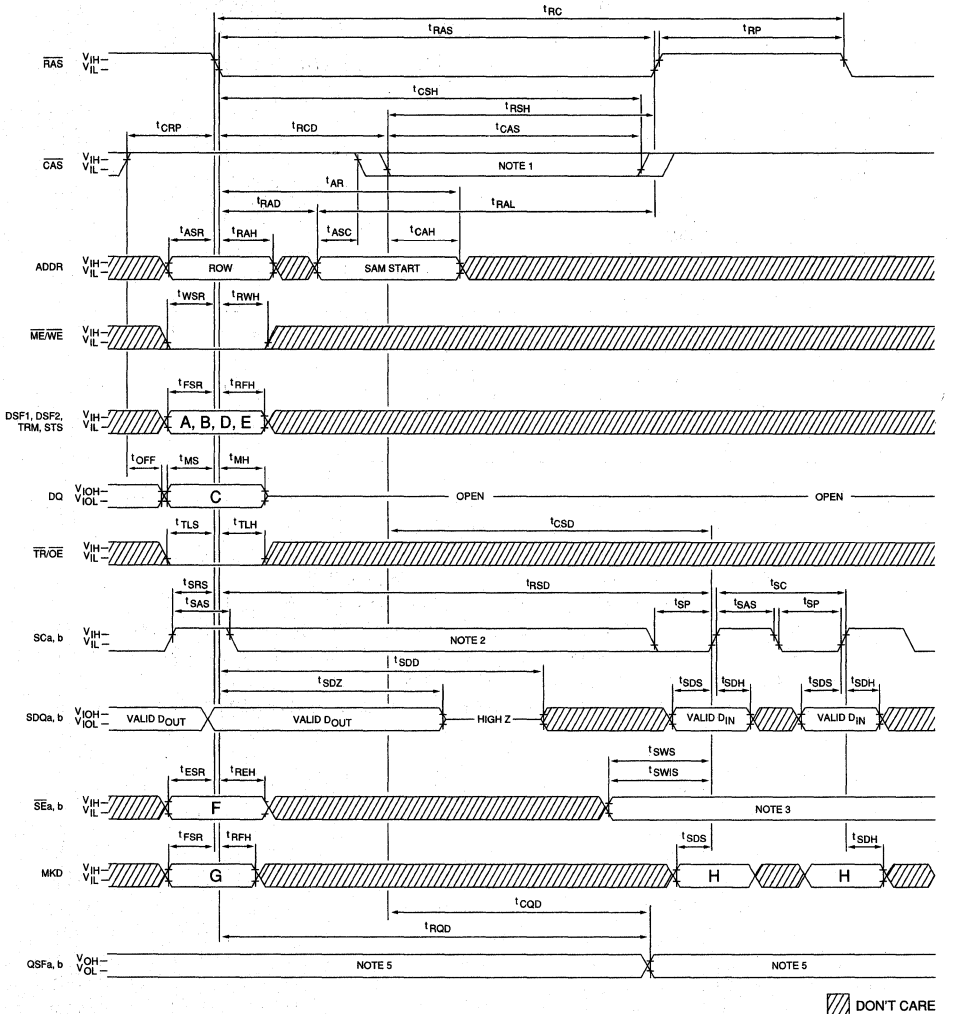
WRITE TRANSFER CYCLE FUNCTION TABLE [1]

CODE	FUNCTION	LOGIC STATES							
		RAS Falling Edge							SC
		A DSF1	B DSF2	C DQ	D TRM	E STS	F $\overline{SE}$	G MKD	H MKD
WT	WRITE TRANSFER (SAM→DRAM)	0	0	X	0	0/1[2]	0	X	-
PWT	PSEUDO WRITE TRANSFER	0	0	X	0	0/1[2]	1	X	-
MSWT	DQ MASKED SPLIT WRITE TRANSFER (SAM→DRAM)	1	0	Mask	0	0/1[2]	X	X	-
MWT	DQ MASKED WRITE TRANSFER (SAM→DRAM)	0	1	Mask	0	0/1[2]	X	X	-
BMWT	BIT MASKED WRITE TRANSFER (SAM→DRAM)	0	1	X	1	0/1[2]	X	X	0/1[4]
BMSWT	BIT MASKED SPLIT WRITE TRANSFER (SAM→DRAM)	1	1	Mask	1	0/1[2]	X	X	0/1[4]
SAM-BMR	(SAM→BMR) TRANSFER	1	0	X	1	0/1[2]	X	0/1[3]	-

NOTE:
1. Refer to this function table to determine the logic states of "A", "B", "C", "D", "E" , "F", "G", and "H" for WRITE TRANSFER cycle timing diagrams on the following pages.
2. The state of STS at the falling edge of RAS determines the SAM involved in the transfer. When STS = LOW, the transfer is to SAMa; when SAM = HIGH, the transfer is to SAMb.
3. Serial Mask Input (SMI) mode is enabled if MKD = HIGH and disabled if MKD = LOW.
4. When in the SMI mode (see BMR transfer waveforms) MKD is the SMI data input. MKD data is clocked into all bit planes of the bit mask register with SCb. A logic "1" on MKD will allow data to pass through the mask; a logic "0" will mask the corresponding location of the SAM during a BIT MASKED TRANSFER. BIT MASKED TRANSFERs to or from SAMa must not take place while mask data is being serially input via SCb and MKD.

WRITE TRANSFER [4]

(When part was previously in the SERIAL OUTPUT mode)

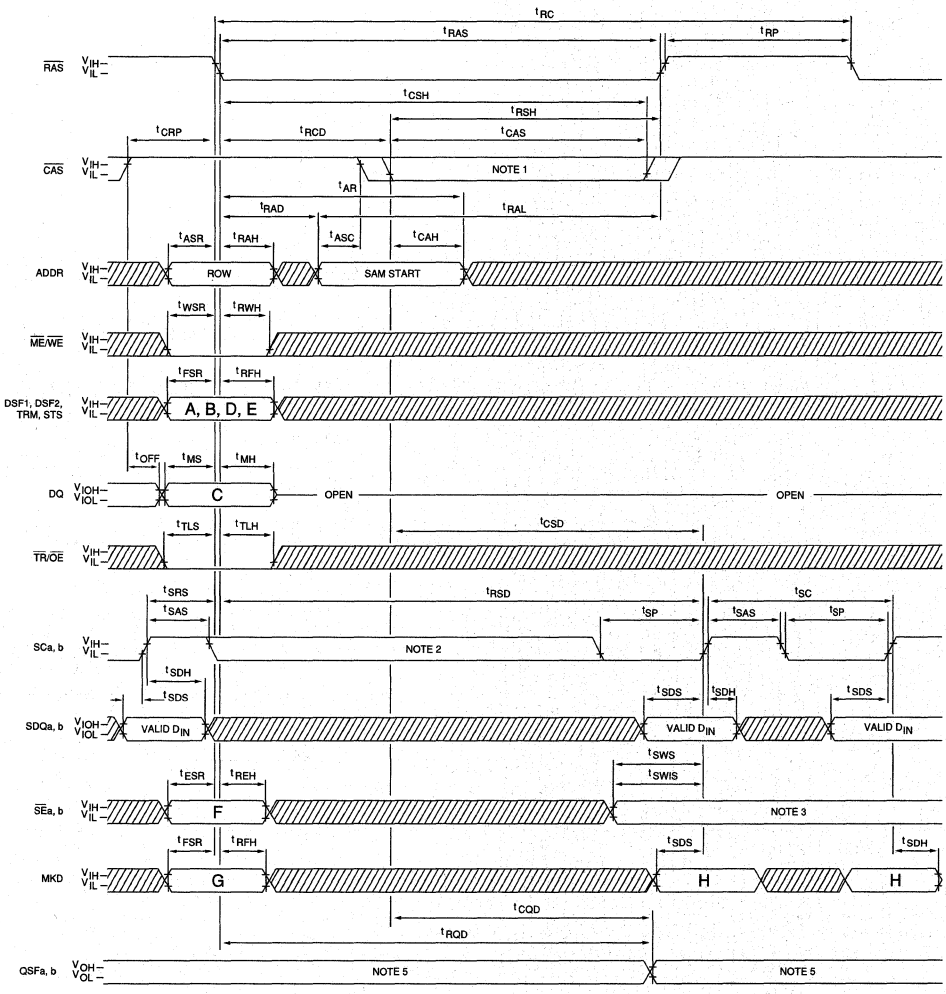


NOTE:

1. $\overline{CAS}$ is used to load the Tap address. If $\overline{CAS}$ does not fall, the last Tap address loaded for the addressed SAM will be reused.
2. There must be no rising edges on the SC input during this time period.
3. $\overline{SE}$ must be LOW to input new serial data, but the serial address register is incremented by SC regardless of $\overline{SE}$.
4. The logic states of "A", "B", "C", "D", "E", "F", "G" and "H" determine the type of TRANSFER operation performed. See the Write Transfer Cycle Function Table.
5. QSF = 0 when the Lower SAM (bits 0–255) is being accessed.
   QSF = 1 when the Upper SAM (bits 256–511) is being accessed. SSFa,b = "don't care" (MT43C4258).

WRITE TRANSFER [4]

(When part was previously in the SERIAL INPUT mode)

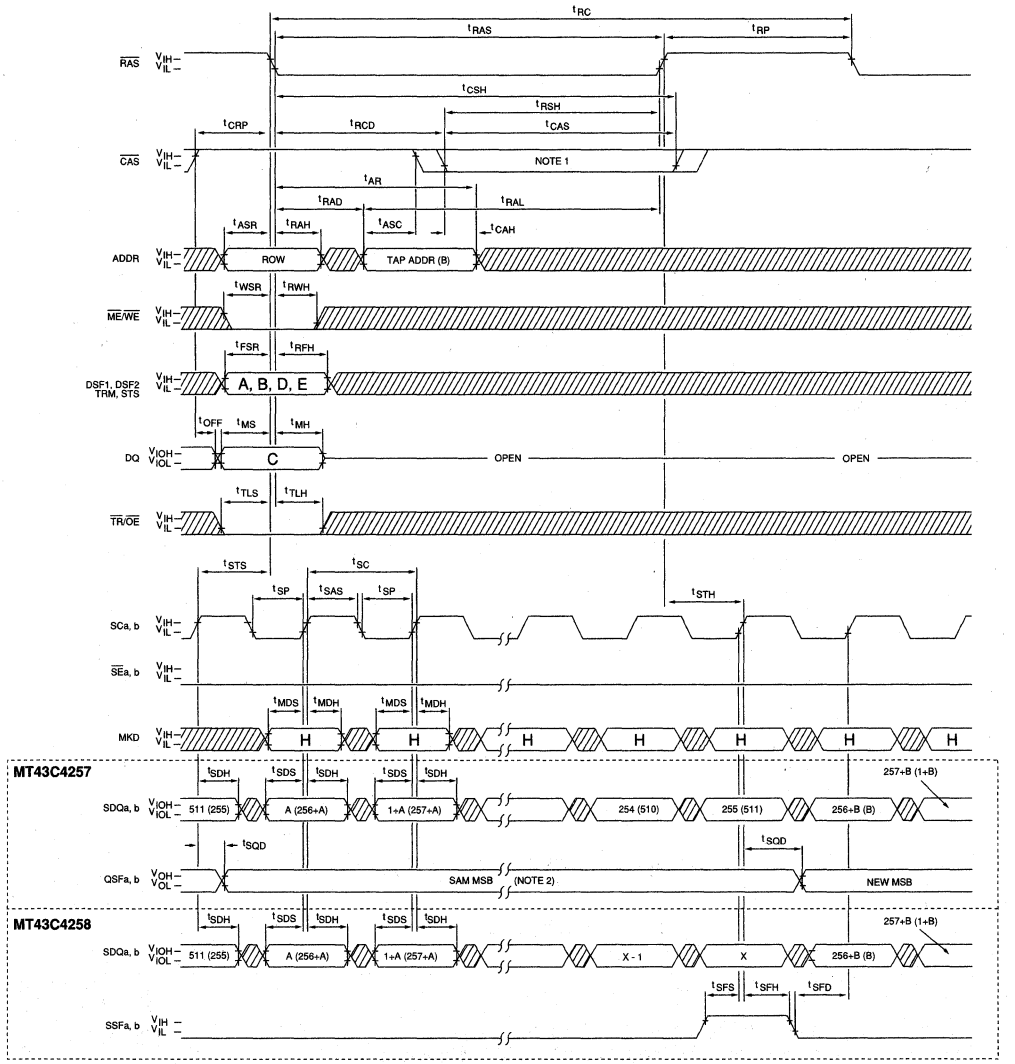


NOTE:

1. $\overline{CAS}$ is used to load the Tap address. If $\overline{CAS}$ does not fall, the last Tap address loaded for the addressed SAM will be reused.
2. $\overline{SE}$ must be LOW to input new serial data, but the serial address register is incremented by SC regardless of $\overline{SE}$.
3. There must be no rising edges on the SC input during this time period.
4. The logic states of "A", "B", "C", "D", "E", "F", "G" and "H" determine the type of TRANSFER operation performed. See the Write Transfer Cycle Function Table.
5. QSF = 0 when the Lower SAM (bits 0–255) is being accessed.
   QSF = 1 when the Upper SAM (bits 256–511) is being accessed. SSFa,b = "don't care" (MT43C4258).

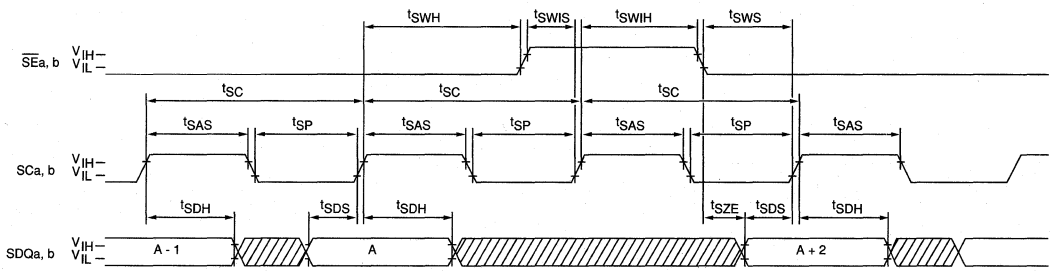
MULTIPORT DRAM

SPLIT WRITE TRANSFER [3]
(SPLIT SAM-TO-DRAM TRANSFER)

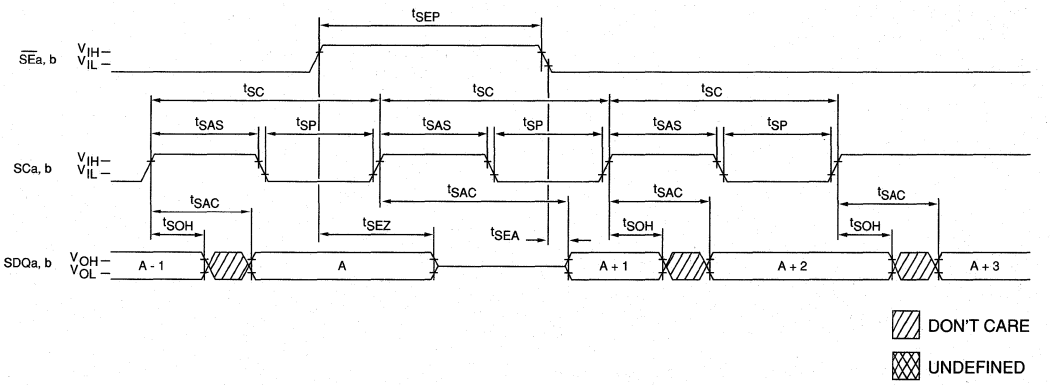


NOTE:
1. $\overline{CAS}$ is used to load the Tap address. If $\overline{CAS}$ does not fall, the last Tap address loaded for the addressed SAM will be reused.
2. QSF = 0 when the Lower SAM (bits 0–255) is being accessed.
   QSF = 1 when the Upper SAM (bits 256–511) is being accessed.
3. The logic states of "A", "B", "C", "D", "E" and "H" determine the type of TRANSFER operation performed. See the Write Transfer Cycle Function Table.

SAMa or SAMb SERIAL INPUT



SAMa or SAMb SERIAL OUTPUT



NOTE : $\overline{SE}$a, SCa and SDQa are used when accessing SAMa and $\overline{SE}$b; SCb and SDQb are used when access in SAMb.

TRIPLE PORT DRAM

128K x 8 DRAM WITH DUAL 256 x 8 SAMS

FEATURES

- Three asynchronous, independent, data access ports
- Fast access times – 80ns random, 25ns serial
- Operation and control compatible with 1 Meg VRAMs
- High-performance, CMOS silicon-gate process
- Inputs and outputs are fully TTL compatible
- Low power: 15mW standby; 550mW active, typical
- 512-cycle refresh within 8ms
- Refresh modes: $\overline{\text{RAS}}$-ONLY, $\overline{\text{CAS}}$-BEFORE-$\overline{\text{RAS}}$ (CBR) and HIDDEN
- FAST PAGE MODE access cycles
- Two bidirectional serial access memories (SAMs)
- Fully static SAMs and Mask Register, no refresh required
- 2,048-bit Bit Mask Register
- SERIAL MASK DATA INPUT mode

SPECIAL FUNCTIONS

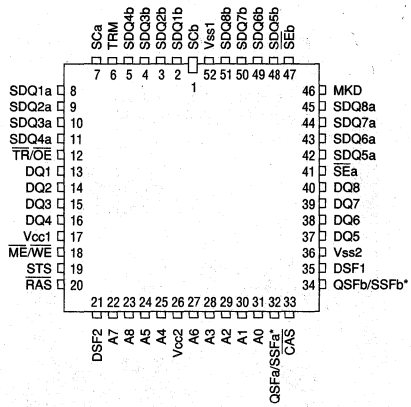
- MASKED WRITE (Write-Per-Bit)
- PERSISTENT MASKED WRITE
- SPLIT READ AND WRITE TRANSFERS
- BLOCK WRITE
- BIT MASKED TRANSFERS

OPTIONS — MARKING

- Timing [DRAM, SAMs (cycle/access)]
  80ns, 28ns/25ns — -8
  100ns, 30ns/27ns — -10
- Packages
  Plastic LCC (750 mil) — EJ
- Functionality
  QSF output — MT43C8128
  (indicates SAM half accessed)
  SSF input — MT43C8129
  (Split SAM special function, stop count)

PIN ASSIGNMENT (Top View)

52-PIN PLCC
(P-1)



*MT43C8128/MT43C8129

GENERAL DESCRIPTION

The MT43C8128/9 are high speed, triple port CMOS dynamic random access memories (TPDRAM) containing 1,048,576 bits. Data may be accessed by an 8 bit wide DRAM port or by either of two independently-clocked 256 x 8-bit serial access memory (SAM) ports. Data may be transferred bidirectionally between the DRAM and the SAMs.

The DRAM portion of the TPDRAM is functionally identical to the MT4C4256 (256K x 4) DRAM. Sixteen 256-bit data registers make up the serial access memory portions of the TPDRAM. Data I/O and internal data transfer are accomplished using five separate bidirectional data paths; the 8-bit random access I/O port, a pair of internal 2,048 bit wide paths between the DRAM and the SAMs, and the pair of 8-bit serial I/O ports for the SAMs. The rest of the circuitry consists of the control, timing, and address decoding logic.

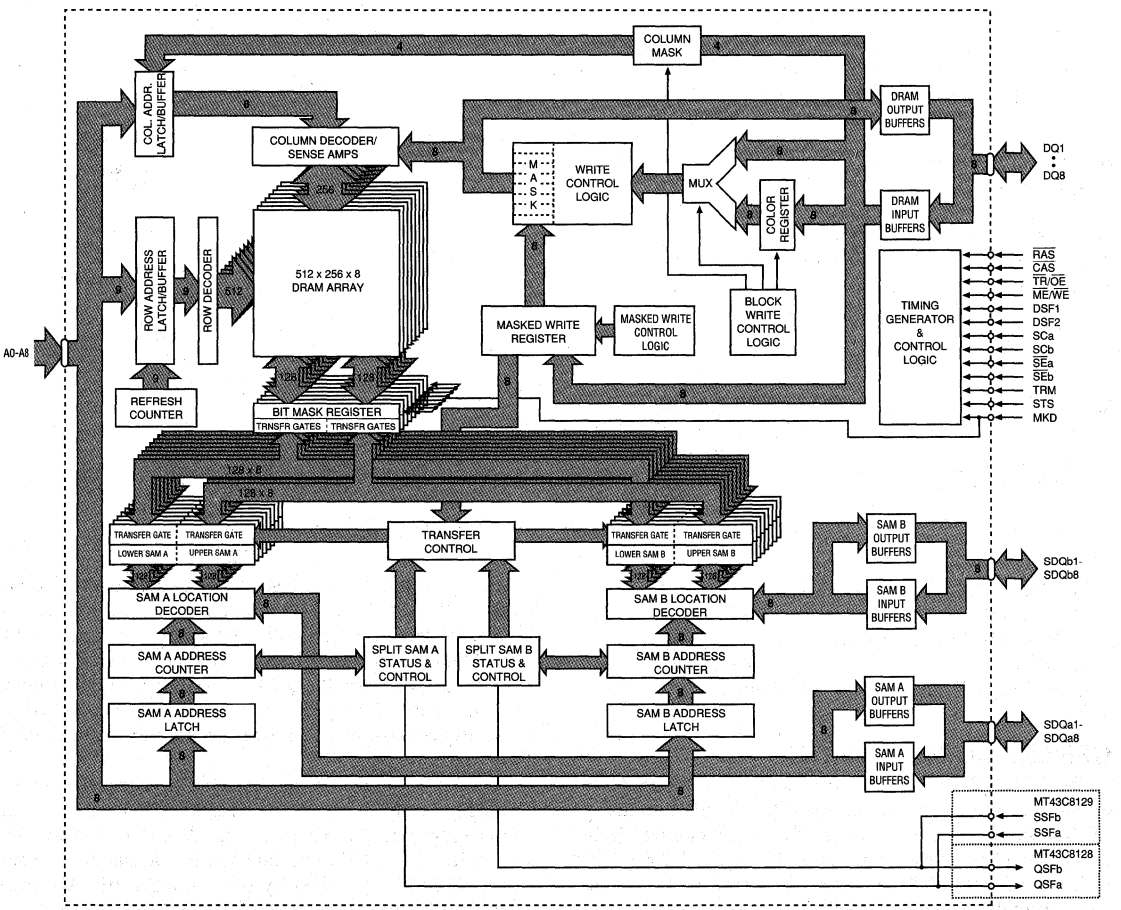
All three ports may be operated asynchronously and independently of the others except when data is being internally transferred between the DRAM and either SAM.

Each of the 2,048 bits involved in an internal transfer may be individually masked by performing a BIT MASKED TRANSFER operation. The 256 x 8-bit Bit Mask Data Register can be parallel loaded from the DRAM or either SAM, or it may be serial loaded through the MKD serial input.

As with all DRAMs, the TPDRAM must be refreshed to maintain data. The refresh cycles must be timed so that all 512 combinations of $\overline{RAS}$ addresses are executed at least every 8ms (regardless of sequence). Micron recommends evenly spaced refresh cycles for maximum data integrity. An internal transfer between the DRAM and either SAM counts as a refresh cycle. The SAM portions of the TPDRAM are fully static and do not require any refresh.

The operation and control of the MT43C8128/9 are optimized for high performance graphics and communication designs. The triple port architecture is well suited to buffering the sequential data types used in rastor graphics display, video windowing, serial/parallel networking and data communications. Special features, such as SPLIT TRANSFER, BIT MASKED TRANSFERs and BLOCK WRITE allow further enhancements to system performance.

FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTIONS

PLCC PIN NUMBER	SYMBOL	TYPE	DESCRIPTION
7	SCa	Input	Serial Clock, SAMa: Clock input to the serial address counter for the SAMa registers and strobe for SAMa control and data inputs.
1	SCb	Input	Serial Clock, SAMb: Clock input to the serial address counter for the SAMb registers and strobe for SAMb control and data inputs.
12	$\overline{TR}/\overline{OE}$	Input	Transfer Enable: Enables an internal TRANSFER operation at the falling edge of $\overline{RAS}$, or Output Enable: Enables the DRAM output buffers when taken LOW after $\overline{RAS}$ goes LOW ($\overline{CAS}$ must also be LOW), otherwise the output buffers are in a high impedance state.
18	$\overline{ME}/\overline{WE}$	Input	Mask Enable: If $\overline{ME}/\overline{WE}$ is LOW at the falling edge of $\overline{RAS}$, a MASKED WRITE cycle is performed, or Write Enable: $\overline{ME}/\overline{WE}$ is also used to select a READ ($\overline{ME}/\overline{WE}$ = H) or WRITE ($\overline{ME}/\overline{WE}$ = L) cycle when accessing the DRAM. This includes a READ TRANSFER ($\overline{ME}/\overline{WE}$ = H) or WRITE TRANSFER ($\overline{ME}/\overline{WE}$ = L).
41	$\overline{SE}$a	Input	Serial Port Enable SAMa: $\overline{SE}$a enables Port A serial I/O buffers and allows a serial READ or WRITE operation to occur; otherwise, the output buffers are in a High-Z state. $\overline{SE}$a is also used during a TRANSFER operation to indicate whether a WRITE TRANSFER or a SERIAL INPUT MODE ENABLE (PSEUDO WRITE TRANSFER) cycle is performed.
47	$\overline{SE}$b	Input	Serial Port Enable, SAMb: $\overline{SE}$b enables Port B serial I/O buffers and allows a serial READ or WRITE operation to occur; otherwise, the output buffers are in a High-Z state. $\overline{SE}$b is also used during a TRANSFER operation to indicate whether a WRITE TRANSFER or a SERIAL-INPUT-MODE ENABLE (PSEUDO WRITE TRANSFER) cycle is performed.
35	DSF1	Input	Special Function (Control) 1: DSF1 is used to indicate which special functions are used on a particular access or transfer cycle. See the Functional Truth Table for a detailed description.
21	DSF2	Input	Special Function (Control) 2: DSF2 is used to indicate which special functions are used on a particular access or transfer cycle. See the Functional Truth Table for a detailed description.
20	$\overline{RAS}$	Input	Row Address Strobe: $\overline{RAS}$ is used to clock-in the 9 row-address bits and as a strobe for control and data inputs.
33	$\overline{CAS}$	Input	Column Address Strobe: $\overline{CAS}$ is used to clock-in the 8 column-address bits, enable the DRAM output buffers (along with $\overline{TR}/\overline{OE}$), and strobe control and data inputs.

PIN DESCRIPTIONS (continued)

PLCC PIN NUMBER(S)	SYMBOL	TYPE	DESCRIPTION
31, 30, 29, 28, 25, 24, 27, 22, 23	A0-A8	Input	Address Inputs: For DRAM operation, these inputs are multiplexed and clocked by $\overline{RAS}$ and $\overline{CAS}$ to select one 8-bit word out of the 128K available. During TRANSFER operations, A0 to A8 indicate the DRAM row being accessed (when $\overline{RAS}$ goes LOW) and A0-A7 indicate the SAM start address (when $\overline{CAS}$ goes LOW). A7, A8 = "don't care" for the start address when doing SPLIT TRANSFER.
19	STS	Input	SAM Transfer Select: The state of STS at $\overline{RAS}$ time determines which SAM is involved in a transfer (SAMa = LOW, SAMb = HIGH).
46	MKD	Input	Mask Data Input: MKD is used during BIT MASK REGISTER LOAD cycles to enable or disable the serial mask input mode (SMI). If SMI is enabled (MKD = HIGH at $\overline{RAS}$), then MKD is used as mask data input and is clocked by SCb into the mask data register.
6	TRM	Input	Transfer Mask Select: TRM is used to select between NORMAL TRANSFER cycles and BIT MASKED TRANSFER or BIT MASK REGISTER LOAD cycles.
13, 14, 15, 16, 37, 38, 39, 40	DQ1-DQ8	Input/ Output	DRAM Data I/O: Data inputs and outputs for the DRAM memory array; inputs for the MASK and COLOR REGISTER load cycles; address mask inputs for BLOCK WRITE cycles.
8, 9, 10, 11, 42, 43, 44, 45	SDQa1-SDQa8	Input/ Output	Serial Data I/O, SAMa: Input, Output, or High-Z.
2, 3, 4, 5, 48, 49, 50, 51	SDQb1-SDQb8	Input/ Output	Serial Data I/O, SAMb: Input, Output, or High-Z.
32	QSFa/SSFa	Output Input	Split SAM Status, SAMa (MT43C8128): QSFa indicates which half of SAMa is being accessed (Lower = LOW, Upper = HIGH). Split SAM Special Function, SAMa (MT43C8129): SSFa = HIGH stops access to current half of SAM and will load the Tap address of the next half into the address pointer. SSFa is synchronized with SCa.
34	QSFb/SSFb	Output Input	Split SAM Status, SAMb (MT43C8128): QSFb indicates which half of SAMb is being accessed (Lower = LOW, Upper = HIGH). Split SAM Special Function, SAMb (MT43C8129): SSFb = HIGH stops access to current half of SAM and will load the Tap address of the next half into the address pointer. SSFb is synchronized with SCb.
17, 26	Vcc	Supply	Power Supply: +5V ±5%
52, 36	Vss	Supply	Ground

FUNCTIONAL DESCRIPTION

The MT43C8128/9 may be divided into four functional blocks: the DRAM and its special functions, the bit mask register (BMR), the two serial access memories (SAMs), and the DRAM/SAM/BMR transfer circuitry. All the operations described below are also shown in the AC Timing Diagrams section of this data sheet and are summarized in the Functional Truth Table.

Note: *For dual function pins, the function that is not being discussed will be surrounded by parentheses. For example, when discussing transfer operations the $\overline{TR}/(\overline{OE})$ pin will be shown as $\overline{TR}/(\overline{OE})$.*

DRAM OPERATION

This section describes the operation of the random access port and the special functions associated with the DRAM.

DRAM REFRESH (ROR, CBR, and HR)

Like any DRAM-based memory, the MT43C8128/9 TPDRAM must be refreshed to retain data. All 512 row-address combinations must be accessed within 8ms. The MT43C8128/9 support $\overline{CAS}$-BEFORE-$\overline{RAS}$, $\overline{RAS}$-ONLY and HIDDEN types of refresh cycles.

For the $\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH cycle, the row addresses are generated and stored in an internal address counter. The user need not supply any address data and simply must perform 512 $\overline{CAS}$-BEFORE-$\overline{RAS}$ cycles within the 8ms time period.

For $\overline{RAS}$-ONLY REFRESH cycles, the refresh address must be generated externally and applied to the A0-A8 inputs. The DQ pins remain in a High-Z state for both the $\overline{RAS}$ ONLY and $\overline{CAS}$-BEFORE-$\overline{RAS}$ cycles.

HIDDEN REFRESH (HR) cycles are performed by toggling $\overline{RAS}$ (while keeping $\overline{CAS}$ LOW) after a READ or WRITE cycle. This performs $\overline{CAS}$-BEFORE-$\overline{RAS}$ cycles but does not disturb the DQ lines.

Any DRAM READ, WRITE, or TRANSFER cycle also refreshes the DRAM row that is being accessed. The SAM and BMR portions of the MT43C8128/9 are fully static and do not require any refreshing.

DRAM READ AND WRITE CYCLES (RW)

The DRAM portion of the TPDRAM is nearly identical to standard 1256K x 4 DRAMs. However, because several of the DRAM control pins are used for additional functions on this device, several conditions that were undefined or "don't care" states for the DRAM are specified for the TPDRAM. These conditions are highlighted in the following discussion. In addition, the TPDRAM has several special functions that may be used when writing to the DRAM.

The 17 address bits used to select an 8-bit word from the 131,072 available are latched into the chip using the A0-A8, $\overline{RAS}$, and $\overline{CAS}$ inputs. First, the 9 row-address bits are set up on the address inputs and clocked into the part when $\overline{RAS}$ transitions from HIGH-to-LOW. Next, the 8 column-address bits (A0-A7) are set up on the address inputs and clocked-in when $\overline{CAS}$ goes from HIGH-to-LOW.

Note: *$\overline{RAS}$ also acts as a "master" chip enable for the TPDRAM. If $\overline{RAS}$ is inactive, HIGH, all other DRAM control pins ($\overline{CAS}$, $\overline{TR}/\overline{OE}$, $\overline{ME}/\overline{WE}$, etc.) are a "don't care" and may change state without effect. No DRAM or TRANSFER cycles will be initiated without $\overline{RAS}$ falling.*

For single port DRAMs, the $\overline{OE}$ pin is a "don't care" when $\overline{RAS}$ goes LOW. For the TPDRAM, $\overline{TR}/(\overline{OE})$ is used when $\overline{RAS}$ goes LOW to select between DRAM and TRANSFER cycles. $\overline{TR}/(\overline{OE})$ must be HIGH at the $\overline{RAS}$ HIGH-to-LOW transition for all DRAM operations.

If $(\overline{ME})/\overline{WE}$ is HIGH when $\overline{CAS}$ goes LOW, a DRAM READ operation is performed and the data from the memory cells selected will appear at the DQ1-DQ8 port. The $(\overline{TR})/\overline{OE}$ input must transition from HIGH-to-LOW some time after $\overline{RAS}$ falls to enable the DRAM output port.

For single port DRAMs, $\overline{WE}$ is a "don't care" when $\overline{RAS}$ goes LOW. For the TPDRAM, $\overline{ME}/(\overline{WE})$ is used, when $\overline{RAS}$ goes LOW, to select between a MASKED WRITE cycle or a normal WRITE cycle. If $\overline{ME}/(\overline{WE})$ is LOW at the $\overline{RAS}$ HIGH-to-LOW transition, a MASKED WRITE operation is selected. For any TPDRAM non-masked access cycle (READ or WRITE), $\overline{ME}/(\overline{WE})$ must be HIGH at the $\overline{RAS}$ HIGH-to-LOW transition. If $(\overline{ME})/\overline{WE}$ is LOW when $\overline{CAS}$ goes LOW, a DRAM WRITE operation is performed and the data present on the DQ1-DQ8 data port will be written into the selected memory cells.

The TPDRAM can perform all the normal DRAM cycles: READ, EARLY-WRITE, LATE-WRITE, READ-MODIFY-WRITE, FAST-PAGE-MODE READ, FAST-PAGE-MODE WRITE, and FAST-PAGE-MODE READ-MODIFY-WRITE. Refer to the AC timing parameters and diagrams in the data sheet for more details on these operations.

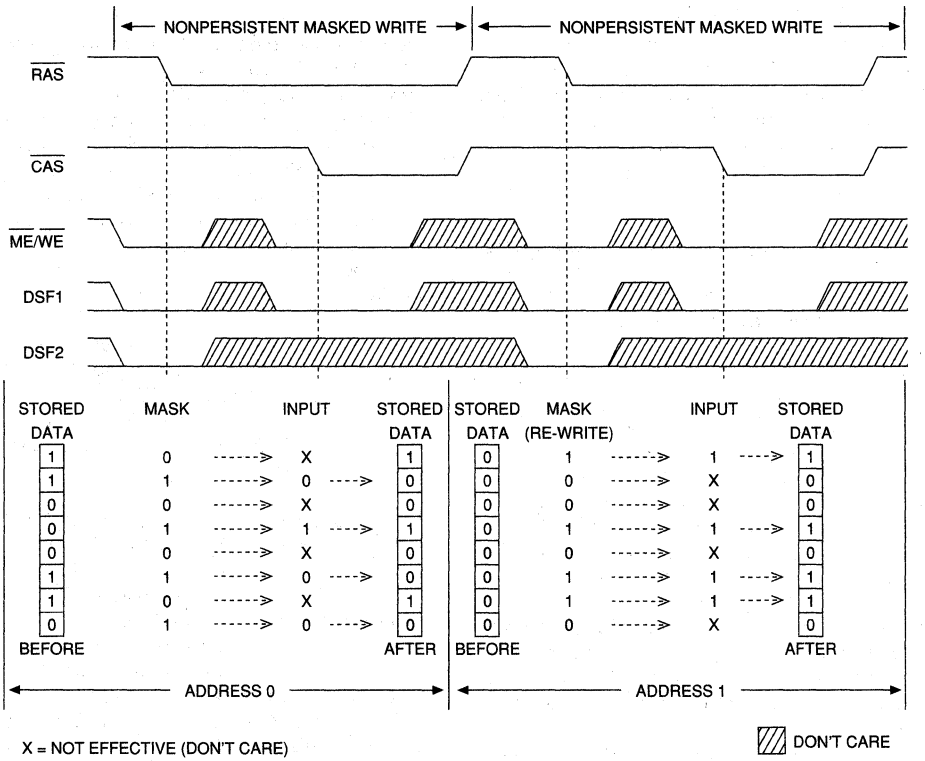


Figure 1
NONPERSISTENT MASKED WRITE EXAMPLE

NONPERSISTENT MASKED WRITE (RWNM)

The MASKED WRITE feature eliminates the need to do a READ-MODIFY-WRITE cycle when changing only certain bits within an 8-bit word. The MT43C8128/9 supports two types of MASKED WRITE cycles, NONPERSISTENT MASKED WRITE and PERSISTENT MASKED WRITE.

If $\overline{ME}$/($\overline{WE}$), DSF1 and DSF2 are LOW at the $\overline{RAS}$ HIGH-to-LOW transition, the data (mask data) present on the DQ1-DQ8 inputs will be written into the mask data register. The mask data acts as an individual write enable for each of the eight DQ1-DQ8 pins. If a LOW (logic 0) is written to a mask data register bit, the input port for that bit is disabled during the subsequent WRITE operation and no new data will be written to that DRAM cell location. A HIGH (logic 1) on a mask data register bit enables the input port and allows normal WRITE operations to proceed. This convention is used for all masks on the MT43C8128/9. Note that $\overline{CAS}$ is still HIGH. When $\overline{CAS}$ or ($\overline{ME}$)/$\overline{WE}$ go LOW, the bits present on the DQ1-DQ8 inputs will be either written to the DRAM (if the mask data bit was HIGH) or ignored (if the mask data bit was LOW). The DRAM contents that correspond to the masked bits will not be changed during the WRITE cycle. When using NONPERSISTENT MASKED WRITE, the data present on the DQ inputs is loaded into the mask data register at every falling edge of $\overline{RAS}$. FAST PAGE MODE may be used in tandem with NONPERSISTENT MASKED WRITE to write several column locations using the same mask during one $\overline{RAS}$ cycle. An example of NONPERSISTENT MASKED WRITE cycle is shown in Figure 2.

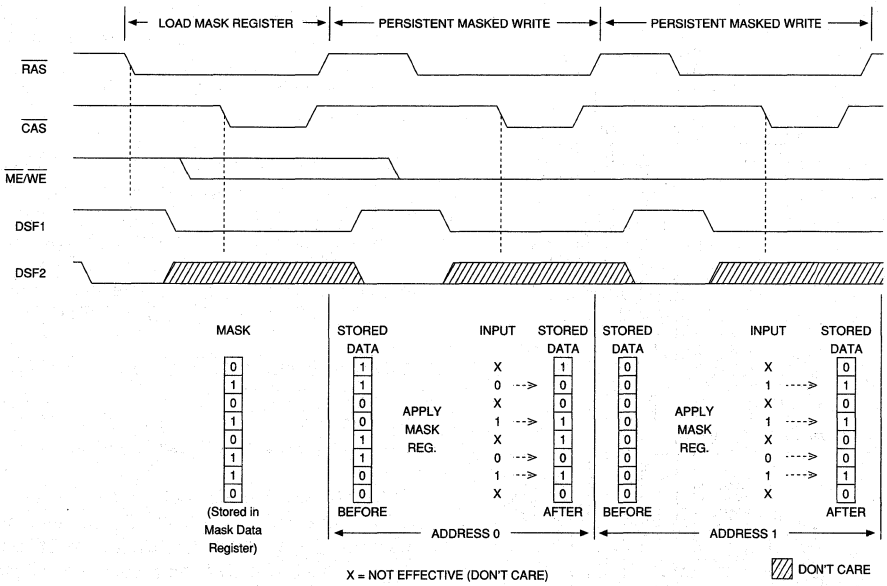


Figure 2
PERSISTENT MASKED WRITE EXAMPLE

PERSISTENT MASKED WRITE (RWOM)

The PERSISTENT MASKED WRITE feature eliminates the need to rewrite the mask data before each MASKED WRITE cycle if the same mask data is being used repeatedly. To initiate a PERSISTENT MASKED WRITE, a LOAD MASK REGISTER cycle is performed by taking $\overline{ME}/(\overline{WE})$ and DSF1 HIGH, and DSF2 LOW, when $\overline{RAS}$ goes LOW. The mask data is loaded into the internal register when $\overline{CAS}$ goes LOW, provided DSF1 is LOW (see the LOAD MASK REGISTER description).

PERSISTENT MASKED WRITE cycles may then be performed by taking $\overline{ME}/(\overline{WE})$ and DSF2 LOW and DSF1 HIGH when $\overline{RAS}$ goes LOW. The contents of the mask data register will then be used as the mask data for the DRAM inputs. Unlike the NONPERSISTENT MASKED WRITE cycle, the data present at the DQ inputs is not loaded into the mask register when $\overline{RAS}$ falls. Another PERSISTENT MASKED WRITE cycle may be performed without reloading the register. Figure 2 shows the LOAD MASK REGISTER and PERSISTENT MASKED WRITE cycle operations. The LOAD MASK REGISTER and PERSISTENT MASKED WRITE cycles allow systems that cannot output data at $\overline{RAS}$ time to perform MASKED WRITE cycles. PERSISTENT MASKED WRITE can also operate in FAST PAGE MODE.

BLOCK WRITE (BW)

If DSF1 is HIGH when $\overline{CAS}$ goes LOW, the MT43C8128/9 will perform a BLOCK WRITE cycle instead of a normal WRITE cycle. In BLOCK WRITE cycles, the contents of the color register (instead of the DQ inputs) are directly written to four adjacent column locations (see Figure 3). A total of 32 bits will be written simultaneously, improving the normal DRAM fill rate by four times. The color register must be loaded prior to beginning BLOCK WRITE cycles (see LOAD COLOR REGISTER).

The row is addressed as in a normal DRAM WRITE cycle. However, when $\overline{CAS}$ goes LOW, only the A2-A7 inputs are used. A2-A7 specify the "block" (out of the 64 possible) of four adjacent column locations that will be accessed. When the later of $\overline{ME}/\overline{WE}$ and $\overline{CAS}$ go LOW, the DQ inputs latched and used to determine which of the four column locations will be written. DQ1 acts as a write enable for column location A0 = 0, A1 = 0; DQ2 controls column location A0 = 1, A1 = 0; DQ3 controls A0 = 0, A1 = 1; and DQ4 controls A0 = 1, A1 = 1. The write enable controls are active HIGH; a logic 1 enables and a logic 0 disables the WRITE function.

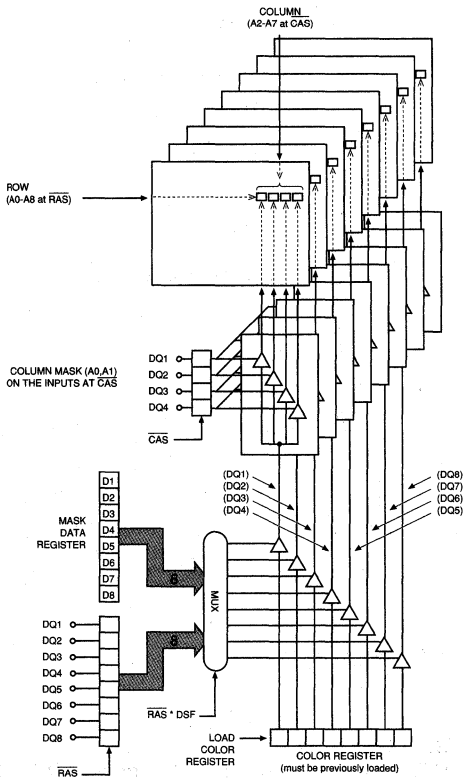


Figure 3
BLOCK WRITE EXAMPLE

The contents of the color register will then be written to the column locations enabled. Each DQ location of the color register is written to the four column locations (or any of the four that are enabled) in the corresponding DQ bit plane. The DQ mask is not used in this mode.

NONPERSISTENT MASKED BLOCK WRITE (BWNM)

The MASKED WRITE functions can also be used during BLOCK WRITE cycles. NONPERSISTENT MASKED BLOCK WRITE operates exactly like the normal NONPERSISTENT MASKED WRITE except the mask is now applied to four column locations instead of just one column location.

Like NONPERSISTENT MASKED WRITE, the combination of $\overline{ME}$/($\overline{WE}$) LOW and DSF1 LOW when $\overline{RAS}$ goes LOW, initiates a NONPERSISTENT MASK cycle. The DSF pin must be driven HIGH when $\overline{CAS}$ goes LOW to perform a NONPERSISTENT MASKED BLOCK WRITE. By using both the column mask input and the MASKED WRITE function, any combination of the four bit planes may be masked and any combination of the eight column locations may be masked.

PERSISTENT MASKED BLOCK WRITE (BWOM)

This cycle is also performed exactly like the normal PERSISTENT MASKED WRITE except that DSF1 is HIGH when $\overline{CAS}$ goes LOW to indicate the BLOCK WRITE function. Both the mask data register and the color register must be loaded with the appropriate data prior to starting a PERSISTENT MASKED BLOCK WRITE.

DRAM REGISTER OPERATIONS

The MT43C8128/9 contains two 8-bit registers that are used as data registers for special functions. This section describes how to load these registers.

LOAD MASK REGISTER (LMR)

The LOAD MASK REGISTER operation and timing are identical to a normal WRITE cycle except that DSF1 is HIGH when $\overline{RAS}$ goes LOW. As shown in the Truth Table, the combination of $\overline{TR}$/($\overline{OE}$), $\overline{ME}$/($\overline{WE}$), and DSF1 being HIGH when $\overline{RAS}$ goes LOW indicates the cycle is a REGISTER load cycle. DSF1 is used when $\overline{CAS}$ goes LOW to select the register to be loaded, and must be LOW for a LOAD MASK REGISTER cycle. The data present on the DQ lines will then be written to the mask data register.

Note: *For a normal DRAM WRITE cycle, the mask data register is disabled but not modified. The contents of mask data register will not be changed unless a NONPERSISTENT MASKED WRITE cycle or a LOAD MASK REGISTER cycle is performed*

The row address supplied will be refreshed, but it is not necessary to provide any particular row address. The column address inputs are ignored during a LOAD MASK REGISTER cycle.

The mask data register contents are used during PERSISTENT MASKED WRITE and PERSISTENT MASKED BLOCK WRITE cycles to selectively enable writes to the eight DQ planes.

LOAD COLOR REGISTER (LCR)

A LOAD COLOR REGISTER cycle is identical to the LOAD MASK REGISTER cycle except DSF1 is HIGH when $\overline{CAS}$ goes LOW. The contents of the color register are retained until changed by another LOAD COLOR REGISTER cycle (or the part loses power) and are used as data inputs during BLOCK WRITE cycles.

TRANSFER OPERATIONS

This section describes transfer operations between the DRAM and either SAM. The direction of the transfer is specified with respect to the DRAM portion of the device. A write is referenced to the DRAM array and a read is referenced from the array.

Note: *The three ports of the TPDRAM are independent and asynchronous to one another. Any or all of the ports may be accessed simultaneously at the maximum allowable frequencies. The only time the ports are synchronized is during transfers to or from the DRAM and SAM portions of the device. A transfer involving a SAM does not affect access from the other SAM port. Both SAMs may be accessed during a DRAM/BMR transfer operation or any other DRAM access cycle other than a SAM transfer.*

TRANSFER operations are initiated when $\overline{TR}/(\overline{OE})$ is LOW at the falling edge of $\overline{RAS}$. The state of STS when $\overline{RAS}$ goes LOW indicates which SAM the TRANSFER will address. The state of $(\overline{ME})/\overline{WE}$ when $\overline{RAS}$ goes LOW indicates the direction of the TRANSFER. At the same time, DSF1 is used to select between normal TRANSFER cycles and SPLIT TRANSFER cycles and DSF2 is used to select between normal TRANSFER cycles and MASKED TRANSFER cycles. A TRANSFER cycle can be performed without dropping $\overline{CAS}$. In this case, the previously loaded Tap address will be used.

The MT43C8128/9 include a feature called BIT MASKED TRANSFER, which uses a third 2,048-bit data register to individually mask every bit involved in a TRANSFER operation. The BIT MASKED TRANSFER may be applied to either READ or WRITE TRANSFERs. The TRM pin is used to select between NORMAL and BIT MASKED TRANSFER (or BIT MASK REGISTER LOAD) cycles. The type of transfer operation is always selected on the falling edge of $\overline{RAS}$.

NORMAL TRANSFERS

The MT43C8128/9 support all of the popular transfer cycles available on the 1 Meg video RAMs. Each of these is described in the following section.

READ TRANSFER (RT)

A READ TRANSFER cycle is selected if $(\overline{ME})/\overline{WE}$ is HIGH, and DSF1 and $\overline{TR}/(\overline{OE})$ are LOW when $\overline{RAS}$ goes LOW. When $\overline{RAS}$ goes LOW, the READ TRANSFER is to SAMa if STS = LOW, or to SAMb if STS = HIGH. The row address bits indicate the eight 256-bit DRAM rows that are to be transferred to the eight SAM data registers. The column address bits indicate the start address (or Tap point) of the next serial output cycle from the designated SAM data registers. QSF indicates the SAM half being accessed: LOW if the lower half; HIGH if the upper half. Performing a READ TRANSFER cycle sets the direction of the selected SAMs I/O buffers to the output mode.

To complete a REAL-TIME READ-TRANSFER, $\overline{TR}/(\overline{OE})$ is taken HIGH while $\overline{RAS}$ and $\overline{CAS}$ are LOW. In order to synchronize the REAL-TIME READ-TRANSFER to the serial clock, the rising edge of $\overline{TR}/(\overline{OE})$ must occur between the rising edges of successive clocks on the SC input (refer to the AC timing diagrams). A "regular" READ TRANSFER is not sychronized with the SC pin of the addressed SAM. This type of RT is performed when $\overline{TR}/(\overline{OE})$ is taken HIGH "early," without regard to the falling edge of $\overline{CAS}$. The transfer will be completed internally by the device. The first serial clock must meet the ^{t}RSD and ^{t}CSD delays (see READ TRANSFER AC timing diagram). The 2,048 bits of DRAM data are then written into the SAM data registers, and the selected SAM's Tap address that was stored in the internal, 8-bit Tap address register is loaded into the address counter. If $\overline{SE}$ for the SAM selected ($\overline{SE}$a for SAMa) is LOW, the first bits of the new row data will appear at the serial outputs with the next SC clock pulse. $\overline{SE}$ enables the serial outputs, and may be either HIGH or LOW during this operation.

SPLIT READ TRANSFER (SRT)

The SPLIT READ TRANSFER cycle eliminates the critical transfer timing required to maintain a continuous serial output data stream (the "full" READ TRANSFER cycle has to occur immediately after the final bit of "old data," and before the first bit of "new data" is clocked out of the SAM port).

When using the SPLIT TRANSFER mode, the SAM is divided into an upper half and a lower half. While data is being serially read from one half of the SAM, new DRAM data may be transferred to the other half. The transfer may occur at any time while the other half is sending data, and need not be synchronized with the SC clock.

The $\overline{TR}/(\overline{OE})$ timing is relaxed for SRT cycles. The rising edge of $\overline{TR}/(\overline{OE})$ is not used to complete the TRANSFER cycle, and therefore is independent of the rising edges of $\overline{RAS}$ and $\overline{CAS}$. The transfer timing is generated internally for SPLIT TRANSFER cycles.

SPLIT TRANSFERs do not change the SAM I/O direction. A normal (nonsplit) READ TRANSFER cycle must precede any sequence of SRT cycles to put the SAM I/O in the output mode and provide the initial SAM Tap address (which half). Then an SRT may be initiated by taking DSF1 HIGH and selecting the desired SAM (using STS) when $\overline{RAS}$ goes LOW during the TRANSFER cycle. As in nonsplit transfers, the row address is used to specify the DRAM row to be transferred. When an SRT cycle is initiated, the half of the SAM not actively being accessed will be the half that

receives the transfer. When $\overline{CAS}$ falls, address pins A0-A6 determine the Tap address for the SAM-half selected; A7 = "don't care." If $\overline{CAS}$ does not fall, the previously loaded Tap address will be reused and the TRANSFER will be to the idle half.

Figure 4 shows a typical SRT initiation sequence. The normal READ TRANSFER is first performed, followed by an SRT of the same row to the upper half of the SAM. The SRT to the upper half is optional, and need only be done if the Tap for the upper half is ≠ 0. For the MT43C8128, serial access continues and when the SAM address counter reaches 127 ("A7" = 1, A0-A6 = 0), the QSF output for that SAM goes HIGH and the Tap address for the upper half is automatically loaded. Since the serial access has now switched to the upper half of the SAM, new data may be transferred to the lower half. This sequence of waiting for the state of QSF to change and then transferring new data to the SAM half that is not being accessed may now be repeated. For example, the next step in Figure 4 would be to wait until QSF went LOW (indicating that row-1 data is shifting out the lower SAM) and then transferring the upper half of row 1 to the upper SAM. $\overline{CAS}$ is used to load the Tap address. If $\overline{CAS}$ does not fall, the last Tap address load for the addressed SAM will be reused.

The split SAM operation is slightly different for the MT43C8129. Instead of having a QSF, this device has a Split SAM Special Function (SSF) input. With this input the serial access may be switched at will from one half of the SAM to the other. In other words, the address count may be stopped on the current half and the Tap address of the next half may be loaded, without waiting for the maximum address count of the current half (127; lower, 255; upper). If no SSF pulse is applied, the Tap address of the next half will be automatically loaded when the maximum count of the current SAM-half is reached. QSF = 0 when the Lower SAM (bits 0–127) is being accessed. QSF = 1 when the Upper SAM (bits 128–255) is being accessed.

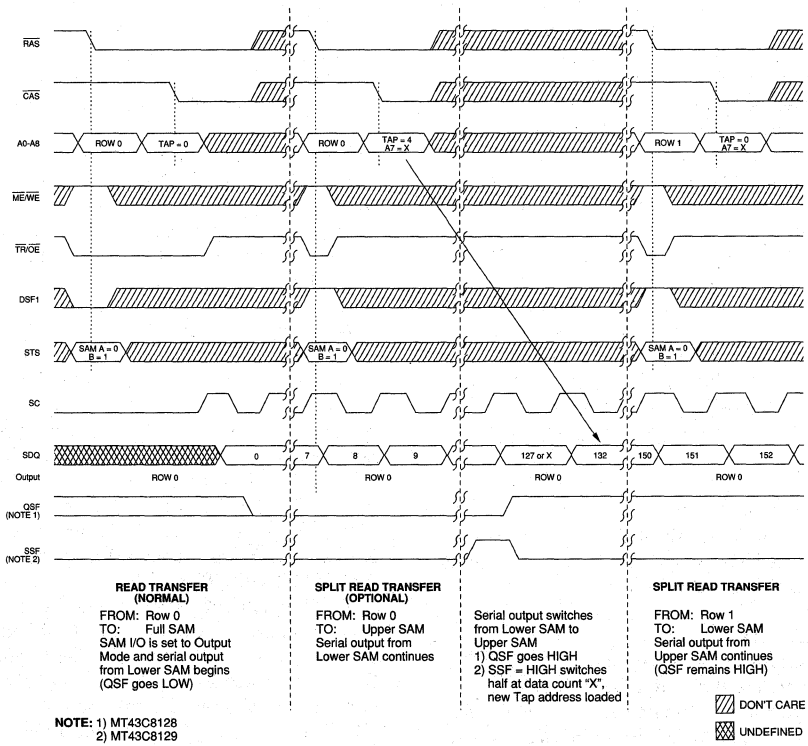


Figure 4
TYPICAL SPLIT-READ-TRANSFER INITIATION SEQUENCE

WRITE TRANSFER (WT)

The operation of the WRITE TRANSFER is identical to the READ TRANSFER described previously, except ($\overline{ME}$)/$\overline{WE}$ and $\overline{SE}$ must be LOW when $\overline{RAS}$ goes LOW. The DSF2 input is used to select between the WT and DQ MASKED WRITE TRANSFER cycles, and must be LOW for the WT cycle. The STS pin is also taken LOW or HIGH to select SAMa or SAMb, respectively, when $\overline{RAS}$ goes LOW. The row address indicates the DRAM row to which the SAM data register will be written, and the Tap address indicates the starting address of the next SERIAL INPUT cycle for the SAM data registers. QSF indicates the SAM half being accessed; LOW if the lower half, HIGH if the upper half. Performing a WT sets the direction of the SAM I/O buffers to the input mode.

PSEUDO WRITE TRANSFER (PWT)

The PSEUDO WRITE TRANSFER cycle may be used to change the direction of a SAM port from output to input without disturbing the DRAM data in the selected row. A PSEUDO WRITE TRANSFER cycle is a WRITE TRANSFER cycle with the $\overline{SE}$ of the appropriate SAM held HIGH instead of LOW. The addressed row will be refreshed. A DQ MASKED WRITE TRANSFER (with all bits masked) is an alternate method for changing the direction of the SAM port without disturbing the addressed row data.

DQ MASKED WRITE TRANSFER (MWT)

The data being transferred from either SAM to the DRAM may be masked by performing a DQ MASKED WRITE TRANSFER cycle. The transfer of data may be selectively enabled for each of the eight DQ planes (see Figure 5). The DMWT cycle is identical to the WRITE TRANSFER cycle except DSF2 is HIGH and mask data must be on the DQ inputs at the falling edge of $\overline{RAS}$.

The complete SAM register will be transferred to the selected row in each DQ plane if the mask data input is HIGH, and the SAM register will not be transferred if the mask data input for that DQ plane is LOW. DRAM data is not disturbed in masked DQ planes.

DQ MASKED SPLIT WRITE TRANSFER (MSWT)

The SPLIT WRITE TRANSFER feature makes it possible to input and transfer uninterrupted bit streams. Figure 6 shows a typical initiation sequence for SWT cycles.

Like the SRT, the DQ MASKED SPLIT WRITE TRANSFER cycle does not change the state of the SAM I/O buffers. A normal, DQ MASKED or PSEUDO WRITE TRANSFER cycle is required to set the Tap address and set the SAM I/O direction to input mode.

After the WT, a MSWT is performed to enter the split SAM operating mode. This sets the Tap for the next half of the SAM. The addressed half of the SAM is immediately transferred to the first destination row. This half of the SAM

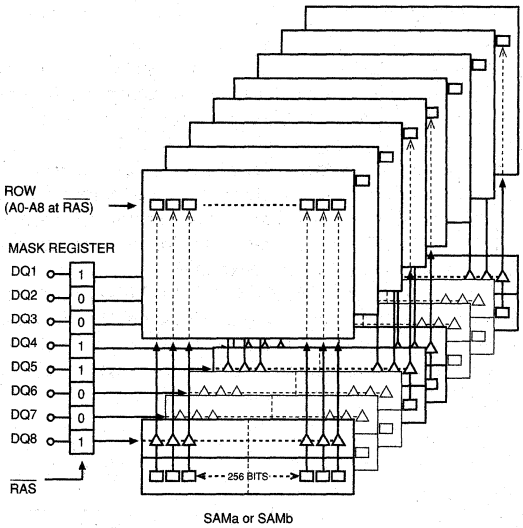


Figure 5
DQ MASKED WRITE TRANSFER

may not yet contain valid data. However, another MSWT to the same row will normally occur after this is loaded, so the initial invalid data will be overwritten. Another approach would be to initiate an MSWT addressed to any DRAM row, but mask (disable) all eight of the DQ planes. This method can be used to initiate the MSWT sequence without disturbing any DRAM data. The MSWT to the upper half is optional, and it is only needed if the Tap for the upper half is $\neq 0$.

Write mask data must be supplied to the DQ inputs during every SWT cycle at $\overline{RAS}$ time. The mask data acts as an individual write enable for each of the eight DRAM DQ planes. For example, DQ1, at $\overline{RAS}$ time, during a DQ1 MASKED WRITE, enables or disables the transfer of the SAM SDQ1 register to the DQ1 plane of the DRAM row selected (see the DQ MASKED WRITE TRANSFER description). As in all other MASKED WRITE operations, a HIGH enables the WRITE TRANSFER and a LOW disables the WRITE TRANSFER. As with SPLIT READ TRANSFER, the half of the SAM not receiving data will be the half transferred and the Tap address (A0-A6) for the other half is loaded when $\overline{CAS}$ falls (A7 is a "don't care"). If $\overline{CAS}$ does not fall, the previously loaded Tap address, A0-A6, will be reused. The TRANSFER will be to the idle half. When the serial clock crosses the half-SAM boundary, the new Tap address for that half is automatically loaded.

The QSFa and QSFb outputs (MT43C8128) indicate which half of SAMa or SAMb, respectively, is currently accepting

data. After QSF goes HIGH, indicating that serial input has now switched to the upper SAM, the contents of the lower half of the SAM may be transferred to any DRAM row. The cycle of checking for a change in QSF and then transferring the half of the SAM just filled may now be repeated. The next step on Figure 6 is to wait for QSF to go LOW and then SWT the contents of the upper half of the SAM to row 0. If the terminal count of the SAM half is reached before an SWT is performed for the next half, the access will be repeated from the same half and previously loaded Tap address (access will not move to the next half).

When operating the MT43C8129 in the MSWT mode, the address pointer may be changed to the new Tap address of the next half when the final desired input data is clocked-in. When the final data is input, the SSF input is taken HIGH at the corresponding rising edge of SC. The next SC rising edge will input data into the Tap location of the next half of the SAM. If SSF is not applied, the Tap address will be automatically loaded when the maximum Tap address count is reached for the current half (127 or 255). If SSF is HIGH at SC before an MSWT is performed for the next half, the access will jump to the old Tap address of the same half. Access will not preceed to the next half. If terminal count is reached before an MSWT, the access will proceed as it does for the MT43C8128.

SERIAL INPUT and SERIAL OUTPUT

The control inputs for SERIAL INPUT and SERIAL OUTPUT are SCa,b, $\overline{SE}$a,b and SSFa,b (MT43C8128). The rising edge of SC increments the serial address counter and provides access to the next SAM location. $\overline{SE}$ enables or disables the serial input/output buffers.

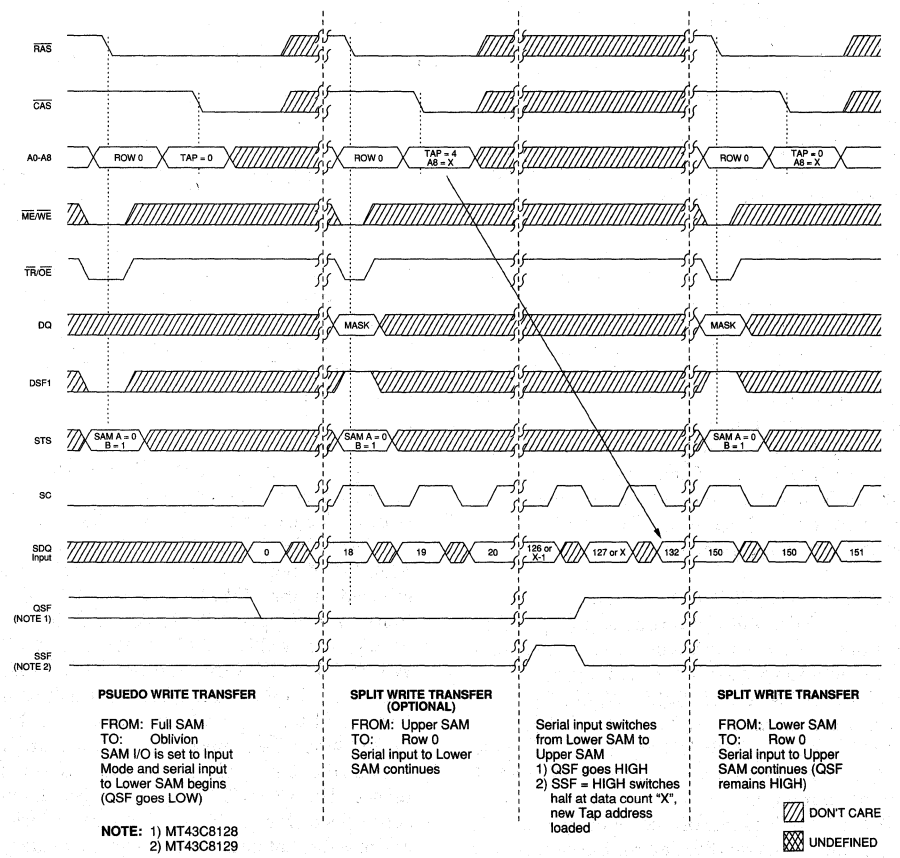


Figure 6
TYPICAL SPLIT-WRITE-TRANSFER INITIATION SEQUENCE

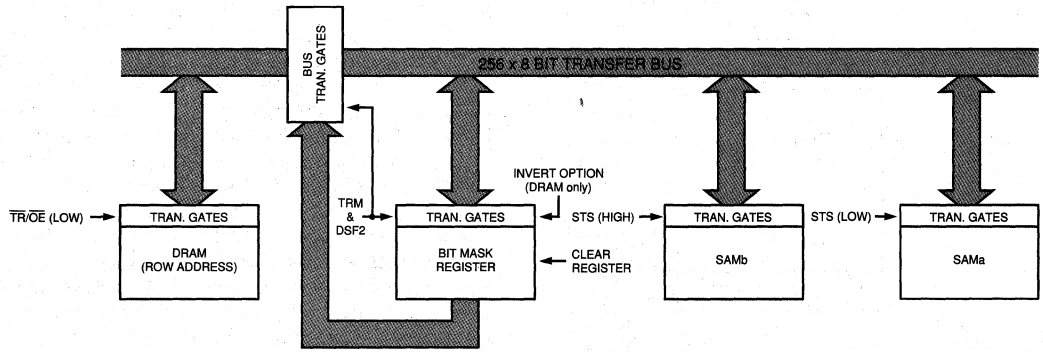


Figure 7
BIT MASKED TRANSFER BLOCK DIAGRAM

Serial output of the SAM contents will start at the serial TAP address that was loaded in the SAMa,b address counter during the DRAM-TO-SAM TRANSFER cycle. The SC nput increments the address counter and presents the contents of the next SAM location to the 8-bit port. $\overline{SE}$ is used as an output enable during the SAM output operation. The serial address is automatically incremented with every SC LOW-to-HIGH transition, regardless of whether $\overline{SE}$ is HIGH or LOW. For the MT43C8128, the address progresses hrough the SAM and will wrap around (after count 127 or 255) to the Tap address of the next half, for split modes. Address count will wrap around (after count 255) to Tap address 0 if in the "full" SAM modes. For the MT43C8129, he address count will wrap as it does for the MT43C8128 or t may be triggered, at will, to the next half by the SSF input split SAM modes). If SSF is HIGH at a LOW-to-HIGH ransition of SC, the Tap address of the next half will be oaded into the address pointer. The subsequent LOW-to-HIGH transition of SC will clock data from the Tap address f the new half.

SC is also used to clock-in data when the device is in the erial input mode. As in the serial output operation, the ontents of the serial address counter (loaded when the erial input mode was enabled) will determine the serial ddress of the first 8-bit word written. $\overline{SE}$ acts as a WRITE NABLE for serial input data and must be LOW for valid erial input. If $\overline{SE}$ = HIGH, the data inputs are disabled and ne SAM contents will not be modified. The serial address ounter is incremented with every LOW-to-HIGH transi-on of SC, regardless of the logic level on the $\overline{SE}$ input. The peration of SSF (MT43C8129) is the same as described for erial output.

BIT MASKED TRANSFERS

This section describes transfers between the DRAM and either of the two SAMs using the BIT MASKED TRANSFER capability. Before performing these BIT MASKED TRANSFERs, the bit mask register must first be loaded with the mask data. See the next section, BIT MASK REGISTER OPERATIONs, for instructions on how to load the bit mask register (BMR).

The BMR is a 2,048-bit register that individually controls each of the 2,048 transfer gates on the internal 256 x 8 transfer bus (see Figure 7). These bus transfer gates reside between the DRAM array and the three data registers and are set to the "pass-thru" mode for nonmasked transfers. For BIT MASKED TRANSFERs, the data in the BMR is coupled to the control inputs of the bus transfer gates. A logic "1" in the BMR will select the pass-thru (unmasked) mode for the corresponding SAM data bit, while a logic "0" will select the masked mode for that bit.

BIT MASKED TRANSFERs may be incorporated when doing READ, WRITE, SPLIT READ and SPLIT WRITE TRANSFERs. The timing and control required for any particular BIT MASKED TRANSFER cycle is identical to the corresponding normal TRANSFER cycle, except that TRM and DSF2 are HIGH instead of LOW. BIT MASKED TRANSFERs between the DRAM and either of the two SAM registers are possible. Figure 8 illustrates the BIT MASKED TRANSFER functions.

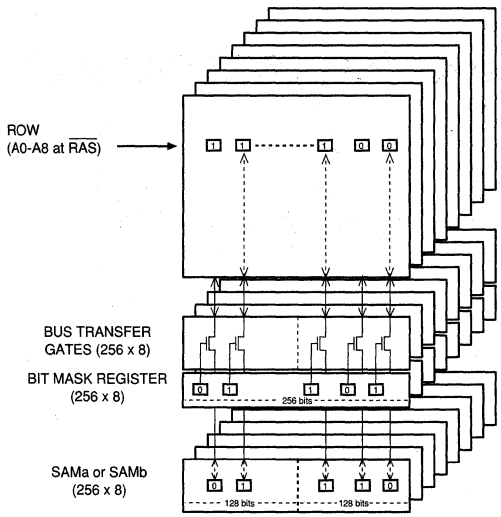


Figure 8
BIT MASK TRANSFER BLOCK DIAGRAM

BIT MASKED READ TRANSFER (BMRT)

BIT MASKED READ TRANSFER may be used to transfer any combination of the 2,048 bits contained in any DRAM row address to either of the two SAMs. The logic conditions and timing for the BMRT function are identical to the normal READ TRANSFER function except that TRM and DSF2 are HIGH select the BIT MASKED feature. If a bit in the BMR is a logic "1", the bus connection between the corresponding DRAM bit and the selected SAM bit is enabled and the data at the destination (one of the SAMs for BMRT) will be changed to the source data (the DRAM row for BMRT).

BIT MASKED SPLIT READ TRANSFER (BMSRT)

The BIT MASKED SPLIT READ TRANSFER operation is identical to the normal SPLIT READ TRANSFER except that the bit mask (stored in the bit mask register) is applied to the transfer data by taking TRM and DSF2 HIGH when $\overline{RAS}$ falls. The remaining control timing is identical to the requirements for a normal SPLIT READ TRANSFER.

BIT MASKED WRITE TRANSFER (BMWT)

Like WRITE TRANSFER, the BIT MASKED WRITE TRANSFER function may be used to transfer data to any DRAM row address from either of the two SAM registers. In this case, the SAM data will be masked by the contents of the bit mask register before the data is written to the DRAM.

BIT MASKED SPLIT WRITE TRANSFER (BMSWT)

Like the other BIT MASKED TRANSFER cycles, the BMSWT is nearly identical to the SPLIT WRITE TRANSFER, except TRM and DSF2 are HIGH when $\overline{RAS}$ falls. Two masks are applied during a BMSWT operation. Each of the individual bits are masked by the bit mask register and each of the DQ planes are masked by the DQ inputs at $\overline{RAS}$ time. If a DQ input is LOW at $\overline{RAS}$ time, none of the 128 SAM bits for that DQ plane will be transferred to the DRAM row-half selected. If a DQ input is HIGH, the 128 SAM bits for that row-half will be masked by the corresponding 128 mask register bits when written to the selected DRAM row-half. The remaining control timing is identical to the requirements for a normal SPLIT WRITE TRANSFER.

BIT MASK REGISTER OPERATIONS

This section describes how to transfer data to or from the Bit Mask Register (BMR) and how to clear the BMR's contents. Data may also be inverted when being transferred between the BMR and DRAM.

BMR READ TRANSFER (BMR-RT)

Any DRAM row may be transferred to the bit mask register by using the BMR READ TRANSFER function. When $\overline{RAS}$ falls, $\overline{TR}/(\overline{OE})$ is LOW to select a transfer cycle. TRM is HIGH to indicate that the BMR is involved in the TRANSFER cycle, and DSF2 is LOW to indicate that the data is to be transferred to the BMR (as opposed to using the contents of the BMR as bit mask data). The remainder of the timing and control required is identical to a normal READ TRANSFER cycle. No Tap address is loaded in this TRANSFER.

Note that the SAM transfer select (STS) pin is used to select whether non-inverted (STS = LOW) or inverted (STS = HIGH) data is transferred to the bit mask register. For all transfers to or from the bit mask register, the state of the MKD pin when $\overline{RAS}$ falls selects whether the Serial Mask Input (SMI) feature is enabled (see the Functional Truth Table). SMI is a special serial input mode that allows mask information to be clocked into the BMR at the same address location as the data clocked into SAMb (see the SMI mode description). MKD is LOW when $\overline{RAS}$ falls to disable SMI or HIGH to enable SMI. After the transfer is completed, the MKD pin then acts either as a mask data input to the BMR (SMI enabled) or is "don't care" (SMI disabled). The MKD input is tied to the 8 bit-planes, the data on the MKD pin is written to each bit-plane simultaneously.

BMR INVERTED READ TRANSFER (BMR-IRT)

If the STS pin is HIGH at $\overline{RAS}$ time the DRAM data will be inverted before being written to the BMR. All 2,048 bits involved in the transfer will be complemented. The functionality and logic levels for the other control inputs are

identical to the BMR READ TRANSFER cycle. Note that MKD is still used to enable or disable the SMI mode. There is no added cycle time delay for either the BMR INVERTED READ or BMR INVERTED WRITE TRANSFER cycles.

BMR WRITE TRANSFER (BMR-WT)

The contents of the BMR may also be transferred to any DRAM row by using the BMR WRITE TRANSFER cycle. $\overline{(ME)}/\overline{WE}$ and DSF2 are LOW and TRM is HIGH when $\overline{RAS}$ falls, to select a write transfer from the BMR. The DQ inputs are used to input a DQ bit-plane mask when $\overline{RAS}$ falls. This allows each of the four DQ planes to be write enabled or disabled during the BMR-WT. The MKD input is used to enable or disable the SMI mode. STS must be LOW at $\overline{RAS}$ time to transfer non-inverted BMR data to the DRAM row selected.

BMR INVERTED WRITE TRANSFER (BMR-IWT)

As with the BMR INVERTED READ TRANSFER, the 2,048 bits involved in the transfer may be inverted while being transferred. Taking STS HIGH at $\overline{RAS}$ time will cause the BMR data to be inverted before it is stored in the selected DRAM row. The other control and DQ (mask) inputs are the same as the BMR-WT.

SAM-TO-BMR TRANSFER (SAM-BMR)

The contents of either SAM may be transferred to the BMR in the same manner that a DRAM row is transferred. In this case, DSF1 is HIGH to indicate that the SAM is the source of the data instead of the DRAM. $\overline{(ME)}/\overline{WE}$ is used to indicate the direction of the transfer and must be LOW, when $\overline{RAS}$ falls, for a SAM-TO-BMR TRANSFER. STS is no longer used to select between normal and inverted data, it now indicates which SAM is involved in the transfer. Since a SAM-TO-BMR TRANSFER "reads" data from the SAM, the SAM will be placed into input mode by this transfer cycle. The MKD input is still used to determine if the SMI mode will be enabled after the transfer is completed. Since no DRAM access is involved, it is not necessary to provide any particular ROW address at $\overline{RAS}$ time. However, whichever ROW address is present at $\overline{RAS}$ time will be used as the address for a $\overline{RAS}$-ONLY REFRESH. Since a SAM is involved in the transfer, a new SAM starting address (or Tap) will be loaded at $\overline{CAS}$ time. This address will be loaded into the serial address counter of the SAM selected by STS at $\overline{RAS}$ time.

Note: *Any SAM/BMR TRANSFER will take the SAM involved in the transfer out of the split SAM mode, if it was in that mode before the transfer.*

BMR-TO-SAM TRANSFER (BMR-SAM)

The contents of the BMR may also be transferred to one of the SAM registers. The $\overline{(ME)}/\overline{WE}$ input is used to indicate the direction of the transfer and must be HIGH for a BMR-TO-SAM TRANSFER. STS is LOW to select SAMa or HIGH to select SAMb as the destination for the BMR data. The remaining inputs and functionality are identical to the SAM-TO-BMR TRANSFER. Since a BMR-TO-SAM TRANSFER writes new data to the selected SAM register, the I/O for the SAM involved will be placed in the output mode and a new Tap address will be loaded when $\overline{CAS}$ falls.

CLEAR BIT MASK REGISTER (CLR-BMR)

The entire contents of the BMR can be cleared (set all bit LOW) within a single transfer cycle by performing a CLEAR BMR cycle. Unlike the other cycles that access the BMR, TRM is LOW at $\overline{RAS}$ time for the CLEAR BIT MASK REGISTER function. $\overline{TR}/\overline{(OE)}$ is LOW to indicate that the cycle is a transfer cycle (although there is really no data transfer involved). The CLR-BMR function is selected when $\overline{ME}/\overline{(WE)}$, DSF1 and DSF2 are HIGH when RAS falls.

When the BMR is cleared, all data will be masked when a BIT MASKED TRANSFER cycle is performed.

The BMR INVERTED WRITE and BMR WRITE TRANSFERS may be used with the CLR-BMR function to set or clear, respectively, any DRAM row. The CLR-BMR function is used to clear the BMR then the BMR TRANSFERS are performed to the addressed DRAM row.

The CLEAR BIT MASK REGISTER function is useful when using the SERIAL MASK INPUT mode. It is automatically performed (when in the SMI mode) when data is transferred from SAMb to the DRAM (see SERIAL MASK INPUT section).

SERIAL MASK INPUT (SMI)

Whenever the BMR is accessed, the MKD input is sensed and latched into the BMR control logic. If the MKD pin is LOW at $\overline{RAS}$ time the Serial Mask Input (SMI) mode is disabled and the BMR may only be loaded via internal transfer cycles. If MKD is HIGH when $\overline{RAS}$ falls, during a BMR access, then the BMR control logic enables the SMI mode and the BMR may be serially loaded via the MKD input.

When SMI is enabled, the MKD input is coupled to all eight of the bit mask register's DQ planes (see Figure 9). The SCb clock input and SAMb's address counter are used to input data to SAMb and the BMR. SEb will enable (LOW) or disable (HIGH) input data to SAMb and the BMR, the address count will increment regardless of the state of SEb.

The most common application of the SMI mode is to automatically load a transfer mask with the new data written to SAMb. To initialize the sequence, the BMR is cleared (CLR-BMR) with MKD = HIGH at $\overline{RAS}$ time to

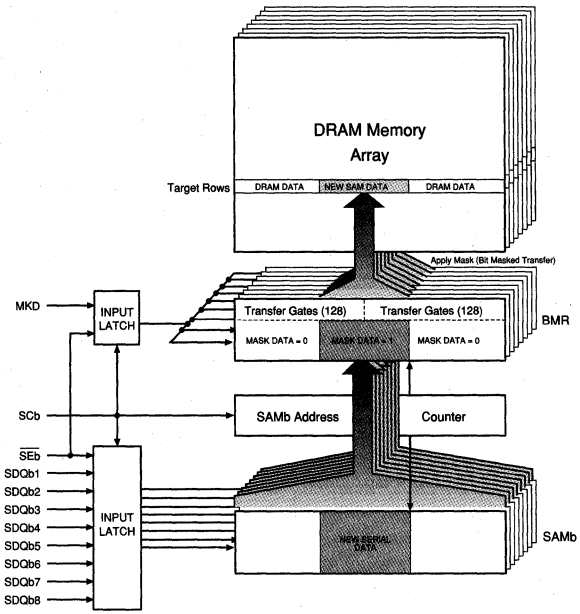


Figure 9
SERIAL-MASK-INPUT MODE BLOCK DIAGRAM

enable the SMI mode. Then SAMb is prepared to accept input data by performing PSEUDO WRITE TRANSFER. The SAM starting address loaded will also apply to the BMR. For every address location that to which data is written in SAMb, the corresponding address location in the BMR will be written to the value present on MKD (all eight planes of the BMR will be written). After the input of data to SAMb is complete, a BIT MASKED WRITE TRANSFER may be performed and only the unmasked data from SAMb will be transferred to the DRAM. The BMR will be cleared automatically after a BIT MASKED WRITE TRANSFER from SAMb, if the device is in the SMI mode. A BMSWT from SAMb will clear on half of the BMR. This allows a new mask to be loaded during the next fill of SAMb, without performing a CLR-BMR cycle. If data is to be masked during the BMWT, then MKD is held LOW when the corresponding SAMb data is written. If the data is to be written (unmasked) to the DRAM during the BMWT, then MKD is held HIGH when the corresponding SAMb location is written. The function of the MKD pin is dependent on the I/O direction of SAMb. MKD is an input only, if SMI is enabled and SAMb is in input mode. If SMI is enabled and SAMb is in output mode, the MKD input is a "don't care," and no new data may be written to the BMR via MKD. MKD is also "don't care" if the SMI mode is disabled. Note that the mask data loaded via SAMb may also be applied to a SAMa TRANSFER cycle, if the mask has not been cleared by a SAMb TRANSFER or a CLR-BMR cycle. The BMR will not be cleared after a TRANSFER involving SAMa.

POWER UP INITIALIZATION

When Vcc is initially supplied or when refresh is interrupted for more than 8ms the device must be initialized.

After Vcc is at specified operating conditions, for 100µs (minimum), eight $\overline{RAS}$ cycles must be executed to initalize the dynamic memory array. When the device is initialized the DRAM I/O pins (DQs) are in a High-Z state, regardless of the state of ($\overline{TR}$)/$\overline{OE}$. The DRAM array will contain random data.

The SAM portion of the device is completely static and does not require an initialization cycle. Both SAM ports will power up in the serial input mode (WRITE TRANSFERs) and the SAM I/O pins (SDQ's) are in a High-Z state, regardless of the state of $\overline{SE}$ ab. Also, SPLIT TRANSFER and SMI modes are disabled. Both QSF (MT43C8128) outputs may be in the High or LOW state. Both SAMs as well as bit mask, color, and DRAM mask registers all contain random data after power-up.

TRUTH TABLE[1]

CODE	FUNCTION	RAS FALLING EDGE									CAS FALL	A0-A8[2]		DQ1-DQ8[3]		REGISTERS	
		CAS	TR/OE	ME/WE[10]	DSF1	DSF2	SEa,SEb	TRM	MKD	STS	DSF1	RAS	CAS,A8=X	RAS	CAS,WE[4]	MASK	COLOR
	DRAM OPERATIONS																
CBR	CAS-BEFORE-RAS REFRESH	0	X	1[11]	X	X	X	X	X	X	X	X	X	X	X	—	—
ROR	RAS-ONLY REFRESH	1	1	X	X	X	X	X	X	X	—	ROW	—	X	—	—	—
RW	NORMAL DRAM READ OR WRITE	1	1	1	0	0[11]	X	X	X	X	0	ROW	COLUMN	X	VALID DATA	—	—
RWNM	NONPERSISTENT (LOAD AND USE) MASKED WRITE TO DRAM	1	1	0	0	0[11]	X	X	X	X	0	ROW	COLUMN	WRITE MASK	VALID DATA	LOAD & USE	—
RWOM	PERSISTENT (USE REGISTER) MASKED WRITE TO DRAM	1	1	0	1	0[11]	X	X	X	X	0	ROW	COLUMN	X	VALID DATA	USE	—
BW	BLOCK WRITE TO DRAM (NO DATA MASK)	1	1	1	0	0[11]	X	X	X	X	1	ROW	COLUMN (A2-A7)	X	COLUMN MASK	—	USE
BWNM	NONPERSISTENT (LOAD & USE) MASKED BLOCK WRITE TO DRAM	1	1	0	0	0[11]	X	X	X	X	1	ROW	COLUMN (A2-A7)	WRITE MASK	COLUMN MASK	LOAD & USE	USE
BWOM	PERSISTENT (USE MASK REGISTER) MASKED BLOCK WRITE TO DRAM	1	1	0	1	0[11]	X	X	X	X	1	ROW	COLUMN (A2-A7)	X	COLUMN MASK	USE	USE
	REGISTER OPERATIONS																
LMR	LOAD MASK REGISTER	1	1	1	1	0[11]	X	X	X	X	0	X[5]	X	X	WRITE MASK	LOAD	—
LCR	LOAD COLOR REGISTER	1	1	1	1	0[11]	X	X	X	X	1	X[5]	X	X	COLOR DATA	—	LOAD
	TRANSFER OPERATIONS																
RT	READ TRANSFER (DRAM-TO-SAM TRANSFER)	1	0	1	0	0	X	0	X	0=SAMa 1=SAMb	X	ROW	TAP[6]	X	X	—	—
SRT[9]	SPLIT READ TRANSFER (SPLIT DRAM-TO-SAM TRANSFER)	1	0	1	1	0	X	0	X	0=SAMa 1=SAMb	X	ROW	TAP[6]	X	X	—	—
WT	WRITE TRANSFER (SAM-TO-DRAM TRANSFER)	1	0	0	0	0	0	0	X	0=SAMa 1=SAMb	X	ROW	TAP[6]	X	X	—	—
PWT	PSEUDO WRITE TRANSFER (SERIAL INPUT MODE ENABLE)	1	0	0	0	0	1	0	X	0=SAMa 1=SAMb	X	X[5]	TAP[6]	X	X	—	—
MSWT[9]	SPLIT WRITE TRANSFER (SPLIT SAM-TO-DRAM TRANSFER DQ WITH MASK)	1	0	0	1	0	X	0	X	0=SAMa 1=SAMb	X	ROW	TAP[6]	DQ MASK	X	—	—
MWT	DQ MASKED WRITE TRANSFER	1	0	0	0	1	X	0	X	0=SAMa 1=SAMb	X	ROW	TAP[6]	DQ MASK	X	—	—

TRUTH TABLE [1]

CODE	FUNCTION	RAS FALLING EDGE									CAS FALL	A0-A8[2]		DQ1-DQ8[3]		REGISTERS	
		CAS	TR/OE	ME/WE[10]	DSF1	DSF2	SEa,SEb	TRM	MKD	STS	DSF1	RAS	CAS,A8=X	RAS	CAS,WE[4]	MASK	COLOR
	BIT MASK REGISTER OPERATIONS																
BMR-RT	BMR READ TRANSFER (DRAM→BMR TRANSFER)	1	0	1	0	0	X	1	0/1[7]	0	X	ROW	X	X	X	—	—
BMR-IRT	BMR READ TRANSFER (DRAM→INVERT→BMR TRANSFER)	1	0	1	0	0	X	1	0/1[7]	1	X	ROW	X	X	X	—	—
BMR-WT	BMR WRITE TRANSFER (BMR→DRAM TRANSFER)	1	0	0	0	0	X	1	0/1[7]	0	X	ROW	X	DQ MASK	X	—	—
BMR-IWT	BMR WRITE TRANSFER (BMR→INVERT→DRAM TRANSFER)	1	0	0	0	0	X	1	0/1[7]	1	X	ROW	X	DQ MASK	X	—	—
SAM-BMR	SAM→BMR TRANSFER	1	0	0	1	0	X	1	0/1[7]	0=SAMa 1=SAMb	X	X[5]	TAP[6]	X	X	—	—
BMR-SAM	BMR→SAM TRANSFER	1	0	1	1	0	X	1	0/1[7]	0=SAMa 1=SAMb	X	X[5]	TAP[6]	X	X	—	—
CLR-BMR	CLEAR BIT MASK REGISTER (SETS BMR TO ALL "0's")	1	0	1	1	1	X	0	0/1[7]	X	X	X[5]	X	X	X	—	—
	BIT MASKED TRANSFER OPERATIONS																
BMRT	BIT MASKED READ TRANSFER (BM DRAM→SAM TRANSFER)	1	0	1	0	1	X	1	X	0=SAMa 1=SAMb	X	ROW	TAP[6]	X	X	—	—
BMSRT[9]	BIT MASKED SPLIT READ TRANSFER (BM SPLIT DRAM→SAM TRANSFER)	1	0	1	1	1	X	1	X	0=SAMa 1=SAMb	X	ROW	TAP[6]	X	X	—	—
BMWT	BIT MASKED WRITE TRANSFER (BM SAM→DRAM TRANSFER)	1	0	0	0	1	X	1	X[8]	0=SAMa 1=SAMb	X	ROW	TAP[6]	X	X	—	—
BMSWT[9]	BIT MASKED SPLIT WRITE TRANSFER (BM SPLIT SAM→DRAM TRANSFER)	1	0	0	1	1	X	1	X[8]	0=SAMa 1=SAMb	X	ROW	TAP[6]	DQ MASK	X	—	—

NOTE:
1. 0 = LOW (V_{IL}), 1 = HIGH (V_{IH}), X = "don't care," – = "not applicable."
2. These columns show what must be present on the A0-A8 inputs when $\overline{RAS}$ falls and A0-A7 when $\overline{CAS}$ falls.
3. These columns show what must be present on the DQ1-DQ8 inputs when $\overline{RAS}$ falls and when $\overline{CAS}$ falls.
4. With WRITE cycles, the input data is latched at the falling edge of $\overline{CAS}$ or $\overline{ME/WE}$, whichever is later. Similarly, with READ cycles, the output data is enabled on the falling edge of $\overline{CAS}$ or $\overline{TR/OE}$, whichever is later.
5. The row that is addressed will be refreshed, but no particular ROW address is required.
6. Tap Address; this is the SAM location that the first SC cycle will access. For SPLIT TRANSFERs, the half receiving the transfer is determined by the MSB of the internal address counter. The SAM half not currently being accessed will be the half receiving the transfer.
   Column address A7 is a "don't care" for SPLIT TRANSFERs.
7. The Serial Mask Input mode (SMI) is enabled ("1") or disabled ("0") when the BMR is accessed (see BMR OPERATIONS). If SMI is enabled (MKD = "1"), mask data is serially clocked into the BMR with SCb and the BMR is automatically cleared after a BIT MASKED WRITE or BIT MASKED SPLIT WRITE TRANSFER cycle from SAMb. For BIT MASKED READ TRANSFERs to any SAM and BIT MASKED WRITE TRANSFERs from SAMa, the BMR is not cleared automatically.
8. If the SMI mode is enabled, mask data is clocked into the BMR with SCb.
9. SPLIT TRANSFERs do not change SAM I/O direction.
10. SAM I/O direction is a function of the state of $\overline{ME/WE}$ at $\overline{RAS}$ time. If $\overline{ME/WE}$ is LOW, then the selected SAM is an input; if $\overline{ME/WE}$ is HIGH, then the SAM is an output (except for SPLIT TRANSFERs).
11. The MT43C8128/9 operates properly if this state is "X", but to allow for future functional enhancements it is recommended that they are driven as shown in the Truth Table.

ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc Supply Relative to Vss ..... -1V to +7V
Operating Temperature, T_A (Ambient) ..... 0°C to +70°C
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation 1.5W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.75	5.25	V	1
Input High (Logic 1) Voltage, All Inputs	V_{IH}	2.4	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, All Inputs	V_{IL}	-1.0	0.8	V	1

DC ELECTRICAL CHARACTERISTICS

(0°C ≤ T_A ≤ 70°C; V_{CC} = 5V ±5%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
INPUT LEAKAGE CURRENT Any input (0V ≤ V_{IN} ≤ V_{CC}); all other pins not under test = 0V	I_L	-10	10	µA	
OUTPUT LEAKAGE CURRENT (Dout is disabled, 0V ≤ V_{OUT} ≤ V_{CC}).	I_{OZ}	-10	10	µA	
OUTPUT LEVELS Output High Voltage (I_{OUT} = -2.5mA)	V_{OH}	2.4		V	1
Output Low Voltage (I_{OUT} = 2.5mA)	V_{OL}		0.4	V	

CAPACITANCE

(T_A = 25°C)

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A8, TRM, MKD	C_{I1}		5	pF	2
Input Capacitance: $\overline{RAS}$, $\overline{CAS}$, $\overline{ME}$/$\overline{WE}$, $\overline{TR}$/$\overline{OE}$, SCa,b, $\overline{SE}$a,b, DSF1,2, STS SSFa,b	C_{I2}		7	pF	2
Input/Output Capacitance: DQ, SDQa,b	$C_{I/O}$		9	pF	2
Output Capacitance: QSFa,b	C_O		9	pF	2

DRAM CURRENT DRAIN; SAMa, SAMb and SERIAL MASK INPUT (SMI) INACTIVE

($0°C \le T_A \le 70°C$; V_{CC} = 5V ±5%)

PARAMETER/CONDITION	SYMBOL	MAX -8	MAX -10	UNITS	NOTES
OPERATING CURRENT ($\overline{RAS}$ and $\overline{CAS}$ = Cycling; ^tRC = ^tRC (MIN))	I_{CC1}	105	95	mA	3, 4 25
OPERATING CURRENT: PAGE MODE ($\overline{RAS}$ = V_{IL} $\overline{CAS}$ = Cycling; ^tPC = ^tPC (MIN))	I_{CC2}	100	90	mA	3, 4 27
STANDBY CURRENT: TTL INPUT LEVELS Power supply standby current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH}, after 8 $\overline{RAS}$ cycles (MIN))	I_{CC3}	10	10	mA	
STANDBY CURRENT: CMOS INPUT LEVELS Power supply standby current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC}-0.2V, after 8 $\overline{RAS}$ cycles min). All other inputs ≥ V_{CC} -0.2V or ≤ V_{SS} +0.2V	I_{CC4}	2	2	mA	
REFRESH CURRENT: $\overline{RAS}$-ONLY ($\overline{RAS}$ = Cycling; $\overline{CAS}$ = V_{IH})	I_{CC5}	110	100	mA	3, 26
REFRESH CURRENT: $\overline{CAS}$-BEFORE-$\overline{RAS}$ ($\overline{RAS}$ and $\overline{CAS}$ = Cycling)	I_{CC6}	110	100	mA	3, 5 26
TRANSFER CURRENT: SAM/DRAM DATA TRANSFER	I_{CC7}	105	95	mA	3

SERIAL PORT CURRENT DRAIN; SAMa, SAMb and/or SMI MODE

(Notes 3, 4) ($0°C \le T_A \le 70°C$; V_{CC} = 5V ±5%)

PARAMETER/CONDITION	SYMBOL	MAX -8	MAX -10	UNITS	NOTES
OPERATING CURRENT: SERIAL PORT (SAMa/SAMb) (SCa/SCb = Cycling; ^tSC = ^tSC (MIN); $\overline{SE}a/\overline{SE}b$ = V_{IL})	I_{CC8}	45	40	mA	
OPERATING CURRENT: SMI MODE (SAMb) (SCb = Cycling; ^tSC = ^tSC (MIN); $\overline{SE}b$ = V_{IL})	I_{CC9}	20	20	mA	
STANDBY CURRENT: SERIAL PORT (SAMa/SAMb) Power supply standby current (SCa/SCb = V_{IH} or V_{IL}; $\overline{SE}a/\overline{SE}b$ = V_{IH})	I_{CC10}	0	0	mA	
STANDBY CURRENT: SMI MODE (SAMb) Power supply standby current (SCb = V_{IH} or V_{IL}; $\overline{SE}b$ = V_{IH})	I_{CC11}	0	0	mA	

TOTAL CURRENT DRAIN

(Notes 3, 4) ($0°C \le T_A \le 70°C$; V_{CC} = 5V ±5%)

$I_{CC(TOTAL)}$	= DRAM CURRENT (I_{CC1-7}) + SAMa CURRENT (I_{CC8} or I_{CC10}) + SAMb CURRENT (I_{CC8} or I_{CC10}) + SMI CURRENT (I_{CC9} or I_{CC11}) [+ 10mA (If DRAM CURRENT = I_{CC3} or I_{CC4})]

Example 1:
Operating current (-8) with DRAM operating in Fast Page Mode, SAMa active, SAMb and SMI inactive:

$I_{CC(TOTAL)}$	= DRAM CURRENT (I_{CC2}) + SAMa CURRENT (I_{CC8}) + SAMb CURRENT (I_{CC10}) + SMI CURRENT (I_{CC11}) [+ 0] = 100 + 45 + 0 + 0 = 145mA (MAX)

Example 2:
Operating current (-10) with DRAM operating in CMOS Standby, SAMa and SAMb active, SMI active:

$I_{CC(TOTAL)}$	= DRAM CURRENT (I_{CC4}) + SAMa CURRENT (I_{CC8}) + SAMb CURRENT (I_{CC8}) + SMI CURRENT (I_{CC9}) [+ 10] = 2 + 40 + 40 + 20 + 10 = 112mA (MAX)

DRAM TIMING PARAMETERS

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) ($0°C \le T_A \le +70°C$; $V_{CC} = 5V \pm 5\%$)

AC CHARACTERISTICS		-8		-10			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Random READ or WRITE cycle time	tRC	150		180		ns	
READ-MODIFY-WRITE cycle time	tRWC	205		235		ns	
FAST-PAGE-MODE READ or WRITE cycle time	tPC	50		50		ns	
FAST-PAGE-MODE READ-MODIFY-WRITE cycle time	tPRWC	95		120		ns	
Access time from $\overline{RAS}$	tRAC		80		100	ns	14, 17
Access time from $\overline{CAS}$	tCAC		20		25	ns	15
Access time from ($\overline{TR}$)/$\overline{OE}$	tOE		20		25	ns	
Access time from column address	tAA		40		50	ns	
Access time from $\overline{CAS}$ precharge	tCPA		45		55	ns	
$\overline{RAS}$ pulse width	tRAS	80	20,000	100	20,000	ns	
$\overline{RAS}$ pulse width (FAST PAGE MODE)	tRASP	80	100,000	100	100,000	ns	
$\overline{RAS}$ hold time	tRSH	20		25		ns	
$\overline{RAS}$ precharge time	tRP	60		70		ns	
$\overline{CAS}$ pulse width	tCAS	20	10,000	25	10,000	ns	
$\overline{CAS}$ hold time	tCSH	80		100		ns	
$\overline{CAS}$ precharge time	tCP	10		10		ns	16
$\overline{RAS}$ to $\overline{CAS}$ delay time	tRCD	20	60	25	75	ns	17
$\overline{CAS}$ to $\overline{RAS}$ precharge time	tCRP	5		5		ns	
Row address setup time	tASR	0		0		ns	
Row address hold time	tRAH	12		15		ns	
$\overline{RAS}$ to column address delay time	tRAD	17	40	20	50	ns	18
Column address setup time	tASC	0		0		ns	
Column address hold time	tCAH	15		20		ns	
Column address hold time (referenced to $\overline{RAS}$)	tAR	60		70		ns	
Column address to $\overline{RAS}$ lead time	tRAL	40		50		ns	
Read command setup time	tRCS	0		0		ns	
Read command hold time (referenced to $\overline{CAS}$)	tRCH	0		0		ns	19
Read command hold time (referenced to $\overline{RAS}$)	tRRH	0		0		ns	19
$\overline{CAS}$ to output in Low-Z	tCLZ	3		3		ns	
Output buffer turn-off delay	tOFF	3	20	3	20	ns	20, 23
Output disable	tOD	3	10	3	20	ns	20, 23
Output disable hold time from start of WRITE	tOEH	15		15		ns	28
Output Enable to $\overline{RAS}$ delay	tORD	0		0		ns	

DRAM TIMING PARAMETERS (continued)

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C ≤ T_A ≤ +70°C; Vcc = 5V ±5%)

AC CHARACTERISTICS		-8		-10			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Write command setup time	^tWCS	0		0		ns	21
Write command hold time	^tWCH	15		20		ns	
Write command hold time (referenced to $\overline{RAS}$)	^tWCR	60		75		ns	
Write command pulse width	^tWP	15		15		ns	
Write command to $\overline{RAS}$ lead time	^tRWL	20		25		ns	
Write command to $\overline{CAS}$ lead time	^tCWL	20		25		ns	
Data-in setup time	^tDS	0		0		ns	22
Data-in hold time	^tDH	20		20		ns	22
Data-in hold time (referenced to $\overline{RAS}$)	^tDHR	60		70		ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	^tRWD	100		130		ns	21
Column address to $\overline{WE}$ delay time	^tAWD	60		80		ns	21
$\overline{CAS}$ to $\overline{WE}$ delay time	^tCWD	40		60		ns	21
Transition time (rise or fall)	^tT	3	35	3	35	ns	9, 10
Refresh period (512 cycles)	^tREF		8		8	ms	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	^tRPC	0		0		ns	
$\overline{CAS}$ setup time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tCSR	10		10		ns	5
$\overline{CAS}$ hold time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tCHR	30		30		ns	5
$\overline{ME}$/$\overline{WE}$ to $\overline{RAS}$ setup time	^tWSR	0		0		ns	
$\overline{ME}$/$\overline{WE}$ to $\overline{RAS}$ hold time	^tRWH	15		15		ns	
Mask data to $\overline{RAS}$ setup time	^tMS	0		0		ns	
Mask data to $\overline{RAS}$ hold time	^tMH	15		15		ns	

TRANSFER AND MODE CONTROL TIMING PARAMETERS

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes 6, 7, 8, 9, 10) (0° C ≤ T_A ≤ + 70°C; Vcc = 5V ±5%)

AC CHARACTERISTICS		-8		-10			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
$\overline{TR}/(\overline{OE})$ LOW to $\overline{RAS}$ setup time	^tTLS	0		0		ns	
$\overline{TR}/(\overline{OE})$ LOW to $\overline{RAS}$ hold time	^tTLH	15	10,000	15	10,000	ns	
$\overline{TR}/(\overline{OE})$ LOW to $\overline{RAS}$ hold time (REAL-TIME READ TRANSFER only)	^tRTH	70	10,000	80	10,000	ns	
$\overline{TR}/(\overline{OE})$ LOW to $\overline{CAS}$ hold time (REAL-TIME READ TRANSFER only)	^tCTH	20		25		ns	
$\overline{TR}/(\overline{OE})$ HIGH to SC lead time	^tTSL	5		5		ns	
$\overline{TR}/(\overline{OE})$ HIGH to $\overline{RAS}$ precharge time	^tTRP	60		70		ns	
$\overline{TR}/(\overline{OE})$ precharge time	^tTRW	25		30		ns	
First SC edge to $\overline{TR}/(\overline{OE})$ HIGH delay time	^tTSD	15		15		ns	
$\overline{RAS}$ to first SC edge delay time	^tRSD	80		95		ns	
$\overline{CAS}$ to first SC edge delay time	^tCSD	25		30		ns	
Serial output buffer turn-off delay from $\overline{RAS}$	^tSDZ	10	50	10	50	ns	
SC to $\overline{RAS}$ setup time	^tSRS	30		30		ns	
Serial data input to $\overline{SE}$ delay time	^tSZE	0		0		ns	
$\overline{RAS}$ to SD buffer turn-on time	^tSRO	10		15		ns	
Serial data input delay from $\overline{RAS}$	^tSDD	60		60		ns	
Serial data input to $\overline{RAS}$ delay time	^tSZS	0		0		ns	
Serial Input Mode enable ($\overline{SE}$) to $\overline{RAS}$ setup time	^tESR	0		0		ns	
Serial Input Mode enable ($\overline{SE}$) to $\overline{RAS}$ hold time	^tREH	15		15		ns	
$\overline{TR}/(\overline{OE})$ HIGH to $\overline{RAS}$ setup time	^tYS	0		0		ns	
$\overline{TR}/(\overline{OE})$ HIGH to $\overline{RAS}$ hold time	^tYH	15		15		ns	
DSF, TRM, STS, MKD to $\overline{RAS}$ setup time	^tFSR	0		0		ns	
DSF, TRM, STS, MKD to $\overline{RAS}$ hold time	^tRFH	15		15		ns	
DSF to $\overline{RAS}$ hold time	^tFHR	60		65		ns	
DSF to $\overline{CAS}$ setup time	^tFSC	0		0		ns	
DSF to $\overline{CAS}$ hold time	^tCFH	15		20		ns	
SC to QSF delay time	^tSQD		35		40	ns	29
$\overline{RAS}$ to QSF delay time	^tRQD		65		85	ns	29
$\overline{CAS}$ to QSF delay time	^tCQD		35		40	ns	29
$\overline{TR}/\overline{OE}$ to QSF delay time	^tTQD		25		30	ns	29
SPLIT TRANSFER setup time	^tSTS	30		35		ns	29
SPLIT TRANSFER hold time	^tSTH	0		0		ns	29

SAM TIMING PARAMETERS

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

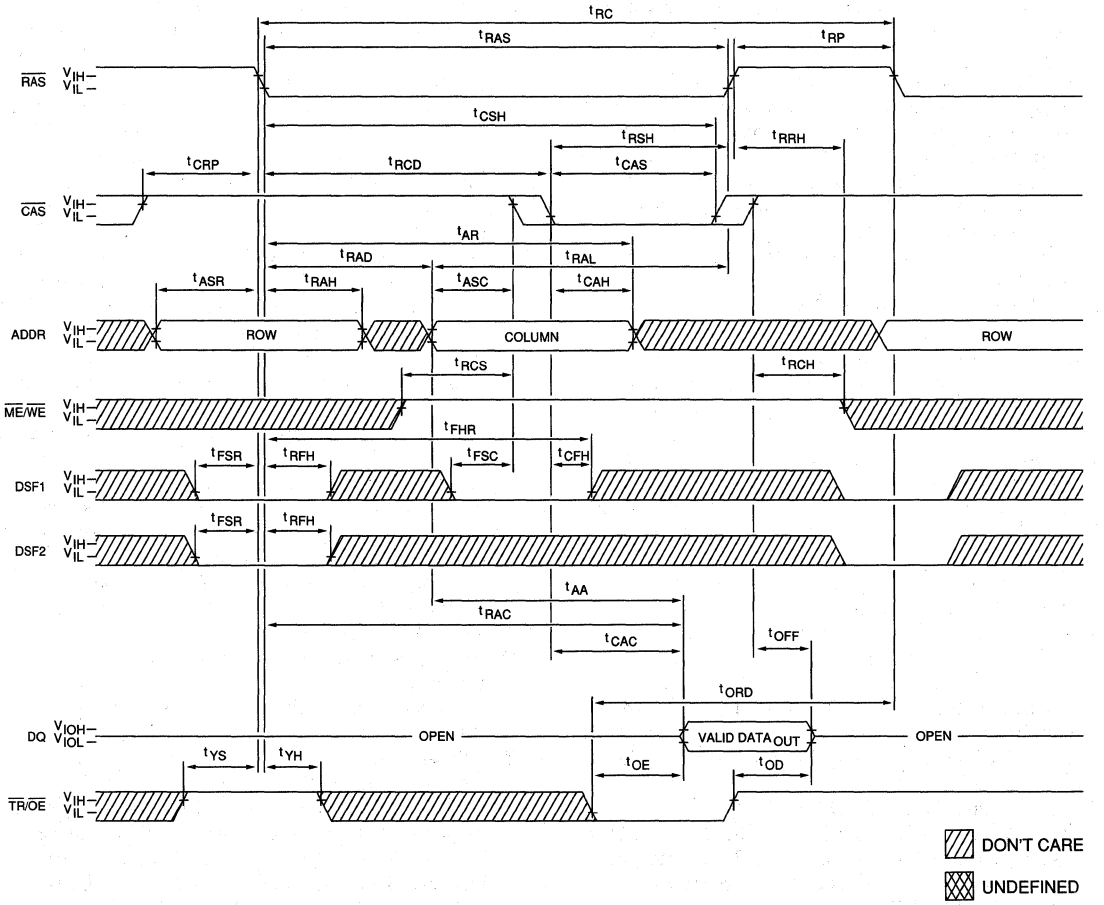
(Notes 6, 7, 8, 9, 10) (0° C ≤ T_A ≤ + 70°C; Vcc = 5V ±5%)

AC CHARACTERISTICS		-8		-10			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Serial clock cycle time	^tSC	28		30		ns	
Access time from SC	^tSAC		25		27	ns	24, 31
SC precharge time (SC LOW time)	^tSP	10		10		ns	
SC pulse width (SC HIGH time)	^tSAS	10		10		ns	
Access time from $\overline{SE}$	^tSEA		15		20	ns	24
$\overline{SE}$ precharge time	^tSEP	10		15		ns	
$\overline{SE}$ pulse width	^tSE	10		15		ns	
Serial data out hold time after SC HIGH	^tSOH	5		5		ns	24, 31
Serial output buffer turn-off delay from $\overline{SE}$	^tSEZ	3	12	3	15	ns	20, 24
Serial data in setup time	^tSDS	0		0		ns	24
Serial data in hold time	^tSDH	10		10		ns	24
Serial mask data in setup time	^tMDS	0		0		ns	
Serial mask data in hold time	^tMDH	10		10		ns	
SERIAL INPUT (Write) Enable setup time	^tSWS	0		0		ns	
SERIAL INPUT (Write) Enable hold time	^tSWH	15		15		ns	
SERIAL INPUT (Write) disable setup time	^tSWIS	0		0		ns	
SERIAL INPUT (Write) disable hold time	^tSWIH	15		15		ns	
SSF to SC setup time	^tSFS	0		0		ns	30
SSF to SC hold time	^tSFH	15		20		ns	30
SSF LOW to SC HIGH delay	^tSFD	5		5		ns	30

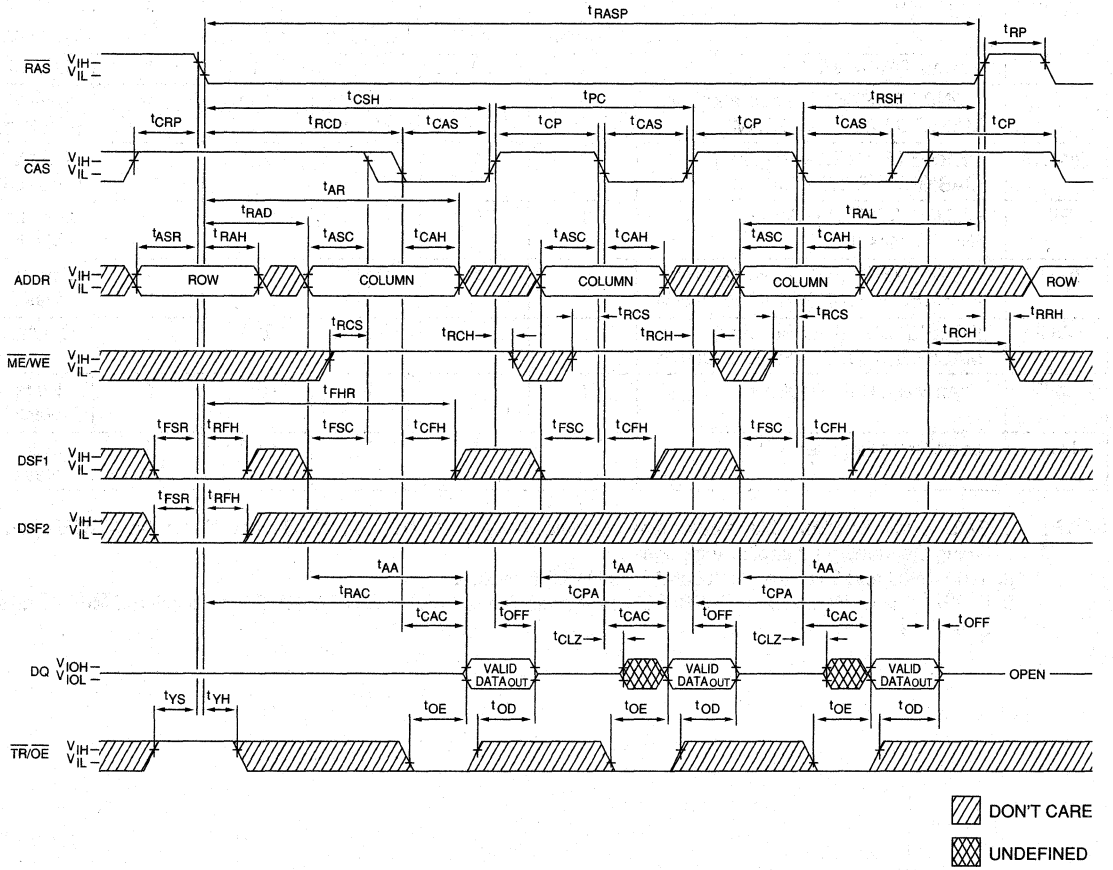
NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. V_{CC} = 5V ±5%, f = 1 MHz.
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading. Specified values are obtained with minimum cycle time and the outputs open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is assured.
7. An initial pause of 100µs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is assured. The 8 $\overline{RAS}$ cycle wake-up should be repeated any time the ^tREF refresh requirement is exceeded.
8. AC characteristics assume ^tT = 5ns.
9. V_{IH} MIN and V_{IL} MAX are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}). Input signals transition between 0V and 3V for AC testing.
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS}$ = V_{IH}, DRAM data outputs (DQ1-DQ8) is High-Z.
12. If $\overline{CAS}$ = V_{IL}, DRAM data outputs (DQ1-DQ8) may contain data from the last valid READ cycle.
13. DRAM output timing measured with a load equivalent to 1 TTL gate and 50pF. Output reference levels: V_{OH} = 2.0V; V_{OL} = 0.8V.
14. Assumes that ^tRCD < ^tRCD (MAX). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
15. Assumes that ^tRCD ≥ ^tRCD (MAX).
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, DQ will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer, $\overline{CAS}$ must be pulsed HIGH for ^tCP.
17. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (MAX) limit, then access time is controlled exclusively by ^tCAC.
18. Operation within the ^tRAD (MAX) limit ensures that ^tRCD (MAX) can be met. ^tRAD (MAX) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (MAX) limit, then access time is controlled exclusively by ^tAA.
19. Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
20. ^tOD, ^tOFF and ^tSEZ define the time when the output achieves open circuit (V_{OH} -200mV, V_{OL} +200mV). This parameter is sampled and not 100% tested.
21. ^tWCS, ^tRWD, ^tAWD and ^tCWD are restrictive operating parameters in LATE-WRITE, READ-WRITE and READ-MODIFY-WRITE cycles only. If ^tWCS ≥ ^tWCS (MIN), the cycle is an EARLY-WRITE cycle and the data output will remain an open circuit throughout the entire cycle, regardless of $\overline{TR}/\overline{OE}$. If ^tWCS ≤ ^tWCS (MIN), the cycle is a LATE-WRITE and $\overline{TR}/\overline{OE}$ must control the output buffers during the WRITE to avoid data contention. If ^tRWD ≥ ^tRWD (MIN), ^tAWD ≥ ^tAWD (MIN) and ^tCWD ≥ ^tCWD (MIN), the cycle is a READ-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of the output buffers (at access time and until $\overline{CAS}$ goes back to V_{IH}) is indeterminate but the WRITE will be valid, if ^tOD and ^tOEH are met. See the LATE-WRITE AC Timing diagram.
22. These parameters are referenced to $\overline{CAS}$ leading edge in early WRITE cycles and $\overline{ME}/\overline{WE}$ leading edge in late WRITE or READ-WRITE cycles.
23. During a READ cycle, if $\overline{TR}/\overline{OE}$ is LOW then taken HIGH, DQ goes open. The DQs will go open with $\overline{OE}$ or $\overline{CAS}$, whichever goes HIGH first.
24. SAM output timing is measured with a load equivalent to 1 TTL gate and 30pF. Output reference levels: V_{OH} = 2.0V; V_{OL} = 0.8V.
25. Addresses (A0-A8) change two times or less while $\overline{RAS}$ = V_{IL}.
26. Addresses (A0-A8) change once or less while $\overline{RAS}$ = L.
27. Addresses (A0-A8) change once or less while $\overline{CAS}$ = V_{IH} and $\overline{RAS}$ = V_{IL}.
28. LATE-WRITE and READ-MODIFY-WRITE cycles must have ^tOD and ^tOEH met ($\overline{OE}$ HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. The DQs will provide previously read data if $\overline{CAS}$ remains LOW and $\overline{OE}$ is taken LOW after ^tOEH is met. If $\overline{CAS}$ goes HIGH prior to $\overline{OE}$ going back LOW, the DQs will remain open.
29. Applies to the MT43C8128 only.
30. Applies to the MT43C8129 only.
31. ^tSAC is MAX at 70° C and 4.75V Vcc; ^tSOH is MIN at 0°C and 5.25V Vcc. These limits will not occur simultaneously at any given voltage or temperature ^tSOH = ^tSAC - output transition time; this is guaranteed by design.

DRAM READ CYCLE



DRAM FAST PAGE MODE READ CYCLE

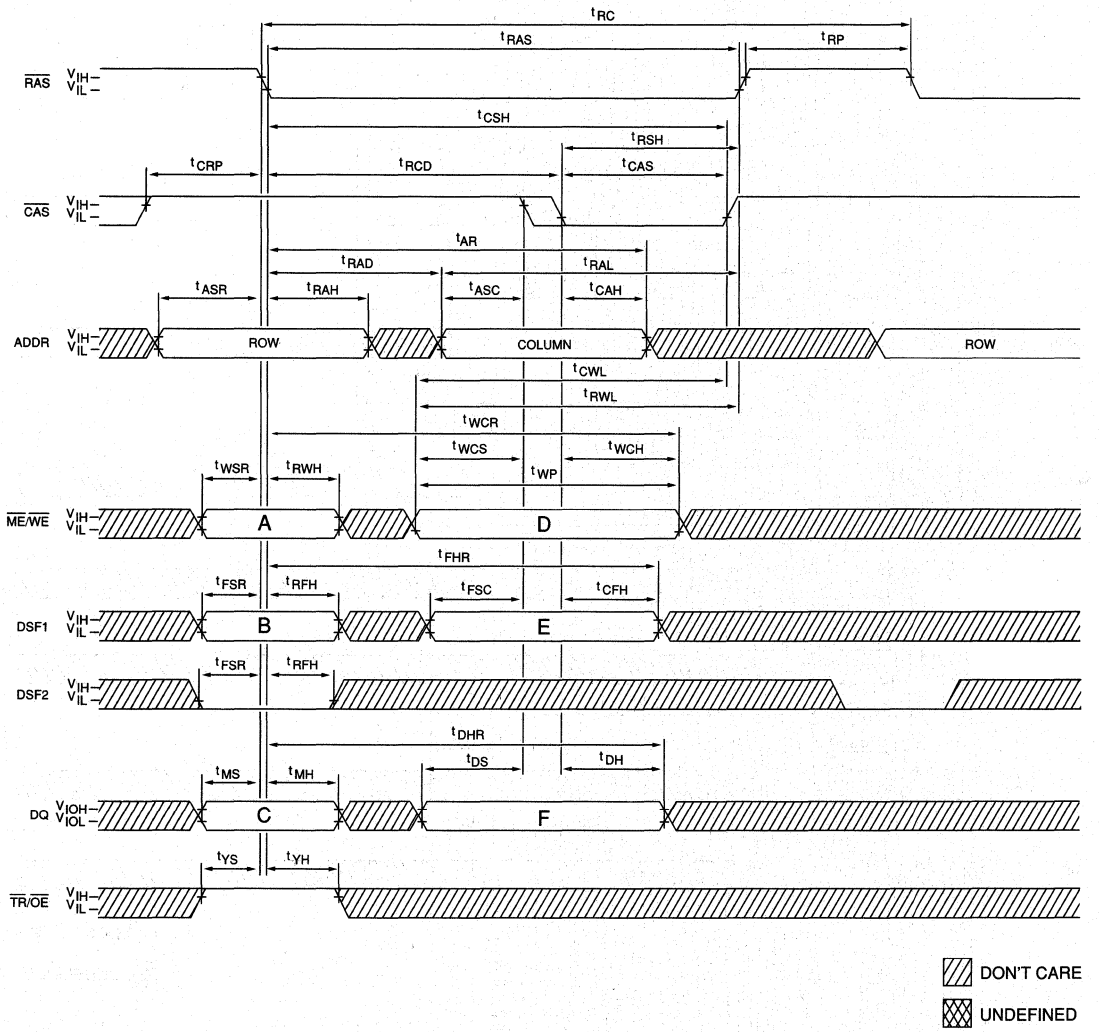


WRITE CYCLE FUNCTION TABLE [1]

CODE	FUNCTION	LOGIC STATES[2]					
		RAS Falling Edge			CAS Falling Edge		
		A ME/WE	B DSF1	C DQ (Input)	D ME/WE	E DSF1	F DQ (Input)
RW	Normal DRAM WRITE	1	0	X	0	0	DRAM
RWNM	NONPERSISTENT (Load and Use) MASKED WRITE to DRAM	0	0	Write Mask	0/1[3]	0	DRAM (Masked)
RWOM	PERSISTENT (Use Register) MASKED WRITE to DRAM	0	1	X	0/1[3]	0	DRAM (Masked)
BW	BLOCK WRITE to DRAM (No DQ Mask)	1	0	X	0/1[3]	1	Column Mask
BWNM	NONPERSISTENT (Load and Use) MASKED BLOCK WRITE to DRAM	0	0	Write Mask	0/1[3]	1	Column Mask
BWOM	PERSISTENT (Use Register) MASKED BLOCK WRITE to DRAM	0	1	X	0/1[3]	1	Column Mask
LMR	Load Mask Data Register	1	1	X	0/1[3]	0	Write Mask
LCR	Load Color Register	1	1	X	0/1[3]	1	Color Mask

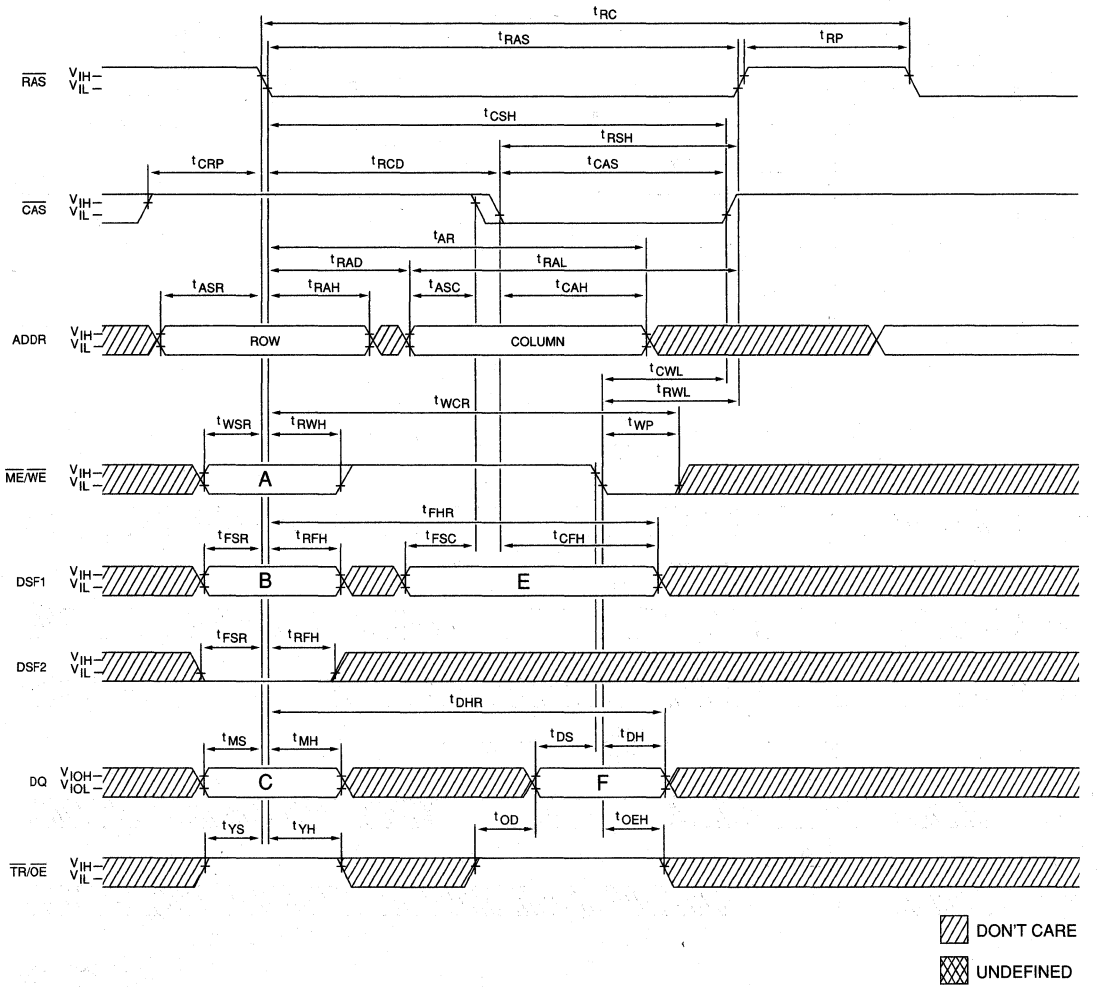
NOTE:
1. Refer to this function table to determine the logic states of "A", "B", "C", "D", "E" and "F" for the WRITE cycle timing diagrams on the following pages.
2. TRM, MKD and STS are "don't care" for all WRITE cycles.
3. If $\overline{ME}/\overline{WE}$ is LOW, an EARLY-WRITE is performed; if it is HIGH, a LATE-WRITE is performed if $\overline{ME}/\overline{WE}$ falls after $\overline{CAS}$.

DRAM EARLY-WRITE CYCLE



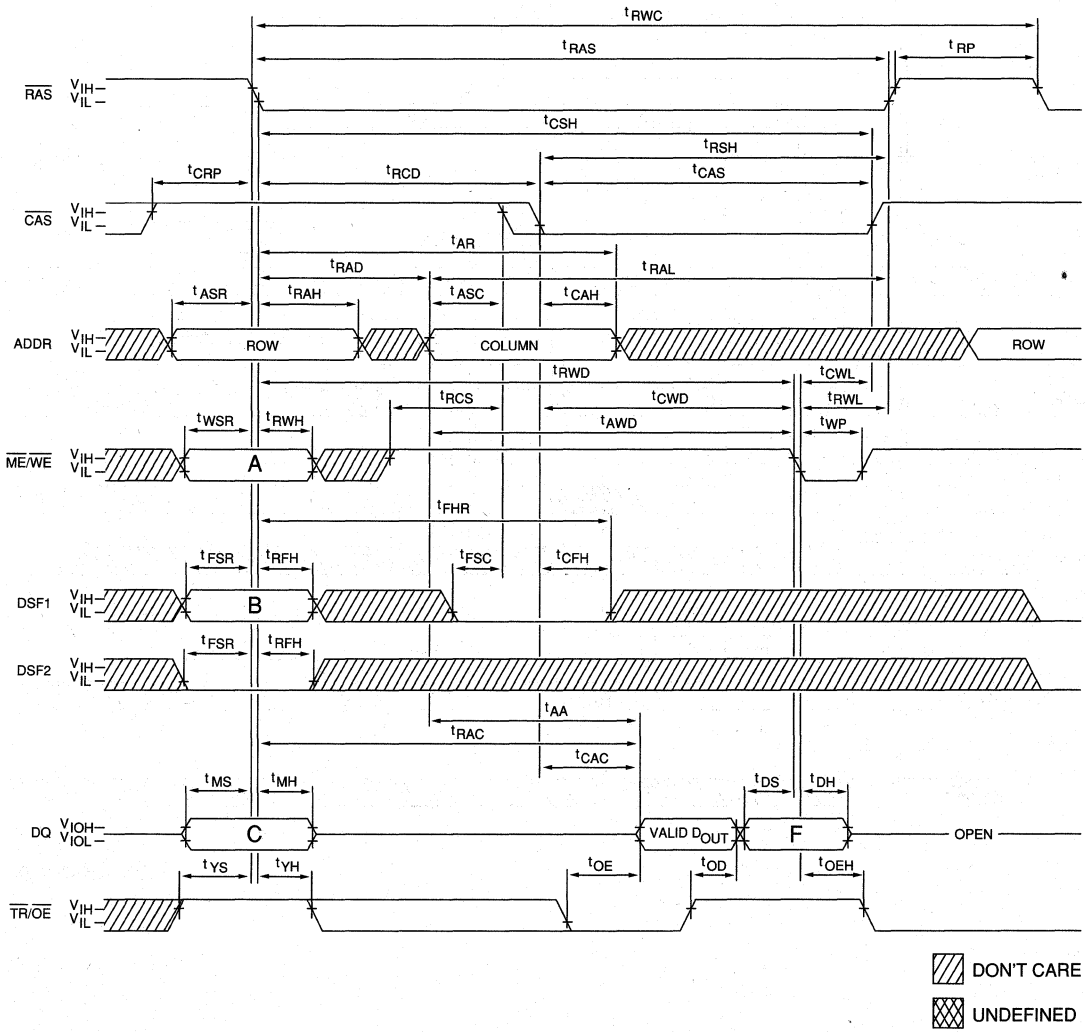
NOTE: The logic states of "A", "B", "C", "D", "E" and "F" determine the type of WRITE operation performed. See the WRITE Cycle Function Table for a detailed description.

DRAM LATE-WRITE CYCLE [1]



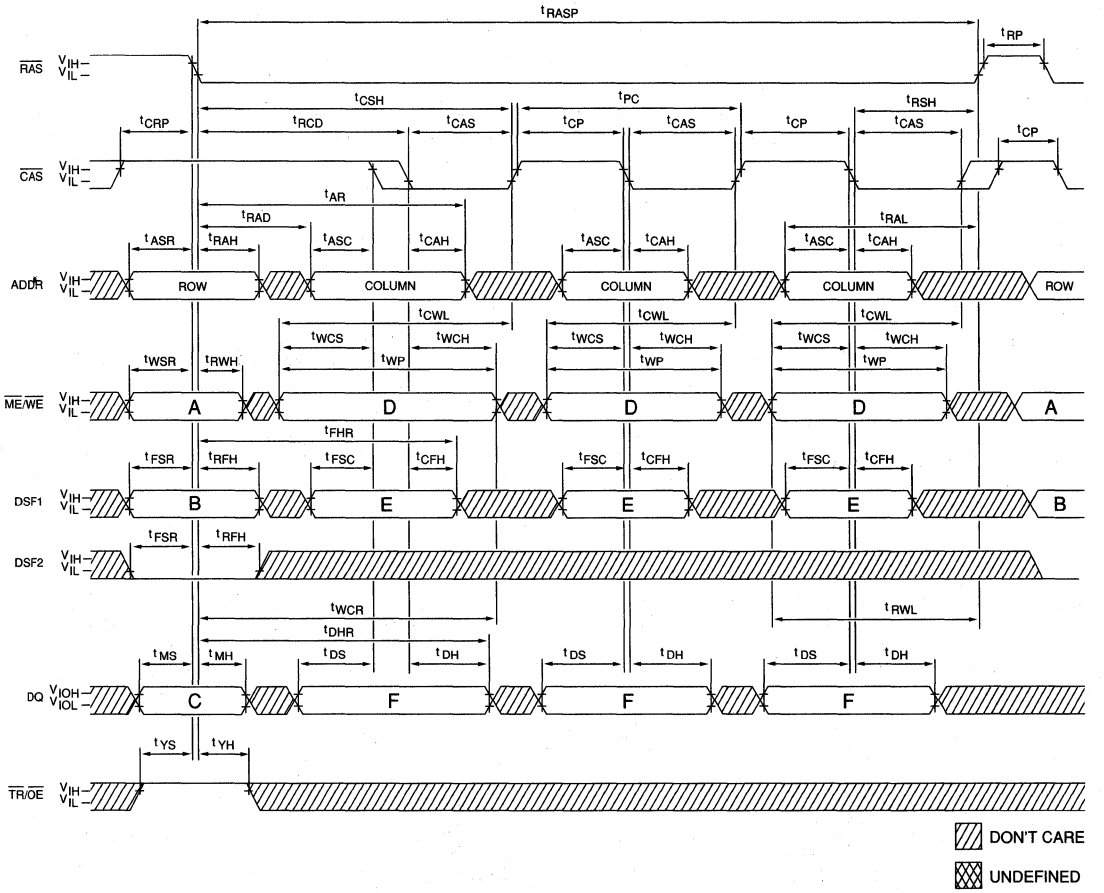
NOTE: 1. The logic states of "A", "B", "C", "E" and "F" determine the type of WRITE operation performed. See the Write Cycle Function Table for a detailed description.

DRAM READ-WRITE CYCLE
(READ-MODIFY-WRITE CYCLE)



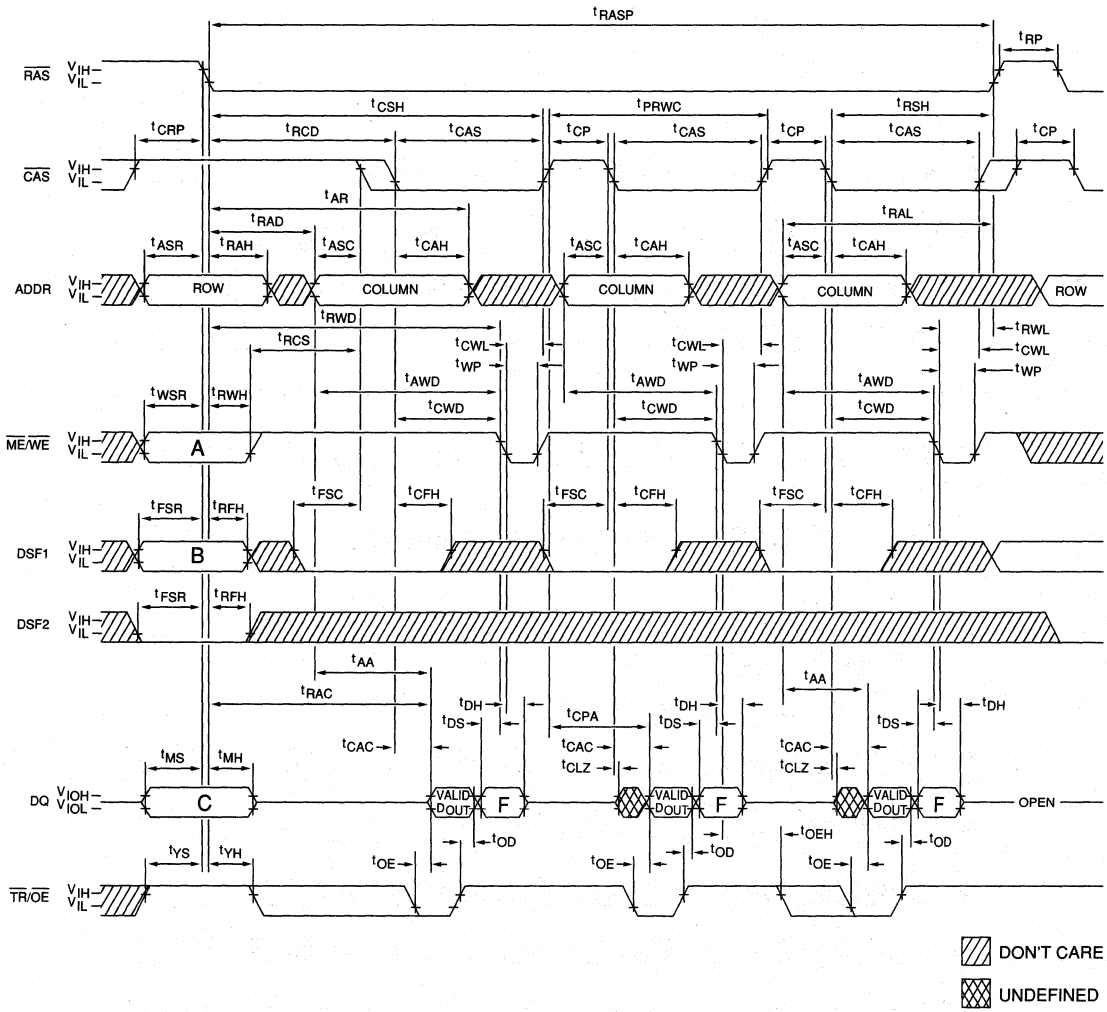
NOTE: The logic states of "A", "B", "C" and "F" determine the type of WRITE operation performed. See the Write Cycle Function Table for a detailed description.

DRAM FAST-PAGE-MODE EARLY-WRITE CYCLE [1, 2]



NOTE:
1. READ cycles or READ-MODIFY-WRITE cycles may be mixed with WRITE cycles while in FAST PAGE MODE.
2. The logic states of "A", "B", "C", "D", "E" and "F" determine the type of WRITE operation performed. See the Write Cycle Function Table for a detailed description.

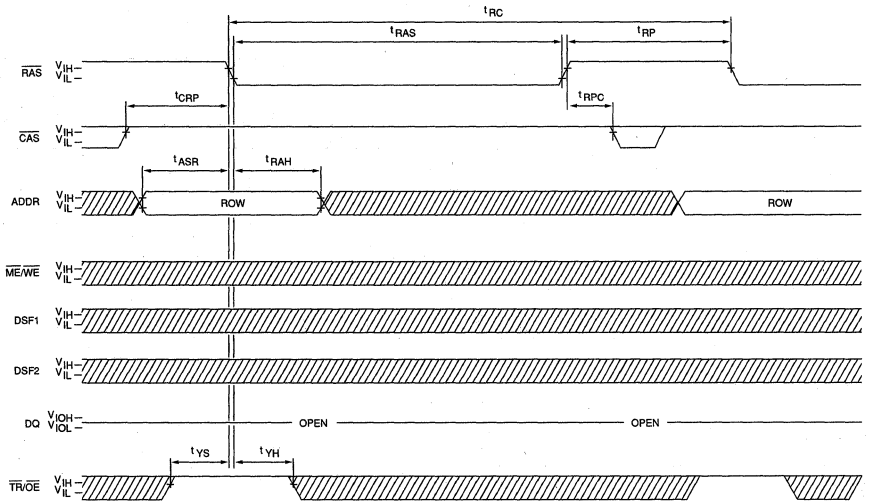
DRAM FAST-PAGE-MODE READ-WRITE CYCLE
(READ-MODIFY-WRITE or LATE-WRITE CYCLES)



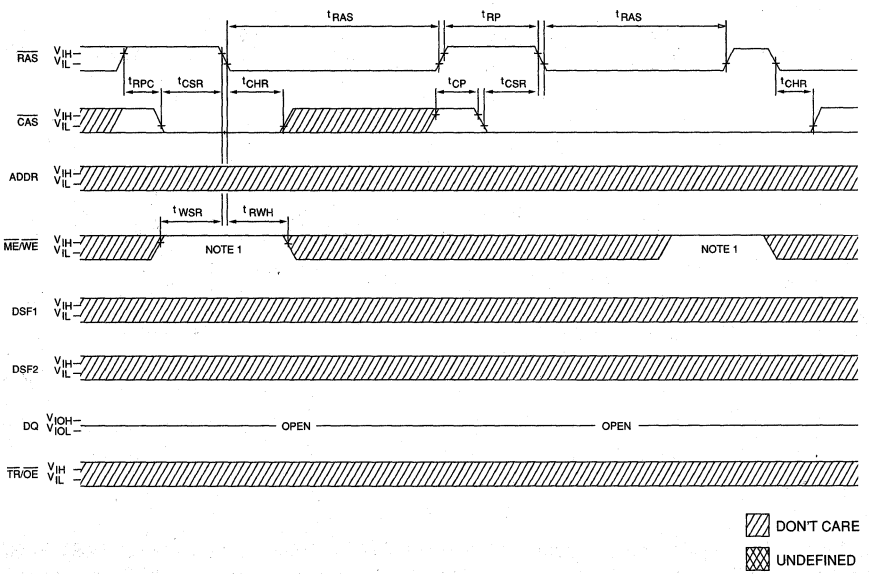
NOTE: 1. READ or WRITE cycles may be mixed with READ-MODIFY-WRITE cycles while in FAST PAGE MODE. Use the Write Function Table to determine the proper DSF1 state for the desired WRITE operation.
2: The logic states of "A", "B", "C" and "F" determine the type of WRITE operation performed. See the Write Cycle Function Table for a detailed description.

MULTIPORT DRAM

DRAM $\overline{RAS}$-ONLY REFRESH CYCLE
(ADDR = A0-A8)

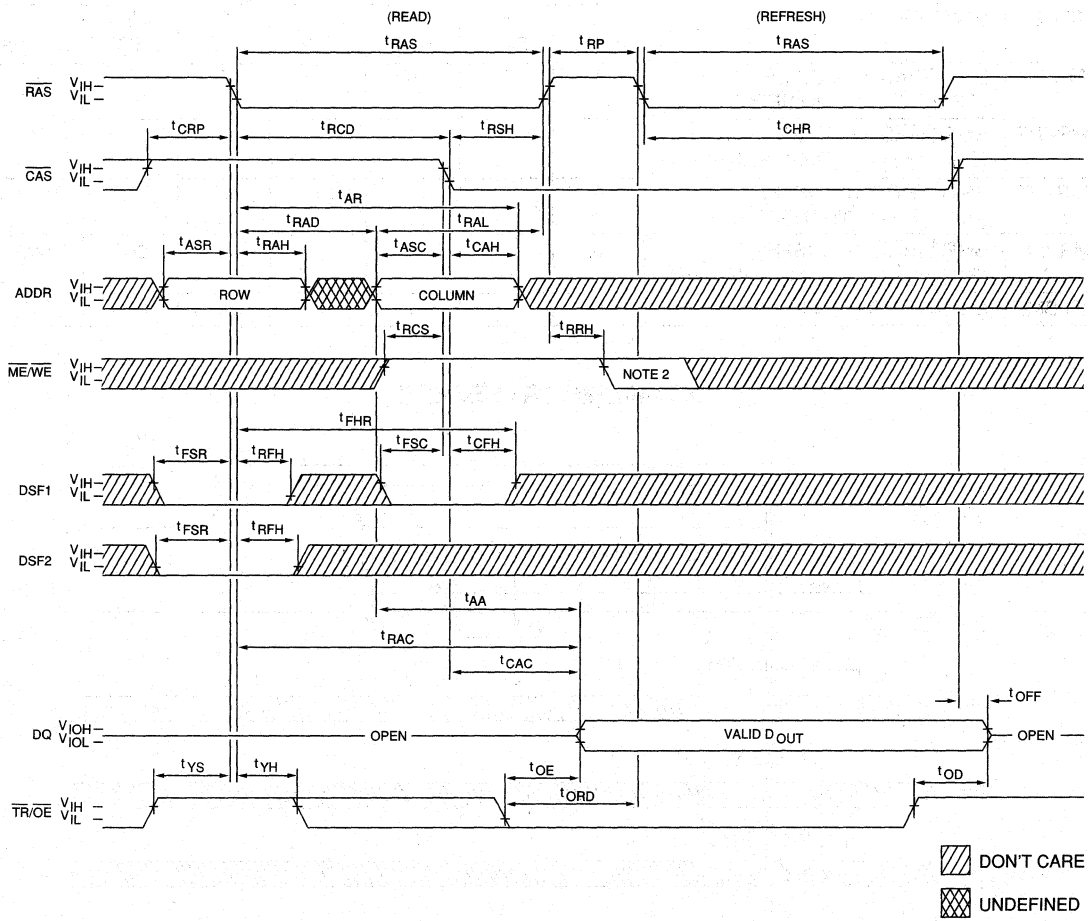


$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE



NOTE: 1. The MT43C8128/9 operates with this state as "don't care," but to allow for future functional enhancements it is recommended that they be driven as illustrated for system upgradability.

DRAM HIDDEN-REFRESH CYCLE

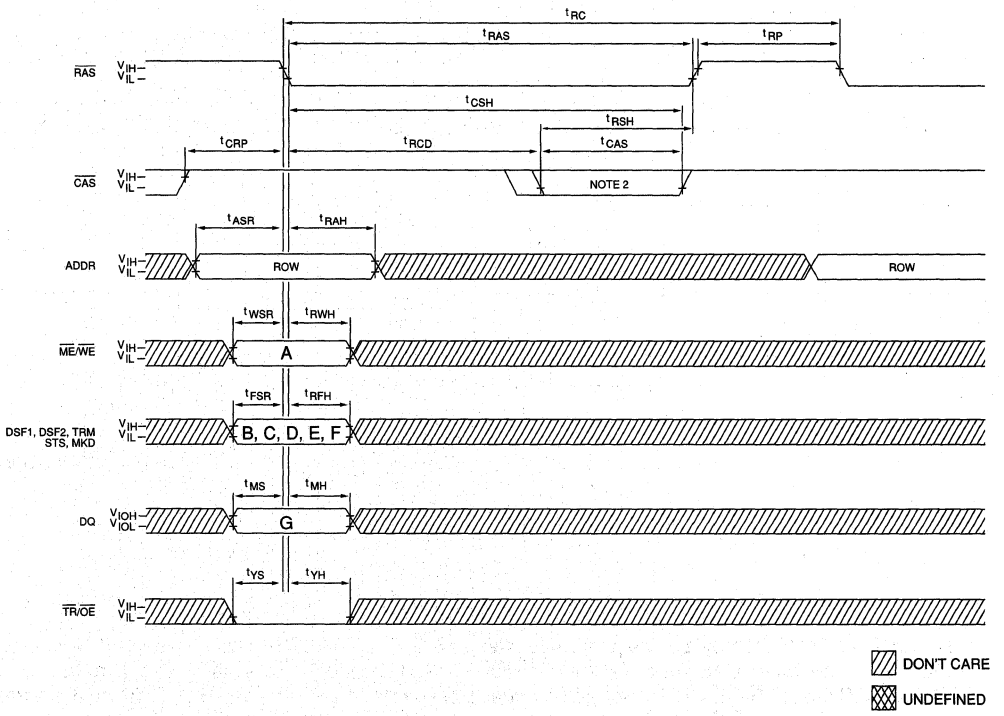


NOTE:
1. A HIDDEN REFRESH may also be performed after a WRITE or TRANSFER cycle. In the WRITE case, $\overline{ME}/\overline{WE}$ = LOW (when $\overline{CAS}$ goes LOW) and $\overline{TR}/\overline{OE}$ = HIGH and the DQ pins stay HIGH-Z. In the TRANSFER case, $\overline{TR}/\overline{OE}$ = LOW (when $\overline{RAS}$ goes LOW) and the DQ pins stay High-Z during the refresh period, regardless of $\overline{TR}/\overline{OE}$.
2. The MT43C8128/9 operates with this state as "don't care," but to allow for future functional enhancements it is recommended that they be driven as illustrated for system upgradability.

DRAM/BMR TRANSFER CYCLE FUNCTION TABLE [1]

CODE	FUNCTION	LOGIC STATES						
		RAS Falling Edge						
		A ME/WE	B DSF1	C DSF2	D TRM	E STS	F MKD	G DQ(Input)
BMR-RT	BMR READ TRANSFER (DRAM→BMR TRANSFER)	1	0	0	1	0	0/1[1]	X
BMR-IRT	BMR READ TRANSFER (DRAM→invert→BMR TRANSFER)	1	0	0	1	1	0/1[1]	X
BMR-WT	BMR WRITE TRANSFER (BMR→DRAM TRANSFER)	0	0	0	1	0	0/1[1]	Mask
BMR-IWT	BMR WRITE TRANSFER (BMR→invert→DRAM TRANSFER)	0	0	0	1	1	0/1[1]	Mask
CLR-BMR	CLEAR BMR (CLR-BMR)	1	1	1	0	X	0/1[1]	X

DRAM/BMR TRANSFERS



NOTE: 1. Serial Mask Input mode is enabled if MKD = HIGH; disabled if MKD = LOW.
2. It is not necessary to drop CAS during a DRAM/BMR TRANSFER.

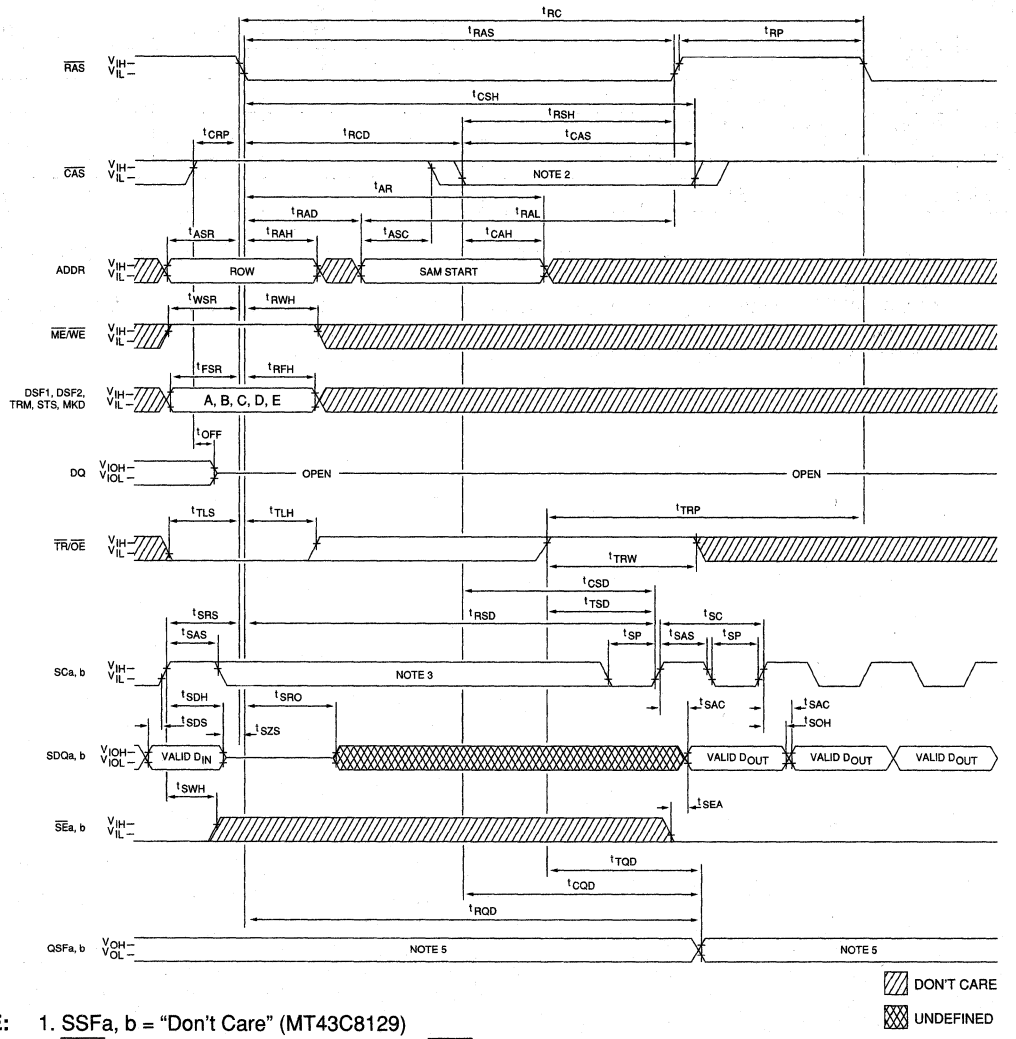
MULTIPORT DRAM

READ TRANSFER CYCLE FUNCTION TABLE [1]

CODE	FUNCTION	LOGIC STATES				
		$\overline{RAS}$ Falling Edge				
		A DSF1	B DSF2	C TRM	D STS	E MKD
RW	READ TRANSFER	0	0	0	0/1[2]	X
SRT	SPLIT READ TRANSFER (DRAM→SAM)	1	0	0	0/1[2]	X
BMRT	BIT MASKED READ TRANSFER	0	1	1	0/1[2]	X
BMSRT	BIT MASKED SPLIT READ TRANSFER	1	1	1	0/1[2]	X
BMR-SAM	BMR→SAM TRANSFER	1	0	1	0/1[2]	0/1[3]

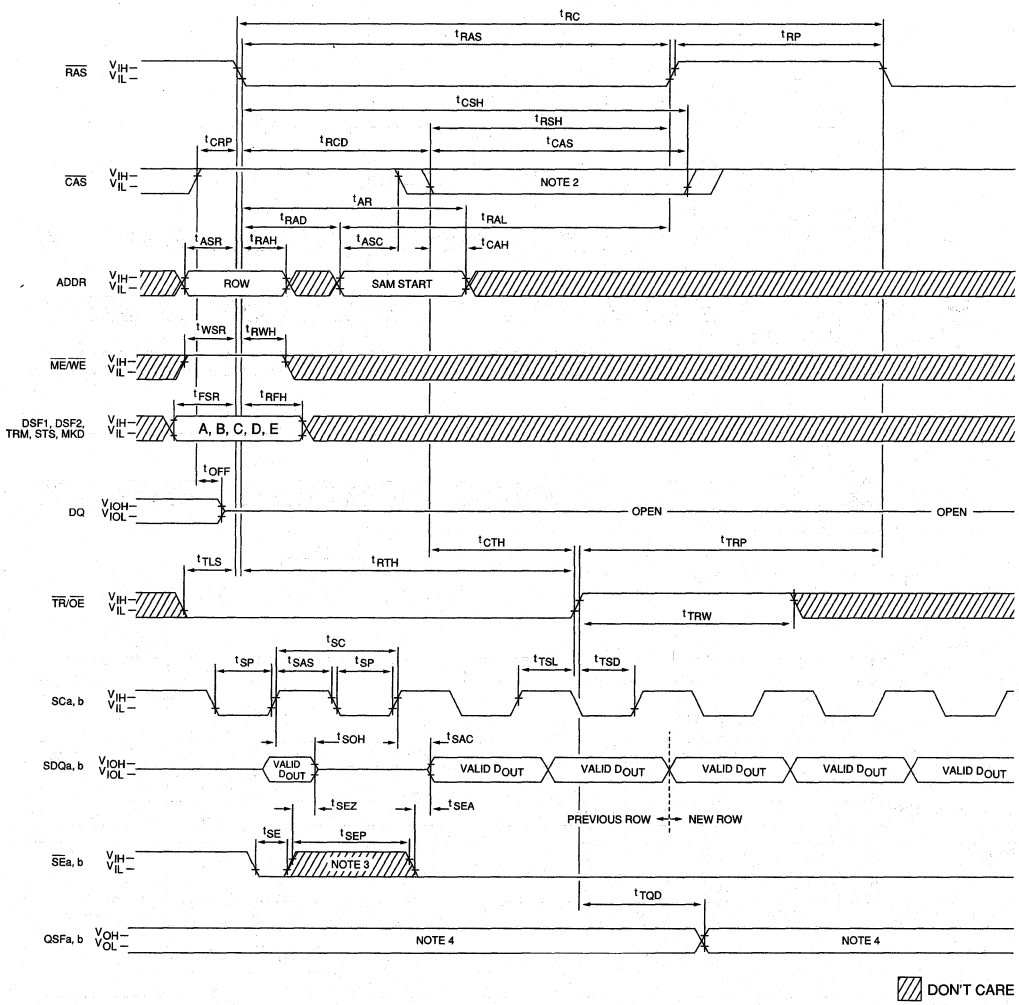
NOTE:
1. Refer to this function table to determine the logic states of "A", "B", "C", "D" and "E" for READ TRANSFER cycle timing diagrams on the following pages.
2. The state of STS at the falling edge of $\overline{RAS}$ determines the SAM involved in the transfer. When STS = LOW, the transfer is to SAMa; when STS = HIGH, the transfer is to SAMb.
3. Serial Mask Input mode is enabled if MKD = HIGH; disabled if MKD = LOW.

READ TRANSFER [1, 4]
(DRAM-TO-SAM TRANSFER)
(When part was previously in the SERIAL INPUT mode)



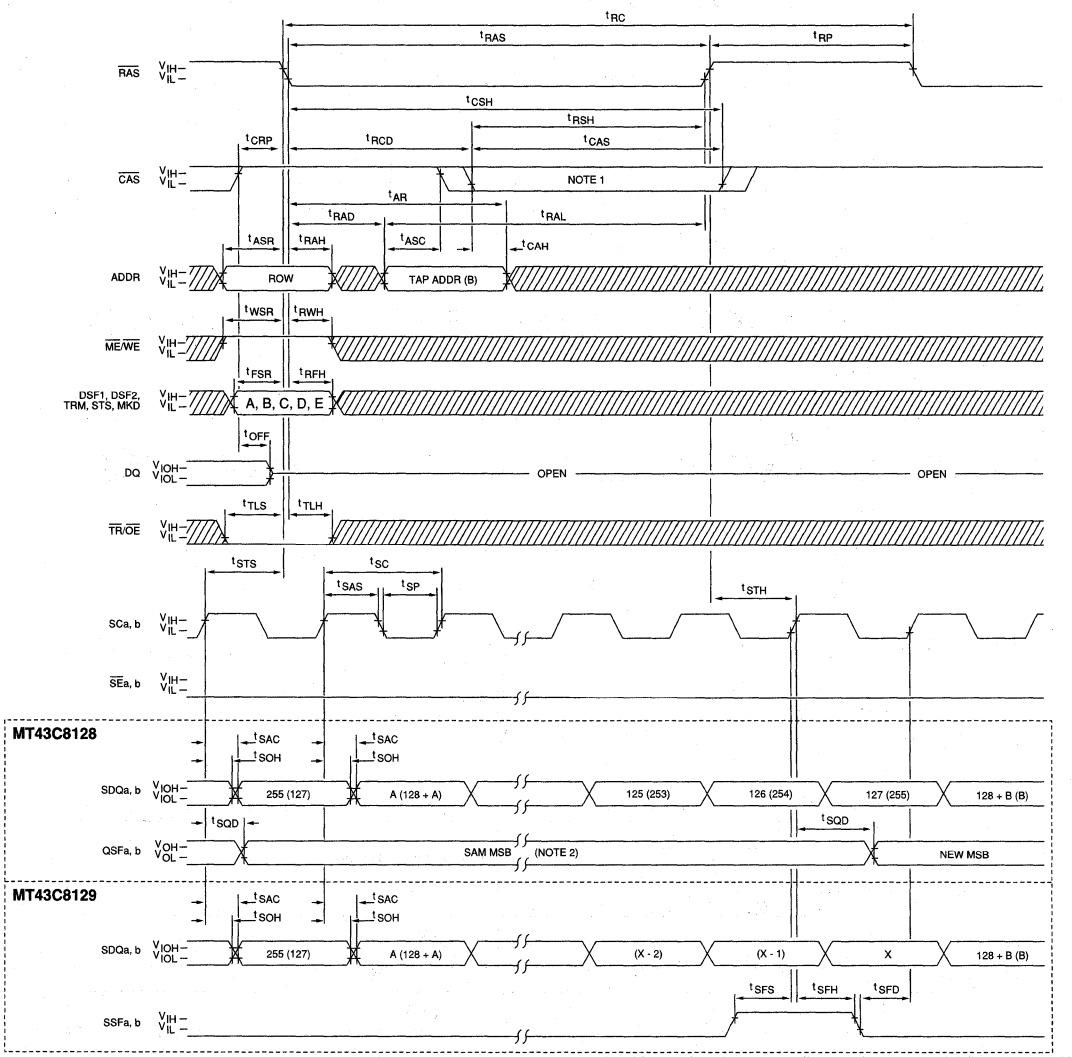
NOTE:
1. SSFa, b = "Don't Care" (MT43C8129)
2. $\overline{CAS}$ is used to load the Tap address. If $\overline{CAS}$ does not fall, the last Tap address loaded for the addressed SAM will be reused.
3. There must be no rising edges on the SC input during this time period.
4. The logic states of "A", "B", "C", "D" and "E" determine the type of TRANSFER operation performed. See the Read Transfer Cycle Function Table.
5. QSF = 0 when the Lower SAM (bits 0–127) is being accessed.
   QSF = 1 when the Upper SAM (bits 128–255) is being accessed.

REAL-TIME READ TRANSFER [1, 4]
(DRAM-TO-SAM TRANSFER)
(When part was previously in the SERIAL OUTPUT mode)



NOTE:
1. SSFa, b = "Don't Care" (MT43C8129)
2. $\overline{CAS}$ is used to load the Tap address. If $\overline{CAS}$ does not fall, the last Tap address loaded for the addressed.
3. The $\overline{SE}$ pulse is shown to illustrate the serial output enable and disable timing. It is not required.
4. The logic states of "A", "B", "C", "D" and "E" determine the type of TRANSFER operation performed. See the Read Transfer Cycle Function Table.
5. QSF = 0 when the Lower SAM (bits 0–127) is being accessed.
   QSF = 1 when the Upper SAM (bits 128–255) is being accessed.

SPLIT READ TRANSFER [3]
(SPLIT DRAM-TO-SAM TRANSFER)



NOTE:
1. $\overline{CAS}$ is used to load the Tap address. If $\overline{CAS}$ does not fall, the last Tap address loaded for the addressed SAM will be reused for the idle half.
2. QSF = 0 when the Lower SAM (bits 0–127) is being accessed.
   QSF = 1 when the Upper SAM (bits 128–255) is being accessed.
3. The logic states of "A", "B", "C", "D" and "E" determine the type of TRANSFER operation performed. See the Read Transfer Cycle Function Table.

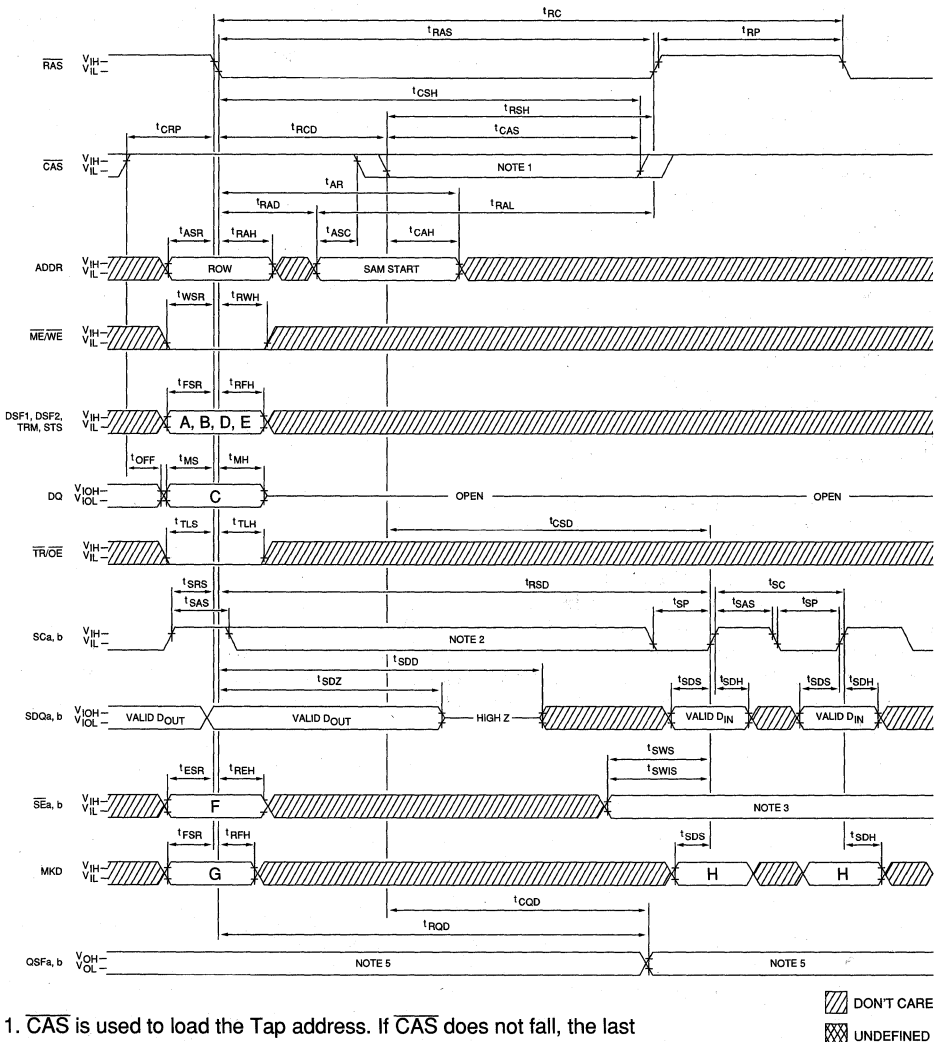
WRITE TRANSFER CYCLE FUNCTION TABLE [1]

CODE	FUNCTION	LOGIC STATES							
		RAS Falling Edge							SC
		A DSF1	B DSF2	C DQ	D TRM	E STS	F $\overline{SE}$	G MKD	H MKD
WT	WRITE TRANSFER (SAM→DRAM)	0	0	X	0	0/1[2]	0	X	-
PWT	PSEUDO WRITE TRANSFER	0	0	X	0	0/1[2]	1	X	-
MSWT	DQ MASKED SPLIT WRITE TRANSFER (SAM→DRAM)	1	0	Mask	0	0/1[2]	X	X	-
MWT	DQ MASKED WRITE TRANSFER (SAM→DRAM)	0	1	Mask	0	0/1[2]	X	X	-
BMWT	BIT MASKED WRITE TRANSFER (SAM→DRAM)	0	1	X	1	0/1[2]	X	X	0/1[4]
BMSWT	BIT MASKED SPLIT WRITE TRANSFER (SAM→DRAM)	1	1	Mask	1	0/1[2]	X	X	0/1[4]
SAM-BMR	(SAM→BMR) TRANSFER	1	0	X	1	0/1[2]	X	0/1[3]	-

NOTE:
1. Refer to this function table to determine the logic states of "A", "B", "C", "D", "E", "F", "G" and "H" for WRITE TRANSFER cycle timing diagrams on the following pages.
2. The state of STS at the falling edge of RAS determines the SAM involved in the transfer. When STS = LOW, the transfer is to SAMa; when SAM = HIGH, the transfer is to SAMb.
3. Serial Mask Input (SMI) mode is enabled if MKD = HIGH and disabled if MKD = LOW.
4. When in the SMI mode (see BMR transfer waveforms) MKD is the SMI data input. MKD data is clocked into all bit planes of the bit mask register with SCb. A logic "1" on MKD will allow data to pass through all the mask; a logic "0" will mask the corresponding location of the SAM during a BIT MASKED TRANSFER. BIT MASKED TRANSFERs to or from SAMa must not take place while mask data is being serially input via SCb and MKD.

WRITE TRANSFER [4]

(When part was previously in the SERIAL OUTPUT mode)

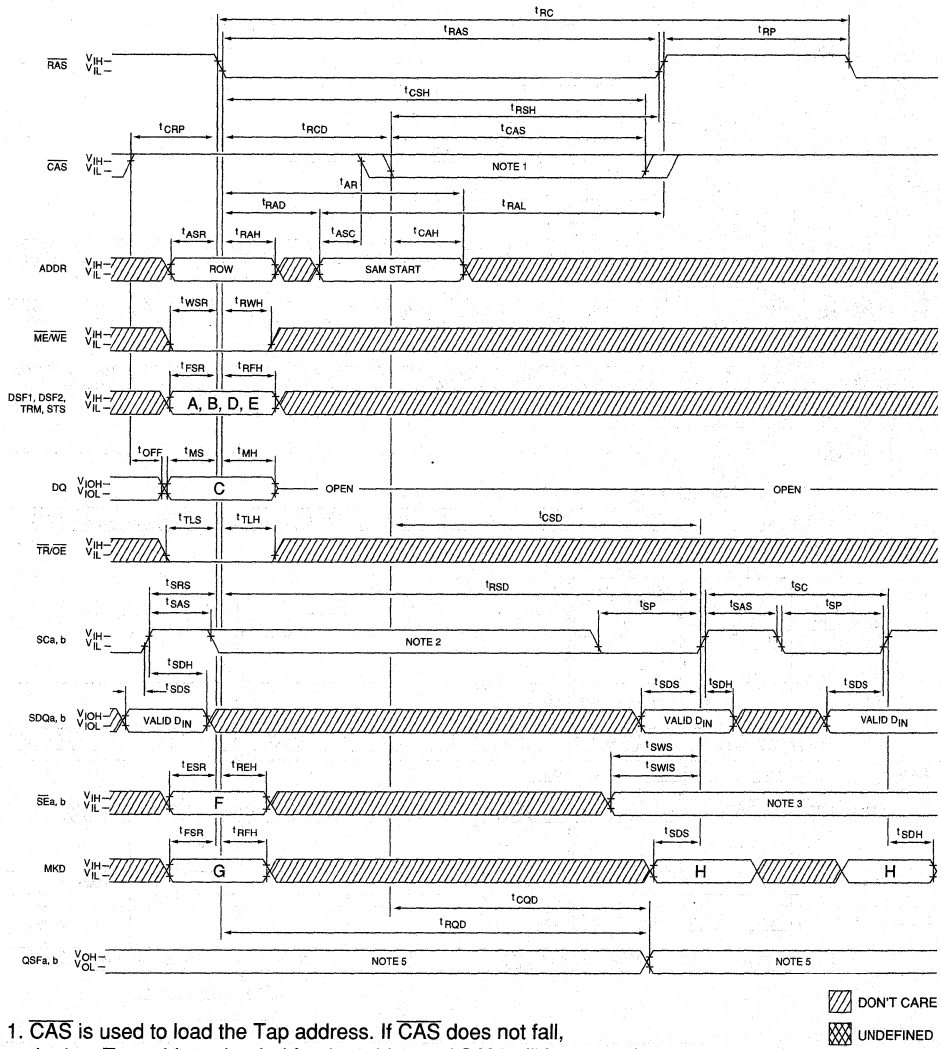


NOTE:

1. $\overline{CAS}$ is used to load the Tap address. If $\overline{CAS}$ does not fall, the last Tap address loaded for the addressed SAM will be reused.
2. There must be no rising edges on the SC input during this time period.
3. $\overline{SE}$ must be LOW to input new serial data, but the serial address register is incremented by SC regardless of $\overline{SE}$.
4. The logic states of "A", "B", "C", "D", "E", "F", "G" and "H" determine the type of TRANSFER operation performed. See the Write Transfer Cycle Function Table.
5. QSF = 0 when the Lower SAM (bits 0–127) is being accessed.
   QSF = 1 when the Upper SAM (bits 128–255) is being accessed. SSFa,b = "don't care" (MT43C8129).

WRITE TRANSFER [4]

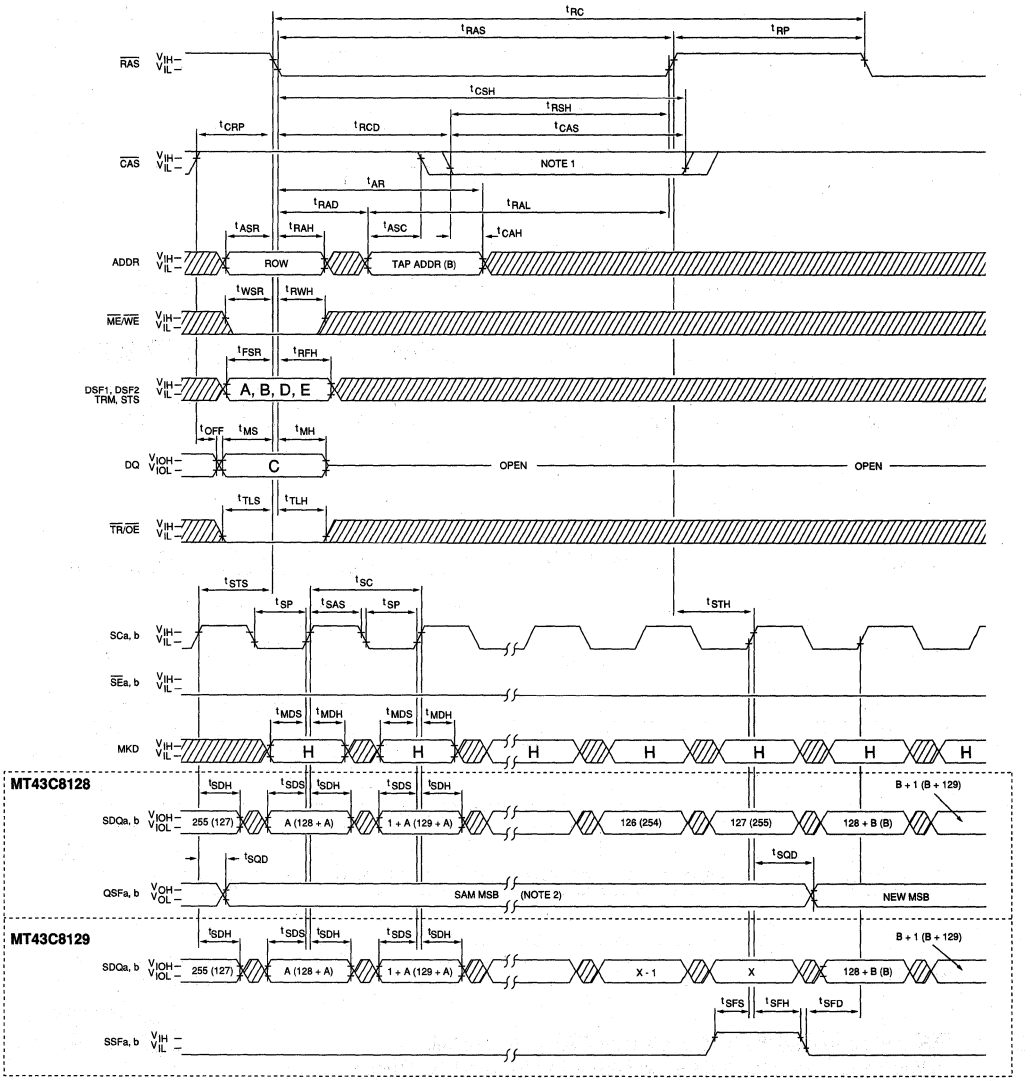
(When part was previously in the SERIAL INPUT mode)



OTE:

1. $\overline{CAS}$ is used to load the Tap address. If $\overline{CAS}$ does not fall, the last Tap address loaded for the addressed SAM will be reused.
2. $\overline{SE}$ must be LOW to input new serial data, but the serial address register is incremented by SC regardless of $\overline{SE}$.
3. There must be no rising edges on the SC input during this time period.
4. The logic states of "A", "B", "C", "D", "E", "F", "G" and "H" determine the type of TRANSFER operation performed. See the Write Transfer Cycle Function Table.
5. QSF = 0 when the Lower SAM (bits 0–127) is being accessed.
   QSF = 1 when the Upper SAM (bits 128–255) is being accessed. SSFa,b = "don't care" (MT43C8129).

SPLIT WRITE TRANSFER [3]
(SPLIT SAM-TO-DRAM TRANSFER)

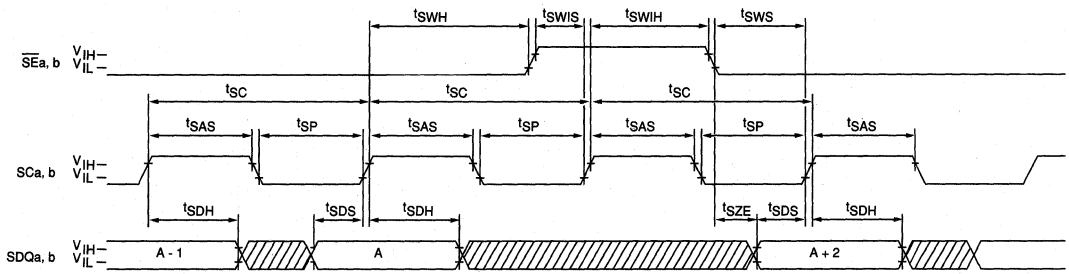


DON'T CARE

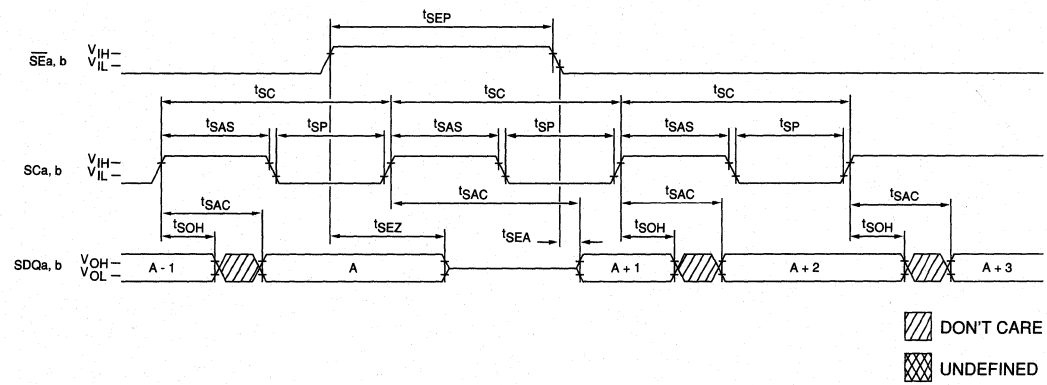
UNDEFINED

NOTE:
1. $\overline{CAS}$ is used to load the Tap address. If $\overline{CAS}$ does not fall, the last Tap address loaded for the addressed SAM will be reused.
2. QSF = 0 when the Lower SAM (bits 0–127) is being accessed.
   QSF = 1 when the Upper SAM (bits 128–255) is being accessed.
3. The logic states of "A", "B", "C", "D", "E" and "H" determine the type of TRANSFER operation performed. See the Write Transfer Cycle Function Table.

SAMa or SAMb SERIAL INPUT



SAMa or SAMb SERIAL OUTPUT



NOTE: $\overline{SE}$a, SCa and SDQa are used when accessing SAMa and $\overline{SE}$b; SCb and SDQb are used when access in SAMb.

TRIPLE PORT DRAM

256K x 8 DRAM WITH DUAL 512 x 8 SAMS

FEATURES

- Three asynchronous, independent, data access ports
- Fast access times – 60ns random, 15ns serial
- Operation and control compatible with 2 Meg VRAMS
- High-performance, CMOS silicon-gate process
- Low power: 15mW standby; 450mW active, typical
- 512-cycle refresh within 8ms
- Refresh modes: $\overline{\text{RAS}}$-ONLY, $\overline{\text{CAS}}$-BEFORE-$\overline{\text{RAS}}$ (CBR) and HIDDEN
- FAST PAGE MODE with Extended Data Out (^{t}PC = 30ns)
- Two bidirectional serial access memories (SAMs)
- Fully static SAMs and Mask Register, no refresh required
- 4,096-bit Transfer Mask Register

SPECIAL FUNCTIONS

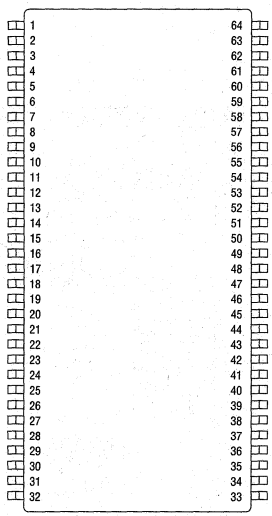
- MASKED WRITE (Write-Per-Bit)
- BLOCK WRITE
- SPLIT READ AND SPLIT WRITE TRANSFERs
- PROGRAMMABLE SPLIT SAMs
- BIT MASKED TRANSFERS
- SERIAL MASK DATA INPUT mode

OPTIONS MARKING

- Timing [DRAM, SAMs (cycle/access)]
  - 60ns, 20ns/15ns - 6
  - 70ns, 25ns/20ns - 7
  - 80ns, 28ns/25ns - 8
- Packages
  - Plastic SOP (550 mil) SG

PIN ASSIGNMENT (Top View)

64-Pin SOP*



*Pinouts to be determined

NEW ■ MULTIPORT DRAM

GENERAL DESCRIPTION

The MT43C256K8A1 is a high speed, triple port CMOS dynamic random access memory (TPDRAM) containing 2,097,152 bits. Data may be accessed by an 8 bit wide DRAM port or by either of two independently-clocked 512 x 8-bit serial access memory (SAM) ports. Data may be transferred bidirectionally between the DRAM and the SAMs.

The DRAM portion of the TPDRAM is functionally identical to the MT4C4256 (256K x 4) DRAM. Sixteen 256-bit data registers make up the serial access memory portions of the TPDRAM. Data I/O and internal data transfer are accomplished using five separate bidirectional data paths; the 8-bit random access I/O port, a pair of internal 2,048 bit wide paths between the DRAM and the SAMs, and the pair of 8-bit serial I/O ports for the SAMs. The rest of the circuitry consists of the control, timing, and address decoding logic.

All three ports may be operated asynchronously and independently of the others except when data is being internally transferred between the DRAM and either SAM.

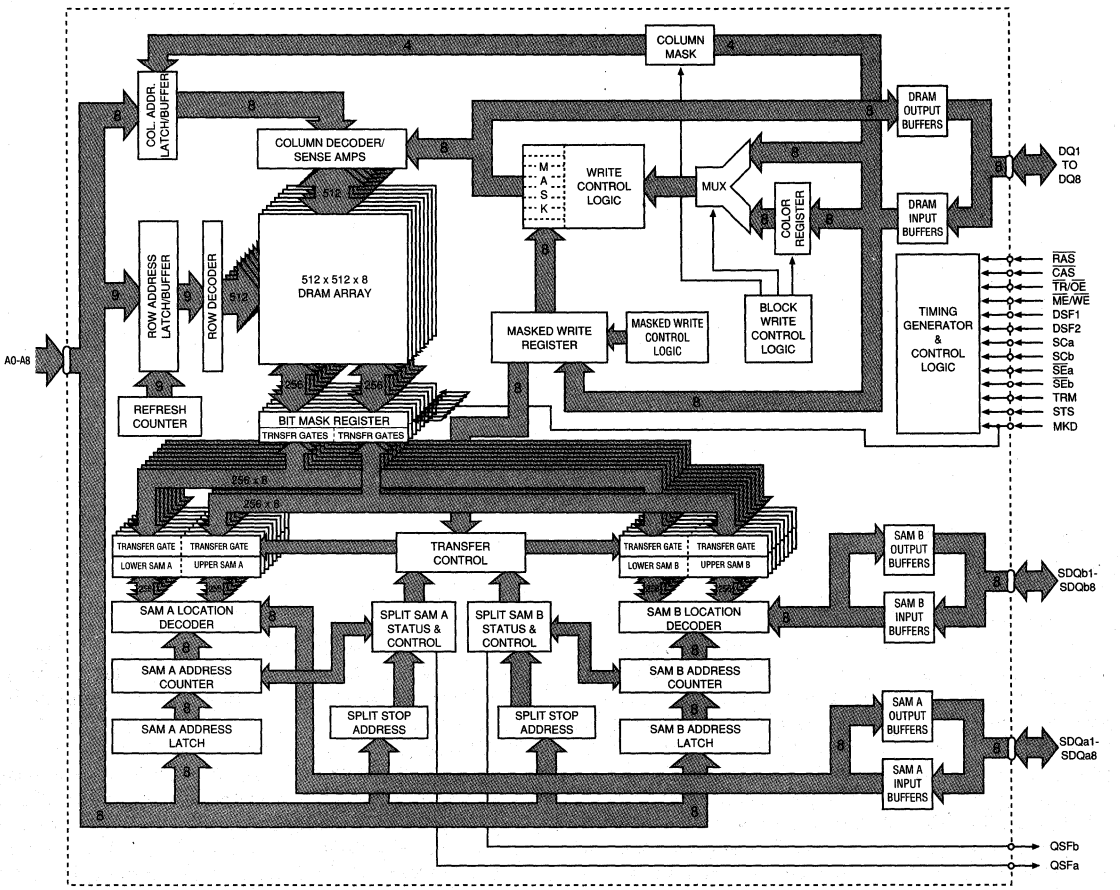
Each of the 4,096 bits involved in an internal transfer may be individually masked by performing a BIT MASKED TRANSFER operation. The 512 x 8-bit, bit mask data register can be parallel loaded from the DRAM or either SAM, or it may be serial loaded through the MKD serial input.

As with all DRAMs, the TPDRAM must be refreshed to maintain data. The refresh cycles must be timed so that all 512 combinations of $\overline{RAS}$ addresses are executed at least every 8ms (regardless of sequence). Micron recommends evenly spaced refresh cycles for maximum data integrity. An internal transfer between the DRAM and either SAM counts as a refresh cycle. The SAM portions of the TPDRAM are fully static and do not require any refresh.

The operation and control of the MT43C256K8A1 are optimized for high performance graphics and communication designs. The triple port architecture is well suited to buffering the sequential data types used in rastor graphics display, video windowing, serial and parallel networking and data communications. Special features, such as SPLIT TRANSFER, BIT MASKED TRANSFERS and BLOCK WRITE allow further enhancements to system performance.

NEW ■ MULTIPORT DRAM

FUNCTIONAL BLOCK DIAGRAM



MICRON TECHNOLOGY, INC.

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TECHNICAL NOTE

MOISTURE ABSORPTION IN PLASTIC PACKAGES

INTRODUCTION

All plastic integrated circuit packages have a tendency to absorb moisture. During surface mount assembly, this moisture can vaporize when subjected to the heat associated with solder reflow operations. Vaporization creates internal stresses that can cause the plastic molding compound to crack. Cracks in the package allow contamination to penetrate to the die and potentially reduce the reliability of the semiconductor device. The cracking process associated with surface-mountable devices is commonly referred to as the "popcorn effect."

Cracks in the plastic pose several reliability concerns. The moisture path to the die is shortened, allowing ion migration or corrosion to occur more readily. Minor cracks, that might not be harmful initially, could propagate with time, resulting in a longer-term functional failure.

Since plastic packages absorb moisture, care must be taken to prevent exposure for any long period prior to surface-mounting the devices on the printed circuit board. If exposed to excessive moisture, the devices should be baked to remove moisture prior to solder reflow operations.

This technical note describes the shipping procedures that ensure Micron customers will receive memory devices that do not exhibit the popcorn effect. It also discusses Micron's recommendations for baking the devices if they are exposed to excessive moisture.

ABSORPTION CHARACTERISTICS

Micron's extensive testing empirically characterizes the moisture absorption characteristics of plastic packages. As the plastic takes on moisture, the weight of the device increases. Micron employs a standard procedure for weighing the device before and after it is exposed to moisture. We calculate the percentage of weight gain to determine the relative efficiency of different packaging techniques used for shipping devices.

MICRON PROCEDURES

Micron has eliminated any chance of having popcorn failures with surface-mount packages by shipping all surface-mount devices in sealed bags containing a desiccant. Devices stored in these bags show no measurable weight gain when subjected to a high humidity environment for long time periods.

DEVICE STORAGE

To prevent device failure due to the popcorn effect, store plastic surface-mount packages carefully before PCB assembly. Micron has run tests on devices that have been exposed to 50 percent humidity outside of their shipping containers for time intervals from six months to one year and no failures have been recorded.

Any concerns about the moisture absorption can be eliminated by storing the devices in Micron's shipping bags. We designed these containers to prevent the passage of water vapor for long periods of time.

DEVICE BAKING

If devices have been removed from their shipping containers and exposed to high levels of moisture, Micron recommends a device bake-out procedure before surface mounting. This bake-out may be accomplished by placing the parts in a tray and baking in an oven for 160 hours at 40° C. Any moisture is driven out of the devices during the exposure to the heat.

Moisture may be removed faster by baking at 100° C for 24 hours.

SUMMARY

1. All plastic packages absorb moisture when exposed to high levels of humidity for long time intervals.
2. Micron devices have not exhibited any popcorn effect when exposed to 50 percent humidity for long time periods.
3. Micron ships all surface-mount packages in containers that prevent absorption of moisture.
4. If devices have been removed from their shipping containers and exposed to excessive moisture, they should be baked before being surface-mounted.

REFERENCES

"Moisture Absorption and Mechanical Performance of Surface Mountable Plastic Packages": Bhattacharyya, B. K. : et. al. : 1988 Proceedings of the 38th Electronics Components Conference.

"Analysis of Package Cracking During Reflow Soldering Process": Kitano, M., et. al. : 26th Annual Proceeding, Reliability Physics, 1988.

"Moisture Induced Package Cracking in Plastic Encapsulated Surface Mounted Components During Solder Reflow Process": Lin, R., et. al. : 26th Annual Proceeding, Reliability Physics, 1988.

TECHNICAL NOTE

TAPE AND REEL PROCEDURES

GENERAL DESCRIPTION

Tape and reel is becoming the packaging and shipment method of choice for Micron's surface-mounted memory devices. Tape and reel minimizes the handling of components by directly interfacing with automatic pick-and-place machines.

Micron supports the Electronic Industries Association's (EIA) standardization of tape and reel specifications number 481A. The intent of this technical note is to describe Micron's status in support of the EIA standard.

Table 1
MICRON TAPE SIZES AND DEVICES PER REEL

COMPONENT	TAPE WIDTH (W) mm	PITCH (P) mm	DEVICES PER 13-INCH REEL
PLCC			
18 Pin	24	12	1,000
52 Pin	32	16	500
SOJ (300 mil)			
20/26 Pin	24	12	1,000
24 Pin	24	12	1,000
28 Pin	24	12	1,000
SOJ (400 mil)			
28 Pin	32	16	500
32 Pin	44	16	500
40 Pin	44	16	500

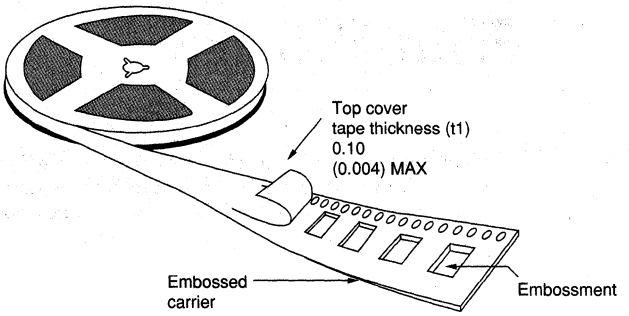


Figure 1
REEL

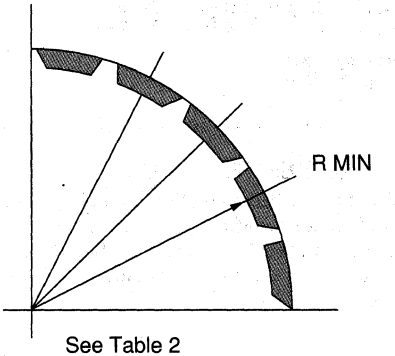
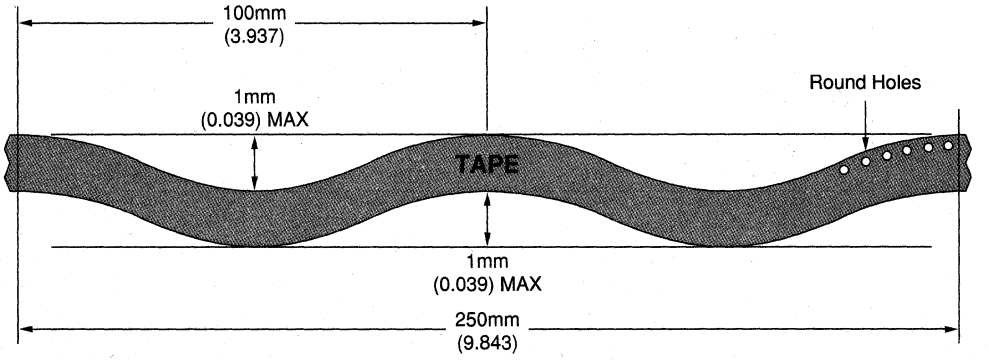


Figure 2
BENDING RADIUS



Allowable camber to be 1mm/100mm nonaccumulative over 250mm.

Figure 3
CAMBER (TOP VIEW)

NEW ■ APPLICATION/TECHNICAL NOTE

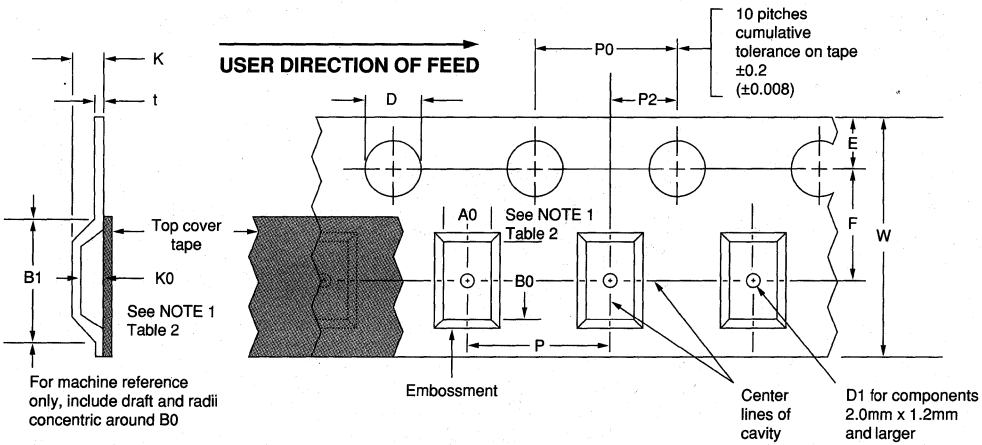


Figure 4
EMBOSSED CARRIER DIMENSIONS
(24mm Tape Only)

Table 2
24mm EMBOSSED TAPE DIMENSIONS [3]

TAPE SIZE	D	E	P0	t (MAX)	A0, B0, K0
24mm	1.5 $^{+0.10}_{-0.00}$ (0.59) $^{+0.004}_{-0.000}$	1.75 (0.069 ±0.004)	4 (0.157 ±0.004)	0.400 (0.16)	NOTE 1

TAPE SIZE	B1 (MAX)	D1 (MIN)	F	K (MAX)	P2	R (MIN)	W
24mm	20.1 (0.791)	1.5 (0.059)	11.5 ±0.10 (0.453 ±0.004)	6.5 (0.256)	2 ±0.10 (0.079 ±0.004)	50 (1.969)	24 ±0.30 (0.945 ±0.012)

TAPE SIZE	P					
	4 ±0.10 (0.157 ±0.004)	8 ±0.10 (0.315 ±0.004)	12 ±0.10 (0.472 ±0.004)	16 ±0.10 (0.630 ±0.004)	20 ±0.10 (0.787 ±0.004)	24 ±0.10 (0.945 ±0.004)
24mm			x	x	x	x

NOTE:
1. A0, B0 and K0 are determined by component size. The clearance between the component and the cavity must be within 0.05 (0.002) MIN to 1.00 (0.039) MAX for 24mm tape. The component cannot rotate more than 20° within the determined cavity.
2. Tape and components shall pass around radius "R" without damage.
3. All dimensions in millimeters (inches).

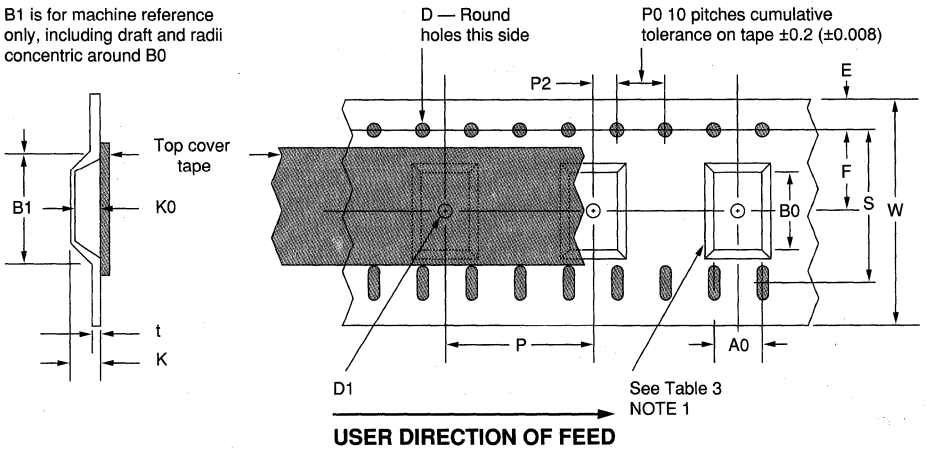


Figure 5
EMBOSSED CARRIER DIMENSIONS
(32 and 44mm Tape Only)

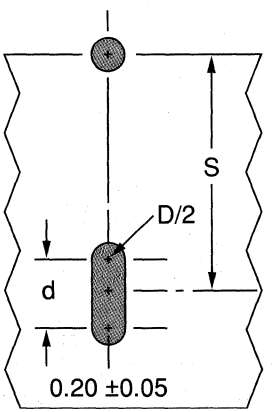


Figure 6
DETAIL ELONGATED HOLE

Table 3
32 AND 44mm EMBOSSED TAPE [3]

TAPE SIZE	D	D1 (MIN)	E	K (MAX)	P0	t (MAX)	A0, B0, K0
32 and 44mm	1.5 $^{+0.10}_{+0.00}$ (0.059) $^{+0.004}_{+0.000}$	2 (0.079)	1.75 ±0.10 (0.069 ±0.004)	10 (0.394)	4 ±0.10 (0.156 ±0.004)	0.500 (0.20)	NOTE 1

TAPE SIZE	B1 (MAX)	F	P2	S	W	R (MIN)
32mm	23 (0.906)	14.2 ±0.10 (0.559 ±0.004)	2 ±0.10 (0.079 ±0.004)	28.4 ±0.10 (1.118 ±0.004)	32 ±0.30 (1.26 ±0.012)	50 (1.973)
44mm	35 (1.378)	20.2 ±0.15 (0.795 ±0.006)	2 ±0.15 (0.079 ±0.006)	40.4 ±0.10 (1.591 ±0.004)	44.8 ±0.30 (1.732 ±0.12)	50 (1.973)

TAPE SIZE	P							
	16 ±0.10 (0.630 ±0.004)	20 ±0.10 (0.787 ±0.004)	24 ±0.10 (0.945 ±0.004)	28 ±0.10 (1.102 ±0.004)	32 ±0.10 (1.26 ±0.004)	36 ±0.10 (1.417 ±0.004)	40 ±0.10 (1.575 ±0.004)	44 ±0.10 (1.732 ±0.004)
32mm	x	x	x	x	x			
44mm			x	x	x	x	x	x

NOTE:
1. A0, B0 and K0 are determined by component size. The clearance between the component and the cavity must be within 0.05 (0.002) MIN to 1.00 (0.039) MAX for 24mm tape. The component cannot rotate more than 20° within the determined cavity.
2. Tape and components shall pass around radius "R" without damage.
3. All dimensions in millimeters (inches).

TECHNICAL NOTE

DRAM POWER-UP AND REFRESH CONSTRAINTS

INTRODUCTION

The JEDEC 4 Meg DRAM introduces two potential incompatibilities compared to the previous generation 1 Meg DRAM. The incompatibilities involve refresh and power-up. Understanding and addressing these incompatibilities and providing for them will offer designers and system users greater compatibility between the 1 Meg and 4 Meg.

REFRESH

The most commonly used refresh mode of the 1 Meg is the $\overline{CAS}$-BEFORE-$\overline{RAS}$ (CBR) REFRESH cycle. The CBR for the 1 Meg specifies the $\overline{WE}$ pin as a "don't care." The 4 Meg, on the other hand, specifies the CBR REFRESH mode with the $\overline{WE}$ pin held at a voltage HIGH level.

A CBR cycle with $\overline{WE}$ LOW will put the the 4 Meg into the JEDEC-specified test mode (WCBR). In contrast, the 1 Meg test mode is entered by applying a HIGH signal to the test pin (pin 4 on DIPs, pin 5 on SOJs and pin 8 on ZIPs). This HIGH signal is usually a "super voltage" (Vin ≥ 7.5V), so normal TTL or CMOS HIGH levels will not cause the part to enter the test mode.

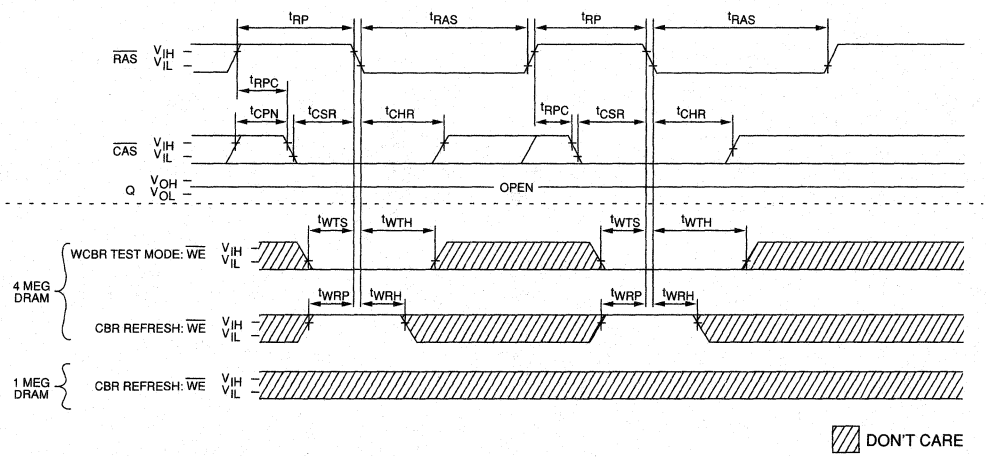
POWER-UP

The 4 Meg JEDEC test mode constraint may introduce another problem. The 1 Meg POWER-UP cycle requires a 100µs delay followed by any eight $\overline{RAS}$ cycles. The 4 Meg POWER-UP is more restrictive in that eight $\overline{RAS}$-ONLY REFRESH or CBR REFRESH ($\overline{WE}$ held HIGH) cycles must be used. The restriction is needed since the 4 Meg may power-up in the JEDEC-specified test mode and must exit out of the test mode. The only way to exit the 4 Meg JEDEC test mode is with either a $\overline{RAS}$-ONLY or a CBR REFRESH cycle ($\overline{WE}$ held HIGH).

SUMMARY

The 1 Meg and 4 Meg are compatible, with the following exceptions:

1. For standard test mode, the 1 Meg requires a vaild HIGH on the test pin while the 4 Meg requires a CBR cycle with $\overline{WE}$ LOW.
2. The 1 Meg CBR REFRESH allows the $\overline{WE}$ pin to be a "don't care" while the 4 Meg CBR requires $\overline{WE}$ to be HIGH.
3. The eight $\overline{RAS}$ wake-up cycles on the 1 Meg may be any valid $\overline{RAS}$ cycle while the 4 Meg may only use $\overline{RAS}$-ONLY REFRESH or CBR REFRESH cycles ($\overline{WE}$ held HIGH).



COMPARISON OF 4 MEG TEST MODE AND WCBR TO 1 MEG CBR

APPLICATION/TECHNICAL NOTE

TECHNICAL NOTE

MT4C1664 AND MT4C1665 COMPATIBILITIES

INTRODUCTION

Micron provides the 64K x 16 DRAM in two versions: MT4C1664 and MT4C1665. The MT4C1664 has two $\overline{WE}$ pins which allow for BYTE-WRITE cycles. It does not support WRITE-PER-BIT. The MT4C1665 has one $\overline{WE}$ pin and offers nonpersistent, WRITE-PER-BIT (MASKED WRITE) cycles.

COMPATIBILITY

The MT4C1664 and MT4C1665 may be used interchangeably, provided precautions are taken. The memory system may not utilize the WRITE-PER-BYTE feature of the MT4C1664 or the WRITE-PER-BIT feature of the MT4C1665 in order to maintain interchangeability.

At the system level, a special timing constraint exists. $\overline{WE}$ must be held HIGH when $\overline{RAS}$ transitions from HIGH to LOW (preventing the MT4C1665 from performing WRITE-PER-BIT cycles). The two $\overline{WE}$ traces must be connected together (pins 12 and 13 on SOJ or pins 22 and 23 on ZIP) in order to ensure that all 16 bits will be written on the MT4C1664.

The MT4C1664 and MT4C1665 are now interchangeable. The MT4C1664 will have twice the capacitive load on the write enable signal as the MT4C1665 due to its two $\overline{WE}$ pins. Its $\overline{WE}$ timing will be a "don't care" when $\overline{RAS}$ transitions from HIGH to LOW. The MT4C1665 will enter a WRITE-PER-BIT cycle if $\overline{WE}$ is LOW when $\overline{RAS}$ transitions from HIGH to LOW.

The MT4C1665 can provide the BYTE-WRITE capability of the MT4C1664 by allowing the mask register to be enabled by bytes. However, this may not be practical since it requires additional circuitry.

SUMMARY

An application that performs 16-bit word writes will allow either the MT4C1664 or MT4C1665 to be used. The MT4C1664 must have both $\overline{WE}$ pins connected, doubling capacitance on the write enable signal, but its timing is a "don't care" when $\overline{RAS}$ goes LOW. On the other hand, the MT4C1665 has only one $\overline{WE}$ for lower capacitance, but $\overline{WE}$ must always be held HIGH when $\overline{RAS}$ transitions from HIGH to LOW (refer to Note 1).

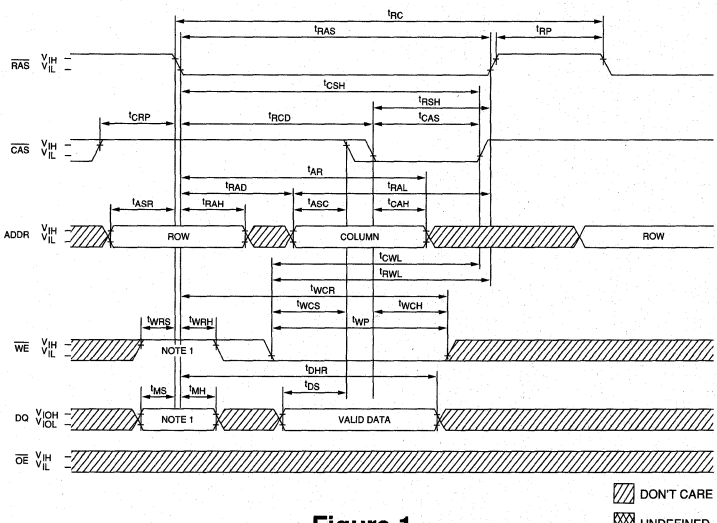


Figure 1
MT4C1665 TIMING CONSTRAINTS

NOTE: 1. Applies to MT4C1665 only. The MT4C1664 specifies these as "don't cares" during this portion of operation.

APPLICATION/TECHNICAL NOTE

TECHNICAL NOTE

MT4C1664: 256 KILOBYTE MEMORY SYSTEM WITH FOUR RAS LINES

INTRODUCTION

Micron's MT4C1664 64K x 16 DRAM is a great solution for replacing 64K x 4 DRAMs in VGA systems. For a 256 kilobyte (KB) memory system, two MT4C1664s replace eight 64K x 4 DRAMs, resulting in improved reliability and performance margins, decreased power consumption, reduced costs and board savings, while maintaining state-of-the-art technology.

This application note shows how the MT4C1664 may be interfaced with a 256KB memory system using four RAS controls and EARLY-WRITE cycles (OE grounded). Reference to the MT4C1664 data sheet will be helpful in understanding how the MT4C1664 functions. The schematic in Figure 1 shows 256KB memory systems using four RAS controls and EARLY-WRITE cycles and how memory is implemented with both the MT4C1664 and 64K x 4 DRAMs.

The same schematic for the MT4C1664 may also be used in systems using LATE-WRITE cycles (OE controlled).

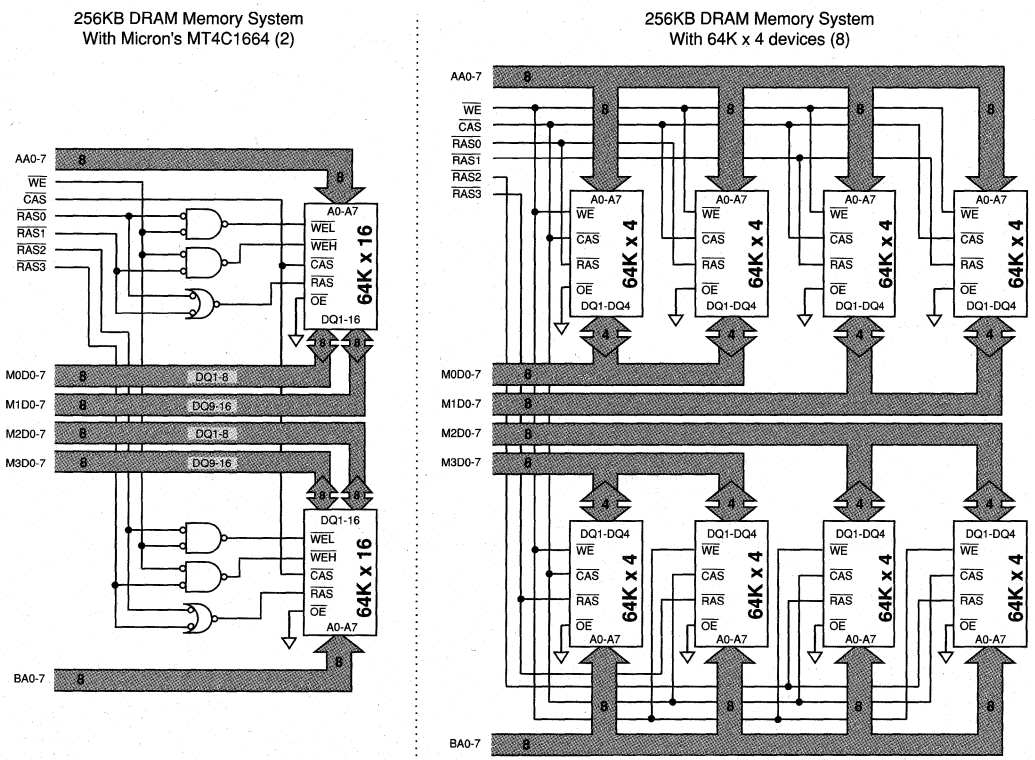


Figure 1
256KB EARLY-WRITE MEMORY

APPLICATION/TECHNICAL NOTE

TECHNICAL NOTE

MT4C1664: 256 KILOBYTE MEMORY SYSTEM WITH FOUR CAS LINES

INTRODUCTION

Micron's MT4C1664 64K x 16 DRAM is a great solution for replacing 64K x 4 DRAMs in VGA systems. For a 256 kilobyte (KB) memory system, two MT4C1664s will replace eight 64K x 4 DRAMs, resulting in improved reliability and performance margins, decreased power consumption, reduced costs and board savings, while maintaining state-of-the-art technology.

This application note shows how the MT4C1664 may interface with a 256KB memory system using four CAS controls and EARLY-WRITE cycles (OE grounded). Reference to the MT4C1664 data sheet will be helpful in understanding how the MT4C1664 functions. The schematic in Figure 1 shows 256KB memory systems using four CAS controls and EARLY-WRITE cycles and how memory is implemented with both the MT4C1664 and 64K x 4 DRAMs.

The same schematic for the MT4C1664 may also be used in systems using LATE-WRITE cycles (OE controlled), except Note 1 no longer applies and the two delay paths may be equal.

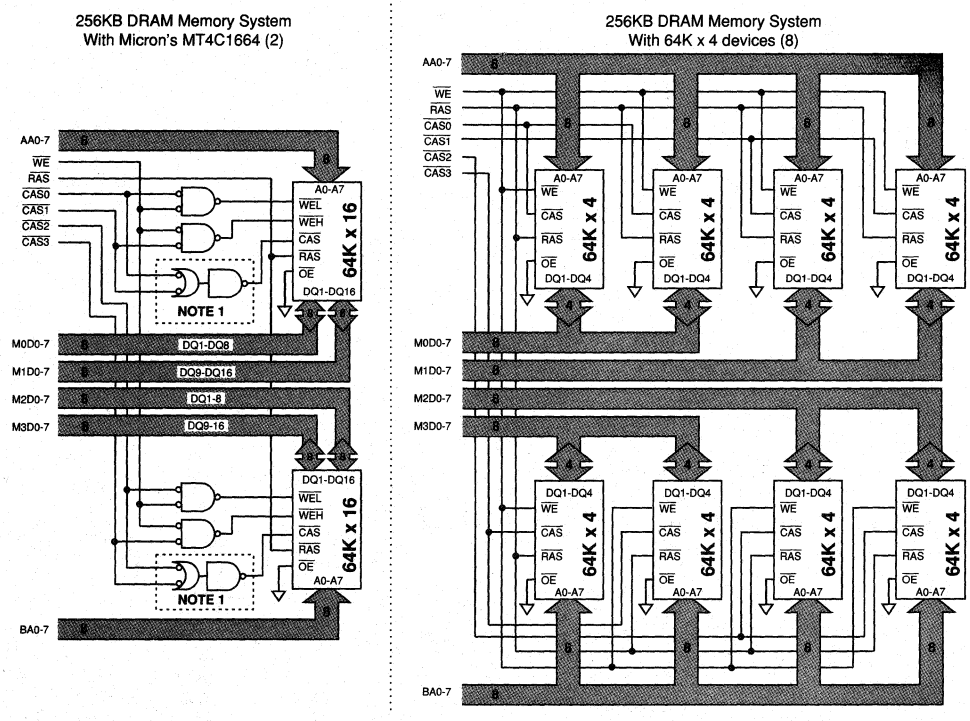


Figure 1
256KB EARLY-WRITE MEMORY

NOTE: 1. This delay path needs to be slightly longer than the two NAND gates to ensure the WE to CAS setup time is met. This will guarantee the DRAM will always be in EARLY-WRITE during WRITE cycles.

APPLICATION/TECHNICAL NOTE

TECHNICAL NOTE

DRAM OE CONTROLLED LATE-WRITE CYCLES

INTRODUCTION

There are three cycles available to write to a DRAM: EARLY-WRITE cycles, READ-MODIFY-WRITE cycles and LATE-WRITE cycles. The industry standard definitions for DRAM WRITE cycles are fairly consistent for both the EARLY-WRITE and READ-MODIFY-WRITE cycles. An exception exists for the "LATE-WRITE" cycle.

COMMON DQ DRAM (x4, x8, etc.)

A LATE-WRITE cycle is a READ-MODIFY-WRITE (see Figure 1) except that the READ portion is not utilized. This is accomplished by keeping the output enable pin (OE) HIGH throughout the cycle. The timing parameters ^{t}RWD, ^{t}AWD and ^{t}CWD no longer apply since OE is HIGH.

This condition may be viewed as an EARLY-WRITE with ^{t}WCS "sliding" past the CAS time and violating the 0ns setup time (WE going LOW prior to CAS going LOW). But, since the output buffers are not being used (OE is HIGH), ^{t}WCS and ^{t}CWD are no longer required.

If WE transitions LOW after CAS transitions LOW, do not bring OE LOW (a noise spike may occur), as the output buffers could turn on and cause contention with the data bus, which could corrupt input data.

The term used for such a WRITE cycle varies throughout the industry. The use of "OE controlled WRITE," "Delayed WRITE" and "LATE-WRITE" all signify the same WRITE cycle described.

SPLIT D AND Q DRAM (x1)

A LATE-WRITE cycle is a READ-MODIFY-WRITE, except the READ portion is not guaranteed and the D and Q pins are separate paths (D and Q cannot be connected together). This is accomplished by ignoring the timing parameters ^{t}RWD, ^{t}AWD and ^{t}CWD.

This condition can be viewed as an EARLY-WRITE with ^{t}WCS "sliding" past the CAS time and violating the 0ns setup time (WE going LOW prior to CAS going LOW). But, since the output buffers are "don't care," ^{t}WCS and ^{t}CWD are no longer required.

This cycle is not available on applications that have the D and Q connected together, as the output will contend with the input.

SUMMARY

A LATE-WRITE cycle is most useful on common DQ DRAMs. Use caution to ensure the output enable pin is properly controlled.

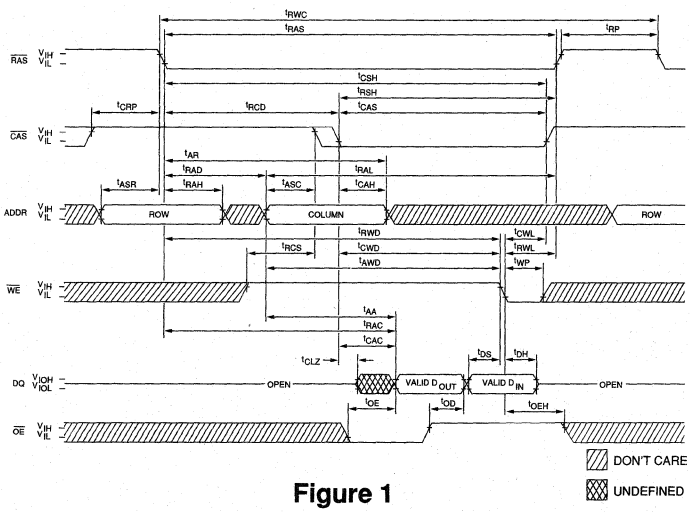


Figure 1
READ-MODIFY-WRITE (MULTIPLE DQ) TIMING

APPLICATION/TECHNICAL NOTE

TECHNICAL NOTE

DRAM TIMING PARAMETERS

INTRODUCTION

A DRAM has many timing parameters, which are specified to help the memory designers define memory system timing. These parameters may be separated into several groups. This note separates these parameters as core parameters (COP) or calculated parameters (CAP).

The calculated parameters are tested by Micron prior to shipment. In cases where the summation of COP parameters is larger than the CAP parameter specification, the CAP parameter overrides the summation of COP parameters. Additionally, if an incoming test is required, the testing of the COP parameter is typically sufficient since CAP parameters are simply combinations of COP parameters.

The CAP parameters are listed below, showing how they are calculated. This will aid the memory designer's understanding of the parameters affected when a COP parameter is altered. Additionally, during testing of the COP parameters, the CAP parameters are also tested by default.

^tRC	=	$^tRAS + ^tRP + 2^tT$
^tPC	=	$^tCPA + ^tT$ or $^tCP + ^tCAS + 2^tT$
^tAR	=	^tRCD (MAX) + ^tCAH
^tRSH	≈	^tCAS
^tCSH	=	$^tCAS + ^tRCD$ (MAX)
^tCPA	=	$^tAA + ^tT$
^tAA	≈	$^tRAS/2$
^tDHR	=	^tRCD (MAX) + ^tDH
^tWCH	=	$^tWP - ^tWCS - ^tT$
^tWCR	=	^tRCD (MAX) + ^tWCH
^tRAD (MIN)	=	$^tRAH + ^tT$
^tRAD (MAX)	=	$^tRAC - ^tAA$
^tRCD (MIN)	=	$^tRAD + ^tASC + ^tT = ^tRAH + ^tASC + 2^tT$
^tRCD (MAX)	=	$^tRAS - ^tRSH$
^tRWD (x1)	=	^tRAC
^tRWD (x4)	=	$^tRAC + ^tOD + 2^tT + ^tDS$
^tCWD (x1)	=	^tCAC
^tCWD (x4)	=	$^tCAC + ^tOD + 2^tT + ^tDS$
^tAWD (x1)	=	^tAA
^tAWD (x4)	=	$^tAA + ^tOD + 2^tT$
^tRWC (x1)	=	$^tRWD + ^tRWL + ^tRP + 2^tT$
^tRWC (x4)	=	$^tRAC + ^tRWL + ^tRP + 4^tT + ^tOD + ^tDS$
^tPRWC (x1)	=	$^tCPA + ^tCWL + 2^tT + ^tDS$
^tPRWC (x4)	=	$^tCPA + ^tCWL + 4^tT + ^tOD + ^tDS$

TECHNICAL NOTE

LPDRAM BBU CURRENT VS. $\overline{\text{RAS}}$ ACTIVE TIME (1 MEG)

INTRODUCTION

One of the most significant features of the low power, extended refresh DRAM (LPDRAM) is its BATTERY BACKUP (BBU) cycle. BBU is essentially a CAS-BEFORE-RAS (CBR) REFRESH at an extended refresh rate of 125µs per cycle.

$\overline{\text{RAS}}$ pulse width (^{t}RAS) affects the BBU current and should be considered when designing a low power system. The longer $\overline{\text{RAS}}$ is held LOW, the more current an LPDRAM will consume while in the BBU mode. Therefore, keeping ^{t}RAS at a minimum will maximize power savings.

Figure 1 shows a typical curve of Micron's 1 Meg LPDRAM (MT4C4256L and MT4C1024L) showing the relationship between its BBU standby current and the width of ^{t}RAS. The 25°C curve has a slope of 4.8µA increase for every additional 1µs $\overline{\text{RAS}}$ is held LOW. The 70°C curve has a slope of 4µA increase for every additional 1µs $\overline{\text{RAS}}$ is held LOW.

SUMMARY

The ^{t}RAS time should be kept as short as possible when the memory array is being designed. This will result in lower standby currents, especially with the BBU cycle.

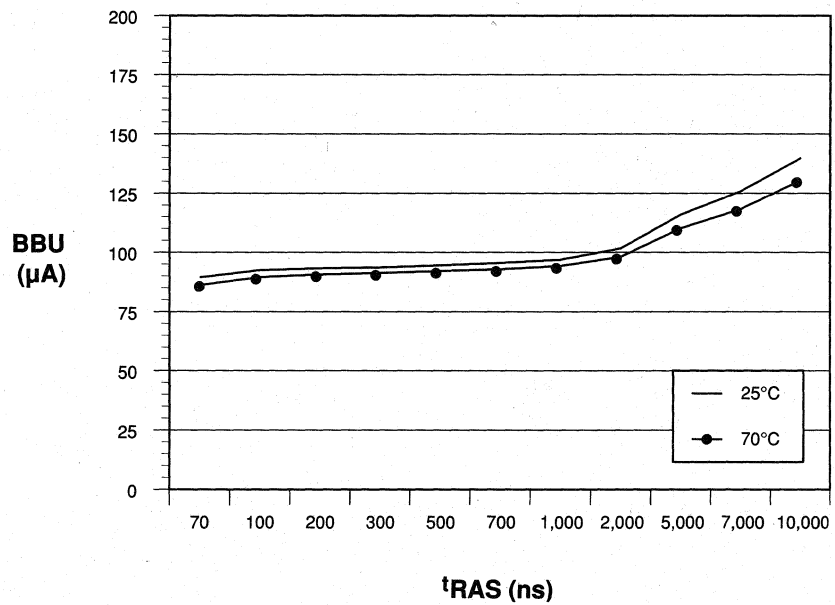


Figure 1
TYPICAL BBU CURRENT AS A FUNCTION OF ^{t}RAS

NEW APPLICATION/TECHNICAL NOTE

TECHNICAL NOTE

LPDRAM BBU CURRENT VS. $\overline{\text{RAS}}$ ACTIVE TIME (4 MEG)

INTRODUCTION

One of the most significant features of the low power extended refresh DRAM (LPDRAM) is its BATTERY BACKUP (BBU) cycle. BBU is essentially a CAS-BEFORE-RAS (CBR) REFRESH at an extended refresh rate of 125µs per cycle.

$\overline{\text{RAS}}$ pulse width (^{t}RAS) affects the BBU current and should be considered when designing a low power system. The longer $\overline{\text{RAS}}$ is held LOW, the more current an LPDRAM will consume while in the BBU mode. Therefore, keeping ^{t}RAS at a minimum will maximize power savings.

Figure 1, a typical curve of Micron's second generation 4 Meg LPDRAM (MT4C4001L and MT4C1004L), shows the relationship between its BBU standby current and the width of ^{t}RAS. The 25°C curve has a slope of 79µA increase for each additional 1µs $\overline{\text{RAS}}$ that is held LOW. The 70°C curve has a slope of 70µA increase for each additional 1µs that $\overline{\text{RAS}}$ is held LOW.

SUMMARY

The ^{t}RAS time should be kept as short as possible when designing memory array timing. This will result in lower standby currents, especially for the BBU cycle.

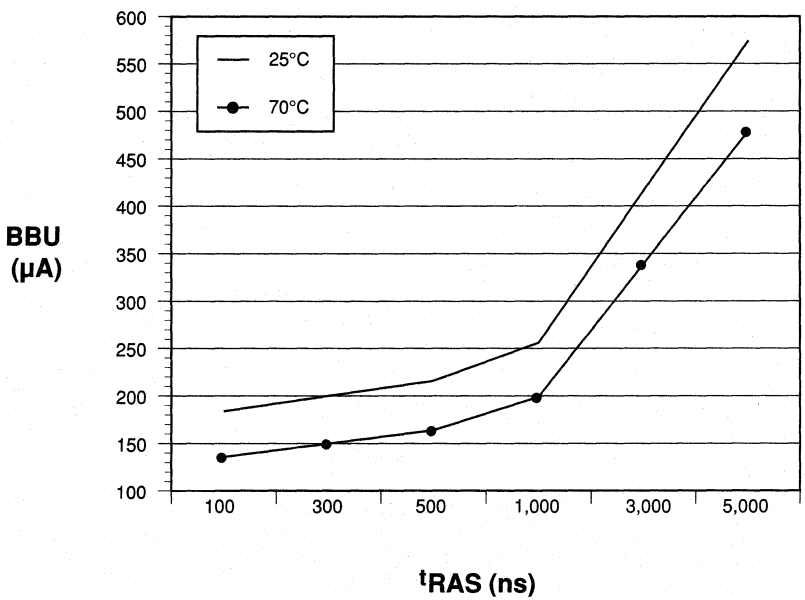


Figure 1
TYPICAL BBU CURRENT AS A FUNCTION OF ^{t}RAS

NEW ■ APPLICATION/TECHNICAL NOTE

TECHNICAL NOTE

LOW-VOLTAGE (3V) DRAM DESIGN ISSUES

INTRODUCTION

Laptop and notebook personal computer markets demand low-voltage memories. This is in direct response to the consumer's demand for portable PCs with longer battery life. To help meet this demand, Micron introduced the industry's first 3.3V 1 Meg DRAM.

The introduction of low-voltage DRAMs, raised design concerns regarding the migration from 5V systems to 3.0, 3.3 and 3.3/5.0V systems. Several issues must be considered prior to selecting DRAM memory for low-voltage PC systems:

- Voltage limits
- Speed
- I/O levels
- Mixed/dual voltages
- Soft error rates (SERs)

VOLTAGE LIMITS

During the development phase of low-voltage DRAMs, manufacturers are expected to introduce offerings in four different voltage ranges:

- 3.3V ±5% (interim)
- 3.0V ±10%
- 3.3V ±10%
- 2.7V to 3.6V

The 3.3V ±5% version is the first available low-voltage DRAM. This is generally an enhanced version of existing 5V DRAMs specially processed for 3.3V operation. Micron is able to offer 3.3V ±5% 1 Meg and 4 Meg DRAMs because Micron uses a leading-edge DRAM process. This type of low-voltage DRAM works reliably in mixed/dual voltage systems and offers early availability for 3.3V system development.

The other versions are manufactured with a low-voltage-only CMOS process and are commonly referred to as 3V-only DRAMs. Micron's 3V-only DRAMs are being developed to operate over the 2.7V to 3.6V voltage range (fourth version). This will provide either 3.0V ±10% or 3.3V ±10% operation from the same DRAM. Devices manufactured with the low-voltage CMOS process are optimized for both high-speed and low-power performance at low voltages.

The 3V-only process limits the allowed maximum Vcc stress to the DRAM at 4.6V. Any violation of this maximum specification can damage the DRAM. Careful review of this parameter is necessary prior to selecting a low-voltage DRAM.

The Micron device part number indicates one of the two process groups for low-voltage DRAMs. "C" designates 3.3V CMOS, while "LC" designates 3V-only low-voltage CMOS processing. For example, the 3.3V 1 Meg DRAM (256K x 4) is an MT4C4256 VL, which allows a 6V maximum Vcc stress. Although Micron has no plans to introduce a 3V-only 256K x 4 DRAM, the device would be a MT4LC4256 L if it were developed and introduced to the market. Additionally, Micron data sheets specify the maximum Vcc stress rating for a given DRAM.

SPEED

The most significant advantage of a 3V-only DRAM is that it will have similar speeds to that of a 5V DRAM operating at 5V, 60ns to 70ns. The interim 3.3V DRAMs will achieve only 100ns, but will achieve speeds in the range of 60 to 80ns when operating at 5V.

Micron's MT4C4256 VL timing parameters are tested for a 3.3V ±5% operation. Although the device is not tested at 5V, characterization data shows the 3.3V 1 Meg DRAM will achieve 70ns or better when operating at 5V.

I/O LEVELS

The interim 3.3V DRAM has an I/O level issue. Since these devices are designed for 5V operation, the trip points will change when the DRAM is operating at 3.3V. In particular, VIL and VOH noise immunity guardbands are reduced and will be less forgiving than when they were at 5V. Since the variances are device specific, consulting the device's data sheet prior to design is recommended.

On the other hand, 3V-only DRAMs do not have I/O level issues. The device and process are designed for optimum drive levels and trip points at 3.3V. It is worth noting that the JEDEC 3.3V output specification states one TTL load rather than two TTL loads.

MIXED/DUAL VOLTAGES

Some of the first and second generation low-voltage systems may require the ability of both 3.3V and 5V operation. This would offer 3.3V operation for low power consumption while in the portable mode and faster speeds when plugged in to a power source such as at the desk or in the car. This application will be supported by the interim 3.3V DRAM, since it allows both 3.3V and 5V operation.

An important issue to consider in a mixed/dual voltage system is the switching of the Vcc power supply level. A DRAM will experienced what is referred to as a "Vbump" when the Vcc level changes. This occurs when the data is stored in the memory cell at a certain level and is read out (internally) at a different level due to a shift in the Vcc level. Switching the Vcc from 3.3V to 5.0V results in a severe "bump" and can corrupt the data stored in the DRAM memory cells.

The system designer has two alternatives when developing a system that will operate with mixed/dual voltages. The first is to require that all the contents of DRAM-based memory be saved (usually onto disk memory) prior to changing the power supply level, then restore the DRAM-based memory once the power-supply levels have been changed.

The second alternative is to increase the power supply in increments with the DRAM memory being completely refreshed at each interval. Ideally, the largest increment Vcc should be raised is no more than the difference between the maximum Vcc limit and the minimum Vcc limit. In the case of the 3.3V ±5% DRAM, Vcc should not increase by more than 300mV at a time. The Micron MT4C4256 VL, on the other hand, can accommodate up to a 1V step.

For example, starting at 3.3V, increase Vcc to 4.2V, then perform a complete set of refresh cycles. After the refresh is complete, raise the Vcc level to 5.0V and perform another complete set of refresh cycles. After the second refresh is complete, the DRAM memory will be ready for 5V operation.

If an application requires the DRAM's Vcc power to come from a different reference level than the input and/or output busses, the I/O pin reference levels must not exceed the Vcc reference levels by more than 1V, unless specified less by the data sheet. Exceeding this can cause the DRAM to either initiate the DRAM manufacturer's internal test mode or cause excessive leakage on the output pins.

SOFT ERROR RATES

A disadvantage with operating interim 3.3V DRAMs at 3.3V rather than at 5.0V is the increased susceptibility of the DRAM to soft errors. Preliminary SER data taken on the interim 3.3V 1 Meg DRAM shows diverging results. Real-time SER data shows no difference between 5V and 3.3V operation. Yet, accelerated SER data shows an increase in soft errors going from 5V to 3.3V operation. Additionally, SER will vary widely between vendors as the design and process employed determine the soft error susceptibility.

Until the SER divergence is well understood, Micron is recommending its interim 3.3V DRAMs be used for the PC-related memory market (low number of units per system). Micron discourages the use of its interim 3.3V DRAMs in memory-intensive systems that require hundreds of DRAMs. The 3V-only DRAM, on the other hand, should not experience an increase in SER and is an excellent choice for low-voltage memory in memory-intensive systems.

TECHNICAL NOTE

MT43C4257/MT43C4258 COMPARISON

INTRODUCTION

Micron Technology, Inc., offers its Triple Port DRAM (TPDRAM) in two versions. The MT43C4257 supports the JEDEC split SAM status function (QSF) pin as defined for VRAMs. The MT43C4258 supports a variation of the QSF function called the split SAM special function (SSF) input function. Other than this difference, the function and performance of the two devices are identical.

MT43C4257 — QSF OUTPUT

The QSF output pin of the MT43C4257 is identical in function to the QSF pin of the MT42C4255 256K x 4 VRAM. The QSF output pin indicates which half of the SAM is being accessed. When data is accessed from the lower half, the QSF is LOW; when data is accessed from the upper half, QSF is HIGH (see Figure 1). When using the MT43C4257 or any standard VRAM in the split SAM mode, the transition between SAM halves occurs only when the SAM-half boundary is reached by the address pointer. This is address count 255 for the lower half and 511 for the upper half. When this boundary is reached, the new Tap address for the next SAM-half is loaded ("X" for the lower, "Y" for the upper). The following SC will access data from the new half.

MT43C4258 — SSF INPUT

The MT43C4258 introduces functionality to the TPDRAM that is not available on standard VRAMs. The "QSF" pin as an input (SSF) offers a higher degree of design flexibility to the system engineer. The SSF applies only to split transfer cycles. It allows access to be switched from one half of the SAM to the other at will. If SSF is HIGH at the rising edge of the serial clock, the split SAM access will be switched to the other half of the SAM (see Figure 2).

By taking SSF HIGH for the rising edge of a serial clock (location "A" for the lower half, "B" for the upper), the access from the current half may be terminated. Data from this clock will appear on the outputs when in serial output mode or will be written if in serial input mode.

The next serial clock will access data at the new Tap address ("X" for the lower, "Y" for the upper) of the next half. The SSF input acts as a "stop address" input so the

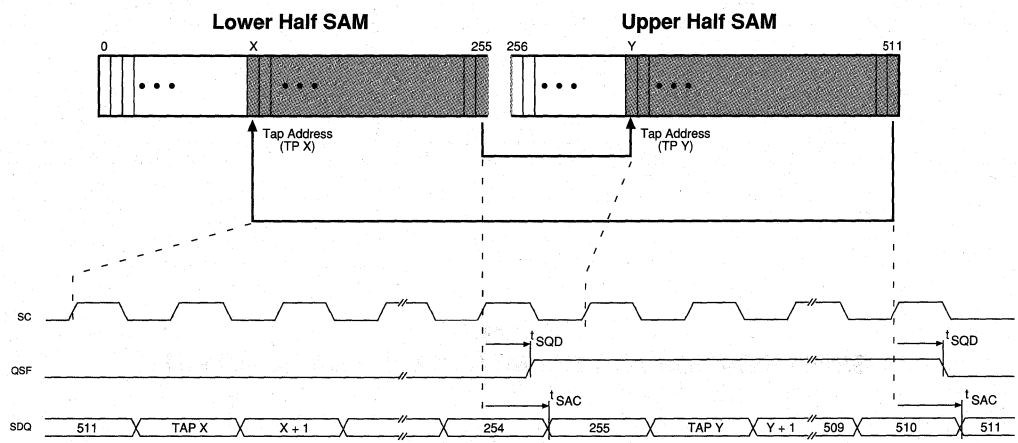


Figure 1
QSF OPERATION FOR THE MT43C4257 (SERIAL OUTPUT)

designer can "force" the access from one half to the next when desired. When operating in the split SAM mode, this option allows different sized "blocks" of data to be input or output from the SAM half regardless of the Tap address and stop point. This feature is useful when performing pans, zooms and scrolling in video-graphics systems and for handling distinct packet sizes in networking or controller applications.

SUMMARY

The only difference between the MT43C4257 and MT43C4258 is the variance in the functionality of the "QSF" pin. The MT43C4258 SSF input pin allows more efficient handling, and therefore higher throughput, of input or output data in either SAM. This improves the performance of video-graphics and networking systems by providing high clock speed and no latency time between reaching the stop point of valid data in one half and the loading of the new Tap address for the next half.

The SSF functionality is also available on the x8 versions of the TPDRAM, the MT43C8128 (QSF) and MT43C8129 (SSF). Refer to the data sheets for detailed timing and functional descriptions.

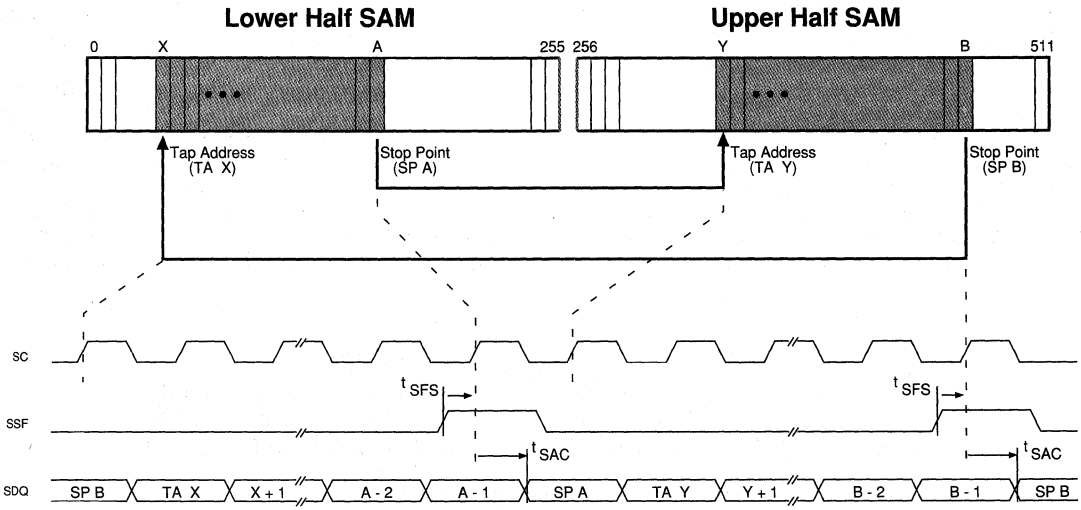


Figure 2
SSF OPERATION FOR THE MT43C4258 (SERIAL OUTPUT)

APPLICATION/TECHNICAL NOTE

TECHNICAL NOTE

88-PIN IC DRAM CARDS

INTRODUCTION

Just as SIMMs began a new period in memory placement and packaging in the 1980s, the 88-pin IC DRAM card promises to have an equal impact on the industry in the 1990s. The 88-pin IC DRAM card combines the architecture of a SIMM with an IC memory card form factor to create a high density, easy-to-use memory device. No longer do end-users have to disassemble their systems and risk ESD damage to add more SIMM modules or memory boards. Finally, a convenient, sensible, and rugged approach to memory packaging has arrived.

For engineers, Micron's 88-pin IC DRAM cards offer a significant improvement in the way system designers manage main and add-in memory. IC DRAM memory cards require less system interface logic, they pack more memory into a given area than SIMM modules and they are better able to withstand use and abuse than contemporary memory upgrade schemes. All this functionality is contained in a convenient, portable, and standardized package.

Standards for the 88-pin IC DRAM card have been jointly ratified by the three major standard-setting bodies: PCMCIA, JEDIA and JEDEC. As a companion to the 68-pin IC memory card, or by itself, the 88-pin IC DRAM card will enhance your product design or offerings.

IC DRAM cards provide a robust, rigid and durable enclosure for the printed circuit board and memory devices contained within. The card's physical dimensions are 2.126 ±0.004 inches wide by 3.37 ±0.004 inches long by 0.129 ±0.004 inches thick, which is about the same dimension as a credit card though three times its thickness.

Once assembled, the strength of the IC DRAM card surpasses that of SIMM modules. Moreover, since the card's components are not subjected to direct physical contact by the user, it can withstand casual, even abusive, handling much better than a SIMM module. When a SIMM module is installed, removed or transported, there is a risk of inflicting damage due to electrostatic discharge. The card is made with a conductive plastic that allows static charges to be safely dissipated to the ground pins via a High-Z path.

IC DRAM cards are designed to ease facilitation. Though the IC DRAM cards appear to function like 72-pin SIMM modules, significant differences favor the IC DRAM card. For example, the IC DRAM card provides its own buffering for its control lines, relieving the system board. Furthermore, buffering enhances system performance, both from noise reduction and reduced capacitive loading of the control lines.

The IC DRAM cards are preferable to SIMMs in small profile notebook and palmtop computers, because the cards offer a twofold improvement in board area usage. Proper choice of receptacle connector for the system board provides the ability for hot insertion or removal, which is impossible for a SIMM module. And the IC DRAM card's size and ruggedness make it ideal for mainframe or industrial applications.

Table 1
MEMORY ADDRESS RANGE

	MEMORY ADDRESS RANGE					
	Presence Detect Bits					Total Memory Size
DRAM Address Space Per Bank	PD1	PD2	PD3	PD4	PD5 = 0	PD5 = 1
no card installed	1	1	1	1	n/a	n/a
256K	0	0	0	0	1MB	2MB
512K	1	0	0	0	2MB	4MB
1 Meg	0	1	0	0	4MB	8MB
2 Meg	1	1	0	0	8MB	16MB
4 Meg	0	0	1	0	16MB	32MB
8 Meg	1	0	1	0	32MB	64MB
16 Meg	0	1	1	0	64MB	128MB

PRESENCE DETECT DEFINITIONS FOR THE 88-PIN IC CARD

It is necessary to clarify the presence detect definitions for the 88-pin IC DRAM cards. The eight presence detect pins are divided into four groups, consisting of memory size (4 bits), number of DRAM banks (1 bit), DRAM access timing (2 bits) and refresh control (1 bit). As shown in Table 1, presence detect bits are defined as 0 = ground, 1 = open.

Presence detect bits PD1, PD2, PD3 and PD4 relate to the byte size of the card or its memory address range. The PD5 presence detect indicates the number of memory banks present on the card. The card will be provided with either 1 or 2 banks (32-, 36- and 40-bit versions) or 2 or 4 banks (16- and 18-bit versions).

For 32-, 36- and 40-bit applications, PD5's definition relates to whether one or two banks are present. Each bank is defined by 2 $\overline{RAS}$ lines. In other words, both $\overline{RAS}$ lines should be activated simultaneously for a 32-, 36- or 40-bit word access. When PD5 = 0, there is one bank present, activated by $\overline{RAS0}$ and $\overline{RAS2}$. When PD5 = 1, there are two banks present. Bank 1 is activated by $\overline{RAS0}$ and $\overline{RAS2}$ while bank 2 is activated by $\overline{RAS1}$ and $\overline{RAS3}$.

For 16- or 18-bit applications, PD5's definition relates to whether 2 or 4 banks are present. Each bank is defined by a single $\overline{RAS}$ lines. When PD5 = 0, two banks are present, activated by $\overline{RAS0}$ and $\overline{RAS2}$. When PD5 = 1, two additional banks are present, activated by $\overline{RAS1}$ and $\overline{RAS3}$. A logical progression within the system's address space would be $\overline{RAS0}$, $\overline{RAS2}$, $\overline{RAS1}$ and $\overline{RAS3}$ in that order. For a 36-bit data bank interpreted as an 18-bit card, $\overline{RAS}$ relates to the data bus as shown in Table 2.

The PD6 and PD7 presence detects indicate the access time of the card from $\overline{RAS}$ true to data out. They are defined in Table 3.

The PD8 presence detect is related to the refresh type of the card, either auto-refresh when PD8 = 0, or a 125 µs per row refresh rate when PD8 = 1. Presently all DRAM cards will leave PD8 open, indicating that the system should provide refreshing, preferably a $\overline{CAS}$-BEFORE-$\overline{RAS}$ type of refresh. This allows an address-independent refresh, which allows interchangeability among different card types.

Table 2
$\overline{RAS}$ RELATION TO DATA BUS

$\overline{RAS0}$	D0-D17	Bank 1
$\overline{RAS1}$	D18-D36	Bank 2
$\overline{RAS2}$	D0-D17	Bank 3
$\overline{RAS3}$	D18-D36	Bank 4

Table 3
DATA OUT ACCESS TIME

ACCESS TIME	PD7	PD6
100ns (or 50ns for future cards)	0	0
80ns	0	1
70ns	1	0
60ns	1	1

Table 4
32-BIT PRODUCT OFFERINGS

PRODUCT NUMBER (32-BIT SERIES)	MEMORY SIZE (MB)	WORD LENGTH (BITS)	POWER SUPPLY	SPEED
MT8D88C25632-xx	1	16, 32	5V	60-100ns
MT8D88C25632-xxV	1	16, 32	3.3V	100ns
MT16D88C51232-xx	2	16, 32	5V	60-100ns
MT16D88C51232-xxV	2	16, 32	3.3V	100ns
MT8D88C132-xx	4	16, 32	5V	60-100ns
MT8D88C132-xxV	4	16, 32	3.3V	100ns
MT8D88C132-xxS	4	16, 32	3.0/3.3V	60-80ns
MT16D88C232-xx	8	16, 32	5V	60-100ns
MT16D88C232-xxV	8	16, 32	3.3V	100ns
MT16D88C232-xxS	8	16, 32	3.0/3.3V	60-80ns

PRODUCT OFFERING

IC DRAM cards are offered through Micron. The current product spectrum provides memory sizes from 1 MB to 8 MB in 16-, 18-, 32-, 36- and 40-bit word sizes, with both 5V and 3.3V (18- and 36-bit word sizes do not have 3.3V option).

IC DRAM CARD 32-BIT SERIES

The series MT8D88C25632 (1MB), MT16D88C51232 (2MB), MT8D88C132 (4MB) and MT16D88C232 (8MB) are organized to provide a 32-bit word. It is identical to the 36-bit series, except that no bits are provided for parity protection. The data pinout will differ from the 36-bit series as shown in Table 5.

Micron's product offering is shown in Table 4. The series is provided with speed grades from 100ns to 60ns. This is specified with a -10, -8 or -6 suffix to the part number where "xx" is shown. The cards use low power extended refresh DRAMs. Cards using a 3.3V supply have their speed grade appended with a "V" option. Cards that use self refresh DRAMs have their speed grade appended with an "S" option.

Table 5
32-BIT AND 36-BIT SERIES

	32-BIT SERIES	36-BIT SERIES
Byte 0	D0-D7	D0-D8
Byte 1	D9-D16	D9-D17
Byte 2	D18-D25	D18-D26
Byte 3	D27-D34	D27-D35

Table 6
36-BIT PRODUCT OFFERINGS

PRODUCT NUMBER (36-BIT SERIES)	MEMORY SIZE (MB)	WORD LENGTH (BITS)	POWER SUPPLY	SPEED (ns)
MT12D88C25636-xx	1	16, 18, 32, 36	5V	60-100ns
MT24D88C51236-xx	2	16, 18, 32, 36	5V	60-100ns
MT12D88C136-xx	4	16, 18, 32, 36	5V	60-100ns
MT24D88C236-xx	8	16, 18, 32, 36	5V	60-100ns

IC DRAM CARD 36-BIT SERIES

The series MT12D88C25636 (1MB), MT24D88C51236 (2MB), MT12D88C136 (4MB) and MT24D88C236 (8MB) are organized to provide a 36-bit word with parity per byte. Each byte is specified by a $\overline{CAS}$ control line; therefore, the card can provide 9- or 18-bit words with appropriate design on the system board. The MT12D88C25636 provides 256K by 36 bits or 512K by 18 bits. Bank access (full word) is provided by the appropriate $\overline{RAS}$ lines. Refer to the appropriate datasheet for a block diagram of the internal architecture. Please note that this series does not support output enable and $\overline{OE}$ is internally tied. It is suggested for compatibility reasons that the system board also provide a tie to ground for the $\overline{OE}$ lines.

Micron's product offering is shown in Table 6. The series is provided with speed grades from 100ns to 60ns. This is specified with a -10, -8, -7 or -6 suffix to the part number where "xx" is marked. The cards use low power extended refresh DRAMs. If an 8- or 9-bit card is desired, it can be created through the use of $\overline{CAS}$ line controls to differentiate the data lines by tying the upper data lines to the lower data lines.

Table 7
40-BIT PRODUCT OFFERINGS

PRODUCT NUMBER (40-BIT SERIES)	MEMORY SIZE (MB)	WORD LENGTH (BITS)	POWER SUPPLY	SPEED
MT12D88C25640-xx	1	16, 18, 32, 36, 40	5V	60-100ns
MT12D88C25640-xxV	1	16, 18, 32, 36, 40	3.3V	100ns
MT24D88C51240-xx	2	16, 18, 32, 36, 40	5V	60-100ns
MT24D88C51240-xxV	2	16, 18, 32, 36, 40	3.3V	100ns
MT12D88C140-xx	4	16, 18, 32, 36, 40	5V	60-100ns
MT12D88C140-xxV	4	16, 18, 32, 36, 40	3.3V	100ns
MT12D88C140-xxS	4	16, 18, 32, 36, 40	3.0/3.3V	60-80ns
MT24D88C240-xx	8	16, 18, 32, 36, 40	5V	60-100ns
MT24D88C240-xxV	8	16, 18, 32, 36, 40	3.3V	100ns
MT24D88C240-xxS	8	16, 18, 32, 36, 40	3.0/3.3V	60-80ns

IC DRAM CARD 40-BIT SERIES

The series MT12D88C25640 (1MB), MT24D88C51240 (2MB), MT12D88C140 (4MB) and MT24D88C240 (8MB) provide a 40-bit word amenable to word-wise error correction coding. The series does support output enable control and, therefore, read-modify-write cycles for error detection and correction. If desired, the card may function as a universal solution for 8-, 9-, 16-, 18-, 32-, 36- or 40-bit solution. The $\overline{RAS}$ and $\overline{CAS}$ lines are configured the same way as the above cards. In a 40-bit mode, $\overline{RAS0}$ is tied to $\overline{RAS2}$ and $\overline{RAS1}$ is tied to $\overline{RAS3}$. Also, $\overline{CAS}$ lines are tied together. This allows the first bank to be selected by $\overline{RAS0}$ and $\overline{RAS2}$ lines, and the second bank by $\overline{RAS1}$ and $\overline{RAS3}$ lines. This is external to the card.

Micron's product offering is shown in Table 7. The series is provided with speed grades from 100ns to 60ns. This is specified with a -10, -8 or -6 suffix to the part number. The cards use low power extended refresh DRAMs. Cards using a 3.3V supply have their speed grade appended with a "V" option. Cards that use self refresh DRAMs have their speed grade appended with an "S" option. Information on these and other IC card products is available from Micron.

SERVICES

Micron stands ready to help customers who wish to enter the IC DRAM card market with proprietary solutions. Our staff engineers are well versed in the design of boards for the entire PCMCIA/JEDEC/JEIDA arena. If one of our standard products does not meet your current needs, we are ready and able to design a custom solution for you.

For customers desiring a standard product under private label, Micron can supply current products labeled and marked in virtually any manner the customer wishes. Simply supply us with the desired artwork showing the desired markings and Micron will do the rest.

Often overlooked by companies considering entrance into the IC card market are the mechanical considerations. Micron has invested considerable time and effort into developing superior card frames, covers and components. Our custom design services break down the significant entry barriers to this burgeoning market and will get your product to market on-time and on-budget. Design services offered include

Design from concept
Schematic capture
Board layout
Enclosure design
Thermal and signal noise analysis
Custom marking
Comprehensive testing
Connector redesign
ASIC solutions
Packaging solutions

For those considering including IC DRAM cards in their system design as an add in product, turnkey solution or custom design, a design guideline, "Designing for IC Cards" (publication no. PPG03) is available through Micron. Applications engineering assistance is also available from 8 a.m. to 5 p.m. Mountain Time at (208) 368-3900.

The IC card arena is very fast-paced. Product development and introduction will quickly outdate current information. When contemplating a design in this arena, please call us for the latest product datasheets and design guidelines.

APPLICATION NOTE

CHIPS & TECHNOLOGIES' 82C456 CONTROLLER USING MT4C1664

INTRODUCTION

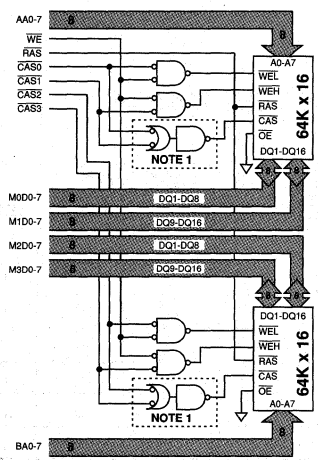
Micron's MT4C1664 64K x 16 DRAM is an ideal solution for replacing 64K x 4 DRAMs in VGA systems. For a 256KB memory system, two MT4C1664 components replace eight 64K x 4 DRAMs. This provides improved reliability and performance margins, decreased power consumption, reduced costs and board savings using state-of-the-art technology.

This application note shows how the MT4C1664 can be interfaced with the Chips and Technologies 82C456 VGA controller chip. It evaluates the pertinent timing parameters and determines the amount of margin available between the two components.

Micron's Technical Notes (TN-04-03 and TN-04-04) show that the MT4C1664 can interface with virtually any VGA controller available on the market. The timing analysis procedure used to evaluate the MT4C1664 and the 82C456 may also be applied to other VGA controllers to determine how they may best be used with the MT4C1664.

The schematics in Figure 1 show a 256KB memory, which interfaces with the 82C456. The memory is implemented with both MT4C1664 (64K x 16 DRAM) and 64K x 4 DRAMs.

256KB DRAM Memory with Two Micron 64K x 16 DRAMs



256KB DRAM Memory with Eight 64K x 4 DRAMs

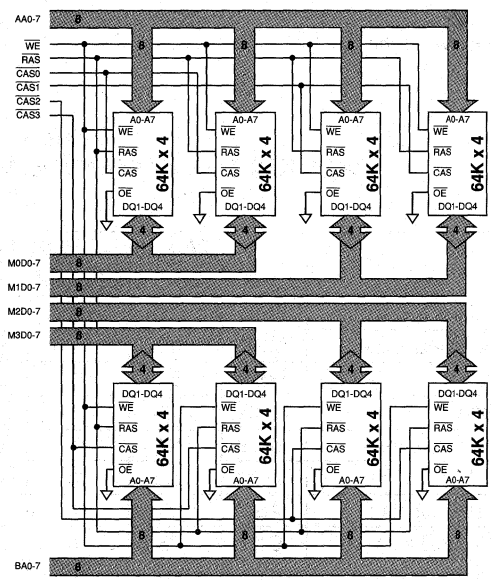


Figure 1
256KB EARLY-WRITE MEMORY

NOTE: 1. This delay path needs to be slightly longer (minimum of 0ns) than either NAND gate to ensure the $\overline{WE}$ to $\overline{CAS}$ setup time is met. This guarantees the DRAM will always be in EARLY-WRITE during WRITE cycles.

TIMING ANALYSIS

The timing margin available between the MT4C1664 and the 82C456 is determined using each device's guaranteed minimum timing specifications. The first step in determining the amount of timing margin is to construct the timing waveforms of the VGA controller (Figure 2). The control and data comes from the controller and goes to the DRAM memory except for data out (Q), which comes from the DRAM back to the controller.

The second step is to compare the specifications required by the DRAM to those of the VGA controller. The amount of margin available is the difference between the two. Remember that the minimum specification of the VGA controller is not the same as that of the DRAM. The VGA controller's minimum is that which the controller is guaranteed to provide to the DRAM. The DRAM's minimum is that which the DRAM requires in order to function properly. For example, the 82C456 specs its ^{t}CRP to be 25ns minimum (@ 40 MHz) while the MT4C1664 only requires a minimum of 5ns. Thus, this difference results in a margin of 20ns between what the 82C456 provides and what the MT4C1664 requires.

The additional logic required to use the MT4C1664 with the Chips and Technologies 82C456 VGA controller introduces a timing skew on the $\overline{CAS}$, $\overline{WE}$ and Q signals. The final portion of the analysis determines how much skew is tolerable. The second section of the timing waveform in Figure 2 shows the effects of the additional logic delays (timing skews) and the decrease in margin between the two devices.

The analysis shows that logic delays of 10ns and 15ns (10ns for the negated NAND path and 15ns for the negated OR connected to a NAND path) allows the MT4C1664 to meet all of the Chips and Technologies 82C456 VGA specifications.

Additional timing delay may be used in the added logic circuitry. The negated OR in series with the NAND path may have its delay increased by 5ns (from 15ns to 20ns). An additional delay of more than 5ns will violate the ^{t}CRP minimum of the MT4C1664. Except for ^{t}CRP and ^{t}RSH, all the other parameters skewed by the added logic have more than sufficient timing margins.

Table 1 summarizes the memory timing specifications of a VGA system using the 82C456 VGA controller with the MT4C1664. Logic delays of 10ns and 15ns introduced by the additional logic are also evaluated. The amount of timing margin available in both cases (with and without the logic delays) is summarized.

Table 1
MINIMUM TIMING SPECIFICATION COMPARISON

		DATA SHEET SPECIFICATIONS			WITH LOGIC DELAY				
PARAMETER	SYM	82C456	MT4C1664	MARGIN	82C456	MT4C1664	MARGIN	UNITS	NOTES
$\overline{RAS}$ pulse width	^{t}RAS	100	100	0	-	-	-	ns	1
$\overline{CAS}$ to $\overline{RAS}$ precharge time	^{t}CRP	25	5	20	10	5	5	ns	
$\overline{RAS}$ hold time	^{t}RSH	50	25	25	35	25	10	ns	
$\overline{CAS}$ pulse width	^{t}CAS	100	25	75	-	-	-	ns	1
Write command hold time	^{t}WCS	50	0	50	5	0	5	ns	
Write command setup time	^{t}WCH	125	20	105	95	20	75	ns	
Column address setup time	^{t}ASC	25	0	25	-	-	-	ns	1
Column address hold time	^{t}CAH	75	15	60	-	-	-	ns	1
Data-in setup time	^{t}DS	50	0	50	65	0	65	ns	
Data-in hold time	^{t}DH	125	15	110	110	15	95	ns	
Access time from $\overline{CAS}$	^{t}CAC	75	30	45	60	30	30	ns	
Access time from $\overline{RAS}$	^{t}RAC	125	100	25	-	-	-	ns	1

NOTE: 1. Additional logic does not skew timing between the 82C456 and the MT4C1664.

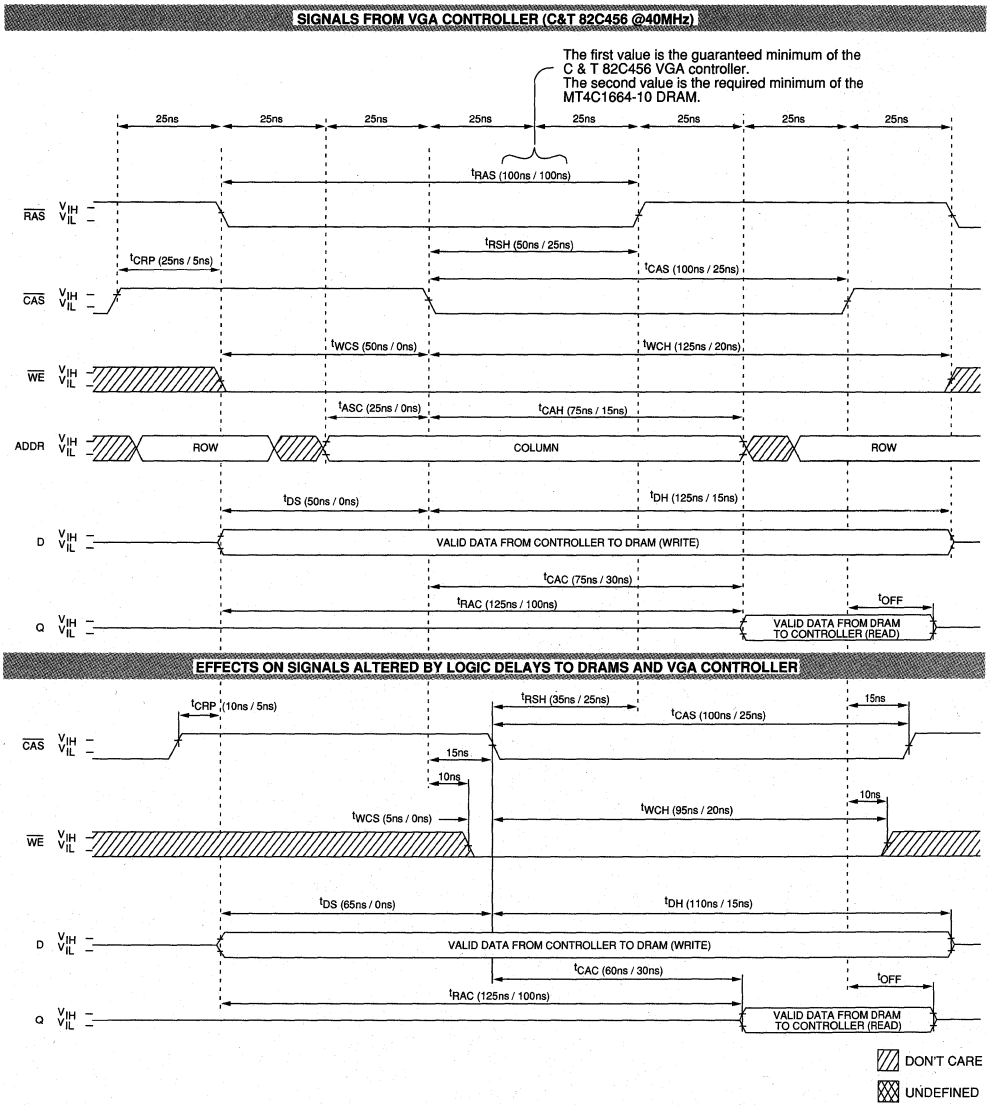


Figure 2
TIMING ANALYSIS OF MT4C1664 WITH C & T 82C456

NEW ■ APPLICATION/TECHNICAL NOTE

MICRON TECHNOLOGY, INC.

DYNAMIC RAMS 1

WIDE DRAMS 2

DRAM MODULES 3

IC DRAM CARDS 4

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OVERVIEW

At Micron, we emphasize superior product quality through our unmatched reliability system. We define product reliability as a product's ability to perform its intended functions and operate under specified environmental conditions for a specified length of time. This section contains a brief overview of some of the issues that affect the reliability of IC devices, and briefly describes Micron's reliability program.

For a more in-depth discussion of reliability, please refer to Micron's Quality/Reliability literature.

RELIABILITY GOALS

When we discuss reliability goals of semiconductor ICs, we typically refer to the traditional reliability curve of component life. The reliability curve, or "bathtub curve," appears below, where h(t) is the hazard rate or the probability of a component failing at t_0+1 in time if it has survived at time t_0.

Figure 1 shows that the significant portion of this curve is the random failure segment. The term "infant mortality" refers to those ICs that would fail early in their lives due to manufacturing defects. To screen out such failures, Micron evaluates all our products using intelligent burn-in. This unique AMBYX™ intelligent burn-in/test system, developed by Micron is described in the following section.

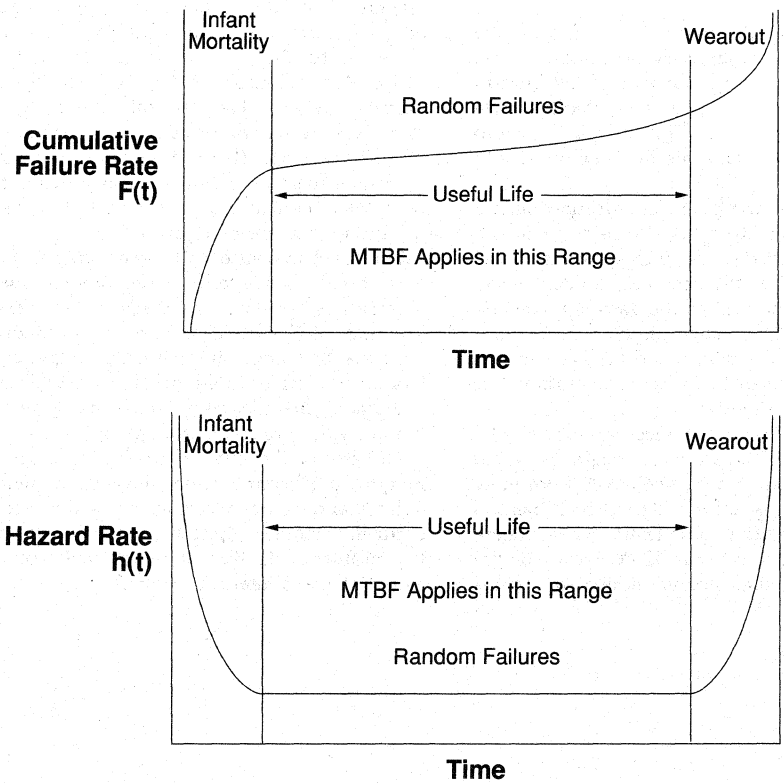


Figure 1
RELIABILITY CURVE

MICRON'S AMBYX™ INTELLIGENT BURN-IN AND TEST SYSTEM

Throughout the semiconductor industry, burn-in has been a crucial factor to increase memory product reliability. Micron stresses our memory devices to simulate years of normal use. Then we document and analyze the results so that we can take any corrective action needed. To effectively screen out infant mortalities, Micron believes it is critical to functionally test devices several times during the burn-in cycle without removing them from the burn-in oven. We were so convinced of the importance of highly refined burn-in that we searched for a system to meet this need. Because we found no system that met our requirements, we introduced the concept of "intelligent" burn-in and, in 1986, developed the AMBYX™ intelligent burn-in and test system. Today, we use AMBYX to test every component product we make.

With AMBYX, we can determine if the failure rate curves of *individual* product lots reach the random failure region of the bathtub curve by the end of the burn-in cycle. We subject product lots that do not exhibit a stable failure rate to additional burn-in. This burn-in flow also brings the slightest variation in a product's failure rate to our attention.

Since AMBYX allows us to test devices for functionality without removing them from the burn-in oven, we effectively eliminate failures resulting from handling, thereby minimizing "noise" from the test results. During the test phase, output produced by the devices under test is compared to the pattern expected. If a discrepancy occurs, AMBYX records the failure and provides the bit address, device address, board address, temperature, Vcc voltage, test pattern and time set.

During the burn-in cycle itself, devices are functionally tested in four intervals. The first test begins at room temperature. Then, we ramp up the oven to 85°C for more functional testing. This enables us to detect thermal intermittent failures, another unique feature of intelligent burn-in. We conduct the next test at 125°C — any device that does not pass this sequence is eliminated. As the burn-in process continues, the devices are dynamically stressed at high temperature and voltage for a given number of hours. At the end of this period, we functionally test all devices again, followed by another burn-in cycle and further tests. This sequence is repeated four times on every device in every production lot.

These test results allow us to identify individual failures after each burn-in cycle. Figure 2 illustrates how the four burn-in and test cycles flow. The typical test results shown make up the first portion of the bathtub curve of component reliability.

There are two important reasons that Micron conducts the last two burn-in and test periods (or "quarters") at lower Vcc than the first two portions. First, we want the several million device hours that we accumulate weekly on production lots to be conducted at stress conditions identical to the conditions for the extended high-temperature-operating-life (HTOL) test. All semiconductor manufacturers use this test to calculate random field failure rates. Second, we want to be sure we are not introducing new failure modes (failures unrelated to normal wearout) by testing them at extremely elevated conditions. In this way, Micron ensures that we've effectively screened our products for infant mortalities.

Control charts, such as the one shown in Figure 3, alert us to trends in the failure rates of some lots. When we detect an increase in a certain failure rate, we pinpoint the lots that need additional burn-in cycles to identify all variables that might influence the failure rates of those lots. Such variables could include fabrication and assembly equipment, manufacturing shifts and time frames when the lots were processed through specific steps.

The overall benefits of intelligent burn-in are wide ranging. Intelligent burn-in allows us to identify early-life failures and failure mechanisms as they would actually occur in customer applications. It also allows us to identify problem lots that, if undetected, could contribute substantially to infant mortalities.

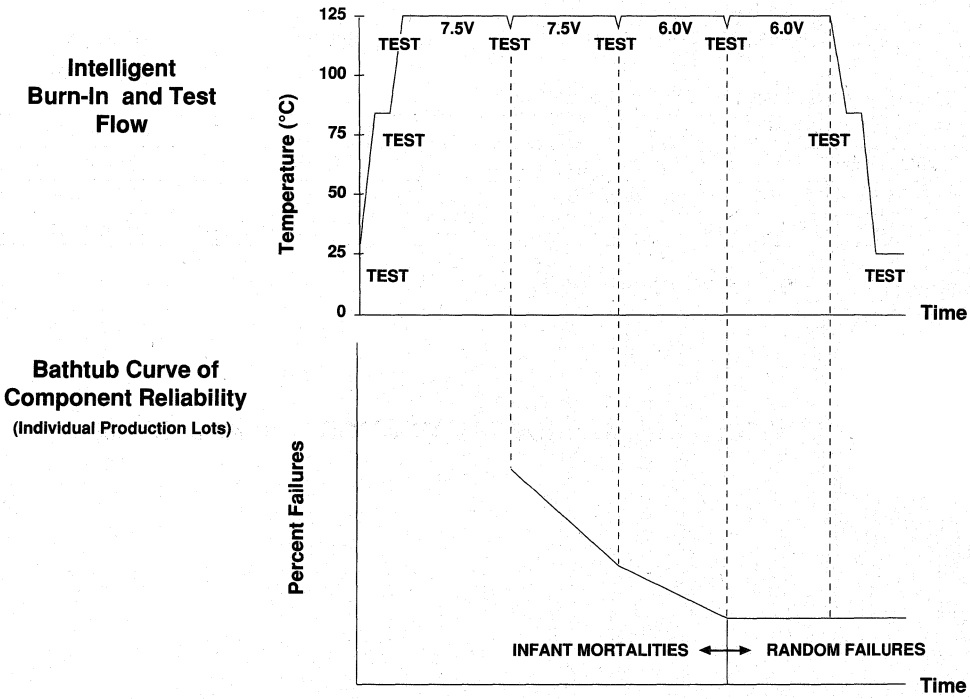


Figure 2
AMBYX™ BURN-IN/TEST FLOW AND TEST RESULTS

ENVIRONMENTAL PROCESS MONITOR PROGRAM

Micron's environmental process monitor (EPM) program is designed to ensure the reliability of our standard products. Under this program, we subject weekly samples of our various product and package types to a battery of environmental stress tests.

As discussed in the previous pages, we test our devices for many hours under conditions designed to simulate years of normal field use. We then apply equations derived from intricate engineering models to the data collected from the accelerated tests. From these calculations, we are able to predict failure rates under *normal use*. Figure 3 shows the conditions for these tests, known as "accelerated environmental stress" tests. The EPM program described in Figure 3 is for our 1 Meg SRAM.

TEST NAME AND DESCRIPTION	TEST DURATION	BIWEEKLY SAMPLE SIZE
HIGH TEMPERATURE OPERATING LIFE (125°C, 6.0V, Checkerboard/Checkerboard Complement Pattern)	1,008 Hours	100 Devices
TEMPERATURE AND HUMIDITY (85°C, 85% R.H., 5.5V, Alternating Bias)	1,008 Hours	50 Devices
AUTOCLAVE (121°C, 100% R.H., 15 PSI, No Bias)	288 Hours	25 Devices
LOW TEMPERATURE LIFE (-25°C, 7.0V, Checkerboard/Checkerboard Complement Pattern)	1,008 Hours	5 Devices
TEMPERATURE CYCLE (-65°C TO +150°C, Air to Air)	1,000 Cycles	50 Devices
THERMAL SHOCK (-55°C TO +125°C, Liquid to Liquid)	700 Cycles	10 Devices
HIGH TEMPERATURE STORAGE (150°C, No Bias)	1,008 Hours	50 Devices
ELECTROSTATIC DISCHARGE (+ and -)	MIL-STD-3015.7	40 Devices

NOTE: Samples pulled from five different lots at finished goods.

Figure 3
SAMPLE ENVIRONMENTAL PROCESS MONITOR – 1 MEG SRAM

FAILURE RATE CALCULATION

The failure rate during the useful life of a device is expressed as percent failures per thousand device hours or as FITs (failures in time, per billion device hours). Using Micron's 4 Meg DRAM as an example, the failure rate is calculated as follows:

Failure Rate = Pn ÷ [Device hours × A.F. environment]

A.F. is relative to the typical operating environment.

where: Pn = Poisson Statistic (at a given confidence level). In our example, Pn = 0.916 at at 60 percent confidence level.

Device hours = sample size multiplied by test time (in hours) In our example, device hours equal 8.145×10^5 in an accelerated environment.

A.F. = acceleration factor between the stress environment and ***typical*** use conditions. For the 4 Meg DRAM, the acceleration factor between 125°C, 6V (HTOL stress conditions) and 50°C, 5V (typical operating conditions) equals 89.2. (Calculation of this acceleration factor is described in the following section.)

Thus, the failure rate of the Micron 4 Meg DRAM family is computed as follows:

Failure Rate = $0.916 \div (8.145 \times 10^5)\ (89.2) = 1.261 \times 10^{-8}$

where: total device hours at test conditions = 3.04×10^6. Equivalent device hours at typical use conditions (50°C, 5V Vcc) using an acceleration factor of 89.2 equals $89.2\ (8.145 \times 10^5) = 75 \times 10^6$.

To translate this failure rate into percent failures per thousand device hours, we multiply the failure rate obtained from the equation above by 10^5:

Failure Rate = $(1.261 \times 10^{-8}) \times 10^5 = 0.001261\%$ or 0.0013% per 1K device hours

To state the failure rate in FITs, we multiply the failure rate obtained from the equation above by 10^9:

Failure Rate = $(1.261 \times 10^{-8}) \times 10^9 = 12.61$ or 13 FITs

ACCELERATION FACTOR CALCULATION

Again, using the 4 Meg DRAM as our example, the acceleration factor between high temperature operating life stress conditions (125°C, 6V) and typical operating conditions (50°C, 5V) is computed using the following models:

ACCELERATION FACTOR DUE TO TEMPERATURE STRESS

The acceleration factor due to temperature stress is computed using the Arrhenius equation, which is stated as follows:

$$A.F._{t1/t2} = e\left[\frac{E_a}{kT_1} - \frac{E_a}{kT_2}\right]$$

where: k = Boltzmann's constant , which is equal to 8.617×10^{-5} eV/K

T_1 and T_2 = typical operating and stress temperatures, respectively, in kelvins

E = activation energy in eV (For oxide defects, which is the most common failure mechanism for the 4 Meg DRAM, used in our example, the activation energy is determined to be 0.3eV.)

Using these values, the temperature acceleration factor between 125°C and 50°C is computed to be 7.62.

ACCELERATION FACTOR DUE TO VOLTAGE STRESS

The acceleration factor due to voltage stress is computed using the following model:

$$A.F._{v1/v2} = e\left[\beta\left(\frac{v_1 - v_2}{2}\right)\right]$$

where:

v_1 and v_2 = stress voltage and typical operating voltage, respectively, in volts

β = constant, the value of which was derived experimentally by running several sessions of Micron's intelligent burn-in test sequence at different voltages on large numbers of the device. (For the 4 Meg DRAM used in our example, ß equals 4.92.)

Thus, the voltage acceleration factor for the 4 Meg DRAM between 6V (stress condition) and 5V (typical operating condition) is computed to be 11.70.

Finally, the overall acceleration factor due to temperature and voltage stress is calculated as the product of the two respective acceleration factors or:

$$A.F._{overall} = A.F._{temperature} \times A.F._{voltage}$$
$$= 7.62 \times 11.70$$
$$= 89.2$$

RELIABILITY

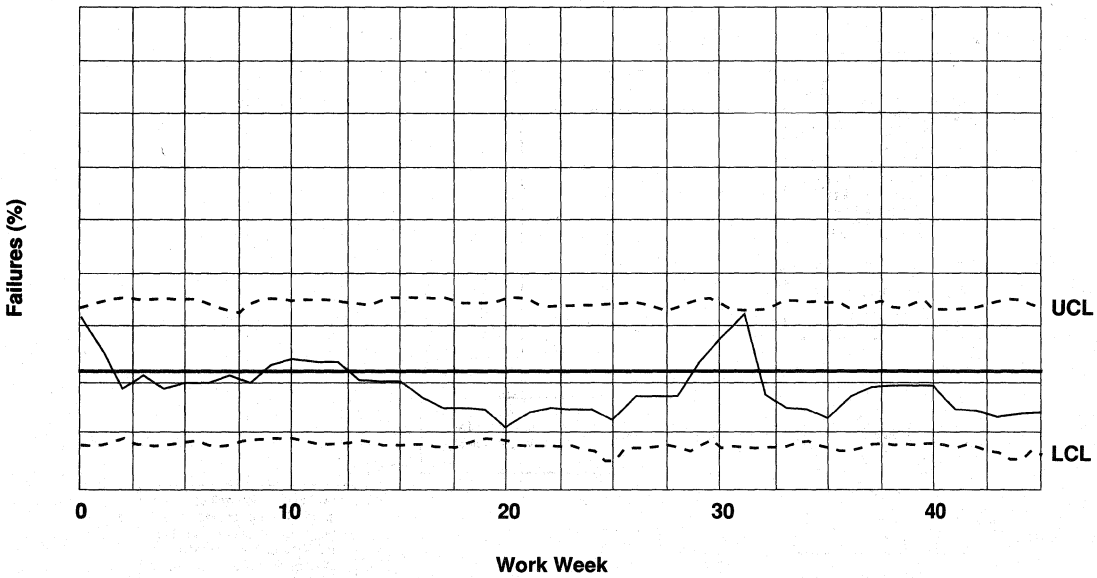


Figure 4
AMBYX™ FOURTH QUARTER FAILURES

OUTGOING PRODUCT QUALITY

Before being sent to our finished goods area, where products are prepared for shipping, a special unit within the quality assurance department takes a one-percent sample from each production lot. These samples are subjected to visual and electrical testing in order to measure the acceptable quality level (AQL) of all outgoing product. Figure 4 shows a flowchart illustrating Micron's AQL test procedure.

Visual or mechanical testing consists of an unaided visual inspection of the sample devices for any physical irregularities that could negatively affect device performance. If a sample device is found to have, for example, a bent lead, a package irregularity or excess solder, the entire lot is returned to our test area for a 100 percent visual inspection.

Electrical testing of the sample devices is performed using ATE (automatic test equipment) systems. Testing is conducted at room temperature (~25°C) and at 70°C. Should an electrical failure occur, a quality assurance engineer further evaluates the failing device. After completing this analysis, the quality assurance engineer determines which production monitor/test should have caught the failure, and the entire lot is retested at that point in the test flow. These are important steps to preserve the integrity of our test process.

Micron records the percent of devices found to be defective in the total number sampled weekly on a control chart. This chart, containing AQL data for the previous 52 weeks, is presented in weekly management meetings so that the quality assurance department can take appropriate action.

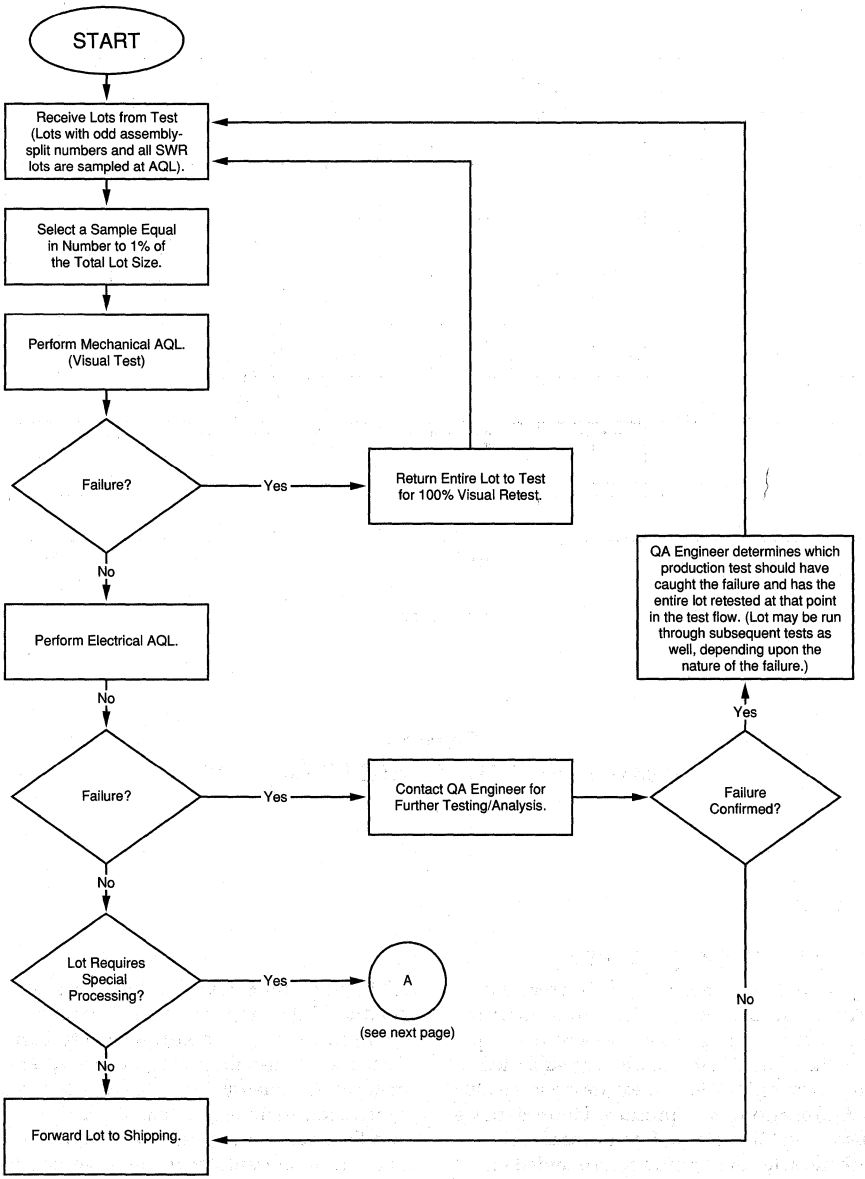


Figure 5
AQL TEST FLOW FOR ALL OUTGOING PRODUCTS

Example of Special Processing: Lot Mounted on Tape & Reel

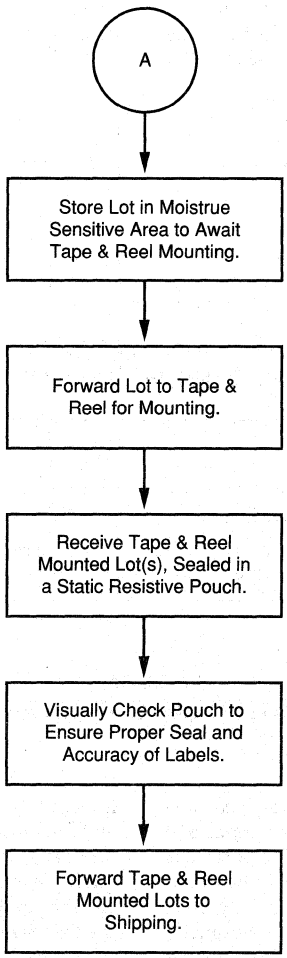


Figure 6
AQL TEST FLOW — SPECIAL PROCESSING

AUTOMATED DATA CAPTURE & ANALYSIS

Micron has developed a sophisticated data capture and analysis system with a computer network tailored to the needs of quality IC manufacturing. Figure 5 shows the various functional areas that provide the input to our VAX data bases.

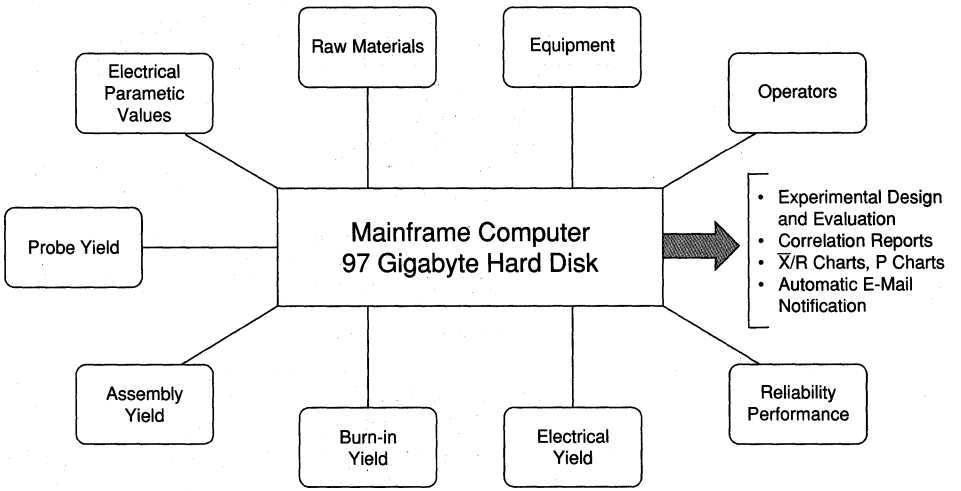


Figure 7
STATISTICAL CORRELATION

DATA CAPTURE

Automated, real-time data capture makes real-time charting ($\bar{X}$ and R charts, etc.) of all critical operations and processes possible and ensures that appropriate personnel know of any unexpected variation on a timely basis. As production lots move through each manufacturing step, detailed information (including step number, lot number, machine number, date/time, and operator number) is entered into the production data base. Automated, highly-programmable measurement systems capture a host of parameters associated with equipment, on-line process material and environmental variables.

ANALYTICAL TOOLS

By using highly flexible, on-line data extraction programs, system users can tap this vast data base and design their own correlation and trend analyses. Because we can correlate process variables to product performance, we can make on-line projections of the quality of our finished product for a given lot or process run. In addition, we can estimate the impact of process improvements on quality well in advance and can make the impact of process deviations more visible to our engineers. This approach allows us to model yield and quality parameters based on on-line parameters. We then use this model to predict the final product results through the following means:

GROUP SUMMARIES

Summaries, which provide the means and standard deviations of user-defined parametrics, enable system users to compare the parametric values of production lots as well as special engineering lots.

TREND ANALYSIS

Trend charts are routinely generated for critical parameters. System users can plot the means and ranges of any probe or parametric data captured throughout the manufacturing process.

CORRELATION ANALYSIS

Correlation analysis can be performed on any combination of factors; such as equipment, masks or electrical parameters. One report, regularly produced and disseminated to key personnel, takes two groups of lots (one with a high failure rate, the other with a low failure rate) and identifies all the pieces of equipment that are common to one or the other group. The report quickly alerts us to any correlation between a lot with a high failure rate and particular piece(s) of equipment in the wafer fabrication or assembly areas.

Another regularly produced report analyzes a user-selected set of database parametrics against an index, such as manufacturing yield. Lots are divided into three subgroups (upper yielding, middle yielding and lower yielding). The report then correlates the yields with all electrical parametric values taken on individual lots at wafer sort. It helps us determine which processing step may have caused the yields to vary among the three subgroups.

STATISTICAL PROCESS CONTROL CHARTS

Micron employs SPC control charts throughout the company to monitor and evaluate critical process parameters, such as critical dimensions (CDs), oxide thickness, chemical vapor depositions (CVDs), particle counts, temperature and humidity, and many other critical process and product quality parameters.

OVERLAYS OR WAFER MAPS

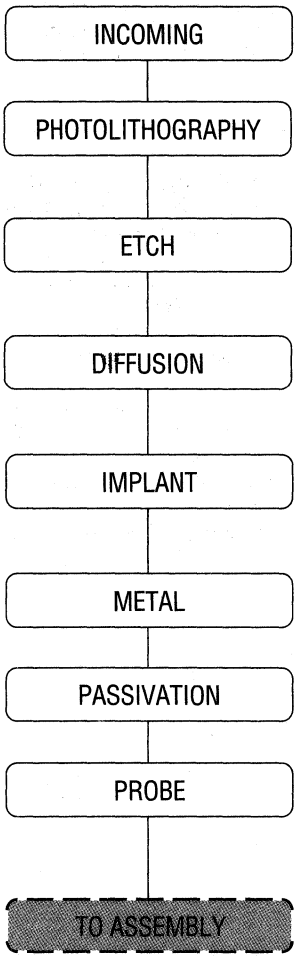
Maps, which are produced for all wafers during probe, show various parameters as a function of position on the wafer and are very useful for problem isolation. Maps may be analyzed individually or in groups. For example, wafers from an entire lot may be analyzed in relation to one particular parameter.

RS/1 DISCOVER/EXPLORE

This analysis software is used for experimental design, and evaluation of results. The statistical approach supported by this software (*t* tests, ANOVA tables, multiregression analysis, etc.) has proven invaluable in reducing time expended for product development and trouble shooting. It is also used to determine the relationships between process output and probe and parametric data. Using multiregression analysis, for example, we are able to determine the relationship between L effective and CD dimensions to the speed of a device.

The use of automation in data capture, analysis and feedback greatly enhances the flexibility and speed with which we can view all aspects of the manufacturing process. This effective data analysis and feedback system helps to reduce parametric deviations, improve margin to specifications, increase manufacturing yields and provide more accurate fabrication output planning.

FABRICATION*



Incoming
Verification that the starting material is clean and uniform, and complies with all requirements. Each wafer receives an individual laser scribe for total product traceability.

Photolithography
Wafers are coated with a layer of light-sensitive photoresist. Specified sections of the wafer are exposed by projecting ultraviolet light onto the wafer through a mask. The exposed photoresist hardens and becomes impervious to etchants.

Etch
The areas of the wafer not protected by the exposed photoresist are removed by either plasma (dry etch) or acid (wet etch). The photoresist is then cleaned ("stripped") off of the wafer, leaving a pattern in the exact design of the mask.

Thermal Processing
Wafers are placed in furnaces where they are exposed to various gases while being heated to temperatures over 1,000 degrees celsius.Layers similar to glass are grown on the wafer. These layers help form the building blocks for the circuitry constructed on each wafer.

Implant
Wafers are bombarded with positively or negatively charged dopant ions, which are implanted into the silicon. This process changes electrical characteristics in selective areas of the silicon. This is called "doping," and forms conductive regions on the wafer.

Metal
A thin layer of aluminum or other metal is deposited and patterned, forming interconnections between various regions of the die.

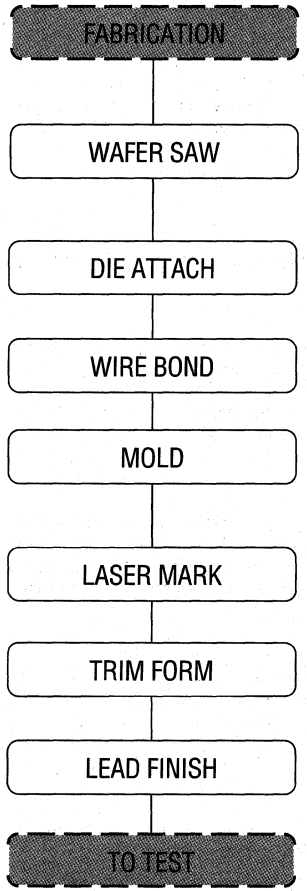
Passivation
The fabrication process is completed by forming a final glass layer on the wafer. This layer protects the circuits from contamination or damage through the testing and packaging process flows.

Probe
When the fabrication process is complete, each wafer consists of many "dice." Each die on the wafer is taken individually through a series of tests. A computer attached to a probe card tests the die and produces a "wafer map" storing data on each functioning (good) die . All data is collected and stored for each die. Wafer maps are used in assembly to ensure that only good dice are packaged.

Assembly (see next page)

*This flow is general and is based on DRAM products.

ASSEMBLY*



Fabrication
Before assembly, incoming raw silicon wafers are processed through a myriad of fabrication steps. This fabrication process yields fully-fabricated wafers containing complete, functioning circuitry in die form. These wafers go to assembly so each individual die may be separated and packaged prior to final testing.

Wafer Saw
Wafers that have finished Fab processing and probe are automatically mounted on a carrying film. The wafer is then sawed using an automated, high-speed diamond blade and high-pressure water. This separates each individual die from the others on the wafer without disturbing the carrying film.

Die Attach
With automated pick-and-place equipment, the good dice as specified by the probe "wafer map" are removed from the carrier film. Each die is attached to a leadframe with a layer of adhesive.

Wire Bond
With high-speed automated equipment, interconnections are made with gold wire (the diameter of a human hair). These interconnections are between the aluminum circuit on the die and the lead fingers of the leadframe.

Mold
A heated mold with a hydraulic press is used to transfer hot thermosetting plastic into mold cavities where the leadframe is placed. This encapsulation protects the die and the interconnections throughout the useful life of the product.

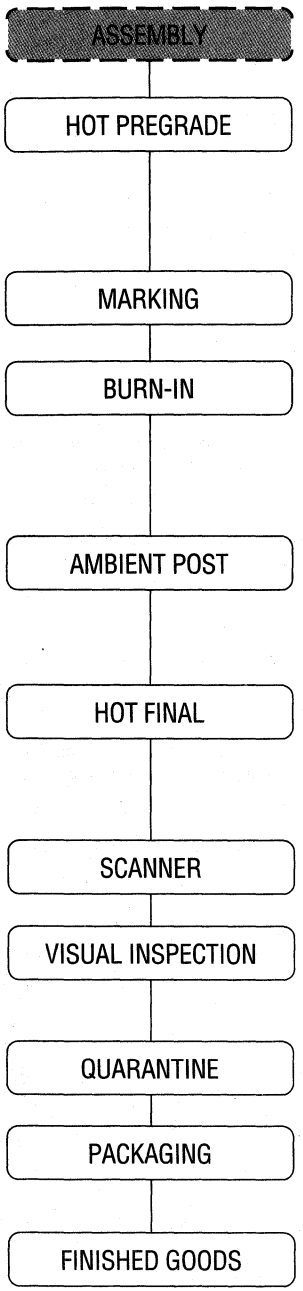
Laser Mark
A laser mark is scribed on the bottom side of the package. This mark is a code used to identify the assembly manufacturing lot.

Trim/Form
A press with a tool set is used to cut and form leads of the lead frame into specified shapes. Some packages have leads formed for surface mount applications. Other packages have leads for through-hole applications.

Lead Finish
Each package is given a lead finish of tin/lead (solder) to ensure reliable application by the customer.

Test (see next page)

*This flow is general and is based on DRAM products.



TEST*

Assembly
Fully fabricated silicon wafers reach assembly after each die has been probed to screen out failures. Passing chips are then carried through a number of steps to become individual units in leaded packages.

Hot Pregrade
At temperatures ranging from 83°C to 125°C, parts are tested for speed grade and functionality. Parametric tests are performed to detect opens, shorts, input and output leakage, input and output high and low levels and standby current. Functional tests include low and high Vcc margin, vbump, speed sorting, dynamic and static refresh, and a full range of patterns and backgrounds. Patterns performed include row fast, column fast, single and multiple walking columns and diagonals, moving inversions, and fast page or static column. Backgrounds used include solids, checkerboard, row stripes, column stripes and parity. Specific tests and temperatures as applicable to specific products.

Marking
Devices are marked with ink with the following information: year, special process designator, part type, package type and speed grade.

Burn-in
Micron uses its exclusive AMBYX™ intelligent burn-in and test system to screen out infant mortalities. Devices are dynamically burned-in using checkerboard/checkerboard complement patterns in four intervals under the following conditions: 125°C, 7.5V Vcc for the first two intervals and 125°C, 6V Vcc for the final two intervals. Functional testing is performed at 85°C and back to 25°C AMBYX™ tests for thermal intermittent opens. Devices are also functionally tested at burn-in conditions (125°C, 7.5V) at the beginning of the burn-in cycle to verify that the devices under test are being properly exercised.

Ambient Post
At a temperature of 25°C, parametric tests include input and output leakage as well as standby and operating currents. Functional tests include low and high Vcc margin, vbump, speed sorting, dynamic and static refresh, and a full range of patterns and backgrounds. Patterns performed include row fast, column fast, single and multiple walking columns and diagonals, moving inversions and fast page or static column. Backgrounds used include solids, checkerboard, row stripes, column stripes and parity.

Hot Final
At a temperature of 78°C to 100°C, parametric tests include input and output leakage as well as input and output high and low levels. Functional tests include low and high Vcc margin, vbump, speed sorting, dynamic and static refresh, and a full range of patterns and backgrounds. Patterns performed include row fast, column fast, single and multiple walking columns and diagonals, moving inversions and fast page or static column. Backgrounds used include solids, checkerboard, row stripes, column stripes and parity.

Scanner
Devices are optically scanned by an automated scanning machine for bent leads, incorrect splay, coplanarity failures and tweeze failures. Passing and failing parts are then sorted into appropriate bins.

Visual Inspection
All devices, now tested to be functional, are visually inspected for cosmetic defects such as bent leads, poor marks, broken packages and poor solder. Defective products are removed and repaired if possible. Data on the type of defects found is carefuly recorded and used for improving the manufacturing processes in both assembly and test.

Quarantine
All production lots are held at this stage until a quality assurance monitoring program confirms that electrical and environmental specifications are met.

Packaging
Devices are prepared for shipping. They may remain in tubes or they may be mechanically placed in tape-and-reel packages, ready for application in automatic pick-and-place machines. Products will be either dry packed in vacuum sealed bags, or placed in black antistatic bags.

Finished Goods
Devices are shipped through a system that maintains lot identity.

*This flow is general and is based on DRAM products.

MICRON TECHNOLOGY, INC.

DYNAMIC RAMS 1

WIDE DRAMS 2

DRAM MODULES 3

IC DRAM CARDS 4

MULTIPORT DRAMS 5

APPLICATION/TECHNICAL NOTES 6

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PACKAGE INFORMATION 8

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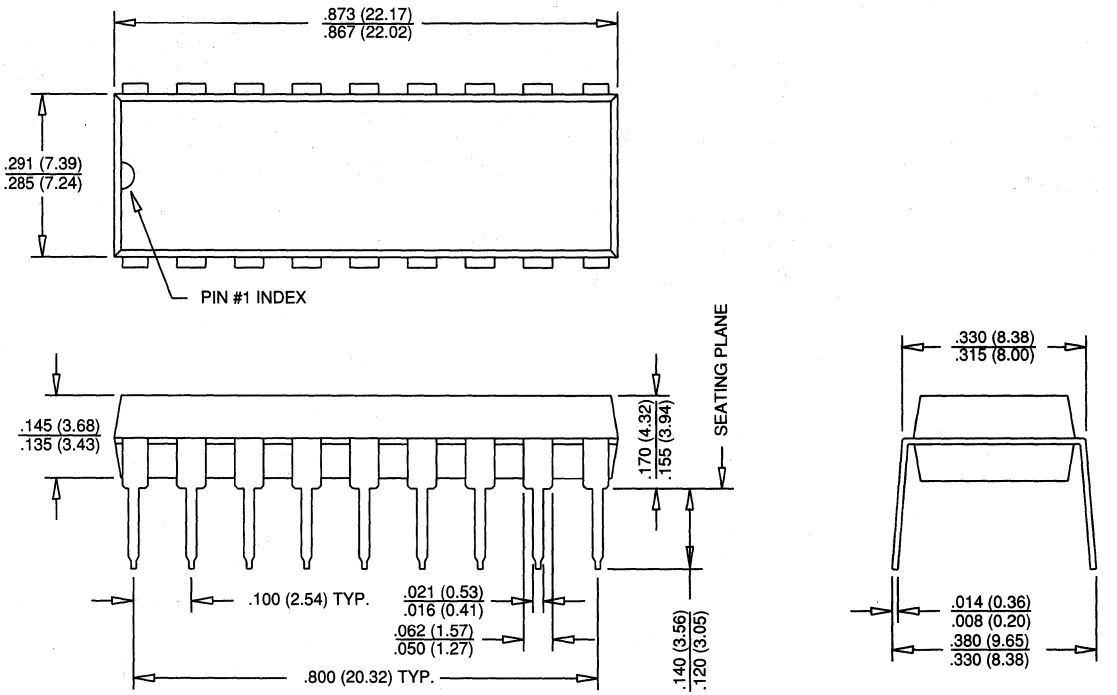
PACKAGE TYPE	PIN COUNT	PAGE
PLASTIC DIP	18	8-2
	20	8-3
PLASTIC ZIP	20	8-4
	20	8-5
	28	8-6
	40	8-7
PLCC	52	8-8
PLASTIC SOJ	20/26	8-9
	24/26	8-10
	24/28	8-11
	28	8-12
	32	8-13
	40	8-14
	42	8-15
TSOP	20/26	8-16
	24/28	8-17
	28	8-18
	32	8-19
	40/44	8-20
	44/50	8-21
MODULE SIP	30	8-22
MODULE SIMM	30	8-28
	72	8-34
IC DRAM CARD	88	8-41

18-PIN PLASTIC DIP (300 mil)

N-1



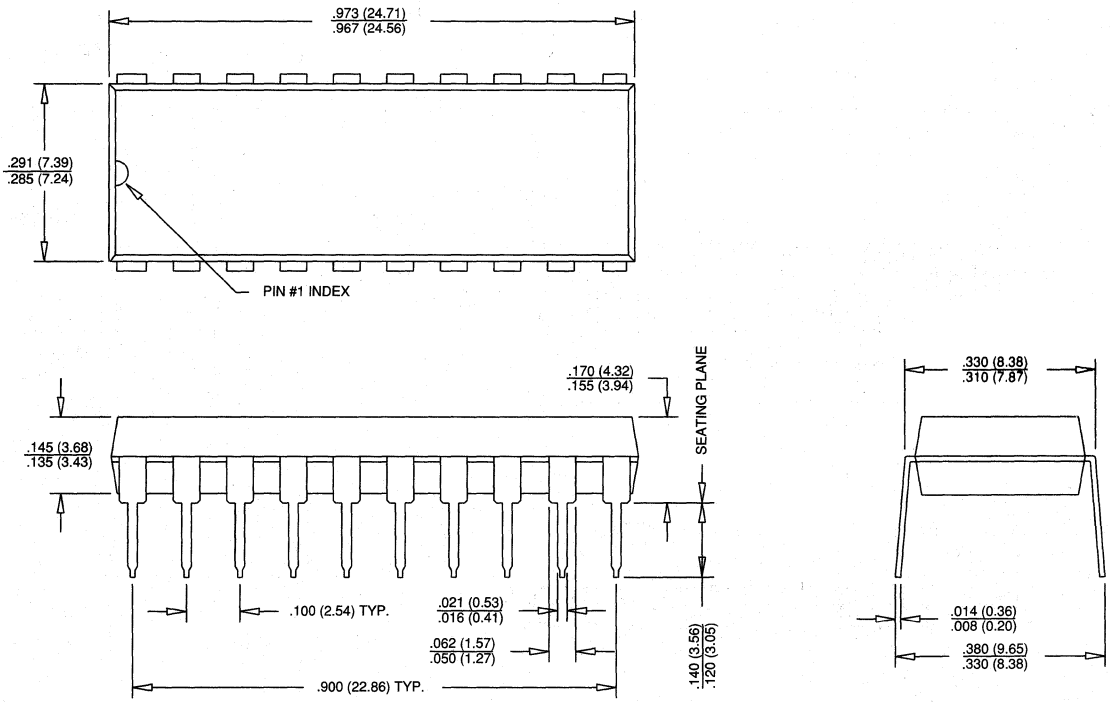
NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

2. Package width and length do not include mold protrusion, allowable mold protrusion is .01" per side.

PACKAGE INFORMATION

20-PIN PLASTIC DIP (300 mil)

N-2

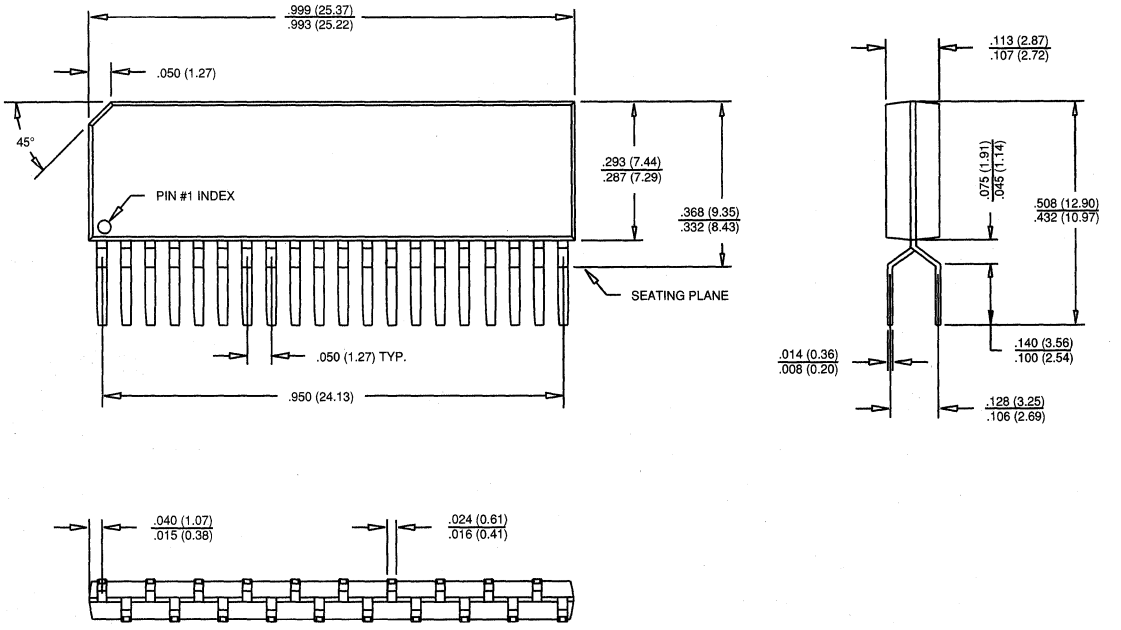


NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

2. Package width and length do not include mold protrusion, allowable mold protrusion is .01" per side.

20-PIN PLASTIC ZIP (350 mil)

O-1



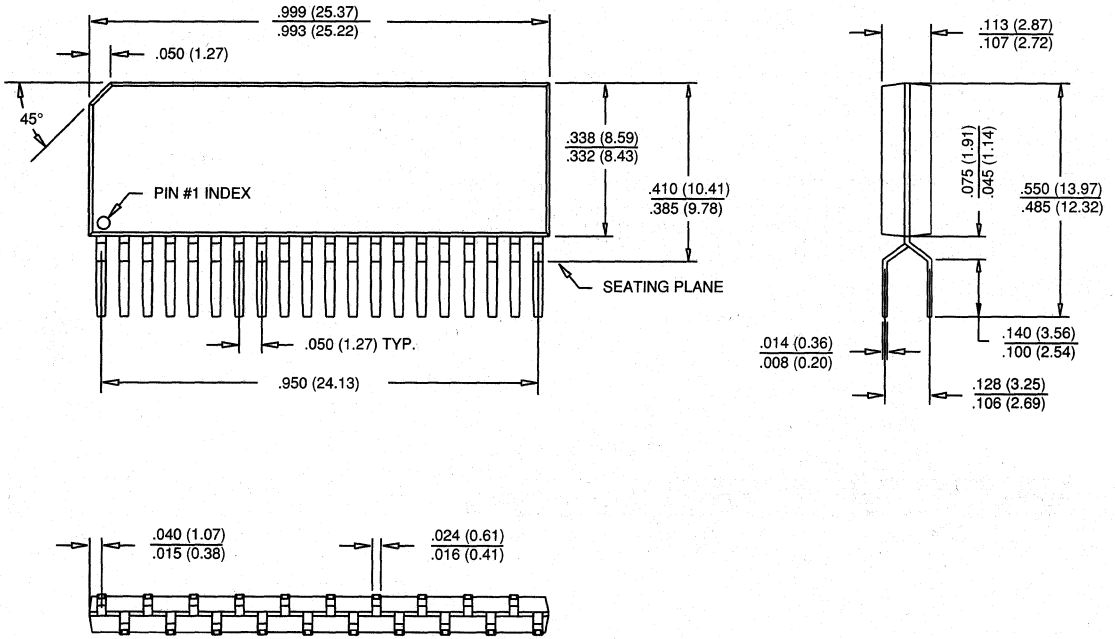
PACKAGE INFORMATION

NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

2. Package width and length do not include mold protrusion, allowable mold protrusion is .01" per side.

20-PIN PLASTIC ZIP (400 mil)

O-2

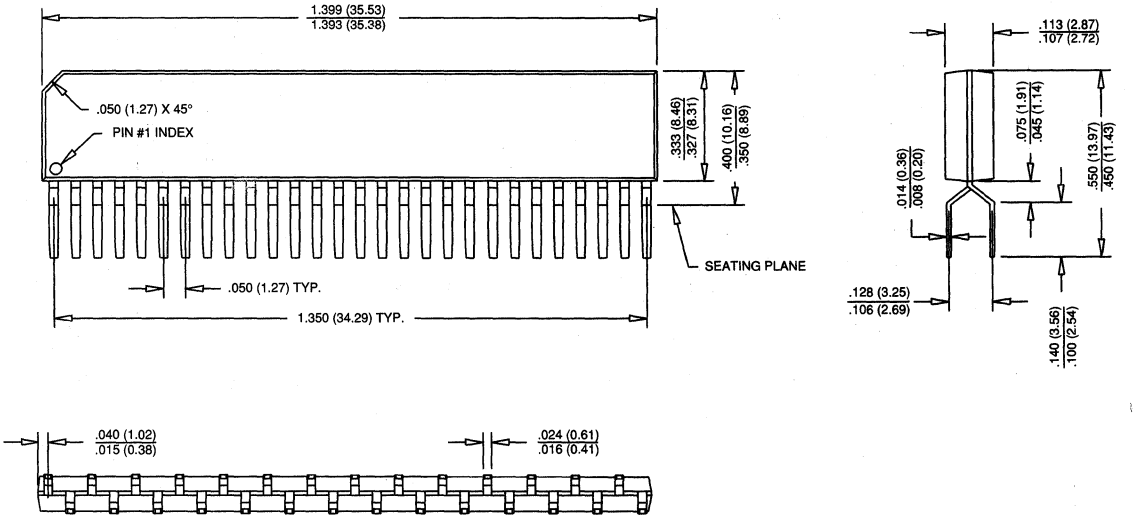


NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

2. Package width and length do not include mold protrusion, allowable mold protrusion is .01" per side.

28-PIN PLASTIC ZIP (375 mil)

O-3

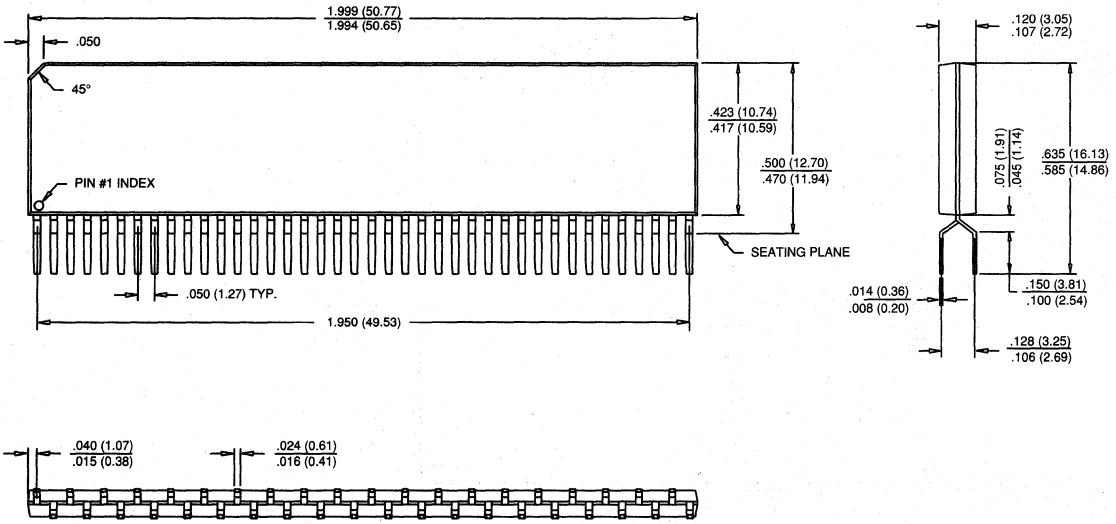


NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

2. Package width and length do not include mold protrusion, allowable mold protrusion is .01" per side.

40-PIN PLASTIC ZIP (475 mil)

O-4

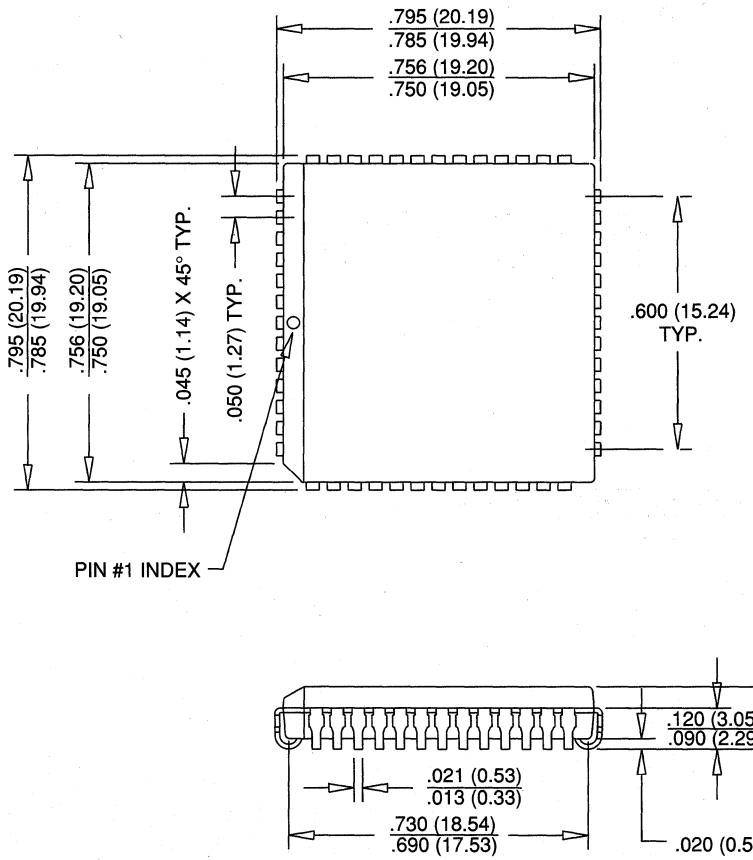


NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

2. Package width and length do not include mold protrusion, allowable mold protrusion is .01" per side.

52-PIN PLCC

P-1

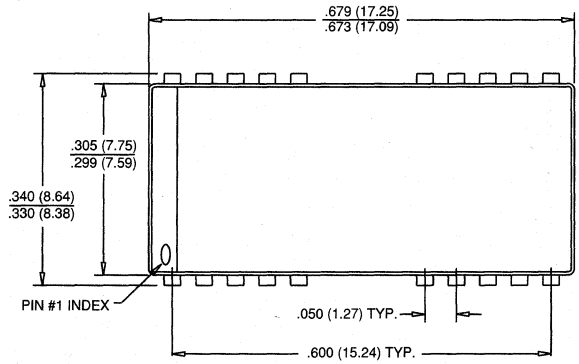


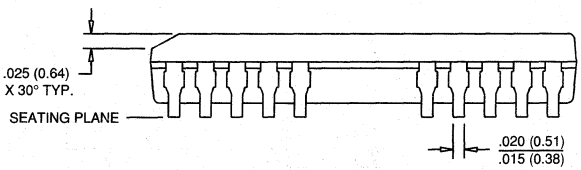
NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

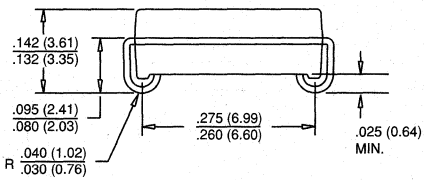
2. Package width and length do not include mold protrusion, allowable mold protrusion is .01" per side.

20/26-PIN PLASTIC SOJ (300 mil)

Q-1





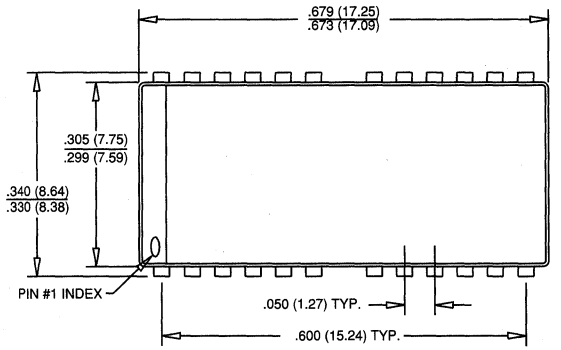


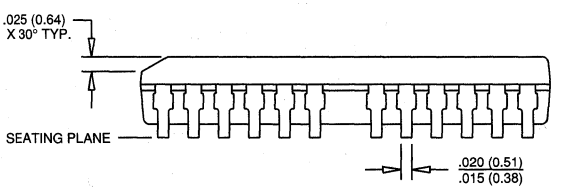
NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

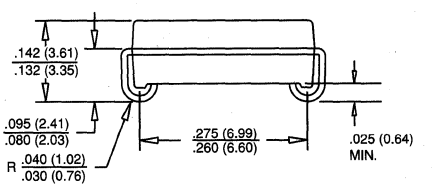
2. Package width and length do not include mold protrusion, allowable mold protrusion is .01" per side.

24/26-PIN PLASTIC SOJ (300 mil)

Q-2







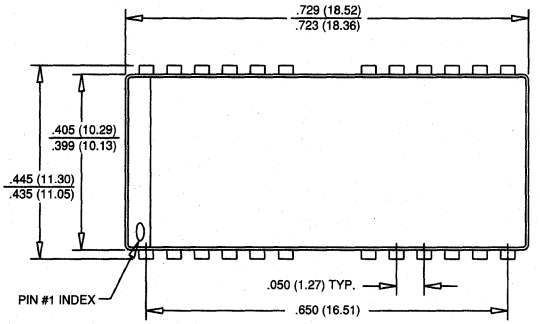
NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

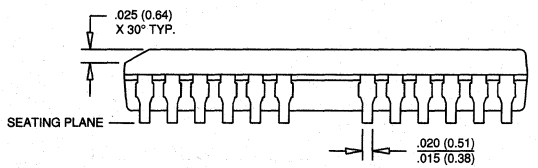
2. Package width and length do not include mold protrusion, allowable mold protrusion is .01" per side.

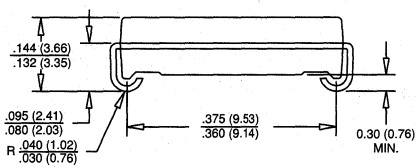
PACKAGE INFORMATION

24/28-PIN PLASTIC SOJ (400 mil)

Q-3





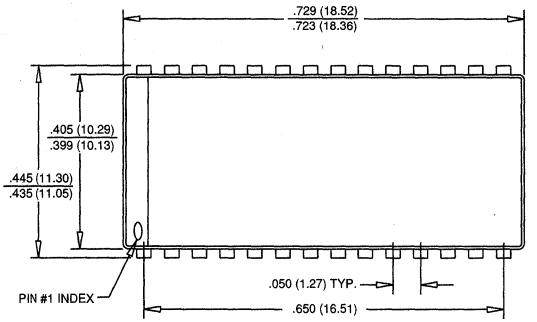


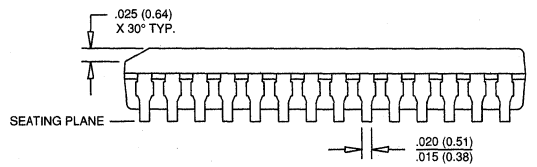
NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

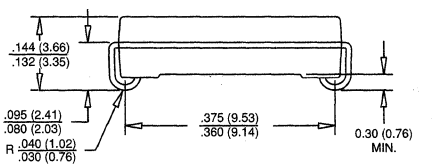
2. Package width and length do not include mold protrusion, allowable mold protrusion is .01" per side.

28-PIN PLASTIC SOJ (400 mil)

Q-4







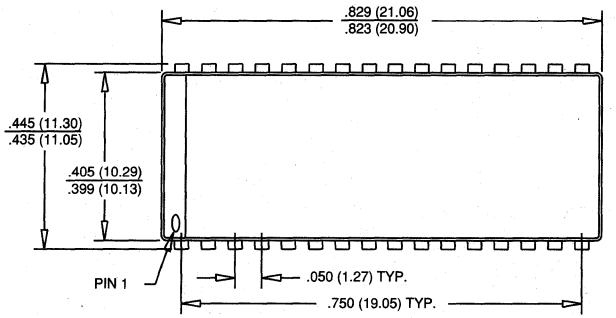
NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

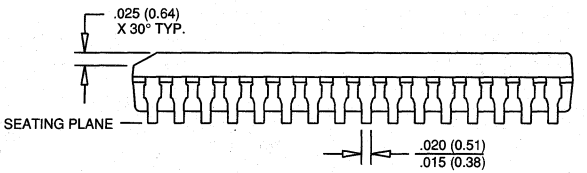
2. Package width and length do not include mold protrusion, allowable mold protrusion is .01" per side.

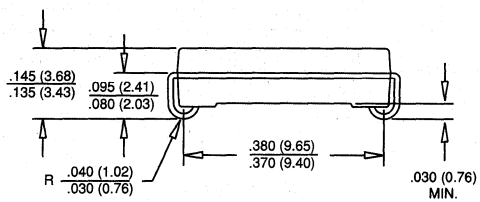
PACKAGE INFORMATION

32-PIN PLASTIC SOJ (400 mil)

Q-5





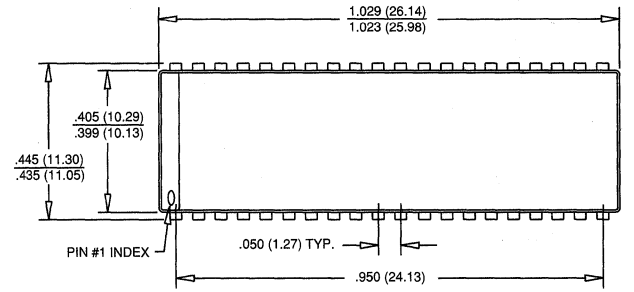


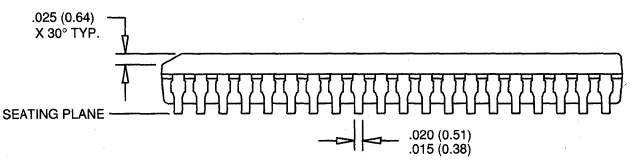
NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

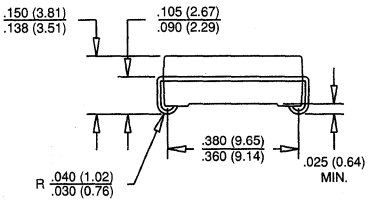
2. Package width and length do not include mold protrusion, allowable mold protrusion is .01" per side.

40-PIN PLASTIC SOJ (400 mil)

Q-6







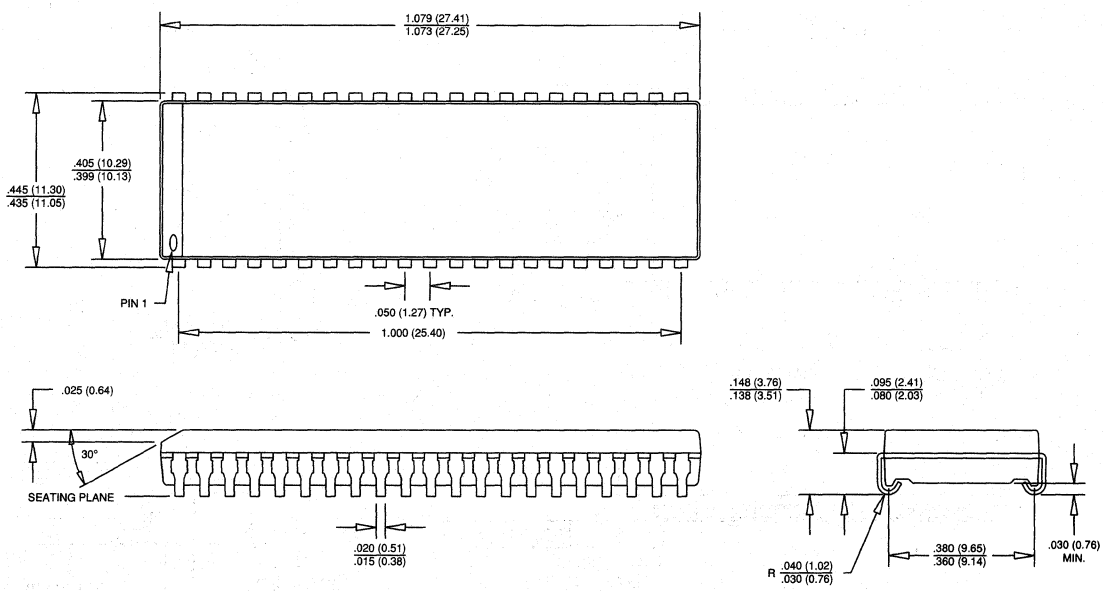
PACKAGE INFORMATION

NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

2. Package width and length do not include mold protrusion, allowable mold protrusion is .01" per side.

42-PIN PLASTIC SOJ (400 mil)

Q-7

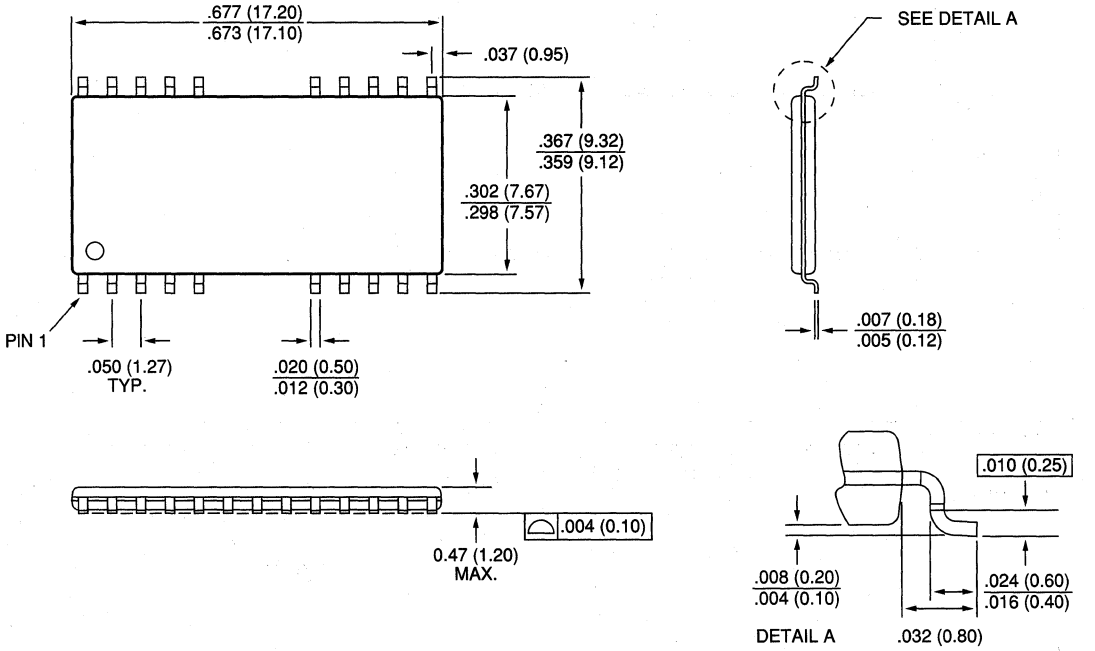


NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

2. Package width and length do not include mold protrusion, allowable mold protrusion is .01" per side.

20/26-PIN PLASTIC TSOP (300 mil)

R-1

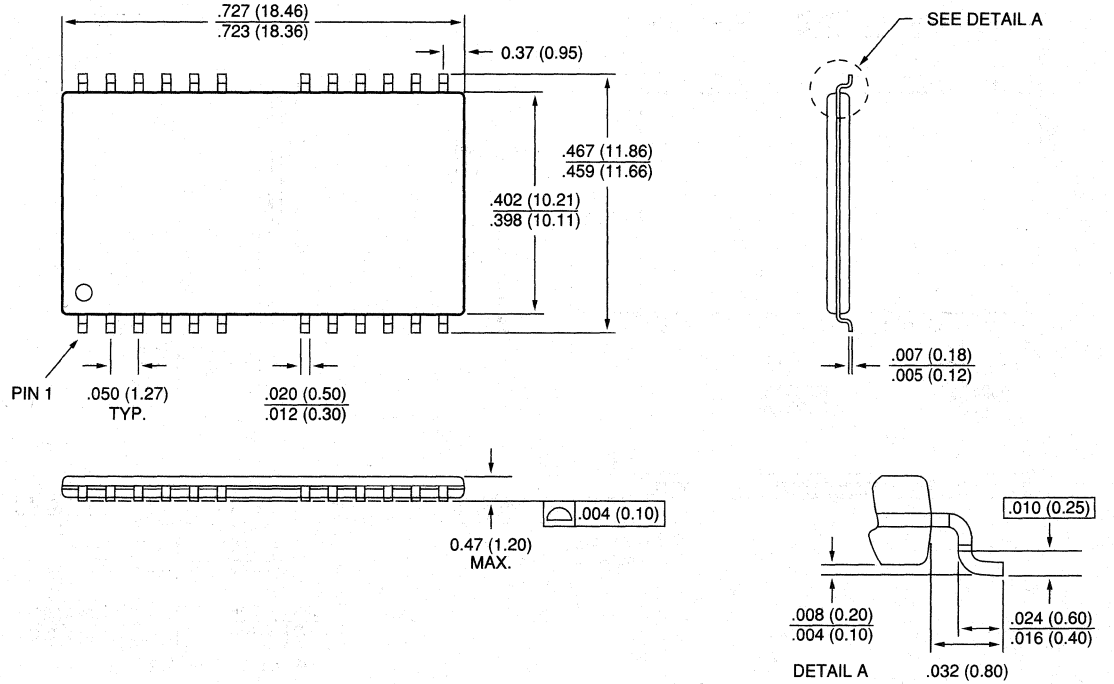


NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

2. Package width and length do not include mold protrusion, allowable mold protrusion is .01" per side.

24/28-PIN PLASTIC TSOP (400 mil)

R-2

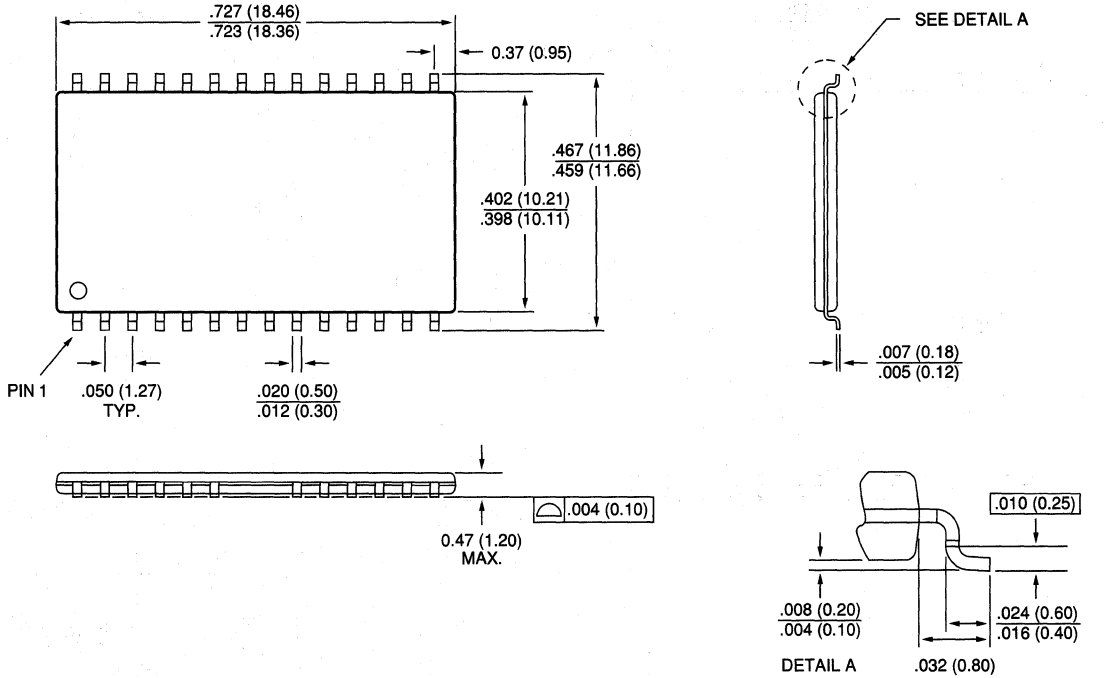


NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

2. Package width and length do not include mold protrusion, allowable mold protrusion is .01" per side.

28-PIN PLASTIC TSOP (400 mil)

R-3



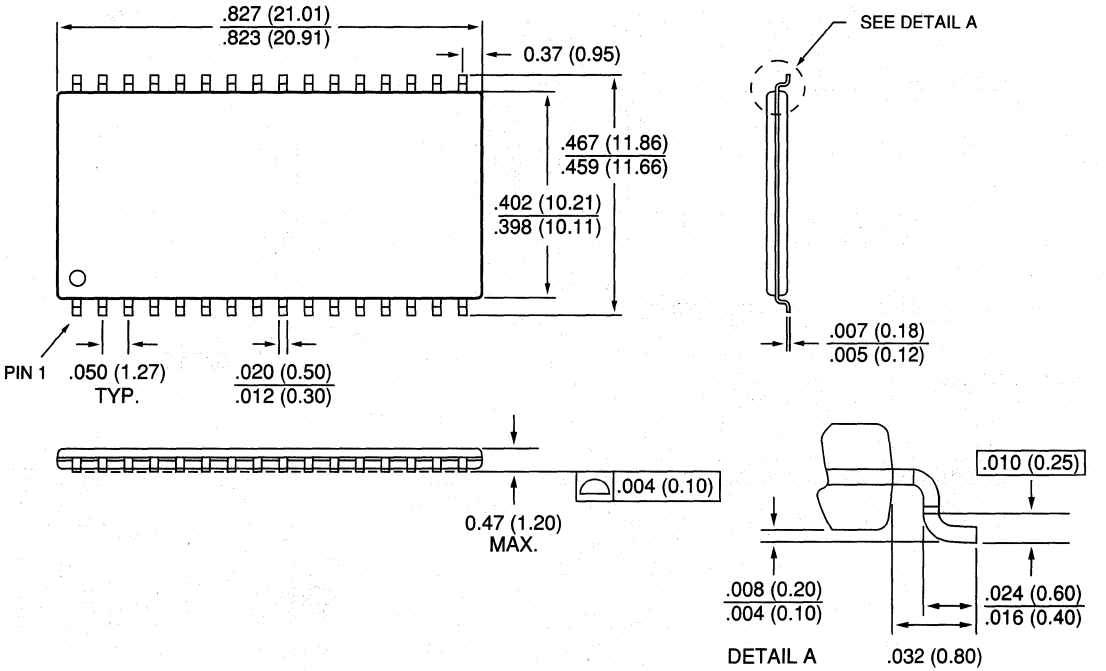
NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

2. Package width and length do not include mold protrusion, allowable mold protrusion is .01" per side.

PACKAGE INFORMATION

32-PIN PLASTIC TSOP (400 mil)

R-4

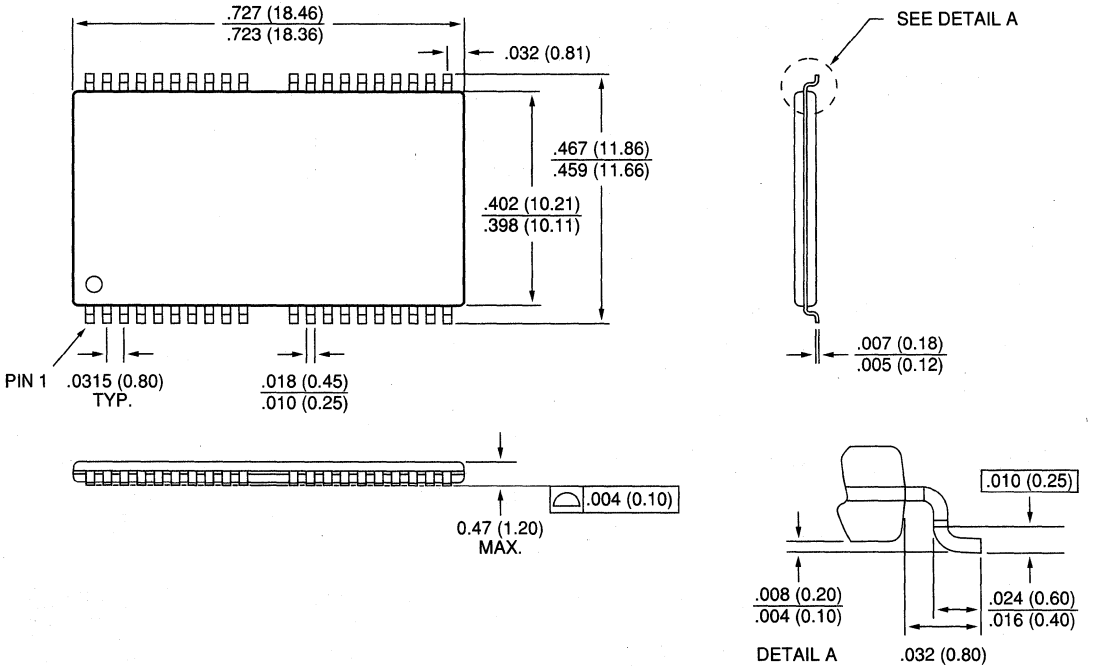


NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

2. Package width and length do not include mold protrusion, allowable mold protrusion is .01" per side.

40/44-PIN PLASTIC TSOP (400 mil)

R-5



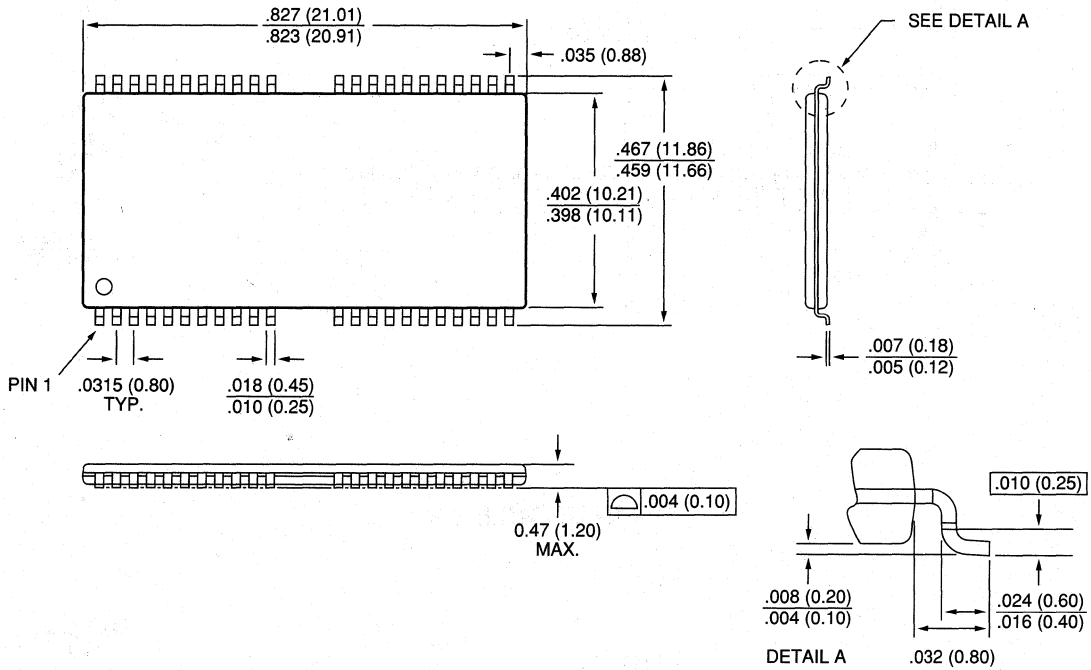
NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

2. Package width and length do not include mold protrusion, allowable mold protrusion is .01" per side.

PACKAGE INFORMATION

44/50-PIN PLASTIC TSOP (400 mil)

R-6



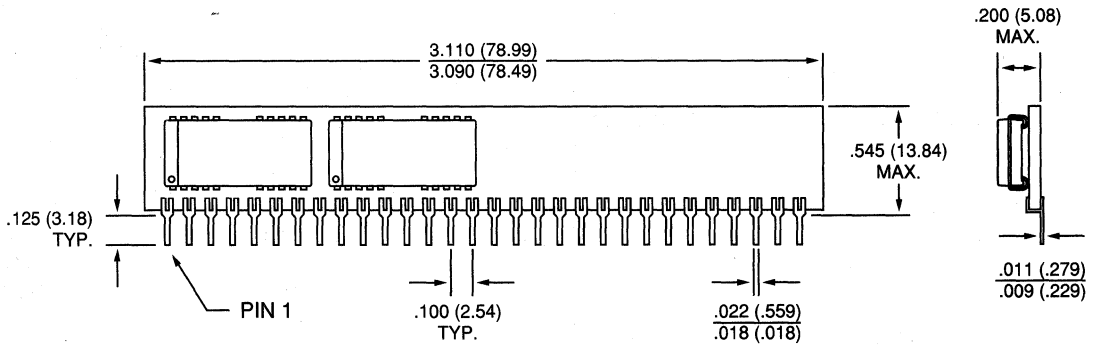
NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

2. Package width and length do not include mold protrusion, allowable mold protrusion is .01" per side.

PACKAGE INFORMATION

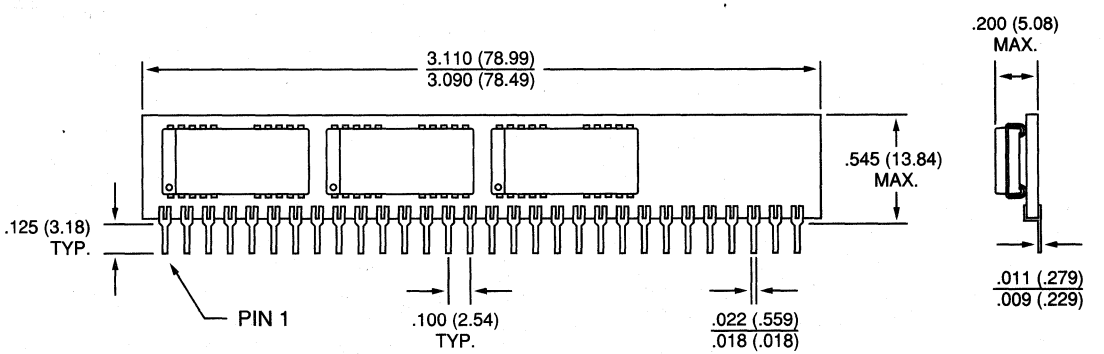
30-PIN MODULE SIP

S-1



30-PIN MODULE SIP

S-2

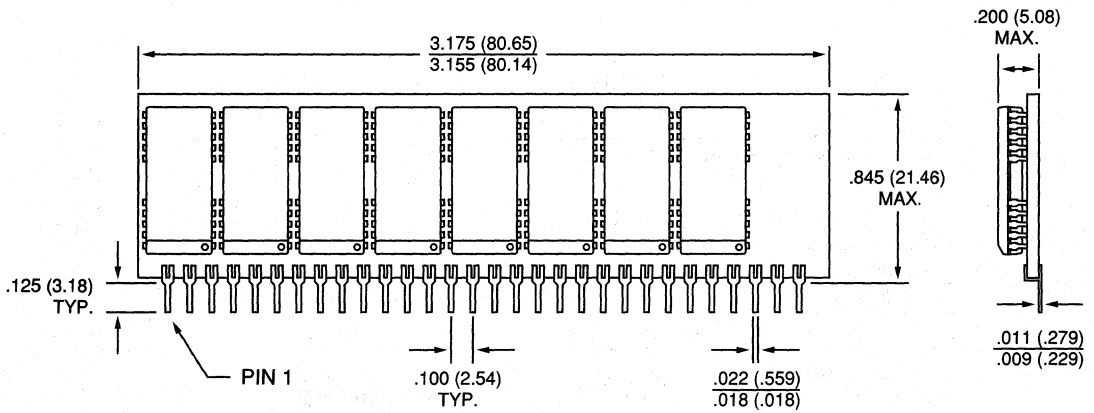


PACKAGE INFORMATION

NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

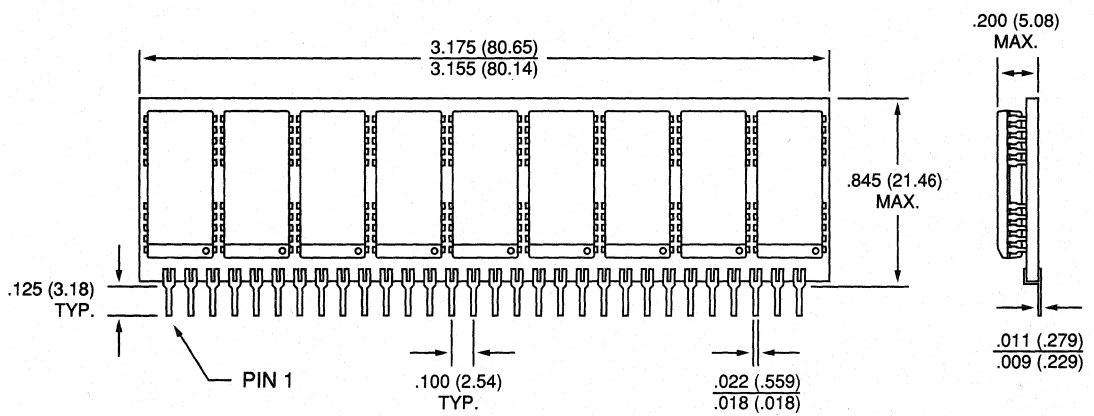
30-PIN MODULE SIP

S-3



30-PIN MODULE SIP

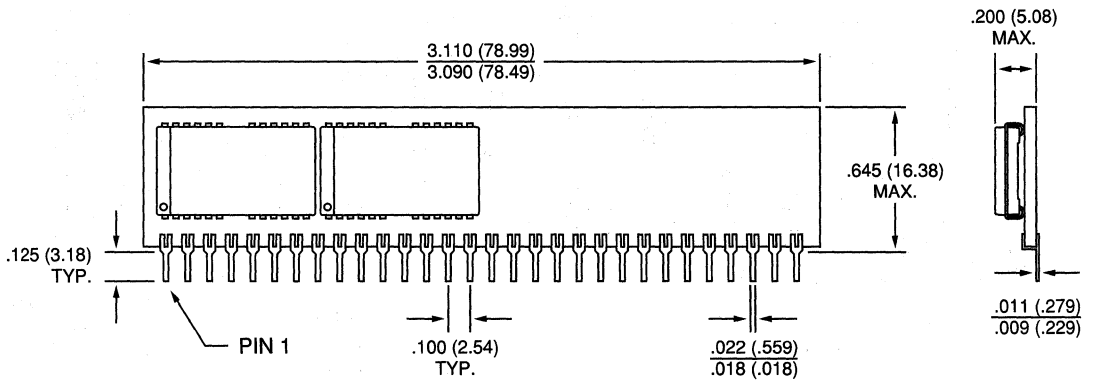
S-4



NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

30-PIN MODULE SIP

S-5

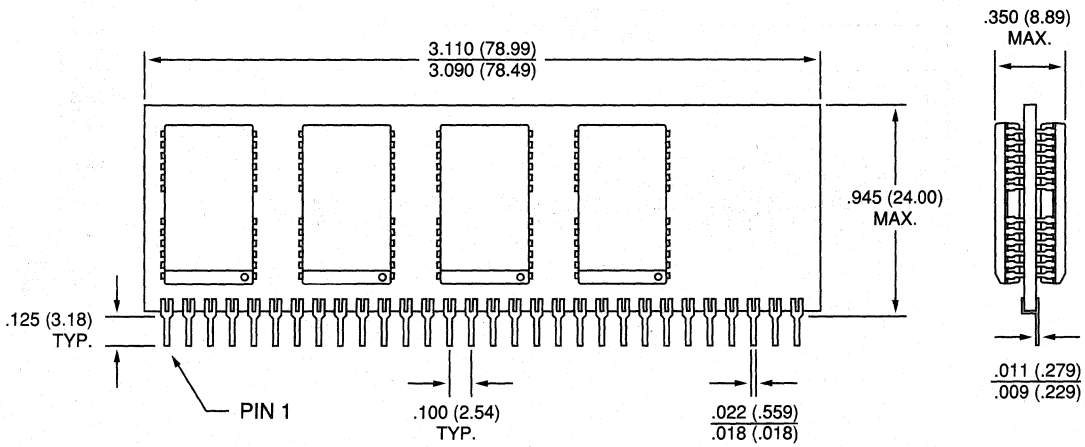


NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

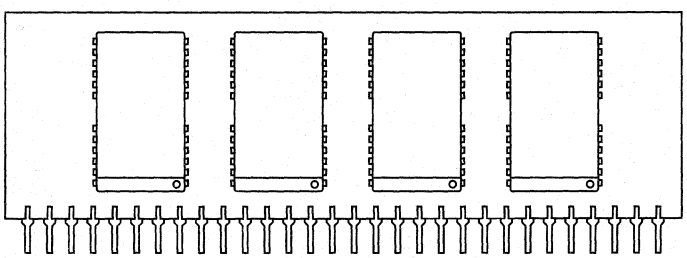
30-PIN MODULE SIP

S-6

FRONT VIEW



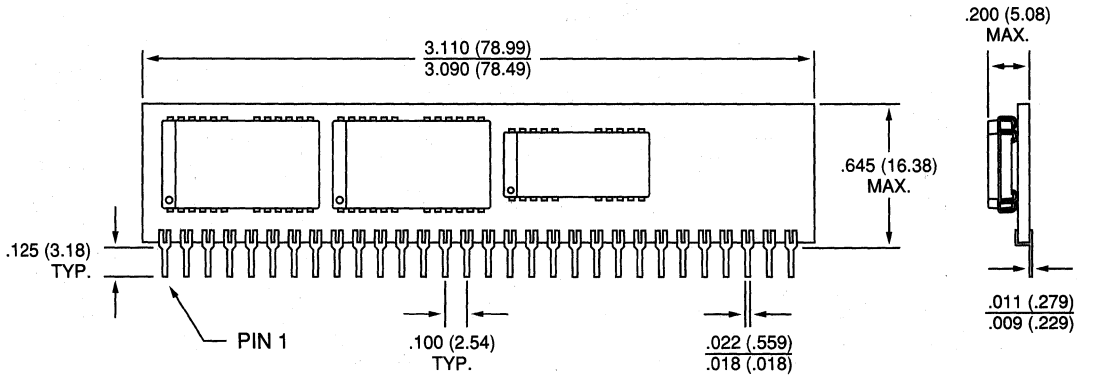
BACK VIEW



NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

30-PIN MODULE SIP

S-7

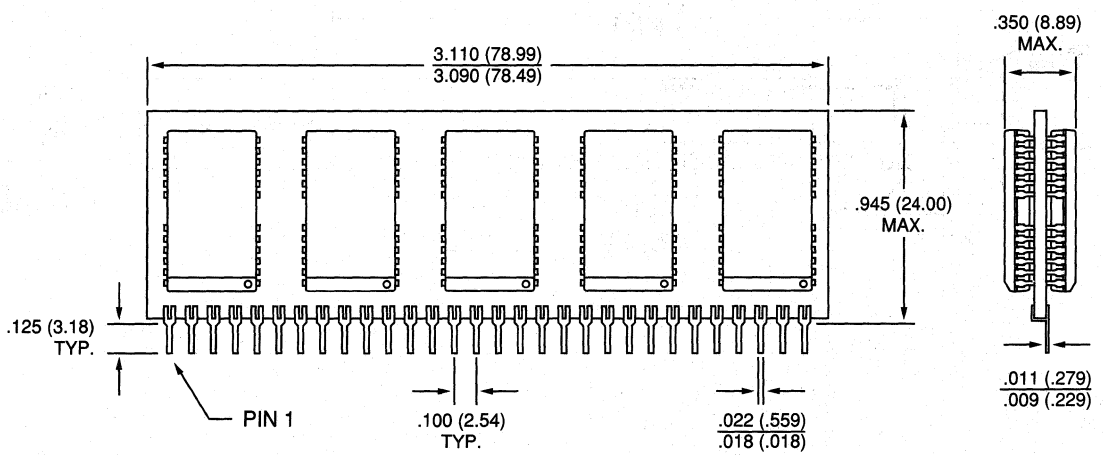


NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

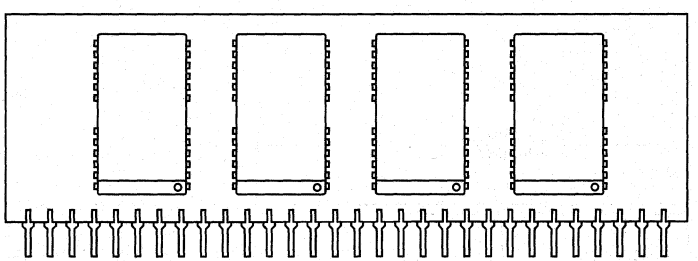
30-PIN MODULE SIP

S-8

FRONT VIEW



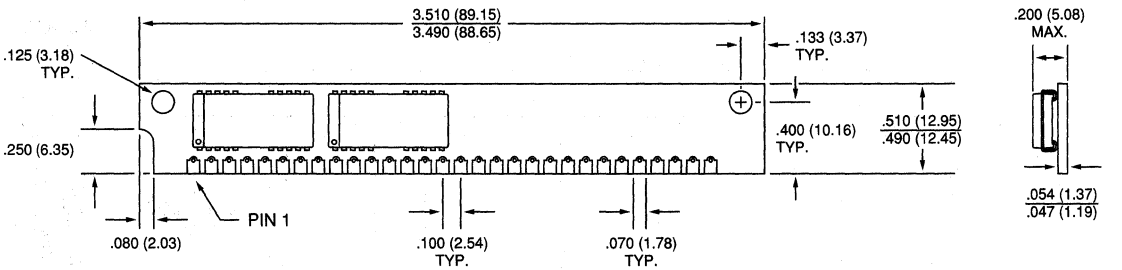
BACK VIEW



NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

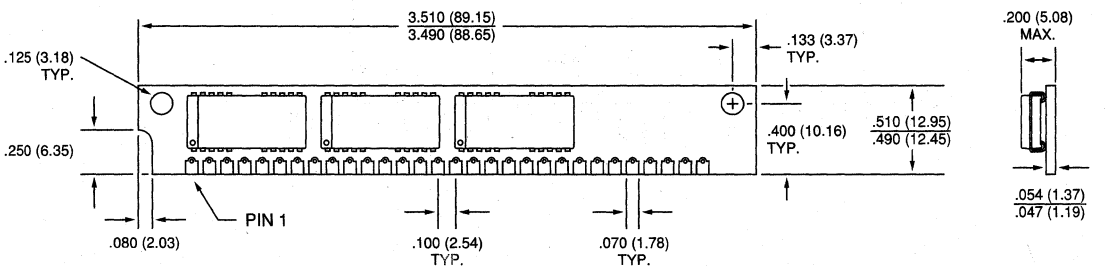
30-PIN MODULE SIMM

T-1



30-PIN MODULE SIMM

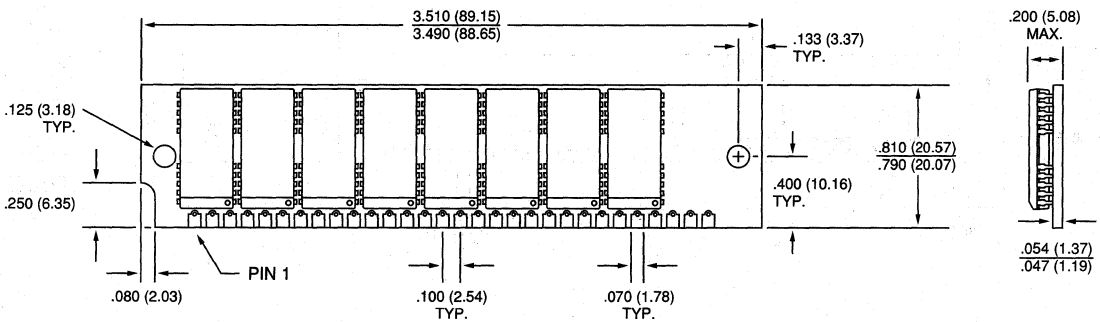
T-2



NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

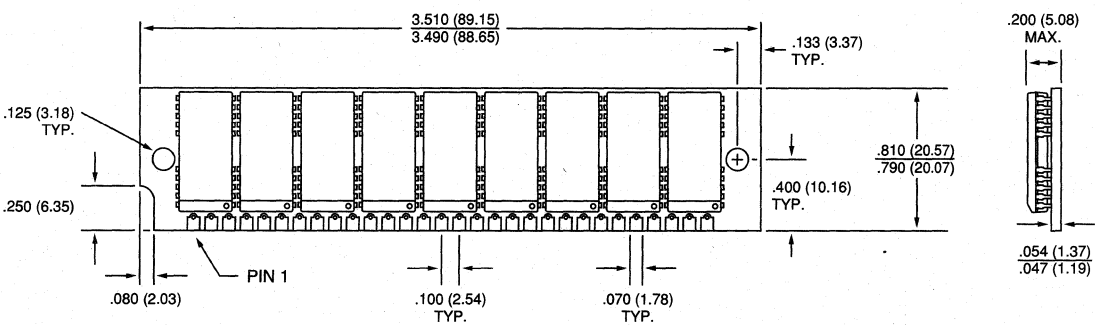
30-PIN MODULE SIMM

T-3



30-PIN MODULE SIMM

T-4

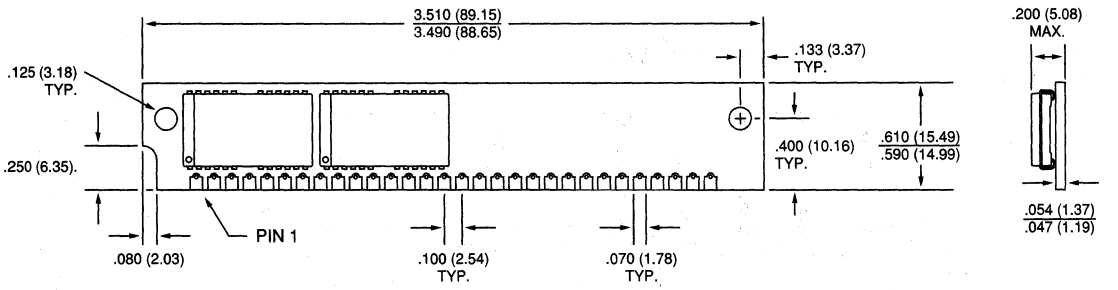


NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

PACKAGE INFORMATION

30-PIN MODULE SIMM

T-5



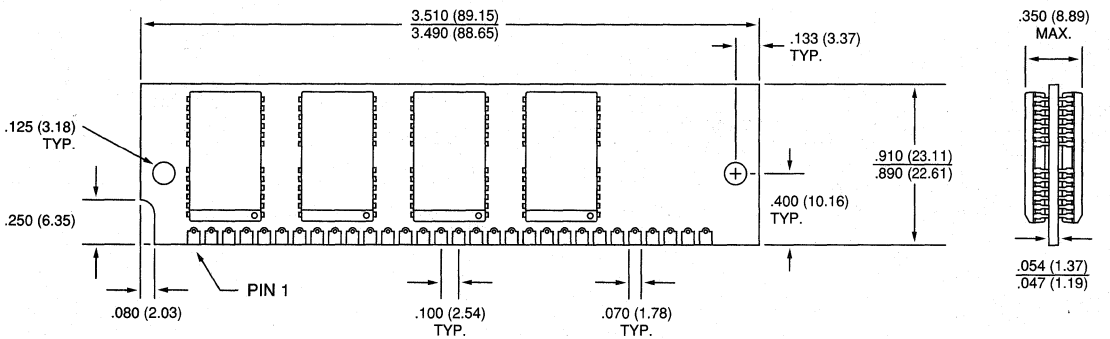
PACKAGE INFORMATION

NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

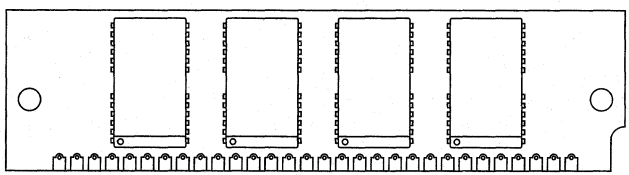
30-PIN MODULE SIMM

T-6

FRONT VIEW



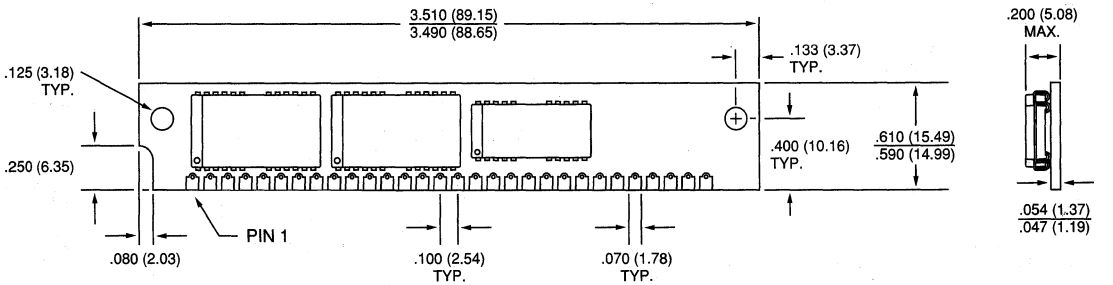
BACK VIEW



NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

30-PIN MODULE SIMM

T-7

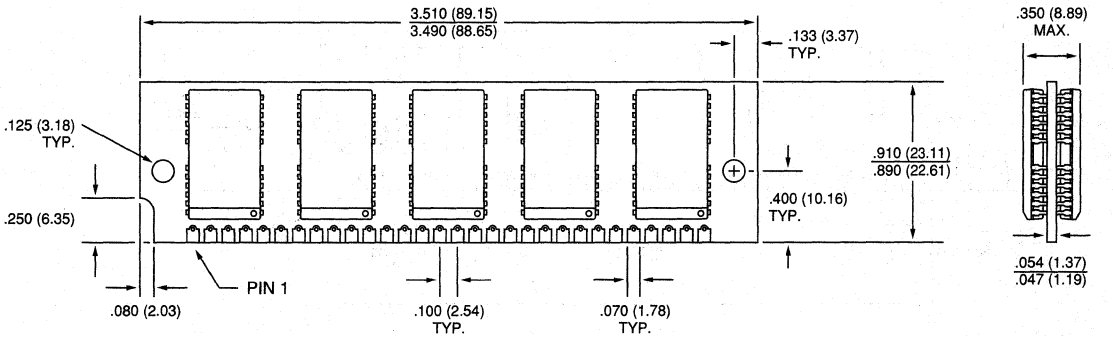


NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

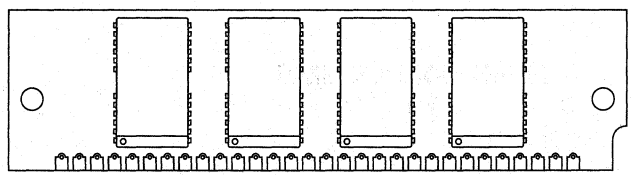
30-PIN MODULE SIMM

T-8

FRONT VIEW



BACK VIEW

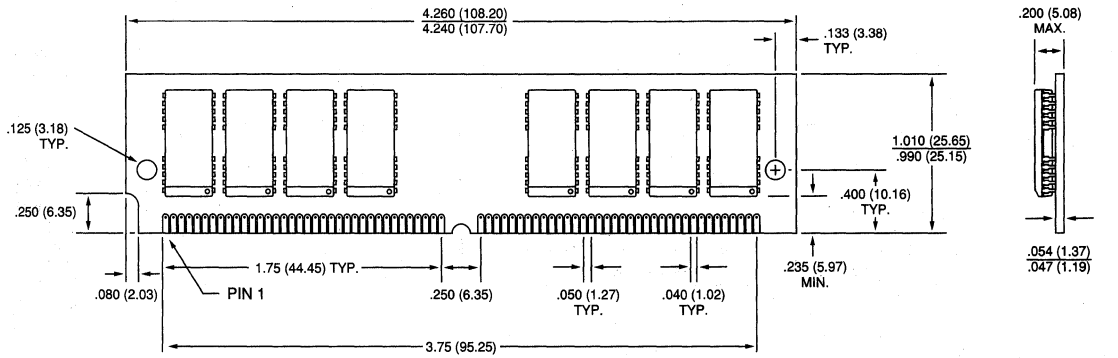


NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

PACKAGE INFORMATION

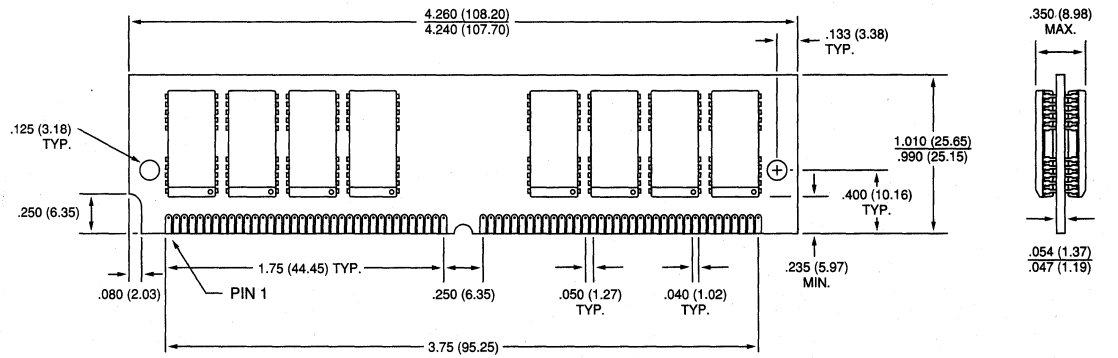
72-PIN MODULE SIMM

T-9



72-PIN MODULE SIMM

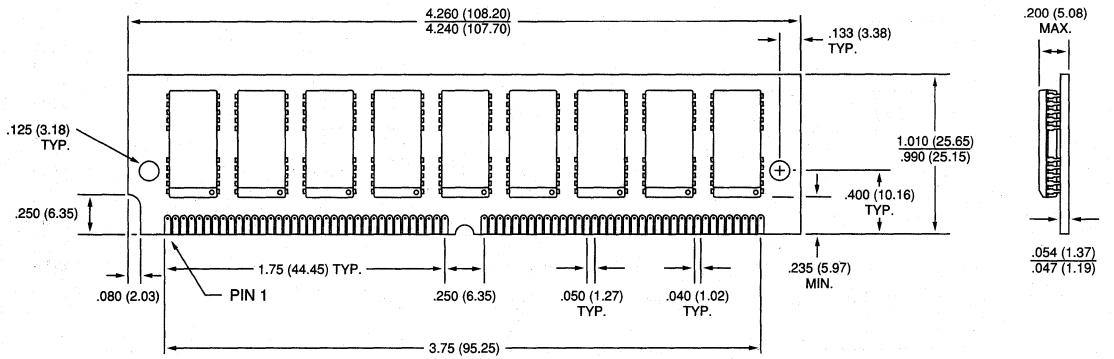
T-10



NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

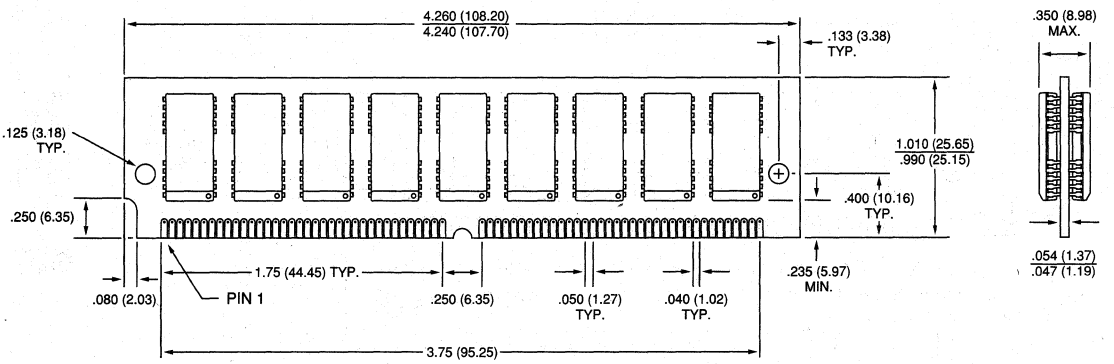
72-PIN MODULE SIMM

T-11



72-PIN MODULE SIMM

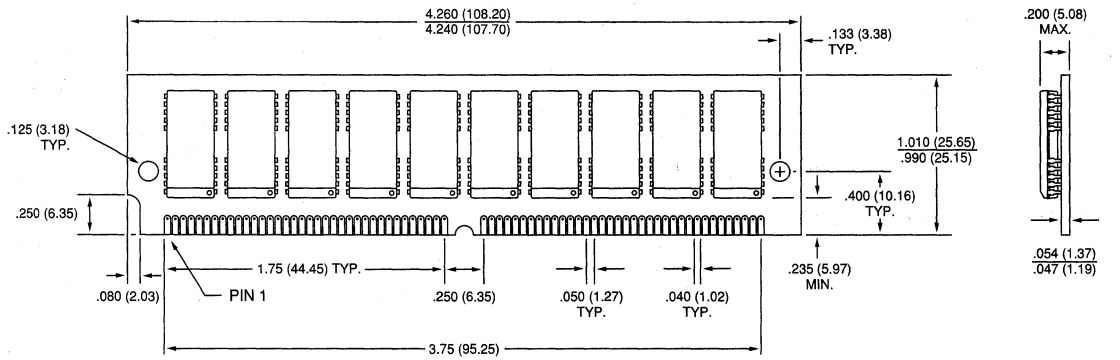
T-12



NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

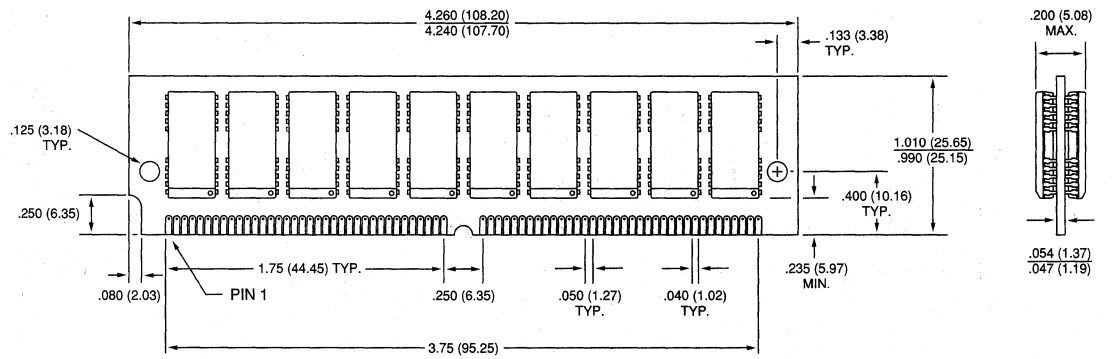
72-PIN MODULE SIMM

T-13



72-PIN MODULE SIMM

T-14

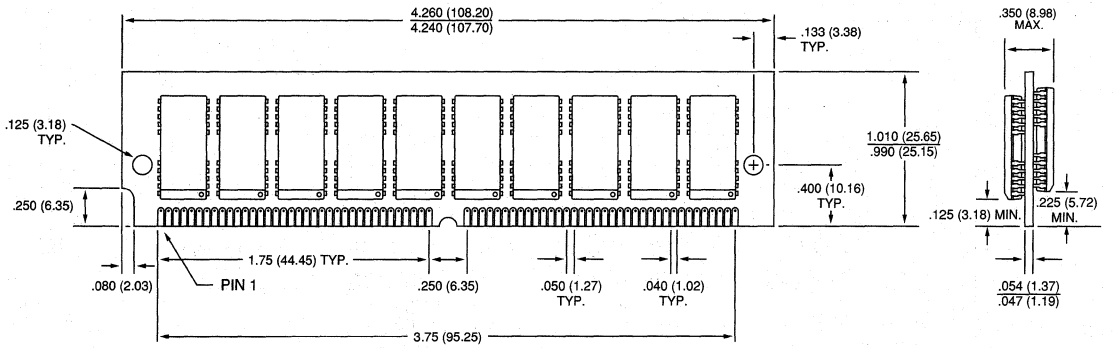


PACKAGE INFORMATION

NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

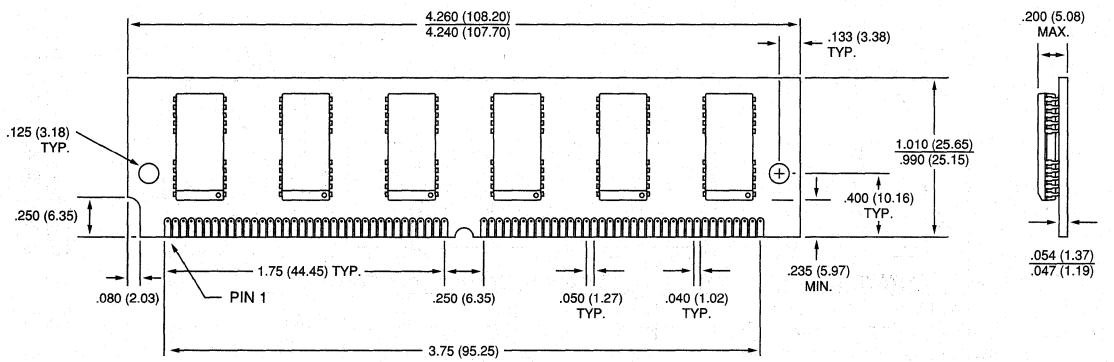
72-PIN MODULE SIMM

T-15



72-PIN MODULE SIMM

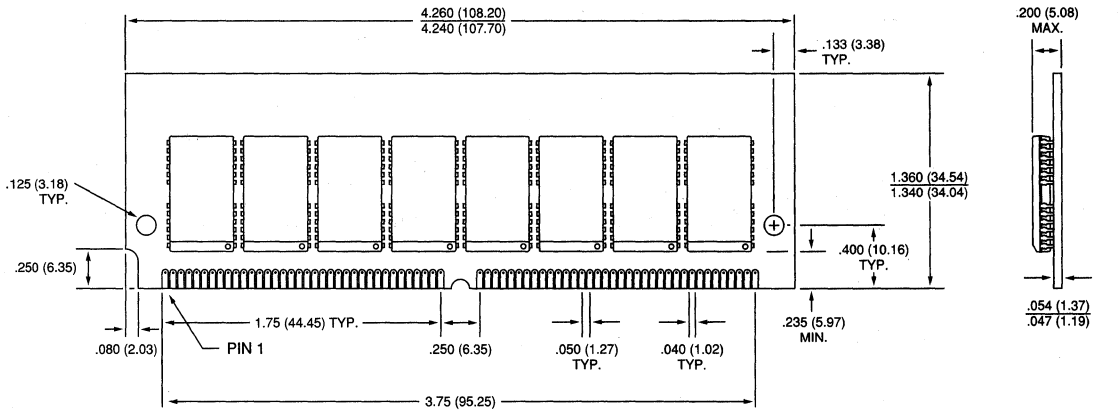
T-16



NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

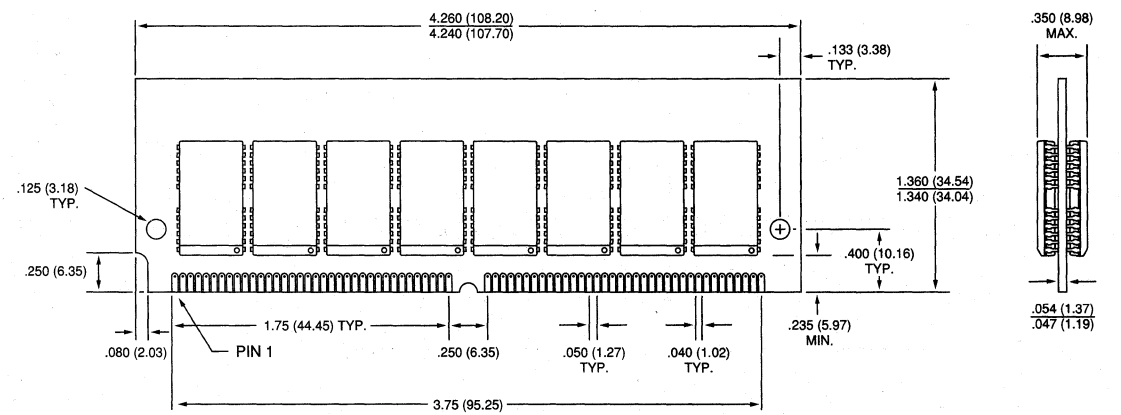
72-PIN MODULE SIMM

T-17



72-PIN MODULE SIMM

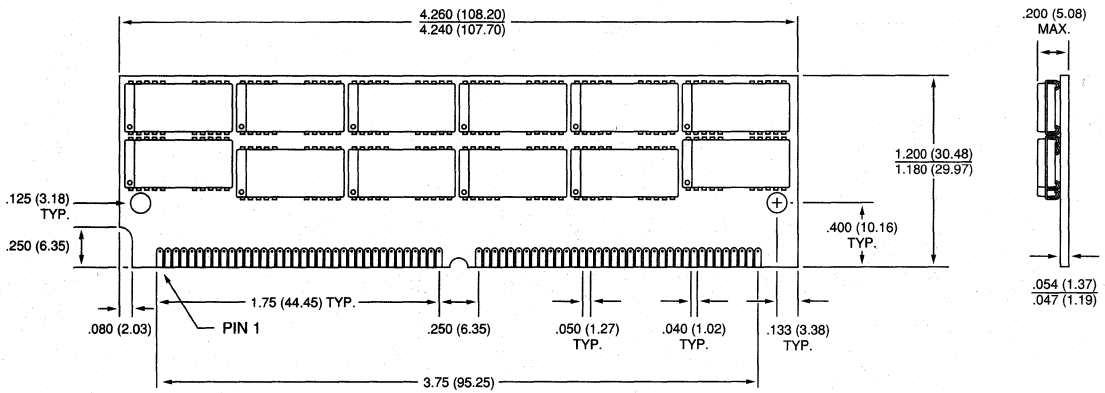
T-18



NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

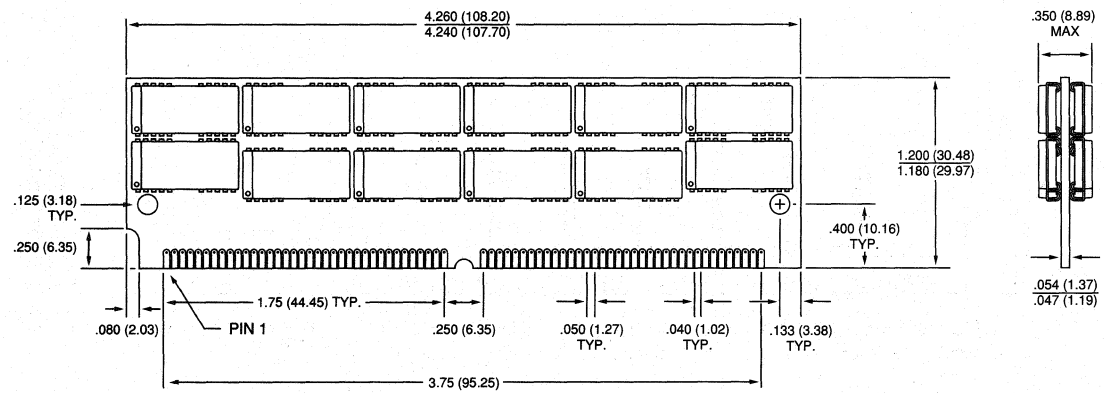
72-PIN MODULE SIMM

T-19



72-PIN MODULE SIMM

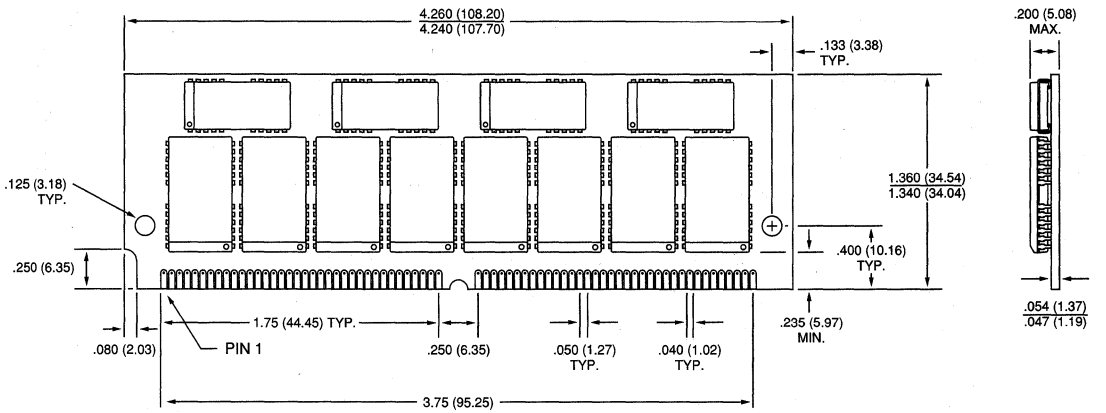
T-20



NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

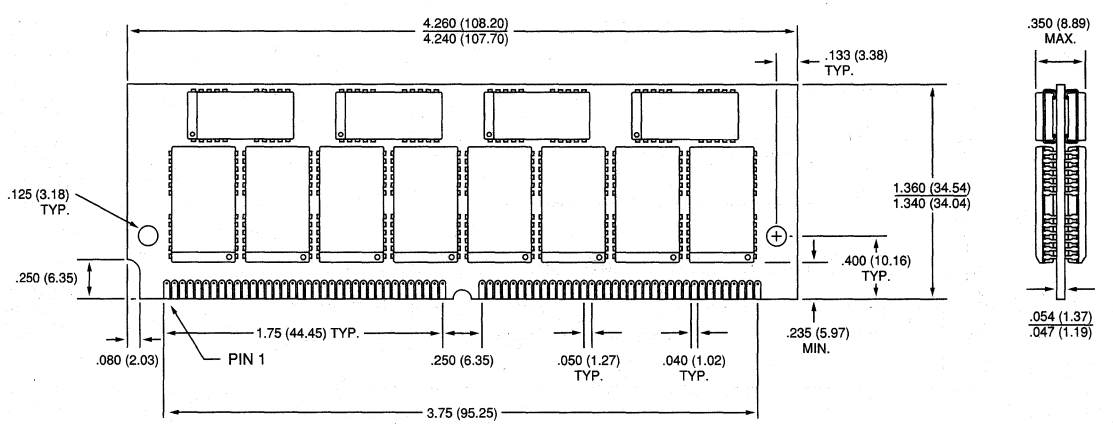
72-PIN MODULE SIMM

T-21



72-PIN MODULE SIMM

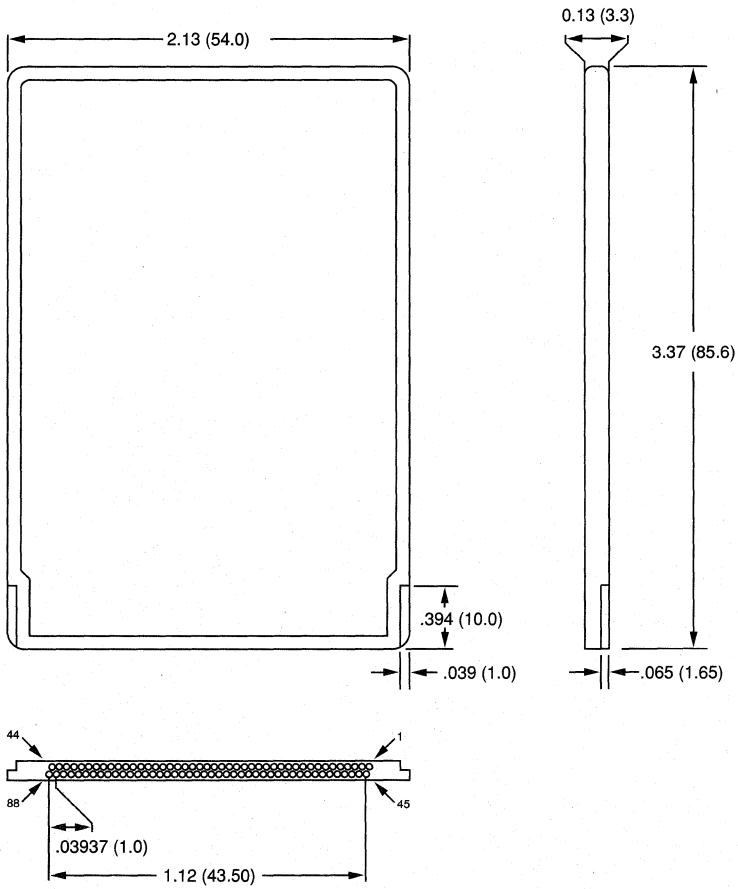
T-22



NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

88-PIN IC DRAM CARD

U-1



NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

MICRON TECHNOLOGY, INC.

DYNAMIC RAMS 1

WIDE DRAMS 2

DRAM MODULES 3

IC DRAM CARDS 4

MULTIPORT DRAMS 5

APPLICATION/TECHNICAL NOTES 6

PRODUCT RELIABILITY 7

PACKAGE INFORMATION 8

SALES INFORMATION 9

CUSTOMER SERVICE NOTE

STANDARD SHIPPING BAR CODE LABELS

INTRODUCTION

Effective July 1, 1991, Micron Technology implemented new standard bar coding labels which will accompany all shipments. These labels conform to EIA Standard 556.

Samples and tape-and-reel boxes have their own individual bar code labels (see CSN-02). The bar code labels allow customers to scan individual Micron containers for quick order verification. Figure 1 shows an example of the standard bar coding label.

BAR CODE INFORMATION

The information provided on the label is:

(S) — Serial: Individual box serial number

(13Q) — Special: Individual box number and total number of boxes in the shipment (example: 2 of 10)

(Q) — Quantity: Total quantity of parts in the box

(K) — Trans ID: Customer purchase order number

(P) — Customer Product ID: Customer part number. If a customer part number is not designated, the Micron part number will be printed.

ADDITIONAL SALES INFORMATION

Ship-to-Name: Customer's name and ship-to address

Ship-From-Name: Micron name and address

Lot Date Code: Indicates date of oldest lot in the box

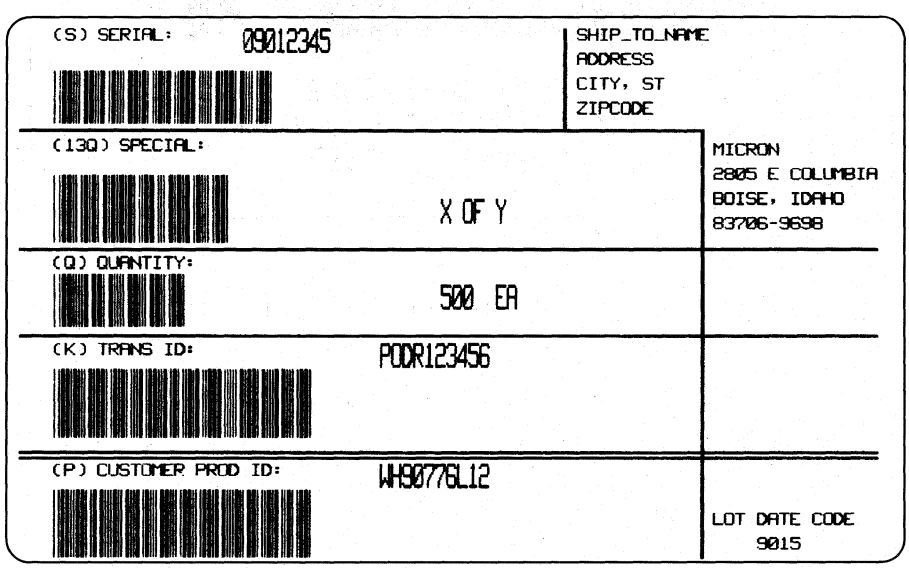


Figure 1
STANDARD BAR CODE LABEL

SALES INFORMATION

CUSTOMER SERVICE NOTE

TAPE-AND-REEL/SAMPLE BAR CODE LABELS

INTRODUCTION

Micron Technology provides a standard bar code label on each individual sample and tape-and-reel box. The standard bar code label allows scanning of Micron shipping containers at a receiving dock for quick order verification.

Figure 1 shows an example of the standard bar code label.

BAR CODE INFORMATION

The information provided on the label is:

Label 1: Individual box number (in a multi-box shipment)
Actual box number printed
Micron part number/speed/customer code
Part type/rev/quantity/date code of oldest lot*

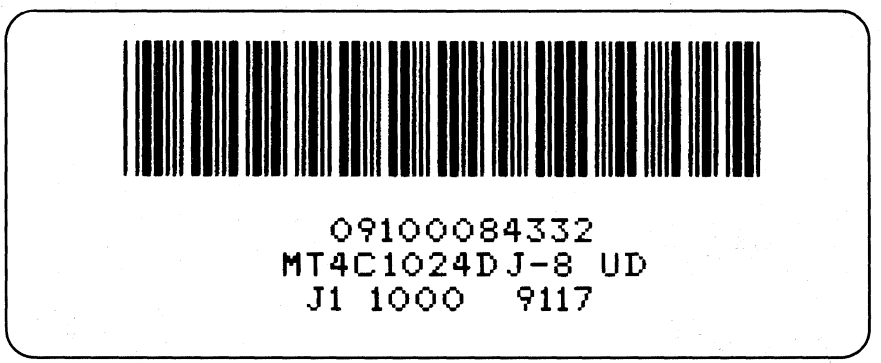


Figure 1
LABEL 1

*Indicates that more than one date code is contained on the reel.

CUSTOMER SERVICE NOTE

SURFACE-MOUNT PRODUCTS' SPC LABELS

INTRODUCTION

Effective November 15 1991, Micron Technology began providing a new SPC label on all surface-mount products. The label is attached to the static column bag for tubed products and to the front of the bag for tape-and-reel packaged products.

Figure 1 shows an example of the standard SPC label, while Figures 2 and 3 show the difference between the labels for tubed and tape-and-reel packaged products.

DATE INFORMATION

The SPC label includes the date on which the tube or reel was hermetically sealed in drypack. It also lists the ID number of the operator who sealed the product.

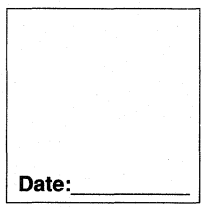


Figure 1
SURFACE-MOUNT PRODUCT SPC LABEL

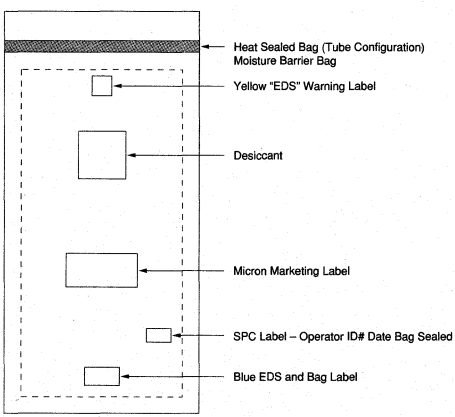


Figure 2
TUBED PRODUCT LABEL

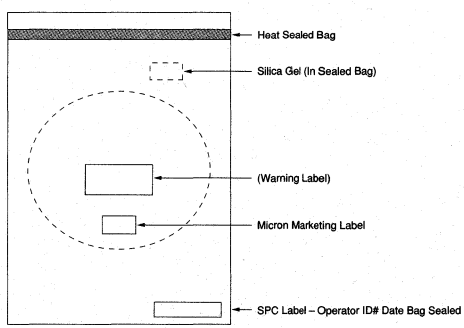
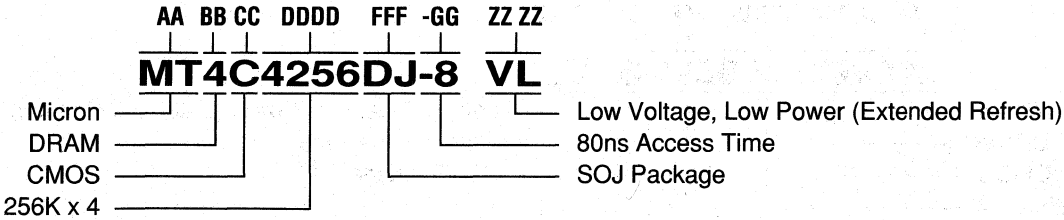


Figure 3
TAPE-AND-REEL PACKAGED PRODUCT LABEL

SALES INFORMATION

EXPANDED COMPONENT NUMBERING SYSTEM



AA – PRODUCT LINE IDENTIFIER

Component Product	MT

BB – PRODUCT FAMILY

DRAM	4
DPDRAM	42
TPDRAM	43
SRAM	5
FIFO	52
Cache Data SRAM	56
Synchronous SRAM	58

CC – PROCESS TECHNOLOGY

CMOS	C
Low Voltage CMOS	LC

DDDD – DEVICE NUMBER

(Can be modified to indicate variations)

DRAM	Width, Density
DPDRAM	Width, Density
TPDRAM	Width, Density
SRAM	Total Bits, Width
CACHE	Density, Width
Latched SRAM	Total Bits, Width
FIFO	Width, Total Bits
Synchronous SRAM	Density, Width

E – DEVICE VERSIONS

(Alphabetic characters only; located between D and F when required)

JEDEC Test Mode (4 Meg DRAM)	J
Errata on Base Part	Q

FFF – PACKAGE CODES

PLASTIC	
DIP	Blank
DIP (Wide Body)	W
ZIP	Z
LCC	EJ
SOP/SOIC	SG

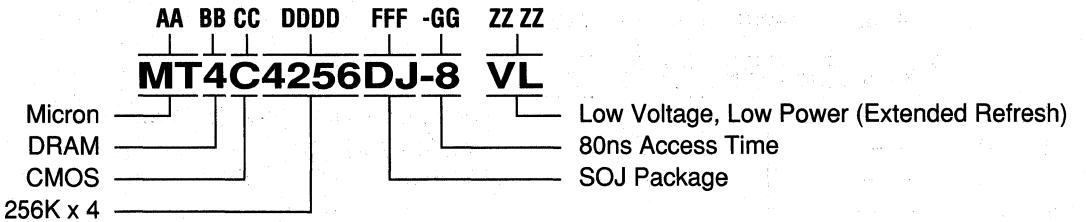
FFF – PACKAGE CODES (continued)

QFP	LG
TSOP (Type II)	TG
TSOP (Reversed)	RG
TSOP (Longer)	TL
SOJ	DJ
SOJ (Reversed)	DR
SOJ (Longer)	DL
DIE	
Die	XDC
Wafer	XWC
Military Die	XD
Military Wafer	XW
Ceramic	
DIP	C
DIP (Narrow Body)	CN
DIP (Wide Body)	CW
LCC	EC
LCC (Narrow Body)	ECN
LCC (Wide Body)	ECW
SOP/SOIC	CG
SOJ	DCJ
PGA	CA
FLAT PACK	F

GG – ACCESS TIME

-5	5ns or 50ns
-6	6ns or 60ns
-7	7ns or 70ns
-8	8ns or 80ns
-10	10ns or 100ns
-12	12ns or 120ns
-15	15ns or 150ns
-17	17ns
-20	20ns
-25	25ns
-35	35ns
-45	45ns
-50 (SRAM only)	50ns
-53	53ns

EXPANDED COMPONENT NUMBERING SYSTEM (continued)



GG – ACCESS TIME (continued)

-55 ..... 55ns
-70 (SRAM only) 70ns

ZZ ZZ – PROCESSING CODES

(Multiple processing codes are separated by a space and are listed in hierarchical order).

Example:
A DRAM supporting low power, extended refresh (L); low voltage (V) and the industrial temperature range (IT) would be indicated as:
V L IT

Interim I
Low Voltage V
DRAMS
- Low Power (Extended Refresh) L
- Low Voltage, Low Power (Extended Refresh) VL
- Low Power (Self Refresh) ..... S
- Low Voltage, Low Power (Self Refresh) ..... VS

SRAMS
- Low Volt Data Retention L
- Low Power ..... P
- Low Power, Low Volt Data Retention ..... LP
- Low Voltage, Low Power ..... VP

ZZ ZZ – PROCESSING CODES (continued)

- Low Voltage, Low Volt Data Retention VL
- Low Voltage, Low Volt Data Retention, Low Power ..... VB

EPI Wafer ..... E

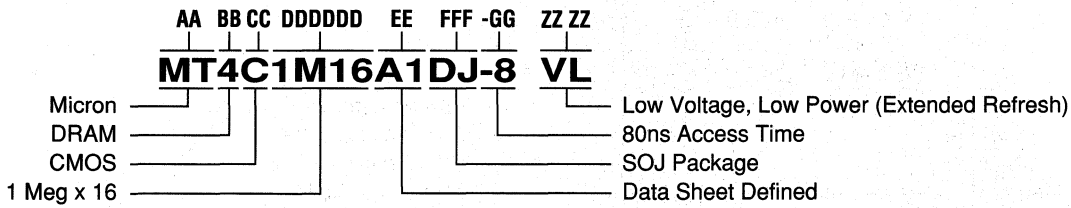
Commercial Testing
- 0°C to +70°C ..... Blank
- -40°C to +85°C ..... IT
- -40°C to +125°C ..... AT
- -55°C to +125°C ..... XT

MIL-STD-883C Testing
- -55°C to +125°C 883C
- -55°C to +110°C (DRAMs) 883C
- 0°C to +70°C M070

Special Processing
- Engineering Sample ..... ES
- Mechanical Sample ..... MS
- Sample Kit* ..... SK
- Tape and Reel* ..... TR
- Bar Code* ..... BC

* Used in device order codes; this code is not marked on device.

NEW COMPONENT NUMBERING SYSTEM



AA – PRODUCT LINE IDENTIFIER

Component Product ..... MT

BB – PRODUCT FAMILY

DRAM 4
DPDRAM 42
TPDRAM 43
Synchronous DRAM 48
SRAM 5
FIFO 52
Latched SRAM 56
Synchronous SRAM 58

CC – PROCESS TECHNOLOGY

CMOS C
Low Voltage CMOS LC

DDDDDD – DEVICE NUMBER

Depth, Width

Example:
1M16 = 1 Megabit deep by 16 bits wide = 16 Megabits of total memory

No Letter ..... Bits
K ..... Kilobits
M ..... Megabits
G ..... Gigabits

EE – DEVICE VERSIONS

(The first character is an alphabetic character only; the second character is a numeric character only.)
Specified by individual data sheet

FFF – PACKAGE CODES

Plastic
DIP ..... Blank
DIP (Wide Body) ..... W
ZIP ..... Z
LCC ..... EJ
SOP/SOIC ..... SG

FFF – PACKAGE CODES (continued)

QFP ..... LG
TSOP (Type II) ..... TG
TSOP (Reversed) ..... RG
TSOP (Longer) ..... TL
SOJ ..... DJ
SOJ (Reversed) ..... DR
SOJ (Longer) ..... DL

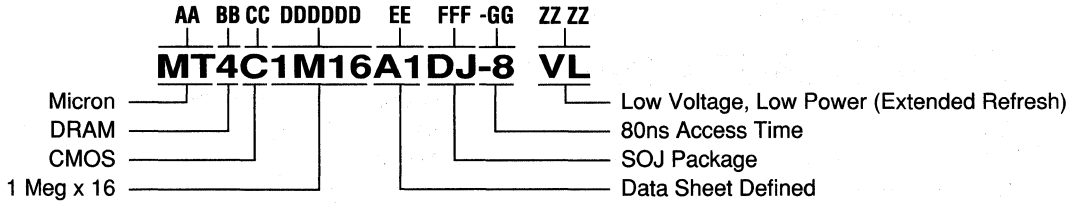
DIE
Die ..... XDC
Wafer ..... XWC
Military Die ..... XD
Military Wafer ..... XW

CERAMIC
DIP C
DIP (Narrow Body) ..... CN
DIP (Wide Body) ..... CW
LCC (Narrow Body) ..... ECN
LCC ..... EC
LCC (Wide Body) ..... ECW
SOP/SOIC ..... CG
SOJ ..... DCJ
PGA ..... CA
FLAT PACK ..... F

GG – ACCESS TIME

-5 ..... 5ns or 50ns
-6 ..... 6ns or 60ns
-7 ..... 7ns or 70ns
-8 ..... 8ns or 80ns
-10 ..... 10ns or 100ns
-12 ..... 12ns or 120ns
-15 ..... 15ns or 150ns
-17 ..... 17ns
-20 ..... 20ns
-25 ..... 25ns
-35 ..... 35ns
-45 ..... 45ns
-50 (SRAM only) 50ns

NEW COMPONENT NUMBERING SYSTEM (continued)



GG – ACCESS TIME (continued)

-53 ..... 53ns
-55 ..... 55ns
-70 (SRAM only) 70ns

ZZ ZZ – PROCESSING CODES

(Multiple processing codes are separated by a space and are listed in hierarchical order.)

Example:
A DRAM supporting low power, extended refresh (L); low voltage (V) and the industrial temperature range (IT) would be indicated as:
V L IT

Interim I
Low Voltage V
DRAMs
- Low Power (Extended Refresh) L
- Low Voltage, Low Power (Extended Refresh) VL
- Low Power (Self Refresh) ..... S
- Low Voltage, Low Power (Self Refresh) ..... VS

SRAMs
- Low Volt Data Retention L
- Low Power ..... P
- Low Power, Low Volt Data Retention ..... LP
- Low Voltage, Low Power ..... VP

ZZ ZZ – PROCESSING CODES (continued)

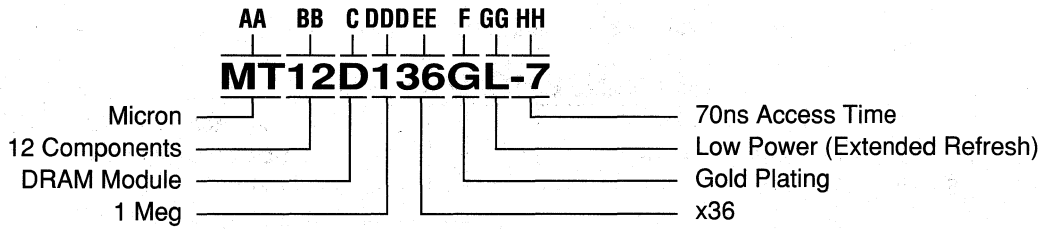
Low Voltage, Low Volt Data Retention VL
Low Voltage, Low Volt Data Retention, Low Power ..... VB
EPI Wafer ..... E
Commercial Testing
- 0°C to +70°C ..... Blank
- -40°C to +85°C ..... IT
- -40°C to +125°C ..... AT
- -55°C to +125°C ..... XT

MIL-STD-883C Testing
- -55°C to +125°C 883C
- -55°C to +110°C (DRAMs) 883C
- 0°C to +70°C M070

Special Processing
- Engineering Sample ..... ES
- Mechanical Sample ..... MS
- Sample Kit* ..... SK
- Tape and Reel* ..... TR
- Bar Code* ..... BC

* Used in device order codes; this code is not marked on device.

MODULE NUMBERING SYSTEM



AA – PRODUCT LINE IDENTIFIER
Micron Technology Component Product ..... MT

BB – NUMBER OF MEMORY COMPONENTS

C – RAM FAMILY
SRAM ..... S
DRAM ..... D

DDD – DEPTH

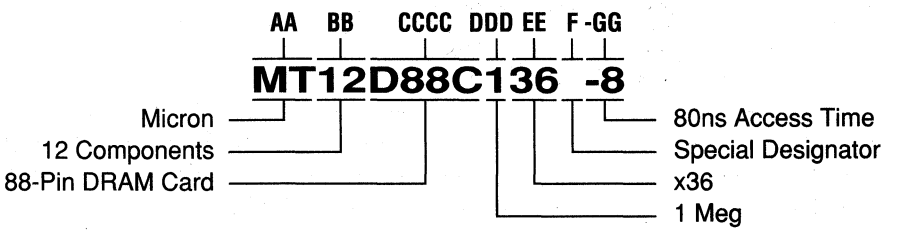
EE – WIDTH

F – PACKAGE CODE
DIP ..... D
Gold Plate ..... G
ZIP ..... Z
SIP ..... N
SIMM ..... M

GG – SPECIAL DESIGNATOR
Low Power L

HH – ACCESS TIME
-10 ..... 10ns or 100ns
-15 ..... 15ns
-20 ..... 20ns
-25 ..... 25ns
-30 ..... 30ns
-35 ..... 35ns
-45 ..... 45ns
-6 ..... 60ns
-7 ..... 70ns
-8 ..... 80ns

IC DRAM CARD NUMBERING SYSTEM



AA – PRODUCT LINE IDENTIFIER
Micron Technology Component Product ..... MT

BB – NUMBER OF MEMORY COMPONENTS

CCCC – DRAM CARD DESIGNATOR AND PIN COUNT
88-Pin DRAM Card D88C
60-Pin DRAM Card D60C

DDD – DEPTH

EE – WIDTH

F – SPECIAL DESIGNATOR
3.3 Volts V

G – ACCESS TIME
-5 ..... 50ns
-6 ..... 60ns
-7 ..... 70ns
-8 ..... 80ns

SALES INFORMATION

ORDER INFORMATION*

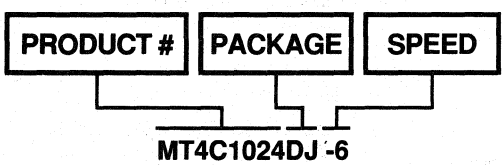
Each Micron component family is manufactured and quality controlled in the USA at our modern Boise, Idaho, facility employing Micron's low-power, high-performance CMOS silicon-gate process. Micron products are functionally equivalent to other manufacturers' products meeting JEDEC standards. Device functionality is consistently assured over a wider power supply, temperature range and refresh range than specified. Each unit receives continuous system-level testing during many hours of accelerated burn-in prior to final test and shipment. This testing is performed with Micron's exclusive **AMBYX™** intelligent burn-in and test system.

Please contact the factory for technical, test and application assistance. Micron can also furnish the sales representative and distributors nearest you. Micron's quality assured policy is to offer prompt, accurate and courteous service while assuring reliability and quality.

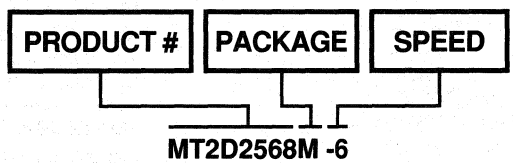
Telephone: (208) 368-3900
FAX: (208) 368-4431
Customer Comment Line:
(800) 932-4992 (USA)
01 (208) 368-3410 (Intl.)

ORDER EXAMPLES

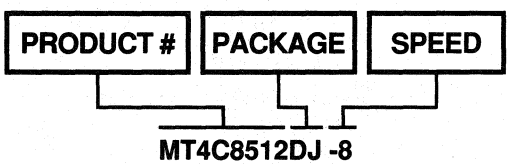
DRAM
1 Meg x 1, 60ns in Plastic SOJ



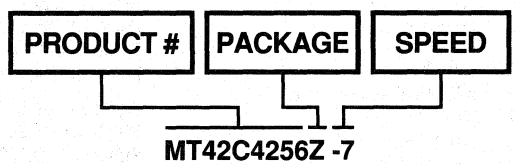
DRAM MODULE
1 Meg x 8, 60ns in SIMM Module



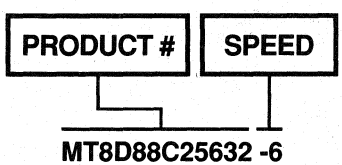
WIDE DRAM
512K x 8, 80ns in Plastic SOJ



MULTIPORT
256K x 4, 70ns in Plastic ZIP



IC DRAM CARD
256K x 32, 60ns IC DRAM Card



*For more detailed information, refer to the Product Numbering charts on pages 9-4 through 9-9.

ALABAMA

Representative

Southeast Technical Group
101 Washington, Suite 6
Huntsville, AL 35801
Phone - 205-534-2376
FAX - 205-534-2384

Distributors

Hall-Mark Electronics Corporation
4890 University Square
Business Center, Suite 1
Huntsville, AL 35816
Phone - 205-837-8700
FAX - 205-830-2565

Pioneer Technology
4835 University Square, Suite #5
Huntsville, AL 35818
Phone - 205-837-9300
FAX - 205-837-9358

Military Distributor

Zeus Components, Inc.
1750 West Broadway, Suite 114
Oviedo, FL 32765
Phone - 407-365-3000
FAX - 407-365-2356

ARIZONA

Representative

Quatra Associates
4645 South Lakeshore Dr., Suite #1
Tempe, AZ 85282
Phone - 602-820-7050
FAX - 602-820-7054

Distributors

Anthem Electronics Incorporated
1555 10th Pl., Suite #101
Tempe, AZ 85281
Phone - 602-966-6600
FAX - 602-966-4826

Hall-Mark Electronics Corporation
4637 S. 36th Place
Phoenix, AZ 85040
Phone - 602-437-1200
FAX - 602-437-2348

Wyle Laboratories
4141 E. Raymond St., Suite #1
Phoenix, AZ 85040
Phone - 602-437-2088
FAX - 602-437-2124

Military Distributors

JAN Devices, Inc.
6925 Canby Ave., Bldg. 109
Reseda, CA 91335
Phone - 818-708-1100
FAX - 818-708-7436

Zeus Components, Inc.
6276 San Ignacio Ave., Suite E
San Jose, CA 95119
Phone - 408-629-4789
FAX - 408-629-4892

ARKANSAS

Representative

Nova Marketing Incorporated
8350 Meadow Road, Suite 174
Dallas, TX 75231
Phone - 214-750-6082
FAX - 214-750-6068

Distributors

Anthem Electronics, Inc.
651 N. Plano Rd., Suite 429
Richardson, TX 75081
Phone - 214-238-7100
FAX - 214-238-0237

Hall-Mark Electronics Corporation
11420 Pagemill Road
Dallas, TX 75243
Phone - 214-553-4300
FAX - 214-343-5988

Pioneer Electronics
13765 Beta Road
Dallas, TX 75244
Phone - 214-386-7300
FAX - 214-490-6419

Wyle Laboratories
1810 N. Greenville Avenue
Richardson, TX 75081
Phone - 214- 235-9953
FAX - 214-644-5064

Military Distributor

Zeus Components, Inc.
1800 North Glenville, Suite 120
Richardson, TX 75081
Phone - 214-783-7010
FAX - 214-234-4385

CALIFORNIA

Representatives (Northern California)

Bay Area Electronics Sales, Inc.
2001 Gateway Place, Suite 315
San Jose, CA 95110
Phone - 408-452-8133
FAX - 408-452-8139

Bay Area Electronics, Inc.
5711 Reinhold St.
Fair Oaks, CA 95628
Phone - 916-863-0563
FAX - 916-863-0615

Representatives (Southern California)

Jones & McGeoy Sales, Incorporated
801 Parkcenter Drive, Suite 250
Santa Ana, CA 92705
Phone - 714-547-6466
FAX - 714-547-7670

Jones & McGeoy Sales, Incorporated
5060 Shoreham Place
San Diego, CA 92122
Phone - 619-458-5856
FAX - 619-453-0034

Jones & McGeoy Sales, Incorporated
20501 Ventura Blvd., Suite 130
Woodland Hills, CA 91364
Phone - 818-715-7161
FAX - 818-715-7199

Distributors

Anthem Electronics Incorporated
1160 Ridder Park Drive
San Jose, CA 95131
Phone - 408-453-1200
FAX - 408-452-2281

Anthem Electronics Incorporated
9131 Oakdale Avenue
Chatsworth, CA 91311
Phone - 818-700-1000
FAX - 818-775-1302

Anthem Electronics Incorporated
1 Old Field Drive
East Irvine, CA 92718-2809
Phone - 714-768-4444
FAX - 714-380-4747

Anthem Electronics Incorporated
580 Menlo Drive, Suite 8
Rocklin, CA 95677
Phone - 916-624-9744
FAX - 916-624-9750

Anthem Electronics Incorporated
9369 Carroll Park Drive
San Diego, CA 92121
Phone - 619-453-9005
FAX - 619-546-7893

Hall-Mark Electronics Corporation
9420 Topanga Canyon Blvd.
Chatsworth, CA 91311
Phone - 818-773-4500
FAX - 818-773-4555

Hall-Mark Electronics Corporation
580 Menlo Drive, Suite 2
Rocklin, CA 95677
Phone - 916-624-9781
FAX - 916-961-0922

Hall-Mark Electronics Corporation
3878 Ruffin Road, Unit 10B
San Diego, CA 92123
Phone - 619-268-1201
FAX - 619-268-0209

Hall-Mark Electronics Corporation
2105 Lundy Avenue
San Jose, CA 95030
Phone - 408-432-4000
FAX - 408-432-4044

Hall-Mark Electronics Corporation
#1 Mauchly
Irvine, CA 92718
Phone - 714-727-6000
FAX - 714-727-6066

Pioneer Technologies
134 Rio Robles
San Jose, CA 95134
Phone - 408-954-9100
FAX - 408-954-9113

Pioneer Technologies
217 Technology Drive, Suite 110
Irvine, CA 92718
Phone - 714-753-5500
FAX - 714-753-5074

Wyle Laboratories
(Accounting Office Only)
128 Maryland Avenue
El Segundo, CA 90245
Phone - 213-322-1763
FAX - 213-322-1763

Wyle Laboratories
3000 Bowers Avenue
Santa Clara, CA 95051
Phone - 408-727-2500
FAX - 408-727-5896

Wyle Laboratories
17872 Cowan Avenue
Irvine, CA 92714
Phone - 714-863-9953
FAX - 714-863-0473

Wyle Laboratories
2951 Sunrise Blvd., Suite #175
Rancho Cordova, CA 95742
Phone - 916-638-5282
FAX - 916-638-1491

Wyle Laboratories
9525 Chesapeake Drive
San Diego, CA 92123
Phone - 619-565-9171
FAX - 619-565-0512

Wyle Laboratories
26010 Mureau Road, #150
Calabasas, CA 91302
Phone - 818-880-9000
FAX - 818-880-5510

Military Distributors

JAN Devices, Inc.
6925 Canby, Bldg. 109
Reseda, CA 91335
Phone - 818-708-1100
FAX - 818-708-7436

Zeus Components, Inc.
22700 Savi Ranch Parkway
Yorba Linda, CA 92686
Phone - 714-921-9000
FAX - 714-921-2715

Zeus Components, Inc.
5236 Colodny Drive, Suite 102
Agoura Hills, CA 91301
Phone - 818-889-3838
FAX - 818-889-2464

Zeus Components, Inc.
5225 Ruffin Road, Suite 200
San Diego, CA 92123
Phone - 619-277-9681
FAX - 619-277-7105

Zeus Components, Inc.
6276 San Ignacio Ave., Suite E
San Jose, CA 95119
Phone - 408-629-4789
FAX - 408-629-4892

CANADA

Representatives

Clark-Hurman Associates
20 Regan Road, Unit #14
Brampton, Ontario L7A 1C3
Canada
Phone - 416-840-6066
FAX - 416-840-6091

Clark-Hurman Associates
66 Colonnade Road, Suite 205
Nepean, Ontario K2E 7K7
Canada
Phone - 613-727-5626
FAX - 613-727-1707

Clark-Hurman Associates
4 Chester
Pointe Claire, Quebec H9R 4H7
Canada
Phone - 514-426-0453
FAX - 514-426-0455

Davetek Marketing
107-3738 North Fraser Way
Burnaby, BC V5J 5G1
Canada
Phone 604-430-3680
FAX - 604-435-5490

Distributors

Semad Electronic
85 Spy Court
Markham, Ontario L3R 4Z4
Canada
Phone - 416-475-3922
FAX - 416-475-4158

Semad Electronic
1825 Woodward Dr.
Ottawa, Ontario K2C OR3
Canada
Phone - 613-727-8325
FAX - 613-727-9489

Semad Electronic
8563 Government Street
Burnaby, B.C. V3N 4S9
Canada
Phone - 604-420-9889
FAX - 604-420-0124

Semad Electronic
243 Place Frontenac
Pointe Claire, PQ H9R 4Z7
Canada
Phone - 514-694-0860
FAX - 514-694-0965

Semad Electronic
6120 3rd St. S.E., Unit 9
Calgary, Alberta T2H 1K4
Canada
Phone - 403-252-5664
FAX - 403-255-0966

COLORADO

Representative

Wescom Marketing
4891 Independence St.
Wheatridge, CO 80033
Phone - 303-422-8957
FAX - 303-422-9892

Distributors

Anthem Electronics Incorporated
373 Inverness Drive
Englewood, CO 80112
Phone - 303-790-4500
FAX - 303-790-4532

Hall-Mark Electronics Corporation
12503 E. Euclid Dr., Suite #20
Englewood, CO 80111
Phone - 303-790-1662
FAX - 303-790-4991

Wyle Laboratories
451 E 124th Street
Thornton, CO 80241
Phone - 303-457-9953
FAX - 303-457-4831

Military Distributors

JAN Devices, Inc.
6925 Canby, Bldg. 109
Reseda, CA 91335
Phone - 818-708-1100
FAX - 818-708-7436

Zeus Components, Inc.
6276 San Ignacio Ave., Suite E
San Jose, CA 95119
Phone - 408-629-4789
FAX - 408-629-4892

CONNECTICUT

Representative

Advanced Tech Sales Incorporated
Westview Office Park
Building 2, Suite 1C
850 N. Main St. Extension
Wallingford, CT 06492
Phone - 203-284-0838
FAX - 203-284-8232

Distributors

Anthem Electronics
61 Mattatuck Heights
Waterbury, CT 06705
Phone - 203-575-1575
FAX - 203-596-3232

Hall-Mark Electronics Corporation
125 Commerce Ct., Unit 6
Cheshire, CT 06410
Phone - 203-271-2844
FAX - 203-272-1704

Pioneer Standard
112 Main Street
Norwalk, CT 06851
Phone - 203-853-1515
FAX - 203-838-9901

Military Distributor

Zeus Components, Inc.
100 Midland Avenue
Port Chester, NY 10573
Phone - 914-937-7400
FAX - 914-937-2553

DELAWARE

Representative

Omega Electronic Sales Incorporated
2655 Interplex Drive, Suite 104
Trevose, PA 19047
Phone - 215-244-4000
FAX - 215-244-4104

Distributor

Pioneer Technologies
500 Enterprise Road
Horsham, PA 19044
Phone - 215-674-4000
FAX - 215-674-3107

Military Distributor

Zeus Components, Inc.
8930-A Route 108
Columbia, MD 21045
Phone - 301-997-1118
FAX - 301-964-9784

DISTRICT OF COLUMBIA

Representative

Electronic Engineering & Sales, Inc.
235 Prince George Street
Annapolis, MD 21401
Phone - 301-269-6573
FAX - 301-269-6476

Distributors

Anthem Electronics, Inc.
7168 A Columbia Gateway Drive
Columbia, MD 21046-2101
Phone - 301-995-6640
FAX - 301-381-4379

Hall-Mark Electronics Corporation
10240 Old Columbia Road
Columbia, MD 21046
Phone - 301-988-9800
FAX - 301-381-2036

Pioneer Technologies
9100 Gaither Road
Gaithersburg, MD 20877
Phone - 301-921-0660
FAX - 301-921-3852

Military Distributor

Zeus Components, Inc.
8930-A Route 108
Columbia, MD 21045
Phone - 301-997-1118
FAX - 301-964-9784

FLORIDA

Representatives

Photon Sales, Inc.
1600 Sarno Rd., Suite #21
Melbourne, FL 32935
Phone - 407-259-8999
FAX - 407-259-1323

Photon Sales, Inc.
715 Florida St.
Orlando, FL 32806
Phone - 407-896-6064
FAX - 407-896-6197

Photon Sales, Inc.
11210 Garfield Court
Seffner, FL 33584
Phone - 813-689-6751
FAX - 813-689-6811

Photon Sales, Inc.
3475 B. East Bay Drive
Largo, FL 34641
Phone - 813-531-2272
FAX - 813-536-4599

Distributors

Anthem Electronics Incorporated
2555 Enterprise Rd., Suite #11-2
Clearwater, FL 34623
Phone - 813-797-2900
FAX - 813-796-4880

Chip Supply
7725 N. Orange Blossom Trail
Orlando, FL 32810-2696
Phone - 407-298-7100
FAX - 407-290-0164

Hall-Mark Electronics Corporation
10491 72nd St. North, #303
Largo, FL 34647
Phone - 813-541-7440
FAX - 813-544-4394

Hall-Mark Electronics Corporation
3161 Southwest 15th Street
Pompano Beach, FL 33069-4806
Phone - 305-971-9280
FAX - 305-971-9339

Hall-Mark Electronics Corporation
489 E. Semoran Blvd., Suite #145
Casselberry, FL 32707
Phone - 407-830-5855
FAX - 407-767-5002

Pioneer Technologies
337 South-North Lake #1000
Altamonte Springs, FL 32701
Phone - 407-834-9090
FAX - 407-834-0865

Pioneer Technologies
5500 Rio Vista Drive
Clearwater, FL 34620
Phone - 813-531-5037
FAX - 918-492-0546

Pioneer Technologies
674 S. Military Trail
Deerfield Beach, FL 33442
Phone - 305-428-8877
FAX - 305-481-2950

Military Distributor

Zeus Components, Inc.
1750 W. Broadway, Suite 114
Oviedo, FL 32765
Phone - 407-365-3000
FAX - 407-365-2356

GEORGIA

Representative

Southeast Technical Group
2620 Deer Isle Cove
Lawrenceville, GA 30244
Phone - 404-979-2055
FAX - 404-979-2055

Distributors

Hall-Mark Electronics Corporation
3425 Corporate Way, Suite A
Duluth, GA 30136-2552
Phone - 404-623-4400
FAX - 404-476-8806

Pioneer Technologies
4250 C Rivergreen Parkway
Duluth, GA 30136
Phone - 404-623-1003
FAX - 404-623-0665

Military Distributor

Zeus Components, Inc.
1750 West Broadway, Suite 114
Oveido, FL 32765
Phone - 407-365-3000
FAX - 407-365-2356

HAWAII

Representatives

Bay Area Electronics
2001 Gateway Pl., Suite 315
San Jose, CA 95110
Phone - 408-452-8133
FAX - 408-452-8139

Bay Area Electronics
5711 Reinhold Street
Fair Oaks, CA 95628
Phone - 916-863-0563
FAX - 916-863-0615

Distributors

Anthem Electronics Incorporated
1160 Ridder Park Drive
San Jose, CA 95131
Phone - 408-453-1200
FAX - 408-452-2281

Hall-Mark Electronics Corporation
2105 Lundy Avenue
San Jose, CA 95030
Phone - 408-432-4000
FAX - 408-432-4044

Wyle Laboratories
3000 Bowers Avenue
Santa Clara, CA 95051
Phone - 408-727-2500
FAX - 408-727-5896

IDAHO

Representative

Contact Micron
Component Sales
Phone - 208-368-3900

Distributors

Anthem Electronics, Inc.
1279 West 2200 South
Salt Lake City, UT 84119
Phone - 801-973-8555
FAX - 801-973-8909

Hall-Mark Electronics Corporation
12503 E. Euclid Drive, Suite 20
Englewood, CO 80111
Phone - 303-790-1662
FAX - 303-790-4991

Wyle Laboratories
1325 West 2200 South, Suite E
West Valley, UT 84119
Phone - 801-974-9953
FAX - 801-972-2524

Military Distributors

JAN Devices, Inc.
6925 Canby, Bldg. 109
Reseda, CA 91335
Phone - 818-708-1100
FAX - 818-708-7436

Zeus Components, Inc.
6276 San Ignacio Ave., Suite E
San Jose, CA 95119
Phone - 408-629-4789
FAX - 408-629-4892

ILLINOIS

Representatives

Advanced Technical Sales
13755 St. Charles Rock Road
Bridgeton, MO 63044
Phone - 314-291-5003
FAX - 314-291-7958

Industrial Representatives, Inc.
8430 Gross Point Road
Skokie, IL 60077
Phone - 708-967-8430
FAX - 708-967-5903

Distributors

Anthem Electronics Incorporated
1300 Remington, Suite A
Schaumburg, IL 60173
Phone - 708-884-0200
FAX - 708-884-0480

Hall-Mark Electronics Corporation
210 Mittel Drive
Wooddale, IL 60191
Phone - 708-860-3800
FAX - 708-860-0239

Pioneer Standard
2171 Executive Drive, Suite 200
Addison, IL 60101
Phone - 708-495-9680
FAX - 708-495-9831

Military Distributors

Zeus Components, Inc.
100 Midland Avenue
Port Chester, NY 10573
Phone - 914-937-7400
FAX - 914-937-2553

Zeus Components, Inc.
2912 Springboro West, Suite 106
Dayton, OH 45439
Phone - 513-293-6162
FAX - 513-293-1781

INDIANA

Representatives

Scott Electronics, Inc. (S. Indiana)
7321 Shadeland Station, Suite 256
Indianapolis, IN 46256
Phone - 317-841-0010
FAX - 317-841-0107

Scott Electronics, Inc. (N. Indiana)
Lima Valley Office Village
8109 Lima Road
Fort Wayne, IN 46818
Phone - 219-489-5690
FAX - 219-489-1842

Distributors

Hall-Mark Electronics Corporation
4275 W. 96th Street
Indianapolis, IN 46268
Phone - 317-872-8875
FAX - 317-876-7165

Pioneer Standard
9350 N. Priority Way, West Dr.
Indianapolis, IN 46240
Phone - 317-573-0880
FAX - 317-573-0979

Military Distributors

Zeus Components, Inc.
100 Midland Avenue
Port Chester, NY 10573
Phone - 914-937-7400
FAX - 914-937-2553

Zeus Components, Inc.
2912 Springboro West, Suite 106
Dayton, OH 45439
Phone - 513-293-6162
FAX - 513-293-1781

IOWA

Representative

Advanced Technical Sales
375 Collins Road N.E.
Cedar Rapids, IA 52402
Phone - 319-393-8280
FAX - 319-393-7258

Distributors

Anthem Electronics Incorporated
7646 Golden Triangle Dr., #160
Eden Prairie, MN 55344
Phone - 612-944-5454
FAX - 612-944-3045

Hall-Mark Electronics Corporation
210 Mittel Drive
Wooddale, IL 60191
Phone - 708-860-3800
FAX - 708-860-0239

Pioneer Standard
7625 Golden Triangle Drive
Eden Prarie, MN 55344
Phone - 612-944-3355
FAX - 612-944-3794

Military Distributor

Zeus Components, Inc.
1800 North Glenville, Suite 120
Richardson, TX 75081
Phone - 214-783-7010
FAX - 214-234-4385

KANSAS

Representative

Advanced Technical Sales
601 N. Mur-Len, Suite 8
Olathe, KS 66062
Phone - 913-782-8702
FAX - 913-782-8641

Distributors

Hall-Mark Electronics Corporation
10809 Lakeview Avenue
Lenexa, KS 66215
Phone - 913-888-4747
FAX - 913-888-0523

Pioneer Electronics
111 Westport Plaza, #625
St. Louis, MO 63146
Phone - 314-542-3077
FAX - 314-542-3078

Military Distributor

Zeus Components, Inc.
1800 North Glenville, Suite 120
Richardson, TX 75081
Phone - 214-783-7010
FAX - 214-234-4385

KENTUCKY

Representatives

Scott Electronics, Inc.
10901 Reed-Hartman Hwy., Suite 301
Cincinnati, OH 45242-2821
Phone - 513-791-2513
FAX - 513-791-8059

Distributors

Hall-Mark Electronics Corporation (E. Ky.)
777 Dearborn Park Lane, Suite L
Worthington, OH 43085
Phone - 614-888-3313
FAX - 614-888-0767

Hall-Mark Electronics Corporation (W. Ky.)
4275 W. 96th Street
Indianapolis, IN 46268
Phone - 317-872-8875
FAX - 317-876-7165

Pioneer Standard (W. Ky.)
9350 N. Priority Way, W. Dr.
Indianapolis, IN 46240
Phone - 317-573-0880
FAX - 317-573-0979

Pioneer Standard (E. Ky.)
4433 Interpoint Boulevard
Dayton, OH 45424
Phone - 513-236-9900
FAX - 513-236-8133

LOUISIANA

Representative

Nova Marketing Incorporated
8350 Meadow Road, Suite 174
Dallas, TX 75231
Phone - 214-750-6082
FAX - 214-750-6068

Distributors

Hall-Mark Electronics Corporation
11420 Pagemill Road
Dallas, TX 75243
Phone - 214-553-4300
FAX - 214-343-5988

Pioneer Electronics
13765 Beta Road
Dallas, TX 75244
Phone - 214-386-7300
FAX - 214-490-6419

Wyle Laboratories
1810 North Greenville Avenue
Richardson, TX 75081
Phone - 214-235-9953
FAX - 214-644-5064

Military Distributors

Zeus Components, Inc.
8930-A Route 108
Columbia, MD 21045
Phone - 301-997-1118
FAX - 301-964-9784

Zeus Components, Inc.
1800 North Glenville, Suite 120
Richardson, TX 75081
Phone - 214-783-7010
FAX - 214-234-4385

MAINE

Representative

Advanced Tech Sales Incorporated
348 Park Street, Suite 102
North Reading, MA 01864
Phone - 508-664-0888
FAX - 508-664-5503

Distributors

Anthem Electronics
36 Jonspin Road
Wilmington, MA 01887
Phone - 508-657-5170
FAX - 508-657-6008

Gerber Electronics
128 Carnegie Road
Norwood, MA 02062
Phone - 617-769-6000
FAX - 617-762-8931

Hall-Mark Electronics Corporation
Pinehurst Park, 6 Cook Street
Billerica, MA 01821
Phone - 508-667-0902
FAX - 508-667-4129

Pioneer Standard
44 Hartwell Avenue
Lexington, MA 02173
Phone - 617-861-9200
FAX - 617-863-1547

Wyle Laboratories
15 3rd Avenue
Burlington, MA 01803
Phone - 617-272-7300
FAX - 617-272-6809

Military Distributors

JAN Devices
44 Cochrane St.
Melrose, MA 02176
Phone - 617-662-3901
FAX - 617-662-0837

Zeus Components, Inc.
11 Lakeside Office Park
607 North Avenue
Wakefield, MA 01880
Phone - 617-246-8200
FAX - 617-246-8293

MARYLAND

Representative

Electronic Engineering & Sales, Inc.
235 Prince George Street
Annapolis, MD 21401
Phone - 301-269-6573
FAX - 301-269-6476

Distributors

Anthem Electronics
7168 A Columbia Gateway Drive
Columbia, MD 21046-2101
Phone - 301-995-6640
FAX - 301-381-4379

Hall-Mark Electronics Corporation
10240 Old Columbia Road
Columbia, MD 21046
Phone - 301-988-9800
FAX - 301-381-2036

Pioneer Technologies
9100 Gaither Road
Gaithersburg, MD 20877
Phone - 301-921-0660
FAX - 301-921-3852

Military Distributor

Zeus Components, Inc.
8930-A Route 108
Columbia, MD 21045
Phone - 301-997-1118
FAX - 301-964-9784

MASSACHUSETTS

Representative

Advanced Tech Sales, Inc.
348 Park Street, Suite 102
North Reading, MA 01864
Phone - 508-664-0888
FAX - 508-664-5503

Distributors

Anthem Electronics, Inc.
36 Jonspin Road
Wilmington, MA 01887
Phone - 508-657-5170
FAX - 508-657-6008

Gerber Electronics
128 Carnegie Road
Norwood, MA 02062
Phone - 617-769-6000
FAX - 617-762-8931

Hall-Mark Electronics Corporation
Pinehurst Park, 6 Cook Street
Billerica, MA 01821
Phone - 508-667-0902
FAX - 508-667-4129

Pioneer Standard
44 Hartwell Avenue
Lexington, MA 02173
Phone - 617-861-9200
FAX - 617-863-1547

Wyle Laboratories
15 3rd Avenue
Burlington, MA 01803
Phone - 617-272-7300
FAX - 617-272-6809

Military Distributors

JAN Devices, Inc.
44 Cochrane St.
Melrose, MA 02176
Phone - 617-662-3901
FAX - 617-662-0837

Zeus Components, Inc.
11 Lakeside Office Park
607 North Avenue
Wakefield, MA 01880
Phone 617-246-8200
FAX - 617-246-8293

MICHIGAN

Representative

Rathsburg Associates Incorporated
34605 Twelve Mile Rd.
Farmington Hills, MI 48331-3263
Phone - 313-489-1500
FAX - 313-489-1480

Distributors

Hall-Mark Electronics Corporation
38027 Schoolcraft Road
Livonia, MI 48150
Phone - 313-462-1205
FAX - 313-462-1830

Pioneer Standard
4505 Broadmoor Avenue, S.E.
Grand Rapids, MI 49512
Phone - 616-698-1800
FAX - 616-698-1831

Pioneer Standard
13485 Stamford
Livonia, MI 48150
Phone - 313-525-1800
FAX - 313-427-3720

Military Distributors

Zeus Components, Inc.
100 Midland Avenue
Port Chester, NY 10573
Phone - 914-937-7400
FAX - 914-937-2553

Zeus Components, Inc.
2912 Springboro West, Suite 106
Dayton, OH 45439
Phone - 513-293-6162
FAX - 513-293-1781

MINNESOTA

Representative

HMR Incorporated
9065 Lyndale Avenue
Minneapolis, MN 55420-3520
Phone - 612-888-2122
FAX - 612-884-4768

Distributors

Anthem Electronics Inc.
7646 Golden Triangle Dr., #160
Eden Prairie, MN 55344
Phone - 612-944-5454
FAX - 612-944-3045

Hall-Mark Electronics Corporation
9401 James Avenue South, Suite 140
Bloomington, MN 55431
Phone - 612-881-2600
FAX - 612-881-9461

Pioneer Standard
7625 Golden Triangle Drive
Eden Prairie, MN 55344
Phone - 612-944-3355
FAX - 612-944-3794

Military Distributors

Zeus Components, Inc.
100 Midland Avenue
Port Chester, NY 10573
Phone - 914-937-7400
FAX - 914-937-2553

Zeus Components, Inc.
2912 Springboro West, Suite 106
Dayton, OH 45439
Phone - 513-293-6162
FAX - 513-293-1781

MISSISSIPPI

Representative

Southeast Technical Group
Route 10, Box 368
Meridian, MS 39301
Phone - 601-485-7055
FAX - 601-485-7063

Distributors

Hall-Mark Electronics Corporation
4890 University Square
Business Center, Suite 1
Huntsville, AL 35816
Phone - 205-837-8700
FAX - 205-830-2565

Pioneer Technologies
4835 University Square, Suite #5
Huntsville, AL 35818
Phone - 205-837-9300
FAX - 205-837-9358

Military Distributor

Zeus Components, Inc.
1800 North Glenville, Suite 120
Richardson, TX 75081
Phone - 214-783-7010
FAX - 214-234-4385

MISSOURI

Representative

Advanced Technical Sales
13755 St. Charles Rock Road
Bridgeton, MO 63044
Phone - 314-291-5003
FAX - 314-291-7958

Distributors

Hall-Mark Electronics Corporation
3783 Rider Trail So.
Earth City, MO 63045
Phone - 314-291-5350
FAX - 314-291-0362

Pioneer Standard
111 Westport Plaza, #625
St. Louis, MO 63146
Phone - 314-542-3077
FAX - 314-542-3078

Military Distributor

Zeus Components, Inc.
1800 North Glenville, Suite 120
Richardson, TX 75081
Phone - 214-783-7010
FAX - 214-234-4385

MONTANA

Military Distributor

Zeus Components, Inc.
6276 San Ignacio Ave., Suite E
San Jose, CA 95119
Phone - 408-629-4789
FAX - 408-629-4892

NEBRASKA

Representative

Advanced Technical Sales
601 North Mur-Len, Suite 8
Olathe, KS 66062
Phone - 913-782-8702
FAX - 913-782-8641

Distributors

Hall-Mark Electronics Corporation
10809 Lakeview Dr.
Lenexa, KS 66215
Phone - 913-888-4747
FAX - 913-888-0523

Wyle Laboratories
451 E 124th Street
Thornton, CO 80241
Phone - 303-457-9953
FAX - 303-457-4831

Military Distributor

Zeus Components, Inc.
1800 North Glenville, Suite 120
Richardson, TX 75081
Phone - 214-783-7010
FAX - 214-234-4385

NEVADA

Representatives

Bay Area Electronics Sales, Inc.
2001 Gateway Place, Suite 315
San Jose, CA 95110
Phone - 408-452-8133
FAX - 408-452-8139

Bay Area Electronics Sales, Inc.
235 Prince George St.
Annapolis, MD 21401
Phone - 301-269-6573
FAX - 301-269-6476

Distributors

Anthem Electronics Incorporated
580 Menlo Drive, Suite 8
Rocklin, CA 95677
Phone - 916-624-9744
FAX - 916-624-9750

Hall-Mark Electronics Corporation
580 Menlo Dr., Suite 2
Rocklin, CA 95677
Phone - 916-624-9781
FAX - 916-961-0922

Wyle Laboratories
2951 Sunrise Blvd., Suite 175
Rancho Cordova, CA 95742
Phone - 916-638-5282
FAX - 916-638-1491

Military Distributors

JAN Devices, Inc.
44 Cochrane St.
Melrose, MA 02176
Phone - 617-662-3901
FAX - 617-662-0837

Zeus Components, Inc.
6276 San Ignacio Ave., Suite E
San Jose, CA 95119
Phone - 408-629-4789
FAX - 408-629-4892

NEW HAMPSHIRE

Representative

Advanced Tech Sales Incorporated
348 Park Street, Suite 102
North Reading, MA 01864
Phone - 508-664-0888
FAX - 508-664-5503

Distributors

Anthem Electronics
36 Jonspin Road
Wilmington, MA 01887
Phone - 508-657-5170
FAX - 508-657-6008

Hall-Mark Electronics Corporation
Pinehurst Park, 6 Cook Street
Billerica, MA 01821
Phone - 508-667-0902
FAX - 508-667-4129

Pioneer Standard
44 Hartwell Avenue
Lexington, MA 02173
Phone - 617-861-9200
FAX - 617-863-1547

Military Distributor

Zeus Components, Inc.
11 Lakeside Office Park
607 North Avenue
Wakefield, MA 01880
Phone - 617-246-8200
FAX - 617-246-8293

NEW JERSEY

Representatives

Omega Electronics
2655 Interplex Dr., Suite 104
Trevose, PA 19047
Phone - 215-244-4000
FAX - 215-244-4104

Parallax, Inc.
734 Walt Whitman Road
Melville, NY 11747
Phone - 516-351-1000
FAX - 516-351-1606

Distributors

Anthem Electronics, Inc.
355 Business Center Drive
Horsham, PA 19044
Phone - 215-443-5150
FAX - 215-675-9875

Anthem Electronics, Inc.
26 Chapin Road, Unit K
Pine Brook, NJ 07058
Phone - 201-227-7960
FAX - 201-227-9246

Hall-Mark Electronics Corporation
Moorestown West Corporate Center
225 Executive Drive, Suite 5
Moorestown, NJ 08057
Phone - 609-235-1900
FAX - 609-235-3381

Hall-Mark Electronics Corporation
200 Lanidex Plaza, 2nd Floor
Parsippany, NJ 07054
Phone - 201-515-3000
FAX - 201-515-4475

Pioneer Standard
14A Madison Road
Fairfield, NJ 07006
Phone - 201-575-3510
FAX - 201-575-3454

Pioneer Technologies
500 Enterprise Road
Horsham, PA 19044
Phone - 215-674-4000
FAX - 215-674-3107

Military Distributors

Zeus Components, Inc.
100 Midland Avenue
Port Chester, NY 10573
Phone - 914-937-7400
FAX - 914-937-2553

Zeus Components, Inc.
8930-A Route 108
Columbia, MD 21045
Phone - 301-997-1118
FAX - 301-964-9784

NEW MEXICO

Representative

Quatra Associates Incorporated
600 Autumnwood Place, S.E.
Albuquerque, NM 87123
Phone - 505-296-6781
FAX - 505-292-2092

Distributors

Anthem Electronics Inc.
1555 W. 10th Pl., Suite #101
Tempe, AZ 85281
Phone - 602-966-6600
FAX - 602-966-4826

Hall-Mark Electronics Corporation
4637 South 36th Place
Phoenix, AZ 85040
Phone - 602-437-1200
FAX - 602-437-2348

Wyle Laboratories
4141 E. Raymond St., Suite #1
Phoenix, AZ 85040
Phone - 602-437-2088
FAX - 602-437-2124

Military Distributors

JAN Devices, Inc.
6925 Canby, Bldg. 109
Reseda, CA 91335
Phone - 818-708-1100
FAX - 818-708-7436

Zeus Components, Inc.
6276 San Ignacio Ave., Suite E
San Jose, CA 95119
Phone - 408-629-4789
FAX - 408-629-4892

NEW YORK

Representatives

Electra Sales Corporation
3000 Winston Rd. S., Bldg. E
Rochester, NY 14623
Phone - 716-427-7860
FAX - 716-427-0614

Electra Sales Corporation
1 Adler Drive
East Syracuse, NY 13057
Phone - 315-463-1248
FAX - 315-463-1717

Parallax, Inc.
734 Walt Whitman Road
Melville, NY 11747
Phone - 516-351-1000
FAX - 516-351-1606

Distributors

Anthem Electronics-Military
47 Mall Drive
Commack, NY 11725-5703
Phone - 516-864-6600
FAX - 516-493-2244

Anthem Electronics, Inc.
26 Chapin Road, Unit K
Pinebrook, NJ 07058
Phone - 201-227-7960
FAX - 201-227-9246

Hall-Mark Electronics Corporation
6605 Pittsford - Palmyra Road, Suite E8
Fairport, NY 14450
Phone - 716-425-3300
FAX - 716-425-7195

Hall-Mark Electronics Corporation
3075 Veterans Memorial Hwy.
Ronkonkoma, NY 11779
Phone - 516-737-0600
FAX - 516-737-0838

Hall-Mark Electronics Corporation
200 Lanidex Plaza, 2nd Floor
Parsippany, NJ 07054
Phone - 201-515-3000
FAX - 201-515-4475

MAST Distributors, Inc.
710-2 Union Parkway
Ronkonkoma, NY 11779
Phone - 516-471-4422
FAX - 516-471-2040

Pioneer Standard
68 Corporate Drive
Binghamton, NY 13904
Phone - 607-722-9300
FAX - 607-722-9562

Pioneer Standard
14A Madison Road
Fairfield, NJ 07006
Phone - 201-575-3510
FAX - 201-575-3454

Pioneer Standard
840 Fairport Park
Fairport, NY 14450
Phone - 716-381-7070
FAX - 716-381-5955

Pioneer Standard
60 Crossways Park West
Woodbury, NY 11797
Phone - 516-921-8700
FAX - 516-921-2143

Military Distributors

Zeus Components, Inc.
100 Midland Avenue
Port Chester, NY 10573
Phone - 914-937-7400
FAX - 914-937-2553

Zeus Components, Inc.
2110 Smithtown Avenue
Ronkonkoma, L.I., NY 11779
Phone - 516-737-4500
FAX - 516-737-4520

Zeus Components, Inc.
2912 Springboro West, Suite 106
Dayton, OH 45439
Phone - 513-293-6162
FAX - 513-293-1781

NORTH CAROLINA

Representatives

Southeast Technical Group
700 N. Arendell Avenue
Zebulon, NC 27597
Phone - 919-269-5589
FAX - 919-269-5670

Distributors

Hall-Mark Electronics Corporation
5234 Green's Dairy Road
Raleigh, NC 27604
Phone - 919-872-0712
FAX - 919-878-8729

Pioneer Technologies
9401L Southern Pine Blvd.
Charlotte, NC 28273
Phone - 704-526-8188
FAX - 704-522-8564

Pioneer Electronics
2810 Meridian Parkway, #148
Durham, NC 27713
Phone - 919-544-5400
FAX - 919-544-5885

Military Distributor

Zeus Components, Inc.
8930-A Route 108
Columbia, MD 21045
Phone - 301-997-1118
FAX - 301-964-9784

NORTH DAKOTA

Representative

HMR Incorporated
9065 Lyndale Ave. South
Minneapolis, MN 55420-3520
Phone - 612-888-2122
FAX - 612-884-4768

Distributors

Anthem Electronics Incorporated
7646 Golden Triangle Dr., #160
Eden Prairie, MN 55344
Phone - 612-944-5454
FAX - 612-944-3045

Hall-Mark Electronics Corporation
9401 James Avenue South, Suite 140
Bloomington, MN 55431
Phone - 612-881-2600
FAX - 612-881-9461

Pioneer Standard
7625 Golden Triangle Drive
Eden Prairie, MN 55344
Phone - 612-944-3355
FAX - 612-944-3794

Military Distributors

Zeus Components, Inc.
100 Midland Avenue
Port Chester, NY 10573
Phone - 914-937-7400
FAX - 914-937-2553

Zeus Components, Inc.
2912 Springboro West, Suite 106
Dayton, OH 45439
Phone - 513-293-6162
FAX - 513-293-1781

OHIO

Representatives

Scott Electronics, Inc.
Corporate Headquarters
3131 S. Dixie Dr., Suite 200
Dayton, OH 45439-2223
Phone - 513-294-0539
FAX - 513-294-4769

Scott Electronics, Inc.
360 Alpha Park
Cleveland OH 44143-2240
Phone - 216-473-5050
FAX - 216-473-5055

Scott Electronics, Inc.
916 Eastwind Drive
Westerville, OH 43081-3379
Phone - 614-882-6100
FAX - 614-882-0900

Scott Electronics, Inc.
10901 Reed-Hartman Hwy., Suite 301
Cincinnati, OH 45242-2821
Phone - 513-791-2513
FAX - 513-791-8059

Distributors

Hall-Mark Electronics Corporation
5821 Harper Road
Solon, OH 44139
Phone - 216-349-4632
FAX - 216-248-4803

Hall-Mark Electronics Corporation
777 Dearborn Park Lane, Suite L
Worthington, OH 43085
Phone - 614-888-3313
FAX - 614-888-0767

Pioneer Standard
4800 E. 131st Street
Cleveland, OH 44105
Phone - 216-587-3600
FAX - 216-587-3906

Pioneer Standard
4433 Interpoint Blvd.
Dayton, OH 45424
Phone - 513-236-9900
FAX - 513-236-8133

Pioneer Standard
6421 E. Main St., #201
Reynoldsburg, OH 43608
Phone - 614-221-0043
FAX - 614-759-1955

Military Distributors

Zeus Components, Inc.
2912 Springboro West, Suite 106
Dayton, OH 45439
Phone - 513-293-6162
FAX - 513-293-1781

Zeus Components, Inc.
100 Midland Avenue
Port Chester, NY 10573
Phone - 914-937-7400
FAX - 914-937-2553

Zeus Components, Inc.
2912 Springboro West, Suite 106
Dayton, OH 45439
Phone - 513-293-6162
FAX - 513-293-1781

OKLAHOMA

Representative

Nova Marketing Incorporated
8125 E. 51st St., Suite 1339
Tulsa, OK 74145
Phone - 918-660-5105
FAX - 918-665-3815

Distributors

Hall-Mark Electronics Corporation
5411 S. 125th East Avenue, #305
Tulsa, OK 74146
Phone - 918-254-3200
FAX - 918-254-6207

Pioneer Standard
4110 South 100th East Avenue, Suite 100
Tulsa, OK 74146
Phone - 918-665-7840
FAX - 918-665-1891

Military Distributor

Zeus Components, Inc.
1800 N. Glenville, Suite 120
Richardson, TX 75081
Phone - 214-783-7010
FAX - 214-234-4385

OREGON

Representative

Westerberg & Associates
7165 S.W. Firloop
Portland, OR 97223
Phone - 503-620-1931
FAX - 503-684-5376

Distributors

Anthem Electronics Incorporated
9090 S.W. Gemini Drive
Beaverton, OR 97005
Phone - 503-643-1114
FAX - 503-626-7928

Wyle Laboratories
9640 Sunshine Court, Suite 200, Bldg. G
Beaverton, OR 97005
Phone - 503-643-7900
FAX - 503-646-5466

Military Distributors

JAN Devices, Inc.
6925 Canby, Bldg. 109
Reseda, CA 91335
Phone - 818-708-1100
FAX - 818-708-7436

Zeus Components, Inc.
6276 San Ignacio Ave., Suite E
San Jose, CA 95119
Phone - 408-629-4789
FAX - 408-629-4892

PENNSYLVANIA

Representatives

Omega Electronic Sales Incorporated
2655 Interplex Dr., #104
Trevose, PA 19047
Phone - 215-244-4000
FAX - 215-244-4104

Scott Electronics, Inc. (W. PA)
916 Eastwind Drive
Westerville, OH 43081-3379
Phone - 614-882-6100
FAX - 614-882-0900

Distributors

Anthem Electronics, Inc.
355 Business Center Drive
Horsham, PA 19044
Phone - 215-443-5150
FAX - 215-675-9875

Hall-Mark Electronics Corporation
Moorestown W. Corporate Center
225 Executive Dr., Suite 5
Moorestown, NJ 08057
Phone - 609-235-1900
FAX - 609-235-3381

Hall-Mark Electronics Corporation (W. PA)
5821 Harper Road
Solon, OH 44139
Phone - 216-349-4632
FAX - 216-248-4803

Pioneer Technologies
500 Enterprise Road
Horsham, PA 19044
Phone - 215-674-4000
FAX - 215-674-3107

Pioneer Technologies (W. PA)
259 Kappa Drive
Pittsburgh, PA 15238
Phone - 412-782-2300
FAX - 412-963-8255

Military Distributors

Zeus Components, Inc.
100 Midland Avenue
Port Chester, NY 10573
Phone - 914-937-7400
FAX - 914-937-2553

Zeus Components, Inc.
2912 Springboro West, Suite 106
Dayton, OH 45439
Phone - 513-293-6162
FAX - 513-293-1781

RHODE ISLAND

Representative

Advanced Tech Sales Incorporated
348 Park Street, Suite 102
North Reading, MA 01864
Phone - 508-664-0888
FAX - 508-664-5503

Distributors

Anthem Electronics
61 Mattatuck Heights
Waterbury, CT 06705
Phone - 203-575-1575
FAX - 203-596-3232

Hall-Mark Electronics Corporation
125 Commerce Ct., Unit 6
Cheshire, CT 06410
Phone - 203-271-2844
FAX - 203-272-1704

Pioneer Standard
112 Main Street
Norwalk, CT 06851
Phone - 203-853-1515
FAX - 203-838-9901

Military Distributor

Zeus Components, Inc.
11 Lakeside Office Park
607 North Avenue
Wakefield, MA 01880
Phone - 617-246-8200
FAX - 617-246-8293

SOUTH CAROLINA

Representative

Southeast Technical Group
700 N. Arendell Avenue
Zebulon, NC 27597
Phone - 919-269-5589
FAX - 919-269-5670

Distributors

Hall-Mark Electronics Corporation
5234 Green's Dairy Road
Raleigh, NC 27604
Phone - 919-872-0712
FAX - 919-878-8729

Pioneer Technologies
9401 L. Southern Pine Blvd.
Charlotte, NC 28273
Phone - 704-526-8188
FAX - 704-522-8564

Pioneer Technologies
2810 Meridian Parkway, #148
Durham, NC 27713
Phone - 919-544-5400
FAX - 919-544-5885

Military Distributor

Zeus Components, Inc.
1750 West Broadway, Suite 114
Oviedo, FL 32765
Phone - 407-365-3000
FAX - 407-365-2356

SOUTH DAKOTA

Representative

HMR Incorporated
9065 Lyndale Avenue
Minneapolis, MN 55420-3520
Phone - 612-888-2122
FAX - 612-884-4768

Distributors

Anthem Electronics Incorporated
7646 Golden Triangle Dr., #160
Eden Prairie, MN 55344
Phone - 612-944-5454
FAX - 612-944-3045

Hall-Mark Electronics Corporation
9401 James Avenue South, Suite 140
Bloomington, MN 55431
Phone - 612-881-2600
FAX - 612-881-9461

Pioneer Standard
7625 Golden Triangle Drive
Eden Prairie, MN 55344
Phone - 612-944-3355
FAX - 612-944-3794

Military Distributors

Zeus Components, Inc.
100 Midland Avenue
Port Chester, NY 10573
Phone - 914-937-7400
FAX - 914-937-2553

Zeus Components, Inc.
2912 Springboro West, Suite 106
Dayton, OH 45439
Phone - 513-293-6162
FAX - 513-293-1781

TENNESSEE

Representative

Southeast Technical Group
101 Washington, Suite 6
Huntsville, AL 35801
Phone - 205-534-2376
FAX - 205-534-2384

Distributors

Hall-Mark Electronics Corporation
4890 University Square
Business Center, Suite 1
Huntsville, AL 35816
Phone - 205-837-8700
FAX - 205-830-2565

Pioneer Technologies
4835 University Square, #5
Huntsville, AL 35818
Phone - 205-837-9300
FAX - 205-837-9358

Military Distributor

Zeus Components, Inc.
8930-A Route 108
Columbia, MD 21045
Phone - 301-997-1118
FAX - 301-964-9784

TEXAS

Representatives

Nova Marketing Incorporated
8350 Meadow Road, Suite 174
Dallas, TX 75231
Phone - 214-750-6082
FAX - 214-750-6068

Nova Marketing Incorporated
9207 Country Creek, Suite 141
Houston, TX 77036
Phone - 713-988-6082
FAX - 713-774-1014

Nova Marketing Incorporated
8310 Capitol of Texas Hwy. North, Suite 180
Austin, TX 78731
Phone - 512-343-2321
FAX - 512-343-2487

Quatra Associates, Inc. (El Paso, TX)
600 Autumnwood Place, S.E.
Albuquerque, NM 87123
Phone - 505-296-6781
FAX - 505-292-2092

Distributors

Anthem Electronics, Inc.
651 N. Plano Road, Suite 429
Richardson, TX 75081
Phone - 214-238-7100
FAX - 214-238-0237

Hall-Mark Electronics Corporation
12211 Technology Boulevard
Austin, TX 78727
Phone - 512-258-8848
FAX - 512-258-3777

Hall-Mark Electronics Corporation
11333 Pagemill Road
Dallas, TX 75243
Phone - 214-343-5000
FAX - 214-343-5851

Hall-Mark Electronics Corporation
11420 Pagemill Road
Dallas, TX 75243
Phone - 214-553-4300
FAX - 214-343-5988

Hall-Mark Electronics Corporation
11000 Westglen
Houston, TX 77063
Phone - 713-781-6100
FAX - 713-953-8420

Pioneer Standard
10326 Kramer Lane, Suite D
Austin, TX 78758
Phone - 512-835-4000
FAX - 512-835-9829

Pioneer Electronics
13765 Beta Road
Dallas, TX 75244
Phone - 214-386-7300
FAX - 214-490-6419

Pioneer Standard
10530 Rockley Rd., Suite 100
Houston, TX 77099
Phone - 713-495-4700
FAX - 713-495-5642

Wyle Laboratories
4030 W. Braker Lane, Suite 420
Austin, TX 78759
Phone - 512-345-8853
FAX - 512-834-0981

Wyle Laboratories
1810 N. Greenville Avenue
Richardson, TX 75081
Phone - 214-235-9953
FAX - 214-644-5064

Wyle Laboratories
11001 S. Wilcrest, Suite 100
Houston, TX 77099
Phone - 713-879-9953
FAX - 713-879-6540

Military Distributor

Zeus Components, Inc.
1800 N. Glenville, Suite 120
Richardson, TX 75081
Phone - 214-783-7010
FAX - 214-234-4385

UTAH

Representative

Wescom Marketing
3500 So. Main, Suite 100
Salt Lake City, UT 84115
Phone - 801-269-0419
FAX - 801-269-0665

Distributors

Anthem Electronics Incorporated
1279 West 2200 South
Salt Lake City, UT 84119
Phone - 801-973-8555
FAX - 801-973-8909

Hall-Mark Electronics Corporation
12503 E. Euclid Drive, Suite 20
Englewood, CO 80111
Phone - 303-790-1662
FAX - 303-790-4991

Wyle Laboratories
1325 West 2200 South, Suite E
Salt Lake City, UT 84119
Phone - 801-974-9953
FAX - 801-972-2524

Military Distributors

JAN Devices, Inc.
6925 Canby, Bldg. 109
Reseda, CA 91335
Phone - 818-708-1100
FAX - 818-708-7436

Zeus Components, Inc.
6276 San Ignacio Ave., Suite E
San Jose, CA 95119
Phone - 408-629-4789
FAX - 408-629-4892

VERMONT

Representative

Advanced Tech Sales Incorporated
348 Park Street, Suite 102
North Reading, MA 01864
Phone - 508-664-0888
FAX - 508-664-5503

Distributors

Anthem Electronics
36 Jonspin Road
Wilmington, MA 01887
Phone - 508-657-5170
FAX - 508-657-6008

Hall-Mark Electronics Corporation
Pinehurst Park, 6 Cook Street
Billerica, MA 01821
Phone - 508-667-0902
FAX - 508-667-4129

Pioneer Standard
44 Hartwell Avenue
Lexington, MA 02173
Phone - 617-861-9200
FAX - 617-863-1547

Military Distributor

Zeus Components, Inc.
11 Lakeside Office Park
607 North Avenue
Wakefield, MA 01880
Phone - 617-246-8200
FAX - 617-246-8293

VIRGINIA

Representative

Electronic Engineering & Sales, Inc.
235 Prince George Street
Annapolis, MD 21401
Phone - 301-269-6573
FAX - 301-269-6476

Distributors

Anthem Electronics
7168 A Columbia Gateway Drive
Columbia, MD 21046-2101
Phone - 301-995-6640
FAX - 301-381-4379

Hall-Mark Electronics Corporation
10240 Old Columbia Road
Columbia, MD 21046
Phone - 301-988-9800
FAX - 301-381-2036

Pioneer Technologies
9100 Gaither Drive
Gaithersburg, MD 20877
Phone - 301-921-0660
FAX - 301-921-3852

Military Distributor

Zeus Components, Inc.
8930-A Route 108
Columbia, MD 21045
Phone - 301-997-1118
FAX - 301-964-9784

WASHINGTON

Representative

Westerberg & Associates
12505 N.E. Bel-Red Rd., #112
Bellevue, WA 98005
Phone - 206-453-8881
FAX - 206-453-8758

Distributors

Anthem Electronics Incorporated
19017-120th Ave. N.E., Suite 102
Bothell, WA 98011
Phone - 206-483-1700
FAX - 206-486-0571

Hall-Mark Electronics Corporation
250 Northwest 39th, Suite #4
Seattle, WA 98107
Phone - 206-547-0415
FAX - 206-632-4814

Wyle Laboratories
15385 NE 90th Street
Redmond, WA 98052-3522
Phone - 206-881-1150
FAX - 206-453-0071

Military Distributor

JAN Devices, Inc.
6925 Canby, Bldg. 109
Reseda, CA 91335
Phone - 818-708-1100
FAX - 818-708-7436

Zeus Components, Inc.
6276 San Ignacio Ave., Suite E
San Jose, CA 95119
Phone - 408-629-4789
FAX - 408-629-4892

WEST VIRGINIA

Representative

Scott Electronics, Inc.
916 Eastwind Drive
Westerville, OH 43081-3379
Phone - 614-882-6100
FAX - 614-882-0900

Distributor

Hall-Mark Electronics Corporation
777 Dearborn Park Lane, Suite L
Worthington, OH 43085
Phone - 614-888-3313
FAX - 614-888-0767

Military Distributor

Zeus Components, Inc.
8930-A Route 108
Columbia, MD 21045
Phone - 301-997-1118
FAX - 301-964-9784

WISCONSIN

Representatives

HMR Incorporated (E. WI)
9065 Lyndale Avenue South
Minneapolis, MN 55420-3520
Phone - 612-888-2122
FAX - 612-884-4768

Industrial Representatives, Inc. (W. WI)
16745 W. Bluemound Road, Suite 340
Brookfield, WI 53005
Phone - 414-789-9393
FAX - 414-789-9272

Distributors

Anthem Electronics, Inc.
1300 Remington, Suite A
Schaumburg, IL 60173
Phone - 708-884-0200
FAX - 708-884-0480

Hall-Mark Electronics Corporation
210 Mittle Drive
Wood Dale, IL 60191
Phone - 708-860-3800
FAX - 708-860-0239

Hall-Mark Electronics Corporation
16255 West Lincoln Avenue
New Berlin, WI 53151
Phone - 414-797-7844
FAX - 414-797-9259

Pioneer Standard
120 Bishops Way, #163
Brookfield, WI 53005
Phone - 414-784-3480
FAX - 414-784-8207

Military Distributors

Zeus Components, Inc.
100 Midland Avenue
Port Chester, NY 10573
Phone - 914-937-7400
FAX - 914-937-2553

Zeus Components, Inc.
2912 Springboro West, Suite 106
Dayton, OH 45439
Phone - 513-293-6162
FAX - 513-293-1781

WYOMING

Representative

Wescom Marketing
3500 South Main, Suite 100
Salt Lake City, UT 84115
Phone - 801-269-0419
FAX - 801- 269-0665

Distributors

Anthem Electronics Incorporated
373 Inverness Drive
Englewood, CO 80112
Phone - 303-790-4500
FAX - 303-790-4532

Wyle Laboratories
1325 West 2200 South, Suite E
West Valley, UT 84119
Phone - 801-974-9953
FAX - 801-972-2524

Military Distributors

JAN Devices, Inc.
6925 Canby, Bldg. 109
Reseda, CA 91335
Phone - 818-708-1100
FAX - 818-708-7436

Zeus Components, Inc.
6276 San Ignacio Ave., Suite E
San Jose, CA 95119
Phone - 408-629-4789
FAX - 408-629-4892

AFRICA

Distributor

Monte Vista International
5976 W. Las Postias Blvd., #220
Pleasanton, CA 94588
Phone - 415-463-8683
FAX - 415-463-8732

AUSTRALIA

Representative

Reptechnic Pty. Ltd.
3/36 Bydown Street
Neutral Bay NSW 2089
Phone - 612-953-9844
FAX - 612-953-9683

AUSTRIA

Representative & Distributor

Thomas Neuroth GmbH
Hietzinger Hauptstrasse 22/A/2
A-1130 Wien
Phone - 431-82-56-45
FAX - 431-82-84-920

BELGIUM

Representative & Distributor

MCA - Tronix SPRL
Parc de Recherches
Du Sart Tilman
Ave. des Noisetiers
B-4031 Angleur
Phone - 32-41-67-4208
FAX - 32-41-67-6331

Microtron
Generaal Dewittelaan
2800 Mechelen
Phone - 32-15-212223
FAX - 32-15-210069

DENMARK

Representative

Delco A/S
Mejeribakken 8
3540 Lynge
Phone - 45-42-18-95-33
FAX - 45-42-18-95-30

Distributor

Prescom A/S
Mejeribakken 8
3540 Lynge
Phone - 45-42-18-98-00
FAX - 45-42-18-98-11

FINLAND

Representative & Distributor

Integrated Electronics OY AB
Turkhaudantie 1
P.O. Box 160
SF-00700 Helsinki
Phone - 358-0-351-3133
FAX - 358-0-351-3134

FRANCE

Representative

Rep'Tronic, SA
1 Bis, rue Marcel Paul
Bâtiment A
Z.I. de la Bonde
91300 Massy
Phone - 33-1-60-13-9300
FAX - 33-1-60-13-9198

Distributors

Arrow Electronique S.A.
73-79, rue des Solets
Silic 585
94663 Rungis Cedex
Phone - 33-1-49-78-4848
FAX - 33-1-49-78-0699

Paris Sud Electronique Composants
12, rue René Cassin
91300 Massy
Phone - 33-1-69-20-6699
FAX - 33-1-69-20-7532

RTF Diffusion
79, rue Pierre Semard
92320 Chatillon
Phone - 33-1-49-65-2600
FAX - 33-1-49-65-2649

Thomson Composants Distribution
30, Avenue de l'Epi d'Or
94807 Villejuif, Cedex
Phone - 33-1-46-87-2224
FAX - 33-1-46-87-0711

GERMANY

Sales & Customer Service Office

Micron Technology (Deutschland) GmbH
Marsstrasse 3
D-8011 Aschheim
Phone - 49-89-903-0021
FAX - 49-89-904-3114

Representative & Distributor

EBV-Elektronik GmbH
Hans-Pinsel-Str. 4
D-8013 Haar b. München
Phone - 49-89-4-60-96-255
FAX - 49-89-46-44-88

Distributors

Metronik GmbH
Leonhardsweg 2
D-8025 Unterhaching b. München
Phone - 49-89-611-08-0
FAX - 49-89-611-22-46

Neumüller GmbH
Eschenstrasse 2
Postfach 1250
D-8028 Taufkirchen
Phone - 49-89-612-08227
FAX - 49-89-612-2680

HONG KONG

Sales & Customer Service Office

Micron Technology Asia
Apt. A, 15/F, Block 3
Pacific View, 38 Tai Tam Road
Phone - 852-813-5609
FAX - 852-813-5914

Representative

Lestina International Ltd.
14/F, Park Tower
15 Austin Road
Tsimshatsui
Phone - 852-735-1736
FAX - 852-730-5260

INDIA

Distributor

Silicon Electronics
3350 Scott Blvd.
Suite 1201
Santa Clara, CA 95054
Phone - 408-988-4408
FAX - 408-988-4431

INDONESIA

Representative

Desner Electronics (FE) Ltd.
42 Mactaggart Road
#04-01 Mactaggart Bldg.
Singapore 1336
Phone - 65-285-1566
FAX - 65-284-9466

IRELAND

Representative

New England Technical Sales
The Diamond
Malahide County Dublin
Phone - 353-1-450635
FAX - 353-1-453625

Distributor

Lyco, Ltd.
Estuary House
New Street
Malahide, Dublin
Phone - 353-1-452-020
FAX - 353-1-451-741

ISRAEL

Representative & Distributor

C.R.G. Electronics, Ltd.
29 Hagaaton Str.
P.O.B. 154
Nahariya 22100
Phone - 972-4-925-819
FAX - 972-4-924-065

ITALY

Representative & Distributor

Moxel S.R.L.
Via C Frova, 34
20092 Cinisello Balsamo (MI)
Phone - 39-261-290521
FAX - 39-261-72582

Distributor

EUR Elettronica S.p.A.
Sede: Via E. Fermi, 8
20094 Assago (MI)
Partita IVA 00883800153
Phone - 02-4880022
FAX - 02-4880275

JAPAN

Distributor

Sanyo Electronic Co., Ltd.
Natsume Bldg., 4th Floor
18-6, 2-Chome, Yushima
Bunkyo-Ku, Tokyo 113
Phone - 81-3-3818-4430
FAX - 81-3-3818-1124

KOREA

Representative

Anam Semiconductor
3rd Floor, Yoowha Bldg.
995-16, Daechi-Dong
Kangnam-Gu, Seoul
Phone - 822-553-2997
FAX - 822-553-2998

MALAYSIA

Representative

Desner Electronics (FE) Ltd.
42 Mactaggart Road
#04-01 Mactaggart Bldg.
Singapore 1336
Phone - 65-285-1566
FAX - 65-284-9466

THE NETHERLANDS

Representative & Distributor

Microtron
Postbus 188
1243 ZK's Graveland
Phone - 31-35-61834
FAX - 31-35-62709

NEW ZEALAND

Representative

Reptechnic
3/36 Bydown Street
Neutral Bay, NSW 2089
Australia
Phone - 612-953-9844
FAX - 612-953-9683

NORWAY

Representative & Distributor

BIT Elektronikk A/S
Smedsvigen 4
P.O. Box 194
1364 Hvalstad
Phone - 47-2-981370
FAX - 47-2-981371

PHILLIPINES

Representative

Desner Electronics (FE) Ltd.
42 Mactaggart Road
#04-01 Mactaggart Bldg.
Singapore 1336
Phone - 65-285-1566
FAX - 65-284-9466

PORTUGAL

Representative & Distributor

ATD Electronica, LDA.
Rua Dr. Faria De Vasconcelos, 3A
1900 Lisboa
Phone - 351-1-847-2196
FAX - 351-1-847-2197

SINGAPORE

Representative

Desner Electronics (FE) Ltd.
42 Mactaggart Road
#04-01 Mactaggart Bldg.
Singapore 1336
Phone - 65-285-1566
FAX - 65-284-9466

SPAIN

Representative & Distributor

ATD Electronica, S.A.
Avda. de la Industria 32
Nave 17, 2o B.
28100 Alcobendas Madrid
Phone - 341-661-6551
FAX - 341-661-6300

SWEDEN

Representative

Gateline AB
Sadelmakarvagen 9, Box 590
S-146 00
Tullinge
Phone - 46-8-778-44-40
FAX - 46-8-778-87-17

Representative & Distributor

IE Komponenter AB
Box 11 113
S-161 11 Bromma
Phone - 46-8-804685
FAX - 46-8-262286

SWITZERLAND

Representative & Distributor

Alltron AG
Hintermättlistr. 3
5506 Mägenwil
Phone - 41-64-56-00-00
FAX - 41-64-56-00-05

TAIWAN, R.O.C.

Representative

ASEC International Corporation
4F, No. 180, Sec. 2
Min-Sheng E. Road
Taipei, Taiwan R.O.C.
Phone - 886-2-505-7025
FAX - 886-2-501-1524

THAILAND

Representative

Desner Electronics (FE) Ltd.
42 Mactaggart Road
#04-01 Mactaggart Bldg.
Singapore 1336
Phone - 65-285-1566
FAX - 65-284-9466

UNITED KINGDOM

Sales & Customer Service Office

Micron Technology (U.K.) Ltd.
Centennial Court
Easthampstead Road
Bracknell
Berkshire RG12 1JA
Phone - 44-344-360055
FAX - 44-344-869504

Assembly & Test Facility

Micron Technology (U.K.) Ltd.
Crompton Way
North Newmoor Industrial Estate
Irvine, Ayrshire, KA11 4DY
Scotland
Phone - 44-294-222400
FAX - 44-294-222404

Representatives

Cedar Technologies (U.K.) Ltd.
Trustrock House
Woodend Estate
Cowdenbeath
Fife KY4 8HW
Phone - 44-383-610-910
FAX - 44-383-610-911

Cedar Technologies (U.K.) Ltd.
The Old Water Works
Howse Lane
Bicester
Oxon OX6 8XF
Phone - 44-869-322-366
FAX - 44-869-322-377

Cedar Technologies (U.K.) Ltd.
131 Bramley Way
Hardwick
Cambridge CB3 7XE
Phone - 44-954-211360
FAX - 44-954-211538

Distributors

Abacus Electronics Holdings Ltd.
Abacus House
Bone Lane
Newbury
Berkshire RG14 5SF
Phone - 44-635-36222
FAX - 44-635-38432

Bytech Components, Ltd.
12 A Cedarwood
Chineham Business Park
Crockford Lane
Basingstoke
Hampshire RG24 OWD
Phone - 44-256-707-107
FAX - 44-256-707-162

Force Technologies, Ltd.
Unit 18
Campbell Court
Bramley
Basingstoke
Hampshire RG26 5EG
Phone - 44-256-880788
FAX - 44-256-880307

Thame Components, Ltd.
Thame Park Road
Thame
Oxfordshire OX9 3UQ
Phone - 44-84-426-1188
FAX - 44-84-426-1681

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MICRON TECHNOLOGY, INC.

DYNAMIC RAMS 1

WIDE DRAMS 2

DRAM MODULES 3

IC DRAM CARDS 4

MULTIPORT DRAMS 5

APPLICATION/TECHNICAL NOTES 6

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MICRON TECHNOLOGY, INC.

1 ..... DYNAMIC RAMS

2 ..... WIDE DRAMS

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5 ..... MULTIPORT DRAMS

6 ..... APPLICATION/TECHNICAL NOTES

7 ..... PRODUCT RELIABILITY

8 ..... PACKAGE INFORMATION

9 ..... SALES INFORMATION

Micron Technology, Inc.
2805 East Columbia Road
Boise, Idaho 83706
Telephone: (208) 368-3900
FAX: (208) 368-4431
Customer Comment Line (USA): (800) 932-4992
Customer Comment Line (Intl.): (208) 368-3410