MACRONIX INC.

MACRONIX INC.™

MEMORY DATA BOOK

MEMORY DATA BOOK 1993-1994

MACRONIX, INC.

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MEMORY DATA BOOK

The Company

Macronix Inc., a leader in high density non-volatile memory technology, designs, manufactures, and markets high performance ROMs, EPROMs and FLASH memory components for the world's most sophisticated computers, data communication devices and electronics products.

Dedicated to providing a wide range of advanced communication solutions, the company's innovative product line includes integrated FAX modems, LAN controllers and UARTs, as well as high resolution graphic and PC chip sets.

History

Macronix Inc., operational since 1987 was founded by former members of the VLSI Technology Inc. start-up group. The dynamic Macronix management team has more than eighty years combined experience in the semiconductor field and is committed to providing the most advanced VLSI solutions for the worldwide electronics industry. Headquartered in San Jose, the company has grown significantly and will continue to expand to serve the rapidly evolving global electronics market.

Dedicated to innovative design, superior quality products and responsive customer service, Macronix is one of the major U.S. semiconductor suppliers providing total turnkey solutions and a fully compatible product line for ROM, EPROM and FLASH memory.

Macronix International was established December, 1989 in Taiwan to provide a world class semiconductor fabrication facility to meet the industry's needs on a more global scale. A member of the Semiconductor Industry Association (SIA) since 1990, Macronix has formed significant alliances around the world.

Quality Assurance

Dedicated to the highest level of quality assurance, Macronix has invested significant capital in the most advanced manufacturing and testing equipment to insure the superior quality and reliability that is so critical in large volume production.

Quality and reliability are built into products throughout the development and manufacturing stages, then verified through rigorous testing, characterization and qualification phases before shipping.

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MX27C1000/1001	1M	(128K x 8)	CMOS EPROM	8-1
MX27C1024	1M	(128K x 8)	CMOS EPROM	9-1
MX27C1100	1M	(128K x 8/64K x 16)	CMOS EPROM	9-1
MX27C2000	2M	(256K x 8)	CMOS EPROM	10-1
MX27C2048	2M	(128K x 16)	CMOS EPROM	11-1
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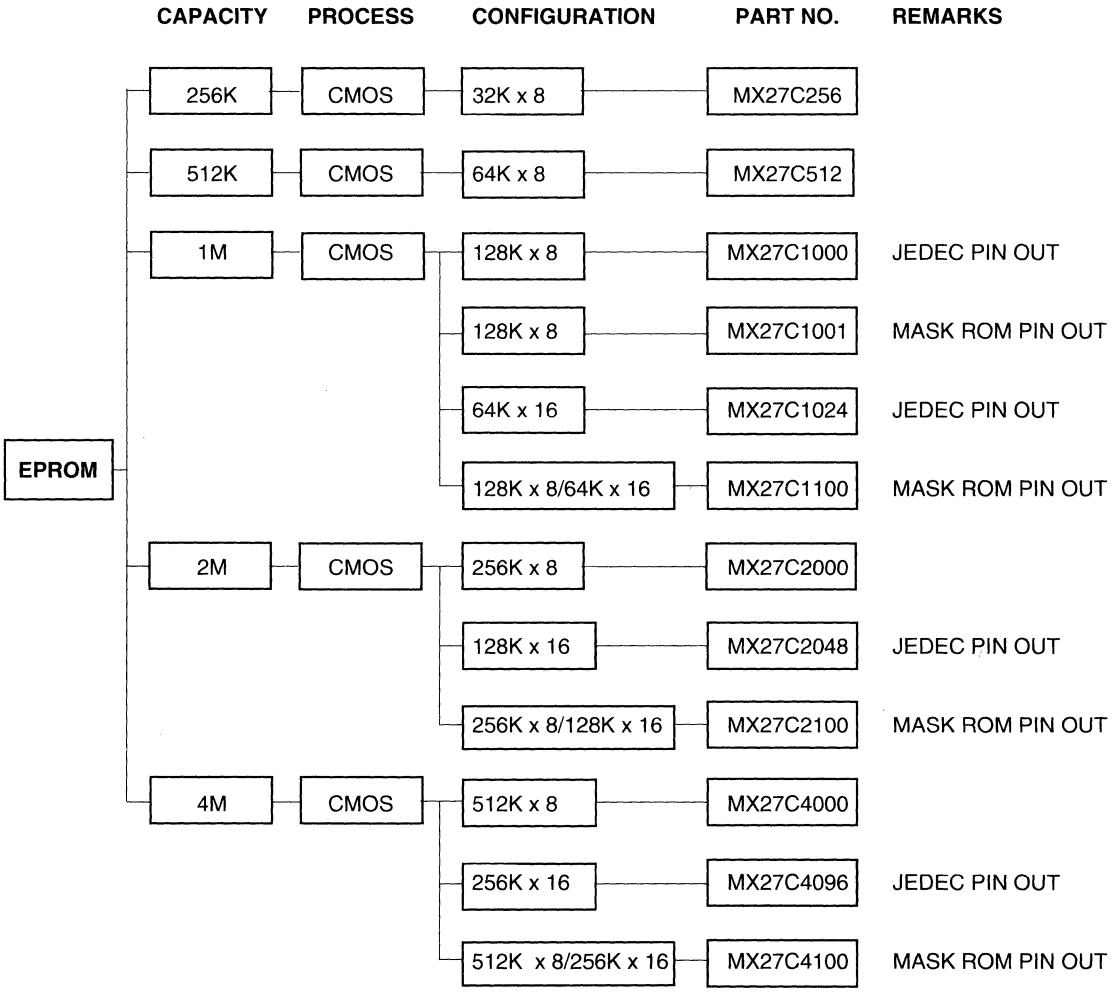
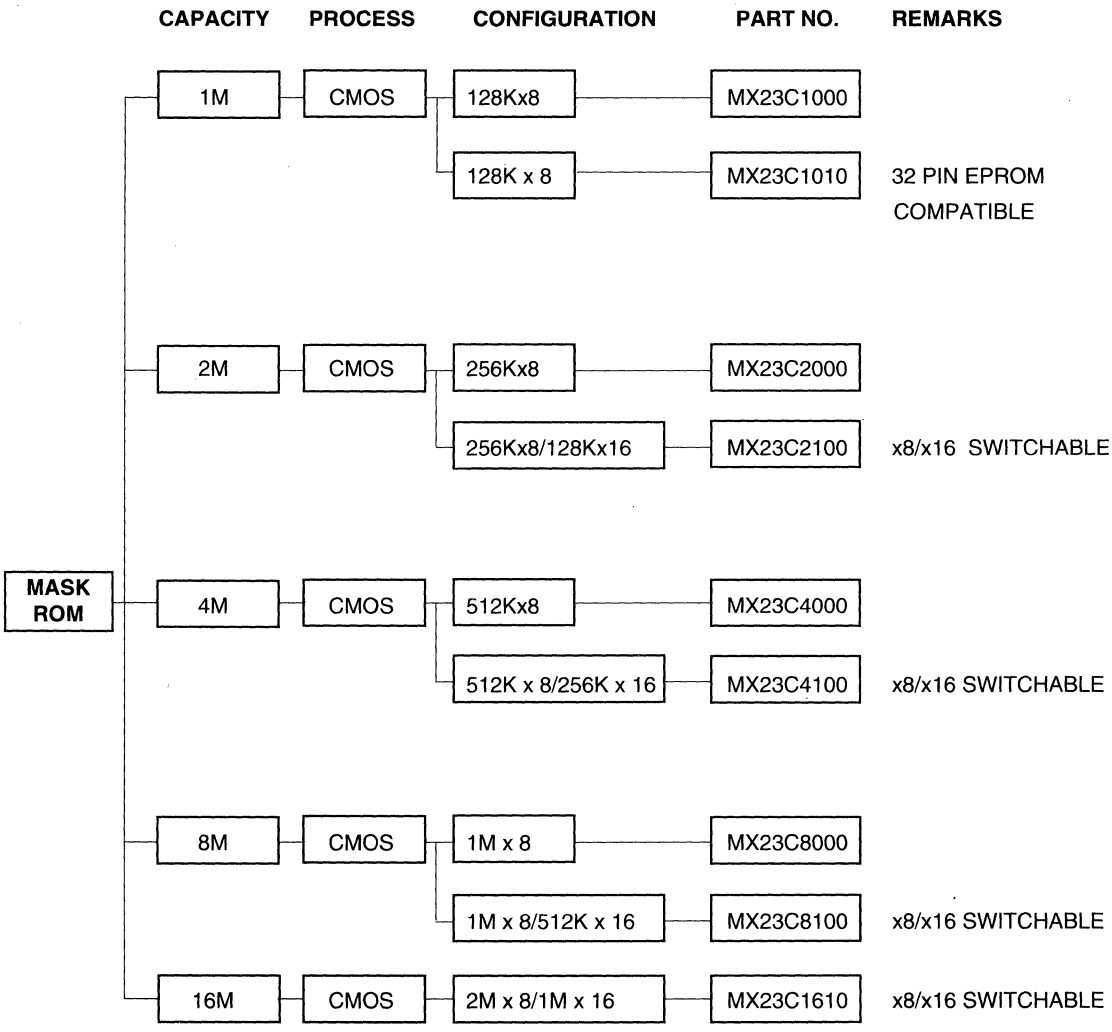
2. PRODUCT INTRODUCTION

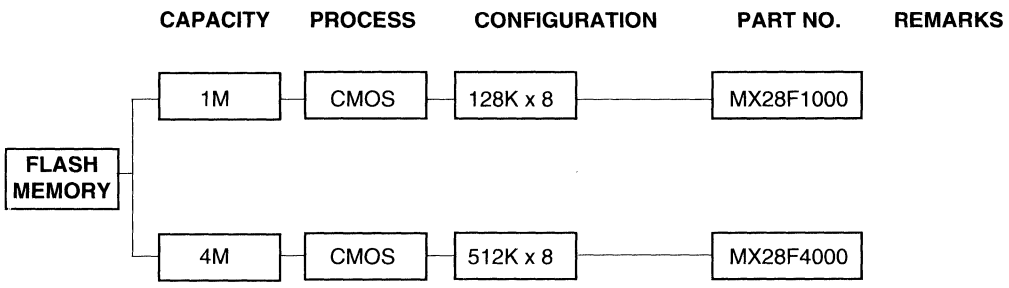
2-1. EPROM



2-2. MASK ROM


CAPACITY
PROCESS
CONFIGURATION
PART NO.
REMARKS
MASK ROM
1M
CMOS
128Kx8
MX23C1000
128K x 8
MX23C1010
32 PIN EPROM COMPATIBLE
2M
CMOS
256Kx8
MX23C2000
256Kx8/128Kx16
MX23C2100
x8/x16 SWITCHABLE
4M
CMOS
512Kx8
MX23C4000
512K x 8/256K x 16
MX23C4100
x8/x16 SWITCHABLE
8M
CMOS
1M x 8
MX23C8000
1M x 8/512K x 16
MX23C8100
x8/x16 SWITCHABLE
16M
CMOS
2M x 8/1M x 16
MX23C1610
x8/x16 SWITCHABLE

2-3. FLASH MEMORY



3. PRODUCT SELECTION GUIDE

3.1 EPROM

CAPACITY	PART NUMBER	CONFIGURATION	SPEED (NS)	TECHNOLOGY	PACKAGE
256K	MX27C256DC	32K x 8	55/70/90/100/120/150	CMOS	28 PIN CERAMIC DIP
	MX27C256PC	32K x 8	55/70/90/100/120/150	CMOS	28 PIN PLASTIC DIP
	MX27C256MC	32K x 8	55/70/90/100/120/150	CMOS	28 PIN PLASTIC SOP
	MX27C256QC	32K x 8	55/70/90/100/120/150	CMOS	32 PIN PLCC
512K	MX27C512DC	64K x 8	55/70/90/100/120/150	CMOS	28 PIN CERAMIC DIP
	MX27C512PC	64K x 8	55/70/90/100/120/150	CMOS	28 PIN PLASTIC DIP
	MX27C512MC	64K x 8	55/70/90/100/120/150	CMOS	28 PIN PLASTIC SOP
	MX27C512QC	64K x 8	55/70/90/100/120/150	CMOS	32 PIN PLCC
1M	MX27C1000DC	128K x 8	55/70/90/120/150	CMOS	32 PIN CERAMIC DIP
	MX27C1000PC	128K x 8	55/70/90/120/150	CMOS	32 PIN PLASTIC DIP
	MX27C1000QC	128K x 8	55/70/90/120/150	CMOS	32 PIN PLCC
	MX27C1000MC	128K x 8	55/70/90/120/150	CMOS	32 PIN PLASTIC SOP
	MX27C1001DC	128K x 8	70/90/120/150	CMOS	32 PIN CERAMIC DIP
	MX27C1024DC	64K x 16	90/120/150	CMOS	40 PIN CERAMIC DIP
	MX27C1024PC	64K x 16	90/120/150	CMOS	40 PIN PLASTIC DIP
	MX27C1024QC	64K x 16	90/120/150	CMOS	44 PIN PLCC
	MX27C1100DC	128K x 8/64K x 16	90/120/150	CMOS	40 PIN CERAMIC DIP
	MX27C1100PC	128K x 8/64K x 16	90/120/150	CMOS	40 PIN PLASTIC DIP
2M	MX27C2000DC	256K x 8	90/120/150	CMOS	32 PIN CERAMIC DIP
	MX27C2000PC	256K x 8	90/120/150	CMOS	32 PIN PLASTIC DIP
	MX27C2048DC	128K x 16	90/120/150	CMOS	40 PIN CERAMIC DIP
	MX27C2048PC	128K x 16	90/120/150	CMOS	40 PIN PLASTIC DIP
	MX27C2048QC	128K x 16	90/120/150	CMOS	44 PIN PLCC
	MX27C2100DC	256K x 8/128K x16	90/120/150	CMOS	40 PIN CERAMIC DIP
	MX27C2100PC	256K x 8/128K x16	90/120/150	CMOS	40 PIN PLASTIC DIP
4M	MX27C4000DC	512K x 8	120/150	CMOS	32 PIN CERAMIC DIP
	MX27C4000PC	512K x 8	120/150	CMOS	32 PIN PLASTIC DIP
	MX27C4096DC	256K x 16	120/150	CMOS	40 PIN CERAMIC DIP
	MX27C4096PC	256K x 16	120/150	CMOS	40 PIN PLASTIC DIP
	MX27C4096QC	256K x 16	120/150	CMOS	44 PIN PLCC
	MX27C4100DC	512K x 8/256K x 16	120/150	CMOS	40 PIN CERAMIC DIP
	MX27C4100PC	512K x 8/256K x 16	120/150	CMOS	40 PIN PLASTIC DIP

3.2 MASK ROM

CAPACITY	PART NUMBER	CONFIGURATION	SPEED (NS)	TECHNOLOGY	PACKAGE
1M	MX23C1000PC	128K x 8	150/200	CMOS	28 PIN PLASTIC DIP
	MX23C1000MC	128K x 8	150/200	CMOS	28 PIN PLASTIC SOP
	MX23C1010PC	128K x 8	150/200	CMOS	32 PIN PLASTIC DIP
	MX23C1010MC	128K x 8	150/200	CMOS	32 PIN PLASTIC SOP
2M	MX23C2000PC	256K x 8	150/200	CMOS	32 PIN PLASTIC DIP
	MX23C2000MC	256K x 8	150/200	CMOS	32 PIN PLASTIC SOP
	MX23C2100PC	256K x 8/128K x16	150/200	CMOS	40 PIN PLASTIC DIP
4M	MX23C4000PC	512K x 8	120/150/200	CMOS	32 PIN PLASTIC DIP
	MX23C4000MC	512K x 8	120/150/200	CMOS	32 PIN PLASTIC SOP
	MX23C4100PC	512K x 8/256K x16	120/150/200	CMOS	40 PIN PLASTIC DIP
8M	MX23C8000PC	1M x 8	120/150/200	CMOS	32 PIN PLASTIC DIP
	MX23C8000MC	1M x 8	120/150/200	CMOS	32 PIN PLASTIC SOP
	MX23C8100PC	1M x 8/512K x16	120/150/200	CMOS	42 PIN PLASTIC DIP
	MX23C8100MC	1M x 8/512K x16	120/150/200	CMOS	44 PIN PLASTIC SOP
16M	MX23C1610PC	2M x 8/1M x 16	120/150/200	CMOS	42 PIN PLASTIC DIP
	MX23C1610MC	2M x 8/1M x 16	120/150/200	CMOS	44 PIN PLASTIC SOP

3.3 FLASH MEMORY

CAPACITY	PART NUMBER	CONFIGURATION	SPEED (NS)	TECHNOLOGY	PACKAGE
1M	MX28F1000PC	128K x 8	120/150/200	CMOS	32 PIN PLASTIC DIP
	MX28F1000MC	128K x 8	120/150/200	CMOS	32 PIN PLASTIC SOP
	MX28F1000QC	128K x 8	120/150/200	CMOS	32 PIN PLCC
	MX28F1000TC	128K x 8	120/150/200	CMOS	32 PIN PLASTIC TSOP
4M	MX28F4000PC	512K x 8	120/150/200	CMOS	32 PIN PLASTIC DIP
	MX28F4000MC	512K x 8	120/150/200	CMOS	32 PIN PLASTIC SOP
	MX28F4000TC	512K x 8	120/150/200	CMOS	32 PIN PLASTIC TSOP

4. CROSS-REFERENCE GUIDE

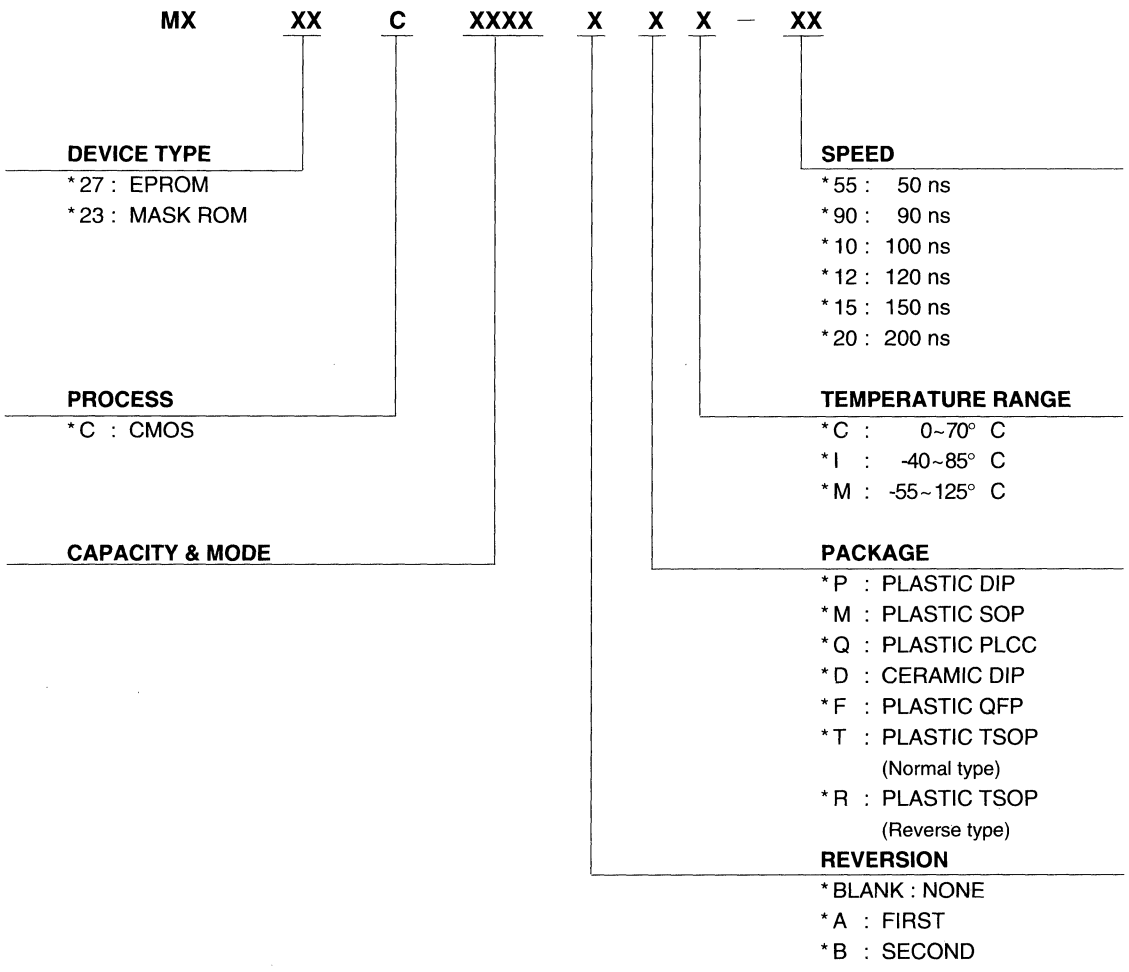
4.1 EPROM

CAPACITY	CONFIGRUATION	MACRONIX	INTEL	AMD	N.S.	S.G.S.	NEC	TOSHIBA	HITACHI	FUJITSU	MITSUBISHI	TI
256K	32K x 8	MX27C256	i27C256	Am27C256	NMC27C256	M27C256	μPD27C256	TC57256	HN27C256	MB27C256	M5M27C256	TMS27C256
512K	64K x 8	MX27C512	i27C512	Am27C512	NMC27C512	M27C512	μPD27C512	TC57512	HN27C512	MB27C512	M5M27C512	TMS27C512
1M	128K x 8	MX27C1000	i27C010	Am27C010	NMC27C010	M27C1001	μPD27C1001	TC571000	HN27C101	MB27C1001	M5M27C101	TMS27C010
	128K x 8	MX27C1001				M27C1000		TC571001	HN27C301	MB27C1000		
	64K x 16	MX27C1024	i27C210	Am27C1024	NMC27C1024	M27C1024	μPD27C1024	TC571024	HN27C1024	MB27C1024	M5M27C102	
	64K x 16/128Kx 8	MX27C1100										
2M	256K x 8	MX27C2000	i27C020	Am27C020	NMC27C020	M27C2001	μPD27C2001				M5M27C201	TMS27C020
	64K x 16	MX27C2048		Am27C2048	NMC27C2048						M5M27C202	
	64K x 16/256K x8	MX27C2100										
4M	512K x 8	MX27C4000	i27C040	Am27C040		M27C4001	μPD27C4001	TC574000	HN27C4001	MB27C4000	M5M27C401	TMS27C040
	256K x 16	MX27C4096	i27C240	Am27C4096		M27C4002	μPD27C4096	TC574096	HN27C4096	MB27C4096	M5M27C402	TMS27C240
	256K x 16/512Kx8	MX27C4100	i27C400				μPD27C4000	TC574200				

4.2 MASK ROM

CAPACITY	CONFIGURATION	MACRONIX	SHARP	NEC	TOSHIBA	HITACHI	FUJITSU	MITSUBISHI	SAMSUNG
1M	128K x 8	MX23C1000	LH531000	μPD23C1000	TC531000	HN62321	MB831000		KM23C1000
	128K x 8	MX23C1010	LH530800	μPD23C1001	TC531001				KM23C1010
			LH530900						
2M	256K x 8	MX23C2000	LH532100	μPD23C2001	TC532000	HN62302	MB832000		KM23C2000
	256K x 8/128Kx16	MX23C2100	LH532000						KM23C2100
4M	512K x 8	MX23C4000	LH534300	μPD23C4000	TC534000	HN62314	MB834000	M5M23401	KM23C4000
	512K x 8/256Kx16	MX23C4100	LH534000	μPD23C4001	TC534200	HN62414	MB834100	M5M23400	KM23C4100
8M	1M x 8	MX23C8000	LH538100	μPD23C8001	TC538000	HN62328	MB838000	M5M23801	KM23C8000
	1M x 8/512Kx16	MX23C8100	LH538000	μPD23C8000	TC538200	HN62428	MB838200	M5M23800	KM23C8100
16M	2M x 8/1Mx16	MX23C1610	LH5316000	μPD23C16000	TC5316200	HN624017		M5M23160	KM23C1610

5. ORDERING INFORMATION



II. EPROM

(ERASABLE PROGRAMMABLE READ ONLY MEMORY)

MX27C256

256K-BIT(32K x 8) CMOS EPROM

FEATURES

- 32K x 8 organization
- Single +5V power supply
- +12.5V programming voltage
- Fast access time: 55/70/90/100/120/150 ns
- Totally static operation
- Completely TTL compatible
- Operating current: 40mA
- Standby current: 100μA
- Package type:
  - 28 pin ceramic DIP, plastic DIP
  - 32 pin PLCC

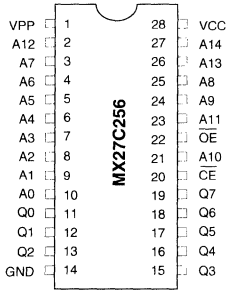
GENERAL DESCRIPTION

The MX27C256 is a 5V only, 256K-bit, ultraviolet Erasable Programmable Read Only Memory. It is organized as 32K by 8 bits, operates from a single + 5volt supply, has a static standby mode, and features fast single address location programming. All programming signals are TTL levels, requiring a single pulse. For programming from outside the system, existing EPROM programmers may be used. The MX27C256 supports intelligent quick pulse programming algorithm which can result in programming times of less than ten seconds.

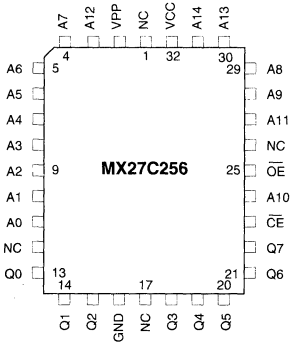
This EPROM is packaged in industry standard 28 pin, dual-in-line packages or 32 lead, PLCC packages.

PIN CONFIGURATIONS

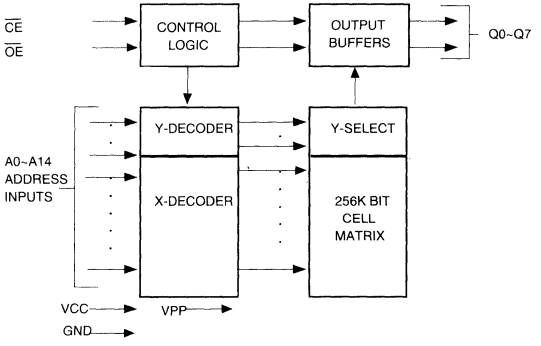
CDIP/PDIP



PLCC



BLOCK DIAGRAM



PIN DESCRIPTION

SYMBOL	PIN NAME
A0~A14	Address Input
Q0~Q7	Data Input/Output
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
VPP	Program Supply Voltage
NC	No Internal Connection
VCC	Power Supply Pin (+5V)
GND	Ground Pin

FUNCTIONAL DESCRIPTION

THE ERASURE OF THE MX27C256

The MX27C256 is erased by exposing the chip to an ultraviolet light source. A dosage of 15 W seconds/cm2 is required to completely erase a MX27C256. This dosage can be obtained by exposure to an ultraviolet lamp — wavelength of 2537 Angstroms (Å) — with intensity of 12,000 μW/cm2 for 15 to 20 minutes. The MX27C256 should be directly under and about one inch from the source and all filters should be removed from the UV light source prior to erasure.

It is important to note that the MX27C256, and similar devices, will be cleared for all bits of their programmed states with light sources having wavelengths shorter than 4000 Å. Although erasure times will be much longer than that with UV sources at 2537Å, nevertheless the exposure to fluorescent light and sunlight will eventually erase the MX27C256 and exposure to them should be prevented to realize maximum system reliability. If used in such an environment, the package window should be covered by an opaque label or substance.

THE PROGRAMMING OF THE MX27C256

When the MX27C256 is delivered, or it is erased, the chip has all 256K bits in the "ONE", or HIGH state. "ZEROs" are loaded into the MX27C256 through the procedure of programming.

The programming mode is entered when 12.5 ± 0.5 V is applied to the Vpp pin, $\overline{OE}$ is at VIH, and $\overline{CE}$ is at VIL.

For programming, the data to be programmed is applied with 8 bits in parallel to the data pins.

The flowchart in Figure 1 shows MXIC's interactive algorithm. Interactive algorithm reduces programming time by using short programming pulses and giving each address only as many pulses as is necessary in order to reliably program the data. After each pulse is applied to a given address, the data in that address is verified. If the data is not verified, additional pulses are given until it is verified or the maximum is reached. This process is repeated while sequencing through each address of the MX27C256. This part of the algorithm is done at VCC= 6.0V to assure that each EPROM bit is programmed to a sufficiently high threshold voltage. After the interactive programming is completed, an overprogram pulse is given to each memory location; this ensures that all bits have sufficient margin. After the final address is completed, the entire EPROM memory is verified at VCC = 5V ± 10%.

FAST PROGRAMMING

The device is set up in the fast programming mode when the programming voltage VPP = 12.75V is applied, with VCC = 6.25 V and $\overline{OE}$ = VIH (Algorithm is shown in Figure 2). The programming is achieved by applying a single TTL low level 100μs pulse to the $\overline{CE}$ input after addresses and data line are stable. If the data is not verified, an additional pulse is applied for a maximum of 25 pulses. This process is repeated while sequencing through each address of the device. When the programming mode is completed, the data in all address is verified at VCC = VPP = 5V ± 10%.

PROGRAM INHIBIT MODE

Programming of multiple MX27C256s in parallel with different data is also easily accomplished by using the Program Inhibit Mode. Except for $\overline{CE}$ and $\overline{OE}$, all like inputs of the parallel MX27C256 may be common. A TTL low-level program pulse applied to an MX27C256 $\overline{CE}$ input with VPP = 12.5 ± 0.5 V and $\overline{OE}$ HIGH will program that MX27C256. A high-level $\overline{CE}$ input inhibits the other MX27C256s from being programmed.

PROGRAM VERIFY MODE

Verification should be performed on the programmed bits to determine that they were correctly programmed. The verification should be performed with $\overline{CE}$ at VIH, $\overline{OE}$ at VIL and VPP at its programming voltage.

AUTO IDENTIFY MODE

The auto identify mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and device type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ± 5°C ambient temperature range that is required when programming the MX27C256.

To activate this mode, the programming equipment must force 12.0 ± 0.5 (VH) on address line A9 of the device. Two identifier bytes may then be sequenced from the device outputs by toggling address line A0 from VIL to VIH. All other address lines must be held at VIL during

auto identify mode.

Byte 0 (A0 = VIL) represents the manufacturer code, and byte 1 (A0 = VIH), the device identifier code. For the MX27C256, these two identifier bytes are given in the Mode Select Table. All identifiers for manufacturer and device codes will possess odd parity, with the MSB (DQ7) defined as the parity bit.

READ MODE

The MX27C256 has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (tACC) is equal to the delay from $\overline{CE}$ to output (tCE). Data is available at the outputs tOE after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been LOW and addresses have been stable for at least tACC - tOE.

STANDBY MODE

The MX27C256 has a CMOS standby mode which reduces the maximum Vcc current to 100 μA. It is placed in CMOS standby when $\overline{CE}$ is at VCC ± 0.3 V. The MX27C256 also has a TTL-standby mode which reduces the maximum VCC current to 1.5 mA. It is placed in TTL-standby when $\overline{CE}$ is at VIH. When in standby mode, the outputs are in a high-impedance state, independent of the $\overline{OE}$ input.

TWO-LINE OUTPUT CONTROL FUNCTION

To accommodate multiple memory connections, a two-line control function is provided to allow for:

1. Low memory power dissipation,
2. Assurance that output bus contention will not occur.

It is recommended that $\overline{CE}$ be decoded and used as the primary device-selecting function, while $\overline{OE}$ be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low-power standby mode and that the output pins are only active when data is desired from a particular memory device.

SYSTEM CONSIDERATIONS

During the switch between active and standby conditions, transient current peaks are produced on the rising and falling edges of Chip Enable. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. At a minimum, a 0.1 μF ceramic capacitor (high frequency, low inherent inductance) should be used on each device between VCC and GND to minimize transient effects. In addition, to overcome the voltage drop caused by the inductive effects of the printed circuit board traces on EPROM arrays, a 4.7 μF bulk electrolytic capacitor should be used between Vcc and GND for each eight devices. The location of the capacitor should be close to where the power supply is connected to the array.

MODE SELECT TABLE

	PINS					
MODE	**$\overline{CE}$**	**$\overline{OE}$**	**A0**	**A9**	**VPP**	**OUTPUTS**
Read	VIL	VIL	X	X	VCC	DOUT
Output Disable	VIL	VIH	X	X	VCC	High Z
Standby (TTL)	VIH	X	X	X	VCC	High Z
Standby (CMOS)	VCC±0.3V	X	X	X	VCC	High Z
Program	VIL	VIH	X	X	VPP	DIN
Program Verify	VIH	VIL	X	X	VPP	DOUT
Program Inhibit	VIH	VIH	X	X	VPP	High Z
Manufacturer Code	VIL	VIL	VIL	VH	VCC	C2H
Device Code	VIL	VIL	VIH	VH	VCC	10H

NOTES: 1. X can be either VIL or VIH
2. VH = 12.0 V ± 0.5 V
3. A1 - A8 = A10 - A12 = VIL(For auto select)
4. A13 and A14 = X (For auto select)
5. See DC Programming characteristics for VPP voltage during programming.

FIGURE 1. INTERACTIVE PROGRAMMING FLOW CHART

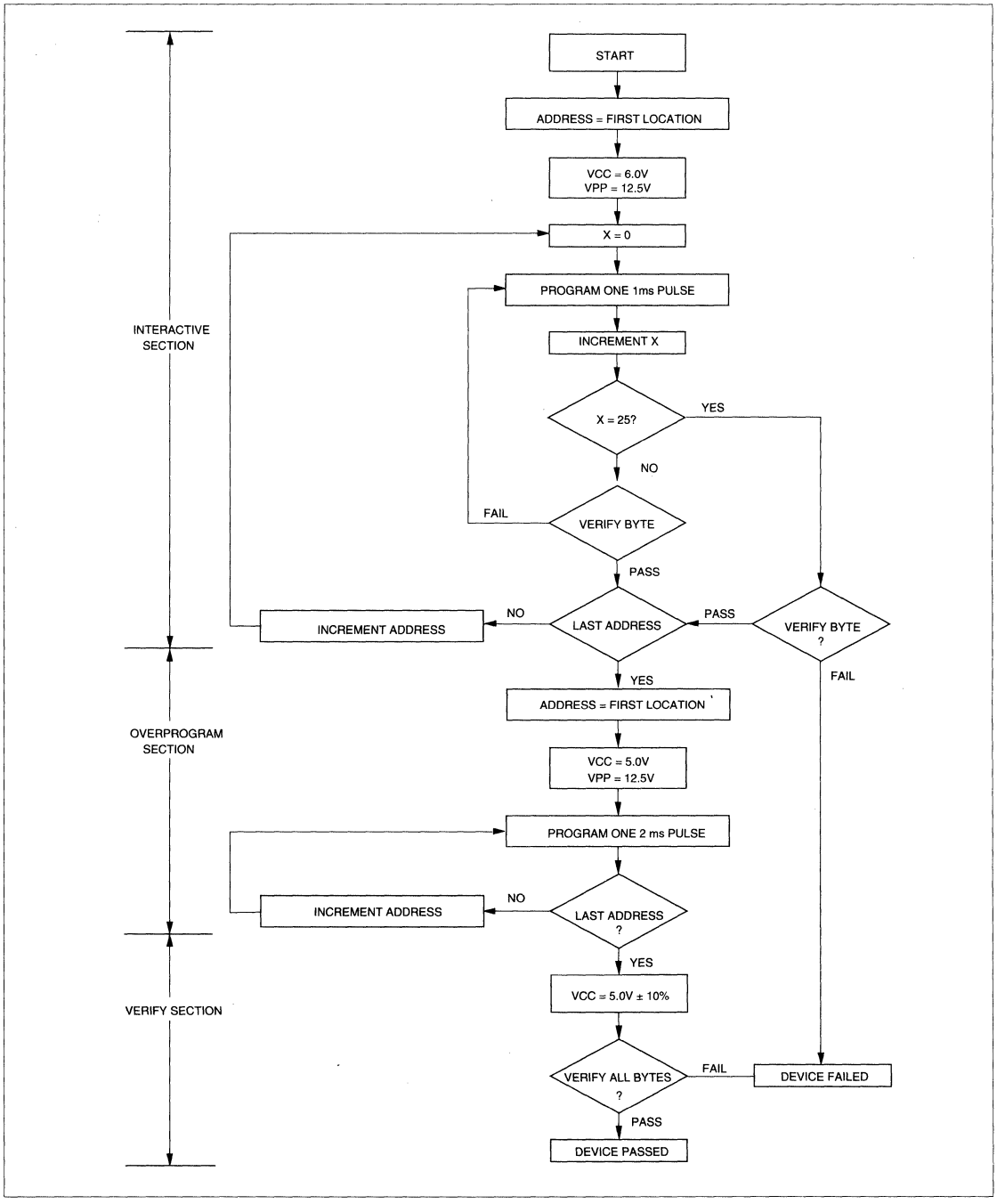
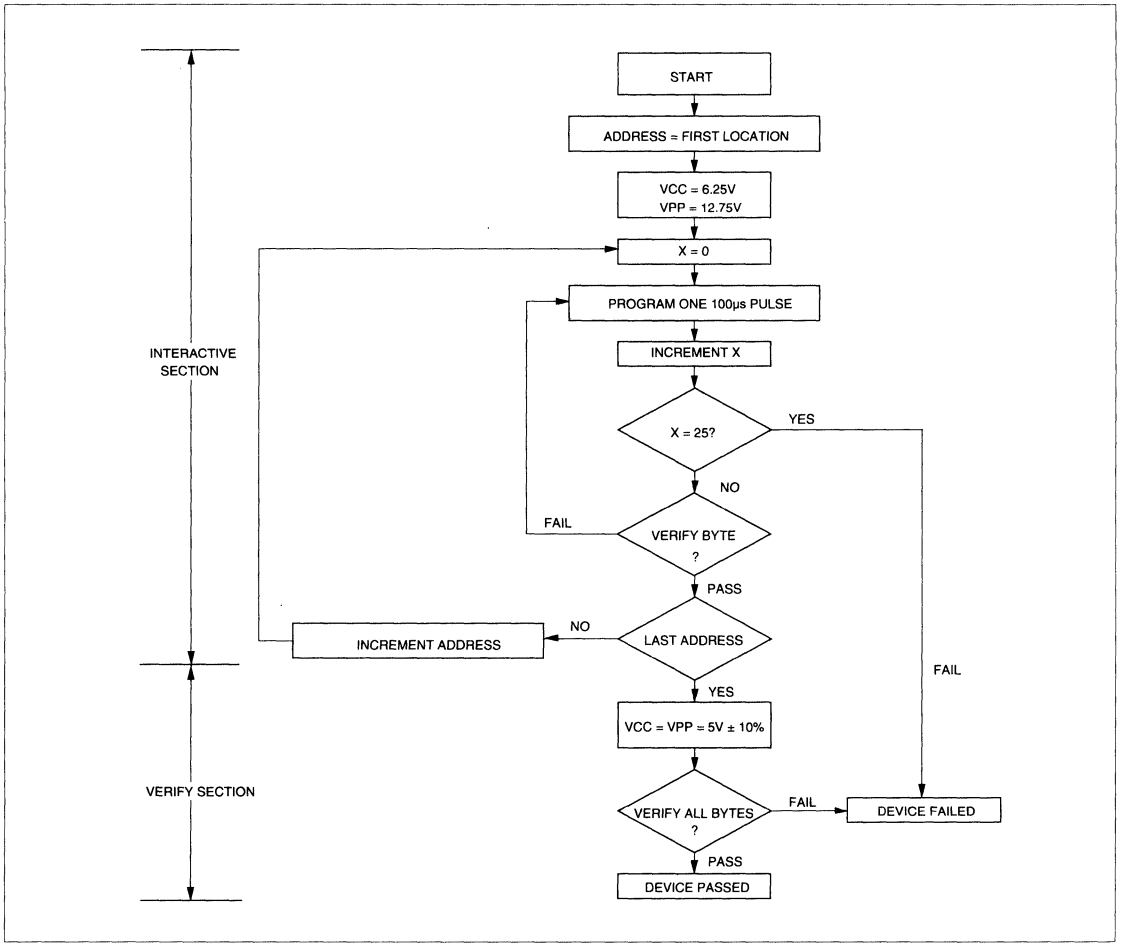
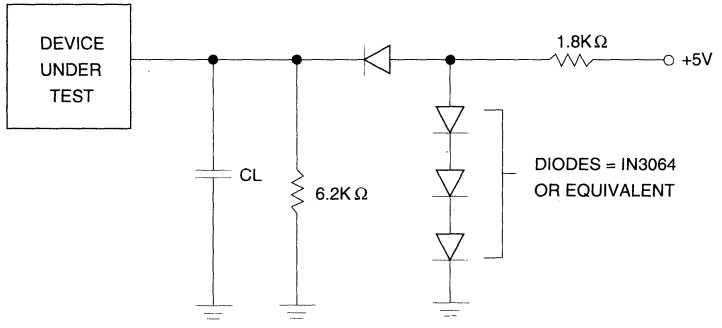


FIGURE 2. FAST PROGRAMMING FLOW CHART

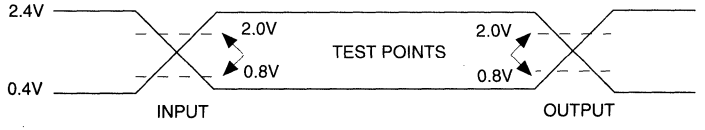


SWITCHING TEST CIRCUITS

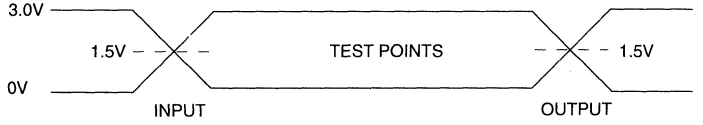


CL = 100 pF including jig capacitance(30pF for 55/70 ns parts)

SWITCHING TEST WAVEFORMS



AC TESTING: Inputs are driven at 2.4V for a logic "1" and 0.4V for a logic "0".
Input pulse rise and fall times are ≤10ns.



AC TESTING: (1) Inputs are driven at 3.0V for a logic "1" and 0V for a logic "0".
Input pulse rise and fall times are ≤10ns.
(2) For MX27C256-55, MX27C256-70 only

ABSOLUTE MAXIMUM RATINGS

RATING	VALUE
Ambient Operating Temperature	0°C to 70°C
Storage Temperature	-65°C to 125°C
Applied Input Voltage	-0.5V to 7.0V
Applied Output Voltage	-0.5V to VCC + 0.5V
VCC to Ground Potential	-0.5V to 7.0V
A9 & Vpp	-0.5V to 13.5V

NOTICE:
Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended period may affect reliability.

NOTICE:
Specifications contained within the following tables are subject to change.

DC CHARACTERISTICS TA = 0°C to 70°C, VCC = 5V ± 10%

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
VOH	Output High Voltage	2.4		V	IOH = -0.4mA
VOL	Output Low Voltage		0.4	V	IOL = 2.1mA
VIH	Input High Voltage	2.0	VCC + 0.5	V	
VIL	Input Low Voltage	-0.3	0.8	V	
ILI	Input Leakage Current	-10	10	µA	VIN = 0 to 5.5V
ILO	Output Leakage Current	-10	10	µA	VOUT = 0 to 5.5V
ICC3	VCC Power-Down Current		100	µA	$\overline{CE}$ = VCC ± 0.3V
ICC2	VCC Standby Current		1.5	mA	$\overline{CE}$ = VIH
ICC1	VCC Active Current		40	mA	$\overline{CE}$ = VIL, f=5MHz, Iout = 0mA
IPP	VPP Supply Current Read		100	µA	$\overline{CE}$ = $\overline{OE}$ = VIL, VPP = 5.5V

CAPACITANCE TA = 25°C, f = 1.0 MHz (Sampled only)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
CIN	Input Capacitance	8	12	pF	VIN = 0V
COUT	Output Capacitance	8	12	pF	VOUT = 0V
VPP	VPP Capacitance	18	25	pF	VPP = 0V

AC CHARACTERISTICS TA = 0°C to 70°C, VCC = 5V± 10%

		27C256-55		27C256-70		27C256-90			
SYMBOL	PARAMETER	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	UNIT	CONDITIONS
tACC	Address to Output Delay		55		70		90	ns	$\overline{CE}$ = $\overline{OE}$ = VIL
tCE	Chip Enable to Output Delay		55		70		90	ns	$\overline{OE}$ = VIL
tOE	Output Enable to Output Delay		30		35		40	ns	$\overline{CE}$ = VIL
tDF	$\overline{OE}$ High to Output Float, or $\overline{CE}$ High to Output Float	0	20	0	20	0	25	ns	
tOH	Output Hold from Address, $\overline{CE}$ or $\overline{OE}$ which ever occurred first	0		0		0		ns	

		27C256-10		27C256-12		27C256-15			
SYMBOL	PARAMETER	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	UNIT	CONDITIONS
tACC	Address to Output Delay		100		120		150	ns	$\overline{CE}$ = $\overline{OE}$ = VIL
tCE	Chip Enable to Output Delay		100		120		150	ns	$\overline{OE}$ = VIL
tOE	Output Enable to Output Delay		45		50		55	ns	$\overline{CE}$ = VIL
tDF	$\overline{OE}$ High to Output Float, or $\overline{CE}$ High to Output Float	0	30	0	35	0	50	ns	
tOH	Output Hold from Address, $\overline{CE}$ or $\overline{OE}$ which ever occurred first	0		0		0		ns	

DC PROGRAMMING CHARACTERISTICS TA = 25°C ± 5°C

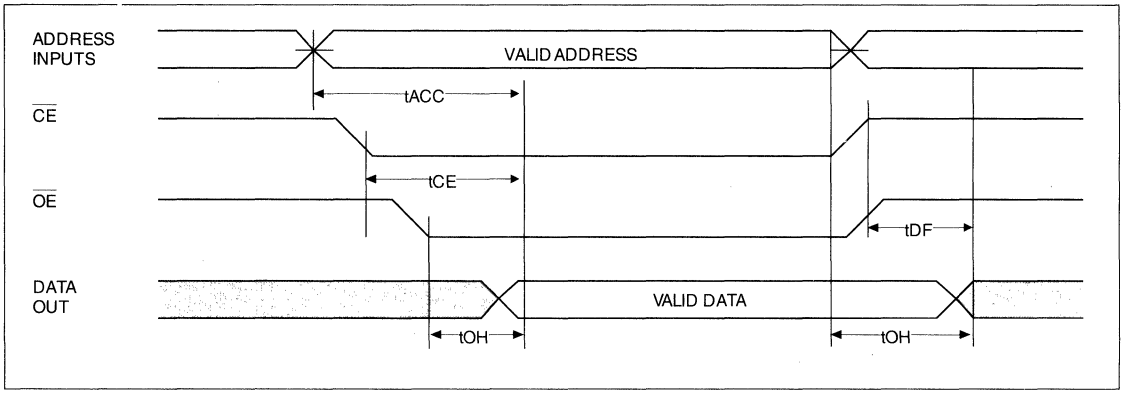
SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
VOH	Output High Voltage	2.4		V	IOH = -0.40mA
VOL	Output Low Voltage		0.4	V	IOL = 2.1mA
VIH	Input High Voltage	2.0	VCC + 0.5	V	
VIL	Input Low Voltage	-0.3	0.8	V	
ILI	Input Leakage Current	-10	10	μA	VIN = 0 to 5.5V
VH	A9 Auto Select Voltage	11.5	12.5	V	
ICC3	VCC Supply Current(Program & Verify)		40	mA	
IPP2	VPP Supply Current(Program)		30	mA	$\overline{CE}$ = VIL, $\overline{OE}$ = VIH
VCC1	Interactive Supply Voltage	5.75	6.25	V	
VPP1	Interactive Programming Voltage	12.0	13.0	V	
VCC2	Fast Programming Supply Voltage	6.00	6.50	V	
VPP2	Fast Programming Voltage	12.5	13.0	V	

AC PROGRAMMING CHARACTERISTICS TA = 25°C ± 5°C

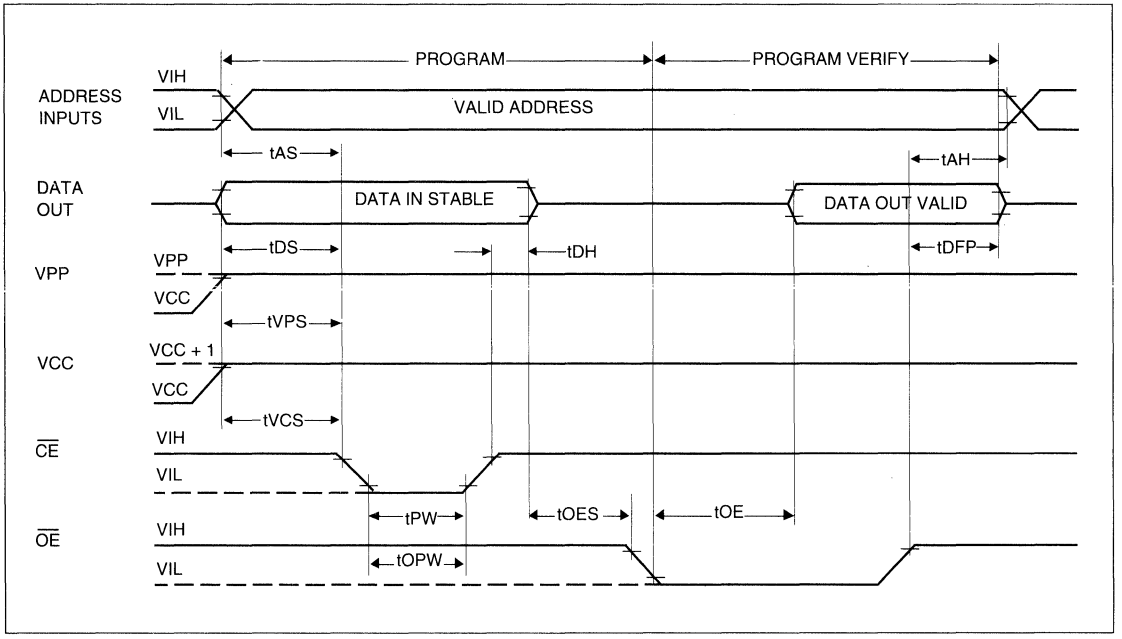
SYMBOL	PARAMETER		MIN.	MAX.	UNIT	CONDITIONS
tAS	Address Setup Time		2.0		µS	
tOES	$\overline{OE}$ Setup Time		2.0		µS	
tDS	Data Setup Time		2.0		µS	
tAH	Address Hold Time		0		µS	
tDH	Data Hold Time		2.0		µS	
tDFP	$\overline{CE}$ to Output Float Delay		0	50	nS	
tVPS	VPP Setup Time		2.0		µS	
tVCS	VCC Setup Time		2.0		µS	
tOE	Data Valid from $\overline{OE}$			150	nS	
tPW	$\overline{CE}$ Initial Program Pulse Width	*Fast*	95	105	µS	
		Interactive	0.95	1.05	mS	
tOPW	$\overline{CE}$ Over program Pulse Width (Interactive)		1.95	2.05	mS	
tDV	Data Valid from $\overline{CE}$			250	nS	
tOEH	$\overline{OE}$ Hold Time		2.0		µS	
tVR	$\overline{OE}$ Recovery Time		2.0		µS	

WVEFORMS

READ CYCLE



INTERACTIVE PROGRAMMING ALGORITHM WAVEFORMS



ORDERING INFORMATION

CERAMIC PACKAGE

PART NO.	ACCESS TIME(ns)	OPERATING CURRENT MAX.(mA)	STANDBY CURRENT MAX.(μ A)	PACKAGE
MX27C256DC-55	55	40	100	28 Pin DIP
MX27C256DC-70	70	40	100	28 Pin DIP
MX27C256DC-90	90	40	100	28 Pin DIP
MX27C256DC-10	100	40	100	28 Pin DIP
MX27C256DC-12	120	40	100	28 Pin DIP
MX27C256DC-15	150	40	100	28 Pin DIP

PLASTIC PACKAGE

PART NO.	ACCESS TIME(ns)	OPERATING CURRENT MAX.(mA)	STANDBY CURRENT MAX.(μ A)	PACKAGE
MX27C256PC-55	55	40	100	28 Pin DIP
MX27C256QC-55	55	40	100	32 Pin PLCC
MX27C256PC-70	70	40	100	28 Pin DIP
MX27C256QC-70	70	40	100	32 Pin PLCC
MX27C256PC-90	90	40	100	28 Pin DIP
MX27C256QC-90	90	40	100	32 Pin PLCC
MX27C256PC-12	120	40	100	28 Pin DIP
MX27C256QC-12	120	40	100	32 Pin PLCC
MX27C256PC-15	150	40	100	28 Pin DIP
MX27C256QC-15	150	40	100	32 Pin PLCC

MX27C512

512K-BIT(64K x 8) CMOS EPROM

FEATURES

- 64K x 8 organization
- Single +5V power supply
- +12.5V programming voltage
- Fast access time: 55/70/90/100/120/150ns
- Totally static operation
- Completely TTL compatible
- Operating current: 40mA
- Standby current: 100μA
- Package type:
  - 28 pin ceramic DIP, plastic DIP
  - 32 pin PLCC

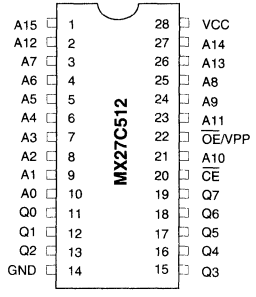
GENERAL DESCRIPTION

The MX27C512 is a 5V only, 512K-bit, ultraviolet Erasable Programmable Read Only Memory. It is organized as 64K words by 8 bits per word, operates from a single +5volt supply, has a static standby mode, and features fast single address location programming. All programming signals are TTL levels, requiring a single pulse. For programming outside from the system, existing EPROM programmers may be used. The MX27C512 supports intelligent quick pulse programming algorithm which can result in programming times of less than fifteen seconds.

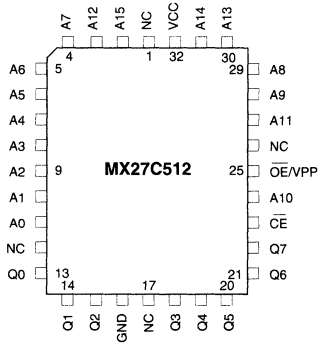
This EPROM is packaged in industry standard 28 pin, dual-in-line packages or 32 lead, PLCC packages.

PIN CONFIGURATIONS

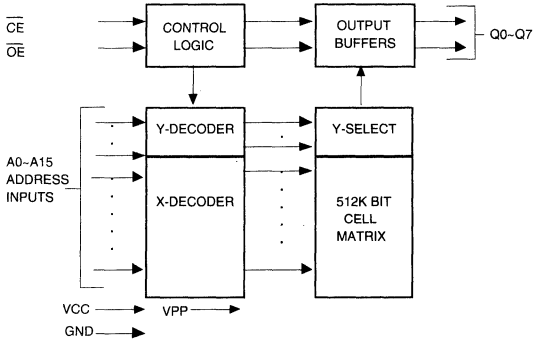
CDIP/PDIP



PLCC



BLOCK DIAGRAM



PIN DESCRIPTION

SYMBOL	PIN NAME
A0~A15	Address Input
Q0~Q7	Data Input/Output
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
VPP	Program Supply Voltage
NC	No Internal Connection
VCC	Power Supply Pin (+5V)
GND	Ground Pin

FUNCTIONAL DESCRIPTION

THE ERASURE OF THE MX27C512

The MX27C512 is erased by exposing the chip to an ultraviolet light source. A dosage of 15 W seconds/cm2 is required to completely erase a MX27C512. This dosage can be obtained by exposure to an ultraviolet lamp — wavelength of 2537 Angstroms (Å) — with intensity of 12,000 μW/cm2 for 15 to 20 minutes. The MX27C512 should be directly under and about one inch from the source and all filters should be removed from the UV light source prior to erasure.

It is important to note that the MX27C512, and similar devices, will be cleared for all bits of their programmed states with light sources having wavelengths shorter than 4000 Å. Although erasure times will be much longer than that with UV sources at 2537Å, nevertheless the exposure to fluorescent light and sunlight will eventually erase the MX27C512 and exposure to them should be prevented to realize maximum system reliability. If used in such an environment, the package window should be covered by an opaque label or substance.

THE PROGRAMMING OF THE MX27C512

When the MX27C512 is delivered, or it is erased, the chip has all 512K bits in the "ONE", or HIGH state. "ZEROs" are loaded into the MX27C512 through the procedure of programming.

The programming mode is entered when 12.5 ± 0.5 V is applied to the OE/VPP pin and CE is at VIL.

For programming, the data to be programmed is applied with 8 bits in parallel to the data pins.

The flowchart in Figure 1 shows MXIC's interactive algorithm. Interactive algorithm reduces programming time by using short programming pulses and giving each address only as many pulses as is necessary in order to reliably program the data. After each pulse is applied to a given address, the data in that address is verified. If the data is not verified, additional pulses are given until it is verified or the maximum is reached. This process is repeated while sequencing through each address of the MX27C512. This part of the algorithm is done at VCC = 6.0V to assure that each EPROM bit is programmed to a sufficiently high threshold voltage. After the interactive programming is completed, an overprogram pulse is given to each memory location; this ensures that all bits have sufficient margin. After the final address is completed, the entire EPROM memory is verified at VCC = 5V ± 10%.

FAST PROGRAMMING

The device is set up in the fast programming mode when the programming voltage OE/VPP = 12.75V is applied, with VCC = 6.25 V, (Algorithm is shown in Figure 2). The programming is achieved by appling a single TTL low level 100μs pulse to the CE input after addresses and data line are stable. If the data is not verified, an additional pulse is applied for a maximum of 25 pulses. This process is repeated while sequencing through each address of the device. When the programming mode is completed, the data in all address is verified at VCC = 5V ± 10%.

PROGRAM INHIBIT MODE

Programming of multiple MX27C512s in parallel with different data is also easily accomplished by using the Program Inhibit Mode. Except for CE and OE, all like inputs of the parallel MX27C512 may be common. A TTL low-level program pulse applied to an MX27C512 CE input with OE/VPP = 12.5 ± 0.5V will program that MX27C512. A high-level CE input inhibits the other MX27C512s from being programmed.

PROGRAM VERIFY MODE

Verification should be performed on the programmed bits to determine that they were correctly programmed. The verification should be performed with OE/VPP and CE, at VIL. Data should be verified tDV after the falling edge of CE.

AUTO IDENTIFY MODE

The auto identify mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and device type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ± 5°C ambient temperature range that is required when programming the MX27C512.

To activate this mode, the programming equipment must force 12.0 ± 0.5(VH) on address line A9 of the device. Two identifier bytes may then be sequenced from the device outputs by toggling address line A0 from VIL to VIH. All other address lines must be held at VIL during auto identify mode.

Byte 0 (A0 = VIL) represents the manufacturer code, and byte 1 (A0 = VIH), the device identifier code. For the MX27C512, these two identifier bytes are given in the Mode Select Table. All identifiers for manufacturer and device codes will possess odd parity, with the MSB (DQ7) defined as the parity bit.

READ MODE

The MX27C512 has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable (CE) is the power control and should be used for device selection. Output Enable (OE) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (tACC) is equal to the delay from CE to output (tCE). Data is available at the outputs tOE after the falling edge of OE, assuming that CE has been LOW and addresses have been stable for at least tACC - tOE.

STANDBY MODE

The MX27C512 has a CMOS standby mode which reduces the maximum VCC current to 100 μA. It is placed in CMOS standby when CE is at VCC ± 0.3 V. The MX27C512 also has a TTL-standby mode which reduces the maximum VCC current to 1.5 mA. It is placed in TTL-standby when CE is at VIH. When in standby mode, the outputs are in a high-impedance state, independent of the OE input.

TWO-LINE OUTPUT CONTROL FUNCTION

To accommodate multiple memory connections, a two-line control function is provided to allow for:

1. Low memory power dissipation,
2. Assurance that output bus contention will not occur.

It is recommended that CE be decoded and used as the primary device-selecting function, while OE be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low-power standby mode and that the output pins are only active when data is desired from a particular memory device.

SYSTEM CONSIDERATIONS

During the switch between active and standby conditions, transient current peaks are produced on the rising and falling edges of Chip Enable. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. At a minimum, a 0.1 μF ceramic capacitor (high frequency, low inherent inductance) should be used on each device between VCC and GND to minimize transient effects. In addition, to overcome the voltage drop caused by the inductive effects of the printed circuit board traces on EPROM arrays, a 4.7 μF bulk electrolytic capacitor should be used between VCC and GND for each eight devices. The location of the capacitor should be close to where the power supply is connected to the array.

MODE SELECT TABLE

	PINS				
MODE	**CE**	**OE/VPP**	**A0**	**A9**	**OUTPUTS**
Read	VIL	VIL	X	X	DOUT
Output Disable	VIL	VIH	X	X	High Z
Standby (TTL)	VIH	X	X	X	High Z
Standby (CMOS)	VCC±0.3V	X	X	X	High Z
Program	VIL	VPP	X	X	DIN
Program Verify	VIL	VIL	X	X	DOUT
Program Inhibit	VIH	VPP	X	X	High Z
Manufacturer Code	VIL	VIL	VIL	VH	C2H
Device Code	VIL	VIL	VIH	VH	91H

NOTES: 1. VH = 12.0 V ± 0.5 V
2. X = Either VIH or VIL(For auto select)
3. A1 - A8 = A10 - A15 = VIL(For auto select)
4. See DC Programming Characteristics for VPP voltage during programming.

FIGURE 1. INTERACTIVE PROGRAMMING FLOW CHART

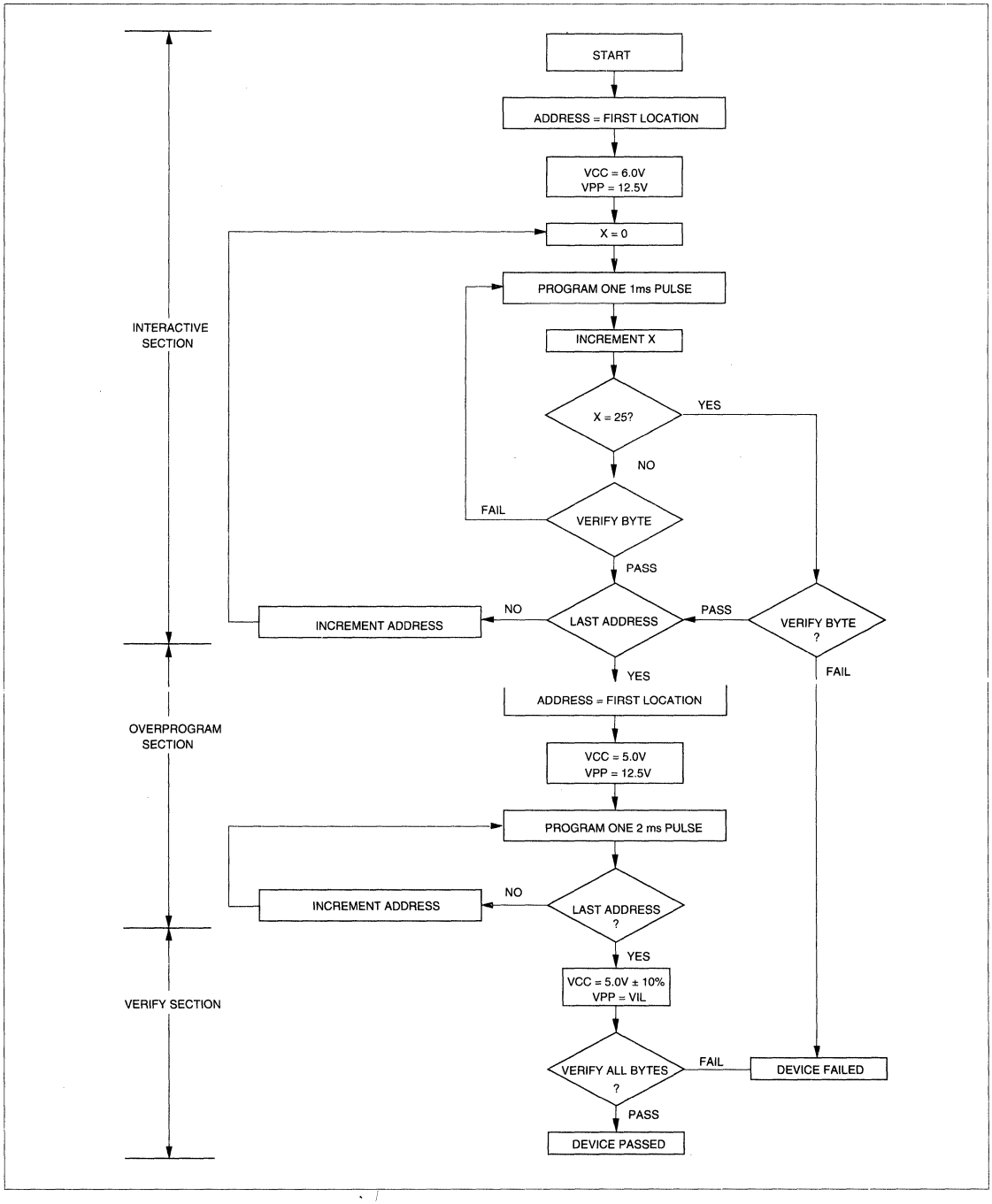
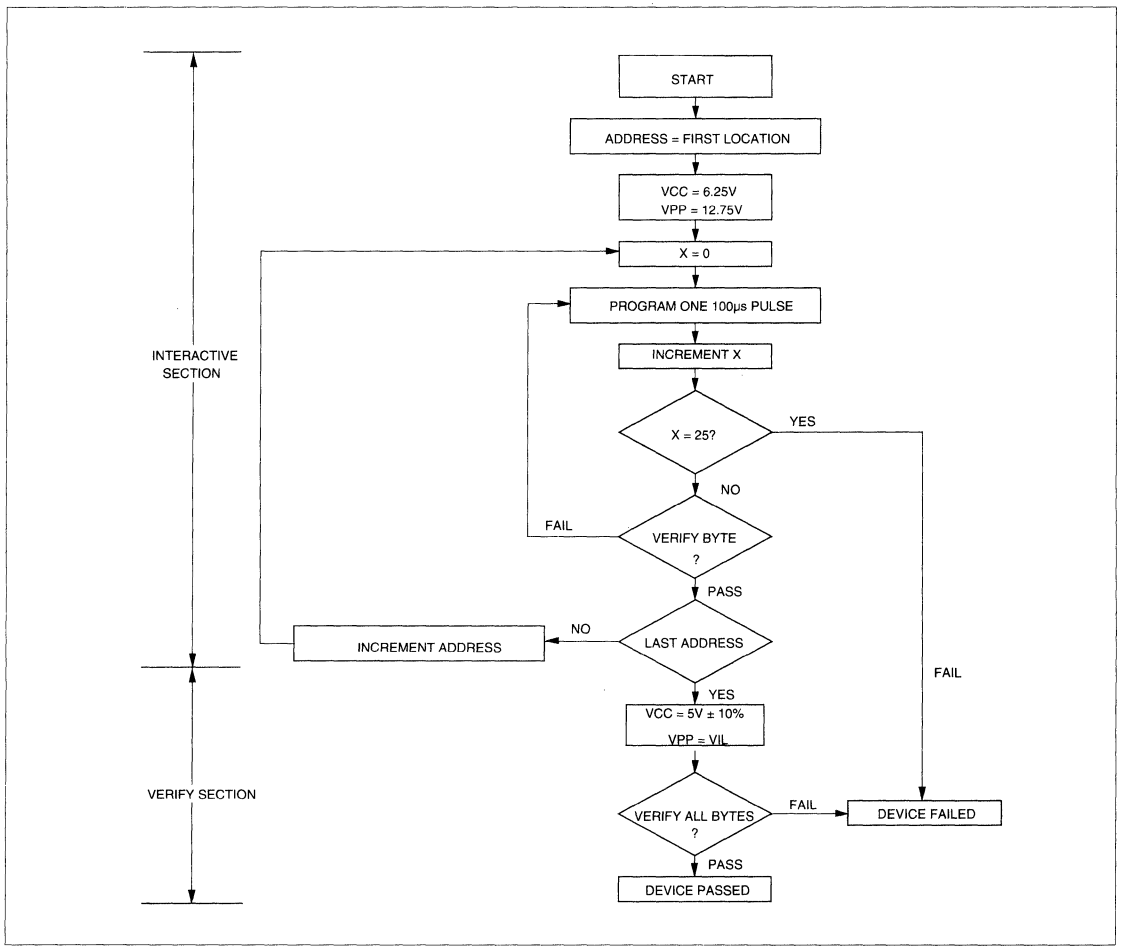
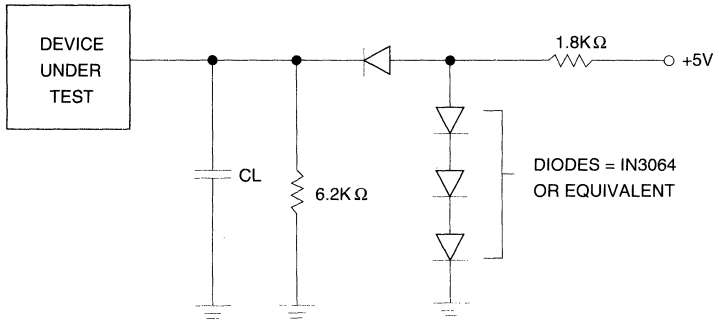


FIGURE 2. FAST PROGRAMMING FLOW CHART

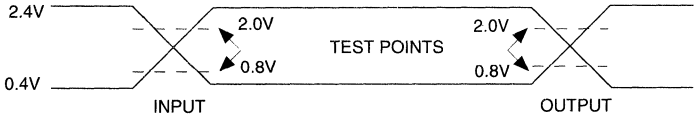


SWITCHING TEST CIRCUITS

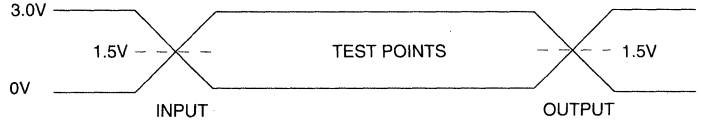


CL = 100 pF including jig capacitance(30pF for 55/70 ns parts)

SWITCHING TEST WAVEFORMS



AC TESTING: Inputs are driven at 2.4V for a logic "1" and 0.4V for a logic "0".
Input pulse rise and fall times are ≤ 10ns.



AC TESTING: (1) Inputs are driven at 3.0V for a logic "1" and 0V for a logic "0".
Input pulse rise and fall times are ≤10ns.
(2) For MX27C512-55, MX27C512-70 only

ABSOLUTE MAXIMUM RATINGS

RATING	VALUE
Ambient Operating Temperature	0°C to 70°C
Storage Temperature	-65°C to 125°C
Applied Input Voltage	-0.5V to 7.0V
Applied Output Voltage	-0.5V to VCC + 0.5V
VCC to Ground Potential	-0.5V to 7.0V
A9 & Vpp	-0.5V to 13.5V

NOTICE:
Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended period may affect reliability.

NOTICE:
Specifications contained within the following tables are subject to change.

DC CHARACTERISTICS TA = 0°C to 70°C, VCC = 5V ± 10%

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
VOH	Output High Voltage	2.4		V	IOH = -0.4mA
VOL	Output Low Voltage		0.4	V	IOL = 2.1mA
VIH	Input High Voltage	2.0	VCC + 0.5	V	
VIL	Input Low Voltage	-0.2	0.8	V	
ILI	Input Leakage Current	-10	10	µA	VIN = 0 to 5.5V
ILO	Output Leakage Current	-10	10	µA	VOUT = 0 to 5.5V
ICC3	VCC Power-Down Current		100	µA	$\overline{CE}$ = VCC ± 0.3V
ICC2	VCC Standby Current		1.5	mA	$\overline{CE}$ = VIH
ICC1	VCC Active Current		40	mA	$\overline{CE}$ = VIL, f=5MHz, Iout = 0mA
IPP	VPP Supply Current Read		100	µA	$\overline{CE}$ = VIL, VPP = 5.5V

CAPACITANCE TA = 25°C, f = 1.0 MHz (Sampled only)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
CIN	Input Capacitance	8	12	pF	VIN = 0V
COUT	Output Capacitance	8	12	pF	VOUT = 0V
Vpp	VPP Capacitance	18	25	pF	VPP = 0V

AC CHARACTERISTICS TA = 0°C to 70°C, VCC = 5V± 10%

		27C512-55		27C512-70		27C512-90			
SYMBOL	PARAMETER	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	UNIT	CONDITIONS
tACC	Address to Output Delay		55		70		90	ns	$\overline{CE}$ = $\overline{OE}$ = VIL
tCE	Chip Enable to Output Delay		55		70		90	ns	$\overline{OE}$ = VIL
tOE	Output Enable to Output Delay		30		35		40	ns	$\overline{CE}$ = VIL
tDF	$\overline{OE}$ High to Output Float, or $\overline{CE}$ High to Output Float	0	20	0	20	0	25	ns	
tOH	Output Hold from Address, $\overline{CE}$ or $\overline{OE}$ which ever occurred first	0		0		0		ns	

		27C512-10		27C512-12		27C512-15			
SYMBOL	PARAMETER	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	UNIT	CONDITIONS
tACC	Address to Output Delay		100		120		150	ns	$\overline{CE}$ = $\overline{OE}$ = VIL
tCE	Chip Enable to Output Delay		100		120		150	ns	$\overline{OE}$ = VIL
tOE	Output Enable to Output Delay		45		50		65	ns	$\overline{CE}$ = VIL
tDF	$\overline{OE}$ High to Output Float, or $\overline{CE}$ High to Output Float	0	30	0	35	0	50	ns	
tOH	Output Hold from Address, $\overline{CE}$ or $\overline{OE}$ which ever occurred first	0		0		0		ns	

DC PROGRAMMING CHARACTERISTICS TA = 25°C ± 5°C

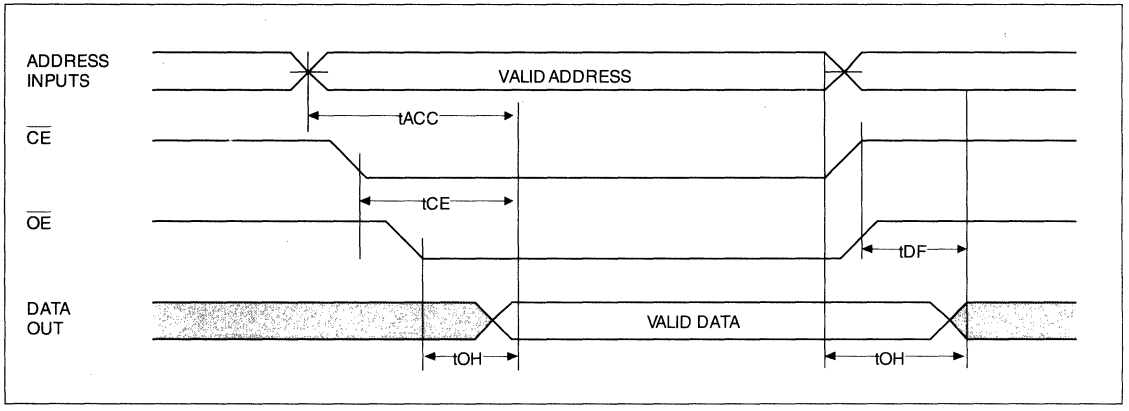
SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
VOH	Output High Voltage	2.4		V	IOH = -0.40mA
VOL	Output Low Voltage		0.4	V	IOL = 2.1mA
VIH	Input High Voltage	2.0	VCC + 0.5	V	
VIL	Input Low Voltage	-0.2	0.8	V	
ILI	Input Leakage Current	-10	10	μA	VIN = 0 to 5.5V
VH	A9 Auto Select Voltage	11.5	12.5	V	
ICC3	VCC Supply Current(Program & Verify)		40	mA	
IPP2	VPP Supply Current(Program)		30	mA	$\overline{CE}$ = VIL
VCC1	Interactive Supply Voltage	5.75	6.25	V	
VPP1	Interactive Programming Voltage	12.0	13.0	V	
VCC2	Fast Programming Supply Voltage	6.00	6.50	V	
VPP2	Fast Programming Voltage	12.5	13.0	V	

AC PROGRAMMING CHARACTERISTICS TA = 25°C ± 5°C

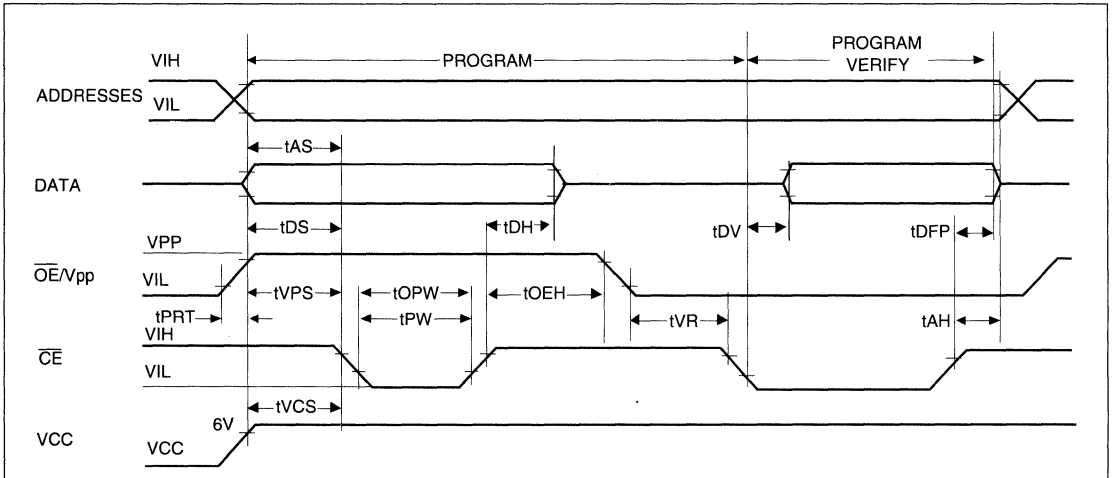
SYMBOL	PARAMETER		MIN.	MAX.	UNIT	CONDITIONS
tAS	Address Setup Time		2.0		µS	
tOES	$\overline{OE}$/VPP Setup Time		2.0		µS	
tDS	Data Setup Time		2.0		µS	
tAH	Address Hold Time		0		µS	
tDH	Data Hold Time		2.0		µS	
tDFP	$\overline{CE}$ to Output Float Delay		0	60	nS	
tVPS	VPP Setup Time		2.0		µS	
tPW	$\overline{CE}$ Initial Program Pulse Width	*Fast*	95	105	µS	
		Interactive	0.95	1.05	mS	
tOPW	$\overline{CE}$ Overprogram Pulse Width(Interactive)		1.95	2.05	mS	
tVCS	VCC Setup Time		2.0		µS	
tDV	Data Valid from $\overline{CE}$			250	nS	
tOEH	$\overline{OE}$/VPP Hold Time		2.0		µS	
tVR	$\overline{OE}$/VPP Recovery Time		2.0		µS	

WAVEFORMS

READ CYCLE



INTERACTIVE PROGRAMMING ALGORITHM WAVEFORMS



NOTES:

1. The input timing reference level is 0.8V for VIL and 2V for VIH.
2. tOE and tDFP are characteristics of the device, but must be accomodated by the programmer.

ORDERING INFORMATION

CERAMIC PACKAGE

PART NO.	ACCESS TIME(ns)	OPERATING CURRENT MAX.(mA)	STANDBY CURRENT MAX.(μ A)	PACKAGE
MX27C512DC-55	55	40	100	28 Pin DIP
MX27C512DC-70	70	40	100	28 Pin DIP
MX27C512DC-90	90	40	100	28 Pin DIP
MX27C512DC-10	100	40	100	28Pin DIP
MX27C512DC-12	120	40	100	28Pin DIP
MX27C512DC-15	150	40	100	28 Pin DIP

PLASTIC PACKAGE

PART NO.	ACCESS TIME(ns)	OPERATING CURRENT MAX.(mA)	STANDBY CURRENT MAX.(μ A)	PACKAGE
MX27C512PC-55	55	40	100	28 Pin DIP
MX27C512QC-55	55	40	100	32 Pin PLCC
MX27C512PC-70	70	40	100	28 Pin DIP
MX27C512QC-70	70	40	100	32 Pin PLCC
MX27C512PC-90	90	40	100	28 Pin DIP
MX27C512QC-90	90	40	100	32 Pin PLCC
MX27C512PC-12	120	40	100	28Pin DIP
MX27C512QC-12	120	40	100	32 Pin PLCC
MX27C512PC-15	150	40	100	28 Pin DIP
MX27C512QC-15	150	40	100	32 Pin PLCC

FEATURES

- 128K x 8 organization
- Single +5V power supply
- +12.5V programming voltage
- Fast access time: 55/70/90/120/150 ns
- Totally static operation
- Completely TTL compatible
- Operating current: 60mA
- Standby current: 100μA
- Package type:
  - 32 pin ceramic DIP, plastic DIP
  - 32 pin SOP
  - 32 pin PLCC

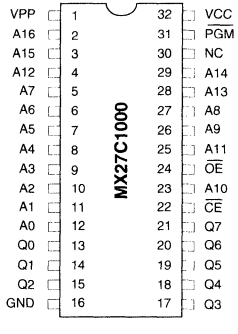
GENERAL DESCRIPTION

The MX27C1000/27C1001 is a 5V only, 1M-bit, ultraviolet Erasable Programmable Read Only Memory. It is organized as 128K words by 8 bits per word, operates from a single + 5 volt supply, has a static standby mode, and features fast single address location programming. All programming signals are TTL levels, requiring a single pulse. For programming outside from the system, existing EPROM programmers may be used. The MX27C1000/27C1001 supports a intelligent quick pulse programming algorithm which can result in programming times of less than thirty seconds.

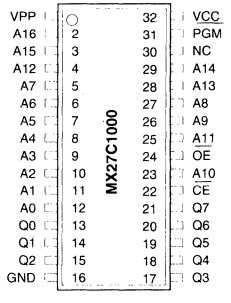
This EPROM is packaged in industry standard 32 pin dual-in-line packages or 32 lead, PLCC packages.

PIN CONFIGURATIONS

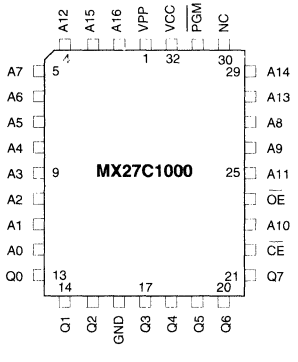
CDIP/PDIP(MX27C1000)



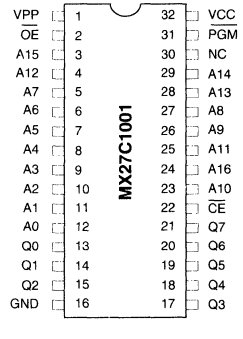
SOP(MX27C1000)



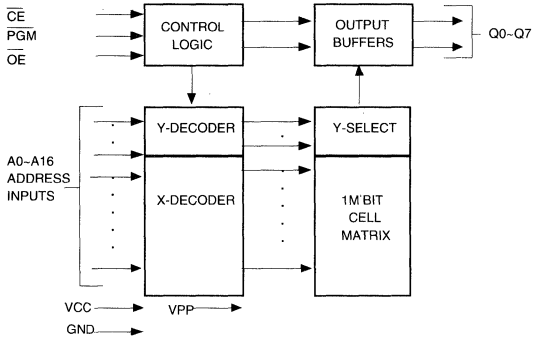
PLCC(MX27C1000)



CDIP(MX27C1001)



BLOCK DIAGRAM



PIN DESCRIPTION

SYMBOL	PIN NAME
A0~A16	Address Input
Q0~Q7	Data Input/Output
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
$\overline{PGM}$	Programmable Enable Input
VPP	Program Supply Voltage
NC	No Internal Connection
VCC	Power Supply Pin (+5V)
GND	Ground Pin

FUNCTIONAL DESCRIPTION

THE ERASURE OF THE MX27C1000/27C1001

The MX27C1000/27C1001 is erased by exposing the chip to an ultraviolet light source. A dosage of 15 W seconds/cm^2 is required to completely erase a MX27C1000/27C1001. This dosage can be obtained by exposure to an ultraviolet lamp — wavelength of 2537 Angstroms (Å) — with intensity of 12,000 μW/cm^2 for 15 to 20 minutes. The MX27C1000/27C1001 should be directly under and about one inch from the source and all filters should be removed from the UV light source prior to erasure.

It is important to note that the MX27C1000/27C1001, and similar devices, will be cleared for all bits of their programmed states with light sources having wavelengths shorter than 4000 Å. Although erasure times will be much longer than that with UV sources at 2537Å, nevertheless the exposure to fluorescent light and sunlight will eventually erase the MX27C1000/27C1001 and exposure to them should be prevented to realize maximum system reliability. If used in such an environment, the package window should be covered by an opaque label or substance.

THE PROGRAMMING OF THE MX27C1000/27C1001

When the MX27C1000 is delivered, or it is erased, the chip has all 1M bits in the "ONE", or HIGH state. "ZEROs" are loaded into the MX27C1000/27C1001 through the procedure of programming.

The programming mode is entered when 12.5 ± 0.5 V is applied to the VPP pin, OE is at VIH, and $\overline{CE}$ and $\overline{PGM}$ at VIL.

For programming, the data to be programmed is applied with 8 bits in parallel to the data pins.

The flowchart in Figure 1 shows MXIC's interactive algorithm. Interactive algorithm reduces programming time by using short programming pulses and giving each address only as many pulses as is necessary in order to reliably program the data. After each pulse is applied to a given address, the data in that address is verified. If the data is not verified, additional pulses are given until it is verified or the maximum is reached. This process is repeated while sequencing through each address of the MX27C100027C1001. This part of the algorithm is done at VCC = 6.0V to assure that each EPROM bit is programmed to a sufficiently high threshold voltage. After the interactive programming is completed, an overprogram pulse is given to each memory location; this ensures that all bits have sufficient margin. After the final address is completed, the entire EPROM memory is verified at VCC = 5V ± 10%.

FAST PROGRAMMING

The device is set up in the fast programming mode when the programming voltage VPP = 12.75V is applied, with VCC = 6.25 V and $\overline{PGM}$ = VIH (Algorithm is shown in Figure 2). The programming is achieved by applying a single TTL low level 100μs pulse to the $\overline{PGM}$ input after addresses and data line are stable. If the data is not verified, an additional pulse is applied for a maximum of 25 pulses. This process is repeated while sequencing through each address of the device. When the programming mode is completed, the data in all address is verified at VCC = VPP = 5V ± 10%.

PROGRAM INHIBIT MODE

Programming of multiple MX27C1000/27C1001s in parallel with different data is also easily accomplished by using the Program Inhibit Mode. Except for CE and OE, all like inputs of the parallel MX27C1000/27C1001 may be common. A TTL low-level program pulse applied to an MX27C1000/27C1001 CE input with VPP = 12.5 ± 0.5 V and PGM LOW will program that MX27C1000/27C1001. A high-level CE input inhibits the other MX27C1000/27C1001s from being programmed.

PROGRAM VERIFY MODE

Verification should be performed on the programmed bits to determine that they were correctly programmed. The verification should be performed with OE and CE, at VIL, PGM at VIH, and VPP at its programming voltage.

AUTO IDENTIFY MODE

The auto identify mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and device type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ± 5°C ambient temperature range that is required when programming the MX27C1000/27C1001.

To activate this mode, the programming equipment must force 12.0 ± 0.5 V on address line A9 of the device. Two identifier bytes may then be sequenced from the device outputs by toggling address line A0 from VIL to VIH. All other address lines must be held at VIL during auto identify mode.

Byte 0 (A0 = VIL) represents the manufacturer code, and byte 1 (A0 = VIH), the device identifier code. For the MX27C1000/1001, these two identifier bytes are given in the Mode Select Table. All identifiers for manufacturer and device codes will possess odd parity, with the MSB (DQ7) defined as the parity bit.

READ MODE

The MX27C1000/27C1001 has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable (CE) is the power control and should be used for device selection. Output Enable (OE) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (tACC) is equal to the delay from CE to output (tCE). Data is available at the outputs tQE after the falling edge of OE, assuming that CE has been LOW and addresses have been stable for at least tACC - tQE.

STANDBY MODE

The MX27C1000/27C1001 has a CMOS standby mode which reduces the maximum VCC current to 100 µA. It is placed in CMOS standby when CE is at VCC ± 0.3 V. The MX27C1000 also has a TTL-standby mode which reduces the maximum VCC current to 1.5 mA. It is placed in TTL-standby when CE is at VIH. When in standby mode, the outputs are in a high-impedance state, independent of the OE input.

TWO-LINE OUTPUT CONTROL FUNCTION

To accommodate multiple memory connections, a two-line control function is provided to allow for:

1. Low memory power dissipation,
2. Assurance that output bus contention will not occur.

It is recommended that CE be decoded and used as the primary device-selecting function, while OE be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low-power standby mode and that the output pins are only active when data is desired from a particular memory device.

SYSTEM CONSIDERATIONS

During the switch between active and standby conditions, transient current peaks are produced on the rising and falling edges of Chip Enable. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. At a minimum, a 0.1 µF ceramic capacitor (high frequency, low inherent inductance) should be used on each device between VCC and GND to minimize transient effects. In addition, to overcome the voltage drop caused by the inductive effects of the printed circuit board traces on EPROM arrays, a 4.7 µF bulk electrolytic capacitor should be used between VCC and GND for each eight devices. The location of the capacitor should be close to where the power supply is connected to the array.

MODE SELECT TABLE

	PINS						
MODE	**$\overline{CE}$**	**$\overline{OE}$**	**$\overline{PGM}$**	**A0**	**A9**	**VPP**	**OUTPUTS**
Read	VIL	VIL	X	X	X	VCC	DOUT
Output Disable	VIL	VIH	X	X	X	VCC	High Z
Standby (TTL)	VIH	X	X	X	X	VCC	High Z
Standby (CMOS)	VCC±0.3V	X	X	X	X	VCC	High Z
Program	VIL	VIH	VIL	X	X	VPP	DIN
Program Verify	VIL	VIL	VIH	X	X	VPP	DOUT
Program Inhibit	VIH	X	X	X	X	VPP	High Z
Manufacturer Code	VIL	VIL	X	VIL	VH	VCC	C2H
Device Code(27C1000)	VIL	VIL	X	VIH	VH	VCC	0EH
Device Code(27C1001)	VIL	VIL	X	VIH	VH	VCC	0FH

NOTES: 1. VH = 12.0 V ± 0.5 V
2. X = Either VIH or VIL(For auto select)
3. A1 - A8 = A10 - A16 = VIL(For auto select)
4. See DC Programming Characteristics for VPP voltage during programming.

FIGURE 1. INTERACTIVE PROGRAMMING FLOW CHART

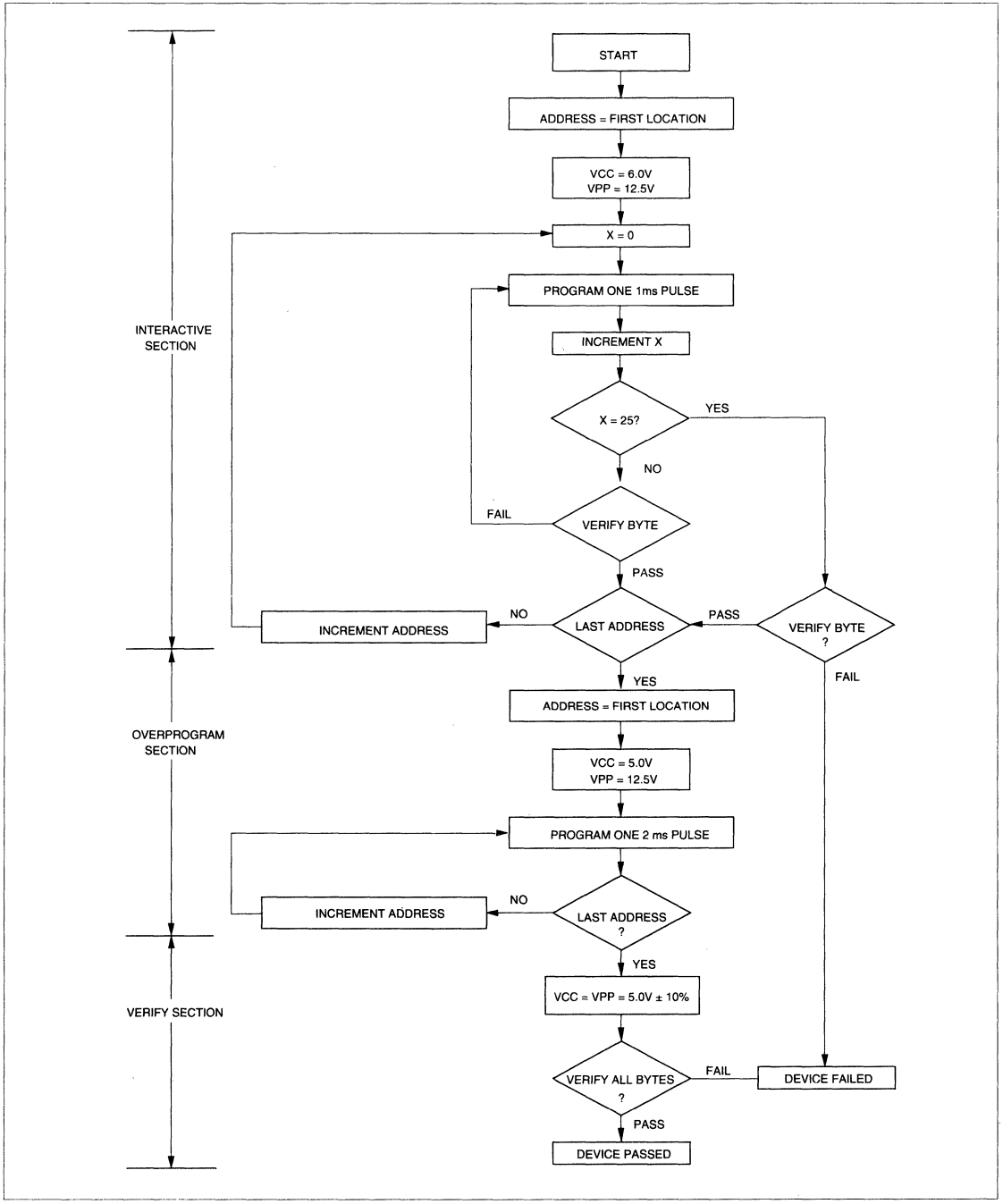
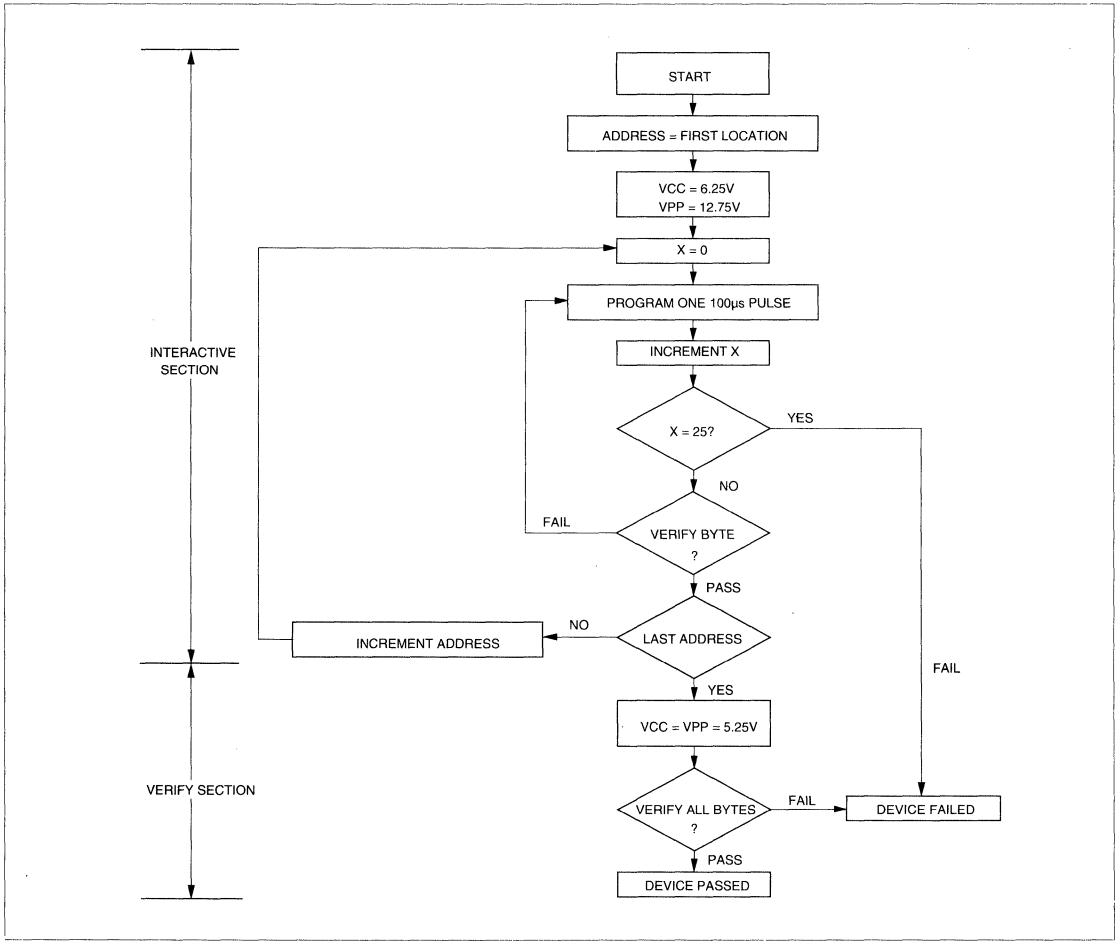
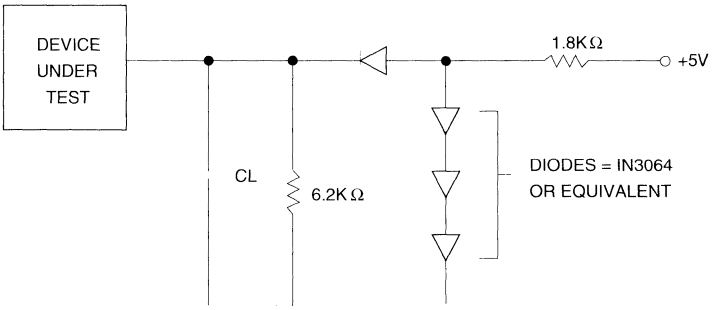


FIGURE 2. FAST PROGRAMMING FLOW CHART

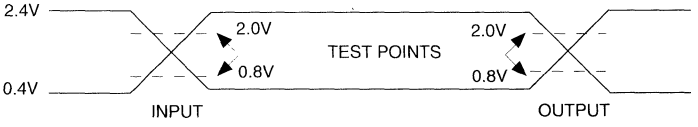


SWITCHING TEST CIRCUITS

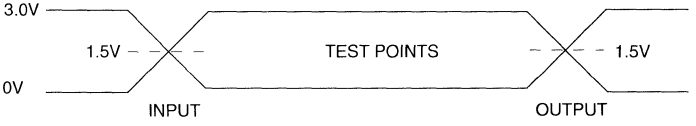


CL = 100 pF including jig capacitance(30pF for 55/70 ns parts)

SWITCHING TEST WAVEFORMS



AC TESTING: Inputs are driven at 2.4V for a logic "1" and 0.4V for a logic "0".
Input pulse rise and fall times are ≤10ns.



AC TESTING: (1) Inputs are driven at 3.0V for a logic "1" and 0V for a logic "0".
Input pulse rise and fall times are ≤10ns.
(2) For MX27C1000/1001-55, MX27C1000/1001-70 only

ABSOLUTE MAXIMUM RATINGS

RATING	VALUE
Ambient Operating Temperature	0°C to 70°C
Storage Temperature	-65°C to 125°C
Applied Input Voltage	-0.5V to 7.0V
Applied Output Voltage	-0.5V to VCC + 0.5V
VCC to Ground Potential	-0.5V to 7.0V
V9 & Vpp	-0.5V to 13.5V

NOTICE:
Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended period may affect reliability.

NOTICE:
Specifications contained within the following tables are subject to change.

DC CHARACTERISTICS TA = 0°C to 70°C, VCC = 5V ± 10%

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
VOH	Output High Voltage	2.4		V	IOH = -0.4mA
VOL	Output Low Voltage		0.4	V	IOL = 2.1mA
VIH	Input High Voltage	2.0	VCC + 0.5	V	
VIL	Input Low Voltage	-0.3	0.8	V	
ILI	Input Leakage Current	-10	10	μA	VIN = 0 to 5.5V
ILO	Output Leakage Current	-10	10	μA	VOUT = 0 to 5.5V
ICC3	VCC Power-Down Current		100	μA	$\overline{CE}$ = VCC ± 0.3V
ICC2	VCC Standby Current		1.5	mA	$\overline{CE}$ = VIH
ICC1	VCC Active Current		60	mA	$\overline{CE}$ = VIL, f=5MHz, Iout = 0mA
IPP	VPP Supply Current Read		100	μA	$\overline{CE}$ = $\overline{OE}$ = VIL, VPP = 5.5V

CAPACITANCE TA = 25°C, f = 1.0 MHz (Sampled only)

SYMBOL	PARAMETER	TYP.	MAX.	UNIT	CONDITIONS
CIN	Input Capacitance	8	12	pF	VIN = 0V
COUT	Output Capacitance	8	12	pF	VOUT = 0V
CVPP	VPP Capacitance	18	25	pF	VPP = 0V

AC CHARACTERISTICS TA = 0°C to 70°C, VCC = 5V± 10%

		27C10001001 -55		27C1000/1001 -70		27C1000/1001 -90			
SYMBOL	PARAMETER	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	UNIT	CONDITIONS
tACC	Address to Output Delay		55		70		90	ns	$\overline{CE}$ = $\overline{OE}$ = VIL
tCE	Chip Enable to Output Delay		55		70		90	ns	$\overline{OE}$ = VIL
tOE	Output Enable to Output Delay		30		35		40	ns	$\overline{CE}$ = VIL
tDF	$\overline{OE}$ High to Output Float, or $\overline{CE}$ High to Output Float	0	20	0	20	0	25	ns	
tOH	Output Hold from Address, $\overline{CE}$ or $\overline{OE}$ which ever occurred first	0		0		0		ns	

		27C10001001 -12		27C1000/1001 -15			
SYMBOL	PARAMETER	MIN.	MAX.	MIN.	MAX.	UNIT	CONDITIONS
tACC	Address to Output Delay		120		150	ns	$\overline{CE}$ = $\overline{OE}$ = VIL
tCE	Chip Enable to Output Delay		120		150	ns	$\overline{OE}$ = VIL
tOE	Output Enable to Output Delay		50		65	ns	$\overline{CE}$ = VIL
tDF	$\overline{OE}$ High to Output Float, or $\overline{CE}$ High to Output Float	0	35	0	50	ns	
tOH	Output Hold from Address, $\overline{CE}$ or $\overline{OE}$ which ever occurred first	0		0		ns	

DC PROGRAMMING CHARACTERISTICS TA = 25°C ± 5°C

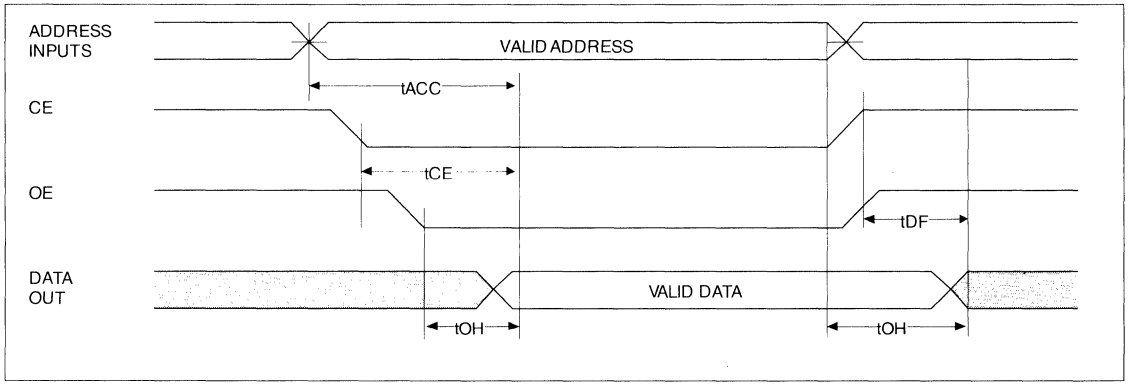
SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
VOH	Output High Voltage	2.4		V	IOH = -0.40mA
VOL	Output Low Voltage		0.4	V	IOL = 2.1mA
VIH	Input High Voltage	2.0	VCC + 0.5	V	
VIL	Input Low Voltage	-0.3	0.8	V	
ILI	Input Leakage Current	-10	10	µA	VIN = 0 to 5.5V
VH	A9 Auto Select Voltage	11.5	12.5	V	
ICC3	VCC Supply Current (Program & Verify)		50	mA	
IPP2	VPP Supply Current(Program)		30	mA	$\overline{CE}$ = $\overline{PGM}$ = VIL, $\overline{OE}$ = VIH
VCC1	Interactive Supply Voltage	5.75	6.25	V	
VPP1	Interactive Programming Voltage	12.0	13.0	V	
VCC2	Fast Programming Supply Voltage	6.00	6.50	V	
VPP2	Fast Programming Voltage	12.5	13.0	V	

AC PROGRAMMING CHARACTERISTICS TA = 25°C ± 5°C

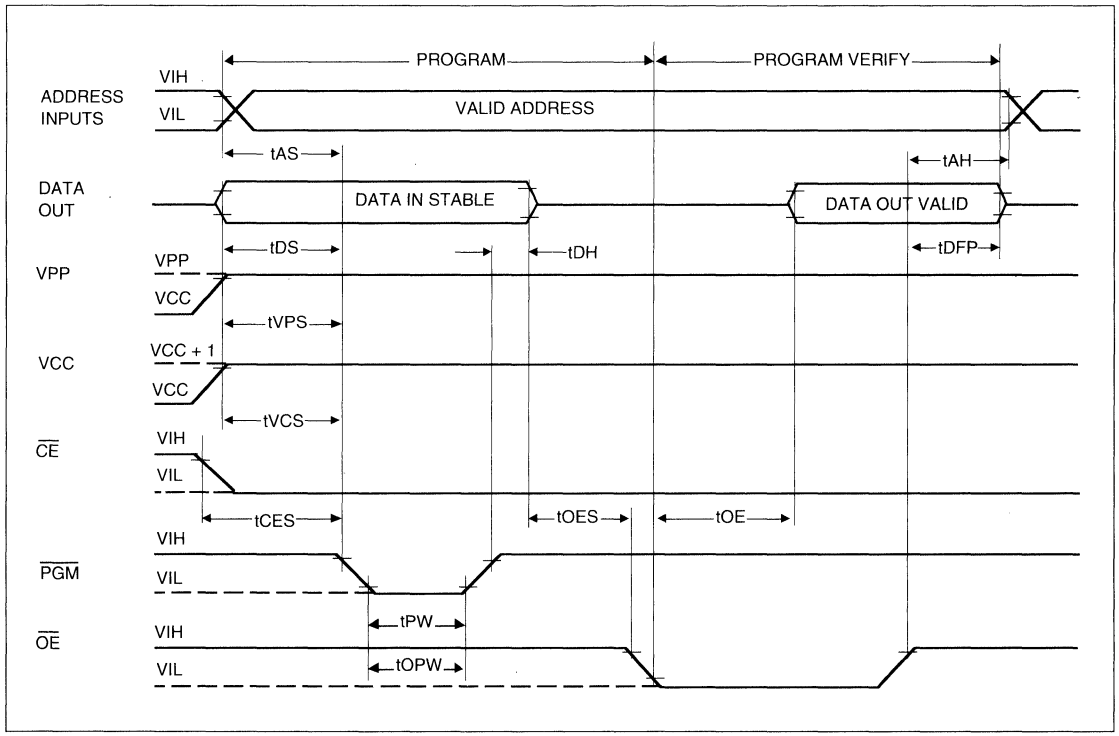
SYMBOL	PARAMETER		MIN.	MAX.	UNIT	CONDITIONS
tAS	Address Setup Time		2.0		mS	
tOES	$\overline{OE}$ Setup Time		2.0		mS	
tDS	Data Setup Time		2.0		mS	
tAH	Address Hold Time		0		mS	
tDH	Data Hold Time		2.0		mS	
tDFP	$\overline{CE}$ to Output Float Delay		0	130	nS	
tVPS	VPP Setup Time		2.0		mS	
tPW	$\overline{PGM}$ Program Pulse Width	*Fast*	95	105	mS	
		Interactive	0.95	1.05	mS	
tOPW	$\overline{PGM}$ Overprogram Pulse(Interactive)		1.95	2.05	mS	
tVCS	VCC Setup Time		2.0		mS	
tDV	Data Valid from $\overline{CE}$			250	nS	
tCES	$\overline{CE}$ Setup Time		2.0		mS	
tOE	Data valid from $\overline{OE}$			150	nS	

WAVEFORMS

READ CYCLE



INTERACTIVE PROGRAMMING ALGORITHM WAVEFORMS(NOTE1 & 2)



ORDERING INFORMATION

CERAMIC PACKAGE

PART NO.	ACCESS TIME(ns)	OPERATING CURRENT MAX.(mA)	STANDBY CURRENT MAX.(mA)	PACKAGE
MX27C1000DC-55	55	60	100	32 Pin DIP
MX27C1000DC-70	70	60	100	32 Pin DIP
MX27C1000DC-90	90	60	100	32 Pin DIP
MX27C1000DC-12	120	60	100	32 Pin DIP
MX27C1000DC-15	150	60	100	32 Pin DIP
MX27C1001DC-55	55	60	100	32 Pin DIP
MX27C1001DC-70	70	60	100	32 Pin DIP
MX27C1001DC-90	90	60	100	32 Pin DIP
MX27C1001DC-12	120	60	100	32 Pin DIP
MX27C1001DC-15	150	60	100	32 Pin DIP

PLASTIC PACKAGE

PART NO.	ACCESS TIME(ns)	OPERATING CURRENT MAX.(mA)	STANDBY CURRENT MAX.(mA)	PACKAGE
MX27C1000PC-55	55	60	100	32 Pin DIP
MX27C1000MC-55	55	60	100	32 Pin SOP
MX27C1000QC-55	55	60	100	32 Pin PLCC
MX27C1000PC-70	70	60	100	32 Pin DIP
MX27C1000MC-70	70	60	100	32 Pin SOP
MX27C1000QC-70	70	60	100	32 Pin PLCC
MX27C1000PC-90	90	60	100	32 Pin DIP
MX27C1000MC-90	90	60	100	32 Pin SOP
MX27C1000QC-90	90	60	100	32 Pin PLCC
MX27C1000PC-12	120	60	100	32 Pin DIP
MX27C1000MC-12	120	60	100	32 Pin SOP
MX27C1000QC-12	120	60	100	32 Pin PLCC
MX27C1000PC-15	150	60	100	32 Pin DIP
MX27C1000MC-15	150	60	100	32 Pin SOP
MX27C1000QC-15	150	60	100	32 Pin PLCC

MX27C1100/27C1024

1M-BIT(128K x 8/64K x 16) CMOS EPROM

FEATURES

- 64K x 16 organization(MX27C1024, JEDEC pin out)
- 128K x 8 or 64K x 16 organization(MX27C1100, ROM pin out compatible)
- +12.5V programming voltage
- Fast access time: 90/120/150 ns
- Totally static operation
- Completely TTL compatible
- Operating current: 60mA
- Standby current: 100μA
- Package type:
  - 40 pin ceramic DIP
  - 40 pin plastic DIP
  - 44 pin PLCC

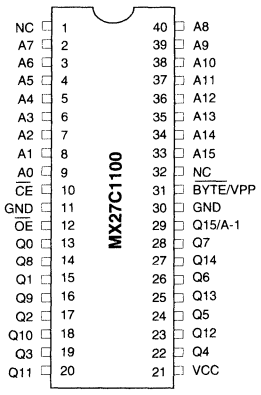
GENERAL DESCRIPTION

The MX27C1024 is a 5V only, 1M-bit, ultraviolet Erasable Programmable Read Only Memory. It is organized as 64K words by 16 bits per word(MX27C1024), 128K x 8 or 64K x 16(MX27C1100), operates from a single + 5 volt supply, has a static standby mode, and features fast single address location programming. All programming signals are TTL levels, requiring a single pulse. For programming outside from the system, existing EPROM programmers may be used. The MX27C1100/1024 supports a intelligent quick pulse programming algorithm which can result in programming times of less than thirty seconds.

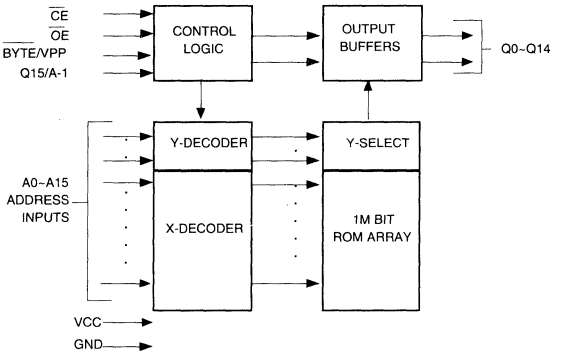
This EPROM is packaged in industry standard 40 pin dual-in-line ceramic packages or 40 pin plastic packages.

PIN CONFIGURATIONS

CDIP/PDIP(MX27C1100)

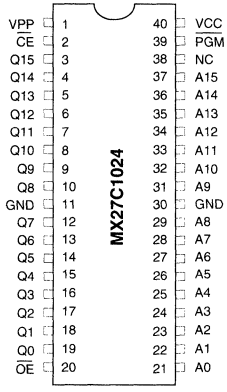


BLOCK DIAGRAM (MX27C1100)

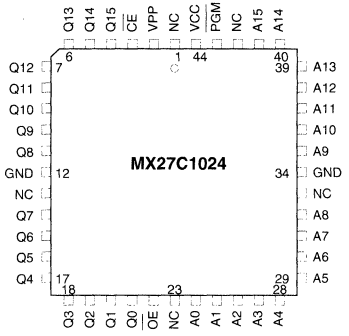


PIN CONFIGURATIONS

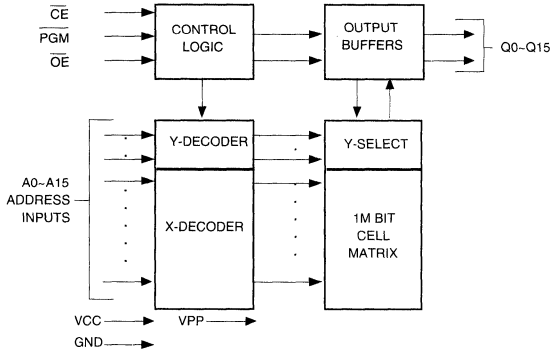
CDIP/PDIP(MX27C1024)



PLCC(MX27C1024)



BLOCK DIAGRAM (MX27C1024)



PIN DESCRIPTION(MX27C1100)

SYMBOL	PIN NAME
A0~A15	Address Input
Q0~Q14	Data Input/Output
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
$\overline{BYTE}$/VPP	Word/Byte Selection /Program Supply Voltage
Q15/A-1	Q15(Word mode)/LSB addr. (Byte mode)
VCC	Power Supply Pin (+5V)
GND	Ground Pin

PIN DESCRIPTION(MX27C1024)

SYMBOL	PIN NAME
A0~A15	Address Input
Q0~Q15	Data Input/Output
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
$\overline{PGM}$	Program Enable Input
VPP	Program Supply Voltage
VCC	Power Supply Pin (+5V)
GND	Ground Pin

TRUTH TABLE OF $\overline{BYTE}$ FUNCTION(MX27C1100)

BYTE MODE($\overline{BYTE}$ = GND)

$\overline{CE}$	OE/$\overline{OE}$	D15/A-1	MODE	D0-D7	SUPPLY CURRENT	NOTE
H	X	X	Non selected	High Z	Standby(ICC2)	1
L	L/H	X	Non selected	High Z	Operating(ICC1)	1
L	H/L	A-1 input	Selected	DOUT	Operating(ICC1)	1

WORD MODE($\overline{BYTE}$ = VCC)

$\overline{CE}$	OE/$\overline{OE}$	D15/A-1	MODE	D0-D14	SUPPLY CURRENT	NOTE
H	X	High Z	Non selected	High Z	Standby(ICC2)	1
L	L/H	High Z	Non selected	High Z	Operating(ICC1)	1
L	H/L	DOUT	Selected	DOUT	Operating(ICC1)	1

NOTE1: X = H or L

FUNCTIONAL DESCRIPTION

THE ERASURE OF THE MX27C1100/1024

The MX27C1100/1024 is erased by exposing the chip to an ultraviolet light source. A dosage of 15 W seconds/cm^2 is required to completely erase a MX27C1100/1024. This dosage can be obtained by exposure to an ultraviolet lamp — wavelength of 2537 Angstroms (Å) — with intensity of 12,000 $\mu W/cm^2$ for 15 to 20 minutes. The MX27C1100/1024 should be directly under and about one inch from the source and all filters should be removed from the UV light source prior to erasure.

It is important to note that the MX27C1100/1024, and similar devices, will be cleared for all bits of their programmed states with light sources having wavelengths shorter than 4000 Å. Although erasure times will be much longer than that with UV sources at 2537Å, nevertheless the exposure to fluorescent light and sunlight will eventually erase the MX27C1100/1024 and exposure to them should be prevented to realize maximum system reliability. If used in such an environment, the package window should be covered by an opaque label or substance.

THE PROGRAMMING OF THE MX27C1100/1024

When the MX27C1100/1024 is delivered, or it is erased, the chip has all 1M bits in the "ONE", or HIGH state. "ZEROs" are loaded into the MX27C1100/1024 through the procedure of programming.

The programming mode is entered when 12.5 ± 0.5V is applied to the VPP pin, $\overline{OE}$ is at VIH and $\overline{PGM}$ is at VIL (MX27C1024) and programming mode entered when 12.5 ± 5V is applied to the BYTE/VPP pin, $\overline{OE}$ at VIH and $\overline{CE}$ at VIL (MX27C1100).

For programming, the data to be programmed is applied with 16 bits in parallel to the data pins.

The flowchart in Figure 1 shows MXIC's interactive algorithm. Interactive algorithm reduces programming time by using short programming pulses and giving each address only as many pulses as is necessary in order to reliably program the data. After each pulse is applied to a given address, the data in that address is verified. If the data is not verified, additional pulses are given until it is verified or the maximum is reached. This process is repeated while sequencing through each address of the MX27C1100/1024. This part of the algorithm is done at VCC = 6.0V to assure that each EPROM bit is programmed to a sufficiently high threshold voltage. After the interactive programming is completed, an overprogram pulse is given to each memory location; this ensures that all bits have sufficient margin. After the final address is completed, the entire EPROM memory is verified at VCC = $5V \pm 10\%$.

FAST PROGRAMMING

The device is set up in the fast programming mode when the programming voltage VPP = 12.75V is applied, with VCC = 6.25 V and $\overline{PGM}$ = VIH (Algorithm is shown in Figure 2). The programming is achieved by applying a single TTL low level 100μs pulse to the $\overline{PGM}$ input after addresses and data line are stable. If the data is not verified, an additional pulse is applied for a maximum of 25 pulses. This process is repeated while sequencing through each address of the device. When the programming mode is completed, the data in all address is verified at VCC = VPP = $5V \pm 10\%$.

PROGRAM INHIBIT MODE

Programming of multiple MX27C1100/1024's in parallel with different data is also easily accomplished by using the Program Inhibit Mode. Except for $\overline{CE}$ and $\overline{OE}$, all like inputs of the parallel MX27C1100/1024 may be common. A TTL low-level program pulse applied to an MX27C1100/1024 $\overline{CE}$ input with VPP = 12.5 ± 0.5 V will program the MX27C1100/1024. A high-level $\overline{CE}$ input inhibits the other MX27C1100/1024s from being programmed.

PROGRAM VERIFY MODE

Verification should be performed on the programmed bits to determine that they were correctly programmed. The verification should be performed with $\overline{OE}$ and $\overline{CE}$, at VIL, and VPP at its programming voltage.

AUTO IDENTIFY MODE

The auto identify mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and device type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its

corresponding programming algorithm. This mode is functional in the 25°C ± 5°C ambient temperature range that is required when programming the MX27C1100/1024.

To activate this mode, the programming equipment must force 12.0 ± 0.5 V on address line A9 of the device. Two identifier bytes may then be sequenced from the device outputs by toggling address line A0 from VIL to VIH. All other address lines must be held at VIL during auto identify mode.

Byte 0 (A0 = VIL) represents the manufacturer code, and byte 1 (A0 = VIH), the device identifier code. For the MX27C1100/1024, these two identifier bytes are given in the Mode Select Table. All identifiers for manufacturer and device codes will possess odd parity, with the MSB (DQ15) defined as the parity bit.

READ MODE

The MX27C1100/1024 has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (tACC) is equal to the delay from $\overline{CE}$ to output (tCE). Data is available at the outputs tOE after the falling edge of $\overline{OE}$'s, assuming that $\overline{CE}$ has been LOW and addresses have been stable for at least tACC - t OE.

WORD-WIDE MODE

With $\overline{BYTE}$/VPP at VCC ± 0.2V outputs Q0-7 present data D0-7 and outputs Q8-15 present data D8-15, after $\overline{CE}$ and $\overline{OE}$ are appropriately enabled.

BYTE-WIDE MODE

With $\overline{BYTE}$/VPP at GND ± 0.2V, outputs Q8-15 are tri-stated. If Q15/A-1 = VIH, outputs Q0-7 present data bits D8-15. If Q15/A-1 = VIL, outputs Q0-7 present data bits D0-7.

STANDBY MODE

The MX27C1100/1024 has a CMOS standby mode which reduces the maximum VCC current to 100 μA. It is placed in CMOS standby when $\overline{CE}$ is at VCC ± 0.3 V. The MX27C1100/1024 also has a TTL-standby mode which reduces the maximum VCC current to 1.5 mA. It is placed in TTL-standby when $\overline{CE}$ is at VIH. When in standby mode, the outputs are in a high-impedance state, independent of the OE input.

TWO-LINE OUTPUT CONTROL FUNCTION

To accommodate multiple memory connections, a two-line control function is provided to allow for:

1. Low memory power dissipation,
2. Assurance that output bus contention will not occur.

It is recommended that $\overline{CE}$ be decoded and used as the primary device-selecting function, while $\overline{OE}$ be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low-power standby mode and that the output pins are only active when data is desired from a particular memory device.

SYSTEM CONSIDERATIONS

During the switch between active and standby conditions, transient current peaks are produced on the rising and falling edges of Chip Enable. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. At a minimum, a 0.1 μF ceramic capacitor (high frequency, low inherent inductance) should be used on each device between Vcc and GND to minimize transient effects. In addition, to overcome the voltage drop caused by the inductive effects of the printed circuit board traces on EPROM arrays, a 4.7 μF bulk electrolytic capacitor should be used between VCC and GND for each eight devices. The location of the capacitor should be close to where the power supply is connected to the array.

MODE SELECT TABLE (MX27C1024)

	PINS						
MODE	**$\overline{CE}$**	**$\overline{OE}$**	**$\overline{PGM}$**	**A0**	**A9**	**VPP**	**OUTPUTS**
Read	VIL	VIL	X	X	X	VCC	DOUT
Output Disable	VIL	VIH	X	X	X	VCC	High Z
Standby (TTL)	VIH	X	X	X	X	VCC	High Z
Standby (CMOS)	VCC±0.3V	X	X	X	X	VCC	High Z
Program	VIL	VIH	VIL	X	X	VPP	DIN
Program Verify	VIL	VIL	VIH	X	X	VPP	DOUT
Program Inhibit	VIH	X	X	X	X	VPP	High Z
Manufacturer Code	VIL	VIL	X	VIL	VH	VCC	00C2H
Device Code	VIL	VIL	X	VIH	VH	VCC	0111H

NOTES: 1. VH = 12.0 V ± 0.5 V
2. X = Either VIH or VIL(For auto select)
3. A1 - A8 = A10 - A16 = VIL(For auto select)
4. See DC Programming Characteristics for VPP voltage during programming.

MODE SELECT TABLE (MX27C1100)

MODE	**NOTES**	**$\overline{CE}$**	**$\overline{OE}$**	**A9**	**A0**	**Q15/A-1**	**$\overline{BYTE}$/ VPP(4)**	**Q8-14**	**Q0-7**
Read (Word)	1	VIL	VIL	X	X	D15 Out	VCC	D8-14 Out	D0-7 Out
Read (Upper Byte)		VIL	VIL	X	X	VIH	GND	High Z	D8-15 Out
Read (Lower Byte)		VIL	VIL	X	X	VIL	GND	High Z	D0-7 Out
Output Disable		VIL	VIH	X	X	High Z	X	High Z	High Z
Standby		VIH	X	X	X	High Z	X	High Z	High Z
Program	2	VIL	VIH	X	X	D15 In	VPP	D8-14 In	D0-7 In
Program Verify		VIH	VIL	X	X	D15 Out	VPP	D8-14 Out	D0-7 Out
Program Inhibit		VIH	VIH	X	X	High Z	VPP	High Z	High Z
Manufacturer Code	2,3	VIL	VIL	VH	VIL	0B	VCC	00H	C2H
Device Code		VIL	VIL	VH	VIH	0B	VCC	01H	12H

NOTES: 1. X can be VIL or VIH.
2. See DC Programming Characteristics for VPP voltages.
3. A1 - A8, A10 - A15 = VIL , A9 = VH = 12.0V ± 0.5V
4. $\overline{BYTE}$/VPP is intended for operation under DC Voltage conditions only.

FIGURE 1. INTERACTIVE PROGRAMMING FLOW CHART

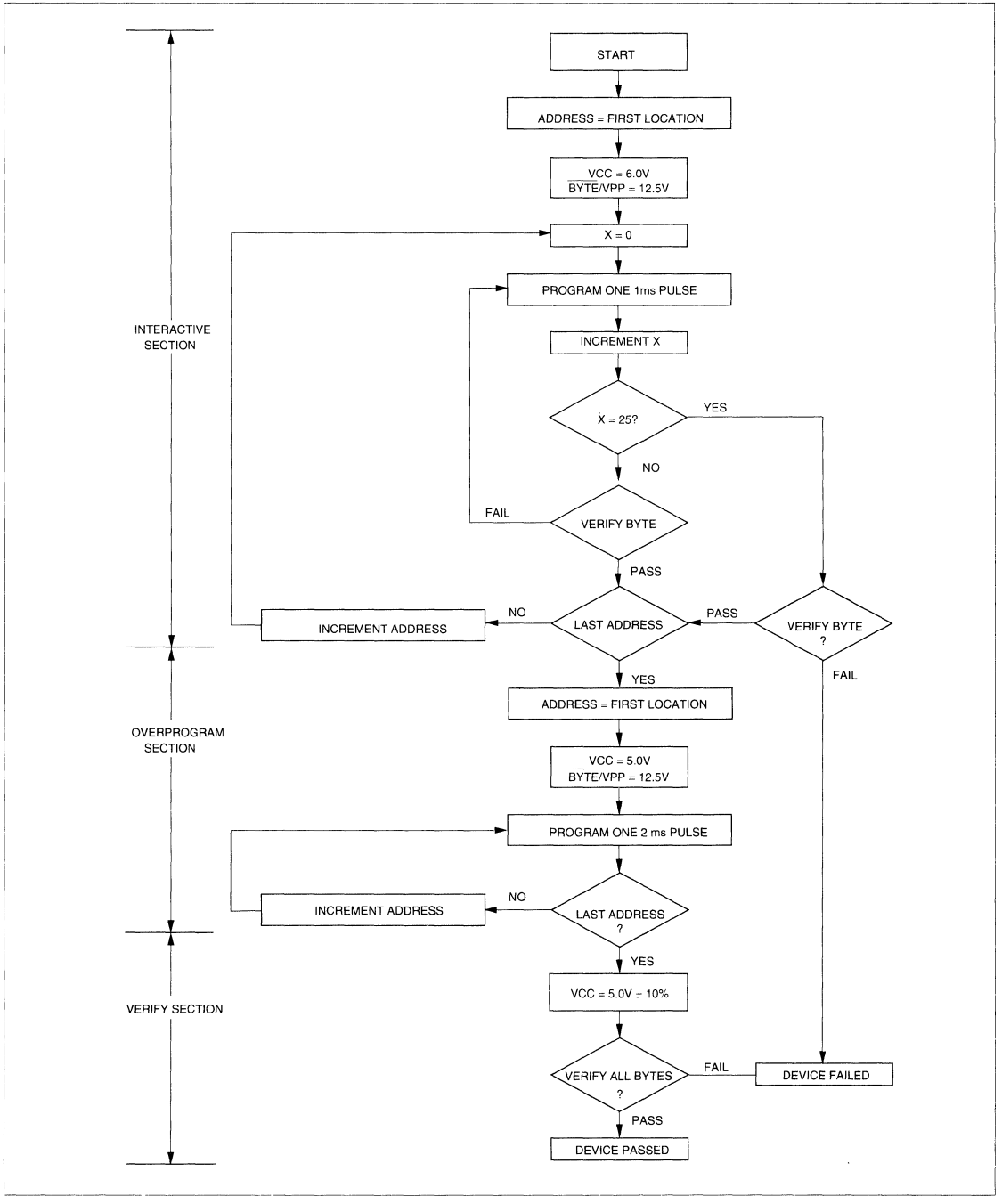
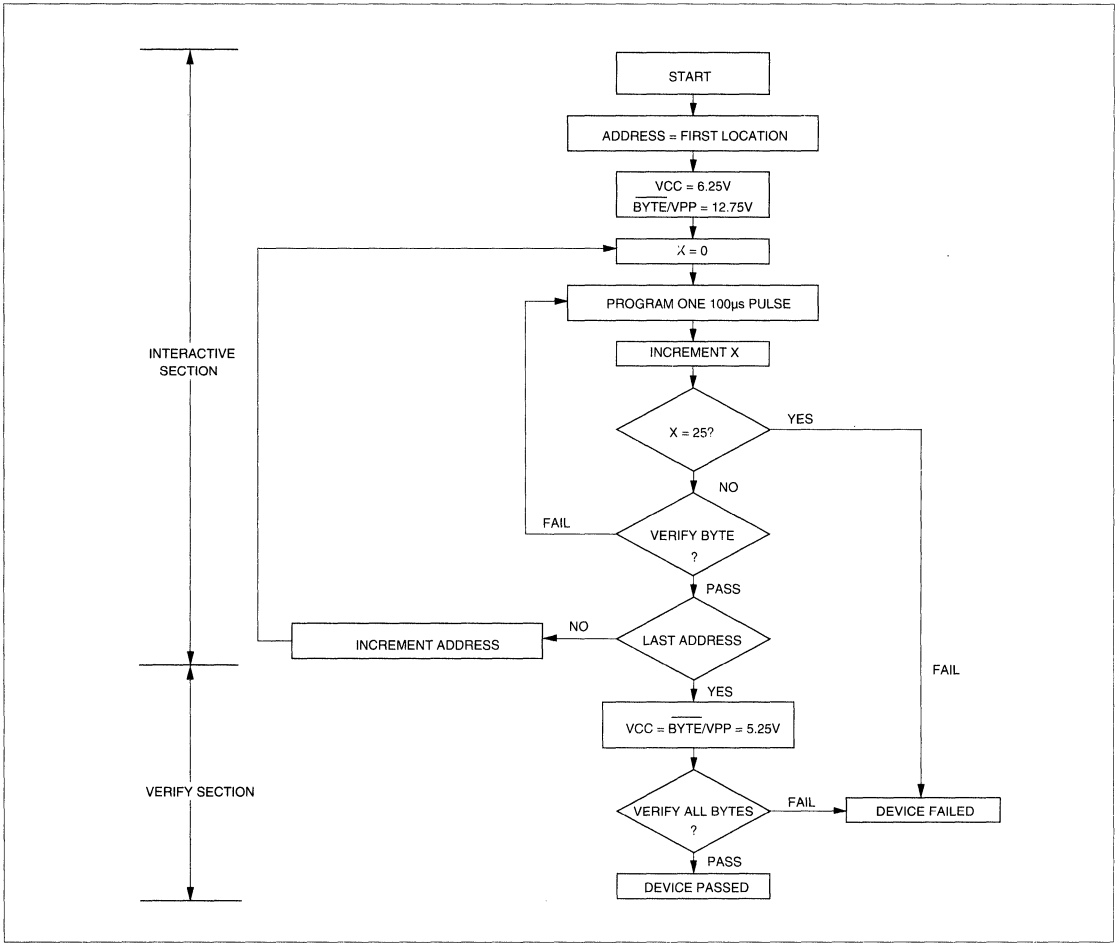
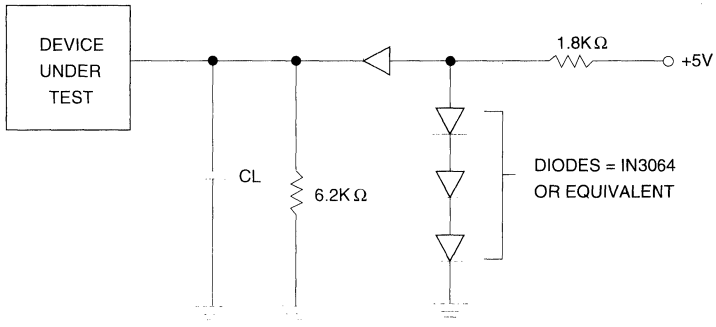


FIGURE 2. FAST PROGRAMMING FLOW CHART

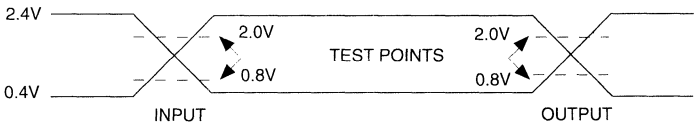


SWITCHING TEST CIRCUITS



CL = 100 pF Including jig capacitance

SWITCHING TEST WAVEFORMS



AC TESTING: Inputs are driven at 2.4V for a logic "1" and 0.4V for a logic "0".
Input pulse rise and fall times are <20ns.

ABSOLUTE MAXIMUM RATINGS

RATING	VALUE
Ambient Operating Temperature	0°C to 70°C
Storage Temperature	-65°C to 125°C
Applied Input Voltage	-0.5V to 7.0V
Applied Output Voltage	-0.5V to VCC + 0.5V
VCC to Ground Potential	-0.5V to 7.0V
A9 & Vpp	-0.5V to 13.5V

NOTICE:
Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended period may affect reliability.

NOTICE:
Specifications contained within the following tables are subject to change.

DC CHARACTERISTICS TA = 0°C to 70°C, VCC = 5V ± 10%

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
VOH	Output High Voltage	2.4		V	IOH = -0.4mA
VOL	Output Low Voltage		0.4	V	IOL = 2.1mA
VIH	Input High Voltage	2.0	VCC + 0.5	V	
VIL	Input Low Voltage	-0.3	0.8	V	
ILI	Input Leakage Current	-10	10	µA	VIN = 0 to 5.5V
ILO	Output Leakage Current	-10	10	µA	VOUT = 0 to 5.5V
ICC3	VCC Power-Down Current		100	µA	$\overline{CE}$ = VCC ± 0.3V
ICC2	VCC Standby Current		1.5	mA	$\overline{CE}$ = VIH
ICC1	VCC Active Current		60	mA	$\overline{CE}$ = VIL, f=5MHz, Iout = 0mA
IPP	VPP Supply Current Read		100	µA	$\overline{CE}$ = $\overline{OE}$ = VIL, VPP = 5.5V

CAPACITANCE TA = 25°C, f = 1.0 MHz (Sampled only)

SYMBOL	PARAMETER	TYP.	MAX.	UNIT	CONDITIONS
CIN	Input Capacitance	8	12	pF	VIN = 0V
COUT	Output Capacitance	8	12	pF	VOUT = 0V
CVPP	VPP Capacitance	18	25	pF	VPP = 0V

AC CHARACTERISTICS TA = 0°C to 70°C, VCC = 5V± 10%

		27C1100/1024-90		27C1100/1024-12		27C1100/1024-15			
SYMBOL	PARAMETER	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	UNIT	CONDITIONS
tACC	Address to Output Delay		90		120		150	ns	$\overline{CE}$ = $\overline{OE}$ = VIL
tCE	Chip Enable to Output Delay		90		120		150	ns	$\overline{OE}$ = VIL
tOE	Output Enable to Output Delay		40		50		65	ns	$\overline{CE}$ = VIL
tDF	$\overline{OE}$ High to Output Float, or $\overline{CE}$ High to Output Float	0	25	0	35	0	50	ns	
tOH	Output Hold from Address, $\overline{CE}$ or $\overline{OE}$ which ever occurred first	0		0		0		ns	

AC CHARACTERISTICS(Continued)

SYMBOL	PARAMETER	27C1100-90 MIN.	27C1100-90 MAX.	27C1100-12 MIN.	27C1100-12 MAX.	27C1100-15 MIN.	27C1100-15 MAX.	UNIT	CONDITIONS
tBHA	$\overline{BYTE}$ Access Time		90		120		150	ns	
tOHB	$\overline{BYTE}$ Output Hold Time	0		0		0		ns	
tBHZ	$\overline{BYTE}$ Output Delay Time		70		70		70	ns	
tBLZ	$\overline{BYTE}$ Output Set Time	10		10		10		ns	

DC PROGRAMMING CHARACTERISTICS TA = 25°C ± 5°C

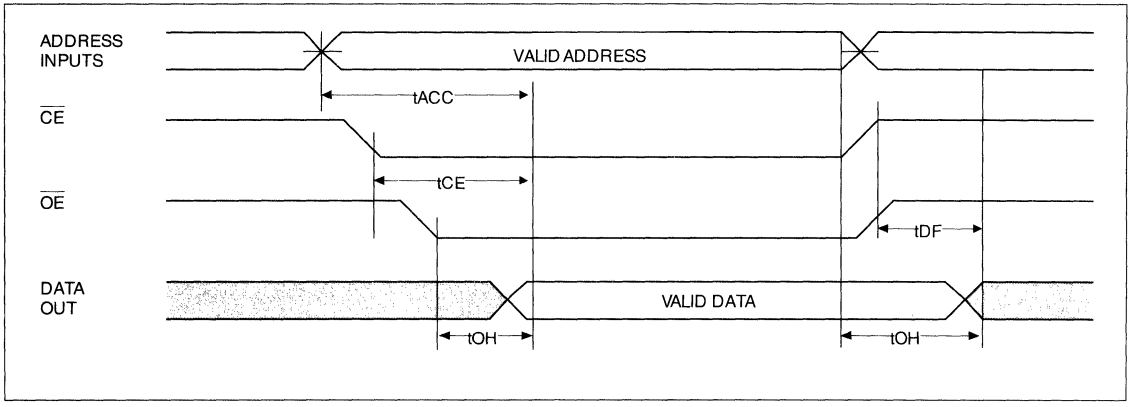
SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
VOH	Output High Voltage	2.4		V	IOH = -0.40mA
VOL	Output Low Voltage		0.4	V	IOL = 2.1mA
VIH	Input High Voltage	2.0	VCC + 0.5	V	
VIL	Input Low Voltage	-0.3	0.8	V	
ILI	Input Leakage Current	-10	10	µA	VIN = 0 to 5.5V
VH	A9 Auto Select Voltage	11.5	12.5	V	
ICC3	VCC Supply Current (Program & Verify)		50	mA	
IPP2	VPP Supply Current(Program)		30	mA	$\overline{CE}$ = VIL, $\overline{OE}$ = VIH
VCC1	Interactive Supply Voltage	5.75	6.25	V	
VPP1	Interactive Programming Voltage	12.0	13.0	V	
VCC2	Fast Programming Supply Voltage	6.00	6.50	V	
VPP2	Fast Programming Voltage	12.5	13.0	V	

AC PROGRAMMING CHARACTERISTICS TA = 25°C ± 5°C

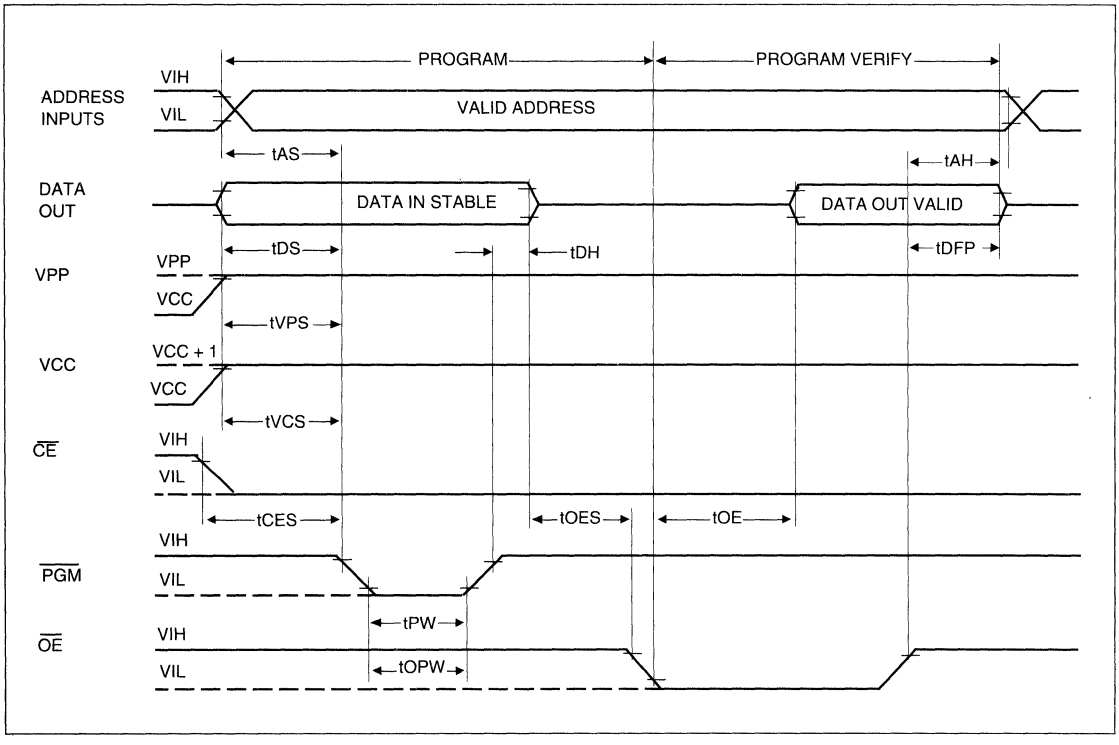
SYMBOL	PARAMETER		MIN.	MAX.	UNIT	CONDITIONS
tAS	Address Setup Time		2.0		µS	
tOES	$\overline{OE}$ Setup Time		2.0		µS	
tDS	Data Setup Time		2.0		µS	
tAH	Address Hold Time		0		µS	
tDH	Data Hold Time		2.0		µS	
tDFP	$\overline{CE}$ to Output Float Delay		0	130	nS	
tVPS	VPP Setup Time		2.0		µS	
tPW	$\overline{CE}$ Program Pulse Width	*Fast*	95	105	µS	
		Interactive	0.95	1.05	mS	
tOPW	$\overline{CE}$ Overprogram Pulse(Interactive)		1.95	2.05	mS	
tVCS	VCC Setup Time		2.0		µS	
tDV	Data Valid from $\overline{CE}$			250	nS	
tCES	$\overline{CE}$ Setup Time		2.0		µS	
tOE	Data valid from $\overline{OE}$			150	nS	

WAVEFORMS(MX27C1024)

READ CYCLE

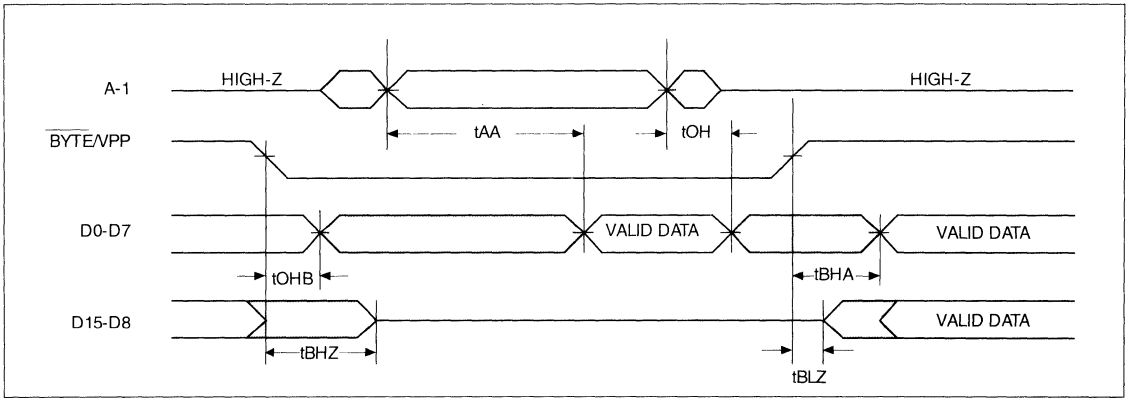


INTERACTIVE PROGRAMMING ALGORITHM WAVEFORMS

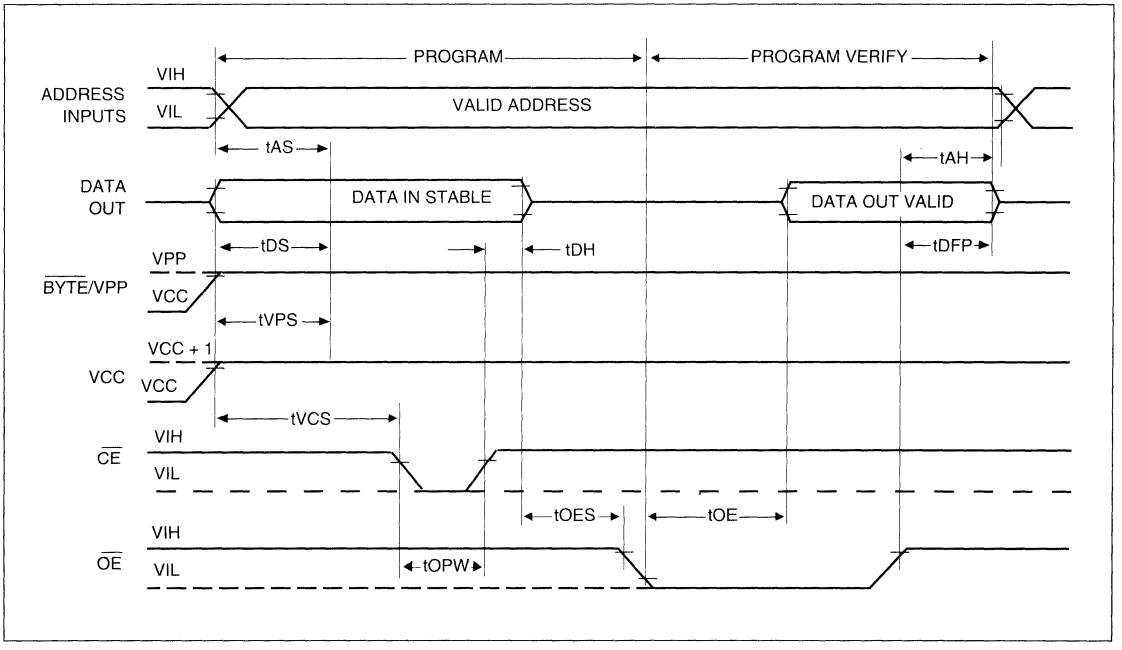


WAVEFORMS(MX27C1100)

PROPAGATION DELAY FROM CHIP ENABLE(ADDRESS VALID)



INTERACTIVE PROGRAMMING ALGORITHM WAVEFORMS



ORDERING INFORMATION

CERAMIC PACKAGE

PART NO.	ACCESS TIME (ns)	OPERATING CURRENT MAX.(mA)	STANDBY CURRENT MAX.(mA)	PACKAGE
MX27C1100DC-90	90	60	100	40 Pin DIP(ROM pin out)
MX27C1100DC-12	120	60	100	40 Pin DIP(ROM pin out)
MX27C1100DC-15	150	60	100	40 Pin DIP(ROM pin out)
MX27C1024DC-90	90	60	100	40 Pin DIP(JEDEC pin out)
MX27C1024DC-12	120	60	100	40 Pin DIP(JEDEC pin out)
MX27C1024DC-15	150	60	100	40 Pin DIP(JEDEC pin out)

PLASTIC PACKAGE

PART NO.	ACCESS TIME (ns)	OPERATING CURRENT MAX.(mA)	STANDBY CURRENT MAX.(mA)	PACKAGE
MX27C1100PC-90	90	60	100	40 Pin DIP(ROM pin out)
MX27C1100PC-12	120	60	100	40 Pin DIP(ROM pin out)
MX27C1100PC-15	150	60	100	40 Pin DIP(ROM pin out)
MX27C1024PC-90	90	60	100	40 Pin DIP(JEDEC pin out)
MX27C1024PC-12	120	60	100	40 Pin DIP(JEDEC pin out)
MX27C1024PC-15	150	60	100	40 Pin DIP(JEDEC pin out)
MX27C1024QC-90	90	60	100	44 Pin PLCC
MX27C1024QC-12	120	60	100	44 Pin PLCC
MX27C1024QC-15	150	60	100	44 Pin PLCC

MX27C2000

2M-BIT(256K x 8) CMOS EPROM

FEATURES

- 256Kx 8 organization
- Single +5V power supply
- +12.5V programming voltage
- Fast access time: 90/120/150 ns
- Totally static operation
- Completely TTL compatible
- Operating current: 60mA
- Standby current: 100μA
- Package type:
  - 32 pin ceramic DIP, plastic DIP
  - 32 pin SOP

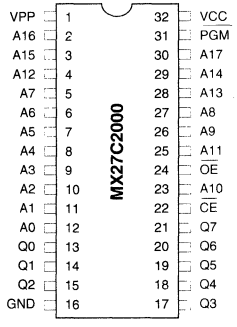
GENERAL DESCRIPTION

The MX27C2000 is a 5V only, 2M-bit, ultraviolet Erasable Programmable Read Only Memory. It is organized as 256K words by 8 bits per word, operates from a single + 5 volt supply, has a static standby mode, and features fast single address location programming. All programming signals are TTL levels, requiring a single pulse. For programming outside from the system, existing EPROM programmers may be used. The MX27C2000 supports a intelligent quick pulse programming algorithm which can result in programming times of less than one minute.

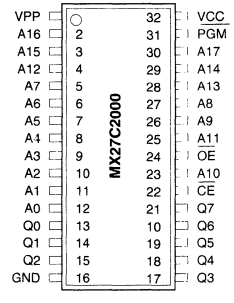
This EPROM is packaged in industry standard 32 pin dual-in-line packages or 32 lead, SOP packages.

PIN CONFIGURATIONS

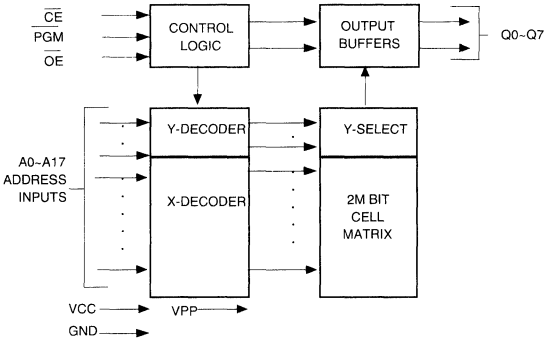
32 CDIP/PDIP



32 SOP



BLOCK DIAGRAM



PIN DESCRIPTION

SYMBOL	PIN NAME
A0~A17	Address Input
Q0~Q7	Data Input/Output
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
$\overline{PGM}$	Programmable Enable Input
VPP	Program Supply Voitage
NC	No Internal Connection
VCC	Power Supply Pin (+5V)
GND	Ground Pin

FUNCTIONAL DESCRIPTION

THE ERASURE OF THE MX27C2000

The MX27C2000 is erased by exposing the chip to an ultraviolet light source. A dosage of 15 W seconds/cm^2 is required to completely erase a MX27C2000. This dosage can be obtained by exposure to an ultraviolet lamp — wavelength of 2537 Angstroms (Å) — with intensity of 12,000 μW/cm^2 for 15 to 20 minutes. The MX27C2000 should be directly under and about one inch from the source and all filters should be removed from the UV light source prior to erasure.

It is important to note that the MX27C2000, and similar devices, will be cleared for all bits of their programmed states with light sources having wavelengths shorter than 4000 Å. Although erasure times will be much longer than that with UV sources at 2537Å, nevertheless the exposure to fluorescent light and sunlight will eventually erase the MX27C2000 and exposure to them should be prevented to realize maximum system reliability. If used in such an environment, the package window should be covered by an opaque label or substance.

THE PROGRAMMING OF THE MX27C2000

When the MX27C2000 is delivered, or it is erased, the chip has all 2M bits in the "ONE", or HIGH state. "ZEROs" are loaded into the MX27C2000 through the procedure of programming.

The programming mode is entered when 12.5 ± 0.5 V is applied to the VPP pin, $\overline{OE}$ is at VIH, and $\overline{CE}$ and $\overline{PGM}$ are at VIL.

For programming, the data to be programmed is applied with 8 bits in parallel to the data pins.

The flowchart in Figure 1 shows MXIC's interactive algorithm. Interactive algorithm reduces programming time by using short programming pulses and giving each address only as many pulses as is necessary in order to reliably program the data. After each pulse is applied to a given address, the data in that address is verified. If the data is not verified, additional pulses are given until it is verified or the maximum is reached. This process is repeated while sequencing through each address of the MX27C2000. This part of the algorithm is done at VCC= 6.0V to assure that each EPROM bit is programmed to a sufficiently high threshold voltage. After the interactive programming is completed, an overprogram pulse is given to each memory location; this ensures that all bits have sufficient margin. After the final address is completed, the entire EPROM memory is verified at VCC = 5V ± 10%.

FAST PROGRAMMING

The device is set up in the fast programming mode when the programming voltage VPP = 12.75V is applied, with VCC = 6.25 V and $\overline{PGM}$ = VIH (Algorithm is shown in Figure 2). The programming is achieved by applying a single TTL low level 100μs pulse to the $\overline{PGM}$ input after addresses and data line are stable. If the data is not verified, an additional pulse is applied for a maximum of 25 pulses. This process is repeated while sequencing through each address of the device. When the programming mode is completed, the data in all address is verified at VCC = VPP = 5V ± 10%.

PROGRAM INHIBIT MODE

Programming of multiple MX27C2000s in parallel with different data is also easily accomplished by using the Program Inhibit Mode. Except for $\overline{CE}$ and $\overline{OE}$, all like inputs of the parallel MX27C2000 may be common. A TTL low-level program pulse applied to an MX27C2000 $\overline{CE}$ input with VPP = 12.5 ± 0.5 V and $\overline{PGM}$ LOW will program that MX27C2000. A high-level $\overline{CE}$ input inhibits the other MX27C2000s from being programmed.

PROGRAM VERIFY MODE

Verification should be performed on the programmed bits to determine that they were correctly programmed. The verification should be performed with $\overline{OE}$ and $\overline{CE}$, at VIL, PGM at VIH, and VPP at its programming voltage.

AUTO IDENTIFY MODE

The auto identify mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and device type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ± 5°C ambient temperature range that is required when programming the MX27C2000.

To activate this mode, the programming equipment must force 12.0 ± 0.5 V on address line A9 of the device. Two identifier bytes may then be sequenced from the device outputs by toggling address line A0 from VIL to VIH. All other address lines must be held at VIL during auto identify mode.

Byte 0 (A0 = VIL) represents the manufacturer code, and byte 1 (A0 = VIH), the device identifier code. For the MX27C2000, these two identifier bytes are given in the Mode Select Table. All identifiers for manufacturer and device codes will possess odd parity, with the MSB (DQ7) defined as the parity bit.

READ MODE

The MX27C2000 has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (tACC) is equal to the delay from $\overline{CE}$ to output (tCE). Data is available at the outputs tQE after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been LOW and addresses have been stable for at least tACC - tQE.

STANDBY MODE

The MX27C2000 has a CMOS standby mode which reduces the maximum VCC current to 100 μA. It is placed in CMOS standby when $\overline{CE}$ is at VCC ± 0.3 V. The MX27C2000 also has a TTL-standby mode which reduces the maximum VCC current to 1.5 mA. It is placed in TTL-standby when $\overline{CE}$ is at VIH. When in standby mode, the outputs are in a high-impedance state, independent of the $\overline{OE}$ input.

TWO-LINE OUTPUT CONTROL FUNCTION

To accommodate multiple memory connections, a two-line control function is provided to allow for:

1. Low memory power dissipation,
2. Assurance that output bus contention will not occur.

It is recommended that $\overline{CE}$ be decoded and used as the primary device-selecting function, while $\overline{OE}$ be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low-power standby mode and that the output pins are only active when data is desired from a particular memory device.

SYSTEM CONSIDERATIONS

During the switch between active and standby conditions, transient current peaks are produced on the rising and falling edges of Chip Enable. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. At a minimum, a 0.1 μF ceramic capacitor (high frequency, low inherent inductance) should be used on each device between Vcc and GND to minimize transient effects. In addition, to overcome the voltage drop caused by the inductive effects of the printed circuit board traces on EPROM arrays, a 4.7 μF bulk electrolytic capacitor should be used between VCC and GND for each eight devices. The location of the capacitor should be close to where the power supply is connected to the array.

MODE SELECT TABLE

	PINS						
MODE	**$\overline{CE}$**	**$\overline{OE}$**	**$\overline{PGM}$**	**A0**	**A9**	**VPP**	**OUTPUTS**
Read	VIL	VIL	X	X	X	VCC	DOUT
Output Disable	VIL	VIH	X	X	X	VCC	High Z
Standby (TTL)	VIH	X	X	X	X	VCC	High Z
Standby (CMOS)	VCC±0.3V	X	X	X	X	VCC	High Z
Program	VIL	VIH	VIL	X	X	VPP	DIN
Program Verify	VIL	VIL	VIH	X	X	VPP	DOUT
Program Inhibit	VIH	X	X	X	X	VPP	High Z
Manufacturer Code	VIL	VIL	X	VIL	VH	VCC	C2H
Device Code	VIL	VIL	X	VIH	VH	VCC	20H

NOTES: 1. VH = 12.0 V ± 0.5 V
2. X = Either VIH or VIL(For auto select)
3. A1 - A8 = A10 - A16 = VIL(For auto select)
4. See DC Programming Characteristics for VPP voltage during programming.

FIGURE 1. INTERACTIVE PROGRAMMING FLOW CHART

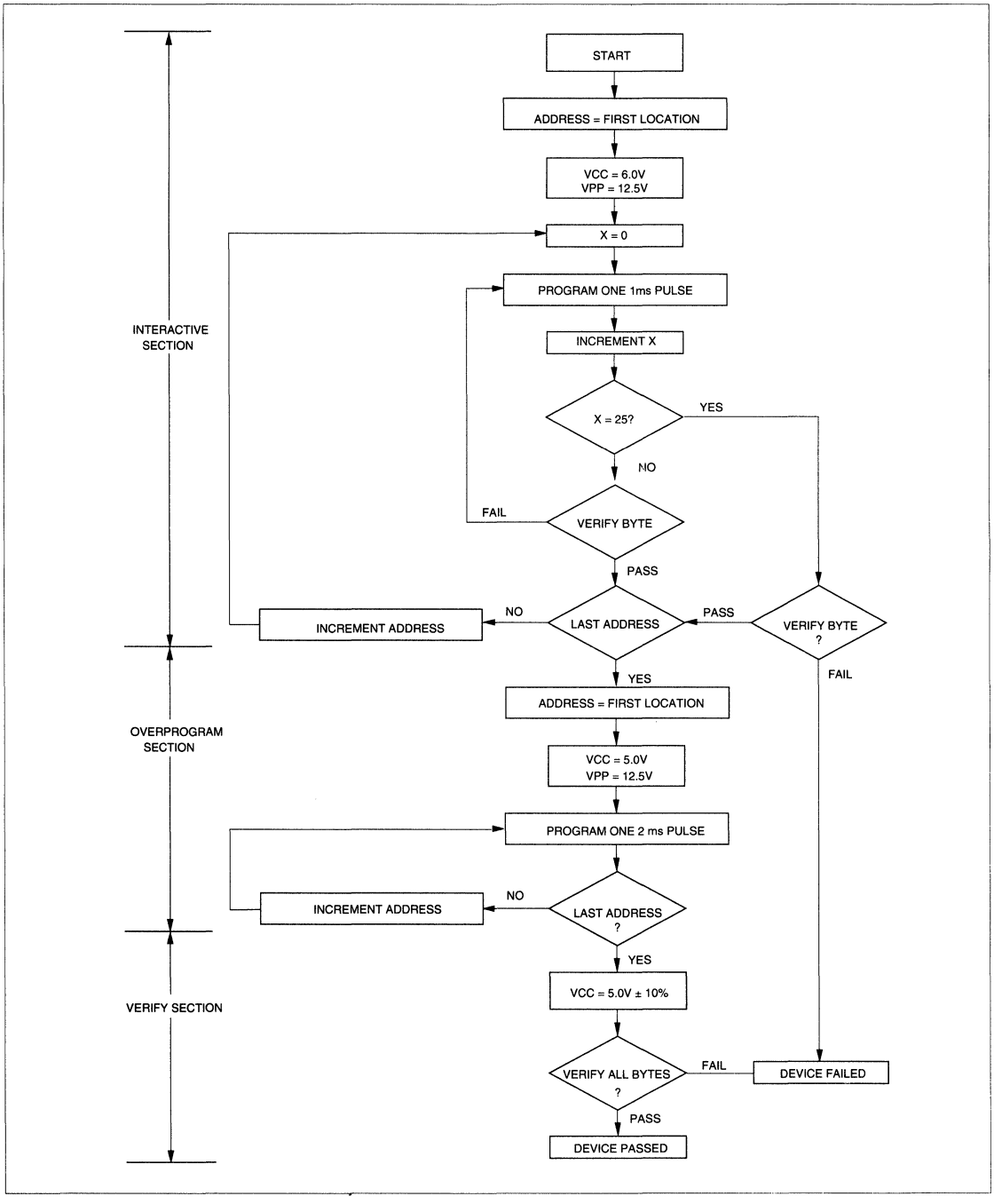
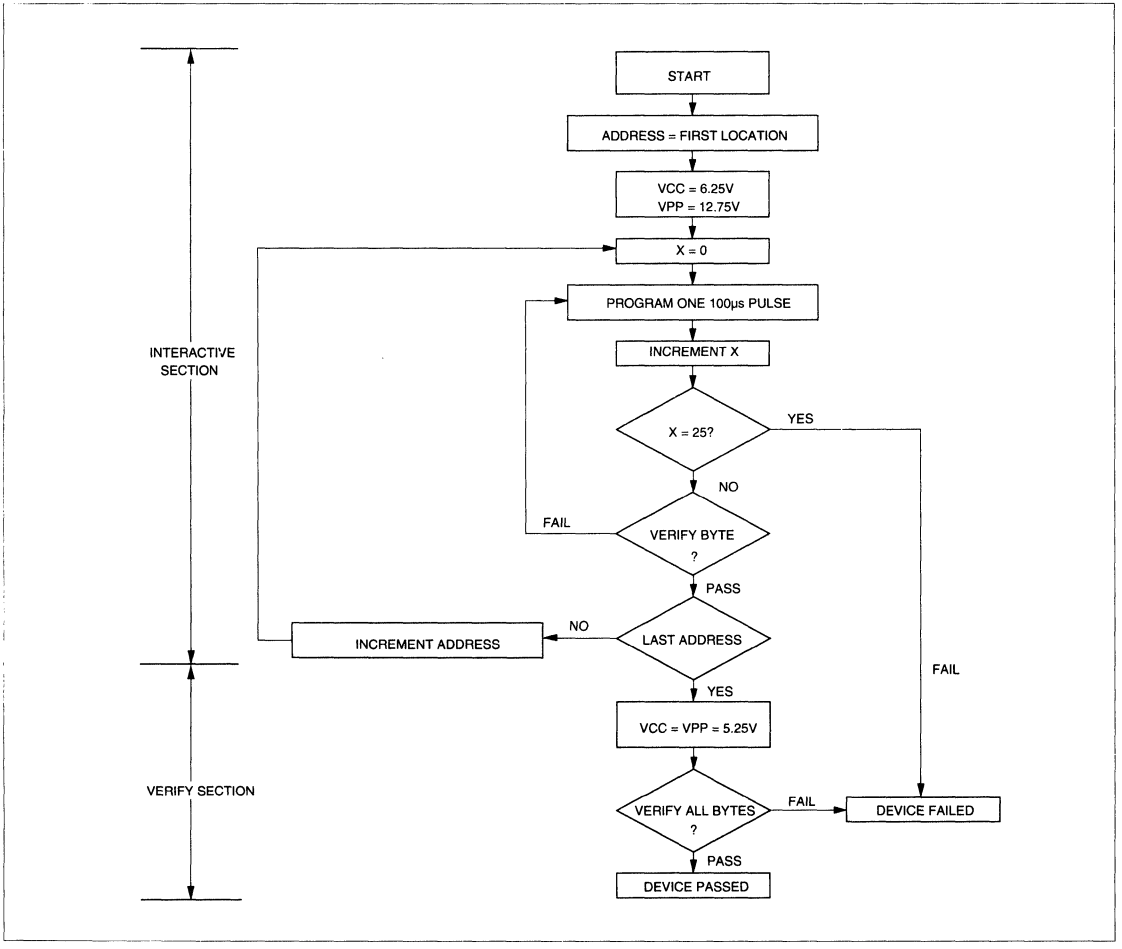
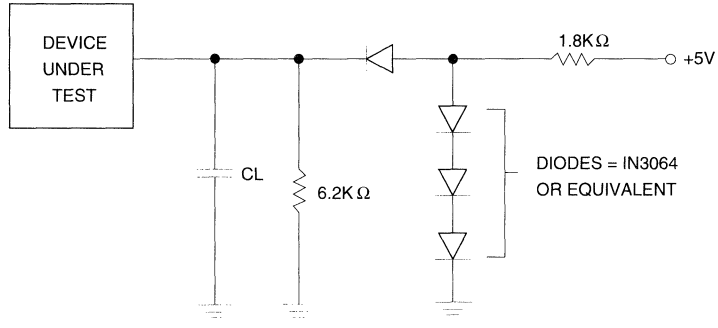


FIGURE 2. FAST PROGRAMMING FLOW CHART

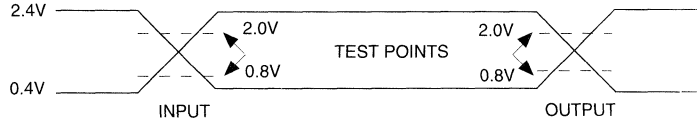


SWITCHING TEST CIRCUITS



CL = 100 pF Including jig capacitance

SWITCHING TEST WAVEFORMS



AC TESTING: Inputs are driven at 2.4V for a logic "1" and 0.4V for a logic "0".
Input pulse rise and fall times are ≤ 10ns.

ABSOLUTE MAXIMUM RATINGS

RATING	VALUE
Ambient Operating Temperature	0°C to 70°C
Storage Temperature	-65°C to 125°C
Applied Input Voltage	-0.5V to 7.0V
Applied Output Voltage	-0.5V to VCC + 0.5V
VCC to Ground Potential	-0.5V to 7.0V
V9 & VPP	-0.5V to 13.5V

NOTICE:
Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended period may affect reliability.

NOTICE:
Specifications contained within the following tables are subject to change.

DC CHARACTERISTICS TA = 0°C to 70°C, VCC = 5V ± 10%

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
VOH	Output High Voltage	2.4		V	IOH = -0.4mA
VOL	Output Low Voltage		0.4	V	IOL = 2.1mA
VIH	Input High Voltage	2.0	VCC + 0.5	V	
VIL	Input Low Voltage	-0.3	0.8	V	
ILI	Input Leakage Current	-10	10	µA	VIN = 0 to 5.5V
ILO	Output Leakage Current	-10	10	µA	VOUT = 0 to 5.5V
ICC3	VCC Power-Down Current		100	µA	$\overline{CE}$ = VCC ± 0.3V
ICC2	VCC Standby Current		1.5	mA	$\overline{CE}$ = VIH
ICC1	VCC Active Current		60	mA	$\overline{CE}$ = VIL, f=5MHz, Iout = 0mA
IPP	VPP Supply Current Read		100	µA	$\overline{CE}$ = $\overline{OE}$ = VIL, VPP = 5.5V

CAPACITANCE TA = 25°C, f = 1.0 MHz (Sampled only)

SYMBOL	PARAMETER	TYP.	MAX.	UNIT	CONDITIONS
CIN	Input Capacitance	8	12	pF	VIN = 0V
COUT	Output Capacitance	8	12	pF	VOUT = 0V
CVPP	VPP Capacitance	18	25	pF	VPP = 0V

AC CHARACTERISTICS TA = 0°C to 70°C, VCC = 5V± 10%

		27C2000-90		27C2000-12		27C2000-15			
SYMBOL	PARAMETER	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	UNIT	CONDITIONS
tACC	Address to Output Delay		90		120		150	ns	$\overline{CE}$ = $\overline{OE}$ = VIL
tCE	Chip Enable to Output Delay		90		120		150	ns	$\overline{OE}$ = VIL
tOE	Output Enable to Output Delay		40		50		65	ns	$\overline{CE}$ = VIL
tDF	$\overline{OE}$ High to Output Float, or $\overline{CE}$ High to Output Float	0	25	0	35	0	50	ns	
tOH	Output Hold from Address, $\overline{CE}$ or $\overline{OE}$ which ever occurred first	0		0		0		ns	

DC PROGRAMMING CHARACTERISTICS TA = 25°C ± 5°C

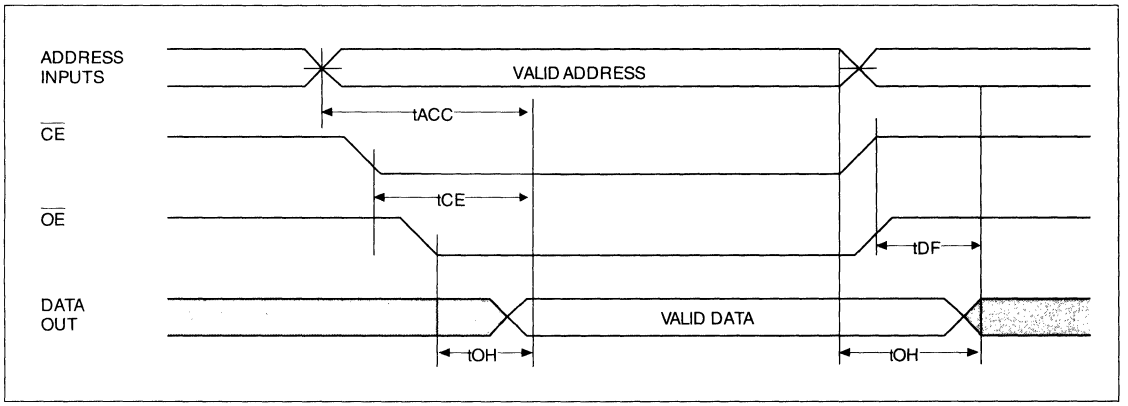
SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
VOH	Output High Voltage	2.4		V	IOH = -0.40mA
VOL	Output Low Voltage		0.4	V	IOL = 2.1mA
VIH	Input High Voltage	2.0	VCC + 0.5	V	
VIL	Input Low Voltage	-0.3	0.8	V	
ILI	Input Leakage Current	-10	10	μA	VIN = 0 to 5.5V
VH	A9 Auto Select Voltage	11.5	12.5	V	
ICC3	VCC Supply Current (Program & Verify)		50	mA	
IPP2	VPP Supply Current(Program)		30	mA	$\overline{CE}$=$\overline{PGM}$ =VIL,$\overline{OE}$=VIH
VCC1	Interactive Supply Voltage	5.75	6.25	V	
VPP1	Interactive Programming Voltage	12.0	13.0	V	
VCC2	Fast Programming Supply Voltage	6.00	6.50	V	
VPP2	Fast Programming Voltage	12.5	13.0	V	

AC PROGRAMMING CHARACTERISTICS TA = 25°C ± 5°C

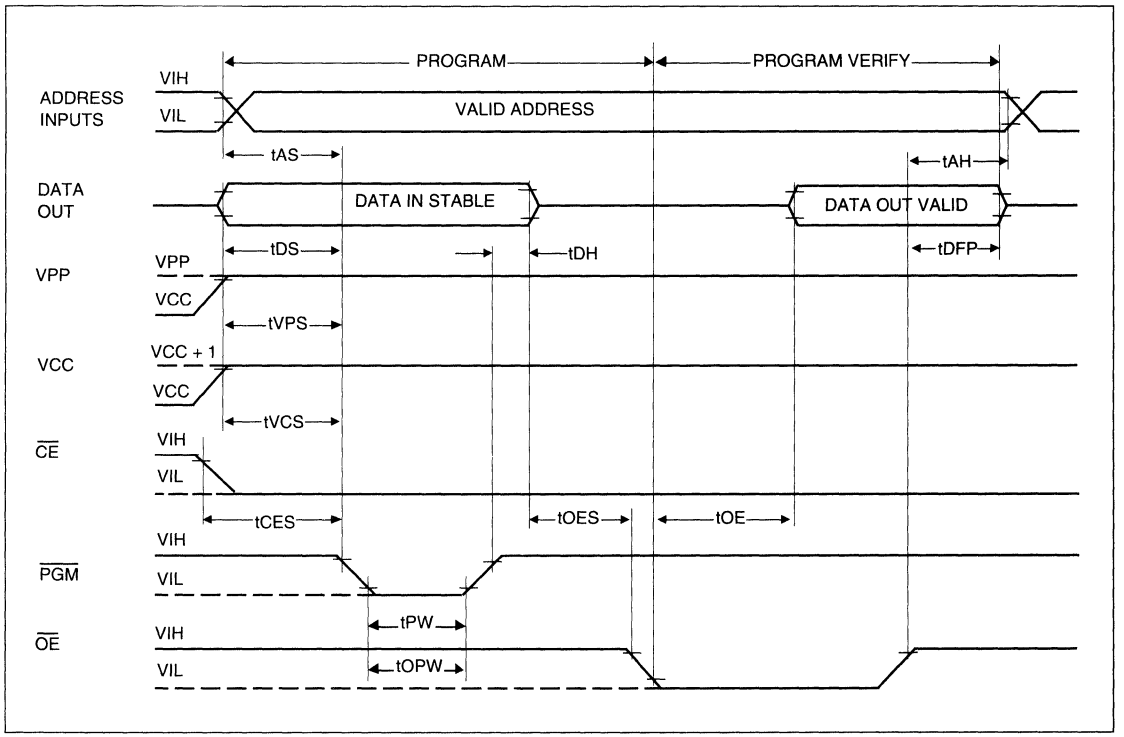
SYMBOL	PARAMETER		MIN.	MAX.	UNIT	CONDITIONS
tAS	Address Setup Time		2.0		μS	
tOES	$\overline{OE}$ Setup Time		2.0		μS	
tDS	Data Setup Time		2.0		μS	
tAH	Address Hold Time		0		μS	
tDH	Data Hold Time		2.0		μS	
tDFP	$\overline{CE}$ to Output Float Delay		0	130	nS	
tVPS	VPP Setup Time		2.0		mS	
tPW	$\overline{PGM}$ Program Pulse Width	*Fast*	95	105	mS	
		Interactive	0.95	1.05	mS	
tOPW	$\overline{PGM}$ Overprogram Pulse(Interactive)		1.95	2.05	mS	
tVCS	VCC Setup Time		2.0		mS	
tDV	Data Valid from $\overline{CE}$			250	nS	
tCES	$\overline{CE}$ Setup Time		2.0		μS	
tOE	Data valid from $\overline{OE}$			150	nS	

WAVEFORMS

READ CYCLE



INTERACTIVE PROGRAMMING ALGORITHM WAVEFORMS(NOTE1 & 2)



ORDERING INFORMATION

CERAMIC PACKAGE

PART NO.	ACCESS TIME(ns)	OPERATING CURRENT MAX.(mA)	STANDBY CURRENT MAX.(μ A)	PACKAGE
MX27C2000DC-90	90	60	100	32 Pin DIP
MX27C2000DC-12	120	60	100	32 Pin DIP
MX27C2000DC-15	150	60	100	32 Pin DIP

PLASTIC PACKAGE

PART NO.	ACCESS TIME(ns)	OPERATING CURRENT MAX.(mA)	STANDBY CURRENT MAX.(μ A)	PACKAGE
MX27C2000PC-90	90	60	100	32 Pin DIP
MX27C2000MC-90	90	60	100	32 Pin SOP
MX27C2000PC-12	120	60	100	32 Pin DIP
MX27C2000MC-12	120	60	100	32 Pin SOP
MX27C2000PC-15	150	60	100	32 Pin DIP
MX27C2000MC-15	150	60	100	32 Pin SOP

MX27C2100/27C2048

2M-BIT(256K x 8/128K x 16) CMOS EPROM

FEATURES

- 128K x 16 organization(MX27C2048, JEDEC pin out)
- 256K x 8 or 128K x 16 organization(MX27C2100, ROM pin out compatible)
- +12.5V programming voltage
- Fast access time: 90/120/150 ns
- Totally static operation
- Completely TTL compatible
- Operating current: 60mA
- Standby current: 100μA
- Package type:
  - 40 pin ceramic DIP
  - 40 pin plastic DIP
  - 44 pin PLCC (MX27C2048)

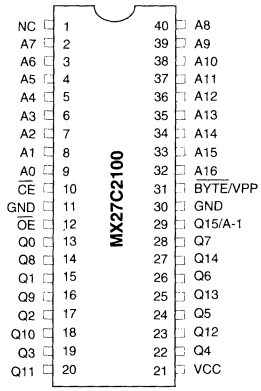
GENERAL DESCRIPTION

The MX27C2100/2048 is a 5V only, 2M-bit, ultraviolet Erasable Programmable Read Only Memory. It is organized as 128K words by 16 bits per word(MX27C2048), 256K x 8 or 128K x 16(MX27C2100), operates from a single + 5 volt supply, has a static standby mode, and features fast single address location programming. All programming signals are TTL levels, requiring a single pulse. For programming outside from the system, existing EPROM programmers may be used. The MX27C2100/2048 supports a intelligent quick pulse programming algorithm which can result in programming times of less than one minute.

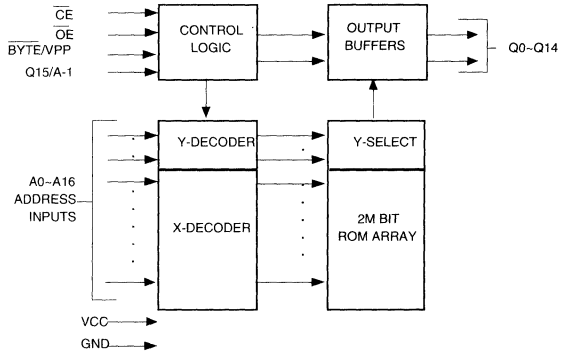
This EPROM is packaged in industry standard 40 pin dual-in-line ceramic packages or 40 pin plastic packages.

PIN CONFIGURATIONS

CDIP/PDIP(MX27C2100)

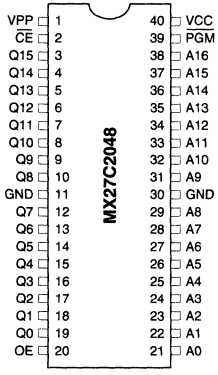


BLOCK DIAGRAM (MX27C2100)



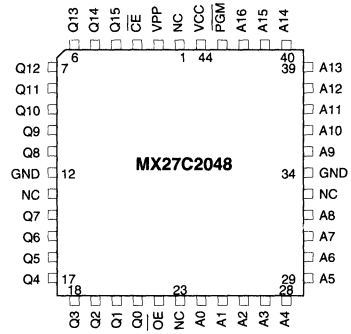
PIN CONFIGURATIONS

CDIP/PDIP(MX27C2048)

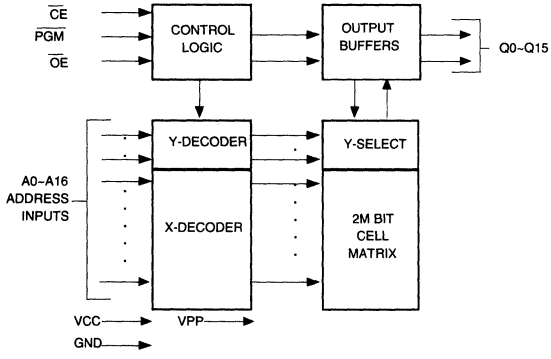


PIN CONFIGURATIONS

PLCC(MX27C2048)



BLOCK DIAGRAM (MX27C2048)



PIN DESCRIPTION(MX27C2100)

SYMBOL	PIN NAME
A0~A16	Address Input
Q0~Q14	Data Input/Output
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
$\overline{BYTE}$/VPP	Word/Byte Selection /Program Supply Voltage
Q15/A-1	Q15(Word mode)/LSB addr. (Byte mode)
VCC	Power Supply Pin (+5V)
GND	Ground Pin

PIN DESCRIPTION(MX27C2048)

SYMBOL	PIN NAME
A0~A16	Address Input
Q0~Q15	Data Input/Output
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
$\overline{PGM}$	Program Enable Input
VPP	Program Supply Voltage
VCC	Power Supply Pin (+5V)
GND	Ground Pin

TRUTH TABLE OF $\overline{BYTE}$ FUNCTION(MX27C2100)

BYTE MODE($\overline{BYTE}$ = GND)

$\overline{CE}$	$\overline{OE}$	D15/A-1	MODE	D0-D7	SUPPLY CURRENT	NOTE
H	X	X	Non selected	High Z	Standby(ICC2)	1
L	L/H	X	Non selected	High Z	Operating(ICC1)	1
L	H/L	A-1 input	Selected	DOUT	Operating(ICC1)	1

WORD MODE($\overline{BYTE}$ = VCC)

$\overline{CE}$	$\overline{OE}$	D15/A-1	MODE	D0-D14	SUPPLY CURRENT	NOTE
H	X	High Z	Non selected	High Z	Standby(ICC2)	1
L	L/H	High Z	Non selected	High Z	Operating(ICC1)	1
L	H/L	DOUT	Selected	DOUT	Operating(ICC1)	1

NOTE1: X = H or L

FUNCTIONAL DESCRIPTION

THE ERASURE OF THE MX27C2100/2048

The MX27C2100/2048 is erased by exposing the chip to an ultraviolet light source. A dosage of 15 W seconds/cm^2 is required to completely erase a MX27C2100/2048. This dosage can be obtained by exposure to an ultraviolet lamp — wavelength of 2537 Angstroms (Å) — with intensity of 12,000 μW/cm^2 for 15 to 20 minutes. The MX27C2100/2048 should be directly under and about one inch from the source and all filters should be removed from the UV light source prior to erasure.

It is important to note that the MX27C2100/2048, and similar devices, will be cleared for all bits of their programmed states with light sources having wavelengths shorter than 4000 Å. Although erasure times will be much longer than that with UV sources at 2537Å, nevertheless the exposure to fluorescent light and sunlight will eventually erase the MX27C2100/2048 and exposure to them should be prevented to realize maximum system reliability. If used in such an environment, the package window should be covered by an opaque label or substance.

THE PROGRAMMING OF THE MX27C2100/2048

When the MX27C2100/2048 is delivered, or it is erased, the chip has all 2M bits in the "ONE", or HIGH state. "ZEROs" are loaded into the MX27C2100/2048 through the procedure of programming.

The programming mode is entered when 12.5 ± 0.5V is applied to the VPP pin, $\overline{OE}$ is at VIH and $\overline{PGM}$ is at VIL (MX27C2048) and programming mode entered when 12.5 ± 5V is applied to the $\overline{BYTE}$/VPP pin, $\overline{OE}$ at VIH and $\overline{CE}$ at VIL (MX27C2100).

For programming, the data to be programmed is applied with 16 bits in parallel to the data pins.

The flowchart in Figure 1 shows MXIC's interactive algorithm. Interactive algorithm reduces programming time by using short programming pulses and giving each address only as many pulses as is necessary in order to reliably program the data. After each pulse is applied to a given address, the data in that address is verified. If the data is not verified, additional pulses are given until it is verified or the maximum is reached. This process is repeated while sequencing through each address of the MX27C2100/2048. This part of the algorithm is done at VCC = 6.0V to assure that each EPROM bit is programmed to a sufficiently high threshold voltage. After the interactive programming is completed, an overprogram pulse is given to each memory location; this ensures that all bits have sufficient margin. After the final address is completed, the entire EPROM memory is verified at VCC = 5V ± 10%.

FAST PROGRAMMING

The device is set up in the fast programming mode when the programming voltage VPP = 12.75V is applied, with VCC = 6.25 V and $\overline{PGM}$ = VIH (Algorithm is shown in Figure 2). The programming is achieved by applying a single TTL low level 100μs pulse to the $\overline{PGM}$ input after addresses and data line are stable. If the data is not verified, an additional pulse is applied for a maximum of 25 pulses. This process is repeated while sequencing through each address of the device. When the programming mode is completed, the data in all address is verified at VCC = VPP = 5V ± 10%.

PROGRAM INHIBIT MODE

Programming of multiple MX27C2100/2048's in parallel with different data is also easily accomplished by using the Program Inhibit Mode. Except for $\overline{CE}$ and $\overline{OE}$, all like inputs of the parallel MX27C2100/2048 may be common. A TTL low-level program pulse applied to an MX27C2100/2048 $\overline{CE}$ input with VPP = 12.5 ± 0.5 V will program the MX27C2100/2048. A high-level $\overline{CE}$ input inhibits the other MX27C2100/2048s from being programmed.

PROGRAM VERIFY MODE

Verification should be performed on the programmed bits to determine that they were correctly programmed. The verification should be performed with $\overline{OE}$ and $\overline{CE}$, at VIL, and VPP at its programming voltage.

AUTO IDENTIFY MODE

The auto identify mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and device type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its

corresponding programming algorithm. This mode is functional in the 25°C ± 5°C ambient temperature range that is required when programming the MX27C2100/2048.

To activate this mode, the programming equipment must force 12.0 ± 0.5 V on address line A9 of the device. Two identifier bytes may then be sequenced from the device outputs by toggling address line A0 from VIL to VIH. All other address lines must be held at VIL during auto identify mode.

Byte 0 (A0 = VIL) represents the manufacturer code, and byte 1 (A0 = VIH), the device identifier code. For the MX27C2100/2048, these two identifier bytes are given in the Mode Select Table. All identifiers for manufacturer and device codes will possess odd parity, with the MSB (DQ15) defined as the parity bit.

READ MODE

The MX27C2100/2048 has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (tACC) is equal to the delay from $\overline{CE}$ to output (tCE). Data is available at the outputs tOE after the falling edge of $\overline{OE}$'s, assuming that $\overline{CE}$ has been LOW and addresses have been stable for at least tACC - t OE.

WORD-WIDE MODE

With $\overline{BYTE}$/VPP at VCC ± 0.2V outputs Q0-7 present data D0-7 and outputs Q8-15 present data D8-15, after $\overline{CE}$ and $\overline{OE}$ are appropriately enabled.

BYTE-WIDE MODE

With $\overline{BYTE}$/VPP at GND ± 0.2V, outputs Q8-15 are tri-stated. If Q15/A-1 = VIH, outputs Q0-7 present data bits D8-15. If Q15/A-1 = VIL, outputs Q0-7 present data bits D0-7.

STANDBY MODE

The MX27C2100/2048 has a CMOS standby mode which reduces the maximum VCC current to 100 μA. It is placed in CMOS standby when $\overline{CE}$ is at VCC ± 0.3 V. The MX27C2100/2048 also has a TTL-standby mode which reduces the maximum VCC current to 1.5 mA. It is placed in TTL-standby when $\overline{CE}$ is at VIH. When in standby mode, the outputs are in a high-impedance state, independent of the $\overline{OE}$ input.

TWO-LINE OUTPUT CONTROL FUNCTION

To accommodate multiple memory connections, a two-line control function is provided to allow for:

1. Low memory power dissipation,
2. Assurance that output bus contention will not occur.

It is recommended that $\overline{CE}$ be decoded and used as the primary device-selecting function, while $\overline{OE}$ be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low-power standby mode and that the output pins are only active when data is desired from a particular memory device.

SYSTEM CONSIDERATIONS

During the switch between active and standby conditions, transient current peaks are produced on the rising and falling edges of Chip Enable. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. At a minimum, a 0.1 μF ceramic capacitor (high frequency, low inherent inductance) should be used on each device between Vcc and GND to minimize transient effects. In addition, to overcome the voltage drop caused by the inductive effects of the printed circuit board traces on EPROM arrays, a 4.7 μF bulk electrolytic capacitor should be used between VCC and GND for each eight devices. The location of the capacitor should be close to where the power supply is connected to the array.

MODE SELECT TABLE (MX27C2048)

	PINS						
MODE	**$\overline{CE}$**	**$\overline{OE}$**	**$\overline{PGM}$**	**A0**	**A9**	**VPP**	**OUTPUTS**
Read	VIL	VIL	VIH	X	X	VCC	DOUT
Output Disable	VIL	VIH	VIH	X	X	VCC	High Z
Standby (TTL)	VIH	X	X	X	X	VCC	High Z
Standby (CMOS)	VCC±0.3V	X	X	X	X	VCC	High Z
Program	VIL	VIH	VIL	X	X	VPP	DIN
Program Verify	VIL	VIL	VIH	X	X	VPP	DOUT
Program Inhibit	VIH	X	X	X	X	VPP	High Z
Manufacturer Code	VIL	VIL	X	VIL	VH	VCC	00C2H
Device Code	VIL	VIL	X	VIH	VH	VCC	0122H

NOTES: 1. VH = 12.0 V ± 0.5 V
2. X = Either VIH or VIL(For auto select)
3. A1 - A8 = A10 - A16 = VIL(For auto select)
4. See DC Programming Characteristics for VPP voltage during programming.

MODE SELECT TABLE (MX27C2100)

MODE	**NOTES**	**$\overline{CE}$**	**$\overline{OE}$**	**A9**	**A0**	**Q15/A-1**	**$\overline{BYTE}$/ VPP(4)**	**Q8-14**	**Q0-7**
Read (Word)	1	VIL	VIL	X	X	D15 Out	VCC	D8-14 Out	D0-7 Out
Read (Upper Byte)		VIL	VIL	X	X	VIH	GND	High Z	D8-15 Out
Read (Lower Byte)		VIL	VIL	X	X	VIL	GND	High Z	D0-7 Out
Output Disable		VIL	VIH	X	X	High Z	X	High Z	High Z
Standby		VIH	X	X	X	High Z	X	High Z	High Z
~~P~~rogram	2	VIL	VIH	X	X	D15 In	VPP	D8-14 In	D0-7 In
Program Verify		VIH	VIL	X	X	D15 Out	VPP	D8-14 Out	D0-7 Out
Program Inhibit		VIH	VIH	X	X	High Z	VPP	High Z	High Z
Manufacturer Code	2,3	VIL	VIL	VH	VIL	0B	VCC	00H	C2H
Device Code		VIL	VIL	VH	VIH	0B	VCC	00H	8AH

NOTES: 1. X can be VIL or VIH.
2. See DC Programming Characteristics for VPP voltages.
3. A1 - A8, A10 - A15 = VIL , A9 = VH = 12.0V ± 0.5V
4. $\overline{BYTE}$/VPP is intended for operation under DC Voltage conditions only.

FIGURE 1. INTERACTIVE PROGRAMMING FLOW CHART

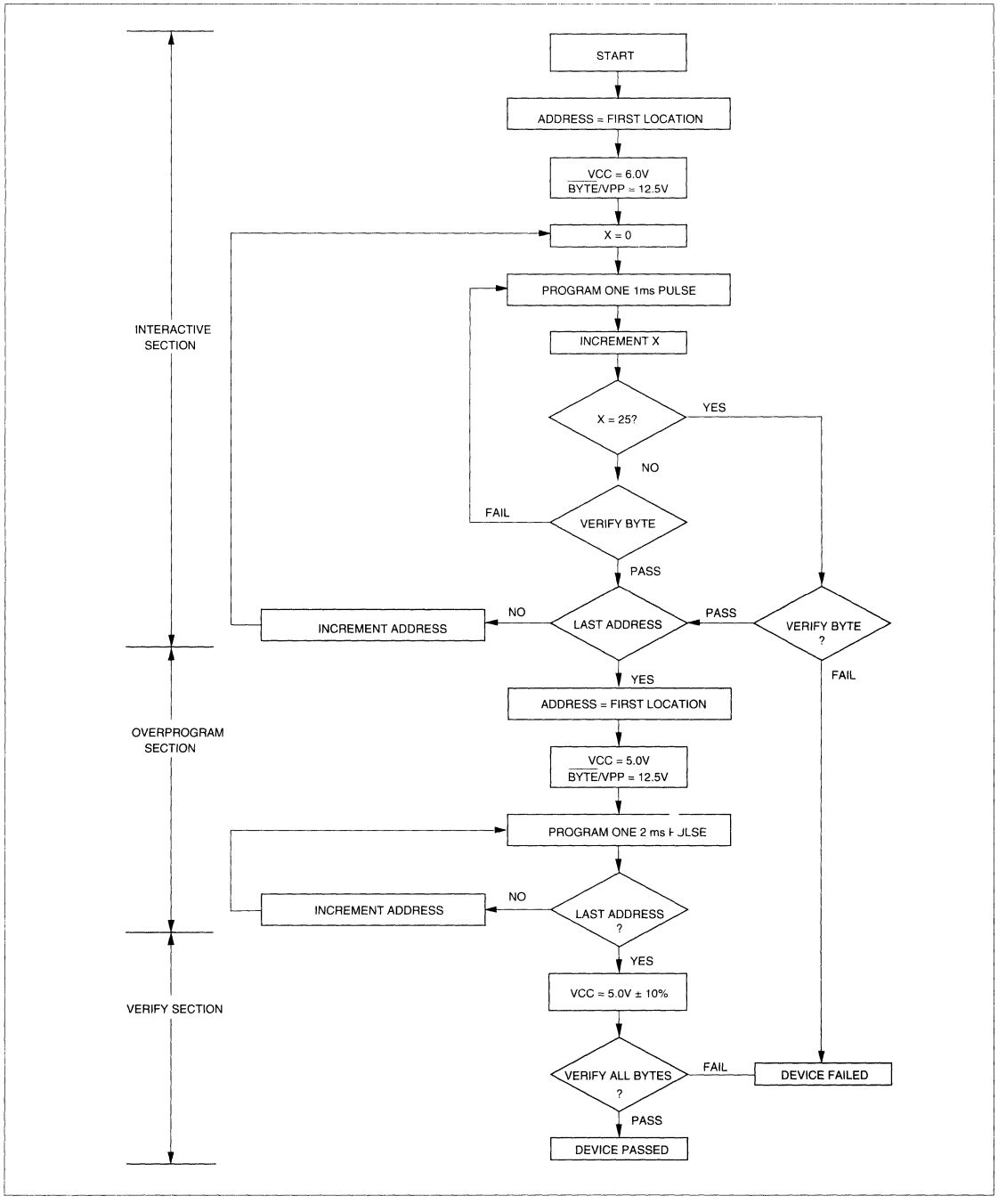
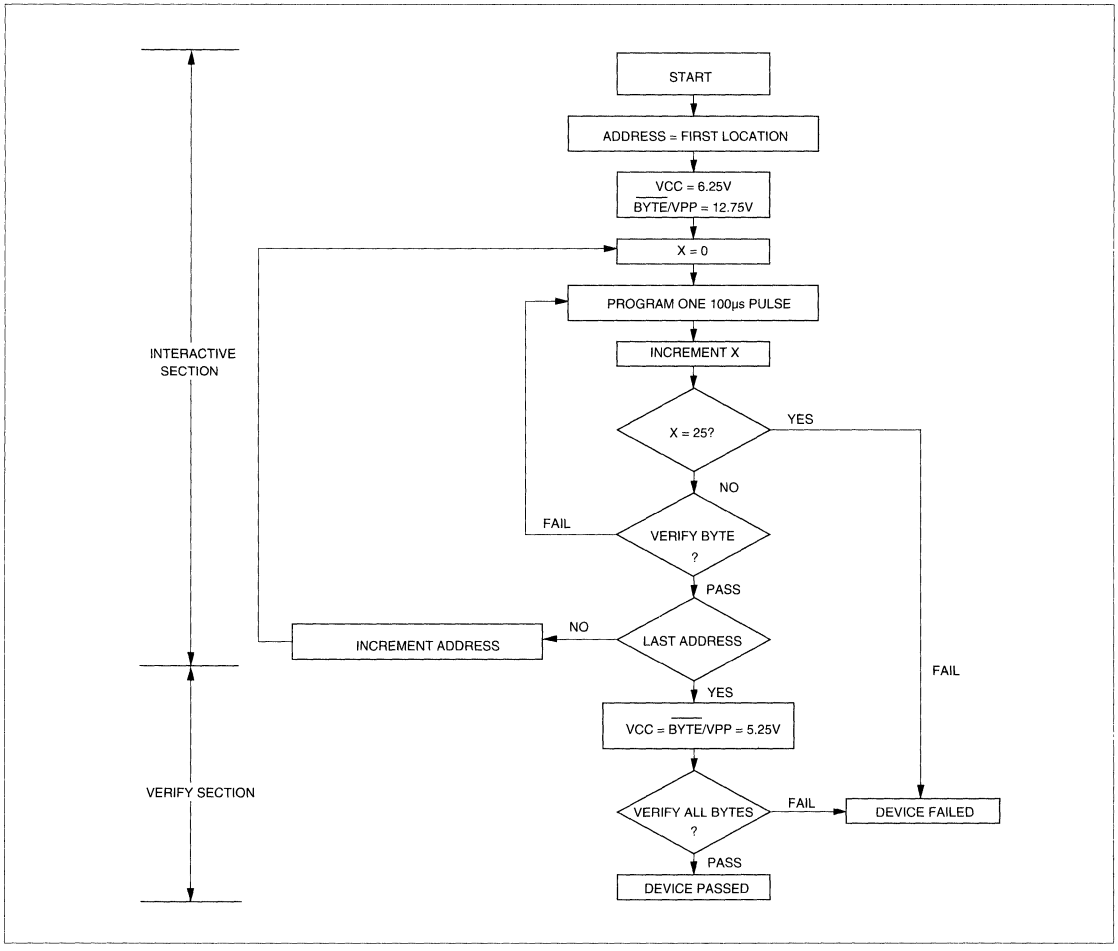
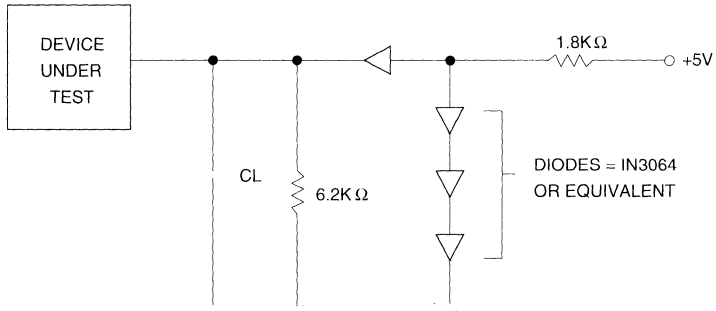


FIGURE 2. FAST PROGRAMMING FLOW CHART

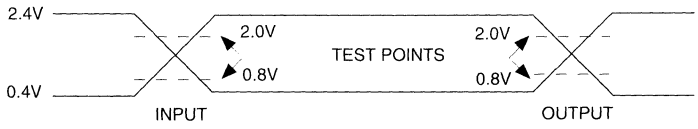


SWITCHING TEST CIRCUITS



CL = 100 pF Including jig capacitance

SWITCHING TEST WAVEFORMS



AC TESTING: Inputs are driven at 2.4V for a logic "1" and 0.4V for a logic "0".
Input pulse rise and fall times are <20ns.

ABSOLUTE MAXIMUM RATINGS

RATING	VALUE
Ambient Operating Temperature	0°C to 70°C
Storage Temperature	-65°C to 125°C
Applied Input Voltage	-0.5V to 7.0V
Applied Output Voltage	-0.5V to VCC + 0.5V
VCC to Ground Potential	-0.5V to 7.0V
A9 & Vpp	-0.5V to 13.5V

NOTICE:
Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended period may affect reliability.

NOTICE:
Specifications contained within the following tables are subject to change.

DC CHARACTERISTICS TA = 0°C to 70°C, VCC = 5V ± 10%

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
VOH	Output High Voltage	2.4		V	IOH = -0.4mA
VOL	Output Low Voltage		0.4	V	IOL = 2.1mA
VIH	Input High Voltage	2.0	VCC + 0.5	V	
VIL	Input Low Voltage	-0.3	0.8	V	
ILI	Input Leakage Current	-10	10	µA	VIN = 0 to 5.5V
ILO	Output Leakage Current	-10	10	µA	VOUT = 0 to 5.5V
ICC3	VCC Power-Down Current		100	µA	$\overline{CE}$ = VCC ± 0.3V
ICC2	VCC Standby Current		1.5	mA	$\overline{CE}$ = VIH
ICC1	VCC Active Current		60	mA	$\overline{CE}$ = VIL, f=5MHz, Iout = 0mA
IPP	VPP Supply Current Read		100	µA	$\overline{CE}$ = $\overline{OE}$ = VIL, VPP = 5.5V

CAPACITANCE TA = 25°C, f = 1.0 MHz (Sampled only)

SYMBOL	PARAMETER	TYP	MAX.	UNIT	CONDITIONS
CIN	Input Capacitance	8	12	pF	VIN = 0V
COUT	Output Capacitance	8	12	pF	VOUT = 0V
CVPP	VPP Capacitance	18	25	pF	VPP = 0V

AC CHARACTERISTICS TA = 0°C to 70°C, VCC = 5V± 10%

		27C2100/2048-90		27C2100/2048-12		27C2100/2048-15			
SYMBOL	PARAMETER	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	UNIT	CONDITIONS
tACC	Address to Output Delay		90		120		150	ns	$\overline{CE}$ = $\overline{OE}$ = VIL
tCE	Chip Enable to Output Delay		90		120		150	ns	$\overline{OE}$ = VIL
tOE	Output Enable to Output Delay		40		50		65	ns	$\overline{CE}$ = VIL
tDF	$\overline{OE}$ High to Output Float, or $\overline{CE}$ High to Output Float	0	25	0	35	0	50	ns	
tOH	Output Hold from Address, $\overline{CE}$ or $\overline{OE}$ which ever occurred first	0		0		0		ns	

AC CHARACTERISTICS(Continued)

SYMBOL	PARAMETER	27C2100-90 MIN.	27C2100-90 MAX.	27C2100-12 MIN.	27C2100-12 MAX.	27C2100-15 MIN.	27C2100-15 MAX.	UNIT	CONDITIONS
tBHA	$\overline{BYTE}$ Access Time		90		120		150	ns	
tOHB	$\overline{BYTE}$ Output Hold Time	0		0		0		ns	
tBHZ	$\overline{BYTE}$ Output Delay Time		70		70		70	ns	
tBLZ	$\overline{BYTE}$ Output Set Time	10		10		10		ns	

DC PROGRAMMING CHARACTERISTICS TA = 25°C ± 5°C

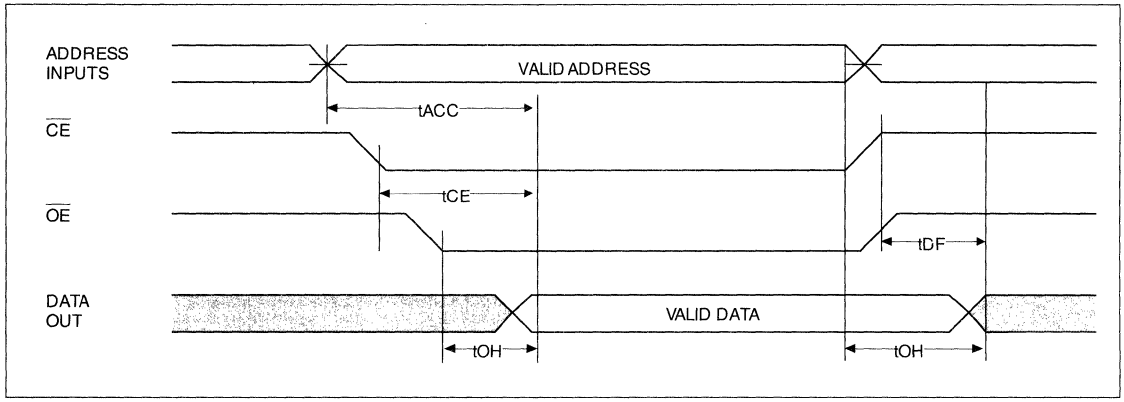
SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
VOH	Output High Voltage	2.4		V	IOH = -0.40mA
VOL	Output Low Voltage		0.4	V	IOL = 2.1mA
VIH	Input High Voltage	2.0	VCC + 0.5	V	
VIL	Input Low Voltage	-0.3	0.8	V	
ILI	Input Leakage Current	-10	10	µA	VIN = 0 to 5.5V
VH	A9 Auto Select Voltage	11.5	12.5	V	
ICC3	VCC Supply Current (Program & Verify)		50	mA	
IPP2	VPP Supply Current(Program)		30	mA	$\overline{CE}$ = VIL, $\overline{OE}$ = VIH
VCC1	Interactive Supply Voltage	5.75	6.25	V	
VPP1	Interactive Programming Voltage	12.0	13.0	V	
VCC2	Fast Programming Supply Voltage	6.00	6.50	V	
VPP2	Fast Programming Voltage	12.5	13.0	V	

AC PROGRAMMING CHARACTERISTICS TA = 25°C ± 5°C

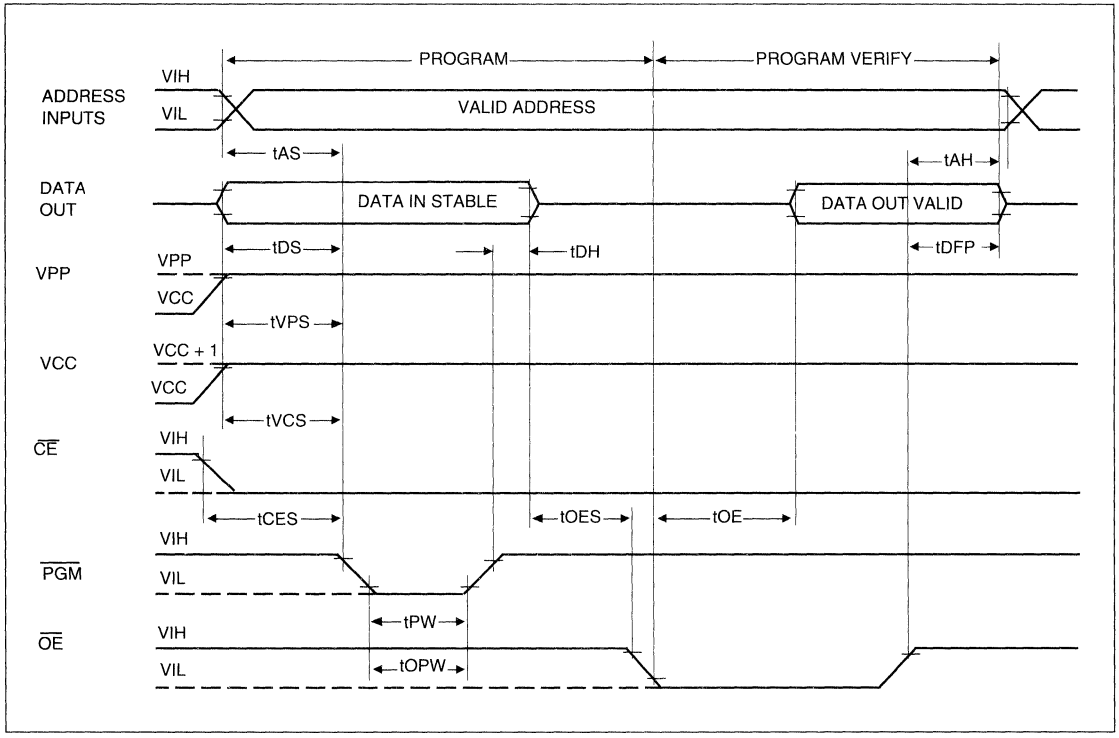
SYMBOL	PARAMETER		MIN.	MAX.	UNIT	CONDITIONS
tAS	Address Setup Time		2.0		µS	
tOES	$\overline{OE}$ Setup Time		2.0		µS	
tDS	Data Setup Time		2.0		µS	
tAH	Address Hold Time		0		µS	
tDH	Data Hold Time		2.0		µS	
tDFP	$\overline{CE}$ to Output Float Delay		0	130	nS	
tVPS	VPP Setup Time		2.0		µS	
tPW	$\overline{CE}$ Program Pulse Width	*Fast*	95	105	µS	
		Interactive	0.95	1.05	mS	
tOPW	$\overline{CE}$ Overprogram Pulse(Interactive)		1.95	2.05	mS	
tVCS	VCC Setup Time		2.0		µS	
tDV	Data Valid from $\overline{CE}$			250	nS	
tCES	$\overline{CE}$ Setup Time		2.0		µS	
tOE	Data valid from $\overline{OE}$			150	nS	

WAVEFORMS(MX27C2048)

READ CYCLE

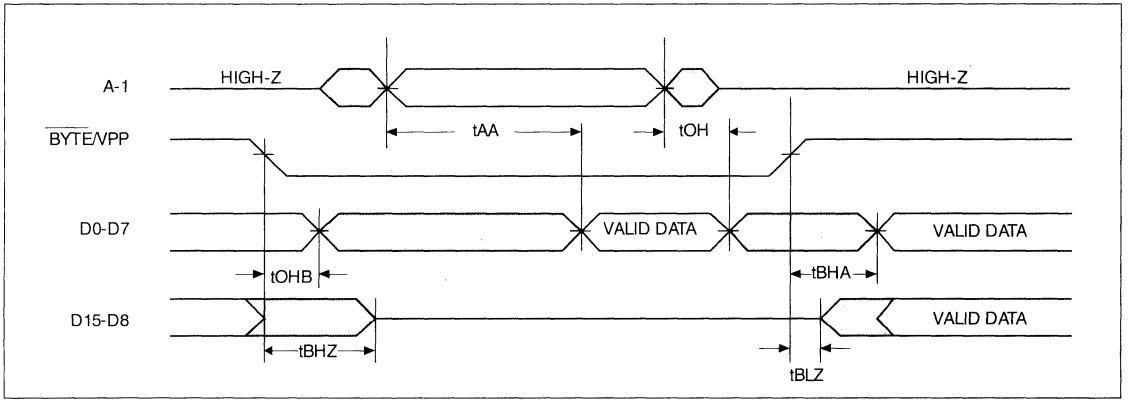


INTERACTIVE PROGRAMMING ALGORITHM WAVEFORMS

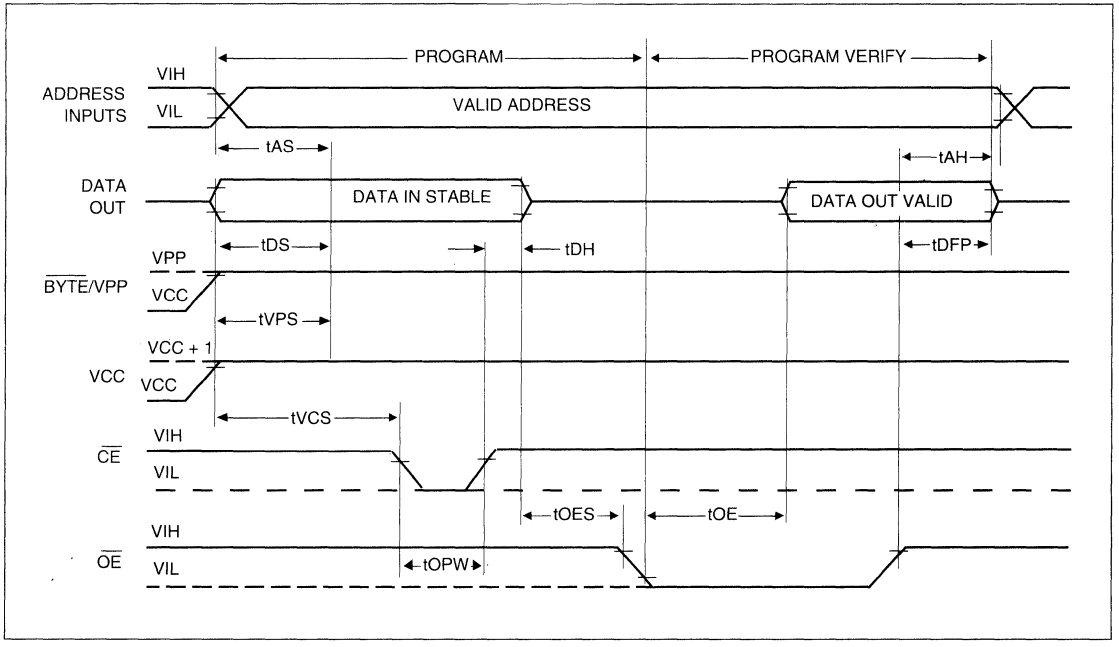


WAVEFORMS(MX27C2100)

PROPAGATION DELAY FROM CHIP ENABLE(ADDRESS VALID)



INTERACTIVE PROGRAMMING ALGORITHM WAVEFORMS



ORDERING INFORMATION

CERAMIC PACKAGE

PART NO.	ACCESS TIME (ns)	OPERATING CURRENT MAX.(mA)	STANDBY CURRENT MAX.(μ A)	PACKAGE
MX27C2100DC-90	90	60	100	40 Pin DIP(ROM pin out)
MX27C2100DC-12	120	60	100	40 Pin DIP(ROM pin out)
MX27C2100DC-15	150	60	100	40 Pin DIP(ROM pin out)
MX27C2048DC-90	90	60	100	40 Pin DIP(JEDEC pin out)
MX27C2048DC-12	120	60	100	40 Pin DIP(JEDEC pin out)
MX27C2048DC-15	150	60	100	40 Pin DIP(JEDEC pin out)

PLASTIC PACKAGE

PART NO.	ACCESS TIME (ns)	OPERATING CURRENT MAX.(mA)	STANDBY CURRENT MAX.(μ A)	PACKAGE
MX27C2100PC-90	90	60	100	40 Pin DIP(ROM pin out)
MX27C2100PC-12	120	60	100	40 Pin DIP(ROM pin out)
MX27C2100PC-15	150	60	100	40 Pin DIP(ROM pin out)
MX27C2048PC-90	90	60	100	40 Pin DIP(JEDEC pin out)
MX27C2048PC-12	120	60	100	40 Pin DIP(JEDEC pin out)
MX27C2048PC-15	150	60	100	40 Pin DIP(JEDEC pin out)
MX27C2048QC-90	90	60	100	44 Pin PLCC
MX27C2408QC-12	120	60	100	44 Pin PLCC
MX27C2408QC-15	150	60	100	44 Pin PLCC

MX27C4000

4M-BIT(512K x 8) CMOS EPROM

FEATURES

- 512K x 8 organization
- Single +5V power supply
- +12.5V programming voltage
- Fast access time: 120/150 ns
- Totally static operation
- Completely TTL compatible
- Operating current: 60mA
- Standby current: 100μA
- Package type:
  - 32 pin ceramic DIP, plastic DIP

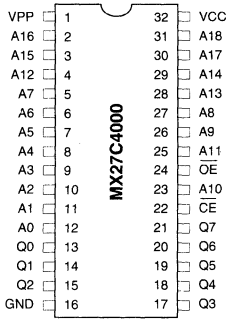
GENERAL DESCRIPTION

The MX27C4000 is a 5V only, 4M-bit, ultraviolet Erasable Programmable Read Only Memory. It is organized as 512K words by 8 bits per word, operates from a single +5 volt supply, has a static standby mode, and features fast single address location programming. All programming signals are TTL levels, requiring a single pulse. For programming outside from the system, existing EPROM programmers may be used. The MX27C4000 supports a intelligent quick pulse programming algorithm which can result in programming times of less than two minutes.

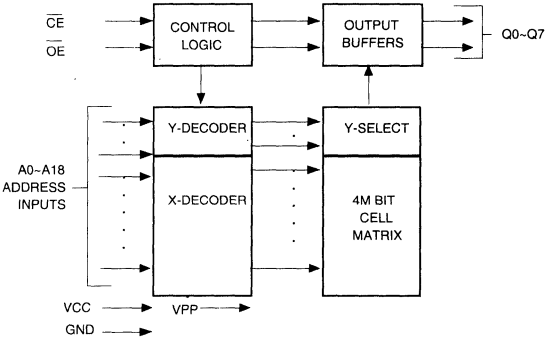
This EPROM is packaged in industry standard 32 pin dual-in-line packages.

PIN CONFIGURATIONS

32 CDIP/PDIP



BLOCK DIAGRAM



PIN DESCRIPTION

SYMBOL	PIN NAME
A0~A18	Address Input
Q0~Q7	Data Input/Output
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
VPP	Program Supply Voltage
VCC	Power Supply Pin (+5V)
GND	Ground Pin

FUNCTIONAL DESCRIPTION

THE ERASURE OF THE MX27C4000

The MX27C4000 is erased by exposing the chip to an ultraviolet light source. A dosage of 15 W seconds/cm^2 is required to completely erase a MX27C4000. This dosage can be obtained by exposure to an ultraviolet lamp — wavelength of 2537 Angstroms (Å) — with intensity of 12,000 μW/cm^2 for 15 to 20 minutes. The MX27C4000 should be directly under and about one inch from the source and all filters should be removed from the UV light source prior to erasure.

It is important to note that the MX27C4000, and similar devices, will be cleared for all bits of their programmed states with light sources having wavelengths shorter than 4000 Å. Although erasure times will be much longer than that with UV sources at 2537Å, nevertheless the exposure to fluorescent light and sunlight will eventually erase the MX27C4000 and exposure to them should be prevented to realize maximum system reliability. If used in such an environment, the package window should be covered by an opaque label or substance.

THE PROGRAMMING OF THE MX27C4000

When the MX27C4000 is delivered, or it is erased, the chip has all 4M bits in the "ONE", or HIGH state. "ZEROs" are loaded into the MX27C4000 through the procedure of programming.

The programming mode is entered when 12.5 ± 0.5 V is applied to the VPP pin, $\overline{OE}$ is at VIH, and $\overline{CE}$ is at VIL.

For programming, the data to be programmed is applied with 8 bits in parallel to the data pins.

The flowchart in Figure 1 shows MXIC's interactive algorithm. Interactive algorithm reduces programming time by using short programming pulses and giving each address only as many pulses as is necessary in order to reliably program the data. After each pulse is applied to a given address, the data in that address is verified. If the data is not verified, additional pulses are given until it is verified or the maximum is reached. This process is repeated while sequencing through each address of the MX27C4000. This part of the algorithm is done at VCC = 6.0V to assure that each EPROM bit is programmed to a sufficiently high threshold voltage. After the interactive programming is completed, an overprogram pulse is given to each memory location; this ensures that all bits have sufficient margin. After the final address is completed, the entire EPROM memory is verified at VCC = 5V ± 10%.

FAST PROGRAMMING

The device is set up in the fast programming mode when the programming voltage VPP = 12.75V is applied, with VCC = 6.25 V and $\overline{OE}$ = VIH (Algorithm is shown in Figure 2). The programming is achieved by applying a single TTL low level 100μs pulse to the $\overline{CE}$ input after addresses and data line are stable. If the data is not verified, an additional pulse is applied for a maximum of 25 pulses. This process is repeated while sequencing through each address of the device. When the programming mode is completed, the data in all address is verified at VCC = VPP = 5V ± 10%.

PROGRAM INHIBIT MODE

Programming of multiple MX27C4000s in parallel with different data is also easily accomplished by using the Program Inhibit Mode. Except for $\overline{CE}$ and $\overline{OE}$, all like inputs of the parallel MX27C4000 may be common. A TTL low-level program pulse applied to an MX27C4000 $\overline{CE}$ input with VPP = 12.5 ± 0.5 V and $\overline{CE}$ LOW will program that MX27C4000. A high-level $\overline{CE}$ input inhibits the other MX27C4000s from being programmed.

PROGRAM VERIFY MODE

Verification should be performed on the programmed bits to determine that they were correctly programmed. The verification should be performed with $\overline{OE}$ at VILand $\overline{CE}$, at VIH, and VPP at its programming voltage.

AUTO IDENTIFY MODE

The auto identify mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and device type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ± 5°C ambient temperature range that is required when programming the MX27C4000.

To activate this mode, the programming equipment must force 12.0 ± 0.5 V on address line A9 of the device. Two identifier bytes may then be sequenced from the device outputs by toggling address line A0 from VIL to VIH. All other address lines must be held at VIL during auto identify mode.

Byte 0 (A0 = VIL) represents the manufacturer code, and

byte 1 (A0 = VIH), the device identifier code. For the MX27C4000, these two identifier bytes are given in the Mode Select Table. All identifiers for manufacturer and device codes will possess odd parity, with the MSB (DQ7) defined as the parity bit.

READ MODE

The MX27C4000 has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (tACC) is equal to the delay from $\overline{CE}$ to output (tCE). Data is available at the outputs tOE after the falling edge of $\overline{OE}$'s, assuming that $\overline{CE}$ has been LOW and addresses have been stable for at least tACC - tOE.

STANDBY MODE

The MX27C4000 has a CMOS standby mode which reduces the maximum VCC current to 100 μA. It is placed in CMOS standby when $\overline{CE}$ is at VCC ± 0.3 V. The MX27C4000 also has a TTL-standby mode which reduces the maximum VCC current to 1.5 mA. It is placed in TTL-standby when $\overline{CE}$ is at VIH. When in standby mode, the outputs are in a high-impedance state, independent of the $\overline{OE}$ input.

TWO-LINE OUTPUT CONTROL FUNCTION

To accommodate multiple memory connections, a two-line control function is provided to allow for:

1. Low memory power dissipation,
2. Assurance that output bus contention will not occur.

It is recommended that $\overline{CE}$ be decoded and used as the primary device-selecting function, while $\overline{OE}$ be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low-power standby mode and that the output pins are only active when data is desired from a particular memory device.

SYSTEM CONSIDERATIONS

During the switch between active and standby conditions, transient current peaks are produced on the rising and falling edges of Chip Enable. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. At a minimum, a 0.1 μF ceramic capacitor (high frequency, low inherent inductance) should be used on each device between VCC and GND to minimize transient effects. In addition, to overcome the voltage drop caused by the inductive effects of the printed circuit board traces on EPROM arrays, a 4.7 μF bulk electrolytic capacitor should be used between VCC and GND for each eight devices. The location of the capacitor should be close to where the power supply is connected to the array.

MODE SELECT TABLE

	PINS					
MODE	**$\overline{CE}$**	**$\overline{OE}$**	**A0**	**A9**	**VPP**	**OUTPUTS**
Read	VIL	VIL	X	X	VCC	DOUT
Output Disable	VIL	VIH	X	X	VCC	High Z
Standby (TTL)	VIH	X	X	X	VCC	High Z
Standby (CMOS)	VCC±0.3V	X	X	X	VCC	High Z
Program	VIL	VIH	X	X	VPP	DIN
Program Verify	VIH	VIL	X	X	VPP	DOUT
Program Inhibit	VIH	X	X	X	VPP	High Z
Manufacturer Code	VIL	VIL	VIL	VH	VCC	C2H
Device Code	VIL	VIL	VIH	VH	VCC	40H

NOTES: 1. VH = 12.0 V ± 0.5 V
2. X = Either VIH or VIL(For auto select)
3. A1 - A8 = A10 - A16 = VIL(For auto select)
4. See DC Programming Characteristics for VPP voltage during programming.

FIGURE 1. INTERACTIVE PROGRAMMING FLOW CHART

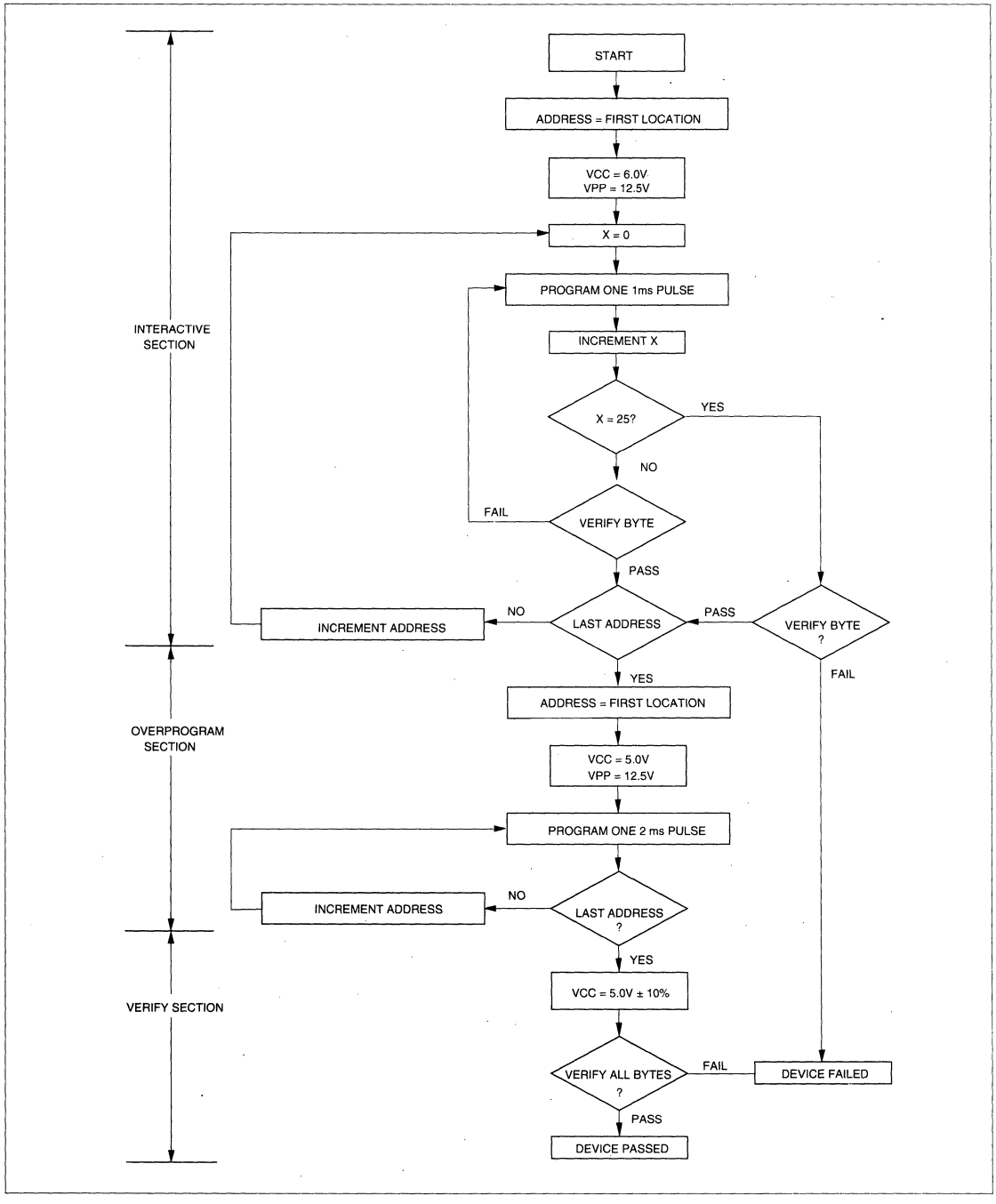
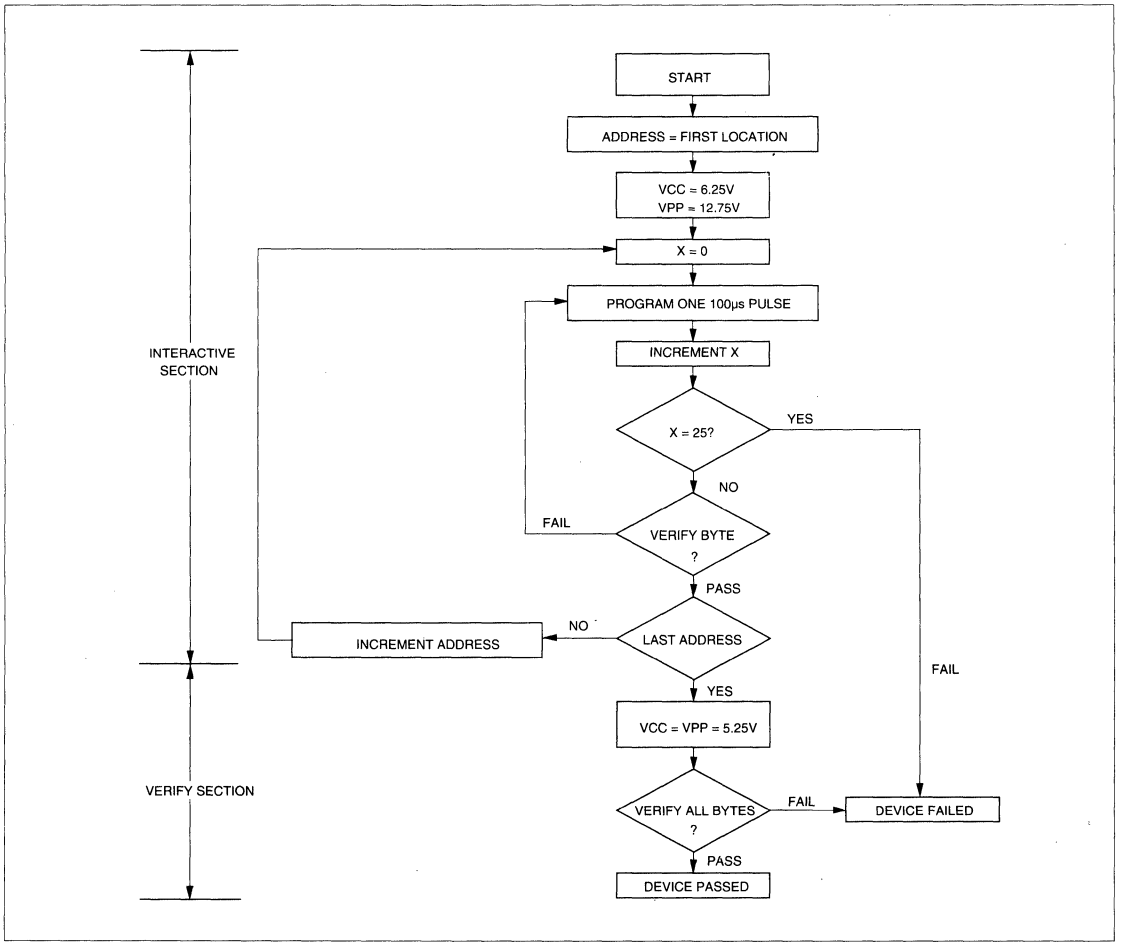
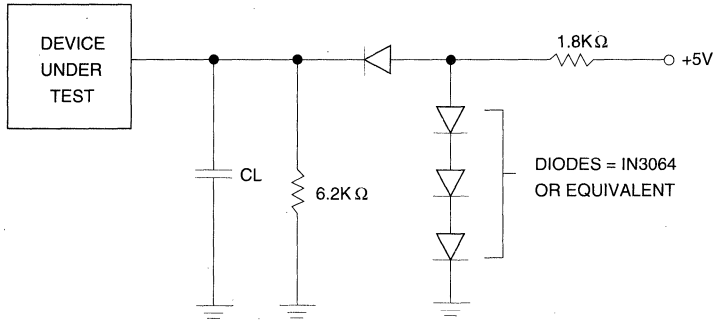


FIGURE 2. FAST PROGRAMMING FLOW CHART

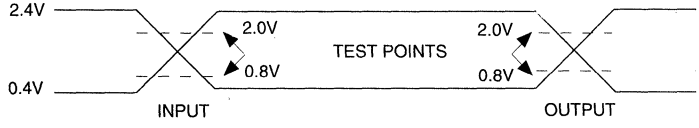


SWITCHING TEST CIRCUITS



CL = 100 pF Including jig capacitance

SWITCHING TEST WAVEFORMS



AC TESTING: Inputs are driven at 2.4V for a logic "1" and 0.4V for a logic "0".
Input pulse rise and fall times are ≤ 10ns.

ABSOLUTE MAXIMUM RATINGS

RATING	VALUE
Ambient Operating Temperature	0°C to 70°C
Storage Temperature	-65°C to 125°C
Applied Input Voltage	-0.5V to 7.0V
Applied Output Voltage	-0.5V to VCC + 0.5V
VCC to Ground Potential	-0.5V to 7.0V
V9 & VPP	-0.5V to 13.5V

NOTICE:
Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended period may affect reliability.

NOTICE:
Specifications contained within the following tables are subject to change.

DC CHARACTERISTICS TA = 0°C to 70°C, VCC = 5V ± 10%

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
VOH	Output High Voltage	2.4		V	IOH = -0.4mA
VOL	Output Low Voltage		0.4	V	IOL = 2.1mA
VIH	Input High Voltage	2.0	VCC + 0.5	V	
VIL	Input Low Voltage	-0.3	0.8	V	
ILI	Input Leakage Current	-10	10	µA	VIN = 0 to 5.5V
ILO	Output Leakage Current	-10	10	µA	VOUT = 0 to 5.5V
ICC3	VCC Power-Down Current		100	µA	$\overline{CE}$ = VCC ± 0.3V
ICC2	VCC Standby Current		1.5	mA	$\overline{CE}$ = VIH
ICC1	VCC Active Current		60	mA	$\overline{CE}$ = VIL, f=5MHz, Iout = 0mA
IPP	VPP Supply Current Read		100	µA	$\overline{CE}$ = $\overline{OE}$ = VIL, VPP = 5.5V
IPP2	VPP Supply Current (Program)		50	mA	

CAPACITANCE TA = 25°C, f = 1.0 MHz (Sampled only)

SYMBOL	PARAMETER	TYP.	MAX.	UNIT	CONDITIONS
CIN	Input Capacitance	8	12	pF	VIN = 0V
COUT	Output Capacitance	8	12	pF	VOUT = 0V
CVPP	VPP Capacitance	18	25	pF	VPP = 0V

AC CHARACTERISTICS TA = 0°C to 70°C, VCC = 5V± 10%

		27C4000-12		27C4000-15			
SYMBOL	PARAMETER	MIN.	MAX.	MIN.	MAX.	UNIT	CONDITIONS
tACC	Address to Output Delay		120		150	ns	$\overline{CE}$ = $\overline{OE}$ = VIL
tCE	Chip Enable to Output Delay		120		150	ns	$\overline{OE}$ = VIL
tOE	Output Enable to Output Delay		50		65	ns	$\overline{CE}$ = VIL
tDF	$\overline{OE}$ High to Output Float, or $\overline{CE}$ High to Output Float	0	35	0	50	ns	
tOH	Output Hold from Address, $\overline{CE}$ or $\overline{OE}$ which ever occurred first	0		0		ns	

DC PROGRAMMING CHARACTERISTICS TA = 25°C ± 5°C

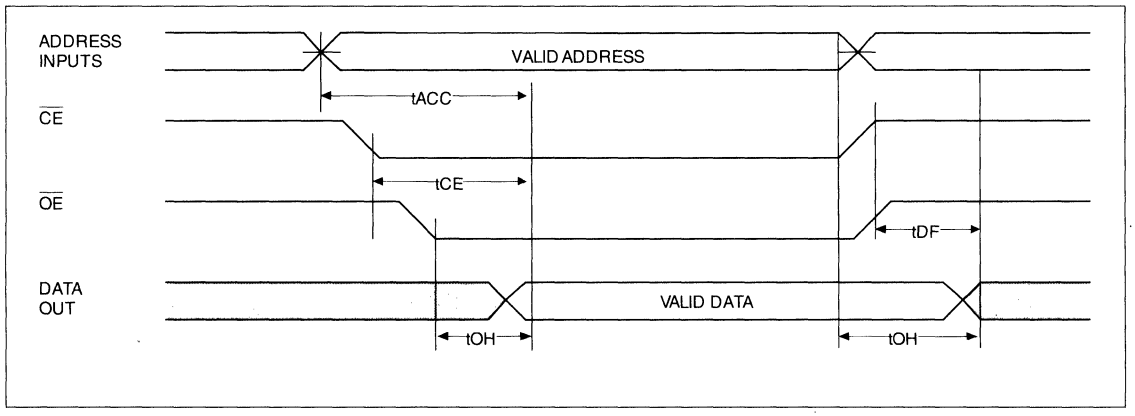
SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
VOH	Output High Voltage	2.4		V	IOH = -0.40mA
VOL	Output Low Voltage		0.4	V	IOL = 2.1mA
VIH	Input High Voltage	2.0	VCC + 0.5	V	
VIL	Input Low Voltage	-0.3	0.8	V	
ILI	Input Leakage Current	-10	10	μA	VIN = 0 to 5.5V
VH	A9 Auto Select Voltage	11.5	12.5	V	
ICC3	VCC Supply Current (Program & Verify)		50	mA	
IPP2	VPP Supply Current(Program)		30	mA	$\overline{CE}$ = VIL, $\overline{OE}$ = VIH
VCC1	Interactive Supply Voltage	5.75	6.25	V	
VPP1	Interactive Programming Voltage	12.0	13.0	V	
VCC2	Fast Programming Supply Voltage	6.00	6.50	V	
VPP2	Fast Programming Voltage	12.5	13.0	V	

AC PROGRAMMING CHARACTERISTICS TA = 25°C ± 5°C

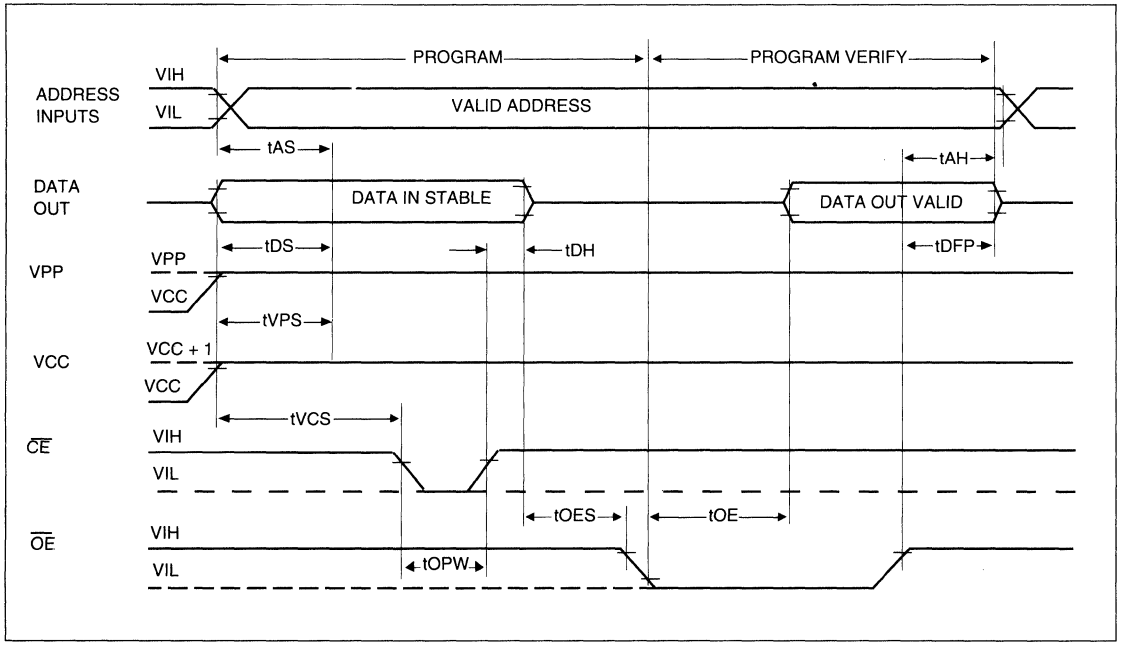
SYMBOL	PARAMETER		MIN.	MAX.	UNIT	CONDITIONS
tAS	Address Setup Time		2.0		μS	
tOES	$\overline{OE}$ Setup Time		2.0		μS	
tDS	Data Setup Time		2.0		μS	
tAH	Address Hold Time		0		μS	
tDH	Data Hold Time		2.0		μS	
tDFP	$\overline{CE}$ to Output Float Delay		0	130	nS	
tVPS	VPP Setup Time		2.0		μS	
tPW	$\overline{CE}$ Program Pulse Width	*Fast*	95	105	μS	
		Interactive	0.95	1.05	mS	
tOPW	$\overline{CE}$ Overprogram Pulse(Interactive)		1.95	2.05	mS	
tVCS	VCC Setup Time		2.0		μS	
tDV	Data Valid from $\overline{CE}$			250	nS	
tCES	$\overline{CE}$ Setup Time		2.0		μS	
tOE	Data valid from $\overline{OE}$			150	nS	

WAVEFORMS

READ CYCLE



INTERACTIVE PROGRAMMING ALGORITHM WAVEFORMS(NOTE1 & 2)



ORDERING INFORMATION

CERAMIC PACKAGE

PART NO.	ACCESS TIME(ns)	OPERATING CURRENT MAX.(mA)	STANDBY CURRENT MAX.(μ A)	PACKAGE
MX27C4000DC-12	120	60	100	32 Pin DIP
MX27C4000DC-15	150	60	100	32 Pin DIP

PLASTIC PACKAGE

PART NO.	ACCESS TIME(ns)	OPERATING CURRENT MAX.(mA)	STANDBY CURRENT MAX.(μ A)	PACKAGE
MX27C4000PC-12	120	60	100	32 Pin DIP
MX27C4000PC-15	150	60	100	32 Pin DIP

MX27C4100/27C4096

4M-BIT(512K x 8/256K x 16) CMOS EPROM

FEATURES

- 256K x 16 organization(MX27C4096, JEDEC pin out)
- 512K x 8 or 256K x 16 organization(MX27C4100, ROM pin out compatible)
- +12.5V programming voltage
- Fast access time: 120/150 ns
- Totally static operation
- Completely TTL compatible
- Operating current: 60mA
- Standby current: 100μA
- Package type:
  - 40 pin ceramic DIP
  - 40 pin plastic DIP
  - 44 pin PLCC

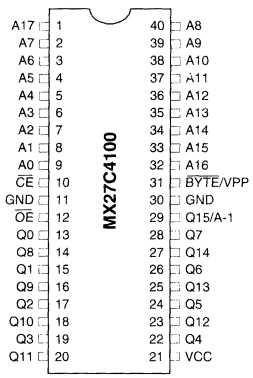
GENERAL DESCRIPTION

The MX27C4100/4096 is a 5V only, 4M-bit, ultraviolet Erasable Programmable Read Only Memory. It is organized as 256K words by 16 bits per word(MX27C4096), 512K x 8 or 256K x 16(MX27C4100), operates from a single + 5 volt supply, has a static standby mode, and features fast single address location programming. All programming signals are TTL levels, requiring a single pulse. For programming outside from the system, existing EPROM programmers may be used. The MX27C4100/4096 supports a intelligent quick pulse programming algorithm which can result in programming times of less than two minutes.

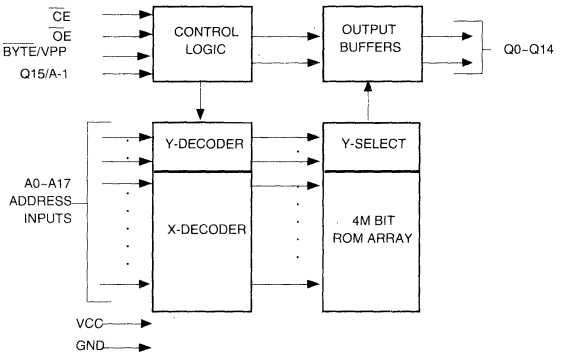
This EPROM is packaged in industry standard 40 pin dual-in-line ceramic packages or 40 pin plastic packages.

PIN CONFIGURATIONS

CDIP/PDIP(MX27C4100)

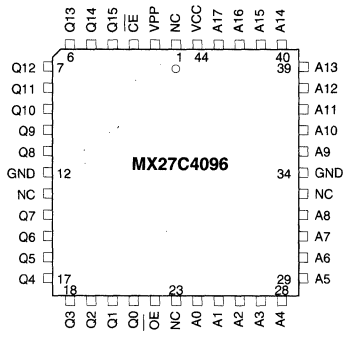


BLOCK DIAGRAM (MX27C4100)



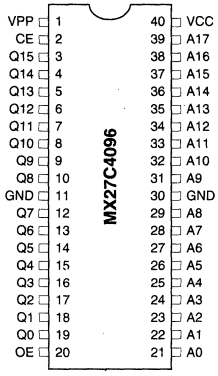
PIN CONFIGURATIONS

PLCC(MX27C4096)

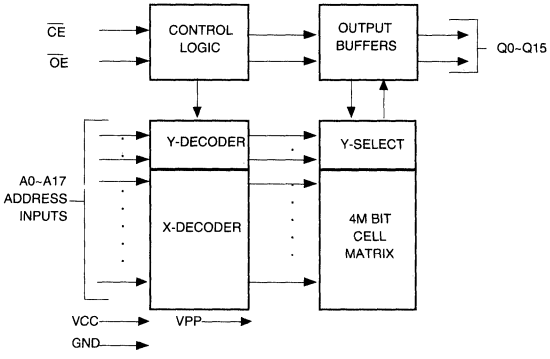


PIN CONFIGURATIONS

CDIP/PDIP(MX27C4096)



BLOCK DIAGRAM (MX27C4096)



PIN DESCRIPTION(MX27C4100)

SYMBOL	PIN NAME
A0~A17	Address Input
Q0~Q14	Data Input/Output
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
$\overline{BYTE}$/VPP	Word/Byte Selection /Program Supply Voltage
Q15/A-1	Q15(Word mode)/LSB addr. (Byte mode)
VCC	Power Supply Pin (+5V)
GND	Ground Pin

PIN DESCRIPTION(MX27C4096)

SYMBOL	PIN NAME
A0~A17	Address Input
Q0~Q15	Data Input/Output
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
VPP	Program Supply Voltage
VCC	Power Supply Pin (+5V)
GND	Ground Pin

TRUTH TABLE OF $\overline{BYTE}$ FUNCTION(MX27C4100)

BYTE MODE($\overline{BYTE}$ = GND)

$\overline{CE}$	OE/$\overline{OE}$	D15/A-1	MODE	D0-D7	SUPPLY CURRENT	NOTE
H	X	X	Non selected	High Z	Standby(ICC2)	1
L	L/H	X	Non selected	High Z	Operating(ICC1)	1
L	H/L	A-1 input	Selected	DOUT	Operating(ICC1)	1

WORD MODE($\overline{BYTE}$ = VCC)

$\overline{CE}$	OE/$\overline{OE}$	D15/A-1	MODE	D0-D14	SUPPLY CURRENT	NOTE
H	X	High Z	Non selected	High Z	Standby(ICC2)	1
L	L/H	High Z	Non selected	High Z	Operating(ICC1)	1
L	H/L	DOUT	Selected	DOUT	Operating(ICC1)	1

NOTE1: X = H or L

FUNCTIONAL DESCRIPTION

THE ERASURE OF THE MX27C4100/4096

The MX27C4100/4096 is erased by exposing the chip to an ultraviolet light source. A dosage of 15 W seconds/cm^2 is required to completely erase a MX27C4100/4096. This dosage can be obtained by exposure to an ultraviolet lamp — wavelength of 2537 Angstroms (Å) — with intensity of 12,000 μW/cm^2 for 15 to 20 minutes. The MX27C4100/4096 should be directly under and about one inch from the source and all filters should be removed from the UV light source prior to erasure.

It is important to note that the MX27C4100/4096, and similar devices, will be cleared for all bits of their programmed states with light sources having wavelengths shorter than 4000 Å. Although erasure times will be much longer than that with UV sources at 2537Å, nevertheless the exposure to fluorescent light and sunlight will eventually erase the MX27C4100/4096 and exposure to them should be prevented to realize maximum system reliability. If used in such an environment, the package window should be covered by an opaque label or substance.

THE PROGRAMMING OF THE MX27C4100/4096

When the MX27C4100/4096 is delivered, or it is erased, the chip has all 4M bits in the "ONE", or HIGH state. "ZEROs" are loaded into the MX27C4100/4096 through the procedure of programming.

The programming mode is entered when 12.5 ± 5V is applied to the VPP pin, $\overline{OE}$ is at VIH and $\overline{CE}$ is at VIL (MX27C4096) and programming mode entered when 12.5 ± 5V is applied to the $\overline{BYTE}$/VPP pin, $\overline{OE}$ at VIH and $\overline{CE}$ at VIL (MX27C4100).

For programming, the data to be programmed is applied with 16 bits in parallel to the data pins.

The flowchart in Figure 1 shows MXIC's interactive algorithm. Interactive algorithm reduces programming time by using short programming pulses and giving each address only as many pulses as is necessary in order to reliably program the data. After each pulse is applied to a given address, the data in that address is verified. If the data is not verified, additional pulses are given until it is verified or the maximum is reached. This process is repeated while sequencing through each address of the MX27C4100/4096. This part of the algorithm is done at VCC = 6.0V to assure that each EPROM bit is programmed to a sufficiently high threshold voltage. After the interactive programming is completed, an overprogram pulse is given to each memory location; this ensures that all bits have sufficient margin. After the final address is completed, the entire EPROM memory is verified at VCC = 5V ± 10%.

FAST PROGRAMMING

The device is set up in the fast programming mode when the programming voltage VPP = 12.75V is applied, with VCC = 6.25 V and $\overline{OE}$ = VIH (Algorithm is shown in Figure 2). The programming is achieved by applying a single TTL low level 100μs pulse to the $\overline{CE}$ input after addresses and data line are stable. If the data is not verified, an additional pulse is applied for a maximum of 25 pulses. This process is repeated while sequencing through each address of the device. When the programming mode is completed, the data in all address is verified at VCC = VPP = 5V ± 10%.

PROGRAM INHIBIT MODE

Programming of multiple MX27C4100/4096's in parallel with different data is also easily accomplished by using the Program Inhibit Mode. Except for $\overline{CE}$ and $\overline{OE}$, all like inputs of the parallel MX27C4100/4096 may be common. A TTL low-level program pulse applied to an MX27C4100/4096 $\overline{CE}$ input with VPP = 12.5 ± 0.5 V will program the MX27C4100/4096. A high-level $\overline{CE}$ input inhibits the other MX27C4100/4096s from being programmed.

PROGRAM VERIFY MODE

Verification should be performed on the programmed bits to determine that they were correctly programmed. The verification should be performed with $\overline{OE}$ and $\overline{CE}$, at VIL, and VPP at its programming voltage.

AUTO IDENTIFY MODE

The auto identify mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and device type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its

corresponding programming algorithm. This mode is functional in the 25°C ± 5°C ambient temperature range that is required when programming the MX27C4100/4096.

To activate this mode, the programming equipment must force 12.0 ± 0.5 V on address line A9 of the device. Two identifier bytes may then be sequenced from the device outputs by toggling address line A0 from VIL to VIH. All other address lines must be held at VIL during auto identify mode.

Byte 0 (A0 = VIL) represents the manufacturer code, and byte 1 (A0 = VIH), the device identifier code. For the MX27C4100/4096, these two identifier bytes are given in the Mode Select Table. All identifiers for manufacturer and device codes will possess odd parity, with the MSB (DQ15) defined as the parity bit.

READ MODE

The MX27C4100/4096 has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (tACC) is equal to the delay from $\overline{CE}$ to output (tCE). Data is available at the outputs tOE after the falling edge of $\overline{OE}$'s, assuming that $\overline{CE}$ has been LOW and addresses have been stable for at least tACC - t OE.

WORD-WIDE MODE

With $\overline{BYTE}$/VPP at VCC ± 0.2V outputs Q0-7 present data D0-7 and outputs Q8-15 present data D8-15, after $\overline{CE}$ and $\overline{OE}$ are appropriately enabled.

BYTE-WIDE MODE

With $\overline{BYTE}$/VPP at GND ± 0.2V, outputs Q8-15 are tri-stated. If Q15/A-1 = VIH, outputs Q0-7 present data bits D8-15. If Q15/A-1 = VIL, outputs Q0-7 present data bits D0-7.

STANDBY MODE

The MX27C4100/4096 has a CMOS standby mode which reduces the maximum VCC current to 100 μA. It is placed in CMOS standby when $\overline{CE}$ is at VCC ± 0.3 V. The MX27C4100/4096 also has a TTL-standby mode which reduces the maximum VCC current to 1.5 mA. It is placed in TTL-standby when $\overline{CE}$ is at VIH. When in standby mode, the outputs are in a high-impedance state, independent of the $\overline{OE}$ input.

TWO-LINE OUTPUT CONTROL FUNCTION

To accommodate multiple memory connections, a two-line control function is provided to allow for:

1. Low memory power dissipation,
2. Assurance that output bus contention will not occur.

It is recommended that $\overline{CE}$ be decoded and used as the primary device-selecting function, while $\overline{OE}$ be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low-power standby mode and that the output pins are only active when data is desired from a particular memory device.

SYSTEM CONSIDERATIONS

During the switch between active and standby conditions, transient current peaks are produced on the rising and falling edges of Chip Enable. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. At a minimum, a 0.1 μF ceramic capacitor (high frequency, low inherent inductance) should be used on each device between Vcc and GND to minimize transient effects. In addition, to overcome the voltage drop caused by the inductive effects of the printed circuit board traces on EPROM arrays, a 4.7 μF bulk electrolytic capacitor should be used between VCC and GND for each eight devices. The location of the capacitor should be close to where the power supply is connected to the array.

MODE SELECT TABLE (MX27C4096)

	PINS					
MODE	**$\overline{CE}$**	**$\overline{OE}$**	**A0**	**A9**	**VPP**	**OUTPUTS**
Read	VIL	VIL	X	X	VCC	DOUT
Output Disable	VIL	VIH	X	X	VCC	High Z
Standby (TTL)	VIH	X	X	X	VCC	High Z
Standby (CMOS)	VCC±0.3V	X	X	X	VCC	High Z
Program	VIL	VIH	X	X	VPP	DIN
Program Verify	VIH	VIL	X	X	VPP	DOUT
Program Inhibit	VIH	X	X	X	VPP	High Z
Manufacturer Code	VIL	VIL	VIL	VH	VCC	00C2H
Device Code	VIL	VIL	VIH	VH	VCC	0151H

NOTES: 1. VH = 12.0 V ± 0.5 V
2. X = Either VIH or VIL(For auto select)
3. A1 - A8 = A10 - A16 = VIL(For auto select)
4. See DC Programming Characteristics for VPP voltage during programming.

MODE SELECT TABLE (MX27C4100)

MODE	**NOTES**	**$\overline{CE}$**	**$\overline{OE}$**	**A9**	**A0**	**Q15/A-1**	**$\overline{BYTE}$/ VPP(4)**	**Q8-14**	**Q0-7**
Read (Word)	1	VIL	VIL	X	X	D15 Out	VCC	D8-14 Out	D0-7 Out
Read (Upper Byte)		VIL	VIL	X	X	VIH	GND	High Z	D8-15 Out
Read (Lower Byte)		VIL	VIL	X	X	VIL	GND	High Z	D0-7 Out
Output Disable		VIL	VIH	X	X	High Z	X	High Z	High Z
Standby		VIH	X	X	X	High Z	X	High Z	High Z
Program	2	VIL	VIH	X	X	D15 In	VPP	D8-14 In	D0-7 In
Program Verify		VIH	VIL	X	X	D15 Out	VPP	D8-14 Out	D0-7 Out
Program Inhibit		VIH	VIH	X	X	High Z	VPP	High Z	High Z
Manufacturer Code	2,3	VIL	VIL	VH	VIL	0B	VCC	00H	C2H
Device Code		VIL	VIL	VH	VIH	0B	VCC	98H	B800H

NOTES: 1. X can be VIL or VIH.
2. See DC Programming Characteristics for VPP voltages.
3. A1 - A8, A10 - A15 = VIL , A9 = VH = 12.0V ± 0.5V
4. $\overline{BYTE}$/VPP is intended for operation under DC Voltage conditions only.

FIGURE 1. INTERACTIVE PROGRAMMING FLOW CHART

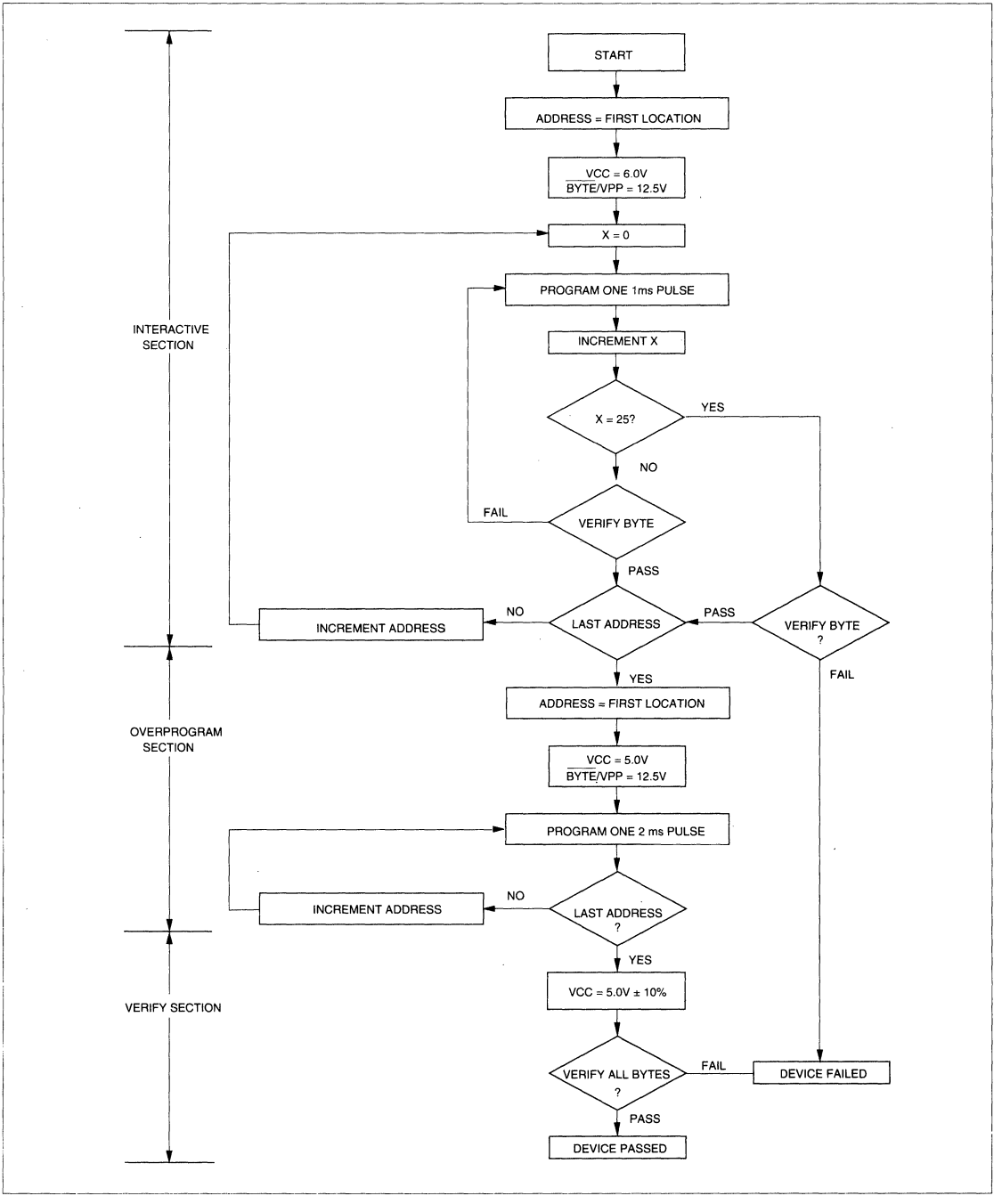
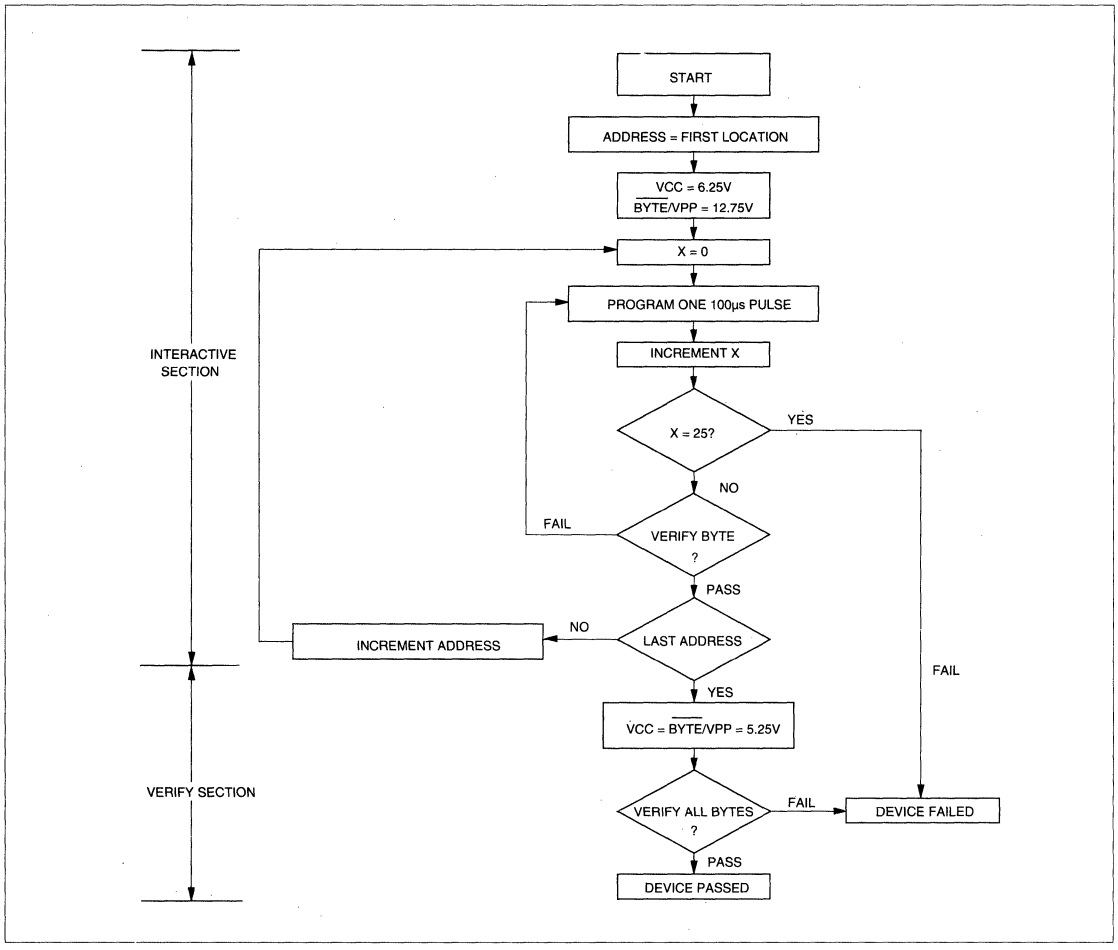
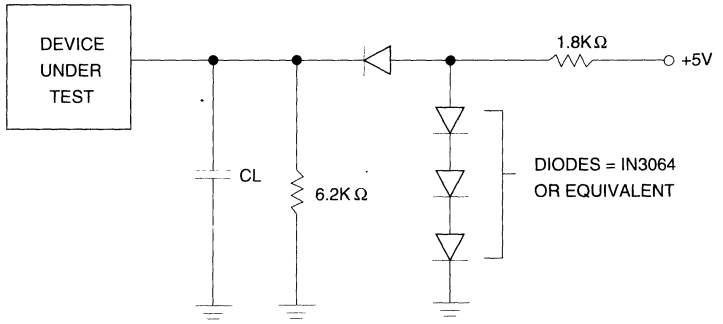


FIGURE 2. FAST PROGRAMMING FLOW CHART

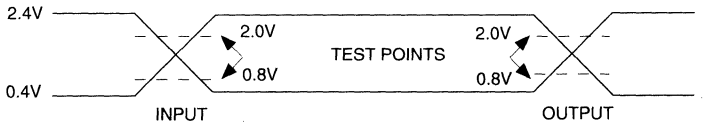


SWITCHING TEST CIRCUITS



CL = 100 pF Including jig capacitance

SWITCHING TEST WAVEFORMS



AC TESTING: Inputs are driven at 2.4V for a logic "1" and 0.4V for a logic "0".
Input pulse rise and fall times are <20ns.

ABSOLUTE MAXIMUM RATINGS

RATING	VALUE
Ambient Operating Temperature	0°C to 70°C
Storage Temperature	-65°C to 125°C
Applied Input Voltage	-0.5V to 7.0V
Applied Output Voltage	-0.5V to VCC + 0.5V
VCC to Ground Potential	-0.5V to 7.0V
A9 & VPP	-0.5V to 13.5V

NOTICE:
Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended period may affect reliability.

NOTICE:
Specifications contained within the following tables are subject to change.

DC CHARACTERISTICS TA = 0°C to 70°C, VCC = 5V ± 10%

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
VOH	Output High Voltage	2.4		V	IOH = -0.4mA
VOL	Output Low Voltage		0.4	V	IOL = 2.1mA
VIH	Input High Voltage	2.0	VCC + 0.5	V	
VIL	Input Low Voltage	-0.3	0.8	V	
ILI	Input Leakage Current	-10	10	µA	VIN = 0 to 5.5V
ILO	Output Leakage Current	-10	10	µA	VOUT = 0 to 5.5V
ICC3	VCC Power-Down Current		100	µA	$\overline{CE}$ = VCC ± 0.3V
ICC2	VCC Standby Current		1.5	mA	$\overline{CE}$ = VIH
ICC1	VCC Active Current		60	mA	$\overline{CE}$ = VIL, f=5MHz, Iout = 0mA
IPP	VPP Supply Current Read		100	µA	$\overline{CE}$ = $\overline{OE}$ = VIL, VPP = 5.5V

CAPACITANCE TA = 25°C, f = 1.0 MHz (Sampled only)

SYMBOL	PARAMETER	TYP.	MAX.	UNIT	CONDITIONS
CIN	Input Capacitance	8	12	pF	VIN = 0V
COUT	Output Capacitance	8	12	pF	VOUT = 0V
CVPP	VPP Capacitance	18	25	pF	VPP = 0V

AC CHARACTERISTICS TA = 0°C to 70°C, VCC = 5V± 10%

		27C4100/4096-12		27C4100/4096-15			
SYMBOL	PARAMETER	MIN.	MAX.	MIN.	MAX.	UNIT	CONDITIONS
tACC	Address to Output Delay		120		150	ns	$\overline{CE}$ = $\overline{OE}$ = VIL
tCE	Chip Enable to Output Delay		120		150	ns	$\overline{OE}$ = VIL
tOE	Output Enable to Output Delay		50		65	ns	$\overline{CE}$ = VIL
tDF	$\overline{OE}$ High to Output Float, or $\overline{CE}$ High to Output Float	0	35	0	50	ns	
tOH	Output Hold from Address, $\overline{CE}$ or $\overline{OE}$ which ever occurred first	0		0		ns	

AC CHARACTERISTICS(Continued)

SYMBOL	PARAMETER	27C4100-12 MIN.	27C4100-12 MAX.	27C4100-15 MIN.	27C4100-15 MAX.	UNIT	CONDITIONS
tBHA	$\overline{BYTE}$ Access Time		120		150	ns	
tOHB	$\overline{BYTE}$ Output Hold Time	0		0		ns	
tBHZ	$\overline{BYTE}$ Output Delay Time		70		70	ns	
tBLZ	$\overline{BYTE}$ Output Set Time	10		10		ns	

DC PROGRAMMING CHARACTERISTICS TA = 25°C ± 5°C

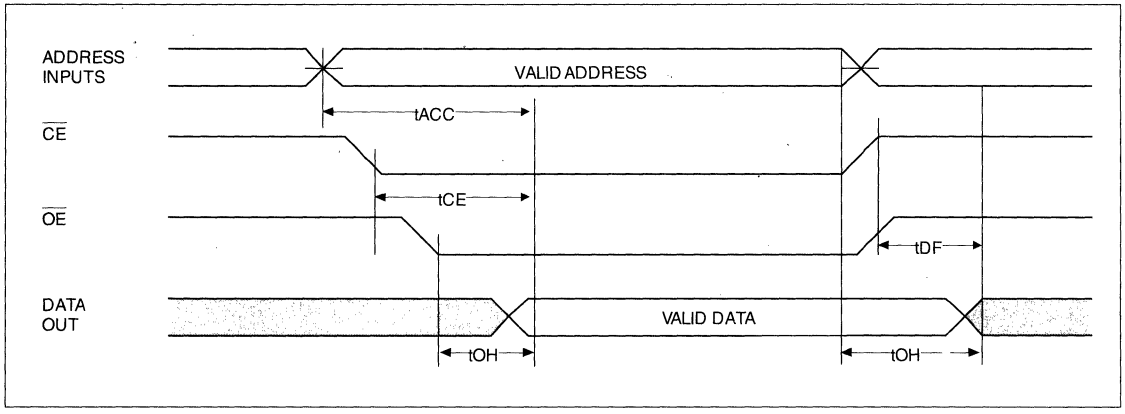
SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
VOH	Output High Voltage	2.4		V	IOH = -0.40mA
VOL	Output Low Voltage		0.4	V	IOL = 2.1mA
VIH	Input High Voltage	2.0	VCC + 0.5	V	
VIL	Input Low Voltage	-0.3	0.8	V	
ILI	Input Leakage Current	-10	10	µA	VIN = 0 to 5.5V
VH	A9 Auto Select Voltage	11.5	12.5	V	
ICC3	VCC Supply Current (Program & Verify)		50	mA	
IPP2	VPP Supply Current(Program)		30	mA	$\overline{CE}$ = VIL, $\overline{OE}$ = VIH
VCC1	Interactive Supply Voltage	5.75	6.25	V	
VPP1	Interactive Programming Voltage	12.0	13.0	V	
VCC2	Fast Programming Supply Voltage	6.00	6.50	V	
VPP2	Fast Programming Voltage	12.5	13.0	V	

AC PROGRAMMING CHARACTERISTICS TA = 25°C ± 5°C

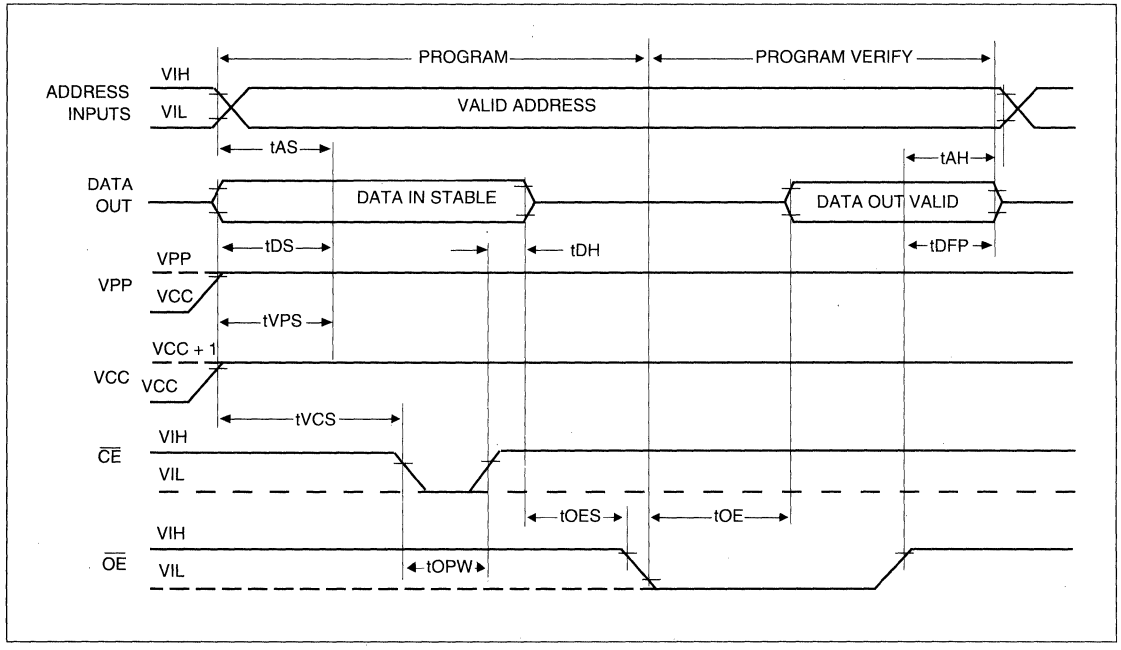
SYMBOL	PARAMETER		MIN.	MAX.	UNIT	CONDITIONS
tAS	Address Setup Time		2.0		µS	
tOES	$\overline{OE}$ Setup Time		2.0		µS	
tDS	Data Setup Time		2.0		µS	
tAH	Address Hold Time		0		µS	
tDH	Data Hold Time		2.0		µS	
tDFP	$\overline{CE}$ to Output Float Delay		0	130	nS	
tVPS	VPP Setup Time		2.0		µS	
tPW	$\overline{CE}$ Program Pulse Width	*Fast*	95	105	µS	
		Interactive	0.95	1.05	mS	
tOPW	$\overline{CE}$ Overprogram Pulse(Interactive)		1.95	2.05	mS	
tVCS	VCC Setup Time		2.0		µS	
tDV	Data Valid from $\overline{CE}$			250	nS	
tCES	$\overline{CE}$ Setup Time		2.0		µS	
tOE	Data valid from $\overline{OE}$			150	nS	

WEFORMS(MX27C4096)

READ CYCLE

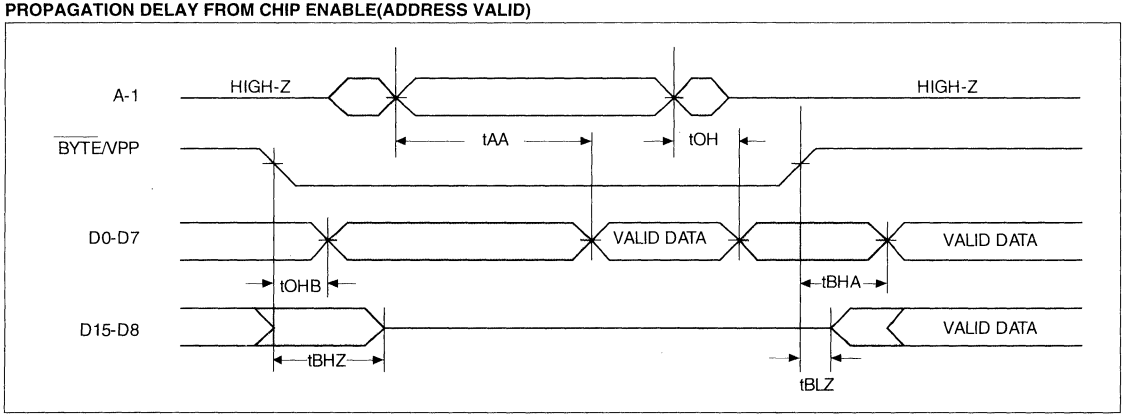


INTERACTIVE PROGRAMMING ALGORITHM WAVEFORMS

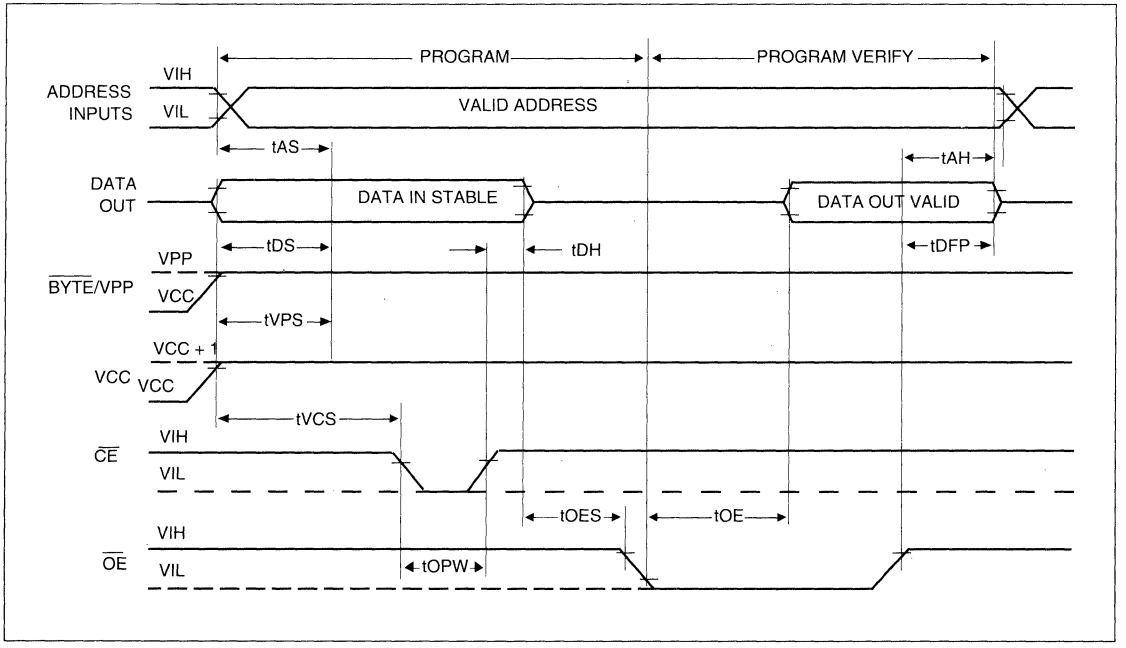


WAVEFORMS(MX27C4100)

PROPAGATION DELAY FROM CHIP ENABLE(ADDRESS VALID)



INTERACTIVE PROGRAMMING ALGORITHM WAVEFORMS



ORDERING INFORMATION

CERAMIC PACKAGE

PART NO.	ACCESS TIME (ns)	OPERATING CURRENT MAX.(mA)	STANDBY CURRENT MAX.(μ A)	PACKAGE
MX27C4100DC-12	120	60	100	40 Pin DIP(ROM pin out)
MX27C4100DC-15	150	60	100	40 Pin DIP(ROM pin out)
MX27C4096DC-12	120	60	100	40 Pin DIP(JEDEC pin out)
MX27C4096DC-15	150	60	100	40 Pin DIP(JEDEC pin out)

PLASTIC PACKAGE

PART NO.	ACCESS TIME (ns)	OPERATING CURRENT MAX.(mA)	STANDBY CURRENT MAX.(μ A)	PACKAGE
MX27C4100PC-12	120	60	100	40 Pin DIP(ROM pin out)
MX27C4100PC-15	150	60	100	40 Pin DIP(ROM pin out)
MX27C4096PC-12	120	60	100	40 Pin DIP(JEDEC pin out)
MX27C4096PC-15	150	60	100	40 Pin DIP(JEDEC pin out)
MX27C4096QC-12	120	60	100	44 Pin PLCC
MX27C4096QC-15	150	60	100	44 Pin PLCC

III. MASK ROM

(MASK PROGRAMMABLE READ ONLY MEMORY)

MX23C1000/MX23C1010

1M-BIT(128K x 8) CMOS MASK ROM

FEATURES

- 131,072 x 8 organization
- Single +5V power supply
- Fast access time: 150/200ns
- Totally static operation
- Completely TTL compatible
- Operating current: 40mA
- Standby current: 100μA
- Package type:
  - 28 pin plastic DIP
  - 32 pin plastic DIP/SOP

DESCRIPTION

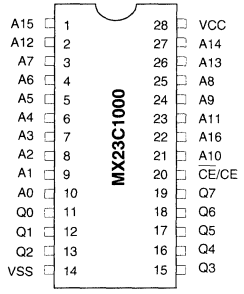
The MX23C1000/1010 is a 5V static CMOS ROM with an access time of 150/200ns and low standby current of 100μA. It has a total of 1M programmable bits arranged as 128K x 8-bit words. It offers a broad range of compatibility to nowaday's high speed and large program storage system designs.

The MX23C1000 is available in 28 pin DIP and MX23C1010 is 32 pin DIP. MX23C1000 pin 20 chip enable (CE/$\overline{CE}$) may be programmabled either active HIGH or LOW. MX23C1000 pin 20 output enable (OE/$\overline{OE}$) may be programmed either active HIGH or LOW.

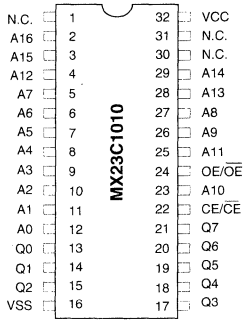
MX23C1010 pin 22 chip enable(CE/$\overline{CE}$) and pin 24(OE/$\overline{OE}$) maybe programmed either active HIGH or LOW.

PIN CONFIGURATIONS

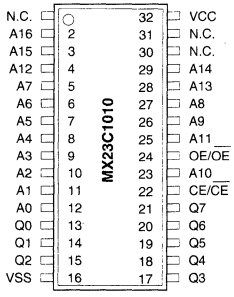
28 PDIP



32 PDIP



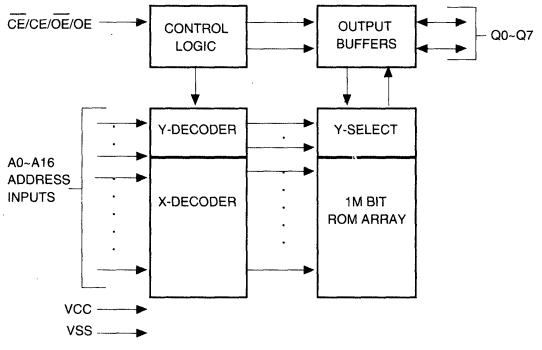
32 SOP



PIN FUNCTIONS

SYMBOL	PIN NAME
A0~A16	Address Input
Q0~Q7	Data Output
CE/$\overline{CE}$	Chip Enable Input
OE/$\overline{OE}$	Output Enable Input
VCC	Power Supply Pin(+5V)
VSS	Ground Pin

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

RATING	VALUE
Ambient Operating Temperature	0°C to 70°C
Storage Temperature	-65°C to 125°C
Applied Input Voltage	-0.5V to VCC + 0.5V
Applied Output Voltage	-0.5V to VCC + 0.5V
VCC to Ground Potential	-0.5V to 7.0V
Power Dissipation	0.5W

***NOTICE:**
Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended period may affect reliability.

DC CHARACTERISTICS TA = 0°C TO 70°C, VCC = 5V ± 10%

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
VOH	Output High Voltage	2.4		V	IOH = -1.0mA
VOL	Output Low Voltage		0.4	V	IOL = 2.1mA
VIH	Input High Voltage	2.2	VCC + 0.3	V	
VIL	Input Low Voltage	-0.3	0.8	V	
ILI	Input Leakage Current		10	µA	VIN = 0 to 5.5V
ILO	Output Leakage Current		10	µA	VOUT = 0 to 5.5V
ICC3	Power-Down Supply Current		100	µA	$\overline{CE}$ > VCC - 0.2V
ICC2	Standby Supply Current		1	mA	$\overline{CE}$ = VIH
ICC1	Operating Supply Current		40	mA	Note 1

CAPACITANCE TA = 25°C, f = 1.0 MHz (Note 2)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONTITIONS
CIN	Input Capacitance		10	pF	VIN = 0V
COUT	Output Capacitance		10	pF	VOUT = 0V

AC CHARACTERISTICS TA = 0°C to 70°C, VCC = 5V ± 10%

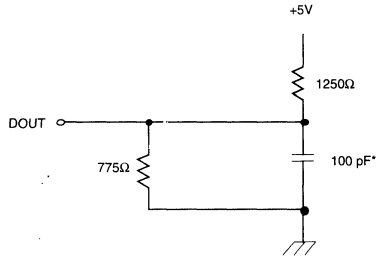
		23C1000/1010-15		23C1000/1010-20			
SYMBOL	PARAMETER	MIN.	MAX.	MIN.	MAX.	UNIT	CONDITIONS
tCYC	Cycle Time	150		200		ns	
tAA	Address Access Time		150		200	ns	
tOH	Output Hold Time After Address Change	10		10		ns	
tACE	Chip Enable Access Time		150		200	ns	
tAOE	Output Enable/Chip Select Access Time		80		100	ns	
tLZ	Output Low Z Delay	0		0		ns	Note 3
tHZ	Output High Z Delay		70		70	ns	Note 4

NOTE:
1. Measured with device selected at f = 5 MHz and output unloaded.
2. This parameter is periodically sampled and is not 100% tested.
3. Output low-impedance delay (tLZ) is measured from $\overline{CE}$ going low.
4. Output high-impedance delay (tHZ) is measured from $\overline{CE}$ going high.

AC TEST CONDITIONS

Input Pulse Levels	0.4V to 2.4V
Input Rise and Fall Times	10ns
Input Timing Level	1.5V
Output Timing Level	0.8V and 2.0V
Output Load	See Figure 1

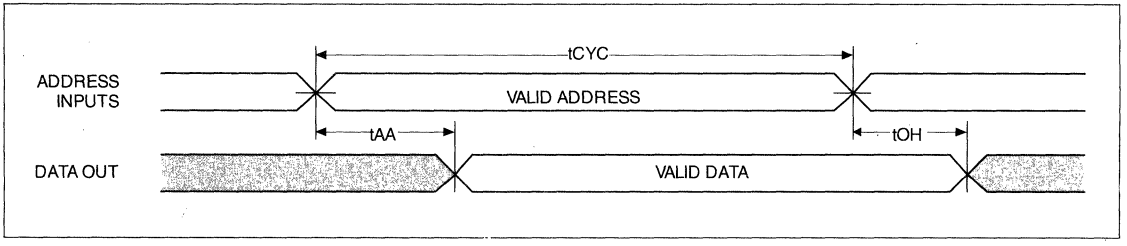
FIGURE 1. OUTPUT LOAD CIRCUIT



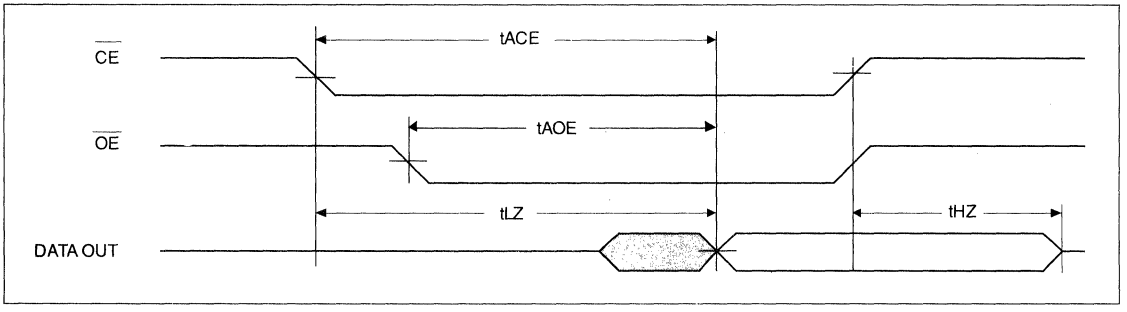
* Including scope and jig.

WAVEFORMS

PROPAGATION DELAY FROM ADDRESS ($\overline{CE}$/$\overline{OE}$ = ACTIVE)



PROPAGATION DELAY FROM CHIP ENABLE (ADDRESS VALID)



ORDERING INFORMATION

PART NO.	ACCESS TIME(ns)	OPERATING CURRENT MAX.(mA)	STANDBY CURRENT MAX.(μA)	PACKAGE
MX23C1000PC-15	150	40	100	28 Pin DIP
MX23C1010PC-15	150	40	100	32 Pin DIP
MX23C1000MC-15	150	40	100	28 Pin SOP
MX23C1010MC-15	150	40	100	32 Pin SOP
MX23C1000PC-20	200	40	100	28 Pin DIP
MX23C1010PC-20	200	40	100	32 Pin DIP
MX23C1000MC-20	200	40	100	28 Pin SOP
MX23C1010MC-20	200	40	100	32 Pin SOP

MX23C2000

2M-BIT(256K x 8) CMOS MASK ROM

FEATURES

- 256K x 8 organization
- Single +5V power supply
- Fast access time: 150/200ns (max)
- Totally static operation
- Completely TTL compatible
- Operating current: 40mA
- Standby current: 100μ A
- Package type:
  - 32 pin plastic DIP
  - 32 pin plastic SOP

GENERAL DESCRIPTION

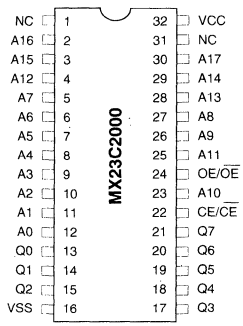
The MX23C2000 is a 5V only, 2M-bit, Read Only Memory. It is organized as 256K words by 8 bit, operates from a single +5 volt supply, has a static standby mode, and has an access time of 150/200ns. It is designed to be compatible with all microprocessors and similar applications in which high performance, large bit storage and simple interfacing are important design considerations.

The MX23C2000 offers automatic power-down, with power-down controlled by the chip enable($\overline{CE}$) Input. When $\overline{CE}$ goes high, the device automatically powers down and remains in a low-power standby mode as long as $\overline{CE}$ remains high.

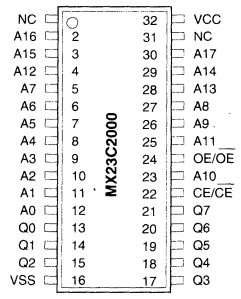
MX23C2000 pin 24 may also be programmed either active HIGH or LOW in order to eliminate bus contention in multiple-bus microprocessor systems.

PIN CONFIGURATIONS

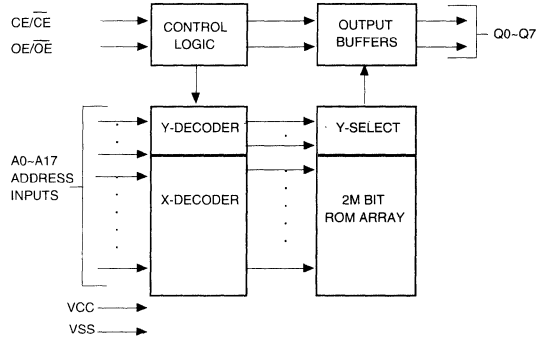
32 PDIP



32 SOP



BLOCK DIAGRAM



PIN DESCRIPTION:

SYMBOL	PIN NAME
A0~A17	Address Input
Q0~Q7	Data Output
CE/$\overline{CE}$	Chip Enable Input
OE/$\overline{OE}$	Output Enable Input
VCC	Power Supply Pin (+5V)
VSS	Ground Pin

ABSOLUTE MAXIMUM RATINGS*

RATING	VALUE
Ambient Operating Temperature	0°C to 70°C
Storage Temperature	-65°C to 125°C
Applied Input Voltage	-0.5V to VCC + 0.5V
Applied Output Voltage	-0.5V to VCC + 0.5V
VCC to Ground Potential	-0.5V to 7.0V
Power Dissipation	1.0W

***NOTICE:**
Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended period may affect reliability.

DC CHARACTERISTICS TA = 0°C TO 70°C, VCC = 5V ± 10%

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
VOH	Output High Voltage	2.4		V	IOH = -1.0mA
VOL	Output Low Voltage		0.4	V	IOL = 2.1mA
VIH	Input High Voltage	2.2	VCC + 0.3	V	
VIL	Input Low Voltage	-0.3	0.8	V	
ILI	Input Leakage Current		10	µA	VIN = 0 to 5.5V
ILO	Output Leakage Current		10	µA	VOUT = 0 to 5.5V
ICC3	Power-Down Supply Current		100	µA	$\overline{CE}$ > VCC - 0.2V
ICC2	Standby Supply Current		1.0	mA	$\overline{CE}$ = VIH
ICC1	Operating Supply Current		40	mA	Note 1

CAPACITANCE TA = 25°C, f = 1.0 MHz (Note 2)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
CIN	Input Capacitance		10	pF	VIN = 0V
COUT	Output Capacitance		10	pF	VOUT = 0V

AC CHARACTERISTICS TA = 0°C to 70°C, VCC = 5V ± 10%

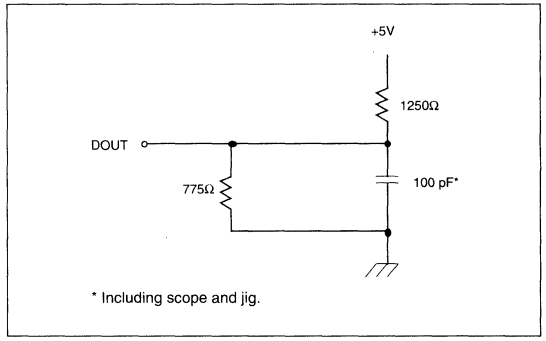
		23C2000-15		23C2000-20			
SYMBOL	PARAMETER	MIN.	MAX.	MIN.	MAX.	UNIT	CONDITIONS
tCYC	Cycle Time	150		200		ns	
tAA	Address Access Time		150		200	ns	
tOH	Output Hold Time After Address Change	10		10		ns	
tACE	Chip Enable Access Time		150		200	ns	
tAOE	Output Enable/Chip Select Access Time		80		100	ns	
tLZ	Output Low Z Delay	0		0		ns	Note 3
tHZ	Output High Z Delay		70		70	ns	Note 4

NOTE:
1. Measured with device selected at f = 5 MHz and output unloaded.
2. This parameter is periodically sampled and is not 100% tested.
3. Output low-impedance delay (tLZ) is measured from $\overline{CE}$ going low.
4. Output high-impedance delay (tHZ) is measured from $\overline{CE}$ going high.

AC TEST CONDITIONS

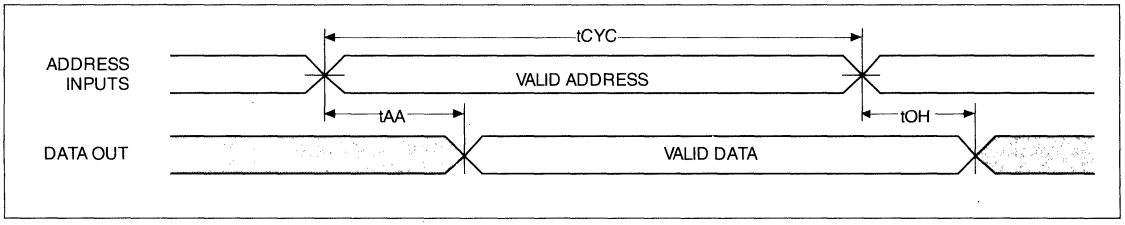
Input Pulse Levels	0.4V to 2.4V
Input Rise and Fall Times	10ns
Input Timing Level	1.5V
Output Timing Level	0.8V and 2.0V
Output Load	See Figure 1

FIG 1. OUTPUT LOAD CIRCUIT

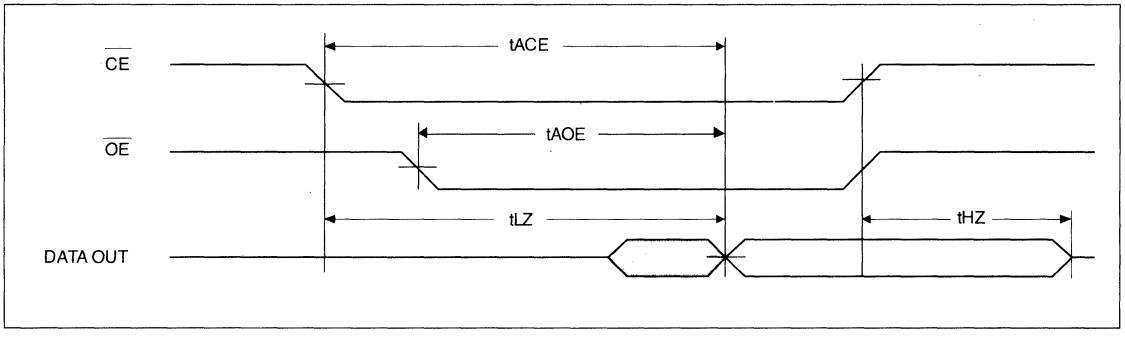


WAVEFORMS

PROPAGATION DELAY FROM ADDRESS ($\overline{CE}$/$\overline{OE}$ = ACTIVE)



PROPAGATION DELAY FROM CHIP ENABLE (ADDRESS VALID)



ORDERING INFORMATION

PART NO.	ACCESS TIME(ns)	OPERATING CURRENT MAX.(mA)	STANDBY CURRENT MAX.(μA)	PACKAGE
MX23C2000PC-15	150	40	100	32 Pin DIP
MX23C2000MC-15	150	40	100	32 Pin SOP
MX23C2000PC-20	200	40	100	32 Pin DIP
MX23C2000MC-20	200	40	100	32 Pin SOP

MX23C2100

2M-BIT(256K x 8/128K x 16) CMOS MASK ROM

FEATURES

- Switchable organization
  - 256K x 8(byte mode)
  - 128K x 16(word mode)
- Single +5V power supply
- Fast access time: 150/200ns
- Totally static operation
- Completely TTL compatible
- Operating current: 60mA
- Standby current: 100μ A
- Package
  - 40 pin DIP(600 mil)

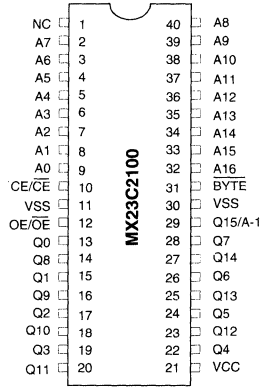
GENERAL DESCRIPTION

The MX23C2100 is a 5V only, 2M-bit, Read Only Memory. It is organized as 256Kx 8 bits (byte mode) or as 128Kx16 bit (word mode) depending on BYTE (pin 31) voltage level. MX23C2100 has a static standby mode, and has an access time of 150/200ns. It is designed to be compatible with all microprocessors and similar applications in which high performance, large bit storage and simple interfacing are important design considerations.

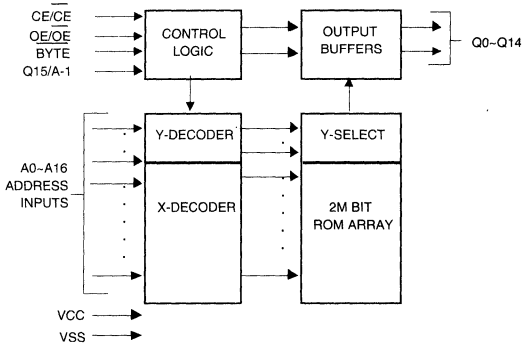
MX23C2100 offers automatic power-down, with power-down controlled by the chip enable(CE/$\overline{CE}$) Input. When CE/$\overline{CE}$ is not selected, the device automatically powers down and remains in a low-power standby mode as long as CE/$\overline{CE}$ stays in the unselected mode.

The OE/$\overline{OE}$ inputs as well as CE/$\overline{CE}$ input may be programmed either active High or Low.

PIN CONFIGURATIONS



BLOCK DIAGRAM



PIN DESCRIPTION:

SYMBOL	PIN NAME
A0~A16	Address Input
Q0~Q14	Data Output
CE/$\overline{CE}$	Chip Enable Input
OE/$\overline{OE}$	Output Enable Input
$\overline{BYTE}$	Word/Byte Selection
Q15/A-1	Q15(Word mode)/LSB addr. (Byte mode)
VCC	Power Supply Pin (+5V)
VSS	Ground Pin

TRUTH TABLE OF $\overline{BYTE}$ FUNCTION

BYTE MODE($\overline{BYTE}$ = VSS)

$\overline{CE}$	OE/$\overline{OE}$	D15/A-1	MODE	D0-D7	SUPPLY CURRENT	NOTE
H	X	X	Non selected	High Z	Standby(ICC2)	1
L	L/H	X	Non selected	High Z	Operating(ICC1)	1
L	H/L	A-1 input	Selected	DOUT	Operating(ICC1)	1

WORD MODE($\overline{BYTE}$ = VCC)

$\overline{CE}$	OE/$\overline{OE}$	D15/A-1	MODE	D0-D14	SUPPLY CURRENT	NOTE
H	X	High Z	Non selected	High Z	Standby(ICC2)	1
L	L/H	High Z	Non selected	High Z	Operating(ICC1)	1
L	H/L	DOUT	Selected	DOUT	Operating(ICC1)	1

NOTE1: X = H or L

ABSOLUTE MAXIMUM RATINGS*

RATING	VALUE
Ambient Operating Temperature	0°C to 70°C
Storage Temperature	-65°C to 125°C
Applied Input Voltage	-0.5V to 7.0V
Applied Output Voltage	-0.5V to 7.0V
VCC to Ground Potential	-0.5V to 7.0V
Power Dissipation	1.0W

***NOTICE:**
Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended period may affect reliability.

DC CHARACTERISTICS TA = 0°C TO 70°C, VCC = 5V ± 10%

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
VOH	Output High Voltage	2.4		V	IOH = -1.0mA
VOL	Output Low Voltage		0.4	V	IOL = 2.1mA
VIH	Input High Voltage	2.2	VCC + 0.3	V	
VIL	Input Low Voltage	-0.3	0.8	V	
ILI	Input Leakage Current		10	µA	VIN = 0 to 5.5V
ILO	Output Leakage Current		10	µA	VOUT = 0 to 5.5V
ICC3	Power-Down Supply Current		100	µA	$\overline{CE}$ > VCC - 0.2V
ICC2	Standby Supply Current		1.0	mA	$\overline{CE}$ = VIH
ICC1	Operating Supply Current		60	mA	Note 1

CAPACITANCE TA = 25°C, f = 1.0 MHz (Note 2)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
CIN	Input Capacitance		10	pF	VIN = 0V
COUT	Output Capacitance		10	pF	VOUT = 0V

AC CHARACTERISTICS: TA = 0°C to 70°C, VCC = 5V ± 10%

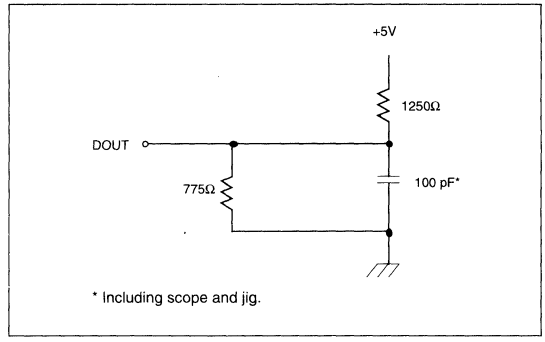
		23C2100-15		23C2100-20			
SYMBOL	PARAMETER	MIN.	MAX.	MIN.	MAX.	UNIT	CONDITIONS
tCYC	Cycle Time	150		200		ns	
tAA	Address Access Time		150		200	ns	
tOH	Output Hold Time After Address Change	10		10		ns	
tACE	Chip Enable Access Time		150		200	ns	
tAOE	Output Enable/Chip Select Access Time		80		90	ns	
tLZ	Output Low Z Delay	0		0		ns	Note 3
tHZ	Output High Z Delay		70		70	ns	Note 4
tBHA	$\overline{BYTE}$ Access Time		150		200	ns	
tOHB	$\overline{BYTE}$ Output Hold Time	0		0		ns	
tBHZ	$\overline{BYTE}$ Output Delay Time		70		70	ns	
tBLZ	$\overline{BYTE}$ Output Set Time	10		10		ns	

NOTE:
1. Measured with device selected at f = 5 MHz and output unloaded.
2. Tnis parameter is periodically sampled and is not 100% tested.
3. Output low-impedance delay (tLZ) is measured from CE going low.
4. Output high-impedance delay (tHZ) is measured from CE going high.

AC TEST CONDITIONS

Input Pulse Levels	0.4V to 2.4V
Input Rise and Fall Times	10ns
Input Timing Level	1.5V
Output Timing Level	0.8V and 2.0V
Output Load	See Figure 1

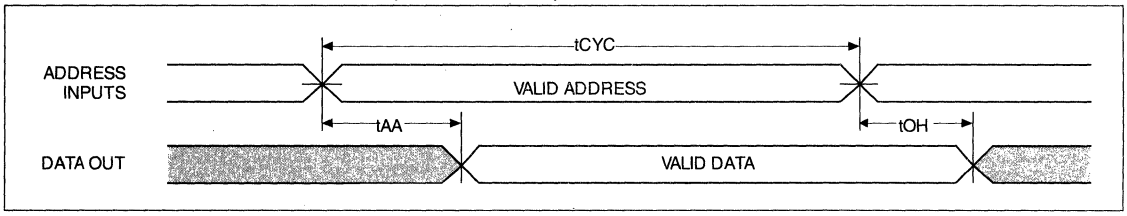
FIG. 1 OUTPUT LOAD CIRCUIT



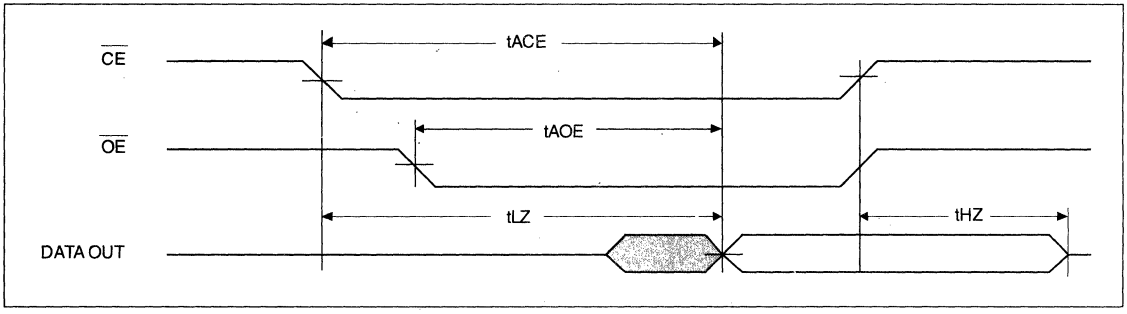
MASK ROM DATA SHEETS

WAVEFORMS

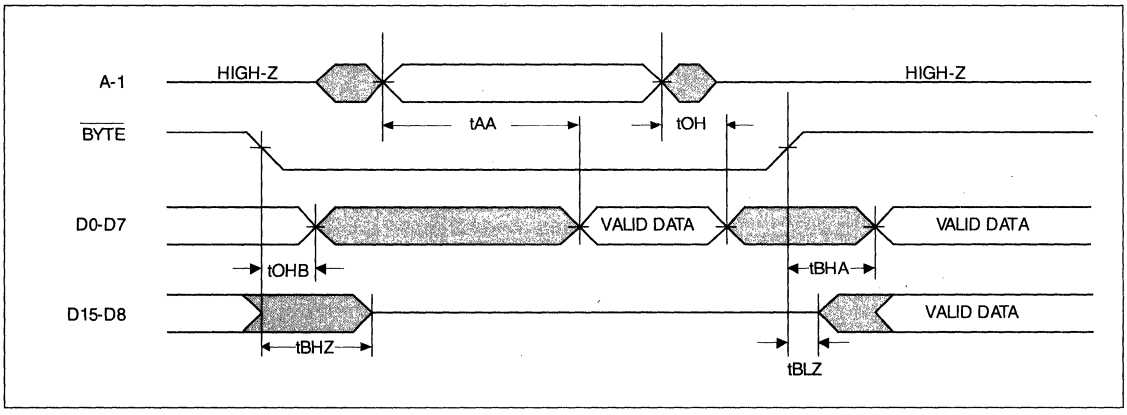
PROPAGATION DELAY FROM ADDRESS ($\overline{CE}$/$\overline{OE}$ = ACTIVE)



PROPAGATION DELAY FROM CHIP ENABLE (ADDRESS VALID)



PROPAGATION DELAY FROM CHIP ENABLE (ADDRESS VALID)



ORDERING INFORMATION

PART NO.	ACCESS TIME(ns)	OPERATING CURRENT MAX.(mA)	STANDBY CURRENT MAX.(μA)	PACKAGE
MX23C2100PC-15	150	60	100	40 Pin DIP
MX23C2100PC-20	200	60	100	40 Pin DIP

FEATURES

- 512K x 8 organization
- Single +5V power supply
- Fast access time: 120/150/200ns (max)
- Totally static operation
- Completely TTL compatible
- Operating current: 40mA
- Standby current: 100μ A
- Package type:
  - 32 pin plastic DIP
  - 32 pin plastic SOP

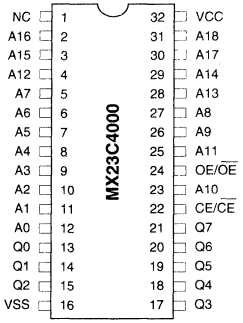
GENERAL DESCRIPTION

The MX23C4000 is a 5V only, 4M-bit, Read Only Memory. It is organized as 512K words by 8 bit, operates from a single +5 volt supply, has a static standby mode, and has an access time of 120/150/200ns. It is designed to be compatible with all microprocessors and similar applications in which high performance, large bit storage and simple interfacing are important design considerations. The MX23C4000 offers automatic power-down, with power-down controlled by the chip enable($\overline{CE}$) Input. When $\overline{CE}$ goes high, the device automatically powers down and remains in a low-power standby mode as long as $\overline{CE}$ remains high.

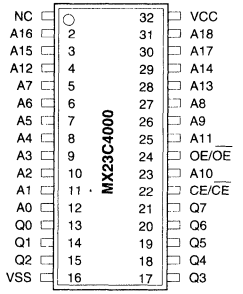
MX23C4000 pin 24 may also be programmed either active HIGH or LOW in order to eliminate bus contention in multiple-bus microprocessor systems.

PIN CONFIGURATIONS

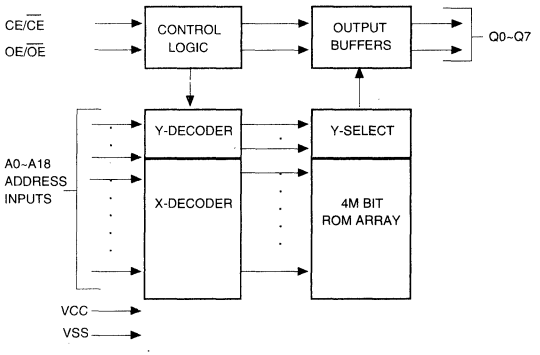
32 PDOP



32 PSOP



BLOCK DIAGRAM



PIN DESCRIPTION:

SYMBOL	PIN NAME
A0~A18	Address Input
Q0~Q7	Data Output
CE/$\overline{CE}$	Chip Enable Input
OE/$\overline{OE}$	Output Enable Input
VCC	Power Supply Pin (+5V)
VSS	Ground Pin

ABSOLUTE MAXIMUM RATINGS*

RATING	VALUE
Ambient Operating Temperature	0°C to 70°C
Storage Temperature	-65°C to 125°C
Applied Input Voltage	-0.5V to VCC + 0.5
Applied Output Voltage	-0.5V to VCC + 0.5
VCC to Ground Potential	-0.5V to 7.0V
Power Dissipation	1.0W

***NOTICE:**
Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended period may affect reliability.

DC CHARACTERISTICS TA = 0°C TO 70°C, VCC = 5V ± 10%

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
VOH	Output High Voltage	2.4		V	IOH = -1.0mA
VOL	Output Low Voltage		0.4	V	IOL = 2.1mA
VIH	Input High Voltage	2.2	VCC + 0.3	V	
VIL	Input Low Voltage	-0.3	0.8	V	
ILI	Input Leakage Current		10	µA	VIN = 0 to 5.5V
ILO	Output Leakage Current		10	µA	VOUT = 0 to 5.5V
ICC3	Power-Down Supply Current		100	µA	$\overline{CE}$ > VCC - 0.2V
ICC2	Standby Supply Current		1.0	mA	$\overline{CE}$ = VIH
ICC1	Operating Supply Current		40	mA	Note 1

CAPACITANCE TA = 25°C, f = 1.0 MHz (Note 2)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
CIN	Input Capacitance		10	pF	VIN = 0V
COUT	Output Capacitance		10	pF	VOUT = 0V

AC CHARACTERISTICS TA = 0°C to 70°C, VCC = 5V ± 10%

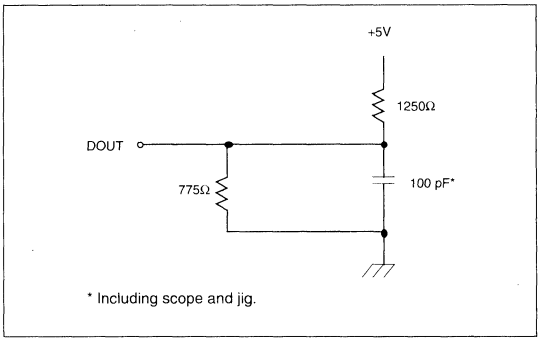
		23C4000-12		23C4000-15		23C4000-20			
SYMBOL	PARAMETER	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	UNIT	CONDITIONS
tCYC	Cycle Time	120		150		200		ns	
tAA	Address Access Time		120		150		200	ns	
tOH	Output Hold Time After Address Change	10		10		10		ns	
tACE	Chip Enable Access Time		120		150		200	ns	
tAOE	Output Enable/Chip Select Access Time		80		80		100	ns	
tLZ	Output Low Z Delay	0		0		0		ns	Note 3
tHZ	Output High Z Delay		70		70		70	ns	Note 4

NOTE:
1. Measured with device selected at f = 5 MHz and output unloaded.
2. This parameter is periodically sampled and is not 100% tested.
3. Output low-impedance delay (tLZ) is measured from $\overline{CE}$ going low.
4. Output high-impedance delay (tHZ) is measured from $\overline{CE}$ going high.

AC TEST CONDITIONS

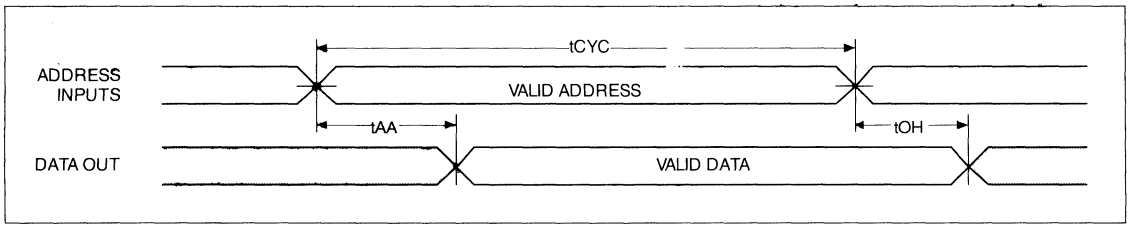
Input Pulse Levels	0.4V to 2.4V
Input Rise and Fall Times	10ns
Input Timing Level	1.5V
Output Timing Level	0.8V and 2.0V
Output Load	See Figure 1

FIG 1. OUTPUT LOAD CIRCUIT

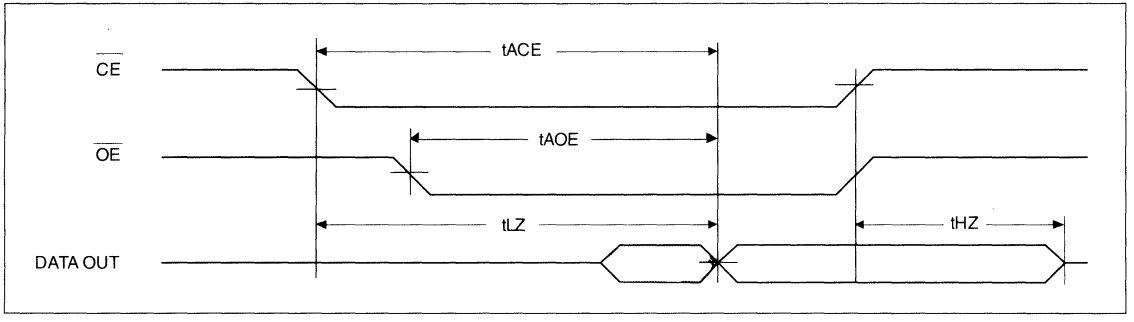


WAVEFORMS

PROPAGATION DELAY FROM ADDRESS ($\overline{CE}$/$\overline{OE}$ = ADDRESS)



PROPAGATION DELAY FROM CHIP ENABLE (ADDRESS VALID)



ORDERING INFORMATION

PART NO.	ACCESS TIME(ns)	OPERATING CURRENT MAX.(mA)	STANDBY CURRENT MAX.(μA)	PACKAGE
MX23C4000PC-12	120	40	100	32 Pin DIP
MX23C4000MC-12	120	40	100	32 Pin SOP
MX23C4000PC-15	150	40	100	32 Pin DIP
MX23C4000MC-15	150	40	100	32 Pin SOP
MX23C4000PC-20	200	40	100	32 Pin DIP
MX23C4000MC-20	200	40	100	32 Pin SOP

MX23C4100

4M-BIT(512K x 8/256K x 16) CMOS MASK ROM

FEATURES

- Switchable configuration
  - 512K x 8(byte mode)
  - 256K x 16(word mode)
- Single +5V power supply
- Fast access time: 120/150/200ns
- Totally static operation
- Completely TTL compatible
- Operating current: 60mA
- Standby current: 100μ A
- Package
  - 40 pin DIP(600 mil)

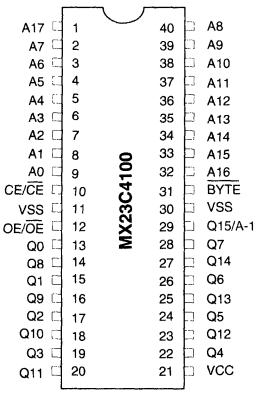
GENERAL DESCRIPTION

The MX23C4100 is a 5V only, 4M-bit, Read Only Memory. It is organized as 512K x 8 bits (byte mode) or as 256K x16 bit (word mode) depending on $\overline{BYTE}$ (pin 31) voltage level. MX23C4100 has a static standby mode, and has an access time of 120/150/200ns. It is designed to be compatible with all microprocessors and similar applications in which high performance, large bit storage and simple interfacing are important design considerations.

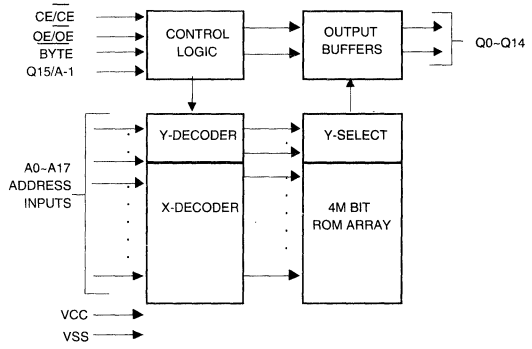
MX23C4100 offers automatic power-down, with power-down controlled by the chip enable($CE/\overline{CE}$) Input. When $CE/\overline{CE}$ is not selected, the device automatically powers down and remains in a low-power standby mode as long as $CE/\overline{CE}$ stays in the unselected mode.

The $OE/\overline{OE}$ inputs as well as $CE/\overline{CE}$ input may be programmed either active High or Low.

PIN CONFIGURATIONS



BLOCK DIAGRAM



PIN DESCRIPTION:

SYMBOL	PIN NAME
A0~A17	Address Input
Q0~Q14	Data Output
$CE/\overline{CE}$	Chip Enable Input
$OE/\overline{OE}$	Output Enable Input
$\overline{BYTE}$	Word/Byte Selection
Q15/A-1	Q15(Word mode)/LSB addr. (Byte mode)
VCC	Power Supply Pin (+5V)
VSS	Ground Pin

TRUTH TABLE OF $\overline{BYTE}$ FUNCTION

BYTE MODE($\overline{BYTE}$ = VSS)

$\overline{CE}$	OE/$\overline{OE}$	D15/A-1	MODE	D0-D7	SUPPLY CURRENT	NOTE
H	X	X	Non selected	High Z	Standby(ICC2)	1
L	L/H	X	Non selected	High Z	Operating(ICC1)	1
L	H/L	A-1 input	Selected	DOUT	Operating(ICC1)	1

WORD MODE($\overline{BYTE}$ = VCC)

$\overline{CE}$	OE/$\overline{OE}$	D15/A-1	MODE	D0-D14	SUPPLY CURRENT	NOTE
H	X	High Z	Non selected	High Z	Standby(ICC2)	1
L	L/H	High Z	Non selected	High Z	Operating(ICC1)	1
L	H/L	DOUT	Selected	DOUT	Operating(ICC1)	1

NOTE1: X = H or L

ABSOLUTE MAXIMUM RATINGS*

RATING	VALUE
Ambient Operating Temperature	0°C to 70°C
Storage Temperature	-65°C to 125°C
Applied Input Voltage	-0.5V to 7.0V
Applied Output Voltage	-0.5V to 7.0V
VCC to Ground Potential	-0.5V to 7.0V
Power Dissipation	1.0W

***NOTICE:**
Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended period may affect reliability.

DC CHARACTERISTICS TA = 0°C TO 70°C, VCC = 5V ± 10%

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
VOH	Output High Voltage	2.4		V	IOH = -1.0mA
VOL	Output Low Voltage		0.4	V	IOL = 2.1mA
VIH	Input High Voltage	2.2	VCC + 0.3	V	
VIL	Input Low Voltage	-0.3	0.8	V	
ILI	Input Leakage Current		10	µA	VIN = 0 to 5.5V
ILO	Output Leakage Current		10	µA	VOUT = 0 to 5.5V
ICC3	Power-Down Supply Current		100	µA	$\overline{CE}$ > VCC - 0.2V
ICC2	Standby Supply Current		1.0	mA	$\overline{CE}$ = VIH
ICC1	Operating Supply Current		60	mA	Note 1

CAPACITANCE TA = 25°C, f = 1.0 MHz (Note 2)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
CIN	Input Capacitance		10	pF	VIN = 0V
COUT	Output Capacitance		10	pF	VOUT = 0V

AC CHARACTERISTICS: TA = 0°C to 70°C, VCC = 5V ± 10%

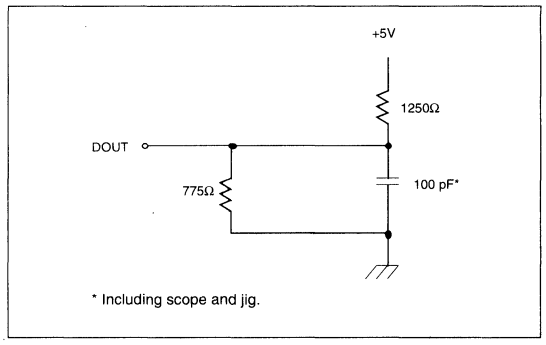
		23C4100-12		23C4100-15		23C4100-20			
SYMBOL	PARAMETER	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	UNIT	CONDITIONS
tCYC	Cycle Time	120		150		200		ns	
tAA	Address Access Time		120		150		200	ns	
tOH	Output Hold Time After Address Change	10		10		10		ns	
tACE	Chip Enable Access Time		120		150		200	ns	
tAOE	Output Enable/Chip Select Access Time		70		80		90	ns	
tLZ	Output Low Z Delay	0		0		0		ns	Note 3
tHZ	Output High Z Delay		70		70		70	ns	Note 4
tBHA	$\overline{BYTE}$ Access Time		120		150		200	ns	
tOHB	$\overline{BYTE}$ Output Hold Time	0		0		0		ns	
tBHZ	$\overline{BYTE}$ Output Delay Time		70		70		70	ns	
tBLZ	$\overline{BYTE}$ Output Set Time	10		10		10		ns	

NOTE:
1. Measured with device selected at f = 5 MHz and output unloaded.
2. This parameter is periodically sampled and is not 100% tested.
3. Output low-impedance delay (tLZ) is measured from CE going low.
4. Output high-impedance delay (tHZ) is measured from CE going high.

AC TEST CONDITIONS

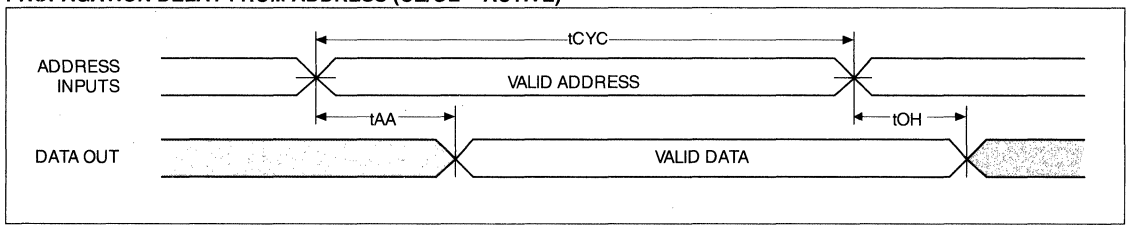
Input Pulse Levels	0.4V to 2.4V
Input Rise and Fall Times	10ns
Input Timing Level	1.5V
Output Timing Level	0.8V and 2.0V
Output Load	See Figure 1

FIG. 1 OUTPUT LOAD CIRCUIT

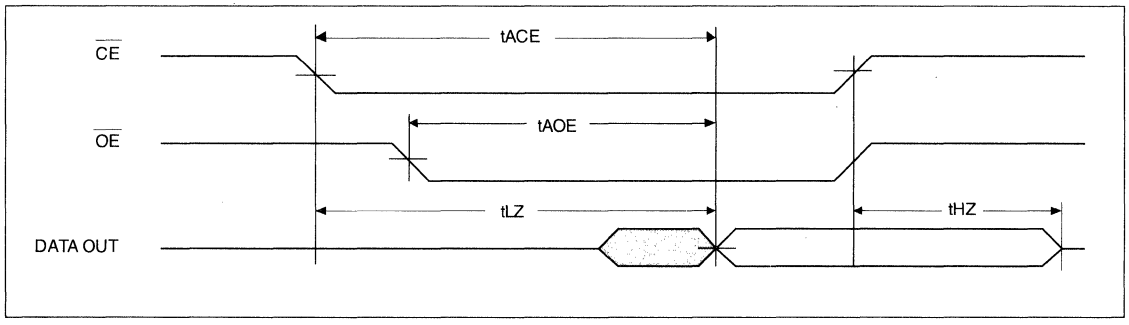


WAVEFORMS

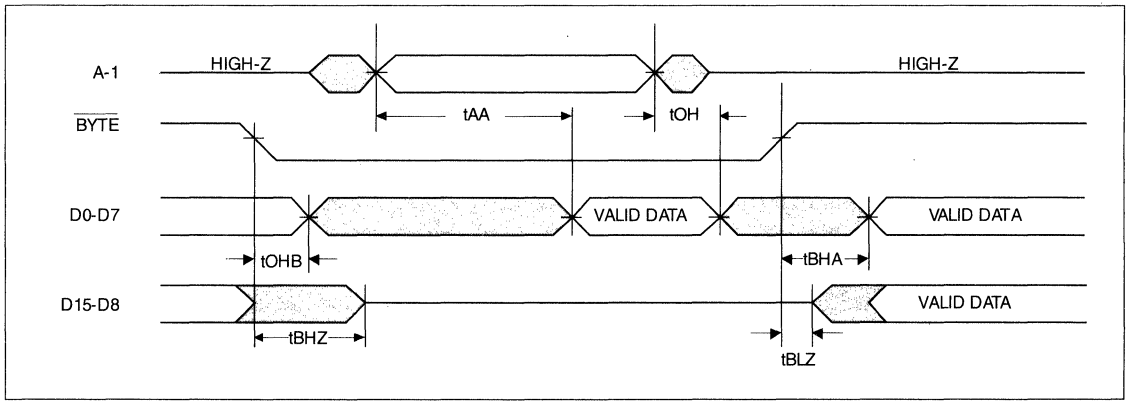
PROPAGATION DELAY FROM ADDRESS ($\overline{CE}$/$\overline{OE}$ = ACTIVE)



PROPAGATION DELAY FROM CHIP ENABLE (ADDRESS VALID)



PROPAGATION DELAY FROM CHIP ENABLE (ADDRESS VALID)



ORDERING INFORMATION

PART NO.	ACCESS TIME(ns)	OPERATING CURRENT MAX.(mA)	STANDBY CURRENT MAX.(μA)	PACKAGE
MX23C4100PC-12	120	60	100	40 Pin DIP
MX23C4100PC-15	150	60	100	40 Pin DIP
MX23C4100PC-20	200	60	100	40 Pin DIP

MX23C8000

8M-BIT(1M x 8) CMOS MASK ROM

FEATURES

- 1M x 8 organization
- Single +5V power supply
- Fast access time: 120/150/200ns (max)
- Totally static operation
- Completely TTL compatible
- Operating current: 40mA
- Standby current: 100μ A
- Package type:
  - 32 pin plastic DIP
  - 32 pin plastic SOP

GENERAL DESCRIPTION

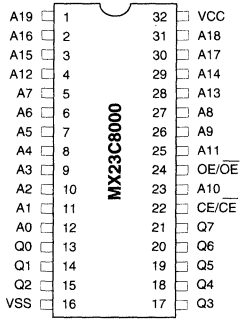
The MX23C8000 is a 5V only, 8M-bit, Read Only Memory. It is organized as 1M words by 8 bit, operates from a single +5 volt supply, has a static standby mode, and has an access time of 120/150/200ns. It is designed to be compatible with all microprocessors and similar applications in which high performance, large bit storage and simple interfacing are important design considerations.

The MX23C8000 offers automatic power-down, with power-down controlled by the chip enable($\overline{CE}$) Input. When $\overline{CE}$ goes high, the device automatically powers down and remains in a low-power standby mode as long as $\overline{CE}$ remains high.

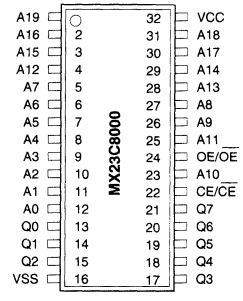
MX23C8000 pin 24 may also be programmed either active HIGH or LOW in order to eliminate bus contention in multiple-bus microprocessor systems.

PIN CONFIGURATIONS

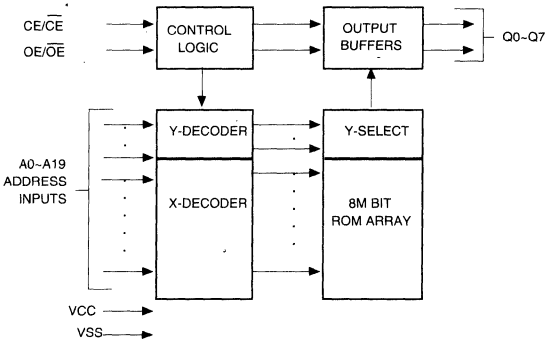
32 PDIP



32 SOP



BLOCK DIAGRAM



PIN DESCRIPTION:

SYMBOL	PIN NAME
A0~A19	Address Input
Q0~Q7	Data Output
CE/$\overline{CE}$	Chip Enable Input
OE/$\overline{OE}$	Output Enable Input
VCC	Power Supply Pin (+5V)
VSS	Ground Pin

ABSOLUTE MAXIMUM RATINGS*

RATING	VALUE
Ambient Operating Temperature	0°C to 70°C
Storage Temperature	-65°C to 125°C
Applied Input Voltage	-0.5V to VCC + 0.5
Applied Output Voltage	-0.5V to VCC + 0.5
VCC to Ground Potential	-0.5V to 7.0V
Power Dissipation	1.0W

***NOTICE:**
Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended period may affect reliability.

DC CHARACTERISTICS TA = 0°C TO 70°C, VCC = 5V ± 10%

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
VOH	Output High Voltage	2.4		V	IOH = -1.0mA
VOL	Output Low Voltage		0.4	V	IOL = 2.1mA
VIH	Input High Voltage	2.2	VCC + 0.3	V	
VIL	Input Low Voltage	-0.3	0.8	V	
ILI	Input Leakage Current		10	µA	VIN = 0 to 5.5V
ILO	Output Leakage Current		10	µA	VOUT = 0 to 5.5V
ICC3	Power-Down Supply Current		100	µA	$\overline{CE}$ > VCC - 0.2V
ICC2	Standby Supply Current		1.0	mA	$\overline{CE}$ = VIH
ICC1	Operating Supply Current		40	mA	Note 1

CAPACITANCE TA = 25°C, f = 1.0 MHz (Note 2)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
CIN	Input Capacitance		10	pF	VIN = 0V
COUT	Output Capacitance		10	pF	VOUT = 0V

AC CHARACTERISTICS TA = 0°C to 70°C, VCC = 5V ± 10%

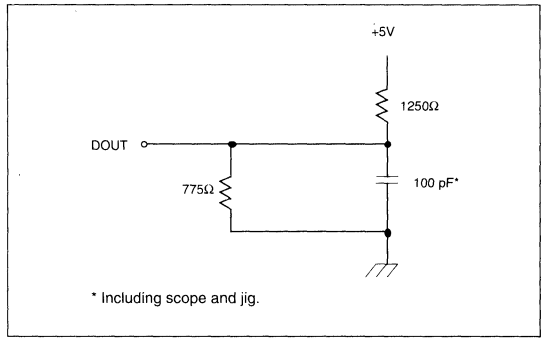
		23C8000-12		23C8000-15		23C8000-20			
SYMBOL	PARAMETER	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	UNIT	CONDITIONS
tCYC	Cycle Time	120		150		200		ns	
tAA	Address Access Time		120		150		200	ns	
tOH	Output Hold Time After Address Change	10		10		10		ns	
tACE	Chip Enable Access Time		120		150		200	ns	
tAOE	Output Enable/Chip Select Access Time		80		80		100	ns	
tLZ	Output Low Z Delay	0		0		0		ns	Note 3
tHZ	Output High Z Delay		70		70		70	ns	Note 4

NOTE:
1. Measured with device selected at f = 5 MHz and output unloaded.
2. This parameter is periodically sampled and is not 100% tested.
3. Output low-impedance delay (tLZ) is measured from $\overline{CE}$ going low.
4. Output high-impedance delay (tHZ) is measured from $\overline{CE}$ going high.

AC TEST CONDITIONS

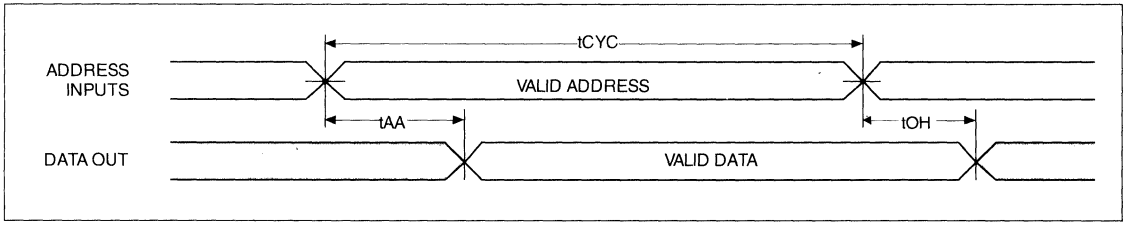
Input Pulse Levels	0.4V to 2.4V
Input Rise and Fall Times	10ns
Input Timing Level	1.5V
Output Timing Level	0.8V and 2.0V
Output Load	See Figure 1

FIG 1. OUTPUT LOAD CIRCUIT

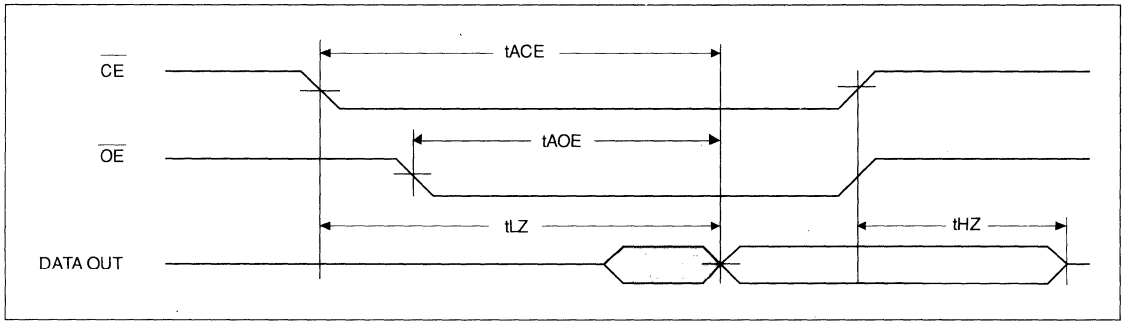


WAVEFORMS

PROPAGATION DELAY FROM ADDRESS ($\overline{CE}$/$\overline{OE}$ = ACTIVE)



PROPAGATION DELAY FROM CHIP ENABLE (ADDRESS VALID)



ORDERING INFORMATION

PART NO.	ACCESS TIME(ns)	OPERATING CURRENT MAX.(mA)	STANDBY CURRENT MAX.(μA)	PACKAGE
MX23C8000PC-12	120	40	100	32 Pin DIP
MX23C8000MC-12	120	40	100	32 Pin SOP
MX23C8000PC-15	150	40	100	32 Pin DIP
MX23C8000MC-15	150	40	100	32 Pin SOP
MX23C8000PC-20	200	40	100	32 Pin DIP
MX23C8000MC-20	200	40	100	32 Pin SOP

MX23C8100

8M-BIT[1M x 8/512K x 16] CMOS MASK ROM

FEATURES

- Switchable configuration
  - 1M x 8(byte mode)
  - 512K x 16(word mode)
- Single +5V power supply
- Fast access time: 120/150/200ns (max)
- Totally static operation
- Completely TTL compatible
- Operating current: 60mA
- Standby current: 100μ A
- Package
  - 42 pin DIP(600 mil)
  - 44 pin SOP(500 mil)

GENERAL DESCRIPTION

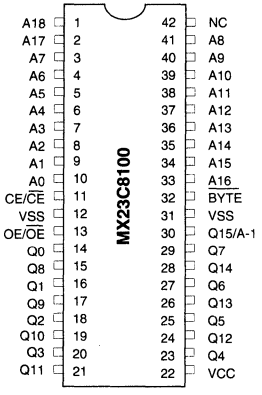
The MX23C8100 is a 5V only, 8M-bit, Read Only Memory. It is organized as 1M x 8 bits (byte mode) or as 512K x 16 bit (word mode) depending on BYTE (pin 32) voltage level. MX23C8100 has a static standby mode, and has an access time of 120/150/200ns. It is designed to be compatible with all microprocessors and similar applications in which high performance, large bit storage and simple interfacing are important design considerations.

MX23C8100 offers automatic power-down, with power-down controlled by the chip enable(CE/$\overline{CE}$) Input. When CE/$\overline{CE}$ is not selected, the device automatically powers down and remains in a low-power standby mode as long as CE/$\overline{CE}$ stays in the unselected mode.

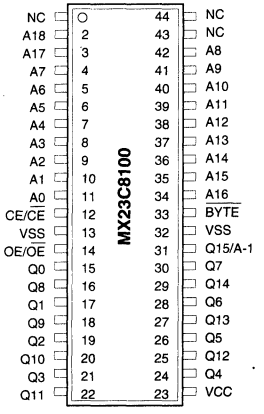
The OE/$\overline{OE}$ inputs as well as CE/$\overline{CE}$ input may be programmed either active High or Low.

PIN CONFIGURATIONS

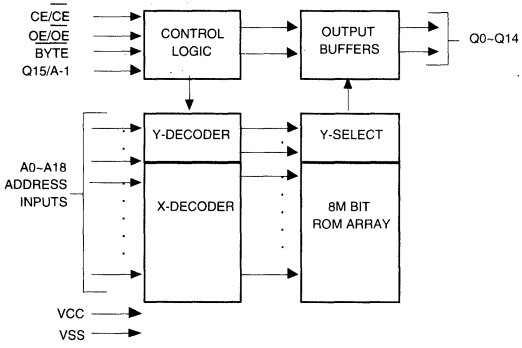
42 PDIP



44 SOP



BLOCK DIAGRAM



PIN DESCRIPTION:

SYMBOL	PIN NAME
A0~A18	Address Input
Q0~Q14	Data Output
CE/$\overline{CE}$	Chip Enable Input
OE/$\overline{OE}$	Output Enable Input
$\overline{BYTE}$	Word/Byte Selection
Q15/A-1	Q15(Word mode)/LSB addr. (Byte mode)
VCC	Power Supply Pin (+5V)
VSS	Ground Pin

TRUTH TABLE OF $\overline{BYTE}$ FUNCTION

BYTE MODE($\overline{BYTE}$ = VSS)

$\overline{CE}$	OE/$\overline{OE}$	D15/A-1	MODE	D0-D7	SUPPLY CURRENT	NOTE
H	X	X	Non selected	High Z	Standby(ICC2)	1
L	L/H	X	Non selected	High Z	Operating(ICC1)	1
L	H/L	A-1 input	Selected	DOUT	Operating(ICC1)	1

WORD MODE($\overline{BYTE}$ = VCC)

$\overline{CE}$	OE/$\overline{OE}$	D15/A-1	MODE	D0-D14	SUPPLY CURRENT	NOTE
H	X	High Z	Non selected	High Z	Standby(ICC2)	1
L	L/H	High Z	Non selected	High Z	Operating(ICC1)	1
L	H/L	DOUT	Selected	DOUT	Operating(ICC1)	1

NOTE1: X = H or L

ABSOLUTE MAXIMUM RATINGS*

RATING	VALUE
Ambient Operating Temperature	0°C to 70°C
Storage Temperature	-65°C to 125°C
Applied Input Voltage	-0.5V to 7.0V
Applied Output Voltage	-0.5V to 7.0V
VCC to Ground Potential	-0.5V to 7.0V
Power Dissipation	1.0W

***NOTICE:**
Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended period may affect reliability.

DC CHARACTERISTICS TA = 0°C TO 70°C, VCC = 5V ± 10%

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
VOH	Output High Voltage	2.4		V	IOH = -1.0mA
VOL	Output Low Voltage		0.4	V	IOL = 2.1mA
VIH	Input High Voltage	2.2	VCC + 0.3	V	
VIL	Input Low Voltage	-0.3	0.8	V	
ILI	Input Leakage Current		10	µA	VIN = 0 to 5.5V
ILO	Output Leakage Current		10	µA	VOUT = 0 to 5.5V
ICC3	Power-Down Supply Current		100	µA	$\overline{CE}$ > VCC - 0.2V
ICC2	Standby Supply Current		1	mA	$\overline{CE}$ = VIH
ICC1	Operating Supply Current		60	mA	Note 1

CAPACITANCE TA = 25°C, f = 1.0 MHz (Note 2)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
CIN	Input Capacitance		10	pF	VIN = 0V
COUT	Output Capacitance		10	pF	VOUT = 0V

AC CHARACTERISTICS: TA = 0°C to 70°C, VCC = 5V ± 10%

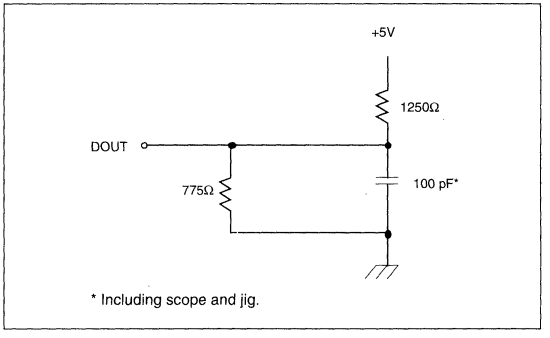
		23C8100-12		23C8100-15		23C8100-20			
SYMBOL	PARAMETER	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	UNIT	CONDITIONS
tCYC	Cycle Time	120		150		200		ns	
tAA	Address Access Time		120		150		200	ns	
tOH	Output Hold Time After Address Change	10		10		10		ns	
tACE	Chip Enable Access Time		120		150		200	ns	
tAOE	Output Enable/Chip Select Access Time		70		80		90	ns	
tLZ	Output Low Z Delay	0		0		0		ns	Note 3
tHZ	Output High Z Delay		70		70		70	ns	Note 4
tBHA	$\overline{\text{BYTE}}$ Access Time		120		150		200	ns	
tOHB	$\overline{\text{BYTE}}$ Output Hold Time	0		0		0		ns	
tBHZ	$\overline{\text{BYTE}}$ Output Delay Time		70		70		70	ns	
tBLZ	$\overline{\text{BYTE}}$ Output Set Time	10		10		10		ns	

NOTE:
1. Measured with device selected at f = 5 MHz and output unloaded.
2. This parameter is periodically sampled and is not 100% tested.
3. Output low-impedance delay (tLZ) is measured from CE going low.
4. Output high-impedance delay (tHZ) is measured from CE going high.

AC TEST CONDITIONS

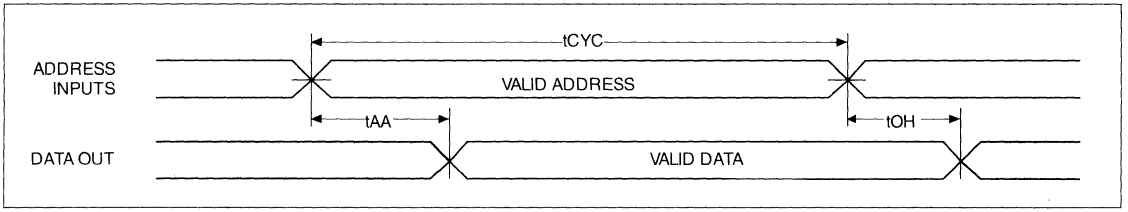
Input Pulse Levels	0.4V to 2.4V
Input Rise and Fall Times	10ns
Input Timing Level	1.5V
Output Timing Level	0.8V and 2.0V
Output Load	See Figure 1

FIG. 1 OUTPUT LOAD CIRCUIT

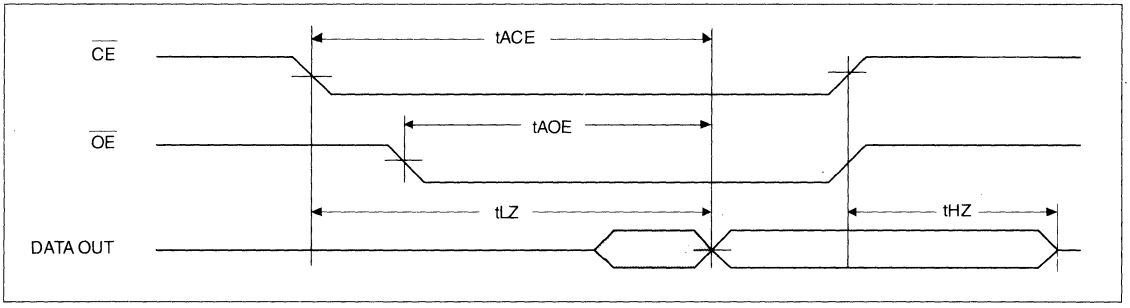


WAVEFORMS

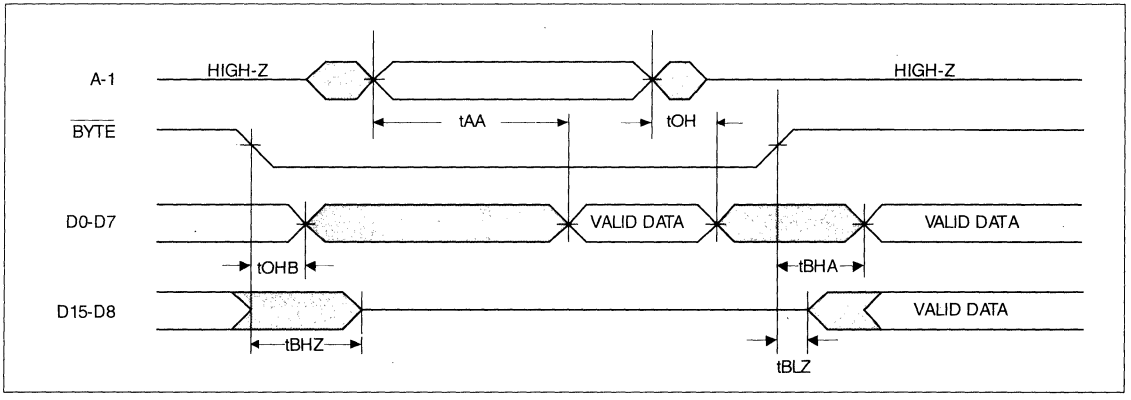
PROPAGATION DELAY FROM ADDRESS ($\overline{CE}$/$\overline{OE}$ = ACTIVE)



PROPAGATION DELAY FROM CHIP ENABLE (ADDRESS VALID)



PROPAGATION DELAY FROM CHIP ENABLE (ADDRESS VALID)



ORDERING INFORMATION

PART NO.	ACCESS TIME(ns)	OPERATING CURRENT MAX.(mA)	STANDBY CURRENT MAX.(μA)	PACKAGE
MX23C8100PC-12	120	60	100	42 Pin DIP
MX23C8100MC-12	120	60	100	44 Pin SOP
MX23C8100PC-15	150	60	100	42 Pin DIP
MX23C8100MC-15	150	60	100	44 Pin SOP
MX23C8100PC-20	200	60	100	42 Pin DIP
MX23C8100MC-20	200	60	100	44 Pin SOP

MX23C1610

16M-BIT(2M x 8/1M x 16) CMOS MASK ROM

FEATURES

- Switchable configuration
  - 2M x 8(byte mode)
  - 1M x 16(word mode)
- Single +5V power supply
- Fast access time: 120/150/200ns (max)
- Totally static operation
- Completely TTL compatible
- Operating current: 60mA
- Standby current: 100μ A
- Package
  - 42 pin DIP (600 mil)
  - 44 pin SOP (500 mil)

GENERAL DESCRIPTION

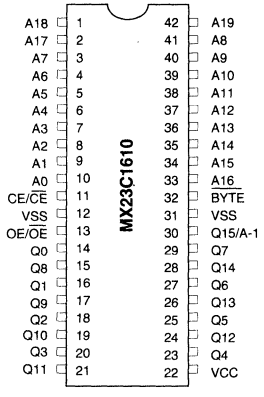
The MX23C1610 is a 5V only, 16M-bit, Read Only Memory. It is organized as 2,097,152 x 8 bits (byte mode) or as 1M x 16 bit (word mode) depending on BYTE (pin 32) voltage level. MX23C1610 has a static standby mode, and has an access time of 120/150/200ns. It is designed to be compatible with all microprocessors and similar applications in which high performance, large bit storage and simple interfacing are important design considerations.

MX23C1610 offers automatic power-down, with power-down controlled by the chip enable(CE/$\overline{CE}$) Input. When CE/$\overline{CE}$ is not selected, the device automatically powers down and remains in a low-power standby mode as long as CE/$\overline{CE}$ stays in the unselected mode.

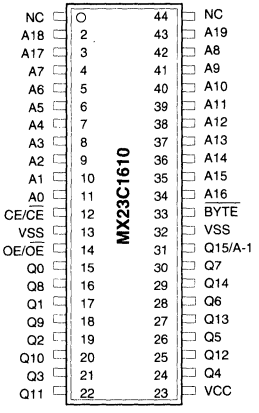
The OE/$\overline{OE}$ inputs as well as CE/$\overline{CE}$ input may be programmed either active High or Low.

PIN CONFIGURATIONS

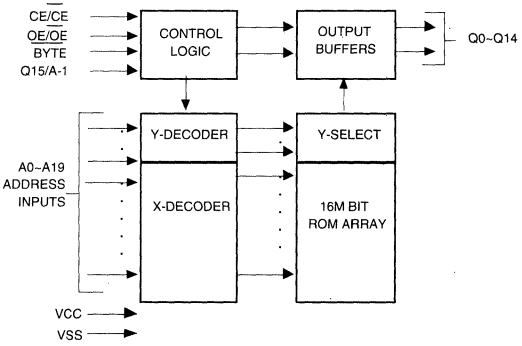
42 PDIP



44 SOP



BLOCK DIAGRAM



PIN DESCRIPTION:

SYMBOL	PIN NAME
A0~A19	Address Input
Q0~Q14	Data Output
CE/$\overline{CE}$	Chip Enable Input
OE/$\overline{OE}$	Output Enable Input
$\overline{BYTE}$	Word/Byte Selection
Q15/A-1	Q15(Word mode)/LSB addr. (Byte mode)
VCC	Power Supply Pin (+5V)
VSS	Ground Pin

TRUTH TABLE OF $\overline{BYTE}$ FUNCTION

BYTE MODE($\overline{BYTE}$ = VSS)

$\overline{CE}$	OE/$\overline{OE}$	D15/A-1	MODE	D0-D7	SUPPLY CURRENT	NOTE
H	X	X	Non selected	High Z	Standby(ICC2)	1
L	L/H	X	Non selected	High Z	Operating(ICC1)	1
L	H/L	A-1 input	Selected	DOUT	Operating(ICC1)	1

WORD MODE($\overline{BYTE}$ = VCC)

$\overline{CE}$	OE/$\overline{OE}$	D15/A-1	MODE	D0-D14	SUPPLY CURRENT	NOTE
H	X	High Z	Non selected	High Z	Standby(ICC2)	1
L	L/H	High Z	Non selected	High Z	Operating(ICC1)	1
L	H/L	DOUT	Selected	DOUT	Operating(ICC1)	1

NOTE1: X = H or L

ABSOLUTE MAXIMUM RATINGS*

RATING	VALUE
Ambient Operating Temperature	0°C to 70°C
Storage Temperature	-65°C to 125°C
Applied Input Voltage	-0.5V to 7.0V
Applied Output Voltage	-0.5V to 7.0V
VCC to Ground Potential	-0.5V to 7.0V
Power Dissipation	1.0W

***NOTICE:**
Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended period may affect reliability.

DC CHARACTERISTICS TA = 0°C TO 70°C, VCC = 5V ± 10%

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
VOH	Output High Voltage	2.4		V	IOH = -1.0mA
VOL	Output Low Voltage		0.4	V	IOL = 2.1mA
VIH	Input High Voltage	2.2	VCC + 0.3	V	
VIL	Input Low Voltage	-0.3	0.8	V	
ILI	Input Leakage Current		10	μA	VIN = 0 to 5.5V
ILO	Output Leakage Current		10	μA	VOUT = 0 to 5.5V
ICC3	Power-Down Supply Current		100	μA	$\overline{CE}$ > VCC - 0.2V
ICC2	Standby Supply Current		1	mA	$\overline{CE}$ = VIH
ICC1	Operating Supply Current		60	mA	Note 1

CAPACITANCE TA = 25°C, f = 1.0 MHz (Note 2)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
CIN	Input Capacitance		10	pF	VIN = 0V
COUT	Output Capacitance		10	pF	VOUT = 0V

AC CHARACTERISTICS: TA = 0°C to 70°C, VCC = 5V ± 10%

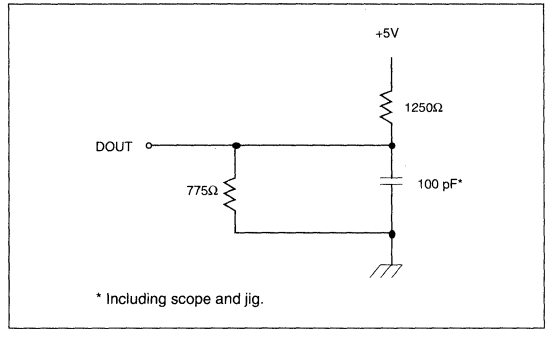
		23C1610-12		23C1610-15		23C1610-20			
SYMBOL	PARAMETER	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	UNIT	CONDITIONS
tCYC	Cycle Time	120		150		200		ns	
tAA	Address Access Time		120		150		200	ns	
tOH	Output Hold Time After Address Change	10		10		10		ns	
tACE	Chip Enable Access Time		120		150		200	ns	
tAOE	Output Enable/Chip Select Access Time		70		80		90	ns	
tLZ	Output Low Z Delay	0		0		0		ns	Note 3
tHZ	Output High Z Delay		70		70		70	ns	Note 4
tBHA	$\overline{BYTE}$ Access Time		120		150		200	ns	
tOHB	$\overline{BYTE}$ Output Hold Time	0		0				ns	
tBHZ	$\overline{BYTE}$ Output Delay Time		70		70		70	ns	
tBLZ	$\overline{BYTE}$ Output Set Time	10		10		10		ns	

NOTE:
1. Measured with device selected at f = 5 MHz and output unloaded.
2. This parameter is periodically sampled and is not 100% tested.
3. Output low-impedance delay (tLZ) is measured from CE going low.
4. Output high-impedance delay (tHZ) is measured from CE going high.

AC TEST CONDITIONS

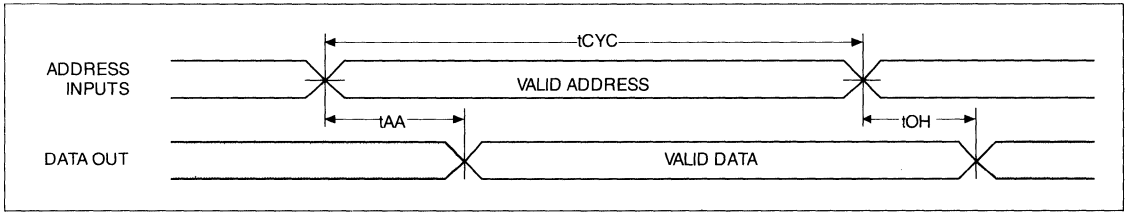
Input Pulse Levels	0.4V to 2.4V
Input Rise and Fall Times	10ns
Input Timing Level	1.5V
Output Timing Level	0.8V and 2.0V
Output Load	See Figure 1

FIG. 1 OUTPUT LOAD CIRCUIT

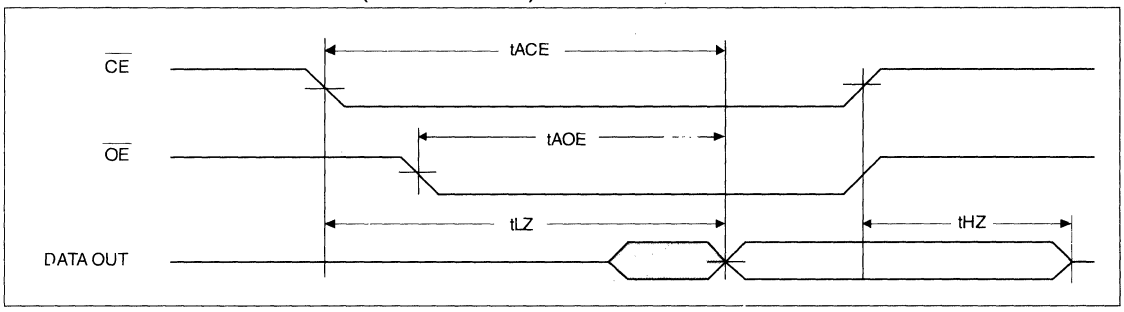


WAVEFORMS

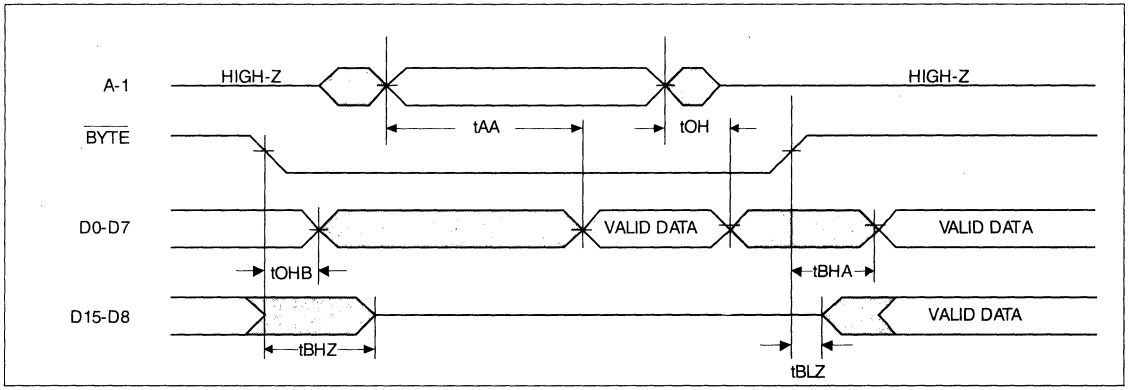
PROPAGATION DELDELAY FROM ADDRESS ($\overline{CE}$/$\overline{OE}$ = ACTIVE)



PN DELAY FROM CHIP ENABLE CHIP (ADDRESS VALID)



PROPAGATION DELAY FROM CHIP ENABLE (ADDRESS VALID)



ORDERING INFORMATION

PART NO.	ACCESS TIME(ns)	OPERATING CURRENT MAX.(mA)	STANDBY CURRENT MAX.(μA)	PACKAGE
MX23C1610PC-12	120	60	100	42 Pin DIP
MX23C1610MC-12	120	60	100	44 Pin SOP
MX23C1610PC-15	150	60	100	42 Pin DIP
MX23C1610MC-15	150	60	100	44 Pin SOP
MX23C1610PC-20	200	60	100	42 Pin DIP
MX23C1610MC-20	200	60	100	44 Pin SOP

IV. FLASH MEMORY

MX28F1000

1M-BIT (128K x 8) CMOS FLASH MEMORY

FEATURES

- 131,072 bytes by 8-bit organization
- Fast access time: 90/120/150 ns
- Low power consumption
  - 50mA maximum active current
  - 100μ A maximum standby current
- Programming and erasing voltage 12V ± 0.6V
- Command register architecture
  - Byte Programming (10μ s typical)
  - Chip Erase (1 sec typical)
  - Block Erase (16384 bytes by 8 blocks)
- Auto Erase (chip & block) and Auto Program
  - DATA polling
  - Toggle bit
- 10,000 minimum erase/program cycles
- Latch-up protected to 100mA from -1 to VCC+1V
- Advanced CMOS Flash memory technology
- Compatible with JEDEC-standard byte-wide 32-pin EPROM pinouts
- Package type:
  - 32-pin plastic DIP
  - 32-pin PLCC
  - 32-pin SOP
  - 32-pin TSOP (Type 1)

GENERAL DESCRIPTION

The MX28F1000 is a 1-mega bit Flash memory organized as 128K bytes of 8 bits each. MXIC's Flash memories offer the most cost-effective and reliable read/write non-volatile random access memory. The MX28F1000 is packaged in 32-pin PDIP, PLCC, SOP and TSOP. It is designed to be reprogrammed and erased in-system or in-standard EPROM programmers.

The standard MX28F1000 offers access times as fast as 120 ns, allowing operation of high-speed microprocessors without wait states. To eliminate bus contention, the MX28F1000 has separate chip enable ($\overline{CE}$) and output enable ($\overline{OE}$) controls.

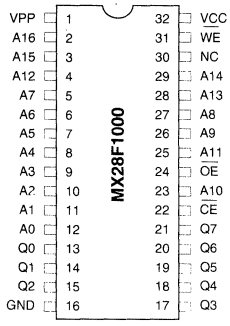
MXIC's Flash memories augment EPROM functionality with in-circuit electrical erasure and programming. The MX28F1000 uses a command register to manage this functionality, while maintaining a standard 32-pin pinout. The command register allows for 100% TTL level control inputs and fixed power supply levels during erase and programming, while maintaining maximum EPROM compatibility.

MXIC Flash technology reliably stores memory contents even after 10,000 erase and program cycles. The MXIC cell is designed to optimize the erase and programming mechanisms. In addition, the combination of advanced tunnel oxide processing and low internal electric fields for erase and programming operations produces reliable cycling. The MX28F1000 uses a 12.0V + 5% VPP supply to perform the High Reliability Erase and High Reliability Program algorithms.

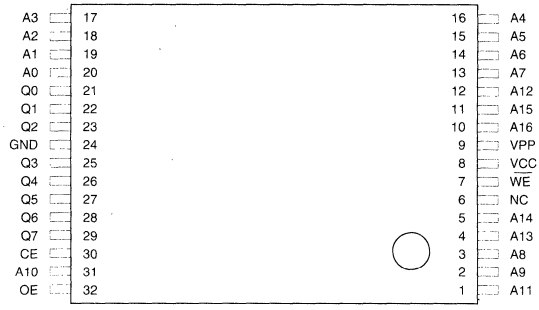
The highest degree of latch-up protection is achieved with MXIC's proprietary non-epi process. Latch-up protection is proved for stresses up to 100 milliamps on address and data pin from -1V to VCC + 1V.

PIN CONFIGURATIONS

32 PDIP

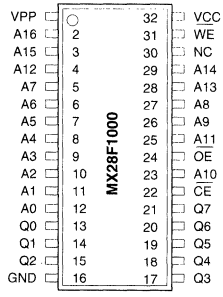


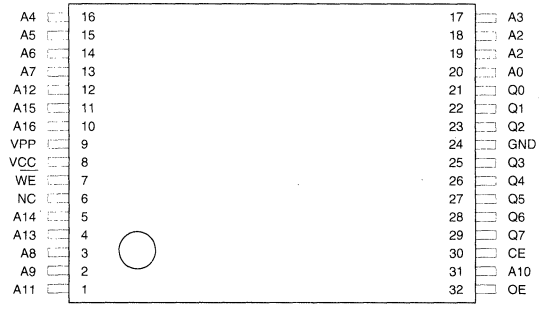
TSOP (TYPE 1)



(NORMAL TYPE)

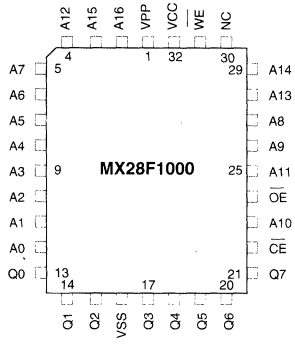
32 SOP





(REVERSE TYPE)

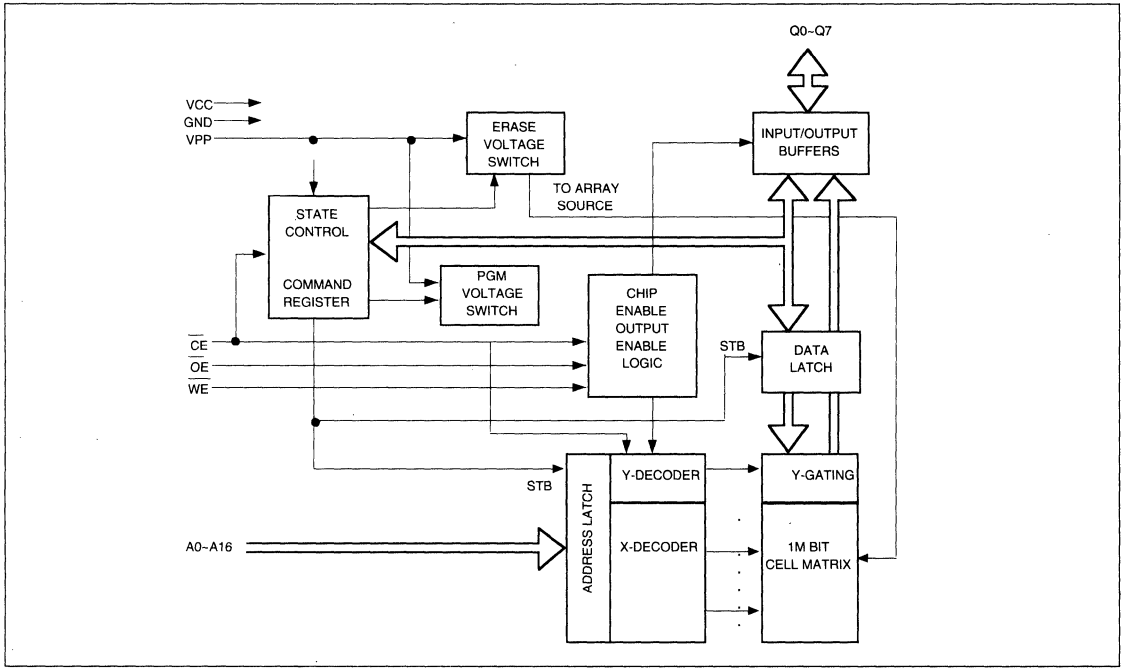
32 PLCC



PIN DESCRIPTION:

SYMBOL	PIN NAME
A0~A16	Address Input
Q0~Q7	Data Input/Output
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
$\overline{WE}$	Write enable Pin
VPP	Program Supply Voltage
VCC	Power Supply Pin (+5V)
GND	Ground Pin

BLOCK DIAGRAM



MX28F4000

4M-BIT (512K x 8) CMOS FLASH MEMORY

FEATURES

- 524,288 bytes by 8-bit organization
- Fast access time: 120/150/200 ns
- Low power consumption
  - 50mA maximum active current
  - 100μ A maximum standby current
- Programming and erasing voltage 12V ± 0.6V
- Command register architecture
  - Byte Programming (10μ s typical)
  - Chip Erase (1 sec typical)
  - Block Erase (16384 bytes by 32 blocks)
- Auto Erase (chip & block) and Auto Program
  - DATA polling
  - Toggle bit
- 10,000 minimum erase/program cycles
- Latch-up protected to 100mA from -1 to VCC+1V
- Advanced CMOS Flash memory technology
- Compatible with JEDEC-standard byte-wide 32-pin EPROM pinouts
- Package type:
  - 32-pin plastic DIP
  - 32-pin SOP
  - 32-pin TSOP (Type 1)

GENERAL DESCRIPTION

The MX28F4000 is a 4-mega bit Flash memory organized as 512K bytes of 8 bits each. MXIC's Flash memories offer the most cost-effective and reliable read/write non-volatile random access memory. The MX28F4000 is packaged in 32-pin PDIP, SOP and TSOP. It is designed to be reprogrammed and erased in-system or in-standard EPROM programmers.

The standard MX28F4000 offers access times as fast as 120 ns, allowing operation of high-speed microprocessors without wait states. To eliminate bus contention, the MX28F4000 has separate chip enable ($\overline{CE}$) and output enable ($\overline{OE}$) controls.

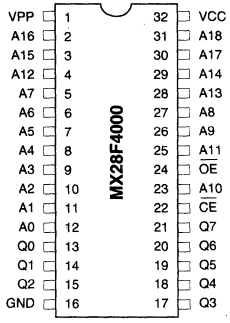
MXIC's Flash memories augment EPROM functionality with in-circuit electrical erasure and programming. The MX28F4000 uses a command register to manage this functionality, while maintaining a standard 32-pin pinout. The command register allows for 100% TTL level control inputs and fixed power supply levels during erase and programming, while maintaining maximum EPROM compatibility.

MXIC Flash technology reliably stores memory contents even after 10,000 erase and program cycles. The MXIC cell is designed to optimize the erase and programming mechanisms. In addition, the combination of advanced tunnel oxide processing and low internal electric fields for erase and programming operations produces reliable cycling. The MX28F4000 uses a 12.0V + 5% VPP supply to perform the High Reliability Erase and High Reliability Program algorithms.

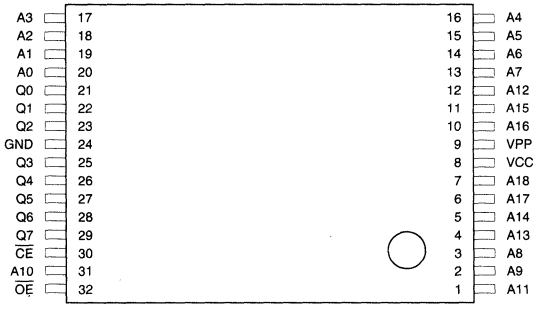
The highest degree of latch-up protection is achieved with MXIC's proprietary non-epi process. Latch-up protection is proved for stresses up to 100 milliamps on address and data pin from -1V to VCC + 1V.

PIN CONFIGURATIONS

32 PDIP

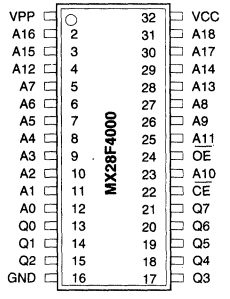


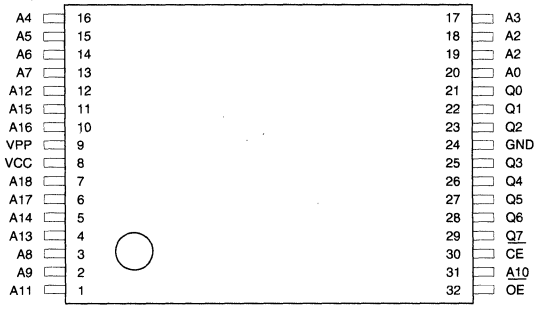
TSOP (TYPE 1)



(NORMAL TYPE)

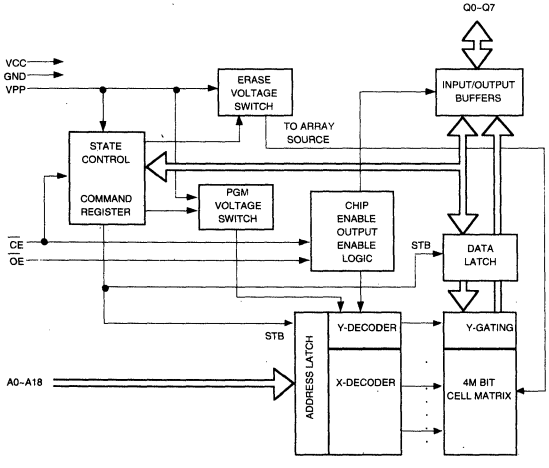
32 SOP





(REVERSE TYPE)

BLOCK DIAGRAM



PIN DESCRIPTION:

SYMBOL	PIN NAME
A0~A18	Address Input
Q0~Q7	Data Input/Output
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
VPP	Program Supply Voltage
VCC	Power Supply Pin (+5V)
GND	Ground Pin

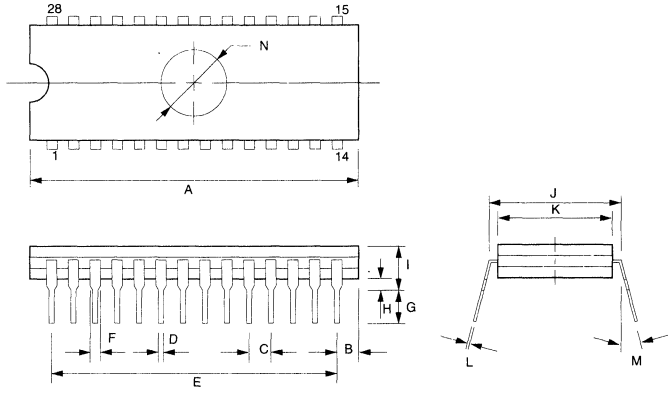
V. PACKAGE INFORMATION

MACRONIX, INC.

28-PIN CERDIP(MSI) WITH WINDOW (600 mil)

ITEM	MILLIMETERS	INCHES
A	37.69 max	1.485 max
B	1.85 ± .30	.073 ± .012
C	2.54 [TP]	.100 [TP]
D	.46 ± .05	.018 ± .002
E	33.02	1.300
F	1.40 ± .05	.055 ± .002
G	3.43 ± .38	.135 ± .015
H	.96 ± .43	.038 ± .017
I	4.87	.198
J	15.48 ± .13	.610 ± .005
K	13.38 ± .38	.527 ± .015
L	.25 ± .13	.010 ± .005
M	0 ~ 15°	0 ~ 15°
N	ø7.11	ø.280

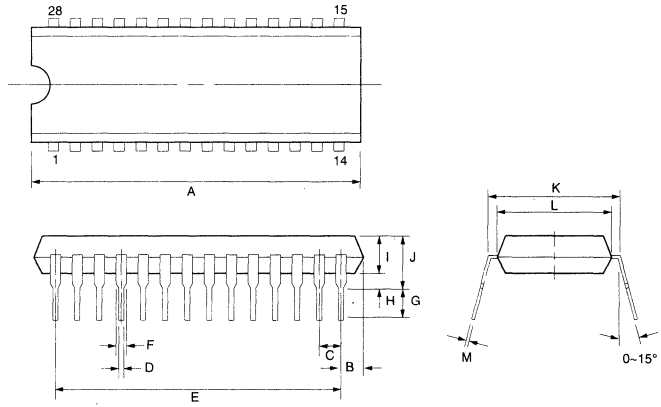
NOTE: Each lead centerline is located within .25 mm[.01 inch] of its true position [TP] at a maximum material condition.



28-PIN PLASTIC DIP (600 mil)

ITEM	MILLIMETERS	INCHES
A	37.34 max	1.470 max
B	2.03 [REF]	.080 [REF]
C	2.54 [TP]	.100 [TP]
D	.46 [Typ.]	.018 [Typ.]
E	32.99	1.300
F	1.52 [Typ.]	.060 [Typ.]
G	3.30 ± .25	.130 ± .010
H	.51 [REF]	.020 [REF]
I	3.94 ± .25	.155 ± .010
J	5.33 max.	.210 max.
K	15.22 ± .25	.600 ± .010
L	13.84 ± .25	.545 ± .010
M	.25 [Typ.]	.010 [Typ.]

NOTE: Each lead centerline is located within .25 mm[.01 inch] of its true position [TP] at a maximum material condition.



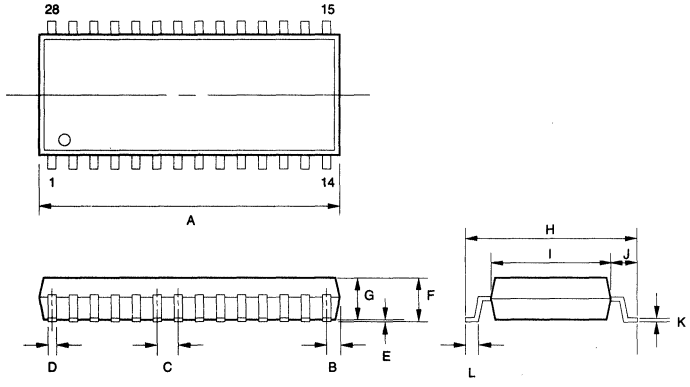
PACKAGE INFORMATION

MACRONIX, INC.

28-PIN PLASTIC SOP (450 mil)

ITEM	MILLIMETERS	INCHES
A	18.42 max.	.725 max.
B	.71 [REF]	.028 [REF]
C	1.27 [TP]	.050 [TP]
D	.41 [Typ.]	.016 [Typ.]
E	.10 min.	.004 min.
F	2.79 max.	.110 max.
G	2.36 ± .13	.093 ± .005
H	10.30 ± .25	.406 ± .010
I	7.49 ± .13	.295 ± .005
J	1.42	.056
K	.25 [Typ.]	.010 [Typ.]
L	.76	.030

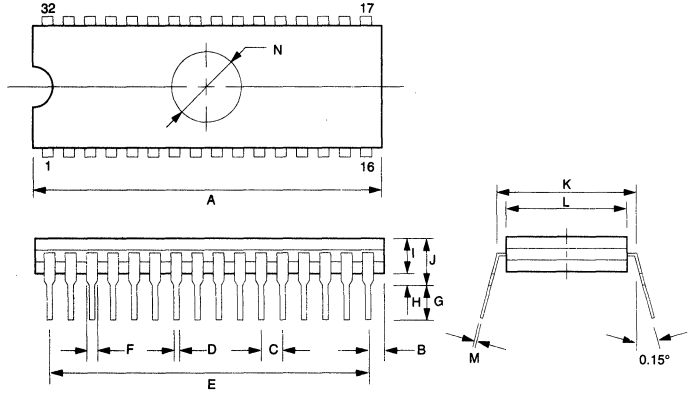
NOTE: Each lead centerline is located within .25 mm[.01 inch] of its true position [TP] at a maximum material condition.



32-PIN CERDIP (MSI) WITH WINDOW (600 mil)

ITEM	MILLIMETERS	INCHES
A	42.26 max	1.665 max
B	1.90 ± .38	.075 ± .015
C	2.54 [TP]	.100 [TP]
D	.46 [REF]	.018 [REF]
E	38.07	1.500
F	1.42 [REF]	.056 [REF]
G	3.43 ± .38	.135 ± .015
H	.96 ± .43	.038 ± .017
I	4.06	.160
J	5.00	.203
K	15.58 ± .13	.614 ± .005
L	13.20 ± .38	.520 ± .015
M	.25 [REF]	.010 [REF]
N	ø8.12	ø.320

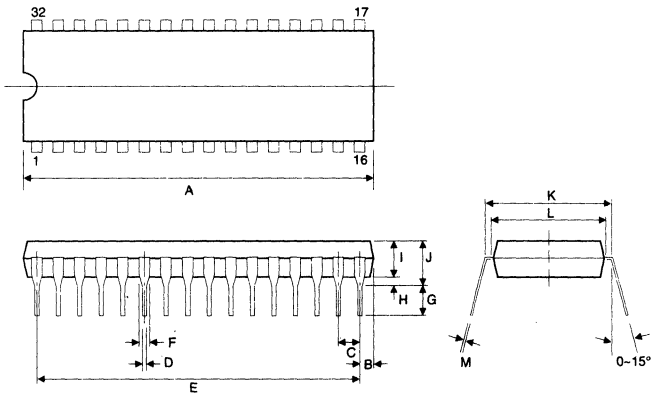
NOTE: Each lead centerline is located within .25 mm[.01 inch] of its true position [TP] at a maximum material condition.



32-PIN PLASTIC DIP (600 mil)

ITEM	MILLIMETERS	INCHES
A	42.13 max.	1.660 max.
B	1.90 [REF]	.075 [REF]
C	2.54 [TP]	.100 [TP]
D	.46 [Typ.]	.018 [Typ.]
E	38.07	1.500
F	1.27 [Typ.]	.050 [Typ.]
G	3.30 ± .25	.130 ± .010
H	.51 [REF]	.020 [REF]
I	3.94 ± .25	.155 ± .010
J	5.33 max.	.210 max.
K	15.22 ± .25	.600 ± .010
L	13.97 ± .25	.550 ± .010
M	.25 [Typ.]	.010 [Typ.]

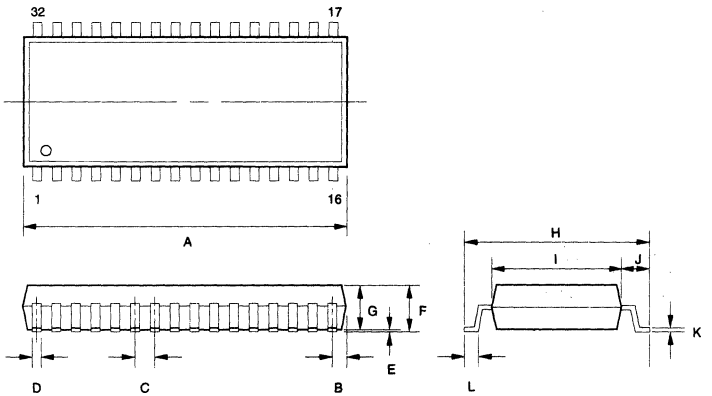
NOTE: Each lead centerline is located within .25 mm[.01 inch] of its true position [TP] at a maximum material condition.



32-PIN PLASTIC SOP (450 mil)

ITEM	MILLIMETERS	INCHES
A	20.95 max.	.825 max.
B	1.00 [REF]	.039 [REF]
C	1.27 [TP]	.050 [TP]
D	.40 [Typ.]	.016 [Typ.]
E	.05 min.	.002 min.
F	3.05 max.	.120 max.
G	2.69 ± .13	.106 ± .005
H	14.12 ± .25	.556 ± .010
I	11.30 ± .13	.445 ± .005
J	1.42	.056
K	.20 [Typ.]	.008 [Typ.]
L	.79	.031

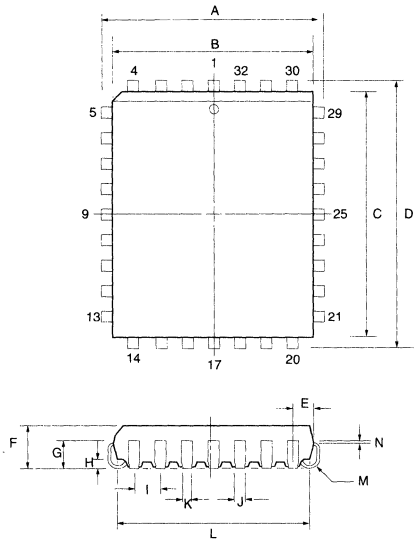
NOTE: Each lead centerline is located within .25 mm[.01 inch] of its true position [TP] at a maximum material condition.



32-PIN PLASTIC LEADED CHIP CARRIER (PLCC)

ITEM	MILLIMETERS	INCHES
A	12.44 ± .13	.490 ± .005
B	11.50 ± .13	.453 ± .005
C	14.04 ± .13	.553 ± .005
D	14.98 ± .13	.590 ± .005
E	1.93	.076
F	3.30 ± .25	.130 ± .010
G	2.03 ± .13	.080 ± .005
H	.51 ± .13	.020 ± .005
I	1.27 [Typ.]	.050 [Typ.]
J	.71[REF]	.028[REF]
K	.46 [REF]	.018 [REF]
L	10.40/12.94 (W) (L)	.410/.510 (W) (L)
M	.89 R	.035 R
N	.25 (TYP.)	.010 (TYP.)

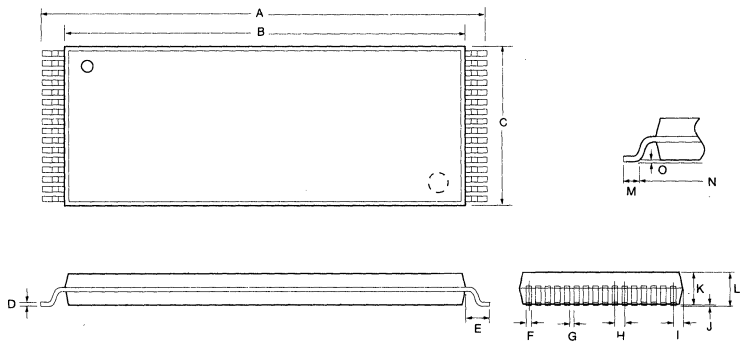
NOTE: Each lead centerline is located within .25 mm[.01 inch] of its true position [TP] at a maximum material condition.



32-PIN PLASTIC TSOP

ITEM	MILLIMETERS	INCHES
A	20.0 ± .20	.078 ± .006
B	18.40 ± .10	.724 ± .004
C	8.20 max.	.323 max.
D	0.15 [Typ.]	.006 [Typ.]
E	.80 [Typ.]	.031 [Typ.]
F	.20 ± .10	.008 ± .004
G	.30 ± .10	.012 ± .004
H	.50 [Typ.]	.020 [Typ.]
I	.45 max.	.018 max.
J	0 ~ .20	0 ~ .008
K	1.00 ± .10	.039 ± .004
L	1.27 max.	.050 max.
M	.50	.020
N	19.00	.748
O	0 ~ 5	.500

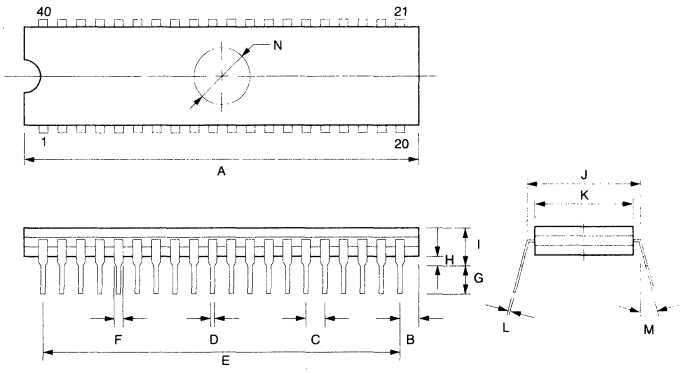
NOTE: Each lead centerline is located within .25 mm[.01 inch] of its true position [TP] at a maximum material condition.



40-PIN CERDIP (MSI) WITH WINDOW (600 mil)

ITEM	MILLIMETERS	INCHES
A	53.34 max.	2.100 max.
B	1.85 ± .30	.073 ± .012
C	2.54 [TP]	.100 [TP]
D	.46 ± .05	.018 ± .002
E	48.22	1.900
F	1.40 ± .05	.055 ± .002
G	3.43 ± .38	.135 ± .015
H	.94 ± .41	.037 ± .016
I	5.00	.197
J	15.51 ± .08	.611 ± .003
K	14.82 ± .38	.584 ± .015
L	.25 ± .13	.010 ± .005
M	0~15°	0~15°
N	φ9.64	φ.380

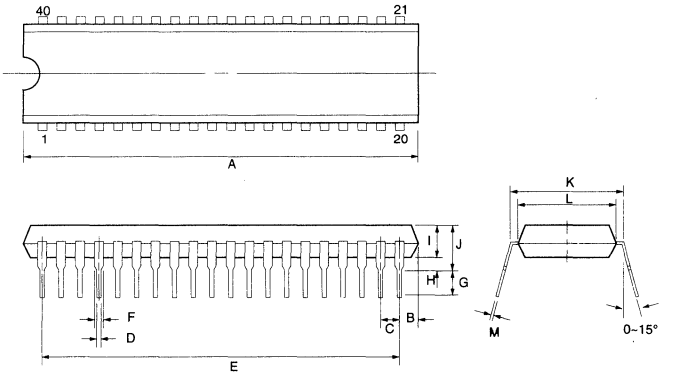
NOTE: Each lead centerline is located within .25 mm[.01 inch] of its true position [TP] at a maximum material condition.



40-PIN PLASTIC DIP (600 mil)

ITEM	MILLIMETERS	INCHES
A	52.54 max.	2.070 max.
B	2.03 [REF]	.080 [REF]
C	2.54 [TP]	.100 [TP]
D	.46 [Typ.]	.018 [Typ.]
E	48.22	1.900
F	1.52 [Typ.]	.060 [Typ.]
G	3.30 ± .25	.130 ± .010
H	.51 [REF]	.020 [REF]
I	3.94 ± .25	.155 ± .010
J	5.33 max.	.210 max.
K	15.22 ± .25	.600 ± .010
L	13.97 ± .25	.550 ± .010
M	.25 [Typ.]	.010 [Typ.]

NOTE: Each lead centerline is located within .25 mm[.01 inch] of its true position [TP] at a maximum material condition.

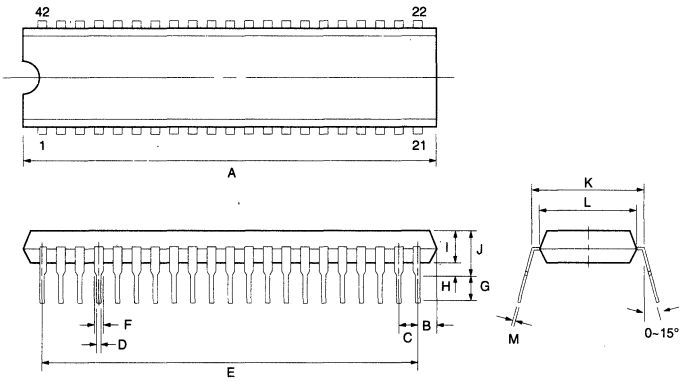


MACRONIX, INC.

42-PIN PLASTIC DIP (600 mil)

ITEM	MILLIMETERS	INCHES
A	52.54 max.	2.070 max.
B	0.76 [REF]	.030 [REF]
C	2.54 [TP]	.100 [TP]
D	.46 [Typ.]	.018 [Typ.]
E	50.76	2.000
F	1.27 [Typ.]	.050 [Typ.]
G	3.30 ± . 25	.130 ± .010
H	.51 [REF]	.020 [REF]
I	3.94 ±. 25	.155 ± .010
J	5.33 max.	.210 max.
K	15.22 ± .25	.600 ± .010
L	13.97± .25	.550 ± .010
M	.25 [Typ.]	.010 [Typ.]

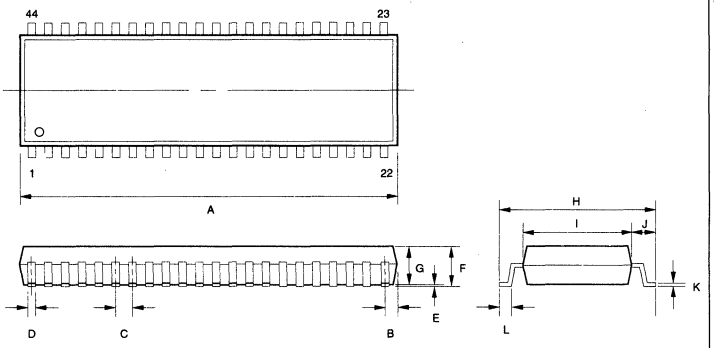
NOTE: Each lead centerline is located within .25 mm[.01 inch] of its true position [TP] at a maximum material condition.



44-PIN PLASTIC SOP

ITEM	MILLIMETERS	INCHES
A	28.70 max.	1.130 max.
B	1.10 [REF]	.043 [REF]
C	1.27 [TP]	.050 [TP]
D	.40 ± .10 [Typ.]	.016 ± .004 [Typ.]
E	.010 min.	.004 min.
F	3.00 max.	.118 max.
G	2.80 ± .13	.110 ± .005
H	16.04 ± .30	.631 ± .012
I	12.60	0.496
J	1.72	.068
K	.15 ± .10 [Typ.]	.006 ± .004 [Typ.]
L	.80 ± .20	.031 ± .008

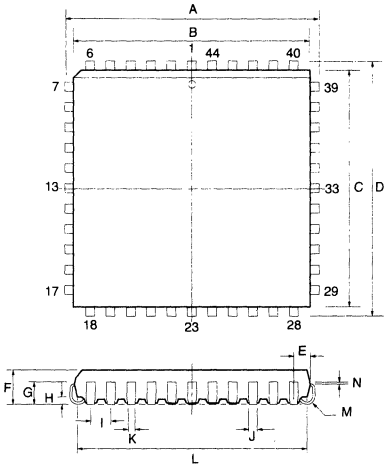
NOTE: Each lead centerline is located within .25 mm[.01 inch] of its true position [TP] at a maximum material condition.



44-PIN PLASTIC LEADED CHIP CARRIER (PLCC)

ITEM	MILLIMETERS	INCHES
A	17.53 ± .12	.690 ± .005
B	16.59 ± .12	.653 ± .005
C	16.59 ± .12	.653 ± .005
D	17.53 ± .12	.690 ± .005
E	1.95	.077
F	4.70 max.	.185 max
G	2.55 ± .25	.100 ± .010
H	.51 min.	.020 min.
I	1.27 [Typ.]	.050 [Typ.]
J	.71 ± .10	.028 ± .004
K	.46 ± .10	.018 ± .004
L	15.50 ± .51	.610 ± .020
M	.63 R	.025 R
N	.25 [Typ.]	.010 [Typ.]

NOTE: Each lead centerline is located within .25 mm[.01 inch] of its true position [TP] at a maximum material condition.



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