LINEAR TECHNOLOGY

Linear Databook

EXCLUSIVELY COMMITTED TO LINEAR

The founding theme of Linear Technology Corporation was to create a company capable of leading and directing linear circuit technology and design concepts of the future, and thus become the market's linear specialist. The company believes that the total IC business has become so diverse and so complex that a single company will have great difficulty assembling the engineering talent necessary to lead in all areas of device technology.

Today, the customer base benefits by accessing the best product available in each functional area of the IC market from those vendors who are at the leading edge of performance and technology as a result of their "focused" strategy approach. The customer now has the choice of acquiring the best linear, the best microprocessor, the best memory products, etc., by choosing the best vendor in each area. In order to achieve the goal of becoming the market's first choice in the linear area, LTC has assembled the leading design, test, product, assembly, quality and process engineering talent in the industry, operating in what we feel is the most modern linear integrated circuit facility in production today.

Linear Technology possesses a wide variety of bipolar processes including Super Beta, Bifet, low noise, high speed, thin film resistors, sinkers, sub-surface zeners, and more. The company also has in production a very modern silicon-gate CMOS process, LTCMOS™, which is specifically tailored to satisfy the special needs of linear IC functions.

Linear Technology is committed to servicing the demanding requirements of the Military/Aerospace marketplace. Our 883 program is designed to consistently provide off-the-shelf high performance linear integrated circuits tested to the requirements of MIL-STD-883 Class B, and fully compliant to Revision C. Our documentation, designs, procedures, and facilities have been carefully established to meet the rigid requirements of MIL-STD-38510 level devices. The company's facility is JAN approved and numerous JAN QPL part types are currently being supplied by Linear Technology. All military-grade products are 100% tested at temperature extremes. Both commercial and military outgoing quality levels are sampled over temperature with full lot traceability back to the original wafer from which the device was derived. Presently Linear Technology can boast that its products are used by all of the top 25 largest military contractors in the U.S.

On the commercial side of the business, the company's proprietary products are currently being used by leading manufacturers of automobiles, computers, instruments, cameras, telecommunication systems and in many other areas. The company prides itself in doing business with the major manufacturers and leaders in each of these market segments.

This catalog contains products that already enjoy very wide acceptance status in new and existing end products.

In addition to the commitment to provide better technical solutions, we also commit to our customers that we will strive to make quality and reliability a reason to buy from Linear Technology. Our products address the instrumentation, industrial, data acquisition, peripheral, interface, and military markets with solutions to linear systems application problems.

Linear Technology Corporation

Linear Databook
1986

LIFE SUPPORT POLICY

LINEAR'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF LINEAR TECHNOLOGY CORPORATION. As used herein:

a. *Life support devices or systems are devices or systems which (1) are intended for surgical implant into the body, or (2) support or sustain life and whose failure to perform when properly used in accordance with instructions for use provided in the labeling can be reasonably expected to result in a significant injury to the user.*

b. *A critical component is any component in a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system or to affect its safety or effectiveness.*

Information furnished herein by Linear Technology Corporation is believed to be accurate and reliable. However, no responsibility is assumed for its use. Linear Technology Corporation makes no representaiton that the interconnection of its circuits, as described herein, will not infringe on existing patent rights.

Linear Technology Corporation • 1630 McCarthy Blvd. • Milpitas, CA 95035 • (408) 942-0810 Printed in USA

LINEAR TECHNOLOGY

1986 Linear Databook

SECTION 1—GENERAL INFORMATION

SECTION 2—OPERATIONAL AMPLIFIERS

TABLE OF CONTENTS

SECTION 3—VOLTAGE REGULATORS

SECTION 4—VOLTAGE REFERENCES

SECTION 5—COMPARATORS

SECTION 6—FILTERS

SECTION 7—PULSE-WIDTH MODULATORS

SECTION 8—CMOS/DATA CONVERSION/INTERFACE

TABLE OF CONTENTS

ALPHANUMERIC INDEX

SECTION 1—GENERAL INFORMATION

SECTION 1—GENERAL INFORMATION

I. ORDERING INFORMATION

Linear Technology employs numerous sales representatives, stocking distributors and stocking representatives, throughout the world. For a list of the distributors nearest your location, please contact Linear Technology in Milpitas, California. Local inventories and pricing of Linear Technology products are generally available through these distributors.

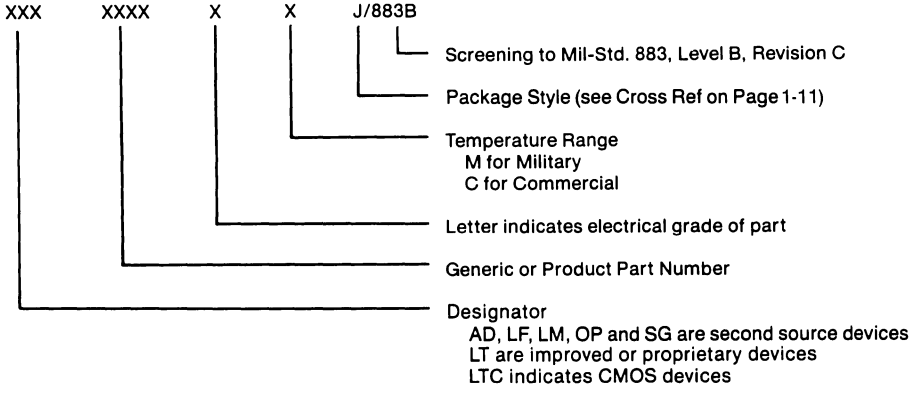
Orders placed directly with the factory require a minimum order value of $2000.00, and a minimum line item value of $500.00. Terms are net 30, FOB Milpitas, California.

II. RELIABILITY PROGRAMS

Linear Technology Corporation currently offers the following Reliability Programs:

A. JAN QPL devices.
B. DESC drawings.
C. Mil-Std 883, Level B, Revision C for all military temperature range devices.
D. "R-Flow" Burn-In Program for commercial temperature range devices. Consult Factory regarding burn-in program.

III. PART NUMBER EXPLANATION



IV. PACKAGE SUFFIX EXPLANATION

Letter Designator	Description
D	14, 16, 18 and 20 Pin Side Brazed Hermetic DIP
D8	8 Pin Side Brazed Hermetic DIP
H	Multi Lead Metal Can
J	14, 16, 18 and 20 Pin Ceramic DIP
J8	8 Pin Ceramic DIP
K	TO-3 Metal Can (Steel)
N	14, 16, 18 and 20 Pin Molded DIP
N8	8 Pin Molded DIP
T	TO-220 Molded (3 lead, 5 lead)
Z	TO-92 Molded (3 lead)
S8	8 Lead Small Outline (SO) Package

AMD

AMD P/N	LTC DIRECT REPL
LF155A	LF155A
	LT1055AM*
LF155	LF155
	LT1055M*
LF156A	LF156A
	LT1056AM*
LF156	LF156
	LT1056M*
LF198	LF198
LF355A	LF355A
	LT1055AC*
LF356A	LF356A
	LT1056AC*
LF398	LF398
LM108	LM108
	LT1008M*
LM108A	LM108A
	LT1008M*
LM111	LM111
	LT111A*
	LT1011M*
LM118	LM118
	LT118A*
LM119	LM119
	LT119A*
LM148	LT1014*
LM308A	LM308A
	LT1008C*
LM311	LM311
	LT311A*
	LT1011C*
LM318	LM318
	LT318A*
LM319	LM319
	LT319A*

ANALOG DEVICES

AD P/N	LTC DIRECT REPL
AD101A	LM101A
AD518	LM118**
	LT118A**
AD517	OP07**
	LT1001**
AD510J	OP07E*
	LT1001C*
AD510K	LT1001AC*
AD510L	LT1001AC*
AD510S	OP07A*
	LT1001AM*
ADOP07	OP07
	LT1001M*
ADOP07A	OP07
	LT1001AM*
ADOP07C	OP07C
	LT1001C*
ADOP07D	OP07D
	LT1001C*
ADOP07E	OP07E
	LT1001C*
AD580	LT1019-2.5**
AD581	AD581
	LT1031**
AD589	LT1004†

FAIRCHILD

FSC P/N	LTC DIRECT REPL
UA101A	LM101A
UA107A	LM107
UA108	LM108
	LT1008M*
UA108A	LM108A
	LT1008M*
UA111	LM111
	LT111A*
	LT1011M*
UA117	LM117
	LT117A*
SH123	LM123
	LT123A*
	LT1003M**
UA124	LT1014M*
UA148	LT1014M*
UA1558M	LT1013M*
UA78H05C	LT1003C**
UA308A	LM308A
	LT1003M**
UA311	LM311
	LT311A*
	LT1011C*
UA317	LM317
	LT317A*
UA318	LM318
	LT318A*
SH323	LM323
	LT323A*
	LT1003M**
UA714	OP07
	LT1001M*
UA714C	OP07C
	LT1001C*
UA714L	OP07D
	LT1001C*
UA714E	OP07E
	LT1001C*

* **LTC Improved Replacement:** 100% Pin-for-Pin compatible with better electrical specifications.

** **Similar Device:** Please consult the data sheet to determine the suitability of the replacement for specific applications.

† Consult factory for guaranteed TC devices.

HARRIS

HARRIS P/N	LTC DIRECT REPL
HAOP07	OP07 LT1001M*
HAOP07A	OP07A LT1001AM*
HAOP07C	OP07C LT1001C*
HAOP07E	OP07E LT1001C*
HA5135-2	OP07 LT1001M*
HA5130-2	OP07A LT1001AM*
HA5135-5	OP07C LT1001C*
HA5130-5	OP07E LT1001C*
HA2510	LT118A** LM118**
HA2512	LT118A** LM118**
HA2515	LT318A** LM318**

INTERSIL

INTERSIL P/N	LTC DIRECT REPL
ICL7650 8-Pin	LTC1052*
ICL7652 8-Pin	LTC7652
ICL7660	LTC1044*
ICL8069C	LM385-1.2 LT1004C-1.2*
ICL8069M	LM185-1.2 LT1004M-1.2*
LF155A	LF155A
LF155	LF155
LF156A	LF156A
LF156	LF156
LF355A	LF355A
LF356A	LF356A
LH2108A	LH2108A
LH2108	LH2108
LM101A	LM101A
LM107	LM107
LM108	LM108 LT1008M*
LM108A	LM108A LT1008M*
LM111	LM111 LT111A* LT1011M*
LM124	LT1014M*

MOTOROLA

MOTO P/N	LTC DIRECT REPL
LM101A	LM101A
LM107	LM107
LM108	LM108 LT1008M*
LM108A	LM108A LT1008M*
LM111	LM111 LT111A* LT1011M*
LM117	LM117 LT117A*
LM123	LM123 LT123A* LT1003M**
LM137	LM137 LT137A* LT1033M**
LM150	LM150 LT150A*
LM158	LT1013M*
LM308A	LM308A LT1008C*
LM311	LM311 LT311A* LT1011C*
LM317	LM317 LT317A*
LM323	LM323 LT323A* LT1003C**
LM337	LM337 LT337A* LT1033C**
LM350	LM350 LT350A*
MC1558	LT1013M*
MC78T05	LM323T LT323AT*
SG1524	SG1524 LT1524*
SG1525A	SG1525A LT1525A*
SG1527A	SG1527A LT1527A*
SG3524	SG3524 LT3524*
SG3525A	SG3525A LT3525A*
SG3527A	SG3527A LT3527A*
LF355A	LF355A
LF356A	LF356A
LM148	LT1014M*
LM124	LT1014M*

* **LTC Improved Replacement:** 100% Pin-for-Pin compatible with better electrical specifications.

** **Similar Device:** Please consult the data sheet to determine the suitability of the replacement for specific applications.

† Consult factory for guaranteed TC devices.

MOTO P/N	LTC DIRECT REPL
MC1400U2	LT1019CN8-2.5*
MC1400AU2	LT1019ACN8-2.5*
MC1400U5	LT1019CN8-5*
MC1400AU5	LT1019ACN8-5*
MC1400U10	LT1019CN8-10*
MC1400AU10	LT1019ACN8-10*
LF155A	LF155A
LF155	LF155
LF156A	LF156A
LF156	LF156

NATIONAL SEMICONDUCTOR

NSC P/N	LTC DIRECT REPL
LF155A	LF155A
	LT1055AM*
LF155	LF155
	LT1055M*
LF156A	LF156A
	LT1056AM*
LF156	LF156
	LT1056M*
LF198A	LF198A
LF198	LF198
LF355A	LF355A
	LT1055AC*
LF356A	LF356A
	LT1056AC*
LF398A	LF398A
LF398	LF398
LH0002	LT1010M**
LH0044	LT1001M**
LH0070	LH0070
	LT1021M*
LH2108	LH2108
LH2108A	LH2108A
LM10	LM10
LM10B	LM10B
LM10C	LM10C
LM101A	LM101A
LM107	LM107
LM108	LM108
	LT1008M*
LM108A	LM108A
	LT1008M*
LM111	LM111
	LT111A*
	LT1011M*
LM112	LT1012M*
LM113	LT1004M-1.2*
LM117	LM117
	LT117A*
LM117HV	LM117HV
	LT117AHV*
LM118	LM118
	LT118A*

NSC P/N	LTC DIRECT REPL
LM119	LM119
	LT119A*
LM123	LM123
	LT123A*
	LT1003M**
LM124	LT1014M*
LM129A	LM129A
LM129B	LM129B
LM129C	LM129C
LM133	LT1033M*
LM134	LM134
LM134-3	LM134-3
LM134-6	LM134-6
LM136A	LM136A
	LT1009M*
LM136-2.5	LM136-2.5
	LT1009M*
LM136-5	LT1029M**
LM137	LM137
	LT137A
	LT1033M**
LM137HV	LM137HV
	LT137AHV*
LM138	LM138
	LT138A*
LM148	LT1038M**
LM150	LM150
	LT150A*
LM158	LT1013M*
LM168BY-5.0	LT1019AM-5*
LM168BY-10.0	LT1019AM-5*
LM185-1.2	LM185-1.2
	LT1004M-1.2*
LM185-2.5	LM185-2.5
	LT1004M-2.5*
LM196	LT1038M**
LM199	LM199
LM199A	LM199A
LM199A-20	LM199A-20
LM234-3	LM234-3
LM234-6	LM234-6
LM308A	LM308A
	LT1008C*
LM311	LM311
	LT311A*
	LT1011C*
LM317	LM317
	LT317A*
LM317HV	LM317HV
	LT317AHV*
LM318	LM318
	LT318A*
LM319	LM319
	LT319A*
LM323	LM323
	LT323A*
	LT1003C**

* **LTC Improved Replacement:** 100% Pin-for-Pin compatible with better electrical specifications.

** **Similar Device:** Please consult the data sheet to determine the suitability of the replacement for specific applications.

† Consult factory for guaranteed TC devices.

NSC P/N	LTC DIRECT REPL
LM329A	LM329A
LM329B	LM329B
LM329C	LM329C
LM329D	LM329D
LM333	LT1033C*
LM333A	LT1033C
LM334	LM334
LM336-2.5	LM336
	LT1009C*
LM336B-2.5	LM336B
	LT1009C*
LM336-5	LT1029C**
LM337	LM337
	LT337A*
	LT1033C**
LM337HV	LM337HV
	LT337AHV*
LM338	LM338
	LT338A*
LM350	LM350
	LT350A*
LM368Y-5.0	LT1019AC-5*
LM368-5.0	LT1019AC-5*
LM368Y-10.0	LT1019AC-10*
LM368-10.0	LT1019AC-10*
LM385-1.2	LM385-1.2
	LT1004C-1.2*
LM385-2.5	LM385-2.5
	LT1004C-2.5*
LM396	LT1038C**
LM399	LM399
LM399A	LM399A
LM399A-50	LM399A-50
LM1524	SG1524
	LT1524*
LM3524	SG3524
	LT3524*
LM2935	LT1005**
MF5	LTC1059*
MF10	LTC1060*

NEC

NEC P/N	LTC DIRECT REPL
μPC156	LM308A
	LT1008C*
μPC159	LM318
	LT318A*
μPC254	OP07
	LT1001*
μPC271	LM311
	LT311A*
	LT1011C*
μPC272	LM319
	LT319A*
μPC311	LM311
	LT311A*
	LT1011C*
μPC319	LM319
	LT319A*
μPC354	OP07
	LT1001*
μPC454	LT1002
μPC649	LF398

PMI

PMI P/N	LTC DIRECT REPL
CMP01	LT1011**
CMP02	LT1011**
OP01	LT1023*
OP04	LT1013*
OP05	OP05
	LT1001M*
OP05A	OP05A
	LT1001M*
OP05C	OP05C
	LT1001C*
OP05E	OP05E
	LT1001C*
OP07	OP07
	LT1001M*
OP07A	OP07A
	LT1001AM*
OP07C	OP07C
	LT1001C*
OP07E	OP07E
	LT1001C*
OP10	LT1002M*
OP10A	LT1002AM*
OP10C	LT1002C*
OP10E	LT1002C
OP11	LT1014*
OP12A	LT1012M*
OP12B	LT1012M*
OP12C	LT1012M*
OP12E	LT1012C*
OP12F	LT1012C*
OP12G	LT1012C*
OP15A	OP15A
	LT1055AM*
OP15B	OP15B
	LT1055M
OP15C	OP15C
	LT1055M*
OP15E	OP15E
	LT1055AC*
OP15F	OP15F
	LT1055C*
OP15G	OP15G
	LT1055C*

* **LTC Improved Replacement:** 100% Pin-for-Pin compatible with better electrical specifications.
** **Similar Device:** Please consult the data sheet to determine the suitability of the replacement for specific applications.
† Consult factory for guaranteed TC devices.

PMI P/N	LTC DIRECT REPL
OP16A	OP16A
	LT1056AM*
OP16B	OP16B
	LT1056M*
OP16C	OP16C
	LT1056M*
OP16E	OP16E
	LT1056AC*
OP16F	OP16F
	LT1056C*
OP16G	OP16G
	LT1056C*
OP207A	LT1002M*
OP207B	LT1002M*
OP207E	LT1002C*
OP207F	LT1002C*
OP27A	OP27A
	LT1007AM*
OP27B	LT1007M*
OP27C	OP27C
	LT1007M*
OP27E	OP27E
	LT1007AC*
OP27F	LT1007C*
OP27G	OP27G
	LT1007C*
OP37A	OP37A
	LT1037AM*
OP37B	OP37A
	LT1037M*
OP37C	OP37C
	LT1037M*
OP37E	OP37E
	LT1037AC*
OP37F	OP37E
	LT1037C*
OP37G	OP37G
	LT1037C*
OP221	LT1013*
OP227A	OP227A
OP227B	OP227A
OP227C	OP227C
OP227E	OP227E
OP227F	OP227E
OP227G	OP227G
OP421	LT1014*
PM108	LM108
	LT1008M*
PM108A	LM108A
	LT1008M*
PM155A	LF155A
	LT1055M*
PM155	LF155
	LT1055M*
PM1558	LT1013M*
PM156A	LF156A
	LT1056M*

PMI P/N	LTC DIRECT REPL
PM156	LF156
	LT1056M*
PM2108A	LH2108A
PM2108	LH2108
PM308A	LM308A
	LT1008C*
PM355A	LF355A
	LT1055C*
PM356A	LF356A
	LT1056C*
REF01	REF01
	LT1019M-10*
	LT1021-10**
REF01A	REF01A
	LT1019AM-10*
	LT1021-10**
REF01C	REF01C
	LT1019C-10*
	LT1021-10**
REF01E	REF01E
	LT1019AC-10*
	LT1021-10**
REF01H	REF01H
	LT1019C-10*
	LT1021-10**
REF02	REF02
	LT1019M-5*
	LT1021-5**
REF02A	REF02A
	LT1019AM-5*
	LT1021-5**
REF02C	REF02C
	LT1019C-5*
	LT1021-5**
REF02D	LT1019C-5*
	LT1021-5**
REF02E	REF02E
	LT1019AC-5*
	LT1021-5**
REF02H	REF02H
	LT1019C-5*
	LT1021-5**

RAYTHEON

RAYTH P/N	LTC DIRECT REPL
LM101A	LM101A
LM107	LM107
LM111	LM111
	LT111A*
	LT1011M*
LM124	LT1014M*
LM148	LT1014M*
LM311	LM311
	LT311A*
	LT1011C*

* **LTC Improved Replacement:** 100% Pin-for-Pin compatible with better electrical specifications.

** **Similar Device:** Please consult the data sheet to determine the suitability of the replacement for specific applications.

† Consult factory for guaranteed TC devices.

RAYTH P/N	LTC DIRECT REPL
OP05	OP05
	LT1001M*
OP05A	OP05A
	LT1001AM*
OP05C	OP05C
	LT1001C*
OP05E	OP05E
	LT1001C*
OP07	OP07
	LT1001M*
OP07A	OP07A
	LT1001AM*
OP07C	OP07C
	LT1001C*
OP07E	OP07E
	LT1001C*
OP27A	OP27A
	LT1007AM*
OP27B	OP27A
	LT1007M
OP27C	OP27C
	LT1007M*
OP27E	OP27E
	LT1007AC*
OP27F	OP27E
	LT1007C*
OP27G	OP27G
	LT1007C*
OP37A	OP37A
	LT1037AM*
OP37B	OP37A
	LT1037M
OP37C	OP37C
	LT1037M*
OP37E	OP37E
	LT1037AC*
OP37F	OP37E
	LT1037C*
OP37G	OP37G
	LT1037C*
RC714CH	OP07C
	LT1001C*
RC714EH	OP07E
	LT1001C*
RM1558	LT1013M*
RM714H	OP07
	LT1001M*

SIGNETICS

SIGNETICS P/N	LTC DIRECT REPL
LF398	LF398
LF398A	LF398A
LM101A	LM101A
LM111	LM111
	LT111A*
	LT1011M*
LM119	LM119
	LT119A*
LM124	LT1014M*
LM158	LT1013M*
LM311	LM311
	LT311A*
	LT1011C*
MC1558	LT1013M*
NE5534	OP37*
	LT1037*
NE5534A	OP37*
	LT1037*
SE5534	OP37*
	LT1037*
SE5534A	OP37*
	LT1037*
SG3524	SG3524
	LT3524*

SILICON GENERAL

SILICON GEN P/N	LTC DIRECT REPL
SG101A	LM101A
SG108	LM108
	LT1008M*
SG108A	LM108A
	LT1008M*
SG111	LM111
	LT111A*
	LT1011M*
SG117	LM117
	LT117A*
SG123	LM123
	LT123A*
	LT1003M**
SG124	LT1014M*
SG137	LM137
	LT137A*
	LT1033M**
SG138	LM138
	LT138A*
SG150	LM150
	LT150A*
SG1558	LT1013M*
SG311	LM311
	LT311A*
	LT1011C*
SG317	LM317
	LT317A*
SG323	LM323
	LT323A*
	LT1003C**

* **LTC Improved Replacement:** 100% Pin-for-Pin compatible with better electrical specifications.

** **Similar Device:** Please consult the data sheet to determine the suitability of the replacement for specific applications.

† Consult factory for guaranteed TC devices.

SILICON GEN P/N	LTC DIRECT REPL
SG337	LM337
	LT337A*
	LT1033C**
SG338	LM338
	LT338A*
SG350	LM350
	LT350A*
SG1524	SG1524
	LT1524*
SG1525A	SG1525A
	LT1525A*
SG1526	LT1526
SG1527A	SG1527A
	LT1527A*
SG3524	SG3524
	LT3524*
SG3525A	SG3525A
	LT3525A*
SG3526	LT3526
SG3527A	SG3527A
	LT3527A*

TEXAS INSTRUMENTS

TI P/N	LTC DIRECT REPL
LM101A	LM101A
LM107	LM107
LM111	LM111
	LT111A*
	LT1011M*
LM124	LT1014M*
LM148	LT1014M*
LM158	LT1013M*
LM311	LM311
	LT311A*
	LT1011C*
LM317KC	LM317T
	LT317AT*
LM318	LM318
	LT318A*
LM323	LM323
	LT323A*
LM350	LM350
	LT350A*
MC1558	LT1013M*
OP07/714C	OP07C
	LT1001C*
OP07/714D	OP07D
	LT1001C*
OP07/714E	OP07E
	LT1001C*
SG1524	SG1524
	LT1524*
SG1525A	SG1525A
	LT1525A*
SG3524	SG3524
	LT3524*
SG3525A	SG3525A
	LT3525A*

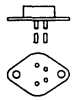
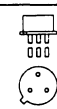
UNITRODE

UNITRODE P/N	LTC DIRECT REPL
UC117	LM117
	LT117A*
UC137	LM137
	LT137A*
	LT1033M**
UC150	LM150
	LT150A*
UC317	LM317
	LT317A*
UC337	LM337
	LT337A*
	LT1033C**
UC350	LM350
	LT350A*
UC1524	SG1524
	LT1524*
UC1525A	SG1525A
	LT1525A*
UC1527A	SG1527A
	LT1527A*
UC3524	SG3524
	LT3524*
UC3525A	SG3525A
	LT3525A*
UC3527A	SG3527A
	LT3527A*

* **LTC Improved Replacement:** 100% Pin-for-Pin compatible with better electrical specifications.

** **Similar Device:** Please consult the data sheet to determine the suitability of the replacement for specific applications.

† Consult factory for guaranteed TC devices.

	LTC	NSC	SIG	FSC	MOT	TI	SG	AMD	RAYTH	PMI
 Plastic Dip 8-Lead	N8	N N-8	N	T	P1	P	M	P-8	P,NB	P
 14, 16, 18 and 20 Lead	N	N N-14	N	P	P2	N NE NG	N	P-14 P-16	P,N	P
 TO-220 3 Lead	T	T	—	U	T	KC	P	—	—	—
 TO-220 5 Lead	T	T	—	U	—		P	—	—	—
 Side Brazed Hermetic DIP 8-Lead	D-8	D	I	D	L	—	—	D-8	—	—
 Side Brazed Hermetic DIP 14, 16, 18 and 20 Lead	D	D	I	D	L	—	—	D-14 D-16 D-18	—	YB QB XB
 TO-92	Z	Z	—	W	P	LP	—	—	—	—
 TO-5, TO-39, TO-96, TO-99, TO-100 and TO-101	H	H	—	H	G H	—	T	H	T H	H J K
 Ceramic DIP 8-Lead	J8	J J-8	F	R	U	JG	Y	D-8	DE	Z
 Ceramic DIP 14, 16, 18 and 20 Lead	J	J J-14	F	D	L	J	J	D-14 D-16	DB DC J	Y Q X
 TO-3 (Steel)	K	K STEEL	—	K	K	—	K	—	—	—
 (Aluminum)	—	K	—	K	K	—	—	—	—	—
 TO-3 4 Lead	K	K	—	K	—	—	K	—	—	—
 TO-46 2, 3, 4 Lead TO-52 3 Lead	H	H	—	—	—	—	T	—	—	H J K
PROPRIETARY DEVICE PREFIXES	LT LTC	LF LH LM LP MF	NE SE	μA	MC	TL	SG	AM	RM RC	OP REF BUF

SECTION 2—OPERATIONAL AMPLIFIERS

SECTION 2—OPERATIONAL AMPLIFIERS

MILITARY

Part Number	Electrical Characteristics							Important Features
	V_{OS} Max (μV)	TC V_{OS} (μV/°C)	I_B Max (NA)	A_{VOL} Min (V/mV)	Slew Rate Min (V/μS)	Noise Max 10Hz (nV/$\sqrt{Hz}$)	Packages Available	
LT1001AM	15	0.6	2.0	450	0.15	18	H, J8	Extremely Low Offset Voltage Low Noise, Low Drift
LT1001M	60	1.0	3.8	400	0.15	18	H, J8	
LT1002AM	60	0.9	3.0	400	0.15	20	J	Dual, Matched LT1001 High CMRR, PSRR Matching
LT1002M	100	1.3	4.5	350	0.15	20	J	
LT1007AM	25	0.6	35	7000	1.7	4.5	H, J8	Extremely Low Noise, Low Drift
LT1007M	60	1.0	55	5000	1.7	4.5	H, J8	
LT1008M	120	1.5	0.1	200	0.1	30	H	Low Bias Current, Low Power
LT1010M	90mV	0.6mV/°C †	150μA	0.995	75	90†	H, K	High Speed Buffer. Drives ± 10V into 75Ω.
LT1012M	35	1.5	0.1	200	0.1	30	H	Low V_{OS}, Low Power
LT1013AM	150	2.0	20	1500	0.2	24†	H, J8	Precision Dual Op Amp in 8-Pin Package
LT1013M	300	2.5	30	1200	0.2	24†	H, J8	
LT1014AM	180	2.0	20	1500	0.2	24†	J	Precision Quad Op Amp in 14-Pin Package
LT1014M	300	2.5	30	1200	0.2	24†	J	
LT1022AM	250	5.0	0.05 |	150	23	50	H	Very High Speed JFET Input Op Amp With Very Good DC Specs.
LT1022M	600	9.0	0.05 |	120	18	60	H	
LT1037AM	25	0.6	35	7000	11	4.5	H, J8	Extremely Low Noise, High Speed
LT1037M	60	1.0	55	5000	11	4.5	H, J8	
LT1055AM	150	4	0.05	150	10	50	H	Lowest Offset, JFET Input Op Amp Combines High Speed and Precision
LT1055M	400	8	0.05	120	7.5	60	H	
LT1056AM	180	4	0.05	150	12	50	H	
LT1056M	450	8	0.05	120	9	60	H	
LTC1052M	5	0.05	30	1000	3†	0.5μVp-p**	H	Chopper, Stabilized Low Noise
LF155A	2000	5	0.05	75	5	25†*	H	JFET Inputs, Low I Bias, No Phase Reversal, Guaranteed TC V_{os} on all Grades
LF155	3500	15	0.10	50	5	25†*	H	
LF156A	2000	5	0.05	75	10	15†*	H	
LF156	3500	15	0.10	50	9	15†*	H	
LH2108A	500	5.0	2	40	0.1	30†	D	Dual, Low Bias Current, Side Brazed Package
LH2108	2000	15.0	2	25	0.1	30†	D	
LM10	2000	2†	20	120	—	50†	H, J8	On-Chip Reference Operates with + 1.2V Single Battery
LM101A	2000	15	75	25	0.3	28†	H, J8	Uncompensated Gen. Purp.
LM107	2000	15	75	25	0.3	28†	H, J8	Compensated Gen. Purp.
LM108A	500	5	2	40	0.1	30†	H	Low Bias Current, Low Supply Current
LM108	2000	15	3	25	0.1	30†	H	
LM118	4000		250	25	50	42†	H	High Speed, 15MHz
LT118A	1000		250	200	50	42†	H, J8	High Speed, 15MHZ
OP-05A	150	0.9	2	300	0.1	18	H, J8	Low Noise, Low Offset Drift With Time
OP-05	500	2.0	3	200	0.1	18	H, J8	
OP-07A	25	0.6	2	300	0.1	18	H, J8	Low Initial Offset, Low Noise, Low Drift
OP-07	75	1.3	3	200	0.1	18	H, J8	
OP-15A	500	5	0.05	100	10	20†*	H	Precision JFET Input, Low I Bias, No Phase Reversal
OP-15B	1000	10	0.1	75	7.5	20†*	H	
OP-15C	3000	15	0.2	50	5	20†*	H	
OP-16A	500	5	0.5	100	18	20†*	H	Precision JFET Input, High Speed, No Phase Reversal
OP-16B	1000	10	0.1	75	12	20†*	H	
OP-16C	3000	15	0.2	50	9	20†*	H	
OP-27A	25	0.6	40	1000	1.7	5.5	H, J8	Very Low Noise, Unity Gain Stable
OP-27C	100	1.8	80	700	1.7	8.0	H, J8	
OP-37A	25	0.6	40	1000	11	5.5	H, J8	Very Low Noise, Stable For Gains ≥5
OP-37C	100	1.8	80	700	11	8.0	H, J8	
OP-227A	80	1.0	40	3000	1.7	6	J	Dual Matched OP-27
OP-227C	180	1.8	80	2000	1.7	9	J	
OP-237A	80	1.0	40	3000	10	6	J	Dual Matched OP-37
OP-237C	180	1.8	80	2000	10	9	J	

† Typical Spec *100 Hz Noise **DC to 1 Hz Noise

COMMERCIAL

Part Number	Electrical Characteristics							Important Features
	V_{OS} Max (μV)	TC V_{OS} (μV/°C)	I_B Max (NA)	A_{VOL} Min (V/mV)	Slew Rate Min (V/μS)	Noise Max 10Hz (nV/$\sqrt{Hz}$)	Packages Available	
LT1001AC	25	0.6	2.0	450	0.15	18	H, J8, N8	Extremely Low Offset Voltage Low Noise, Low Drift
LT1001C	60	1.0	3.8	400	0.15	18	H, J8, N8	
LT1002AC	60	0.9	3.0	400	0.15	20	J, N	Dual, Matched LT1001 High CMRR, PSRR Matching
LT1002C	100	1.3	4.5	350	0.15	20	J, N	
LT1007AC	25	0.6	35	7000	1.7	4.5	H, J8, N8	Extremely Low Noise, Low Drift
LT1007C	60	1.0	55	5000	1.7	4.5	H, J8, N8	
LT1008C	120	1.5	0.1	200	0.1	30	H, N8	Low Bias Current, Low Power
LT1010C	100mV	0.6mV/°C†	250μA	0.995	75	90†	H, K, T	High Speed Buffer. Drives ± 10V into 75Ω.
LT1012C	50	1.5	0.15	200	0.1	30	H, N8	Low V_{OS}, Low Power
LT1013AC	150	2.0	20	1500	0.2	24†	H, J8	Precision Dual Op Amp in 8-Pin Package
LT1013C	300	2.5	30	1200	0.2	24†	H, J8, N8	
LT1013D	800	5.0	30	1200	0.2	24†	N8	
LT1014AC	180	2.0	20	1500	0.2	24†	J	Precision Quad Op Amp in 14-Pin Package
LT1014C	300	2.5	30	1200	0.2	24†	J, N	
LT1014D	800	5.0	30	1200	0.2	24†	N	
LT1022AC	250	5.0	0.05	150	23	50	H	Very High Speed JFET Input Op Amp With Very Good DC Specs.
LT1022CH	600	9.0	0.05	120	18	60	H	
LT1022CN8	1000	15.0	0.05	100	18	60	N8	
LT1037AC	25	0.6	35	7000	11	4.5	H, J8, N8	Extremely Low Noise, High Speed
LT1037C	60	1.0	55	5000	11	4.5	H, J8, N8	
LT1055AC	150	4	0.05	150	10	50	H	Lowest Offset, JFET Input Op Amp Combines High Speed and Precision
LT1055C	400	8	0.05	120	7.5	60	H	
LT1055CN8	700	12	0.05	120	7.5	60	N8	
LT1056AC	180	4	0.05	150	12	50	H	
LT1056C	450	8	0.05	120	9	60	H	
LT1056CN8	800	12	0.05	120	9	60	N8	
LTC1052C	5	0.05	30	1000	3†	0.5μVp-p**	H, N8	Chopper Stabilized, Low Noise
LTC7652C	5	0.05	30	1000	3†	0.5μVp-p**	H, N8	
LF355	8000	25	0.20	40	2.5	25†*	H, N8	JFET Inputs, Low I Bias, No Phase Reversal, Guaranteed TC V_{OS} on All Grades
LF355A	2000	5	0.05	75	5	25†*	H, N8	
LF356	8000	25	0.20	40	4	15†*	H, N8	
LF356A	2000	5	0.05	75	10	15†*	H, N8	
LM10B	2000	2†	20	120	—	50†	H, J8	On-Chip Reference. Operates with + 1.2V Single Battery
LM10BL	2000	2†	20	60	—	50†	H, J8	
LM10C	4000	5†	30	80	—	50†	H, J8, N8	
LM10CL	4000	5†	30	40	—	50†	H, J8, N8	
LM301A	7500	30	250	15	0.3	28†	H, J8	Uncompensated Gen. Purp.
LM307	7500	30	250	15	0.3	28†	H, J8	Compensated Gen. Purp.
LM308A	500	5	7	60	0.1	30†	H, N8	Low Bias, Supply Current
LT318A	1000		250	200	50	42†	H, J8, N8	High Speed, 15MHZ
LM318	10000		500	25	50	42†	H, J8, N8	High Speed, 15MHz
OP-05C	1300	4.5	7	120	0.1	20	H, J8, N8	Low Noise, Low Offset Drift With Time
OP-05E	500	2.0	4	200	0.1	18	H, J8, N8	
OP-07C	150	1.8	7	120	0.1	20	H, J8, N8	Low Initial Offset, Low Noise, Low Drift
OP-07E	75	1.3	4	200	0.1	18	H, J8, N8	
OP-15E	500	5	0.05	100	10	20†*	H, N8	Precision JFET Input, Low I Bias, No Phase Reversal
OP-15F	1000	10	0.1	75	7.5	20†*	H, N8	
OP-15G	3000	15	0.2	50	5	20†*	H, N8	
OP-16E	500	5	0.05	100	18	20†*	H, N8	Precision JFET Input, High Speed, No Phase Reversal
OP-16F	1000	10	0.1	75	12	20†*	H, N8	
OP-16G	3000	15	0.2	50	9	20†*	H, N8	
OP-27E	25	0.6	40	1000	1.7	5.5	H, J8, N8	Very Low Noise, Unity Gain Stable
OP-27G	100	1.8	80	700	1.7	8.0	H, N8	

† Typical Spec * 100 Hz Noise ** DC to 1 Hz Noise

COMMERCIAL

Part Number	Electrical Characteristics							Important Features
	V_{OS} Max (μV)	TC V_{OS} (μV/°C)	I_B Max (NA)	A_{VOL} Min (V/mV)	Slew Rate Min (V/μS)	Noise Max 10Hz (nV/$\sqrt{Hz}$)	Packages Available	
OP-37E	25	0.6	40	1000	11	5.5	H, J8, N8	Very Low Noise, Stable For Gains $\geq$5
OP-37G	100	1.8	80	700	11	8.0	H, N8	
OP-227E	80	1.0	40	3000	1.7	6	J, N	Dual Matched OP-27
OP-227G	180	1.8	80	2000	1.7	9	J, N	
OP-237E	80	1.0	40	3000	10	6	J, N	Dual Matched OP-37
OP-237G	180	1.8	80	2000	10	9	J, N	

† Typical Spec *100 Hz Noise **DC to 1 Hz Noise

SELECTION BY DESIGN PARAMETER

Max Input Offset Voltage (T_A = 25°C)

$\leq$15μV	$\leq$25μV	$\leq$75μV	$\leq$150μV	$\leq$1mV	$\leq$5mV	$\leq$10mV
LT1001AM LTC7652 LTC1052	LT1001AC LT1007A LT1037A OP-07A OP-27A OP-27E OP-37A OP-37E	LT1001 LT1002A LT1007 LT1012 LT1037 OP-07E OP-07	LT1002 LT1008 LT1013A LT1055AM LT1055AC OP-05A OP-07C,D OP-27C OP-37C OP-227A, E OP-237A, E	LT1013 LT1014 LT1014A LT1022 ALL LT1055C LT1055M LT1056AM LT1056AC LT1056M LT1056C LH2108A LM108A LM308A OP-05 OP-05E OP-15A, E OP-15B, F OP-16A, E OP-16B, F	LT118A LT318A LF155A LF155 LF156A LF156 LF355A LF355 LH2108 LM10 LM10B, BL LM10C, CL LM101A LM107 LM108 LM118 OP-05C OP-15C, G OP-16C, G	LM301A LM307 LM308 LM318

Max Input Bias Current (T_j = 25°C)

$\leq$0.2nA	$\leq$3nA	$\leq$5nA	$\leq$10nA	$\leq$50nA	$\leq$100nA	>200nA
LT1008 LT1012 LT1022 ALL LT1055 ALL LT1056 ALL LF155 ALL LF156 ALL LTC7652 LTC1052 OP-15 ALL OP-16 ALL	LT1001A LT1002A LM108 LM108A OP-05A OP-05 OP-07A OP-07	LT1001 LT1002 OP-05E OP-07E	OP-05C OP-07 LM308A	LT1007A LT1013A LT1013 LT1014A LT1014 LT1037 LM10(ALL) OP-27A, E OP-37A, E OP-227A, E OP-237A, E	LT1007 LT1037 LM101A LM107 OP-27C, G OP-37C, G OP-227C, G OP-237C, G	LT118A LT318A LM301A LM307 LM118 LM318

SELECTION BY DESIGN PARAMETER

Typ Equivalent Input Noise Voltage
per $\sqrt{Hz}$, f = 10 Hz R_S = 100Ω

≤5nV/$\sqrt{Hz}$	≤25nV/$\sqrt{Hz}$
LT1007 ALL LT1037 ALL	LT1001 ALL LT1002 ALL LT1008 LT1012 LT1013 ALL LT1014 ALL LT1022 ALL LTC1052 *LT1055 ALL *LT1056 ALL LTC7652 *LF 155 ALL *LF 355 ALL *LF 156 ALL *LF 356 ALL OP-05 ALL OP-07 ALL *OP-15 ALL *OP-16 ALL OP-27 ALL OP-37 ALL OP-227 ALL OP-237 ALL

* 100 Hz Noise

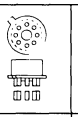
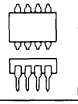
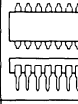
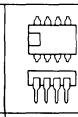
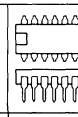
Typ Slew Rate

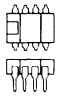
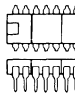
≤1V/μS	≥2V/μS	≥11V/μS	≥50V/μS
LT1001 ALL LT1002 ALL LT1008 LT1012 LT1013 ALL LT1014 ALL LH2108 ALL OP-05 OP-07 LM101A/301A LM107/307 LM108/308 LM108A/308A	LT1007 ALL LT1055 ALL LT1056M LT1056C OP-27 ALL OP-15 ALL OP-16C, G OP-227 ALL LF155 ALL LF355 ALL LF156 ALL LF356 ALL	LT1022 ALL LT1037 ALL LT1056A OP-37 ALL OP-16A, B OP-16E, F OP-237 ALL	LT118A/318A LM118/318 LT1010

Gain

≥15 $\frac{V}{mV}$	≥50 $\frac{V}{mV}$	≥200 $\frac{V}{mV}$	≥1000 $\frac{V}{mV}$
LM301A LM307 LM308 LM318	LT1022 ALL LT1055 ALL LT1056 ALL LM101A LM107 LM108 LM118 LM10	LT1001 LT1002 LT1008 LT1012 LT118A LT318A OP-05 OP-07	LT1007 LT1013 LT1014 LT1037 OP-27 OP-37 OP-227 OP-237 LTC1052 LTC7652

Packages

				
H TO-5 8 LEAD 10 LEAD	J8 HERMETIC DIP 8 LEAD	J HERMETIC DIP 14 LEAD 16 LEAD 18 LEAD	N8 PLASTIC DIP 8 LEAD	N PLASTIC DIP 14 LEAD 16 LEAD 18 LEAD

	
D8 HERMETIC DIP 8 LEAD	D HERMETIC DIP 14 LEAD 16 LEAD 18 LEAD

Precision Operational Amplifier

FEATURES

- *Guaranteed* Low Offset Voltage
  - LT1001AM 15μV max
  - LT1001C 60μV max
- *Guaranteed* Low Drift
  - LT1001AM 0.6μV/°C max
  - LT1001C 1.0μV/°C max
- *Guaranteed* Low Bias Current
  - LT1001AM 2nA max
  - LT1001C 4nA max
- *Guaranteed* CMRR
  - LT1001AM 114dB min
  - LT1001C 110dB min
- *Guaranteed* PSRR
  - LT1001AM 110dB min
  - LT1001C 106dB min
- Low Power Dissipation
  - LT1001AM 75mW max
  - LT1001C 80mW max
- Low Noise 0.3μV_{p-p}

APPLICATIONS

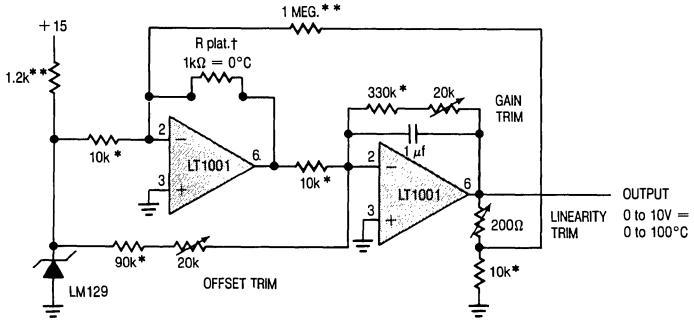
- Thermocouple amplifiers
- Strain gauge amplifiers
- Low level signal processing
- High accuracy data acquisition

DESCRIPTION

The LT1001 significantly advances the state-of-the-art of precision operational amplifiers. In the design, processing, and testing of the device, particular attention has been paid to the optimization of the entire distribution of several key parameters. Consequently, the specifications of the lowest cost, commercial temperature device, the LT1001C, have been dramatically improved when compared to equivalent grades of competing precision amplifiers.

Essentially, the input offset voltage of all units is less than 50μV (see distribution plot below). This allows the LT1001AM/883 to be specified at 15μV. Input bias and offset currents, common-mode and power supply rejection of the LT1001C offer guaranteed performance which were previously attainable only with expensive, selected grades of other devices. Power dissipation is nearly halved compared to the most popular precision op amps, without adversely affecting noise or speed performance. A beneficial by-product of lower dissipation is decreased warm-up drift. Output drive capability of the LT1001 is also enhanced with voltage gain guaranteed at 10 mA of load current. For similar performance in a dual precision op amp, with guaranteed matching specifications, see the LT1002. Shown below is a platinum resistance thermometer application.

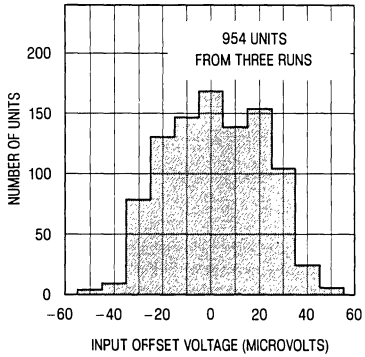
Linearized Platinum Resistance Thermometer with ±0.025°C Accuracy Over 0 to 100°C



* ULTRONIX 105A WIREWOUND
** 1% FILM
† PLATINUM RTD 118MF (ROSEMOUNT, INC.)

‡ Trim sequence: trim offset (0°C = 1000.0Ω), trim linearity (35°C = 1138.7Ω), trim gain (100°C = 1392.6Ω). Repeat until all three points are fixed with ±.025°C.

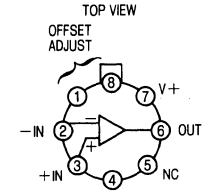
Typical Distribution of Offset Voltage $V_S = \pm 15V$, $T_A = 25°C$



ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... ±22V
Differential Input Voltage ..... ±30V
Input Voltage ..... ±22V
Output Short Circuit Duration ..... Indefinite
Operating Temperature Range
LT1001AM/LT1001M ..... −55°C to 150°C
LT1001AC/LT1001C ..... 0°C to 125°C
Storage: All Devices ..... −65°C to 150°C
Lead Temperature (Soldering, 10 sec.) ..... 300°C

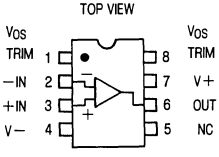
PACKAGE/ORDER INFORMATION



H PACKAGE
METAL CAN

ORDER PART NUMBER

LT1001AMH/883
LT1001MH
LT1001ACH
LT1001CH



J8 PACKAGE
8 PIN HERMETIC DIP

N8 PACKAGE
8 PIN PLASTIC DIP

LT1001AMJ8/883
LT1001MJ8
LT1001ACJ8
LT1001CJ8

LT1001ACN8
LT1001CN8

ELECTRICAL CHARACTERISTICS

$V_S = \pm 15V$, $T_A = 25°C$, unless otherwise noted

SYMBOL	PARAMETER	CONDITIONS	LT1001AM/883 LT1001AC MIN	LT1001AM/883 LT1001AC TYP	LT1001AM/883 LT1001AC MAX	LT1001M/LT1001C MIN	LT1001M/LT1001C TYP	LT1001M/LT1001C MAX	UNITS
V_{OS}	Input Offset Voltage	Note 1 LT1001AM/883		7	15		18	60	μV
		LT1001AC		10	25				
$\frac{\Delta V_{OS}}{\Delta \text{ Time}}$	Long Term Input Offset Voltage Stability	Notes 2 and 3		0.2	1.0		0.3	1.5	μV/month
I_{OS}	Input Offset Current			0.3	2.0		0.4	3.8	nA
I_b	Input Bias Current			±0.5	±2.0		±0.7	±4.0	nA
e_n	Input Noise Voltage	0.1Hz to 10Hz (Note 2)		0.3	0.6		0.3	0.6	μV_{p-p}
e_n	Input Noise Voltage Density	f_o = 10Hz (Note 5)		10.3	18.0		10.5	18.0	$nV\sqrt{Hz}$
		f_o = 1000Hz (Note 2)		9.6	11.0		9.8	11.0	
A_{VOL}	Large Signal Voltage Gain	$R_L \geq 2k\Omega$, $V_o = \pm 12V$	450	800		400	800		V/mV
		$R_L \geq 1k\Omega$, $V_o = \pm 10V$	300	500		250	500		
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm 13V$	114	126		110	126		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 3V$ to $\pm 18V$	110	123		106	123		dB
R_{in}	Input Resistance Differential Mode	(Note 4)	30	100		15	80		MΩ
	Input Voltage Range		±13	±14		±13	±14		V
V_{OUT}	Maximum Output Voltage Swing	$R_L \geq 2k\Omega$	±13	±14		±13	±14		V
		$R_L \geq 1k\Omega$	±12	±13.5		±12	±13.5		
S_R	Slew Rate	$R_L \geq 2k\Omega$ (Note 4)	0.1	0.25		0.1	0.25		V/μs
GBW	Gain-Bandwidth Product	(Note 4)	0.4	0.8		0.4	0.8		MHz
P_d	Power Dissipation	No load		46	75		48	80	mW
		No load, $V_s = \pm 3V$		4	6		4	8	

See Notes on page 3.

ELECTRICAL CHARACTERISTICS $V_S = \pm 15V$, $-55°C \leq T_A \leq 125°C$, unless otherwise noted

SYMBOL	PARAMETER	CONDITIONS		LT1001AM/883 MIN	LT1001AM/883 TYP	LT1001AM/883 MAX	LT1001M MIN	LT1001M TYP	LT1001M MAX	UNITS
V_{OS}	Input Offset Voltage		●		30	60		45	160	μV
$\frac{\Delta V_{OS}}{\Delta \text{ Temp}}$	Average Offset Voltage Drift		●		0.2	0.6		0.3	1.0	μV/°C
I_{OS}	Input Offset Current		●		0.8	4.0		1.2	7.6	nA
I_B	Input Bias Current		●		±1.0	±4.0		±1.5	±8.0	nA
A_{VOL}	Large Signal Voltage Gain	$R_L \geq 2k\Omega$, $V_O = \pm 10V$	●	300	700		200	700		V/mV
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm 13V$	●	110	122		106	120		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 3$ to $\pm 18V$	●	104	117		100	117		dB
	Input Voltage Range		●	±13	±14		±13	±14		V
V_{OUT}	Output Voltage Swing	$R_L \geq 2k\Omega$	●	±12.5	±13.5		±12.0	±13.5		V
P_d	Power Dissipation	No load	●		55	90		60	100	mW

$V_S = \pm 15V$, $0°C \leq T_A \leq 70°C$, unless otherwise noted

SYMBOL	PARAMETER	CONDITIONS		LT1001AC MIN	LT1001AC TYP	LT1001AC MAX	LT1001C MIN	LT1001C TYP	LT1001C MAX	UNITS
V_{OS}	Input Offset Voltage		●		20	60		30	110	μV
$\frac{\Delta V_{OS}}{\Delta \text{ Temp}}$	Average Offset Voltage Drift		●		0.2	0.6		0.3	1.0	μV/°C
I_{OS}	Input Offset Current		●		0.5	3.5		0.6	5.3	nA
I_B	Input Bias Current		●		±0.7	±3.5		±1.0	±5.5	nA
A_{VOL}	Large Signal Voltage Gain	$R_L \geq 2k\Omega$, $V_O = \pm 10V$	●	350	750		250	750		V/mV
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm 13V$	●	110	124		106	123		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 3V$ to $\pm 18V$	●	106	120		103	120		dB
	Input Voltage Range		●	±13	±14		±13	±14		V
V_{OUT}	Output Voltage Swing	$R_L \geq 2k\Omega$	●	±12.5	±13.8		±12.5	±13.8		V
P_d	Power Dissipation	No load	●		50	85		55	90	mW

The ● denotes the specifications which apply over the full operating temperature range.

Note 1: Offset voltage for the LT1001AM/883 and LT1001AC are measured after power is applied and the device is fully warmed up. All other grades are measured with high speed test equipment, approximately 1 second after power is applied. The LT1001AM/883 receives 168 hr. burn-in at 125°C. or equivalent.

Note 2: This parameter is tested on a sample basis only.

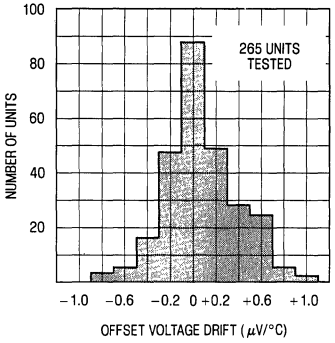
Note 3: Long Term Input Offset Voltage Stability refers to the averaged trend line of V_{os} versus Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{os} during the first 30 days are typically 2.5μV.

Note 4: Parameter is guaranteed by design.

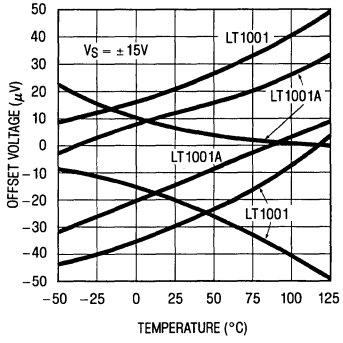
Note 5: 10Hz noise voltage density is sample tested on every lot. Devices 100% tested at 10Hz are available on request.

TYPICAL PERFORMANCE CHARACTERISTICS

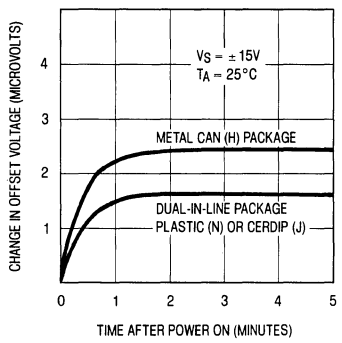
Typical Distribution of Offset Voltage Drift with Temperature



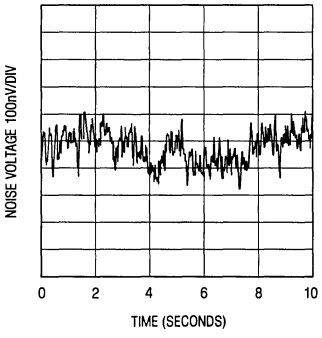
Offset Voltage Drift with Temperature of Representative Units



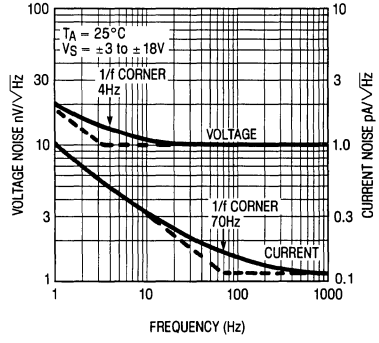
Warm-Up Drift



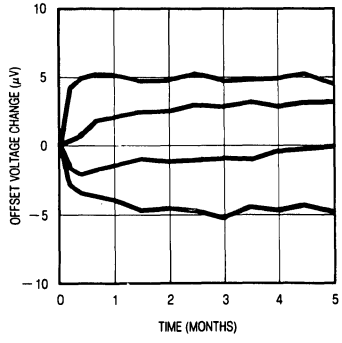
0.1Hz to 10Hz Noise



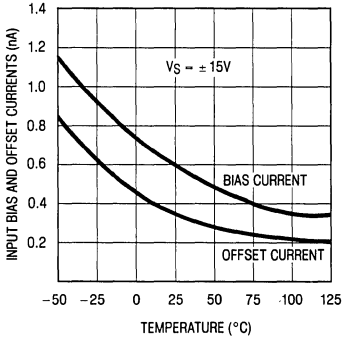
Noise Spectrum



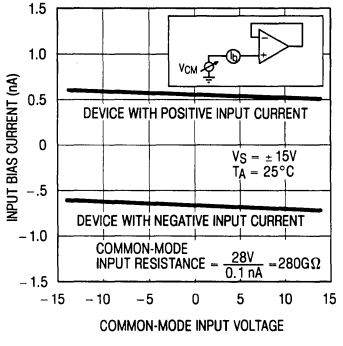
Long Term Stability of Four Representative Units



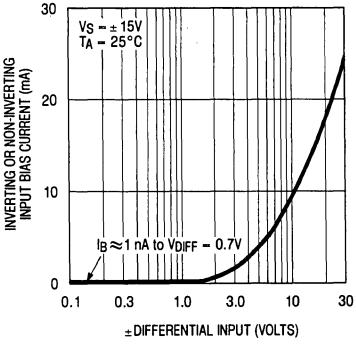
Input Bias and Offset Current vs Temperature



Input Bias Current Over the Common Mode Range

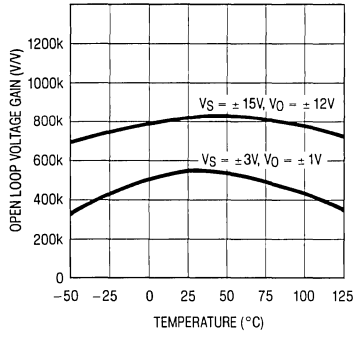


Input Bias Current vs. Differential Input Voltage

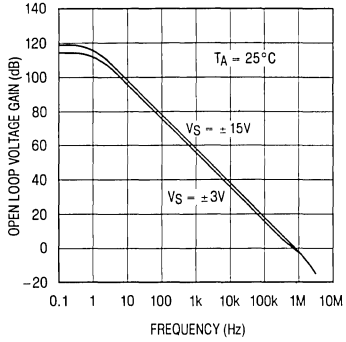


TYPICAL PERFORMANCE CHARACTERISTICS

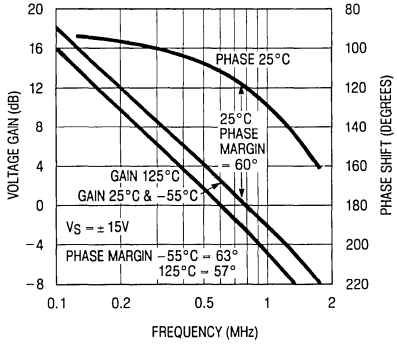
Open Loop Voltage Gain vs Temperature



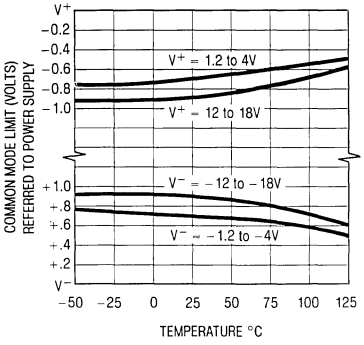
Open Loop Voltage Gain Frequency Response



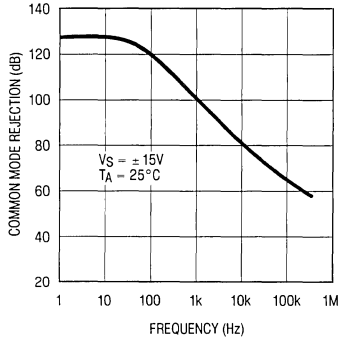
Gain, Phase Shift vs. Frequency



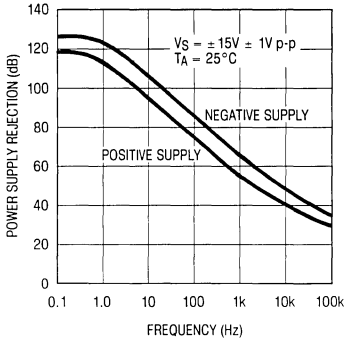
Common Mode Limit vs Temperature



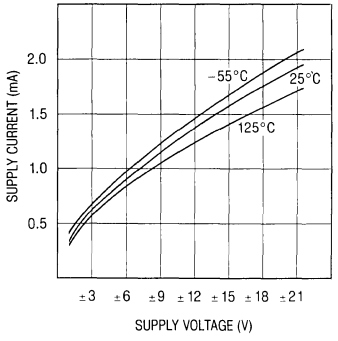
Common Mode Rejection Ratio vs Frequency



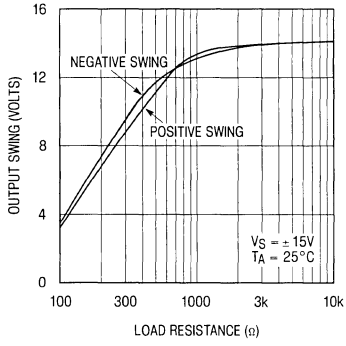
Power Supply Rejection Ratio vs Frequency



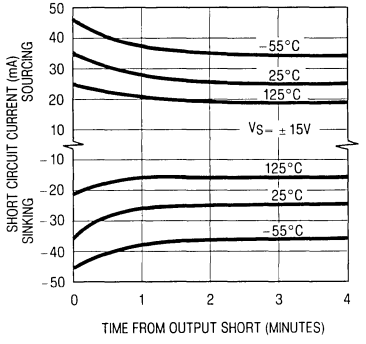
Supply Current vs Supply Voltage



Output Swing vs. Load Resistance

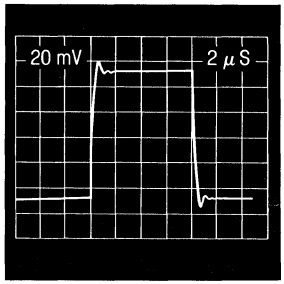


Output Short Circuit Current vs Time



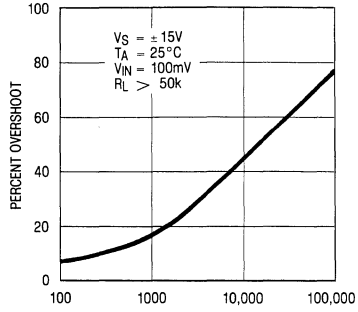
TYPICAL PERFORMANCE CHARACTERISTICS

Small Signal Transient Response

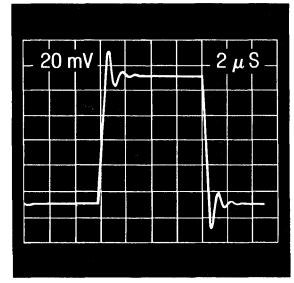


$A_V = +1$, $C_L = 50pF$

Voltage Follower Overshoot vs Capacitive Load

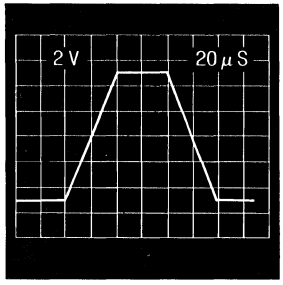


Small Signal Transient Response

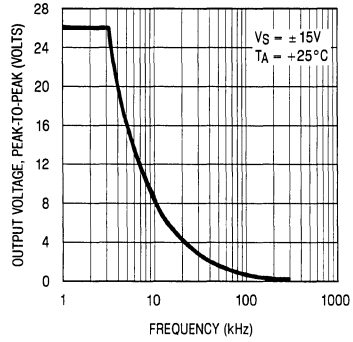


$A_V = +1$, $C_L = 1000pF$

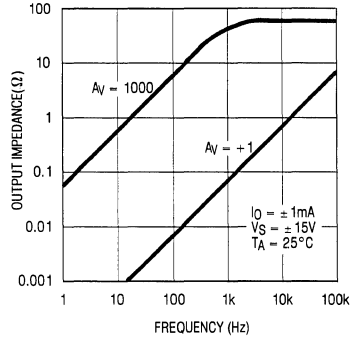
Large Signal Transient Response



Maximum Undistorted Output vs. Frequency



Closed Loop Output Impedance



APPLICATIONS INFORMATION

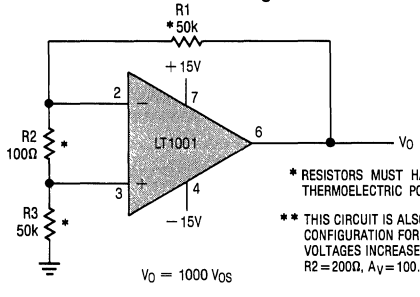
Application Notes and Test Circuits

The LT1001 series units may be inserted directly into OP-07, OP-05, 725, 108A or 101A sockets with or without removal of external frequency compensation or nulling components. The LT1001 can also be used in 741, LF156 or OP-15 applications provided that the nulling circuitry is removed.

The LT1001 is specified over a wide range of power supply voltages from ±3V to ±18V. Operation with lower supplies is possible down to ±1.2V (two Ni-Cad batteries). However, with ±1.2V supplies, the device is stable only in closed loop gains of +2 or higher (or inverting gain of one or higher).

Unless proper care is exercised, thermocouple effects caused by temperature gradients across dissimilar metals at the contacts to the input terminals, can exceed the inherent drift of the amplifier. Air currents over device leads should be minimized, package leads should be short, and the two input leads should be as close together as possible and maintained at the same temperature.

Test Circuit for Offset Voltage and its Drift with Temperature



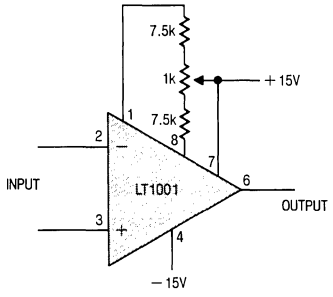
* RESISTORS MUST HAVE LOW THERMOELECTRIC POTENTIAL.

** THIS CIRCUIT IS ALSO USED AS THE BURN-IN CONFIGURATION FOR THE LT1001, WITH SUPPLY VOLTAGES INCREASED TO ±20V, R1 = R3 = 10k, R2 = 200Ω, A_V = 100.

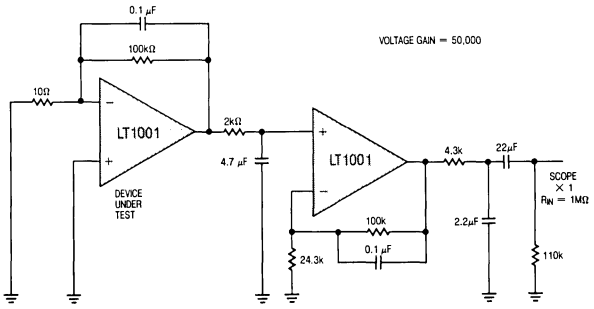
Offset Voltage Adjustment

The input offset voltage of the LT1001, and its drift with temperature, are permanently trimmed at wafer test to a low level. However, if further adjustment of Vos is necessary, nulling with a 10k or 20k potentiometer will not degrade drift with temperature. Trimming to a value other than zero creates a drift of (Vos/300) μV/°C, e.g. if Vos is adjusted to 300 μV, the change in drift will be 1 μV/°C. The adjustment range with a 10k or 20k pot is approximately $\pm$2.5mV. If less adjustment range is needed, the sensitivity and resolution of the nulling can be improved by using a smaller pot in conjunction with fixed resistors. The example below has an approximate null range of $\pm$ 100 μV.

Improved Sensitivity Adjustment



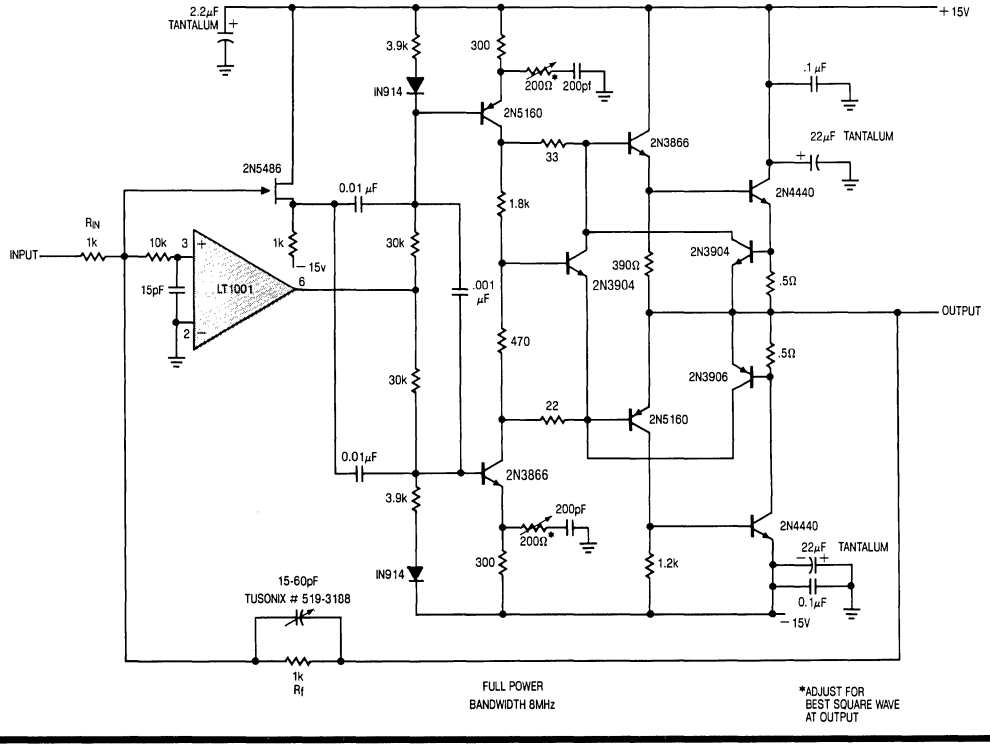
0.1Hz to 10Hz Noise Test Circuit



(Peak to Peak noise measured in 10 Sec interval)

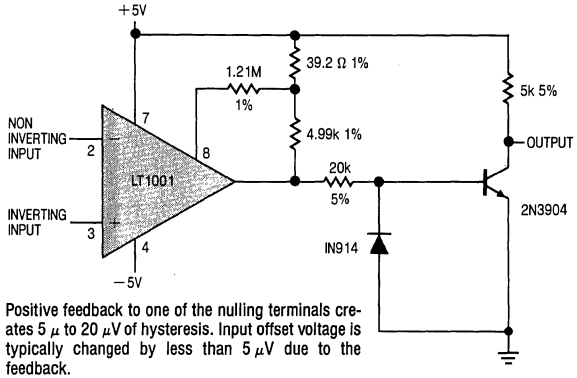
The device under test should be warmed up for three minutes and shielded from air currents.

DC Stabilized 1000v/μsec Op Amp



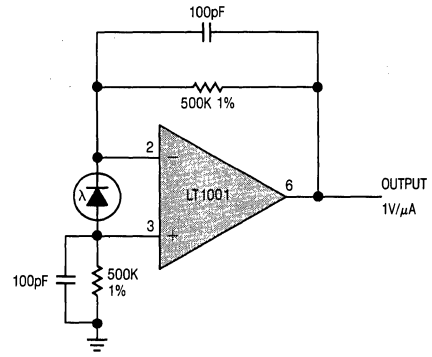
TYPICAL APPLICATIONS

Microvolt Comparator with TTL Output

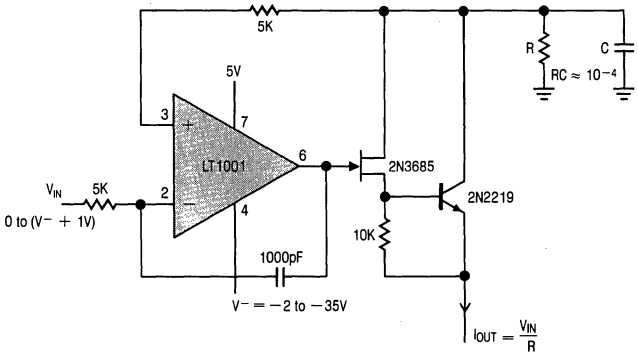


Positive feedback to one of the nulling terminals creates 5 μ to 20 μV of hysteresis. Input offset voltage is typically changed by less than 5 μV due to the feedback.

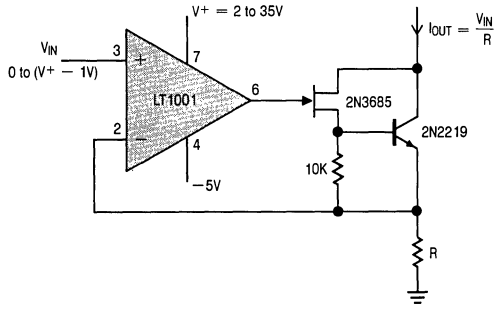
Photodiode Amplifier



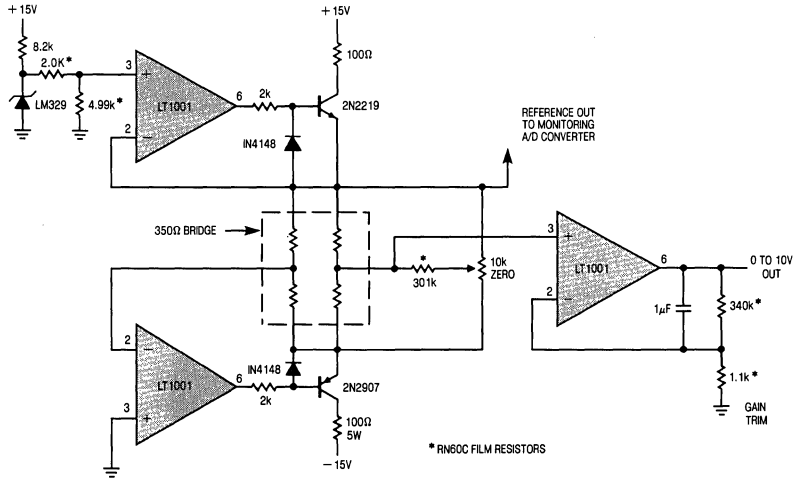
Precision Current Source



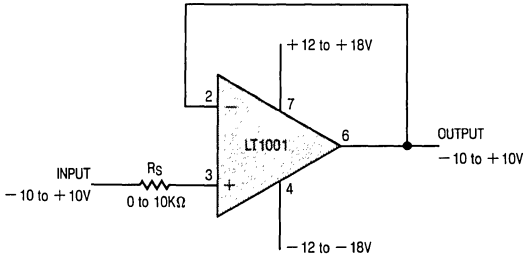
Precision Current Sink



Strain Gauge Signal Conditioner with Bridge Excitation



Large Signal Voltage Follower With 0.001% Worst-Case Accuracy

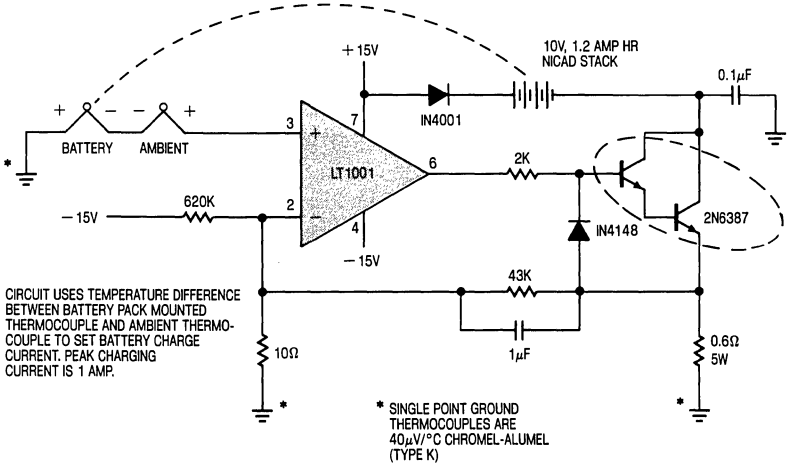


The voltage follower is an ideal example illustrating the overall excellence of the LT1001. The contributing error terms are due to offset voltage, input bias current, voltage gain, common-mode and power-supply rejections. Worst-case summation of guaranteed specifications is tabulated below.

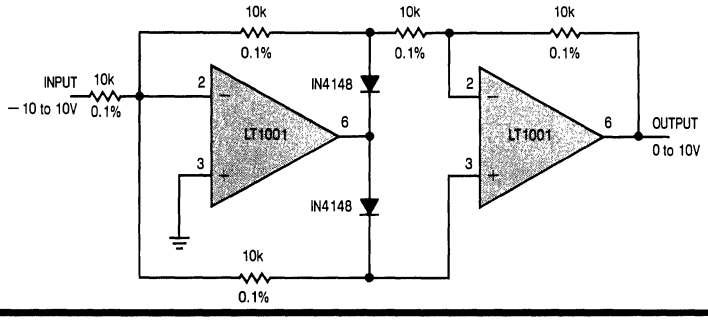
OUTPUT ACCURACY

Error	LT1001AM /883 25°C Max.	LT1001C 25°C Max.	LT1001AM /883 −55 to 125°C Max.	LT1001C 0 to 70°C Max.
Offset Voltage	15μV	60μV	60μV	110μV
Bias Current	20μV	40μV	40μV	55μV
Common-Mode Rejection	20μV	30μV	30μV	50μV
Power Supply Rejection	18μV	30μV	36μV	42μV
Voltage Gain	22μV	25μV	33μV	40μV
Worst-case Sum	95μV	185μV	199μV	297μV
Percent of Full Scale (=20V)	0.0005%	0.0009%	0.0010%	0.0015%

Thermally Controlled Nicad Charger

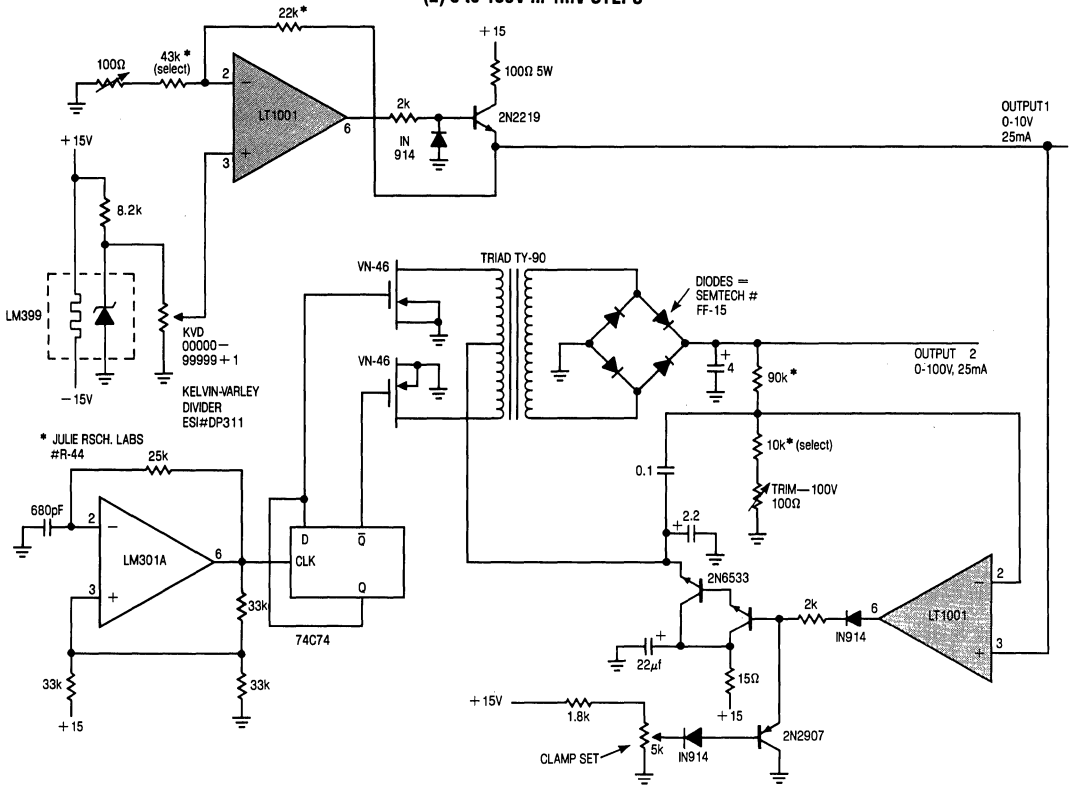


Precision Absolute Value Circuit



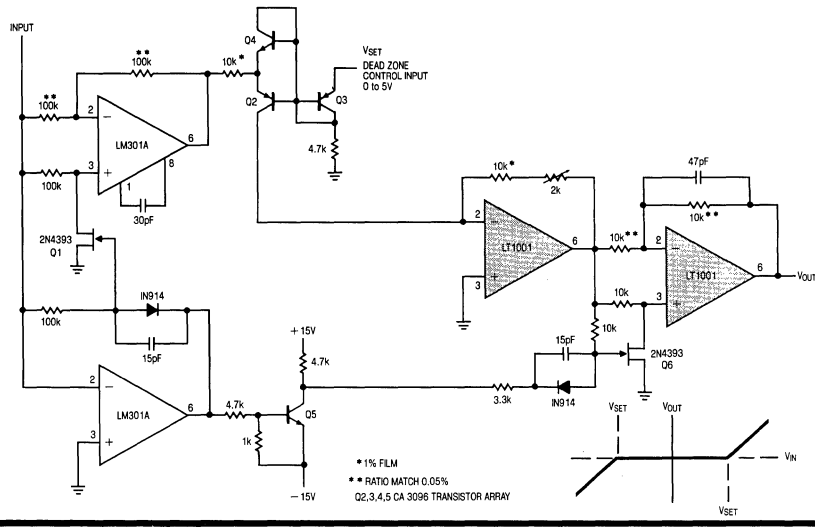
Precision Power Supply with Two Outputs

(1) 0 to 10V in 100μV STEPS
(2) 0 to 100V in 1mV STEPS

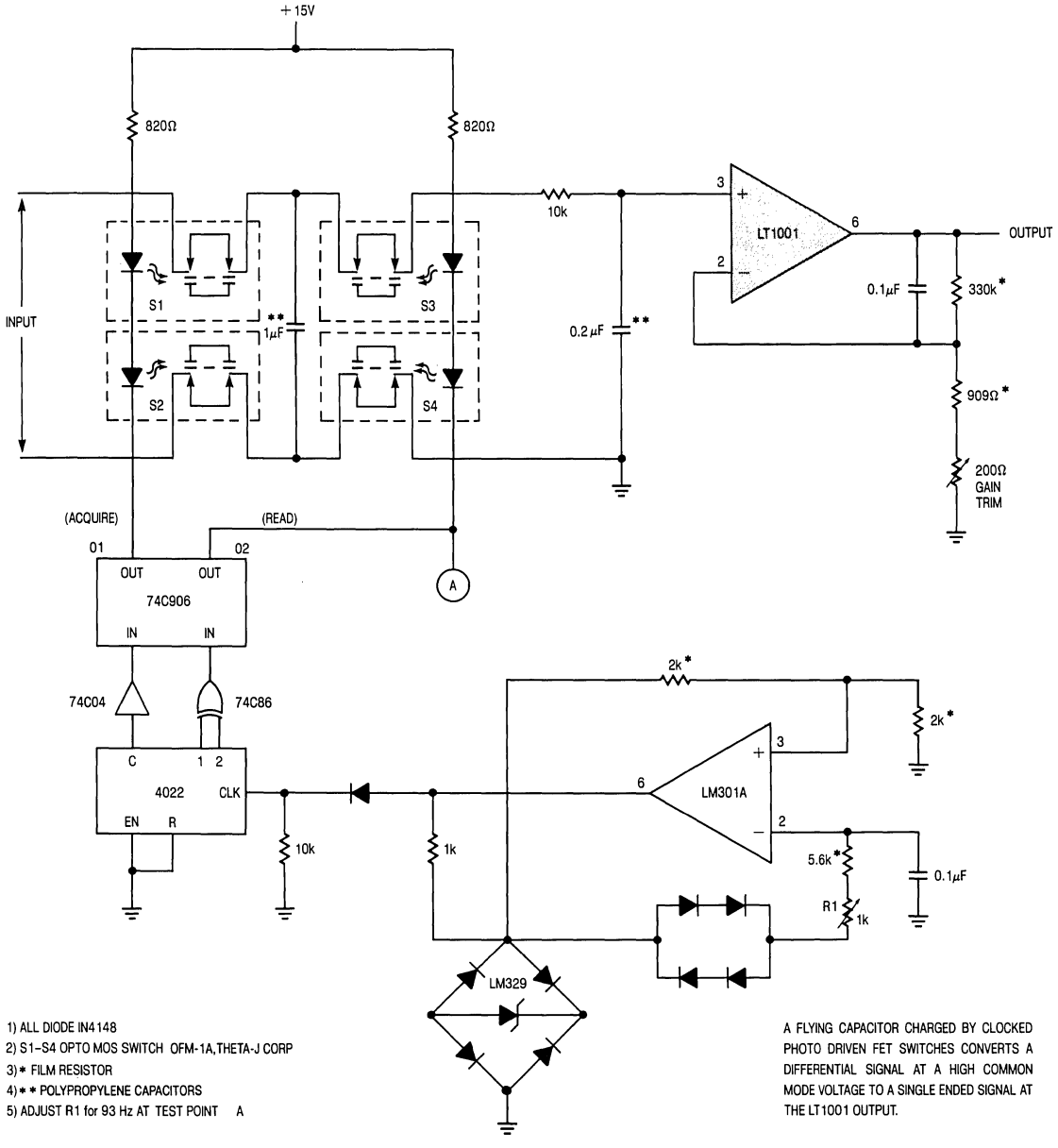


Dead Zone Generator

BIPOLAR SYMMETRY IS EXCELLENT BECAUSE ONE DEVICE, Q2, SETS BOTH LIMITS



Instrumentation Amplifier with ±300V Common Mode Range and CMRR > 150dB

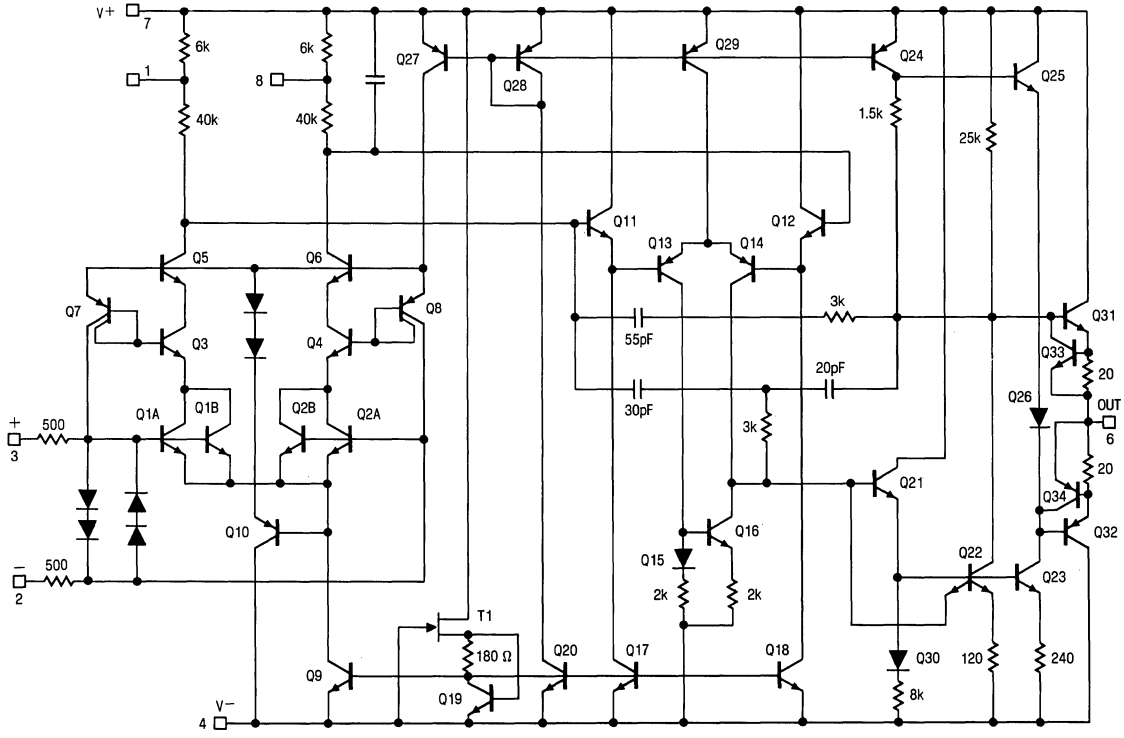


1) ALL DIODE IN4148
2) S1–S4 OPTO MOS SWITCH OFM-1A, THETA-J CORP
3) * FILM RESISTOR
4) * * POLYPROPYLENE CAPACITORS
5) ADJUST R1 for 93 Hz AT TEST POINT A

A FLYING CAPACITOR CHARGED BY CLOCKED PHOTO DRIVEN FET SWITCHES CONVERTS A DIFFERENTIAL SIGNAL AT A HIGH COMMON MODE VOLTAGE TO A SINGLE ENDED SIGNAL AT THE LT1001 OUTPUT.

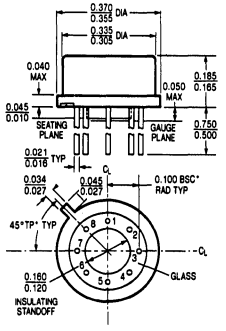
SCHEMATIC DIAGRAM

LT1001 Schematic Diagram



PACKAGE DESCRIPTION

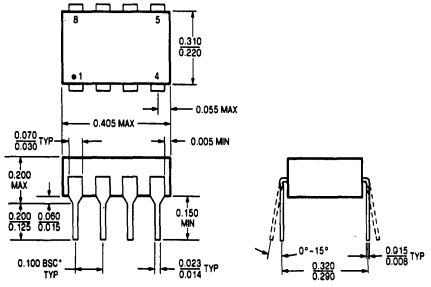
H Package
Metal Can



NOTE: DIMENSIONS IN INCHES

$T_j$max	Θ_{ja}	Θ_{jc}
150°C	150°C/W	45°C/W

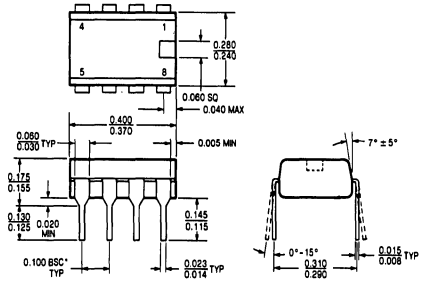
J8 Package
8 Lead Hermetic Dip



NOTE: DIMENSIONS IN INCHES UNLESS OTHERWISE NOTED.
*LEADS WITHIN 0.007 OF TRUE POSITION (TP) AT GAUGE PLANE

$T_j$max	Θ_{ja}
150°C	100°C/W

N8 Package
8 Lead Plastic



NOTE: DIMENSIONS IN INCHES UNLESS OTHERWISE NOTED.
*LEADS WITHIN 0.007 OF TRUE POSITION (TP) AT GAUGE PLANE.

$T_j$max	Θ_{ja}
100°C	130°C/W

Dual, Matched Precision Operational Amplifier

FEATURES

- *Guaranteed* low offset voltage
  - LT1002A 60μV max
  - LT1002 100μV max
- *Guaranteed* offset voltage match
  - LT1002A 40μV max
  - LT1002 80μV max
- *Guaranteed* low drift
  - LT1002A 0.9μV/°C max
  - LT1002 1.3μV/°C max
- *Guaranteed* CMRR
  - LT1002A 110dB min
  - LT1002 110dB min
- *Guaranteed* channel separation
  - LT1002A 132dB min
  - LT1002 130dB min
- *Guaranteed* matching characteristics
- Low noise 0.35μV p-p

APPLICATIONS

- Thermocouple Amplifiers
- Strain Gauge Amplifiers
- Low level signal processing
- Medical instrumentation
- Precision dual limit threshold detection
- Instrumentation amplifiers

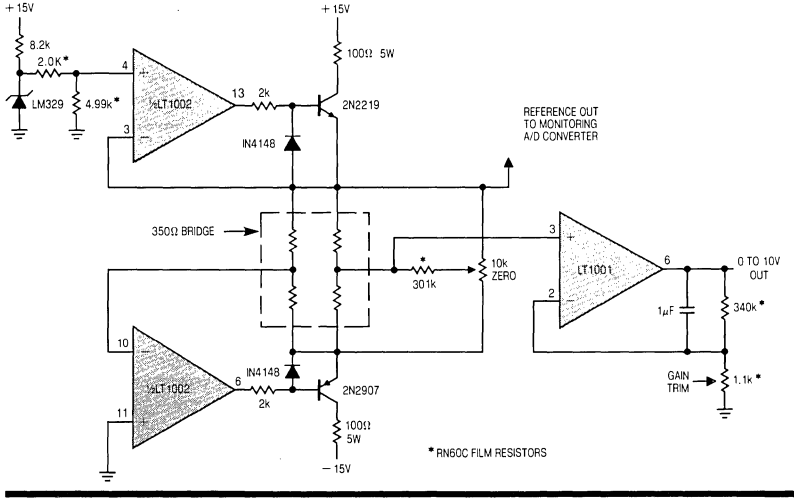
DESCRIPTION

The LT1002 dual, matched precision operational amplifiers combine excellent individual amplifier performance with tight matching and temperature tracking between amplifiers.

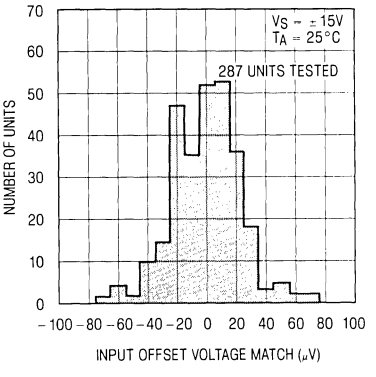
In the design, processing, and testing of the device, particular attention has been paid to the optimization of the entire distribution of several key parameters and their matching. Consequently, the specifications of even the low cost commercial grade (the LT1002C) have been spectacularly improved compared to presently available devices.

Essentially, the input offset voltage of all units is less than 80μV, and matching between amplifiers is consistently better than 60μV (see distribution plot below). Input bias and offset currents, channel separation, common mode and power supply rejections of the LT1002C are all specified at levels which were previously attainable only on very expensive, selected grades of other dual devices. Power dissipation is nearly halved compared to the most popular precision duals, without adversely affecting noise or speed performance. A by-product of lower dissipation is decreased warm-up drift. For even better performance in a single precision op amp, refer to the LT1001 data sheet. A bridge signal conditioning application is shown below. This circuit illustrates the requirement for both excellent matching and individual amplifier specifications.

Strain Gauge Signal Conditioner With Bridge Excitation



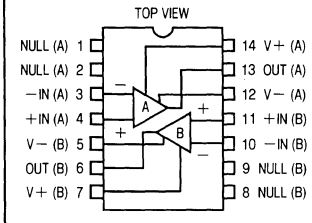
Distribution of Offset Voltage Match



ABSOLUTE MAXIMUM RATINGS

Supply Voltage (Note 6) ..... ±22V
Differential Input Voltage ..... ±30V
Input Voltage Equal to Supply Voltage
Output Short Circuit Duration..... Indefinite
Operating Temperature Range
LT1002AM/LT1002M..... −55°C to 125°C
LT1002AC/LT1002C ..... 0°C to 70°C
Storage Temperature Range
All Grades ..... −65°C to 150°C
Lead Temperature (Soldering, 10 sec.)..... 300°C

PACKAGE/ORDER INFORMATION



J PACKAGE
14 PIN HERMETIC

N PACKAGE
14 PIN PLASTIC

NOTE: Device may be operated even if insertion is reversed; this is due to inherent symmetry of pin locations of amplifiers A and B. (Note 6)

ORDER PART NO.	OFFSET VOLTAGE MAX at 25°C
LT1002AMJ	60μV
LT1002MJ	100μV
LT1002ACJ	60μV
LT1002CJ	100μV
LT1002ACN	60μV
LT1002CN	100μV

ELECTRICAL CHARACTERISTICS, INDIVIDUAL AMPLIFIERS

V_S = ±15V, T_A = 25°C, unless otherwise noted

SYMBOL	PARAMETER	CONDITIONS	LT1002AM/LT1002AC MIN	LT1002AM/LT1002AC TYP	LT1002AM/LT1002AC MAX	LT1002M/LT1002C MIN	LT1002M/LT1002C TYP	LT1002M/LT1002C MAX	UNITS
V_{OS}	Input Offset Voltage	Note 1		20	60		25	100	μV
$\frac{\Delta V_{OS}}{\Delta \text{ Time}}$	Long Term Input Offset Voltage Stability	Notes 2 and 3		0.3	1.5		0.4	2.0	μV/month
I_{OS}	Input Offset Current			0.3	2.8		0.4	4.2	nA
I_B	Input Bias Current			±0.6	±3.0		±0.7	±4.5	nA
e_n	Input Noise Voltage	0.1Hz to 10Hz (Note 2)		0.35	0.7		0.38	0.75	μV_{p-p}
e_n	Input Noise Voltage Density	f_o = 10Hz (Note 5) f_o = 1000Hz (Note 2)		10.3 9.6	20.0 11.5		10.5 9.8	20.0 12.0	$nV\sqrt{Hz}$
A_{VOL}	Large Signal Voltage Gain	$R_L \geq 2k\Omega$, V_o = ±12V $R_L \geq 1k\Omega$, V_o = ±10V	400 250	800 500		350 220	800 500		V/mV
CMRR	Common Mode Rejection Ratio	V_{CM} = ±13V	110	126		110	126		dB
PSRR	Power Supply Rejection Ratio	V_S = ±3V to ±18V	108	123		105	123		dB
R_{in}	Input Resistance Differential Mode	Note 4	20	100		13	80		MΩ
	Input Voltage Range		±13	±14		±13	±14		V
V_{OUT}	Maximum Output Voltage Swing	$R_L \geq 2k\Omega$ $R_L \geq 1k\Omega$	±13 ±12	±14 ±13.5		±13 ±12	±14 ±13.5		V
SR	Slew Rate	$R_L \geq 2k\Omega$ (Note 4)	0.1	0.25		0.1	0.25		V/μs
GBW	Gain Bandwidth Product	Note 4	0.4	0.8		0.4	0.8		MHz
P_d	Power Dissipation per amplifier	No load No load, V_s = ±3V		46 4	75 7		48 4	85 8	mW

ELECTRICAL CHARACTERISTICS, INDIVIDUAL AMPLIFIERS

$V_S = \pm 15V$, $-55°C \leq T_A \leq 125°C$, unless otherwise noted

SYMBOL	PARAMETER	CONDITIONS		LT1002AM MIN	LT1002AM TYP	LT1002AM MAX	LT1002M MIN	LT1002M TYP	LT1002M MAX	UNITS
V_{OS}	Input Offset Voltage	Note 1	●		30	150		45	230	μV
$\frac{\Delta V_{OS}}{\Delta Temp}$	Average Input Offset Voltage Drift		●		0.2	0.9		0.3	1.3	μV/°C
I_{OS}	Input Offset Current		●		0.8	5.6		1.2	8.5	nA
I_B	Input Bias Current		●		±1.0	±6.0		±1.5	±9.0	nA
A_{VOL}	Large Signal Voltage Gain	$R_L \geq 2k\Omega$, $V_o = \pm 10V$	●	300	700		200	700		V/mV
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm 13V$	●	106	122		104	120		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 3V$ to $\pm 18V$	●	102	117		96	117		dB
	Input Voltage Range		●	±13	±14		±13	±14		V
V_{OUT}	Output Voltage Swing	$R_L \geq 2k\Omega$	●	±12.5	±13.5		±12.0	±13.5		V
P_d	Power Dissipation per amplifier	No load	●		55	90		60	100	mW

$V_S = \pm 15V$, $0°C \leq T_A \leq 70°C$, unless otherwise noted

SYMBOL	PARAMETER	CONDITIONS		LT1002AC MIN	LT1002AC TYP	LT1002AC MAX	LT1002C MIN	LT1002C TYP	LT1002C MAX	UNITS
V_{OS}	Input Offset Voltage	Note 1	●		20	100		30	160	μV
$\frac{\Delta V_{OS}}{\Delta Temp}$	Average Input Offset Voltage Drift		●		0.2	0.9		0.3	1.3	μV/°C
I_{OS}	Input Offset Current		●		0.5	4.2		0.6	5.7	nA
I_B	Input Bias Current		●		±0.7	±4.5		±1.0	±6.0	nA
A_{VOL}	Large Signal Voltage Gain	$R_L \geq 2k\Omega$, $V_o = \pm 10V$	●	350	750		250	750		V/mV
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm 13V$	●	108	124		106	123		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 3V$ to $\pm 18V$	●	105	120		100	120		dB
	Input Voltage Range		●	±13	±14		±13	±14		V
V_{OUT}	Output Voltage Swing	$R_L \geq 2k\Omega$	●	±12.5	±13.8		±12.5	±13.8		V
P_d	Power Dissipation per amplifier	No load	●		50	85		55	90	mW

The ● denotes the specifications which apply over the full operating temperature range.

For MIL-STD components, please refer to LTC 883C data sheet for test listing and parameters.

Note 1: Offset voltage measured with high speed test equipment, approximately 1 second after power is applied.

Note 2: This parameter is tested on a sample basis only.

Note 3: Long Term Input Offset Voltage Stability refers to the averaged trend line of V_{os} versus Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{os} during the first 30 operating days are typically 2.5μV.

Note 4: Parameter is guaranteed by design.

Note 5: 10Hz noise voltage density is sample tested on every lot. Devices 100% tested at 10Hz are available on request.

Note 6: The V+ supply terminals are completely independent and may be powered by separate supplies if desired (this approach, however, would sacrifice the advantages of the power supply rejection ratio matching). The V− supply terminals are both connected to the common substrate and must be tied to the same voltage. Both V− pins should be used.

MATCHING CHARACTERISTICS at $V_S = \pm 15V$, $T_A = 25°C$, unless otherwise noted

SYMBOL	PARAMETER	CONDITIONS	LT1002AM/AC MIN	LT1002AM/AC TYP	LT1002AM/AC MAX	LT1002M/C MIN	LT1002M/C TYP	LT1002M/C MAX	UNITS
	Input Offset Voltage Match		—	15	40	—	25	80	μV
I_B^+	Average Non-Inverting Bias Current		—	±0.6	±3.5	—	±0.7	±4.8	nA
I_{OS}^+	Non-Inverting Offset Current		—	0.6	3.5	—	0.7	6.0	nA
I_{OS}^-	Inverting Offset Current		—	0.6	3.5	—	0.7	6.0	nA
ΔCMRR	Common Mode Rejection Ratio Match	$V_{CM} = \pm 13V$	110	132	—	108	132	—	dB
ΔPSRR	Power Supply Rejection Ratio Match	$V_S = \pm 3V$ to $\pm 18V$	108	130	—	102	128	—	dB
	Channel Separation	$f \leq 10Hz$ (Note 4)	132	148	—	130	146	—	dB

MATCHING CHARACTERISTICS at $V_S = \pm 15V$, $-55°C \leq T_A \leq 125°C$, unless otherwise noted

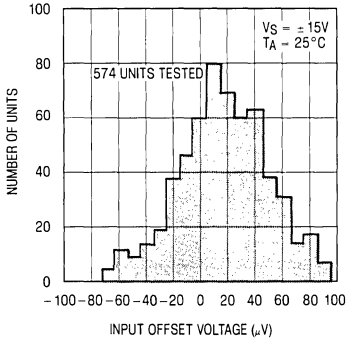
SYMBOL	PARAMETER	CONDITIONS		LT1002AM MIN	LT1002AM TYP	LT1002AM MAX	LT1002M MIN	LT1002M TYP	LT1002M MAX	UNITS
	Input Offset Voltage Match		●	—	50	140	—	60	230	μV
	Input Offset Voltage Tracking		●	—	0.3	1.0	—	0.4	1.5	μV/°C
I_B^+	Average Non-Inverting Bias Current		●	—	±1.5	±6.0	—	±1.8	±10.0	nA
I_{OS}^+	Non-Inverting Offset Current		●	—	1.5	6.5	—	1.8	12.0	nA
I_{OS}^-	Inverting Offset Current		●	—	1.5	6.5	—	1.8	12.0	nA
ΔCMRR	Common Mode Rejection Ratio Match	$V_{CM} = \pm 13V$	●	106	126	—	102	124	—	dB
ΔPSRR	Power Supply Rejection Ratio Match	$V_S = \pm 3V$ to $\pm 18V$	●	102	122	—	94	120	—	dB

MATCHING CHARACTERISTICS at $V_S = \pm 15V$, $0°C \leq T_A \leq 70°C$, unless otherwise noted

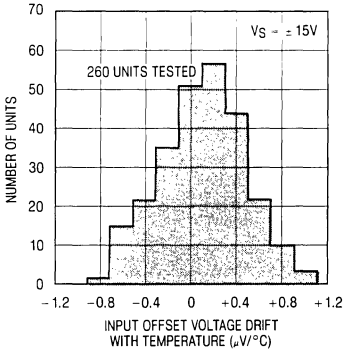
SYMBOL	PARAMETER	CONDITIONS		LT1002AC MIN	LT1002AC TYP	LT1002AC MAX	LT1002C MIN	LT1002C TYP	LT1002C MAX	UNITS
	Input Offset Voltage Match		●	—	30	85	—	45	150	μV
	Input Offset Voltage Tracking		●	—	0.3	1.0	—	0.4	1.5	μV/°C
I_B^+	Average Non-Inverting Bias Current		●	—	±1.0	±4.5	—	±1.2	±7.0	nA
I_{OS}^+	Non-Inverting Offset Current		●	—	1.0	5.0	—	1.2	8.5	nA
I_{OS}^-	Inverting Offset Current		●	—	1.0	5.0	—	1.2	8.5	nA
ΔCMRR	Common Mode Rejection Ratio Match	$V_{CM} = \pm 13V$	●	108	130	—	105	128	—	dB
ΔPSRR	Power Supply Rejection Ratio Match	$V_S = \pm 3V$ to $\pm 18V$	●	105	126	—	98	124	—	dB

TYPICAL PERFORMANCE CHARACTERISTICS

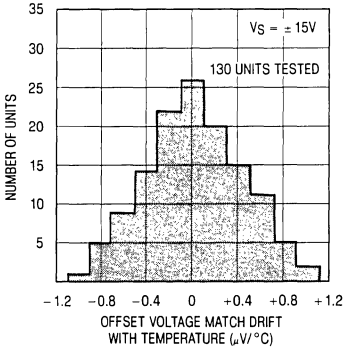
Distribution of Offset Voltage of Individual Amplifiers



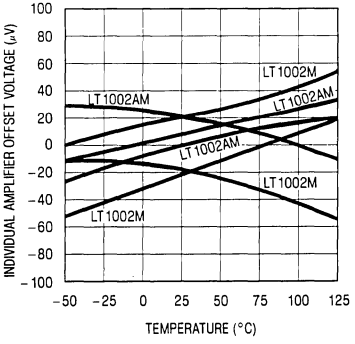
Distribution of Offset Voltage Drift with Temperature (Individual Amplifiers)



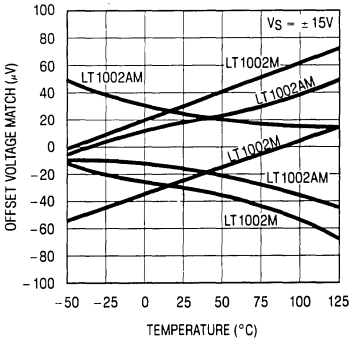
Distribution of Offset Voltage Match Drift with Temperature



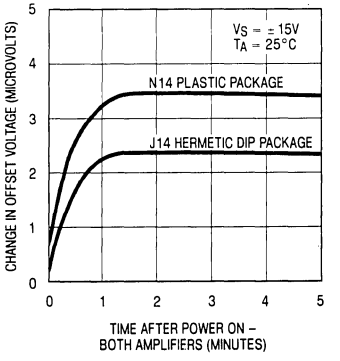
Offset Voltage Drift with Temperature of Six Representative Units



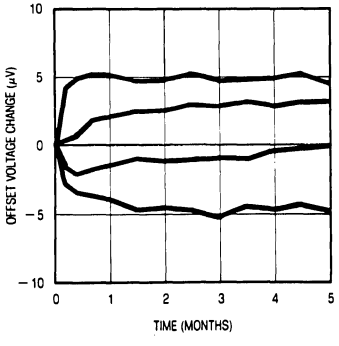
Offset Voltage Tracking with Temperature of Six Representative Units



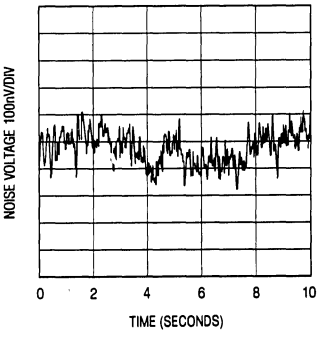
Warm-Up Drift



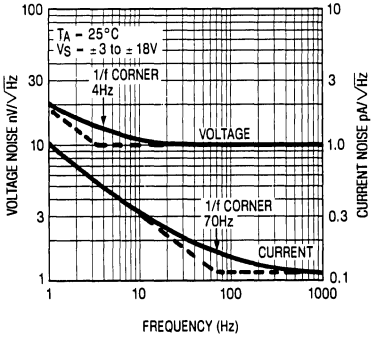
Long Term Stability of Four Representative Units



0.1Hz to 10Hz Noise

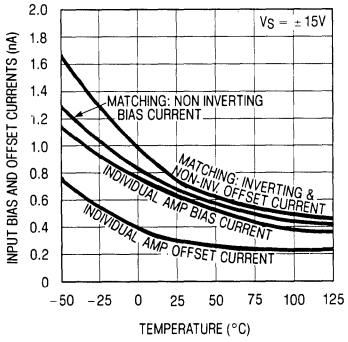


Noise Spectrum

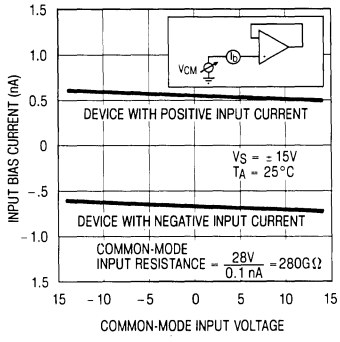


TYPICAL PERFORMANCE CHARACTERISTICS

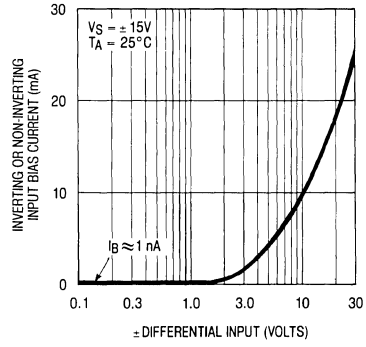
Matching and Individual Amplifier Bias and Offset Currents vs Temperature



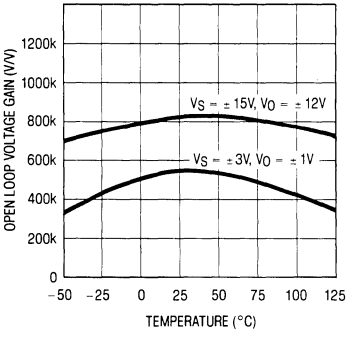
Input Bias Current Over the Common Mode Range



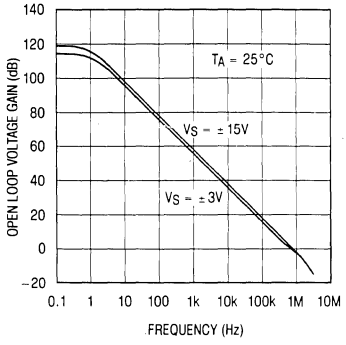
Input Bias Current vs. Differential Input Voltage



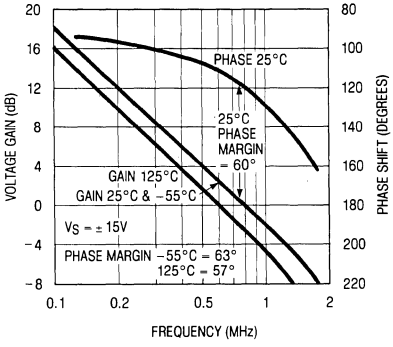
Open Loop Voltage Gain vs Temperature



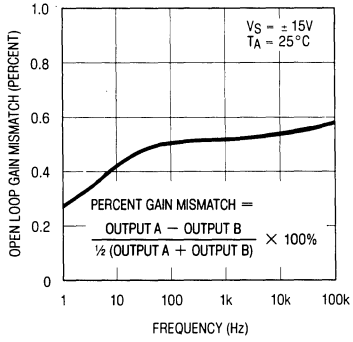
Open Loop Voltage Gain Frequency Response



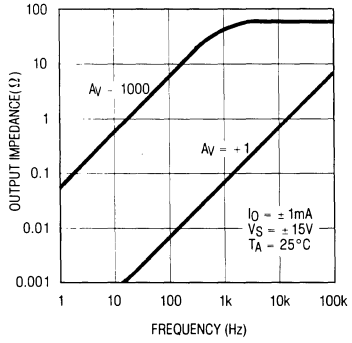
Gain, Phase Shift vs. Frequency



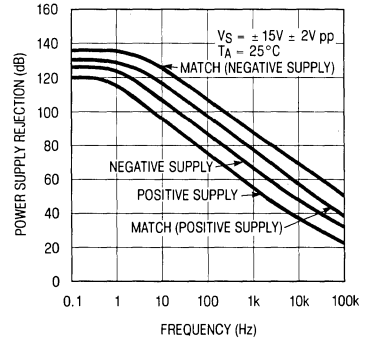
Open Loop Gain Mismatch vs Frequency



Closed Loop Output Impedance

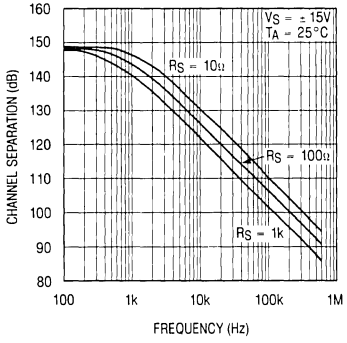


Power Supply Rejection and PSRR Match vs Frequency

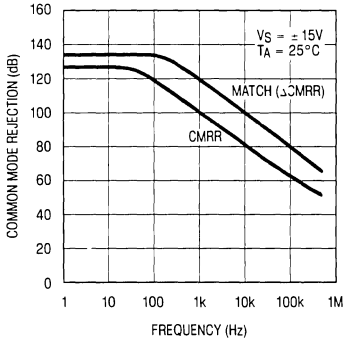


TYPICAL PERFORMANCE CHARACTERISTICS

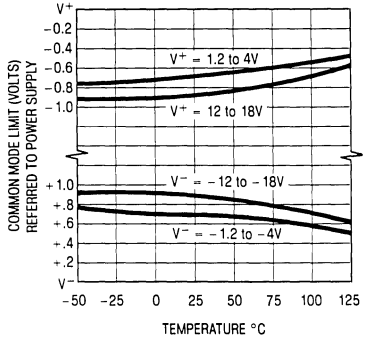
Channel Separation vs Frequency



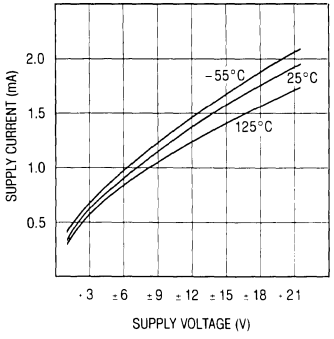
Common Mode Rejection and CMRR Match vs Frequency



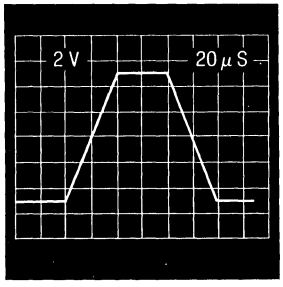
Common Mode Limit vs Temperature



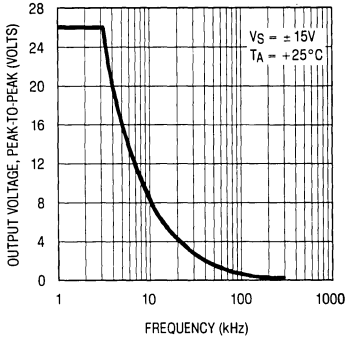
Supply Current vs. Supply Voltage For Each Amplifier



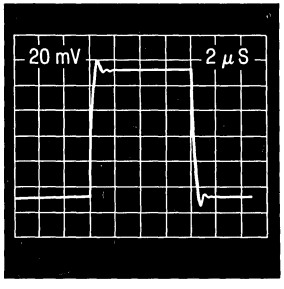
Large Signal Transient Response



Maximum Undistorted Output vs. Frequency

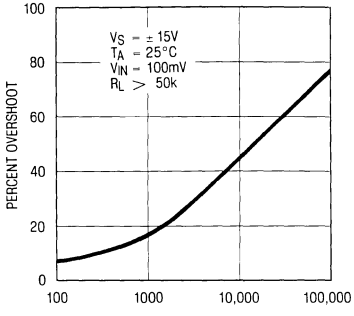


Small Signal Transient Response

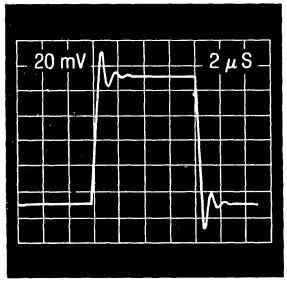


$A_V = +1$, $C_L = 50pF$

Voltage Follower Overshoot vs Capacitive Load



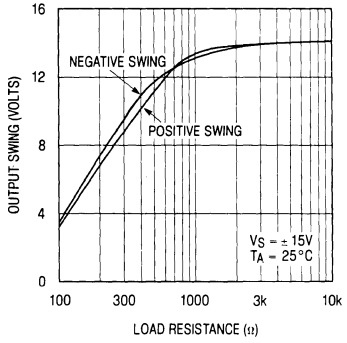
Small Signal Transient Response



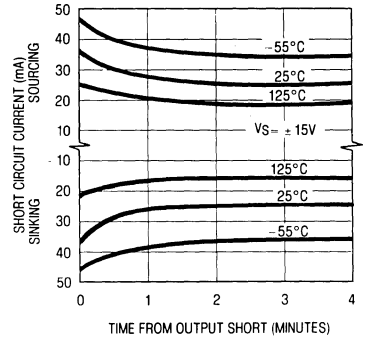
$A_V = +1$, $C_L = 1000pF$

TYPICAL PERFORMANCE CHARACTERISTICS

Output Swing vs. Load Resistance



Output Short Circuit Current vs Time



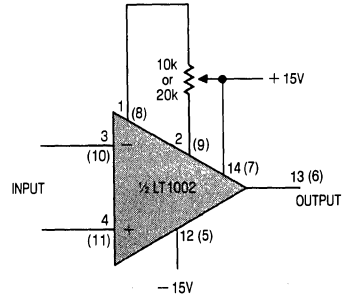
APPLICATIONS INFORMATION

The LT1002 dual amplifier may be inserted directly into OP-10, OP207, OP227 sockets with or without removal of external nulling potentiometers.

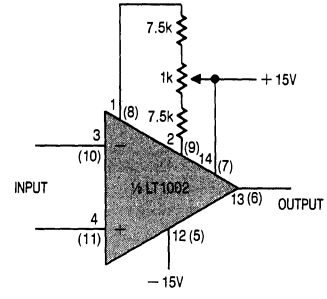
Offset Voltage Adjustment The input offset voltage of the LT1002, and its drift with temperature, are permanently trimmed at wafer testing to a low level. However, if further adjustment of V_{OS} is necessary, nulling with a 10k or 20k potentiometer will not degrade drift with temperature. Trimming to a value other than zero creates a drift of $(V_{OS}/300)\ \mu V/°C$, e.g. if V_{OS} is adjusted to 300μV, the change in drift will be 1μV/°C. The adjustment range with a 10k or 20k pot is approximately ±2.5mV. If less adjustment range is needed, the sensitivity and resolution of the nulling can be improved by using a smaller pot in conjunction with fixed resistors. The example has an approximate null range of ±100μV.

In matching applications, both amplifiers can be trimmed to zero, or the offset of one amplifier can be trimmed to match the offset of the other. Offset adjustment, however, slightly degrades the gain, common-mode and power-supply rejection match between the two op amps. Fortunately, the guaranteed offset voltage match of the LT1002 is very low, in most applications offset adjustment will be unnecessary.

Standard Adjustment

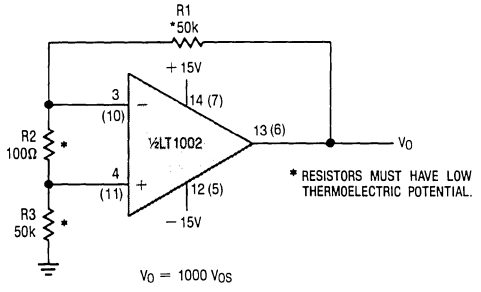


Improved Sensitivity Adjustment



APPLICATIONS INFORMATION

Test Circuit for Offset Voltage and its Drift with Temperature



This circuit is also used as the burn-in configuration for the LT1002, with supply voltages increased to ±20V, R1 = R3 = 20k, R2 = 200Ω, A_V = 100.

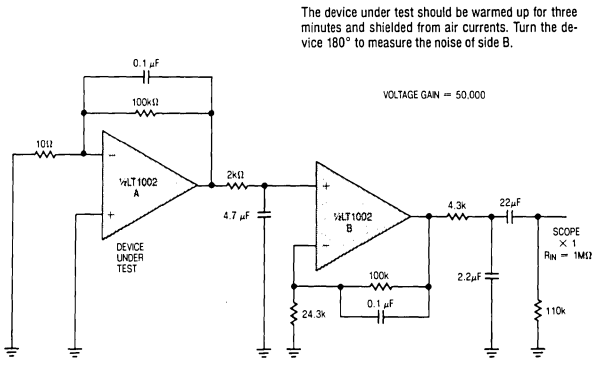
Unless proper care is exercised, thermocouple effects, caused by temperature gradients across dissimilar metals at the contacts to the input terminals, can exceed the inherent drift of the amplifier. Air currents should be minimized, package leads should be short, the two input leads should be as close together as possible and maintained at the same temperature.

Channel Separation

This parameter is defined as the ratio of the change in input offset voltage of one amplifier to the change in output voltage of the other amplifier causing the offset change.

At low frequencies the LT1002's channel separation is an almost unmeasurable 148dB. As frequency increases, pin to pin capacitance of the package, between the output of one amplifier and the inputs of the other, becomes dominant. Since these pins are non-adjacent, the capacitance is only 0.02pF. To maintain the LT1002's excellent channel separation at higher frequencies, the socket and PC board capacitances should be minimized.

0.1Hz to 10Hz Noise Test Circuit



(Peak to Peak noise measured in 10 Sec interval)

Power supplies

The LT1002 is specified over a wide range of power supply voltages from ±3V to ±18V. Operation with lower supplies is possible, down to ±1.2V (two Ni-Cad batteries). However, with ±1.2V supplies, the device is stable only in closed loop gains of +2 or higher (or inverting gain of one or higher).

The V+ supply terminals are completely independent and may be powered by separate supplies if desired (this approach, however, would sacrifice the advantages of the power supply rejection ratio matching). The V− supply terminals are both connected to the common substrate and must be tied to the same voltage. Both V− pins should be used.

APPLICATIONS INFORMATION

Advantages of Matched Dual Op Amps In many applications the performance of a system depends on the matching between two operational amplifiers rather than the individual characteristics of the two op amps. Two or three op amp instrumentation amplifiers, tracking voltage references and low drift active filters are some of the circuits requiring matching between two op amps.

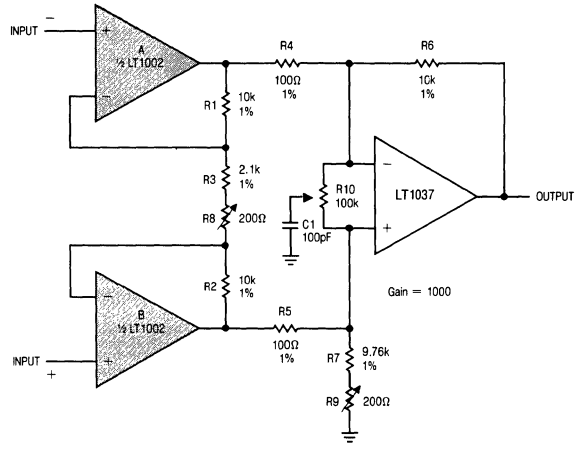
The well-known triple op amp configuration illustrates these concepts. Output offset is a function of the difference between the offsets of the two halves of the LT1002. This error cancellation principle holds for a considerable number of input referred parameters in addition to offset voltage and its drift with temperature. Input bias current will be the average of the two non-inverting input currents (I_B^+). The difference between these two currents (I_{OS}^+) is the offset current of the instrumentation amplifier. The difference between the inverting input currents (I_{OS}^-) will cause errors flowing through R1, R2, and R3. Common-mode and power supply rejections will be dependent only on the match between the two amplifiers (assuming perfect resistor matching).

The concepts of common mode and power supply rejection ratio match (ΔCMRR and ΔPSRR) are best demonstrated with a numerical example:

Assume $CMRR_A = +1.0\mu V/V$ or 120dB,
and $CMRR_B = +0.75\mu V/V$ or 122.5dB,
then $\Delta CMRR = 0.25\mu V/V$ or 132dB;
if $CMRR_B = -0.75\mu V/V$ which is still 122.5dB,
then $\Delta CMRR = 1.75\mu V/V$ or 115dB.

Clearly, the LT1002, by specifying and guaranteeing all of these matching parameters, can significantly improve the performance of matching dependent circuits.

Three Op Amp Instrumentation Amplifier



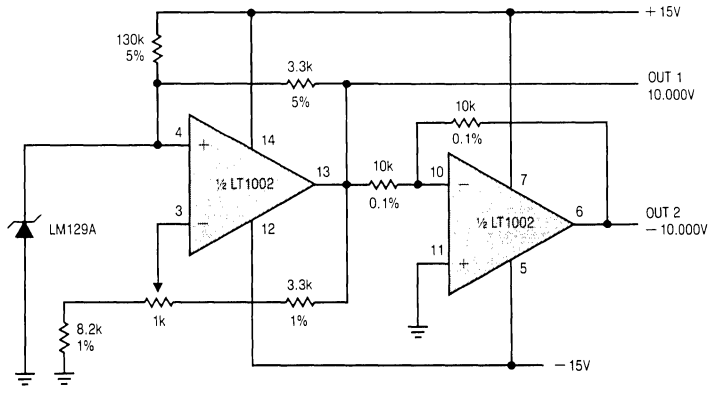
Trim R8 for gain
Trim R9 for DC common mode rejection
Trim R10 for AC common mode rejection

Typical performance of the instrumentation amplifer:

Input offset voltage = 25μV
Input bias current = 0.7nA
Input resistance = 200 GΩ
Input offset current = 0.6nA
Input noise = 0.5μV p-p
Power bandwidth ($V_O = \pm 10V$) = 80kHz

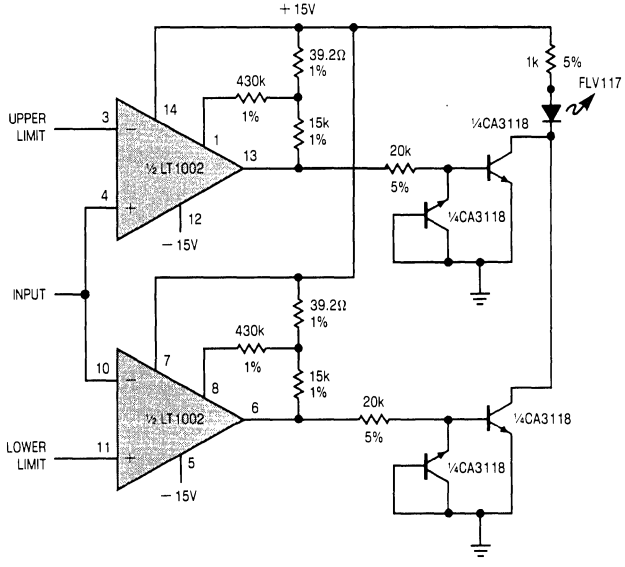
APPLICATIONS INFORMATION

Precision ± 10V Reference



The LT1002 contributes less than 5% of the total drift with temperature, noise and long term drift of the reference. The accuracy of the −10V output is limited by the matching of the two 10k resistors.

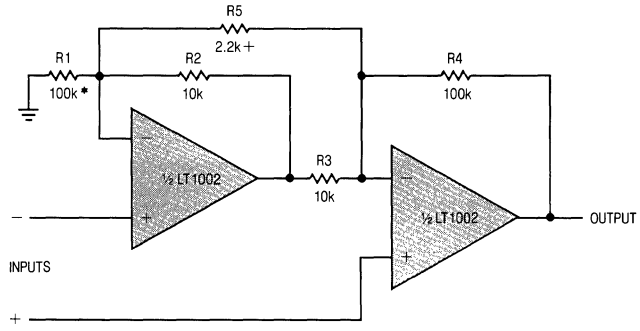
Dual Limit Microvolt Comparator



When the upper or lower limit is exceeded the LED lights up. Positive feedback to one of the nulling terminals creates 5 to 20μV of hysteresis on both amplifiers. This feedback changes the offset voltage of the LT1002 by less than 5μV. Therefore, the basic accuracy of the comparator is limited only by the low offset voltage of the LT1002.

APPLICATIONS INFORMATION

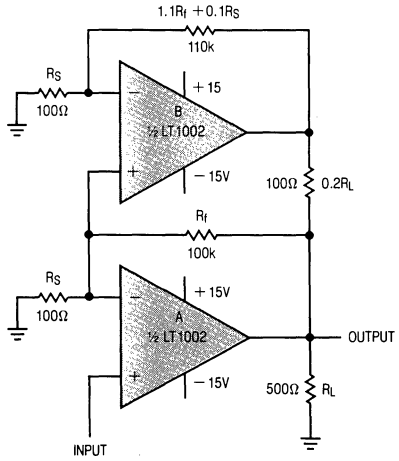
Two Op Amp Instrumentation Amplifier



* TRIM FOR COMMON-MODE REJECTION
\+ TRIM FOR GAIN

$$\text{Gain} = \frac{R4}{R3}\left[1 + \frac{1}{2}\left(\frac{R2}{R1} + \frac{R3}{R4}\right) + \frac{R2 + R3}{R5}\right] \approx 100$$

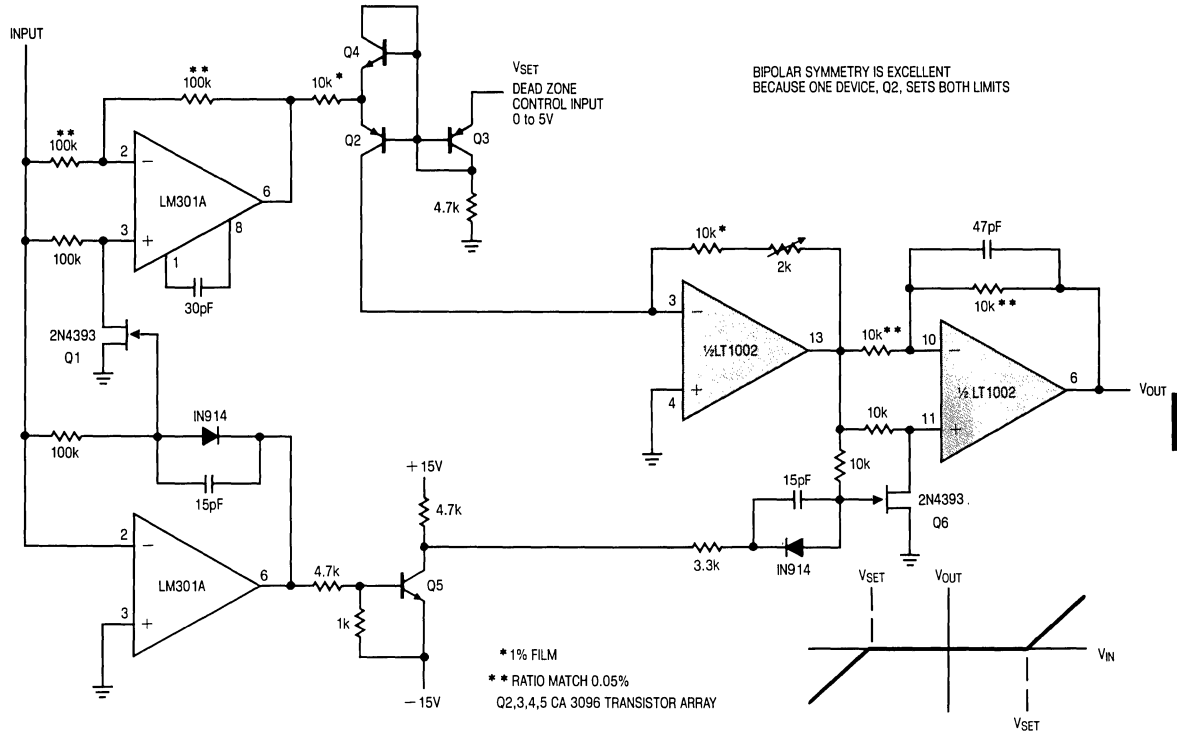
Precision Amplifier Drives 500Ω Load to ± 10V



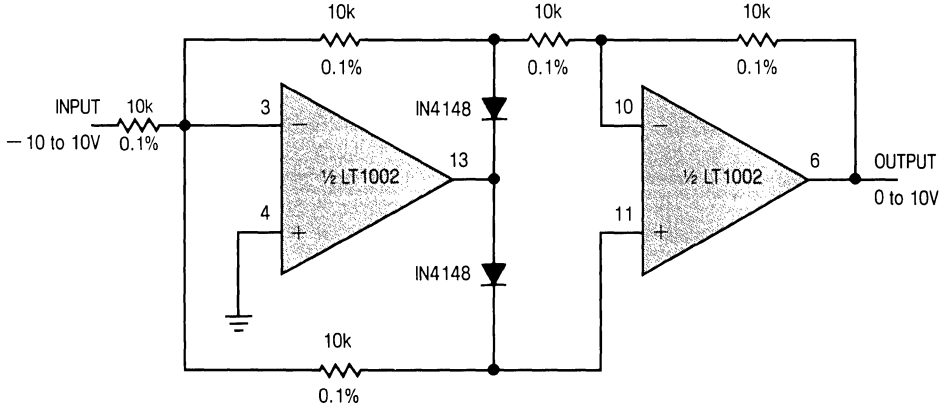
This application utilizes the guaranteed 10mA load driving capability of the LT1002. The offset voltage of amplifier A is the offset of the configuration. Amplifier B provides the additional 10mA load current. When load resistor R_L is removed, amplifier A sinks this current without affecting accuracy. In the gain of 1000 configuration shown, approximately 0.3% gain accuracy can be realized.

APPLICATIONS INFORMATION

Dead Zone Generator

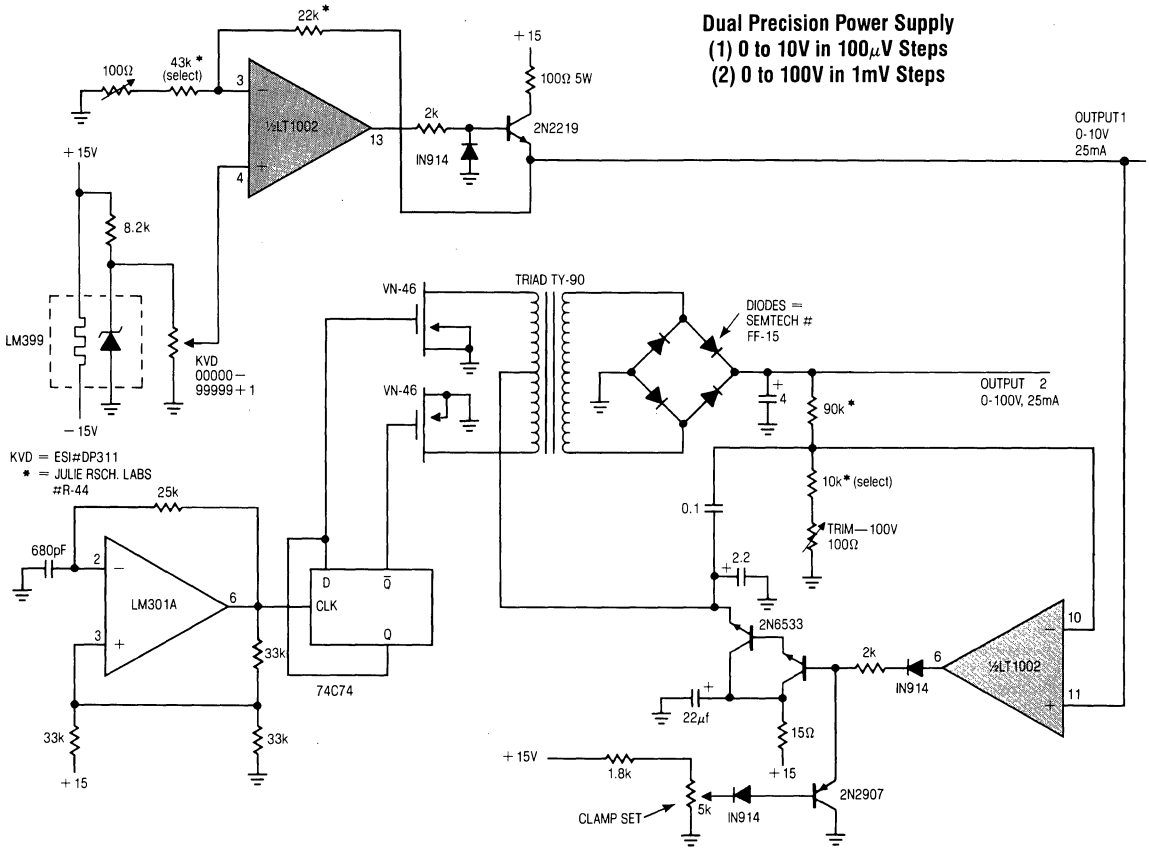


Precision Absolute Value Circuit

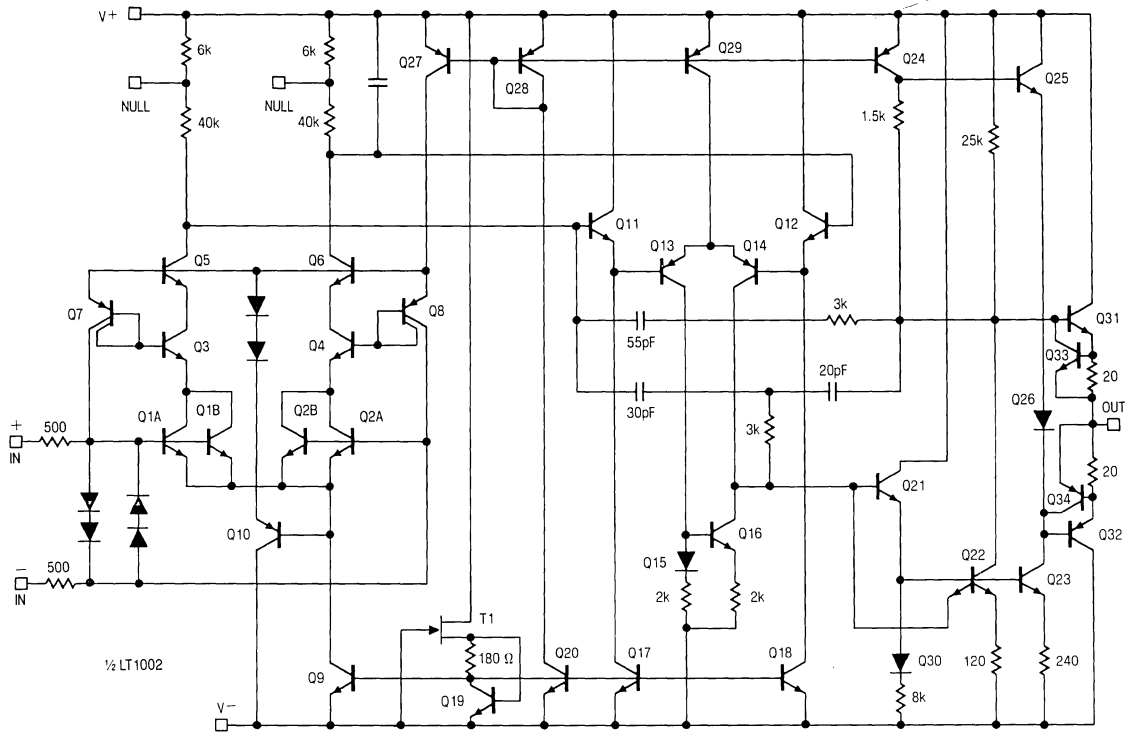


APPLICATIONS INFORMATION

Dual Precision Power Supply
(1) 0 to 10V in 100μV Steps
(2) 0 to 100V in 1mV Steps



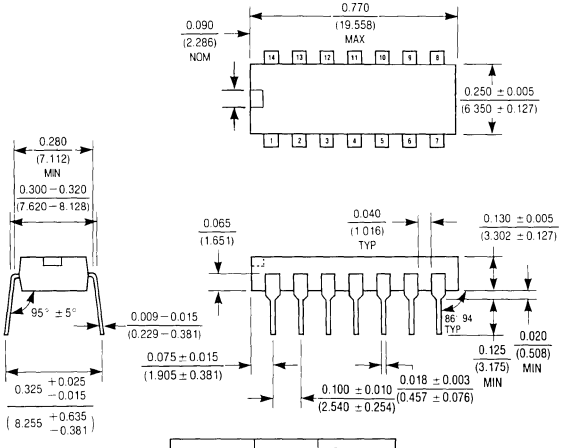
SCHEMATIC DIAGRAM



PACKAGE DESCRIPTION

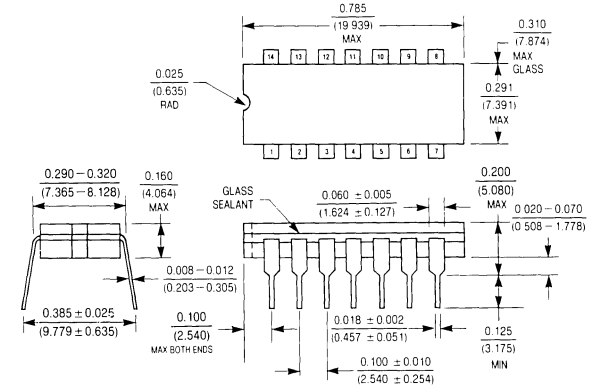
Dimensions in inches (millimeters) unless otherwise noted.

14-Lead Molded DIP (N)



	T_{JMAX}	Θ_{JA}
LT1002ACN LT1002CN	125°C	100°C/W

14-Lead Cavity DIP (J)



	T_{JMAX}	Θ_{JA}
LT1002ACJ LT1002CJ	125°C	100°C/W
LT1002AMJ LT1002MJ	150°C	100°C/W

Low Noise, High Speed Precision Operational Amplifiers

FEATURES

- *Guaranteed* 4.5 nV/$\sqrt{\text{Hz}}$ 10 Hz noise
- *Guaranteed* 3.8 nV/$\sqrt{\text{Hz}}$ 1kHz noise
- 0.1 Hz to 10 Hz noise, 60 nV p-p, typical
- *Guaranteed* 7 million min. voltage gain, $R_L = 2k\Omega$
- *Guaranteed* 3 million min. voltage gain, $R_L = 600\Omega$
- *Guaranteed* 25μV max. offset voltage
- *Guaranteed* 0.6μV/°C max. drift with temperature
- *Guaranteed* 11V/μsec min. slew rate (LT1037)
- *Guaranteed* 117 dB min. CMRR

APPLICATIONS

- Low Noise Signal Processing
- Microvolt Accuracy Threshold Detection
- Strain Gauge Amplifiers
- Direct Coupled Audio Gain Stages
- Sine Wave Generators
- Tape Head Preamplifiers
- Microphone Preamplifiers

DESCRIPTION

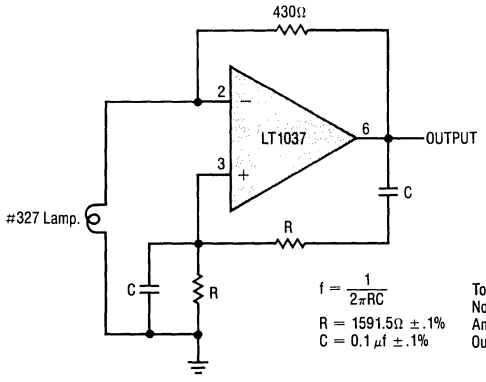
The LT1007/LT1037 series features the lowest noise performance available to date for monolithic operational amplifiers: 2.5nV/$\sqrt{\text{Hz}}$ wideband noise (less than the noise of a 400Ω resistor), 1/f corner frequency of 2Hz and 60nV peak to peak 0.1Hz to 10Hz noise. Low noise is combined with outstanding precision and speed specifications: 10μV offset voltage, 0.2μV/°C drift, 130 dB common-mode and power supply rejection, and 60MHz gain-bandwith-product on the decompensated LT1037, which is stable for closed loop gains of 5 or greater.

The voltage gain of the LT1007/1037 is an extremely high 20 million driving a 2kΩ load and 12 million driving a 600Ω load to ± 10V.

In the design, processing, and testing of the device, particular attention has been paid to the optimization of the entire distribution of several key parameters. Consequently, the specifications of even the lowest cost grades (the LT1007C and the LT1037C) have been spectacularly improved compared to equivalent grades of competing amplifiers.

The sine wave generator application shown below utilizes the low noise and low distortion characteristics of the LT1037.

Ultra-Pure 1kHz Sine Wave Generator

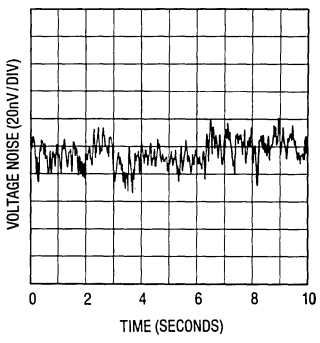


$f = \frac{1}{2\pi RC}$

R = 1591.5Ω ±.1%
C = 0.1 μf ±.1%

Total Harmonic Distortion = < .0025%
Noise = < .0001%
Amplitude = ± 8 volts
Output Frequency = 1.000kHz for values given ±.4%

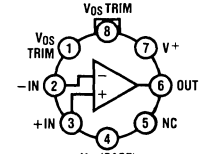
0.1Hz to 10Hz Noise



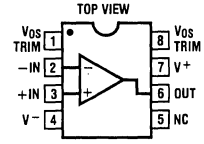
ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... ±22V
Input Voltage ..... Equal to Supply Voltage
Output Short Circuit Duration ..... Indefinite
Differential Input Current (Note 8) ..... ±25mA
Lead Temperature (Soldering, 10 sec.) ..... 300°C
Operating Temperature Range
LT1007/1037AM, M ..... −55°C to 125°C
LT1007/1037AC, C ..... 0°C to 70°C
Storage Temperature Range
All Devices ..... −65°C to 150°C

PACKAGE/ORDER INFORMATION



METAL CAN H PACKAGE



HERMETIC DIP J8 PACKAGE
PLASTIC DIP N8 PACKAGE

ORDER PART NUMBER	
LT1007AMH	LT1037AMH
LT1007MH	LT1037MH
LT1007ACH	LT1037ACH
LT1007CH	LT1037CH
LT1007AMJ8	LT1037AMJ8
LT1007MJ8	LT1037MJ8
LT1007ACJ8	LT1037ACJ8
LT1007CJ8	LT1037CJ8
LT1007ACN8	LT1037ACN8
LT1007CN8	LT1037CN8

ELECTRICAL CHARACTERISTICS $V_S = \pm 15V$, $T_A = 25°C$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	LT1007AM/AC LT1037AM/AC MIN	TYP	MAX	LT1007M/C LT1037M/C MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	(Note 1)		10	25		20	60	μV
$\frac{\Delta V_{OS}}{\Delta Time}$	Long Term Input Offset Voltage Stability	(Notes 2 and 3)		0.2	1.0		0.2	1.0	μV/Mo
I_{OS}	Input Offset Current			7	30		12	50	nA
I_B	Input Bias Current			±10	±35		±15	±55	nA
e_n	Input Noise Voltage	0.1Hz to 10Hz (Notes 3 and 5)		0.06	0.13		0.06	0.13	μVp-p
	Input Noise Voltage Density	f_o = 10Hz (Notes 3 and 4) f_o = 1000Hz (Note 3)		2.8 2.5	4.5 3.8		2.8 2.5	4.5 3.8	nV/√Hz nV/√Hz
i_n	Input Noise Current Density	f_o = 10Hz (Notes 3 and 6) f_o = 1000Hz (Notes 3 and 6)		1.5 0.4	4.0 0.6		1.5 0.4	4.0 0.6	pA/√Hz pA/√Hz
	Input Resistance — Common Mode			7			5		GΩ
	Input Voltage Range		±11.0	±12.5		±11.0	±12.5		V
CMRR	Common Mode Rejection Ratio	V_{CM} = ±11V	117	130		110	126		dB
PSRR	Power Supply Rejection Ratio	V_S = ±4V to ±18V	110	130		106	126		dB
A_{VOL}	Large Signal Voltage Gain	$R_L \geq 2k\Omega$, V_O = ±12V $R_L \geq 1k\Omega$, V_O = ±10V $R_L \geq 600\Omega$, V_O = ±10V	7.0 5.0 3.0	20.0 16.0 12.0		5.0 3.5 2.0	20.0 16.0 12.0		V/μV V/μV V/μV
V_{OUT}	Maximum Output Voltage Swing	$R_L \geq 2k\Omega$ $R_L \geq 600\Omega$	±13.0 ±11.0	±13.8 ±12.5		±12.5 ±10.5	±13.5 ±12.5		V V
SR	Slew Rate LT1007 LT1037	$R_L \geq 2k\Omega$ $A_{VCL} \geq 5$	1.7 11	2.5 15		1.7 11	2.5 15		V/μS V/μS
GBW	Gain-Bandwidth Product: LT1007 LT1037	f_o = 100kHz (Note 7) f_o = 10kHz (Note 7) ($A_{VCL} \geq 5$)	5.0 45	8.0 60		5.0 45	8.0 60		MHz MHz
Z_o	Open Loop Output Resistance	V_O = 0, I_O = 0		70			70		Ω
P_d	Power Dissipation LT1007 LT1037			80 80	120 130		80 85	140 140	mW mW

ELECTRICAL CHARACTERISTICS $V_S = \pm 15V$, $-55°C \leq T_A \leq 125°C$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		LT1007AM/LT1037AM MIN	LT1007AM/LT1037AM TYP	LT1007AM/LT1037AM MAX	LT1007M/LT1037M MIN	LT1007M/LT1037M TYP	LT1007M/LT1037M MAX	UNITS
V_{OS}	Input Offset Voltage	(Note 1)	●		25	60		50	160	μV
$\frac{\Delta V_{OS}}{\Delta Temp}$	Average Input Offset Drift	(Note 9)	●		0.2	0.6		0.3	1.0	μV/°C
I_{OS}	Input Offset Current		●		15	50		20	85	nA
I_B	Input Bias Current		●		±20	±60		±35	±95	nA
	Input Voltage Range		●	±10.3	±11.5		±10.3	±11.5		V
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm 10.3V$	●	112	126		104	120		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 4.5V$ to $\pm 18V$	●	104	126		100	120		dB
A_{VOL}	Large Signal Voltage Gain	$R_L \geq 2k\Omega$, $V_o = \pm 10V$ $R_L \geq 1k\Omega$, $V_o = \pm 10V$	● ●	3.0 2.0	14.0 10.0		2.0 1.5	14.0 10.0		V/μV V/μV
V_{OUT}	Maximum Output Voltage Swing	$R_L \geq 2k\Omega$	●	±12.5	±13.5		±12.0	±13.5		V
P_d	Power Dissipation		●		100	150		100	170	mW

ELECTRICAL CHARACTERISTICS $V_S = \pm 15V$, $0°C \leq T_A \leq 70°C$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		LT1007AC/LT1037AC MIN	LT1007AC/LT1037AC TYP	LT1007AC/LT1037AC MAX	LT1007C/LT1037C MIN	LT1007C/LT1037C TYP	LT1007C/LT1037C MAX	UNITS
V_{OS}	Input Offset Voltage	(Note 1)	⊛		20	50		35	110	μV
$\frac{\Delta V_{OS}}{\Delta Temp}$	Average Input Offset Drift	(Note 9)	⊛		0.2	0.6		0.3	1.0	μV/°C
I_{OS}	Input Offset Current		⊛		10	40		15	70	nA
I_B	Input Bias Current		⊛		±14	±45		±20	±75	nA
	Input Voltage Range		⊛	±10.5	±11.8		±10.5	±11.8		V
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm 10.5V$	⊛	114	126		106	120		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 4.5V$ to $\pm 18V$	⊛	106	126		102	120		dB
A_{VOL}	Large Signal Voltage Gain	$R_L \geq 2k\Omega$, $V_o = \pm 10V$ $R_L \geq 1k\Omega$, $V_o = \pm 10V$	⊛ ⊛	4.0 2.5	18.0 14.0		2.5 2.0	18.0 14.0		V/μV V/μV
V_{OUT}	Maximum Output Voltage Swing	$R_L \geq 2k\Omega$	⊛	±12.5	±13.6		±12.0	±13.6		V
P_d	Power Dissipation		⊛		90	144		90	160	mW

NOTES:

The ⊛ denotes the specifications which apply over full operating temperature range.

For MIL-STD components, please refer to LTC 883C data sheet for test listing and parameters.

Note 1: Input Offset Voltage measurements are performed by automatic test equipment approximately 0.5 seconds after application of power. AM and AC grades are guaranteed fully warmed up.

Note 2: Long Term Input Offset Voltage Stability refers to the average trend line of Offset Voltage vs. Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30 days are typically 2.5μV — refer to typical performance curve.

Note 3: This parameter is tested on a sample basis only.

Note 4: 10Hz noise voltage density is sample tested on every lot. Devices 100% tested at 10Hz are available on request.

Note 5: See the test circuit and frequency response curve for 0.1Hz to 10Hz tester in the Applications Information section.

Note 6: See the test circuit for current noise measurement in the Applications Information section.

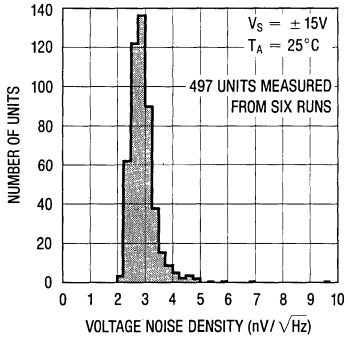
Note 7: This parameter is guaranteed by design and is not tested.

Note 8: The inputs are protected by back-to-back diodes. Current limiting resistors are not used in order to achieve low noise. If differential input voltage exceeds ±0.7V, the input current should be limited to 25mA.

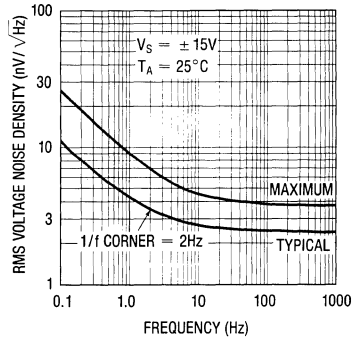
Note 9: The Average Input Offset Drift performance is within the specifications unnulled or when nulled with a pot having a range of 8kΩ to 20kΩ.

TYPICAL PERFORMANCE CHARACTERISTICS

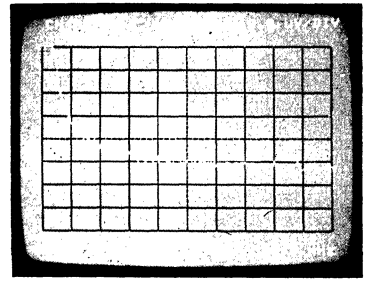
10Hz Voltage Noise Distribution



Voltage Noise vs Frequency



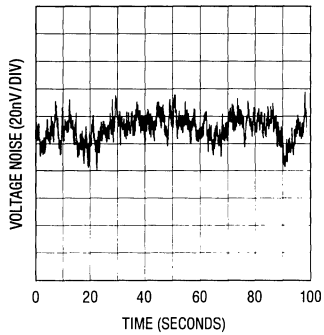
0.02 to 10Hz RMS Noise. Gain = 50,000 (Measured on HP3582 Spectrum Analyzer)



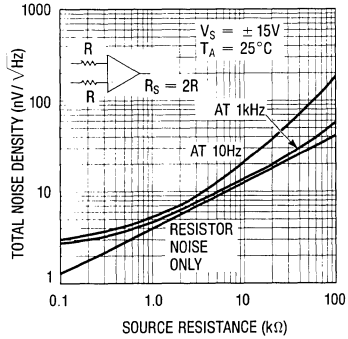
Marker at 2Hz (= 1/f corner) =

$$\frac{179\mu V/\sqrt{Hz}}{50{,}000} = 3.59\frac{nV}{\sqrt{Hz}}$$

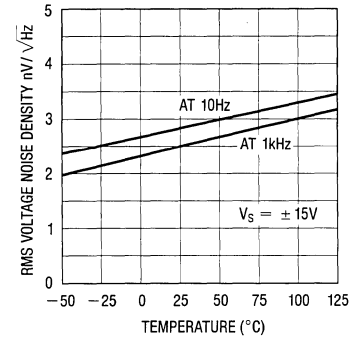
0.01 to 1Hz Peak to Peak Noise



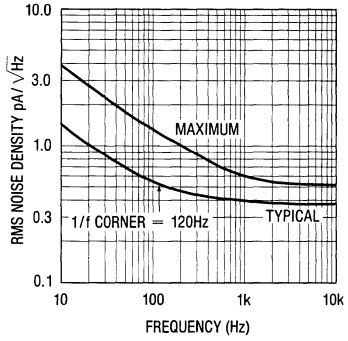
Total Noise vs Source Resistance



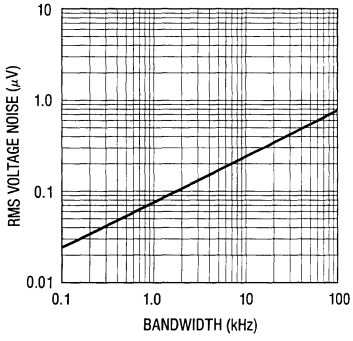
Voltage Noise vs Temperature



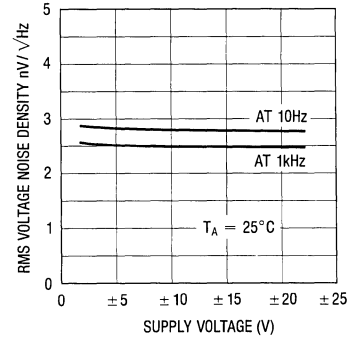
Current Noise vs Frequency



Wideband Voltage Noise (0.1Hz to Frequency Indicated)

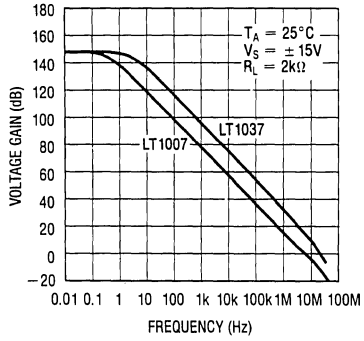


Voltage Noise vs Supply Voltage

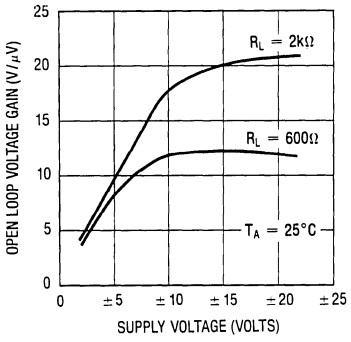


TYPICAL PERFORMANCE CHARACTERISTICS

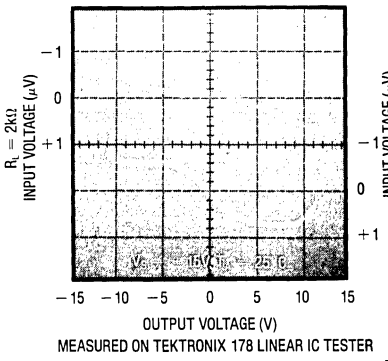
Voltage Gain vs Frequency



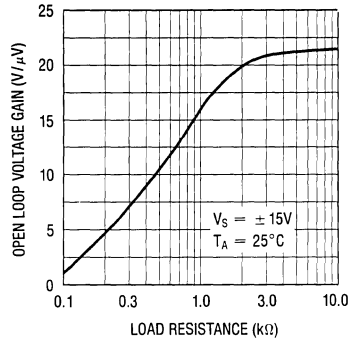
Voltage Gain vs Supply Voltage



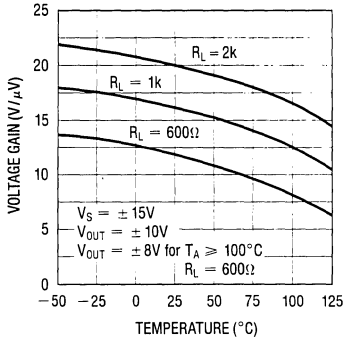
Voltage Gain, R_L = 2K and 600Ω



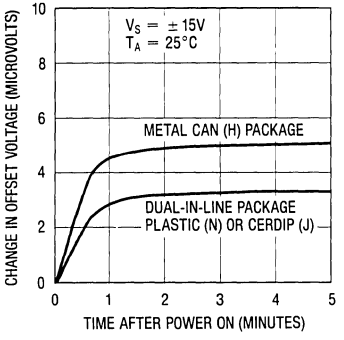
Voltage Gain vs Load Resistance



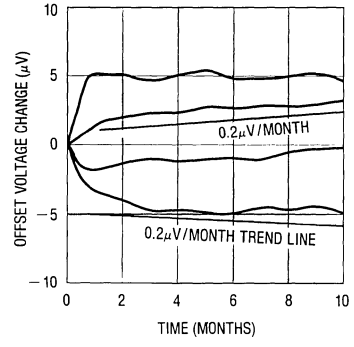
Voltage Gain vs Temperature



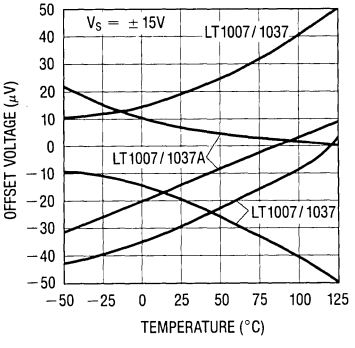
Warm-Up Drift



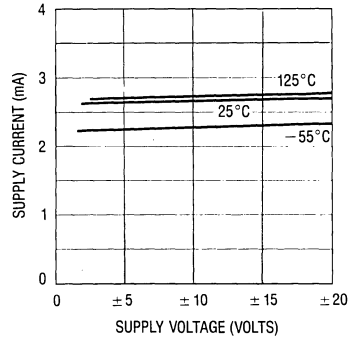
Long Term Stability of Four Representative Units



Offset Voltage Drift with Temperature of Representative Units

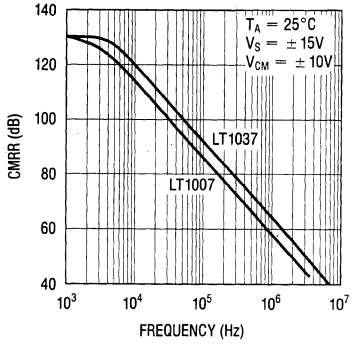


Supply Current vs Supply Voltage

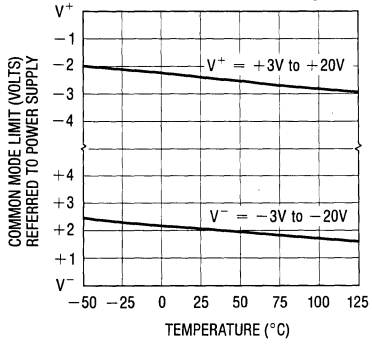


TYPICAL PERFORMANCE CHARACTERISTICS

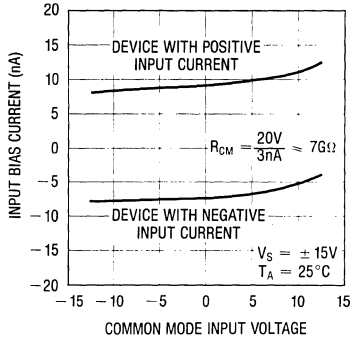
Common Mode Rejection vs Frequency



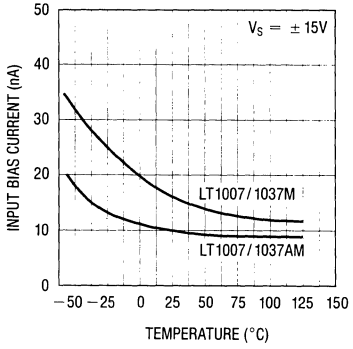
Common Mode Limit vs Temperature



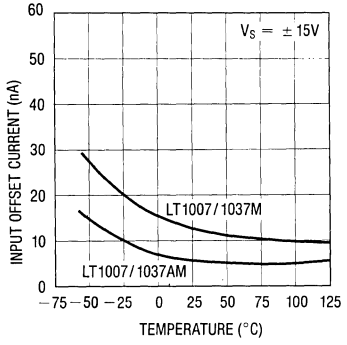
Input Bias Current Over the Common Mode Range



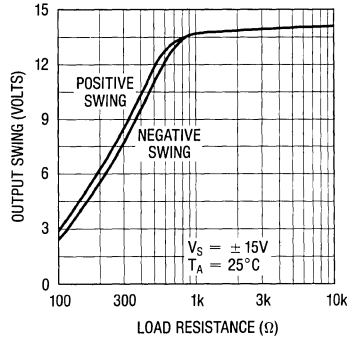
Input Bias Current vs Temperature



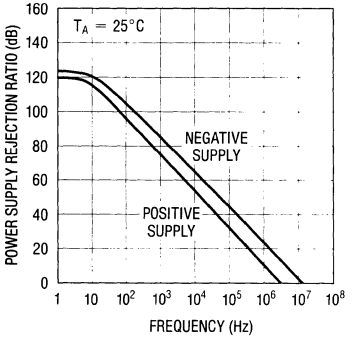
Input Offset Current vs Temperature



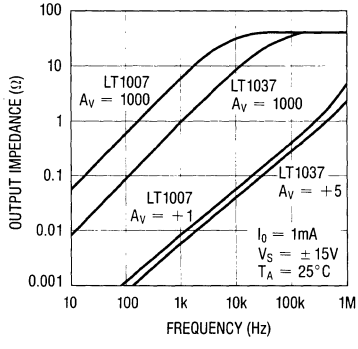
Output Swing vs Load Resistance



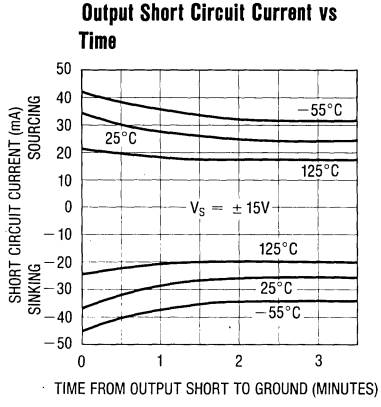
PSRR vs Frequency



Closed Loop Output Impedance

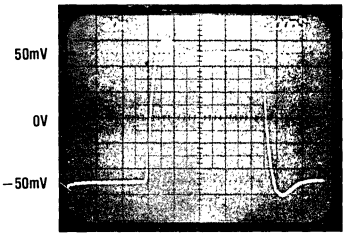


Output Short Circuit Current vs Time



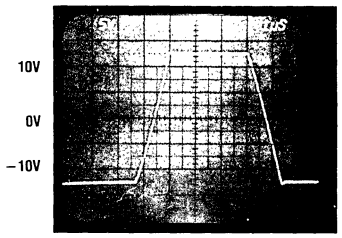
TYPICAL PERFORMANCE CHARACTERISTICS

LT1037 Small Signal Transient Response



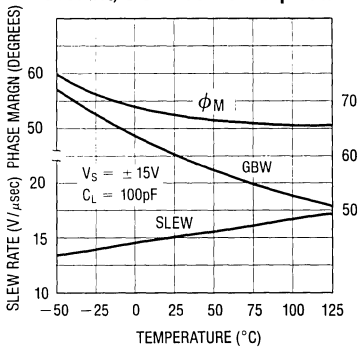
$A_{VCL} = +5$, $V_S = \pm 15V$
$C_L = 15pF$

LT1037 Large Signal Response

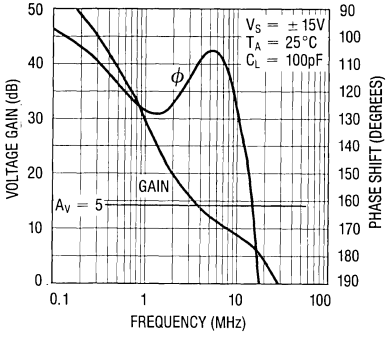


$A_{VCL} = +5$, $V_S = \pm 15V$

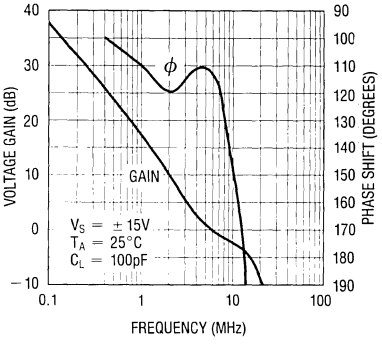
LT1037 Phase Margin, Gain Bandwidth Product, Slew Rate vs Temperature



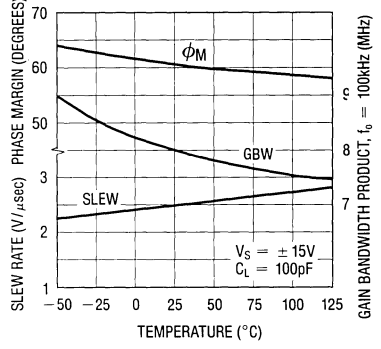
LT1037 Gain, Phase Shift vs Frequency



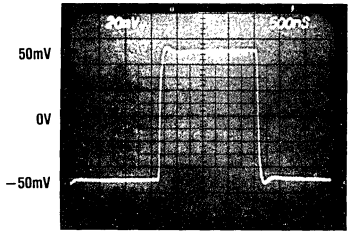
LT1007 Gain, Phase Shift vs Frequency



LT1007 Phase Margin, Gain-Bandwidth Product, Slew Rate vs Temperature

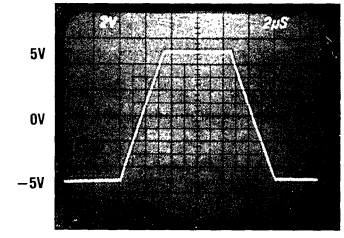


LT1007 Small Signal Transient Response



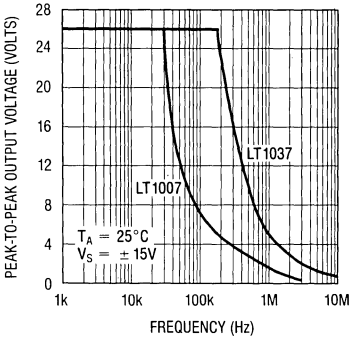
$A_{VCL} = +1$, $V_S = \pm 15V$
$C_L = 15pF$

LT1007 Large Signal Response



$A_{VCL} = -1$, $V_S = \pm 15V$

Maximum Undistorted Output vs Frequency



APPLICATIONS INFORMATION

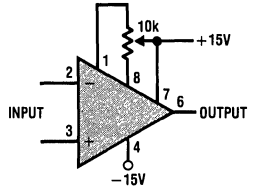
General

The LT1007/1037 series devices may be inserted directly into OP-07, OP-27, OP-37, and 5534 sockets with or without removal of external compensation or nulling components. In addition, the LT1007/1037 may be fitted to 741 sockets with the removal or modification of external nulling components.

Offset Voltage Adjustment

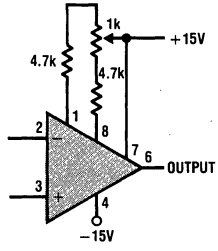
The input offset voltage of the LT1007/1037 and its drift with temperature, are permanently trimmed at wafer testing to a low level. However, if further adjustment of V_{OS} is necessary, the use of a 10k nulling potentiometer will not degrade drift with temperature. Trimming to a value other than zero creates a drift of $(V_{OS}/300)\ \mu V/°C$, e.g., if V_{OS} is adjusted to $300\mu V$, the change in drift will be $1\mu V/°C$.

Standard Adjustment



The adjustment range with a 10k pot is approximately $\pm 2.5mV$. If less adjustment range is needed, the sensitivity and resolution of the nulling can be improved by using a smaller pot in conjunction with fixed resistors. The example has an approximate null range of $\pm 200\mu V$.

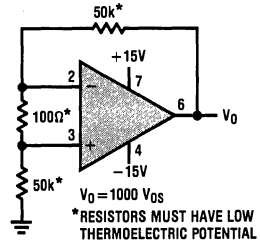
Improved Sensitivity Adjustment



Offset Voltage and Drift

Thermocouple effects, caused by temperature gradients across dissimilar metals at the contacts to the input terminals, can exceed the inherent drift of the amplifier unless proper care is exercised. Air currents should be minimized, package leads should be short, the two input leads should be close together and maintained at the same temperature.

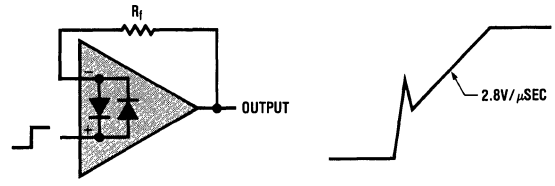
The circuit shown to measure offset voltage is also used as the burn-in configuration for the LT1007/1037, with the supply voltages increased to $\pm 20V$.



Test Circuit for Offset Voltage and Offset Voltage Drift with Temperature

Unity Gain Buffer Applications (LT1007 Only)

When $R_f \leq 100\Omega$ and the input is driven with a fast, large signal pulse ($>1V$), the output waveform will look as shown in the pulsed operation diagram.



During the fast feedthrough-like portion of the output, the input protection diodes effectively short the output to the input and a current, limited only by the output short circuit protection, will be drawn by the signal generator. With $R \geq 500\Omega$, the output is capable of handling the current requirements ($I_L \leq 20mA$ at 10V) and the amplifier stays in its active mode and a smooth transition will occur.

As with all operational amplifiers when $R_f > 2k\Omega$, a pole will be created with R_f and the amplifier's input capacitance, creating additional phase shift and reducing the phase margin. A small capacitor (20pF to 50pF) in parallel with R_f will eliminate this problem.

APPLICATIONS INFORMATION — NOISE

Noise Testing

The 0.1Hz to 10Hz peak-to-peak noise of the LT1007/1037 is measured in the test circuit shown. The frequency response of this noise tester indicates that the 0.1Hz corner is defined by only one zero. The test time to measure 0.1Hz to 10Hz noise should not exceed 10 seconds, as this time limit acts as an additional zero to eliminate noise contributions from the frequency band below 0.1Hz.

Measuring the typical 60nV peak-to-peak noise performance of the LT1007/1037 requires special test precautions:

(a) The device should be warmed up for at least five minutes. As the op amp warms up, its offset voltage changes typically 3μV due to its chip temperature increasing 10°C to 20°C from the moment the power supplies are turned on. In the 10 second measurement interval these temperature-induced effects can easily exceed tens of nanovolts.

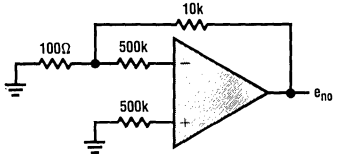
(b) For similar reasons, the device must be well shielded from air currents to eliminate the possibility of thermoelectric effects in excess of a few nanovolts, which would invalidate the measurements.

(c) Sudden motion in the vicinity of the device can also "feedthrough" to increase the observed noise.

A noise-voltage density test is recommended when measuring noise on a large number of units. A 10Hz noise-voltage density measurement will correlate well with a 0.1Hz to 10Hz peak-to-peak noise reading since both results are determined by the white noise and the location of the 1/f corner frequency.

Current noise is measured in the circuit shown and calculated by the following formula:

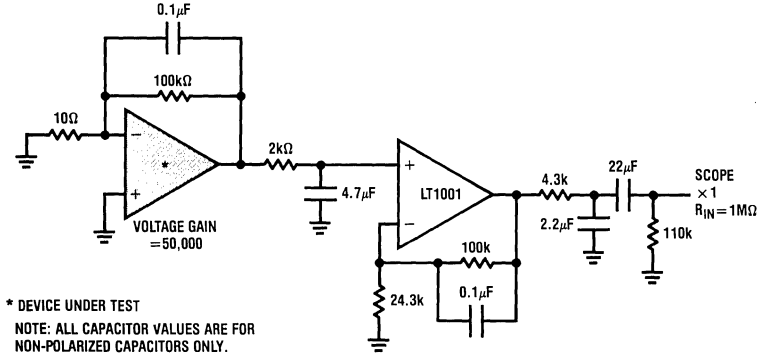
$$i_n = \frac{[e^2_{no} - (130nV)^2]^{1/2}}{1M\Omega \times 100}$$



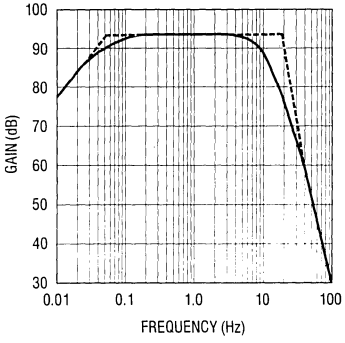
The LT1007/1037 achieves its low noise, in part, by operating the input stage at 120μA versus the typical 10μA of most other op amps. Voltage noise is inversely proportional while current noise is directly proportional to the square root of the stage current. Therefore the LT1007/1037's current noise will be relatively high. At low frequencies, the low 1/f current noise corner frequency (≈120Hz) minimizes current noise to some extent.

In most practical applications, however, current noise will not limit system performance. This is illustrated in

0.1Hz to 10Hz Noise Test Circuit



0.1Hz to 10Hz p-p Noise Tester Frequency Response



the total noise versus source resistance plot, where total noise = [(voltage noise)^2 + (current noise × R_S)^2 + (resistor noise)^2]$^{1/2}$

Three regions can be identified as a function of source resistance:

(i) $R_S \leq 400\Omega$. Voltage noise dominates

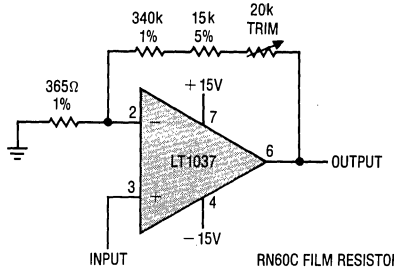
(ii) $400\Omega \leq R_S \leq 50k\Omega$ at 1kHz
$400\Omega \leq R_S \leq 8k\Omega$ at 10Hz
} Resistor noise dominates

(iii) $R_S > 50k\Omega$ at 1kHz
$R_S > 8k\Omega$ at 10Hz
} Current noise dominates

Clearly the LT1007/1037 should not be used in region (iii), where total system noise is at least six times higher than the voltage noise of the op amp, i.e., the low voltage noise specification is completely wasted.

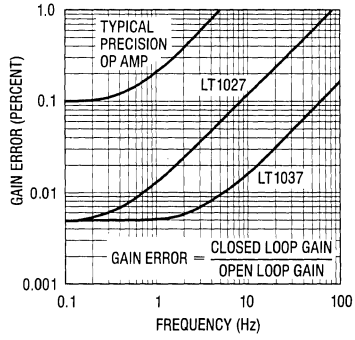
TYPICAL APPLICATIONS

Gain 1000 Amplifier with 0.01% Accuracy, DC to 5Hz

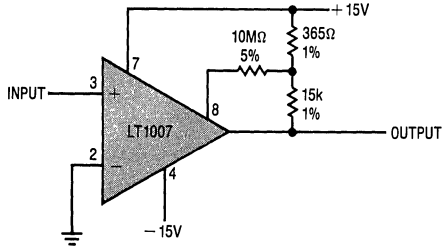


The high gain and wide bandwidth of the LT1037 and (LT1007) is useful in low frequency high closed loop gain amplifier applications. A typical precision Op Amp may have an open loop gain of one million with 500kHz bandwidth. As the gain error plot shows, this device is capable of 0.1% amplifying accuracy up to 0.3Hz only. Even instrumentation range signals can vary at a faster rate. The LT1037's "gain precision — bandwidth product" is 200 times higher, as shown.

Gain Error vs Frequency Closed Loop Gain = 1000



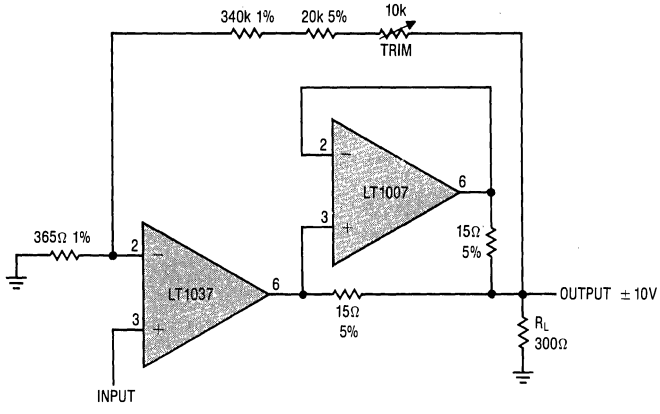
Microvolt Comparator with Hysteresis



Positive feedback to one of the nulling terminals creates approximately 5μV of hysteresis. Output can sink 16mA.

Input offset voltage is typically changed less than 5μV due to the feedback.

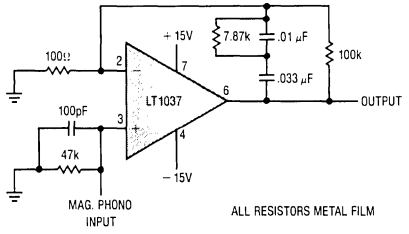
Precision Amplifier Drives 300Ω Load to ±10V



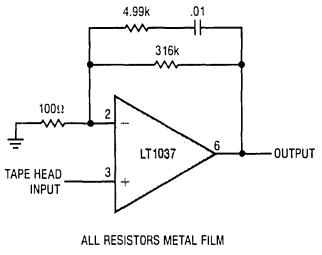
The addition of the LT1007 doubles the amplifier's output drive to ±33mA. Gain accuracy is 0.02%, slightly degraded compared to above because of self heating of the LT1037 under load.

TYPICAL APPLICATIONS

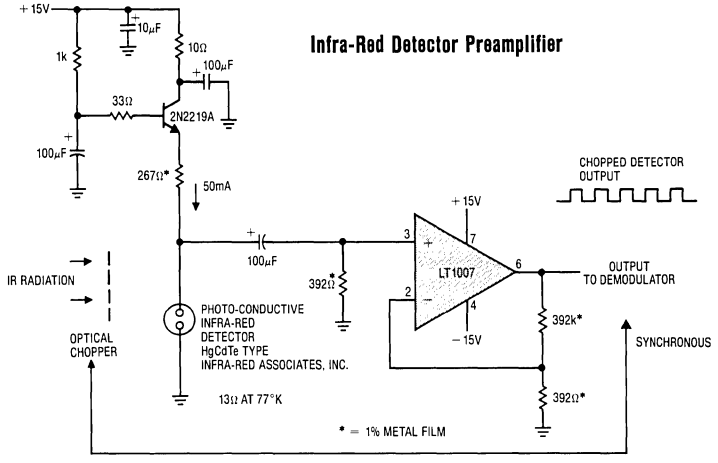
Phono Preamplifier



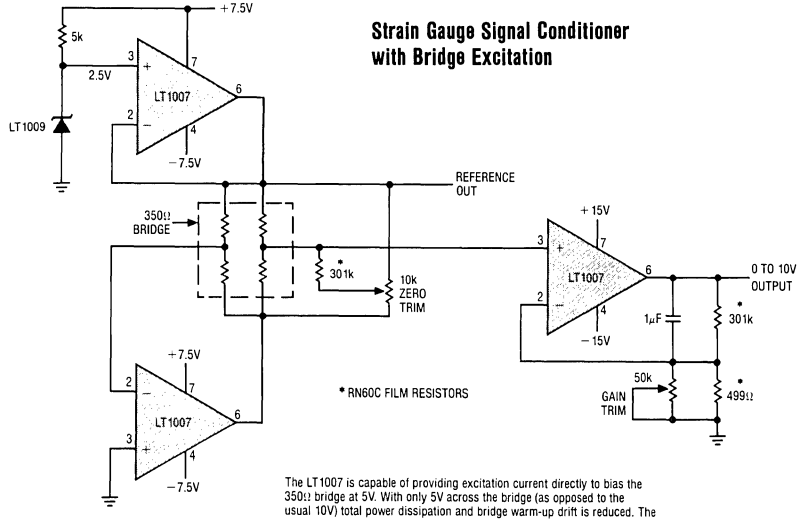
Tape Head Amplifier



Infra-Red Detector Preamplifier

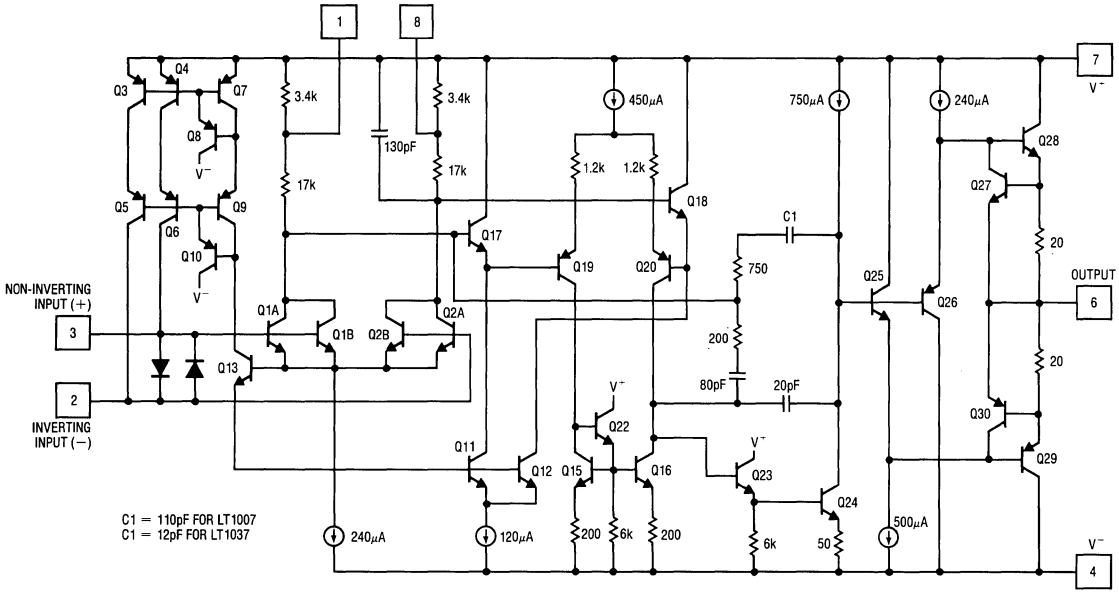


Strain Gauge Signal Conditioner with Bridge Excitation



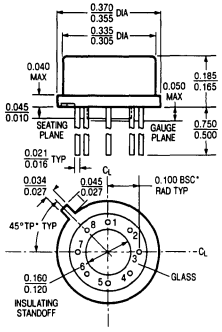
The LT1007 is capable of providing excitation current directly to bias the 350Ω bridge at 5V. With only 5V across the bridge (as opposed to the usual 10V) total power dissipation and bridge warm-up drift is reduced. The bridge output signal is halved, but the LT1007 can amplify the reduced signal accurately.

SCHEMATIC DIAGRAM



PACKAGE DESCRIPTION

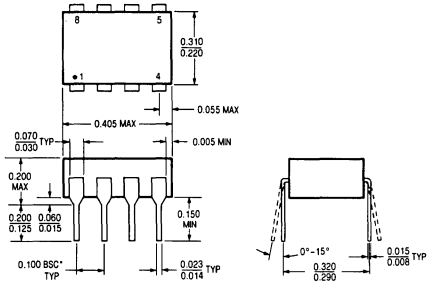
H Package
Metal Can



NOTE: DIMENSIONS IN INCHES

$T_j$max	Θ_{ja}	Θ_{jc}
150°C	150°C/W	45°C/W

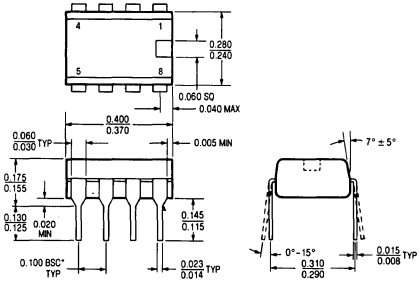
J8 Package
8 Lead Hermetic Dip



NOTE: DIMENSIONS IN INCHES UNLESS OTHERWISE NOTED.
*LEADS WITHIN 0.007 OF TRUE POSITION (TP) AT GAUGE PLANE

$T_j$max	Θ_{ja}
150°C	100°C/W

N8 Package
8 Lead Plastic



NOTE: DIMENSIONS IN INCHES UNLESS OTHERWISE NOTED.
*LEADS WITHIN 0.007 OF TRUE POSITION (TP) AT GAUGE PLANE.

$T_j$max	Θ_{ja}
100°C	130°C/W

Picoamp Input Current, Microvolt Offset, Low Noise Op Amp

FEATURES

- *Guaranteed* Bias Current
  - 25°C . . . . . 100pA max.
  - −55°C to 125°C . . . . . 600pA max.
- *Guaranteed* Offset Voltage . . . . . 120μV max.
- *Guaranteed* Drift . . . . . 1.5μV/°C max.
- Low Noise, 0.1Hz to 10Hz 0.5μVp-p
- *Guaranteed* Low Supply Current . . . . 600μA max.
- *Guaranteed* CMRR . . . . . 114 dB min.
- *Guaranteed* PSRR . . . . . 114 db min.
- *Guaranteed* Voltage Gain with 5mA load current

APPLICATIONS

- Precision instrumentation
- Charge integrators
- Wide dynamic range logarithmic amplifiers
- Light meters
- Low frequency active filters
- Standard cell buffers
- Thermocouple amplifiers

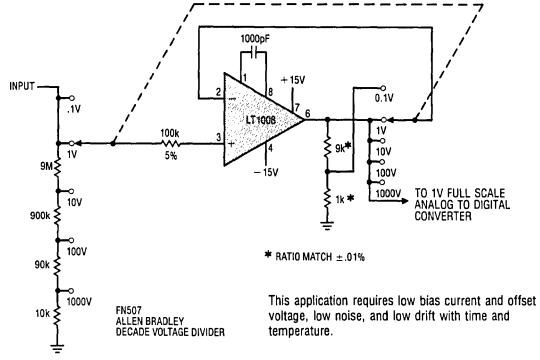
DESCRIPTION

The LT1008 is a universal precision operational amplifier which can be used in practically all precision applications. The LT1008 combines for the first time picoampere bias currents (which are maintained over the full −55°C to 125°C temperature range) microvolt offset voltage (and low drift with time and temperature), low voltage and current noise, and low power dissipation. Extremely high common-mode and power supply rejection ratios, and the ability to deliver 5mA load current with high voltage gain round out the LT1008's superb precision specifications.

The all around excellence of the LT1008 eliminates the necessity of the time consuming error analysis procedure of precision system design in many applications; the LT1008 can be stocked as the universal precision op amp.

The LT1008 is externally compensated with a single capacitor for additional flexibility in shaping the frequency response of the amplifier. It plugs into and upgrades all standard LM108A/308A applications. For an internally compensated version with even lower offset voltage but otherwise similar performance see the LT1012.

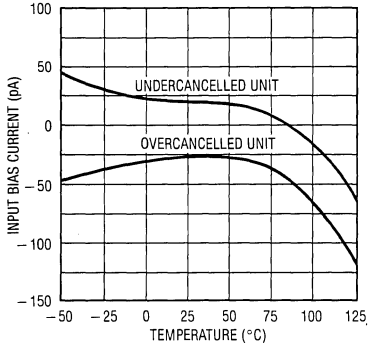
Input Amplifier for 4½ Digit Voltmeter



FN507
ALLEN BRADLEY DECADE VOLTAGE DIVIDER

This application requires low bias current and offset voltage, low noise, and low drift with time and temperature.

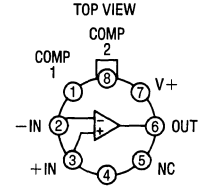
Input Bias Current vs Temperature



ABSOLUTE MAXIMUM RATING

Supply Voltage ..... ±20V
Differential Input Current (Note 1) ..... ±10mA
Input Voltage ..... ±20V
Output Short Circuit Duration ..... Indefinite
Operating Temperature Range
LT1008M ..... −55°C to 125°C
LT1008C ..... 0°C to 70°C
Storage Temperature Range
All Devices ..... −65°C to 150°C
Lead Temperature (Soldering, 10 sec.) ..... 300°C

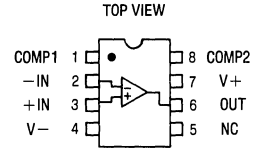
PACKAGE/ORDER INFORMATION



METAL CAN H PACKAGE

ORDER PART NO.

LT1008MH
LT1008CH



PLASTIC DIP N8 PACKAGE

LT1008CN8

ELECTRICAL CHARACTERISTICS $V_S = \pm 15V$, $V_{CM} = 0V$, $T_A = 25°C$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	LT1008M MIN	LT1008M TYP	LT1008M MAX	LT1008C MIN	LT1008C TYP	LT1008C MAX	UNITS
V_{OS}	Input Offset Voltage			30	120		30	120	μV
		Note 2		40	180		40	180	μV
	Long Term Input Offset Voltage Stability			0.3			0.3		μV/month
I_{OS}	Input Offset Current			30	100		30	100	pA
		Note 2		40	150		40	150	pA
I_B	Input Bias Current			±30	±100		±30	±100	pA
		Note 2		±40	±150		±40	±150	pA
e_n	Input Noise Voltage	0.1Hz to 10Hz		0.5			0.5		μVp-p
e_n	Input Noise Voltage Density	f_0 = 10Hz (Note 3)		17	30		17	30	nV/√Hz
		f_0 = 1000Hz (Note 4)		14	22		14	22	nV/√Hz
i_n	Input Noise Current Density	f_0 = 10Hz		20			20		fA/√Hz
A_{VOL}	Large Signal Voltage Gain	$V_{OUT} = \pm 12V$, $R_L \geq 10k\Omega$	200	2000		200	2000		V/mV
		$V_{OUT} = \pm 10V$, $R_L \geq 2k\Omega$	120	600		120	600		V/mV
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm 13.5V$	114	132		114	132		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 2V$ to $\pm 20V$	114	132		114	132		dB
	Input Voltage Range		±13.5	±14.0		±13.5	±14.0		V
V_{OUT}	Output Voltage Swing	$R_L = 10k\Omega$	±13	±14		±13	±14		V
	Slew Rate	$C_f = 30pF$	0.1	0.2		0.1	0.2		V/μsec
I_S	Supply Current	Note 2		380	600		380	600	μA

ELECTRICAL CHARACTERISTICS

$V_S = \pm 15V$, $V_{CM} = 0V$, $0°C \leq T_A \leq 70°C$ for the LT1008C and $-55°C \leq T_A \leq 125°C$ for the LT1008M, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		LT1008M MIN	LT1008M TYP	LT1008M MAX	LT1008C MIN	LT1008C TYP	LT1008C MAX	UNITS
V_{OS}	Input Offset Voltage		●		50	250		40	180	μV
		Note 2	●		60	320		50	250	μV
	Average Temperature Coefficient of Input Offset Voltage		●		0.2	1.5		0.2	1.5	μV/°C
I_{OS}	Input Offset Current		●		60	250		40	180	pA
		Note 2	●		80	350		50	250	pA
	Average Temperature Coefficient of Input Offset Current		●		0.4	2.5		0.4	2.5	pA/°C
I_B	Input Bias Current		●		±80	±600		±40	±180	pA
		Note 2	●		±150	±800		±50	±250	pA
	Average Temperature Coefficient of Input Bias Current		●		0.6	6.0		0.4	2.5	pA/°C
A_{VOL}	Large Signal Voltage Gain	$V_{OUT} = \pm 12V$, $R_L \geq 10k\Omega$	●	100	1000		150	1500		V/mV
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm 13.5V$	●	108	128		110	130		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 2.5V$ to $\pm 20V$	●	108	126		110	128		dB
	Input Voltage Range		●	±13.5			±13.5			V
V_{OUT}	Output Voltage Swing	$R_L = 10k\Omega$	●	±13	±14		±13	±14		V
I_S	Supply Current		●		400	800		400	800	μA

The ● denotes the specifications which apply over the full operating temperature range.

Note 1: Differential input voltages greater than 1V will cause excessive current to flow through the input protection diodes unless current limiting resistors are used.

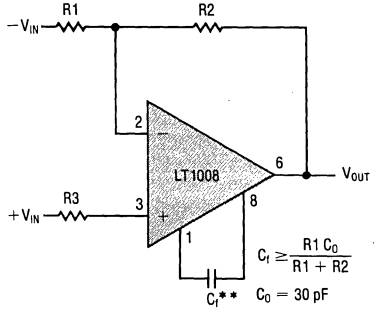
Note 2: These specifications apply for $\pm 2V \leq V_S \leq \pm 20V$ ($\pm 2.5V \leq V_S \leq \pm 20V$ over the temperature range) and $-13.5V \leq V_{CM} \leq 13.5V$ (for $V_S = \pm 15V$).

Note 3: 10Hz noise voltage density is sample tested on every lot. Devices 100% tested at 10Hz are available on request.

Note 4: This parameter is tested on a sample basis only.

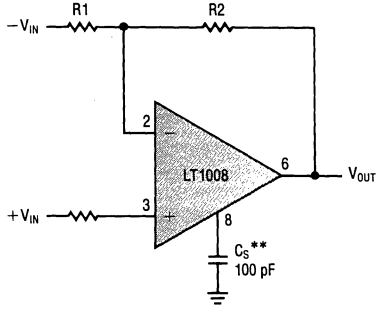
FREQUENCY COMPENSATION CIRCUITS

Standard Compensation Circuit



** BANDWIDTH AND SLEW RATE ARE PROPORTIONAL TO $1/C_f$

Alternate* Frequency Compensation



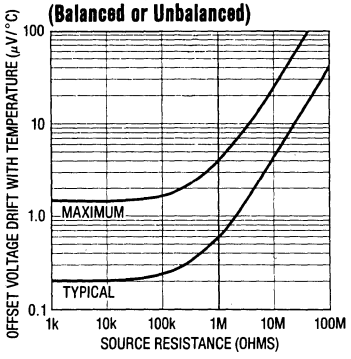
* IMPROVES REJECTION OF POWER SUPPLY NOISE BY A FACTOR OF 5.

** BANDWIDTH AND SLEW RATE ARE PROPORTIONAL TO $1/C_S$

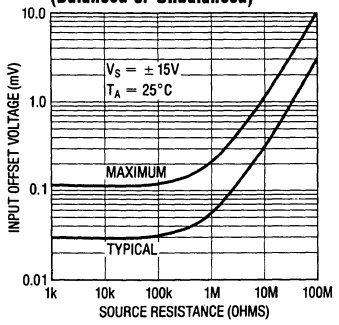
FOR $\frac{R2}{R1} > 200$ NO EXTERNAL FREQUENCY COMPENSATION IS NECESSARY

TYPICAL PERFORMANCE CHARACTERISTICS

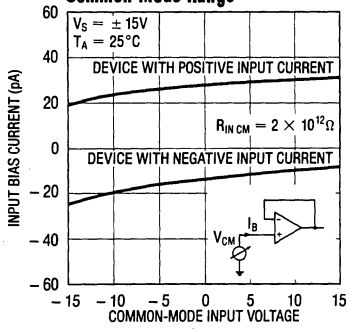
Offset Voltage Drift vs Source Resistance (Balanced or Unbalanced)



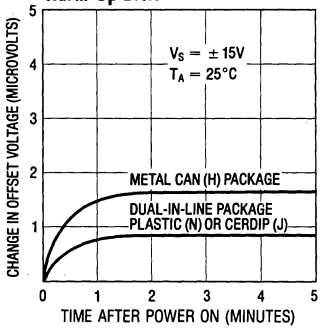
Offset Voltage vs Source Resistance (Balanced or Unbalanced)



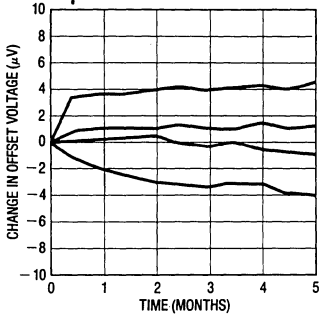
Input Bias Current Over Common Mode Range



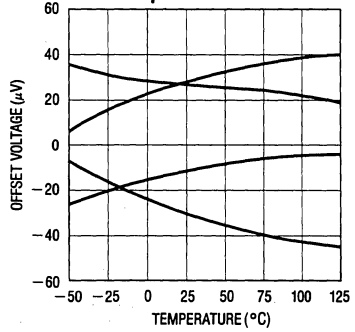
Warm-Up Drift



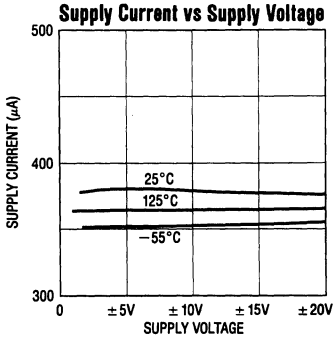
Long Term Stability of Four Representative Units



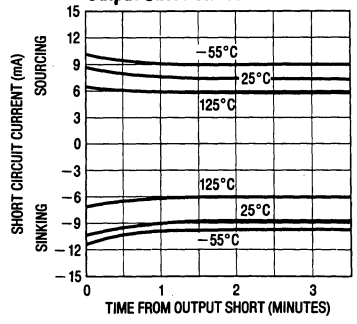
Offset Voltage Drift with Temperature of Four Representative Units



Supply Current vs Supply Voltage

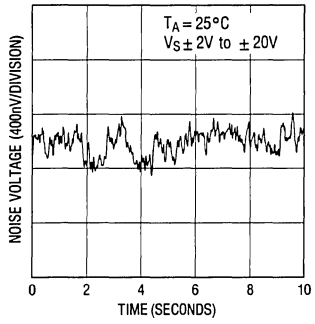


Output Short Circuit Current vs Time

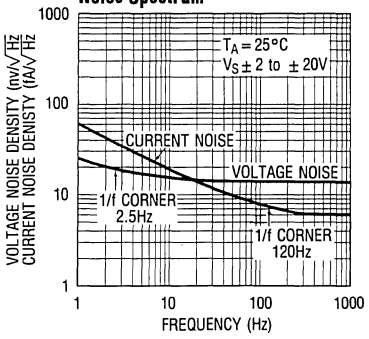


TYPICAL PERFORMANCE CHARACTERISTICS

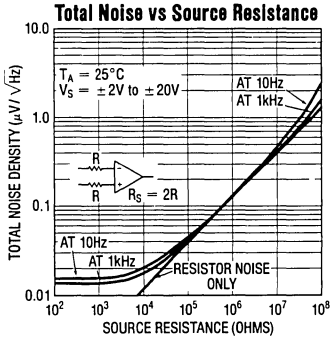
0.1Hz to 10Hz Noise



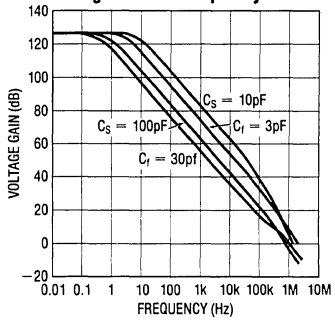
Noise Spectrum



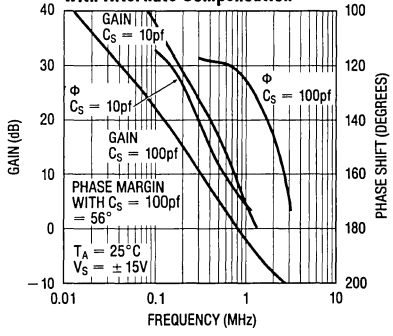
Total Noise vs Source Resistance



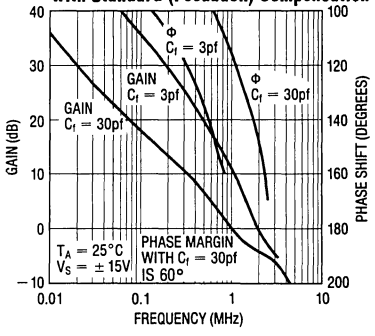
Voltage Gain vs Frequency



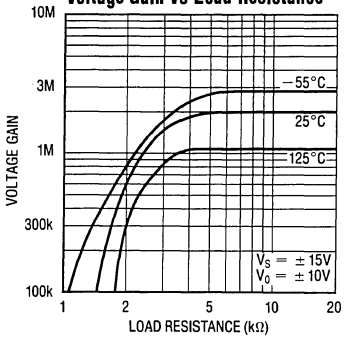
Gain, Phase Shift vs Frequency with Alternate Compensation



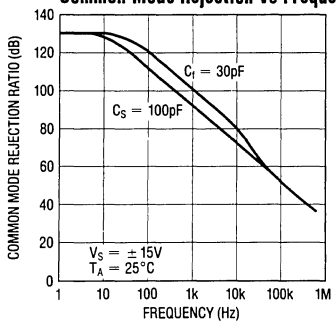
Gain, Phase Shift vs Frequency with Standard (Feedback) Compensation



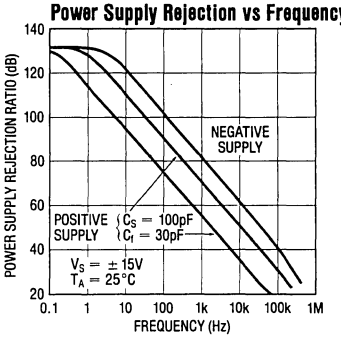
Voltage Gain vs Load Resistance



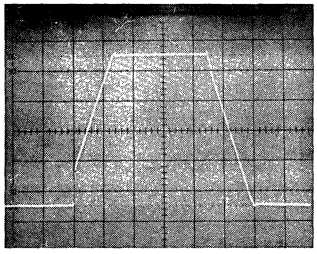
Common Mode Rejection vs Frequency



Power Supply Rejection vs Frequency

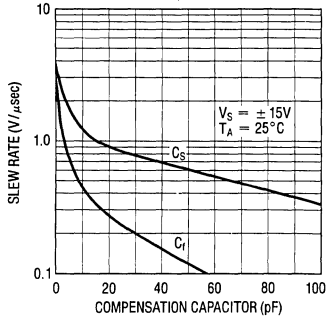


Large Signal Transient Response

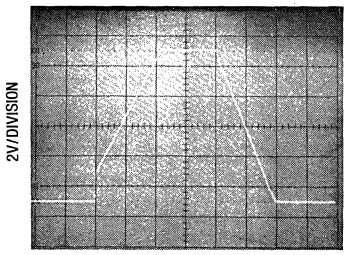


$A_V = +1$, $C_S = 100pF$, $20\mu sec/DIV$

Slew Rate vs Compensation Capacitance

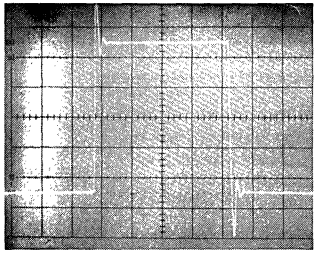


Large Signal Transient Response



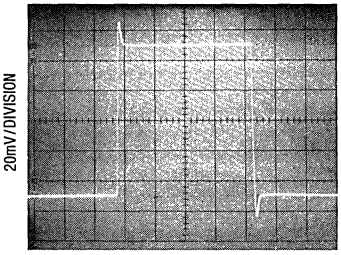
$A_V = +1$, $C_f = 30pF$, $20\mu sec/DIV$

Small Signal Transient Response



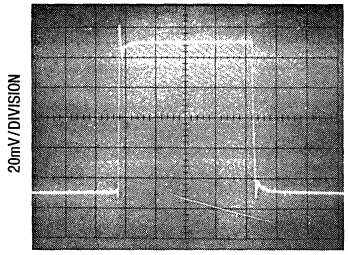
$A_V = +1$, $C_S = 100pF$, $C_{LOAD} = 100pF$, $5\mu sec/DIV$

Small Signal Transient Response



$A_V = +1$, $C_S = 100pF$, $C_{LOAD} = 600pF$, $5\mu sec/DIV$

Small Signal Transient Response



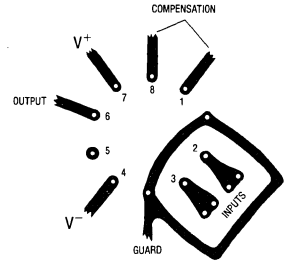
$A_V = +1$, $C_f = 30pF$, $C_{LOAD} = 100pF$, $5\mu sec/DIV$

APPLICATIONS INFORMATION

Achieving Picoampere/Microvolt Performance

In order to realize the picoampere — microvolt level accuracy of the LT1008, proper care must be exercised. For example, leakage currents in circuitry external to the op amp can significantly degrade performance. High quality insulation should be used (e.g. Teflon, Kel-F); cleaning of all insulating surfaces to remove fluxes and other residues will probably be required. Surface coating may be necessary to provide a moisture barrier in high humidity environments.

Board leakage can be minimized by encircling the input circuitry with a guard ring operated at a potential close to that of the inputs: in inverting configurations the guard ring should be tied to ground, in non-inverting connections to the inverting input at pin 2. Guarding both sides of the printed circuit board is required. Bulk leakage reduction depends on the guard ring width. Nanoampere level leakage into the compensation terminals can affect offset voltage and drift with temperature.

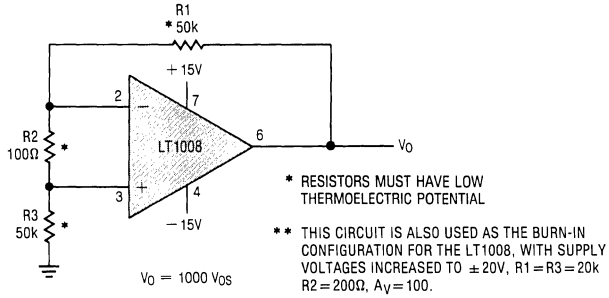


APPLICATIONS INFORMATION

Microvolt level error voltages can also be generated in the external circuitry. Thermocouple effects caused by temperature gradients across dissimilar metals at the contacts to the input terminals can exceed the inherent drift of the amplifier. Air currents over device leads should be minimized, package leads should be short, and the two input leads should be as close together as possible and maintained at the same temperature.

The LT1008 is specified over a wide range of power-supply voltages from ±2V to ±18V. Operation with lower supplies is possible down to ±1.0V (two Ni-Cad-batteries).

Test Circuit for Offset Voltage and its Drift with Temperature



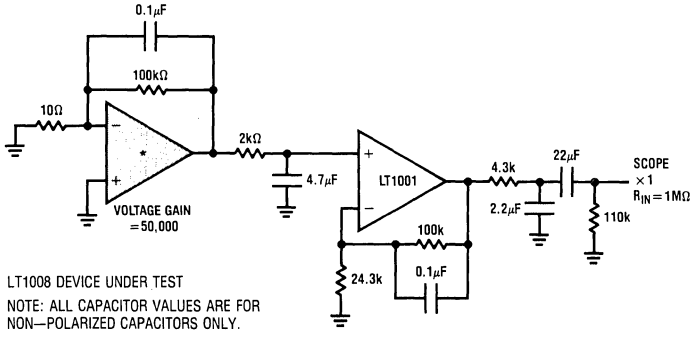
Noise Testing

The 0.1Hz to 10Hz peak-to-peak noise of the LT1008 is measured in the test circuit shown. The frequency response of this noise tester indicates that the 0.1Hz corner is defined by only one zero. The test time to measure 0.1Hz to 10Hz noise should not exceed 10 seconds, as this time limit acts as an additional zero to eliminate noise contributions from the frequency band below 0.1Hz.

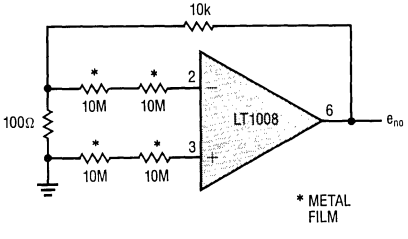
A noise-voltage density test is recommended when measuring noise on a large number of units. A 10Hz noise-voltage density measurement will correlate well with a 0.1Hz to 10Hz peak-to-peak noise reading since both results are determined by the white noise and the location of the 1/f corner frequency.

Current noise is measured in the circuit shown and calculated by the following formula where the noise of the source resistors is subtracted.

0.1Hz to 10Hz Noise Test Circuit



$$i_n = \frac{[e^2_{no} - (820nV)^2]^{1/2}}{40M\Omega \times 100}$$



APPLICATIONS INFORMATION

Frequency Compensation

The LT1008 is externally frequency compensated with a single capacitor. The two standard compensation circuits shown on page 3 are identical to the LM108A/308A frequency compensation schemes. Therefore, the LT1008 operational amplifiers can be inserted directly into LM108A/308A sockets, with similar AC and upgraded DC performance.

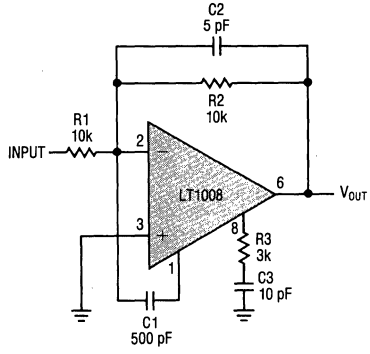
External frequency compensation provides the user with additional flexibility in shaping the frequency response of the amplifier. For example, for a voltage gain of ten, and $C_f = 3pF$, a gain bandwidth product of 5MHz and slew rate of 1.2V/μsec can be realized. For closed loop gains in excess of 200, no external compensation is necessary, and slew rate increases to 4V/μsec. The LT1008 can also be overcompensated (i.e. $C_f > 30pF$ or $C_S > 100pF$) to improve capacitive load handling capability or to narrow noise bandwidth. In many applications, the feedback loop around the amplifier has gain (e.g. logarithmic amplifiers); overcompensation can stabilize these circuits with a single capacitor.

The availability of the compensation terminals permits the use of feedforward frequency compensation to enhance slew rate in low closed loop gain configurations. The inverter slew rate is increased to 1.4V/μsec. The voltage follower feedforward scheme bypasses the amplifier's gain stages and slews at nearly 10V/μsec.

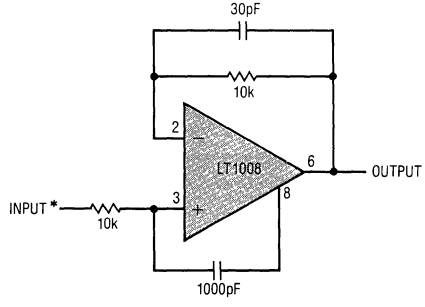
The inputs of the LT1008 are protected with back-to-back diodes. Current limiting resistors are not used, because the leakage of these resistors would prevent the realization of picoampere level bias currents at elevated temperatures. In the voltage follower configuration, when the input is driven by a fast, large signal pulse ($> 1V$), the input protection diodes effectively short the output to the input during slewing, and a current, limited only by the output short circuit protection will flow through the diodes.

The use of a feedback resistor, as shown in the voltage follower, feedforward diagram, is recommended because this resistor keeps the current below the short circuit limit, resulting in faster recovery and settling of the output.

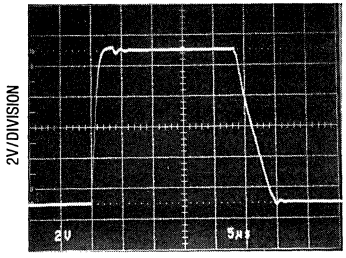
Inverter Feedforward Compensation



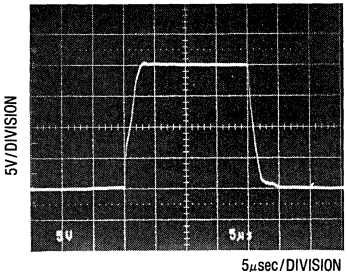
Follower Feedforward Compensation



* SOURCE RESISTANCE ≤ 15k FOR STABILITY



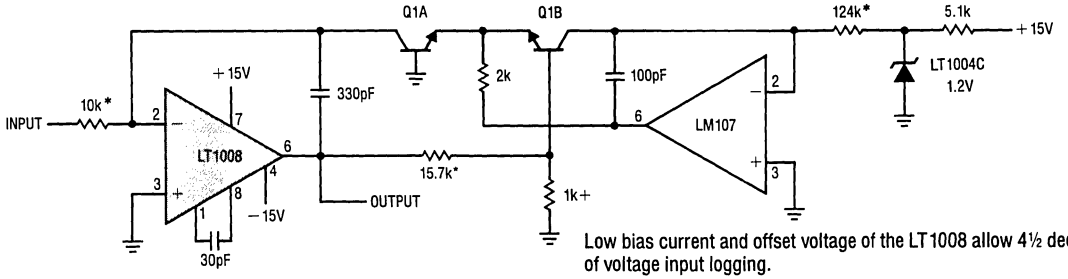
5μsec/DIVISION



5μsec/DIVISION

APPLICATIONS

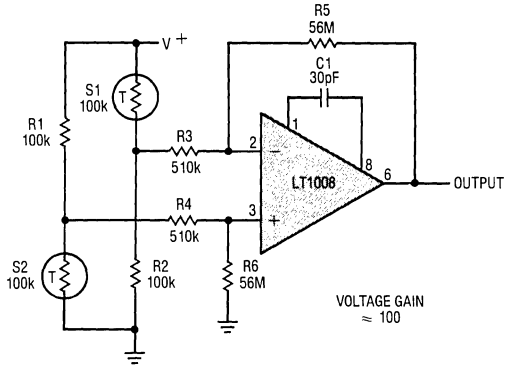
Logarithmic Amplifier



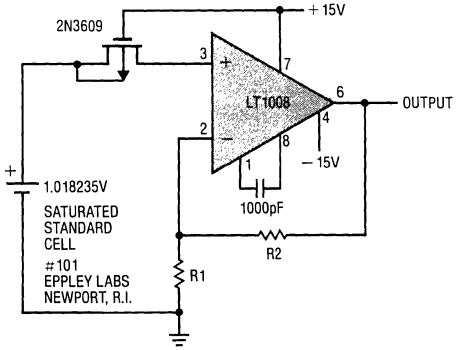
Low bias current and offset voltage of the LT1008 allow 4½ decades of voltage input logging.

+ = TEL. LABS, TYPE Q81
* = 1% FILM RESISTOR
Q1 = 2N2979

Amplifier for Bridge Transducers

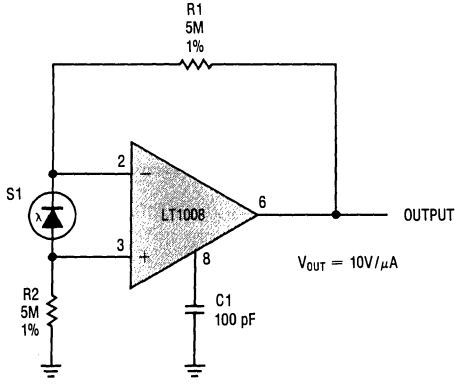


Saturated Standard Cell Amplifier

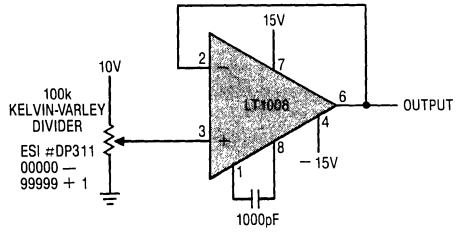


The typical 30pA bias current of the LT1008 will degrade the standard cell by only 1 ppm/year. Noise is a fraction of a ppm. Unprotected gate MOSFET isolates standard cell on power down.

Amplifier For Photodiode Sensor

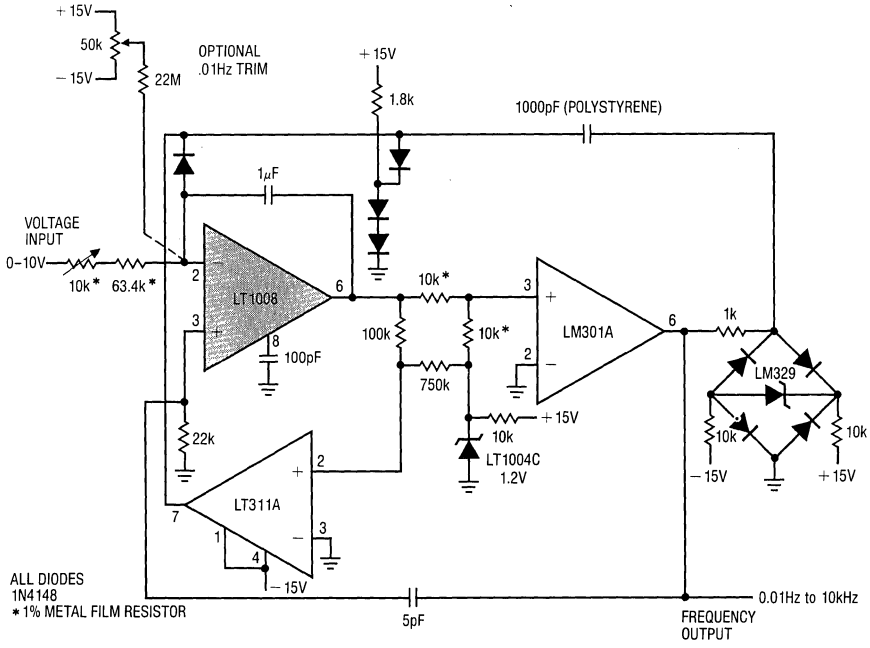


Five Decade Kelvin-Varley Divider Buffered by the LT1008



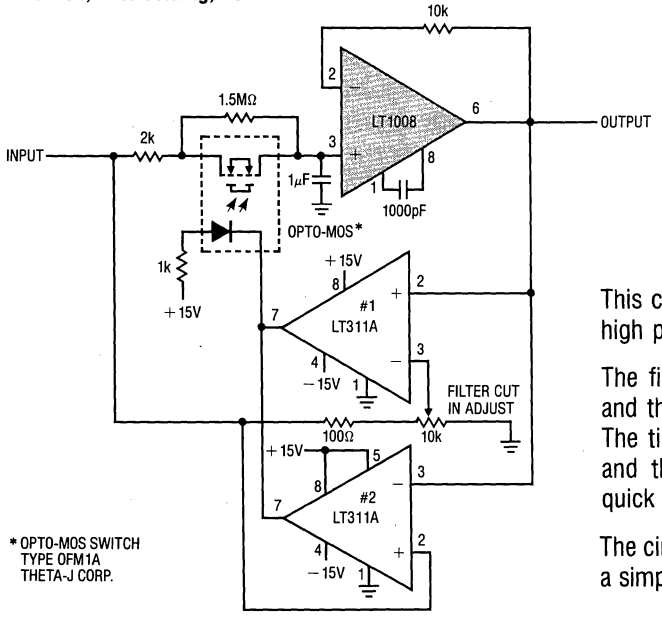
Approximate error due to noise, bias current, common-mode rejection, voltage gain of the amplifier is 1/5 of a least significant bit.

Extended Range Charge Pump Voltage to Frequency Converter



The LT1008 integrator extends low frequency range. Total dynamic range is 0.01Hz to 10kHz (or 120dB) with 0.01% linearity.

Precision, Fast Settling, Low Pass Filter

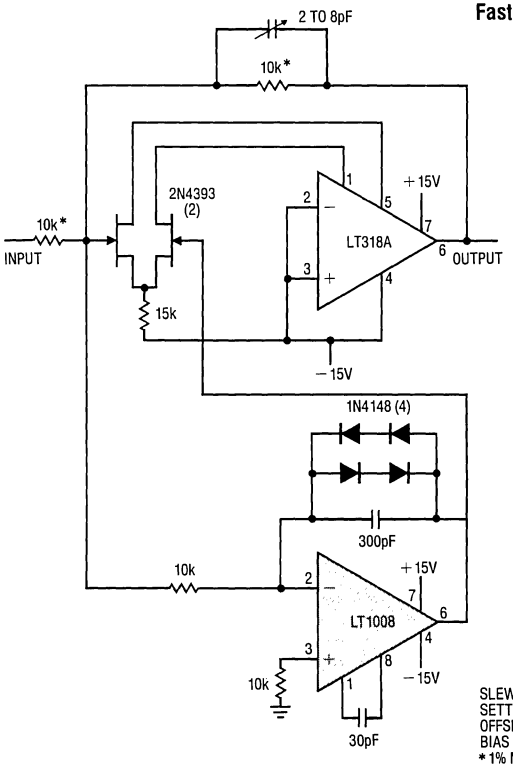


This circuit is useful where fast signal acquisition and high precision are required, as in electronic scales.

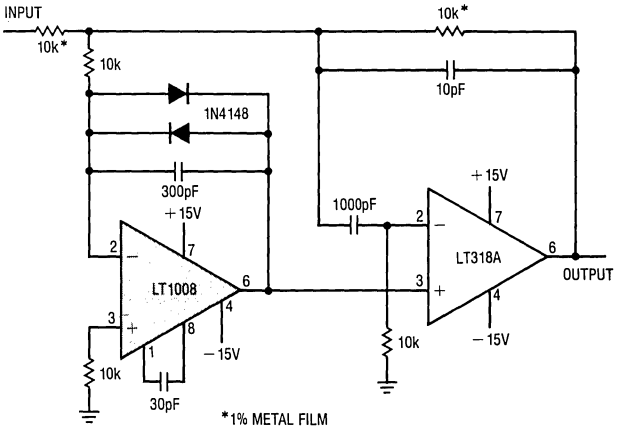
The filter's time constant is set by the 2KΩ resistor and the 1μF capacitor until comparator #1 switches. The time constant is then set by the 1.5MΩ resistor and the 1μF capacitor. Comparator #2 provides a quick reset.

The circuit settles to a final value three times as fast as a simple 1.5MΩ — 1μF filter, with almost no DC error.

Fast Precision Inverters



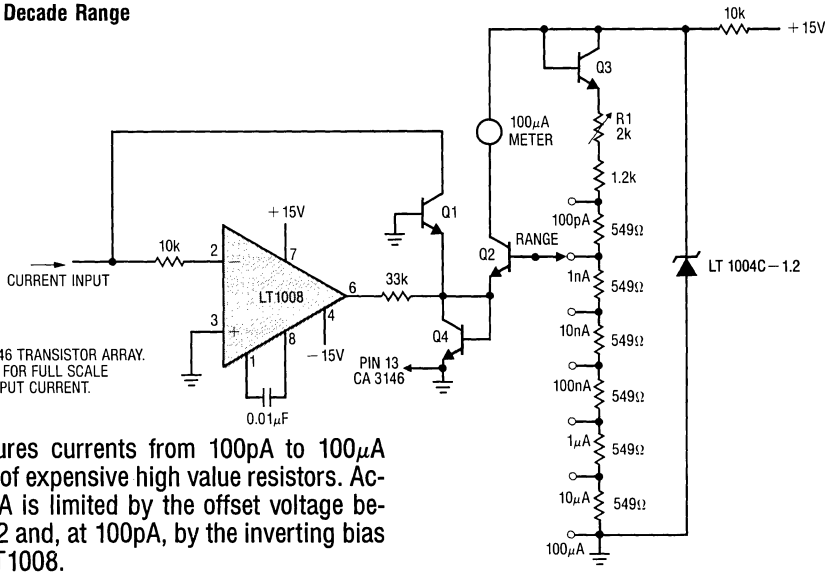
SLEW RATE @ 100V/μS
SETTLING = 5μS TO .01%/10 VOLT STEP
OFFSET VOLTAGE = 30μV
BIAS CURRENT = 30pA
*1% METAL FILM



*1% METAL FILM

FULL POWER BANDWIDTH = 2MHz
SLEW RATE = 50V/μsec
SETTLING (10V STEP) = 12μS TO 0.01%
BIAS CURRENT DC = 30pA
OFFSET DRIFT = 0.3μV/°C
OFFSET VOLTAGE = 30μV

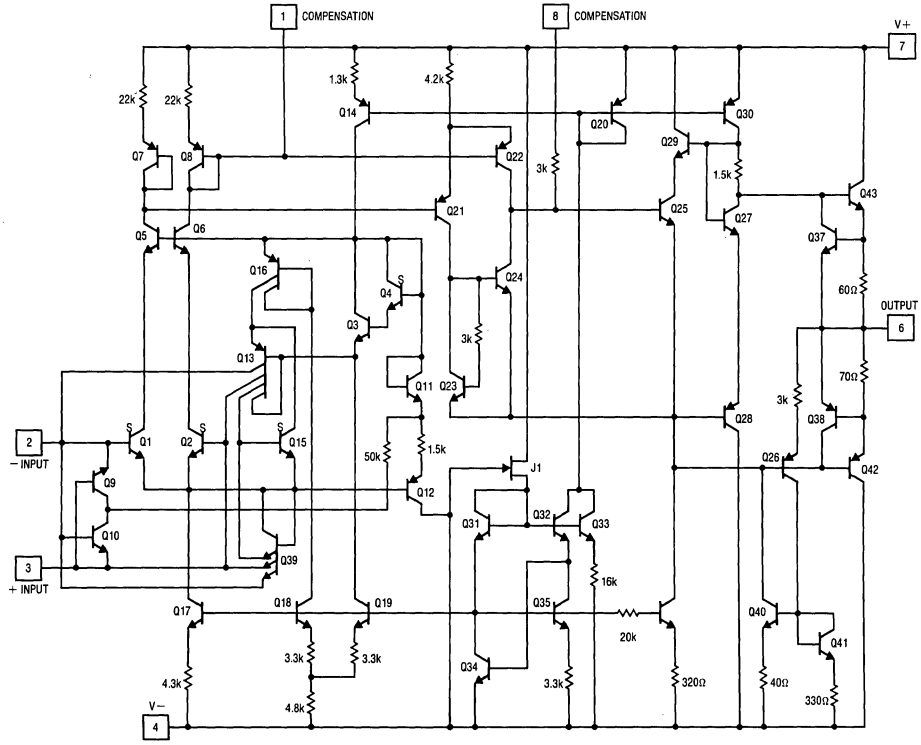
Ammeter With Six Decade Range



Q1, Q2, Q3, Q4, RCA CA3146 TRANSISTOR ARRAY.
CALIBRATION: ADJUST R1 FOR FULL SCALE DEFLECTION WITH 1μA INPUT CURRENT.

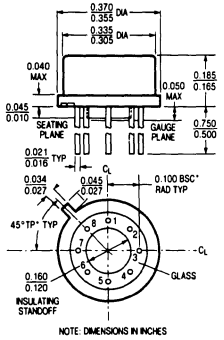
Ammeter measures currents from 100pA to 100μA without the use of expensive high value resistors. Accuracy at 100μA is limited by the offset voltage between Q1 and Q2 and, at 100pA, by the inverting bias current of the LT1008.

SCHEMATIC DIAGRAM



PACKAGE DESCRIPTION

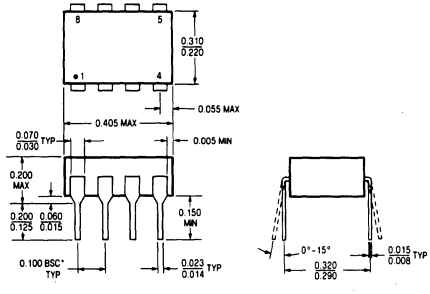
H Package
Metal Can



NOTE: DIMENSIONS IN INCHES

$T_j$max	Θ_{ja}	Θ_{jc}
150°C	150°C/W	45°C/W

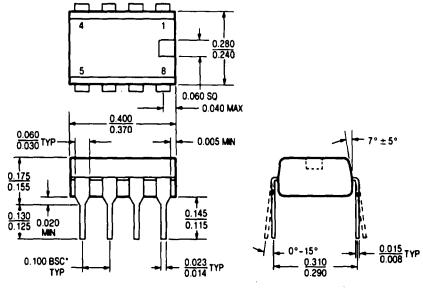
J8 Package
8 Lead Hermetic Dip



NOTE: DIMENSIONS IN INCHES UNLESS OTHERWISE NOTED.
*LEADS WITHIN 0.007 OF TRUE POSITION (TP) AT GAUGE PLANE

$T_j$max	Θ_{ja}
150°C	100°C/W

N8 Package
8 Lead Plastic



NOTE: DIMENSIONS IN INCHES UNLESS OTHERWISE NOTED.
*LEADS WITHIN 0.007 OF TRUE POSITION (TP) AT GAUGE PLANE.

$T_j$max	Θ_{ja}
100°C	130°C/W

Fast ±150mA Power Buffer

FEATURES

- 20MHz Bandwidth
- 75V/μs Slew Rate
- Drives ±10V into 75Ω
- 5mA Quiescent Current
- Drives Capacitive Loads >1μF
- Current and Thermal Limit
- Operates from Single Supply ≥4.5V

APPLICATIONS

- Boost Op Amp Output
- Isolate Capacitive Loads
- Drive Long Cables
- Video Amplifiers
- Power Small Motors
- Operate Proportional Actuators
- Operational Power Supply

DESCRIPTION

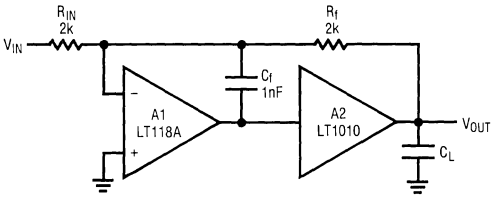
The LT1010 is a fast, unity-gain buffer that can increase the output capability of existing IC op amps by more than an order of magnitude. This easy-to-use part makes fast amplifiers less sensitive to capacitive loading, reduces thermal feedback in precision dc amplifiers and is recommended for a wide range of fast and slow applications.

Designed to be incorporated within the feedback loop, the buffer can isolate almost any reactive load. Internal operating currents are essentially unaffected by supply or output voltage, accounting for the 4.5V to 40V supply voltage range with unchanged specifications. Single-supply operation is also practical.

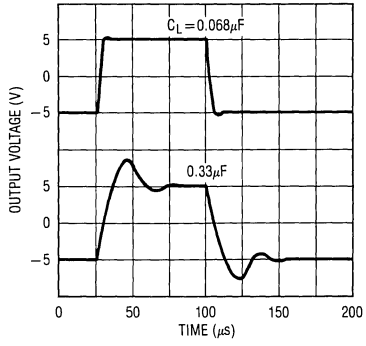
This monolithic IC is supplied in three standard power packages: the solid kovar base TO-5 (TO-39), the steel TO-3 and the plastic TO-220. These low thermal resistance packages are an aid in reducing operating junction temperatures. With the TO-3 and TO-220 packages, an option is available to raise quiescent current and improve speed.

In the TO-39 package, the LT1010 can sometimes replace the hybrid LH0002. With the exception of speed it exceeds key specifications and fault protection is vastly better. Further, the lower thermal resistance package and higher maximum operating temperature of the new monolithic circuit allow more usable output.

Isolating Capacitive Loads



Pulse Response



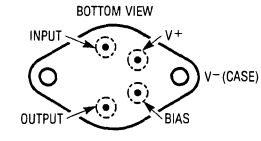
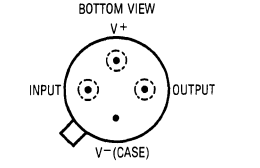
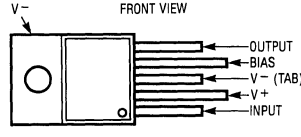
ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage ..... ±22V
Continuous Output Current ..... ±150mA
Continuous Power Dissipation (Note 1)
LT1010MK 5.0W
LT1010CK 4.0W
LT1010CT 4.0W
LT1010MH 3.1W
LT1010CH 2.5W
Input Current (Note 2) ..... ±40mA
Operating Junction Temperature
LT1010M ..... −55°C to 150°C
LT1010C ..... 0°C to 125°C
Storage Temperature ..... −65°C to 150°C
Lead Temperature (Soldering, 10 sec.) ..... 300°C

PRECONDITIONING

100% Thermal Limit Burn In

PACKAGE/ORDER INFORMATION

	ORDER PART NUMBER
 STEEL TO-3 PACKAGE	LT1010MK LT1010CK
 KOVAR BASE TO-39 PACKAGE	LT1010MH LT1010CH
 PLASTIC TO-220 PACKAGE	LT1010CT

ELECTRICAL CHARACTERISTICS (See Note 3. Typical values in curves)

SYMBOL	PARAMETER	CONDITIONS (NOTE 3)		LT1010M MIN	LT1010M MAX	LT1010C MIN	LT1010C MAX	UNITS
V_{OS}	Output Offset Voltage	Note 3		20	110	0	150	mV
			•	−10	220	−20	220	mV
		$V_S = \pm 15V$, $V_{IN} = 0$		40	90	20	100	mV
I_B	Input Bias Current	$I_{OUT} = 0$		0	150	0	250	μA
		$I_{OUT} \leq 150mA$		0	250	0	500	μA
			•	0	300	0	800	μA
A_V	Large Signal Voltage Gain		•	0.995	1.00	0.995	1.00	V/V
R_{OUT}	Output Resistance	$I_{OUT} = \pm 1mA$		6	9	5	10	Ω
		$I_{OUT} = \pm 150mA$		6	9	5	10	Ω
			•		12		12	Ω
	Slew Rate	$V_S = \pm 15V$, $V_{IN} = \pm 10V$						
		$V_{OUT} = \pm 8V$, $R_L = 100\Omega$		75		75		V/μs
V_{SOS}^+	Positive Saturation Offset	Note 4, $I_{OUT} = 0$			1.0		1.0	V
			•		1.1		1.1	V
V_{SOS}^-	Negative Saturation Offset	Note 4, $I_{OUT} = 0$			0.2		0.2	V
			•		0.3		0.3	V
R_{SAT}	Saturation Resistance	Note 4, $I_{OUT} = \pm 150mA$			18		22	Ω
			•		24		28	Ω
V_{BIAS}	Bias Terminal Voltage	Note 5, $R_{BIAS} = 20\Omega$		750	810	700	840	mV
			•	560	925	560	880	mV
I_S	Supply Current	$I_{OUT} = 0$, $I_{BIAS} = 0$			8		9	mA
			•		9		10	mA

Note 1: For case temperatures above 25°C, dissipation must be derated based on a thermal resistance of 25°C/W with the K and T packages or 40°C/W with the H package. See applications information.

Note 2: In current limit or thermal limit, input current increases sharply with input-output differentials greater than 8V; so input current must be limited. Input current also rises rapidly for input voltages 8V above V^+ or 0.5V below V^-.

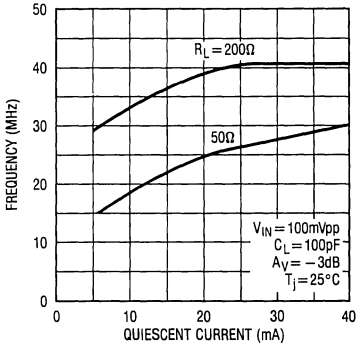
Note 3: Specifications apply for $4.5V \leq V_S \leq 40V$, $V^- + 0.5V \leq V_{IN} \leq V^+ - 1.5V$ and $I_{OUT} = 0$, unless otherwise stated. Temperature range is $-55°C \leq T_j \leq 150°C$, $T_C \leq 125°C$, for the LT1010M and $0°C \leq T_j \leq 125°C$, $T_C \leq 100°C$, for the LT1010C. The ● denotes the specifications that apply over the full temperature range.

Note 4: The output saturation characteristics are measured with 100mV output clipping. See applications information for determining available output swing and input drive requirements for a given load.

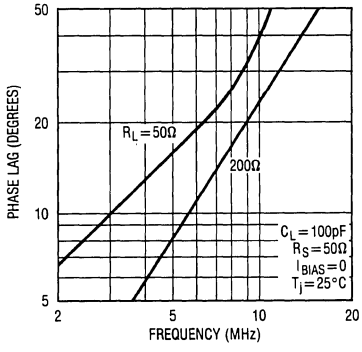
Note 5: With the TO-3 and TO-220 packages, output stage quiescent current can be increased by connecting a resistor between the bias pin and V^+. The increase is equal to the bias terminal voltage divided by this resistance.

TYPICAL PERFORMANCE CHARACTERISTICS

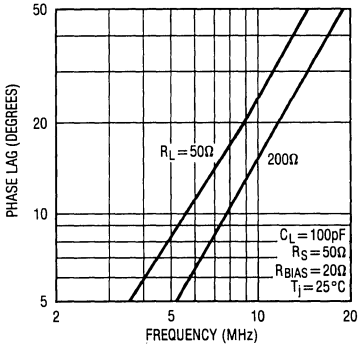
Bandwidth



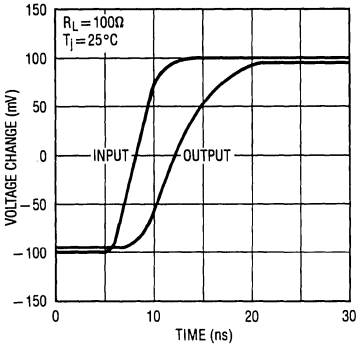
Phase Lag



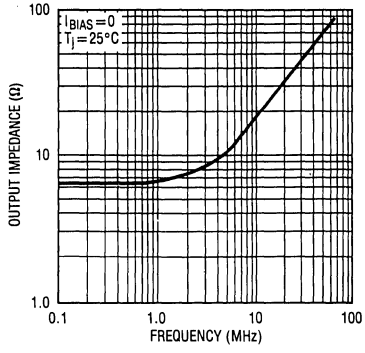
Phase Lag



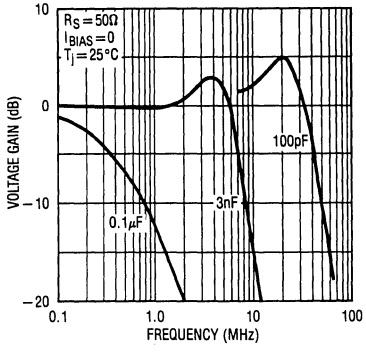
Small-Step Response



Output Impedance

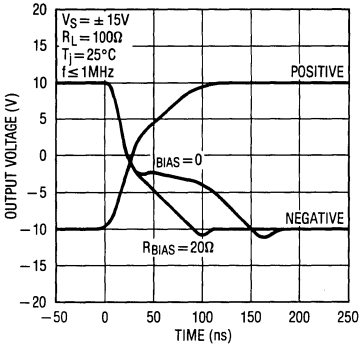


Capacitive Loading

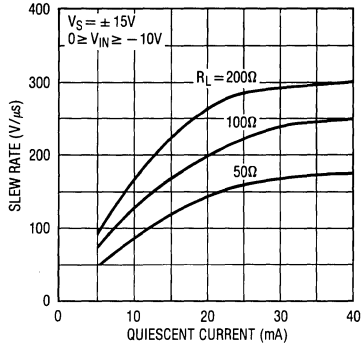


TYPICAL PERFORMANCE CHARACTERISTICS

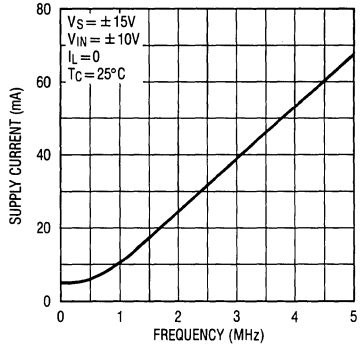
Slew Response



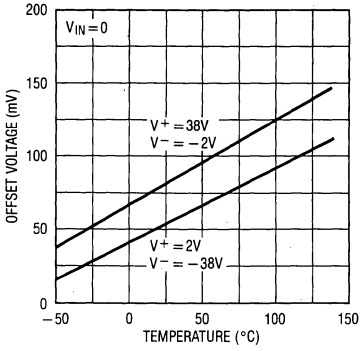
Negative Slew Rate



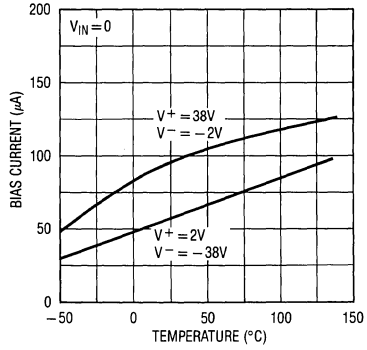
Supply Current



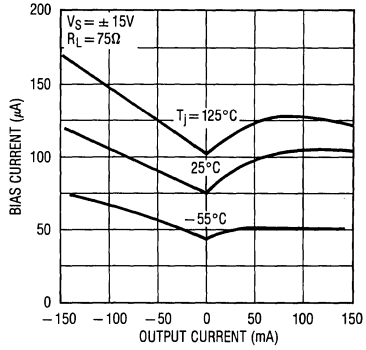
Output Offset Voltage



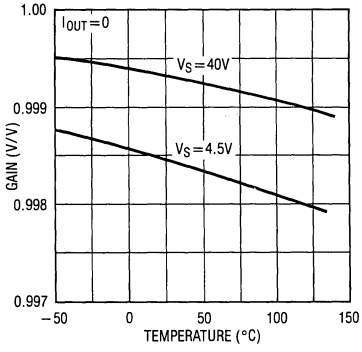
Input Bias Current



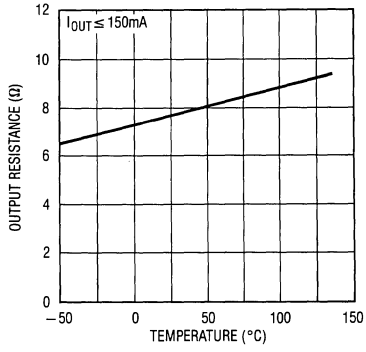
Input Bias Current



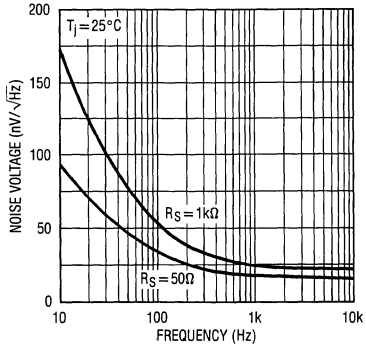
Voltage Gain



Output Resistance

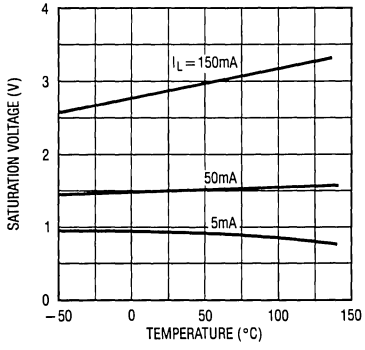


Output Noise Voltage

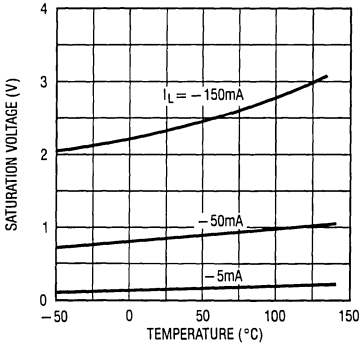


TYPICAL PERFORMANCE CHARACTERISTICS

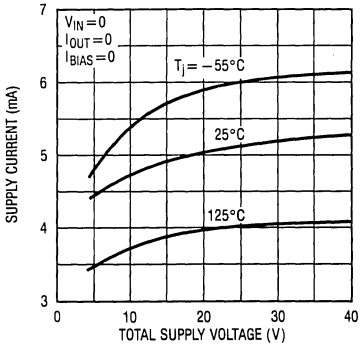
Positive Saturation Voltage



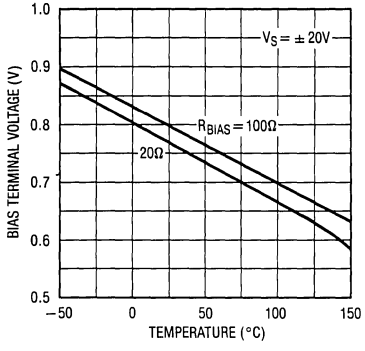
Negative Saturation Voltage



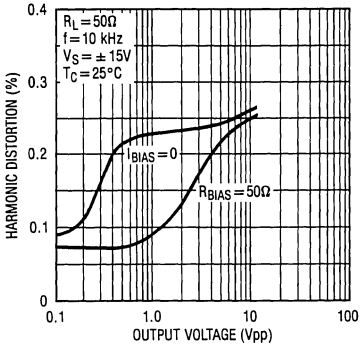
Supply Current



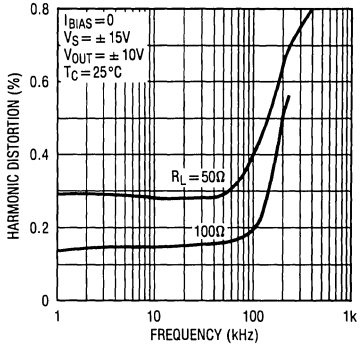
Bias Terminal Voltage



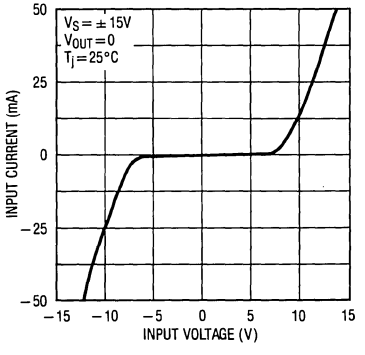
Total Harmonic Distortion



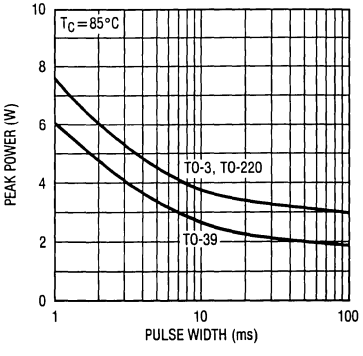
Total Harmonic Distortion



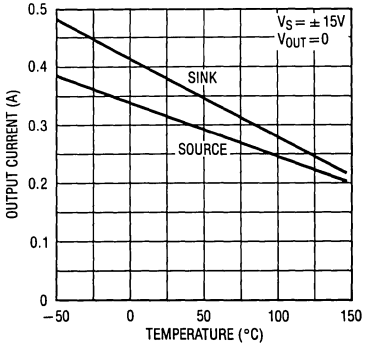
Shorted Input Characteristics



Peak Power Capability



Peak Output Current



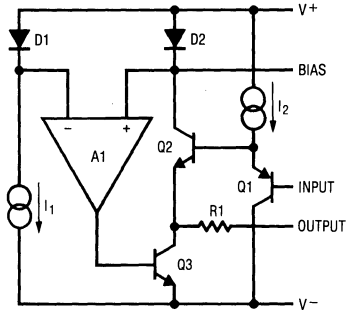
APPLICATIONS INFORMATION

General

These notes briefly describe the LT1010 and how it is used; a detailed explanation is given elsewhere.* Emphasis here will be on practical suggestions that have resulted from working extensively with the part over a wide range of conditions. A number of applications are also outlined that demonstrate the usefulness of the buffer beyond that of driving a heavy load.

Design Concept

The schematic below describes the basic elements of the buffer design. The op amp drives the output sink transistor, Q3, such that the collector current of the output follower, Q2, never drops below the quiescent value (determined by I_1 and the area ratio of D1 and D2). As a result, the high frequency response is essentially that of a simple follower even when Q3 is supplying the load current. The internal feedback loop is isolated from the effects of capacitive loading by a small resistor in the output lead.

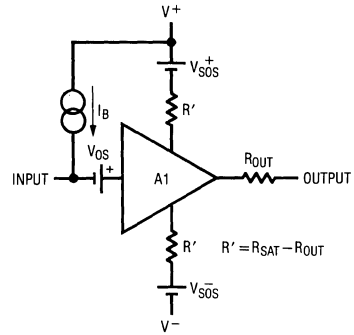


The scheme is not perfect in that the rate of rise of sink current is noticeably less than for source current. This can be mitigated by connecting a resistor between the bias terminal and V+, raising quiescent current. A feature of the final design is that the output resistance is largely independent of the follower quiescent current or the output load current. The output will also swing to the negative rail, which is particularly useful with single-supply operation.

*R. J. Widlar, "Unique IC Buffer Enhances Op Amp Designs; Tames Fast Amplifiers", *Linear Technology Corp. TP-1,* April, 1984.

Equivalent Circuit

Below 1MHz, the LT1010 is quite accurately represented by the equivalent circuit shown here for both small and large signal operation. The internal element, A1, is an idealized buffer with the unloaded gain specified for the LT1010. Otherwise, it has zero offset voltage, bias current and output resistance. Its output also saturates to the internal supply terminals.†



Loaded voltage gain can be determined from the unloaded gain, A_V, the output resistance, R_{OUT}, and the load resistance, R_L, using

$$A_{VL} = \frac{A_V R_L}{R_{OUT} + R_L}.$$

Maximum positive output swing is given by

$$V_{OUT}^+ = \frac{(V^+ - V_{SOS}^+)\, R_L}{R_{SAT} + R_L}.$$

The input swing required for this output is

$$V_{IN}^+ = V_{OUT}^+ \left(1 + \frac{R_{OUT}}{R_L}\right) - V_{OS} + \Delta V_{OS},$$

where ΔV_{OS} is the 100mV clipping specified for the saturation measurements. Negative output swing and input drive requirements are similarly determined.

† See electrical characteristics section for guaranteed limits.

APPLICATIONS INFORMATION

Supply Bypass

The buffer is no more sensitive to supply bypassing than slower op amps, as far as stability is concerned. The 0.1μF disc ceramic capacitors usually recommended for op amps are certainly adequate for low frequency work. As always, keeping the capacitor leads short and using a ground plane is prudent, especially when operating at high frequencies.

The buffer slew rate can be reduced by inadequate supply bypass. With output current changes much above 100mA/μs, using 10μF solid tantalum capacitors on both supplies is good practice, although bypassing from the positive to the negative supply may suffice.

When used in conjunction with an op amp and heavily loaded (resistive or capacitive), the buffer can couple into supply leads common to the op amp causing stability problems with the overall loop and extended settling time. Adequate bypassing can usually be provided by 10μF solid tantalum capacitors. Alternately, smaller capacitors could be used with decoupling resistors. Sometimes the op amp has much better high frequency rejection on one supply, so bypass requirements are less on this supply.

Power Dissipation

In many applications, the LT1010 will require heat sinking. Thermal resistance, junction to still air is 150°C/W for the TO-39 package, 100°C/W for the TO-220 package and 60°C/W for the TO-3 package. Circulating air, a heat sink or mounting the package to a printed circuit board will reduce thermal resistance.

In dc circuits, buffer dissipation is easily computed. In ac circuits, signal waveshape and the nature of the load determine dissipation. Peak dissipation can be several times average with reactive loads. It is particularly important to determine dissipation when driving large load capacitance.

With ac loading, power is divided between the two output transistors. This reduces the effective thermal resistance, junction to case, to 30°C/W for the TO-39 package and 15°C/W for the TO-3 and TO-220 packages, as long as the peak rating of neither output transistor is exceeded. The typical curves indicate the peak dissipation capabilities of one output transistor.

Overload Protection

The LT1010 has both instantaneous current limit and thermal overload protection. Foldback current limiting has not been used, enabling the buffer to drive complex loads without limiting. Because of this, it is capable of power dissipation in excess of its continuous ratings.

Normally, thermal overload protection will limit dissipation and prevent damage. However, with more than 30V across the conducting output transistor, thermal limiting is not quick enough to insure protection in current limit. The thermal protection is effective with 40V across the conducting output transistor as long as the load current is otherwise limited to 150mA.

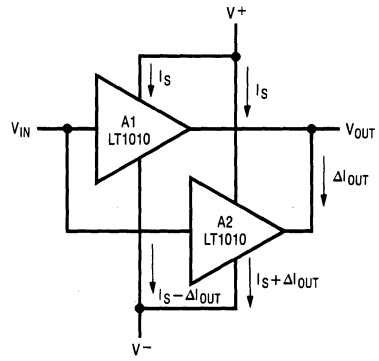
Drive Impedance

When driving capacitive loads, the LT1010 likes to be driven from a low source impedance at high frequencies. Certain low power op amps (e.g., the LM10) are marginal in this respect. Some care may be required to avoid oscillations, especially at low temperatures.

Bypassing the buffer input with more than 200pF will solve the problem. Raising the operating current also works, but this cannot be done with the TO-39 package.

APPLICATIONS INFORMATION

Parallel Operation



Parallel operation provides reduced output impedance, more drive capability and increased frequency response under load. Any number of buffers can be directly paralleled as long as the increased dissipation in individual units caused by mismatches of output resistance and offset voltage is taken into account.

When the inputs and outputs of two buffers are connected together, a current, ΔI_{OUT}, flows between the outputs:

$$\Delta I_{OUT} = \frac{V_{OS1} - V_{OS2}}{R_{OUT1} + R_{OUT2}},$$

where V_{OS} and R_{OUT} are the offset voltage and output resistance of the respective buffers.

Normally, the negative supply current of one unit will increase and the other decrease, with the positive supply current staying the same. The worst-case ($V_{IN} \rightarrow V^+$) increase in standby dissipation can be assumed to be $\Delta I_{OUT}\ V_T$, where V_T is the total supply voltage.

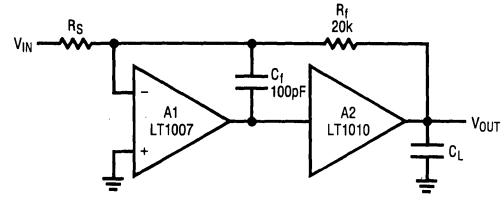
Offset voltage is specified worst-case over a range of supply voltages, input voltage and temperature. It would be unrealistic to use these worst-case numbers above because paralleled units are operating under identical conditions. The offset voltage specified for $V_S = \pm 15V$, $V_{IN} = 0$ and $T_A = 25°C$ will suffice for a worst-case condition.

Output load current will be divided based on the output resistance of the individual buffers. Therefore, the available output current will not quite be doubled unless output resistances are matched. As for offset voltage above, the 25°C limits should be used for worst-case calculations.

Parallel operation is not thermally unstable. Should one unit get hotter than its mates, its share of the output and its standby dissipation will decrease.

As a practical matter, parallel connection needs only some increased attention to heat sinking. In some applications, a few ohms equalization resistance in each output may be wise. Only the most demanding applications should require matching, and then just of output resistance at 25°C.

Isolating Capacitive Loads



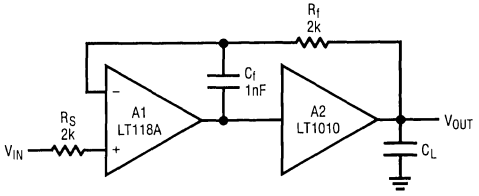
The inverting amplifier above shows the recommended method of isolating capacitive loads. Non-inverting amplifiers are handled similarly.

At lower frequencies, the buffer is within the feedback loop so that its offset voltage and gain errors are negligible. At higher frequencies, feedback is through C_f, so that phase shift from the load capacitance acting against the buffer output resistance does not cause loop instability.

Stability depends upon the R_fC_f time constant, or the closed loop bandwidth. With an 80kHz bandwidth, ringing is negligible for $C_L = 0.05\mu F$ and damps rapidly for $C_L = 0.3\mu F$.

APPLICATIONS INFORMATION

Small signal bandwidth is reduced by C_f, but considerable isolation can be obtained without reducing it below the power bandwidth. Often, a bandwidth reduction is desirable to filter high frequency noise or unwanted signals.

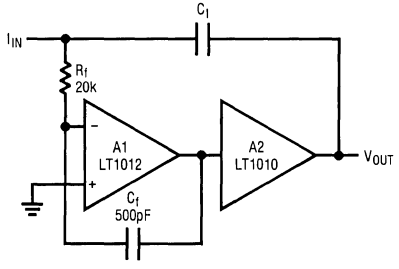


The follower configuration is unique in that capacitive load isolation is obtained without a reduction in small signal bandwidth, although the output impedance of the buffer comes into play at high frequencies. The precision unity-gain buffer above has a 10MHz bandwidth without capacitive loading, yet it is stable for all load capacitance to over 0.3μF, again determined by R_fC_f.

This is a good example of how fast op amps can be made quite easy to use by employing an output buffer.

Integrator

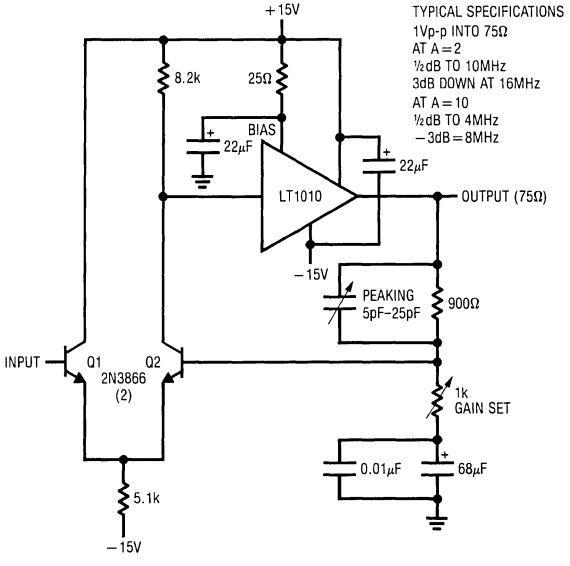
A low pass amplifier can be formed just by using large C_f in the inverter described earlier, as long as the increasing closed loop output impedance above the cutoff frequency is not a problem and the op amp is capable of supplying the required current at the summing junction.



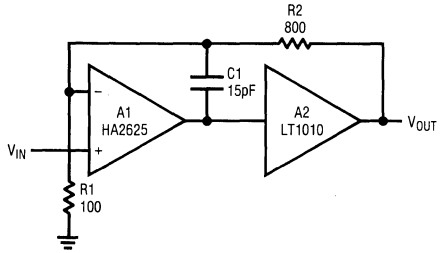
If the integrating capacitor must be driven from the buffer output, the circuit above can be used to provide capacitive load isolation. As before, the stability with large capacitive loads is determined by R_fC_f.

Wideband Amplifiers

This simple circuit provides an adjustable gain video amplifier which will drive 1V p-p into 75Ω. The differential pair provides gain, with the LT1010 serving as an output stage. Feedback is arranged in the conventional manner, although the 68μf – 0.01 combination limits DC gain to unity for all gain settings. For applications sensitive to NTSC requirements, dropping the 25Ω output stage bias value will aid performance.



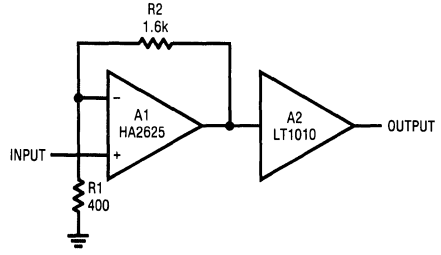
APPLICATIONS INFORMATION



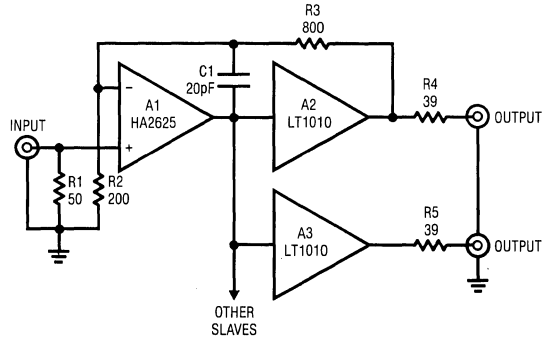
This shows the buffer being used with a wideband amplifier that is not unity-gain stable. In this case, C1 cannot be used to isolate large capacitive loads. Instead, it has an optimum value for a limited range of load capacitances.

The buffer can cause stability problems in circuits like this. With the TO-3 and TO-220 packages, behavior can be improved by raising the quiescent current with a 20Ω resistor from the bias terminal to V^+. Alternately, devices in the TO-39 package can be operated in parallel.

It is possible to improve capacitive load stability by operating the buffer class-A at high frequencies. This is done by using quiescent current boost and bypassing the bias terminal to V^- with more than 0.02μF.



Putting the buffer outside the feedback loop as shown here will give capacitive load isolation, with large output capacitors only reducing bandwidth. Buffer offset, referred to the op amp input, is divided by the gain. If the load resistance is known, gain error is determined by the output resistance tolerance. Distortion is low.



The 50Ω video line splitter shown here puts feedback on one buffer, with the others slaved. Offset and gain accuracy of slaves depend on their matching with master.

When driving long cables, including a resistor in series with the output should be considered. Although it reduces gain, it does isolate the feedback amplifier from the effects of unterminated lines which present a resonant load.

When working with wideband amplifiers, special attention should *always* be paid to supply bypassing, stray capacitance and keeping leads short. Direct grounding of test probes, rather than the usual ground lead, is absolutely necessary for reasonable results.

The LT1010 has slew limitations that are not obvious from standard specifications. Negative slew is subject to glitching, but this can be minimized with quiescent current boost. The appearance is always worse with fast rise signal generators than in practical applications.

APPLICATIONS INFORMATION

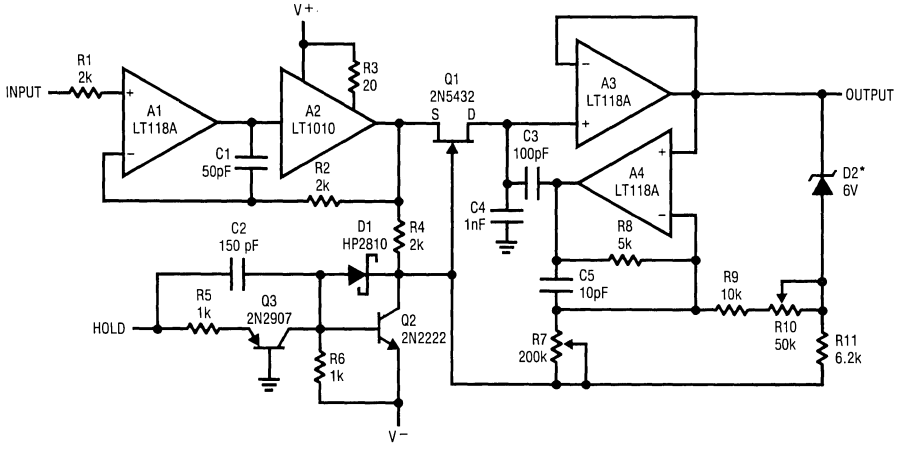
Track and Hold

The 5MHz track and hold shown here has a 400kHz power bandwidth driving ±10V. A buffered input follower drives the hold capacitor, C4, through Q1, a low resistance FET switch. The positive hold command is supplied by TTL logic, with Q3 level shifting to the switch driver, Q2. The output is buffered by A3.

When the gate is driven to V⁻ for HOLD, it pulls charge out of the hold capacitor. A compensating charge is put into the hold capacitor through C3. The step into hold is made independent of the input level with R7 and adjusted to zero with R10.

Since internal dissipation can be quite high when driving fast signals into a capacitive load, using a buffer in a power package is recommended. Raising buffer quiescent current to 40mA with R3 improves frequency response.

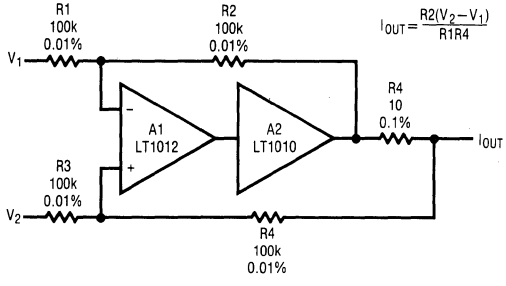
This circuit is equally useful as a fast acquisition sample and hold. An LF156 might be used for A3 to reduce drift in hold because its lower slew rate is not usually a problem in this application.



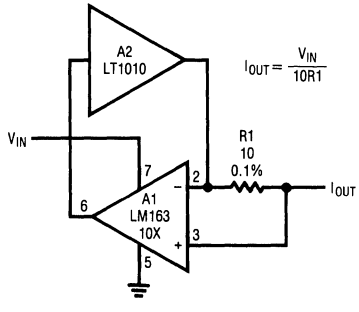
*2N2369 EMITTER BASE JUNCTION

APPLICATIONS INFORMATION

Current Sources



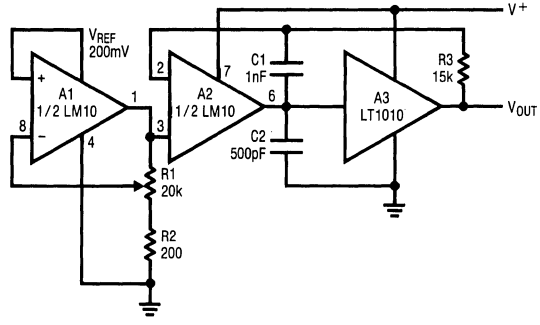
A standard op amp voltage to current converter with a buffer to increase output current is shown here. As usual, excellent matching of the feedback resistors is required to get high output resistance. Output is bi-directional.



This circuit uses an instrumentation amplifier to eliminate the matched resistors. The input is not high impedance and must be driven from a low impedance source like an op amp. Reversal of output sense can be obtained by grounding pin 7 of the LM163 and driving pin 5.

Output resistances of several megohms can be obtained with both circuits. This is impressive considering the ±150mA output capability. High frequency output characteristics will depend on the bandwidth and slew rate of the amplifiers. Both these circuits have an equivalent output capacitance of about 30nF.

Voltage Regulator

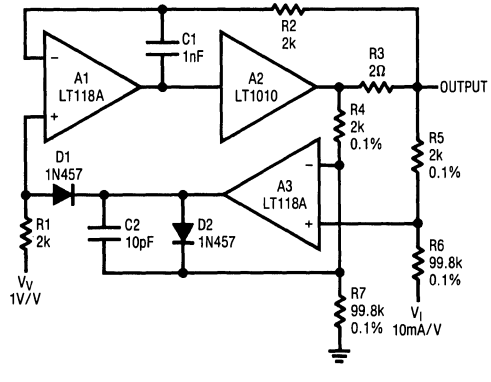


Although it operates from a single supply, this circuit will regulate voltage down to 200mV. It will also source or sink current.

The ability of the circuit to handle capacitive loads is determined by R3 and C1. The values given are optimized for up to 1μF output capacitance, as might be required for an IC test supply.

The purpose of C1 is to lower the drive impedance to the buffer as discussed earlier. It is, incidentally, important to connect pin 4 of the LM10 and the bottom of R2 to a common ground point to avoid ground loop problems.

Voltage/Current Regulator



APPLICATIONS INFORMATION

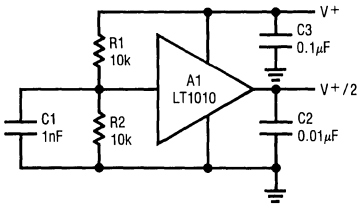
This circuit regulates the output voltage at V_V until the load current reaches a value programmed by V_I. For heavier loads, it is a precision current regulator.

With output currents below the current limit, the current regulator is disconnected from the loop by D1, with D2 keeping its output out of saturation. This output clamp enables the current regulator to get control of the output current from the buffer current limit within a microsecond for an instantaneous short.

In the voltage regulation mode, A1 and A2 act as a fast voltage follower using the capacitive load isolation technique described earlier. Load transient recovery as well as capacitive load stability are determined by C1. Recovery from short circuit is clean.

Bi-directional current limit can be obtained by adding another op amp connected as a complement to A3.

Supply Splitter



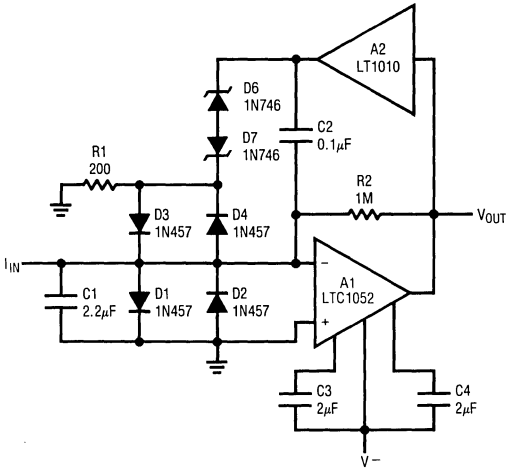
Dual supply op amps and comparators can be operated from a single supply by creating an artificial ground at half the supply voltage. The supply splitter shown here can source or sink 150mA.

The output capacitor, C2, can be made as large as necessary to absorb current transients. An input capacitor is also used on the buffer to avoid high frequency instability that can be caused by high source impedance.

Overload Clamping

The input of a summing amplifier is at virtual ground as long as it is in the active region. With overloads, this is no longer true, unless the feedback is kept active.

This schematic shows a chopper stabilized current to voltage converter. It is capable of 10pA resolution, yet is able to keep the summing node under control with overload currents to ±150mA.



During normal operation, D3 and D4 are not conducting; and R1 absorbs any leakage current from the zener clamps, D6 and D7. In overload, current is supplied to the summing node through the zener clamps, rather than the scaling resistor, R2.

DEFINITION OF TERMS

Output Offset Voltage: The output voltage measured with reference to the input.

Input Bias Current: The current out of the input terminal.

Large Signal Voltage Gain: The ratio of the output voltage change to the input voltage change over the specified input voltage range.*

Output Resistance: The ratio of the change in output voltage to the change in load current producing it.*

Output Saturation Voltage: The voltage between the output and the supply rail at the limit of the output swing toward that rail.

Saturation Offset Voltage: The output saturation voltage with no load.

Saturation Resistance: The ratio of the change in output saturation voltage to the change in current producing it, going from no load to full load.*

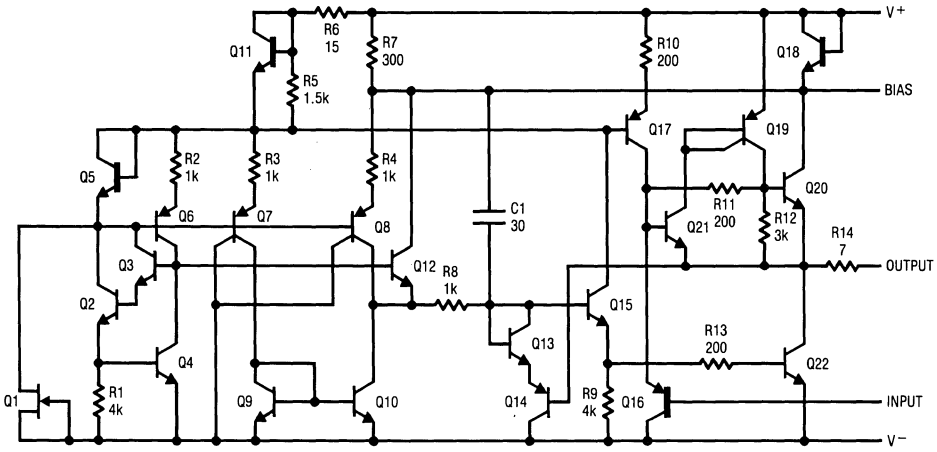
Slew Rate: The average time rate of change of output voltage over the specified output range with an input step between the specified limits.

Bias Terminal Voltage: The voltage between the bias terminal and V^+.

Supply Current: The current at either supply terminal with no output loading.

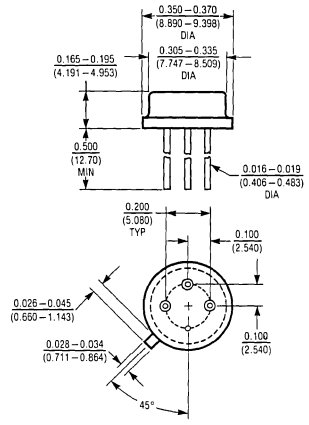
*Pulse measurements (~1ms) as required to minimize thermal effects.

SCHEMATIC DIAGRAM (excluding protection circuits)



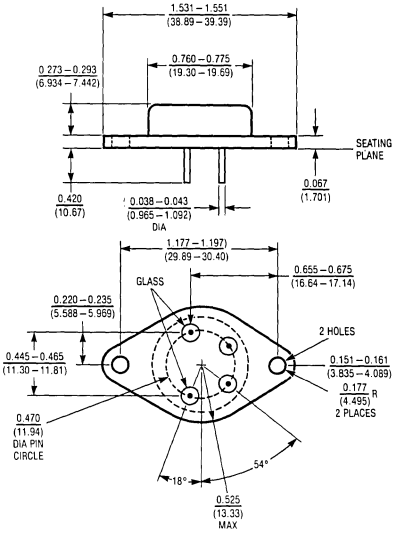
PACKAGE DESCRIPTION

TO-39 Type Metal Can
H Package



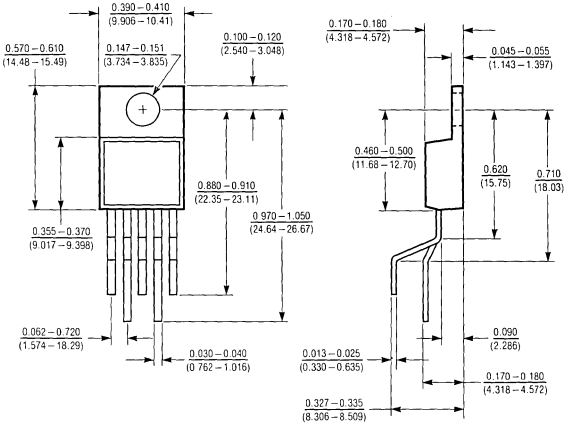
DEVICE	$T_{J(MAX)}$	Θ_{JC}
LT1010M	150°C	40°C/W
LT1010C	125°C	40°C/W

TO-3 Type Metal Can (Steel)
K Package



DEVICE	$T_{J(MAX)}$	Θ_{JC}
LT1010M	150°C	25°C/W
LT1010C	125°C	25°C/W

TO-220 Type Plastic
T Package



DEVICE	$T_{J(MAX)}$	Θ_{JC}
LT1010C	125°C	25°C/W

Picoamp Input Current, Microvolt Offset, Low Noise Op Amp

FEATURES

- Internally Compensated
- *Guaranteed* Offset Voltage 35μV max.
- *Guaranteed* Bias Current
  - 25°C 100pA max.
  - −55°C to 125°C 600pA max.
- *Guaranteed* Drift 1.5μV/°C max.
- 0.1Hz to 10Hz 0.5μVp-p
- *Guaranteed* Low Supply Current 600μA max.
- *Guaranteed* CMRR 114 dB min.
- *Guaranteed* PSRR 114 db min.
- *Guaranteed* Voltage Gain with 5mA load current

APPLICATIONS

- Precision instrumentation
- Charge integrators
- Wide dynamic range logarithmic amplifiers
- Light meters
- Low frequency active filters
- Standard cell buffers
- Thermocouple amplifiers

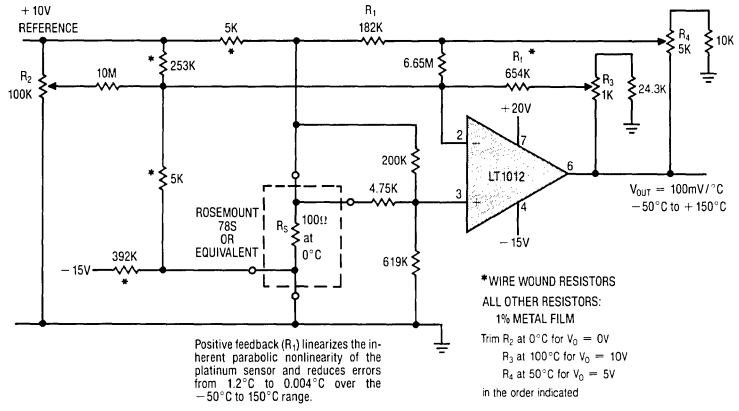
DESCRIPTION

The LT1012 is an internally compensated universal precision operational amplifier which can be used in practically all precision applications. The LT1012 combines picoampere bias currents (which are maintained over the full −55°C to 125°C temperature range), microvolt offset voltage (and low drift with time and temperature), low voltage and current noise, and low power dissipation. Extremely high common-mode and power supply rejection ratios, practically unmeasurable warm-up drift, and the ability to deliver 5mA load current with a voltage gain of a million round out the LT1012's superb precision specifications.

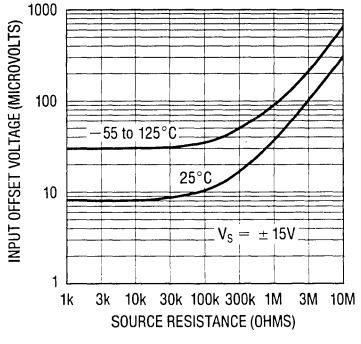
The all around excellence of the LT1012 eliminates the necessity of the time consuming error analysis procedure of precision system design in many applications; the LT1012 can be stocked as the universal internally compensated precision op amp.

For an externally compensated version with additional flexibility in shaping the frequency response of the amplifier, but otherwise similar performance, see the LT1008.

Kelvin-Sensed Platinum Temperature Sensor Amplifier



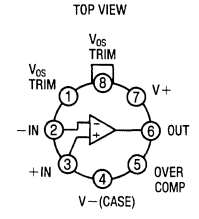
Offset Voltage vs Source Resistance (Balanced or Unbalanced)



ABSOLUTE MAXIMUM RATING

Supply Voltage ..... ±20V
Differential Input Current (Note 1) ..... ±10mA
Input Voltage ..... ±20V
Output Short Circuit Duration ..... Indefinite
Operating Temperature Range
LT1012M ..... −55°C to 125°C
LT1012C ..... 0°C to 70°C
Storage Temperature Range
All Devices ..... −65°C to 150°C
Lead Temperature (Soldering, 10 sec.) ..... 300°C

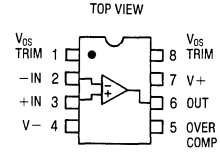
PACKAGE/ORDER INFORMATION



METAL CAN H PACKAGE

ORDER PART NO.

LT1012MH
LT1012CH



PLASTIC DIP N8 PACKAGE

LT1012CN8

ELECTRICAL CHARACTERISTICS $V_S = \pm 15V$, $V_{CM} = 0V$, $T_A = 25°C$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	LT1012M MIN	LT1012M TYP	LT1012M MAX	LT1012C MIN	LT1012C TYP	LT1012C MAX	UNITS
V_{OS}	Input Offset Voltage			8	35		10	50	μV
		Note 2		20	90		25	120	μV
	Long Term Input Offset Voltage Stability			0.3			0.3		μV/month
I_{OS}	Input Offset Current			15	100		20	150	pA
		Note 2		25	150		30	200	pA
I_B	Input Bias Current			±25	±100		±30	±150	pA
		Note 2		±35	±150		±40	±200	pA
e_n	Input Noise Voltage	0.1Hz to 10Hz		0.5			0.5		μVp-p
e_n	Input Noise Voltage Density	$f_0 = 10Hz$ (Note 3)		17	30		17	30	$nV/\sqrt{Hz}$
		$f_0 = 1000Hz$ (Note 4)		14	22		14	22	$nV/\sqrt{Hz}$
i_n	Input Noise Current Density	$f_0 = 10Hz$		20			20		$fA/\sqrt{Hz}$
A_{VOL}	Large Signal Voltage Gain	$V_{OUT} = \pm 12V$, $R_L \geq 10k\Omega$	300	2000		200	2000		V/mV
		$V_{OUT} = \pm 10V$, $R_L \geq 2k\Omega$	200	1000		120	1000		V/mV
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm 13.5V$	114	132		110	132		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 2V$ to $\pm 20V$	114	132		110	132		dB
	Input Voltage Range		±13.5	±14.0		±13.5	±14.0		V
V_{OUT}	Output Voltage Swing	$R_L = 10k\Omega$	±13	±14		±13	±14		V
	Slew Rate		0.1	0.2		0.1	0.2		V/μsec
I_S	Supply Current	Note 2		380	600		380	600	μA

ELECTRICAL CHARACTERISTICS

$V_S = \pm 15V$, $V_{CM} = 0V$, $0°C \leq T_A \leq 70°C$ for the LT1012C and $-55°C \leq T_A \leq 125°C$ for the LT1012M, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		LT1012M MIN	LT1012M TYP	LT1012M MAX	LT1012C MIN	LT1012C TYP	LT1012C MAX	UNITS
V_{OS}	Input Offset Voltage		●		30	180		20	120	μV
		Note 2	●		40	250		30	200	μV
	Average Temperature Coefficient of Input Offset Voltage		●		0.2	1.5		0.2	1.5	μV/°C
I_{OS}	Input Offset Current		●		30	250		20	230	pA
		Note 2	●		70	350		40	300	pA
	Average Temperature Coefficient of Input Offset Current		●		0.3	2.5		0.3	2.5	pA/°C
I_B	Input Bias Current		●		±80	±600		±35	±230	pA
		Note 2	●		±150	±800		±50	±300	pA
	Average Temperature Coefficient of Input Bias Current		●		0.6	6.0		0.3	2.5	pA/°C
A_{VOL}	Large Signal Voltage Gain	$V_{OUT} = \pm 12V$, $R_L \geq 10k\Omega$	●	150	1000		150	1500		V/mV
		$V_{OUT} = \pm 10V$, $R_L \geq 2k\Omega$	●	100	600		100	800		V/mV
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm 13.5V$	●	108	128		108	130		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 2.5V$ to $\pm 20V$	●	108	126		108	128		dB
	Input Voltage Range		●	±13.5			±13.5			V
V_{OUT}	Output Voltage Swing	$R_L = 10k\Omega$	●	±13	±14		±13	±14		V
I_S	Supply Current		●		400	800		400	800	μA

The ● denotes the specifications which apply over the full operating temperature range.

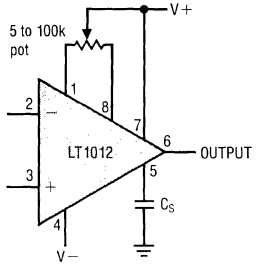
Note 1: Differential input voltages greater than 1V will cause excessive current to flow through the input protection diodes unless limiting resistance is used.

Note 2: These specifications apply for $\pm 2V \leq V_S \leq \pm 20V$ ($\pm 2.5V \leq V_S \leq \pm 20V$ over the temperature range) and $-13.5V \leq V_{CM} \leq 13.5V$ (for $V_S = \pm 15V$).

Note 3: 10Hz noise voltage density is sample tested on every lot. Devices 100% tested at 10Hz are available on request.

Note 4: This parameter is tested on a sample basis only.

Optional Offset Nulling and Over-Compensation Circuits

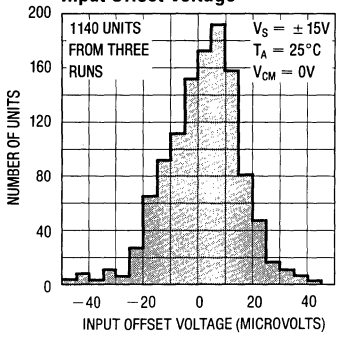


Input offset voltage can be adjusted over a $\pm 800\mu V$ range with a 5k to 100k potentiometer.

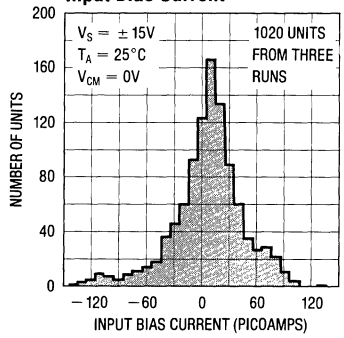
The LT1012 is internally compensated for unity gain stability. The over-compensation capacitor, C_S, can be used to improve capacitive load handling capability, to narrow noise bandwidth, or to stabilize circuits with gain in the feedback loop.

TYPICAL PERFORMANCE CHARACTERISTICS

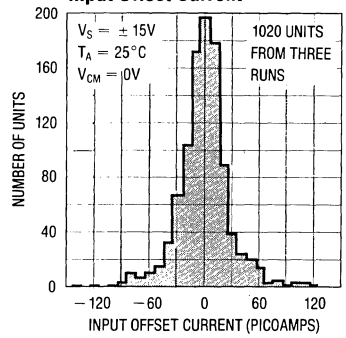
Typical Distribution of Input Offset Voltage



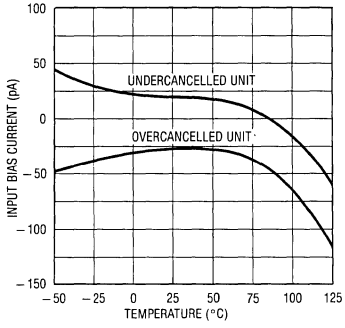
Typical Distribution of Input Bias Current



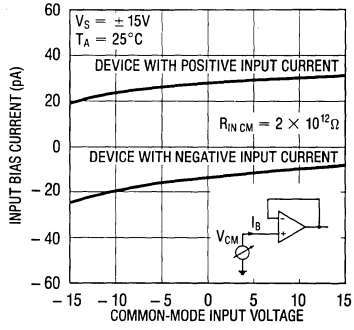
Typical Distribution of Input Offset Current



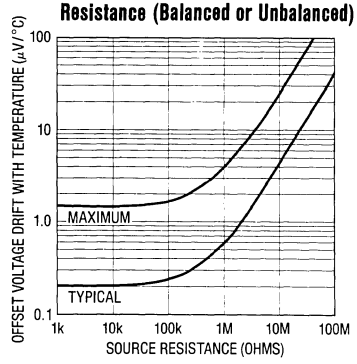
Input Bias Current vs Temperature



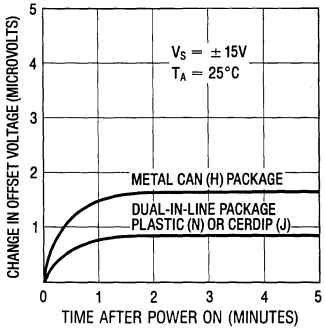
Input Bias Current Over Common Mode Range



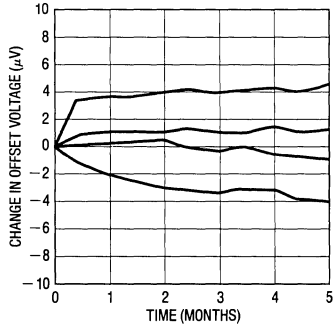
Offset Voltage Drift vs Source Resistance (Balanced or Unbalanced)



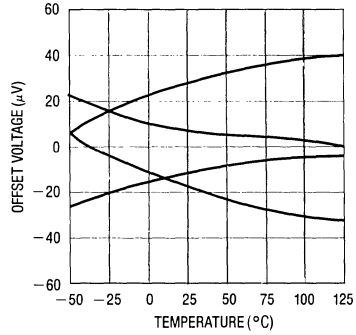
Warm-Up Drift



Long Term Stability of Four Representative Units

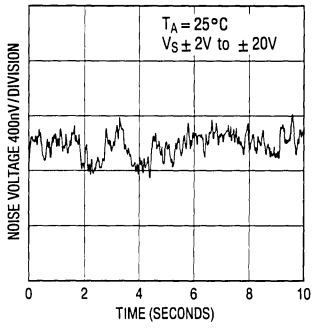


Offset Voltage Drift with Temperature of Four Representative Units

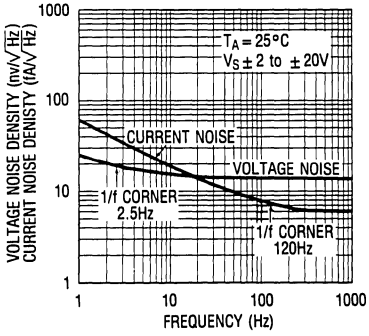


TYPICAL PERFORMANCE CHARACTERISTICS

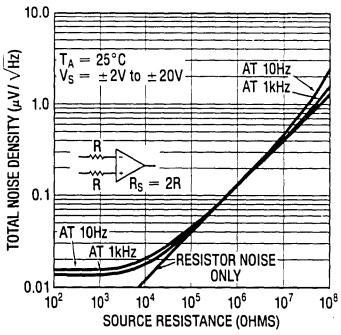
0.1Hz to 10Hz Noise



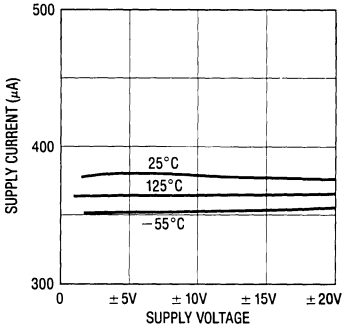
Noise Spectrum



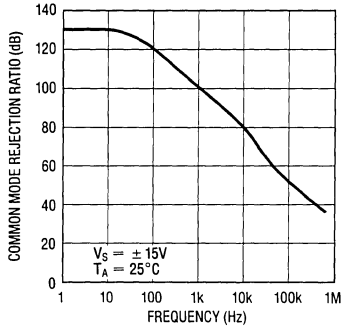
Total Noise vs Source Resistance



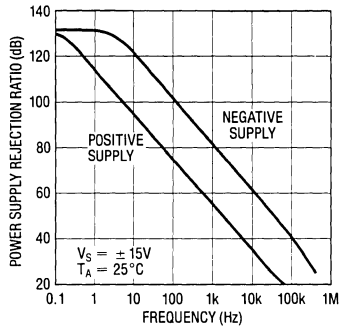
Supply Current vs Supply Voltage



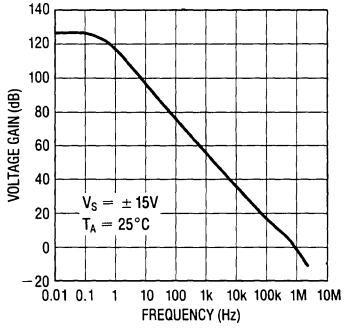
Common Mode Rejection vs Frequency



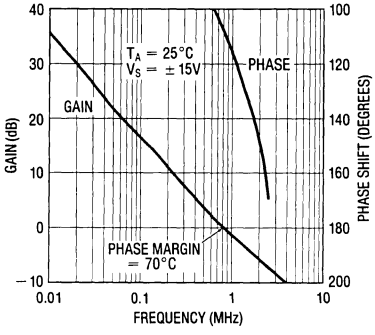
Power Supply Rejection vs Frequency



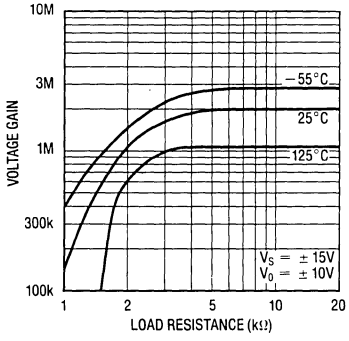
Voltage Gain vs Frequency



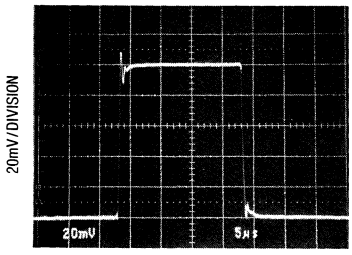
Gain, Phase Shift vs Frequency



Voltage Gain vs Load Resistance

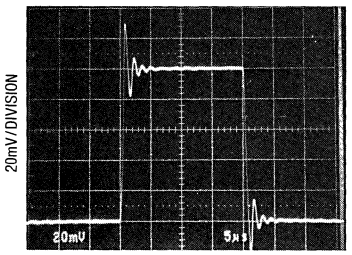


Small Signal Transient Response



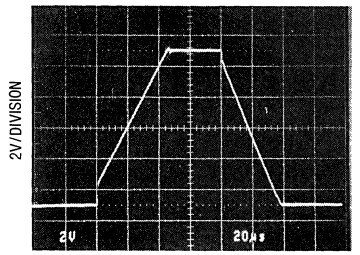
$A_V = +1$, $C_{LOAD} = 100pF$, $5\mu sec/DIV$

Small Signal Transient Response



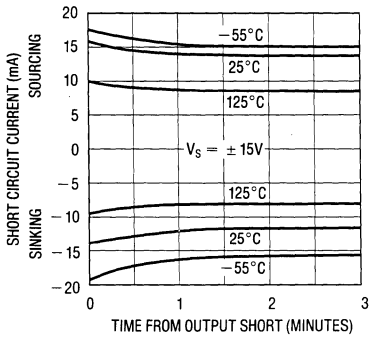
$A_V = +1$, $C_{LOAD} = 1000pF$, $5\mu sec/DIV$

Large Signal Transient Response

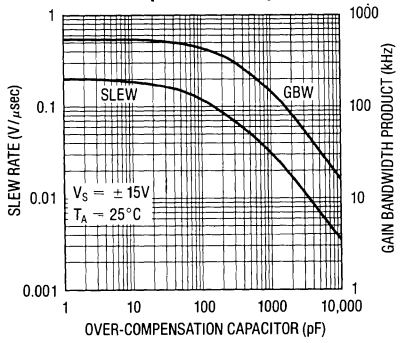


$A_V = +1$, $20\mu sec/DIV$

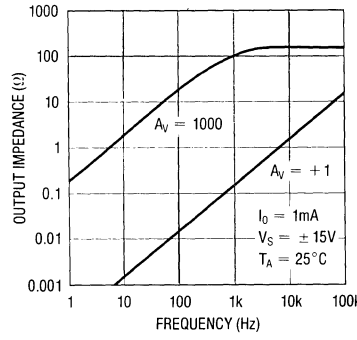
Output Short Circuit Current vs Time



Slew Rate, Gain Bandwidth Product vs Over-Compensation Capacitor



Closed Loop Output Impedance



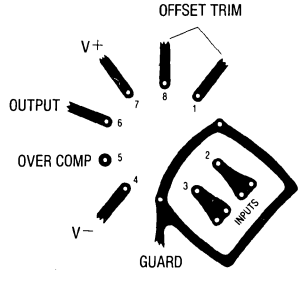
APPLICATIONS INFORMATION

The LT1012 may be inserted directly into OP-07, LM11, 108A or 101A sockets with or without removal of external frequency compensation or nulling components. The LT1012 can also be used in 741, LF411, LF156 or OP-15 applications provided that the nulling circuitry is removed.

The LT1012 is specified over a wide range of power supply voltages from $\pm 2V$ to $\pm 18V$. Operation with lower supplies is possible down to $\pm 1.0V$ (two Ni-Cad batteries).

Achieving Picoampere/Microvolt Performance

In order to realize the picoampere — microvolt level accuracy of the LT1012, proper care must be exercised. For example, leakage currents in circuitry external to the op amp can significantly degrade performance. High quality insulation should be used (e.g. Teflon, Kel-F); cleaning of all insulating surfaces to remove fluxes and other residues will probably be required. Surface coating may be necessary to provide a moisture barrier in high humidity environments.



APPLICATIONS INFORMATION

Board leakage can be minimized by encircling the input circuitry with a guard ring operated at a potential close to that of the inputs: in inverting configurations the guard ring should be tied to ground, in non-inverting connections to the inverting input at pin 2. Guarding both sides of the printed circuit board is required. Bulk leakage reduction depends on the guard ring width. Nanoampere level leakage into the offset trim terminals can affect offset voltage and drift with temperature.

Microvolt level error voltages can also be generated in the external circuitry. Thermocouple effects caused by temperature gradients across dissimilar metals at the contacts to the input terminals can exceed the inherent drift of the amplifier. Air currents over device leads should be minimized, package leads should be short, and the two input leads should be as close together as possible and maintained at the same temperature.

Noise Testing

For application information on noise testing and calculations, please see the LT1008 data sheet.

Frequency Compensation

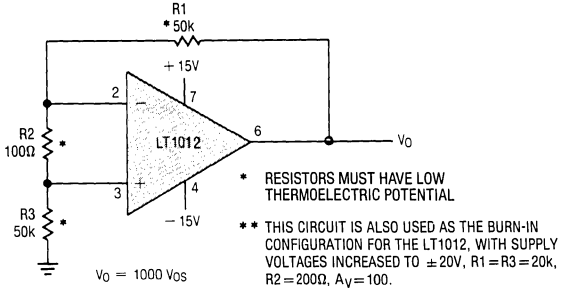
The LT1012 can be overcompensated to improve capacitive load handling capability or to narrow noise bandwidth. In many applications, the feedback loop around the amplifier has gain (e.g. logarithmic amplifiers); overcompensation can stabilize these circuits with a single capacitor.

The availability of the compensation terminal permits the use of feedforward frequency compensation to enhance slew rate. The voltage follower feedforward scheme bypasses the amplifier's gain stages and slews at nearly 10V/μsec.

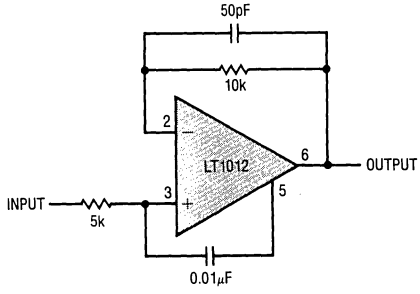
The inputs of the LT1012 are protected with back-to-back diodes. Current limiting resistors are not used, because the leakage of these resistors would prevent the realization of picoampere level bias currents at elevated temperatures. In the voltage follower configuration, when the input is driven by a fast, large signal pulse (> 1V), the input protection diodes effectively short the output to the input during slewing, and a current, limited only by the output short circuit protection will flow through the diodes.

The use of a feedback resistor, as shown in the voltage follower feedforward diagram, is recommended because this resistor keeps the current below the short circuit limit, resulting in faster recovery and settling of the output.

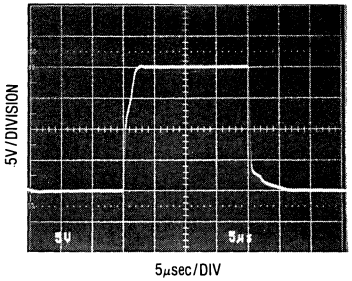
Test Circuit for Offset Voltage and its Drift with Temperature



Follower Feedforward Compensation

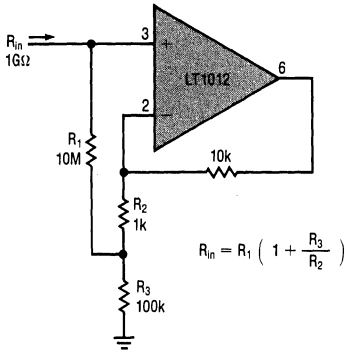


Pulse Response of Feedforward Compensation

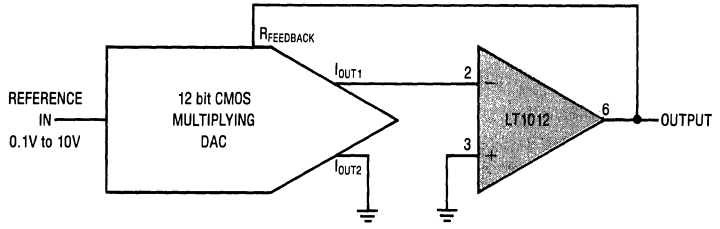


TYPICAL APPLICATIONS

Resistor Multiplier

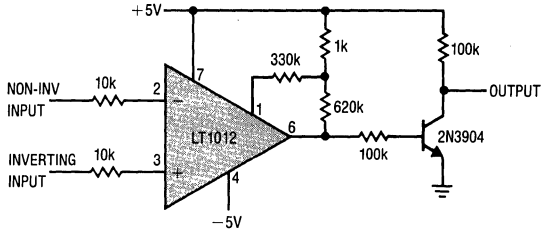


"No Trims" 12 bit Multiplying DAC Output Amplifier

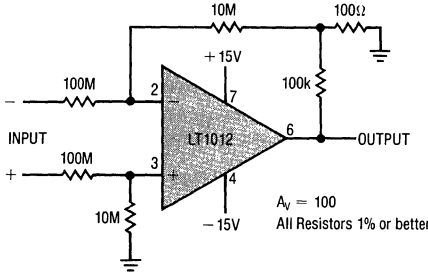


When the reference input drops to 0.1V, the least significant bit decreases to the microvolt/picoampere range.

Low Power Comparator with $<10\mu V$ Hysteresis

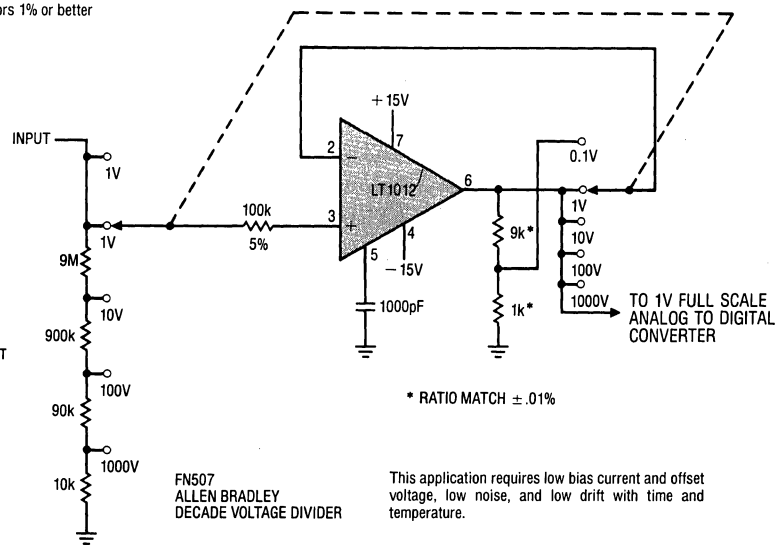


Instrumentation Amplifier with ±100 Volt Common Mode Range



$A_V = 100$
All Resistors 1% or better

Input Amplifier for 4½ Digit Voltmeter

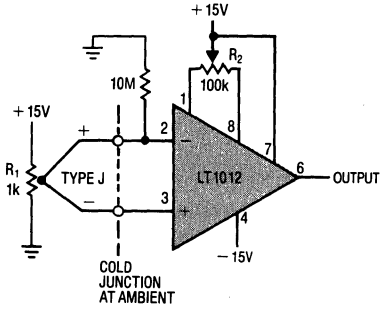


* RATIO MATCH ±.01%

FN507
ALLEN BRADLEY
DECADE VOLTAGE DIVIDER

This application requires low bias current and offset voltage, low noise, and low drift with time and temperature.

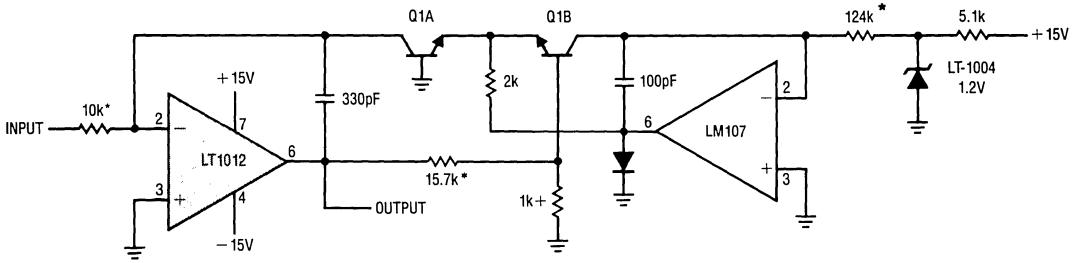
Air Flow Detector



Mount R_1 in airflow.
Adjust R_2 so output goes high when airflow stops.

TYPICAL APPLICATIONS

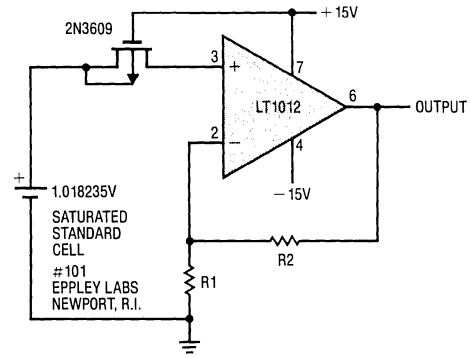
Logarithmic Amplifier



+ = TEL. LABS, TYPE Q81
* = 1% FILM RESISTOR
Q1 = 2N2979

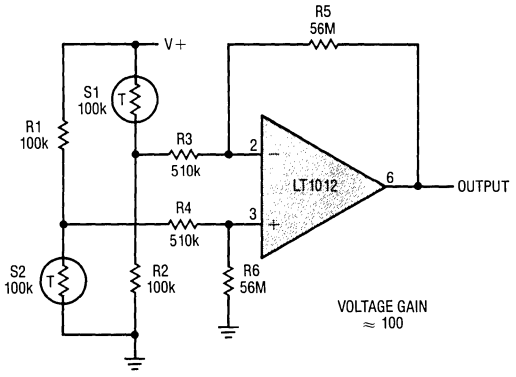
Low bias current and offset voltage of the LT1012 allow 4½ decades of voltage input logging.

Saturated Standard Cell Amplifier

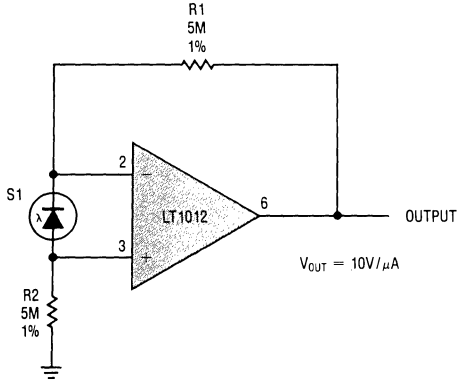


The typical 30pA bias current of the LT1012 will degrade the standard cell by only 1 ppm/year. Noise is a fraction of a ppm. Unprotected gate MOSFET isolates standard cell on power down.

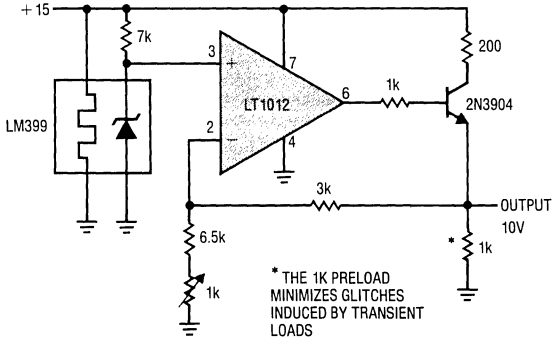
Amplifier for Bridge Transducers



Amplifier For Photodiode Sensor



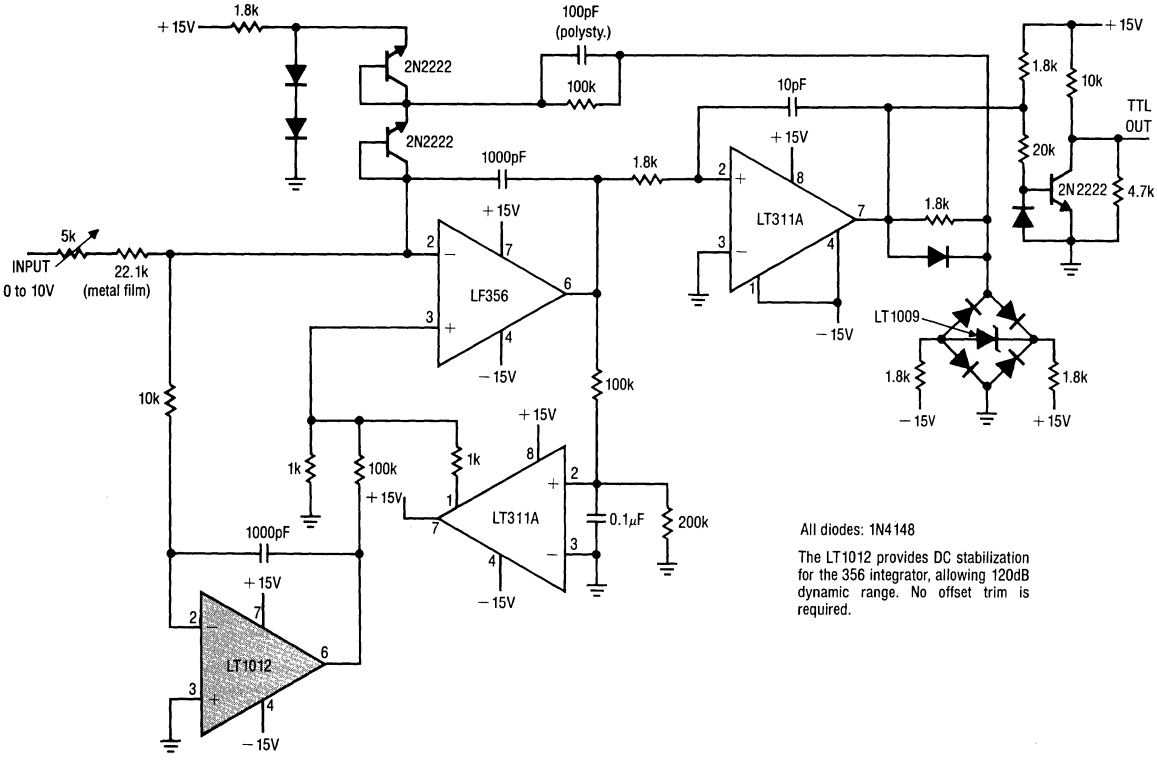
Buffered Reference for A to D Converters



* THE 1K PRELOAD MINIMIZES GLITCHES INDUCED BY TRANSIENT LOADS

TYPICAL APPLICATIONS

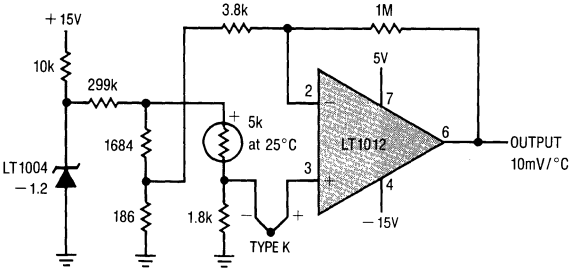
1Hz to 1MHz Voltage to Frequency Converter



All diodes: 1N4148

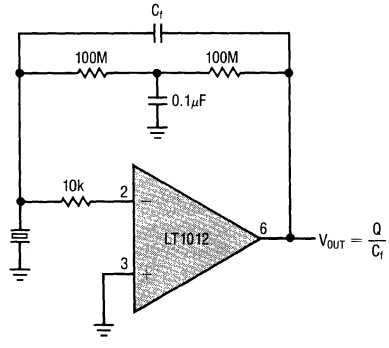
The LT1012 provides DC stabilization for the 356 integrator, allowing 120dB dynamic range. No offset trim is required.

Thermocouple Thermometer

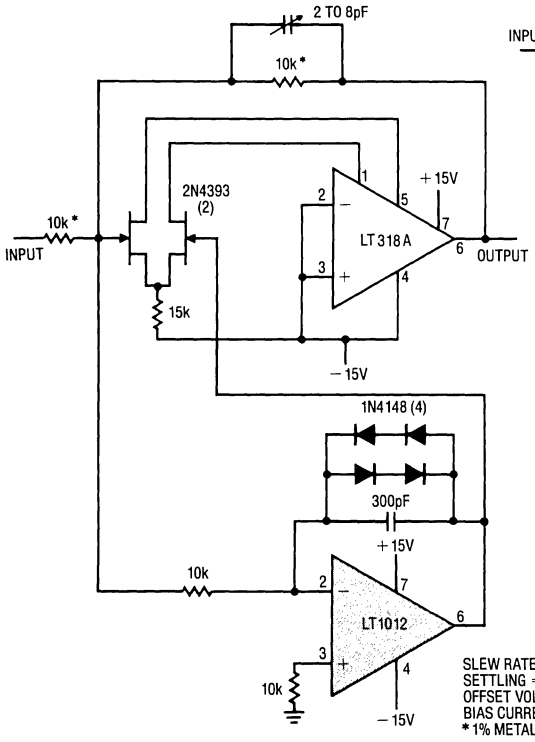


+ YSI #44007
COLD JUNCTION
COMPENSATION ± 1°C
OVER 0 to 60°C

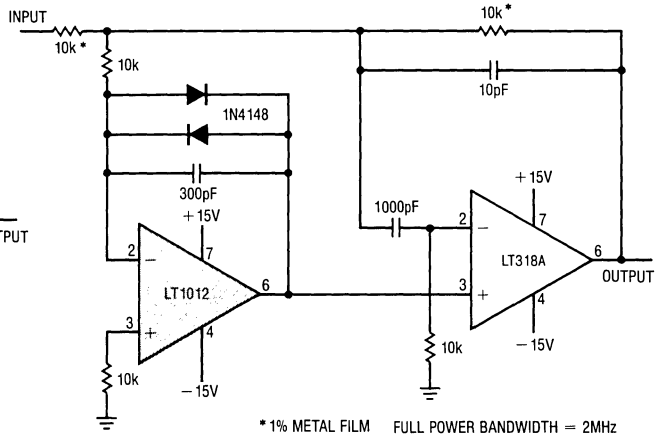
Charge Amplifier for Piezoelectric Transducers



Fast Precision Inverters



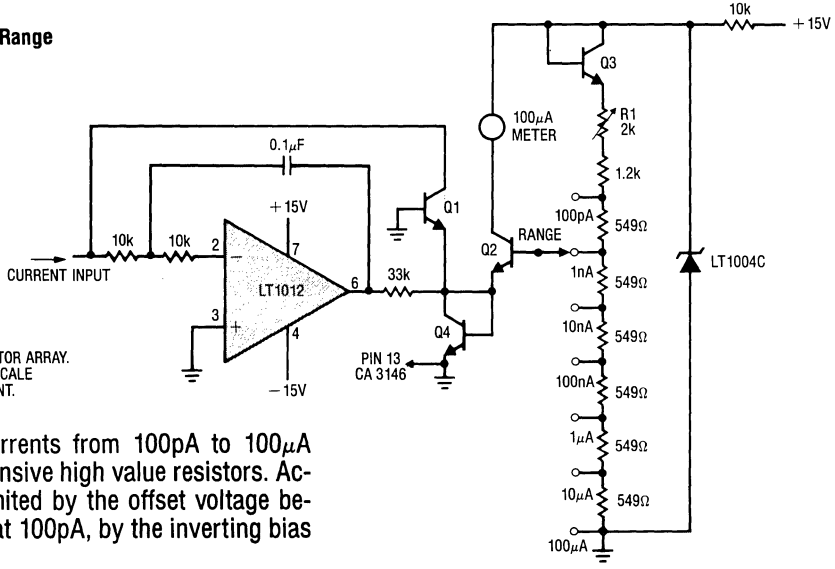
SLEW RATE @ 100V/μS
SETTLING = 5μS TO .01%/10 VOLT STEP
OFFSET VOLTAGE = 30μV
BIAS CURRENT = 30pA
*1% METAL FILM



*1% METAL FILM

FULL POWER BANDWIDTH = 2MHz
SLEW RATE = 50V/μsec
SETTLING (10V STEP) = 12μS TO 0.01%
BIAS CURRENT DC = 30pA
OFFSET DRIFT = 0.3μV/°C
OFFSET VOLTAGE = 30μV

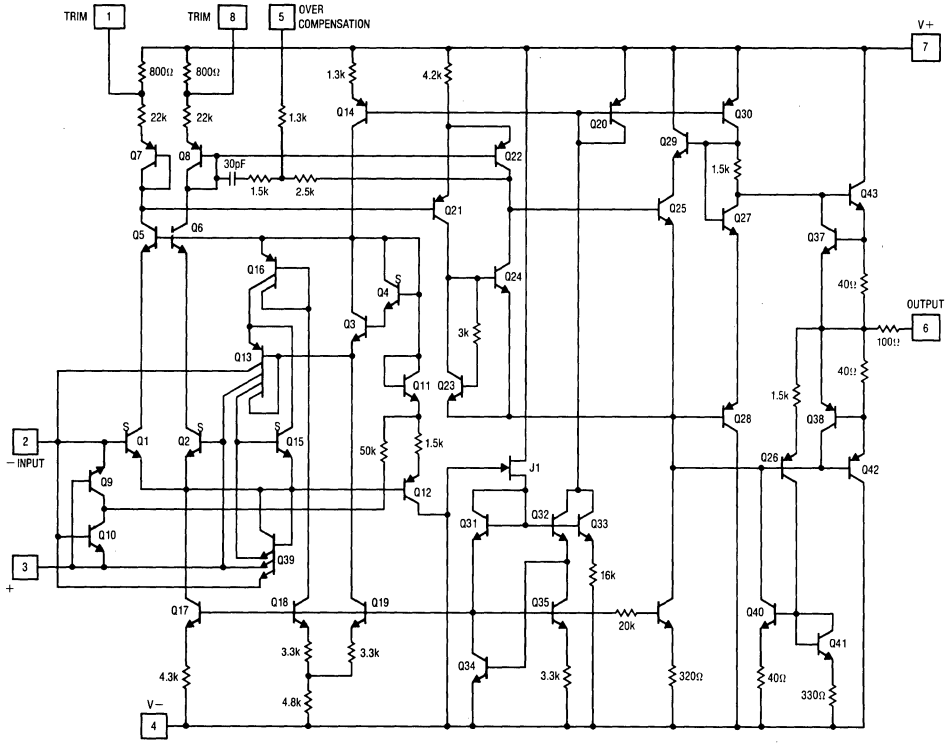
Ammeter With Six Decade Range



Q1, Q2, Q3, Q4, RCA CA3146 TRANSISTOR ARRAY.
CALIBRATION: ADJUST R1 FOR FULL SCALE DEFLECTION WITH 1μA INPUT CURRENT.

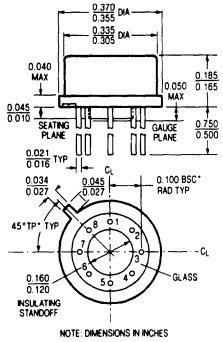
Ammeter measures currents from 100pA to 100μA without the use of expensive high value resistors. Accuracy at 100μA is limited by the offset voltage between Q1 and Q2 and, at 100pA, by the inverting bias current of the LT1012.

SCHEMATIC DIAGRAM



PACKAGE DESCRIPTION

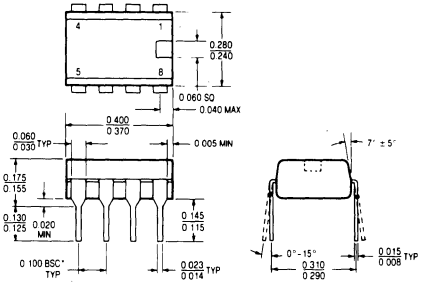
H Package
Metal Can



NOTE: DIMENSIONS IN INCHES

$T_j$max	Θ_{ja}	Θ_{jc}
150°C	150°C/W	45°C/W

N8 Package
8 Lead Plastic



NOTE: DIMENSIONS IN INCHES UNLESS OTHERWISE NOTED
*LEADS WITHIN 0.007 OF TRUE POSITION (TP) AT GAUGE PLANE

$T_j$max	Θ_{ja}
100°C	130°C/W

Quad Precision Op Amp (LT1014)
Dual Precision Op Amp (LT1013)

FEATURES

- Single Supply Operation
  - Input Voltage Range Extends to Ground
  - Output Swings to Ground while Sinking Current
- Pin Compatible to 1458 and 324 with Precision Specs
- *Guaranteed* Offset Voltage — 150μV Max.
- *Guaranteed* Low Drift — 2μV/°C Max.
- *Guaranteed* Offset Current — 0.8nA Max.
- *Guaranteed* High Gain
  - 5mA Load Current — 1.5 Million Min.
  - 17mA Load Current — 0.8 Million Min.
- *Guaranteed* Low Supply Current — 500μA Max.
- Low Voltage Noise, 0.1Hz to 10Hz — 0.55μVp-p
- Low Current Noise—Better than OP-07, 0.07 pA/√Hz

APPLICATIONS

- Battery-Powered Precision Instrumentation
  - Strain Gauge Signal Conditioners
  - Thermocouple Amplifiers
  - Instrumentation Amplifiers
- 4mA–20mA Current Loop Transmitters
- Multiple Limit Threshold Detection
- Active Filters
- Multiple Gain Blocks

DESCRIPTION

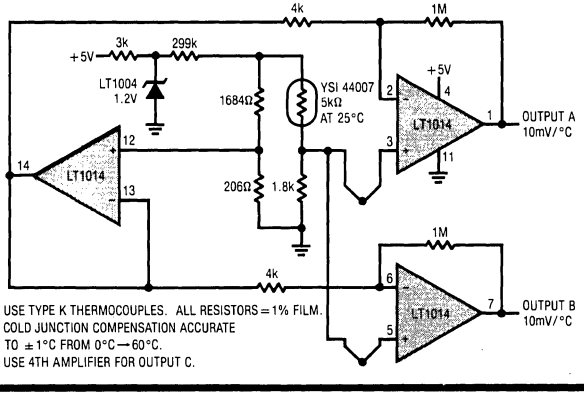
The LT1014 is the first precision quad operational amplifier which directly upgrades designs in the industry standard 14-pin DIP LM324/LM348/OP-11/4156 pin configuration. It is no longer necessary to compromise specifications, while saving board space and cost, as compared to single operational amplifiers.

The LT1014's low offset voltage of 50μV, drift of 0.3μV/°C, offset current of 0.15nA, gain of 8 million, common-mode rejection of 117dB, and power supply rejection of 120dB qualify it as four truly precision operational amplifiers. Particularly important is the low offset voltage, since no offset null terminals are provided in the quad configuration. Although supply current is only 350μA per amplifier, a new output stage design sources and sinks in excess of 20mA of load current, while retaining high voltage gain.

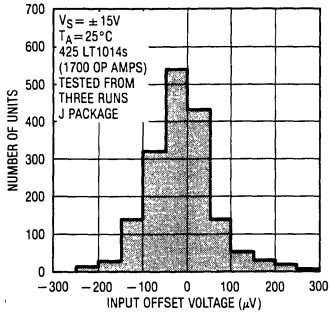
Similarly, the LT1013 is the first precision dual op amp in the 8-pin industry standard configuration, upgrading the performance of such popular devices as the MC1458/1558, LM158 and OP-221. The LT1013's specifications are similar to (even somewhat better than) the LT1014's.

Both the LT1013 and LT1014 can be operated off a single 5V power supply: input common-mode range includes ground; the output can also swing to within a few millivolts of ground. Crossover distortion, so apparent on previous single-supply designs, is eliminated. A full set of specifications is provided with ±15V and single 5V supplies.

3 Channel Thermocouple Thermometer



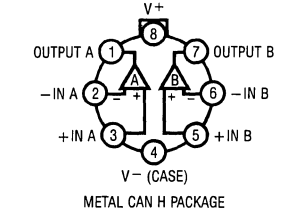
LT1014 Distribution of Offset Voltage



ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... ±22V
Differential Input Voltage ..... ±30V
Input Voltage ..... Equal to Positive Supply Voltage
..... 5V Below Negative Supply Voltage
Output Short Circuit Duration ..... Indefinite
Operating Temperature Range
LT1013AM/LT1013M/
LT1014AM/LT1014M ..... −55°C to 125°C
LT1013AC/1013C/1013D
LT1014AC/1014C/1014D ..... 0°C to 70° C
Storage Temperature Range
All Grades ..... −65°C to 150°C
Lead Temperature (Soldering, 10 sec.)..... 300°C

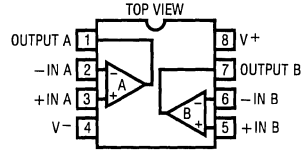
PACKAGE/ORDER INFORMATION



METAL CAN H PACKAGE

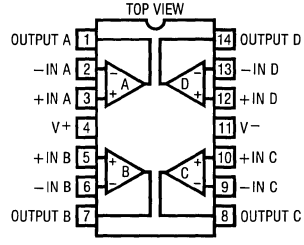
ORDER PART NUMBER

LT1013AMH
LT1013MH
LT1013ACH
LT1013CH



HERMETIC DIP J8 PACKAGE
PLASTIC DIP N8 PACKAGE

LT1013AMJ8
LT1013MJ8
LT1013ACJ8
LT1013CJ8
LT1013CN8
LT1013DN8



HERMETIC DIP J14 PACKAGE
PLASTIC DIP N14 PACKAGE

LT1014AMJ
LT1014MJ
LT1014ACJ
LT1014CJ
LT1014CN
LT1014DN

ELECTRICAL CHARACTERISTICS

$V_S = \pm 15V$, $V_{CM} = 0V$, $T_A = 25°C$ unless otherwise noted

SYMBOL	PARAMETER	CONDITIONS	LT1013AM LT1013AC LT1014AM LT1014AC			LT1013M/LT1013C LT1013DN8 LT1014M/LT1014C LT1014DN			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{OS}	Input Offset Voltage	LT1013	—	40	150	—	60	300	μV
		LT1014	—	50	180	—	60	300	μV
		LT1013DN8/LT1014DN	—	—	—	—	200	800	μV
	Long Term Input Offset Voltage Stability		—	0.4	—	—	0.5	—	μV/Mo.
I_{OS}	Input Offset Current		—	0.15	0.8	—	0.2	1.5	nA
I_B	Input Bias Current		—	12	20	—	15	30	nA
e_n	Input Noise Voltage	0.1Hz to 10Hz	—	0.55	—	—	0.55	—	μVp-p
e_n	Input Noise Voltage Density	$f_0 = 10Hz$	—	24	—	—	24	—	$nV/\sqrt{Hz}$
		$f_0 = 1000Hz$	—	22	—	—	22	—	$nV/\sqrt{Hz}$
i_n	Input Noise Current Density	$f_0 = 10Hz$	—	0.07	—	—	0.07	—	$pA/\sqrt{Hz}$
	Input Resistance—Differential	(Note 1)	100	400	—	70	300	—	MΩ
	Common-Mode		—	5	—	—	4	—	GΩ

ELECTRICAL CHARACTERISTICS

$V_S = \pm 15V$, $V_{CM} = 0V$, $T_A = 25°C$ unless otherwise noted

SYMBOL	PARAMETER	CONDITIONS	LT1013AM LT1013AC LT1014AM LT1014AC			LT1013M/LT1013C LT1013DN8 LT1014M/LT1014C LT1014DN			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
A_{VOL}	Large Signal Voltage Gain	$V_O = \pm 10V$, $R_L = 2k$ $V_O = \pm 10V$, $R_L = 600\Omega$	1.5 0.8	8.0 2.5	— —	1.2 0.5	7.0 2.0	— —	V/μV V/μV
	Input Voltage Range		+13.5 −15.0	+13.8 −15.3	— —	+13.5 −15.0	+13.8 −15.3	— —	V V
CMRR	Common-Mode Rejection Ratio	$V_{CM} = +13.5V, -15.0V$	100	117	—	97	114	—	dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 2V$ to $\pm 18V$	103	120	—	100	117	—	dB
	Channel Separation	$V_O = \pm 10V$, $R_L = 2k$	123	140	—	120	137	—	dB
V_{OUT}	Output Voltage Swing	$R_L = 2k$	±13	±14	—	±12.5	±14	—	V
	Slew Rate		0.2	0.4	—	0.2	0.4	—	V/μs
I_S	Supply Current	Per Amplifier	—	0.35	0.50	—	0.35	0.55	mA

Note 1: This parameter is guaranteed by design and is not tested. Typical parameters are defined as the 60% yield of parameter distributions of individual amplifiers; i.e., out of 100 LT1014s (or 100 LT1013s) typically 240 op amps (or 120) will be better than the indicated specification.

ELECTRICAL CHARACTERISTICS

$V_S^+ = +5V$, $V_S^- = 0V$, $V_{OUT} = 1.4V$, $V_{CM} = 0V$, $T_A = 25°C$ unless otherwise noted

SYMBOL	PARAMETER	CONDITIONS	LT1013AM LT1013AC LT1014AM LT1014AC			LT1013M/LT1013C LT1013DN8 LT1014M/LT1014C LT1014DN			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{OS}	Input Offset Voltage	LT1013 LT1014 LT1013DN8/LT1014DN	— — —	60 70 —	250 280 —	— — —	90 90 250	450 450 950	μV μV μV
I_{OS}	Input Offset Current		—	0.2	1.3	—	0.3	2.0	nA
I_B	Input Bias Current		—	15	35	—	18	50	nA
A_{VOL}	Large Signal Voltage Gain	$V_O = 5mV$ to $4V$, $R_L = 500\Omega$	—	1.0	—	—	1.0	—	V/μV
	Input Voltage Range		+3.5 0	+3.8 −0.3	— —	+3.5 0	+3.8 −0.3	— —	V V
V_{OUT}	Output Voltage Swing	Output Low, No Load Output Low, 600Ω to Ground Output Low, $I_{SINK} = 1mA$ Output High, No Load Output High, 600Ω to Ground	— — — 4.0 3.4	15 5 220 4.4 4.0	25 10 350 — —	— — — 4.0 3.4	15 5 220 4.4 4.0	25 10 350 — —	mV mV mV V V
I_S	Supply Current	Per Amplifier	—	0.31	0.45	—	0.32	0.50	mA

ELECTRICAL CHARACTERISTICS $V_S = \pm 15V$, $V_{CM} = 0V$, $-55°C \le T_A \le 125°C$ unless otherwise noted

SYMBOL	PARAMETER	CONDITIONS		LT1013AM MIN	LT1013AM TYP	LT1013AM MAX	LT1014AM MIN	LT1014AM TYP	LT1014AM MAX	LT1013M/LT1014M MIN	LT1013M/LT1014M TYP	LT1013M/LT1014M MAX	UNITS
V_{OS}	Input Offset Voltage		●	—	80	300	—	90	350	—	110	550	μV
		$V_S = +5V, 0V$; $V_O = +1.4V$											
		$-55°C \le T_A \le 100°C$	●	—	80	450	—	90	480	—	100	750	μV
		$V_{CM} = 0.1V$, $T_A = 125°C$		—	120	450	—	150	480	—	200	750	μV
		$V_{CM} = 0V$, $T_A = 125°C$		—	250	900	—	300	960	—	400	1500	μV
	Input Offset Voltage Drift	(Note 2)	●	—	0.4	2.0	—	0.4	2.0	—	0.5	2.5	μV/°C
I_{OS}	Input Offset Current		●	—	0.3	2.5	—	0.3	2.8	—	0.4	5.0	nA
		$V_S = +5V, 0V$; $V_O = +1.4V$	●	—	0.6	6.0	—	0.7	7.0	—	0.9	10.0	nA
I_B	Input Bias Current		●	—	15	30	—	15	30	—	18	45	nA
		$V_S = +5V, 0V$; $V_O = +1.4V$	●	—	20	80	—	25	90	—	28	120	nA
A_{VOL}	Large Signal Voltage Gain	$V_O = \pm 10V$, $R_L = 2k$	●	0.5	2.0	—	0.4	2.0	—	0.25	2.0	—	V/μV
CMRR	Common-Mode Rejection	$V_{CM} = +13.0V, -14.9V$	●	97	114	—	96	114	—	94	113	—	dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 2V$ to $\pm 18V$	●	100	117	—	100	117	—	97	116	—	dB
V_{OUT}	Output Voltage Swing	$R_L = 2k$	●	±12	±13.8	—	±12	±13.8	—	±11.5	±13.8	—	V
		$V_S = +5V, 0V$;											
		$R_L = 600\Omega$ to Ground											
		Output Low	●	—	6	15	—	6	15	—	6	18	mV
		Output High	●	3.2	3.8	—	3.2	3.8	—	3.1	3.8	—	V
I_S	Supply Current Per Amplifier		●	—	0.38	0.60	—	0.38	0.60	—	0.38	0.7	mA
		$V_S = +5V, 0V$; $V_O = +1.4V$	●	—	0.34	0.55	—	0.34	0.55	—	0.34	0.65	mA

ELECTRICAL CHARACTERISTICS $V_S = \pm 15V$, $V_{CM} = 0V$, $0°C \le T_A \le 70°C$ unless otherwise noted

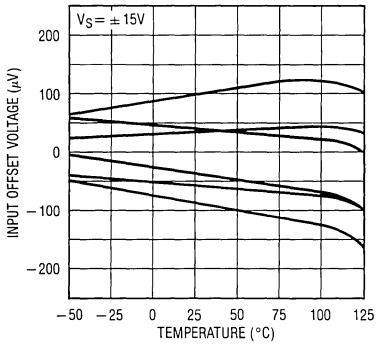
SYMBOL	PARAMETER	CONDITIONS		LT1013AC MIN	LT1013AC TYP	LT1013AC MAX	LT1014AC MIN	LT1014AC TYP	LT1014AC MAX	LT1013C/LT1013DN8 LT1014C/LT1014DN MIN	LT1013C/LT1013DN8 LT1014C/LT1014DN TYP	LT1013C/LT1013DN8 LT1014C/LT1014DN MAX	UNITS
V_{OS}	Input Offset Voltage		●	—	55	240	—	65	270	—	80	400	μV
		LT1013DN8, LT1014DN	●	—	—	—	—	—	—	—	230	1000	μV
		$V_S = +5V, 0V$; $V_O = 1.4V$	●	—	75	350	—	85	380	—	110	570	μV
		LT1013DN8, LT1014DN	●	—	—	—	—	—	—	—	280	1200	μV
	Average Input Offset Voltage Drift	(Note 2)	●	—	0.3	2.0	—	0.3	2.0	—	0.4	2.5	μV/°C
		LT1013DN, LT1014DN	●	—	—	—	—	—	—	—	0.7	5.0	μV/°C
I_{OS}	Input Offset Current		●	—	0.2	1.5	—	0.2	1.7	—	0.3	2.8	nA
		$V_S = +5V, 0V$; $V_O = 1.4V$	●	—	0.4	3.5	—	0.4	4.0	—	0.5	6.0	nA
I_B	Input Bias Current		●	—	13	25	—	13	25	—	16	38	nA
		$V_S = +5V, 0V$; $V_O = 1.4V$	●	—	18	55	—	20	60	—	24	90	nA
A_{VOL}	Large Signal Voltage Gain	$V_O = \pm 10V$, $R_L = 2k$	●	1.0	5.0	—	1.0	5.0	—	0.7	4.0	—	V/μV
CMRR	Common-Mode Rejection Ratio	$V_{CM} = +13.0V, -15.0V$	●	98	116	—	98	116	—	94	113	—	dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 2V$ to $\pm 18V$	●	101	119	—	101	119	—	97	116	—	dB
V_{OUT}	Output Voltage Swing	$R_L = 2k$	●	±12.5	±13.9	—	±12.5	±13.9	—	±12.0	±13.9	—	V
		$V_S = +5V, 0V$; $R_L = 600\Omega$											
		Output Low	●	—	6	13	—	6	13	—	6	13	mV
		Output High	●	3.3	3.9	—	3.3	3.9	—	3.2	3.9	—	V
I_S	Supply Current per Amplifier		●	—	0.36	0.55	—	0.36	0.55	—	0.37	0.60	mA
		$V_S = +5V, 0V$; $V_O = 1.4V$	●	—	0.32	0.50	—	0.32	0.50	—	0.34	0.55	mA

Note 2: This parameter is not 100% tested.

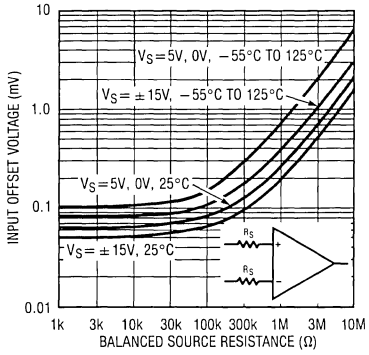
The ● denotes the specifications which apply over the full operating temperature range.

TYPICAL PERFORMANCE CHARACTERISTICS

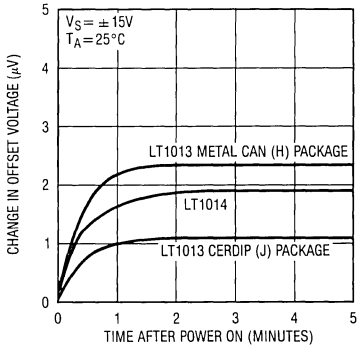
Offset Voltage Drift with Temperature of Representative Units



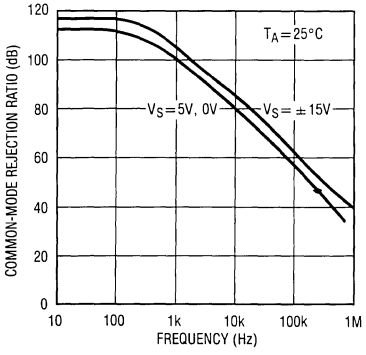
Offset Voltage vs Balanced Source Resistance



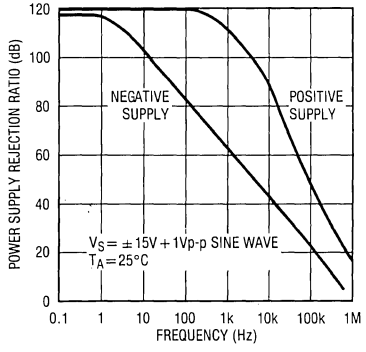
Warm-Up Drift



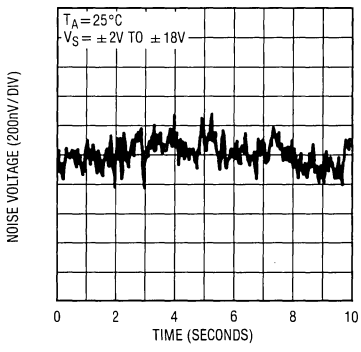
Common-Mode Rejection Ratio vs Frequency



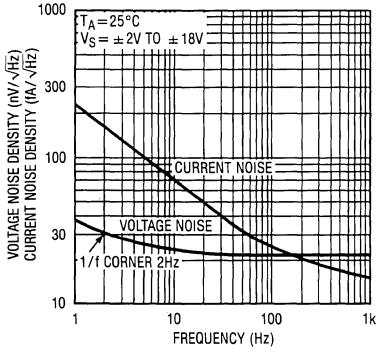
Power Supply Rejection Ratio vs Frequency



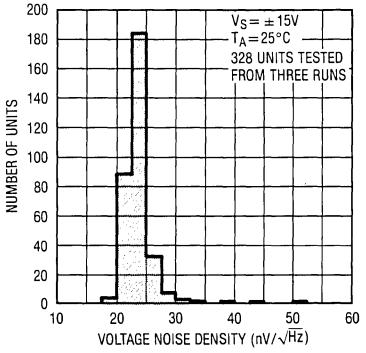
0.1Hz to 10Hz Noise



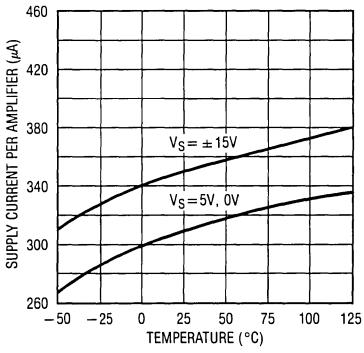
Noise Spectrum



10Hz Voltage Noise Distribution

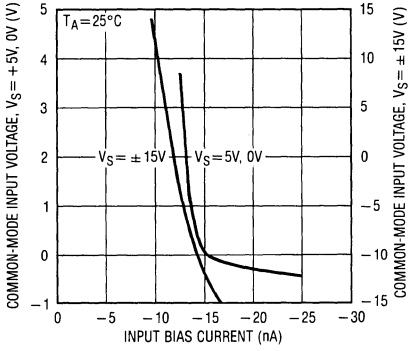


Supply Current vs Temperature

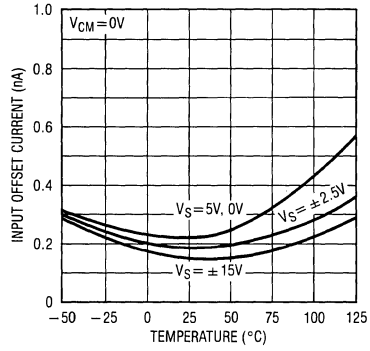


TYPICAL PERFORMANCE CHARACTERISTICS

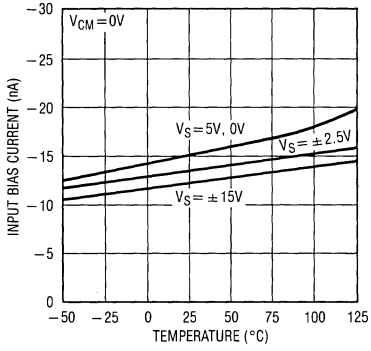
Input Bias Current vs Common-Mode Voltage



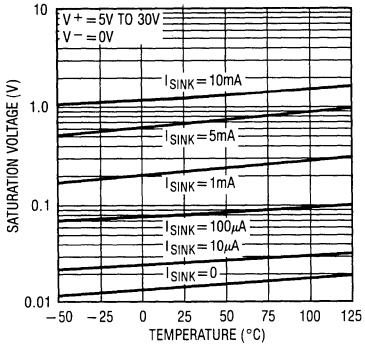
Input Offset Current vs Temperature



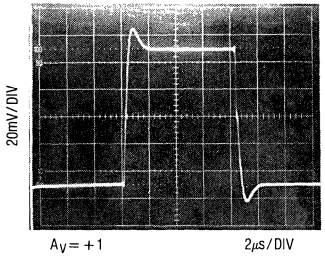
Input Bias Current vs Temperature



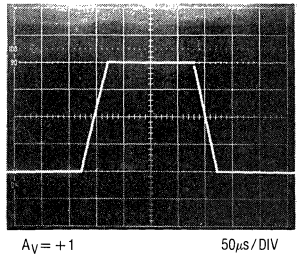
Output Saturation vs Sink Current vs Temperature



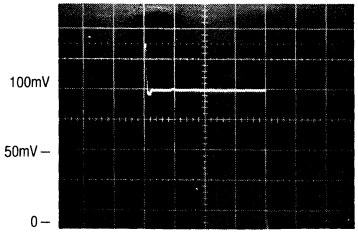
Small Signal Transient Response, V_S = ±15V



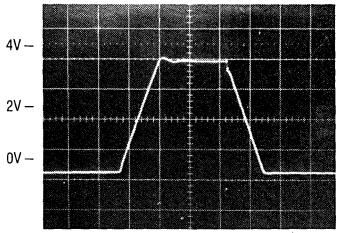
Large Signal Transient Response, V_S = ±15V



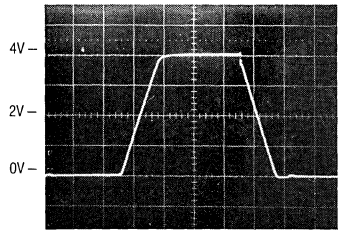
Small Signal Transient Response, V_S = 5V, 0V



Large Signal Transient Response, V_S = 5V, 0V

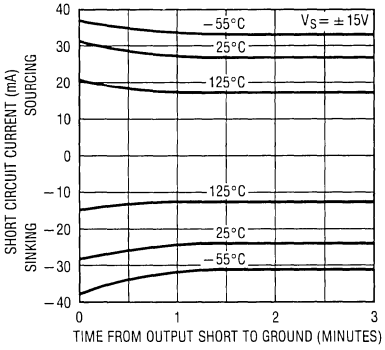


Large Signal Transient Response, V_S = 5V, 0V

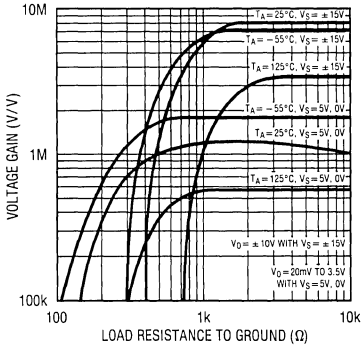


TYPICAL PERFORMANCE CHARACTERISTICS

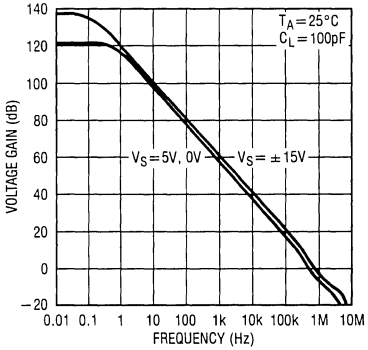
Output Short Circuit Current vs Time



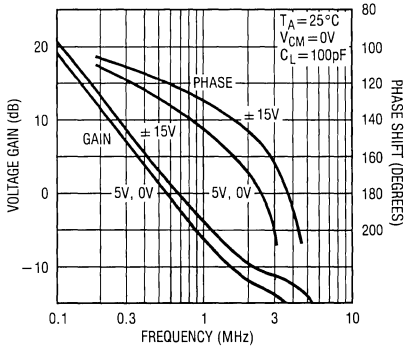
Voltage Gain vs Load Resistance



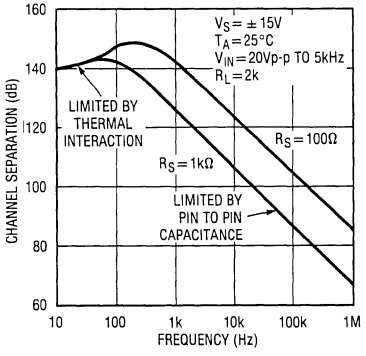
Voltage Gain vs Frequency



Gain, Phase vs Frequency



Channel Separation vs Frequency



APPLICATIONS INFORMATION

Single Supply Operation

The LT1013/1014 are fully specified for single supply operation, i.e., when the negative supply is 0V. Input common-mode range includes ground; the output swings within a few millivolts of ground. Single supply operation, however, can create special difficulties, both at the input and at the output. The LT1013/LT1014 have specific circuitry which addresses these problems.

At the input, the driving signal can fall below 0V—inadvertently or on a transient basis. If the input is more than a few hundred millivolts below ground, two distinct problems can occur on previous single supply designs, such as the LM124, LM158, OP-20, OP-21, OP-220, OP-221, OP-420:

a) When the input is more than a diode drop below ground, unlimited current will flow from the substrate (V^- terminal) to the input. This can destroy the unit. On the LT1013/1014, the 400Ω resistors, in series with the input (see schematic diagram), protect the devices even when the input is 5V below ground.

APPLICATIONS INFORMATION

(b) When the input is more than 400mV below ground (at 25°C), the input stage saturates (transistors Q3 and Q4) and phase reversal occurs at the output. This can cause lock-up in servo systems. Due to a unique phase reversal protection circuitry (Q21, Q22, Q27, Q28), the LT1013/1014's outputs do not reverse, as illustrated below, even when the inputs are at −1.5V.

There is one circumstance, however, under which the phase reversal protection circuitry does not function: when the other op amp on the LT1013, or one specific amplifier of the other three on the LT1014, is driven hard into negative saturation at the output.

Phase reversal protection does not work on amplifier:
A when D's output is in negative saturation. B's and C's outputs have no effect.
B when C's output is in negative saturation. A's and D's outputs have no effect.
C when B's output is in negative saturation. A's and D's outputs have no effect.
D when A's output is in negative saturation. B's and C's outputs have no effect.

At the output, the aforementioned single supply designs either cannot swing to within 600mV of ground (OP-20) or cannot sink more than a few microamperes while swinging to ground (LM124, LM158). The LT1013/1014's all-NPN output stage maintains its low output resistance and high gain characteristics until the output is saturated.

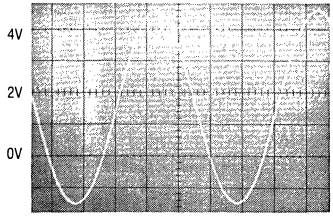
In dual supply operations, the output stage is crossover distortion-free.

Comparator Applications

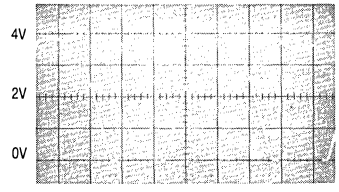
The single supply operation of the LT1013/1014 lends itself to its use as a precision comparator with TTL compatible output:

In systems using both op amps and comparators, the LT1013/1014 can perform multiple duties; for example, on the LT1014, two of devices can be used as op amps and the other two as comparators.

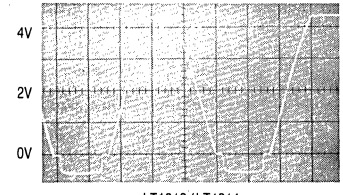
Voltage Follower with Input Exceeding the Negative Common-Mode Range



6Vp-p INPUT, −1.5V TO 4.5V

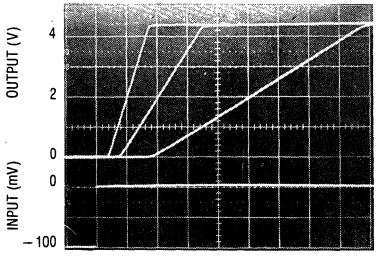


LM324, LM358, OP-20
EXHIBIT OUTPUT PHASE
REVERSAL



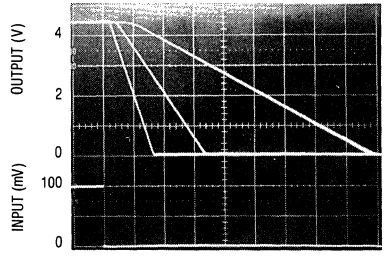
LT1013/LT1014
NO PHASE REVERSAL

Comparator Rise Response Time
10mV, 5mV, 2mV Overdrives



V_S = 5V, 0V 50µs/DIV

Comparator Fall Response Time
to 10mV, 5mV, 2mV Overdrives



V_S = 5V, 0V 50µs/DIV

APPLICATIONS INFORMATION

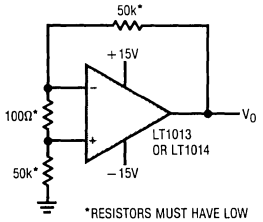
Low Supply Operation

The minimum supply voltage for proper operation of the LT1013/1014 is 3.4V (three Ni-Cad batteries). Typical supply current at this voltage is 290μA, therefore power dissipation is only one milliwatt per amplifier.

Noise Testing

For application information on noise testing and calculations, please see the LT1007 or LT1008 data sheet.

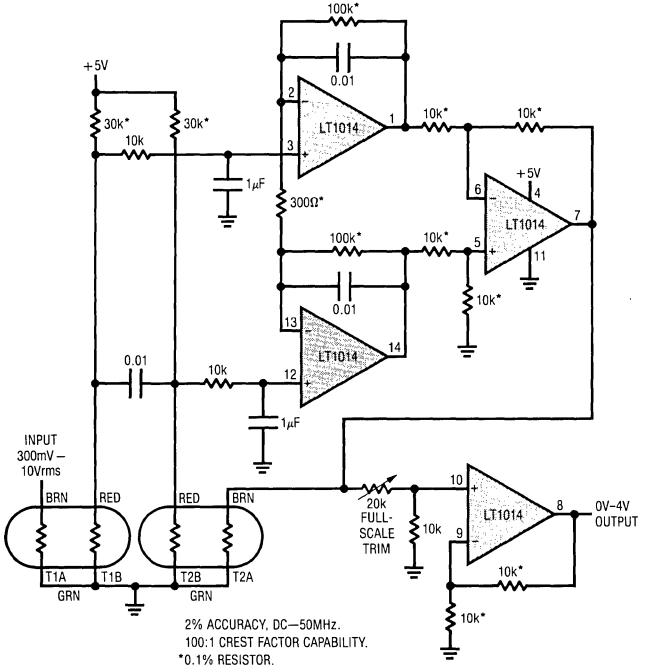
Test Circuit for Offset Voltage and Offset Drift with Temperature



*RESISTORS MUST HAVE LOW THERMOELECTRIC POTENTIAL.
**THIS CIRCUIT IS ALSO USED AS THE BURN-IN CONFIGURATION, WITH SUPPLY VOLTAGES INCREASED TO ±20V.
$V_O = 1000V_{OS}$

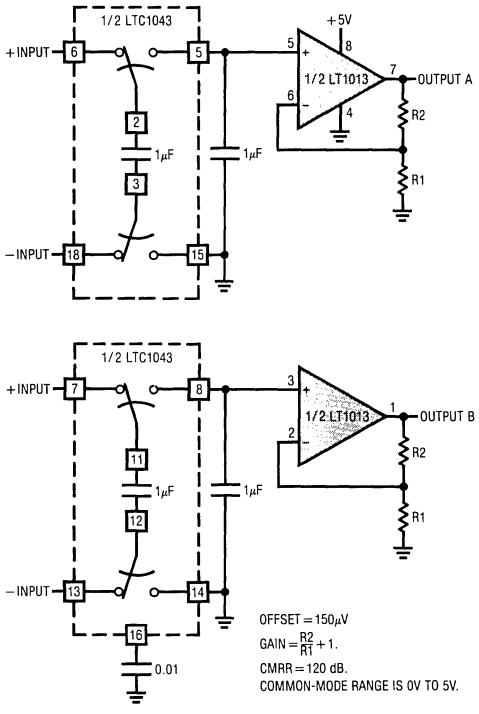
TYPICAL APPLICATIONS

50MHz Thermal rms to DC Converter



2% ACCURACY, DC—50MHz.
100:1 CREST FACTOR CAPABILITY.
*0.1% RESISTOR.
T1-T2 = YELLOW SPRINGS INST. CO. THERMISTOR COMPOSITE #44018.
ENCLOSE T1 AND T2 IN STYROFOAM.
7.5mW DISSIPATION.

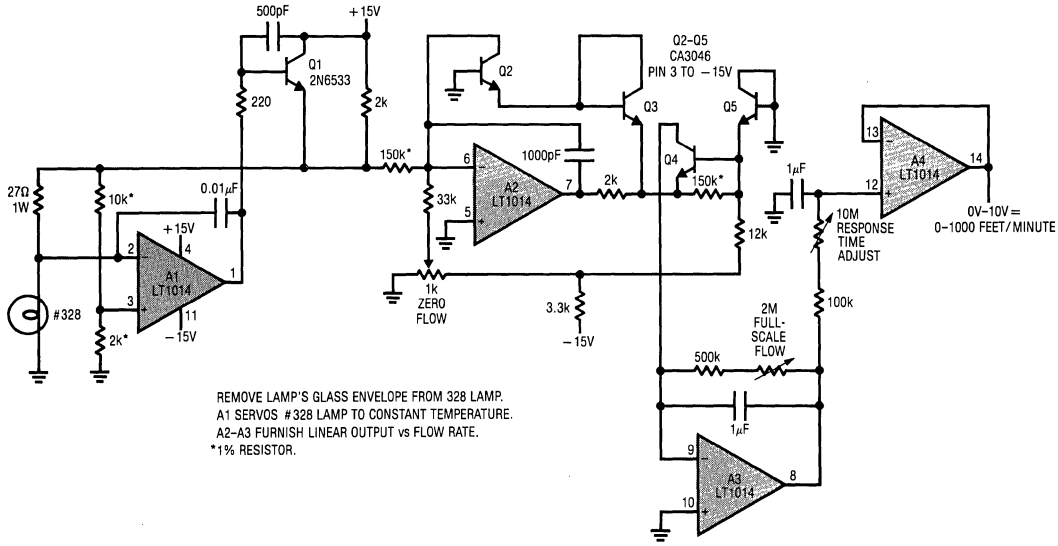
5V Single Supply Dual Instrumentation Amplifier



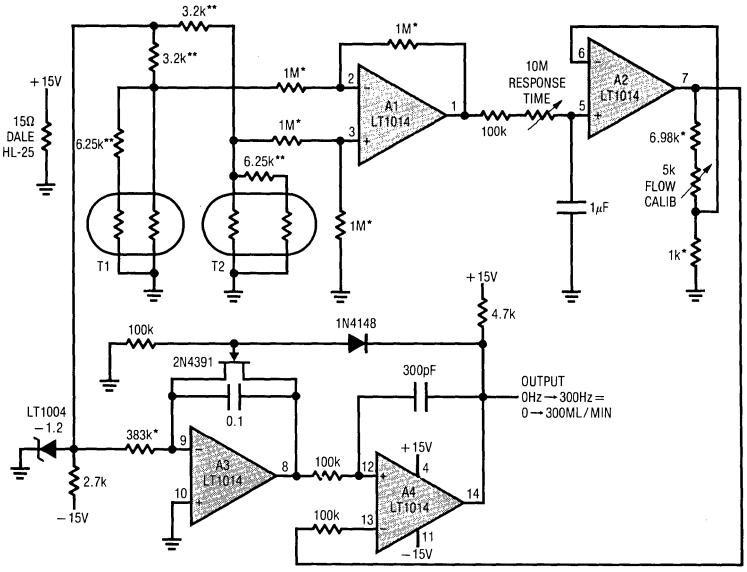
OFFSET = 150μV
GAIN = $\frac{R2}{R1}$ + 1.
CMRR = 120 dB.
COMMON-MODE RANGE IS 0V TO 5V.

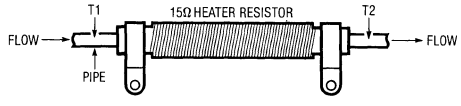
TYPICAL APPLICATIONS

Hot Wire Anemometer



Liquid Flowmeter

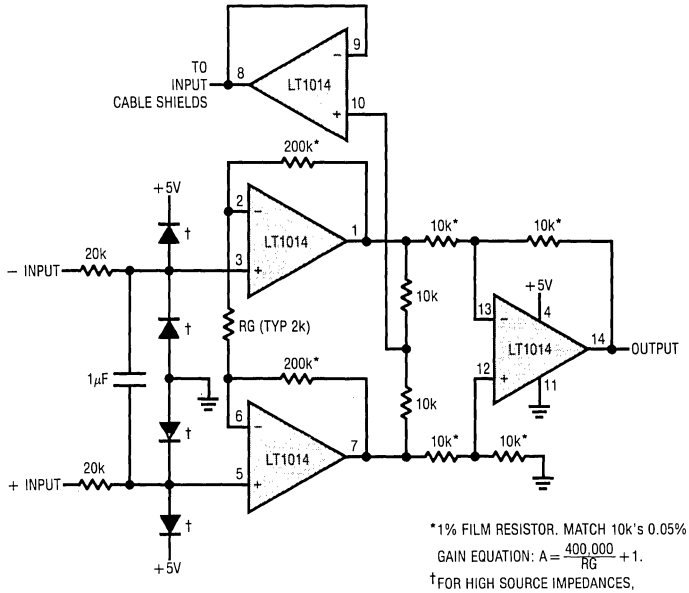




*1% FILM RESISTOR.
**SUPPLIED WITH YSI THERMISTOR NETWORK.
T1, T2 YSI THERMISTOR NETWORK = #44201.
FLOW IN PIPE IS INVERSELY PROPORTIONAL TO RESISTANCE OF T1–T2 TEMPERATURE DIFFERENCE.
A1–A2 PROVIDE GAIN. A3–A4 PROVIDE LINEARIZED FREQUENCY OUTPUT.

TYPICAL APPLICATIONS

5V Powered Precision Instrumentation Amplifier

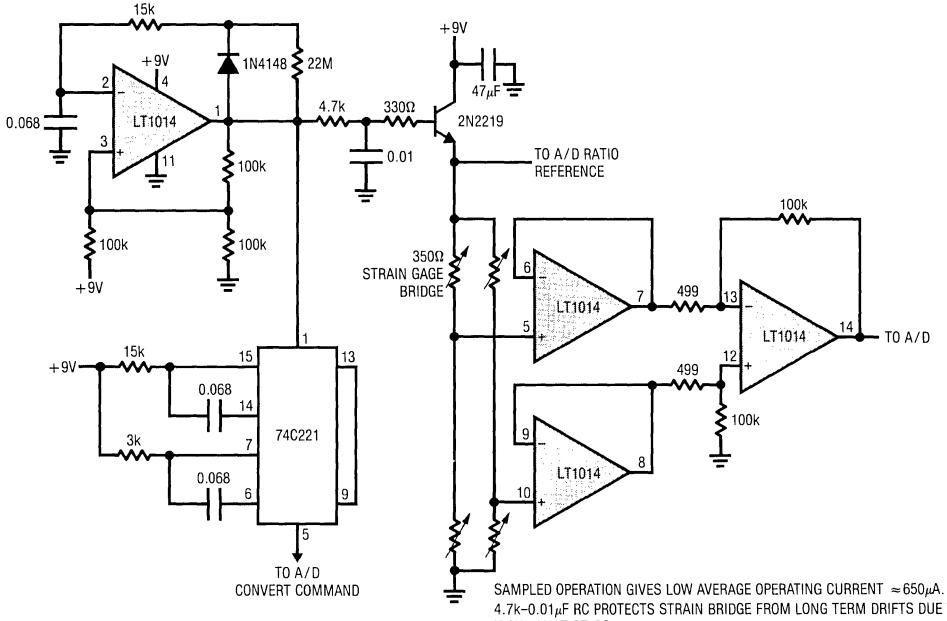


*1% FILM RESISTOR. MATCH 10k's 0.05%

GAIN EQUATION: $A = \frac{400,000}{RG} + 1$.

†FOR HIGH SOURCE IMPEDANCES, USE 2N2222 AS DIODES.

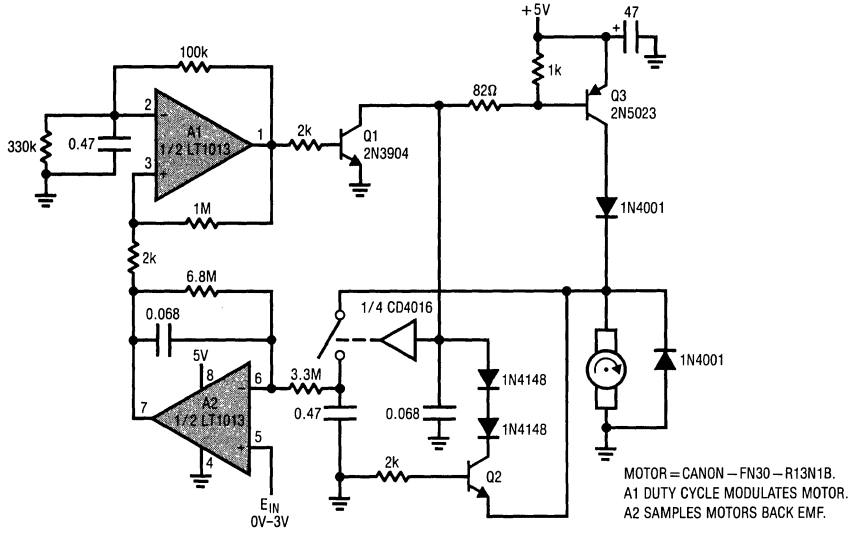
9V Battery Powered Strain Gage Signal Conditioner



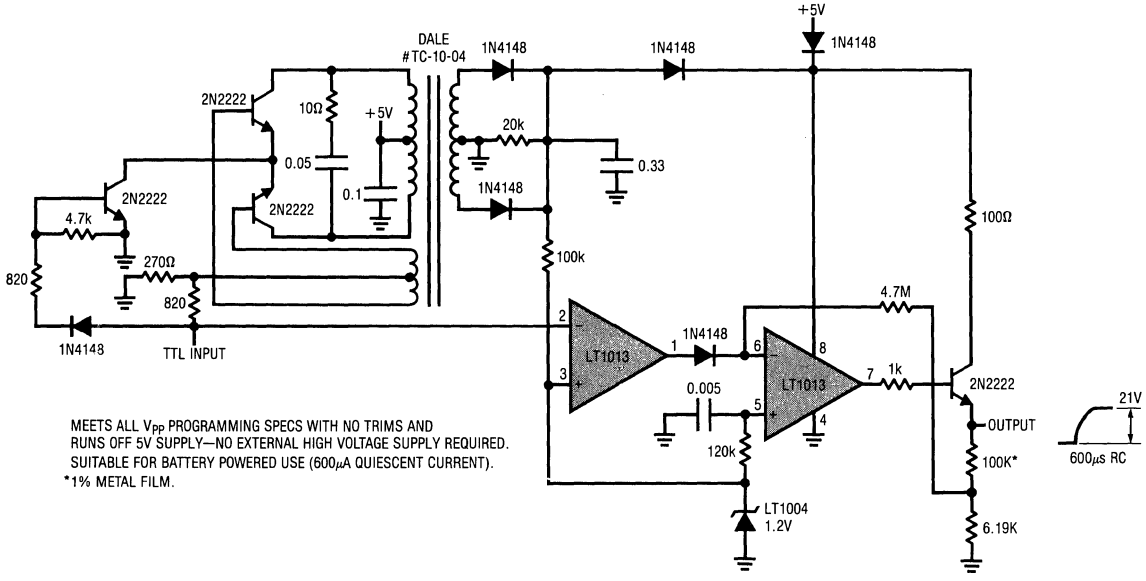
SAMPLED OPERATION GIVES LOW AVERAGE OPERATING CURRENT ≈650μA. 4.7k–0.01μF RC PROTECTS STRAIN BRIDGE FROM LONG TERM DRIFTS DUE TO HIGH ΔV/ΔT STEPS.

TYPICAL APPLICATIONS

5V Powered Motor Speed Controller
No Tachometer Required

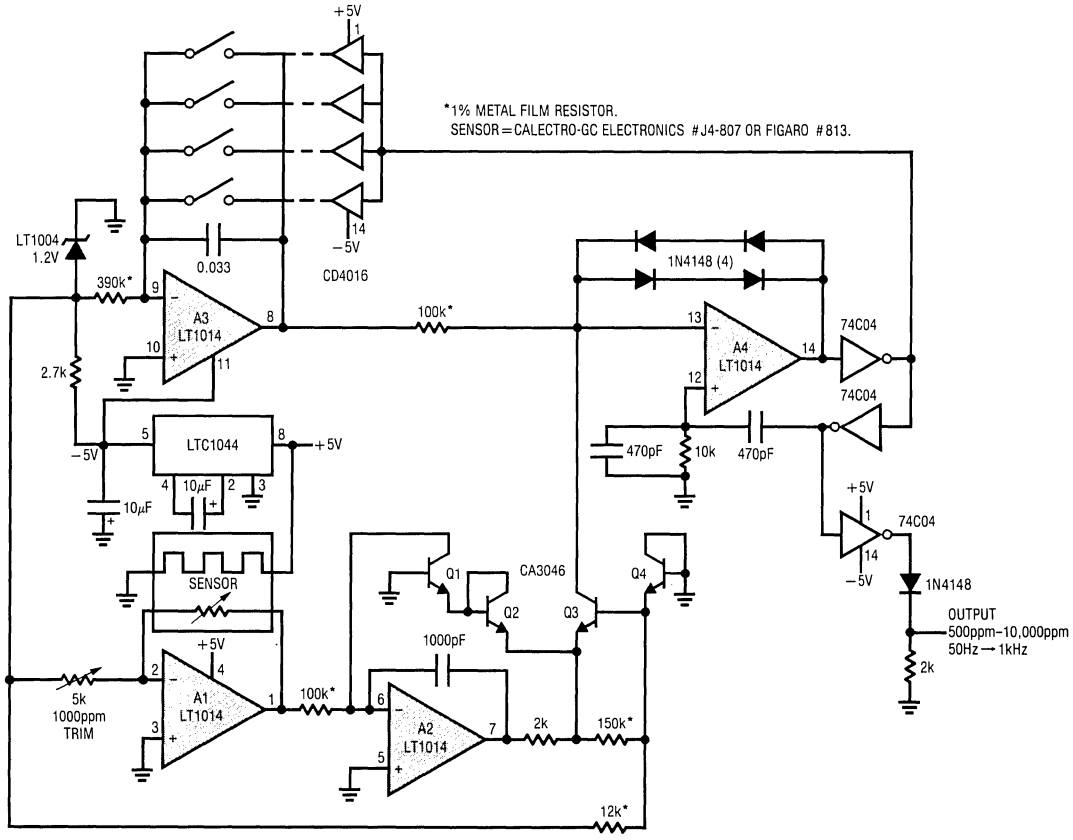


5V Powered EEPROM Pulse Generator

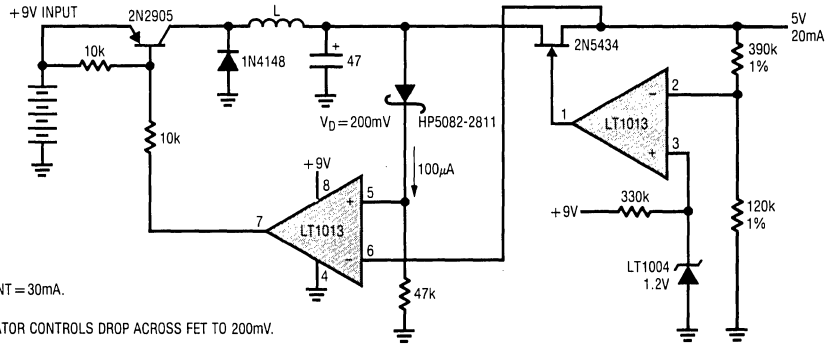


TYPICAL APPLICATIONS

Methane Concentration Detector with Linearized Output



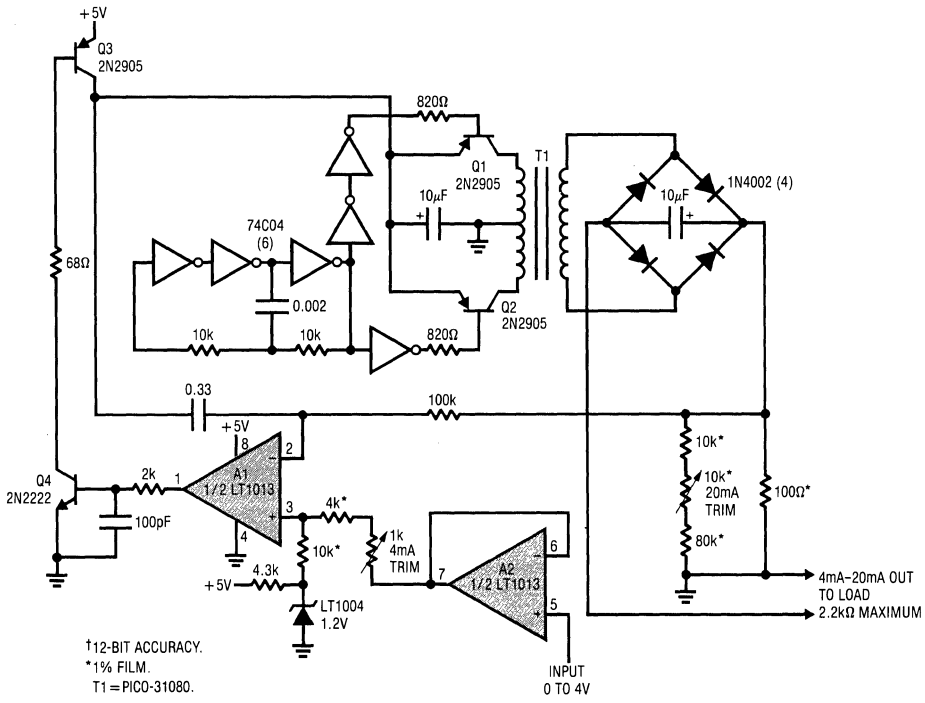
Low Power 9V to 5V Converter



L = DALE TE-3/Q3/TA.
SHORT CIRCUIT CURRENT = 30mA.
≈75% EFFICIENCY.
SWITCHING PREREGULATOR CONTROLS DROP ACROSS FET TO 200mV.

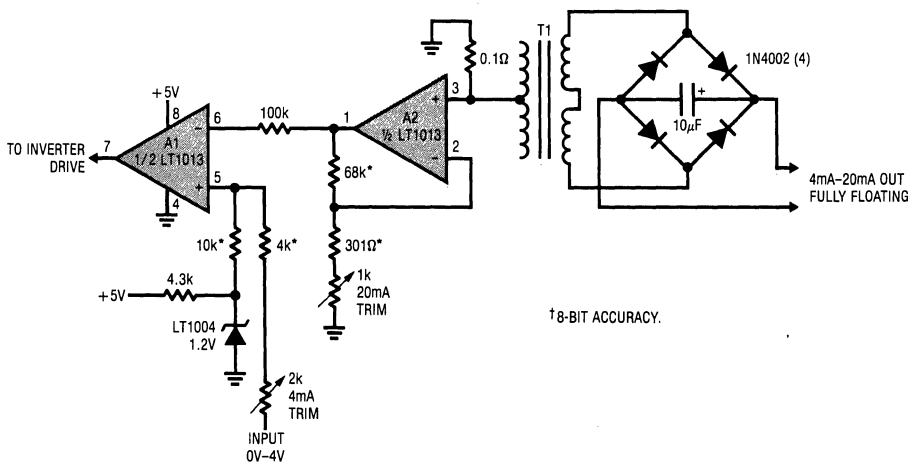
TYPICAL APPLICATIONS

5V Powered 4mA-20mA Current Loop Transmitter †



†12-BIT ACCURACY.
*1% FILM.
T1 = PICO-31080.

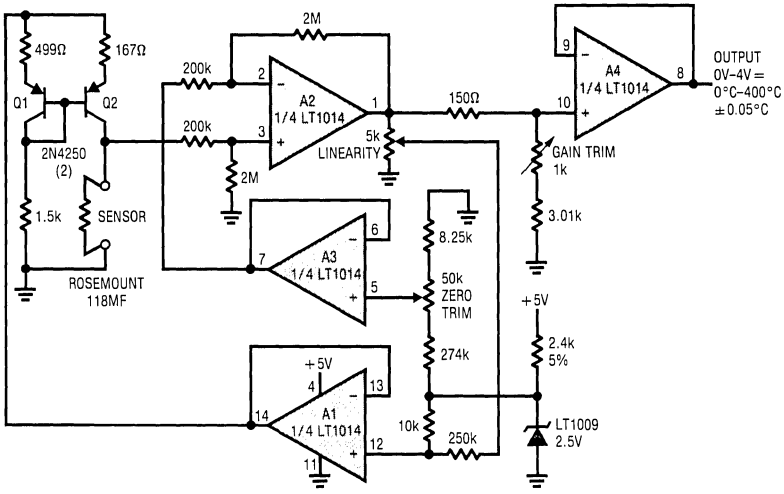
Fully Floating Modification to 4mA-20mA Current Loop †



†8-BIT ACCURACY.

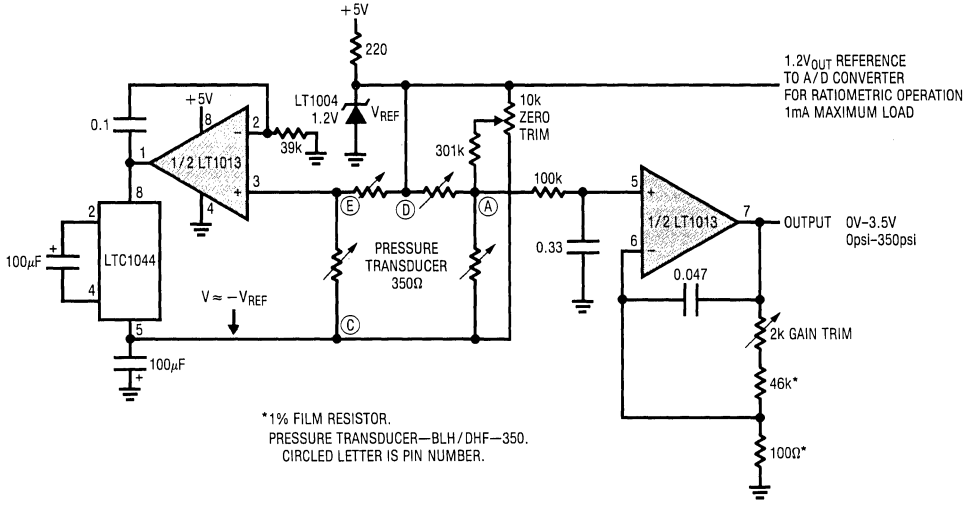
TYPICAL APPLICATIONS

5V Powered, Linearized Platinum RTD Signal Conditioner



ALL RESISTORS ARE TRW-MAR-6 METAL FILM.
RATIO MATCH 2M–200K ±0.01%.
TRIM SEQUENCE:
SET SENSOR TO 0° VALUE.
ADJUST ZERO FOR 0V OUT.
SET SENSOR TO 100°C VALUE.
ADJUST GAIN FOR 1.000V OUT.
SET SENSOR TO 400°C.
ADJUST LINEARITY FOR 4.000V OUT, REPEAT AS REQUIRED.

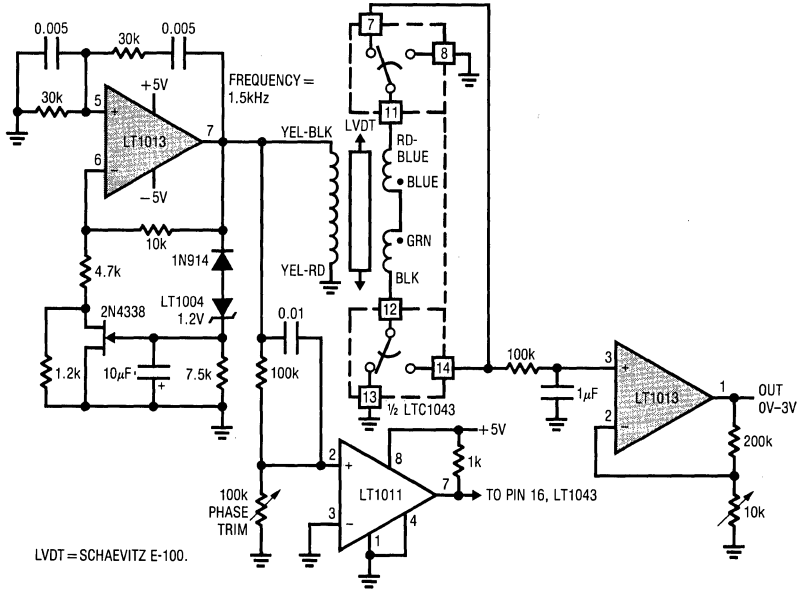
Strain Gage Bridge Signal Conditioner



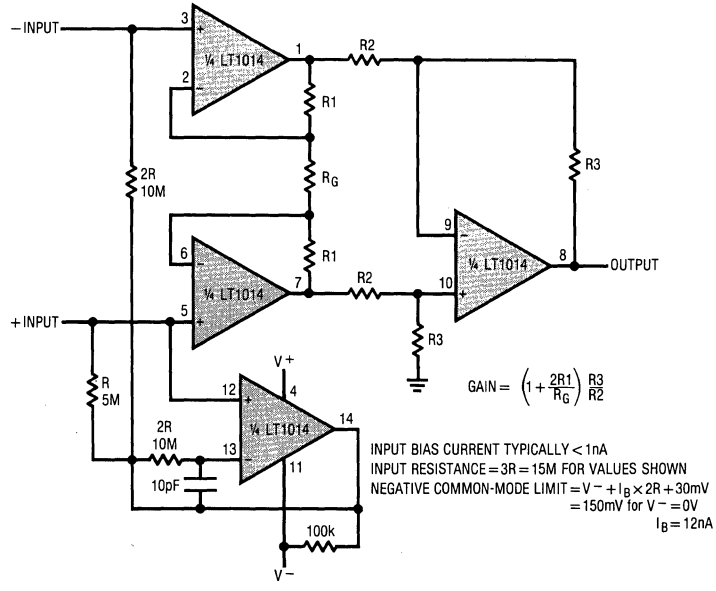
*1% FILM RESISTOR.
PRESSURE TRANSDUCER—BLH/DHF—350.
CIRCLED LETTER IS PIN NUMBER.

TYPICAL APPLICATIONS

LVDT Signal Conditioner

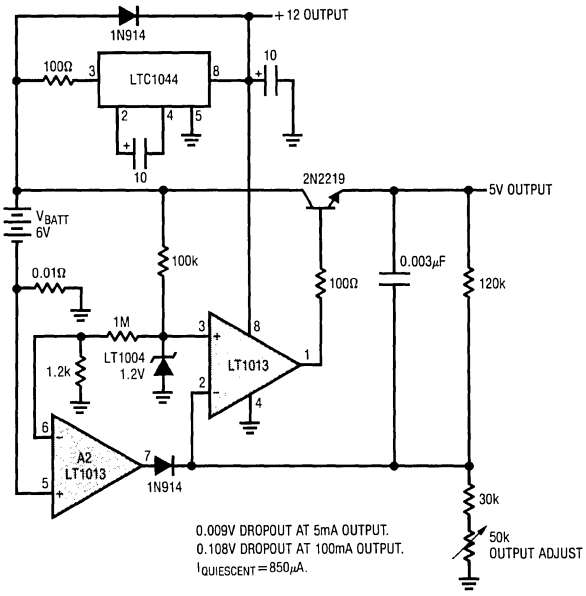


Triple Op Amp Instrumentation Amplifier with Bias Current Cancellation

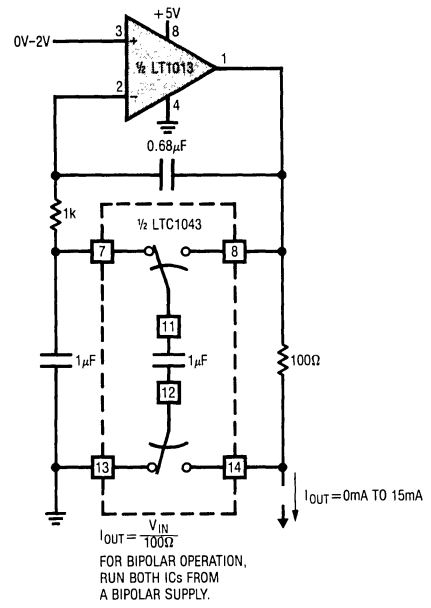


TYPICAL APPLICATIONS

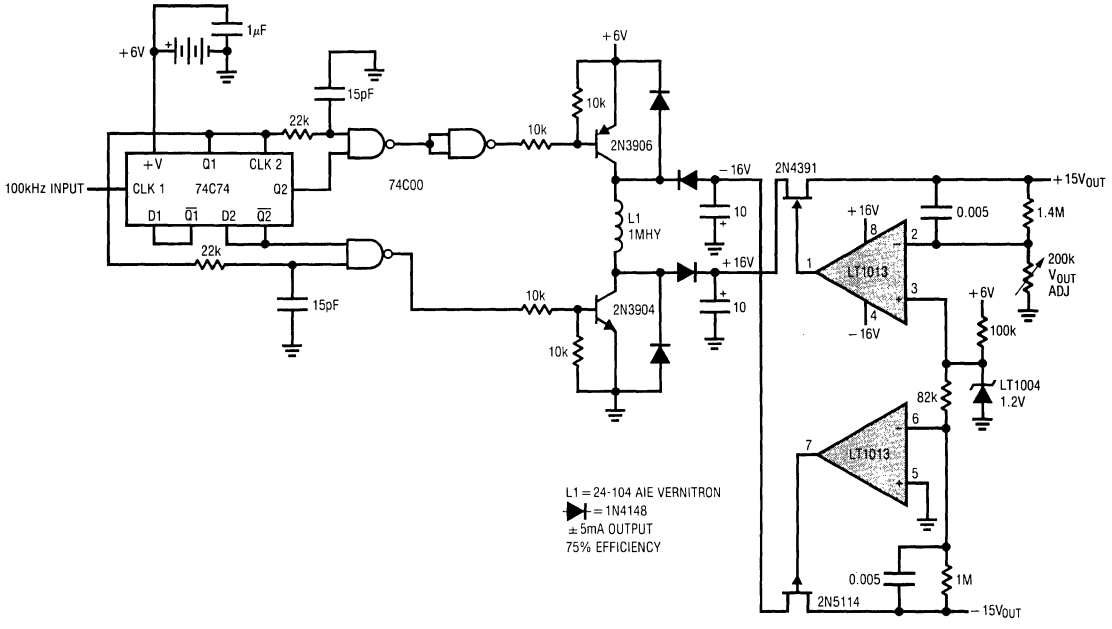
Low Dropout Regulator for 6V Battery



Voltage Controlled Current Source with Ground Referred Input and Output

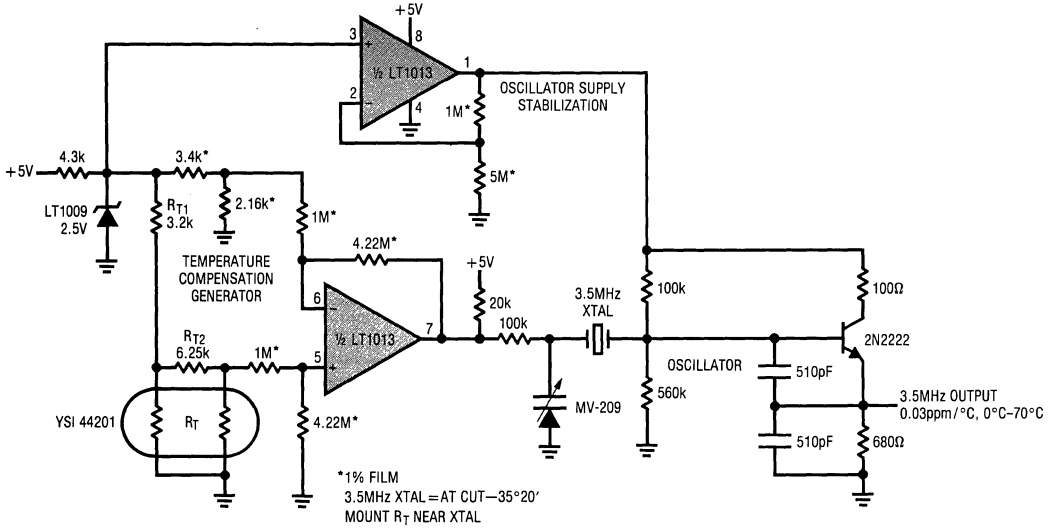


6V to ±15V Regulating Converter



TYPICAL APPLICATIONS

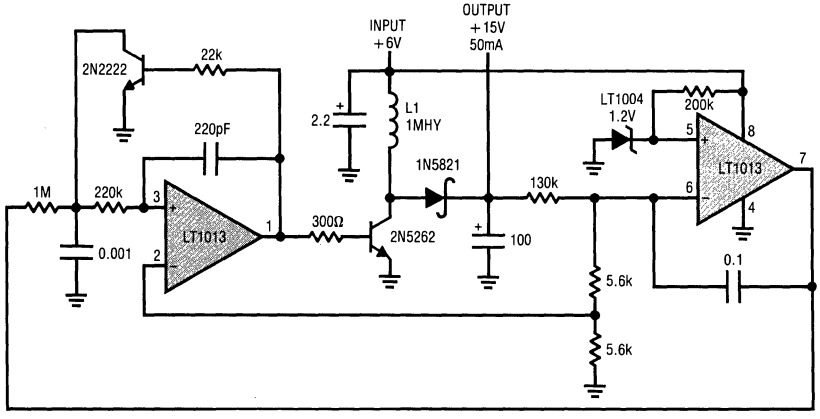
Low Power, 5V Driven, Temperature Compensated Crystal Oscillator (TXCO)†



*1% FILM
3.5MHz XTAL = AT CUT–35°20′
MOUNT R_T NEAR XTAL
3mA POWER DRAIN

†THERMISTOR-AMPLIFIER-VARACTOR NETWORK GENERATES A TEMPERATURE COEFFICIENT OPPOSITE THE CRYSTAL TO MINIMIZE OVERALL OSCILLATOR DRIFT

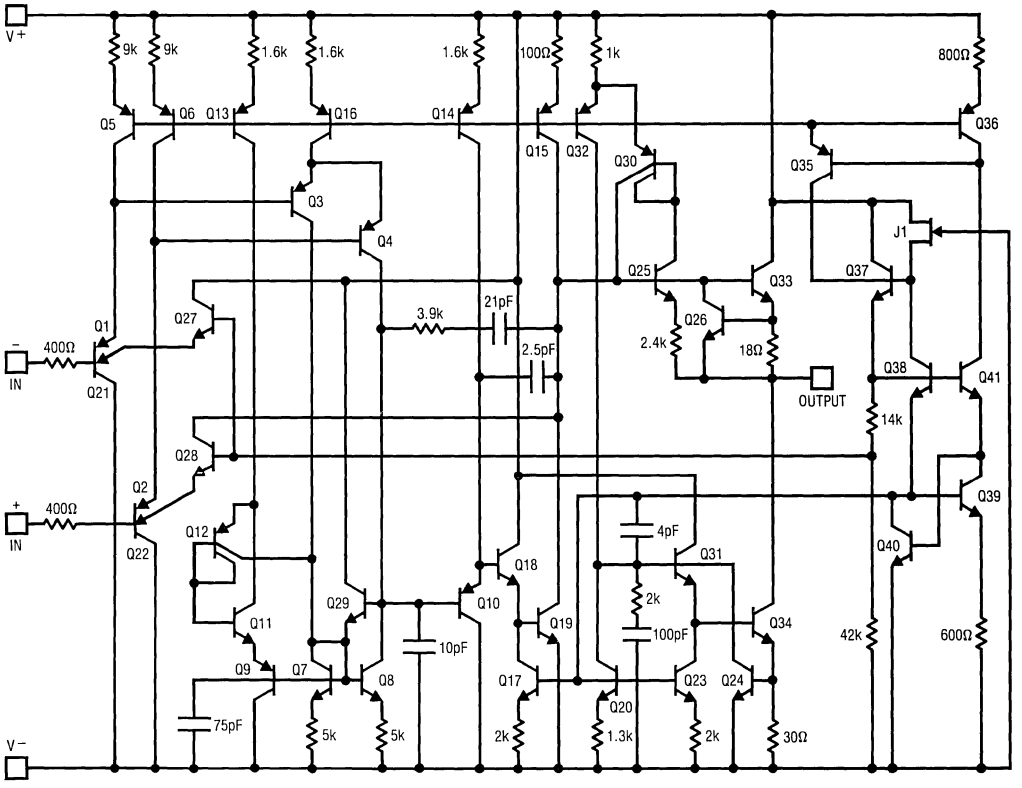
Step-Up Switching Regulator for 6V Battery



L1 = AIE–VERNITRON 24-104
78% EFFICIENCY

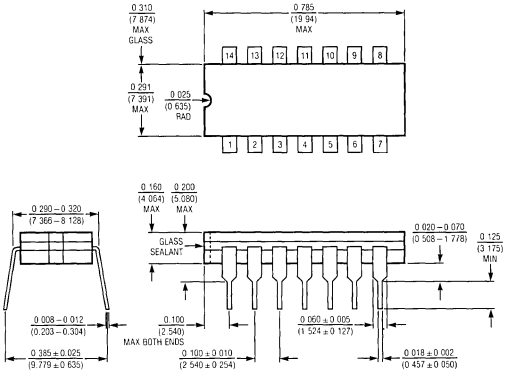
SCHEMATIC DIAGRAM

½ LT1013, ¼ LT1014



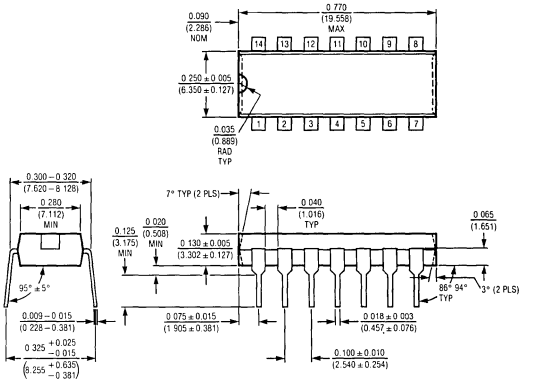
PACKAGE DESCRIPTION

J Package 14 Lead Cavity DIP



$T_j$max	Θ_{jA}
150°C	100°C/W

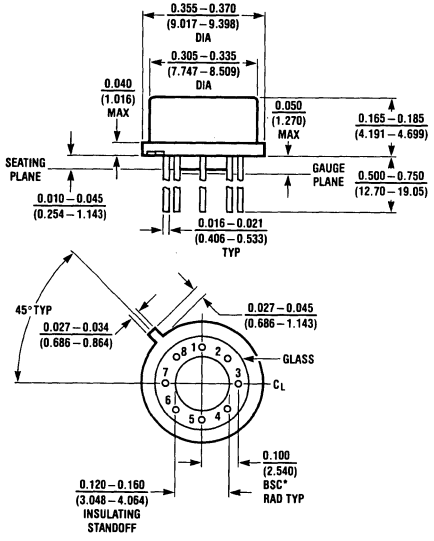
N Package 14 Lead Molded DIP



$T_j$max	Θ_{jA}
100°C	100°C/W

PACKAGE DESCRIPTION

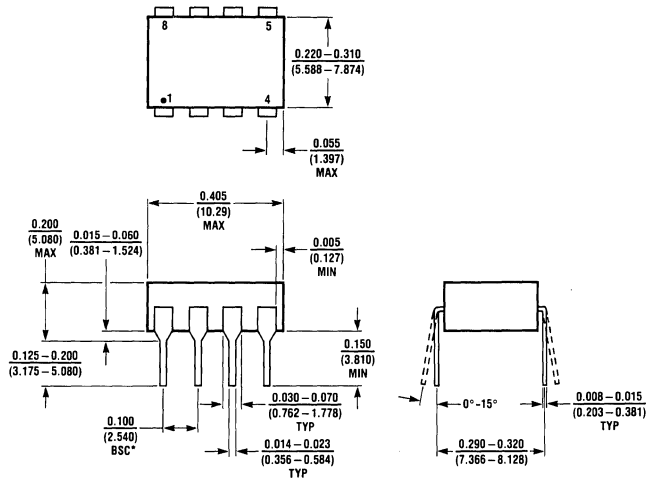
H Package
Metal Can



NOTE: DIMENSIONS IN INCHES (MILLIMETERS)

$T_j$max	θ_{ja}	θ_{jc}
150°C	150°C/W	45°C/W

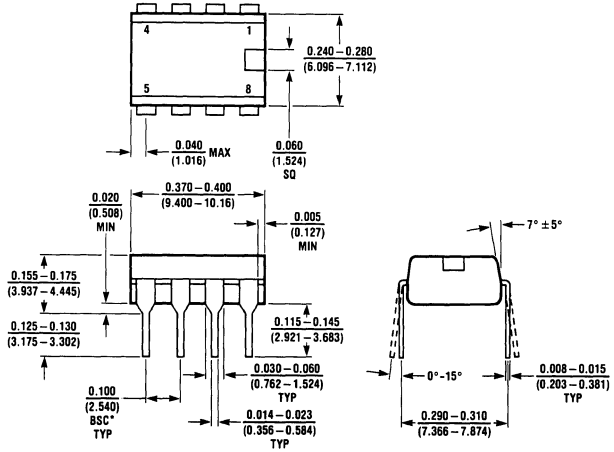
J8 Package
8 Lead Hermetic DIP



NOTE: DIMENSIONS IN INCHES (MILLIMETERS) UNLESS OTHERWISE NOTED
*LEADS WITHIN 0.007 OF TRUE POSITION (TP) AT GAUGE PLANE

$T_j$max	θ_{ja}
150°C	100°C/W

N8 Package
8 Lead Plastic



NOTE: DIMENSIONS IN INCHES UNLESS OTHERWISE NOTED
*LEADS WITHIN 0.007 OF TRUE POSITION (TP) AT GAUGE PLANE

$T_j$max	θ_{ja}
100°C	130°C/W

High Speed, Precision JFET Input Operational Amplifier

FEATURES

■ *Guaranteed* Slew Rate	23V/μs Min.
■ *Guaranteed* Offset Voltage	250μV Max.
−55°C to 125°C	750μV Max.
■ *Guaranteed* Drift	5μV/°C Max.
■ *Guaranteed* Bias Current	
70°C	180pA Max.
125°C	4nA Max.
■ Gain-Bandwidth Product	8.5MHz Typ.
■ Settling Time to 0.05% (10V Step)	0.9μs Typ.

APPLICATIONS

- Fast D/A Output Amplifiers (12, 14, 16 Bits)
- High Speed Instrumentation
- Fast, Precision Sample and Hold
- Voltage-to-Frequency Converters
- Logarithmic Amplifiers

DESCRIPTION

The LT1022 JFET input operational amplifier combines high speed and precision performance.

A 26V/μs slew rate and 8.5MHz gain-bandwidth product are simultaneously achieved with offset voltage of typically 80μV, 1.5μV/°C drift, bias currents of 50pA at 70°C, 500pA at 125°C. The output delivers 20mA of load current without gain degradation.

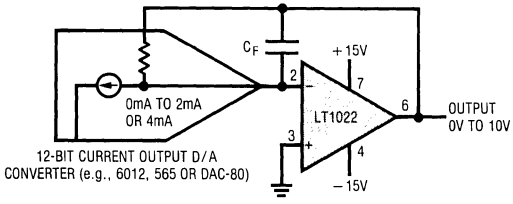
The 250μV maximum offset voltage specification represents less than ½ least significant bit error in a 14-bit, 10V system.

The LT1022A meets or exceeds all OP-16A and OP-16E specifications. It is faster and more accurate without stability problems at cold temperatures.

The LT1022 can be used as the output amplifier for 12-bit current output D/A converters, as shown below.

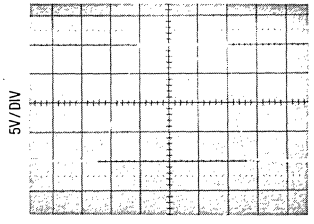
For a more accurate, lower power dissipation, but slower JFET input op amp, please refer to the LT1055 data sheet.

12-Bit Voltage Output D/A Converter



C_F = 15pF TO 33pF
SETTLING TIME TO 2mV (0.8 LSB) = 1.5μs TO 2μs

Large Signal Response

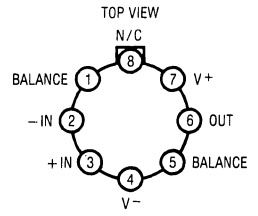


A_V = 1, C_L = 100pF, 0.5μs/DIV
T_A = 25°C, V_S = ±15V

ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... ±20V
Differential Input Voltage ..... ±40V
Input Voltage ..... ±20V
Output Short Circuit Duration ..... Indefinite
Operating Temperature Range
LT1022AM/1022M ..... −55°C to 125°C
LT1022AC/1022C ..... 0°C to 70°C
Storage Temperature Range
All Devices ..... −65°C to 150°C
Lead Temperature (Soldering, 10 sec.) ..... 300°C

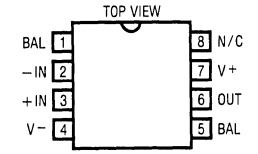
PACKAGE/ORDER INFORMATION



METAL CAN H PACKAGE

ORDER PART NUMBER

LT1022AMH
LT1022MH
LT1022ACH
LT1022CH



PLASTIC DIP N8 PACKAGE

LT1022CN8

ELECTRICAL CHARACTERISTICS

$V_S = \pm 15V$, $T_A = 25°C$, $V_{CM} = 0V$ unless otherwise noted

SYMBOL	PARAMETER	CONDITIONS	LT1022AM LT1022AC MIN	LT1022AM LT1022AC TYP	LT1022AM LT1022AC MAX	LT1022M LT1022CH LT1022CN8 MIN	LT1022M LT1022CH LT1022CN8 TYP	LT1022M LT1022CH LT1022CN8 MAX	UNITS
V_{OS}	Input Offset Voltage (Note 1)	H Package	—	80	250	—	100	600	μV
		N8 Package	—	—	—	—	160	1000	μV
I_{OS}	Input Offset Current	Fully Warmed Up	—	2	10	—	2	20	pA
I_B	Input Bias Current	Fully Warmed Up	—	±10	±50	—	±10	±50	pA
		$V_{CM} = +10V$	—	+30	+100	—	+30	+150	pA
	Input Resistance—Differential		—	10^{12}	—	—	10^{12}	—	Ω
	—Common-Mode	$V_{CM} = -11V$ to $+8V$	—	10^{12}	—	—	10^{12}	—	Ω
		$V_{CM} = +8V$ to $+11V$	—	10^{11}	—	—	10^{11}	—	Ω
	Input Capacitance		—	4	—	—	4	—	pF
e_n	Input Noise Voltage	0.1Hz to 10Hz	—	2.5	—	—	2.8	—	μVp-p
e_n	Input Noise Voltage Density	$f_O = 10Hz$ (Note 2)	—	28	50	—	30	60	nV/√Hz
		$f_O = 1kHz$ (Note 3)	—	14	20	—	15	22	nV/√Hz
i_n	Input Noise Current Density	$f_O = 10Hz$, 1kHz (Note 4)	—	1.8	4	—	1.8	4	fA/√Hz
A_{VOL}	Large Signal Voltage Gain	$V_O = \pm 10V$ $R_L = 2k$	150	400	—	120	400	—	V/mV
		$R_L = 1k$	130	300	—	100	300	—	V/mV
	Input Voltage Range		±10.5	±12	—	±10.5	±12	—	V
CMRR	Common-Mode Rejection Ratio	$V_{CM} = \pm 10.5V$	86	94	—	82	92	—	dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 10V$ to $\pm 18V$	88	104	—	86	102	—	dB
V_{OUT}	Output Voltage Swing	$R_L = 2k$	±12	±13.2	—	±12	±13.2	—	V
SR	Slew Rate		23	26	—	18	24	—	V/μs
GBW	Gain-Bandwidth Product	$f = 1MHz$	—	8.5	—	—	8.0	—	MHz
I_S	Supply Current		—	5.2	7.0	—	5.2	7.0	mA
	Settling Time	$A = +1$ or $A = -1$							
		10V Step to 0.05%	—	0.9	—	—	0.9	—	μs
		10V Step to 0.02%	—	1.3	—	—	1.3	—	μs
	Offset Voltage Adjustment Range	$R_{POT} = 100k$	—	±7	—	—	±7	—	mV

ELECTRICAL CHARACTERISTICS $V_S = \pm 15V$, $V_{CM} = 0V$, $0°C \leq T_A \leq 70°C$ unless otherwise noted

SYMBOL	PARAMETER	CONDITIONS		LT1022AC MIN	LT1022AC TYP	LT1022AC MAX	LT1022CH LT1022CN8 MIN	LT1022CH LT1022CN8 TYP	LT1022CH LT1022CN8 MAX	UNITS
V_{OS}	Input Offset Voltage (Note 1)	H Package	●	—	140	480	—	180	1000	μV
		N8 Package	●	—	—	—	—	300	1700	μV
	Average Temperature Coefficient of Input Offset Voltage	H Package	●	—	1.3	5.0	—	1.8	9.0	μV/°C
		N8 Package (Note 5)	●	—	—	—	—	3.0	15.0	μV/°C
I_{OS}	Input Offset Current	Warmed Up, $T_A = 70°C$	●	—	15	80	—	18	100	pA
I_B	Input Bias Current	Warmed Up, $T_A = 70°C$	●	—	±50	±200	—	±60	±250	pA
A_{VOL}	Large Signal Voltage Gain	$V_O = \pm 10V$, $R_L = 2k$	●	80	250	—	60	250	—	V/mV
CMRR	Common-Mode Rejection Ratio	$V_{CM} = \pm 10.4V$	●	85	93	—	80	91	—	dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 10V$ to $\pm 18V$	●	86	103	—	84	101	—	dB
V_{OUT}	Output Voltage Swing	$R_L = 2k$	●	±12	±13.1	—	±12	±13.1	—	V

ELECTRICAL CHARACTERISTICS $V_S = \pm 15V$, $V_{CM} = 0V$, $-55°C \leq T_A \leq 125°C$ unless otherwise noted

SYMBOL	PARAMETER	CONDITIONS		LT1022AM MIN	LT1022AM TYP	LT1022AM MAX	LT1022M MIN	LT1022M TYP	LT1022M MAX	UNITS
V_{OS}	Input Offset Voltage	(Note 1)	●	—	230	750	—	300	1500	μV
	Average Temperature Coefficient of Input Offset Voltage	(Note 5)	●	—	1.5	5.0	—	2.0	9.0	μV/°C
I_{OS}	Input Offset Current	Warmed Up, $T_A = 125°C$	●	—	0.3	2.0	—	0.30	3.0	nA
I_B	Input Bias Current	Warmed Up, $T_A = 125°C$	●	—	±0.5	±4.0	—	±0.7	±6.0	nA
A_{VOL}	Large Signal Voltage Gain	$V_O = \pm 10V$, $R_L = 2k$	●	40	120	—	35	120	—	V/mV
CMRR	Common-Mode Rejection Ratio	$V_{CM} = \pm 10.4V$	●	85	92	—	80	90	—	dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 10V$ to $\pm 17V$	●	86	102	—	84	100	—	dB
V_{OUT}	Output Voltage Swing	$R_L = 2k$	●	±12	±12.9	—	±12	±12.9	—	V

The ● denotes the specifications which apply over the full operating temperature range.

Note 1: Offset voltage is measured under two different conditions:
(a) approximately 0.5 seconds after application of power;
(b) at $T_A = 25°C$, with the chip self-heated to approximately 45°C to account for chip temperature rise when the device is fully warmed up.

Note 2: 10Hz noise voltage density is sample tested on every lot of A grades. Devices 100% tested at 10Hz are available on request.

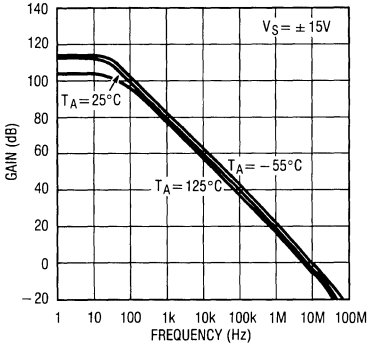
Note 3: This parameter is tested on a sample basis only.

Note 4: Current noise is calculated from the formula: $i_n = (2qI_B)^{1/2}$, where $q = 1.6 \times 10^{-19}$ coulomb. The noise of source resistors up to 1GΩ swamps the contribution of current noise.

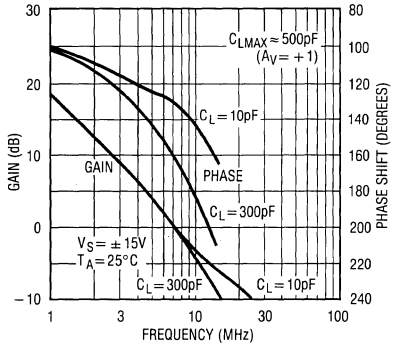
Note 5: Offset voltage drift with temperature is practically unchanged when the offset voltage is trimmed to zero with a 100k potentiometer between the balance terminals and the wiper tied to V^+. Devices tested to tighter drift specifications are available on request.

TYPICAL PERFORMANCE CHARACTERISTICS

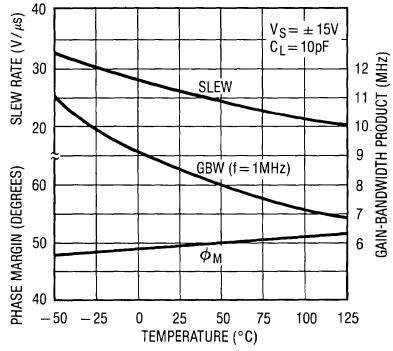
Gain vs Frequency



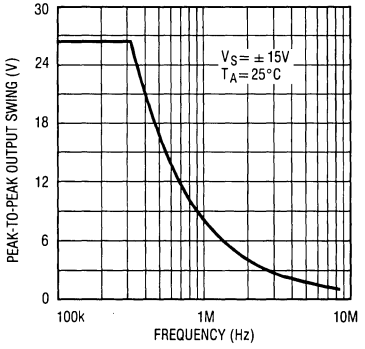
Gain, Phase Shift vs Frequency



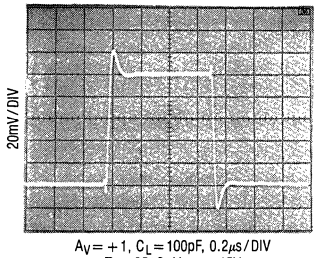
Phase Margin, Gain Bandwidth Product, Slew Rate vs Temperature



Undistorted Output Swing vs Frequency

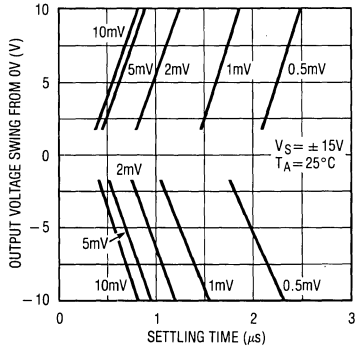


Small Signal Response



$A_V = +1$, $C_L = 100pF$, $0.2\mu s$/DIV
$T_A = 25°C$, $V_S = \pm 15V$

Settling Time



The typical behavior of many LT1022 parameters is identical to the LT1056. Please refer to the LT1055/1056 data sheet for the following typical performance characteristics:

- **Input Bias and Offset Currents vs Temperature**
- **Input Bias Current Over the Common-Mode Range**
- **Distribution of Input Offset Voltage (H and N8 Package)**
- **Distribution of Offset Voltage Drift with Temperature**
- **Warm-Up Drift**
- **Long Term Drift of Representative Units**
- **0.1Hz to 10Hz Noise**
- **Voltage Noise vs Frequency**
- **Noise vs Chip Temperature**
- **Output Impedance vs Frequency**
- **Common-Mode Range vs Temperature**
- **Common-Mode and Power Supply Rejections vs Temperature**
- **Common-Mode Rejection Ratio vs Frequency**
- **Power Supply Rejection Ratio vs Frequency**
- **Voltage Gain vs Temperature**
- **Supply Current vs Supply Voltage**
- **Output Swing vs Load Resistance**
- **Short Circuit Current vs Time**

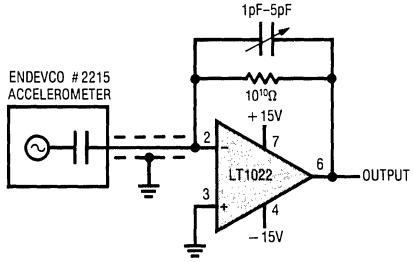
APPLICATIONS INFORMATION

The LT1056 applications information is directly applicable to the LT1022. Please consult the LT1055/1056 data sheet for details on:

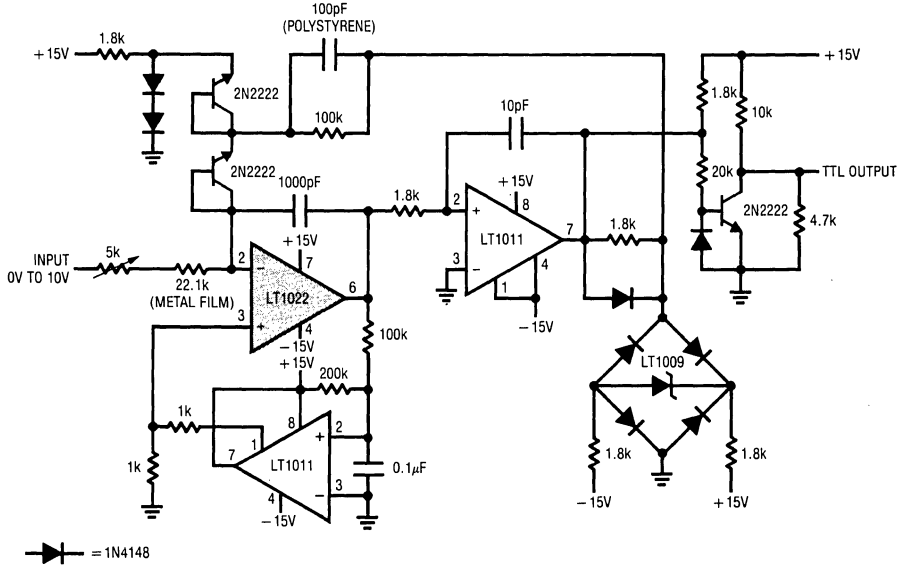
(1) plug-in compatibility to industry standard devices
(2) offset nulling
(3) achieving picoampere/microvolt performance
(4) phase-reversal protection
(5) high speed operation (including settling time test circuit)
(6) noise performance
(7) simplified circuit schematic.

TYPICAL APPLICATIONS

Fast Piezoelectric Accelerometer

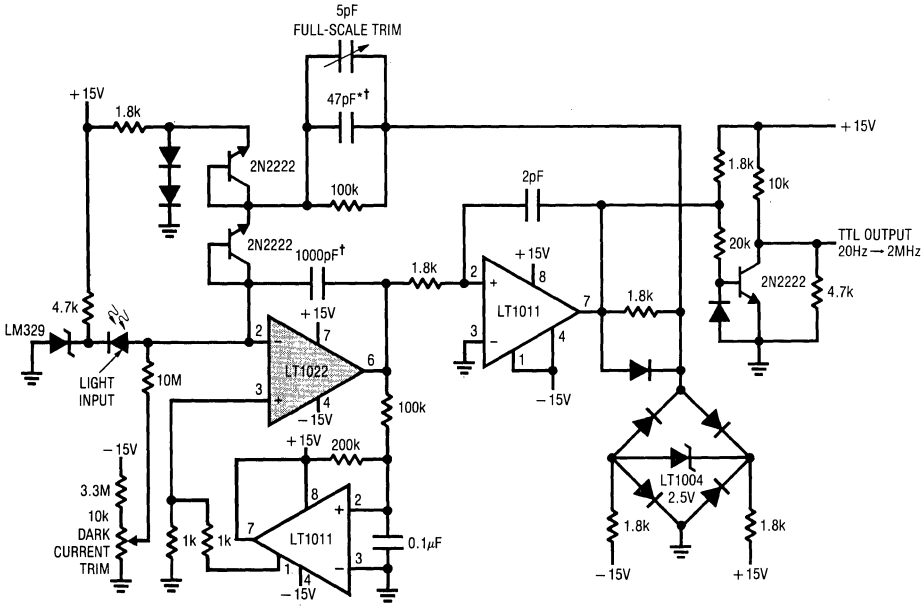


10Hz to 1MHz Voltage-to-Frequency Converter



TYPICAL APPLICATIONS

PIN Photodiode-to-Frequency Converter



SCALE FACTOR =
1nW/Hz AT 900 NANOMETERS FROM 20nW TO 2mW

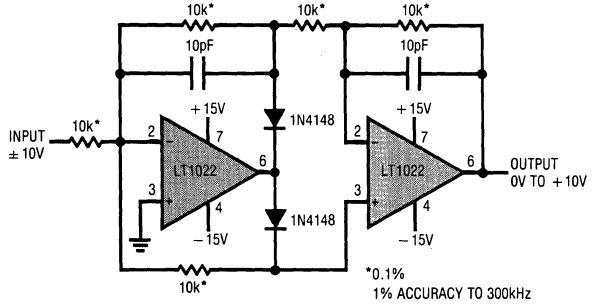
= HEWLETT PACKARD PHOTODIODE HP5082-4204

= 1N4148

†POLYSTYRENE

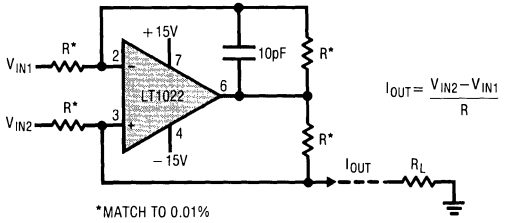
*SELECT VALUE FOR 2mW IN = 2MHz OUT.

Wide Bandwidth Absolute Value Circuit



*0.1%
1% ACCURACY TO 300kHz
5% ACCURACY TO 700kHz

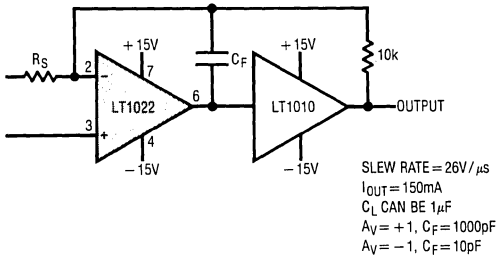
Fast, Differential Input Current Source



*MATCH TO 0.01%
FULL-SCALE POWER BANDWIDTH
= 1MHz FOR $I_{OUT}R$ = 8Vp-p
= 400kHz FOR $I_{OUT}R$ = 20Vp-p
MAXIMUM I_{OUT} = 10mAp-p
COMMON-MODE VOLTAGE AT LT1022 INPUT = $\frac{I_{OUTp\text{-}p} \times R_L}{2}$

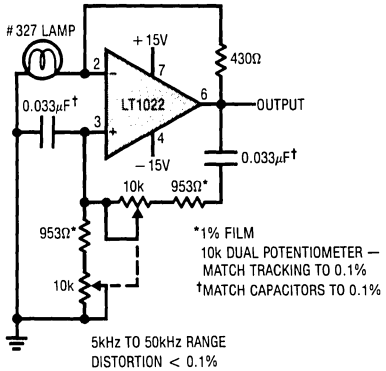
TYPICAL APPLICATIONS

High Output Current Op Amp



SLEW RATE = 26V/μs
I_{OUT} = 150mA
C_L CAN BE 1μF
A_V = +1, C_F = 1000pF
A_V = −1, C_F = 10pF

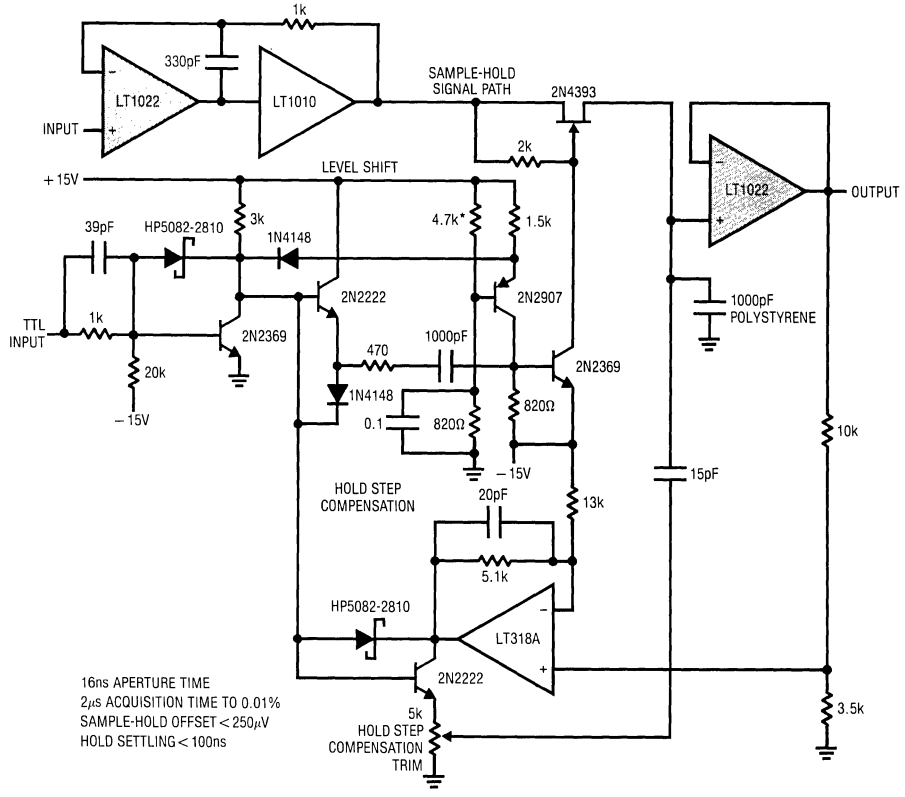
Low Distortion Sine Wave Oscillator



*1% FILM
10k DUAL POTENTIOMETER — MATCH TRACKING TO 0.1%
†MATCH CAPACITORS TO 0.1%

5kHz TO 50kHz RANGE
DISTORTION < 0.1%
AMPLITUDE = 18Vp-p.

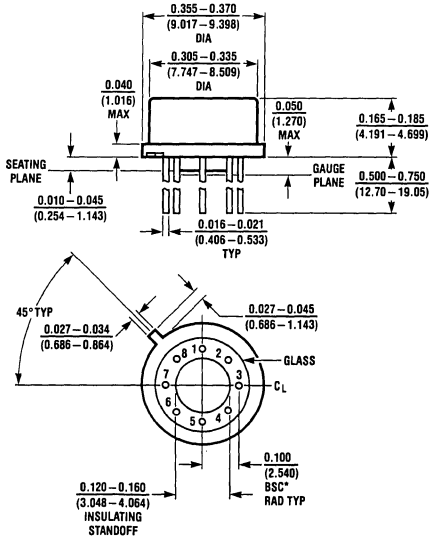
Fast, Precision Sample-Hold



16ns APERTURE TIME
2μs ACQUISITION TIME TO 0.01%
SAMPLE-HOLD OFFSET < 250μV
HOLD SETTLING < 100ns

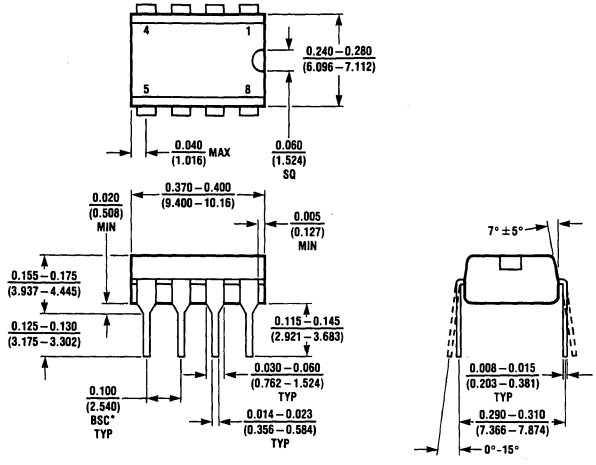
PACKAGE DESCRIPTION Dimensions in inches (millimeters) unless otherwise noted.

H Package
Metal Can



$T_j$max	θ_{ja}	θ_{jc}
150°C	150°C/W	45°C/W

N8 Package
8 Lead Plastic



*LEADS WITHIN 0.007 OF TRUE POSITION (TP) AT GAUGE PLANE

$T_j$max	θ_{ja}
100°C	130°C/W

Dual, Matched Picoampere, Microvolt Input, Low Noise Op Amp

FEATURES

- *Guaranteed* Offset Voltage 50μV Max.
- *Guaranteed* Bias Current
  - 25°C 120pA Max.
  - −55°C to 125°C 700pA Max.
- *Guaranteed* Drift 1.5μV/°C Max.
- Low Noise, 0.1Hz to 10Hz 0.5μVp-p
- *Guaranteed* Supply Current 600μA Max.
- *Guaranteed* CMRR 112dB Min.
- *Guaranteed* PSRR 112dB Min.
- *Guaranteed* Voltage Gain with 5mA Load Current
- *Guaranteed* Matching Characteristics

APPLICATIONS

- Strain Gauge Signal Conditioner
- Dual Limit Precision Threshold Detection
- Charge Integrators
- Wide Dynamic Range Logarithmic Amplifiers
- Light Meters
- Low Frequency Active Filters
- Standard Cell Buffers
- Thermocouple Amplifiers

DESCRIPTION

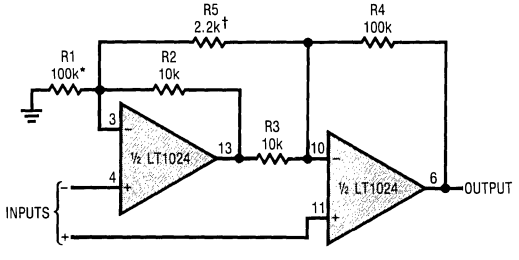
The LT1024 dual, matched internally compensated universal precision operational amplifier can be used in practically all precision applications requiring multiple op amps. The LT1024 combines picoampere bias currents (which are maintained over the full −55°C to 125°C temperature range), microvolt offset voltage (and low drift with time and temperature), low voltage and current noise, and low power dissipation. Extremely high common-mode and power supply rejection ratios, practically immeasurable warm-up drift, and the ability to deliver 5mA load current with a voltage gain of a million round out the LT1024's superb precision specifications.

Tight matching is guaranteed on offset voltage, noninverting bias currents and common-mode and power supply rejections.

The all-around excellence of the LT1024 eliminates the necessity of the time-consuming error analysis procedure of precision system design in many dual applications; the LT1024 can be stocked as the universal dual op amp in the 14-pin DIP configuration.

For a single op amp with similar specifications, see the LT1012 data sheet; for a single supply dual precision op amp in the 8-pin configuration, see the LT1013 data sheet.

Two Op Amp Instrumentation Amplifier

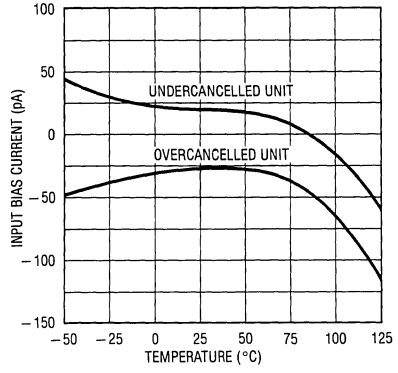


$$GAIN = \frac{R4}{R3}\left[1+\frac{1}{2}\left(\frac{R2}{R1}+\frac{R3}{R4}\right)+\frac{R2+R3}{R5}\right] \approx 100$$

*TRIM FOR COMMON-MODE REJECTION
†TRIM FOR GAIN

TYPICAL PERFORMANCE:
OFFSET VOLTAGE = 20μV
BIAS CURRENT = ±30pA
OFFSET CURRENT = 30pA

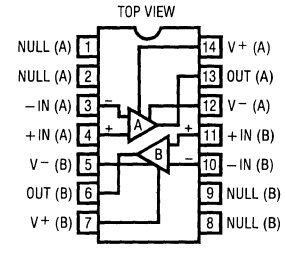
Input Bias Current vs Temperature



ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... ±20V
Differential Input Current (Note 1) ..... ±10mA
Input Voltage ..... ±20V
Output Short Circuit Duration ..... Indefinite
Operating Temperature Range
LT1024AM/LT1024M ..... −55°C to 125°C
LT1024AC/LT1024C ..... 0°C to 70°C
Storage Temperature Range
All Devices ..... −65°C to 150°C
Lead Temperature (Soldering, 10 sec.)..... 300°C

PACKAGE/ORDER INFORMATION



D PACKAGE
14 PIN HERMETIC
(SIDEBRAZED)

N PACKAGE
14 PIN PLASTIC

NOTE: DEVICE MAY BE OPERATED EVEN IF INSERTION IS REVERSED; THIS IS DUE TO INHERENT SYMMETRY OF PIN LOCATIONS OF AMPLIFIERS A AND B (NOTE 2).

ORDER PART NUMBER

LT1024AMD
LT1024MD
LT1024ACN
LT1024CN

ELECTRICAL CHARACTERISTICS $V_S = \pm 15V$, $V_{CM} = 0V$, $T_A = 25°C$ unless otherwise noted

Individual Amplifiers

SYMBOL	PARAMETER	CONDITIONS	LT1024AM/LT1024AC MIN	LT1024AM/LT1024AC TYP	LT1024AM/LT1024AC MAX	LT1024M/LT1024C MIN	LT1024M/LT1024C TYP	LT1024M/LT1024C MAX	UNITS
V_{OS}	Input Offset Voltage			15	50		20	100	μV
	Long Term Input Offset Voltage Stability			0.3			0.3		μV/month
I_{OS}	Input Offset Current			20	100		25	180	pA
I_B	Input Bias Current			±25	±120		±30	±200	pA
e_n	Input Noise Voltage	0.1Hz to 10Hz		0.5			0.5		μVp-p
e_n	Input Noise Voltage Density	$f_O = 10Hz$ (Note 3) $f_O = 1000Hz$ (Note 3)		17 14	33 24		17 14	33 24	nV/√Hz nV/√Hz
i_n	Input Noise Current Density	$f_O = 10Hz$		20			20		fA/√Hz
A_{VOL}	Large Signal Voltage Gain	$V_{OUT} = \pm 12V$, $R_L \geq 10k\Omega$ $V_{OUT} = \pm 10V$, $R_L \geq 2k\Omega$	250 150	2000 1000		180 100	2000 1000		V/mV V/mV
CMRR	Common-Mode Rejection Ratio	$V_{CM} = \pm 13.5V$	112	132		108	132		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 2V$ to $\pm 20V$	112	132		108	132		dB
	Input Voltage Range		±13.5	±14.0		±13.5	±14.0		V
V_{OUT}	Output Voltage Swing	$R_L = 10k\Omega$	±13	±14		±13	±14		V
	Slew Rate		0.1	0.2		0.1	0.2		V/μs
I_S	Supply Current per Amplifier			380	600		380	700	μA

Matching Specifications

SYMBOL	PARAMETER	CONDITIONS	LT1024AM/LT1024AC MIN	LT1024AM/LT1024AC TYP	LT1024AM/LT1024AC MAX	LT1024M/LT1024C MIN	LT1024M/LT1024C TYP	LT1024M/LT1024C MAX	UNITS
	Input Offset Voltage Match		—	20	75	—	25	150	μV
I_B^+	Average Non-Inverting Bias Current		—	±30	±150	—	±40	±250	pA
I_{OS}^+	Non-Inverting Offset Current		—	30	150	—	30	300	pA
ΔCMRR	Common Mode Rejection Ratio Match	$V_{CM} = \pm 13.5V$	110	132	—	106	132	—	dB
ΔPSRR	Power Supply Rejection Ratio Match	$V_S = \pm 2V$ to $20V$	110	132	—	106	132	—	dB
	Channel Separation	$f \leq 10Hz$ (Note 3)	134	150	—	134	150	—	dB

ELECTRICAL CHARACTERISTICS

$V_S = \pm 15V$, $V_{CM} = 0V$, $0°C \le T_A \le 70°C$ for the LT1024AC and LT1024C; $-55°C \le T_A \le 125°C$ for the LT1024AM and LT1024M unless otherwise noted

Individual Amplifiers

SYMBOL	PARAMETER	CONDITIONS		LT1024AM/LT1024AC MIN	LT1024AM/LT1024AC TYP	LT1024AM/LT1024AC MAX	LT1024M/LT1024C MIN	LT1024M/LT1024C TYP	LT1024M/LT1024C MAX	UNITS
V_{OS}	Input Offset Voltage	0°C to 70°C	●		30	120		35	200	μV
		−55°C to 125°C	●		40	200		50	300	μV
	Average Temperature Coefficient of Input Offset Voltage		●		0.25	1.5		0.3	2.0	μV/°C
I_{OS}	Input Offset Current	0°C to 70°C	●		40	250		50	300	pA
		−55°C to 125°C	●		80	350		100	500	pA
	Average Temperature Coefficient of Input Offset Current		●		0.5	2.5		0.7	3	pA/°C
I_B	Input Bias Current	0°C to 70°C	●		±40	±250		±50	±400	pA
		−55°C to 125°C	●		±100	±700		±200	±1300	pA
	Average Temperature Coefficient of Input Bias Current	0°C to 70°C	●		0.4	3		0.5	4	pA/°C
		−55°C to 125°C	●		1	6		2	12	pA/°C
A_{VOL}	Large Signal Voltage Gain	$V_{OUT} = \pm 12V$, $R_L \ge 10k\Omega$	●	150	1000		150	1000		V/mV
		$V_{OUT} = \pm 10V$, $R_L \ge 2k\Omega$	●	100	600		100	600		V/mV
CMRR	Common-Mode Rejection Ratio	$V_{CM} = \pm 13.5V$	●	108	128		106	128		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 2.5V$ to $\pm 18V$	●	108	128		106	128		dB
	Input Voltage Range		●	±13.5			±13.5			V
V_{OUT}	Output Voltage Swing	$R_L = 10k\Omega$	●	±13	±14		±13	±14		V
I_S	Supply Current		●		400	800		400	900	μA

Matching Specifications

SYMBOL	PARAMETER	CONDITIONS		LT1024AM/LT1024AC MIN	LT1024AM/LT1024AC TYP	LT1024AM/LT1024AC MAX	LT1024M/LT1024C MIN	LT1024M/LT1024C TYP	LT1024M/LT1024C MAX	UNITS
	Input Offset Voltage Match	0°C to 70°C	●		35	170		45	300	μV
		−55°C to 125°C	●	—	50	280	—	70	500	μV
	Input Offset Voltage Tracking		●	—	0.3	2.0	—	0.4	3.5	μV/°C
I_B^+	Average Non-Inverting Bias Current	0°C to 70°C	●		±40	±300		±50	±500	pA
		−55°C to 125°C	●	—	±100	±800	—	±200	±1400	pA
I_{OS}^+	Non-Inverting Offset Current	0°C to 70°C	●	—	40	300	—	50	500	pA
		−55°C to 125°C	●	—	80	800	—	150	1500	pA
ΔCMRR	Common-Mode Rejection Ratio Match	$V_{CM} = \pm 13.5V$	●	106	128	—	104	128	—	dB
ΔPSRR	Power Supply Rejection Ratio Match	$V_S = \pm 2.5V$ to $\pm 18V$	●	106	128	—	104	128	—	dB

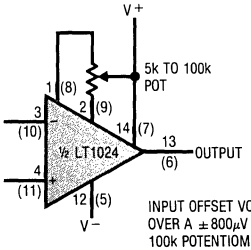
The ● denotes the specifications which apply over the full operating temperature range.

Note 1: Differential input voltages greater than 1V will cause excessive current to flow through the input protection diodes unless limiting resistance is used.

Note 2: The V^+ supply terminals are completely independent and may be powered by separate supplies if desired (this approach, however, would sacrifice the advantages of the power supply rejection ratio matching). The V^- supply terminals are both connected to the common substrate and must be tied to the same voltage. Both V^- pins should be used.

Note 3: This parameter is tested on a sample basis only.

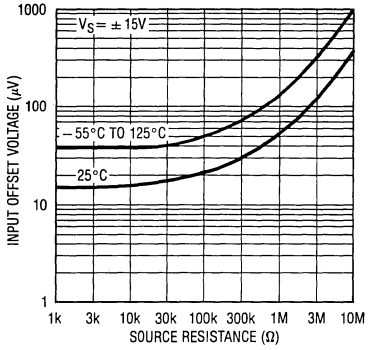
Optional Offset Nulling Circuit



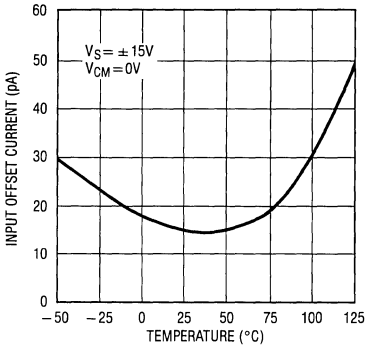
INPUT OFFSET VOLTAGE CAN BE ADJUSTED OVER A ±800μV RANGE WITH A 5k TO 100k POTENTIOMETER.

TYPICAL PERFORMANCE CHARACTERISTICS

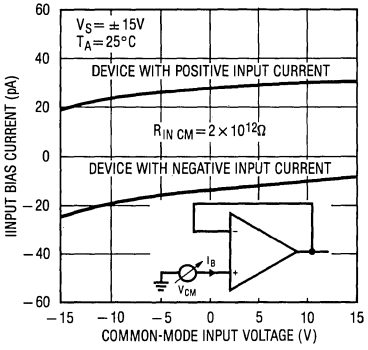
Offset Voltage vs Source Resistance (Balanced or Unbalanced)



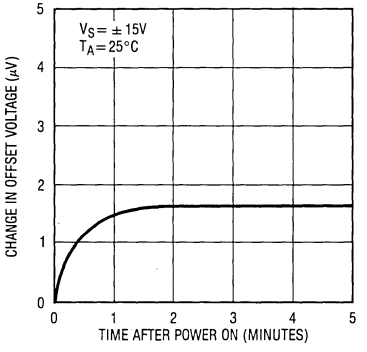
Input Offset Current vs Temperature



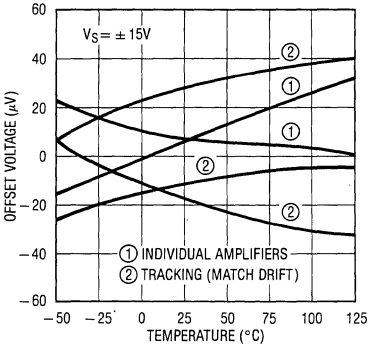
Input Bias Current Over Common-Mode Range



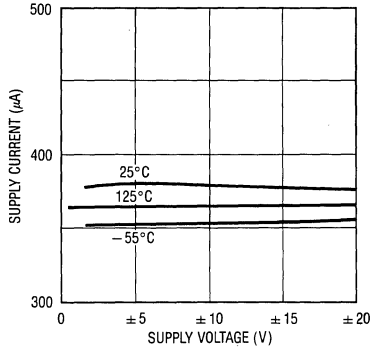
Warm-Up Drift



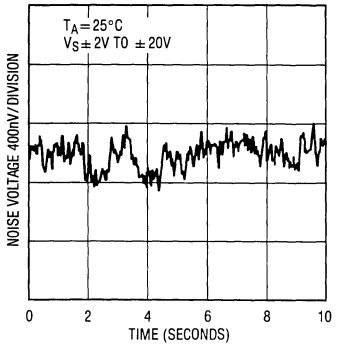
Offset Voltage Drift and Tracking with Temperature of Representative Units



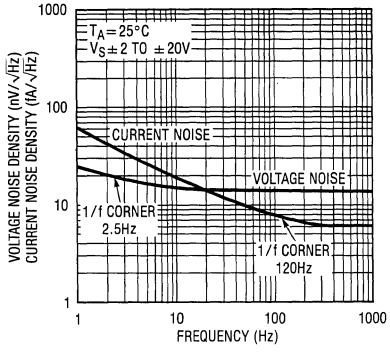
Supply Current vs Supply Voltage per Amplifier



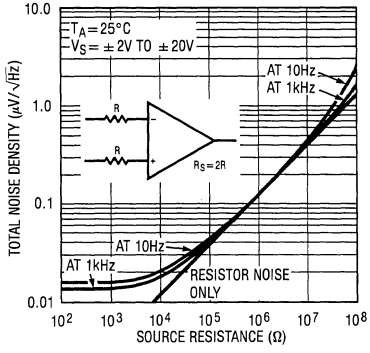
0.1Hz to 10Hz Noise



Noise Spectrum

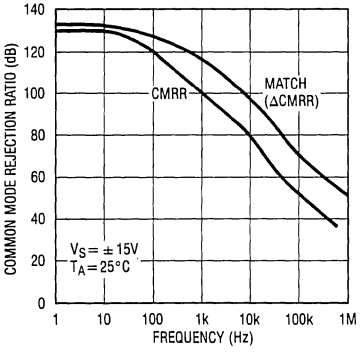


Total Noise vs Source Resistance

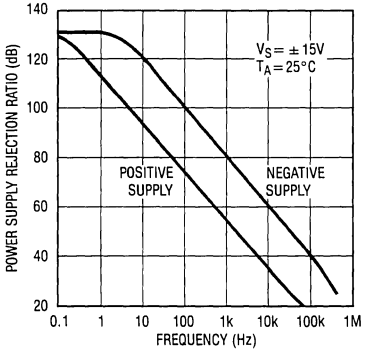


TYPICAL PERFORMANCE CHARACTERISTICS

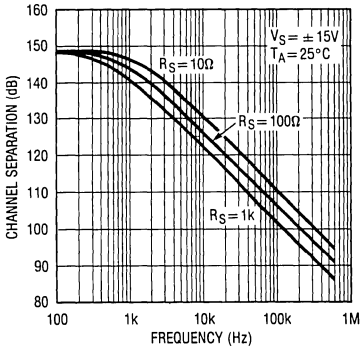
Common-Mode Rejection and CMRR Match vs Frequency



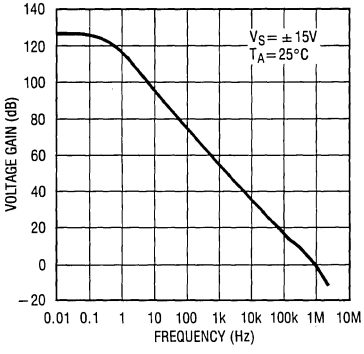
Power Supply Rejection vs Frequency



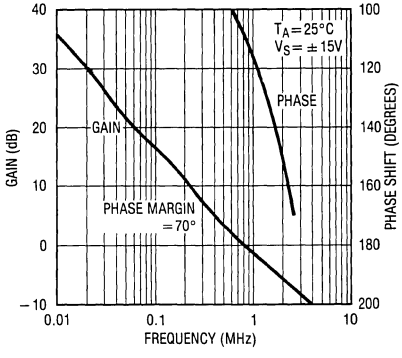
Channel Separation vs Frequency



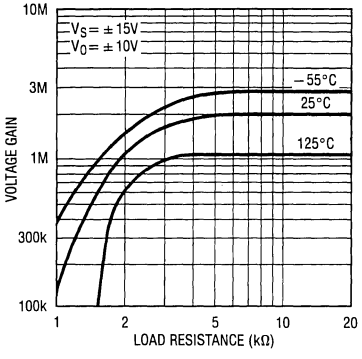
Voltage Gain vs Frequency



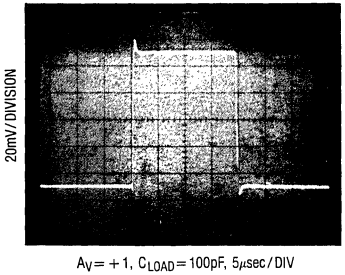
Gain, Phase Shift vs Frequency



Voltage Gain vs Load Resistance

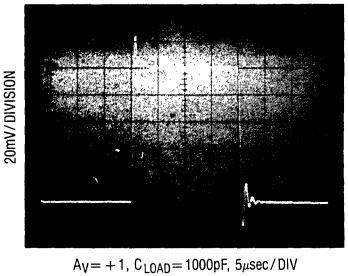


Small Signal Transient Response



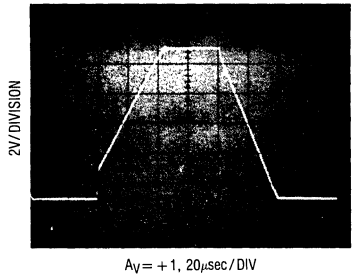
$A_V = +1$, $C_{LOAD} = 100pF$, $5\mu sec/DIV$

Small Signal Transient Response



$A_V = +1$, $C_{LOAD} = 1000pF$, $5\mu sec/DIV$

Large Signal Transient Response



$A_V = +1$, $20\mu sec/DIV$

APPLICATIONS INFORMATION

The LT1024 may be inserted directly into OP-10, OP-207 or OP227 sockets with or without removal of external nulling components.

The LT1024 is specified over a wide range of power supply voltages from ±2V to ±18V. Operation with lower supplies is possible down to ±1.2V (two NiCad batteries).

Advantages of Matched Dual Op Amps

In many applications, the performance of a system depends on the matching between two operational amplifiers rather than the individual characteristics of the two op amps. Two or three op amp instrumentation amplifiers, tracking voltage references, and low drift active filters are some of the circuits requiring matching between two op amps.

The well-known triple op amp configuration illustrates these concepts. Output offset is a function of the difference between the offsets of the two halves of the LT1024. This error cancellation principle holds for a considerable number of input-referred parameters in addition to offset voltage and its drift with temperature. Input bias current will be the average of the two non-inverting input currents (I_B^+). The difference between these two currents (I_{OS}^+) is the offset current of the instrumentation amplifier. Common-mode and power supply rejections will be dependent only on the match between the two amplifiers (assuming perfect resistor matching).

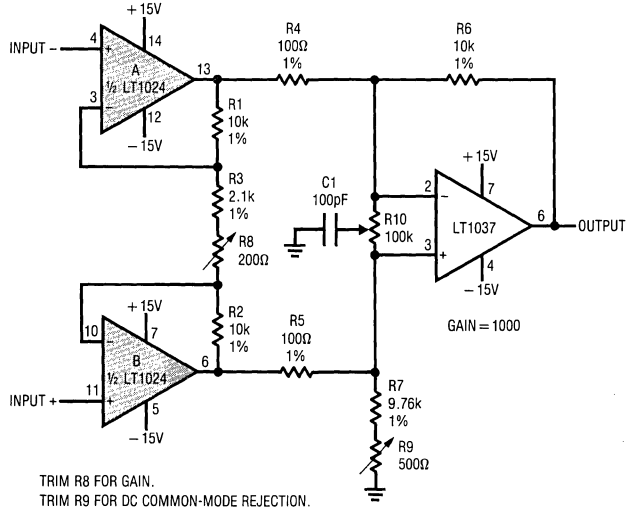
The concepts of common-mode and power supply rejection ratio match (ΔCMRR and ΔPSRR) are best demonstrated with a numerical example:

Assume $CMRR_A = +1.0\mu V/V$ or 120dB
and $CMRR_B = +0.5\mu V/V$ or 126dB,
then $\Delta CMRR = 0.5\mu V/V$ or 126dB
if $CMRR_B = -0.5\mu V/V$, which is still 126dB,
then $\Delta CMRR = 1.5\mu V/V$ or 116.5dB.

Typical performance of the instrumentation amplifier:
Input offset voltage = 25μV.
Input bias current = 30pA.
Input resistance = $10^{12}\Omega$.
Input offset current = 30pA.
Input noise = 0.7μVp-p.
Power bandwidth ($V_O = \pm 10V$) = 80kHz.

Clearly, the LT1024, by specifying and guaranteeing all of these matching parameters, can significantly improve the performance of matching dependent circuits.

Three Op Amp Instrumentation Amplifier



APPLICATIONS INFORMATION

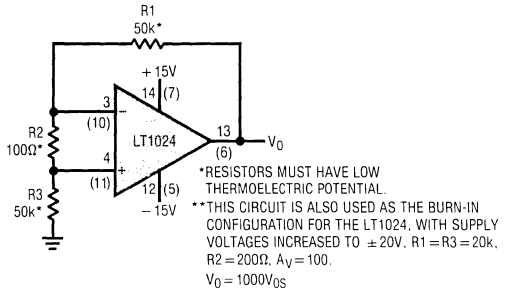
Achieving Picoampere/Microvolt Performance

In order to realize the picoampere/microvolt level accuracy of the LT1024, proper care must be exercised. For example, leakage currents in circuitry external to the op amp can significantly degrade performance. High quality insulation should be used (e.g., Teflon, Kel-F); cleaning of all insulating surfaces to remove fluxes and other residues will probably be required. Surface coating may be necessary to provide a moisture barrier in high humidity environments.

Board leakage can be minimized by encircling the input circuitry with a guard ring operated at a potential close to that of the inputs: in inverting configurations, the guard ring should be tied to ground, in non-inverting connections, to the inverting input. Guarding both sides of the printed circuit board is required. Bulk leakage reduction depends on the guard ring width. Nanoampere level leakage into the offset trim terminals can affect offset voltage and drift with temperature.

Microvolt level error voltages can also be generated in the external circuitry. Thermocouple effects caused by temperature gradients across dissimilar metals at the contacts to the input terminals can exceed the inherent drift of the amplifier. Air currents over device leads should be minimized, package leads should be short, and the two input leads should be as close together as possible and maintained at the same temperature.

Test Circuit for Offset Voltage and its Drift with Temperature

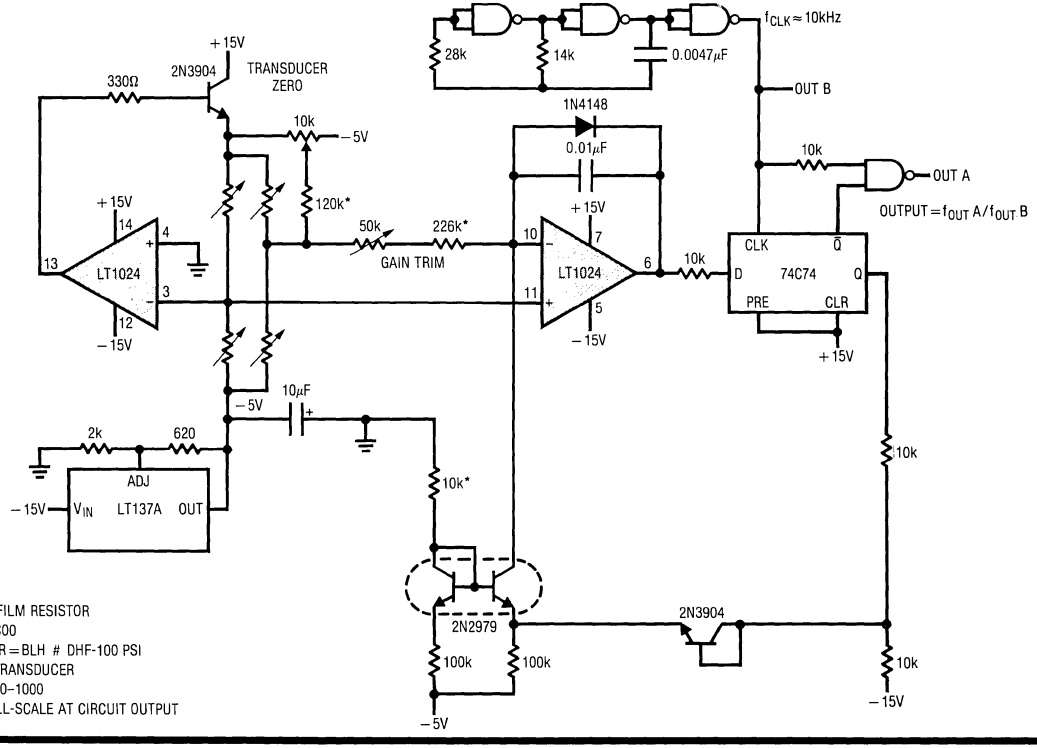


*RESISTORS MUST HAVE LOW THERMOELECTRIC POTENTIAL.

**THIS CIRCUIT IS ALSO USED AS THE BURN-IN CONFIGURATION FOR THE LT1024, WITH SUPPLY VOLTAGES INCREASED TO ±20V. R1 = R3 = 20k, R2 = 200Ω, A_V = 100.

$V_O = 1000V_{OS}$

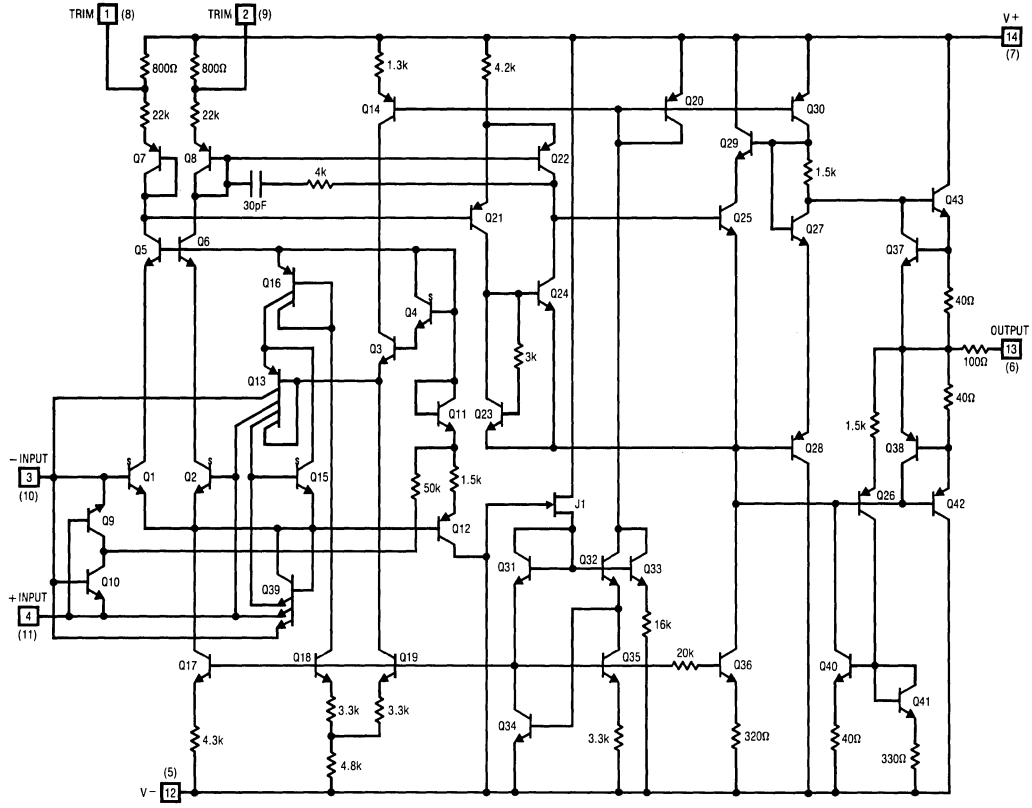
Direct Pressure Transducer to Digital Output Signal Conditioner



*1% METAL FILM RESISTOR
GATES = 74C00
TRANSDUCER = BLH # DHF-100 PSI PRESSURE TRANSDUCER
0–100 PSI = 0–1000 COUNTS FULL-SCALE AT CIRCUIT OUTPUT

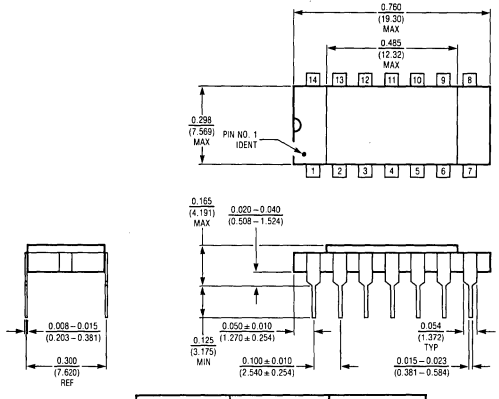
SCHEMATIC DIAGRAM

½ LT1024



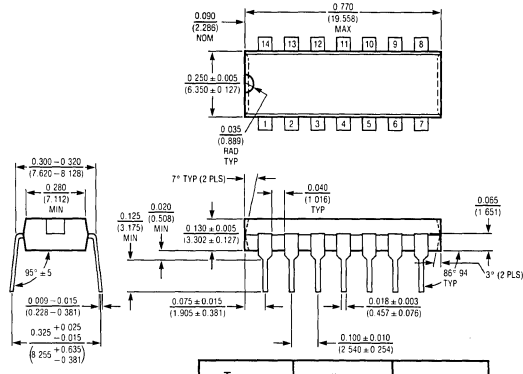
PACKAGE DESCRIPTION

D14 Package 14-Lead Hermetic DIP (Sidebrazed)



T_{JMAX}	Θ_{JA}	Θ_{JC}
150°C	100°C/W	60°C/W

N14 Package 14-Lead Plastic



T_{JMAX}	Θ_{JA}	Θ_{JC}
100°C	100°C/W	60°C/W

Chopper-Stabilized Operational Amplifier (CSOA™)

FEATURES

- *Guaranteed* Max. Offset 5μV
- *Guaranteed* Max. Offset Drift 0.05μV/°C
- Typ. Offset Drift 0.01μV/°C
- Excellent Long Term Stability 100nV/√Month
- *Guaranteed* Max. Input Bias Current 30pA
- Over Operating Temperature Range
  - *Guaranteed* Min. Gain 120dB
  - *Guaranteed* Min. CMRR 120dB
  - *Guaranteed* Min. PSRR 120dB
- Single Supply Operation 4.75V to 16V (Input Voltage Range Extends to Ground)
- External Capacitors can be Returned to V^- with No Noise Degradation

APPLICATIONS

- Thermocouple Amplifiers
- Strain Gauge Amplifiers
- Low Level Signal Processing
- Medical Instrumentation

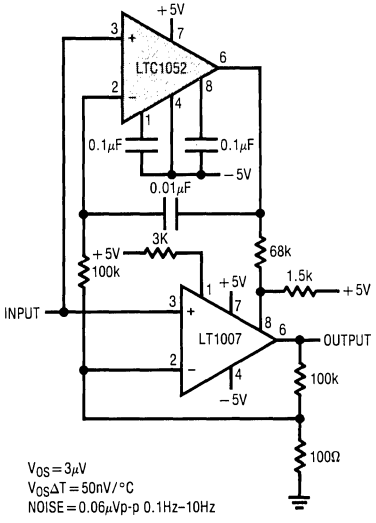
DESCRIPTION

The LTC1052 and LTC7652 are low noise Chopper-stabilized op amps (CSOA™) manufactured using Linear Technology's enhanced LTCMOS™ silicon gate process. Chopper-stabilization constantly corrects offset voltage errors. Both initial offset and changes in the offset due to time, temperature and common-mode voltage are corrected. This, coupled with picoampere input currents, gives these amplifiers unmatched performance.

Low frequency (1/f) noise is also improved by the chopping technique. Instead of increasing continuously at a 3dB/octave rate, the internal chopping causes noise to decrease at low frequencies.

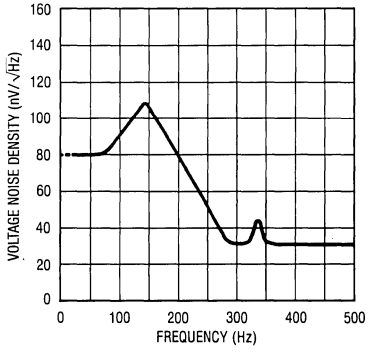
The chopper circuitry is entirely internal and completely transparent to the user. Only two external capacitors are required to alternately sample and hold the offset correction voltage and the amplified input signal. Control circuitry is brought out on the 14-pin version to allow the sampling of the LTC1052 to be synchronized with an external frequency source.

Ultra Low Noise, Low Drift Amplifier



$V_{OS} = 3\mu V$
$V_{OS}\Delta T = 50nV/°C$
NOISE = 0.06μVp-p 0.1Hz–10Hz

LTC1052 Noise Spectrum

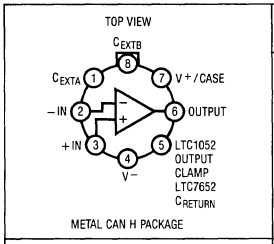


ABSOLUTE MAXIMUM RATINGS

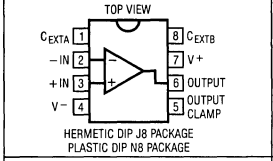
(Notes 1 and 2)

Total Supply Voltage (V^+ to V^-) 18V
Input Voltage ..... ($V^+ + 0.3V$) to ($V^- - 0.3V$)
Output Short Circuit Duration ..... Indefinite
Operating Temperature Range
LTC1052C/LTC7652C ..... −40°C to 85°C
LTC1052M ..... −55°C to 125°C
Storage Temperature Range ..... −55°C to 150°C
Lead Temperature (Soldering, 10 sec.) ..... 300°C

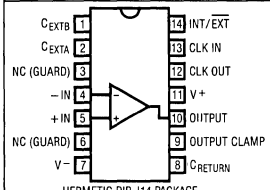
PACKAGE/ORDER INFORMATION



METAL CAN H PACKAGE



HERMETIC DIP J8 PACKAGE
PLASTIC DIP N8 PACKAGE



HERMETIC DIP J14 PACKAGE
PLASTIC DIP N14 PACKAGE

ORDER PART NUMBER	REPLACES
LTC7652CH	ICL7652CTV ICL7652ITV ICL7650CTV-1 ICL7650ITV-1
LTC1052CH	ICL7650CTV ICL7650ITV
LTC1052MH	ICL7650MTV
LTC1052CN8 LTC1052CJ8 LTC1052MJ8	ICL7650CPA ICL7650IJA
LTC1052CJ	ICL7652IJD ICL7650IJD
LTC1052CN	ICL7652CPD ICL7650CPD
LTC1052MJ	ICL7650MJD

ELECTRICAL CHARACTERISTICS

$V_S = \pm 5V$, T_A = operating temperature range, test circuit TC1, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		LTC1052M MIN	LTC1052M TYP	LTC1052M MAX	LTC1052C/LTC7652C MIN	LTC1052C/LTC7652C TYP	LTC1052C/LTC7652C MAX	UNITS
V_{OS}	Input Offset Voltage	$T_A = 25°C$ (Note 3)			±0.5	±5		±0.5	±5	µV
$\Delta V_{OS}/\Delta Temp$	Average Input Offset Drift	(Note 3)	●		±0.01	±0.05		±0.01	±0.05	µV/°C
$\Delta V_{OS}/\Delta Time$	Long Term Offset Voltage Stability				100			100		nV/√Month
I_{OS}	Input Offset Current	$T_A = 25°C$			±5	±30		±5	±30	pA
			●			±2000			±350	pA
I_B	Input Bias Current	$T_A = 25°C$			±1	±30		±1	±30	pA
			●			±1000			±175	pA
e_{np-p}	Input Noise Voltage	$R_S = 100\Omega$, DC to 10Hz, TC3			1.5			1.5		µVp-p
		$R_S = 100\Omega$, DC to 1Hz, TC3			0.5			0.5		µVp-p
i_n	Input Noise Current	f = 10Hz (Note 5)			0.6			0.6		fA/√Hz
CMRR	Common-Mode Rejection Ratio	$V_{CM} = V^-$ to $+2.7V$	●	120	140		120	140		dB
PSRR	Power Supply Rejection Ratio	$V_{SUPPLY} = \pm 2.375V$ to $\pm 8V$	●	120	150		120	150		dB
A_{VOL}	Large Signal Voltage Gain	$R_L = 10k$, $V_{OUT} = \pm 4V$	●	120	150		120	150		dB
V_{OUT}	Maximum Output Voltage Swing (Note 4)	$R_L = 10k$	●	±4.7	±4.85		±4.7	±4.85		V
		$R_L = 100k$			±4.95			±4.95		V
SR	Slew Rate	$R_L = 10k$, $C_L = 50pF$			4			4		V/µs
GBW	Gain Bandwidth Product				1.2			1.2		MHz
I_S	Supply Current	No Load, $T_A = 25°C$			1.7	2.0		1.7	2.0	mA
			●			3.0			3.0	mA
f_S	Internal Sampling Frequency				330			330		Hz
	Clamp On Current	$R_L = 100k$	●	25	100		25	100		µA
	Clamp Off Current	$-4V < V_{OUT} < +4V$			10	100		10	100	pA
			●			2			1	nA

The ● denotes the specifications which apply over the full operating temperature range.

Note 1: Absolute Maximum Ratings are those values beyond which the life of the device may be impaired.

Note 2: Connecting any terminal to voltages greater than V^+ or less than V^- may cause destructive latch-up. It is recommended that no sources operating from external supplies be applied prior to power-up of the LTC1052/LTC7652.

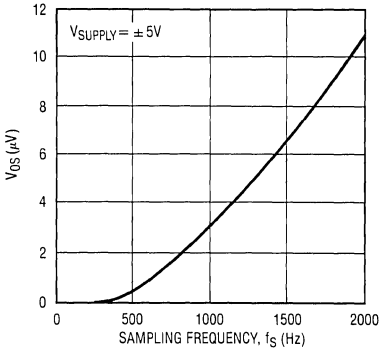
Note 3: These parameters are guaranteed by design. Thermocouple effects preclude measurement of these voltage levels in high speed automatic testing. V_{OS} is measured to a limit determined by test equipment capability. Voltages on C_{EXTA} and C_{EXTB}, A_{VOL}, CMRR and PSRR are measured to insure proper operation of the nulling loop to insure meeting the V_{OS} and V_{OS} drift specifications. See Package-Induced V_{OS} in applications section.

Note 4: Output clamp not connected.

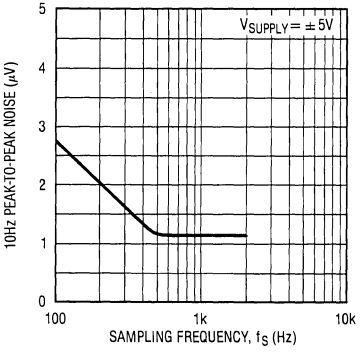
Note 5: Current noise is calculated from the formula: $i_n = (2q\ I_B)^{1/2}$, where $q = 1.6 \times 10^{-19}$ coulomb.

TYPICAL PERFORMANCE CHARACTERISTICS

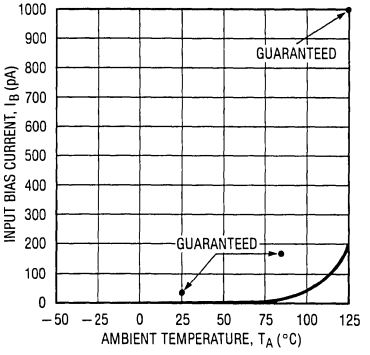
Offset Voltage vs Sampling Frequency



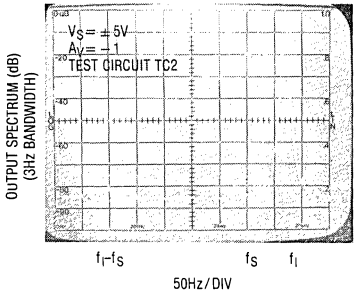
10Hzp-p Noise vs Sampling Frequency



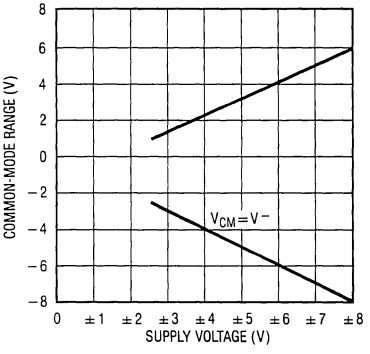
Input Bias Current vs Temperature



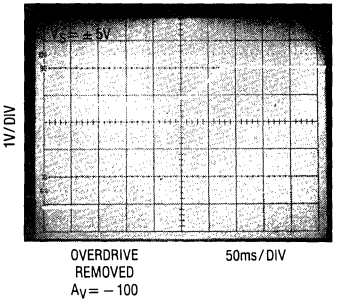
Aliasing Error



Common-Mode Input Range vs Supply Voltage

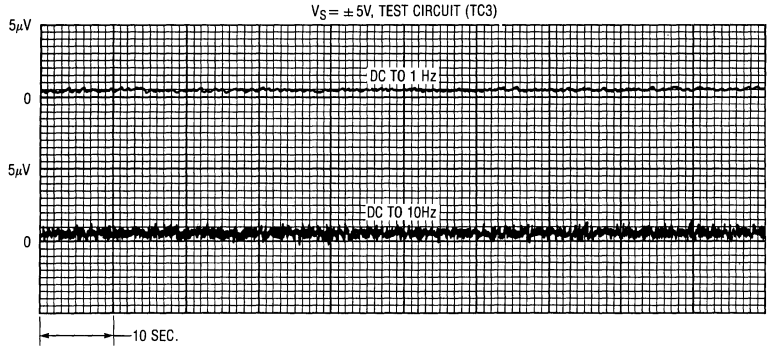


Overload Recovery (Output Clamp Not Used)

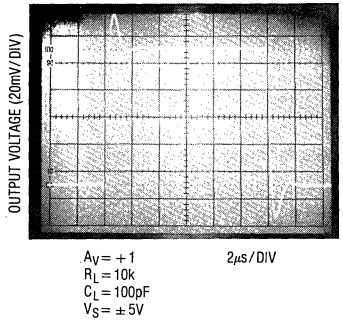


TYPICAL PERFORMANCE CHARACTERISTICS

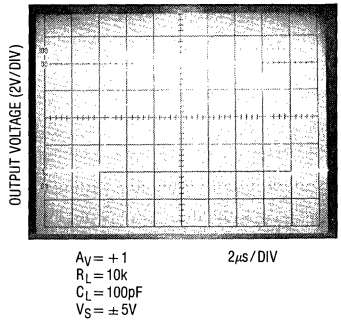
Input Noise Voltage



Small Signal Transient Response*

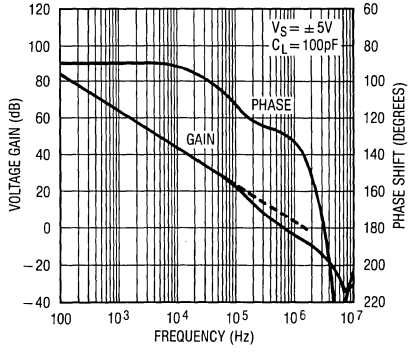


Large Signal Transient Response*

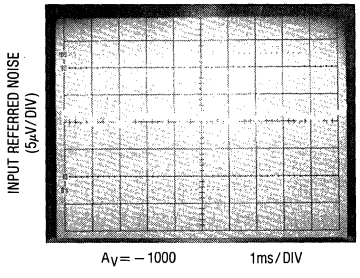


*RESPONSE IS NOT DEPENDENT ON PHASE OF CLOCK

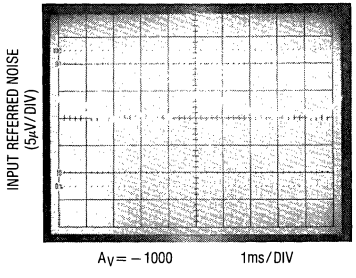
Gain Phase vs Frequency



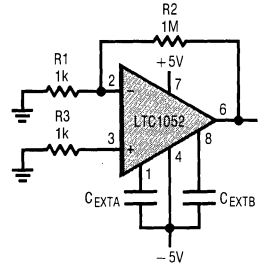
Broadband Noise, $C_{EXT} = 0.1\mu F$



Broadband Noise, $C_{EXT} = 1.0\mu F$

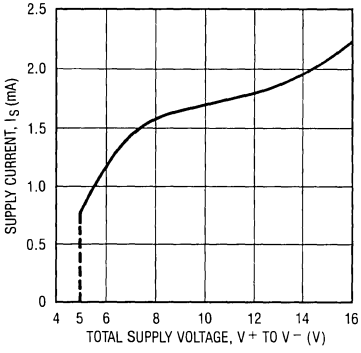


Broadband Noise Test Circuit (TC2)

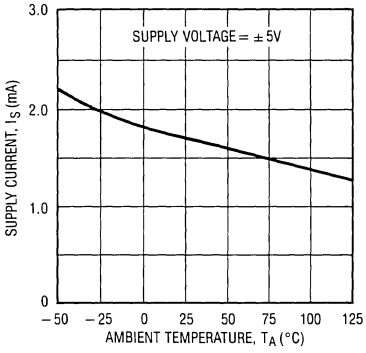


TYPICAL PERFORMANCE CHARACTERISTICS

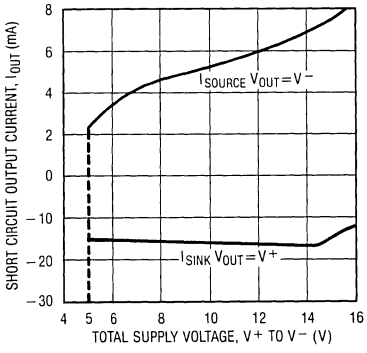
Supply Current vs Supply Voltage



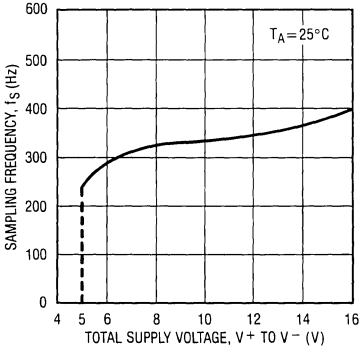
Supply Current vs Temperature



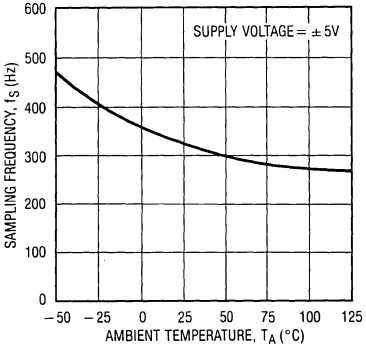
Output Short Circuit Current vs Supply Voltage



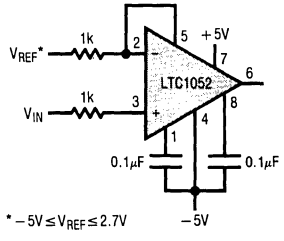
Sampling Frequency vs Supply Voltage



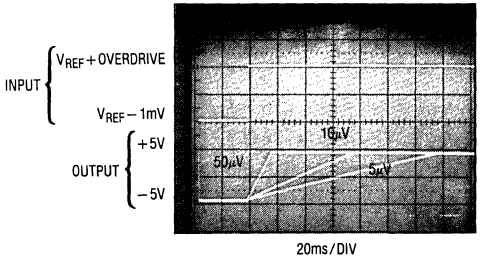
Sampling Frequency vs Temperature



Comparator Operation

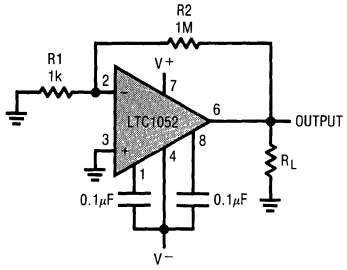


Response Time vs Overdrive

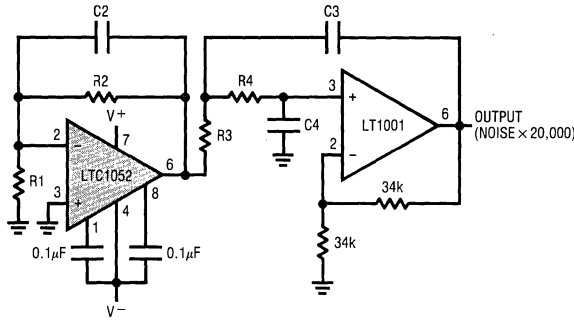


TEST CIRCUITS

Electrical Characteristics Test Circuit (TC1)



DC to 10Hz and DC to 1Hz Noise Test Circuit (TC3)



BANDWIDTH	R1	R2	R3	R4	C2	C3	C4
10Hz	16.2Ω	162k	16.2k	16.2k	0.1μF	1.0μF	1.0μF
1Hz	16.2Ω	162k	162k	162k	1.0μF	1.0μF	1.0μF

THEORY OF OPERATION

DC OPERATION

The shaded portion of the LTC1052 block diagram (Figure 1) entirely determines the amplifier's DC characteristics. During the auto-zero portion of the cycle, the inputs are shorted together and a feedback path is closed around the input stage to null its offset. Switch S2 and capacitor C_{EXTA} act as a sample and hold to store the nulling voltage during the next step—the sampling cycle.

In the sampling cycle, the zeroed amplifier is used to amplify the differential input voltage. Switch S2 connects the amplified input voltage to C_{EXTB} and the output gain stage. C_{EXTB} and S2 act as a sample and hold to store the amplified input signal during the auto-zero cycle. By switching between these two states at a frequency much higher than the signal frequency, a continuous output results.

Notice that during the auto-zero cycle the inputs are not only shorted together, but are also shorted to the negative input. This forces nulling with the common-mode voltage present and accounts for the extremely high CMRR of the LTC1052. In the same fashion, variations in power supply are also nulled. For nulling to take place, the offset voltage, common-mode voltage and power supply must not change at a frequency which is high compared to the frequency response of the nulling loop.

AC OPERATION AND ALIASING ERRORS

So far, the DC performance of the LTC1052 has been explained. As the input signal frequency increases, the problem of aliasing must be addressed. Aliasing is the spurious formation of low and high frequency signals caused by the mixing of the input signal with the sampling frequency, f_S. The frequency of the error signals, f_E, is:

$$f_E = f_S \pm f_I$$

where f_I = input signal frequency.

Normally it is the difference frequency ($f_S - f_I$) which is of concern because the high frequency ($f_S + f_I$) can be easily filtered. As the input frequency approaches the sampling frequency, the difference frequency approaches zero and will cause DC errors—the exact problem that the chopping amplifier is meant to eliminate.

The solution is simple. Filter the input so the sampling loop never sees any frequency near the sampling frequency.

At a frequency well below the sampling frequency, the LTC1052 forces I_1 to equal I_2 (see Figure 1B). This makes δI zero, thus the gain of the sampling loop zero at this and higher frequencies—i.e., a low pass filter. The corner frequency of this low pass filter is set by the output stage pole ($1/R_{L4}\ g_{m5}\ R_{L5}\ C2$).

THEORY OF OPERATION

For frequencies above this pole, I_2 is:

$$I_2 = V_{IN}\ g_{m6} \times \frac{1}{SC2} \times SC1$$

and

$$I_1 - I_2 = V_{IN}\ g_{m1} - V_{IN}\ g_{m6} \times \frac{C1}{C2}.$$

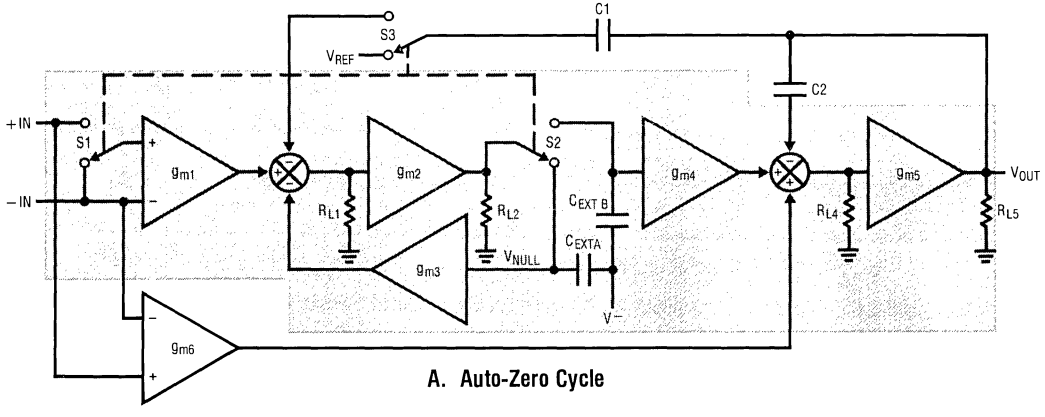
The LTC1052 is very carefully designed so that $g_{m1} = g_{m6}$ and C1 = C2. Substituting these values in the above equation shows $I_1 - I_2 = 0$.

The g_{m6} input stage, with C1 and C2, not only filters the input to the sampling loop, but also acts as a high frequency path to give the LTC1052 good high frequency response. The unity-gain cross frequencies for both the DC path and high frequency path are identical

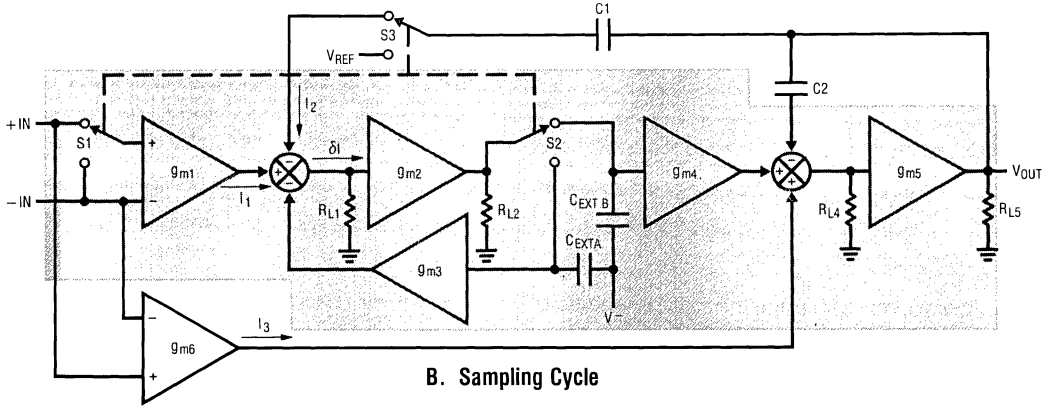
$$[f3dB = \frac{1}{2\pi}\ (g_{m1}/C1) = \frac{1}{2\pi}\ (g_{m6}/C2)].$$

This makes the frequency response smooth and continuous and eliminates sampling noise in the output as the loop transitions from the high gain DC loop to the high frequency loop.

The typical curves show just how well the amplifier works. The output spectrum shows the difference frequency ($f_I - f_S = 100Hz$) is down by 80dB and the frequency response curve shows no abnormalities or perturbations. Also note the well-behaved small and large signal step responses and the absence of the sampling frequency in the output spectrum. If the dynamics of the amplifier, i.e., slew rate and overshoot, depend on the sampling clock, the sampling frequency will appear in the output spectrum.



A. Auto-Zero Cycle



B. Sampling Cycle

Figure 1. LTC1052 Block Diagram

APPLICATIONS INFORMATION

EXTERNAL CAPACITORS

C_{EXTA} and C_{EXTB} are the holding elements of a sample and hold circuit. The important capacitor characteristics are leakage current and dielectric absorption. A high quality film-type capacitor such as mylar or polypropylene provides excellent performance. However, low grade capacitors such as ceramic are suitable in many applications.

Capacitors with very high dielectric absorption (ceramic) can take several seconds to settle after power is first turned on. This settling appears as clock ripple on the output and, as the capacitor settles, the ripple gradually disappears. If fast settling after power turn-on is important, mylar or polypropylene is recommended.

Above 85°C, leakage, both from the holding capacitors and the printed circuit board, becomes important. To maintain the capabilities of the LTC1052 it may be necessary to use Teflon™ capacitors and Teflon standoffs when operating at 125°C (see Achieving Picoampere/Microvolt Performance).

C_{EXTA} and C_{EXTB} are normally in the range of 0.1μF to 1.0μF. All specifications are guaranteed with 0.1μF and the broadband noise (see typical photos) is only very slightly degraded with 0.1μF. Output clock ripple is not present for capacitors of 0.1μF or greater at any temperature.

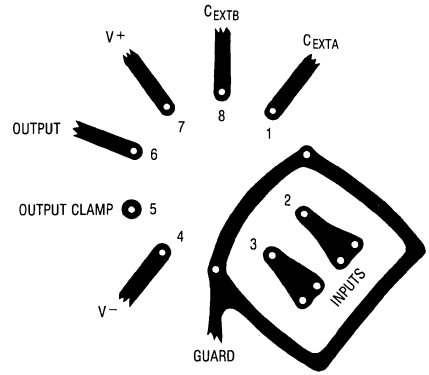
On competitive devices, connecting C_{EXTA} and C_{EXTB} to V^- causes an increase in amplifier noise. Design changes have eliminated this problem on the LTC1052. On the 14-pin LTC1052 and 8-pin LTC7652, the capacitors can be returned to V^- or C_{RETURN} with no change in noise performance.

ACHIEVING PICOAMPERE/MICROVOLT PERFORMANCE

Picoamperes

In order to realize the picoampere level of accuracy of the LTC1052, proper care must be exercised. Leakage currents in circuitry external to the amplifier can significantly degrade performance. High quality insulation should be used (e.g., Teflon, Kel-F); cleaning of all insulating surfaces to remove fluxes and other residues will probably be necessary—particularly for high temperature performance. Surface coating may be necessary to provide a moisture barrier in high humidity environments.

Board leakage can be minimized by encircling the input connections with a guard ring operated at a potential close to that of the inputs: in inverting configurations the guard ring should be tied to ground; in non-inverting connections to the inverting input. Guarding both sides of the printed circuit board is required. Bulk leakage reduction depends on the guard ring width.



Microvolts

Thermocouple effects must be considered if the LTC1052's ultra low drift is to be fully utilized. Any connection of dissimilar metals forms a thermoelectric junction producing an electric potential which varies with temperature (Seebeck effect). As temperature sensors, thermocouples exploit this phenomenon to produce useful information. In low drift amplifier circuits the effect is a primary source of error.

Connectors, switches, relay contacts, sockets, resistors, solder, and even copper wire are all candidates for thermal EMF generation. Junctions of copper wire from different manufacturers can generate thermal EMFs of 200nV/°C—4 times the maximum drift specification of

APPLICATIONS INFORMATION

the LTC1052. The copper/kovar junction, formed when wire or printed circuit traces contact a package lead, has a thermal EMF of approximately 35μV/°C—700 times the maximum drift specification of the LTC1052.

Minimizing thermal EMF-induced errors is possible if judicious attention is given to circuit board layout and component selection. It is good practice to minimize the number of junctions in the amplifier's input signal path. Avoid connectors, sockets, switches and relays where possible. In instances where this is not possible, attempt to balance the number and type of junctions so that differential cancellation occurs. Doing this may involve deliberately introducing junctions to offset unavoidable junctions.

Figure 2 is an example of the introduction of an unnecessary resistor to promote differential thermal balance. Maintaining compensating junctions in close physical proximity will keep them at the same temperature and reduce thermal EMF errors.

When connectors, switches, relays and/or sockets are necessary they should be selected for low thermal EMF activity. The same techniques of thermally balancing and coupling the matching junctions are effective in reducing the thermal EMF errors of these components.

Resistors are another source of thermal EMF errors. Table I shows the thermal EMF generated for different resistors. The temperature gradient across the resistor is important, not the ambient temperature. There are two junctions formed at each end of the resistor and if these junctions are at the same temperature, their thermal EMFs will cancel each other. The thermal EMF numbers are approximate and vary with resistor value. High values give higher thermal EMF.

When all of these errors are considered, it may seem impossible to take advantage of the extremely low drift specifications of the LTC1052. To show that this is not the case, examine the temperature test circuit of Figure 3. The lead lengths of the resistors connected to the amplifier's inputs are identical. The thermal capacity and thermal resistance each input sees is balanced because of the symmetrical connection of resistors and their identical size. Thermal EMF-induced shifts are equal in phase and amplitude, thus cancellation occurs.

Figure 4 shows the response of this circuit under temperature transient conditions. Metal film resistors and an 8-pin DIP socket were used. Care was taken in the construction to thermally balance the inputs to the amplifier. The units were placed in an oven and allowed to stabilize at 25°C. The recording was started, and after 100 seconds the oven, preset to 125°C, was switched on. The test was first performed on an 8-pin plastic package and then was repeated for a TO-5 package plugged into the same test board. It is significant that the change in V_{OS}, even under these severe thermal transient conditions, is quite good. As temperature stabilizes, note that the steady-state change of V_{OS} is well within the maximum ±0.05μV/°C drift specification.

Table I. Resistor Thermal EMF

Resistor Type	Thermal EMF/°C Gradient
Tin Oxide	~mV/°C
Carbon Composition	~450μV/°C
Metal Film	~20μV/°C
Wire Wound	
Evenohm	~2μV/°C
Manganin	~2μV/°C

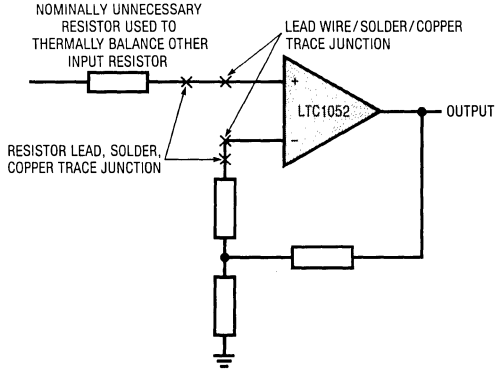


Figure 2

APPLICATIONS INFORMATION

Very slight air currents can still affect even this arrangement. Figure 5 shows strip charts of output noise with the circuit covered and with no cover in ''still'' air. This data illustrates why it is often prudent to enclose the LTC1052 and its attendant components inside some form of thermal baffle.

PACKAGE-INDUCED OFFSET VOLTAGE

Since the LTC1052 is constantly fixing its own offset, it may be asked why there is any error at all, even under transient temperature conditions. The answer is simple. The LTC1052 can only fix offsets inside its own nulling loop. There are many thermal junctions outside this loop that cannot be distinguished from legitimate signals.

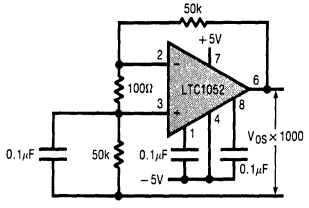


Figure 3. Offset Drift Test Circuit

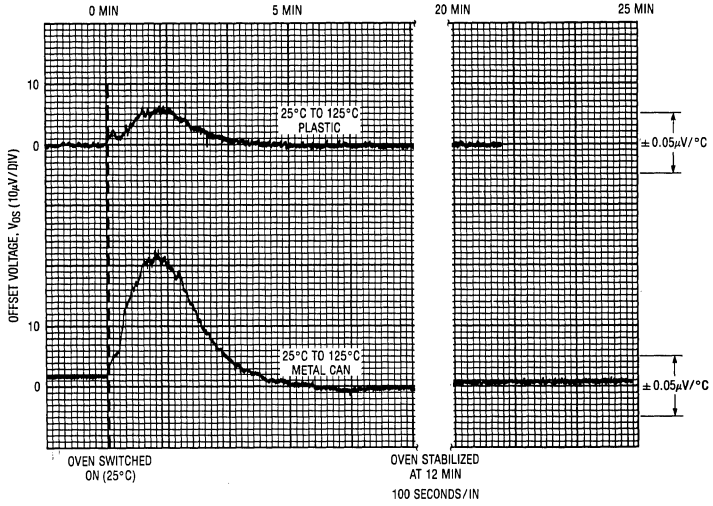


Figure 4. Transient Response of Offset Drift Test Circuit with 100°C Temperature Step

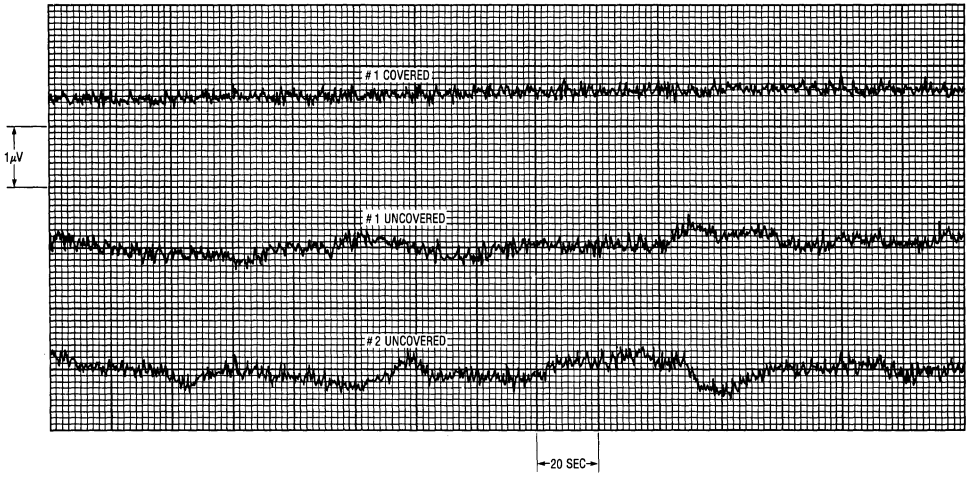


Figure 5. DC to 1Hz (Test Circuit TC3)

APPLICATIONS INFORMATION

Some have been discussed previously, but the package thermal EMF effects are an important source of errors.

Notice the difference in the thermal response curves of Figure 4. This can only be attributed to the package since everything else is identical. In fact, the V_{OS} specification is set by the package-induced warm-up drift, not by the LTC1052. TO-99 metal cans exhibit the worst warm-up drift and Linear Technology sample tests TO-99 lots to minimize this problem.

Two things make 100% screening costly: (1) the extreme precision required on the LTC1052 and (2) the thermal time constant of the package is 0.5 to 3 minutes, depending on package type. The first precludes the use of automatic handling equipment and the second takes a long time. Bench test equipment is available to 100% test for warmed-up drift if offsets of less than $\pm 5\mu V$ are required.

CLOCK

The LTC1052 has an internal clock, setting the nominal sampling frequency at 330Hz. On 8-pin devices there is no way to control the clock externally. In some applications it may be desirable to control the sampling clock and this is the function of the 14-pin device.

CLK IN, CLK OUT and INT/$\overline{EXT}$ are provided to accomplish this. With no external connection, an internal pull-up holds INT/$\overline{EXT}$ at the V^+ supply and the 14-pin device self-oscillates at 330Hz. In this mode there is a signal on the CLK IN pin of 660Hz (2 times sampling frequency) with a 30% duty cycle. A divide-by-two drives the CLK OUT pin and sets the sampling frequency.

To use an external clock, connect INT/$\overline{EXT}$ to V^- and the external clock to CLK IN. The logic threshold of CLK IN is 2.5V below the positive supply. This allows CMOS logic to drive it directly with logic supplies of V^+ and ground. CLK IN can be driven from V^+ to V^- if desired. The duty cycle of the external clock is not particularly critical but should be kept between 30% and 60%.

Capacitance between CLK IN and CLK OUT (pins 13 and 12) can cause the divide-by-two circuit to malfunction. To avoid this, keep this capacitance below 5pF.

OUTPUT CLAMP

If the LTC1052 is driven into saturation, the nulling loop, attempting to force the differential input voltage to zero, will drive C_{EXTA} and C_{EXTB} to a supply rail. After the saturating drive is removed, the capacitors take a finite time to recover—this is the overload recovery time. The overload recovery is longest when the capacitors are driven to the negative rail (see Overload Recovery in typical performance section). The overload recovery time in this case is typically 225ms. In the opposite direction, i.e., C_{EXTA} and C_{EXTB} at positive rail, it is about ten times faster (25ms). The overload recovery time for the LTC1052 is much faster than competitive devices, but if a faster overload recovery time is necessary, the output clamp function can be used.

When the output clamp is connected to the negative input it prevents the amplifier from saturating and thus keeps C_{EXTA} and C_{EXTB} at their nominal voltages. The output clamp is a switch that turns on when the output gets to within approximately 1V of either supply rail. This switch is in parallel with the amplifier's feedback resistor and as the output moves closer to the rail, the switch on resistance decreases, reducing the closed loop gain. The output swing is reduced when the clamp function is used.

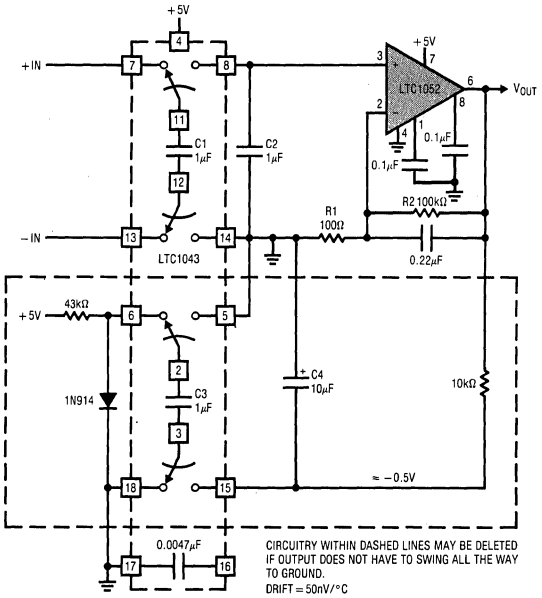
How much current the output clamp leaks when off is important because, when used, it is connected to the amplifier's negative input. Any current acts like input bias current and will degrade accuracy. At the other extreme, the maximum current the clamp conducts when on determines how much overdrive the clamp will take and still keep the amplifier from saturating. Both of these numbers are guaranteed in the table of electrical characteristics.

LOW SUPPLY OPERATION

The minimum supply voltage for proper operation of the LTC1052 is typically 4.0V ($\pm 2.0V$). In single supply applications, PSRR is guaranteed down to 4.7V ($\pm 2.35V$). This assures proper operation down to the minimum TTL specified voltage of 4.75V.

TYPICAL APPLICATIONS

5V Powered Ultra Precision Instrumentation Amplifier



CIRCUITRY WITHIN DASHED LINES MAY BE DELETED IF OUTPUT DOES NOT HAVE TO SWING ALL THE WAY TO GROUND.

DRIFT = 50nV/°C

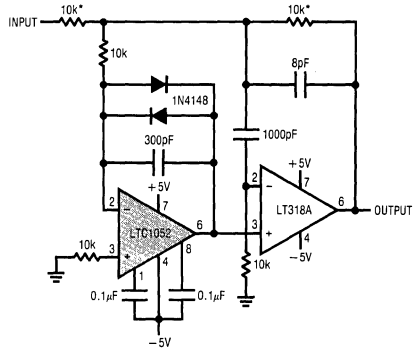
V_{OS} = 3µV

$GAIN = \frac{R2}{R1} + 1$

CMRR = > 120dB DC – 20kHz

BANDWIDTH = 10Hz

Fast Precision Inverter



*1% METAL FILM

FULL POWER BANDWIDTH = 2MHz

SLEW RATE = 40V/µs

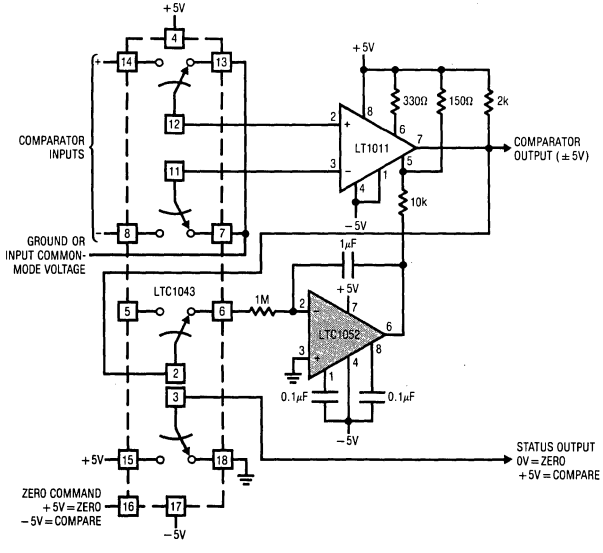
SETTLING (10V STEP) = 12µs TO 0.01%

BIAS CURRENT DC = 30pA

OFFSET DRIFT = 50nV/°C

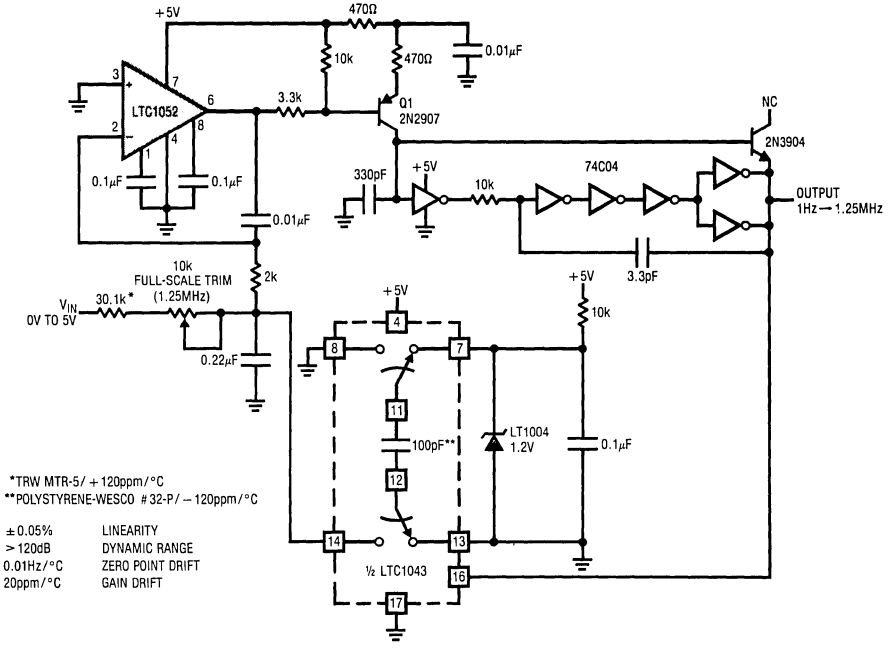
OFFSET VOLTAGE = 5µV

Offset Stabilized Comparator

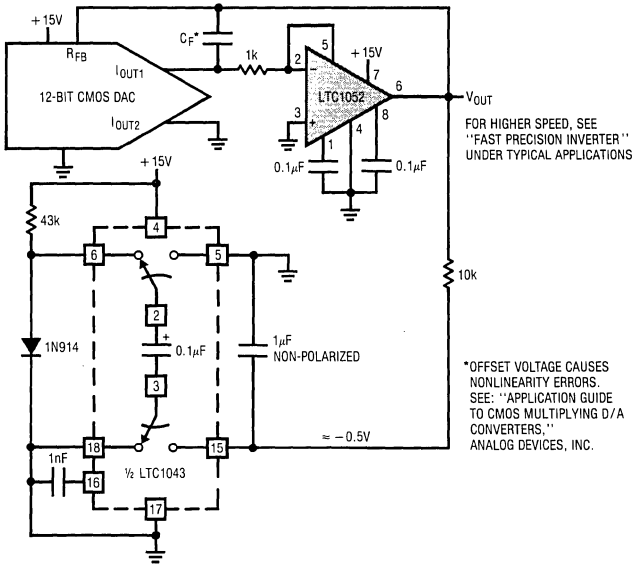


TYPICAL APPLICATIONS

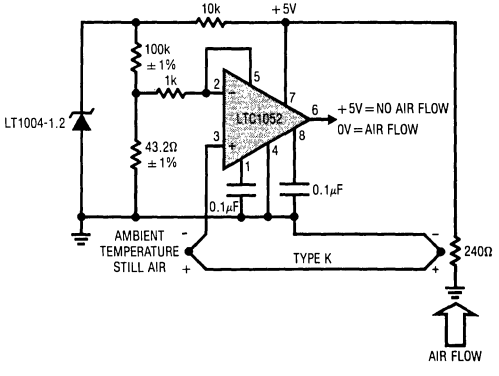
1Hz → 1.25MHz Voltage-to-Frequency Converter (+5V Supply)



No V_{OS} Adjust* CMOS DAC Buffer—Single Supply

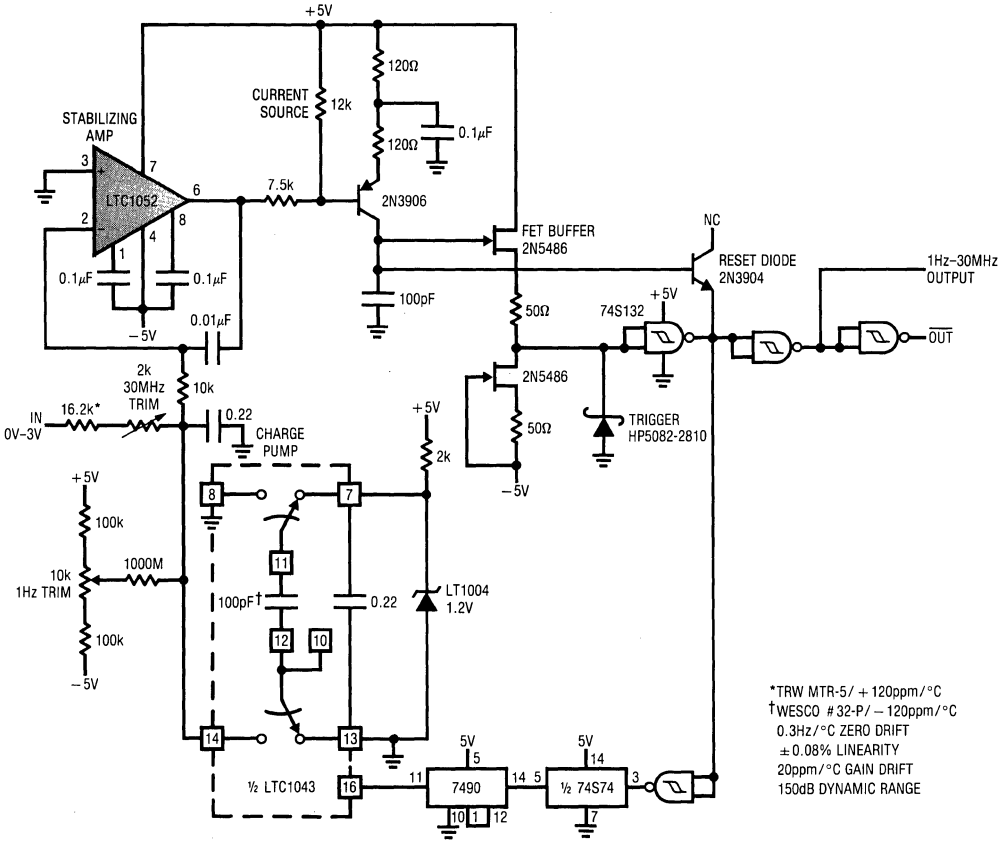


Air Flow Detector

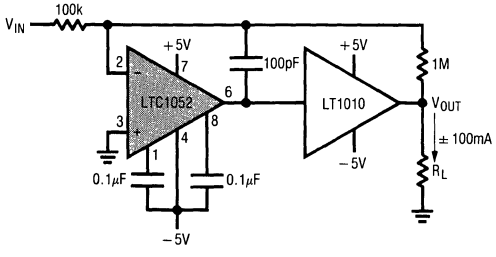


TYPICAL APPLICATIONS

1Hz → 30MHz Voltage-to-Frequency Converter

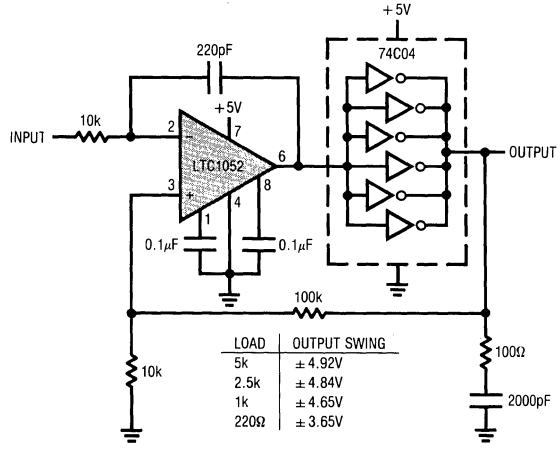


±100mA Output Drive



$V_{OS} = 5\mu V$
$V_{OS}/\Delta T = 50nV/°C$
GAIN = 10
FULL POWER BANDWIDTH = 1kHz

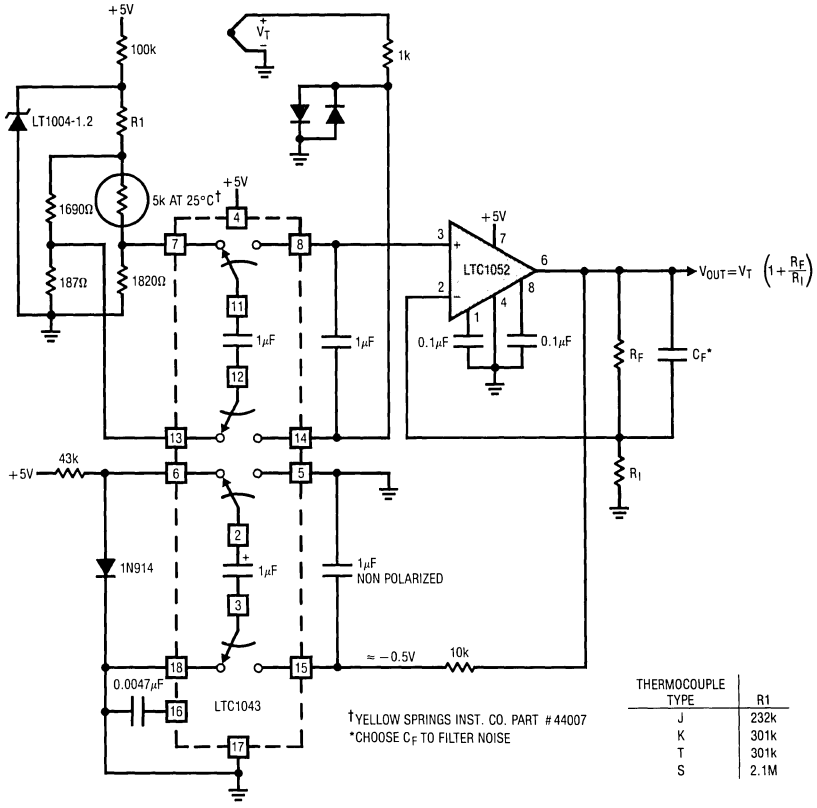
Increasing Output Current



LOAD	OUTPUT SWING
5k	±4.92V
2.5k	±4.84V
1k	±4.65V
220Ω	±3.65V

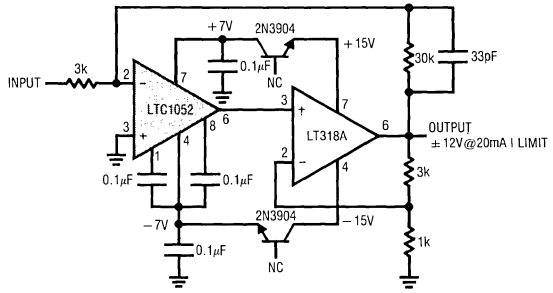
TYPICAL APPLICATIONS

Single +5V Thermocouple Amplifier with Cold Junction Compensation

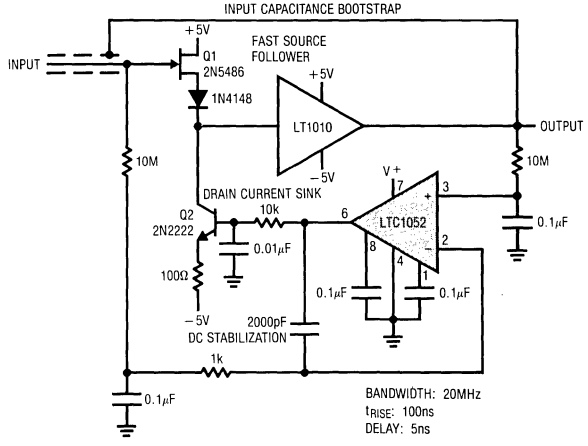


THERMOCOUPLE TYPE	R1
J	232k
K	301k
T	301k
S	2.1M

Increasing Output Current and Voltage ($V_{SUPPLY} = \pm 15V$)

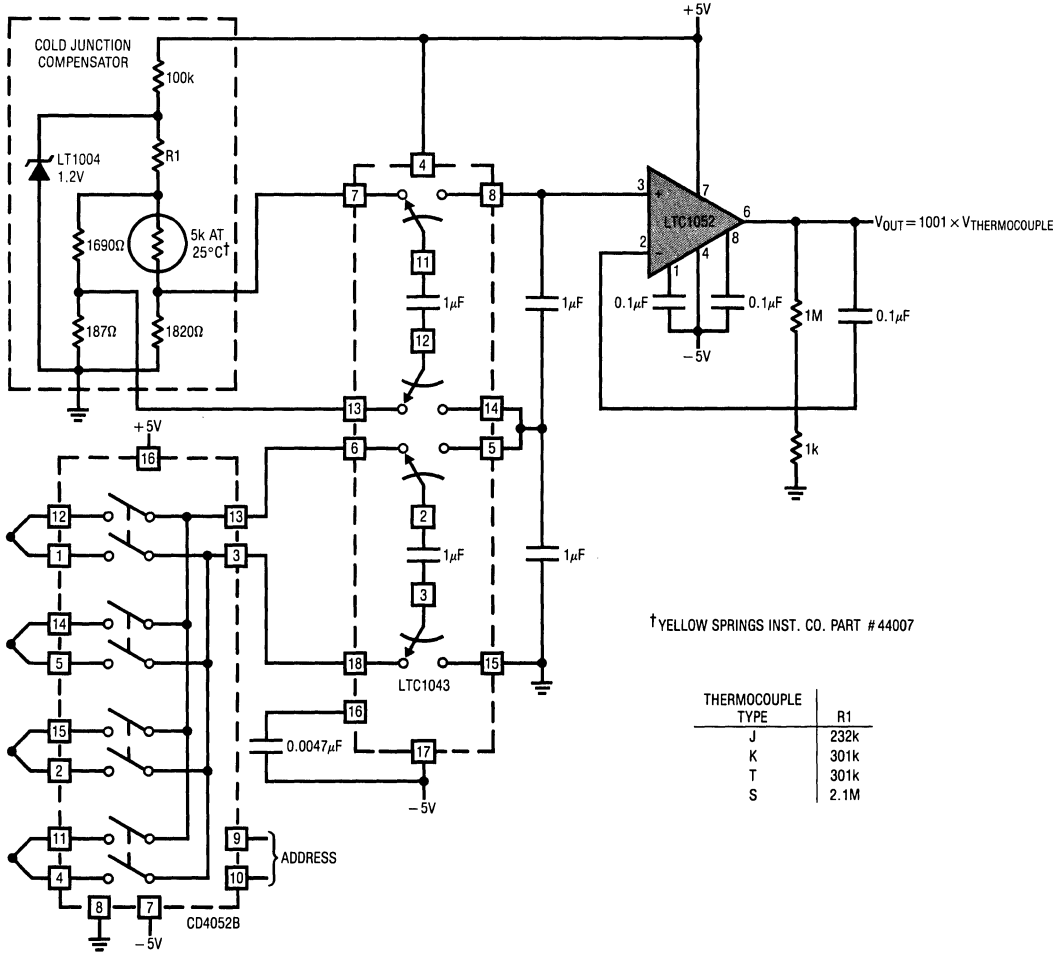


DC Stabilized FET Probe



TYPICAL APPLICATIONS

Precision Multiplexed Differential Thermocouple Amplifier

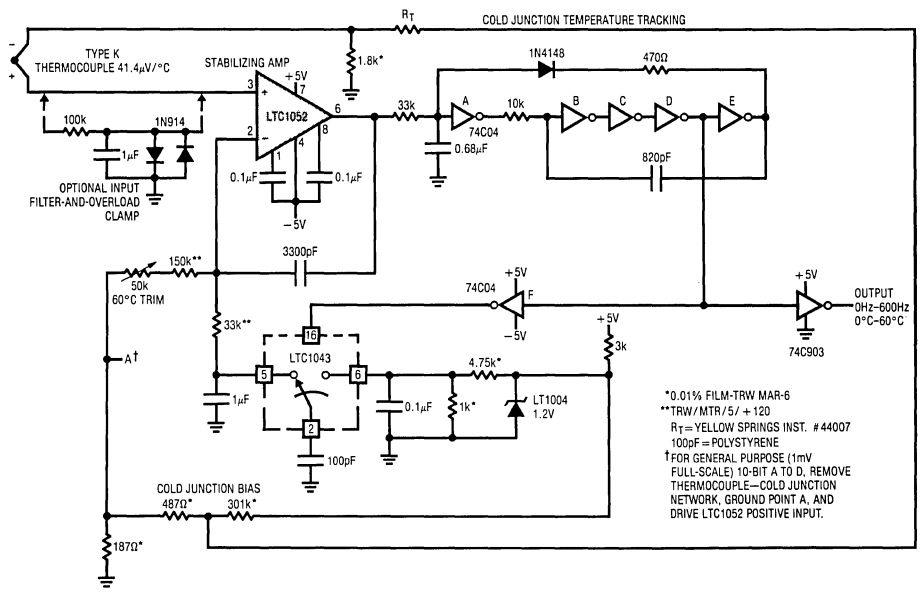


†YELLOW SPRINGS INST. CO. PART #44007

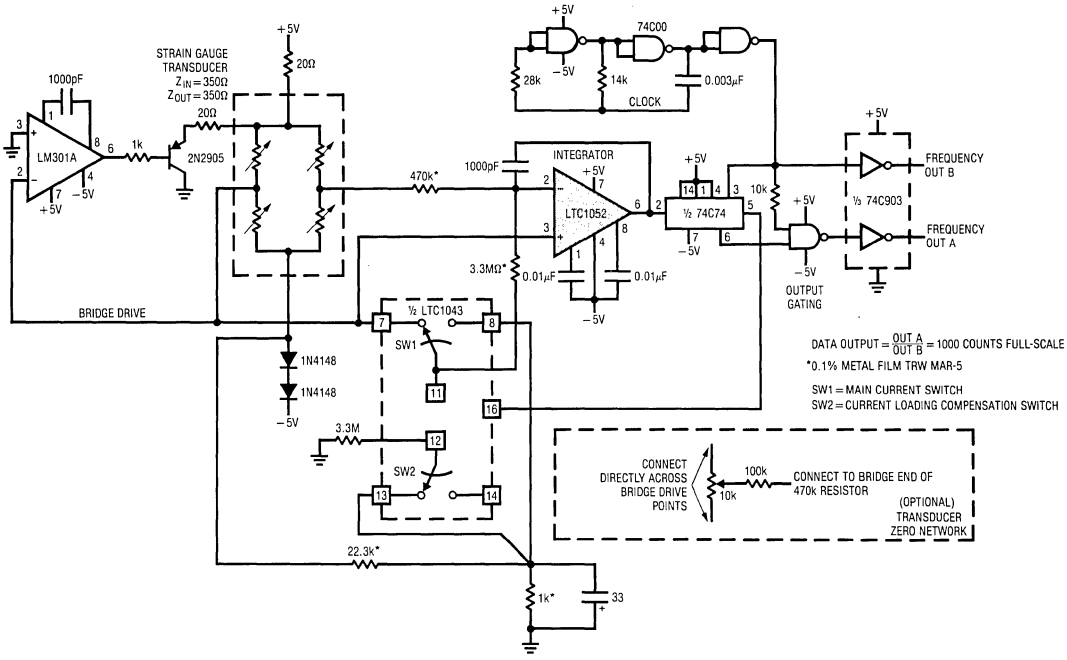
THERMOCOUPLE TYPE	R1
J	232k
K	301k
T	301k
S	2.1M

TYPICAL APPLICATIONS

Direct Thermocouple-to-Frequency Converter

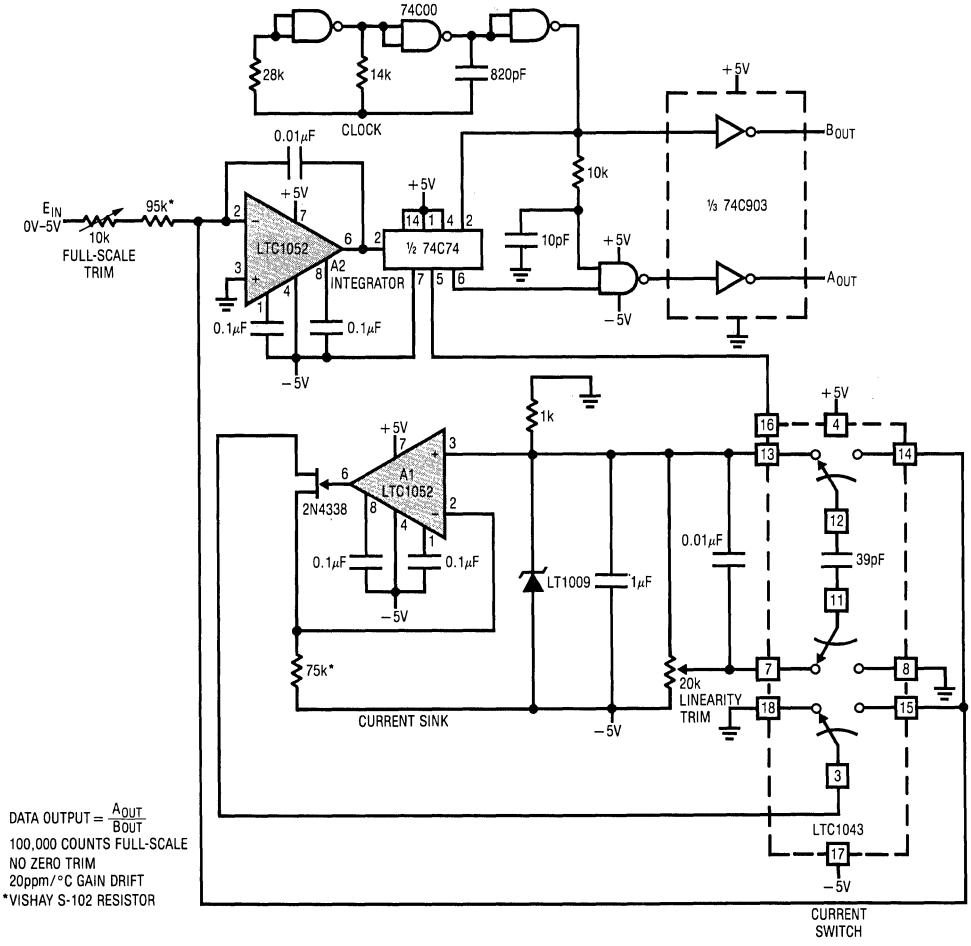


Direct 10-Bit Strain Gauge Digitizer



TYPICAL APPLICATIONS

16-Bit A → D Converter

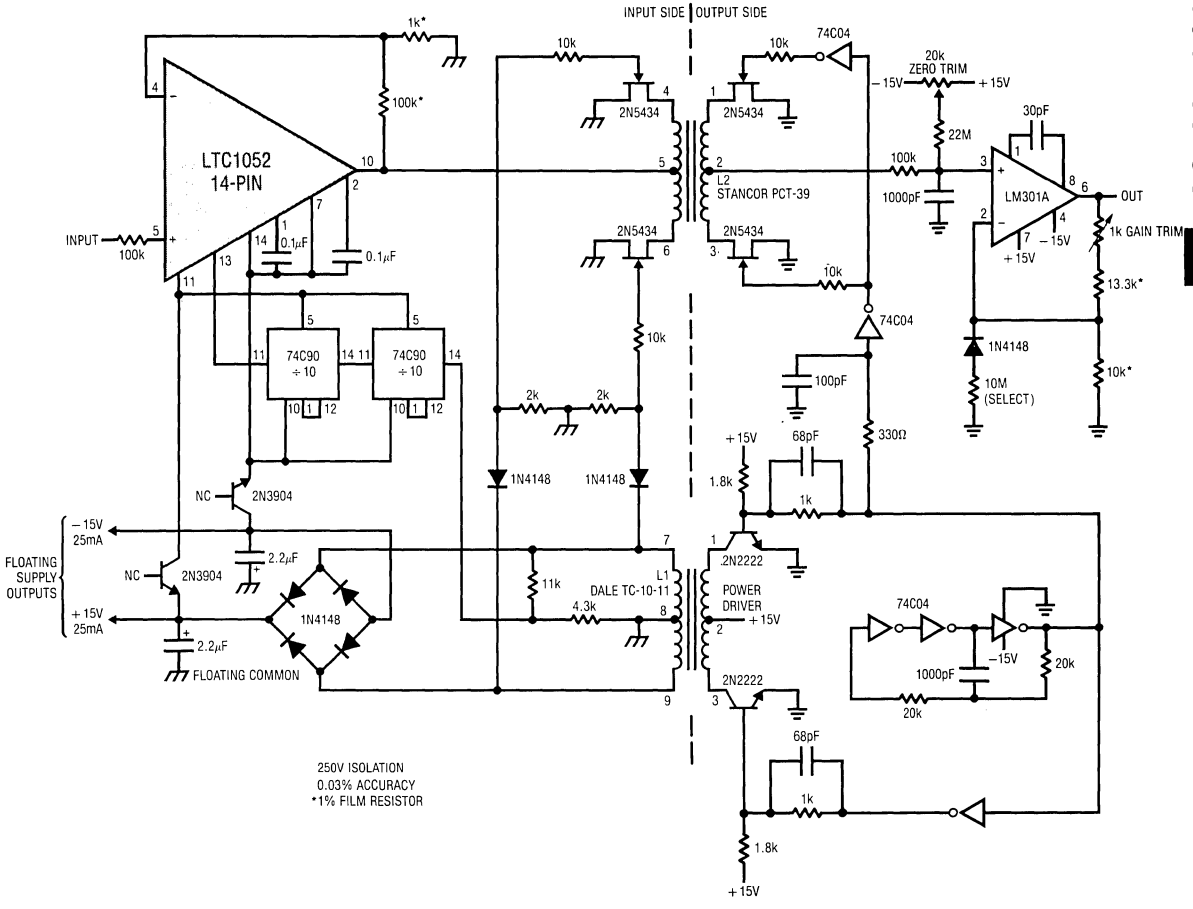


$$\text{DATA OUTPUT} = \frac{A_{OUT}}{B_{OUT}}$$

100,000 COUNTS FULL-SCALE
NO ZERO TRIM
20ppm/°C GAIN DRIFT
*VISHAY S-102 RESISTOR

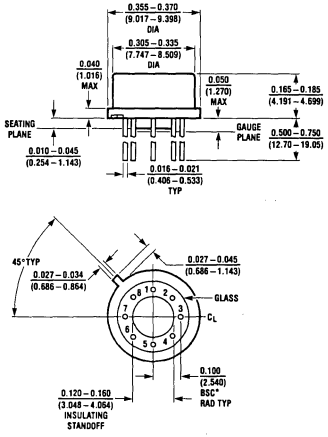
TYPICAL APPLICATIONS

Precision Isolation Amplifier



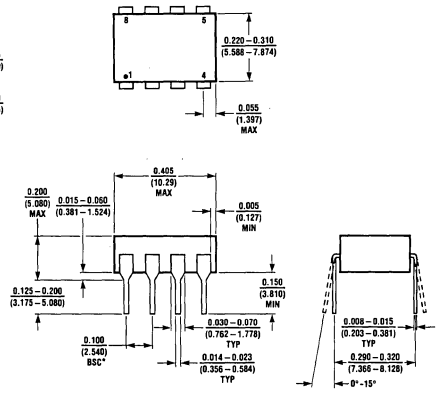
PACKAGE DESCRIPTION Dimensions in inches (millimeters) unless otherwise noted.

H Package
Metal Can



T_{jmax}	Θ_{jA}	Θ_{jc}
150°C	150°C/W	45°C/W

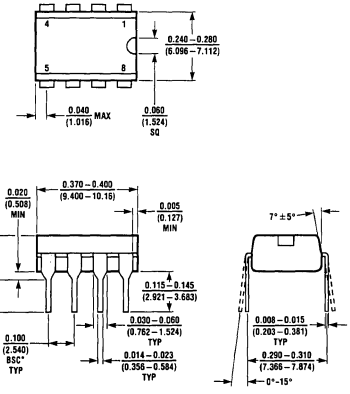
J8 Package
8 Lead Hermetic Dip



*LEADS WITHIN 0.007 OF TRUE POSITION (TP) AT GAUGE PLANE

T_{jmax}	Θ_{jA}
150°C	100°C/W

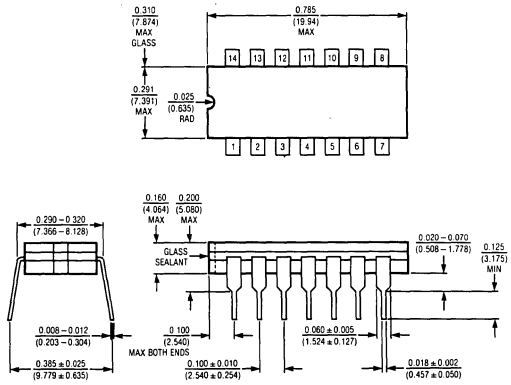
N8 Package
8 Lead Plastic



*LEADS WITHIN 0.007 OF TRUE POSITION (TP) AT GAUGE PLANE.

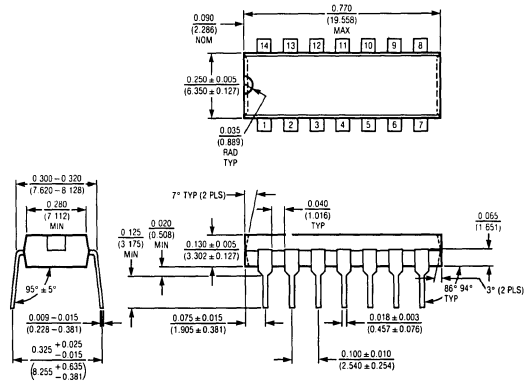
T_{jmax}	Θ_{jA}
110°C	150°C/W

J Package
14-Lead Hermetic DIP



T_{jmax}	Θ_{jA}
150°C	80°C/W

N Package
14-Lead Plastic



T_{jmax}	Θ_{jA}
110°C	130°C/W

Precision, High Speed, JFET Input Operational Amplifiers

FEATURES

- *Guaranteed* Offset Voltage — 150μV Max.
  - −55°C to +125°C — 500μV Max.
- *Guaranteed* Drift — 4μV/°C Max.
- *Guaranteed* Bias Current
  - 70°C — 150pA Max.
  - 125°C — 2.5nA Max.
- *Guaranteed* Slew Rate — 12V/μs Min.

APPLICATIONS

- Precision, High Speed Instrumentation
- Logarithmic Amplifiers
- D/A Output Amplifiers
- Photodiode Amplifiers
- Voltage to Frequency Converters
- Frequency to Voltage Converters
- Fast, Precision Sample and Hold

DESCRIPTION

The LT1055/1056 JFET input operational amplifiers combine precision specifications with high speed performance.

For the first time, 16V/μs slew rate and 6.5MHz gain-bandwidth product are simultaneously achieved with offset voltage of typically 50μV, 1.2μV/°C drift, bias currents of 40pA at 70°C and 500pA at 125°C.

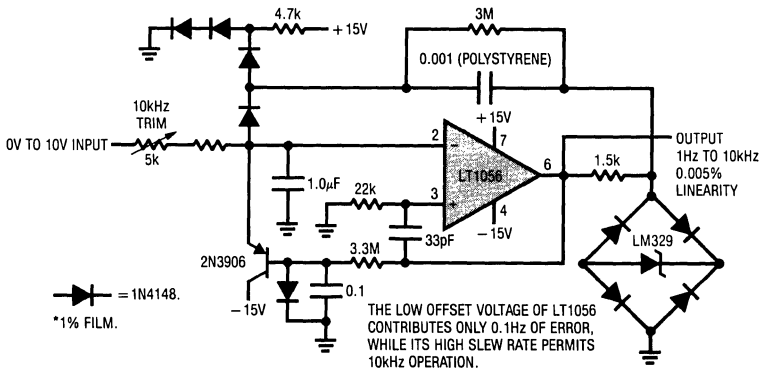
The 150μV maximum offset voltage specification is the best available on any JFET input operational amplifier.

The LT1055 and LT1056 are differentiated by their operating currents. The lower power dissipation LT1055 achieves lower bias and offset currents and offset voltage. The additional power dissipation of the LT1056 permits higher slew rate, bandwidth and faster settling time with a slight sacrifice in DC performance.

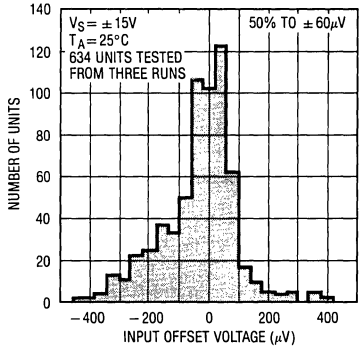
The voltage to frequency converter shown below is one of the many applications which utilize both the precision and high speed of the LT1055/1056.

For a JFET input op amp with 23V/μs guaranteed slew rate, refer to the LT1022 data sheet.

0 to 10kHz Voltage-to-Frequency Converter



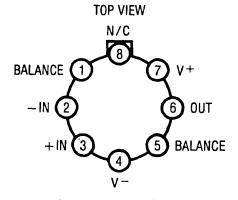
Distribution of Input Offset Voltage (H Package)



ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... ±20V
Differential Input Voltage ..... ±40V
Input Voltage ..... ±20V
Output Short Circuit Duration ..... Indefinite
Operating Temperature Range
LT1055AM/1055M/1056AM/1056M ..... −55°C to 125°C
LT1055AC/1055C/1056AC/1056C ... 0°C to 70°C
Storage Temperature Range
All Devices ..... −65°C to 150°C
Lead Temperature (Soldering, 10 sec.)..... 300°C

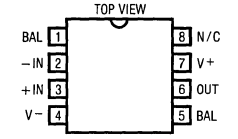
PACKAGE/ORDER INFORMATION



METAL CAN H PACKAGE

ORDER PART NUMBER

LT1055AMH LT1056AMH
LT1055MH LT1056MH
LT1055ACH LT1056ACH
LT1055CH LT1056CH



PLASTIC DIP N8 PACKAGE

LT1055CN8
LT1056CN8

ELECTRICAL CHARACTERISTICS $V_S = \pm 15V$, $T_A = 25°C$, $V_{CM} = 0V$ unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	LT1055AM/1056AM LT1055AC/1056AC MIN	TYP	MAX	LT1055M/1056M LT1055CH/1056CH LT1055CN8/1056CN8 MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage (Note 1)	LT1055 H Package	—	50	150	—	70	400	μV
		LT1056 H Package	—	50	180	—	70	450	μV
		LT1055 N8 Package	—	—	—	—	120	700	μV
		LT1056 N8 Package	—	—	—	—	140	800	μV
I_{OS}	Input Offset Current	Fully Warmed Up	—	2	10	—	2	20	pA
I_B	Input Bias Current	Fully Warmed Up	—	±10	±50	—	±10	±50	pA
		$V_{CM} = +10V$	—	+30	+100	—	+30	+150	pA
	Input Resistance—Differential		—	10^{12}	—	—	10^{12}	—	Ω
	—Common-Mode	$V_{CM} = -11V$ to $+8V$	—	10^{12}	—	—	10^{12}	—	Ω
		$V_{CM} = +8V$ to $+11V$	—	10^{11}	—	—	10^{11}	—	Ω
	Input Capacitance		—	4	—	—	4	—	pF
e_n	Input Noise Voltage	0.1 Hz to 10 Hz LT1055	—	1.8	—	—	2.0	—	μVp-p
		LT1056	—	2.5	—	—	2.8	—	μVp-p
e_n	Input Noise Voltage Density	$f_O = 10Hz$ (Note 2)	—	28	50	—	30	60	nV/√Hz
		$f_O = 1kHz$ (Note 3)	—	14	20	—	15	22	nV/√Hz
I_n	Input Noise Current Density	$f_O = 10Hz$, 1kHz (Note 4)	—	1.8	4	—	1.8	4	fA/√Hz
A_{VOL}	Large Signal Voltage Gain	$V_O = \pm 10V$ $R_L = 2k$	150	400	—	120	400	—	V/mV
		$R_L = 1k$	130	300	—	100	300	—	V/mV
	Input Voltage Range		±11	±12	—	±11	±12	—	V
CMRR	Common-Mode Rejection Ratio	$V_{CM} = \pm 11V$	86	100	—	83	98	—	dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 10V$ to $\pm 18V$	90	106	—	88	104	—	dB
V_{OUT}	Output Voltage Swing	$R_L = 2k$	±12	±13.2	—	±12	±13.2	—	V
SR	Slew Rate	LT1055	10	13	—	7.5	12	—	V/μs
		LT1056	12	16	—	9.0	14	—	V/μs
GBW	Gain Bandwidth Product	f = 1MHz LT1055	—	5.0	—	—	4.5	—	MHz
		LT1056	—	6.5	—	—	5.5	—	MHz
I_S	Supply Current	LT1055	—	2.8	4.0	—	2.8	4.0	mA
		LT1056	—	5.0	6.5	—	5.0	7.0	mA
	Offset Voltage Adjustment Range	$R_{POT} = 100k$	—	±5	—	—	±5	—	mV

ELECTRICAL CHARACTERISTICS $V_S = \pm 15V$, $V_{CM} = 0V$, $0°C \le T_A \le 70°C$ unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		LT1055AC LT1056AC MIN	LT1055AC LT1056AC TYP	LT1055AC LT1056AC MAX	LT1055CH/1056CH LT1055CN8/1056CN8 MIN	LT1055CH/1056CH LT1055CN8/1056CN8 TYP	LT1055CH/1056CH LT1055CN8/1056CN8 MAX	UNITS
V_{OS}	Input Offset Voltage (Note 1)	LT1055 H Package	●	—	100	330	—	140	750	μV
		LT1056 H Package	●	—	100	360	—	140	800	μV
		LT1055 N8 Package	●	—	—	—	—	250	1250	μV
		LT1056 N8 Package	●	—	—	—	—	280	1350	μV
	Average Temperature Coefficient of Input Offset Voltage	H Package (Note 5)	●	—	1.2	4.0	—	1.6	8.0	μV/°C
		N8 Package (Note 5)	●	—	—	—	—	3.0	12.0	μV/°C
I_{OS}	Input Offset Current	Warmed Up LT1055	●	—	10	50	—	16	80	pA
		$T_A = 70°C$ LT1056	●	—	14	70	—	18	100	pA
I_B	Input Bias Current	Warmed Up LT1055	●	—	±30	±150	—	±40	±200	pA
		$T_A = 70°C$ LT1056	●	—	±40	±180	—	±50	±240	pA
A_{VOL}	Large Signal Voltage Gain	$V_O = \pm 10V$, $R_L = 2k$	●	80	250	—	60	250	—	V/mV
CMRR	Common-Mode Rejection Ratio	$V_{CM} = \pm 10.5V$	●	85	100	—	82	98	—	dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 10V$ to $\pm 18V$	●	89	105	—	87	103	—	dB
V_{OUT}	Output Voltage Swing	$R_L = 2k$	●	±12	±13.1	—	±12	±13.1	—	V

ELECTRICAL CHARACTERISTICS $V_S = \pm 15V$, $V_{CM} = 0V$, $-55°C \le T_A \le 125°C$ unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		LT1055AM LT1056AM MIN	LT1055AM LT1056AM TYP	LT1055AM LT1056AM MAX	LT1055M LT1056M MIN	LT1055M LT1056M TYP	LT1055M LT1056M MAX	UNITS
V_{OS}	Input Offset Voltage (Note 1)	LT1055	●	—	180	500	—	250	1200	μV
		LT1056	●	—	180	550	—	250	1250	μV
	Average Temperature Coefficient of Input Offset Voltage	(Note 5)	●	—	1.3	4.0	—	1.8	8.0	μV/°C
I_{OS}	Input Offset Current	Warmed Up LT1055	●	—	0.20	1.2	—	0.25	1.8	nA
		$T_A = 125°C$ LT1056	●	—	0.25	1.5	—	0.30	2.4	nA
I_B	Input Bias Current	Warmed Up LT1055	●	—	±0.4	±2.5	—	±0.5	±4.0	nA
		$T_A = 125°C$ LT1056	●	—	±0.5	±3.0	—	±0.6	±5.0	nA
A_{VOL}	Large Signal Voltage Gain	$V_O = \pm 10V$, $R_L = 2k$	●	40	120	—	35	120	—	V/mV
CMRR	Common-Mode Rejection Ratio	$V_{CM} = \pm 10.5V$	●	85	100	—	82	98	—	dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 10V$ to $\pm 17V$	●	88	104	—	86	102	—	dB
V_{OUT}	Output Voltage Swing	$R_L = 2k$	●	±12	±12.9	—	±12	±12.9	—	V

The ● denotes the specifications which apply over the full operating temperature range.

For MIL-STD components, please refer to LTC883 data sheet for test listing and parameters.

Note 1: Offset voltage is measured under two different conditions: (a) approximately 0.5 seconds after application of power; (b) at $T_A = 25°C$ only, with the chip heated to approximately 38°C for the LT1055 and to 45°C for the LT1056, to account for chip temperature rise when the device is fully warmed up.

Note 2: 10Hz noise voltage density is sample tested on every lot of A grades. Devices 100% tested at 10Hz are available on request.

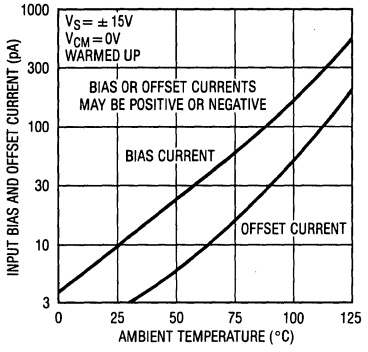
Note 3: This parameter is tested on a sample basis only.

Note 4: Current noise is calculated from the formula: $i_n = (2qI_B)^{1/2}$, where $q = 1.6 \times 10^{-19}$ coulomb. The noise of source resistors up to 1GΩ swamps the contribution of current noise.

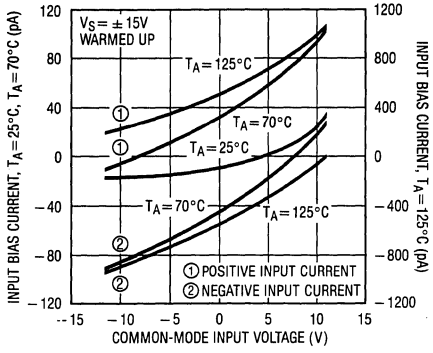
Note 5: Offset voltage drift with temperature is practically unchanged when the offset voltage is trimmed to zero with a 100k potentiometer between the balance terminals and the wiper tied to V^+. Devices tested to tighter drift specifications are available on request.

TYPICAL PERFORMANCE CHARACTERISTICS

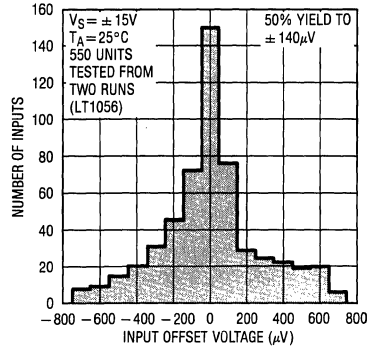
Input Bias and Offset Currents vs Temperature



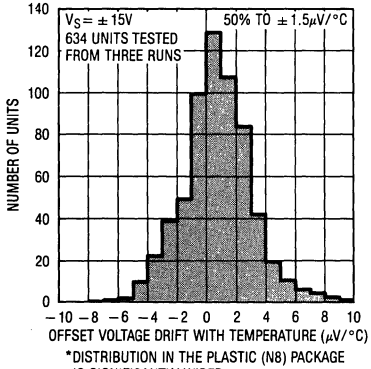
Input Bias Current Over the Common-Mode Range



Distribution of Input Offset Voltage (N8 Package)

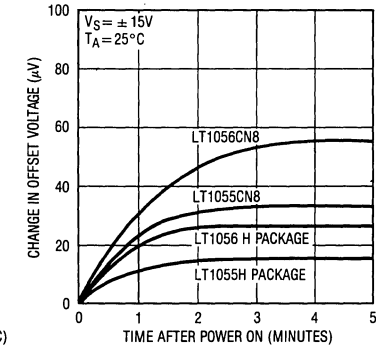


Distribution of Offset Voltage Drift with Temperature (H Package)*

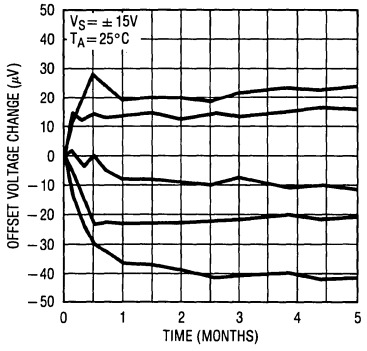


*DISTRIBUTION IN THE PLASTIC (N8) PACKAGE IS SIGNIFICANTLY WIDER.

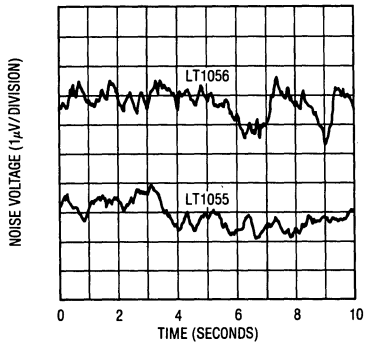
Warm-Up Drift



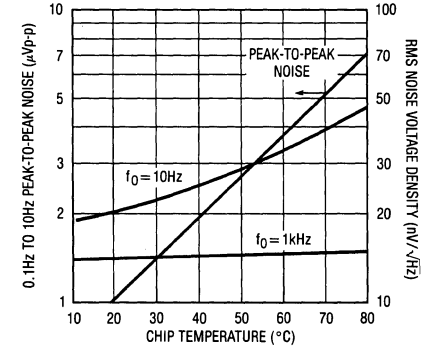
Long Term Drift of Representative Units



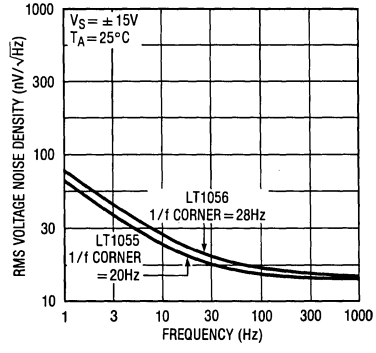
0.1Hz to 10Hz Noise



Noise vs Chip Temperature

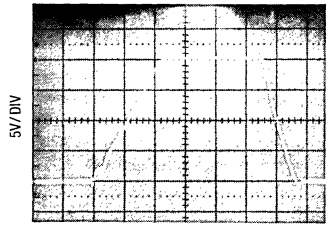


Voltage Noise vs Frequency



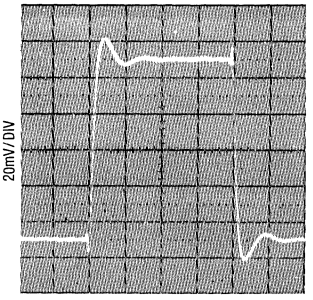
TYPICAL PERFORMANCE CHARACTERISTICS

LT1056 Large Signal Response



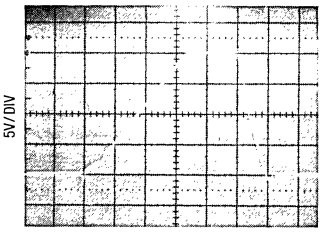
$A_V = +1$, $C_L = 100pF$, $0.5\mu s/DIV$

Small Signal Response



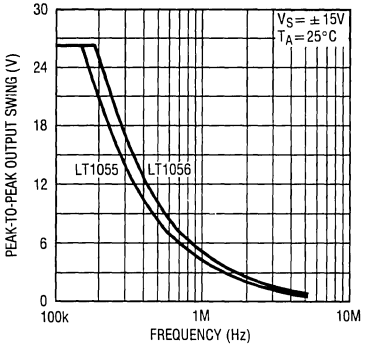
$A_V = +1$, $C_L = 100pF$, $0.2\mu s/DIV$

LT1055 Large Signal Response

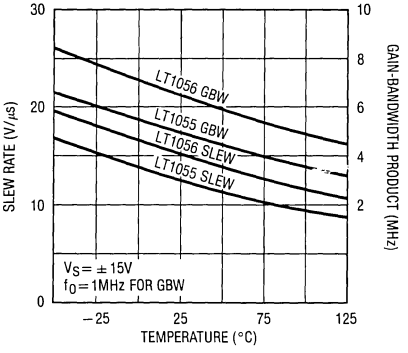


$A_V = 1$, $C_L = 100pF$, $0.5\mu s/DIV$

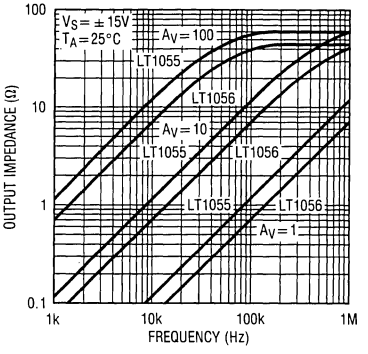
Undistorted Output Swing vs Frequency



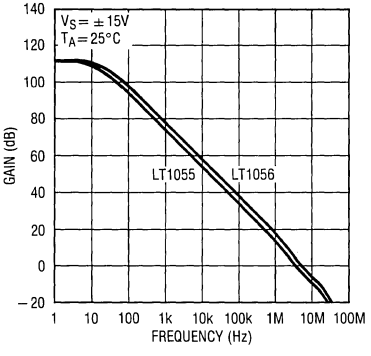
Slew Rate, Gain-Bandwidth vs Temperature



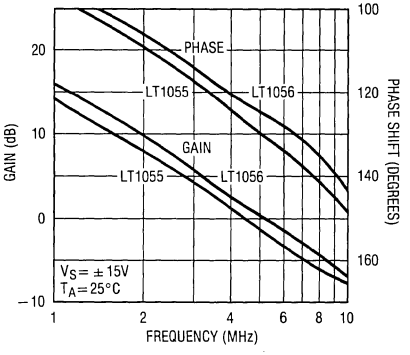
Output Impedance vs Frequency



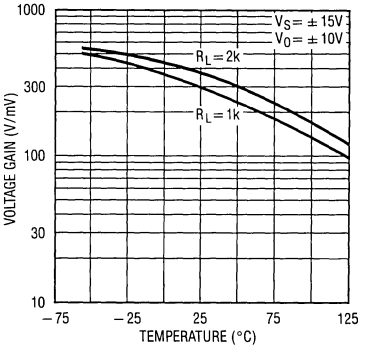
Gain vs Frequency



Gain, Phase Shift vs Frequency

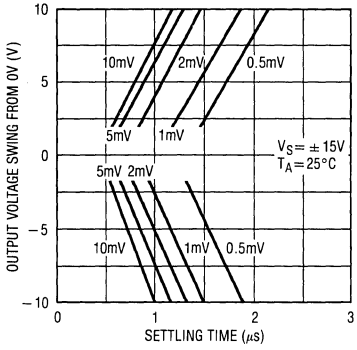


Voltage Gain vs Temperature

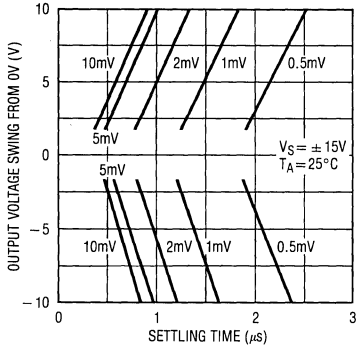


TYPICAL PERFORMANCE CHARACTERISTICS

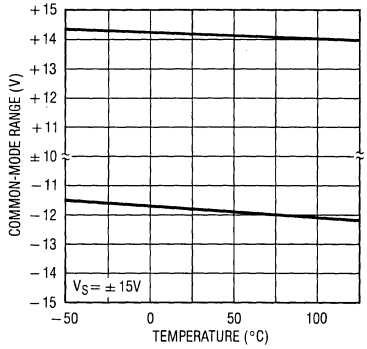
LT1055 Settling Time



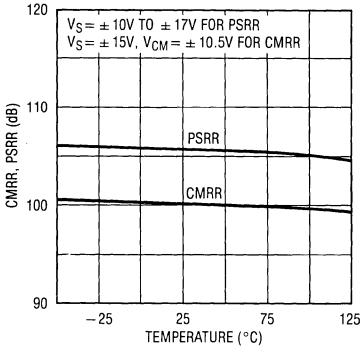
LT1056 Settling Time



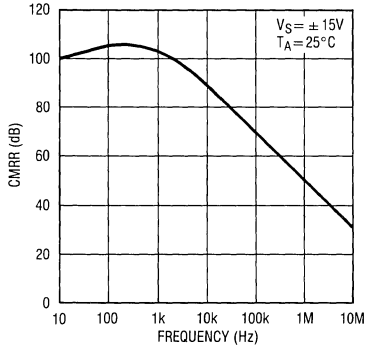
Common-Mode Range vs Temperature



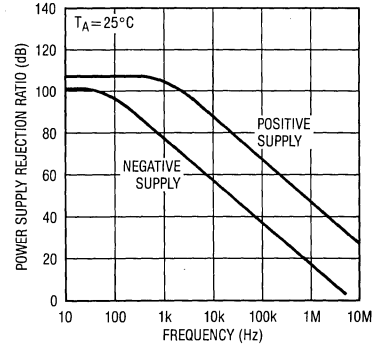
Common-Mode and Power Supply Rejections vs Temperature



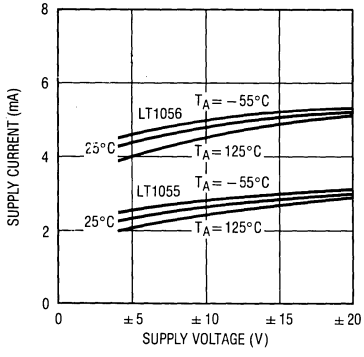
Common-Mode Rejection Ratio vs Frequency



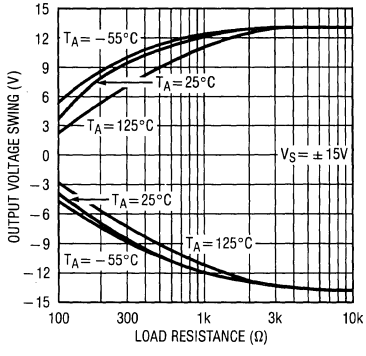
Power Supply Rejection Ratio vs Frequency



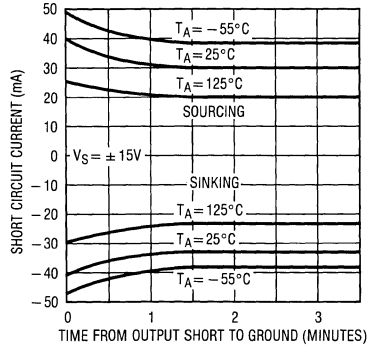
Supply Current vs Supply Voltage



Output Swing vs Load Resistance



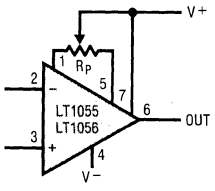
Short Circuit Current vs Time



APPLICATIONS INFORMATION

The LT1055/1056 may be inserted directly into LF155A/355A, LF156A/356A, OP-15 and OP-16 sockets. Offset nulling will be compatible with these devices with the wiper of the potentiometer tied to the positive supply.

Offset Nulling



No appreciable change in offset voltage drift with temperature will occur when the device is nulled with a potentiometer, R_P, ranging from 10k to 200k.

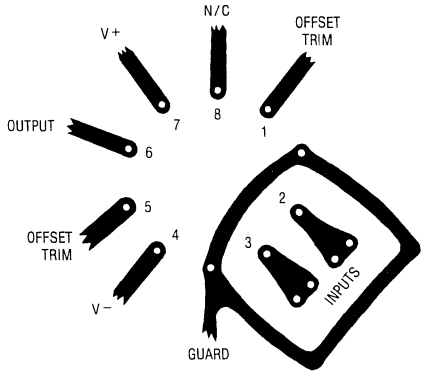
The LT1055/1056 can also be used in LF351, LF411, AD547, AD611, OPA-111, and TL081 sockets, provided that the nulling circuitry is removed. Because of the LT1055/1056's low offset voltage, nulling will not be necessary in most applications.

Achieving Picoampere/Microvolt Performance

In order to realize the picoampere-microvolt level accuracy of the LT1055/1056 proper care must be exercised. For example, leakage currents in circuitry external to the op amp can significantly degrade performance. High quality insulation should be used (e.g. Teflon™, Kel-F); cleaning of all insulating surfaces to remove fluxes and other residues will probably be required. Surface coating may be necessary to provide a moisture barrier in high humidity environments.

Board leakage can be minimized by encircling the input circuitry with a guard ring operated at a potential close to that of the inputs: in inverting configurations the guard ring should be tied to ground, in non-inverting connections to the inverting input at pin 2. Guarding both sides of the printed circuit board is required. Bulk leakage reduction depends on the guard ring width.

Teflon™ is a trademark of DuPont.



The LT1055/1056 has the lowest offset voltage of any JFET input op amp available today. However, the offset voltage and its drift with time and temperature are still not as good as on the best bipolar amplifiers because the transconductance of FETs is considerably lower than that of bipolar transistors. Conversely, this lower transconductance is the main cause of the significantly faster speed performance of FET input op amps.

Offset voltage also changes somewhat with temperature cycling. The AM grades show a typical 20μV hysteresis (30μV on the M grades) when cycled over the $-55°C$ to $125°C$ temperature range. Temperature cycling from $0°C$ to $70°C$ has a negligible (less than 10μV) hysteresis effect.

The offset voltage and drift performance are also affected by packaging. In the plastic N8 package the molding compound is in direct contact with the chip, exerting pressure on the surface. While NPN input transistors are largely unaffected by this pressure, JFET device matching and drift are degraded. Consequently, for best DC performance, as shown in the typical performance distribution plots, the TO-5 H package is recommended.

Noise Performance

The current noise of the LT1055/1056 is practically immeasurable at $1.8fA/\sqrt{Hz}$. At $25°C$ it is negligible up to $1G\Omega$ of source resistance, R_S (compared to the noise of R_S). Even at $125°C$ it is negligible to $100M\Omega$ of R_S.

APPLICATIONS INFORMATION

The voltage noise spectrum is characterized by a low 1/f corner in the 20Hz to 30Hz range, significantly lower than on other competitive JFET input op amps. Of particular interest is the fact that, with any JFET IC amplifier, the frequency location of the 1/f corner is proportional to the square root of internal gate leakage currents and, therefore, noise doubles every 20°C. Furthermore, as illustrated in the noise versus chip temperature curves, the 0.1Hz to 10Hz peak-to-peak noise is a strong function of temperature, while wideband noise ($f_O = 1kHz$) is practically unaffected by temperature.

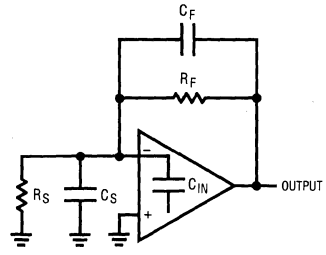
Consequently, for optimum low frequency noise, chip temperature should be minimized. For example, operating an LT1056 at ±5V supplies or with a 20°C/W case-to-ambient heat sink reduces 0.1Hz to 10Hz noise from typically 2.5μVp-p (±15V, free-air) to 1.5μVp-p. Similarly, the noise of an LT1055 will be 1.8μVp-p typically because of its lower power dissipation and chip temperature.

High Speed Operation

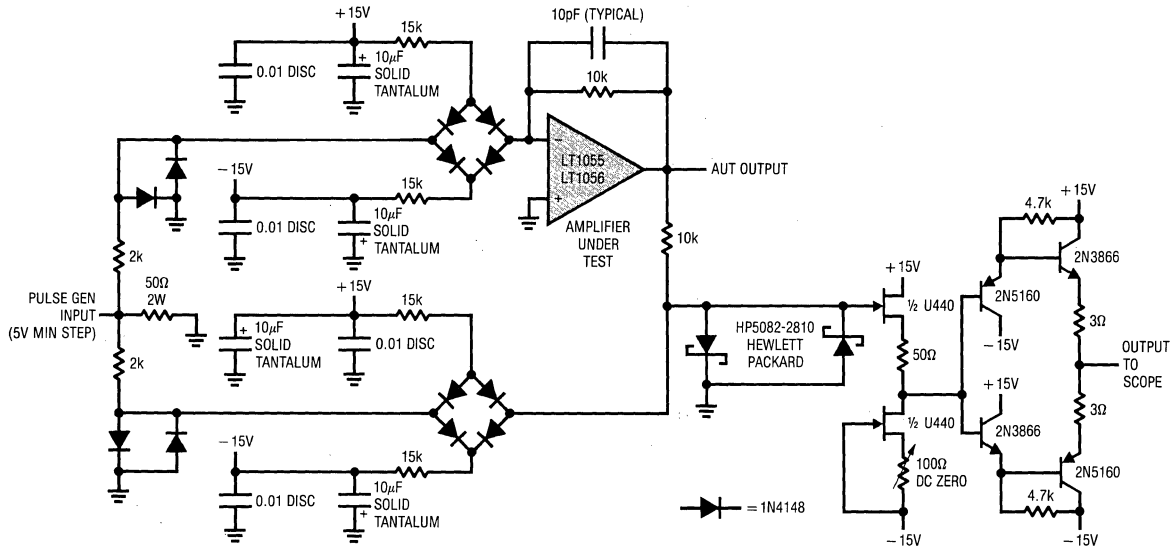
Settling time is measured in the test circuit shown. This test configuration has two features which eliminate problems common to settling time measurements: (1) probe capacitance is isolated from the "false summing" node, and (2) it does not require a "flat top" input pulse since the input pulse is merely used to steer current through the diode bridges. For more details, please see Application Note 10.

As with most high speed amplifiers, care should be taken with supply decoupling, lead dress and component placement.

When the feedback around the op amp is resistive (R_F), a pole will be created with R_F, the source resistance and capacitance (R_S, C_S), and the amplifier input capacitance ($C_{IN} \approx 4pF$). In low closed loop gain configurations and with R_S and R_F in the kilohm range, this pole can create excess phase shift and even oscillation. A small capacitor (C_F) in parallel with R_F eliminates this problem. With $R_S(C_S + C_{IN}) = R_F C_F$, the effect of the feedback pole is completely removed.



Settling Time Test Circuit

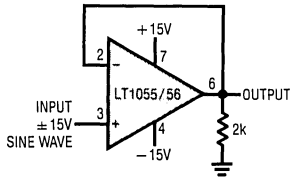


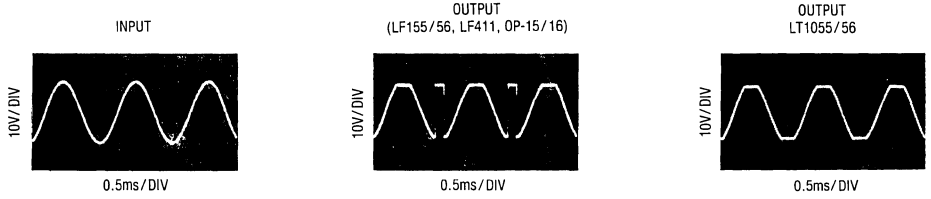
APPLICATIONS INFORMATION

Phase Reversal Protection

Most industry standard JFET input op amps (e.g., LF155/156, LF351, LF411, OP15/16) exhibit phase reversal at the output when the negative common-mode limit at the input is exceeded (i.e., from −12V to −15V with ±15V supplies). This can cause lock-up in servo systems. As shown below, the LT1055/1056 does not have this problem due to unique phase reversal protection circuitry (Q1 on simplified schematic).

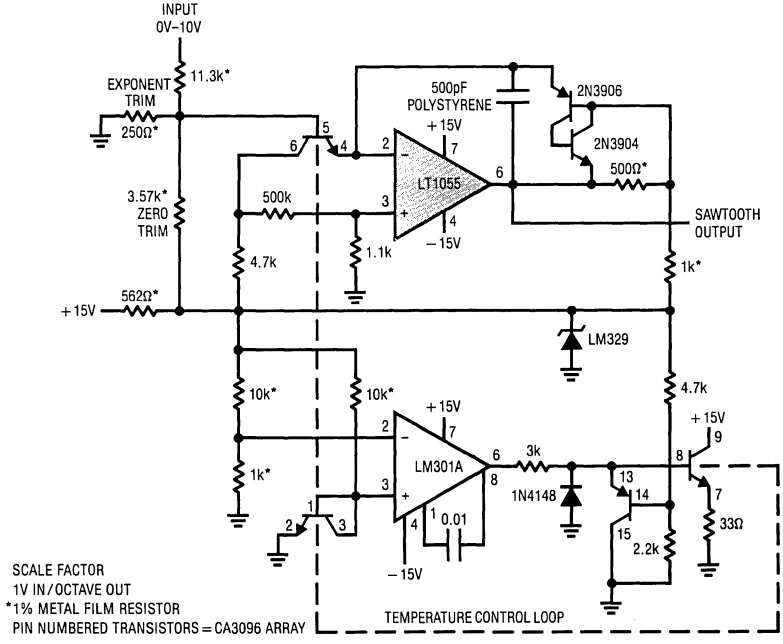
Voltage Follower with Input Exceeding the Negative Common-Mode Range





TYPICAL APPLICATIONS†

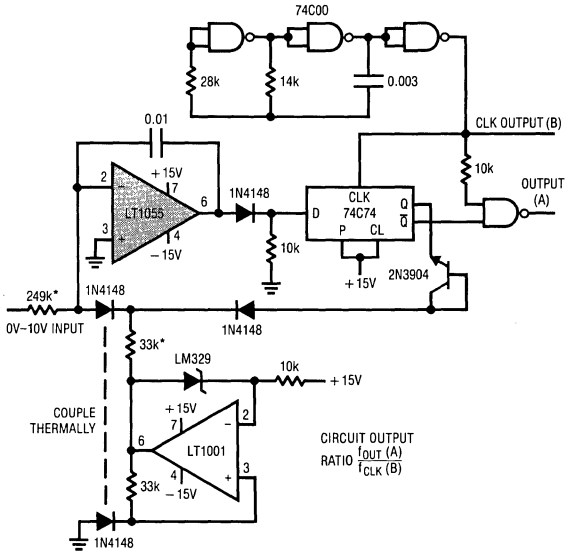
Exponential Voltage-to-Frequency Converter for Music Synthesizers



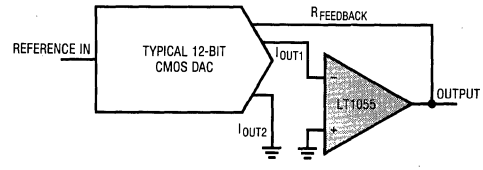
† For ten additional applications utilizing the LT1055 and LT1056, please see the LTC1043 data sheet and Application Note 3.

TYPICAL APPLICATIONS

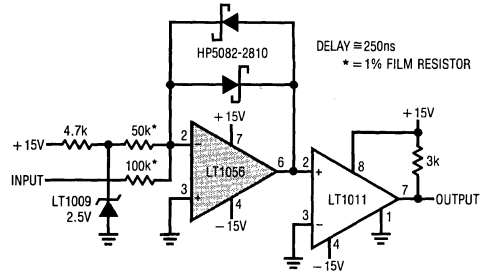
12-Bit Charge Balance Analog-to-Digital Converter



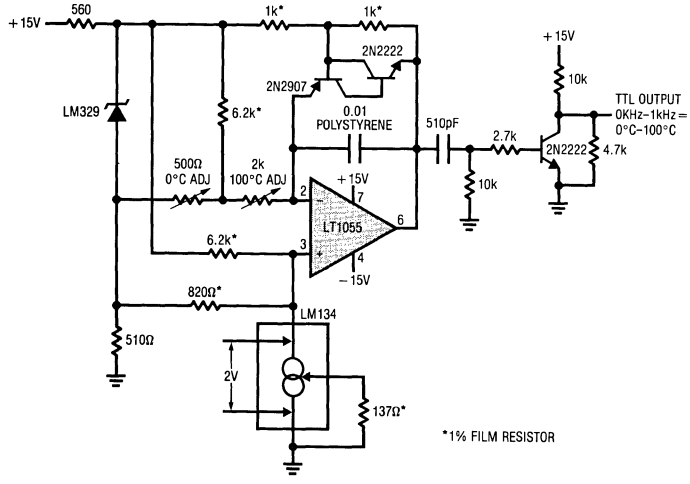
Fast ''No Trims'' 12-Bit Multiplying CMOS DAC Amplifier



Fast, 16-Bit Current Comparator

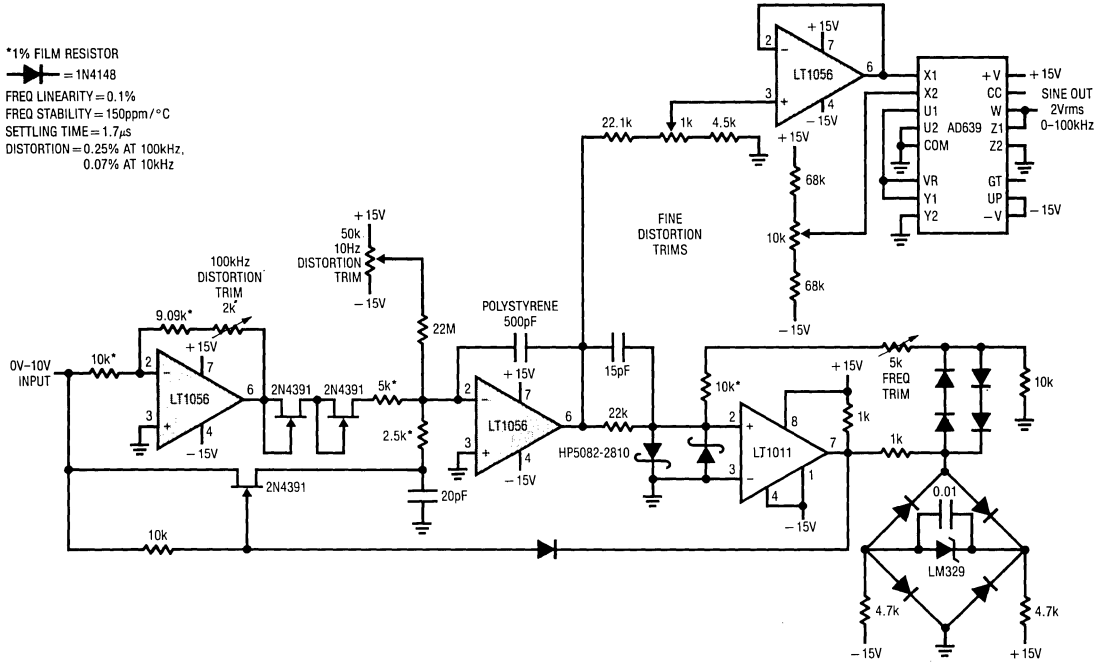


Temperature-to-Frequency Converter

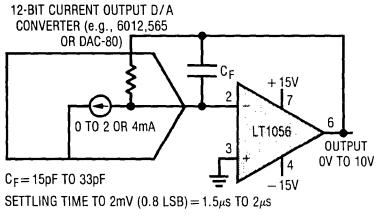


TYPICAL APPLICATIONS

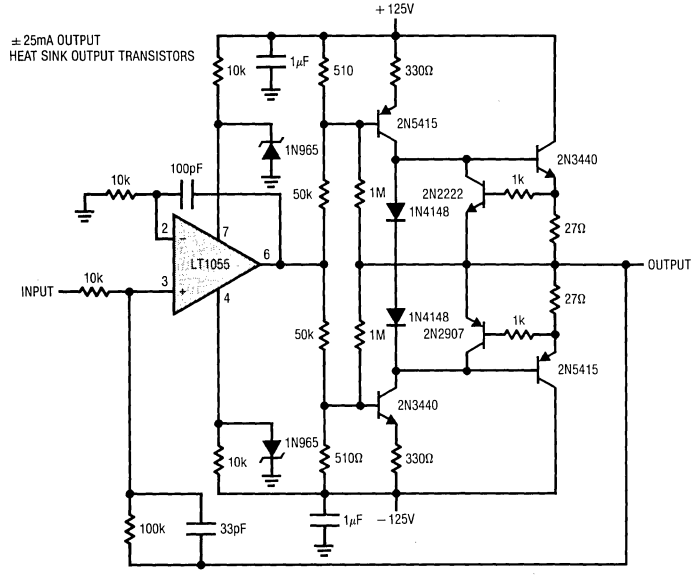
100kHz Voltage Controlled Oscillator



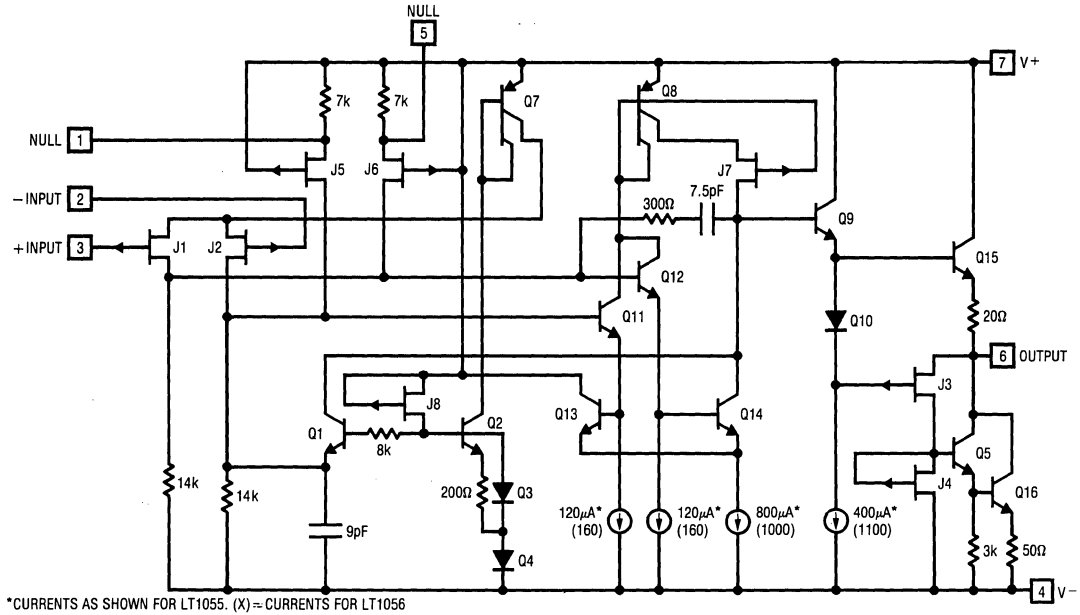
12-Bit Voltage Output D/A Converter



±120V Output Precision Op Amp

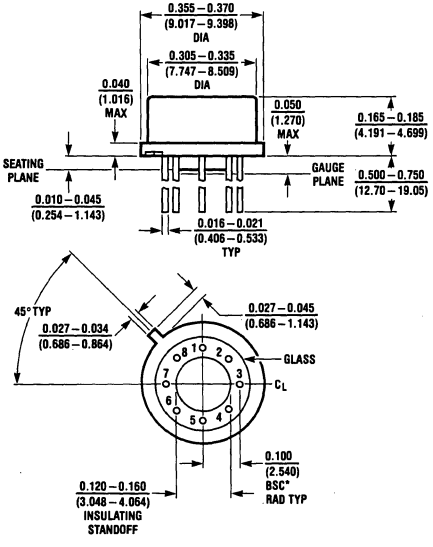


SIMPLIFIED SCHEMATIC



PACKAGE DESCRIPTION

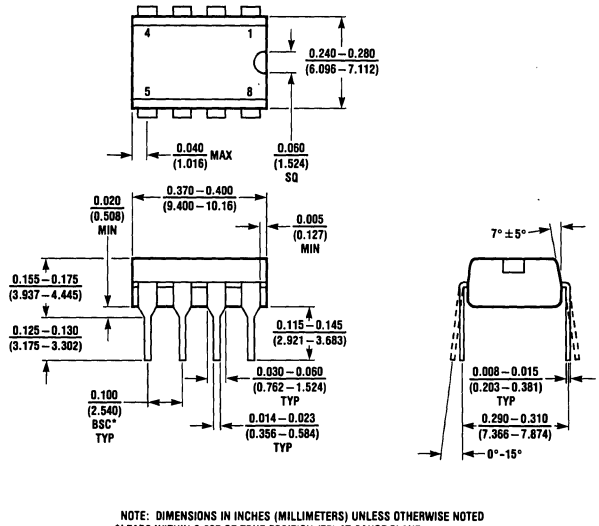
H Package Metal Can



NOTE: DIMENSIONS IN INCHES (MILLIMETERS)

$T_j$max	θ_{ja}	θ_{jc}
150°C	150°C/W	45°C/W

N8 Package
8 Lead Plastic



NOTE: DIMENSIONS IN INCHES (MILLIMETERS) UNLESS OTHERWISE NOTED
*LEADS WITHIN 0.007 OF TRUE POSITION (TP) AT GAUGE PLANE

$T_j$max	θ_{ja}
100°C	130°C/W

JFET-Input Operational Amplifiers
Low Supply Current (LF155)
High Speed (LF156)

FEATURES

- *Guaranteed* Offset Voltage Drift on All Grades
- *Guaranteed* Slew Rate on All Grades
- *Guaranteed* Low Input Offset Current 10pA Max.
- *Guaranteed* Low Input Bias Current 50pA Max.
- *Guaranteed* High Slew Rate (156A/356A) 10V/μs Min.
- Fast Settling to 0.01% 1.5μs

APPLICATIONS

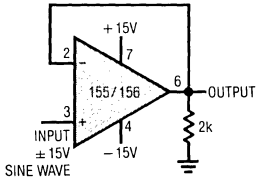
- Output Amplifiers for D/A Converters
- Fast Sample and Hold Circuits
- High Speed Integrators
- Photocell Amplifiers
- High Input Impedance Buffers

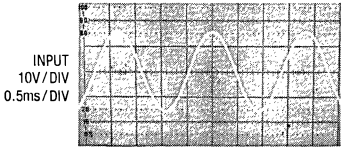
DESCRIPTION

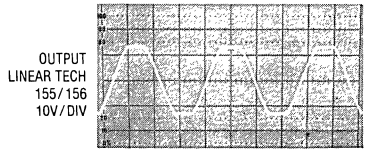
Linear Technology's LF155/156 series features several improvements compared to similar types from other manufacturers: offset voltage drift with temperature and slew rate are guaranteed on all grades, not just on the more expensive "A" grades. Other specifications such as voltage gain and high temperature bias and offset currents are also improved.

The industry standard LF155/156 devices exhibit phase reversal at the output when the negative common-mode limit at the input is exceeded (i.e., from −12V to −15V with ±15V supplies). This can cause lock-up in servo systems. As shown below, Linear Technology's LF155/156 does not have this problem due to unique phase reversal protection circuitry. For applications requiring higher performance, see the LT1055 and LT1056 data sheets.

Voltage Follower with Input Exceeding the Negative Common-Mode Range







ABSOLUTE MAXIMUM RATINGS

Supply Voltage
- LF155A/155/355A, LF156A/156/356A ..... ±22V
- LF355/356 ..... ±18V

Differential Input Voltage
- LF155A/155/156A/156 ..... ±40V
- LF355A/355/356A/356 ..... ±30V

Input Voltage (Note 1)
- LF155A/155/156A/156 ..... ±20V
- LF355A/355/356A/356 ..... ±16V

Output Short Circuit Duration ..... Indefinite

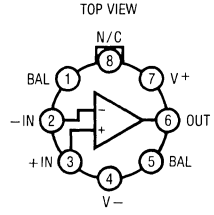
Operating Temperature Range
- LF155A/155/156A/156 ..... −55°C to 125°C
- LF355A/355/356A/356 ..... 0°C to 70°C

Maximum Junction Temperature
- LF155A/155/156A/156 ..... 150°C
- LF355A/355/356A/356 ..... 100°C

Storage Temperature Range
- All Devices ..... −65°C to 150°C

Lead Temperature (Soldering, 10 sec.)..... 300°C

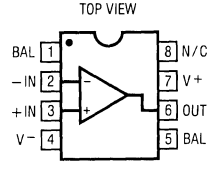
PACKAGE/ORDER INFORMATION



H PACKAGE
METAL CAN

ORDER PART NUMBER

LF155H LF156H
LF155AH LF156AH
LF355H LF356H
LF355AH LF356AH



N8 PACKAGE
8 PIN PLASTIC

LF355N8 LF356N8
LF355AN8 LF356AN8

V_{OS} is adjusted with a 20k or 50k potentiometer between the balance terminals. The wiper is tied to V^+

ELECTRICAL CHARACTERISTICS (Note 2)

SYMBOL	PARAMETER	CONDITIONS		LF155A/156A LF355A/356A MIN	LF155A/156A LF355A/356A TYP	LF155A/156A LF355A/356A MAX	LF155/156 MIN	LF155/156 TYP	LF155/156 MAX	LF355/356 MIN	LF355/356 TYP	LF355/356 MAX	UNITS
V_{OS}	Input Offset Voltage	$T_A = 25°C$			1	2		2	3.5		3	8	mV
		Over Temperature	●			2.5			4.8			9	mV
		355A/356A	●			2.3							mV
$\frac{\Delta V_{OS}}{\Delta T}$	Average TC of Input Offset Voltage	$R_S = 50\Omega$	●		3	5		5	15		5	25	µV/°C
	Change in Average TC with V_{OS} Adjust	$R_S = 50\Omega$ (Note 4)	●		0.5			0.5			0.5		µV/°C per mV
I_{OS}	Input Offset Current	$T_j = 25°C$ (Note 3)			3	10		3	20		3	50	pA
		$T_j \leq 125°C$	●			9			9			—	nA
		$T_j \leq 70°C$	●			0.7			—			1.5	nA
I_B	Input Bias Current	$T_j = 25°C$ (Note 3)			30	50		30	100		30	200	pA
		$T_j \leq 125°C$	●			15			15			—	nA
		$T_j \leq 70°C$	●			0.9						3.0	nA
R_{IN}	Input Resistance	$T_j = 25°C$			10^{12}			10^{12}			10^{12}		Ω
A_{VOL}	Large Signal Voltage Gain	$V_S = \pm 15V$, $T_A = 25°C$, $V_O = \pm 10V$, $R_L = 2k$		75	200		50	200		40	200		V/mV
		Over Temperature	●	30			25			25			V/mV

ELECTRICAL CHARACTERISTICS (Note 2)

SYMBOL	PARAMETER	CONDITIONS		LF155A/156A LF355A/356A			LF155/156			LF355/356			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_O	Output Voltage Swing	$V_S = \pm 15V$, $R_L = 10k$	●	±12	±13		±12	±13		±12	±13		V
		$V_S = \pm 15V$, $R_L = 2k$	●	±10	±12		±10	±12		±10	±12		V
V_{CM}	Input Common-Mode Voltage Range	$V_S = \pm 15V$	●	±11	+15.1 −12		±11	+15.1 −12		±10	+15.1 −12		V
CMRR	Common-Mode Rejection Ratio		●	85	100		85	100		80	100		dB
PSRR	Supply Voltage Rejection Ratio	$V_S = \pm 10V$ to $\pm 18V$	●	85	100		85	100		—	—		dB
		$V_S = \pm 10V$ to $\pm 15V$	●		—			—		80	100		dB
I_S	Supply Current	$T_A = 25°C$, $V_S = \pm 15V$											
		LF155/355 Series			2	4		2	4		2	4	mA
		LF156/356 Series			5	7		5	7		5	10	mA
		LF356A			5	7		—	—		—	—	mA
SR	Slew Rate	$A_V = +1$											
		$T_A = 25°C$, $V_S = \pm 15V$											
		LF155/355 Series		5	7		5	7		2.5	6		V/μs
		LF156/356 Series		10	12		9	12		4	12		V/μs
GBW	Gain Bandwidth Product	$T_A = 25°C$, $V_S = \pm 15V$											
		LF155/355 Series		—	2.5			2.5			2.5		MHz
		LF156/356 Series		4	5			5			5		MHz
t_S	Settling Time to 0.01%	$T_A = 25°C$, $V_S = \pm 15V$											
		LF155 Series (Note 5)			4			4			4		μs
		LF156 Series			1.5			1.5			1.5		μs
e_n	Input Noise Voltage Density	$T_A = 25°C$, $V_S = \pm 15V$											
		f = 100Hz											
		LF155 Series			25			25			25		$nV/\sqrt{Hz}$
		LF156 Series			15			15			15		$nV/\sqrt{Hz}$
		f = 1000Hz											
		LF155 Series			20			20			20		$nV/\sqrt{Hz}$
		LF156 Series			12			12			12		$nV/\sqrt{Hz}$
i_n	Input Noise Current Density	$T_A = 25°C$, $V_S = \pm 15V$											
		f = 100Hz			0.01			0.01			0.01		$pA/\sqrt{Hz}$
		f = 1000Hz			0.01			0.01			0.01		$pA/\sqrt{Hz}$
C_{IN}	Input Capacitance		●		3			3			3		pF

The ● denotes the specifications which apply over the full operating temperature range. The shaded electrical specifications indicate those parameters which have been improved or guaranteed test limits provided for the first time.

For MIL-STD components, please refer to LTC 883C data sheet for test listing and parameters.

Note 1: Unless otherwise specified, the absolute maximum negative input voltage is equal to the negative power supply voltage.

Note 2: Unless otherwise stated, these test conditions apply:

	LF155A/156A LF155/156	LF355A/356A	LF355/356
Supply Voltage, V_S	$\pm 15V \le V_S \le \pm 20V$	$\pm 15V \le V_S \le \pm 18V$	$V_S = \pm 15V$
T_A	$-55°C \le T_A \le +125°C$	$0°C \le T_A \le +70°C$	$0°C \le T_A \le +70°C$

and V_{OS}, I_B and I_{OS} are measured at $V_{CM} = 0$.

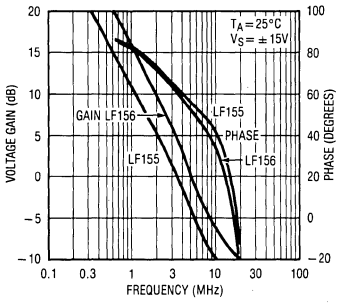
Note 3: The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature, T_j. Due to limited production test time, the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, P_D. $T_j = T_A + \Theta_{JA} P_D$ where Θ_{JA} is the thermal resistance from junction to ambient. Use of a heat sink is recommended if input bias current is to be kept to a minimum.

Note 4: The temperature coefficient of the adjusted input offset voltage changes only a small amount (0.5μV/°C typically) for each mV of adjustment from its original unadjusted value. Common-mode rejection and open loop voltage gain are also unaffected by offset adjustment.

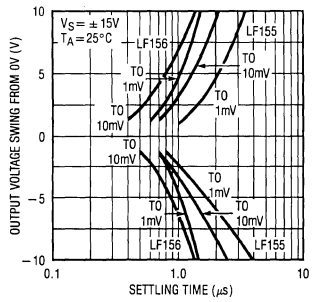
Note 5: Settling time is defined here for a unity gain inverter connection using 2kΩ resistors. It is the time required for the error voltage (the voltage at the inverting input pin on the amplifier) to settle to within 0.01% of its final value from the time a 10V step input is applied to the inverter.

TYPICAL PERFORMANCE CHARACTERISTICS

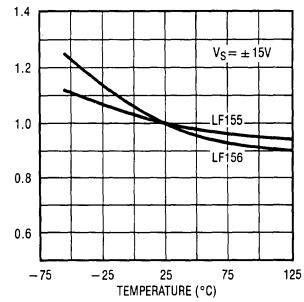
Gain, Phase vs Frequency



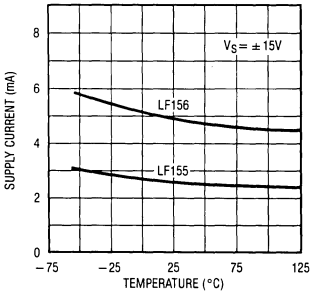
Inverter Settling Time



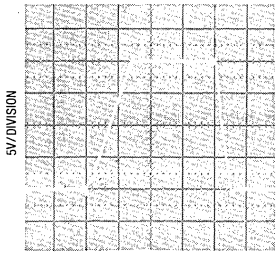
Normalized Slew Rate vs Temperature



Supply Current vs Temperature

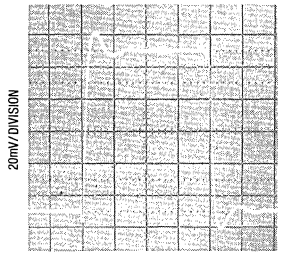


LF156 Large Signal Response



$A_V = +1$, $C_L = 100pF$, $1\mu S/DIV$

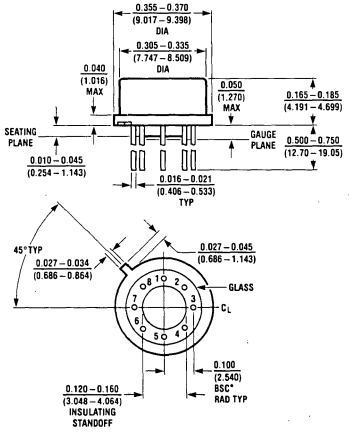
LF156 Small Signal Response



$A_V = +1$, $C_L = 100pF$, $0.2\mu SEC/DIV$

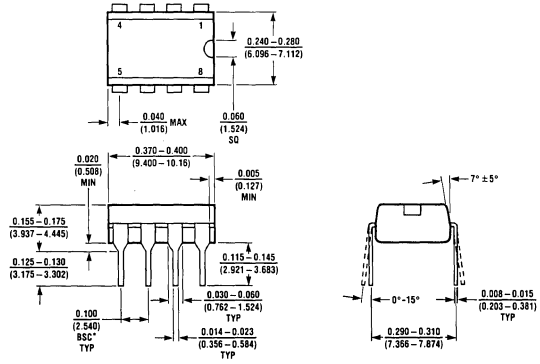
PACKAGE DESCRIPTION Dimensions in inches (millimeters) unless otherwise noted.

H Package Metal Can



$T_j$max	θ_{ja}	θ_{jc}
150°C	150°C/W	45°C/W

N8 Package 8 Lead Plastic



*LEADS WITHIN 0.007 OF TRUE POSITION (TP) AT GAUGE PLANE

$T_j$max	θ_{ja}
100°C	130°C/W

Low Power Op Amp and Reference

FEATURES

- *Guaranteed* Operation at +1.2V Op Amp and Reference on Single Chip
- Low Supply Current 400μA
- Capable of Floating Mode Operation
- Low Reference Drift 20ppm/°C
- Low Offset Voltage
- Output Swings to Within 15mV of Rails

APPLICATIONS

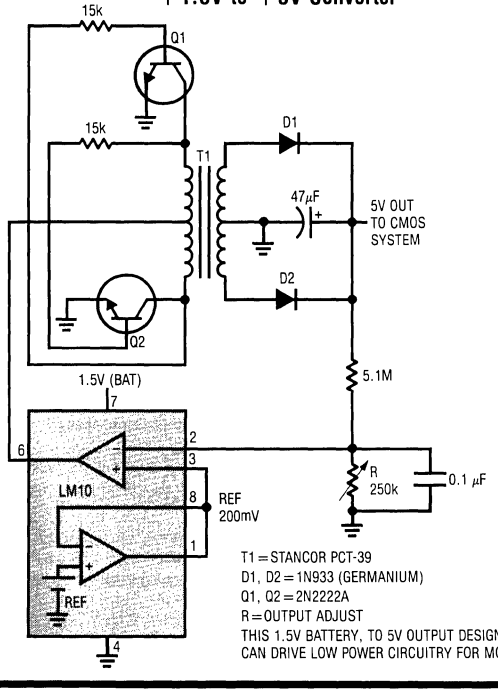
- Remote Signal Conditioner/Transmitter
- Battery Operated Instruments
- Precision Current Regulators
- Precision Voltage Regulators
- Thermocouple Transmitter

DESCRIPTION

The LM10 combines a precision reference, a reference buffer amplifier and an independent, high quality op amp on a single chip. The device is capable of operation from a single supply as low as 1.1V, from dual supplies up to ±20V and typically draws 270μA supply current. Input voltage range for the op amp includes ground, while the unloaded output can swing to within 15mV of each rail. Further, the LM10 will deliver 20mA output current and still swing within ±400mV of the supply rails.

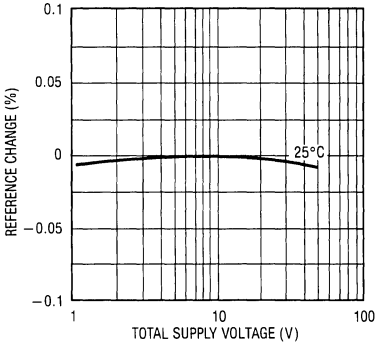
With its low operating current and floating operation capability, the LM10 is ideal for two wire analog transmitter circuits where the processed signal is carried on the same line used for power. The LM10 is suggested for portable battery powered equipment and is fully specified for operation from a single 1.2V battery. Other applications include precision current and voltage regulators, operating from very low voltages to several hundred volts.

+1.5V to +5V Converter



T1 = STANCOR PCT-39
D1, D2 = 1N933 (GERMANIUM)
Q1, Q2 = 2N2222A
R = OUTPUT ADJUST
THIS 1.5V BATTERY, TO 5V OUTPUT DESIGN CAN DRIVE LOW POWER CIRCUITRY FOR MONTHS.

Line Regulation



ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage
- LM10/LM10B/LM10C 45V
- LM10BL/LM10CL 7V

Differential Input Voltage (Note 1)
- LM10/LM10B/LM10C ..... ±40V
- LM10BL/LM10CL ..... ±7V

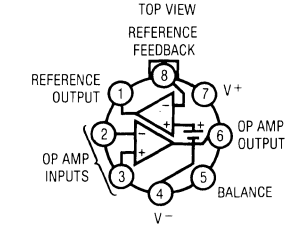
Output Short Circuit Duration ..... Indefinite

Operating Temperature Range (Note 2)
- LM10 ..... $-55°C \leq T_A \leq 125°C$
- LM10B/LM10BL ..... $-25°C \leq T_A \leq 85°C$
- LM10C/LM10CL ..... $0°C \leq T_A \leq 70°C$

Storage Temperature Range .... $-65°C \leq T_A \leq 150°C$

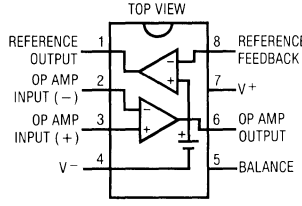
Lead Temperature (Soldering, 10 sec.) ..... 300°C

PACKAGE/ORDER INFORMATION



METAL CAN H PACKAGE

ORDER PART NUMBER: LM10H, LM10BH, LM10CH, LM10BLH, LM10CLH



J8 HERMETIC PACKAGE
N8 PLASTIC DIP PACKAGE

ORDER PART NUMBER: LM10CN8, LM10CLN8, LM10CJ8, LM10CLJ8, LM10J8, LM10BJ8, LM10BLJ8

OP AMP ELECTRICAL CHARACTERISTICS (Note 3)

SYMBOL	PARAMETER	CONDITIONS		LM10/LM10B MIN	LM10/LM10B TYP	LM10/LM10B MAX	LM10C MIN	LM10C TYP	LM10C MAX	UNITS
V_{OS}	Input Offset Voltage				0.3	2.0		0.5	4.0	mV
			●			3.0			5.0	mV
$\frac{\Delta V_{OS}}{\Delta Temp}$	Average Offset Voltage Drift		●		2.0			5.0		µV/°C
I_{OS}	Input Offset Current	(Note 4)			0.25	0.7		0.4	2.0	nA
			●			1.5			3.0	nA
$\frac{\Delta I_{OS}}{\Delta Temp}$	Offset Current Drift		●		2.0			5.0		pA/°C
I_B	Input Bias Current				10	20		12	30	nA
			●			30			40	nA
$\frac{\Delta I_B}{\Delta Temp}$	Bias Current Drift		●		60			90		pA/°C
A_{VOL}	Large Signal Voltage Gain	$V_S = \pm 20V$, $I_{OUT} = 0$, $V_{OUT} = \pm 19.95V$		120	400		80	400		V/mV
			●	80			50			V/mV
		$V_S = \pm 20V$, $V_{OUT} = \pm 19.4V$								
		$I_{OUT} = \pm 20mA$		50	130		25	130		V/mV
		$I_{OUT} = \pm 15mA$	●	20			15			V/mV
		$V_S = \pm 0.6V$, $I_{OUT} = \pm 2mA$								
		$V_{OUT} = \pm 0.4V$, $V_{CM} = -0.4V$			1.5	3.0		1.0	3.0	V/mV
		$V_S = \pm 0.65V$, $I_{OUT} = \pm 2mA$								
		$V_{OUT} = \pm 0.3V$, $V_{CM} = -0.4V$	●		0.5			0.75		V/mV
	Shunt Gain (Note 5)	$0.1mA \leq I_{OUT} \leq 5mA$, $R_L = 1.1k\Omega$								
		$1.2V \leq V_{OUT} \leq 40V$		14	33		10	33		V/mV
		$1.3V \leq V_{OUT} \leq 40V$	●	6			6			V/mV
		$0.1mA \leq I_{OUT} \leq 20mA$, $R_L = 250\Omega$								
		$1.5V \leq V^+ \leq 40V$		8	25		6	25		V/mV
			●	4			4			V/mV

OP AMP ELECTRICAL CHARACTERISTICS (Note 3)

SYMBOL	PARAMETER	CONDITIONS		LM10/LM10B MIN	LM10/LM10B TYP	LM10/LM10B MAX	LM10C MIN	LM10C TYP	LM10C MAX	UNITS
CMRR	Common-Mode Rejection Ratio	$V_S = \pm 20V$								
		$-20V \le V_{CM} \le 19.15V$		93	102		90	102		dB
		$-20V \le V_{CM} \le 19V$	●	87			87			dB
PSRR	Power Supply Rejection Ratio	$-0.2V \ge V^- \ge -39V$								
		$V^+ = 1.0V$		90	96		87	96		dB
		$V^+ = 1.1V$	●	84			84			dB
		$V^- = -0.2V$								
		$1.0V \le V^+ \le 39.8V$		96	106		93	106		dB
		$1.1V \le V^+ \le 39.8V$	●	90			90			dB
R_{IN}	Input Resistance	(Note 6)		250	500		150	400		kΩ
			●	150			115			kΩ
I_S	Supply Current				270	400		300	500	μA
			●			500			570	μA
ΔI_S	Supply Current Change	$1.2V \le V_S \le 40V$			15	75		15	75	μA
		$1.3V \le V_S \le 40V$	●			75			75	μA

REFERENCE AMPLIFIER ELECTRICAL CHARACTERISTICS (Note 3)

SYMBOL	PARAMETER	CONDITIONS		LM10/LM10B MIN	LM10/LM10B TYP	LM10/LM10B MAX	LM10C MIN	LM10C TYP	LM10C MAX	UNITS
V_{REF}	Feedback Sense Voltage	Voltage at Pin 1 with Pin 1		195	200	205	190	200	210	mV
		Connected to Pin 8	●	194	200	206	189	200	211	mV
$\frac{\Delta V_{REF}}{\Delta Temp}$	Reference Drift		●		0.002			0.003		%/°C
	Feedback Current	Current into Pin 8			20	50		22	75	nA
			●			65			90	nA
	Line Regulation	$0 \le I_{REF} \le 1mA$, $V_{REF} = 200mV$								
		$1.2V \le V_S \le 40V$			0.001	0.003		0.001	0.008	%/V
		$1.3V \le V_S \le 40V$	●		0.001	0.006		0.001	0.01	%/V
	Load Regulation	$0 \le I_{REF} \le 1mA$								
		$V^+ - V_{REF} \ge 1.0V$			0.01	0.1		0.01	0.15	%
		$V^+ - V_{REF} \ge 1.1V$	●		0.01	0.15		0.01	0.20	%
	Reference Amplifier Gain	$0.2V \le V_{REF} \le 35V$		50	75		25	70		V/mV
			●	23			15			V/mV

OP AMP ELECTRICAL CHARACTERISTICS (Note 3)

SYMBOL	PARAMETER	CONDITIONS		LM10BL MIN	LM10BL TYP	LM10BL MAX	LM10CL MIN	LM10CL TYP	LM10CL MAX	UNITS
V_{OS}	Input Offset Voltage				0.3	2.0		0.5	4.0	mV
			●			3.0			5.0	mV
$\frac{\Delta V_{OS}}{\Delta Temp}$	Average Offset Voltage Drift		●		2.0			5.0		μV/°C
I_{OS}	Input Offset Current	(Note 4)			0.1	0.7		0.2	2.0	nA
			●			1.5			3.0	nA
$\frac{\Delta I_{OS}}{\Delta Temp}$	Offset Current Drift		●		2.0			5.0		pA/°C
I_B	Input Bias Current				10	20		12	30	nA
			●			30			40	nA
$\frac{\Delta I_B}{\Delta Temp}$	Bias Current Drift		●		60			90		pA/°C
A_{VOL}	Large Signal Voltage Gain	$V_S = \pm 3.25V$, $I_{OUT} = 0$, $V_{OUT} = \pm 3.2V$		60	300		40	300		V/mV
			●	40			25			V/mV
		$V_S = \pm 3.25V$, $V_{OUT} = \pm 2.75V$ $I_{OUT} = \pm 10mA$		10	25		5	25		V/mV
			●	4			3			V/mV
		$I_{OUT} = \pm 2mA$, $V_{CM} = -0.4V$								
		$V_S = \pm 0.6V$, $V_{OUT} = \pm 0.4V$		1.5	3.0		1.0	3.0		V/mV
		$V_S = \pm 0.65V$, $V_{OUT} = \pm 0.3V$	●	0.5			0.75			V/mV
	Shunt Gain (Note 5)	$0.1mA \le I_{OUT} \le 10mA$, $R_L = 500\Omega$ $1.5V \le V^+ \le 6.5V$		8	30		6	30		V/mV
			●	4			4			V/mV
CMRR	Common-Mode Rejection Ratio	$V_S = \pm 3.25V$ $-3.25V \le V_{CM} \le 2.4V$		89	102		80	102		dB
		$-3.25V \le V_{CM} \le 2.25V$	●	83			74			dB
PSRR	Power Supply Rejection Ratio	$-0.2V \ge V^- \ge -5.4V$ $V^+ = 1.0V$		86	96		80	96		dB
		$V^+ = 1.2V$	●	80			74			dB
PSRR		$V^- = -0.2V$ $1.0V \le V^+ \le 6.3V$		94	106		80	106		dB
		$1.1V \le V^+ \le 6.3V$	●	88			74			dB
R_{IN}	Input Resistance	(Note 6)		250	500		150	400		kΩ
			●	150			115			kΩ
I_S	Supply Current				260	400		280	500	μA
			●			500			570	μA

REFERENCE AMPLIFIER ELECTRICAL CHARACTERISTICS (Note 3)

SYMBOL	PARAMETER	CONDITIONS		LM10BL MIN	LM10BL TYP	LM10BL MAX	LM10CL MIN	LM10CL TYP	LM10CL MAX	UNITS
V_{REF}	Feedback Sense Voltage	Voltage at Pin 1 with Pin 1 Connected to Pin 8		195	200	205	190	200	210	mV
			●	194	200	206	189	200	211	mV
$\frac{\Delta V_{REF}}{\Delta Temp}$	Reference Drift		●		0.002			0.003		%/°C
	Feedback Current	Current into Pin 8			20	50		22	75	nA
			●			65			90	nA
	Line Regulation	$0 \le I_{REF} \le 0.5mA$, $V_{REF} = 200mV$								
		$1.2V \le V_S \le 6.5V$			0.001	0.01		0.001	0.02	%/V
		$1.3V \le V_S \le 6.5V$	●		0.001	0.02		0.001	0.03	%/V
	Load Regulation	$0 \le I_{REF} \le 0.5mA$								
		$V^+ - V_{REF} \ge 1.0V$			0.01	0.1		0.01	0.15	%
		$V^+ - V_{REF} \ge 1.1V$	●		0.01	0.15		0.01	0.20	%
	Reference Amplifier Gain	$0.2V \le V_{REF} \le 5.5V$		30	70		20	70		V/mV
			●	20			15			V/mV

The ● denotes the specifications which apply over full operating temperature range.

Note 1: The input voltage can exceed the supply voltages as long as the voltage from the input to any other terminal does not exceed the maximum differential voltage, and the maximum junction temperature is not exceeded due to the excess power dissipation that occurs when the input voltage is less than the negative supply voltage.

Note 2: The maximum operating junction temperatures are: 150°C for the LM10; 100°C for the LM10B and LM10BL; and 85°C for the LM10C and LM10CL. Package derating factors will be found on the back page of this data sheet.

Note 3: These specifications apply for the following conditions unless otherwise noted:

	at 25°C	over temperature
(a)	$V^- \le V_{CM} \le V^+ - 0.85V$	$V^- \le V_{CM} \le V^+ - 1.0V$
(b)	$1.2V \le V_S \le V_{MAX}$	$1.3V \le V_S \le V_{MAX}$

$V_{REF} = 0.2V$ and $0 \le I_{REF} \le 1.0mA$ where $V_{MAX} = 40V$ for the LM10, LM10B and LM10C and $V_{MAX} = 6.5V$ for the LM10BL and LM10CL. The specifications do not include errors due to thermal gradients ($\tau_1 \approx 20ms$), die heating ($\tau_2 \approx 0.2$ sec) or package heating.

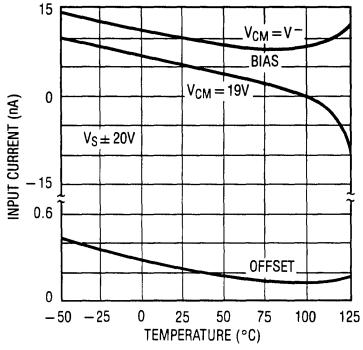
Note 4: For $T_J > 90°C$, I_{OS} may exceed 1.5nA when $V_{CM} = V^-$. When the common-mode input voltage is within 100mV of the negative supply and $T_J = 125°C$, the offset current will be less than 5nA.

Note 5: Shunt gain defines the operation in floating applications when the output is connected to the V^+ terminal and input common-mode is referred to V^- (see typical applications). The effects of larger output voltage swing with higher load resistance can be accounted for by adding the positive supply rejection error.

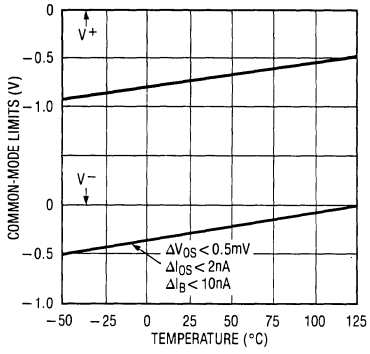
Note 6: Guaranteed by design.

TYPICAL PERFORMANCE CHARACTERISTICS (Op Amp)

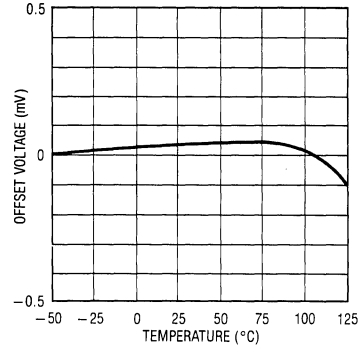
Input Current



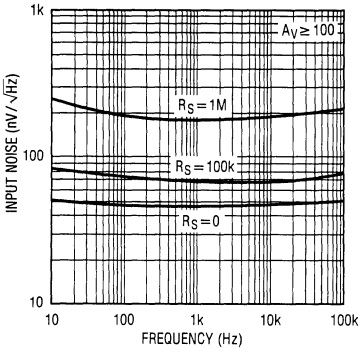
Common-Mode Limits



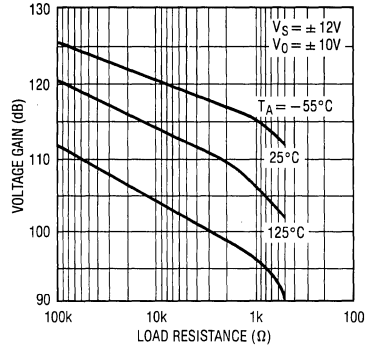
Offset Voltage Drift



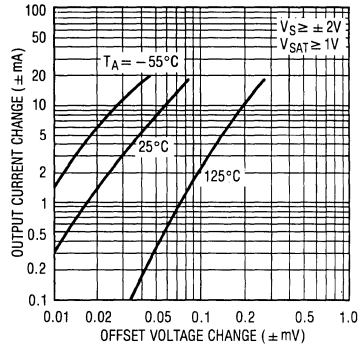
Input Noise Voltage



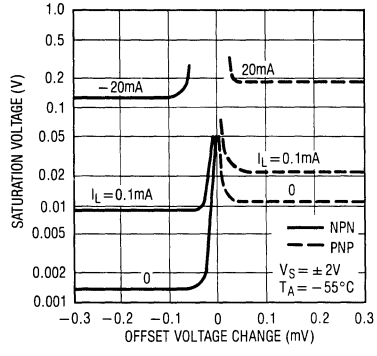
DC Voltage Gain



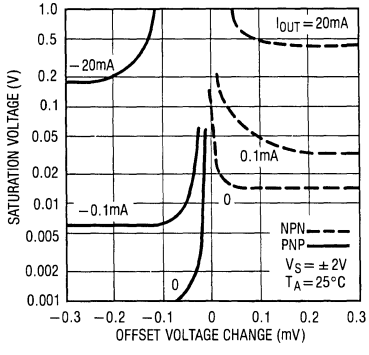
Transconductance



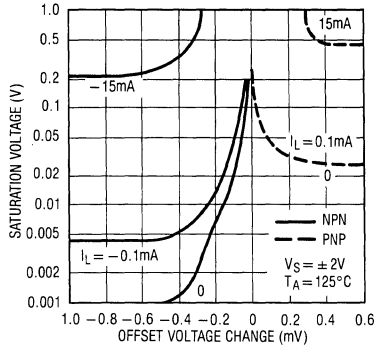
Output Saturation Characteristics



Output Saturation Characteristics

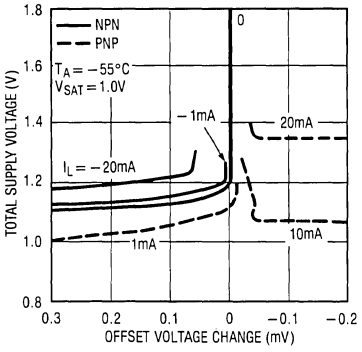


Output Saturation Characteristics

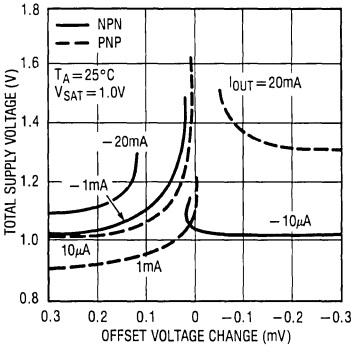


TYPICAL PERFORMANCE CHARACTERISTICS (Op Amp)

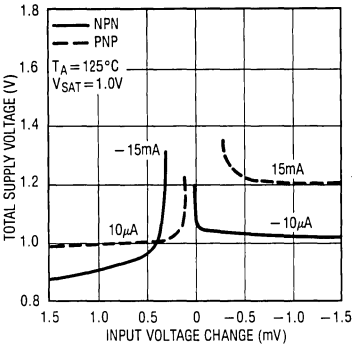
Minimum Supply Voltage



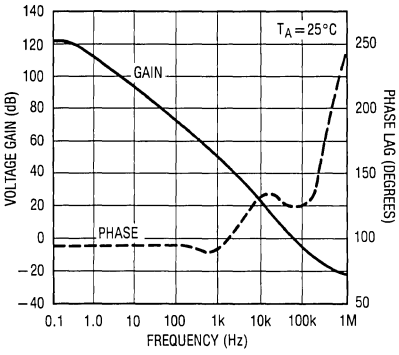
Minimum Supply Voltage



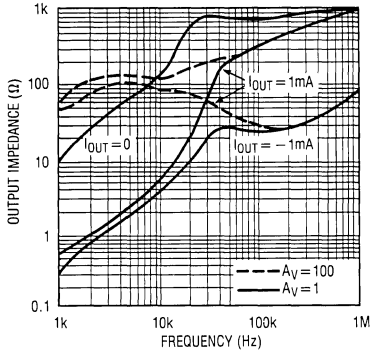
Minimum Supply Voltage



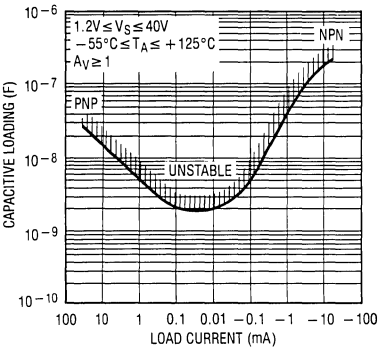
Frequency Response



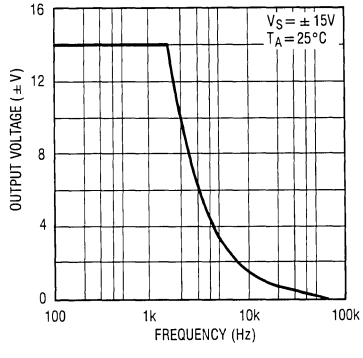
Output Impedance



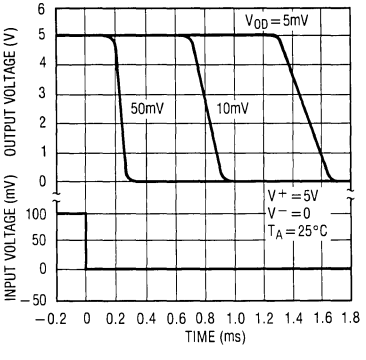
Typical Stability Range



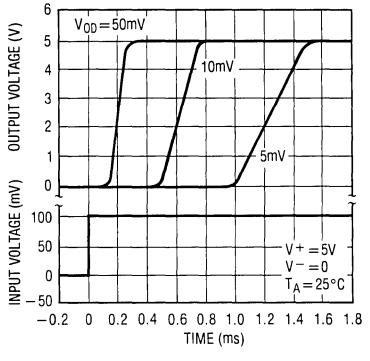
Large Signal Response



Comparator Response Time for Various Input Overdrives

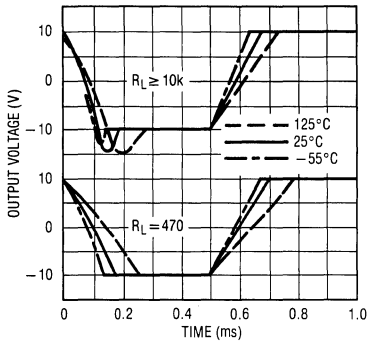


Comparator Response Time for Various Input Overdrives

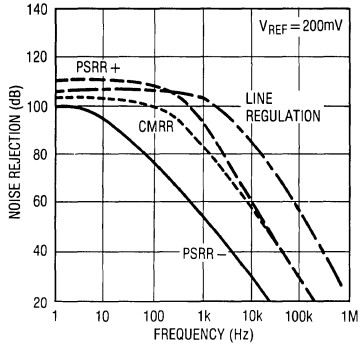


TYPICAL PERFORMANCE CHARACTERISTICS

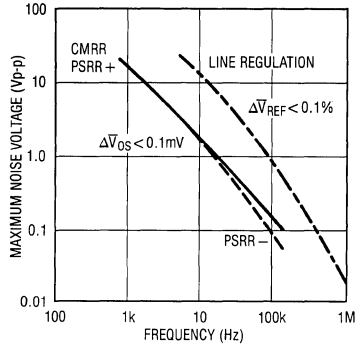
Follower Pulse Response



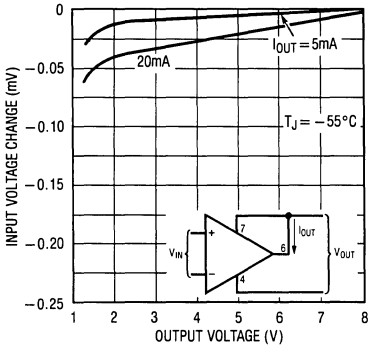
Noise Rejection



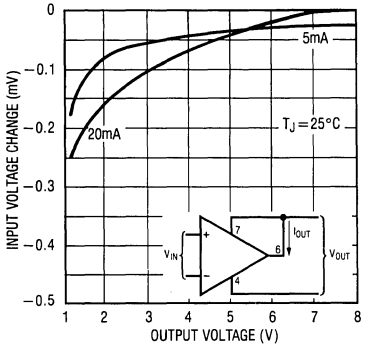
Rejection Slew Limiting



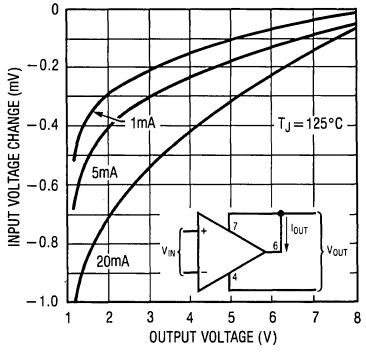
Shunt Gain



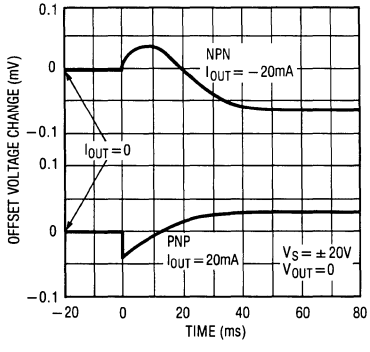
Shunt Gain



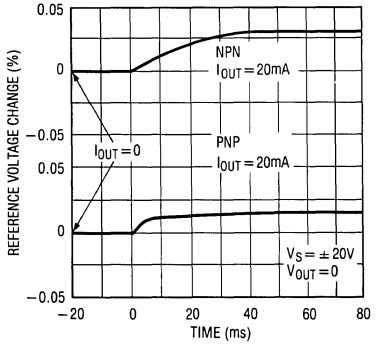
Shunt Gain



Thermal Gradient Feedback

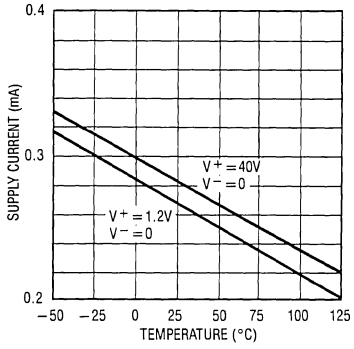


Change in Reference Op Amp Loading

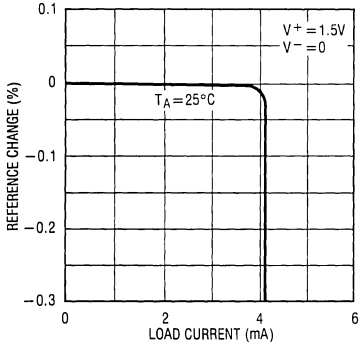


TYPICAL PERFORMANCE CHARACTERISTICS (Reference)

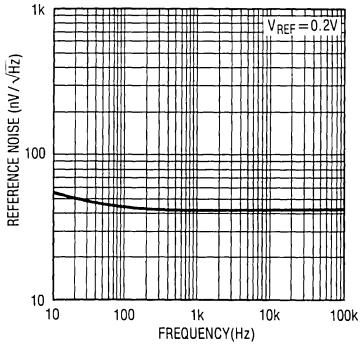
Supply Current



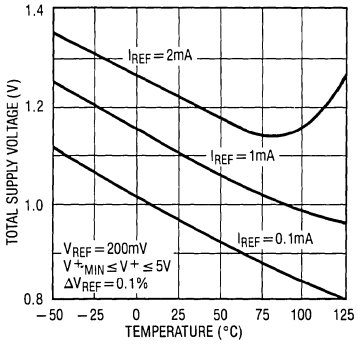
Load Regulation



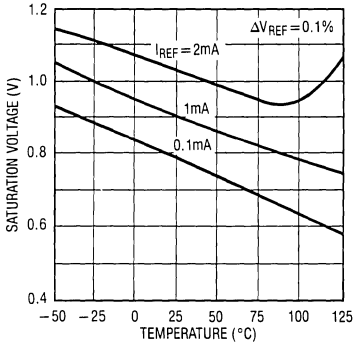
Reference Noise Voltage



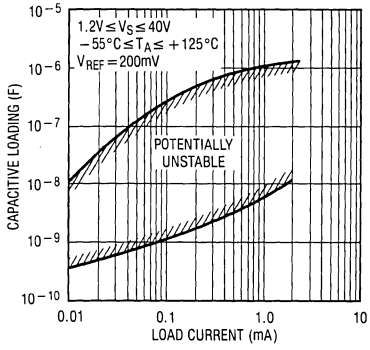
Minimum Supply Voltage



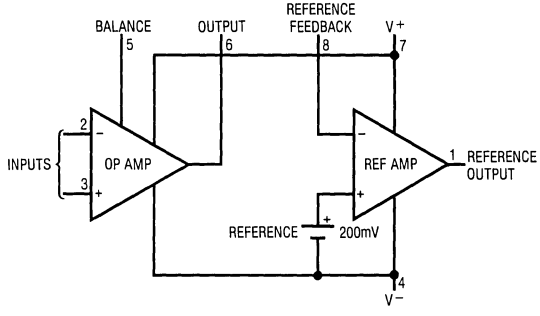
Output Saturation



Typical Stability Range



BLOCK DIAGRAM

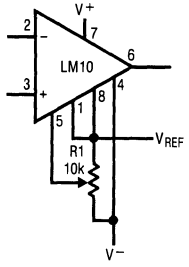


APPLICATION HINTS

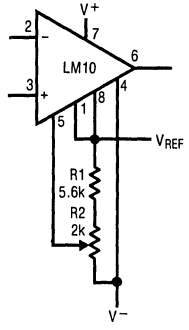
With heavy amplifier loading to V^-, resistance drops in the V^- lead can adversely affect reference regulation. Lead resistance can approach 1Ω. Therefore, the common to the reference circuitry should be connected as close as possible to the package.

TYPICAL APPLICATIONS

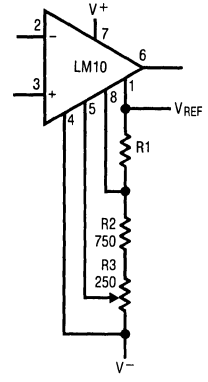
Standard Offset Adjustment



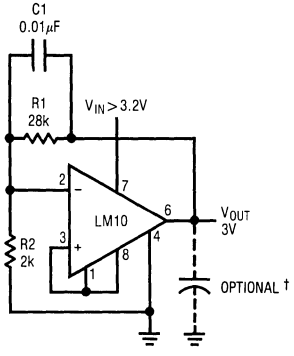
Limited Range Offset Adjustment



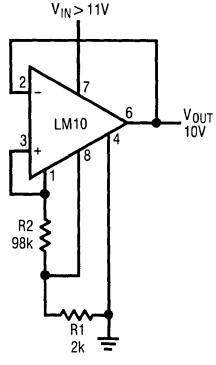
Limited Range Offset Adjustment with Boosted Reference



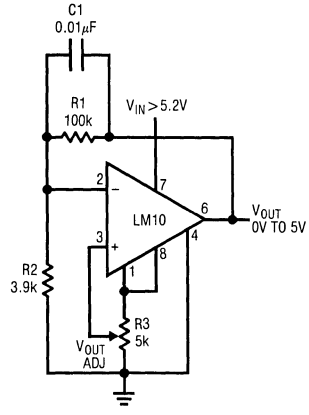
Low Voltage Regulator



Best Regulation



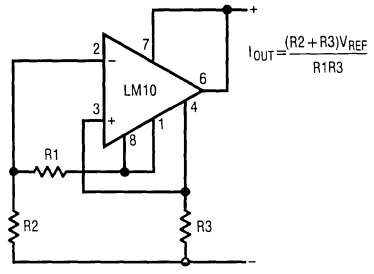
0V to 5V Regulator



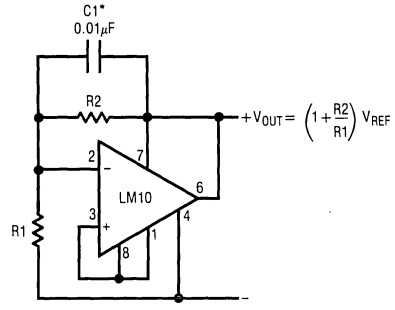
† USE ELECTROLYTIC OUTPUT CAPACITORS

TYPICAL APPLICATIONS

Two-Terminal Current Regulator

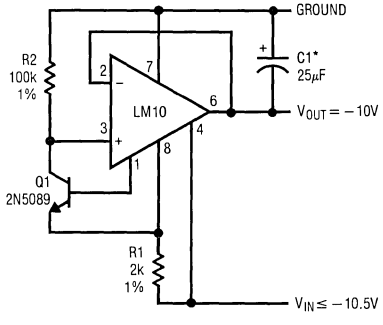


Shunt Regulator



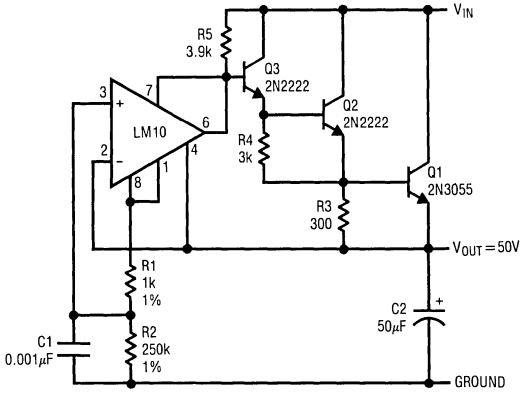
*REQUIRED FOR CAPACITIVE LOADING

Negative Regulator



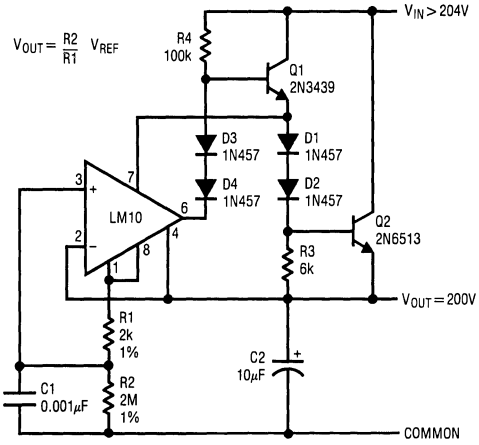
*ELECTROLYTIC

Floating Regulator

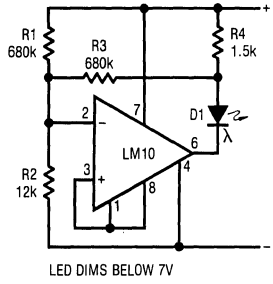


TYPICAL APPLICATIONS

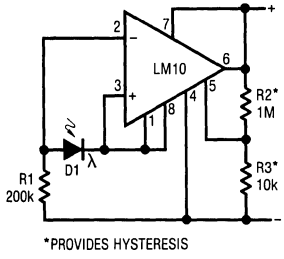
High Voltage Regulator



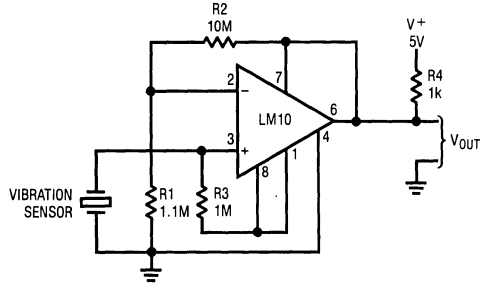
6V Battery-Level Indicator



Light Level Sensor

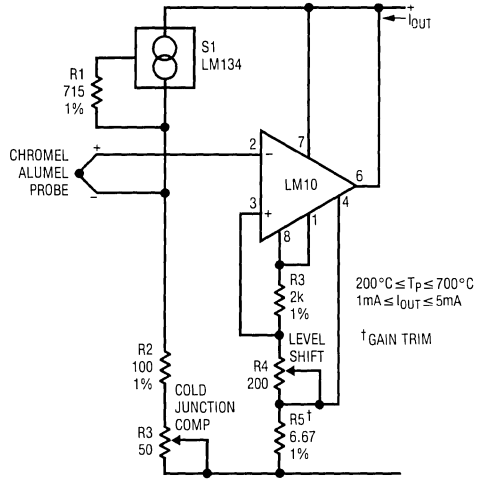


Transducer Amplifier

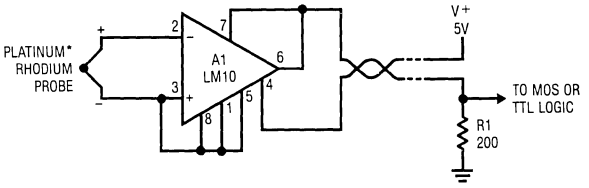


TYPICAL APPLICATIONS

Thermocouple Transmitter

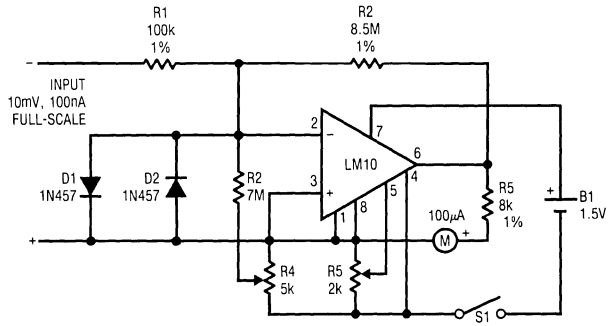


Flame Detector

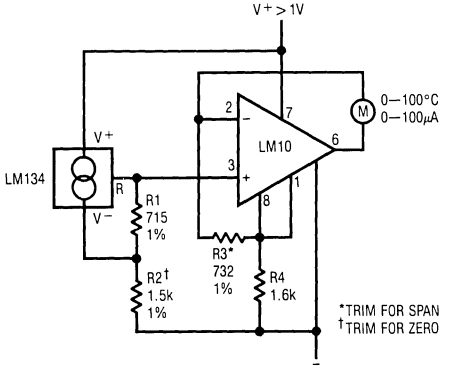


*800°C THRESHOLD IS ESTABLISHED BY CONNECTING BALANCE TO V_{REF}.

Meter Amplifier

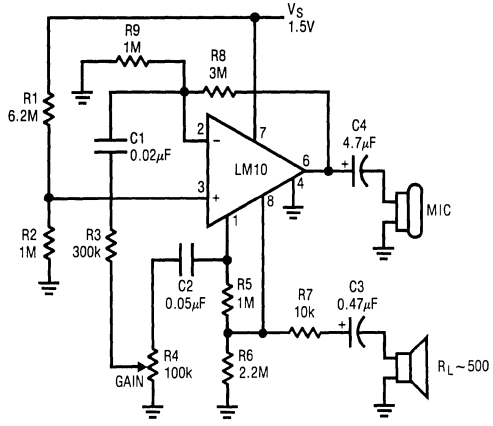


Thermometer

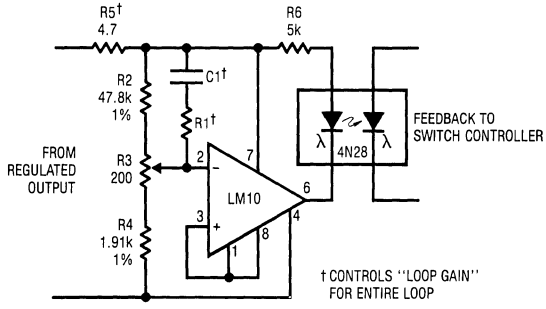


TYPICAL APPLICATIONS

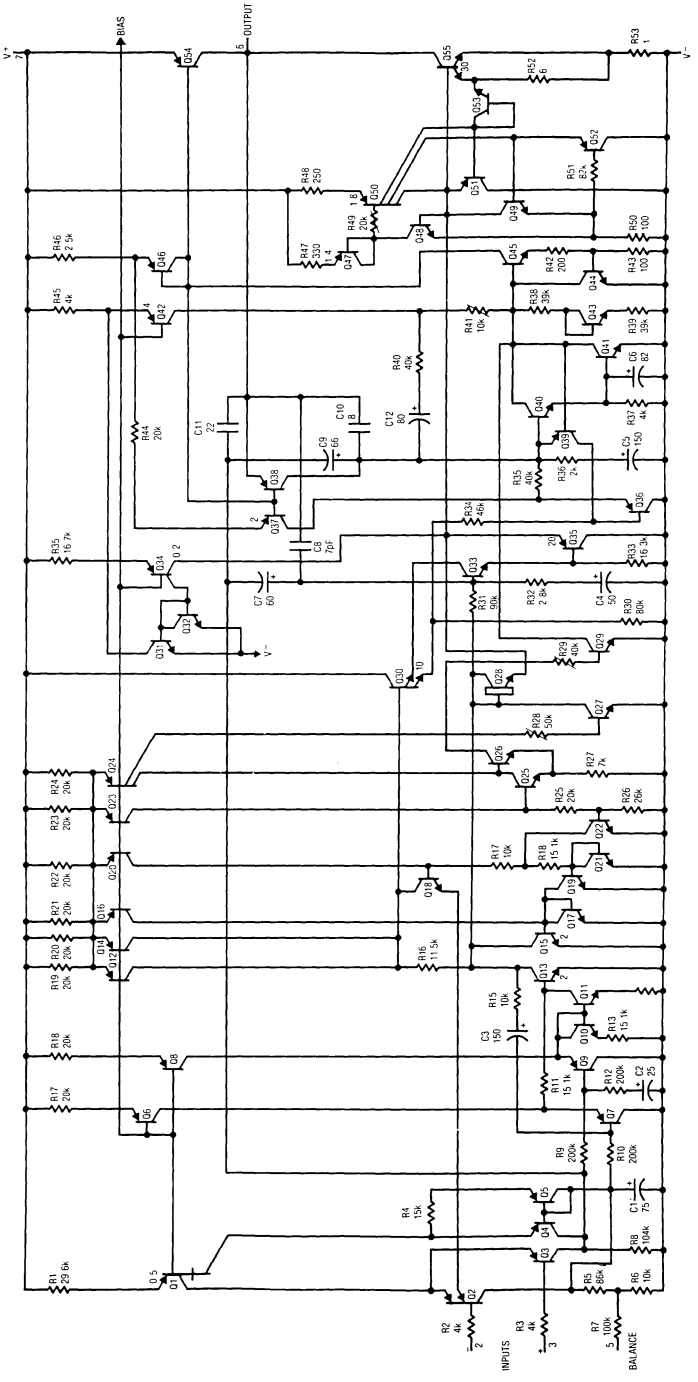
Microphone Amplifier
$A_V \approx 1k$



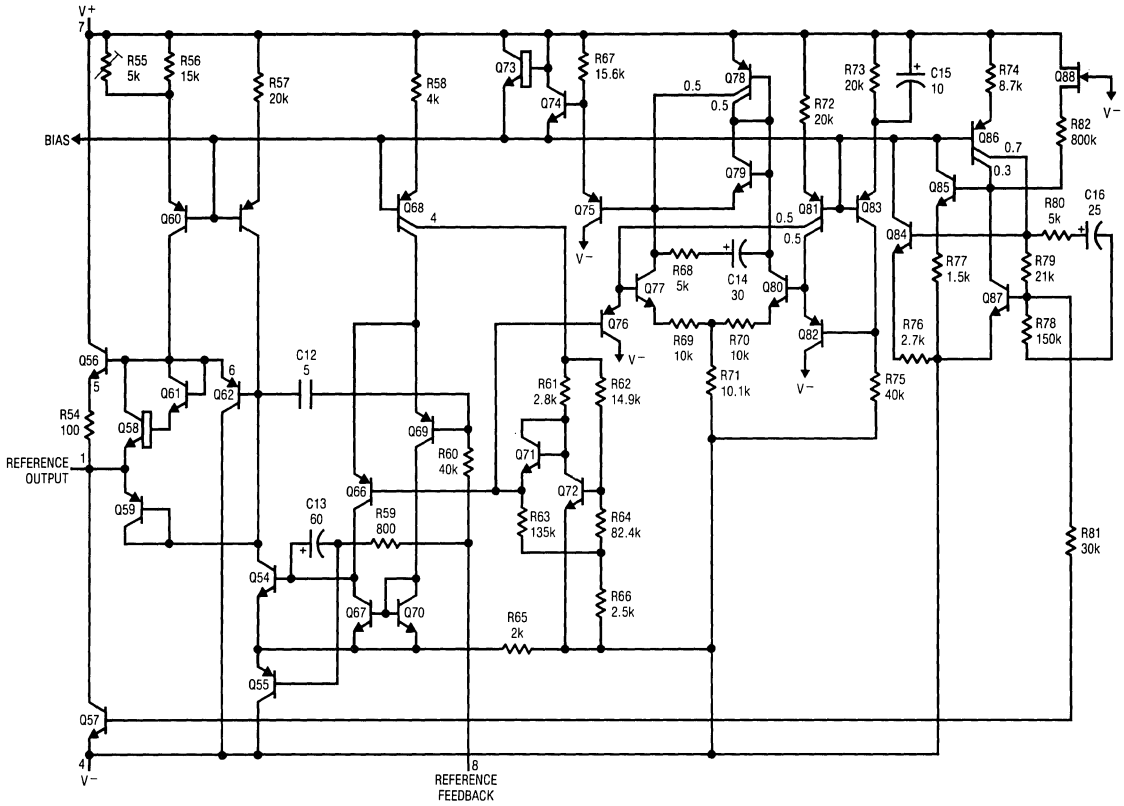
Isolated Voltage Sensor
for Switching Regulators



OP AMP SCHEMATIC DIAGRAM

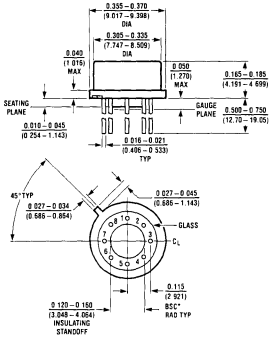


REFERENCE AND INTERNAL REGULATOR SCHEMATIC DIAGRAM



PACKAGE DESCRIPTION

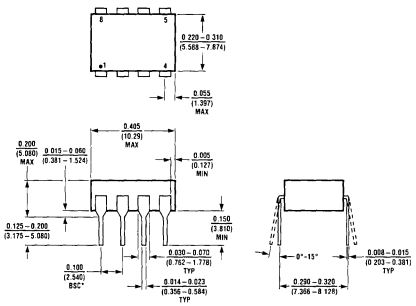
H Package
Metal Can



NOTE: DIMENSIONS IN INCHES

$T_j$max	θ_{ja}	θ_{jc}
150°C	150°C/W	45°C/W

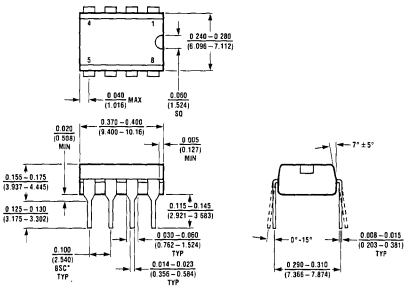
J8 Package
8 Lead Hermetic Dip



NOTE: DIMENSIONS IN INCHES UNLESS OTHERWISE NOTED
*LEADS WITHIN 0.007 OF TRUE POSITION (TP) AT GAUGE PLANE

$T_j$max	θ_{ja}
150°C	100°C/W

N8 Package
8 Lead Plastic



NOTE: DIMENSIONS IN INCHES UNLESS OTHERWISE NOTED
*LEADS WITHIN 0.007 OF TRUE POSITION (TP) AT GAUGE PLANE

$T_j$max	θ_{ja}
100°C	130°C/W

FEATURES

- *Guaranteed* 2nA Max. Input Bias Current
- *Guaranteed* 600μA Max. Supply Current
- *Guaranteed* 0.5mV Max. Offset Voltage
- *Guaranteed* 5μV/°C Max. Drift
- Wide Supply Voltage Range: ±2V to ±20V
- Interchangeable with Other Manufacturers' LH2108

APPLICATIONS

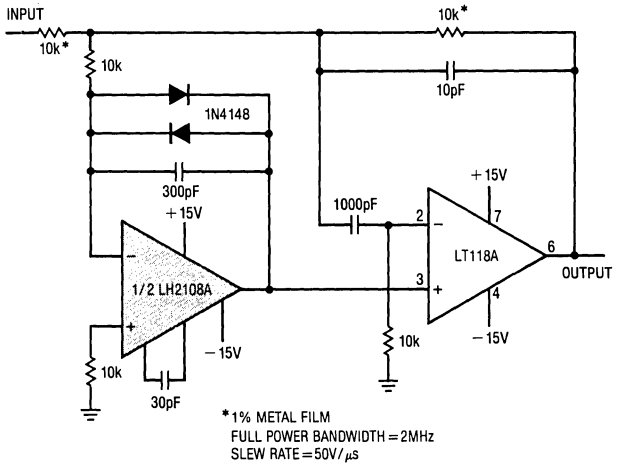
- Integrators
- Transducer Amplifiers
- Analog Memories
- Light Meters

DESCRIPTION

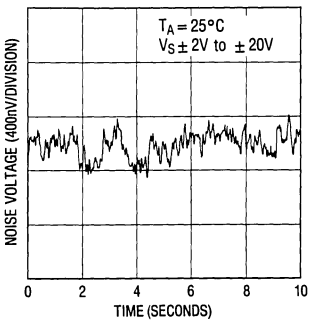
The LH2108A series of precision operational amplifiers is particularly well suited for high source impedance applications requiring low offset and bias currents, as well as low power dissipation. Unlike FET input amplifiers, the offset and bias currents of the LH2108A do not change significantly with temperature variations. Advanced design, processing and testing techniques make Linear's LH2108A a superior choice over previous devices.

For higher performance dual amplifiers, see the LT1024, LT1002, and LT1013 data sheets.

Fast Precision Inverter



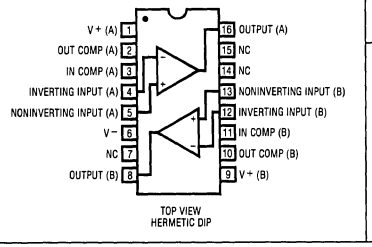
0.1Hz to 10Hz Noise



ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... ±20V
Differential Input Current (Note 1) ..... ±10mA
Input Voltage (Note 2) ..... ±15V
Output Short Circuit Duration ..... Indefinite
Operating Temperature Range ..... −55°C to 125°C
Storage Temperature Range ..... −65°C to 150°C
Lead Temperature (Soldering, 10 sec.)..... 300°C

PACKAGE/ORDER INFORMATION



TOP VIEW
HERMETIC DIP

ORDER PART NUMBER
LH2108AD/883B
LH2108D/883B
LH2108AD
LH2108D

ELECTRICAL CHARACTERISTICS

±5V ≤ V_S ≤ ±20V and −55°C ≤ T_A ≤ 125°C unless otherwise noted.

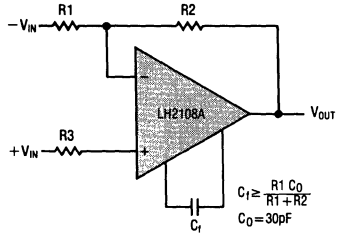
SYMBOL	PARAMETER	CONDITIONS	LH2108A MIN	LH2108A TYP	LH2108A MAX	LH2108 MIN	LH2108 TYP	LH2108 MAX	UNITS
V_{OS}	Input Offset Voltage	T_A = 25°C		0.3	0.5 1.0		0.7	2.0 3.0	mV mV
$\frac{\Delta V_{OS}}{\Delta Temp}$	Average Temperature Coefficient of Input Offset Voltage			1.0	5.0		3.0	15	µV/°C
I_{OS}	Input Offset Current	T_A = 25°C		0.05	0.2 0.4		0.05	0.2 0.4	nA nA
$\frac{\Delta I_{OS}}{\Delta Temp}$	Average Temperature Coeffcient of Input Offset Current			0.5	2.5		0.5	2.5	pA/°C
I_B	Input Bias Current	T_A = 25°C		0.5	2.0 3.0		0.5	2.0 3.0	nA nA
A_{VOL}	Large Signal Voltage Gain	T_A = 25°C, V_S = ±15V, V_{OUT} = ±10V, R_L ≥ 10kΩ	80 40	300		50 25	300		V/mV V/mV
CMRR	Common Mode Rejection Ratio		96	110		85	100		dB
PSRR	Power Supply Rejection Ratio		96	110		80	96		dB
	Input Voltage Range	V_S = ±15V	±13.5			±13.5			V
V_{OUT}	Output Voltage Swing	V_S = ±15V, R_L = 10kΩ	±13	±14		±13	±14		V
R_{IN}	Input Resistance	T_A = 25°C	30	70		30	70		MΩ
I_S	Supply Current	T_A = 25°C T_A = 125°C		0.3 0.15	0.6 0.4		0.3 0.15	0.6 0.4	mA mA

Note 1: Differential input voltages greater than 1V will cause excessive current to flow through the input protection diodes unless current limiting resistance is used.

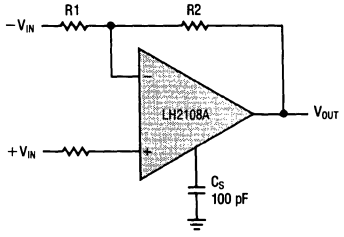
Note 2: For supply voltages less than ±15V, the maximum input voltage is equal to the supply voltage. For typical performance, see LM108A data sheet.

COMPENSATION CIRCUITS

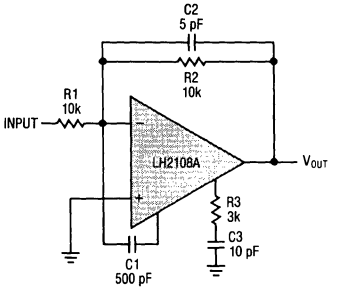
Standard Compensation Circuit



Alternate Frequency Compensation



Feedforward Compensation



FEATURES

- 30 Volt Differential Input Range
- 75 nA Input Bias Current
- Wide Common Mode Voltage Range

APPLICATIONS

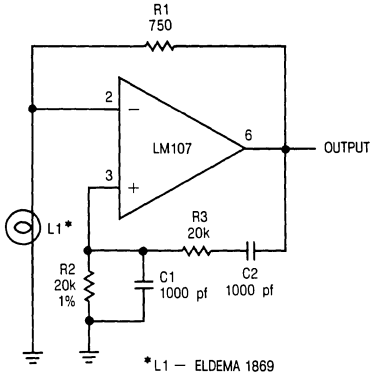
- Signal Conditioning Amplifiers
- Voltage Followers
- Comparators

DESCRIPTION

The LM101A and LM107 are general purpose operational amplifiers, featuring low bias current and the ability to operate with high input differential voltages up to 30 Volts. Unlike many FET input amplifiers, the output of the LM101A/107 does not reverse if the common mode range is exceeded, making them particularly useful in comparator and oscillator circuits.

The LM101A uses external compensation, allowing the frequency response and slew rate to be optimized for the application. The LM107 is identical to the LM101A with the exception that the compensation capacitor is internal. Linear's LM101A and LM107 include improved design and processing techniques resulting in superior long term stability and reliability over previous devices. The curve of bias current versus differential input voltage indicates that a minimal change in input current occurs over a wide range of input signal, which is important in many applications.

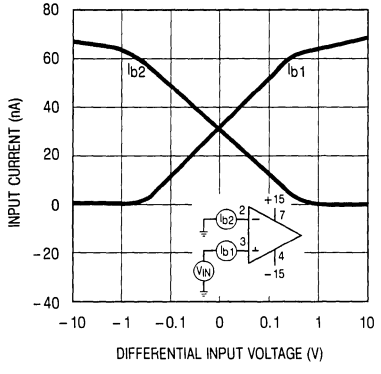
Wein Bridge Sine Wave Oscillator



*L1 — ELDEMA 1869
R1 = R2
C1 = C2

$$f = \frac{1}{2\pi R2\,C1}$$

Bias Current vs Differential Input Voltage



ABSOLUTE MAXIMUM RATINGS

Supply Voltage
- LM101A/LM107 ..... ±22 Volts
- LM301A/LM307 ..... ±18 Volts

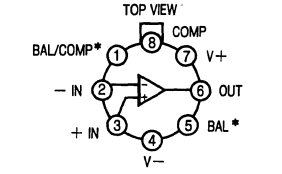
Differential Input Voltage ..... ±30 Volts
Input Voltage, Note 2 ..... ±15 Volts
Output Short Circuit Duration, Note 3..... Indefinite
Operating Temperature Range
- LM101A/LM107 ..... −55°C to 125°C
- LM301A/LM307 ..... 0°C to 70°C

Maximum Junction Temperature
- LM101A/LM107 ..... 150°C
- LM301A/LM307 ..... 100°C

Storage Temperature Range
- All Devices..... −65°C to 150°C

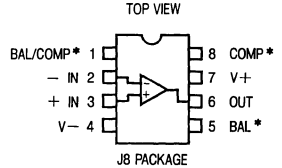
Lead Temperature (Soldering, 10 sec.)..... 300°C

PACKAGE/ORDER INFORMATION



METAL CAN H PACKAGE
*PINS 1, 5, 8 NO CONNECTION ON LM107/307

ORDER PART NUMBER: LM101AH, LM301AH, LM107H, LM307H



J8 PACKAGE
HERMETIC DIP
*PINS 1, 5, 8 NO CONNECTION ON LM107/307

ORDER PART NUMBER: LM101AJ8, LM301AJ8, LM107J8, LM307J8

ELECTRICAL CHARACTERISTICS (Note 1)

SYMBOL	PARAMETER	CONDITIONS		LM101A/LM107 MIN	LM101A/LM107 TYP	LM101A/LM107 MAX	LM301A/LM307 MIN	LM301A/LM307 TYP	LM301A/LM307 MAX	UNITS
V_{OS}	Input Offset Voltage	$R_S \leq 50K\Omega$, $T_A = 25°C$			0.7	2.0		2.0	7.5	mV
		$R_S \leq 50K\Omega$	●			3.0			10	mV
$\frac{\Delta V_{OS}}{\Delta \text{Temp}}$	Average Temperature Coefficient of Input Offset Voltage	$R_S \leq 50K\Omega$	●		3.0	15		6.0	30	μV/°C
I_{OS}	Input Offset Current	$T_A = 25°C$			1.5	10		3.0	50	nA
			●			20			70	nA
$\frac{\Delta I_{OS}}{\Delta \text{Temp}}$	Average Temperature Coefficient of Input Offset Current	$25°C \leq T_A \leq T_{MAX}$			0.01	0.1		0.01	0.3	nA/°C
		$T_{MIN} \leq T_A \leq 25°C$			0.02	0.2		0.02	0.6	nA/°C
I_B	Input Bias Current	$T_A = 25°C$			30	75		70	250	nA
			●			100			300	nA
A_{VOL}	Large Signal Voltage Gain	$T_A = 25°C$, $V_S \pm 15V$, $V_{OUT} = \pm 10V$, $R_L \geq 2K\Omega$		50	160		25	160		V/mV
		$V_S = \pm 15V$, $V_{OUT} = \pm 10V$, $R_L \geq 2K\Omega$	●	25			15			V/mV
CMRR	Common Mode Rejection Ratio	$R_S \leq 50K\Omega$	●	80	96		70	90		dB
PSRR	Power Supply Rejection Ratio	$R_S \leq 50K\Omega$	●	80	96		70	96		dB
	Input Voltage Range	$V_S = \pm 20V$	●	±15						V
		$V_S = \pm 15V$	●		+15 −13		±12	+15 −13		V V
V_{OUT}	Output Voltage Swing	$V_S = \pm 15V$ $R_L = 10K\Omega$	●	±12	±14		±12	±14		V
		$R_L = 2K\Omega$	●	±10	±13		±10	±13		V
R_{IN}	Input Resistance	$T_A = 25°C$		1.5	4.0		0.5	2.0		MΩ
I_S	Supply Current	$T_A = 25°C$, $V_S = \pm 20V$			1.8	3.0		1.8	3.0	mA
		$T_A = 125°C$, $V_S = \pm 20V$	●		1.2	2.5				mA

The ● denotes the specifications which apply over the full operating temperature range.

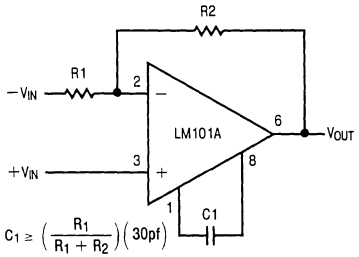
Note 1: Unless otherwise noted; all measurements are made with unity gain compensation (C_1 = 30pf for the LM101A/301A); these specifications apply for $\pm 5V \leq V_S \leq \pm 20V$ for the LM101A/LM107; and $\pm 5V \leq V_S \leq \pm 15V$ for the LM301A/LM307.

Note 2: For supply voltages less than ± 15 Volts, the maximum input voltage is equal to the supply voltage.

Note 3: The output may be shorted to ground or either power supply indefinitely, provided the case temperature is below 125°C for the LM101A/107 and below 70°C for the LM301A/307.

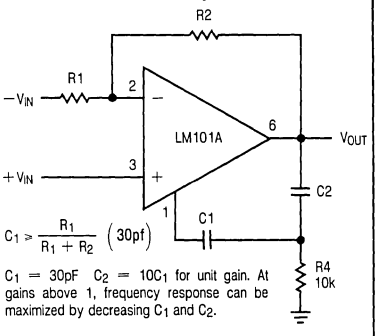
TYPICAL PERFORMANCE CHARACTERISTICS (LM101A)

Single Pole Compensation



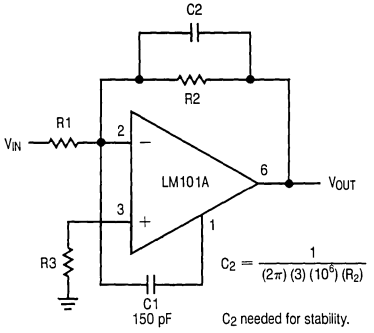
C_1 = 30pF for unity gain stability. At gains above 1 frequency response can be maximized by decreasing C_1.

Two Pole Compensation



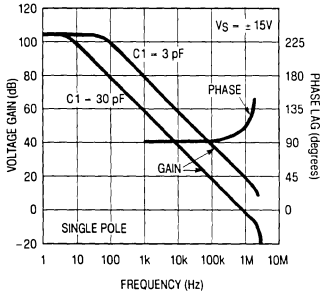
C_1 = 30pF C_2 = 10C_1 for unit gain. At gains above 1, frequency response can be maximized by decreasing C_1 and C_2.

Feedforward Compensation

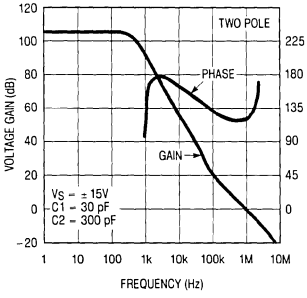


C_2 needed for stability.

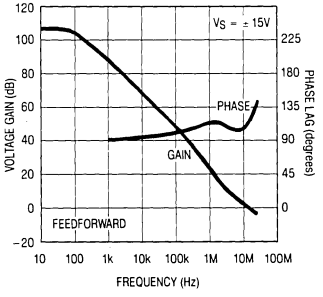
Open Loop Frequency Response



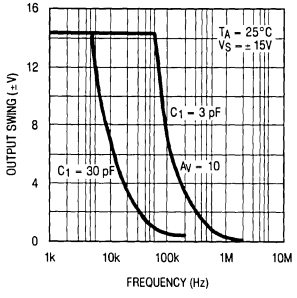
Open Loop Frequency Response



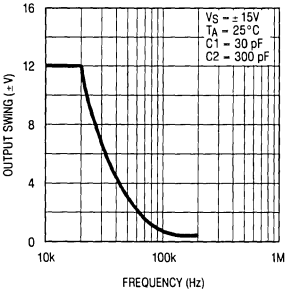
Open Loop Frequency Response



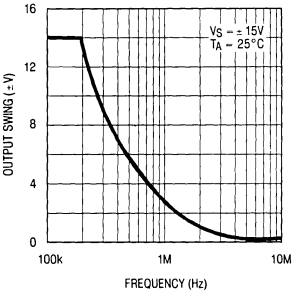
Single Pole Large Signal Frequency Response



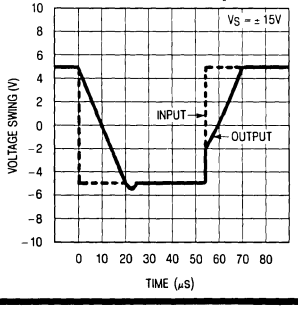
2 Pole Large Signal Frequency Response



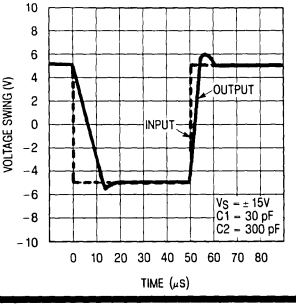
Feedforward Large Signal Frequency Response



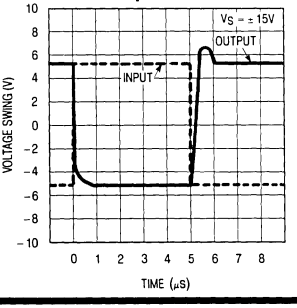
Single Pole Voltage Follower Pulse Response



2 Pole Voltage Follower Pulse Response

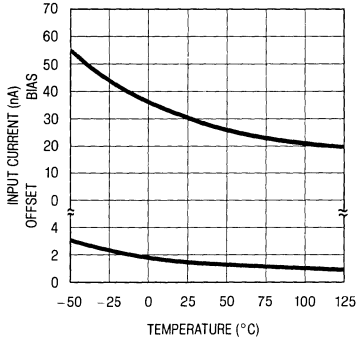


Feedforward Inverter Pulse Response

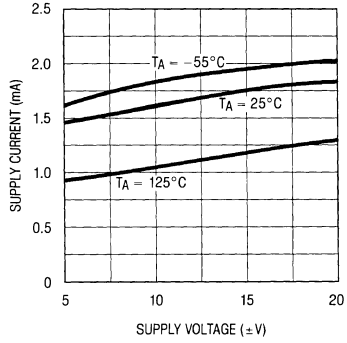


TYPICAL PERFORMANCE CHARACTERISTICS (LM101A/LM107)

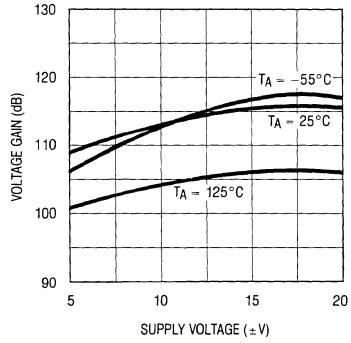
Input Current



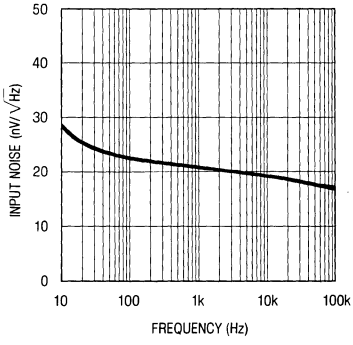
Supply Current



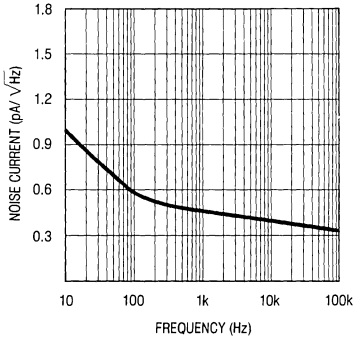
Voltage Gain



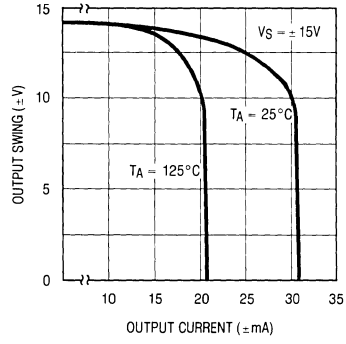
Input Noise Voltage



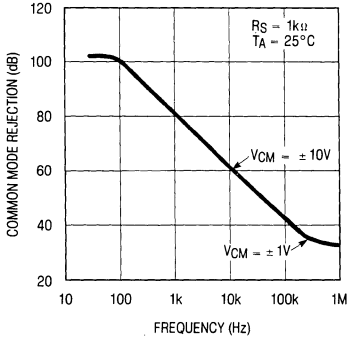
Input Noise Current



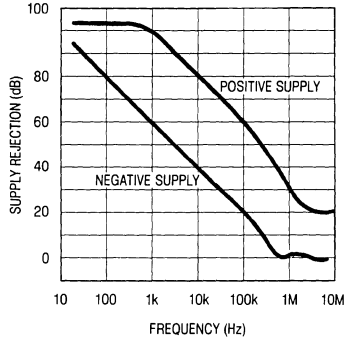
Current Limiting



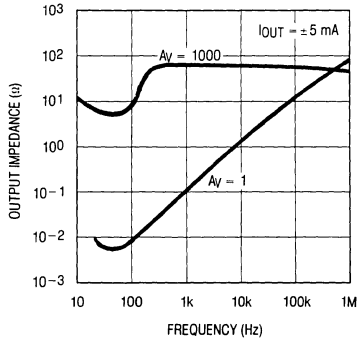
Common Mode Rejection



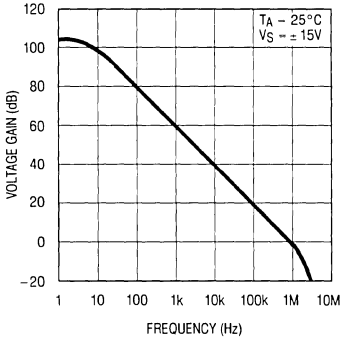
Power Supply Rejection



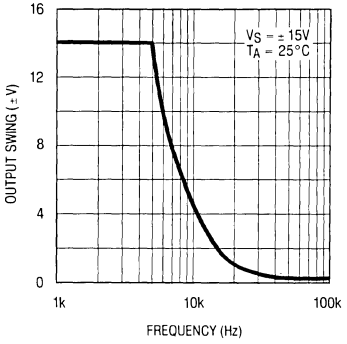
Closed Loop Output Impedance



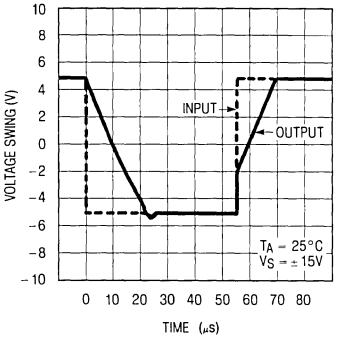
LM107
Open Loop Frequency Response



LM107
Large Signal Frequency Response

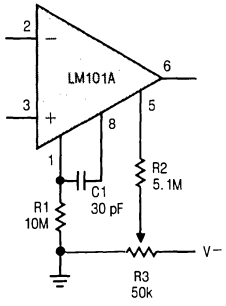


LM107
Voltage Follower Pulse Response

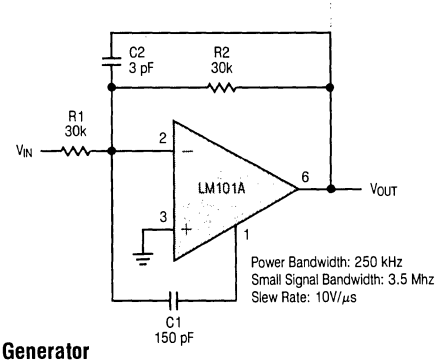


TYPICAL APPLICATIONS

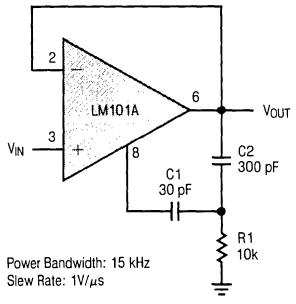
Standard Compensation and Offset Balancing Circuit



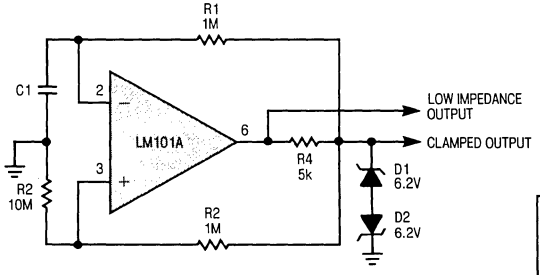
Fast Summing Amplifier



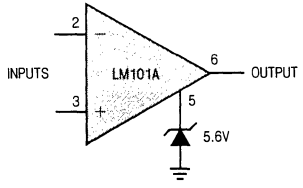
Fast Voltage Follower



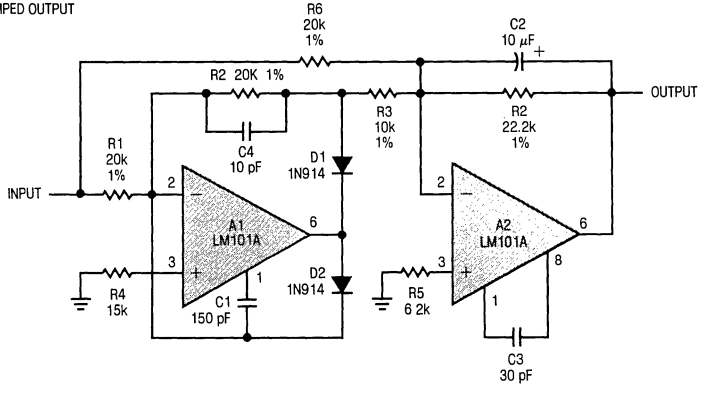
Low Frequency Square Wave Generator



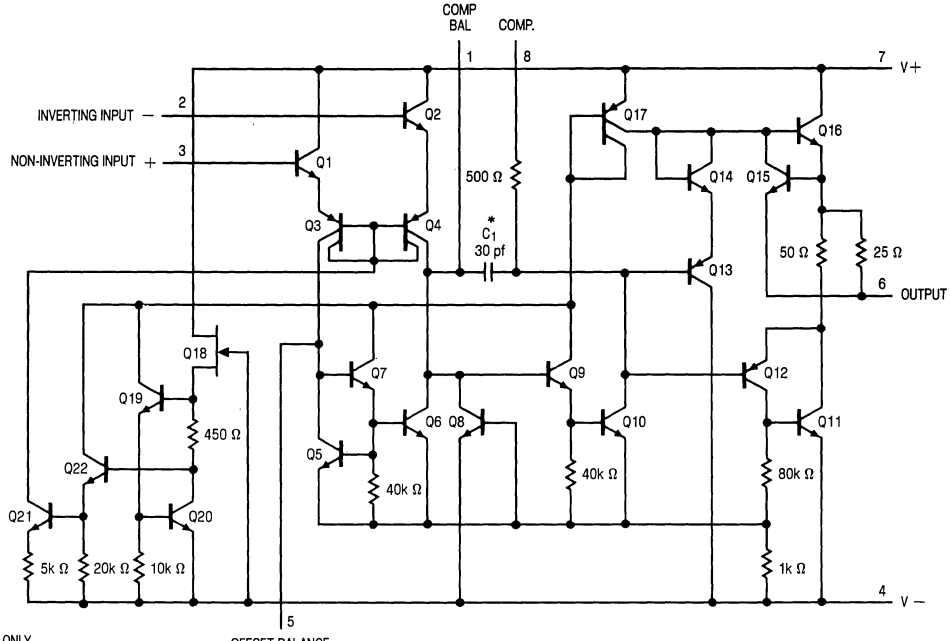
Voltage Comparator with Clamp



Precision Rectifier



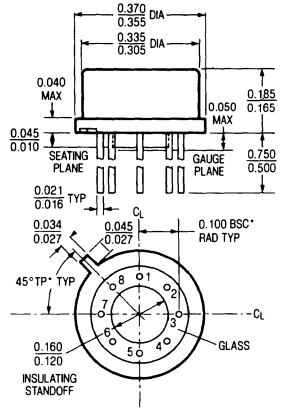
SCHEMATIC DIAGRAM



* C1 FOR LM107 ONLY
FOR LM107, THERE ARE NO INTERNAL CONNECTIONS TO PINS 1, 5 AND 8

PACKAGE DESCRIPTION

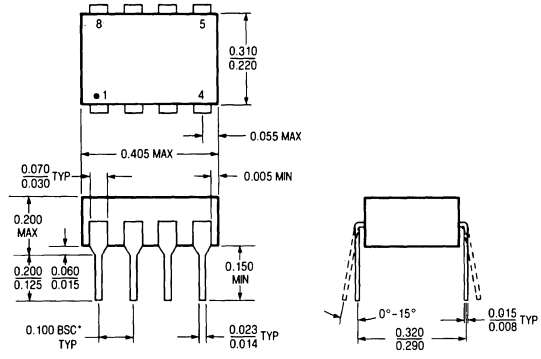
H Package
Metal Can



NOTE: DIMENSIONS IN INCHES

$T_j$max	Θ_{ja}	Θ_{jc}
150°C	150°C/W	45°C/W

J8 Package
8 Lead Hermetic Dip



NOTE: DIMENSIONS IN INCHES UNLESS OTHERWISE NOTED.
*LEADS WITHIN 0.007 OF TRUE POSITION (TP) AT GAUGE PLANE

$T_j$max	Θ_{ja}
150°C	100°C/W

FEATURES

- *Guaranteed* 200pA max. input offset current
- *Guaranteed* 2nA max. input bias current
- *Guaranteed* 600μA max. supply current
- *Guaranteed* 0.5mV max. offset voltage
- *Guaranteed* 5μV/°C max. drift
- Wide supply voltage range: ± 2V to ± 18V

APPLICATIONS

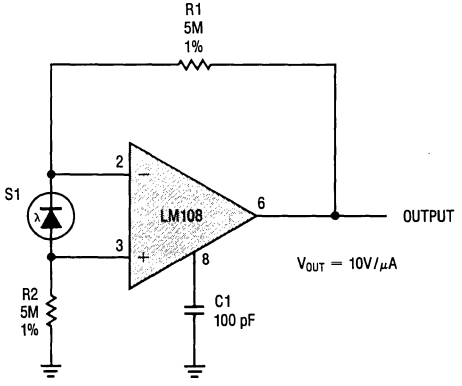
- Integrators
- Transducer amplifiers
- Analog memories
- Light meters

DESCRIPTION

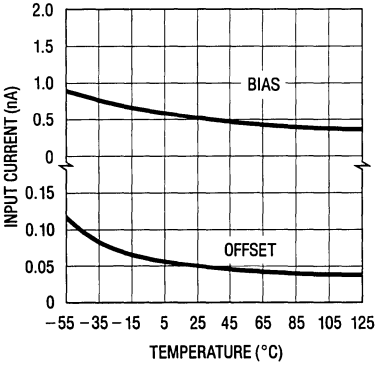
The LM108 series of precision operational amplifiers are particularly well-suited for high source impedance applications requiring low offset and bias currents as well as low power dissipation. Unlike FET input amplifiers, the offset and bias currents of the LM108 do not change significantly with temperature variations. Advanced design, processing and testing techniques make Linear's LM108 a superior choice over previous devices.

A photodiode sensor application is shown below. For applications requiring higher performance, see the LT1008, and LT1012.

Amplifier For Photodiode Sensor



Input Currents



ABSOLUTE MAXIMUM RATINGS

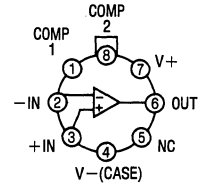
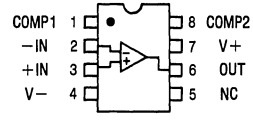
Supply Voltage
- LM108A/LM108 ..... ±20V
- LM308A/LM308 ..... ±18V

Differential Input Current (Note 1)..... ±10mA
Input Voltage (Note 2)..... ±15V
Output Short Circuit Duration..... Indefinite
Operating Temperature Range
- LM108A/LM108 ..... −55°C to 125°C
- LM308A/LM308 ..... 0°C to 70°C

Storage Temperature Range
- All Devices..... −65°C to 150°C

Lead Temperature (Soldering, 10 sec.)..... 300°C

PACKAGE/ORDER INFORMATION

	ORDER PART NO.
TOP VIEW  METAL CAN H PACKAGE	LM108AH LM108H LM308AH LM308H
TOP VIEW  PLASTIC DIP N8 PACKAGE	LM308AN8 LM308N8

ELECTRICAL CHARACTERISTICS ±5V ≤ V_s ≤ ±20V and −55°C ≤ T_A ≤ 125°C, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		LM108A MIN	LM108A TYP	LM108A MAX	LM108 MIN	LM108 TYP	LM108 MAX	UNITS
V_{OS}	Input Offset Voltage	T_A = 25°C			0.3	0.5		0.7	2.0	mV
			●			1.0			3.0	mV
$\frac{\Delta V_{OS}}{\Delta Temp}$	Average Temperature Coefficient of Input Offset Voltage		●		1.0	5.0		3.0	15	µV/°C
I_{OS}	Input Offset Current	T_A = 25°C			0.05	0.2		0.05	0.2	nA
			●			0.4			0.4	nA
$\frac{\Delta I_{OS}}{\Delta Temp}$	Average Temperature Coefficient of Input Offset Current		●		0.5	2.5		0.5	2.5	pA/°C
I_B	Input Bias Current	T_A = 25°C			0.5	2.0		0.5	2.0	nA
			●			3.0			3.0	nA
A_{VOL}	Large Signal Voltage Gain	T_A = 25°C, V_S ± 15V, V_{OUT} = ± 10V, R_L ≥ 10kΩ		80	300		50	300		V/mV
			●	40			25			V/mV
CMRR	Common Mode Rejection Ratio		●	96	110		85	100		dB
PSRR	Power Supply Rejection Ratio		●	96	110		80	96		dB
	Input Voltage Range	V_S = ± 15V	●	± 13.5			± 13.5			V
V_{OUT}	Output Voltage Swing	V_S = ± 15V, R_L = 10kΩ	●	± 13	± 14		± 13	± 14		V
R_{IN}	Input Resistance	T_A = 25°C (Note 3)		30	70		30	70		MΩ
I_S	Supply Current	T_A = 25°C			0.3	0.6		0.3	0.6	mA
		T_A = 125°C			0.15	0.4		0.15	0.4	mA

ELECTRICAL CHARACTERISTICS $\pm 5V \leq V_S \leq \pm 15V$ and $0°C \leq T_A \leq 70°C$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		LM308A MIN	LM308A TYP	LM308A MAX	LM308 MIN	LM308 TYP	LM308 MAX	UNITS
V_{OS}	Input Offset Voltage	$T_A = 25°C$			0.3	0.5		2.0	7.5	mV
			●			0.73			10	mV
$\frac{\Delta V_{OS}}{\Delta Temp}$	Average Temperature Coefficient of Input Offset Voltage		●		2.0	5.0		6.0	30	µV/°C
I_{OS}	Input Offset Current	$T_A = 25°C$			0.2	1.0		0.2	1.0	nA
			●			1.5			1.5	nA
$\frac{\Delta I_{OS}}{\Delta Temp}$	Average Temperature Coefficient of Input Offset Current		●		2.0	10		2.0	10	pA/°C
I_B	Input Bias Current	$T_A = 25°C$			1.5	7.0		1.5	7.0	nA
			●			10			10	nA
A_{VOL}	Large Signal Voltage Gain	$T_A = 25°C$, $V_S \pm 15V$, $V_{OUT} = \pm 10V$, $R_L \geq 10k\Omega$		80	300		25	300		V/mV
			●	60			15			V/mV
CMRR	Common Mode Rejection Ratio		●	96	110		80	100		dB
PSRR	Power Supply Rejection Ratio		●	96	110		80	96		dB
	Input Voltage Range	$V_S = \pm 15V$	●	±14			±14			V
V_{OUT}	Output Voltage Swing	$V_S = \pm 15V$ $R_L = 10k\Omega$	●	±13	±14		±13	±14		V
R_{IN}	Input Resistance	$T_A = 25°C$ (Note 3)		10	40		10	40		MΩ
I_S	Supply Current	$T_A = 25°C$			0.3	0.8		0.3	0.8	mA

The ● denotes the specifications which apply over the full operating temperature range.

For MIL-STD components, please refer to LTC 883 data sheet for test listing and parameters.

Note 1: Differential input voltages greater than 1V will cause excessive current to flow through the input protection diodes unless current limiting resistance is used.

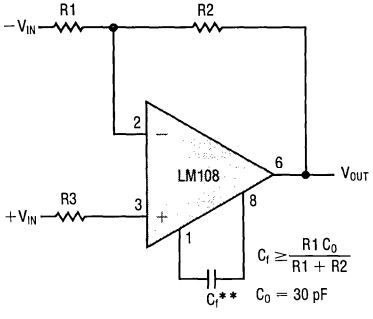
Note 2: For supply voltages less than ± 15V, the maximum input voltage is equal to the supply voltage.

Note 3: Guaranteed by design.

TYPICAL APPLICATIONS

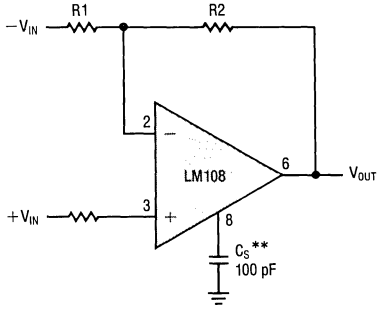
COMPENSATION CIRCUITS

Standard Compensation Circuit



** BANDWIDTH AND SLEW RATE ARE PROPORTIONAL TO $1/C_f$

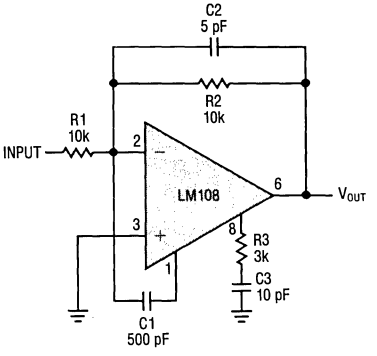
Alternate* Frequency Compensation



* IMPROVES REJECTION OF POWER SUPPLY NOISE BY A FACTOR OF TEN.

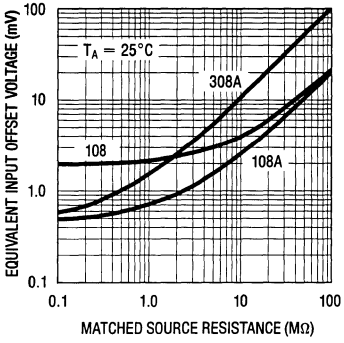
** BANDWIDTH AND SLEW RATE ARE PROPORTIONAL TO $1/C_S$

Feedforward Compensation

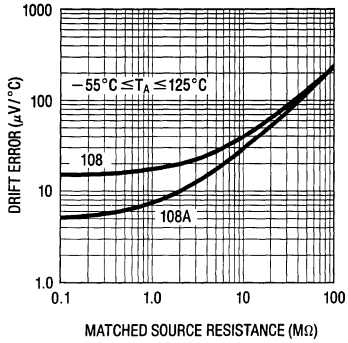


TYPICAL PERFORMANCE CHARACTERISTICS

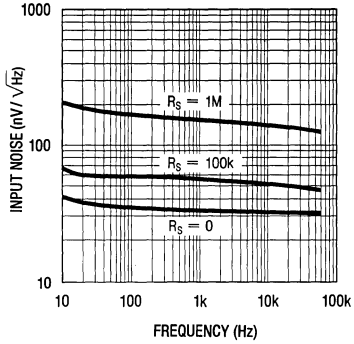
Guaranteed Offset Error



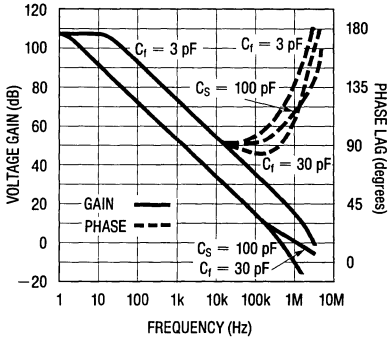
Guaranteed Drift Error



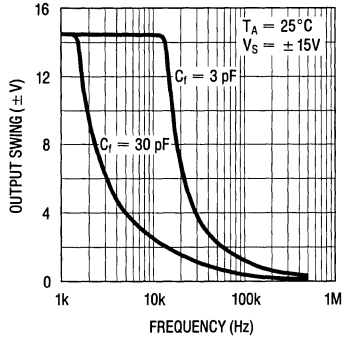
Input Noise Voltage



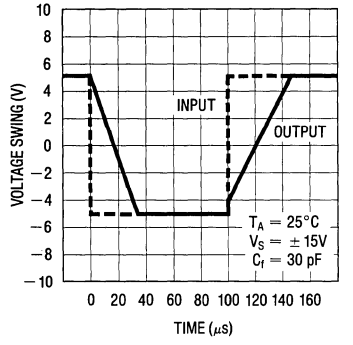
Open Loop Frequency Response



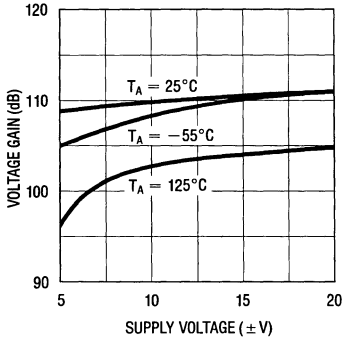
Large Signal Frequency Response



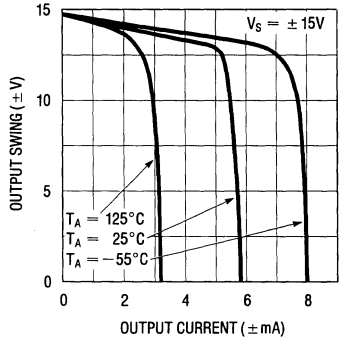
Voltage Follower Pulse Response



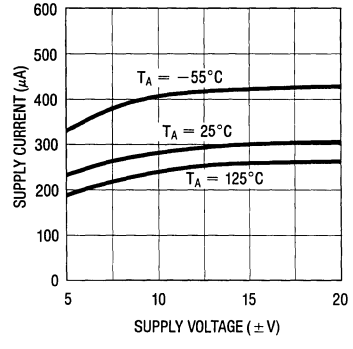
Voltage Gain



Output Swing



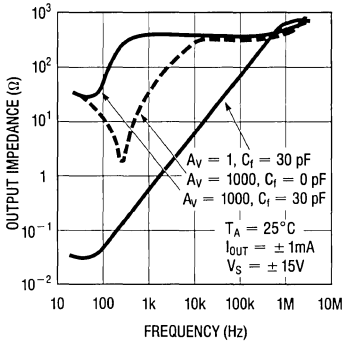
Supply Current



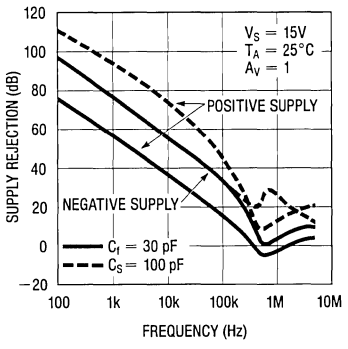
LINEAR TECHNOLOGY

TYPICAL PERFORMANCE CHARACTERISTICS

Closed Loop Output Impedance

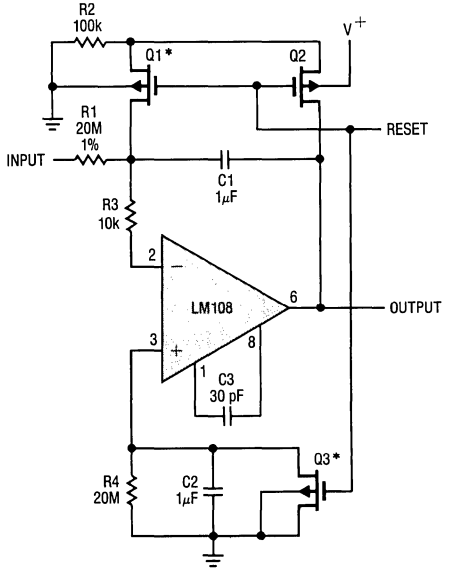


Power Supply Rejection



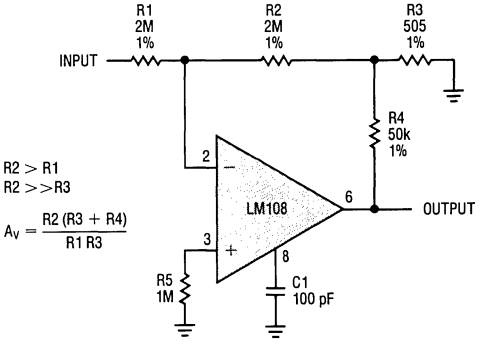
TYPICAL APPLICATIONS

Low Drift Integrator With Reset



* Q1 AND Q3 SHOULD NOT HAVE INTERNAL GATE-PROTECTION DIODES.

Inverting Amplifier With High Input Resistance

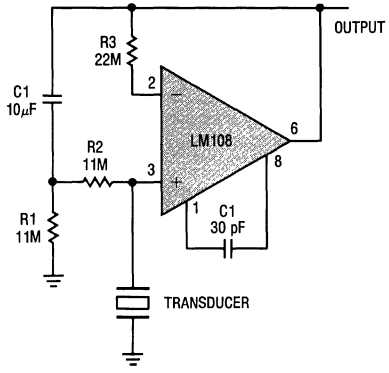


R2 > R1
R2 >>R3

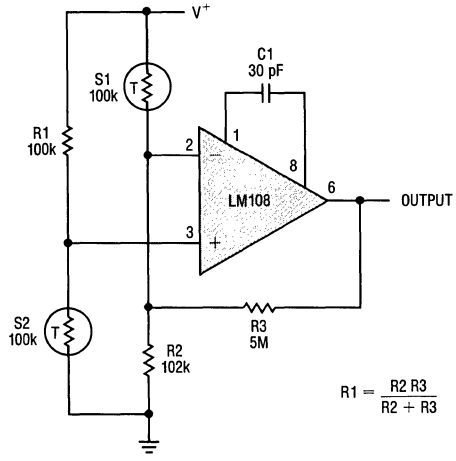
$$A_V = \frac{R2\,(R3 + R4)}{R1\,R3}$$

TYPICAL APPLICATIONS

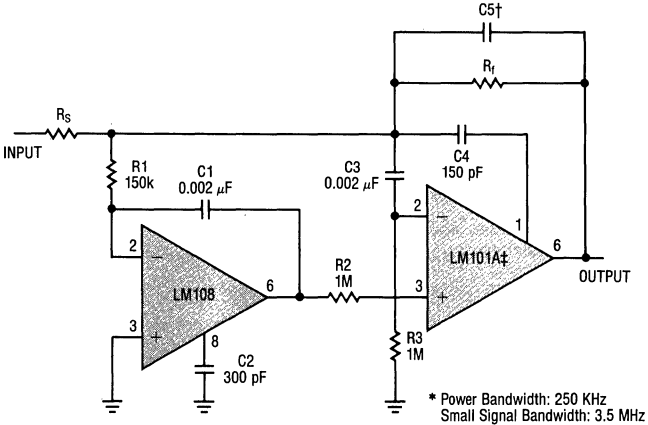
Amplifier For Piezoelectric Transducers



Amplifier For Bridge Transducers



Fast* Summing Amplifier

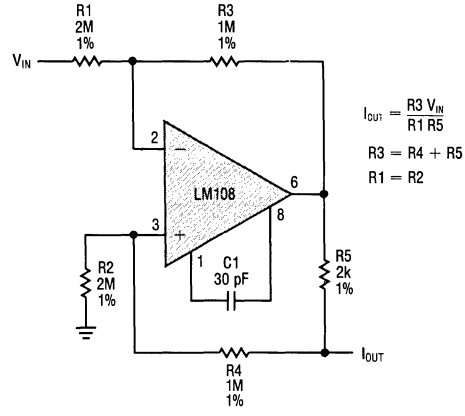


‡ In addition to increasing speed, the LM101A raises high and low frequency gain, increases output drive capability and eliminates thermal feedback.

* Power Bandwidth: 250 KHz
Small Signal Bandwidth: 3.5 MHz
Slew Rate: 10V/μS

$$\dagger C5 = \frac{6 \times 10^{-8}}{R_f}$$

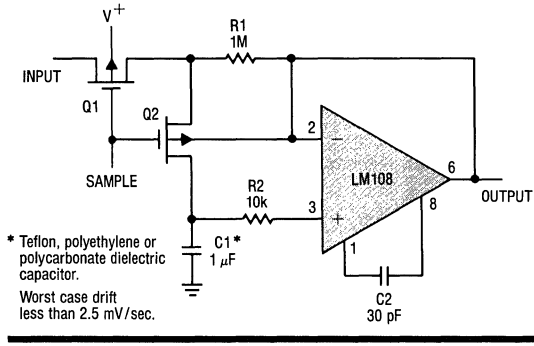
Bilateral Current Source



$$I_{OUT} = \frac{R3\ V_{IN}}{R1\ R5}$$

R3 = R4 + R5
R1 = R2

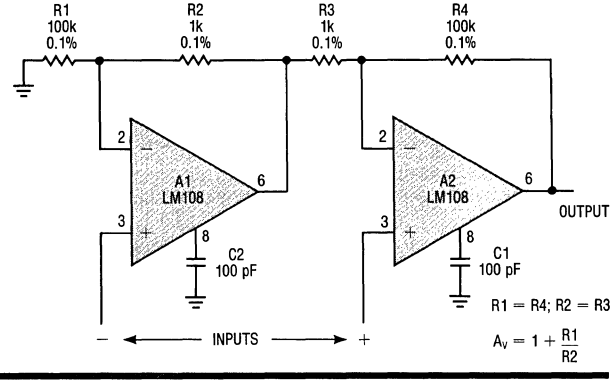
Sample and Hold



* Teflon, polyethylene or polycarbonate dielectric capacitor.

Worst case drift less than 2.5 mV/sec.

Differential Input Instrumentation Amplifier



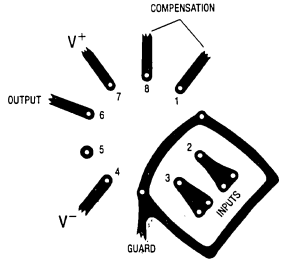
R1 = R4; R2 = R3

$$A_V = 1 + \frac{R1}{R2}$$

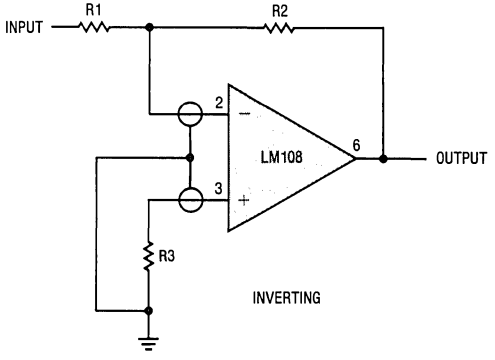
APPLICATIONS INFORMATION

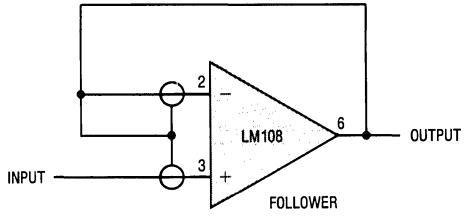
Input guarding

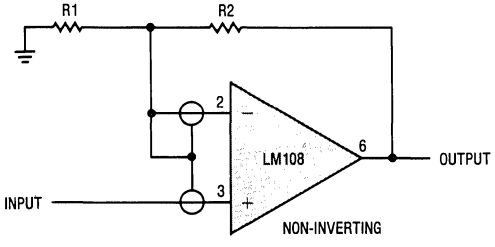
Input guarding is used to reduce surface leakage. Guarding both sides of the board is required. Bulk leakage reduction is less and depends on the guard ring width.



The guard ring is connected to a low impedance point at same potential as the sensitive input leads. Connections for various op amp configurations are shown below.

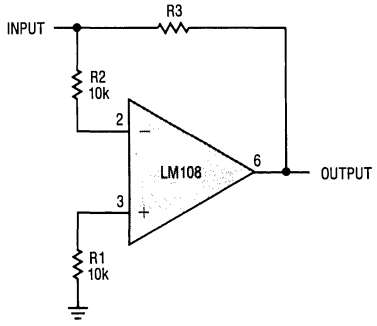




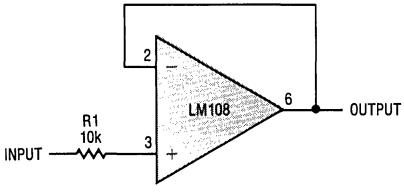


Input protection

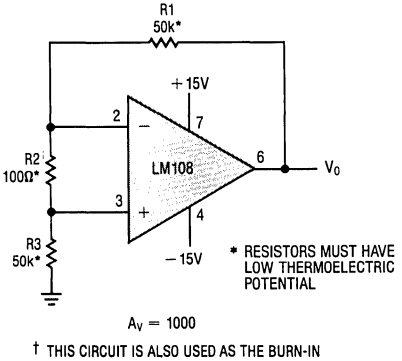
Current is limited by R2 even when input is connected to a voltage source outside the common mode range. If one supply reverses, current is controlled by R1. These resistors do not affect normal operation.



The input resistor controls the current when the input exceeds the supply voltages, when the power for the op amp is turned off, or when the output is shorted.



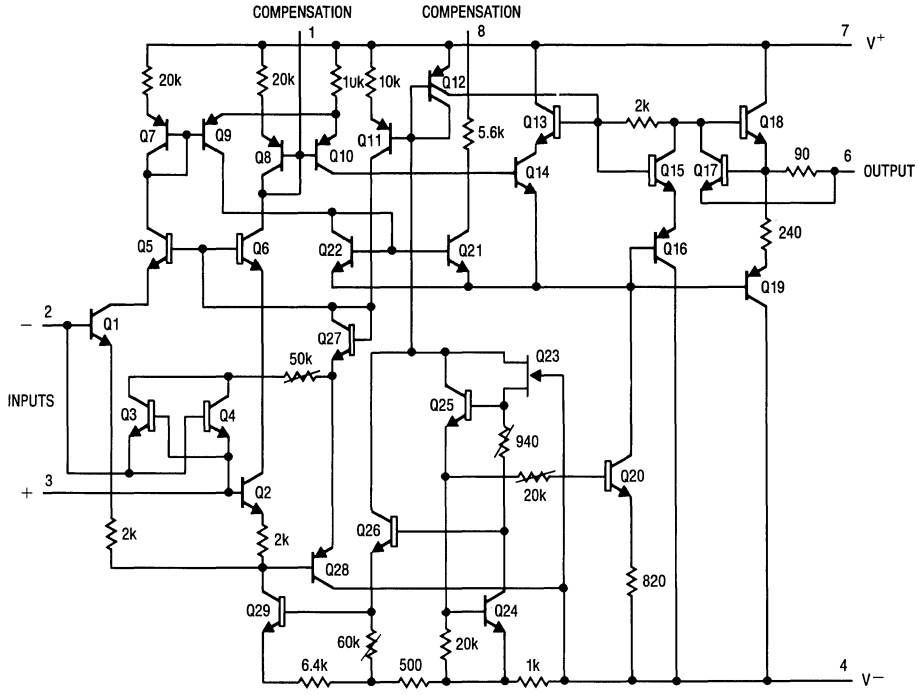
Offset Voltage Test Circuit†



$A_V = 1000$

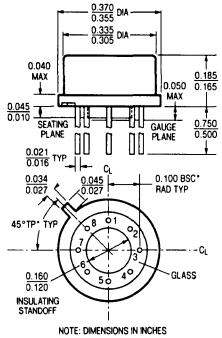
† THIS CIRCUIT IS ALSO USED AS THE BURN-IN CONFIGURATION WITH SUPPLY VOLTAGES EQUAL TO ±20V, R1 = R3 = 10k, R2 = 200Ω, A_V = 100.

SCHEMATIC DIAGRAM



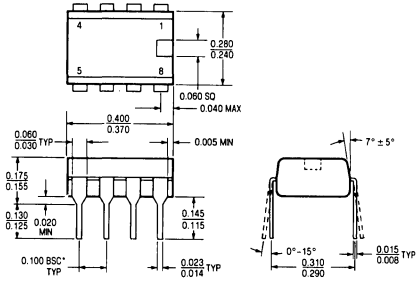
PACKAGE DESCRIPTION

H Package
Metal Can



$T_j$max	Θ_{ja}	Θ_{jc}
150°C	150°C/W	45°C/W

N8 Package
8 Lead Plastic



NOTE: DIMENSIONS IN INCHES UNLESS OTHERWISE NOTED.
*LEADS WITHIN 0.007 OF TRUE POSITION (TP) AT GAUGE PLANE.

$T_j$max	Θ_{ja}
100°C	130°C/W

High Speed Operational Amplifier

FEATURES

- *Guaranteed* 1.0mV Max. Input Offset Voltage
- *Guaranteed* 100,000 Min. Gain
- *Guaranteed* 50V/μs Slew Rate
- *Guaranteed* 20nA Max. Input Offset Current
- 15MHz Bandwidth
- Unity Gain Stable

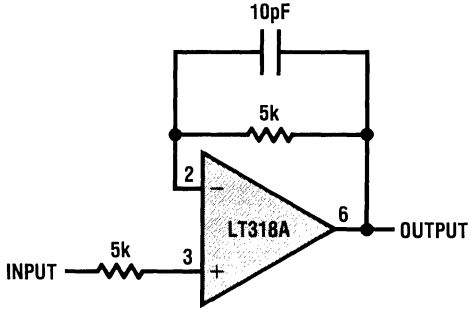
APPLICATIONS

- Wideband Amplifiers
- High Frequency Absolute Value Circuits
- D/A Converter Amplifiers
- Fast Integrators

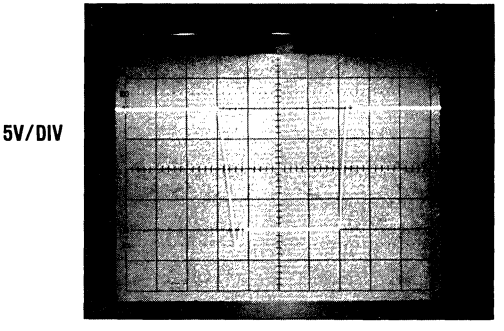
DESCRIPTION

The LT118A is an improved version of the industry standard LM118. The LT118A features lower input offset voltage, lower input offset currents, higher gain and higher common mode and power supply rejection. Because of these enhancements, the LT118A will improve the accuracy of most applications. Unlike many wideband amplifiers, the LT118A is unity gain stable and has a slew rate of 50V/μs. When used in inverting amplifier applications, feedforward compensation can be used to achieve slew rates in excess of 150V/μs. Linear Technology Corporation's advanced processing techniques make the LT118A an ideal choice for high speed applications.

Voltage Follower



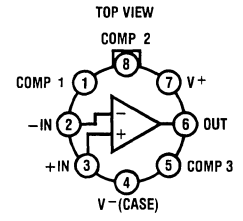
Voltage Follower Pulse Response



ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... ±20V
Differential Input Current (Note 1) ..... ±10mA
Input Voltage (Note 2) ..... ±20V
Output Short Circuit Duration ..... Indefinite
Operating Temperature Range
LT118A/LM118 ..... −55°C to 125°C
LT318A/LM318 ..... 0°C to 70°C
Storage Temperature Range
All Devices ..... −65°C to 150°C
Lead Temperature (Soldering, 10 sec.) ..... 300°C

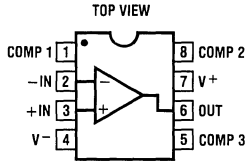
PACKAGE/ORDER INFORMATION



METAL CAN H PACKAGE

ORDER PART NUMBER

LT118AH
LM118H
LT318AH
LM318H



HERMETIC DIP J8 PACKAGE
PLASTIC DIP N8 PACKAGE

LT118AJ8
LM118J8
LT318AJ8
LM318J8
LT318AN8
LM318N8

ELECTRICAL CHARACTERISTICS (Note 3)

SYMBOL	PARAMETER	CONDITIONS		LT118A MIN	LT118A TYP	LT118A MAX	LM118 MIN	LM118 TYP	LM118 MAX	UNITS
V_{OS}	Input Offset Voltage				0.5	1		2	4	mV
			●		1	2			6	mV
I_{OS}	Input Offset Current				6	20		6	50	nA
			●		10	30			100	nA
I_B	Input Bias Current				120	250		120	250	nA
			●			500			500	nA
R_{IN}	Input Resistance			1	3		1	3		MΩ
A_V	Large Signal Voltage Gain	$V_S = \pm 15V$, $V_{OUT} = \pm 10V$, $R_L \geq 2k\Omega$		100	500		50	200		V/mV
			●	100			25			V/mV
SR	Slew Rate	$V_S = \pm 15V$, $A_V = 1$		50	70		50	70		V/μs
GBW	Gain Bandwidth Product	$V_S = \pm 15V$			15			15		MHz
	Output Voltage Swing	$V_S = \pm 15V$, $R_L = 2k\Omega$	●	±12	±13		±12	±13		V
	Input Voltage Range	$V_S = \pm 15V$	●	±11.5			±11.5			V
I_S	Supply Current				5	8		5	8	mA
		$T_A = 125°C$			4.5	7		4.5	7	mA
CMRR	Common Mode Rejection Ratio		●	86	100		80	100		dB
PSRR	Power Supply Rejection Ratio		●	86	100		70	80		dB

ELECTRICAL CHARACTERISTICS (Note 3)

SYMBOL	PARAMETER	CONDITIONS		LT318A MIN	LT318A TYP	LT318A MAX	LM318 MIN	LM318 TYP	LM318 MAX	UNITS
V_{OS}	Input Offset Voltage				0.5	1		4	10	mV
			●			2			15	mV
I_{OS}	Input Offset Current				10	20		30	200	nA
			●			30			750	nA
I_B	Input Bias Current				150	250		150	500	nA
			●			500			750	nA
R_{IN}	Input Resistance			0.5	3		0.5	3		MΩ
A_V	Large Signal Voltage Gain	$V_S = \pm 15V$, $V_{OUT} = \pm 10V$, $R_L \geq 2k\Omega$		100	500		25	200		V/mV
			●	100			20			V/mV
SR	Slew Rate	$V_S = \pm 15V$, $A_V = 1$		50	70		50	70		V/μs
GBW	Gain Bandwidth Product	$V_S = \pm 15V$			15			15		MHz
	Output Voltage Swing	$V_S = \pm 15V$, $R_L = 2k\Omega$	●	±12	±13		±12	±13		V
	Input Voltage Range	$V_S = \pm 15V$	●	±11.5			±11.5			V
I_S	Supply Current				5	10		5	10	mA
CMRR	Common Mode Rejection Ratio		●	86	100		70	100		dB
PSRR	Power Supply Rejection Ratio		●	86	100		65	80		dB

The ● denotes those specifications which apply over the full operating temperature range.

The shaded electrical specifications indicate those parameters which have been improved or guaranteed test limits provided for the first time.

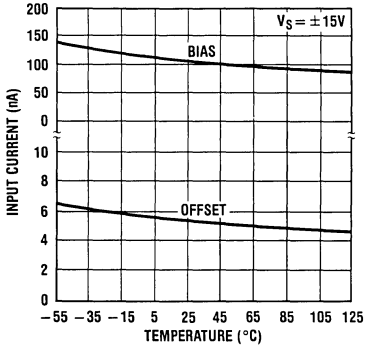
Note 1: The inputs are shunted with back-to-back zeners for overvoltage protection. Excessive current will flow if a differential voltage greater than 5V is applied to the inputs.

Note 2: For supply voltages less than ±15V, the maximum input voltage is equal to the supply voltage.

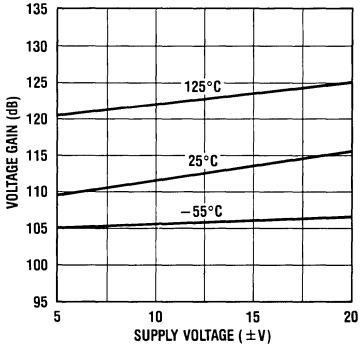
Note 3: These specifications apply for $\pm 5V \leq V_S \leq \pm 20V$. The power supplies must be bypassed with a 0.1μF or greater disc capacitor within 4 inches of the device.

TYPICAL PERFORMANCE CHARACTERISTICS

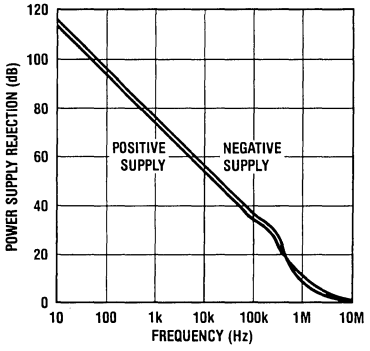
Input Current



Voltage Gain

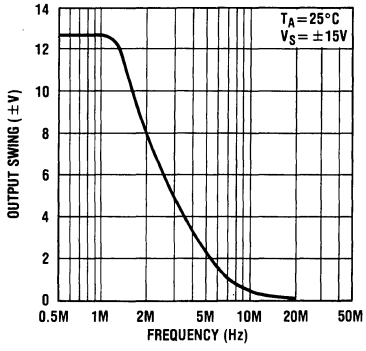


Power Supply Rejection

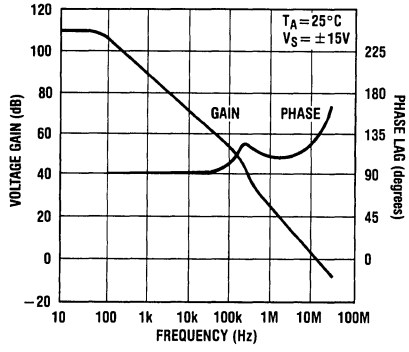


TYPICAL PERFORMANCE CHARACTERISTICS

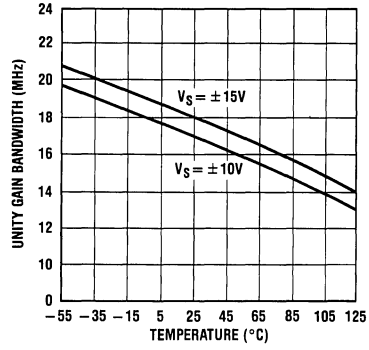
Large Signal Frequency Response



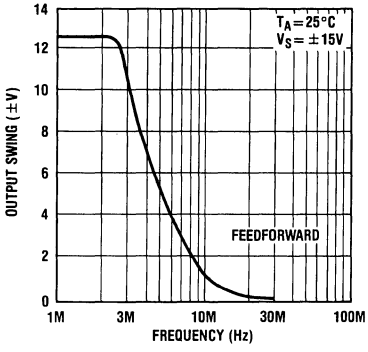
Open Loop Frequency Response



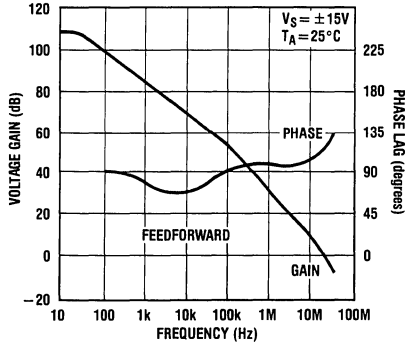
Unity Gain Bandwidth



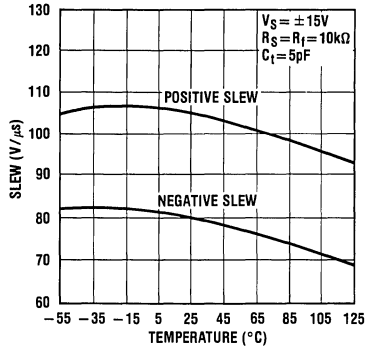
Large Signal Frequency Response



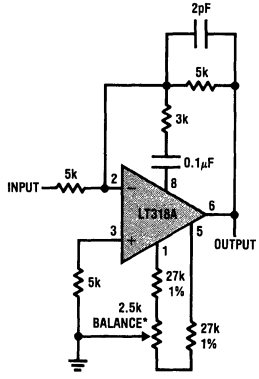
Open Loop Frequency Response



Voltage Follower Slew Rate

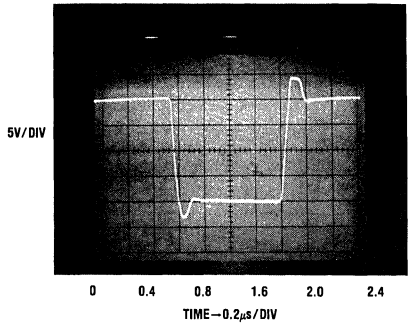


Feedforward Compensation for Slew Rates of 150V/μs



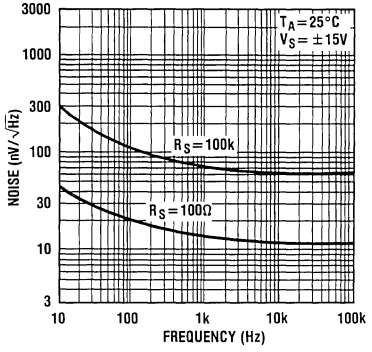
*BALANCE CIRCUIT NECESSARY FOR INCREASED SLEW RATE

Pulse Response of Feedforward Inverter

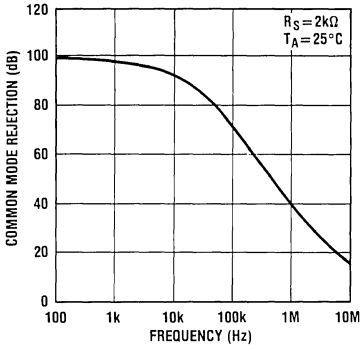


TYPICAL PERFORMANCE CHARACTERISTICS

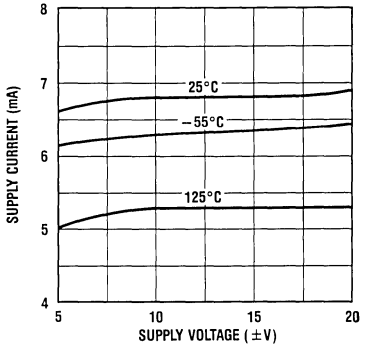
Input Noise Voltage



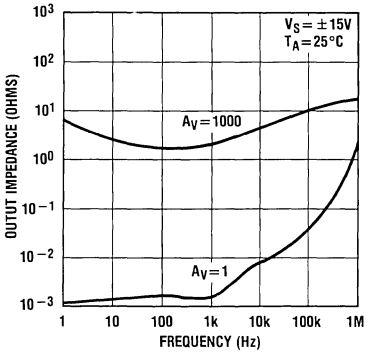
Common Mode Rejection



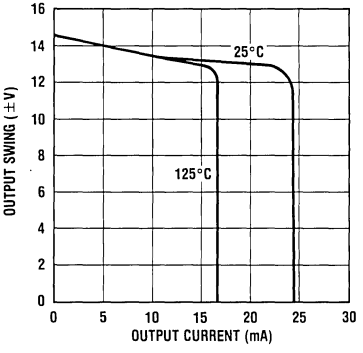
Supply Current



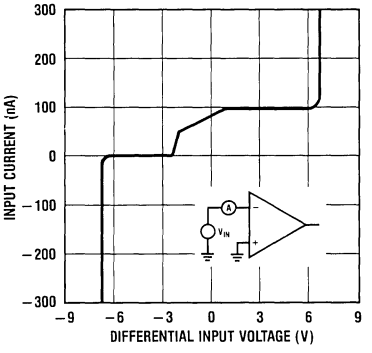
Closed Loop Output Impedance



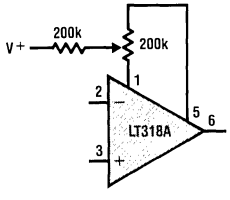
Current Limiting



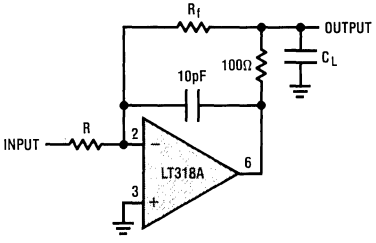
LT118A Input Current



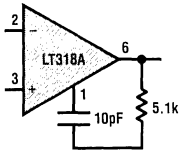
Offset Balancing



Isolating Large Capacitive Loads

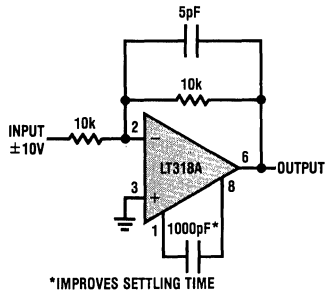


Overcompensation for Increased Stability



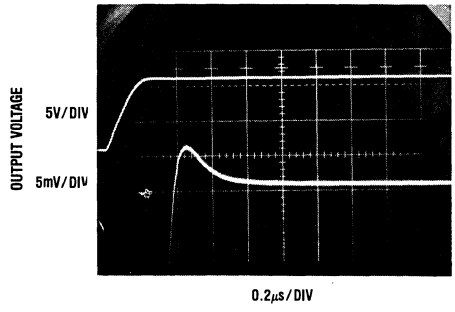
SETTLING TIME CIRCUITS

Settling Time Test Circuit

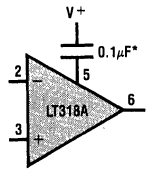


*IMPROVES SETTLING TIME

Settling Time

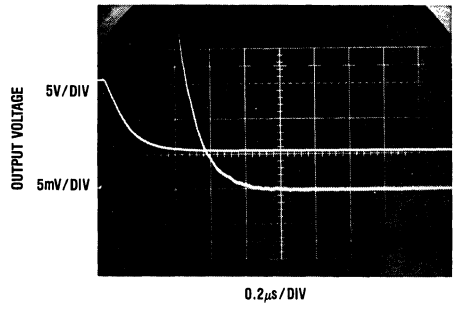


Alternate Compensation for Improved Settling Time



*IMPROVES SETTLING TIME

Settling Time



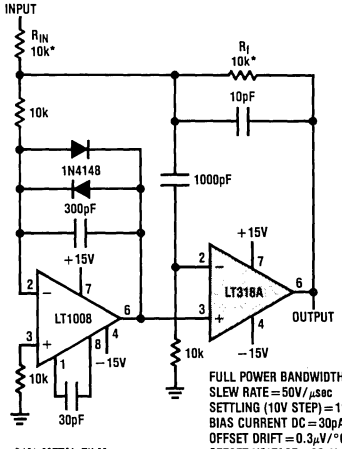
APPLICATIONS INFORMATION

Because of their wider bandwidth, the LT118A and LM118 operational amplfiers require more application care than most general purpose low frequency amplifiers. One of the most critical requirements is that power supplies should be bypassed with a 0.1μF (or larger) disc ceramic capacitor within an inch of the device. Also, stray capacitance at either the input or output can cause oscillation. While input capacitance can be compensated by placing a capacitor across the feedback resistor, load capacitance must be minimized or isolated as shown. Even the 50pF input capacitance of a 1X scope probe can alter the response of the device.

Settling time, an important parameter in many high speed amplifier applications, is difficult to measure and optimize. Settling time is very "application dependent" and is influenced by external components, layout and the amplifier. In general, the settling time to 0.01% can be minimized by using a circuit similar to that shown. In addition to the compensation network shown, a capacitor is needed across the feedback resistor to minimize ringing.

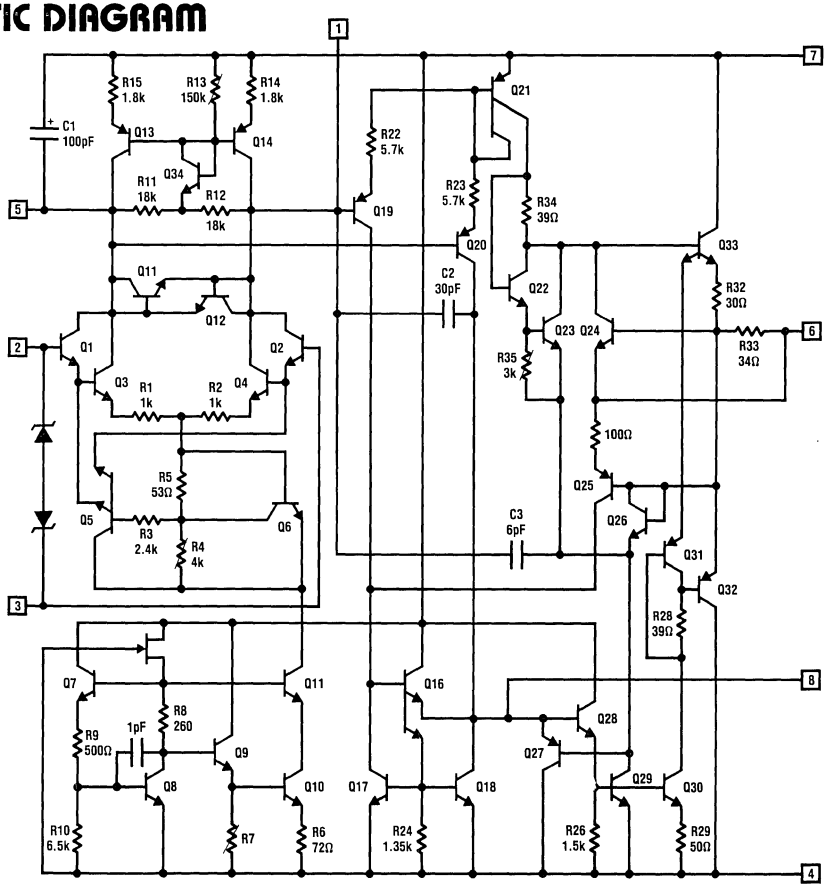
Power supply bypassing can also affect settling time. The amplifier has low power supply rejection ratio at high frequencies, so transients and ringing on the supply leads can appear at the output. Large (22μF) solid tantalum capacitors are preferred to minimize supply aberrations.

Precision Inverting Amplifier



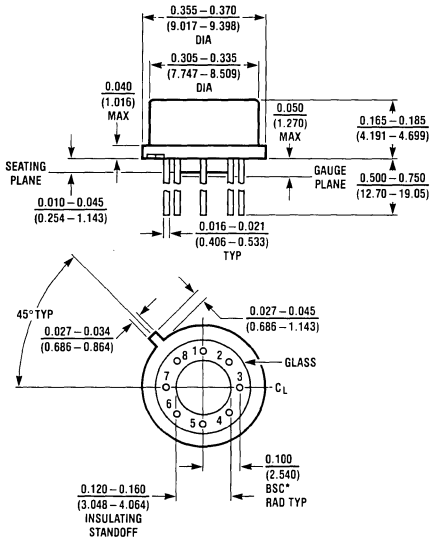
FULL POWER BANDWIDTH = 2MHz
SLEW RATE = 50V/μsec
SETTLING (10V STEP) = 12μs TO 0.01%
BIAS CURRENT DC = 30pA
OFFSET DRIFT = 0.3μV/°C
OFFSET VOLTAGE = 30μV

SCHEMATIC DIAGRAM



PACKAGE DESCRIPTION

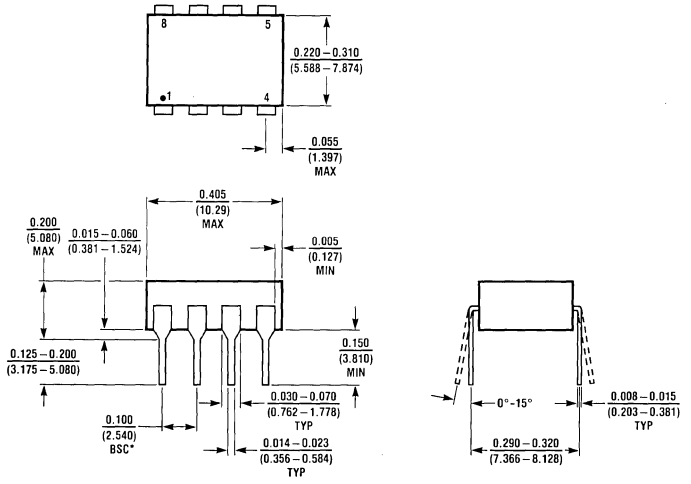
H Package
Metal Can



NOTE: DIMENSIONS IN INCHES

$T_j$max	θ_{ja}	θ_{jc}
150°C	150°C/W	45°C/W

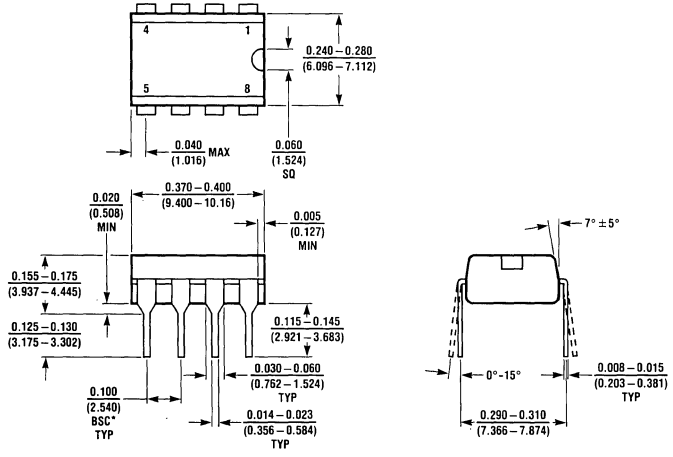
J8 Package
8 Lead Hermetic DIP



NOTE: DIMENSIONS IN INCHES UNLESS OTHERWISE NOTED
*LEADS WITHIN 0.007 OF TRUE POSITION (TP) AT GAUGE PLANE

$T_j$max	θ_{ja}
150°C	100°C/W

N8 Package
8 Lead Plastic



NOTE: DIMENSIONS IN INCHES UNLESS OTHERWISE NOTED
*LEADS WITHIN 0.007 OF TRUE POSITION (TP) AT GAUGE PLANE

$T_j$max	θ_{ja}
100°C	130°C/W

FEATURES

- *Guaranteed max.* 0.5μV/°C Drift
- *Guaranteed max.* 0.6μV pk-pk Noise
- *Guaranteed max.* 2nA Bias Current
- *Guaranteed minimum* 114dB CMRR

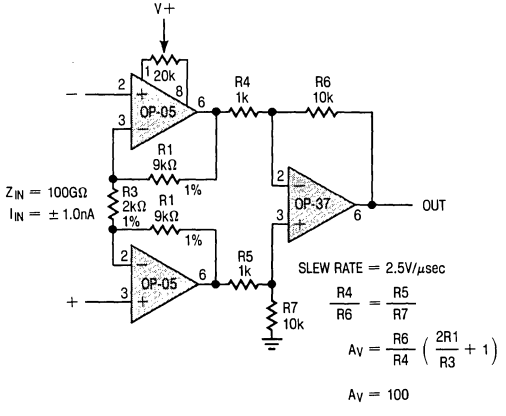
APPLICATIONS

- Strain Gauges
- Thermocouple Amplifiers
- Instrumentation Amplifiers
- Medical Instruments

DESCRIPTION

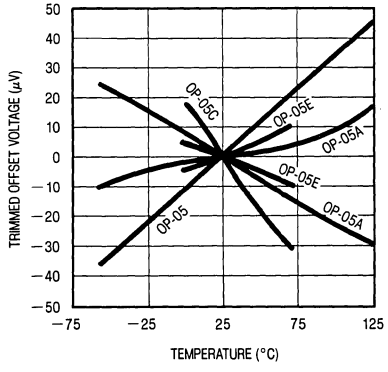
The OP-05 is an internally compensated op-amp which provides excellent input offset voltage, low bias current, very high common mode rejection, and low offset voltage drift with temperature when the input offset voltage is externally trimmed to zero. Direct replacement of similar devices in existing systems can result in significant system performance improvement without redesign. The OP-05 is particularly well suited for instrumentation and low signal level applications where precision and stability over time and temperature are important. Internal frequency compensation enhances the OP-05's versatility for a wide variety of precision op-amp uses. Linear's advanced design, process and test techniques ensure device performance as well as reliability. An instrumentation amplifier application is shown below. For higher performance requirements see the LT1001 single precision op amp and the LT1002 dual matched precision op amp series.

Instrumentation Amplifier



Trimmed Offset Voltage with Temperature of Six Representative Units

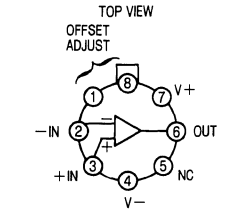
(Offset Trimmed to Zero at 25°C with 20kΩ Pot)



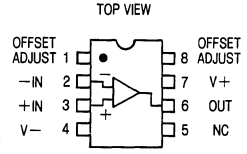
ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... ±22V
Differential Input Voltage ..... ±30V
Input Voltage Equal to Supply Voltage
Output Short Circuit Duration ..... Indefinite
Operating Temperature Range
OP-05/OP-05A ..... −55°C to 125°C
OP-05E/OP-05C ..... 0°C to 70°C
Storage Temperature Range
All Devices ..... −65°C to 150°C
Lead Temperature (Soldering, 10 sec.) ..... 300°C

PACKAGE/ORDER INFORMATION



METAL CAN H PACKAGE



HERMETIC J8 PACKAGE

PLASTIC DIP N8 PACKAGE

ORDER PART NO.	OFFSET VOLTAGE MAX
OP-05AH	0.15mV
OP-05H	0.5mV
OP-05EH	0.5mV
OP-05CH	1.3mV
OP-05AJ8	0.15mV
OP-05J8	0.5mV
OP-05EJ8	0.5mV
OP-05CJ8	1.3mV
OP-05EN8	0.5mV
OP-05CN8	1.3mV

ELECTRICAL CHARACTERISTICS $V_S = \pm 15V$, $T_A = 25°C$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	OP-05A MIN	OP-05A TYP	OP-05A MAX	OP-05 MIN	OP-05 TYP	OP-05 MAX	UNITS
V_{OS}	Input Offset Voltage			0.07	0.15		0.2	0.5	mV
$\frac{\Delta V_{OS}}{\Delta Time}$	Long Term Input Offset Voltage Stability	(Notes 1 and 2)		0.2	1.0		0.2	1.0	µV/Month
I_{OS}	Input Offset Current			0.7	2.0		1.0	2.8	nA
I_B	Input Bias Current			±0.7	±2.0		±1.0	±3.0	nA
e_n	Input Noise Voltage	0.1Hz to 10Hz (Note 2)		0.35	0.6		0.35	0.6	μV_{p-p}
	Input Noise Voltage Density	f_o = 10Hz f_o = 100Hz (Note 2) f_o = 1000Hz		10.3 10.0 9.6	18.0 13.0 11.0		10.3 10.0 9.6	18.0 13.0 11.0	$nV/\sqrt{Hz}$
i_n	Input Noise Current	0.1Hz to 10Hz (Note 2)		14	30		14	30	pA_{p-p}
	Input Noise Current Density	f_o = 10Hz f_o = 100Hz (Note 2) f_o = 1000Hz		0.32 0.14 0.12	0.80 0.23 0.17		0.32 0.14 0.12	0.80 0.23 0.17	$pA/\sqrt{Hz}$
R_{in}	Input Resistance Differential Mode	(Note 3)	30	80		20	60		MΩ
	Input Resistance Common Mode			200			200		GΩ
	Input Voltage Range		±13.5	±14.0		±13.5	±14.0		V
CMRR	Common Mode Rejection Ratio	V_{CM} = ±13.5V	114	126		114	126		dB
PSRR	Power Supply Rejection Ratio	V_S = ±3V to ±18V	100	108		100	108		dB
A_{VOL}	Large Signal Voltage Gain	$R_L \geq 2k\Omega$, V_O = ±10V $R_L \geq 500\Omega$, V_O = ±0.5V V_S = ±3V (Note 3)	300 150	500 500		200 150	500 500		V/mV
V_{OUT}	Maximum Output Voltage Swing	$R_L \geq 10k\Omega$ $R_L \geq 2k\Omega$ $R_L \geq 1k\Omega$	±12.5 ±12.0 ±10.5	±13.0 ±12.8 ±12.0		±12.5 ±12.0 ±10.5	±13.0 ±12.8 ±12.0		V
SR	Slew Rate	$R_L \geq 2k\Omega$ (Note 2)	0.1	0.3		0.1	0.3		V/µS
GBW	Closed Loop Bandwidth	A_{VCL} = +1 (Note 2)	0.4	0.6		0.4	0.6		MHz
Z_o	Open Loop Output Impedance	V_O = 0, I_O = 0, f = 10Hz		60			60		Ω
P_d	Power Dissipation	No load V_S = ±3V, No load		90 4	120 6		90 4	120 6	mW
	Offset Adjustment Range	Null Pot = 20kΩ		±4			±4		mV

See Notes on page 2-202.

ELECTRICAL CHARACTERISTICS $V_S = \pm 15V$, $-55°C \leq T_A \leq 125°C$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		OP-05A MIN	OP-05A TYP	OP-05A MAX	OP-05 MIN	OP-05 TYP	OP-05 MAX	UNITS
V_{OS}	Input Offset Voltage		●		0.10	0.24		0.3	0.7	mV
$\frac{\Delta V_{OS}}{\Delta Temp}$	Average Input Offset Voltage Drift Without External Trim With External Trim	 Null Pot = 20kΩ (Note 2)	 ● ●		 0.3 0.2	 0.9 0.5		 0.7 0.3	 2.0 1.0	μV/°C
I_{OS}	Input Offset Current		●		1.0	4.0		1.8	5.6	nA
$\frac{\Delta I_{OS}}{\Delta Temp}$	Average Input Offset Current Drift	(Note 2)	●		5	25		8	50	pA/°C
I_B	Input Bias Current		●		±1.0	±4.0		±2.0	±6.0	nA
$\frac{\Delta I_B}{\Delta Temp}$	Average Input Bias Current Drift	(Note 2)	●		8	25		13	50	pA/°C
	Input Voltage Range		●	±13.0	±13.5		±13.0	±13.5		V
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm 13V$	●	110	123		110	123		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 3V$ to $\pm 18V$	●	94	106		94	106		dB
A_{VOL}	Large Signal Voltage Gain	$R_L \geq 2k\Omega$, $V_o = \pm 10V$	●	200	400		150	400		V/mV
V_{OUT}	Output Voltage Swing	$R_L \geq 2k\Omega$	●	±12.0	±12.6		±12.0	±12.6		V

ELECTRICAL CHARACTERISTICS $V_S = \pm 15V$, $T_A = 25°C$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	OP-05E MIN	OP-05E TYP	OP-05E MAX	OP-05C MIN	OP-05C TYP	OP-05C MAX	UNITS
V_{OS}	Input Offset Voltage			0.2	0.5		0.3	1.3	mV
$\frac{\Delta V_{OS}}{\Delta Time}$	Long Term Input Offset Voltage Stability	(Notes 1 and 2)		0.3	1.5		0.4	2.0	μV/Month
I_{OS}	Input Offset Current			1.2	3.8		1.8	6.0	nA
I_B	Input Bias Current			±1.2	±4.0		±1.8	±7.0	nA
e_n	Input Noise Voltage	0.1Hz to 10Hz (Note 2)		0.35	0.6		0.38	0.65	μV_{p-p}
	Input Noise Voltage Density	$f_o = 10Hz$ $f_o = 100Hz$ (Note 2) $f_o = 1000Hz$		10.3 10.0 9.6	18.0 13.0 11.0		10.5 10.2 9.8	20.0 13.5 11.5	nV/$\sqrt{Hz}$
i_n	Input Noise Current	0.1Hz to 10Hz (Note 2)		14	30		15	35	pA_{p-p}
	Input Noise Current Density	$f_o = 10Hz$ $f_o = 100Hz$ (Note 2) $f_o = 1000Hz$		0.32 0.14 0.12	0.80 0.23 0.17		0.35 0.15 0.13	0.90 0.27 0.18	pA/$\sqrt{Hz}$
R_{in}	Input Resistance Differential Mode	(Note 3)	15	50		8	33		MΩ
	Input Resistance Common Mode			160			120		GΩ
	Input Voltage Range		±13.5	±14.0		±13.5	±14.0		V
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm 13.5V$	110	123		100	120		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 3V$ to $\pm 18V$	94	106		90	104		dB
A_{VOL}	Large Signal Voltage Gain	$R_L \geq 2k\Omega$, $V_O = \pm 10V$ $R_L \geq 500\Omega$, $V_O = \pm 0.5V$ $V_S = \pm 3V$ (Note 3)	200 150	500 500		120 100	400 400		V/mV
V_{OUT}	Maximum Output Voltage Swing	$R_L \geq 10k\Omega$ $R_L \geq 2k\Omega$ $R_L \geq 1k\Omega$	±12.5 ±12.0 ±10.5	±13.0 ±12.8 ±12.0		±12.0 ±11.5	±13.0 ±12.8 ±12.0		V
SR	Slew Rate	$R_L \geq 2k\Omega$ (Note 2)	0.1	0.3		0.1	0.3		V/μS
GBW	Closed Loop Bandwidth	$A_{VCL} = +1$ (Note 2)	0.4	0.6		0.4	0.6		MHz
Z_o	Open Loop Output Impedance	$V_O = 0$, $I_O = 0$, $f = 10Hz$		60			60		Ω
P_d	Power Dissipation	No load $V_S = \pm 3V$, No load		90 4	120 6		95 4	150 8	mW
	Offset Adjustment Range	Null Pot = 20kΩ		±4			±4		mW

See Notes on page 2-202.

ELECTRICAL CHARACTERISTICS $V_S = \pm 15V$, $0°C \leq T_A \leq 70°C$.

SYMBOL	PARAMETER	CONDITIONS		OP-05E MIN	OP-05E TYP	OP-05E MAX	OP-05C MIN	OP-05C TYP	OP-05C MAX	UNITS
V_{OS}	Input Offset Voltage		●		0.25	0.6		0.35	1.6	mV
$\frac{\Delta V_{OS}}{\Delta Temp}$	Average Input Offset Voltage Drift									
	Without External Trim		●		0.7	2.0		1.3	4.5	μV/°C
	With External Trim	Null Pot = 20kΩ (Note 2)	●		0.2	0.6		0.4	1.5	μV/°C
I_{OS}	Input Offset Current		●		1.4	5.3		2.0	8.0	nA
$\frac{\Delta I_{OS}}{\Delta Temp}$	Average Input Offset Current Drift	(Note 2)	●		8	35		12	50	pA/°C
I_B	Input Bias Current		●		±1.5	±5.5		±2.2	±9.0	nA
$\frac{\Delta I_B}{\Delta Temp}$	Average Input Bias Current Drift	(Note 2)	●		13	35		18	50	pA/°C
	Input Voltage Range		●	±13.0	±13.5		±13.0	±13.5		V
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm 13V$	●	107	123		97	120		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 3V$ to $\pm 18V$	●	90	103		86	100		dB
A_{VOL}	Large Signal Voltage Gain	$R_L \geq 2k\Omega$, $V_o = \pm 10V$	●	180	450		100	400		V/mV
V_{OUT}	Output Voltage Swing	$R_L \geq 2k\Omega$	●	±12.0	±12.6		±11.0	±12.6		V

The ● denotes the specifications which apply over the full operating temperature range.

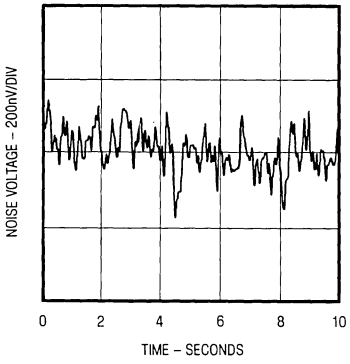
Note 1: Long term offset voltage stability is the average value of offset voltage vs. time plotted over extended periods following 30 days of operation. Values for time under 30 days of operation are typically 2.5μV following the first hour of operation.

Note 2: This parameter is sample tested.

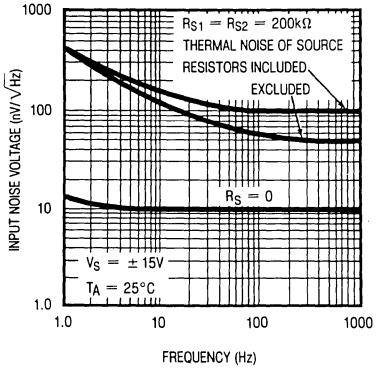
Note 3: This parameter is guaranteed by design.

TYPICAL PERFORMANCE CHARACTERISTICS

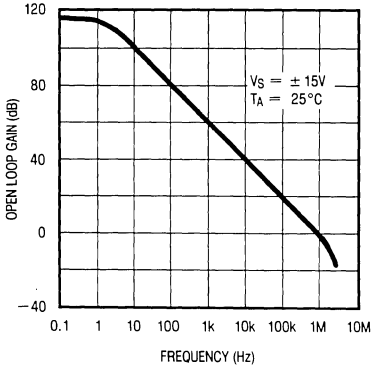
Low Frequency Noise (Closed Loop Gain = 25,000)



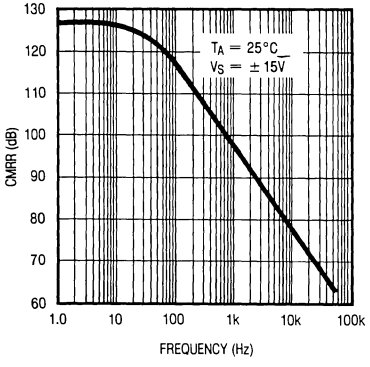
Total Input Noise Voltage vs Frequency



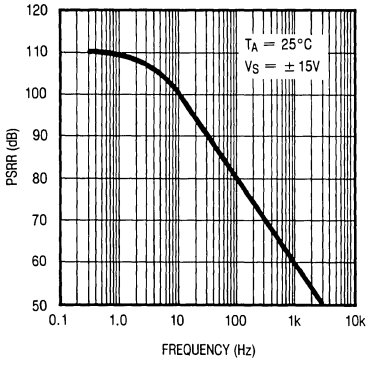
Open-Loop Frequency Response



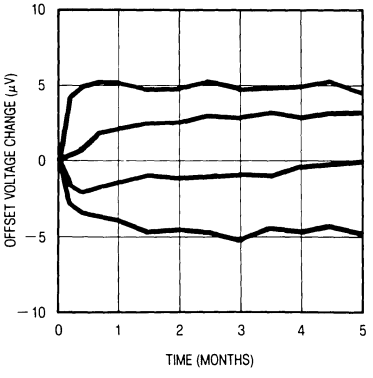
Common Mode Rejection Ratio vs Frequency



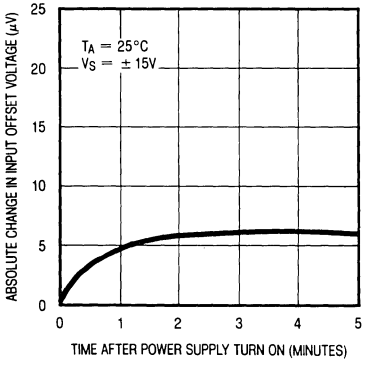
Power Supply Rejection Ratio vs Frequency



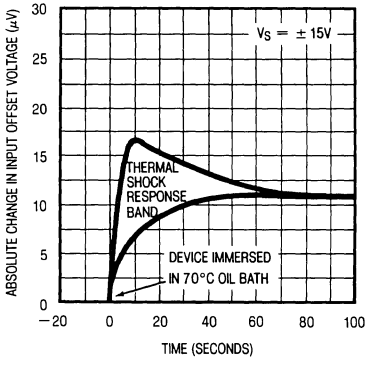
Long Term Stability of Four Representative Units



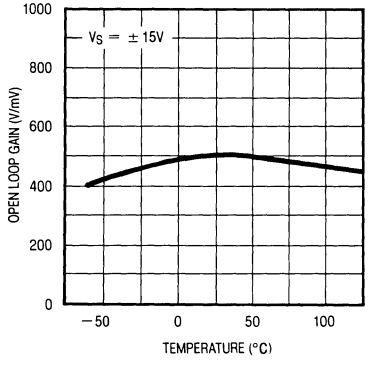
Warm-Up Drift



Offset Voltage Change Due to Thermal Shock

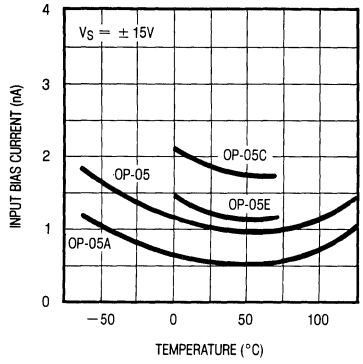


Open-Loop Gain vs Temperature

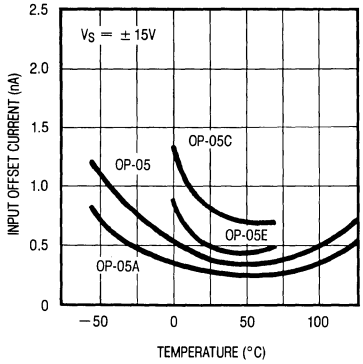


TYPICAL PERFORMANCE CHARACTERISTICS

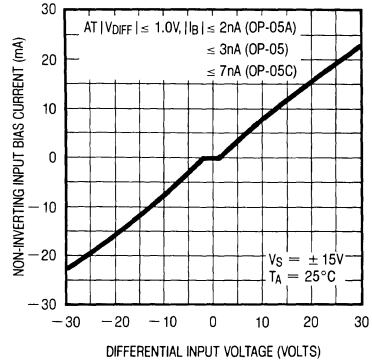
Input Bias Current vs Temperature



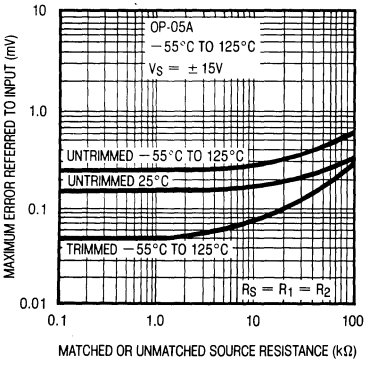
Input Offset Current vs Temperature



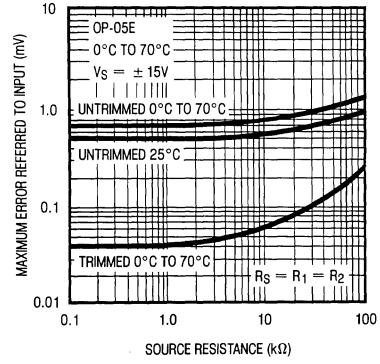
Input Bias Current vs Differential Input Voltage



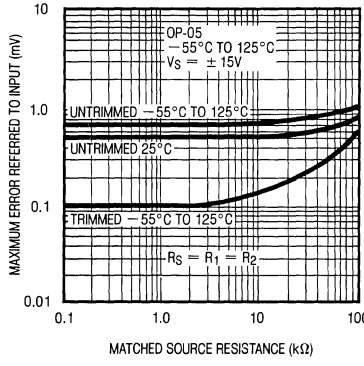
Maximum Error vs Source Resistance



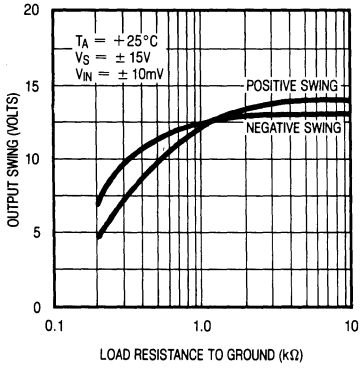
Maximum Error vs Source Resistance



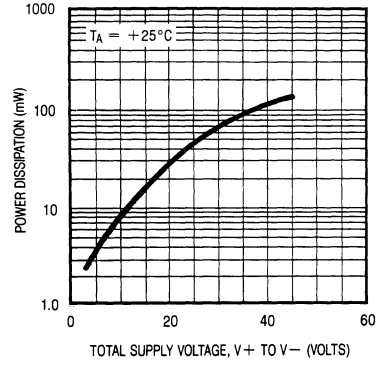
Maximum Error vs Source Resistance



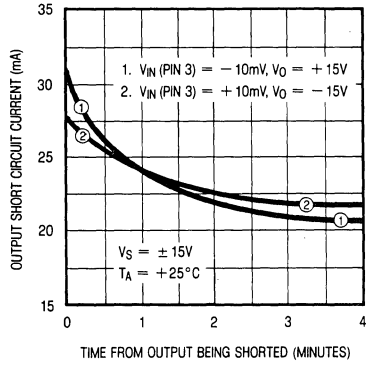
Output Voltage vs Load Resistance



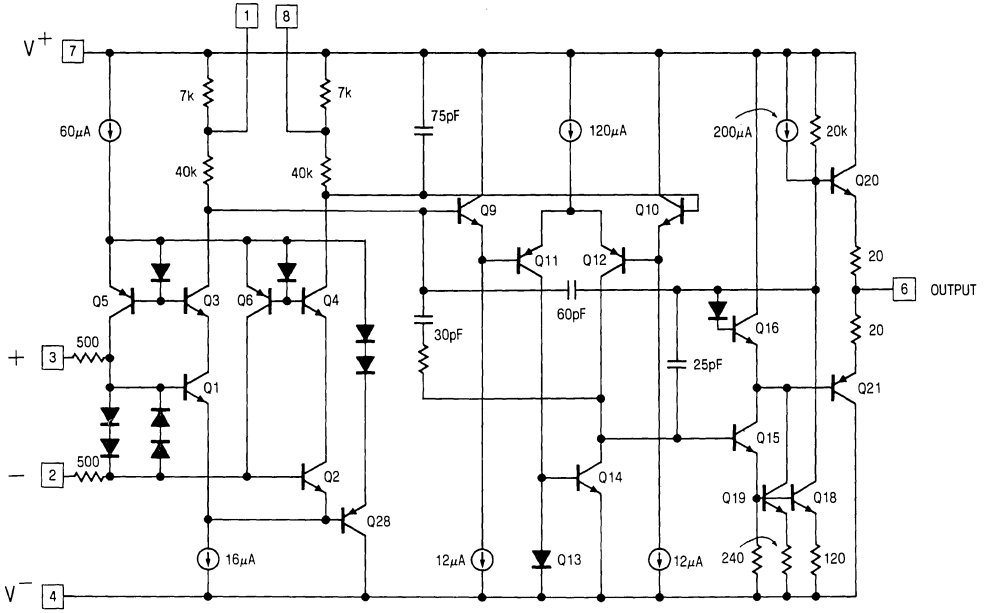
Power Consumption vs Power Supply



Output Short-Circuit Current vs Time

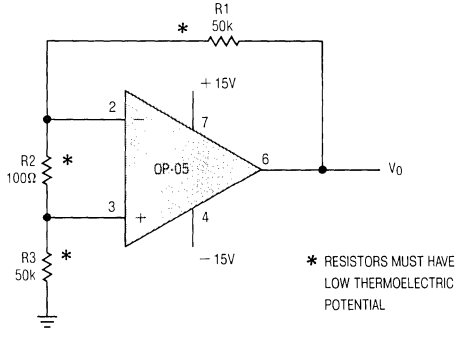


SCHEMATIC DIAGRAM



TEST CIRCUIT DIAGRAMS

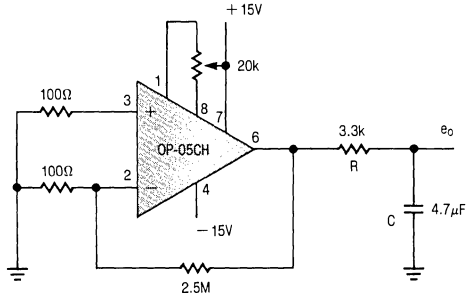
Offset Voltage Test Circuit †



$A_V = 1000$

† This circuit is also used as the burn-in configuration with supply voltages changed to ±20V, R1 = R3 = 10k, R2 = 200Ω, A_V = 100.

Offset Nulling and Low Frequency Noise Test Circuit



NOTES:

1) RC APPROXIMATELY 10Hz FILTER

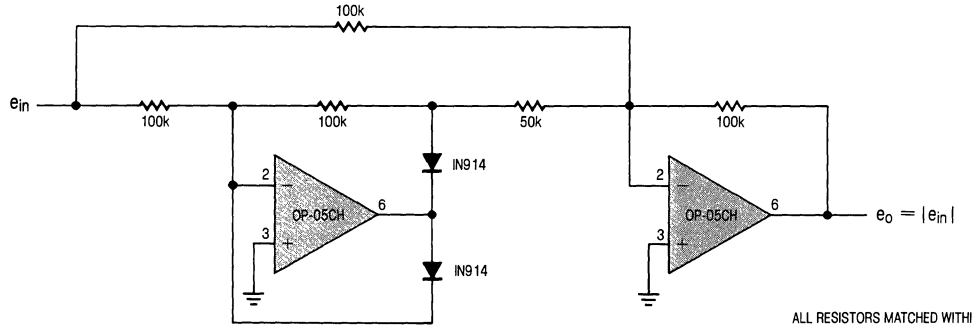
2) OBSERVE OUTPUT FOR 10 SECONDS
A_V = 25000

Application Tip

When the OP-05 is used as a replacement in 725, 108/108A, 308/308A applications, removal of external compensation is optional. For conventionally nulled 741 type applications, external trimming should be removed. Care should be taken to avoid thermocouple voltages caused by temperature variations between the input terminals or dissimilar metals.

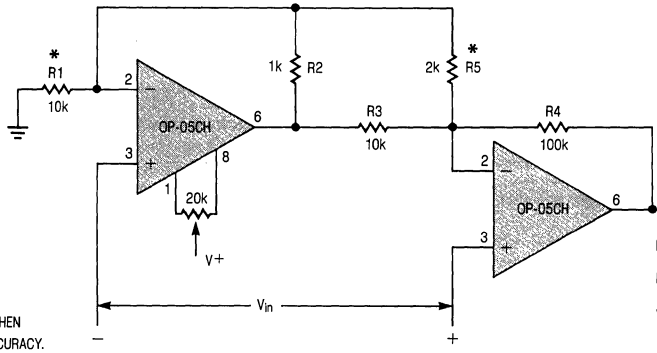
TYPICAL APPLICATIONS

Precision Absolute Value Circuit



ALL RESISTORS MATCHED WITHIN 0.1%

Two Op-Amp Instrumentation Amplifier



FOR MAXIMUM CMRR, $\frac{R2}{R1} = \frac{R3}{R4}$

FOR THIS CONDITION,

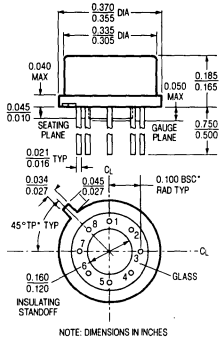
$$V_o = V_{in}\left[\frac{R4}{R3}\right]\left[1 + \frac{R2}{R1} + \frac{R2 + R3}{R5}\right]$$

$\frac{V_o}{V_{in}}$ = 210 FOR VALUES SHOWN

*ADJUST R1 FOR CMRR, THEN ADJUST R5 FOR GAIN ACCURACY. R5 DOES NOT AFFECT CMRR.

PACKAGE DESCRIPTION

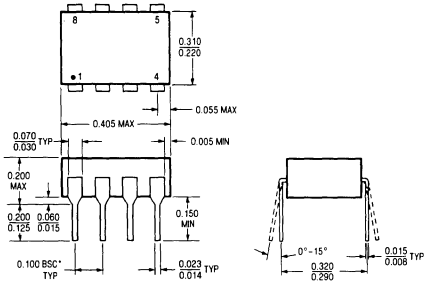
H Package
Metal Can



NOTE: DIMENSIONS IN INCHES

$T_j$max	Θ_{ja}	Θ_{jc}
150°C	150°C/W	45°C/W

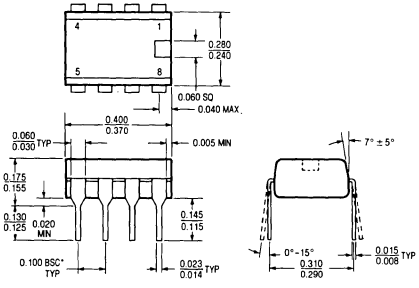
J8 Package
8 Lead Hermetic Dip



NOTE: DIMENSIONS IN INCHES UNLESS OTHERWISE NOTED.
*LEADS WITHIN 0.007 OF TRUE POSITION (TP) AT GAUGE PLANE

$T_j$max	Θ_{ja}
150°C	100°C/W

N8 Package
8 Lead Plastic



NOTE: DIMENSIONS IN INCHES UNLESS OTHERWISE NOTED.
*LEADS WITHIN 0.007 OF TRUE POSITION (TP) AT GAUGE PLANE

$T_j$max	Θ_{ja}
100°C	130°C/W

FEATURES

- *Guaranteed* 25μV *max.* Offset Voltage
- *Guaranteed* 0.6μV/°C *max.* Offset Voltage Drift with Temperature
- *Excellent* 1.0μV/Month *max.* Long Term Stability
- *Guaranteed* 0.6μV_{p-p} *max.* Noise
- *Guaranteed* 2.0nA *max.* Input Bias Current

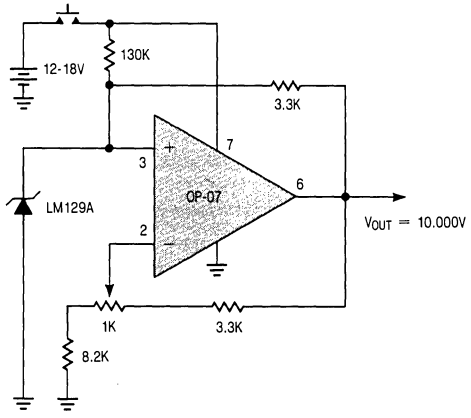
APPLICATIONS

- Thermocouple Amplifiers
- Strain Gauge Amplifiers
- Low Level Signal Processing
- Medical Instrumentation

DESCRIPTION

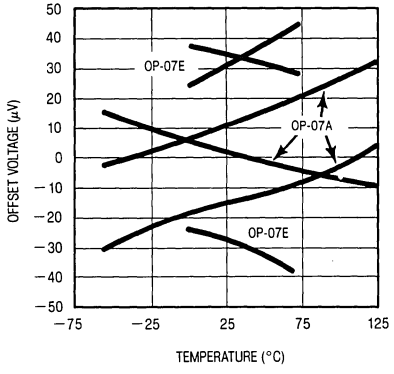
The OP-07 offers excellent performance in applications requiring low offset voltage, low drift with time and temperature and very low noise. Linear's OP-07 is interchangeable with many of the precision op-amp device types. The OP-07 also offers a wide input voltage range, high common mode rejection and low input bias current. These features result in optimum performance for small signal level and low frequency applications. Use of advanced design, processing and testing techniques make Linear's OP-07 a superior choice over similar products. A buffered reference application is shown below. For single op amp applications requiring higher performance, see the LT1001 and for matched dual precision applications see the LT1002.

Precision Buffered Single Supply Reference



The OP-07 contributes less than 5% of the total drift with temperature, noise and long term drift of the reference application.

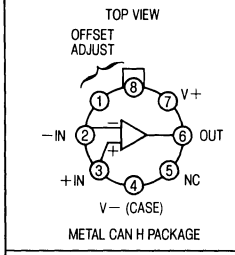
Offset Voltage Drift With Temperature Of Representative Units



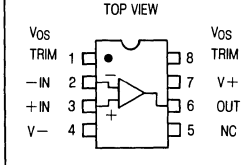
ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... ±22V
Differential Input Voltage ..... ±30V
Input Voltage Equal to Supply Voltage
Output Short Circuit Duration ..... Indefinite
Operating Temperature Range
OP-07/OP-07A ..... −55°C to 125°C
OP-07E/OP-07C ..... 0°C to 70°C
Storage Temperature Range
All Devices ..... −65°C to 150°C
Lead Temperature (Soldering, 10 sec.) ..... 300°C

PACKAGE/ORDER INFORMATION



METAL CAN H PACKAGE



HERMETIC DIP J8 PACKAGE

PLASTIC DIP N8 PACKAGE

ORDER PART NO.	OFFSET VOLTAGE (MAX)
OP-07AH	25μV
OP-07H	75μV
OP-07EH	75μV
OP-07CH	150μV
OP-07AJ8	25μV
OP-07J8	75μV
OP-07EJ8	75μV
OP-07CJ8	150μV
OP-07EN8	75μV
OP-07CN8	150μV

ELECTRICAL CHARACTERISTICS $V_S = \pm 15V$, $T_A = 25°C$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	OP-07A MIN	OP-07A TYP	OP-07A MAX	OP-07 MIN	OP-07 TYP	OP-07 MAX	UNITS
V_{OS}	Input Offset Voltage	(Note 1)		10	25		30	75	μV
$\frac{\Delta V_{OS}}{\Delta Time}$	Long Term Input Offset Voltage Stability	(Notes 2 and 3)		0.2	1.0		0.2	1.0	μV/Month
I_{OS}	Input Offset Current			0.3	2.0		0.4	2.8	nA
I_B	Input Bias Current			±0.7	±2.0		±1.0	±3.0	nA
e_n	Input Noise Voltage	0.1Hz to 10Hz (Note 2)		0.35	0.6		0.35	0.6	μV_{p-p}
	Input Noise Voltage Density	f_o = 10Hz f_o = 100Hz (Note 2) f_o = 1000Hz		10.3 10.0 9.6	18.0 13.0 11.0		10.3 10.0 9.6	18.0 13.0 11.0	$nV/\sqrt{Hz}$
i_n	Input Noise Current	0.1Hz to 10Hz (Note 2)		14	30		14	30	pA_{p-p}
	Input Noise Current Density	f_o = 10Hz f_o = 100Hz (Note 2) f_o = 1000Hz		0.32 0.14 0.12	0.80 0.23 0.17		0.32 0.14 0.12	0.80 0.23 0.17	$pA/\sqrt{Hz}$
R_{in}	Input Resistance Differential Mode	(Note 4)	30	80		20	60		MΩ
	Input Resistance Common Mode			200			200		GΩ
	Input Voltage Range		±13.5	±14.0		±13.5	±14.0		V
CMRR	Common Mode Rejection Ratio	V_{CM} = ±13V	110	126		110	126		dB
PSRR	Power Supply Rejection Ratio	V_S = ±3V to ±18V	100	108		100	108		dB
A_{VOL}	Large Signal Voltage Gain	$R_L \geq 2k\Omega$, V_O = ±10V $R_L \geq 500\Omega$, V_O = ±0.5V V_S = ±3V (Note 4)	300 150	500 400		200 150	500 400		V/mV
V_{OUT}	Maximum Output Voltage Swing	$R_L \geq 10k\Omega$ $R_L \geq 2k\Omega$ $R_L \geq 1k\Omega$	±12.5 ±12.0 ±10.5	±13.0 ±12.8 ±12.0		±12.5 ±12.0 ±10.5	±13.0 ±12.8 ±12.0		V
SR	Slew Rate	$R_L \geq 2k\Omega$ (Note 4)	0.1	0.25		0.1	0.25		V/μS
GBW	Closed Loop Bandwidth	A_{VCL} = +1 (Note 4)	0.4	0.6		0.4	0.6		MHz
Z_o	Open Loop Output Impedance	V_O = 0, I_O = 0, f = 10Hz		60			60		Ω
P_d	Power Dissipation	V_S = ±15V V_S = ±3V		75 4	120 6		75 4	120 6	mW
	Offset Adjustment Range	Null Pot = 20kΩ		±4			±4		mV

See Notes on page 2-210.

ELECTRICAL CHARACTERISTICS $V_S = \pm 15V$, $-55°C \leq T_A \leq 125°C$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		OP-07A MIN	OP-07A TYP	OP-07A MAX	OP-07 MIN	OP-07 TYP	OP-07 MAX	UNITS
V_{OS}	Input Offset Voltage	(Note 1)	●		25	60		60	200	μV
$\frac{\Delta V_{OS}}{\Delta Temp}$	Average Input Offset Voltage Drift Without External Trim With External Trim	 Null Pot = 20kΩ (Note 2)	●		0.2 0.2	0.6 0.6		0.3 0.3	1.3 1.3	μV/°C
I_{OS}	Input Offset Current		●		0.8	4.0		1.2	5.6	nA
$\frac{\Delta I_{OS}}{\Delta Temp}$	Average Input Offset Current Drift	(Note 2)	●		5	25		8	50	pA/°C
I_B	Input Bias Current		●		±1.0	±4.0		±2.0	±6.0	nA
$\frac{\Delta I_B}{\Delta Temp}$	Average Input Bias Current Drift	(Note 2)	●		8	25		13	50	pA/°C
	Input Voltage Range		●	±13.0	±13.5		±13.0	±13.5		V
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm 13V$	●	106	123		106	123		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 3V$ to $\pm 18V$	●	94	106		94	106		dB
A_{VOL}	Large Signal Voltage Gain	$R_L \geq 2k\Omega$, $V_o = \pm 10V$	●	200	400		150	400		V/mV
V_{OUT}	Output Voltage Swing	$R_L \geq 2k\Omega$	●	±12.0	±12.6		±12.0	±12.6		V

ELECTRICAL CHARACTERISTICS $V_S = \pm 15V$, $T_A = 25°C$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	OP-07E MIN	OP-07E TYP	OP-07E MAX	OP-07C MIN	OP-07C TYP	OP-07C MAX	UNITS
V_{OS}	Input Offset Voltage	(Note 1)		30	75		60	150	μV
$\frac{\Delta V_{OS}}{\Delta Time}$	Long Term Input Offset Voltage Stability	(Notes 2 and 3)		0.3	1.5		0.4	2.0	μV/Month
I_{OS}	Input Offset Current			0.5	3.8		0.8	6.0	nA
I_B	Input Bias Current			±1.2	±4.0		±1.8	±7.0	nA
e_n	Input Noise Voltage	0.1Hz to 10Hz (Note 2)		0.35	0.6		0.35	0.65	μV_{p-p}
	Input Noise Voltage Density	$f_o = 10Hz$ $f_o = 100Hz$ (Note 2) $f_o = 1000Hz$		10.3 10.0 9.6	18.0 13.0 11.0		10.5 10.2 9.8	20.0 13.5 11.5	$nV/\sqrt{Hz}$
I_n	Input Noise Current	0.1Hz to 10Hz (Note 2)		14	30		15	35	pA_{p-p}
	Input Noise Current Density	$f_o = 10Hz$ $f_o = 100Hz$ (Note 2) $f_o = 1000Hz$		0.32 0.14 0.12	0.80 0.23 0.17		0.32 0.15 0.13	0.90 0.27 0.18	$pA/\sqrt{Hz}$
R_{in}	Input Resistance Differential Mode	(Note 4)	15	50		8	33		MΩ
	Input Resistance Common Mode			160			120		GΩ
	Input Voltage Range		±13.5	±14.0		±13.0	±14.0		V
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm 13V$	106	123		100	120		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 3V$ to $\pm 18V$	94	106		90	104		dB
A_{VOL}	Large Signal Voltage Gain	$R_L \geq 2k\Omega$, $V_O = \pm 10V$ $R_L \geq 500\Omega$, $V_O = \pm 0.5V$ $V_S = \pm 3V$ (Note 4)	200 150	500 400		120 100	400 400		V/mV
V_O	Maximum Output Voltage Swing	$R_L \geq 10k\Omega$ $R_L \geq 2k\Omega$ $R_L \geq 1k\Omega$	±12.5 ±12.0 ±10.5	±13.0 ±12.8 ±12.0		±12.5 ±11.5	±13.0 ±12.8 ±12.0		V
SR	Slewing Rate	$R_L \geq 2k\Omega$ (Note 2)	0.1	0.25		0.1	0.25		V/μS
GBW	Closed Loop Bandwidth	$A_{VCL} = +1$ (Note 2)	0.4	0.6		0.4	0.6		MHz
Z_o	Open Loop Output Impedance	$V_O = 0$, $I_O = 0$, f = 10Hz		60			60		Ω
P_d	Power Dissipation	$V_S = \pm 15V$. $V_S = \pm 3V$.		75 4	120 6		80 4	150 8	mW mW
	Offset Adjustment Range	Null Pot = 20kΩ		±4			±4		mV

See Notes on page 2-210.

ELECTRICAL CHARACTERISTICS $V_S = \pm 15V$, $0°C \leq T_A \leq 70°C$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		OP-07E MIN	OP-07E TYP	OP-07E MAX	OP-07C MIN	OP-07C TYP	OP-07C MAX	UNITS
V_{OS}	Input Offset Voltage		●		45	130		85	250	μV
$\frac{\Delta V_{OS}}{\Delta Temp}$	Average Input Offset Voltage Drift Without External Trim With External Trim	 Null Pot = 20kΩ (Note 2)	●		 0.3 0.3	 1.3 1.3		 0.5 0.4	 1.8 1.6	μV/°C
I_{OS}	Input Offset Current		●		0.9	5.3		1.6	8.0	nA
$\frac{\Delta I_{OS}}{\Delta Temp}$	Average Input Offset Current Drift	(Note 2)	●		8	35		12	50	pA/°C
I_B	Input Bias Current		●		±1.5	±5.5		±2.2	±9.0	nA
$\frac{\Delta I_B}{\Delta Temp}$	Average Input Bias Current Drift	(Note 2)	●		13	35		18	50	pA/°C
	Input Voltage Range		●	±13.0	±13.5		±13.0	±13.5		V
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm 13V$	●	103	123		97	120		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 3V$ to $\pm 18V$	●	90	104		86	100		dB
A_{VOL}	Large Signal Voltage Gain	$R_L \geq 2k\Omega$, $V_o = \pm 10V$	●	180	450		100	400		V/mV
V_{OUT}	Output Voltage Swing	$R_L \geq 2k\Omega$	●	±12.0	±12.6		±11.0	±12.6		V

The ● denotes the specifications which apply over full operating temperature range.

For MIL-STD components, please refer to LTC 883C data sheet for test listing and parameters.

Note 1: Offset voltage for the OP-07A is measured 60 seconds after power is applied. All other grades are measured with high speed test equipment, approximately 1 second after power is applied.

Note 2: This parameter is tested on a sample basis only.

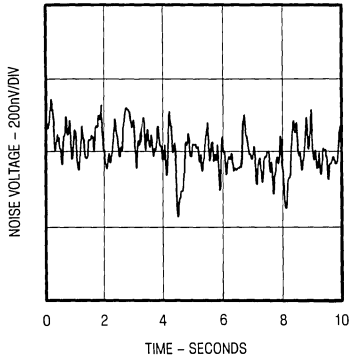
Note 3: Long term Input Offset Voltage Stability refers to the averaged trend line of V_{OS} versus Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30 operating days are typically 2.5μV.

Note 4: This parameter is guaranteed by design.

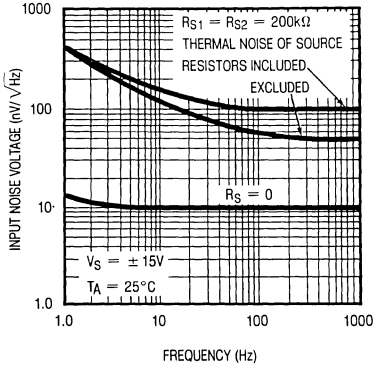
Note 5: The OP-07D is available by special request.

TYPICAL PERFORMANCE CHARACTERISTICS

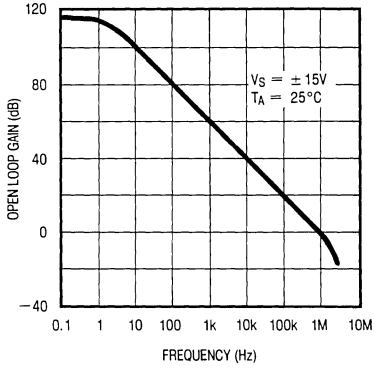
Low Frequency Noise (Closed Loop Gain = 25,000)



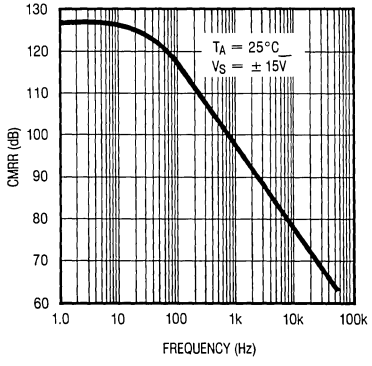
Total Input Noise Voltage vs Frequency



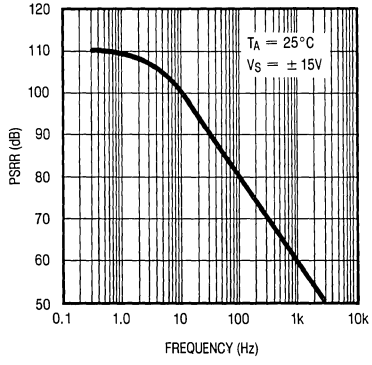
Open-Loop Frequency Response



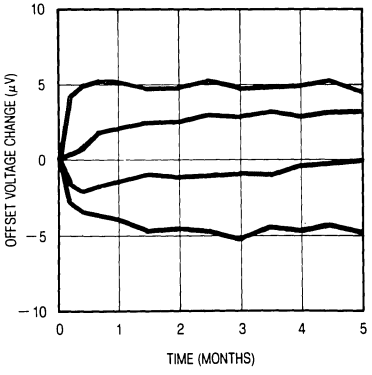
Common Mode Rejection Ratio vs Frequency



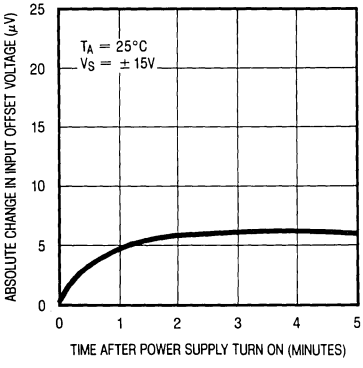
Power Supply Rejection Ratio vs Frequency



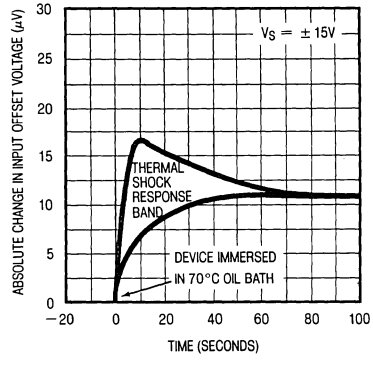
Long Term Stability of Four Representative Units



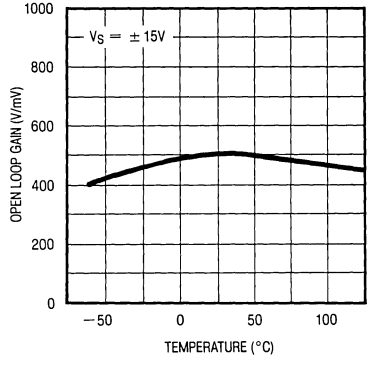
Warm-Up Drift



Offset Voltage Change Due to Thermal Shock

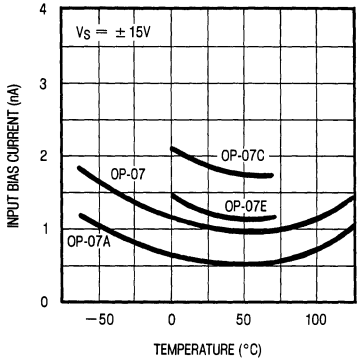


Open-Loop Gain vs Temperature

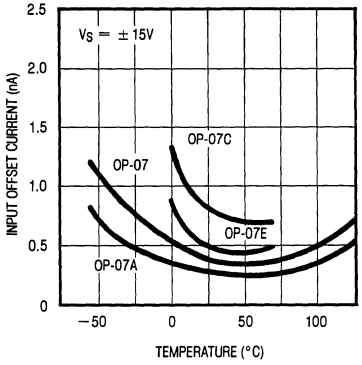


TYPICAL PERFORMANCE CHARACTERISTICS

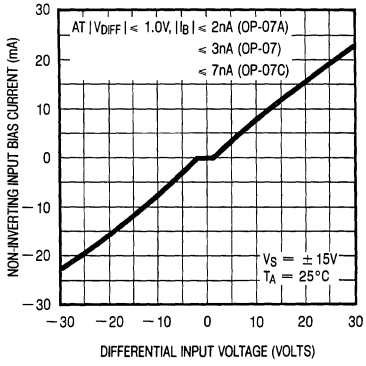
Input Bias Current vs Temperature



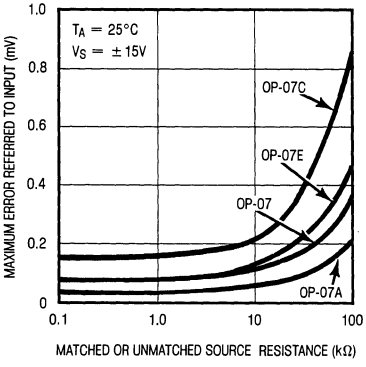
Input Offset Current vs Temperature



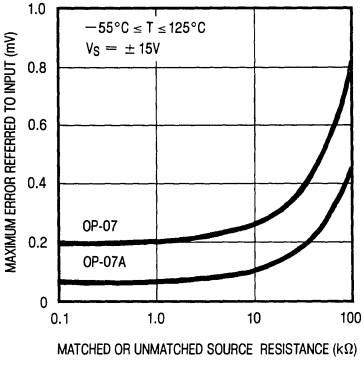
Input Bias Current vs Differential Input Voltage



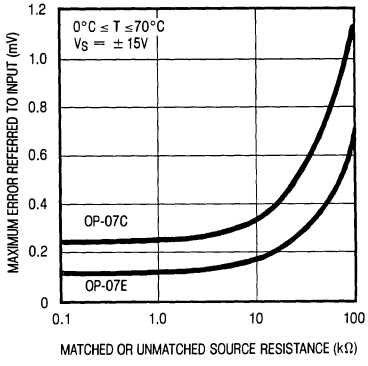
Maximum Error vs Source Resistance



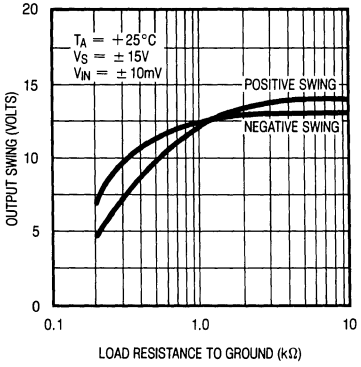
Maximum Error vs Source Resistance



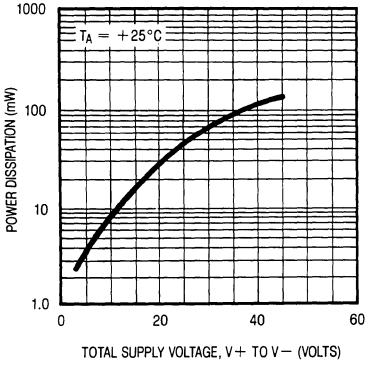
Maximum Error vs Source Resistance



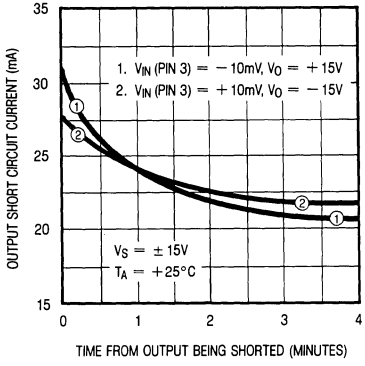
Output Voltage vs Load Resistance



Power Consumption vs Power Supply

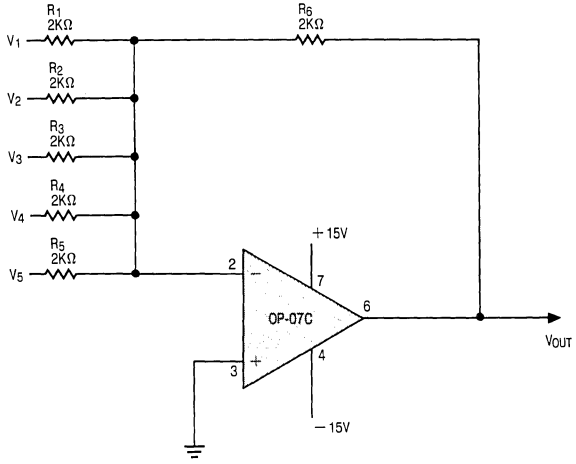


Output Short-Circuit Current vs Time

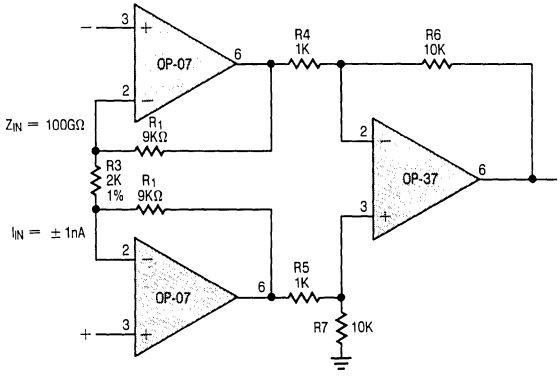


TYPICAL APPLICATIONS

Precision Summing Amplifier



Instrumentation Amplifier

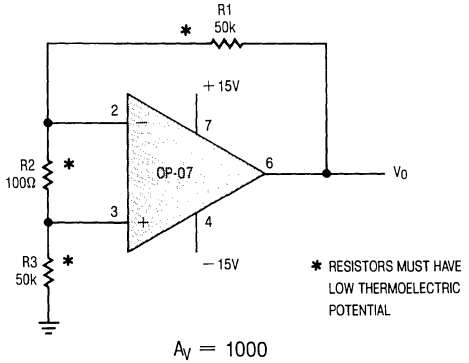


$$A_V = \frac{R6}{R4}\left(\frac{2R1}{R3} + 1\right)$$

$A_V = 100$

TEST CIRCUIT DIAGRAMS

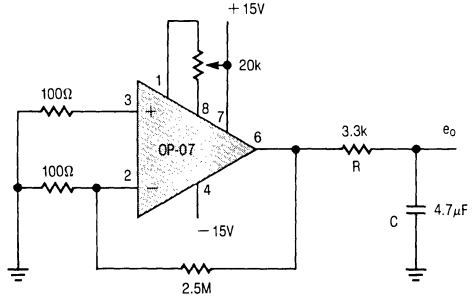
Offset Voltage Test Circuit †



$A_V = 1000$

† This circuit is also used as the burn-in configuration with supply voltages changed to ±20V, R1 = R3 = 10k, R2 = 200Ω, A_V = 100.

Offset Nulling and Low Frequency Noise Test Circuit

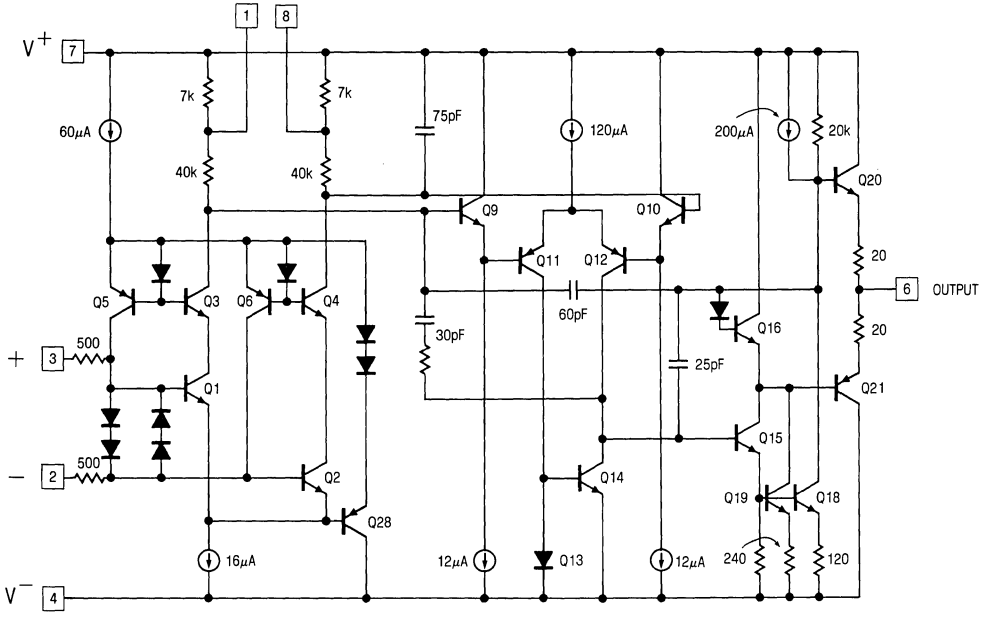


NOTES:
1) RC APPROXIMATELY 10Hz FILTER
2) OBSERVE OUTPUT FOR 10 SECONDS
A_V = 25000

Application Tip:

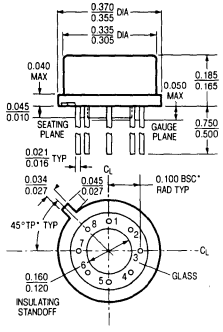
When the OP-07 is used as a replacement in 725, 108/108A, 308/308A applications, removal of external compensation is optional. For conventionally nulled 741 type applications, external trimming should be removed. Care should taken to avoid thermocouple voltages caused by temperature variations between the input terminals or dissimilar metals.

SCHEMATIC DIAGRAM



PACKAGE DESCRIPTION

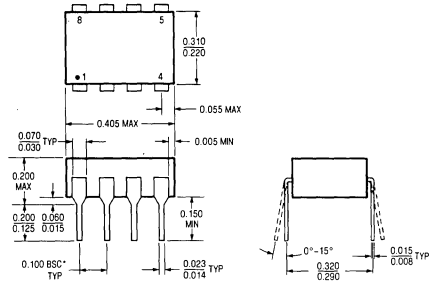
H Package
Metal Can



NOTE: DIMENSIONS IN INCHES

$T_j$max	Θ_{ja}	Θ_{jc}
150°C	150°C/W	45°C/W

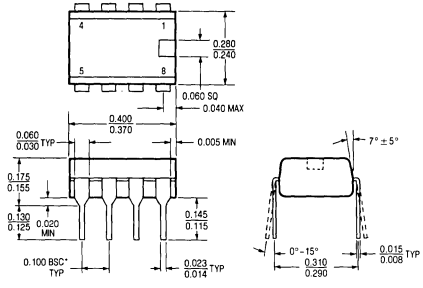
J8 Package
8 Lead Hermetic Dip



NOTE: DIMENSIONS IN INCHES UNLESS OTHERWISE NOTED.
*LEADS WITHIN 0.007 OF TRUE POSITION (TP) AT GAUGE PLANE

$T_j$max	Θ_{ja}
150°C	100°C/W

N8 Package
8 Lead Plastic



NOTE: DIMENSIONS IN INCHES UNLESS OTHERWISE NOTED.
*LEADS WITHIN 0.007 OF TRUE POSITION (TP) AT GAUGE PLANE.

$T_j$max	Θ_{ja}
100°C	130°C/W

Precision, High Speed JFET-Input Operational Amplifiers

FEATURES

- Improved Specifications Compared to LF155/156 Devices
- *Guaranteed* Low Offset Voltage 500μV Max.
- *Guaranteed* Low Offset Drift 5μV/°C Max.
- *Guaranteed* Bias Current Fully Warmed-Up over Temperature
- OP-15: LF156 Speed with LF155 Power Dissipation
  - *Guaranteed* Supply Current 4mA Max.
  - *Guaranteed* Slew Rate 10V/μs Min.
- OP-16:
  - *Guaranteed* Faster Slew Rate 18V/μs Min.
  - No High Frequency Oscillation at Cold Temperatures
- No Phase Reversal when Negative Common-Mode Limit is Exceeded

APPLICATIONS

Long Term Precision Integration
Current to Voltage Conversion
Medical Instrumentation—CAT Scanner
High Speed, Precision Sample and Hold

DESCRIPTION

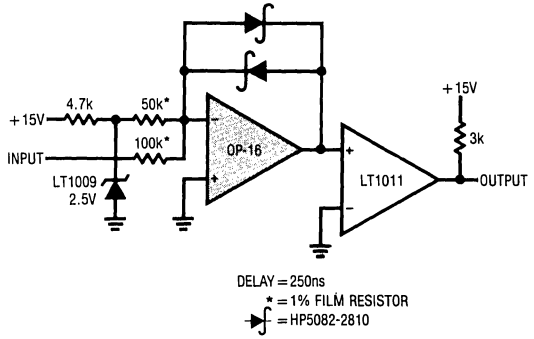
The OP-15/16 series devices feature distinct advantages over other JFET-input operational amplifiers, in particular compared to LF155/156 types.

The OP-15 has the speed of the LF156 design with the low power dissipation of the slower LF155. The OP-16 is considerably faster. Both devices offer offset voltages as low as 0.5mV, with guaranteed drift of 5μV/°C. Input bias current at 125°C is just a few nanoamperes.

Other manufacturers' OP-15/16 (and LF155/156) exhibit phase reversal at the output when the negative common-mode limit at the input is exceeded; i.e., driving from −12V to −15V with ±15V supplies. This can cause lock-up in servo systems. As shown in the application section, Linear Technology's OP-15/16 does not have this problem due to unique phase reversal protection circuitry.

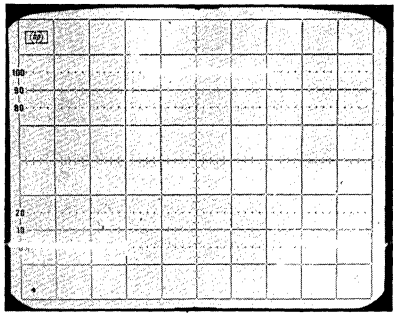
In addition, Linear's OP-16 is free from high frequency oscillation problems at cold temperatures, as is illustrated in the "Voltage Follower Small Signal Pulse Response" photo. For applications requiring higher performance, see the LT1022, LT1055 and LT1056 data sheets.

Fast, 12-Bit Current Comparator



DELAY = 250ns
* = 1% FILM RESISTOR
= HP5082-2810

Voltage Follower Small Signal Pulse Response
$T_A = -55°C$



$C_L = 100pF$
VERTICAL SCALE = 20mV/DIV
HORIZONTAL SCALE = 0.2μs/DIV

ABSOLUTE MAXIMUM RATINGS

Supply Voltage
- A, B, E, F Grades ..... ±22V
- C, G Grades ..... ±18V

Internal Power Dissipation 500mW

Operating Temperature Range
- A, B, C Grades ..... −55°C to 125°C
- E, F, G Grades ..... 0°C to 70°C

Junction Temperature ..... 150°C

Differential Input Voltage
- A, B, E, F Grades ..... ±40V
- C, G Grades ..... ±30V

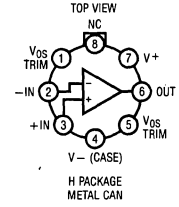
Input Voltage (Note 4)
- A, B, E, F Grades ..... ±20V
- C, G Grades ..... ±16V

Output Short Circuit Duration ..... Indefinite

Storage Temperature Range ..... −65°C to 150°C

Lead Temperature (Soldering, 10 sec.) ..... 300°C

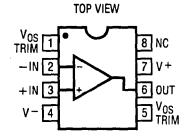
PACKAGE/ORDER INFORMATION



H PACKAGE
METAL CAN

ORDER PART NUMBER

OP-15AH	OP-16AH
OP-15BH	OP-16BH
OP-15CH	OP-16CH
OP-15EH	OP-16EH
OP-15FH	OP-16FH
OP-15GH	OP-16GH



N8 PACKAGE
8 PIN PLASTIC DIP

OP-15GN8 OP-16GN8

V_{OS} is adjusted with a potentiometer ranging from 10k to 1M. The wiper is connected to V^+

ELECTRICAL CHARACTERISTICS $V_S = \pm 15V$, $T_A = 25°C$ unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	OP-15A/E OP-16A/E MIN	OP-15A/E OP-16A/E TYP	OP-15A/E OP-16A/E MAX	OP-15B/F OP-16B/F MIN	OP-15B/F OP-16B/F TYP	OP-15B/F OP-16B/F MAX	OP-15C/G OP-16C/G MIN	OP-15C/G OP-16C/G TYP	OP-15C/G OP-16C/G MAX	UNITS
V_{OS}	Input Offset Voltage	$R_S = 50\Omega$	—	0.2	0.5	—	0.4	1.0	—	0.5	3.0	mV
I_{OS}	Input Offset Current	$T_j = 25°C$ (Note 1)	—	3	10	—	6	20	—	12	50	pA
		Warmed-Up OP-15	—	5	22	—	10	40	—	20	100	pA
		OP-16	—	5	25	—	10	50	—	20	125	pA
I_B	Input Bias Current	$T_j = 25°C$ (Note 1)	—	±15	±50	—	±30	±100	—	±60	±200	pA
		Warmed-Up OP-15	—	±18	±110	—	±40	±200	—	±80	±400	pA
		OP-16	—	±20	±130	—	±40	±250	—	±80	±500	pA
R_{IN}	Input Resistance		—	10^{12}	—	—	10^{12}	—	—	10^{12}	—	Ω
A_{VOL}	Large Signal Voltage Gain	$R_L \geq 2k\Omega$, $V_O = \pm 10V$	100	240	—	75	220	—	50	200	—	V/mV
V_O	Output Voltage Swing	$R_L = 10k\Omega$	±12	±13	—	±12	±13	—	±12	±13	—	V
		$R_L = 2k\Omega$	±11	±12.7	—	±11	±12.7	—	±11	±12.7	—	V
I_S	Supply Current	OP-15	—	2.7	4.0	—	2.7	4.0	—	2.8	5.0	mA
		OP-16	—	4.6	7.0	—	4.6	7.0	—	4.8	8.0	mA
SR	Slew Rate	$A_{VCL} = +1$ OP-15	10	13	—	7.5	11	—	5	9	—	V/μs
		OP-16	18	20	—	12	18	—	9	16	—	V/μs
GBW	Gain Bandwidth Product	(Note 3) OP-15	4.0	6.0	—	3.5	5.7	—	3.0	5.4	—	MHz
		OP-16	—	8.0	—	—	7.6	—	—	7.2	—	MHz
	Settling Time (Note 2)	to 0.01% OP-15	—	4.5	—	—	4.5	—	—	4.7	—	μs
		to 0.10%	—	1.2	—	—	1.2	—	—	1.3	—	μs
		to 0.01% OP-16	—	3.8	—	—	3.8	—	—	4.0	—	μs
		to 0.10%	—	0.9	—	—	0.9	—	—	1.0	—	μs
	Input Voltage Range		±10.5	—	—	±10.5	—	—	±10.3	—	—	V
CMRR	Common-Mode Rejection Ratio	$V_{CM} = \pm 10.5V$	86	100	—	86	100	—	—	—	—	dB
		$V_{CM} = \pm 10.3V$	—	—	—	—	—	—	82	96	—	dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 10V$ to $\pm 18V$	—	10	51	—	10	51	—	—	—	μV/V
		$V_S = \pm 10V$ to $\pm 15V$	—	—	—	—	—	—	—	10	80	μV/V
e_n	Input Noise Voltage Density	$f_O = 100Hz$	—	20	—	—	20	—	—	20	—	nV/√Hz
		$f_O = 1000Hz$	—	15	—	—	15	—	—	15	—	nV/√Hz
i_n	Input Noise Current Density	$f_O = 100Hz$	—	0.01	—	—	0.01	—	—	0.01	—	pA/√Hz
		$f_O = 1000Hz$	—	0.01	—	—	0.01	—	—	0.01	—	pA/√Hz
C_{IN}	Input Capacitance		—	3	—	—	3	—	—	3	—	pF

ELECTRICAL CHARACTERISTICS $V_S = \pm 15V$, $-55°C \le T_A \le 125°C$ unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		OP-15A OP-16A MIN	OP-15A OP-16A TYP	OP-15A OP-16A MAX	OP-15B OP-16B MIN	OP-15B OP-16B TYP	OP-15B OP-16B MAX	OP-15C OP-16C MIN	OP-15C OP-16C TYP	OP-15C OP-16C MAX	UNITS
V_{OS}	Input Offset Voltage	$R_S = 50\Omega$	●	—	0.4	0.9	—	0.7	2.0	—	0.9	4.5	mV
	Average Input Offset Voltage Drift												
TCV_{OS}	Without External Trim		●	—	2	5	—	3	10	—	4	15	μV/°C
TCV_{OSn}	With External Trim	$R_P = 100k\Omega$	●	—	2	—	—	3	—	—	4	—	μV/°C
I_{OS}	Input Offset Current	$T_j = 125°C$ (Note 1)	●	—	0.6	4.0	—	0.8	6.0	—	1.0	9.0	nA
		$T_A = 125°C$, Warmed-Up OP-15	●	—	0.8	7.0	—	1.2	11	—	1.5	17	nA
		OP-16	●	—	1.0	8.5	—	1.3	14.5	—	1.7	22	nA
I_B	Input Bias Current	$T_j = 125°C$ (Note 1)	●	—	±1.2	±5.0	—	±1.5	±7.5	—	±1.8	±10	nA
		$T_A = 125°C$, Warmed-Up OP-15	●	—	±1.7	±9.0	—	±2.2	±14	—	±2.7	±19	nA
		OP-16	●	—	±2.0	±11	—	±2.5	±18	—	±3.0	±25	nA
	Input Voltage Range		●	±10.4	—	—	±10.4	—	—	±10.25	—	—	V
CMRR	Common-Mode Rejection Ratio	$V_{CM} = \pm 10.4V$	●	85	97	—	85	97	—	—	—	—	dB
		$V_{CM} = \pm 10.25V$	●	—	—	—	—	—	—	80	93	—	dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 10V$ to $\pm 18V$	●	—	15	57	—	15	57	—	—	—	μV/V
		$V_S = \pm 10V$ to $\pm 15V$	●	—	—	—	—	—	—	—	23	100	μV/V
A_{VOL}	Large Signal Voltage Gain	$R_L \ge 2k\Omega$, $V_O = \pm 10V$	●	35	120	—	30	110	—	25	100	—	V/mV
V_O	Output Voltage Swing	$R_L \ge 10k\Omega$	●	±12	±13	—	±12	±13	—	±12	±13	—	V

ELECTRICAL CHARACTERISTICS $V_S = \pm 15V$, $0°C \le T_A \le 70°C$ unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		OP-15E OP-16E MIN	OP-15E OP-16E TYP	OP-15E OP-16E MAX	OP-15F OP-16F MIN	OP-15F OP-16F TYP	OP-15F OP-16F MAX	OP-15G OP-16G MIN	OP-15G OP-16G TYP	OP-15G OP-16G MAX	UNITS
V_{OS}	Input Offset Voltage	$R_S = 50\Omega$	●	—	0.3	0.75	—	0.55	1.5	—	0.7	3.8	mV
	Average Input Offset Voltage Drift												
TCV_{OS}	Without External Trim		●	—	2	5	—	3	10	—	4	15	μV/°C
TCV_{OSn}	With External Trim	$R_P = 100k\Omega$	●	—	2	—	—	3	—	—	4	—	μV/°C
I_{OS}	Input Offset Current	$T_j = 70°C$ (Note 1)	●	—	0.04	0.30	—	0.06	0.45	—	0.08	0.65	nA
		$T_A = 70°C$, Warmed-Up OP-15	●	—	0.06	0.55	—	0.08	0.80	—	0.10	1.2	nA
		OP-16	●	—	0.07	0.70	—	0.10	1.1	—	0.15	1.7	nA
I_B	Input Bias Current	$T_j = 70°C$ (Note 1)	●	—	±0.10	±0.40	—	±0.12	±0.60	—	±0.14	±0.80	nA
		$T_A = 70°C$, Warmed-Up OP-15	●	—	±0.13	±0.75	—	±0.16	±1.1	—	±0.19	±1.5	nA
		OP-16	●	—	±0.15	±0.90	—	±0.20	±1.4	—	±0.25	±2.0	nA
	Input Voltage Range		●	±10.4	—	—	±10.4	—	—	±10.25	—	—	V
CMRR	Common-Mode Rejection Ratio	$V_{CM} = \pm 10.4V$	●	85	98	—	85	98	—	—	—	—	dB
		$V_{CM} = \pm 10.25V$	●	—	—	—	—	—	—	80	94	—	dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 10V$ to $\pm 18V$	●	—	13	57	—	13	57	—	—	—	μV/V
		$V_S = \pm 10V$ to $\pm 15V$	●	—	—	—	—	—	—	—	20	100	μV/V
A_{VO}	Large Signal Voltage Gain	$R_L \ge 2k\Omega$, $V_O = \pm 10V$	●	65	200	—	50	180	—	35	160	—	V/mV
V_O	Output Voltage Swing	$R_L \ge 10k\Omega$	●	±12	±13	—	±12	±13	—	±12	±13	—	V

The ● denotes the specifications which apply over full operating temperature range.

For MIL-STD components, please refer to LTC 883C data sheet for test listing and parameters.

Note 1: Input bias current is specified for two different conditions. The T_j specification is with the junction at ambient temperature; the warmed-up specification is with the device operating in a warmed-up condition at the ambient temperature specified. I_B and I_{OS} are measured at $V_{CM} = 0$.

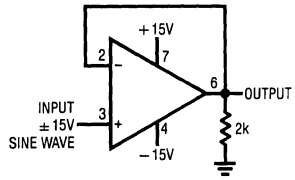
Note 2: Settling time is defined here for a unity gain inverter connection using 2kΩ resistors. It is the time required for the error voltage (the voltage at the inverting input pin on the amplifier) to settle to within a specified percentage of its final value from the time a 10V step input is applied to the inverter.

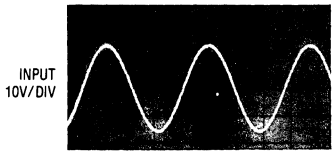
Note 3: Sample tested.

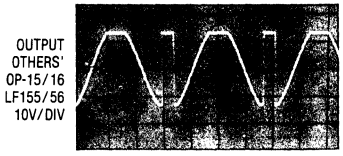
Note 4: Unless otherwise specified, the absolute maximum negative input voltage is equal to the negative power supply voltage.

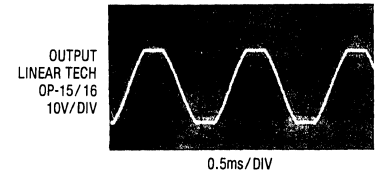
APPLICATIONS

Voltage Follower with Input Exceeding the Negative Common-Mode Range



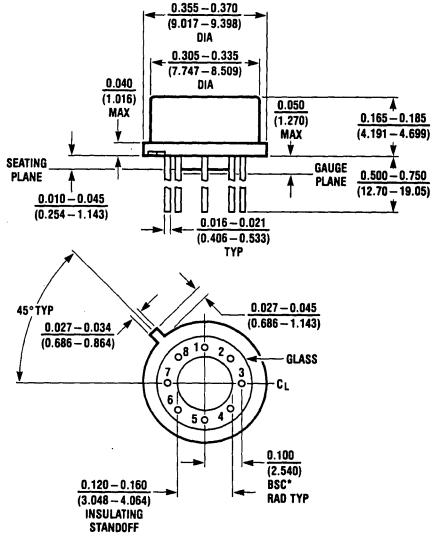






PACKAGE DESCRIPTION

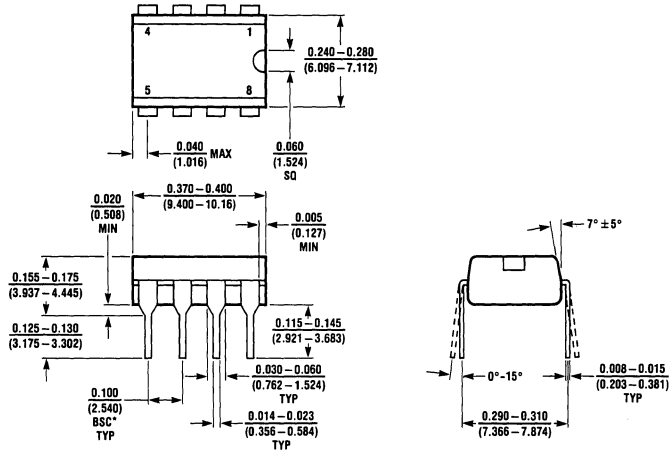
H Package
Metal Can



NOTE: DIMENSIONS IN INCHES

T_{jmax}	θ_{ja}	θ_{jc}
150°C	150°C/W	45°C/W

N8 Package
8 Lead Plastic



NOTE: DIMENSIONS IN INCHES UNLESS OTHERWISE NOTED
*LEADS WITHIN 0.007 OF TRUE POSITION (TP) AT GAUGE PLANE

T_{jmax}	θ_{ja}
100°C	130°C/W

Low Noise, High Speed Precision Operational Amplifiers

FEATURES

- *Guaranteed* 3.8nV/$\sqrt{Hz}$ *max* 1kHz Noise
- *Guaranteed* 5.5nV/$\sqrt{Hz}$ *max* 10Hz Noise
- Very Low Peak-to-Peak Noise, 80nV Typical
- *Guaranteed* 25μV *max* Offset Voltage
- *Guaranteed* 0.6μV/°C *max* Drift with Temperature
- *Guaranteed* 11V/μsec *min* Slew Rate (OP-37)
- *Guaranteed* 1 Million *min* Voltage Gain

APPLICATIONS

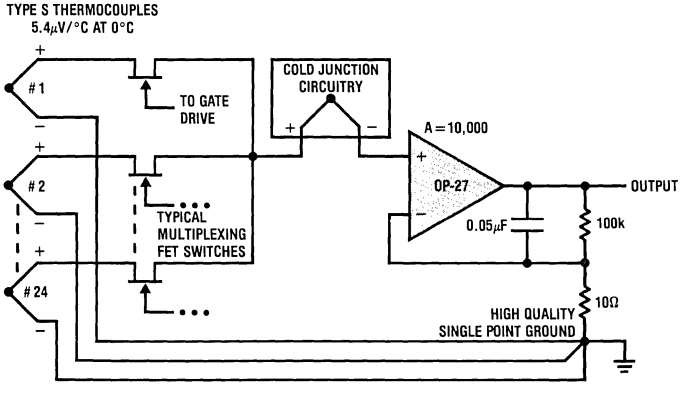
- Low Level Transducer Amplifiers
- Precision Threshold Detectors
- Tape Head Preamplifiers
- Microphone Preamplifiers
- Direct Coupled Audio Gain Stages

DESCRIPTION

The OP-27/OP-37 series of operational amplifiers combine outstanding noise performance with excellent precision and high speed specifications. The wideband noise is only 3nV/$\sqrt{Hz}$, and with the 1/f noise corner at 2.7Hz, low noise is maintained for all low frequency instrumentation applications. Precision DC specifications match or exceed the best available op amps: offset voltage is 10μV, drift with temperature and time are 0.2μV/°C and 0.2μV/month, respectively; common mode rejection is 126dB, voltage gain is two million. The unity gain compensated OP-27 is an order of magnitude faster than other precision op amps. The decompensated OP-37 is even faster at a gain-bandwidth product of 63MHz and 17V/μsec slew rate. These characteristics plus Linear Technology's advanced process and test techniques make the OP-27/37 an excellent choice for performance and reliability in all low noise, precision amplifier applications. In addition, Linear's OP-37 is completely latch-up free in high gain, large capacitive feedback configurations. The accurate, microvolt, low noise signal handling capabilities of the OP-27/37 are taken advantage of in the multiplexed thermocouple application shown.

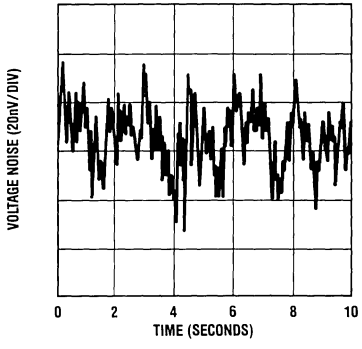
For applications requiring higher performance, see the LT1007 and LT1037 data sheets.

Low Noise, Multiplexed Thermocouple Amplifier



If 24 channels are multiplexed per second, and the output is required to settle to 0.1% accuracy, the amplifier's bandwidth cannot be limited to less than 30Hz. Yet the noise contribution of the OP-27 will still be only 0.11μVp-p, which is equivalent to an error of only 0.02°C.

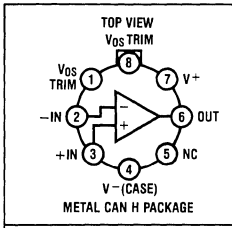
0.1Hz to 10Hz Noise



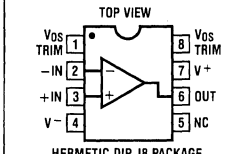
ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... ±22V
Internal Power Dissipation 500mW
Input Voltage ..... Equal to Supply Voltage
Output Short Circuit Duration ..... Indefinite
Differential Input Current (Note 8) ..... ±25mA
Lead Temperature (Soldering, 10 sec.) ..... 300°C
Operating Temperature Range
OP-27/OP-37 A, C ..... −55°C to 125°C
OP-27/OP-37 E, G ..... −25°C to 85°C
Junction Temperature Range
OP-27/OP-37 A, C ..... −55°C to 150°C
OP-27/OP-37 E, G ..... −25°C to 125°C
Storage Temperature Range
OP-27/OP-37 A, C, E, G −65°C to 150°C

PACKAGE/ORDER INFORMATION



METAL CAN H PACKAGE



HERMETIC DIP J8 PACKAGE
PLASTIC DIP N8 PACKAGE

ORDER PART NUMBER	
OP-27AH	OP-37AH
OP-27CH	OP-37CH
OP-27EH	OP-37EH
OP-27GH	OP-37GH
OP-27AJ8	OP-37EJ8
OP-27CJ8	OP-37GJ8
OP-27EJ8	OP-27EN8
OP-27GJ8	OP-27GN8
OP-37AJ8	OP-37EN8
OP-37CJ8	OP-37GN8

ELECTRICAL CHARACTERISTICS $V_S = \pm 15V$, $T_A = 25°C$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	OP-27A,E/OP-37A,E MIN	TYP	MAX	OP-27C,G/OP-37C,G MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	(Note 1)		10	25		30	100	μV
$\frac{\Delta V_{OS}}{\Delta Time}$	Long Term Offset Voltage Stability	(Note 2)		0.2	1.0		0.4	2.0	μV/Mo
I_{OS}	Input Offset Current			7	35		12	75	nA
I_B	Input Bias Current			±10	±40		±15	±80	nA
e_n	Input Noise Voltage	0.1Hz to 10Hz (Notes 3 and 5)		0.08	0.18		0.09	0.25	μVp-p
	Input Noise Voltage Density	f_o = 10Hz (Note 3)		3.5	5.5		3.8	8.0	nV/√Hz
		f_o = 30Hz (Note 3)		3.1	4.5		3.3	5.6	nV/√Hz
		f_o = 1000Hz (Note 3)		3.0	3.8		3.2	4.5	nV/√Hz
i_n	Input Noise Current Density	f_o = 10Hz (Notes 3 and 6)		1.7	4.0		1.7		pA/√Hz
		f_o = 30Hz (Notes 3 and 6)		1.0	2.3		1.0		pA/√Hz
		f_o = 1000Hz (Notes 3 and 6)		0.4	0.6		0.4	0.6	pA/√Hz
	Input Resistance—Common Mode			3			2		GΩ
	Input Voltage Range		±11.0	±12.3		±11.0	±12.3		V
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm 11V$	114	126		100	120		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 4V$ to $\pm 18V$	100	120		94	118		dB
A_{VOL}	Large Signal Voltage Gain	$R_L \geq 2k\Omega$, $V_O = \pm 10V$	1000	1800		700	1500		V/mV
		$R_L \geq 1k\Omega$, $V_O = \pm 10V$	800	1500			1500		V/mV
		$R_L = 600\Omega$, $V_O = \pm 1V$	250	700		200	500		V/mV
		$V_S = \pm 4V$ (Note 4)							
V_{OUT}	Maximum Output Voltage Swing	$R_L \geq 2k\Omega$	±12.0	±13.8		±11.5	±13.5		V
		$R_L \geq 600\Omega$	±10.0	±11.5		±10.0	±11.5		V
SR	Slew Rate OP-27	$R_L \geq 2k\Omega$ (Note 4)	1.7	2.8		1.7	2.8		V/μs
	OP-37	$A_{VCL} \geq 5$ (Note 4)	11	17		11	17		V/μs
GBW	Gain-Bandwidth OP-27	f_o = 100kHz (Note 4)	5.0	8.0		5.0	8.0		MHz
	Product OP-37	f_o = 10kHz (Note 4)	45	63		45	63		MHz
		f_o = 1MHz ($A_{VCL} \geq 5$)		40			40		MHz
Z_O	Open Loop Output Resistance	$V_O = 0$, $I_O = 0$		70			70		Ω
P_d	Power Dissipation			90	140		100	170	mW

ELECTRICAL CHARACTERISTICS $V_S = \pm 15V$, $-55°C \leq T_A \leq 125°C$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		OP-27A/OP-37A MIN	OP-27A/OP-37A TYP	OP-27A/OP-37A MAX	OP-27C/OP-37C MIN	OP-27C/OP-37C TYP	OP-27C/OP-37C MAX	UNITS
V_{OS}	Input Offset Voltage	(Note 1)	●		30	60		70	300	μV
$\frac{\Delta V_{OS}}{\Delta Temp}$	Average Input Offset Drift	(Note 7)	●		0.2	0.6		0.4	1.8	μV/°C
I_{OS}	Input Offset Current		●		15	50		30	135	nA
I_B	Input Bias Current		●		±20	±60		±35	±150	nA
	Input Voltage Range		●	±10.3	±11.5		±10.2	±11.5		V
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm 10V$	●	108	122		94	116		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 4.5V$ to $\pm 18V$	●	96	116		86	110		dB
A_{VOL}	Large Signal Voltage Gain	$R_L \geq 2k\Omega$, $V_O = \pm 10V$	●	600	1200		300	800		V/mV
V_{OUT}	Maximum Output Voltage Swing	$R_L \geq 2k\Omega$	●	±11.5	±13.5		±10.5	±13.0		V

ELECTRICAL CHARACTERISTICS $V_S = \pm 15V$, $-25°C \leq T_A \leq 85°C$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		OP-27E/OP-37E MIN	OP-27E/OP-37E TYP	OP-27E/OP-37E MAX	OP-27G/OP-37G MIN	OP-27G/OP-37G TYP	OP-27G/OP-37G MAX	UNITS
V_{OS}	Input Offset Voltage	(Note 1)	●		20	50		55	220	μV
$\frac{\Delta V_{OS}}{\Delta Temp}$	Average Input Offset Drift	(Note 7)	●		0.2	0.6		0.4	1.8	μV/°C
I_{OS}	Input Offset Current		●		10	50		20	135	nA
I_B	Input Bias Current		●		±14	±60		±25	±150	nA
	Input Voltage Range		●	±10.5	±11.8		±10.5	±11.8		V
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm 10V$	●	110	124		96	118		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 4.5V$ to $\pm 18V$	●	97	118		90	114		dB
A_{VOL}	Large Signal Voltage Gain	$R_L \geq 2k\Omega$, $V_O = \pm 10V$	●	750	1500		450	1000		V/mV
V_{OUT}	Maximum Output Voltage Swing	$R_L \geq 2k\Omega$	●	±11.7	±13.6		±11.0	±13.3		V

The ● denotes the specifications which apply over full operating temperature range.

Note 1: Input Offset Voltage measurements are performed by automatic test equipment approximately 0.5 seconds after application of power. A and E grades are guaranteed fully warmed up.

Note 2: Long Term Input Offset Voltage Stability refers to the average trend line of Offset Voltage vs Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30 days are typically 2.5μV—refer to typical performance curve.

Note 3: Sample tested. Contact factory for 100% testing of 10Hz voltage noise.

Note 4: Parameter is guaranteed by design and is not tested.

Note 5: See test circuit and frequency response curve for 0.1Hz to 10Hz tester in Applications Information section.

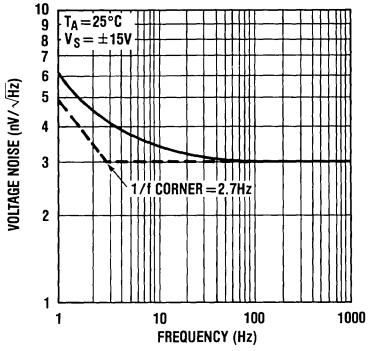
Note 6: See test circuit for current noise measurement in Applications Information section.

Note 7: The Average Input Offset Drift performance is within the specifications unnulled or when nulled with a pot having a range of 8kΩ to 20kΩ.

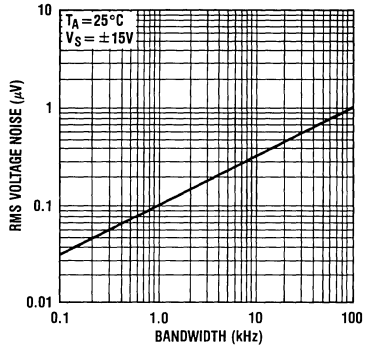
Note 8: The OP-27/37's inputs are protected by back-to-back diodes. Current limiting resistors are not used in order to achieve low noise. If differential input voltage exceeds ±0.7V, the input current should be limited to 25mA.

TYPICAL PERFORMANCE CHARACTERISTICS

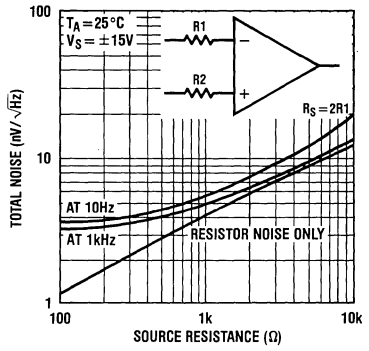
Voltage Noise vs Frequency



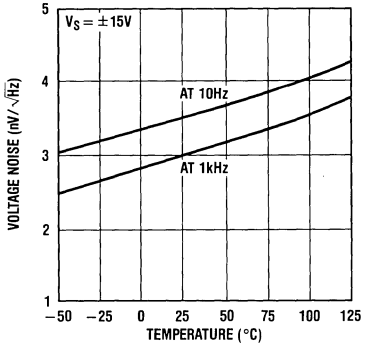
Input Wideband Voltage Noise vs Bandwidth (0.1Hz to Frequency Indicated)



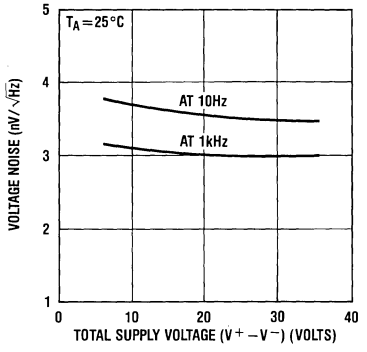
Total Noise vs Source Resistance



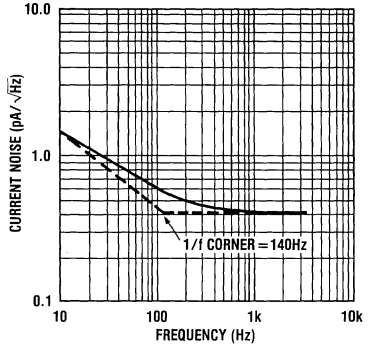
Voltage Noise vs Temperature



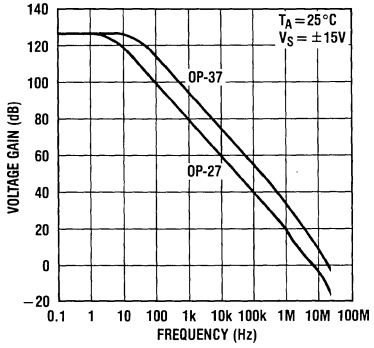
Voltage Noise vs Supply Voltage



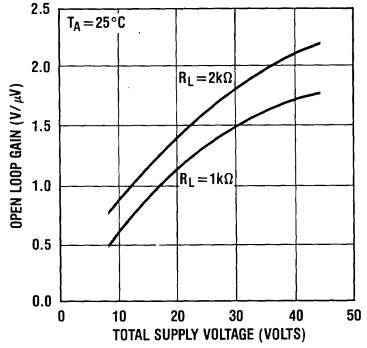
Current Noise vs Frequency



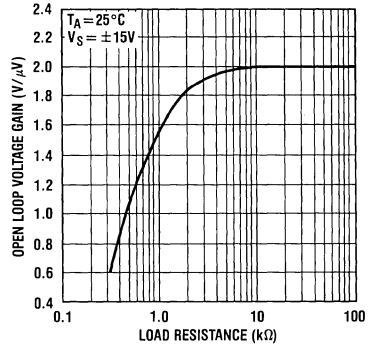
Voltage Gain vs Frequency



Open Loop Voltage Gain vs Supply Voltage

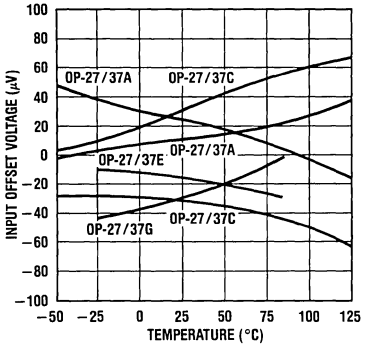


Open Loop Voltage Gain vs Load Resistance

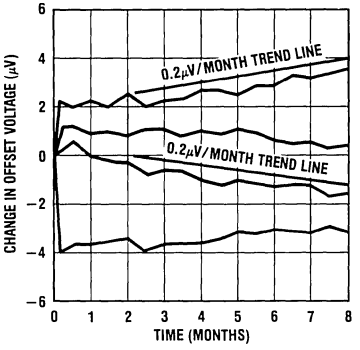


TYPICAL PERFORMANCE CHARACTERISTICS

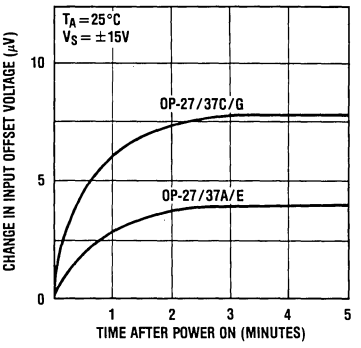
Offset Voltage Drift of Representative Units



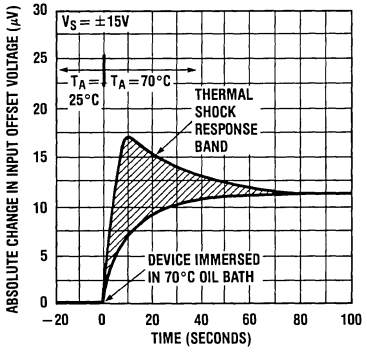
Long Term Drift of Representative Units



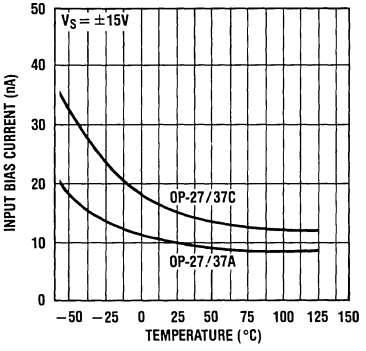
Warm-Up Drift



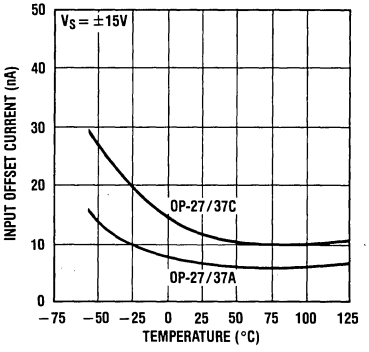
Offset Voltage Change Due to Thermal Shock



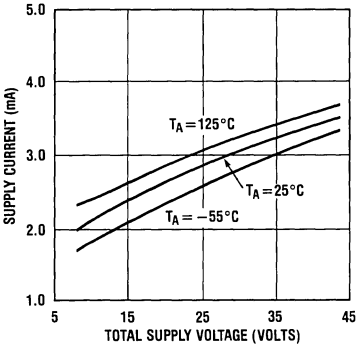
Input Bias Current vs Temperature



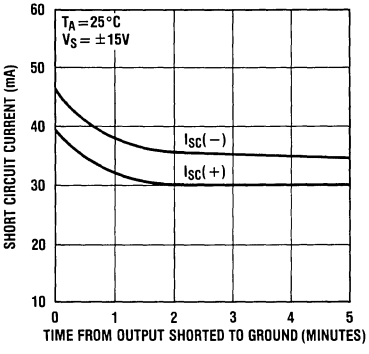
Input Offset Current vs Temperature



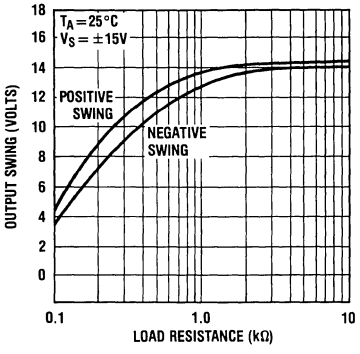
Supply Current vs Supply Voltage



Short Circuit Current vs Time

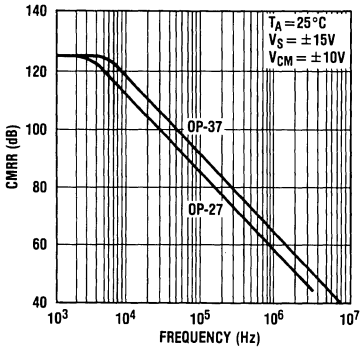


Maximum Output Swing vs Resistive Load

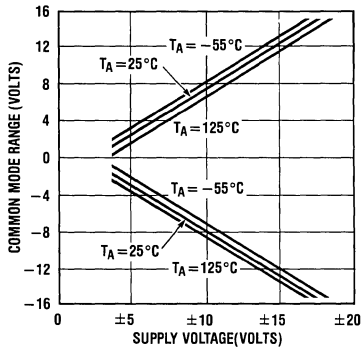


TYPICAL PERFORMANCE CHARACTERISTICS

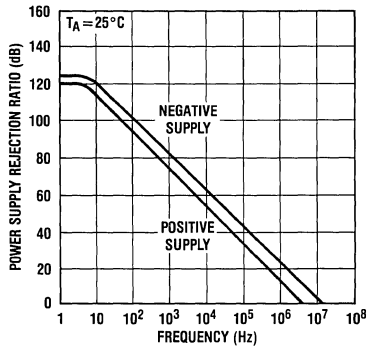
Common Mode Rejection vs Frequency



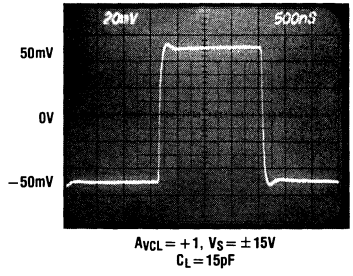
Common Mode Input Range vs Supply Voltage



PSRR vs Frequency

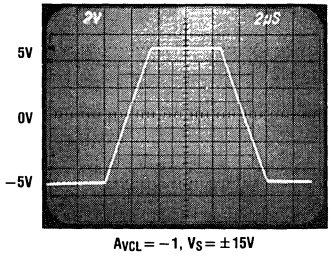


OP-27 Small Signal Transient Response



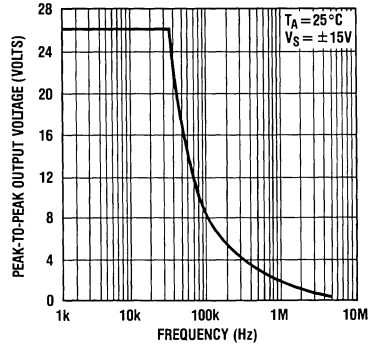
$A_{VCL} = +1$, $V_S = \pm 15V$
$C_L = 15pF$

OP-27 Large Signal Transient Response

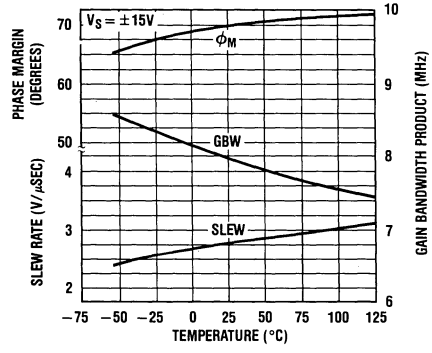


$A_{VCL} = -1$, $V_S = \pm 15V$

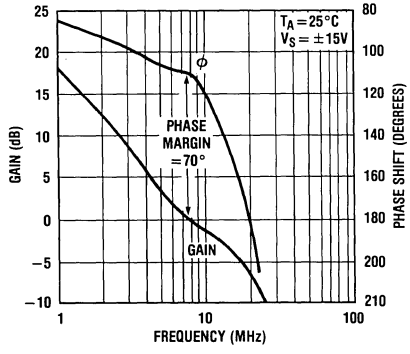
OP-27 Maximum Undistorted Output vs Frequency



OP-27 Slew Rate, Gain Bandwidth Product, Phase Margin vs Temperature

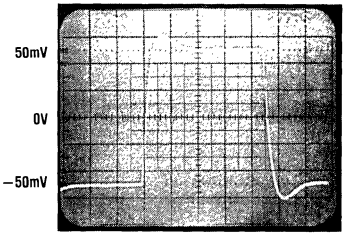


OP-27 Gain, Phase Shift vs Frequency



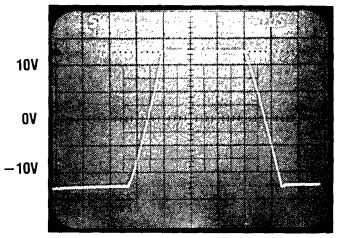
TYPICAL PERFORMANCE CHARACTERISTICS

OP-37 Small Signal Transient Response



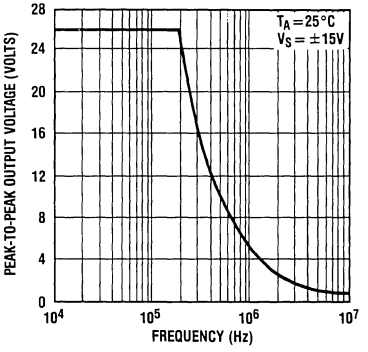
$A_{VCL} = +5$, $V_S = \pm 15V$
$C_L = 15pF$

OP-37 Large Signal Response

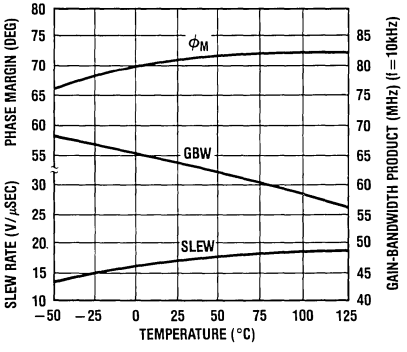


$A_{VCL} = +5$, $V_S = \pm 15V$

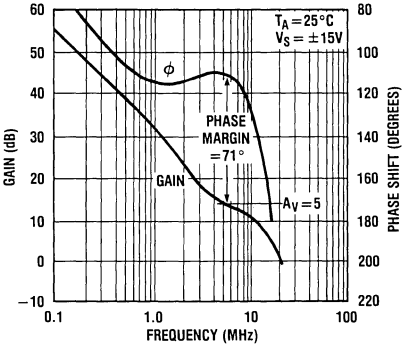
OP-37 Maximum Undistorted Output vs Frequency



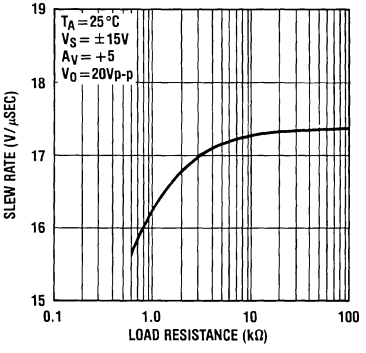
OP-37 Slew Rate, Gain Bandwidth Product, Phase Margin vs Temperature



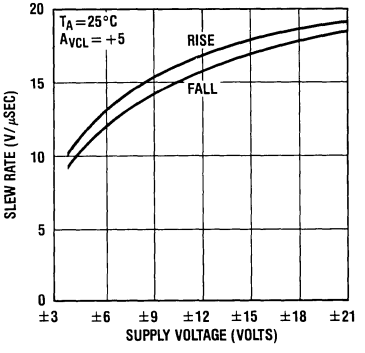
OP-37 Gain, Phase Shift vs Frequency



OP-37 Slew Rate vs Load



OP-37 Slew Rate vs Supply Voltage



APPLICATIONS INFORMATION

General

The OP-27/37 series devices may be inserted directly into OP-07, OP-05, 725, and 5534 sockets with or without removal of external compensation or nulling components. In addition, the OP-27/37 may be fitted to 741 sockets with the removal or modification of external nulling components.

Noise Testing

The 0.1Hz to 10Hz peak-to-peak noise of the OP-27/OP-37 is measured in the test circuit shown. The frequency response of this noise tester indicates that the 0.1Hz corner is defined by only one zero. The test time to measure 0.1Hz to 10Hz noise should not exceed 10 seconds, as this time limit acts as an additional zero to eliminate noise contributions from the frequency band below 0.1Hz.

Measuring the typical 80nV peak-to-peak noise performance of the OP-27/37 requires special test precautions:

(a) The device should be warmed up for at least five minutes. As the op amp warms up, its offset voltage changes typically 4μV due to its chip temperature increasing 10°C to 20°C from the moment the power supplies are turned on. In the 10 second measurement interval these temperature-induced effects can easily exceed tens of nanovolts.

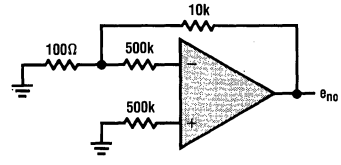
(b) For similar reasons, the device must be well shielded from air currents to eliminate the possibility of thermoelectric effects in excess of a few nanovolts, which would invalidate the measurements.

(c) Sudden motion in the vicinity of the device can also "feedthrough" to increase the observed noise.

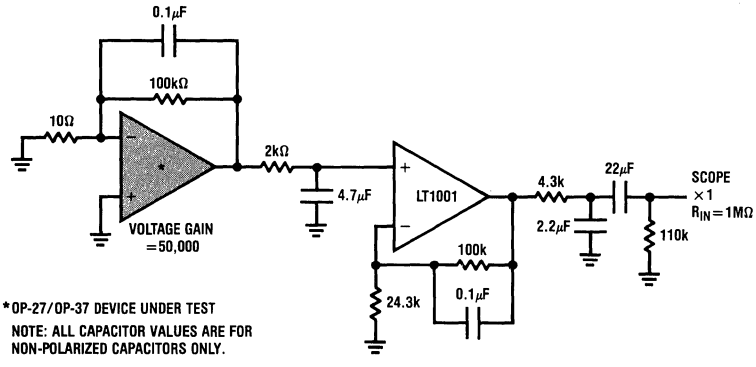
A noise-voltage density test is recommended when measuring noise on a large number of units. A 10Hz noise-voltage density measurement will correlate well with a 0.1Hz to 10Hz peak-to-peak noise reading since both results are determined by the white noise and the location of the 1/f corner frequency.

Current noise is measured and calculated by the following formula:

$$i_n = \frac{[e^2_{no} - (130nV)^2]^{1/2}}{1M\Omega \times 100}$$



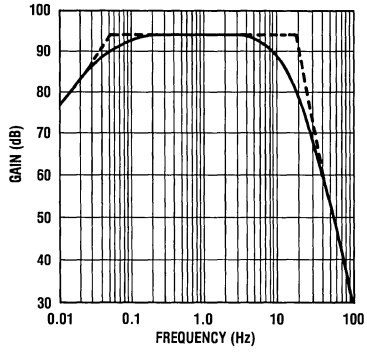
0.1Hz to 10Hz Noise Test Circuit



*OP-27/OP-37 DEVICE UNDER TEST

NOTE: ALL CAPACITOR VALUES ARE FOR NON-POLARIZED CAPACITORS ONLY.

0.1Hz to 10Hz p-p Noise Tester Frequency Response

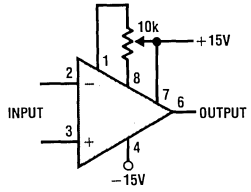


APPLICATIONS INFORMATION

Offset Voltage Adjustment

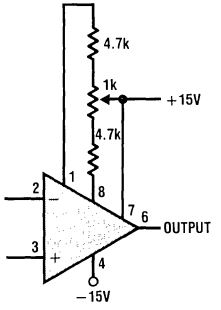
The input offset voltage of the OP-27/37, and its drift with temperature, are permanently trimmed at wafer testing to a low level. However, if further adjustment of V_{OS} is necessary, the use of a 10k nulling potentiometer will not degrade drift with temperature. Trimming to a value other than zero creates a drift of (V_{OS}/300) μV/°C, e.g., if V_{OS} is adjusted to 300μV, the change in drift will be 1μV/°C.

Standard Adjustment



The adjustment range with a 10k pot is approximately ±2.5mV. If less adjustment range is needed, the sensitivity and resolution of the nulling can be improved by using a smaller pot in conjunction with fixed resistors. The example has an approximate null range of ±200μV.

Improved Sensitivity Adjustment

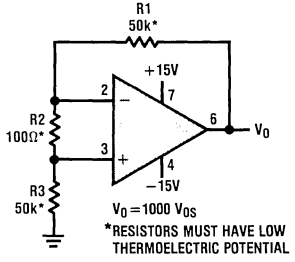


Offset Voltage and Drift

Thermocouple effects, caused by temperature gradients across dissimilar metals at the contacts to the input terminals, can exceed the inherent drift of the amplifier unless proper care is exercised. Air currents should be minimized, package leads should be short, the two input leads should be close together and maintained at the same temperature.

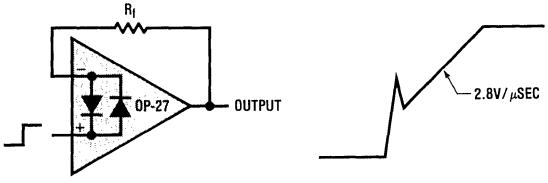
The circuit shown to measure offset voltage is also used as the burn-in configuration for the OP-27/37, with the supply voltages increased to ±20V, R1=R3=10k, R2=200Ω, A_V=100.

Test Circuit for Offset Voltage and Offset Voltage Drift with Temperature



Unity Gain Buffer Applications (OP-27 Only)

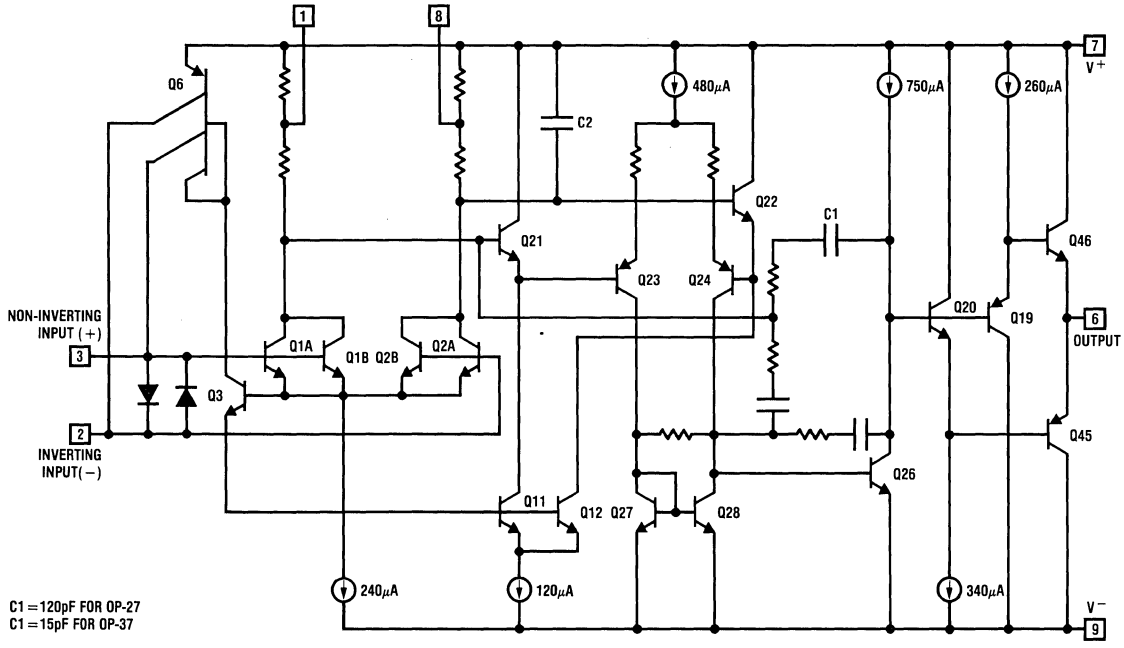
When $R_f \leq 100\Omega$ and the input is driven with a fast, large signal pulse (>1V), the output waveform will look as shown in the pulsed operation diagram.



During the fast feedthrough-like portion of the output, the input protection diodes effectively short the output to the input and a current, limited only by the output short circuit protection, will be drawn by the signal generator. With $R_f \geq 500\Omega$, the output is capable of handling the current requirements ($I_L \leq 20$mA at 10V) and the amplifier stays in its active mode and a smooth transition will occur.

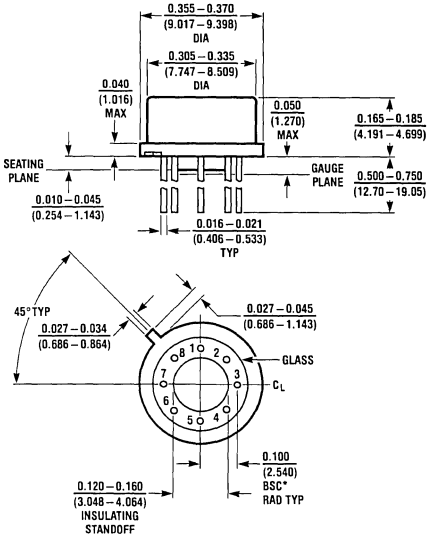
As with all operational amplifiers when $R_f > 2k\Omega$, a pole will be created with R_f and the amplifier's input capacitance, creating additional phase shift and reducing the phase margin. A small capacitor (20pF to 50pF) in parallel with R_f will eliminate this problem.

SCHEMATIC DIAGRAM



PACKAGE DESCRIPTION

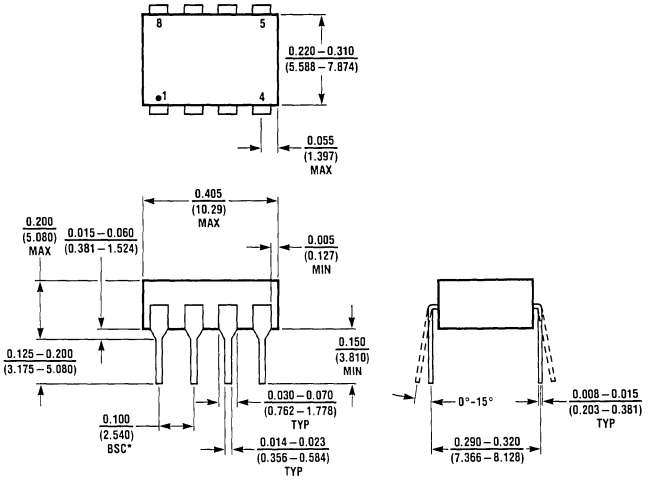
H Package
Metal Can



NOTE: DIMENSIONS IN INCHES (MILLIMETERS)

$T_j$max	θ_{ja}	θ_{jc}
150°C	150°C/W	45°C/W

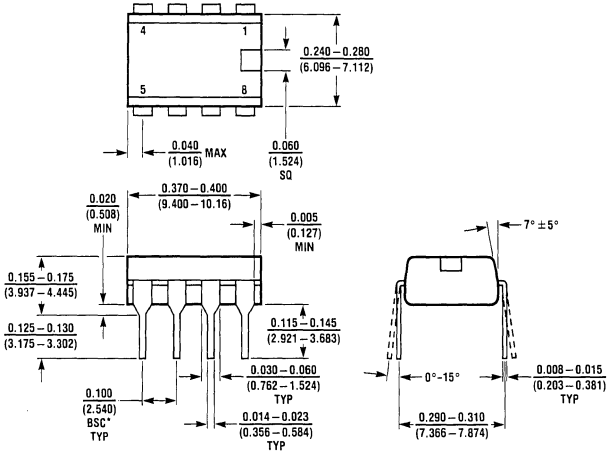
J8 Package
8 Lead Hermetic DIP



NOTE: DIMENSIONS IN INCHES (MILLIMETERS) UNLESS OTHERWISE NOTED
*LEADS WITHIN 0.007 OF TRUE POSITION (TP) AT GAUGE PLANE

$T_j$max	θ_{ja}
150°C	100°C/W

N8 Package
8 Lead Plastic



NOTE: DIMENSIONS IN INCHES UNLESS OTHERWISE NOTED
*LEADS WITHIN 0.007 OF TRUE POSITION (TP) AT GAUGE PLANE

$T_j$max	θ_{ja}
100°C	130°C/W

Dual Matched Low Noise Precision Op Amp and Dual High Speed Low Noise Precision Op Amp

FEATURES

- *Guaranteed* 80μV Max. V_{OS}
- *Guaranteed* 6.0nV/$\sqrt{Hz}$ 10Hz Voltage Noise Density
- *Guaranteed* 3.9nV/$\sqrt{Hz}$ 1kHz Voltage Noise Density
- *Guaranteed* 1μV/°C Max. V_{OS} Drift
- *Guaranteed* 1 Million Min. Voltage Gain
- *Guaranteed* Matching Characteristics
- *Guaranteed* 10V/μs Min. Slew Rate (OP-237)

APPLICATIONS

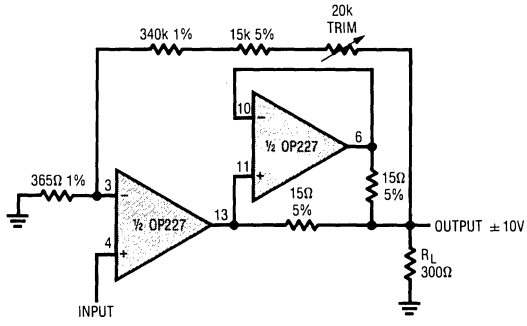
- Instrumentation Amplifiers
- Low Level Signal Processing
- Low Noise Audio Amplifiers
- Strain Gauge Amplifiers

DESCRIPTION

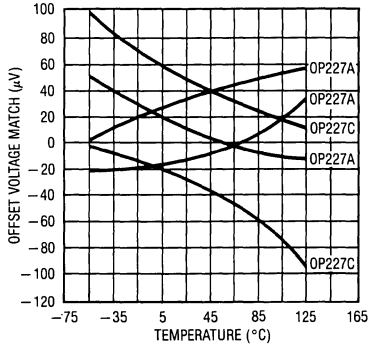
The OP-227 is a dual matched precision op amp which combines low offset, low noise, and high gain with excellent matching characteristics. Typical individual amplifier specifications of 20μV V_{OS}, 0.2μV/°C drift, 10nA I_B and 2.8nV/$\sqrt{Hz}$ 10Hz noise voltage density make the OP-227 an impressive performer in terms of single amplifiers. Matching characteristics are specified with guaranteed limits on all critical parameters including V_{OS}, V_{OS} drift, I_{BIAS} and CMRR (see the Features section), which make the OP-227 an ideal choice for two and three op amp instrumentation amplifier applications.

The OP-237 offers DC specifications identical to the OP-227 and is decompensated for higher speed operation at inverting gains greater than 5.

Precision Amplifier Drives 300Ω Load to ±10V with 0.05% Accuracy



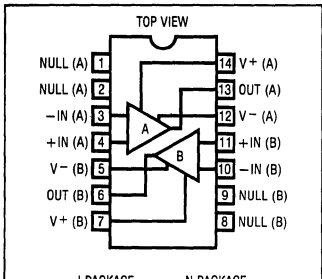
Matching Characteristic; Drift of Offset Voltage Match of Representative Units



ABSOLUTE MAXIMUM RATINGS

Supply Voltage (Note 9) . . . . . ±22V
Internal Power Dissipation 500mW
Input Voltage . . . . . Equal to Supply Voltage
Output Short-Circuit Duration . . . . . Indefinite
Differential Input Current (Note 8) . . . . . ±25mA
Storage Temperature Range . . . . . −65°C to +150°C
Operating Temperature
OP-227A/237A/227C/237C . . −55°C to +125°C
OP-227E/237E/227G/237G . . . −25°C to +85°C
Lead Temperature Range (Soldering, 10 sec.) . . 300°C

PACKAGE/ORDER INFORMATION



J PACKAGE 14 PIN HERMETIC
N PACKAGE 14 PIN PLASTIC

NOTE: DEVICE MAY BE OPERATED EVEN IF INSERTION IS REVERSED; THIS IS DUE TO INHERENT SYMMETRY OF PIN LOCATIONS OF AMPLIFIERS A AND B (NOTE 9).

ORDER PART NUMBER
OP-227AJ OP-237AJ
OP-227CJ OP-237CJ
OP-227EJ OP-237EJ
OP-227GJ OP-237GJ
OP-227EN OP-237EN
OP-227GN OP-237GN

ELECTRICAL CHARACTERISTICS Individual Amplifiers

$V_S = \pm 15V$, $T_A = 25°C$, unless otherwise noted

SYMBOL	PARAMETER	CONDITIONS	OP-227A, E OP-237A, E			OP-227C, G OP-237C, G			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{OS}	Input Offset Voltage	(Note 1)	—	20	80	—	60	180	μV
$\frac{\Delta V_{OS}}{\Delta Time}$	Long Term V_{OS} Stability	(Notes 2, 3)	—	0.2	1.0	—	0.2	2.0	μV/Mo
I_{OS}	Input Offset Current		—	7	35	—	12	75	nA
I_B	Input Bias Current		—	±10	±40	—	±15	±80	nA
e_{np-p}	Input Noise Voltage	0.1Hz to 10Hz (Notes 3, 5)	—	0.06	0.20	—	0.06	0.28	μVp-p
e_n	Input Noise Voltage Density	f_O = 10Hz (Note 3)	—	2.8	6.0	—	2.8	9.0	nV/√Hz
		f_O = 30Hz (Note 3)	—	2.6	4.7	—	2.6	5.9	nV/√Hz
		f_O = 1000Hz (Note 3)	—	2.5	3.9	—	2.5	4.6	nV/√Hz
i_n	Input Noise Current Density	f_O = 10Hz (Notes 3, 6)	—	1.5	4.5	—	1.5	—	pA/√Hz
		f_O = 30Hz (Notes 3, 6)	—	1.0	2.5	—	1.0	—	pA/√Hz
		f_O = 1000Hz (Notes 3, 6)	—	0.4	0.7	—	0.4	0.7	pA/√Hz
	Input Resistance—Common Mode		—	7	—	—	5	—	GΩ
	Input Voltage Range		±11.0	±12.5	—	±11.0	±12.5	—	V
CMRR	Common Mode Rejection Ratio	V_{CM} = ±11V	114	126	—	100	126	—	dB
PSRR	Power Supply Rejection Ratio	V_S = ±4V to ±18V	—	1	10	—	2	20	μV/V
A_{VOL}	Large-Signal Voltage Gain	$R_L \geq 2k\Omega$, V_O = ±12V	3	20	—	2	20	—	V/μV
		$R_L \geq 600\Omega$, V_O = ±10V	1	12	—	0.8	12	—	V/μV
V_{OUT}	Output Voltage Swing	$R_L \geq 2k\Omega$	±12.0	±13.8	—	±11.5	±13.5	—	V
		$R_L \geq 600\Omega$	±10.0	±12.5	—	±10.0	±12.5	—	V
SR	Slew Rate OP-227	$R_L \geq 2k\Omega$	1.7	2.8	—	1.7	2.8	—	V/μs
	OP-237	$A_{VCL} \geq 5$	10	15	—	10	15	—	V/μs
GBW	Gain Bandwidth Prod. OP-227	f_O = 100kHz (Note 4)	5	8	—	5	8	—	MHz
	OP-237	f_O = 10kHz (Note 4)	35	63	—	35	63	—	MHz
	OP-237	f_O = 1MHz ($A_{VCL} \geq 5$)	—	40	—	—	40	—	MHz
Z_O	Open-Loop Output Resistance	V_O = 0, I_O = 0	—	70	—	—	70	—	Ω
P_d	Power Consumption	Each Amplifier	—	80	140	—	90	170	mW
	Offset Adjustment Range	R_P = 10kΩ	—	±4	—	—	±4	—	mV

ELECTRICAL CHARACTERISTICS Individual Amplifiers

$V_S = \pm 15V$, $-25°C \le T_A \le 85°C$, unless otherwise noted

SYMBOL	PARAMETER	CONDITIONS		OP-227E OP-237E			OP-227G OP-237G			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{OS}	Input Offset Voltage	(Note 1)	●	—	40	140	—	85	280	μV
$\frac{\Delta V_{OS}}{\Delta Temp}$	Average Input Offset Drift	(Note 7)	●	—	0.2	1.0	—	0.3	1.8	μV/°C
I_{OS}	Input Offset Current		●	—	15	50	—	20	135	nA
I_B	Input Bias Current		●	—	±20	±60	—	±35	±150	nA
	Input Voltage Range		●	±10.5	±11.5	—	±10.5	±11.5	—	V
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm 10V$	●	110	124	—	96	118	—	dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 4.5V$ to $\pm 18V$	●	—	2	15	—	2	32	μV/V
A_{VOL}	Large Signal Voltage Gain	$R_L \ge 2k\Omega$, $V_O = \pm 10V$	●	1	14	—	0.8	14	—	V/μV
V_{OUT}	Output Voltage Swing	$R_L \ge 2k\Omega$	●	±11.7	±13.6	—	±11.0	±13.3	—	V

ELECTRICAL CHARACTERISTICS Individual Amplifiers

$V_S = \pm 15V$, $-55°C \le T_A \le 125°C$, unless otherwise noted

SYMBOL	PARAMETER	CONDITIONS		OP-227A OP-237A			OP-227C OP-237C			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{OS}	Input Offset Voltage	(Note 1)	●	—	60	180	—	110	350	μV
$\frac{\Delta V_{OS}}{\Delta Temp}$	Average Input Offset Drift	(Note 7)	●	—	0.2	1.0	—	0.3	1.8	μV/°C
I_{OS}	Input Offset Current		●	—	15	50	—	30	135	nA
I_B	Input Bias Current		●	—	±20	±60	—	±35	±150	nA
	Input Voltage Range		●	±10.5	±11.8	—	±10.2	±11.8	—	V
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm 10V$	●	108	122	—	94	116	—	dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 4.5V$ to $\pm 18V$	●	—	2	16	—	4	51	μV/V
A_{VOL}	Large Signal Voltage Gain	$R_L \ge 2k\Omega$, $V_O = \pm 10V$	●	1	14	—	0.8	14	—	V
V_{OUT}	Output Voltage Swing	$R_L \ge 2k\Omega$	●	±11.5	±13.5	—	±10.5	±13.0	—	V

The ● denotes the specifications which apply over the full operating temperature range.

For MIL-STD components, please refer to LTC 883C data sheet for test listing and parameters.

Note 1: Input offset voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power.

Note 2: Long-Term Input Offset Voltage Stability refers to the average trend line of V_{OS} vs Time over extended periods after the first 30 days of operation.

Note 3: Sample tested.

Note 4: Parameter is guaranteed by design.

Note 5: See test circuit and frequency response curve for 0.1Hz to 10Hz tester.

Note 6: See test circuit for current noise measurement.

Note 7: The input offset drift performance is within the specifications unnulled or when nulled with $R_P = 8k\Omega$ to $20k\Omega$.

Note 8: The inputs are protected by back-to-back diodes. Current limiting resistors are not used in order to achieve low noise. If differential input voltage exceeds ±0.7V, the input current should be limited to 25mA.

Note 9: The V^+ supply terminals are completely independent and may be powered by separate supplies if desired (this approach, however, would sacrifice the advantages of the power supply rejection ratio matching). The V^- supply terminals are both connected to the common substrate and must be tied to the same voltage. *Both* V^- pins should be used.

MATCHING CHARACTERISTICS See notes on page 2-233.

at $V_S = \pm 15V$, $T_A = 25°C$, unless otherwise noted

SYMBOL	PARAMETER	CONDITIONS	OP-227A, E, OP-237A, E			OP-227C, G, OP-237C, G			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
ΔV_{OS}	Input Offset Voltage Match		—	25	80	—	55	300	μV
I_B^+	Average Non-Inverting Bias Current		—	±10	±40	—	±15	±90	nA
I_{OS}^+	Non-Inverting Offset Current		—	±12	±60	—	±20	±130	nA
I_{OS}^-	Inverting Offset Current		—	±12	±60	—	±20	±130	nA
ΔCMRR	Common Mode Rejection Ratio Match	$V_{CM} = \pm 11V$	110	123	—	97	117	—	dB
ΔPSRR	Power Supply Rejection Ratio Match	$V_S = \pm 4V$ to $\pm 18V$	—	2	10	—	2	20	μV/V
	Channel Separation	(Note 4)	126	154	—	126	154	—	dB
ΔA_{VOL}	Gain Match	$f_O = 100kHz$ (Note 4) $R_L \geq 2k\Omega$, $V_O = \pm 10V$	—	1.5	6.0	—	2.0	9.0	%

at $V_S = \pm 15V$, $-55°C \leq T_A \leq 125°C$, unless otherwise noted

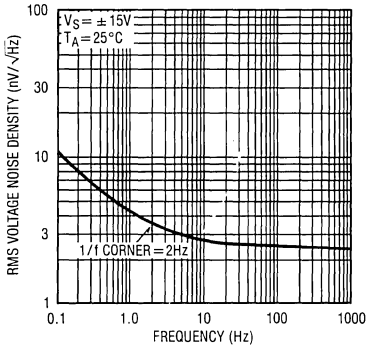
SYMBOL	PARAMETER	CONDITIONS		OP-227A, OP-237A			OP-227C, OP-237C			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	
ΔV_{OS}	Input Offset Voltage Match		●	—	55	180	—	100	480	μV
$\frac{\Delta V_{OS}}{\Delta Temp}$	Input Offset Voltage Tracking	(Note 7)	●	—	0.3	1.0	—	0.5	1.8	μV/°C
I_B^+	Average Non-Inverting Bias Current		●	—	±20	±60	—	±35	±170	nA
$\frac{\Delta I_B^+}{\Delta Temp}$	Average Drift of Non-Inverting Bias Current		●	—	100	—	—	200	—	pA/°C
I_{OS}^+	Non-Inverting Offset Current		●	—	±25	±90	—	±45	±250	nA
$\frac{I_{OS}^+}{\Delta Temp}$	Average Drift of Non-Inverting Offset Current		●	—	130	—	—	250	—	pA/°C
I_{OS}^-	Inverting Offset Current		●	—	±25	±90	—	±45	±250	nA
ΔCMRR	Common Mode Rejection Ratio Match	$V_{CM} = \pm 10V$	●	105	118	—	90	110	—	dB
ΔPSRR	Power Supply Rejection Ratio Match	$V_S = \pm 4.5V$ to $\pm 18V$	●	—	2	16	—	4	51	μV/V

at $V_S = \pm 15V$, $-25°C \leq T_A \leq 85°C$, unless otherwise noted

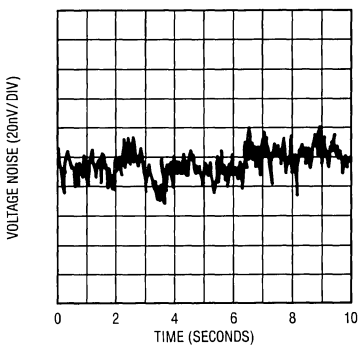
SYMBOL	PARAMETER	CONDITIONS		OP-227E, OP-237E			OP-227G, OP-237G			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	
ΔV_{OS}	Input Offset Voltage Match		●	—	40	140	—	90	400	μV
$TC\Delta V_{OS}$	Input Offset Voltage Tracking	(Note 7)	●	—	0.3	1.0	—	0.5	1.8	μV/°C
I_B^+	Average Non-Inverting Bias Current		●	—	±14	±60	—	±25	±170	nA
$\frac{\Delta I_B^+}{\Delta Temp}$	Average Drift of Non-Inverting Bias Current		●	—	80	—	—	180	—	pA/°C
I_{OS}^+	Non-Inverting Offset Current		●	—	±20	±90	—	±35	±250	nA
$\frac{\Delta I_{OS}^+}{\Delta Temp}$	Average Drift of Non-Inverting Offset Current		●	—	130	—	—	250	—	pA/°C
I_{OS}^-	Inverting Offset Current		●	—	±20	±90	—	±35	±250	nA
ΔCMRR	Common Mode Rejection Ratio Match	$V_{CM} = \pm 10V$	●	106	120	—	90	112	—	dB
ΔPSRR	Power Supply Rejection Ratio Match	$V_S = \pm 4.5V$ to $\pm 18V$	●	—	2	15	—	3	32	μV/V

TYPICAL PERFORMANCE CHARACTERISTICS

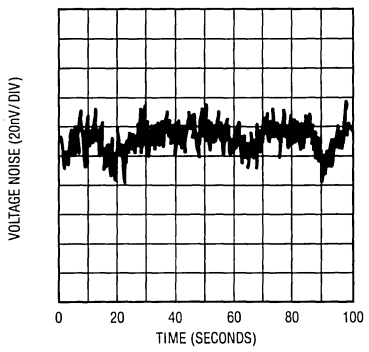
Voltage Noise vs Frequency



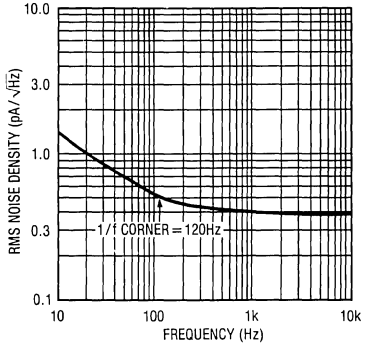
0.1Hz to 10Hz Noise



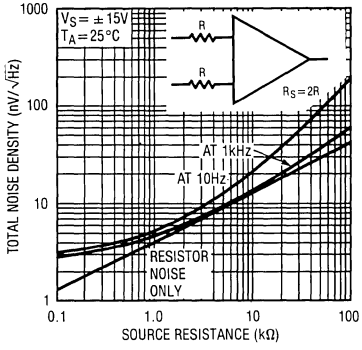
0.01Hz to 1Hz Peak-to-Peak Noise



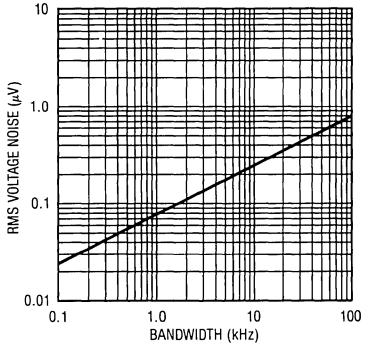
Current Noise vs Frequency



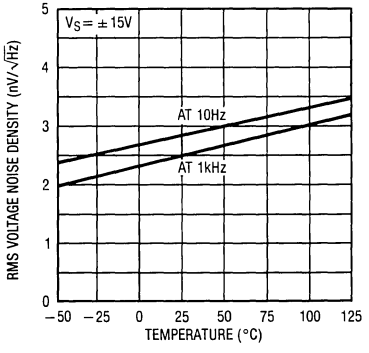
Total Noise vs Source Resistance



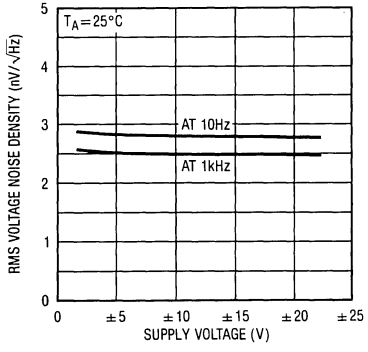
Wideband Voltage Noise (0.1Hz to Frequency Indicated)



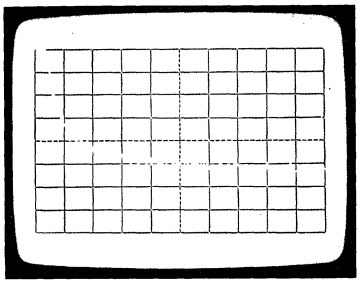
Voltage Noise vs Temperature



Voltage Noise vs Supply Voltage



0.02Hz to 10Hz RMS Noise. Gain = 50,000 (Measured on HP3582 Spectrum Analyzer)

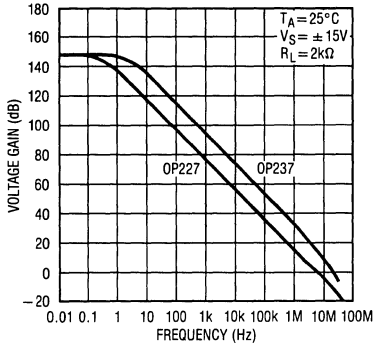


MARKER AT 2Hz (= 1/f CORNER) =

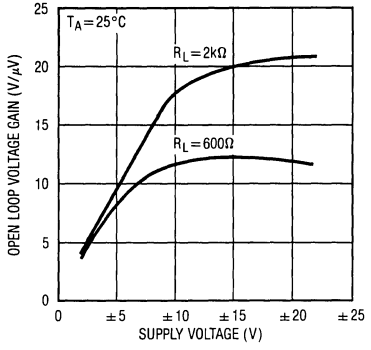
$$\frac{179\mu V/\sqrt{Hz}}{50{,}000} = 3.59\frac{nV}{\sqrt{Hz}}$$

TYPICAL PERFORMANCE CHARACTERISTICS

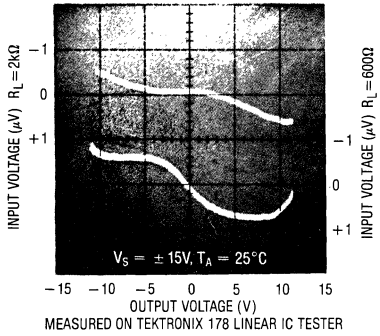
Voltage Gain vs Frequency



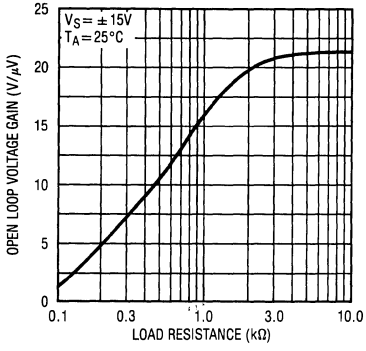
Voltage Gain vs Supply Voltage



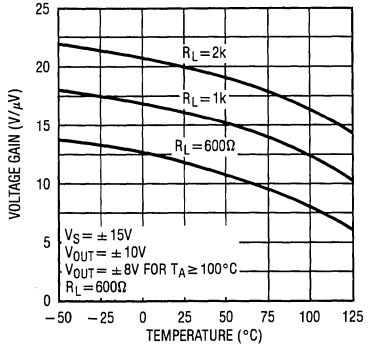
Voltage Gain, R_L=2k and 600Ω



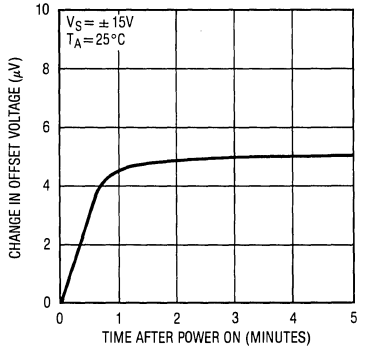
Voltage Gain vs Load Resistance



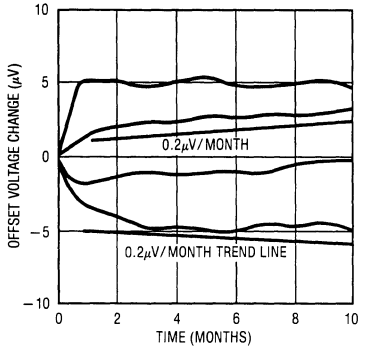
Voltage Gain vs Temperature



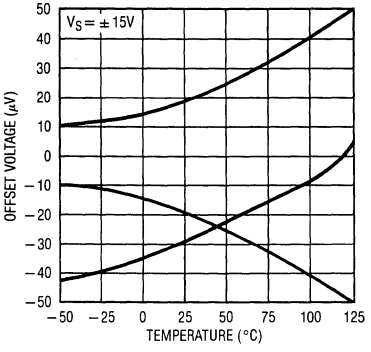
Warm-Up Drift



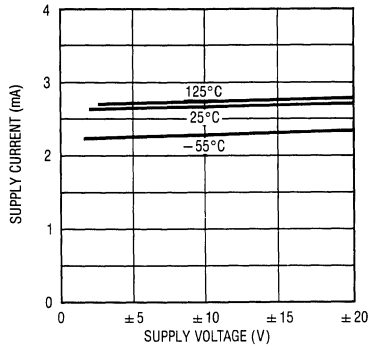
Long Term Stability of Four Representative Units



Offset Voltage Drift with Temperature of Representative Units

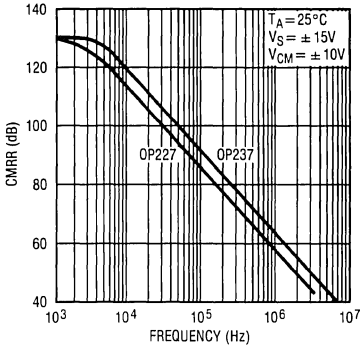


Supply Current vs Supply Voltage

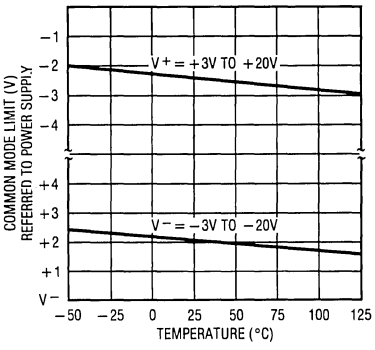


TYPICAL PERFORMANCE CHARACTERISTICS

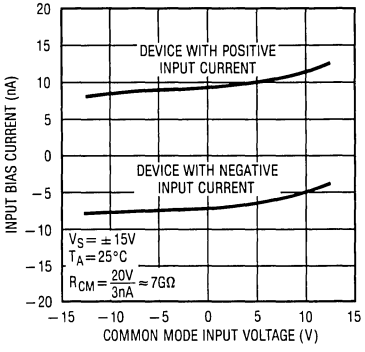
Common Mode Rejection vs Frequency



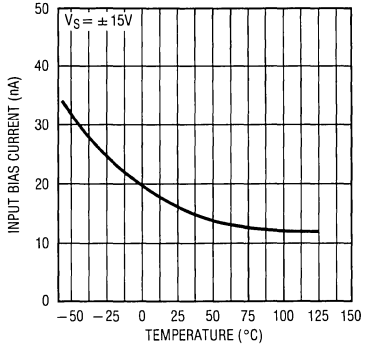
Common Mode Limit vs Temperature



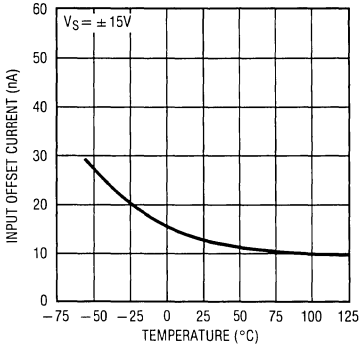
Input Bias Current Over the Common Mode Range



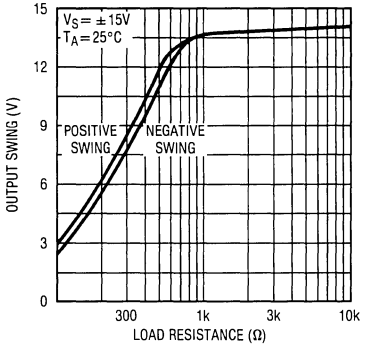
Input Bias Current vs Temperature



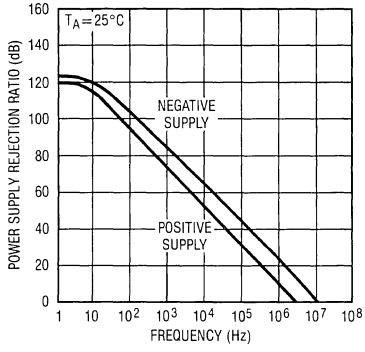
Input Offset Current vs Temperature



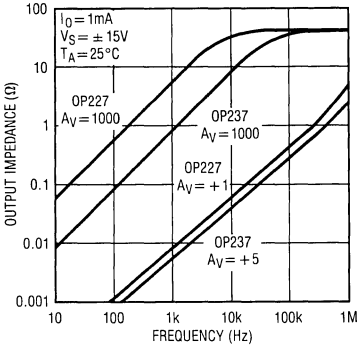
Output Swing vs Load Resistance



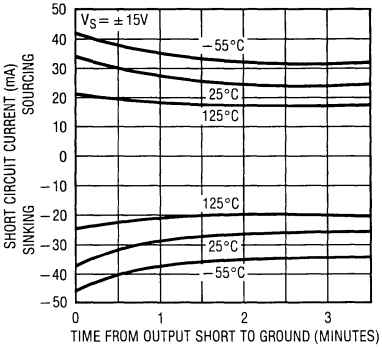
PSRR vs Frequency



Closed Loop Output Impedance

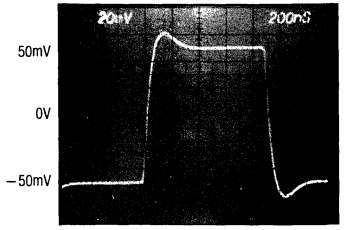


Output Short Circuit Current vs Time



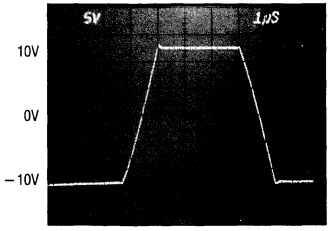
TYPICAL PERFORMANCE CHARACTERISTICS

OP-237 Small Signal Transient Response



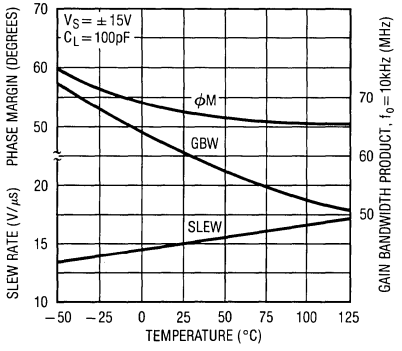
$A_{VCL} = +5V$, $V_S = \pm 15V$
$C_L = 15pF$

OP-237 Large Signal Response

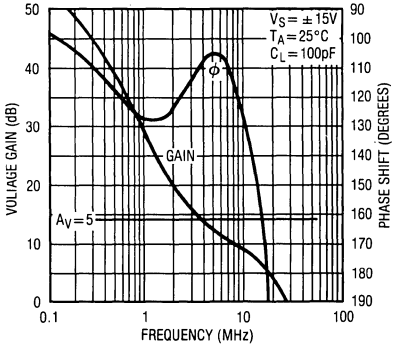


$A_{VCL} = +5$, $V_S = \pm 15V$

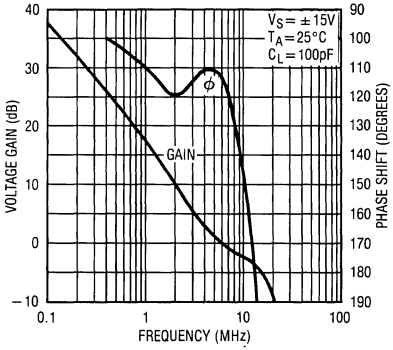
OP-237 Phase Margin, Gain Bandwidth Product, Slew Rate vs Temperature



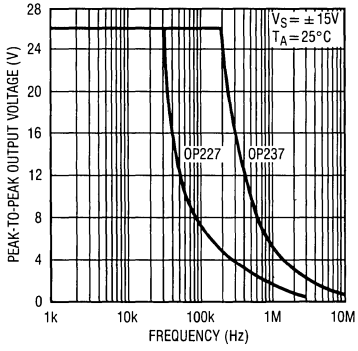
OP-237 Gain, Phase Shift vs Frequency



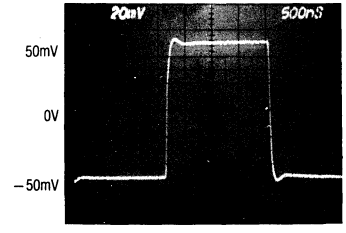
OP-227 Gain, Phase Shift vs Frequency



Maximum Undistorted Output vs Frequency

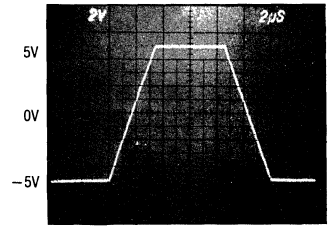


OP-227 Small Signal Transient Response



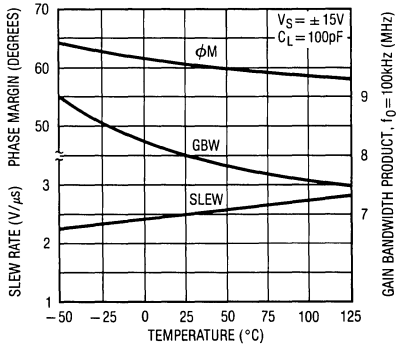
$A_{VCL} = +1$, $V_S = \pm 15V$
$C_L = 15pF$

OP-227 Large Signal Response



$A_{VCL} = -1$, $V_S = \pm 15V$

OP-227 Phase Margin, Gain Bandwidth Product, Slew Rate vs Temperature



APPLICATIONS INFORMATION

Noise Testing

The 0.1Hz to 10Hz peak-to-peak noise of the OP-227/OP-237 is measured in the test circuit shown. The frequency response of this noise tester indicates that the 0.1Hz corner is defined by only one zero. The test time to measure 0.1Hz to 10Hz noise should not exceed 10 seconds, as this time limit acts as an additional zero to eliminate noise contributions from the frequency band below 0.1Hz.

Measuring the typical 60nV peak-to-peak noise performance of the OP-227/OP-237 requires special test precautions:

(a) The device should be warmed up for at least five minutes. As the op amp warms up, its offset voltage changes typically 3μV due to its chip temperature increasing 10°C to 20°C from the moment the power supplies are turned on. In the 10 second measurement interval these temperature-induced effects can easily exceed tens of nanovolts.

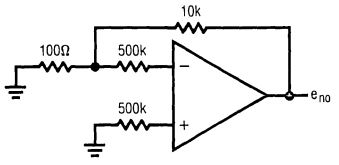
(b) For similar reasons, the device must be well shielded from air currents to eliminate the possibility of thermoelectric effects in excess of a few nanovolts, which would invalidate the measurements.

(c) Sudden motion in the vicinity of the device can also "feed through" to increase the observed noise.

A noise-voltage density test is recommended when measuring noise on a large number of units. A 10Hz noise voltage density measurement will correlate well with a 0.1Hz to 10Hz peak-to-peak noise reading since both results are determined by the white noise and the location of the 1/f corner frequency.

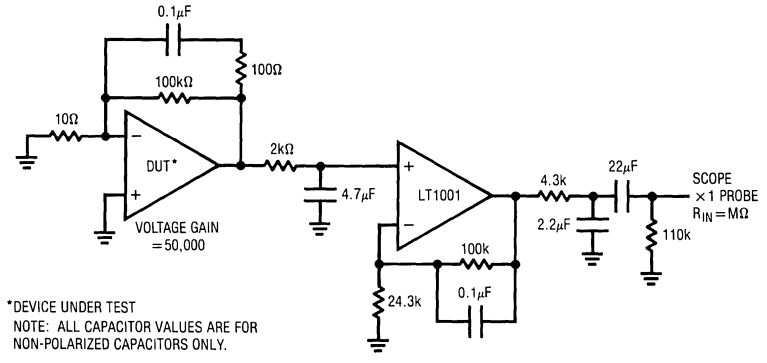
Current noise is measured in the circuit shown and calculated by the following formula:

$$i_n = \frac{[e^2_{no} - (130nV)^2]^{1/2}}{1M\Omega \times 100}$$



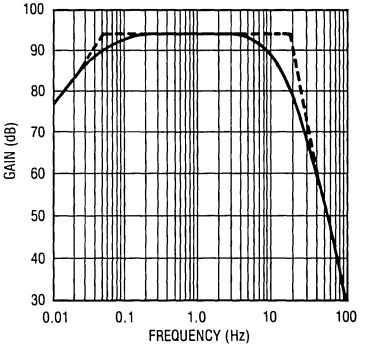
The OP-227/OP-237 achieves its low noise, in part, by operating the input stage at 120μA versus the typical 10μA of most other op amps. Voltage noise is inversely proportional, while current noise is directly proportional to the square root of the stage current. Therefore, the OP-227/OP-237 current noise will be relatively high. At low frequencies, the low 1/f current noise corner frequency (≈120Hz) minimizes current noise to some extent.

0.1Hz to 10Hz Noise Test Circuit



*DEVICE UNDER TEST
NOTE: ALL CAPACITOR VALUES ARE FOR NON-POLARIZED CAPACITORS ONLY.

0.1Hz to 10Hz p-p Noise Tester Frequency Response



APPLICATIONS INFORMATION

In most practical applications, however, current noise will not limit system performance. This is illustrated in the total noise versus source resistance plot, where total noise = $[(\text{voltage noise})^2 + (\text{current noise} \times R_S)^2 + (\text{resistor noise})^2]^{1/2}$.

Three regions can be identified as a function of source resistance:

(i) $R_S \leq 400\Omega$-Voltage noise dominates

(ii) $400\Omega \leq R_S \leq 50k\Omega$ at 1kHz Resistor noise
$400\Omega \leq R_S \leq 8k\Omega$ at 10Hz dominates

(iii) $R_S > 50k\Omega$ at 1kHz Current noise
$R_S > 8k\Omega$ at 10Hz dominates

Clearly the OP-227/OP-237 should not be used in region (iii), where total system noise is at least six times higher than the voltage noise of the op amp, i.e., the low voltage noise specification is completely wasted.

APPLICATIONS INFORMATION

OP AMP MATCHING

Advantages of Matched Dual Op Amps

In many applications the performance of a system depends on the matching between two operational amplifiers rather than the individual characteristics of the two op amps. Two or three op amp instrumentation amplifiers, tracking voltage references and low drift active filters are some of the circuits requiring matching between two op amps.

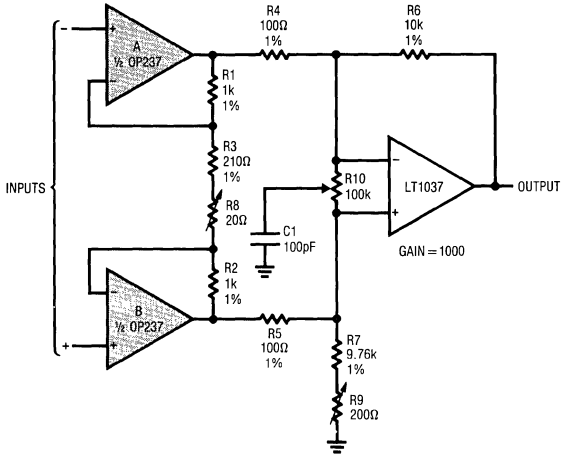
The well-known triple op amp configuration illustrates these concepts. Output offset is a function of the difference between the offsets of the two halves of the OP-227/OP-237. This error cancellation principle holds for a considerable number of input referred parameters in addition to offset voltage and its drift with temperature. Input bias current will be the average of the two noninverting input currents (I_B^+). The difference between these two currents (I_{OS}^+) is the offset current of the instrumentation amplifier. The difference between the inverting input currents (I_{OS}^-) will cause errors flowing through R1, R2, and R3. Common mode and power supply rejections will be dependent only on the match between the two amplifiers (assuming perfect resistor matching).

The concepts of common mode and power supply rejection ratio match (ΔCMRR and ΔPSRR) are best demonstrated with a numerical example:

Assume $CMRR_A = +1.0\mu V/V$ or 120dB,
and $CMRR_B = +0.75\mu V/V$ or 122.5dB,
then $\Delta CMRR = 0.25\mu V/V$ or 132dB;
if $CMRR_B = -0.75\mu V/V$ which is still 122.5dB,
then $\Delta CMRR = 1.75\mu V/V$ or 115dB.

Clearly, the OP-227/OP-237, by specifying and guaranteeing all of these matching parameters, can significantly improve the performance of matching dependent circuits.

Three Op Amp Instrumentation Amplifier



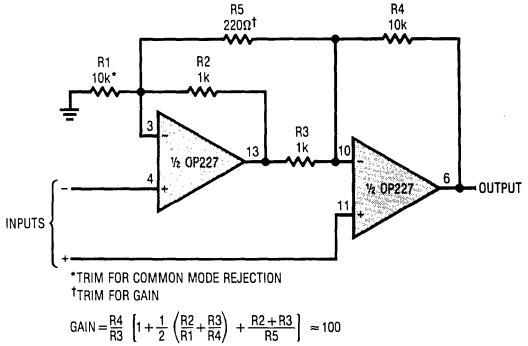
Trim R8 for gain
Trim R9 for DC common mode rejection
Trim R10 for AC common mode rejection

Typical performance of the instrumentation amplifier:

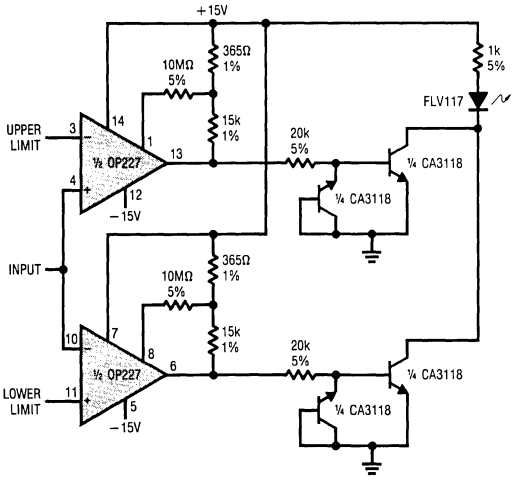
Input offset voltage = $60\mu V$
Input bias current = $\pm 15nA$
Input offset current = $\pm 20nA$
Input noise = $0.08\mu Vp\text{-}p$
Power bandwidth ($V_O = \pm 10V$) = 250kHz

APPLICATIONS INFORMATION

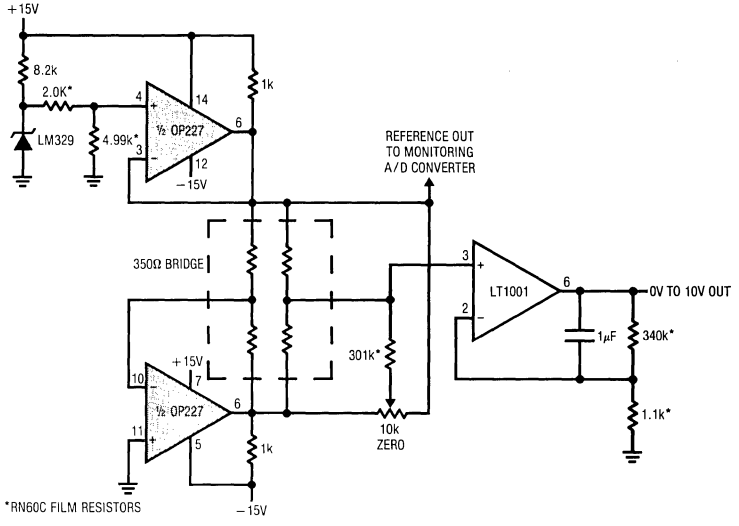
Two Op Amp Instrumentation Amplifier



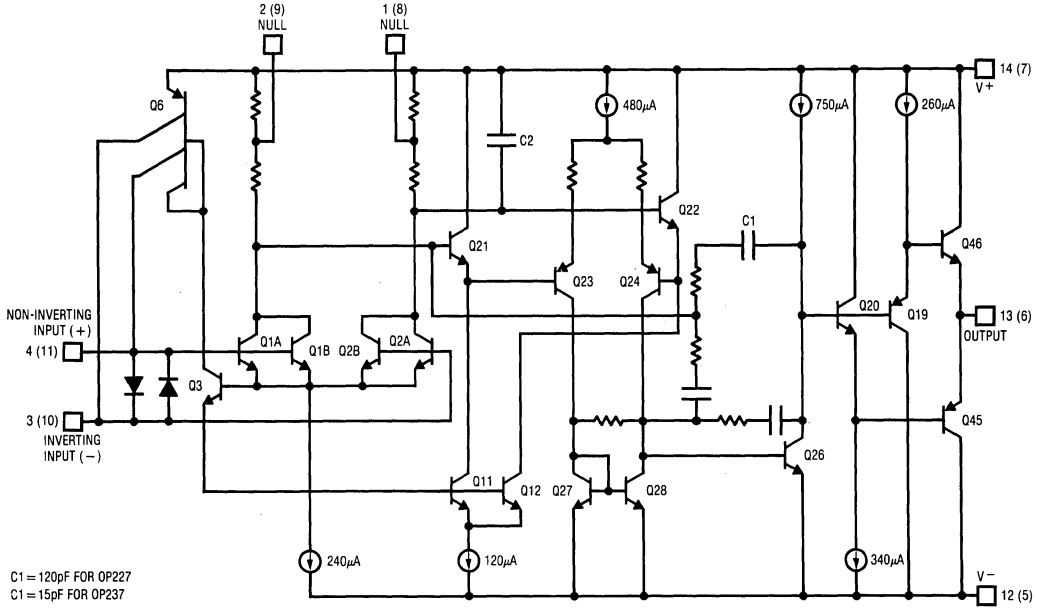
Dual Limit Microvolt Comparator



Strain Gauge Signal Conditioner with Bridge Excitation

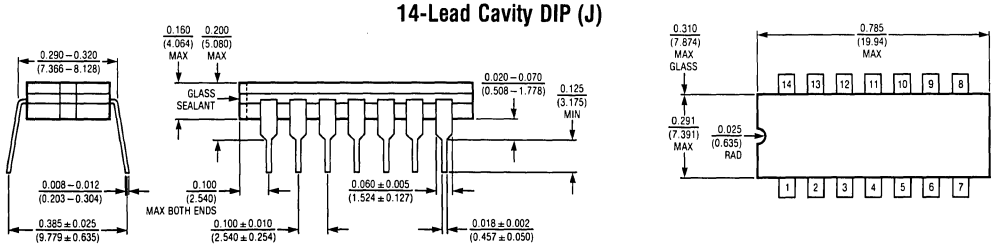


SCHEMATIC DIAGRAM



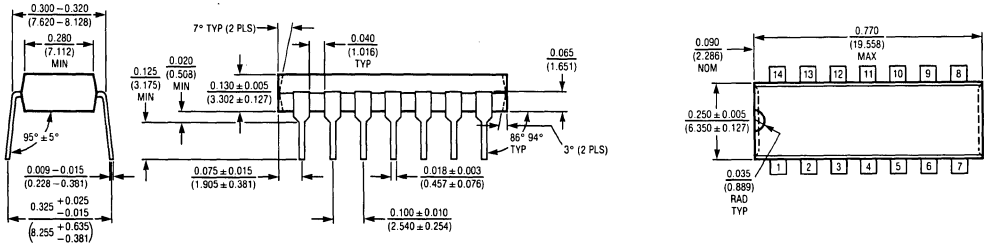
PACKAGE DESCRIPTION Dimensions in inches (millimeters) unless otherwise noted.

14-Lead Cavity DIP (J)



OP-227EJ OP-237EJ OP-227GJ OP-237GJ	T_{JMAX} 125°C	Θ_{JA} 100°C/W
OP-227AJ OP-237AJ OP-227CJ OP-237CJ	150°C	100°C/W

14-Lead Molded DIP (N)



OP-227EN OP-237EN OP-227GN OP-237GN	T_{JMAX} 125°C	Θ_{JA} 100°C/W

SECTION 3—VOLTAGE REGULATORS

SECTION 3—VOLTAGE REGULATORS

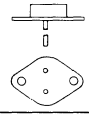
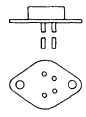
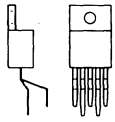
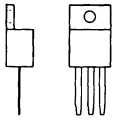
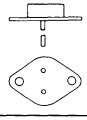
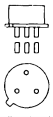
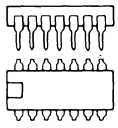
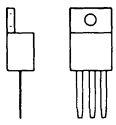
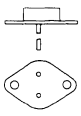
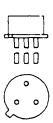
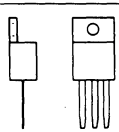
MILITARY

I_o OUTPUT CURRENT (AMPS)	POSITIVE OR NEGATIVE OUTPUT	PART NUMBER	PACKAGE TYPE	V_{in} MAX (V)	V_o NOMINAL REGULATED OUTPUT VOLTAGE (V)	FEATURES/COMMENTS
10.0	POS. ADJ.	LT1038MK	STEEL TO-3	35	1.2 TO 33	0.8% V_{OUT} TOL, PLUG IN COMPATIBLE WITH 117, 150, 138.
5.0	POS. FIXED	LT1003MK	STEEL TO-3	20	5	2% V_{OUT} TOL.
	POS. ADJ.	LT138AK LM138K	STEEL TO-3	35	1.2 TO 33	LT138A HAS 1% V_{REF} TOL.
3.0	POS. FIXED	LT123AK LM123K	STEEL TO-3	20	5	LT123A HAS 1% V_{OUT} TOL.
	POS. ADJ.	LT150AK LM150K	STEEL TO-3	35	1.2 TO 33	LT150A HAS 1% V_{REF} TOL.
	NEG. ADJ.	LT1033MK	STEEL TO-3	40	−1.2 TO −37	2% V_{REF} TOL.
	DUAL POS. FIXED	LT1035MK	STEEL TO-3	20	TWO 5V OUTPUTS	LOGIC CONTROLLED MAIN OUTPUT VOLTAGE, 75mA AUXILIARY OUTPUT
	POSITIVE	LT1036MK	STEEL TO-3	30	12,5	LOGIC CONTROLLED 12V, 3A OUTPUT, 5V, 75mA AUXILIARY OUTPUT
	POS. ADJ.	LT117AK LM117K LT117AH LM117H	STEEL TO-3 TO-39	40 40	1.2 TO 37	LT117A HAS 1% V_{REF} TOL.
	NEG. ADJ.	LT137AK LM137K LT137AH LM137H	STEEL TO-3 TO-39	40 40	−1.2 TO −37	LT137A HAS 1% V_{REF} TOL.
0.5 TO 1.5	POS. ADJ. HIGH VOLTAGE	LT117AHVK LM117HVK LT117AHVH LM117HVH	STEEL TO-3 TO-39	60 60	1.2 TO 57	LT117AHV HAS 1% V_{REF} TOL.
	NEG. ADJ. HIGH VOLTAGE	LT137AHVK LM137HVK LT137AHVH LM137HVH	STEEL TO-3 TO-39	50 50	−1.2 TO −47	LT137AHV HAS 1% V_{REF} TOL.
1.0	DUAL POS. FIXED	LT1005MK	STEEL TO-3	20	TWO 5V OUTPUTS	LOGIC CONTROLLED 1 AMP MAIN OUTPUT VOLTAGE, 35mA AUXILIARY OUTPUT.
125mA	POSITIVE	LT1020MJ	14 PIN CERDIP	36	4 TO 30	DROPOUT VOLTAGE = 0.5V, 40μA I_Q, REFERENCE AND COMPARATOR

COMMERCIAL

I_o OUTPUT CURRENT (AMPS)	POSITIVE OR NEGATIVE OUTPUT	PART NUMBER	PACKAGE TYPE	V_{in} MAX (V)	V_o NOMINAL REGULATED OUTPUT VOLTAGE (V)	FEATURES/COMMENTS
10.0	POS. ADJ.	LT1038CK	STEEL TO-3	35	1.2 TO 33	2% V_{OUT} TOL, PLUG IN COMPATIBLE WITH 117, 150, 138.
5.0	POS. FIXED	LT1003CK	STEEL TO-3	20	5	2% V_{OUT} TOL.
	POS. ADJ.	LT338AK LM338K	STEEL TO-3	35	1.2 TO 33	LT338A HAS 1% V_{REF} TOL.
3.0	POS. FIXED	LT323AK LM323K LT323AT	STEEL TO-3 TO-220	20 20	5	LT323A HAS 1% V_{OUT} TOL.
	POS. ADJ.	LT350AK LM350K LT350AT LM350T	STEEL TO-3 TO-220	35 35	1.2 TO 33	LT350A HAS 1% V_{REF} TOL.
	NEG. ADJ.	LT1033CK LT1033CT	STEEL TO-3 TO-220	40 40	−1.2 TO −37	2% V_{REF} TOL.
	DUAL POS. FIXED	LT1035CK LT1035CT	STEEL TO-3 TO-220	20 20	TWO 5V OUTPUTS	LOGIC CONTROLLED MAIN OUTPUT VOLTAGE, 75mA AUXILIARY OUTPUT
	POSITIVE	LT1036CK LT1036CT	STEEL TO-3 TO-220	30 30	12,5 12,5	LOGIC CONTROLLED 12V, 3A OUTPUT, 5V, 75mA AUXILIARY OUTPUT
	POS. ADJ.	LT317AK LM317K LT317AH LM317H LT317AT LM317T	STEEL TO-3 TO-39 TO-220	40 40 40	1.2 TO 37	LT317A HAS 1% V_{REF} TOL.
0.5 TO 1.5	NEG. ADJ.	LT337AK LM337K LT337AH LM337H LT337AT LM337T	STEEL TO-3 TO-39 TO-220	40 40 40	−1.2 TO −37	LT337A HAS 1% V_{REF} TOL.
	POS. ADJ. HIGH VOLTAGE	LT317AHVK LM317HVK LT317AHVH LM317HVH	STEEL TO-3 TO-39	60 60	1.2 TO 57	LT317 HV HAS 1% V_{REF} TOL.
	NEG. ADJ. HIGH VOLTAGE	LT337AHVK LM337HVK LT337AHVH LM337HVH	STEEL TO-3 TO-39	50 50	−1.2 TO −47	LT337 HV HAS 1% V_{REF} TOL.
1.0	DUAL POS. FIXED	LT1005CK LT1005CT	STEEL TO-3 TO-220	20 20	TWO 5V OUTPUTS	LOGIC CONTROLLED MAIN OUTPUT VOLTAGE.
125mA	POSITIVE	LT1020CJ LT1020CN	14 PIN CERDIP 14 PIN PLASTIC	36	4 TO 30 4 TO 30	DROPOUT VOLTAGE = 0.5V, 40μA I_Q, REFERENCE AND COMPARATOR

REGULATOR SELECTION GUIDE

		MILITARY	COMMERCIAL	FEATURES
POSITIVE FIXED		LT1003MK LT123AK LM123K	LT1003CK LT323AK LM323K	5V ± 2%, 5 AMP 5V ± 1%, 3 AMP 5V ± 3%, 3 AMP
		LT1005MK	LT1005CK	DUAL OUTPUT REGULATOR WITH 5V 1AMP LOGIC SWITCHABLE OUTPUT AND AUXILIARY 5V 35mA OUTPUT
		LT1035MK	LT1035CK	DUAL OUTPUT REGULATOR WITH 5V 3AMP LOGIC SWITCHABLE OUTPUT AND AUXILIARY 5V 75mA OUTPUT
		LT1036MK	LT1036CK	DUAL OUTPUT REGULATOR WITH 12V 3AMP LOGIC SWITCHABLE OUTPUT AND AUXILIARY 5V, 75mA OUTPUT
			LT1005CT	DUAL OUTPUT REGULATOR WITH 5V 1AMP LOGIC SWITCHABLE OUTPUT AND AUXILIARY 5V 35mA OUTPUT
			LT1035CT	DUAL OUTPUT REGULATOR WITH 5V 3AMP LOGIC SWITCHABLE OUTPUT AND AUXILIARY 5V 75mA OUTPUT
			LT1036CT	DUAL OUTPUT REGULATOR WITH 12V 3AMP LOGIC SWITCHABLE OUTPUT AND AUXILIARY 5V, 75mA OUTPUT
			LT323AT	5V ± 1%, 3 A
POSITIVE ADJUSTABLES		LT1038MK LT138AK LM138K LT150AK LM150K LT117AK LM117K LT117AHVK LM117AHVK	LT1038CK LT338AK LM338K LT350AK LM350K LT317AK LM317K LT317AHVK LM317AHVK	10 AMP 1% REFERENCE, 5 AMP 5 AMP 1% REFERENCE, 3 AMP 3 AMP 1% REFERENCE, 1.5 AMP 1.5 AMP 1% REFERENCE, 1.5 AMP, HI VOLTAGE 1.5 AMP, HI VOLTAGE
		LT117AH LM117H LT117AHVH LM117HVH	LT317AH LM317H LT317AHVH LM317HVH	1% REFERENCE, 0.5 AMP 0.5 AMP 1% REFERENCE, 0.5 AMP, HI VOLTAGE 0.5 AMP, HI VOLTAGE
		LT1020MJ	LT1020CJ LT1020CN	VERY LOW DROPOUT VOLTAGE, 40μA SUPPLY CURRENT, 2.5V INDEPENDENT REFERENCE, AND VOLTAGE COMPARATOR ON SAME CHIP.
			LT350AT LM350T LT317AT LM317T	1% REFERENCE, 3 A 3 AMP 1% REFERENCE, 1.5 AMP 1.5 AMP
NEGATIVE ADJUSTABLES		LT137AK LM137K LT137AHVK LM137HVK LT1033MK	LT337AK LM337K LT337AHVK LT337HVK LT1033CK	1% REFERENCE, 1.5 AMP 1.5 AMP 1% REFERENCE, 1.5 AMP, HI VOLTAGE 1.5 AMP, HI VOLTAGE 2% REFERENCE, 3 AMP
		LT137AH LM137H LT137AHVH LM137 HVH	LT337AH LM337H LT337AHVH LM337HVH	1% REFERENCE, 0.5 AMP 0.5 AMP 1% REFERENCE, 0.5 AMP, HI VOLTAGE 0.5 AMP, HI VOLTAGE
			LT337AT LM337T LT1033CT	1% REFERENCE, 1.5 AMP 1.5 AMP 2% REFERENCE, 3 AMP

5 Volt, 5 Amp Voltage Regulator

FEATURES

- *Guaranteed* 2% Initial Tolerance of output voltage
- 5 Amp Output Current
- 40 Watt Capability
- Full Internal Overload Protection
- 100% Burn-in in Thermal Limit

APPLICATIONS

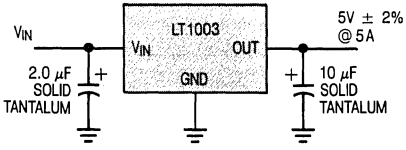
- Local 5V Regulators
- On Card Regulation
- Lab Supplies
- Instrumentation Supplies

DESCRIPTION

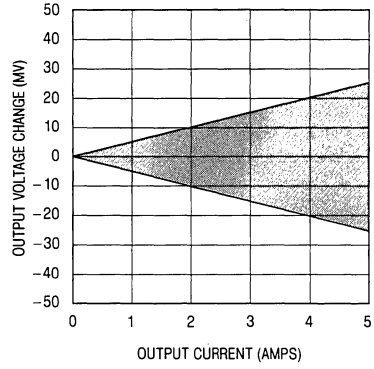
The LT1003 is a 5 amp version of the popular LM123 5V regulator. In addition to higher output current, it offers improved line regulation and an initial output voltage tolerance of ±2%. These tightened specifications ease design and application problems several ways: safety margin is improved, error budgets on other parts of the system are expanded, and output voltage loss due to long supply runs can be better tolerated.

The LT1003 incorporates Linear Technology's advanced design, process and test techniques for improved quality and reliability over similar device types. Specifically, all devices are burned in by shorting the outputs, thereby forcing the regulator into its current limit and eventually, thermal limit mode. This ensures that all device protection features are working.

Standard 5 Volt Regulator



Load Regulation *

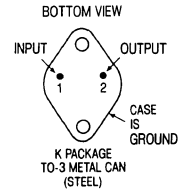


* The LT1003 has load compensation to cancel the effects of voltage loss in the output lead. This results in a nominal "zero" load regulation. The shaded band shows typical production spread.

ABSOLUTE MAXIMUM RATINGS

Input Voltage ..... 20 Volts
Power Dissipation ..... Internally Limited
Operating Junction Temperature Range
LT1003M ..... −55°C to 150°C
LT1003C ..... 0°C to 125°C
Storage Temperature Range
LT1003M ..... −65°C to 150°C
LT1003C ..... −65°C to 150°C
Lead Temperature (Soldering, 10 sec.)..... 300°C

PACKAGE/ORDER INFORMATION



K PACKAGE
TO-3 METAL CAN
(STEEL)

ORDER PART NO.
LT1003CK
LT1003MK

PRECONDITIONING

100% Burn-In in Thermal Limit

ELECTRICAL CHARACTERISTICS (See Note 1)

SYMBOL	PARAMETER	CONDITIONS		LT1003M MIN	LT1003M TYP	LT1003M MAX	LT1003C MIN	LT1003C TYP	LT1003C MAX	UNITS
V_{OUT}	Output Voltage	$T_j = 25°C$, $V_{IN} = 7.5V$, $I_{OUT} = 0$		4.9	5.0	5.1	4.9	5.0	5.1	V
		$7.5V \leq V_{IN} \leq 15V$ $0 \leq I_{OUT} \leq 5A$, $P \leq 30W$	●	4.8		5.2	4.8		5.2	V
$\frac{\Delta V_{OUT}}{\Delta V_{IN}}$	Line Regulation	$T_j = 25°C$, $7.5V \leq V_{IN} \leq 15V$ (See Note 1)			5	15		5	15	mV
$\frac{\Delta V_{OUT}}{\Delta I_{OUT}}$	Load Regulation	$T_j = 25°C$, $V_{IN} = 7.5V$ $0 \leq I_{OUT} \leq 5A$ (See Note 1)			25	100		25	100	mV
	Thermal Regulation	$T_j = 25°C$, 20 msec pulse			0.005	0.02		0.005	0.02	%/W
I_Q	Quiescent Current	$7.5V \leq V_{IN} \leq 15V$, $0 \leq I_{OUT} \leq 5A$	●		12	20		12	20	mA
e_n	Output Noise Voltage	$T_j = 25°C$, $10Hz \leq f \leq 100kHz$			40			40		μV_{rms}
I_{SC}	Short Circuit Current Limit	$T_j = 25°C$, $V_{IN} = 15V$ $V_{IN} = 7.5V$			5 7	8 9		5 7	8 9	A A
	Long Term Stability of Output Voltage					35		35		mV
θ_{JC}	Thermal Resistance Junction to Case	K Package			1	1.5		1	1.5	°C/W

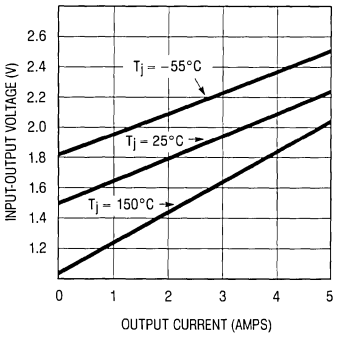
The ● denotes the specifications which apply over the full operating temperature range.

Note 1: Load and line regulation are tested with pulsed low duty cycle techniques where pulse width ≤ 1msec and duty cycle ≤ 5%.

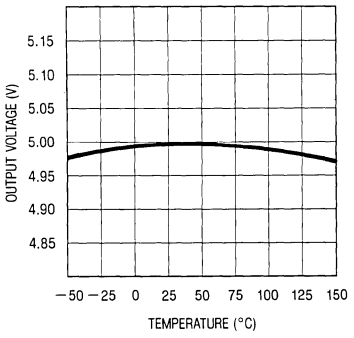
Note 2: $T_{min} = -55°C$ for the LT1003MK and 0°C for LT1003CK. $T_{max} = 150°C$ for LT1003MK and 125°C for LT1003CK.

TYPICAL PERFORMANCE CHARACTERISTICS

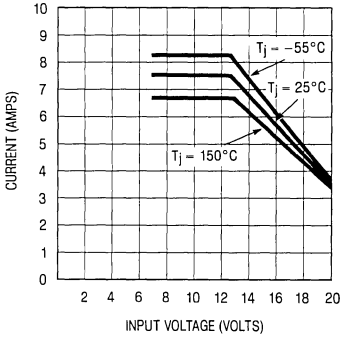
Minimum Input-Output Voltage Differential



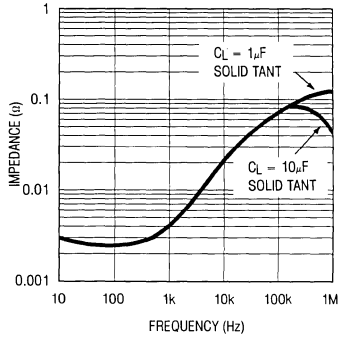
Output Voltage Temperature Drift



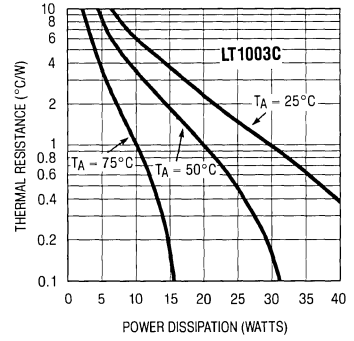
Peak Available Output Current



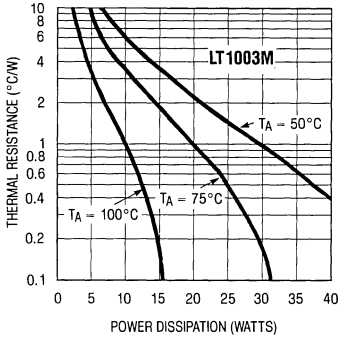
Output Impedance



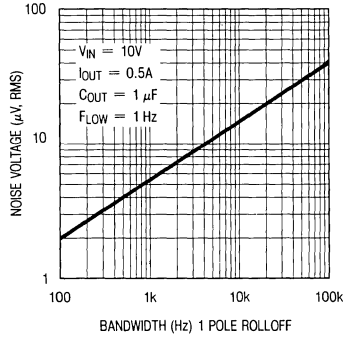
Suggested Heat Sink Thermal Resistance (LT1003C)



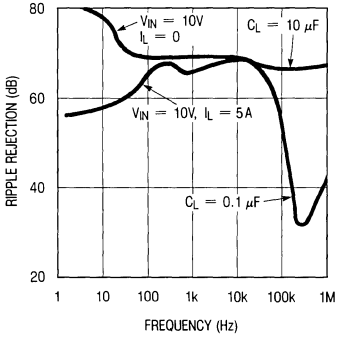
Suggested Heat Sink Thermal Resistance (LT1003M)



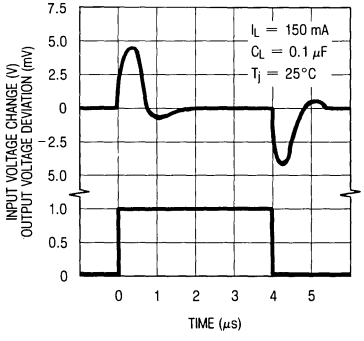
Output Noise Voltage



Ripple Rejection

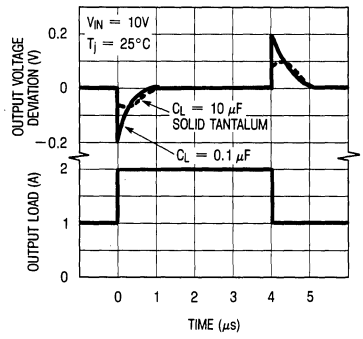


Line Transient Response

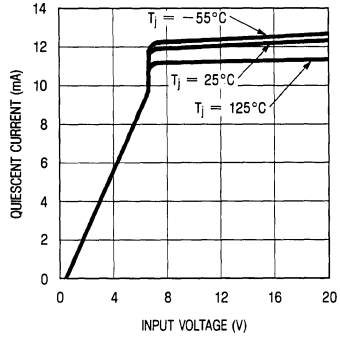


TYPICAL PERFORMANCE CHARACTERISTICS

Load Transient Response

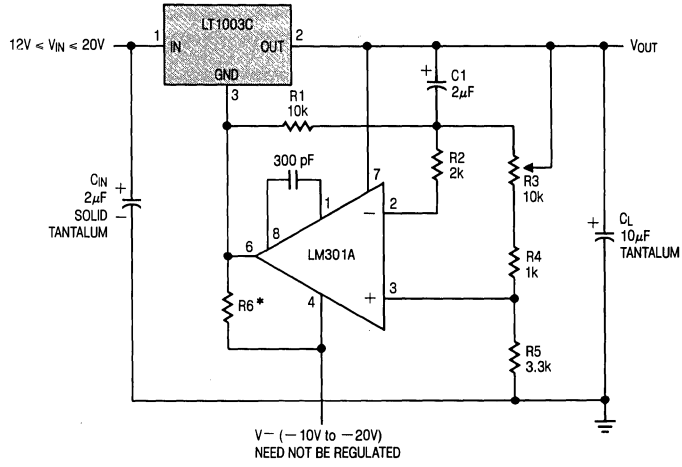


Quiescent Current



TYPICAL APPLICATIONS

Adjustable Regulator 0–10V @ 5A

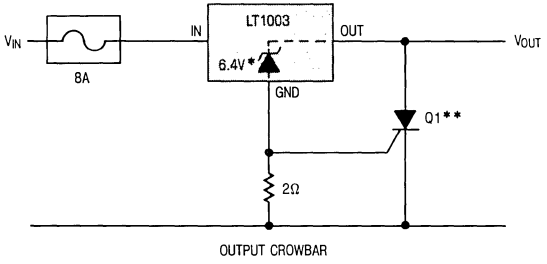


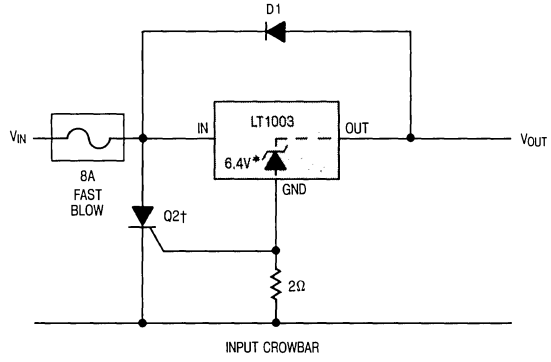
$$* R6 = \frac{V-}{12\ mA}$$

C_1 = OPTIONAL — IMPROVES RIPPLE REJECTION, NOISE AND TRANSIENT RESPONSE

TYPICAL APPLICATIONS

Crowbar Protection††





* THE 6.4V ZENER IS INTERNAL TO THE LT1003.

** Q1 MUST BE ABLE TO WITHSTAND CONTINUOUS CURRENTS OF 8A IF ADDITIONAL SYSTEM SHUTDOWN IS NOT USED.

† Q2 MUST WITHSTAND LARGE SURGE CURRENTS UNTIL THE 8A FUSE BLOWS. PEAK SURGE CURRENT IS LIMITED ONLY BY FUSE, WIRING, AND FILTER CAP RESISTANCE.

†† TRIP POINT IS APPROXIMATELY 7.3V.

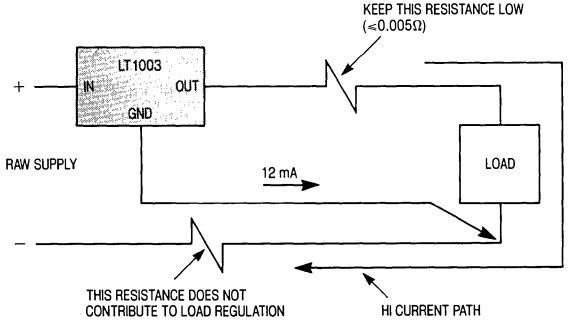
Bypass Capacitors

The LT1003 does not require an output capacitor for resistive loads. For almost all applications, however, a 1μF or larger solid tantalum capacitor is used on the output within 2″ of the regulator. This greatly improves the output impedance of the regulator at high frequencies. For critical applications where very low impedance is required at high frequencies, a 10μF solid tantalum output capacitor is recommended. Total output capacitance may be increased without limit, either local or distributed.

A 2μF or larger input capacitor (solid tantalum) must be added if the regulator is more than 4″ away from the large filter capacitor in the input supply. A 25μF aluminum capacitor may be substituted for the tantalum unit.

Avoiding Ground Loops

For best regulation, the ground pin of the LT1003 should be tied directly to the load point as shown below. This prevents excess drop in load voltage caused by load current flowing through the ground return lead. This is essentially a Kelvin connection for the low side of the regulator. A Kelvin connection cannot be made for the high output of the regulator because only three pins are available on the package. Therefore, every attempt should be made to minimize the resistance between the output pin of the regulator and the load. #18 gauge hookup wire has a resistance of 0.006 ohms per foot. This translates to 0.6% change in load voltage at full load current. The LT1003 is specified at 2% maximum load regulation, so one foot of wire represents a significant loss of regulation. If connectors are used, careful consideration must be given to contact resistance, especially if the connector is subjected to nasty ambients, vibration, or multiple insertions.



TYPICAL APPLICATIONS

Raw Supply

Transformer, diode, and capacitor selection for the raw supply to the LT1003 is very important because of the conflicting requirements for reliability, efficiency, and resistance to "brown-out" conditions. High secondary voltage on the transformer will cause unnecessarily high power dissipation in the regulator. Too low a secondary voltage will cause the regulator output to drop out of regulation with only a small reduction in AC mains voltage. The following formula gives a good starting point for transformer selection. This formula assumes a full-wave center tapped transformer, using two rectifier diodes.

$$V_{RMS} = \left(\frac{V_{OUT} + V_{DO} + V_{RECT} + V_{RIP)}}{\sqrt{2}}\right)\left(\frac{V_{NOM}}{V_{LOW}}\right) \quad (1.1^*)$$

(secondary each side)

$$I_{RMS} = (I_{OUT})\,(1.2)$$

where:

V_{OUT} = 5V
V_{DO} = Minimum input-output differential of the regulator

*1.1 is a nominal load regulation factor for the transformer

V_{RECT} = Rectifier forward drop at $3I_{OUT}$
V_{RIP} = ½ p-p capacitor ripple voltage

$$V_{RIP} \approx \frac{(5.3 \times 10^{-3})\,(I_{OUT})}{2C}$$

V_{NOM} = Rated line voltage for the transformer (RMS)
V_{LOW} = Lowest expected line voltage (RMS)
I_{OUT} = DC output current

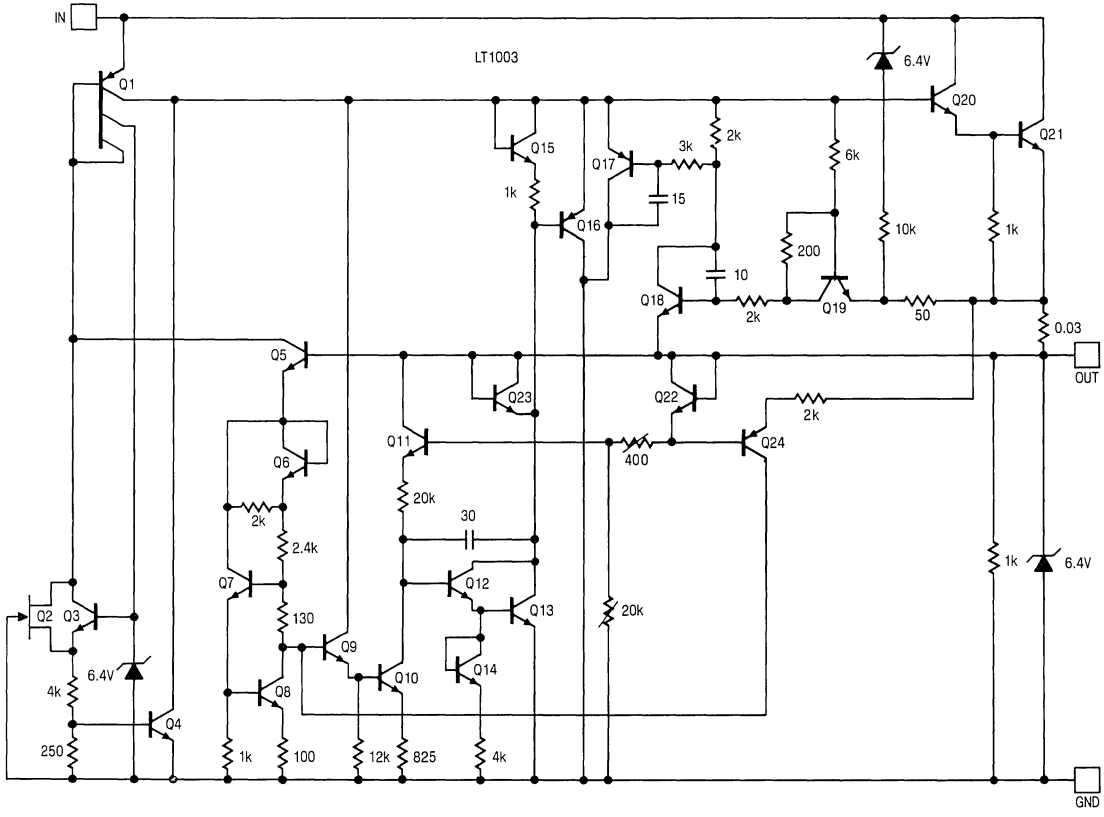
Example: I_{OUT} = 4A, V_{OUT} = 5V
Assume: V_{DO} = 2.5V, V_{RECT} = 1.1V, C = 12,000μF
V_{NOM} = 115V, V_{LOW} = 105V

$$V_{RIP} = \frac{(5.3 \times 10^{-3})\,(4)}{2\,(12 \times 10^{-3})} = 0.88V$$

$$V_{RMS} = \left(\frac{5 + 2.5 + 1.1 + 0.88}{\sqrt{2}}\right)\left(\frac{115}{105}\right)(1.1)$$
$$= 8.08\ V_{RMS}$$

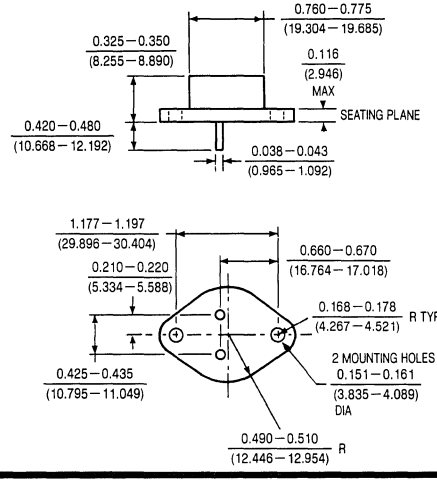
The filter capacitor should be at *least* 2000μF per amp of load current to minimize capacitor heating and ripple voltage. The diodes should be rated at 8–10 amps even though their average current is only 2.5A at full rated load current. The reason for this is that although the *average* current is 2.5A, the RMS current is typically twice this value. In addition, the diode must withstand very high surge currents during power turn-on. This surge can be 10–20 times the DC rating of the supply, depending on capacitor size and wiring resistance and inductance.

SCHEMATIC DIAGRAM



PACKAGE DESCRIPTION Dimensions in inches (millimeters) unless otherwise noted.

K Package TO-3 STEEL Metal Can



	T_j max.	θ_{ja}	θ_{jc}
LT1003MK	150°C	35°C/W	1.5°C/W
LT1003CK	125°C	35°C/W	1.5°C/W

FEATURES

- Two Regulated Outputs
  - +5V at 1 amp
  - +5V at 35mA
- 2% Output Voltage Tolerance
- 66 dB Ripple Rejection
- 0.5% Load Regulation
- TTL and CMOS Compatible Logic Control
- 100% Thermal Burn-in On All Devices

APPLICATIONS

- Power Supply Sequencing
- Remote On/Off Power Control
- Selective System Power During Emergency Power Operation
- Memory Power Supply With Back-Up

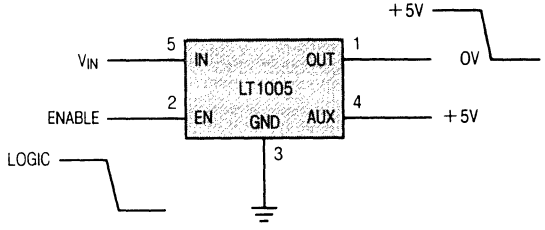
DESCRIPTION

The LT1005 features two positive 5 volt regulators in the same package. The main regulator offers excellent performance while supplying load currents up to 1 amp, and the auxiliary regulator provides similar performance while supplying lighter loads of 35mA. The main regulator has the additional feature of being under the shutdown control of a logic signal. When the enable pin is taken to a low logic level, the main regulator shuts down and its output voltage goes to near zero volts. During this command, the auxiliary output is unaffected by the main regulator's condition and continues to provide a 5 volt output.

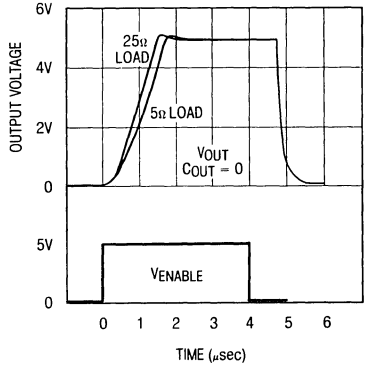
The main output has current and power limiting combined with thermal shutdown to make it virtually blow-out proof. The auxiliary output is not affected by the thermal shutdown mechanism or the state of the main output, allowing it to be used as a back-up in case of overloads or shorts on the main supply.

The logic input of the LT1005 (enable pin) has a 1.6V threshold and can be driven from a high source impedance. This allows it to be driven by most logic families, including TTL & CMOS.

Functional Diagram



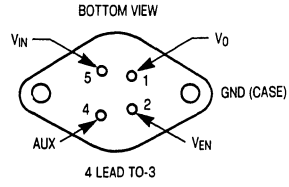
Switching Characteristics



ABSOLUTE MAXIMUM RATINGS

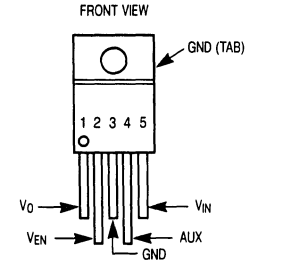
Power Dissipation ..... Internally Limited
Input Voltage (V_{IN}) 20V
Enable Voltage (V_{EN}) 20V
Operating Junction Temperature
LT1005M ..... −55°C to 150°C
LT1005C ..... 0°C to 125°C
Storage ..... −65°C to 150°C
Lead Temperature (Soldering, 10 sec.)..... 300°C

PACKAGE/ORDER INFORMATION



4 LEAD TO-3

LT1005MK
LT1005CK



5 LEAD TO-220

LT1005CT

PRECONDITIONING:

100% Burn-in in thermal limit

ELECTRICAL CHARACTERISTICS — MAIN REGULATOR (See Note 1)

SYMBOL	PARAMETER	CONDITIONS		LT1005M MIN	LT1005M TYP	LT1005M MAX	LT1005C MIN	LT1005C TYP	LT1005C MAX	UNITS
V_O	Output Voltage	$T_j = 25°C$		4.9	5.0	5.1	4.9	5.0	5.1	V
	High	$7.4V \leq V_{IN} \leq 20V$ $P_d \leq 10W$ $0mA \leq I_O \leq 1A$	●	4.8	5.0	5.2	4.8	5.0	5.2	V
	Low	$7.2V \leq V_{IN} \leq 20V$ $I_O = 0$	●		0.1	0.3		0.1	0.3	V
$\frac{\Delta V_O}{\Delta I_O}$	Load Regulation	$7.5V \leq V_{IN} \leq 15V$ $0mA \leq I_O \leq 1A$ (Note 2)	●		5	25		5	25	mV
$\frac{\Delta V_O}{\Delta V_{IN}}$	Line Regulation	$7.4V \leq V_{IN} \leq 20V$ (Note 2)			0.3	2		0.3	2	mV/V
	Ripple Rejection	$50Hz \leq f \leq 500Hz$			66			66		dB
	Thermal Regulation	$\Delta P_d = 10W$ (Note 4)			0.005	0.02		0.005	0.02	%/W
I_O	Available Load Current	$7.4V \leq V_{IN} \leq 15V$ $V_{IN} = 20V$		1 0.7	1.7 1.3		1 0.7	1.7 1.0		A A
I_{SC}	Short Circuit Current	$7.0V \leq V_{IN} \leq 15V$ $V_{IN} = 20V$			1.5 1.2	2.5 2.0		1.5 1.2	2.5 2.0	A A
V_{IN}	Minimum Input Voltage to Maintain Regulation	(Note 5) $I_O = 0.2A$ $I_O = 1.0A$	 ● ●	 7.0 7.5	 6.5 7.0		 6.9 7.5	 6.5 7.0		 V V
I_Q	Quiescent Current	 Output High Output Low			 2 1.5	 4 3		 2 1.5	 4 4	 mA mA
Θ_{JC}	Thermal Resistance Junction to Case	TO-3 TO-220			3	4		3 3	4 5	°C/W °C/W

ELECTRICAL CHARACTERISTICS — AUXILIARY REGULATOR (See Note 1)

SYMBOL	PARAMETER	CONDITIONS		LT1005M MIN	LT1005M TYP	LT1005M MAX	LT1005C MIN	LT1005C TYP	LT1005C MAX	UNITS
V_O	Output Voltage	$T_j = 25°C$		4.9	5.0	5.1	4.9	5.0	5.1	V
		$7.0V \leq V_{IN} \leq 20V$ $0mA \leq I_O \leq 35mA$	●	4.8	5.0	5.2	4.8	5.0	5.2	V
$\frac{\Delta V_O}{\Delta I_O}$	Load Regulation	$7.0V \leq V_{IN} \leq 20V$ $0mA \leq I_O \leq 35mA$ (Note 2)	●		5	15		5	15	mV
$\frac{\Delta V_O}{\Delta V_{IN}}$	Line Regulation	$7.0V \leq V_{IN} \leq 20V$ (Note 2)			0.2	1		0.2	1	mV/V
	Ripple Rejection	$50Hz \leq f \leq 500Hz$			74			74		dB
I_{SC}	Short Circuit Current	$7.0V \leq V_{IN} \leq 20V$			90	150		90	150	mA
V_{IN}	Minimum Input Voltage to Maintain Regulation	(Note 5) $I_O = 1mA$ $I_O = 35mA$	 ● ●	 6.5 6.9	 6.1 6.5	 	 6.5 6.9	 6.1 6.5	 	 V V

ELECTRICAL CHARACTERISTICS — LOGIC CONTROL (See Note 1)

SYMBOL	PARAMETER	CONDITIONS		LT1005M MIN	LT1005M TYP	LT1005M MAX	LT1005C MIN	LT1005C TYP	LT1005C MAX	UNITS
V_{EN}	Enable Threshold Voltage	$7.0V \leq V_{IN} \leq 20V$ $T_j = 25°C$	 ●	1.45 1.3	1.6 1.6	1.75 1.85	1.45 1.3	1.6 1.6	1.75 1.85	V V
	Enable Pin Current	$V_{EN} \leq 1V$ (See Note 3)		0		150	0		150	μA
		$V_{EN} \geq 2.4V$			0	1		0	1	μA

The ● denotes the specifications which apply over the full operating temperature range.

Note 1: Unless otherwise indicated, these specifications apply for $V_{IN} = 10V$, $I_O = 0mA$, and $T_J = 25°C$.

Note 2: Line and load regulation are measured using a low duty cycle pulse, causing little change in the junction temperature. Effects due to thermal gradients and device heating must be taken into account separately.

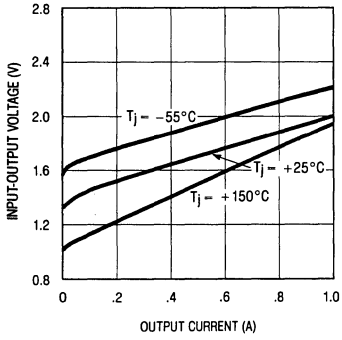
Note 3: When the enable pin is at a low logic level, current flows out of the enable pin.

Note 4: Pulse length for this measurement is 20msec.

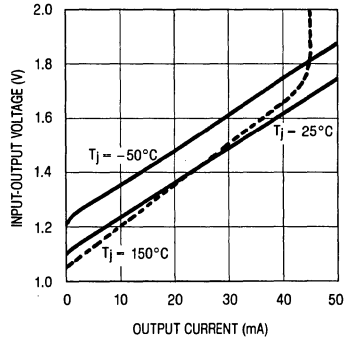
Note 5: Input Voltage is reduced until output drops by 100mV from its initial value.

TYPICAL PERFORMANCE CHARACTERISTICS

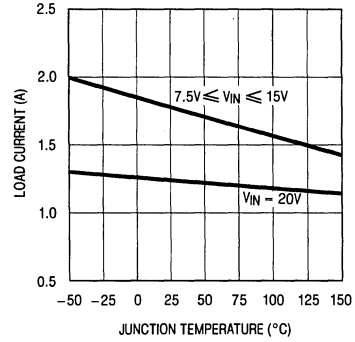
Minimum Input-Output Differential of Main Output



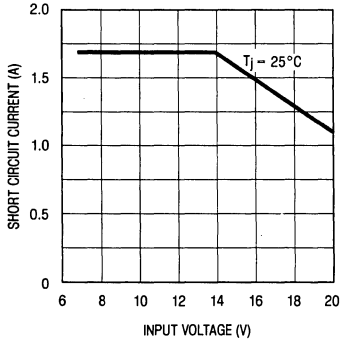
Minimum Input-Output Differential of Auxiliary Output



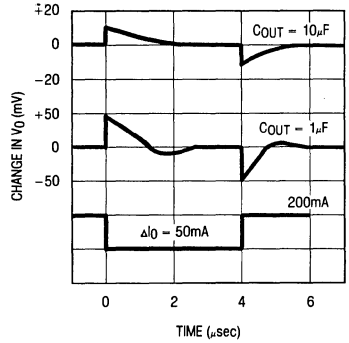
Maximum Available Load Current—Main Output



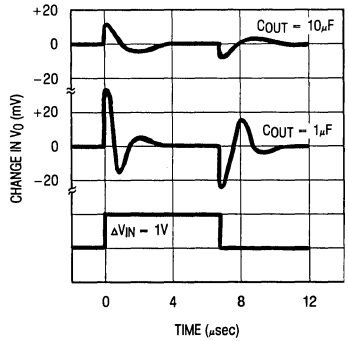
Short Circuit Output Current



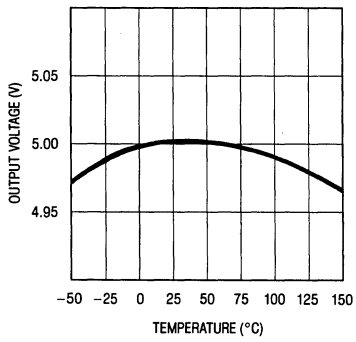
Load Transient Response of Main Output



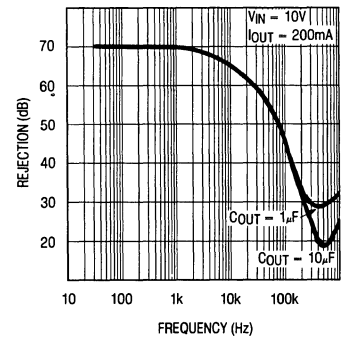
Line Transient Response of Main Output



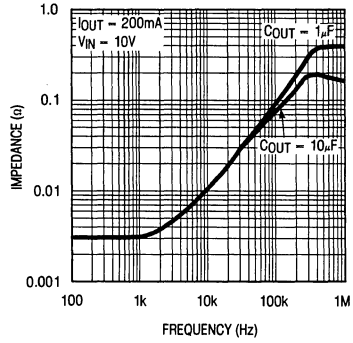
Output Voltage as Function of Temperature



Ripple Rejection

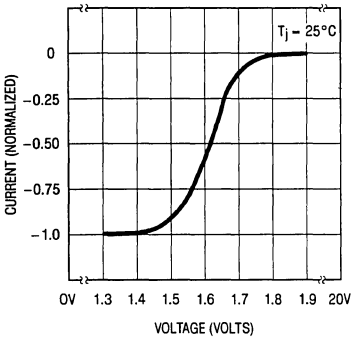


Output Impedance

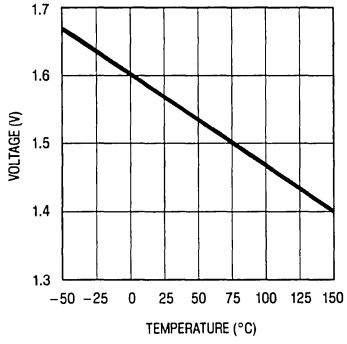


TYPICAL PERFORMANCE CHARACTERISTICS

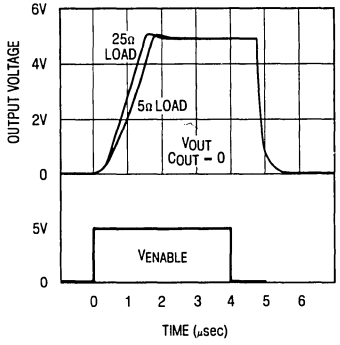
Enable Pin Characteristics



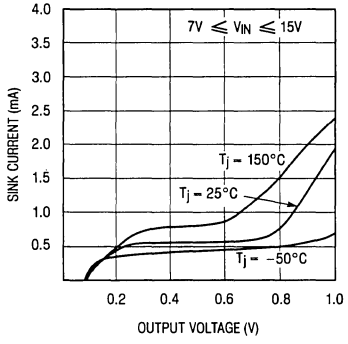
Enable Threshold



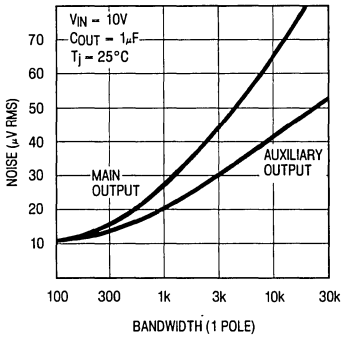
Switching Characteristics



Output Characteristics in Low State



Output Noise



APPLICATIONS INFORMATION

General Information

The LT1005 is a dual output 5V regulator. The main output is capable of delivering up to 1 amp of load current and can be shut down with a logic signal. The auxiliary output supplies a minimum of 35mA and is unaffected by the logic signal. The outputs are trimmed to ±2% initial tolerance and exhibit excellent line and load regulation.

The logic control feature makes the LT1005 ideal for many system applications where it is desirable to power up a portion of the system for a period of time and then power the system down during a standby operation. As an example, the LT1005 could be used to activate various memory space locations only as needed, thus saving substantial power dissipation and other cooling costs. The LT1005 could also be used to power micro-computers, such as the 8048 series. The auxiliary supply can be used for RAM keep-alive during power down operation. Additional power savings can be accomplished by using the LT1005 to power PROM, EPROM, and E^2PROM devices. During program load, or look-up table operations the ROM type device can be activated and its' contents placed in RAM, and then the ROM power can be removed. Or for high speed but low power data acquisition systems, the power could be applied to fast memory, then the data transferred to CMOS memory. The main regulator can then be shutdown and the CMOS memory can be powered by the auxiliary for lower power dissipation. Other applications, such as multiple power supply sequencing, elimination of expensive AC and DC power switches, delayed start applications, switching 5V DC loads, and many others are now easily accomplished.

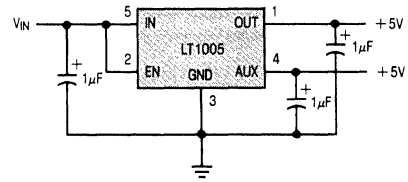
Timing functions can also be performed directly at the enable pin, such as delayed power-up or power-down.

Because a logic low on the enable pin shuts down the main regulator, feedback from output to enable can be used to generate hysterisis or latching functions.

The low quiescent current drain of the LT1005 makes it useful in battery powered or battery back-up applications. The enable pin can be used as a "low battery" detector or to shut down major portions of system power, allowing memory portions to continue to operate from the auxiliary output. At low output currents, the auxiliary output will regulate with input voltage typically as low as 6.1V, giving maximum battery life.

Good design practice with all regulators is to bypass the input and output terminals. A 1μF solid tantalum at the input and at both outputs is suggested. For the applications which follow, the bypass capacitors are still recommended, but are not shown on the diagram for simplicity. It is also recommended that for maximum noise immunity, the voltage enable pin be tied high if it is unused. It can be tied directly to V_{IN} as shown in Figure 1, or to the auxiliary output. If the enable pin is left open, it will float to a high logic level of approximately 1.6V and the main output regulator will be at 5V.

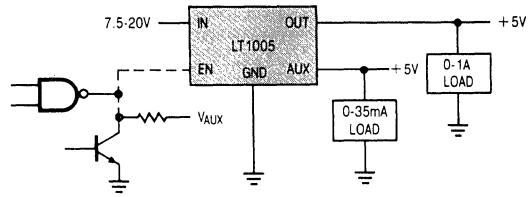
Figure 1.



The enable pin is fully protected against input voltages up to 20 volts, even if the power input voltage is zero.

The basic shutdown control circuit uses a direct gate drive or an open collector driver and a pull-up resistor which is tied to V_{AUX} as shown in Figure 2.

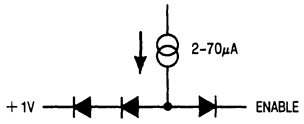
Figure 2.



Driving the Enable Pin

The enable pin equivalent schematic is shown in Fig. 3, with V/I characteristics shown in Fig. 4. Basically, enable pin current is zero above the threshold, and between 2 and 70μA below the threshold, flowing out of the pin. Standard logic, such as TTL & CMOS will interface directly to the enable pin, even if the logic output swing is higher than the input voltage (V_{IN}) to the regulator. 15V CMOS can be used to drive the enable pin even if the regulator is not powered up, without loading the CMOS output.

Figure 3.

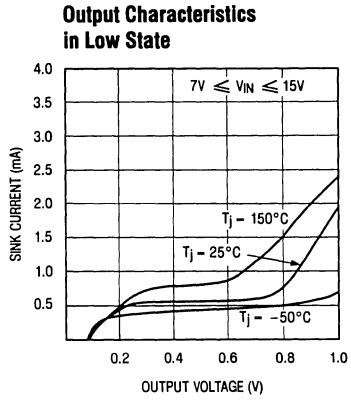


Timing functions, such as delayed power-up or power-down can be implemented by driving the enable pin with an RC network. The current flowing out of the enable pin should not be used as the timing current in delayed power up applications, as it is temperature sensitive and varies somewhat from device to device. Instead, a resistor tied to the auxiliary output, the input, or to a logic signal should be used. The timing resistor chosen should provide at least 500μA of current to "swamp-out" the effects of the internal current.

Main Output Current/Voltage Characteristics

Following a high to low transition at the enable pin, the main regulator output will begin to drop after a delay of approximately 1μsec. With no capacitive load, the output will fall to zero in approximately 0.5μsec (R_L = 5–100Ω). With a capacitive load, fall time is limited by the RC product of the load and the output capacitance. For light loads (R_L > 100Ω), the discharge time is controlled by an internal *equivalent* load of 200Ω for output voltages down to 1 volt. Below 1 volt, the output decays linearly, with a slope equivalent to the load capacitance and a pull down current of approximately 0.5mA. The DC output voltage in the shutdown mode is approximately 0.1 volt for input voltages (V_{IN}) up to 15V. If V_{IN} is 20V, the output during shutdown will be approximately 0.2V due to an internal current path in the regulator.

Figure 4.



The user should note that the output in the low state can only sink about 0.5mA. If current is forced into the output, the output voltage will rise to 0.8V at 1mA and above 1V at 10mA. With no output capacitor, the rise time of the main output is about 1.5μs. With an output capacitor, rise time is limited by the short circuit current of the LT1005 and the load capacitance; $t_r \approx (C)(5V)/(1.5A)$. A 1μF output capacitor slows the output rise time to approximately 3μs and a 10μF output capacitor slows the output rise time to 30μs.

Output Current

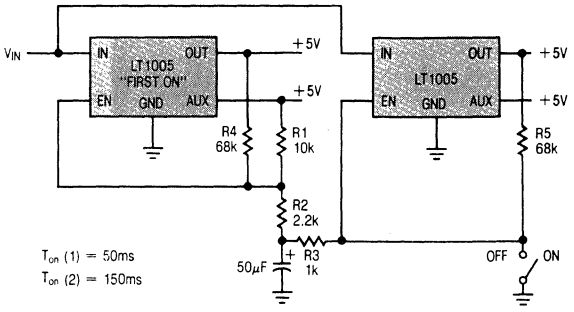
The main output current limits at about 1.7A for input voltages below 19V. Internal foldback, or "power limiting" circuitry detects the input-output voltage differential and reduces current limit for input to output voltages exceeding 14V. With 20V input, for instance, short circuit current is reduced to ≈ 1.1A.

An additional feature of the LT1005 is that the auxiliary supply does not incorporate nor is it affected by thermal shutdown. Any fault condition of the main regulator will not affect the auxiliary output voltage.

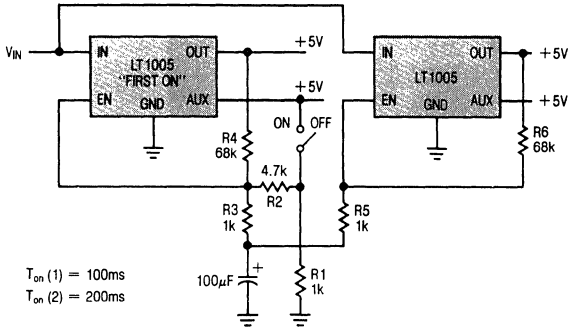
The following applications circuits will serve to indicate the versatility of the LT1005.

TYPICAL APPLICATIONS

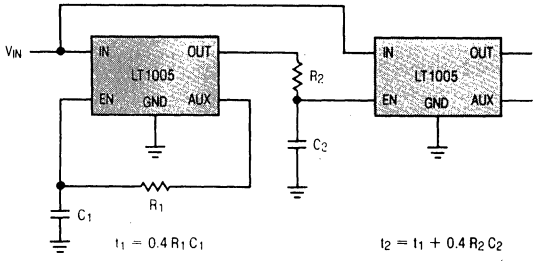
First-On, Last-Off Sequencing



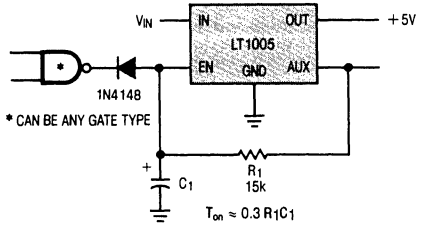
First-On, First-Off Sequencing



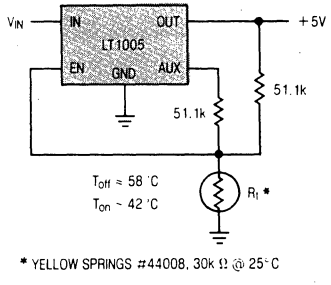
Power Supply Turn-On Sequencing



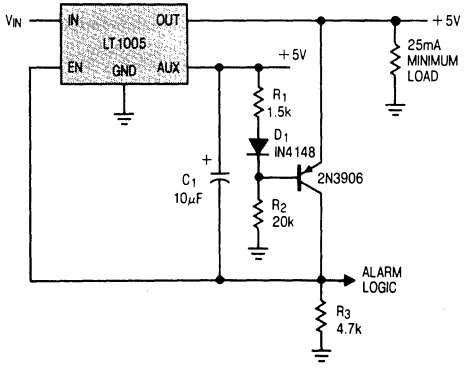
Fast Turn-Off, Delayed Turn-On



Thermal Cutoff at High Ambient Temperature

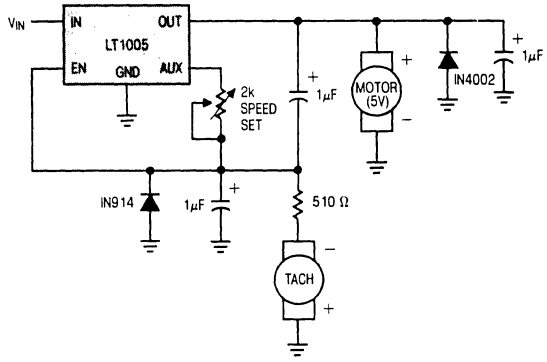


Latch-Off for $V_{OUT} \leq 4.7V$

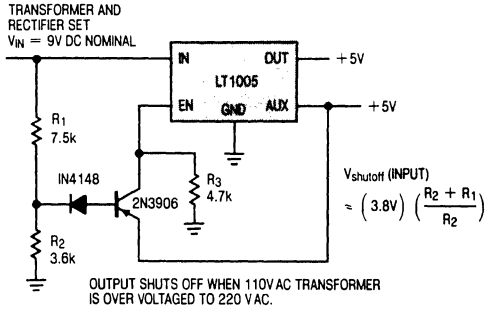


TYPICAL APPLICATIONS

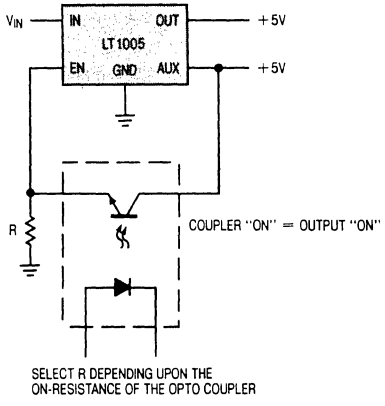
Proportional Motor Speed Controller



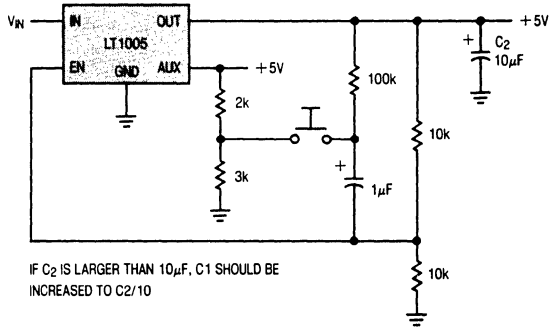
High Input Voltage Detection



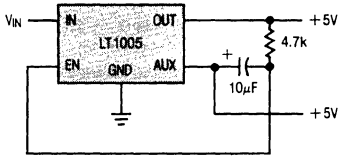
Opto-Coupled Output Control



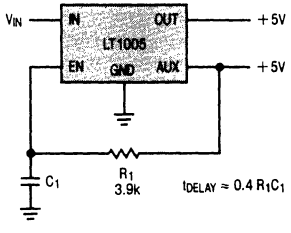
Push-On, Push-Off



Latch-Off When Output Short

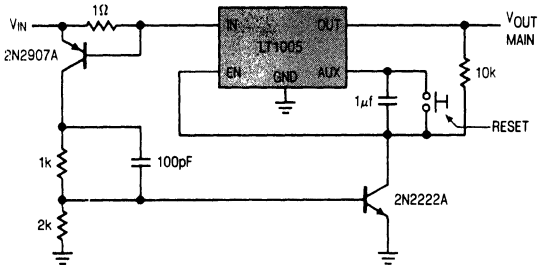


Delayed Power Up

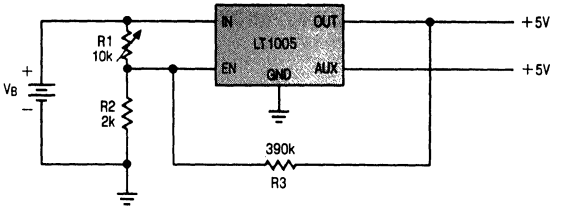


TYPICAL APPLICATIONS

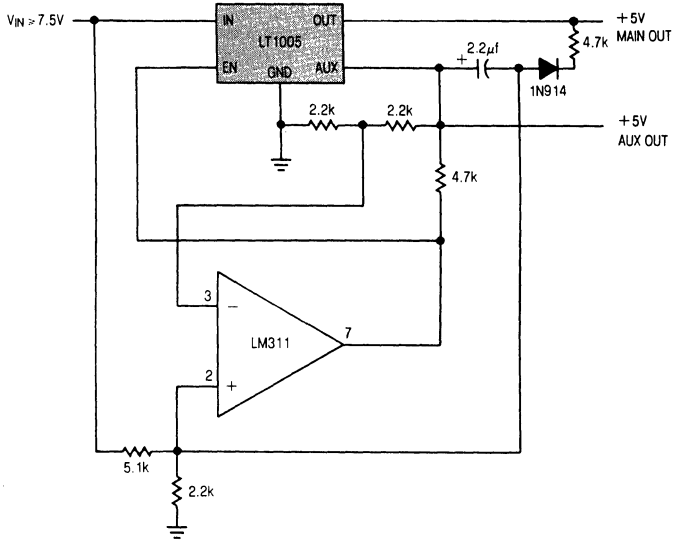
Fast Electronic Circuit Breaker



Battery Voltage Sensing Circuit



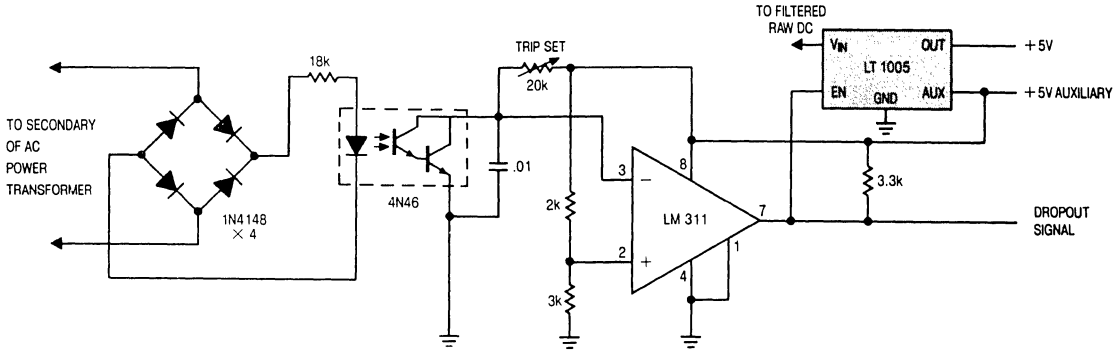
Memory Save-on-Power-Down



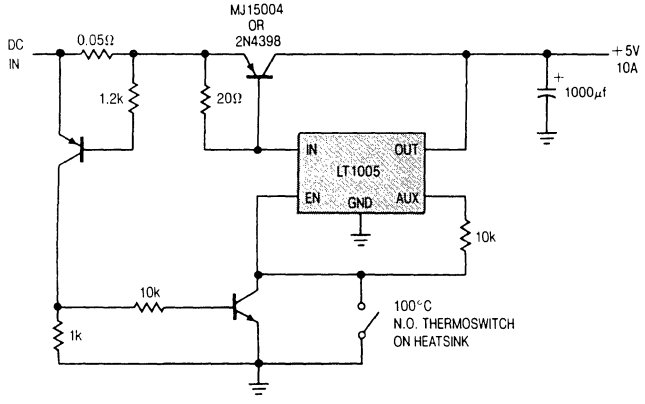
The auxiliary output powers the memory, while the main output powers the system and is connected to the memory store pin. When power goes down, the main output goes low, commanding the memory to store. The auxiliary output then drops out.

TYPICAL APPLICATIONS

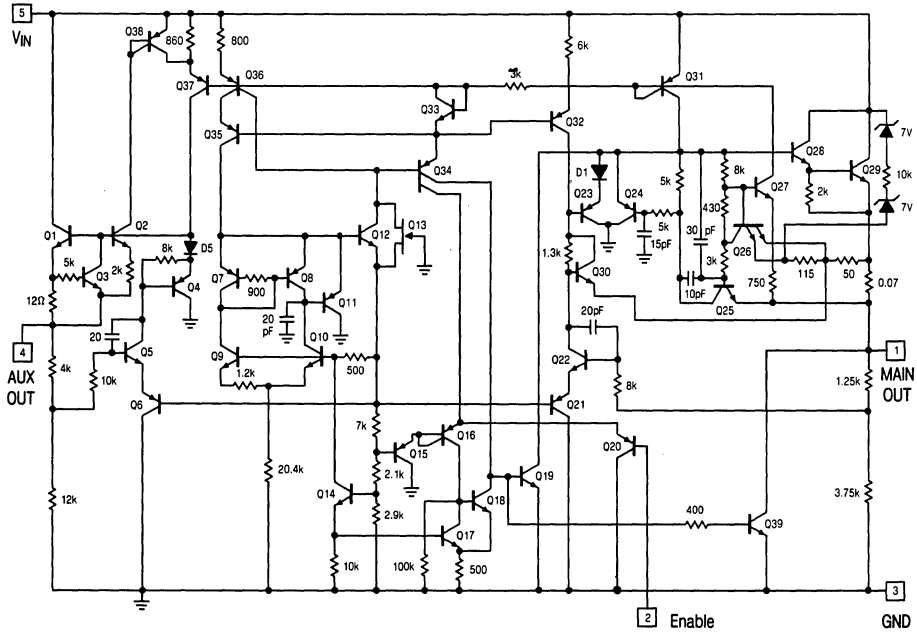
Line Dropout Detector



10 Amp Regulator with Current and Thermal Protection

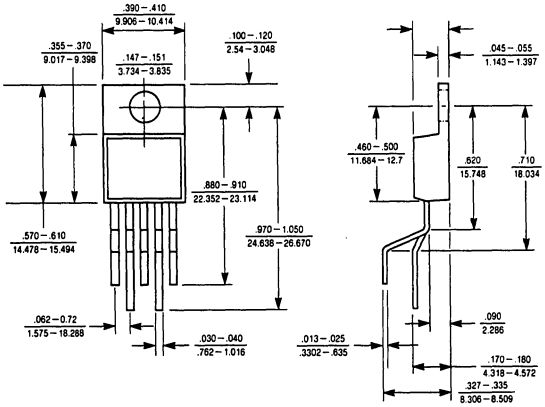


SCHEMATIC DIAGRAM



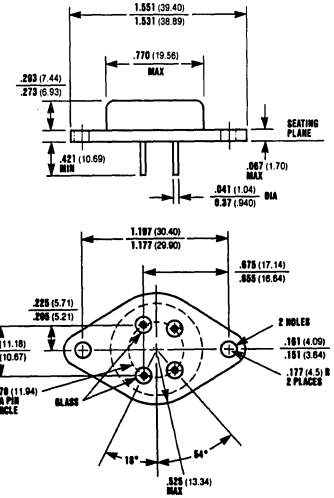
PACKAGE DESCRIPTION

TO-220 PACKAGE (5 LEAD)



	T_{JMAX}	Θ_{JC}
LT1005C	125°C	5°C/W

4-Pin Metal Package Similar to JEDEC TO-3



All dimensions in inches **bold** and millimeters (parentheses)

	T_{JMAX}	Θ_{JC}
LT1005M	150°C	4°C/W
LT1005C	125°C	4°C/W

3A. Negative Adjustable Regulator

FEATURES

- *Guaranteed* 1% Initial Voltage Tolerance
- *Guaranteed* 0.015%/V Line Regulation
- *Guaranteed* 0.02%/W Thermal Regulation
- 100% Burn-in in Thermal Limit

APPLICATIONS

- Adjustable Power Supplies
- System Power Supplies
- Precision Voltage/Current Regulators
- On-Card Regulators

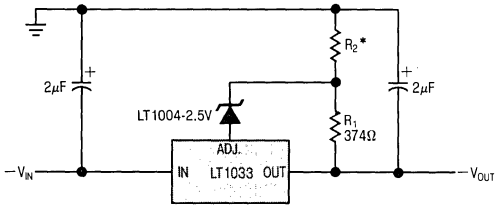
DESCRIPTION

The LT1033 negative adjustable regulator will deliver up to 3 Amps output current over an output voltage range of −1.2V to −32V. Linear Technology has made significant improvements in these regulators compared to previous devices, such as better line and load regulation, and a maximum output voltage error of 1%.

The LT1033 is easy to use and difficult to damage. Internal current and power limiting as well as true thermal limiting prevents device damage due to overloads or shorts, even if the regulator is not fastened to a heat sink.

Maximum reliability is attained with Linear Technology's advanced processing techniques combined with a 100% burn-in in the thermal limit mode. This assures that all device protection circuits are working and eliminates field failures experienced with other regulators that receive only standard electrical testing.

Precision Regulator †



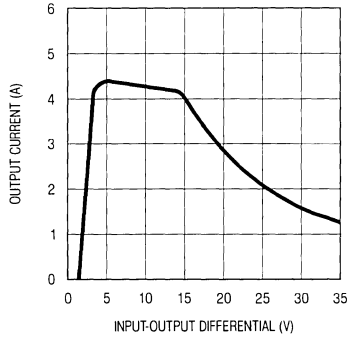
IMPROVED LINE & LOAD REGULATION **

* $R_2 = \frac{R_1}{3.75}(V_{OUT} - 3.75)$

** REGULATION IS IMPROVED BY $\frac{V_{OUT}}{1.25}$

† EXTERNAL LT1004 REFERENCE IMPROVES LINE, LOAD, AND THERMAL REGULATION

Current Limit



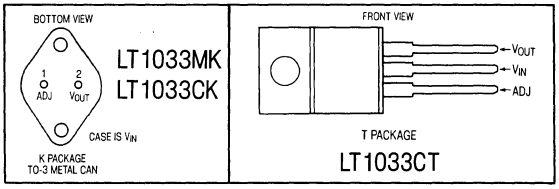
ABSOLUTE MAXIMUM RATINGS

Power Dissipation ..... Internally Limited
Input to Output Voltage Differential 35V
Operating Junction Temperature Range
LT1033M ..... −55°C to 150°C
LT1033C ..... 0°C to 125°C
Storage Temperature Range
LT1033M ..... −65°C to 150°C
LT1033C ..... −65°C to 150°C
Lead Temperature (Soldering, 10 sec.)..... 300°C

PRECONDITIONING

100% THERMAL LIMIT BURN-IN

PACKAGE/ORDER INFORMATION



ELECTRICAL CHARACTERISTICS (See Note 1)

SYMBOL	PARAMETER	CONDITIONS		LT1033M MIN	LT1033M TYP	LT1033M MAX	LT1033C MIN	LT1033C TYP	LT1033C MAX	UNITS
V_{REF}	Reference Voltage	$\lvert V_{IN}-V_{OUT}\rvert = 5V$, $I_{OUT} = 5mA$, $T_j = 25°C$		−1.238	−1.250	−1.262	−1.238	−1.250	−1.262	V
		$3V \leq \lvert V_{IN} - V_{OUT}\rvert \leq 35V$ $5mA \leq I_{OUT} \leq I_{MAX}$, $P \leq P_{MAX}$	●	−1.215	−1.250	−1.285	−1.200	−1.250	−1.300	V
$\frac{\Delta V_{OUT}}{\Delta I_{OUT}}$	Load Regulation	$10mA \leq I_{OUT} \leq I_{MAX}$, (See Note 2)								
		$T_j = 25°C$, $\lvert V_{OUT}\rvert \leq 5V$			10	50		10	50	mV
		$T_j = 25°C$, $\lvert V_{OUT}\rvert \geq 5V$			0.2	1.0		0.2	1.0	%
		$\lvert V_{OUT}\rvert \leq 5V$	●		20	75		20	75	mV
		$\lvert V_{OUT}\rvert \geq 5V$	●		0.4	1.5		0.4	1.5	%
$\frac{\Delta V_{OUT}}{\Delta V_{IN}}$	Line Regulation	$3V \leq \lvert V_{IN}-V_{OUT}\rvert \leq 35V$, (See Note 2) $T_j = 25°C$			0.005	0.015		0.01	0.02	%/V
			●		0.01	0.04		0.02	0.05	%/V
	Ripple Rejection	$V_{OUT} = -10V$, f = 120Hz $C_{ADJ} = 0$		56	66			60		dB
		$C_{ADJ} = 10\mu F$		70	80		66	77		dB
	Thermal Regulation	$T_j = 25°C$, 10msec Pulse			0.002	0.02		0.002	0.02	%/W
I_{ADJ}	Adjust Pin Current		●		65	100		65	100	μA
ΔI_{ADJ}	Adjust Pin Current Change	$10mA \leq I_{OUT} \leq I_{MAX}$	●		0.2	2		0.5	2	μA
		$3V \leq \lvert V_{IN}-V_{OUT}\rvert \leq 35V$	●		1.0	5		2	5	μA
	Minimum Load Current	$\lvert V_{IN}-V_{OUT}\rvert \leq 35V$			2.5	5.0		2.5	5.0	mA
		$\lvert V_{IN}-V_{OUT}\rvert \leq 10V$			1.2	3.0		1.2	3.0	mA
I_{SC}	Current Limit	$\lvert V_{IN}-V_{OUT}\rvert \leq 10V$, (See Note 2) $\lvert V_{IN}-V_{OUT}\rvert = 35V$,		3	4.3	6	3	4.3	6	A
		$T_j = 25°C$		0.5	1.3	2.5	.5	1.3	2.5	A
$\frac{\Delta V_{OUT}}{\Delta Temp}$	Temperature Stability of Output Voltage	$T_{MIN} \leq T \leq T_{MAX}$	●		0.6	1.5		0.6	1.5	%
$\frac{\Delta V_{OUT}}{\Delta Time}$	Long Term Stability	$T_A = 125°C$, 1000 Hours			0.3	1.0		0.3	1.0	%
e_n	RMS Output Noise (% of V_{OUT})	$T_A = 25°C$, 10Hz ≤ f ≤ 10kHz			0.003			0.003		%
Θ_{JC}	Thermal Resistance Junction to Case	T Package						4		°C/W
		K Package			1.2	2.0		1.2	2.0	°C/W

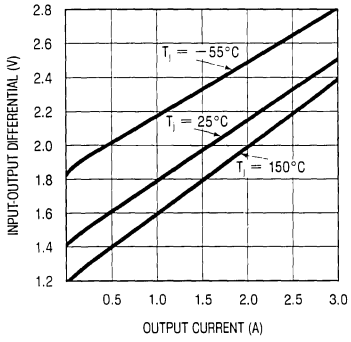
The ● denotes the specifications which apply over the full operating temperature range. Otherwise $T_j = 25°C$.

Note 1: Unless otherwise indicated, these specifications apply: $\lvert V_{IN} - V_{OUT}\rvert = 5V$; and $I_{OUT} = 5mA$. Power dissipation is internally limited. However, these specifications apply for power dissipation up to 30W. See guaranteed minimum output current curve. $I_{MAX} = 3A$.

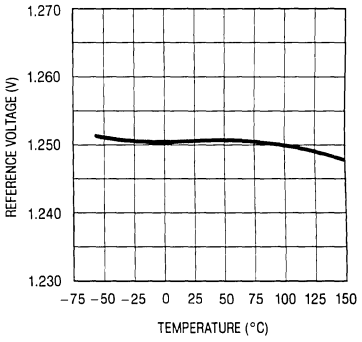
Note 2: Testing is done using a pulsed low duty cycle technique. See thermal regulation specifications for output changes due to heating effects. Load regulation is measured on the output pin at a point 1/8" below the base of the package.

TYPICAL PERFORMANCE CHARACTERISTICS

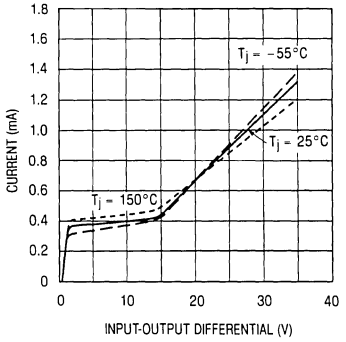
Dropout Voltage



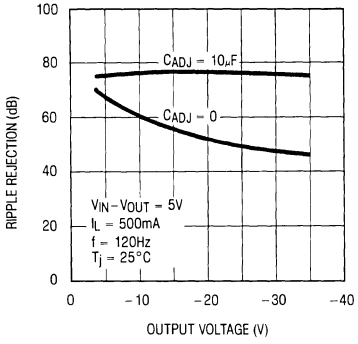
Temperature Stability



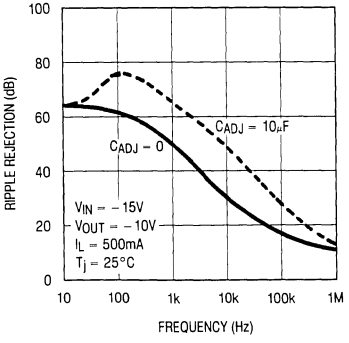
Minimum Load Current



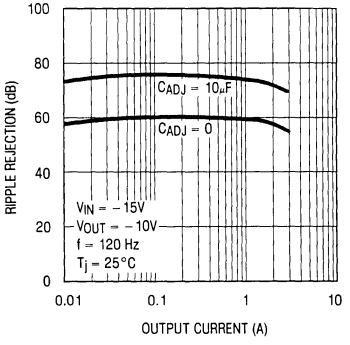
Ripple Rejection



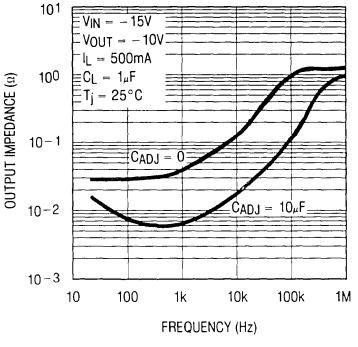
Ripple Rejection



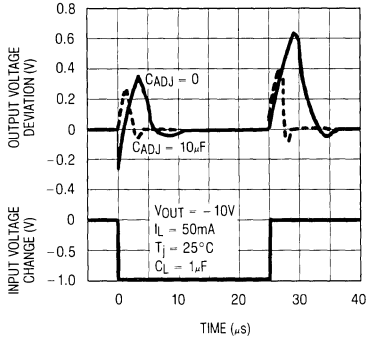
Ripple Rejection



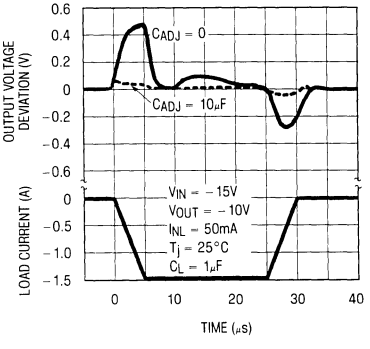
Output Impedance



Line Transient Response

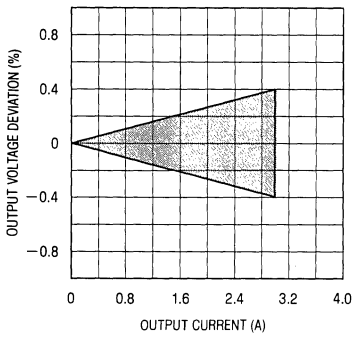


Load Transient Response



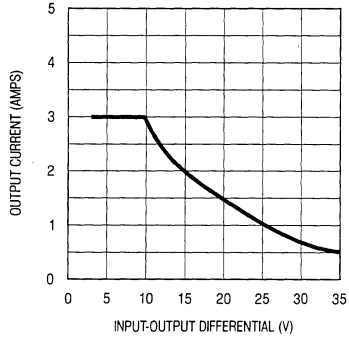
TYPICAL PERFORMANCE CHARACTERISTICS

Load Regulation*

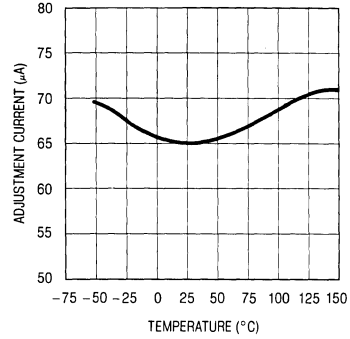


* The LT1033 has load regulation compensation which makes the typical unit read close to zero. This band represents the typical production spread.

Guaranteed Minimum Output Current



Adjustment Current



APPLICATION INFORMATION

Output Voltage: The output voltage is determined by two external resistors, R_1 & R_2 (see Figure 1). The exact formula for the output voltage is:

$$V_{OUT} = V_{Ref}\left(1 + \frac{R_2}{R_1}\right) + I_{ADJ}(R_2)$$

Where: V_{Ref} = Reference Voltage, I_{ADJ} = Adjustment Pin Current. In most applications, the second term is small enough to be ignored, typically about 0.5% of V_{OUT}. In more critical applications, the exact formula should be used, with I_{ADJ} equal to 65μA. Solving for R_2 yields:

$$R_2 = \frac{V_{OUT} - V_{Ref}}{\frac{V_{Ref}}{R_1} - I_{ADJ}}$$

Smaller values of R_1 and R_2 will reduce the influence of I_{ADJ} on the output voltage, but the no-load current drain on the regulator will be increased. Typical values for R_1 are between 100Ω and 300Ω, giving 12.5mA and 4.2mA no-load current respectively. There is an additional consideration in selecting R_1, the minimum load current specification of the regulator. The operating current of the LT1033 flows from input to output. If this current is not absorbed by the load, the output of the regulator will rise above the regulated value. The current drawn by R_1 and R_2 is normally high enough to absorb the current, but care must be taken in no-load situations where R_1 and R_2 have high values. The maximum value for the operating current, which must be absorbed, is 5mA for the LT1033. If input-output voltage differential is less than 10V, the operating current that must be absorbed drops to 3mA.

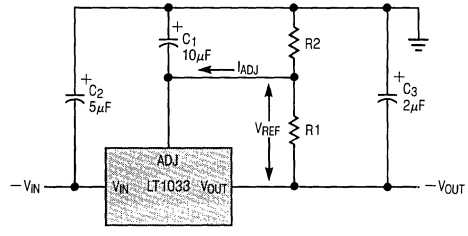


Figure 1

EXAMPLE:

1. A precision 10V regulator to supply up to 3 Amp load current.

   a. Select R_1 = 100Ω to minimize effect of I_{ADJ}

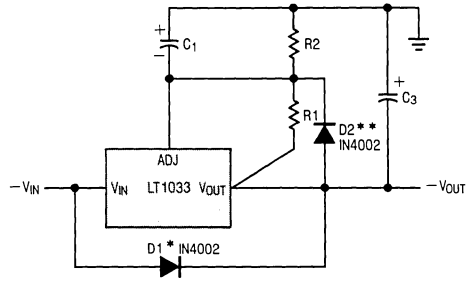
   b. Calculate $R_2 = \frac{V_{OUT} - V_{Ref}}{\frac{V_{Ref}}{R_1} - I_{ADJ}} = \frac{10V - 1.25V}{\frac{1.25V}{100\Omega} - 65\mu A} = 704\Omega$

APPLICATION INFORMATION

Capacitors and Protection Diodes: An output capacitor, C3, is required to provide proper frequency compensation of the regulator feedback loop. A 2μF or larger solid tantalum capacitor is generally sufficient for this purpose if the 1MHz impedance of the capacitor is 1Ω or less. High Q capacitors, such as Mylar, are not recommended because they tend to reduce the phase margin at light load currents. Aluminum electrolytic capacitors may also be used, but the minimum value should be 25μF to ensure a low impedance at 1MHz. The output capacitor should be located within a few inches of the regulator to keep lead impedance to a minimum. The following caution should be noted: if the output voltage is greater than 6V and an output capacitor greater than 20μF has been used, it is possible to damage the regulator if the input voltage becomes shorted, due to the output capacitor discharging into the regulator. This can be prevented by using diode DI (see Figure 2) between the input and the output.

The input capacitor, C2, is only required if the regulator is more than 4 inches from the raw supply filter capacitor.

Bypassing the Adjustment Pin: The adjustment pin of the LT1033 may be bypassed with a capacitor to ground, C1, to reduce output ripple, noise, and impedance. These parameters scale directly with output voltage if the adjustment pin is not bypassed. A bypass capacitor reduces ripple, noise, and impedance to that of a 1.25V regulator. In a 15V regulator for example, these parameters are improved by 15V/1.25V = 12 to 1. This improvement holds only for those frequencies where the impedance of the bypass capacitor is less than R_1. Ten microfarads is generally sufficient for 60Hz power line applications where the ripple frequency is 120Hz, since X_C = 130Ω. The capacitor should have a voltage rating at least as high as the output voltage of the regulator. Values larger than 10μF may be used, but if the output is larger than 25V, a diode, D2, should be added between the output and adjustment pins (see Figure 2).



* D1 protects the regulator from input shorts to ground. It is required only when C3 is larger than 20μF and V_{OUT} is larger than 6V.

** D2 protects the adjust pin of the regulator from output shorts if C2 is larger than 10μF *and* V_{OUT} is larger than −25V.

Figure 2

Proper Connection of Divider Resistors: The LT1033 has a load regulation specification of 0.8% and is measured at a point 1/8" from the bottom of the package. To prevent degradation of load regulation, the resistors which set output voltage, R1 and R2, must be connected as shown in Figure 3. Note that the positive side of the load has a true force and sense (Kelvin) connection, but the negative side of the load does not.

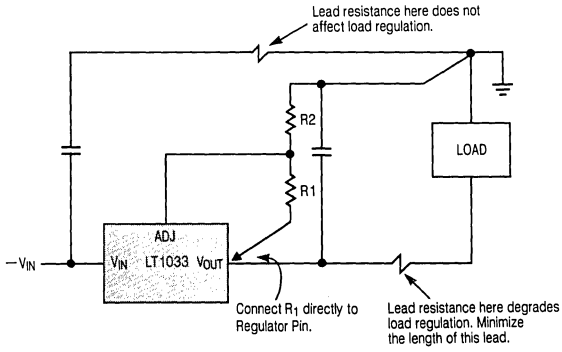


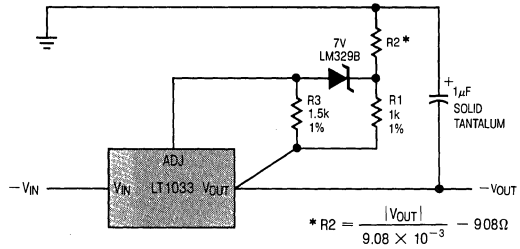
Figure 3

R1 should be connected *directly* to the output lead of the regulator, as close as possible to the specified point 1/8" from the case. R2 should be connected to the positive side of the load separately from the positive (ground) connection to the raw supply. With this arrangement, load regulation is degraded only by the resistance between the regulator output pin and the load. If R1 is connected to the load, regulation will be degraded.

TYPICAL APPLICATIONS

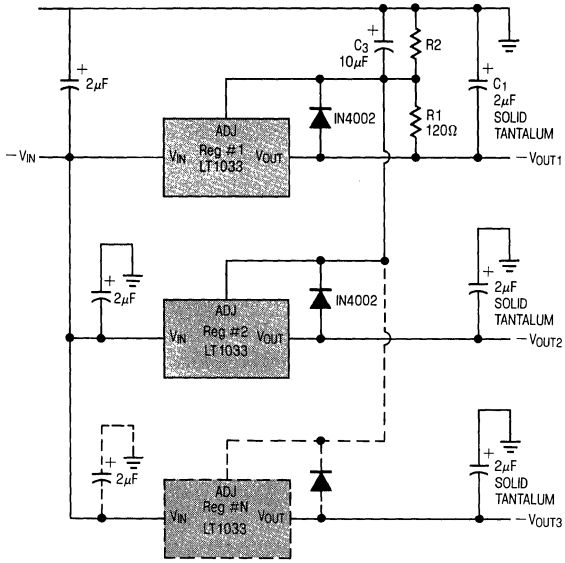
The output stability, load regulation, line regulation, thermal regulation, temperature drift, long term drift, and noise, can be improved by a factor of 6.6 over the standard regulator configuration. This assumes a zener whose drift and noise is considerably better than the regulator itself. The LM329B has 20PPM/°C maximum drift and about 10 times lower noise than the regulator.

High Stability Regulator

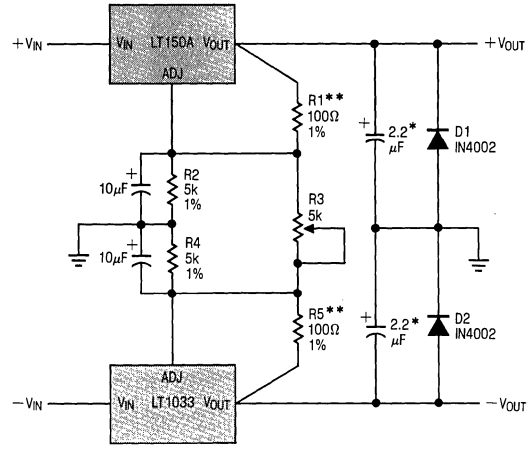


In the application shown below, regulators #2 to "N" will track regulator #1 to within ±24mV initially, and to ±60mV over all load, line, and temperature conditions. If any regulator output is shorted to ground, all other outputs will drop to ≈ –2V. Load regulation of regulators 2 to "N" will be improved by $V_{OUT}/1.25V$ compared to a standard regulator, so regulator #1 should be the one which has the lowest load current.

Multiple Tracking Regulators



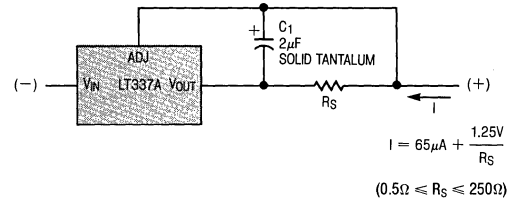
Dual Tracking 3A Supply ± 1.25V to ± 20V



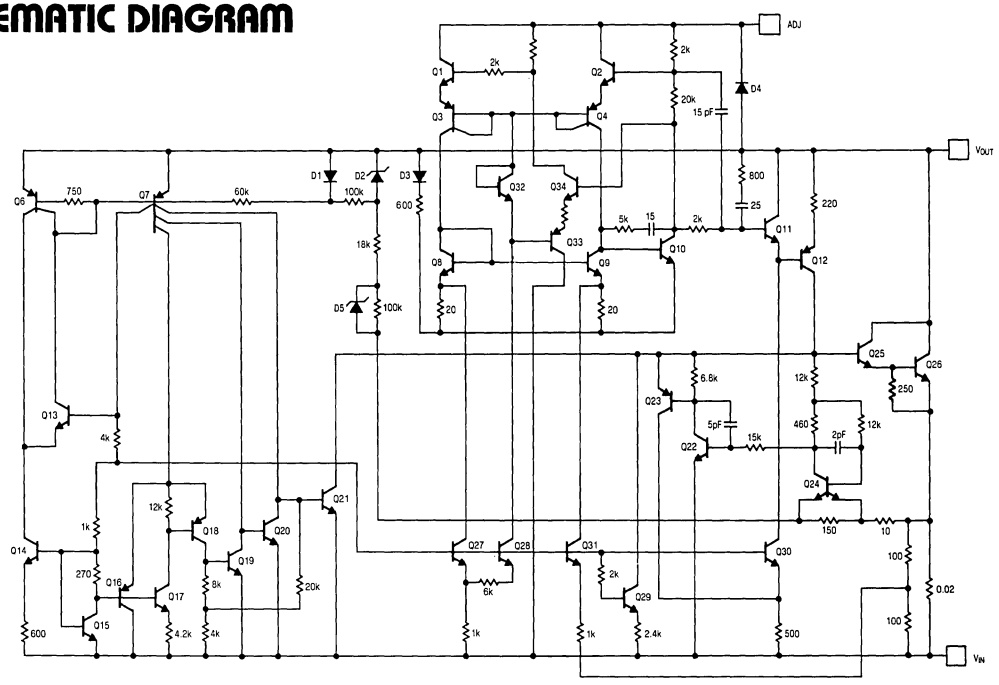
* Solid Tantalum

** R_1 or R_5 may be trimmed slightly to improve tracking

Current Regulator



SCHEMATIC DIAGRAM

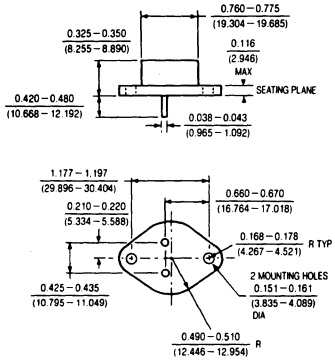


The following table allows convenient selection of program resistors from standard 1% values.

V_{OUT}	R_1	R_2	OUTPUT ERROR (%)
5	100	301	0.6
6	121	453	−0.7
8	115	619	0.6
10	115	806	0.6
12	118	1020	1
15	100	1100	0.5
18	150	2000	0.2
20	121	1820	0.8
22	130	2150	0.2
24	121	2210	0.9
28	115	2430	−0.7
30	121	2740	−0.9

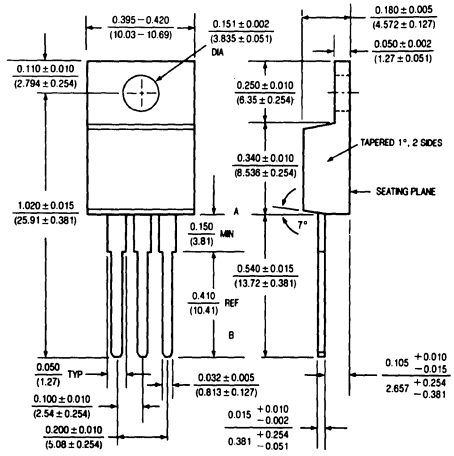
PACKAGE DESCRIPTION

K Package TO-3 STEEL Metal Can



	$T_{J\,MAX}$	Θ_{JC}
LT1033M	150°C	2°C/W
LT1033C	125°C	2°C/W

T Package TO-220 Plastic



	$T_{J\,MAX}$	Θ_{JC}
LT1033C	125°C	4°C/W

FEATURES

- Two Regulated Outputs
  - +5V at 3A
  - +5V at 75mA
- 2% Output Voltage Tolerance
- 66dB Ripple Rejection
- 0.7% Load Regulation
- TTL and CMOS Compatible Logic Control
- 100% Thermal Burn-In on All Devices

APPLICATIONS

- Power Supply Sequencing
- Remote On/Off Power Control
- Selective System Power during Emergency Power Operation
- Memory Power Supply with Back-Up

DESCRIPTION

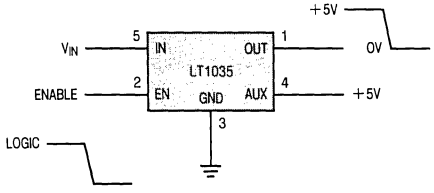
The LT1035 features two positive 5V regulators in the same package. The main regulator offers excellent performance while supplying load currents up to 3A, and the auxiliary regulator provides similar performance while supplying lighter loads of 75mA. The main regulator has the additional feature of being under the shutdown control of a logic signal. When the enable pin is taken to a low logic level, the main regulator shuts down and its output voltage goes to near 0V. During this command, the auxiliary output is unaffected by the main regulator's condition and continues to provide a 5V output.

The main output has current and power limiting combined with thermal shutdown to make it virtually blowout proof. The auxiliary output is not affected by the thermal shutdown mechanism or the state of the main output, allowing it to be used as a back-up in case of overloads or shorts on the main supply.

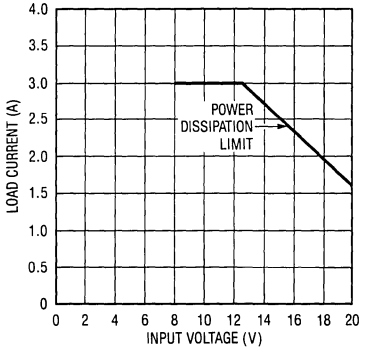
The logic input of the LT1035 (enable pin) has a 1.6V threshold and can be driven from a high source impedance. This allows it to be driven by most logic families, including TTL and CMOS.

For a 1A version of the LT1035, please see the LT1005 data sheet. For a 12V output voltage version, consult the factory.

Functional Diagram



Guaranteed Load Current



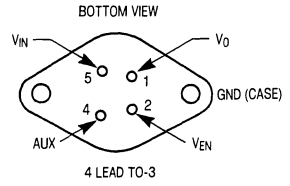
ABSOLUTE MAXIMUM RATINGS

Power Dissipation—Continuous 24W
Power Dissipation—Fault Conditions . . . Internally Limited
Input Voltage (V_{IN}) 20V
Enable Voltage (V_{EN}) 20V
Operating Junction Temperature
LT1035M . . . . . −55°C to 150°C
LT1035C . . . . . 0°C to 125°C
Storage . . . . . −65°C to 150°C
Lead Temperature (Soldering, 10 sec.) . . . . . 300°C

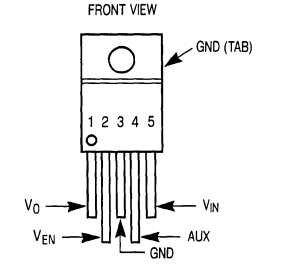
PRECONDITIONING

100% Burn-In in Thermal Limit

PACKAGE/ORDER INFORMATION



4 LEAD TO-3



5 LEAD TO-220

ORDER PART NUMBER
LT1035MK LT1035CK
LT1035CT

ELECTRICAL CHARACTERISTICS **Main Regulator (See Note 1)**

SYMBOL	PARAMETER	CONDITIONS		LT1035M MIN	LT1035M TYP	LT1035M MAX	LT1035C MIN	LT1035C TYP	LT1035C MAX	UNITS
V_O	Output Voltage	$T_j = 25°C$		4.9	5.0	5.1	4.9	5.0	5.1	V
	High	$7.7V \le V_{IN} \le 20V$ $P_D \le 24W$ $0mA \le I_O \le 3A$	●	4.8	5.0	5.2	4.8	5.0	5.2	V
	Low	$7V \le V_{IN} \le 12.5V$	●		0.1	0.2		0.1	0.2	V
		$V_{IN} = 20V$	●		0.1	0.3		0.1	0.3	V
$\frac{\Delta V_O}{\Delta I_O}$	Load Regulation (Note 6)	$8V \le V_{IN} \le 12.5V$ $0 \le I_O \le 3A$ (Note 2)	●		10	35		10	35	mV
$\frac{\Delta V_O}{\Delta V_{IN}}$	Line Regulation	$7.4V \le V_{IN} \le 20V$ (Note 2)			0.3	2		0.3	2	mV/V
	Ripple Rejection	$50Hz \le f \le 500Hz$		60	70		60	70		dB
	Thermal Regulation	$\Delta P_D = 20W$ (Note 4)			0.003	0.012		0.003	0.012	%/W
I_O	Available Load Current (Note 6)	$8V \le V_{IN} \le 12.5V$	●	3	4		3	4		A
		$V_{IN} = 20V$	●	1.6	2.4		1.6	2.4		A
I_{SC}	Short Circuit Current	$V_{IN} = 8V$			4	6		4	6	A
		$V_{IN} = 20V$			2.5	4		2.5	4	A
V_{IN}	Minimum Input Voltage to Maintain Regulation	(Note 5) $I_O = 1A$	●	7.2	6.7		7.2	6.7		V
		$I_O = 3A$	●	7.7	7.2		7.7	7.2		V
I_Q	Quiescent Current	Output High			3	5		3	5	mA
		Output Low			2	4		2	4	mA
Θ_{JC}	Thermal Resistance, Junction to Case	TO-3			1.5	2.5		1.5	2.5	°C/W
		TO-220						2	3	°C/W

ELECTRICAL CHARACTERISTICS Auxiliary Regulator (See Note 1)

SYMBOL	PARAMETER	CONDITIONS		LT1035M MIN	LT1035M TYP	LT1035M MAX	LT1035C MIN	LT1035C TYP	LT1035C MAX	UNITS
V_O	Output Voltage	$T_j = 25°C$		4.9	5.0	5.1	4.9	5.0	5.1	V
		$7.2V \le V_{IN} \le 20V$ $0mA \le I_O \le 75mA$	●	4.8	5.0	5.2	4.8	5.0	5.2	V
$\frac{\Delta V_O}{\Delta I_O}$	Load Regulation	$7.2V \le V_{IN} \le 20V$ $0mA \le I_O \le 75mA$ (Note 2)	●		5	15		5	15	mV
$\frac{\Delta V_O}{\Delta V_{IN}}$	Line Regulation	$7.2V \le V_{IN} \le 20V$ (Note 2)	 ●		0.2	1 2		0.2	1 2	mV/V mV/V
	Ripple Rejection	$50Hz \le f \le 500Hz$			74			74		dB
I_{SC}	Short Circuit Current	$7.0V \le V_{IN} = 20V$			140	250		140	250	mA
V_{IN}	Minimum Input Voltage to Maintain Regulation	(Note 5) $I_O \le 10mA$ $I_O = 75mA$	 ● ●	 6.5 7.2	 6.2 6.8		 6.5 7.2	 6.2 6.8		 V V

ELECTRICAL CHARACTERISTICS Logic Control (See Note 1)

SYMBOL	PARAMETER	CONDITIONS		LT1035M MIN	LT1035M TYP	LT1035M MAX	LT1035C MIN	LT1035C TYP	LT1035C MAX	UNITS
V_{EN}	Enable Threshold Voltage	$7.0V \le V_{IN} \le 20V$ $T_j = 25°C$	 ●	1.45 1.3	1.6 1.6	1.7 1.8	1.45 1.3	1.6 1.6	1.7 1.8	V V
	Enable Pin Current	$V_{EN} \le 1V$ (Note 3)		0	1.5	6	0	1.5	6	μA
		$V_{EN} \ge 2.4V$			0	1		0	1	μA

The ● denotes the specifications which apply over the full operating temperature range.

Note 1: Unless otherwise indicated, these specifications apply for $V_{IN} = 10V$, $I_O = 0mA$, and $T_j = 25°C$.

Note 2: Line and load regulation is measured using a low duty cycle pulse, causing little change in the junction temperature. Effects due to thermal gradients and device heating must be taken into account separately.

Note 3: When the enable pin is at a low logic level, current flows out of the enable pin.

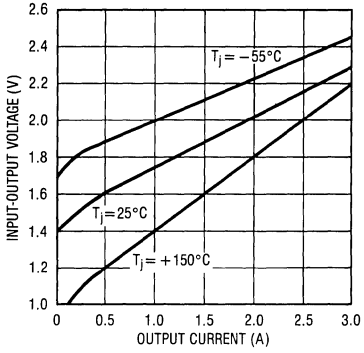
Note 4: Pulse length for this measurement is 20ms.

Note 5: Input voltage is reduced until output drops by 100mV from its initial value.

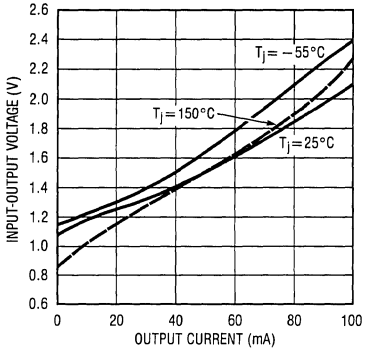
Note 6: See "Guaranteed Load Current" graph.

TYPICAL PERFORMANCE CHARACTERISTICS

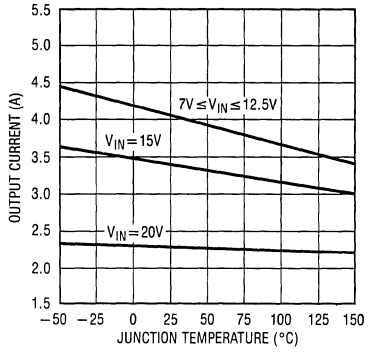
Minimum Input-Output Differential of Main Output



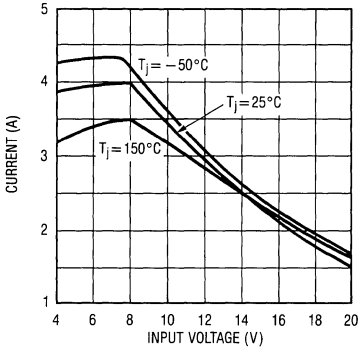
Minimum Input-Output Differential of Auxiliary Output



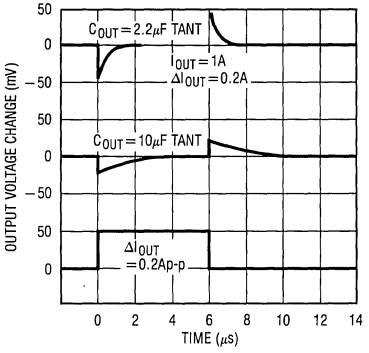
Maximum Available Load Current—Main Output



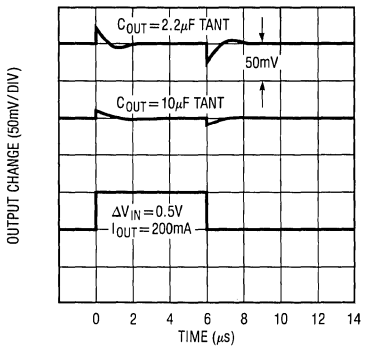
Short Circuit Output Current



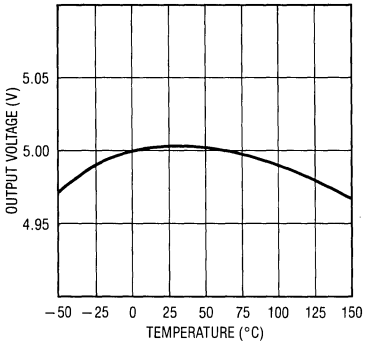
Load Transient Response



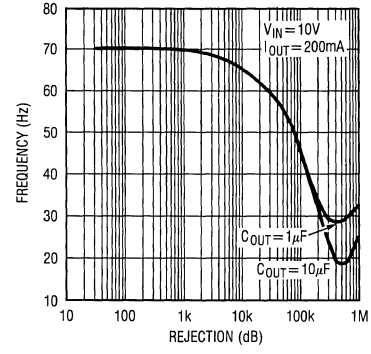
Line Transient Response



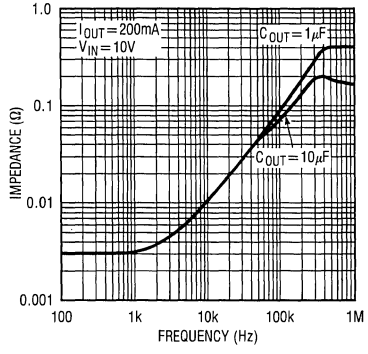
Output Voltage as Function of Temperature



Ripple Rejection

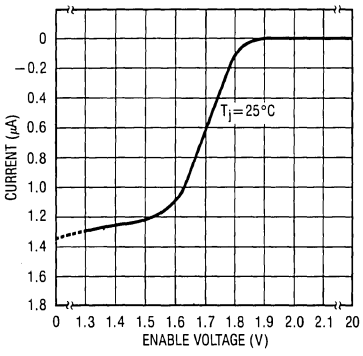


Output Impedance

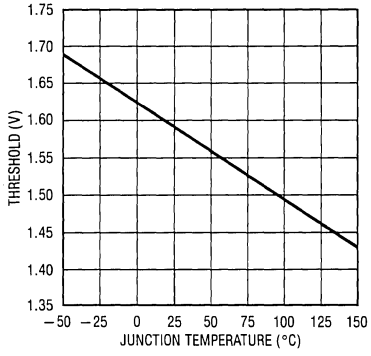


TYPICAL PERFORMANCE CHARACTERISTICS

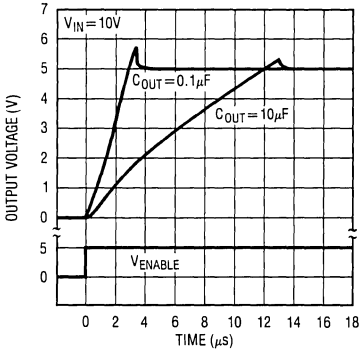
Enable Pin Characteristics



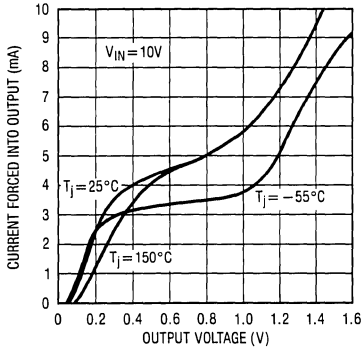
Enable Threshold



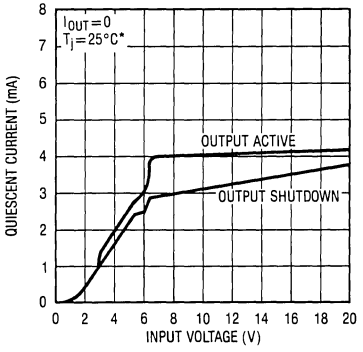
Output Switching Characteristics



Output Characteristics in Low State

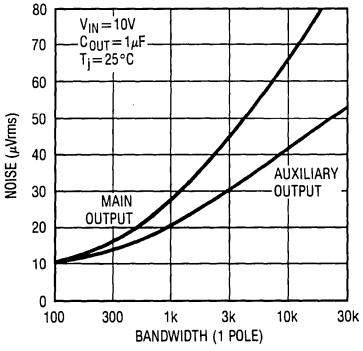


Quiescent Current



*I_Q IS NEARLY INDEPENDENT OF TEMPERATURE

Output Noise



APPLICATIONS INFORMATION

General Information

The LT1035 is a dual output 5V regulator. The main output is capable of delivering up to 3A of load current and can be shut down with a logic signal. The auxiliary output supplies a minimum of 75mA and is unaffected by the logic signal. The outputs are trimmed to ± 2% initial tolerance and exhibit excellent line and load regulation.

The logic control feature makes the LT1035 ideal for many system applications where it is desirable to power-up a portion of the system for a period of time, and then power the system down during a standby operation. As an example, the LT1035 could be used to activate various memory space locations only as needed, thus saving substantial power dissipation and other cooling costs. The LT1035 could also be used to power microcomputers such as the 8048 series. The auxiliary supply can be used for RAM keep-alive during power-down operation. Additional power savings can be accomplished by using the LT1035 to power PROM, EPROM, and E²PROM devices. During program load or look-up table operations, the ROM type device can be activated and its contents placed in RAM, and then the ROM power can be removed. Or for high speed but low power data acquisition systems, the power could be applied to fast memory, then the data transferred to CMOS memory. The main regulator can then be shut down and the CMOS memory can be powered by the auxiliary for lower power dissipation. Other applications such as multiple power supply sequencing, elimination of expensive AC and DC power switches, delayed start applications, switching 5V DC loads, and many others are now easily accomplished.

Timing functions, such as delayed power-up or power-down, can also be performed directly at the enable pin.

Because a logic low on the enable pin shuts down the main regulator, feedback from output to enable can be used to generate hysteresis or latching functions.

The low quiescent current drain of the LT1035 makes it useful in battery-powered or battery back-up applications. The enable pin can be used as a "low battery" detector or to shut down major portions of system power, allowing memory portions to continue to operate from the auxiliary output. At low output currents, the auxiliary output will regulate with input voltage typically as low as 6.1V, giving maximum battery life.

Good design practice with all regulators is to bypass the input and output terminals. A 2μF solid tantalum at the input and at both outputs is suggested. For the applications which follow, the bypass capacitors are still recommended, but for simplicity are not shown on the diagram. It is also recommended that for maximum noise immunity the voltage enable pin be tied high if it is unused. It can be tied directly to V_{IN}, as shown in Figure 1, or to the auxiliary output. If the enable pin is left open, it will float to a high logic level of approximately 1.6V and the main output regulator will be at 5V.

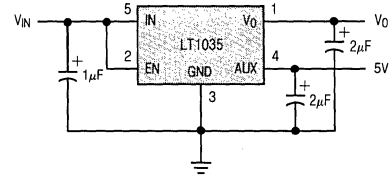


Figure 1

The enable pin is fully protected against input voltages up to 20V, even if the power input voltage is zero.

The basic shutdown control circuit uses a direct gate drive or an open collector driver and a pull-up resistor which are tied to V_{AUX}, as shown in Figure 2.

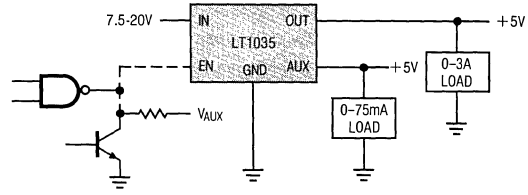


Figure 2

APPLICATIONS INFORMATION

Driving the Enable Pin

The enable pin equivalent schematic is shown in Figure 3. Basically, enable pin current is zero above the threshold and about 1.5μA below the threshold, flowing out of the pin. Standard logic, such as TTL and CMOS, will interface directly to the enable pin, even if the logic output swing is higher than the input voltage (V_{IN}) to the regulator. 15V CMOS can be used to drive the enable pin, even if the regulator is not powered up, without loading the CMOS output.

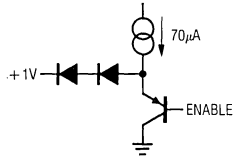


Figure 3

Timing functions, such as delayed power-up or power-down, can be implemented by driving the enable pin with an RC network. The current flowing out of the enable pin should not be used as the timing current in delayed power-up applications as it is temperature sensitive and varies somewhat from device to device. Instead, a resistor tied to the auxiliary output, the input, or to a logic signal should be used. The timing resistor chosen should provide at least 25μA of current to "swamp out" the effects of the internal current.

Main Output Current/Voltage Characteristics

Following a high to low transition at the enable pin, the main regulator output will begin to drop after a delay of approximately 0.4μs. With no capacitive load, the output will fall to zero in approximately 0.8μs ($R_L = 2\Omega$–100Ω). With a capacitive load, fall time is limited by the RC product of the load and the output capacitance. For light loads ($R_L > 400\Omega$), the discharge time is controlled by an internal current pull-down of 15mA for output voltages down to 1.5V. Below 1.5V, the pull-down current drops to ≈4mA. The DC output voltage in the shutdown mode is approximately 0.07V for input voltages (V_{IN}) up to 12V. If V_{IN} is 20V, the output during shutdown will be approximately 0.15V due to an internal current path in the regulator.

Output Characteristics in Low State

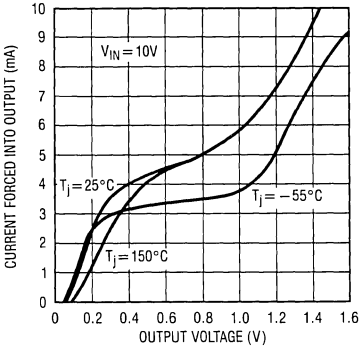


Figure 4

The user should note that the output in the low state can only sink about 3mA. If current is forced into the output, the output voltage will rise to 1V at 5mA and about 1.5V at 10mA. With no output capacitor, the rise time of the main output is about 3μs. With an output capacitor, rise time is limited by the short circuit current of the LT1035 and the load capacitance; $t_r \approx (C)\ (5V)/4A$. A 10μF output capacitor slows the output rise time to approximately 12μs.

Output Current

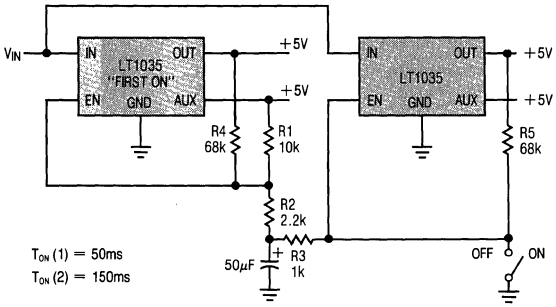
The main output current limits at about 4A for input voltages below 12.5V. Internal foldback, or "power limiting", circuitry detects the input-output voltage differential and reduces current limit for input to output voltages exceeding 7.5V. With 20V input, for instance, short circuit current is reduced to ≈2.4A.

An additional feature of the LT1035 is that the auxiliary supply does not incorporate, nor is it affected by, thermal shutdown. Any fault condition of the main regulator will not affect the auxiliary output voltage.

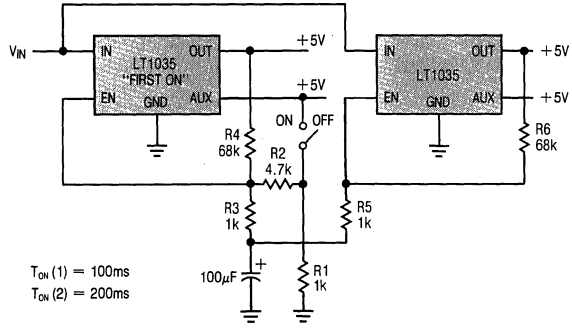
The following applications circuits will serve to indicate the versatility of the LT1035.

TYPICAL APPLICATIONS

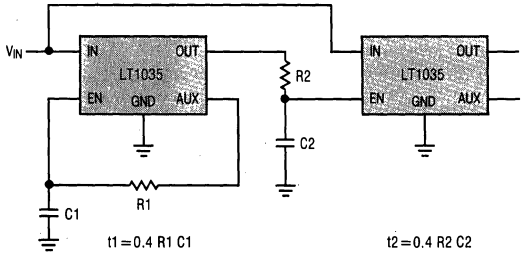
First-On, Last-Off Sequencing



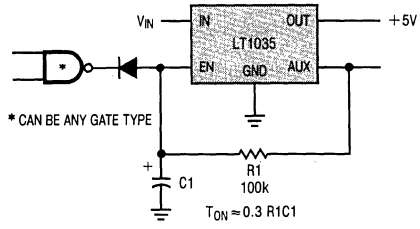
First-On, First-Off Sequencing



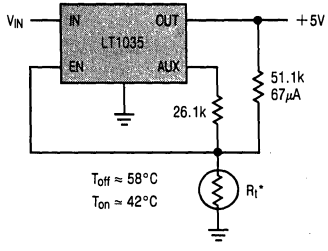
Power Supply Turn-On Sequencing



Fast Turn-Off, Delayed Turn-On

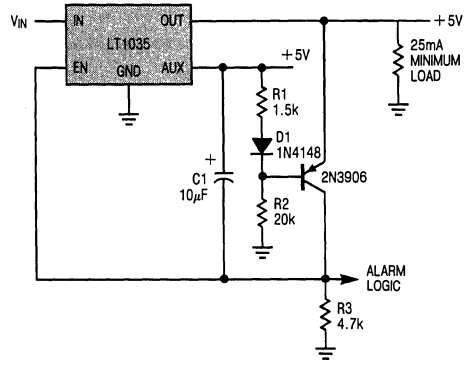


Thermal Cutoff at High Ambient Temperature



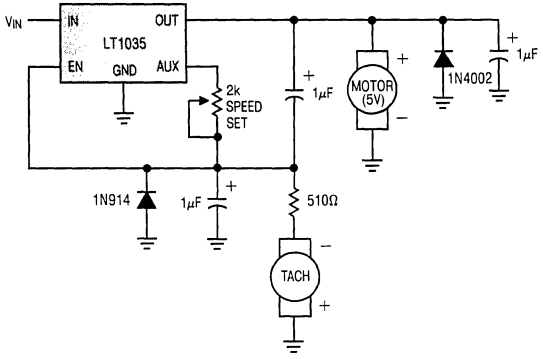
*YELLOW SPRINGS #44008, 30kΩ @ 25°C

Latch-Off for $V_{OUT} \leq 4.7V$

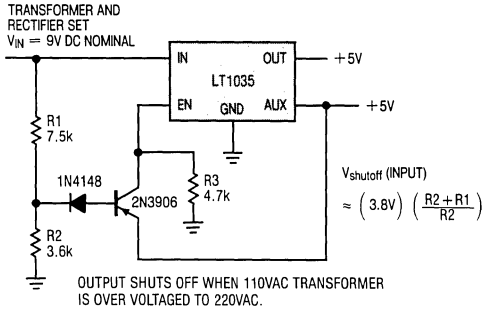


TYPICAL APPLICATIONS

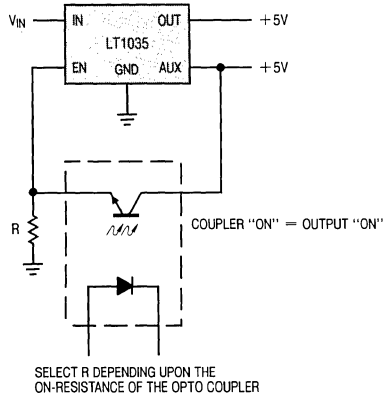
Proportional Motor Speed Controller



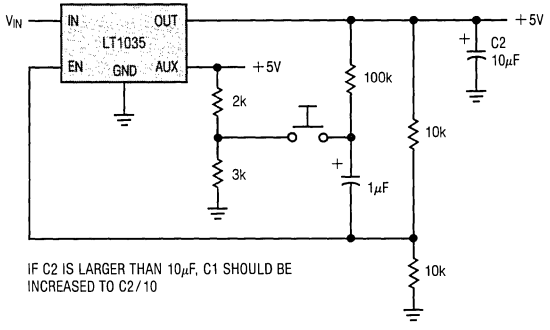
High Input Voltage Detection



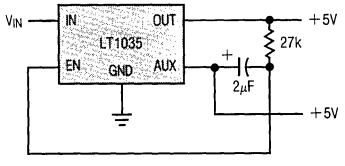
Opto-Coupled Output Control



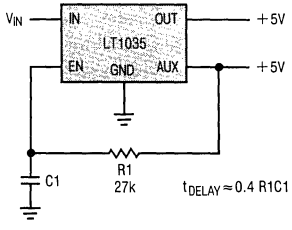
Push-On, Push-Off



Latch-Off when Output Short

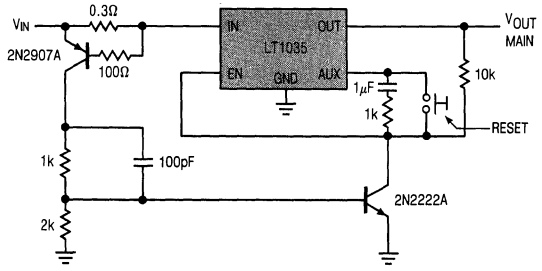


Delayed Power-Up

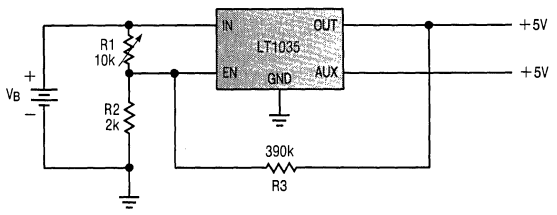


TYPICAL APPLICATIONS

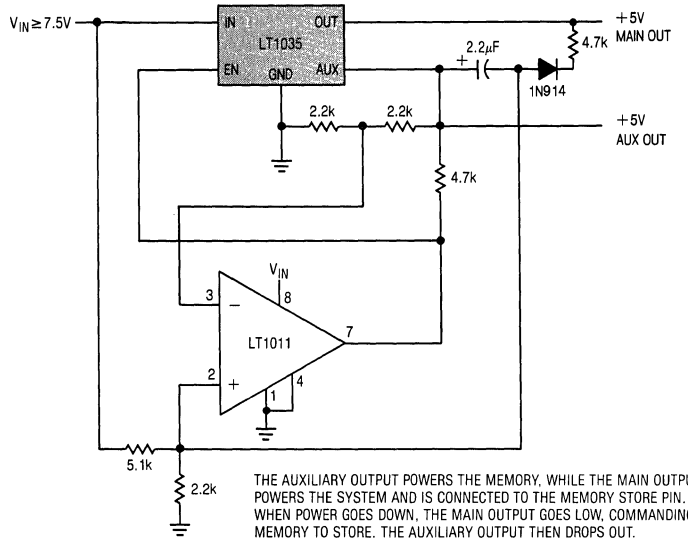
Fast Electronic Circuit Breaker



Battery Voltage Sensing Circuit

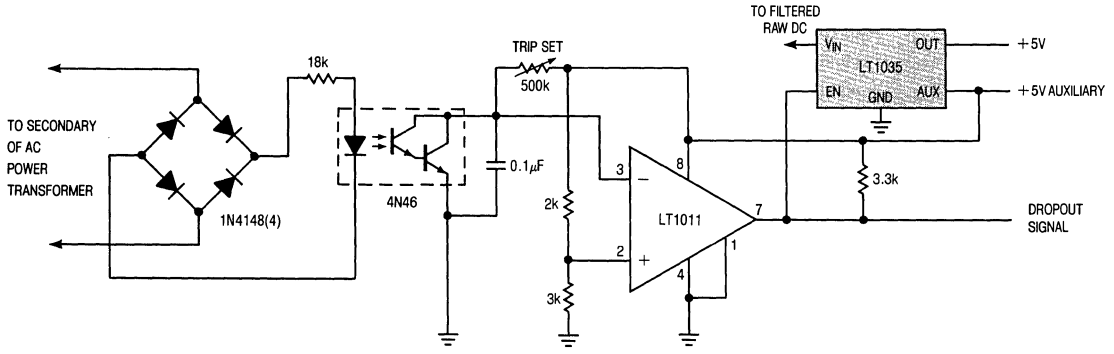


Memory Save on Power-Down



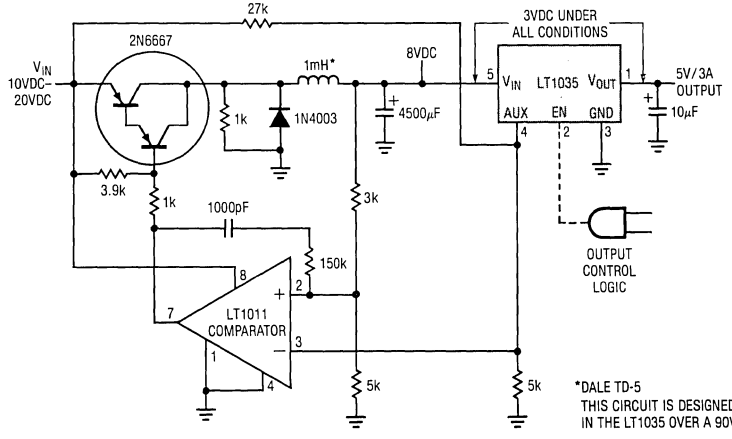
THE AUXILIARY OUTPUT POWERS THE MEMORY, WHILE THE MAIN OUTPUT POWERS THE SYSTEM AND IS CONNECTED TO THE MEMORY STORE PIN. WHEN POWER GOES DOWN, THE MAIN OUTPUT GOES LOW, COMMANDING THE MEMORY TO STORE. THE AUXILIARY OUTPUT THEN DROPS OUT.

Line Dropout Detector



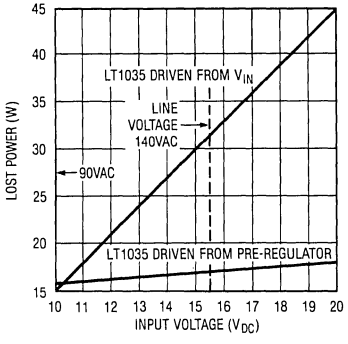
TYPICAL APPLICATIONS

Low Dissipation Regulator

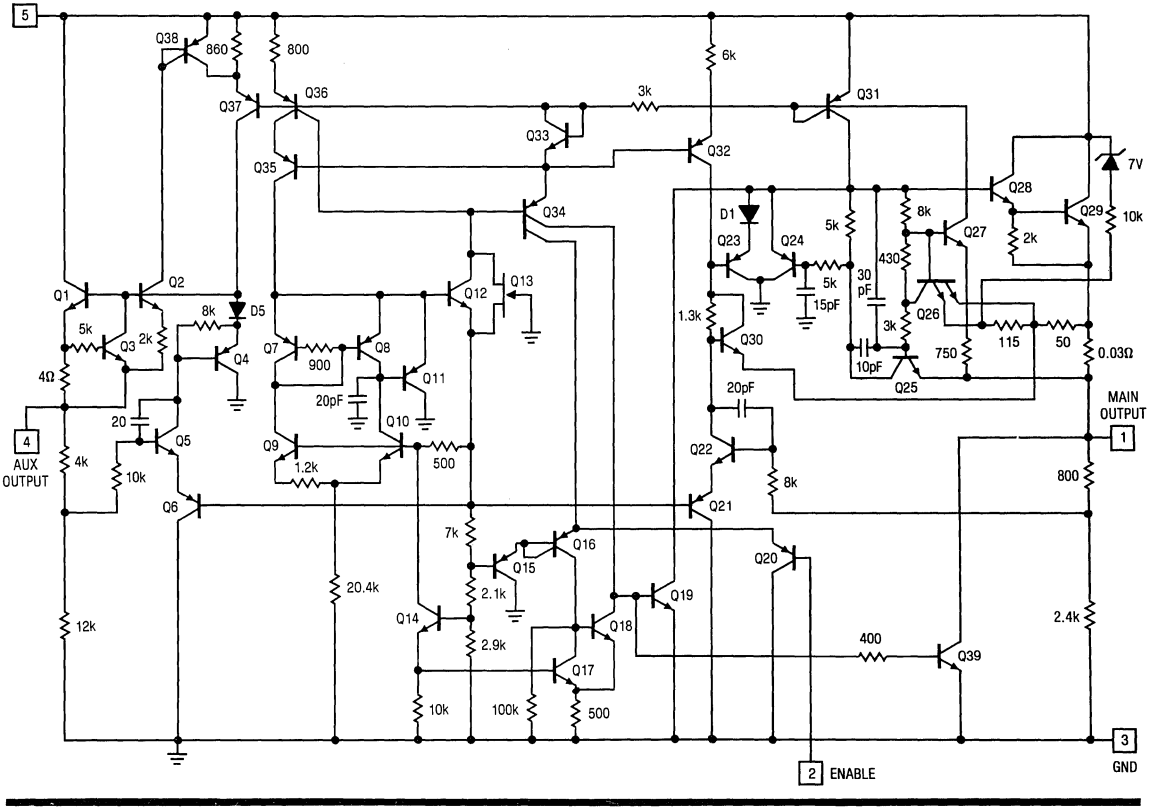


*DALE TD-5
THIS CIRCUIT IS DESIGNED TO REDUCE POWER DISSIPATION IN THE LT1035 OVER A 90VAC–140VAC INPUT RANGE.

Regulator Losses at $I_{OUT} = 3A$

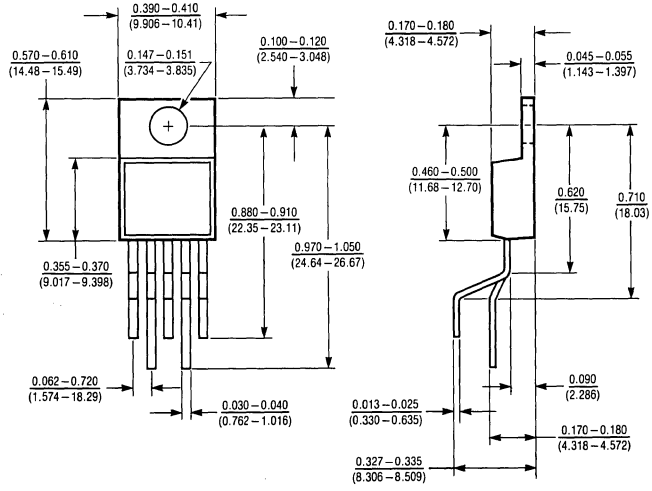


SCHEMATIC DIAGRAM



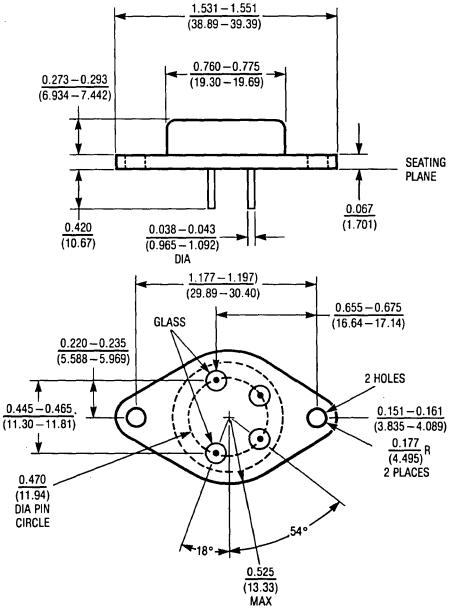
PACKAGE DESCRIPTION

TO-220 Package (5 Lead)



	T_{jMAX}	Θ_{jC}
LT1035C	125°C	3°C/W

4-Pin Metal Package Similar to JEDEC TO-3



	T_{jMAX}	Θ_{jC}
LT1035M	150°C	2.5°C/W
LT1035C	125°C	2.5°C/W

Logic Controlled Regulator

FEATURES

- Two Regulated Outputs
  - + 12V at 3A
  - + 5V at 75mA
- 2% Output Voltage Tolerance
- 60dB Ripple Rejection
- 0.7% Load Regulation
- TTL and CMOS Compatible Logic Control
- 100% Thermal Burn-In on All Devices

APPLICATIONS

- Power Supply Sequencing
- Remote On/Off Power Control
- Selective System Power during Emergency Power Operation
- Power Supply with Back-Up

DESCRIPTION

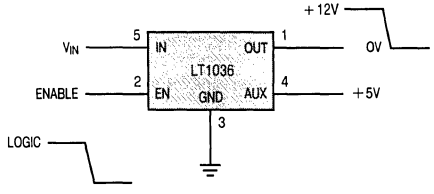
The LT1036 features two positive regulators in the same package. The 12V main regulator offers excellent performance while supplying load currents up to 3A, and the 5V auxiliary regulator provides similar performance while supplying lighter loads of 75mA. The main regulator has the additional feature of being under the shutdown control of a logic signal. When the enable pin is taken to a low logic level, the main regulator shuts down and its output voltage goes to near 0V. During this command, the auxiliary output is unaffected by the main regulator's condition and continues to provide a 5V output.

The main output has current and power limiting combined with thermal shutdown to make it virtually blowout proof. The auxiliary output is not affected by the thermal shutdown mechanism or the state of the main output, allowing it to be used as a back-up in case of overloads or shorts on the main supply.

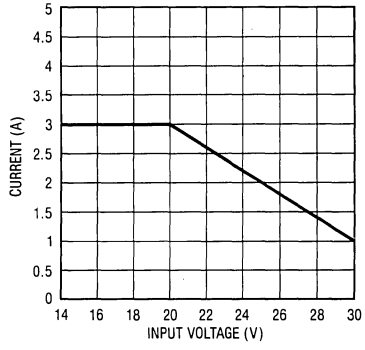
The logic input of the LT1036 (enable pin) has a 1.6V threshold and can be driven from a high source impedance. This allows it to be driven by most logic families, including TTL and CMOS.

For a dual 5V version of the LT1036, please see the LT1035 data sheet.

Functional Diagram



Guaranteed Load Current, 12V Output



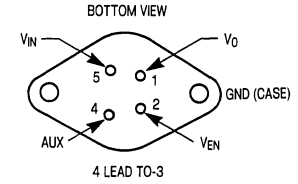
ABSOLUTE MAXIMUM RATINGS

Power Dissipation—Continuous (Note 6) 24W
Power Dissipation—Fault Conditions .. Internally Limited
Input Voltage (V_{IN}) 30V
Enable Voltage (V_{EN}) 30V
Operating Junction Temperature
LT1036M ..... −55°C to 150°C
LT1036C ..... 0°C to 125°C
Storage ..... −65°C to 150°C
Lead Temperature (Soldering, 10 sec.) ..... 300°C

PRECONDITIONING

100% Burn-In in Thermal Limit

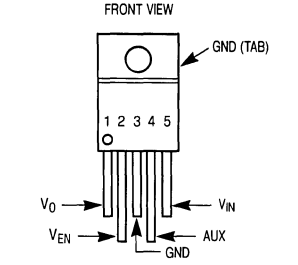
PACKAGE/ORDER INFORMATION



4 LEAD TO-3

ORDER PART NUMBER

LT1036MK
LT1036CK



5 LEAD TO-220

LT1036CT

ELECTRICAL CHARACTERISTICS

Main Regulator (See Note 1) V_{IN} = 15V unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS		LT1036M/C MIN	TYP	MAX	UNITS
V_O	Output Voltage	T_j = 25°C		11.76	12	12.24	V
	High	15V ≤ V_{IN} ≤ 30V $I_{OUT} \le I_{MAX}$ (Note 6)	●	11.52		12.48	V
	Low	7V ≤ V_{IN} ≤ 30V	●		0.1	0.3	V
$\frac{\Delta V_O}{\Delta I_O}$	Load Regulation (Note 6)	V_{IN} = 16V 0 ≤ I_O ≤ 3A (Note 2)	●		10	80	mV
$\frac{\Delta V_O}{\Delta V_{IN}}$	Line Regulation	15V ≤ V_{IN} ≤ 30V (Note 2)			1	4	mV/V
	Ripple Rejection	50Hz ≤ f ≤ 500Hz (Note 8)		50	60		dB
	Thermal Regulation	ΔP_D = 20W (Note 4)			0.003	0.012	%/W
I_O	Available Load Current (Note 6)	15V ≤ V_{IN} ≤ 20V V_{IN} = 25V	● ●	3 2	4 2.7		A A
I_{SC}	Short Circuit Current	V_{IN} = 15V V_{IN} = 25V			2.3 1	4 2	A A
V_{IN}	Input Voltage to Maintain Regulation (Dropout Voltage)	(Note 5) I_O = 1A I_O = 3A	 ● ●		 13.8 14.4	 14.5 15	 V V
I_Q	Quiescent Current	Output High Output Low			4 3	5.5 4.5	mA mA
Θ_{JC}	Thermal Resistance, Junction to Case	TO-3 TO-220			1.5 2	2.5 3	°C/W °C/W

ELECTRICAL CHARACTERISTICS Auxiliary Regulator (See Note 1)

SYMBOL	PARAMETER	CONDITIONS		LT1036M/C MIN	TYP	MAX	UNITS
V_O	Output Voltage	$T_j = 25°C$		4.9	5.0	5.1	V
		$7.2V \le V_{IN} \le 30V$ $0mA \le I_O \le 75mA$	●	4.8	5.0	5.2	V
$\frac{\Delta V_O}{\Delta I_O}$	Load Regulation	$7.2V \le V_{IN} \le 30V$ $0mA \le I_O \le 75mA$ (Note 2)	●		5	15	mV
$\frac{\Delta V_O}{\Delta V_{IN}}$	Line Regulation	$7.2V \le V_{IN} \le 30V$ (Note 2)	 ●		0.2	1 2	mV/V mV/V
	Ripple Rejection	$50Hz \le f \le 500Hz$			74		dB
I_{SC}	Short Circuit Current (Note 7)	$7.0V \le V_{IN} = 30V$			140	250	mA
V_{IN}	Input Voltage to Maintain Regulation (Dropout Voltage)	(Note 5) $I_O \le 10mA$ $I_O = 75mA$	 ● ●		6.2 6.8	6.5 7.2	V V

ELECTRICAL CHARACTERISTICS Logic Control (See Note 1)

SYMBOL	PARAMETER	CONDITIONS		LT1036M/C MIN	TYP	MAX	UNITS
V_{EN}	Enable Threshold Voltage	$7.0V \le V_{IN} \le 30V$ $T_j = 25°C$	 ●	1.45 1.3	1.6 1.6	1.7 1.8	V V
	Enable Pin Current	$V_{EN} \le 1V$ (Note 3)	●	0	1.5	12	μA
		$V_{EN} \ge 2.4V$	●		0	6	μA

The ● denotes the specifications which apply over the full operating temperature range.

Note 1: Unless otherwise indicated, these specifications apply for $V_{IN} = 15V$, $I_O = 0mA$, and $T_j = 25°C$.

Note 2: Line and load regulation is measured using a low duty cycle pulse, causing little change in the junction temperature. Effects due to thermal gradients and device heating must be taken into account separately.

Note 3: When the enable pin is at a low logic level, current flows out of the enable pin.

Note 4: Pulse length for this measurement is 20ms.

Note 5: Input voltage is reduced until output drops by 100mV from its initial value.

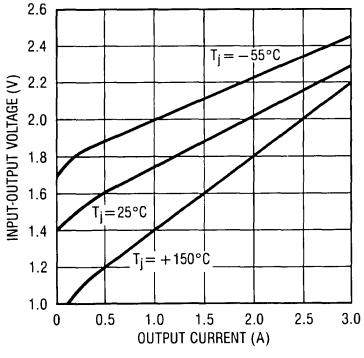
Note 6: See "Guaranteed Load Current" graph.

Note 7: Continuous shorts on the auxiliary output are not allowed unless adequate heat sinking is used to maintain junction temperature below 150°C.

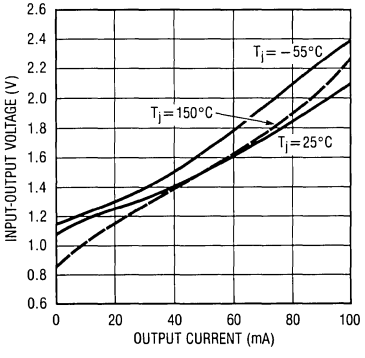
Note 8: Guaranteed but not tested.

TYPICAL PERFORMANCE CHARACTERISTICS

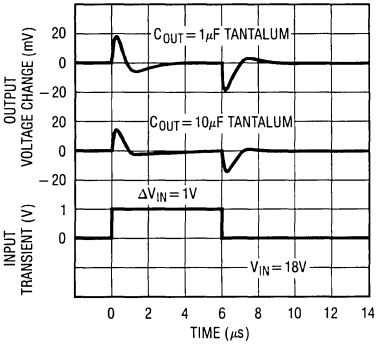
Minimum Input-Output Differential of Main Output



Minimum Input-Output Differential of Auxiliary Output

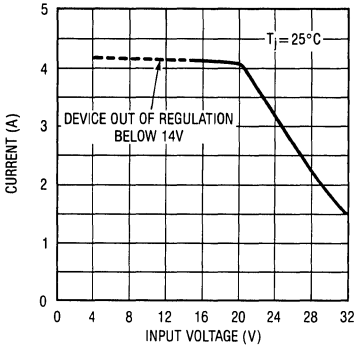


Line Transient Response, 12V Output

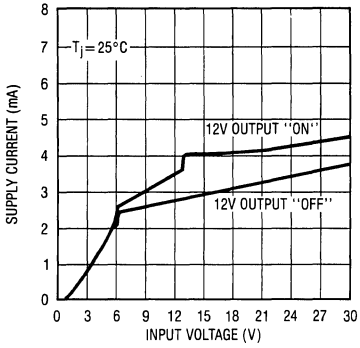


TYPICAL PERFORMANCE CHARACTERISTICS

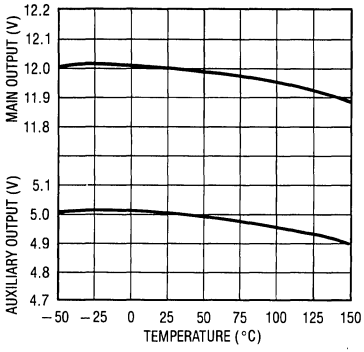
Maximum Available Load Current, 12V Output



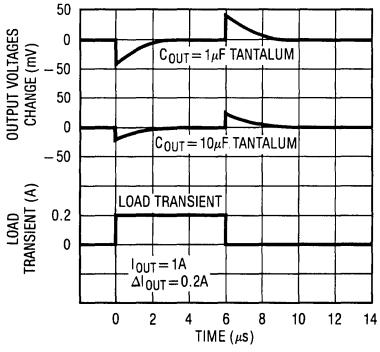
Quiescent Current



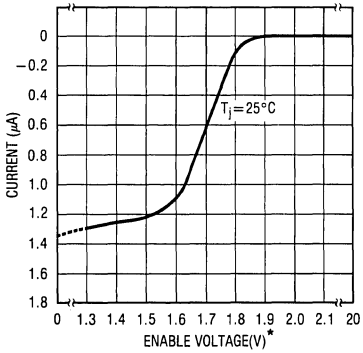
Output Voltage vs Temperature



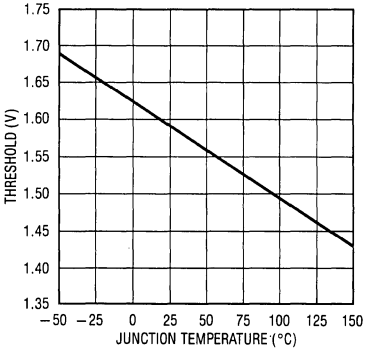
Load Transient Response, 12V Output



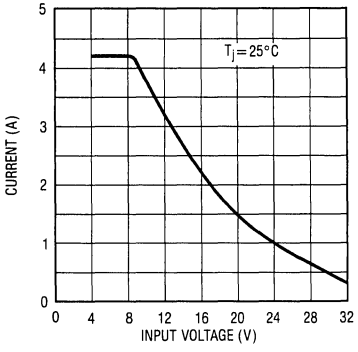
Enable Pin Characteristics



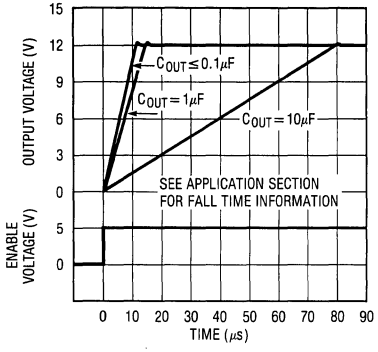
Enable Threshold



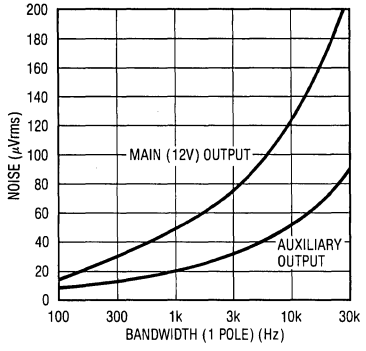
Short Circuit Current, 12V Output



Output Switching Characteristics



Output Voltage Noise



APPLICATIONS INFORMATION

General Information

The LT1036 is a dual output regulator. The main 12V output is capable of delivering up to 3A of load current and can be shut down with a logic signal. The auxiliary 5V output supplies a minimum of 75mA and is unaffected by the logic signal. The outputs are trimmed to ±2% initial tolerance and exhibit excellent line and load regulation.

The logic control feature makes the LT1036 ideal for many system applications where it is desirable to power-up a portion of the system for a period of time, and then power the system down during a standby operation. Applications such as multiple power supply sequencing, elimination of expensive AC and DC power switches, delayed start applications, switching 12V DC loads, and many others are now easily accomplished.

Timing functions, such as delayed power-up or power-down, can also be performed directly at the enable pin.

Because a logic low on the enable pin shuts down the main regulator, feedback from output to enable can be used to generate hysteresis or latching functions.

The low quiescent current drain of the LT1036 makes it useful in battery-powered or battery back-up applications. The enable pin can be used as a "low battery" detector or to shut down major portions of system power, allowing memory portions to continue to operate from the auxiliary output. At low output currents, the auxiliary output will regulate with input voltage typically as low as 6.2V, giving maximum battery life.

Good design practice with all regulators is to bypass the input and output terminals. A 2μF solid tantalum at the input and at both outputs is suggested. For the applications which follow, the bypass capacitors are still recommended, but for simplicity are not shown on the diagram. It is also recommended that for maximum noise immunity the voltage enable pin be tied high if it is unused. It can be tied directly to V_{IN}, as shown in Figure 1, or to the auxiliary output. If the enable pin is left open, it will float to a high logic level of approximately 1.6V and the main output regulator will be at 12V.

The enable pin is fully protected against input voltages up to 30V, even if the power input voltage is zero.

The basic shutdown control circuit uses a direct gate drive or an open collector driver and a pull-up resistor which are tied to V_{AUX}, as shown in Figure 2.

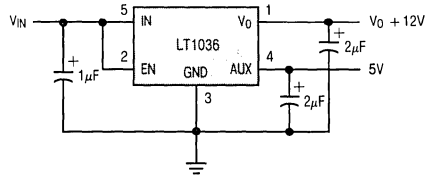


Figure 1

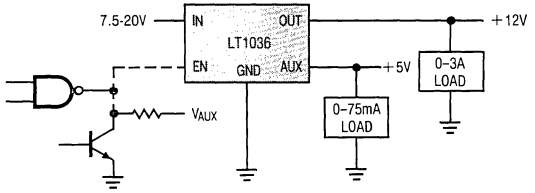


Figure 2

Driving the Enable Pin

The enable pin equivalent schematic is shown in Figure 3. Basically, enable pin current is zero above the threshold and about 1.5μA below the threshold, flowing out of the pin. Standard logic, such as TTL and CMOS, will interface directly to the enable pin, even if the logic output swing is higher than the input voltage (V_{IN}) to the regulator. 15V CMOS can be used to drive the enable pin, even if the regulator is not powered up, without loading the CMOS output.

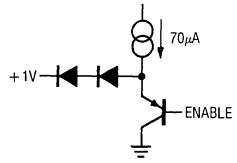


Figure 3

Timing functions, such as delayed power-up or power-down, can be implemented by driving the enable pin with an RC network. The current flowing out of the enable pin should not be used as the timing current in delayed power-up applications as it is temperature sensitive and varies somewhat from device to device. Instead, a resistor tied to the auxiliary output, the input, or to a logic signal

APPLICATIONS INFORMATION

should be used. The timing resistor chosen should provide at least 25μA of current to "swamp out" the effects of the internal current.

Main Output Current/Voltage Characteristics

Following a high to low transition at the enable pin, the main regulator output will begin to drop after a delay of approximately 0.4μs. With no capacitive load, the output will fall to zero in approximately 0.8μs (R_L = 4Ω to 100Ω). With a capacitive load, fall time is limited by the RC product of the load and the output capacitance. For light loads (R_L > 400Ω), the discharge time is controlled by an internal current pull-down of 15mA for output voltages down to 1.5V. Below 1.5V, the pull-down current drops to ≈4mA. The DC output voltage in the shutdown mode is approximately 0.12V due to an internal current path in the regulator. (See Figure 4)

The user should note that the output in the low state can only sink about 3mA. If current is forced into the output, the output voltage will rise to 1V at 5mA and about 1.5V at 10mA. With no output capacitor, the rise time of the main output is about 12μs. With an output capacitor, rise time is limited by the short circuit current of the LT1036 and the load capacitance. A 10μF output capacitor slows the output rise time to approximately 80μs.

Output Current

The main output current limits at about 4A for input voltages below 20V. Internal foldback, or "power limiting", circuitry detects the input-output voltage differential and reduces current limit for input to output voltages exceeding 8V. With 25V input, for instance, short circuit current is reduced to ≈0.9A.

An additional feature of the LT1036 is that the auxiliary supply does not incorporate, nor is it affected by, thermal shutdown. Any fault condition of the main regulator will not affect the auxiliary output voltage.

The following applications circuits will serve to indicate the versatility of the LT1036.

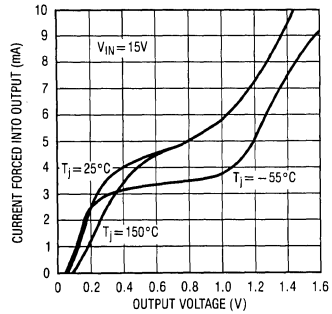
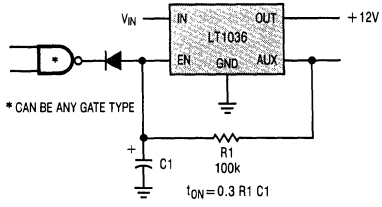


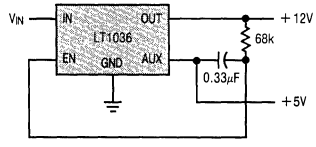
Figure 4

TYPICAL APPLICATIONS

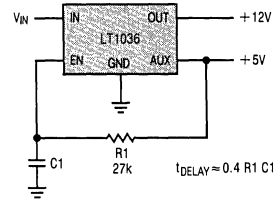
Fast Turn-Off, Delayed Turn-On



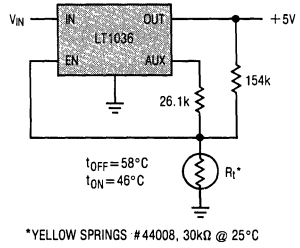
Latch-Off with Output Short



Delayed Power-Up

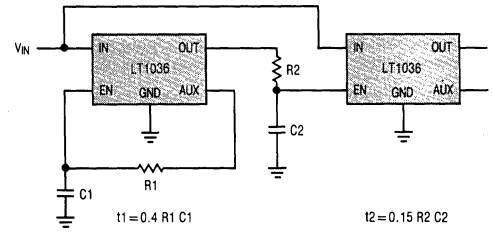


Thermal Cutoff at High Ambient Temperature



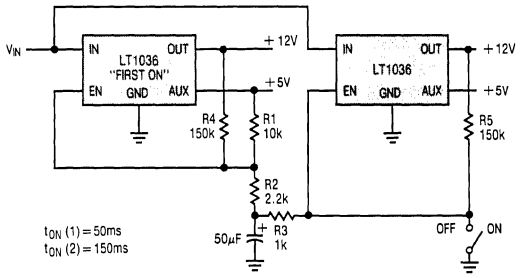
*YELLOW SPRINGS #44008, 30kΩ @ 25°C

Power Supply Turn-On Sequencing

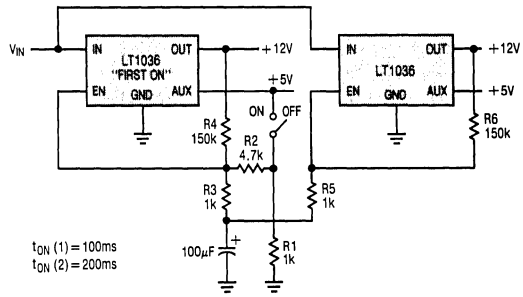


TYPICAL APPLICATIONS

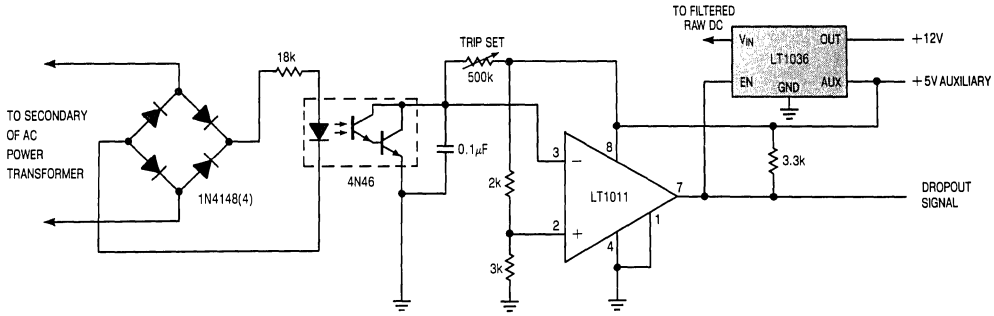
First-On, Last-Off Sequencing



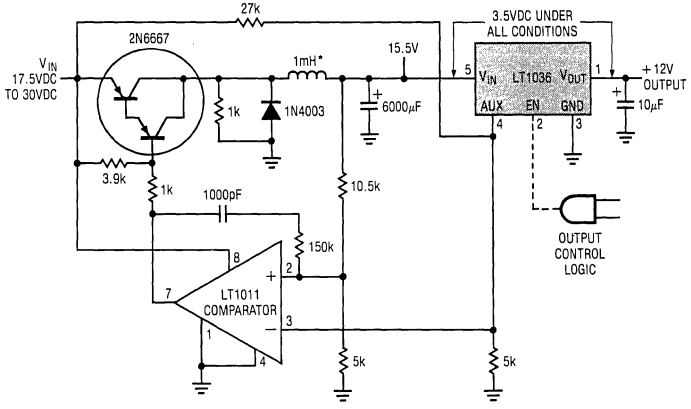
First-On, First-Off Sequencing



Line Dropout Detector

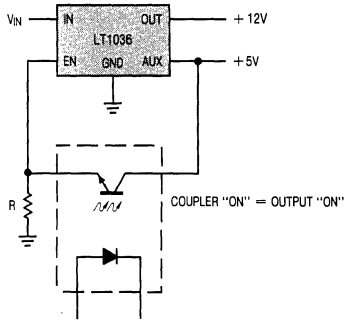


Low Dissipation Regulator



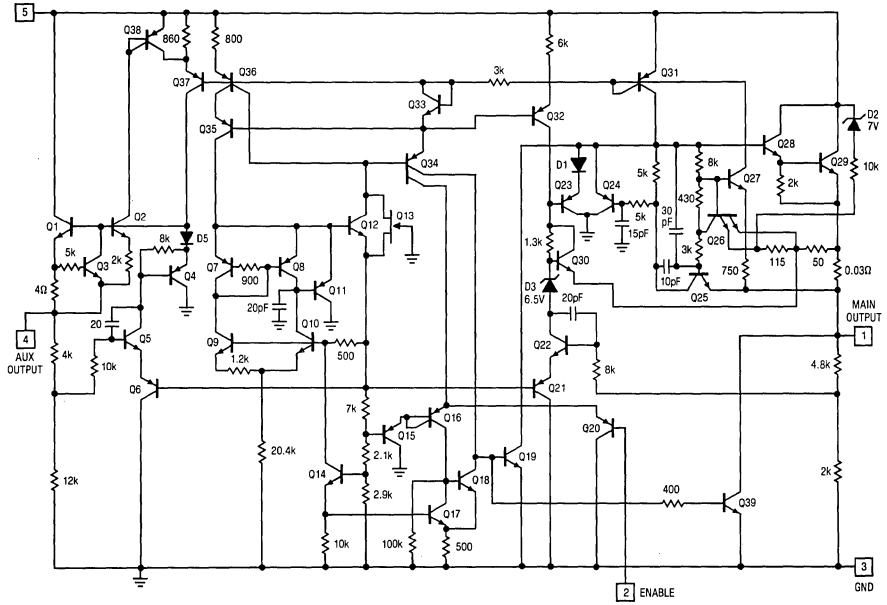
*DALE TD-5
THIS CIRCUIT IS DESIGNED TO REDUCE POWER DISSIPATION IN THE LT1036 OVER A 90VAC–140VAC INPUT RANGE.

Opto-Coupled Output Control



SELECT R DEPENDING UPON THE ON-RESISTANCE OF THE OPTO COUPLER

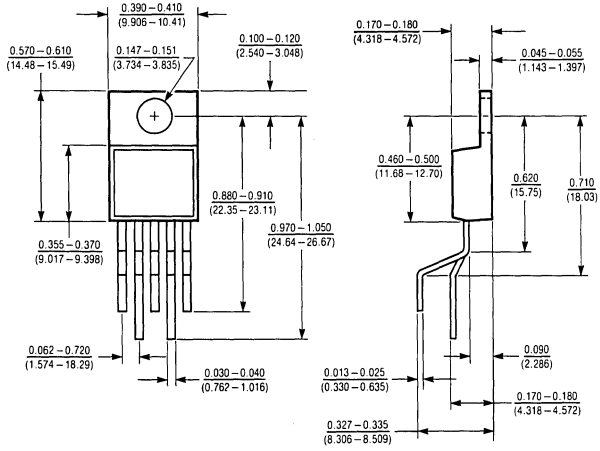
SCHEMATIC DIAGRAM



PACKAGE DESCRIPTION

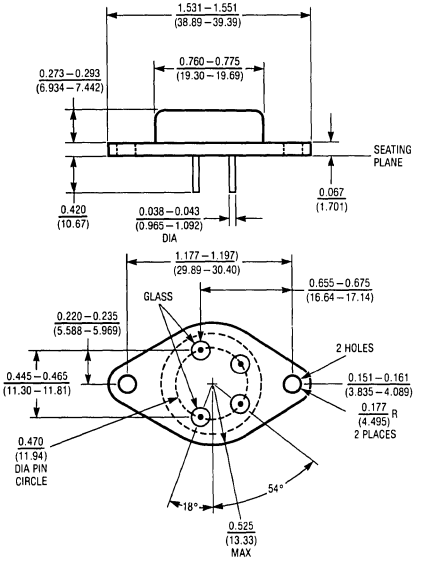
Dimensions in inches (millimeters) unless otherwise noted.

TO-220 Package (5 Lead)



	T_{jMAX}	θ_{jC}
LT1036C	125°C	3°C/W

4-Pin Metal Package Similar to JEDEC TO-3



	T_{jMAX}	θ_{jC}
LT1036M	150°C	2.5°C/W
LT1036C	125°C	2.5°C/W

10 Amp Positive Adjustable Voltage Regulator

FEATURES

- *Guaranteed* 0.8% Initial Tolerance
- *Guaranteed* 0.4% Load Regulation
- *Guaranteed* 10 Amp Output Current
- 100% Thermal Limit Burn-in
- 24 Amp Transient Output Current
- Standard Adjustable Pinout
- Operates to 35V

APPLICATIONS

- System Power Supplies
- High Power Linear Regulator
- Battery Chargers
- Power Driver
- Constant Current Regulator

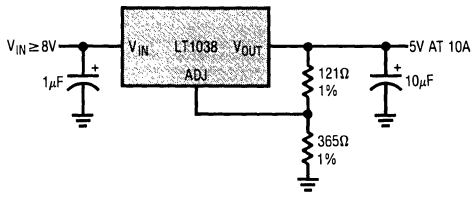
DESCRIPTION

The LT1038 is a three terminal regulator which is capable of providing in excess of 10 amps output current over 1.2V to 32V range. The device is packaged in a standard TO-3 power package, and is plug-in compatible with industry standard adjustable regulators, such as the LM117 and LM138. Also, the LT1038 is a functional replacement for the LM396.

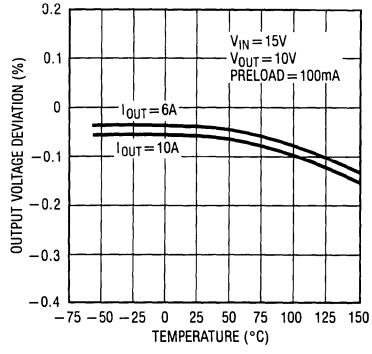
In addition to excellent load and line regulations, the LT1038 is fully protected by current limiting, safe area protection and thermal shutdown. New current limiting circuitry allows transient load currents up to 24 amps to be supplied for 500μs without causing the regulator to current limit and drop out of regulation during the transient.

On-chip trimming of initial reference voltage to $\pm$0.8% combined with 0.4% load regulation minimize errors in all high current applications. Further, the LT1038 is manufactured with standard bipolar processing and has Linear Technology's high reliability.

5V, 10 Amp Regulator



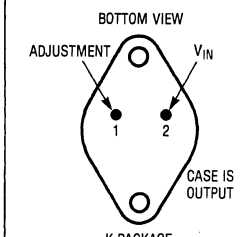
Load Regulation



ABSOLUTE MAXIMUM RATINGS

Power Dissipation ..... Internally Limited
Input to Output Voltage Differential 35V
Operating Junction Temperature Range
LT1038M
Control Circuitry ..... −55°C to 150°C
Power Transistor ..... −55°C to 200°C
LT1038C
Control Circuitry ..... 0°C to 125°C
Power Transistor ..... 0°C to 175°C
Storage Temperature ..... −65°C to 150°C
Lead Temperature (Soldering, 10 sec.) ..... 300°C

PACKAGE/ORDER INFORMATION



K PACKAGE
TO-3 METAL CAN
(STEEL)

ORDER PART NUMBER
LT1038MK LT1038CK

PRECONDITIONING

100% THERMAL LIMIT BURN-IN

ELECTRICAL CHARACTERISTICS (See Note 1)

SYMBOL	PARAMETER	CONDITIONS		LT1038M MIN	LT1038M TYP	LT1038M MAX	LT1038C MIN	LT1038C TYP	LT1038C MAX	UNITS
V_{REF}	Reference Voltage	$I_{OUT}=20mA$, $T_j=25°C$		1.24	1.25	1.26	1.23	1.25	1.275	V
		$3V \le (V_{IN}-V_{OUT}) \le 35V$ $20mA \le I_{OUT} \le 10A$, $P \le 75W$	●	1.22	1.25	1.285	1.22	1.25	1.285	V
$\frac{\Delta V_{OUT}}{\Delta V_{IN}}$	Line Regulation	$3V \le (V_{IN}-V_{OUT}) \le 35V$, $I_{OUT}=20mA$ (See Note 2) $T_A=25°C$			0.005	0.01		0.005	0.02	%/V
			●		0.02	0.03		0.02	0.03	%/V
$\frac{\Delta V_{OUT}}{\Delta I_{OUT}}$	Load Regulation	$20mA \le I_{OUT} \le 10A$ (See Note 2) $T_A=25°C$								
		$3V \le (V_{IN}-V_{OUT}) \le 35V$			0.1	0.4		0.1	0.6	%
		$3V \le (V_{IN}-V_{OUT}) \le 35V$	●		0.3	0.8		0.3	1	%
	Thermal Regulation	$T_A=25°C$, 20ms Pulse			0.002	0.005		0.002	0.01	%/W
	Ripple Rejection	$V_{OUT}=10V$, $f=120Hz$ $C_{ADJ}=0$	●		60			60		dB
		$C_{ADJ}=10\mu F$	●	60	75		60	75		dB
I_{ADJ}	Adjust Pin Current		●		50	100		50	100	μA
ΔI_{ADJ}	Adjust Pin Current Change	$20mA \le I_{OUT} \le 10A$ $3V \le (V_{IN}-V_{OUT}) \le 35V$	●		0.2	3		0.2	3	μA
	Minimum Load Current	$(V_{IN}-V_{OUT})=35V$	●		7	20		7	20	mA
		$(V_{IN}-V_{OUT}) \le 20V$	●			10			10	mA
I_{SC}	Current Limit	$(V_{IN}-V_{OUT}) \le 10V$ DC	●	10	14		10	14		A
		Transient (0.5ms)		14	22		14	22		A
		$(V_{IN}-V_{OUT})=30V$, $T_j=25°C$		1	2		1	2		A
$\frac{\Delta V_{OUT}}{\Delta Temp}$	Temperature Stability		●		1	2		1		%

ELECTRICAL CHARACTERISTICS (See Note 1)

SYMBOL	PARAMETER	CONDITIONS		LT1038M MIN	LT1038M TYP	LT1038M MAX	LT1038C MIN	LT1038C TYP	LT1038C MAX	UNITS
$\frac{\Delta V_{OUT}}{\Delta Time}$	Long Term Stability	$T_A = 125°C$, 1000 Hours			0.3	1		0.3	1	%
e_n	RMS Output Noise (% of V_{OUT})	$T_A = 25°C$, $10Hz \leq f \leq 10kHz$			0.001			0.001		%
Θ_{JC}	Thermal Resistance Junction to Case	Power Transistor Control Circuitry	●			1 0.5			1 0.5	°C/W °C/W

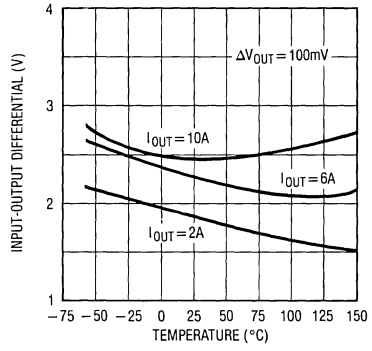
The ● denotes the specifications which apply over the full operating temperature range.

Note 1: Unless otherwise specified, these specifications apply: $V_{IN} - V_{OUT} = 5V$ and $I_{OUT} = 5A$. These specifications are applicable for power dissipations up to 75W. At input-output voltage differentials greater than 10V, achievable output current and power dissipation decrease due to protection circuitry.

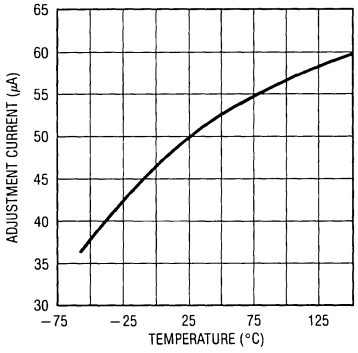
Note 2: See thermal regulation specifications for changes in output voltage due to heating effects. Load and line regulation are measured at a constant junction temperature by low duty cycle pulse testing.

TYPICAL PERFORMANCE CHARACTERISTICS

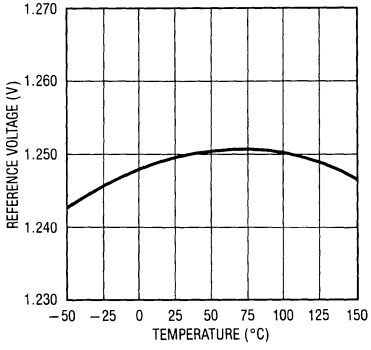
Dropout Voltage



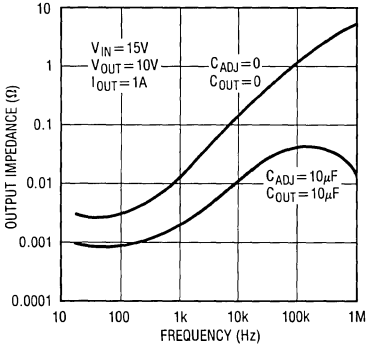
Adjustment Current



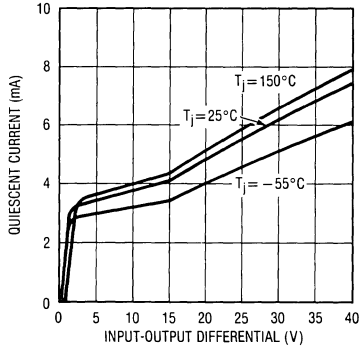
Temperature Stability



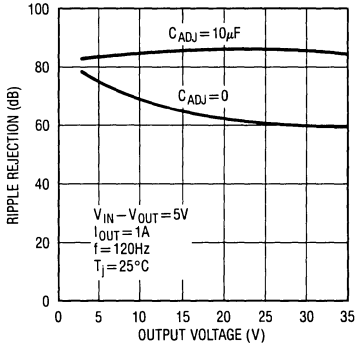
Output Impedance



Minimum Operating Current

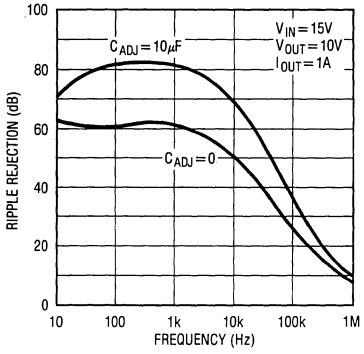


Ripple Rejection

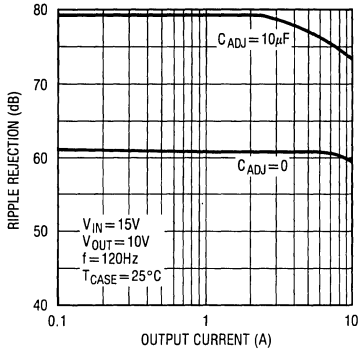


TYPICAL PERFORMANCE CHARACTERISTICS

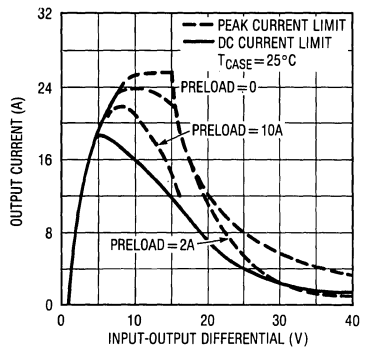
Ripple Rejection



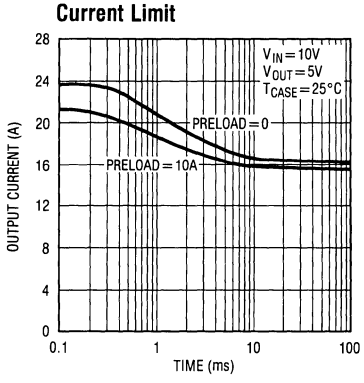
Ripple Rejection



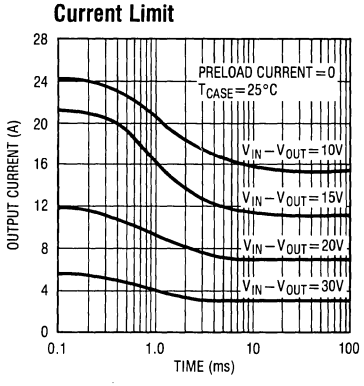
Current Limit



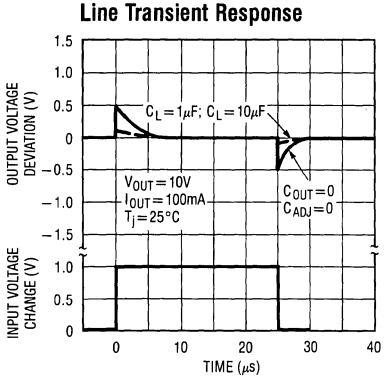
Current Limit



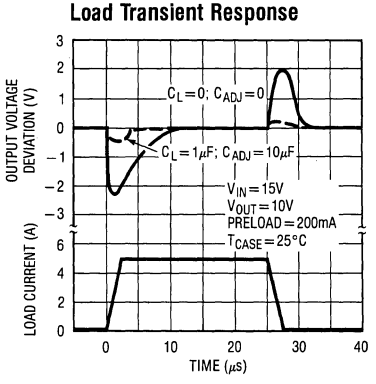
Current Limit



Line Transient Response



Load Transient Response



APPLICATIONS INFORMATION

General

The LT1038 develops a 1.25V reference voltage between the output and the adjustment terminal (see Figure 1). By placing a resistor, R1, between these two terminals, a constant current is caused to flow through R1 and down through R2 to set the overall output voltage. Normally this current is the specified minimum load current of 10 or 20mA. Because I_{ADJ} is very small and constant when compared with the current through R1, it represents a small error and can usually be ignored.

Bypass Capacitors

Input bypassing using a 1μF tantalum or 25μF electrolytic is recommended when the input filter capacitors are more than 5 inches from the device. Improved ripple rejection (80dB) can be accomplished by adding a 10μF capacitor from the adjust pin to ground. Increasing the size of the capacitor to 20μF will help ripple rejection at low output voltage since the reactance of this capacitor should be small compared to the voltage setting resistor, R2. For improved AC transient response and to prevent the possibility of oscillation due to unknown reactive load, a 1μF capacitor is also recommended at the output. Because of their low impedance at high frequencies, the best type of capacitor to use is solid tantalum.

Protection Diodes

The LT1038 does not require a protection diode from the adjustment terminal to the output (see Figure 2). Improved internal circuitry eliminates the need for this diode when the adjustment pin is bypassed with a capacitor to improve ripple rejection.

If a very large output capacitor is used, such as a 100μF shown in Figure 2, the regulator could be damaged or destroyed if the input is accidentally shorted to ground or crowbarred, due to the output capacitor discharging into the output terminal of the regulator. To prevent this, a diode, D1 as shown, is recommended to safely discharge the capacitor.

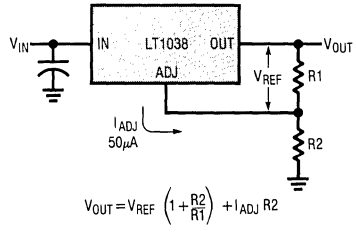


Figure 1. Basic Adjustable Regulator

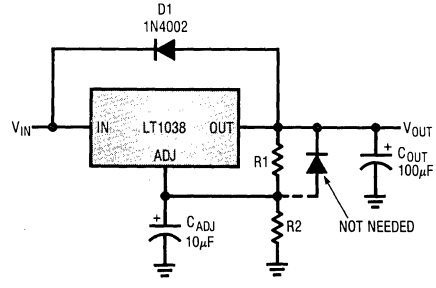


Figure 2

APPLICATIONS INFORMATION

Load Regulation

Because the LT1038 is a three-terminal device, it is not possible to provide true remote load sensing. Load regulation will be limited by the resistance of the wire connecting the regulator to the load. The data sheet specification for load regulation is measured at the bottom of the package. Negative side sensing can be a true Kelvin connection if the bottom of resistor R2 is returned to the negative side of the load. Although it may not be immediately obvious, best load regulation is obtained when the top of the resistor divider, R1, is connected *directly* to the case, *not to the load*. This is illustrated in Figure 3. If R1 were connected to the load, the effective resistance between the regulator and the load would be

$$R_p \times \left(\frac{R2+R1}{R1}\right), \; R_p = \text{Parasitic Line Resistance.}$$

Connected as shown, R_p is not multiplied by the divider ratio. R_p is about 0.004Ω per foot using 16 gauge wire. This translates to 4mV/ft at 1A load current, so it is important to keep the lead between the regulator and the load as short as possible, and use large wire or PC board traces.

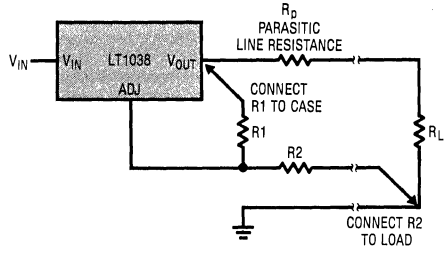
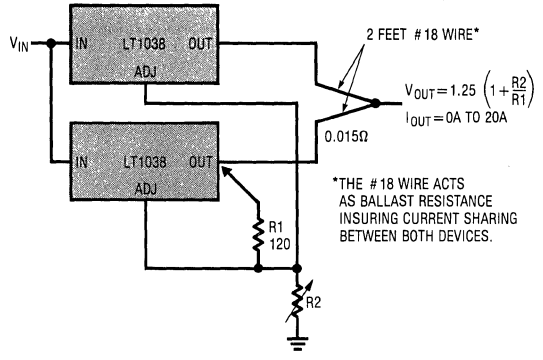


Figure 3. Connections for Best Load Regulation

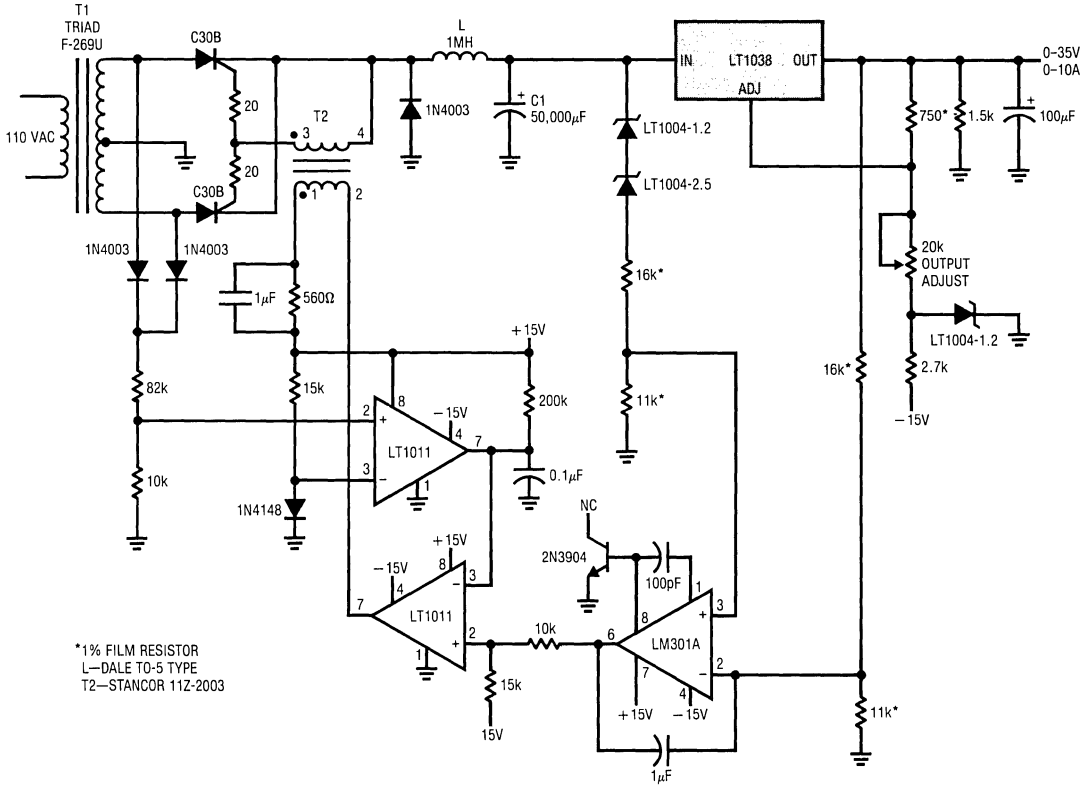
TYPICAL APPLICATIONS

Paralleling Regulators



TYPICAL APPLICATIONS

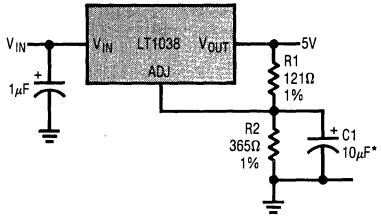
10 Amp Variable Regulator*



GENERAL PURPOSE REGULATOR WITH SCR PREREGULATOR TO LOWER POWER DISSIPATION. ABOUT 4V DIFFERENTIAL IS MAINTAINED ACROSS THE LT1038 INDEPENDENT OF OUTPUT VOLTAGE AND LOAD CURRENT.

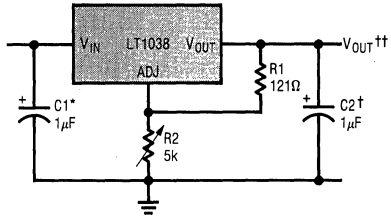
TYPICAL APPLICATIONS

Improving Ripple Rejection



*C1 IMPROVES RIPPLE REJECTION. X_C SHOULD BE SMALL COMPARED TO R2.

1.2V–25V Adjustable Regulator

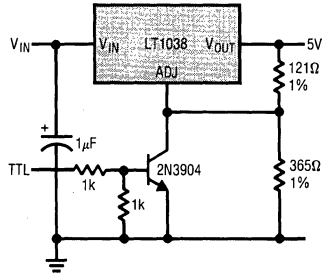


*NEEDED IF DEVICE IS FAR FROM FILTER CAPACITORS

†OPTIONAL—IMPROVES TRANSIENT RESPONSE

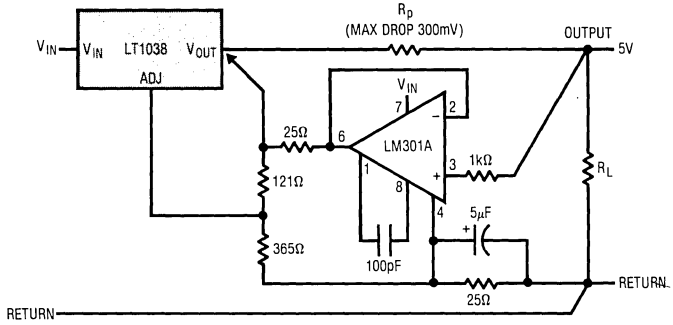
$^{\dagger\dagger}V_{OUT} = 1.25V\left(1+\frac{R2}{R1}\right)$

5V Regulator with Shutdown

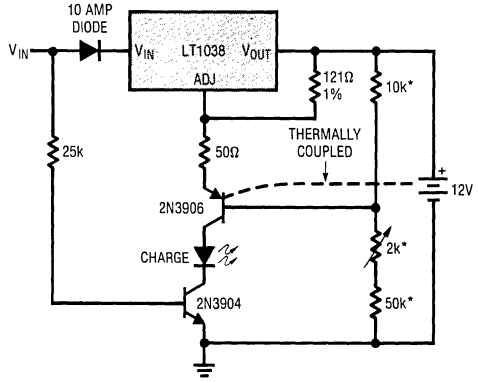


TYPICAL APPLICATIONS

Remote Sensing



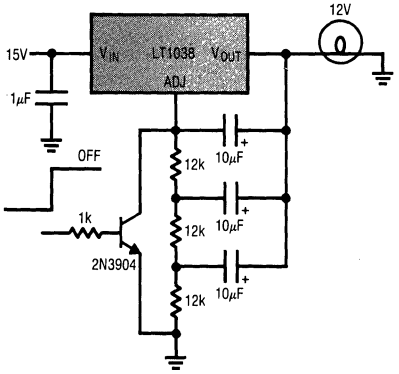
Temperature Compensated Lead Acid Battery Charger



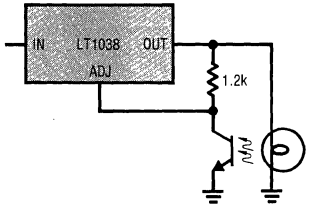
*LOAD ON BATTERY ≈200μA WHEN NOT CHARGING

TYPICAL APPLICATIONS

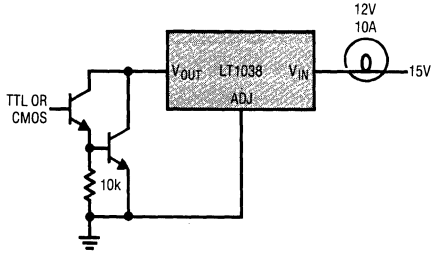
Lamp Flasher



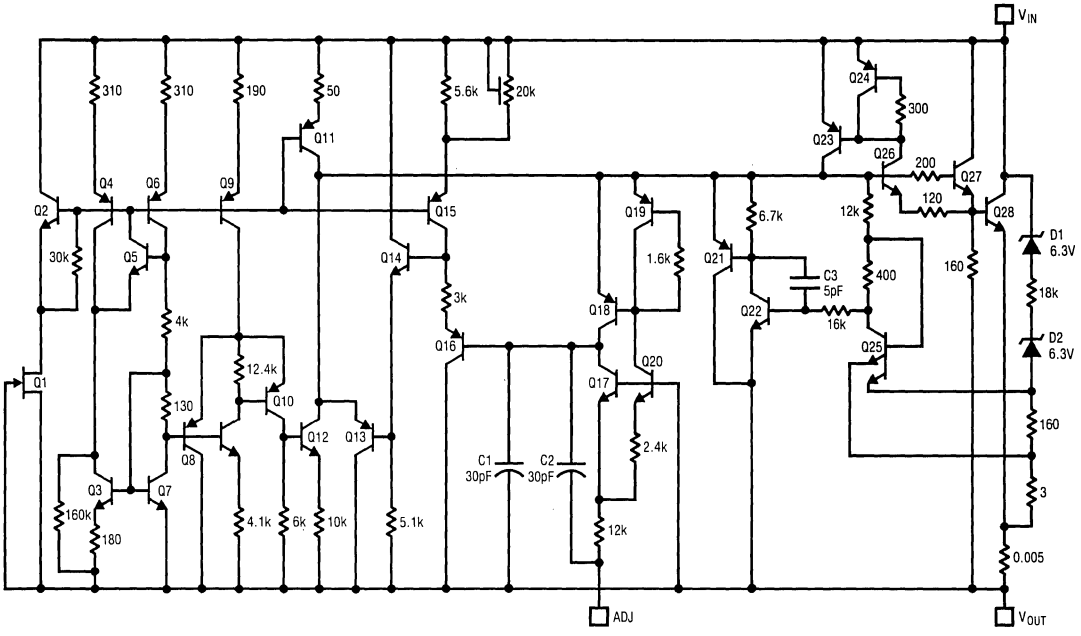
Automatic Light Control



Protected High Current Lamp Driver

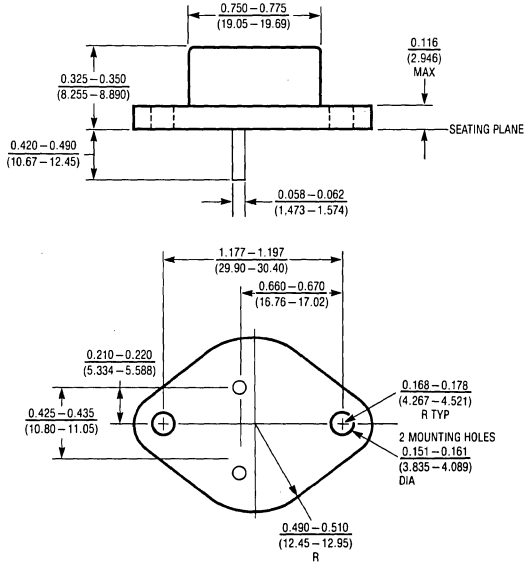


SCHEMATIC DIAGRAM



PACKAGE DESCRIPTION

K Package TO-3 Steel Metal Can



Positive Adjustable Regulator

FEATURES

- *Guaranteed* 1% Output Voltage Tolerance
- *Guaranteed* max. 0.01%/V Line Regulation
- *Guaranteed* max. 0.3% Load Regulation
- Min. 1.5A Output Current
- 100% Burn-in in Thermal Overload

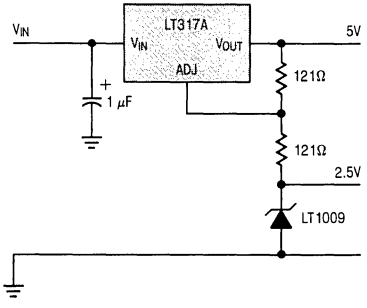
APPLICATIONS

- Wide Range Power Supplies
- Constant Current Supplies
- Voltage Programmable Supplies

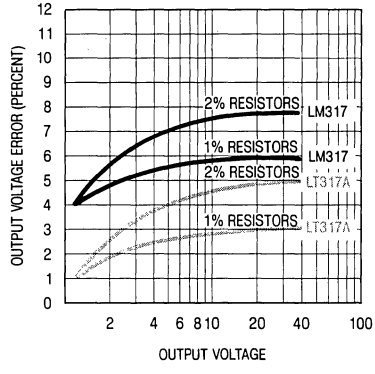
DESCRIPTION

The LT117A Series are 3-terminal positive adjustable voltage regulators which offer improved performance over earlier devices. A major feature of the LT117A is the output voltage tolerance is guaranteed at a maximum of ± 1%, allowing an overall power supply tolerance to be better than 3% using inexpensive 1% resistors. Line and load regulation performance has been improved as well. Additionally, the LT117A reference voltage is guaranteed not to exceed 2% when operating over the full load, line and power dissipation conditions. The LT117A adjustable regulators offer an improved solution for all positive voltage regulator requirements with load currents up to 1.5 amps.

Regulator with Reference



Output Voltage Error



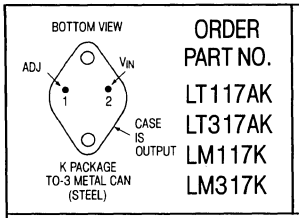
ABSOLUTE MAXIMUM RATINGS

Power Dissipation ..... Internally Limited
Input to Output Voltage Differential 40V
Operating Junction Temperature Range
LT117A/LM117 ..... −55°C to 150°C
LT317A/LM317 ..... 0°C to 125°C
Storage Temperature Range
LT117A/LM117 ..... −65°C to 150°C
LT317A/LM317 ..... −65°C to 150°C
Lead Temperature (Soldering, 10 sec.)..... 300°C

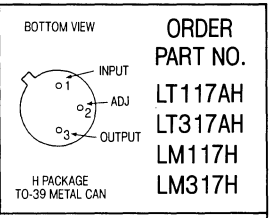
PRECONDITIONING:

100% THERMAL LIMIT BURN-IN

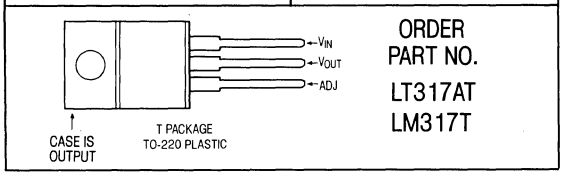
PACKAGE/ORDER INFORMATION



ORDER PART NO.
LT117AK
LT317AK
LM117K
LM317K



ORDER PART NO.
LT117AH
LT317AH
LM117H
LM317H



ORDER PART NO.
LT317AT
LM317T

ELECTRICAL CHARACTERISTICS (See Note 1) LT117A/LM117

SYMBOL	PARAMETER	CONDITIONS		LT117A MIN	LT117A TYP	LT117A MAX	LM117 MIN	LM117 TYP	LM117 MAX	UNITS
V_{REF}	Reference Voltage	I_{OUT} = 10mA T_J = 25°C		1.238	1.250	1.262				V
		3V ≤ (V_{IN} − V_{OUT}) ≤ 40V 10mA ≤ I_{OUT} ≤ I_{max}, P ≤ P_{max}	●	1.225	1.250	1.270	1.20	1.25	1.30	V
$\frac{\Delta V_{OUT}}{\Delta V_{IN}}$	Line Regulation	3V ≤ (V_{IN} − V_{OUT}) ≤ 40V, (See Note 2)			0.005	0.01		0.01	0.02	%/V
			●		0.01	0.02		0.02	0.05	%/V
$\frac{\Delta V_{OUT}}{\Delta I_{OUT}}$	Load Regulation	10mA ≤ I_{OUT} ≤ I_{max}, (See Note 2) V_{OUT} ≤ 5V V_{OUT} ≥ 5V			5 0.1	15 0.3		5 0.1	15 0.3	mV %
		V_{OUT} ≤ 5V V_{OUT} ≥ 5V	● ●		20 0.3	50 1		20 0.3	50 1	mV %
	Thermal Regulation	T_A = 25°C, 20msec Pulse			0.002	0.02		0.03	0.07	%/W
	Ripple Rejection	V_{OUT} = 10V, f = 120Hz C_{ADJ} = 0	●		65			65		dB
		C_{ADJ} = 10μF	●	66	80		66	80		dB
I_{ADJ}	Adjust Pin Current		●		50	100		50	100	μA
ΔI_{ADJ}	Adjust Pin Current Change	10mA ≤ I_{OUT} ≤ I_{max} 2.5V ≤ (V_{IN} − V_{OUT}) ≤ 40V	●		0.2	5		0.2	5	μA
I_{min}	Minimum Load Current	(V_{IN} − V_{OUT}) = 40V	●		3.5	5		3.5	5	mA
	Current Limit	(V_{IN} − V_{OUT}) ≤ 15V K Package H Package	● ●	1.5 0.5	2.2 0.8		1.5 0.5	2.2 0.8		A A
		(V_{IN} − V_{OUT}) = 40V, T_j = 25°C K Package H Package		0.3 0.15	0.5 0.2		0.3 0.15	0.4 0.2		A A
$\frac{\Delta V_{OUT}}{\Delta Temp}$	Temperature Stability	−55°C ≤ T_j ≤ +150°C			1	2		1		%
$\frac{\Delta V_{OUT}}{\Delta Time}$	Long Term Stability	T_A = 125°C			0.3	1		0.3	1	%
e_n	RMS Output Noise (% of V_{OUT})	T_A = 25°C, 10Hz ≤ f ≤ 10kHz			0.001			0.001		%
Θ_{jc}	Thermal Resistance Junction to Case	H Package K Package			12 2.3	15 3		12 2.3	15 3	°C/W °C/W

ELECTRICAL CHARACTERISTICS (See Note 1) LT317A/LM317

SYMBOL	PARAMETER	CONDITIONS		LT317A MIN	LT317A TYP	LT317A MAX	LM317 MIN	LM317 TYP	LM317 MAX	UNITS
V_{REF}	Reference Voltage	I_{OUT} = 10mA T_j = 25°C		1.238	1.250	1.262				V
		3V ≤ (V_{IN} − V_O) ≤ 40V 10mA ≤ I_{OUT} ≤ I_{max}, P ≤ P_{max}	●	1.225	1.250	1.270	1.20	1.25	1.30	V
$\frac{\Delta V_{OUT}}{\Delta V_{IN}}$	Line Regulation	3V ≤ (V_{IN} − V_{OUT}) ≤ 40V, (See Note 2)			0.005	0.01		0.01	0.04	%/V
			●		0.01	0.02		0.02	0.07	%/V
$\frac{\Delta V_{OUT}}{\Delta I_{OUT}}$	Load Regulation	10mA ≤ I_{OUT} ≤ I_{max}, (See Note 2) V_O ≤ 5V V_O ≥ 5V			5 0.1	25 0.5		5 0.1	25 0.5	mV %
		V_O ≤ 5V V_O ≥ 5V	● ●		20 0.3	50 1		20 0.3	70 1.5	mV %
	Thermal Regulation	T_A = 25°C, 20msec Pulse	●		0.002	0.02		0.04	0.07	%/W
	Ripple Rejection	V_O = 10V, f = 120Hz C_{ADJ} = 0			65			65		dB
		C_{ADJ} = 10μF		66	80		66	80		dB
I_{ADJ}	Adjust Pin Current				50	100		50	100	μA
ΔI_{ADJ}	Adjust Pin Current Change	10mA ≤ I_{OUT} ≤ I_{max} 2.5V ≤ (V_{IN} − V_{OUT}) ≤ 40V	●		0.2	5		0.2	5	μA
I_{min}	Minimum Load Current	(V_{IN} − V_{OUT}) = 40V	●		3.5	10		3.5	10	mA
	Current Limit	(V_{IN} − V_{OUT}) ≤ 15V K and T Package H Package	 ● ●	 1.5 0.5	 2.2 0.8		 1.5 0.5	 2.2 0.8		 A A
		(V_{IN} − V_{OUT}) = 40V, T_j = 25°C K and T Package H Package		 0.15 0.075	 0.4 0.2		 0.15 0.075	 0.4 0.2		 A A
$\frac{\Delta V_{OUT}}{\Delta Temp}$	Temperature Stability	0°C ≤ T_j ≤ 125°C			1	2		1		%
$\frac{\Delta V_{OUT}}{\Delta Time}$	Long Term Stability	T_A = 125°C			0.3	1		0.3	1	%
e_n	RMS Output Noise (% of V_{OUT})	T_A = 25°C, 10Hz ≤ f ≤ 10kHz			0.001			0.001		%
Θ_{jc}	Thermal Resistance Junction to Case	H Package K Package T Package			12 2.3 4	15 3 5		12 2.3 4	15 3	°C/W °C/W °C/W

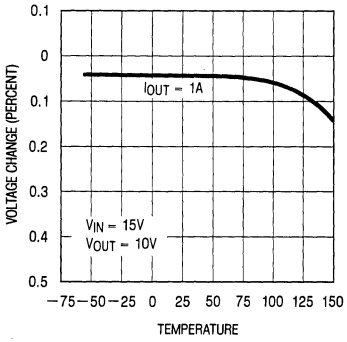
The ● denotes the specifications which apply over the full operating temperature range.

Note 1: Unless otherwise specified, these specifications apply for V_{IN} − V_{OUT} = 5V; and I_{OUT} = 0.1A for the TO-39 and I_{OUT} = 0.5A for the TO-3 and TO-220 packages. Although power dissipation is internally limited, these specifications are applicable for power dissipations of 2W for the TO-39, and 20W for the TO-3 and TO-220. I_{MAX} is 1.5A for the TO-3 and TO-220 packages and 0.5A for the TO-39.

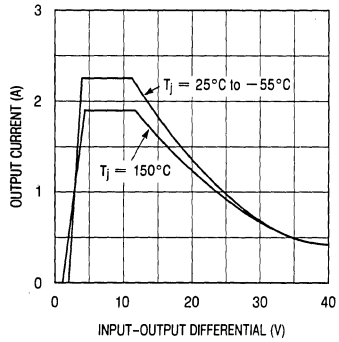
Note 2: Regulation is measured at constant junction temperature, using pulse testing with a low duty cycle. Changes in output voltage due to heating effects are covered under the specification for thermal regulation. Load regulation is measured on the output pin at a point 1/8" below the base of the K and H package and at the junction of the wide and narrow portion of the lead on the T package.

TYPICAL PERFORMANCE CHARACTERISTICS

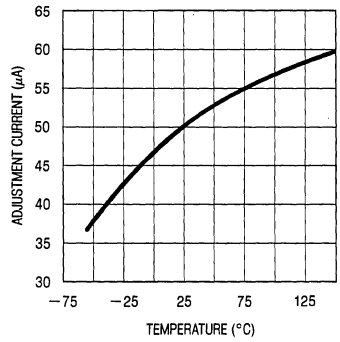
Load Regulation



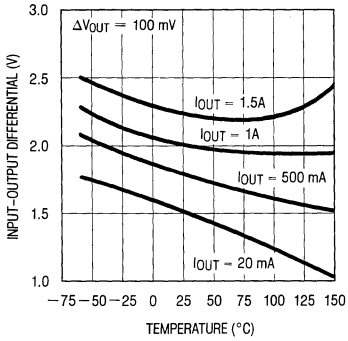
Current Limit (TO-3 and TO-220 Package)



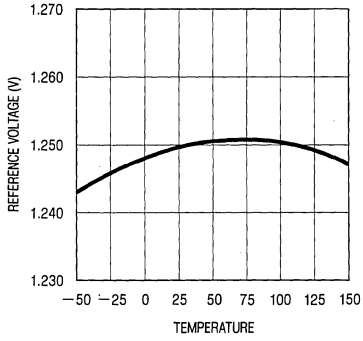
Adjustment Current



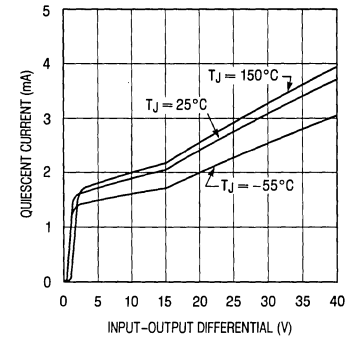
Dropout Voltage



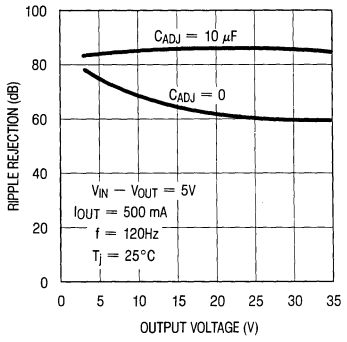
Temperature Stability



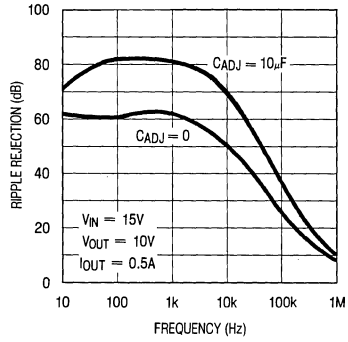
Minimum Operating Current



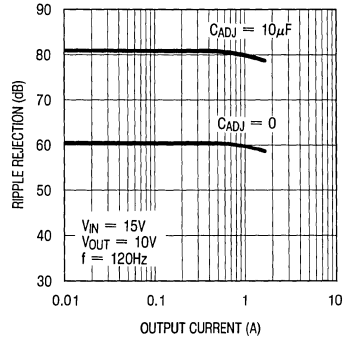
Ripple Rejection



Ripple Rejection (dB)



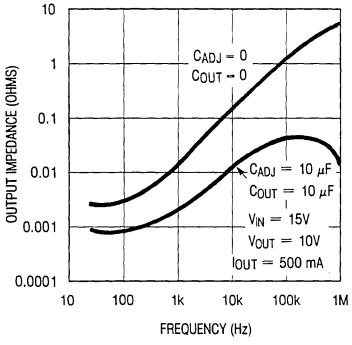
Ripple Rejection



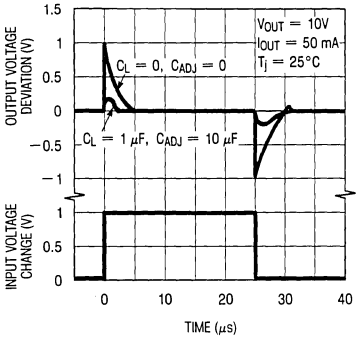
LINEAR TECHNOLOGY

TYPICAL PERFORMANCE CHARACTERISTICS

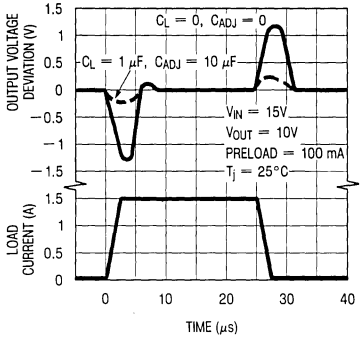
Output Impedance



Line Transient Response



Load Transient Response



APPLICATIONS INFORMATION

General: The LT117A develops a 1.25V reference voltage between the output and the adjustable terminal (see Figure 1). By placing a resistor, R1, between these two terminals, a constant current is caused to flow through R1 and down through R2 to set the overall output voltage. Normally this current is the specified minimum load current of 5mA or 10mA.

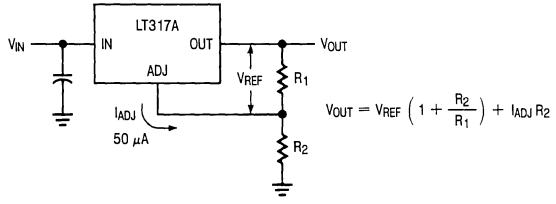


Figure 1

Because I_{ADJ} is very small and constant when compared with the current through R1, it represents a small error and can usually be ignored.

It is easily seen from the above equation, that even if the resistors were of exact value, the accuracy of the output is limited by the accuracy of V_{REF}. Earlier adjustable regulators had a reference tolerance of ±4%. This tolerance is dangerously close to the ±5% supply tolerance required in many logic and analog systems. Further, many 1% resistors can drift 0.01%/°C adding another 1% to the output voltage tolerance.

For example, using 2% resistors and ±4% tolerance for V_{REF}, calculations will show that the expected range of a 5V regulator design would be $4.66V \leq V_{OUT} \leq 5.36V$ or approximately ±7%. If the same example were used for a 15V regulator, the expected tolerance would be ±8%. With these results most applications require some method of trimming, usually a trim pot. This solution is both expensive and not conducive to volume production.

One of the enhancements of Linear Technology's adjustable regulators over existing devices is tightened initial tolerance. This allows relatively inexpensive 1% or 2% film resistors to be used for R1 and R2 while setting output voltage within an acceptable tolerance range.

With a guaranteed 1% reference, a 5V power supply design, using ±2% resistors, would have a worst case manufacturing tolerance of ±4%. If 1% resistors were used, the tolerance would drop to ±2.5%. A plot of the worst case output voltage tolerance as a function of resistor tolerance is shown on the front page.

For convenience, a table of standard 1% resistor values is shown below.

Table of ½% and 1% Standard Resistance Values

1.00	1.47	2.15	3.16	4.64	6.81
1.02	1.50	2.21	3.24	4.75	6.98
1.05	1.54	2.26	3.32	4.87	7.15
1.07	1.58	2.32	3.40	4.99	7.32
1.10	1.62	2.37	3.48	5.11	7.50
1.13	1.65	2.43	3.57	5.23	7.68
1.15	1.69	2.49	3.65	5.36	7.87
1.18	1.74	2.55	3.74	5.49	8.06
1.21	1.78	2.61	3.83	5.62	8.25
1.24	1.82	2.67	3.92	5.76	8.45
1.27	1.87	2.74	4.02	5.90	8.66
1.30	1.91	2.80	4.12	6.04	8.87
1.33	1.96	2.87	4.22	6.19	9.09
1.37	2.00	2.94	4.32	6.34	9.31
1.40	2.05	3.01	4.42	6.49	9.53
1.43	2.10	3.09	4.53	6.65	9.76

Standard Resistance Values are obtained from the Decade Table by multiplying by multiples of 10. As an example, 1.21 can represent 1.21Ω, 12.1Ω, 121Ω, 1.21KΩ etc.

Bypass Capacitors: Input bypassing using a 1μF tantalum or 25μF electrolytic is recommended when the input filter capacitors are more than 5 inches from the device. Improved ripple rejection (80 dB) can be accomplished by adding a 10μF capacitor from the adjust pin to ground. Increasing the size of the capacitor to 20μF will help ripple rejection at low output voltage since the reactance of this capacitor should be small compared to the voltage setting resistor, R2. For improved AC transient response and to prevent the possibility of oscillation due to unknown reactive load, a 1μF capacitor is also recommended at the output. Because of their low impedance at high frequencies, the best type of capacitor to use is solid tantalum.

Protection Diodes: The LT117A/317A do not require a protection diode from the adjustment terminal to the output (see Figure 2). Improved internal circuitry eliminates the need for this diode when the adjustment pin is bypassed with a capacitor to improve ripple rejection.

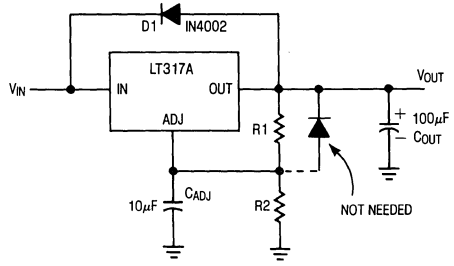


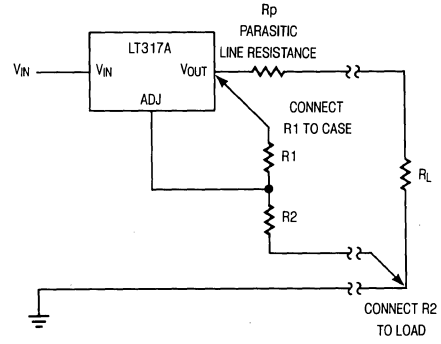
Figure 2

If a very large output capacitor is used, such as a 100μF shown in Figure 2, the regulator could be damaged or destroyed if the input is accidentally shorted to ground or crowbarred. This is due to the output capacitor discharging into the output terminal of the regulator. To prevent damage a diode D1 is recommended to safely discharge the capacitor.

Load Regulation: Because the LT117A is a three-terminal device, it is not possible to provide true remote load sensing. Load regulation will be limited by the resistance of the wire connecting the regulator to the load. For the data sheet specification, regulation is measured at the bottom of the package. Negative side sensing is a true Kelvin connection, with the bottom of the output divider returned to the negative side of the load. Although it may not be immediately obvious, best load regulation is obtained when the top of the divider is connected *directly* to the case *not to the load.* This is illustrated in *Figure 3.* If R1 were connected to the load, the effective resistance between the regulator and the load would be

$$R_p \times \left(\frac{R2 + R1}{R1}\right), R_p = \text{Parasitic Line Resistance.}$$

Connected as shown, R_p is not multiplied by the divider ratio. R_p is about 0.004Ω per foot using 16 guage wire. This translates to 4mV/ft at 1A load current, so it important to keep the positive lead between regulator and load as short as possible.

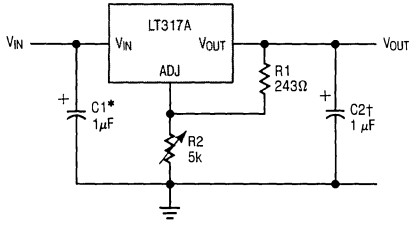


Connections for Best Load Regulation

Figure 3

TYPICAL APPLICATIONS

1.2V–25V Adjustable Regulator

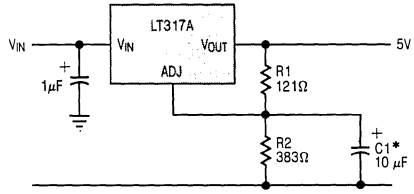


† Optional — improves transient response

* Needed if device is far from filter capactiors

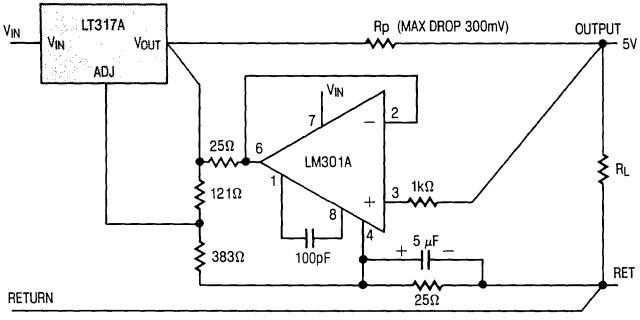
$$V_{OUT} = 1.25V \left(1 + \frac{R2}{R1}\right)$$

Improving Ripple Rejection

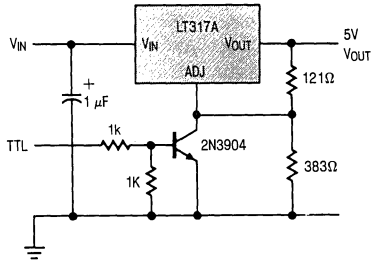


*C1 IMPROVES RIPPLE REJECTION
X_C SHOULD BE SMALL
COMPARED TO R2

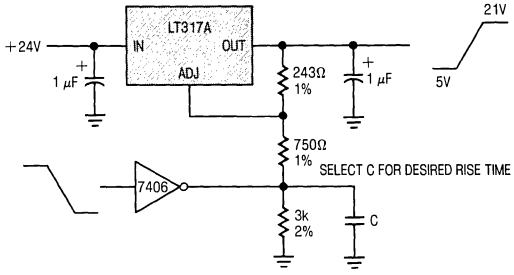
Remote Sensing



5V Regulator with Shut Down

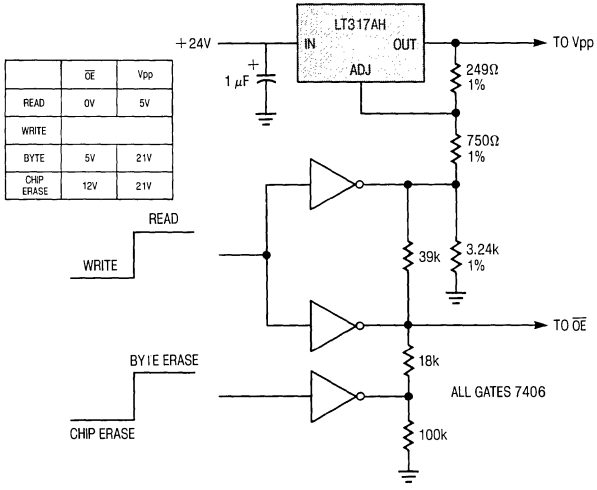


21V Programming Supply for UV PROM/EEROM

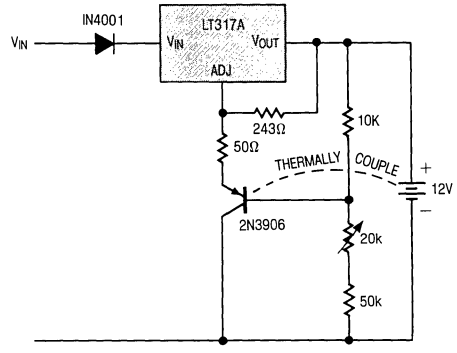


2816 EEPROM Supply Programmer for Read/Write Control

	$\overline{OE}$	Vpp
READ	0V	5V
WRITE		
BYTE	5V	21V
CHIP ERASE	12V	21V

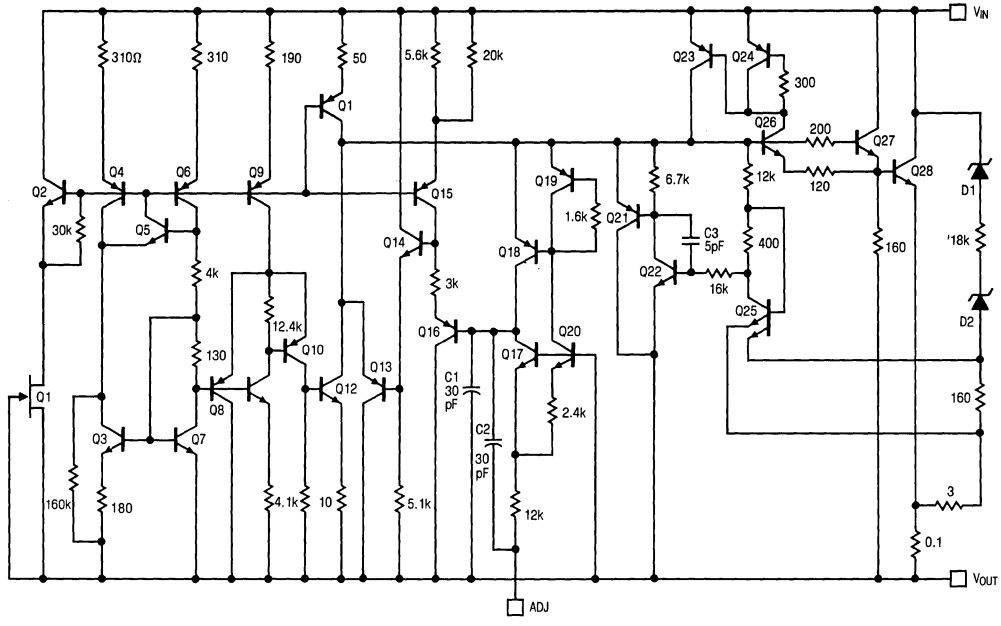


Temperature Compensated Lead Acid Battery Charger



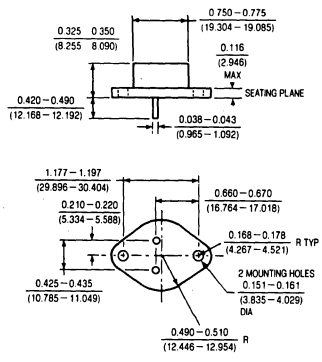
SCHEMATIC DIAGRAM

LT117A/LT317A



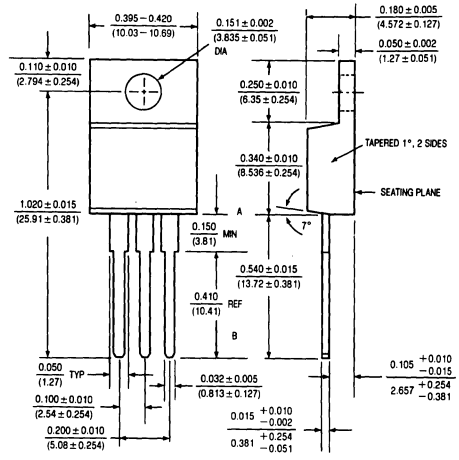
PACKAGE DESCRIPTION

K Package TO-3 STEEL Metal Can



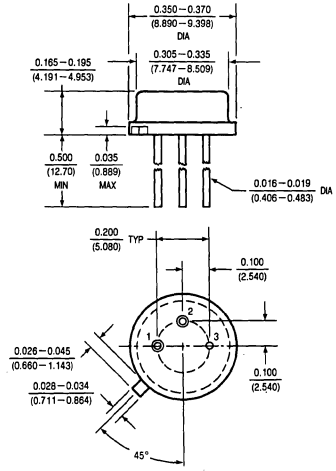
	T_j max.	θ_{ja}	θ_{jc}
117A 117	150°C	35°C/W	3°C/W
317A 317	125°C	35°C/W	3°C/W

T Package TO-220 Plastic



	T_j max.	θ_{ja}	θ_{jc}
317A 317	125°C	50°C/W	5°C/W

H Package 3-Lead Metal Can



	T_j max.	θ_{ja}	θ_{jc}
117A 117	150°C	150°C/W	15°C/W
317A 317	125°C	150°C/W	15°C/W

LINEAR TECHNOLOGY

High Voltage Positive Adjustable Regulators

FEATURES

- 60V Operation
- *Guaranteed* 1% Output Voltage Tolerance
- *Guaranteed* max. 0.01%/V Line Regulation
- *Guaranteed* max. 0.3% Load Regulation
- Min. 1.5A Output Current
- 100% Burn-in in Thermal Overload

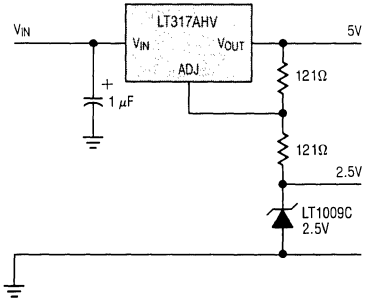
APPLICATIONS

- Wide Range Power Supplies
- Constant Current Supplies
- Voltage Programmable Supplies

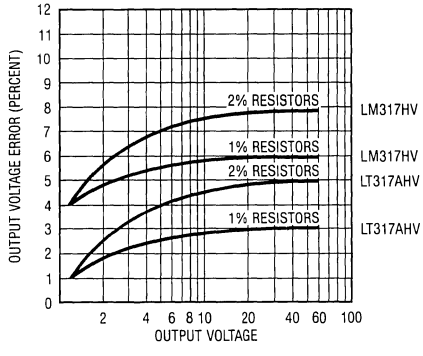
DESCRIPTION

The LT117AHV Series are 3-terminal positive adjustable voltage regulators which offer improved performance over earlier devices. A major feature of the LT117AHV is the output voltage tolerance is guaranteed at a maximum of ±1%, allowing an overall power supply tolerance to be better than 3% using inexpensive 1% resistors. Line and load regulation performance has been improved as well. Additionally, the LT117AHV reference voltage is guaranteed not to exceed 2% when operating over the full load, line and power dissipation conditions. The LT117AHV adjustable regulators offer an improved solution for all positive voltage regulator requirements with load currents up to 1.5 amps. For performance curves and applications circuits see the LT117A series data sheet.

Regulator with Reference



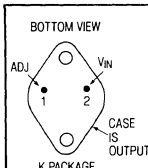
Output Voltage Error



ABSOLUTE MAXIMUM RATINGS

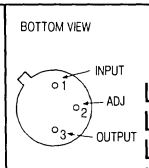
Power Dissipation ..... Internally Limited
Input to Output Voltage Differential 60V
Operating Junction Temperature Range
LT117AHV/LM117HV ..... −55°C to 150°C
LT317AHV/LM317HV ..... 0°C to 125°C
Storage Temperature Range
LT117AHV/LM117HV ..... −65°C to 150°C
LT317AHV/LM317HV ..... −65°C to 150°C
Lead Temperature (Soldering, 10 sec.) ..... 300°C

PACKAGE/ORDER INFORMATION



K PACKAGE
TO-3 METAL CAN
(STEEL)

ORDER PART NO.
LT117AHVK
LT317AHVK
LM117HVK
LM317HVK



H PACKAGE
TO-39 METAL CAN

ORDER PART NO.
LT117AHVH
LT317AHVH
LM117HVH
LM317HVH

PRECONDITIONING:

100% THERMAL LIMIT BURN-IN

ELECTRICAL CHARACTERISTICS (See Note 1) LT117AHV/LM117HV

SYMBOL	PARAMETER	CONDITIONS		LT117AHV MIN	LT117AHV TYP	LT117AHV MAX	LM117HV MIN	LM117HV TYP	LM117HV MAX	UNITS
V_{REF}	Reference Voltage	I_{OUT} = 10mA T_J = 25°C		1.238	1.250	1.262				V
		$3V \leq (V_{IN} - V_{OUT}) \leq 60V$ $10mA \leq I_{OUT} \leq I_{max}$, $P \leq P_{max}$	●	1.225	1.250	1.270	1.20	1.25	1.30	V
$\frac{\Delta V_{OUT}}{\Delta V_{IN}}$	Line Regulation	$3V \leq (V_{IN} - V_{OUT}) \leq 60V$ (See Note 2)			0.005	0.01		0.01	0.02	%/V
			●		0.01	0.02		0.02	0.05	%/V
$\frac{\Delta V_{OUT}}{\Delta I_{OUT}}$	Load Regulation	$10mA \leq I_{OUT} \leq I_{max}$, (See Note 2) $V_{OUT} \leq 5V$ $V_{OUT} \geq 5V$			5 0.1	15 0.3		5 0.1	15 0.3	mV %
		$V_{OUT} \leq 5V$ $V_{OUT} \geq 5V$	● ●		20 0.3	50 1		20 0.3	50 1	mV %
	Thermal Regulation	T_A = 25°C, 20msec Pulse			0.002	0.02		0.03	0.07	%/W
	Ripple Rejection	V_{OUT} = 10V, f = 120Hz C_{ADJ} = 0	●		65			65		dB
		C_{ADJ} = 10μF	●	66	80		66	80		dB
I_{ADJ}	Adjust Pin Current		●		50	100		50	100	μA
ΔI_{ADJ}	Adjust Pin Current Change	$10mA \leq I_{OUT} \leq I_{max}$ $2.5V \leq (V_{IN} - V_{OUT}) \leq 60V$	●		0.2	5		0.2	5	μA
I_{min}	Minimum Load Current	$(V_{IN} - V_{OUT}) = 60V$	●		3.5	7		3.5	7	mA
	Current Limit	$(V_{IN} - V_{OUT}) \leq 15V$ K Package H Package	 ● ●	 1.5 0.5	 2.2 0.8		 1.5 0.5	 2.2 0.8		 A A
		$(V_{IN} - V_{OUT}) = 60V$, T_j = 25°C K Package H Package			 0.1 0.03			 0.1 0.03		 A A
$\frac{\Delta V_{OUT}}{\Delta Temp}$	Temperature Stability	$-55°C \leq T_j \leq +150°C$			1	2		1		%
$\frac{\Delta V_{OUT}}{\Delta Time}$	Long Term Stability	T_A = 125°C			0.3	1		0.3	1	%
e_n	RMS Output Noise (% of V_{OUT})	T_A = 25°C, 10Hz ≤ f ≤ 10kHz			0.001			0.001		%
Θ_{jc}	Thermal Resistance Junction to Case	H Package K Package			12 2.3	15 3		12 2.3	15 3	°C/W °C/W

ELECTRICAL CHARACTERISTICS (See Note 1) LT317AHV/LM317HV

SYMBOL	PARAMETER	CONDITIONS		LT317AHV MIN	LT317AHV TYP	LT317AHV MAX	LM317HV MIN	LM317HV TYP	LM317HV MAX	UNITS
V_{REF}	Reference Voltage	I_{OUT} = 10mA T_j = 25°C		1.238	1.250	1.262				V
		3V ≤ (V_{IN} − V_O) ≤ 60V 10mA ≤ I_{OUT} ≤ I_{max}, P ≤ P_{max}	●	1.225	1.250	1.270	1.20	1.25	1.30	V
$\frac{\Delta V_{OUT}}{\Delta V_{IN}}$	Line Regulation	3V ≤ (V_{IN} − V_{OUT}) ≤ 60V (See Note 2)			0.005	0.01		0.01	0.04	%/V
			●		0.01	0.02		0.02	0.07	%/V
$\frac{\Delta V_{OUT}}{\Delta I_{OUT}}$	Load Regulation	10mA ≤ I_{OUT} ≤ I_{max}, (See Note 2) V_O ≤ 5V V_O ≥ 5V			5 0.1	25 0.5		5 0.1	25 0.5	mV %
		V_O ≤ 5V V_O ≥ 5V	● ●		20 0.3	50 1		20 0.3	70 1.5	mV %
	Thermal Regulation	T_A = 25°C, 20msec Pulse			0.002	0.02		0.04	0.07	%/W
	Ripple Rejection	V_O = 10V, f = 120Hz C_{ADJ} = 0	●		65			65		dB
		C_{ADJ} = 10μF	●	66	80		66	80		dB
I_{ADJ}	Adjust Pin Current		●		50	100		50	100	μA
ΔI_{ADJ}	Adjust Pin Current Change	10mA ≤ I_{OUT} ≤ I_{max} 2.5V ≤ (V_{IN} − V_{OUT}) ≤ 60V	●		0.2	5		0.2	5	μA
I_{min}	Minimum Load Current	(V_{IN} − V_{OUT}) = 60V	●		3.5	12		3.5	12	mA
	Current Limit	(V_{IN} − V_{OUT}) ≤ 15V K Package H Package	● ●	1.5 0.5	2.2 0.8		1.5 0.5	2.2 0.8		A A
		(V_{IN} − V_{OUT}) = 60V, T_j = 25°C K Package H Package			0.1 0.03			0.1 0.03		A A
$\frac{\Delta V_{OUT}}{\Delta Temp}$	Temperature Stability	0°C ≤ T_j ≤ 125°C			1	2		1		%
$\frac{\Delta V_{OUT}}{\Delta Time}$	Long Term Stability	T_A = 125°C			0.3	1		0.3	1	%
e_n	RMS Output Noise (% of V_{OUT})	T_A = 25°C, 10Hz ≤ f ≤ 10kHz			0.001			0.001		%
Θ_{jc}	Thermal Resistance Junction to Case	H Package K Package			12 2.3	15 3		12 2.3	15 3	°C/W °C/W

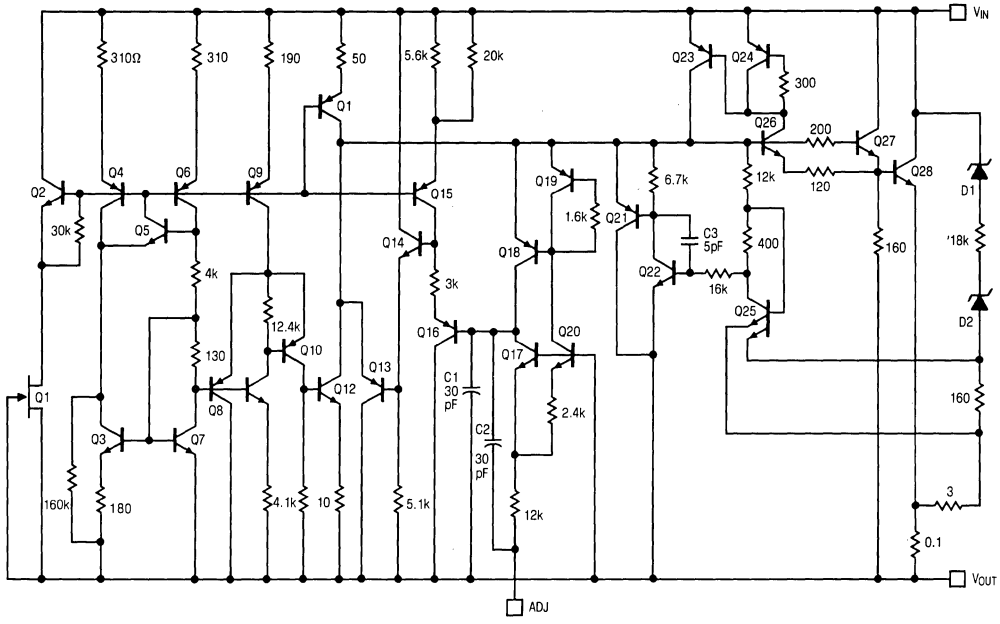
The ● denotes the specifications which apply over the full operating temperature range.

The shaded electrical specifications indicate those parameters which have been improved or guaranteed test limits provided for the first time.

Note 1: Unless otherwise specified, these specifications apply for (V_{IN} − V_{OUT}) = 5V: and I_{OUT} = 0.1A for the TO-39 and I_{OUT} = 0.5A for the TO-3 package. Although power dissipation is internally limited, these specifications are applicable for power dissipations of 2W for the TO-39, and 20W for the TO-3. I_{MAX} is 1.5A for the TO-3 package and 0.5A for the TO-39.

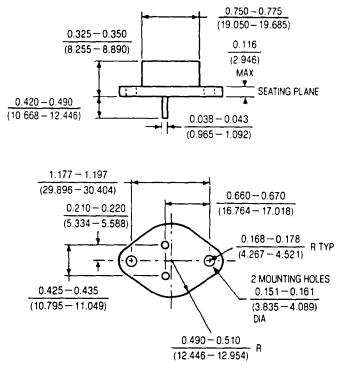
Note 2: Regulation is measured at constant junction temperature, using pulse testing with a low duty cycle. Changes in output voltage due to heating effects are covered under the specification for thermal regulation.

SCHEMATIC DIAGRAM



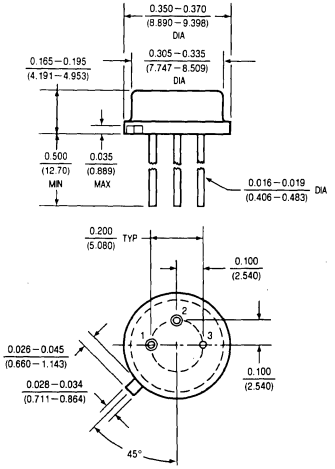
PACKAGE DESCRIPTION

K Package TO-3 STEEL Metal Can



	T_j max.	θ_{ja}	θ_{jc}
117AHV 117HV	150°C	35°C/W	3°C/W
317AHV 317HV	125°C	35°C/W	3°C/W

H Package 3-Lead Metal Can



	T_j max.	θ_{ja}	θ_{jc}
117AHV 117HV	150°C	150°C/W	15°C/W
317AHV 317HV	125°C	150°C/W	15°C/W

5 Volt, 3 Amp Voltage Regulator

FEATURES

- *Guaranteed* 1% Initial Tolerance of Output Voltage
- 3 Amp Output Current
- 30 Watt
- Full Internal Overload Protection
- 100% Burn-in in Thermal Limit

APPLICATIONS

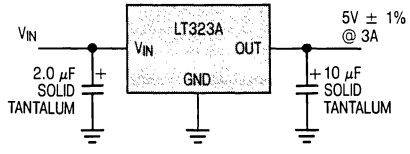
- Local 5V Regulators
- On Card Regulation
- Lab Supplies
- Instrumentation Supplies

DESCRIPTION

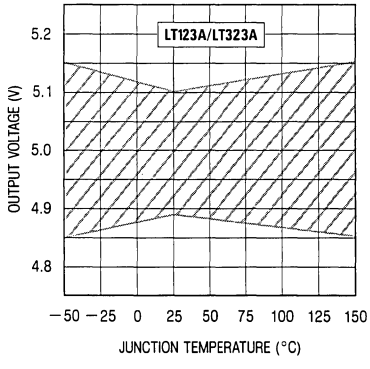
The LT123A/LT323A is an improved version of the popular LM123/LM323 5 Volt, 3 Amp Regulator. These new devices offer maximum initial output voltage tolerance of 1% and maintain a maximum tolerance of 3% over worst case operating conditions. Line and load regulation are also improved by a factor of 2. These tightened specifications ease design and application problems since safety margins are improved. Also, error budgets in other parts of the system can be expanded, and output voltages at the end of long supply runs can be more accurately maintained.

The LT123A/LT323A incorporates Linear Technology's advanced design, process and test techniques for improved quality and reliability over similar device types. Specifically, all devices are burned in by shorting the output, thereby forcing the regulator into its current limit and eventually, thermal limit. This ensures that all device protection features are functional. A graph of the worst case output voltage, taking into account temperature, load and line variations, and power dissipation is shown below. For higher output current requirements, see the LT1003, 5V, 5A regulator data sheet.

Precision 5 Volt Regulator



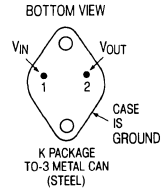
Worst Case Output Voltage



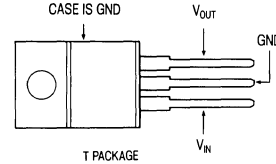
ABSOLUTE MAXIMUM RATINGS

Input Voltage ..... 20 Volts
Power Dissipation ..... Internally Limited
Operating Junction Temperature Range
LT123A/LM123 ..... −55°C to 150°C
LT323A/LM323 ..... 0°C to 125°C
Storage Temperature Range
LT123A/LM123 ..... −65°C to 150°C
LT323A/LM323 ..... −65°C to 150°C
Lead Temperature (Soldering, 10 sec.)..... 300°C

PACKAGE/ORDER INFORMATION



ORDER PART NO.
LT123AK
LT323AK
LM123K
LM323K



LT323AT
LM323T

PRECONDITIONING:

Thermal limit burn-in for all devices.

ELECTRICAL CHARACTERISTICS (See Note 1)

SYMBOL	PARAMETER	CONDITIONS		LT123A MIN	LT123A TYP	LT123A MAX	LM123 MIN	LM123 TYP	LM123 MAX	UNITS
V_{OUT}	Output Voltage	$T_j = 25°C$, $V_{IN} = 7.5V$, $I_{OUT} = 0$		4.95	5.0	5.05	4.7	5.0	5.3	V
		$7.5V \leq V_{IN} \leq 15V$, $T_{MIN} \leq T_j \leq T_{MAX}$ $0 \leq I_{OUT} \leq 3A$, $P \leq 30W$	●	4.85	5.0	5.15	4.6		5.4	V
$\frac{\Delta V_{OUT}}{\Delta V_{IN}}$	Line Regulation	$T_j = 25°C$, $7.5V \leq V_{IN} \leq 15V$ (See Note 1)			5	10		5	25	mV
$\frac{\Delta V_{OUT}}{\Delta I_{OUT}}$	Load Regulation	$T_j = 25°C$, $V_{IN} = 7.5V$ $0 \leq I_{OUT} \leq 3A$ (See Note 1)			25	50		25	100	mV
I_Q	Quiescent Current	$7.5V \leq V_{IN} \leq 15V$, $0 \leq I_{OUT} \leq 3A$	●		12	20		12	20	mA
e_n	Output Noise Voltage	$T_j = 25°C$, $10Hz \leq f \leq 100kHz$			40			40		μV_{rms}
I_{SC}	Short Circuit Current Limit	$T_j = 25°C$, $V_{IN} = 15V$ $V_{IN} = 7.5V$			3 4	4.5 6		3 4	4.5 5	A A
	Long Term Stability of Output Voltage					35			35	mV
θ_{JC}	Thermal Resistance Junction to Case	K Package			1.8	2.5		1.8		°C/W

The ● denotes the specifications which apply over the full operating temperature range.

Note 1: Load and line regulation are tested with pulsed low duty cycle techniques where pulse width ≤ 1msec and duty cycle ≤ 5%.

Note 2: $T_{min} = -55°C$ for the LT123A/LM123 and 0°C for LT323A/LM323. $T_{max} = 150°C$ for LT123A/LM123 and 125°C for LT323A/LM323.

ELECTRICAL CHARACTERISTICS (See Note 1)

SYMBOL	PARAMETER	CONDITIONS		LT323A MIN	LT323A TYP	LT323A MAX	LM323 MIN	LM323 TYP	LM323 MAX	UNITS
V_{OUT}	Output Voltage	$T_J = 25°C$, $V_{IN} = 7.5V$, $I_{OUT} = 0$		4.95	5.0	5.05	4.8	5.0	5.2	V
		$7.5V \leq V_{IN} \leq 15V$, $T_{MIN} \leq T_J \leq T_{MAX}$ $0 \leq I_{OUT} \leq 3A$, $P \leq 30W$ (Note 2)	●	4.85	5.0	5.15	4.75	5.0	5.25	V
$\frac{\Delta V_{OUT}}{\Delta V_{IN}}$	Line Regulation	$T_J = 25°C$, $7.5V \leq V_{IN} \leq 15V$ (See Note 1)			5	10		5	25	mV
$\frac{\Delta V_{OUT}}{\Delta I_{OUT}}$	Load Regulation	$T_J = 25°C$, $V_{IN} = 7.5V$ $0 \leq I_{OUT} \leq 3A$ (See Note 1)			25	50		25	100	mV
I_Q	Quiescent Current	$7.5V \leq V_{IN} \leq 15V$, $0 \leq I_{OUT} \leq 3A$	●		12	20		12	20	mA
e_n	Output Noise Voltage	$T_J = 25°C$, $10Hz \leq f \leq 100kHz$			40			40		μV_{rms}
I_{SC}	Short Circuit Current Limit	$T_J = 25°C$, $V_{IN} = 15V$ $V_{IN} = 7.5V$			3 4	4.5 6		3 4	4.5 5	A A
	Long Term Stability of Output Voltage					35			35	mV
θ_{JC}	Thermal Resistance Junction to Case	K Package T Package			1.8 2.5	2.5 4.0		1.8 3.0		°C/W °C/W

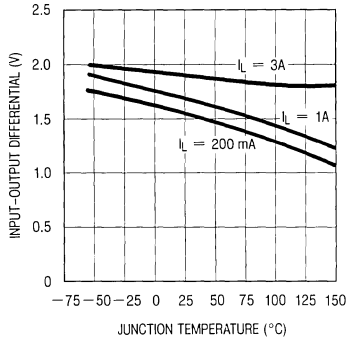
The ● denotes the specifications which apply over the full operating temperature range.

Note 1: Load and line regulation are tested with pulsed low duty cycle techniques where pulse width ≤ 1msec and duty cycle ≤ 5%.

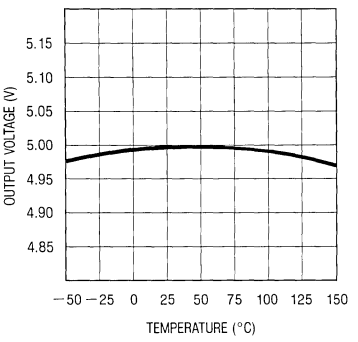
Note 2: $T_{min} = -55°C$ for the LT123A/LM123 and 0°C for LT323A/LM323. $T_{max} = +150°C$ for LT123A/LM123 and $+125°C$ for LT323A/LM323.

TYPICAL PERFORMANCE CHARACTERISTICS

Dropout Voltage

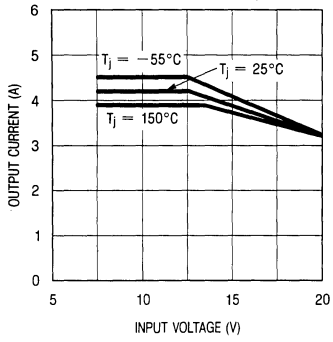


Output Voltage Temperature Drift

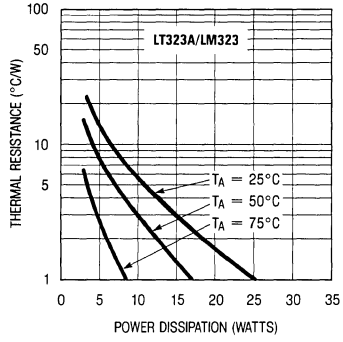


TYPICAL PERFORMANCE CHARACTERISTICS

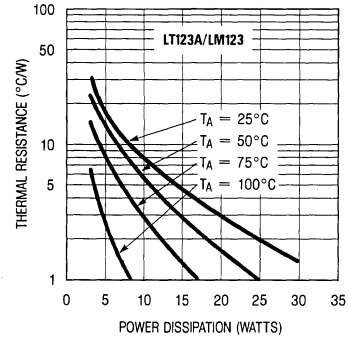
Peak Available Output Current



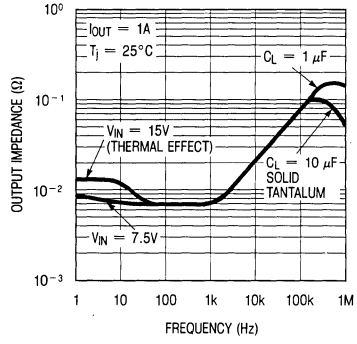
Suggested Heat Sink Thermal Resistance



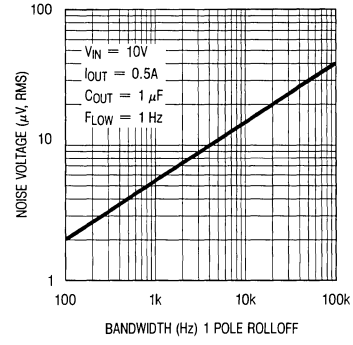
Suggested Heat Sink Thermal Resistance



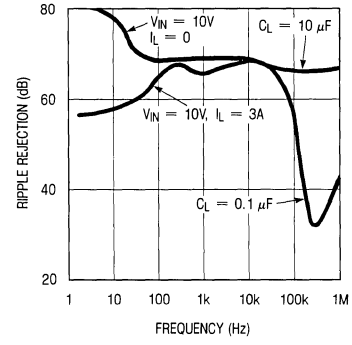
Output Impedance



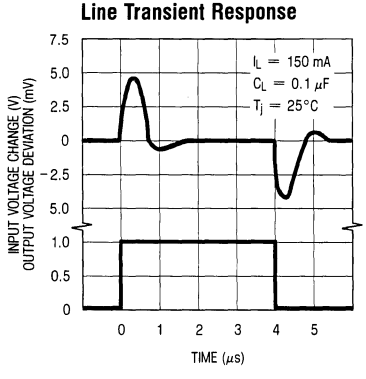
Output Noise Voltage



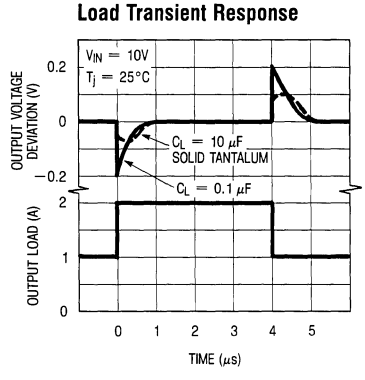
Ripple Rejection



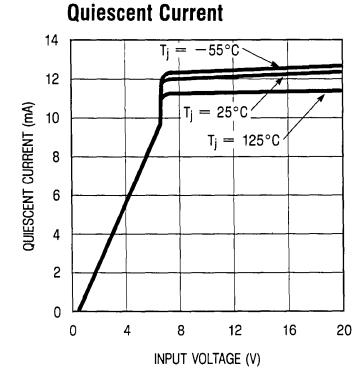
Line Transient Response



Load Transient Response



Quiescent Current

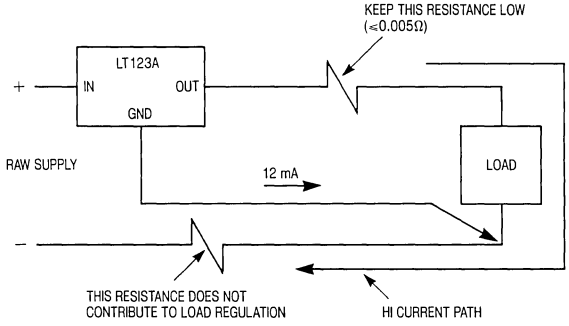


APPLICATIONS INFORMATION

Bypass Capacitors: The LT123A does not require an output capacitor for resistive loads. For almost all applications, however, a 1μF or larger solid tantalum capacitor should be used at the output within 2" of the regulator to improve the output impedance at high frequencies. For applications where very low high frequency impedance is required, a 10μF solid tantalum output capacitor is recommended. Total output capacitance either local or distributed may be increased without limit.

A 2μF or larger solid tantalum capacitor or a 25μF aluminum capacitor, must be used at the input if the regulator is more than 4" away from the large rectifier capacitor.

Avoiding Ground Loops: For best regulation, the ground pin of the LT123A should be tied directly to the load point as shown. This prevents excess drop in load voltage caused by load current flowing through the ground return lead. This is essentially a Kelvin connection for the low side of the regulator. A Kelvin connection cannot be made for the high output of regulator because only three pins are available on the package. Therefore, every attempt should be made to minimize the resistance between the output pin of the regulator and the load. #18 gauge hookup wire has a resistance of 0.006 ohms per foot. This translates to 0.36% change in load voltage at full load current. The LT123A is specified at 1% maximum load regulation, so one foot of wire represents a significant loss of regulation. If connectors are used, careful consideration must be given to contact resistance, especially if the connector is subjected to nasty ambients, vibration, or multiple insertions.



Raw Supply: Transformer, diode, and capacitor selection for the raw supply to the LT123A is very important because of the conflicting requirements for reliability, efficiency, and resistance to "brown-out" conditions. High secondary voltage on the transformer will cause unnecessarily high power dissipation in the regulator. Too low a secondary voltage will cause the regulator output to drop out of regulation with only a small reduction in AC mains voltage. The following formula gives a good starting point for transformer selection. This formula assumes a center tapped transformer, using two rectifier diodes.

where:

V_{OUT} = 5V
V_{DO} = Minimum input-output differential of the regulator
V_{RECT} = Rectifier forward drop at $3I_{OUT}$
V_{RIP} = ½ p-p capacitor ripple voltage

$$\approx \frac{(5.3 \times 10^{-3})\,(I_{OUT})}{2C}$$

V_{NOM} = Rated line voltage for the transformer (RMS)
V_{LOW} = Lowest expected line voltage (RMS)
I_{OUT} = DC output current

*1.1 is a nominal load regulation factor for the transformer

APPLICATIONS INFORMATION

Example: $I_{OUT} = 2.5A$, $V_{OUT} = 5V$
Assume: $V_{DO} = 2.5V$, $V_{RECT} = 1.1V$, $C = 8{,}000\mu F$
$V_{NOM} = 115V$, $V_{LOW} = 0.88V$

$$V_{RIP} = \frac{(5.3 \times 10^{-3})(2.5)}{2(8 \times 10^{-3})} = 0.83V$$

$$V_{RMS} = \left(\frac{5 + 2.5 + 1.1 + 0.83}{\sqrt{2}}\right)\left(\frac{115}{05}\right) \quad (1.1)$$

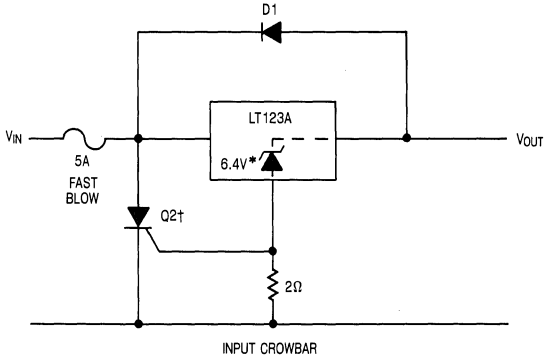
$$= 8.03\ V_{RMS}$$

$$V_{RMS} = \left(\frac{V_{OUT} + V_{DO} + V_{RECT} + V_{RIP})}{\sqrt{2}}\right)\left(\frac{V_{NOM}}{V_{LOW}}\right) \quad (1.1^*)$$

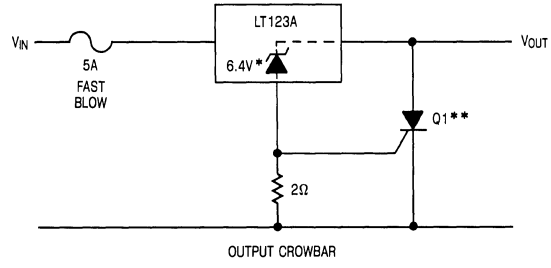
$$I_{RMS} = (I_{OUT})(1.2)$$

The filter capacitor should be at *least* 2000μF per amp of load current to minimize capacitor heating and ripple voltage. The diodes should be rated at 5–6 amps even though their average current is only 1.5A at full rated load current. The reason for this is that although the *average* current is 1.5A, the RMS current is typically twice this value. In addition, the diode must withstand very high surge currents during power turn-on. This surge can be 10–20 times the DC rating of the supply, depending on capacitor size and wiring resistance and inductance.

TYPICAL APPLICATIONS



INPUT CROWBAR



OUTPUT CROWBAR

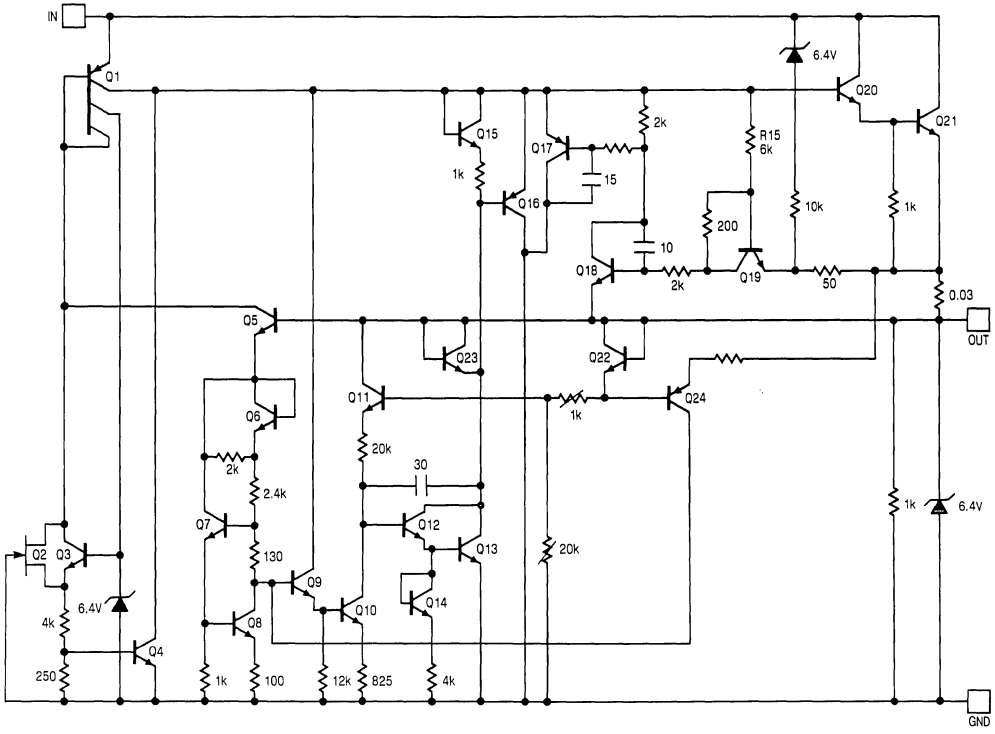
† Q2 AND D1 MUST WITHSTAND LARGE SURGE CURRENTS UNTIL THE 5A FUSE BLOWS. PEAK SURGE CURRENT IS LIMITED ONLY BY THE FUSE, WIRING, AND FILTER CAP RESISTANCE.

†† TRIP POINT IS APPROXIMATELY 7.3V.

* THE 6.4V ZENER IS INTERNAL TO THE LT123A.

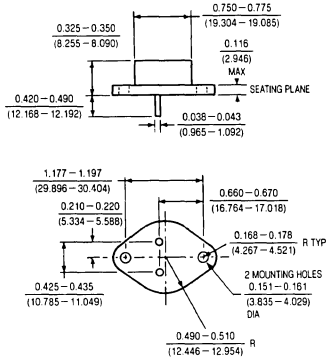
** Q1 MUST BE ABLE TO WITHSTAND CONTINUOUS CURRENTS OF 5A IF ADDITIONAL SYSTEM SHUTDOWN IS NOT USED.

SCHEMATIC DIAGRAM



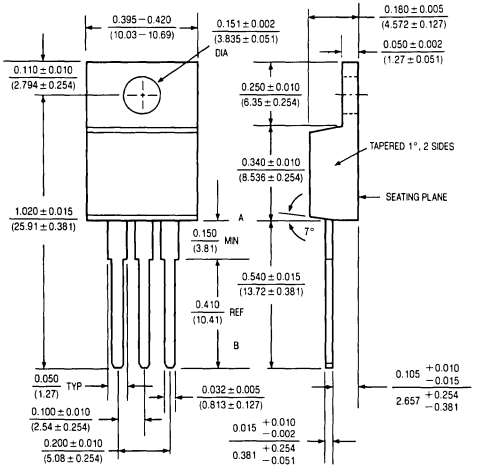
PACKAGE DESCRIPTION

K Package STEEL METAL CAN



	T_j max.	θ_{ja}	θ_{jc}
LT123AK LM123K	150°C	35°C/W	1.8°C/W
LT323AK LM323K	125°C	35°C/W	1.8°C/W

T Package TO-220



	T_j max.	θ_{ja}	θ_{jc}
LT323AT LM323T	125°C	50°C/W	2.5°C/W

Negative Adjustable Regulator

FEATURES

- *Guaranteed* 1% Initial Voltage Tolerance
- *Guaranteed* 0.01%/V Line Regulation
- *Guaranteed* 0.5% Load Regulation
- *Guaranteed* 0.02%/W Thermal Regulation
- 100% Burn-in in Thermal Limit

APPLICATIONS

- Adjustable Power Supplies
- System Power Supplies
- Precision Voltage/Current Regulators
- On-Card Regulators

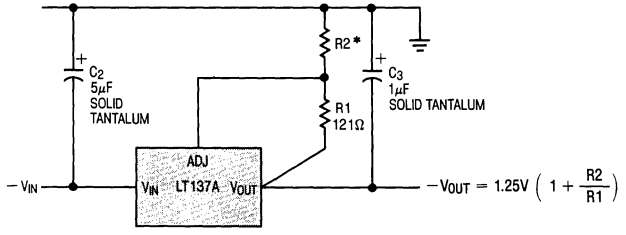
DESCRIPTION

The LT137A/LT337A negative adjustable regulators will deliver up to 1.5Amps output current over an output voltage range of −1.2V to −37V. Linear Technology has made significant improvements in these regulators compared to previous devices, such as better line and load regulation, and a maximum output voltage error of 1%.

Every effort has been made to make these devices easy to use and difficult to damage. Internal current and power limiting coupled with true thermal limiting prevents device damage due to overloads or shorts, even if the regulator is not fastened to a heat sink.

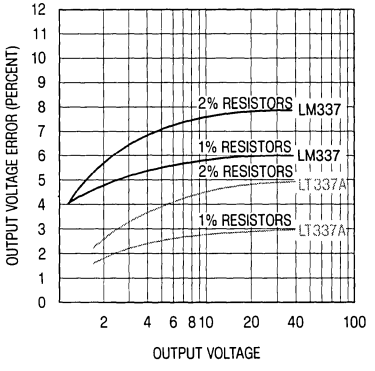
Maximum reliability is attained with Linear Technology's advanced processing techniques combined with a 100% burn-in in the thermal limit mode. This assures that all device protection circuits are working and eliminates field failures experienced with other regulators that receive only standard electrical testing.

Negative Regulator



$$*R2 = R1\left(\frac{|V_{OUT}|}{1.25V} - 1\right)$$

Output Voltage Error



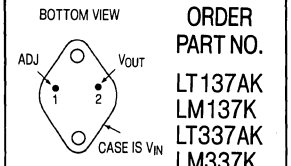
ABSOLUTE MAXIMUM RATINGS

Power Dissipation ..... Internally Limited
Input to Output Voltage Differential 40V
Operating Junction Temperature Range
LT137A/LM137 ..... −55°C to 150°C
LT337A/LM337 ..... 0°C to 125°C
Storage Temperature Range
LT137A/LM137 ..... −65°C to 150°C
LT337A/LM337 ..... −65°C to 150°C
Lead Temperature (Soldering, 10 sec.)..... 300°C

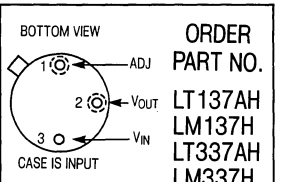
PRECONDITIONING

100% THERMAL LIMIT BURN-IN

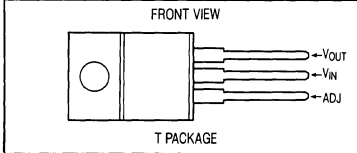
PACKAGE/ORDER INFORMATION



ORDER PART NO.
LT137AK
LM137K
LT337AK
LM337K



ORDER PART NO.
LT137AH
LM137H
LT337AH
LM337H



ORDER PART NO.
LT337AT
LM337T

ELECTRICAL CHARACTERISTICS (See Note 1)

SYMBOL	PARAMETER	CONDITIONS		LT137A MIN	LT137A TYP	LT137A MAX	LM137 MIN	LM137 TYP	LM137 MAX	UNITS
V_{REF}	Reference Voltage	$\lvert V_{IN}-V_{OUT}\rvert = 5V$, $I_{OUT} = 10mA$, $T_j = 25°C$		−1.238	−1.250	−1.262	−1.225	−1.250	−1.275	V
		$3V \leq \lvert V_{IN} - V_{OUT}\rvert \leq 40V$ $10mA \leq I_{OUT} \leq I_{MAX}$, $P \leq P_{MAX}$	●	−1.220	−1.250	−1.280	−1.200	−1.250	−1.300	V
$\frac{\Delta V_{OUT}}{\Delta I_{OUT}}$	Load Regulation	$10mA \leq I_{OUT} \leq I_{MAX}$, (See Note 2)								
		$T_j = 25°C$, $\lvert V_{OUT}\rvert \leq 5V$			5	25		15	25	mV
		$T_j = 25°C$, $\lvert V_{OUT}\rvert \geq 5V$			0.1	0.5		0.3	0.5	%
		$\lvert V_{OUT}\rvert \leq 5V$	●		10	50		20	50	mV
		$\lvert V_{OUT}\rvert \geq 5V$	●		0.2	1.0		0.3	1.0	%
$\frac{\Delta V_{OUT}}{\Delta V_{IN}}$	Line Regulation	$3V \leq \lvert V_{IN}-V_{OUT}\rvert \leq 40V$, (See Note 2) $T_j = 25°C$			0.005	0.01		0.01	0.02	%/V
			●		0.01	0.03		0.02	0.05	%/V
	Ripple Rejection	$V_{OUT} = -10V$, f = 120Hz $C_{ADJ} = 0$		60	66			60		dB
		$C_{ADJ} = 10\mu F$	●	70	80		66	77		dB
	Thermal Regulation	$T_j = 25°C$, 10msec Pulse			0.002	0.02		0.002	0.02	%/W
I_{ADJ}	Adjust Pin Current		●		65	100		65	100	μA
ΔI_{ADJ}	Adjust Pin Current Change	$10mA \leq I_{OUT} \leq I_{MAX}$	●		0.2	2		0.5	5	μA
		$3V \leq V_{IN} \quad V_{OUT} \leq 40V$	●		1.0	5		2	5	μA
	Minimum Load Current	$\lvert V_{IN}-V_{OUT}\rvert \leq 40V$	●		2.5	5.0		2.5	5.0	mA
		$\lvert V_{IN}-V_{OUT}\rvert \leq 10V$	●		1.2	3.0		1.2	3.0	mA
I_{SC}	Current Limit	$\lvert V_{IN}-V_{OUT}\rvert \leq 15V$, K and T Package	●	1.5	2.2	3.2	1.5	2.2		A
		H Package	●	0.5	0.8	1.5	0.5	0.8		A
		$\lvert V_{IN}-V_{OUT}\rvert = 40V$, K and T Package		0.24	0.4	1.0	0.24	0.4		A
		$T_j = 25°C$ H Package		0.15	0.25	0.5	0.15	0.25		A
$\frac{\Delta V_{OUT}}{\Delta Temp}$	Temperature Stability of Output Voltage (Note 4)	$T_{MIN} \leq T \leq T_{MAX}$	●		0.6	1.5		0.6		%
$\frac{\Delta V_{OUT}}{\Delta Time}$	Long Term Stability	$T_A = 125°C$, 1000 Hours			0.3	1.0		0.3	1.0	%
e_n	RMS Output Noise (% of V_{OUT})	$T_A = 25°C$, $10Hz \leq f \leq 10kHz$			0.003			0.003		%
Θ_{JC}	Thermal Resistance Junction to Case	H Package			12	15		12	15	°C/W
		K Package			2.3	3.0		2.3	3.0	°C/W

ELECTRICAL CHARACTERISTICS (See Note 1)

SYMBOL	PARAMETER	CONDITIONS		LT337A MIN	LT337A TYP	LT337A MAX	LM337 MIN	LM337 TYP	LM337 MAX	UNITS
V_{REF}	Reference Voltage	$\|V_{IN}-V_{OUT}\| = 5V$, $I_{OUT} = 10mA$, $T_j = 25°C$		−1.238	−1.250	−1.262	−1.213	−1.250	−1.287	V
		$3V \leq \|V_{IN} - V_{OUT}\| \leq 40V$ $10mA \leq I_{OUT} \leq I_{MAX}$, $P \leq P_{MAX}$	●	−1.220	−1.250	−1.280	−1.200	−1.250	−1.300	V
$\frac{\Delta V_{OUT}}{\Delta I_{OUT}}$	Load Regulation	$10mA \leq I_{OUT} \leq I_{MAX}$, (See Note 2 & 3)								
		$T_j = 25°C$, $\|V_{OUT}\| \leq 5V$			5	25		15	50	mV
		$T_j = 25°C$, $\|V_{OUT}\| \geq 5V$			0.1	0.5		0.3	1.0	%
		$\|V_{OUT}\| \leq 5V$	●		10	50		20	70	mV
		$\|V_{OUT}\| \geq 5V$	●		0.2	1.0		0.3	1.5	%
$\frac{\Delta V_{OUT}}{\Delta V_{IN}}$	Line Regulation	$3V \leq \|V_{IN}-V_{OUT}\| \leq 40V$, (See Note 2)								
		$T_j = 25°C$			0.005	0.01		0.01	0.04	%/V
			●		0.01	0.03		0.02	0.07	%/V
	Ripple Rejection	$V_{OUT} = -10V$, f = 120Hz								
		$C_{ADJ} = 0$		60	66			60		dB
		$C_{ADJ} = 10\mu F$	●	70	80		66	77		dB
	Thermal Regulation	$T_j = 25°C$, 10msec Pulse			0.002	0.02		0.003	0.04	%/W
I_{ADJ}	Adjust Pin Current		●		65	100		65	100	μA
ΔI_{ADJ}	Adjust Pin Current Change	$10mA \leq I_{OUT} \leq I_{MAX}$	●		0.2	2		0.5	5	μA
		$3V \leq \|V_{IN} - V_{OUT}\| \leq 40V$	●		1.0	5		2	5	μA
	Minimum Load Current	$\|V_{IN}-V_{OUT}\| \leq 40V$	●		2.5	5		2.5	10	mA
		$\|V_{IN}-V_{OUT}\| \leq 10V$	●		1.2	3		1	6	mA
I_{SC}	Current Limit	$\|V_{IN}-V_{OUT}\| \leq 15V$,								
		K and T Package	●	1.5	2.2	3.5	1.5	2.2		A
		H Package	●	0.5	0.8	1.5	0.5	0.8		A
		$\|V_{IN}-V_{OUT}\| = 40V$,								
		K and T Package		0.24	0.5	1.0	0.15	0.4		A
		$T_j = 25°C$ H Package		0.15	0.25	0.5	0.10	0.17		A
$\frac{\Delta V_{OUT}}{\Delta Temp}$	Temperature Stability of Output Voltage (Note 4)		●		0.6	1.5		0.6		%
$\frac{\Delta V_{OUT}}{\Delta Time}$	Long Term Stability	$T_A = 125°C$, 1000 Hours			0.3	1.0		0.3	1.0	%
e_n	RMS Output Noise (% of V_{OUT})	$T_A = 25°C$, $10Hz \leq f \leq 10kHz$			0.003			0.003		%
Θ_{JC}	Thermal Resistance Junction to Case	H Package			12	15		12	15	°C/W
		K Package			2.3	3.0		2.3	3.0	°C/W
		T Package			3	5		3	5	°C/W

The ● denotes the specifications which apply over the full operating temperature range.

The shaded electrical specifications indicate those parameters which have been improved or guaranteed test limits provided for the first time.

Note 1: Unless otherwise indicated, these specifications apply: $|V_{IN} - V_{OUT}| = 5V$; and $I_{OUT} = 0.1A$ for the H package, $I_{OUT} = 0.5A$ for the K and T packages. Power dissipation is internally limited. However, these specifications apply for power dissipation up to 2W for the H package and 20W for the K and T packages. $I_{MAX} = 1.5A$ for the K and T packages, and 0.2A for the H package.

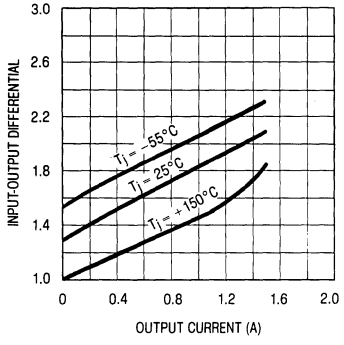
Note 2: Testing is done using a pulsed low duty cycle technique. See thermal regulation specifications for output changes due to heating effects. Load regulation is measured on the output pin at a point 1/8" below the base of the K and H package and at the junction of the wide and narrow portion of the lead on the T package.

Note 3: Load Regulation for the LT337AT is the same as for LM337T.

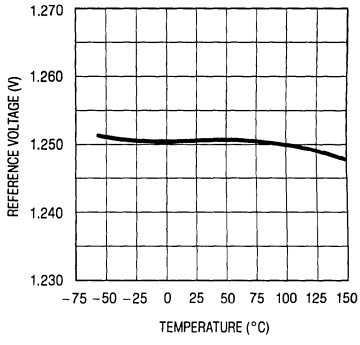
Note 4: Guaranteed on LT137A and LT337A, but not 100% tested in production.

TYPICAL PERFORMANCE CHARACTERISTICS

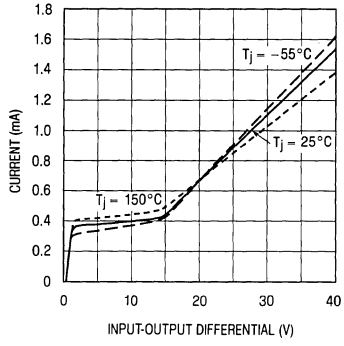
Dropout Voltage



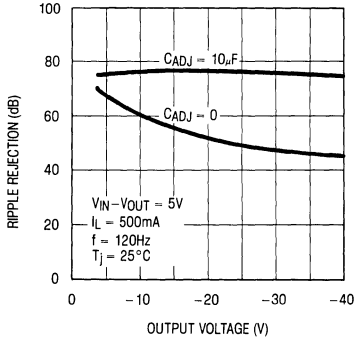
Temperature Stability



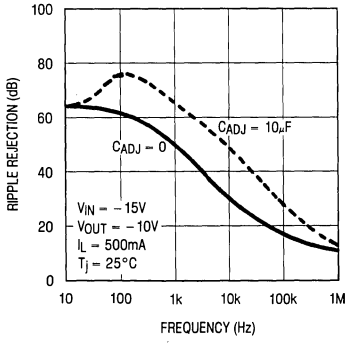
Minimum Load Current



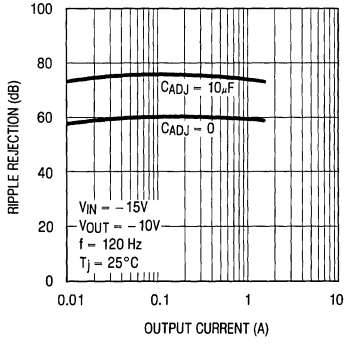
Ripple Rejection



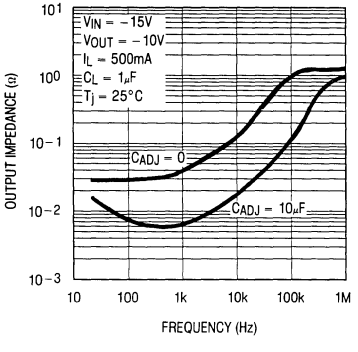
Ripple Rejection



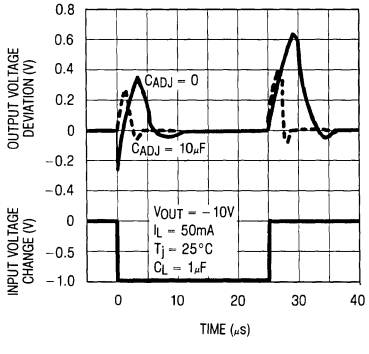
Ripple Rejection



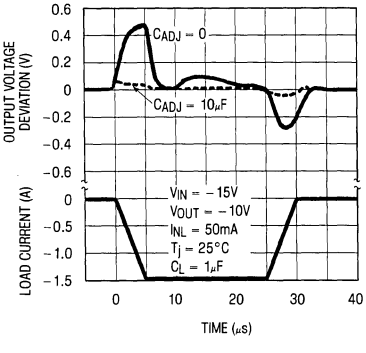
Output Impedance



Line Transient Response

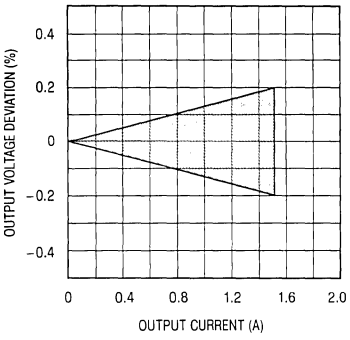


Load Transient Response



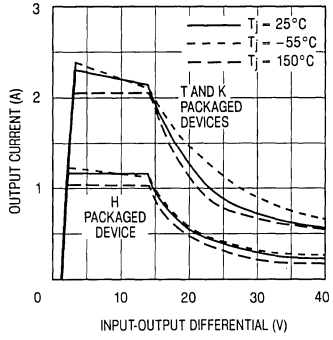
TYPICAL PERFORMANCE CHARACTERISTICS

Load Regulation*

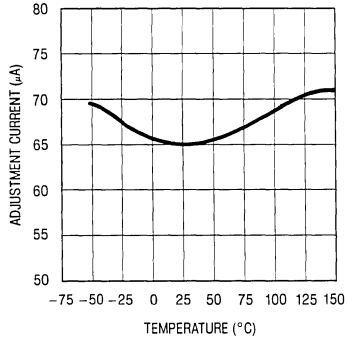


*The LT137A/337A has load regulation compensation which makes the typical unit read close to zero. This band represents the typical production spread.

Current Limit



Adjustment Current



APPLICATION INFORMATION

Output Voltage: The output voltage is determined by two external resistors, R_1 & R_2 (see Figure 1). The exact formula for the output voltage is:

$$V_{OUT} = V_{Ref}\left(1 + \frac{R_2}{R_1}\right) + I_{ADJ}(R_2)$$

Where: V_{Ref} = Reference Voltage, I_{ADJ} = Adjustment Pin Current. In most applications, the second term is small enough to be ignored, typically about 0.5% of V_{OUT}. In more critical applications, the exact formula should be used, with I_{ADJ} equal to 65μa. Solving for R_2 yields:

$$R_2 = \frac{V_{OUT} - V_{Ref}}{\frac{V_{Ref}}{R_1} + I_{ADJ}}$$

Smaller values of R_1 and R_2 will reduce the influence of I_{ADJ} on the output voltage, but the no-load current drain on the regulator will be increased. Typical values for R_1 are between 100Ω and 300Ω, giving 12.5mA and 4.2mA no-load current respectively. There is an additional consideration in selecting R_1, the minimum load current specification of the regulator. The operating current of the LT137A flows from input to output. If this current is not absorbed by the load, the output of the regulator will rise above the regulated value. The current drawn by R_1 and R_2 is normally high enough to absorb the current, but care must be taken in no-load situations where R_1 and R_2 have high values. The maximum value for the operating current, which must be absorbed, is 5mA for the LT137A. If input-output voltage differential is less than 10V, the operating current that must be absorbed drops to 3mA.

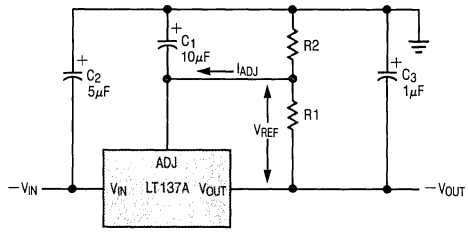


Figure 1

EXAMPLES:

1. A precision 10V regulator to supply up to 1Amp load current.
   a. Select R_1 = 100Ω to minimize effect of I_{ADJ}
   b. Calculate $R_2 = \frac{V_{OUT} - V_{Ref}}{\frac{V_{Ref}}{R_1} - I_{ADJ}} = \frac{10V - 1.25V}{\frac{1.25V}{100\Omega} - 65\mu A} = 704\Omega$
2. A 15V regulator to run off batteries and supply 50mA. V_{IN} MAX = 25V
   a. To minimize battery drain, select R_1 as high as possible

$$R_1 = \frac{1.25V}{3mA} = 417\Omega, \text{ use } 404\Omega, 1\%$$

b. The high value for R_1 will exaggerate the error due to I_{ADJ}, so the exact formula to calculate R_2 should be used.

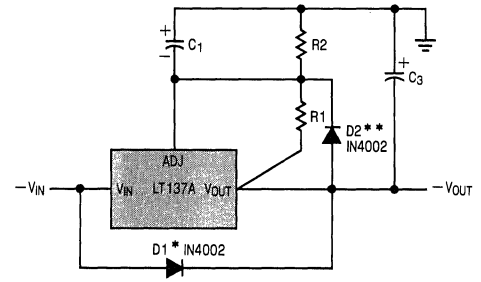
$$R_2 = \frac{V_{OUT} - V_{Ref}}{\frac{V_{Ref}}{R_1} - I_{ADJ}} = \frac{15V - 1.25V}{\frac{1.25V}{404\Omega} - 65 \times 10^{-6}} = 4539\Omega$$

Use $R_2 = 4530\Omega$

Capacitors and Protection Diodes: An output capacitor, C3, is required to provide proper frequency compensation of the regulator feedback loop. A 1μF or larger solid tantalum capacitor is generally sufficient for this purpose if the 1MHz impedance of the capacitor is 2Ω or less. High Q capacitors, such as Mylar, are not recommended because they tend to reduce the phase margin at light load currents. Aluminum electrolytic capacitors may also be used, but the minimum value should be 10μF to ensure a low impedance at 1MHz. The output capacitor should be located within a few inches of the regulator to keep lead impedance to a minimum. The following caution should be noted: if the output voltage is greater than 6V and an output capacitor greater than 20μF has been used, it is possible to damage the regulator if the input voltage becomes shorted, due to the output capacitor discharging into the regulator. This can be prevented by using diode DI (see Figure 2) between the input and the output.

The input capacitor, C2, is only required if the regulator is more than 4 inches from the raw supply filter capacitor.

Bypassing the Adjustment Pin: The adjustment pin of the LT137A may be bypassed with a capacitor to ground, C1, to reduce output ripple, noise, and impedance. These parameters scale directly with output voltage if the adjustment pin is not bypassed. A bypass capacitor reduces ripple, noise, and impedance to that of a 1.25V regulator. In a 15V regulator for example, these parameters are improved by 15V/1.25V = 12 to 1. This improvement holds only for those frequencies where the impedance of the bypass capacitor is less than R_1. Ten microfarads is generally sufficient for 60Hz power line applications where the ripple frequency is 120Hz, since $X_C = 130\Omega$. The capacitor should have a voltage rating at least as high as the output voltage of the regulator. Values larger than 10μF may be used, but if the output is larger than 25V, a diode, D2, should be added between the output and adjustment pins (see Figure 2).



* D1 protects the regulator from input shorts to ground. It is required only when C3 is larger than 20μF and V_{OUT} is larger than 6V.

** D2 protects the adjust pin of the regulator from output shorts if C2 is larger than 10μF *and* V_{OUT} is larger than −25V.

Figure 2

Proper Connection of Divider Resistors: The LT137A has an excellent load regulation specification of 0.5% and is measured at a point 1/8" from the bottom of the package. To prevent degradation of load regulation, the resistors which set output voltage, R1 and R2, must be connected as shown in Figure 3. Note that the positive side of the load has a true force and sense (Kelvin) connection, but the negative side of the load does not.

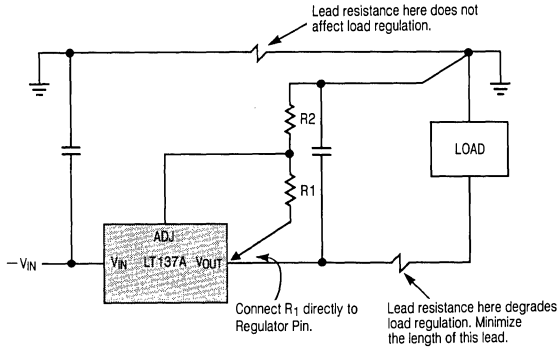


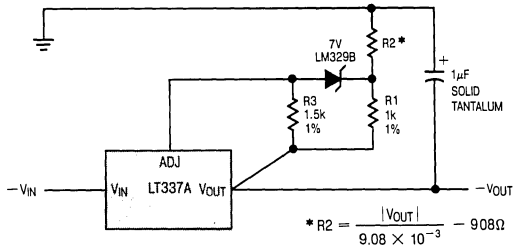
Figure 3

R1 should be connected *directly* to the output lead of the regulator, as close as possible to the specified point 1/8" from the case. R2 should be connected to the positive side of the load separately from the positive (ground) connection to the raw supply. With this arrangement, load regulation is degraded only by the resistance between the regulator output pin and the load. If R1 is connected to the load, regulation will be degraded.

TYPICAL APPLICATIONS

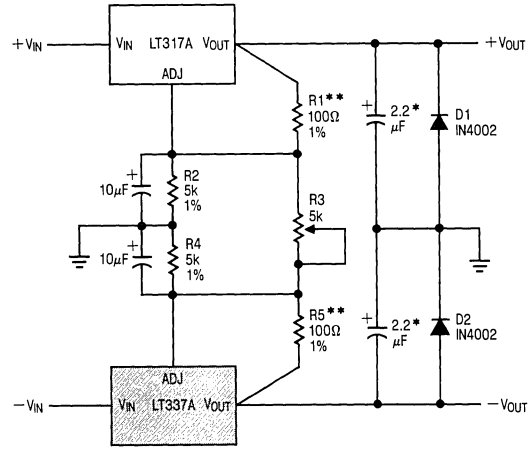
The output stability, load regulation, line regulation, thermal regulation, temperature drift, long term drift, and noise, can be improved by a factor of 6.6 over the standard regulator configuration. This assumes a zener whose drift and noise is considerably better than the regulator itself. The LM329B has 20PPM/°C maximum drift and about 10 times lower noise than the regulator.

High Stability Regulator



In the application shown below, regulators #2 to "N" will track regulator #1 to within ±24mV initially, and to ±60mV over all load, line, and temperature conditions. If any regulator output is shorted to ground, all other outputs will drop to ≈ −2V. Load regulation of regulators 2 to "N" will be improved by $V_{OUT}/1.25V$ compared to a standard regulator, so regulator #1 should be the one which has the lowest load current.

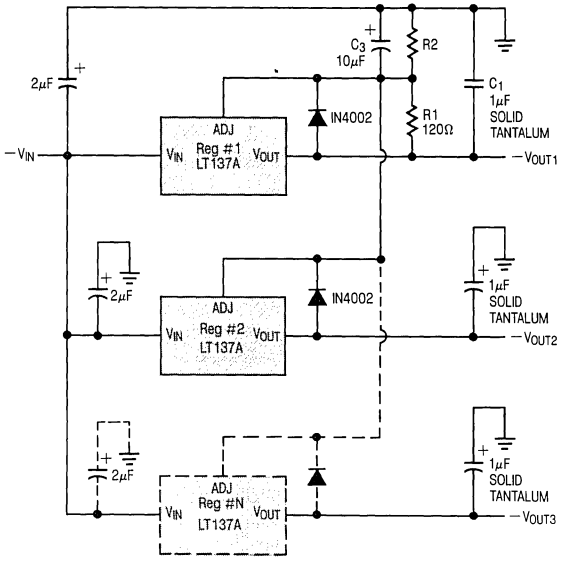
Dual Tracking Supply ±1.25V to ±20V



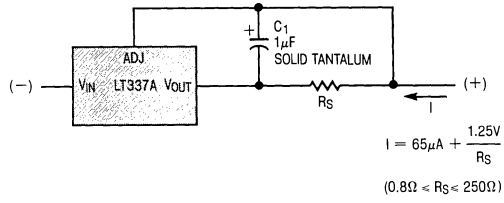
* Solid Tantalum

** R_1 or R_5 may be trimmed slightly to improve tracking

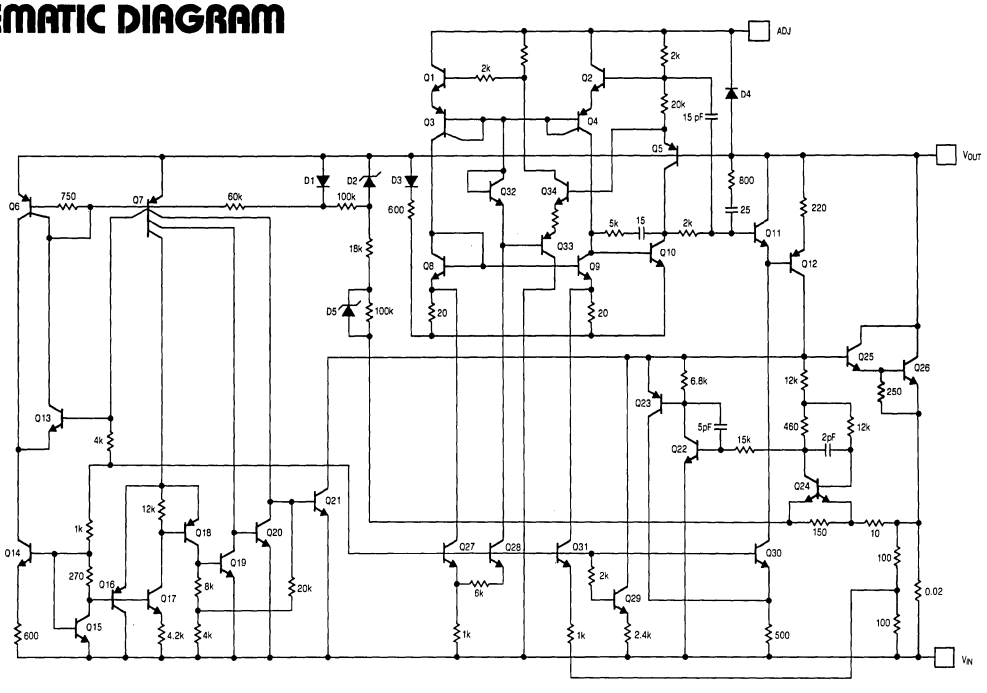
Multiple Tracking Regulators



Current Regulator

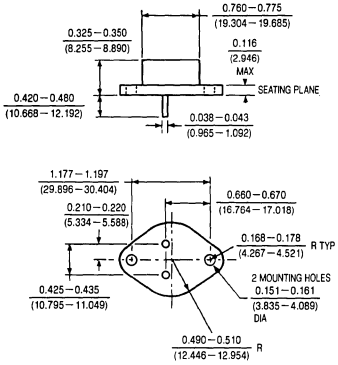


SCHEMATIC DIAGRAM



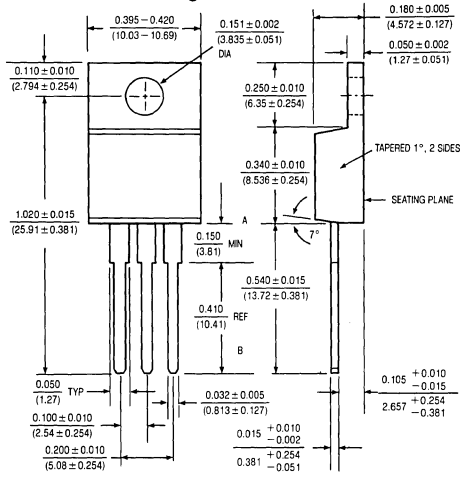
PACKAGE DESCRIPTION

K Package TO-3 STEEL Metal Can



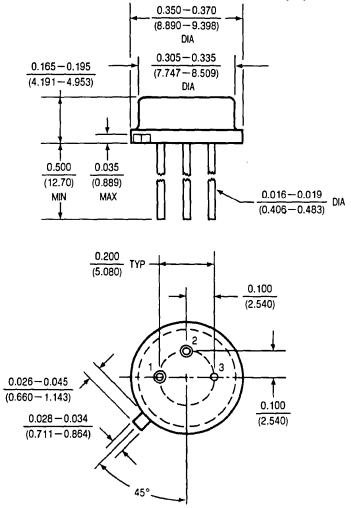
	$T_{J\,MAX}$	Θ_{JC}
137A 137	150°C	3°C/W
337A 337	125°C	3°C/W

T Package TO-220 Plastic



	$T_{J\,MAX}$	Θ_{JC}
337A	125°C	4°C/W
337	125°C	4°C/W

3-Lead Metal Can Package (H)



	$T_{J\,MAX}$	Θ_{JC}
137A 137	150°C	15°C/W
337A 337	125°C	15°C/W

High Voltage Negative Adjustable Regulators

FEATURES

- 50V Operation
- *Guaranteed* 1% Initial Voltage Tolerance
- *Guaranteed* 0.01%/V Line Regulation
- *Guaranteed* 0.5% Load Regulation
- *Guaranteed* 0.02%/W Thermal Regulation
- 100% Burn-in in Thermal Limit

APPLICATIONS

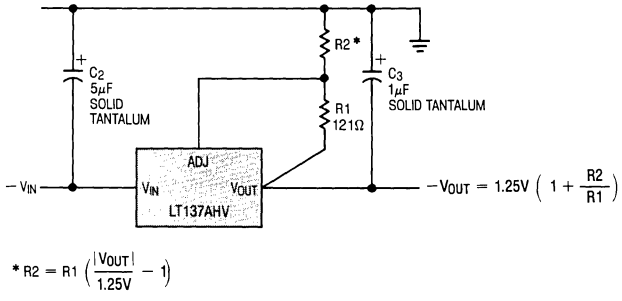
- Adjustable Power Supplies
- System Power Supplies
- Precision Voltage/Current Regulators
- On-Card Regulators

The LT137AHV/LM137HV negative high voltage adjustable regulators will deliver up to 1.5 Amps output current over an output voltage range of −1.2V to −47V. Linear Technology has made significant improvements in these regulators compared to previous devices, such as better line and load regulation, and a maxium output voltage error of 1% for the LT137AHV and LT337AHV.

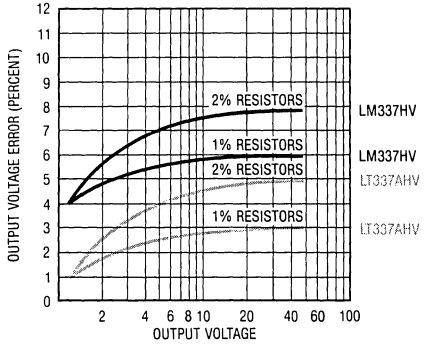
Every effort has been made to make these devices easy to use and difficult to damage. Internal current and power limiting coupled with true thermal limiting prevents device damage due to overloads or shorts, even if the regulator is not fastened to a heat sink.

Maximum reliability is attained with Linear Technology's advanced processing techniques combined with a 100% burn-in in the thermal limit mode. This assures that all device protection circuits are working and eliminates field failures experienced with other regulators that receive only standard electrical testing. For performance curves and applications circuits see the LT137A series data sheet.

Negative Regulator



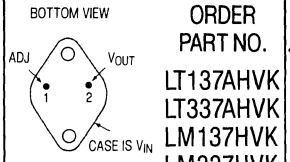
Worst Case Output Voltage Error @ $T_J = 25°C$



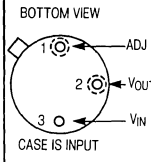
ABSOLUTE MAXIMUM RATINGS

Power Dissipation . . . . . Internally Limited
Input to Output Voltage Differential 50V
Operating Junction Temperature Range
LT137AHV/LM137HV . . . . . −55°C to 150°C
LT337AHV/LM337HV . . . . . 0°C to 125°C
Storage Temperature Range
LT137AHV/LM137HV . . . . . −65°C to 150°C
LT337AHV/LM337HV . . . . . −65°C to 150°C
Lead Temperature (Soldering, 10 sec.) . . . . . 300°C

PACKAGE/ORDER INFORMATION



ORDER PART NO.
LT137AHVK
LT337AHVK
LM137HVK
LM337HVK



ORDER PART NO.
LT137AHVH
LT337AHVH
LM137HVH
LM337HVH

PRECONDITIONING

100% THERMAL LIMIT BURN-IN

ELECTRICAL CHARACTERISTICS (See Note 1)

SYMBOL	PARAMETER	CONDITIONS		LT137AHV MIN	LT137AHV TYP	LT137AHV MAX	LM137HV MIN	LM137HV TYP	LM137HV MAX	UNITS
V_{REF}	Reference Voltage	$\lvert V_{IN}-V_{OUT}\rvert = 5V$, $I_{OUT} = 10mA$, $T_j = 25°C$		−1.238	−1.250	−1.262	−1.225	−1.250	−1.275	V
		$3V \leq \lvert V_{IN}-V_{OUT}\rvert \leq 50V$ $10mA \leq I_{OUT} \leq I_{MAX}$, $P \leq P_{MAX}$	●	−1.220	−1.250	−1.280	−1.200	−1.250	−1.300	V
$\frac{\Delta V_{OUT}}{\Delta I_{OUT}}$	Load Regulation	$10mA \leq I_{OUT} \leq I_{MAX}$, (See Note 2)								
		$T_j = 25°C$, $\lvert V_{OUT}\rvert \leq 5V$			5	25		15	25	mV
		$T_j = 25°C$, $\lvert V_{OUT}\rvert \geq 5V$			0.1	0.5		0.3	0.5	%
		$\lvert V_{OUT}\rvert \leq 5V$	●		10	50		20	50	mV
		$\lvert V_{OUT}\rvert \geq 5V$	●		0.2	1.0		0.3	1.0	%
$\frac{\Delta V_{OUT}}{\Delta V_{IN}}$	Line Regulation	$3V \leq \lvert V_{IN}-V_{OUT}\rvert \leq 50V$ (See Note 2) $T_j = 25°C$			0.005	0.01		0.01	0.02	%/V
			●		0.01	0.03		0.02	0.05	%/V
	Ripple Rejection	$V_{OUT} = -10V$, f = 120Hz $C_{ADJ} = 0$		60	66			60		dB
		$C_{ADJ} = 10\mu F$	●	70	80		66	77		dB
	Thermal Regulation	$T_j = 25°C$, T = 2ms to 12ms			0.002	0.02		0.002	0.02	%/W
I_{ADJ}	Adjust Pin Current		●		65	100		65	100	μA
ΔI_{ADJ}	Adjust Pin Current Change	$10mA \leq I_{OUT} \leq I_{MAX}$	●		0.2	2		0.5	5	μA
		$2.5V \leq \lvert V_{IN}-V_{OUT}\rvert \leq 50V$	●		2	6		3	6	μA
	Minimum Load Current	$\lvert V_{IN}-V_{OUT}\rvert \leq 50V$	●		2.5	5.0		2.5	5.0	mA
		$\lvert V_{IN}-V_{OUT}\rvert \leq 10V$	●		1.2	3.0		1.2	3.0	mA
I_{SC}	Current Limit	$\lvert V_{IN}-V_{OUT}\rvert \leq 13V$ K Package	●	1.5	2.2	3.2	1.5	2.2	3.2	A
		H Package	●	0.5	0.8	1.6	0.5	0.8	1.6	A
		$\lvert V_{IN}-V_{OUT}\rvert = 50V$ K Package		0.2	0.4	0.8	0.2	0.4	0.8	A
		$T_j = 25°C$ H Package		0.1	0.17	0.5	0.1	0.17	0.5	A
$\frac{\Delta V_{OUT}}{\Delta Temp}$	Temperature Stability of Output Voltage (Note 3)	$T_{MIN} \leq T \leq T_{MAX}$	●		0.6	1.5		0.6		%
$\frac{\Delta V_{OUT}}{\Delta Time}$	Long Term Stability	$T_A = 125°C$, 1000 Hours			0.3	1.0		0.3	1.0	%
e_n	RMS Output Noise (% of V_{OUT})	$T_A = 25°C$, 10Hz ≤ f ≤ 10kHz			0.003			0.003		%
Θ_{JC}	Thermal Resistance Junction to Case	H Package			12	15		12	15	°C/W
		K Package			2.3	3.0		2.3	3.0	°C/W

ELECTRICAL CHARACTERISTICS (See Note 1)

SYMBOL	PARAMETER	CONDITIONS		LT337AHV MIN	LT337AHV TYP	LT337AHV MAX	LM337HV MIN	LM337HV TYP	LM337HV MAX	UNITS
V_{REF}	Reference Voltage	$\lvert V_{IN}-V_{OUT}\rvert = 5V$, $I_{OUT} = 10mA$, $T_j = 25°C$		−1.238	−1.250	−1.262	−1.213	−1.250	−1.287	V
		$3V \leq \lvert V_{IN} - V_{OUT}\rvert \leq 50V$ $10mA \leq I_{OUT} \leq I_{MAX}$, $P \leq P_{MAX}$	●	−1.220	−1.250	−1.280	−1.200	−1.250	−1.300	V
$\frac{\Delta V_{OUT}}{\Delta I_{OUT}}$	Load Regulation	$10mA \leq I_{OUT} \leq I_{MAX}$ (See Note 2)								
		$T_j = 25°C$, $\lvert V_{OUT}\rvert \leq 5V$			5	25		15	50	mV
		$T_j = 25°C$, $\lvert V_{OUT}\rvert \geq 5V$			0.1	0.5		0.3	1.0	%
			●		10	50		20	70	mV
		$\lvert V_{OUT}\rvert \geq 5V$	●		0.2	1.0		0.3	1.5	%
$\frac{\Delta V_{OUT}}{\Delta V_{IN}}$	Line Regulation	$3V \leq \lvert V_{IN} - V_{OUT}\rvert \leq 50V$ (See Note 2)								
		$T_j = 25°C$			0.005	0.01		0.01	0.04	%/V
			●		0.01	0.03		0.02	0.07	%/V
	Ripple Rejection	$V_{OUT} = -10V$, f = 120Hz								
		$C_{ADJ} = 0$		60	66			60		dB
		$C_{ADJ} = 10\mu F$	●	70	80		66	77		dB
	Thermal Regulation	$T_j = 25°C$, T = 2ms to 12ms			0.002	0.04		0.003	0.04	%/W
I_{ADJ}	Adjust Pin Current		●		65	100		65	100	μA
ΔI_{ADJ}	Adjust Pin Current Change	$10mA \leq I_{OUT} \leq I_{MAX}$	●		0.2	2		2	5	μA
		$2.5V \leq \lvert V_{IN} - V_{OUT}\rvert \leq 50V$	●		2	6		3	6	μA
	Minimum Load Current	$\lvert V_{IN}-V_{OUT}\rvert \leq 40V$	●		2.5	5		2.5	10	mA
		$\lvert V_{IN}-V_{OUT}\rvert \leq 10V$	●		1.2	3		1	6	mA
I_{SC}	Current Limit	$\lvert V_{IN} - V_{OUT}\rvert \leq 13V$								
		K Package	●	1.5	2.2	3.5	1.5	2.2	3.5	A
		H Package	●	0.5	0.8	1.8	0.5	0.8	1.8	A
		$\lvert V_{IN} - V_{OUT}\rvert = 50V$								
		K Package		0.1	0.4	0.8	0.1	0.4	0.8	A
		H Package		0.05	0.17	0.5	0.05	0.17	0.5	A
$\frac{\Delta V_{OUT}}{\Delta Temp}$	Temperature Stability of Output Voltage (Note 3)		●		0.6	1.5		0.6		%
$\frac{\Delta V_{OUT}}{\Delta Time}$	Long Term Stability	$T_A = 125°C$, 1000 Hours			0.3	1.0		0.3	1.0	%
e_n	RMS Output Noise (% of V_{OUT})	$T_A = 25°C$, 10Hz ≤ f ≤ 10kHz			0.003			0.003		%
Θ_{JC}	Thermal Resistance Junction to Case	H Package			12	15		12	15	°C/W
		K Package			2.3	3.0		2.3	3.0	°C/W

The ● denotes the specifications which apply over the full operating temperature range.

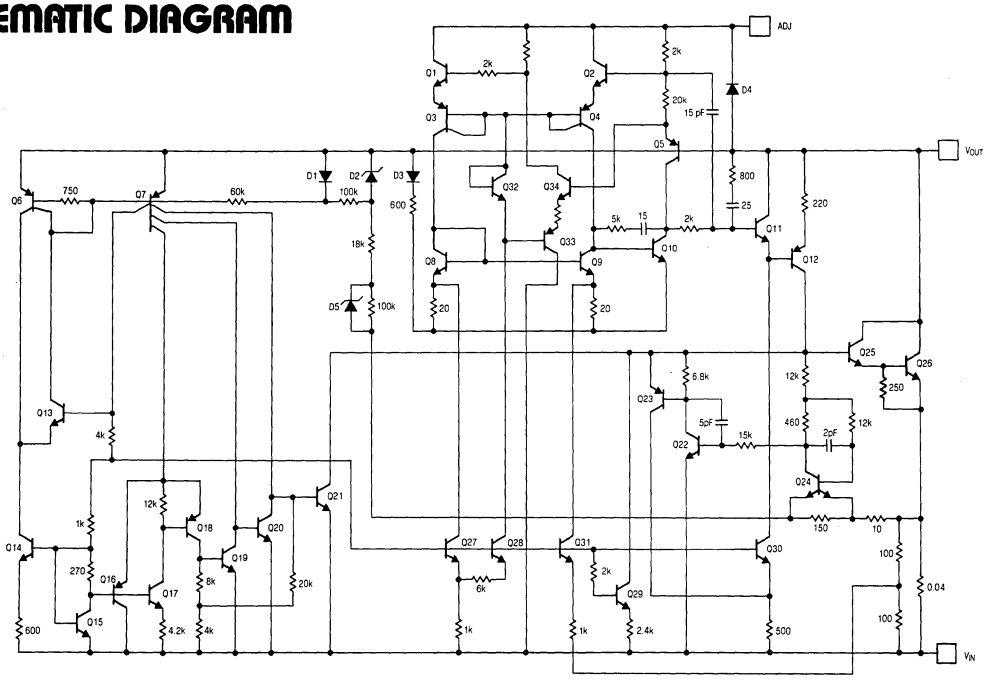
The shaded electrical specifications indicate those parameters which have been improved or guaranteed test limits provided for the first time.

Note 1: Unless otherwise indicated, these specifications apply: $\lvert V_{IN} - V_{OUT}\rvert = 5V$; and $I_{OUT} = 0.1A$ for the H package, $I_{OUT} = 0.5A$ for the K package. Power dissipation is internally limited. However, these specifications apply for power dissipation up to 2W for the H package and 20W for the K package. $I_{MAX} = 1.5A$ for the K package, and 0.2A for the H package.

Note 2: Testing is done using a pulsed low duty cycle technique. See thermal regulation specifications for output changes due to heating effects. Load regulation is measured on the output pin at a point 1/8 inch below the base of the K and H package.

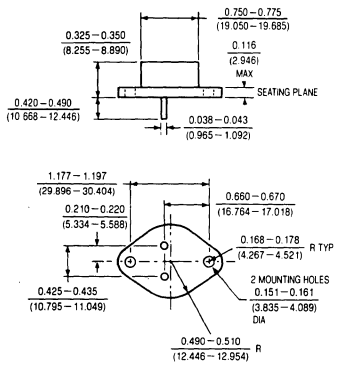
Note 3: Guaranteed on the LT137AHV and LT337AHV, but not 100% tested in production.

SCHEMATIC DIAGRAM



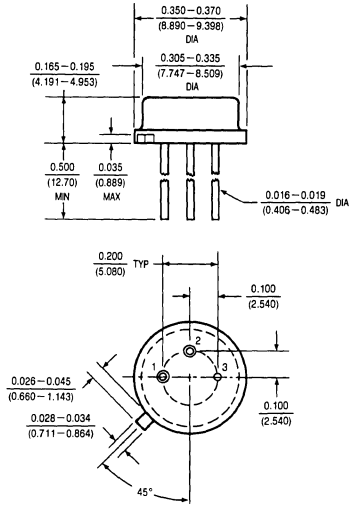
PACKAGE DESCRIPTION

K Package TO-3 STEEL Metal Can



	$T_{J\,MAX}$	Θ_{JC}
137AHV 137HV	150°C	3°C/W
337AHV 337HV	125°C	3°C/W

H Package 3-Lead Metal Can



	$T_{J\,MAX}$	Θ_{JC}
137AHV 137HV	150°C	15°C/W
337AHV 337HV	125°C	15°C/W

5 Amp Positive Adjustable Voltage Regulator

FEATURES

- *Guaranteed* 1% Initial Tolerance
- *Guaranteed* 0.3% Load Regulation
- *Guaranteed* 5 Amp Output Current
- 100% Thermal Limit Burn-in
- 12 Amp Transient Output Current

APPLICATIONS

- High Power Linear Regulator
- Battery Chargers
- Power Driver
- Constant Current Regulator

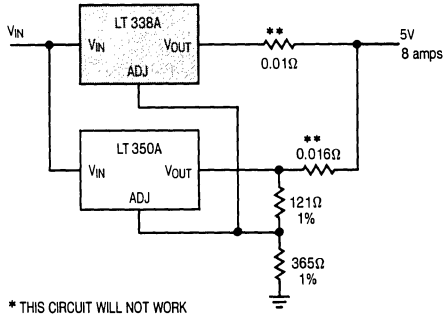
DESCRIPTION

The LT138A series of adjustable regulators provide 5 amps output current over an output voltage range of 1.2 volts to 32 volts. The internal voltage reference is trimmed to less than 1%, enabling a very tight output voltage. In addition to excellent line and load regulation, with full overload protection, the LT138A incorporates new current limiting circuitry allowing large transient load currents to be handled for short periods. Transient load currents of up to 12 amps can be supplied without limiting, eliminating the need for a large output capacitor.

The LT138A is an improved version of the popular LM138 with improved circuit design and advanced process techniques to provide superior performance and reliability.

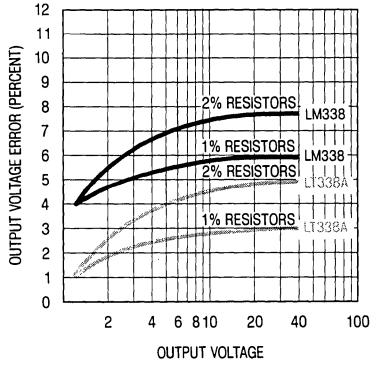
The graph below shows the significant improvement in output voltage tolerance achieved by using the LT138A or LT338A.

*** Parallel Regulators for Higher Current**



* THIS CIRCUIT WILL NOT WORK WITH LM VERSION DEVICES
** CURRENT SHARING RESISTORS DEGRADE REGULATION TO 1%

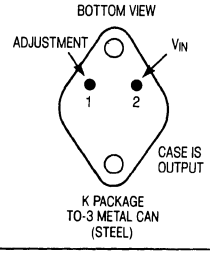
Output Voltage Error



ABSOLUTE MAXIMUM RATINGS

Power Dissipation ..... Internally Limited
Input to Output Voltage Differential 35V
Operating Junction Temperature Range
LT138A/LM138 ..... −55°C to 150°C
LT338A/LM338 ..... 0°C to 125°C
Storage Temperature Range
LT138A/LM138 ..... −65°C to 150°C
LT338A/LM338 ..... −65°C to 150°C
Lead Temperature (Soldering, 10 sec.)..... 300°C

PACKAGE/ORDER INFORMATION



K PACKAGE
TO-3 METAL CAN
(STEEL)

ORDER PART NUMBER
LT138AK
LT338AK
LM138K
LM338K

PRECONDITIONING

100% THERMAL LIMIT BURN-IN

ELECTRICAL CHARACTERISTICS (See Note 1)

SYMBOL	PARAMETER	CONDITIONS		LT138A MIN	LT138A TYP	LT138A MAX	LM138 MIN	LM138 TYP	LM138 MAX	UNITS
V_{REF}	Reference Voltage	I_{OUT} = 10mA T_j = 25°C		1.238	1.250	1.262				V
		3V ≤ (V_{IN} − V_{OUT}) ≤ 35V 10mA ≤ I_{OUT} ≤ 5A, P ≤ 50W	●	1.225	1.250	1.270	1.19	1.24	1.29	V
$\frac{\Delta V_{OUT}}{\Delta V_{IN}}$	Line Regulation	3V ≤ (V_{IN} − V_{OUT}) ≤ 35V, (See Note 2) T_A = 25°C			0.005	0.01		0.005	0.01	%/V
			●		0.02	0.04		0.02	0.04	%/V
$\frac{\Delta V_{OUT}}{\Delta I_{OUT}}$	Load Regulation	10mA ≤ I_{OUT} ≤ 5A, (See Note 2) T_A = 25°C V_{OUT} ≤ 5V			5	15		5	15	mV
		V_{OUT} ≥ 5V			0.1	0.3		0.1	0.3	%
		V_{OUT} ≤ 5V	●		20	30		20	30	mV
		V_{OUT} ≥ 5V	●		0.3	0.6		0.3	0.6	%
	Thermal Regulation	T_A = 25°C, 20msec pulse			0.002	0.01		0.002	0.01	%/W
	Ripple Rejection	V_{OUT} = 10V, f = 120Hz C_{ADJ} = 0	●		60			60		dB
		C_{ADJ} = 10μF	●	60	75		60	75		dB
I_{ADJ}	Adjust Pin Current		●		45	100		45	100	μA
ΔI_{ADJ}	Adjust Pin Current Change	10mA ≤ I_{OUT} ≤ 5A, 3V ≤ (V_{IN}−V_{OUT}) ≤ 35V	●		0.2	5		0.2	5	μA
	Minimum Load Current	(V_{IN} − V_{OUT}) = 35V	●		3.5	5		3.5	5	mA
I_{SC}	Current Limit	(V_{IN} − V_{OUT}) ≤ 10V DC	●	5	8		5	8		A
		0.5ms peak	●	7	12		7	12		A
		(V_{IN} − V_{OUT}) = 30V, T_j = 25°C			1			1		A
$\frac{\Delta V_{OUT}}{\Delta Temp}$	Temperature Stability		●		1	2		1		%
$\frac{\Delta V_{OUT}}{\Delta Time}$	Long Term Stability	T_A = 125°C, 1000 Hours			0.3	1		0.3	1	%
e_n	RMS Output Noise (% of V_{OUT})	T_A = 25°C, 10Hz ≤ f ≤ 10kHz			0.001			0.003		%
Θ_{JC}	Thermal Resistance Junction to Case	K Package				1			1	°C/W

ELECTRICAL CHARACTERISTICS (See Note 1)

SYMBOL	PARAMETER	CONDITIONS		LT338A MIN	LT338A TYP	LT338A MAX	LM338 MIN	LM338 TYP	LM338 MAX	UNITS
V_{REF}	Reference Voltage	I_{OUT} = 10mA T_A = 25°C		1.238	1.250	1.262				V
		3V ≤ (V_{IN} − V_{OUT}) ≤ 35V 10mA ≤ I_{OUT} ≤ 5A, P ≤ 50W	●	1.225	1.250	1.270	1.19	1.24	1.29	V
$\frac{\Delta V_{OUT}}{\Delta V_{IN}}$	Line Regulation	3V ≤ (V_{IN} − V_{OUT}) ≤ 35V, (See Note 2) T_A = 25°C			0.005	0.01		0.005	0.03	%/V
			●		0.02	0.04		0.02	0.06	%/V
$\frac{\Delta V_{OUT}}{\Delta I_{OUT}}$	Load Regulation	10mA ≤ I_{OUT} ≤ 5A, (See Note 2) T_A = 25°C								
		V_{OUT} ≤ 5V			5	15		5	25	mV
		V_{OUT} ≥ 5V			0.1	0.3		0.1	0.5	%
		V_{OUT} ≤ 5V	●		20	30		20	50	mV
		V_{OUT} ≥ 5V	●		0.3	0.6		0.3	1	%
	Thermal Regulation	T_A = 25°C, 20msec Pulse			0.002	0.02		0.002	0.02	%/W
	Ripple Rejection	V_{OUT} = 10V, f = 120Hz C_{ADJ} = 0	●		60			60		dB
		C_{ADJ} = 10μF	●	60	75		60	75		dB
I_{ADJ}	Adjust Pin Current		●		45	100		45	100	μA
ΔI_{ADJ}	Adjust Pin Current Change	10mA ≤ I_{OUT} ≤ 5A, 3V ≤ (V_{IN}−V_{OUT}) ≤ 35V	●		0.2	5		0.2	5	μA
	Minimum Load Current	(V_{IN} − V_{OUT}) = 35V	●		3.5	10		3.5	10	mA
I_{SC}	Current Limit	(V_{IN} − V_{OUT}) ≤ 10V DC	●	5	8		5	8		A
		0.5ms peak	●	7	12		7	12		A
		(V_{IN} − V_{OUT}) = 30V, T_J = 25°C			1	2		1		A
$\frac{\Delta V_{OUT}}{\Delta Temp}$	Temperature Stability		●		1	2		1		%
$\frac{\Delta V_{OUT}}{\Delta Time}$	Long Term Stability	T_A = 125°C, 1000 Hours			0.3	1		0.3	1	%
e_n	RMS Output Noise (% of V_{OUT})	T_A = 25°C, 10Hz ≤ f ≤ 10kHz			0.001			0.003		%
Θ_{JC}	Thermal Resistance Junction to Case	K Package				1			1	°C/W

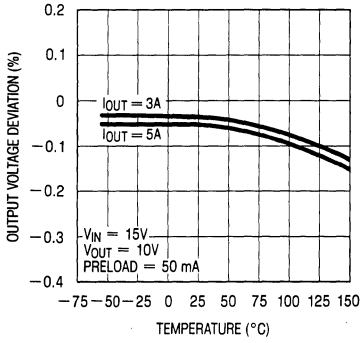
The ● denotes the specifications which apply over the full operating temperature range.

Note 1: Unless otherwise specified, these specifications apply: V_{IN} − V_{OUT} = 5V and I_{OUT} = 2.5A. These specifications are applicable for power dissipations up to 50W.

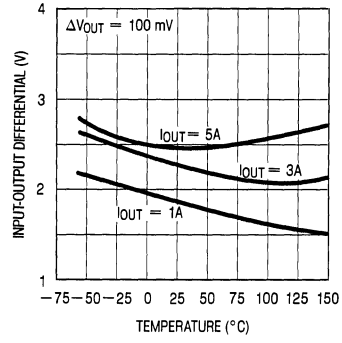
Note 2: See thermal regulation specifications for changes in output voltage due to heating effects. Load and line regulation are measured at a constant junction temperature by low duty cycle pulse testing.

TYPICAL PERFORMANCE CHARACTERISTICS

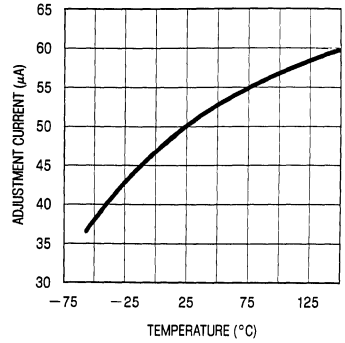
Load Regulation



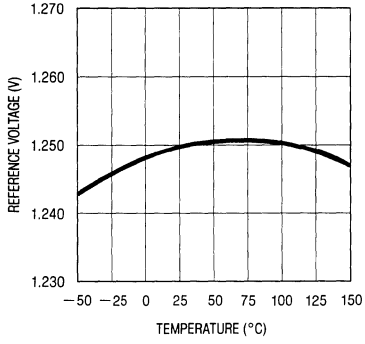
Dropout Voltage



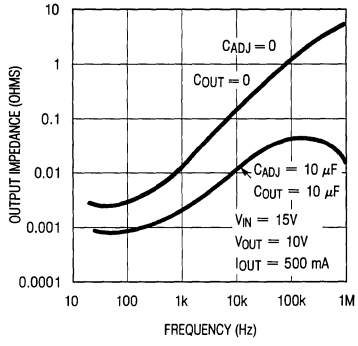
Adjustment Current



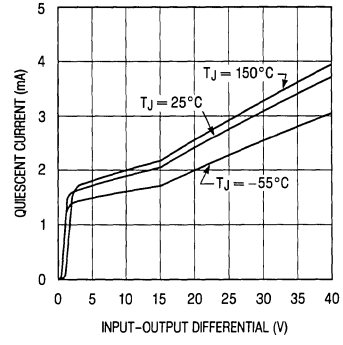
Temperature Stability



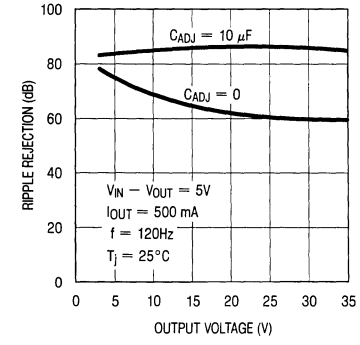
Output Impedance



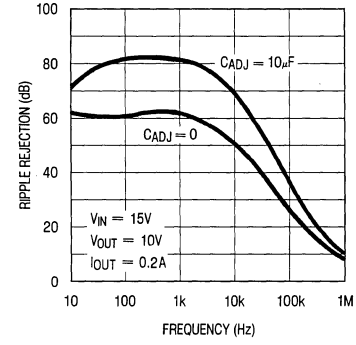
Minimum Operating Current



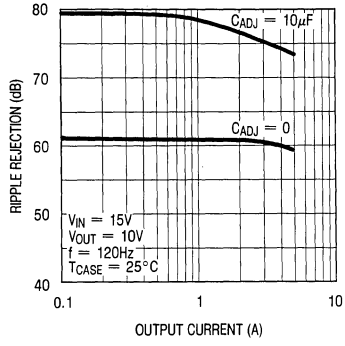
Ripple Rejection



Ripple Rejection

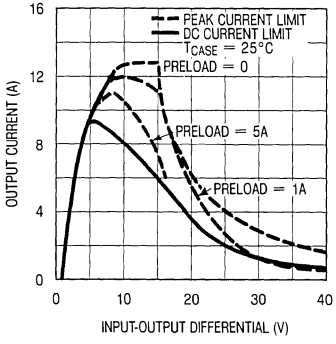


Ripple Rejection

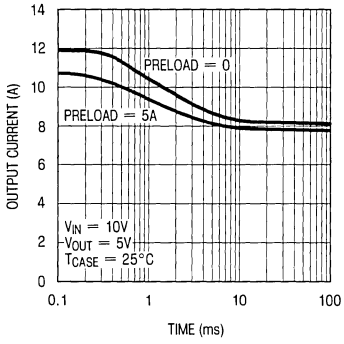


TYPICAL PERFORMANCE CHARACTERISTICS

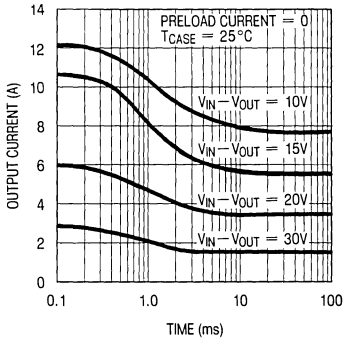
Current Limit



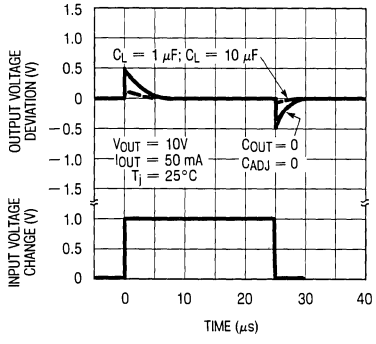
Current Limit



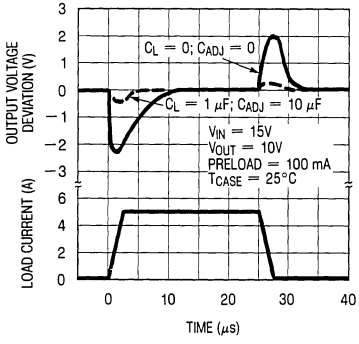
Current Limit



Line Transient Response



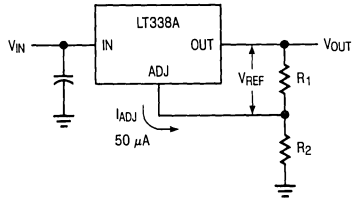
Load Transient Response



APPLICATIONS INFORMATION

General

The LT138A develops a 1.25V reference voltage between the output and the adjustable terminal (see Figure 1). By placing a resistor, R1, between these two terminals, a constant current is caused to flow through R1 and down through R2 to set the overall output voltage. Normally this current is the specified minimum load current of 5mA or 10mA. Because I_{ADJ} is very small and constant when compared with the current through R1, it represents a small error and can usually be ignored. It is easily seen from the output voltage equation, that even if the resistors were of exact value, the accuracy of the output is limited by the accuracy of V_{REF}. Earlier adjustable regulators had a reference tolerance of ±4% which is dangerously close to the ±5% supply tolerance required in many logic and analog systems. Further, even 1% resistors can drift 0.01%/°C, adding additional error to the output voltage tolerance.



$$V_{OUT} = V_{REF}\left(1 + \frac{R_2}{R_1}\right) + I_{ADJ}R_2$$

Basic Adjustable Regulator
Figure 1

For example, using 2% resistors and ±4% tolerance for V_{REF}, calculations will show that the expected range of a 5V regulator design would be $4.66V \leq V_{OUT} \leq 5.36V$ or approximately ±7%. If the same example were used for a 15V regulator, the expected tolerance would be ±8%. With these results most applications required some method of trimming, usually a trim pot. This solution is both expensive and not conducive to volume production.

One of the enhancements of Linear Technology's adjustable regulators over existing devices is the tightened initial tolerance of V_{REF}. This allows relatively inexpensive 1% or 2% film resistors to be used for R1 and R2 to set the output voltage within an acceptable tolerance.

With a guaranteed 1% reference, a 5V power supply design, using ±2% resistors, would have a worst case manufacturing tolerance of ±4%. If 1% resistors are used, the tolerance will drop to ±2.5%. A plot of the worst case output voltage tolerance as a function of resistor tolerance is shown on the front page.

For convenience, a table of standard 1% resistor values is shown below.

Table of ½% and 1% Standard Resistance Values

1.00	1.47	2.15	3.16	4.64	6.81
1.02	1.50	2.21	3.24	4.75	6.98
1.05	1.54	2.26	3.32	4.87	7.15
1.07	1.58	2.32	3.40	4.99	7.32
1.10	1.62	2.37	3.48	5.11	7.50
1.13	1.65	2.43	3.57	5.23	7.68
1.15	1.69	2.49	3.65	5.36	7.87
1.18	1.74	2.55	3.74	5.49	8.06
1.21	1.78	2.61	3.83	5.62	8.25
1.24	1.82	2.67	3.92	5.76	8.45
1.27	1.87	2.74	4.02	5.90	8.66
1.30	1.91	2.80	4.12	6.04	8.87
1.33	1.96	2.87	4.22	6.19	9.09
1.37	2.00	2.94	4.32	6.34	9.31
1.40	2.05	3.01	4.42	6.49	9.53
1.43	2.10	3.09	4.53	6.65	9.76

Standard Resistance Values are obtained from the Decade Table by multiplying by multiples of 10. As an example, 1.21 can represent 1.21Ω, 12.1Ω, 121Ω, 1.21KΩ etc.

Bypass Capacitors

Input bypassing using a 1μF tantalum or 25μF electrolytic is recommended when the input filter capacitors are more than 5 inches from the device. Improved ripple rejection (80 dB) can be accomplished by adding a 10μF capacitor from the adjust pin to ground. Increasing the size of the capacitor to 20μF will help ripple rejection at low output voltage since the reactance of this capacitor should be small compared to the voltage setting resistor, R2. For improved AC transient response and to prevent the possibility of oscillation due to unknown reactive load, a 1μF capacitor is also recommended at the output. Because of their low impedance at high frequencies, the best type of capacitor to use is solid tantalum.

Protection Diodes

The LT138A/338A do not require a protection diode from the adjustment terminal to the output (see figure 2). Improved internal circuitry eliminates the need for this diode when the adjustment pin is bypassed with a capacitor to improve ripple rejection.

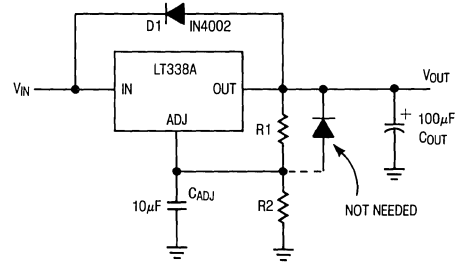


Figure 2

If a very large output capacitor is used, such as a 100μF shown in figure 2, the regulator could be damaged or destroyed if the input is accidentally shorted to ground or crowbarred, due to the output capacitor discharging into the output terminal of the regulator. To prevent this, a diode D1 as shown, is recommended to safely discharge the capacitor.

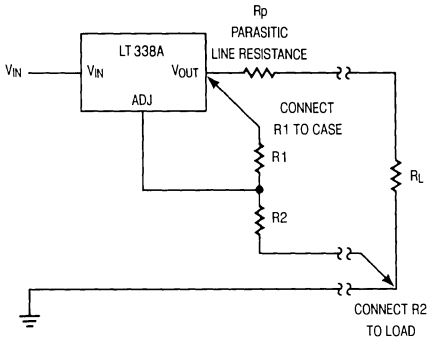
Load Regulation

Because the LT138A is a three-terminal device, it is not possible to provide true remote load sensing. Load regulation will be limited by the resistance of the wire connecting the regulator to the load. The data sheet specification for load regulation is measured at the bottom of the package. Negative side sensing is a true Kelvin connection, with the bottom of the output divider returned to the negative side of the load. Although it may not be immediately obvious, best load regulation is obtained when the top of the resistor divider, (R1), is connected *directly* to the case *not to the load.* This is illustrated in *Figure 3.* If R1 were connected to the

load, the effective resistance between the regulator and the load would be

$$R_p \times \left(\frac{R2 + R1}{R1}\right), R_p = \text{Parasitic Line Resistance.}$$

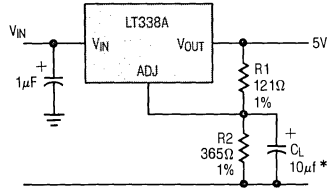
Connected as shown, R_p is not multiplied by the divider ratio. R_p is about 0.004Ω per foot using 16 gauge wire. This translates to 4mV/ft at 1A load current, so it is important to keep the positive lead between regulator and load as short as possible, and use large wire or PC board traces.



Connections For Best Load Regulation
Figure 3.

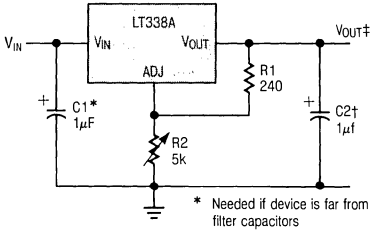
TYPICAL APPLICATIONS

Improving Ripple Rejection



* C_1 IMPROVES RIPPLE REJECTION X_C SHOULD BE SMALL COMPARED TO R_2

1.2V–25V Adjustable Regulator

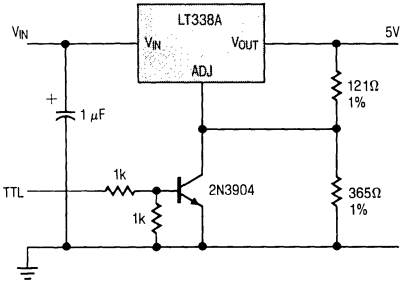


* Needed if device is far from filter capacitors

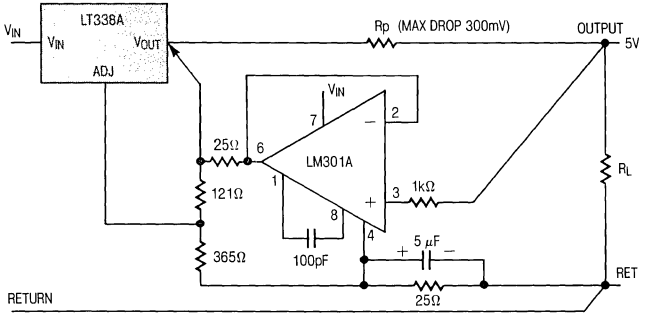
† Optional—improves transient response

‡ $V_{OUT} = 1.25V\left(1 + \frac{R2}{R1}\right)$

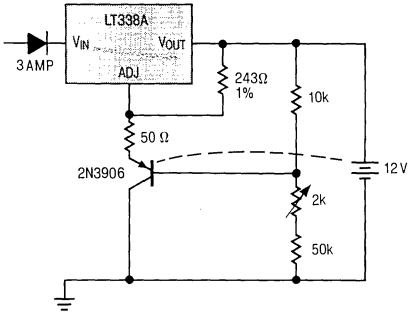
5V Regulator With Shut Down



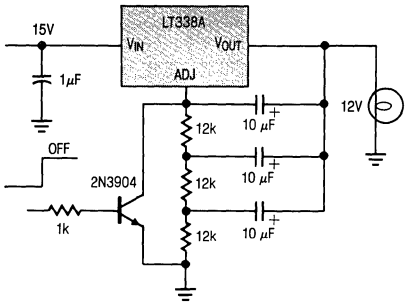
Remote Sensing



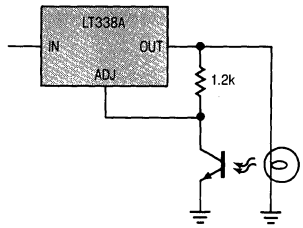
Temperature Compensated Lead Acid Battery Charger



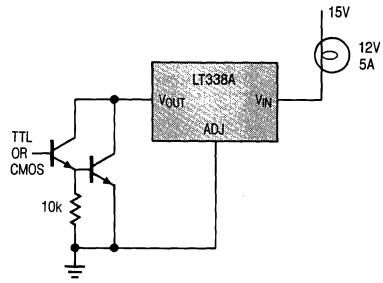
Lamp Flasher



Automatic Light Control

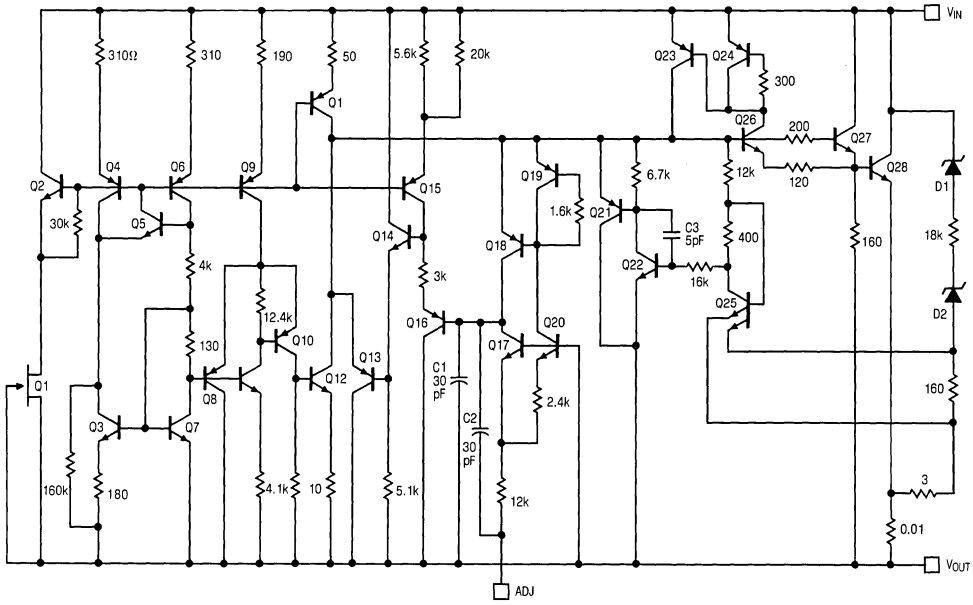


Protected High Current Lamp Driver



SCHEMATIC DIAGRAM

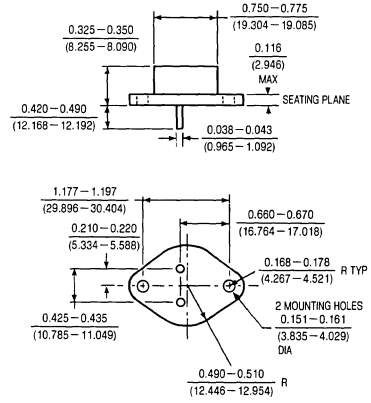
LT138A/LT338A



PACKAGE DESCRIPTION

K Package To-3
Steel Metal Can

	T_j max.	θ_{ja}	θ_{jc}
138A 138	150°C	35°C/W	1°C/W
338A 338	125°C	35°C/W	1°C/W



3 Amp Positive Adjustable Regulator

FEATURES

- *Guaranteed* 1% Initial Voltage Tolerance
- *Guaranteed* 3A Output Current
- *Guaranteed* 0.3% Load Regulation
- *Guaranteed* 0.01%/V Line Regulation
- 100% Thermal Limit Burn-in

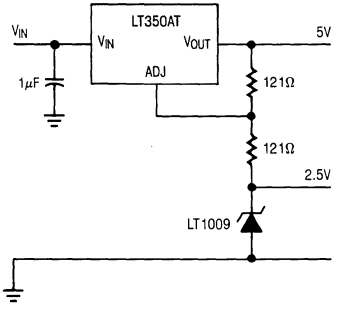
APPLICATIONS

- Improved Linear Regulators
- Adjustable Power Supplies
- Constant Current Regulation
- Battery Chargers

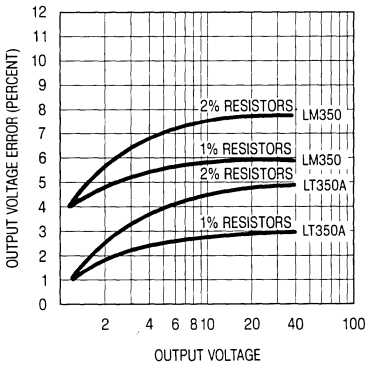
DESCRIPTION

The LT150A Series are 3-terminal positive adjustable voltage regulators which offer improved performance over earlier devices. A major feature of the LT150A/350A is the output voltage tolerance is guaranteed at a maximum of ±1%, allowing an overall power supply tolerance to be better than 3% using inexpensive 1% resistors. Line and load regulation performance has been improved as well. Additionally, the LT150A/350A reference voltage is guaranteed not to exceed 2% when operating over the full load, line and power dissipation conditions. The LT150A/350A adjustable regulators offer an improved solution for all positive voltage regulator requirements with load currents up to 3 amps.

Regulator With Reference



Output Voltage Error



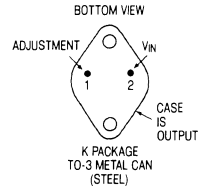
ABSOLUTE MAXIMUM RATINGS

Power Dissipation ..... Internally Limited
Input to Output Voltage Differential 35V
Operating Junction Temperature Range
LT150A/LM150 ..... −55°C to 150°C
LT350A/LM350 ..... 0°C to 125°C
Storage Temperature Range
LT150A/LM150 ..... −65°C to 150°C
LT350A/LM350 ..... −65°C to 150°C
Lead Temperature (Soldering, 10 sec.)..... 300°C

PRECONDITIONING:

100% THERMAL LIMIT BURN-IN

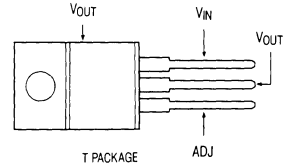
PACKAGE/ORDER INFORMATION



K PACKAGE
TO-3 METAL CAN
(STEEL)

ORDER PART NUMBER

LT150AK
LT350AK
LM150K
LM350K



T PACKAGE
TO-220 PLASTIC

LT350AT

LM350T

ELECTRICAL CHARACTERISTICS (See Note 1)

SYMBOL	PARAMETER	CONDITIONS		LT150A MIN	LT150A TYP	LT150A MAX	LM150 MIN	LM150 TYP	LM150 MAX	UNITS
V_{REF}	Reference Voltage	I_{OUT} = 10mA, T_j = 25°C		1.238	1.250	1.262				V
		3V ≤ (V_{IN} − V_{OUT}) ≤ 35V 10mA ≤ I_{OUT} ≤ 3A, P ≤ 30W	●	1.225	1.250	1.270	1.20	1.25	1.30	V
$\frac{\Delta V_{OUT}}{\Delta V_{IN}}$	Line Regulation	3V ≤ (V_{IN} − V_{OUT}) ≤ 35V, (See Note 2)			0.005	0.01		0.005	0.01	%/V
			●		0.02	0.05		0.02	0.05	%/V
$\frac{\Delta V_{OUT}}{\Delta I_{OUT}}$	Load Regulation	10mA ≤ I_{OUT} ≤ 3A, (See Note 2) T_A = 25°C								
		V_{OUT} ≤ 5V			5	15		5	15	mV
		V_{OUT} ≥ 5V			0.1	0.3		0.1	0.3	%
		V_{OUT} ≤ 5V	●		15	50		20	50	mV
		V_{OUT} ≥ 5V	●		0.3	1		0.3	1	%
	Thermal Regulation	T_A = 25°C, 20msec Pulse			0.002	0.01		0.002	0.01	%/W
	Ripple Rejection	V_{OUT} = 10V, f = 120Hz C_{ADJ} = 0	●		65			65		dB
		C_{ADJ} = 10μF	●	66	86		66	86		dB
I_{ADJ}	Adjust Pin Current		●		50	100		50	100	μA
ΔI_{ADJ}	Adjust Pin Current Change	10mA ≤ I_L ≤ 3A 3V ≤ (V_{IN} − V_{OUT}) ≤ 35V	●		0.2	5		0.2	5	μA
	Minimum Load Current	(V_{IN} − V_{OUT}) = 35V	●		3.5	5		3.5	5	mA
	Current Limit	(V_{IN} − V_{OUT}) ≤ 10V	●	3	4.5		3.0	4.5		A
		(V_{IN} − V_{OUT}) = 30V	●	0.3	1		0.3	1		A
$\frac{\Delta V_{OUT}}{\Delta Temp}$	Temperature Stability	−55°C ≤ T_j ≤ +150°C	●		1	2		1		%
$\frac{\Delta V_{OUT}}{\Delta Time}$	Long Term Stability	T_A = 125°C			0.3	1		0.3	1	%
e_n	RMS Output Noise (% of V_{OUT})	T_A = 25°C, 10Hz ≤ f ≤ 10kHz			0.001			0.001		%
Θ_{jc}	Thermal Resistance Junction to Case	K Package				1.5			1.5	°C/W

ELECTRICAL CHARACTERISTICS (See Note 1)

SYMBOL	PARAMETER	CONDITIONS		LT350A MIN	LT350A TYP	LT350A MAX	LM350 MIN	LM350 TYP	LM350 MAX	UNITS
V_{REF}	Reference Voltage	I_{OUT} = 10mA, T_j = 25°C		1.238	1.250	1.262				V
		3V ≤ (V_{IN} − V_{OUT}) ≤ 35V 10mA ≤ I_{OUT} ≤ 3A, P ≤ 30W	●	1.225	1.250	1.270	1.20	1.25	1.30	V
$\frac{\Delta V_{OUT}}{\Delta V_{IN}}$	Line Regulation	3V ≤ (V_{IN} − V_{OUT}) ≤ 35V, (See Note 2) T_A = 25°C			0.005	0.01		0.005	0.03	%/V
			●		0.02	0.05		0.02	0.07	%/V
$\frac{\Delta V_{OUT}}{\Delta I_{OUT}}$	Load Regulation	10mA ≤ I_{OUT} ≤ 3A, (See Note 2) T_A = 25°C V_{OUT} ≤ 5V			5	15		5	25	mV
		V_{OUT} ≥ 5V			0.1	0.3		0.1	0.5	%
		V_{OUT} ≤ 5V	●		15	50		20	70	mV
		V_{OUT} ≥ 5V	●		0.3	1		0.3	1.5	%
	Thermal Regulation	T_A = 25°C, 20msec Pulse			0.002	0.01		0.002	0.03	%/W
	Ripple Rejection	V_{OUT} = 10V, f = 120Hz C_{ADJ} = 0	●		65			65		dB
		C_{ADJ} = 10μF	●	66	86		66	86		dB
I_{ADJ}	Adjust Pin Current		●		50	100		50	100	μA
ΔI_{ADJ}	Adjust Pin Current Change	10mA ≤ I_{OUT} ≤ 3A 3V ≤ (V_{IN} − V_{OUT}) ≤ 35V	●		0.2	5		0.2	5	μA
	Minimum Load Current	(V_{IN} − V_{OUT}) ≤ 35V	●		3.5	10		3.5	10	mA
	Current Limit	(V_{IN} − V_{OUT}) ≤ 10V	●	3	4.5		3	4.5		A
		(V_{IN} − V_{OUT}) = 30V, T_j = 25°C		0.25	1		0.25	1		A
$\frac{\Delta V_{OUT}}{\Delta Temp}$	Temperature Stability		●		1	2		1		%
$\frac{\Delta V_{OUT}}{\Delta Time}$	Long Term Stability	T_A = 125°C			0.3	1		0.3	1	%
e_n	RMS Output Noise (% of V_{OUT})	T_A = 25°C, 10Hz ≤ f ≤ 10kHz			0.001			0.001		%
Θ_{jc}	Thermal Resistance Junction to Case	K Package			1.2	1.5		1.2	1.5	°C/W
		T Package			3	4		3	4	°C/W

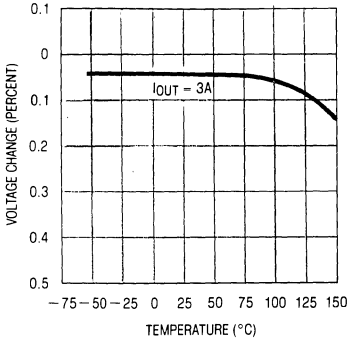
The ● denotes the specifications which apply over the full operating temperature range.

Note 1: Unless otherwise specified, these specifications apply for $V_{IN}-V_{OUT}$ = 5V and I_{OUT} = 1.5A. These specifications are applicable for power dissipations up to 30W for the K package and up to 25W for the T package. Power dissipation is guaranteed at these values up to 15 Volts input-output differential. Above 15 Volts input-output differential power dissipation is limited by device internal protection circuitry.

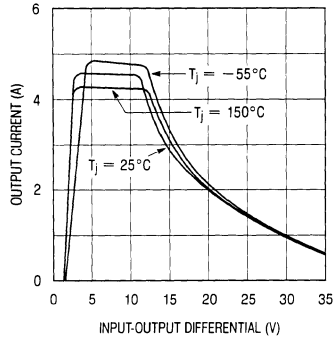
Note 2: Regulation is measured at a constant T_j. Changes in output due to heating must be taken into account separately. Pulse testing with low duty cycle is used.

TYPICAL PERFORMANCE CHARACTERISTICS

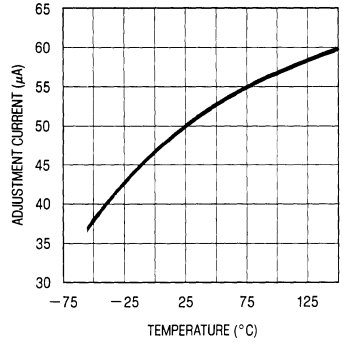
Load Regulation



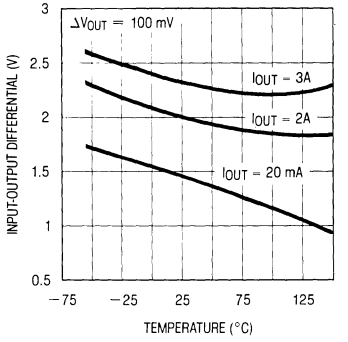
Current Limit



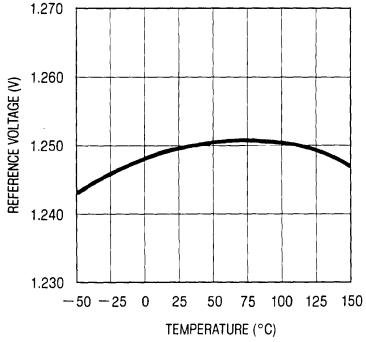
Adjustment Current



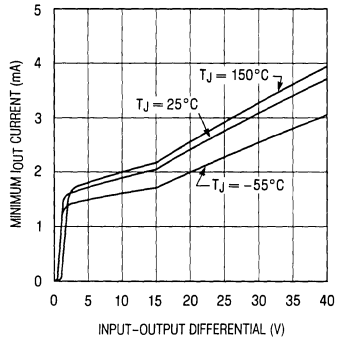
Dropout Voltage



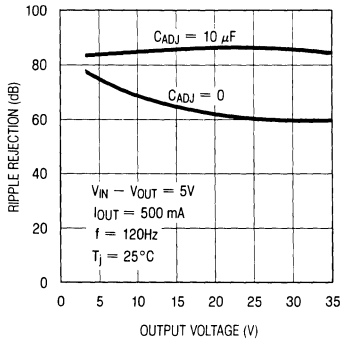
Temperature Stability



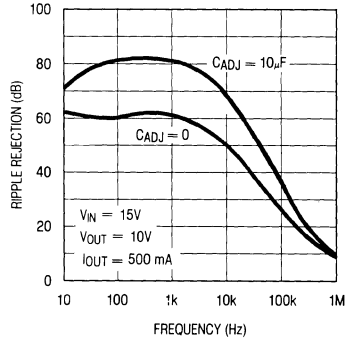
Minimum Operating Current



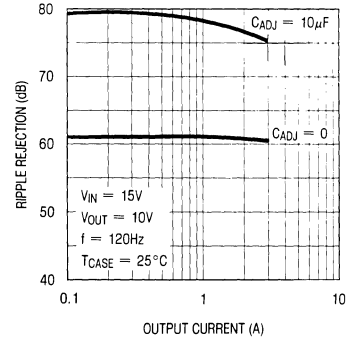
Ripple Rejection



Ripple Rejection

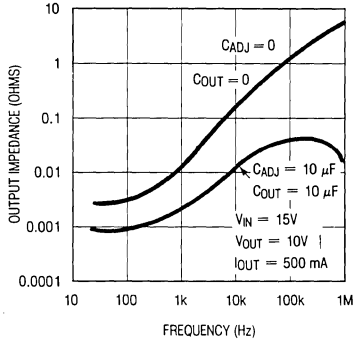


Ripple Rejection

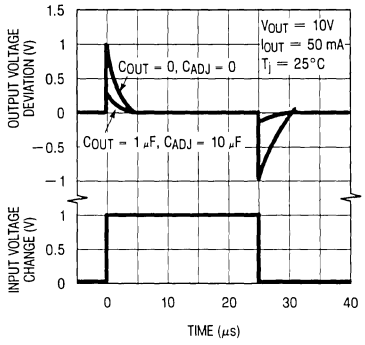


TYPICAL PERFORMANCE CHARACTERISTICS

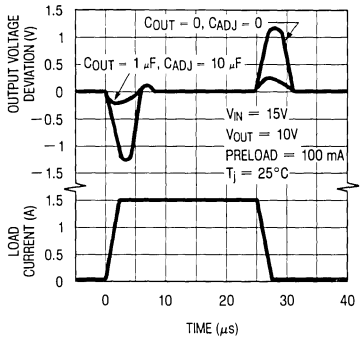
Output Impedance



Line Transient Response



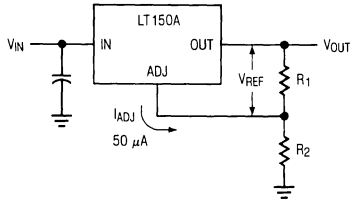
Load Transient Response



APPLICATION INFORMATION

General

The LT150A develops a 1.25V reference voltage between the output and the adjustable terminal (see Figure 1). By placing a resistor, R1, between these two terminals, a constant current is caused to flow through R1 and down through R2 to set the overall output voltage. Normally this current is the specified minimum load current of 5mA or 10mA.



$$V_{OUT} = V_{REF}\left(1 + \frac{R_2}{R_1}\right) + I_{ADJ}R_2$$

Basic Adjustable Regulator
Figure 1

Because I_{ADJ} is very small and constant when compared with the current through R1, it represents a small error and can usually be ignored. It is easily seen from the above equation, that even if the resistors were of exact value, the accuracy of the output is limited by the accuracy of V_{REF}. Earlier adjustable regulators had a reference tolerance of ±4% which is dangerously close to the ±5% supply tolerance required in many logic and analog systems. Further, even 1% resistors can drift 0.01%/°C, adding additional error to the output voltage tolerance.

For example, using 2% resistors and ±4% tolerance for V_{REF}, calculations will show that the expected range of a 5V regulator design would be 4.66V ≤ V_{OUT} ≤ 5.36V or approximately ±7%. If the same example were used for a 15V regulator, the expected tolerance would be ±8%. With these results most applications required some method of trimming, usually a trim pot. This solution is both expensive and not conducive to volume production.

One of the enhancements of Linear Technology's adjustable regulators over existing devices is the tightened initial tolerance of V_{REF}. This allows relatively inexpensive 1% or 2% film resistors to be used for R1 and R2 to set the output voltage within an acceptable tolerance.

With a guaranteed 1% reference, a 5V power supply design, using ±2% resistors, would have a worst case manufacturing tolerance of ±4%. If 1% resistors were used, the tolerance would drop to ±2.5%. A plot of the worst case output voltage tolerance as a function of resistor tolerance is shown on the front page.

For convenience, a table of standard 1% resistor values is shown below.

Table of ½% and 1% Standard Resistance Values

1.00	1.47	2.15	3.16	4.64	6.81
1.02	1.50	2.21	3.24	4.75	6.98
1.05	1.54	2.26	3.32	4.87	7.15
1.07	1.58	2.32	3.40	4.99	7.32
1.10	1.62	2.37	3.48	5.11	7.50
1.13	1.65	2.43	3.57	5.23	7.68
1.15	1.69	2.49	3.65	5.36	7.87
1.18	1.74	2.55	3.74	5.49	8.06
1.21	1.78	2.61	3.83	5.62	8.25
1.24	1.82	2.67	3.92	5.76	8.45
1.27	1.87	2.74	4.02	5.90	8.66
1.30	1.91	2.80	4.12	6.04	8.87
1.33	1.96	2.87	4.22	6.19	9.09
1.37	2.00	2.94	4.32	6.34	9.31
1.40	2.05	3.01	4.42	6.49	9.53
1.43	2.10	3.09	4.53	6.65	9.76

Standard Resistance Values are obtained from the Decade Table by multiplying by multiples of 10. As an example, 1.21 can represent 1.21Ω, 12.1Ω, 121Ω, 1.21KΩ etc.

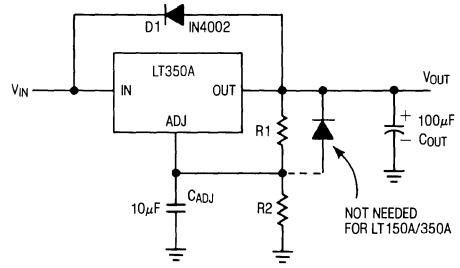


Figure 2

If a very large output capacitor is used, such as a 100μF shown in Figure 2, the regulator could be damaged or destroyed if the input is accidentally shorted to ground or crowbarred, due to the output capacitor discharging into the output terminal of the regulator. To prevent this, a diode D1 as shown, is recommended to safely discharge the capacitor.

Bypass Capacitors

Input bypassing using a 1μF tantalum or 25μF electrolytic is recommended when the input filter capacitors are more than 5 inches from the device. Improved ripple rejection (80 dB) can be accomplished by adding a 10μF capacitor from the adjust pin to ground. Increasing the size of the capacitor to 20μF will help ripple rejection at low output voltage since the reactance of this capacitor should be small compared to the voltage setting resistor, R2. For improved AC transient response and to prevent the possibility of oscillation due to unknown reactive load, a 1μF capacitor is also recommended at the output. Because of their low impedance at high frequencies, the best type of capacitor to use is solid tantalum.

Protection Diodes

The LT150A/350A do not require a protection diode from the adjustment terminal to the output (see Figure 2). Improved internal circuitry eliminates the need for this diode when the adjustment pin is bypassed with a capacitor to improve ripple rejection.

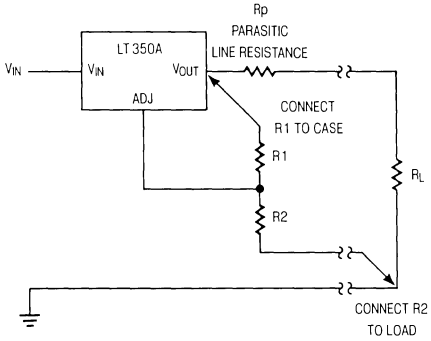
Load Regulation

Because the LT150A is a three-terminal device, it is not possible to provide true remote load sensing. Load regulation will be limited by the resistance of the wire connecting the regulator to the load. The data sheet specification for load regulation is measured at the bottom of the package. Negative side sensing is a true Kelvin connection, with the bottom of the output divider returned to the negative side of the load. Although it may not be immediately obvious, best load regulation is obtained when the top of the resistor divider (R1) is connected *directly* to the case *not to the load.* This is illustrated in *Figure 3.* If R1 were connected to the load, the effective resistance between the regulator and the load would be

$$R_p \times \left(\frac{R2 + R1}{R1}\right), R_p = \text{Parasitic Line Resistance.}$$

Connected as shown, R_p is not multiplied by the divider ratio. R_p is about 0.004Ω per foot using 16 gauge wire. This translates to 4mV/ft at 1A load current, so it

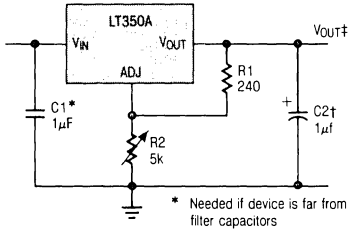
is important to keep the positive lead between regulator and load as short as possible, and use large wire or PC board traces.



Connections for Best Load Regulation
Figure 3

TYPICAL APPLICATIONS

1.2V–25V Adjustable Regulator

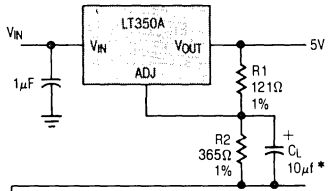


* Needed if device is far from filter capacitors

† Optional—improves transient response

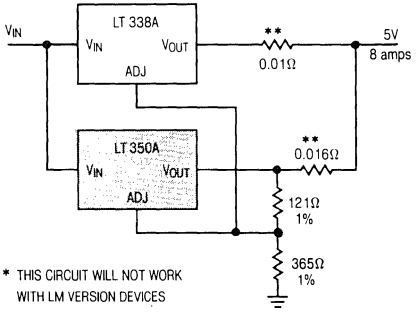
‡ $V_{OUT} = 1.25V \left(1 + \frac{R2}{R1}\right)$

Improving Ripple Rejection



* C_1 IMPROVES RIPPLE REJECTION X_C SHOULD BE SMALL COMPARED TO R_2

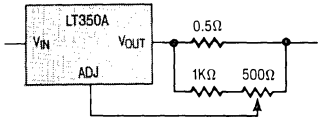
*Parallel Regulators for Higher Current



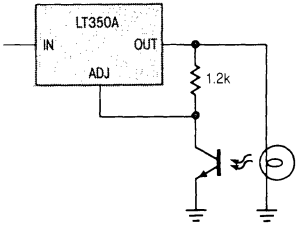
* THIS CIRCUIT WILL NOT WORK WITH LM VERSION DEVICES BECAUSE OF WIDER REFERENCE VOLTAGE LIMITS

** CURRENT SHARING RESISTORS DEGRADE REGULATION TO 1%

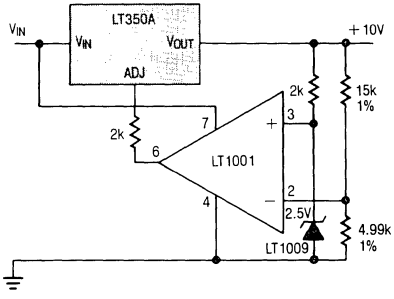
Adjustable Current Limiter



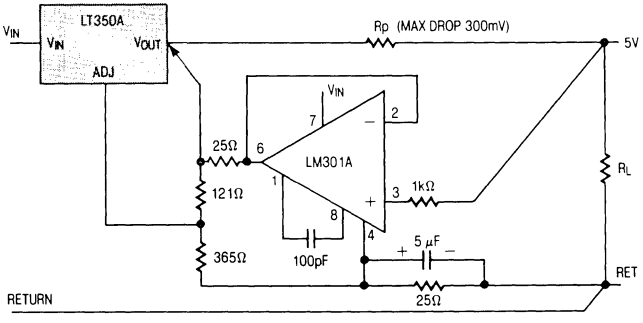
Automatic Light Control



Precision High Current Reference

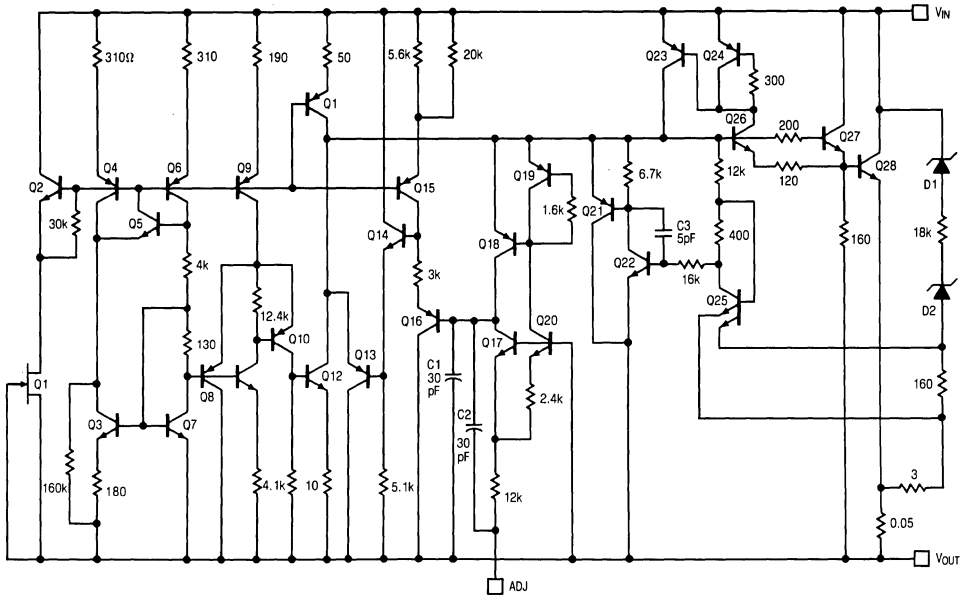


Remote Sensing



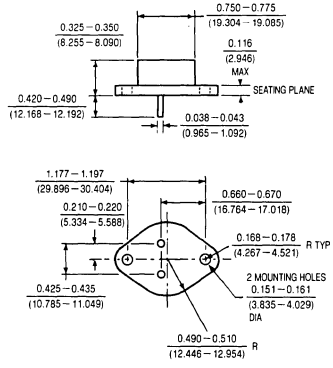
SCHEMATIC DIAGRAM

LT150A/LT350A



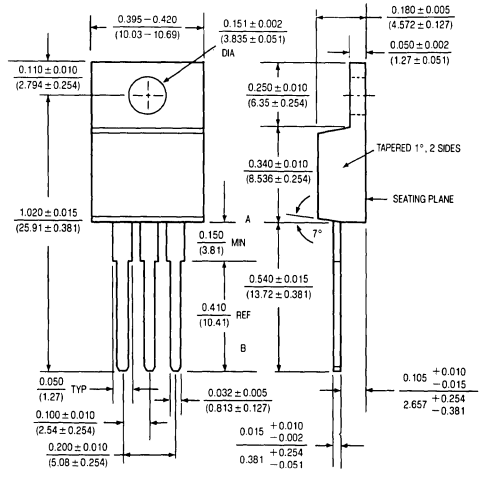
PACKAGE DESCRIPTION

K Package TO-3 STEEL Metal Can



	T_j max.	θ_{ja}	θ_{jc}
LT150A LM150	150°C	35°C/W	1.5°C/W
LT350A LM350	125°C	35°C/W	1.5°C/W

T Package TO-220 Plastic



	T_j max.	θ_{ja}	θ_{jc}
LT350A LM350	125°C	50°C/W	2.5°C/W

SECTION 4—VOLTAGE REFERENCES

SECTION 4—VOLTAGE REFERENCES

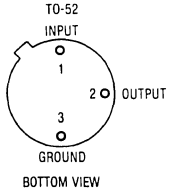
MILITARY TEMPERATURE RANGE
−55°C TO +125°C

VOLTAGE V_Z (VOLTS)	VOLTAGE TOLERANCE MAXIMUM $T_A = 25°C$	DEVICE	TEMPERATURE DRIFT, ppm/°C OR mV CHANGE	OPERATING CURRENT RANGE (OR SUPPLY CURRENT)	MAXIMUM DYNAMIC IMPEDANCE (Ω)	MAJOR FEATURE
1.235	±0.32%	LT1004M-1.2	20ppm (typ)	10μA to 20mA	1.5	Micropower
	±1%	LM185-1.2	20ppm (typ)	10μA to 20mA	1.5	Micropower
	±1%	LT1034BM	20ppm(max)	20μA to 20mA	1.5	Low TC Micropower with 7V Aux. Reference
	±1%	LT1034M	40ppm(max)	20μA to 20mA	1.5	Low TC Micropower with 7V Aux. Reference
2.5	±0.5%	LT1004M-2.5	20ppm (typ)	20μA to 20mA	1.5	Micropower
	±0.2%	LT1009M	18mV (max)	400μA to 10μA	1.0	Precision
	±0.2%	LT1019M-2.5	25ppm (max)	1.2μA	N/A	Precision Bandgap
	±0.05%	LT1019AM-2.5	10ppm (max)	1.0μA	N/A	Precision Bandgap
	±2%	LM136-2.5	18mV (max)	400μA to 10mA	1.0	General Purpose
	±1%	LM136A-2.5	18mV (max)	400μA to 10mA	1.0	General Purpose
	±1.5%	LM185-2.5	20ppm (typ)	20μA to 20mA	1.5	Micropower
	±1%	AD580S	55ppm(max)	1.5mA	N/A	3 Terminal Low Drift
	±0.4%	AD580T	25ppm(max)	1.5mA	N/A	3 Terminal Low Drift
	±0.4%	AD580U	10ppm(max)	1.5mA	N/A	3 Terminal Low Drift
5.0	±0.2%	LT1019M-5	25ppm (max)	1.2mA	N/A	Precision Bandgap
	±0.05%	LT1019AM-5	10ppm (max)	1.0mA	N/A	Precision Bandgap
	±1%	LT1021BM-5	5ppm (max)	1.2mA	0.1	Very Low Drift
	±0.05%	LT1021CM-5	20ppm (max)	1.2mA	0.1	Very Tight Initial Tolerance
	±1%	LT1021DM-5	20ppm (max)	1.2mA	0.1	Low Cost, High Performance
	±0.2%	LT1029AM	20ppm (max)	600μA to 10mA	0.6	Precision Bandgap
	±1%	LT1029M	40ppm (max)	600μA to 10mA	0.6	Precision Bandgap
6.9	±3%	LM129A	10ppm (max)	600μA to 15mA	0.8 (typ)	Low Drift
	±3%	LM129B	20ppm (max)	600μA to 15mA	0.8 (typ)	Low Drift
	±3%	LM129C	50ppm (max)	600μA to 15mA	0.8 (typ)	Low Cost
6.95	±2%	LM199A	0.5ppm (max) − 55°C to +85°C 10ppm (max) + 85°C to +125°C	500μA to 10mA	1.0	Ultra Low Drift
	±2%	LM199	1ppm (max) − 55°C to +85°C 15ppm (max) + 85°C to +125°C	500μA to 10mA	1.0	Ultra Low Drift
7.0	±0.7%	LT1021BM-7	5ppm (max)	1.0mA	0.2	Low Drift/Noise, Exc. Stability
	±0.7%	LT1021DM-7	20ppm (max)	1.0mA	0.2	Low Cost, High Performance
10.0	±0.05%	LT1019AM-10	10ppm (max)	1.0mA	N/A	Precision Bandgap
	±0.2%	LT1019M-10	25ppm (max)	1.2mA	N/A	Precision Bandgap
	±0.5%	LT1021BM-10	5ppm (max)	1.7mA	0.25	Very Low Drift
	±0.05%	LT1021CM-10	20ppm (max)	1.7mA	0.25	Very Tight Initial Tolerance
	±0.5%	LT1021DM-10	20ppm (max)	1.7mA	0.25	Low Cost, High Performance
	±0.05%	LT1031BM	5ppm (max)	1.7mA	0.25	Very Low Drift
	±0.1%	LT1031CM	15ppm (max)	1.7mA	0.25	Very Tight Initial Tolerance
	±0.2%	LT1031DM	25ppm (max)	1.7mA	0.25	Low Cost, High Performance
	±0.3%	AD581J	30ppm (max)	1.0mA	N/A	3 Terminal Low Drift
	±0.1%	AD581T	15ppm (max)	1.0mA	N/A	3 Terminal Low Drift
	±0.05%	AD581U	10ppm (max)	1.0mA	N/A	3 Terminal Low Drift
	±0.05%	LH0070-2	6.7ppm (max)	5.0mA	0.6	Low Drift
	±0.1%	LH0070-1	17ppm (max)	5.0mA	0.6	Good Initial Tolerance
	±0.1%	LH0070-0	33ppm (max)	5.0mA	0.6	Low Cost, High Performance

COMMERCIAL TEMPERATURE RANGE
0°C TO +70°C

VOLTAGE V_Z (VOLTS)	VOLTAGE TOLERANCE MAXIMUM $T_A = 25°C$	DEVICE	TEMPERATURE DRIFT, ppm/°C OR mV CHANGE	OPERATING CURRENT RANGE (OR SUPPLY CURRENT)	MAXIMUM DYNAMIC IMPEDANCE (Ω)	MAJOR FEATURE
1.235	±0.32%	LT1004C-1.2	20ppm (typ)	10μA to 20mA	1.5	Micropower
	±1%	LT1034BC	20ppm(max)	20μA to 20mA	1.5	Low TC Micropower with 7V Aux. Reference
	±1%	LT1034C	40ppm(max)	20μA to 20mA	1.5	Low TC Micropower with 7V Aux. Reference
	±2%	LM385-1.2	20ppm (typ)	15μA to 20mA	1.5	Micropower
	±1%	LM385B-1.2	20ppm (typ)	15μA to 20mA	1.5	Micropower
2.5	±0.5%	LT1004C-2.5	20ppm (typ)	20μA to 20mA	1.5	Micropower
	±0.2%	LT1009C	6mV (max)	400μA to 10mA	1.4	Precision
	±0.2%	LT1019C-2.5	20ppm (max)	1.2mA	N/A	Precision Bandgap
	±0.05%	LT1019AC-2.5	5ppm (max)	1.0mA	N/A	Precision Bandgap
	±4%	LM336-2.5	6mV (max)	400μA to 10mA	1.4	General Purpose
	±2%	LM336B-2.5	6mV (max)	400μA to 10mA	1.4	General Purpose
	±3%	LM385-2.5	20ppm (typ)	20μA to 20mA	1.5	Micropower
	±1.5%	LM385B-2.5	20ppm (typ)	20μA to 20mA	1.5	Micropower
	±3%	AD580J	85 (max)	1.5mA	N/A	3 Terminal Low Drift
	±1%	AD580K	40 (max)	1.5mA	N/A	3 Terminal Low Drift
	±0.4%	AD580L	25 (max)	1.5mA	N/A	3 Terminal Low Drift
	±0.4%	AD580M	10 (max)	1.5mA	N/A	3 Terminal Low Drift
5.0	±0.2%	LT1019C-5	20ppm (max)	1.2mA	N/A	Precision Bandgap
	±0.05%	LT1019AC-5	5ppm (max)	1.0mA	N/A	Precision Bandgap
	±1%	LT1021BC-5	5ppm (max)	1.2mA	0.1	Very Low Drift
	±0.05%	LT1021CC-5	20ppm (max)	1.2mA	0.1	Very Tight Initial Tolerance
	±1%	LT1021DC-5	20ppm (max)	1.2mA	0.1	Low Cost, High Performance
	±0.2%	LT1029AC	20ppm(max)	600μA to 10mA	0.6	Precision Bandgap
	±1%	LT1029C	34ppm(max)	600μA to 10mA	0.6	Precision Bandgap
6.9	±3%	LM329A	10ppm (max)	600μA to 15mA	1.0 (typ)	Low Drift
	±5%	LM329B	20ppm (max)	600μA to 15mA	1.0 (typ)	Low Drift
	±5%	LM329C	50ppm (max)	600μA to 15mA	1.0 (typ)	General Purpose
	±5%	LM329D	100ppm (max)	600μA to 15mA	1.0 (typ)	General Purpose
6.95	±5%	LM399	2ppm (max)	500μA to 10mA	1.5	Ultra Low Drift
	±5%	LM399A	1ppm (max)	500μA to 10mA	1.5	Ultra Low Drift
7.0	±0.7%	LT1021BC-7	5ppm (max)	1.0mA	0.2	Low Drift/Noise, Exc. Stability
	±0.7%	LT1021DC-7	20ppm (max)	1.0mA	0.2	Low Cost, High Performance
10.0	±0.2%	LT1019C-10	20ppm (max)	1.2mA	N/A	Precision Bandgap
	±0.05%	LT1019AC-10	5ppm (max)	1.0mA	N/A	Precision Bandgap
	±0.5%	LT1021BC-10	5ppm (max)	1.7mA	0.25	Very Low Drift
	±0.05%	LT1021CC-10	20ppm (max)	1.7mA	0.25	Very Tight Initial Tolerance
	±0.5%	LT1021DC-10	20ppm (max)	1.7mA	0.25	Low Cost, High Performance
	±0.5%	LT1031BC	5ppm (max)	1.7mA	0.25	Very Low Drift
	±0.1%	LT1031CC	15ppm (max)	1.7mA	0.25	Very Tight Initial Tolerance
	±0.2%	LT1031DC	25ppm (max)	1.7mA	0.25	Low Cost, High Performance
	±0.3%	AD581J	30ppm (max)	1.0mA	N/A	3 Terminal Low Drift
	±0.1%	AD581K	15ppm (max)	1.0mA	N/A	3 Terminal Low Drift
	±0.05%	AD581L	10ppm (max)	1.0mA	N/A	3 Terminal Low Drift

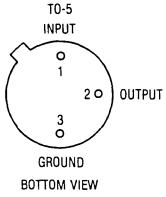
AD580



– FEATURES –
- 2.5V Output
- Direct Replacement for Analog Devices
- Selected Parts with 10ppm/°C TC
- Low Quiescent Current

– MINI DESCRIPTION –
Alternate source for industry standard 2.5V 3 terminal reference

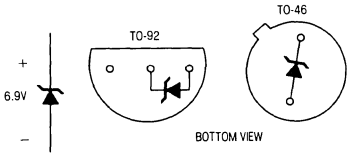
AD581



– FEATURES –
- 10V Output
- Direct Replacement for Analog Devices
- Selected Parts with 10ppm/°C TC
- Low Quiescent Current

– MINI DESCRIPTION –
Alternate source for industry standard 10V 3-terminal reference.

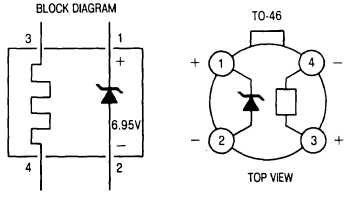
LM129/329



– FEATURES –
- Low Noise
- Low Cost
- Max Temperature Drift Selections 10, 20, 50 and 100 ppm/°C
- Wide Operating Current Range

– MINI DESCRIPTION –
Subsurface zener reference with wide operating current range from 600μA to 15mA. Similar to LM199/399 without stabilizing heater on the die.

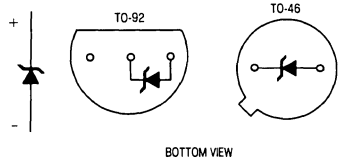
LM199A/199
LM399A/399



– FEATURES –
- Ultra Low Drift
- Very Low Noise
- Wide Operating Current Range
- Provided with Thermal Shield
- Excellent Long Term Stability
- Low Hysteresis
- Guaranteed Long Term Stability Available

– MINI DESCRIPTION –
An on board stabilizing heater keeps the die at constant temperature. Reference is a low noise subsurface zener. Excellent long term stability.

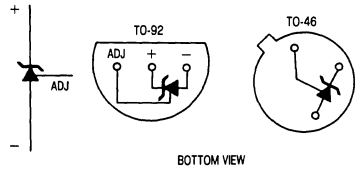
LT1004
LM185/385



– FEATURES –
- Micropower
- 1.235V and 2.5V Available
- Low Dynamic Impedance
- Wide Operating Current Range
- Very Tight Tolerance

– MINI DESCRIPTION –
Bandgap reference with operating current range as low as 10μA. Low noise and good long term stability.

LT1009
LM136/336



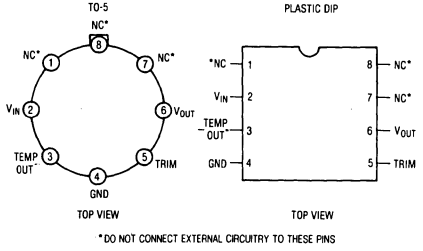
– FEATURES –

- No Adjustment Needed on LT1009
- Temperature Coefficient or Voltage Easily Adjusted on LM136
- Wide Operating Current Range
- Low Cost
- 2.5V
- Very Tight Tolerance

– MINI DESCRIPTION –

General purpose reference using bandgap circuit. Low cost, medium performance.

LT1019



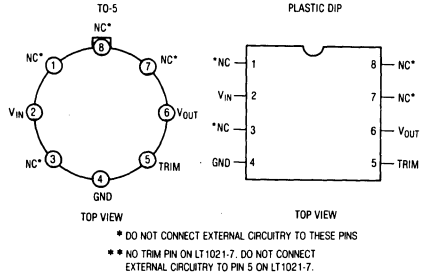
– FEATURES –

- 2.5V, 5V and 10V Versions
- Plug-In Replacement for Many Devices
- Series or Shunt Operation
- Low Drift—3ppm/°C Typ.
- 0.05% Initial Tolerance
- 100% Noise Tested
- Optional Chip Heater Can Be Used for Lower Drift
- Temperature Output

– MINI DESCRIPTION –

Curvature corrected bandgap design for very low drift and tight initial tolerance. Replaces and upgrades REF-01, REF-02, MC14XX and other popular series type references.

LT1021



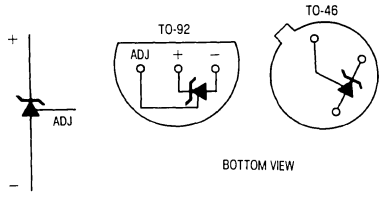
– FEATURES –

- Ultra Low Drift
- Trimmed Output Voltage
- Very Low Noise
- Operates in Series or Shunt Mode
- Replaces REF01, REF02, LM368, MC1400 and MC1404 with Improved Stability, Noise and Drift

– MINI DESCRIPTION –

Trimmed voltage reference with ultra low drift. Reference is a low noise subsurface zener. Available in 5V, 7V and 10V versions. The 7V and 10V versions can be used as 2-terminal shunt regulators as well as series references.

LT1029



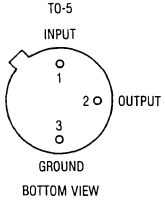
– FEATURES –

- 0.2% Output Tolerance
- 0.5Ω Shunt Impedance
- 600μA to 10mA Operating Current
- Pin Compatible with LM136-5
- 20ppm/°C Max. Drift Output Voltage Trim does not Affect Drift
- Can be Used as Positive or Negative Reference

– MINI DESCRIPTION –

Precision 3 terminal shunt 5V bandgap reference. Very low drift and tight intial output tolerance.

LT1031/LH0070



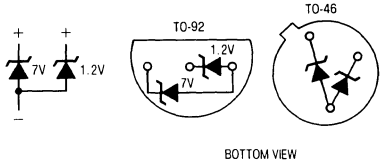
– FEATURES –

- 10V Output
- Ultra Low Drift
- Very Low Noise
- Trimmed Output Voltage
- Operates in Series or Shunt Mode
- Pin Compatible with AD581
- LH0070 is a Direct Replacement for NSC LH0070

– MINI DESCRIPTION –

Very low tempco is achieved without chip heater. The LT1031 can replace the AD581 with better specifications.

LT1034



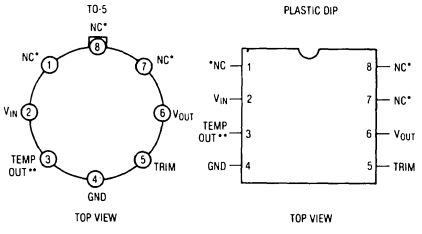
– FEATURES –

- *Guaranteed* Drift (1.2V) of 20ppm/°C and 40ppm/°C
- 1.2V and 7V Reference
- 1.2V Reference operates 20μA to 20mA
- 1% Tolerance on 1.2V Reference
- 7V Reference Operates 100μA to 20mA
- Compatible with the LM385 and LT1004

– MINI DESCRIPTION –

The LT1034 is a bandgap 1.2V reference with low operating current and low temperature coefficient, combined with a 7V subsurface zener reference on the same chip.

REF-01/REF-02



*DO NOT CONNECT EXTERNAL CIRCUITRY TO THESE PINS
**REF-02 ONLY.

– FEATURES –

- Direct Replacement for PMI Devices
- Low Drift
- High Line Rejection
- Low Supply Current
- Temperature Output on REF-02

– MINI DESCRIPTION –

Industry standard 5V and 10V bandgap voltage references.

FEATURES

- *Guaranteed* ±4mV initial accuracy LT1004-1.2
- *Guaranteed* ±20mV accuracy LT1004-2.5
- *Guaranteed* 10μA operating current
- *Guaranteed* temperature performance
- Operates up to 20mA
- Very low dynamic impedance

APPLICATIONS

- Portable meter references
- Portable test instruments
- Battery operated systems
- Current loop instrumentation

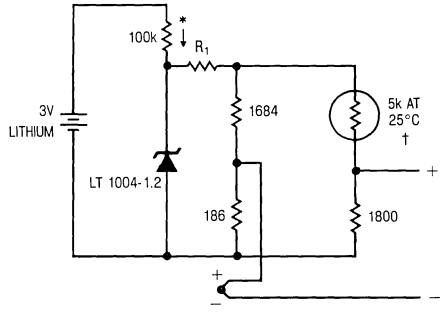
DESCRIPTION

The LT1004 Micropower Voltage References are two terminal bandgap reference diodes designed to provide high accuracy and excellent temperature characteristics at very low operating currents. Optimization of the key parameters in the design, processing and testing of the device results in accuracy specifications previously attainable only with selected units. Below is a distribution plot of reference voltage for a typical lot of LT1004-1.2. Virtually all of the units fall well within the prescribed limits of ±4mV.

The LT1004 is a pin for pin replacement for the LM185/385 series of references with improved accuracy specifications. More important, the LT1004 is an attractive device for use in systems where accuracy was previously obtained at the expense of power consumption and trimming.

For a low drift micropower reference with guaranteed temperature coefficient, see the LT1034 data sheet.

Micropower Cold Junction Compensation For Thermocouples



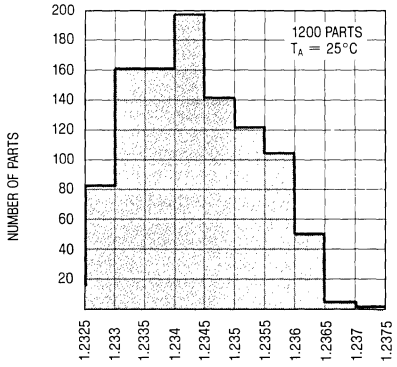
THERMOCOUPLE TYPE	R_1
J	233k
K	299k
T	300k
S	2.1M

* QUIESCENT CURRENT ≃ 15μA

† YELLOW SPRINGS INST. CO. PART #44007

COMPENSATES WITHIN ±1°C FROM 0°C TO 60°C

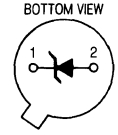
Typical Distribution of Reference Voltage (LT1004-1.2)



ABSOLUTE MAXIMUM RATINGS

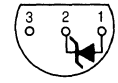
Reverse Breakdown Current..... 30mA
Forward Current..... 10mA
Operating Temperature Range
LT1004M ..... −55°C to 125°C
LT1004C ..... 0°C to 70°C
Storage Temperature Range
LT1004M ..... −65°C to 150°C
LT1004C ..... −65°C to 150°C
Lead Temperature (Soldering, 10 sec.)..... 300°C

PACKAGE/ORDER INFORMATION



H PACKAGE
TO-46 METAL CAN

LT1004MH
LT1004CH



Z PACKAGE
TO-92 PLASTIC

LT1004CZ

ELECTRICAL CHARACTERISTICS (See Note 1)

SYMBOL	PARAMETER	CONDITIONS		LT1004-1.2 MIN	LT1004-1.2 TYP	LT1004-1.2 MAX	LT1004-2.5 MIN	LT1004-2.5 TYP	LT1004-2.5 MAX	UNITS
V_Z	Reverse Breakdown Voltage	$I_R = 100\mu A$		1.231	1.235	1.239	2.480	2.500	2.520	V
		LT1004M $-55°C \leq T_A \leq 125°C$	●	1.220	1.230	1.245	2.460	2.500	2.535	V
		LT1004M/C $0°C \leq T_A \leq 70°C$	●	1.225	1.235	1.245	2.470	2.500	2.530	V
$\frac{\Delta V_Z}{\Delta \text{Temp}}$	Average Temperature Coefficient	$I_{min} \leq I_R \leq 20mA$ (Note 2)			20			20		ppm/°C
I_{min}	Minimum Operating Current		●		8	10		12	20	μA
$\frac{\Delta V_Z}{\Delta I_R}$	Reverse Breakdown Voltage Change with Current	$I_{min} \leq I_R \leq 1mA$				1			1	mV
			●			1.5			1.5	mV
		$1mA \leq I_R \leq 20mA$				10			10	mV
			●			20			20	mV
r_Z	Reverse Dynamic Impedance	$I_R = 100\mu A$			0.2	0.6		0.2	0.6	Ω
			●			1.5			1.5	Ω
e_n	Wide Band Noise (RMS)	$I_R = 100\mu A$ $10Hz \leq f \leq 10kHz$			60			120		μV
$\frac{\Delta V_Z}{\Delta \text{Time}}$	Long Term Stability	$I_R = 100\mu A$ $T_A = 25°C \pm 0.1°C$			20			20		ppm/kHr

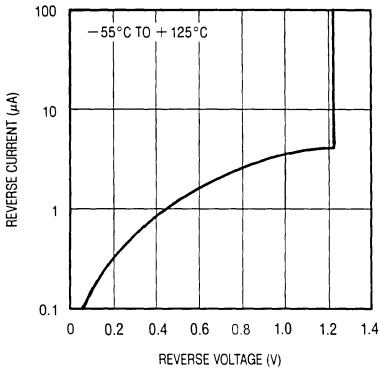
The ● denotes the specifications which apply over the full operating temperature range.

Note 1: All specifications are for $T_A = 25°C$ unless otherwise noted.

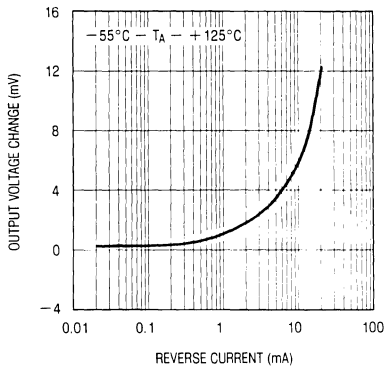
Note 2: Selected devices with guaranteed maximum temperature coefficient are available upon request.

TYPICAL PERFORMANCE CHARACTERISTICS 1.2 VOLT

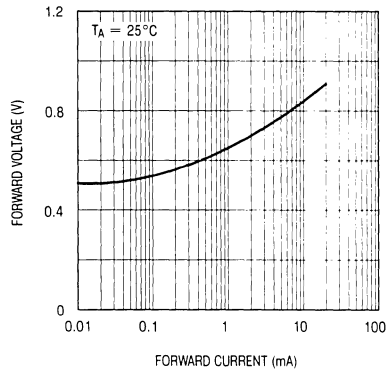
Reverse Characteristics



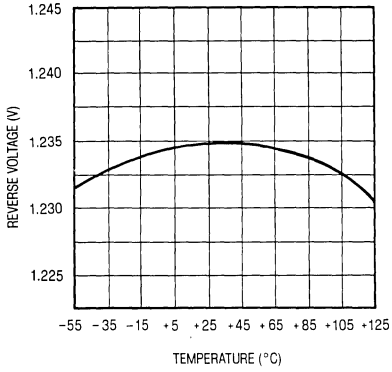
Reverse Voltage Change



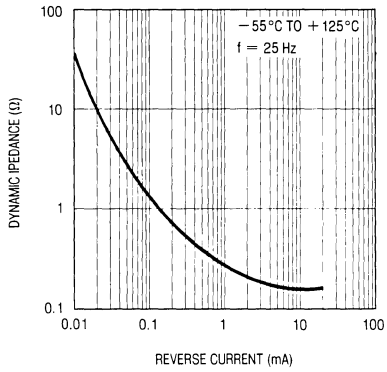
Forward Characteristics



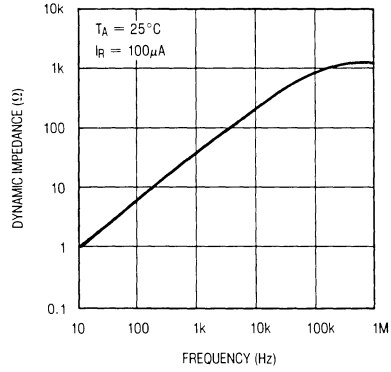
Temperature Drift



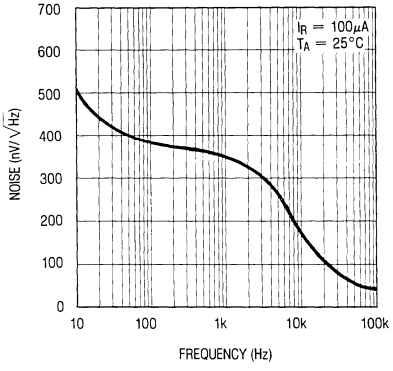
Reverse Dynamic Impedance



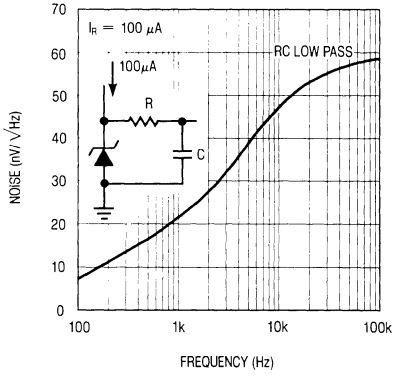
Reverse Dynamic Impedance



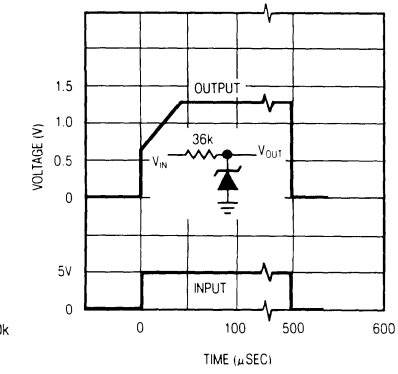
Noise Voltage



Filtered Output Noise

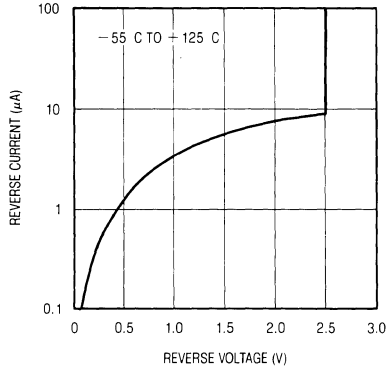


Response Time

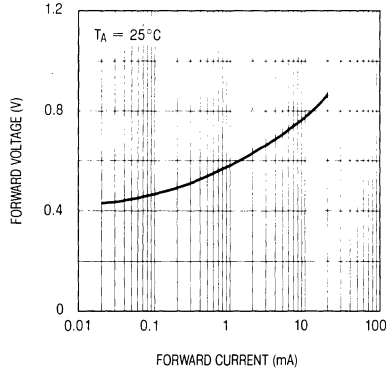


TYPICAL PERFORMANCE CHARACTERISTICS 2.5 VOLT

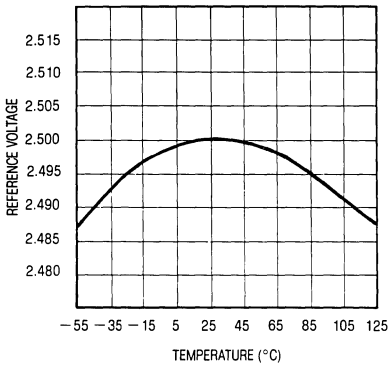
Reverse Characteristics



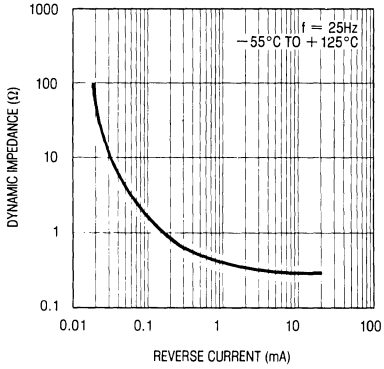
Forward Characteristics



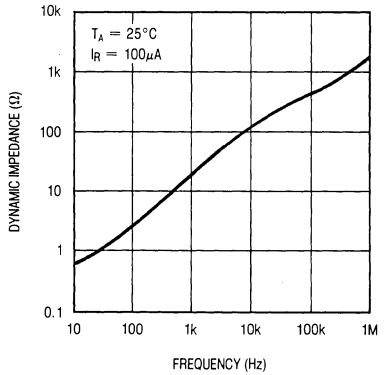
Temperature Drift



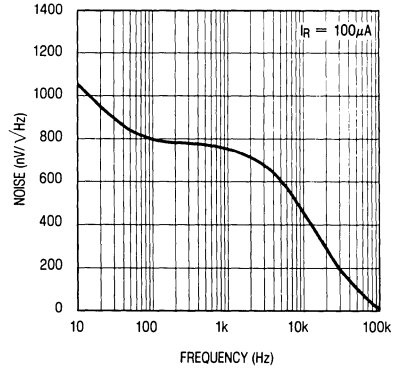
Reverse Dynamic Impedance



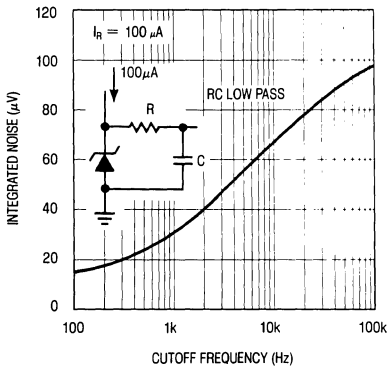
Reverse Dynamic Impedance



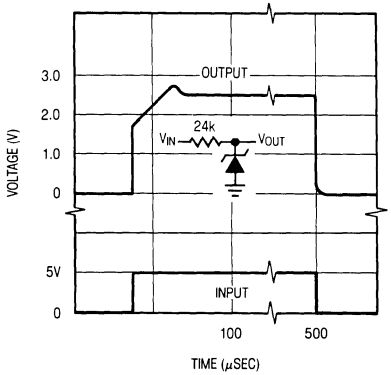
Noise Voltage



Filtered Output Noise

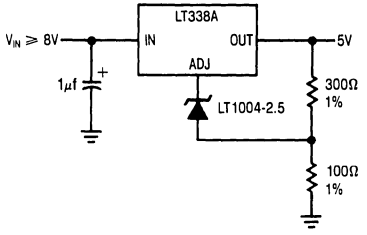


Response Time

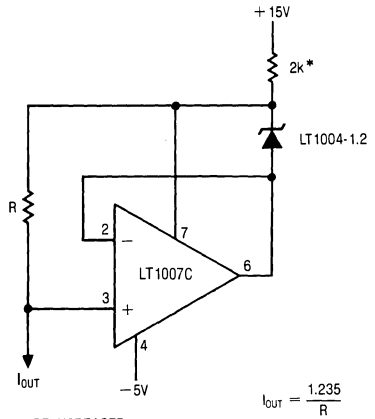


TYPICAL APPLICATIONS

High Stability 5V Regulator



Ground Referenced Current Source

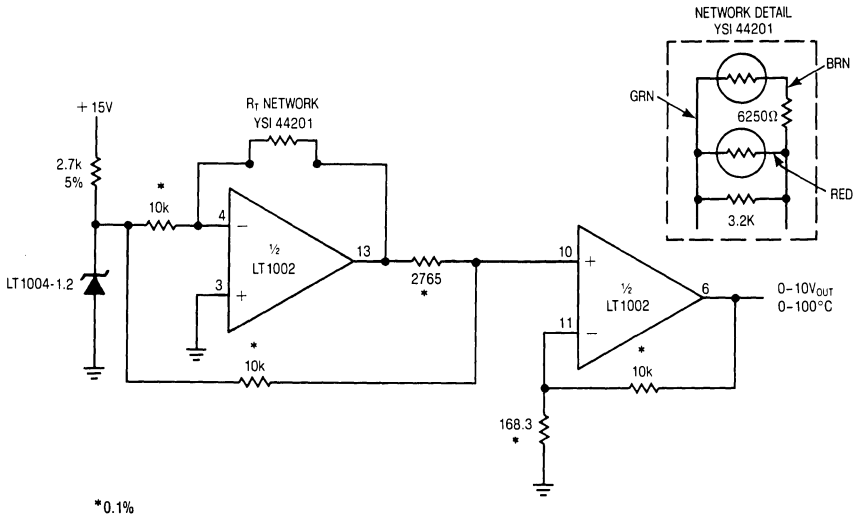


$$I_{OUT} = \frac{1.235}{R}$$

* MAY BE INCREASED FOR SMALL OUTPUT CURRENTS

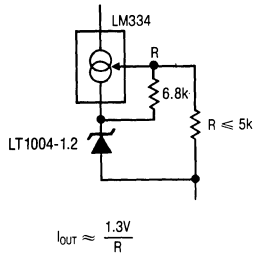
$$R \approx \frac{2V}{I_{OUT} + 10\mu A}$$

0-100°C Linear Output Thermometer

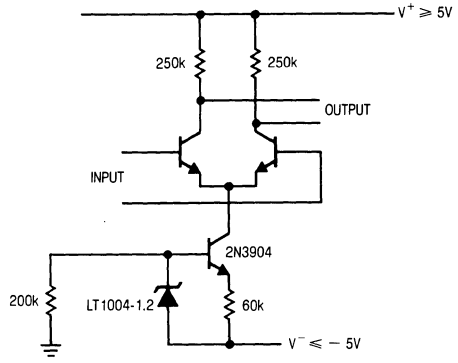


TYPICAL APPLICATIONS

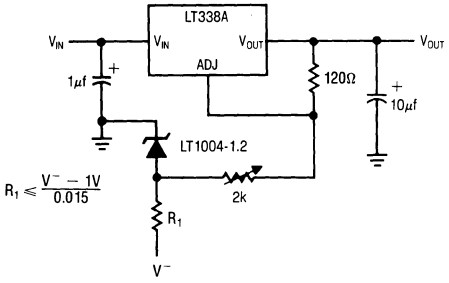
Low Temperature Coefficient 2 Terminal Current Source



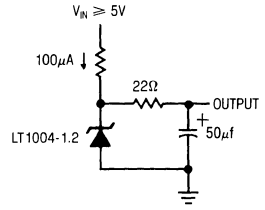
Constant Gain Amplifier Over Temperature



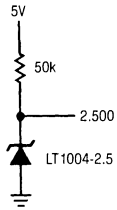
Variable Output Supply



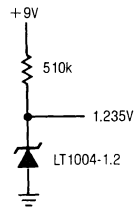
Low Noise Reference



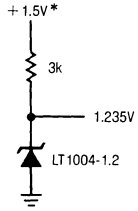
2.5V Reference



Micropower Reference from 9V Battery



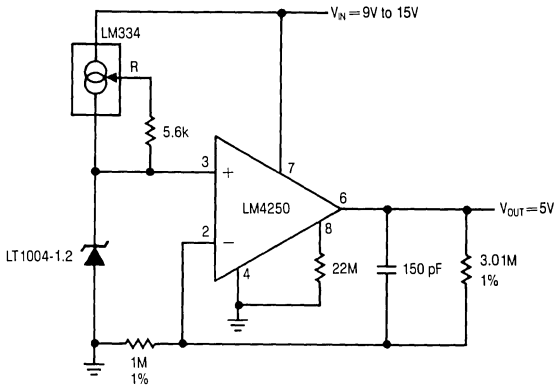
1.2V Reference from 1.5V Battery



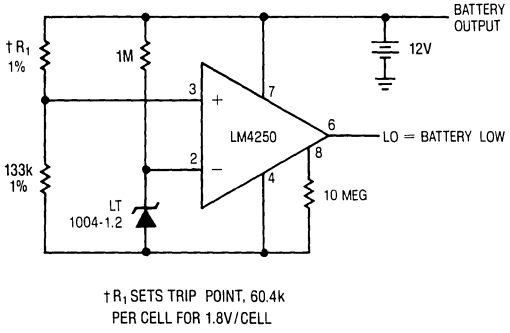
* OUTPUT REGULATES DOWN TO 1.285V FOR $I_{OUT} = 0$

TYPICAL APPLICATIONS

Micropower 5V Reference

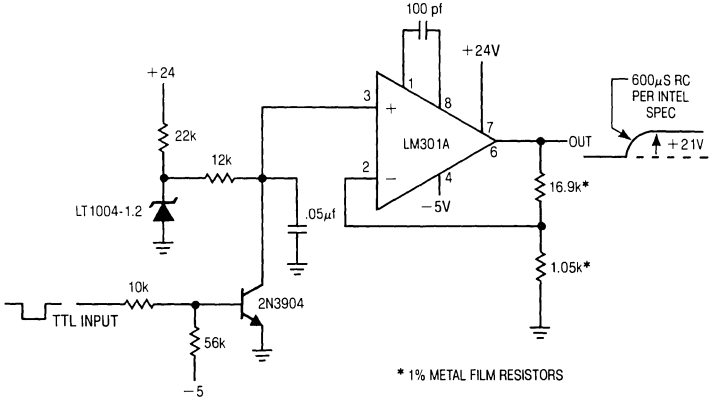


Lead Acid Low Battery Detector



†R_1 SETS TRIP POINT, 60.4k
PER CELL FOR 1.8V/CELL

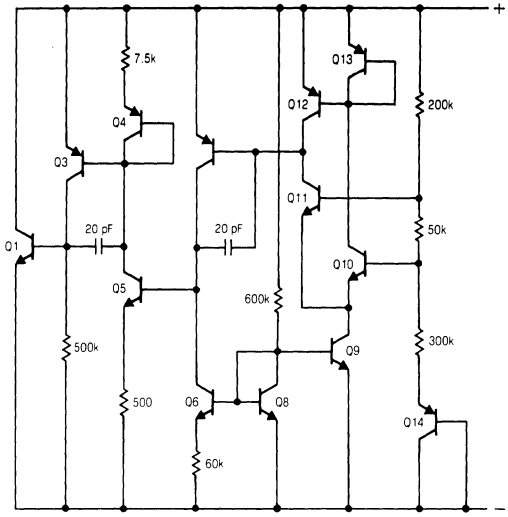
V_{pp} Generator for Eproms — No Trim Required



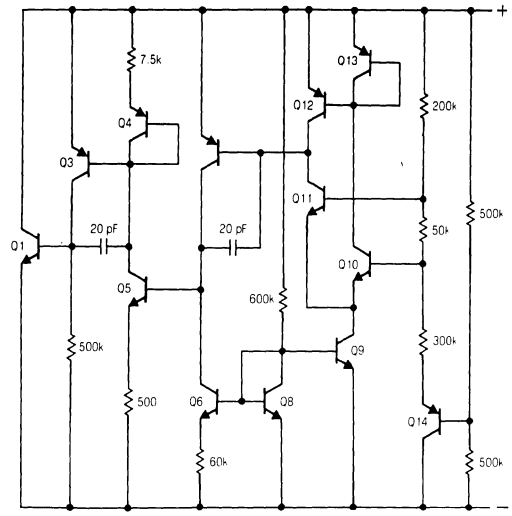
* 1% METAL FILM RESISTORS

SCHEMATIC DIAGRAM

LT1004-1.2



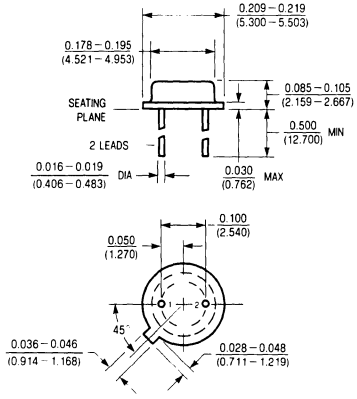
LT1004-2.5



PACKAGE DESCRIPTION

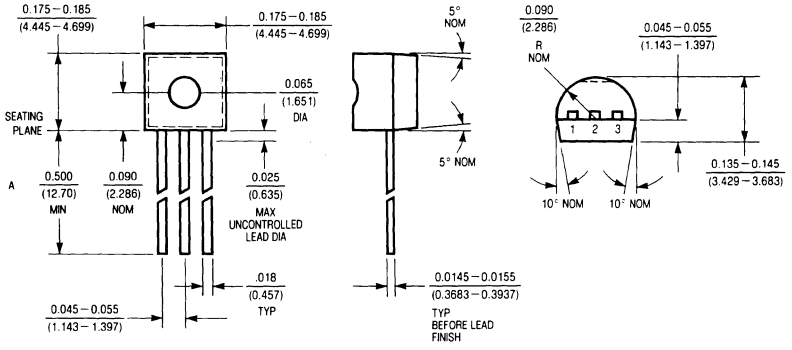
Dimensions in inches (millimeters) unless otherwise noted.

H Package, 2 Lead TO-46 Metal Can



$T_j$max	Θ_{ja}	Θ_{jc}
150°C	440°C/W	80°C/W

Z Package, 3 Lead TO-92 Plastic



$T_j$max	Θ_{ja}
100°C	160°C/W

FEATURES

- 0.2% Initial Tolerance Max
- *Guaranteed* Temperature Stability
- Maximum 0.6Ω Dynamic Impedance
- Wide Operating Current Range
- Directly Interchangeable with LM136 for Improved Performance
- No Adjustments Needed for Minimum Temperature Coefficient

APPLICATIONS

- Reference for 5V Systems
- 8 Bit A/D and D/A Reference
- Digital Voltmeters
- Current Loop Measurement and Control Systems
- Power Supply Monitor

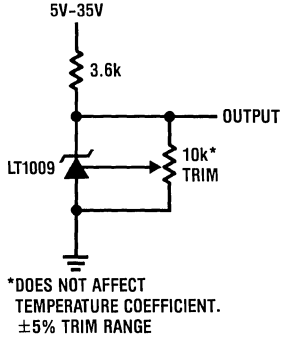
DESCRIPTION

The LT1009 is a precision trimmed 2.500 Volt shunt regulator diode featuring a maximum initial tolerance of only ±5mV. The low dynamic impedance and wide operating current range enhances its versatility. The 0.2% reference tolerance is achieved by on-chip trimming which not only minimizes the initial voltage tolerance but also minimizes the temperature drift.

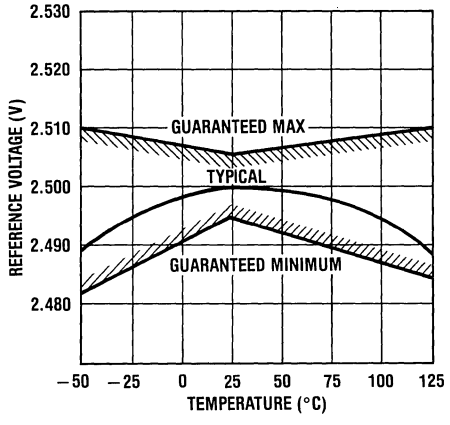
Even though no adjustments are needed with the LT1009, a third terminal allows the reference voltage to be adjusted ±5% to calibrate out system errors. In many applications, the LT1009 can be used as a pin-to-pin replacement of the LM136H-2.5 and the external trim network eliminated.

For a lower drift 2.5V reference, see the LT1019 data sheet.

2.5 Volt Reference



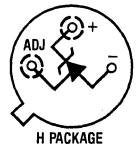
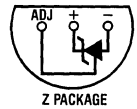
Output Voltage



ABSOLUTE MAXIMUM RATINGS

Reverse Current 20mA
Forward Current 10mA
Operating Temperature Range
LT1009M ..... −55°C to 125°C
LT1009C ..... 0°C to 70°C
Storage Temperature Range
LT1009M and C ..... −65°C to 150°C
Lead Temperature (Soldering, 10 sec.)..... 300°C

PACKAGE/ORDER INFORMATION

	ORDER PART NUMBER
BOTTOM VIEW  H PACKAGE TO-46 METAL CAN	LT1009MH LT1009CH
BOTTOM VIEW  Z PACKAGE TO-92 PLASTIC	LT1009CZ

ELECTRICAL CHARACTERISTICS

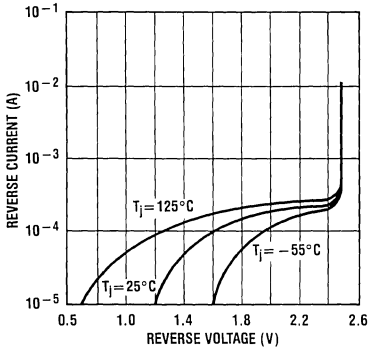
SYMBOL	PARAMETER	CONDITIONS		LT1009M MIN	LT1009M TYP	LT1009M MAX	LT1009C MIN	LT1009C TYP	LT1009C MAX	UNITS
V_Z	Reverse Breakdown Voltage	$T_A = 25°C$, $I_R = 1mA$		2.495	2.500	2.505	2.495	2.500	2.505	V
$\frac{\Delta V_Z}{\Delta I_R}$	Reverse Breakdown Change with Current	$400\mu A \le I_R \le 10mA$			2.6	6		2.6	10	mV
			●		3	10		3	12	mV
r_Z	Reverse Dynamic Impedance	$I_R = 1mA$			0.2	0.6		0.2	1.0	Ω
			●		0.4	1		0.4	1.4	Ω
$\frac{\Delta V_Z}{\Delta Temp}$	Temperature Stability	$T_{MIN} \le T_A \le T_{MAX}$	●			15		1.8	4	mV
	Average Temperature Coefficient	$0°C \le T_A \le 70°C$			15	25		15	25	ppm/°C
		$-55°C \le T_A \le 125°C$ (Note 1)			25	35				ppm/°C
$\frac{\Delta V_Z}{\Delta Time}$	Long Term Stability	$T_A = 25°C \pm 0.1°C$, $I_R = 1mA$			20			20		ppm/kHr

The ● denotes the specifications which apply over full operating temperature range.

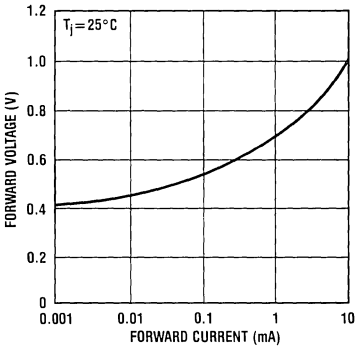
Note 1: Average temperature coefficient is defined as the total voltage change divided by the specified temperature range.

TYPICAL PERFORMANCE CHARACTERISTICS

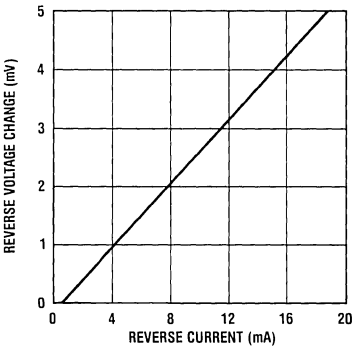
Reverse Characteristics



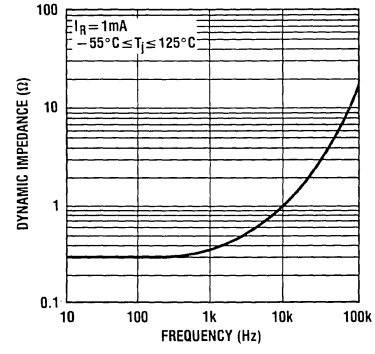
Forward Characteristics



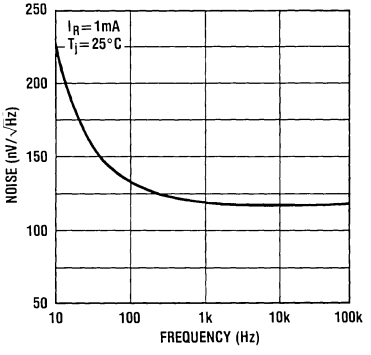
Reverse Voltage Change



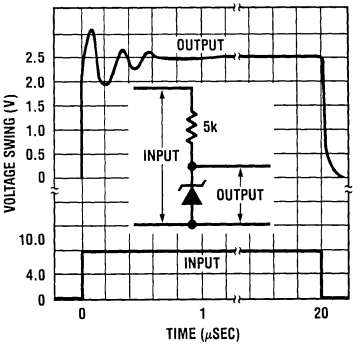
Dynamic Impedance



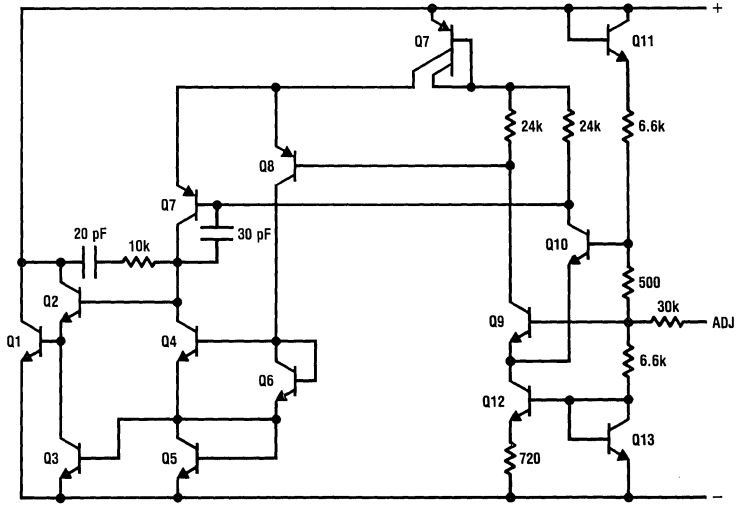
Zener Noise Voltage



Response Time

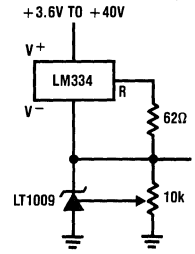


SCHEMATIC DIAGRAM

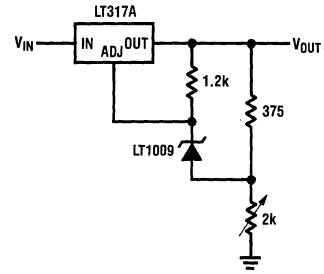


TYPICAL APPLICATIONS

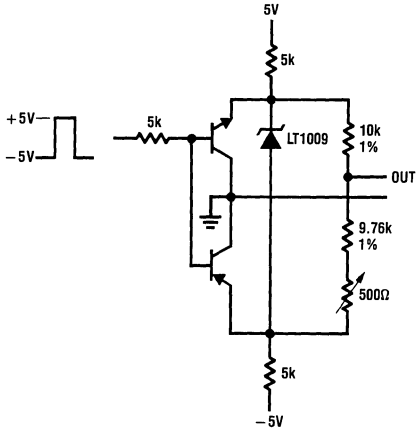
Wide Supply Range, Adjustable Reference



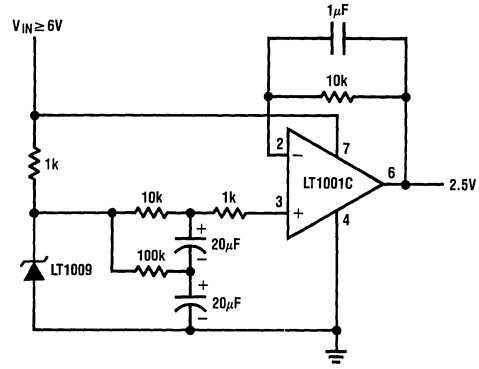
Low Temperature Coefficient Power Regulator



Switchable ±1.25V Bipolar Reference



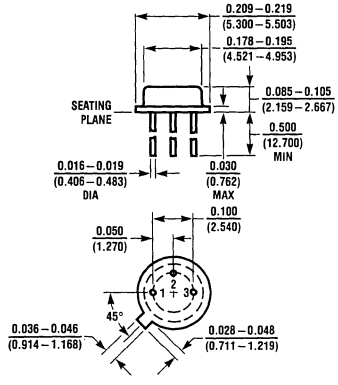
Low Noise 2.5V Buffered Reference



PACKAGE DESCRIPTION

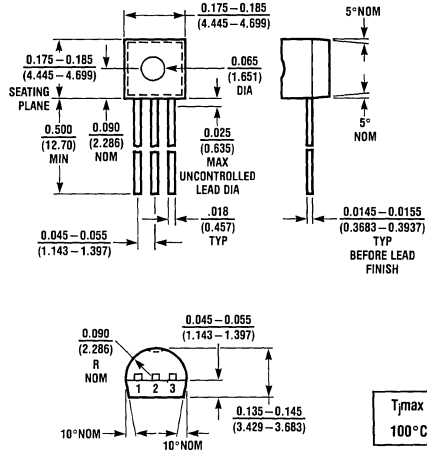
Dimensions in inches (millimeters) unless otherwise noted.

H Package
Metal Can



$T_j$max	θ_{ja}	θ_{jc}
150°C	440°C/W	80°C/W

Z Package
Plastic



$T_j$max	θ_{ja}
100°C	160°C/W

FEATURES

- Plug-In Replacement for Present References
- Ultra Low Drift—3ppm/°C Typical
- Curvature Corrected
- Series or Shunt Operation
- Ultra High Line Rejection ≈ ½ppm/V
- Low Output Impedance ≈0.02Ω
- Tight Initial Output Voltage <0.05%
- Can be Heated for Drifts below 2ppm/°C
- 100% Noise Tested
- Temperature Output

APPLICATIONS

- A to D and D to A Converters
- Precision Regulators
- Constant Current Sources
- V to F Converters
- Bridge Excitation

DESCRIPTION

The LT1019 is a third generation bandgap voltage reference utilizing thin film technology and a greatly improved curvature correction technique. Wafer level trimming of both reference and output voltage combines to produce units with high yields to very low TC and tight initial tolerance of output voltage.

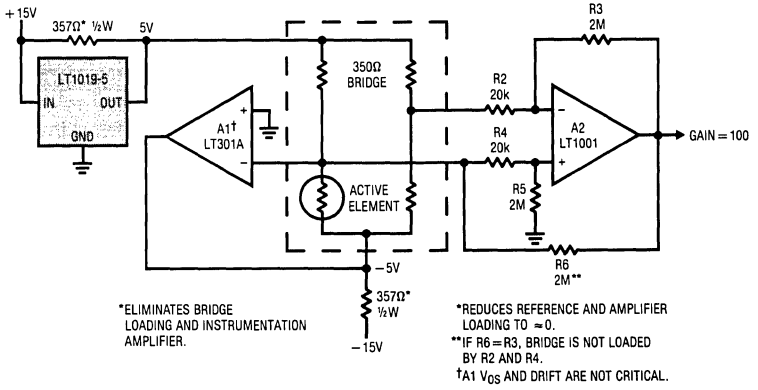
The LT1019 can both sink and source up to 10mA and can be used in either the series or shunt mode. This allows the reference to be used for both positive and negative output voltages without external components. Minimum input-output voltage is less than 1V in the series mode, providing improved tolerance of low line conditions.

The LT1019 is available in three voltages: 2.5V, 5V, and 10V. It is a direct replacement for most bandgap references presently available including AD580, AD581, REF-01, REF-02, MC1400, MC1404 and LM168.

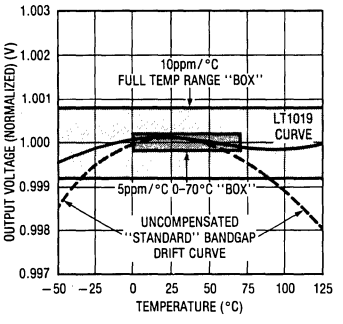
For ultra low drift applications (<2ppm/°C), the LT1019 can be operated in a heated mode by driving an internal resistor with an external amplifier. Chip temperature can be externally set for minimum power consumption.

For a 6.2V version of the LT1019, consult the factory.

Ultralinear Strain Gauge*



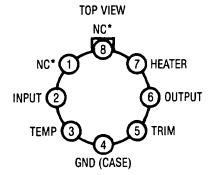
Output Voltage Drift



ABSOLUTE MAXIMUM RATINGS

Input Voltage 40V
Output Voltage ($V_{IN} \geq V_{OUT}$) (Note 1) 16V
Output Short Circuit Duration (Note 1)
$V_{IN} \geq 20V$ ..... Indefinite
$20V \leq V_{IN} \leq 35V$ ..... 10 sec
Trim Pin Voltage ..... ±30V
Temp Pin Voltage 5V
Heater Voltage
(Continuous) 18V
(Intermittent—30 sec.) 32V

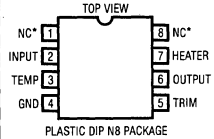
PACKAGE/ORDER INFORMATION



METAL CAN H PACKAGE
*INTERNALLY CONNECTED. DO NOT CONNECT EXTERNALLY.

ORDER PART NUMBER

LT1019AMH-10 LT1019ACH-5
LT1019MH-10 LT1019CH-5
LT1019ACH-10 LT1019AMH-2.5
LT1019CH-10 LT1019MH-2.5
LT1019AMH-5 LT1019ACH-2.5
LT1019MH-5 LT1019CH-2.5



PLASTIC DIP N8 PACKAGE
*INTERNALLY CONNECTED. DO NOT CONNECT EXTERNALLY.

LT1019ACN8-10
LT1019CN8-10
LT1019ACN8-5
LT1019CN8-5
LT1019ACN8-2.5
LT1019CN8-2.5

ELECTRICAL CHARACTERISTICS

$V_{IN} - V_{OUT} = 5V$, $I_{OUT} = 0$, $T_J = 25°C$ unless otherwise noted

SYMBOL	PARAMETER	CONDITIONS		LT1019A MIN	LT1019A TYP	LT1019A MAX	LT1019 MIN	LT1019 TYP	LT1019 MAX	UNITS
	Output Voltage Tolerance				0.002	0.05		0.02	0.2	%
T_C	Output Voltage Temperature Coefficient (Note 2)	LT1019C (0°C to 70°C)	●		3	5		5	20	ppm/°C
		LT1019M (−55°C to +125°C)	●		5	10		8	25	ppm/°C
$\frac{\Delta V_{OUT}}{\Delta V_{IN}}$	Line Regulation (Note 3)	$(V_{OUT} + 1.5V) \leq V_{IN} \leq 40V$			0.5	3		0.5	3	ppm/V
			●		1	5		1	5	ppm/V
RR	Ripple Rejection	$50Hz \leq f \leq 400Hz$		90	110		90	110		dB
			●	84			84			dB
$\frac{\Delta V_{OUT}}{\Delta I_{OUT}}$	Load Regulation Series Mode (Notes 3 and 4)	$0 \leq I_{OUT} \leq 10mA$*			0.02	0.05		0.02	0.05	mV/mA (Ω)
			●			0.08			0.08	mV/mA (Ω)
	Load Regulation Sink (Shunt Mode)	$I_{MIN} \leq I_{SINK} \leq 10mA$ (Notes 4 and 5)			0.1	0.3		0.1	0.3	mV/mA (Ω)
			●			0.4			0.4	mV/mA (Ω)
	Thermal Regulation (Note 6)	$\Delta P = 200mW$, $t = 50ms$			0.1	0.5		0.1	0.5	ppm/mW
I_Q	Quiescent Current Series Mode				0.65	1		0.65	1.2	mA
			●			1.3			1.5	mA
	Minimum Shunt Current	(Note 7)	●		0.5	0.8		0.5	0.8	mA
	Minimum Input-Output Voltage Differential	$I_{OUT} \leq 1mA$	●		0.9	1.1		0.9	1.1	V
		$I_{OUT} = 10mA$	●			1.3			1.3	V
	Trim Range	LT1019-2.5		±4	±6		±4	±6		%
		LT1019-5		±4	+5, −13		±4	+5, −13		%
		LT1019-10		±4	+5, −27		±4	+5, −27		%
	Heater Resistance			300	400	500	300	400	500	Ω
I_{SC}	Short Circuit Current Output Connected to Ground	$2V \leq V_{IN} \leq 35V$		15	25	50	15	25	50	mA
			●	10			10			mA
e_n	Output Voltage Noise (Note 9)	$10Hz \leq f \leq 1kHz$			2.5	4		2.5	4	ppm (Rms)
		$0.1Hz \leq f \leq 10Hz$			2.5			2.5		ppm (p-p)

The ● denotes the specifications which apply over the full operating temperature range.

Note 1: These are high power conditions and are therefore guaranteed only at temperatures equal to or below 35°C.

Note 2: Output voltage drift is measured using the box method. Output voltage is recorded at T_{MIN}, 25°C, and T_{MAX}. The lowest of these three readings is subtracted from the highest and the resultant difference is divided by ($T_{MAX} - T_{MIN}$).

Note 3: Line regulation and load regulation are measured on a pulse basis with low duty cycle. Effects due to die heating must be taken into account separately. See thermal regulation and application section.

Note 4: Load regulation is measured at a point 1/8" below the base of the package with Kelvin contacts.

Note 5: I_{MIN} is equal to minimum shunt current when in the shunt mode (V_{IN} disconnected). In sink mode, $I_{MIN} = 0$.

Note 6: Thermal regulation is caused by die temperature gradients created by load current or input voltage changes. This effect must be added to normal line or load regulation.

Note 7: Minimum shunt current is measured with shunt voltage held 20mV below value measured at 1mA shunt current.

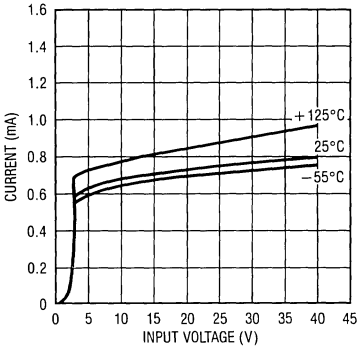
Note 8: Minimum input-output voltage is measured by holding input voltage 0.5V above the nominal output voltage, while measuring $V_{IN} - V_{OUT}$.

Note 9: RMS noise is measured with a single high pass filter at 10Hz and a 2-pole low pass filter at 1kHz. The resulting output is full wave rectified and then integrated for a fixed period, making the final reading an average as opposed to RMS. A correction factor of 1.1 is used to convert from average to RMS, and a second correction of 0.88 is used to correct for the non-ideal bandpass of the filters.

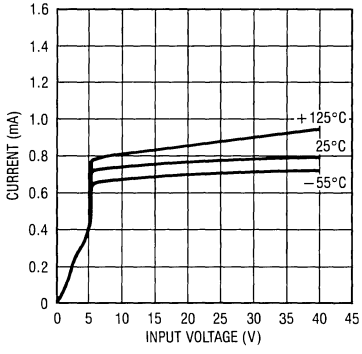
Peak-to peak noise is measured with a single high pass filter at 0.1Hz and a 2-pole low pass filter at 10Hz. The unit is enclosed in a still-air environment to eliminate thermocouple effects on the leads. Test time is 10 seconds.

TYPICAL PERFORMANCE CHARACTERISTICS

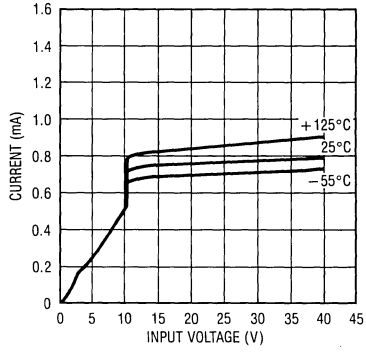
Quiescent Current (LT1019-2.5)



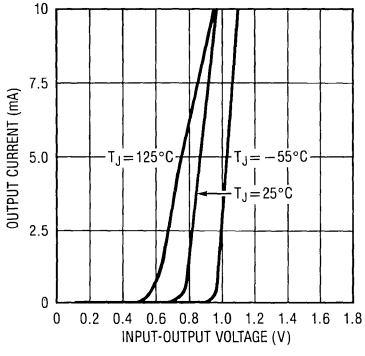
Quiescent Current (LT1019-5)



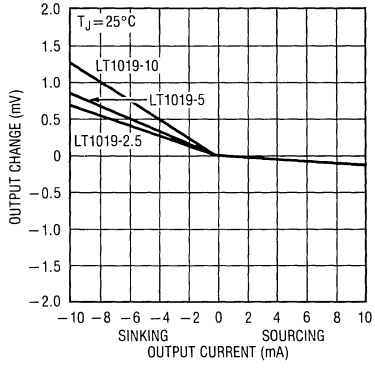
Quiescent Current (LT1019-10)



Minimum Input-Output Voltage Differential

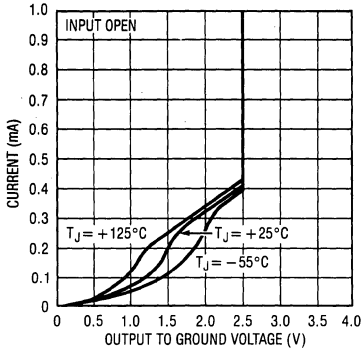


Load Regulation

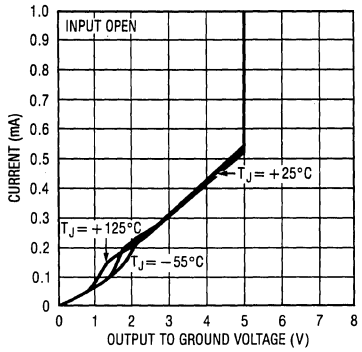


TYPICAL PERFORMANCE CHARACTERISTICS

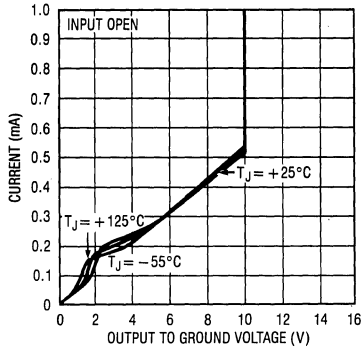
Shunt Mode Characteristics (LT1019-2.5V)



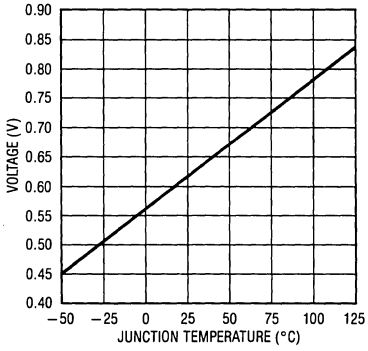
Shunt Mode Characteristics (LT1019-5)



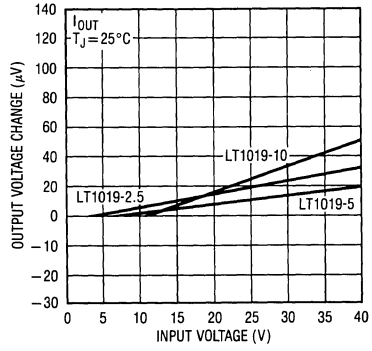
Shunt Mode Characteristics (LT1019-10)



Temp Pin Voltage



Line Regulation



APPLICATIONS INFORMATION

Line and Load Regulation

Line regulation on the LT1019 is nearly perfect. A 10V change in input voltage causes a typical output shift of less than 5ppm. Load regulation (sourcing current) is nearly as good. A 5mA change in load current shifts output voltage by only 100μV. These are *electrical* effects, measured with low duty cycle pulses to eliminate heating effects. In real world applications, the *thermal* effects of load and line changes must be considered.

Two separate thermal effects are evident in monolithic circuits. One is a gradient effect, where power dissipation on the die creates temperature gradients. These gradients can cause output voltage shifts *even if the overall temperature coefficient of the reference is zero.* The LT1019, unlike previous references, specifies thermal regulation caused by die temperature gradients. The specification is 0.5ppm/mW. To calculate the effect on

APPLICATIONS INFORMATION

output voltage, simply multiply the *change* in device power dissipation by the thermal regulation specification. Example: a 10V device with a nominal input voltage of 15V and load current of 5mA. Find the effect of an input voltage change of 1V and a load current change of 2mA.

$$\Delta P \text{ (line change)} = (\Delta V_{IN})(I_{LOAD}) = (1V)(5mA) = 5mW$$
$$\Delta V_{OUT} = (0.5ppm/mW)(5mW) = 2.5ppm$$
$$\Delta P \text{ (load change)} = (\Delta I_{LOAD})(V_{IN} - V_{OUT})$$
$$= (2mA)(5V) = 10mW$$
$$\Delta V_{OUT} = (0.5ppm/mW)(10mW) = 5ppm$$

Even though these effects are small, they should be taken into account in critical applications, especially where input voltage or load current is high.

The second thermal effect is overall die temperature change. The magnitude of this change is the product of change in power dissipation times the thermal resistance (Θ_{JA}) of the IC package $\simeq$ (100°C/W–150°C/W). The effect on reference output is calculated by multiplying die temperature change by the temperature drift specification of the reference. Example: same conditions as above with Θ_{JA} = 150°C/W and an LT1019 with 20ppm/°C drift specification.

$$\Delta P \text{ (line change)} = 5mW$$
$$\Delta V_{OUT} = (5mW)(150°C/W)(20ppm/°C)$$
$$= 15ppm$$
$$\Delta P \text{ (load change)} = 10mW$$
$$\Delta V_{OUT} = (10mW)(150°C/W)(20ppm/°C)$$
$$= 30ppm$$

These calculations show that thermally induced output voltage variations can easily exceed the electrical effects. In critical applications where shifts in power dissipation are expected, a small clip-on heat sink can significantly improve these effects by reducing overall die temperature change. Alternately, an LT1019A can be used with 4 times lower TC. If warm-up drift is of concern, these measures will also help. With warm-up drift, *total* device power dissipation must be considered. In the example given, warm-up drift (worst-case) is equal to:

$$\text{Warm-up drift} = [(V_{IN})(I_Q) + (V_{IN} - V_{OUT})(I_{LOAD})]$$
$$[(\Theta_{JA})(TC)]$$

with I_Q (quiescent current) = 0.6mA,

$$\text{warm-up drift} = [(15V)(0.6mA) + (5V)(5mA)]$$
$$[(150°C/W)(25ppm/°C)]$$
$$= 127.5ppm$$

Note that 74% of the warm-up drift is due to load current times input-output differential. This emphasizes the importance of keeping both these numbers low in critical applications. With heavy loads, warm-up drift can also be improved using the technique described under "Driving Loads Above 10mA", or by heat sinking.

Driving Loads Above 10mA

The LT1019 is guaranteed to drive loads up to 10mA. Much higher load currents can be accommodated by adding an external PNP (see application circuits), but this is often not necessary for relatively constant loads in the 10mA–40mA range. Instead, a resistor is added from input to output with a value chosen to supply most of the load current. The LT1019 can both sink and source current, so it maintains proper reference voltage as long as the difference between resistor current and load current does not exceed 10mA. The example shown in Figure 1 assumes an input voltage of 14.5V to 15.5V, a reference voltage of 10V, and a load current of 25mA–35mA. The resistor is chosen to supply nominal load current at nominal input voltage. This causes the LT1019 to operate in the source or sink mode, depending on load or line conditions. The resistor value may be modified in some cases to create all-source or all-sink conditions to minimize power dissipation in the reference or to keep power supply current to a minimum.

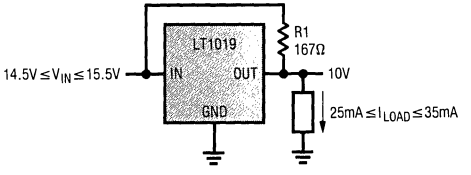


Figure 1

APPLICATIONS INFORMATION

Note that line regulation is now affected by reference output impedance. R1 should have a wattage rating high enough to withstand full input voltage if output shorts must be tolerated. Even with load currents below 10mA, R1 can be used to reduce power dissipation in the LT1019 for lower warm-up drift, etc.

Output Trimming

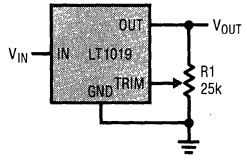
Output voltage trimming on the LT1019 is nominally accomplished with a potentiometer connected from output to ground with the wiper tied to the trim pin. The LT1019 was made compatible with existing references, so the trim range is large; +6%, −6% for the LT1019-2.5, +5%, −13% for the LT1019-5, and +5%, −27% for the LT1019-10. This large trim range makes precision trimming rather difficult. One solution is to insert resistors in series with both ends of the potentiometer. This has the disadvantage of potentially poor tracking between the fixed resistors and the potentiometer. A second method of reducing trim range is to insert a resistor in series with the wiper of the potentiometer. This works well only for very small trim range because of the mismatch in TCs between the series resistor and the internal thin film resistors. These film resistors can have a TC as high as 500ppm/°C. That same TC is then transferred to the change in output voltage; a 1% shift in output voltage causes a (500ppm) (1%) = 5ppm/°C change in output voltage drift. The worst-case error in initial output voltage for the LT1019 is 0.2%, so a series resistor is satisfactory if the output is simply trimmed to nominal value. 1ppm/°C TC shift would be the maximum expected.

Using the Temp Pin

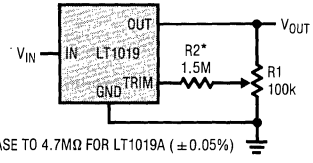
The LT1019 has a TEMP pin like several other bandgap references. The voltage on this pin is directly proportional to absolute temperature (PTAT) with a slope of ≈2.1mV/°C. Room temperature voltage is therefore ≈(295°K) (2.1mV/°C) = 620mV. Previous bandgap references have been very sensitive to any loading on the TEMP pin because it is an integral part of the reference "core" itself. The LT1019 "taps" the core at a special point which has much less effect on the reference. The relationship between TEMP pin loading and a change in reference output voltage is less than 0.05%/μA, about 10 times improvement over previous references.

The TEMP pin can be used to sense chip temperature in applications where the chip is forced to constant temperature (see "Heated Mode") or to sense ambient temperature in applications where the temperature difference between chip and ambient is tolerable or can be calibrated out. Typical chip temperature rise over ambient is ≃2°C with no output load and 15V input voltage, but it could be as high as 6°C with a 5mA load and 5V input-output differential. A Centigrade thermometer is shown in the application circuits. This particular configuration has

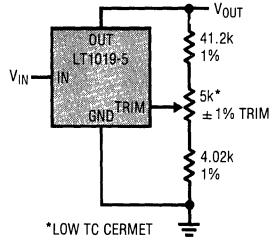
Wide Range Trim ≥ ±5%



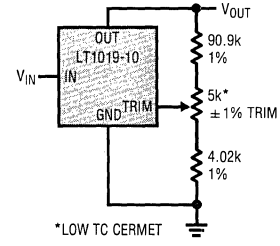
Narrow Trim Range (±0.2%)



Trimming LT1019-5 Output to 5.120V



Trimming LT1019-10 Output to 10.240V



APPLICATIONS INFORMATION

the advantage of trimming "zero" and "slope" simultaneously. The PTAT nature of the TEMP pin output has a known predictable relationship between initial zero error and slope. This circuit takes advantage of that relationship by trimming at a point that corrects the zero and slope errors simultaneously.

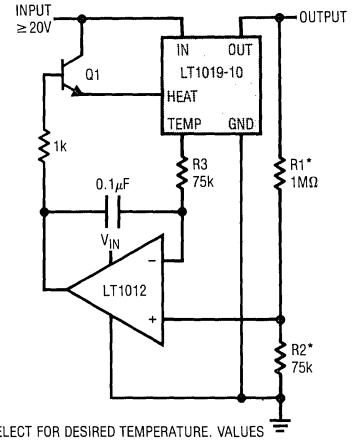
A simple over-temp circuit is also shown in the application section using an LT1011 comparator. This circuit is intended to be an *ambient* sensor, so temperature rise in the reference must be considered when setting trip level. R2B is adjusted by connecting a DVM across the inputs of the comparator and setting the DVM to read 2.1mV for each degree above room temperature. A 70°C trip would require (2.1mV)(70°C – 22°C) = 101mV. R3 provides about 1°C hysteresis to prevent oscillations.

Heated Mode

The LT1019 has an internal heater resistor which can be used to maintain constant chip temperature. The TEMP output is used to sense chip temperature and, in conjunction with an external amplifier, forms a complete thermal control loop. Using the circuit shown in Figure 2, chip temperature is maintained extremely accurately. Residual refrence output voltage shift with ambient temperature changes is less than 2ppm/°C. This small residue is the result of chip temperature gradients and heater current flowing in the ground pin of the reference. Heater power required to maintain a chip temperature of 70°C is about 300mW at 25°C ambient. With a heater resistance of 400Ω nominal, this requires a heater voltage of 11V and heater current of 28mA. Lower ambient temperatures will require proportionately higher power levels.

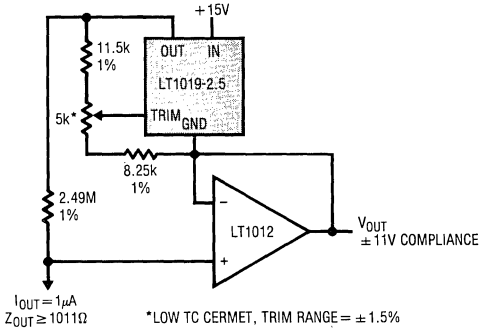
The amplifier used in this application is non-critical. For single supply operation, it must have a common-mode range down to 0.6V. With a negative supply available, this restriction is removed. Higher supply voltages (>15V) may require a small heat sink on Q1.

Heated Mode Reduces Temperature Drift to Less than 2ppm/°C



*SELECT FOR DESIRED TEMPERATURE. VALUES GIVEN SET CHIP TEMPERATURE TO ≃70°C WITH V_{OUT} = 10V.

Precision 1μA Current Source

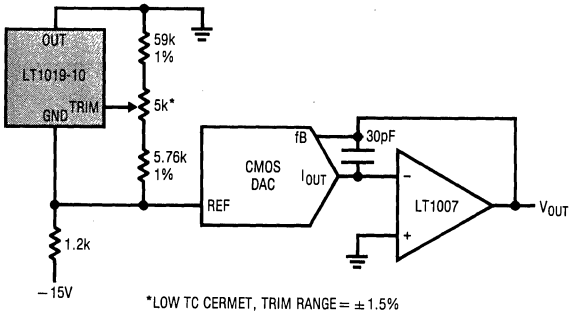


I_{OUT} = 1μA
Z_{OUT} ≥ 1011Ω

*LOW TC CERMET, TRIM RANGE = ±1.5%

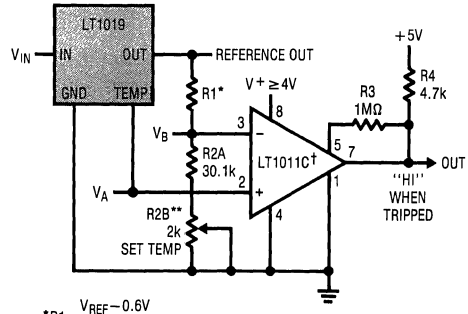
APPLICATIONS INFORMATION

Negative 10V Reference for CMOS DAC



*LOW TC CERMET, TRIM RANGE = ±1.5%

Over Temperature Alarm

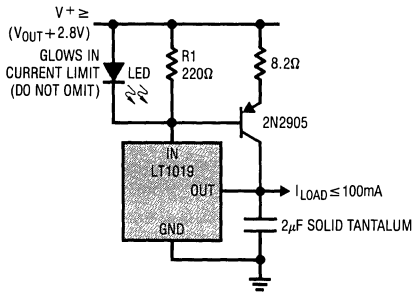


$$*R1 = \frac{V_{REF} - 0.6V}{200\mu A}$$

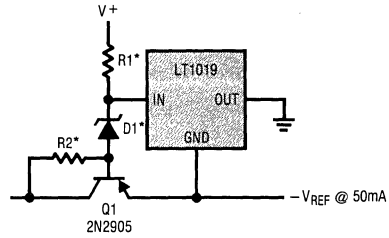
**SET $V_B - V_A = 2.1mV/°C\ (T_{ALARM} - T_{AMBIENT})$

†LM311 MAY BE SUBSTITUTED.

Output Current Boost with Current Limit



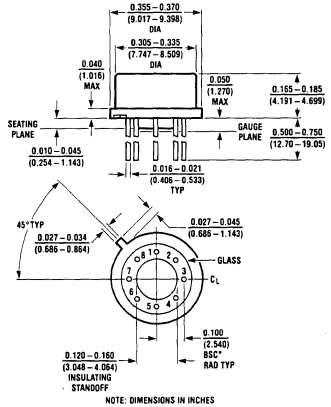
Negative Series Reference



$$*R1 = \frac{V+ - 5V}{2mA},\ R2 = \frac{|V-| - V_{REF}}{1mA},\ D1 = V_{REF} + 5V$$

PACKAGE DESCRIPTION

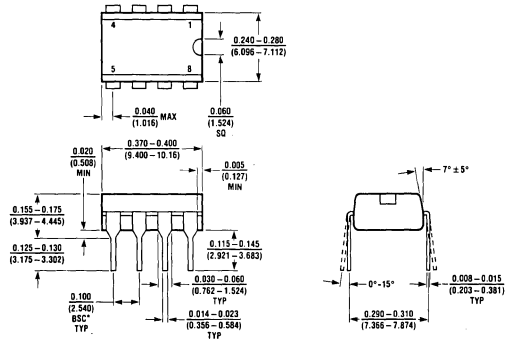
H Package Metal Can



NOTE: DIMENSIONS IN INCHES

T_{jmax}	θ_{JA}	θ_{JC}
150°C	150°C/W	45°C/W

N8 Package 8 Lead Plastic



NOTE: DIMENSIONS IN INCHES UNLESS OTHERWISE NOTED

*LEADS WITHIN 0.007 OF TRUE POSITION (TP) AT GAUGE PLANE

T_{jmax}	θ_{JA}
100°C	130°C/W

FEATURES

- Pin Compatible with Most Bandgap Reference Applications, Including Ref 01, Ref 02, LM368, MC1400, and MC1404, with Greatly Improved Stability, Noise, and Drift
- Ultra Low Drift—5ppm/°C Max Slope
- Trimmed Output Voltage
- Operates in Series or Shunt Mode
- Output Sinks and Sources in Series Mode
- Very Low Noise < 1ppm p-p (0.1Hz to 10Hz)
- > 100dB Ripple Rejection
- Minimum Input-Output Differential of 1V
- 2ppm/°C Max Drift Available on Request
- 100% Noise Tested

APPLICATIONS

- A to D and D to A Converters
- Precision Regulators
- Digital Voltmeters
- Inertial Navigation Systems
- Precision Scales
- Portable Reference Standard

DESCRIPTION

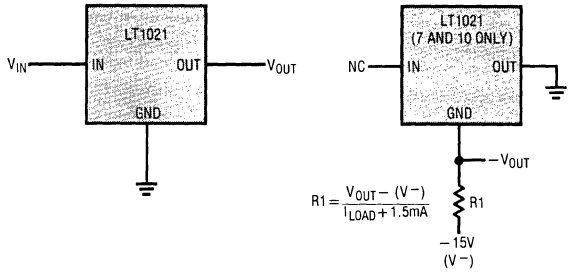
The LT1021 is a precision reference with ultra low drift and noise, extremely good long term stability, and almost total immunity to input voltage variations. The reference output will both source and sink up to 10mA. Three voltages are available; 5V, 7V and 10V. The 7V and 10V units can be used as shunt regulators (two terminal zeners) with the same precision characteristics as the three terminal connection. Special care has been taken to minimize thermal regulation effects and temperature induced hysteresis.

The LT1021 references are based on a buried zener diode structure which eliminates noise and stability problems associated with surface breakdown devices. Further, a subsurface zener exhibits better temperature drift and time stability than even the best band-gap references.

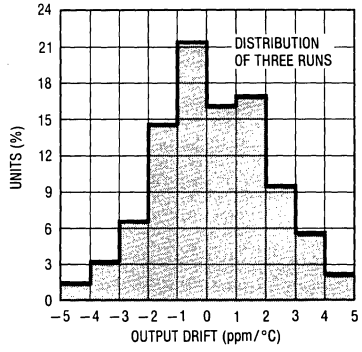
Unique circuit design makes the LT1021 the first IC reference to offer ultra low drift without the use of high power on-chip heaters.

The LT1021-7 uses no resistive divider to set output voltage, and therefore exhibits the best long term stability and temperature hysteresis. The LT1021-5 and LT1021-10 are intended for systems requiring a precise 5V or 10V reference, with an initial tolerance as low as ±0.05%.

Basic Positive and Negative Connections



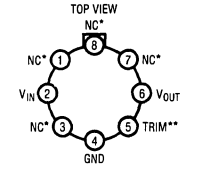
Typical Distribution of Temperature Drift—LT1021



ABSOLUTE MAXIMUM RATINGS

Input Voltage 40V
Input-Output Voltage Differential 35V
Output to Ground Voltage (Shunt Mode Current Limit)
  LT1021-5 ..... 10V
  LT1021-7 ..... 10V
  LT1021-10 ..... 16V
Trim Pin to Ground Voltage
  Positive ..... Equal to V_{OUT}
  Negative ..... −20V
Output Short Circuit Duration
  V_{IN} = 35V ..... 10 sec
  $V_{IN} \leq$ 20V ..... Indefinite
Operating Temperature Range
  LT1021 Mil ..... −55°C to 125°C
  LT1021 Comm ..... 0°C to 70°C
Storage Temperature Range
  All Devices ..... −65°C to 150°C
Lead Temperature (Soldering, 10 sec.) ..... 300°C

PACKAGE/ORDER INFORMATION



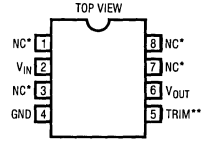
METAL CAN H PACKAGE

*CONNECTED INTERNALLY. DO NOT CONNECT EXTERNAL CIRCUITRY TO THESE PINS.
**NO TRIM PIN ON LT1021-7. DO NOT CONNECT EXTERNAL CIRCUITRY TO PIN 5 ON LT1021-7.

ORDER PART NUMBER

LT1021BMH-5 LT1021BMH-10
LT1021CMH-5 LT1021CMH-10
LT1021DMH-5 LT1021DMH-10
LT1021BCH-5 LT1021BCH-10
LT1021CCH-5 LT1021CCH-10
LT1021DCH-5 LT1021DCH-10

LT1021BMH-7
LT1021DMH-7
LT1021BCH-7
LT1021DCH-7



PLASTIC DIP N8 PACKAGE

*CONNECTED INTERNALLY. DO NOT CONNECT EXTERNAL CIRCUITRY TO THESE PINS.
**NO TRIM PIN ON LT1021-7. DO NOT CONNECT EXTERNAL CIRCUITRY TO PIN 5 ON LT1021-7.

LT1021BCN8-5
LT1021CCN8-5
LT1021DCN8-5

LT1021BCN8-7
LT1021DCN8-7

LT1021BCN8-10
LT1021CCN8-10
LT1021DCN8-10

ELECTRICAL CHARACTERISTICS LT1021-5

V_{IN} = 10V, I_{OUT} = 0, T_A = 25°C, Mil or Comm version, unless otherwise noted

PARAMETER	CONDITIONS		LT1021-5 MIN	LT1021-5 TYP	LT1021-5 MAX	UNITS
Output Voltage (Note 1)	LT1021C-5		4.9975	5.000	5.0025	V
	LT1021B-5, D-5		4.95	5.00	5.05	V
Output Voltage Temperature Coefficient (Note 2)	$T_{MIN} \leq T_J \leq T_{MAX}$ LT1021B-5			2	5	ppm/°C
	LT1021C-5, D-5			3	20	ppm/°C
Line Regulation (Note 3)	7.2V ≤ V_{IN} ≤ 10V			4	12	ppm/V
		•			20	ppm/V
	10V ≤ V_{IN} ≤ 40V			2	6	ppm/V
		•			10	ppm/V
Load Regulation (Sourcing Current)	0 ≤ I_{OUT} ≤ 10mA			10	20	ppm/mA
	(Note 3)	•			35	ppm/mA
Load Regulation (Sinking Current)	0 ≤ I_{OUT} ≤ 10mA			60	100	ppm/mA
	(Note 3)	•			150	ppm/mA
Supply Current				0.8	1.2	mA
		•			1.5	mA
Output Voltage Noise (Note 5)	0.1Hz ≤ f ≤ 10Hz			3		μVp-p
	10Hz ≤ f ≤ 1kHz			2.2	3.5	μVrms
Long Term Stability of Output Voltage (Note 6)	Δt = 1000 Hrs Non-Cumulative			15		ppm
Temperature Hysteresis of Output	ΔT = ±25°C			10		ppm

ELECTRICAL CHARACTERISTICS LT1021-7

V_{IN} = 12V, I_{OUT} = 0, T_A = 25°C, Mil or Comm version, unless otherwise noted

PARAMETER	CONDITIONS		LT1021-7 MIN	LT1021-7 TYP	LT1021-7 MAX	UNITS
Output Voltage (Note 1)			6.95	7.00	7.05	V
Output Voltage Temperature Coefficient (Note 2)	$T_{MIN} \le T_J \le T_{MAX}$ LT1021B-7 LT1021D-7			 2 3	 5 20	 ppm/°C ppm/°C
Line Regulation (Note 3)	8.5V ≤ V_{IN} ≤ 12V 12V ≤ V_{IN} ≤ 40V 	 ● ●		1 2 0.5 1	4 8 2 4	ppm/V ppm/V ppm/V ppm/V
Load Regulation (Sourcing Current)	0 ≤ I_{OUT} ≤ 10mA (Note 3)	 ●		12	25 40	ppm/mA ppm/mA
Load Regulation (Shunt Mode)	1.2mA ≤ I_{SHUNT} ≤ 10mA (Notes 3, 4)	 ●		50	100 150	ppm/mA ppm/mA
Supply Current (Series Mode)		 ●		0.75	1.2 1.5	mA mA
Minimum Current (Shunt Mode)	V_{IN} is Open	 ●		0.7	1.0 1.2	mA mA
Output Voltage Noise (Note 5)	0.1Hz ≤ f ≤ 10Hz 10Hz ≤ f ≤ 1kHz			4 2.5	 4	µVp-p µVrms
Long Term Stability of Output Voltage (Note 6)	Δt = 1000 Hrs Non-Cumulative			7		ppm
Temperature Hysteresis of Output	ΔT = ±25°C			3		ppm

ELECTRICAL CHARACTERISTICS LT1021-10

V_{IN} = 15V, I_{OUT} = 0, T_A = 25°C, Mil or Comm version, unless otherwise noted

PARAMETER	CONDITIONS		LT1021-10 MIN	LT1021-10 TYP	LT1021-10 MAX	UNITS
Output Voltage (Note 1)	LT1021C-10 LT1021B-10, D-10		9.995 9.95	10.00 10.00	10.005 10.05	V V
Output Voltage Temperature Coefficient (Note 2)	$T_{MIN} \le T_J \le T_{MAX}$ LT1021B-10 LT1021C-10, D-10			 2 5	 5 20	 ppm/°C ppm/°C
Line Regulation (Note 3)	11.5V ≤ V_{IN} ≤ 14.5V 14.5V ≤ V_{IN} ≤ 40V 	 ● ●		1 0.5 	4 6 2 4	ppm/V ppm/V ppm/V ppm/V
Load Regulation (Sourcing Current)	0 ≤ I_{OUT} ≤ 10mA (Note 3)	 ●		12	25 40	ppm/mA ppm/mA
Load Regulation (Shunt Mode)	1.7mA ≤ I_{SHUNT} ≤ 10mA (Notes 3, 4)	 ●		50	100 150	ppm/mA ppm/mA
Series Mode Supply Current		 ●		1.2	1.7 2.0	mA mA
Shunt Mode Minimum Current	V_{IN} is Open	 ●		1.1	1.5 1.7	mA mA
Output Voltage Noise (Note 5)	0.1Hz ≤ f ≤ 10Hz 0.1Hz ≤ f ≤ 1kHz			6 3.5	 6	µVp-p µVrms
Long Term Stability of Output Voltage (Note 6)	Δt = 1000 Hrs Non-Cumulative			15		ppm
Temperature Hysteresis of Output	ΔT = ±25°C			5		ppm

The ● denotes the specifications which apply over the full operating temperature range.

Note 1: Output voltage is measured immediately after turn-on. Changes due to chip warm-up are typically less than 0.005%.

Note 2: Temperature coefficient is measured by dividing the change in output voltage over the temperature range by the change in temperature. Separate tests are done for hot and cold; T_{MIN} to 25°C, and 25°C to T_{MAX}. **Incremental slope is also measured at 25°C.**

Note 3: Line and load regulation are measured on a pulse basis. Output changes due to die temperature change must be taken into account separately. Package thermal resistance is 150°C/W for TO-5 (H), and 130°C/W for N.

Note 4: Shunt mode regulation is measured with the input open. With the input connected, shunt mode current can be reduced to 0mA. Load regulation will remain the same.

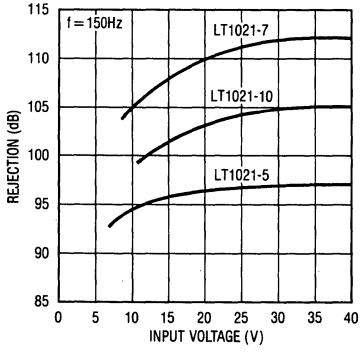
Note 5: RMS noise is measured with a single high pass filter at 10Hz and a 2-pole low pass filter at 1kHz. The resulting output is full wave rectified and then integrated for a fixed period, making the final reading an average as opposed to RMS. A correction factor of 1.1 is used to convert from average to RMS, and a second correction of 0.88 is used to correct for the non-ideal bandpass of the filters.

Peak-to-peak noise is measured with a single high pass filter at 0.1Hz and a 2-pole low pass filter at 10Hz. The unit is enclosed in a still-air environment to eliminate thermocouple effects on the leads. Test time is 10 seconds.

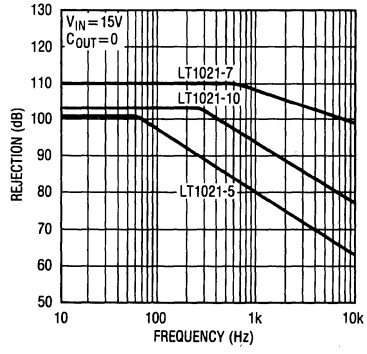
Note 6: Consult factory for units with long term stability data.

TYPICAL PERFORMANCE CHARACTERISTICS

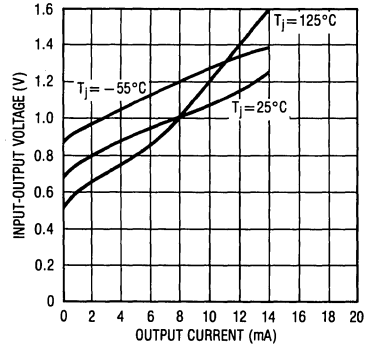
Ripple Rejection



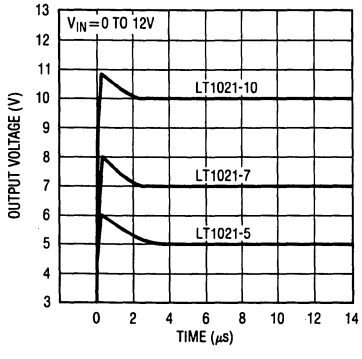
Ripple Rejection



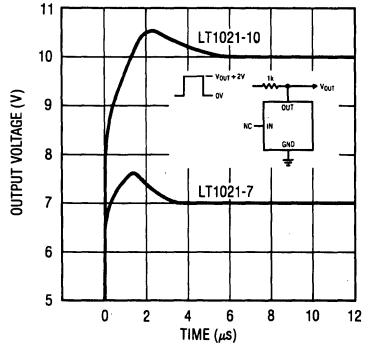
Minimum Input-Output Differential LT1021-7 and LT1021-10



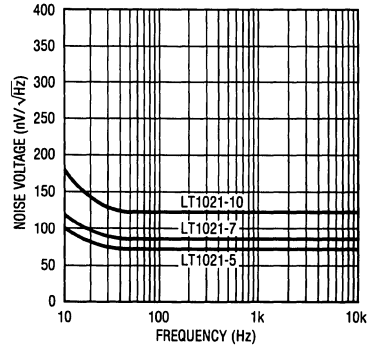
Start-Up (Series Mode)



Start-Up (Shunt Mode) LT1021-7 and LT1021-10

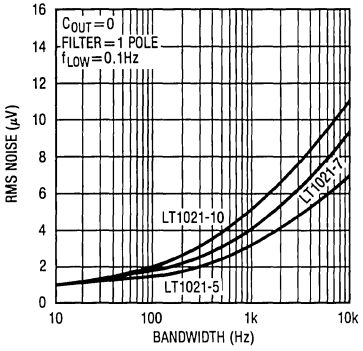


Output Voltage Noise Spectrum

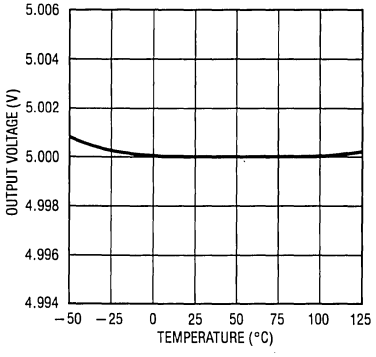


TYPICAL PERFORMANCE CHARACTERISTICS

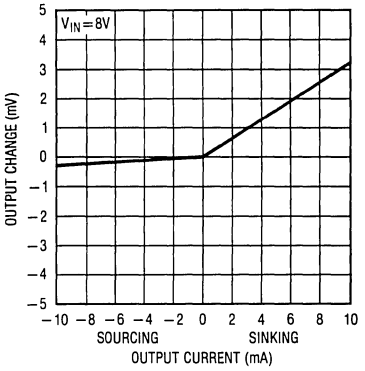
Output Voltage Noise



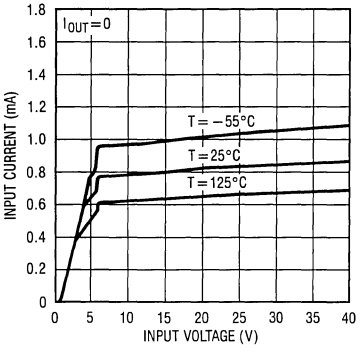
Output Voltage Temperature Drift LT1021-5



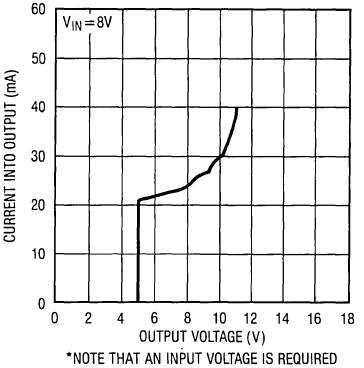
Load Regulation LT1021-5



Quiescent Current LT1021-5

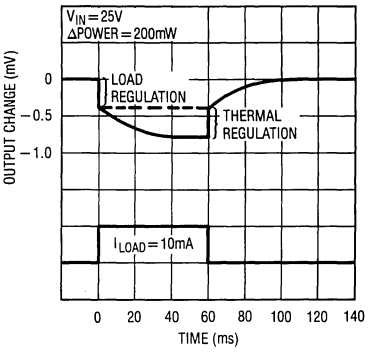


Sink Mode* Current Limit LT1021-5

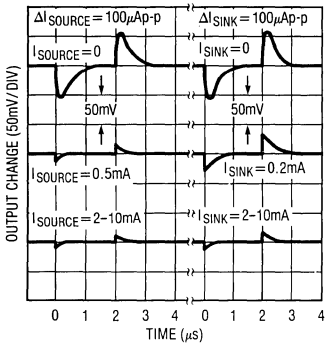


*NOTE THAT AN INPUT VOLTAGE IS REQUIRED FOR 5V UNITS.

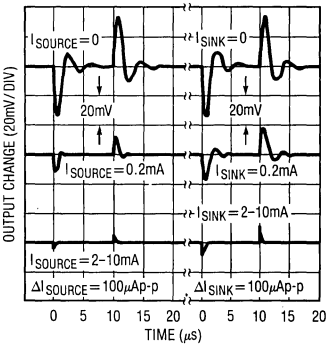
Thermal Regulation LT1021-5



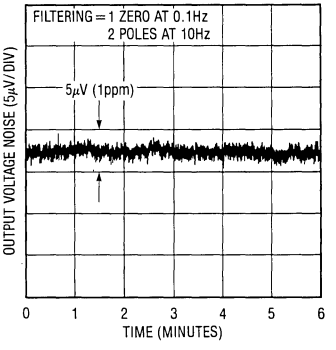
Load Transient Response LT1021-5, C_{LOAD} = 0



Load Transient Response LT1021-5, C_{LOAD} = 1000pF

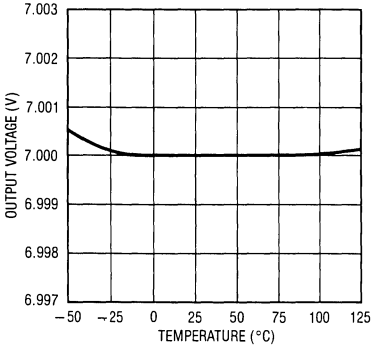


Output Noise 0.1Hz to 10Hz LT1021-5

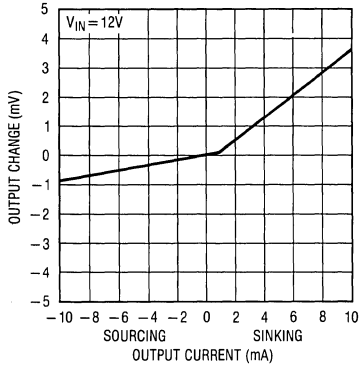


TYPICAL PERFORMANCE CHARACTERISTICS

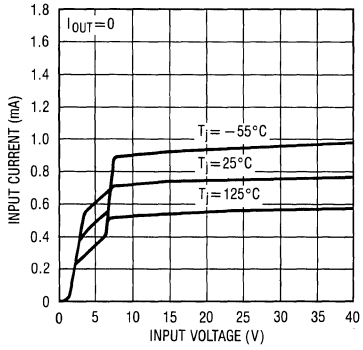
Output Voltage Temperature Drift LT1021-7



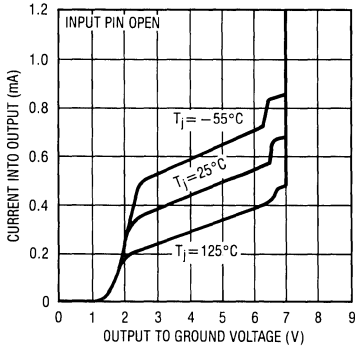
Load Regulation LT1021-7, 10



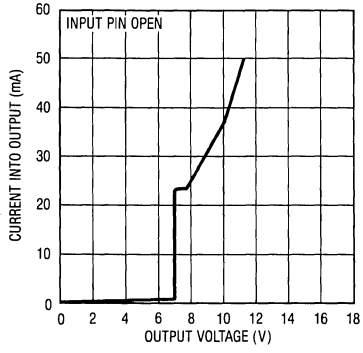
Quiescent Current LT1021-7



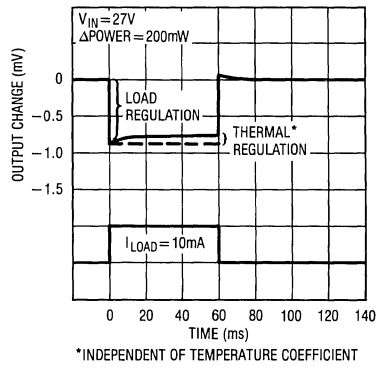
Shunt Characteristics LT1021-7



Shunt Mode Current Limit LT1021-7

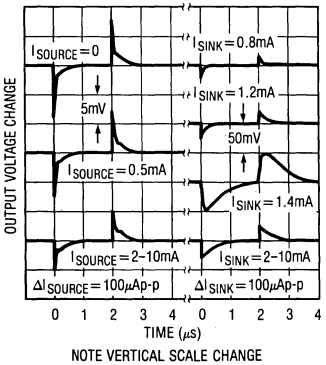


Thermal Regulation LT1021-7



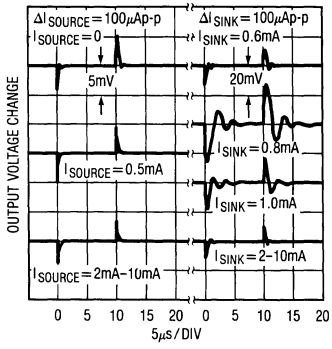
*INDEPENDENT OF TEMPERATURE COEFFICIENT

Load Transient Response LT1021-7, C_{LOAD} = 0



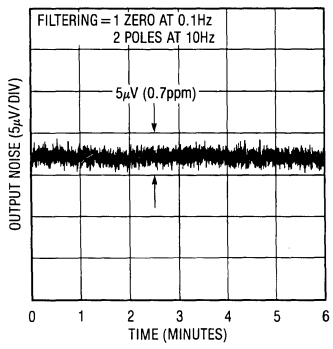
NOTE VERTICAL SCALE CHANGE BETWEEN SOURCING AND SINKING

Load Transient Response LT1021-7, C_{LOAD} = 1000pF



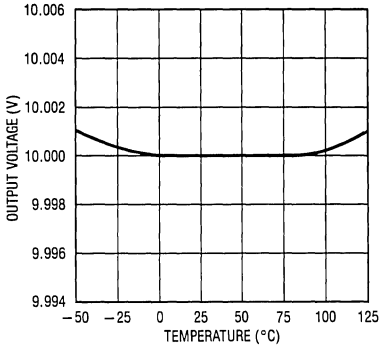
NOTE VERTICAL SCALE CHANGE BETWEEN SOURCING AND SINKING

Output Noise 0.1Hz to 10Hz LT1021-7

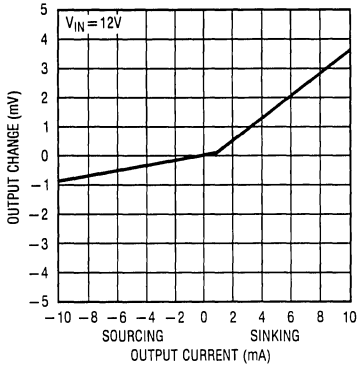


TYPICAL PERFORMANCE CHARACTERISTICS

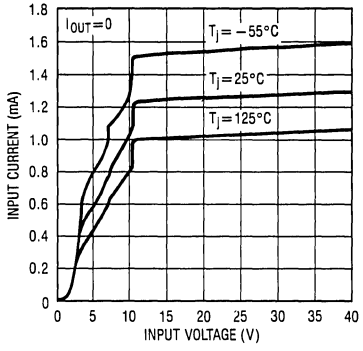
Output Voltage Temperature Drift LT1021-10



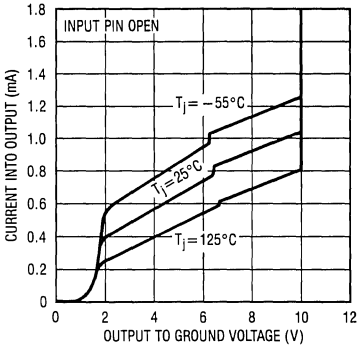
Load Regulation LT1021-7, 10



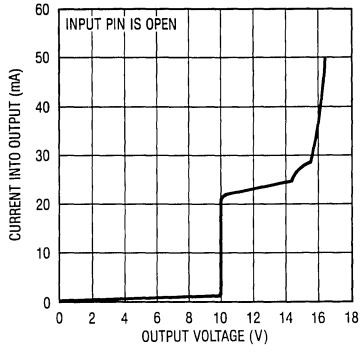
Input Supply Current LT1021-10



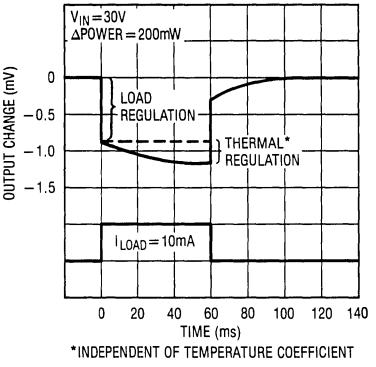
Shunt Characteristics LT1021-10



Shunt Mode Current Limit LT1021-10

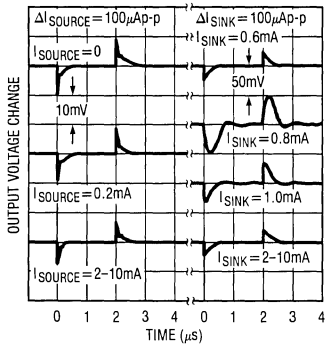


Thermal Regulation LT1021-10



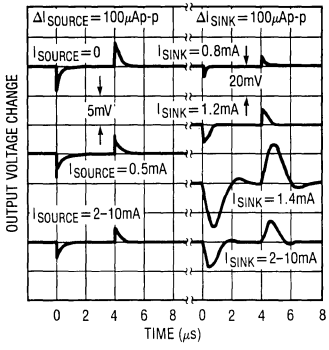
*INDEPENDENT OF TEMPERATURE COEFFICIENT

Load Transient Response LT1021-10, C_{LOAD} = 0



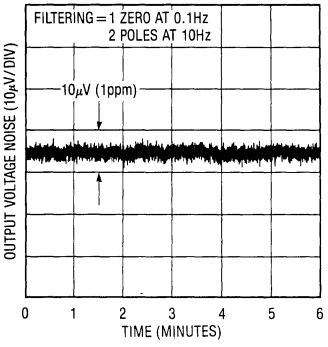
NOTE VERTICAL SCALE CHANGE BETWEEN SOURCING AND SINKING

Load Transient Response LT1021-10, C_{LOAD} = 1000pF



NOTE VERTICAL SCALE CHANGE BETWEEN SOURCING AND SINKING

Output Noise 0.1Hz to 10Hz LT1021-10

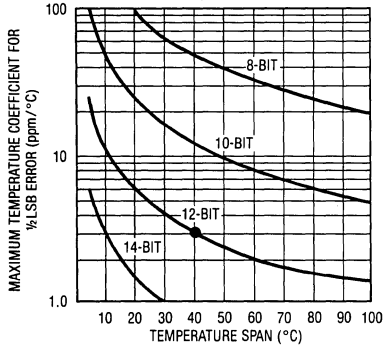


APPLICATIONS INFORMATION

Effect of Reference Drift on System Accuracy

A large portion of the temperature drift error budget in many systems is the system reference voltage. This graph indicates the maximum temperature coefficient allowable if the reference is to contribute no more than ½LSB error to the overall system performance. The example shown is a 12-bit system designed to operate over a temperature range from 25°C to 65°C. Assuming the system calibration is performed at 25°C, the temperature span is 40°C. It can be seen from the graph that the temperature coefficient of the reference must be no worse than 3ppm/°C if it is to contribute less than ½LSB error. For this reason, the LT1021 family has been optimized for low drift.

Maximum Allowable Reference Drift



Trimming Output Voltage

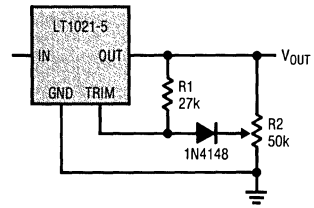
LT1021-10

The LT1021-10 has a trim pin for adjusting output voltage. The impedance of the trim pin is about 12kΩ with a nominal open circuit voltage of 5V. It is designed to be driven from a source impedance of 3kΩ or less to minimize changes in the LT1021 TC with output trimming. Attenuation between the trim pin and the output is 70:1. This allows ±70mV trim range when the trim pin is tied to the wiper of a potentiometer connected between the output and ground. A 10kΩ potentiometer is recommended, preferably a 20 turn cermet type with stable characteristics over time and temperature.

The LT1021-10 "C" version is pre-trimmed to ±5mV and therefore can utilize a restricted trim range. A 75kΩ resistor in series with a 20kΩ potentiometer will give ±10mV trim range. Effect on output TC will be only 1ppm/°C for the ±5mV trim needed to set the "C" device to 10.000V.

LT1021-5

The LT1021-5 does have an output voltage trim pin, but the TC of the nominal 4V open circuit voltage at this pin is about −1.7mV/°C. For the voltage trimming not to affect reference output TC, the external trim voltage must track the voltage on the trim pin. Input impedance of the trim pin is about 100kΩ and attenuation to the output is 13:1. The technique shown below is suggested for trimming the output of the LT1021-5 while maintaining minimum shift in output temperature coefficient. The R1/R2 ratio is chosen to minimize interaction of trimming and TC shifts, so the exact values shown should be used.

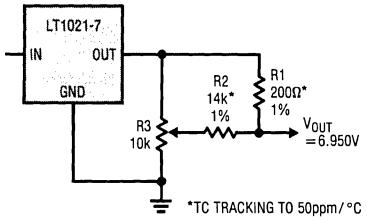


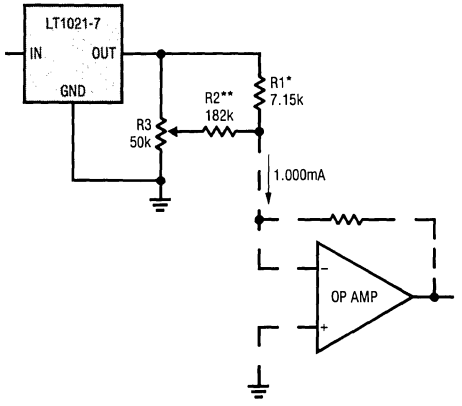
LT1021-7

The 7V version of the LT1021 has no trim pin because the internal architecture does not have a point which could be driven conveniently from the output. Trimming must therefore be done externally, as is the case with ordinary reference diodes. Unlike these diodes, however, the output of the LT1021 can be loaded with a trim potentiometer. The following trim techniques are suggested; one for voltage output, and one for current output. The voltage output is trimmed for 6.95V. Current output is 1mA, as shown, into a summing junction, but all resistors may be scaled for currents up to 10mA.

APPLICATIONS INFORMATION

Both of these circuits use the trimmers in a true potentiometric mode to reduce the effects of trimmer TC. The voltage output has a 200Ω impedance, so loading must be minimized. In the current output circuit, R1 determines output current. It should have a TC commensurate with the LT1021 or track closely with the feedback resistor around the op amp.





Capacitive Loading and Transient Response

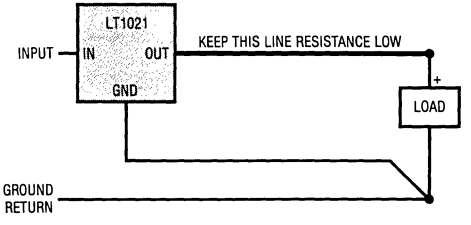
The LT1021 is stable with all capacitive loads, but for optimum settling with load transients, output capacitance should be under 1000pF. The output stage of the reference is class AB with a fairly low idling current. This makes transient response worst-case at light load currents. Because of internal current drain on the output, actual worst-case occurs at $I_{LOAD} = 0$ on LT1021-5, $I_{LOAD} = -0.8$mA (sinking) on LT1021-7, and $I_{LOAD} = 1.4$mA (sinking) on LT1021-10. Significantly better load transient response is obtained by moving slightly away from these points. See Load Transient Response curves for details. In general, best transient response is obtained when the output is sourcing current. In critical applications, a 10μF solid tantalum capacitor with several ohms in series provides optimum output bypass.

Kelvin Connections

Although the LT1021 does not have true force/sense capability at its outputs, significant improvements in ground loop and line loss problems can be achieved with proper hook-up. In series mode operation, the ground pin of the LT1021 carries only ≈1mA and can be used as a sense line, greatly reducing ground loop and loss problems on the low side of the reference. The high side supplies load current so line resistance must be kept low. Twelve feet of #22 gauge hook up wire or 1 foot of 0.025 inch printed circuit trace will create 2mV loss at 10mA output current. This is equivalent to 1LSB in a 10V, 12-bit system.

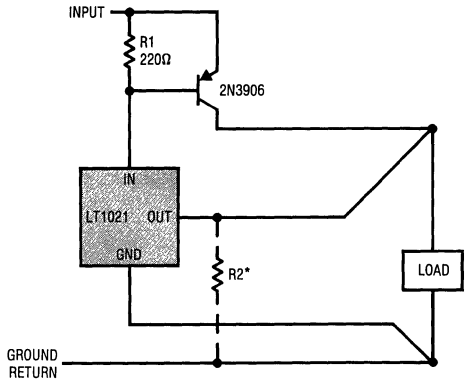
The circuits below show proper hook up to minimize errors due to ground loops and line losses. Losses in the output lead can be greatly reduced by adding a PNP boost transistor if load currents are 5mA or higher. R2 can be added to further reduce current in the output sense lead.

Standard Series Mode



APPLICATIONS INFORMATION

Series Mode with Boost Transistor



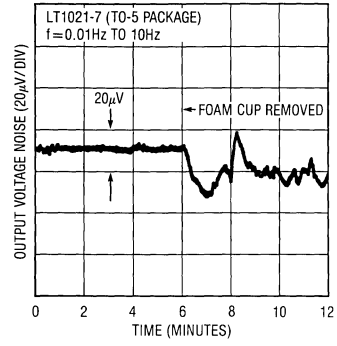
*OPTIONAL—REDUCES CURRENT IN OUTPUT SENSE LEAD
R2 = 2.4k (LT1021-5), 3k (LT1021-7), 5.6k (LT1021-10)

Effects of Air Movement on Low Frequency Noise

The LT1021 has very low noise because of the buried zener used in its design. In the 0.1Hz to 10Hz band, peak-to-peak noise is about 0.5ppm of the DC output. To achieve this low noise, however, care must be taken to shield the reference from ambient air turbulence. Air movement can create noise because of thermoelectric differences between IC package leads (especially kovar lead TO-5) and printed circuit board materials and/or sockets. Power dissipation in the reference, even though it rarely exceeds 20mW, is enough to cause small temperature gradients in the package leads. Variations in thermal resistance, caused by uneven air flow, create differential lead temperatures, thereby causing thermoelectric voltage noise at the output of the reference. The XY plotter trace shown below dramatically illustrates this effect. The first half of the plot was done with the LT1021 shielded from ambient air with a small foam cup. The cup was then removed for the second half of the trace. Ambient in both cases was a lab environment with no excessive air turbulence from air conditioners, opening/closing doors, etc. Removing the foam cup increases the output noise by almost an order of magnitude in the 0.01Hz to 1Hz band! The kovar leads of the TO-5 (H) package are the primary culprit. Alloy 42 and copper lead frames used on dual-in-line packages are not nearly as sensitive to thermally generated noise because they are intrinsically matched.

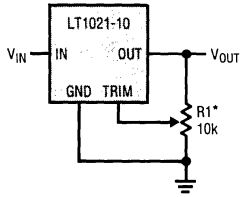
There is nothing magical about foam cups—any enclosure which blocks air flow from the reference will do. Smaller enclosures are better since they do not allow the build-up of internally generated air movement. Naturally, heat generating components external to the reference itself should not be included inside the enclosure.

Noise Induced by Air Turbulence (TO-5 Package)



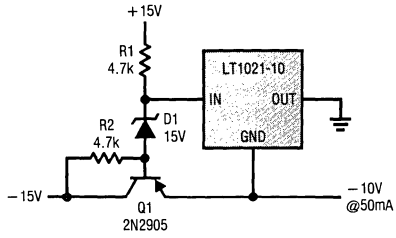
APPLICATION CIRCUITS

LT1021-10 Full Trim Range (±0.7%)

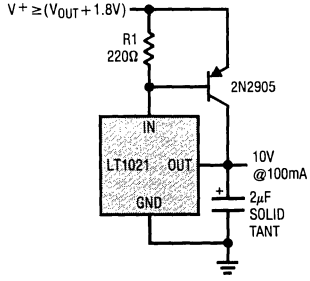


*CAN BE RAISED TO 20kΩ FOR LESS CRITICAL APPLICATIONS

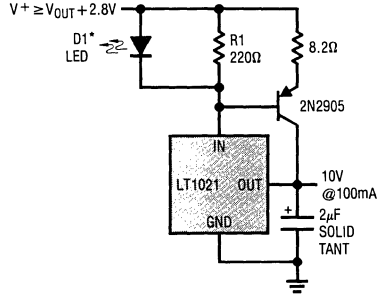
Negative Series Reference



Boosted Output Current With No Current Limit



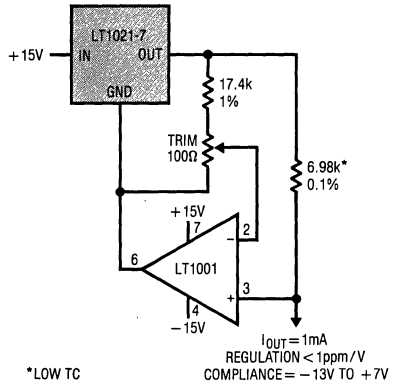
Boosted Output Current With Current Limit



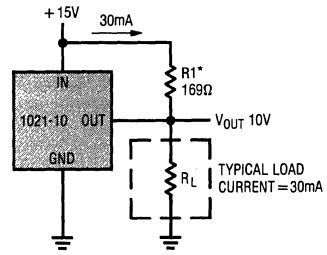
*GLOWS IN CURRENT LIMIT. DO NOT OMIT.

APPLICATION CIRCUITS

Ultra Precise Current Source

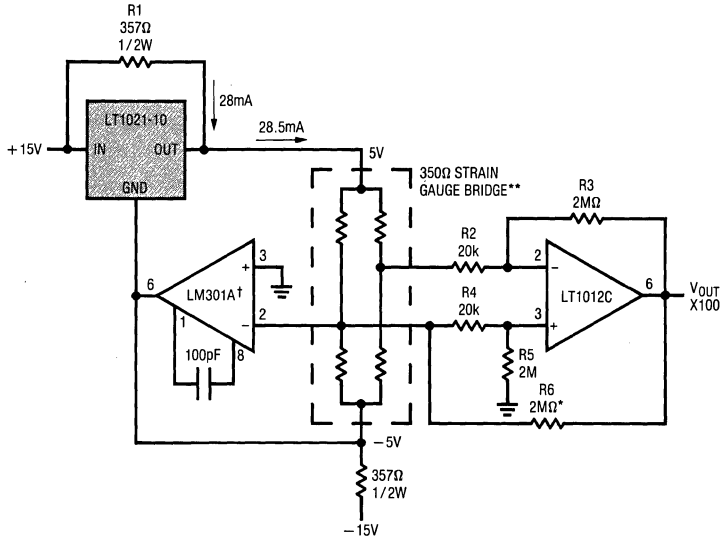


Handling Higher Load Currents



*SELECT R1 TO DELIVER TYPICAL LOAD CURRENT. LT1021 WILL THEN SOURCE OR SINK AS NECESSARY TO MAINTAIN PROPER OUTPUT. DO NOT REMOVE LOAD AS OUTPUT WILL BE DRIVEN UNREGULATED HIGH. LINE REGULATION IS DEGRADED IN THIS APPLICATION.

Strain Gauge Conditioner for 350Ω Bridge



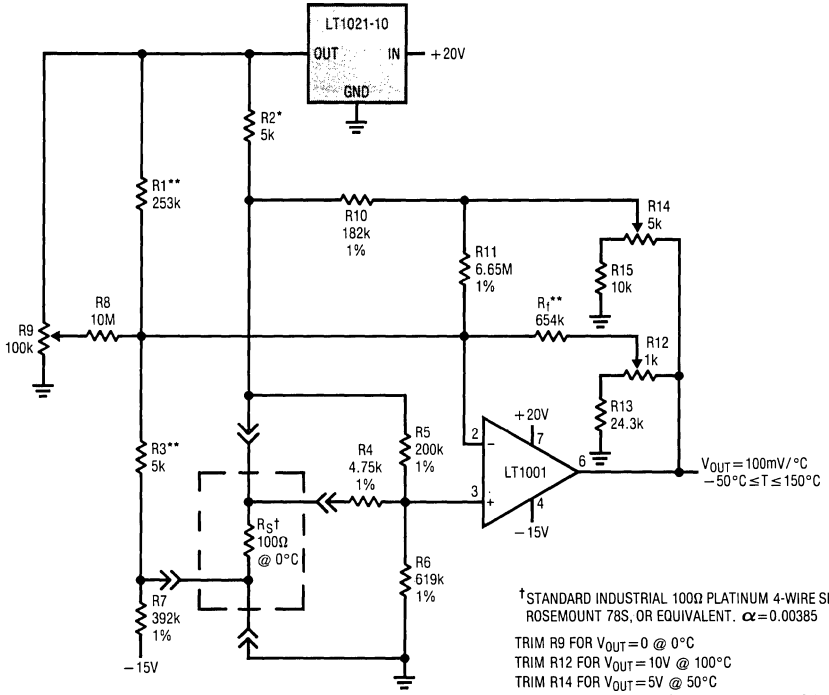
*THIS RESISTOR PROVIDES POSITIVE FEEDBACK TO THE BRIDGE TO ELIMINATE LOADING EFFECT OF THE AMPLIFIER. EFFECTIVE Z_{IN} OF AMPLIFIER STAGE IS ≥ 1MΩ. IF R2–R5 ARE CHANGED, SET R6 = R3.

**BRIDGE IS ULTRA LINEAR WHEN ALL LEGS ARE ACTIVE, TWO IN COMPRESSION AND TWO IN TENSION, OR WHEN ONE SIDE IS ACTIVE WITH ONE COMPRESSED AND ONE TENSIONED LEG.

†OFFSET AND DRIFT OF LM301A ARE VIRTUALLY ELIMINATED BY DIFFERENTIAL CONNECTION OF LT1012C.

APPLICATION CIRCUITS

Ultra Linear Platinum Temperature Sensor*

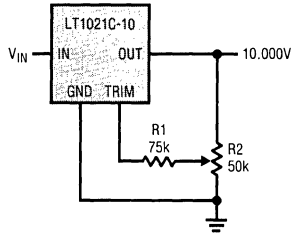


†STANDARD INDUSTRIAL 100Ω PLATINUM 4-WIRE SENSOR, ROSEMOUNT 78S, OR EQUIVALENT. $\alpha = 0.00385$

TRIM R9 FOR $V_{OUT} = 0$ @ 0°C
TRIM R12 FOR $V_{OUT} = 10V$ @ 100°C
TRIM R14 FOR $V_{OUT} = 5V$ @ 50°C
USE TRIM SEQUENCE AS SHOWN. TRIMS ARE NON-INTERACTIVE SO THAT ONLY ONE TRIM SEQUENCE IS NORMALLY REQUIRED.

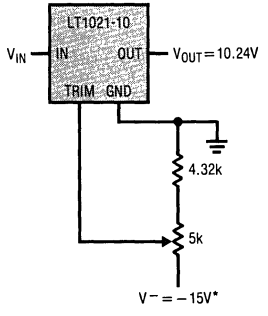
*FEEDBACK LINEARIZES OUTPUT TO ±0.005°C FROM −50°C TO +150°C
**WIREWOUND RESISTORS WITH LOW TC

Restricted Trim Range for Improved Resolution, 10V, "C" Version Only



TRIM RANGE ≈ ±10mV

Trimming 10V Units to 10.24V

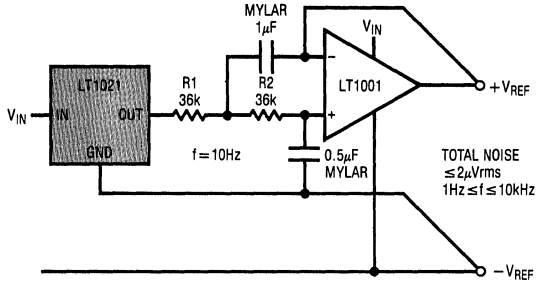


*MUST BE WELL REGULATED

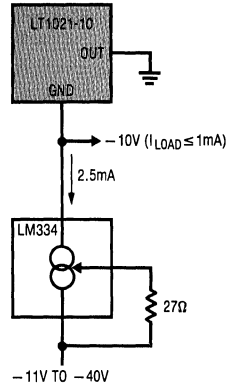
$$\frac{dV_{OUT}}{dV^-} = \frac{15mV}{V}$$

APPLICATION CIRCUITS

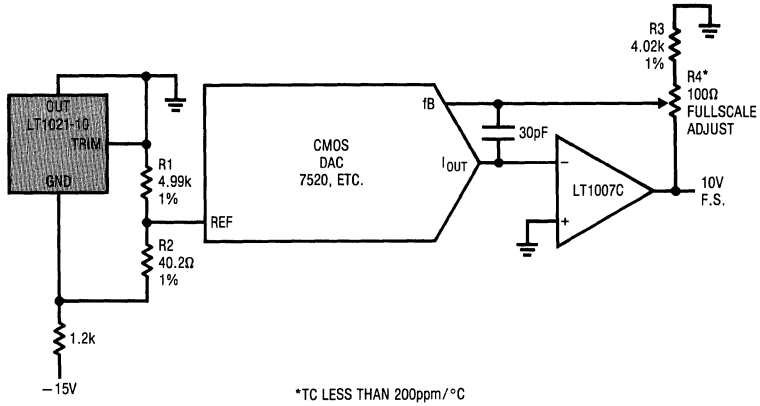
2-Pole Low Pass Filtered Reference



Negative Shunt Reference Driven by Current Source



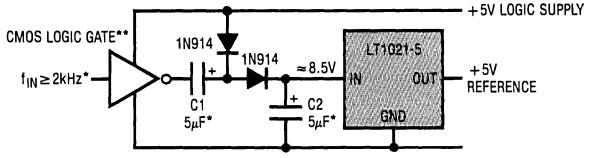
CMOS DAC with Low-Drift Full Scale Trimming**



*TC LESS THAN 200ppm/°C
**NO ZERO ADJUST REQUIRED
WITH LT1007 (V_{OS} ≤ 60μV)

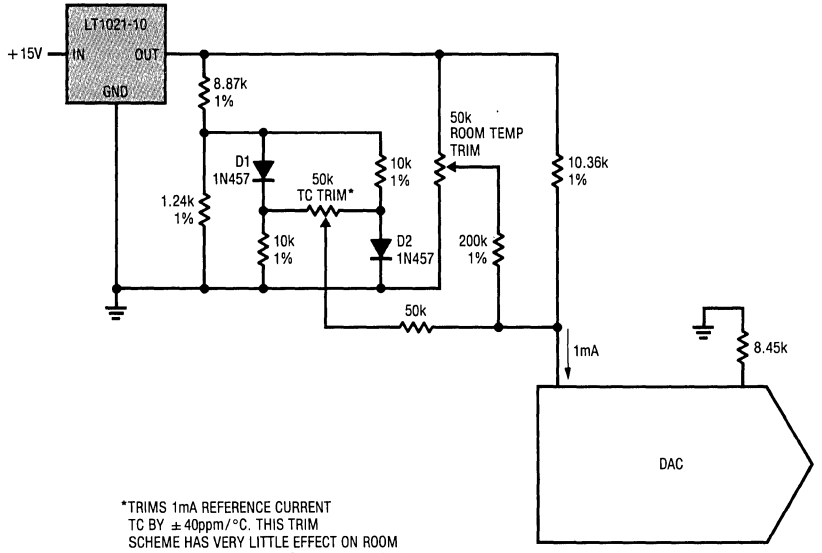
APPLICATION CIRCUITS

Operating 5V Reference from 5V Supply



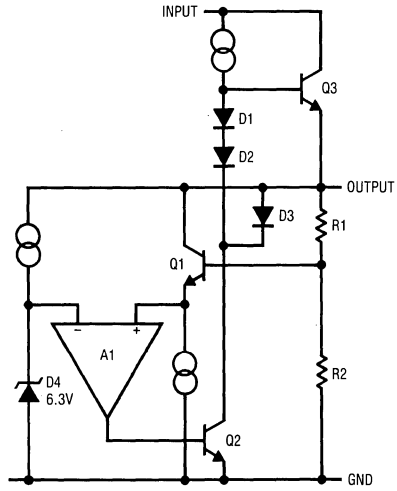
*FOR HIGHER FREQUENCIES C1 AND C2 MAY BE DECREASED.
**PARALLEL GATES FOR HIGHER REFERENCE CURRENT LOADING.

Precision DAC Reference with System TC Trim



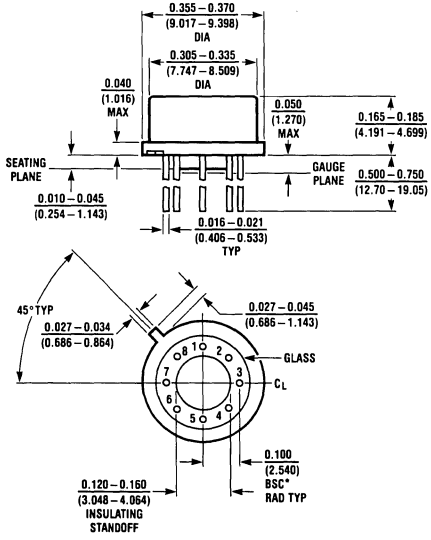
*TRIMS 1mA REFERENCE CURRENT TC BY ±40ppm/°C. THIS TRIM SCHEME HAS VERY LITTLE EFFECT ON ROOM TEMPERATURE CURRENT TO MINIMIZE ITERATIVE TRIMMING.

EQUIVALENT SCHEMATIC



PACKAGE DESCRIPTION

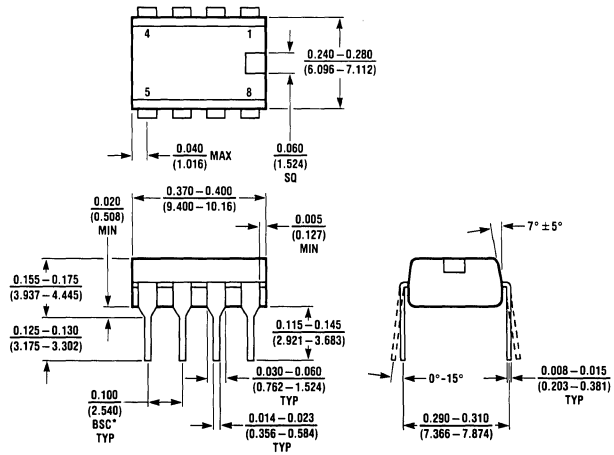
H Package
Metal Can



NOTE: DIMENSIONS IN INCHES (MILLIMETERS)

$T_j$max	θ_{ja}	θ_{jc}
150°C	150°C/W	45°C/W

N8 Package
8 Lead Plastic



NOTE: DIMENSIONS IN INCHES UNLESS OTHERWISE NOTED
*LEADS WITHIN 0.007 OF TRUE POSITION (TP) AT GAUGE PLANE

$T_j$max	θ_{ja}
100°C	130°C/W

5V Bandgap Reference

FEATURES

- 0.2% Output Tolerance
- 0.5Ω Shunt Impedance
- 600μA to 10mA Operating Current
- Pin Compatible with LM136-5
- 20ppm/°C Max. Drift
- Output Voltage Trim does not Affect Drift
- Can be Used as Positive or Negative Reference

APPLICATIONS

- A-to-D and D-to-A Converters
- Precision Regulators
- Precision Current Sources
- V to F and F to V Converters

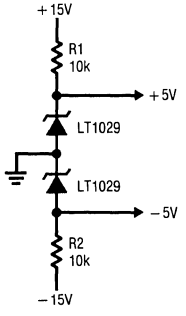
DESCRIPTION

The LT1029 is a 5V bandgap reference intended for use in the shunt or "zener" mode, allowing it to be used as either a positive or negative reference. The output is pretrimmed to ±0.2% accuracy with 20ppm/°C maximum temperature drift. A trim pin allows additional output adjustment for even more precise output voltage.

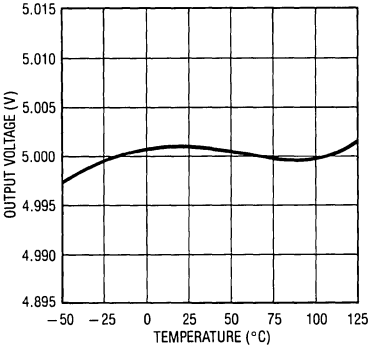
Operating current range for the LT1029 is 600μA to 10mA. Extremely low dynamic impedance allows excellent output regulation even with fluctuating operating current.

The LT1029 will replace an LM136-5 or LM336-5 and simplify circuits using the "minimum temperature coefficient" trim network. The LT1029 does not require this special network to meet its temperature drift specification and these application network components are simply removed. If output trimming is required for initial accuracy, the diodes in the trim network should be replaced with jumpers.

TYPICAL APPLICATION



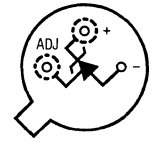
Output Voltage Drift



ABSOLUTE MAXIMUM RATINGS

Reverse Current 15mA
Forward Current 10mA
Operating Temperature Range
LT1029M/LT1029AM ..... −55°C to +125°C
LT1029C/LT1029AC ..... 0°C to +70°C
Storage Temperature ..... −65°C to +150°C
Lead Temperature (Soldering, 10 sec.) ..... 300°C

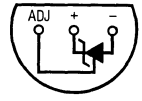
PACKAGE/ORDER INFORMATION



H PACKAGE
TO-46 METAL CAN
BOTTOM VIEW

ORDER PART NUMBER

LT1029AMH
LT1029MH
LT1029ACH
LT1029CH



Z PACKAGE
TO-92 PLASTIC
BOTTOM VIEW

LT1029ACZ
LT1029CZ

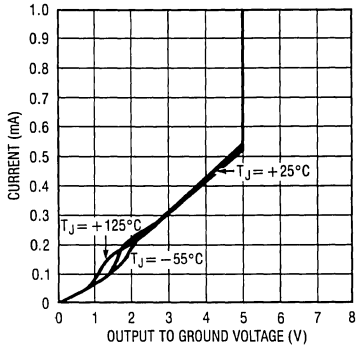
ELECTRICAL CHARACTERISTICS

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Reverse Breakdown Voltage	$I_R = 1mA$ LT1029AM, LT1029AC		4.99	5.00	5.01	V
	LT1029M, LT1029C		4.95	5.00	5.05	V
Reverse Breakdown Change with Current	$600\mu A \le I_R \le 10mA$			2	5	mV
		●		3	8	mV
Reverse Dynamic Impedance	$I_R = 1mA$			0.2	0.6	Ω
		●		0.3	1.0	Ω
Temperature Stability	$I_R = 1mA$ LT1029AC	●		3	7	mV
	LT1029C	●		5	12	mV
	LT1029AM	●		7	18	mV
	LT1029M	●		10	36	mV
Equivalent Temperature Drift	LT1029AM, LT1029AC	●		8	20	ppm/°C
	LT1029C	●		12	34	ppm/°C
	LT1029M	●		15	40	ppm/°C
Long Term Stability				20		ppm/kHr
Trim Range			±3	+5, −13		%

The ● denotes the specifications which apply over the full operating temperature range.

TYPICAL PERFORMANCE CHARACTERISTICS

Reverse Characteristics

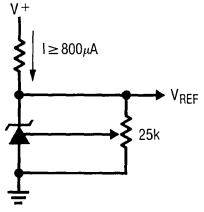


APPLICATIONS INFORMATION

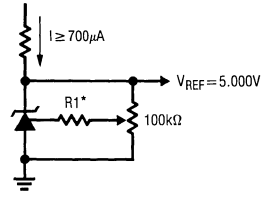
Output Trimming

Output voltage trimming on the LT1029 is nominally accomplished with a potentiometer connected from output to ground with the wiper tied to the trim pin. The LT1029 was made compatible with existing references, so the trim range is large; +5%, –13%. This large trim range makes precision trimming rather difficult. One solution is to insert resistors in series with both ends of the potentiometer. This has the disadvantage of potentially poor tracking between the fixed resistors and the potentiometer. A second method of reducing trim range is to insert a resistor in series with the wiper of the potentiometer. This works well only for a very small trim range because of the mismatch in TCs between the series resistor and the internal thin film resistors. These film resistors can have a TC as high as 500ppm/°C. That same TC is then transferred to the change in output voltage; a 1% shift in output voltage causes a (500ppm) (1%) = 5ppm/°C change in output voltage drift. The worst-case error in initial output voltage for the LT1029A is 0.2% and for the LT1029 is 1%, so a series resistor is satisfactory if the output is simply trimmed to nominal value. 1ppm/°C TC shift would be the maximum expected for the LT1029A and 5ppm/°C for the LT1029.

Wide Trim Range (+5%, –13%)



Narrow Trim Range



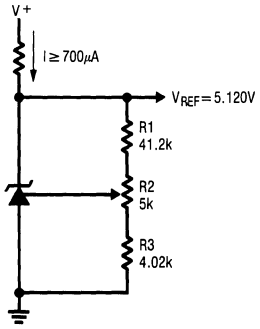
TRIM RANGE
0.4% – LT1029A, R1 = 750k
1.2% – LT1029, R1 = 250k

APPLICATIONS INFORMATION

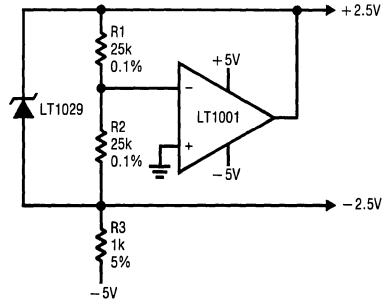
Shunt Capacitance

The LT1029 is stable with all values of shunt capacitance, but values between 300pF and 0.01μF are not recommended because they cause longer settling following a transient in operating current. A 1μF solid tantalum capacitor is suggested for most situations where bypassing is desirable.

Trimming Output to 5.120V

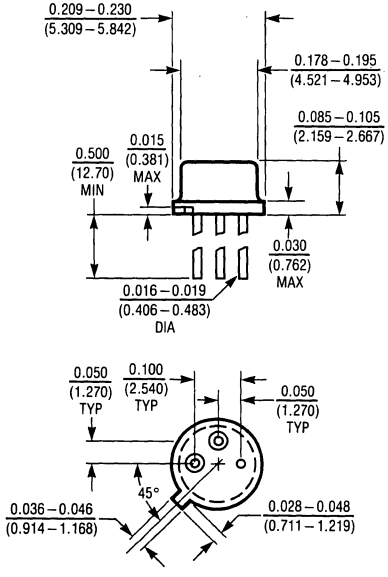


Split ±2.5V References



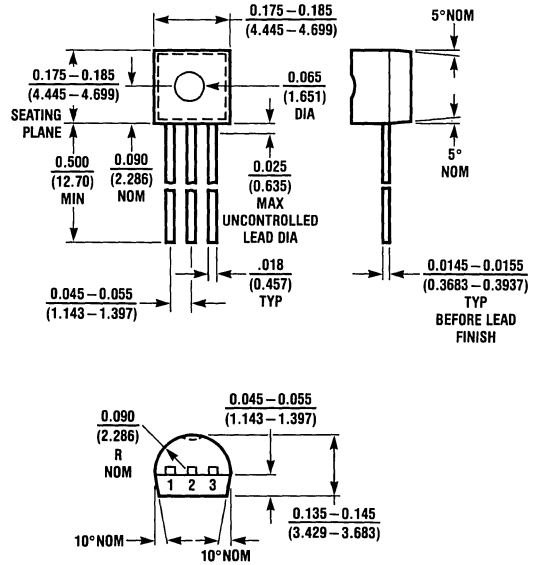
PACKAGE DESCRIPTION Dimensions in inches (millimeters) unless otherwise noted.

H Package
TO-46 Metal Can



T_{jmax}	θ_{jA}	θ_{jC}
150°C	440°C/W	80°C/W

Z Package
TO-92 Plastic



T_{jmax}	θ_{jA}
100°C	160°C/W

Precision 10 Volt Reference

FEATURES

- Pin Compatible with LH0070 and AD581*
- Ultra Low Drift—5ppm/°C Max Slope
- Trimmed Output Voltage
- Operates in Series or Shunt Mode
- Output Sinks and Sources in Series Mode
- Very Low Noise < 1ppm p-p 0.1Hz to 10Hz
- > 100dB Ripple Rejection
- Minimum Input Voltage of 11V

APPLICATIONS

- A to D and D to A Converters
- Precision Regulators
- Digital Voltmeters
- Inertial Navigation Systems
- Precision Scales
- Portable Reference Standard

*See LH0070 Electrical Characteristics table and AD581 cross reference guide.

DESCRIPTION

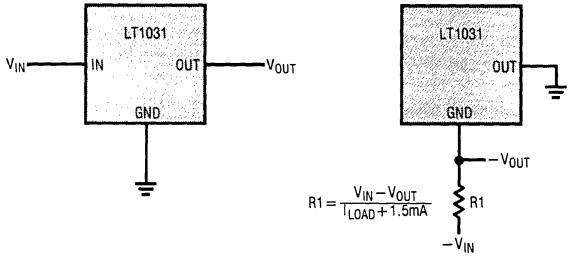
The LT1031 is a precision 10V reference with ultra low drift and noise, extremely good long term stability, and almost total immunity to input voltage variations. The reference output will both source and sink up to 10mA and can be used as a shunt regulator (two terminal zener) with the same precision characteristics as the three terminal connection. Special care has been taken to minimize thermal regulation effects and temperature induced hysteresis.

The LT1031 reference is based on a buried zener diode structure which eliminates noise and stability problems associated with surface breakdown devices. Further, a subsurface zener exhibits better temperature drift and time stability than even the best band-gap references.

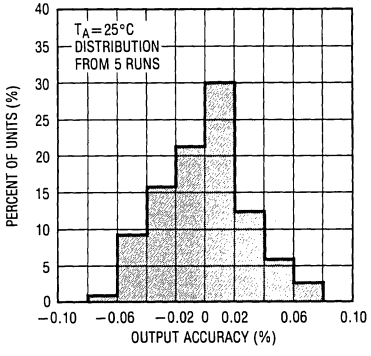
Unique circuit design makes the LT1031 the first three terminal IC reference to offer ultra low drift without the use of high power on-chip heaters. Output voltage is pretrimmed to 0.05% accuracy.

The LT1031 can be used as a plug-in replacement for the AD581 and LH0070*, with improved electrical and thermal performance.

Basic Positive and Negative Connections



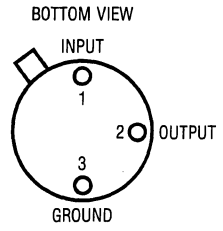
Distribution of Output Accuracy



ABSOLUTE MAXIMUM RATINGS

Input Voltage 40V
Input-Output Voltage Differential 35V
Output to Ground Voltage
(Shunt Mode Current Limit) 16V
Trim Pin to Ground Voltage
Positive ..... Equal to V_{OUT}
Negative ..... −20V
Output Short Circuit Duration
V_{IN} = 35V ..... 10 sec
$V_{IN} \leq$ 20V ..... Indefinite
Operating Temperature Range
LT1031 (Mil) ..... −55°C to 125°C
LT1031 (Comm) ..... 0°C to 70°C
Storage Temperature Range ..... −65°C to 150°C
Lead Temperature (Soldering, 10 sec.) ..... 300°C

PACKAGE/ORDER INFORMATION



H PACKAGE
TO-5 METAL CAN

ORDER PART NUMBER
LH0070-0H
LH0070-1H
LH0070-2H
LT1031BMH
LT1031CMH
LT1031DMH
LT1031BCH
LT1031CCH
LT1031DCH

ELECTRICAL CHARACTERISTICS LT1031

V_{IN} = 15V, I_{OUT} = 0, T_A = 25°C, Mil or Comm version, unless otherwise noted

SYMBOL	PARAMETER	CONDITIONS		LT1031 MIN	LT1031 TYP	LT1031 MAX	UNITS
V_R	Output Voltage (Note 1)	LT1031B LT1031C LT1031D		9.995 9.990 9.980	10.000 10.000 10.000	10.005 10.010 10.020	V V V
$\frac{\Delta V_R}{\Delta T}$	Output Voltage Temperature Coefficient (Note 2)	$T_{MIN} \leq T_J \leq T_{MAX}$ LT1031B LT1031C LT1031D	 ● ● ●		 3 6 10	 5 15 25	 ppm/°C ppm/°C ppm/°C
$\frac{\Delta V_R}{\Delta V_{IN}}$	Line Regulation (Note 3)	11.5V ≤ V_{IN} ≤ 14.5V 14.5V ≤ V_{IN} ≤ 40V	 ● ●		1 0.5	4 6 2 4	ppm/V ppm/V ppm/V ppm/V
$\frac{\Delta V_R}{\Delta I_O}$	Load Regulation (Sourcing Current)	0 ≤ I_{OUT} ≤ 10mA (Note 3)	 ●		12	25 40	ppm/mA ppm/mA
$\frac{\Delta V_R}{\Delta I_O}$	Load Regulation (Shunt Mode)	1.7mA ≤ I_{SHUNT} ≤ 10mA (Notes 3, 4)	 ●		50	100 150	ppm/mA ppm/mA
I_Q	Series Mode Supply Current		 ●		1.2	1.7 2.0	mA mA
I_{MIN}	Shunt Mode Minimum Current	V_{IN} is Open	 ●		1.1	1.5 1.7	mA mA
	Output Short Circuit Current	11V ≤ V_{IN} ≤ 35V			30		mA
	Minimum Input Voltage (Note 6)	$I_{OUT} \leq$ 1mA			10.8	11.0	V
e_n	Output Voltage Noise	0.1Hz ≤ f ≤ 10Hz 0.1Hz ≤ f ≤ 10kHz			6 11		μVp-p μVrms
$\frac{\Delta V_R}{\Delta Time}$	Long Term Stability of Output Voltage	Δt = 1000 Hrs Non-Cumulative			15		ppm
	Temperature Hysteresis of Output	ΔT = 50°C			5		ppm

ELECTRICAL CHARACTERISTICS LH0070

V_{IN} = 15V, R_L = 10kΩ, −55°C ≤ T_A ≤ +125°C unless otherwise noted

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_R	Output Voltage	T_A = 25°C			10.000		V
ΔV_R	Output Accuracy	T_A = 25°C					
	-0, -1				±0.03	±0.1	%
	-2				±0.02	±0.05	%
ΔV_R	Output Accuracy	T_A = −55°C, 125°C					
	-0, −1		●			±0.3	%
	-2					±0.2	%
$\frac{\Delta V_R}{\Delta T}$	Output Voltage Change with Temperature	Note 5					
	-0		●			±0.2	%
	-1		●		±0.02	±0.1	%
	-2		●		±0.01	±0.04	%
$\frac{\Delta V_R}{\Delta V_{IN}}$	Line Regulation	13V ≤ V_{IN} ≤ 33V, T_A = 25°C					
	-0, -1				0.006	0.1	%
	-2				0.006	0.03	%
	Input Voltage Range		●	11.4		40	V
$\frac{\Delta V_R}{\Delta I_O}$	Load Regulation	0mA ≤ I_{OUT} ≤ 5mA	●		0.01	0.03	%
I_Q	Quiescent Current	13V ≤ V_{IN} ≤ 33V	●		1.2	5	mA
$\frac{\Delta I_Q}{\Delta V_{IN}}$	Change in Quiescent Current	ΔV_{IN} = 20V from 13V to 33V	●		0.1	1.5	mA
e_n	Output Noise Voltage				6		μVp-p
	Ripple Rejection	f = 120Hz	●		0.001		%/Vp-p
r_O	Output Resistance		●		0.2	0.6	Ω
$\frac{\Delta V_Z}{\Delta Time}$	Long Term Stability	T_A = 25°C (Note 7)					
	-0, -1					±0.2	%/Yr
	-2					±0.05	%/Yr

The ● denotes the specifications which apply over the full operating temperature range.

Note 1: Output voltage is measured immediately after turn-on. Changes due to chip warm-up are typically less than 0.005%.

Note 2: Temperature coefficient is measured by dividing the change in output voltage over the temperature range by the change in temperature. Separate tests are done for hot and cold; T_{MIN} to 25°C, and 25°C to T_{MAX}. **Incremental slope is also measured at 25°C.** For LT1031BMH, the 5ppm/°C drift specification is for −25°C to 85°C. Drift over the full −55°C to +125°C range is guaranteed to 7ppm/°C.

Note 3: Line and load regulation are measured on a pulse basis. Output changes due to die temperature change must be taken into account separately. Package thermal resistance is 150°C/W.

Note 4: Shunt mode regulation is measured with the input open. With the input connected, shunt mode current can be reduced to 0mA. Load regulation will remain the same.

Note 5: Temperature drift is guaranteed from −25°C to +85°C on LH0070.

Note 6: See curve for guaranteed minimum V_{IN} versus I_{OUT}.

Note 7: Guaranteed by design.

CROSS REFERENCE

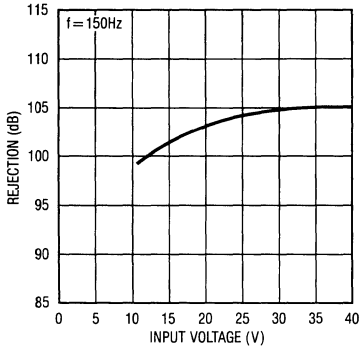
The following cross reference guide may be used to select LT1031 grades which meet or exceed output voltage, temperature drift, load and line regulation, and output current specifications of the AD581 reference. Parameters such as noise, hysteresis, and long term stability will be significantly better for all LT1031 grades compared to the AD581.

Cross Reference Guide—LT1031 to AD581

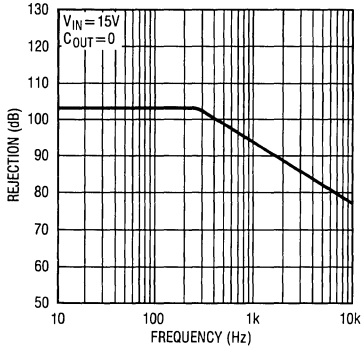
AD581J	order	LT1031DCH
AD581K	order	LT1031CCH
AD581L	order	LT1031BCH
AD581S	order	LT1031DMH
AD581T	order	LT1031CMH
AD581U	order	LT1031BMH

TYPICAL PERFORMANCE CHARACTERISTICS

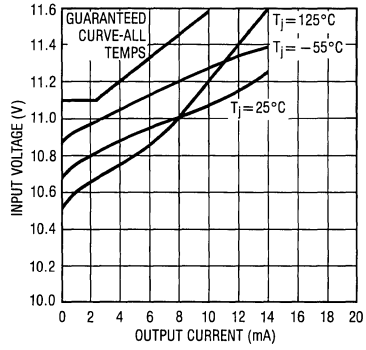
Ripple Rejection



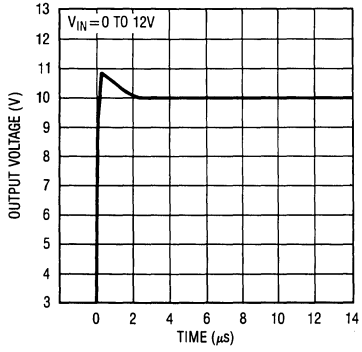
Ripple Rejection



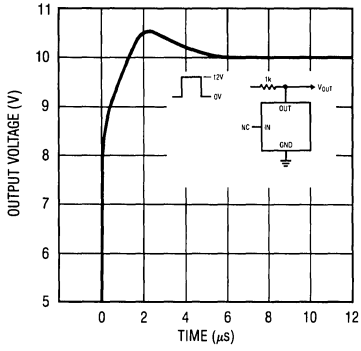
Minimum Input Voltage



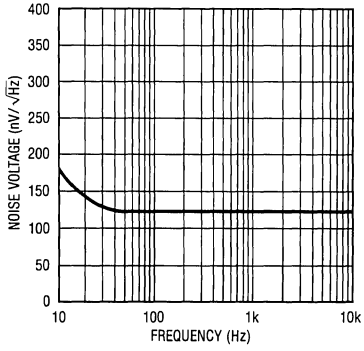
Start-Up (Series Mode)



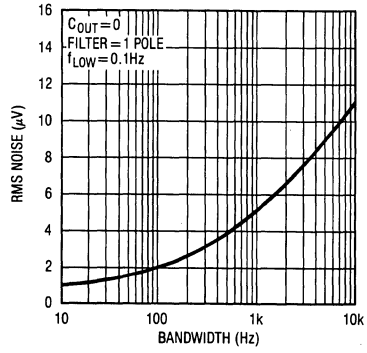
Start-Up (Shunt Mode)



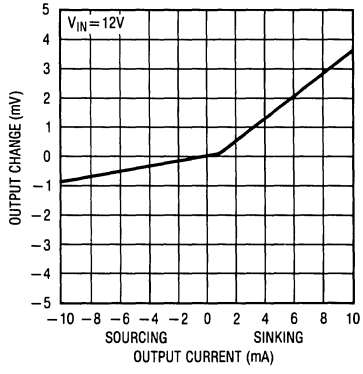
Output Voltage Noise Spectrum



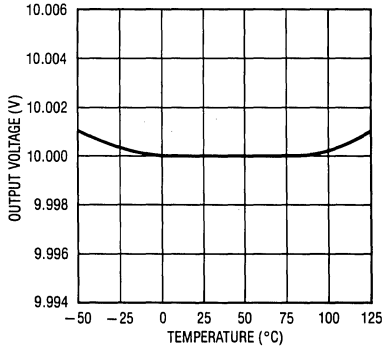
Output Voltage Noise



Load Regulation

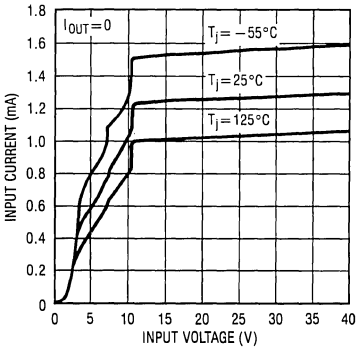


Output Voltage Temperature Drift

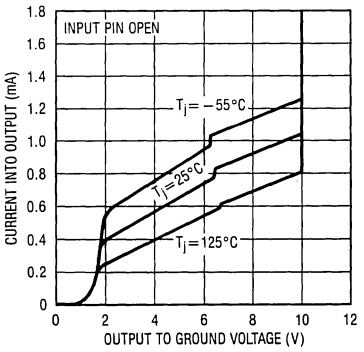


TYPICAL PERFORMANCE CHARACTERISTICS

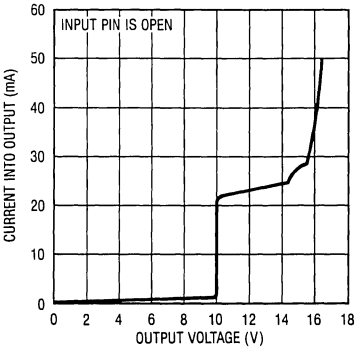
Input Supply Current



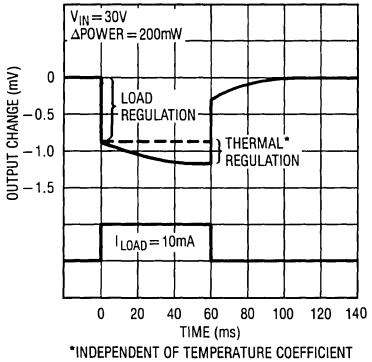
Shunt Characteristics



Shunt Mode Current Limit

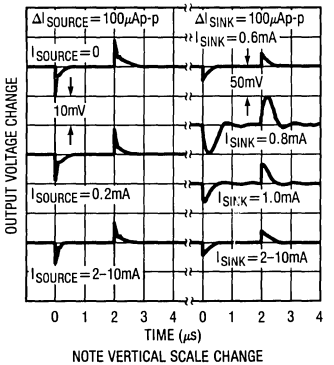


Thermal Regulation



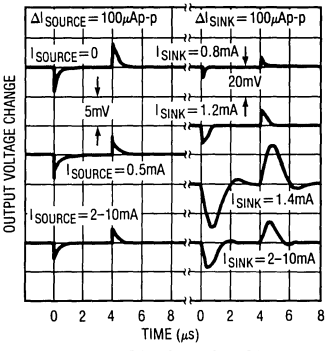
*INDEPENDENT OF TEMPERATURE COEFFICIENT

Load Transient Response $C_{LOAD}=0$



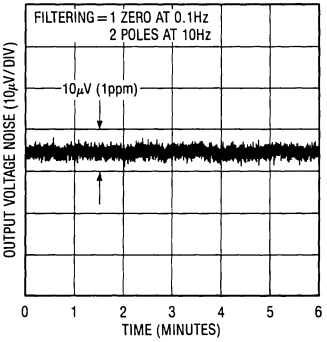
NOTE VERTICAL SCALE CHANGE BETWEEN SOURCING AND SINKING

Load Transient Response $C_{LOAD}=1000pF$



NOTE VERTICAL SCALE CHANGE BETWEEN SOURCING AND SINKING

Output Noise 0.1Hz to 10Hz

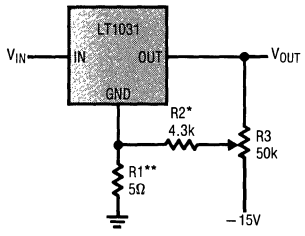


APPLICATIONS INFORMATION

Trimming Output Voltage

The LT1031 output can be trimmed by driving the ground pin. The suggested method is shown in the accompanying figure. A 5Ω resistor is inserted in series with the ground pin and the top of the resistor is supplied current from a trim potentiometer. This technique requires fairly high trim current—up to 1.5mA from the LT1031 or 3.5mA from the −15V supply, but it is necessary to maintain low drift in the reference. Ground pin current changes in the LT1031 (with temperature) could be as high as 4μA/°C. This, coupled with the 5Ω external resistor, creates up to 2ppm/°C drift in the reference (5Ω × 4μA/°C = 20μV/°C = 2ppm/°C). If induced drift higher than this can be tolerated, all resistor values in the trim circuit can be raised proportionately to reduce current drain.

Output Voltage Trimming

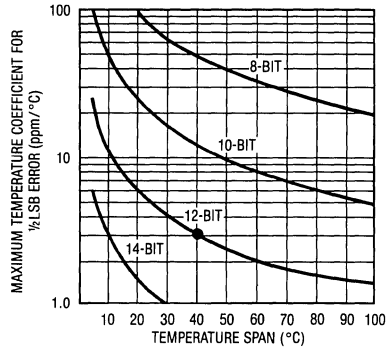


*CAN BE INCREASED TO 5.6k FOR LT1031B AND LH0070-2
**INCREASE TO 10Ω FOR LT1031D

Effect of Reference Drift on System Accuracy

A large portion of the temperature drift error budget in many systems is the system reference voltage. This graph indicates the maximum temperature coefficient allowable if the reference is to contribute no more than ½LSB error to the overall system performance. The example shown is a 12-bit system designed to operate over a temperature range from 25°C to 65°C. Assuming the system calibration is performed at 25°C, the temperature span is 40°C. It can be seen from the graph that the temperature coefficient of the reference must be no worse than 3ppm/°C if it is to contribute less than ½LSB error. For this reason, the LT1031 has been optimized for low drift.

Maximum Allowable Reference Drift



Capacitive Loading and Transient Response

The LT1031 is stable with all capacitive loads, but for optimum settling with load transients, output capacitance should be under 1000pF. The output stage of the reference is class AB with a fairly low idling current. This makes transient response worst-case at light load currents. Because of internal current drain on the output, actual worst-case occurs at $I_{LOAD} = 1.4mA$ (sinking). Significantly better load transient response is obtained by moving slightly away from these points. See Load Transient Response curves for details. In general, best transient response is obtained when the output is sourcing current. In critical applications, a 10μF solid tantalum capacitor with several ohms in series provides optimum output bypass.

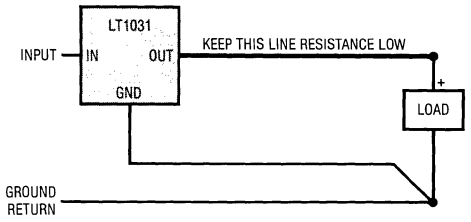
Kelvin Connections

Although the LT1031 does not have true force/sense capability at its outputs, significant improvements in ground loop and line loss problems can be achieved with proper hook-up. In series mode operation, the ground pin of the LT1031 carries only ≈1mA and can be used as a sense line, greatly reducing ground loop and loss problems on the low side of the reference. The high side supplies load current so line resistance must be kept low. Twelve feet of #22 gauge hook up wire or 1 foot of 0.025 inch printed circuit trace will create 2mV loss at 10mA output current. This is equivalent to 1LSB in a 10V, 12-bit system.

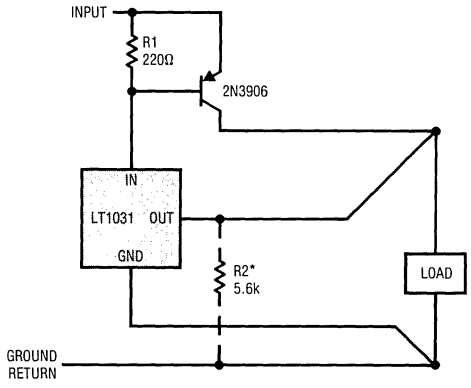
APPLICATIONS INFORMATION

The circuits below show proper hook up to minimize errors due to ground loops and line losses. Losses in the output lead can be greatly reduced by adding a PNP boost transistor if load currents are 5mA or higher. R2 can be added to further reduce current in the output sense lead.

Standard Series Mode



Series Mode with Boost Transistor



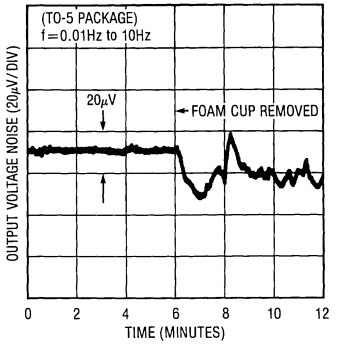
*OPTIONAL—REDUCES CURRENT IN OUTPUT SENSE LEAD

Effects of Air Movement on Low Frequency Noise

The LT1031 has very low noise because of the buried zener used in its design. In the 0.1Hz to 10Hz band, peak-to-peak noise is about 0.5ppm of the DC output. To achieve this low noise, however, care must be taken to shield the reference from ambient air turbulence. Air movement can create noise because of thermoelectric differences between IC package leads (especially kovar lead TO-5) and printed circuit board materials and/or sockets. Power dissipation in the reference, even though it rarely exceeds 20mW, is enough to cause small temperature gradients in the package leads. Variations in thermal resistance, caused by uneven air flow, create differential lead temperatures, thereby causing thermoelectric voltage noise at the output of the reference. The XY plotter trace shown below dramatically illustrates this effect. The first half of the plot was done with the LT1031 shielded from ambient air with a small foam cup. The cup was then removed for the second half of the trace. Ambient in both cases was a lab environment with no excessive air turbulence from air conditioners, opening/closing doors, etc. Removing the foam cup increases the output noise by almost an order of magnitude in the 0.01Hz to 1Hz band! The kovar leads of the TO-5 (H) package are the primary culprit. Alloy 42 and copper lead frames used on dual-in-line packages are not nearly as sensitive to thermally generated noise because they are intrinsically matched.

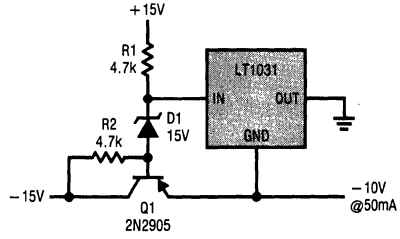
There is nothing magical about foam cups—any enclosure which blocks air flow from the reference will do. Smaller enclosures are better since they do not allow the build-up of internally generated air movement. Naturally, heat generating components external to the reference itself should not be included inside the enclosure.

Noise Induced by Air Turbulence (TO-5 Package)

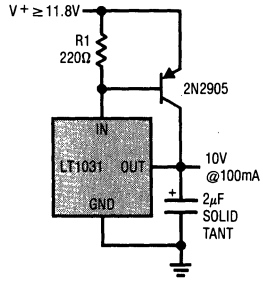


APPLICATION CIRCUITS

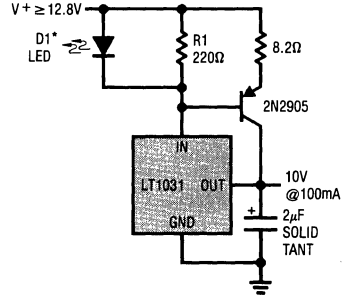
Negative Series Reference



Boosted Output Current With No Current Limit



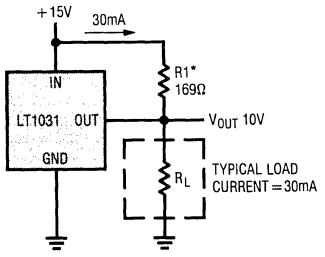
Boosted Output Current With Current Limit



*GLOWS IN CURRENT LIMIT.
DO NOT OMIT.

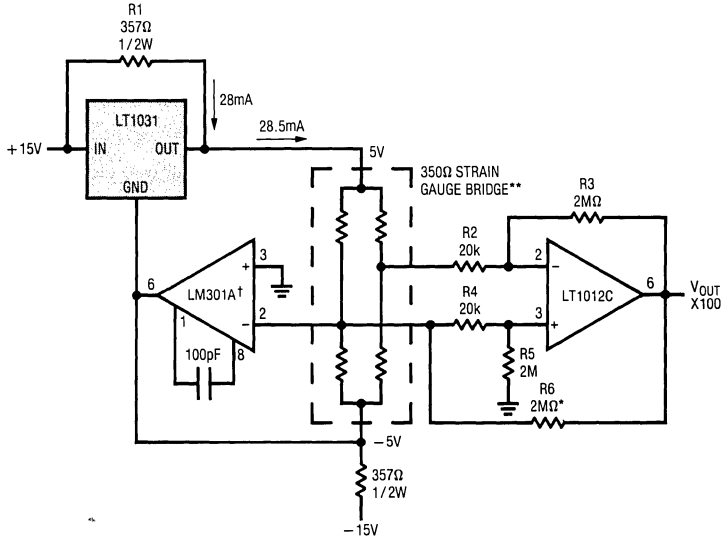
APPLICATION CIRCUITS

Handling Higher Load Currents



*SELECT R1 TO DELIVER TYPICAL LOAD CURRENT. LT1031 WILL THEN SOURCE OR SINK AS NECESSARY TO MAINTAIN PROPER OUTPUT. DO NOT REMOVE LOAD AS OUTPUT WILL BE DRIVEN UNREGULATED HIGH. LINE REGULATION IS DEGRADED IN THIS APPLICATION.

Strain Gauge Conditioner for 350Ω Bridge



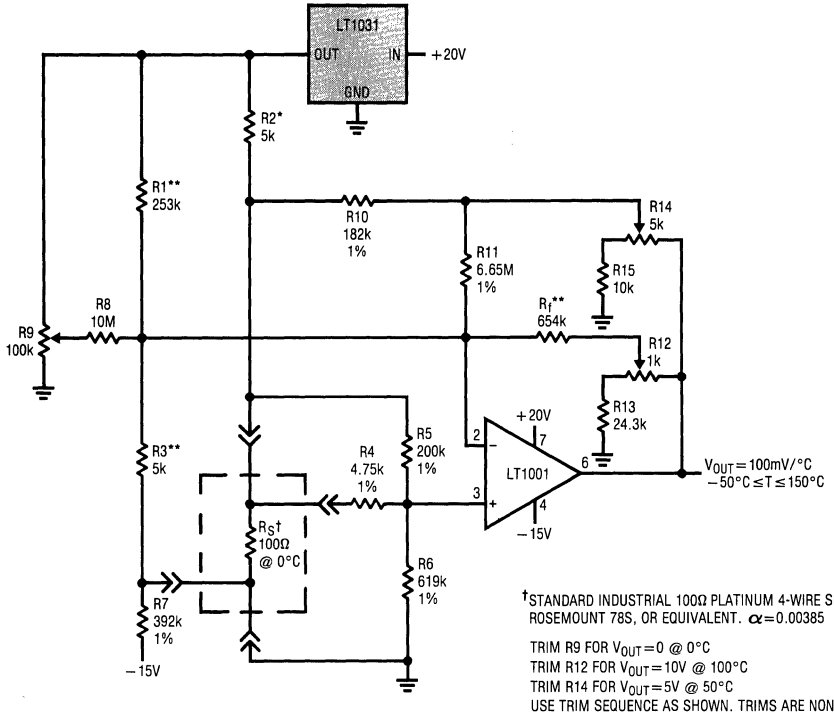
*THIS RESISTOR PROVIDES POSITIVE FEEDBACK TO THE BRIDGE TO ELIMINATE LOADING EFFECT OF THE AMPLIFIER. EFFECTIVE Z_{IN} OF AMPLIFIER STAGE IS ≥ 1MΩ. IF R2-R5 ARE CHANGED, SET R6 = R3.

**BRIDGE IS ULTRA LINEAR WHEN ALL LEGS ARE ACTIVE, TWO IN COMPRESSION AND TWO IN TENSION, OR WHEN ONE SIDE IS ACTIVE WITH ONE COMPRESSED AND ONE TENSIONED LEG.

†OFFSET AND DRIFT OF LM301A ARE VIRTUALLY ELIMINATED BY DIFFERENTIAL CONNECTION OF LT1012C.

APPLICATION CIRCUITS

Ultra Linear Platinum Temperature Sensor*



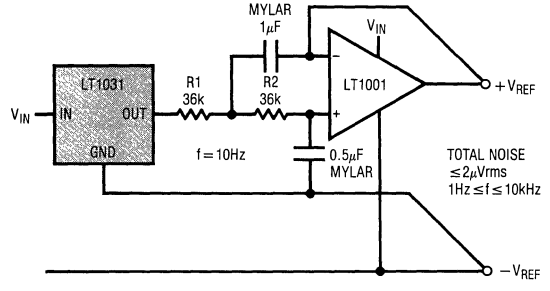
†STANDARD INDUSTRIAL 100Ω PLATINUM 4-WIRE SENSOR, ROSEMOUNT 78S, OR EQUIVALENT. $\alpha = 0.00385$

TRIM R9 FOR $V_{OUT} = 0$ @ 0°C
TRIM R12 FOR $V_{OUT} = 10V$ @ 100°C
TRIM R14 FOR $V_{OUT} = 5V$ @ 50°C
USE TRIM SEQUENCE AS SHOWN. TRIMS ARE NON-INTERACTIVE SO THAT ONLY ONE TRIM SEQUENCE IS NORMALLY REQUIRED.

*FEEDBACK LINEARIZES OUTPUT TO ±0.005°C FROM −50°C TO +150°C

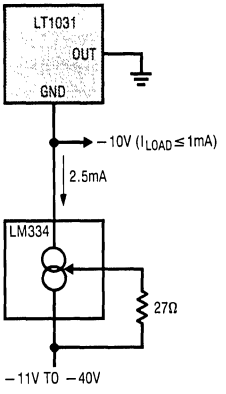
**WIREWOUND RESISTORS WITH LOW TC

2-Pole Low Pass Filtered Reference

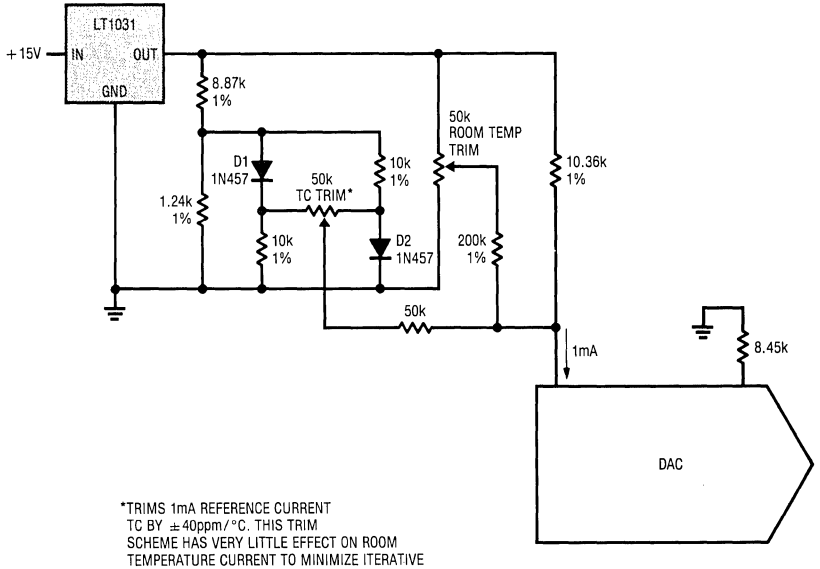


APPLICATION CIRCUITS

Negative Shunt Reference Driven by Current Source

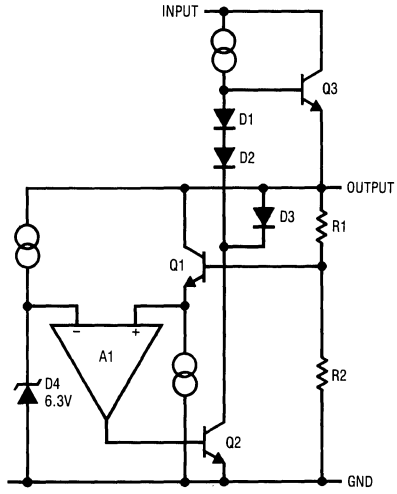


Precision DAC Reference with System TC Trim



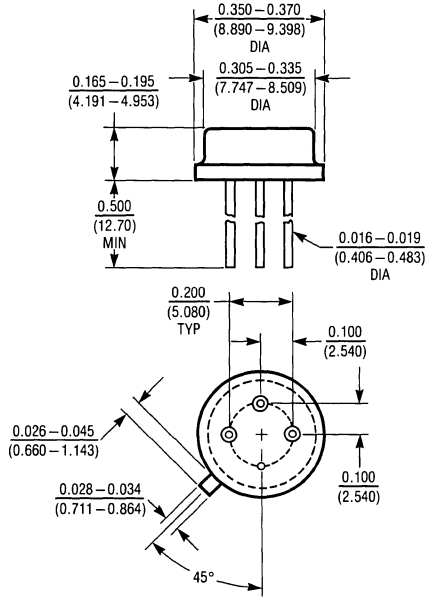
*TRIMS 1mA REFERENCE CURRENT TC BY ±40ppm/°C. THIS TRIM SCHEME HAS VERY LITTLE EFFECT ON ROOM TEMPERATURE CURRENT TO MINIMIZE ITERATIVE TRIMMING.

EQUIVALENT SCHEMATIC



PACKAGE DESCRIPTION

TO-5



T_{jmax}		Θ_{jA}	Θ_{jC}
LH0070	150°C	150°C/W	45°C/W
LT1031M	150°C	150°C/W	45°C/W
LT1031C	85°C	150°C/W	45°C/W

FEATURES

- *Guaranteed* 20 ppm/°C Drift
- 1.2V 1% Initial Tolerance
- 20μA to 20mA Operation
- 1Ω Dynamic Impedance
- 7V, 100μA Reference

APPLICATIONS

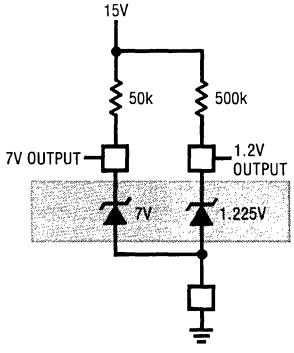
- Portable Meters
- Precision Regulators
- Calibrators

DESCRIPTION

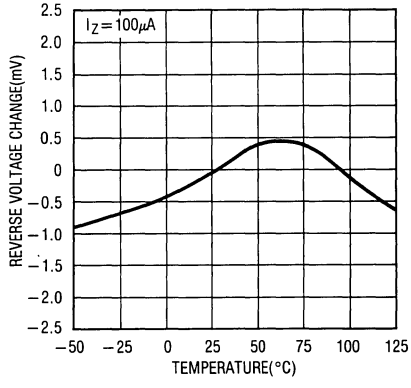
The LT1034 is a micropower, precision 1.2V reference combined with a 7V auxiliary reference. The 1.2V reference is a trimmed, thin-film, band-gap voltage reference with 1% initial tolerance and guaranteed 20ppm/°C temperature drift. Operating on only 20μA, the LT1034 offers guaranteed drift, low temperature cycling hysteresis and good long term stability. The low dynamic impedance makes the LT1034 easy to use from unregulated supplies. The 7V reference is a subsurface zener device for less demanding applications.

The LT1034 1.2V reference can be used as a high performance upgrade of the LM385 or LT1004.

TYPICAL APPLICATION



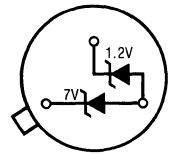
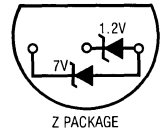
Temperature Drift



ABSOLUTE MAXIMUM RATINGS

Operating Current.....20mA
Forward Current (Note 1).....20mA
Operating Temperature Range
LT1034BM, M..... – 55°C to 125°C
LT1034BC, C.....0°C to 70°C
Storage Temperature..... – 65°C to 150°C
Lead Temperature (Soldering, 10 sec.).....300°C

PACKAGE/ORDER INFORMATION

	ORDER PART NUMBER
 H PACKAGE TO-46 METAL CAN BOTTOM VIEW	LT1034BMH, LT1034MH LT1034BCH, LT1034CH
 Z PACKAGE TO-92 PLASTIC BOTTOM VIEW	LT1034BCZ LT1034CZ

ELECTRICAL CHARACTERISTICS 1.2V Reference

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Reverse Breakdown Voltage	IR = 100μA	25°C	1.210	1.225	1.240	V
		●	1.205	1.225	1.245	V
Reverse Breakdown Change with Current	20μA ≤ IR ≤ 2mA	25°C		.5	2.0	mV
		●		1.0	4.0	mV
	2mA ≤ IR ≤ 20mA	25°C		4	8.0	mV
		●		6.0	15.0	mV
Minimum Operating Current		●		10	20	μA
Temperature Coefficient	IR = 100μA, LT1034BM/BC	●		10	20	ppm/°C
	LT1034M/C			20	40	ppm/°C
Reverse Dynamic Impedance (Note 2)	IR = 100μA	25°C		0.25	1.0	Ω
		●		0.50	2.0	Ω
Low Frequency Noise	IR = 100μA, 0.1Hz ≤ F ≤ 10Hz	●		4		μVp-p
Long Term Stability	IR = 100μA, T = 25°C	25°C		20		ppm

ELECTRICAL CHARACTERISTICS 7V Reference

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Reverse Breakdown Voltage	IR = 100μA	25°C	6.8	7.0	7.3	V
		●	6.75	7.0	7.4	V
Reverse Breakdown Change with Current	100μA ≤ IR ≤ 1mA	25°C		90	140	mV
	100μA ≤ IR ≤ 1mA	●		100	190	mV
	1mA ≤ IR ≤ 20mA	25°C		160	250	mV
	1mA ≤ IR ≤ 20mA	●		200	350	mV
Temperature Coefficient	IR = 100μA	●		40		ppm/°C
Long Term Stability	IR = 100μA	25°C		20		ppm

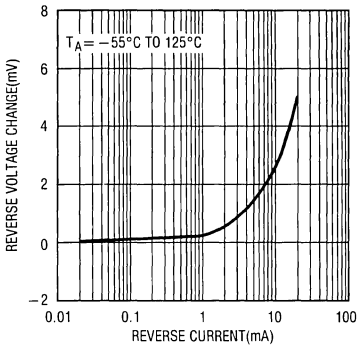
The ● denotes specifications that apply over the operating temperature range.

Note 1: Forward biasing either diode will affect the operation of the other diode.

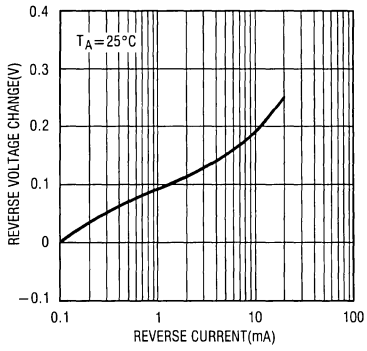
Note 2: This parameter guaranteed by "reverse breakdown change with current" test.

TYPICAL PERFORMANCE CHARACTERISTICS

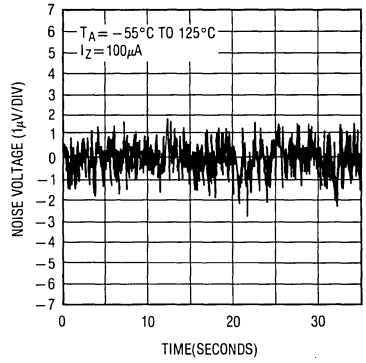
Reverse Voltage Change



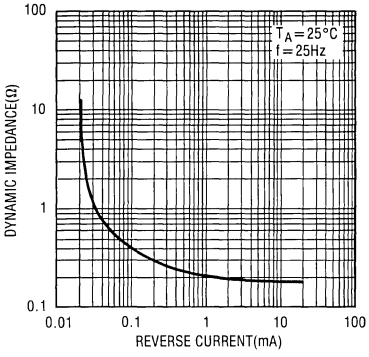
Reverse Voltage Change



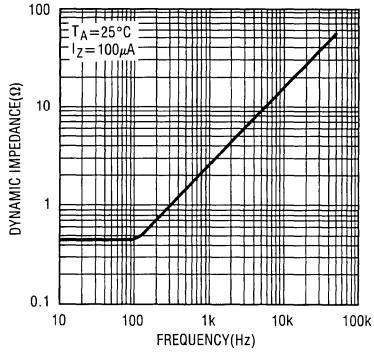
0.1Hz to 10Hz Noise



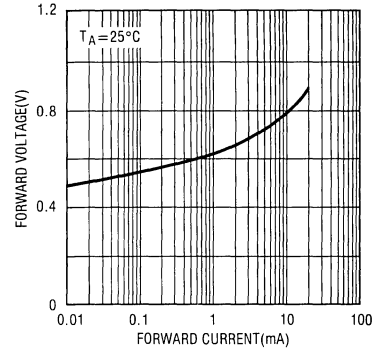
Reverse Dynamic Impedance



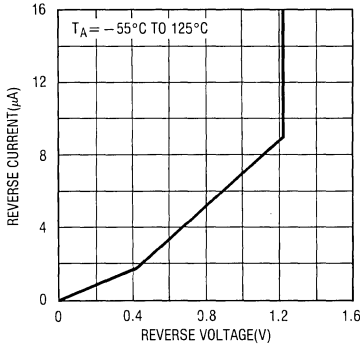
Reverse Dynamic Impedance



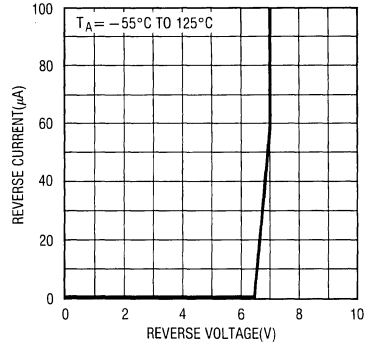
Forward Characteristics



Reverse Characteristics

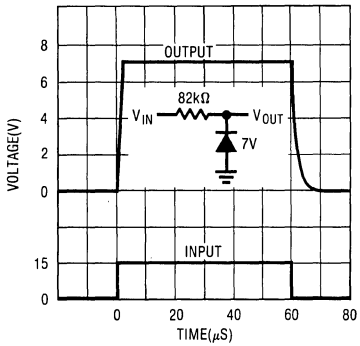


Reverse Characteristics

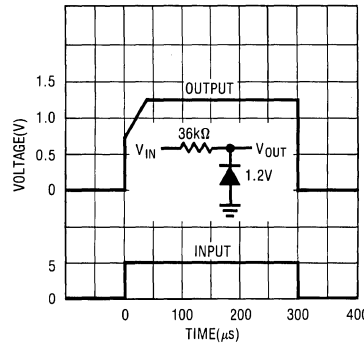


TYPICAL PERFORMANCE CHARACTERISTICS

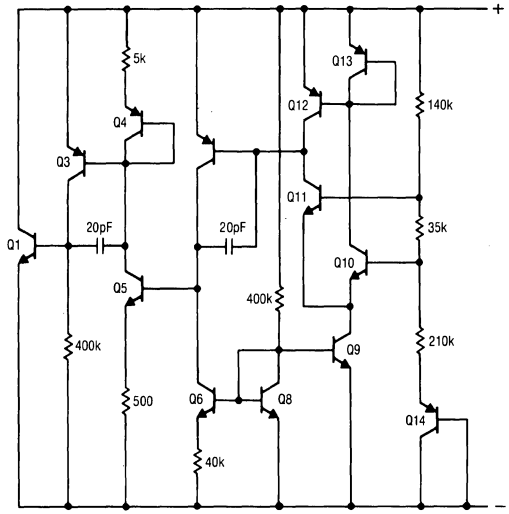
Response Time



Response Time



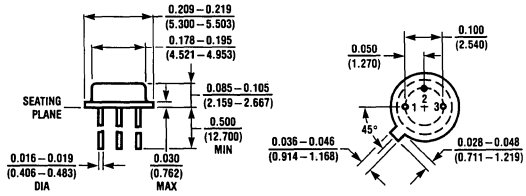
SCHEMATIC DIAGRAM



PACKAGE DESCRIPTION

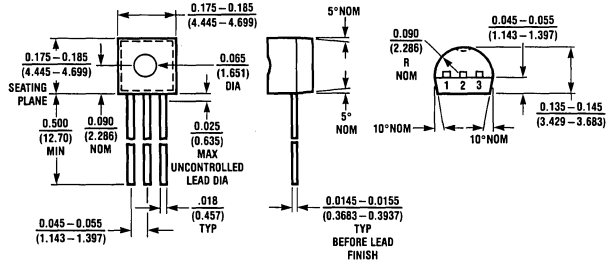
Dimensions in inches (millimeters) unless otherwise noted.

H Package Metal Can



$T_j$max	θ_{ja}	θ_{jc}
150°C	440°C/W	80°C/W

Z Package Plastic



$T_j$max	θ_{ja}
100°C	160°C/W

FEATURES

- Direct Replacement for Present References
- Ultra Low Drift—3ppm/°C Typ.
- Curvature Corrected
- Series or Shunt Operation
- Ultra High Line Rejection ≈ ½ppm/V
- Low Output Impedance ≈0.02Ω
- Tight Initial Output Voltage
- 100% Noise Tested

APPLICATIONS

- A to D and D to A Converters
- Precision Regulators
- Constant Current Sources
- V to F Converters
- Bridge Excitation

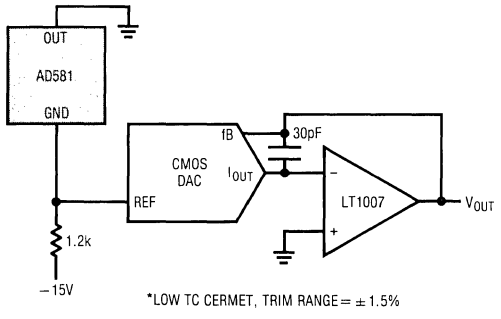
DESCRIPTION

The AD580/AD581 are bandgap voltage references utilizing thin film technology and a greatly improved curvature correction technique. Wafer level trimming of both reference and output voltage combines to produce units with high yields to very low TC and tight initial tolerance of output voltage.

The AD580/AD581 can both sink and source up to 10mA and can be used in either the series or shunt mode. This allows the reference to be used for both positive and negative output voltages without external components. Minimum input-output voltage is less than 1V in the series mode, providing improved tolerance of low line conditions.

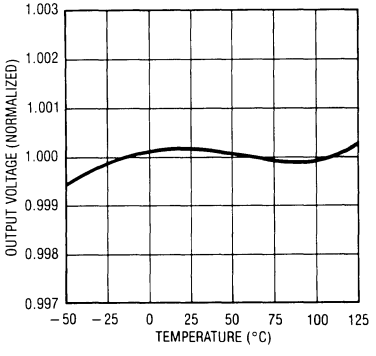
For voltage references with improved specifications, please see the LT1019, LT1021, and LT1031 data sheets.

Negative 10V Reference for CMOS DAC



*LOW TC CERMET, TRIM RANGE = ±1.5%

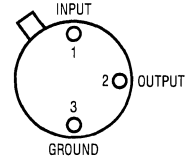
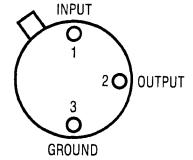
Output Voltage Drift



ABSOLUTE MAXIMUM RATINGS

Input Voltage 40V
Storage Temperature Range ..... –65°C to 175°C
Lead Temperature (Soldering, 10 sec.) ..... 300°C
Operating Temperature Range
J, K, L, M Grades ..... 0°C to 70°C
S, T, U Grades ..... –55°C to 125°C

PACKAGE/ORDER INFORMATION

	ORDER PART NUMBER
BOTTOM VIEW  H PACKAGE TO-52 METAL CAN	AD580JH AD580KH AD580LH AD580MH AD580SH AD580TH AD580UH
BOTTOM VIEW  H PACKAGE TO-39 METAL CAN	AD581JH AD581KH AD581LH AD581SH AD581TH AD581UH

AD580 ELECTRICAL CHARACTERISTICS $V_{IN} = +15V, T_A = 25°C$ unless otherwise noted

SYMBOL	PARAMETER	CONDITIONS		AD580 MIN	AD580 TYP	AD580 MAX	UNITS
V_R	Output Voltage	AD580J		2.425	2.500	2.575	V
		AD580K, S		2.475	2.500	2.525	V
		AD580L, M, T, U		2.490	2.500	2.510	V
TC	Output Voltage Change Over Temperature in mV and (ppm/°C)	AD580J (0°C to 70°C)	●			15 (85)	mV (ppm/°C)
		AD580K (0°C to 70°C)	●			7 (40)	mV (ppm/°C)
		AD580L (0°C to 70°C)	●			4.3 (25)	mV (ppm/°C)
		AD580M (0°C to 70°C)	●			1.75 (10)	mV (ppm/°C)
		AD580S (–55°C to +125°C)	●			25 (55)	mV (ppm/°C)
		AD580T (–55°C to +125°C)	●			11 (25)	mV (ppm/°C)
		AD580U (–55°C to +125°C)	●			4.5 (10)	mV (ppm/°C)
$\frac{\Delta V_{OUT}}{\Delta V_{IN}}$	Line Regulation	$7V \le V_{IN} \le 30V$ AD580J, S			0.5	6	mV
		AD580K			0.5	4	mV
		AD580L, M, T, U			0.5	2	mV
		$4.5V \le V_{IN} \le 7V$ AD580J, S			0.1	3	mV
		AD580K			0.1	2	mV
		AD580L, M, T, U			0.1	1	mV
$\frac{\Delta V_{OUT}}{\Delta I_{OUT}}$	Load Regulation (Sourcing) Shunt Mode	$0 \le I_{OUT} \le 10mA$			1	10	mV
		$1.5mA \le I_{SHUNT} \le 10mA$			2	10	mV
I_Q	Quiescent Current				0.75	1.5	mA
e_n	Output Noise (Note 1)	0.1Hz to 10Hz			10		μVp-p
	Output Voltage Stability with Time	Per Month			25		μV
		Long Term			250		μV

AD581 ELECTRICAL CHARACTERISTICS V_{IN} = +15V, T_A = 25°C unless otherwise noted

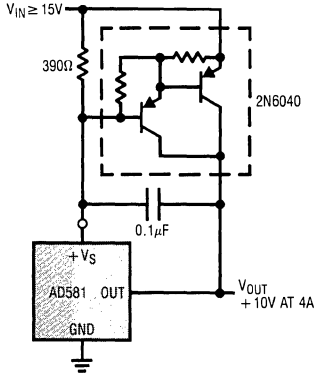
SYMBOL	PARAMETER	CONDITIONS		AD581 MIN	AD581 TYP	AD581 MAX	UNITS
V_R	Output Voltage	AD581S, J		9.970	10.000	10.030	V
		AD581T, K		9.990	10.000	10.010	V
		AD581U, L		9.995	10.000	10.005	V
TC	Output Voltage Change, Maximum Deviation from 25°C in mV and (ppm/°C)	AD581J (0°C to 70°C)	●			13.5 (30)	mV (ppm/°C)
		AD581K (0°C to 70°C)	●			6.75 (15)	mV (ppm/°C)
		AD581L (0°C to 70°C)	●			2.25 (5)	mV (ppm/°C)
		AD581S (−55°C to +125°C)	●			30 (30)	mV (ppm/°C)
		AD581T (−55°C to +125°C)	●			15 (15)	mV (ppm/°C)
		AD581U (−55°C to +125°C)	●			10 (10)	mV (ppm/°C)
$\frac{\Delta V_{OUT}}{\Delta V_{IN}}$	Line Regulation	15V ≤ V_{IN} ≤ 30V			0.5	3	mV
		13V ≤ V_{IN} ≤ 15V			0.1	1	mV
$\frac{\Delta V_{OUT}}{\Delta I_{OUT}}$	Load Regulation (Sourcing) Shunt Mode	0 ≤ I_{OUT} ≤ 5mA			50	500	μV/mA
		1mA ≤ I_{SHUNT} ≤ 5mA			100	500	μV/mA
I_Q	Quiescent Current				0.75	1.0	mA
e_n	Output Noise (Note 1)	0.1Hz to 10Hz			30		μVp-p
	Long Term Stability	Non-Cumulative			25		ppm/kHr
I_{SC}	Short Circuit Current				30		mA
I_{OUT}	Output Current	Sourcing		10	25		mA
		Sourcing	●	5			mA
		Sinking	●	5			mA

The ● denotes the specifications which apply over the full operating temperature range.

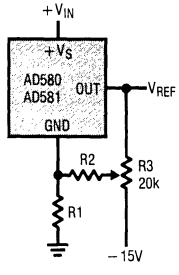
Note 1: Although 0.1Hz to 10Hz noise is not a standard production test, Linear Technology does 100% test 10Hz to 1kHz noise. Consult factory for details.

TYPICAL APPLICATIONS

High Current Precision Supply

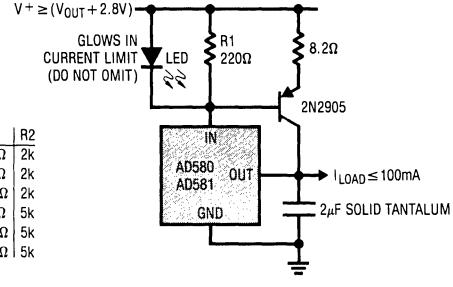


Suggested Output Trim



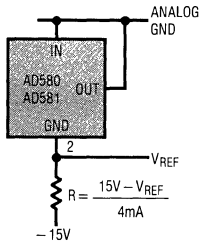
	R1	R2
AD580J	47Ω	2k
AD580K, S	15Ω	2k
AD580L, M, T, U	6.8Ω	2k
AD581S, J	18Ω	5k
AD581T, K	6.8Ω	5k
AD581U, L	3.3Ω	5k

Output Current Boost with Current Limit

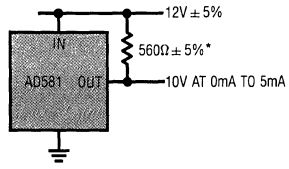


TYPICAL APPLICATIONS

Two-Terminal Negative Reference

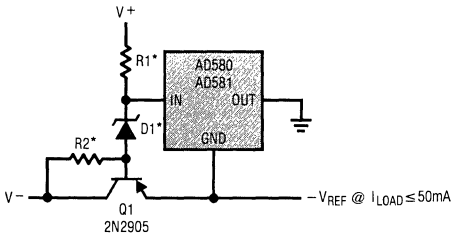


12V Supply Connection



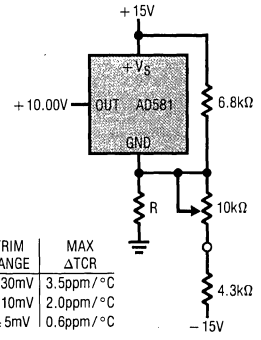
*NOT REQUIRED ON LTC AD580 OR AD581

Negative Series Reference



*R1 = (V+ − 5V) / 2mA, R2 = (|V−| − VREF) / 1mA, D1 ≈ VREF + 5V

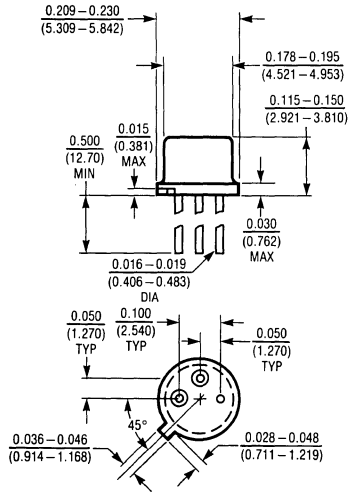
Optional Trim Configuration



R	TRIM RANGE	MAX ΔTCR
22Ω	± 30mV	3.5ppm/°C
12Ω	± 10mV	2.0ppm/°C
3.9Ω	± 5mV	0.6ppm/°C

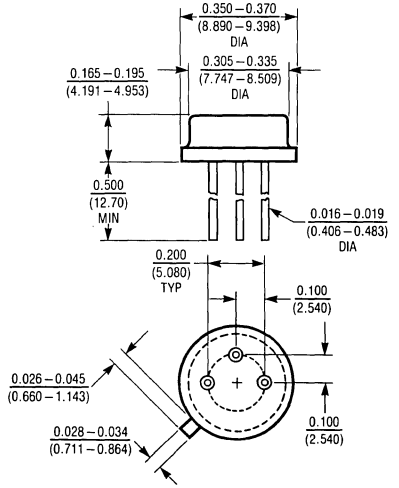
PACKAGE DESCRIPTION

AD580
TO-52



T_{jmax}	θ_{JA}
150°C	360°C/W

AD581
TO-39



T_{jmax}	θ_{JA}
150°C	150°C/W

6.9V Precision Voltage Reference

FEATURES

- *Guaranteed* 10 ppm/°C temperature coefficient
- *Guaranteed* 1.0Ω max. dynamic impedance
- *Guaranteed* 20μV max. wideband noise
- Wide operating current range 0.6mA to 15mA

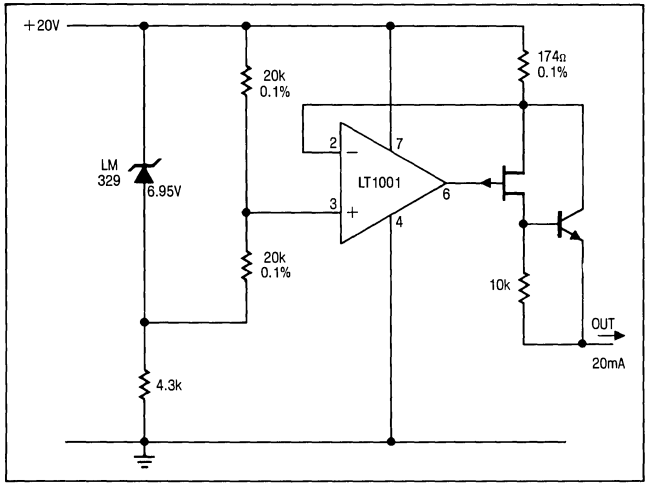
APPLICATIONS

- Transducers
- A/D and D/A Converters
- Calibration Standards
- Instrumentation Reference

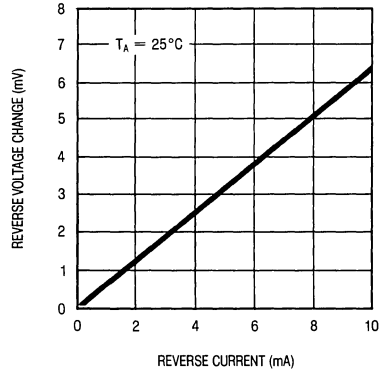
DESCRIPTION

The LM129 temperature compensated 6.9 Volt zener references provide excellent stability over time and temperature, very low dynamic impedance and a wide operating current range. The device achieves low dynamic impedance by incorporating a high gain shunt regulator around the zener. The excellent noise performance of the device is achieved by using a "buried zener" design which eliminates surface noise phenomenon associated with ordinary zeners. To serve a wide variety of applications, the LM129 is available in several temperature coefficient grades and two package styles. A 20mA positive current source application is shown below.

20mA Positive Current Source



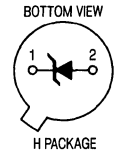
Reverse Voltage Change



ABSOLUTE MAXIMUM RATINGS

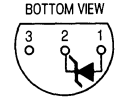
Reverse Breakdown Current..... 30mA
Forward Current..... 2mA
Operating Temperature Range
LM129 ..... −55°C to 125°C
LM329 ..... 0°C to 70°C
Storage Temperature Range
LM129 ..... −65°C to 150°C
LM329 ..... −65°C to 150°C
Lead Temperature (Soldering, 10 sec.)..... 300°C

PACKAGE/ORDER INFORMATION



H PACKAGE
TO-46 METAL CAN

LM129AH LM329AH
LM129BH LM329BH
LM129CH LM329CH
LM329DH



Z PACKAGE
TO-92 PLASTIC

LM329AZ
LM329BZ
LM329CZ
LM329DZ

ELECTRICAL CHARACTERISTICS (See Note 1)

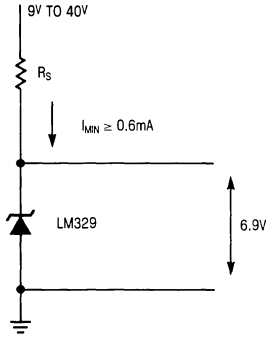
SYMBOL	PARAMETER	CONDITIONS		LM129A,B,C MIN	LM129A,B,C TYP	LM129A,B,C MAX	LM329A,B,C,D MIN	LM329A,B,C,D TYP	LM329A,B,C,D MAX	UNITS
V_Z	Reverse Breakdown Voltage	$T_A = 25°C$ $0.6mA \leq I_R \leq 15mA$		6.7	6.9	7.2	6.6	6.9	7.25	V
$\frac{\Delta V_Z}{\Delta I_R}$	Reverse Breakdown Voltage Change with Current	$T_A = 25°C$ $0.6mA \leq I_R \leq 15mA$			9	14		9	20	mV
$\frac{\Delta V_Z}{\Delta I_R}$	Reverse Breakdown Voltage Change with Current	$1mA \leq I_R \leq 15mA$	●		12			12		mV
$\frac{\Delta V_Z}{\Delta \text{ Temp}}$	Temperature Coefficient	$I_R = 1mA$								
		LM129A/LM329A	●		6	10		6	10	ppm/°C
		LM129B/LM329B	●		15	20		15	20	ppm/°C
		LM129C/LM329C	●		30	50		30	50	ppm/°C
		LM329D	●					50	100	ppm/°C
	Change in Temperature Coefficient	$1mA \leq I_R \leq 15mA$	●		1			1		ppm/°C
r_Z	Dynamic Impedance	$T_A = 25°C, I_R = 1mA$			0.6	1		0.8	2	Ω
r_Z	Dynamic Impedance	$1mA \leq I_R \leq 15mA$	●		0.8			1		Ω
e_n	RMS Noise	$T_A = 25°C$, $10Hz \leq f \leq 10kHz$			7	20		7	100	μV
$\frac{\Delta V_Z}{\Delta \text{ Time}}$	Long Term Stability	$T_A = 45°C \pm 0.1°C$ $I_R = 1mA \pm 0.3\%$			20			20		ppm/kHr

The ● denotes the specifications which apply over full operating temperature range.

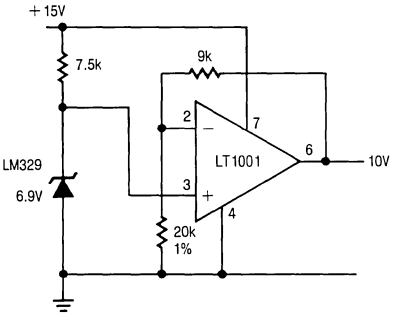
Note 1: These specifications apply over the full operating temperature range unless otherwise noted. To determine the junction temperature as a function of the ambient temperature, see θ_{JA} for each package.

TYPICAL APPLICATIONS

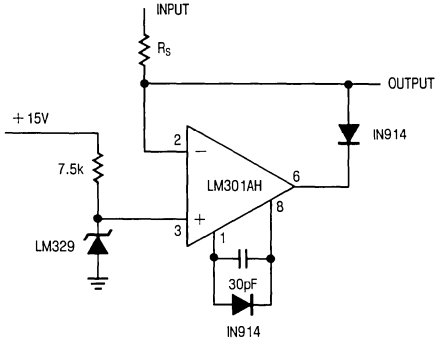
Common Reference



Buffered Reference Using a Single Supply

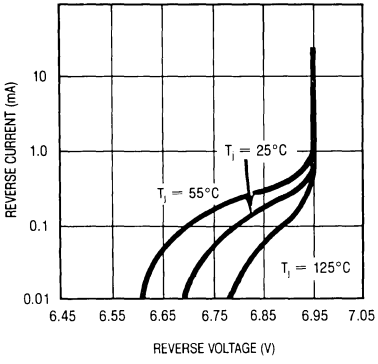


Precision Clamp

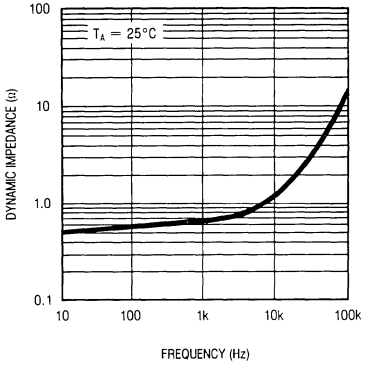


TYPICAL PERFORMANCE CHARACTERISTICS

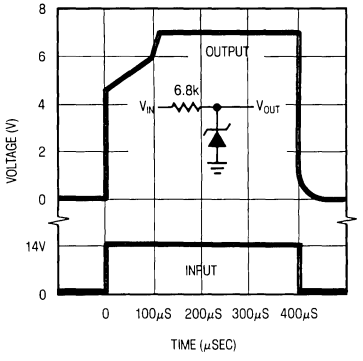
Reverse Characteristics



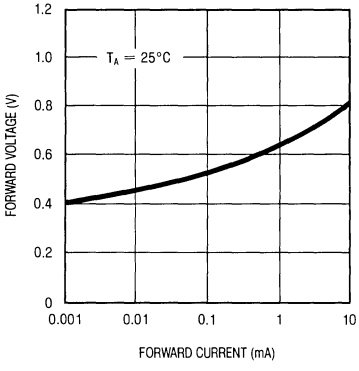
Dynamic Impedance



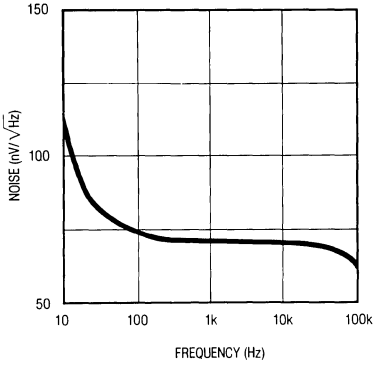
Response Time



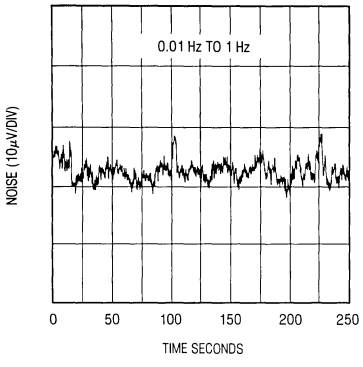
Forward Characteristics



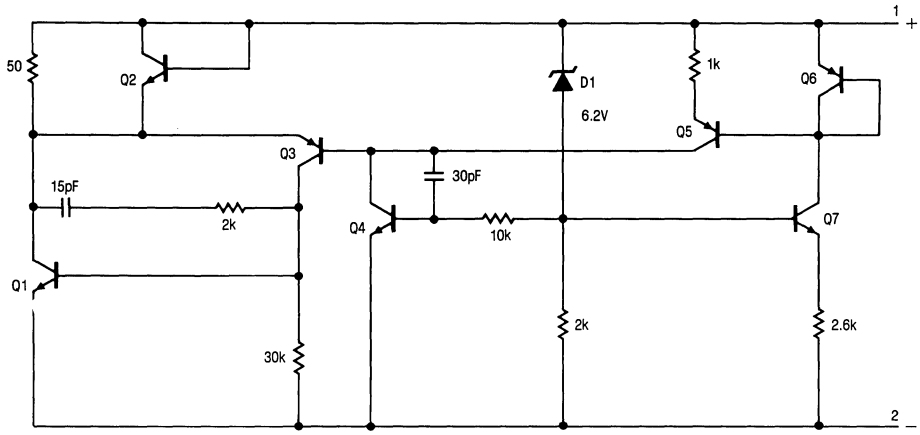
Noise Voltage



Low Frequency Noise Voltage

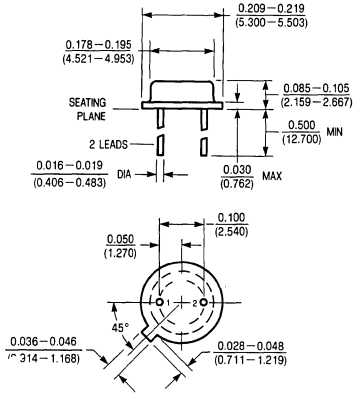


SCHEMATIC DIAGRAM



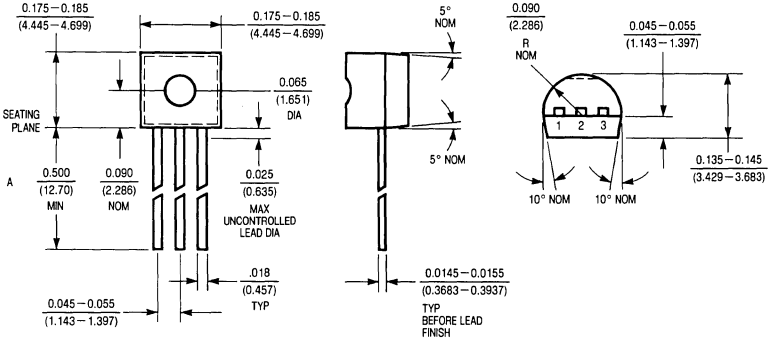
PACKAGE DESCRIPTION

H Package, 2 Lead TO-46 Metal Can



$T_j$max	Θ_{ja}	Θ_{jc}
150°C	440°C/W	80°C/W

Z Package, 3 Lead TO-92 Plastic



$T_j$max	Θ_{ja}
100°C	160°C/W

Constant Current Source and Temperature Sensor

FEATURES

- 1μA to 10mA Operation
- 0.02%/V Regulation
- 0.8V to 40V Operating Voltage
- Can be Used as Linear Temperature Sensor
- Draws No Reverse Current
- Supplied in Standard Transistor Packages

APPLICATIONS

- Current Mode Temperature Sensing
- Constant Current Source for Shunt References
- Cold Junction Compensation
- Constant-Gain Bias for Bipolar Differential Stage
- Micropower Bias Networks
- Buffer for Photoconductive Cell
- Current Limiter

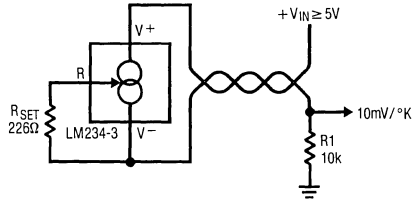
DESCRIPTION

The LM134 is a three-terminal current source designed to operate at current levels from 1μA to 10mA, as set by an external resistor. The device operates as a true two-terminal current source, requiring no extra power connections or input signals. Regulation is typically 0.02%/V and terminal-to-terminal voltage can range from 800mV to 40V.

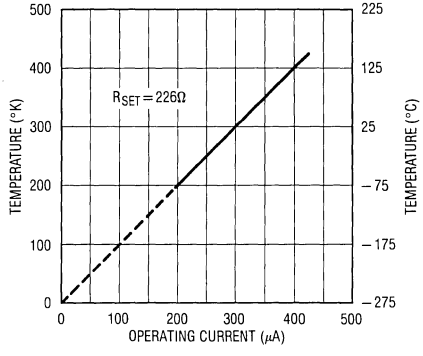
Because the operating current is *directly proportional to absolute temperature* in degrees Kelvin, the device will also find wide applications as a temperature sensor. The temperature dependence of the operating current is +0.336%/°C at room temperature. For example, a device operating at 298μA will have a temperature coefficient of +1μA/°C. The temperature dependence is extremely accurate and repeatable. Devices specified as temperature sensors in the 100μA to 1mA range are the LM134-3, LM234-3 and the LM134-6, LM234-6, with the dash numbers indicating ±3°C and ±6°C accuracies, respectively.

If a zero temperature coefficient current source is required, this is easily achieved by adding a diode and a resistor.

Remote Temperature Sensor with Voltage Output



Operating Current vs Temperature



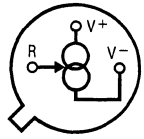
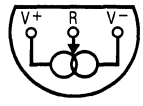
ABSOLUTE MAXIMUM RATINGS

V^+ to V^- Forward Voltage
- LM134 ..... 40V
- LM134-3/LM134-6/LM234-3/ LM234-6/LM334 ..... 30V

V^+ to V^- Reverse Voltage 20V
R Pin to V^- Voltage 5V
Set Current 10mA
Power Dissipation 200mW
Operating Temperature Range
- LM134/LM134-3/LM134-6 .... −55°C to 125°C
- LM234-3/LM234-6 ..... −25°C to 100°C
- LM334 ..... 0°C to 70°C

Lead Temperature (Soldering, 10 sec.) ..... 300°C

PACKAGE/ORDER INFORMATION

	ORDER PART NUMBER	
	CURRENT SOURCE	TEMP SENSOR
BOTTOM VIEW  H PACKAGE TO-46 METAL CAN	LM134H LM334H	LM134H-3 LM234H-3 LM134H-6 LM234H-6
BOTTOM VIEW  Z PACKAGE TO-92 PLASTIC	LM334Z	LM234Z-3 LM234Z-6

ELECTRICAL CHARACTERISTICS CURRENT SOURCE (Note 1)

SYMBOL	PARAMETER	CONDITIONS	LM134 MIN	LM134 TYP	LM134 MAX	LM334 MIN	LM334 TYP	LM334 MAX	UNITS
ΔI_{SET}	Set Current Error, $V^+ = 2.5V$ (Note 2)	$10\mu A \le I_{SET} \le 1mA$			3			6	%
		$1mA < I_{SET} \le 5mA$			5			8	%
		$2\mu A \le I_{SET} < 10\mu A$			8			12	%
	Ratio of Set Current to V^- Current	$10\mu A \le I_{SET} \le 1mA$	14	18	23	14	18	26	
		$1mA \le I_{SET} \le 5mA$		14			14		
		$2\mu A \le I_{SET} \le 10\mu A$		18	23		18	26	
V_{MIN}	Minimum Operating Voltage	$2\mu A \le I_{SET} \le 100\mu A$		0.8			0.8		V
		$100\mu A < I_{SET} \le 1mA$		0.9			0.9		V
		$1mA < I_{SET} \le 5mA$		1.0			1.0		V
$\frac{\Delta I_{SET}}{\Delta V_{IN}}$	Average Change in Set Current with Input Voltage	$1.5V \le V^+ \le 5V$ $2\mu A \le I_{SET} \le 1mA$		0.02	0.05		0.02	0.1	%/V
		$5V \le V^+ \le V_{MAX}$ (Note 4)		0.01	0.03		0.01	0.05	%/V
		$1.5V \le V \le 5V$ $1mA < I_{SET} \le 5mA$		0.03			0.03		%/V
		$5V \le V \le V_{MAX}$ (Note 4)		0.02			0.02		%/V
	Temperature Dependence of Set Current (Note 3)	$25\mu A \le I_{SET} \le 1mA$	0.96T	T	1.04T	0.96T	T	1.04T	
C_S	Effective Shunt Capacitance			15			15		pF

ELECTRICAL CHARACTERISTICS TEMPERATURE SENSOR (Note 1)

SYMBOL	PARAMETER	CONDITIONS	LM134-3, LM234-3			LM134-6, LM234-6			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
ΔI_{SET}	Set Current Error, $V^+ = 2.5V$ (Note 2)	$100\mu A \le I_{SET} \le 1mA$ $T_j = 25°C$			±1			±2	%
	Equivalent Temperature Error				±3			±6	°C
	Ratio of Set Current to V^- Current	$100\mu A \le I_{SET} \le 1mA$	14	18	26	14	18	26	
V_{MIN}	Minimum Operating Voltage	$100\mu A \le I_{SET} \le 1mA$		0.9			0.9		V
$\frac{\Delta I_{SET}}{\Delta V_{IN}}$	Average Change in Set Current with Input Voltage	$1.5V \le V^+ \le 5V$ $100\mu A \le I_{SET} \le 1mA$		0.02	0.05		0.02	0.1	%/V
		$5V \le V^+ \le 30V$		0.01	0.03		0.01	0.05	%/V
	Temperature Dependence of Set Current (Note 3)	$100\mu A \le I_{SET} \le 1mA$	0.98T	T	1.02T	0.97T	T	1.03T	
	Equivalent Slope Error			±2			±3		%
C_S	Effective Shunt Capacitance			15			15		pF

Note 1: Unless otherwise specified, tests are performed at $T_j = 25°C$ with pulse testing so that junction temperature does not change during test.

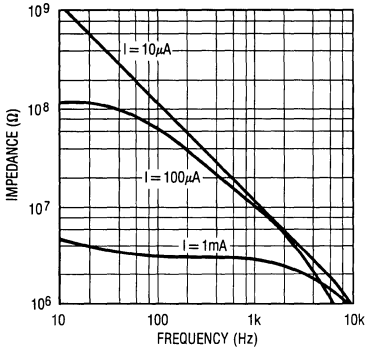
Note 2: Set current is the current flowing into the V^+ pin. It is determined by the following formula: $I_{SET} = 67.7mV/R_{SET}$ (@25°C). Set current error is expressed as a percent deviation from this amount. I_{SET} increases at 0.336%/°C@$T_j = 25°C$.

Note 3: I_{SET} is directly proportional to absolute temperature (°K). I_{SET} at any temperature can be calculated from: $I_{SET} = I_0 (T/T_0)$ where I_0 is I_{SET} measured at T_0 (°K).

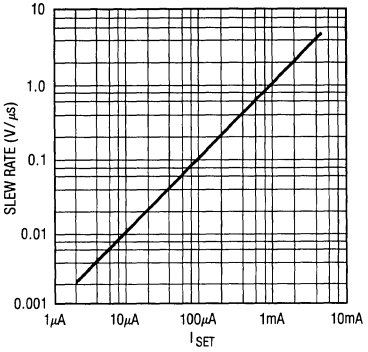
Note 4: $V_{MAX} = 40V$ for LM134 and 30V for other grades.

TYPICAL PERFORMANCE CHARACTERISTICS

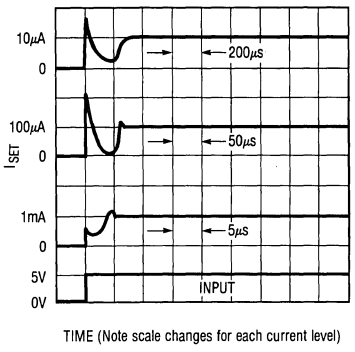
Output Impedance



Maximum Slew Rate for Linear Operation

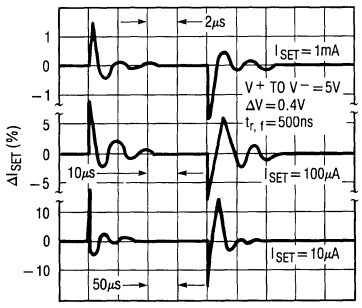


Start-Up



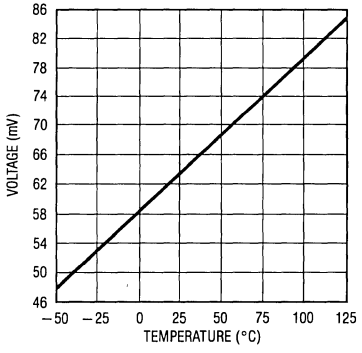
TIME (Note scale changes for each current level)

Transient Response

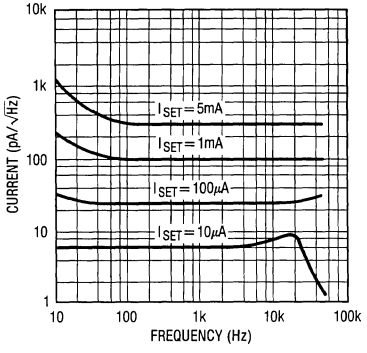


TIME (Note scale changes for each current level)

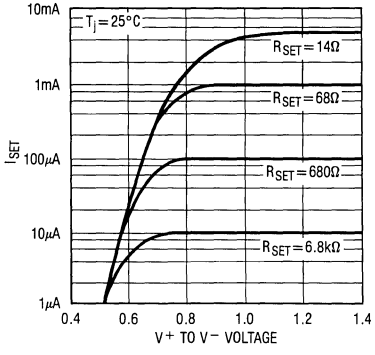
Voltage Across R_{SET}



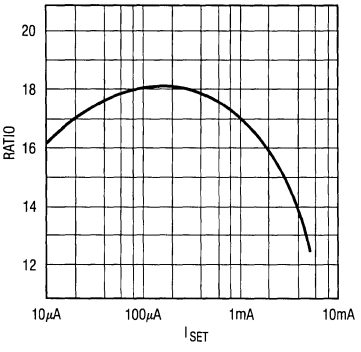
Current Noise



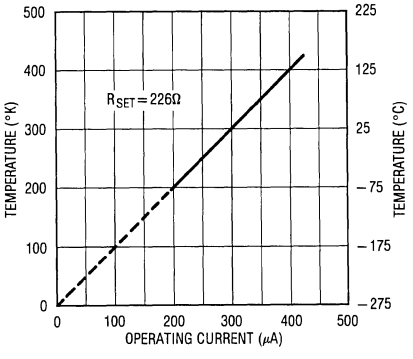
Turn-On Voltage



Ratio of I_{SET} to V^- Current



Operating Current vs Temperature



APPLICATIONS INFORMATION

Basic Theory of Operation

The equivalent circuit of the LM134 is shown in Figure 1. A reference voltage of 64mV is applied to the minus input of A1 with respect to the V^- pin. A1 serves the drive to Q2 to keep the R pin at 64mV, independent of the value of R_{SET}. Transistor Q1 is matched to Q2 at a 17:1 ratio so that the current flowing out of the V^- pin is always 1/18 of the total current into the V^+ pin. This total current is called I_{SET} and is equal to

$$\left(\frac{64mV}{R_{SET}}\right)\left(\frac{18}{17}\right)=\frac{67.7mV}{R_{SET}}.$$

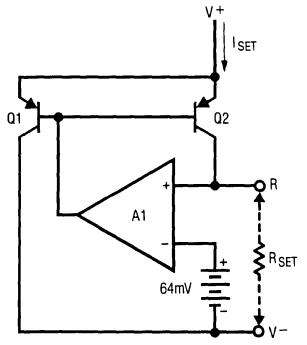


Figure 1

The 67.7mV equivalent reference voltage is directly proportional to absolute temperature in degrees Kelvin (see curve, "Operating Current vs Temperature"). This means that the reference voltage can be plotted as a straight line going from 0mV at absolute zero temperature to 67.7mV at 298°K (25°C). The slope of this line is 67.7mV/298 = 227μV/°C.

The accuracy of the device is specified as a percent error at room temperature, or in the case of the -3 and -6 devices, as both a percent error and an equivalent temperature error. The LM134 operating current changes at a percent rate equal to (100) (227μV/°C)/(67.7mV) = 0.336%/°C at 25°C, so each 1% operating current error is equivalent to ≈3°C temperature error when the device is used as a temperature sensor. The slope accuracy (temperature coefficient) of the LM134 is expressed as a ratio compared to unity. The LM134-3, for instance, is specified at 0.98T to 1.02T, indicating that the maximum slope error of the device is ±2% when the room temperature current is set to the exact desired value.

Supply Voltage Slew Rate

At slew rates above a given threshold (see curve), the LM134 may exhibit non-linear current shifts. The slewing rate at which this occurs is directly proportional to I_{SET}. At I_{SET} = 10μA, maximum dv/dt is 0.01V/μs; at I_{SET} = 1 mA, the limit is 1V/μs. Slew rates above the limit do not harm the LM134, or cause large currents to flow.

Thermal Effects

Internal heating can have a significant effect on current regulation for I_{SET} greater than 100μA. For example, each 1V increase across the LM134 at I_{SET} = 1mA will increase junction temperature by ≈0.4°C in still air. Output current (I_{SET}) has a temperature coefficient of ≈0.33%/°C, so the change in current due to temperature rise will be (0.4) (0.33) = 0.132%. This is a 10:1 degradation in regulation compared to true electrical effects. Thermal effects, therefore, must be taken into account when DC regulation is critical and I_{SET} exceeds 100μA. Heat sinking of the TO-46 package or the TO-92 leads can reduce this effect by more than 3:1.

Shunt Capacitance

In certain applications, the 15pF shunt capacitance of the LM134 may have to be reduced, either because of loading problems or because it limits the AC output impedance of the current source. This can be easily accomplished by buffering the LM134 with an FET, as shown in the applications. This can reduce capacitance to less than 3pF and improve regulation by at least an order of magnitude. DC characteristics (with the exception of minimum input voltage) are not affected.

APPLICATIONS INFORMATION

Noise

Current noise generated by the LM134 is approximately 4 times the shot noise of a transistor. If the LM134 is used as an active load for a transistor amplifier, input referred noise will be increased by about 12dB. In many cases, this is acceptable and a single stage amplifier can be built with a voltage gain exceeding 2000.

Lead Resistance

The sense voltage which determines the operating current of the LM134 is less than 100mV. At this level, thermocouple or lead resistance effects should be minimized by locating the current setting resistor physically close to the device. Sockets should be avoided if possible. It takes only 0.7Ω contact resistance to reduce output current by 1% at the 1mA level.

Start-Up Time

The LM134 is designed to operate at currents as low as 1μA. This requires that internal biasing current be well below that level because the device achieves its wide operating current range by using part of the operating current as bias current for the internal circuitry. To ensure start-up, however, a fixed trickle current must be provided internally. This is typically in the range of 20nA–200nA and is provided by the special ultra-low I_{DSS} FETs shown in the Schematic Diagram as Q7 and Q8. The start-up time of the LM134 is determined by the I_{DSS} of these FETs and the capacitor C1. This capacitor must charge to approximately 500mV before Q3 turns on to start normal circuit operation. This takes as long as (500mV) (50pF)/(20nA) = 1.25ms for very low I_{DSS} values.

Using the LM134 as a Temperature Sensor

Because it has a highly linear output characteristic, the LM134 makes a good temperature sensor. It is particularly useful in remote sensing applications because it is a current output device and is therefore not affected by long wire runs. It is easy to calibrate, has good long term stability, and can be interfaced directly with most data acquisition systems, eliminating the expensive preamplifiers required for thermocouples and platinum sensors.

A typical temperature sensor application is shown in Figure 2. The LM134 operating current at 25°C is set at 298μA by the 226Ω resistor, giving an output of 1μA/°K. The current flows through the twisted pair sensor leads to the 10kΩ termination resistor, which converts the current output to a voltage of 10mV/°K referred to ground. The voltage across the 10kΩ resistor will be 2.98V at 25°C, with a slope of 10mV/°C. The simplest way to convert this signal to a Centigrade scale is to subtract a constant 2.73V in software. Alternately, a hardware conversion can be used, as shown in Figure 3, using an LT1009 as a level shifter to offset the output to a Centigrade scale.

The resistor (R_{SET}) used to set the operating current of the LM134 in temperature sensing applications should have low temperature coefficient and good long term stability.

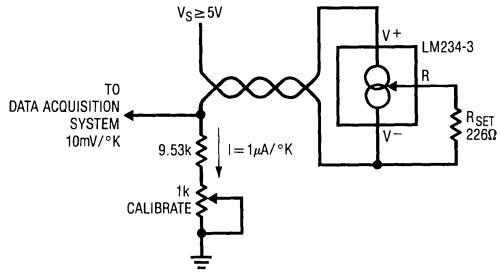


Figure 2. Kelvin Temperature Sensor

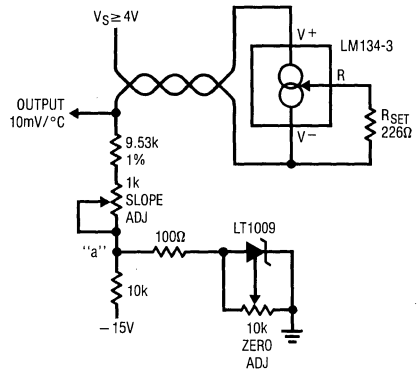


Figure 3. Centigrade Temperature Sensor

APPLICATIONS INFORMATION

30ppm/°C drift in the resistor will change the slope of the temperature sensor by 1%, assuming that the resistor is at the same temperature as the sensor, which is usually the case since the resistor should be located physically close to the LM134 to prevent errors due to wire resistance. A long term shift of 0.3% in the resistor will create a 1°C temperature error. The long term drift of the LM134 is typically much better than this, so stable resistors must be used for best long term performance.

Calibration of the LM134 as a temperature sensor is extremely easy. Referring to Figure 2, calibration is achieved by trimming the termination resistor. *This theoretically trims both zero and slope simultaneously for Centigrade and Fahrenheit applications.* The initial errors in the LM134 are directly proportional to absolute temperature, just like the actual output. This allows the sensor to be trimmed at any temperature and have the slope error be corrected at the same time. Residual slope error is typically less than 1% after this single trim is completed.

The two trims shown in Figure 3 are still intended to be a "one point" temperature calibration, where the zero and the slope are trimmed at a single temperature. The LT1009 reference is adjusted to give 2.700V at node "a" at $T_{SENSOR} = 25°C$. The 1k trimmer then adjusts the output for 0.25V, completing the calibration. If the calibration is to be done at a temperature other than 25°C, trim the LT1009 for $2.7025 - (1\mu A)[T_{SENSOR}\ (°C)](100\Omega)$ at node "a", then adjust the 1k trimmer for proper output.

If higher accuracy is required, a two point calibration technique can be used. In Figure 4, separate zero and slope trims are provided. Residual non-linearity is now the limitation on accuracy. Non-linearity of the LM134 in a 100°C span is typically less than 0.5°C. This particular method of trimming has the advantage that the slope trim does not interact with the zero trim. Trim procedure is to adjust for zero output with $T_{SENSOR} = 0°C$, then trim slope for proper output at some convenient second temperature. No further trimming is required.

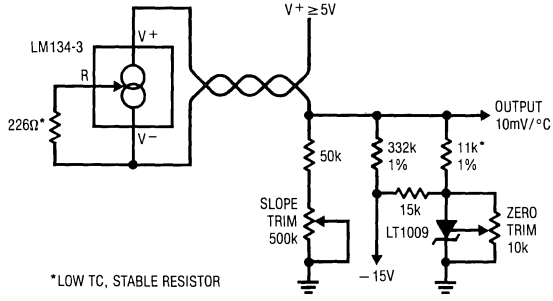
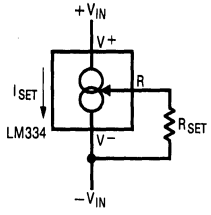


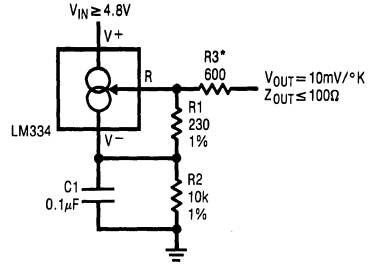
Figure 4. Centigrade Temperature Sensor with 2 Point Trim

TYPICAL APPLICATIONS

Basic 2-Terminal Current Source

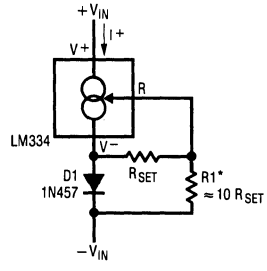


Low Output Impedance Thermometer (Kelvin Output)



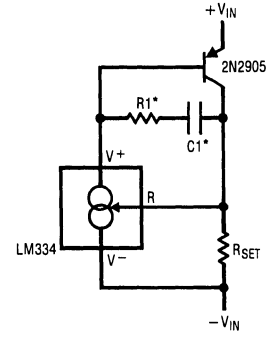
*OUTPUT IMPEDANCE OF THE LM134 AT THE "R" PIN IS APPROXIMATELY $\frac{-R_O}{16}\Omega$, WHERE R_O IS THE EQUIVALENT EXTERNAL RESISTANCE CONNECTED TO THE V− PIN. THIS NEGATIVE RESISTANCE CAN BE REDUCED BY A FACTOR OF 5 OR MORE BY INSERTING AN EQUIVALENT RESISTOR IN SERIES WITH THE OUTPUT.

Zero Temperature Coefficient Current Source



*SELECT RATIO OF R1 TO R_{SET} TO OBTAIN ZERO DRIFT. $I^+ \approx 2\ I_{SET}$.

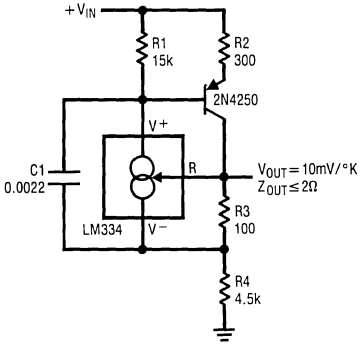
Higher Output Current



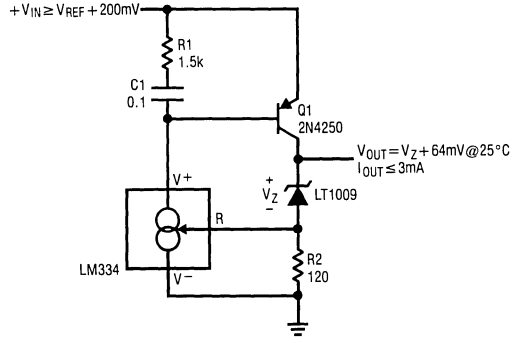
*SELECT R1 AND C1 FOR OPTIMUM STABILITY

TYPICAL APPLICATIONS

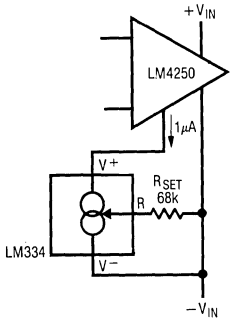
Low Output Impedance Thermometer



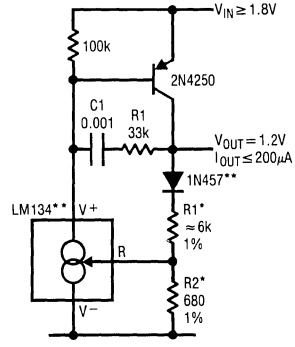
Low Input Voltage Reference Driver



Micropower Bias

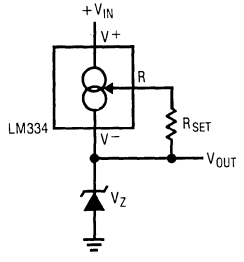


1.2V Regulator with 1.8V Minimum Input



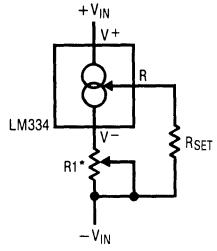
*SELECT RATIO OF R1 TO R2 FOR ZERO TEMPERATURE DRIFT
**LM134 AND DIODE SHOULD BE ISOTHERMAL

Zener Biasing



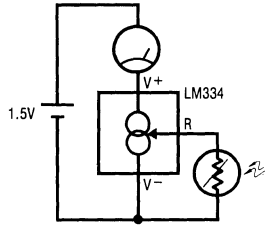
TYPICAL APPLICATIONS

Alternate Trimming Technique

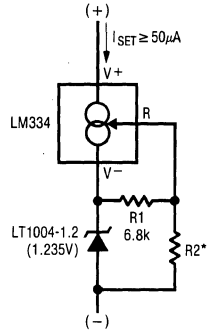


*FOR ±10% ADJUSTMENT, SELECT R_{SET} 10% HIGH AND MAKE R1 ≈ $3R_{SET}$

Buffer for Photoconductive Cell



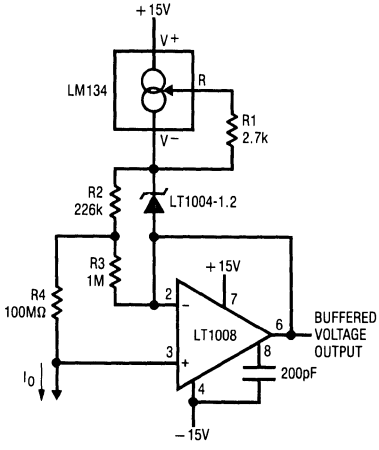
High Precision Low TC Current Source



*$I_{SET} = \frac{1.37V}{R2} + 10\mu A$

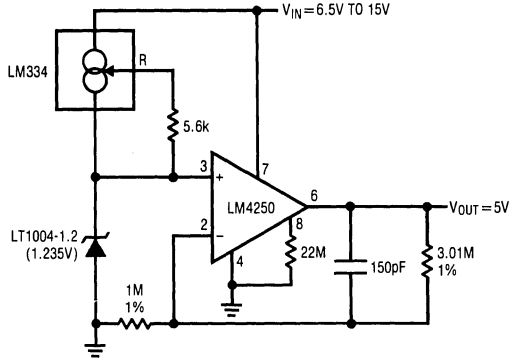
I_{SET} TC = 0.016%/°C + 33nA/°C
REGULATION ≈ 0.001%/V

Precision 10nA Current Source



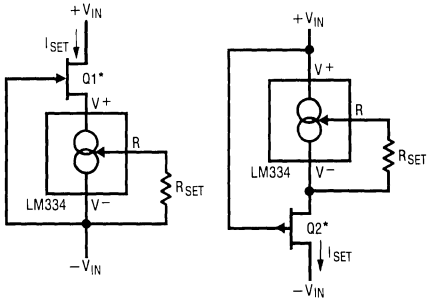
I_O = 10nA
$Z_O \geq 10^{12}\Omega$
COMPLIANCE = −14V TO +12.5V

Micropower 5V Reference



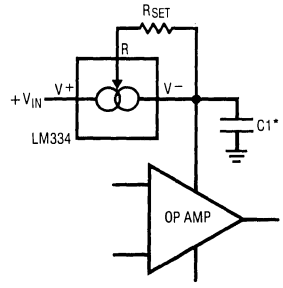
TYPICAL APPLICATIONS

FET Cascoding for Low Capacitance and/or Ultra High Output Impedance



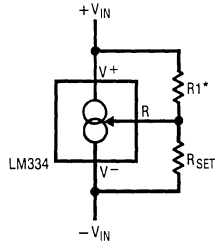
*SELECT Q1 OR Q2 TO ENSURE AT LEAST 1V ACROSS THE LM134. $V_P\,(1-I_{SET}/I_{DSS}) \geq 1.2V$.

In-Line Current Limiter



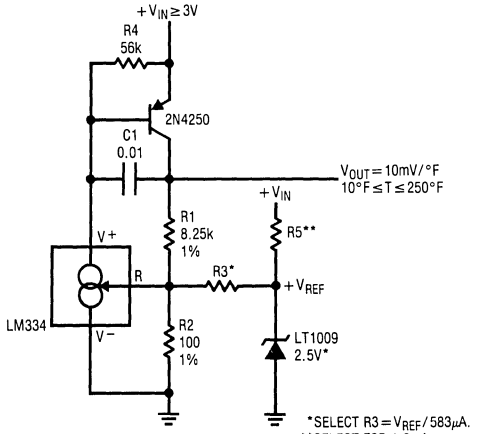
*USE MINIMUM VALUE REQUIRED TO ENSURE STABILITY OF PROTECTED DEVICE. THIS MINIMIZES INRUSH CURRENT TO A DIRECT SHORT.

Generating Negative Output Impedance

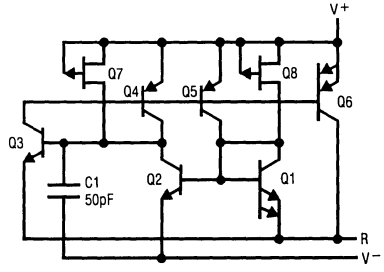


*$Z_{OUT} \approx -16 \bullet$ R1 ($R1/V_{IN}$ MUST NOT EXCEED I_{SET}).

Ground Referred Fahrenheit Thermometer

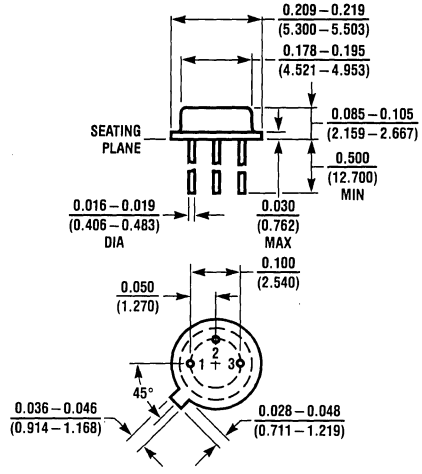


SCHEMATIC DIAGRAM



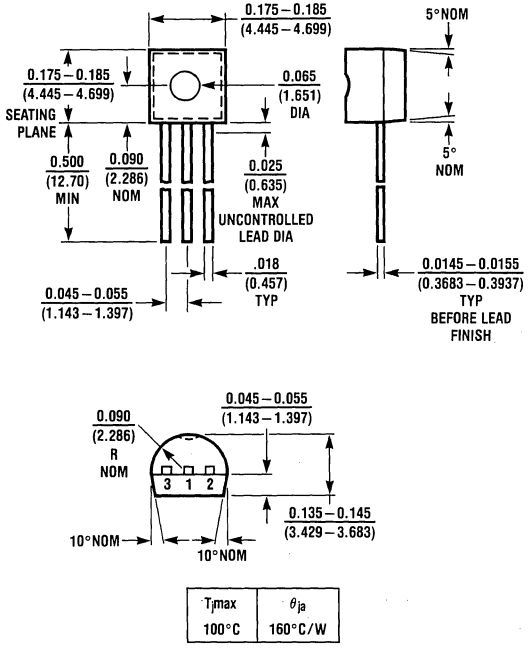
PACKAGE DESCRIPTION

H Package
Metal Can



$T_j$max	θ_{ja}	θ_{jc}
150°C	440°C/W	80°C/W

Z Package
Plastic



$T_j$max	θ_{ja}
100°C	160°C/W

FEATURES

- *Guaranteed* Temperature Stability
- Maximum 0.6Ω Dynamic Impedance
- Adjustable for Minimum Temperature Coefficient
- Wide Operating Current Range

APPLICATIONS

- Reference for 5V Systems
- 8 Bit A/D and D/A Reference
- Digital Voltmeters
- Current Loop Measurement and Control Systems
- Power Supply Monitor

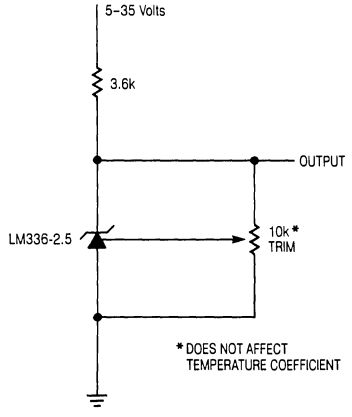
DESCRIPTION

The LM136-2.5 is a general purpose shunt regulator diode designed to operate over a wide current range while maintaining good stability with time and temperature. The third terminal allows either the temperature coefficient to be minimized or the reference voltage to be adjusted without changing the temperature coefficient. Because it operates as a shunt regulator it can be used equally well as a positive or negative reference.

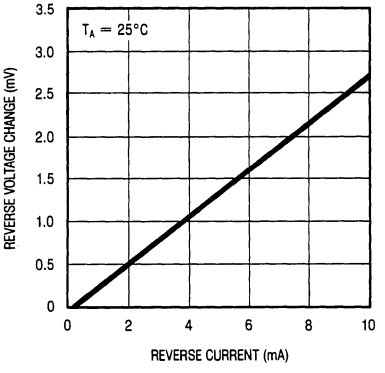
The LM136-2.5 is available with initial tolerances as low as 1% in either a TO-46 metal can for hermetic requirements or a low cost TO-92 plastic package.

Linear's advanced design, test and process techniques have optimized the LM136-2.5 to achieve superior performance and reliability over previous designs. For more demanding precision reference applications requiring very low initial tolerance and temperature coefficients, consult the LT1009 data sheet. A typical 2.5 Volt reference with trim is shown below.

2.5 Volt Reference



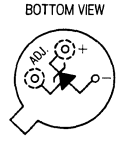
Reverse Voltage Change



ABSOLUTE MAXIMUM RATINGS

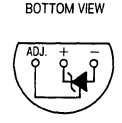
Reverse Current 15mA
Forward Current 10mA
Operating Temperature Range
LM136-2.5 ..... −55°C to 125°C
LM336-2.5 ..... 0°C to 70°C
Storage Temperature Range
LM136-2.5 ..... −65°C to 150°C
LM336-2.5 ..... −65°C to 150°C
Lead Temperature (Soldering, 10 sec.) ..... 300°C

PACKAGE/ORDER INFORMATION



H PACKAGE TO-46 METAL CAN

LM136H-2.5
LM136AH-2.5
LM336H-2.5
LM336BH-2.5
*SEE NOTE 1



Z PACKAGE TO-92 PLASTIC

LM336Z-2.5
LM336BZ-2.5
*SEE NOTE 1

ELECTRICAL CHARACTERISTICS (See Note 1)

SYMBOL	PARAMETER	CONDITIONS		LM136A/LM136 MIN	LM136A/LM136 TYP	LM136A/LM136 MAX	LM336B/LM336 MIN	LM336B/LM336 TYP	LM336B/LM336 MAX	UNITS
V_Z	Reverse Breakdown Voltage	$T_A = 25°C$, $I_R = 1mA$								
		LM136/LM336		2.440	2.490	2.540	2.390	2.490	2.590	V
		LM136A/LM336B		2.465	2.490	2.515	2.440	2.490	2.540	V
$\frac{\Delta V_Z}{\Delta I_R}$	Reverse Breakdown Change with Current	$400\mu A \leq I_R \leq 10mA$								
		$T_A = 25°C$			2.6	6		2.6	10	mV
		$T_{min} \leq T_A \leq T_{max}$	●		3	10		3	12	mV
r_Z	Reverse Dynamic Impedance	$I_R = 1mA$								
		$T_A = 25°C$			0.2	0.6		0.2	1.0	Ω
		$T_{min} \leq T_A \leq T_{max}$	●		0.4	1		0.4	1.4	Ω
$\frac{\Delta V_Z}{\Delta Temp}$	Temperature Stability	V_R adjusted to 2.490V, $I_R = 1mA$								
		$T_{min} \leq T_A \leq T_{max}$								
		LM136A/LM136	●		12	18				mV
		LM336B/LM336	●					1.8	6	mV
		(See Figure 1.)								
$\frac{\Delta V_Z}{\Delta Time}$	Long Term Stability	$T_A = 25°C \pm 0.1°C$, $I_R = 1mA$			20			20		ppm/kHr

The ● denotes the specifications which apply over full operating temperature range.

Note 1: The LT1009 is an improved, low cost, pin for pin replacement for the "A" and "B" versions. For further information consult the LT1009 data sheet.

Adjusting the LM336 for minimum temperature coefficient

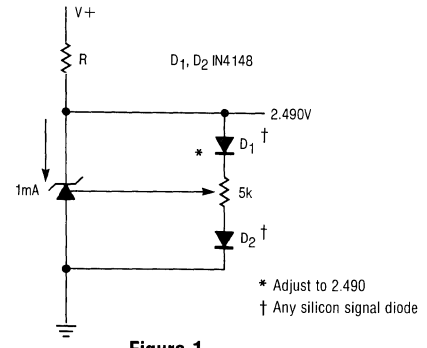
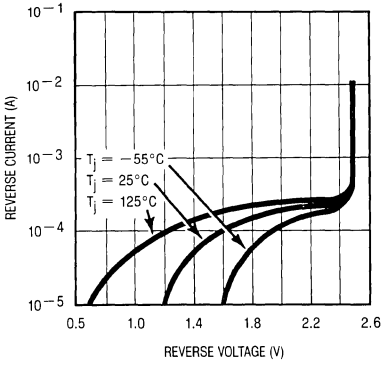


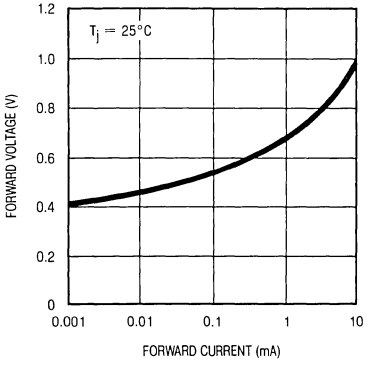
Figure 1

TYPICAL PERFORMANCE CHARACTERISTICS

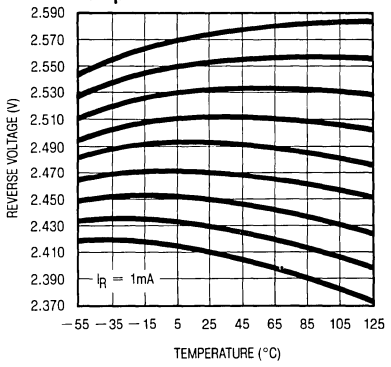
Reverse Characteristics



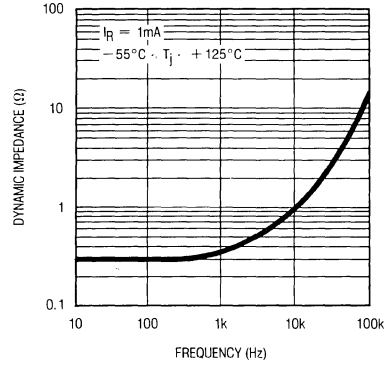
Forward Characteristics



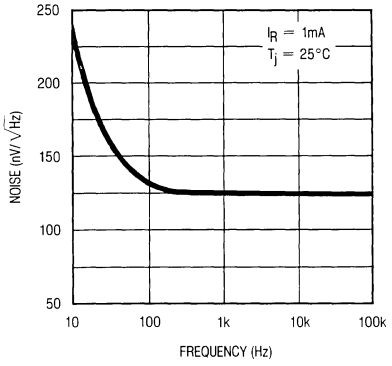
Temperature Drift



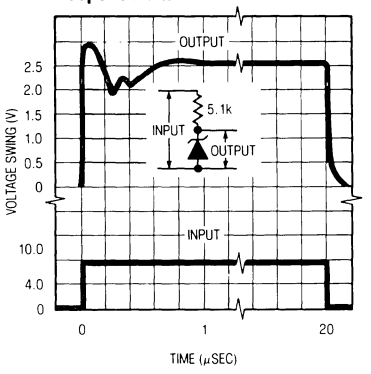
Dynamic Impedance



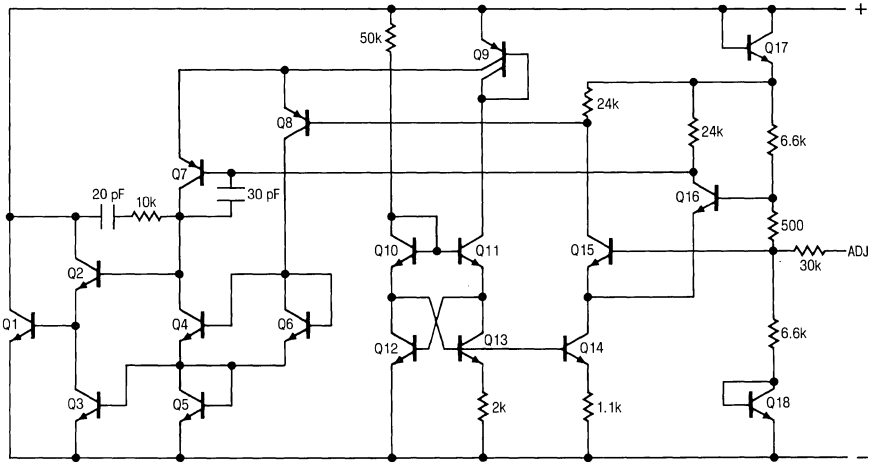
Zener Noise Voltage



Response Time

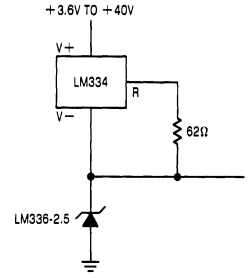


SCHEMATIC DIAGRAM

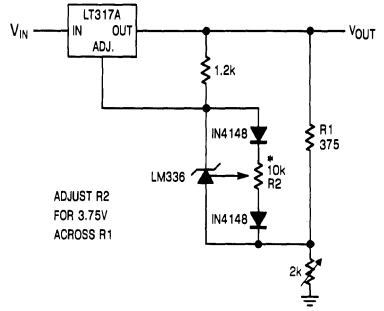


TYPICAL APPLICATIONS

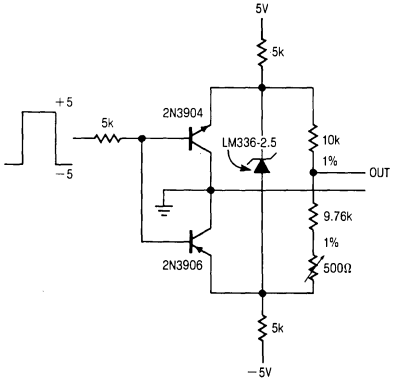
Wide Supply Range, Reference



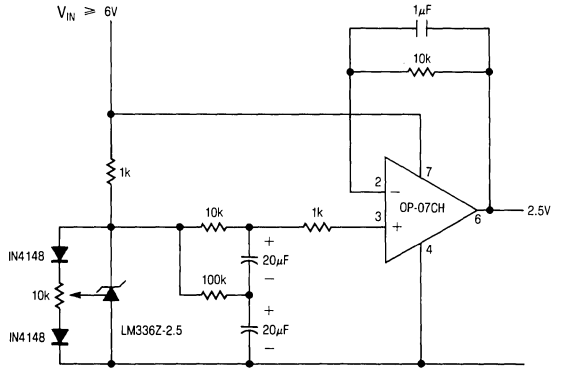
Low Temperature Coefficient Power Regulator



Switchable ±1.25V Bipolar Reference

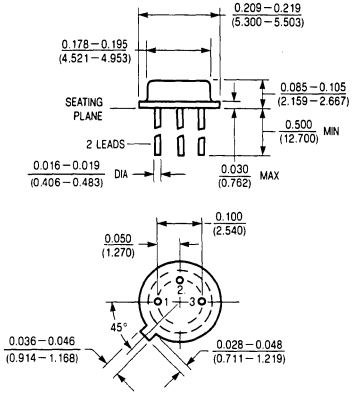


Low Noise 2.5V Buffered Reference



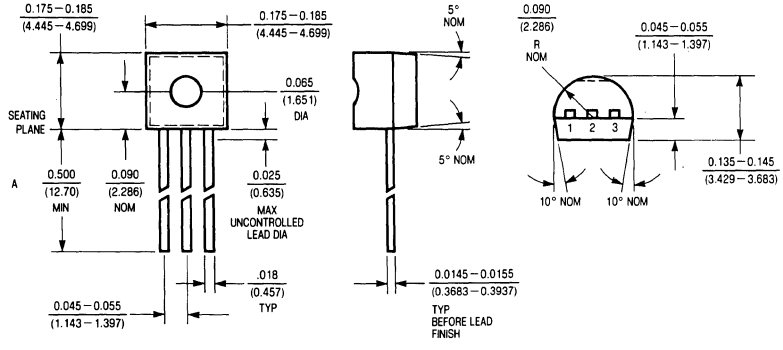
PACKAGE DESCRIPTION

H Package, 3 Lead TO-46 Metal Can



$T_j$max	Θ_{ja}	Θ_{jc}
150°C	440°C/W	80°C/W

Z Package, 3 Lead TO-92 Plastic



$T_j$max	Θ_{ja}
100°C	160°C/W

Micropower Voltage Reference

FEATURES

- 10μA to 20mA operating range
- *Guaranteed* 1% initial voltage tolerance
- *Guaranteed* 1Ω dynamic impedance
- Very low power consumption

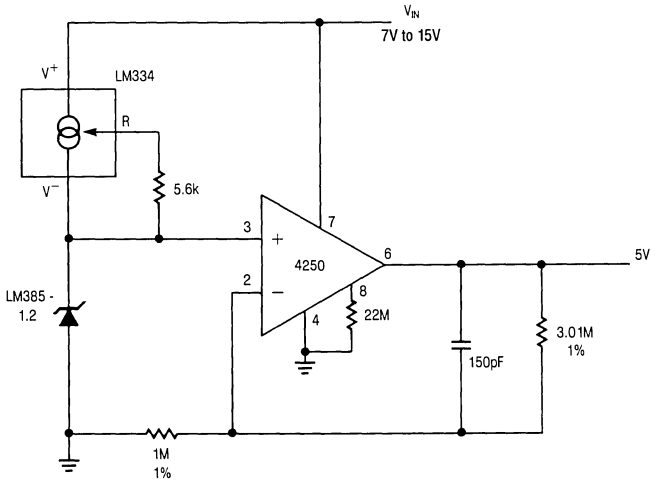
APPLICATIONS

- Portable meter references
- Portable test instruments
- Battery operated systems
- Current loop instrumentation

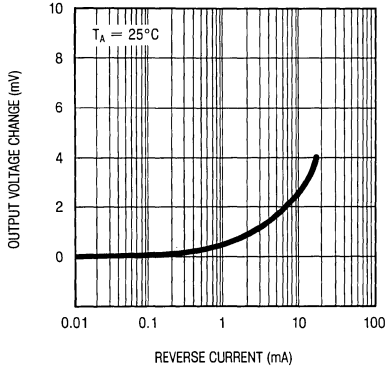
DESCRIPTION

The LM185-1.2 is a two terminal band gap reference diode that has been designed for applications which require precision performance with micropower operation. The device provides guaranteed operating specifications at currents as low as 10μA. The nominal voltage is 1.235V with both 1% and 2% tolerances available. Some additional features are: maximum dynamic impedance of 1Ω, low noise and excellent stability over time and temperature. Advanced design, processing and testing techniques make Linear's LM185-1.2 a superior choice over previous designs. A micro-power 5V reference application is shown below. For guaranteed TC, micropower references, see the LT1034 data sheet.

Micro-power 5V Reference



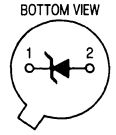
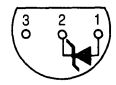
Reverse Voltage Change with Current



ABSOLUTE MAXIMUM RATINGS

Reverse Breakdown Current 30mA
Forward Current 10mA
Operating Temperature Range
LM185-1.2 ..... −55°C to 125°C
LM385-1.2 ..... 0°C to 70°C
Storage Temperature Range
LM185-1.2 ..... −65°C to 150°C
LM385-1.2 ..... −65°C to 150°C
Lead Temperature (Soldering, 10 sec.) ..... 300°C

PACKAGE/ORDER INFORMATION

	ORDER PART NUMBER
BOTTOM VIEW  H PACKAGE TO-46 METAL CAN	LM185H-1.2 LM385H-1.2 LM385BH-1.2 (NOTE 3)
BOTTOM VIEW  Z PACKAGE TO-92 PLASTIC	LM385Z-1.2 LM385BZ-1.2 (NOTE 3)

ELECTRICAL CHARACTERISTICS (See Note 1)

SYMBOL	PARAMETER	CONDITIONS		LM185-1.2 MIN	LM185-1.2 TYP	LM185-1.2 MAX	LM385-1.2/385B-1.2 MIN	LM385-1.2/385B-1.2 TYP	LM385-1.2/385B-1.2 MAX	UNITS
V_Z	Reverse Breakdown Voltage	$T_A = 25°C$, $I_{min} \leq I_R \leq 20mA$								
		LM185-1.2		1.223	1.235	1.247				V
		LM385-1.2					1.205	1.235	1.260	V
		LM385B-1.2 (Note 3)					1.223	1.235	1.247	V
$\frac{\Delta V_Z}{\Delta \text{ Temp}}$	Average Temperature Coefficient	$I_{min} \leq I_R \leq 20mA$ (Note 2 and Note 3)			20			20		ppm/°C
I_{min}	Minimum Operating Current	$T_{min} \leq T_A \leq T_{max}$	●		8	10		8	15	μA
$\frac{\Delta V_Z}{\Delta I_R}$	Reverse Breakdown Voltage Change with Current	$I_{min} \leq I_R \leq 1mA$								
		$T_A = 25°C$				1			1	mV
		$T_{min} \leq T_A \leq T_{max}$	●			1.5			1.5	mV
		$1mA \leq I_R \leq 20mA$								
		$T_A = 25°C$				10			20	mV
		$T_{min} \leq T_A \leq T_{max}$	●			20			25	mV
r_Z	Reverse Dynamic Impedance	$I_R = 100\mu A$								
		$T_A = 25°C$			0.2	0.6		0.4	1	Ω
		$T_{min} \leq T_A \leq T_{max}$	●			1.5			1.5	Ω
e_n	Wide Band Noise (RMS)	$I_R = 100\mu A$								
		$10Hz \leq f \leq 10kHz$			60			60		μV
$\frac{\Delta V_Z}{\Delta \text{ Time}}$	Long Term Stability	$I_R = 100\mu A$								
		$T_A = 25°C \pm 0.1°C$			20			20		ppm/kHr

The ● denotes the specifications which apply over full operating temperature range.

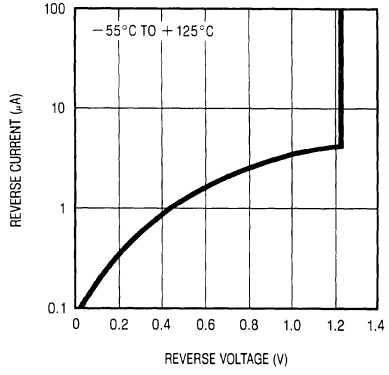
Note 1: All specifications are for $T_A = 25°C$ unless otherwise noted. For the LM185-1.2 $T_{min} = -55°C$ and $T_{max} = +125°C$. For LM385-1.2 $T_{min} = 0°C$ and $T_{max} = +70°C$.

Note 2: Selected devices with guaranteed maximum temperature coefficient are available upon request.

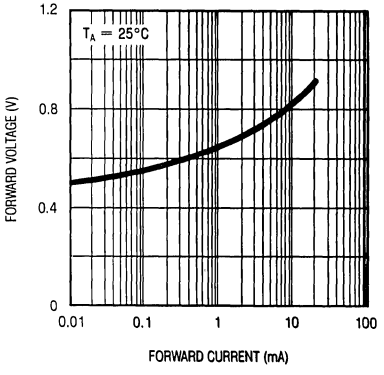
Note 3: For applications requiring low initial tolerance guaranteed over temperature consult LT1004 data sheet. The LT1004 is a low cost pin for pin substitution device

TYPICAL PERFORMANCE CHARACTERISTICS

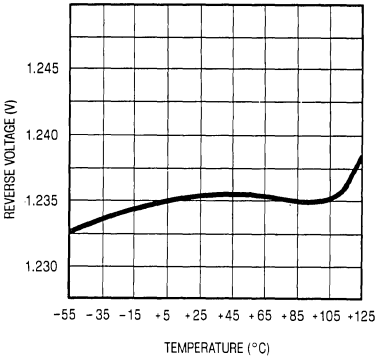
Reverse Characteristics



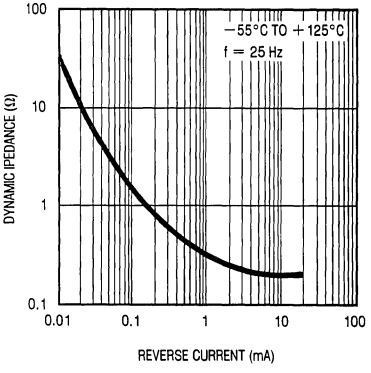
Forward Characteristics



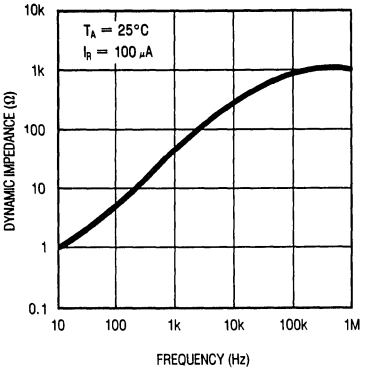
Temperature Drift



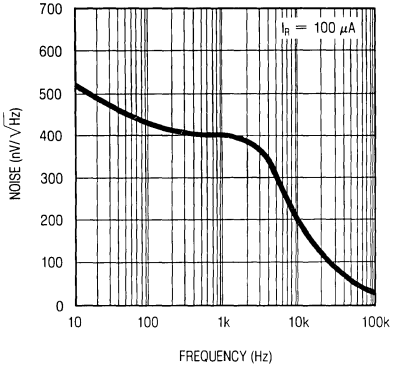
Reverse Dynamic Impedance



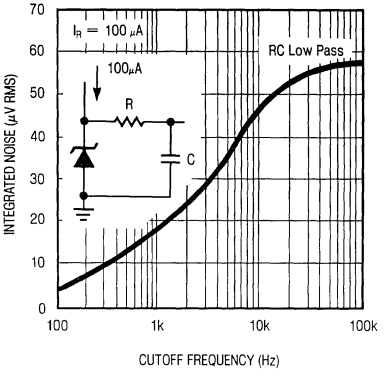
Reverse Dynamic Impedance



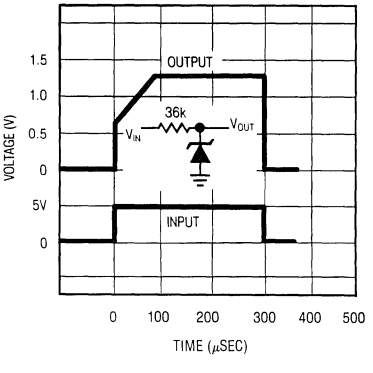
Noise Voltage



Filtered Output Noise

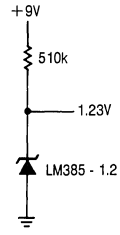


Response Time

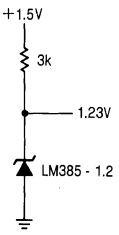


TYPICAL APPLICATIONS

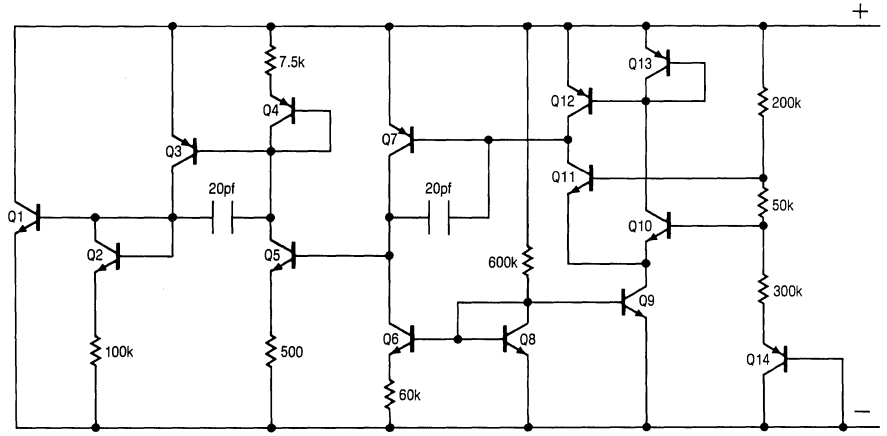
Micropower Reference for 9V Battery



1.2V Reference from 1.5V Battery

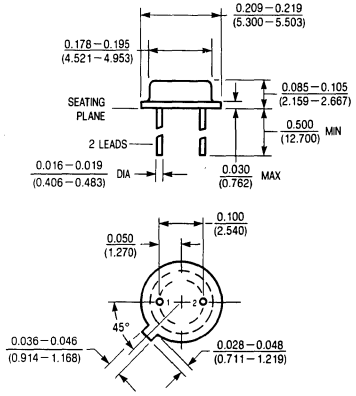


SCHEMATIC DIAGRAM



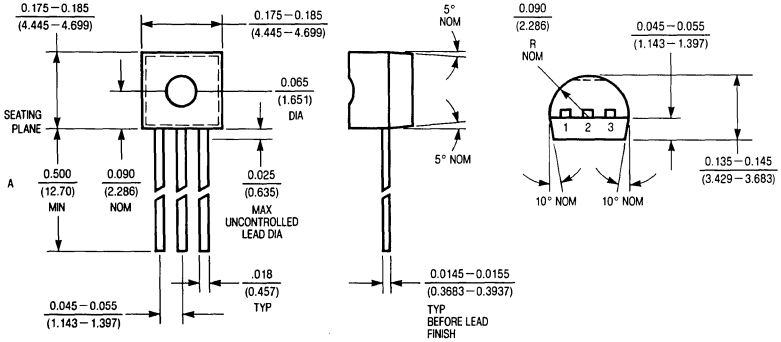
PACKAGE DESCRIPTION

H Package, 2 Lead TO-46 Metal Can



$T_j$max	Θ_{ja}	Θ_{jc}
150°C	440°C/W	80°C/W

Z Package, 3 Lead TO-92 Plastic



$T_j$max	Θ_{ja}
150°C	160°C/W

LM185-2.5/LM385-2.5
Micropower Voltage Reference

FEATURES

- 20μA to 20mA operating range
- *Guaranteed* 1% initial voltage tolerance
- *Guaranteed* 1Ω dynamic impedance
- Very low power consumption

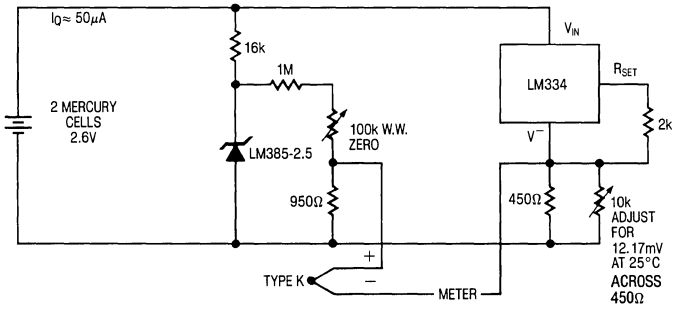
APPLICATIONS

- Portable meter references
- Portable test instruments
- Battery operated systems
- Panel meters
- Current loop instrumentation

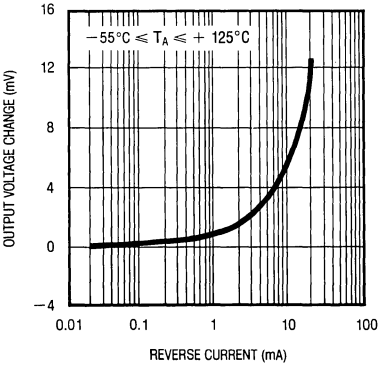
DESCRIPTION

The LM185-2.5 is a two terminal band gap reference diode that has been designed for applications which require precision performance with micropower operation. The device provides guaranteed operating specifications at currents as low as 20μA. The nominal voltage is 2.5V with both 1% and 2% tolerances available. Some additional features are: maximum dynamic impedance of 1Ω, low noise and excellent stability over time and temperature. The advanced design, processing and testing techniques make Linear's LM185-2.5 a superior choice over previous designs. A circuit for cold junction compensation of a thermocouple is show below.

Thermocouple Cold Junction Compensator



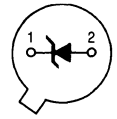
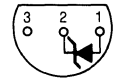
Reverse Voltage Change



ABSOLUTE MAXIMUM RATINGS

Reverse Breakdown Current..... 30mA
Forward Current..... 10mA
Operating Temperature Range
LM185-2.5..... −55°C to 125°C
LM385-2.5..... 0°C to 70°C
Storage Temperature Range
LM185-2.5..... −65°C to 150°C
LM385-2.5..... −65°C to 150°C
Lead Temperature (Soldering, 10 sec.)..... 300°C

PACKAGE/ORDER INFORMATION

	ORDER PART NUMBER
BOTTOM VIEW  H PACKAGE TO-46 METAL CAN	LM185H-2.5 LM385H-2.5 LM385BH-2.5 (NOTE 3)
BOTTOM VIEW  Z PACKAGE TO-92 PLASTIC	LM385Z-2.5 LM385BZ-2.5 (NOTE 3)

ELECTRICAL CHARACTERISTICS (See Note 1)

SYMBOL	PARAMETER	CONDITIONS		LM185-2.5 MIN	LM185-2.5 TYP	LM185-2.5 MAX	LM385-2.5/385B-2.5 MIN	LM385-2.5/385B-2.5 TYP	LM385-2.5/385B-2.5 MAX	UNITS
V_Z	Reverse Breakdown Voltage	$T_A = 25°C$, $20\mu A \leq I_R \leq 20mA$								
		LM185-2.5		2.462	2.5	2.538				V
		LM385-2.5					2.425	2.5	2.575	V
		LM385B-2.5 (Note 3)					2.462	2.5	2.538	V
$\frac{\Delta V_Z}{\Delta \text{Temp}}$	Average Temperature Coefficient	$20\mu A \leq I_R \leq 20mA$ (Note 2 and Note 3)			20			20		ppm/°C
I_{min}	Minimum Operating Current	$T_{min} \leq T_A \leq T_{max}$	●		8	20		8	20	μA
$\frac{\Delta V_Z}{\Delta I_R}$	Reverse Breakdown Voltage Change with Current	$20\mu A \leq I_R \leq 1mA$								
		$T_A = 25°C$				1			2	mV
		$T_{min} \leq T_A \leq T_{max}$	●			1.5			2.5	mV
		$1mA \leq I_R \leq 20mA$								
		$T_A = 25°C$				10			20	mV
		$T_{min} \leq T_A \leq T_{max}$	●			20			25	mV
r_Z	Reverse Dynamic Impedance	$I_R = 100\mu A$								
		$T_A = 25°C$			0.2	0.6		0.4	1	Ω
		$T_{min} \leq T_A \leq T_{max}$	●			1.5			1.5	Ω
e_n	Wide Band Noise (RMS)	$10Hz \leq f \leq 10kHz$, $I_R = 100\mu A$			120			120		μV
$\frac{\Delta V_Z}{\Delta \text{Time}}$	Long Term Stability	$T_A = 25°C \pm 0.1°C$, $I_R = 100\mu A$			20			20		ppm/kHr

The ● denotes the specifications which apply over full operating temperature range.

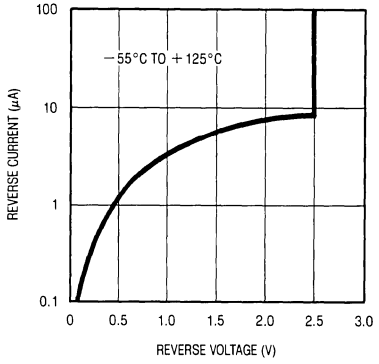
Note 1: All specifications are for $T_A = 25°C$ unless otherwise noted. For the LM185-2.5 $T_{min} = -55°C$ and $T_{max} = +125°C$. For LM385-2.5 $T_{min} = 0°C$ and $T_{max} = +70°C$.

Note 2: Selected devices with guaranteed maximum temperature coefficient are available as a special order.

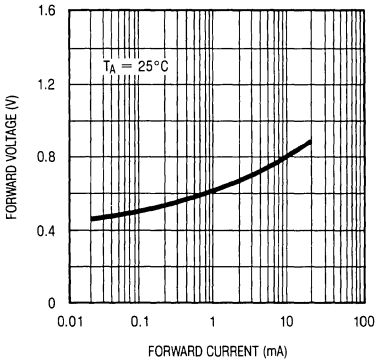
Note 3: For guaranteed TC and very low initial tolerance, consult LT1004 data sheet. The LT1004 is a low cost, pin for pin substitution device.

TYPICAL PERFORMANCE CHARACTERISTICS

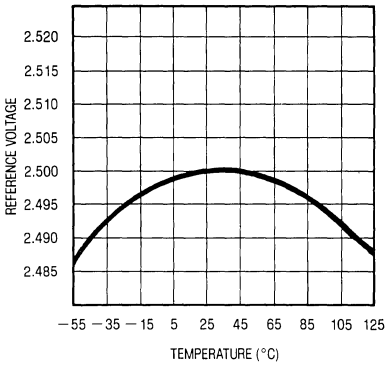
Reverse Characteristics



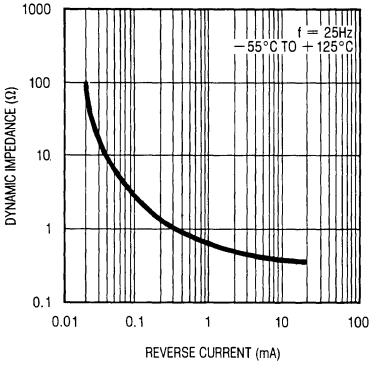
Forward Characteristics



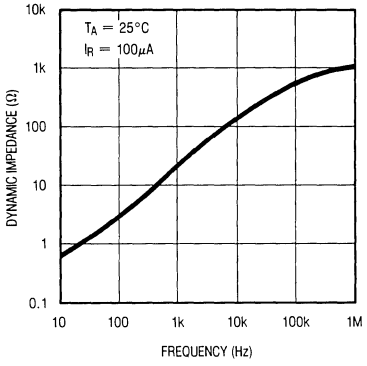
Temperature Drift



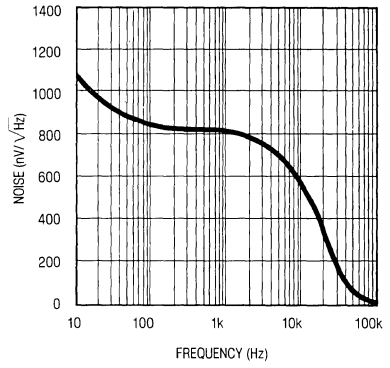
Reverse Dynamic Impedance



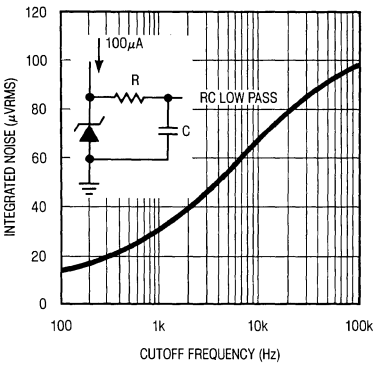
Reverse Dynamic Impedance



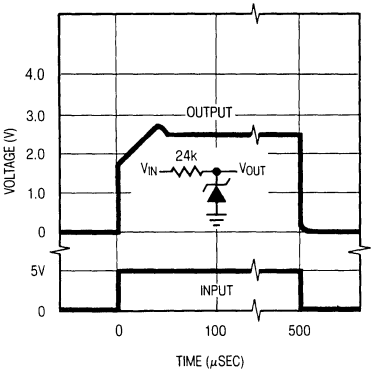
Noise Voltage



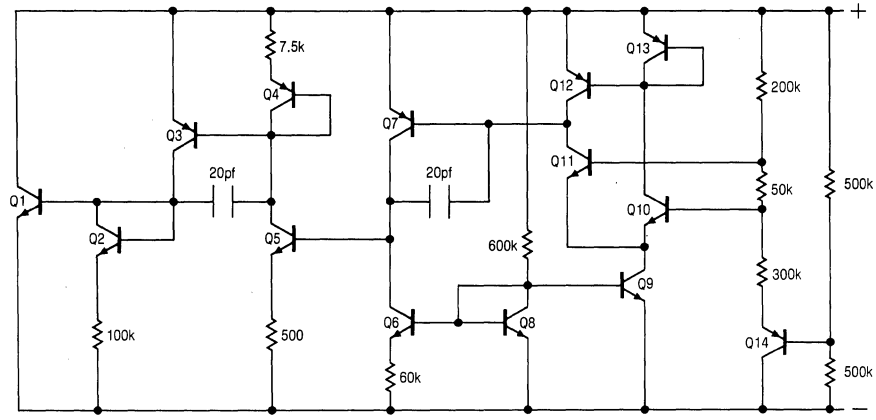
Filtered Output Noise



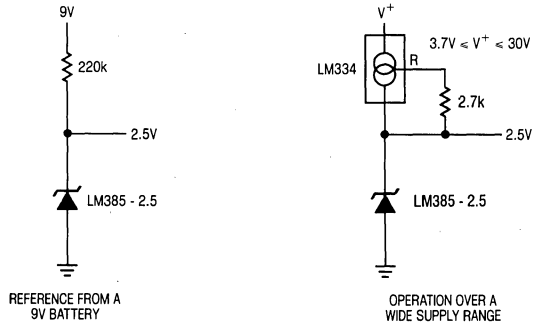
Response Time



SCHEMATIC DIAGRAM

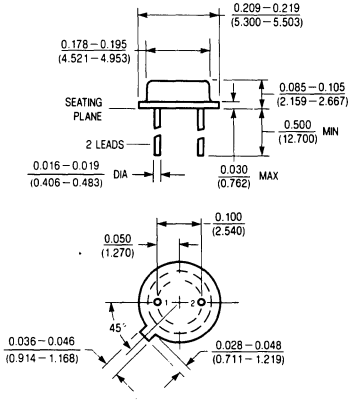


TYPICAL APPLICATIONS



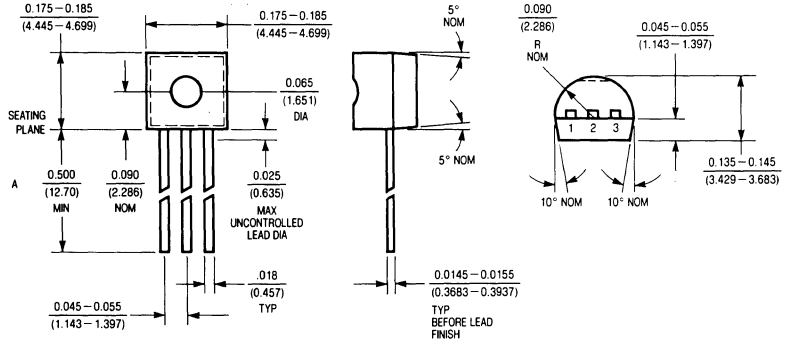
PACKAGE DESCRIPTION

H Package, 2 Lead TO-46 Metal Can



$T_j$max	Θ_{ja}	Θ_{jc}
150°C	440°C/W	80°C/W

Z Package, 3 Lead TO-92 Plastic



$T_j$max	Θ_{ja}
150°C	160°C/W

FEATURES

- *Guaranteed* 0.5 ppm/°C temperature coefficient
- *Guaranteed* 1.0 Ω *max.* dynamic impedance
- *Guaranteed* 20μV RMS *max.* noise
- *Guaranteed* initial tolerance of 2%
- Wide operating current range

APPLICATIONS

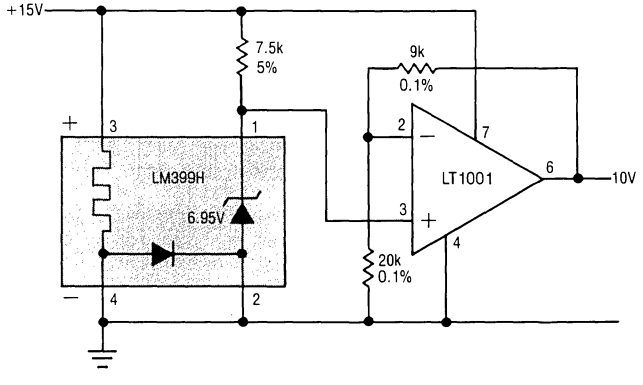
- Precision voltage reference for multimeters
- Calibration equipment voltage standards
- Laboratory measurement equipment
- Industrial monitor/control instruments
- High accuracy data converters

DESCRIPTION

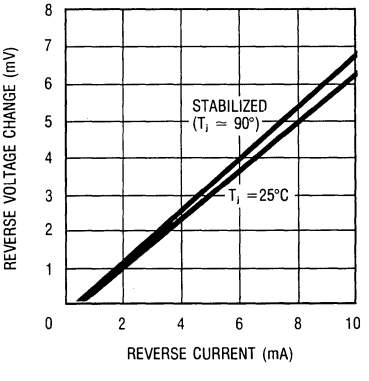
The LM199/399 precision reference features excellent temperature stability over a wide range of voltage, temperature, and operating current conditions. A stabilizing heater is incorporated with the active zener on a monolithic substrate which nearly eliminates changes in voltage with temperature. The subsurface zener operates over a current range of 0.5mA to 10mA, and offers minimal noise and excellent long term stability.

Ideal applications for the LM199/399 include digital voltmeters, precision calibration equipment, current sources and a variety of other precision low cost references. A 10 volt buffered reference application is shown below.

10 Volt Buffered Reference



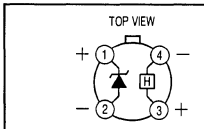
Reverse Voltage Change



ABSOLUTE MAXIMUM RATINGS

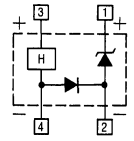
Temperature Stabilizer 40V
Reverse Breakdown Current 20mA
Forward Current 1mA
Reference to Substrate Voltage $V_{(RS)}$, (Note 1). −0.1V
Operating Temperature Range
LM199/199A ..... −55°C to 125°C
LM399/399A ..... 0°C to 70°C
Storage Temperature Range
LM199/199A ..... −65°C to 150°C
LM399/399A ..... −65°C to 150°C
Lead Temperature (Soldering, 10 sec.) ..... 300°C

PACKAGE/ORDER INFORMATION



H PKG.
TO-46 METAL CAN INSIDE THERMAL SHIELD

ORDER PART NO.
LM199H, LM199AH
LM399H, LM399AH
LM199AH-20, LM399AH-50



FUNCTIONAL BLOCK DIAGRAM

ELECTRICAL CHARACTERISTICS (See Note 2)

SYMBOL	PARAMETER	CONDITIONS		LM199/199A MIN	LM199/199A TYP	LM199/199A MAX	LM399/399A MIN	LM399/399A TYP	LM399/399A MAX	UNITS
V_Z	Reverse Breakdown Voltage	$0.5mA \leq I_R \leq 10mA$	●	6.8	6.95	7.1	6.75	6.95	7.3	V
ΔV_Z	Reverse Breakdown Voltage Change with Current	$0.5mA \leq I_R \leq 10mA$	●		6	9		6	12	mV
r_Z	Reverse Dynamic Impedance	$I_R = 1mA$	●		0.5	1		0.5	1.5	Ω
$\frac{\Delta V_Z}{\Delta \text{ Temp}}$	Temperature Coefficient LM199/LM399	$-55°C \leq T_A \leq 85°C$ $+85°C \leq T_A \leq 125°C$ $0°C \leq T_A \leq 70°C$			0.3 5	1 15		 0.3	 2	ppm/°C ppm/°C ppm/°C
	LM199A/LM399A	$-55°C \leq T_A \leq 85°C$ $+85°C \leq T_A \leq 125°C$ $0°C \leq T_A \leq 70°C$			0.2 5	0.5 10		 0.3	 1	ppm/°C ppm/°C ppm/°C
e_n	RMS Noise	$10Hz \leq f \leq 10kHz$	●		7	20		7	50	μV
$\frac{\Delta V_Z}{\Delta \text{ Time}}$	Long Term Stability	Stabilized, $22°C \leq T_A \leq 28°C$ 1000 Hours, $I_R = 1mA \pm 0.1\%$			8	Note 3		8	Note 3	ppm/$\sqrt{kH}$
I_H	Temperature Stabilizer Supply Current	$T_A = +25°C$, Still Air, $V_H = +30V$ $T_A = -55°C$ (Note 4)			8.5 22	14 28		8.5	15	mA
V_H	Temperature Stabilizer Supply Voltage		●	9		40	9		40	V
	Warm-up Time to ±0.05% V_Z	$V_H = 30V$, $T_A = 25°C$			3			3		Seconds
	Initial Turn-on Current	$9V \leq V_H \leq 40V$, $T_A = 25°C$, (See Note 4)			140	200		140	200	mA

The ● denotes the specifications which apply over full operating temperature range.

Note 1: The substrate is electrically connected to the negative terminal of the temperature stabilizer. The voltage that can be applied to either terminal of the reference is 40V more positive or 0.1V more negative than the substrate.

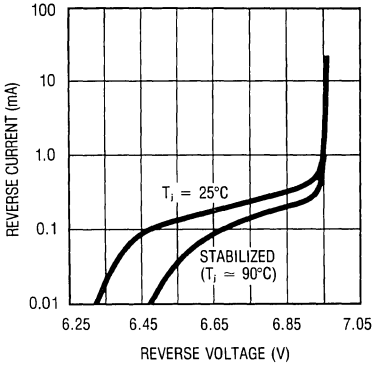
Note 2: These specifications apply for 30V applied to the temperature stabilizer and $-55°C \leq T_A \leq 125°C$ for the LM199; and $0°C \leq T_A \leq 70°C$ for the LM399.

Note 3: Devices with maximum guaranteed long term stability of 20 ppm/$\sqrt{kH}$ are available. Drift decreases with time.

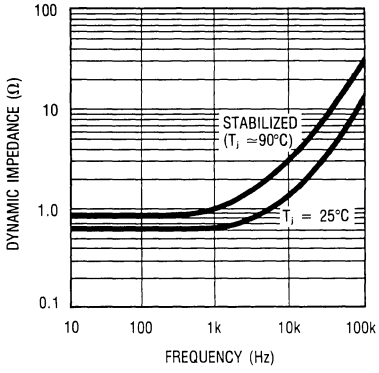
Note 4: This initial current can be reduced by adding an appropriate resistor and capacitor to the heater circuit. See the performance characteristic graphs to determine values.

TYPICAL PERFORMANCE CHARACTERISTICS

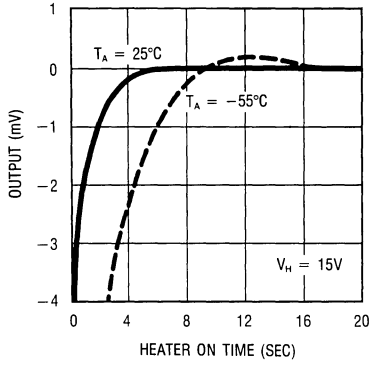
Reverse Characteristics



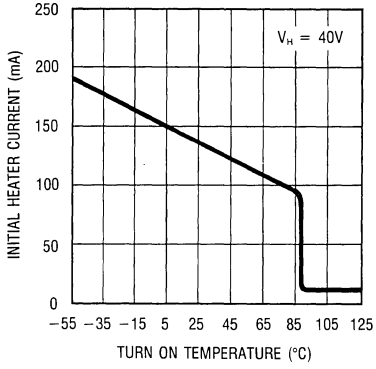
Dynamic Impedance



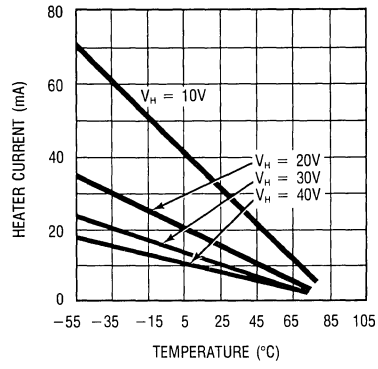
Stabilization Time



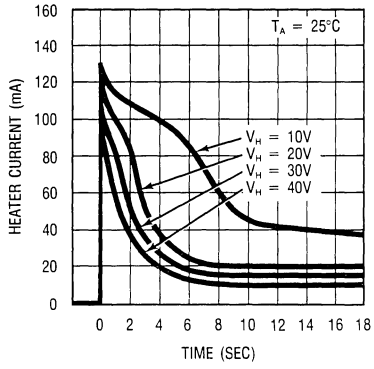
Initial Heater Current



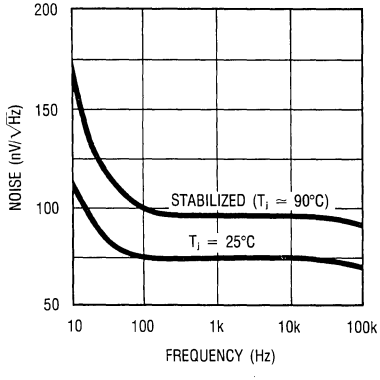
Heater Current



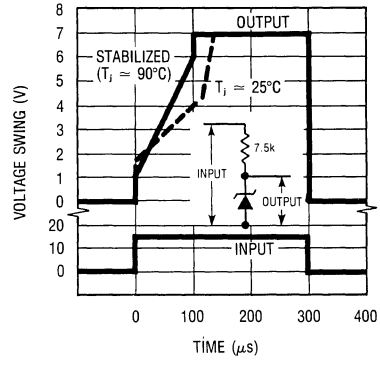
Heater Current



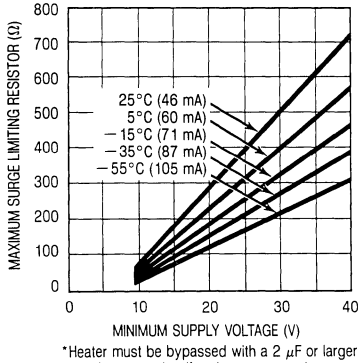
Zener Noise Voltage



Response Time



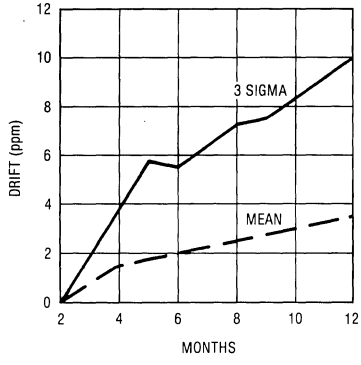
Limiting Surge Current



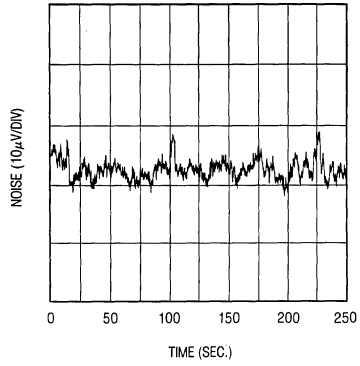
*Heater must be bypassed with a 2 μF or larger tantalum capacitor if resistors are used.

TYPICAL PERFORMANCE CHARACTERISTICS

Long Term Reference Performance
44 Units Tested

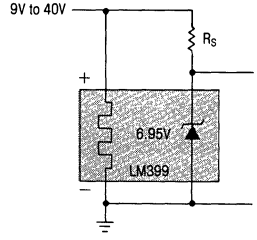


Low Frequency Noise Voltage

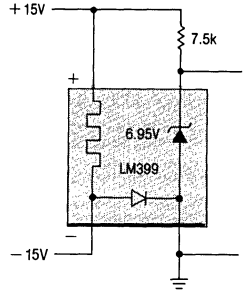


TYPICAL APPLICATIONS

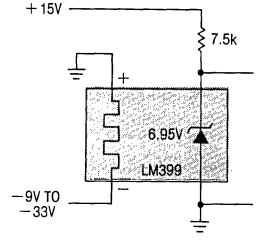
Single Supply Operation



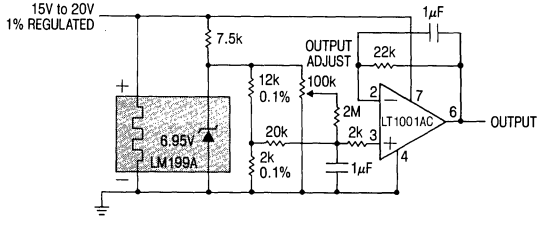
Split Supply Operation



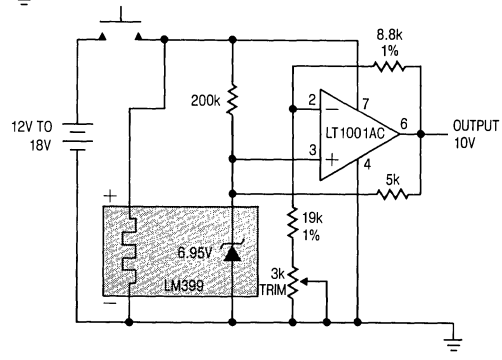
Negative Heater Supply with Positive Reference



Standard Cell Replacement

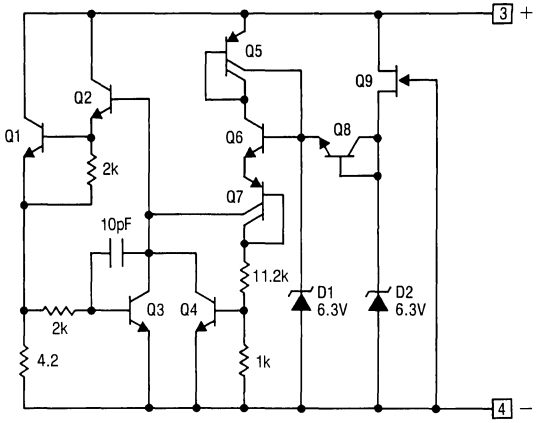


Portable Calibrator

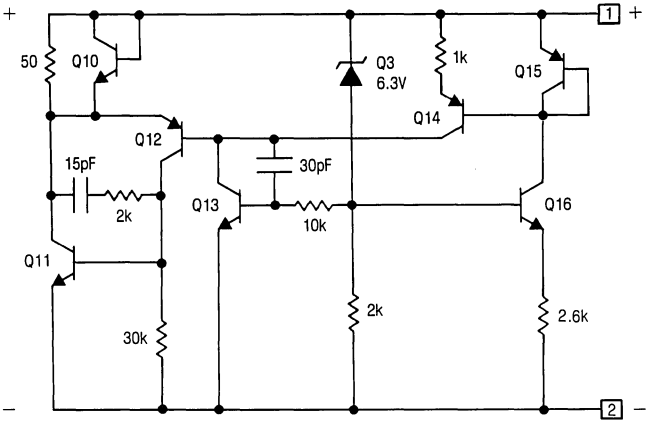


SCHEMATIC DIAGRAMS

Temperature Stabilizer

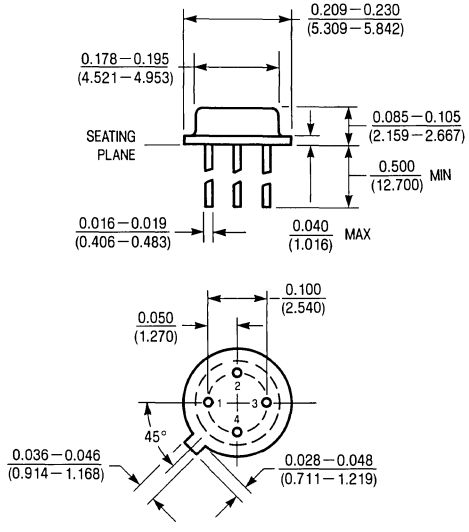


Reference

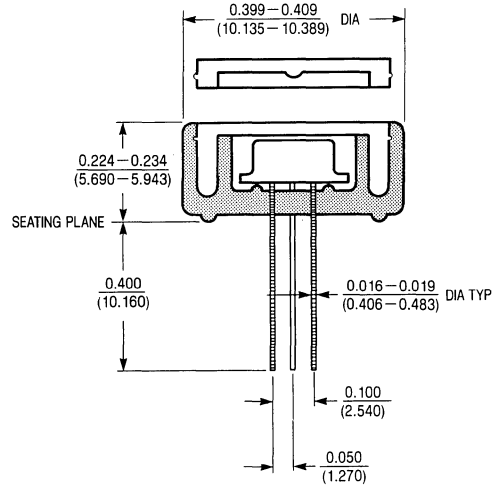


PACKAGE DESCRIPTION

H Package, 4 Lead TO-46 Metal Can



Thermal Shield* For TO-46, H Package



*Thermal Shield Material is Valox™
Valox is a registered trademark of General Electric

FEATURES

- Trimmed Output ±0.3%
- Low Drift—5ppm/°C Typical
- Low Noise—3ppm (p-p)
- High Line Rejection
- Temperature Output—REF-02
- Low Supply Current 1.4mA Max.

APPLICATIONS

- A to D and D to A Converters
- Precision Regulators
- Constant Current Sources
- V to F Converters
- Bridge Excitation

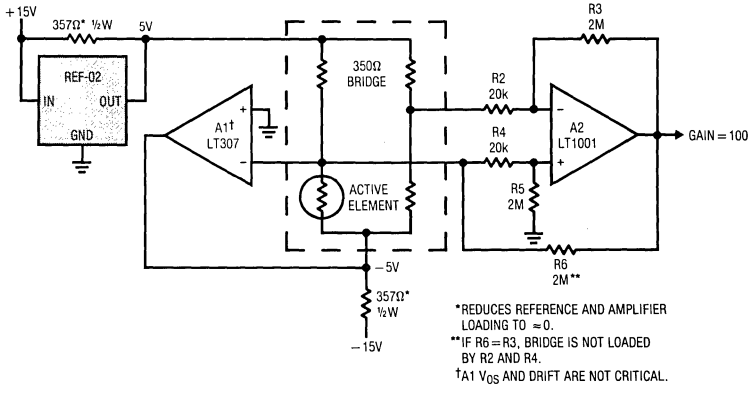
DESCRIPTION

The REF-01/REF-02 are precision 10V and 5V bandgap references which provide stable output voltages over a wide range of operating conditions. Output voltage is accurate to ±0.3% with a low 5ppm/°C typical temperature coefficient. The REF-01 and REF-02 are excellent choices for applications where low drift, moderate accuracy, low power consumption and low cost are considerations.

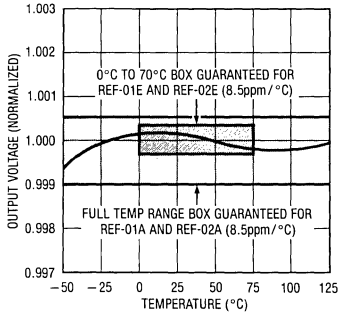
The REF-02 includes a temperature output pin which provides a linear voltage proportional to absolute temperature.

For lower drift and higher accuracy references, please see the LT1019 and LT1021 data sheets.

Ultra Linear Strain Gauge Amplifier



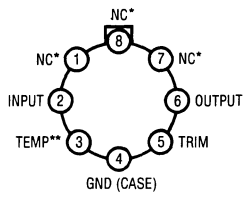
Output Voltage Temperature Drift



ABSOLUTE MAXIMUM RATINGS

REF-01/02, A, E, H 40V
REF-01C/02C 30V
Power Dissipation 500mW
Output Short Circuit Duration
  To Ground ..... Indefinite
  To $V_{IN} \leq 16V$ ..... Indefinite
  To $V_{IN} > 16V$ ..... Not Allowed
Storage Temperature ..... −65°C to 150°C
Operating Temperature
  REF-01/02, REF-01A/02A ..... −55°C to 125°C
  REF-01E/02E, REF-01H/02H,
  REF-01C/02C, REF-01D/02D ..... 0°C to 70°C

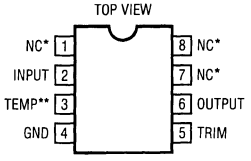
PACKAGE/ORDER INFORMATION



METAL CAN H PACKAGE

*INTERNALLY CONNECTED. DO NOT CONNECT EXTERNALLY.
**DO NOT CONNECT ON REF-01.

ORDER PART NUMBER	
REF-01AH	REF-02AH
REF-01H	REF-02H
REF-01EH	REF-02EH
REF-01HH	REF-02HH
REF-01CH	REF-02CH
	REF-02DH



PLASTIC DIP N8 PACKAGE
8 PIN HERMETIC DIP
*INTERNALLY CONNECTED. DO NOT CONNECT EXTERNALLY.
**DO NOT CONNECT ON REF-01.

ORDER PART NUMBER	
REF-01EJ8	REF-02EJ8
REF-01HJ8	REF-02HJ8
REF-01CJ8	REF-02CJ8
REF-01EN8	REF-02DJ8
REF-01HN8	REF-02EN8
REF-01CN8	REF-02HN8
	REF-02CN8
	REF-02DN8

ELECTRICAL CHARACTERISTICS

$V_{IN} = +15V$, $T_A = 25°C$ unless otherwise noted

SYMBOL	PARAMETER	CONDITIONS		REF-01A/E REF-02A/E MIN	TYP	MAX	REF-01/H REF-02/H MIN	TYP	MAX	UNITS
V_O	Output Voltage	$I_L = 0$	REF-01	9.97	10.00	10.03	9.95	10.00	10.05	V
			REF-02	4.985	5.000	5.015	4.975	5.000	5.025	V
	Output Adjustment Range	$R_p = 10k\Omega$	REF-01	±3.0	+5, −27	—	±3.0	+5, −27	—	%
			REF-02	±3.0	+5, −13	—	±3.0	+5, −13	—	%
e_{np-p}	Output Voltage Noise	0.1Hz to 10Hz (Note 6)	REF-01	—	20	—	—	20	—	μVp-p
			REF-02	—	10	—	—	10	—	μVp-p
V_{IN}	Input Voltage Range		REF-01	12	—	40	12	—	40	V
			REF-02	7	—	40	7	—	40	V
$\frac{\Delta V_{OUT}}{\Delta V_{IN}}$	Line Regulation (Note 1)	$(V_{OUT} + 3V) \leq V_{IN} \leq 33V$		—	0.0001	0.010	—	0.0001	0.010	%/V
$\frac{\Delta V_{OUT}}{\Delta I_{OUT}}$	Load Regulation (Note 1)	$I_L = 0mA$ to 10mA	REF-01	—	0.0005	0.008	—	0.0005	0.010	%/mA
			REF-02	—	0.0010	0.010	—	0.001	0.010	%/mA
I_Q	Quiescent Supply Current	No Load		—	0.65	1.4	—	0.65	1.4	mA
I_{OUT}	Load Current			10	20	—	10	20	—	mA
	Sink Current			−0.3	−20	—	−0.3	−20	—	mA
I_{SC}	Short Circuit Current	$V_O = 0$		—	25	—	—	25	—	mA
V_T	Temperature Voltage Output	(Note 2)	REF-02 Only	—	620	—	—	620	—	mV

ELECTRICAL CHARACTERISTICS

$V_{IN} = +15V$, $T_A = 25°C$ unless otherwise noted

SYMBOL	PARAMETER	CONDITIONS		REF-01C REF-02C MIN	REF-01C REF-02C TYP	REF-01C REF-02C MAX	REF-02D MIN	REF-02D TYP	REF-02D MAX	UNITS
V_O	Output Voltage	$I_L = 0mA$	REF-01	9.90	10.00	10.10				V
			REF-02	4.950	5.000	5.050	4.900	5.000	5.100	V
	Output Adjustment Range	$R_P = 10k\Omega$	REF-01		+5, −27	—	—	—	—	%
			REF-02	±2.7	+5, −13	—	±2.0	+5, −13	—	%
e_{np-p}	Output Voltage Noise	0.1Hz to 10Hz (Note 6)	REF-01		30	—				μVp-p
			REF-02	—	12	—	—	12	—	μVp-p
$\frac{\Delta V_{OUT}}{\Delta V_{IN}}$	Line Regulation (Note 1)	$(V_{OUT} + 3V) \leq V_{IN} \leq 33V$		—	0.0001	0.015	—	0.0001	0.04	%/V
$\frac{\Delta V_{OUT}}{\Delta I_{OUT}}$	Load Regulation (Note 1)	$I_L = 0mA$ to $8mA$		—	0.0005	0.015	—	—	—	%/mA
		$I_L = 0mA$ to $4mA$		—	—	—	—	0.001	0.04	%/mA
I_Q	Quiescent Supply Current	No Load		—	0.65	1.6	—	0.65	2.0	mA
I_{OUT}	Load Current			8	20	—	8	20	—	mA
	Sink Current			−0.2	20	—	−0.2	20	—	mA
I_{SC}	Short Circuit Current	$V_O = 0$		—	25	—	—	25	—	mA
V_T	Temperature Voltage Output	(Note 2)	REF-02 Only	—	620	—	—	620	—	mV

ELECTRICAL CHARACTERISTICS

$V_{IN} = +15V$, $-55°C \leq T_A \leq +125°C$ for REF-01A/02A and REF-01/REF-02, $0°C \leq T_A \leq +70°C$ for REF-01E/02E and REF-01H/02H, $I_L = 0mA$ unless otherwise noted

SYMBOL	PARAMETER	CONDITIONS		REF-01A/E REF-02A/E MIN	REF-01A/E REF-02A/E TYP	REF-01A/E REF-02A/E MAX	REF-01/H REF-02/H MIN	REF-01/H REF-02/H TYP	REF-01/H REF-02/H MAX	UNITS
$\frac{\Delta V}{\Delta T}$	Output Voltage Change with Temperature (Notes 3 and 4)	$0°C \leq T_A \leq +70°C$	●	—	0.02	0.06	—	0.035	0.17	%
		$-55°C \leq T_A \leq +125°C$	●	—	0.09	0.15	—	0.144	0.45	%
TC	Output Voltage Temperature Coefficient	(Note 5)	●	—	5	8.5	—	8	25	ppm/°C
	Change in V_O Temperature Coefficient with Output Adjustment	$R_P = 10k\Omega$	●	—	0.5	—	—	0.5	—	ppm/%
$\frac{\Delta V_{OUT}}{\Delta V_{IN}}$	Line Regulation ($V_{IN} = 8V$ to $33V$) (Note 1)	$0°C \leq T_A \leq +70°C$	●	—	0.0001	0.012	—	0.0001	0.012	%/V
		$-55°C \leq T_A \leq +125°C$	●	—	0.0001	0.015	—	0.0001	0.015	%/V
$\frac{\Delta V_{OUT}}{\Delta I_{OUT}}$	Load Regulation ($I_L = 0mA$ to $8mA$) (Note 1)	$0°C \leq T_A \leq +70°C$	●	—	0.002	0.010	—	0.002	0.012	%/mA
		$-55°C \leq T_A \leq +125°C$	●	—	0.002	0.012	—	0.002	0.015	%/mA
	Temperature Voltage Output Temperature Coefficient	(Note 2) REF-02	●	—	2.1	—	—	2.1	—	mV/°C

The ● denotes the specifications which apply over the full operating temperature range.

ELECTRICAL CHARACTERISTICS

$V_{IN} = +15V$, $0°C \le T_A \le +70°C$ and $I_L = 0mA$ unless otherwise noted

SYMBOL	PARAMETER	CONDITIONS		REF-01C REF-02C MIN	REF-01C REF-02C TYP	REF-01C REF-02C MAX	REF-02D MIN	REF-02D TYP	REF-02D MAX	UNITS
$\frac{\Delta V}{\Delta T}$	Output Voltage Change with Temperature	(Notes 3 and 4)	●	—		0.45	—		1.7	%
TC	Output Voltage Temperature Coefficient	(Note 5)	●	—	8	65	—	8	250	ppm/°C
	Change in V_O Temperature Coefficient with Output Adjustment	$R_p = 10k\Omega$	●	—	0.5	—	—	0.5	—	ppm/%
$\frac{\Delta V_{OUT}}{\Delta V_{IN}}$	Line Regulation (Note 1)	$V_{IN} = 8V$ to $30V$	●	—	0.0001	0.018	—	0.0001	0.05	%/V
$\frac{\Delta V_{OUT}}{\Delta I_{OUT}}$	Load Regulation (Note 1)	$I_L = 0mA$ to $5mA$	●	—	0.002	0.018	—	0.002	0.05	%/mA
	Temperature Voltage Output Temperature Coefficient	(Note 2) REF-02	●	—	2.1	—	—	2.1	—	mV/°C

Note 1: Line and load regulation specifications include the effect of self heating.

Note 2: Limit current in or out of pin 3 to 50nA and capacitance on pin 3 to 30pF.

Note 3: ΔV is defined as the absolute difference between the maximum output voltage and the minimum output voltage over the specified temperature range expressed as a percentage of nominal output.

$$\Delta V = \left| \frac{V_{MAX} - V_{MIN}}{V_{OUT}} \right| \times 100$$

Note 4: ΔV specification applies trimmed or untrimmed.

Note 5: TC is defined as ΔV divided by the temperature range, i.e.,

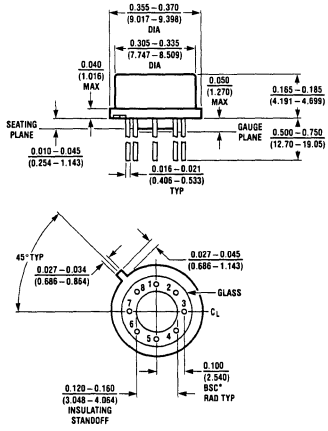
$$TC = \frac{\Delta V}{T_{MAX} - T_{MIN}}$$

Note 6: 0.1Hz to 10Hz noise cannot be 100% tested on modern high speed test equipment, so Linear Technology does not put a guaranteed maximum specification on this parameter for standard units. 100% bench testing of 0.1Hz to 10Hz noise is available on special request. To ensure low output noise, Linear Technology *does* 100% test 10Hz to 1kHz noise. Consult factory for details.

PACKAGE DESCRIPTION

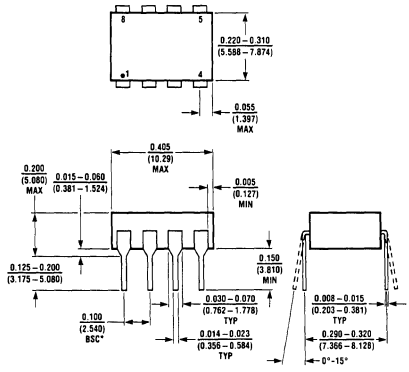
Dimensions in inches (millimeters) unless otherwise noted.

H Package
Metal Can



$T_j$max	θ_{ja}	θ_{jc}
150°C	150°C/W	45°C/W

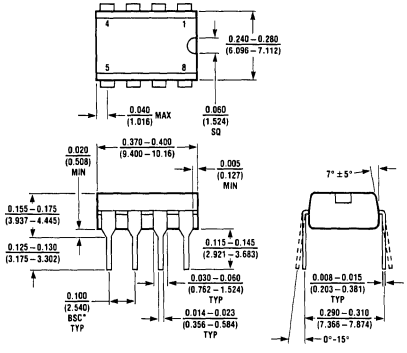
J8 Package
8 Lead Hermetic DIP



*LEADS WITHIN 0.007 OF TRUE POSITION (TP) AT GAUGE PLANE

$T_j$max	θ_{ja}
150°C	100°C/W

N8 Package
8 Lead Plastic



*LEADS WITHIN 0.007 OF TRUE POSITION (TP) AT GAUGE PLANE

$T_j$max	θ_{ja}
100°C	130°C/W

SECTION 5—COMPARATORS

SECTION 5—COMPARATORS

MILITARY

Part Number	Response Time Max (ns)	V_{OS} Max (mV)	I_B Max (nA)	Drive Capability (mA)	Gain Min (V/mV)	I_{SUPPLY} Positive (mA)	I_{SUPPLY} Negative (mA)	Packages Available	Important Features
LT1011AM	250	0.5	25	50	200	4.0	2.5	H, J8	Low V_{OS}, Low I_B, High Output Drive, 12 Bit Acc.
LT1011M	250	1.5	50	50	200	4.0	2.5	H, J8	
LT1016M	12	±2.5	10000	10	2	35	5	H, J8	Ultra High Speed, TTL Outputs, True Output Latch, Stable In Active Region, Pin/Pin Replacement for AM686.
LT1017M	—	1	15	30	1000	0.060	—	H, J8	LT1017 Has Lowest Supply Current, LT1018 is Faster. Both are Dual Comparators with Same Pin-Out as 193 Types.
LT1018M	—	1	75	35	1000	0.250	—	H, J8	
LT111A	250	1.0	100	50	200	4.0	2.5	H, J8	Low V_{OS}, High Gain
LM111	—	3.0	100	50	40	6.0	5.0	H, J8	Gen. Purpose
LT119A	80 (typ)	1.0	500	25	20	11.5	4.5	H, J	Dual, Low V_{OS}, Hi CMRR
LM119	80 (typ)	4.0	500	25	10	11.5	4.5	H, J	Dual, Gen. Purp.
LTC1040M	100μs	0.5	3	*	∞	300nA**	1nA	J	CMOS Sampling Comparator

COMMERCIAL

Part Number	Response Time Max (ns)	V_{OS} Max (mV)	I_B Max (nA)	Drive Capability (mA)	Gain Min (V/mV)	I_{SUPPLY} Positive (mA)	I_{SUPPLY} Negative (mA)	Packages Available	Important Features
LT1011AC	250	0.5	25	50	200	4.0	2.5	H, J8, N8	Low V_{OS}, Low I_B, High Output Drive, 12 Bit Acc.
LT1011C	250	0.5	50	50	200	4.0	2.5	H, J8, N8	
LT1016C	12	±2.5	10000	10	2	35	5	H, J8	Ultra High Speed, TTL Outputs, True Output Latch, Stable In Active Region, Pin/Pin Replacement for AM686.
LT1017C	—	1	15	30	1000	0.060	—	H	LT1017 Has Lowest Supply Current, LT1018 is Faster. Both are Dual Comparators with Same Pin-Out as 193 Types.
LT1018C	—	1	75	35	1000	0.250	—	H	
LT311A	250	1.0	100	50	200	4.0	2.5	H, J8	Low V_{OS}, High Gain
LM311	—	7.5	250	50	40	7.5	5.0	H, J8	Gen. Purpose
LT319A	80 (typ)	1.0	500	25	20	12.5	5.0	H, J, N	Dual, Low V_{OS}, Hi CMRR
LM319	80 (typ)	8.0	1000	25	8	12.5	5.0	H, J, N	Dual, Gen. Purp.
LTC1040C	100μs	0.5	3	*	∞	300nA**	1nA	J	CMOS Sampling Comparator

*1 Std. TTL Load **Supply Current Depends on Clock Rate

Voltage Comparator

FEATURES

- Pin-Compatible with LM111 Series Devices
- *Guaranteed* Max. 0.5mV Input Offset Voltage
- *Guaranteed* Max. 25nA Input Bias Current
- *Guaranteed* Max. 3nA Input Offset Current
- *Guaranteed* Max. 250ns Response Time
- *Guaranteed* Min. 200,000 Voltage Gain
- 50mA Output Current Source or Sink
- ±30V Differential Input Voltage
- Fully Specified for Single +5V Operation

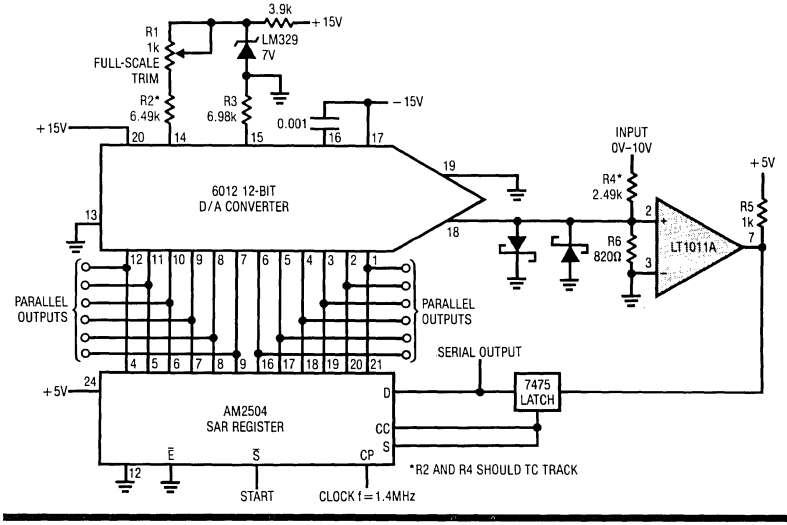
APPLICATIONS

- SAR A to D Converters
- Voltage to Frequency Converters
- Precision R/C Oscillator
- Peak Detector
- Motor Speed Control
- Pulse Generator
- Relay/Lamp Driver

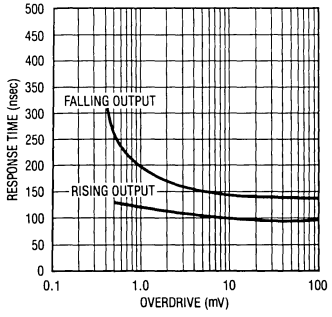
DESCRIPTION

The LT1011 is a general purpose comparator with significantly better input characteristics than the LM111. Although pin-compatible with the LM111, it offers four times lower bias current, six times lower offset voltage, and five times higher voltage gain. Offset voltage drift—a previously unspecified parameter—is guaranteed at 15μV/°C. Additionally, the supply current is lower by a factor of two with no loss in speed. The LT1011 is several times faster than the LM111 when subjected to large overdrive conditions. It is also fully specified for DC parameters and response time when operating on a single +5V supply. These parametric improvements allow the LT1011 to be used in high accuracy (≥12-bit) systems without trimming. In a 12-bit A to D application, for instance, using a 2mA DAC, the offset error introduced by the LT1011 is less than 1/2 LSB. The LT1011 retains all the versatile features of the LM111, including single 3V to ±18V supply operation, and a floating transistor output with 50mA source/sink capability. It can drive loads referenced to ground, negative supply or positive supply, and is specified up to 50V between V^- and the collector output. A differential input voltage up to the full supply voltage is allowed, even with ±18V supplies, enabling the inputs to be clamped to the supplies with simple diode clamps.

10μs 12-Bit A-D Converter



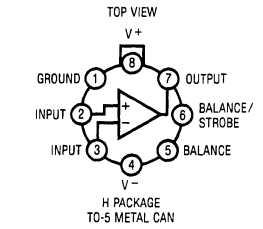
Response Time vs Overdrive



ABSOLUTE MAXIMUM RATINGS

Supply Voltage (pin 8 to pin 4) 36V
Output to Negative Supply (pin 7 to pin 4)
LT1011AM, LT1011M 50V
LT1011AC, LT1011C 40V
Ground to Negative Supply
(pin 1 to pin 4) 30V
Differential Input Voltage ..... ±36V
Voltage at Strobe Pin (pin 6 to pin 8) 5V
Input Voltage (Note 1) ..... Equal to Supplies
Output Short Circuit Duration ..... 10 sec.
Operating Temperature Range (Note 2)
LT1011AM/LT1011M ..... −55°C to 125°C
LT1011AC/LT1011C ..... 0°C to 70°C
Storage Temperature Range ..... −65°C to 150°C
Lead Temperature (Soldering, 10 sec.) ..... 300°C

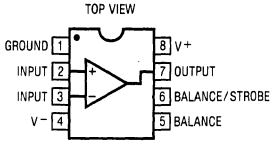
PACKAGE/ORDER INFORMATION



H PACKAGE
TO-5 METAL CAN

ORDER PART NUMBER

LT1011AMH
LT1011MH
LT1011ACH
LT1011CH



NOTE: PIN 4 CONNECTED TO CASE.

J8 PACKAGE 8 PIN CERDIP
N8 PACKAGE 8 PIN PLASTIC

LT1011AMJ8
LT1011MJ8
LT1011ACJ8
LT1011CJ8
LT1011ACN8
LT1011CN8

ELECTRICAL CHARACTERISTICS

$V_S = \pm 15V$, $V_{CM} = 0V$, $R_S = 0$, $T_J = 25°C$, $V_I = -15V$, output at pin 7 unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		LT1011AM/LT1011AC MIN	LT1011AM/LT1011AC TYP	LT1011AM/LT1011AC MAX	LT1011M/LT1011C MIN	LT1011M/LT1011C TYP	LT1011M/LT1011C MAX	UNITS
V_{OS}	Input Offset Voltage	Note 3			0.3	0.5		0.6	1.5	mV
			●			1.0			3.0	mV
V_{OS}	*Input Offset Voltage	$R_S \leq 50k\Omega$ (Note 4)				0.75			2.0	mV
			●			1.5			3.0	mV
I_{OS}	*Input Offset Current	Note 4			0.2	3		0.2	4	nA
			●			5			6	nA
I_b	Input Bias Current	Note 3			15	25		20	50	nA
I_b	*Input Bias Current	Note 4			20	35		25	65	nA
			●			50			80	nA
$\frac{\Delta V_{OS}}{\Delta T}$	Input Offset Voltage Drift (Note 5)	$T_{MIN} \leq T \leq T_{MAX}$	●		4	15		4	25	μV/°C
A_{VOL}	*Large Signal Voltage Gain	$R_L = 1k\Omega$ to $+15V$, $-10V \leq V_{OUT} \leq 14.5V$		200	500		200	500		V/mV
		$R_L = 500\Omega$ to $+5V$, $0.5V \leq V_{OUT} \leq 4.5V$		50	300		50	300		V/mV
CMRR	Common-Mode Rejection Ratio			94	115		90	115		dB
	*Input Voltage Range (Note 8)	$V_S = \pm 15V$	●	−14.5		13	−14.5		13	V
		V_S = Single +5V	●	0.5		3.0	0.5		3.0	V
T_d	*Response Time	Note 6			150	250		150	250	ns
V_{OL}	*Output Saturation Voltage	$V_{IN} = 5$ mV, $I_{SINK} = 8$mA	●		0.25	0.4		0.25	0.4	V
		$V_I = 0$, $I_{SINK} = 50$ mA	●		0.7	1.5		0.7	1.5	V
	*Output Leakage Current	$V_{IN} = 5$mV, $V1 = -15V$			0.2	10		0.2	10	nA
		$V_{OUT} = 35V$ (25V for LT1011C)	●			500			500	nA
	*Positive Supply Current				3.2	4.0		3.2	4.0	mA
	*Negative Supply Current				1.7	2.5		1.7	2.5	mA
	*Strobe Current	Minimum to Ensure Output Transistor is Off		500			500			μA
	Input Capacitance				6			6		pF

*indicates parameters which are guaranteed for all supply voltages, including a single 5V supply. See Note 4.

The ● denotes the specifications which apply over the full operating temperature range.

Note 1: Inputs may be clamped to supplies with diodes so that maximum input voltage actually exceeds supply voltage by one diode drop. See Input Protection in applications section.

Note 2: T_J max = 150°C for the LT1011AM/LT1011M and 95°C for the LT1011AC/LT1011C.

Note 3: Output is sinking 1.5mA with $V_{OUT} = 0V$.

Note 4: These specifications apply for all supply voltages from a single +5V to ±15V, the entire input voltage range, and for both high and low output states. The high state is $I_{SINK} \geq 100\mu A$, $V_{OUT} \geq (V^+ - 1V)$ and the low state is $I_{SINK} \leq 8mA$, $V_{OUT} \leq 0.8V$. Therefore, this specification defines a worst-case error band that includes effects due to common-mode signals, voltage gain, and output load.

Note 5: Drift is calculated by dividing the offset voltage difference measured at min and max temperatures by the temperature difference.

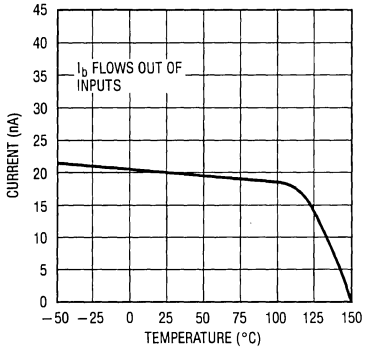
Note 6: Response time is measured with a 100mV step and 5mV overdrive. The output load is a 500Ω resistor tied to +5V. Time measurement is taken when the output crosses 1.4V.

Note 7: Do not short the strobe pin to ground. It should be current driven at 3mA to 5mA for the shortest strobe time. Currents as low as 500μA will strobe the LT111A if speed is not important. External leakage on the strobe pin in excess of 0.2μA when the strobe is "off" can cause offset voltage shifts.

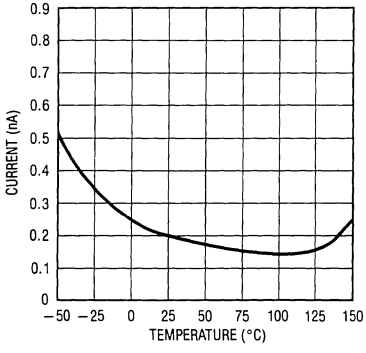
Note 8: See graph, Input Offset Voltage vs Common-Mode Voltage.

TYPICAL PERFORMANCE CHARACTERISTICS

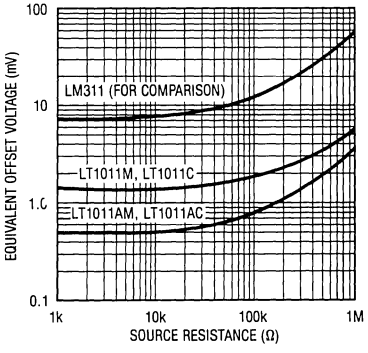
Input Bias Current



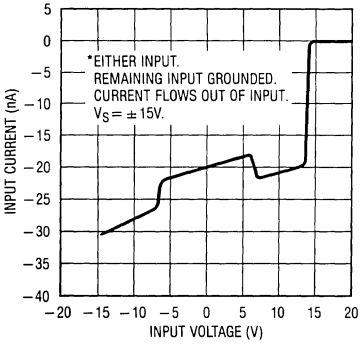
Input Offset Current



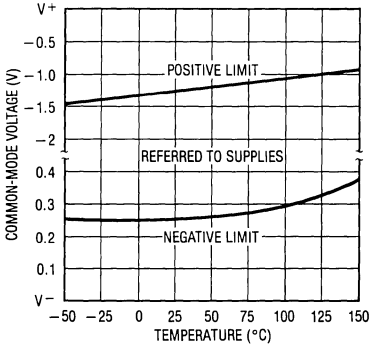
Worst-Case Offset Error



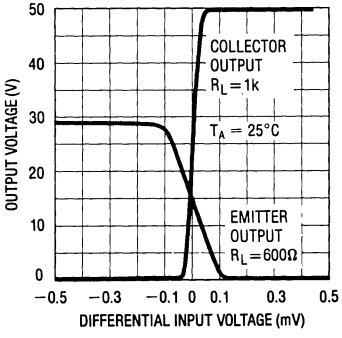
Input Characteristics*



Common-Mode Limits

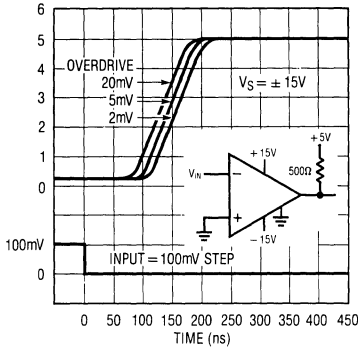


Transfer Function (Gain)

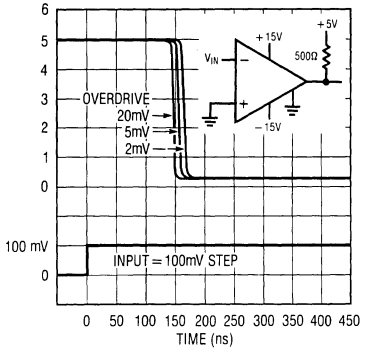


TYPICAL PERFORMANCE CHARACTERISTICS

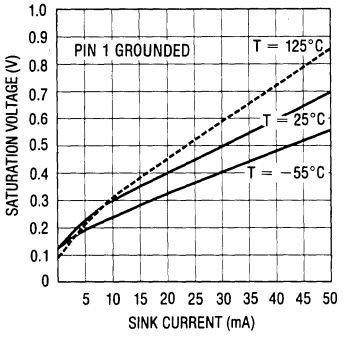
Response Time—Collector Output



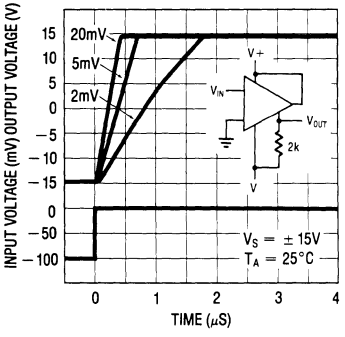
Response Time—Collector Output



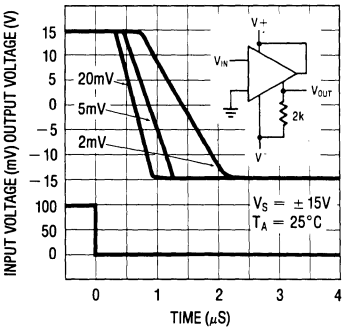
Collector Output Saturation Voltage



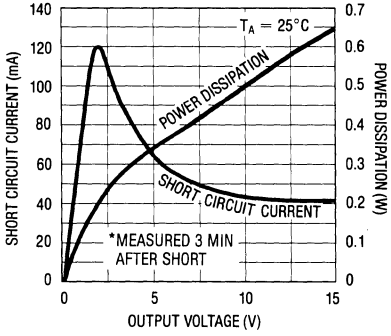
Response Time Using GND Pin as Output



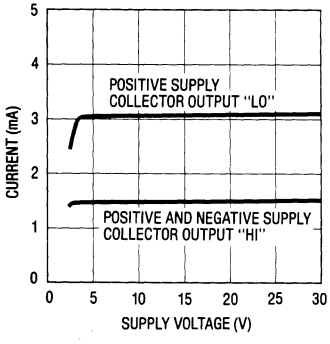
Response Time Using GND Pin as Output



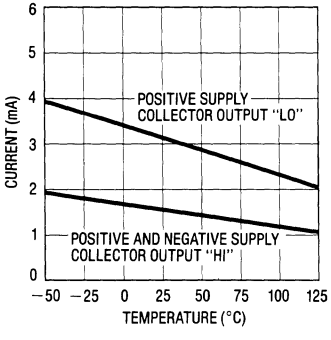
Output Limiting Characteristics*



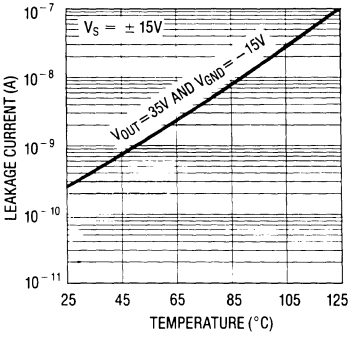
Supply Current vs Supply Voltage



Supply Current vs Temperature

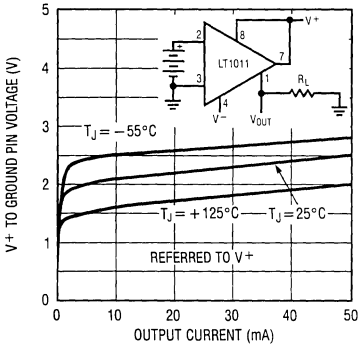


Output Leakage Current

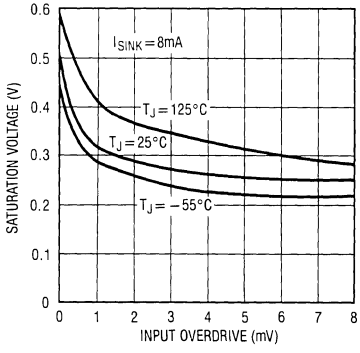


TYPICAL PERFORMANCE CHARACTERISTICS

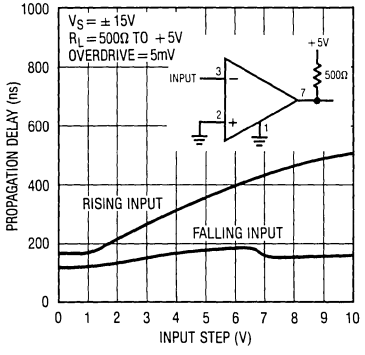
Output Saturation—Ground Output



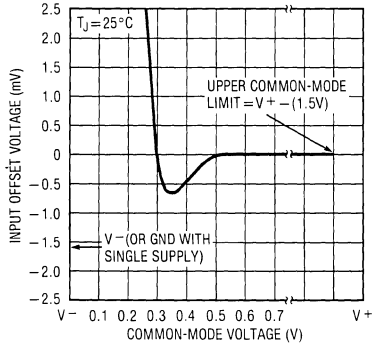
Output Saturation Voltage



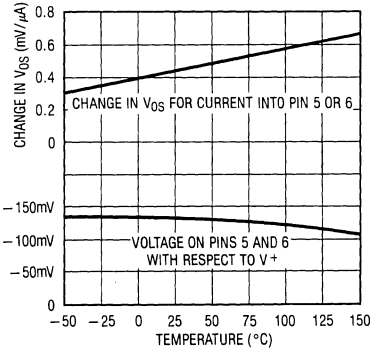
Response Time vs Input Step Size



Input Offset Voltage vs Common-Mode Voltage



Offset Pin Characteristics



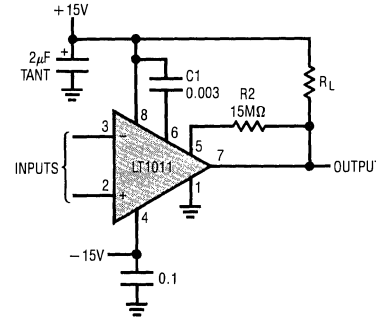
APPLICATIONS INFORMATION

Preventing Oscillation Problems

Oscillation problems in comparators are nearly always caused by stray capacitance between the output and inputs or between the output and other sensitive pins on the comparator. This is especially true with high gain-bandwidth comparators like the LT1011, which are designed for fast switching with millivolt input signal levels. The gain-bandwidth product of the LT1011 is over 10GHz. Oscillation problems tend to occur at frequencies around 5MHz, where the LT1011 has a gain of ≈2000. This implies that attenuation of output signals must be at least 2000:1 at 5MHz as measured at the inputs. If the source impedance is 1kΩ, the effective stray capacitance between output and input must have a reactance of more than (2000) (1kΩ) = 2MΩ, or less than 0.02pF. The actual interlead capacitance between input and output pins on the LT1011 is less than 0.002pF when cut to printed circuit mount length. Additional stray capacitance due to printed circuit traces must be minimized by routing the output trace directly away from input lines and, if possible, running ground traces next to input traces to provide shielding. Additional steps to ensure oscillation-free operation are:

1. Bypass the strobe/balance pins with a 0.01μF capacitor connected from pin 5 to pin 6. This eliminates stray capacitive feedback from the output to the balance pins, which are nearly as sensitive as the inputs.
2. Bypass the negative supply (pin 4) with a 0.1μF ceramic capacitor close to the comparator. 0.1μF can also be used for the positive supply (pin 8) if the pull-up load is tied to a separate supply. When the pull-up load is tied directly to pin 8, use a 2μF solid tantalum bypass capacitor.
3. Bypass any slow moving or DC input with a capacitor (≥0.01μF) close to the comparator to reduce high frequency source impedance.
4. Keep resistive source impedance as low as possible. If a resistor is added in series with one input to balance source impedances for DC accuracy, bypass it with a capacitor. The low input bias current of the LT1011 usually eliminates any need for source resistance balancing. A 5kΩ imbalance, for instance, will create only 0.25mV DC offset.
5. Use hysteresis. This consists of shifting the input offset voltage of the comparator when the output changes state. Hysteresis forces the comparator to move quickly through its linear region, eliminating oscillations by "overdriving" the comparator under all input conditions. Hysteresis may be either AC or DC. AC techniques do not shift the apparent offset voltage of the comparator, but require a *minimum* input signal slew rate to be effective. DC hysteresis works for all input slew rates, but creates a shift in offset voltage dependent on the previous condition of the input signal. The circuit shown below is an excellent compromise between AC and DC hysteresis.

Comparator with Hysteresis

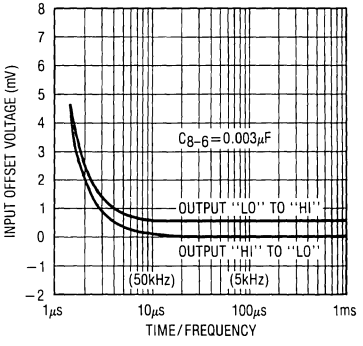


This circuit is especially useful for general purpose comparator applications because it does not force any signals directly back onto the input signal source. Instead, it takes advantage of the unique properties of the balance pins to provide extremely fast, clean output switching even with low frequency input signals in the millivolt range. The 0.003μF capacitor from pin 6 to pin 8 generates AC hysteresis because the voltage on the balance pins shifts slightly, depending on the state of the output. Both pins move about 4mV. If one pin (6) is bypassed, AC hysteresis is created. It is only a few millivolts referred to the inputs, but is sufficient to switch the output at nearly the maximum speed of which the comparator is capable. To prevent

APPLICATIONS INFORMATION

problems from low values of input slew rate, a slight amount of DC hysteresis is also used. The sensitivity of the balance pins to current is about 0.5mV input referred offset for each microampere of balance pin current. The 15mΩ resistor tied from output to pin 5 generates 0.5mV DC hysteresis. The combination of AC and DC hysteresis creates clean oscillation-free switching with very small input errors. The curve below plots input referred error versus switching frequency for the circuit as shown.

Input Offset Voltage vs Time to Last Transition

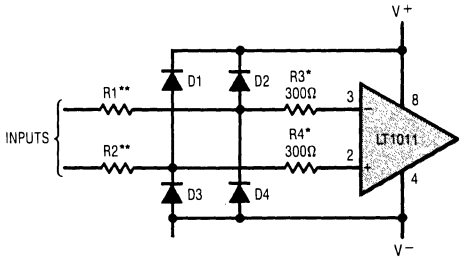


Note that at low frequencies, the error is simply the DC hysteresis, while at high frequencies, an additional error is created by the AC hysteresis. The high frequency error can be reduced by reducing C_H, but lower values may not provide clean switching with very low slew rate input signals.

Input Protection

The inputs to the LT1011 are particularly suited to general purpose comparator applications because large differential and/or common-mode voltages can be tolerated without damage to the comparator. Either or both inputs can be raised 40V above the negative supply, *independent of the positive supply voltage.* Internal forward biased diodes will conduct when the inputs are taken below the negative supply. In this condition, input current must be limited to 1mA. If very large (fault) input voltages must be accommodated, series resistors and clamp diodes should be used (see drawing below).

Limiting Fault Input Currents



D1–D4 1N4148
*MAY BE ELIMINATED FOR $I_{FAULT} \leq 1mA$
**SELECT ACCORDING TO ALLOWABLE FAULT CURRENT AND POWER DISSIPATION

The input resistors should limit fault current to a reasonable value (0.1mA to 20mA). Power dissipation in the resistors must be considered for continuous faults, especially when the LT1011 supplies are off. And one final caution: lightly loaded supplies may be forced to higher voltages by large fault currents flowing through D1–D4.

R3 and R4 limit input current to the LT1011 to less than 1mA when the input signals are held below V^-. They may be eliminated if R1 and R2 are large enough to limit fault current to less than 1mA.

Input Slew Rate Limitations

The response time of a comparator is typically measured with a 100mV step and a 5mV–10mV overdrive. Unfortunately, this does not simulate many real-world situations where the step size is typically much larger and overdrive can be significantly less. In the case of the LT1011, step size is important because the slew rate of internal nodes will limit response time for input step sizes larger than 1V. At 5V step size, for instance, response time increases from 150ns to 360ns. See the curve labeled Response Time vs Input Step Size for more detail.

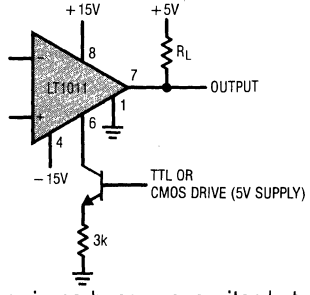
APPLICATIONS INFORMATION

If response time is critical and large input signals are expected, clamp diodes across the inputs are recommended. The slew rate limitation can also affect performance when differential input voltage is low, but both inputs must slew quickly. Maximum suggested common-mode slew rate is $10V/\mu s$.

Strobing

The LT1011 can be strobed by pulling current out of the strobe pin. The output transistor is forced to an "off" state, giving a "hi" output at the collector (pin 7). Currents as low as $250\mu A$ will cause strobing, but at low strobe currents strobe delay will be 200ns–300ns. If strobe current is increased to 3mA, strobe delay drops to about 60ns. The voltage at the strobe pin is about 150mV below V^+ at zero strobe current and about 2V below V^+ for 3mA strobe current. *Do not ground the strobe pin. It must be current driven.* The drawing below shows a typical strobe circuit.

Typical Strobe Circuit



Note that there is no bypass capacitor between pins 5 and 6. This maximizes strobe speed, but leaves the comparator more sensitive to oscillation problems for slow, low level inputs. A 1pF capacitor between the output and pin 5 will greatly reduce oscillation problems without reducing strobe speed.

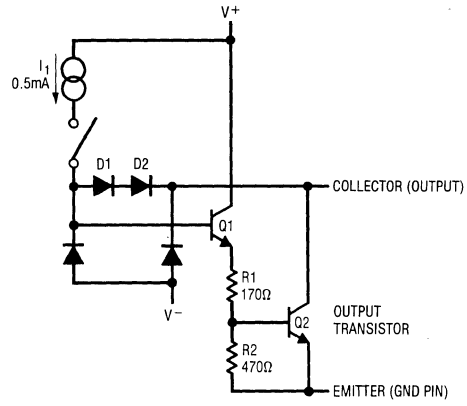
DC hysteresis can also be added by placing a resistor from output to pin 5. See step number 5 under "Preventing Oscillation Problems".

The pin (6) used for strobing is also one of the offset adjust pins. Current flow into or out of pin 6 must be kept very low ($<0.2\mu A$) when not strobing to prevent input offset voltage shifts.

Output Transistor

The LT1011 output transistor is truly floating in the sense that no current flows into or out of either the collector or emitter when the transistor is in the "off" state. The equivalent circuit is shown in the drawing below.

Output Transistor Circuitry



In the "off" state, I_1 is switched off and both Q1 and Q2 turn off. The collector of Q2 can be now held at any voltage above V^- without conducting current, including voltages above the positive supply level. Maximum voltage above V^- is 50V for the LT1011 and 40V for the LT1011C. The emitter can be held at any voltage between V^+ and V^- as long as it is negative with respect to the collector.

In the "on" state, I_1 is connected, turning on Q1 and Q2. Diodes D1 and D2 prevent deep saturation of Q2 to improve speed and also limit the drive current of Q1. The R1/R2 divider sets the saturation voltage of Q2 and provides turn-off drive. Either the collector or emitter pin can be held at a voltage between V^+ and V^-. This allows the remaining pin to drive the load. In typical applications, the emitter is connected to V^- or ground and the collector drives a load tied to V^+ or a separate positive supply.

APPLICATIONS INFORMATION

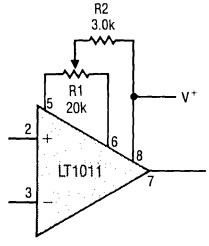
When the emitter is used as the output, the collector is typically tied to V^+ and the load is connected to ground or V^-. Note that the emitter output is phase reversed with respect to the collector output so that the "+" and "–" input designations must be reversed. When the collector is tied to V^+, the voltage at the emitter in the "on" state is about 2V below V^+ (see curves).

Input Signal Range

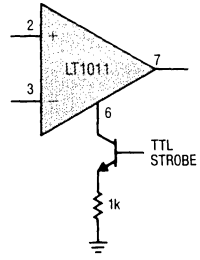
The common-mode input voltage range of the LT1011 is about 300mV above the negative supply and 1.5V below the positive supply, independent of the actual supply voltages (see curve in typical performance characteristics). This is the voltage range over which the output will respond correctly when the common-mode voltage is applied to one input and a higher or lower signal is applied to the remaining input. *If one input is inside the common-mode range and one is outside, the output will be correct. If the inputs are outside the common-mode range in opposite directions, the output will still be correct. If both inputs are outside the common-mode range in the same direction, the output will not respond to the differential input; it will remain unconditionally high* (collector output).

TYPICAL APPLICATIONS

Offset Balancing

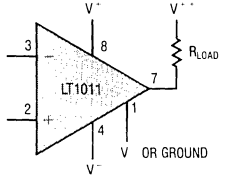


Strobing



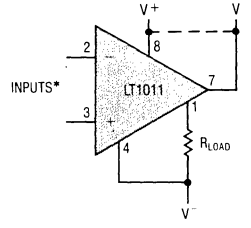
NOTE: DO NOT GROUND STROBE PIN.

Driving Load Referenced to Positive Supply



V^{++} CAN BE GREATER OR LESS THAN V^+

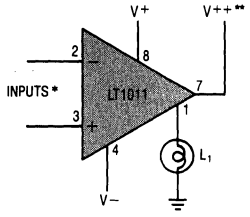
Driving Load Referenced to Negative Supply



* INPUT POLARITY IS REVERSED WHEN USING PIN 1 AS OUTPUT

TYPICAL APPLICATIONS

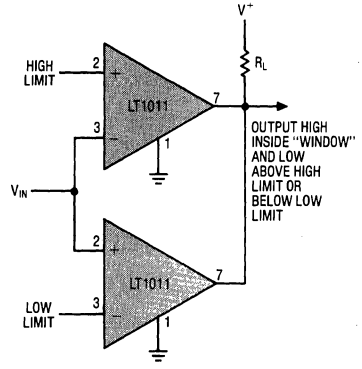
Driving Ground Referred Load



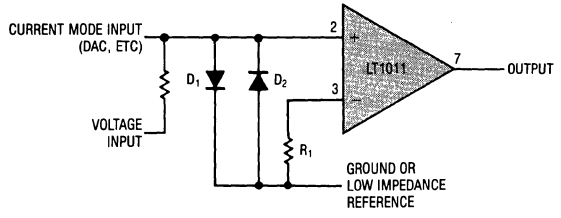
* INPUT POLARITY IS REVERSED WHEN USING PIN 1 AS OUTPUT

**V++ MAY BE ANY VOLTAGE ABOVE V–. PIN 1 SWINGS TO WITHIN ≈2V OF V++.

Window Detector

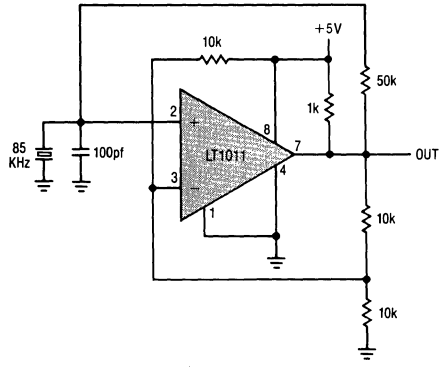


Using Clamp Diodes to Improve Frequency Response*



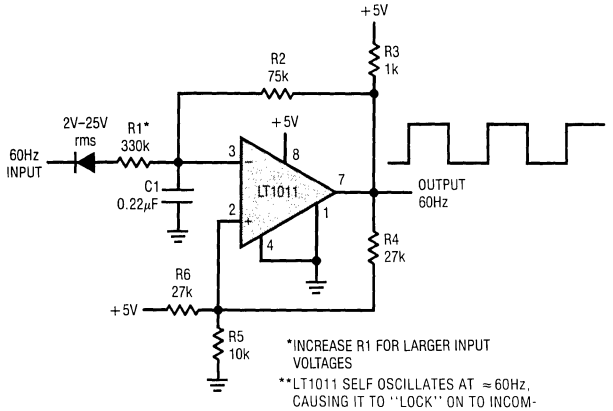
*SEE CURVE, "RESPONSE TIME VS INPUT STEP SIZE"

Crystal Oscillator



TYPICAL APPLICATIONS

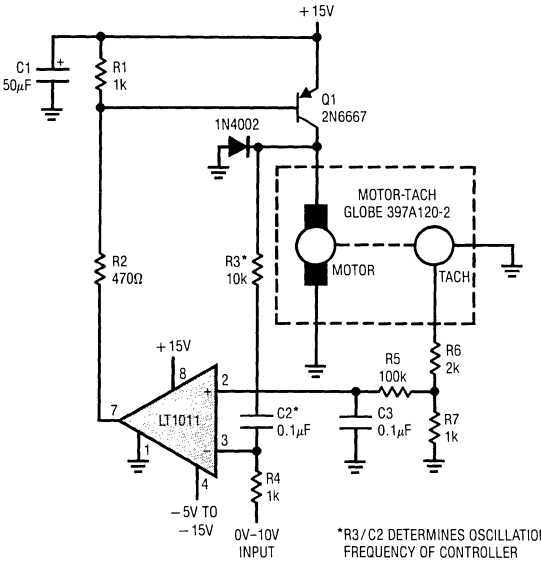
Noise Immune 60Hz Line Sync**



*INCREASE R1 FOR LARGER INPUT VOLTAGES

**LT1011 SELF OSCILLATES AT ≈60Hz, CAUSING IT TO "LOCK" ON TO INCOMING LINE SIGNAL.

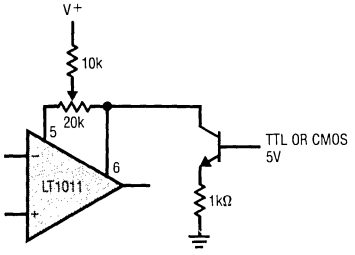
High Efficiency**Motor Speed Controller



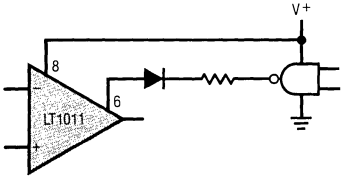
*R3/C2 DETERMINES OSCILLATION FREQUENCY OF CONTROLLER

**Q1 OPERATES IN SWITCH MODE

Combining Offset Adjust and Strobe

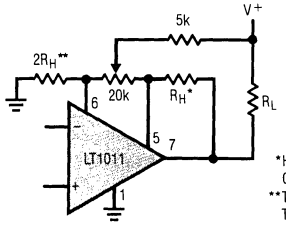


Direct Strobe Drive when CMOS* Logic Uses Same V+ Supply as LT1011



*NOT APPLICABLE FOR TTL LOGIC

Combining Offset Adjustment and Hysteresis

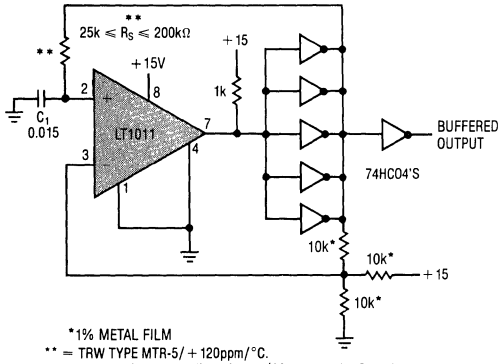


*HYSTERESIS IS ≈0.45mV/μA OF CURRENT CHANGE IN R_H

**THIS RESISTOR CAUSES HYSTERESIS TO BE CENTERED AROUND V_{OS}

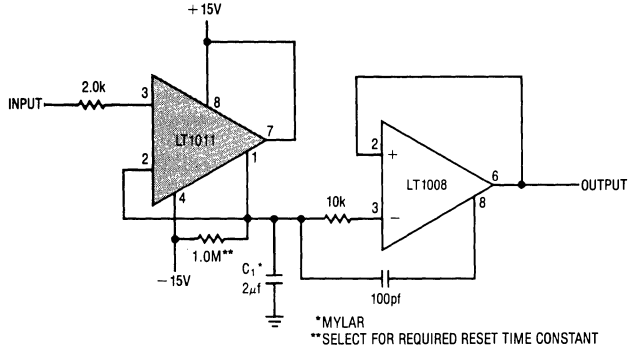
TYPICAL APPLICATIONS

Low Drift R/C Oscillator†



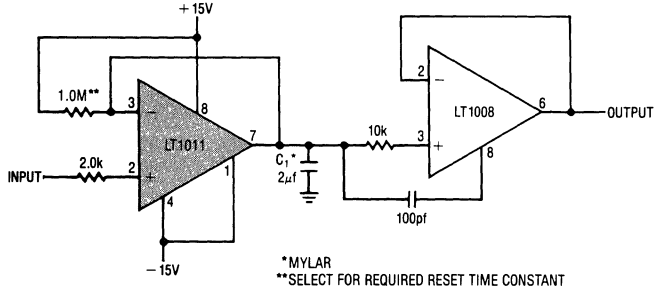
*1% METAL FILM
** = TRW TYPE MTR-5/+120ppm/°C.
C_1 = .015 = POLYSTYRENE −120ppm/°C ±30ppm WESCO TYPE 32-P
NOTE: COMPARATOR CONTRIBUTES ≤ 10ppm/°C DRIFT FOR FREQUENCIES BELOW 10kHz.
†LOW DRIFT AND ACCURATE FREQUENCY ARE OBTAINED BECAUSE THIS CONFIGURATION REJECTS EFFECTS DUE TO INPUT OFFSET VOLTAGE AND BIAS CURRENT OF THE COMPARATOR.

Positive Peak Detector



*MYLAR
**SELECT FOR REQUIRED RESET TIME CONSTANT

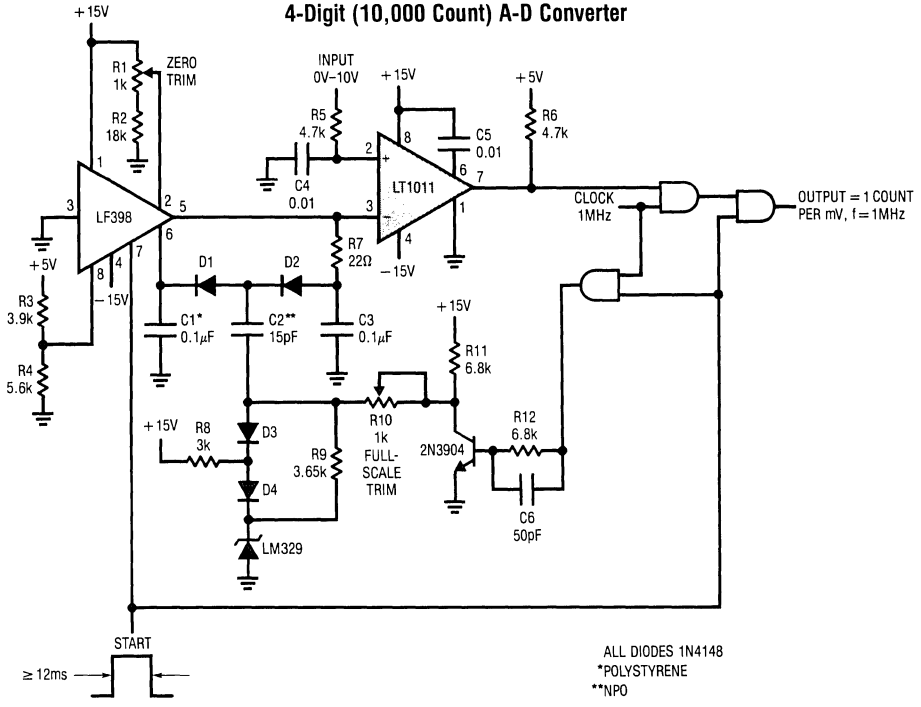
Negative Peak Detector



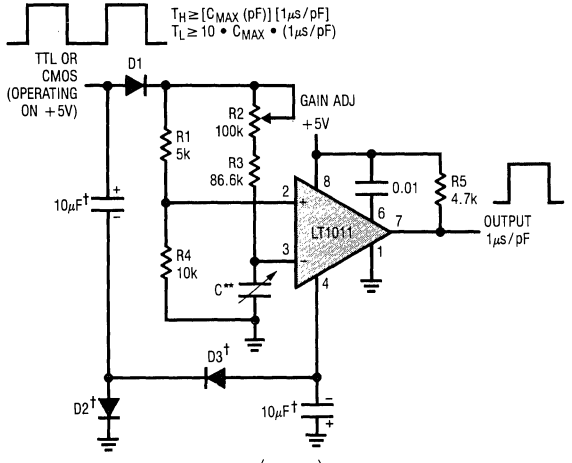
*MYLAR
**SELECT FOR REQUIRED RESET TIME CONSTANT

TYPICAL APPLICATIONS

4-Digit (10,000 Count) A-D Converter



Capacitance to Pulse Width Converter



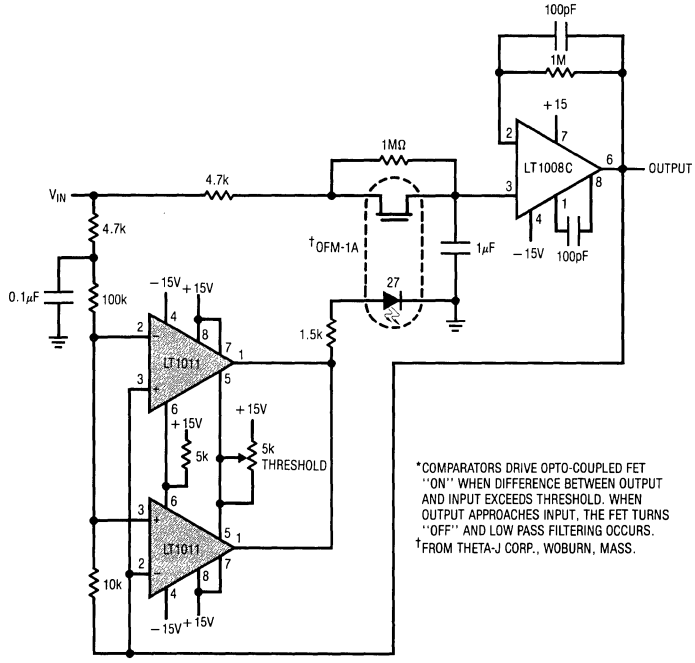
*$PW = (R2 + R3)\ (C)\left(\frac{R1 + R4}{R1}\right)$, INPUT CAPACITANCE OF LT1011 IS ≈6pF. THIS IS AN OFFSET TERM.

†THESE COMPONENTS MAY BE ELIMINATED IF NEGATIVE SUPPLY IS AVAILABLE (–1V TO –15V).

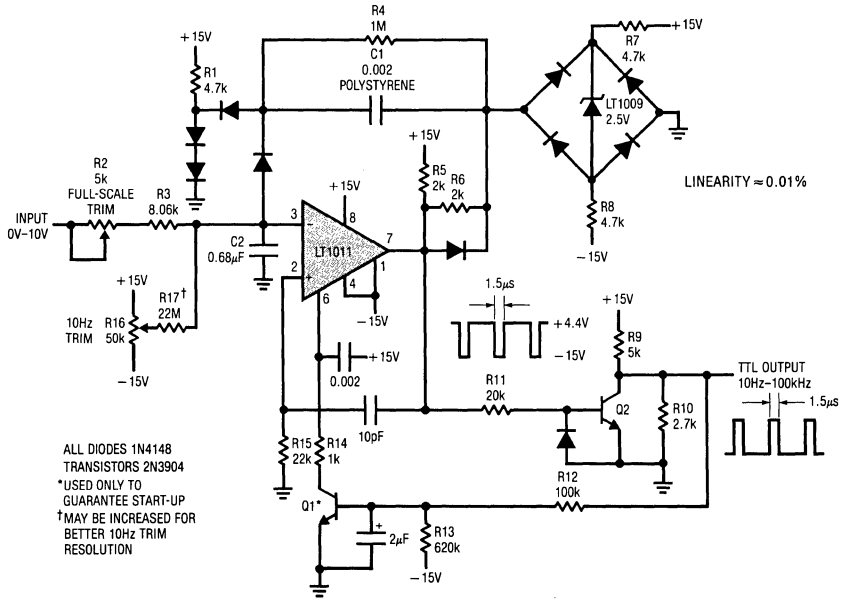
**TYPICAL 2 SECTIONS OF 365pF VARIABLE CAPACITOR WHEN USED AS SHAFT ANGLE INDICATION.

TYPICAL APPLICATIONS

Fast Settling* Filter

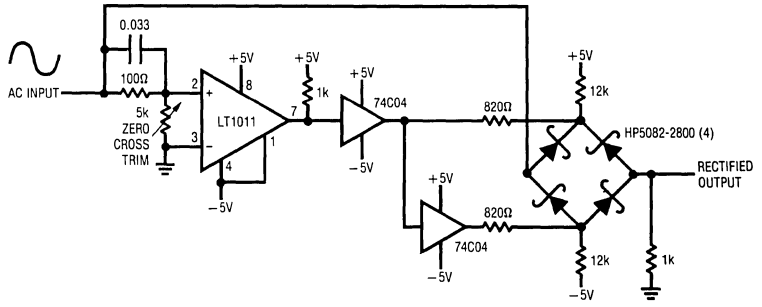


10Hz to 100kHz Voltage to Frequency Converter

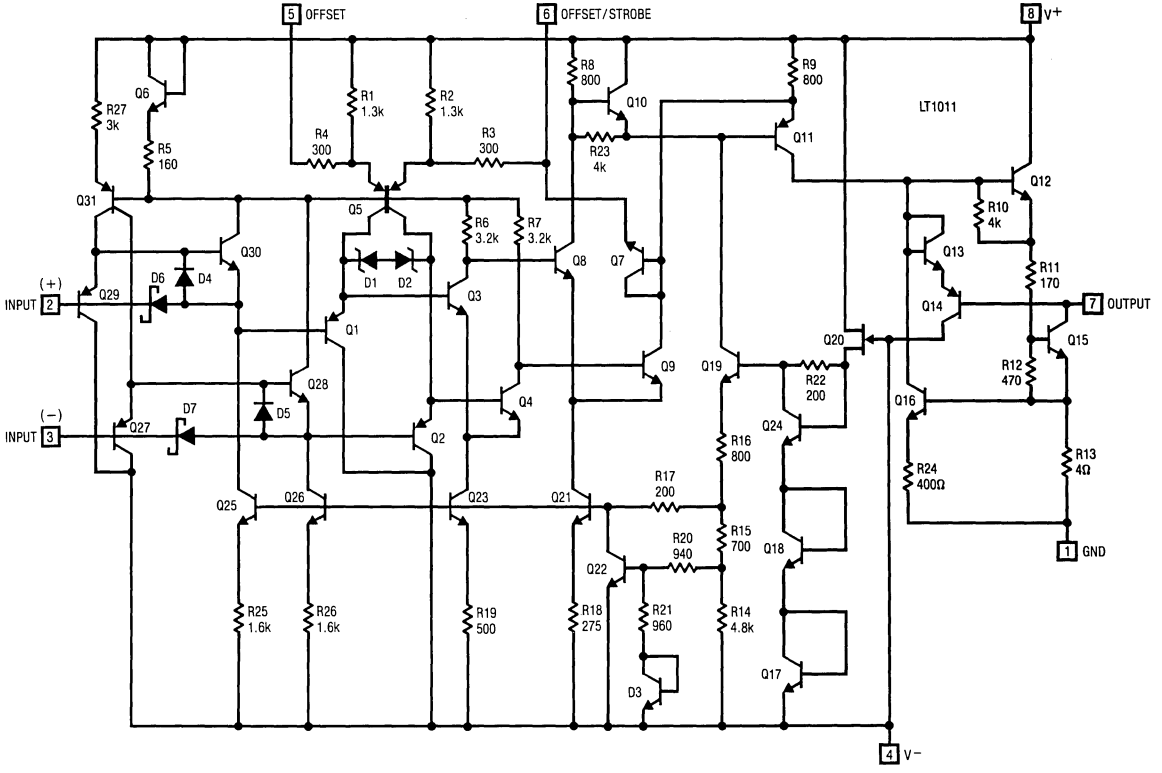


TYPICAL APPLICATIONS

100kHz Precision Rectifier

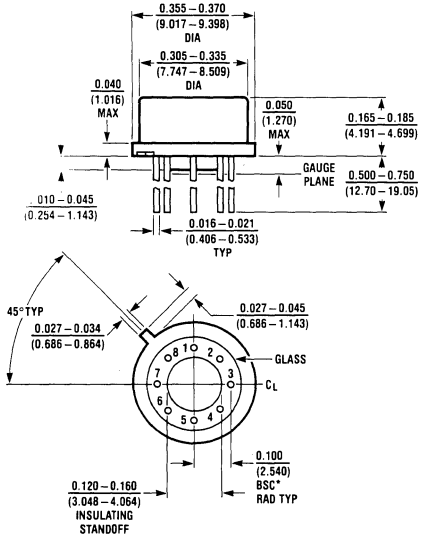


SCHEMATIC DIAGRAM



PACKAGE DESCRIPTION

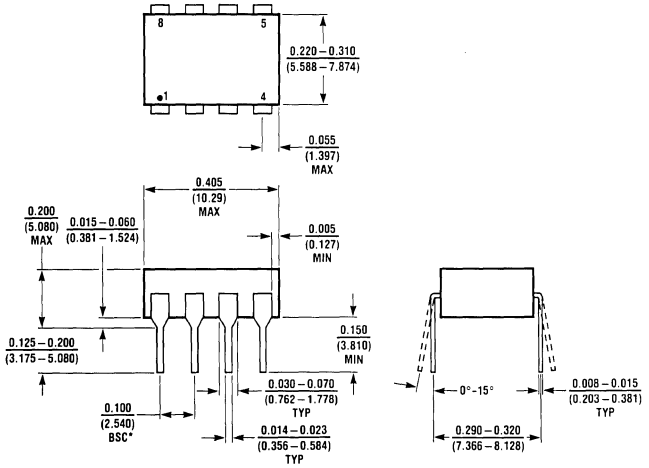
H Package
Metal Can



NOTE: DIMENSIONS IN INCHES

$T_j$max	θ_{ja}	θ_{jc}
150°C	150°C/W	45°C/W

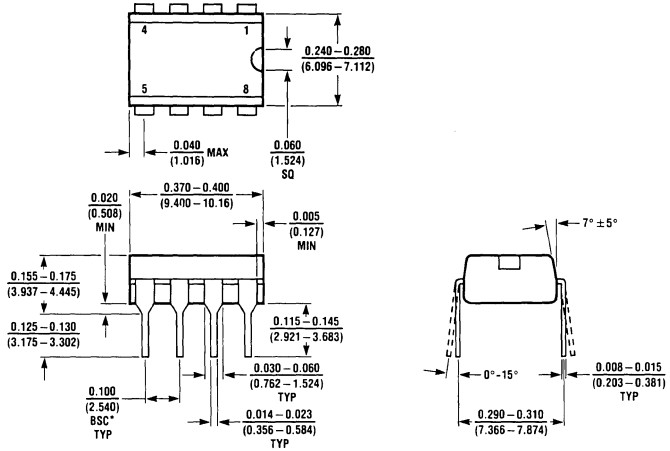
J8 Package
8 Lead Hermetic DIP



NOTE: DIMENSIONS IN INCHES UNLESS OTHERWISE NOTED
*LEADS WITHIN 0.007 OF TRUE POSITION (TP) AT GAUGE PLANE

$T_j$max	θ_{ja}
150°C	100°C/W

N8 Package
8 Lead Plastic



NOTE: DIMENSIONS IN INCHES UNLESS OTHERWISE NOTED
*LEADS WITHIN 0.007 OF TRUE POSITION (TP) AT GAUGE PLANE

$T_j$max	θ_{ja}
100°C	130°C/W

Ultra Fast Precision Comparator

FEATURES

- Ultra Fast (10ns typ)
- Operates Off **Single** +5V Supply, or ±5V
- Complementary Output to TTL
- Low Offset Voltage
- No Minimum Input Slew Rate Requirement
- No Power Supply Current Spiking
- Output Latch Capability

APPLICATIONS

- High Speed A to D Converters
- High Speed Sampling Circuits
- Line Receiver
- Extended Range V to F Converters
- Fast Pulse Height/Width Discriminators

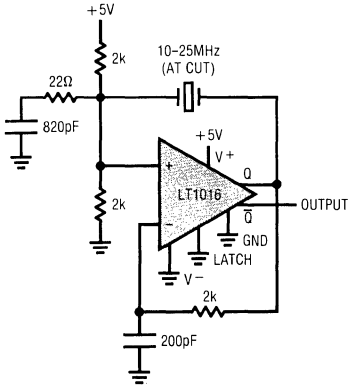
DESCRIPTION

The LT1016 is an ultra fast (10ns) comparator specifically designed to interface directly to TTL logic while operating off either a dual ±5V supply or a single +5V supply. Tight offset voltage specifications and high gain allow the LT1016 to be used in precision applications. Matched complementary outputs further extend the versatility of this new comparator.

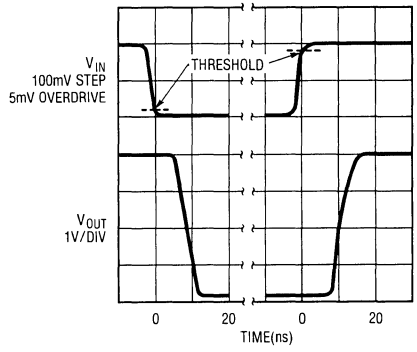
A unique output stage is featured on the LT1016. It provides active drive in both directions for maximum speed into TTL logic or passive loads, yet does not exhibit the large current spikes normally found in ''totem pole'' output stages. This eliminates the need for a minimum input slew rate typical of other very fast comparators. The ability of the LT1016 to remain stable with the outputs in the active region greatly reduces the problem of output ''glitching'' when the input signal is slow moving or is low level.

The LT1016 has a true latch pin for retaining input data at the outputs. The outputs will remain latched as long as the latch pin is held high. Quiescent negative power supply current is only 3mA—about ten times lower than competitive units. This reduces die temperature and allows the negative supply pin to be driven from virtually any supply voltage with a simple resistive divider. Device performance is not affected by variations in negative supply voltage.

10-25MHz Crystal Oscillator



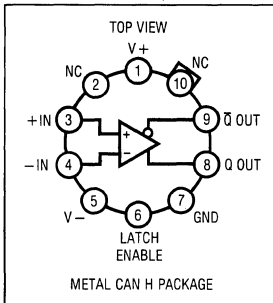
Response Time



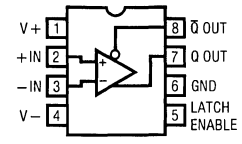
ABSOLUTE MAXIMUM RATINGS

Positive Supply Voltage (Note 4) 7V
Negative Supply Voltage 7V
Differential Input Voltage . . . . . ±5V
Input Voltage (Either Input) . . . . . Equal to Supplies
Latch Pin Voltage . . . . . Equal to Supplies
Output Current (Continuous) . . . . . ±20mA
Operating Temperature Range
LT1016M . . . . . −55°C to +125°C
LT1016C . . . . . 0°C to +70°C
Storage Temperaure Range . . . . . −65°C to +150°C
Lead Temperature (Soldering, 10 sec) . . . . . 300°C

PACKAGE/ORDER INFORMATION



METAL CAN H PACKAGE



HERMETIC DIP J8 PACKAGE
PLASTIC DIP N8 PACKAGE

ORDER PART NUMBER
LT1016MH LT1016CH
LT1016MJ LT1016CJ LT1016CN

ELECTRICAL CHARACTERISTICS

$V^+ = 5V$, $V^- = 5V$, $V_{OUT}(Q) = 1.4V$, $V_{LATCH} = 0V$, $T_A = 25°C$, unless otherwise noted.

SYMBOL	PARAMETERS	CONDITIONS			LT1016M MIN	LT1016M TYP	LT1016M MAX	LT1016C MIN	LT1016C TYP	LT1016C MAX	UNITS
V_{OS}	Input Offset Voltage	$R_S \le 100\Omega$ (Note 1)				0.8	±2		1.0	±3	mV
				●			3			3.5	mV
$\frac{\Delta V_{OS}}{\Delta T}$	Input Offset Voltage Drift			●		4			4		µV/°C
I_{OS}	Input Offset Current	(Note 1)				0.3	1		0.3	1	µA
				●			1.3		0.3	1.3	µA
I_B	Input Bias Current	(Note 2)				5	10		5	10	µA
				●			13			13	µA
	Input Voltage Range	(Note 5)		●	−3.75		+3.5	−3.75		+3.5	V
		Single +5V Supply		●	+1.25		+3.5	+1.25		+3.5	V
CMRR	Common-Mode Rejection	$-3.75V \le V_{CM} \le +3.5V$		●	80	96		80	96		dB
PSRR	Supply Voltage Rejection	Positive Supply $4.6V \le V^+ \le 5.4V$		●	70	85		70	85		dB
		Negative Supply $2V \le V^- \le 7V$		●	80	100		80	100		dB
A_V	Small Signal Voltage Gain	$1V \le V_{OUT} \le 2V$			1400	3000		1400	3000		V/V
V_{OH}	Output High Voltage	$V^+ \le 4.6V$,	$I_{OUT} = 1mA$	●	3.0	3.4		3.0	3.4		V
			$I_{OUT} = 10mA$	●	2.4	3.0		2.4	3.0		V
V_{OL}	Output Low Voltage		$I_{SINK} = 4mA$	●		0.3	0.5		0.3	0.5	V
			$I_{SINK} = 10mA$			0.4			0.4		V
I^+	Positive Supply Current			●		25	35		25	35	mA
I^-	Negative Supply Current			●		3	5		3	5	mA
V_{IH}	Latch Pin Hi Input Voltage			●	2.0			2.0			V
V_{IL}	Latch Pin Lo Input Voltage			●			0.8			0.8	V
I_{IL}	Latch Pin Current	$V_{LATCH} = 0V$		●			500			500	µA

ELECTRICAL CHARACTERISTICS

$V^+ = 5V$, $V^- = 5V$, $V_{OUT}(Q) = 1.4V$, $V_{LATCH} = 0V$, $T_A = 25°C$, unless otherwise noted.

SYMBOL	PARAMETERS	CONDITIONS		LT1016M MIN	LT1016M TYP	LT1016M MAX	LT1016C MIN	LT1016C TYP	LT1016C MAX	UNITS
t_{PD}	Propagation Delay	$\Delta V_{IN} = 100mV$, $OD = 5mV$			10	14		10	14	ns
	(Note 3)		●			16			16	ns
		$\Delta V_{IN} = 100mV$, $OD = 20mV$			9	12		9	12	ns
			●			15			15	ns
Δt_{PD}	Differential Propagation Delay	(Note 3) $\Delta V_{IN} = 100mV$, $OD = 5mV$				3			3	ns
	Latch Setup Time				2			2		ns

The ● denotes the specifications which apply over the full operating temperature range.

Note 1: Input offset voltage is defined as the average of the two voltages measured by forcing first one output, then the other to 1.4V. Input offset current is defined in the same way.

Note 2: Input bias current (I_B) is defined as the average of the two input currents.

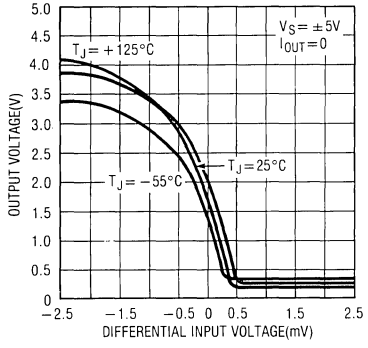
Note 3: Propagation delay is measured with the overdrive added to actual V_{OS}. Units are sample tested only.

Note 4: Electrical specifications apply only up to 5.4V.

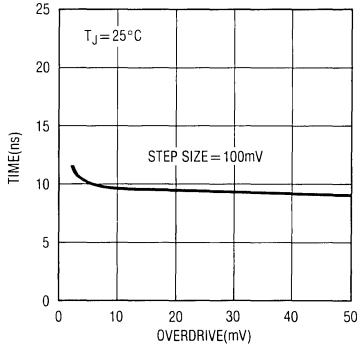
Note 5: See text for discussion of input voltage range for supplies other than ±5V, or +5V.

TYPICAL PERFORMANCE CHARACTERISTICS

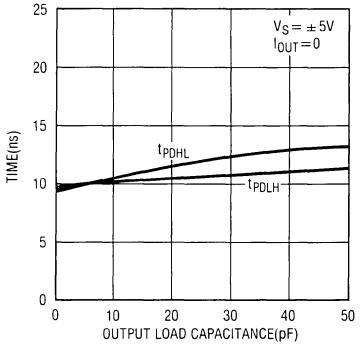
Gain Characteristics



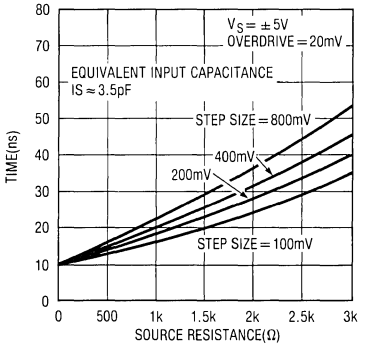
Propagation Delay vs Overdrive



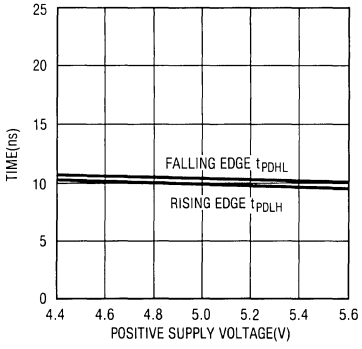
Propagation Delay vs Load Capacitance



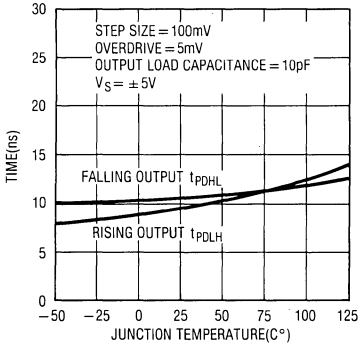
Propagation Delay vs Source Resistance



Propagation Delay vs Supply Voltage

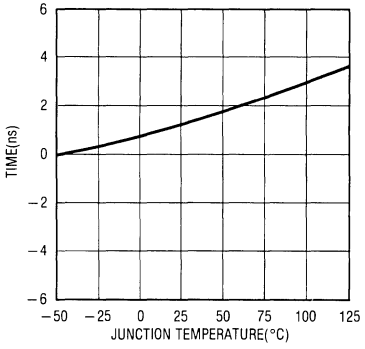


Propagation Delay vs Temperature

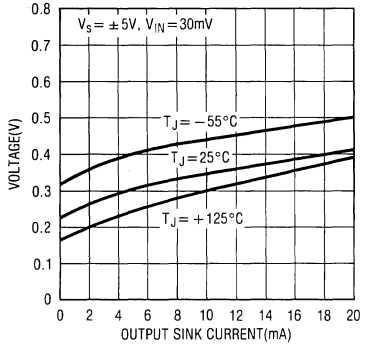


TYPICAL PERFORMANCE CHARACTERISTICS

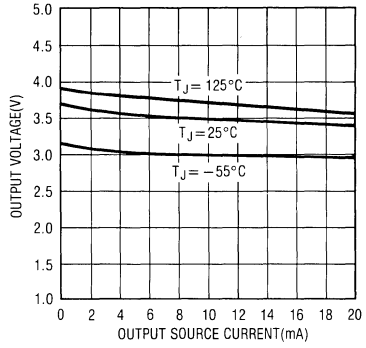
Latch Set-Up Time



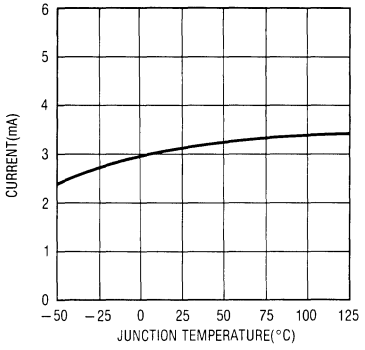
Output Low Voltage (V_{OL})



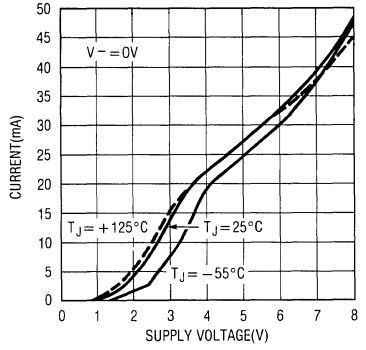
Output High Voltage (V_{OH})



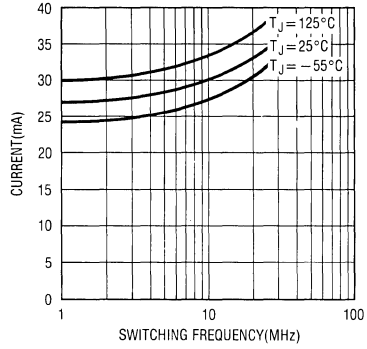
Negative Supply Current



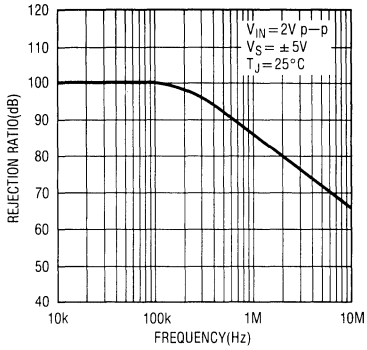
Positive Supply Current



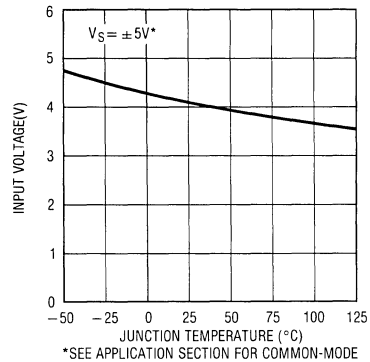
Positive Supply Current



Common-Mode Rejection

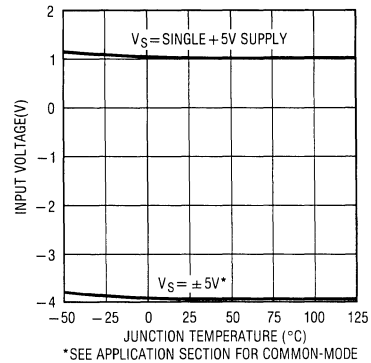


Positive Common-Mode Limit



*SEE APPLICATION SECTION FOR COMMON-MODE LIMIT WITH VARYING SUPPLY VOLTAGE.

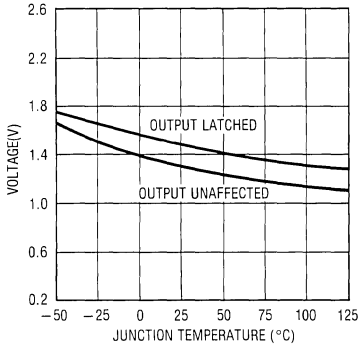
Negative Common-Mode Limit



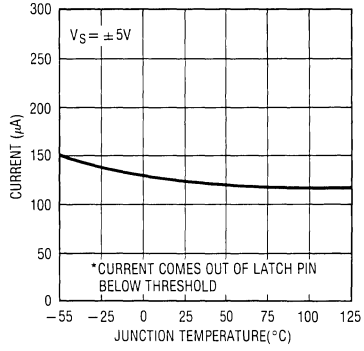
*SEE APPLICATION SECTION FOR COMMON-MODE LIMIT WITH VARYING SUPPLY VOLTAGE.

TYPICAL PERFORMANCE CHARACTERISTICS

Latch Pin Threshold



Latch Pin Current*



APPLICATIONS INFORMATION

Common-Mode Considerations

The LT1016 is specified for a common-mode range of −3.75V to +3.5V with supply voltages of ±5V. A more general consideration is that the common-mode range is 1.25V above the negative supply and 1.5V below the positive supply, independent of the actual supply voltage. The criteria for common-mode limit is that the output still responds correctly to a small differential input signal. Either input may be outside the common-mode limit (up to the supply voltage) as long as the remaining input is within the specified limit, and the output will still respond correctly. There is one consideration, however, for inputs which exceed the positive common-mode limit. Propagation delay will be increased by up to 10ns if the signal input is more positive than the upper common-mode limit and then switches back to within the common-mode range. This effect is not seen for signals more negative than the lower common-mode limit.

Input Impedance and Bias Current

Input bias current is measured with the output held at 1.4V. As with any simple NPN differential input stage, the LT1016 bias current will go to zero on an input which is low and double on the input which is high. If both inputs are less than 0.8V above V^-, both input bias currents will go to zero. If either input exceeds the positive common-mode limit, input bias current will increase rapidly, approaching several milliamperes at $V_{IN} = V^+$.

Differential input resistance at zero differential input voltage is about 10kΩ, rapidly increasing as larger DC differential input signals are applied. Common-mode input resistance is about 4MΩ with zero differential input voltage. With large differential input signals, the high input will have an input resistance of about 2MΩ and the low input, greater than 20MΩ.

Input capacitance is typically 3.5pF. This is measured by inserting a 1kΩ resistor in series with the input and measuring the resultant change in propagation delay.

Latch Pin Dynamics

The latch pin is intended to retain input data (output latched) when the latch pin goes high. This pin will float to a high state when disconnected, so a flow-through condition requires that the latch pin be grounded. To guarantee data retention, the input signal must be valid at least 5ns before the latch goes high (set-up time) and must remain valid at least 3ns after the latch goes high (hold time). When the latch goes low, new data will appear at the output in approximately 8–10ns. The latch pin is designed to be driven with TTL or CMOS gates. It has no built-in hysteresis.

APPLICATIONS INFORMATION

Measuring Response Time

The LT1016 is able to respond quickly to fast low level signals because it has a very high gain-bandwidth product (≈50GHz), even at very high frequencies. To properly measure the response of the LT1016 requires an input signal source with very fast rise times and exceptionally clean settling characteristics. This last requirement comes about because the standard comparator test calls for an input step size that is large compared to the overdrive amplitude. Typical test conditions are 100mV step size with only 5mV overdrive. This requires an input signal that settles to within 1% (1mV) of final value in only a few nanoseconds with no ringing or "long tailing". Ordinary high speed pulse generators are not capable of generating such a signal, and in any case, no ordinary oscilloscope is capable of diplaying the waveform to check its fidelity. Some means must be used to inherently generate a fast, clean edge with known final value.

The circuit shown in Figure 1 is the best *electronic* means of generating a known fast, clean step to test comparators. It uses a very fast transistor in a common base configuration. The transistor is switched "off" with a fast edge from the generator and the collector voltage settles to exactly 0V in just a few nanoseconds. The most important feature of this circuit is the lack of feedthrough from the generator to the comparator input. This prevents overshoot on the comparator input which would give a false fast reading on comparator response time.

To adjust this circuit for exactly 5mV overdrive, V_1 is adjusted so that the LT1016 output under test settles to 1.4V (in the linear region). Then V_1 is *changed* 5V to set overdrive at 5mV.

The test circuit shown measures low to high transition on the "+" input. For opposite polarity transitions on the output, simply reverse the inputs of the LT1016.

High Speed Design Techniques

A substantial amount of design effort has made the LT1016 relatively easy to use. It is much less prone to oscillation and other vagaries than some slower comparators, even with slow input signals. In particular, the LT1016 is stable in its linear region, a feature no other high speed comparator has. Additionally, output stage switching does not appreciably change power supply current, further enhancing stability. These features make the application of the 50GHz gain-bandwidth LT1016 considerably easier than other fast comparators. Unfortunately, laws of physics dictate that the circuit *environment* the LT1016 works in must be properly prepared. The performance limits of high speed circuitry are often determined by parasitics such as stray capacitance, ground impedance, and layout. Some of these considerations are present in digital systems where designers are comfortable describing bit patterns and memory access times in terms of nanoseconds. The LT1016 can be used in such fast digital systems and Figure 2 shows just how fast the device is. The simple test circuit allows us to see that the LT1016's (Trace B)

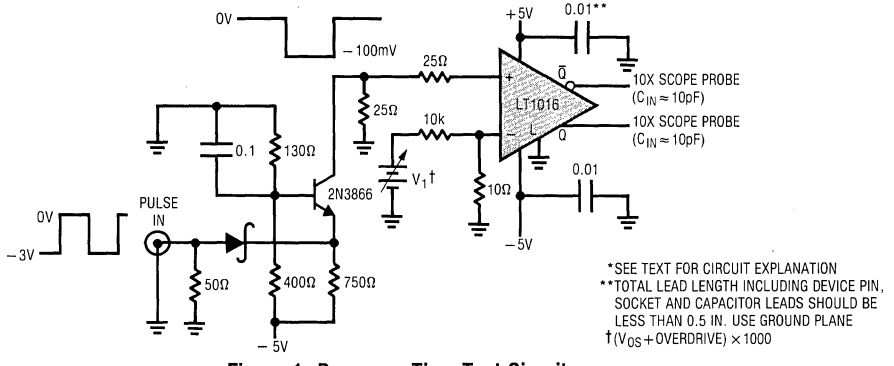


Figure 1. Response Time Test Circuit

APPLICATIONS INFORMATION

response to the pulse generator (Trace A) is as fast as a TTL inverter (Trace C) even when the LT1016 has only millivolts of input signal! Linear circuits operating with this kind of speed make many engineers justifiably wary. Nanosecond domain linear circuits are widely associated with oscillations, mysterious shifts in circuit characteristics, unintended modes of operation and outright failure to function.

Other common problems include different measurement results using various pieces of test equipment, inability to make measurement connections to the circuit without inducing spurious responses and dissimilar operation between two "identical" circuits. If the components used in the circuit are good and the design is sound, all of the above problems can usually be traced to failure to provide a proper circuit "environment." To learn how to do this requires studying the causes of the aforementioned difficulties.

By far the most common error involves power supply bypassing. Bypassing is necessary to maintain low supply impedance. DC resistance and inductance in supply wires and PC traces can quickly build up to unacceptable levels. This allows the supply line to move as internal current levels of the devices connected to it change. This will almost always cause unruly operation. In addition, several devices connected to an unbypassed supply can "communicate" through the finite supply impedances, causing erratic modes. Bypass capacitors furnish a simple way to eliminate this problem by providing a local reservoir of energy at the device. The bypass capacitor acts like an electrical flywheel to keep supply impedance low at high frequencies. The choice of what type of capacitors to use for bypassing is a critical issue and should be approached carefully. An unbypassed LT1016 is shown responding to a pulse input in Figure 3. The power supply the LT1016 sees at its terminals has high impedance at high frequency. This impedance forms a voltage divider with the LT1016, allowing the supply to move as internal conditions in the comparator change. This causes local feedback and oscillation occurs. Although the LT1016 responds to the input pulse, its output is a blur of 100MHz oscillation. *Always use bypass capacitors.*

In Figure 4 the LT1016's supplies are bypassed, but it still oscillates. In this case, the bypass units are either too far from the device or are lossy capacitors. *Use capacitors with good high frequency characteristics and mount*

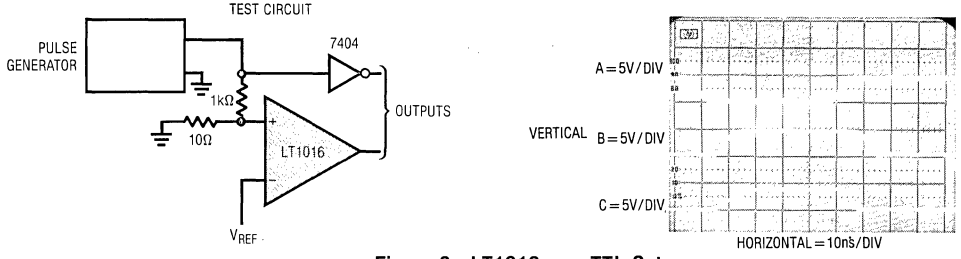


Figure 2. LT1016 vs a TTL Gate

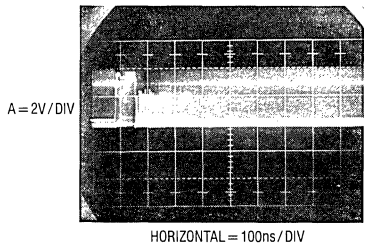


Figure 3. Unbypassed LT1016 Response

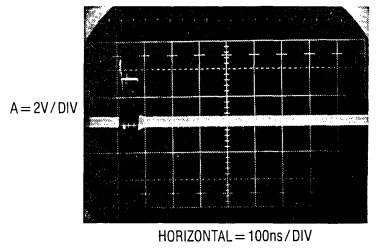


Figure 4. LT1016 Response with Poor Bypassing

APPLICATIONS INFORMATION

them as close as possible to the LT1016. An inch of wire between the capacitor and the LT1016 can cause problems. If operation in the linear region is desired, the LT1016 must be over a ground plate with good RF bypass capacitors ($\geq 0.01\mu F$) having lead lengths less than 0.2 inches. Do not use sockets.

In Figure 5 the device is properly bypassed but a new problem pops up. This photo shows both outputs of the comparator. Trace A appears normal, but Trace B shows an excursion of almost 8V — quite a trick for a device running from a +5V supply. This is a commonly reported problem in high speed circuits and can be quite confusing. It is not due to suspension of natural law, but is traceable to a grossly miscompensated or improperly selected oscilloscope probe. *Use probes which match your oscilloscope's input characteristics and compensate them properly.* Figure 6 shows another probe-induced problem. Here, the amplitude seems correct but the 10ns response time LT1016 appears to have 50ns edges! In this case, the probe used is too heavily compensated or slow for the oscilloscope. Never use 1X or "straight" probes. Their bandwidth is 20MHz or less and capacitive loading is high. *Check probe bandwidth to ensure it is adequate for the measurement. Similarly, use an oscilloscope with adequate bandwidth.*

In Figure 7 the probes are properly selected and applied but the LT1016's output rings and distorts badly. In this case, the probe ground lead is too long. For general purpose work most probes come with ground leads about 6 inches long. At low frequencies this is fine. At high speed, the long ground lead looks inductive, causing the ringing shown. High quality probes are always supplied with some short ground straps to deal with this problem. Some come with very short spring clips which fix directly to the probe tip to facilitate a low impedance ground connection. For fast work, the ground connection to the probe should not exceed 1 inch in length. *Keep the probe ground connection as short as possible.*

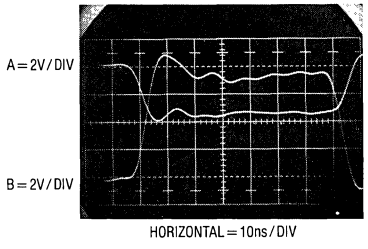


Figure 5. Improper Probe Compensation Causes Seemingly Unexplainable Amplitude Error

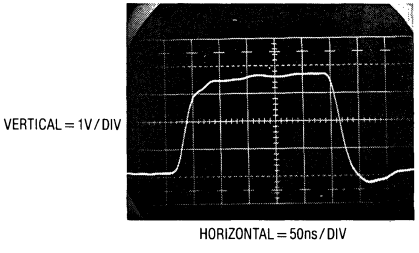


Figure 6. Overcompensated or Slow Probes Make Edges Look Too Slow

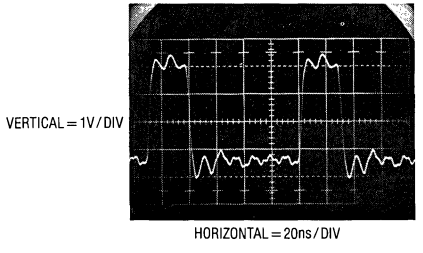


Figure 7. Typical Results Due to Poor Probe Grounding

APPLICATIONS INFORMATION

Figure 8 shows the LT1016's output (Trace B) oscillating near 40MHz as it responds to an input (Trace A). Note that the input signal shows artifacts of the oscillation. This example is caused by improper grounding of the comparator. In this case, the LT1016's ground pin connection is 1 inch long. The ground lead of the LT1016 must be as short as possible and connected directly to a low impedance ground point. Any substantial impedance in the LT1016's ground path will generate effects like this. The reason for this is related to the necessity of bypassing the power supplies. The inductance created by a long device ground lead permits mixing of ground currents, causing undesired effects in the device. The solution here is simple. *Keep the LT1016's ground pin connection as short (typically 1/4 inch) as possible and run it directly to a low impedance ground. Do not use sockets.*

Figure 9 addresses the issue of the "low impedance ground," referred to previously. In this example, the output is clean except for chattering around the edges. This photograph was generated by running the LT1016 without a "ground plane." A ground plane is formed by using a continuous conductive plane over the surface of the circuit board. The only breaks in this plane are for the circuit's necessary current paths. The ground plane serves two functions. Because it is flat (AC currents travel along the surface of a conductor) and covers the entire area of the board, it provides a way to access a low inductance ground from anywhere on the board. Also, it minimizes the effects of stray capacitance in the circuit by referring them to ground. This breaks up potential unintended and harmful feedback paths. *Always use a ground plane with the LT1016, when input signal levels are low or slow moving.*

"Fuzz" on the edges is the difficulty in Figure 10. This condition appears similar to Figure 10, but the oscillation is more stubborn and persists well after the output has gone low. This condition is due to stray capacitive feedback from the outputs to the inputs. A 3kΩ input source impedance and 3pF of stray feedback allowed this oscillation. The solution for this condition is not too difficult. *Keep source impedances as low as possible, preferably 1kΩ or less. Route output and input pins and components away from each other.*

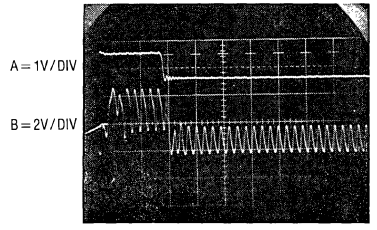


Figure 8. Excessive LT1016 Ground Path Resistance Causes Oscillation

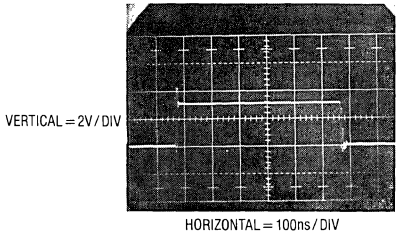


Figure 9. Transition Instabilities Due to No Ground Plane

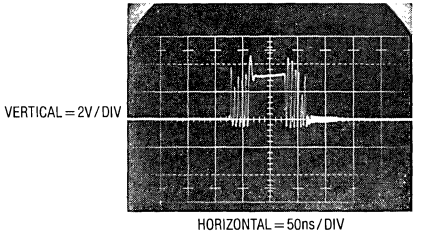


Figure 10. 3pF Stray Capacitive Feedback with 3kΩ Source Can Cause Oscillation

APPLICATIONS INFORMATION

The opposite of stray-caused oscillations appears in Figure 11. Here, the output response (Trace B) badly lags the input (Trace A). This is due to some combination of high source impedance and stray capacitance to ground at the input. The resulting RC forces a lagged response at the input, and output delay occurs. An RC combination of 2kΩ source resistance and 10pF to ground gives a 20ns time constant — significantly longer than the LT1016's response time. *Keep source impedances low and minimize stray input capacitance to ground.*

Figure 12 shows another capacitance-related problem. Here the output does not oscillate, but the transitions are discontinuous and relatively slow. The villain of this situation is a large output load capacitance. This could be caused by cable driving, excessive output lead length or the input characteristics of the circuit being driven. In most situations this is undesirable and may be eliminated by buffering heavy capacitive loads. In a few circumstances it may not affect overall circuit operation and is tolerable. *Consider the comparator's output load characteristics and their potential effect on the circuit. If necessary, buffer the load.*

Another output-caused fault is shown in Figure 13. The output transitions are initially correct but end in a ringing condition. The key to the solution here is the ringing. What is happening is caused by an output lead which is too long. The output lead looks like an unterminated transmission line at high frequencies and reflections occur. This accounts for the abrupt reversal of direction on the leading edge and the ringing. If the comparator is driving TTL this may be acceptable, but other loads may not tolerate it. In this instance, the direction reversal on the leading edge might cause trouble in a fast TTL load. *Keep output lead lengths short. If they get much longer than a few inches, terminate with a resistor (typically 250Ω–400Ω).*

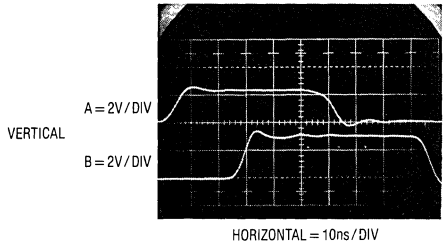


Figure 11. Stray 5pF Capacitance from Input to Ground Causes Delay

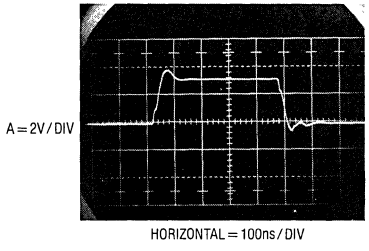


Figure 12. Excessive Load Capacitance Forces Edge Distortion

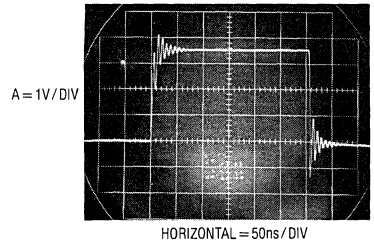


Figure 13. Lengthy, Unterminated Output Lines Ring from Reflections

APPLICATIONS INFORMATION

200ns-0.01% Sample-and-Hold Circuit

Figure 14's circuit uses the LT1016's high speed to improve upon a standard circuit function. The 200ns acquisition time is well beyond monolithic sample-and-hold capabilities. Other specifications exceed the best commercial unit's performance. This circuit also gets around many of the problems associated with standard sample-and-hold approaches, including FET switch errors and amplifier settling time. To achieve this, the LT1016's high speed is used in a circuit which completely abandons traditional sample-and-hold methods.

Important specifications for this circuit include:

Acquisition Time	<200ns
Common-Mode Input Range	± 3V
Droop	$1\mu V/\mu s$
Hold Step	2mV
Hold Settling Time	15ns
Feedthrough Rejection	$>>100$dB

When the sample-hold line goes low, a linear ramp starts just below the input level and ramps upward. When the ramp voltage reaches the input voltage, A1 shuts off the ramp, latches itself off, and sends out a signal indicating sampling is complete.

4μs, 12-Bit A-D Converter

The LT1016's high speed is used to implement a very fast 12-bit A-D converter in Figure 15. The circuit is a modified form of the standard successive approximation approach and is faster than most commercial SAR 12-bit units. In this arrangement the 2504 successive approximation register (SAR), A1 and C1 test each bit, beginning with the MSB, and produce a digital word representing V_{IN}'s value. To get faster conversion time, the clock is sped up after the third MSB is converted. This takes advantage of the segmented DAC used, which has significantly faster settling time for the lower 9 bits.

1Hz-10MHz V→F Converter

The LT1016 and the LT1012 low drift amplifier combine to form a high speed V→F converter in Figure 16. A variety of circuit techniques is used to achieve a 1Hz to 10MHz output. Overrange to 12MHz ($V_{IN}=12$V) is provided. This circuit has a wider dynamic range (140dB, or 7 decades) than any commercially available unit. The 10MHz full-scale frequency is 10 times faster than currently available monolithic V→F's. The theory of operation is based on the identity $Q=CV$.

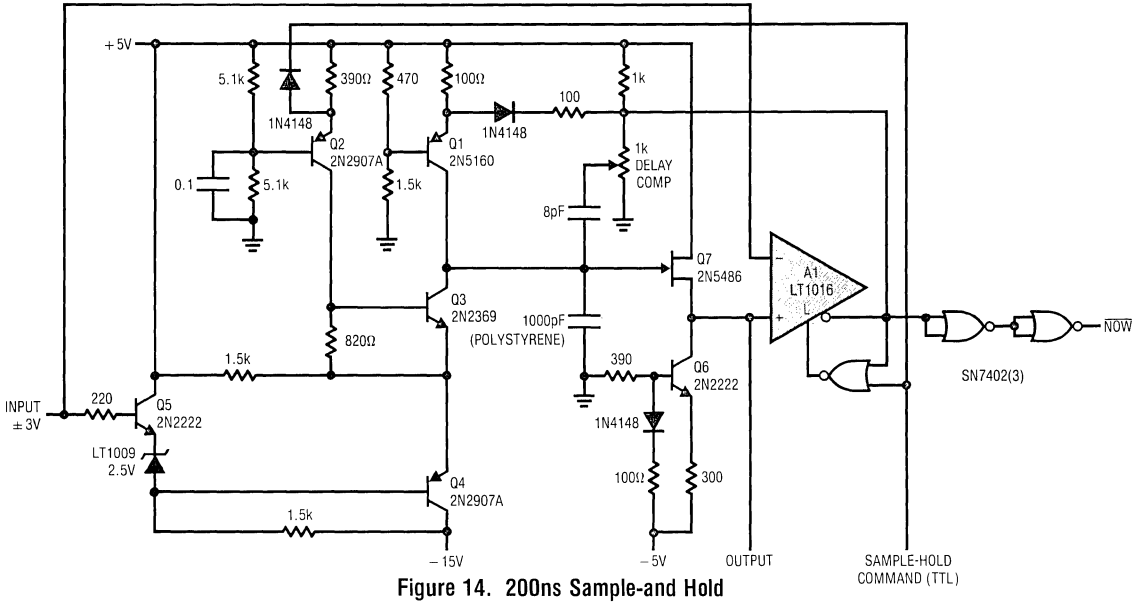


Figure 14. 200ns Sample-and Hold

APPLICATIONS INFORMATION

Each time the circuit produces an output pulse, it feeds back a fixed quantity of charge (Q) to a summing node (Σ). The circuit's input furnishes a comparison current at the summing node. The difference signal at the node is integrated in a monitoring amplifier's feedback capacitor. The amplifier controls the circuit's output pulse generator, completing a feedback loop around the integrating amplifier. To maintain the summing node at zero, the pulse generator runs at a frequency which permits enough charge pumping to offset the input signal. Thus, the output frequency will be linearly related to the input voltage. A1 is the integrating amplifier.

To trim this circuit, ground the input and adjust the 1k pot for 1Hz output. Next, apply 10.000V and set the 2kΩ unit for 10.000MHz output. The transfer linearity of the circuit is 0.06%. Full-scale drift is typically 50ppm/°C and zero point error about 0.2μV/°C (0.2Hz/°C).

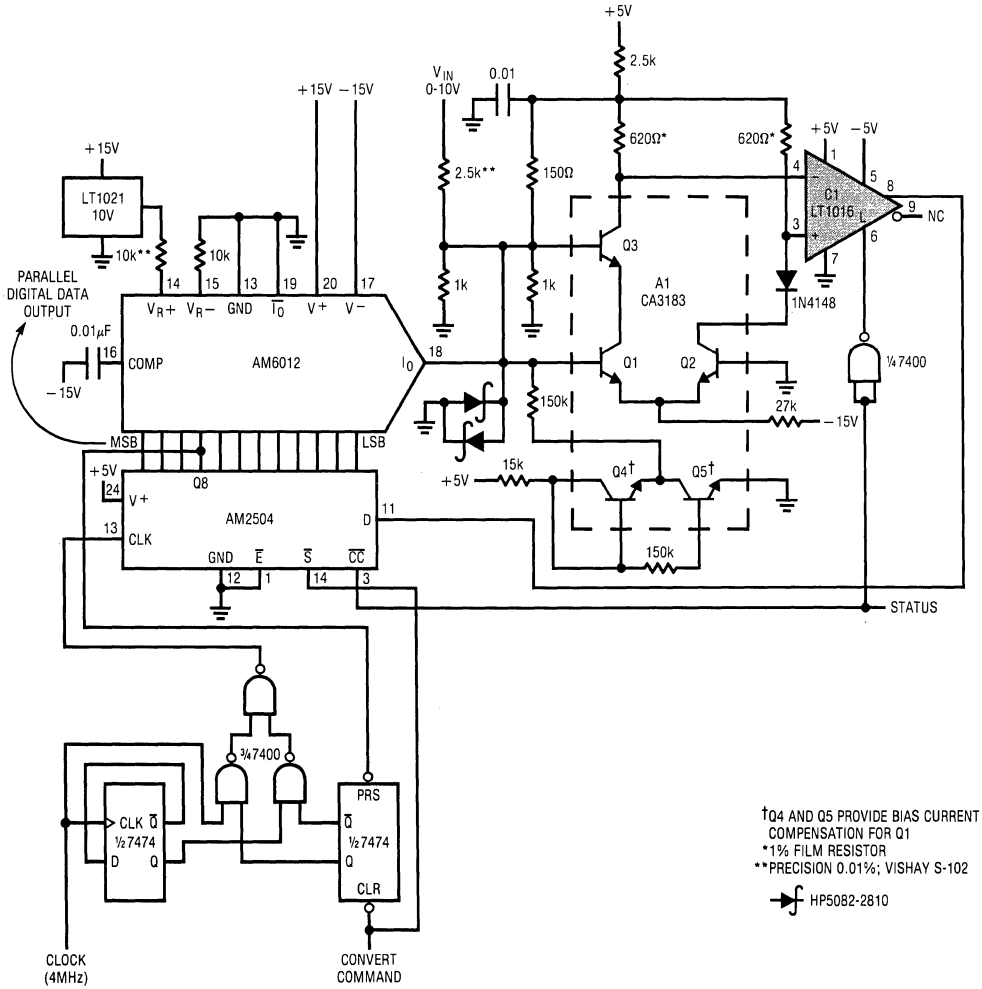


Figure 15. 4μs*, 12-Bit SAR Converter. Clock is Sped up after the Third Bit, Shortening Overall Conversion Time.

*Consult Factory For Improved Version of This Circuit With 2.5μs Conversion Time.

APPLICATIONS INFORMATION

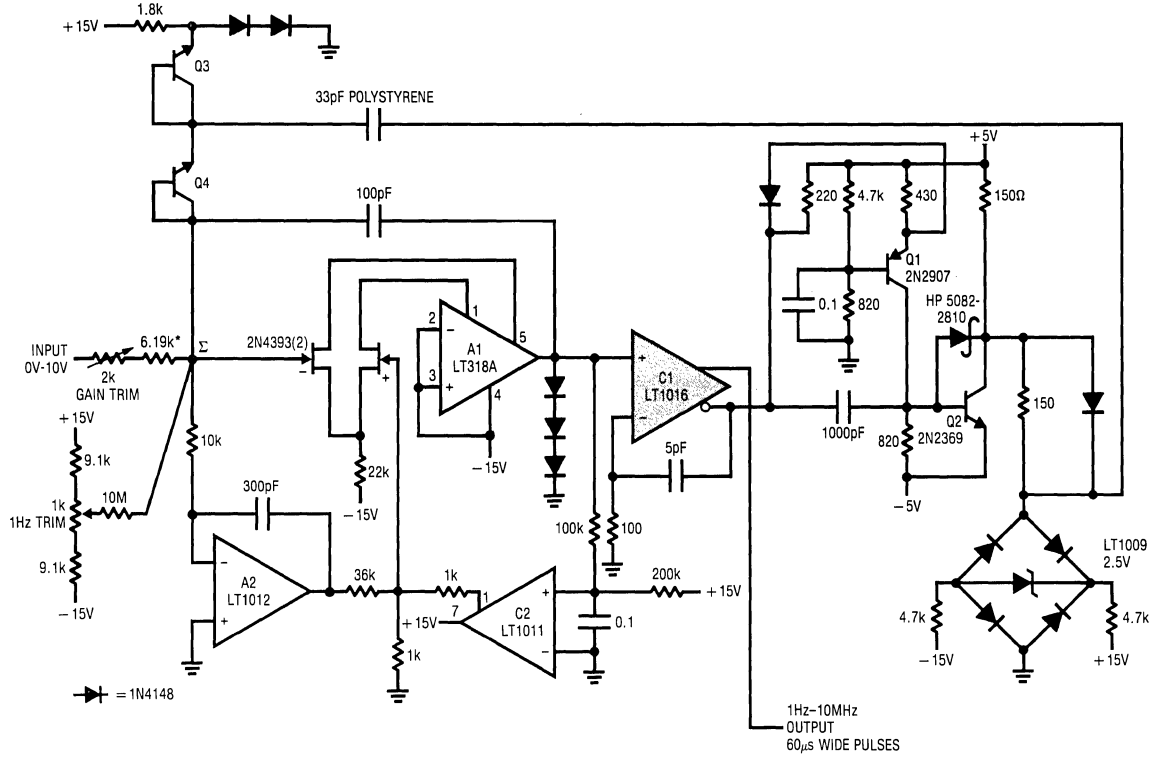
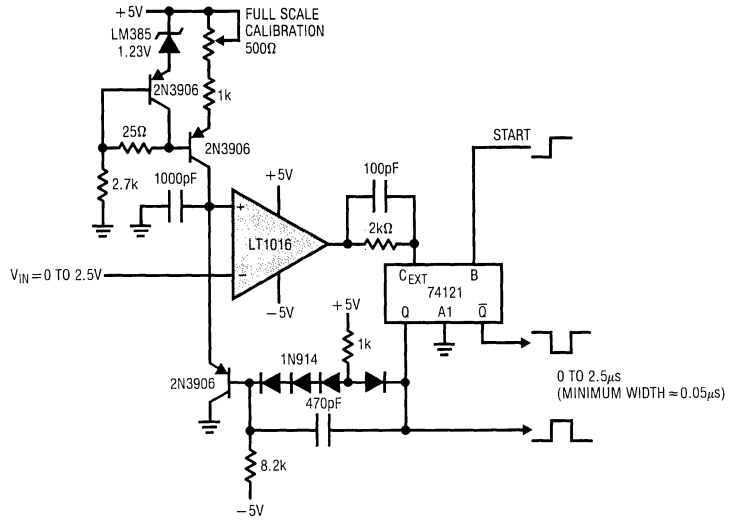


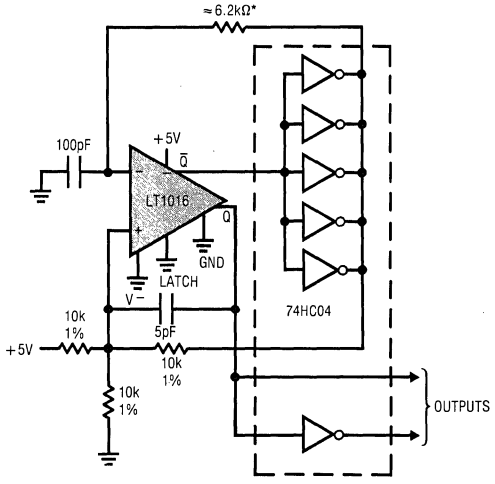
Figure 16. 1Hz-10MHz V to F Converter

Voltage Controlled Pulse Width Generator



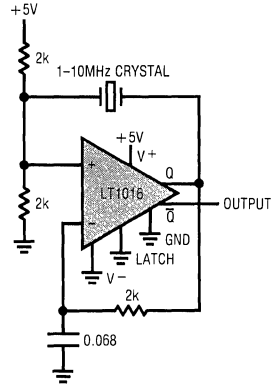
APPLICATIONS INFORMATION

Single Supply Precision RC 1MHz Oscillator



*SELECT OR TRIM FOR f = 1.00MHz

1-10MHz Crystal Oscillator



APPENDIX A

About Level Shifts

The TTL output of the LT1016 will interface with many circuits directly. Many applications, however, require some form of level shifting of the output swing. With LT1016-based circuits this is not trivial because it is desirable to maintain very low delay in the level shifting stage. When designing level shifters, keep in mind that the TTL output of the LT1016 is a sink-source pair (Figure A1) with good ability to drive capacitance (such as feedforward capacitors).

Figure A2 shows a non-inverting voltage gain stage with a 15V output. When the LT1016 switches, the base-emitter voltages at the 2N2369 reverse, causing it to switch very quickly. The 2N3866 emitter-follower gives a low impedance output and the Schottky diode aids current sink capability.

Figure A3 is a very versatile stage. It features a bipolar swing which may be programmed by varying the output transistor's supplies. This 3ns delay stage is ideal for driving FET switch gates. Q1, a gated current source, switches the Baker-clamped output transistor, Q2. The heavy feedforward capacitor from the LT1016 is the key to low delay, providing Q2's base with nearly ideal drive. This capacitor loads the LT1016's output transition (Trace A, Figure A4), but Q2's switching is clean (Trace B, Figure A4) with 3ns delay on the rise and fall of the pulse.

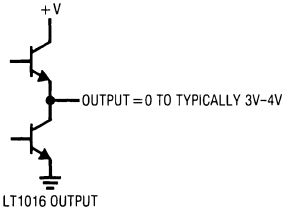


Figure A1

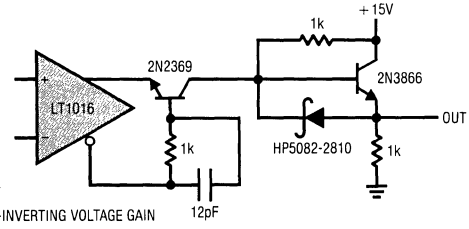


Figure A2

APPENDIX A

Figure A5 is similar to A2 except that a sink transistor has replaced the Schottky diode. The two emitter-followers drive a power MOSFET which switches 1A at 15V. Most of the 7ns–9ns delay in this stage occurs in the MOSFET and the 2N2369.

When designing level shifters, remember to use transistors with fast switching times and high f_T's. To get the kind of results shown, switching times in the ns range and f_T's approaching 1GHz are required.

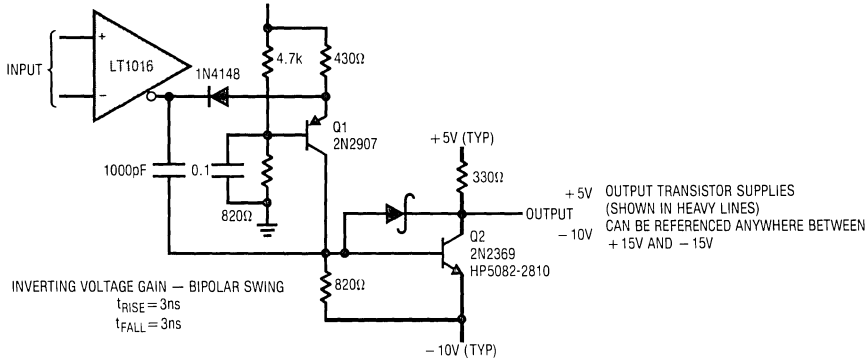


Figure A3

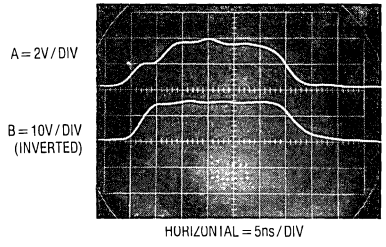


Figure A4. Figure A3's Waveforms

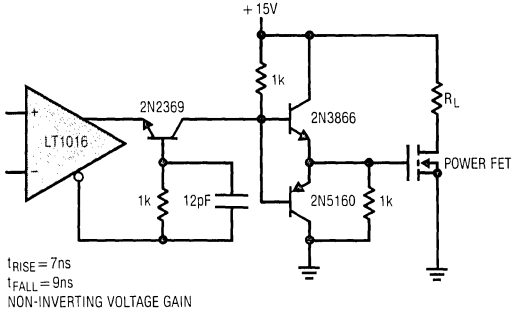
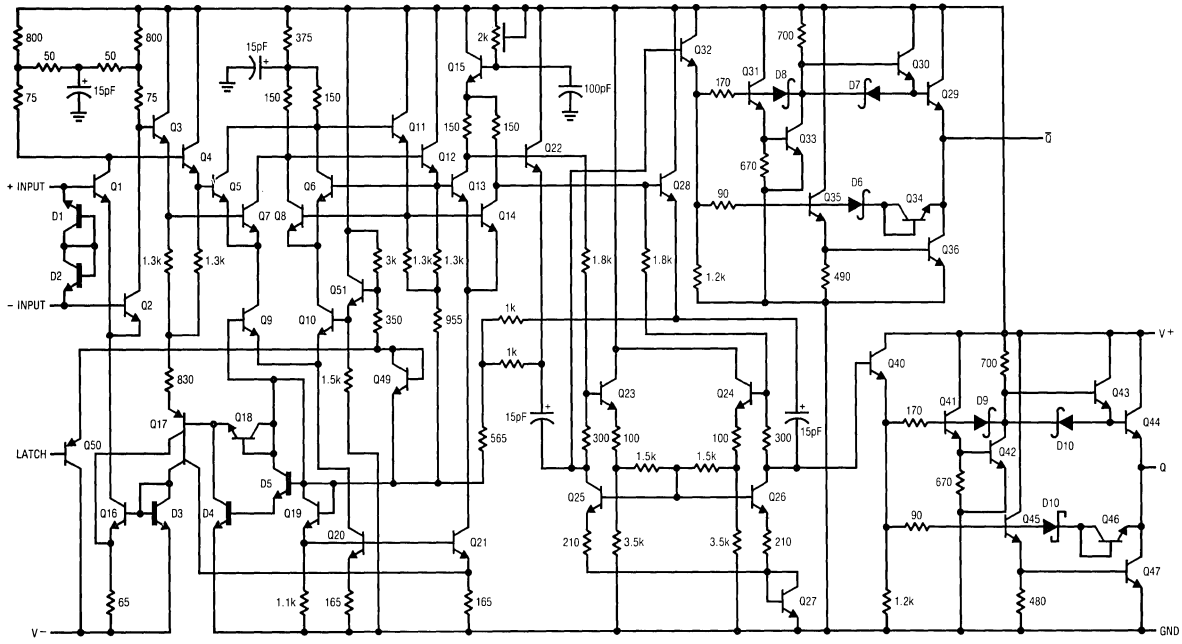


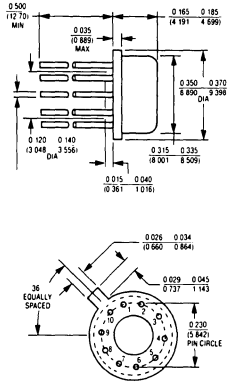
Figure A5

SCHEMATIC DIAGRAM



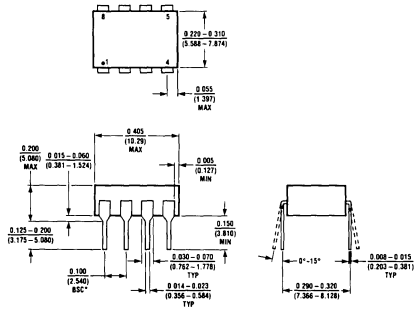
PACKAGE DESCRIPTION Dimensions in inches (millimeters) unless otherwise noted.

10 Lead TO-5 Metal Can (H)



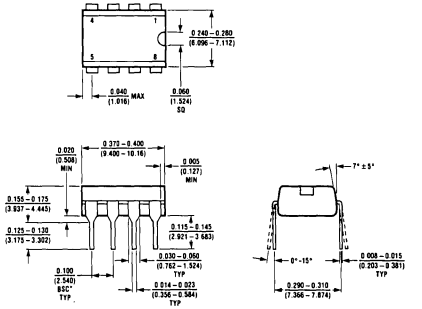
	T_j MAX	Θ_{jA}	Θ_{jC}
LT119AH LM119H	150°C	150°C/W	45°C/W
LT319AH LM319H	85°C	150°C/W	45°C/W

J8 Package
8 Lead Hermetic Dip



$T_j$max	Θ_{ja}
150°C	100°C/W

N8 Package
8 Lead Plastic



$T_j$max	Θ_{ja}
100°C	130°C/W

Micropower Dual Comparator

FEATURES

- Maximum Offset Voltage 1mV
- Maximum Bias Current 15nA
- Typical Output Drive 70mA
- Operates from 1.1V to 40V
- Internal Pull-Up Current
- Output Can Drive Loads Above V^+
- 30μA Supply Current (LT1017)
  110μA Supply Current (LT1018)

APPLICATIONS

- Power Supply Monitors
- Relay Driving
- Oscillators

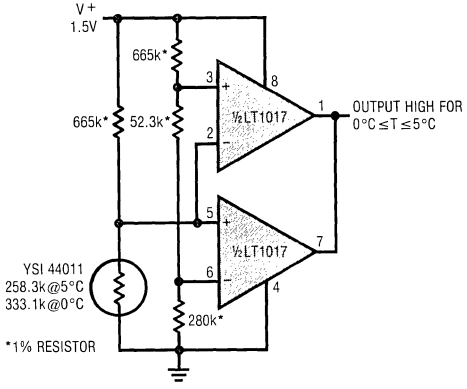
DESCRIPTION

The LT1017 and LT1018 are general purpose micropower comparators. The LT1017 is optimized for lowest operating power while the LT1018 operates at higher power and higher speed. Both devices can operate from a single 1.1V cell up to 40V. The output stage includes a class "B" pull-up current source, eliminating the need for an external resistive pull-up and saving power. The output stage is also designed to allow driving loads connected to a supply more positive than the device, as can comparators with open collector output stages.

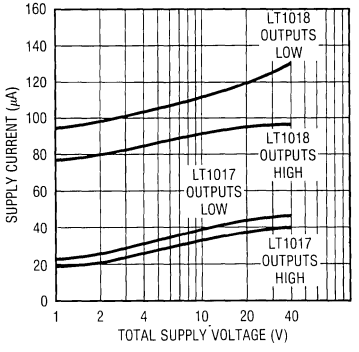
Input specifications are also excellent. On-chip trimming minimizes offset voltage, while high gain and common-mode rejection ratio keep other input-referred errors low. Common-mode voltage range includes ground. Special circuitry prevents false output states even if the input is overdriven.

The LT1017 and LT1018 are pin compatible with older dual comparators such as 393 type devices.

1.5V Powered Refrigerator Alarm



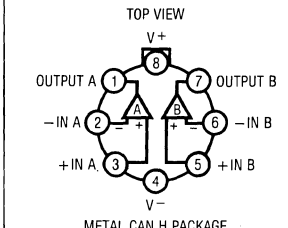
Supply Current



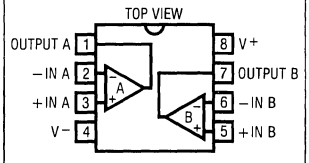
ABSOLUTE MAXIMUM RATINGS

Supply Voltage 40V
Differential Input Voltage 40V
Input Voltage ..... – 0.3V to 40V
Short Circuit Duration ..... Indefinite
Operating Temperature Range
LT1017M, LT1018M ..... – 55°C to 125°C
LT1017C, LT1018C ..... 0°C to 70°C
Storage Temperature Range ..... – 65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



METAL CAN H PACKAGE



PLASTIC DIP N8 PACKAGE

ORDER PART NUMBER

LT1017MH, LT1017CH
LT1018MH, LT1018CH
LT1017CN8
LT1018CN8

ELECTRICAL CHARACTERISTICS

PARAMETER	CONDITIONS		LT1017			LT1018			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Offset Voltage (Note 1)	$\pm 0.75V \le V_S \le \pm 20V$	25°C		0.4	1		0.4	1	mV
		●		0.5	1.4		0.5	1.4	mV
		125°C			1.5		0.7	1.5	mV
Bias Current	$\pm 0.75V \le V_S \le \pm 20V$	25°C		5	15		15	75	nA
		●		7	25		18	100	nA
		125°C		10	40			110	nA
Offset Current	$\pm 0.75V \le V_S \le \pm 20V$	25°C		0.4	2		1	8	nA
		●		0.5	3		1.6	12	nA
		125°C			5			20	nA
Common-Mode Rejection Ratio	$V_S = \pm 20V$, $-20V \le V_{CM} \le 19.1V$	25°C	105	115		105	115		dB
		●	100	115		100	115		dB
		125°C	86	100		95	110		dB
Power Supply Rejection Ratio	$\pm 0.75V \le V_S \le \pm 20V$	25°C	96	110		96	110		dB
		●	95	105		95	105		dB
		125°C	86			86	100		dB
Gain	No Load, $V_{OUT} = \pm 19.9V$ (Note 2)	25°C	110	115		110	125		dB
		●	105	115		105	120		dB
		125°C	100			100			dB
	$R_L = 4k$, $V_{OUT} = \pm 19V$	25°C	100	110		100	110		dB
		●	94			94			dB
Output Sink Current	$V^+ = 4.5V$, $V^- = 0$ Overdrive > 30mV	25°C	30	65		35	70		mA
		●	25	50		25	50		mA
		125°C	10	20		10	30		mA
Output Source Current	$V^+ = 40V$, $V^- = 0$ $V_{IN} = 5mV$, $V_{OUT} = 0.4V$	25°C	30	75		75	250		μA
		●	25	70		50	220		μA
		125°C	25	75		50	200		μA
Output Source Current	$V^+ = 1.2V$, $V^- = 0$ $V_{IN} = 5mV$, $V_{OUT} = 0.4V$	25°C	25	35		70	140		μA
		●	15	20		45	120		μA
		125°C	25	40		40	110		μA

ELECTRICAL CHARACTERISTICS

PARAMETER	CONDITIONS			LT1017 MIN	LT1017 TYP	LT1017 MAX	LT1018 MIN	LT1018 TYP	LT1018 MAX	UNITS
Negative Output Saturation	$I_{OUT}=0$	$V^+=4.5V, V^-=0$	25°C		5	20		5	15	mV
	$=0.1mA$	$V_{IN}=-10mV$	25°C		35	60		35	60	mV
	$=1mA$		25°C		60	120		60	120	mV
	$=10mA$		25°C		120	200		120	250	mV
	$=30mA$		25°C		350	600		350	700	mV
	$I_{OUT}=0$		●		5	20		8	20	mV
	$=0.1mA$		●		40	75		35	70	mV
	$=1mA$		●		75	150		70	150	mV
	$=10mA$		●		150	300		150	300	mV
	$=30mA$		●		600	900		500	900	mV
	$I_{OUT}=0$		125°C		25	50		10	40	mV
	$=0.1mA$		125°C		60	100		60	100	mV
	$=1mA$		125°C		100	200		110	200	mV
	$=10mA$		125°C		300	600		300	400	mV
	$=30mA$		125°C					900		mV
Positive Output Saturation	$I_{OUT}=0$		25°C		40	80		35	80	mV
	$=10\mu A$		25°C		175	250		175	250	mV
	$=0$		●		45	90		45	90	mV
	$=10\mu A$		●		190	300		190	300	mV
	$=0$		125°C		50	100		50	100	mV
	$=10\mu A$		125°C			300			300	mV
Leakage Current	$V_S=5V, V_{OUT}=40V$		25°C		0.5	3		1	8	µA
	$V_{IN}\geq 100mV$		●		0.6	3		1.8	10	µA
			125°C			5			15	µA
Supply Current	$V_S=5V$		25°C		30	60		110	250	µA
			●		40	80		110	250	µA
			125°C			80			300	µA
	$V_S=40V$		25°C		40	90		130	250	µA
			●		55	100		140	270	µA
			125°C			100			300	µA
Minimum Operating Voltage	$I_{OUT}=1mA$		25°C			1.15			1.2	V
			●			1.15			1.2	V
			125°C			1.15			1.2	V

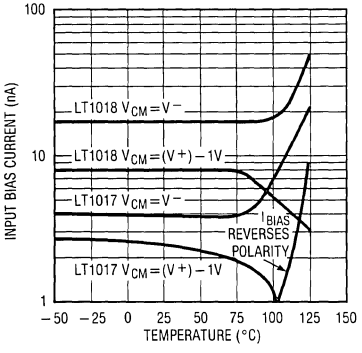
The ● denotes specifications which apply over operating temperature range of −55°C to 85°C for M grade parts and 0°C to 70°C for C grade parts.

Note 1: Offset voltage is guaranteed over a common-mode voltage range of $V^- \leq V_{IN} \leq (V^+ - 0.9V)$.

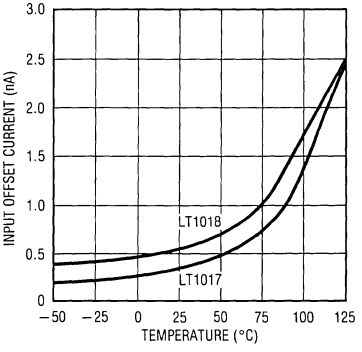
Note 2: No load gain is guaranteed but not tested (LT1017 only).

TYPICAL PERFORMANCE CHARACTERISTICS

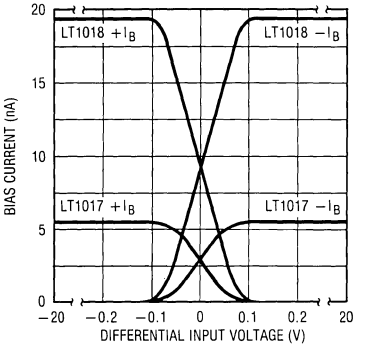
Input Bias Current



Input Offset Current

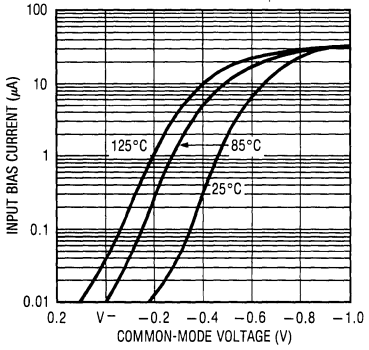


Bias Current vs Differential Input

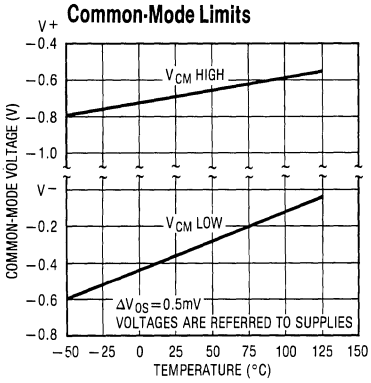


TYPICAL PERFORMANCE CHARACTERISTICS

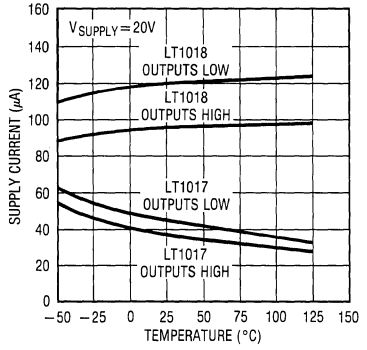
Input Bias Current with Inputs Driven Below the Supply



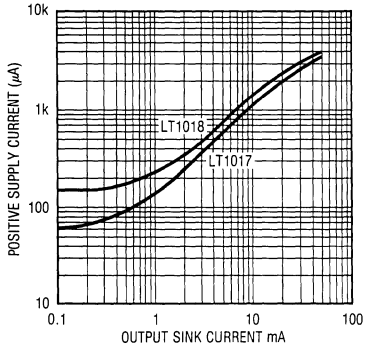
Common-Mode Limits



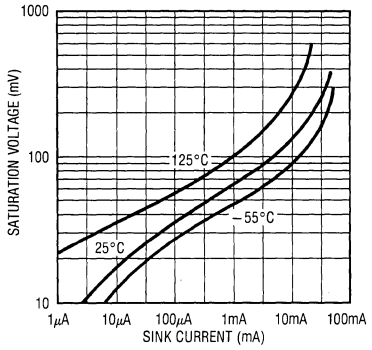
Supply Current



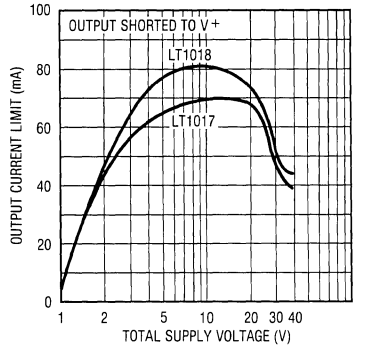
Positive Supply Current



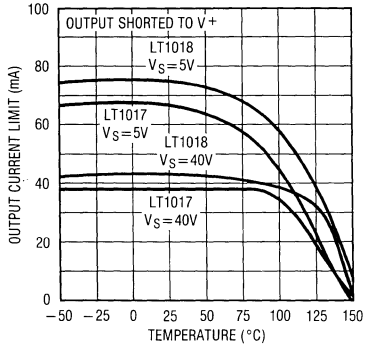
NPN Output Saturation Voltage



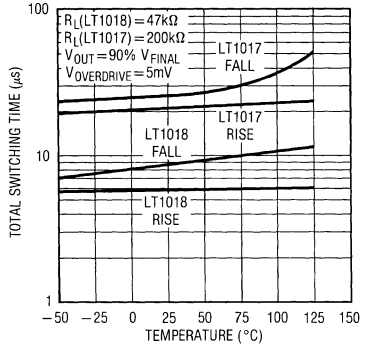
Output Sinking Current Limit



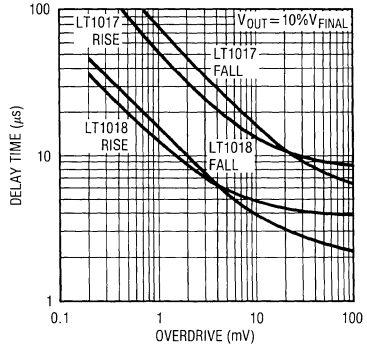
Output Sinking Current Limit



Total Switching Time

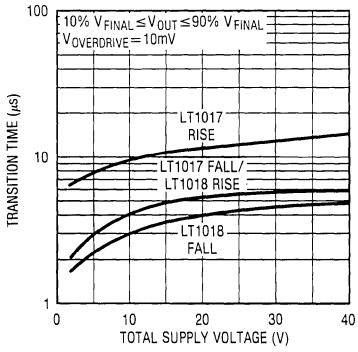


Output Delay

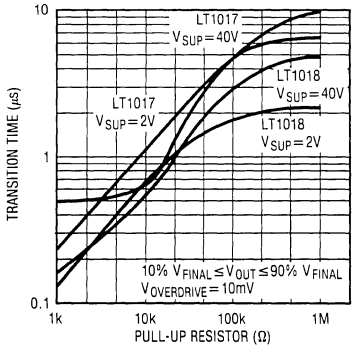


TYPICAL PERFORMANCE CHARACTERISTICS

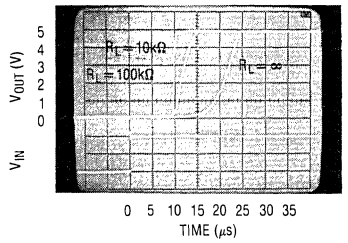
Transition Time



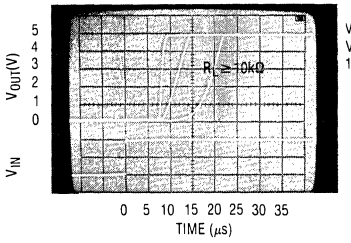
Positive Transition Time



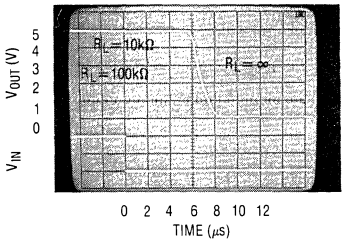
LT1017 Response Time



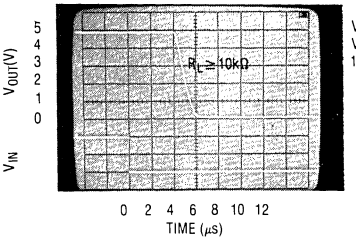
LT1017 Response Time



LT1018 Response Time

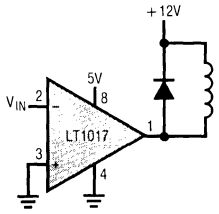


LT1018 Response Time

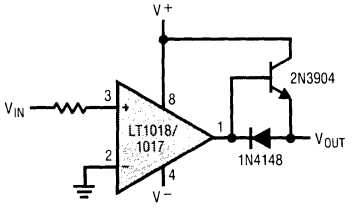


APPLICATIONS

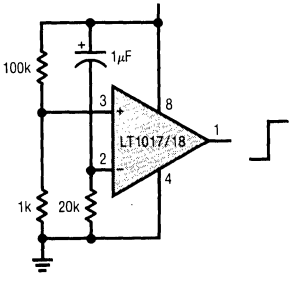
Driving Relays



Increasing Positive Output Current

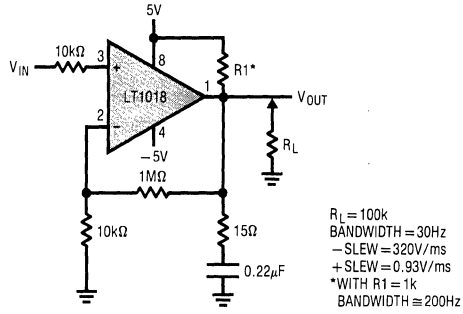


Delay On Power Up

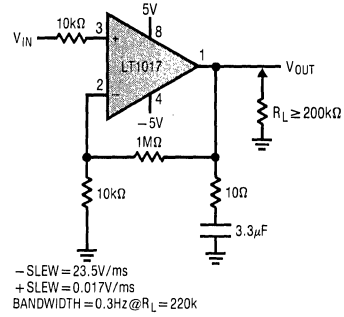


APPLICATIONS

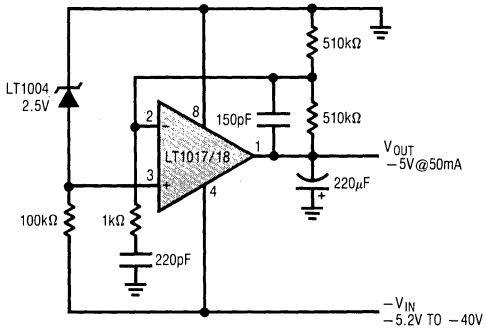
LT1018 Op Amp, $A_V = 100$



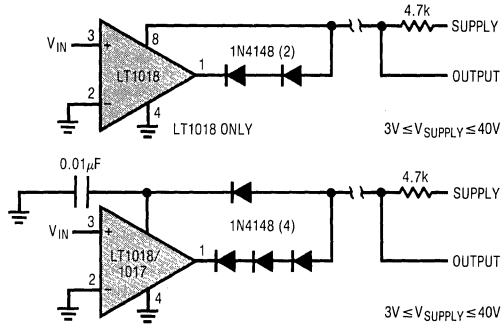
LT1017 Op Amp, $A_V = 100$



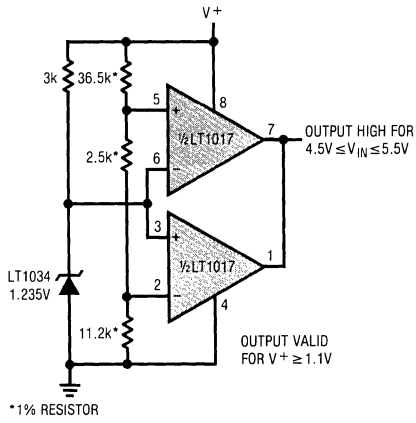
Negative Voltage Regulator



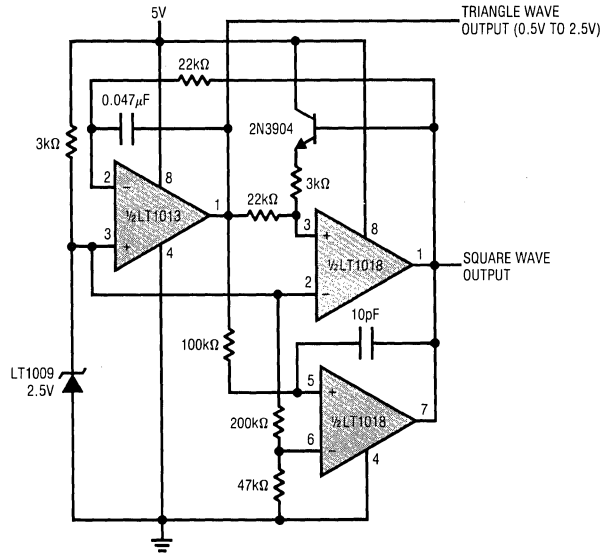
2-Wire Comparator



5V Power Supply Monitor

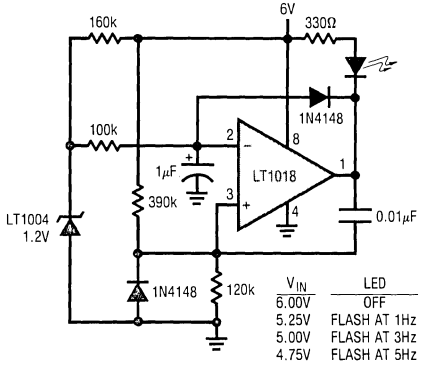


Precise Tri-Wave Generator

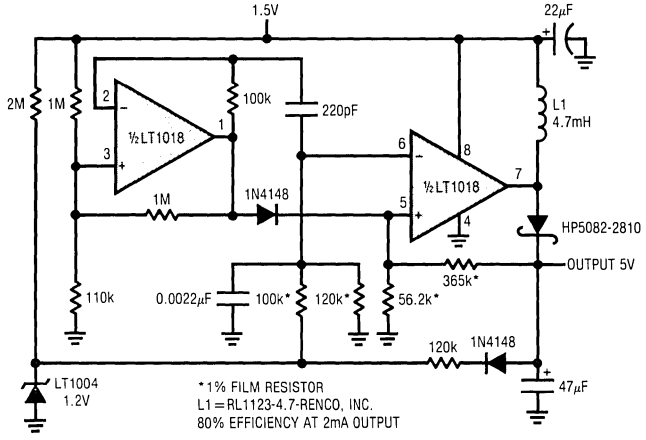


APPLICATIONS

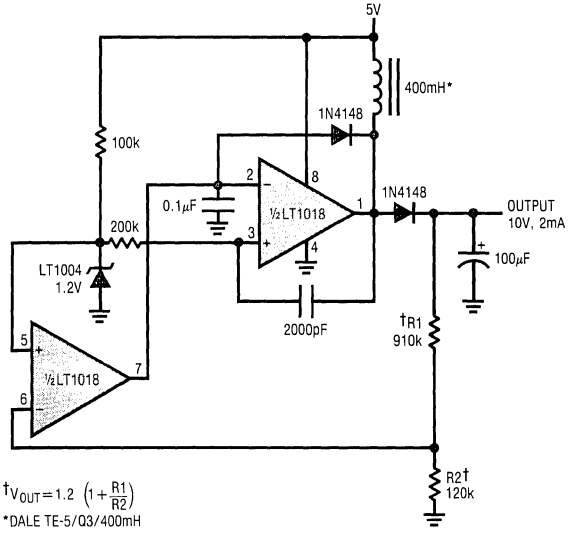
Power Supply Monitor



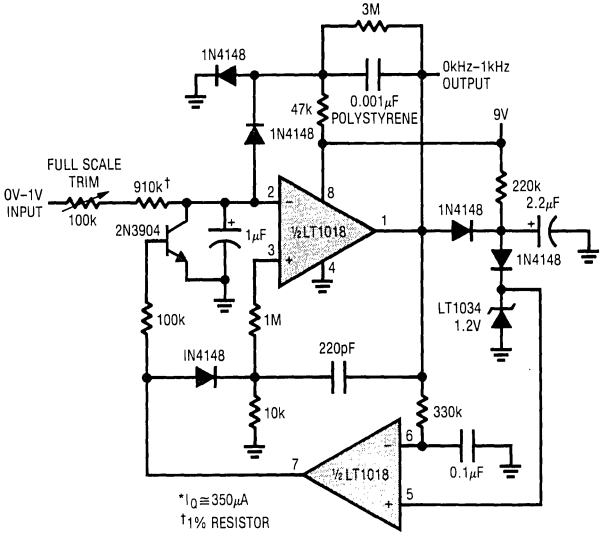
1.5V Input Flyback Regulator



Regulated Up Converter

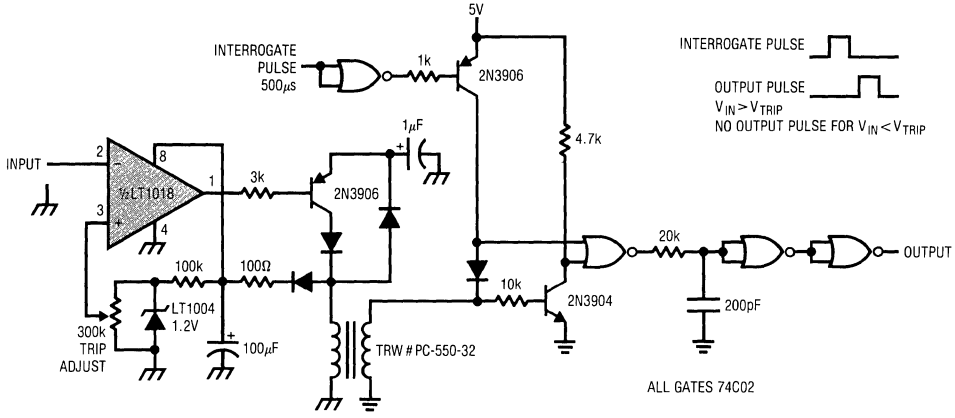


Low Power* V to F Converter



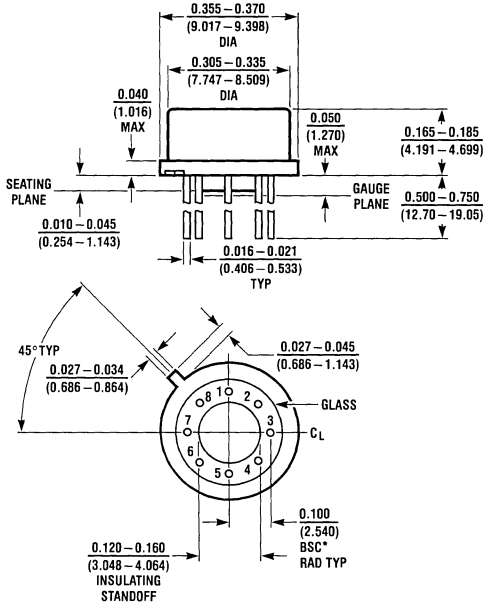
APPLICATIONS

Fully Isolated Limit Comparator



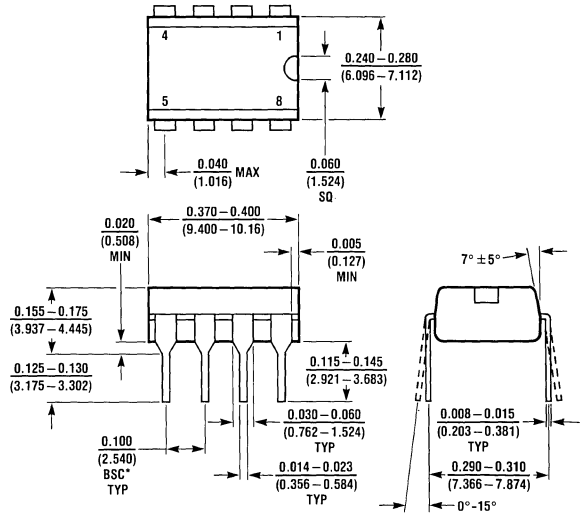
PACKAGE DESCRIPTION

H Package
Metal Can



Tj max	θja	θjc
150°C	150°C/W	45°C/W

N8 Package
8 Lead Plastic



Tj max	θja
100°c	130°C/W

Dual Micropower Comparator

FEATURES

- Micropower
  1.5μW (1 Sample/Second)
- Power Supply Flexibility
  Single Supply +2.8V to +16V
  Split Supply ±2.8V to ±8V
- *Guaranteed* Max. Offset 0.5mV
- *Guaranteed* Max. Tracking Error between Input Pairs ±0.1%
- Input Common-Mode Range to Both Supply Rails
- TTL/CMOS Compatible with ±5V or Single +5V Supply
- Input Errors are Stable with Time and Temperature

APPLICATIONS

- Battery Powered Systems
- Remote Sensing
- Window Comparator
- BANG-BANG Controllers

DESCRIPTION

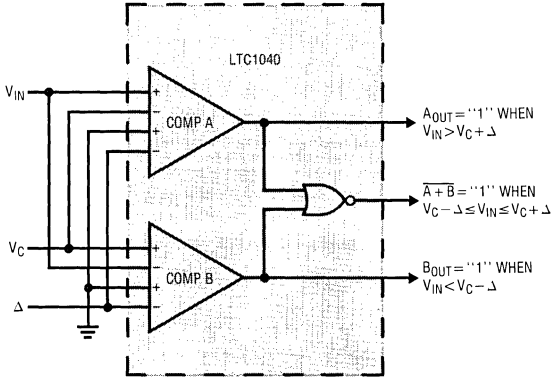
The LTC1040 is a monolithic CMOS dual comparator manufactured using Linear Technology's enhanced LTCMOS™ silicon gate process. Extremely low operating power levels are achieved by internally switching the comparator ON for short periods of time. The CMOS output logic holds the output information continuously while not consuming any power.

In addition to switching power ON, a switched output is provided to drive external loads during the comparator's active time. This allows not only low comparator power, but low total system power.

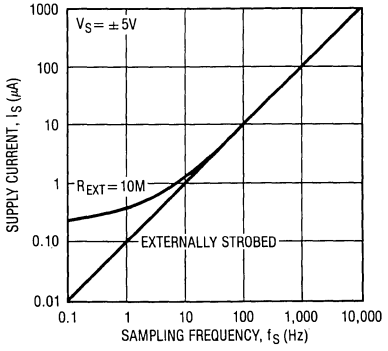
Sampling is controlled by an external strobe input or an internal oscillator. The oscillator frequency is set by an external RC network.

Each comparator has a unique input structure, giving two differential inputs. The output of the comparator will be high if the algebraic sum of the inputs is positive and low if the algebraic sum of the inputs is negative.

Window Comparator with Symmetric Window Limits



Typical LTC1040 Supply Current vs Sampling Frequency

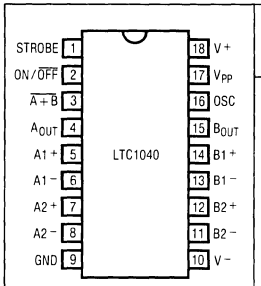


LTCMOS™ is a trademark of Linear Technology Corporation.

ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage (V^+ to V^-) 18V
Input Voltage ..... ($V^+ + 0.3V$) to ($V^- - 0.3V$)
Operating Temperature Range
LTC1040C ..... $-40°C$ to $85°C$
LTC1040M ..... $-55°C$ to $125°C$
Storage Temperature Range ..... $-55°C$ to $150°C$
Lead Temperature (Soldering, 10 sec.) ..... 300°C
Output Short Circuit Duration ..... Continuous

PACKAGE/ORDER INFORMATION



TEMPERATURE RANGE	ORDER PART NUMBER
−55°C to 125°C	LTC1040MJ
−40°C to 85°C	LTC1040CN
	LTC1040CJ

ELECTRICAL CHARACTERISTICS

Test conditions: $V^+ = 5V$, $V^- = -5V$, $T_{MIN} \leq T_A \leq T_{MAX}$ unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		LTC1040M/LTC1040C MIN	TYP	MAX	UNITS
V_{OS}	Offset Voltage (Note 1)	Split Supplies ±2.8V to ±6V Single Supply (V^- = GND) +2.8V to 6V	●		±0.3	±0.5	mV
		Split Supplies ±6V to ±8V Single Supply (V^- = GND) +6V to +15V	●		±1	±3	mV
	Tracking Error between Input Pairs (Notes 1 and 2)	Split Supplies ±2.8V to ±8V Single Supplies (V^- = GND) +2.8 to +16V	●		0.05	0.1	%
I_{BIAS}	Input Bias Current	$T_A = 25°C$, OSC = GND			±0.3		nA
R_{IN}	Average Input Resistance	f_S = 1kHz (Note 3)	●	20	30		MΩ
CMR	Common-Mode Range		●	V^-		V^+	V
PSR	Power Supply Range	Split Supplies	●	±2.8		±8	V
		Single Supplies (V^- = GND)	●	+2.8		+16	V
$I_{S(ON)}$	Power Supply ON Current (Note 4)	$V^+ = 5V$, V_{PP} On	●		1.2	3	mA
$I_{S(OFF)}$	Power Supply OFF Current (Note 4)	$V^+ = 5V$, V_{PP} Off LTC1040C LTC1040M	● ●		0.001 0.001	0.5 5	μA μA
t_D	Response Time (Note 5)	$T_A = 25°C$		60	80	100	μs
	A, B, $\overline{A+B}$ and ON/$\overline{OFF}$ Outputs (Note 6)						
V_{OH}	Logic "1" Output Voltage	$V^+ = 4.75V$, $I_{OUT} = -360\mu A$	●	2.4	4.4		V
V_{OL}	Logic "0" Output Voltage	$V^+ = 4.75V$, $I_{OUT} = 1.6mA$	●		0.25	0.4	V
	STROBE Input (Note 6)						
V_{IH}	Logic "1" Input Voltage	$V^+ = 5.25V$	●	2.0	1.6		V
V_{IL}	Logic "0" Input Voltage	$V^+ = 4.75V$			1.0	0.8	V
R_{EXT}	External Timing Resistor	Resistor Tied between V^+ and OSC Pin	●	100		10,000	kΩ
f_S	Sampling Frequency	$T_A = 25°C$, $R_{EXT} = 1M\Omega$, $C_{EXT} = 0.1\mu F$			5		Hz

The ● denotes the specifications which apply over the full operating temperature range.

Note 1: Applies over input voltage range limit and includes gain uncertainty.

Note 2: Tracking error = $(V_{IN1} - V_{IN2})/V_{IN1}$.

Note 3: R_{IN} is guaranteed by design and is not tested. $R_{IN} = 1/(f_S \times 33pF)$.

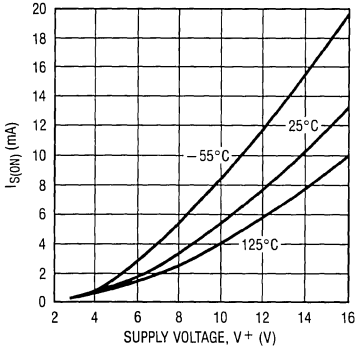
Note 4: Average supply current = $t_D \times I_{S(ON)} \times f_S + (1 - t_D \times f_S) \times I_{S(OFF)}$.

Note 5: Response time is set by an internal oscillator and is independent of overdrive voltage.

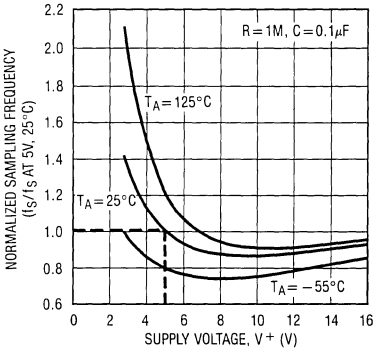
Note 6: Inputs and outputs also capable of meeting EIA/JEDEC B series CMOS specifications.

TYPICAL PERFORMANCE CHARACTERISTICS

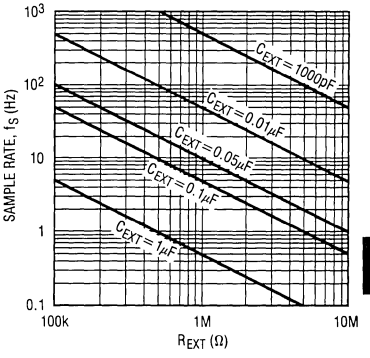
Peak Supply Current vs Supply Voltage



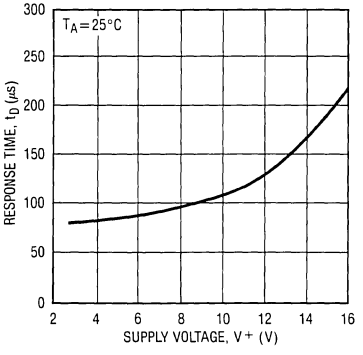
Normalized Sampling Frequency vs Supply Voltage and Temperature



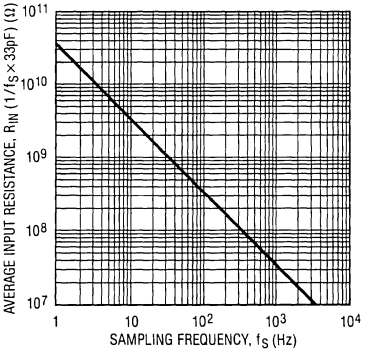
Sampling Rate vs R_{EXT}, C_{EXT}



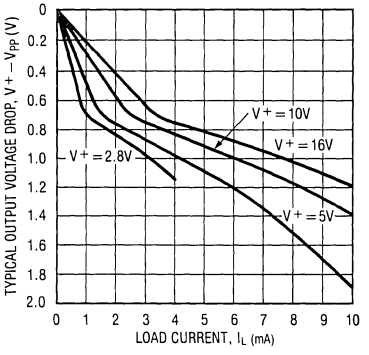
Response Time vs Supply Voltage



Input Resistance vs Sampling Frequency

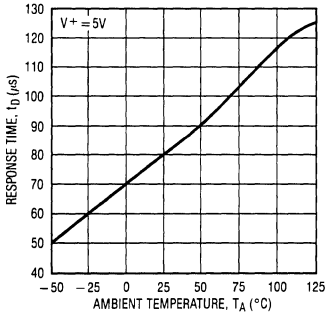


V_{PP} Output Voltage vs Load Current



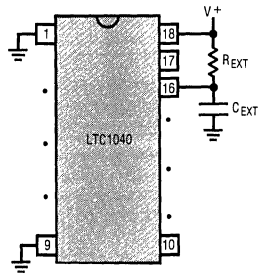
TYPICAL PERFORMANCE CHARACTERISTICS

Response Time vs Temperature

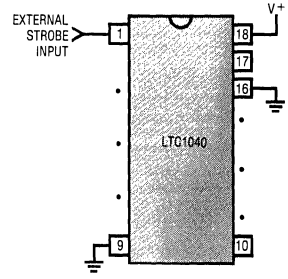


Quick Hookup Guide

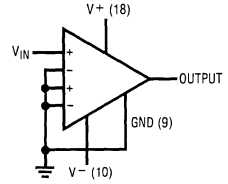
Self-Oscillating



External Strobe

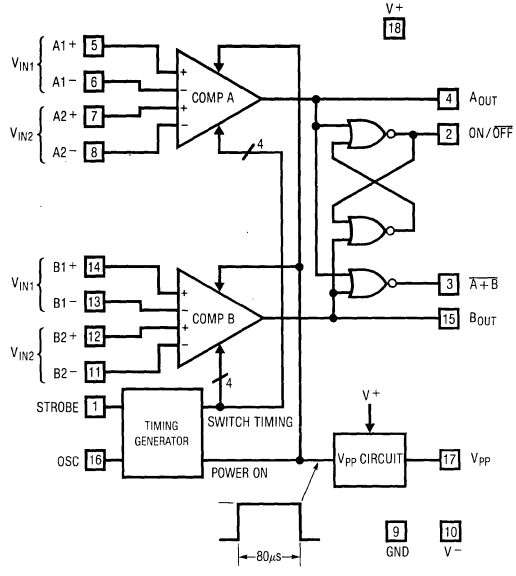


TEST CIRCUIT



ALL INPUTS ON OPPOSITE COMPARATOR AT GROUND

BLOCK DIAGRAM



APPLICATIONS INFORMATION

The LTC1040 uses sampled data techniques to achieve its unique characteristics. Some of the experience acquired using classic linear comparators does not apply to this circuit, so a brief description of internal operation is essential to proper application.

The most obvious difference between the LTC1040 and other comparators is the dual differential input structure. Functionally, when the sum of inputs is positive, the comparator output is high and when the sum of the inputs is negative, the output is low. This unique input structure is achieved with CMOS switches and a precision capacitor array. Because of the switching nature of the inputs, the concept of input current and input impedance needs to be examined.

The equivalent input circuit is shown in Figure 1. Here, the input is being driven by a resistive source, R_S, with a bypass capacitor, C_S. The bypass capacitor may or may not be needed, depending on the size of the source resistance and the magnitude of the input voltage, V_{IN}.

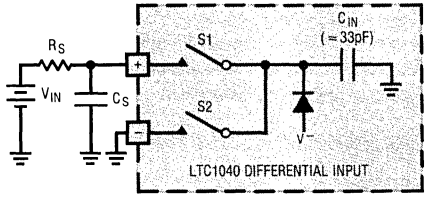


Figure 1. Equivalent Input Circuit

For $R_S < 10k\Omega$

Assuming C_S is zero, the input capacitor, C_{IN}, charges to V_{IN} with a time constant of $R_S C_{IN}$. When R_S is too large, C_{IN} does not have a chance to fully charge during the sampling interval ($\approx 80\mu s$) and errors will result. If R_S exceeds 10kΩ a bypass capacitor is necessary to minimize errors.

For $R_S > 10k\Omega$

For R_S greater than 10kΩ, C_{IN} cannot fully charge and a bypass capacitor, C_S, is needed. When switch S1 closes, charge is shared between C_S and C_{IN}. The change in voltage on C_S because of this charge sharing is:

$$\Delta V = V_{IN} \times \frac{C_{IN}}{C_{IN} + C_S}$$

This represents an error and can be made arbitrarily small by increasing C_S.

With the addition of C_S a second error term caused by the finite input resistance of the LTC1040 must be considered. Switches S1 and S2 alternately open and close, charging and discharging C_{IN} between V_{IN} and ground. The alternate charge and discharge of C_{IN} causes a current to flow into the positive input and out of the negative input. The magnitude of this current is:

$$I_{IN} = q \times f_S = V_{IN}\ C_{IN}\ f_S$$

where f_S is the sampling frequency. Because the input current is directly proportional to input voltage, the LTC1040 can be said to have an average input resistance of:

$$R_{IN} = \frac{V_{IN}}{I_{IN}} = \frac{1}{f_S\ C_{IN}} = \frac{1}{f_S \times 33pF}$$

(see typical curve of R_{IN} vs f_S). A voltage divider is set up between R_S and R_{IN} causing error.

The input voltage error caused by these two effects is:

$$V_{ERROR} = V_{IN} \left(\frac{C_{IN}}{C_{IN} + C_S} + \frac{R_S}{R_S + R_{IN}} \right).$$

Example: $f_S = 10Hz$, $R_S = 1M\Omega$,
$C_S = 1\mu F$, $V_{IN} = 1V$

$$V_{ERROR} = 1V \left(\frac{33 \times 10^{-12}}{1 \times 10^{-6}} + \frac{10^6}{10^6 + 3 \times 10^9} \right)$$

$$= 33\mu V + 330\mu V = 363\mu V.$$

Notice that most of the error is caused by R_{IN}. If the sampling frequency is reduced to 1Hz, the voltage error is reduced to 66μV.

APPLICATIONS INFORMATION

Minimizing Comparison Errors

The two differential input voltages, V1 and V2, are converted to charge by the input capacitors C_{IN1} and C_{IN2} (see Figure 2). The charge is summed at the virtual ground point and if the net charge is positive, the comparator output is high and if negative, it is low. There is an optimum way to connect these inputs, in a specific application, to minimize error.

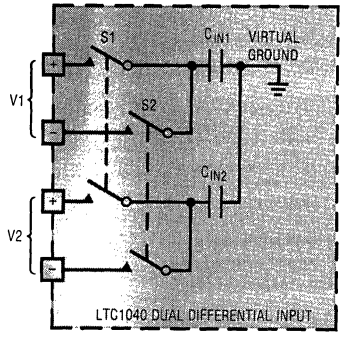


Figure 2. Dual Differential Equivalent Input Circuit

Ignoring internal offset, the LTC1040 will be at its switching point when:

$$V1 \times C_{IN1} + V2 \times C_{IN2} = 0.$$

Optimum error will be achieved when the differential voltages, V1 and V2, are individually minimized. Figure 3 shows two ways to connect the LTC1040 to compare an input voltage, V_{IN}, to a reference voltage, V_{REF}. Using the above equation, each method will be at null when:

(a) $(V_{REF} - 0V)\ C_{IN1} - (0V - V_{IN})\ C_{IN2} = 0$
or $V_{IN} = V_{REF}\ (C_{IN1}/C_{IN2})$

(b) $(V_{REF} - V_{IN})\ C_{IN1} - (0V - 0V)\ C_{IN2} = 0$
or $V_{IN} = V_{REF}$.

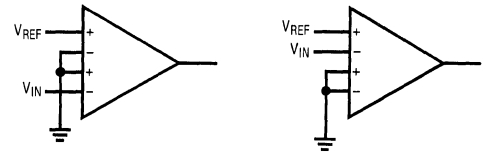
Notice that in method (a) the null point depends on the ratio of C_{IN1}/C_{IN2}, but method (b) is independent of this ratio. Also, because method (b) has zero differential input voltage, the errors due to finite input resistance are negligible. The LTC1040 has a high accuracy capacitor array and even the non-optimum connection will only result in ±0.1% more error worst-case compared to the optimum connection.

Tracking Error

Tracking error is caused by the ratio error between C_{IN1} and C_{IN2} and is expressed as a percentage. For example, consider Figure 3(a) with $V_{REF} = 1V$. Then at null,

$$V_{IN} = V_{REF}\ \frac{C_{IN1}}{C_{IN2}} = 1V \pm 1mV$$

because C_{IN1} is guaranteed to equal C_{IN2} to within 0.1%.



(a) OK (b) Optimum

Figure 3. Two Ways to Do It

Common-Mode Range

The input switches of the LTC1040 are capable of switching to either the V^+ or V^- supply. This means that the input common-mode range includes both supply rails. Many applications, not feasible with conventional comparators, are possible with the LTC1040. In the load current detector shown in Figure 4, a 0.1Ω resistor is used to sense the current in the V^+ supply. This application requires the dual differential input and common-mode capabilities of the LTC1040.

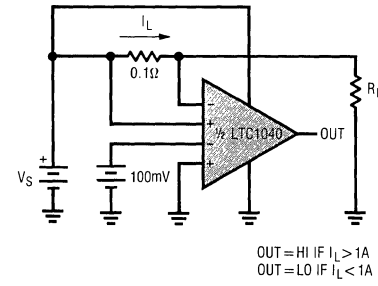


Figure 4. Load Current Detector

APPLICATIONS INFORMATION

Offset Voltage Error

The errors due to offset, common-mode, power supply variation, gain and temperature are all included in the offset voltage specification. This makes it easy to compute the error when using the LTC1040.

Example: error computation for Figure 4.
Assume: $2.8V \leq V_S \leq 6V$.
Then total worst-case error is:

$$I_{L(ERROR)} = \pm(100mV \times 0.001 + 0.5mV) \times \frac{1A}{100mV} = \pm 6mA$$

(Tracking Error, V_{OS})

$$I_{L(ERROR)}\% = \frac{6mA}{1A} \times 100 = \pm 0.6\%.$$

Note: If source resistance exceeds 10kΩ, bypass capacitors should be used and the associated errors must be included.

Pulsed Power (V_{PP}) Output

It is often desirable to use comparators with resistive networks such as bridges. Because of the extremely low power consumption of the LTC1040, the power consumed by these resistive networks can far exceed that of the device itself.

At low sample rates the LTC1040 spends most of its time off. To take advantage of this, a pulsed power (V_{PP}) output is provided. V_{PP} is switched to V^+ when the comparator is on and to a high impedance (open circuit) when the comparator is off. The ON time is nominally 80μs. Figure 5 shows the V_{PP} output circuit.

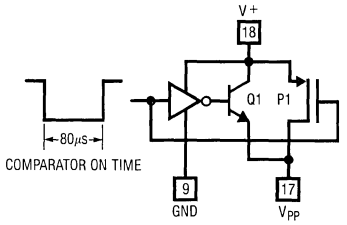


Figure 5. V_{PP} Output Switch

The V_{PP} output voltage is not precise (see V_{PP} Output Voltage versus Load Current curve). There are two ways V_{PP} can be used to power external networks without excessive errors: (1) ratiometric networks and (2) fast settling references.

In a ratiometric network (see Figure 6), the inputs are all proportional to V_{PP}. Consequently, for small changes, the absolute value of V_{PP} does not affect accuracy.

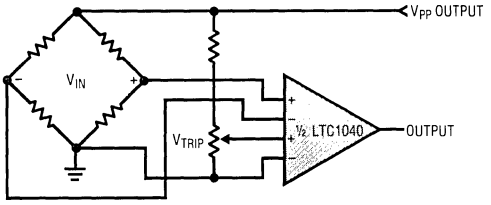


Figure 6. Ratiometric Network Driven by V_{PP}

It is critical that the inputs to the LTC1040 completely settle within 4μs of the start of the comparison cycle and that they do not change during the 80μs ON time. When driving resistive networks with V_{PP}, capacitive loading on the network should be minimized to meet the 4μs settling time requirement. It is not recommended that V_{PP} be used to drive networks with source impedances, as seen by the inputs, of greater than 10kΩ.

In applications where an absolute reference is required, the V_{PP} output can be used to drive a fast settling reference. The LT1009 2.5V reference, ideal in this application, settles in approximately 2μs (see Figure 7). The current through R1 must be large enough to supply the LT1009 minimum bias current (≈ 1mA) and the load current, I_L.

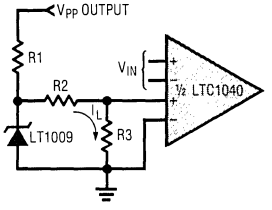


Figure 7. Driving Reference with V_{PP} Output

APPLICATIONS INFORMATION

Output Logic

In addition to the normal outputs (A_{OUT} and B_{OUT}), two additional outputs, $\overline{A+B}$ and ON/$\overline{OFF}$, are provided (see Figure 8 and Table I). All logic is powered from V^+ and ground, thus input and output logic levels are independent of the V^- supply. The LTC1040 is directly compatible with CMOS logic and is TTL compatible for $4.75V \leq V^+ \leq 5.25V$. No external pull-up resistors are required.

Table I. Output Logic Truth Table

ΣA INPUTS	ΣB INPUTS	A_{OUT}	B_{OUT}	$\overline{A+B}$	ON/$\overline{OFF}$
+	+	H	H	L	L
+	−	H	L	L	L
−	+	L	H	L	H
−	−	L	L	H	I*

*I = indeterminate. When both A and B outputs are low, the ON/$\overline{OFF}$ output remains in the state it was in prior to entering $A_{OUT} = B_{OUT} = L$.

Using External Strobe

A positive pulse on the strobe input, with the OSC input tied to ground, will initiate a comparison cycle. The STROBE input is edge-sensitive and pulse widths of 50ns will typically trigger the device.

Because of the sampling nature of the LTC1040, some sensitivity exists between the offset voltage and the falling edge of the input strobe. When the falling edge of the strobe signal falls within the comparator's active time (80μs after rising edge), offset changes of as much as 2mV can occur. To eliminate this problem, make sure the strobe pulse width is greater than the response time, t_D.

Using Internal Strobe

An internal oscillator allows the LTC1040 to strobe itself. The frequency of oscillation, and hence sampling rate, is set by an external RC network (see typical curve of frequency versus R_{EXT}, C_{EXT}).

For self-oscillation, the STROBE pin must be tied to ground. The external RC network is connected as shown in Figure 9.

To assure oscillation, R_{EXT} must be between 100k and 10M. There is no limit to the size of C_{EXT}.

R_{EXT} is very important in determining the power consumption. The average voltage at the oscillator pin is approximately $V^+/2$. The power consumed by R_{EXT} is then: $P_{REXT} = (V^+/2)^2/R_{EXT}$.

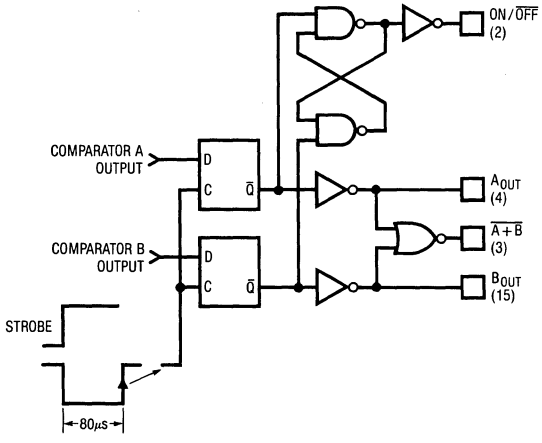


Figure 8. LTC1040 Logic Diagram

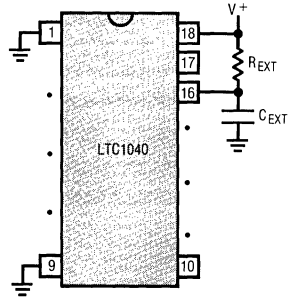


Figure 9. External RC Connection

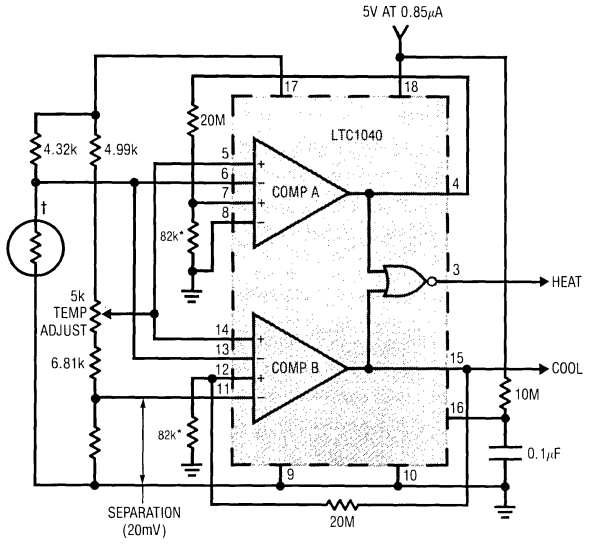
APPLICATIONS INFORMATION

Example: $R_{EXT} = 1M$, $V^+ = 5V$, $P_{REXT} = (2.5)^2/10^6 = 6.25 \times 10^{-6}W$.

This is about four times the power consumed by the LTC1040 at $V^+ = 5V$ and $f_S = 1$ sample/second. Where power is a premium R_{EXT} should be made as large as possible. Note that the power consumed by R_{EXT} is *not* a function of f_S or C_{EXT}.

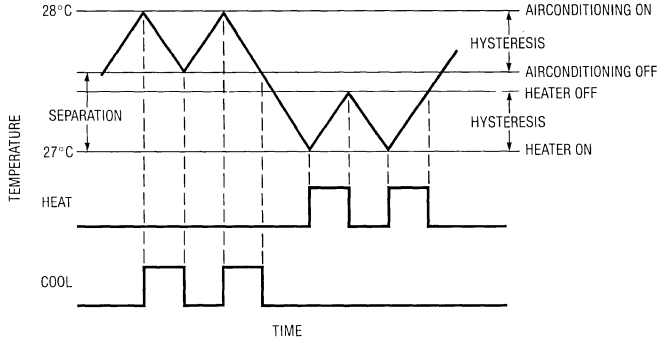
TYPICAL APPLICATIONS

Complete Heating/Cooling Automatic Thermostat



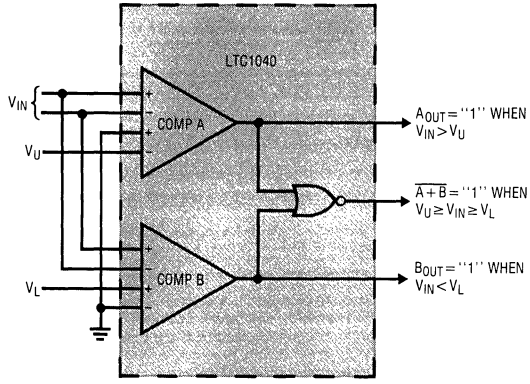
† THERMISTOR #44007
YELLOW SPRINGS INSTRUMENT CO., INC.

*HYSTERESIS $= 5V \times \frac{82k}{20M} = 20mV$

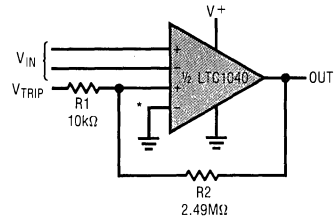


TYPICAL APPLICATIONS

Window Comparator with Independent Window Limits and Fully Floating Differential Input



Hysteresis Comparator with Fully Floating Differential Input



$$OUT = \text{"0" WHEN } V_{IN} > V_U = \frac{V_{TRIP}\,R2 + (5V)\,R1}{R1 + R2} = 0.996\,V_{TRIP} + 20mV$$

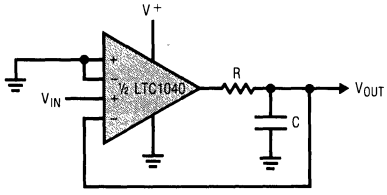
$$OUT = \text{"1" WHEN } V_{IN} < V1 = \frac{V_{TRIP}\,R2}{R1 + R2} = 0.996 V_{TRIP}$$

*TO CENTER HYSTERESIS ABOUT V_{TRIP} FORCE THIS INPUT TO HYSTERESIS/2 (10mV)

The LTC1040 as a Linear Amplifier

With a simple RC filter the LTC1040 can be made to function as a linear amplifier. By filtering the logic output and feeding it back to the negative input, the loop forces the output duty cycle [$t_{ON}/(t_{ON} + t_{OFF})$] so that V_{OUT} equals V_{IN} (Figure 10).

The RC time constant is set to keep the ripple on the output small. The maximum output ripple is: $\Delta V = V^+/f_S RC$ and should be set to 0.5mV to 1mV for best results. Notice that the higher the sampling frequency, f_S, the lower RC can be. This is important because the RC filter also sets the loop response. A convenient way to keep f_S as high as possible under all conditions is to connect a 100k resistor to pin 16 (OSC) with no capacitance to ground.



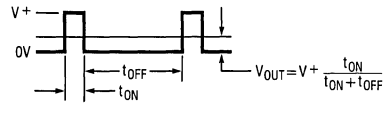
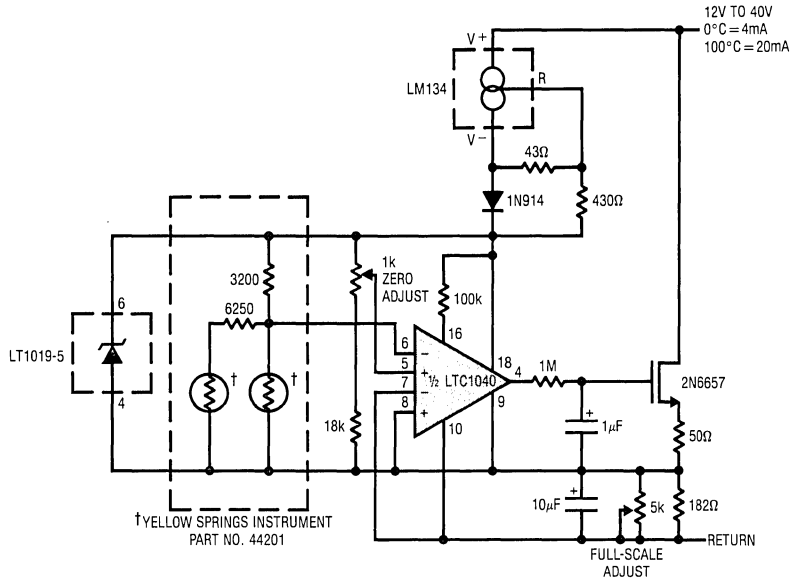


Figure 10. The LTC1040 as a Linear Amplifier

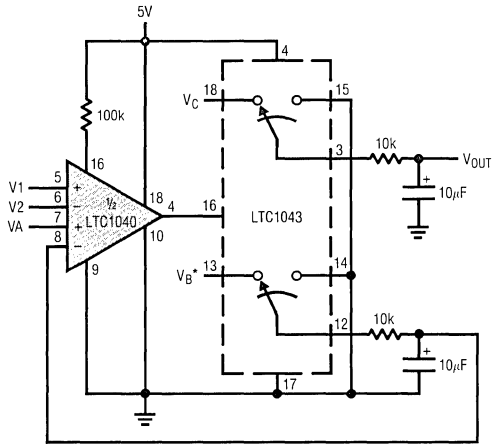
TYPICAL APPLICATIONS

2-Wire 0°C to 100°C Temperature Transducer with 4mA to 20mA Output



$$\text{ACCURACY} = \underset{\text{CIRCUIT ERROR AT 25°C}}{\pm 0.1°C} + \underset{\text{TRANSDUCER ERROR}}{\pm 0.2°C} = \pm 0.3°C$$

Analog Multiplier/Divider

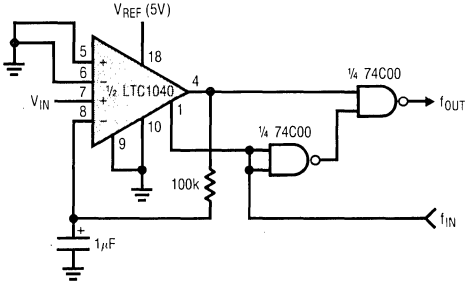


$$V_{OUT} = \frac{(V_A + V1 - V2) \times V_C}{V_B}$$

ACCURACY = ±10mV NO TRIM

*V_B MUST BE > V_A + (V1 – V2)

Single +5V Voltage-to-Frequency Converter

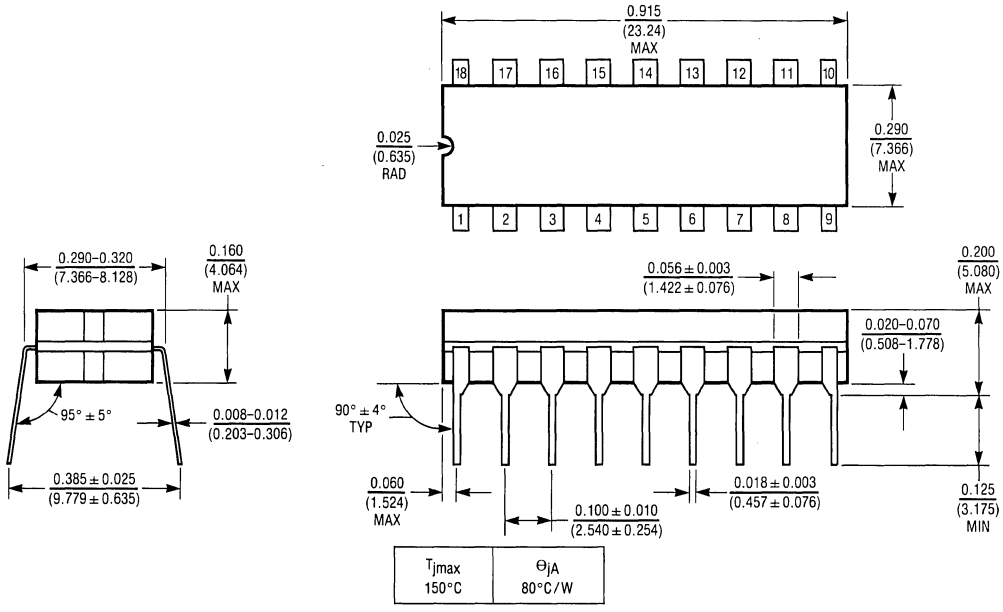


$$f_{OUT}\ (\text{AVERAGE}) = f_{IN} \frac{V_{IN}}{V_{REF}} \pm 0.1\%\ \text{FS}$$

PACKAGE DESCRIPTION

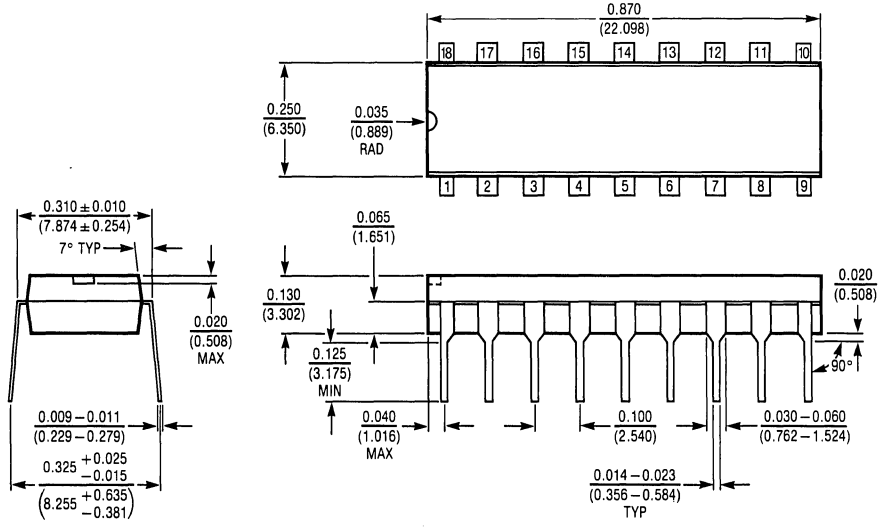
Dimensions in inches (millimeters) unless otherwise noted.

J Package
18 Lead Hermetic DIP



T_{jmax}	Θ_{jA}
150°C	80°C/W

N Package
18 Lead Plastic DIP



T_{jmax}	Θ_{jA}
110°C	120°C/W

BANG-BANG Controller

FEATURES

- Micropower 1.5μW (1 Sample/Second)
- Wide Supply Range 2.8V to 16V
- High Accuracy
  - *Guaranteed* SET POINT Error ±0.5mV Max.
  - *Guaranteed* Deadband ±0.1% of Value Max.
- Wide Input Voltage Range V^+ to Ground
- TTL Outputs with 5V Supply
- Two *Independent* Ground-Referred Control Inputs
- Small Size 8-Pin MiniDIP

APPLICATIONS

- Temperature Control (Thermostats)
- Motor Speed Control
- Battery Charger
- Any ON-OFF Control Loop

DESCRIPTION

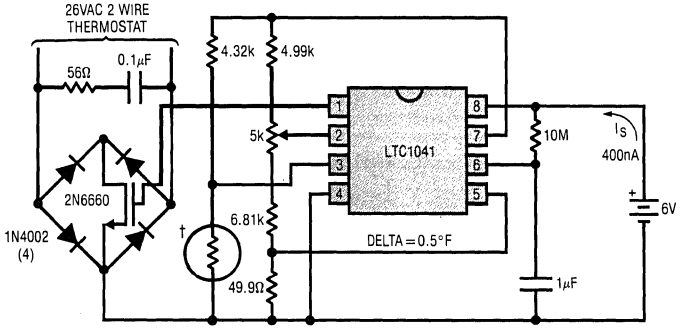
The LTC1041 is a monolithic CMOS BANG-BANG controller manufactured using Linear Technology's enhanced LTCMOS™ silicon gate process. BANG-BANG loops are characterized by turning the control element fully ON or fully OFF to regulate the average value of the parameter to be controlled. The SET POINT input determines the average control value and the DELTA input sets the deadband. The deadband is always 2 × DELTA and is centered around the SET POINT. Independent control of the SET POINT and deadband, with no interaction, is made possible by the unique sampling input structure of the LTC1041.

An external RC connected to the OSC pin sets the sampling rate. At the start of each sample, internal power to the analog section is switched on for ≈80μs. During this time the analog inputs are sampled and compared. After the comparison is complete, power is switched off. This achieves extremely low average power consumption at low sampling rates. CMOS logic holds the output continuously while consuming virtually no power.

To keep system power at an absolute minimum, a switched power output (V_{PP}) is provided. External loads, such as bridge networks and resistive dividers, can be driven by this switched output.

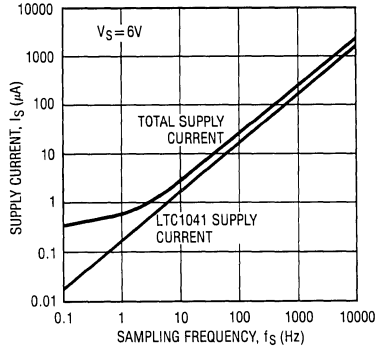
The output logic sense (i.e., ON = V^+) can be reversed (i.e., ON = GND) by interchanging the V_{IN} and SET POINT inputs. This has no other effect on the operation of the LTC1041.

Ultra Low Power 50°F to 100°F (2.4μW) Thermostat



ALL RESISTORS 1%.
†YELLOW SPRINGS INSTRUMENT CO., INC. P/N 44007 DRIVING THERMISTOR WITH V_{PP} ELIMINATES 3.8°F ERROR DUE TO SELF-HEATING.

Supply Current vs Sampling Frequency

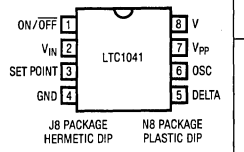


LTCMOS™ is a trademark of Linear Technology Corporation.

ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage (V^+ to V^-) 18V
Input Voltage ..... ($V^+ + 0.3V$) to ($V^- - 0.3V$)
Operating Temperature Range
LTC1041C ..... −40°C to 85°C
LTC1041M ..... −55°C to 125°C
Storage Temperature Range ..... −55°C to 150°C
Lead Temperature (Soldering, 10 sec.) ..... 300°C
Output Short Circuit Duration ..... Continuous

PACKAGE/ORDER INFORMATION



J8 PACKAGE HERMETIC DIP
N8 PACKAGE PLASTIC DIP

TEMPERATURE RANGE	ORDER PART NUMBER
−55°C to 125°C	LTC1041MJ8
−40°C to 85°C	LTC1041CN8

ELECTRICAL CHARACTERISTICS

Test Conditions: $V^+ = 5V$, $T_{MIN} \le T_A \le T_{MAX}$ unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		LTC1041M/LTC1041C MIN	TYP	MAX	UNITS
	SET POINT Error (Note 2)	$V^+ = 2.8V$ to 6V (Note 1)	●		±0.3 + ±0.05	±0.5 + ±0.1	mV % of DELTA
		$V^+ = 6V$ to 15V (Note 1)	●		±1 + ±0.05	±3 + ±0.1	mV % of DELTA
	Deadband Error (Note 3)	$V^+ = 2.8V$ to 6V (Note 1)	●		±0.6 + ±0.1	±1 + ±0.2	mV % of DELTA
		$V^+ = 6V$ to 15V (Note 1)	●		±2 + ±0.1	±6 + ±0.2	mV % of DELTA
I_{OS}	Input Current	$V^+ = 5V$, $T_A = 25°C$, OSC = GND (V_{IN}, SET POINT and DELTA Inputs)			±0.3		nA
R_{IN}	Equivalent Input Resistance	$f_S = 1kHz$ (Note 4)	●	10	15		MΩ
	Input Voltage Range		●	GND		V^+	V
PSR	Power Supply Range		●	2.8		16	V
$I_{S(ON)}$	Power Supply ON Current (Note 5)	$V^+ = 5V$, V_{PP} ON	●		1.2	3	mA
$I_{S(OFF)}$	Power Supply OFF Current (Note 5)	$V^+ = 5V$, V_{PP} OFF LTC1041C LTC1041M	● ●		0.001 0.001	0.5 5	μA μA
t_D	Response Time (Note 6)	$V^+ = 5V$		60	80	100	μs
V_{OH} V_{OL}	ON/$\overline{OFF}$ Output (Note 7) Logical "1" Output Voltage Logical "0" Output Voltage	$V^+ = 4.75V$, $I_{OUT} = -360\mu A$ $V^+ = 4.75V$, $I_{OUT} = 1.6mA$	●	2.4	4.4 0.25	 0.4	V V
R_{EXT}	External Timing Resistor	Resistor Connected between V^+ and OSC Pin	●	100		10,000	kΩ
f_S	Sampling Frequency	$V^+ = 5V$, $T_A = 25°C$, $R_{EXT} = 1M$ $C_{EXT} = 0.1\mu F$			5		Hz

The ● denotes the specifications which apply over the full operating temperature range. The shaded electrical specifications indicate those parameters which have been improved or guaranteed test limits provided for the first time.

Note 1: Applies over input voltage range limit and includes gain uncertainty.

Note 2: SET POINT error $\equiv \left(\frac{V_U + V_L}{2}\right) -$ SET POINT

where V_U = upper band limit and V_L = lower band limit.

Note 3: Deadband error $\equiv (V_U - V_L) - 2 \times$ DELTA where V_U = upper band limit and V_L = lower band limit.

Note 4: R_{IN} is guaranteed by design and is not tested. $R_{IN} = 1/(f_S \times 66pF)$.

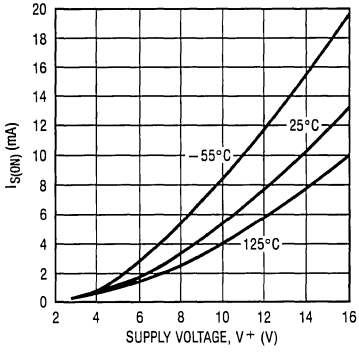
Note 5: Average supply current $= t_D \times I_{S(ON)} \times f_S + (1 - t_D \times f_S)\, I_{S(OFF)}$.

Note 6: Response time is set by an internal oscillator and is independent of overdrive voltage. $t_D = V_{PP}$ pulse width.

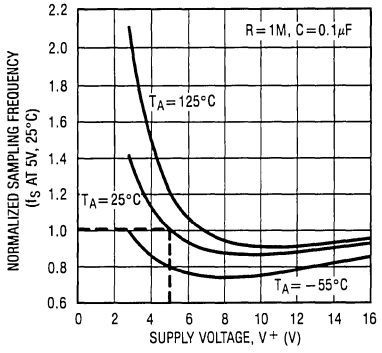
Note 7: Output also capable of meeting EIA/JEDEC standard B series CMOS drive specifications.

TYPICAL PERFORMANCE CHARACTERISTICS

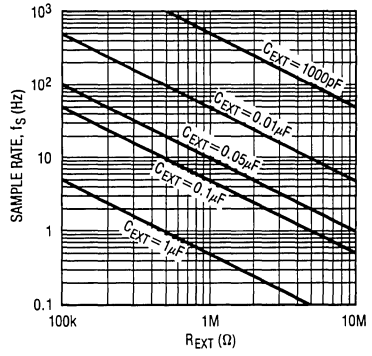
$I_{S(ON)}$ vs V^+



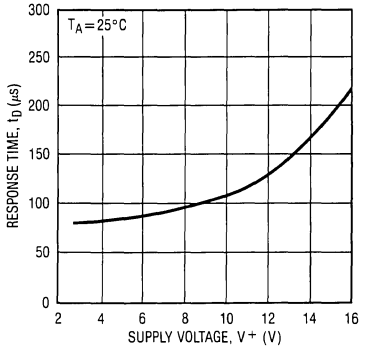
Normalized Sampling Frequency vs V^+, Temperature



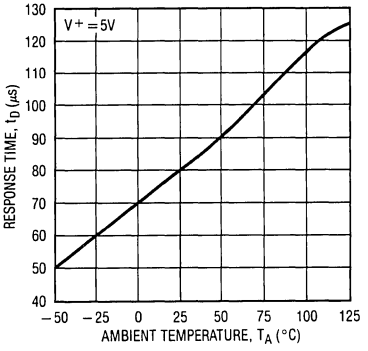
Sampling Rate vs R_{EXT}, C_{EXT}



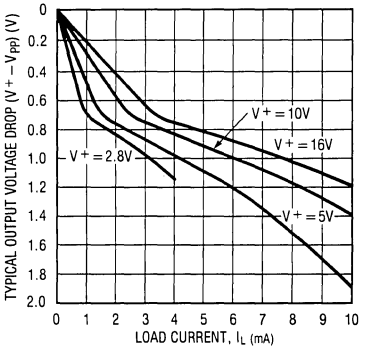
Response Time vs Supply Voltage



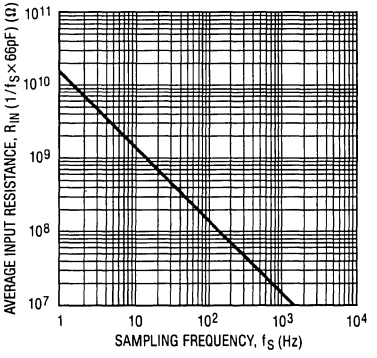
Response Time vs Temperature



V_{PP} Output Voltage vs Load Current



R_{IN} vs Sampling Frequency



APPLICATIONS INFORMATION

The LTC1041 uses sampled data techniques to achieve its unique characteristics. It consists of two comparators, each of which has two differential inputs (Figure 1). When the sum of the voltages on a comparator's inputs is positive, the output is high and when the sum is negative, the output is low. The inputs are interconnected such that the RS flip-flop is reset (ON/$\overline{OFF}$ = GND) when V_{IN} > (SET POINT + DELTA) and is set (ON/$\overline{OFF}$ = V^+) when V_{IN} < (SET POINT − DELTA). This makes a very precise hysteresis loop of 2 × DELTA centered around the SET POINT. See Figure 1(b).

For R_S < 10kΩ

The dual differential input structure is made with CMOS switches and a precision capacitor array. Input impedance characteristics of the LTC1041 can be determined from the equivalent circuit shown in Figure 2. The input capacitance will charge with a time constant of $R_S \times C_{IN}$. The ability to fully charge C_{IN} from the signal source during the controller's active time is critical in determining errors caused by the input charging current. For source resistances less than 10kΩ, C_{IN} fully charges and no error is caused by the charging current.

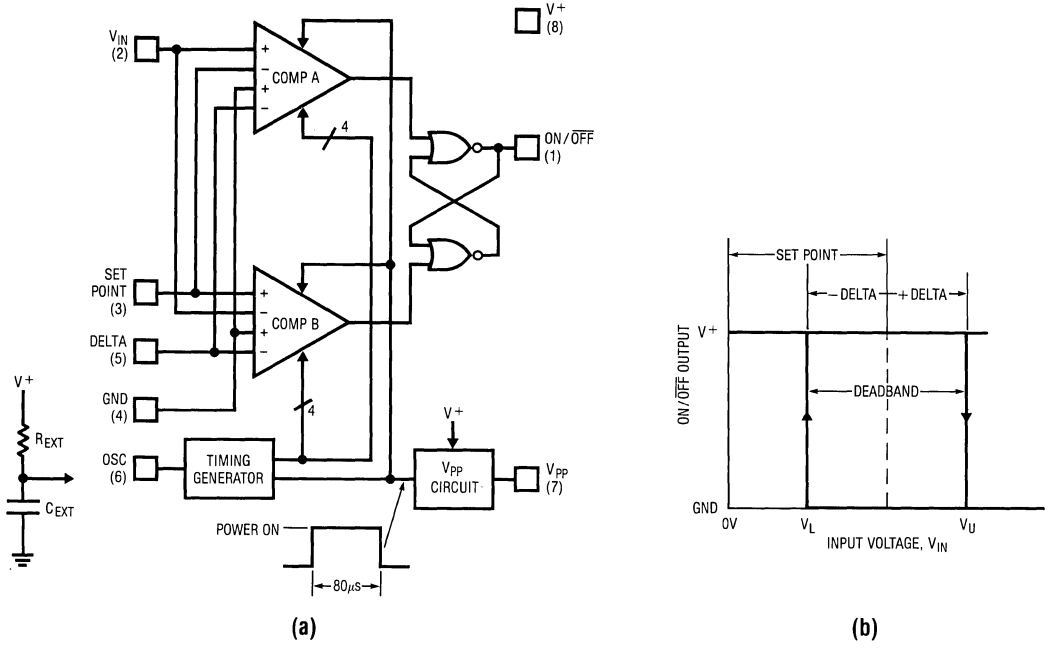


Figure 1. LTC1041 Block Diagram

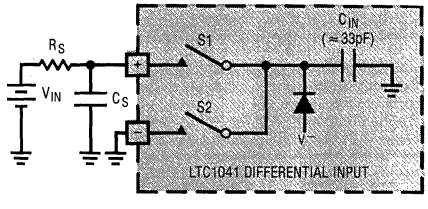


Figure 2. Equivalent Input Circuit

APPLICATIONS INFORMATION

For $R_S > 10k\Omega$

For source resistances greater than 10kΩ, C_{IN} cannot fully charge, causing voltage errors. To minimize these errors, an input bypass capacitor, C_S, should be used. Charge is shared between C_{IN} and C_S, causing a small voltage error. The magnitude of this error is $\Delta V = V_{IN} \times C_{IN} / (C_{IN} + C_S)$. This error can be made arbitrarily small by increasing C_S.

The averaging effect of the bypass capacitor, C_S, causes another error term. Each time the input switches cycle between the plus and minus inputs, C_{IN} is charged and discharged. The average input current due to this is $I_{AVG} = V_{IN} \times C_{IN} \times f_S$, where f_S is the sampling frequency. Because the input current is directly proportional to the differential input voltage, the LTC1041 can be said to have an average input resistance of $R_{IN} = V_{IN} / I_{AVG} = 1/(f_S \times C_{IN})$.

Since two comparator inputs are connected in parallel, R_{IN} is one half of this value (see typical curve of R_{IN} versus f_S). This finite input resistance causes an error due to the voltage divider between R_S and R_{IN}.

The input voltage error caused by both of these effects is $V_{ERROR} = V_{IN} [2C_{IN} / (2C_{IN} + C_S) + R_S / (R_S + R_{IN})]$.

Example: assume $f_S = 10Hz$, $R_S = 1M$, $C_S = 1\mu F$, $V_{IN} = 1V$, $V_{ERROR} = 1V(66\mu V + 660\mu V) = 726\mu V$. Notice that most of the error is caused by R_{IN}. If the sampling frequency is reduced to 1Hz, the voltage error from the input impedance effects is reduced to 136μV.

Input Voltage Range

The input switches of the LTC1041 are capable of switching either to the V^+ supply or ground. Consequently, the input voltage range includes both supply rails. This is a further benefit of the sampling input structure.

Error Specifications

The only measurable errors on the LTC1041 are the deviations from "ideal" of the upper and lower switching levels [Figure 1(b)]. From a control standpoint, the error in the SET POINT and deadband is critical. These errors may be defined in terms of V_U and V_L.

$$\text{SET POINT error} \equiv \left(\frac{V_U + V_L}{2}\right) - \text{SET POINT}$$

$$\text{deadband error} \equiv (V_U - V_L) - 2 \times \text{DELTA}$$

The specified error limits (see electrical characteristics) include error due to offset, power supply variation, gain, time and temperature.

Pulsed Power (V_{PP}) Output

It is often desirable to use the LTC1041 with resistive networks such as bridges and voltage dividers. The power consumed by these resistive networks can far exceed that of the LTC1041 itself.

At low sample rates the LTC1041 spends most of its time off. A switched power output, V_{PP}, is provided to drive the input network, reducing its average power as well. V_{PP} is switched to V^+ during the controller's active time ($\approx 80\mu s$) and to a high impedance (open circuit) when internal power is switched off.

Figure 3 shows the V_{PP} output circuit. The V_{PP} output voltage is not precisely controlled when driving a load (see typical curve of V_{PP} output voltage versus load current). In spite of this, high precision can be achieved in two ways: (1) driving ratiometric networks and (2) driving fast settling references.

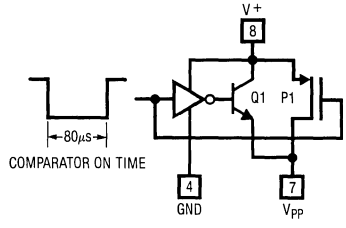


Figure 3. V_{PP} Output Switch

APPLICATIONS INFORMATION

In ratiometric networks (Figure 4) all the inputs are proportional to V_{PP}. Consequently, the absolute value of V_{PP} does not affect accuracy.

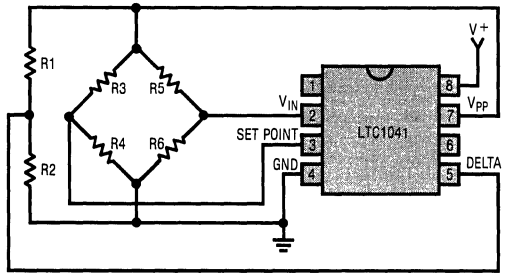


Figure 4. Ratiometric Network Driven by V_{PP}

If the best possible performance is needed, the inputs to the LTC1041 must completely settle within 4μs of the start of the comparison cycle (V_{PP} high impedance to V^+ transition). Also, it is critical that the input voltages do not change during the 80μs active time. When driving resistive input networks with V_{PP}, capacitive loading should be minimized to meet the 4μs settling time requirement. Further, care should be exercised in layout when driving networks with source impedances, as seen by the LTC1041, of greater than 10kΩ (see For $R_S > 10k\Omega$).

In applications where an absolute reference is required, the V_{PP} output can be used to drive a fast settling reference. The LTC1009 2.5V reference settles in ≈2μs and is ideal for this application (Figure 5). The current through R1 must be large enough to supply the LT1009 minimum bias current (≈ 1mA) and the load current, I_L.

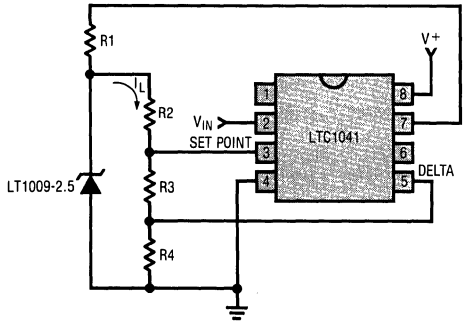


Figure 5. Driving Reference with V_{PP} Output

Internal Oscillator

An internal oscillator allows the LTC1041 to strobe itself. The frequency of the oscillation, and hence the sampling rate, is set with an external RC network (see typical curve, OSC frequency versus R_{EXT}, C_{EXT}). R_{EXT} and C_{EXT} are connected as shown in Figure 1. To assure oscillation, R_{EXT} must be between 100kΩ and 10MΩ. There is no limit to the size of C_{EXT}.

At low sampling rates, R_{EXT} is very important in determining the power consumption. R_{EXT} consumes power continuously. The average voltage at the OSC pin is approximately $V^+/2$, giving a power dissipation of $P_{REXT} = (V^+/2)^2/R_{EXT}$.

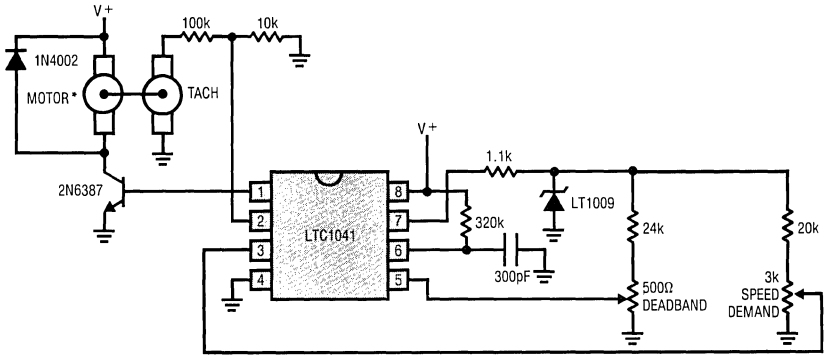
Example: assume $R_{EXT} = 1M\Omega$, $V^+ = 5V$, $P_{REXT} = (2.5)^2/10^6 = 6.25\mu W$. This is approximately four times the power consumed by the LTC1041 at $V^+ = 5V$ and $f_S = 1$ sample/second. Where power is a premium, R_{EXT} should be made as large as possible. Note that the power dissipated by R_{EXT} is *not* a function of f_S or C_{EXT}.

If high sampling rates are needed and power consumption is of secondary importance, a convenient way to get the maximum possible sampling rate is to make $R_{EXT} = 100k\Omega$ and $C_{EXT} = 0$. The sampling rate, set by the controller's active time, will nominally be ≈ 10kHz.

To synchronize the sampling of the LTC1041 to an external frequency source, the OSC pin can be driven by a CMOS gate. A CMOS gate is necessary because the input trip points of the oscillator are close to the supply rails and TTL does not have enough output swing. Externally driven, there will be a delay from the rising edge of the OSC input and the start of the sampling cycle of approximately 5μs.

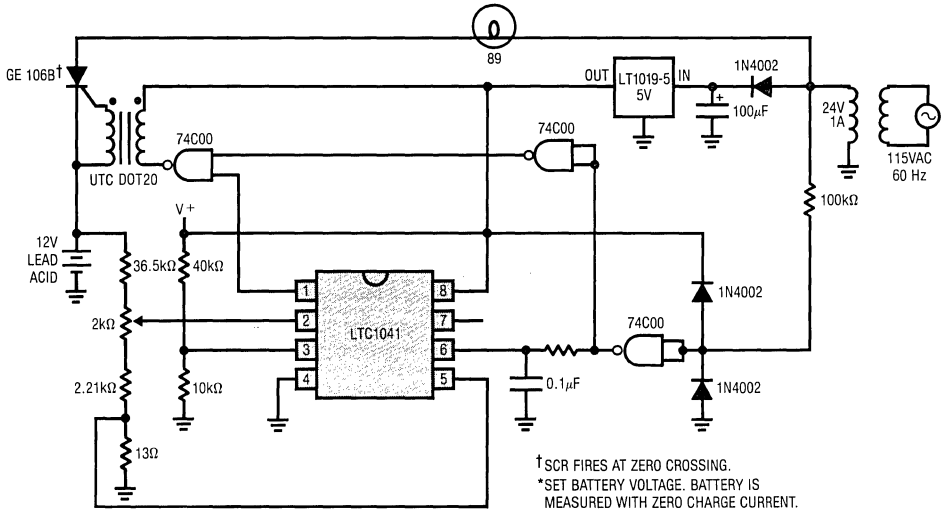
TYPICAL APPLICATIONS

Motor Speed Controller



*CANNON CKT26-T5-3SAE

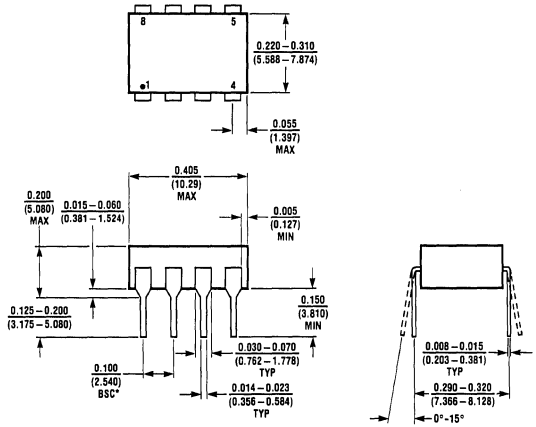
Battery Charger



†SCR FIRES AT ZERO CROSSING.
*SET BATTERY VOLTAGE. BATTERY IS MEASURED WITH ZERO CHARGE CURRENT.

PACKAGE DESCRIPTION Dimensions in inches (millimeters) unless otherwise noted.

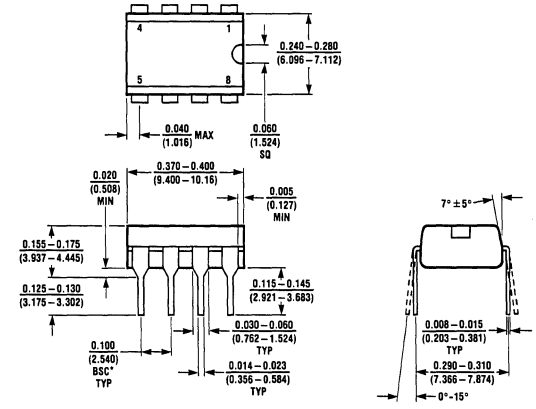
J8 Package
8 Lead Hermetic DIP



*LEADS WITHIN 0.007 OF TRUE POSITION (TP) AT GAUGE PLANE

T_{jmax}	Θ_{jA}
150°C	100°C/W

N8 Package
8 Lead Plastic



*LEADS WITHIN 0.007 OF TRUE POSITION (TP) AT GAUGE PLANE

T_{jmax}	Θ_{jA}
110°C	150°C/W

Voltage Comparator

FEATURES

- *Guaranteed* Max Input Offset Voltage 1.0mV
- *Guaranteed* Max Input Offset Current 5nA
- *Guaranteed* Max Response Time 250nS
- *Guaranteed* Min. Voltage Gain 200,000
- ±30V Differential Input Voltage
- Drives 50mA Loads At Up To 50V.
- ½ The Power Dissipation For LT111A/LT311A

APPLICATIONS

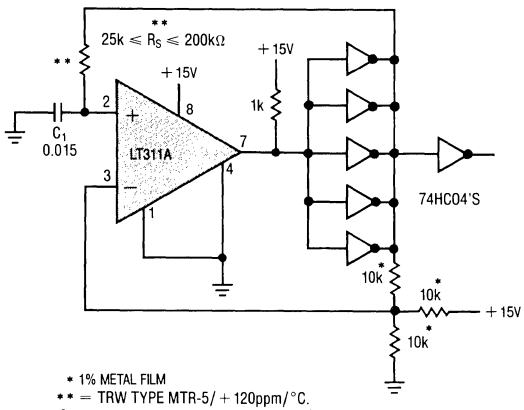
- General Purpose Comparator
- Zero Crossing Detector
- Voltage To Frequency Converter

DESCRIPTION

The LT111A is an improved version of the LM111 general purpose comparator. These new devices offer maximum input offset voltage of 1.0mV and input offset current of 5.0nA with a maximum response time of 250ns. The LT111A operate from a single 5V supply to ±15V supplies and can drive up to 50mA loads referred to ground or either supply. A separate output ground pin allows output signals to be isolated from analog ground.

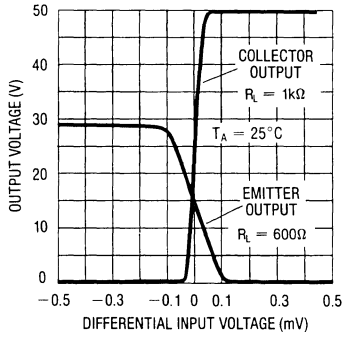
The versatility of the LT111A is enhanced by an input stage design which allows differential input signals of up to ±30V. Offset balancing, strobe capability and the ability to "OR" the output is also included. These features plus Linear Technology Corporation's advanced processing and reliability enhancements make the LT111A an ideal choice for most comparator applications. For higher performance requirements, see the LT1011.

Low Drift R/C Oscillator



* 1% METAL FILM
** = TRW TYPE MTR-5/ + 120ppm/°C.
C_1 = .015 = POLYSTYRENE − 120ppm/°C ± 30ppm WESCO TYPE 32-P
NOTE: COMPARATOR CONTRIBUTES ≤ 10ppm/°C DRIFT FOR FREQUENCIES BELOW 10kHz.

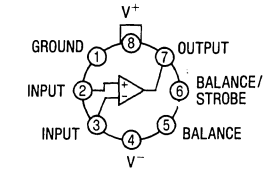
Transfer Function



ABSOLUTE MAXIMUM RATINGS

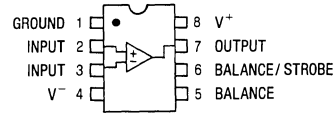
Supply Voltage
(pin 8 to pin 4) 36V
Output to Negative Supply
(pin 7 to pin 4)
LT111A/LM111 ..... 50V
LT311A/LM311 ..... 40V
Ground to Negative Supply
(pin 1 to pin 4) 30V
Differential Input Voltage ..... ±30V
Voltage at Strobe Pin (pin 6 to pin 8) 5V
Input Voltage (Note 1) ..... ±15V
Output Short Circuit Duration ..... 10 sec.
Operating Temperature Range (Note 2)
LT111A/LM111 ..... −55°C to 125°C
LT311A/LM311 ..... 0°C to 70°C
Storage Temperature Range ..... −65°C to 150°C
Lead Temperature (Soldering, 10 sec.) ..... 300°C

PACKAGE/ORDER INFORMATION



H PACKAGE
TO-5 METAL CAN

ORDER PART NUMBER
LT111AH
LM111H
LT311AH
LM311H



NOTE: PIN 4 CONNECTED TO CASE.
J8 PACKAGE 8 PIN CERDIP
N8 PACKAGE 8 PIN PLASTIC

LT111AJ8
LM111J8
LT311AJ8
LM311J8
LT311AN8
LM311N8

ELECTRICAL CHARACTERISTICS $V_S = \pm 15V$, $T_A = 25°C$ unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		LT 111A MIN	LT 111A TYP	LT 111A MAX	LM111 MIN	LM111 TYP	LM111 MAX	UNITS
V_{OS}	Input Offset Voltage	$R_S \leq 50k$ (Note 3, 4)	 ●		0.5	1.0 2.0		0.7	3.0 4.0	mV
I_{OS}	Input Offset Current	 (Note 3,4)	 ●		2.0	5.0 10.0		4.0	10.0 20.0	nA
I_B	Input Bias Current	 Note 3	 ●		60	100 150		60	100 150	nA
A_{VOL}	Large Signal Voltage Gain	Note 7		200	500		40	200		V/mV
	Response Time	Note 5			200	250		200		nS
	Saturation Voltage	$V_{IN} \leq -5mV$, $I_{OUT} = 50mA$ $V+ \geq 4.5V$, $V- = 0$ $V_{IN} \leq -6mV$, $I_{SINK} \leq 8mA$	 ●		0.75 0.23	1.5 0.4		0.75 0.23	1.5 0.4	V V
	Strobe ON Current	Note 6			3.0	4.0		3.0		mA
	Output Leakage Current	$V_{IN} \geq 5mV$, $V_{OUT} = 35V$ $I_{STROBE} = 3mA$	 ●		0.2 0.1	10.0 0.5		0.2 0.1	10.0 0.5	nA μA
	Input Voltage Range	$V+ = 15V$, $V- = 15V$ Pin 7 Pull up may go to 5V	●	−14.5	{13.8 −14.7}	13.0	−14.5	{13.8 −14.7}	13.0	V
	Positive Supply Current				3.0	4.0		5.1	6.0	mA
	Negative Supply Current				1.5	2.5		4.1	5.0	mA

Shading of a specification highlights those items which offer key improvements in parametric performance or guaranteed test limits provided for the first time.

ELECTRICAL CHARACTERISTICS $V_S = \pm 15V$, $T_A = 25°C$ unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		LT311A MIN	LT311A TYP	LT311A MAX	LM311 MIN	LM311 TYP	LM311 MAX	UNITS
V_{OS}	Input Offset Voltage	$R_S \leq 50k$			0.5	1.0		2.0	7.5	mV
		(Note 3, 4)	●			2.0			10	
I_{OS}	Input Offset Current				2.0	10		6.0	50	nA
		(Note 3, 4)	●			20			70	
I_B	Input Bias Current				60	100		100	250	nA
		Note 3	●			150			300	
A_{VOL}	Large Signal Voltage Gain			200	500		40	200		V/mV
	Response Time	Note 5			200	250		200		nS
	Saturation Voltage	$V_{IN} \leq -10mV$, $I_{OUT} = 50mA$			0.75	1.5		0.75	1.5	V
		$V+ \geq 4.5V$, $V- = 0$								
		$V_{IN} \leq -10mV$, $I_{SINK} \leq 8mA$	●		0.23	0.4		0.23	0.4	V
	Strobe ON Current	Note 6			3.0	4.0		3.0		mA
	Output Leakage Current	$V_{IN} \geq 10mV$, $V_{OUT} = 35V$			0.2	50		0.2	50	nA
		$I_{STROBE} = 3mA$	●		0.1	0.5				μA
	Input Voltage Range		●	−14.5	{13.8 / −14.7}	13.0	−14.5	{13.8 / −14.7}	13.0	V
	Positive Supply Current				3.0	4.0		5.1	7.5	mA
	Negative Supply Current				1.5	2.5		4.1	5.0	mA

The ● denotes the specifications which apply over the full operating temperature range.

Note 1: Applicable for ± 15V supplies. The positive input voltage limit is 30V above the negative supply. The negative input voltage limit is the negative supply.

Note 2: T_j max. = 150°C for the LT111A and 95°C for the LT311A.

Note 3: Offset voltage, offset current and bias current specifications apply for any supply voltage from a single 5V up to ± 15V supplies.

Note 4: Offset voltages and offset currents shown are the maximum values required to drive the output within a volt of either supply with a 1mA load. These parameters define an error band and take into account the worst case effects of voltage gain and input impedance.

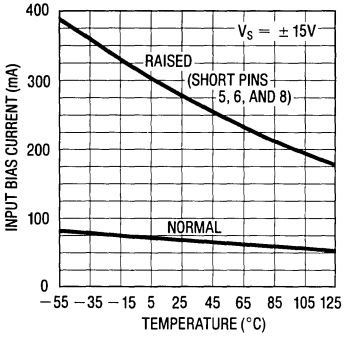
Note 5: Response time is specified for a 100mV input step with 5mV overdrive with the collector output terminated with a 500Ω pullup resistor tied to 5V.

Note 6: Do not short the strobe pin to ground. It should be current driven at 3 to 5mA for the shortest strobe time. Currents as low as 500μA will strobe the LT111A if speed is not important. External leakage on the strobe pin in excess of 0.2μA when the strobe is "off" can cause offset voltage shifts.

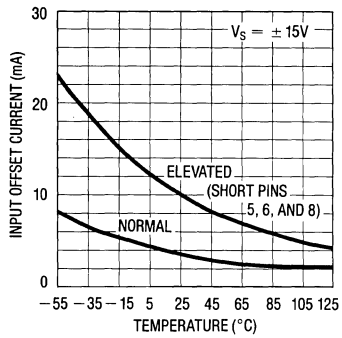
Note 7: $R_L = 1k\Omega$, $-10V \leq V_{OUT} \leq 14.5V$

TYPICAL PERFORMANCE CHARACTERISTICS

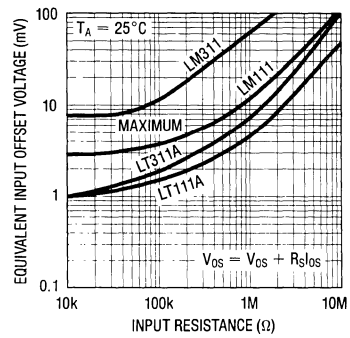
Input Bias Current



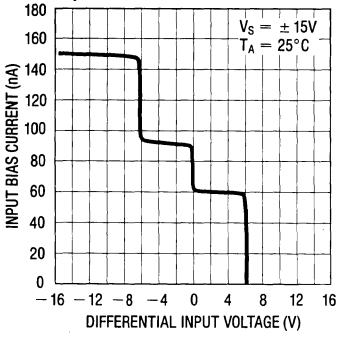
Input Offset Current



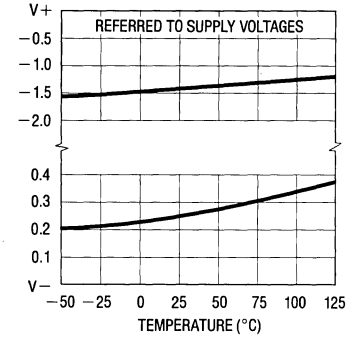
Offset Error



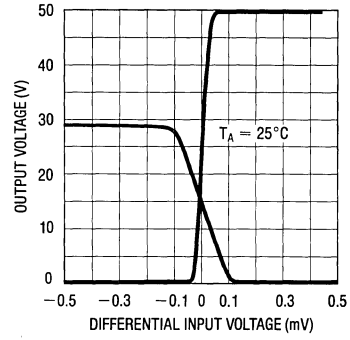
Input Characteristics



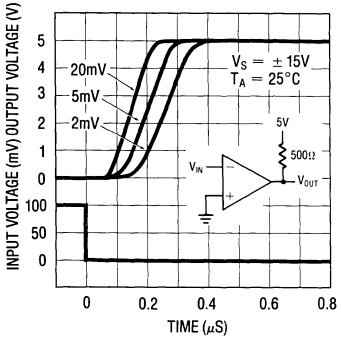
Common Mode Limits



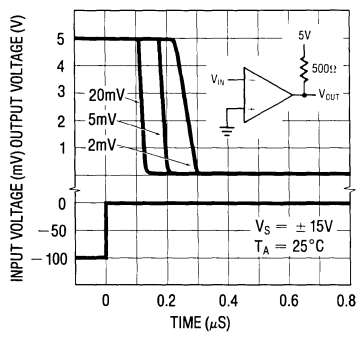
Transfer Function



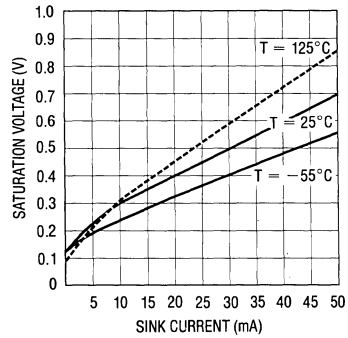
Response Time for Various Input Overdrives



Response Time for Various Input Overdrives

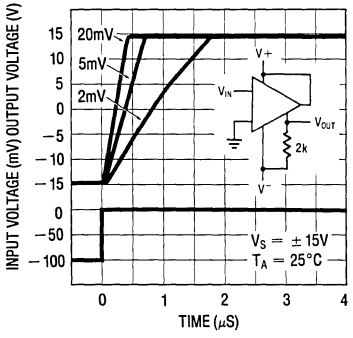


Collector Output Saturation Voltage

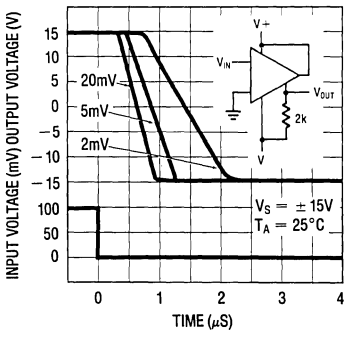


TYPICAL PERFORMANCE CHARACTERISTICS

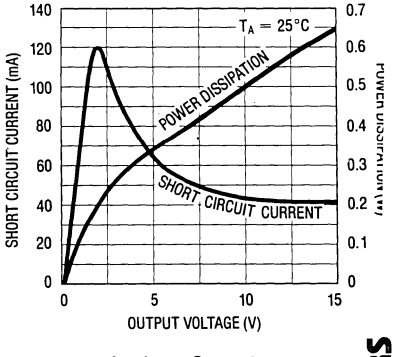
Response Time Using GND Pin as Output



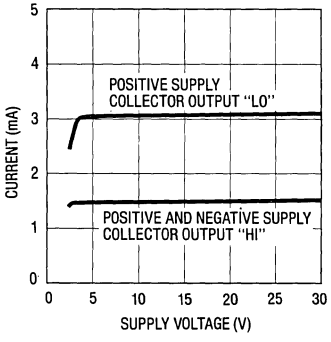
Response Time Using GND Pin as Output



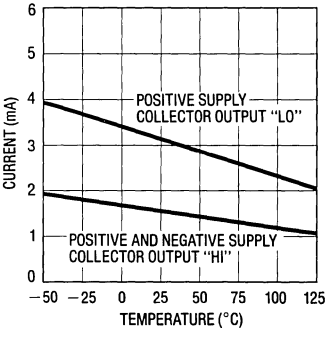
Output Limiting Characteristics



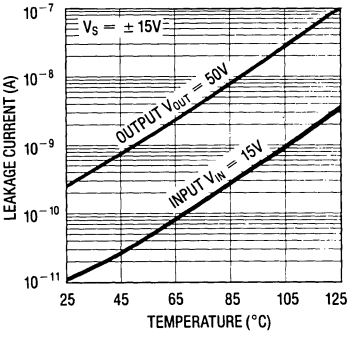
Supply Current vs Supply Voltage



Supply Current vs Temperature

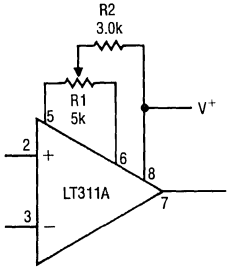


Leakage Current vs Temperature



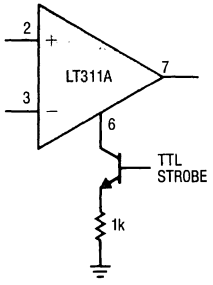
TYPICAL APPLICATIONS

Offset Balancing



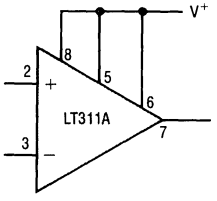
Note: Pin Connections Shown are for TO-5 package

Strobing



Note: Do Not Ground Strobe Pin.

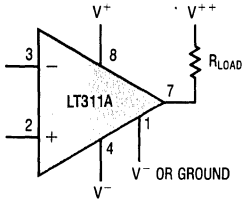
Increasing Input Stage Current



Increases typical common mode slew rate from 7.0 V/μS to 18V/μS.

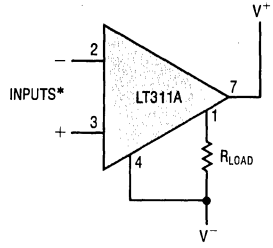
TYPICAL APPLICATIONS

Driving Load Referenced To Positive Supply



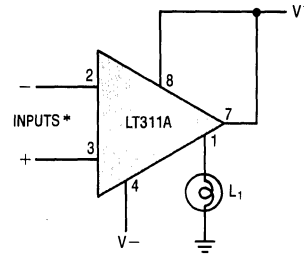
V^{++} CAN BE GREATER OR LESS THAN V^{+}

Driving Load Referenced To Negative Supply



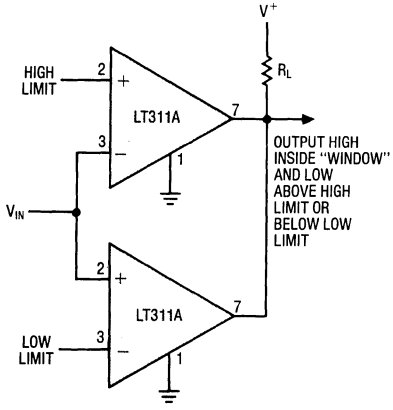
* NOTE THAT INPUT POLARITY IS REVERSED WHEN USING PIN 1 AS OUTPUT

Driving Ground Referred Load

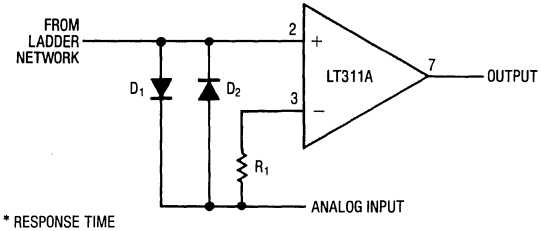


* NOTE THAT INPUT POLARITY IS REVERSED WHEN USING PIN 1 AS OUTPUT

Window Detector

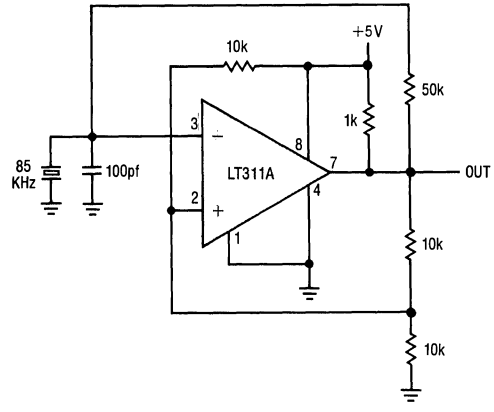


Using Clamp Diodes To Improve Frequency Response*

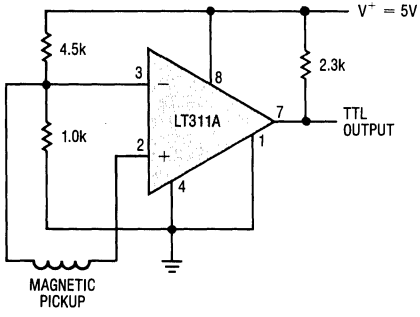


* RESPONSE TIME INCREASES TO ≈500nS IF INPUT MUST SLEW 5V TO REACH THRESHOLD.

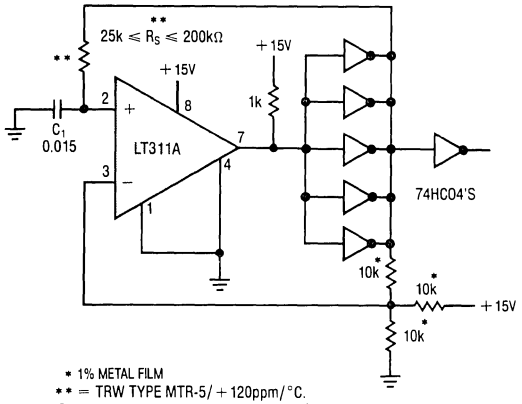
Crystal Oscillator



Detector For Magnetic Transducer

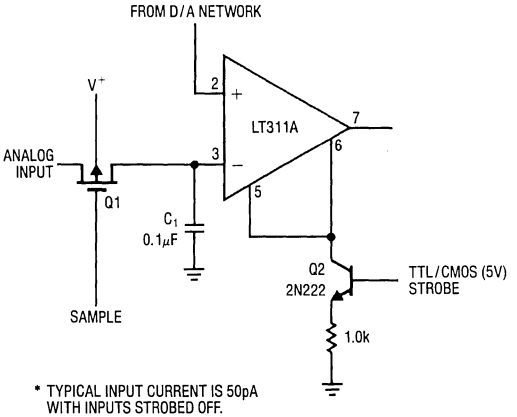


Low Drift R/C Oscillator



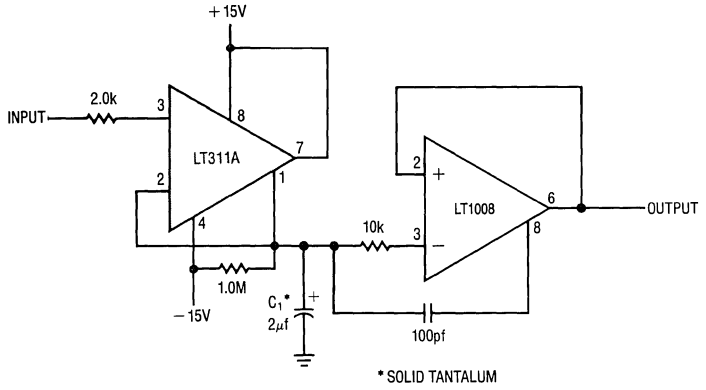
* 1% METAL FILM
** = TRW TYPE MTR-5/ + 120ppm/°C.
C_1 = .015 = POLYSTYRENE − 120ppm/°C ± 30ppm WESCO TYPE 32-P
NOTE: COMPARATOR CONTRIBUTES ≤ 10ppm/°C DRIFT FOR FREQUENCIES BELOW 10kHz.

Strobing Off Both Input* And Output Stages



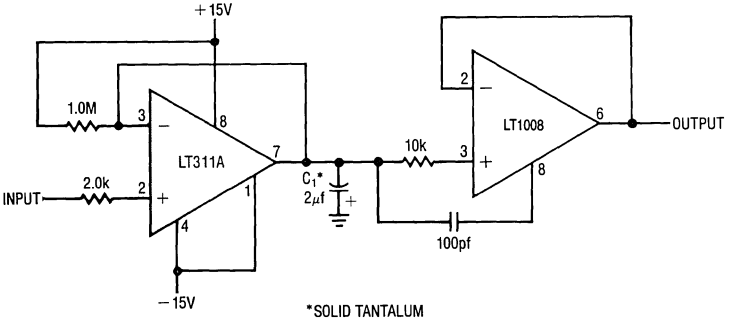
* TYPICAL INPUT CURRENT IS 50pA WITH INPUTS STROBED OFF. DO NOT GROUND STROBE PIN

Positive Peak Detector



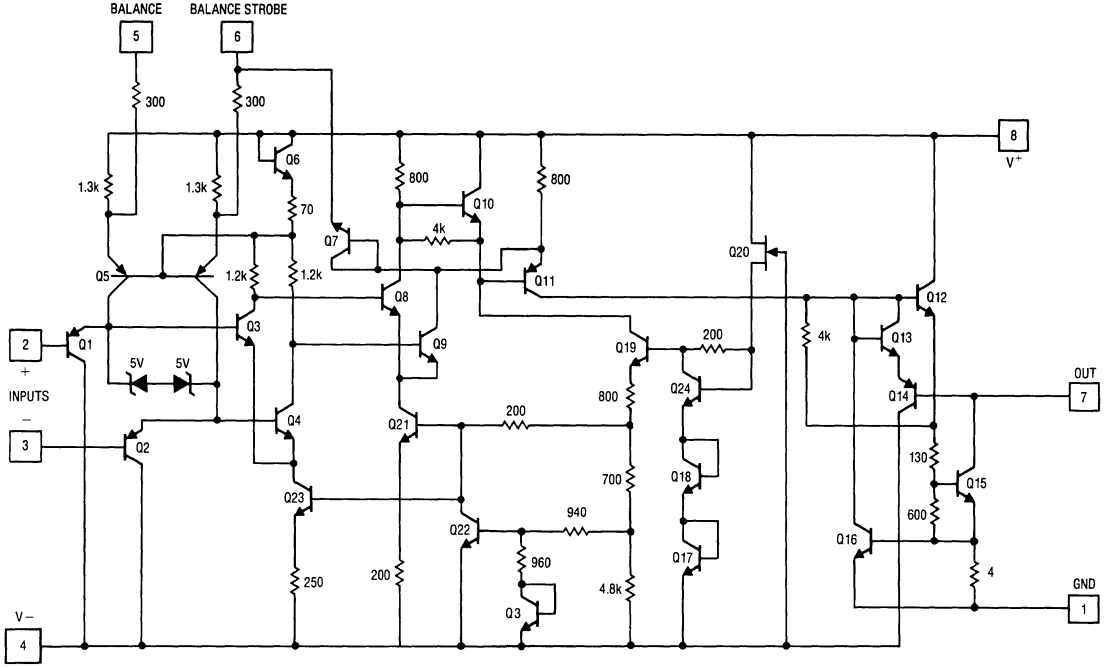
* SOLID TANTALUM

Negative Peak Detector



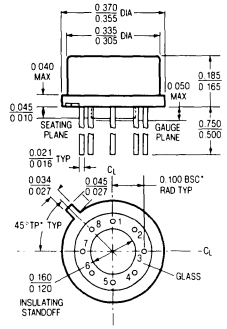
* SOLID TANTALUM

SCHEMATIC DIAGRAM



PACKAGE DESCRIPTION

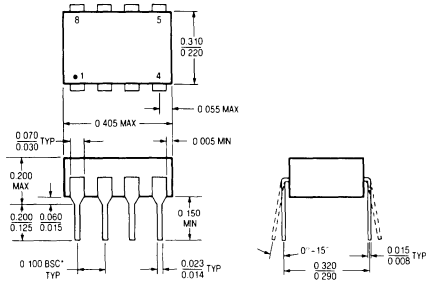
H Package
Metal Can



NOTE: DIMENSIONS IN INCHES

$T_j$max	Θ_{ja}	Θ_{jc}
150°C	150°C/W	45°C/W

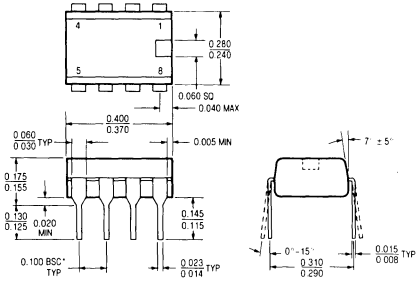
J8 Package
8 Lead Hermetic Dip



NOTE: DIMENSIONS IN INCHES UNLESS OTHERWISE NOTED.
*LEADS WITHIN 0.007 OF TRUE POSITION (TP) AT GAUGE PLANE

$T_j$max	Θ_{ja}
150°C	100°C/W

N8 Package
8 Lead Plastic



NOTE: DIMENSIONS IN INCHES UNLESS OTHERWISE NOTED.
*LEADS WITHIN 0.007 OF TRUE POSITION (TP) AT GAUGE PLANE

$T_j$max	Θ_{ja}
100°C	130°C/W

Dual Comparator

FEATURES

- *Guaranteed* max 0.5 mV input offset voltage
- Input Protection Diodes
- Operates from single 5V supply
- 25mA drive capability
- 80nS response time

APPLICATIONS

- Window detectors
- High speed one shot
- Relay/lamp drivers
- Voltage controlled oscillators

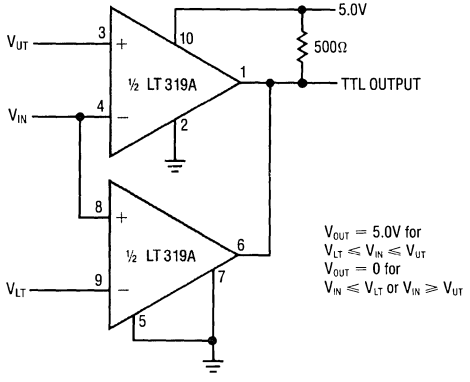
DESCRIPTION

The LT119A is an improved version of the LM119 dual comparator. It features lower input offset voltage and offset current, higher voltage gain, guaranteed common mode rejection, and input protection diodes.

The LT119A is capable of operation over a supply range from 5 Volts to ± 15 Volts and can drive 25mA loads from each open collector output. A separate ground pin allows the LT119A to isolate system grounds.

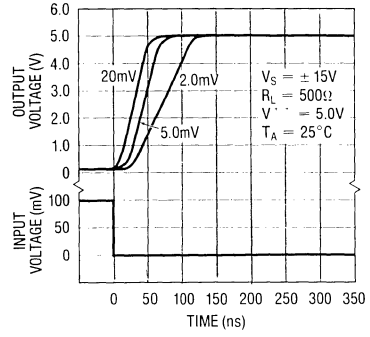
Linear Technology Corporation's advanced processing, design techniques and reliability make the LT119A/LT319A an ideal choice over previous devices in most comparator applications.

Window Detector*



*Allowed window for single +5V supply is 1.2V to 3.8V

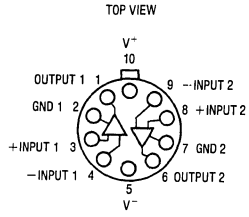
Response Time for Various Input Overdrives



ABSOLUTE MAXIMUM RATINGS

Supply Voltage 36V
Output to Negative Supply Voltage 36V
Ground to Negative Supply Voltage 25V
Ground to Positive Supply Voltage 18V
Differential Input Voltage ..... ±5V
Differential Input Current ..... ±5mA
Input Voltage (See Note 1)
Output Short Circuit Duration ..... 10 Sec
Operating Temperature Range
LT119A, LM119 ..... −55°C to 125°C
LT319A, LM319 ..... 0°C to 70°C
Storage Temperature Range ..... −65°C to 150°C
Lead Temperature
(Soldering, 10 sec) ..... 300°C

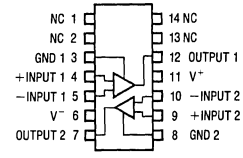
PACKAGE ORDER INFORMATION



H PACKAGE
METAL CAN

ORDER PART NUMBER

LT119AH
LM119H
LT319AH
LM319H



J PACKAGE
14-PIN HERMETIC

N PACKAGE
14 PIN PLASTIC

LT119AJ
LM119J
LT319AN
LM319N
LT319AJ
LM319J

ELECTRICAL CHARACTERISTICS (See Note 2)

SYMBOL	PARAMETER	CONDITIONS		LT119A MIN	LT119A TYP	LT119A MAX	LM119 MIN	LM119 TYP	LM119 MAX	UNITS
V_{OS}	Input Offset Voltage	$V_S = \pm 15V$ $V_{CM} = 0$			0.3	0.5			4.0	mV
V_{OS}	Input Offset Voltage	(See Note 3)			0.5	1.0		0.7	4.0	mV
			●		1.2	2.0			7.0	mV
CMRR	Common Mode Rejection Ratio				106					dB
I_{OS}	Input Offset Current	(See Note 3)		90	20	40		30	75	nA
			●			75			100	nA
I_B	Input Bias Current	(See Note 3)			150	500		150	500	nA
			●			1000			1000	nA
A_V	Voltage Gain			20	40		10	40		V/mV
	Response Time	(See Note 4)			80			80		nS
V_{SAT}	Saturation Voltage	$V_{IN} \leq -5mV$, $I_O = 25mA$ $V^+ \geq 4.5V$, $V^- = 0V$			0.75	1.5		0.75	1.5	V
		$V_{IN} \leq -6mV$, $I_{SINK} \leq 3.2mA$ $T_A \geq 0°C$			0.23	0.4		0.23	0.4	V
		$T_A \leq 0°C$				0.6			0.6	V
	Output Leakage Current	$V_{IN} \geq 5mV$, $V_{OUT} = 35V$			0.2	2		0.2	2	μA
			●		1	10		1	10	μA
	Input Voltage Range	$V_S = \pm 15V$	●	−12	±13	+12	−12	±13	+12	V
		$V^+ = 5V$, $V^- = 0$	●	1		3	1		3	V
	Differential Input Voltage		●			±5			±5	V
I_S	Supply Current	$V^+ = 5V$, $V^- = 0$			4.3			4.3		mA
I_S	Positive Supply Current	$V_S = \pm 15V$			8	11.5		8	11.5	mA
I_S	Negative Supply Current	$V_S = \pm 15V$			3	4.5		3	4.5	mA

LINEAR TECHNOLOGY

ELECTRICAL CHARACTERISTICS (See Note 2)

SYMBOL	PARAMETER	CONDITIONS		LT 319A MIN	LT 319A TYP	LT 319A MAX	LM319 MIN	LM319 TYP	LM319 MAX	UNITS
V_{OS}	Input Offset Voltage	$V_S = \pm 15V$ $V_{CM} = 0$			0.3	0.5			8.0	mV
V_{OS}	Input Offset Voltage	$R_S \leq 5k$ (See Note 3)	 ●		0.5	1		2.0	8.0 10	mV mV
CMRR	Common Mode Rejection Ratio			90	106					dB
I_{OS}	Input Offset Current	(See Note 3)	 ●		30	40		80	200 300	nA nA
I_B	Input Bias Current	(See Note 3)	 ●		150	500 1000		250	1000 1200	nA nA
A_V	Voltage Gain			20	40		8	40		V/mV
	Response Time	(See Note 4)			80			80		nS
V_{SAT}	Saturation Voltage	$V_{IN} \leq -10mV$, $I_{SINK} = 25mA$ $T_A = 25°C$ $V^+ \geq 4.5V$, $V^- = 0$ $V_{IN} \leq -10mV$, $I_{SINK} \leq 3.2mA$	 ●		0.75 0.3	1.5 0.4		0.75 0.3	1.5 0.4	V V
	Output Leakage Current	$V_{IN} \geq 10mV$, $V_{OUT} = 35V$			0.2	10		0.2	10	μA
	Input Voltage Range	$V_S = \pm 15V$ $V^+ = 5V$, $V^- = 0V$	● ●	 1	±13	 3	 1	±13	 3	V V
	Differential Input Voltage		●			±5			±5	V
I_S	Supply Current	$V^+ = 5V$, $V^- = 0V$			4.3			4.3		mA
I_S	Positive Supply Current	$V_S = \pm 15V$			8	12.5		8	12.5	mA
I_S	Negative Supply Current	$V_S = \pm 15V$			3	5		3	5	mA

The ● denotes the specifications which apply over the full operating temperature range.

The shaded electrical specifications indicate those parameters which have been improved or guaranteed test limits provided for the first time.

Note 1: For supply voltages less than ±15V, the maximum input voltage is equal to the supply voltage.

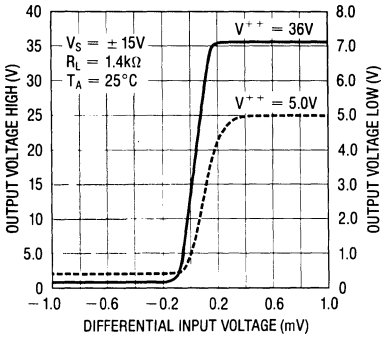
Note 2: Unless otherwise noted, supply voltage equals ±15V and $T_A = 25°C$. The ground pin is grounded. Note that the maximum voltage allowed between the ground pin and V^+ is 18V. Do not tie the ground pin to V^- when the power supply voltage exceeds ±9V. The offset voltage, offset current and bias current specifications apply for all supply voltages between ±15V and +5V unless otherwise specified.

Note 3: The offset voltages and currents given are the maximum values required to drive the output within 1 volt of either supply with a 1mA load — thus, these parameters define an error band and take into account the worst case effects of voltage gain and input impedance.

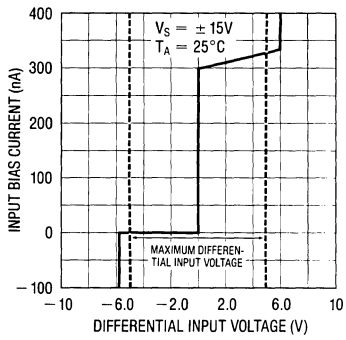
Note 4: Response time specified is for a 100mV input step with 5mV overdrive.

TYPICAL PERFORMANCE CHARACTERISTICS

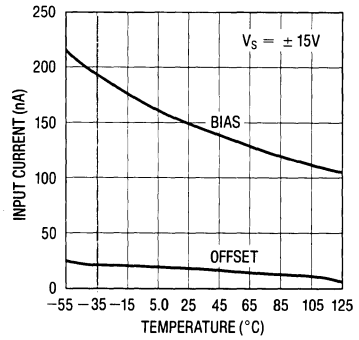
Transfer Function



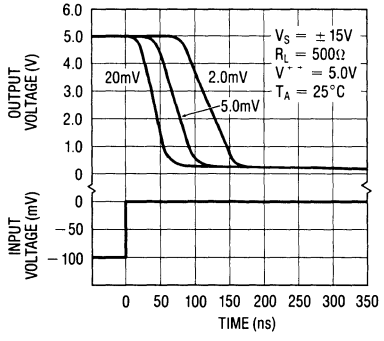
Input Characteristics



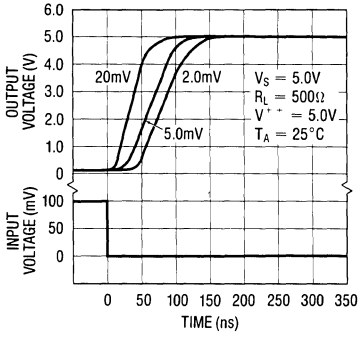
Input Currents



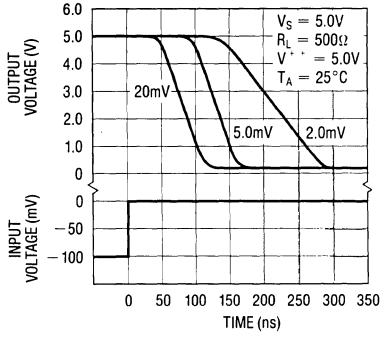
Response Time for Various Input Overdrives



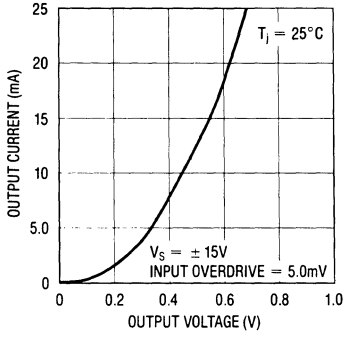
Response Time for Various Input Overdrives



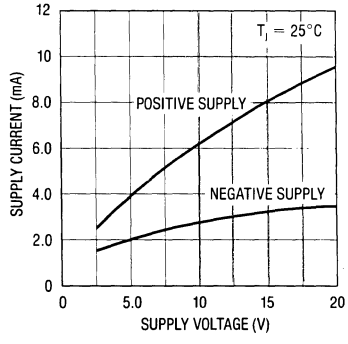
Response Time for Various Input Overdrives



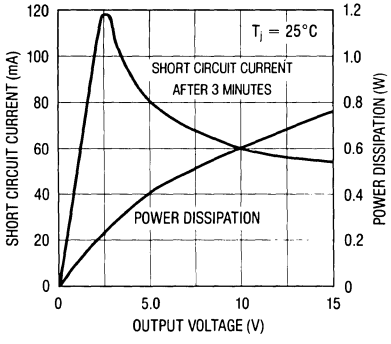
Output Saturation Voltage



Supply Current

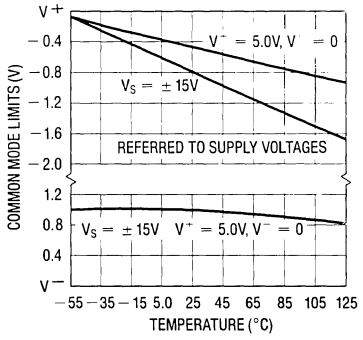


Output Limiting Characteristics

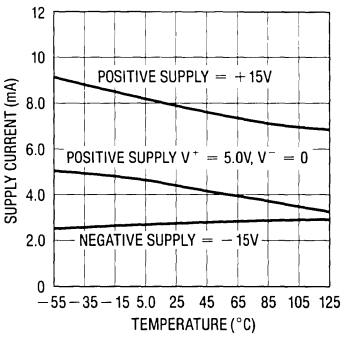


TYPICAL PERFORMANCE CHARACTERISTICS

Common Mode Limits

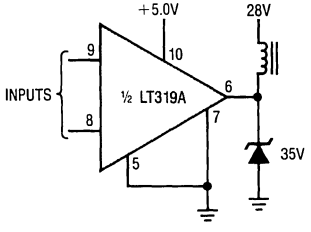


Supply Current

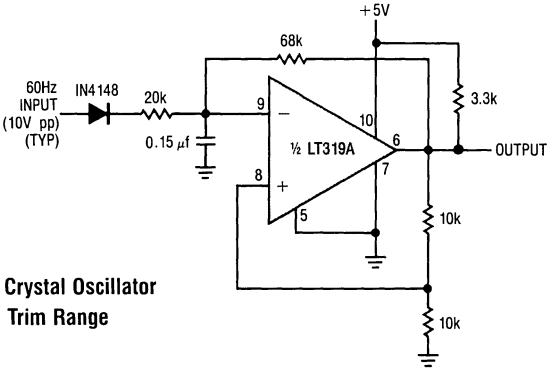


TYPICAL APPLICATIONS

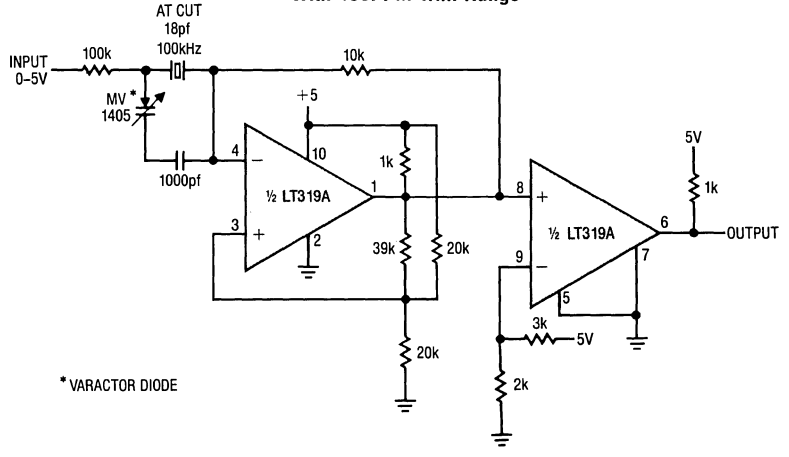
Relay Driver



High Noise Immunity 60Hz Sync Circuit

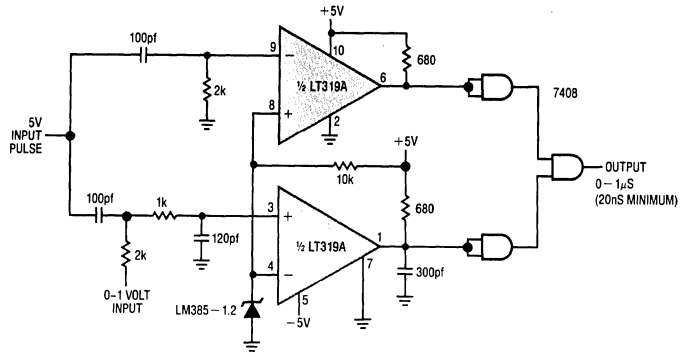


Voltage Controlled Crystal Oscillator With 100PPM Trim Range

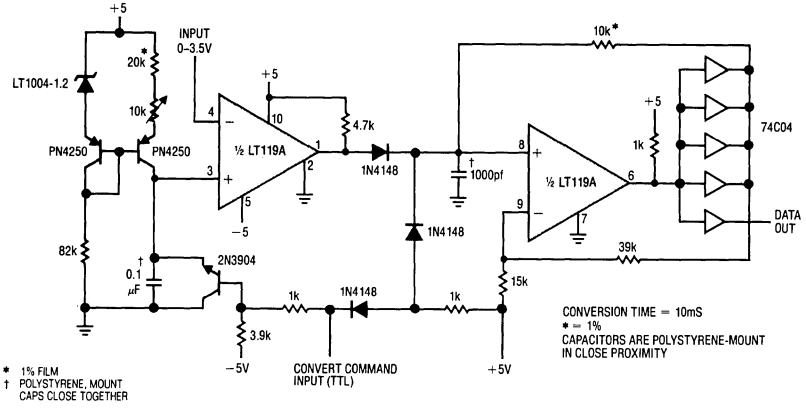


TYPICAL APPLICATIONS

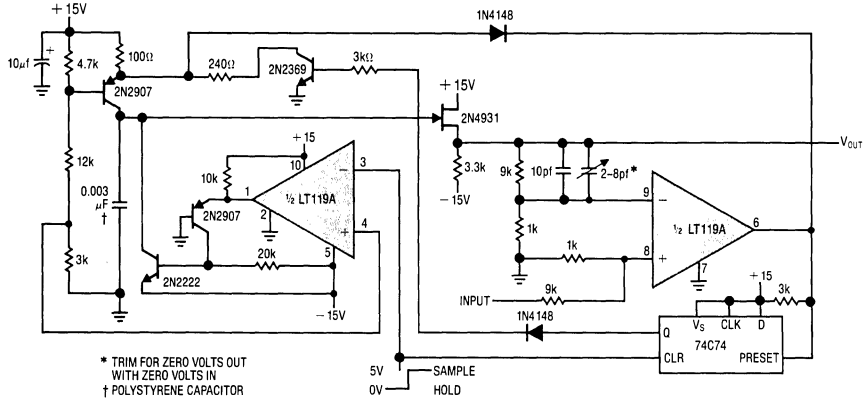
Voltage Controlled High Speed One Shot



10 Bit Serial Output A/D Converter

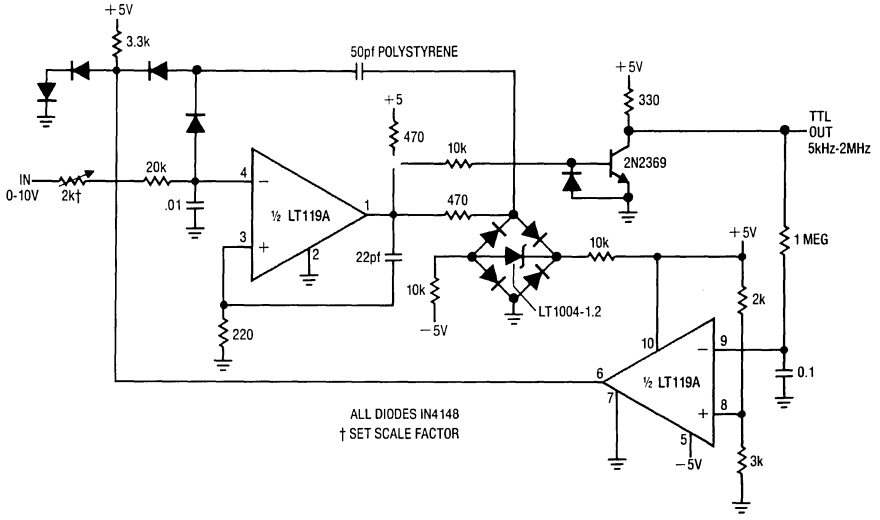


5 Microsecond Sample and Hold with Zero Hold Step

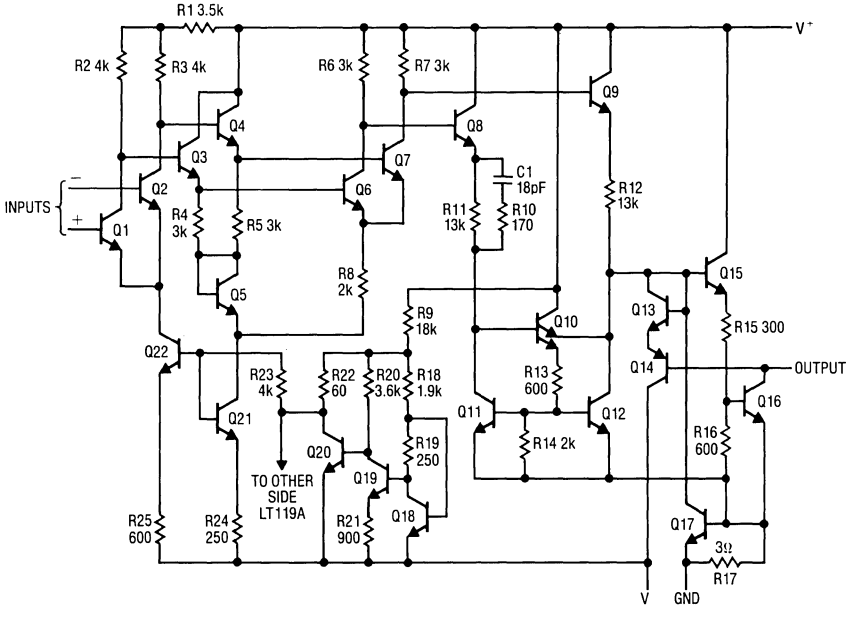


TYPICAL APPLICATIONS

5kHz to 2MHz V → F Converter

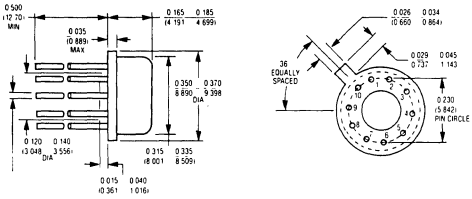


SCHEMATIC DIAGRAM



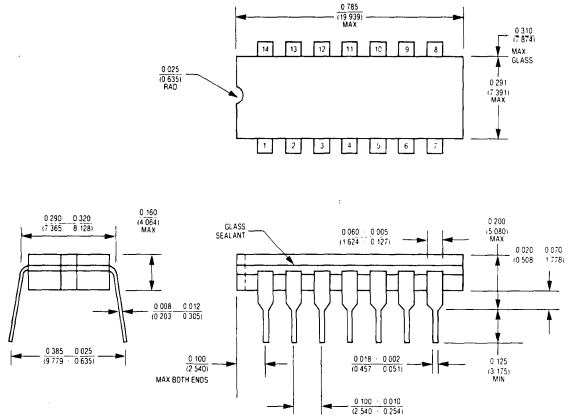
PACKAGE DESCRIPTION

10 Lead TO-5 Metal Can (H)



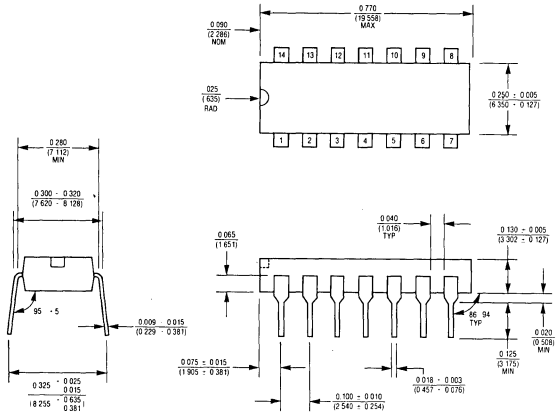
	T_j MAX	Θ_{JA}	Θ_{JC}
LT119AH LM119H	150°C	150°C/W	45°C/W
LT319AH LM319H	85°C	150°C/W	45°C/W

14-Lead Cavity DIP (J)



	T_j MAX	Θ_{JA}
LT119AJ	150°C	100°C/W
LM119J	150°C	100°C/W
LT319AJ	85°C	100°C/W
LM319J	85°C	100°C/W

14-Lead Molded DIP (N)



	T_j MAX	Θ_{JA}
LT319AN LM319N	85°C	100°C/W

SECTION 6—FILTERS

SECTION 6—FILTERS

High Performance Switched Capacitor Universal Filter

FEATURES

- All Filter Parameters *Guaranteed* over Temperature
- Wide Center Frequency Range (0.1Hz to 40kHz)
- Low Noise Wide Dynamic Range
- *Guaranteed* Operation for ±2.37V and ±5V Supply
- Low Power Consumption
- *Guaranteed* Clock to Center Frequency Accuracy of 0.3% (LTC1059A)
- *Guaranteed* Low Offset Voltages over Temperature
- Very Low Center Frequency and Q Tempco
- Clock Input T^2L or CMOS Compatible
- Separate Highpass (or Notch or Allpass), Bandpass, Lowpass Outputs

APPLICATIONS

- Sinewave Oscillators
- Sweepable Bandpass/Notch Filters
- Full Audio Frequency Filters
- Tracking Filters

DESCRIPTION

The LTC1059 consists of a general purpose, high performance, active filter building block and an uncommitted op amp. The filter building block together with an external clock and 2 to 5 resistors can produce various second order functions which are available at its three output pins. Two out of three always provide lowpass and bandpass functions while the third output pin can produce notch or highpass or allpass. The center frequency of these functions can be tuned from 0.1Hz to 40kHz and it is dependent on an external clock or an external clock and a resistor ratio. The filter can handle input frequencies up to 100kHz. The uncommitted op amp can be used to obtain additional allpass and notch functions, for gain adjustment or for cascading techniques.

Higher than second order filter functions can be obtained by cascading the LTC1059 with the LTC1060 dual universal filter or LTC1061 triple universal filter. Any classical filter realization (such as Butterworth, Cauer, Bessel and Chebyshev) can be formed.

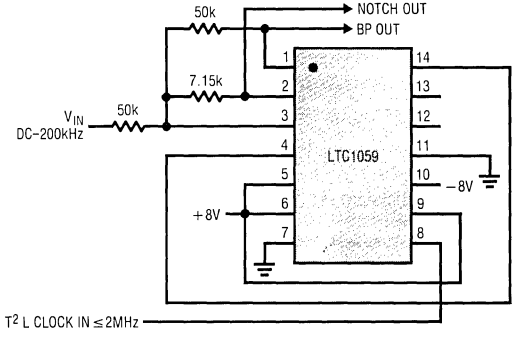
The LTC1059 can be operated with single or dual supplies ranging from ±2.37V to ±8V (or 4.74V to 16V single supply) and is pinout compatible with MF5.

The LTC1059 is manufactured by using Linear Technology's enhanced LTCMOS™ silicon gate process.

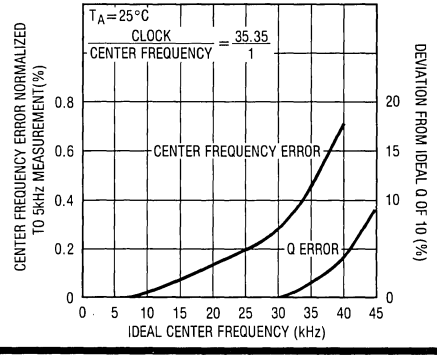
LTCMOS™ is a trademark of Linear Technology Corp.

TYPICAL APPLICATION

Wide Range 2nd Order Bandpass/Notch Filter with Q = 10



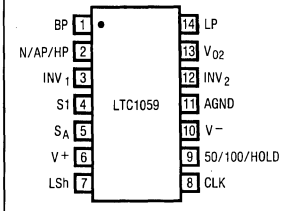
Center Frequency and Q Error



ABSOLUTE MAXIMUM RATINGS

Supply Voltage 18V
Power Dissipation 500mW
Operating Temperature Range
LTC1059AC, LTC1059C ..... $-40°C \le T_A \le 85°C$
LTC1059AM, LTC1059M ..... $-55°C \le T_A \le 125°C$
Storage Temperature Range ..... $-65°C$ to $150°C$
Lead Temperature (Soldering, 10sec) ..... 300°C

PACKAGE/ORDER INFORMATION



ORDER PART NUMBER
LTC1059ACN
LTC1059ACJ
LTC1059AMJ
LTC1059CN
LTC1059CJ
LTC1059MJ

ELECTRICAL CHARACTERISTICS

(Complete Filter) $V_S = \pm 5V$, $T_A = 25°C$, T^2L clock input level unless otherwise specified.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Center Frequency Range, f_o	$f_o \times Q \le 400kHz$, Mode 1			0.1-40k		Hz
	$f_o \times Q \le 1.6MHz$, Mode 1			0.1-18k		Hz
	$f_o \times Q \le 250kHz$, Mode 3, $V_S = \pm 7.5V$			0.1-20k		Hz
	$f_o \times Q \le 1MHz$, Mode 3, $V_S = \pm 7.5V$			0.1-16k		Hz
Input Frequency Range				0-200k		Hz
Clock to Center Frequency Ratio						
LTC1059A	Mode 1, 50:1, $f_{CLK} = 250kHz$, Q = 10	●			50 ± 0.3%	
LTC1059	Mode 1, 50:1, $f_{CLK} = 250kHz$, Q = 10	●			50 ± 0.8%	
LTC1059A	Mode 1, 100:1, $f_{CLK} = 500kHz$, Q = 10	●			100 ± 0.3%	
LTC1059	Mode 1, 100:1, $f_{CLK} = 500kHz$, Q = 10	●			100 ± 0.8%	
Q Accuracy						
LTC1059A	Mode 1, 50:1 or 100:1, $f_o = 5kHz$	●		±0.5	3	%
LTC1059	Q = 10	●		±0.5	5	%
f_o Temperature Coefficient	Mode 1, $f_{CLK} < 500kHz$			5		ppm/°C
Q Temperature Coefficient	Mode 1, $f_{CLK} < 500kHz$, Q = 10			15		ppm/°C
DC Offset V_{OS1}		●		2	15	mV
V_{OS2}	$f_{CLK} = 250kHz$, 50:1, $S_{A/B}$ High	●		3	30	mV
V_{OS2}	$f_{CLK} = 500kHz$, 100:1, $S_{A/B}$ High	●		6	60	mV
V_{OS2}	$f_{CLK} = 250kHz$, 50:1, $S_{A/B}$ Low	●		2	20	mV
V_{OS2}	$f_{CLK} = 500kHz$, 100:1, $S_{A/B}$ Low	●		4	40	mV
V_{OS3}	$f_{CLK} = 250kHz$, 50:1	●		2	20	mV
V_{OS3}	$f_{CLK} = 500kHz$, 100:1	●		4	40	mV
DC Low Pass Gain Accuracy	Mode 1, R1 = R2 = 50kΩ	●		±0.1	2	%
BP Gain Accuracy at f_o	Mode 1, Q = 10, $f_o = 5kHz$			±0.1		%
Clock Feedthrough	$f_{CLK} \le 1MHz$			10		mV
Max. Clock Frequency	Mode 1, Q < 5, $V_S \ge \pm 5V$			2		MHz
Power Supply Current				3.5	5.5	mA
		●			7	mA

ELECTRICAL CHARACTERISTICS (Complete Filter) $V_S = \pm 2.37V$, $T_A = 25°C$ unless otherwise specified

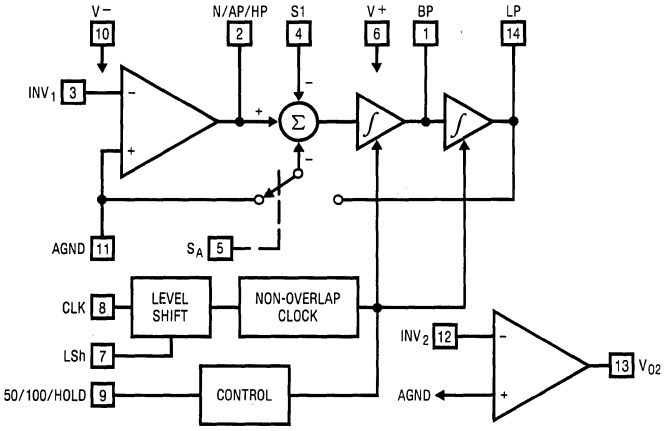
PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Center Frequency Range	$f_o \times Q \leq 120kHz$, Mode 1, 50:1 $f_o \times Q \leq 120kHz$, Mode 3, 50:1			0.1-12k 0.1-10k		Hz Hz
Input Frequency Range				60k		Hz
Clock to Center Frequency Ratio LTC1059A LTC1059 LTC1059A LTC1059	 Mode 1, 50:1, $f_{CLK} = 250kHz$, Q = 10 Mode 1, 50:1, $f_{CLK} = 250kHz$, Q = 10 Mode 1, 100:1, $f_{CLK} = 250kHz$, Q = 10 Mode 1, 100:1, $f_{CLK} = 250kHz$, Q = 10	 ● ● 		 50 ± 0.8% 100 ± 0.5% 100 ± 0.8%	 50 ± 0.5% 	
Q Accuracy LTC1059A LTC1059	 Mode 1, $f_{CLK} = 250kHz$, Q = 10 50:1 and 100:1			 ±1 ±2		 % %
Max. Clock Frequency Power Supply Current				700k 1.5	 2.5	Hz mA

ELECTRICAL CHARACTERISTICS (Internal Op Amps) $T_A = 25°C$ unless otherwise specified

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Voltage Range			±2.375		±8	V
Voltage Swings LTC1059A LTC1059 LTC1059, LTC1059A	 $V_S = \pm 5V$, $R_L = 5k$ (Pins 1, 14) $R_L = 3.5k$ (Pins 2, 13)	 ●	 ±4 ±3.8 ±3.6	 ±4.2 ±4.2		 V V V
Input Offset Voltage Input Bias Current Output Short Circuit Current Source/Sink DC Open Loop Gain	 $V_S = \pm 5V$ $V_S = \pm 5V$	●		1 3 40/3 80	15	mV pA mA dB
GBW Slew Rate	$V_S = \pm 5V$ $V_S = \pm 5V$			2 7		MHz V/μs

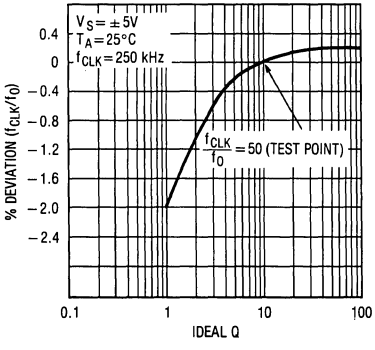
The ● denotes the specifications which apply over the full operating temperature range.

BLOCK DIAGRAM

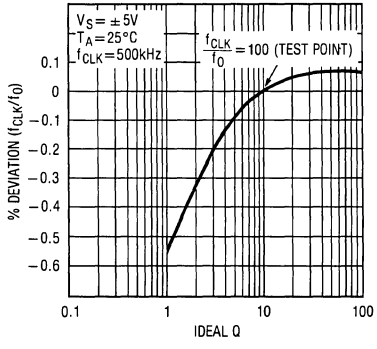


TYPICAL PERFORMANCE CHARACTERISTICS

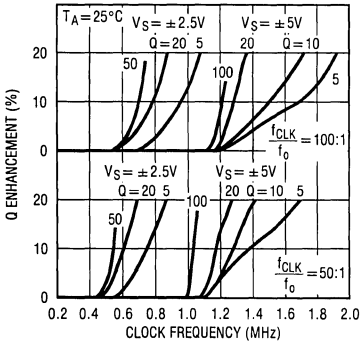
Graph 1. Mode 1: (f_{CLK}/f_o) Deviation vs Q



Graph 2. Mode 1: (f_{CLK}/f_o) Deviation vs Q

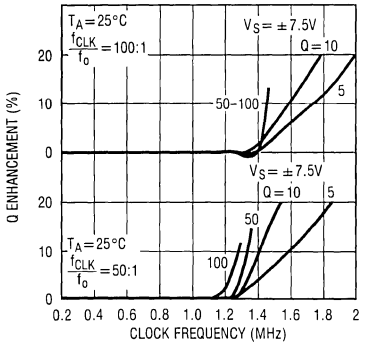


Graph 3. Mode 1: Q Error vs Clock Frequency

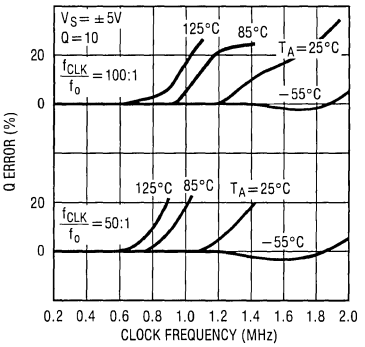


TYPICAL PERFORMANCE CHARACTERISTICS

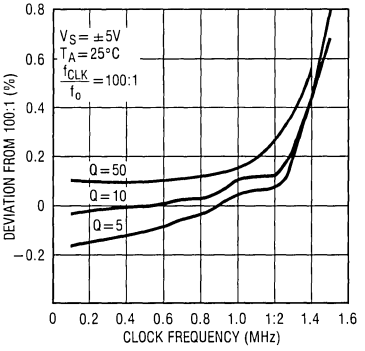
Graph 4. Mode 1: Q Error vs Clock Frequency



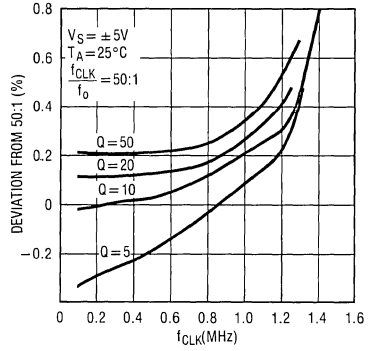
Graph 5. Mode 1: Measured Q vs f_{CLK} and Temperature



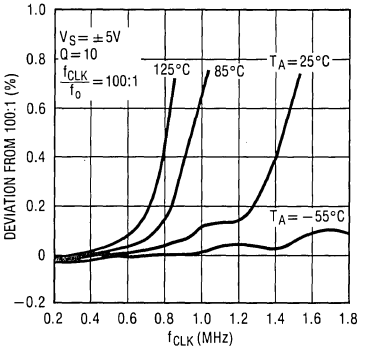
Graph 6. Mode 1: (f_{CLK}/f_o) vs f_{CLK} and Q



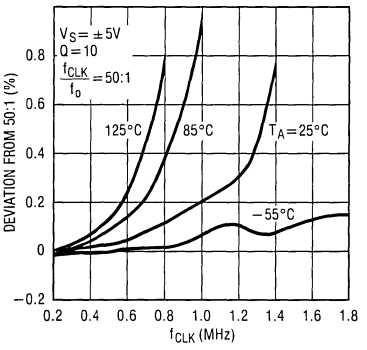
Graph 7. Mode 1: (f_{CLK}/f_o) vs f_{CLK} and Q



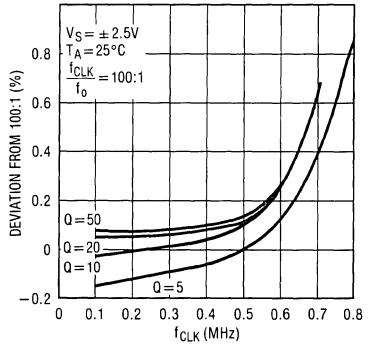
Graph 8. Mode 1: (f_{CLK}/f_o) vs f_{CLK} and Temperature



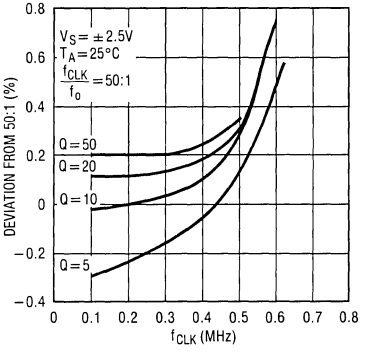
Graph 9. Mode 1: (f_{CLK}/f_o) vs f_{CLK} and Temperature



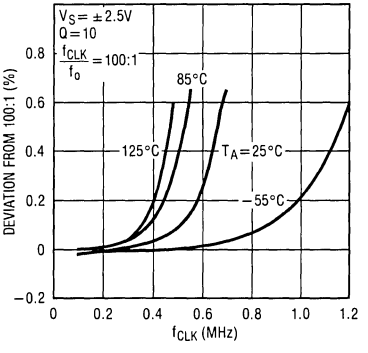
Graph 10. Mode 1: (f_{CLK}/f_o) vs f_{CLK} and Q



Graph 11. Mode 1: (f_{CLK}/f_o) vs f_{CLK} and Q

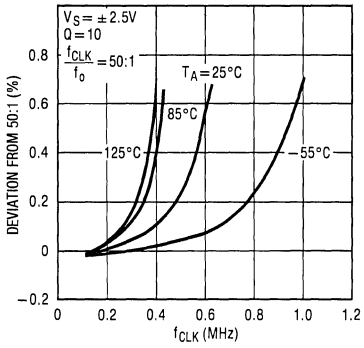


Graph 12. Mode 1: (f_{CLK}/f_o) vs f_{CLK} and Temperature

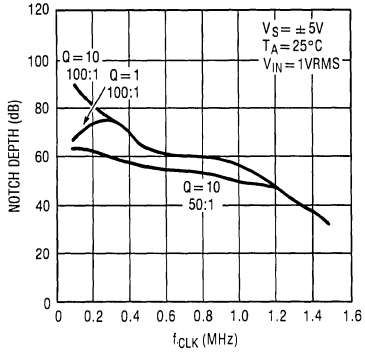


TYPICAL PERFORMANCE CHARACTERISTICS

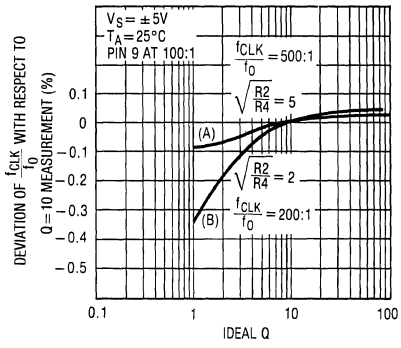
Graph 13. Mode 1: (f_{CLK}/f_o) vs f_{CLK} and Temperature



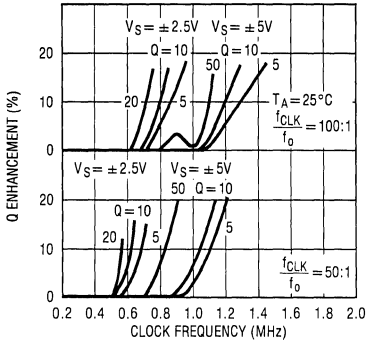
Graph 14. Mode 1: Notch Depth vs Clock Frequency



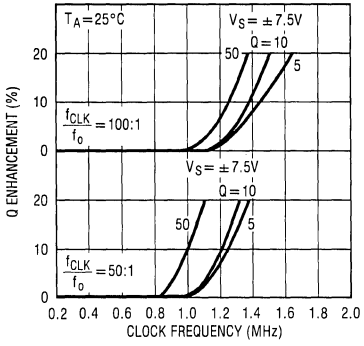
Graph 15. Mode 3: Deviation of (f_{CLK}/f_o) with Respect to Q = 10 Measurement



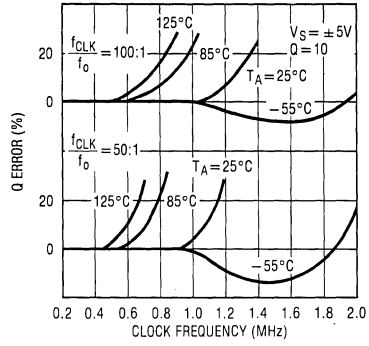
Graph 16. Mode 3: Q Error vs Clock Frequency



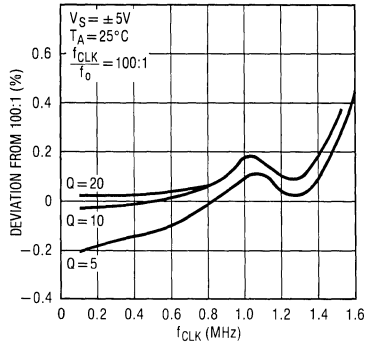
Graph 17. Mode 3 (R2 = R4): Q Error vs Clock Frequency



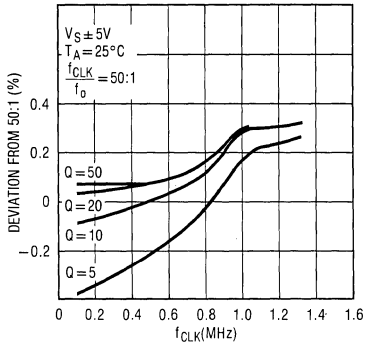
Graph 18. Mode 3 (R2 = R4): Measured Q vs f_{CLK} and Temperature



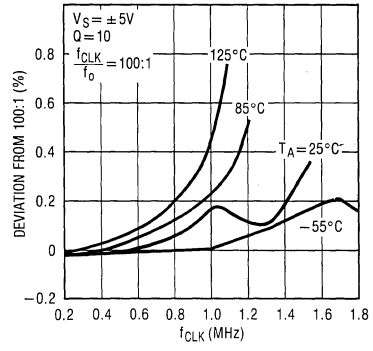
Graph 19. Mode 3 (R2 = R4): f_{CLK}/f_o vs f_{CLK} and Q



Graph 20. Mode 3 (R2 = R4): (f_{CLK}/f_o) vs f_{CLK} and Q

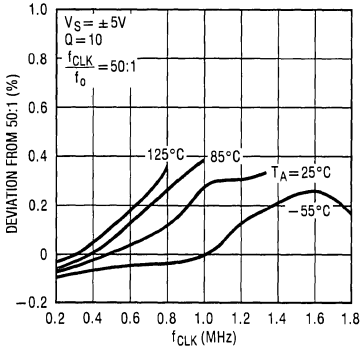


Graph 21. Mode 3 (R2 = R4): (f_{CLK}/f_o) vs f_{CLK} and Temperature

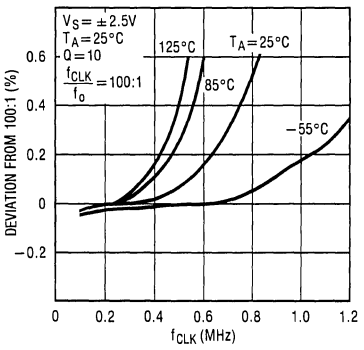


TYPICAL PERFORMANCE CHARACTERISTICS

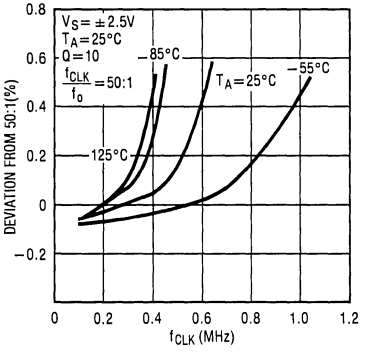
Graph 22. Mode 3 (R2 = R4): (f_{CLK}/f_o) vs f_{CLK} and Temperature



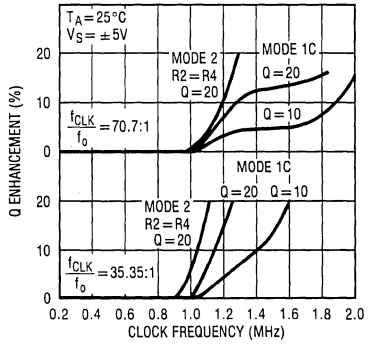
Graph 23. Mode 3 (R2 = R4): (f_{CLK}/f_o) vs f_{CLK} and Temperature



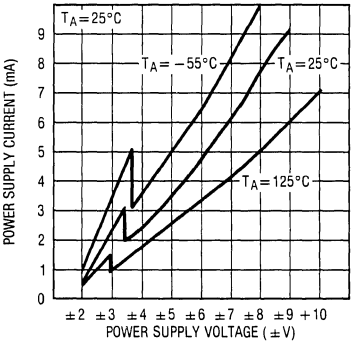
Graph 24. Mode 3 (R2 = R4): (f_{CLK}/f_o) vs f_{CLK} and Temperature



Graph 25. Mode 1c (R5 = 0), Mode 2 (R2 = R4) Q Error vs Clock Frequency



Graph 26. Supply Current vs Supply Voltage

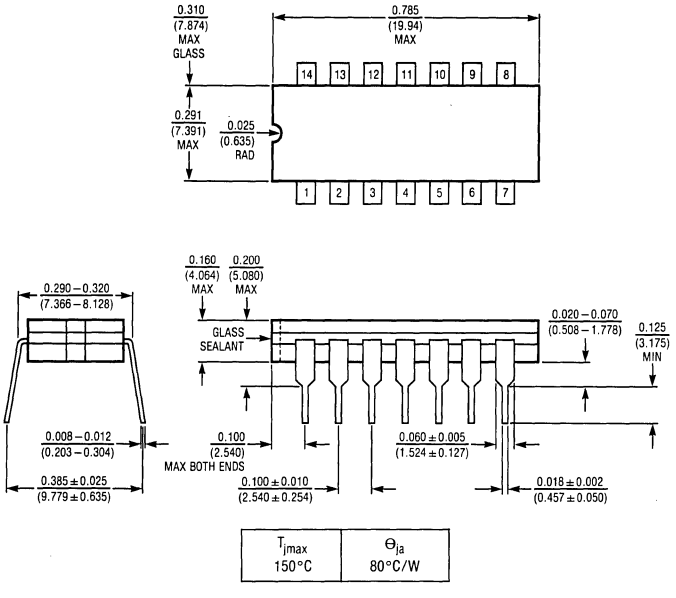


APPLICATIONS INFORMATION

The LTC1059 is compatible with the LTC1060. All the LTC1059 pins are functionally equivalent to the LTC1060 pins bearing the same title. For a detailed pin description and definition of various modes of operation refer to the LTC1060 data sheet. The LTC1059 is typically "faster" than the LTC1060 especially under single 5V (or ±2.5V) supply operation. This becomes apparent through the typical performance characteristics of the part. All the graphs shown in this data sheet have been drawn under the same test conditions as in the LTC1060 data sheet; they are also numbered in the same order. For a complete discussion of the filter characteristics see the LTC1060 data sheet.

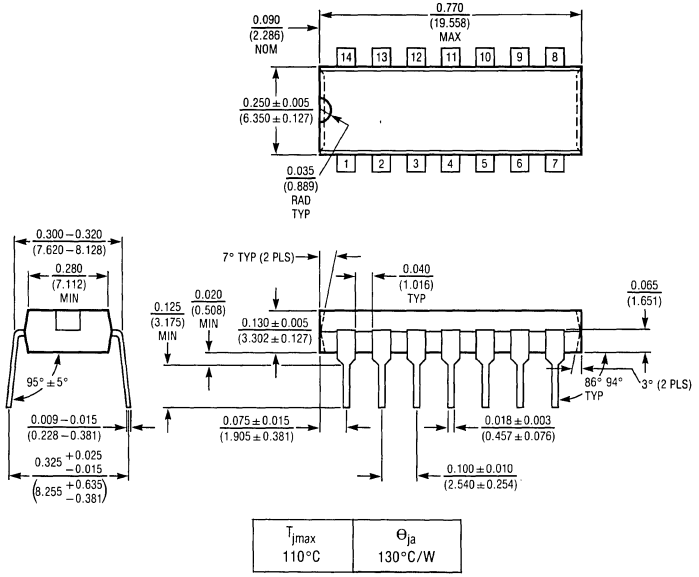
PACKAGE DESCRIPTION Dimensions in inches (millimeters) unless otherwise noted.

J Package
14 Lead Hermetic DIP



T_{jmax}	Θ_{ja}
150°C	80°C/W

N Package
14 Lead Plastic



T_{jmax}	Θ_{ja}
110°C	130°C/W

Universal Dual Filter Building Block

FEATURES

- *Guaranteed* Filter Specification for ±2.37V and ±5V Supply
- Operates up to 30kHz
- Low Power and 88dB Dynamic Range at ±2.5V Supply
- Center Frequency Q Product up to 1.6MHz
- *Guaranteed* Offset Voltages
- *Guaranteed* Clock to Center Frequency Accuracy over Temperature
  - 0.3% for LTC1060A
  - 0.8% for LTC1060
- *Guaranteed* Q Accuracy over Temperature
- Low Temperature Coefficient of Q and Center Frequency
- Low Crosstalk, 70dB
- Clock Inputs TTL and CMOS Compatible

APPLICATIONS

- Single 5V Supply Medium Frequency Filters
- Very High Q and High Dynamic Range Bandpass, Notch Filters
- Tracking Filters
- Telecom Filters

DESCRIPTION

The LTC1060 consists of two high performance, switched capacitor filters. Each filter, together with 2 to 5 resistors, can produce various 2nd order filter functions such as lowpass, bandpass, highpass notch and allpass. The center frequency of these functions can be tuned by an external clock, or by an external clock and resistor ratio. Up to 4th order full biquadratic functions can be achieved by cascading the two filter blocks. Any of the classical filter configurations (like Butterworth, Chebyshev, Bessel, Cauer) can be formed.

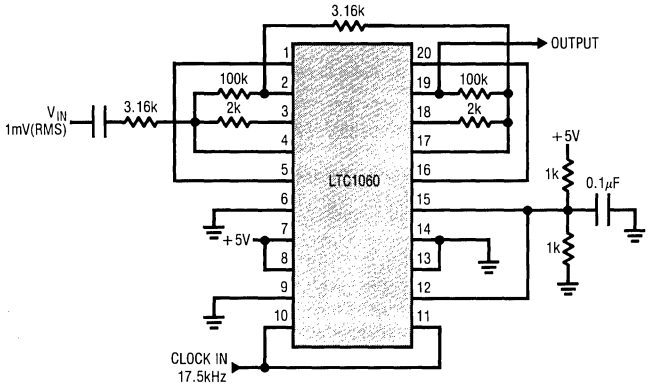
The LTC1060 operates with either a single or dual supply from ±2.37V to ±8V. When used with low supply (i.e. single 5V supply), the filter typically consumes 12mW and can operate with center frequencies up to 10kHz. With ±5V supply, the frequency range extends to 30kHz and very high Q values can also be obtained.

The LTC1060 is manufactured by using Linear Technology's enhanced LTCMOS™ silicon gate process. Because of this, low offsets, high dynamic range, high center frequency Q product and excellent temperature stability are obtained.

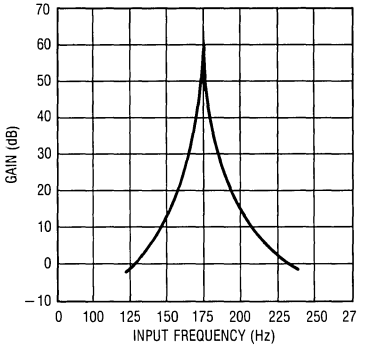
The LTC1060 is pinout compatible with MF10.

LTCMOS™ is a trademark of Linear Technology Corp.

Single 5V, Gain of 1000 4th Order Bandpass Filter



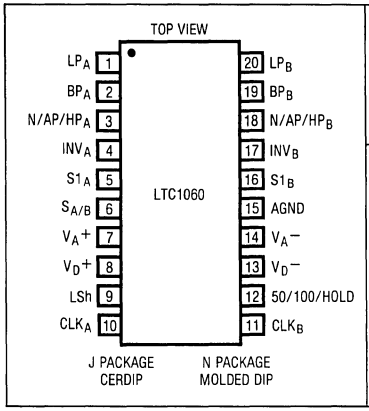
Amplitude Response



ABSOLUTE MAXIMUM RATINGS

Supply Voltage 18V
Power Dissipation 500mW
Operating Temperature Range
LTC1060AC, LTC1060C ..... $-40°C \le T_A \le 85°C$
LTC1060AM, LTC1060M ..... $-55°C \le T_A \le 125°C$
Storage Temperature Range ..... $-65°C$ to $150°C$
Lead Temperature (Soldering, 10sec.) ..... 300°C

PACKAGE/ORDER INFORMATION



ORDER PART NUMBER
LTC1060ACJ
LTC1060MJ
LTC1060ACN
LTC1060AMJ
LTC1060CN
LTC1060CJ

ELECTRICAL CHARACTERISTICS

(Complete Filter) $V_S = \pm 5V$, $T_A = 25°C$ unless otherwise specified.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Center Frequency Range (see Applications Information)	$f_0 \times Q \le 400kHz$, Mode 1, Figure 4			0.1-20K		Hz
	$f_0 \times Q \le 1.6MHz$, Mode 1, Figure 4			0.1-16K		Hz
Clock to Center Frequency Ratio						
LTC1060A	Mode 1, 50:1, $f_{CLK} = 250kHz$, Q = 10	●			50 ± 0.3%	
LTC1060	Mode 1, 50:1, $f_{CLK} = 250kHz$, Q = 10	●			50 ± 0.8%	
LTC1060A	Mode 1, 100:1, $f_{CLK} = 500kHz$, Q = 10	●			100 ± 0.3%	
LTC1060	Mode 1, 100:1, $f_{CLK} = 500kHz$, Q = 10	●			100 ± 0.8%	
Q accuracy						
LTC1060A	Mode 1, 50:1 or 100:1, $f_0 = 5kHz$	●		±0.5	3	%
LTC1060	Q = 10	●		±0.5	5	%
f_0 Temperature Coefficient	Mode 1, $f_{CLK} < 500kHz$			−10		ppm/°C
Q Temperature Coefficient	Mode 1, $f_{CLK} < 500kHz$, Q = 10			+20		ppm/°C
DC Offset V_{OS1}		●		2	15	mV
V_{OS2}	$f_{CLK} = 250kHz$, 50:1, $S_{A/B}$ High	●		3	30	mV
V_{OS2}	$f_{CLK} = 500kHz$, 100:1, $S_{A/B}$ High	●		6	60	mV
V_{OS2}	$f_{CLK} = 250kHz$, 50:1, $S_{A/B}$ Low	●		2	20	mV
V_{OS2}	$f_{CLK} = 500kHz$, 100:1, $S_{A/B}$ Low	●		4	40	mV
V_{OS3}	$f_{CLK} = 250kHz$, 50:1, $S_{A/B}$ Low	●		2	20	mV
V_{OS3}	$f_{CLK} = 500kHz$, 100:1, $S_{A/B}$ Low	●		4	40	mV
DC Low Pass Gain Accuracy	Mode 1, R1 = R2 = 50k			±0.1	2	%
BP Gain Accuracy at f_0	Mode 1, Q = 10, $f_0 = 5kHz$			±0.1		%
Clock Feedthrough	$f_{CLK} \le 1MHz$			10		mV(p-p)
Max. Clock Frequency				1.5		MHz
Power Supply Current			3	5	8	mA
		●			10	mA
Crosstalk				70		dB

ELECTRICAL CHARACTERISTICS (Complete Filter) $V_S = \pm 2.37V$, $T_A = 25°C$

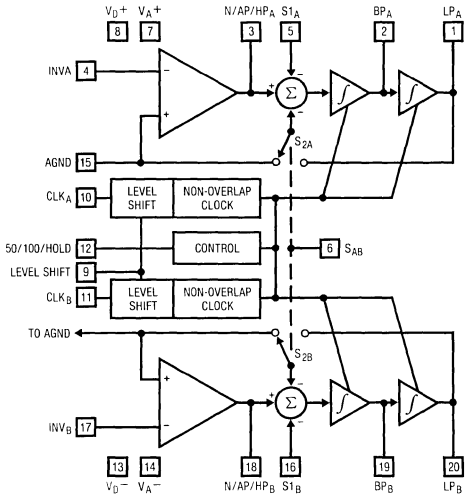
PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Center Frequency Range	$f_0 \times Q \leq 100kHz$			0.1-10k		Hz
Clock to Center Frequency Ratio						
LTC1060A	Mode 1, 50:1, $f_{CLK} = 250kHz$, Q = 10	●			50 ± 0.5%	
LTC1060	Mode 1, 50:1, $f_{CLK} = 250kHz$, Q = 10			50 ± 0.8%		
LTC1060A	Mode 1, 100:1, $f_{CLK} = 250kHz$, Q = 10	●		100 ± 0.5%		
LTC1060	Mode 1, 100:1, $f_{CLK} = 250kHz$, Q = 10			100 ± 0.8%		
Q Accuracy						
LTC1060A	Mode 1, $f_0 = 2.5kHz$, Q = 10			±2		%
LTC1060				±4		%
Max Clock Frequency				500		kHz
Power Supply Current				2.5	4	mA

ELECTRICAL CHARACTERISTICS (Internal Op Amps) $T_A = 25°C$

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Voltage Range			±2.37		±8	V
Voltage Swings						
LTC1060A			±4	±4		V
LTC1060	$V_S = \pm 5V$, $R_L = 5k$ (Pins 1, 2, 19, 20)		±3.8	±4		V
LTC1060, LTC1060A	$R_L = 3.5k$ (Pins 3, 18)	●	±3.6	±4		V
Output Short Circuit Current	$V_S = \pm 5V$					
Source				25		mA
Sink				3		mA
Op Amp GBW Product	$V_S = \pm 5V$			2		MHz
Op Amp Slew Rate	$V_S = \pm 5V$			7		V/μs
Op Amp DC Open Loop Gain	$R_L = 10k$, $V_S = \pm 5V$			85		dB

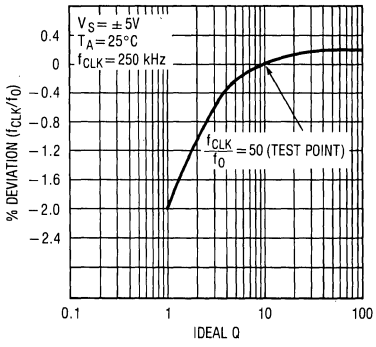
The ● denotes the specifications which apply over the full operating temperature range.

BLOCK DIAGRAM

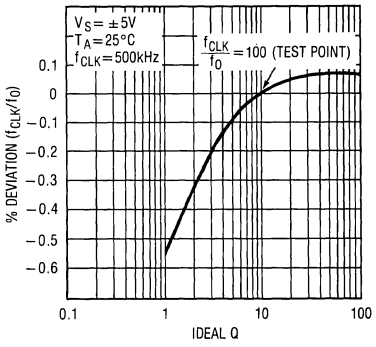


TYPICAL PERFORMANCE CHARACTERISTICS

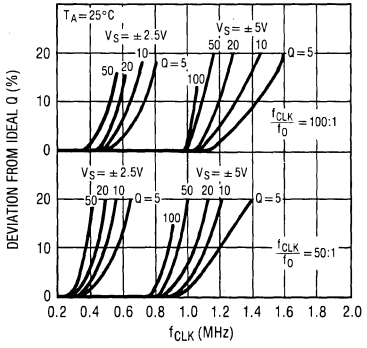
Graph 1. Mode 1: (f_{CLK}/f_o) Deviation vs Q



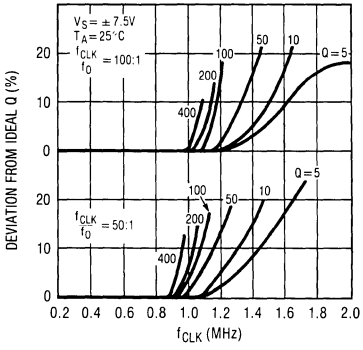
Graph 2. Mode 1: (f_{CLK}/f_o) Deviation vs Q



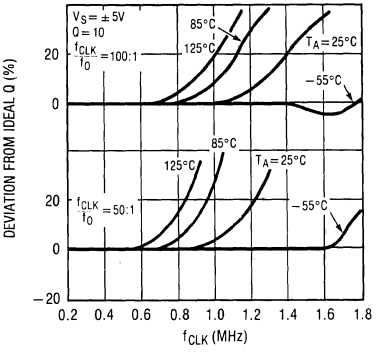
Graph 3. Mode 1: Q Error vs Clock Frequency



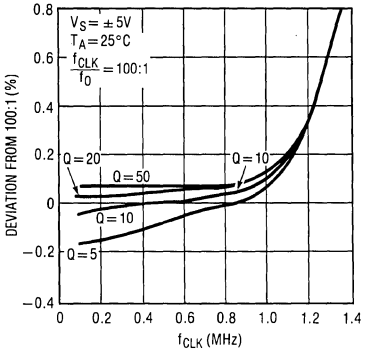
Graph 4. Mode 1: Q Error vs Clock Frequency



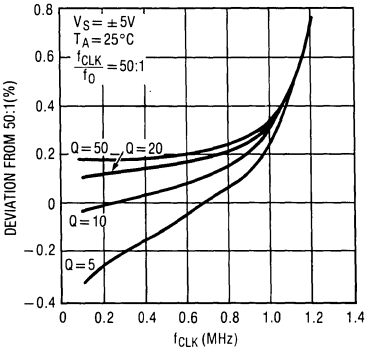
Graph 5. Mode 1: Measured Q vs f_{CLK} and Temperature



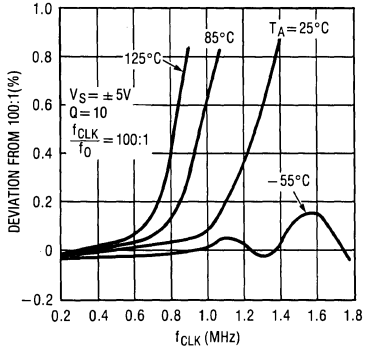
Graph 6. Mode 1: (f_{CLK}/f_o) vs f_{CLK} and Q



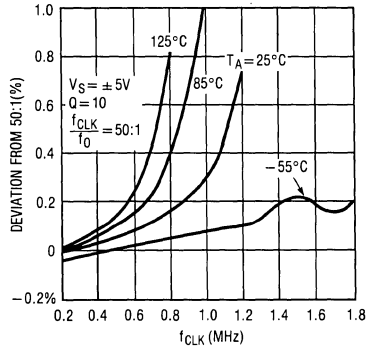
Graph 7. Mode 1: (f_{CLK}/f_o) vs f_{CLK} and Q



Graph 8. Mode 1: (f_{CLK}/f_o) vs f_{CLK} and Temperature

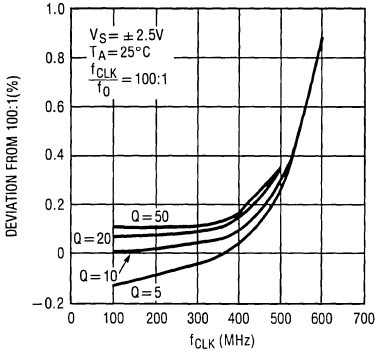


Graph 9. Mode 1: (f_{CLK}/f_o) vs f_{CLK} and Temperature

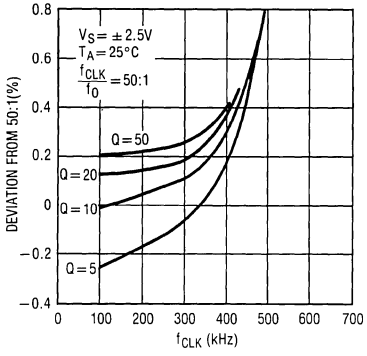


TYPICAL PERFORMANCE CHARACTERISTICS

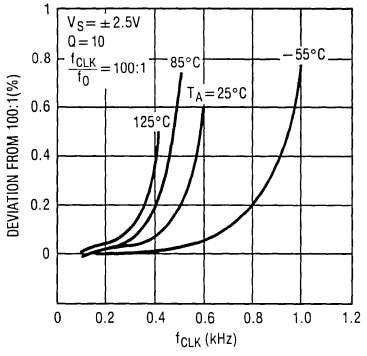
Graph 10. Mode 1: (f_{CLK}/f_o) vs f_{CLK} and Q



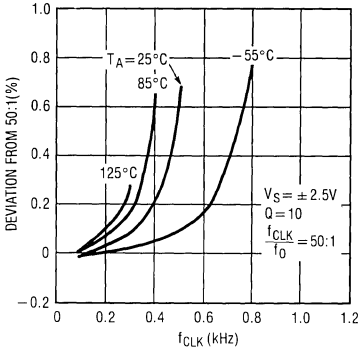
Graph 11. Mode 1: (f_{CLK}/f_o) vs f_{CLK} and Q



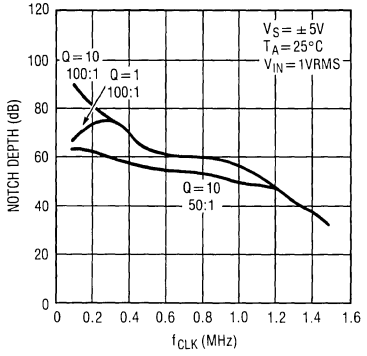
Graph 12. Mode 1: (f_{CLK}/f_o) vs f_{CLK} and Temperature



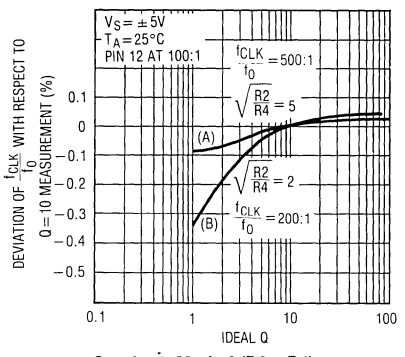
Graph 13. Mode 1: (f_{CLK}/f_o) vs f_{CLK} and Temperature



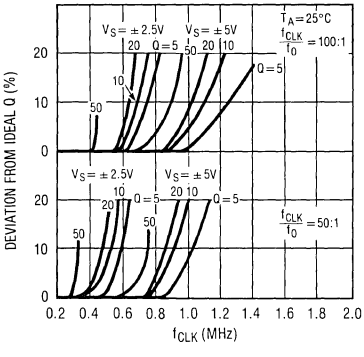
Graph 14. Mode 1: Notch Depth vs Clock Frequency



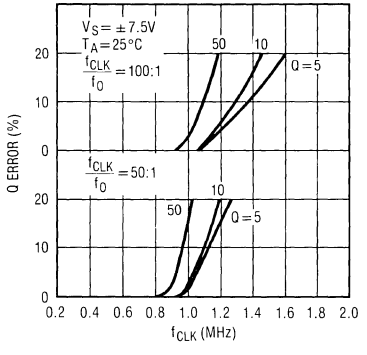
Graph 15. Mode 3: Deviation of (f_{CLK}/f_o) with Respect to Q = 10 Measurement



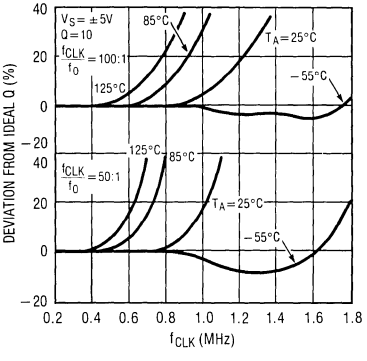
Graph 16. Mode 3: Q Error vs Clock Frequency



Graph 17. Mode 3 (R2 = R4): Q Error vs Clock Frequency

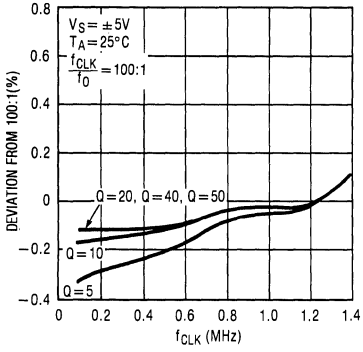


Graph 18. Mode 3 (R2 = R4): Measured Q vs f_{CLK} and Temperature

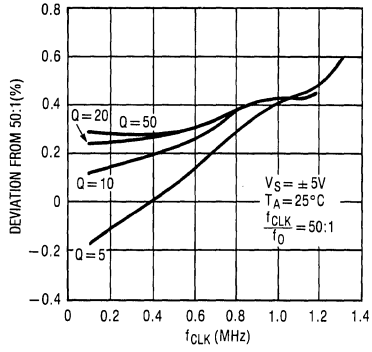


TYPICAL PERFORMANCE CHARACTERISTICS

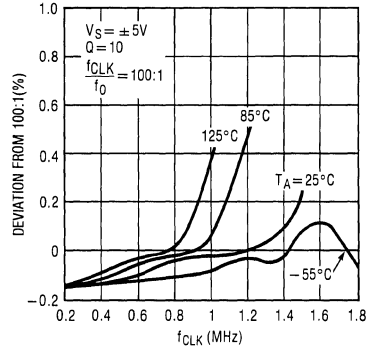
Graph 19. Mode 3 (R2 = R4): f_{CLK}/f_o vs f_{CLK} and Q



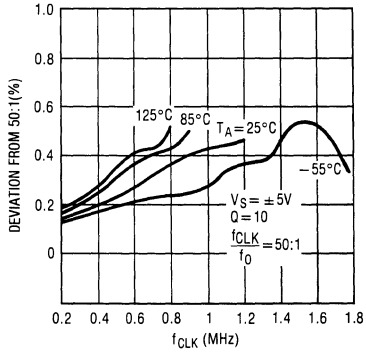
Graph 20. Mode 3 (R2 = R4): (f_{CLK}/f_o) vs f_{CLK} and Q



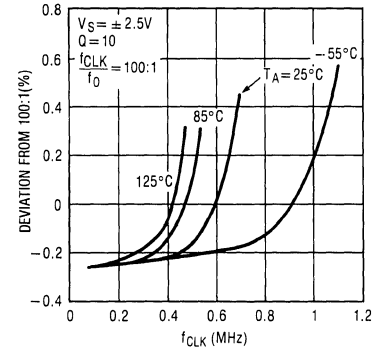
Graph 21. Mode 3 (R2 = R4): (f_{CLK}/f_o) vs f_{CLK} and Temperature



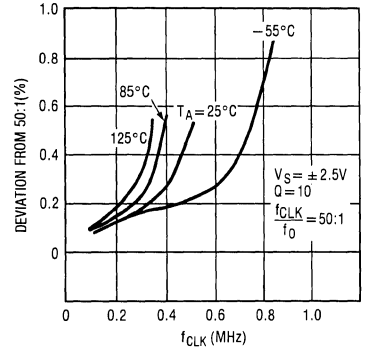
Graph 22. Mode 3 (R2 = R4): (f_{CLK}/f_o) vs f_{CLK} and Temperature



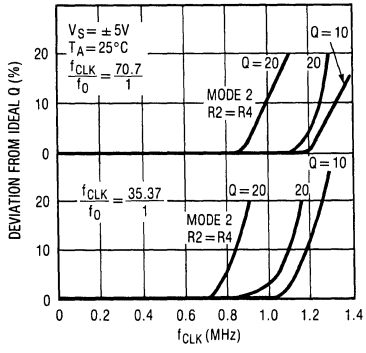
Graph 23. Mode 3 (R2 = R4): (f_{CLK}/f_o) vs f_{CLK} and Temperature



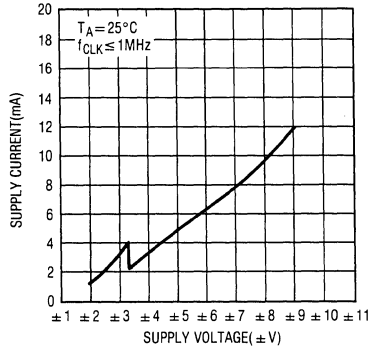
Graph 24. Mode 3 (R2 = R4): (f_{CLK}/f_o) vs f_{CLK} and Temperature



Graph 25. Mode 1c (R5 = 0), Mode 2 (R2 = R4) Q Error vs Clock Frequency



Graph 26. Supply Current vs Supply Voltage



PIN DESCRIPTIONS AND APPLICATIONS INFORMATION

Power Supplies

The V_A^+ and V_D^+ (pins 7 and 8) and the V_A^-, V_D^- (pins 14 and 13) are, respectively, the analog and digital positive and negative supply pins. For most cases, pins 7 and 8 should be tied together and bypassed by a 0.1μF disc ceramic capacitor. The same holds for pins 14 and 13. If the LTC1060 operates in high digital noise environment, the supply pins can be bypassed separately. Pins 7 and 8 are internally connected through the IC substrate and should be biased from the same DC source. Pins 14 and 13 should also be biased from the same DC source.

The LTC1060 is designed to operate with ±2.5V supply (or single 5V) and with ±5V to ±8V supplies. The minimum supply, where the filter operates reliably, is ±2.37V. With low supply operation, the maximum input clock frequency is about 500kHz. Beyond this, the device exhibits excessive Q enhancement and center frequency errors.

Clock Input Pins and Level Shift

The level shift (LSh) pin 9 is used to accommodate T^2L or CMOS clock levels. With dual supplies equal or higher to ±4.5V, pin 9 should be connected to ground (same potential as the AGND pin). Under these conditions the clock levels can be T^2L or CMOS. With single supply operation, the negative supply pins and the LSh pin should be tied to the system ground. The AGND, pin 15, should be biased at 1/2 supplies, as shown in the "Single 5V Gain of 1000 4th Order Bandpass Filter" circuit. Again, under these conditions, the clock levels can be T^2L or CMOS. The input clock pins (10, 11) share the same level shift pin. The clock logic threshold level over temperature is typically 1.5V ± 0.1V above the LSh pin potential. The duty cycle of the input clock should be close to 50%. For clock frequencies below 1MHz, the (f_{CLK}/f_o) ratio is independent from the clock input levels and from its rise and fall times. Fast rising clock edges, however, improve the filter DC offsets. For clock frequencies above 1MHz, T^2L level clocks are recommended.

50/100/Hold (Pin 12)

By tying pin 12 to (V_A^+, V_D^+), the filter operates in the 50:1 mode. With ±5V supplies pin 12 can be typically 1V below the positive supply without affecting the 50:1 operation of the device. By tying pin 12 to 1/2 supplies (which should be the AGND potential), the LTC1060 operates in the 100:1 mode. The 1/2 supply bias of pin 12 can vary around the 1/2 supply potential without affecting the 100:1 filter operation. This is shown in Table 1.

When pin 12 is shorted to the negative supply pin, the filter operation is stopped and the bandpass and lowpass outputs act as a S/H circuit holding the last sample. The hold step is 20mV and the droop rate is 150μV/second!

Table 1

Total Power Supply	Voltage Range of Pin 12 for 100:1 Operation
+5V	2.5V ± 0.5V
+10V	+5V ± 1V
+15V	+7.5V ± 1.5V

$S1_A$, $S1_B$ (Pins 5 and 16)

These are voltage signal input pins and, if used, they should be driven with a source impedance below 5kΩ. The $S1_A$, $S1_B$ pins can be used to alter the CLK to center frequency ratio (f_{CLK}/f_o) of the filter (see Modes 1b, 1c, 2a, 2b) or to feedforward the input signal for allpass filter configurations (see Modes 4 and 5). When these pins are not used, they should be tied to the AGND pin.

$S_{A/B}$ (Pin 6)

When $S_{A/B}$ is high, the S2 input of the filter's voltage summer (see Block Diagram) is tied to the lowpass output. This frees the S1 pin to realize various modes of operation for improved applications flexibility. When the $S_{A/B}$ pin is connected to the negative supply, the S2 input switches to ground and internally becomes inactive. This improves the filter noise performance and typically lowers the value of the offset V_{OS2}.

AGND (Pin 15)

This should be connected to the system ground for dual supply operation. When the LTC1060 operates with a single positive supply, the analog ground pin should be tied to 1/2 supply and bypassed with a 0.1μF capacitor, as shown in the application, "Single 5V, Gain of 1000 4th Order Bandpass Filter". The positive inputs of all the internal op amps, as well as the reference point of all the internal

APPLICATIONS INFORMATION

switches are connected to the AGND pin. Because of this, a "clean" ground is recommended.

f_{CLK}/f_0 Ratio

The (f_{CLK}/f_0) reference of 100:1 or 50:1 is derived from the filter center frequency measured in mode 1, with a Q = 10 and $V_S = \pm 5V$. The clock frequencies are, respectively, 500kHz/250kHz for the 100:1/50:1 measurement. All the curves shown in the Typical Performance Characteristics section are normalized to the above references.

Graphs 1 and 2 in the Typical Performance Characteristics show the (f_{CLK}/f_0) variation versus values of ideal Q. The LTC1060 is a sampled data filter and it only approximates continuous time filters. In this data sheet, the LTC1060 is treated in the frequency domain because this approximation is good enough for most filter applications. The LTC1060 deviates from its ideal continuous filter model when the (f_{CLK}/f_0) ratio decreases and when the Q's are low. Since low Q filters are not selective, the frequency domain approximation is well justified. In graph 15 the LTC1060 is connected in mode 3 and its (f_{CLK}/f_0) ratio is adjusted to 200:1 and 500:1. Under these conditions, the filter is over-sampled and the (f_{CLK}/f_0) curves are nearly independent of the Q values. In mode 3, the (f_{CLK}/f_0) ratio typically deviates from the tested one in mode 1 by ±0.1%.

$f_0 \times Q$ Product Ratio

This is a figure of merit of general purpose active filter building blocks. The $f_0 \times Q$ product of the LTC1060 depends on the clock frequency, the power supply voltages, the junction temperature and the mode of operation.

At 25°C ambient temperature for ±5V supplies, and for clock frequencies below 1MHz, in mode 1 and its derivatives, the $f_0 \times Q$ product is mainly limited by the desired f_0 and Q accuracy. For instance, from graph 4 at 50:1 and for f_{CLK} below 800kHz a predictable ideal Q of 400 can be obtained. Under this condition, a respectable $f_0 \times Q$ product of 6.4MHz is achieved. The 16kHz center frequency will be about 0.22% off from the tested value at 250kHz clock (see graph 1). For the same clock frequency of 800kHz and for the same Q value of 400, the $f_0 \times Q$ product can be further increased if the clock to center frequency ratio is lowered below 50:1. In mode 1c with R5 = 0 and R6 = ∞, the (f_{CLK}/f_0) ratio is $50/\sqrt{2}$. The $f_0 \times Q$ product can now be increased to 9MHz since, with the same clock frequency and same Q value, the filter can handle a center frequency of $16kHz \times \sqrt{2}$.

For clock frequencies above 1MHz, the $f_0 \times Q$ product is limited by the clock frequency itself. From graph 4 at ±7.5V supply, 50:1, and 1.4MHz clock, a Q of 5 has about 8% error; the measured 28kHz center frequency was skewed by 0.8% with respect to the guaranteed value at 250kHz clock. Under these conditions, the $f_0 \times Q$ product is only 140kHz, but the filter can handle higher input signal frequencies than the 800kHz clock frequency-very high Q case described above.

Mode 3, Figure 11, and the modes of operation where R4 is finite, are "slower" than the basic mode 1. This is shown in graph 16 and 17. The resistor R4 places the input op amp inside the resonant loop. The finite GBW of this op amp creates an additional phase shift and enhances the Q value at high clock frequencies. Graph 16 was drawn with a small capacitor, C_C, placed across R4 and as such, at $V_S = \pm 5V$, the $(1/2\pi R4C_C) = 2MHz$. With $V_S = \pm 2.5V$ the $(1/2\pi R4C_C)$ should be equal to 1.4MHz. This allows the Q curve to be slightly "flatter" over a wider range of clock frequencies. If, at ±5V supply, the clock is below 900kHz (or 400kHz for $V_S = \pm 2.5V$), this capacitor, C_C, is not needed.

For graph 25, the clock to center frequency ratios are altered to 70.7:1 and 35.35:1. This is done by using mode 1c with R5 = 0, Figure 7, or mode 2 with R2 = R4 = 10kΩ. The mode 1c, where the input op amp is outside the main loop, is much faster. Mode 2, however, is more versatile. At 50:1, and for $T_A = 25°C$ the mode 1c can be tuned for center frequencies up to 30kHz.

Output Noise

The wideband rms noise of the LTC1060 outputs is nearly independent from the clock frequency provided that the clock itself does not become part of the noise. The LTC1060 noise slightly decreases with ±2.5V supply. The noise at the BP and LP outputs increases for high Q's. Table 2 shows typical values of wideband rms noise. The numbers in parentheses are the noise measurement in mode 1 with the $S_{A/B}$ pin shorted to V^- as shown in Figure 25.

APPLICATIONS INFORMATION

Table 2. Wideband rms Noise

V_s	$\frac{f_{CLK}}{f_o}$	Notch/HP (μVrms)	BP (μVrms)	LP (μVrms)	CONDITIONS
±5V	50:1	49 (42)	52 (43)	75 (65)	Mode 1, R1 = R2 = R3
±5V	100:1	70 (55)	80 (58)	90 (88)	Q = 1
±2.5V	50:1	33 (31)	36 (32)	48 (43)	
±2.5V	100:1	48 (40)	52 (40)	66 (55)	
±5V	50:1	20 (18)	150(125)	186 (155)	Mode 1, Q = 10
±5V	100:1	25 (21)	220 (160)	240 (180)	R1 = R3 for BP out
±2.5V	50:1	16 (15)	100 (80)	106 (87)	R1 = R2 for LP out
±2.5V	100:1	20 (17)	150 (105)	150 (119)	
±5V	50:1	57	57	62	Mode 3, R1 = R2 = R3 = R4
±5V	100:1	72	72	80	Q = 1
±2.5V	50:1	40	40	42	
±2.5V	100:1	50	50	53	
±5V	50:1	135	120	140	Mode 3, R2 = R4, Q = 10
±5V	100:1	170	160	185	R3 = R1 for BP out
±2.5V	50:1	100	88	100	R4 = R1 for LP and HP out
±2.5V	100:1	125	115	130	

Short Circuit Currents

Short circuits to ground, positive or negative power supply are allowed as long as the power supplies do not exceed ±5V and the ambient temperature stays below 85°C. Above ±5V and at elevated temperatures, continuous short circuits to the negative power supply will cause excessive currents to flow. Under these conditions, the device will get damaged if the short circuit current is allowed to exceed 80mA.

DEFINITION OF FILTER FUNCTIONS

Each building block of the LTC1060, together with an external clock and a few resistors, closely approximates 2nd order filter functions. These are tabulated below in the frequency domain.

1. **Bandpass function:** available at the bandpass output pins (2, 19), Figure 1.

$$G(s) = H_{OBP}\frac{s\omega_0/Q}{s^2 + (s\omega_0/Q) + \omega_0^2}$$

H_{OBP} = Gain at $\omega = \omega_0$

$f_0 = \omega_0/2\pi$; f_0 is the center frequency of the complex pole pair. At this frequency, the phase shift between input and output is −180°.

Q = Quality factor of the complex pole pair. It is the ratio of f_0 to the −3dB bandwidth of the 2nd order bandpass function. The Q is always measured at the filter BP output.

2. **Lowpass function:** available at the LP output pins (1, 20), Figure 2.

$$G(s) = H_{OLP}\frac{\omega_0^2}{s^2 + s(\omega_0/Q) + \omega_0^2}$$

H_{OLP} = DC gain of the LP output.

DEFINITION OF FILTER FUNCTIONS

3. **Highpass function:** available only in mode 3 at the output pins (3, 18), Figure 3.

$$G(s) = H_{OHP}\ \frac{s^2}{s^2 + s(\omega_0/Q) + \omega_0^2}$$

H_{OHP} = gain of the HP output for $f \rightarrow \frac{f_{CLK}}{2}$

4. **Notch function:** available at pins 3 (18) for several modes of operation.

$$G(s) = (H_{ON2})\ \frac{(s^2 + \omega_n^2)}{s^2 + s(\omega_0/Q) + \omega_0^2}$$

H_{ON2} = gain of the notch output for $f \rightarrow \frac{f_{CLK}}{2}$

H_{ON1} = gain of the notch output for $f \rightarrow 0$

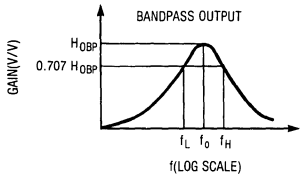
$f_n = \omega_n/2\pi$; f_n is the frequency of the notch occurrence.

5. **Allpass function:** available at pins 3(18) for mode 4, 4a.

$$G(s) = H_{OAP}\frac{[s^2 - s(\omega_0/Q) + \omega_0^2]}{s^2 + s(\omega_0/Q) + \omega_0^2}$$

H_{OAP} = gain of the allpass output for $0 < f < \frac{f_{CLK}}{2}$

For allpass functions, the center frequency and the Q of the numerator complex zero pair is the same as the denominator. Under these conditions, the magnitude response is a straight line. In mode 5, the center frequency f_z, of the numerator complex zero pair, is different than f_0. For high numerator Q's, the magnitude response will have a notch at f_z.

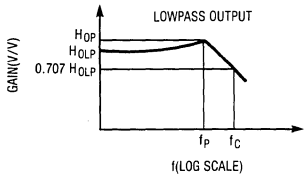


$$Q = \frac{f_0}{f_H - f_L};\ f_0 = \sqrt{f_L f_H}$$

$$f_L = f_0\left(\frac{-1}{2Q} + \sqrt{\left(\frac{1}{2Q}\right)^2 + 1}\right)$$

$$f_H = f_0\left(\frac{1}{2Q} + \sqrt{\left(\frac{1}{2Q}\right)^2 + 1}\right)$$

Figure 1

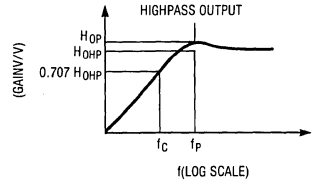


$$f_C = f_0 \times \sqrt{\left(1 - \frac{1}{2Q^2}\right) + \sqrt{\left(1 - \frac{1}{2Q^2}\right)^2 + 1}}$$

$$f_P = f_0\sqrt{1 - \frac{1}{2Q^2}}$$

$$H_{OP} = H_{OLP} \times \frac{1}{\frac{1}{Q}\sqrt{1 - \frac{1}{4Q^2}}}$$

Figure 2



$$f_C = f_0 \times \left[\sqrt{\left(1 - \frac{1}{2Q^2}\right) + \sqrt{\left(1 - \frac{1}{2Q^2}\right)^2 + 1}}\right]^{-1}$$

$$f_P = f_0 \times \left[\sqrt{1 - \frac{1}{2Q^2}}\right]^{-1}$$

$$H_{OP} = H_{OHP} \times \frac{1}{\frac{1}{Q}\sqrt{1 - \frac{1}{4Q^2}}}$$

Figure 3

MODES OF OPERATION

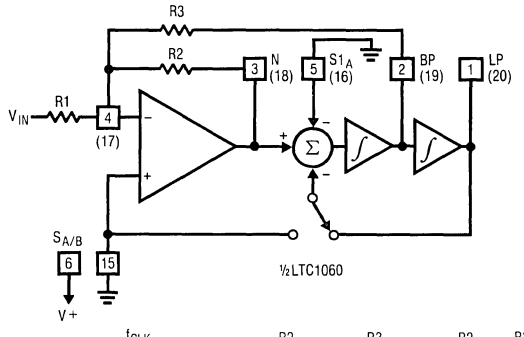
Table 3. Modes of Operation: 1st Order Functions

Mode	Pin 2 (19)	Pin 3 (18)	f_C	f_Z
6a	LP	HP	$\frac{f_{CLK}}{100(50)} \times \frac{R2}{R3}$	
6b	LP	LP	$\frac{f_{CLK}}{100(50)} \times \frac{R2}{R3}$	
7	LP	AP	$\frac{f_{CLK}}{100(50)} \times \frac{R2}{R3}$	$\frac{f_{CLK}}{100(50)} \times \frac{R2}{R3}$

MODES OF OPERATION

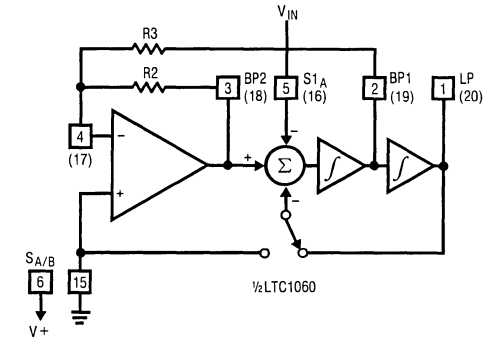
Table 4. Modes of Operation: 2nd Order Functions

Mode	Pin 1 (20)	Pin 2 (19)	Pin 3 (18)	f_o	f_N
1	LP	BP	Notch	$\frac{f_{CLK}}{100(50)}$	f_o
1a	LP	BP	BP	$\frac{f_{CLK}}{100(50)}$	
1b	LP	BP	Notch	$\frac{f_{CLK}}{100(50)} \times \sqrt{\frac{R6}{R5+R6}}$	$\frac{f_{CLK}}{100(50)} \times \sqrt{\frac{R6}{R5+R6}}$
1c	LP	BP	Notch	$\frac{f_{CLK}}{100(50)} \times \sqrt{1+\frac{R6}{R5+R6}}$	$\frac{f_{CLK}}{100(50)} \times \sqrt{1+\frac{R6}{R5+R6}}$
2	LP	BP	Notch	$\frac{f_{CLK}}{100(50)} \times \sqrt{1+\frac{R2}{R4}}$	$\frac{f_{CLK}}{100(50)}$
2a	LP	BP	Notch	$\frac{f_{CLK}}{100(50)} \times \sqrt{1+\frac{R2}{R4}+\frac{R6}{R5+R6}}$	$\frac{f_{CLK}}{100(50)} \times \sqrt{1+\frac{R6}{R5+R6}}$
2b	LP	BP	Notch	$\frac{f_{CLK}}{100(50)} \times \sqrt{\frac{R2}{R4}+\frac{R6}{R5+R6}}$	$\frac{f_{CLK}}{100(50)} \times \sqrt{\frac{R6}{R5+R6}}$
3	LP	BP	HP	$\frac{f_{CLK}}{100(50)} \times \sqrt{\frac{R2}{R4}}$	
3a	LP	BP	Notch	$\frac{f_{CLK}}{100(50)} \times \sqrt{\frac{R2}{R4}}$	$\frac{f_{CLK}}{100(50)} \times \sqrt{\frac{R_h}{R_l}}$
4	LP	BP	AP	$\frac{f_{CLK}}{100(50)}$	
4a	LP	BP	AP	$\frac{f_{CLK}}{100(50)} \times \sqrt{\frac{R2}{R4}}$	
5	LP	BP	C.Z	$\frac{f_{CLK}}{100(50)} \times \sqrt{1+\frac{R2}{R4}}$	$\frac{f_{CLK}}{100(50)} \times \sqrt{1-\frac{R1}{R4}}$



$f_o = \frac{f_{CLK}}{100(50)}$; $f_n = f_o$; $H_{OLP} = -\frac{R2}{R1}$; $H_{OBP} = -\frac{R3}{R1}$; $H_{ON1} = -\frac{R2}{R1}$ $Q = \frac{R3}{R1}$

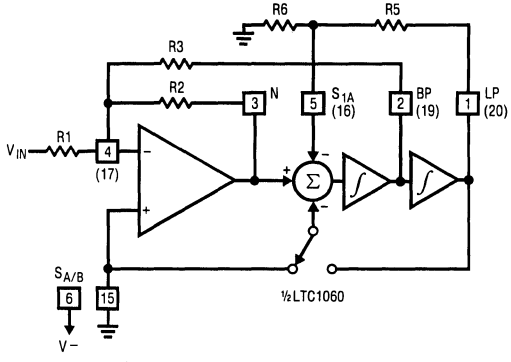
Figure 4. Mode 1: 2nd Order Filter Providing Notch, Bandpass, Lowpass



$f_o = \frac{f_{CLK}}{100(50)}$; $Q = \frac{R3}{R2}$; $H_{OBP1} = -\frac{R3}{R2}$; $H_{OBP2} = 1$(NONINVERTING) $H_{OLP} = -1$

Figure 5. Mode 1a: 2nd Order Filter Providing Bandpass, Lowpass

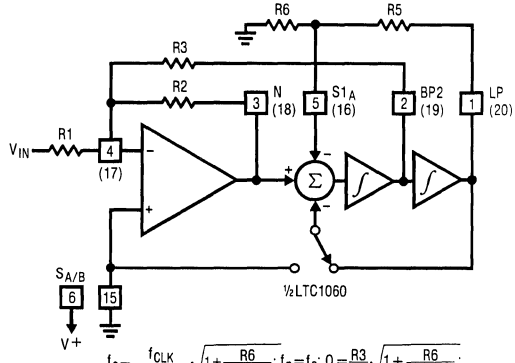
MODES OF OPERATION



$$f_o=\frac{f_{CLK}}{100(50)}\sqrt{\frac{R6}{R5+R6}};\ f_n=f_o;\ Q=\frac{R3}{R2}\sqrt{\frac{R6}{R5+R6}};$$

$$H_{ON1}(f\rightarrow 0)=H_{ON2}\left(f\rightarrow\frac{f_{CLK}}{2}\right)=-\frac{R2}{R1};\ H_{OLP}=\frac{-R2/R1}{R6/(R5+R6)};\ H_{OBP}=-\frac{R3}{R1};\ R5<5k\Omega$$

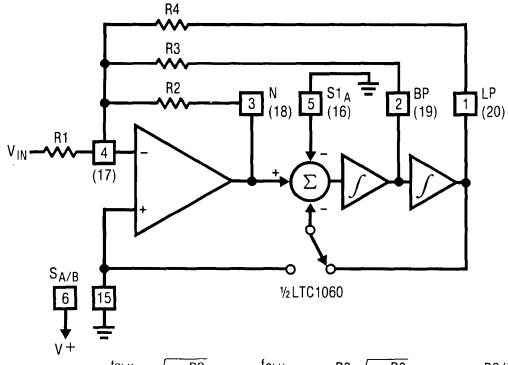
Figure 6. Mode 1b: 2nd Order Filter Providing Notch, Bandpass, Lowpass



$$f_o=\frac{f_{CLK}}{100(50)}\sqrt{1+\frac{R6}{R5+R6}};\ f_n=f_o;\ Q=\frac{R3}{R2}\sqrt{1+\frac{R6}{R5+R6}};$$

$$H_{ON1}(f\rightarrow 0)=H_{ON2}\left(f\rightarrow\frac{f_{CLK}}{2}\right)=-\frac{R2}{R1};H_{OBP}=-\frac{R3}{R1};\ H_{OLP}=\frac{-R2/R1}{1+R6/(R5+R6)};\ R5<5k\Omega$$

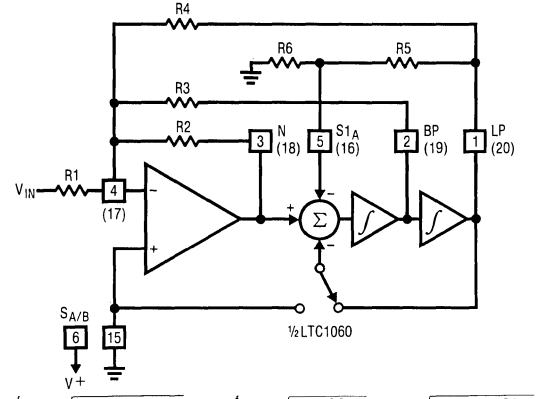
Figure 7. Mode 1c: 2nd Order Filter Providing Notch, Bandpass, Lowpass



$$f_o=\frac{f_{CLK}}{100(50)}\sqrt{1+\frac{R2}{R4}};\ f_n=\frac{f_{CLK}}{100(50)};\ Q=\frac{R3}{R2}\sqrt{1+\frac{R2}{R4}};\ H_{OLP}=\frac{-R2/R1}{1+(R2/R4)}$$

$$H_{OBP}=-R3/R1;\ H_{ON1}(f\rightarrow 0)=\frac{-R2/R1}{1+(R2/R4)};\ H_{ON2}\left(f\rightarrow\frac{f_{CLK}}{2}\right)=-R2/R1$$

Figure 8. Mode 2: 2nd Order Filter Providing Notch, Bandpass, Lowpass



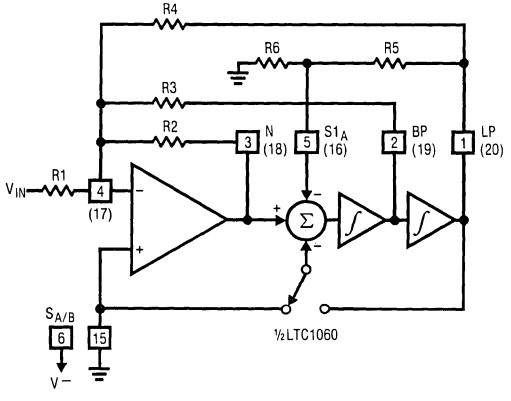
$$f_o=\frac{f_{CLK}}{100(50)}\sqrt{1+\frac{R2}{R4}+\frac{R6}{R5+R6}};\ f_n=\frac{f_{CLK}}{100(50)}\sqrt{1+\frac{R6}{R5+R6}};\ Q=\frac{R3}{R2}\sqrt{1+\frac{R2}{R4}+\frac{R6}{R5+R6}}$$

$$H_{ON1}(f\rightarrow 0)=-\frac{R2}{R1}\left\{\frac{1+R6/(R5+R6)}{1+(R2/R4)+[R6/(R5+R6)]}\right\};\ H_{ON2}\left(f\rightarrow\frac{f_{CLK}}{2}\right)=-R2/R1$$

$$H_{OBP}=-R3/R1;\ H_{OLP}=\frac{-R2/R1}{1+(R2/R4)+[R6/(R5+R6)]}$$

Figure 9. Mode 2a: 2nd Order Filter Providing Notch, Bandpass, Lowpass

MODES OF OPERATION

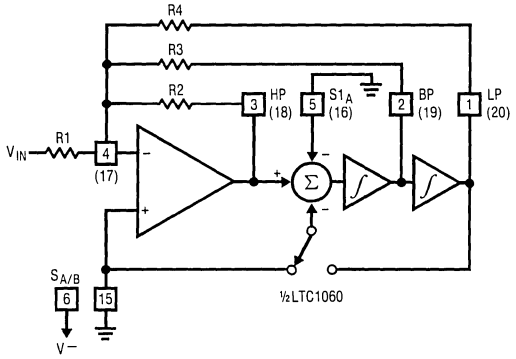


$$f_o = \frac{f_{CLK}}{100(50)}\sqrt{\frac{R2}{R4} + \frac{R6}{R5+R6}};\ f_n = \frac{f_{CLK}}{100(50)}\sqrt{\frac{R6}{R5+R6}};\ Q = \frac{R3}{R2}\sqrt{\frac{R2}{R4} + \frac{R6}{R5+R6}}$$

$$H_{ON1}(f \to 0) = -\frac{R2}{R1}\left\{\frac{R6/(R5+R6)}{[(R2/R4)+[R6/(R5+R6)]}\right\};\ H_{ON2}\left(f \to \frac{f_{CLK}}{2}\right) = -R2/R1$$

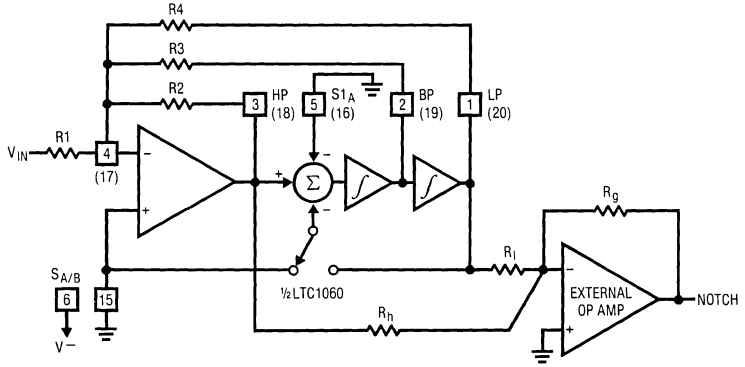
$$H_{OBP} = -R3/R1;\ H_{OLP} = \frac{-R2/R1}{(R2/R4)+[R6/(R5+R6)]}$$

Figure 10. Mode 2b: 2nd Order Filter Providing Notch, Bandpass, Lowpass



$$f_o = \frac{f_{CLK}}{100(50)}\sqrt{\frac{R2}{R4}};\ Q = \frac{R3}{R2}\sqrt{\frac{R2}{R4}};\ H_{OHP} = -R2/R1;\ H_{OBP} = -R3/R1;\ H_{OLP} = -R4/R1$$

Figure 11. Mode 3: 2nd Order Filter Providing Highpass, Bandpass, Lowpass

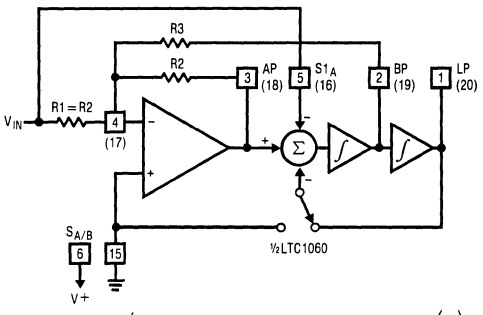


$$f_o = \frac{f_{CLK}}{100(50)}\sqrt{\frac{R2}{R4}};\ f_n = \frac{f_{CLK}}{100(50)}\sqrt{\frac{R_h}{R_i}};\ H_{OHP} = -R2/R1;\ H_{OBP} = -R3/R1,\ H_{OLP} = -R4/R1$$

$$H_{ON1}(f \to 0) = \frac{R_g}{R_i} \times \frac{R4}{R1};\ H_{ON2}\left(f \to \frac{f_{CLK}}{2}\right) = \frac{R_g}{R_h} \times \frac{R2}{R1};\ H_{ON}(f = f_o) = Q\left(\frac{R_g}{R_i} H_{OLP} - \frac{R_g}{R_h} H_{OHP}\right)$$

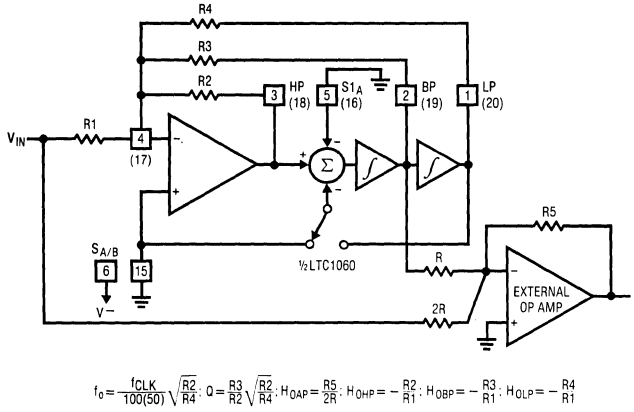
Figure 12. Mode 3a: 2nd Order Filter Providing Highpass, Bandpass, Lowpass, Notch

MODES OF OPERATION



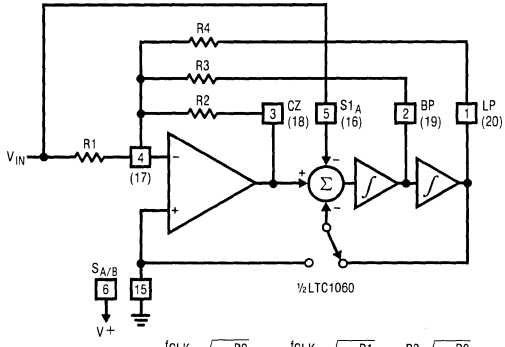
$$f_o = \frac{f_{CLK}}{100(50)};\ Q = \frac{R3}{R2};\ H_{OAP} = -\frac{R2}{R1};\ H_{OLP} = -2\ H_{OBP} = -2\left(\frac{R3}{R2}\right)$$

Figure 13. Mode 4: 2nd Order Filter Providing Allpass, Bandpass, Lowpass



$$f_o = \frac{f_{CLK}}{100(50)}\sqrt{\frac{R2}{R4}};\ Q = \frac{R3}{R2}\sqrt{\frac{R2}{R4}};\ H_{OAP} = \frac{R5}{2R};\ H_{OHP} = -\frac{R2}{R1};\ H_{OBP} = -\frac{R3}{R1};\ H_{OLP} = -\frac{R4}{R1}$$

Figure 14. Mode 4a: 2nd Order Filter Providing Highpass, Bandpass, Lowpass, Allpass

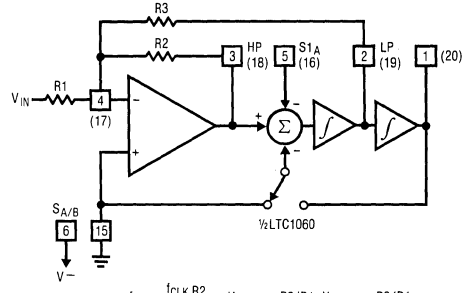


$$f_o = \frac{f_{CLK}}{100(50)}\sqrt{1+\frac{R2}{R4}};\ f_z = \frac{f_{CLK}}{100(50)}\sqrt{1-\frac{R1}{R4}};\ Q = \frac{R3}{R2}\sqrt{1+\frac{R2}{R4}}$$

$$Q_z = \frac{R3}{R1}\sqrt{1-\frac{R1}{R4}};\ H_{OZ}(f\rightarrow 0) = \frac{(R4/R1)-1}{(R4/R2)+1};\ H_{OZ}\left(f\rightarrow\frac{f_{CLK}}{2}\right) = \frac{R2}{R1};$$

$$H_{OBP} = \frac{R3}{R2}\left(1+\frac{R2}{R1}\right);\ H_{OLP} = \frac{1+(R2/R1)}{1+(R2/R4)}$$

Figure 15. Mode 5: 2nd Order Filter Providing Numerator Complex Zeros, Bandpass, Lowpass



$$f_C = \frac{f_{CLK}\,R2}{100(50)\,R3};\ H_{OLP} = -R3/R1;\ H_{OHP} = -R2/R1$$

Figure 16. Mode 6a: 1st Order Filter Providing Highpass, Lowpass

MODES OF OPERATION

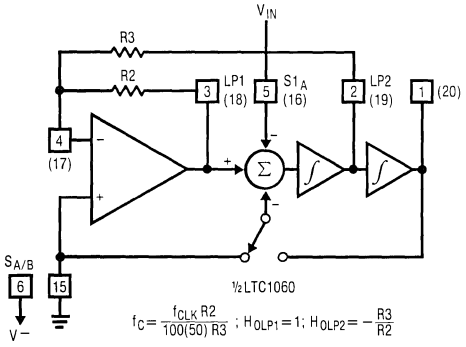


Figure 17. Mode 6b: 1st Order Filter Providing Lowpass

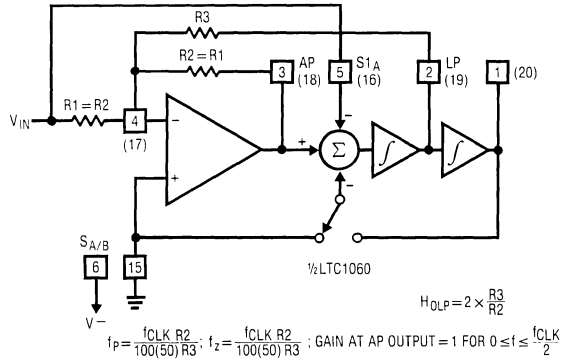


Figure 18. Mode 7: 1st Order Filter Providing Allpass, Lowpass

COMMENTS ON THE MODES OF OPERATION

There are basically three modes of operation: mode 1, mode 2, mode 3. In the mode 1, Figure 4, the input amplifier is outside the resonant loop. Because of this, mode 1 and its derivatives (mode 1a, 1b, 1c) are faster than modes 2 and 3. In mode 1, for instance, the Q errors are becoming noticeable above 1MHz clock frequency.

Mode 1a, (Figure 5), represents the most simple hook-up of the LTC1060. Mode 1a is useful when voltage gain at the bandpass output is required. The bandpass voltage gain, however, is equal to the value of Q; if this is acceptable, a second order, clock tunable, BP resonator can be achieved with only 2 resistors. The filter center frequency directly depends on the external clock frequency. For high order filters, mode 1a is not practical since it may require several clock frequencies to tune the overall filter response.

Mode 1, Figure 4, provides a clock tunable notch; the depth is shown in graph 14. Mode 1 is a practical configuration for second order clock tunable bandpass/notch filters. In mode 1, a bandpass output with a very high Q, together with unity gain, can be obtained without creating problems with the dynamics of the remaining notch and lowpass outputs.

Modes 1b and 1c, Figures 6,7 are similar. They both produce a notch with a frequency which is always equal to the filter building block center frequency. The notch and the center frequency, however, can be adjusted with an external resistor ratio.

The practical clock to center frequency ratio range is:

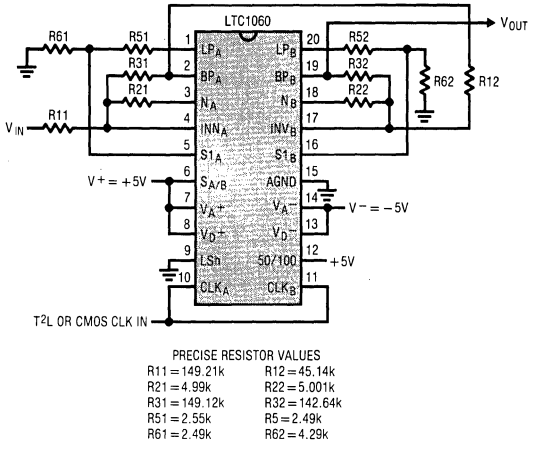
$$\frac{500}{1} \geq \frac{f_{CLK}}{f_0} \geq \frac{100}{1} \left(\text{or} \frac{50}{1}\right); \text{mode 1b}$$

$$\frac{100}{1} \text{ or} \frac{50}{1} \geq \frac{f_{CLK}}{f_0} \geq \frac{100}{\sqrt{2}} \text{ or} \frac{50}{\sqrt{2}}; \text{mode 1c}$$

The input impedance of the S1 pin is clock dependent, and in general R5 should not be larger than 5k. Mode 1b can be used to increase the clock to center frequency ratio beyond 100:1. For this mode, a practical limit for the (f_{CLK}/f_0) ratio is 500:1. Beyond this, the filter will exhibit large output offsets. Mode 1c is the fastest mode of operation: In the 50:1 mode and with (R5 = 0, R6 = ∞) the clock to center frequency ratio becomes ($50/\sqrt{2}$) and center frequencies beyond 20kHz can easily be achieved as shown in graph 25. Figure 19, illustrates how to cascade the two sections of the LTC1060 connected in mode 1c to obtain a sharp fourth order, 1dB ripple, BP Chebyshev filter. Note that the center frequency to the BW ratio for this fourth order bandpass filter is 20/1. By varying the clock frequency to sweep the filter, the center frequency of the overall filter will increase proportionally and, so will the BW to maintain the 20:1 ratio constant. All the modes of operation yield constant Q's; with any filter realization the BW's will vary when the filter is swept. This is shown in Figure 19, where the BP filter is swept from 1kHz to 20kHz center frequency.

COMMENTS ON THE MODES OF OPERATION

Modes 2, 2a, and 2b have a notch output which frequency, f_n, can be tuned independently from the center frequency, f_0. For all cases, however, $f_n < f_0$. These modes are useful when cascading second order functions to create an overall elliptic highpass, bandpass or notch response. The input amplifier and its feedback resistors (R2/R4) are now part of the resonant loop. Because of this, mode 2 and its derivatives are slower than mode 1's.



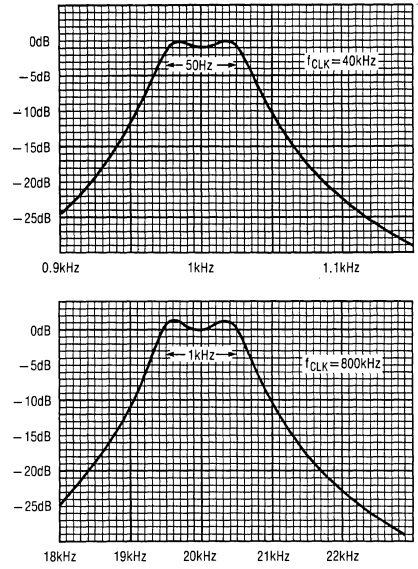
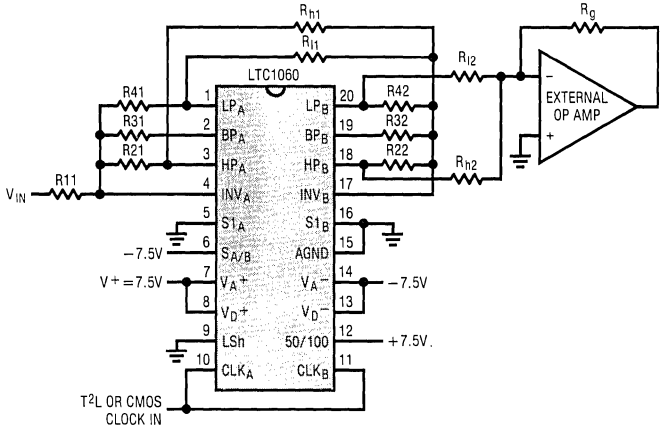


Figure 19. Cascading the 2 sections of the LTC1060 connected in mode 1c to obtain a clock tunable 4th order 1dB ripple bandpass Chebyshev filter with (center frequency) / (Ripple Bw) = 20/1.

In mode 3, Figure 11, a single resistor ratio (R2/R4) can tune the center frequency below or above the $f_{CLK}/100$ (or $f_{CLK}/50$) ratio. Mode 3 is a state variable configuration since it provides a highpass, bandpass, lowpass output through progressive integration; notches are obtained by summing the highpass and lowpass outputs (mode 3a, Figure 12). The notch frequency can be tuned below or above the center frequency through the resistor ratio (R_h/R_l). Because of this, modes 3 and 3a are the most versatile and useful modes for cascading second order sections to obtain high order elliptic filters. Figure 20, shows the 2 sections of an LTC1060 connected in mode 3a to obtain a clock tunable 4th order sharp elliptic bandpass filter. The first notch is created by summing directly the HP and LP outputs of the first section into the inverting input of the second section op amp. The individual Q's are 29.6 and the filter maintains its shape and performance up to 20kHz center frequency, Figure 21. For this circuit an external op amp is required to obtain the 2nd notch. The dynamics of Figure 24 are excellent because the amplitude response at each output pin does not exceed 0dB. The gain in the passband depends on the ratio of $(R_g/R_{h2}) \times (R22/R_{h1}) \times (R21/R11)$. Any gain value can be obtained by acting on the (R_g/R_{h2}) ratio of the external op amp, meanwhile the remaining ratios are adjusted for optimum dynamics of the LTC1060 output nodes. The external op amp of Figure 20 is not always required. In Figure 22, one section of the LTC1060 in mode 3a is cascaded with the other section in mode 2b to obtain a 4th order, 1dB ripple, elliptic bandreject filter. This configuration is interesting because a 4th order function with two different notches is realized without requiring an external op amp. The clock to center frequency ratio is adjusted to 200:1; this is done in order to better approximate a linear R,C notch filter. The amplitude response of the filter is shown in Figure 23 with up to 1MHz clock frequency. The 0dB bandwidth to the stop bandwidth ratio is 8/1. When the filter is centered at 1kHz, it should theoretically have a 44dB rejection with a 50Hz

COMMENTS ON THE MODES OF OPERATION

stop bandwidth. For a more narrow filter than the above, the unused BP output of the mode 2b section, Figure 22, has a gain exceeding unity which limits the dynamic range of the overall filter. For very selective bandpass/bandreject filters, the mode 3a approach as in Figure 12, yields better dynamic range since the external op amp helps to optimize the dynamics of the output nodes of the LTC1060.



RESISTOR VALUES

R11 = 155.93k	R21 = 5k	R31 = 152k	R41 = 5.27k
R_{h1} = 13.2k	R_{l1} = 10.74k	R22 = 5.26k	R32 = 151.8k
R42 = 5k	R_{l2} = 6.11k	R_{h2} = 5k	R_g = 37.3k

NOTE: FOR CLOCK FREQUENCIES ABOVE 700kHz A 12pF CAPACITOR ACROSS R41 AND A 20pF CAPACITOR ACROSS R42 WERE USED TO PREVENT THE PASSBAND RIPPLE FROM ANY ADDITIONAL PEAKING.

Figure 20. Combining mode 3 with mode 3a to make the 4th order BP filter of Figure 21 with improved dynamics. The gain at each output node is ≤0dB for all input frequencies.

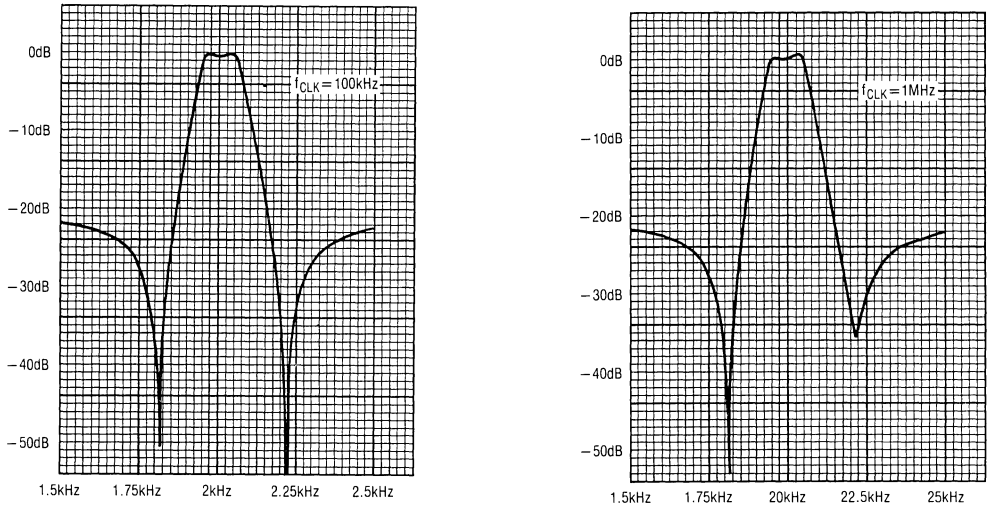


Figure 21. The BP filter of Figure 20, when swept from a 2kHz to 20kHz center frequency.

COMMENTS ON THE MODES OF OPERATION

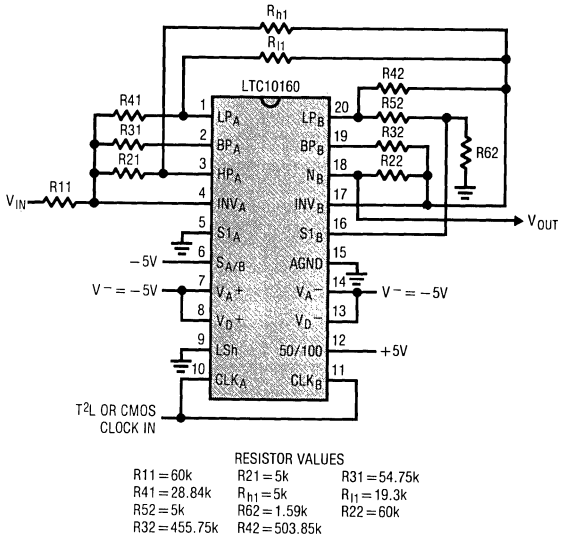


Figure 22. Combining mode 3 with mode 2b to create a 4th order BR elliptic filter with 1dB ripple and a ratio of 0dB to stop bandwidth equal to 9/1.

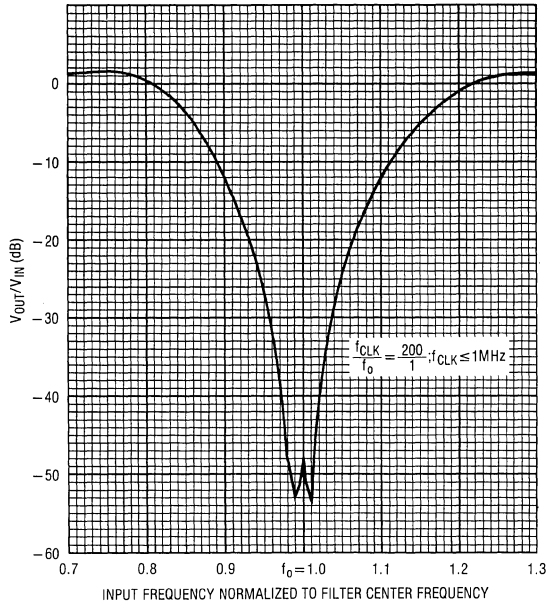


Figure 23. Amplitude Response of the notch filter of Figure 22.

LTC1060 OFFSETS

Switched capacitor integrators generally exhibit higher input offsets than discrete R,C integrators.

These offsets are mainly due to the charge injection of the CMOS switches into the integrating capacitors and they are temperature independent. The internal op amp offsets also add to the overall offset budget and they are typically a couple of millivolts.

Because of this, the DC output offsets of switched capacitor filters are usually higher than the offsets of discrete active filters.

Figure 24 shows half of an LTC1060 filter building block with its equivalent input offsets V_{OS1}, V_{OS2}, V_{OS3}. All three are 100% tested for both sides of the LTC1060. V_{OS2} is generally the larger offset. When the $S_{A/B}$, pin 6, of the LTC 1060 is shorted to the negative supply (i.e., mode 3), the value of the V_{OS2} decreases. Additionally, with $S_{A/B}$ low, a 20%-30% noise reduction is observed. Mode 1 can still be achieved, if desired, by shorting the S1 pin to the lowpass output, Figure 25.

LTC1060 OFFSETS

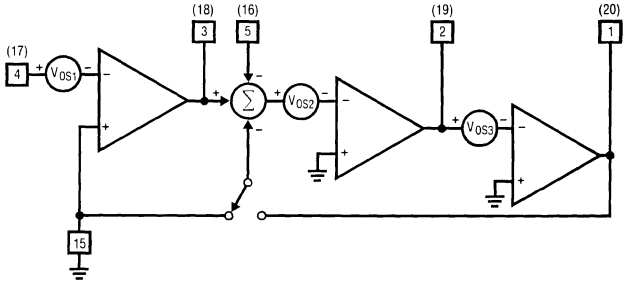


Figure 24. Equivalent Input Offsets of 1/2 LTC1060 Filter Building Block

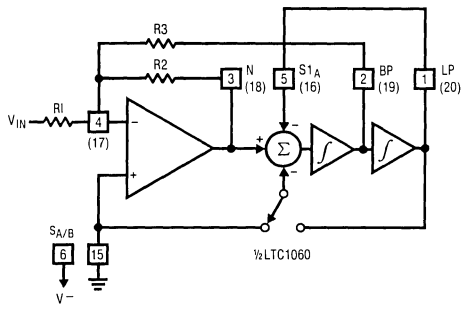


Figure 25. Mode 1(LN): Same Operation as Mode 1 but Lower V_{OS2} Offset and Lower Noise

Output Offsets

The DC offset at the filter bandpass output is always equal to V_{OS3}. The DC offsets at the remaining two outputs (Notch and LP) depend on the mode of operation and external resistor ratios. Table 5 illustrates this.

It is important to know the value of the DC output offsets, especially when the filter handles input signals with large dynamic range. As a rule of thumb, the output DC offsets increase when:

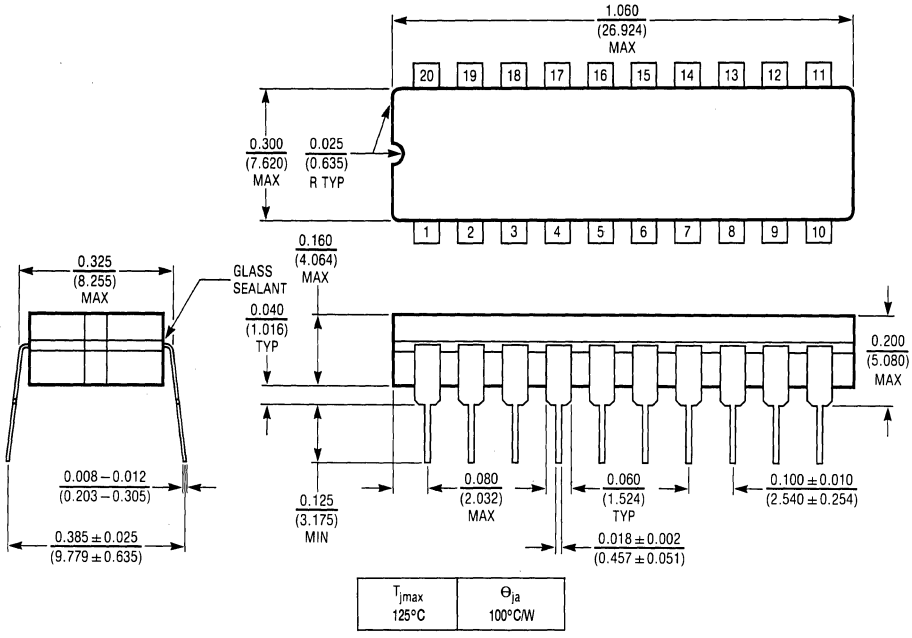
1. The Q's decrease
2. The ratio (f_{CLK}/f_o) increases beyond 100:1. This is done by decreasing either the (R2/R4) or the R6/(R5 + R6) resistor ratios.

Table 5

Mode	V_{OSN} Pin 3 (18)	V_{OSBP} Pin 2 (19)	V_{OSLP} Pin 1 (20)
1,4	$V_{OS1}[(1/Q) + 1 + \lVert H_{OLP} \rVert] - V_{OS3}/Q$	V_{OS3}	$V_{OSN} - V_{OS2}$
1a	$V_{OS1}[1 + (1/Q)] - V_{OS3}/Q$	V_{OS3}	$V_{OSN} - V_{OS2}$
1b	$V_{OS1}[(1/Q) + 1 + R2/R1] - V_{OS3}/Q$	V_{OS3}	$-(V_{OSN} - V_{OS2})(1 + R5/R6)$
1c	$V_{OS1}[(1/Q) + 1 + R2/R1] - V_{OS3}/Q$	V_{OS3}	$-(V_{OSN} - V_{OS2})\dfrac{(R5 + R6)}{(R5 + 2R6)}$
2, 5	$[V_{OS1}(1 + R2/R1 + R2/R3 + R2/R4) - V_{OS3}(R2/R3)] \times$ $\times [R4/(R2 + R4)] + V_{OS2}[R2/(R2 + R4)]$	V_{OS3}	$V_{OSN} - V_{OS2}$
2a	$[V_{OS1}(1 + R2/R1 + R2/R3 + R2/R4) - V_{OS3}(R2/R3)] \times$ $\times \left[\dfrac{R4(1+k)}{R2 + R4(1+k)}\right] + V_{OS2}\left[\dfrac{R2}{R2 + R4(1+k)}\right]; k = \dfrac{R6}{R5 + R6}$	V_{OS3}	$-(V_{OSN} - V_{OS2})\dfrac{(R5 + R6)}{(R5 + 2R6)}$
2b	$[V_{OS1}(1 + R2/R1 + R2/R3 + R2/R4) - V_{OS3}(R2/R3)] \times$ $\times \left[\dfrac{R4k}{R2 + R4k}\right] + V_{OS2}\left[\dfrac{R2}{R2 + R4k}\right]; k = \dfrac{R6}{R5 + R6}$	V_{OS3}	$-(V_{OSN} - V_{OS2})(1 + R5/R6)$
3, 4a	V_{OS2}	V_{OS3}	$V_{OS1}\left[1 + \dfrac{R4}{R1} + \dfrac{R4}{R2} + \dfrac{R4}{R3}\right] - V_{OS2}\left(\dfrac{R4}{R2}\right)$ $- V_{OS3}\left(\dfrac{R4}{R3}\right)$

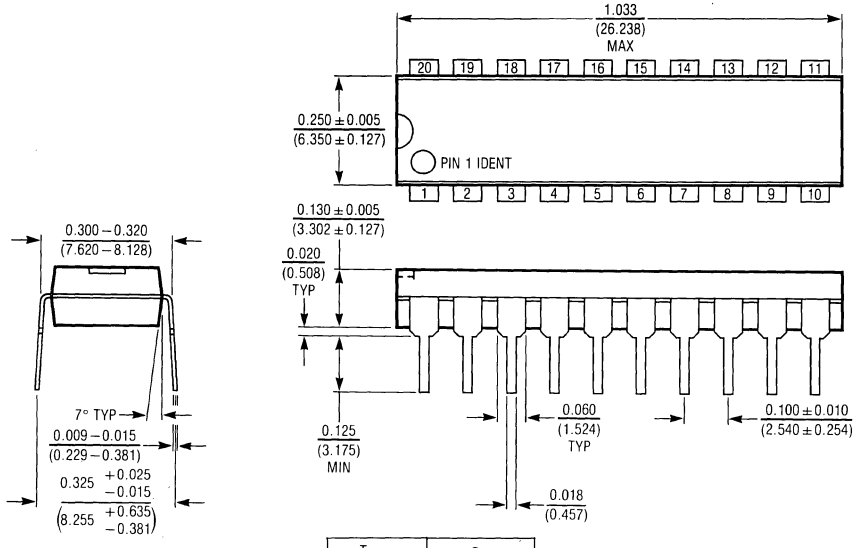
PACKAGE DESCRIPTION Dimensions in inches (millimeters) unless otherwise noted.

J Package
20 Lead CERDIP



T_{jmax}	Θ_{ja}
125°C	100°C/W

N Package
20 Lead Molded DIP



T_{jmax}	Θ_{ja}
100°C	100°C/W

FEATURES

- Lowpass Filter with No DC Error
- Low Passband Noise
- Operates DC to 20kHz
- Operates on a Single 5V Supply or Up to ±8V
- 5th Order Filter
- Maximally Flat Response
- Internal or External Clock
- Cascadable for Faster Rolloff
- Buffer Available
- 8 Pin DIP Package

APPLICATIONS

- 60Hz Lowpass Filters
- Anti-Aliasing Filter
- Low Level Filtering
- Rolling Off AC Signals from High DC Voltages
- Digital Voltmeters
- Scales
- Strain Gauges

DESCRIPTION

The LTC1062 is a 5th order all pole maximally flat lowpass filter with no DC error. Its unusual architecture puts the filter outside the DC path so DC offset and low frequency noise problems are eliminated. This makes the LTC1062 very useful for lowpass filters where DC accuracy is important.

The filter input and output are simultaneously taken across an external resistor. The LTC1062 is coupled to the signal through an external capacitor. This R,C reacts with the internal switched capacitor network to form a 5th order rolloff at the output.

The filter cutoff frequency is set by an internal clock which can be externally driven. The clock to cutoff frequency ratio is typically 100:1, allowing the clock ripple to be easily removed.

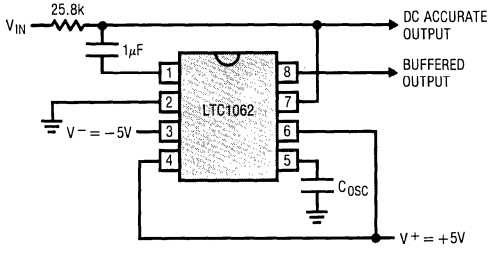
Two LTC1062s can be cascaded to form a 10th order quasi max flat lowpass filter. The device can be operated with single or dual supplies ranging from ±2.5V to ±9V.

The LTC1062 is manufactured using Linear Technology's enhanced LTCMOS™ silicon gate process.

LTCMOS™ is a trademark of Linear Technology Corp.

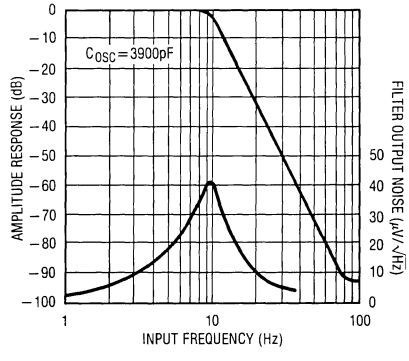
TYPICAL APPLICATION

10Hz 5th Order Butterworth Lowpass Filter



NOTE: TO ADJUST OSCILLATOR FREQUENCY, USE A 6800pF CAPACITOR IN SERIES WITH A 50K POT FROM PIN 5 TO GROUND.

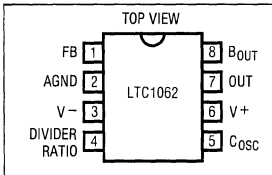
Filter Amplitude Response and Noise



ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage (V^+ to V^-) 18V
Input Voltage at Any Pin ..... $V^- - 0.3V \leq V_{IN} \leq V^+ + 0.3V$
Operating Temperature Range
LTC1062M..... $-55°C \leq T_A \leq 125°C$
LTC1062C ..... $-40°C \leq T_A \leq 85°C$
Storage Temperature Range..... $-65°C$ to $150°C$
Lead Temperature Range (Soldering, 10 sec.)..... 300°C

PACKAGE/ORDER INFORMATION



J8 PACKAGE HERMETIC DIP
N8 PACKAGE PLASTIC DIP

ORDER PART NUMBER
LTC1062MJ8 LTC1062CJ8 LTC1062CN8

ELECTRICAL CHARACTERISTICS

Test Conditions: $V^+ = +5V$, $V^- = -5V$, $T_A = 25°C$ unless otherwise specified, AC output measured at pin 7, Figure 1

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Power Supply Current	C_{OSC} (Pin 5 to V^-) = 100 pF			4.5	7	mA
		●			10	mA
Input Frequency Range				0-20k		Hz
Filter Gain at $f_{IN} = 0$	f_{CLK} = 100kHz, Pin 4 at V^+			0		dB
$f_{IN} = 0.5f_C$ (Note 1)	C = 0.01μF, R = 25.78k			−0.02	−0.3	dB
$f_{IN} = f_C$		●	−2	−3		dB
$f_{IN} = 2f_C$		●	−28	−30		dB
$f_{IN} = 4f_C$		●	−54	−60		dB
Clock to Cutoff Frequency Ratio, f_{CLK}/f_C	Same as above			100 ± 1		%
Filter Gain at f_{IN} = 16kHz	f_{CLK} = 400kHz, Pin 4 at V^+ C = 0.01μF, R = 6.5k	●	−48	−52		dB
f_{CLK}/f_C Tempco	Same as above			10		ppm/°C
Filter Output (Pin 7) DC Swing	Pin 7 bufffered with an external op amp	●	±3.5	±3.8		V
Clock Feedthrough				10		mVp-p
Internal Buffer						
Bias Current				2	50	pA
Bias Current		●		170	1000	pA
Offset Voltage				2	20	mV
Voltage Swing	R1 = 20kΩ	●	±3.5	±3.8		V
Short Circuit Current Source/Sink				40/3		mA
Clock (Note 3)						
Internal Oscillator Frequency	C_{OSC} (Pin 5 to V^-) = 100pF		25	32	50	kHz
	C_{OSC} (Pin 5 to V^-) = 100pF	●	15		65	kHz
Max Clock Frequency				4		MHz
Pin 5 Source or Sink Current		●		40	80	μA

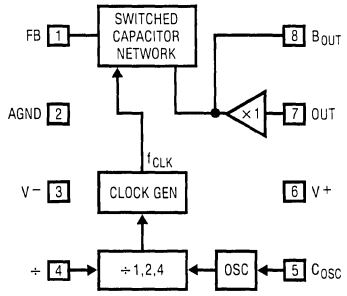
The ● denotes the specifications which apply over the full operating temperature range.

Note 1: f_C is the frequency where the gain is −3dB with respect to the input signal.

Note 2: The LTC1062M operates from $-55°C \leq T_A \leq 125°C$, the LTC1062C operates from $-40°C \leq T_A \leq 85°C$.

Note 3: The external or driven clock frequency is divided by either 1, 2, or 4 depending upon the voltage at pin 4. When pin 4 = V^+, ratio = 1; when pin 4 = GND, ratio = 2; when pin 4 = V^-, ratio = 4.

BLOCK DIAGRAM



BY CONNECTING PIN 4 TO V+, AGND, OR V–, THE OUTPUT FREQUENCY OF THE INTERNAL CLOCK GENERATOR IS THE OSCILLATOR FREQUENCY DIVIDED BY 1,2,4. THE (f_{CLK}/f_C) RATIO OF 100:1 IS WITH RESPECT TO THE INTERNAL CLOCK GENERATOR OUTPUT FREQUENCY. PIN 5 CAN BE DRIVEN WITH AN EXTERNAL CMOS LEVEL CLOCK. THE LTC1062 CAN ALSO BE SELF-CLOCKED BY CONNECTING AN EXTERNAL CAPACITOR (C_{OSC}) TO GROUND (OR TO V– IF C_{OSC} IS POLARIZED). UNDER THIS CONDITION AND WITH ±5V SUPPLIES, THE INTERNAL OSCILLATOR FREQUENCY IS:

$f_{OSC} \simeq 140kHz\ [33pF/(33pF + C_{OSC})]$.

For Adjusting Oscillator Frequency, Insert a 50K Pot in Series with C_{OSC}. Use Two Times Calculated C_{OSC}.

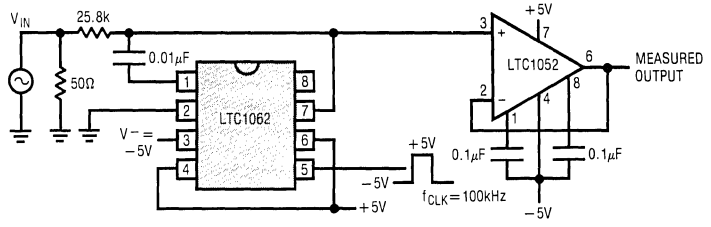
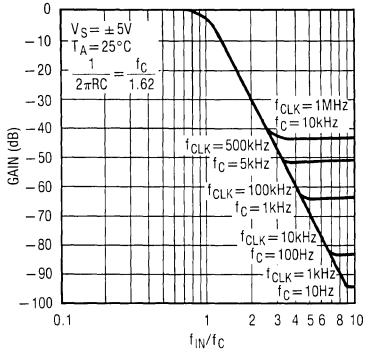


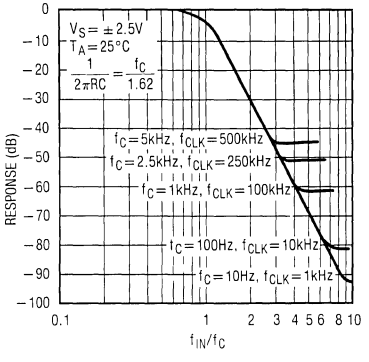
Figure 1. AC Test Circuit

TYPICAL PERFORMANCE CHARACTERISTICS

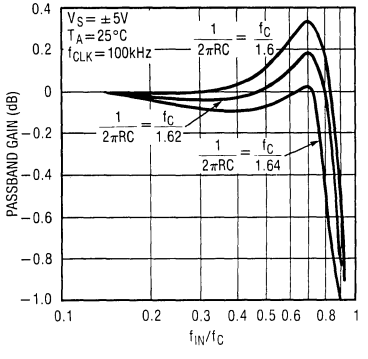
Amplitude Response Normalized to the Cutoff Frequency



Amplitude Response Normalized to the Cutoff Frequency

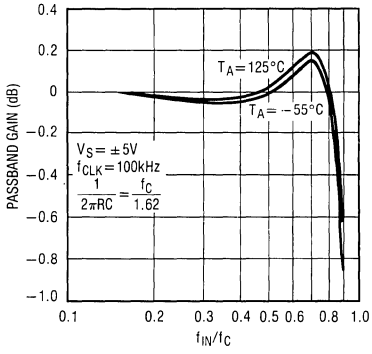


Passband Gain vs Input Frequency

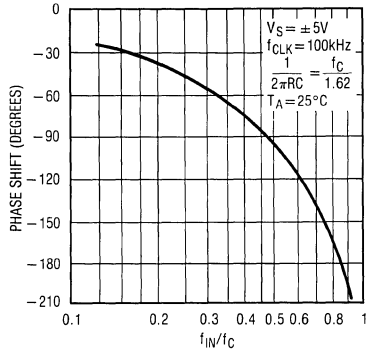


TYPICAL PERFORMANCE CHARACTERISTICS

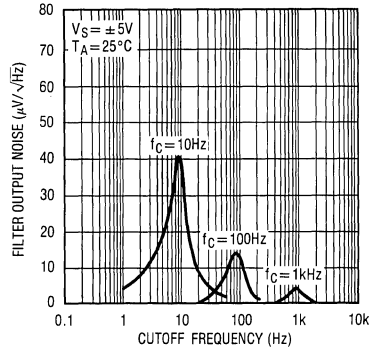
Passband Gain vs Input Frequency



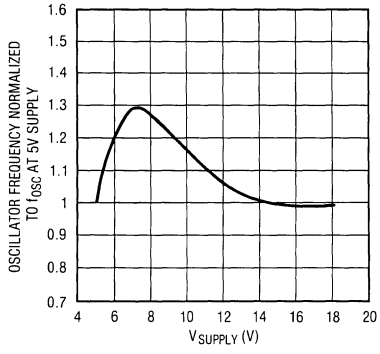
Passband Phase Shift vs Input Frequency



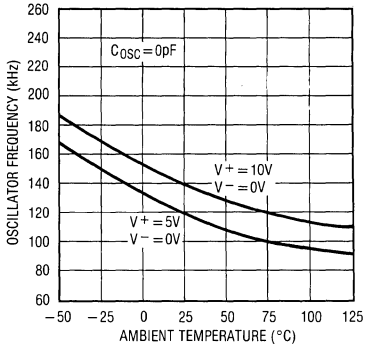
Filter Noise Spectral Density



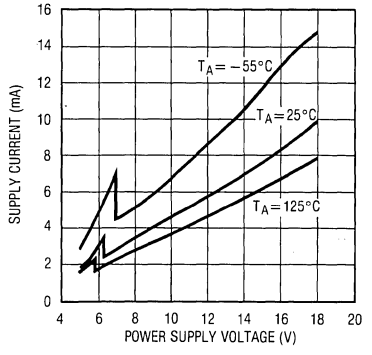
Normalized Oscillator Frequency, f_{OSC} vs Supply Voltage



Oscillator Frequency, f_{OSC} vs Ambient Temperature



Power Supply Current vs Power Supply Voltage



APPLICATIONS INFORMATION

Filter Input Voltage Range

Every node of the LTC1062 typically swings within 1V of either voltage supply, positive or negative. With the appropriate external (R,C) values, the amplitude response of all the internal or external nodes does not exceed a gain of 0 dB with the exception of pin 1. The amplitude response of the feedback node (pin 1) is shown in Figure 2. For an input frequency around 0.8 x f_C, the gain is 1.7 V/V and, with ±5V supplies, the peak-to-peak input voltage should not exceed 4.7V. If the input voltage goes beyond this value, clipping and distortion of the output waveform occur, but the filter will not get damaged nor will it oscillate. Also, the absolute maximum input voltage should not exceed the power supplies.

APPLICATIONS INFORMATION

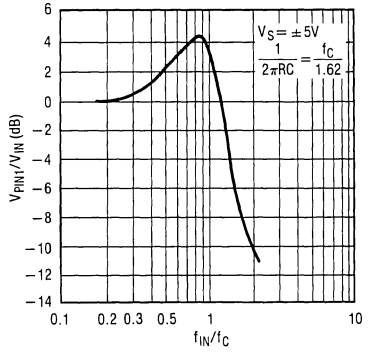


Figure 2. Amplitude Response of Pin 1

Internal Buffer

The internal buffer out (pin 8) and pin 1 are part of the signal AC path. Excessive capacitive loading will cause gain errors in the passband, especially around the cutoff frequency. The internal buffer gain at DC is typically 0.006dB. The internal buffer output can be used as a filter output, however it has a few millivolts of DC offset. The temperature coefficient of the internal buffer is typically 1μV/°C.

Filter Attenuation

The LTC1062 rolloff is typically 30dB/octave. When the clock, and the cutoff frequencies increase, the filter's maximum attenuation decreases. This is shown in the Typical Performance Characteristics. The decrease of the maximum attenuation, is due to the roll off at higher frequencies of the loop gains of the various internal feedback paths and not to the increase of the noise floor. For instance, for a 100kHz clock and 1kHz cutoff frequency, the maximum attenuation is about 64dB. A 4kHz, 1Vrms input signal will be predictably attenuated by 60dB at the output. A 6kHz, 1Vrms input signal will be attenuated by 64dB and not by 77dB as an ideal 5th order maximum flat filter would have dictated. The LTC1062 output at 6kHz will be about 630μVrms. The measured rms noise from DC to 17kHz was 100μVrms which is 16dB below the filter output.

C_{OSC}, Pin 5

The C_{OSC}, pin 5, can be used with an external capacitor, C_{OSC}, connected from pin 5 to ground. If C_{OSC} is polarized it should be connected from pin 5 to the negative supply, pin 3. C_{OSC} lowers the internal oscillator frequency. If pin 5 is floating, an internal 33pF capacitor plus the external interpin capacitance set the oscillator frequency around 140kHz with ±5V supply. An external C_{OSC} will bring the oscillator frequency down by the ratio (33pF)/(33pF + C_{OSC}). The typical performance characteristics curves provide the necessary information to get the internal oscillator frequency for various power supply ranges. Pin 5 can also be driven with an external CMOS clock to override the internal oscillator. Although standard 7400 series CMOS gates do not guarantee CMOS levels with the current source and sink requirements of pin 5, they will, in reality, drive the C_{OSC} pin. CMOS gates conforming to standard B series output drive have the appropriate voltage levels and more than enough output current to simultaneously drive several LTC1062 C_{OSC} pins. The typical trip levels of the internal Schmitt trigger which input is pin 5, are given below.

POWER SUPPLY		TRIP LEVELS	
$V^+ = +5V$	$V^- = 0V$	$V_H = 3.4V$	$V_L = 1.35V$
$V^+ = +10V$	$V^- = 0V$	$V_H = 6.5V$	$V_L = 2.8V$
$V^+ = +15V$	$V^- = 0V$	$V_H = 9.5V$	$V_L = 4.1V$

APPLICATIONS INFORMATION

Divide By 1, 2, 4 (Pin 4)

By connecting pin 4 to V^+, to mid supplies or to V^-, the clock frequency driving the internal switched capacitor network is the oscillator frequency divided by 1, 2, 4, respectively. Note that the f_{CLK}/f_C ratio of 100:1 is with respect to the internal clock generator output frequency. The internal divider is useful for applications where octave tuning is required. The ÷2 threshold is typically ±1V from the mid supply voltage.

Transient Response

Figure 3 shows the LTC1062 response to a 1V input step. The settling time approximates that of an ideal 5th order maximally flat filter.

Filter Noise

The filter wideband rms noise is typically 100μVrms for ±5V supply and it is nearly independent from the value of the cutoff frequency. For single 5V supply the rms noise is 80μVrms. Sixty-two percent of the wideband noise is in the passband, that is from DC to f_C. The noise spectral density, unlike conventional active filters, is nearly zero for frequencies below $0.1 \times f_C$. This is shown in the typical performance characteristics section. Table 1 shows the LTC1062 rms noise for different noise bandwidths.

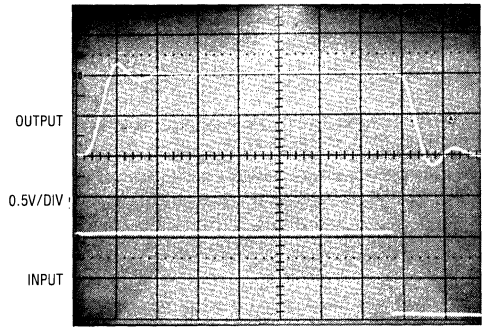


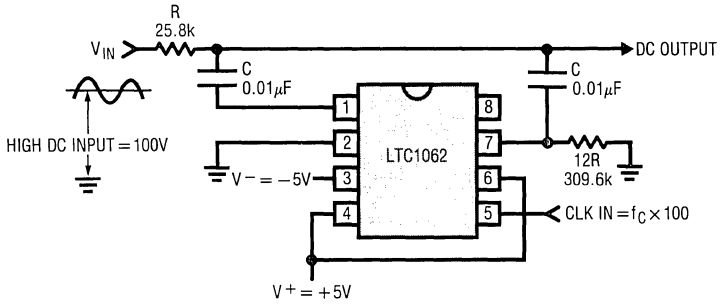
Figure 3. LTC1062 Transient Response

Table 1

NOISE BW	rms NOISE $V_S = \pm 5V$
DC – $0.1 \times f_C$	2μV
DC – $0.25 \times f_C$	8μV
DC – $0.5 \times f_C$	20μV
DC – $1 \times f_C$	62μV
DC – $2 \times f_C$	100μV

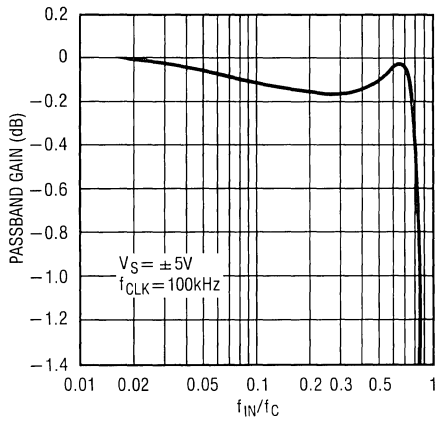
TYPICAL APPLICATIONS

Filtering AC Signals from High DC Voltages



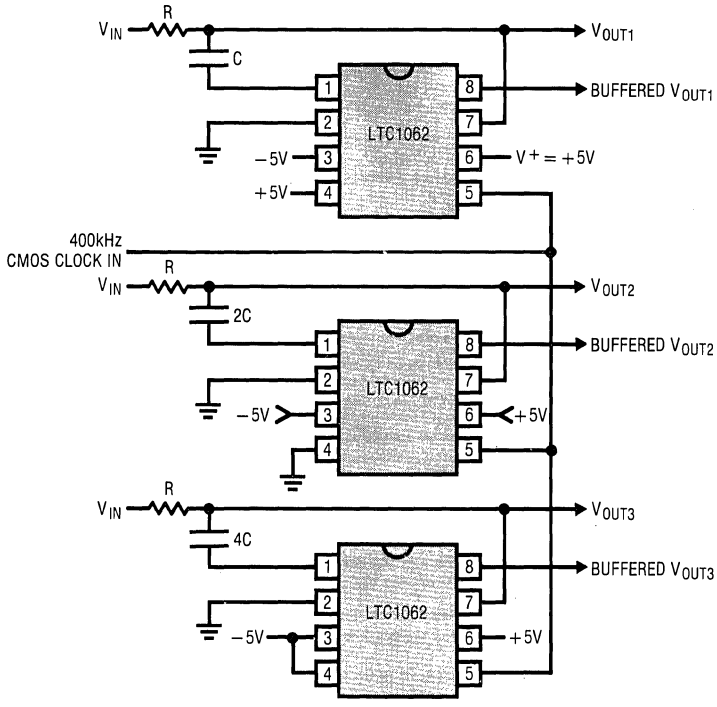
EX f_{CLK} = 100kHz, f_C = 1kHz. THE FILTER ACCURATELY PASSES THE HIGH DC INPUT AND ACTS AS 5th ORDER LP FILTER FOR THE AC SIGNALS RIDING ON THE DC. THE AMPLITUDE RESPONSE IN THE PASSBAND IS SHOWN BELOW.

Passband Amplitude Response for the High DC Accurate 5th Order Filter

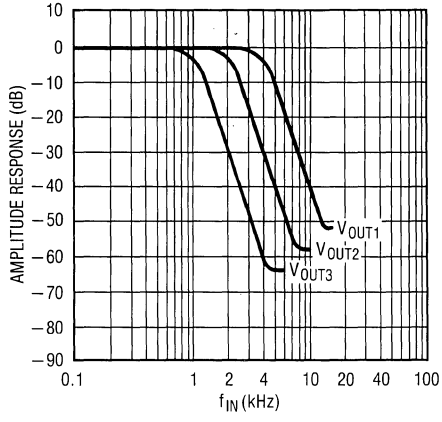


TYPICAL APPLICATIONS

Octave Tuning with a Single Input Clock

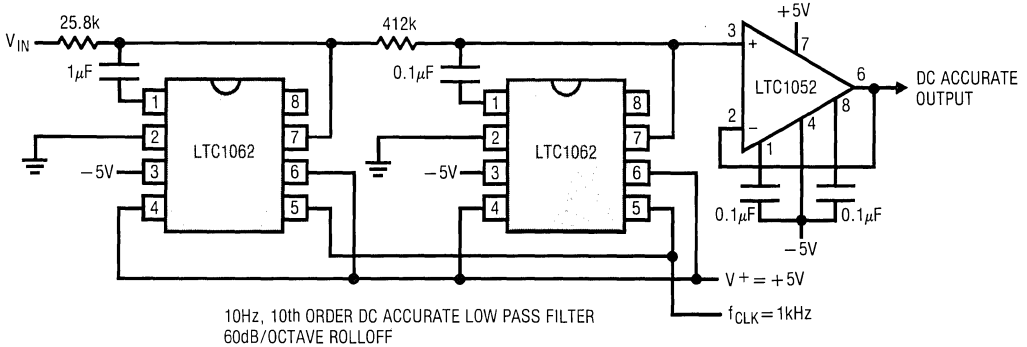


Amplitude Response for the Octave Tuning Circuit



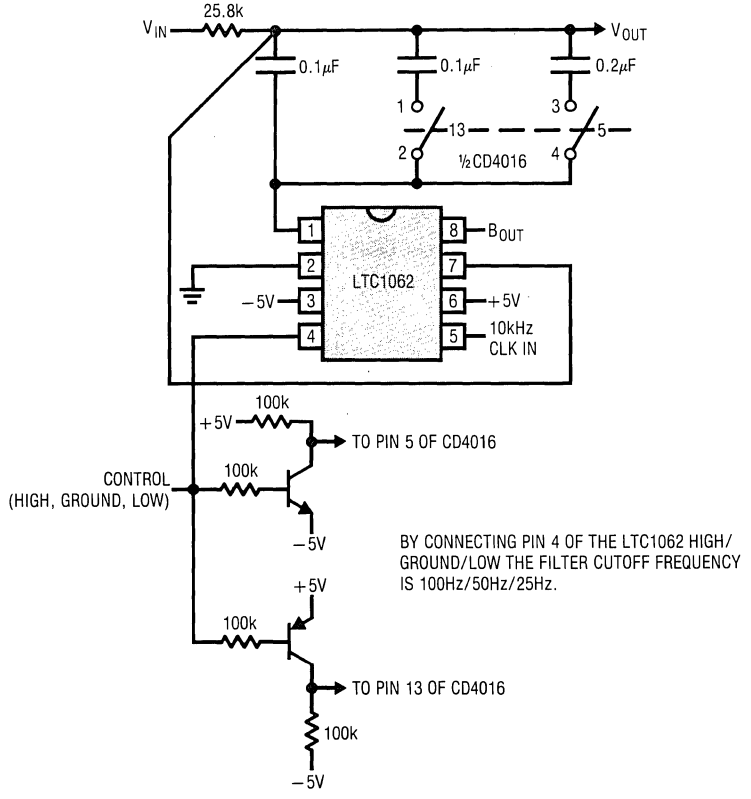
TYPICAL APPLICATIONS

Simple Cascading Technique



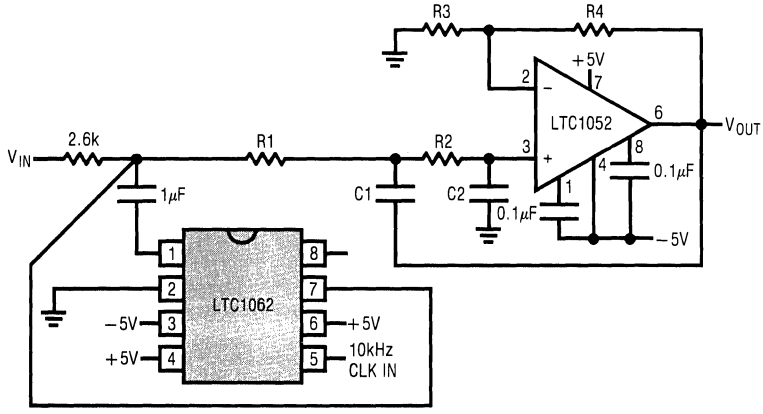
10Hz, 10th ORDER DC ACCURATE LOW PASS FILTER
60dB/OCTAVE ROLLOFF
0.5dB PASSBAND ERROR, 0dB DC GAIN
MAXIMUM ATTENUATION 110dB (f_{CLK} = 10kHz)
100dB (f_{CLK} = 1kHz)
95dB (f_{CLK} = 1MHz)

100Hz, 50Hz, 25Hz 5th Order DC Accurate LP Filter



TYPICAL APPLICATIONS

7th Order 100Hz Lowpass Filter with Continuous Output Filtering, Output Buffering and Gain Adjustment



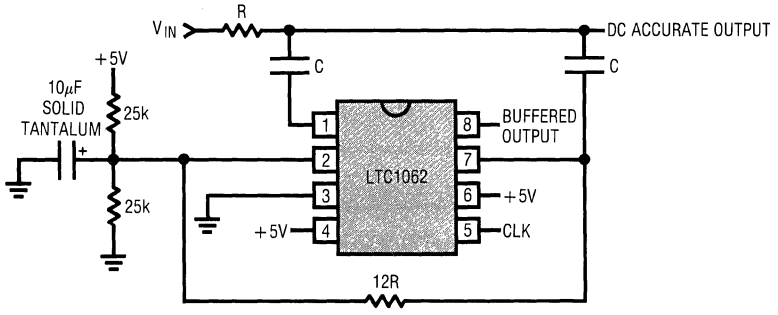
THE LTC1052 IS CONNECTED AS A 2nd ORDER SALLEN AND KEY LOWPASS FILTER WITH A CUTOFF FREQUENCY EQUAL TO THE LTC1062. THE ADDITIONAL FILTERING ELIMINATES ANY 10kHz CLOCK FEED THROUGH PLUS DECREASES THE WIDEBAND NOISE OF THE FILTER.

DC OUTPUT OFFSET (REFERRED TO A DC GAIN OF UNITY) = 5μV MAX.

WIDEBAND NOISE (REFERRED TO A DC GAIN OF UNITY) ≈ 60μVrms

OUTPUT FILTER COMPONENT VALUES						
DC GAIN	R3	R4	R1	R2	C1	C2
1	∞	0	14.3k	53.6k	0.1μF	0.033μF
10	3.57k	32.4k	4.6k	27.4	0.1μF	0.2μF
101	0.324	32.4k	0.31k	16.9k	0.47μF	1μF

Single 5V Supply 5th Order LP Filter



FOR A 10Hz FILTER R = 29.4k, C = 1μF, f_{CLK} = 1kHz

THE FILTER IS MAXIMALLY FLAT FOR $\frac{1}{2\pi RC} = \frac{f_C}{1.84}$

TYPICAL APPLICATIONS

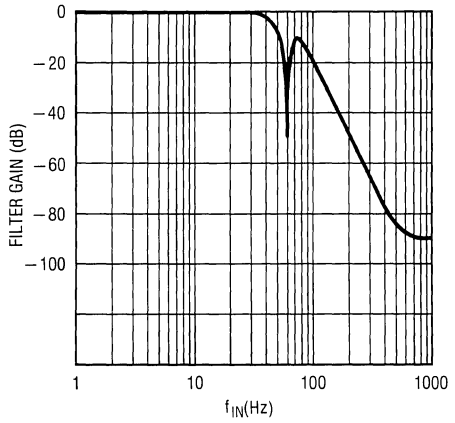
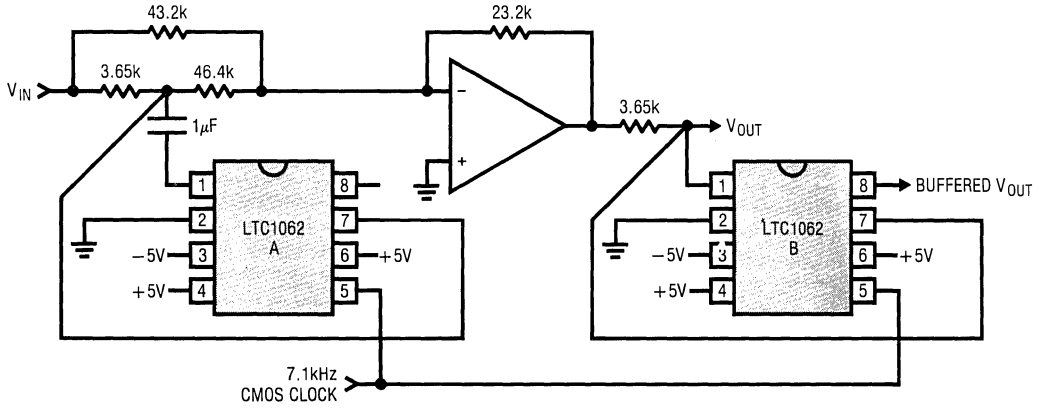


Figure 4

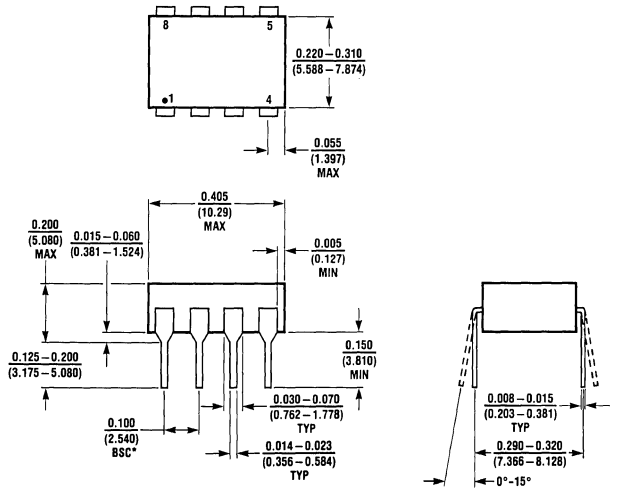
5th Order Lowpass Filter with a 60Hz Notch



OUTPUT DC OFFSET IS 2 TIMES THE EXTERNAL OP AMP OFFSET VOLTAGE. THE LTC1062(A) FORMS A NOTCH WITH $f_{CLK}/f_{NOTCH} \simeq 118.3$ AMPLITUDE RESPONSE IS SHOWN IN FIGURE 4.

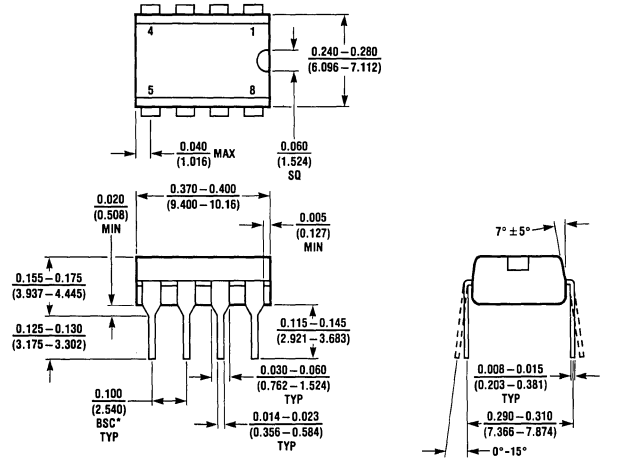
PACKAGE DESCRIPTION Dimensions in inches (millimeters) unless otherwise noted.

J8 Package
8 Lead Hermetic DIP



T_{jmax}	Θ_{ja}
150°C	100°C/W

N8 Package
8 Lead Plastic



T_{jmax}	Θ_{ja}
100°C	130°C/W

SECTION 7—PULSE WIDTH MODULATORS

SECTION 7—PULSE WIDTH MODULATORS

Regulating Pulse Width Modulator

FEATURES

- *Guaranteed* ±2% Reference Tolerance
- *Guaranteed* ±6% Oscillator Tolerance
- *Guaranteed* 10mV/1000 Hrs Long Term Stability
- Interchangeable with all SG1524 or LM1524 Devices
- Operates Above 100kHz

APPLICATIONS

- Switching Power Supplies
- Motor Speed Control
- Off-Line Power Converters

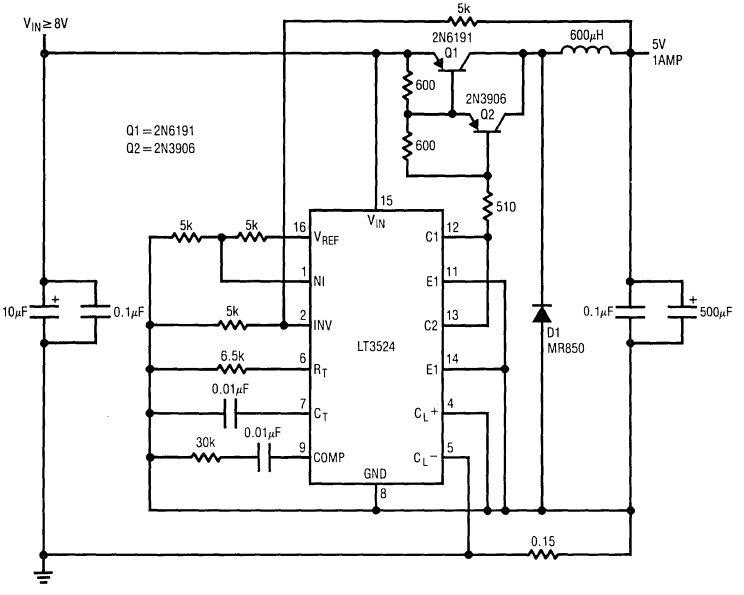
DESCRIPTION

The LT1524 PWM switching regulator control circuit contains all the essential circuitry to implement single-ended or push-pull switching regulators. Included on the circuit are oscillator, voltage reference, a pulse width modulator, error amplifier, overload protection circuitry and output drivers.

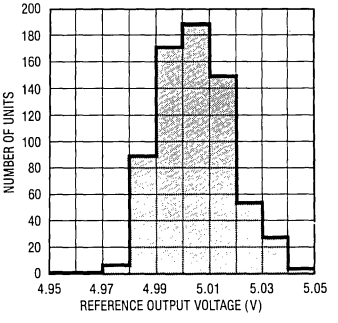
Although pin-for-pin and functionally compatible with industry standard 1524 and 3524 devices, Linear Technology has incorporated several improvements in the design of the LT1524. A subsurface zener reference has been used to provide excellent stability with time and the reference is trimmed at the wafer level to provide an initial accuracy of 2%. Additionally, the oscillator is trimmed to provide a maximum tolerance of 6%.

Linear Technology Corporation's advanced processing, design and passivation techniques make the LT1524 and LT3524 a superior and more reliable choice over previous devices.

5V, 1 Amp Regulator



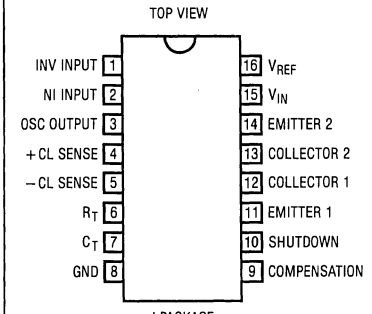
Distribution of Reference Output Voltage



ABSOLUTE MAXIMUM RATINGS

Input Voltage 40V
Reference Output Current 50mA
Output Current (Each Output) 100mA
Oscillator Charging Current (Pin 6 or 7) 5mA
Internal Power Dissipation (Note 1) 1W
Operating Temperature Range
LT1524/SG1524 ..... −55°C to +125°C
LT3524/SG3524 ..... 0°C to +70°C
Storage Temperature Range ..... −65°C to +150°C
Lead Temperature (Soldering, 10 sec.) ..... 300°C

PACKAGE/ORDER INFORMATION



J PACKAGE
16 PIN HERMETIC

N PACKAGE
16 PIN PLASTIC

ORDER PART NUMBER
LT1524J
LT3524J
LT3524N
SG1524J
SG3524J
SG3524N

ELECTRICAL CHARACTERISTICS (Note 2)

PARAMETER	CONDITIONS		LT1524 MIN	LT1524 TYP	LT1524 MAX	SG1524 MIN	SG1524 TYP	SG1524 MAX	UNITS
Reference Section:									
Output Voltage		●	4.9	5.0	5.1	4.8	5.0	5.2	V
Line Regulation	V_{IN} = 8V to 40V	●		2	10		10	20	mV
Load Regulation	I_L = 0mA to 20mA	●		10	20		20	50	mV
Ripple Rejection	f = 120Hz			80			66		dB
Short Circuit Current Limit	V_{REF} = 0			100			100		mA
Temperature Stability		●		0.3	1		0.3	1	%
Long Term Stability	T_J = 125°C			2	10		20		mV/$\sqrt{khr}$
Oscillator Section:									
Maximum Frequency	C_T = 0.001μF, R_T = 2kΩ	●		300			300		kHz
Initial Accuracy	R_T and C_T Constant			3	6		5		%
Voltage Stability	V_{IN} = 8V to 40V				1			1	%
Temperature Stability	Note 3	●		2			2		%
Output Amplitude	Pin 3			3.5			3.5		V
Output Pulse Width	C_T = 0.01μF, T_A = 25°C			0.5			0.5		μs
Error Amplifier Section:									
Input Offset Voltage	V_{CM} = 2.5V	●		0.5	5		0.5	5	mV
Input Bias Current	V_{CM} = 2.5V	●		0.5	2		2	10	μA
Open Loop Voltage Gain		●	72	80		72	80		dB
Common-Mode Voltage			1.8		3.4	1.8		3.4	V
Common-Mode Rejection Ratio			70	86			70		dB
Small Signal Bandwidth	A_V = 0dB			3			3		MHz
Output Voltage			0.5		3.8	0.5		3.8	V

ELECTRICAL CHARACTERISTICS

PARAMETER	CONDITIONS		LT1524 MIN	LT1524 TYP	LT1524 MAX	SG1524 MIN	SG1524 TYP	SG1524 MAX	UNITS
Comparator Section:									
Duty Cycle (Max)	% Each Output On	●	45		45	45		45	%
Input Threshold	Zero Duty Cycle	●		1			1		V
Input Threshold	Max Duty Cycle	●		3.5			3.5		V
Input Bias Current		●		0.2	2		1		μA
Current Limiting Section:									
Sense Voltage	Pin 9 = 2V with Error Amplifier Set for Max Out		190	200	210	190	200	210	mV
Sense Voltage T.C.		●		0.2			0.2		mV/°C
Common-Mode Voltage		●	−0.7		1	−0.7		1	V
Output Section: (Each Output)									
Collector-Emitter Voltage		●	40			40			V
Collector Leakage Current	V_{CE} = 40V	●		0.1	50		0.1	50	μA
Saturation Voltage	I_C = 50mA	●		1	2		1	2	V
Emitter Output Voltage	V_{IN} = 20V	●	17	18		17	18		V
Rise Time	R_C = 2kΩ			0.2			0.2		μs
Fall Time	R_C = 2kΩ			0.1			0.1		μs
Total Standby Current:	V_{IN} = 40V (Note 4)	●		8	10		8	10	mA

ELECTRICAL CHARACTERISTICS (Note 2)

PARAMETER	CONDITIONS		LT3524 MIN	LT3524 TYP	LT3524 MAX	SG3524 MIN	SG3524 TYP	SG3524 MAX	UNITS
Reference Section:									
Output Voltage		●	4.9	5.0	5.1	4.6	5.0	5.4	V
Line Regulation	V_{IN} = 8V to 40V	●		3	10		10	30	mV
Load Regulation	I_L = 0mA to 20mA	●		10	20		20	50	mV
Ripple Rejection	f = 120Hz			80			66		dB
Short Circuit Current Limit	V_{REF} = 0			100			100		mA
Temperature Stability		●		0.3	1		0.3	1	%
Long Term Stability				2	10		20		mV/khr
Oscillator Section:									
Maximum Frequency	C_T = 0.001mfd, R_T = 2kΩ	●		300			300		kHz
Initial Accuracy	R_T and C_T Constant			3	6		5		%
Voltage Stability	V_{IN} = 8V to 40V				1			1	%
Temperature Stability	Note 3	●		2			2		%
Output Amplitude	Pin 3			3.5			3.5		V
Output Pulse Width	C_T = 0.01μF, T_A = 25°C			0.5			0.5		μs
Error Amplifier Section:									
Input Offset Voltage	V_{CM} = 2.5V	●		1	5		2	10	mV
Input Bias Current	V_{CM} = 2.5V	●		0.5	2		2	10	μA
Open Loop Voltage Gain		●	72	80		60	80		dB
Common-Mode Voltage			1.8		3.4	1.8		3.4	V
Common-Mode Rejection Ratio			70	86			70		dB
Small Signal Bandwidth	A_V = 0dB			3			3		MHz
Output Voltage			0.5		3.8	0.5		3.8	V

ELECTRICAL CHARACTERISTICS

PARAMETER	CONDITIONS		LT3524 MIN	LT3524 TYP	LT3524 MAX	SG3524 MIN	SG3524 TYP	SG3524 MAX	UNITS
Comparator Section:									
Duty Cycle	% Each Output On	●	0		45	0		45	%
Input Threshold	Zero Duty Cycle	●		1			1		V
Input Threshold	Max Duty Cycle	●		3.5			3.5		V
Input Bias Current		●		1	2		1		μA
Current Limiting Section:									
Sense Voltage	Pin 9 = 2V with Error Amplifier Set for Max Out		190	200	210	180	200	220	mV
Sense Voltage T.C.		●		0.2			0.2		mV/°C
Common-Mode Voltage		●	−1		1	−1		1	V
Output Section: (Each Output)									
Collector-Emitter Voltage		●	40			40			V
Collector Leakage Current	V_{CE} = 40V	●		0.1	50		0.1	50	μA
Saturation Voltage	I_C = 50mA	●		1	2		1	2	V
Emitter Output Voltage	V_{IN} = 20V	●	17	18		17	18		V
Rise Time	R_C = 2kΩ			0.2			0.2		μs
Fall Time	R_C = 2kΩ			0.1			0.1		μs
Total Standby Current:	V_{IN} = 40V (Note 4)	●		8	10		8	10	mA

The ● denotes specifications that apply over the full operating temperature range.

The shaded electrical specifications indicate those parameters which have been improved or guaranteed test limits provided for the first time.

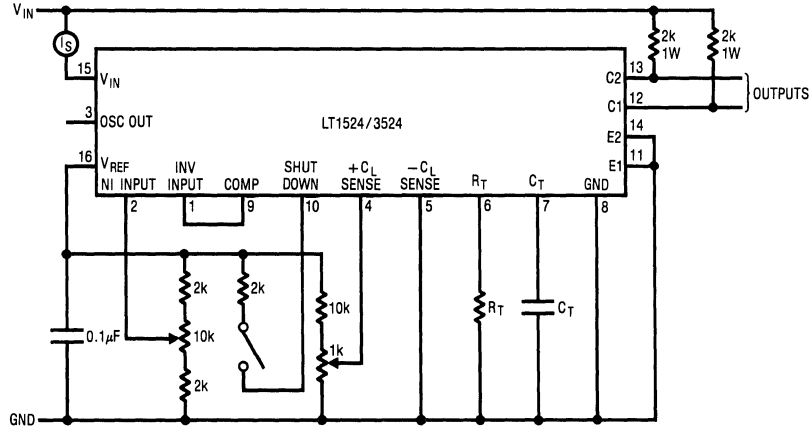
Note 1: For operating at elevated temperatures, the device in the J package must be derated at 100°C/W to a maximum junction temperature of 150°C, while the device in the N package is derated at 150°C/W to a maximum junction temperature of 115°C.

Note 2: These specifications apply for V_{IN} = 20V, f = 20kHz. T_A = 25°C unless otherwise noted.

Note 3: Although many manufacturers specify a maximum specification of 2%, Linear Technology's experience is that this specification is not being presently met by other manufacturers. Linear Technology's basic design, although improved, is essentially identical to other manufacturers' devices. Linear Technology is, however, unwilling to place a maximum specification on its data sheet which cannot be met or guaranteed.

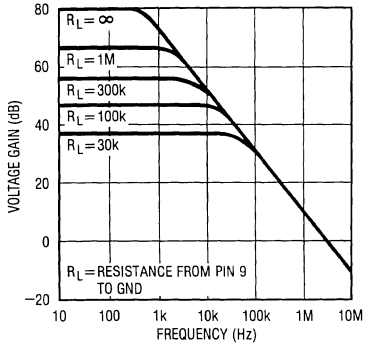
Note 4: Standby current does not include the oscillator charging current, error and current limit dividers, and the outputs are open circuit.

TEST CIRCUIT

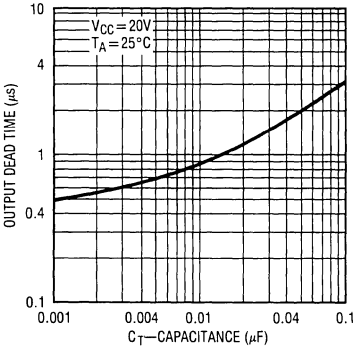


TYPICAL PERFORMANCE CHARACTERISTICS

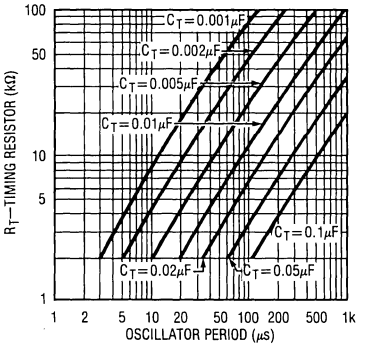
Error Amplifier Gain



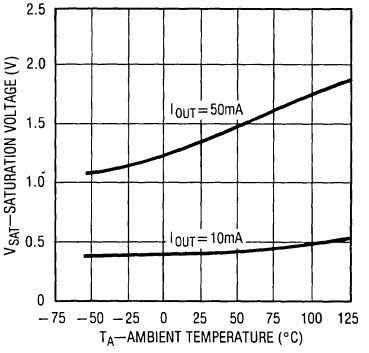
Output Dead Time



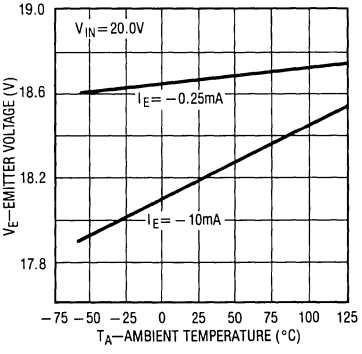
Oscillator Period



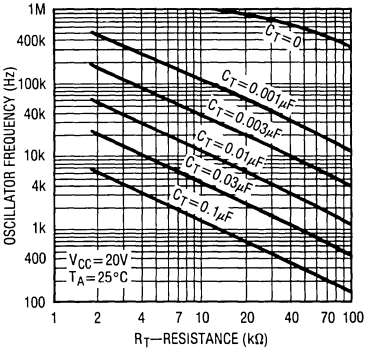
Output Transistor Saturation Voltage



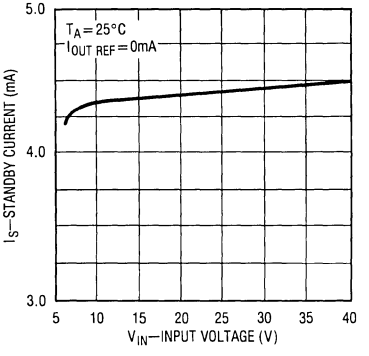
Output Transistor Emitter Voltage



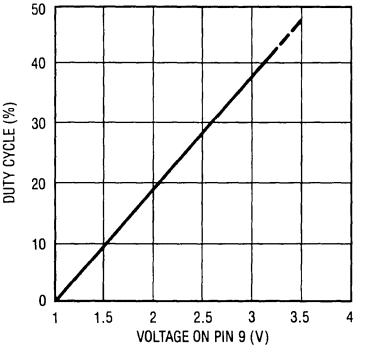
Oscillator Frequency vs Timing Resistance



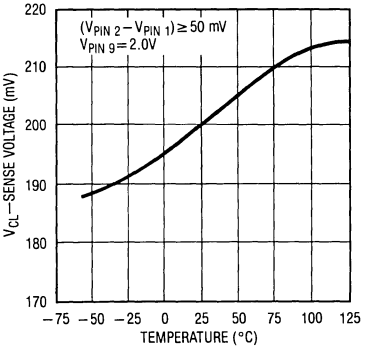
Standby Current



Duty Cycle



Current Limit Sense Voltage ($V_{PIN\ 4} - V_{PIN\ 5}$)



APPLICATIONS INFORMATION

FUNCTIONAL DESCRIPTION AND PIN FUNCTIONS

Voltage Regulator

The internal 5V regulator (input pin 15, output pin 16) supplies a regulated 5V to all internal circuitry, as well as up to 50mA for external circuitry. For operation below 8V input, pins 15 and 16 may be tied together and 5V to 6V externally applied.

Oscillator

The internal oscillator circuitry sets the frequency of operation for the switching regulator. The oscillator waveform is a ramp from about 1V to 3.5V (pin 7). Frequency is set by a timing resistor from pin 6 to ground and a capacitor from pin 7 to ground. The oscillator period is approximately RC for the recommended range of 1.8k to 100k for R and 0.001μF to 0.1μF for C.

The fall time of the ramp sets the blanking or dead time where both outputs are off in push-pull regulators. This is controlled by the value of the capacitor alone.

Output Transistors

The two output transistors have both the emitters (pins 11 and 14) and the collectors available (pins 12 and 13). Internal current limiting for both of these transistors is about 100mA. The two transistors are driven 180° out of phase by the flip-flop. For single-ended operation they should be connected in parallel.

Error Amplifier

The differential input (pins 1 and 2) single-ended output (pin 9) transconductance amplifier provides about 80dB of gain, as well as providing a point for loop frequency compensation or electronic shutdown.

DC gain of the loop can be controlled by resistive loading, while AC compensation is usually accomplished with a series R-C connected from pin 9 to ground. The output impedance at pin 9 is about 5MΩ and current is about 200μA, so external op-amps or voltage sources can easily drive the comparator input. Normally, the 5V reference is divided down to generate a voltage within the common-mode range of the error amplifier.

Synchronous Operation

When an external clock is desired, a clock pulse of approximately 3V can be applied directly to the oscillator output, pin 3. The impedance to ground at this point is approximately 2kΩ. In this configuration, R_T C_T must be selected for a clock period slightly greater than that of the external clock.

If two or more LT1524 regulators are to be operated synchronously, all oscillator output terminals should be tied together. The oscillator programmed for the minimum clock period will be the master from which all the other LT1524s operate. In this application, the C_T R_T values of the slaved regulators must be set for a period approximately 10% longer than that of the master regulator. In addition, C_T (master) = 2 C_T (slave) to ensure that the master output pulse, which occurs first, has a wider pulse width and will subsequently reset the slave regulators.

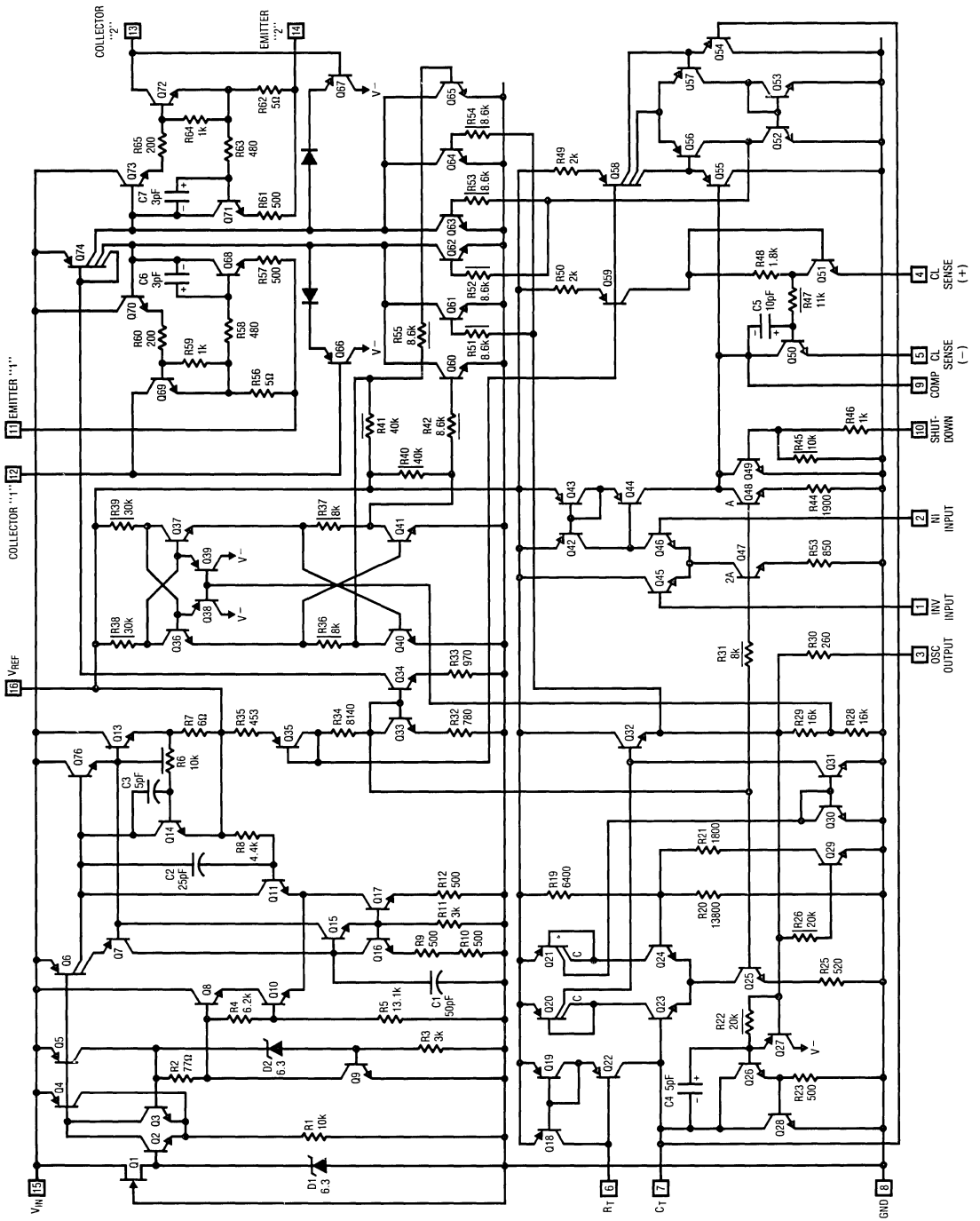
Shutdown

A logic high at pin 10 will shut down the regulator and cause both output transistors to turn off.

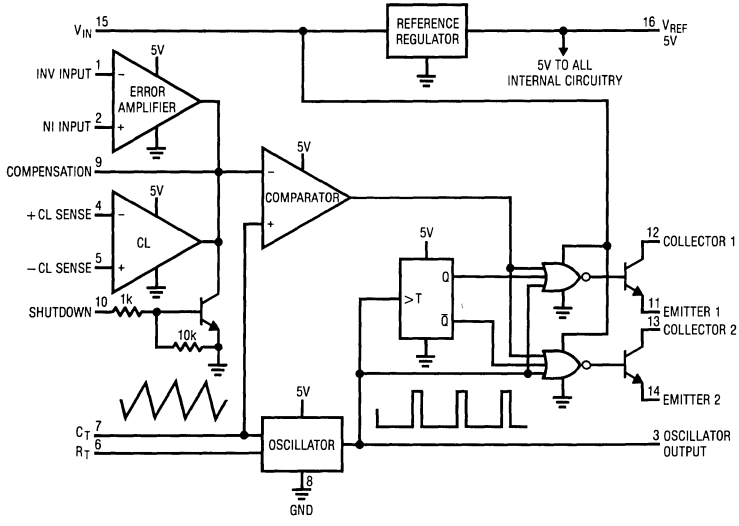
Current Limit

Current limiting is activated when the voltage between pins 4 and 5 exceeds 200mV. The output of the current limit amplifier internally sums with the error amplifier to shorten the output pulse width. The gain of the current limit circuitry is relatively low, so current control in limit is typically about 5%. Two areas of caution should be observed with current limiting. First, the response time of the current limit is set by the loop roll-off on pin 9. Fast current limiting requires external circuitry. Second, the common-mode range of the current limit amplifier is limited. Even fast spikes outside this range can disrupt operation.

SCHEMATIC DIAGRAM

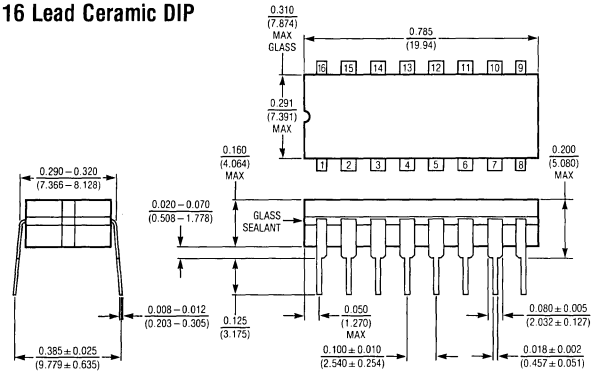


BLOCK DIAGRAM



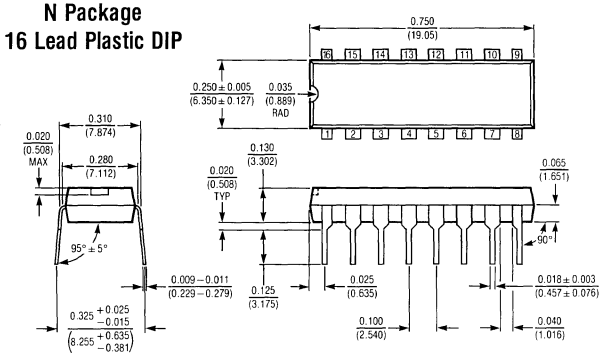
PACKAGE DESCRIPTION

J Package
16 Lead Ceramic DIP



	T_J MAX	Θ_{JA}	Θ_{JC}
LT1524J SG1524J	150°C	100°C/W	30°C/W
LT3524J SG3524J	150°C	100°C/W	30°C/W

N Package
16 Lead Plastic DIP



	T_J MAX	Θ_{JA}	Θ_{JC}
LT3524N SG3524N	115°C	140°C/W	50°C/W

Regulating Pulse Width Modulators

FEATURES

- Undervoltage Lockout with Hysteresis
- *Guaranteed* 1% 5.1V Reference
- *Guaranteed* 10mV/1000 Hr Long Term Stability
- Latching PWM
- 8V to 35V Operation
- 100Hz to 400kHz Oscillator
- 400mA Source and Sink Current

APPLICATIONS

- Switching Power Supplies
- Motor Speed Control
- Power Converters

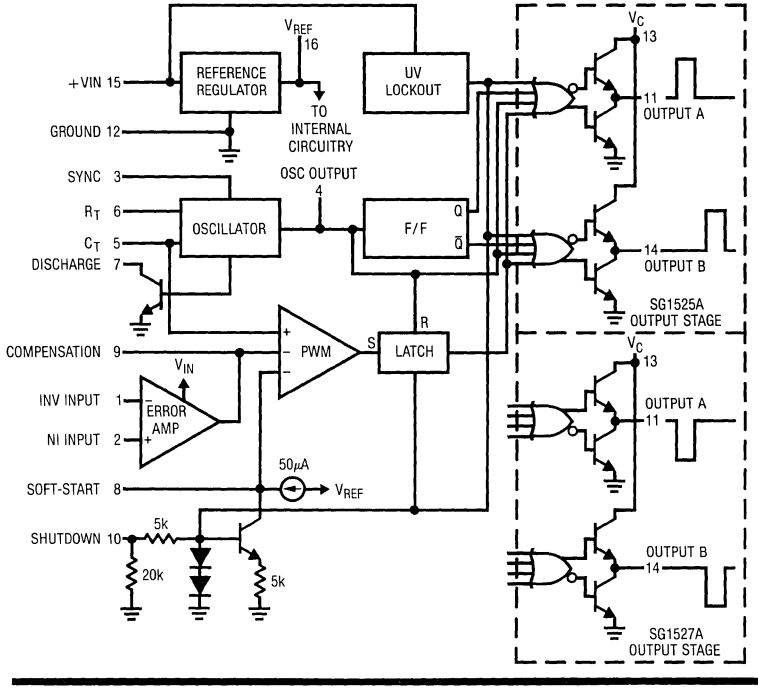
DESCRIPTION

The LT1525A and LT1527A are improved general purpose switching regulator control circuits. Included on the chip are a trimmed 1% voltage subsurface zener reference, oscillator, comparator and high current class B totem pole output drivers. Included in the design of the LT1525A are easy synchronization to an external clock, soft-start and adjustable deadtime control. A shutdown pin allows instantaneous shutdown.

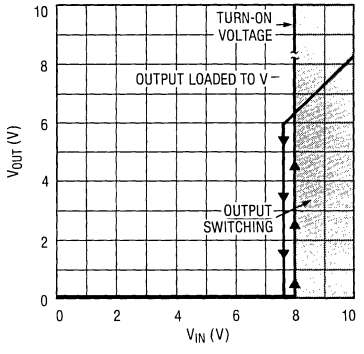
The LT1525A and LT1527A differ only in their output logic phasing. The LT1525A has a low output during the "off" state, while the LT1527A has a high output during the "off" state. Both devices have undervoltage lockout with about 0.5V hysteresis, giving reliable operation even with slowly varying supplies.

The combination of improved features and advanced processing for high reliability make Linear Technology's switching regulators a supreme choice.

BLOCK DIAGRAM



LT1525A Start-Up

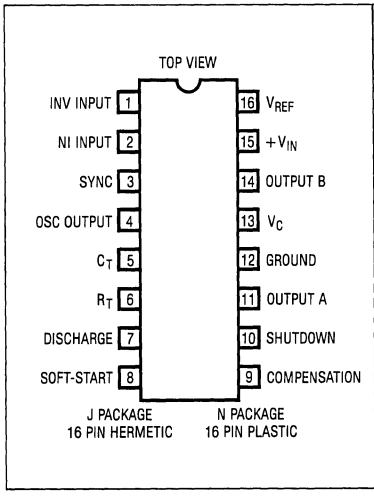


ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltage ($+V_{IN}$) ..... +40V
Logic Inputs ..... −0.3V to +5.5V
Analog Inputs ..... −0.3V to $+V_{IN}$
Output Current, Source or Sink 500mA
Reference Output Current 50mA
Oscillator Charging Current 5mA
Power Dissipation at $T_A = +25°C$ (Note 2)... 1000mW
Thermal Resistance: Junction to Ambient ... 100°C/W
Power Dissipation at $T_C = +25°C$ (Note 3)... 2000mW
Thermal Resistance: Junction to Case ..... 60°C/W
Operating Temperature Range
1525A, 1527A ..... −55°C to 150°C
3525A, 3527A ..... 0°C to 70°C
Storage Temperature Range ..... −65°C to 150°C
Lead Temperature (Soldering, 10 sec.) ..... +300°C

PACKAGE/ORDER INFORMATION



ORDER PART NUMBER

LT1525AJ
LT1527AJ
LT3525AJ
LT3527AJ
LT3525AN
LT3527AN

SG1525AJ
SG1527AJ
SG3525AJ
SG3527AJ
SG3525AN
SG3527AN

RECOMMENDED OPERATING CONDITIONS

(Note 4)

Input Voltage ($+V_{IN}$) ..... +8V to +35V
Collector Supply Voltage (V_C) ..... +4.5V to +35V
Sink/Source Load Current
(Steady State) ..... 0mA to 100mA
Sink/Source Load Current (Peak) ..... 0mA to 400mA
Reference Load Current ..... 0mA to 20mA
Oscillator Frequency Range ..... 100Hz to 400kHz
Oscillator Timing Resistor ..... 2kΩ to 150kΩ
Oscillator Timing Capacitor ..... 0.001μF to 0.1μF
Deadtime Resistor Range ..... 0Ω to 500Ω

ELECTRICAL CHARACTERISTICS $V_{IN} = +20V$ unless otherwise noted

PARAMETER	CONDITIONS		LT1525A LT1527A MIN	LT1525A LT1527A TYP	LT1525A LT1527A MAX	SG1525A SG1527A MIN	SG1525A SG1527A TYP	SG1525A SG1527A MAX	UNITS
REFERENCE SECTION									
Output Voltage	$T_j = 25°C$		5.05	5.10	5.15	5.05	5.10	5.15	V
Line Regulation	$V_{IN} = 8V$ to 35V	●		5	10		10	20	mV
Load Regulation	$I_L = 0mA$ to 20mA	●		20	50		20	50	mV
Temperature Stability		●		20	50		20	50	mV
Total Output Variation	Line, Load, and Temperature	●	5.0	5.1	5.2	5.0	5.1	5.2	V
Short Circuit Current	$V_{REF} = 0$, $T_j = 25°C$			80	100		80	100	mA
Output Noise Voltage	$10Hz \le f \le 10kHz$, $T_j = 25°C$			40	200		40	200	μVrms
Long Term Stability	$T_j = 125°C$			1	10		20	50	$mV/\sqrt{Khr}$

ELECTRICAL CHARACTERISTICS

PARAMETER	CONDITIONS		LT1525A LT1527A			SG1525A SG1527A			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
OSCILLATOR SECTION (Note 6)									
Initial Accuracy	$T_j = 25°C$ (Note 6)			2	6		2	6	%
Voltage Stability	$V_{IN} = 8V$ to 35V	●		0.5	1		0.3	1	%
Temperature Stability		●		3	6		3	6	%
Minimum Frequency	$R_T = 150k\Omega$, $C_T = 0.1\mu F$	●			100			100	Hz
Maximum Frequency	$R_T = 2k\Omega$, $C_T = 1nF$	●	400			400			kHz
Current Mirror	$I_{RT} = 2mA$	●	1.7	2.0	2.2	1.7	2.0	2.2	mA
Clock Amplitude		●	3.0	3.5		3.0	3.5		V
Clock Width	$T_j = 25°C$		0.3	0.5	1	0.3	0.5	1	μs
Sync Threshold		●	1.2	2.0	2.8	1.2	2.0	2.8	V
Sync Input Current	Sync Voltage = 3.5V	●		1.0	2.5		1.0	2.5	mA
ERROR AMPLIFIER SECTION (V_{CM} = 5.1V)									
Input Offset Voltage		●		0.5	5		0.5	5	mV
Input Bias Current		●		0.2	3		1	10	μA
Input Offset Current		●			0.5			1	μA
DC Open Loop Gain	$R_L \geq 10M\Omega$	●	70	80		60	75		dB
Gain Bandwidth Product	$A_V = 0dB$, $T_j = 25°C$ (Note 5)		1	2		1	2		MHz
Output Low Level		●		0.2	0.5		0.2	0.5	V
Output High Level		●	3.8	5.6		3.8	5.6		V
Common Mode Rejection	$V_{CM} = 1.5V$ to 5.2V	●	75	90		60	75		dB
Supply Voltage Rejection	$V_{IN} = 8V$ to 35V	●	75	90		50	60		dB
PWM COMPARATOR									
Minimum Duty Cycle		●			0			0	%
Maximum Duty Cycle		●	45	49		45	49		%
Input Threshold	Zero Duty Cycle (Note 6)	●	0.6	0.9		0.6	0.9		V
Input Threshold	Max Duty Cycle (Note 6)	●		3.3	3.6		3.3	3.6	V
Input Bias Current		●		0.05	1.0		0.05	1.0	μA
SOFT-START SECTION									
Soft-Start Current	$V_{SHUTDOWN} = 0V$	●	25	50	80	25	50	80	μA
Soft-Start Voltage	$V_{SHUTDOWN} = 2V$	●		0.4	0.6		0.4	0.6	V
Shutdown Input Current	$V_{SHUTDOWN} = 2.5V$	●		0.4	1.0		0.4	1.0	mA
OUTPUT DRIVERS (Each Output) (V_C = 20V)									
Undervoltage Lockout Hysteresis			0.2	0.6	1	0.2	0.6	1	V
Output Low Level	$I_{SINK} = 20mA$	●		0.2	0.4		0.2	0.4	V
	$I_{SINK} = 100mA$	●		1.0	2.0		1.0	2.0	V
Output High Level	$I_{SOURCE} = 20mA$	●	18	19		18	19		V
	$I_{SOURCE} = 100mA$	●	17	18		17	18		V
Undervoltage Lockout	V_{COMP} and V_{SS} = High	●	6	7	8	6	7	8	V
Collector Leakage	$V_C = 35V$ (Note 7)	●			200			200	μA
Rise Time	$C_L = 1nF$, $T_j = 25°C$ (Note 5)			100	600		100	600	ns
Fall Time	$C_L = 1nF$, $T_j = 25°C$ (Note 5)			50	300		50	300	ns
Shutdown Delay	$V_{SD} = 3V$, $C_S = 0$, $T_j = 25°C$ (Note 5)			0.2	0.5		0.2	0.5	μs
TOTAL STANDBY CURRENT									
Supply Current	$V_{IN} = 35V$	●		14	20		14	20	mA

ELECTRICAL CHARACTERISTICS

PARAMETER	CONDITIONS		LT3525A LT3527A			SG3525A SG3527A			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
REFERENCE SECTION									
Output Voltage	$T_j = 25°C$		5.05	5.10	5.15	5.00	5.10	5.20	V
Line Regulation	$V_{IN} = 8V$ to 35V	●		5	10		10	20	mV
Load Regulation	$I_L = 0mA$ to 20mA	●		20	50		20	50	mV
Temperature Stability		●		20	50		20	50	mV
Total Output Variation	Line, Load, and Temperature	●	4.95	5.1	5.25	4.95		5.25	V
Short Circuit Current	$V_{REF} = 0$, $T_j = 25°C$			80	100		80	100	mA
Output Noise Voltage	$10Hz \leq f \leq 10kHz$, $T_j = 25°C$			40	100		40	200	μVrms
Long Term Stability	$T_j = 125°C$			1	10		20	50	mV/khr
OSCILLATOR SECTION (Note 6)									
Initial Accuracy	$T_j = 25°C$ (Note 6)			2	6		2	6	%
Voltage Stability	$V_{IN} = 8V$ to 35V	●		0.5	2		1	2	%
Temperature Stability		●		3	6		3	6	%
Minimum Frequency	$R_T = 150k\Omega$, $C_T = 0.1\mu F$	●			100			100	Hz
Maximum Frequency	$R_T = 2k\Omega$, $C_T = 1nF$	●	400			400			kHz
Current Mirror	$I_{RT} = 2mA$	●	1.7	2.0	2.2	1.7	2.0	2.2	mA
Clock Amplitude		●	3.0	3.5		3.0	3.5		V
Clock Width	$T_j = 25°C$		0.3	0.5	1.0	0.3	0.5	1.0	μs
Sync Threshold		●	1.2	2.0	2.8	1.2	2.0	2.8	V
Sync Input Current	Sync Voltage = 3.5V	●		1.0	2.5		1.0	2.5	mA
ERROR AMPLIFIER SECTION ($V_{CM} = 5.1V$)									
Input Offset Voltage		●		2	5		2	10	mV
Input Bias Current		●		1	3		1	10	μA
Input Offset Current		●			0.5			1	μA
DC Open Loop Gain	$R_L \geq 10M\Omega$	●	70	80		60	75		dB
Gain Bandwidth Product	$A_V = 0dB$, $T_j = 25°C$ (Note 5)		1	2		1	2		MHz
Output Low Level		●		0.2	0.5		0.2	0.5	V
Output High Level		●	3.8	5.6		3.8	5.6		V
Common Mode Rejection	$V_{CM} = 1.5V$ to 5.2V	●	75	90		60	75		dB
Supply Voltage Rejection	$V_{IN} = 8V$ to 35V	●	75	90		50	60		dB
PWM COMPARATOR									
Minimum Duty Cycle		●			0			0	%
Maximum Duty Cycle		●	45	49		45	49		%
Input Threshold	Zero Duty Cycle (Note 6)	●	0.6	0.9		0.6	0.9		V
Input Threshold	Max Duty Cycle (Note 6)	●		3.3	3.6		3.3	3.6	V
Input Bias Current		●		0.05	1.0		0.05	1.0	μA
SOFT-START SECTION									
Soft-Start Current	$V_{SHUTDOWN} = 0V$	●	25	50	80	25	50	80	μA
Soft-Start Voltage	$V_{SHUTDOWN} = 2V$	●		0.4	0.6		0.4	0.6	V
Shutdown Input Current	$V_{SHUTDOWN} = 2.5V$	●		0.4	1.0		0.4	1.0	mA

ELECTRICAL CHARACTERISTICS

PARAMETER	CONDITIONS		LT3525A LT3527A MIN	TYP	MAX	SG3525A SG3527A MIN	TYP	MAX	UNITS
OUTPUT DRIVERS (Each Output) (V_C = 20V)									
Undervoltage Lockout Hysteresis			0.2	0.6		0.2	0.6		V
Output Low Level	I_{SINK} = 20mA	●		0.2	0.4		0.2	0.4	V
	I_{SINK} = 100mA	●		1.0	2.0		1.0	2.0	V
Output High Level	I_{SOURCE} = 20mA	●	18	19		18	19		V
	I_{SOURCE} = 100mA	●	17	18		17	18		V
Undervoltage Lockout	V_{COMP} and V_{SS} = High	●	6	7	8	6	7	8	V
Collector Leakage	V_C = 35V (Note 7)	●			200			200	μA
Rise Time	C_L = 1nF, T_j = 25°C (Note 5)			100	600		100	600	ns
Fall Time	C_L = 1nF, T_j = 25°C (Note 5)			50	300		50	300	ns
Shutdown Delay	V_{SD} = 3V, C_S = 0, T_j = 25°C (Note 5)			0.2	0.5		0.2	0.5	μs
TOTAL STANDBY CURRENT									
Supply Current	V_{IN} = 35V	●		14	20		14	20	mA

The ● denotes the specifications which apply of the full operating temperature range.

Note 1: Values beyond which damage may occur.

Note 2: Derate at 10mW/°C for ambient temperatures above +50°C.

Note 3: Derate at 16mW/°C for case temperatures above +25°C.

Note 4: Range over which the device is functional and parameter limits are guaranteed.

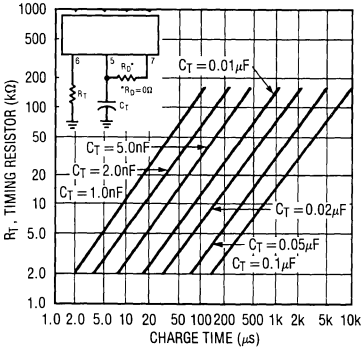
Note 5: These parameters, although guaranteed over the recommended operating conditions, are not 100% tested in production.

Note 6: Tested at f_{OSC} = 40kHz (R_T = 3.6kΩ, C_T = 0.01μF, R_D = 0Ω).

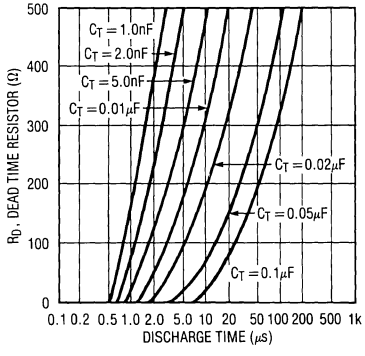
Note 7: Applies to 1525A/3525A only, due to polarity of output pulses.

TYPICAL PERFORMANCE CHARACTERISTICS

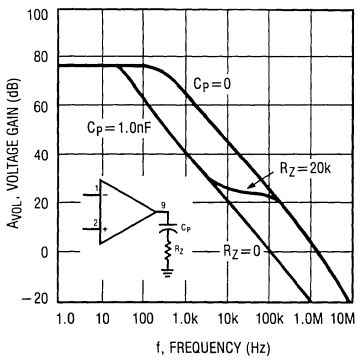
Oscillator Charge Time vs R_T



Oscillator Discharge Time

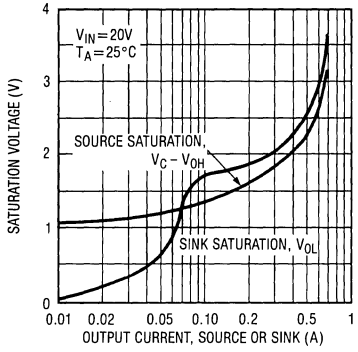


Error Amplifier Open Loop Frequency Response

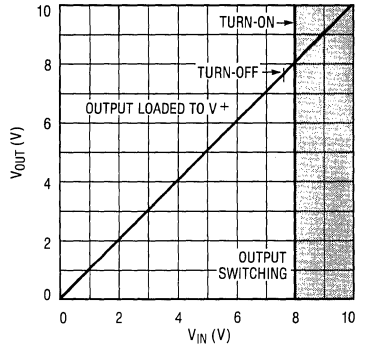


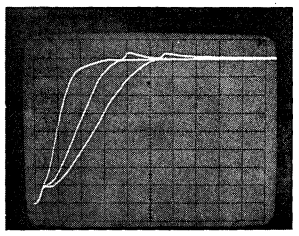
TYPICAL PERFORMANCE CHARACTERISTICS

1525A Output Saturation Characteristics

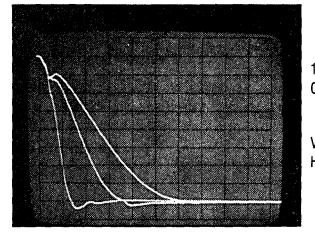


LT1527A Start-Up

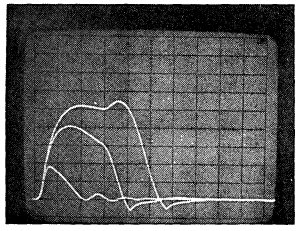




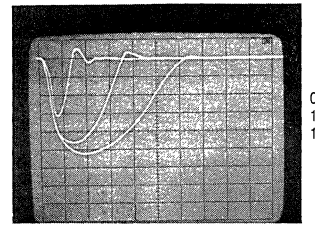
1525A/1527A
C_L = 1kpF,
= 5kpF,
= 10kpF
V = 2.5V/DIV
H = 100ns/DIV



1525A/1527A
C_L = 1kpF,
= 5kpF,
= 10kpF
V = 2.5V/DIV
H = 100ns/DIV



OUTPUT CURRENT
100mA/DIV
100ns/DIV



OUTPUT CURRENT
100mA/DIV
100ns/DIV

APPLICATIONS INFORMATION

Shutdown Options

1. An external open collector comparator or transistor can be used to pull down the compensation pin (9). This will set the PWM latch and turn off both outputs. Pulse-by-pulse protection can be accomplished if the shutdown signal is momentary, since the PWM latch will be reset with each clock pulse.
2. Shutdown can also be accomplished by pulling down on the soft-start pin (8). When using this approach, shutdown will not affect the amplifier compensation network; however, if a soft-start capacitor is used, it must be discharged, possibly slowing shutdown response.

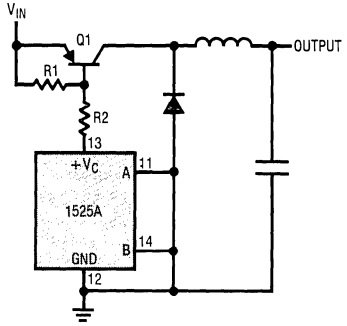
APPLICATIONS INFORMATION

3. Applying a positive-going signal to the shutdown pin (10) will provide the most rapid shutdown of the outputs if a soft-start capacitor is not used at pin 8. An external soft-start capacitor at pin 8 will slow shutdown response due to the discharge time of the soft-start capacitor. Discharge current is approximately twice the charging current.

4. The shutdown terminal can be used to set the PWM latch on a pulse-by-pulse basis if there is no external capacitance on pin 8. Soft-start characteristics may still be achieved by applying an external capacitor, blocking diode and charging resistor to the compensation pin (9).

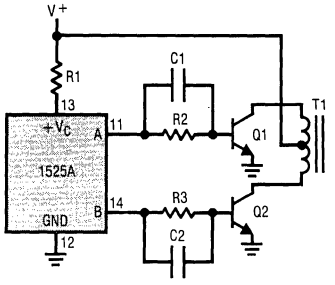
TYPICAL APPLICATIONS

Single Ended Supply



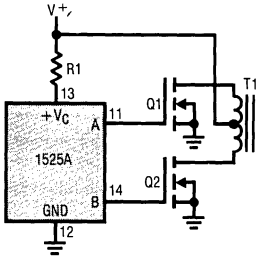
FOR SINGLE ENDED SUPPLIES, THE DRIVER OUTPUTS ARE GROUNDED. THE $+V_C$ TERMINAL IS SWITCHED TO GROUND BY THE TOTEM-POLE SOURCE TRANSISTORS ON EVERY OSCILLATOR CYCLE.

Bipolar Push-Pull Supply



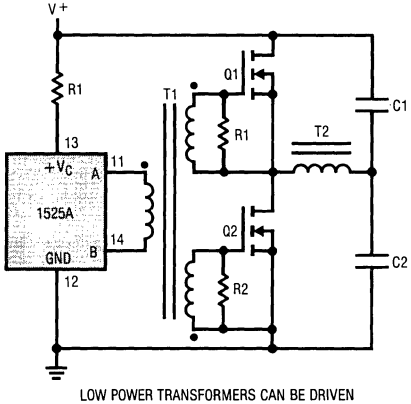
IN CONVENTIONAL PUSH-PULL BIPOLAR DESIGNS, FORWARD BASE DRIVE IS CONTROLLED BY R1–R3. RAPID TURN-OFF TIMES FOR THE POWER DEVICES ARE ACHIEVED WITH SPEED-UP CAPACITORS C1 AND C2.

Power FETs Push-Pull Supply



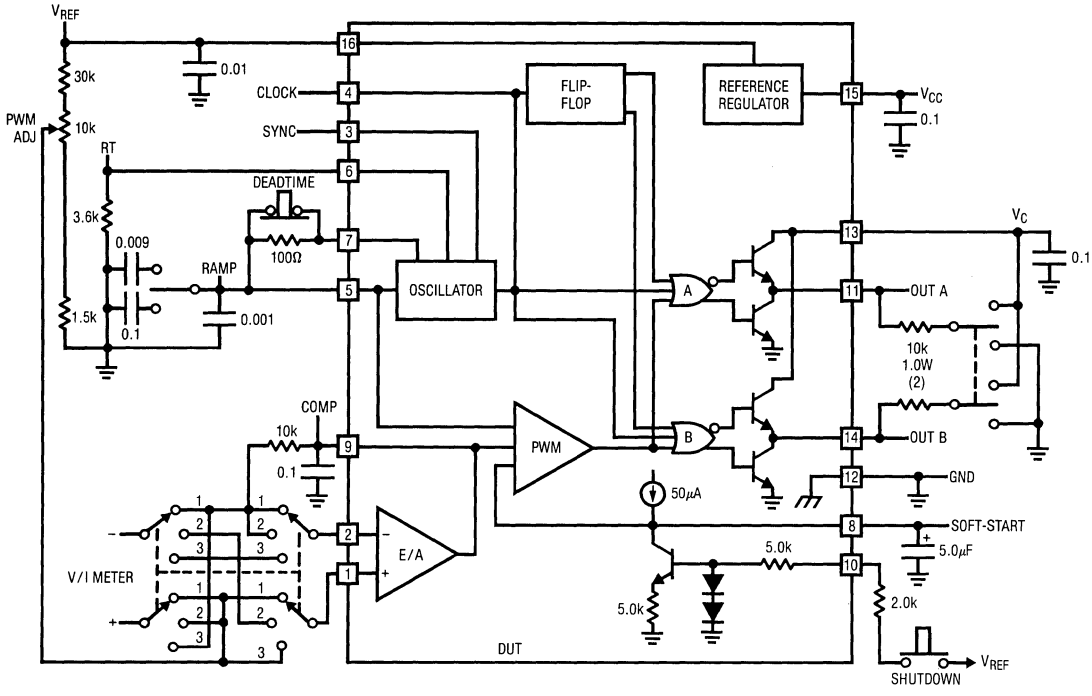
THE LOW SOURCE IMPEDANCE OF THE OUTPUT DRIVERS PROVIDES RAPID CHARGING OF POWER FET INPUT CAPACITANCE, WHILE MINIMIZING EXTERNAL COMPONENTS.

Driving Transformers Directly



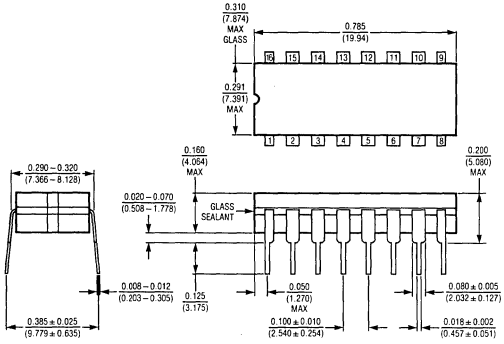
LOW POWER TRANSFORMERS CAN BE DRIVEN DIRECTLY BY THE 1525A. AUTOMATIC RESET OCCURS DURING DEADTIME, WHEN BOTH ENDS OF THE PRIMARY WINDING ARE SWITCHED TO GROUND.

TEST CIRCUIT



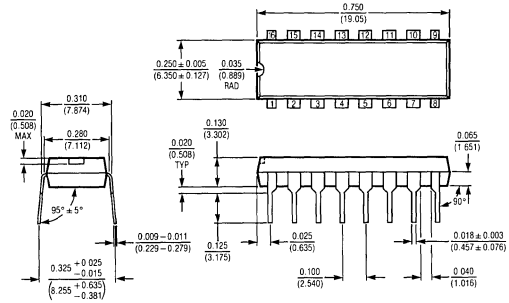
PACKAGE DESCRIPTION

16 Pin Cavity DIP (J)



	$T_j$max	Θ_{jA}	Θ_{jC}
LT/SG1525AJ LT/SG1527AJ	150°C	100°C/W	60°C/W
LT/SG3525AJ LT/SG3527AJ	150°C	100°C/W	60°C/W

16 Pin Molded DIP (N)



	$T_j$max	Θ_{jA}	Θ_{jC}
LT/SG3525AN LT/SG3527AN	105°C	100°C/W	60°C/W

Regulating Pulse Width Modulator

FEATURES

- 8V to 35V Operation
- *Guaranteed* ±1% 5V Reference
- *Guaranteed* 10mV/1000 Hrs. Long Term Stability
- *Guaranteed* ±3% Oscillator Temperature Stability
- Undervoltage Lockout
- 100mA Source/Sink Outputs

APPLICATIONS

- Switching Power Supplies
- Motor Speed Control
- Power Converters

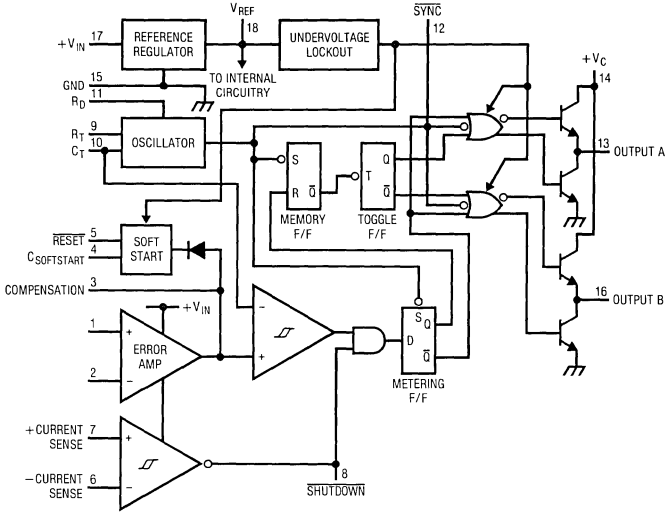
DESCRIPTION

The LT1526 is an improved general purpose switching regulator control ciruit. Included on the chip are a 1% voltage reference, oscillator, error amplifier, pulse width modulator and low impedance output drivers. Also included are protective features such as a current limit comparator, undervoltage lockout, soft-start circuitry, and adjustable deadtime. This versatile device can be used to implement single-ended or push-pull switching regulators of either polarity, both transformerless and transformer-coupled.

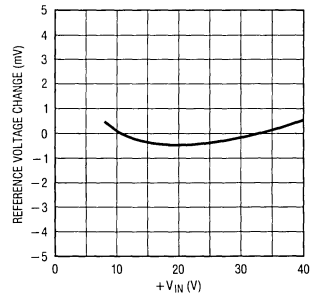
Although pin-for-pin and functionally compatible with industry standard 1526 and 3526 devices, Linear Technology has incorporated several improvements in the design of the LT1526. A subsurface zener has been used to provide excellent reference voltage stability and the reference offers improved line regulation and load regulation. The current limit comparator sense voltage initial accuracy and temperature stability have been greatly improved.

The combination of improved features and advanced linear processing for high reliability make Linear Technology's switching regulators a superior choice.

BLOCK DIAGRAM



Reference Line Regulation

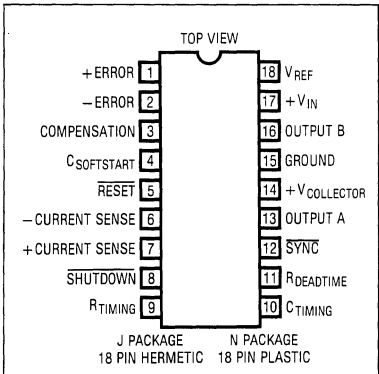


ABSOLUTE MAXIMUM RATINGS

(Note 1)

Input Voltage ($+V_{IN}$) ..... +40V
Collector Supply Voltage ($+V_C$) ..... +40V
Logic Inputs ..... −0.3V to +5.5V
Analog Inputs ..... −0.3V to $+V_{IN}$
Source/Sink Load Current (each output) 200mA
Reference Load Current 50mA
Logic Sink Current 15mA
Operating Junction Temperature Range
LT1526 ..... −55°C to +150°C
LT3526 ..... 0°C to +125°C
Storage Temperature Range ..... −65°C to +150°C
Lead Temperature (Soldering, 10sec) ..... +300°C

PACKAGE/ORDER INFORMATION



ORDER PART NUMBER
LT1526J LT3526J LT3526N

RECOMMENDED OPERATING CONDITIONS (Note 2)

Input Voltage ..... +8V to +35V
Collector Supply Voltage ..... +4.5V to +35V
Sink/Source Load Current (each output) ... 0mA to 100mA
Reference Load Current ..... −5mA to 20mA
Oscillator Frequency Range ..... 1Hz to 400kHz
Oscillator Timing Resistor ..... 2kΩ to 150kΩ
Oscillator Timing Capacitor ..... 1nF to 20μF
Available Deadtime Range at 40kHz ..... 3% to 50%

ELECTRICAL CHARACTERISTICS

($+V_{IN}$ = 15V, and over operating junction temperature, unless otherwise specified.)

PARAMETER	CONDITIONS		LT1526 MIN	LT1526 TYP	LT1526 MAX	LT3526 MIN	LT3526 TYP	LT3526 MAX	UNITS
REFERENCE SECTION (Note 3)									
Output Voltage	T_j = +25°C		4.95	5.00	5.05	4.90	5.00	5.10	V
Line Regulation	$+V_{IN}$ = 8V to 35V	●		2	10		2	15	mV
Load Regulation	I_L = −5mA to +20mA	●		5	10		5	20	mV
Temperature Stability		●		15	50		15	50	mV
Total Output Voltage Range	Over Recommended Operating Conditions	●	4.90	5.00	5.10	4.85	5.00	5.15	V
Short Circuit Current	V_{REF} = 0V	●	25	50	100	25	50	100	mA
Long Term Stability	T_j = 125°C			2	10		2	10	mV/√khr
UNDERVOLTAGE LOCKOUT									
$\overline{\text{RESET}}$ Output Voltage	V_{REF} = 3.8V	●		0.2	0.4		0.2	0.4	V
$\overline{\text{RESET}}$ Output Voltage	V_{REF} = 4.8V	●	2.4	4.8		2.4	4.8		V
OSCILLATOR SECTION (Note 4)									
Initial Accuracy	T_j = +25°C			±3	±8		±3	±8	%
Voltage Stability	$+V_{IN}$ = 8V to 35V	●		0.5	1		0.5	1	%
Temperature Stability		●		1	3		1	3	%

ELECTRICAL CHARACTERISTICS

($+V_{IN}$ = 15V, and over operating junction temperature, unless otherwise specified.)

PARAMETER	CONDITIONS		LT1526 MIN	LT1526 TYP	LT1526 MAX	LT3526 MIN	LT3526 TYP	LT3526 MAX	UNITS
OSCILLATOR SECTION (Note 4)									
Minimum Frequency	R_T = 150kΩ, C_T = 20μF	●			1			1	Hz
Maximum Frequency	R_T = 2kΩ, C_T = 1.0nF	●		400			400		kHz
Sawtooth Peak Voltage	$+V_{IN}$ = 35V	●		3.0	3.5		3.0	3.5	V
Sawtooth Valley Voltage	$+V_{IN}$ = 8V	●	0.5	1.0		0.5	1.0		V
ERROR AMPLIFIER SECTION (Note 5)									
Input Offset Voltage	$R_S \leq 2k\Omega$	●		2	5		2	10	mV
Input Bias Current		●		−350	−1000		−350	−2000	nA
Input Offset Current		●		35	100		35	200	nA
DC Open Loop Gain	$R_L \geq 10M\Omega$	●	64	72		60	72		dB
High Output Voltage	$V_{pin1} - V_{pin2} \geq 150mV$, I_{source} = 100μA	●	3.6	4.2		3.6	4.2		V
Low Output Voltage	$V_{pin2} - V_{pin1} \geq 150mV$, I_{sink} = 100μA	●		0.2	0.4		0.2	0.4	V
Common-Mode Rejection	$R_S \leq 2k\Omega$	●	70	94		70	94		dB
Supply Voltage Rejection	$+V_{IN}$ = 12V to 18V	●	66	80		66	80		dB
PWM COMPARATOR (Note 4)									
Minimum Duty Cycle	$V_{compensation}$ = +0.4V	●			0			0	%
Maximum Duty Cycle	$V_{compensation}$ = +3.6V	●	45	49		45	49		%
DIGITAL PORTS (SYNC, SHUTDOWN, and RESET)									
HIGH Output Voltage	I_{source} = 40μA	●	2.4	4.0		2.4	4.0		V
LOW Output Voltage	I_{sink} = 3.6mA	●		0.2	0.4		0.2	0.4	V
HIGH Input Current	V_{IH} = +2.4V	●		−125	−200		−125	−200	μA
LOW Input Current	V_{IL} = +0.4V	●		−225	−360		−225	−360	μA
CURRENT LIMIT COMPARATOR (Note 6)									
Sense Voltage	$R_S \leq 50\Omega$	●	90	100	110	80	100	120	mV
Input Bias Current		●		−3	−10		−3	−10	μA
SOFT-START SECTION									
Error Clamp Voltage	$\overline{RESET}$ = +0.4V	●		0.1	0.4		0.1	0.4	V
C_S Charging Current	$\overline{RESET}$ = +2.4V	●	50	100	150	50	100	150	μA
OUTPUT DRIVERS (Each Output) (Note 7)									
HIGH Output Voltage	I_{source} = 20mA	●	12.5	13.5		12.5	13.5		V
	I_{source} = 100mA	●	12	13		12	13		V
LOW Output Voltage	I_{sink} = 20mA	●		0.2	0.3		0.2	0.3	V
	I_{sink} = 100mA	●		1.2	2.0		1.2	2.0	V
Collector Leakage	V_C = 40V	●		50	150		50	150	μA
Rise Time	C_L = 1000pF	●		0.3	0.6		0.3	0.6	μs
Fall Time	C_L = 1000pF	●		0.1	0.2		0.1	0.2	μs
POWER CONSUMPTION (Note 8)									
Standby Current	$\overline{SHUTDOWN}$ = +0.4V	●		18	30		18	30	mA

The ● denotes specifications that apply over the full operating temperature range.

The shaded electrical specifications indicate those parameters which have been improved or guaranteed test limits provided for the first time.

Note 1: Values beyond which damage may occur.

Note 2: Range over which the device is functional and parameter limits are guaranteed.

Note 3: I_L = 0mA.

Note 4: f_{OSC} = 40kHz (R_T = 4.12kΩ ± 1%, C_T = 0.01μF ± 1%, R_D = 0Ω).

Note 5: V_{CM} = 0V to +5.2V.

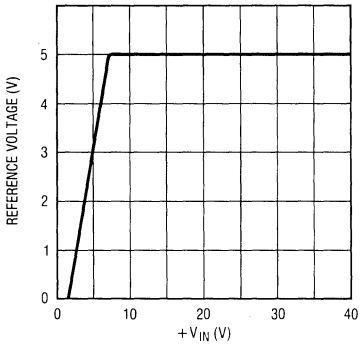
Note 6: V_{CM} = 0 to V_{IN} − 3V. The current limit sense voltage for the LT1526 is $80mV \leq V_{SENSE} \leq 120mV$ for temperatures less than 0°C or greater than 125°C.

Note 7: V_C = +15V.

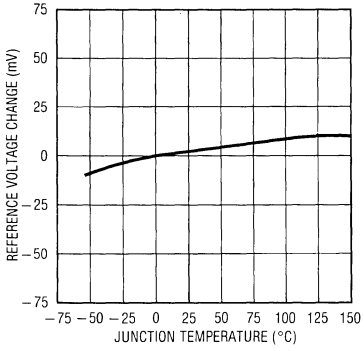
Note 8: $+V_{IN}$ = +35V, R_T = 4.12kΩ.

TYPICAL PERFORMANCE CHARACTERISTICS

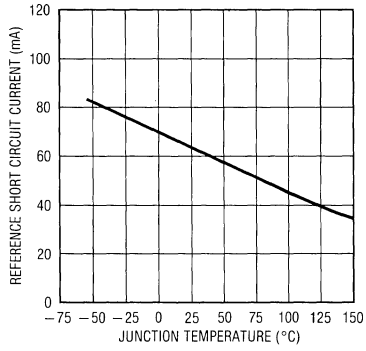
Reference Voltage vs Supply Voltage



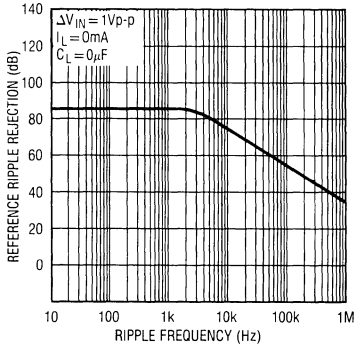
Reference Temperature Stability



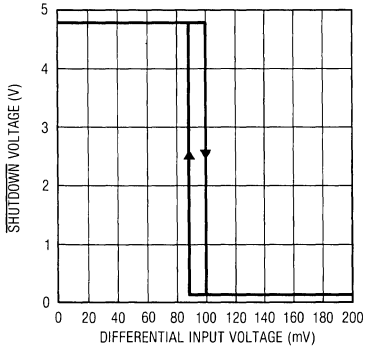
Reference Short Circuit Current



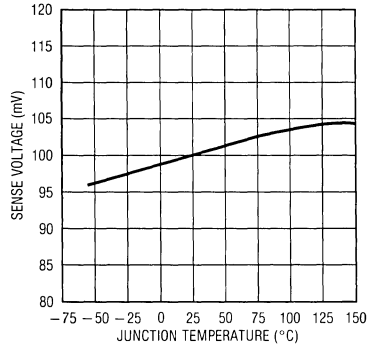
Reference Ripple Rejection



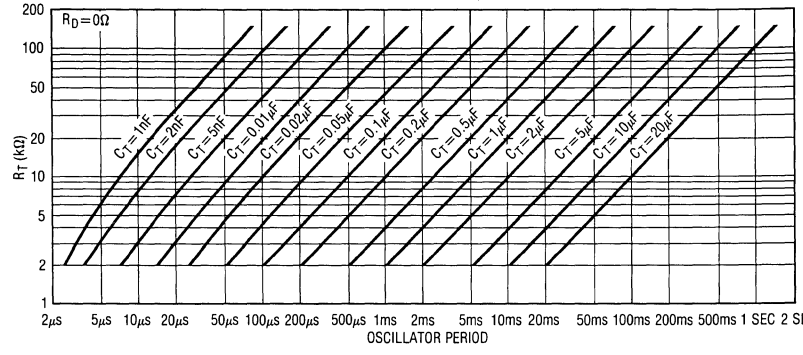
Current Limit Comparator Transfer Function



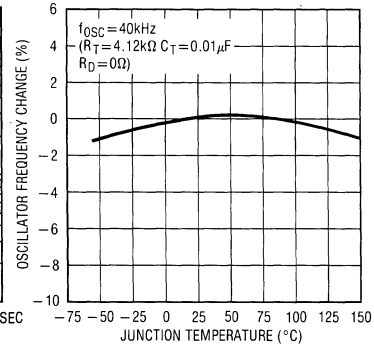
Current Limit Comparator Sense Voltage



Oscillator Period vs R_T and C_T

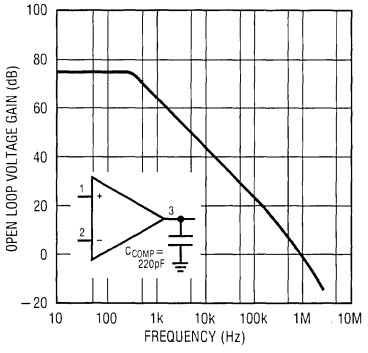


Oscillator Frequency Temperature Stability

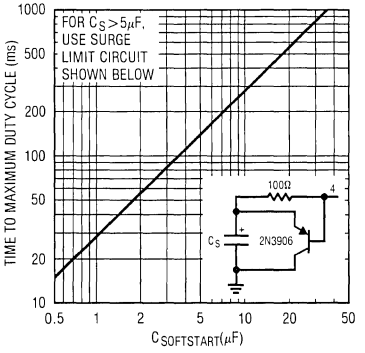


TYPICAL PERFORMANCE CHARACTERISTICS

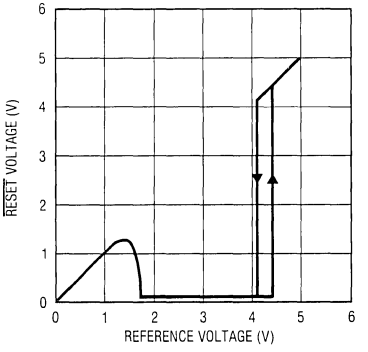
Error Amplifier Open Loop Gain vs Frequency



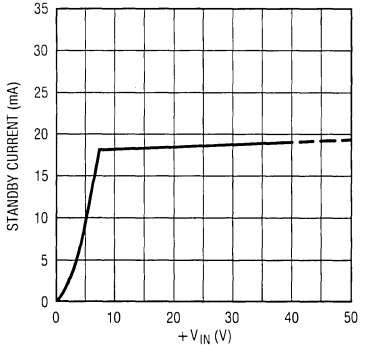
Soft-start Time Constant vs C_S



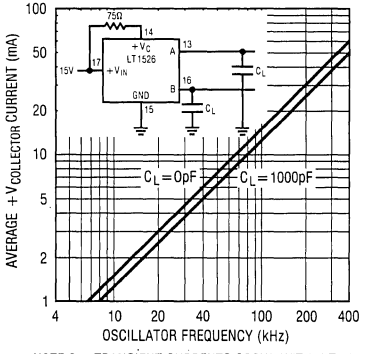
Undervoltage Lockout Characteristic



Standby Current vs Supply Voltage

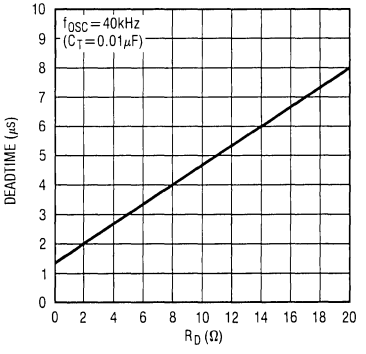


+$V_{COLLECTOR}$ Current (Note 9)

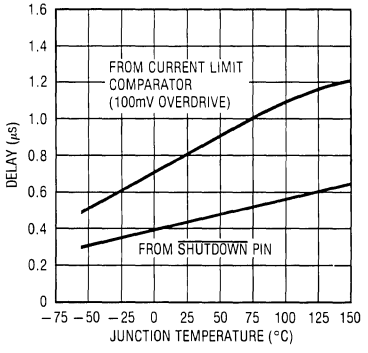


NOTE 9: TRANSIENT CURRENTS OCCUR WITHIN THE OUTPUT STAGES DURING SWITCHING; INDEPENDENT OF LOADING. THE GRAPH SHOWS THE AVERAGE (DC) VALUE OF THE TRANSIENT CURRENTS.

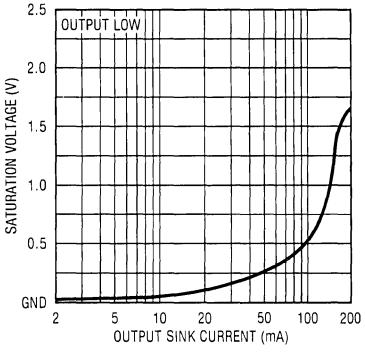
Output Driver Deadtime vs R_D



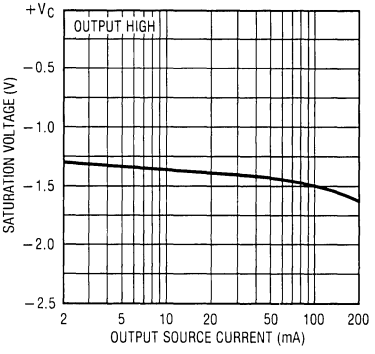
Output Driver Shutdown Delay



Output Driver Saturation Voltage vs I_{SINK}



Output Driver Saturation Voltage vs I_{SOURCE}



APPLICATIONS INFORMATION

FUNCTIONAL DESCRIPTION AND PIN FUNCTION

Voltage Reference

The reference regulator (pin 18) supplies a regulated 5.0V to all internal circuitry, as well as up to 20mA for external circuitry. It is fully active at supply voltages (pin 17) of 8V and greater.

The LT1526 can operate from a 5V supply by connecting $+V_{IN}$ to V_{REF} (pin 18 to pin 17) and maintaining the supply between 4.8V and 5.2V.

Undervoltage Lockout

The undervoltage lockout circuitry protects both the switching regulator and the power devices it controls from inadequate supply voltage, which can result in unstable control circuitry. If $+V_{IN}$ is too low, the circuit turns off the output drivers, holds $\overline{RESET}$ (pin 5) low and the soft-start capacitor in a discharged state.

Soft-Start

The soft-start circuitry protects the power devices from high surge currents during power supply turn-on by limiting the available PWM duty cycle.

When $+V_{IN}$ reaches a sufficient voltage to allow $\overline{RESET}$ to go high, a 100μA current source charges the external C_S capacitor (pin 4) linearly to 5V. The ERROR AMPLIFIER output is clamped to 600mV above the C_S voltage, and the available duty cycle of the PWM increases linearly. Maximum duty cycle is available when the C_S voltage reaches about 3V.

Digital Control Ports

The three digital control ports are bidirectional. Each port can drive TTL and 5V CMOS logic directly. They can also be driven by open-collector TTL, open-drain CMOS, and open-collector voltage comparators.

Driving $\overline{SYNC}$ (pin 12) low causes a discharge cycle in the oscillator. Driving $\overline{SHUTDOWN}$ (pin 8) low causes the outputs to turn off. Driving $\overline{RESET}$ (pin 5) low causes the outputs to turn off and discharges the C_S capacitor.

Oscillator

The internal oscillator circuitry sets the frequency of operation for the switching regulator. Frequency is set by R_T (pin 9), C_T (pin 10), and R_D (pin 11). With $R_D = 0\Omega$, the values for R_T and C_T may be chosen from the oscillator period graph. If the desired deadtime is increased, the value of R_T may need to be decreased to maintain the desired frequency.

The frequency at either output is half that of the oscillator, and the frequency at $+V_C$ (pin 14) is equal to the oscillator.

Synchronous Operation

Two or more switching regulators may be synchronized by setting the master to the desired frequency and sharing the oscillator signals with the slave units. Slave C_T pins are tied to the master C_T pin, and slave $\overline{SYNC}$ pins are tied to the master $\overline{SYNC}$ pin. Slave R_T and R_D pins are left open.

External logic synchronization can be used by setting the oscillator period to be 10% longer than the external clock period, and connecting the external clock to the $\overline{SYNC}$ pin. A periodic low of about 0.5μs wide will lock the oscillator to the external frequency.

Error Amplifier

The differential input (pins 1 and 2), single-ended output (pin 3) transconductance amplifier provides about 70dB of gain. The output has an impedance of 2MΩ, and since all voltage gain occurs at the output, the gain characteristics can be controlled with shunt reactance to ground.

Output Drivers

The totem-pole output drivers can source and sink 100mA continuously and 200mA peak. The outputs are driven 180° out of phase by the flip-flop. Loads can be driven either from the outputs or the $+V_C$ pin. Since large transient currents occur within the output stages during switching, a resistor is recommended in series with $+V_C$ (pin 14) to limit the peak current. The resistor value should be $+V_C/200mA$.

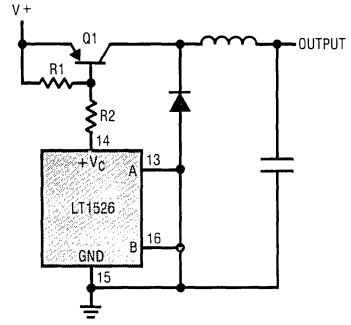
APPLICATIONS INFORMATION

Current Limit

The current limit comparator turns off the outputs when the input voltage (pin 7 to pin 6) exceeds 100mV. Hysteresis is built into the trip point, of about 10mV, to prevent oscillations.

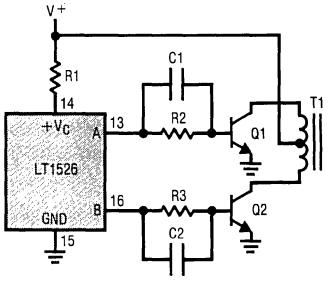
TYPICAL APPLICATIONS

Single Ended Supply



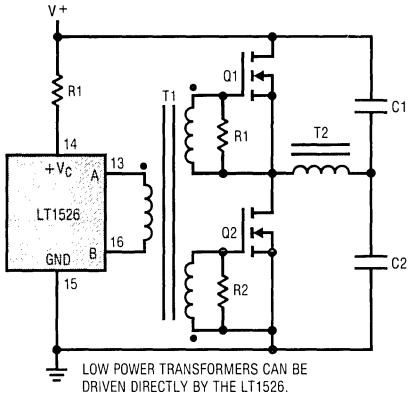
FOR SINGLE ENDED SUPPLIES, THE DRIVER OUTPUTS ARE GROUNDED. THE $+V_C$ TERMINAL IS SWITCHED TO GROUND BY THE TOTEM POLE SOURCE TRANSISTORS ON EVERY OSCILLATOR CYCLE.

Bipolar Push-Pull Supply



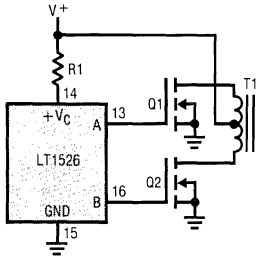
IN CONVENTIONAL BIPOLAR PUSH-PULL DESIGNS, FORWARD BASE DRIVE IS CONTROLLED BY R1-R3. RAPID TURN-OFF TIMES FOR THE POWER DEVICES ARE ACHIEVED WITH SPEED-UP CAPACITORS C1 AND C2.

Driving Transformers Directly



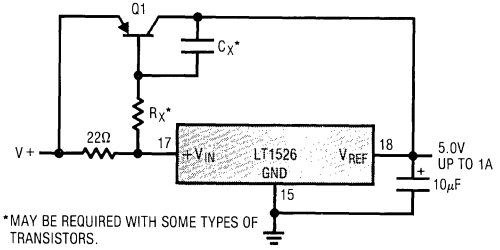
LOW POWER TRANSFORMERS CAN BE DRIVEN DIRECTLY BY THE LT1526. AUTOMATIC RESET OCCURS DURING DEAD-TIME, WHEN BOTH ENDS OF THE PRIMARY WINDING ARE SWITCHED TO GROUND.

Power FETs Push-Pull Supply



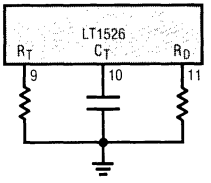
THE LOW SOURCE IMPEDANCE OF THE OUTPUT DRIVERS PROVIDES RAPID CHARGING OF POWER FET INPUT CAPACITANCE, WHILE MINIMIZING EXTERNAL COMPONENTS.

Extending Reference Output Current

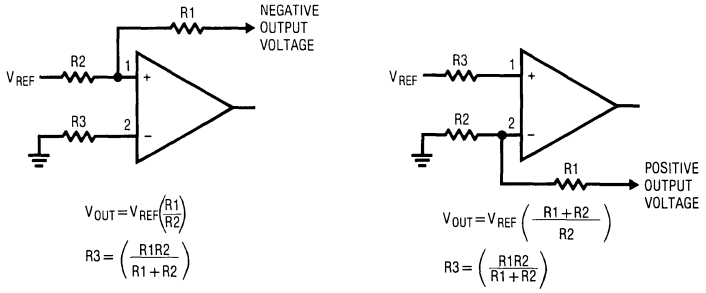


*MAY BE REQUIRED WITH SOME TYPES OF TRANSISTORS.

Oscillator Connections

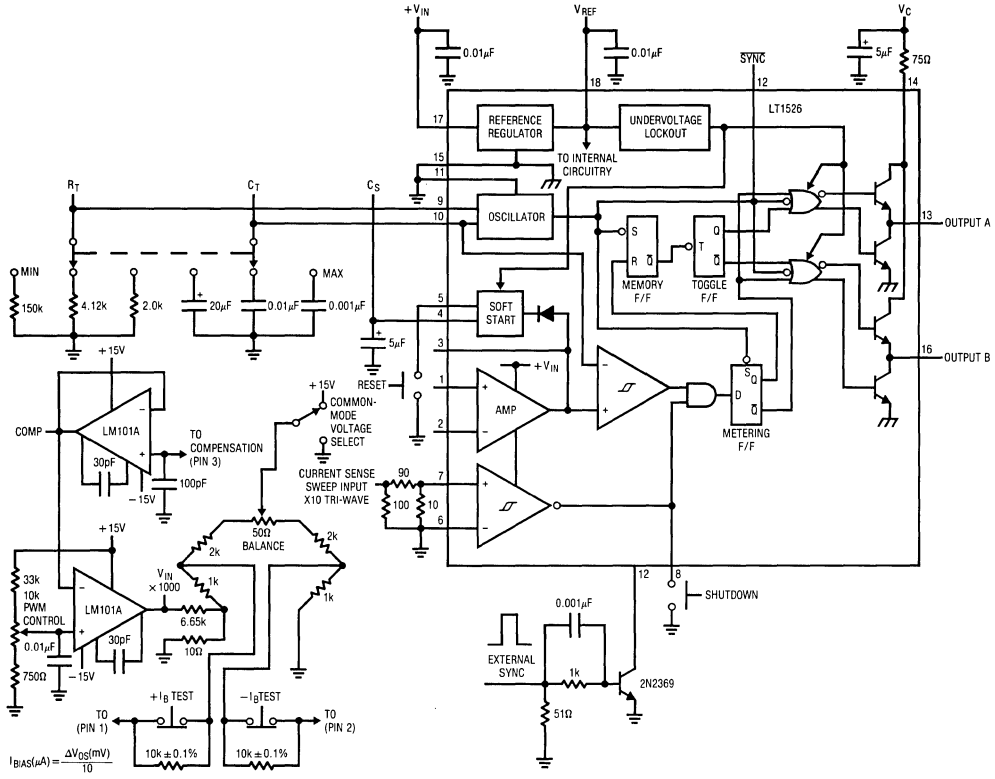


Error Amplifier Connections



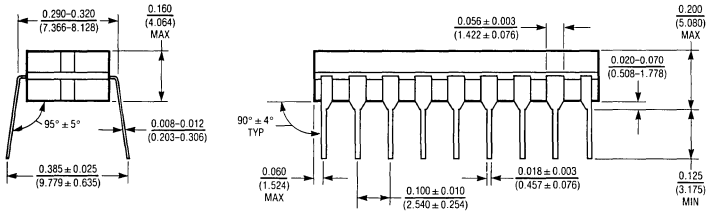
TYPICAL APPLICATIONS

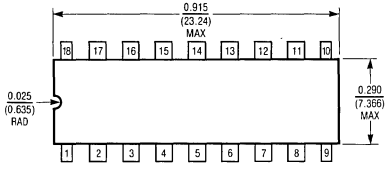
LT1526 Lab Test Fixture



PACKAGE DESCRIPTION

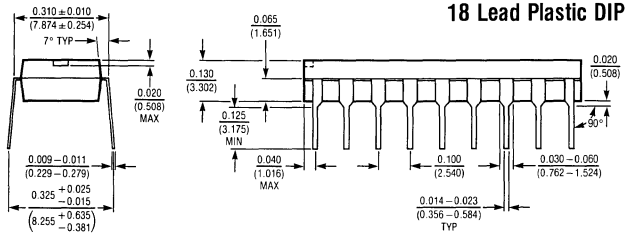
J Package
18 Lead Ceramic DIP

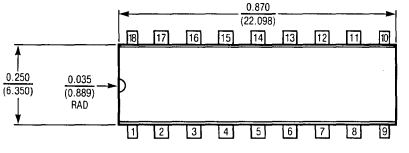




	T_{jmax}	Θ_{ja}	Θ_{jc}
LT1526J	150°C	100°C/W	40°C/W
LT3526J	150°C	100°C/W	40°C/W

N Package
18 Lead Plastic DIP





	T_{jmax}	Θ_{ja}	Θ_{jc}
LT3526N	125°C	100°C/W	40°C/W

Current Mode PWM Controller

FEATURES

- Automatic Feed-Forward Compensation
- Programmable Pulse-by-Pulse Current Limiting
- ±1% Bandgap Reference
- Undervoltage Lockout
- External Shutdown
- Dual 200mA Totem Pole Outputs
- Double Pulse Suppression
- Soft-Start Capability

APPLICATIONS

- Switching Power Supplies
- Motor Speed Control
- Power Converters

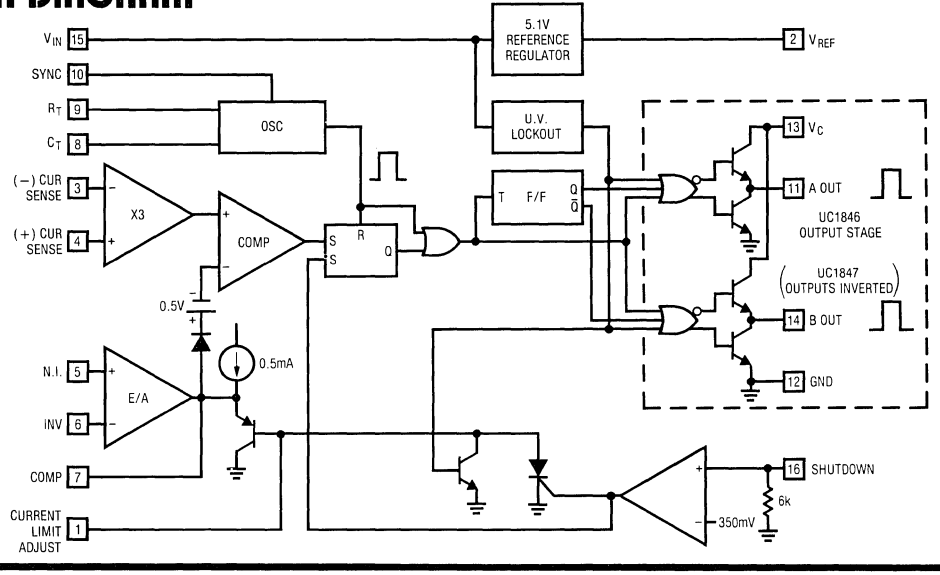
DESCRIPTION

The UC1846 family of control ICs contains all necessary circuitry to implement fixed frequency, fixed output voltage, current mode control schemes. Current mode control loops are easy to design and compensate, and provide superior transient line regulation, inherent pulse-by-pulse current limiting, and automatic symmetry correction for push-pull converters. In addition, the UC1846 has built-in undervoltage lockout with hysteresis to prevent oscillations near the threshold, soft-start capability, and can be shut down instantaneously by an external logic level. Internal logic prevents double-pulsing and output overlap.

The oscillator circuitry of the UC1846 allows the user to adjust output deadtime as well as frequency and also provides a bidirectional sync pin to allow paralleling power modules.

Both the internal error amplifier and current sense amplifiers operate over a wide common-mode range to allow design flexibility. The dual outputs provide active pull up/pull down, ideal for driving bipolar or FET switches. The internal reference regulator provides excellent stability for changes in line, load, and temperature. The UC1846 outputs are low in the off state while the UC1847 outputs are high in the off state.

BLOCK DIAGRAM

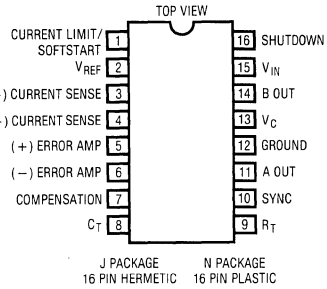


ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltage (Pin 15) ..... +40V
Collector Supply Voltage (Pin 13) ..... +40V
Output Current, Source or Sink (Pins 11, 14) 500mA
Analog Inputs (Pins 3, 4, 5, 6, 16) ..... −0.3V to +V_{IN}
Reference Output Current (Pin 2) ..... −30mA
Sync Output Current (Pin 10) ..... −5mA
Error Amplifier Output Current (Pin 7) ..... −5mA
Soft Start Sink Current (Pin 1) 50mA
Oscillator Charging Current (Pin 9) 5mA
Operating Temperature Range
UC1846/1847 ..... −55°C to +125°C
UC3846/3847 ..... 0°C to 70°C
Power Dissipation at T_A = 25°C (Note 2) 1000mW
Power Dissipation at T_C = 25°C (Note 3) 2000mW
Thermal Resistance, Junction to Ambient ..... 100°C/W
Thermal Resistance, Junction to Case ..... 60°C/W
Storage Temperature Range ..... −65°C to +150°C
Lead Temperature (Soldering, 10sec) ..... +300°C

PACKAGE/ORDER INFORMATION



ORDER PART NUMBER
UC1846J
UC1847J
UC3846J
UC3847J
UC3846N
UC3847N

ELECTRICAL CHARACTERISTICS (Note 4)

PARAMETER	CONDITIONS		UC1846/UC1847			UC3846/UC3847			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Reference Voltage									
Output Voltage	T_j = 25°C, I_O = 1mA		5.05	5.10	5.15	5.00	5.10	5.20	V
Line Regulation	V_{IN} = 8V to 40V	●		5	20		5	20	mV
Load Regulation	I_L = 1mA to 10mA	●		3	15		3	15	mV
Temperature Stability	Over Operating Range, (Note 5)	●		0.4			0.4		mV/°C
Total Output Variation	Line, Load, and Temperature (Note 5)	●	5.00		5.20	4.95		5.25	V
Output Noise Voltage	10Hz ≤ f ≤ 10kHz, T_j = 25°C (Note 5)			100			100		μV
Long Term Stability	T_j = 125°C, 1000Hrs., (Note 5)			5			5		mV
Short Circuit Output Current	V_{REF} = 0V	●	−10	−45		−10	−45		mA
Oscillator Section									
Initial Accuracy	T_j = 25°C		39	43	47	39	43	47	kHz
Voltage Accuracy	V_{IN} = 8V to 40V	●		−1	±2		−1	±2	%
Temperature Stability	Over Operating Range (Note 5)	●		−1			−1		%
Sync Output High Level		●	3.9	4.35		3.9	4.35		V
Sync Output Low Level		●		2.5	2.7		2.5	2.7	V
Sync Input High Level	Pin 8 = 0V	●	3.9	3.0		3.9	3.0		V
Sync Input Low Level	Pin 8 = 0V	●		3.0	2.7		3.0	2.7	V
Sync Input Current	Sync Voltage = 5.25V, Pin 8 = 0V	●		0.7	1.5		0.7	1.5	mA
Error Amp Section									
Input Offset Voltage		●		0.5	5		0.5	10	mV
Input Bias Current		●		−0.6	−1		−0.6	−2	μA
Input Offset Current		●		40	250		40	250	nA
Common-Mode Range	V_{IN} = 8V to 40V	●	0		V_{IN} − 2V	0		V_{IN} − 2V	V

ELECTRICAL CHARACTERISTICS (Note 4)

PARAMETER	CONDITIONS		UC1846/UC1847			UC3846/UC3847			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Error Amp Section (Cont.)									
Open Loop Voltage Gain	ΔV_O = 1.2V to 3V	❶	80	105		80	105		dB
Unity Gain Bandwidth		●	0.7	1.0		0.7	1.0		MHz
CMRR	V_{CM} = 0V to 38V, V_{IN} = 40V	●	75	100		75	100		dB
PSRR	V_{IN} = 8V to 40V	●	80	105		80	105		dB
Output Sink Current	V_{ID} = −15mV to −5V, $V_{Pin\,7}$ = 1V	●	2	6		2	6		mA
Output Source Current	V_{ID} = 15mV to 5V, $V_{Pin\,7}$ = 2.5V	●	−0.4	−0.5		−0.4	−0.5		mA
High Level Output Voltage	R_L (Pin 7) = 15kΩ	●	4.3	4.6		4.3	4.6		V
Low Level Output Voltage	R_L (Pin 7) = 15kΩ	●		0.7	1		0.7	1	V
Current Sense Amplifier Section									
Amplifier Gain	$V_{Pin\,3}$ = 0V, Pin 1 Open (Notes 6 & 7)	●	2.5	3.0	3.15	2.5	3.0	3.15	V
Maximum Differential Input Signal ($V_{Pin\,4} - V_{Pin\,3}$)	Pin 1 Open (Note 6) R_L (Pin 7) = 15kΩ	●	1.1	1.2		1.1	1.2		V
Input Offset Voltage	$V_{Pin\,1}$ = 0.5V Pin 7 Open (Note 6)	●		5	25		5	25	mV
CMRR	V_{CM} = 1V to 12V	❷	60	83		60	83		dB
PSRR	V_{IN} = 8V to 40V	●	60	84		60	84		dB
Input Bias Current	$V_{Pin\,1}$ = 0.5V, Pin 7 Open (Note 6)	●		−2.5	−10		−2.5	−10	μA
Input Offset Current	$V_{Pin\,1}$ = 0.5V, Pin 7 Open (Note 6)	❷		0.08	1		0.08	1	μA
Input Common-Mode Range		❷	0		V_{IN} − 3	0		V_{IN} − 3	V
Delay to Outputs	T_j = 25°C, (Note 5)			200	500		200	500	ns
Current Limit Adjust Section									
Current Limit Offset	$V_{Pin\,3}$ = 0V $V_{Pin\,4}$ = 0V, Pin 7 Open (Note 6)	●	0.4	0.5	0.55	0.4	0.5	0.55	V
Input Bias Current	$V_{Pin\,5}$ = V_{REF}, $V_{Pin\,6}$ = 0V	❷		−10	−30		−10	−30	μA
Shutdown Terminal Section									
Threshold Voltage		❷	250	350	400	250	350	400	mV
Input Voltage Range		●	0		V_{IN}	0		V_{IN}	V
Minimum Latching Current ($I_{Pin\,1}$)	(Note 8)	❷	3.0	1.5		3.0	1.5		mA
Maximum Non-Latching ($I_{Pin\,1}$)	(Note 9)	❹		1.5	0.8		1.5	0.8	mA
Delay to Outputs	(Note 5), T_j = 25°C			300	600		300	600	ns
Output Section									
Collector-Emitter Voltage		●	40			40			V
Collector Leakage Current	V_C = 40V (Note 10)	●			200			200	μA
Output Low Level	I_{SINK} = 20mA	●		0.1	0.4		0.1	0.4	V
	I_{SINK} = 100mA	●		0.4	2.1		0.4	2.1	
Output High Level	I_{SOURCE} = 20mA	●	13	13.5		13	13.5		V
	I_{SOURCE} = 100mA	●	12	13.5		12	13.5		
Rise Time	(Note 5), C_L = 1nF, T_j = 25°C			50	300		50	300	ns
Fall Time	(Note 5), C_L = 1nF, T_j = 25°C			50	300		50	300	ns
Undervoltage Lockout Section									
Start-Up Threshold		●		7.7	8.0		7.7	8.0	V
Threshold Hysteresis		●		0.75			0.75		V
Total Standby Current									
Supply Current	(Note 11)	●		17	21		17	21	mA

The ● denotes the specifications that apply over the full operating temperature range.

Note 1: All voltages are with respect to Ground, pin 12. Currents are positive into, negative out of the specified terminal.

Note 2: Derate at 10mW/°C for T_A above 50°C.

Note 3: Derate at 16mW/°C for T_C above 25°C.

Note 4: Unless otherwise stated V_{IN} = 15V, R_T = 10k, C_T = 4.7nF.

Note 5: These parameters, although guaranteed over the recommended operating conditions are not 100% tested in production.

Note 6: Parameter measured at trip point of latch with $V_{Pin\,5} = V_{REF}$, $V_{Pin\,6}$ = 0V.

Note 7: Amplifier gain defined as

$$G = \frac{\Delta V_{Pin\,7}}{\Delta V_{Pin\,4}};\ \Delta V_{Pin\,4} = 0V \text{ to } 1.0V$$

Note 8: Current into pin 1 guaranteed to latch circuit in shutdown state.

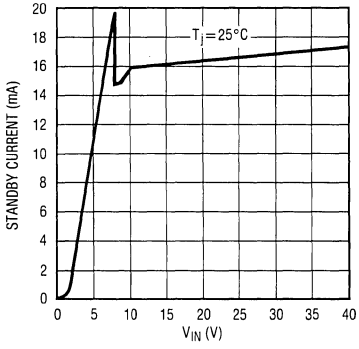
Note 9. Current into pin 1 guaranteed not to latch circuit in shutdown state.

Note 10: Applies to UC1846/3846 only due to polarity of outputs.

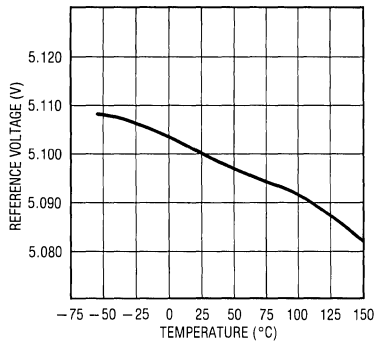
Note 11: Standby currrent does not include oscillator charging current, error and current limit dividers, and the outputs are open circuit.

TYPICAL PERFORMANCE CHARACTERISTICS

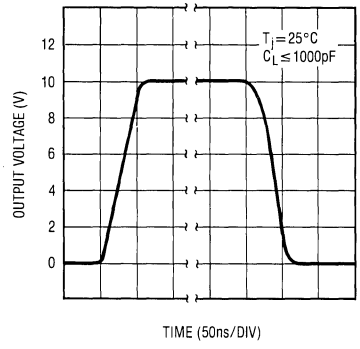
Standby Current vs V_{IN}



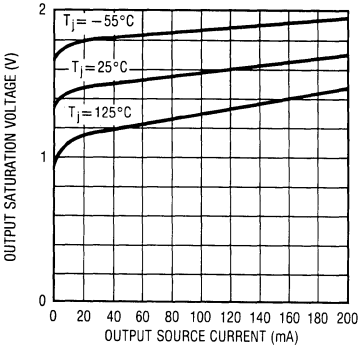
Reference Voltage vs Temperature



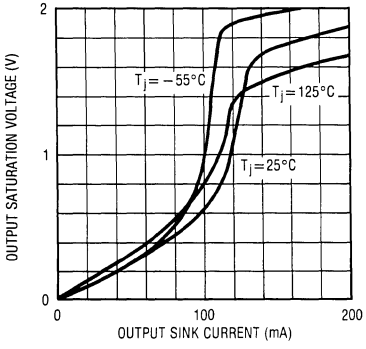
Output Rise and Fall Time



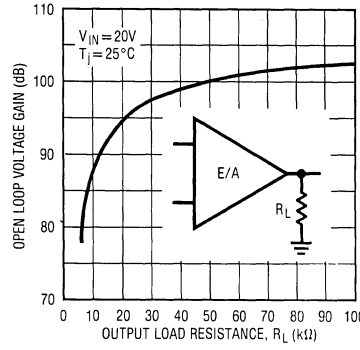
Output High Level Saturation Voltage vs Output Source Current



Output Low Level Saturation Voltage vs Output Sink Current

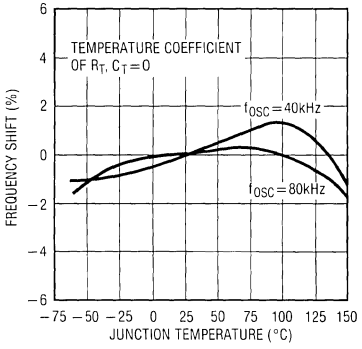


Error Amp Open-Loop DC Gain vs Load Resistance

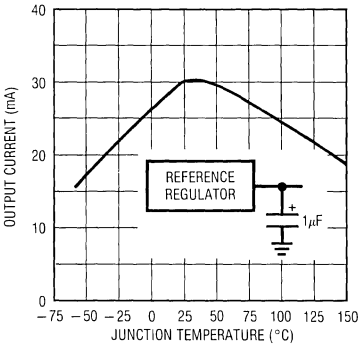


TYPICAL PERFORMANCE CHARACTERISTICS

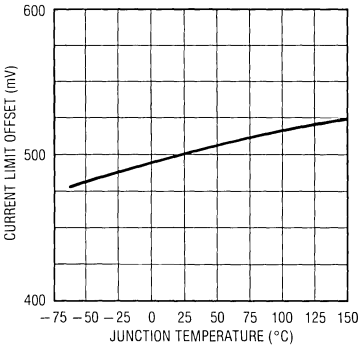
Oscillator Frequency vs Temperature



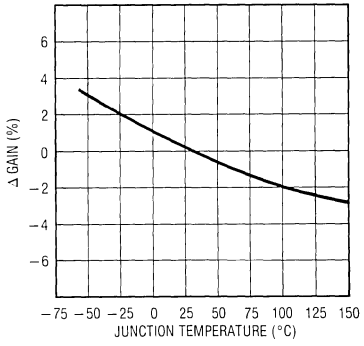
Reference Current Limit



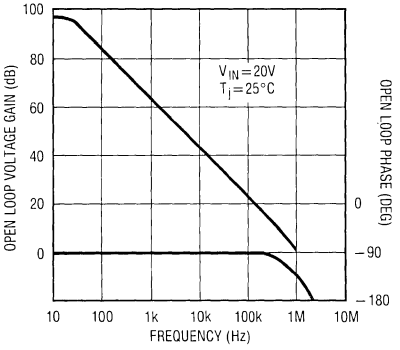
Current Limit Offset vs Temperature



Current Sense Amplifier Gain vs Temperature



Error Amplifier Gain and Phase vs Frequency



APPLICATIONS INFORMATION

Current Mode Control

Current mode controllers directly control peak inductor current with the error signal rather than controlling the duty cycle of the PWM as conventional controllers do. There are several inherent advantages in this type of control.

Current mode controllers are easier to frequency compensate. Peak inductor current is forced to follow the error signal and can change only if the error signal changes. This forces the inductor to act like a constant current source at mid frequencies and the order of the system can be reduced by one, eliminating 90° of phase shift.

Peak current on a pulse-by-pulse basis can be limited by simply limiting the positive swing of the error amplifier.

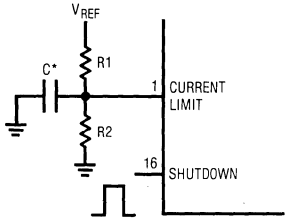
Transient line regulation is greatly improved. A change in the line voltage causes a change in the slope of the inductor current. This means that the time it takes for the inductor current to reach the peak control value automatically changes, and requires very little change in the output of the error amp. Since transient response is limited by the integrator response of the error amplifier, excellent line transient response is obtained if the error amplifier output does not have to change.

APPLICATIONS INFORMATION

With current mode control, some amount of slope compensation is required to prevent oscillations for duty cycles greater than 50%. Slope compensation can also be used to decrease noise sensitivity for low values of inductor current ripple, and to prevent subharmonic oscillations in the inductor current.

Shutdown/Soft Start

A logic high at pin 16 will initiate a shutdown cycle. During a shutdown cycle, both outputs are held off and pins 1 and 7 are pulled low. If pin 1 current ($I_{Pin\ 1} = V_{REF}/R_1$) is less than the latch threshold current, typically 1.5mA (see Electrical Characteristics), the device will restart at the end of the shutdown pulse. If pin 1 current is greater than the latch threshold current, the device will latch off until power is recycled.

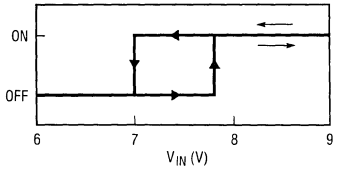


Soft start is accomplished by the addition of a capacitor from pin 1 to ground. This forces the peak value of the switch current to come up slowly. Pin 16 can be left floating if the shutdown function is not used.

Undervoltage Lockout

The purpose of the undervoltage lockout is to prevent the device from switching until the internal circuitry is operating properly. Built-in hysteresis prevents the circuit from oscillating at the threshold point. Pin 1 (current limit adjust) and pin 7 (comp) are held low during undervoltage lockout, and outputs are low (UC1846) or high (UC1847).

Output Switches



Oscillator Section

The frequency of the oscillator is set by an external resistor (R_T) from pin 9 to ground, and an external capacitor (C_T) from pin 8 to ground. C_T is charged by a constant current $I_{R_T} = V_{Pin\ 9}$ (≈3.6V)/R_T, and is discharged by a constant current 8mA – I_{R_T}. Upper and lower trip levels are determined by the internal circuitry, such that the oscillator frequency is approximated by the formula

$$f_T \approx \frac{2.2}{R_T(\Omega)C_T(F)}.$$

In addition, output deadtime, which is equal to the capacitor discharge time, is a function of the size of C_T and can be calculated according to the formula:

$$T_d = 145C_T\left(\frac{8mA}{8mA - \frac{3.6V}{R_T}}\right)$$

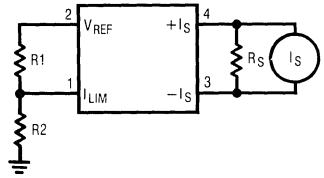
For large values of R_T (small I_{RT}): $T_d \approx 145C_T$.

Current Limit

Peak switch current on a pulse-by-pulse basis is a function of the voltage level set at pin 1 and the current sense resistor R_S, and can be determined by the formula:

$$I_S = \frac{\frac{R2\ V_{REF}}{R1 + R2} - 0.5V}{G \bullet R_S}$$

G = I/A GAIN = 2.75 TYP

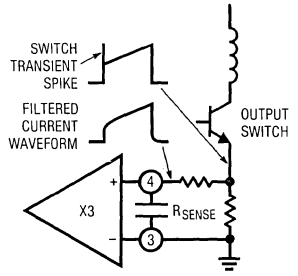


APPLICATIONS INFORMATION

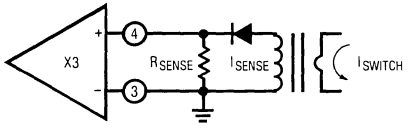
Current Sensing

The current sense amplifier is a differential amplifier with a gain of 3 and a common-mode range of 0 to $V_{IN}-3V$. Maximum differential input signal is 1.2V. Several sensing schemes are possible. Direct resistive sensing is the simplest, but power losses in the resistor may not be acceptable. The use of a current sense transformer will increase efficiency for higher current levels, but will increase circuit complexity. In configurations where switch current is sensed, a small RC may be necessary to keep switch turn on transients from tripping the current sense latch. Without this filter, erratic operation will result especially at lower values of output current. Minimum on-time of the output switch during a short circuit is equal to the delay from the current sense amplifier to the output, typically 200ns. This delay will be longer if a filter for switch transients is added. For best noise immunity, the signal at the current sense amplifier inputs should be as large as possible.

Resistive Sensing of Switch Current with RC Filter



Transformer Sensing Gives Isolation and Improved Efficiency



Error Amplifier

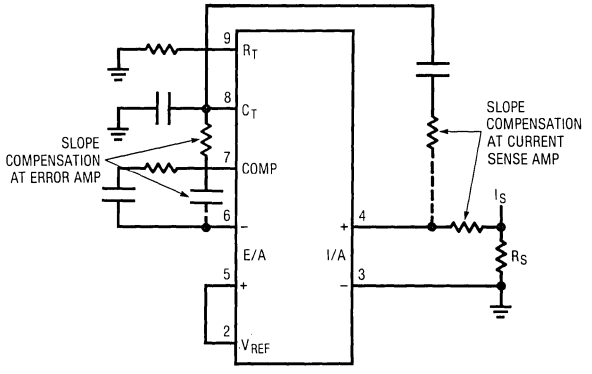
The error amplifier of the UC1846 can operate over a common-mode range of 0 to $V_{IN}-2V$. The output stage consists of an NPN Darlington pull-down and a 0.5mA current source pull-up. See Typical Performance Characteristics for gain and phase characteristics.

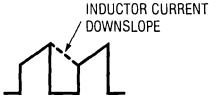
Reference Regulator

The reference regulator provides a fixed 5.1V for internal circuitry as well as up to 20mA of output current for external circuitry such as the current limit divider. A small bypass capacitor (0.1-1.0μF) from the reference pin (pin 2) to the ground pin (pin 12) is recommended. This capacitor should be located as close as possible to the device.

Slope Compensation

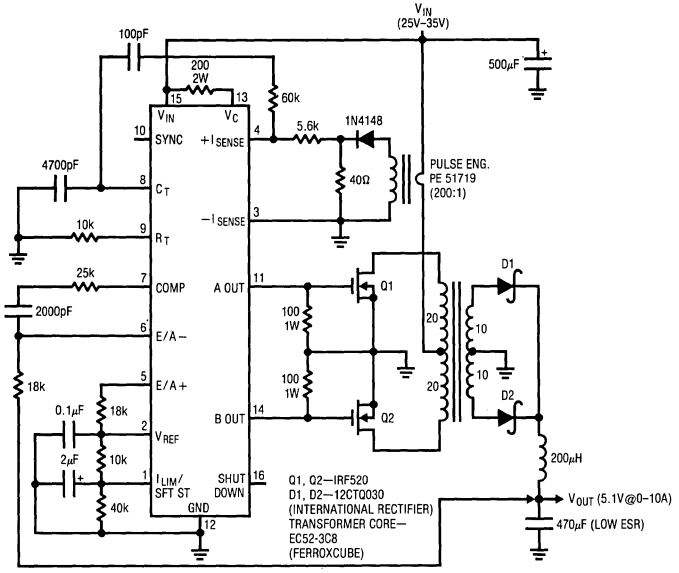
Slope compensation can be accomplished by summing a triangle wave derived from the oscillator waveform, with the inductor current waveform at the current sense amplifier input or the summing node of the error amplifier as shown below. Slope compensation should be greater than 1/2 of the downslope of the inductor current waveform.





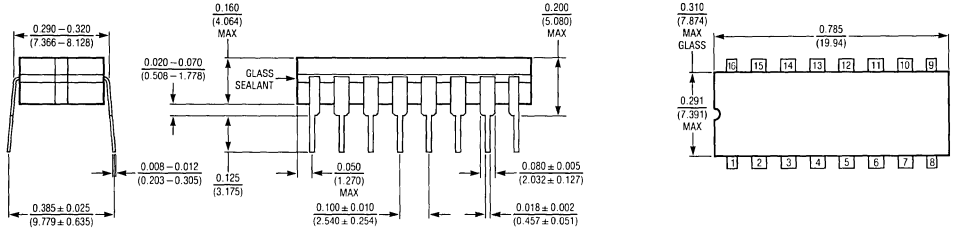
TYPICAL APPLICATIONS CIRCUIT

Push-Pull Forward Converter



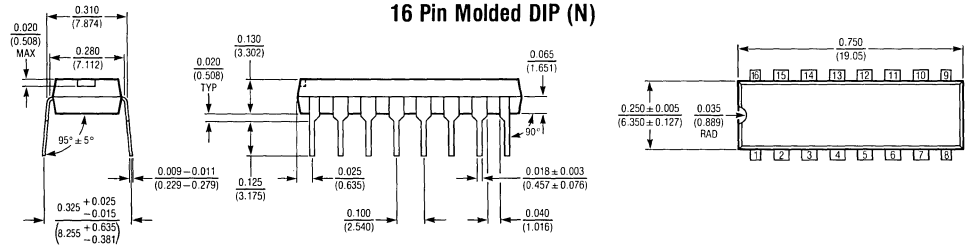
PACKAGE DESCRIPTION Dimensions in inches (millimeters) unless otherwise noted.

16 Pin Cavity DIP (J)



	T_{jmax}	Θ_{JA}	Θ_{JC}
UC1846 UC1847	150°C	100°C/W	60°C/W
UC3846 UC3847	105°C	100°C/W	60°C/W

16 Pin Molded DIP (N)



LINEAR TECHNOLOGY

SECTION 8—CMOS/ DATA CONVERSION/ INTERFACE

SECTION 8—CMOS/DATA CONVERSION/INTERFACE

Dual Precision Instrumentation Switched-Capacitor Building Block

FEATURES

- Instrumentation Front End with 120dB CMRR
- Precise, Charge-Balanced Switching
- Operates from 3V to 18V
- Internal or External Clock
- Operates up to 5MHz Clock Rate
- Low Power
- Two Independent Sections with One Clock

APPLICATIONS

- Precision Instrumentation Amplifiers
- Ultra Precision Voltage Inverters, Multipliers and Dividers
- V–F and F–V Converters
- Sample and Hold
- Switched-Capacitor Filters

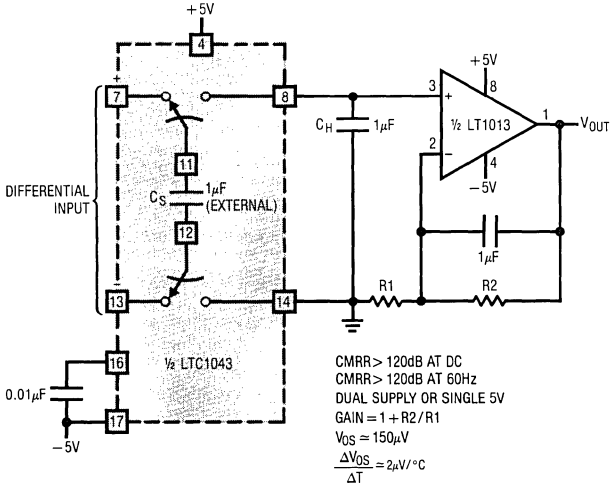
DESCRIPTION

The LTC1043 is a monolithic, charge-balanced, dual switched-capacitor instrumentation building block. A pair of switches alternately connects an external capacitor to an input voltage and then connects the charged capacitor across an output port. The internal switches have a break-before-make action. An internal clock is provided and its frequency can be adjusted with an external capacitor. The LTC1043 can also be driven with an external CMOS clock.

The LTC1043, when used with low clock frequencies, provides ultra precision DC functions without requiring precise external components. Such functions are differential voltage to single-ended conversion, voltage inversion, voltage multiplication and division by 2, 3, 4, 5, etc. The LTC1043 can also be used for precise V–F and F–V circuits without trimming, and it is also a building block for switched-capacitor filters, oscillators and modulators.

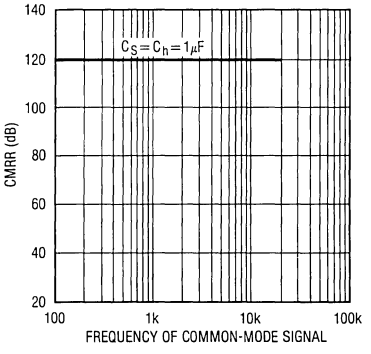
The LTC1043 is manufactured using Linear Technology's enhanced LTCMOS™ silicon gate process.

Instrumentation Amplifier



CMRR > 120dB AT DC
CMRR > 120dB AT 60Hz
DUAL SUPPLY OR SINGLE 5V
GAIN = 1 + R2/R1
$V_{OS} \approx 150\mu V$
$\frac{\Delta V_{OS}}{\Delta T} = 2\mu V/°C$
COMMON-MODE INPUT VOLTAGE INCLUDES THE SUPPLIES

CMRR vs Frequency

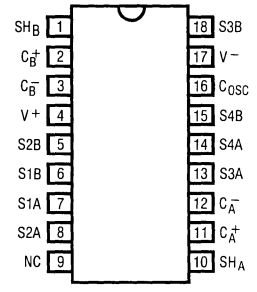


LTCMOS™ is a trademark of Linear Technology Corporation

ABSOLUTE MAXIMUM RATINGS

Supply Voltage 18V
Input Voltage
at Any Pin ..... $-0.3V \leq V_{IN} \leq V^+ + 0.3V$
Operating Temperature Range
LTC1043C ..... $-40°C \leq T_A \leq 85°C$
LTC1043M ..... $-55°C \leq T_A \leq 125°C$
Storage Temperature Range ..... $-65°C$ to $150°C$
Lead Temperature (Soldering, 10 sec.)..... 300°C

PACKAGE/ORDER INFORMATION



ORDER PART NUMBER
LTC1043CN LTC1043MD

ELECTRICAL CHARACTERISTICS $V^+ = 10V$, $V^- = 0V$, $T_A = 25°C$ unless otherwise specified.

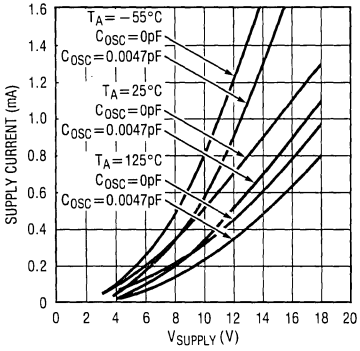
SYMBOL	PARAMETER	CONDITIONS		LTC1043M MIN	LTC1043M TYP	LTC1043M MAX	LTC1043C MIN	LTC1043C TYP	LTC1043C MAX	UNITS
I_S	Power Supply Current	Pin (16) Connected High or Low			0.25	0.4		0.25	0.4	mA
			●			0.7			0.7	mA
		C_{OSC} (Pin 16 to V^-) = 100pF			0.4	0.65		0.4	0.65	mA
			●			1			1	mA
I_I	OFF Leakage Current	Any Switch, Test Circuit 1 (Note 1)			6	100		6	100	pA
			●		6	500		6		nA
R_{ON}	ON Resistance	Test Circuit 2, $V_{IN} = 7V$, $I = \pm 0.5mA$ $V^+ = 10V$, $V^- = 0V$			240	400		240	400	Ω
			●			700			700	Ω
R_{ON}	ON Resistance	Test Circuit 2, $V_{IN} = 3.1V$, $I = \pm 0.5mA$ $V^+ = 5V$, $V^- = 0V$			400	700		400	700	Ω
			●			1			1	kΩ
f_{OSC}	Internal Oscillator Frequency	C_{OSC} (Pin 16 to V^-) = 0pF			185			185		kHz
		C_{OSC} (Pin 16 to V^-) = 100pF Test Circuit 3		20	34	50	20	34	50	kHz
			●	15		75	15		75	kHz
I_{OSC}	Pin Source or Sink Current	Pin 16 at V^+ or V^-			40	70		40	70	μA
			●			100			100	μA
	Break-Before-Make Time				25			25		ns
	Clock to Switching Delay	C_{OSC} Pin Externally Driven			75			75		ns
f_M	Maximum External CLK Frequency	C_{OSC} Pin Externally Driven with CMOS Levels			5			5		MHz
CMRR	Common-Mode Rejection Ratio	$V^+ = 5V$, $V^- = -5V$, $-5V < V_{CM} < 5V$, DC to 400Hz			120			120		dB

The ● denotes the specifications which apply over the full operating temperature range: LTC1043M operates from $-55°C \leq T_A \leq 125°C$; LTC1043C operates from $-40°C \leq T_A \leq 85°C$.

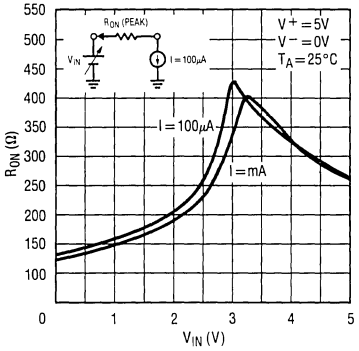
Note 1: OFF leakage current is guaranteed but not tested at 25°C.

TYPICAL PERFORMANCE CHARACTERISTICS (Test Circuits 2 through 4)

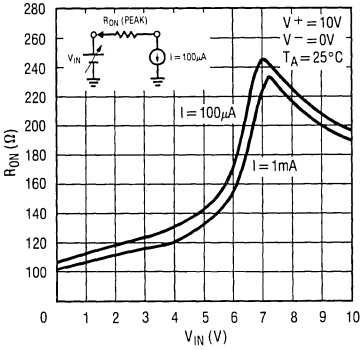
Power Supply Current vs Power Supply Voltage



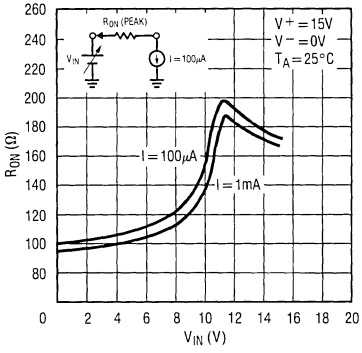
RON vs VIN



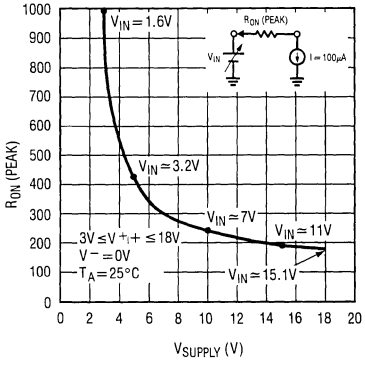
RON vs VIN



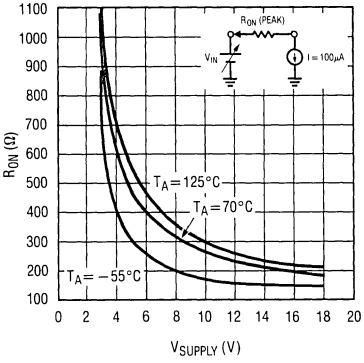
RON vs VIN



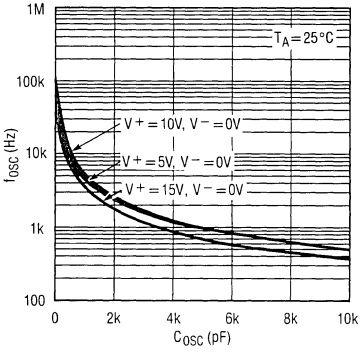
RON (Peak) vs Power Supply Voltage



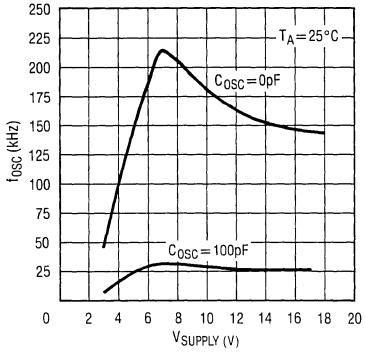
RON (Peak) vs Power Supply Voltage and Temperature



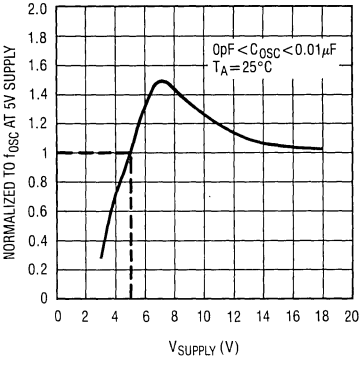
Oscillator Frequency, fOSC, vs COSC



Oscillator Frequency, fOSC, vs Supply Voltage

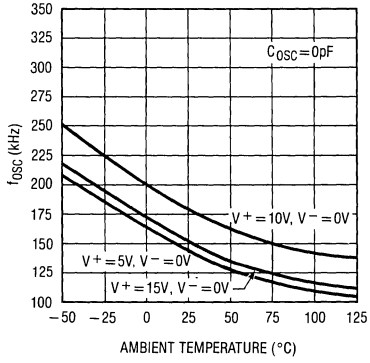


Normalized Oscillator Frequency, fOSC, vs Supply Voltage

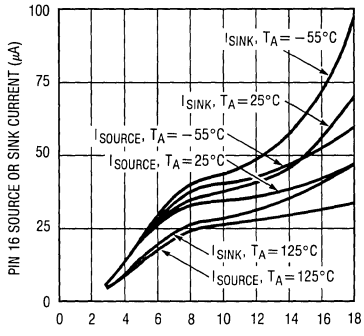


TYPICAL PERFORMANCE CHARACTERISTICS (Test Circuits 2 through 4)

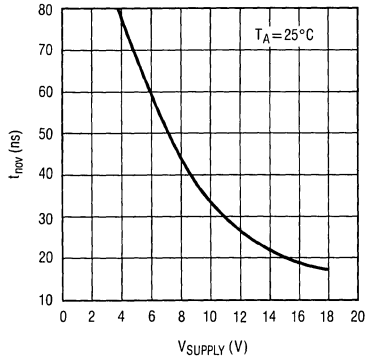
Oscillator Frequency, f_{OSC}, vs Ambient Temperature, T_A



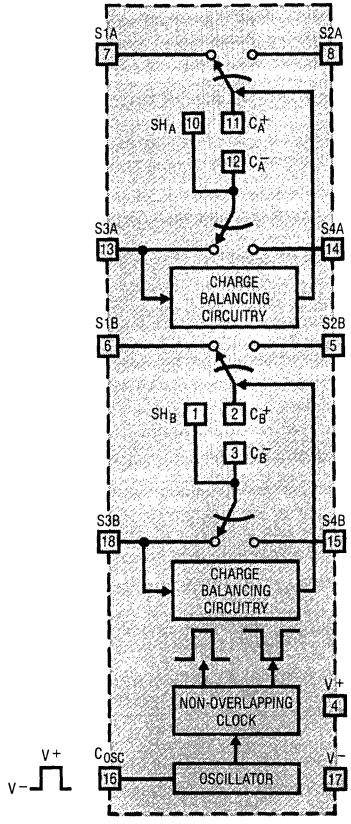
C_{OSC} Pin I_{SINK}, I_{SOURCE} vs Supply Voltage



Break-Before-Make Time, t_{nov}, vs Supply Voltage



BLOCK DIAGRAM

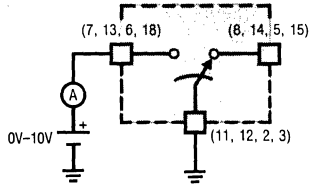


THE SWITCHES ARE TIMED AS SHOWN WITH PIN 16 HIGH

THE CHARGE BALANCING CIRCUITRY SAMPLES THE VOLTAGE AT S3 WITH RESPECT TO S4 (PIN 16 HIGH) AND INJECTS A SMALL CHARGE AT THE C+ PIN (PIN 16 LOW). THIS BOOSTS THE CMRR WHEN THE LTC1043 IS USED AS AN INSTRUMENTATION AMPLIFIER FRONT END.

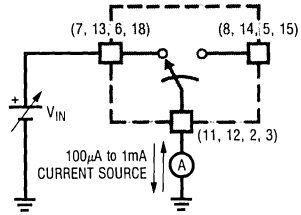
FOR MINIMUM CHARGE INJECTION IN OTHER TYPES OF APPLICATIONS, S3A AND S3B SHOULD BE GROUNDED.

TEST CIRCUITS

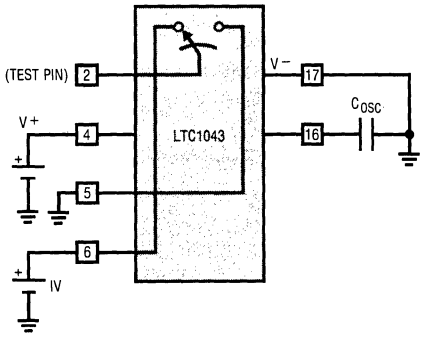


NOTE: TO OPEN SWITCHES S1 AND S3 SHOULD BE CONNECTED to V– TO OPEN S2, S4, C_{OSC} PIN SHOULD BE TO V+. C_{OSC}

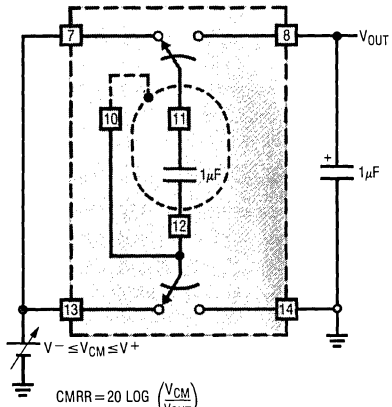
Test Circuit 1. Leakage Current Test



Test Circuit 2. R_{ON} Test



Test Circuit 3. Oscillator Frequency, f_{OSC}



$$CMRR = 20 \log \left(\frac{V_{CM}}{V_{OUT}}\right)$$

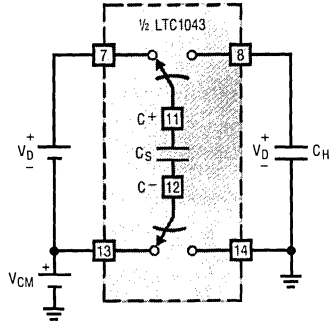
NOTE: FOR OPTIMUM CMRR, THE C_{OSC} SHOULD BE LARGER THAN 0.0047μF, AND THE SAMPLING CAPACITOR ACROSS PINS 11 AND 12 SHOULD BE PLACED OVER A SHIELD TIED TO PIN 10.

Test Circuit 4. CMRR Test

APPLICATIONS INFORMATION

Common-Mode Rejection Ratio (CMRR)

The LTC1043, when used as a differential to single-ended converter (Figure 1) rejects common-mode signals and preserves differential voltages. Unlike other techniques, the LTC1043's CMRR does not degrade with increasing common-mode voltage frequency. During the sampling mode, the impedance of pins 2, 3 (and 11, 12) should be reasonably balanced, otherwise, common-mode signals will appear differentially. The value of the CMRR depends on the value of the sampling and holding capacitors (C_S, C_H) and on the sampling frequency. Since the common-mode voltages are not sampled, the common-mode signal frequency can well exceed the sampling frequency without experiencing aliasing phenomena. The CMRR of Figure 1



C_S, C_H ARE MYLAR OR POLYSTYRENE

Figure 1. Differential to Single-Ended Converter

APPLICATIONS INFORMATION

is measured by shorting pins 7 and 13 and by observing, with a precision DVM, the change of the voltage across C_H with respect to an input CM voltage variation. During the sampling and holding mode, charges are being transferred and minute voltage transients will appear across the holding capacitor. Although the R_{ON} on the switches is low enough to allow fast settling, as the sampling frequency increases, the rate of charge transfer increases and the average voltage measured with a DVM across it will increase proportionally; this causes the CMRR of the sampled data system, as seen by a "continuous" instrument (DVM), to decrease, Figure 2.

Switch Charge Injection

Figure 3 shows one out of the eight switches of the LTC1043, configured as a basic sample and hold circuit. When the switch opens, a "hold step" is observed and its magnitude depends on the value of the input voltage. Figure 4 shows charge injected into the hold capacitor. For instance, a 2pCb of charge injected into a 0.01μF capacitor causes a 200μV hold step. As shown in Figure 4, there is a predictable and repeatable charge injection cancellation when the input voltage is close to half the supply voltage of the LTC1043. This is a unique feature of this product, containing charge-balanced switches fabricated with a self-aligning gate CMOS process. Any switch of the LTC1043, when powered with symmetrical dual supplies, will sample and hold small signals around ground without any significant error.

Shielding the Sampling Capacitor for Very High CMRR

Internal or external parasitic capacitors from the C^+ pin(s) to ground affect the CMRR of the LTC1043, (Figure 1). The common-mode error due to the internal junction capacitances of the C^+ pin(s) 2 and 11 is cancelled through internal circuitry. The C^+ pin, therefore, should be used as the top plate of the sampling capacitor. The interpin capacitance between pin 2 and dummy pin 1 (11 and 10) appears in parallel with the sampling capacitor so it does not degrade the CMRR. A shield placed underneath the sampling capacitor (Figure 5) and connected to either pin 1 or 3 helps to boost the CMRR in excess of 120dB.

Excessive external parasitic capacitance between the C^- pins and ground indirectly degrades CMRR; this becomes visible especially when the LTC1043 is used with clock frequencies above 2kHz. Because of this, if a shield is used, the parasitic capacitance between the shield and circuit ground should be minimized.

It is recommended that the outer plate of the sampling capacitor be connected to the C^- pin(s).

Input Pins, SCR Sensitivity

An internal 60Ω resistor is connected in series with the input of the switches (pins 5, 6, 7, 8, 13, 14, 15, 18) and it is included in the R_{ON} specification. When the input voltage exceeds the power supply by a diode drop, current will flow into the input pin(s). The LTC1043 will not

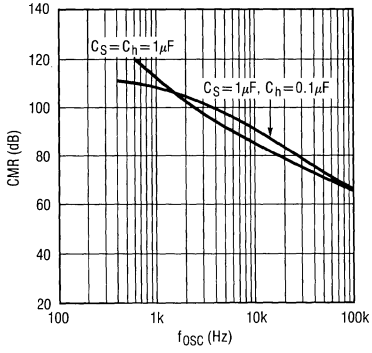


Figure 2. CMRR vs Sampling Frequency

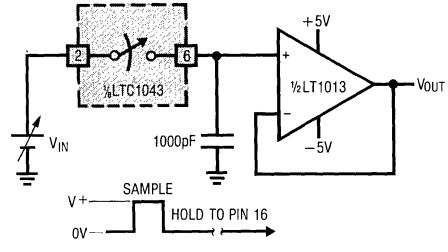


Figure 3

APPLICATIONS INFORMATION

latch until the input current reaches 2mA–3mA. The device will recover from the latch mode when the input drops 3V–4V below the voltage value which caused the latch. For instance, if an external resistor of 200Ω is connected in series with an input pin, the input can be taken 1.3V above the supply without latching the IC. The same applies for the C^+ and C^- pins.

C_{OSC} Pin (16), Figure 6

The C_{OSC} pin can be used with an external capacitor, C_{OSC}, connected from pin 16 to pin 17, to modify the internal oscillator frequency. If pin 16 is floating, the internal 24pF capacitor plus any external interpin capacitance set the oscillator frequency around 190kHz with ±5V supply. The typical performance characteristics curves provide the necessary information to set the oscillator frequency for various power supply ranges. Pin 16 can also be driven with an external clock to override the internal oscillator. Although standard 7400 series CMOS gates do not guarantee CMOS levels with the current source and sink requirements of pin 16, they will in reality drive the C_{OSC} pin. CMOS gates conforming to standard B series output drive have the appropriate voltage levels and more than enough output current to simultaneously drive several LTC1043 C_{OSC} pins. The typical trip levels of the Schmitt trigger, Figure 6, are given below.

SUPPLY	TRIP LEVELS	
$V^+ = 5V$, $V^- = 0V$	$V_H = 3.4V$	$V_L = 1.35V$
$V^+ = 10V$, $V^- = 0V$	$V_H = 6.5V$	$V_L = 2.8V$
$V^+ = 15V$, $V^- = 0V$	$V_H = 9.5V$	$V_L = 4.1V$

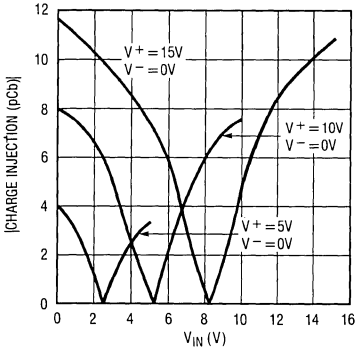


Figure 4. Individual Switch Charge Injection vs Input Voltage

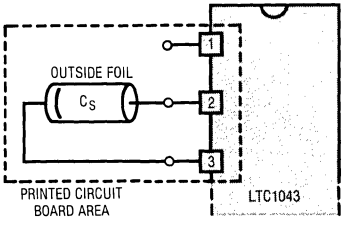
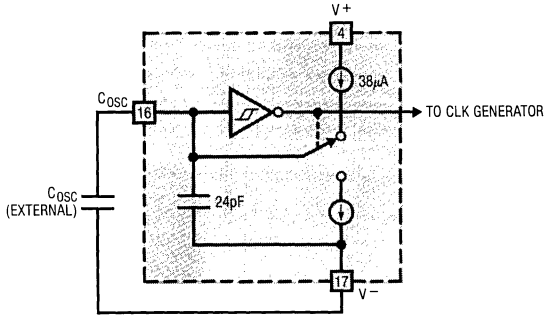


Figure 5. Printed Circuit Board Layout Showing Shielding the Sampling Capacitor

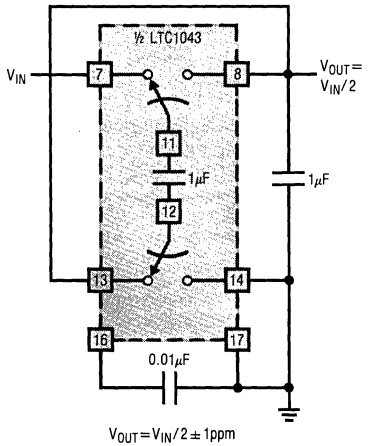


$$f_{OSC} \simeq 190kHz \times \frac{(24pF)}{(24pF + C_{OSC})}$$

Figure 6. Internal Oscillator

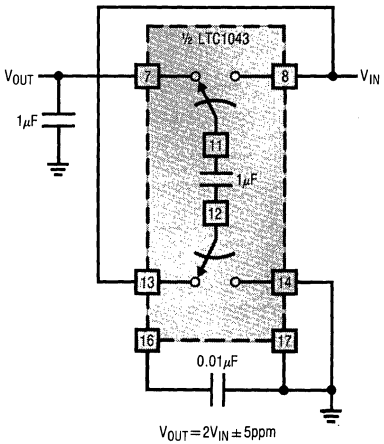
APPLICATIONS

Divide by 2



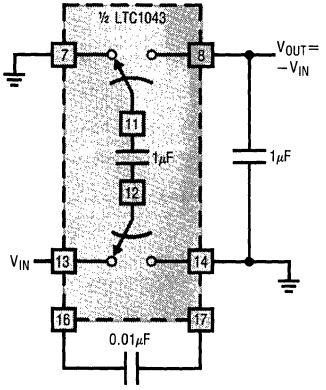
$V_{OUT} = V_{IN}/2 \pm 1ppm$
$0 \le V_{IN} \le V^+$
$3 \le V^+ \le 18V$

Multiply by 2



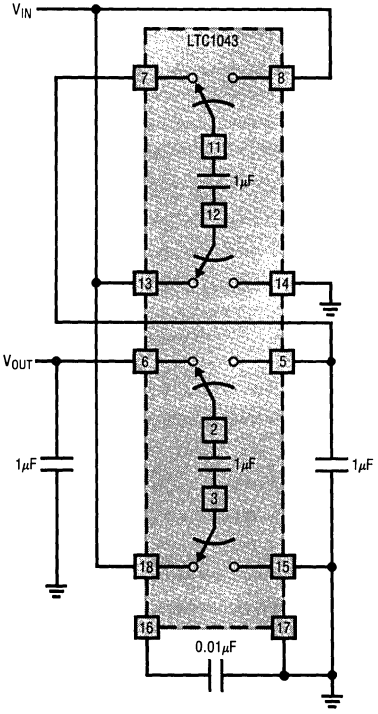
$V_{OUT} = 2V_{IN} \pm 5ppm$
$0 \le V_{IN} < V^+/2$
$3 \le V^+ \le 18V$

Ultra Precision Voltage Inverter



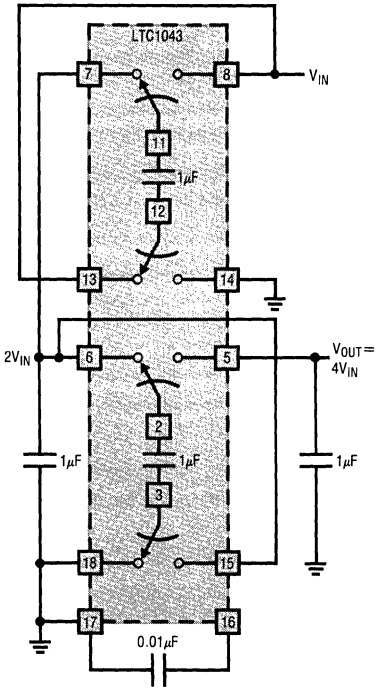
$V_{OUT} = -V_{IN} \pm 2ppm$
$V^- < V_{IN} < V^+$
$V^+ = +5V, V^- = -5V$

Precision Multiply by 3



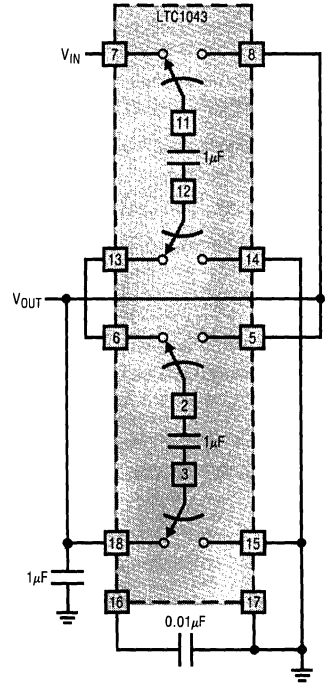
$V_{OUT} = 3V_{IN} \pm 10ppm$
$0 < V_{IN} < V^+/3$
$3V < V^+ < 18V$

Precision Multiply by 4



$V_{OUT} = 4V_{IN} \pm 40ppm$
$0 \le V_{IN} \le V^+/4$
$3V < V^+ < 18V$

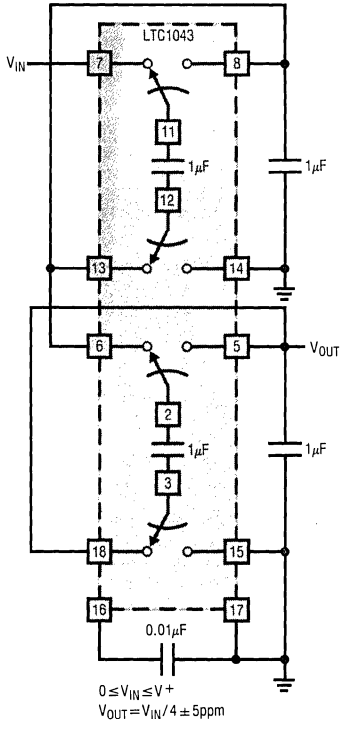
Divide by 3



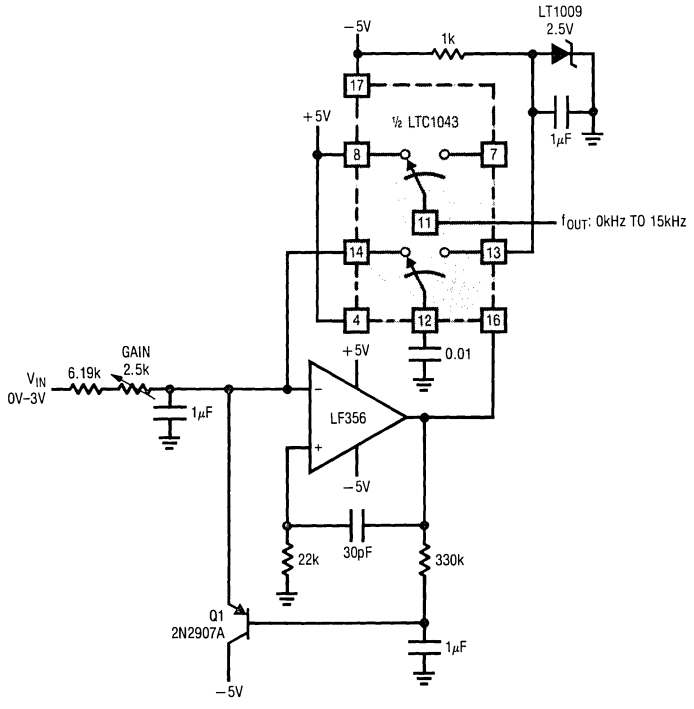
$V_{OUT} = V_{IN}/3 \pm 3ppm$
$0 \le V_{IN} \le V^+$

APPLICATIONS

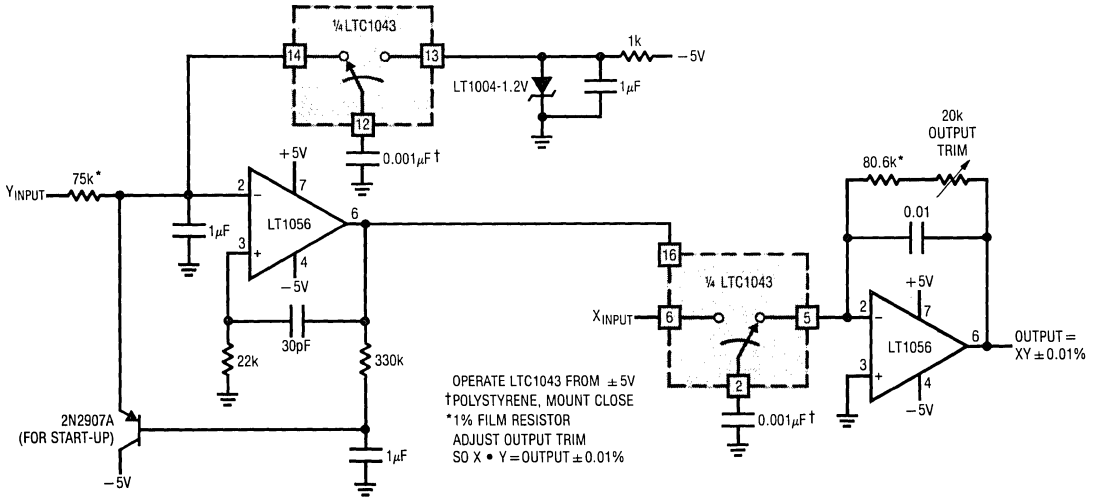
Divide by 4



0.005% V → F Converter

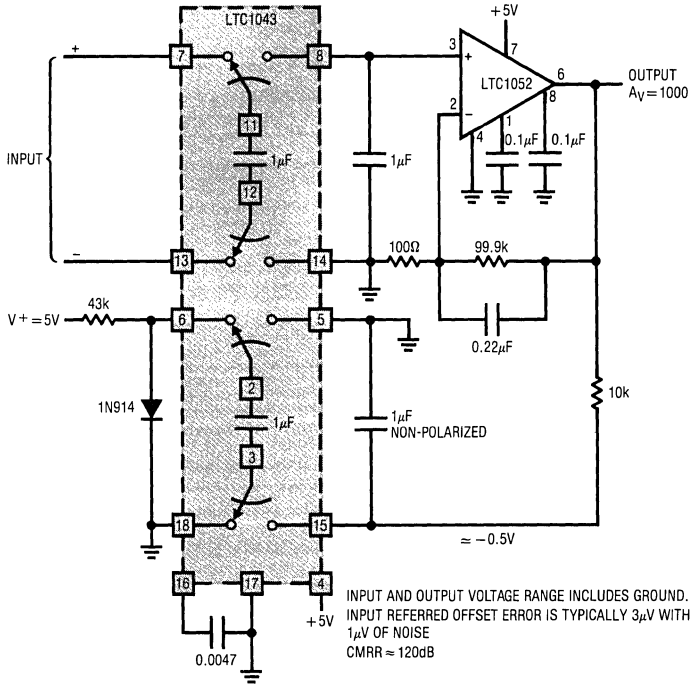


0.01% Analog Multiplier

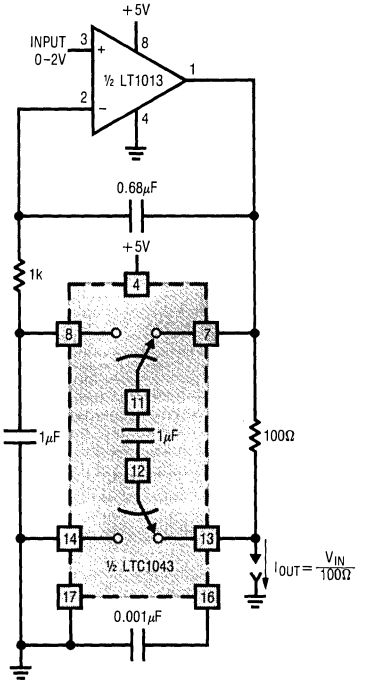


APPLICATIONS

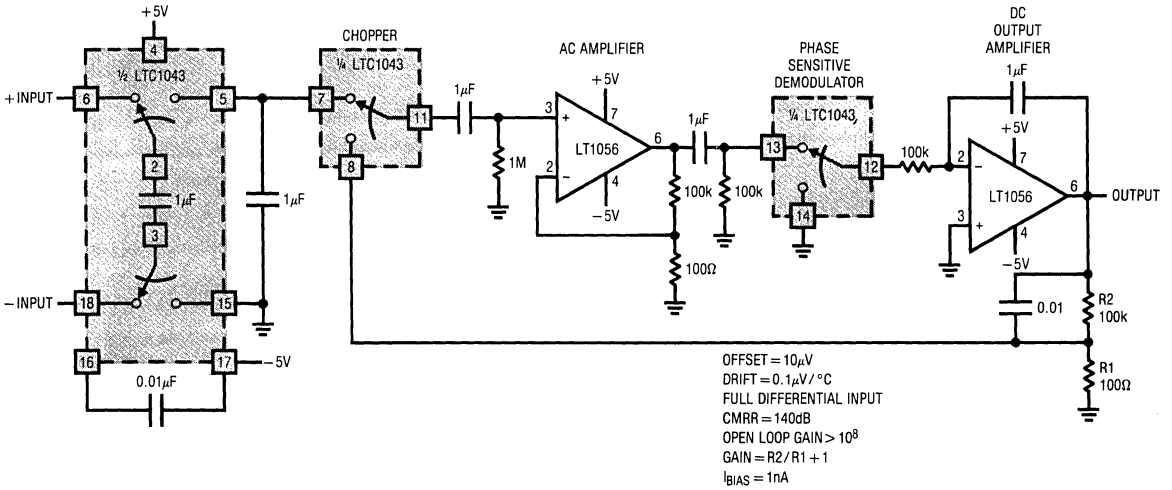
Single 5V Supply, Ultra Precision Instrumentation Amplifier



Voltage Controlled Current Source with Ground Referred Input and Output

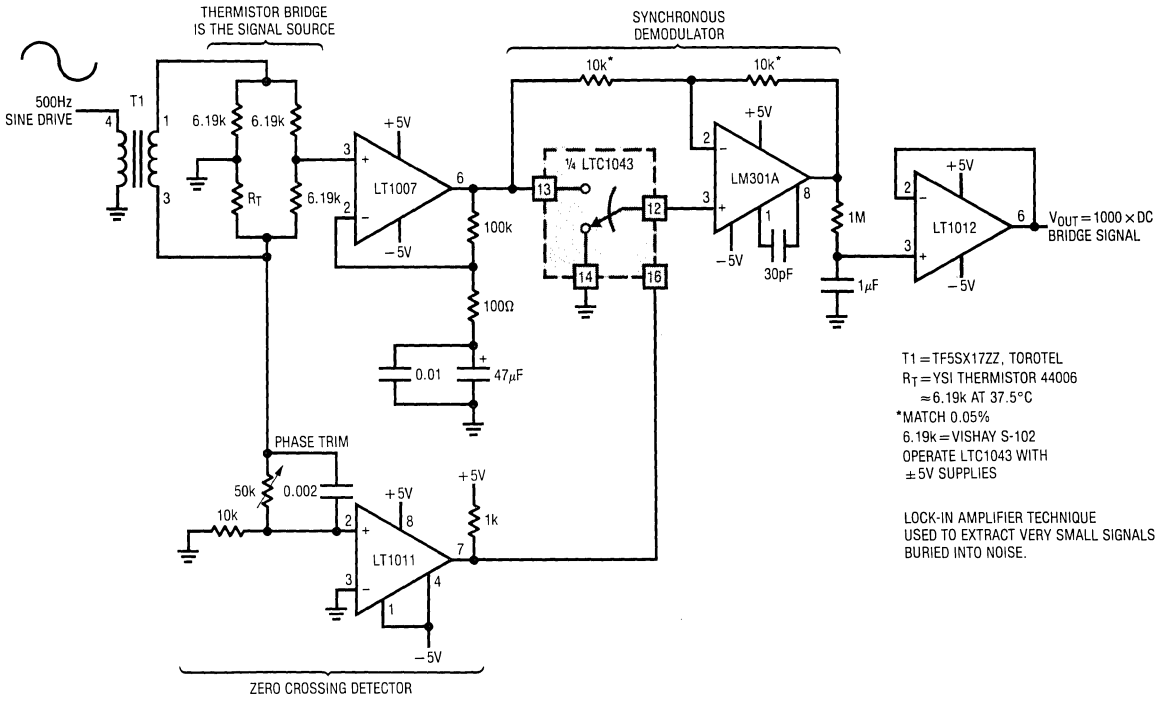


Precision Instrumentation Amplifier

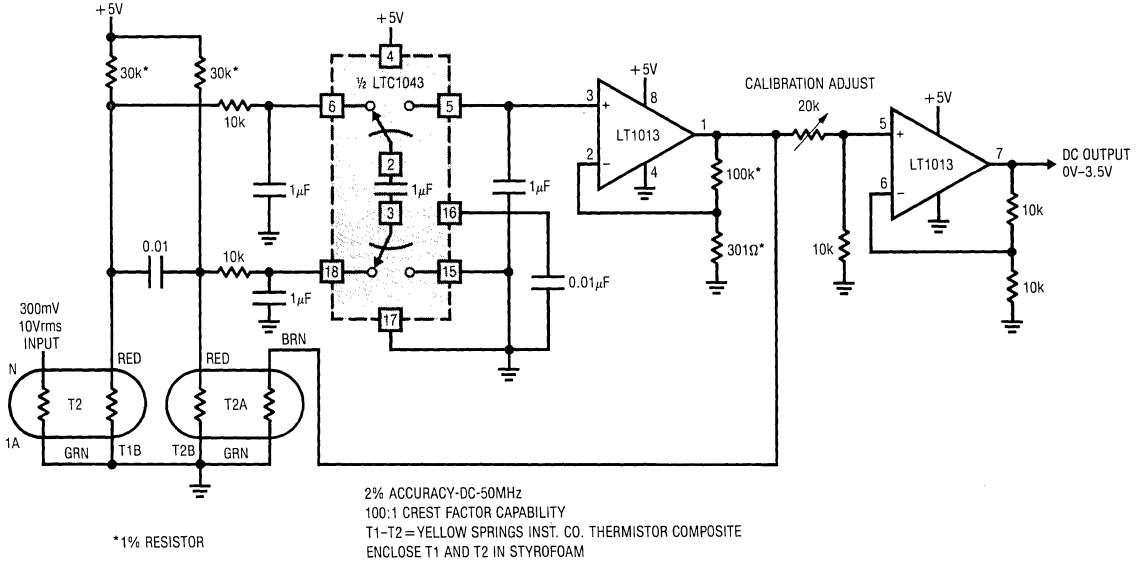


APPLICATIONS

Lock-In Amplifier (= Extremely Narrow-Band Amplifier)

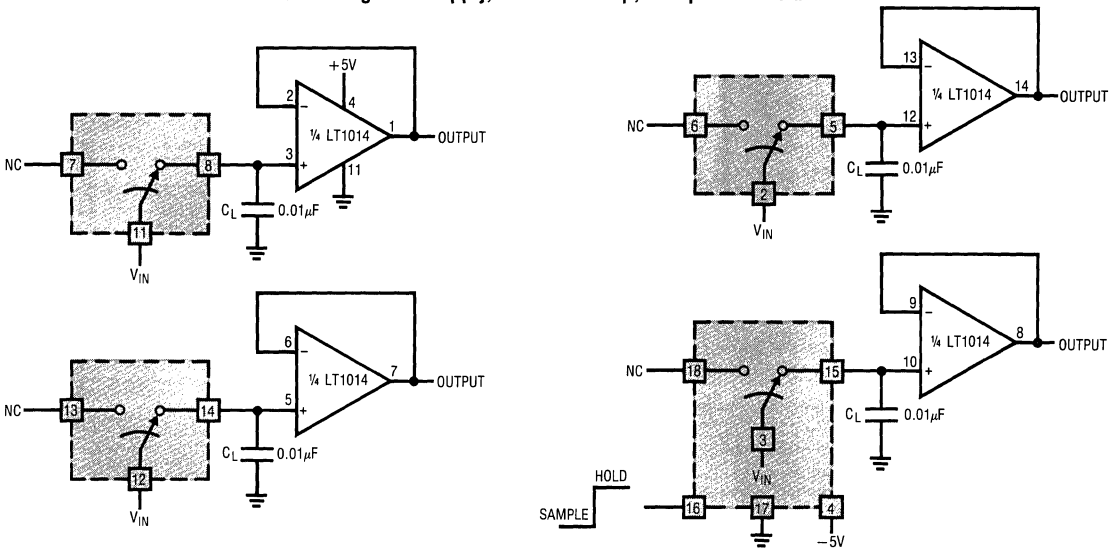


50MHz Thermal rms → DC Converter



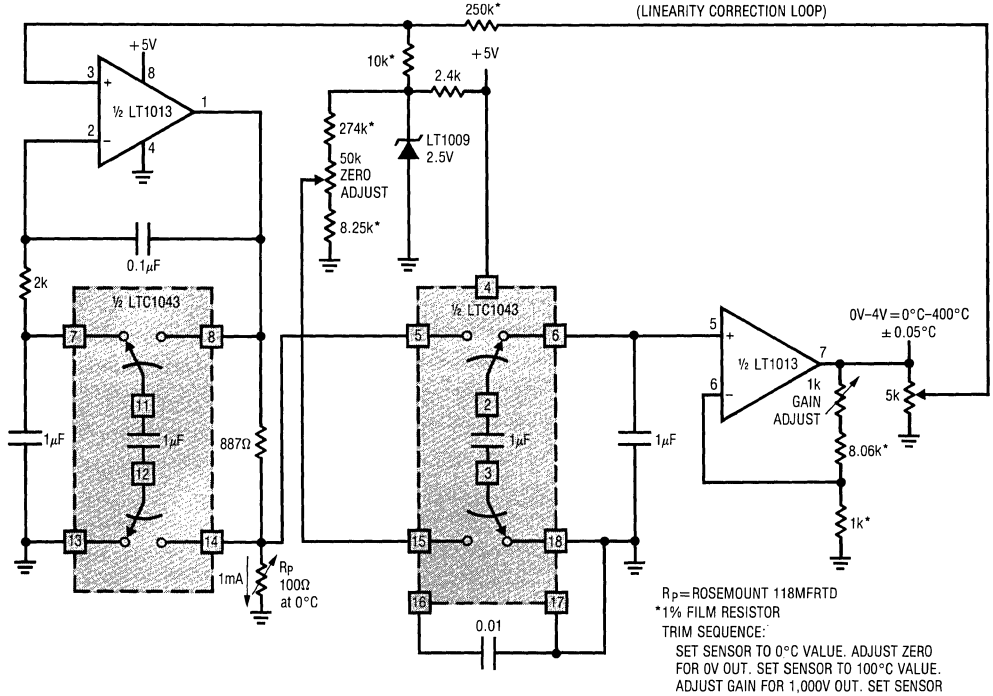
APPLICATIONS

Quad Single 5V Supply, Low Hold Step, Sample and Hold



FOR $1V \leq V_{IN} \leq 4V$, THE HOLD STEP IS $\leq 300\mu V$.
ACQUISITION TIME $\sim 8 \times R_{ON} C_H$ FOR 10-BIT ACCURACY.

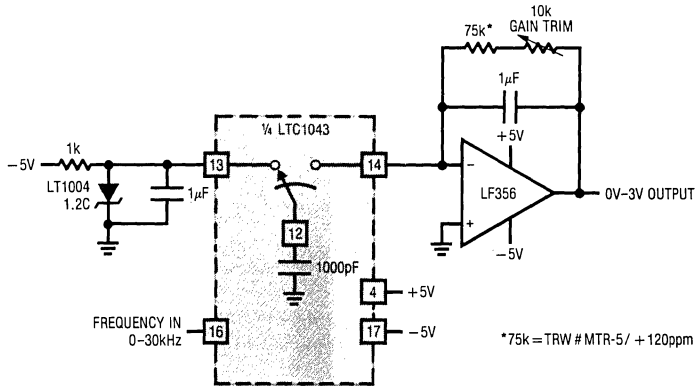
Single Supply Precision Linearized Platinum RTD Signal Conditioner



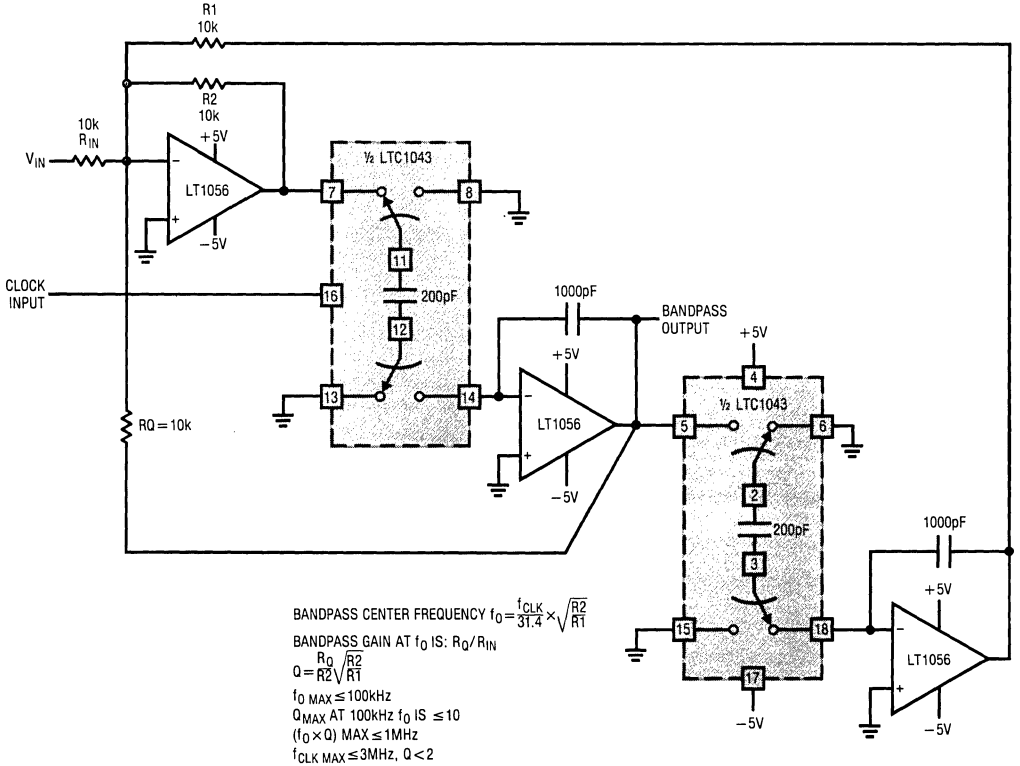
R_P = ROSEMOUNT 118MFRTD
*1% FILM RESISTOR
TRIM SEQUENCE:
SET SENSOR TO 0°C VALUE. ADJUST ZERO FOR 0V OUT. SET SENSOR TO 100°C VALUE. ADJUST GAIN FOR 1,000V OUT. SET SENSOR TO 400°C VALUE. ADJUST LINEARITY FOR 4.000V OUT. REPEAT AS REQUIRED.

APPLICATIONS

0.005%F ⟶ V Converter



High Frequency Clock Tunable Bandpass Filter



BANDPASS CENTER FREQUENCY $f_0 = \frac{f_{CLK}}{31.4} \times \sqrt{\frac{R2}{R1}}$

BANDPASS GAIN AT f_0 IS: R_Q/R_{IN}

$Q = \frac{R_Q}{R2}\sqrt{\frac{R2}{R1}}$

$f_{0\ MAX} \leq 100kHz$

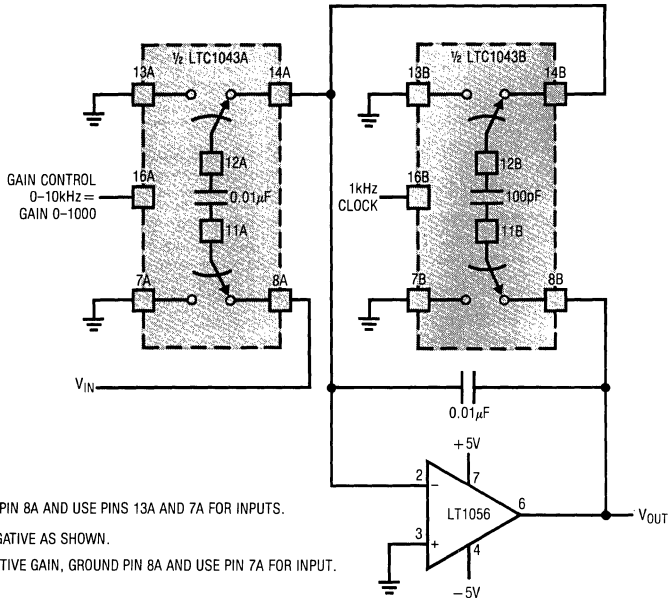
Q_{MAX} AT 100kHz f_0 IS ≤ 10

$(f_0 \times Q)\ MAX \leq 1MHz$

$f_{CLK\ MAX} \leq 3MHz,\ Q < 2$

APPLICATIONS

Frequency-Controlled Gain Amplifier



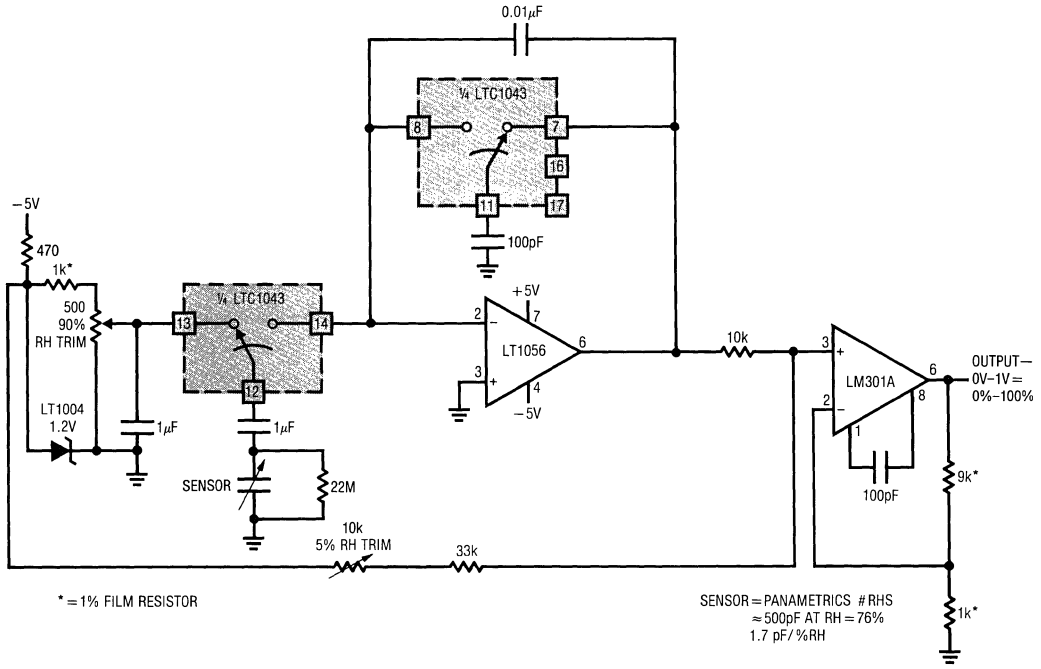
FOR DIFFERENTIAL INPUT, GROUND PIN 8A AND USE PINS 13A AND 7A FOR INPUTS.

$GAIN = \frac{f_{IN} \times 0.01\mu F}{1kHz \times 100pF}$; GAIN IS NEGATIVE AS SHOWN.

FOR SINGLE-ENDED INPUT AND POSITIVE GAIN, GROUND PIN 8A AND USE PIN 7A FOR INPUT.

USE ±5V SUPPLIES FOR LTC1043.

Relative Humidity Sensor Signal Conditioner

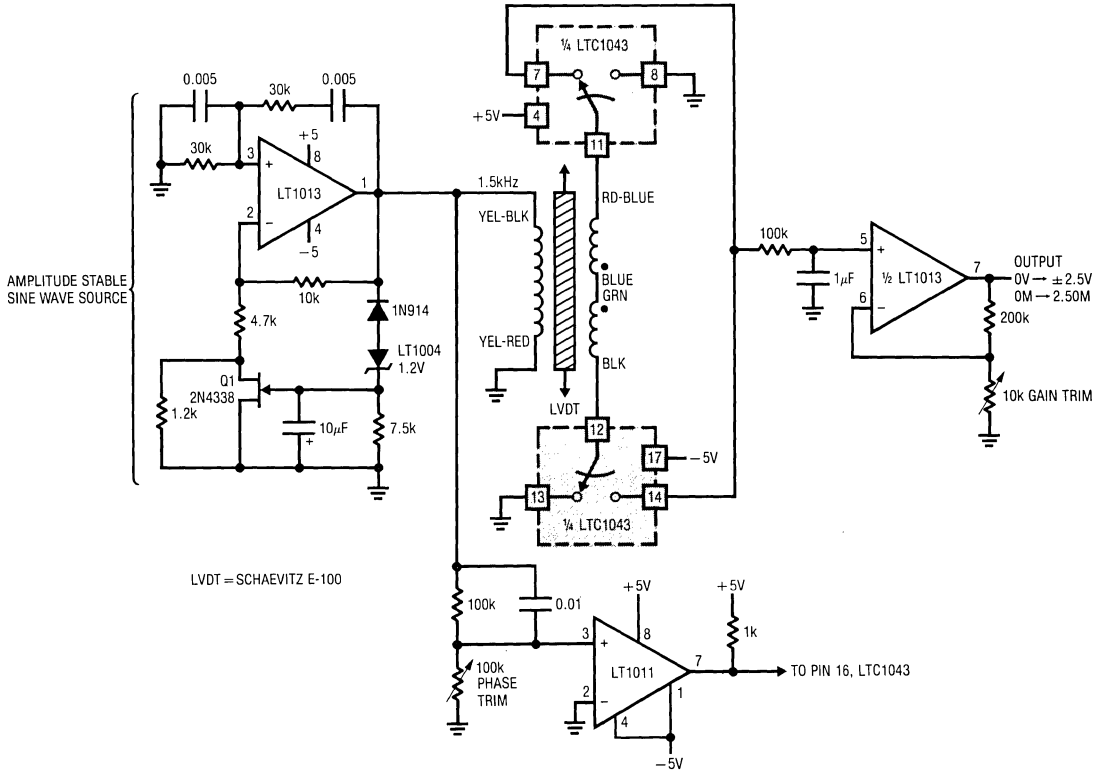


* = 1% FILM RESISTOR

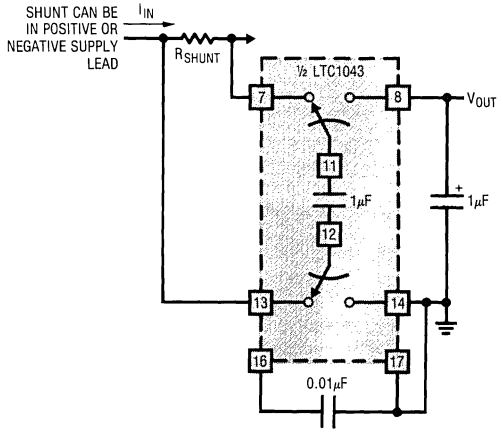
SENSOR = PANAMETRICS # RHS
≈ 500pF AT RH = 76%
1.7 pF/%RH

APPLICATIONS

Linear Variable Differential Transformer (LVDT), Signal Conditioner

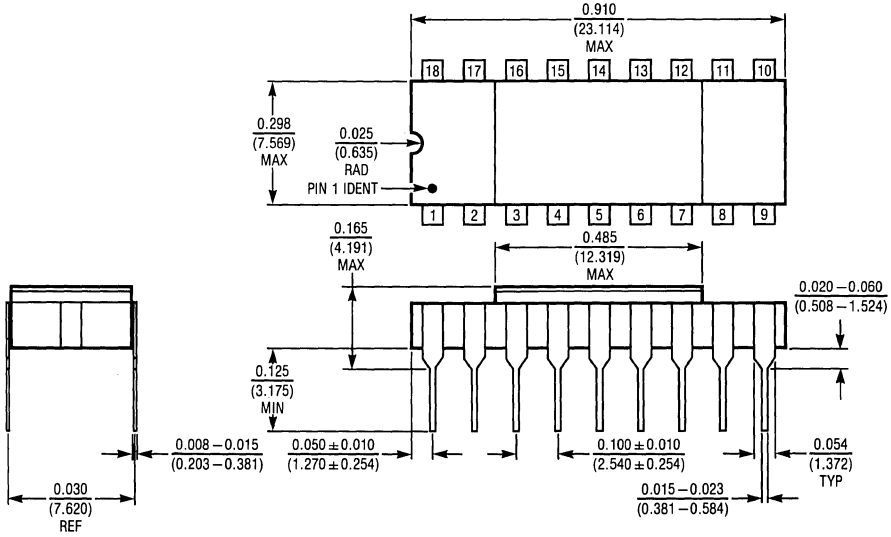


Precision Current Sensing in Supply Rails



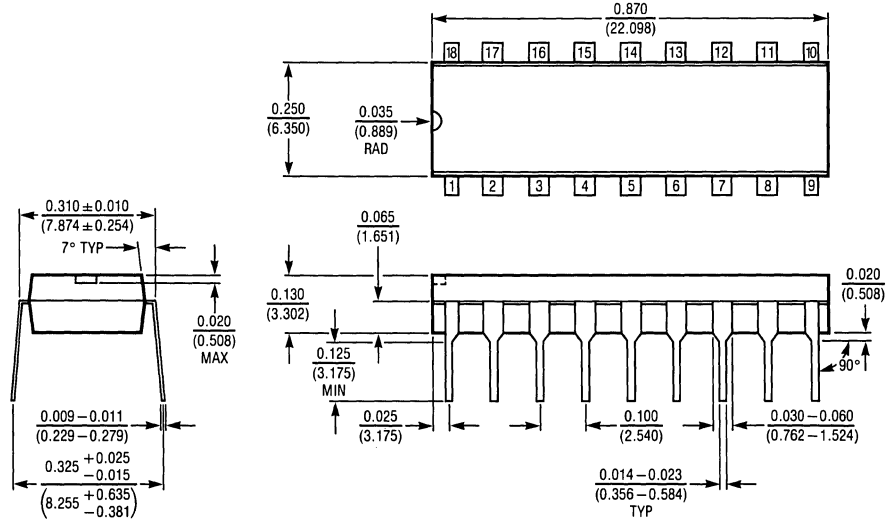
PACKAGE DESCRIPTION Dimensions in inches (millimeters) unless otherwise noted.

D Package
18 Lead Side Brazed



	T_{jmax}	Θ_{ja}
LTC1043MD	150°C	100°C/W
LTC1043CD	150°C	100°C/W

N Package
18 Lead Plastic DIP



	T_{jmax}	Θ_{ja}
LTC1043CN	100°C	100°C/W

Switched Capacitor Voltage Converter

FEATURES

- Plug-In Compatible with 7660 with These Additional Features:
  - *Guaranteed* Operation to 9V, with No External Diode, Over Full Temperature Range
  - Boost Pin (Pin 1) for Higher Switching Frequency
  - Lower Quiescent Power
  - Efficient Voltage Doubler
- 200μA *Max.* No Load Supply Current at 5V
- 97% *Min.* Open Circuit Voltage Conversion Efficiency
- 95% *Min.* Power Conversion Efficiency
- Wide Operating Supply Voltage Range, 1.5V to 9V
- Easy to Use
- Commercial Device *Guaranteed* Over −40°C to 85°C Temperature Range

APPLICATIONS

- Conversion of +5V to ±5V Supplies
- Precise Voltage Division, $V_{OUT} = V_{IN}/2 \pm 20ppm$
- Voltage Multiplication, $V_{OUT} = \pm nV_{IN}$
- Supply Splitter, $V_{OUT} = \pm V_S/2$

DESCRIPTION

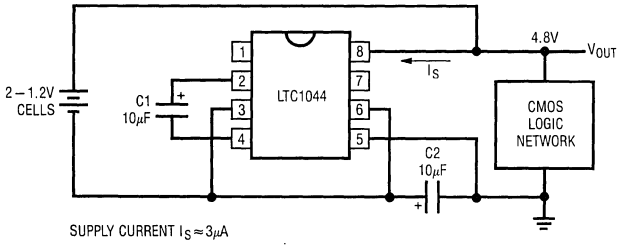
The LTC1044 is a monolithic CMOS switched capacitor voltage converter which is manufactured using Linear Technology's enhanced LTCMOS™ silicon gate process. The LTC1044 provides several voltage conversion functions: the input voltage can be inverted ($V_{OUT} = -V_{IN}$), doubled ($V_{OUT} = 2V_{IN}$), divided ($V_{OUT} = V_{IN}/2$) or multiplied ($V_{OUT} = \pm nV_{IN}$).

Designed to be pin-for-pin and functionally compatible with the popular 7660, the LTC1044 provides significant features and improvements over earlier 7660 designs. These improvements include: full 1.5V to 9V supply operation over the entire operating temperature range, without the need for external protection diodes; 2½ times lower quiescent current for greater power conversion efficiency; and a "boost" function which is available to raise the internal oscillator frequency to optimize performance in specific applications.

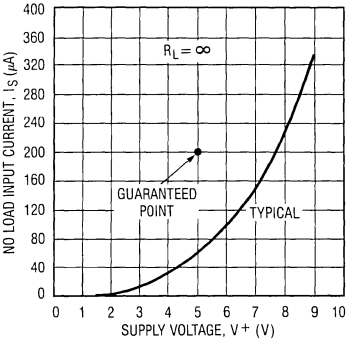
Although the LTC1044 provides significant design and performance advantages over the earlier 7660 device, it still maintains its compatibility with existing 7660 designs.

LTCMOS™ is a trademark of Linear Technology Corp.

Generating CMOS Logic Supply from 2 Mercury Batteries



Supply Current vs Supply Voltage

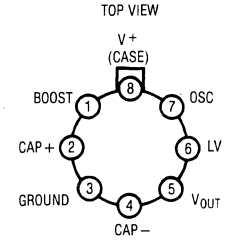


ABSOLUTE MAXIMUM RATINGS

(Notes 1 and 2)

Supply Voltage 9.5V
Input Voltage on Pins 1, 6 and 7
(Note 2) ..... $-0.3V \leq V_{IN} \leq V^+ + 0.3V$
Current into Pin 6 ..... 20μA
Output Short Circuit Duration
($V^+ \leq 5.5V$) ..... Continuous
Operating Temperature Range
LTC1044C ..... $-40°C \leq T_A \leq 85°C$
LTC1044M ..... $-55°C \leq T_A \leq 125°C$
Storage Temperature Range ..... $-65°C$ to $+150°C$
Lead Temperature (Soldering, 10 sec.) ..... 300°C

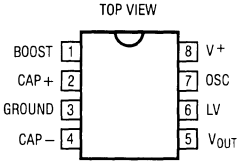
PACKAGE/ORDER INFORMATION



METAL CAN H PACKAGE

ORDER PART NUMBER

LTC1044CH
LTC1044MH



HERMETIC DIP J8 PACKAGE
PLASTIC DIP N8 PACKAGE

LTC1044CJ8
LTC1044CN8
LTC1044MJ8

ELECTRICAL CHARACTERISTICS

$V^+ = 5V$, $T_A = 25°C$, Test Circuit Figure 1, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		LTC1044M MIN	LTC1044M TYP	LTC1044M MAX	LTC1044C MIN	LTC1044C TYP	LTC1044C MAX	UNITS
I_S	Supply Current	$R_L = \infty$, Pins 1 and 7 No Connection			60	200		60	200	μA
		$R_L = \infty$, Pins 1 and 7 $V^+ = 3V$			20			20		μA
V^+_L	Minimum Supply Voltage	$R_L = 10k$	●	1.5			1.5			V
V^+_H	Maximum Supply Voltage	$R_L = 10k$ (Note 3)	●			9			9	V
R_{OUT}	Output Resistance	$I_L = 20mA$, $f_{OSC} = 5kHz$				100			100	Ω
			●			150			130	Ω
		$V^+ = 2V$, $I_L = 3mA$, $f_{OSC} = 1kHz$	●			400			325	Ω
f_{OSC}	Oscillator Frequency	$C_{OSC} = 1pF$ (Note 4)								
		$V^+ = 5V$	●	5			5			kHz
		$V^+ = 2V$	●	1			1			kHz
P_{EFF}	Power Efficiency	$R_L = 5k\Omega$, $f_{OSC} = 5kHz$		95	98		95	98		%
V_{OUTEFF}	Voltage Conversion Efficiency	$R_L = \infty$		97	99.9		97	99.9		%
I_{OSC}	Oscillator Sink or Source Current	$V_{OSC} = 0V$ or V^+								
		Pin 1 = 0V	●			3			3	μA
		Pin 1 = V^+	●			20			20	μA

The ● denotes the specifications which apply over the full operating temperature range.

Note 1: Absolute Maximum Ratings are those values beyond which the life of the device may be impaired.

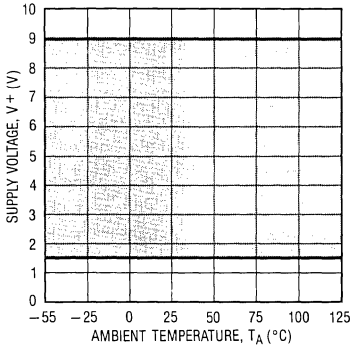
Note 2: Connecting any input terminal to voltages greater than V^+ or less than ground may cause destructive latch-up. It is recommended that no inputs from sources operating from external supplies be applied prior to power-up of the LTC1044.

Note 3: The LTC1044 is guaranteed to operate with alkaline, mercury or NiCad 9V batteries, even though the initial battery voltage may be slightly higher than 9.0V.

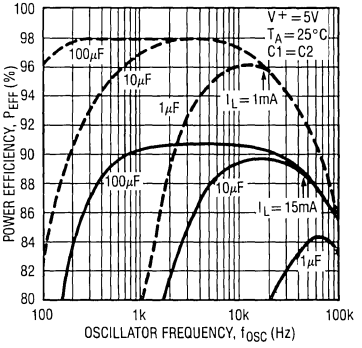
Note 4: f_{OSC} is tested with $C_{OSC} = 100pF$ to minimize the effects of test fixture capacitance loading. The 1pF frequency is correlated to this 100pF test point, and is intended to simulate the capacitance at pin 7 when the device is plugged into a test socket and no external capacitor is used.

TYPICAL PERFORMANCE CHARACTERISTICS (Using Test Circuit Shown in Figure 1)

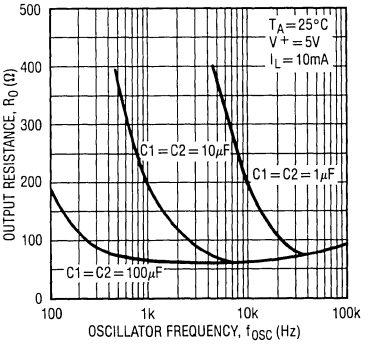
Operating Voltage Range vs Temperature



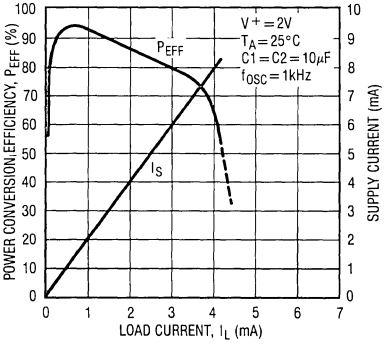
Power Efficiency vs Oscillator Frequency



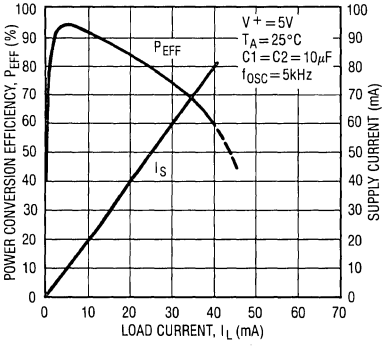
Output Resistance vs Oscillator Frequency



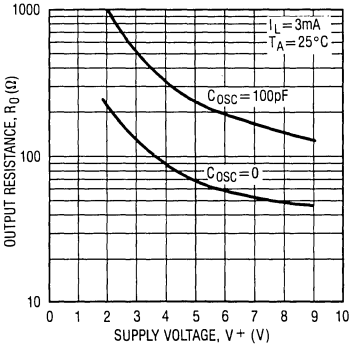
Power Conversion Efficiency vs Load Current for V+ = 2V



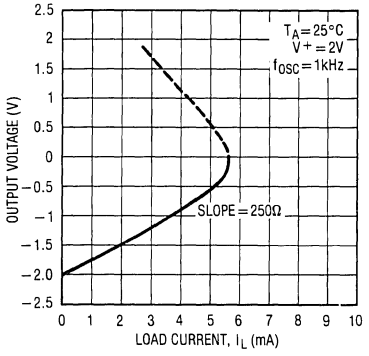
Power Conversion Efficiency vs Load Current for V+ = 5V



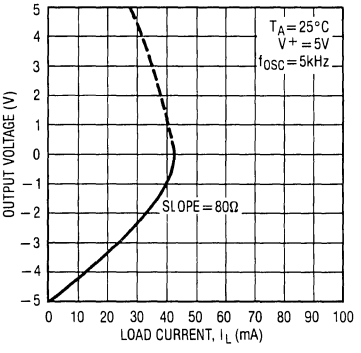
Output Resistance vs Supply Voltage



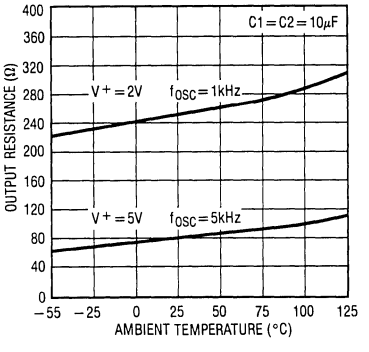
Output Voltage vs Load Current for V+ = 2V



Output Voltage vs Load Current for V+ = 5V

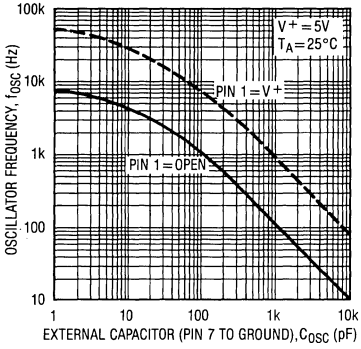


Output Resistance vs Temperature

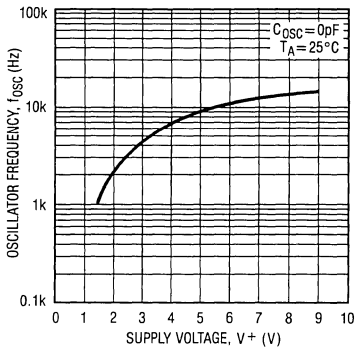


TYPICAL PERFORMANCE CHARACTERISTICS (Using Test Circuit Shown in Figure 1)

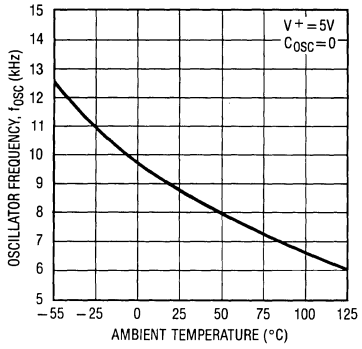
Oscillator Frequency as a Function of C_{OSC}



Oscillator Frequency vs Supply Voltage



Oscillator Frequency vs Temperature



TEST CIRCUIT

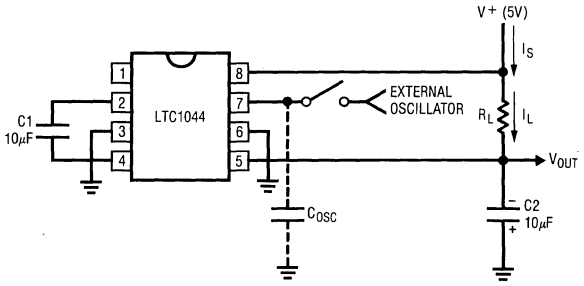


Figure 1

APPLICATIONS INFORMATION

Theory of Operation

To understand the theory of operation of the LTC1044, a review of a basic switched capacitor building block is helpful.

In Figure 2, when the switch is in the left position, capacitor C1 will charge to voltage V1. The total charge on C1 will be q1 = C1V1. The switch then moves to the right, discharging C1 to voltage V2. After this discharge time, the charge on C1 is q2 = C1V2. Note that charge has been transferred from the source, V1, to the output, V2. The amount of charge transferred is:

$$\Delta q = q1 - q2 = C1(V1 - V2).$$

If the switch is cycled f times per second, the charge transfer per unit time (i.e., current) is:

$$I = f \times \Delta q = f \times C1(V1 - V2).$$

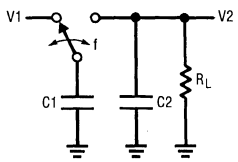


Figure 2. Switched Capacitor Building Block

APPLICATIONS INFORMATION

Rewriting in terms of voltage and impedance equivalence,

$$I = \frac{V1 - V2}{(1/fC1)} = \frac{V1 - V2}{R_{EQUIV}}.$$

A new variable, R_{EQUIV}, has been defined such that $R_{EQUIV} = 1/fC1$. Thus, the equivalent circuit for the switched capacitor network is as shown in Figure 3.

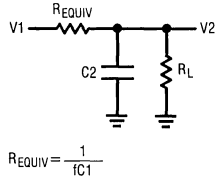


Figure 3. Switched Capacitor Equivalent Circuit

Examination of Figure 4 shows that the LTC1044 has the same switching action as the basic switched capacitor building block. With the addition of finite switch on-resistance and output voltage ripple, the simple theory, although not exact, provides an intuitive feel for how the device works.

For example, if you examine power conversion efficiency as a function of frequency (see typical curve), this simple theory will explain how the LTC1044 behaves. The loss, and hence the efficiency, is set by the output impedance. As frequency is decreased, the output impedance will eventually be dominated by the 1/fC1 term and power efficiency will drop. The typical curves for power efficiency versus frequency show this effect for various capacitor values.

Note also that power efficiency decreases as frequency goes up. This is caused by internal switching losses which occur due to some finite charge being lost on each switching cycle. This charge loss per unit cycle, when multiplied by the switching frequency, becomes a current loss. At high frequency this loss becomes significant and the power efficiency starts to decrease.

LV (Pin 6)

The internal logic of the LTC1044 runs between V^+ and LV (pin 6). For V^+ greater than or equal to 3V, an internal switch shorts LV to GND (pin 3). For V^+ less than 3V, the LV pin should be tied to GND. For V^+ greater than or equal to 3V, the LV pin can be tied to GND or left floating.

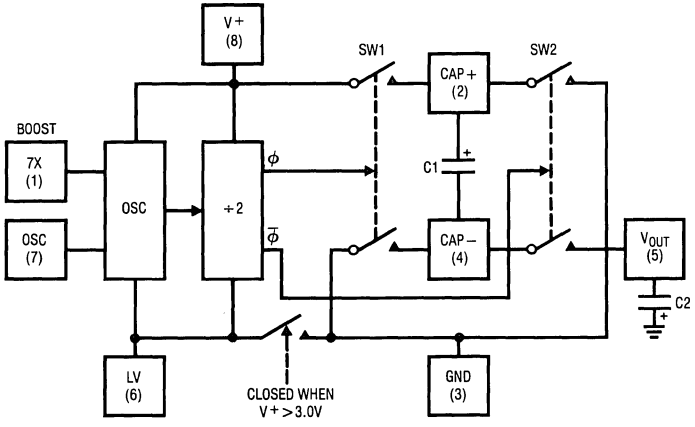


Figure 4. LTC1044 Switched Capacitor Voltage Converter Block Diagram

APPLICATIONS INFORMATION

OSC (Pin 7) and Boost (Pin 1)

The switching frequency can be raised, lowered or driven from an external source. Figure 5 shows a functional diagram of the oscillator circuit.

By connecting the boost pin (pin 1) to V^+, the charge and discharge current is increased and, hence, the frequency is increased by approximately 7 times. Increasing the frequency will decrease output impedance and ripple for higher load currents.

Loading pin 7 with more capacitance will lower the frequency. Using the boost (pin 1) in conjunction with external capacitance on pin 7 allows user selection of the frequency over a wide range.

Driving the LTC1044 from an external frequency source can be easily achieved by driving pin 7 and leaving the boost pin open, as shown in Figure 6. The output current from pin 7 is small, typically 0.5μA, so a logic gate is capable of driving this current. The choice of using a CMOS logic gate is best because it can operate over a wide supply voltage range (3V to 15V) and has enough voltage swing to drive the internal Schmitt trigger shown in Figure 5. For 5V applications, a TTL logic gate can be used by simply adding an external pull-up resistor (see Figure 6).

External Diode (D_X)

Previous circuits of this type have required a diode between V_{OUT} (pin 5) and the external capacitor, C2, for voltages above 6.5V (5V for military temperature range). Because of improvements which have been made in the LTC1044 circuit design and Linear Technology's silicon gate CMOS process, this diode is no longer required. The LTC1044 will operate from 1.5V to 9V, without the protection diode, over all temperature ranges.

It should, however, be noted that the LTC1044 will operate without any problems in existing 7660 designs which use the protection diode, as long as the maximum operating voltage (V^+) of 9V is not exceeded.

Capacitor Selection

External capacitors C1 and C2 are not critical. Matching is not required, nor do they have to be high quality or tight tolerance. Aluminum or tantalum electrolytics are excellent choices, with cost and size being the only consideration.

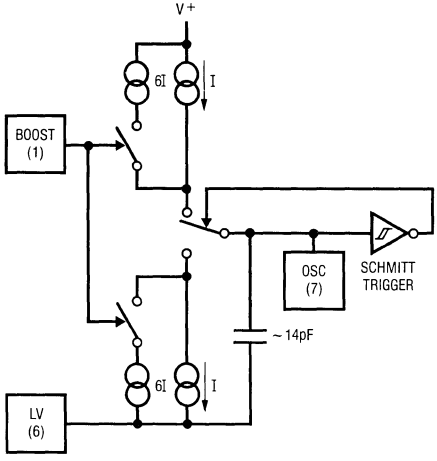


Figure 5. Oscillator

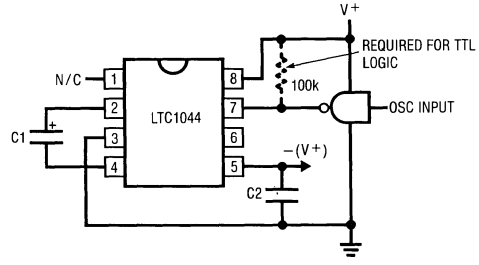


Figure 6. External Clocking

TYPICAL APPLICATIONS

Negative Voltage Converter

Figure 7 shows a typical connection which will provide a negative supply from an available positive supply. This circuit operates over full temperature and power supply ranges *without* the need of any external diodes. The LV pin (pin 6) is shown grounded, but for $V^+ \geq 3V$ it may be "floated", since LV is internally switched to ground (pin 3) for $V^+ \geq 3V$.

The output voltage (pin 5) characteristics of the circuit are those of a nearly ideal voltage source in series with an 80Ω resistor. The 80Ω output impedance is composed of two terms: 1) the equivalent switched capacitor resistance (see Theory of Operation) and 2) a term related to the on-resistance of the MOS switches.

At an oscillator frequency of 10kHz and $C1 = 10\mu F$, the first term is:

$$R_{EQUIV} = \frac{1}{(f_{OSC}/2) \times C1} =$$

$$\frac{1}{5 \times 10^3 \times 10 \times 10^{-6}} = 20\Omega.$$

Notice that the above equation for R_{EQUIV} is *not* a capacitive reactance equation ($X_C = 1/\omega C$) and does not contain a 2π term.

The exact expression for output impedance is extremely complex, but the dominant effect of the capacitor is clearly shown on the typical curves of output impedance and power efficiency versus frequency. For $C1 = C2 = 10\mu F$, the output impedance goes from 60Ω at $f_{OSC} = 10kHz$ to 200Ω at $f_{OSC} = 1kHz$. As the $1/fC$ term becomes large compared to the switch on-resistance term, the output resistance is determined by $1/fC$ only.

Voltage Doubling

Figure 8 shows two methods of voltage doubling. In Figure 8a doubling is achieved by simply rearranging the connection of the two external capacitors. When the input voltage is less than 3V, an external 1MΩ resistor is required to ensure the oscillator will start. It is not required for higher input voltages.

In this application the ground input (pin 3) is taken above V^+ (pin 8) during turn-on, making it prone to latch-up. The latch-up is not destructive but simply prevents the circuit from doubling. Resistor R1 is added to eliminate the problem. In most cases 200Ω is sufficient. It may be necessary in a particular application to increase this value to guarantee start-up.

The voltage drop across R1 is : $V_{R1} = 2 \times I_{OUT} \times R1$. If this voltage exceeds two diode drops (1.4V for silicon, 0.8V for Schottky), the circuit in Figure 8a is recommended. This circuit will never have a start-up problem.

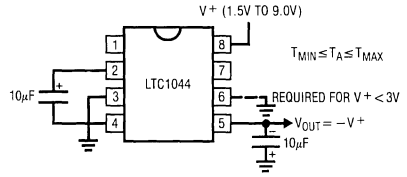


Figure 7. Negative Voltage Converter

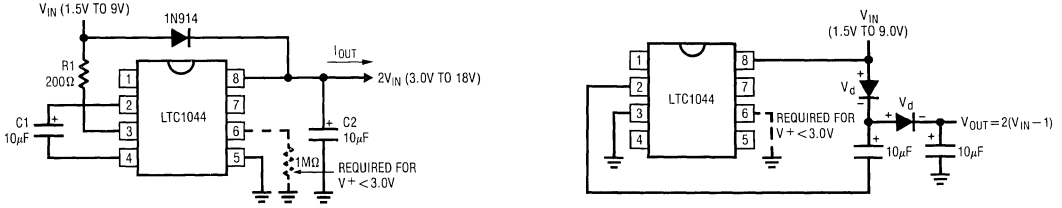


Figure 8. Voltage Doubler

TYPICAL APPLICATIONS

Ultra Precision Voltage Divider

An ultra precision voltage divider is shown in Figure 9. To achieve the 0.0002% accuracy indicated, the load current should be kept below 100nA. However, with a slight loss in accuracy, the load current can be increased.

Battery Splitter

A common need in many systems is to obtain (+) and (−) supplies from a single battery or single power supply system. Where current requirements are small, the circuit shown in Figure 10 is a simple solution. It provides symmetrical ± output voltages, both equal to one half the input voltage. The output voltages are both referenced to pin 3 (output common). If the input voltage between pin 8 and pin 5 is less than 6V, pin 6 should also be connected to pin 3, as shown by the dashed line.

Paralleling for Lower Output Resistance

Additional flexibility of the LTC1044 is shown in Figures 11, 12 and 13.

Figure 11 shows two LTC1044s connected in parallel to provide a lower effective output resistance. If, however, the output resistance is dominated by 1/fC1, increasing the capacitor size (C1) or increasing the frequency will be of more benefit than the paralleling circuit shown.

Figures 12 and 13 make use of "stacking" two LTC1044s to provide even higher voltages. In Figure 12, a negative voltage doubler or tripler can be achieved, depending upon how pin 8 of the second LTC1044 is connected, as shown schematically by the switch. Figure 13 indicates a similar circuit which can be used to obtain positive tripling, or even quadrupling (the doubler circuit appears in Figure 8a. In both of these circuits, the available output current will be dictated/decreased by the product of the individual power conversion efficiencies and the voltage step-up ratio.

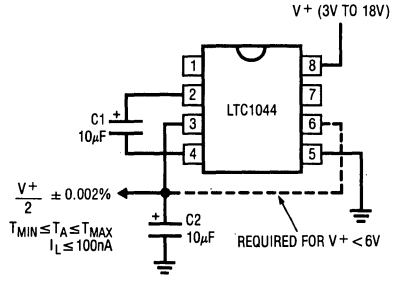


Figure 9. Ultra Precision Voltage Divider

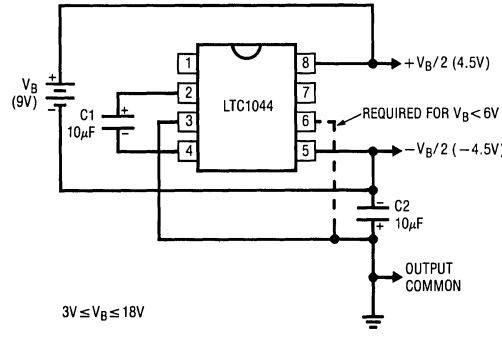
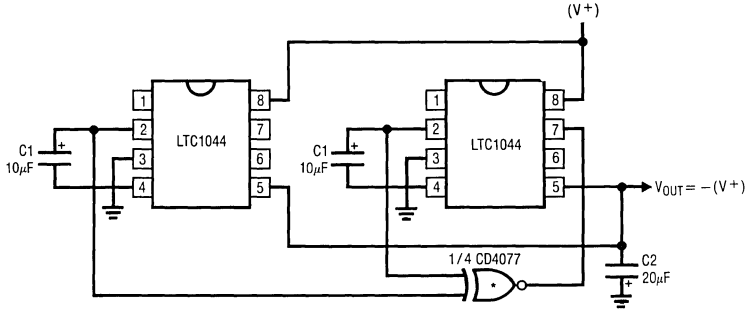


Figure 10. Battery Splitter

TYPICAL APPLICATIONS



*THE EXCLUSIVE NOR GATE SYNCHRONIZES BOTH LTC1044s TO MINIMIZE RIPPLE

Figure 11. Paralleling for Lower Output Resistance

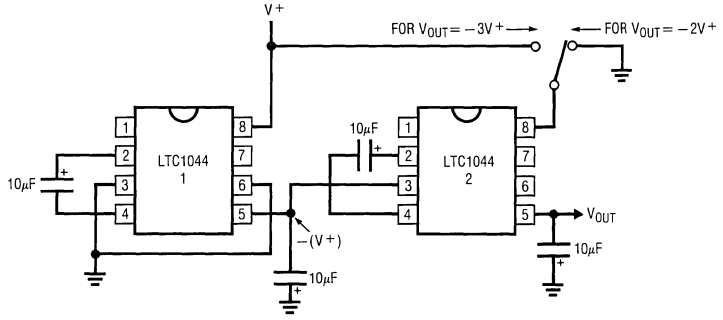
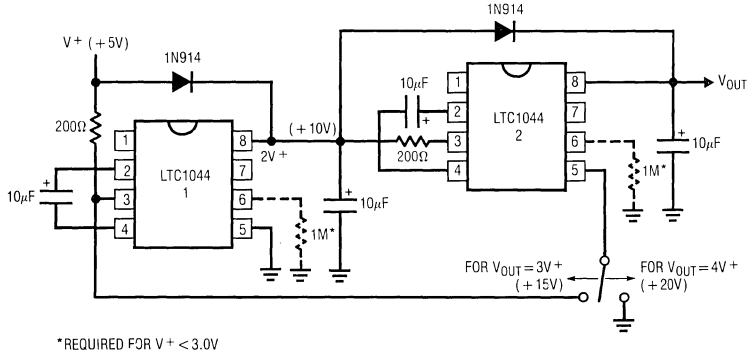


Figure 12. Stacking for Higher Voltage



*REQUIRED FOR V+ < 3.0V

Figure 13. Voltage Tripler/Quadrupler

TYPICAL APPLICATIONS

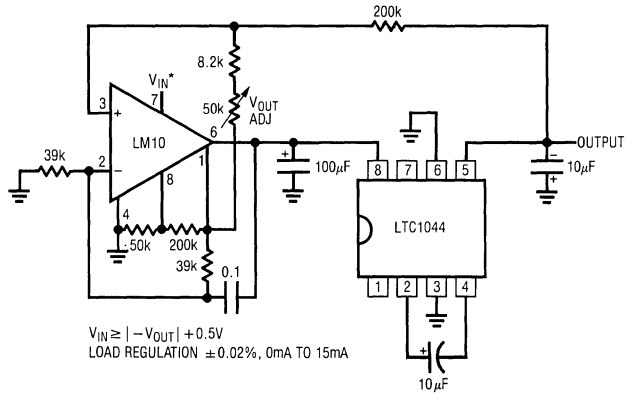


Figure 14. Low Output Impedance Voltage Converter

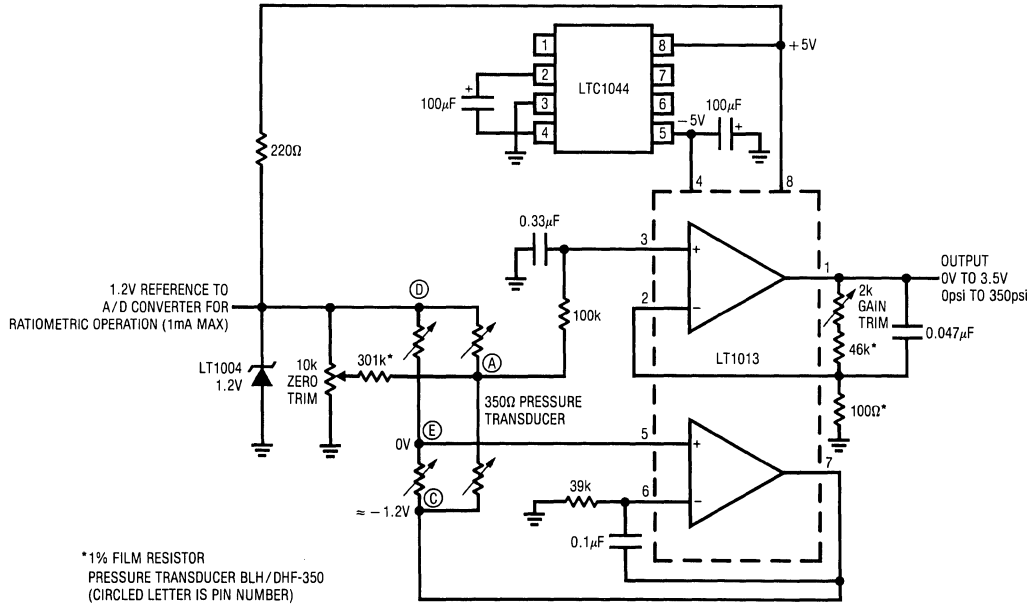


Figure 15. Single 5V Strain Gauge Bridge Signal Conditioner

TYPICAL APPLICATIONS

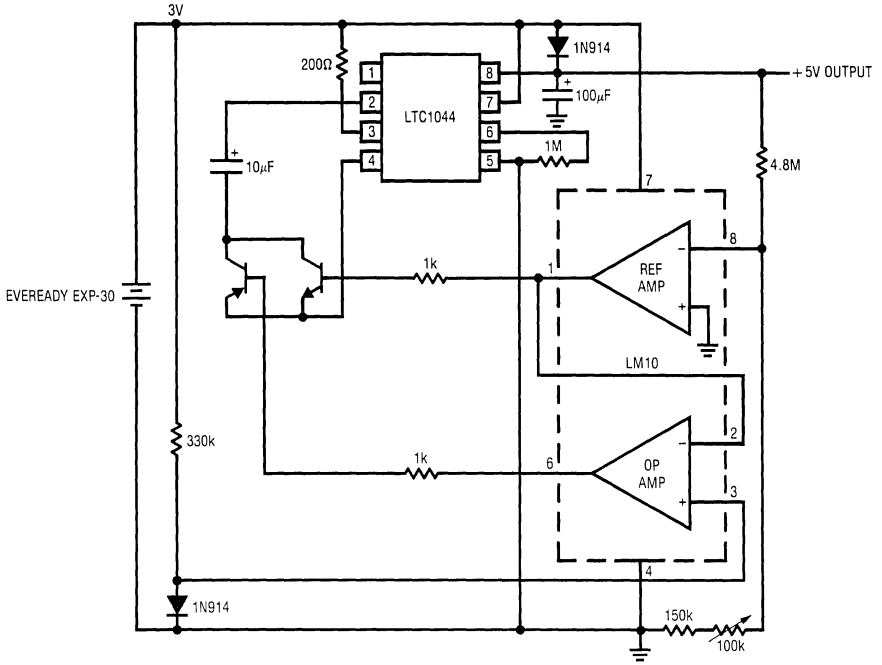


Figure 16. Regulated Output +3V to +5V Converter

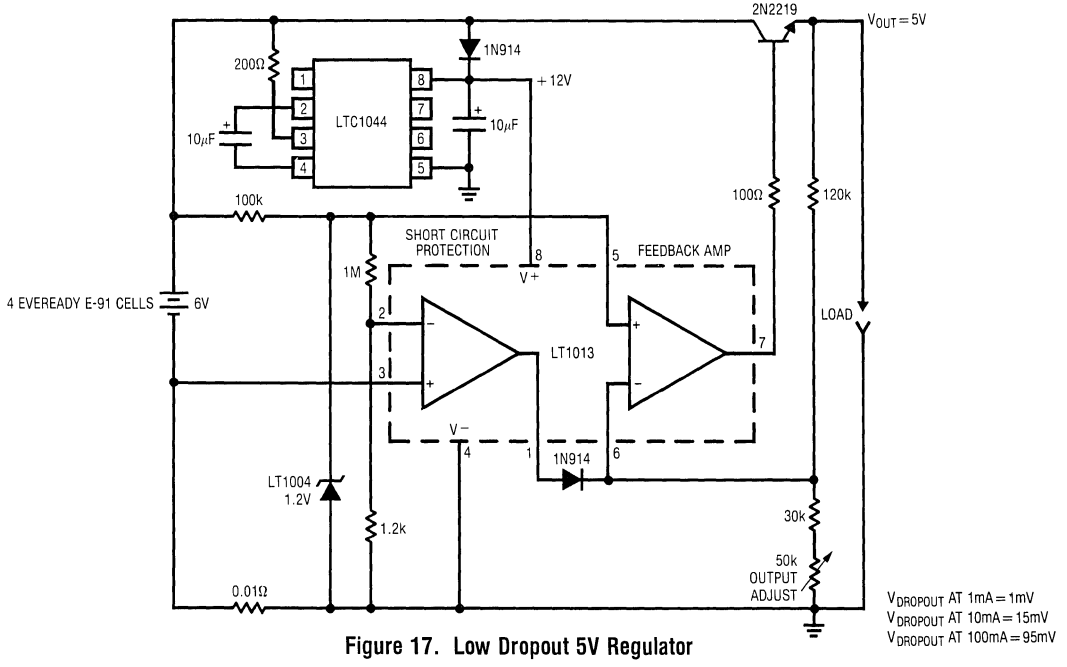
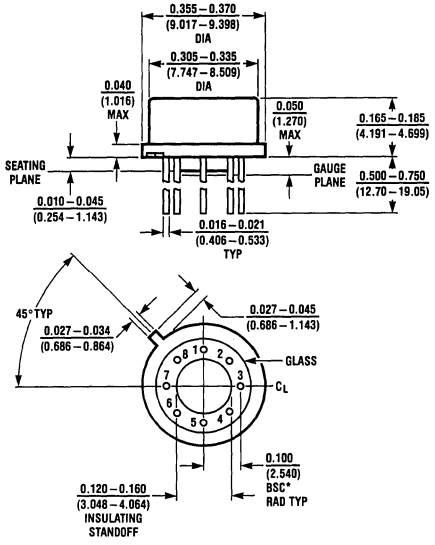


Figure 17. Low Dropout 5V Regulator

PACKAGE DESCRIPTION

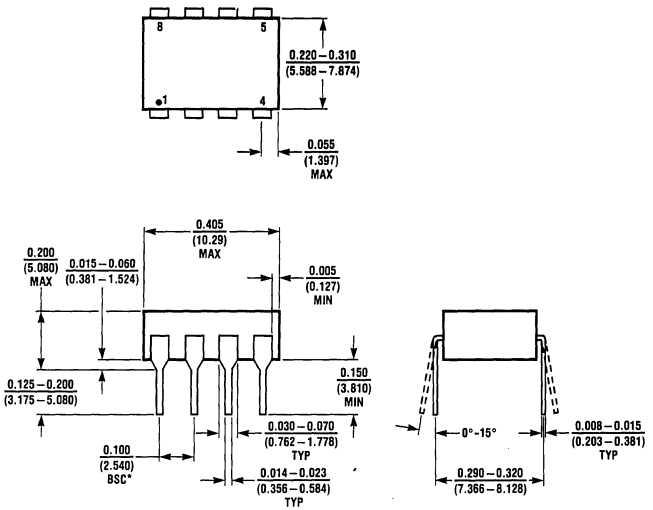
H Package
Metal Can



NOTE: DIMENSIONS IN INCHES (MILLIMETERS)

$T_j$max	θ_{ja}	θ_{jc}
150°C	150°C/W	45°C/W

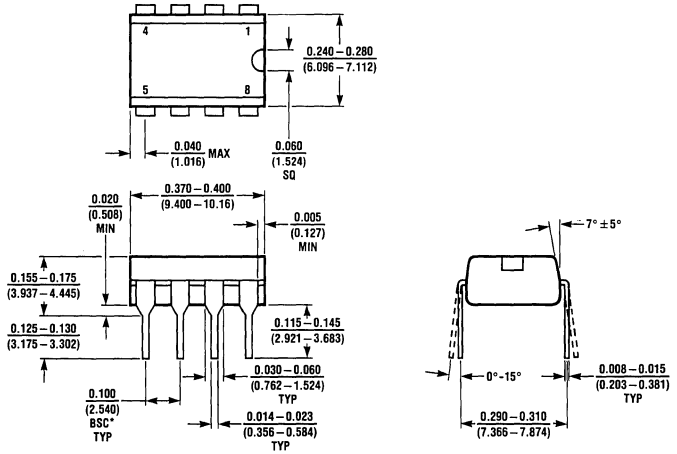
J8 Package
8 Lead Hermetic DIP



NOTE: DIMENSIONS IN INCHES (MILLIMETERS) UNLESS OTHERWISE NOTED
*LEADS WITHIN 0.007 OF TRUE POSITION (TP) AT GAUGE PLANE

$T_j$max	θ_{ja}
150°C	100°C/W

N8 Package
8 Lead Plastic



NOTE: DIMENSIONS IN INCHES (MILLIMETERS) UNLESS OTHERWISE NOTED
*LEADS WITHIN 0.007 OF TRUE POSITION (TP) AT GAUGE PLANE

$T_j$max	θ_{ja}
100°C	130°C/W

Precision Sample and Hold Amplifier

FEATURES

- *Guaranteed* 6μs Max. Acquisition Time
- *Guaranteed* 0.005% Max. Gain Error
- *Guaranteed* 1mV Max. Offset Voltage
- *Guaranteed* 1mV Max. Hold Step
- Very Low Feedthrough 86dB Min.
- High Input Impedance under All Conditions
- Logic Inputs Compatible with All Logic Families

APPLICATIONS

- 12-Bit Data Acquisition Systems
- Ramp Generators
- Analog Switches
- Staircase Generators
- Sample and Difference Circuits

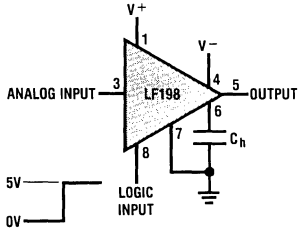
DESCRIPTION

The LF198 is a precision sample and hold amplifier which uses a combination of bipolar and junction FET transistors to provide precision, high speed, and long hold times. A typical offset voltage of 1mV and gain error of 0.002% allow this sample and hold amplifier to be used in 12-bit systems. Dynamic performance can be optimized by proper selection of the external hold capacitor. Acquisition times can be as low as 4μs for small capacitors while hold step and droop errors can be held below 0.1mV and 30μV/sec respectively when using larger capacitors.

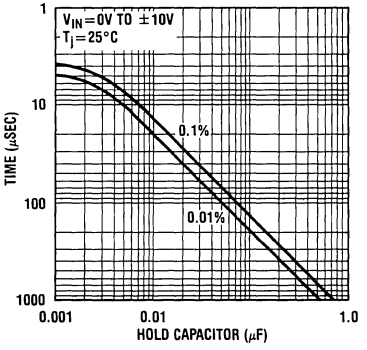
The LF198 is fixed at unity gain with $10^{10}\Omega$ input impedance independent of sample/hold mode. The logic inputs are high impedance differential to allow easy interfacing to any logic family without ground loop problems. A separate offset adjust pin can be used to zero the offset voltage in either the sample or hold mode. Additionally, the hold capacitor can be driven with an external signal to provide precision level shifting or "differencing" operation. The device will operate over a wide supply voltage range from ±5V to ±18V with very little change in performance, and key parameters are specified over this full supply range.

The LF198A version offers tightened electrical specifications for key parameters.

Basic Sample and Hold



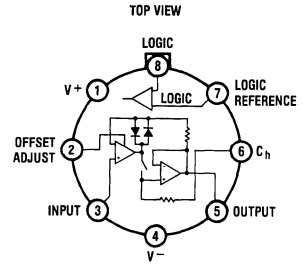
Acquisition Time



ABSOLUTE MAXIMUM RATINGS

Input Voltage ..... Equal to Supply Voltage
Logic to Logic Reference Differential
Voltage (Note 2) ..... +30V, −30V
Output Short Circuit Duration ..... Indefinite
Hold Capacitor Short Circuit Duration ..... 10 sec
Lead Temperature (Soldering, 10 seconds) ..... 300°C
Supply Voltage ..... ±18V
Power Dissipation (Package Limitation)
(Note 1) 500mW
Operating Temperature Range
LF198/LF198A ..... −55°C to 125°C
LF398/LF398A ..... 0°C to 70°C
Storage Temperature Range ..... −65°C to 150°C

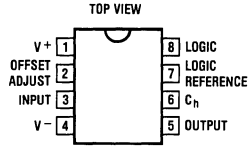
PACKAGE/ORDER INFORMATION



H PACKAGE
METAL CAN

ORDER PART NUMBER

LF198AH
LF198H
LF398AH
LF398H



J8 PACKAGE HERMETIC DIP
N8 PACKAGE
PLASTIC DUAL IN LINE

LF398J8
LF398AN8
LF398N8

ELECTRICAL CHARACTERISTICS (Note 3)

PARAMETER	CONDITIONS		LF198A MIN	LF198A TYP	LF198A MAX	LF398A MIN	LF398A TYP	LF398A MAX	UNITS
Input Offset Voltage (Note 6)				0.5	1		1	2	mV
		●			2			3	mV
Input Bias Current (Note 6)				5	25		10	25	nA
		●			75			50	nA
Input Impedance				10^{10}			10^{10}		Ω
Gain Error	R_L=10k			0.001	0.005		0.001	0.005	%
		●			0.01			0.01	%
Feedthrough Attenuation Ratio at 1kHz	C_h=0.01μF		86	96		86	96		dB
Output Impedance	"HOLD" Mode			0.5	1		0.5	1	Ω
		●			4			6	Ω
"HOLD" Step (Note 4)	C_h=0.01μF, V_{OUT}=0			0.25	1		0.25	1	mV
Supply Current (Note 6)	$T_j \geq 25°C$			4.5	5.5		4.5	6.5	mA
Logic and Logic Reference Input Current				2	10		2	10	μA
Leakage Current into Hold Capacitor (Note 6)	"HOLD" Mode (Note 5)			10	100		10	100	pA
Acquisition Time to 0.1%	ΔV_{OUT}=10V, C_h=1000pF			4	6		4	6	μs
	C_h=0.01μF			16	25		16	25	μs
Hold Capacitor Charging Current	$V_{IN}-V_{OUT}$=2V			5			5		mA
Supply Voltage Rejection Ratio	V_{OUT}=0		90	110		90	110		dB
Differential Logic Threshold			0.8	1.4	2.4	0.8	1.4	2.4	V

ELECTRICAL CHARACTERISTICS (Note 3)

PARAMETER	CONDITIONS		LF198 MIN	LF198 TYP	LF198 MAX	LF398 MIN	LF398 TYP	LF398 MAX	UNITS
Input Offset Voltage (Note 6)				1	3		2	7	mV
		•			5			10	mV
Input Bias Current (Note 6)				5	25		10	50	nA
		•			75			100	nA
Input Impedance				10^{10}			10^{10}		Ω
Gain Error	$R_L = 10k$			0.002	0.005		0.004	0.01	%
		•			0.02			0.02	%
Feedthrough Attenuation Ratio at 1kHz	$C_h = 0.01\mu F$		86	96		80	96		dB
Output Impedance	"HOLD" Mode			0.5	2		0.5	4	Ω
		•			4			6	Ω
"HOLD" Step (Note 4)	$C_h = 0.01\mu F$, $V_{OUT} = 0$			0.5	2.0		0.5	2.5	mV
Supply Current (Note 6)	$T_j \geq 25°C$			4.5	5.5		4.5	6.5	mA
Logic and Logic Reference Input Current				2	10		2	10	μA
Leakage Current into Hold Capacitor (Note 6)	"HOLD" Mode (Note 5)			30	100		30	200	pA
Acquisition Time to 0.1%	$\Delta V_{OUT} = 10V$, $C_h = 1000pF$			4			4		μs
	$C_h = 0.01\mu F$			16			16		μs
Hold Capacitor Charging Current	$V_{IN} - V_{OUT} = 2V$			5			5		mA
Supply Voltage Rejection Ratio	$V_{OUT} = 0$		80	110		80	110		dB
Differential Logic Threshold			0.8	1.4	2.4	0.8	1.4	2.4	V

The • denotes the specifications which apply over the full operating temperature range.

Note 1: T_j max for the LF198/LF198A is 150°C; T_j max for the LF398/LF398A is 100°C.

Note 2: The logic inputs are protected to ±30V differential as long as the voltage on both pins does not exceed the supply voltage. For proper operation, however, both logic and logic reference pins must be at least 2V below the positive supply and one of these pins must be at least 3V above the negative supply.

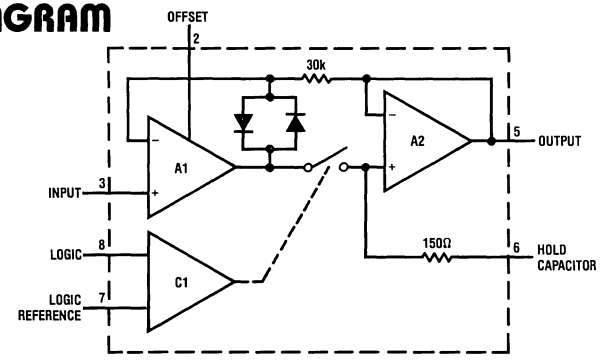
Note 3: Unless otherwise noted, $V_S = \pm 15V$, $T_j = 25°C$, $-11.5V \leq V_{IN} \leq +11.5V$, $C_h = 0.01\mu F$, $R_L = 10k\Omega$ and unit is in "sample" mode. Logic reference = 0V and logic voltage = 2.5V.

Note 4: The hold step is sensitive to stray capacitance coupling between input logic signals and the hold capacitor. 1pF, for instance, will create an additional 0.5mV step with a 5V logic swing and a 0.01μF hold capacitor. Magnitude of the hold step is inversely proportional to hold capacitor value.

Note 5: Leakage current is measured at a *junction* temperature of 25°C. The effects of junction temperature rise due to power dissipation or elevated ambient can be calculated by doubling the 25°C value for each 11°C increase in chip temperature. Leakage is guaranteed over full input signal range.

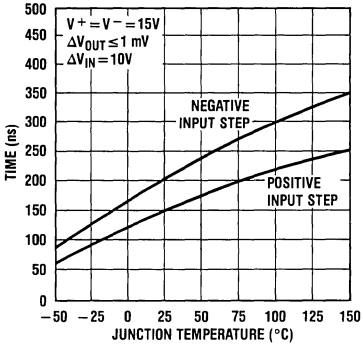
Note 6: These parameters are guaranteed over a supply voltage range of ±5V to ±18V.

FUNCTIONAL DIAGRAM



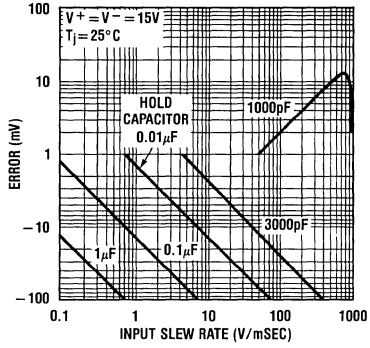
TYPICAL PERFORMANCE CHARACTERISTICS

Aperture Time*



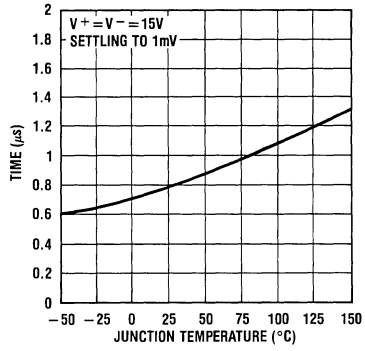
*See Definition of Terms

Dynamic Sampling Error*



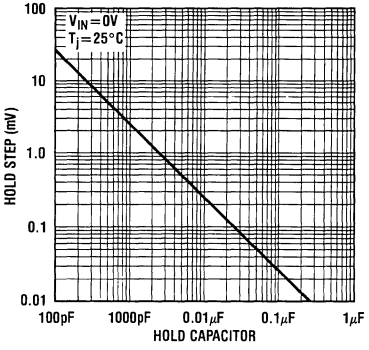
*See Definition of Terms

"Hold" Settling Time*

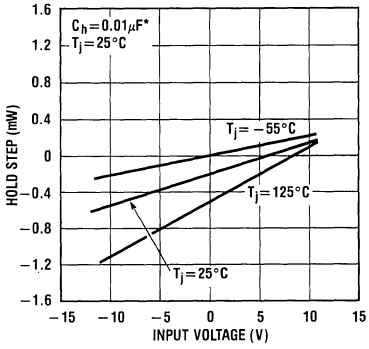


*See Definition of Terms

Hold Step

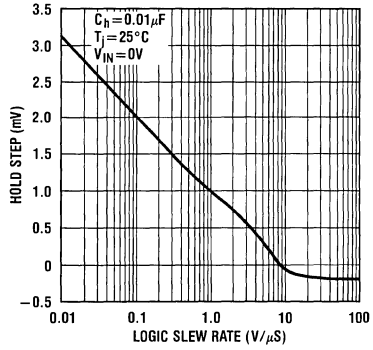


Hold Step vs Input Voltage

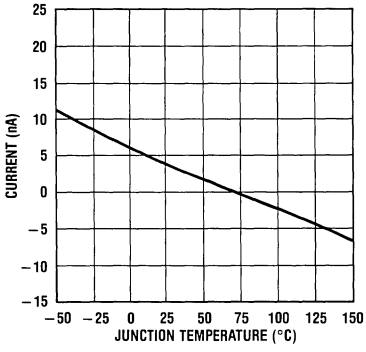


*Amplitude of hold step scales inversely with hold capacitor value

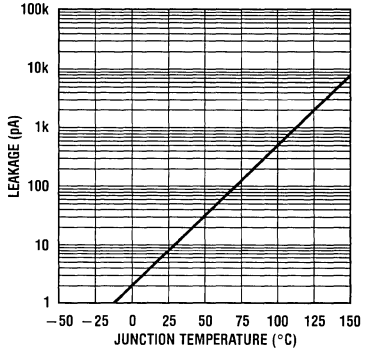
Hold Step vs Logic Slew Rate



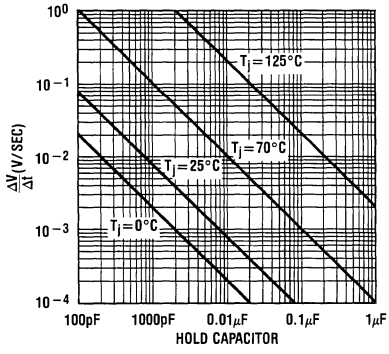
Input Bias Current



Capacitor Pin Leakage

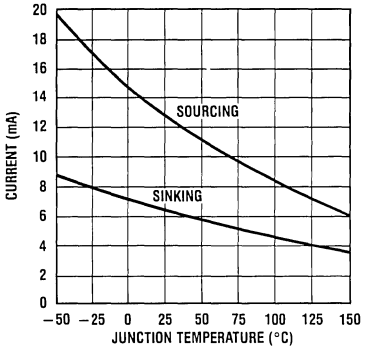


Output Droop Rate

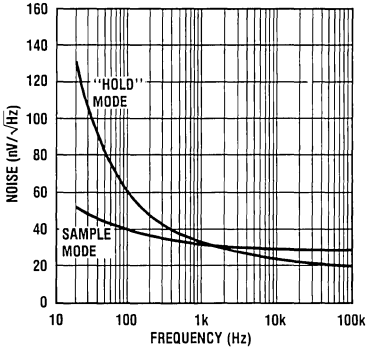


TYPICAL PERFORMANCE CHARACTERISTICS

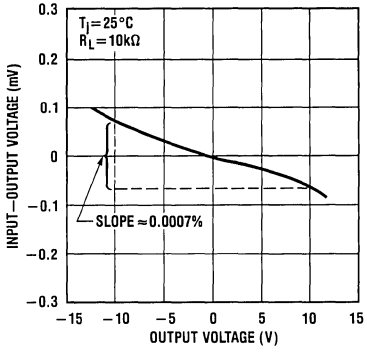
Output Short Circuit Current



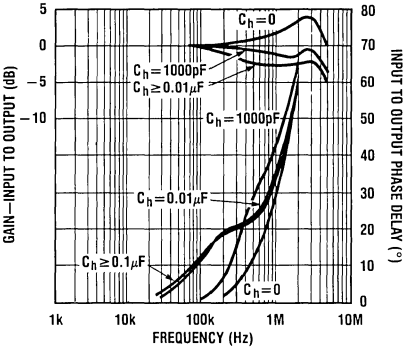
Output Noise



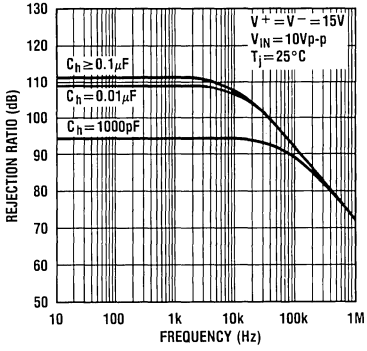
Gain Error



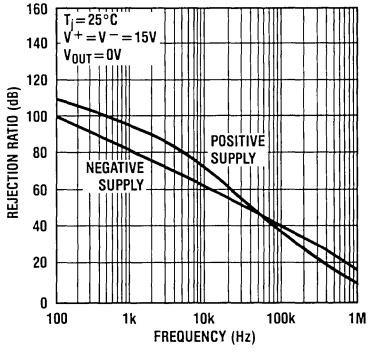
Phase and Gain (Input to Output, Small Signal)



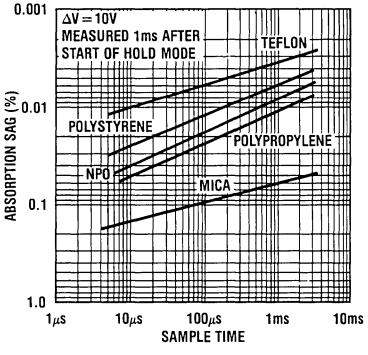
Feedthrough Rejection Ratio



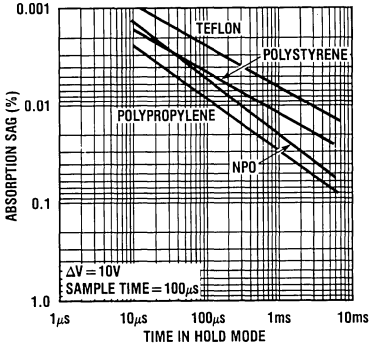
Power Supply Rejection



Capacitor Dielectric Absorption

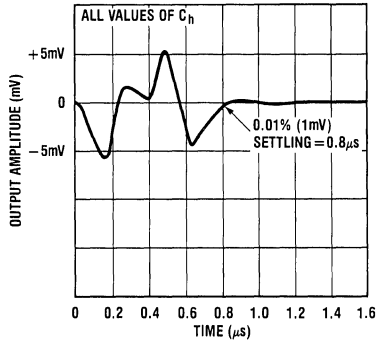


Capacitor Dielectric Absorption

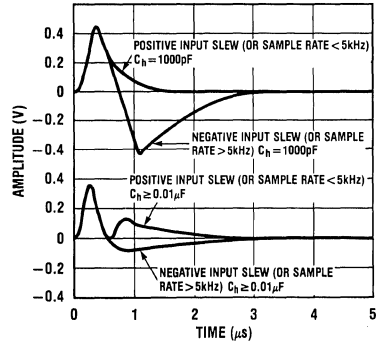


TYPICAL PERFORMANCE CHARACTERISTICS

Output Transient at Start of Hold Mode



Output Transient at Start of Sample Period



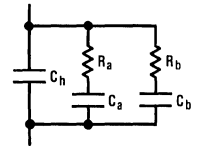
APPLICATIONS INFORMATION

Hold Capacitor

For fast sample and hold applications, the size of the hold capacitor is critical. A low value will give fast acquisition, but will also increase errors due to hold step, and droop caused by amplifier bias current. The capacitor should be made as large as possible, consistent with acquisition time and dynamic sampling error requirements. Capacitors larger than 0.1μF have an additional problem. They are generally not available in the low loss dielectrics like Teflon, Polystyrene, and NPO, at least not at a reasonable price and size. Mylar, even with its poor dielectric absorption properties, may be a reasonable choice where very long sample times are used and low droop rates are needed.

Dielectric absorption in the hold capacitor can often be the major source of error in a sample and hold. The equivalent "circuit" of a typical capacitor is shown below with parallel RC networks used to model dielectric absorption.

Typical Hold Capacitor Equivalent Circuit



C_a, $C_b \approx 0.01$ TO 0.1 C_h
R_a, R_b GENERATE TIME CONSTANTS OF 0.1-50 MILLISECONDS WITH C_a, C_b

One can see that rapid changes in capacitor voltage will not be tracked by the internal parasitic capacitors because of the resistance in series with them. This leads to a "sag" effect in the hold capacitor after a sudden change in voltage followed by rapid switch to the hold mode. The capacitor remembers its previous state via the charge on the internal parasitic capacitance and sags

APPLICATIONS INFORMATION

back slightly toward the previous voltage. The magnitude of the sag depends on the voltage change and the time spent sampling the new voltage. Several time constants are typically evident in the sag, although some capacitors tend to exhibit a single time constant, while others show a sag that indicates a blending of many time constants. The curves labeled CAPACITOR DIELECTRIC ABSORPTION show the amount of sag found after a 10V step with sample time at the new voltage and hold time at the new voltage as variables. It is obvious that sag problems are minimized by long sample times and short hold times. This is often in conflict with basic sampling requirements, but one point should be made: if at all possible, keep the sample and hold amplifier in the "tracking", or sampling, mode as much as possible to maximize the time the hold capacitor spends near the voltage at which it will eventually "hold".

The best capacitor for sample and hold applications is Teflon. It is clearly superior with regard to dielectric absorption and operates over the full −55°C to 125°C temperature range. If size or price becomes a problem, the second choice for full temperature range operation is "NPO", or "COG" ceramic units. Some care must be used here—not all NPO capacitors use the low dielectric constant ceramic necessary for low dielectric absorption. For lower temperatures ($\leq$70°C), Polystyrene has traditionally been the best hold capacitor. The best units are cylindrical and fairly large—there seems to be a strong correlation between small size and poorer dielectric performance. Polypropylene has nearly the same absorption properties as polystyrene and offers 85°C operation. It also tends to be smaller. Again, stay with cylindrically wrapped units. Other standard dielectrics such as mica, glass, mylar, and ordinary ceramic are much worse with regard to dielectric absorption. Mylar is sometimes used for large values when the ratio of sample to hold time is large and extremely low droop is required.

Dynamic Sampling Error

A significant sampling error can occur in any sample and hold if the input is moving when the unit is put into the hold mode. The two major causes for this error are digital delay in switch opening and analog delay across the hold capacitor. The switch opening delay is obvious and leads to a "held" output error of $(dv/dt) \times (T_d)$, where dv/dt is the slew rate of the input signal and T_d is switch delay. In the case of the LF198, T_d is approximately 150ns, giving a 4.5mV error when sampling the zero crossing of a 5V (peak) sine wave at 1kHz ($dv/dt = A \cdot 2\pi f = 5 \cdot 2\pi \cdot 10^3$). The analog delay is the difference between input signal and capacitor voltage. It is determined by the RC product of the hold capacitor and the effective series resistance, which in the case of the LF198 is about 150Ω. This analog delay with a 0.01μF hold capacitor is $R \cdot C = 150 \times 10^{-8} = 1.5\mu s$, or about ten times the delay of the switch. The sign of the analog delay is negative—the held output is related in time to the input voltage *before* the hold command was given. The overall dynamic sampling error is the sum of the digital and analog errors. The curve labeled *Dynamic Sampling Error* will be helpful in estimating these errors as a function of input slew rate and hold capacitor size.

Dynamic sampling error can be reduced by a factor of ten or more by inserting a delay in the logic input so that the "hold" command is delayed by an amount equal to the RC time constant of the LF198 and external hold capacitor. For a 0.01μF hold capacitor and the 150Ω resistor internal to the LF198, this is 1.5μs. A simple RC network can be used in front of the logic input for delays up to $\approx$1μs. Longer delays require the addition of a logic gate to speed up the rise time of the delayed signal. See LOGIC RISE TIME in this section for further details.

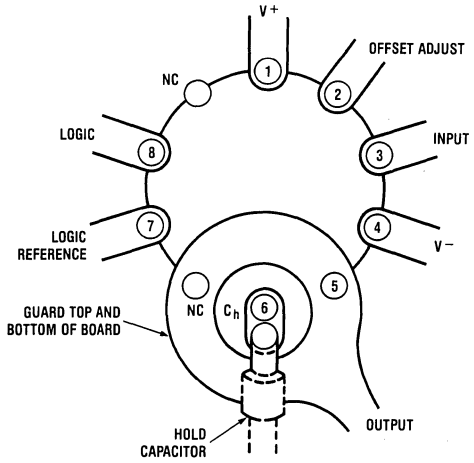
Hold Step

Hold step is the small voltage step (after settling) seen at the output of a sample and hold amplifier when it is switched from the sample mode to the hold mode with a steady DC input. Hold step is typically the result of, or can be modeled as, a fixed quantity of charge transferred to the hold capacitor as a result of the internal switching that occurs during the hold command. In the case of the LF198, that charge is about 5 picocoulombs, giving a hold step of 0.5mV for a 0.01μF hold capacitor and 5mV for a 1000pF hold capacitor. ($V = Q/C$.) Hold step is reasonably independent of logic amplitude if care is taken to minimize the stray capacitance between the logic input

APPLICATIONS INFORMATION

and the hold capacitor. With thoughtful layout, including the guarding technique shown below, stray capacitance should be under 0.3pF, limiting charge variations to less than 0.3 picocoulombs per volt.

Guarding Technique



BOTTOM VIEW

Use 10-pin layout. Guard around C_h is tied to output.

Hold step varies slightly with analog input voltage (see curves). A typical unit will change at 0.4 picocoulombs per volt. This manifests itself as a gain error when the amplifier is switched to the hold mode. With a 0.01μF capacitor, the resulting gain error will be (0.4 PC/V)/0.01μF = 0.004%. This gain error is in the opposite direction of DC (sample mode) gain error. At high values of hold capacitor, DC gain error will dominate and gain will be slightly below unity (0.002%). For low value capacitors (< 0.01μF), hold step induced gain error will dominate and hold mode gain will be slightly above unity. Zeroing out hold step does not change the variation of hold step with regard to input voltage.

Offset Zeroing

A sample and hold amplifier has two distinct offset voltages. The first is just the DC offset of the amplifier while in the sample or "tracking" mode. It is identical to the input offset of any operational amplifier. The second offset voltage is the sum of the DC offset plus a dynamic term called hold step. Hold step is a change in output voltage when the amplifier is switched from sample mode to hold mode, with the input held steady. This second offset is often called hold mode offset. It can be less than or much greater than the DC offset, depending on the magnitude and sign of hold step.

A fairly accurate model for hold step is a fixed charge injected into the hold capacitor by the switch turn-off circuitry. The magnitude of the charge is reasonably independent of logic input amplitude. The resulting change in hold capacitor voltage is Q/C_h. The charge, Q, is typically 5 picocoulombs, giving a 0.5mV hold step with a 0.01μF hold capacitor. Since most sample and hold amplifiers are "used," i.e., have their outputs read by an A to D converter, etc., during the hold mode, hold mode offset is arguably much more important than sample mode DC offset.

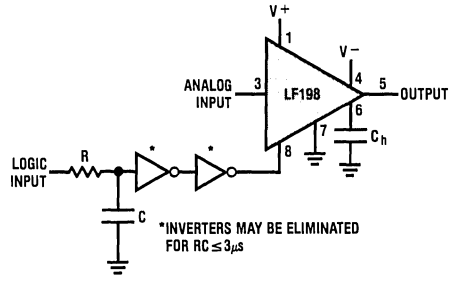
DC offset adjustment is accomplished with a 1k low TC cermet potentiometer tied to V^+ with 0.6mA flowing through it and the wiper tied to pin 2. This allows pin 2 to be moved ±300mV around its nominal voltage (0.3V below V^+). Offset adjustment range is ±9mV, and the adjustment procedure nominally improves offset drift when the DC offset is reduced to zero. This offset method *can* be used to zero out hold mode offset, but at the expense of some induced offset drift. Each millivolt of hold step offset that is corrected by this method introduces 3.3μV/°C drift. For 0.002μF or larger hold capacitors where hold step is a few millivolts or less, this is a practical solution to hold mode offset. In precision wide temperature range applications, or where C_h is less than 0.002μF, a separate hold mode zeroing method should be used. The circuit shown in the application section using a logic inverter and a 5pF capacitor is recommended (DC AND AC ZEROING).

APPLICATIONS INFORMATION

Logic Fall Time

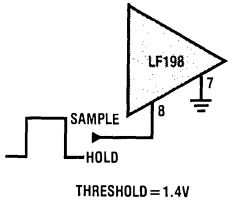
Hold step is independent of logic input fall time only for fall times faster than 10V/μs. For instance, as logic fall time changes from 10V/μs to 1V/μs, hold step with a 0.01μF hold capacitor will typically increase from 0.25mV to 1.0mV. See the curve labeled HOLD STEP vs LOGIC SLEW RATE for further data points. If logic slew rate is not constant, use the value at the threshold point (1.5V with respect to logic reference). An RC network will have a discharge slew rate of V_L/RC, where V_L is the logic threshold of the LF198. The delay generated by the network will be $RC \cdot \ln(V^+/V_L)$, where V^+ is logic amplitude. For a 1μs delay, with 5V logic, an RC time constant of 0.8μs is needed. This has a slew rate of 2V/μs at threshold, which will slightly degrade hold step. It is obvious that an RC delay network significantly longer then 1μs will have a large effect on hold step. If longer delays are required, they should be followed by several inverter stages or a Schmitt trigger to increase slew rate.

Adding Delay to Logic Input

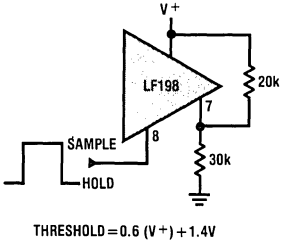


LOGIC INPUT CONFIGURATIONS*

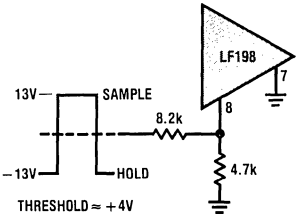
TTL and CMOS
$3V \leq V_L$ (Hi State) $\leq 10V$

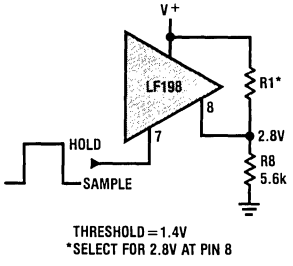


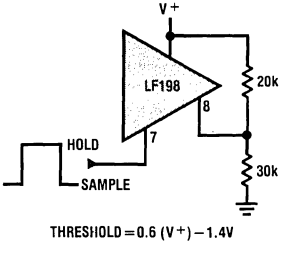
CMOS
$7V \leq V_L$ (Hi State) $\leq 15V$

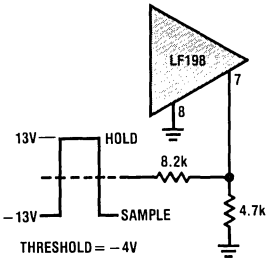


Op Amp Drive





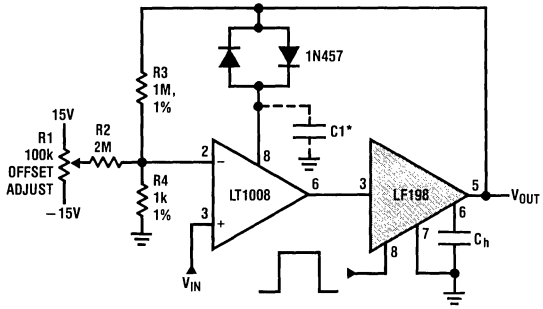




*The logic input signal high state must be at least 2V below the positive supply voltage of the LF198.

TYPICAL APPLICATIONS

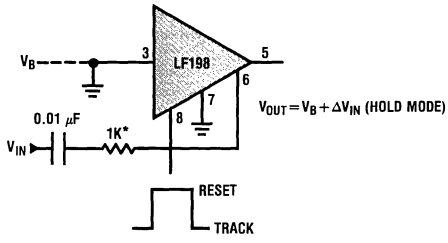
X1000 Sample and Hold



*FOR LOWER GAINS, THE LT1008 MUST BE FREQUENCY COMPENSATED

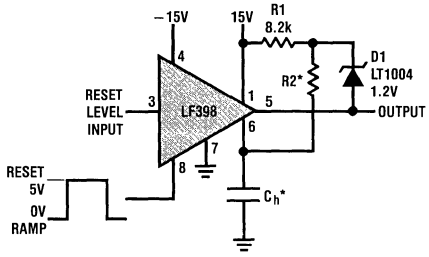
USE $\approx \frac{100}{A_V}$pF FROM COMP 2 TO GROUND

Sample and Difference Circuit (Output Follows Input in Hold Mode and Resets to V_B in Sample Mode)



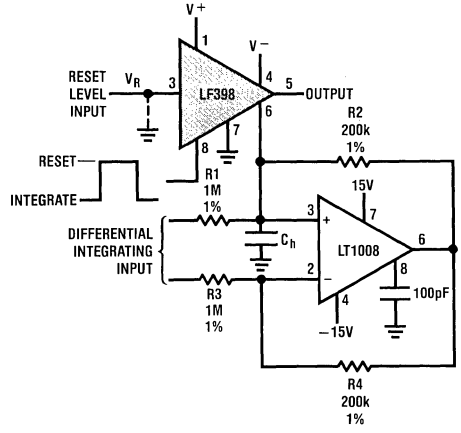
*THIS RESISTOR PROTECTS INPUT FROM SURGE CURRENTS, BUT INCREASES SAMPLE TIME. IT CAN BE ELIMINATED IF INPUT IS OTHERWISE PROTECTED.

Ramp Generator with Variable Reset Level



*SELECT FOR RAMP RATE $\frac{\Delta V}{\Delta T} = \frac{1.2V}{(R2)C_h)}$
$R \geq 10k$

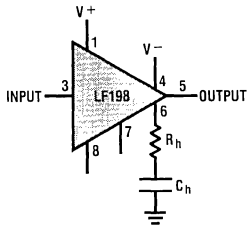
Integrator with Programmable Reset Level



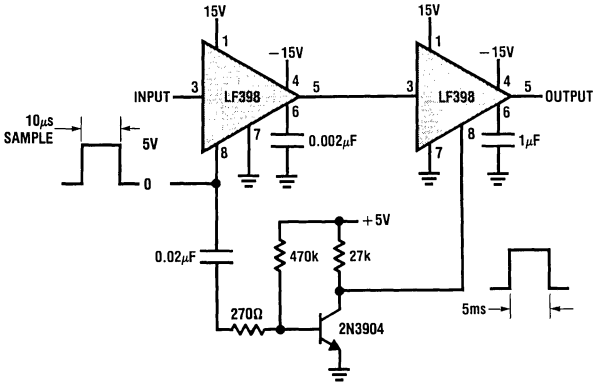
V_{OUT} (HOLD MODE) $= \left[\frac{1}{(R1)C_h}\int_0^t V_{IN} dt\right] + \left[V_R\right]$

TYPICAL APPLICATIONS

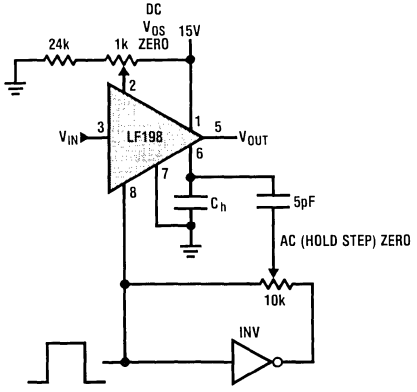
Output Holds at Average of Sampled Input



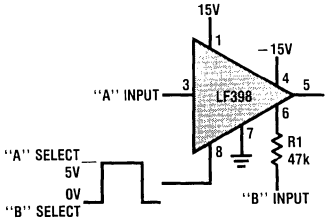
Fast Acquisition, Low Droop Sample and Hold



DC and AC Zeroing



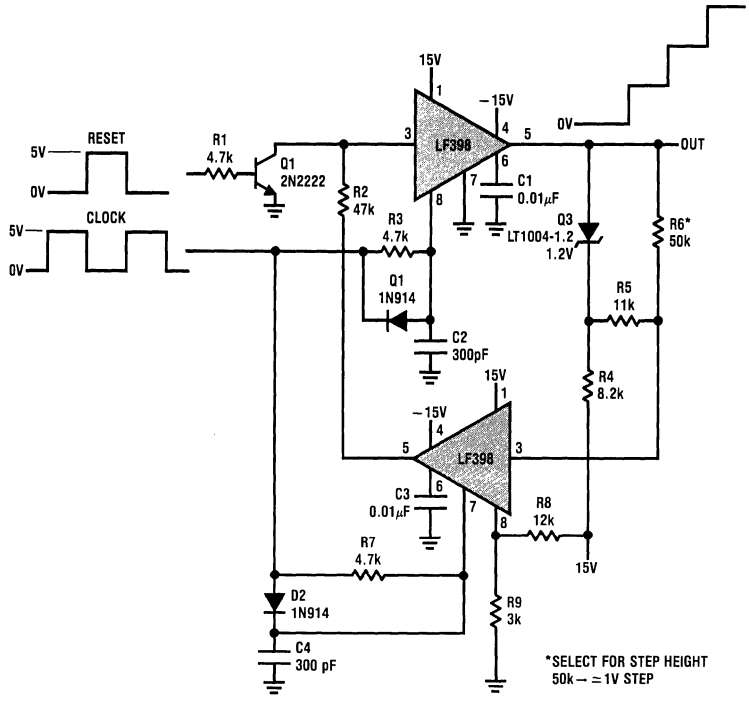
2-Channel Switch



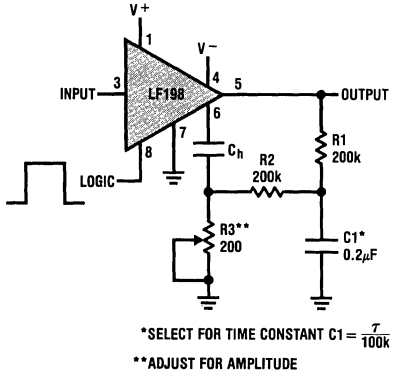
	A	B
Gain	1 ± 0.02%	1 ± 0.2%
Z_{IN}	$10^{10}\Omega$	47kΩ
BW	= 1MHz	≈ 400kHz
Crosstalk @1kHz	−90dB	−90dB
Offset	≤ 6mV	≤ 75mV

TYPICAL APPLICATIONS

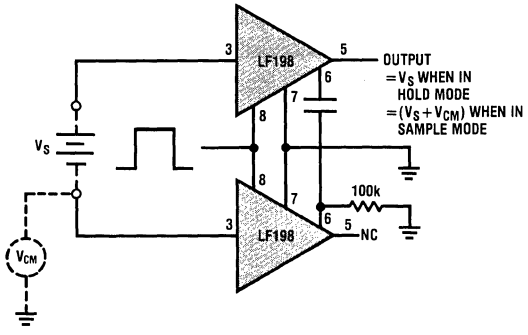
Staircase Generator



Capacitor Hysteresis Compensation

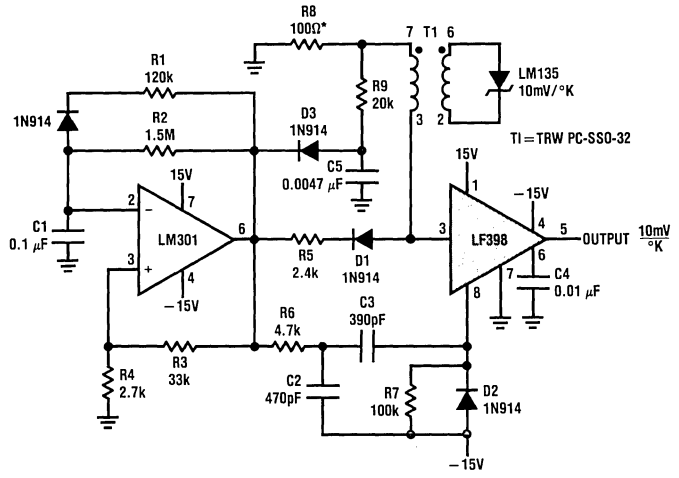


Differential Hold



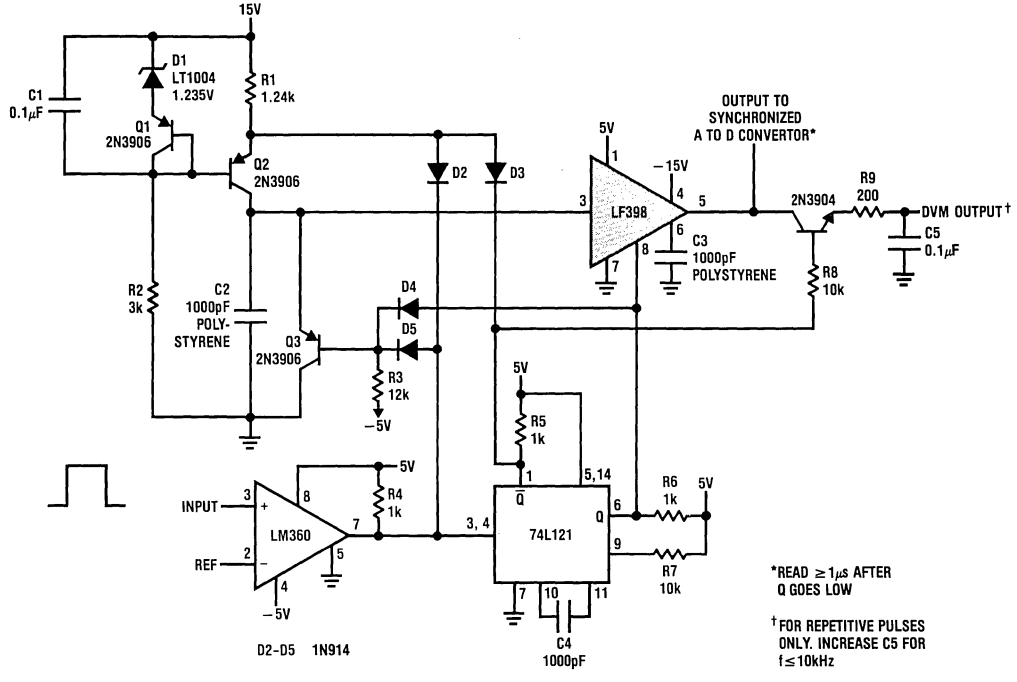
TYPICAL APPLICATIONS

Isolated Temperature Sensor



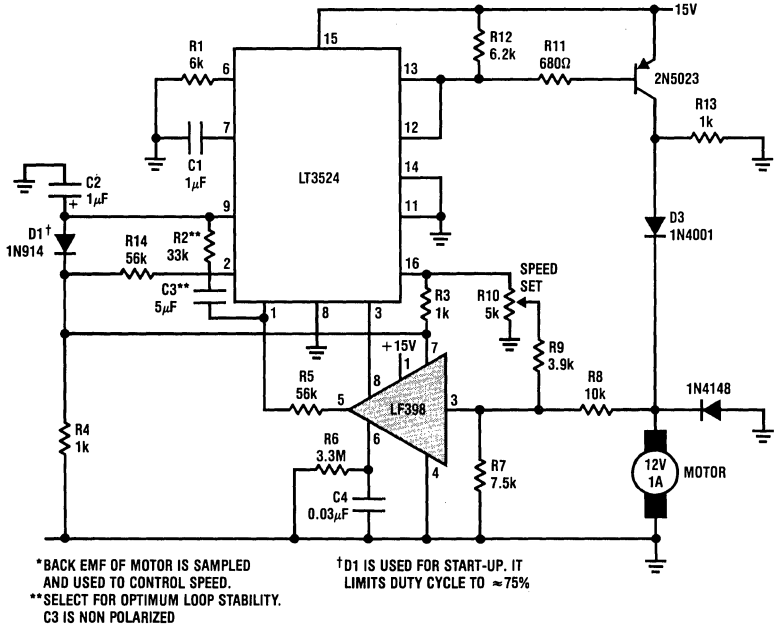
*COMPENSATES FOR TRANSFORMER RESISTANCE. SELECT FOR FLAT OUTPUT FROM LF198 WHILE IN SAMPLE MODE.

Pulse Width to Voltage Converter



TYPICAL APPLICATIONS

Motor Speed Controller Needs No Tachometer*



*BACK EMF OF MOTOR IS SAMPLED AND USED TO CONTROL SPEED.
**SELECT FOR OPTIMUM LOOP STABILITY. C3 IS NON POLARIZED

†D1 IS USED FOR START-UP. IT LIMITS DUTY CYCLE TO ≈75%

DEFINITION OF TERMS

Hold Step: The voltage step at the output of the amplifier when switching from sample mode to hold mode with a constant analog input voltage and a logic swing of 5V.

Acquisition Time: The time required to acquire, within a defined error, a new analog input voltage with an output change of 10V. Acquisition time includes output settling time and includes the time required for all internal nodes to settle so that the output is at the proper value when switched to the hold mode.

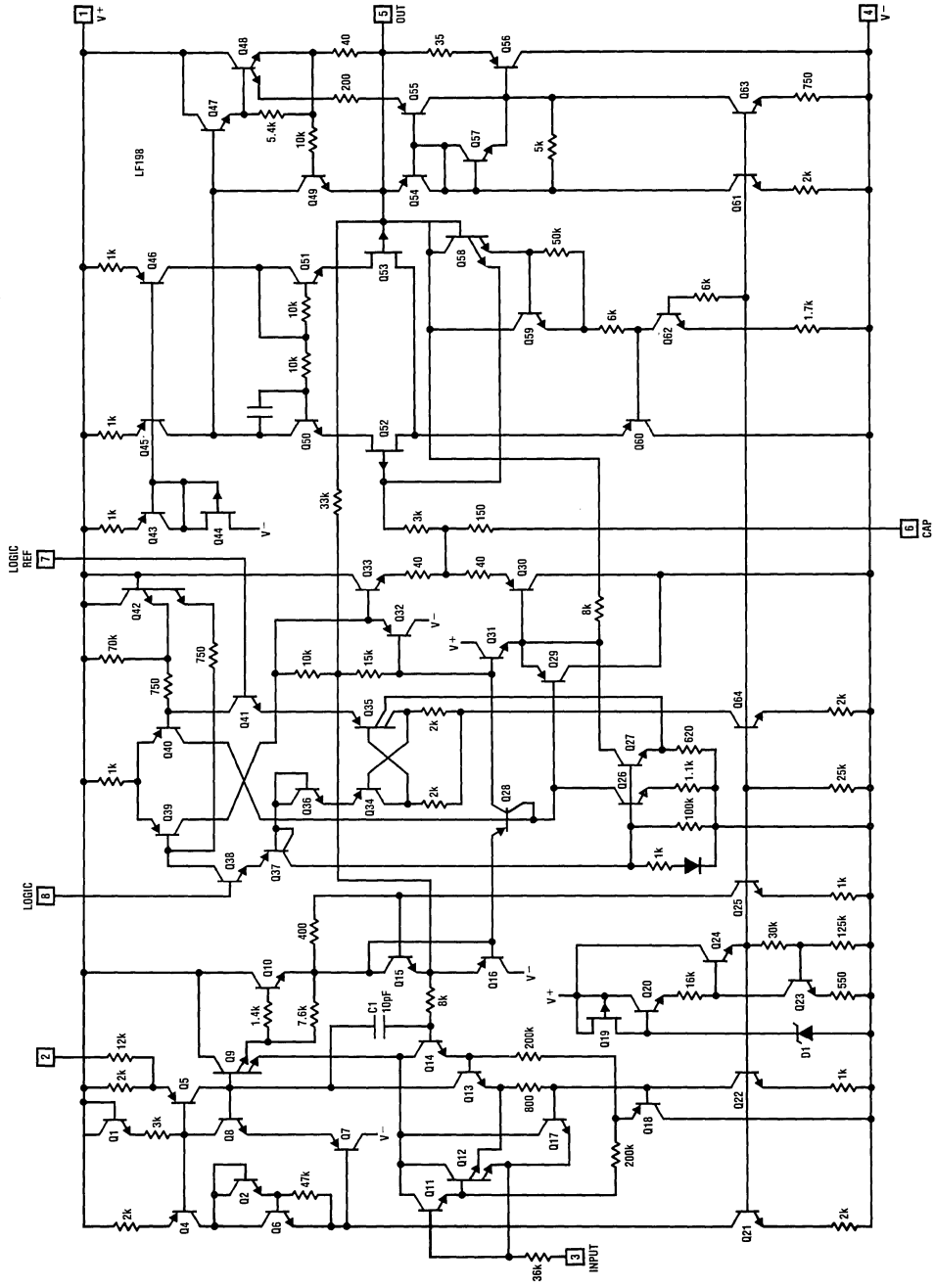
Gain Error: The ratio of output voltage swing to input voltage swing in the sample mode expressed as a percent difference.

Hold Settling Time: The time required for the output to settle within 1mV of final value after a hold command is initiated.

Dynamic Sampling Error: The error introduced into the held output voltage due to a changing analog input at the time the hold command is given. Error is expressed in mV with a given hold capacitor value and input slew rate. Note that this error term occurs even for long sample times.

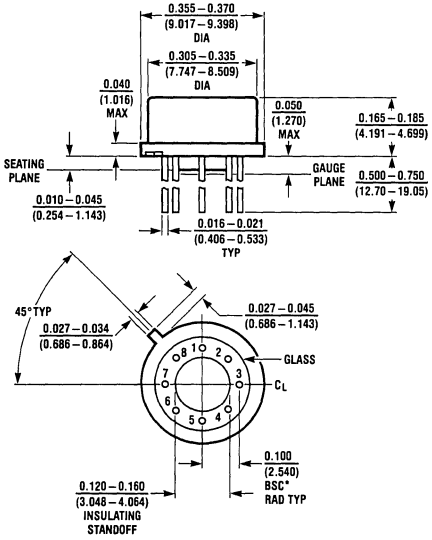
Aperture Time: The delay required between "Hold" command and an input analog transition, so that the transition does not affect the held output.

SCHEMATIC DIAGRAM



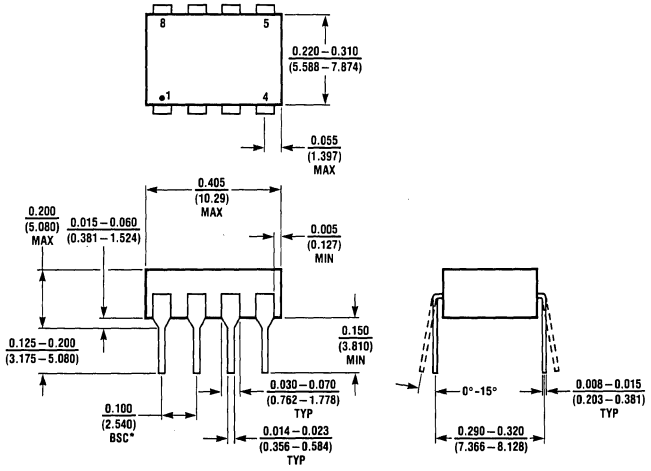
PACKAGE DESCRIPTION Dimensions in inches (millimeters) unless otherwise noted.

H Package
Metal Can



	$T_j$max	θ_{ja}	θ_{jc}
LF198/LF198A	150°C	150°C/W	45°C/W
LF398/LF398A	100°C	150°C/W	45°C/W

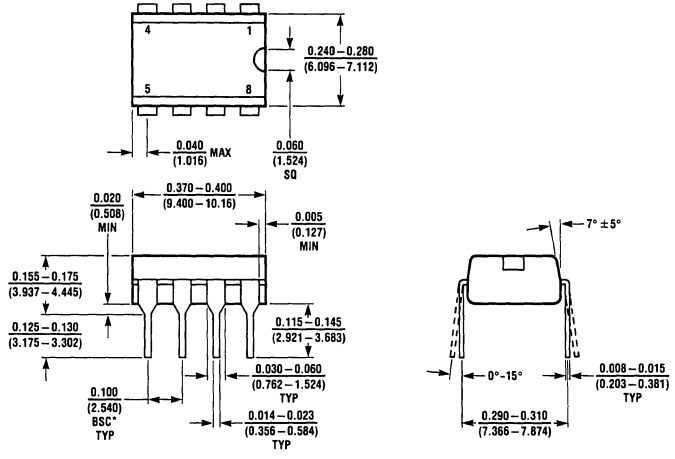
J8 Package
8 Lead Hermetic DIP



*LEADS WITHIN 0.007 OF TRUE POSITION (TP) AT GAUGE PLANE

	$T_j$max	θ_{ja}
LF398	100°C	100°C/W

N8 Package
8 Lead Plastic



*LEADS WITHIN 0.007 OF TRUE POSITION (TP) AT GAUGE PLANE

	$T_j$max	θ_{ja}
LF398/LF398A	100°C	130°C/W

Quad Low Power Line Driver

FEATURES

- Low Operating Voltage ±5V to ±15V
- 500μA Supply Current
- Zero Supply Current when Shut Down
- Outputs Can Be Driven ±30V
- Thermal Limiting
- Output "Open" when Off
- 10mA Output Drive
- Pin Compatible with 1488

APPLICATIONS

- RS232 Driver
- Power Supply Inverter
- Micropower Interface
- Level Translator

DESCRIPTION

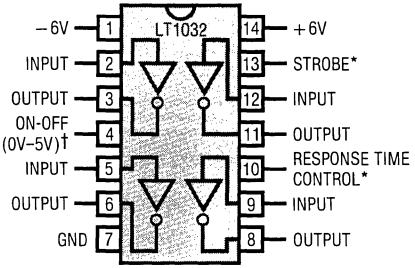
The LT1032 is a RS232 and RS423 line driver that operates over a ±5V to ±15V range on low supply current and can be shut down to zero supply current. Outputs are fully protected from externally applied voltages of ±30V by both current and thermal limiting. Since the output swings to within 200mV of the positive supply and 600mV of the negative supply, power supply needs are minimized.

Also included is a strobe pin to force all outputs low independent of input or shutdown conditions. Further, slew rate can be adjusted with a resistor connected to the supply.

A major advantage of the LT1032 is the high impedance output state when off or powered down.

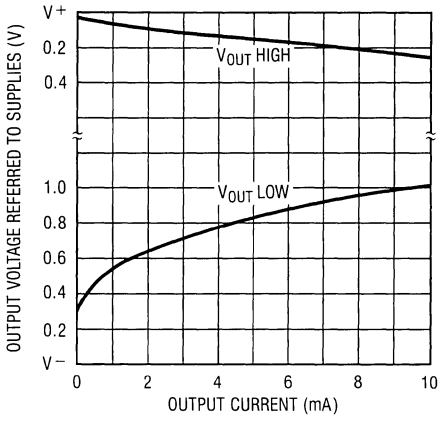
TYPICAL APPLICATION

RS232 Line Driver



*NO CONNECTION NEEDED WHEN NOT USED.
†5V = ON.

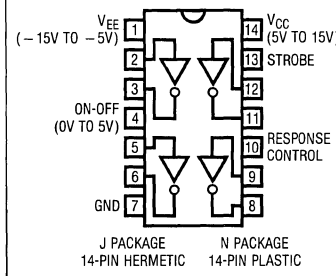
Output Swing vs Output Current



ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... ±15V
Logic Input Pins ..... V^- to 25V
On-Off Pin ..... GND to 15V
Output (Forced) ..... V^- +30V, V^+ −30V
Response Pin ..... ±6V
Short Circuit Duration (to ±30V) ..... Indefinite
Operating Temperature Range
LT1032M ..... −55°C to 125°C
LT1032C ..... 0°C to 70°C
Guaranteed Functional by Design ... −25°C to 85°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



J PACKAGE 14-PIN HERMETIC
N PACKAGE 14-PIN PLASTIC

ORDER PART NUMBER
LT1032MJ LT1032CJ LT1032CN

ELECTRICAL CHARACTERISTICS

(Supply Voltage = ±5V to ±15V)

PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
Supply Current	$V_{ON/OFF} \geq 2.4V$, $I_{OUT} = 0$, All Outputs Low		●		500	1000	μA
Power Supply Leakage Current	$V_{ON-OFF} \leq 0.4V$				1	10	μA
	$V_{ON-OFF} \leq 0.1V$, $T_A = 125°C$		●		10	50	μA
Output Voltage Swing	Load = 2mA	Positive		$V^+ - 0.3V$	$V^+ - 0.1V$		V
		Negative		$V^- + 0.9V$	$V^- + 0.7V$		V
Output Current	V_{SUPPLY} ±5V to ±15V			10	22		mA
Output Overload Voltage (Forced)	Operating or Shutdown		●	$V^+ - 30V$		$V^- + 30V$	V
Output Current	Shutdown $V_{OUT} = \pm 30V$				2	100	μA
Input Overload Voltage (Forced)	Operating or Shutdown		●	V^-		30V	V
Logic Input Levels	Low Input (V_{OUT} = High)		●		1.4	0.8	V
	High Input (V_{OUT} = Low)		●	2	1.4		V
Logic Input Current	$V_{IN} > 2.0V$				2	20	μA
	$V_{IN} < 0.8V$				10	20	μA
On-Off Pin Current	$0 \leq V_{IN} \leq 5V$		●	−10	3	50	μA
Slew Rate	$I_{RESPONSE} = 0$			4	15	30	V/μS
Change in Slew Rate (Note 2)	$I_{RESPONSE} = +50\mu A$				+50		%
	$I_{RESPONSE} = -50\mu A$				−50		%
Response Pin Leakage	$V_{SUPPLY} = \pm 6V$, $V_{ON/OFF} \leq 0.4V$, $V_{RESPONSE} = \pm 6V$				1		μA

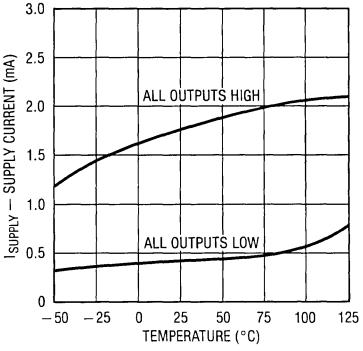
The ● denotes specifications which apply over the operating temperature range.

Note 1: 3V applied to the strobe pin will force all outputs low. Strobe pin input impedance is about 2k to ground. Leave open when not used.

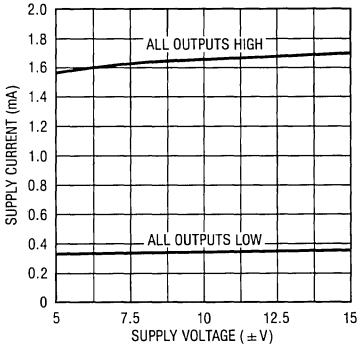
Note 2: Response can be changed by connecting a resistor to the supply. For supplies less than ±6V this current is disconnected when shut down. Leave open when not used.

TYPICAL PERFORMANCE CHARACTERISTICS

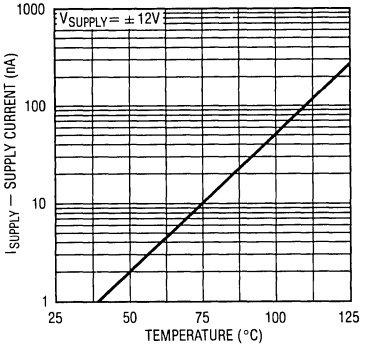
On Supply Current vs Temperature



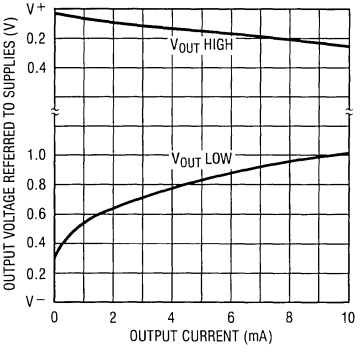
Supply Current vs Supply Voltage



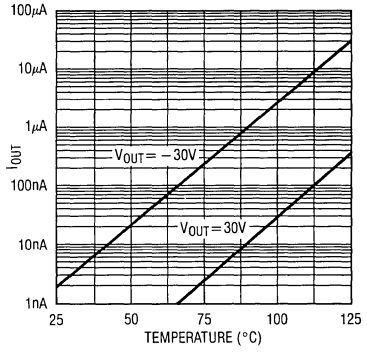
Off Supply Current vs Temperature



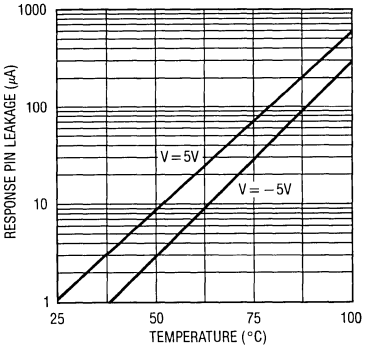
Output Swing vs Output Current



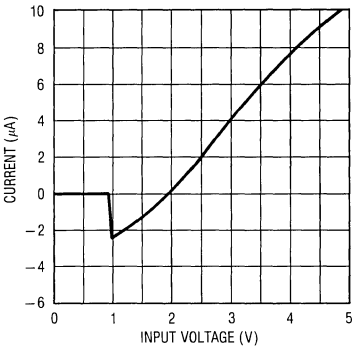
Output Leakage vs Temperature



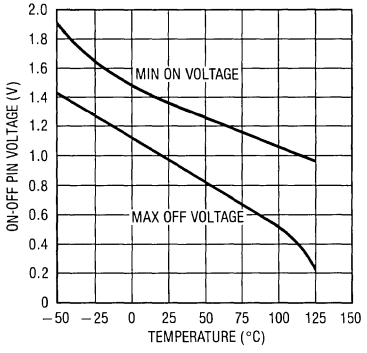
Response Pin Leakage vs Temperature (Device Off)



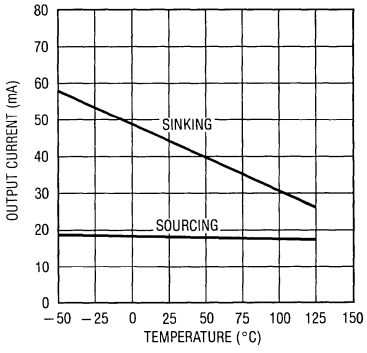
On-Off Pin Current vs Voltage



Shutdown Pin Voltage vs Temperature

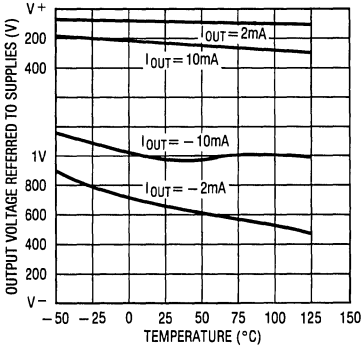


Current Limit vs Temperature

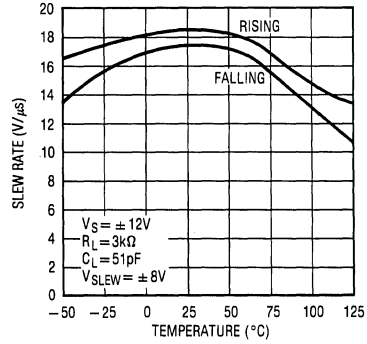


TYPICAL PERFORMANCE CHARACTERISTICS

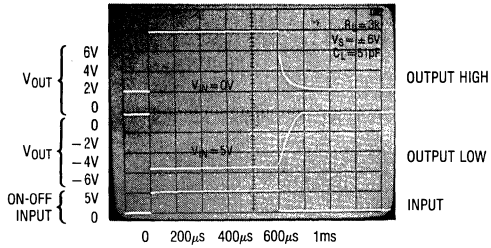
Output Swing vs Temperature



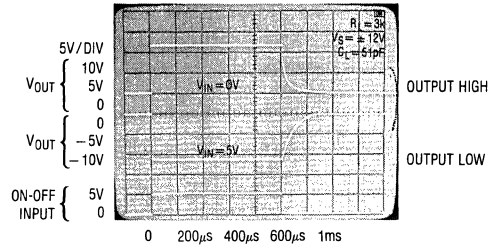
Slew Rate vs Temperature



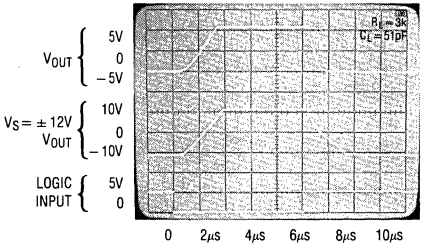
On-Off Response Time



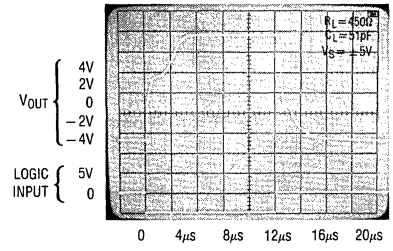
On-Off Response Time



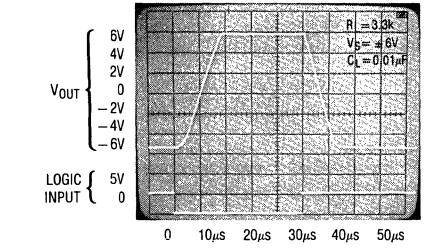
Output Waveform



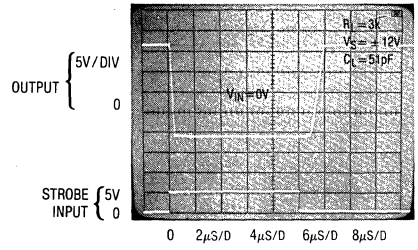
Output Waveform



Output Waveform Driving Capacitive Load



Strobe Pin Response



APPLICATIONS INFORMATION

Application Hints

The LT1032 is exceptionally easy to use when compared to older drivers. Operating supply voltage can be as low as ±3V or as high as ±15V. Input levels are referred to ground.

The logic inputs are internally set at TTL levels. Outputs are valid for input voltages from 1V above V^- to 25V. Driving the logic inputs to V^- turns off the output stage. The "on-off" control completely turns off all supply current of the LT1032. The levels required to drive the device on or off are set by internal emitter-base voltages. Since the current into the "on-off" pin is so low, TTL or CMOS drivers have no problem controlling the device.

The strobe pin is not fully logic compatible. The impedance of the strobe pin is about 2kΩ to ground. Driving the strobe pin positive forces the output stages low—even if the device is shut off. Under worst-case conditions, 3V minimum at 2mA are needed driving the strobe pin to insure strobing.

The response pin can be used to make some adjustment in slew rate. A resistor can be connected between the response pin and the power supplies to drive 50μA to 100μA into the pin. The response pin is a low impedance point operating at about 0.75V above ground. For supply voltage up to ±6V, current is turned off when the device is turned off. For higher supply voltages, a zener should be connected in series with the resistor to limit the voltage applied to the response pin to 6V. Also, for temperatures above 100°C, using the response pin is not recommended. The leakage current into the response pin at high temperatures is excessive.

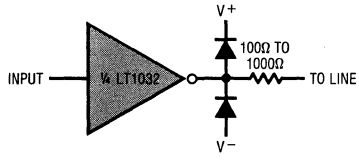
Outputs are well protected against shorts or externally applied votlage. Tested limits are ±30V, but the device can withstand external voltages up to the breakdown of the transistors (typically about 50V). The LT1032 is usually immune to ESD up to 2500V on the outputs with no damage (limit of LTC tester).

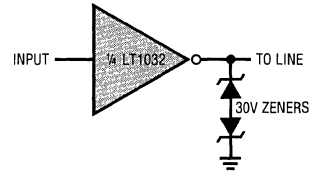
PIN FUNCTION

PIN	FUNCTION	COMMENT
1	Minus Supply	Operates −2V to −15V
2,5,9,12	Logic Input	Operates properly on TTL or CMOS levels. Output valid from $(V^- + 2V) \leq V_{IN} \leq 15V$. Connect to ground when not used.
3,6,8,11	Output	Line drive output.
4	On-Off	Shuts down entire circuit. Cannot be left open. For "normally on" operation, connect to V+.
7	Ground	Ground must be more positive than V^-
10	Response Control	Allows limited change of slew rate. Leave open when not used.
13	Strobe	Forces all outputs low. Drive with 3V.

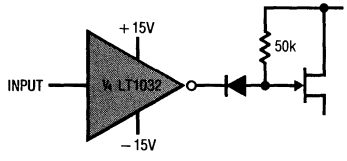
TYPICAL APPLICATIONS

Protecting Against More than ±30V Output Overload

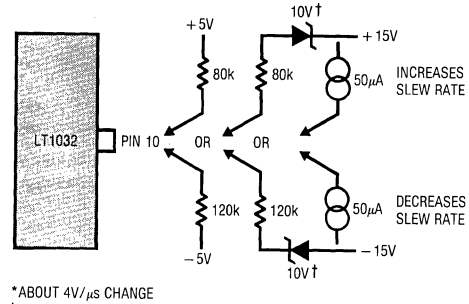




FET Driver

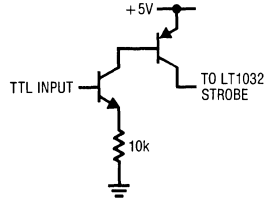


Slew Rate Adjustment*

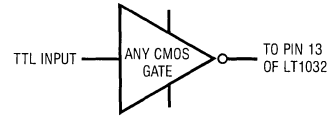


*ABOUT 4V/μs CHANGE
†ZENERS PREVENT LEAKAGE DURING SHUT DOWN

TTL/CMOS Compatible Strobe

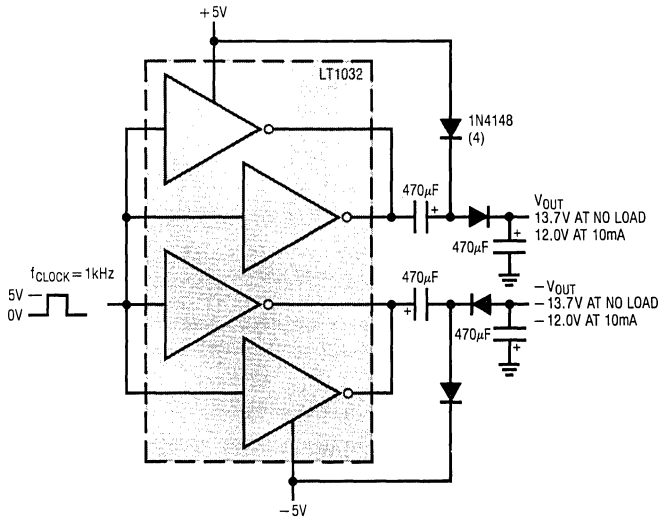


Strobing with CMOS

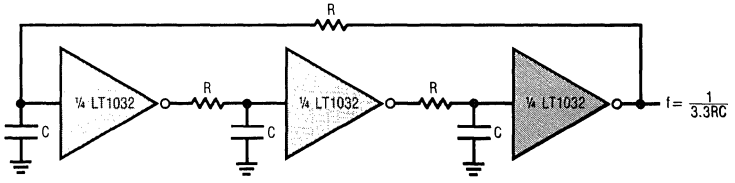


TYPICAL APPLICATIONS

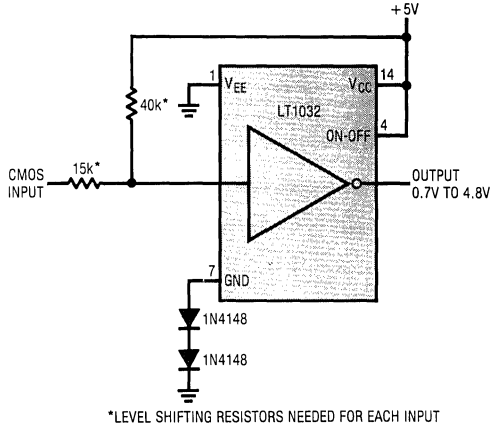
±5V to ±15V Voltage Multiplier



Phase Shift Oscillator

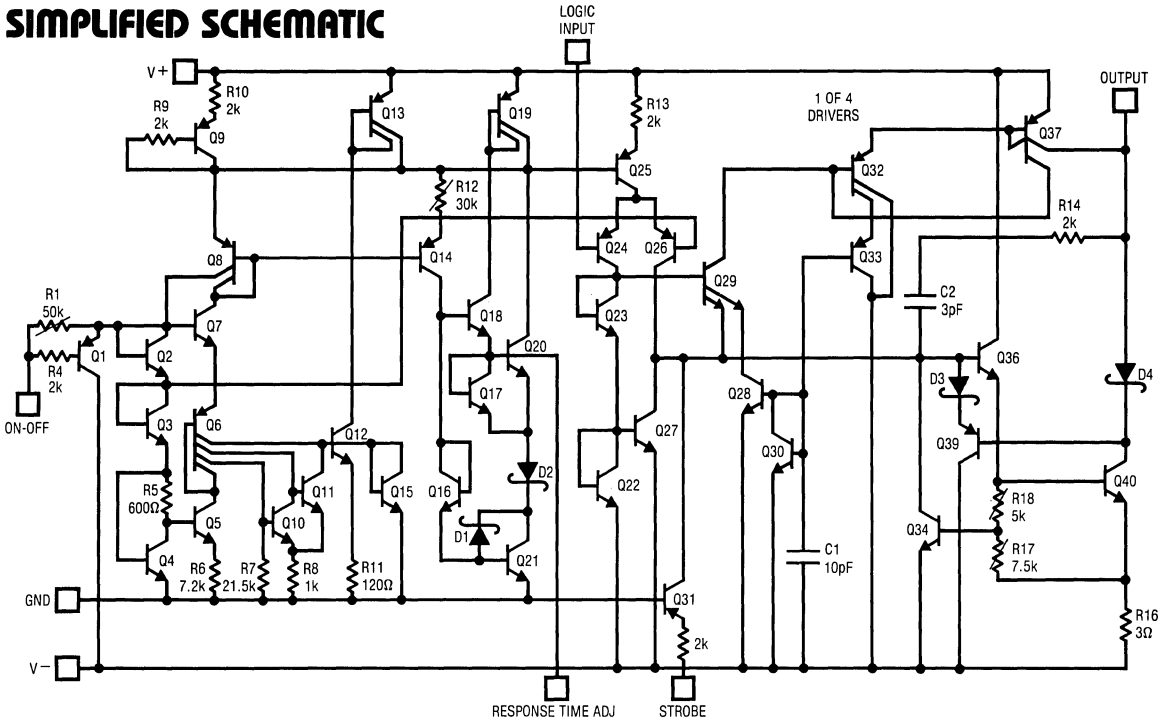


Operating from a Single 5V Supply



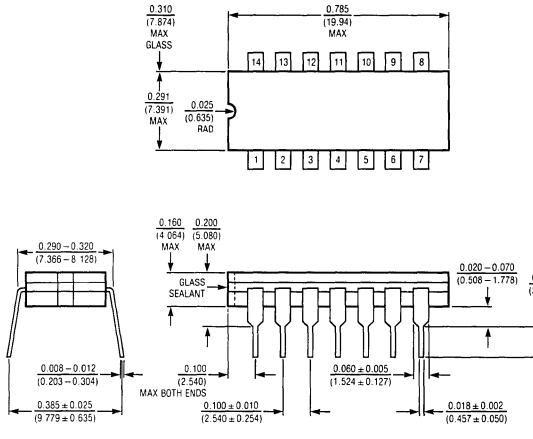
*LEVEL SHIFTING RESISTORS NEEDED FOR EACH INPUT

SIMPLIFIED SCHEMATIC

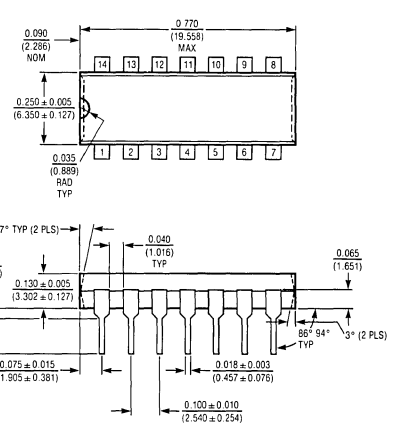


PACKAGE DESCRIPTION

J Package
14-Lead Hermetic DIP



N Package
14-Lead Plastic



	T_{jmax}	Θ_{jA}	Θ_{jC}
LT1032MJ	150°C	100°C/W	60°C/W
LT1032CJ	85°C	100°C/W	60°C/W
LT1032CN	85°C	100°C/W	60°C/W

SECTION 9—MILITARY PRODUCTS

SECTION 9—MILITARY PRODUCTS

LINEAR TECHNOLOGY MIL/JAN PRODUCTS

Linear Technology Corporation offers a comprehensive selection of precision voltage references, operational amplifiers, voltage regulators, comparators, and CMOS circuits designed specifically to serve the rigorous requirements of the military marketplace.

The company's specification system and quality procedures and policies were set up from the beginning to meet the exacting demands of MIL-Q-9858 (Quality Program Requirements), MIL-I-45208 (Inspection System Requirements), MIL-M-38510 (General Specification For Microcircuits) and MIL-STD-883 (Test Methods and Procedures For Microelectronics).

Compliance to these specifications is a statutory requirement for all employees at Linear Technology. The programs now in place that serve the varied requirements for ground, sea, air, and space applications include:

- JAN
- DESC Drawings
- Hi-Rel (SCD)
- 883

Linear Technology JAN

At the end of 1969, the Solid State Applications Branch of the Rome Air Development Center (RADC) issued the first copy of MIL-M-38510. This general specification for microcircuits established the procedures that a manufacturer must follow to have his products listed on the Qualified Parts List (QPL).

One major problem faced by defense contractors using semiconductor devices was the inability to interchange devices caused by a proliferation of non-standard electrical specifications. The 38510 (JAN) program addressed this problem by publishing detailed electrical specifications (slash sheets) for each component to be listed on the QPL.

JAN devices are completely processed in the United States or its territories and all wafer fabrication, wafer sort, assembly, testing, and conformance testing are performed onshore.

In early 1985, Linear Technology Corporation joined the ranks of the eighteen existing QPL suppliers. Of these eighteen, only a handful of suppliers participate in the linear military JAN market. Linear Technology believes its analog design experience and manufacturing strength can contribute significantly to this market.

In August 1984, Linear Technology Corporation was visited by a team of DESC (Defense Electronics and Supply Center) personnel. This team spent almost four days on their audit and at the end of the visit they awarded the company "line certification". *This was a first for any company to receive this distinction on a first audit!*

Linear Technology's first QPL listing was achieved in February, 1985, one year after the company made JAN Class B a corporate goal. Other companies have typically taken 2 to 3 years to achieve this status. The line certification and QPL approvals were awarded to the *new MIL-38510 Rev. F* and *MIL-STD-883 Rev. C* specifications.

Linear Technology's policy of providing JAN Class B linear components supports the United States Government's position of standardization to decrease the number of active part types maintained by DESC. This number is currently in excess of 70,000 for all types of components (contrasted to approximately 5,000 industry standard components). Standardization will clearly decrease costs and assist in the maintenance of military weapon systems and equipment now in the field. By the end of 1985, the company plans to have at least 6 devices on the Qualified Parts List and we have an active program to pursue more qualifications in the future.

EXAMPLES OF LINEAR TECHNOLOGY MILITARY PROGRAM PARTICIPATION

AMRAAM	SPARROW	PERSHING II
PHOENIX	HARPOON	MINUTEMAN
PHALANX	HARM	B-1B
F-15	COPPERHEAD	B-52
F-16	GPS	TOW
F-18	HTTB	MAVERICK
DRAGON	SEAHAWK	ACTS
STD. MISSILE	FLEET SATCOM	M-1 TANK

Linear Technology DESC Drawings

DESC drawings were initiated in 1976 to standardize the electrical requirements for full temperature-tested military components. These DESC drawings (or minispecs) were initially issued for low power Schottky devices (54LS) used by defense subcontractors on the Air Force's F16. The program accomplished standardization of testing, without the delays associated with the qualification process for JAN components.

The DESC drawing was viewed as a preliminary specification prior to JAN approval, and it ranks second in the order of purchasing hierarchy to JAN. This order is defined in Requirement 64 of MIL-STD-454. If a JAN part is available, it is still preferred, however, there are many types of devices where the volume is such that the cost of a full JAN qualification may not be justified, but where a need exists for electrical standardization.

CMOS and analog circuits were added to the DESC Drawing Program in 1977, 1978 and 1979, but widespread acceptance of these parts was not achieved. Today with more emphasis being placed on standardization, the interest level in DESC drawings has accelerated. This category of product can be built offshore with 883-level processing and the electrical parameters are tested specifically to the DESC drawing.

To provide parts to a DESC drawing, a manufacturer has to have at least one part on the 38510 Qualified Parts List. He must also provide DESC with a certificate of compliance agreeing to the tests and conditions listed on the drawing.

Linear Technology has a number of devices listed on DESC drawings, and we are actively supporting this program by having parts available off the shelf from Linear Technology Corporation and from distribution outlets.

Linear Technology Hi-Rel

Linear Technology Corporation recognizes the need for source controlled drawings (SCD's) and the company's DESC-certified line is well equipped to handle these requirements for hi-rel applications. The company has a comprehensive review procedure and emphasis is placed on compliance to test methods and procedures. Over 1,200 specifications have been reviewed to date with fast feedback to our customers.

Linear Technology has serviced source controlled drawing orders including "S" level specifications with a variety of source inspection and conformance test requirements. Each source controlled drawing requires dedicated flows, software and hardware, and as a result, certain minimum requirements have to be fulfilled. Linear Technology's Product Marketing group can provide you with more details on a case-by-case basis.

Linear Technology MIL-STD-883 Product

The semiconductor industry 883 designation on military semiconductor components established a defacto standard in response to a significant demand from the military defense contractors. The Government recognized the existence of 883 components in the recent revisions of MIL-STD-883C and MIL-M-38510F, and the requirements for compliant 883 components are now defined very specifically in these documents.

MIL-STD-883 is a test procedures and methods document and the lastest revision (Rev. C) became effective on June 1, 1984. Twenty-seven test methods were modified extensively and four new test methods were added. Class C product was eliminated leaving Class B and Class S. Class B is intended for applications where maintenance is difficult or expensive and where reliability is vital. Class S is intended for space and critical applications where replacement is extremely difficult or impossible and where reliability is imperative. The Class B PDA (Percent Defective Allowable) was tightened from 10% to 5% following burn-in and the Group A electrical sampling plans (LTPD levels) also were tightened. In addition, a critical paragraph was added to MIL-STD-883 to alleviate any misinterpretation; a factor that had previously created vastly different 883 programs throughout the semiconductor industry.

On December 31, 1984, another key clause was added to MIL-STD-883 Rev. C, "paragraph 1.2.1." This states that if a manufacturer advertises, certifies, or marks parts as compliant with MIL-STD-883 those parts must meet all of the provisions of MIL-STD-883, a practice consistent with "Truth in Advertising".

According to the Defense Electronics Supply Center (a branch of the Defense Department's Logistics Agency), the intent of paragraph 1.2.1 was to link MIL-STD-883 with the controls and details contained in MIL-M-38510.

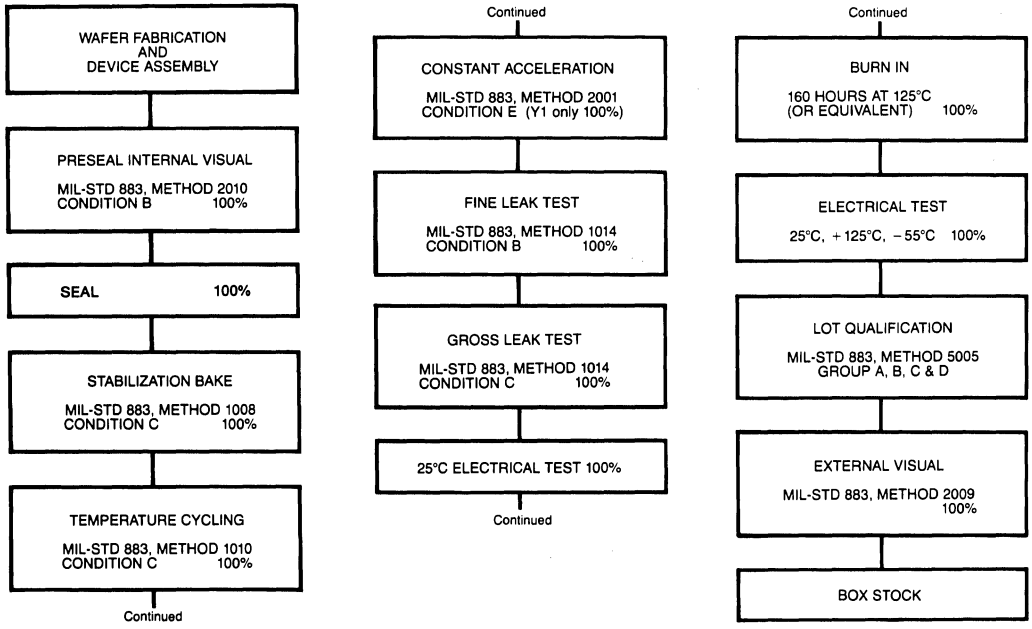
Linear Technology Corporation can state unequivocally that all of its 883 products are in full compliance with the new MIL-STD-883 Rev. C requirements. We have over 150 versions of our 883 products listed in our current catalog, including operational amplifiers, voltage regulators, voltage references, comparators, and our advanced line of proprietary CMOS circuits.

All products manufactured by Linear Technology are designed to meet the full requirements of the military, from –55°C to 125°C.

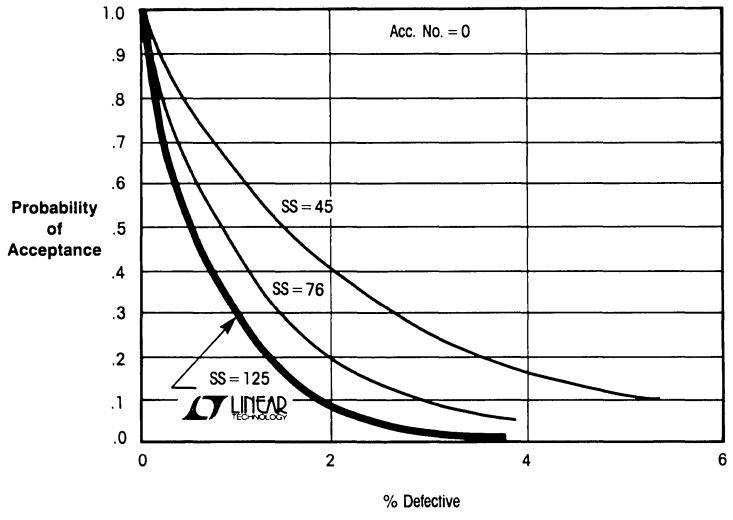
Military Market Commitment

Linear Technology Corporation is a focused, dedicated company servicing the needs of the linear military marketplace. We are shipping to the top U. S. defense electronics contractors who have qualified and approved our products. Linear Technology Corporation is committed to being the best and most proficient high quality supplier of analog military components.

883 PRODUCT FLOW — CLASS B



OC CURVES — TIGHTENED SAMPLING PLANS



LINEAR TECHNOLOGY 883 GROUP A SAMPLING PLAN

Test	Condition	Linear Technology			883C (Class B)	
		Sample Size	AQL	LTPD	Sample Size	LTPD
DC Parametric	T_A = 25°C	125	.04%	1.8%	116	2.0%
DC Parametric	T_A = −55°C +125°C	125	.04%	1.8%	45 76	5.0% 3.0%
AC Parametric	T_A = 25°C	125	.04%	1.8%	116	2.0%

Linear Technology Corporation uses a Group A sampling plan which *exceeds* the LTPD requirements of the present 883 specification. This ensures an even higher outgoing quality level of Linear Technology product, as is shown in the graph and table above.

Note (1) AQL defined at a 'Probability of Acceptance' of 95%.

883 CERTIFICATE OF CONFORMANCE

LTC Part Number _____

Customer ID _____

Purchase Order No. _____

Lot Traceability No. _____

Date Code(s) _____

QUALITY ASSURANCE ACCEPTANCE	
DATE	QA STAMP

LINEAR TECHNOLOGY CORPORATION HEREBY DECLARES THAT THE COMPONENTS SPECIFIED ON THE ABOVE PURCHASE ORDER COMPLY WITH THE PROVISIONS AND SPECIFICATIONS DEFINED BY THE LTC 883C PROGRAM. ALL SUPPORTING DOCUMENTATION AND RECORDS ARE RETAINED ON FILE BY LTC AND ARE AVAILABLE FOR INSPECTION. THE MAJOR ELEMENTS OF THE 883C PROGRAM ARE SHOWN BELOW:

Operation	Screening Procedure MIL-STD-883C Method 5004
Internal Visual	Method 2010 Condition B
Stabilization Bake	Method 1008 Condition C 24 hrs at 150°C
Temperature Cycling	Method 1010 Condition C 10 cycles −65°C to 150°C
Constant Acceleration	Method 2001 Condition E 30K G's Y, axis (TO-3 PKG at 20K G's)
Fine Leak	Method 1014 Condition B 5×10^{-8}
Gross Leak	Method 1014 Condition C
Burn-in	Method 1015 160 hrs at 125°C (or equivalent)
Final Electrical	+25°C DC per LTC Data Sheet PDA = 5% +125°C DC −55°C DC +25°C AC
QA Acceptance	Method 5005 Group A (sample/lot)
Quality Conformance	Group B (sample/lot) Group C (sample every 3 months/Generic Group) Group D (sample every 6 months/Package Type)
External Visual	Method 2009

NOTE: Each operation is performed on a 100% basis unless otherwise stated.

GROUP A DATA
Mil-Std 883, METHOD 5005

LTC P/N: _____ LOT #: _____
GENERIC TYPE: _____ PKG: _____ DATE CODE: _____
ASSEMBLY LOC: _____

	AQL =	ACC #	S/S	# FAILED	DATE TEST	OPER NUMBER
SUBGROUP 1 Static test at 25°C	.1%					
SUBGROUP 2 Static tests at maximum rated operating temperature	.1%					
SUBGROUP 3 Static tests at minimum rated operating temperature	.1%					
SUBGROUP 4 Dynamic tests at 25°C	.1%					
SUBGROUP 5 Dynamic tests at maximum rated operating temperature	.1%					
SUBGROUP 6 Dynamic tests at minimum rated operating temperature	.1%					
SUBGROUP 7 Functional tests at 25°C	SAME AS SUBGROUP #1					
SUBGROUP 8 Functional tests at maximum and minimum operating temperature	SAME AS SUBGROUPS 2 & 3					
SUBGROUP 9 Switching tests at 25°C	.1%					
SUBGROUP 10 Switching tests at maximum rated operating temperature	.1%					
SUBGROUP 11 Switching tests at minimum rated operating temperature	.1%					

QA APPROVAL: _____ DATE: _____

FORM No. 00-03-6037

GROUP B DATA
Mil-Std 883, METHOD 5005

LTC P/N: _____ LOT #: _____
GENERIC TYPE: _____ PKG: _____ DATE CODE: _____
ASSEMBLY LOC: _____

TEST	METHOD	CONDITION	LTPD	ACC #	S/S	# FAILED	DATE TESTED	OPER #
SUBGROUP 1 Physical Dimensions	2016			0	2			
SUBGROUP 2 Resistance to Solvents	2015			0	4			
SUBGROUP 3 Solderability	2003	Soldering Temp. of 245 ± 5°C	15					
SUBGROUP 4 Internal Visual/Mechanical	2014	design and construction requirements		0	1			
SUBGROUP 5 Bond Strength	2011	C or D	15					
SUBGROUP 7 Fine Leak Gross Leak	1014		5					

EXAMPLE

QA APPROVAL: _____ DATE: _____

FORM No. 00-03-6006

GROUP C DATA
Mil-Std 883, METHOD 5005

LTC P/N: _____ LOT # _____
GENERIC TYPE: _____ PKG: _____ DATE CODE: _____
CT. GROUP: _____

TEST	METHOD	CONDITION	LTPD	ACC #	S/S	# FAILED	DATE TESTED	OPER #
SUBGROUP 1 Steady State Life Test Electrical Endpoints	1005	T_A = 125°C (1000 Hours or Equiv.) Test #	5					
SUBGROUP 2 Temperature Cycling Constant Acceleration Fine Leak Gross Leak Visual Examination Electrical Endpoints	1010 2001 1014 1014 1010 1011 Test #	C E Y1 only	15					

EXAMPLE

QA APPROVAL: _____ DATE: _____

FORM No. 00-03-6007

GROUP D DATA
Mil-Std 883, METHOD 5005

LTC P/N: _____ LOT #: _____
GENERIC TYPE: _____ PKG: _____ DATE CODE: _____
ASSEMBLY LOC: _____

TEST	METHOD	CONDITION	LTPD	ACC #	S/S	# FAILED	DATE TESTED	OPER #
SUBGROUP 1			15					
Physical Dimensions	2016							
SUBGROUP 2			15					
Lead Integrity	2004	B2 (lead fatigue)						
Fine Leak	1014							
Gross Leak	1014							
SUBGROUP 3			15					
Thermal Shock	1011	B 15 cycles						
Temperature Cycle	1010	C 100 cycles						
Moisture Resistance	1004							
Fine Leak	1014							
Gross Leak	1014							
Visual Examination	1004/ 1010							
Electrical Endpoints		Test #						
SUBGROUP 4			15					
Mechanical Shock	2002	B						
Vibration Variables-Frequency	2007	A						
Constant Acceleration	2001	E Y1 only						
Fine Leak	1014							
Gross Leak	1014							
Visual Examination	1010/ 1011							
Electrical Endpoints		Test #						
SUBGROUP 5			15					
Salt Atmosphere	1009	A						
Fine Leak	1014							
Gross Leak	1014							
Visual Examination	1009	Visual Criteria						
SUBGROUP 6				0	3			
Internal Water-Vapor	1018	5000ppm Max water content @ 100°C						
SUBGROUP 7			15					
Adhesion of Lead Finish	2025							
SUBGROUP 8				0	5			
Lid Torque	2024	Glass Frit Seal only						

QA APPROVAL: _____ DATE: _____

FORM No. 00-03-6008

MILITARY PARTS LIST

JAN QPL†

JM38510/10104BGA	JM38510/10107BGC	JM38510/11405BGA*	JM38510/13501BPA*
JM38510/10104BGC	JM38510/10107BPA*	JM38510/11405BGC*	JM38510/13502BGA*
JM38510/10104BPA*	JM38510/11402BGA*	JM38510/13501BGA*	JM38510/13502BGC*
JM38510/10106BEA*	JM38510/11402BGC*	JM38510/13501BGC*	JM38510/13502BPA*
JM38510/10106BEC*			
JM38510/10107BGA			

DESC Drawings

7703401XA	7703401YA	7703402XX	7802801EA
7703401XC	7703401YX	7703402YA	7802801EX
7703401XX			

883 Operational Amplifiers

LF155AH/883B	LM118J8/883B	LT1022AMH/883B	OP-07AJ8/883B
LF155H/883B	LT118AH/883B	LT1022MH/883B	OP-07H/883B
LF156AH/883B	LT118AJ8/883B	LT1023MH/883B	OP-07J8/883B
LF156H/883B	LT1001AMH/883B	LT1023MJ8/883B	OP-15AH/883B
LF198AH/883B	LT1001AMJ8/883B	LT1024AMD/883B	OP-15BH/883B
LF198H/883B	LT1001MH/883B	LT1024MD/883B	OP-15CH/883B
LH0070-0H/883B	LT1001MJ8/883B	LT1037AMH/883B	OP-16AH/883B
LH0070-1H/883B	LT1002AMJ/883B	LT1037AMJ8/883B	OP-16BH/883B
LH0070-2H/883B	LT1002MJ/883B	LT1037MH/883B	OP-16CH/883B
LH2108AD/883B	LT1007AMH/883B	LT1037MJ8/883B	OP-27AH/883B
LH2108D/883B	LT1007AMJ8/883B	LT1055AMH/883B	OP-27AJ8/883B
LM10H/883B	LT1007MH/883B	LT1055MH/883B	OP-27CH/883B
LM10J8/883B	LT1007MJ8/883B	LT1056AMH/883B	OP-27CJ8/883B
LM101AH/883B	LT1008MH/883B	LT1056MH/883B	OP-37AH/883B
LM101AJ8/883B	LT1012MD/883B	LTC1052MH/883B	OP-37AJ8/883B
LM107H/883B	LT1012MH/883B	LTC1052MJ/883B	OP-37CH/883B
LM107J8/883B	LT1013AMH/883B	LTC1052MJ8/883B	OP-37CJ8/883B
LM108AH/883B	LT1013AMJ8/883B	OP-05AH/883B	OP-227AJ/883B
LM108H/883B	LT1013MH/883B	OP-05AJ8/883B	OP-227CJ/883B
LM108AJ8/883B	LT1013MJ8/883B	OP-05H/883B	OP-237AJ/883B
LM108J8/883B	LT1014AMJ/883B	OP-05J8/883B	OP-237CJ/883B
LM118H/883B	LT1014MJ/883B	OP-07AH/883B	

883 Regulators

LM117H/883B	LM137HVK/883B	LT117AK/883B	LT150AK/883B
LM117HVH/883B	LM137K/883B	LT123AK/883B	LT1003MK/883B
LM117HVK/883B	LM138K/883B	LT137AH/883B	LT1005MK/883B
LM117K/883B	LM150K/883B	LT137AHVH/883B	LT1033MK/883B
LM123K/883B	LT117AH/883B	LT137AHVK/883B	LT1035MK/883B
LM137H/883B	LT117AHVH/883B	LT137AK/883B	LT1036MK/883B
LM137HVH/883B	LT117AHVK/883B	LT138AK/883B	LT1038MK/883B

883 References

AD580SH/883B	LM185H-1.2/883B	LT1019AMH-10/883B	LT1021DMH-10/883B
AD580TH/883B	LM185H-2.5/883B	LT1019MH-2.5/883B	LT1029AMH/883B
AD580UH/883B	LM199AH/883B	LT1019MH-5.0/883B	LT1029MH/883B
AD581SH/883B	LM199AH-20/883B	LT1019MH-6.2/883B	LT1031BMH/883B
AD581TH/883B	LM199AH-50/883B	LT1019MH-10/883B	LT1031CMH/883B
AD581UH/883B	LM199H/883B	LT1021BMH-5/883B	LT1031DMH/883B
LM129AH/883B	LT1004MH-1.2/883B	LT1021CMH-5/883B	LT1034BMH/883B
LM129BH/883B	LT1004MH-2.5/883B	LT1021DMH-5/883B	LT1034MH/883B
LM129CH/883B	LT1009MH/883B	LT1021BMH-7/883B	REF-01AH/883B
LM134H/883B	LT1019AMH-2.5/883B	LT1021DMH-7/883B	REF-01H/883B
LM136AH-2.5/883B	LT1019AMH-5.0/883B	LT1021BMH-10/883B	REF-02AH/883B
LM136H-2.5/883B	LT1019AMH-6.2/883B	LT1021CMH-10/883B	REF-02H/883B

883 Comparators

LM111H/883B	LT111AJ8/883B	LT1011MH/883B	LT1017MJ8/883B
LM111J8/883B	LT119AH/883B	LT1011MJ8/883B	LT1018MH/883B
LM119H/883B	LT119AJ/883B	LT1016MH/883B	LT1018MJ8/883B
LM119J/883B	LT1011AMH/883B	LT1016MJ8/883B	
LT111AH/883B	LT1011AMJ8/883B	LT1017MH/883B	

Other 883

LF198AH/883B	LT1525AJ/883B	LTC1044MJ8/883B	SG1524J/883B
LF198H/883B	LT1526J/883B	LTC1059AMJ/883B	SG1525AJ/883B
LT1010MH/883B	LT1527AJ/883B	LTC1059MJ/883B	SG1527AJ/883B
LT1010MK/883B	LTC1040MJ/883B	LTC1060AMJ/883B	UC1846J/883B
LT1020MJ/883B	LTC1041MJ8/883B	LTC1060MJ/883B	UC1847J/883B
LT1032MJ/883B	LTC1043MD/883B	LTC1061MJ/883B	
LT1524J/883B	LTC1044MH/883B	LTC1062MJ8/883B	

*JAN QPL qualification expected to be completed by December 31, 1985.
†Parts may be ordered using an "X" lead finish suffix. These parts will be supplied with either gold plate or solder-dip lead finish, at Linear Technology Corporation's discretion.

SECTION 10— NEW PRODUCTS

SECTION 10—NEW PRODUCTS

LT1020

Micropower Regulator and Comparator

FEATURES

- 40μA Supply Current
- 125mA Output Current
- 2.5V Reference Voltage
- Reference Output Sources 1mA and Sinks 0.5mA
- Dual Output Comparator
- Comparator Sinks 10mA
- Dropout Detector
- 0.2V Dropout Voltage
- Thermal Limiting

APPLICATIONS

- Battery Systems
- Battery Backup System
- Portable Terminals
- Portable Instruments

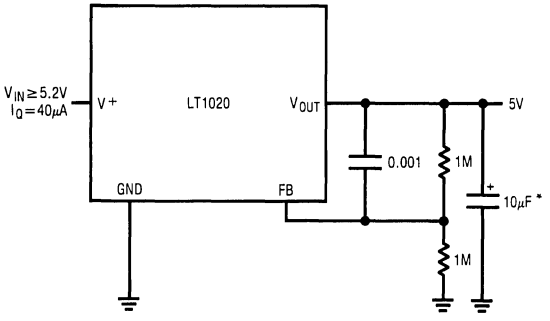
DESCRIPTION

The LT1020 is a combination micropower positive regulator and free collector comparator on a single monolithic chip. With only 40μA supply current, the LT1020 can supply over 125mA of output current. Input voltage range is from 5V to over 36V and dropout voltage is 0.6V at 125mA. Dropout decreases with lower load currents. Also included on the chip is a class B output 2.5V reference that can either source or sink current. A dropout detector provides an output current to indicate when the regulator is about to drop out of regulation.

The dual output comparator can be used as a comparator for system or battery monitoring. For example, the comparator can be used to warn of low system voltage while the dropout detector shuts down the system to prevent abnormal operation. Frequency compensation of the comparator for amplifier applications can be obtained by adding external output capacitance. Dual output or positive and negative regulators can also be made.

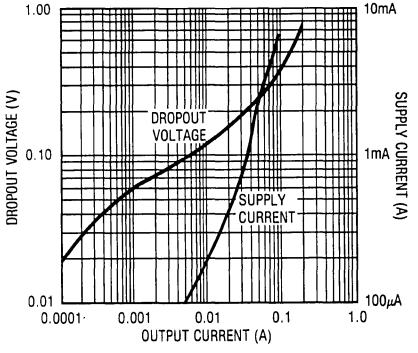
TYPICAL APPLICATIONS

5V Regulator



*A 10μF OR GREATER OUTPUT CAPACITOR IS NEEDED FOR FREQUENCY COMPENSATION

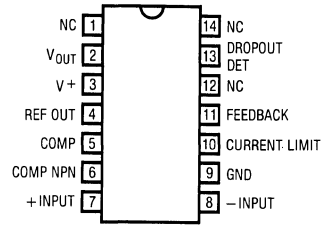
Dropout Voltage and Supply Current



ABSOLUTE MAXIMUM RATINGS

Input Voltage 36V
NPN Collector Voltage 36V
PNP Collector Voltage ..... Positive Supply – 36V
Output Short Circuit Duration ..... Indefinite
Power Dissipation ..... Internally Limited
Operating Temperature Range
LT1020C ..... 0°C to 100°C
LT1020M ..... – 55°C to 125°C
Storage Temperature Range
LT1020C,M ..... – 65°C to 150°C

PACKAGE/ORDER INFORMATION

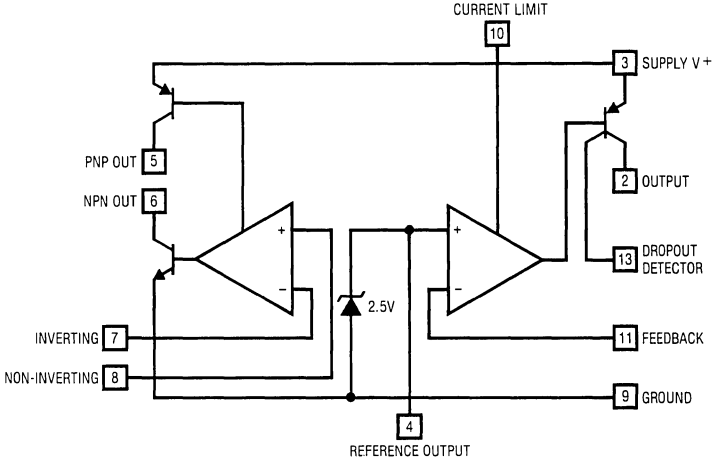


ORDER PART NUMBER
LT1020MJ LT1020CJ LT1020CN

ELECTRICAL CHARACTERISTICS

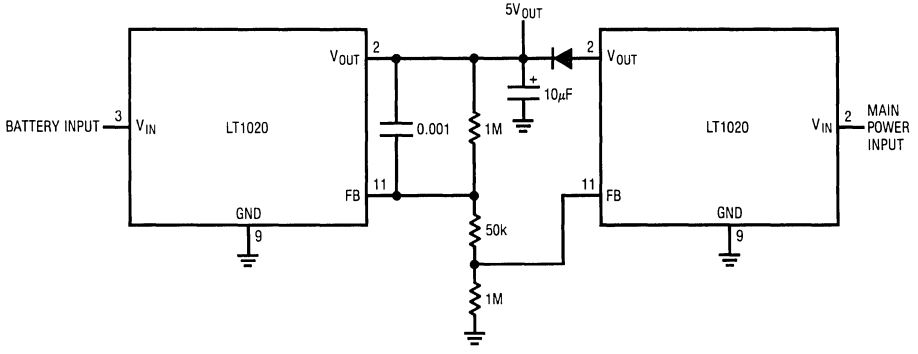
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Reference					
Reference Voltage	$V_{IN} = 10V$		2.5		V
Line Regulation	$7V \le V_{IN} \le 36V$		0.01		%/V
Load Regulation	$I_{OUT} = 1mA$		0.3		%
Output Source Current	$V_{IN} \ge 5V$		5		mA
Output Sink Current			2		mA
Temperature Stability			1		%
Regulator					
Supply Current	$V_{IN} = 10V$, $I_{OUT} \le 100\mu A$		40		μA
Output Current	$(V_{OUT} - V_{IN}) \ge 1V$		125		mA
Load Regulation	$(V_{OUT} - V_{IN}) \ge 1V$		0.2		%
Line Regulation	$6V \le V_{IN} \le 36V$		0.01		%
Dropout Voltage	$I_{OUT} = 100\mu A$ $I_{OUT} = 125mA$		0.02 0.5		V V
Feedback Sense Voltage	$V_{IN} = 10V$, $I_{OUT} = 100\mu A$		2.5		V
I Dropout Detector	$I_{OUT} = 100\mu A$, $V_{DIFF} = 0.03V$		5		μA
Feedback Bias Current			15		nA
Minimum Load Current	$T_J = 125°C$		30		μA
Short Circuit Current	 Pin 9 and Pin 10 Shorted		250 40		mA mA
Comparator					
Offset Voltage	$V_{CM} = 2.5V$		3		mV
Bias Current	$V_{CM} = 2.5V$		40		nA
Offset Current			4		nA
Gain-NPN Pulldown	$I_{OUT} = 1mA$		10000		V/V
Output Current Sink			10		mA
Output Current Source			80		μA
Input Voltage Range		0		$V^+ - 1$	V
Response Time			5		μs

BLOCK DIAGRAM

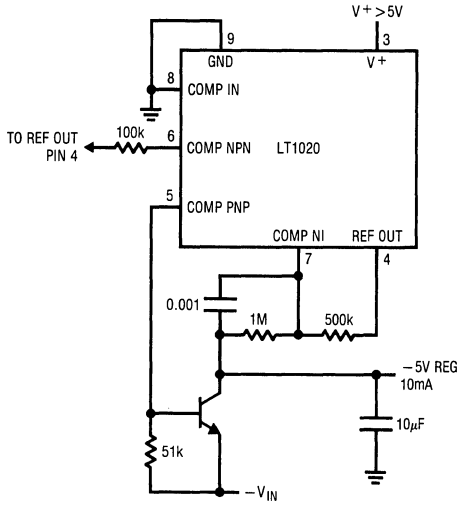


TYPICAL APPLICATIONS

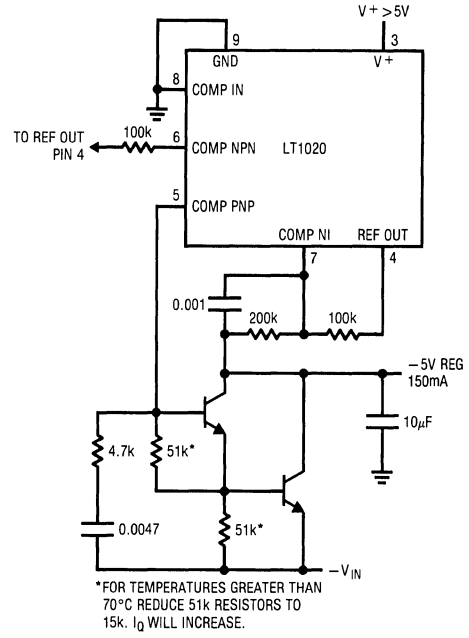
Battery Backup Regulator



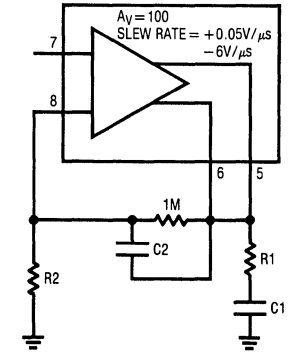
Dual Output Regulator



Dual Output 150mA Regulator

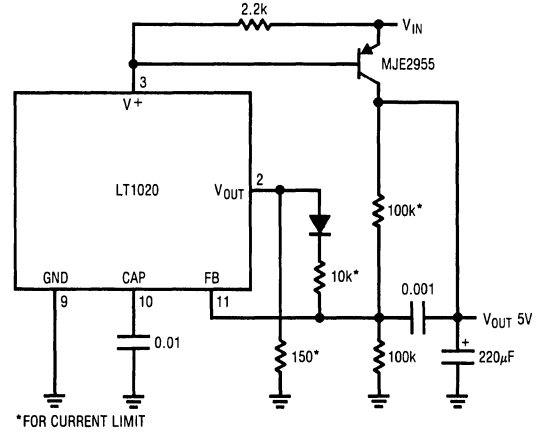


Compensating the Comparator as an Op-Amp



A_V	R1	C1	C2	R2
1	33Ω	0.1μF	0.001μF	—
10	100Ω	0.047μF	—	100k
100	10k	0.002μF	—	10k

1 Amp Low Dropout Regulator



LT1023

DAC Output Amplifier

FEATURES

- 3μS Settling Time
- 1mV Offset Voltage
- 100nA Bias Current
- 18V/μS Slew Rate
- 3MHz Gain Bandwidth

APPLICATIONS

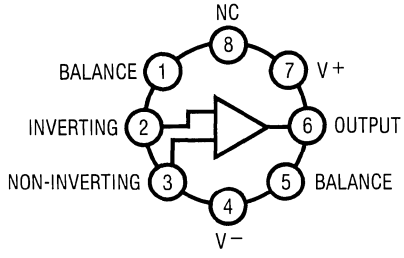
- DAC Output Amplifier
- Fast Inverting Amplifier

DESCRIPTION

The LT1023 is a fast inverting op amp with 18V/μS slew rate as well as good DC characteristics. Designed as a DAC output amplifier, the LT1023 settles to 0.1% of a 10V step in a maximum of 3μS. The low offset voltage and drift eliminate the need for adjustments in most applications.

Other applications for the LT1023 are fast inverters, oscillators, or audio. Available in packages or dice for hybrids the LT1023 is compatible with the OP-01.

PIN CONNECTIONS



LT1025

Thermocouple Cold Junction Compensator

FEATURES

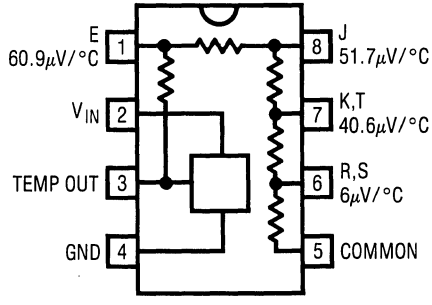
- 1°C Accuracy
- Compensates for E, J, K, R, S, T Thermocouples
- 50μA Operating Current
- Operates from 3.5V to 40V

DESCRIPTION

The LT1025 is a monolithic temperature sensor designed to cold-junction compensate a variety of thermocouples. Accuracy is better than 1°C. A 10mV°C output is provided from the sensing circuitry to a precision thin film divider network. High output accuracy is maintained over a 0°C to 60°C range.

APPLICATIONS

- Temperature Measurement
- Controllers
- Sensing



LT1028

Ultra-Low Noise, High Speed Op Amp

FEATURES

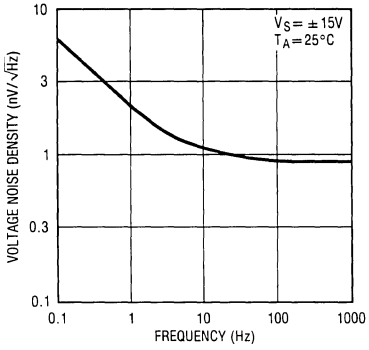
- Voltage Noise @ 1kHz — 0.9nV/$\sqrt{Hz}$ typ.
- Voltage Noise @ 10Hz — 1.1nV/$\sqrt{Hz}$ typ.
- Slew Rate — 15V/μs typ.
- Offset Voltage — 15μV typ.
- Bias Current — 15nA typ.
- Voltage Gain — 5 million typ.

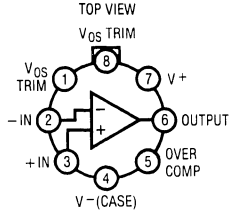
DESCRIPTION

The LT1028 achieves a new low in noise performance with 0.9nV/$\sqrt{Hz}$ 1kHz noise, and 35nV peak-to-peak noise from 0.1Hz to 10Hz. This ultra-low noise is combined with excellent high speed specifications (gain bandwidth product is 65MHz), distortion free output, and true precision parameters (0.2μV/°C drift). Although the LT1028 input stage operates at 1mA of collector currents to achieve low noise, input bias current is only 15nA.

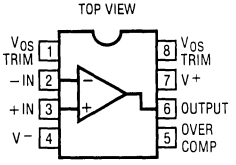
The LT1028's voltage noise is less than the noise of a 50Ω resistor. Therefore, even in very low source impedance transducer or audio amplifier applications, the LT1028's contribution to total system noise will be negligible.

Voltage Noise vs Frequency





METAL CAN H PACKAGE



HERMETIC DIP J8 PACKAGE
PLASTIC DIP N8 PACKAGE

LT1030

Quad Low Power Line Driver

FEATURES

- Low Operating Voltage ±5V to ±15V
- 500μA Supply Current
- Zero Supply Current when Shut Down
- Outputs Can Be Driven ±30V
- Thermal Limiting
- Output "Open" when Off
- 10mA Output Drive
- Pin Compatible with 1488

APPLICATIONS

- RS232 Driver
- Power Supply Inverter
- Micropower Interface
- Level Translator

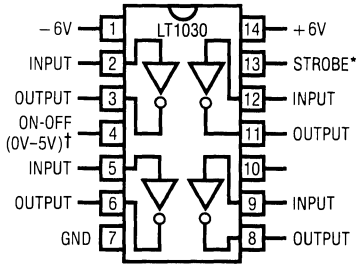
DESCRIPTION

The LT1030 is an RS232 line driver that operates over a ±5V to ±15V range on low supply current and can be shut down to zero supply current. Outputs are fully protected from externally applied voltages of ±30V by current limiting. Since the output swings to within 200mV of the positive supply and 1V of the negative supply, power supply needs are minimized.

A major advantage of the LT1030 is the high impedance output state when off or powered down.

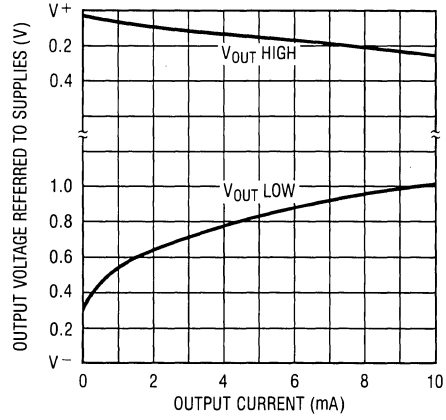
TYPICAL APPLICATION

RS232 Line Driver



*NO CONNECTION NEEDED WHEN NOT USED.
†5V = ON.

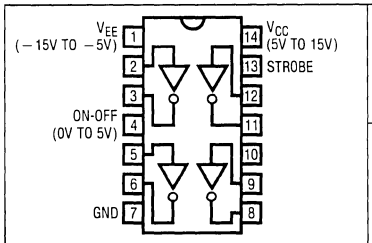
Output Swing vs Output Current



ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... ±15V
Logic Input Pins ..... V^- to 25V
On-Off Pin ..... GND to 12V
Output (Forced) ..... $V^- + 30V$, $V^+ - 30V$
Short Circuit Duration (to ±30V) ..... Indefinite
Operating Temperature Range
LT1030M ..... −55°C to 125°C
LT1030C ..... 0°C to 70°C
Guaranteed Functional by Design ... −25°C to 85°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



J PACKAGE 14-PIN HERMETIC
N PACKAGE 14-PIN PLASTIC

ORDER PART NUMBER

LT1030MJ
LT1030CJ
LT1030CN

ELECTRICAL CHARACTERISTICS (Supply Voltage = ±5V to ±15V)

PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
Supply Current	$V_{ON/OFF} \geq 2.4V$, $I_{OUT} = 0$, All Outputs Low		●		500	1000	μA
Power Supply Leakage Current	$V_{ON-OFF} \leq 0.4V$				1	10	μA
	$V_{ON-OFF} \leq 0.1V$, $T_A = 125°C$		●		10	100	μA
Output Voltage Swing	Load = 2mA	Positive		$V^+ - 0.3V$	$V^+ - 0.1V$		V
		Negative			$V^- + 0.7V$		V
Output Current	V_{SUPPLY} ±5V to ±15V			5	12		mA
Output Overload Voltage (Forced)	Operating or Shutdown		●	$V^+ - 30V$		$V^- + 30V$	V
Output Current	Shutdown	$V_{OUT} = \pm 30V$			2	100	μA
Input Overload Voltage (Forced)	Operating or Shutdown		●	V^-		30V	V
Logic Input Levels	Low Input (V_{OUT} = High)		●		1.4	0.8	V
	High Input (V_{OUT} = Low)		●	2	1.4		V
Logic Input Current	$V_{IN} > 2.0V$				2	20	μA
	$V_{IN} < 0.8V$				10	20	μA
On-Off Pin Current	$0 \leq V_{IN} \leq 5V$		●	−10	3	50	μA
Slew Rate	$I_{RESPONSE} = 0$			4	15	30	V/μS

The ● denotes specifications which apply over the operating temperature range.

Note 1: 3V applied to the strobe pin will force all outputs low. Strobe pin input impedance is about 2k to ground. Leave open when not used.

Note 2: Response can be changed by connecting a resistor to the supply. For supplies less than ±6V this current is disconnected when shut down. Leave open when not used.

PIN FUNCTIONS

PIN	FUNCTION	COMMENT
1	Minus Supply	Operates −2V to −15V
2,5,9,12	Logic Input	Operates properly on TTL or CMOS levels. Output valid from $(V^- + 2V) \leq V_{IN} \leq 15V$. Connect to ground when not used.
3,6,8,11	Output	Line drive output.
4	On-Off	Shuts down entire circuit. Cannot be left open. For "normally on" operation, connect 5V to 10V.
7	Ground	Ground must be more positive than V^-
13	Strobe	Forces all outputs low. Drive with 3V.

LT1039

Triple RS232 Line Driver and Receiver

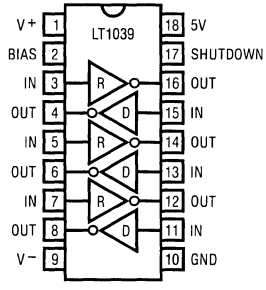
FEATURES

- Three Drivers and Receivers
- Low Power
- Shuts Down to Zero Power
- High Impedance Output When Off
- Operates ±5V to ±15V
- Wide Output Swing
- "Keep-Alive" Bias Point
- Overload Protected

APPLICATIONS

The LT1039 is a triple RS232 line driver and line receiver featuring low supply current and shutdown. Operating from ±5V to ±15V, the LT1039 has wide output swing minimizing the supply requirements. Outputs can be overdriven up to ±30V. The receiver accepts standard RS232 levels up to ±30V input. The receiver output is compatible with CMOS or TTL.

Two unique features available on the LT1039 make it more useful. The shutdown completely turns off the LT1039 decreasing supply current to zero. Also, the output goes to a high impedance state allowing devices to be paralleled. A bias pin allows one of the receivers to be powered up while the rest of the LT1039 is shut down. This receiver could then be used to power up the rest of the LT1039 in response to an external control.



LT1057/LT1058

Dual, JFET Input, Precision High Speed Op Amp
Quad, JFET Input, Precision High Speed Op Amp

FEATURES

- 13V/μs Slew Rate
- 5MHz Gain Bandwidth Product
- 250μV Offset Voltage (LT1073)
- 500μV Offset Voltage (LT1074)
- 2μV/°C Drift
- 80pA Bias Current at 70°C

DESCRIPTION

The LT1057 is a matched JFET input dual op amp in the industry standard 8 pin DIP configuration, featuring a combination of outstanding high speed and precision specifications. It replaces all the popular bipolar and JFET input dual op amps. In particular, the LT1057 upgrades the performance of systems using the LF412A and OP-215 JFET input duals.

The LT1058 is the first precision quad JFET input operational amplifier in the standard 14 pin DIP configuration. It offers significant accuracy improvements over presently available JFET input quad operational amplifiers.

LT1070

5A High Efficiency Switching Regulator

FEATURES

- Wide Input Voltage Range 3V-60V
- Low Quiescent Current—6mA
- Internal 5A Switch
- Very Few External Parts Required
- Self-Protected Against Overloads
- Operates in Nearly All Switching Topologies
- Shutdown Mode Draws Only 50μA Supply Current
- Flyback-Regulated Mode has Fully Floating Outputs
- Comes in Standard 5-Pin Packages

APPLICATIONS

- Logic Supply 5V @ 10A
- +5V Logic to ±15V Op Amp Supply
- Offline Converter up to 200W
- Battery Upconverter
- Power Inverter (+ to −) or (− to +)
- Fully Floating Multiple Outputs

DESCRIPTION

The LT1070 is a monolithic high power switching regulator. It can be operated in all standard switching configurations including buck, boost, flyback, forward, inverting and "Cuk". A 5 amp high efficiency switch is included on the die along with all oscillator, control, and protection circuitry. Integration of all functions allows the LT1070 to be built in a standard 5-pin TO-3 or TO-220 power package. This makes it extremely easy to use and provides "bust proof" operation similar to that obtained with 3-pin linear regulators.

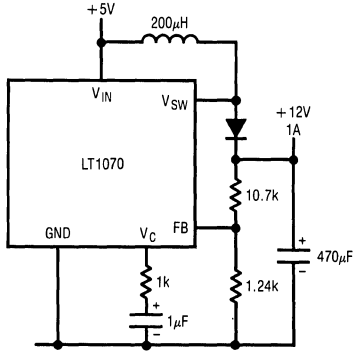
The LT1070 operates with supply voltages from 3V to 60V, and draws only 6mA quiescent current. It can deliver load power up to 100 watts with no external power devices. By utilizing current-mode switching techniques, it provides excellent AC and DC load and line regulation.

The LT1070 has many unique features not found even on the vastly more difficult to use low power control chips presently available. It uses adaptive anti-sat switch drive to allow very wide ranging load currents with no loss in efficiency. An externally activated shutdown mode reduces total supply current to 50μA for standby operation. Totally isolated and regulated outputs can be generated by using the optional "flyback regulation mode" built into the LT1070, without the need for opto-couplers or extra transformer windings.

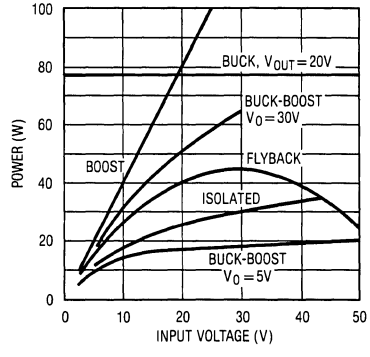
The LT1070 can also be used as an off-line converter by driving an external MOSFET, with power levels up to 300W.

TYPICAL APPLICATION

Up Converter (5V to +12V)



Maximum Output Power



ABSOLUTE MAXIMUM RATINGS

Supply Voltage
- LT1070HV 60V
- LT1070 ..... 40V

Switch Output Voltage
- LT1070HV 75V
- LT1070 ..... 65V

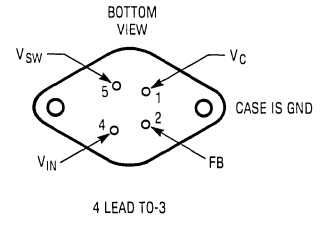
Feedback Pin Voltage (Transient, 1ms) ..... ±15V

Operating Junction Temperature Range
- LT1070MHV, LT1070M ..... –55°C to +150°C
- LT1070CHV, LT1070C ..... 0°C to +100°C

Storage Temperature Range
- LT1070MHV, LT1070M ..... –65°C to +150°C
- LT1070CHV, LT1070C ..... –65°C to +150°C

Lead Temperature (Soldering, 10sec) ..... 300°C

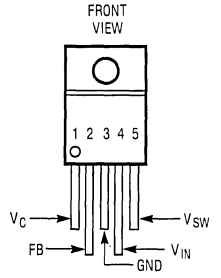
PACKAGE/ORDER INFORMATION



4 LEAD TO-3

ORDER PART NUMBER

LT1070MHVK
LT1070MK
LT1070CHVK
LT1070CK



5 LEAD TO-220

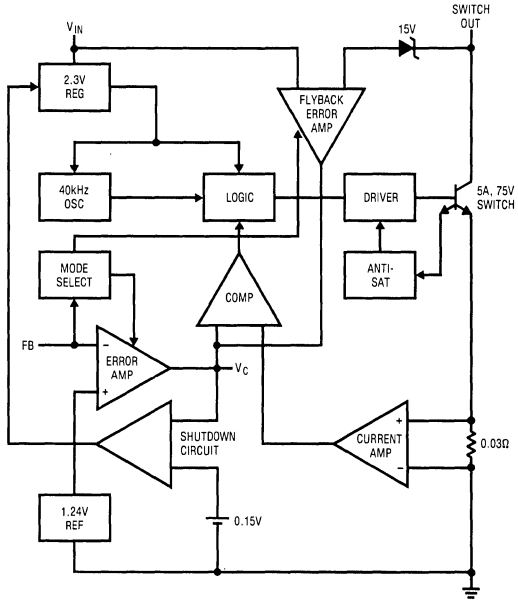
LT1070CHVT
LT1070CT

ELECTRICAL CHARACTERISTICS

V_{IN} = 15V, T_j = 25°C unless noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage Range	LT1070HV LT1070	3 3		60 40	V V
Quiescent Supply Current	$3V \le V_{IN} \le V_{MAX}$		6	9	mA
Switch Breakdown Voltage	LT1070HV LT1070	75 65	90 80		V V
Peak Switch Current (Internally Limited)	Duty Cycle ≤ 50% Duty Cycle = 80%	6 5	9 8		A A
Switch On Resistance	I_{SWITCH} = 5A		0.13	0.2	Ω
Switch Duty Cycle		0		95	%
Load Regulation			0.1	0.3	%
Line Regulation			0.02	0.05	%/V
Switching Frequency		36	40	44	kHz
Operating Efficiency	Buck or Boost Mode		90		%
Reference Voltage		1.220	1.244	1.268	V
Feedback Pin Bias Current			200	500	nA

BLOCK DIAGRAM



LT1070 OPERATION

The LT1070 is a current mode switcher. This means that switch duty cycle is directly controlled by switch current rather than by output voltage. Referring to the block diagram, the switch is turned "ON" at the start of each oscillator cycle. It is turned "OFF" when switch current reaches a predetermined level. Control of output voltage is obtained by using the output of a voltage sensing error amplifier to set current trip level. This technique has several advantages. First, it has immediate response to input voltage variations, unlike ordinary switchers which have notoriously poor line transient response. Second, it eliminates the 90° phase shift at midfrequencies in the energy storage inductor. This greatly simplifies closed loop frequency compensation under widely varying input voltage or output load conditions. Finally, it allows simple pulse-by-pulse current limiting to provide maximum switch protection under output overload or short conditions. A low-dropout internal regulator provides a 2.3V supply for all internal circuitry on the LT1070. This low-dropout design allows input voltage to vary from 2.5V to 60V with virtually no change in device performance. A 40kHz oscillator is the basic clock for all internal timing. It turns "ON" the output switch via the logic and driver circuitry. Special adaptive anti-sat circuitry detects onset of saturation in the power switch and adjusts driver current instantaneously to limit switch saturation. This minimizes driver dissipation and provides very rapid turn-off of the switch.

A 1.2V bandgap reference biases the positive input of the error amplifier. The negative input is brought out for output voltage sensing. This feedback pin has a second function; when pulled low with an external resistor, it programs the LT1070 to disconnect the main error amplifier output and connects the output of the flyback amplifier to the comparator input. The LT1070 will then regulate the value of the flyback pulse with respect to the supply voltage. This flyback pulse is directly proportional to output voltage in the traditional transformer coupled flyback topology regulator. By regulating the amplitude of the flyback pulse, the output voltage can be regulated with no direct connection between input and output. The output is fully floating up to the breakdown voltage of the transformer windings. Multiple floating outputs are easily obtained with additional windings. A special delay network inside the LT1070 ignores the leakage inductance spike at the leading edge of the flyback pulse to improve output regulation.

LT1070 OPERATION

The error signal developed at the comparator input is brought out externally. This pin (V_C) has four different functions. It is used for frequency compensation, current limit adjustment, soft starting, and total regulator shutdown. During normal regulator operation this pin sits at a voltage between 0.9V (low output current) and 2.0V (high output current). The error amplifiers are current output (Gm) types, so this voltage can be externally clamped for adjusting current limit. Likewise, a capacitor coupled external clamp will provide soft start. Switch duty cycle goes to zero if the V_C pin is pulled to ground through a diode, placing the LT1070 in an idle mode. Pulling the V_C pin below 0.15V causes total regulator shutdown, with only 50μA supply current for shutdown circuitry biasing.

LINEAR TECHNOLOGY

PRELIMINARY

LT1071

2.5A High Efficiency Switching Regulator

FEATURES

- Wide Input Voltage Range 3V-60V
- Low Quiescent Current—6mA
- Internal 2.5A Switch
- Very Few External Parts Required
- Self-Protected Against Overloads
- Operates in Nearly All Switching Topologies
- Shutdown Mode Draws Only 50μA Supply Current
- Flyback-Regulated Mode has Fully Floating Outputs
- Comes in Standard 5-Pin Packages

APPLICATIONS

- Logic Supply 5V @ 5A
- +5V Logic to ±15V Op Amp Supply
- Offline Converter up to 100W
- Battery Upconverter
- Power Inverter (+ to −) or (− to +)
- Fully Floating Multiple Outputs

DESCRIPTION

The LT1071 is a monolithic high power switching regulator. It can be operated in all standard switching configurations including buck, boost, flyback, forward, inverting and "Cuk". A 2.5 amp high efficiency switch is included on the die along with all oscillator, control, and protection circuitry. Integration of all functions allows the LT1071 to be built in a standard 5-pin TO-3 or TO-220 power package. This makes it extremely easy to use and provides "bust proof" operation similar to that obtained with 3-pin linear regulators.

The LT1071 operates with supply voltages from 3V to 60V, and draws only 6mA quiescent current. It can deliver load power up to 50 watts with no external power devices. By utilizing current-mode switching techniques, it provides excellent AC and DC load and line regulation.

The LT1071 has many unique features not found even on the vastly more difficult to use low power control chips presently available. It uses adaptive anti-sat switch drive to allow very wide ranging load currents with no loss in efficiency. An externally activated shutdown mode reduces total supply current to 50μA for standby operation. Totally isolated and regulated outputs can be generated by using the optional "flyback regulation mode" built into the LT1071, without the need for opto-couplers or extra transformer windings.

The LT1071 can also be used as an off-line converter by driving an external MOSFET, with power levels up to 150W.

PRELIMINARY

LTC1045

Hex Universal Level Translator (ULT™)/RS232 Receiver

FEATURES

- Programmable Power/Speed
- Translate Any Input Voltage to Any Output Voltage
- Power Can Be Completely Shut Off
- Three-State Outputs
- Output Latch Included

DESCRIPTION

The LTC1045 is a CMOS circuit consisting of six high speed comparators with output latches and three-state capability. The comparator's bias current can be easily programmed, with an external resistor, to trade off power consumption and speed. When power is shut off the outputs are latched and continuously available.

With external current limit resistors the inputs can be driven above and below the power supplies making the LTC1045 ideal for us as an RS232 line receiver.

ULT™ is a trademark of Linear Technology Corp.

LTC1061

High Performance Triple Universal Filter Building Block

FEATURES

- Up to 6th Order Filter Functions with a Single 20 Pin 0.3″ Wide Package
- Center Frequency Range up to 35kHz
- $f_0 \times Q$ Product Up to 1 MHz
- *Guaranteed* Center Frequency and Q Accuracy Over Temperature
- *Guaranteed* Low Offset Voltages Over Temperature
- 90dB Dynamic Range
- Filter Operates From Single 4.7V Supply and Up to ±8V Supplies
- *Guaranteed* Filter Specifications with ±5V Supply and ±2.37V Supply
- Low Power
- Clock Inputs T^2L and CMOS Compatible

APPLICATIONS

- High Order, Wide Frequency Range Bandpass, Lowpass, Notch Filters
- Low Power Consumption, Single 5V Supply Clock Tunable Filters
- Tracking Filters

DESCRIPTION

The LTC1061 consists of three high performance, universal filter building blocks. Each filter building block together with an external clock and 2 to 5 resistors can produce various second order functions which are available at its three output pins. Two out of three always provide lowpass and bandpass functions while the third output pin can produce highpass or notch or allpass. The center frequency of these functions can be tuned from 0.1Hz to 35kHz and is dependent on an external clock or an external clock and a resistor ratio.

The LTC1061 can be used with single or dual supplies ranging from ±2.37V to ±8V (or 4.74V to 16V). When the filter operates with supplies of ±5V and above, it can handle input frequencies up to 100kHz.

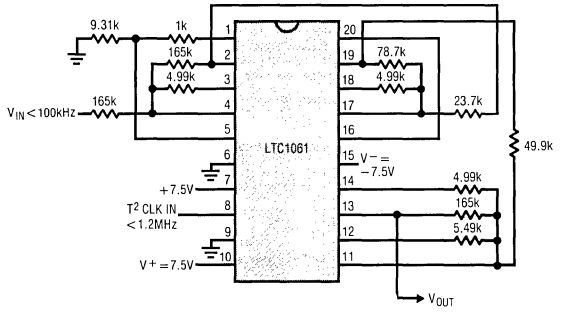
The LTC1061 is compatible with the LTC1059 single universal filter and the LTC1060 dual. Higher than 6th order functions can be obtained by cascading the LTC1061 with the LTC1059 or LTC1060. Any classical filter realization (such as Butterworth, Cauer, Bessel and Chebyshev) can be obtained by the appropriate choice of the external resistors.

The LTC1059 is manufactured by using Linear Technology's enhanced LTCMOS™ silicon gate process.

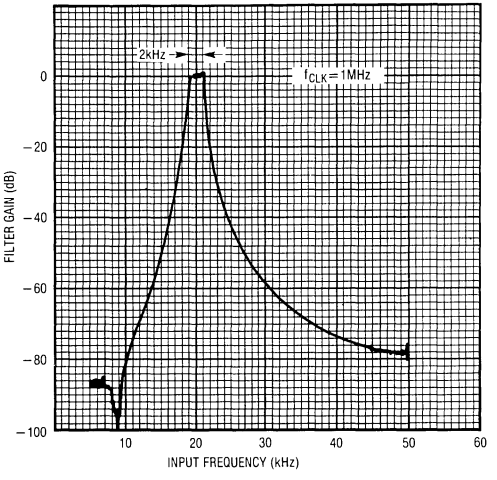
LTCMOS™ is a trademark of Linear Technology Corp.

TYPICAL APPLICATION

6th Order, Clock Tunable, 0.5dB Ripple Chebyshev BP Filter



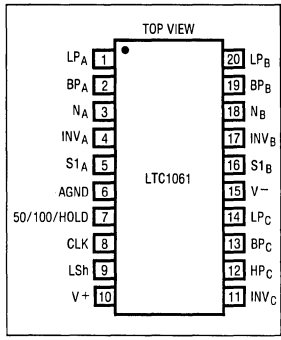
Amplitude Response



ABSOLUTE MAXIMUM RATINGS

Supply Voltage 18V
Power Dissipation 500mW
Operating Temperature Range
LTC1061AC, LTC1061C ..... $-40°C \le T_A \le 85°C$
LTC1061AM, LTC1061M ..... $-55°C \le T_A \le 125°C$
Storage Temperature Range ..... $-65°C$ to $150°C$
Lead Temperature (Soldering, 10sec) ..... 300°C

PACKAGE/ORDER INFORMATION



ORDER PART NUMBER

LTC1061AMJ, LTC1061MJ
LTC1061ACJ, LTC1061CJ
LTC1061ACN, LTC1061CN

ELECTRICAL CHARACTERISTICS

(Complete Filter) $V_S = \pm 5V$, $T_A = 25°C$, T^2L clock input level, unless otherwise specified

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Center Frequency Range, f_o	$f_o \times Q \le 250kHz$, Mode 1			0.1-30k		Hz
	$f_o \times Q \le 1.6MHz$, Mode 1			0.1-18k		Hz
	$f_o \times Q \le 250kHz$, Mode 3, $V_S = \pm 7.5V$			0.1-20k		Hz
	$f_o \times Q \le 1MHz$, Mode 3, $V_S = \pm 7.5V$ (Note 1)			0.1-16k		Hz
Input Frequency Range				0-100k		Hz
Clock to Center Frequency Ratio, f_{CLK}/f_o						
LTC1061A	Sides A, B: Mode 1, R1 = R3 = 50kΩ	●			50 ± 0.4%	
LTC1061	R2 = 5kΩ, Q = 10, f_{CLK} = 250kHz Pin 7 High. Side C: Mode 3, R1 = R3 = 50k R2 = R4 = 5k, f_{CLK} = 250kHz	●			50 ± 1%	
LTC1061A	Same as Above, Pin 7 at	●			100 ± 0.4%	
LTC1061	Mid-Supplies, f_{CLK} = 500kHz	●			100 ± 1%	
Q Accuracy						
LTC1061A	Sides A, B, Mode 1	●		±2	3	%
LTC1061	Side C, Mode 3 $f_o \times Q \le 50kHz$, $f_o \le 5kHz$	●		±3	5	%
f_o Temperature Coefficient	Mode 1, 50:1, $f_{CLK} < 300kHz$			−1		ppm/°C
Q Temperature Coefficient	Mode 1, 100:1, $f_{CLK} < 500kHz$			−5		ppm/°C
	Mode 1, $f_{CLK} < 500kHz$			+5		ppm/°C
DC Offset Voltage						
V_{OS1}, Figure 1		●		2	15	mV
V_{OS2}	f_{CLK} = 250kHz, 50:1	●		3	20	mV
V_{OS2}	f_{CLK} = 500kHz, 100:1	●		6	40	mV
V_{OS3}	f_{CLK} = 250kHz, 50:1	●		3	20	mV
V_{OS3}	f_{CLK} = 500kHz, 100:1	●		6	40	mV
Clock Feedthrough	$f_{CLK} < 1MHz$			10		mV
Max. Clock Frequency	Mode 1, Q < 5, $V_S \ge \pm 5V$			2		MHz
Power Supply Current			6	8	10	mA
		●			13	mA

ELECTRICAL CHARACTERISTICS (Complete Filter) $V_S = \pm 2.37V$, $T_A = 25°C$ unless otherwise specified

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Center Frequency Range, f_o	$f_o \times Q \leq 120kHz$, Mode 1, 50:1 $f_o \times Q \leq 120kHz$, Mode 3, 50:1			0.1–12k 0.1–10k		Hz Hz
Input Frequency Range				0–20k		Hz
Clock to Center Frequency Ratio LTC1061A LTC1061 LTC1061A LTC1061	50:1, $f_{CLK} = 250kHz$, Q = 10 Sides A, B: Mode 1 Side C: Mode 3 100: 1, $f_{CLK} = 500kHz$, Q = 10 Sides A, B: Mode 1 Side C: Mode 3	 ● ● 		 50 ± 1% 100 ± 1%	 50 ± 0.6% 100 ± 0.6% 	
Q Accuracy LTC1061A LTC1061	Same as Above			±2 ±3		% %
Max. Clock Frequency				700k		Hz
Power Supply Current				4.5	6	mA

ELECTRICAL CHARACTERISTICS (Internal Op Amps) $T_A = 25°C$ unless otherwise specified

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Voltage Range			±2.375		±9	V
Voltage Swings LTC1061A LTC1061 LTC1061, LTC1061A	 $V_S = \pm 5V$, $R_L = 5k$ (Pins 1, 2, 13, 14, 19, 20) $R_L = 3.5k$ (Pins 3, 12, 18)	 ●	 ±4 ±3.8 ±3.6	 ±4.2 ±4.2 	 	 V V V
Output Short Circuit Current Source/Sink	$V_S = \pm 5V$		40/3			mA
DC Open Loop Gain	$V_S = \pm 5V$, $R_L = 5k$			80		dB
GBW Product	$V_S = \pm 5V$			2.5		MHz
Slew Rate	$V_S = \pm 5V$			7		V/μs

The ● denotes the specifications which apply over the full operating temperature range.

Note 1: For a complete description of the various modes of operation and application hints, refer to the LTC1060 data sheet.

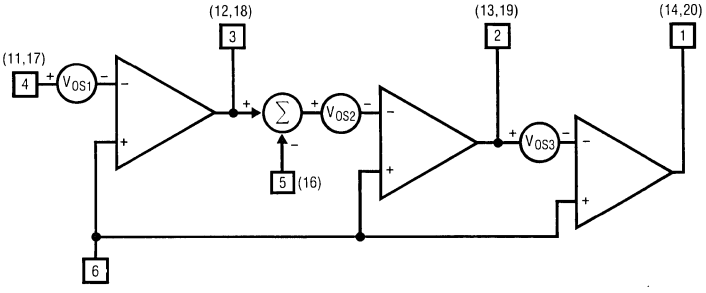
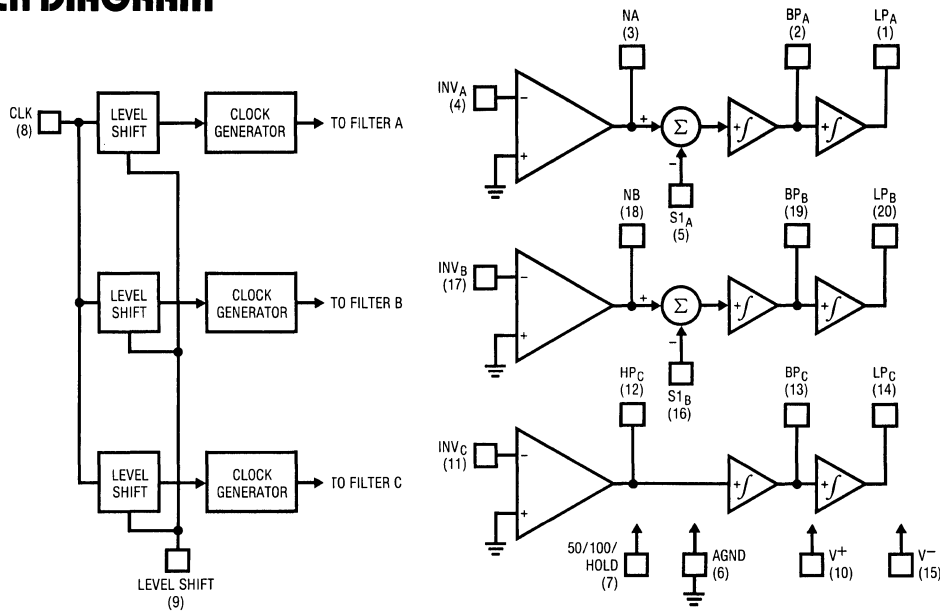


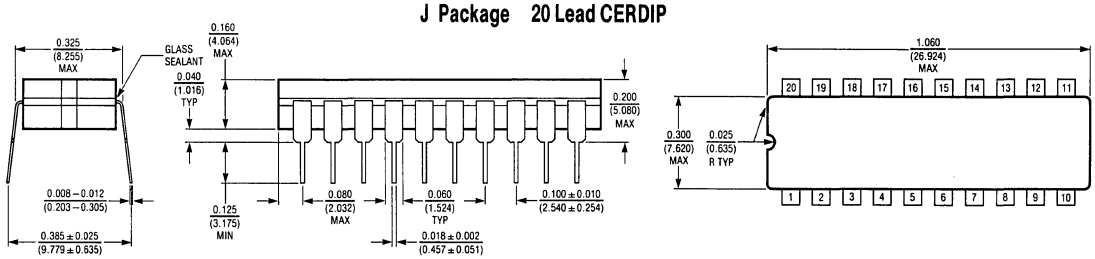
Figure 1. Equivalent Input Offsets of 1/3 LTC1061 Filter Building Block

BLOCK DIAGRAM



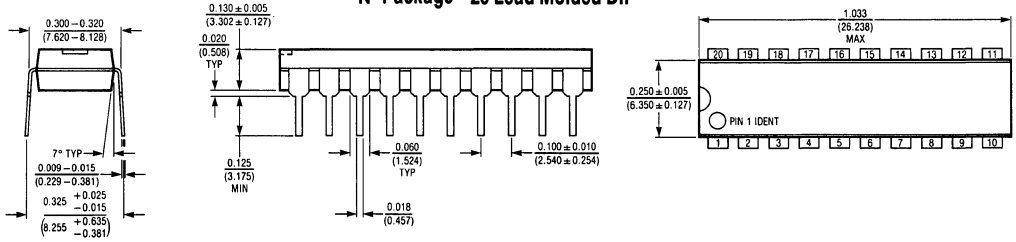
PACKAGE DESCRIPTION Dimensions in inches (millimeters) unless otherwise noted.

J Package 20 Lead CERDIP



θ_{ja}	θ_{jc}	T_{jmax}
100	60	150

N Package 20 Lead Molded DIP



θ_{ja}	θ_{jc}	T_{jmax}
100	60	100

LTC1090

10-Bit A/D with Serial I/O and 8-Channel MUX

FEATURES

- 10-Bit Unipolar, or 9-Bit Plus Sign Bipolar
- 2's Complement Output Coding on Bipolar Conversion
- 8-Channel MUX with Address Logic
- Built in Sample and Hold
- +5V or ±5V Operation
- Reference and Analog Inputs Common-Mode to Both Supply Rails
- Compatible with Industry Standard Full Duplex Serial Interface
- User Selectable MSB or LSB First Data
- 20-Pin 0.3″ Wide DIP Package

DESCRIPTION

The LTC1090 is a serial I/O successive approximation A/D converter with the capability of performing either 10-bit unipolar, or 9-bit plus sign bipolar, conversions on any input selected from the 8-channel input multiplexer. The serial I/O is designed to be compatible with the industry standard full duplex serial interface and provides either MSB or LSB first data with 2's complement output coding automatically provided in the bipolar mode. An on chip sample and hold is also included.

A single input address configures the A/D for channel assignment of the 8-channel MUX, single ended or differential inputs, conversion mode (unipolar vs bipolar) and output data format.

LTC1091

10-Bit A/D with Serial I/O and 2-Channel MUX

FEATURES

- 10-Bit Resolution
- 2-Channel MUX with Address Logic
- Built in Sample and Hold
- 8-Pin Mini-Dip
- Compatible with Industry Standard Half Duplex Serial Interface

DESCRIPTION

The LTC1091 is a 10-bit successive approximation A/D converter with serial I/O, 2-channel input multiplexer and built in sample and hold all in an 8-pin mini-dip. The serial I/O is designed to be compatible with the industry standard half duplex serial interface.

The 2-channel multiplexer is software configurable for single ended or differential inputs, and the input common-mode range includes both supply rails.

A sample and hold is provided to allow easy, accurate conversion of time varying signals.

LTZ1000

Super-Zener

FEATURES

- 1μVp-p Noise
- 2ppm Stability
- Low Hysteresis
- Temperature Stabilized
- 0.3ppm/°C Drift

APPLICATIONS

- 7-1/2 Digit Meters
- Scales
- Calibrators
- References

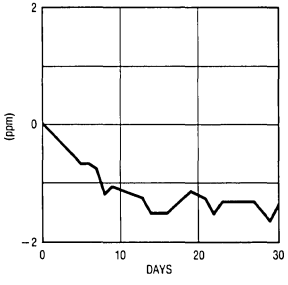
DESCRIPTION

The Super-Zener is a monolithic IC voltage reference designed for exceptionally low temperature drift (0.1ppm/°C), about 1μV peak-to-peak noise, and less than 5ppm long term stability. It offers superior performance to the 199 family at the expense of increased circuit complexity and thermal layout considerations.

Included on the die is the reference with temperature compensating transistor, heater for temperature stabilizing and a temperature sensing transistor. All the control and biasing circuitry is external to allow maximum flexibility and best long term stabilty.

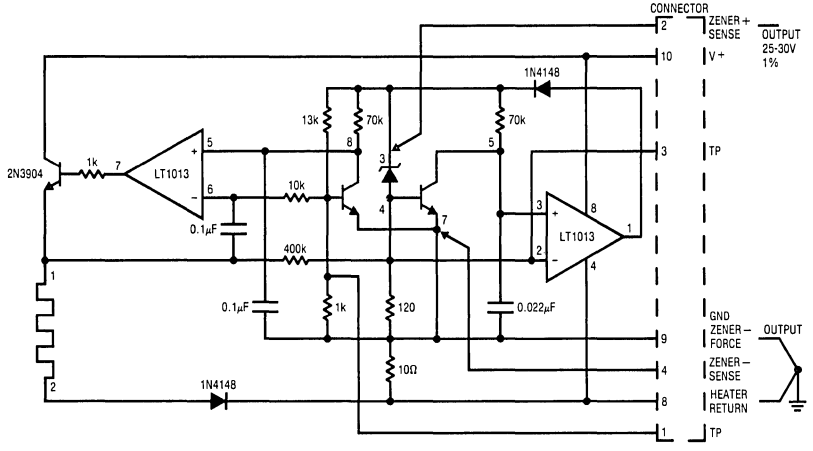
Typical stabilized temperature is about 60°C for best performance although both higher and lower temperatures can be set.

Long Term Stability



LONG TERM STABILITY OF A TYPICAL DEVICE FROM TIME = 0 WITH NO PRECONDITIONING OR AGING

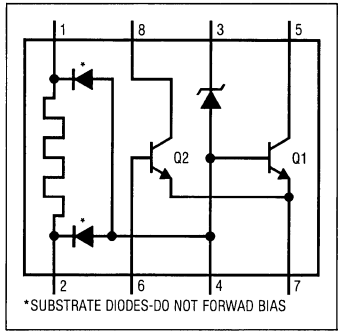
7V Reference Circuit



ABSOLUTE MAXIMUM RATINGS

Heater to Substrate (Pin 4) 40V
Collector-Emitter Breakdown (Q1) 15V
Collector-Emitter Breakdown (Q2) 25V
Emitter-Base Reverse Bias 2V
Operating Temperature Range ..... –55°C to 125°C
Storage Temperature Range ..... –65°C to 150°C
Substrate Diode Forward Bias 0.1V

PACKAGE/ORDER INFORMATION



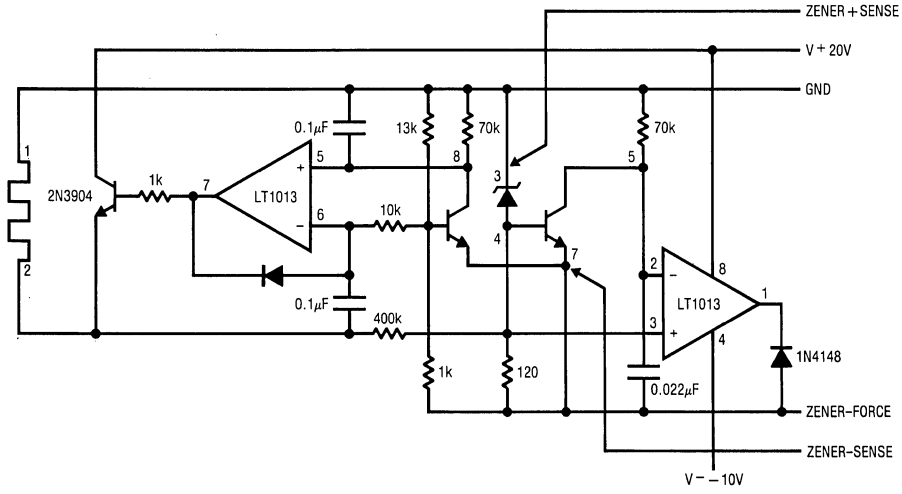
ORDER PART NUMBER
LTZ1000 FACTORY ORDER

TYPICAL ELECTRICAL CHARACTERISTICS

Reference Voltage (I_Z = 5mA) 7.2V
Drift ..... 0.1ppm/°C
Operating Current 5mA
Voltage Noise (0.1Hz to 10Hz) 1μVp-p
Heater Resistance 600Ω
Long Term Stability ..... <2ppm/month
(This Measurement Test Equipment Limited)
Transistor Current Gain 150
Transistor V_{BE} 620mV
Zener Impedance (I_Z = 5mA) 0.20Ω

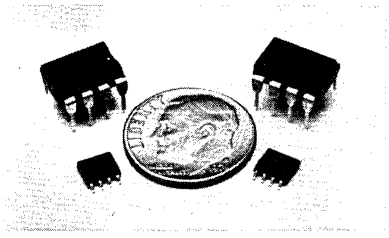
Device must be shielded from air currents. More thermal insulation around the LTZ1000 improves performance.

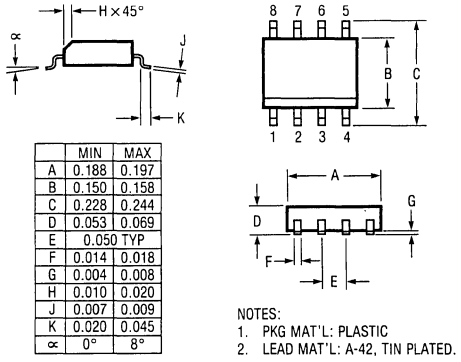
Negative Voltage Reference



Small Outline (SO) Device Packaging

Linear Technology now offers a continually increasing number of high performance CMOS and bipolar linear devices in surface mount packages. At the time of this databook printing, the following device types were available from LTC packaged in the SO-8 (Small Outline Package) per the JEDEC standard outline. For pin out configuration and electrical specification limits consult either your LTC sales representative or the factory.





	MIN	MAX
A	0.188	0.197
B	0.150	0.158
C	0.228	0.244
D	0.053	0.069
E	0.050 TYP	
F	0.014	0.018
G	0.004	0.008
H	0.010	0.020
J	0.007	0.009
K	0.020	0.045
α	0°	8°

NOTES:
1. PKG MAT'L: PLASTIC
2. LEAD MAT'L: A-42, TIN PLATED.

Op Amps:
- LT1001 Precision Op Amp
- LT1008 Low Bias Current, Low Noise, Op Amp
- LT1012 Low Bias Current, Low Offset, Low Noise Op Amp
- LT1013 Precision, Low Offset Dual Op Amp
- LT1056 Precision, High Speed JFET Op Amp
- OP-07 Precision Op Amp

Voltage References:
- LT1004 Precision Micropower Reference
- LT1009 Precision 2.5 Volt Reference
- LT1019 Precision Bandgap Voltage Reference
- LT1021 Ultra Low Drift Precision Reference
- LM385 Micropower Voltage Reference

CMOS Products:
- LTC1044 Switched Capacitor Voltage Converter

Note: By the time you read this list, it will most likely be incomplete. Contact LTC for additional products being offered in the Small Outline Package.

Extended Temperature Range Linear ICs (200°C)

Linear Technology now offers a number of its high performance products fully characterized, tested, and with specification limits guaranteed over an extended operating temperature range of from −55°C to +200°C.

The list of extended temperature range products being offered by Linear Technology continues to grow. At the time this catalog was printed, the company offered for sale the following products.

Op Amps:

LT1001XH Precision Op Amp
LT1007XH Low Noise, High Speed Precision Op Amp
LM101AXH Uncompensated General Purpose Op Amp
LM118XH High Slew Rate Op Amp

Precision References:

LM129XH 6.9V Precision Voltage Reference

Comparators:

LM119XH High Speed Dual Comparator

Complete specifications on Linear Technology's 200°C product offerings can be obtained directly from your local LTC sales representative or directly from the factory.

SECTION 11— APPENDICES

SECTION 11—APPENDICES

Quality and Reliability Assurance Programs

Linear Technology Corporation has a wide ranging program integrating vendor participation, design engineering, and manufacturing to produce the most reliable and highest quality linear integrated circuits available on the market. Our modern manufacturing facility in Milpitas, California is DESC line certified and we have successfully completed over 30 major OEM quality system surveys to MIL-Q-9858 and MIL-I-45208. Our Quality and Reliability Assurance Programs are summarized below:

- **Wafer Fabrication**—A modern class 100 area, modular clean room construction with full environmental monitors. Emphasis is placed on statistical quality control, CV plots, SEM monitors and on our proprietary dual layer passivation system.
- **Assembly & End of Line**—Incoming inspection of all materials and piece-parts, line surveillance and process control monitors.
- **Testing**—Incoming inspection and acceptance of all offshore lots prior to release to test. Ultra modern LTX testers, multipass testing with closed loop binning to reduce outgoing electrical defective levels. Many "beyond data sheet" tests and full temperature QA lot buy-offs are performed as standard processing.
- **Traceability**—A backside or side mark is placed on all units, where space permits, to give information on a unit-by-unit basis tracing back to the wafer fab lot, assembly, end of line (e.o.l.) and test lots. We consider traceability to be essential for good engineering control and additional insurance for our customers. The information provided exceeds the seal week control required by MIL-STD-883.
- **ESD (Electro Static Discharge)**—A full program is in place from design through manufacturing. Products are fully characterized to MIL-STD-883C (Method 3015) and strict controls on handling and packaging are observed.
- **Training and Certification**—Operator training has been established for all operations and certification is performed on a 6 monthly basis.
- **Major Change Control**—Major change controls are in place to notify our customers in accordance with MIL-M-38510F, LTC internal specifications, or specific customer specifications as required.
- **Quality Assurance**—Full monitoring and reporting of quality data with emphasis on statistical process control charts. Refer to our Quality Assurance Program.
- **Failure Analysis and Reporting**—A formal program exists to record, analyze and take appropriate corrective action on all returns. A report is generated and sent to the customer stating our findings and action.
- **Reliability Flows**—Linear Technology reliability flows include JAN-38510, DESC Drawings, 883 (to the new Rev. C) R-Flow, and Hi-Rel (Source Controlled Drawings). In addition, specialized processing such as SEM, PIND and other tests can be performed as required.
- **Reliability Monitor**—LTC has a unique reliability structure built into each wafer that is used to obtain rapid feedback on reliability. This data is obtained in less than 1 week, versus 40 weeks for a typical reliability audit. See the LTC Reliability Program for more details.
- **Reliability Audit**—Data is gathered on a monthly basis for selected package/product combinations. This data is summarized each quarter and published in a Data Pak showing Operating Life, 85/85, Autoclave, 883 Group C, and 883 Group D summary data. Copies of Data Pak summaries are available by writing or calling Linear Technology, 1630 McCarthy Blvd., Milpitas, CA 95035, (408) 942-0810.

Introduction

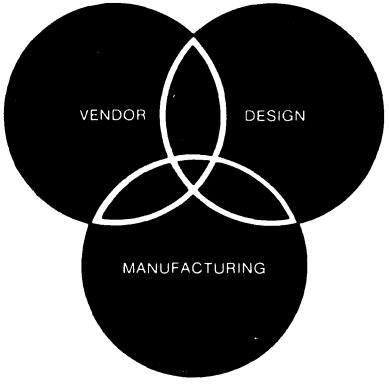
In the early 1960's the study of reliability was mainly the province of mathematicians and statisticians. In the late 1960's and throughout the 1970's it was realized that an understanding of the physical phenomena was necessary to identify the various failure mechanisms and considerable progress was made in this area. Sophisticated diagnostic techniques were devised and this knowledge complemented the earlier theoretical work to form a very sound foundation.

At Linear Technology Corporation we have a firm appreciation for the impact of Reliability on our products and we have made every effort to integrate this knowledge into our device designs and manufacturing processes. We believe that "LINEAR" should be "THE MOST RELIABLE COMPONENTS" and it is our intention to supply "TOMORROW'S RELIABILITY—TODAY"!

All areas that impact reliability have received considerable attention and achieving our goal of "THE NUMBER ONE" Reliability Supplier of Analog Circuits has impacted the DESIGN, FABRICATION, PACKAGING AND TESTING of our products.

"RELIABILITY" requires a total systems approach involving all parties; from the raw material vendor, to the designer, to manufacturing.

Cooperative Interface

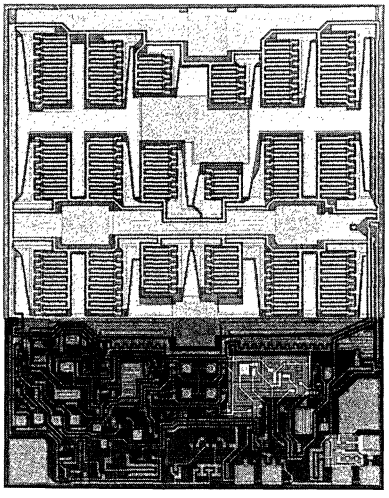


Design

At the DESIGN stage the reliability of the circuit is heavily dependent on layout considerations. The thickness and width of the metallization has been defined to minimize the current density and avoid electromigration problems at elevated temperatures. The routing of the metal pattern is designed to eliminate potential inversion, or leakage failures and guard ring structures are used where appropriate. The positions of the bonding pads are carefully selected to optimize device performance and also to fit easily into a variety of packages without creating potential bond loop problems that could result in shorted wires. In all of our voltage regulators, thermal limiting is included in the circuitry to shut down the device if the temperature exceeds a threshold value. Additional insurance is provided by employing short circuit current protection to safeguard catastrophic failure. The philosophy of incorporating fault tolerant designs with innovative circuit concepts is a fundamental design rule at Linear Technology

5 Amp Positive Adjustable Regulator

SAFE AREA
Large Ballasted Power Transistor ensures equal current sharing.



THERMAL LIMIT CIRCUIT

ISOLATING RESISTOR
Prevents destruction from high transient current in 'Adjust' Pin.

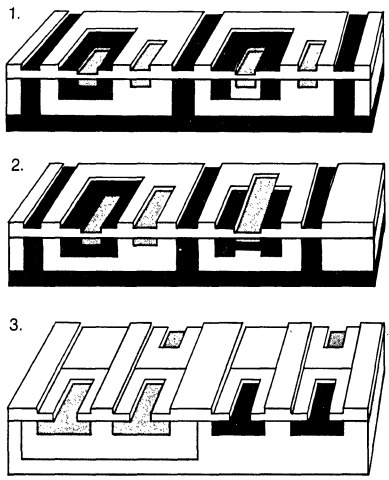
Corporation. The design rules used by Linear Technology are conservative to avoid compromising reliability, and safe operation regions are chosen to prolong device life in the field. Input protection is provided and the ability of our devices to withstand transient voltage spikes is better than average. We focus on reducing lead count of our device designs since there is generally a strong correlation between the number of leads in a package and the mean time between failures for a device. The thermal layout of our circuits is also a major consideration to minimize parameter drift and optimize performance. The designs at Linear Technology Corporation cover a diverse technological base ranging from Bipolar to CMOS. In the case of CMOS, design techniques are used to minimize SCR and latch-up phenomena. Many integrated circuit designs are susceptible to electrostatic discharge effects (ESD) and electrical overstress (EOS) with generally catastrophic results. In the designs at Linear Technology Corporation, care is taken to ensure that a high degree of protection is built into our products to minimize this effect.

Prior to release, new devices are thorougly characterized and subjected to rigorous mechanical and electrical stress testing to exercise all facets of the design, process, and package combination. Linear Technology Corporation has an active in-house ESD (Electrostatic Discharge) program to prevent yield loss and the potential weakening on devices.

Wafer Fabrication

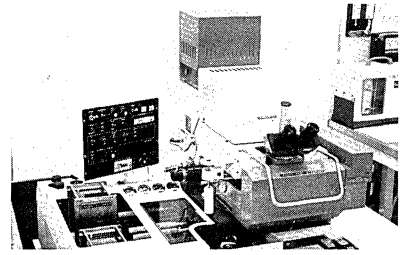
In the WAFER FABRICATION area the key to a reliable process is consistency and repeatability. Linear Technology has a brand new ultramodern wafer fabrication facility and wafer handling has been kept to a minimum. Cassette to cassette transfer is used extensively and proximity mode aligners are utilized in masking to significantly reduce photomasking defects. Microprocessor controlled furnaces are used to eliminate the impact of operator error.

Diverse Range of Processes

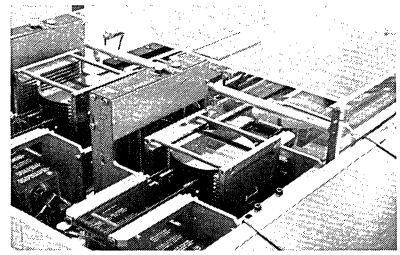


1. Super Beta Structure
2. Bi-fet Structure
3. Silicon Gate CMOS Structure

Cassette to Cassette Transfer



Canon Proximity Aligner

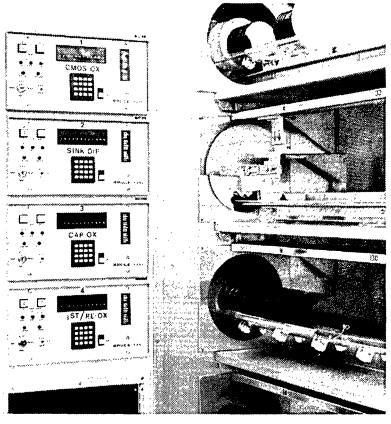


Stringent incoming inspection checks are made on the raw silicon wafers and masks used in the process. Environmental monitoring of the gases, clean air, particle count, deionized water, and furnace temperature and flows are done on a routine basis to avoid any sudden changes that could impact device reliability.

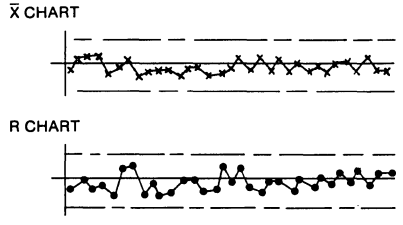
Quality Control checks at various points in the process ensure consistency and control charting is used extensively throughout the fabrication area. The quality of the oxide is checked regularly using C-V plots to check for contamination and surface state anomolies and processes are not operational until minimum requirements are met. Each wafer contains diagnostic structures in addition to the device structures and these test vehicles are used to investigate and detect potential yield and reliability hazards in advance. Scanning electron microscope pictures are taken periodically to check the integrity of the metallization system. Emphasis is given to the early detection of step coverage or misalignment problems. A proprietary passivation system has been developed that will enable our die to operate in a variety of plastic packages and the nature of this unique multilayer system will make the die virtually impervious to the packaging medium.

The strategy of Linear Technology in developing its process is to make the chip as impervious as possible to moisture and ionic contaminants. This approach assures reliable operation even in marginal environments. The Linear Technology process offers several layers of protection. 1) Extensive CV monitoring of all diffusion tubes and deposition systems assure underlying oxides with low levels of positive ionic contamination. Phosphorous gettering ties up these ions in an inactive state. 2) A proprietary deposited oxide gives conformal coverage of metal and oxide steps, and is free of cracks. 3) A plasma nitride overcoat protects the die from external ionic contamination during handling, testing and assembly. The dual nitride/oxide layer is completely free of cracks and pinholes which enhance corrosion protection against moisture contamination.

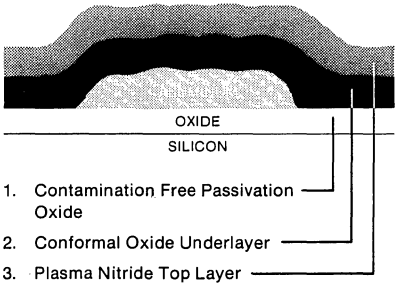
Microprocessor Controlled Furnaces

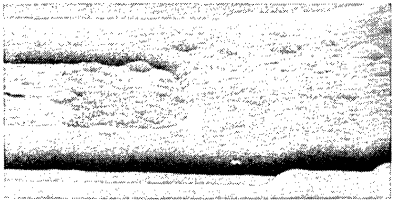


Control Chart



Passivation Process



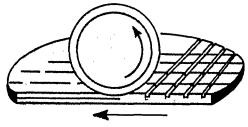


Packaging

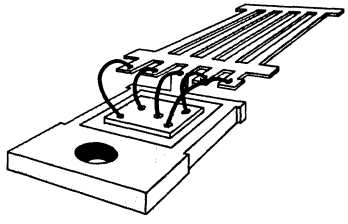
The impact of new equipment, techniques and materials have had a tremendous impact on device reliability. In the area of wafer scribing, sawing of the wafers has decreased device chipping and cracking significantly. The handling of dice at second optical inspection and die attach is now mainly semi-automatic, removing the need to use tweezers and the resultant damage due to this operation. Semi-automatic lead bonding machines have produced tremendous gains in productivity but as importantly more consistent lead bonds have resulted from this new innovation. Die attach materials have improved and modern low temperature glass ceramic seals have dramatically increased product reliability. At Linear Technology we are using the latest state-of-the-art assembly equipment and materials. Our epoxy material has the lowest sodium and chlorine content of any molding compound available and the data on operating life, power cycling and pressure pot is outstanding. All materials are inspected to better than industry standards prior to use and strict QC checks are performed on-line to assure control and conformance to specifications. At LTC traceability to a fabrication lot is considered to be of primary importance. On all packages where space allows a side mark or a backside mark is used to give this key information. We are able to track the country of origin, assembly location, die type, wafer fab lot, exact seal dated and also identify non standard processing if required on a special flow. This unique benefit is offered as a standard feature at no additional cost and adds immensely to the level of control and traceability on Linear Technology products.

Mil-Standard 883 Method 2010 Condition B visual criteria are applied to all Linear Technology products and a thorough inspection of all lots received from our assembly operations in Southeast Asia is performed prior to testing. A system of effective and rapid communications exist between our operation in Milpitas, California and Southeast Asia to analyze and correct any assembly or process related problems before the product is shipped to the customer. Precautions are taken throughout the assembly process to minimize the impact of ESD (Electrostatic Discharge) on our devices.

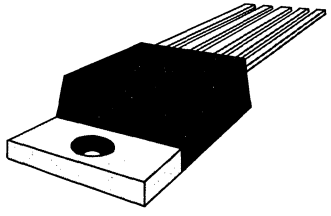
Wafer Saw



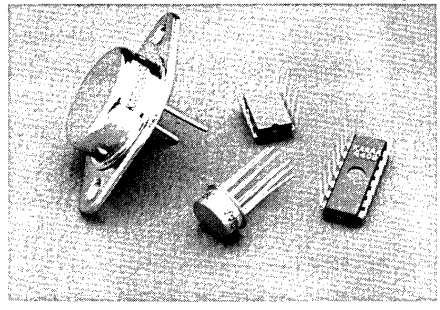
Die Attached and Wire Bonded Unit



Encapsulated and Finished Unit



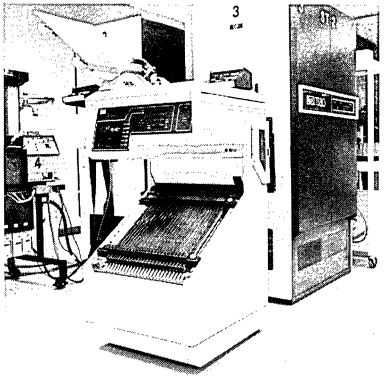
Side/Backside Mark on Unit



Test

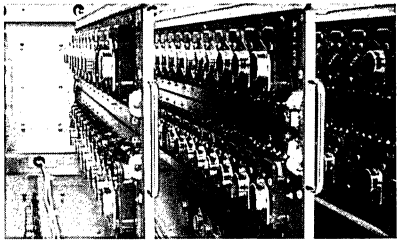
The testing of analog circuits is a science in its own right and requires very special technical skills to overcome the challenges that are presented. At Linear Technology we have invested in the very latest "state-of-the-art" computer controlled testers and our device designs exercise the limits of these excellent testers. All Military 883 products receive a 150°C burn-in prior to test and full temperature testing is performed. Regulator products are put on "rack burn-in" and the devices are exercised in the thermal shutdown mode prior to testing. This pretest burn-in contributes to the removal of infant mortality failures and enhances product reliability. Other tests check the thermal regulation and verify the integrity of the die attach as the presence of voids under the die for a regulator affects device performance adversely. Often, tests additional to the data sheet tests are added to a test flow to detect potential flaws that could impact reliability.

LTX/LINEAR Tester with Environmental Handler

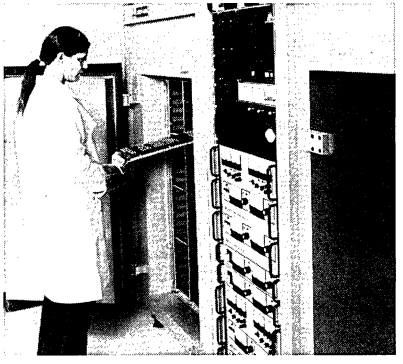


At Linear Technology we believe that the thorough and complete testing of our components is an essential element in our plan to provide 'premier' reliable products. Precautions are taken throughout test to safeguard our devices from the insidious effects of ESD (Electrostatic Discharge). As an example, all chip capacitors are prestressed with voltages (in excess of the device maximum voltage ratings) to induce failure in substandard lots.

Rack 'Burn-in' of TO-3 Regulators



Burn-in Operation

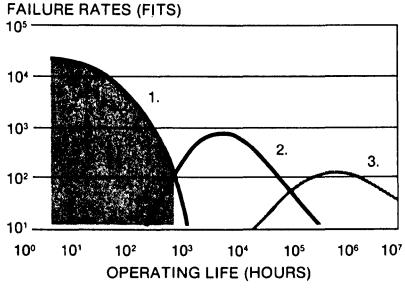


Reliability Flow

Reliability failure rate can be broken out into three main categories: 1) Infant Mortality, 2) Freak Failures and 3) Long Term Failures. Short term burn-in screening as described in the previous section address the first category—infant mortality. The long term failures represent a significant number of hours in terms of the mean time between failures and so the major area of concern is a sufficient pre-screen conditioning to eliminate the bulk of the infant mortality and freak failures.

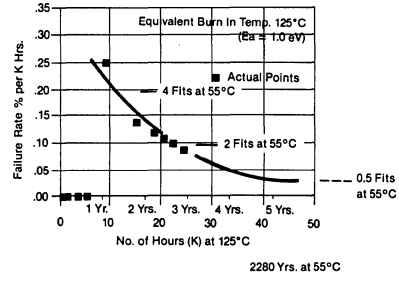
These early life failures impact customer warranty costs and reputation severely and the replacement costs are clearly several orders of magnitude greater than the initial component costs. The Linear Technology 883 program addresses this requirement and offers a cost effective in-house flow. The flow is defined in our MIL-STD 883 brochure and the essential elements of the program include visual inspection at second and third optical inspection to Condition B (Mil-Standard 883, Method 2010, stabilization bake at 150°C, temperature cycling from −65°C to 150°C, constant acceleration, fine and gross leak, followed by a 125°C burn-in for 160 hours or equivalent. Assuming an active energy of 1.0ev, this burn-in is equivalent to 80,000 hours or approximately 9 years at a normal operating temperature of around 55°C.

Typical Representation of IC Lot Failure Rates at 50°C Operation

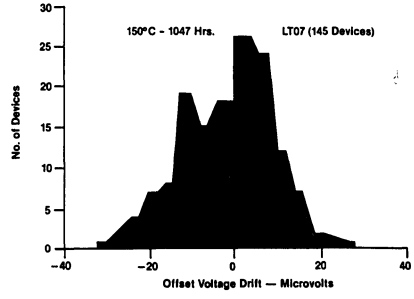


1. Infant mortality population which could be 0.5% of the lot. Its mean life could be as low as 50 hrs.
2. The freak population could represent up to 5% of the lot. Its mean life could be 5 yrs.
3. Main population whose mean life could be hundreds of years.
4. The dramatic impact on total lot reliability that is achieved by weeding out early failures via 100% burn-in.

Failure Rate vs Time—LT07H



Operating Life Drift Data



Wafer Fab Reliability Audit

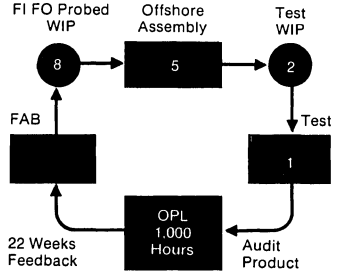
As an additional reliability control, Linear Technology has innovated a periodic reliability audit of the wafer fab process, using a specifically designed reliability structure which is stepped into all wafers.

This structure is optimized to accelerate, under temperature and bias, the two most common failure mechanisms in linear circuits, namely mobile positive ions and surface charged-induced inversions. The three-terminal structure is scribed from a run and assembled in a hermetic package. These devices are burned-in for a predetermined temperature and time. The same structure becomes sensitive to either failure mechanism depending upon the bias scheme used during burn-in. A limit is defined for the leakage current change during burn-in; a failure indicates a wafer fab problem which will be addressed by the process engineering group. The use of a test pattern allows any device to be monitored and also gives faster unambiguous feedback than is normally achieved by performing reliability testing on assembled product. Reliability data is generated in less than one week giving immediate feedback on device reliability. The standard industry monitoring schemes typically take a minimum of 22 weeks to obtain this feedback and it is not uncommon for the cycle time to be up to 40 weeks before fab is alerted of a problem.

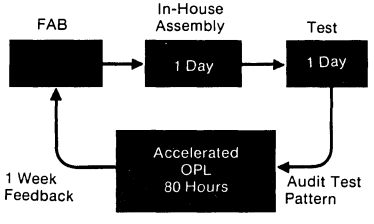
Linear Technology utilizes this new control technique in addition to the conventional reliability audit on randomly pulled finished product.

Process Reliability Monitor

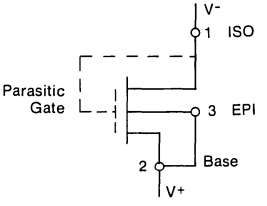
STANDARD INDUSTRY RELIABILITY AUDIT



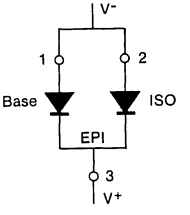
ACCELERATED FAB RELIABILITY AUDIT



FIELD CHANNEL MONITOR

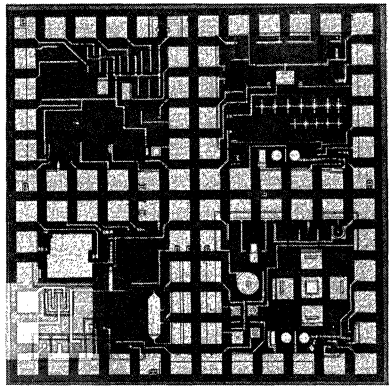


SODIUM MONITOR

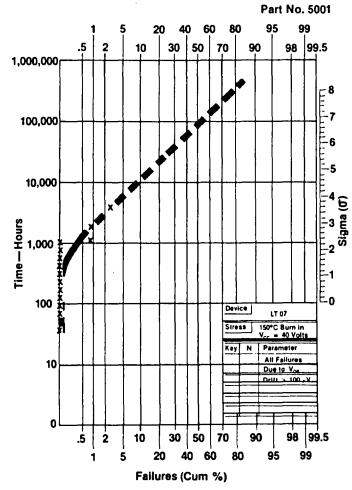


Conclusion

At Linear Technology Corporation we are addressing reliability and quality with the same priority to produce the best possible product in the analog world. We believe that the combination of our extensive design skills, and exciting innovations in the wafer fabrication process, coupled with the most modern assembly techniques, has produced the "MOST RELIABLE" linear products available in the market today. Our standard product flows include thermal limit rack burn-in (for all regulators) and 150°C burn-in for Military 883 products to significantly reduce the infant mortality failures. In addition, our 883 flow is designed to further enhance product reliability. We fully realize that the cost of failure in the field is many orders of magnitude more than the initial component cost. By purchasing Linear Technology Corporation's products, worthwhile insurance can be gained.



LT07H—Mean Time Between Failures



At Linear Technology Corporation our overriding commitment is to achieve Excellence in Quality, Reliability and Service (QRS). We interpret the word "excellence" to mean delivering products that consistently exceed all the requirements and expectations of our customers. The commitment to QRS extends from the President to every employee, from design to product qualification, and from manufacturing to shipping. To meet this commitment, Linear Technology has established a comprehensive program called "Quality for the Eighties."

This program is divided into four separate, but highly interrelated programs, namely Quality Environment, Total Quality Control, Vendor Participation, and Focus for the Eighties.

Quality Environment

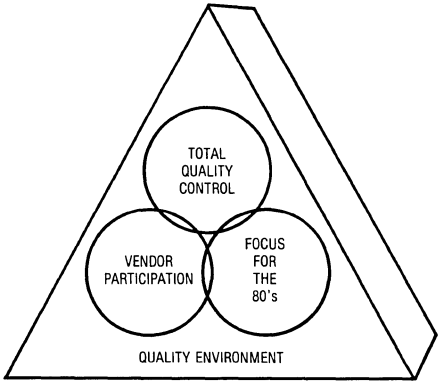
This first program, Quality Environment, serves as the building block for three other programs. It entails establishing an environment that is conducive to the participation of each and every employee in helping to build quality into our products. This program encourages every employee to identify any quality problem and participate in recommending solutions.

An operator training and certification program has been established that covers every area of manufacturing from incoming raw material inspection, wafer fabrication, assembly, and test to shipping. Emphasis is placed on compliance with specifications, performance to quality goals, electrostatic discharge damage (ESD) awareness and controls, encouraging operators to think quality and recommend quality improvement ideas.

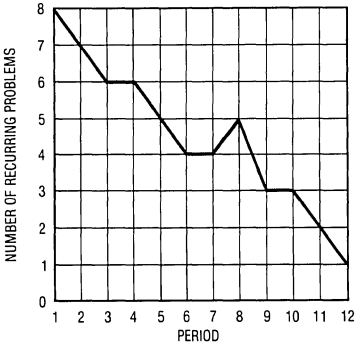
To ensure compliance with specifications, a Quality Audit Team performs a systems audit of key manufacturing areas at periodic intervals. Compliance with process specifications and the detailed programs of the Corporate Quality Assurance Policy are verified, and discrepancies reported for quick resolution with special emphasis to eliminate recurring problems. The performance of each area is then rated, providing a strong incentive for each area to excel.

With the philosophy that each department, starting from incoming raw materials, is considered a customer of the preceding department, every effort is made by working closely together to meet or exceed our end-customer requirements and goals.

Quality for the '80's



Systems Quality Audit-Tracking Recurring Problems



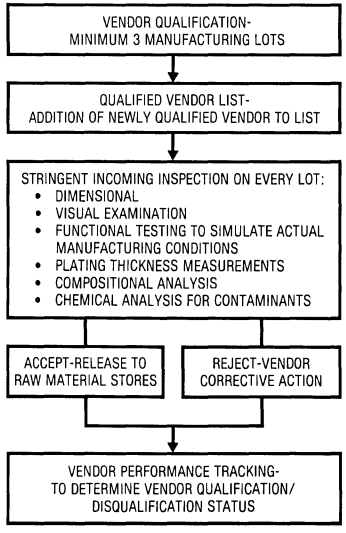
Total Quality Control

The second program starts with the incorporation of innovative, but conservative, design and layout rules to achieve the best performance without sacrificing quality and reliability. During the design and development cycle, Design, Product, Package, Manufacturing, Quality and Reliabilty Engineering groups participate in design reviews to ensure that all program aspects are covered; ranging from product performance objectives to ensuring reproducibility and repeatability in wafer fabrication and assembly. Special emphasis is placed on devising input protection circuitry to minimize susceptibility to voltage spikes and ESD, optimizing thermal layout to minimize parametric drift, and optimizing bond pad layout to maximize assembly and electrical test yields, at the same time allowing the die to be assembled in a wide selection of packages.

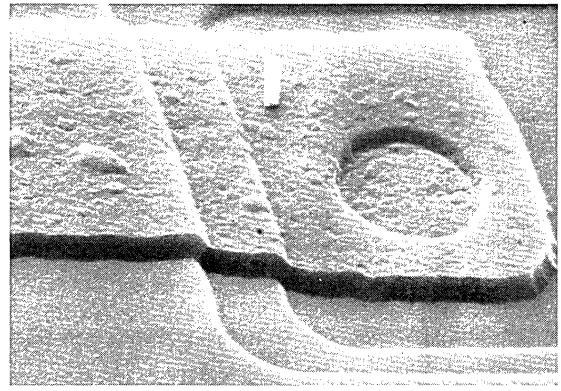
Once the design is approved, a stringent manufacturing qualification test plan is conducted on the initial engineering runs. The test plan is selected to bring out any weaknesses in the design and any manufacturability problems, and includes reliability stress tests such as high temperature operational life and high temperature humidity bias 85°C/85% RH for plastic packages, and MIL-STD-883C method 5005 qualification testing for hermetic packages. Product performance on these tests must be equal to or better than similar products within the same generic group to be considered qualified. Major design, package, material and process changes are also subjected to these same stringent qualification requirements. In addition to achieving the required reliability performance, an engineering change must also achieve manufacturing yield and quality performance levels equal to or better than the original product to be considered qualified.

In manufacturing, process controls start with vendor qualification on raw material piece parts. A Qualified Vendor List is maintained and performance of each vendor is continuously monitored on a Vendor Rating Program. A dimensional, visual, functional and, where applicable, compositional analysis is performed on each direct raw material lot. Automated state-of-the-art wafer fabrication, assembly and test equipment, cassette-to-cassette handling in wafer fabrication and automated handling in assembly are utilized, where possible, to maintain manufacturing consistency and quality. Only fully trained and certified operators are allowed to work on production material.

Raw Material Controls



SEM Monitor of Metallization Quality



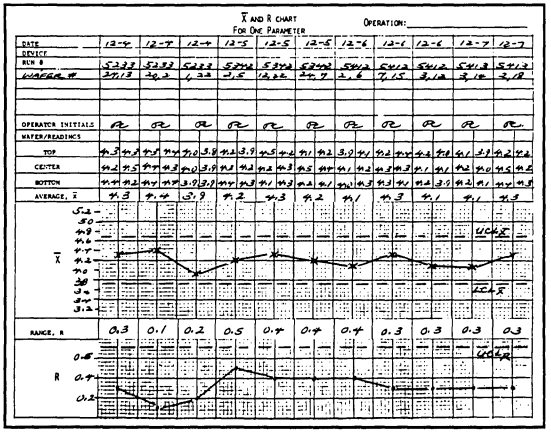
Stringent process controls, typically beyond industry standards, are established for each critical manufacturing step in wafer fabrication, wafer test, assembly, package finishing, mark and pack and shipping as depicted in the Quality Control Flow Diagram. The process controls include monitors of critical assembly processes at a minimum frequency of four times per shift, and lot acceptance inspection for operations requiring 100% production inspection. Initial die inspection and preseal visual inspection are performed per MIL-STD-883 Method 2010 Test Condition B. Statistical quality control techniques are employed in optimizing process parameters, and monitoring process performance through the use of control charts with action limits and upper and lower control limits, and in parametric distribution analysis at electrical test.

Electrical quality is guaranteed by conservative guardbanding on production test programs of a minimum of three machine guardbands, by using state-of-the-art test equipment and 0.04% AQL for lot acceptance testing at 25°C for all military and commercial lots. All lots also receive a QA AQL lot acceptance test at the high and low temperature extremes of the specification. Additional tests, like rack burn-in, beyond the data sheet specifications on regulator products are performed by exercising the parts in a thermal shutdown mode. These tests are incorporated into the test flow to improve reliability and weed out infant mortality failures. Visual and mechanical quality is optimized by minimizing handling of parts in assembly, test and end of line operations. Lead finish processes have been selected that mimimize solderability problems and all lots are subjected to a stringent major visual/mechanical inspection. Administrative errors due to mixed and wrong parts are minimized by strictly adhering to a one lot per station policy, and double checking orders at order entry and shipping. Before shipment of a lot to the customer each lot is inspected to ensure that it meets internal and customer specifications and purchase order requirements. The level of attention paid to each unit is demonstrated by the fact that each unit is traceable to the wafer fabrication lot number via a side or back mark on both 883 and commercial products on all packages, except where there is a physical constraint.

Through the use of automated equipment, strict process controls (utilizing proven statistical quality control techniques), periodic systems and quality audits (conducted by the Quality Audit Team), stringent facilities and environmental controls and monitors, Linear Technology is able to ensure quality is built into the product and to guarantee a consistently high quality level.

The manufacturing quality controls are complimented by a reliability audit program designed to weed out design, fabrication, packaging and assembly deficiencies. Additionally, controls are supported by a comprehensive failure analysis and corrective action program designed to provide timely feedback of findings to all operating groups for resolution. The analysis of customer returns, and corrective action taken, completes the closed loop of our Total Quality Control program.

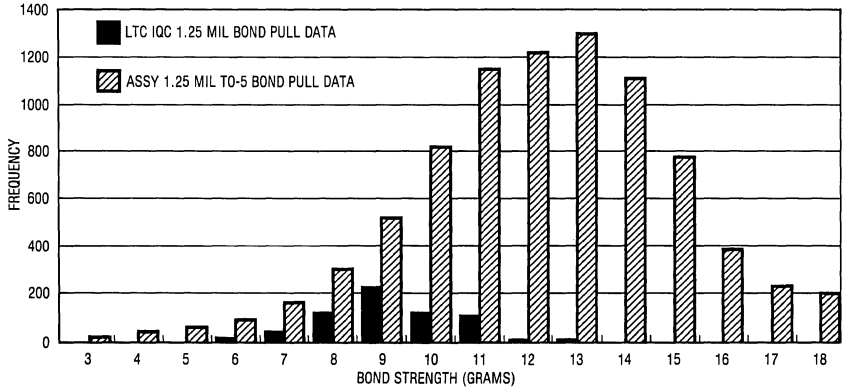
$\bar{X}$ and R Control Chart for One Variable



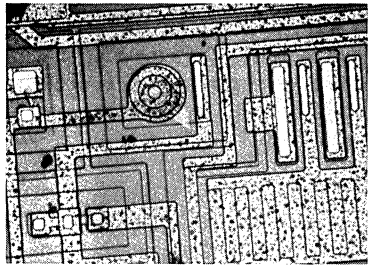
Military and Commercial Products Share the Same Stringent Inspections and Controls

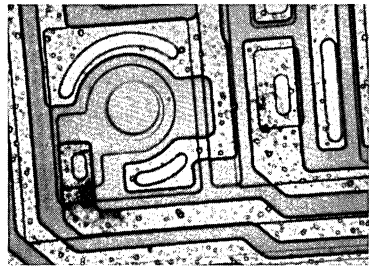
- WAFER FABRICATION PROCESS CONTROLS & CLASS 100 PROCESSING.
- REGULAR SEM MONITORS.
- DICE INSPECTION PER MIL-STD-883C METHOD. 2010 TEST CONDITION B.
- PRE-SEAL VISUAL INSPECTION PER MIL-STD-883C METHOD 2010. TEST CONDITION B.
- DIE SHEAR TEST PER MIL-STD-883C METHOD 2019.
- BOND PULL TEST PER MIL-STD-883C METHOD 2011.
- SOLDERABILITY TEST PER MIL-STD-883C METHOD 2003.
- MARK PERMANENCY TEST PER MIL-STD-883C METHOD 2015.
- HERMETICITY TESTING PER MIL-STD-883C METHOD 1014.
- QA ELECTRICAL TEST TO 0.04% AQL AT 25°C, AND TEMPERATURE TESTING.
- EXTERNAL VISUAL PER MIL-STD-883C METHOD 2009.

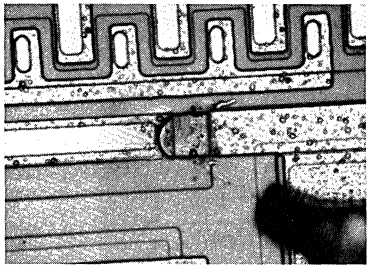
Bond Strength Histogram

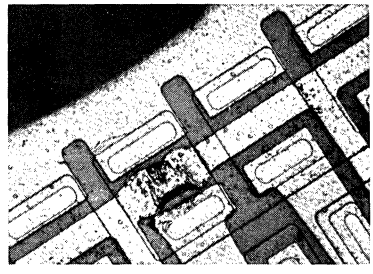


Failure Analysis Photomicrographs









Vendor Participation

The requirements of high quality raw materials for integrated circuit manufacture range from ppb (parts per billion) impurity levels for electronic grade chemicals to ppm (parts per million) defective levels for lead frame packaging materials. It is not only essential, but critical for the semiconductor manufacturer to work closely with their vendors to attain the high quality levels needed in raw materials. At Linear Technology, a program has been established and implemented to allow vendor participation in formulating specifications and establishing percentage defective and lot rejection rate goals. This vendor participation ensures that the direct and raw material quality levels received are consistent with our manufacturing and end-product quality goals. Clearly, achieving optimum quality product requires the use of the best possible materials available and with continuous communication and feedback from our vendors to improve in this key area.

Focus For the 80's

The following key quality improvements programs have been established to meet the quality requirements of the 80's.

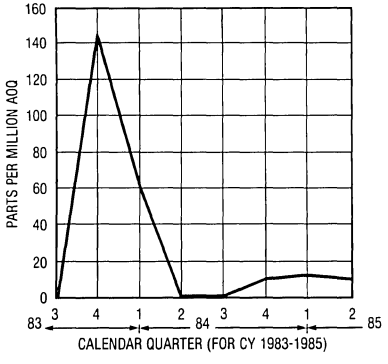
PPM Goals

As demand for quality semiconductor components becomes increasingly more stringent, the percentage goals from the 1970's have given way to ppm goals in the 1980's. At Linear Technology, ppm quality goals are established for every major operation, from incoming inspection to customer returns. Performance to goals is reviewed quarterly and, where goals are not met, quality improvement programs are defined and implemented. Quality goals are updated and tightened on an annual basis, and quality programs are redefined to achieve the new goals established. One of the early benefits of this program is demonstrated by the excellent average outgoing electrical quality (AOQ).

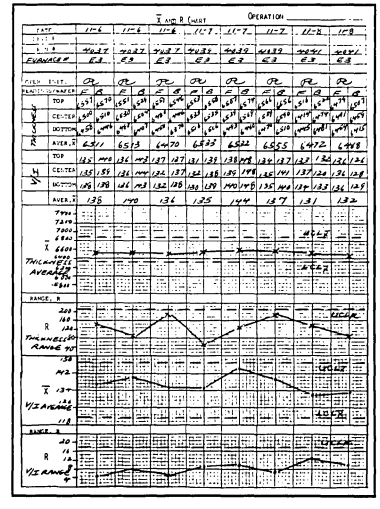
Statistical QC

The increased reliance on automated manufacturing and test equipment underlines the need for strict process control techniques. Statistical QC is a valuable tool and, at Linear Technology, we realize the importance of these methods. Engineering analysis is performed regularly, using SQC techniques to establish the process capability. Control charts showing $\overline{X}$ and R points are tracked to ensure the process is within normal limits and action and shutdown limits are established for critical operations.

25°C Electrical Average Outgoing Quality (AOQ)



$\overline{X}$ and R Control Chart for Two Variables



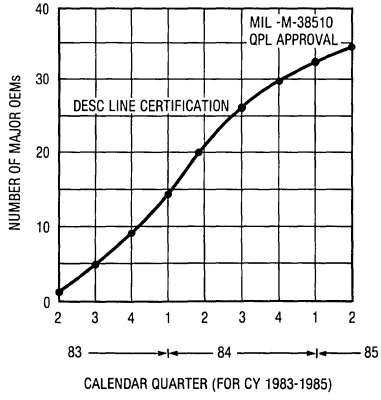
ESD Control

A comprehensive ESD control program has been established which encompasses design, handling, testing, storage, and final packaging for shipment. The program includes the use of grounded table tops, floor mats, wrist straps and heel straps, topical antistatic treatment of floor coverings, banning of static bearing materials from the manufacturing environment, ionizers, and use of conductive or antistatic materials for handling and final packaging. Areas where ESD control must be enforced are designated as ESD Protected areas. ESD awareness training programs help to increase the operator's awareness for successful implementation of this program. Every effort is made to stamp out this silent chip killer. The benefits of this program are improved quality and reliability to the customer.

Customer Ship-To-Stock Program

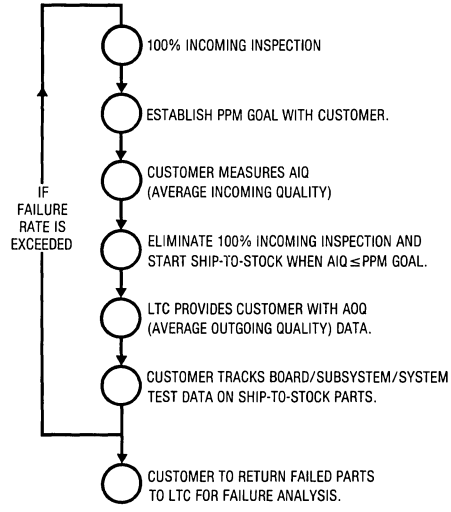
Linear Technology is working hand-in-hand with customers to supply consistently high quality-level products to help achieve a ship-to-stock program by eliminating the need to do an incoming inspection. We recognize the benefits to our customers of a ship-to-stock program, namely savings in the need to purchase and maintain incoming test equipment, savings in the need to maintain a safety stock in case of incoming lot rejections, and reduction in board failures and re-work costs because of higher component quality.

Quality System Surveys MIL-Q-9858 and MIL-I-45208 Approval

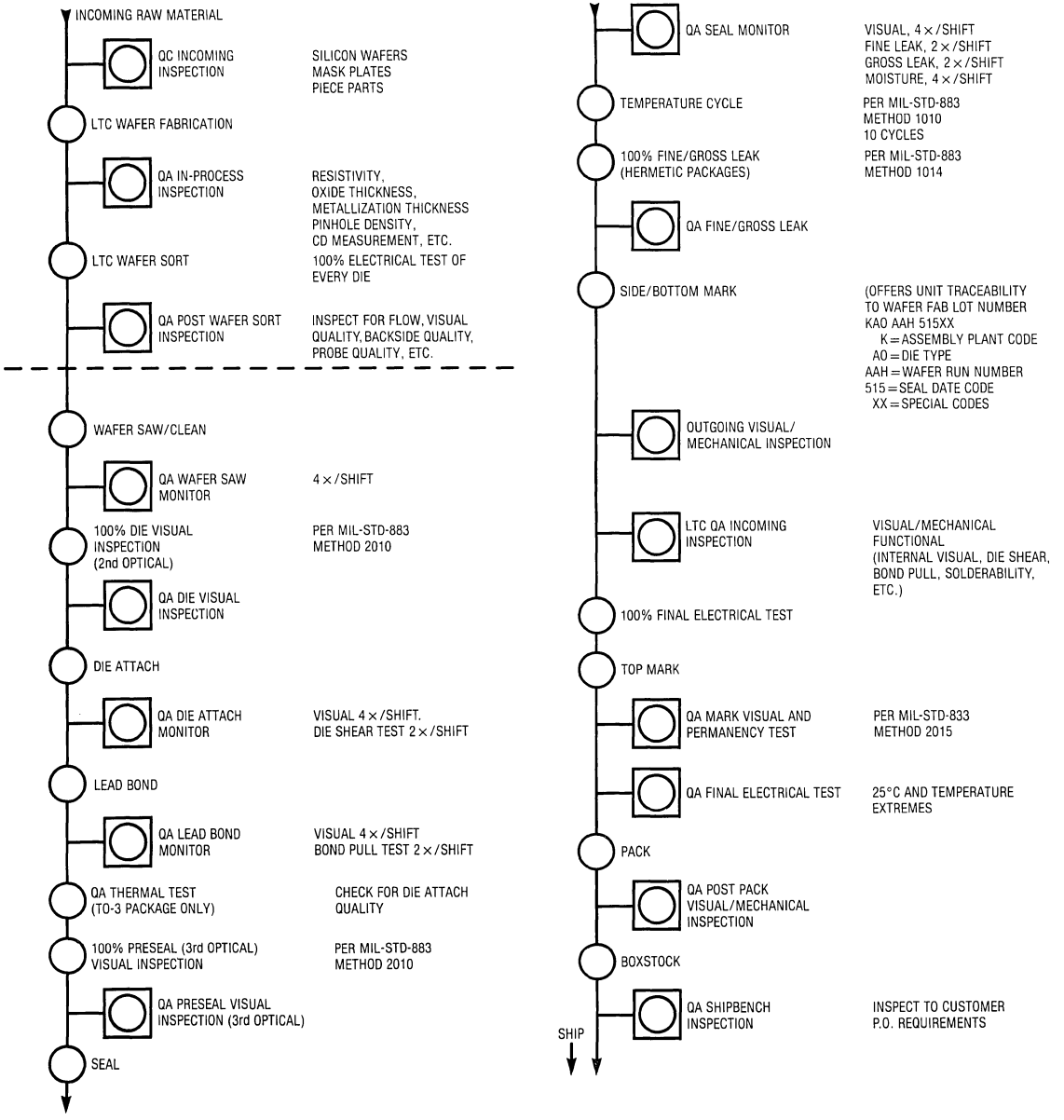


Based on the foregoing quality programs, Linear Technology Corporation is positioned to continuously improve our product quality and exceed the demands of our customers in the 80's and beyond.

Ship-To-Stock Program Flow



Quality Control Flow Diagram



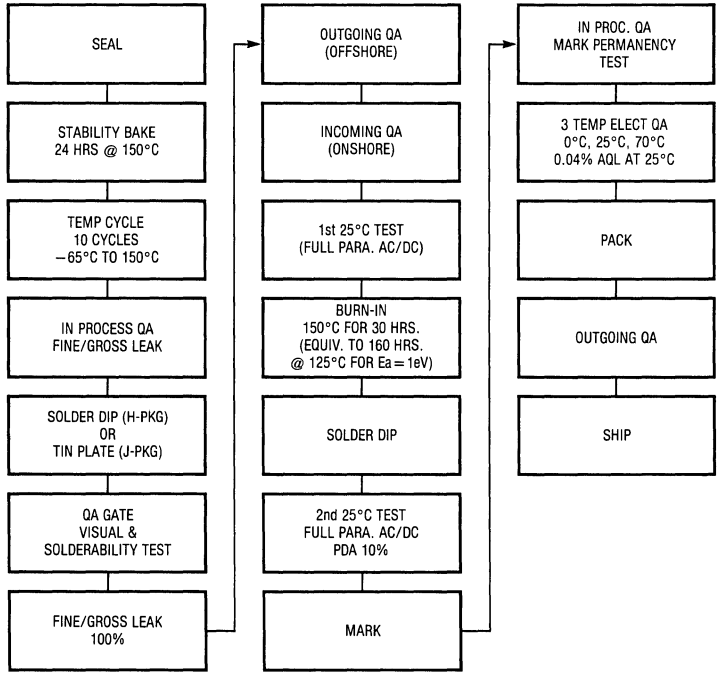
Linear Technology R-Flow

Reliability has been a key focal point at Linear Technology Corporation since our inception in 1981. Our standard product reliability is monitored closely and we have generated an extensive reliability data base for both hermetic and plastic devices. This data is published on a quarterly basis and we are seeing very low reliability failure rates in the 1 to 3 FIT range at 55°C.*

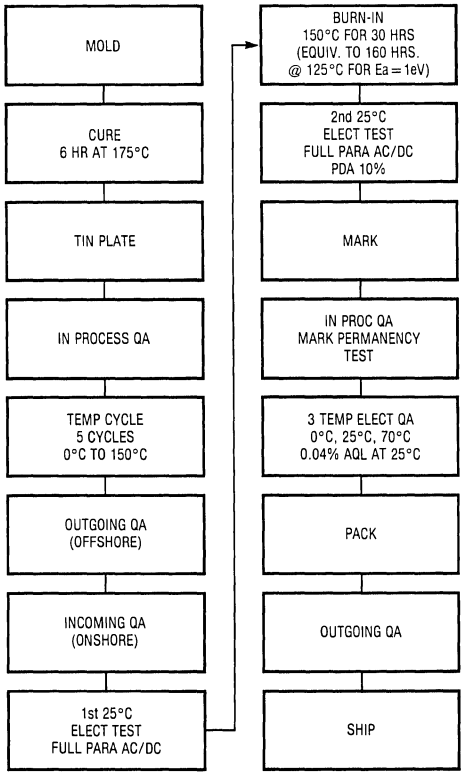
*Note: 1 FIT = 1 failure in 10^9 device hours.

In response to customer requests, we have added an even higher level of reliability screening for commercial hermetic and plastic components. LTC's R-Flow adds an equivalent 160 hours 125°C burn-in to the standard commercial process flow. Following burn-in, a 100% room temperature test is performed and a 10% PDA (Percent Defective Allowed) is applied. This PDA limit affords an additional level of insurance on a lot-by-lot basis and prevents the occasional disparate lot from being shipped for critical applications. The additional room temperature insertion also decreases the probability of any electrical defectives in the R-Flow lot.

R-Flow for TO-5 and CERDIP Packages



R-Flow for Plastic Dual-In-Line Packages



Introduction

As integrated circuit technologies achieve higher speed, smaller geometries, lower power and lower voltage, there is a tendency toward greater ESD (Electrostatic Damage) susceptibility. State-of-the-art CMOS ICs can be susceptible to as little as 50V, a static level that is way below the 500V to 15,000V commonly found in an ESD unprotected work environment. As these state-of-the-art ICs get designed into systems, the ESD susceptibility of system hardware also increases proportionately. Industry estimates of losses due to ESD are in the range of a few billion dollars annually.

It has become increasingly important for semiconductor manufacturers and users of semiconductor and other electronic components to fully understand the nature of ESD, the sources of ESD, and the impact on quality and reliability to effectively deal with this silent chip killer.

Linear Technology Corporation has successfully undertaken a simple but effective ESD Protection Program as part of an overall program designed to enhance product quality and reliability.

The objective of this tutorial is to provide increased ESD awareness by identifying the sources of ESD in the work environment and recommending keypoints for the successful implementation of an ESD program in your company.

The end result of a successful ESD program is the reduction of line failures, final inspection failures and field failures, improved manufacturing yields, improved product quality and reliability and lower warranty costs. We believe that an ESD Protection Program must be an important integral part of every electronic company's product quality and reliability program.

A copy of the Linear Technology ESD Protection Program Brochure can be obtained on request by writing directly to:

Linear Technology Corporation
1630 McCarthy Blvd.
Milpitas, CA 95035-7487

AN1 Understanding and Applying the LT1005 Multifunction Regulator

This application note describes the unique operating characteristics of the LT1005 and describes a number of useful applications which take advantage of the regulator's ability to control the output with a logic control signal.

AN2 Performance Enhancement Techniques for 3-Terminal Regulators

This application note describes a number of enhancement circuit techniques used with existing 3-terminal regulators which extend current capability, limit power dissipation, provide high voltage output, operate from 110VAC or 220VAC without the need to switch transformer windings, and many other useful application ideas.

AN3 Applications for a Switched-Capacitor Instrumentation Building Block

This application note describes a wide range of useful applications for the LTC1043 dual precision instrumentation switched-capacitor building block. Some of the applications described are ultra high performance instrumentation amplifier, lock-in amplifier, wide range digitally controlled variable gain amplifier, relative humidity sensor signal conditioner, LVDT signal conditioner, charge pump F to V and V to F converters, 12-bit A to D converter and more.

AN4 Applications for a New Power Buffer

The LT1010 150μA power buffer is described in a number of useful applications such as a boosted op amp, a feed-forward, wideband DC stabilized buffer, a video line driver amplifier, a fast sample-hold with hold step compensation, an overload protected motor speed controller, and a piezoelectric fan servo.

AN5 Thermal Techniques in Measurement and Control Circuitry

6 applications utilizing thermally based circuits are detailed. Included are a 50MHz RMS to DC converter, an anemometer, a liquid flowmeter and others. A general discussion of thermodynamic considerations involved in circuitry is also presented.

AN6 Applications of New Precision Op Amps

Application considerations and circuits for the LT1001 and LT1002 single and dual precision amplifiers are illustrated in a number of circuits, including strain gauge signal conditioners, linearized platinum RTD circuits, an ultra precision dead zone circuit for motor servos and other examples.

AN7 Some Techniques for Direct Digitization of Transducer Outputs

Analog-to-digital conversion circuits which directly digitize low level transducer outputs, without DC preamplification, are presented. Covered are circuits which operate with thermocouples, strain gauges, humidity sensors, level transducers and other sensors.

AN8 Power Conditioning Techniques for Batteries

A variety of approaches for power conditioning batteries is given. Switching and linear regulators and converters are shown, with attention to efficiency and low power operation. 14 circuits are presented with performance data.

AN9 Application Considerations and Circuits for a New Chopper-Stabilized Op Amp

A discussion of circuit, layout and construction considerations for low level DC circuits includes error analysis of solder, wire and connector junctions. Applications include sub-microvolt instrumentation and isolation amplifiers, stabilized buffers and comparators and precision data converters.

3rd Qtr '85

AN11 Designing Linear Circuits for 5V Operation

This note covers the considerations for designing precision linear circuits which must operate from a single 5V supply. Applications include various transducer signal conditioners, instrumentation amplifiers, controllers and isolated data converters.

4th Qtr '85

AN12 Circuit Techniques for Clock Sources

Circuits for clock sources are presented. Special attention is given to crystal-based designs including TXCOs and VXCOs.

3rd Qtr '85

AN13 High Speed Comparator Techniques

The AN13 is an extensive discussion of the causes and cures of problems in very high speed comparator circuits. A separate applications section presents circuits, including a 0.025% accurate 1Hz–30MHz V to F converter, a 200ns 0.01% sample-hold and a 10MHz fiber optic receiver. Five appendices covering related topics complete this note.

4th Qtr '85

AN14 Designs for High Frequency Voltage-To-Frequency Converters

A variety of high performance V to F circuits are presented. Included are a 1Hz to 100MHz design, a quartz stabilized type and a 0.0007% linear unit. Other circuits feature 1.5V operation, sine wave output and non-linear transfer functions. A separate section examines the trade-offs and advantages of various approaches to V to F conversion.

4th Qtr '85

AN15 Circuitry for Single Cell Operation

1.5V powered circuits for complex linear functions are detailed. Designs include a V to F converter, a 10 bit A—D, sample-hold amplifiers, a switching regulator and other circuits. Also included is a section on component considerations for 1.5V powered linear circuits.

AN16 Unique IC Buffer Enhances Op Amp Designs, Tames Fast Amplifiers

This note describes some of the unique IC design techniques incorporated into a fast, monolithic power buffer, the LT1010. Also, some application ideas are described such as capacitive load driving, boosting fast op amp output current and power supply circuits.

LINEAR TECHNOLOGY CORPORATION

1630 McCarthy Blvd., Milpitas, CA 95035
Phone: (408) 942-0810
FAX: (408) 434-0507
Telex: 499-3977

IM/GP/BC 1085 50M